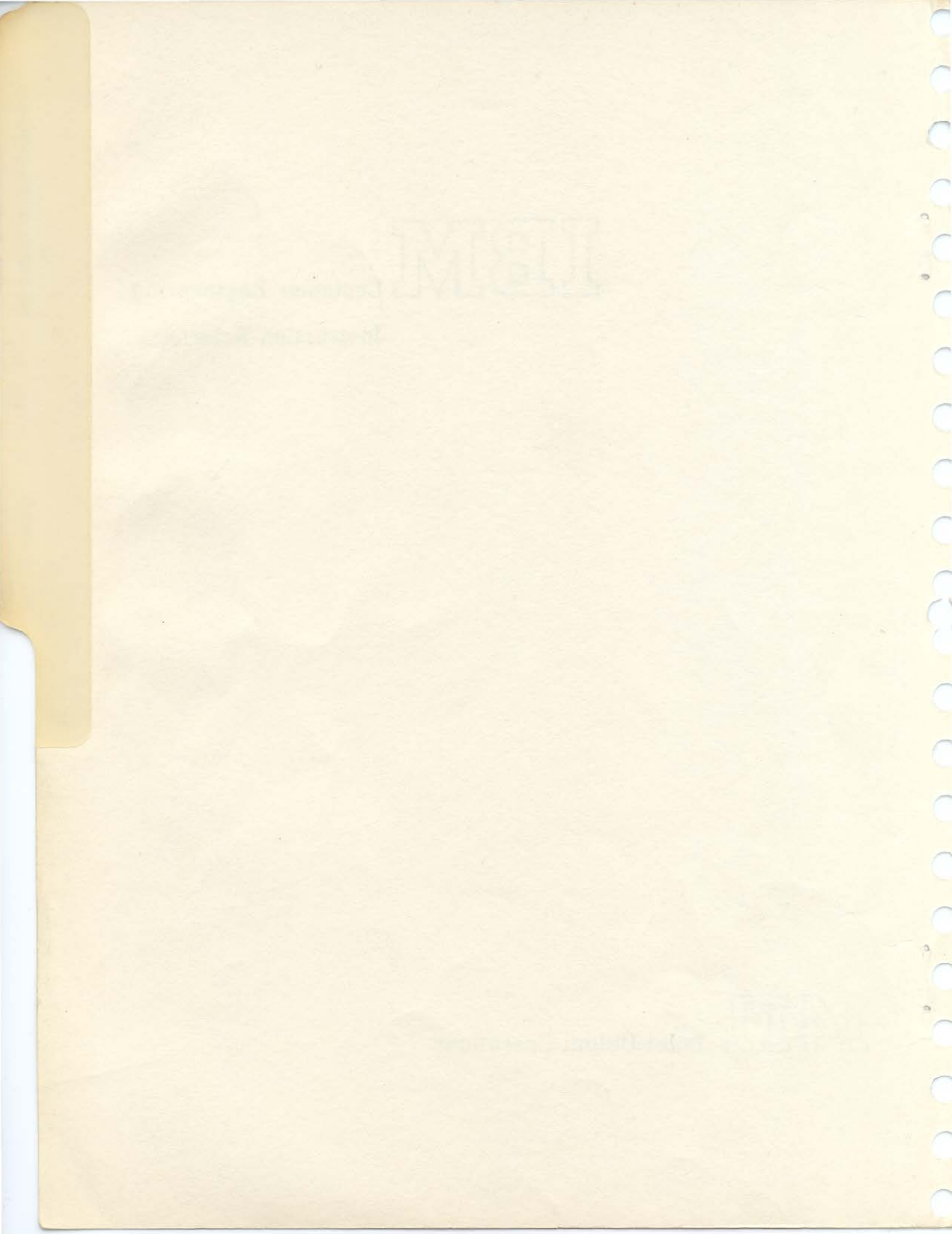


IBM Customer Engineering
Instruction-Reference

1411 Input-Output Operations

223-2692

1411 Input-Output Operations



IBM

Instruction-Reference

1411 Input-Output Operations

Preface

This manual provides instructional and reference material for input-output (I-O) operations of the IBM 1411 Processing Unit. The manual contains five logical segments.

1. "I-O Principles of Operation" presents basic concepts of data flow, data control, and channel status indicators.

2. "Channel Data Register Controls" presents register operation as a functional unit because operation is the same for all I-O devices.

3. "I-O Sequence" presents the machine logic highlights of a move or load command.

4. Specific IBM 1411 I-O operations — this manual describes 1411 functions, and tie-in for the following IBM I-O devices (Page 85).

- a. 1402 Card Read Punch
- b. 1403 Printer
- c. 1011 Paper Tape Reader
- d. 1405 Disk Storage Unit
- e. 1311 Disk Storage Unit

5. The "Reference Section" in the back of the manual contains status indicator charts and condensed logic.

This manual does not cover operation of the I-O devices; refer to the appropriate manual for the I-O devices.

1411 functions for devices not listed above are presented in the manual for that device. A list of IBM 1410 system manuals is in the *IBM 1410 Customer Engineering Handbook*, Form 223-2588, and in IBM 1410 CEM Service Aid 72.

Users of this manual should be familiar with the information presented in *IBM 1410 Systems Fundamentals*, Form 223-2589.

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Input-Output Principles of Operation

Input-output principles apply to all input-output (I-O) devices of the IBM 1410 Data Processing System. The basic I-O move or load command (M/L XXX BBBB d) is used with all I-O devices. Disk storage devices (IBM 1301, IBM 1311, and IBM 1405) operate similarly to other I-O devices except that an address transfer operation precedes the transfer of data to the disk unit.

I-O commands control data transfer between an I-O device and the IBM 1411 Processing Unit (CPU). Data transfer from an I-O device to the CPU is called input operation. Data transfer from the CPU to an I-O device is called output operation. Some special I-O commands do not transfer data; instead they control I-O unit functions such as paper feeding (printer) and stacker pocket selection (reader). These document control commands for card I-O units, and unit control commands for tape units, are described in the section for the I-O device using that command.

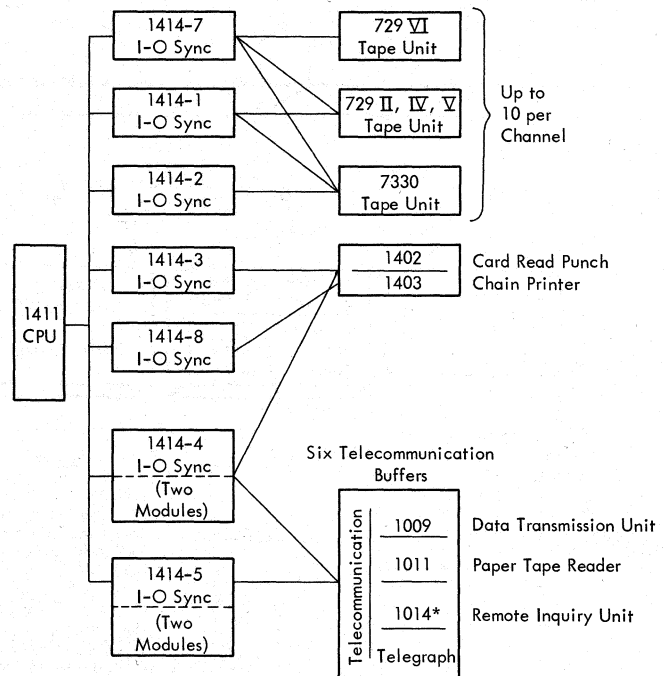
Input-Output Units

A number of I-O units are available as attachments to the IBM 1410 Data Processing System (Figures 1 and 2). I-O units are described in *IBM 1410 Principles of Operation*, Form A22-0526, and *IBM Telecommunications Equipment with IBM 1410 System*, Form A22-0525. The I-O units share the same basic instruction word and the same basic data flow path.

Input-Output Synchronizers

Because the I-O units and the CPU operate at different speeds, most I-O units have a synchronizer unit that controls data transfer between the I-O unit and the CPU, and supervises operation of the I-O unit. Synchronizers provide temporary storage for data being transferred between the I-O unit and the CPU. Synchronizers, then, provide buffer storage for input-output data. Some synchronizers have only a single-character buffer, while others, such as the synchronizer for the IBM 1402 Card Read Punch, have 80-position core storage buffers. The term *buffer* as used in this manual refers to a synchronizer core storage unit with 80 or more positions of storage.

The buffering of I-O units reduces CPU waiting time during transfer of data between the CPU and a relatively slow I-O unit; for example, compare the data

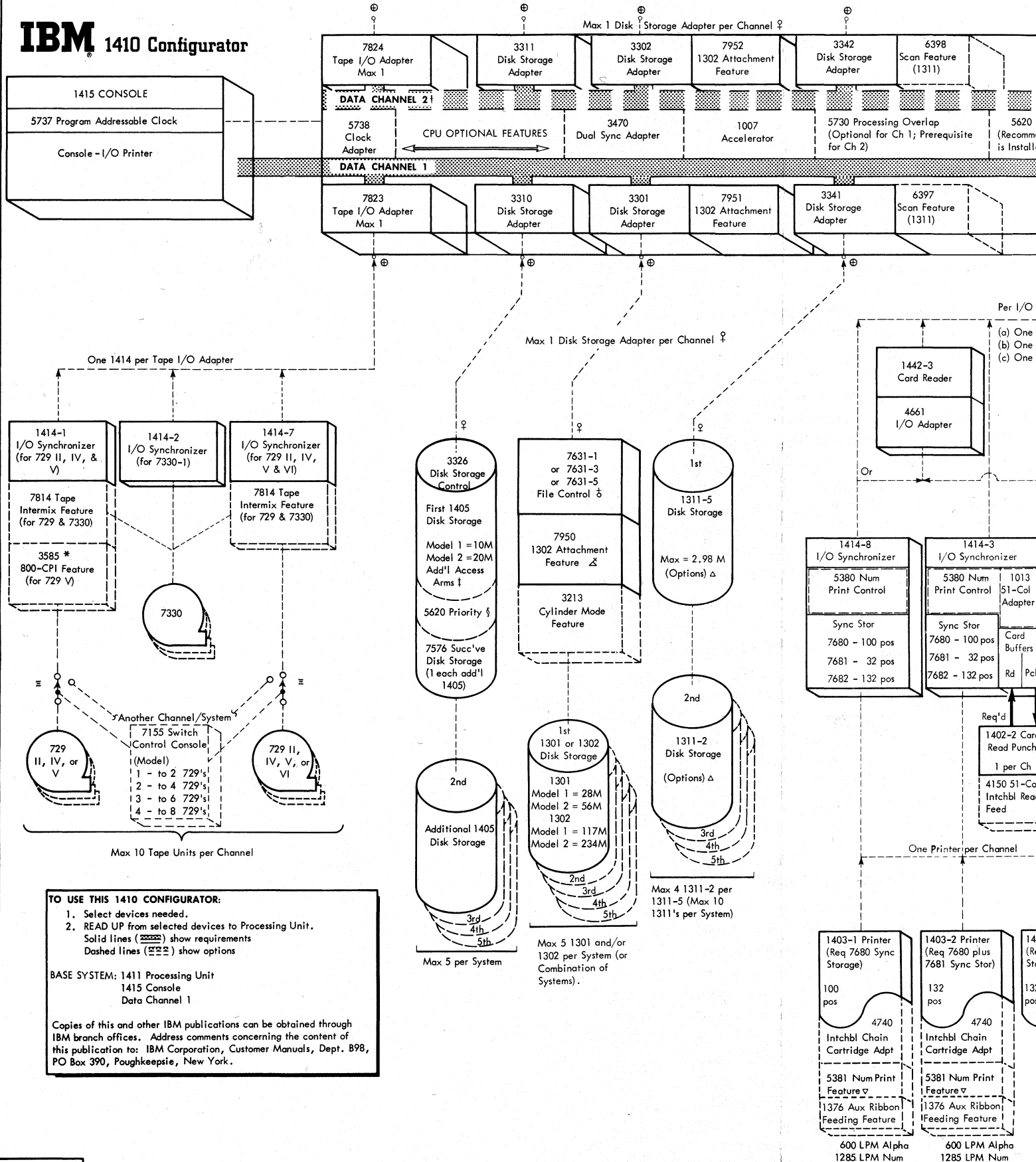


*Up to 20 on System

Figure 1. Input-Output Units and Synchronizers

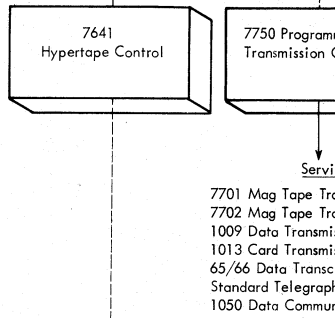
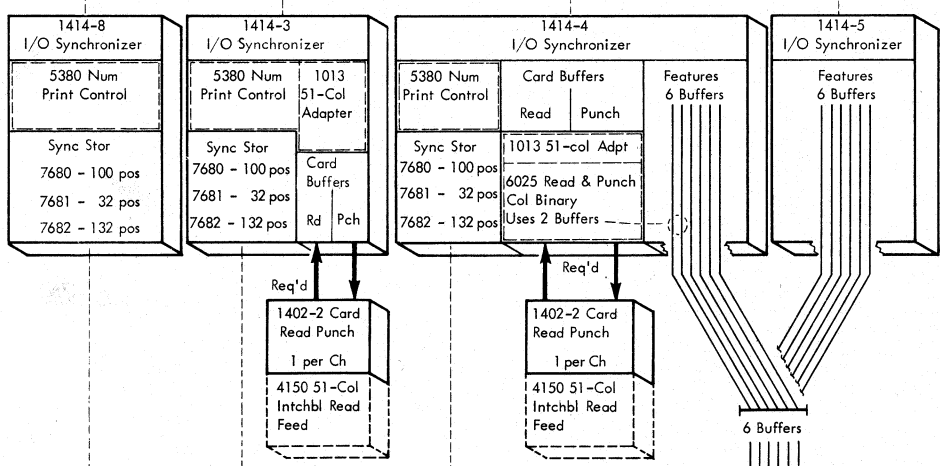
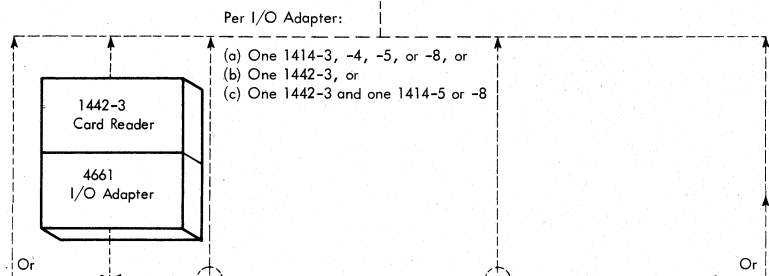
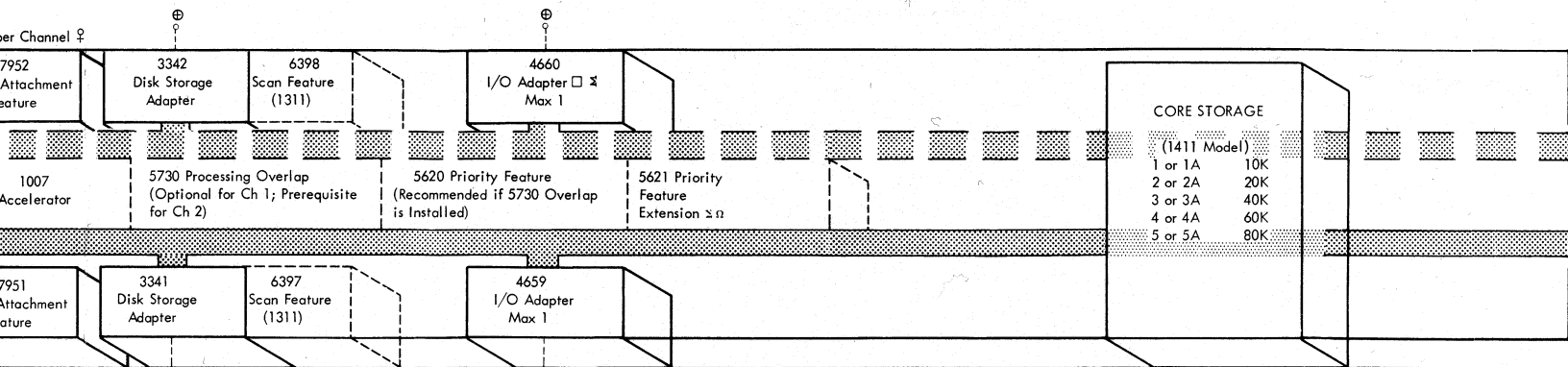
transfer times of unbuffered versus buffered IBM 1402 operation. If data were transferred from the 1402 reader directly to the CPU, a total of 75,000 microseconds (card feed cycle) would be required to read one card and transmit the data to the CPU. If the card data are first loaded into the synchronizer buffer, the time required to transmit 80 characters from the buffer to the CPU is only 880 microseconds because data are transferred at an 11-microsecond rate (Figure 3). The IBM 1410 system employs buffered operation for the IBM 1402 Card Reader Punch and the IBM 1403 Printer. For the 1410 to benefit from input unit buffering, the interval between read commands must be long enough to permit the input unit to reload the buffer. The CPU is free to process data during the interval. For the 1410 to benefit from output unit buffering, the interval between write commands must be long enough to permit the output unit to unload the buffer. The CPU is free to process data during the interval.

IBM 1410 Configurator

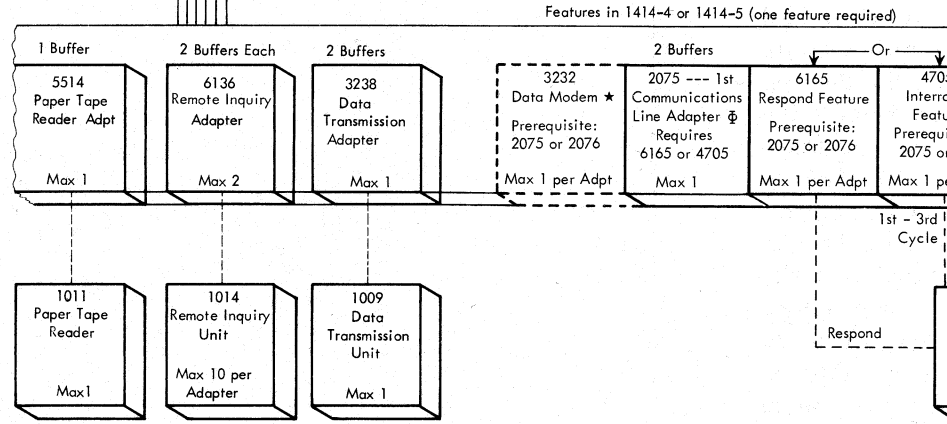
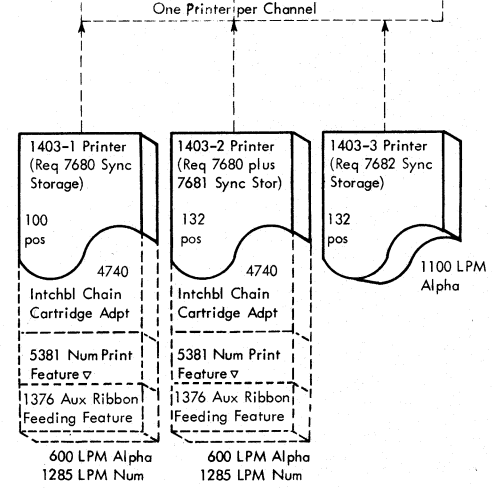
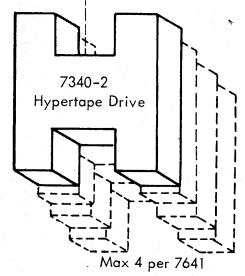


NOTES

* 3586 if on Data Channel 2
 † Prerequisite: 3470 Dual Sync Adapter.
 ‡ Optional and recommended. Prerequisite: 5620 Priority on 1411.
 ‡ Optional features on 1311-5: 6400 Seek Overlap, 6396 Scan Disk, and 8011 Track Record; on 1311-2: 6400 Seek Overlap only. Seek Overlap on 1311-5 necessitates Seek Overlap on all companion 1311-2's. 6396 Scan Disk on 1311 necessitates 6397 or 6398 Scan Feature on CPU.
 ∇ Prerequisites: 4740 on printer and 5380 on 1414 I/O devices and features shown attached to Ch1 also be attached to Channel 2 adapters, with 7631-3 permits sharing (a) 1301's with 7000 series 7010 or 7072 (b) 1302's with 7000 series system or 7072. 7631-5 permits shared use by a 7010
 ⚡ Not available on 7631's with serial number 10



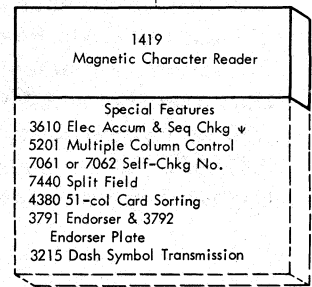
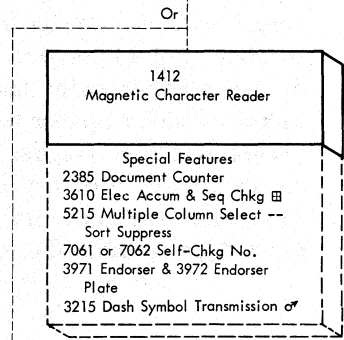
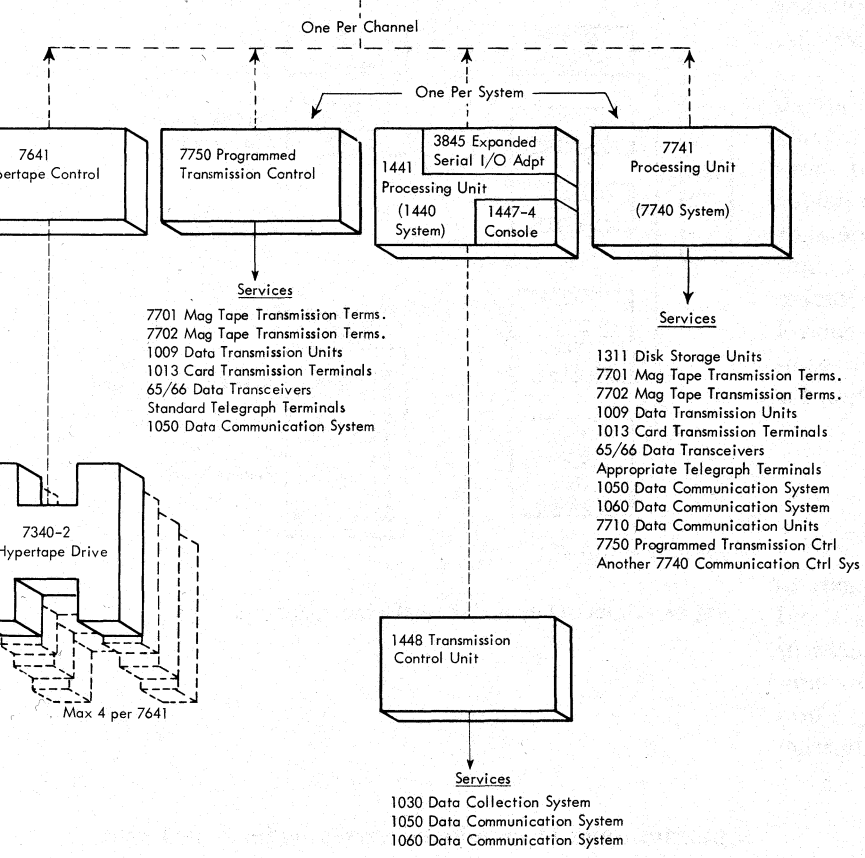
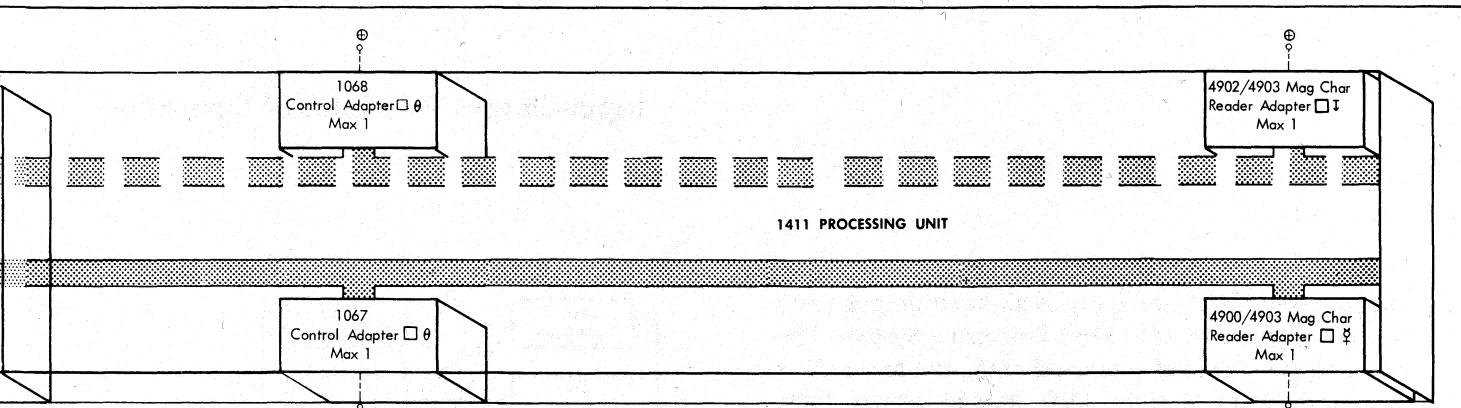
- 7701 Mag Tape Trans
- 7702 Mag Tape Tran
- 1009 Data Transmiss
- 1013 Card Transmiss
- 65/66 Data Transce
- Standard Telegraph
- 1050 Data Communi



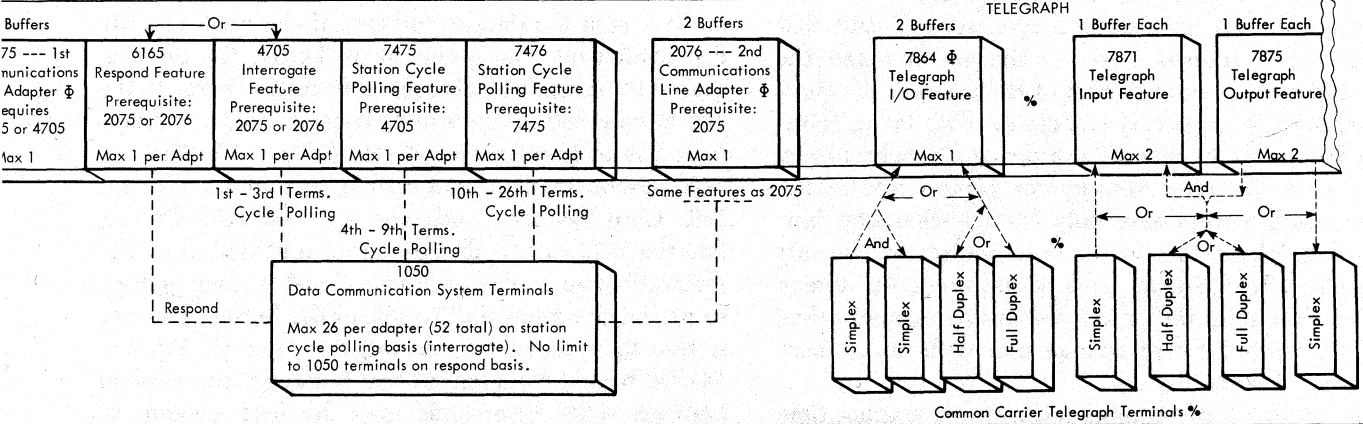
▽ Prerequisites: 4740 on printer and 5380 on 1414.
 ● I/O devices and features shown attached to Channel 1 adapters can also be attached to Channel 2 adapters, with same restrictions.
 ⚬ 7631-3 permits sharing (a) 1301's with 7000 series systems except 7010 or 7072 (b) 1302's with 7000 series systems except 7010, 7070, or 7072. 7631-5 permits shared use by a 7010 or another 1410.
 ✕ Not available on 7631's with serial number lower than 12000.

⊠ Prerequisites: 4660 I/O adapter and 5620 Priority.
 ⊕ Prerequisites: 5620 Priority and 5730 Overlap.
 □ Prerequisite: 1411 Model A1 through A5.
 ✕ 5621 Priority Feature Extension required to extend system priority-interrupt capabilities to I/O operations transmitted through 4660 I/O adapter (Channel 2).
 † 4902 used if Ch 1 has no 4900; 4903 used if Ch 1 already has a 4900.

‡ 4900 used if Ch 2 has no 4902; 4903 used if Ch 2 already has a 4900.
 ⊞ Prerequisite: 5215 Multiple Column Selection.
 ⊟ Prerequisite: 5201 Multiple Column Selection.
 † Not available on 1412's with serial number 2075 or 2076.
 * Required for 2075, 2076 if 1050 terminating wires of 50 ft -- 8 miles. (Under 50 ft over 8 miles requires common carrier.)



4 or 1414-5 (one feature required)



4900 used if Ch 2 has no 4902; 4903 used if Ch 2 already has a 4902.
 Prerequisite: 5215 Multiple Column Select -- Sort Suppress feature.
 Prerequisite: 5201 Multiple Column Control feature.
 Not available on 1412's with serial number lower than 10058.
 Required for 2075, 2076 if 1050 terminals use customer-provided wires of 50 ft -- 8 miles. (Under 50 ft permits direct interface; over 8 miles requires common carrier.)

⊕ Communications line adapters and telegraph features cannot be installed on same 1414 (use the same space).

% Total buffers for telegraph are: minimum of 2, maximum of 4. The minimum 2 must be 1 in and 1 out (feature 7864). The additional 1 or 2 features can be one or two 7871 in, one or two 7875 out, or one 7871 in and one 7875 out.
 Simplex = one way only
 Half Duplex = two ways, one at a time
 Full Duplex = two ways simultaneously.

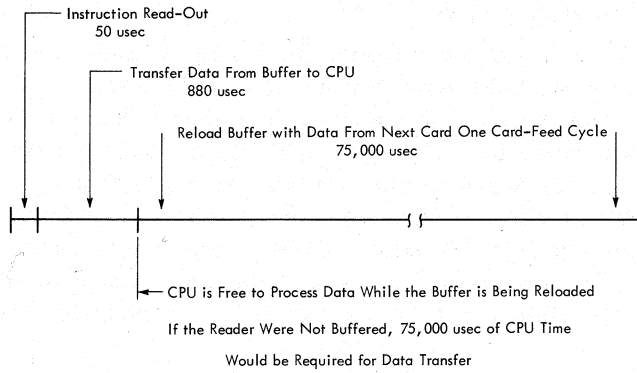


Figure 3. Buffered Reader Operation

Input-Output Channels

An I-O channel consists of input and output data lines, channel data registers 1 and 2, and control lines between the CPU and the I-O devices. Channel 1 (E-channel) is a standard feature on the IBM 1410. Channel 2 (F-channel) is an optional feature. Each channel has two eight-bit, single character channel data registers that provide buffering for overlap operation, and w-m-s conversion for data transfer operations with I-O devices that cannot handle word marks. Because the

two channels operate the same, only E-channel operation is described.

Data Flow

Channels 1 and 2 are capable of input and output operation, but not at the same time. Figure 4 shows input data flow on E-channel and output data flow on F-channel. Note that data transfer on input or output is always from data register 1 into data register 2 thus permitting the same register transfer controls to be used for both input and output operation. The processing overlap feature, described later, permits both channels to operate while the CPU is processing data.

Input: During E-channel input operation, the input data lines carry information from the I-O unit to E-channel data register 1 (E-1). Data in E-1 are transferred to E-channel data register 2 (E-2), gated to A-channel, assembly channel, and into the core storage of the IBM 1411. Input data are checked for odd parity on A-channel and the assembly channel; F-channel input operation is similar.

Output: During an F-channel output operation, information is read out of the core storage of the IBM 1411; gated to the B-channel, assembly channel, and into F-1; information appears on the output data lines after an F-1 to F-2 data transfer. Output data are checked for odd parity on B-channel and the assembly channel; E-channel output operation is similar.

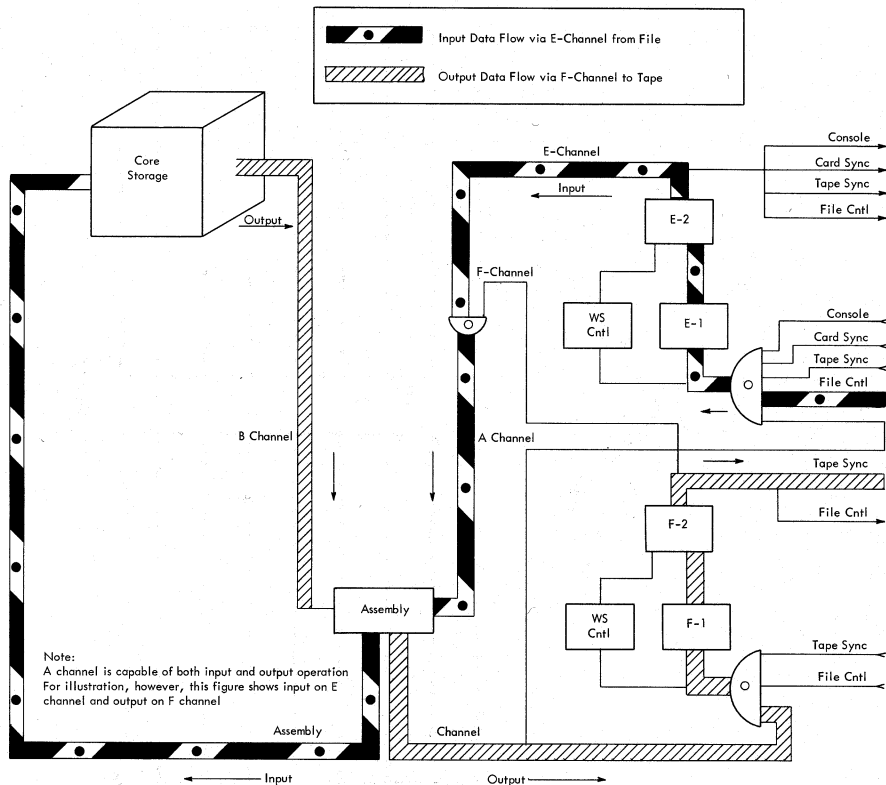


Figure 4. I-O Data Flow

Data Transmission

An I-O instruction controlling data transfer must specify one of two modes of transmission: load mode or move mode. Load mode operation processes word marks and word separator characters. Move mode operation ignores word marks; word separator characters are transferred the same as any binary coded decimal (BCD) character (Figure 5).

EIGHT-BIT DEVICES

The core storage of the IBM 1411 is an eight-bit device because it can write a word mark (WM), along with a BCD character, into a single core storage location. A BCD character with a WM is called a WM character. The data registers and data buses of the 1411 also can handle eight-bit characters. The WM bit is included in the character bit count, and odd parity is maintained.

The IBM 1415 Console and the disk storage units (IBM 1301, IBM 1311, and IBM 1405) are eight-bit de-

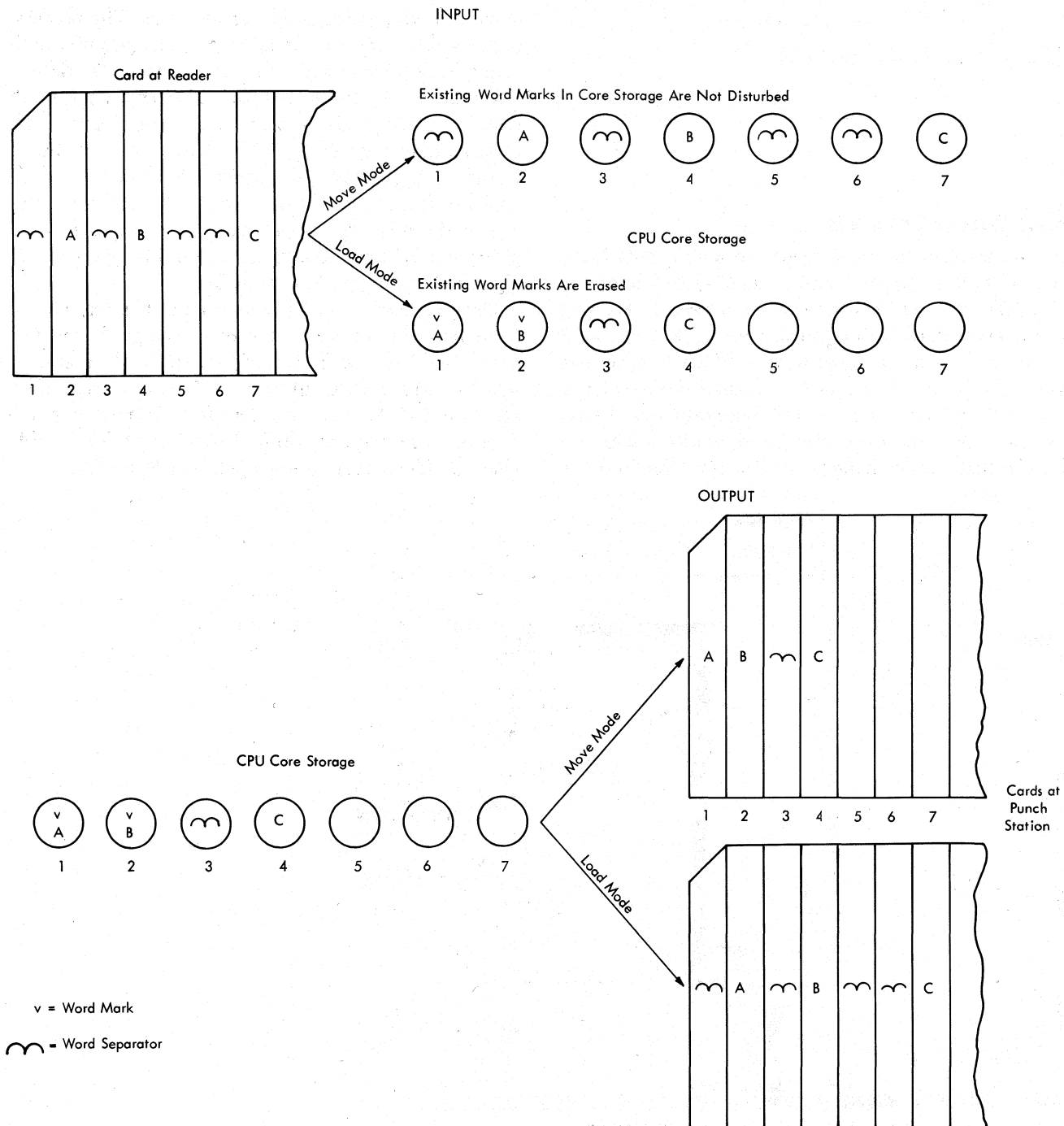


Figure 5. Word Separator Processing

vices and hence can handle word mark characters. All other I-O units are seven-bit devices and can handle only seven-bit characters.

SEVEN-BIT DEVICES

All I-O units except the disk storage units are seven-bit devices. They cannot handle word mark characters; for example, the 1402 reader is a seven-bit device because a WM-A (A) that requires only a single core storage location in the 1411 requires two locations (card columns) when represented in the IBM card code. One column contains the card code representation of the word mark called a word separator character (0, 5, 8), and the following column contains the card code representation of the A (12, 1).

MOVE MODE

Word marks are ignored in move mode operation. Characters are transferred on a one-for-one basis; a single input character results in a single 1411 core storage character, and a single 1411 core storage character results in a single output character.

Input: During move mode data transmission (Figure 6), punched card information from the 1402 reader is encoded into BCD as it is being read into the 1414 buffer, and the information is transferred, unchanged, to core storage. Existing word marks in core storage are retained.

Output: Only zone and numeric portions of characters are transferred to the buffer of the IBM 1414 Input/Output Synchronizer (Figure 7). The assembly controls invert the C-bit and ignore the word mark of B-channel WM characters, removing the word mark, and maintaining odd parity of characters placed on the assembly channel. Characters on the assembly channel are gated into the channel registers. The BCD information in the 1414 buffer is decoded into IBM card code as it is being punched.

LOAD MODE

Word marks are transmitted along with the associated BCD characters. Characters are transferred on a one-for-one basis between the CPU and eight-bit devices. Characters transferred between the CPU and seven-bit devices require special handling if they are WM characters or ws characters. During input operation with a seven-bit device, ws characters are converted to word marks; during output operation, word marks are converted to ws characters. Conversion occurs within the channel data registers. Characters other than ws characters or WM characters are transferred on a one-for-one basis. A description of load mode channel operation for seven-bit I-O devices follows.

Input: Word separator characters are converted into word marks, combined with the following character,

and the resultant WM character is transferred to the 1411 core storage (Figure 6). Exception: two consecutive word separator characters result in a single word separator character with no word mark (C, A, 8, 4, 1) being transferred to 1411 core storage. A WM-ws character (WM, A, 8, 4, 1) cannot be read into the CPU from a seven-bit I-O device.

Output: WM characters are transmitted to the I-O device as two characters. The first character is a ws character representing the word mark; the second character is the BCD portion of the WM character. Exception: one ws character in 1411 core storage results in two ws characters being transferred to the I-O device. A word mark over a ws character (Figure 7 — note circled WM) has no effect on the output character. A ws character, with or without a word mark, results in two word separator characters being transferred to the I-O device.

Channel Data Registers

The 1411 has two eight-bit, single-character channel data registers for each channel; E-1 and E-2 registers for E-channel and F-1 and F-2 registers for F-channel. The registers provide two-character buffering (necessary for overlap operation), WM-ws conversion for seven-bit I-O units, and parity correction during WM-ws conversion. Parity inversion for even parity tape operation is made on the data lines entering and leaving the channel data registers.

Because operation on both channels is the same, only E-1 and E-2 functions are described here. During input operation the CPU tries to keep E-1 and E-2 empty, and during output to keep E-1 and E-2 full. The channel data registers are never reset; a set pulse enters a character into the register, replacing the existing character. Actual circuit operation is described in the Channel Data Register Controls section.

MOVE MODE CHARACTER PROCESSING

All E-channel data, input or output, is first set into E-1, is transferred to E-2, and appears on the channel data lines. The data are then available to A-channel (input) or to the I-O devices (output). Load mode operation with eight-bit I-O devices and any move mode operation employ a simple E-1 to E-2 data transfer operation (Figure 8) controlled by two lines:

Copy E-1 BCD to E-2

Copy E-1 WM and C-bit

The copy lines determine what information is transferred when the set pulse occurs. Set pulses are generated from the CPU clock, which runs continuously unless the CPU is in stop status. The CPU logic ring, however, runs only when a CPU I-O data cycle is required (unoverlapped operation).

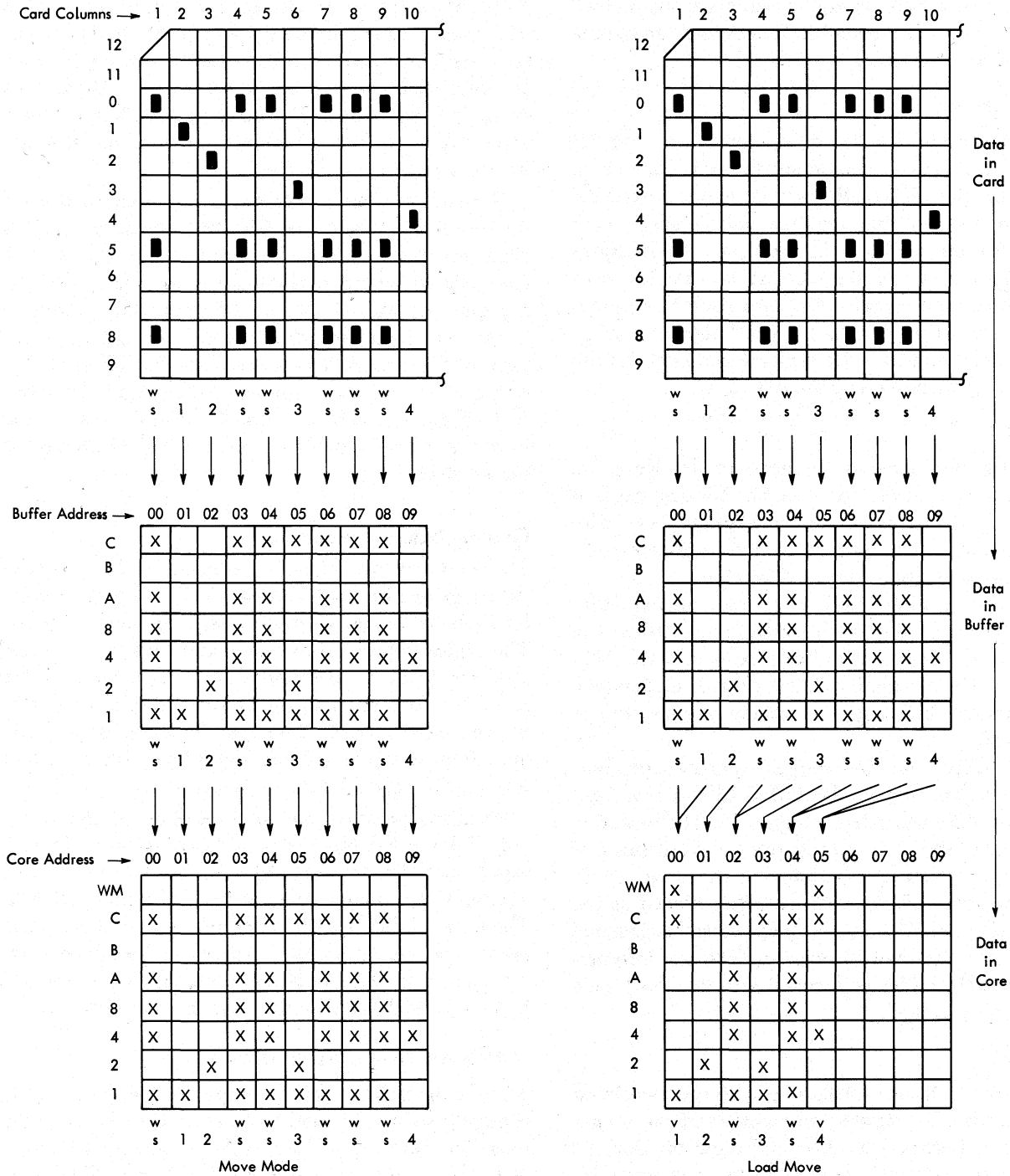


Figure 6. Data Transmission - Input

LOAD MODE CHARACTER PROCESSING

Load mode operation with a seven-bit i-o device causes the channel data registers to operate in word separator mode.

Two additional control lines are used in word separator mode:

Set E-2 word separator (sets a ws character into E-2)
Copy invert E-1 WM and C-bit

Input: One of three cases exists during input load mode:

1. E-1 character is not a ws character.
2. E-1 character is a ws character followed by a different character.
3. E-1 character is a ws character followed by another ws character.

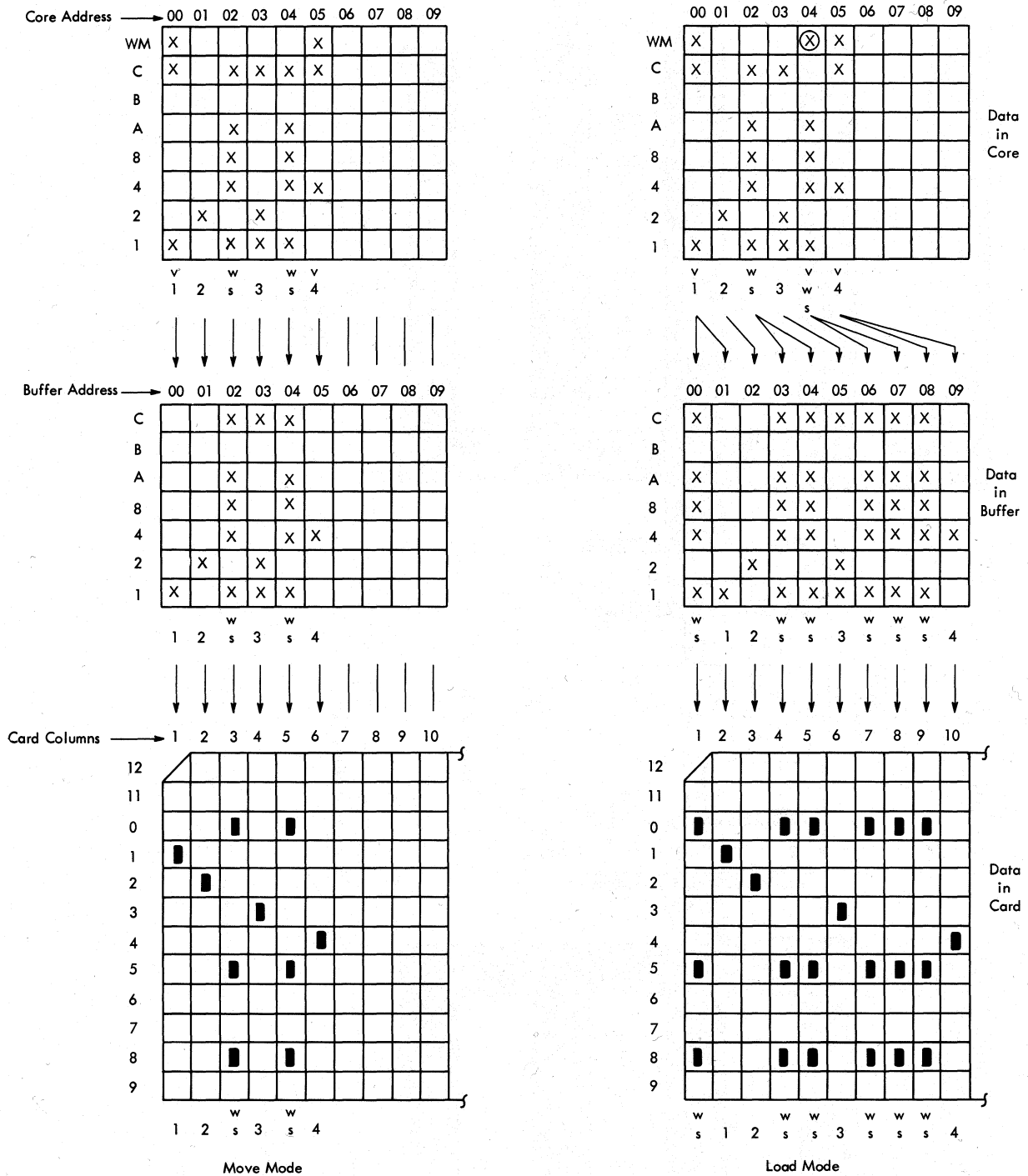


Figure 7. Data Transmission - Output

Case 1 -

Characters are copied the same as in move mode.

Case 2 -

- a. A ws in E-1 sets a ws into E-2 (the ws in E-2 serves no purpose during input operation).
- b. The \overline{bcd} portion of the following character is copied from E-1 into E-2.

- c. The E-1 wm and C-bit lines (no wm is present) are inverted and copied into E-2, producing an odd parity wm character in E-2 that is transferred to 1411 core storage. Note that steps b and c replace the ws character in E-2 before the contents of E-2 are transferred to 1411 core storage.

→ Data Flow →

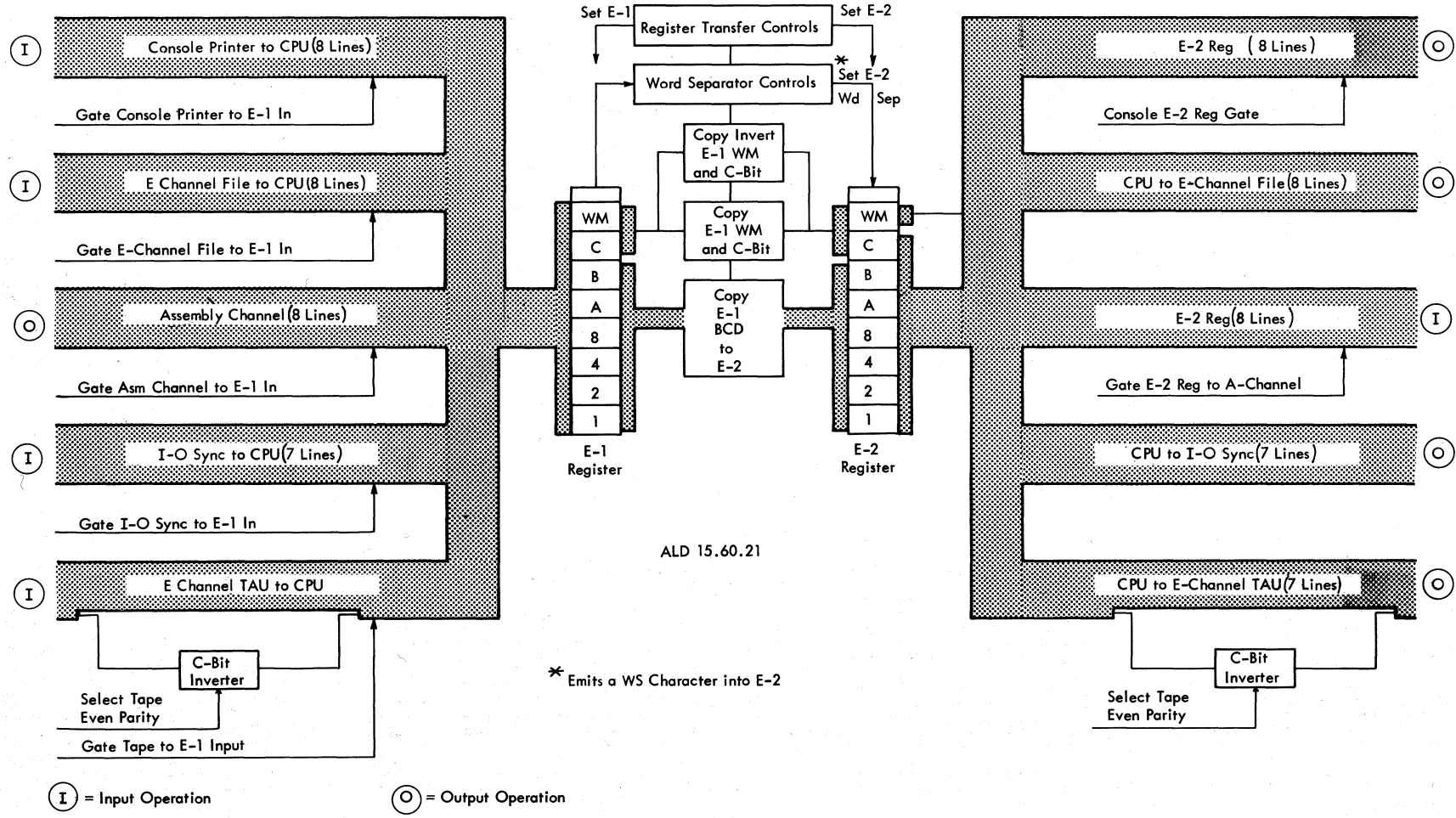


Figure 8. Channel Data Registers

White Indicators

Red Indicators

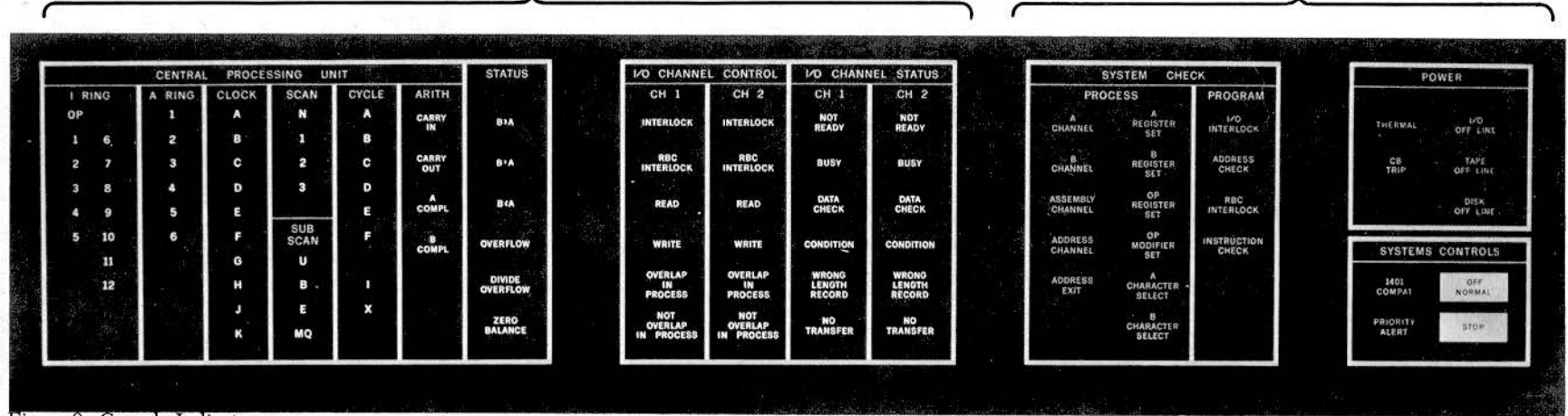


Figure 9. Console Indicators

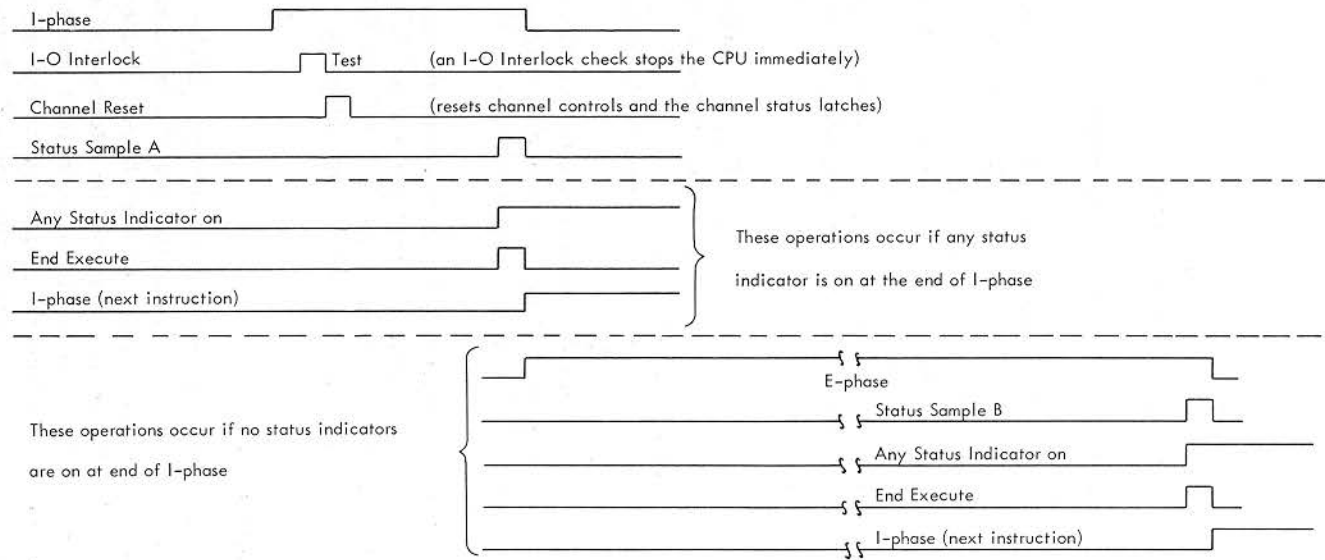


Figure 10. Channel Status Indicators

Case 3—

- a. A ws in E-1 sets a ws into E-2 (the ws in E-2 serves no purpose during input operation).
- b. The BCD portion of the following character is copied from E-1 into E-2.
- c. The E-1 WM and C bit (no WM present) are copied into E-2, producing an odd parity character that is transferred to 1411 core storage. Note that steps b and c replaced the first ws character in E-2 with the second ws character before the contents of E-2 were transferred to 1411 core storage. (two ws characters were combined into one).

Output: One of four cases exists during output:

1. E-1 character is not a ws or WM character.
2. E-1 character is a WM character.
3. E-1 character is a ws character.
4. E-1 character is a WM-ws character.

Case 1—

Characters are copied as in move mode.

Case 2—

- a. A WM in E-1 sets a ws into E-2. No further register operation occurs until the ws is received by the output unit.
- b. The BCD portion of the WM character is copied from E-1 to E-2.
- c. The WM and C-bit lines are inverted and copied from E-1 into E-2, removing the WM and maintaining odd parity.

Case 3—

- a. A ws in E-1 sets a ws into E-2. No further register operation occurs until the ws is received by the output unit.
- b. The BCD portion of the ws character is copied from E-1 into E-2.
- c. The WM and C-bit (no WM present) are copied from E-1 into E-2, producing another ws character in E-2 from the single ws character in E-1.

Case 4—

A WM-ws character in E-1 is processed the same way as a ws character except the WM and C-bit lines are inverted when copied from E-1 into E-2, removing the WM and maintaining odd parity.

Channel Status Indicators

Each I-O channel has six status indicators (latches), with console indicating lamps, that reveal information about the previous operation on that channel (Figures 9 and 10). The six indicators can be interrogated at any time by the program. All I-O units on a channel are served by the same six channel status indicators, although some units, such as the IBM 1403 Printer, do not use all six indicators. Because operation is the

same for both channels, only E-channel status indicator operation is described.

The basic I-O command provides three distinct functions:

1. *Selecting*

- a. Selects I-O channel
- b. Selects I-O unit
- c. Selects mode of transmission (move or load)
- d. Selects input or output
- e. Selects overlap or unoverlap

2. *Sensing*

- a. Senses status of I-O devices
- b. Senses status (or validity) of data transfers

3. *Executing*

An I-O unit is selected and sensed (its status is sampled; if the I-O unit indicates proper status, CPU executes the I-O command).

When an I-O unit is sensed, channel status indicators are set to "remember" the status of the selected unit.

Early in the I-phase of an I-O operation, the six status latches are reset. Twice during an I-O operation, the latches are set by sampling selected conditions; they retain this information until another I-O operation occurs on that channel. The conditions selected for sampling are determined by the type of I-O unit selected and by the direction of data flow (input or output). Because of this selective method of setting the status latches, only a general description of status latch operation can be given here. For specific information on conditions that set the status latches, refer to the status indicator charts and the condensed logic in the reference section of this manual.

The status latches must be interrogated by the program between I-O operations because their information is lost when the latches reset during the next I-O operation. A failure of the program to interrogate the status latches is detected by an automatic test within the CPU, resulting in a system check that causes a master error to stop the CPU with the I-O interlock indicator glowing in the system check section of the IBM 1415 Console (Figure 9). Examples of I-O programming sequences are given in a following section which describes the I-O interlock check.

Status latches are set at only two times during an I-O operation, either at the end of I-phase or at the end of E-phase. A-status indicators are set at the end of I-phase (status sample A); B-status indicators are set at the end of E-phase (status sample B). These indicators are set conditionally; that is, only when the selected conditions are present at status sample time. Figure 10 shows the six channel status indicators grouped in their most common arrangement. Note that the condition indicator and the no transfer indicator may be either A-status or B-status indicators, depend-

ing on the I-O operation. The selected conditions represented by the condition and the no transfer indicators vary according to the type of I-O unit selected and according to the direction of data flow, input or output. In the following description, the condition and no transfer indicator functions are briefly described for the 1402 reader operation. The four remaining status latches: not ready, busy, data check, and wrong length record, represent much the same conditions for all I-O operations.

A-STATUS INDICATORS (I-PHASE INDICATORS)

A-status latches are set at status sample A time (end of I-phase), and they indicate the status of the selected unit, in contrast to the B-status latches which indicate the status of the data transfer operation. If any status latch is on at the end of I-phase, the operation is ended (no E-phase) and the program proceeds to the next sequential instruction (Figure 10).

Not Ready: The ready line from the selected I-O device is gated to the channel ready bus. If the ready line is active, the ready bus becomes active, blocking the set of the channel not ready status latched.

Busy: The busy line from the selected I-O device is gated to the channel busy bus. With both the busy bus and the ready bus active, status sample A turns on the channel busy status latch.

Condition: The condition status latch is an A-status indicator for all channel operations that transfer data between the CPU and the IBM 1414, Models 3, 4, 5, and 8. In 1402 reader operation, for example, reader end-of-file status is gated to the channel condition bus. With the condition bus and the ready bus both active, the condition status latch is turned on at status sample A time.

B-STATUS INDICATORS (E-PHASE INDICATORS)

B-status latches are set at status sample B time (end of E-phase), and they indicate the status of the data transfer operation. In contrast to the A-status indicators, they have no effect on subsequent CPU operation except through a programmed branch as a result of interrogating the status indicators.

Data Check: A data error, and in some cases a control circuit error, from an I-O device is gated to the channel check bus, gating the set of the channel check status latch at status sample B time. During input operation, a parity error character on the A-channel sets the check status latch immediately because the error condition is gone when the check bus is sampled at status sample B time.

An *asterisk insert* switch on the 1415 CE panel is available to the operator or Customer Engineer for use in handling parity error input characters during input

operation. With the asterisk insert switch off, a parity error input character detected on the A-channel causes a master error which stops the CPU. With the asterisk insert switch on, a parity error input character detected on the A-channel causes an asterisk to be stored in place of the error character. Master error is blocked and the operation continues. The channel check status latch is *always* turned on by a parity error input character on the A-channel, regardless of the setting of the asterisk insert switch.

Parity error characters can be read into core storage by switching asterisk insert switch to off, switching the print out control switch to INHIBIT, and turning the check control switch to RESTART.

Wrong Length Record: Input and output field lengths in 1411 core storage are controlled by a GM-WM character in the 1411 core storage location following the last position of the field. The GM-WM is placed in the input or output field by programming or by the console operator. When the GM-WM is sensed during input or output operation, an internal end of transfer condition occurs which terminates transfer of data between 1411 core storage and the channel data registers. If no GM-WM is placed in an input or output field, a wrong length record indication occurs during I-O operations using those fields.

The wrong length record (WLR) status latch operates as follows:

1. *Input operation:* The number of input characters must correspond to the number of positions in the input field or the WLR status latch will be turned on at status sample B time. No more characters are transferred from the channel data registers to 1411 core storage after the internal end of transfer condition occurs.

2. *Output operation with fixed-length record I-O devices:* The number of characters in the output field must correspond to the record length specified for the selected I-O device, or the WLR status latch is turned on at status sample B time. When a WLR indicator is turned on during output operation with a buffered I-O unit, the output unit will not write the record; for example, if a 79 character record is transferred to the punch buffer in the 1414 I-O Synchronizer, no punch or card feeding operation occurs in the 1402 punch.

3. *Output operation with variable-length record I-O devices:* The GM-WM in the output field terminates data transfer. The WLR status latch is not set (not used).

When load mode operation is performed with a seven-bit I-O device, WM-WS character conversion must be considered in computing record length; for example, 80 word separator characters placed on the channel input data lines result in only 40 input characters (WS characters) being stored in the input field

in the 1411 core storage. Conversely, the 40 characters in the 1411 core storage result in 80 output characters (ws characters) on the channel output data lines during output operation.

Record length is also controlled by the d-character of the i-o instruction, which may have any one of four d-characters:

R (read): Accepts input characters until an input field GM-WM is sensed, the end of storage is sensed, or the input unit signals end of transfer.

\$ (read): Accepts input characters until the end of storage is reached.

W (write): Transfers characters to the channel until an output field GM-WM is sensed, the end of storage is sensed, or the output unit signals an end of transfer.

X (write): Transfers characters to output unit until end of storage is sensed or the output unit signals an end of transfer.

The X and \$ d-characters are used primarily for memory dump routines in tape operations.

i-o record lengths are checked by a correct length record latch as well as the wrong length record latch, providing a double check; for example, to branch on a branch on wrong length record instruction requires the WLR latch to be on and the CLR latch off.

i-o commands are terminated at the end of I-phase if any status latches are on, including the correct length record latch. Special i-o commands for the tape unit control (U op codes) involving no data transfer (no E-phase) force on the correct length record latch to terminate the operation.

No Transfer: The selected condition represented by the no transfer status latch varies with the i-o operation. The following example briefly describes the function of the no transfer indicator as used with the 1402 reader; three instructions are available:

Read a card	M%10	Transfers contents of buffer to CPU and causes next card to be read into the buffer.
Read the buffer	M%19	Transfers contents of buffer to CPU. No card feed cycle.
Feed a card	Kd	Causes a card to be read into the buffer. No buffer to CPU data transfer.

Multiple buffer transfer operations or multiple feed a card instructions result in a no transfer indication. The usual programming sequence is: feed a card, read the buffer, feed a card, read the buffer, and so on. (Refer to the appropriate section of the manual for operation of the no transfer latch during a particular op code.)

CHANNEL I-O INTERLOCK

The stored program must interrogate the channel status indicators between successive operations on the same channel or a system program check (i-o *interlock*)

occurs and the system stops. At the end of I-phase of a channel 1 i-o operation, the op code (M or L) conditions the turn-on of either the E-channel move latch or the E-channel load latch. Either latch being on will light the channel 1 interlock indicator in the i-o channel control section of the IBM 1415 console indicator panel (Figure 9). If the channel 1 interlock indicator is still on when channel 1 is again selected for an i-o operation, the system stops with the *systems check* i-o interlock indicator on. Special i-o commands (op codes F, K, and U) also turn on the channel interlock and require a programmed test of the channel status indicators the same as M and L op codes.

The interlock (move or load latch) for channel 1 is turned off as follows:

1. The stored program encounters a branch on any channel 1 status indicator instruction (R *mmid*). The interlock is turned off regardless of whether or not a branch occurs.

Note: The branch on channel 1 status indicator instruction is also referred to as a branch on external indicator instruction.

Mnemonic	BEX 1	(Channel 1)
	BEX 2	(Channel 2)

2. The stored program encounters a branch on selected channel 1 indicator instruction and a branch occurs.

3. E-channel reset line active (an E-channel reset occurs during I-phase of a channel 1 i-o instruction if the i-o interlock test is satisfied).

4. Computer reset line active (a computer reset forces an E-channel reset).

Channel 1 status indicators are tested with an R-type op code. The d-character in the instruction format selects the indicator to be tested. The format for the branch if channel status indicator on is:

OP CODE	I-ADDRESS	d-CHARACTER
R (channel 1)	XXXXX	(see following table)
X (channel 2)	XXXXX	(see following table)

d-CHARACTER	SELECTED INDICATOR	MNEMONIC
1-bit	Not Ready	BNR
2-bit	Busy	BCB
4-bit	Data Check	BER
8-bit	Condition	BEF
A-bit	No Transfer	BNT
B-bit	Wrong Length Record	BWL

More than one status indicator may be tested with a single instruction by using a d-character with a combination of bits; for example:

R (I) 3 Tests both Not Ready and Busy

R (I) \neq Tests all six indicators

Mnemonic: BEX1 Address, 3

BEX1 Address, \neq

A branch to the I-address occurs if any one of the selected indicators are on.

If the system is equipped with the processing Overlap feature, the program should test the overlap in process indicator before testing the channel status indicators. If the channel status indicators are interrogated by the program before the overlapped operation is completed, the CPU is interlocked (computing is suspended) until the channel operation is completed. This is done because a valid interrogation of the status indicators cannot be made until the end of the operation and all status indicators have been set.

The following example shows simple I-O programming:

00001	$\bar{M}\%11BBBBBR$	Read a card
00011	$\bar{R}000012$	If busy, try again
00015	$\bar{R}01000\#$	Branch if any status indicator on
00025	AAAAAABBBBBB	Process data
00036	$\bar{M}\%44BBBBBW$	Punch a card
00046	$\bar{R}000362$	If busy, try again
00053	$\bar{R}04000\#$	Branch if any status indicator on
00060	$\bar{J}00001\#$	Branch to repeat program
00067	$\bar{V}\bar{V}$	
01000	RXXXXX1	Conditional branch to not ready type routine
01007	RXXXXX8	Conditional branch to end of file routine
01014	RXXXXX4	Conditional branch to data check type out routine
01021	RXXXXXb (A-bit)	Conditional branch to no transfer routine
01028	RXXXXX- (B-bit)	Conditional branch to wrong length record routine

If the reader is busy when the read instruction is attempted, the E-channel busy indicator is turned on and the operation is ended immediately (no E-phase). The branch on busy instruction causes the CPU to attempt the read operation repeatedly until the reader is no longer busy. When the reader is no longer busy, the E-channel busy indicator is not turned on, and E-phase (data transfer) of the read instruction occurs. At the end of E-phase, the B-status channel indicators are set (conditionally), and the program proceeds to the next sequential instruction. The next sequential instruction is the branch on busy instruction. Because the busy indicator was not set during the I-phase of the read instruction, no branch occurs. The reader itself is busy at this time, but it was not busy at the time the busy bus was sampled at status sample A time of the read instruction. Note that the branch on busy instruction tests the channel status indicator, not the current status of the I-O unit.

Instruction Format — Move or Load

One basic instruction word is common to all I-O devices. See Figure 11. Special instructions (op codes F,

		Basic I-O Command	
Instruction format:		O XXX BBBBB d	
Example: (card read)		M %12 03000 R	
Specifies data transmission mode	-- O M --	Move mode	
Selects channel and overlap or unoverlap operation	-- X % --	E channel, unoverlap	
Selects I-O unit	-- X 1 --	Select reader	
(function varies with I-O unit)	-- X 2 --	Select stacker 2	
Initial data address (five digits)	-- B 0 --	Store first input char in address 03000	
		B 3	
		B 0	
		B 0	
		B 0	
Specifies direction of data flow (input or output)	-- d R --	Read (input mode)	

d-characters

- R Accept input characters until a GM-WM is sensed in the input field
- S Accept input characters until the end of storage is sensed
- W Transfer output characters until a GM-WM is sensed in the output field
- X Transfer output characters until the end of storage is sensed

Figure 11. Move or Load Instruction Format

K, and U) are described with the device employing that op code. Instruction formats are shown on the IBM 1410 Data Processing System Reference Card, Form X24-6502.

Op Code Character

The op code character is set into the op register and brings up the op code grouping lines to control subsequent events. The op code also determines the mode of data transmission: move mode or load mode. An M op code specifies move mode; an L specifies load mode.

A 1410 system with the process overlap feature is able to initiate an I-O operation and then proceed with the stored program while the I-O operation is in process. Consequently, the CPU must "remember" the op code. It does so by setting either the channel move mode latch or the channel load mode latch during late I-phase of any move or load op code. The E-channel move or load latch will light the channel 1 interlock indicator in the I-O channel control section of the IBM 1415 Console (Figure 9).

X-Control Field

Characters in the X-control field provide channel and unit selection. These characters may be gated onto the address channel as first address characters in the same manner as any other two address instruction, but the characters are not read into any address register. During I-phase first address time of an I-O instruction, the address check circuits permit 8-4 (8-bit, 4-bit) combination characters on the assembly channel, to avoid an address check from the channel select character

(%, □, @ or *). The character 4 (in two of five code) is emitted onto the address channel in place of the 8-bit, 4-bit channel select character.

Channel Selection: The hundreds position of the X-control field contains the special character that determines which one of the four channel select latches is set.

Percent sign	%	E-channel unoverlap in process
Commercial at	@	E-channel overlap in process
Asterisk	*	F-channel unoverlap in process
Lozenge	□	F-channel overlap in process

Each latch has an indicator in the I-O channel control section on the IBM 1415 Console. Note that the character selects overlap or unoverlap operation as well as selecting the channel.

Unit Selection: The tens position of the X-control field contains the unit select character which is set into the unit select register. The character 1, for example, selects the 1402 reader, conditioning the circuits between the reader synchronizer (IBM 1414) and the CPU.

Unit Number Selection: The units position of the X-control field contains the unit number character which is set into the unit number register. The function of the unit number character varies with the I-O device selected. During reader operation, for example, a 1 selects the reader stacker pocket number 1. During IBM 1402 Card Read Punch move or load op codes, the unit number is sent to the synchronizer over the channel output data lines and, although the unit number character is set into the unit number register, the register is not used.

B-address

The B-address is the initial data address. During input operation, the first input character is stored in this address. The next character is stored in the next higher storage location. During output operation, the first output character is taken from this initial address and the next character is taken from the next higher storage location. During I-phase of unoverlapped operation, the working address register is the B-address register (BAR). For overlapped operation, the E-address register (EAR) is the working address register.

d-character

The d-character is set into the op modifier register and specifies input or output mode. An R specifies input mode (read) and a W specifies output mode (write). The output of the op modifier register is used to gate the setting of either the channel input mode latch or the output mode latch late in I-phase of the I-O instruction, leaving the op modifier register free to accept another character in case of overlap operation.

The on output of the E-channel input mode latch lights the E-channel read indicator in the channel control section of the IBM 1415 Console. The on output of the E-channel output mode latch lights the E-channel write indicator on the 1415 (Figure 9). F-channel latches have the same name as the console indicators. Figure 12 shows a simplified logic flow for move or load command.

Processing Overlap

The process overlap feature permits a 1410 system to process data (compute) while an input-output (I-O) operation is being performed. Process overlap is an optional feature, not on a basic 1410 system. A basic 1410 system is interlocked (unable to compute) during an I-O operation, remaining idle except when an I-O data cycle is required to transfer a character between core storage and the I-O channel.

With process overlap, the 1410 system may use this idle time to take compute cycles. The computing is interrupted (disabled) when an I-O data cycle is required. Computing is resumed when the I-O data cycle is completed.

Compute cycles use the normal logic gate ring; overlapped I-O operations use a logic gate extension ring. Computing is interrupted by disabling the logic gate ring. The I-O data cycle starts the logic gate extension ring which times the operations for that cycle.

The process overlap feature is optional on a single-channel system; required on a two-channel system. The priority feature is recommended on systems equipped with process overlap. (See *SRL IBM Priority Feature*, Form A22-0530).

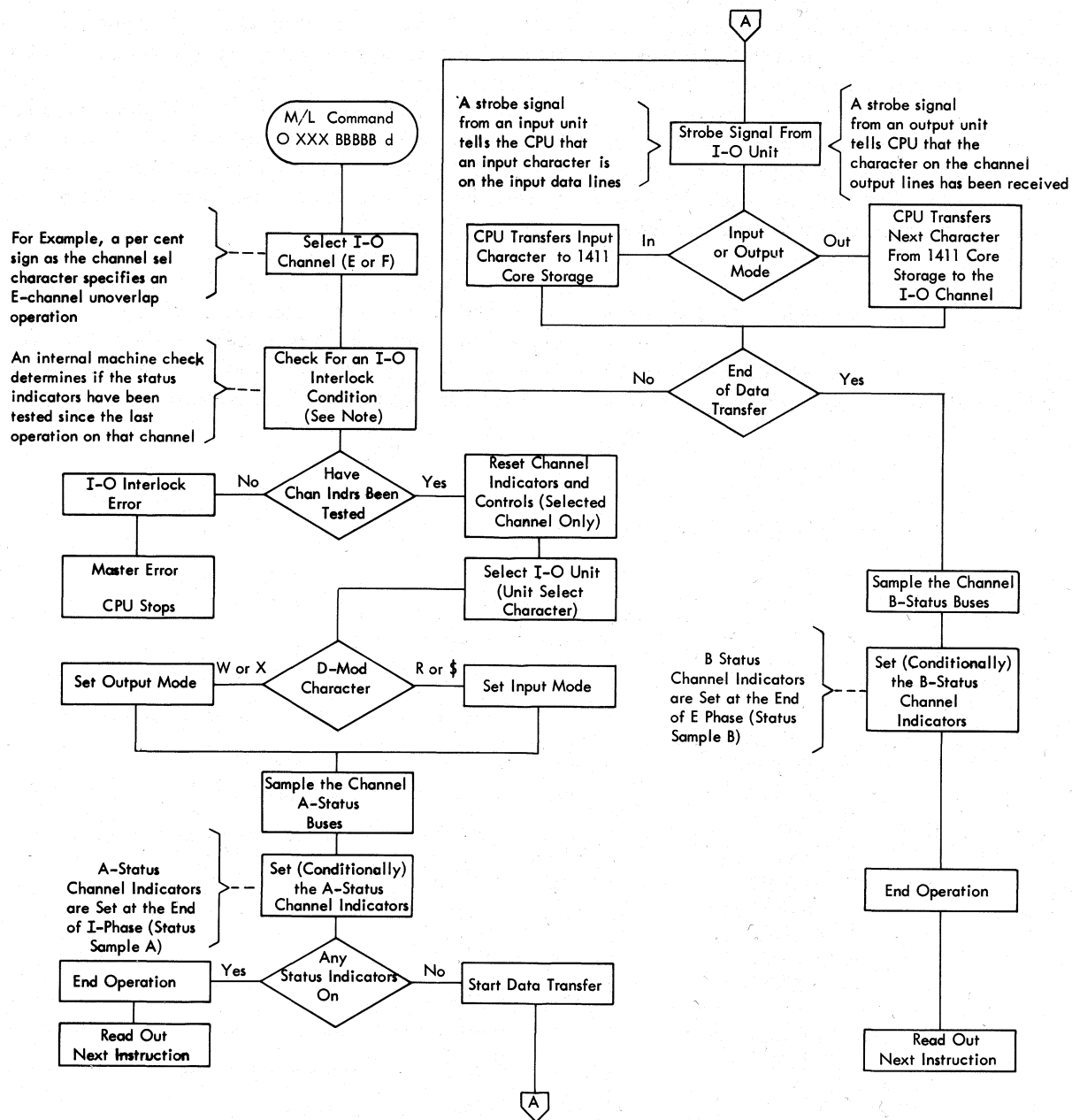
The process overlap feature requires additional circuits and components such as:

- Logic clock extension ring
- E-address register (EAR) for E-channel
- F-address register (FAR) for F-channel (if a two-channel system)
- E-channel overlap in process indicator
- F-channel overlap in process indicator
- Compute disable circuitry
- E-cycle and F-cycle control circuitry

The overlap in process indicators can be interrogated by the stored program. Programming considerations for systems with the process overlap feature are described in *IBM 1410 Principles of Operation*, Form A22-0526.

Some general rules concerning processing overlap are:

1. Only one I-O unit can be operated per channel at any given time, whether or not overlap mode is being used.



Note

The program must test the channel status indicators between successive I-O operations on the same channel.

The I-O Interlock test is satisfied by:

1. A branch-any-indicator instruction R (I) GM.
2. A successful branch on a selected channel indicator.

Figure 12. Move or Load Command Logic Flow

2. If one channel is operating in overlap mode, the other channel may not operate in unoverlap. However, both channels may operate simultaneously in overlap mode.

3. Status indicators should be tested for the last I-O instruction just prior to executing another I-O instruction. If the program attempts to check the indicators before the channel operation is complete, compute disable interrupts the program until the channel operation is finished.

4. The E-channel has priority unless the last cycle was an E-cycle.

5. A \$ d-character (read to end of storage) is effective only with an unoverlapped read command. An

overlapped read command with a \$ d-character is treated the same as an overlapped read command with an R d-character.

6. An X d-character (write to end of storage) is effective only with an unoverlapped write command. An overlapped write command with an X d-character is treated the same as an overlapped write command with a W d-character.

Figure 13 illustrates a typical application of processing overlap. A reel of tape on the E-channel is being copied onto a reel of tape on the F-channel. The reading and writing is done in overlap mode so the time between the E- and F-cycles can be used to move the data from an input area of memory to an output area.

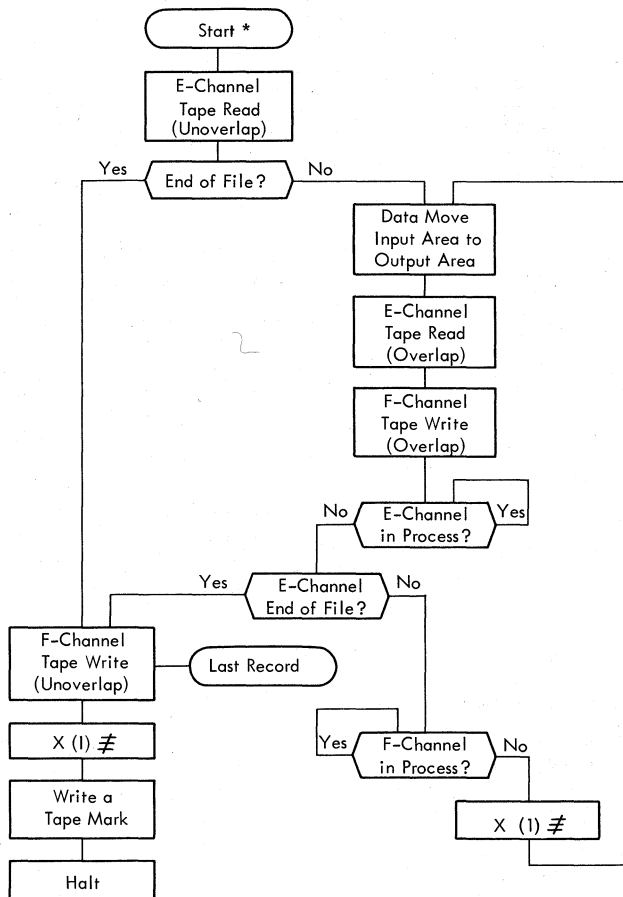


Figure 13. Processing Overlap

Actual Program:

10200	✓ M%U010100R	Read First Record
10210	✓ R10284 ≠	End of File?
10217	✓ D1010010181\$	Data Move Input Area to Output Area
10229	✓ M@U010100R	Overlapped Read
10239	✓ M*U010181W	Overlapped Write
10249	✓ J102491	E-Channel in Process (Busy)?
10256	✓ R10284 ≠	End of File?
10263	✓ J102632	F-Channel in Process (Busy)?
10270	✓ X10277 ≠	F-Channel I-O Interlock
10277	✓ J10217b1	Start
10284	✓ M U010181W	Write Last Record
10294	✓ X10301 ≠	F-Channel I-O Interlock
10301	✓ U U0M	Write a Tape Mark
10306	✓	
10307	✓	

* Assume:

1. No Errors
2. I-O Areas Already Set Up
3. Input Tape On E-Channel
4. Output Tape On F-Channel

Channel Data Register Controls

Each channel has two eight-bit data registers and associated control circuits. Operation is basically the same for all types of I-O operations. The registers are used for transfer of data during E-phase, and also, in the case of the IBM 1402 Card Read Punch, for transfer of the stacker select character during I-phase.

For ease in learning channel register operation, the presentation is divided into four sections:

1. Register components and controls
2. Input operation – move mode
3. Output operation – move mode
4. Input-output operation – load mode (word separator mode)

Register Components and Controls

Because both E- and F-channels are similar, only E-channel operation is described. In some cases, line names in the ALD's may vary slightly between E-channel and F-channel, but the operation is identical.

Data Registers: The registers have no reset, retaining one character until a new character is set into the register. A register is made up of eight latches (Figure 14). Each channel has two registers:

Data Register one (E-1 or F-1)
Data Register two (E-2 or F-2)

Data Flow Controls (Copy Controls): Data flow from E-1 to E-2 is controlled by the four lines:

Copy E-1 BCD to E-2 Reg
Copy E-1 WM and C-Bit
*Set E-2 Word Separator (emits a WS into E-2)
*Copy Invert E-1 WM and C-Bit
*Used only in word separator mode.

Transfer Controls: The transfer (set) lines determine when the data is transferred from E-1 to E-2, in con-

trast to the copy controls which determine what data is transferred.

Set E-1 Register	(sets E-1 to the character at E-1 input, Figures 15 and 16)
Set E-2 Register	(sets E-2 to the character in E-1)
E-1 Reg Full	(indicates a new character has been set into E-1)
E-2 Reg Full	(indicates a new character has been set into E-2)
Reset E-2 Full Latch	(calls for a new character in E-2)

Word Separator Controls: Additional controls are required to enable the registers to process word separator characters and WM characters.

E-1 Reg Word Separator
E-2 Reg Word Separator
Set E-2 Reg Delayed

Five "rules" to remember are:

1. Direction of data flow is always from E-1 to E-2.
2. A register transfer (E-1 to E-2) always occurs when E-1 is full and E-2 is not full.
3. During input operation, the CPU tries to keep E-2 empty (not full).
4. During output operation, the CPU tries to keep E-1 full.
5. Channel data registers have no reset. The old character remains in the register until the register is set to the bit and no-bit configuration of a new character.

Move Mode Operation

Channel register operation is first presented in move mode. Load mode operation requires additional circuits and is described later.

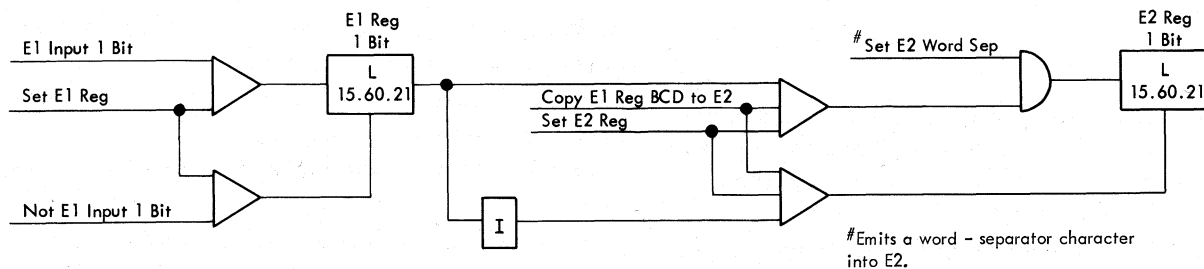
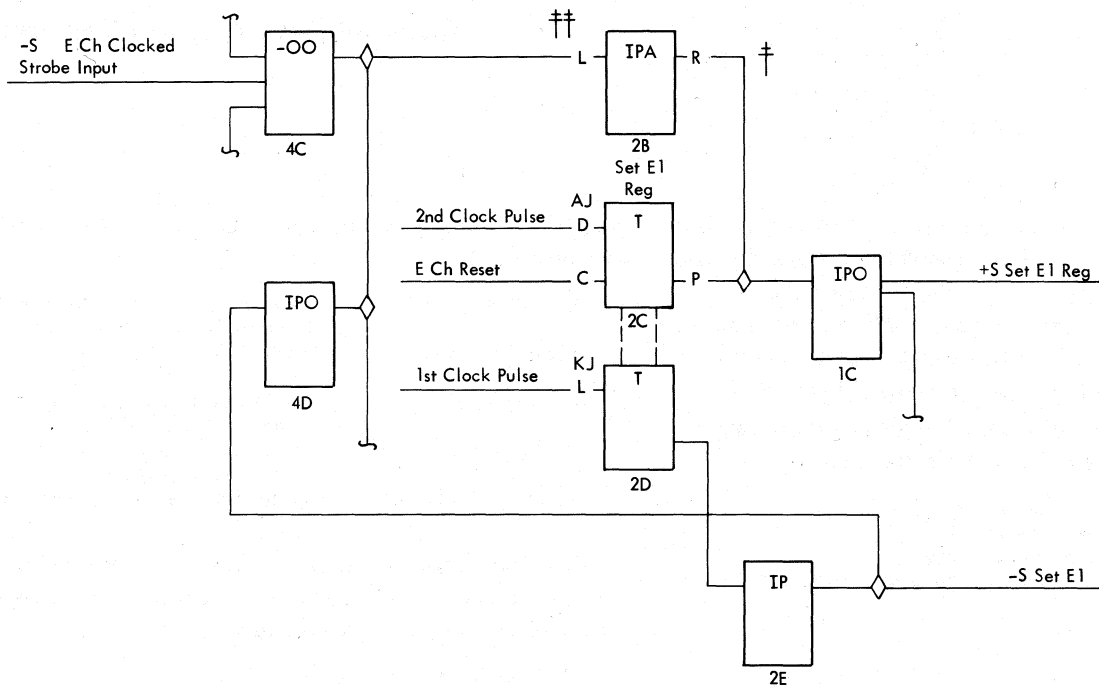
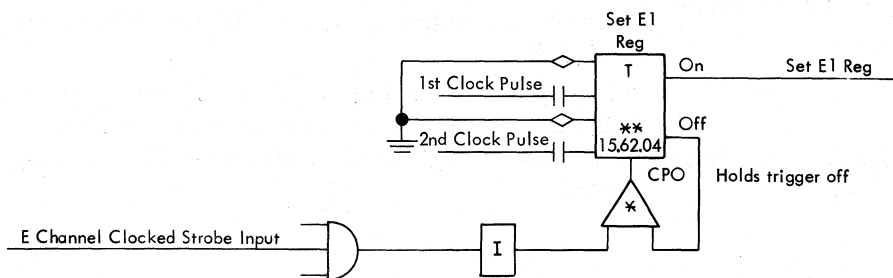


Figure 14. E-1 and E-2 Register Latches



† Collector Pullover
 †† A +S at pin L of "IPA" at co-ord 2B will remove the collector pullover, permitting the next 1st clock pulse to turn trigger on. The "IPO" at co-ord 4D prevents the trigger from being turned off by collector pullover, insuring that trigger remains on for a full clock pulse.

Figure 15. Set E-1 Register Trigger - ALD



* Collector Pullover To permit easy identification of the collector pullover circuit, it is shown as a reset input into the bottom of the logic block.
 ** E-Channel Reset

Figure 16. Set E-1 Register Trigger - Condensed Logic

Note: Close timing relationships occur in the channel circuits. Excessive delay(s) in logic circuits may cause machine failures.

Input Mode

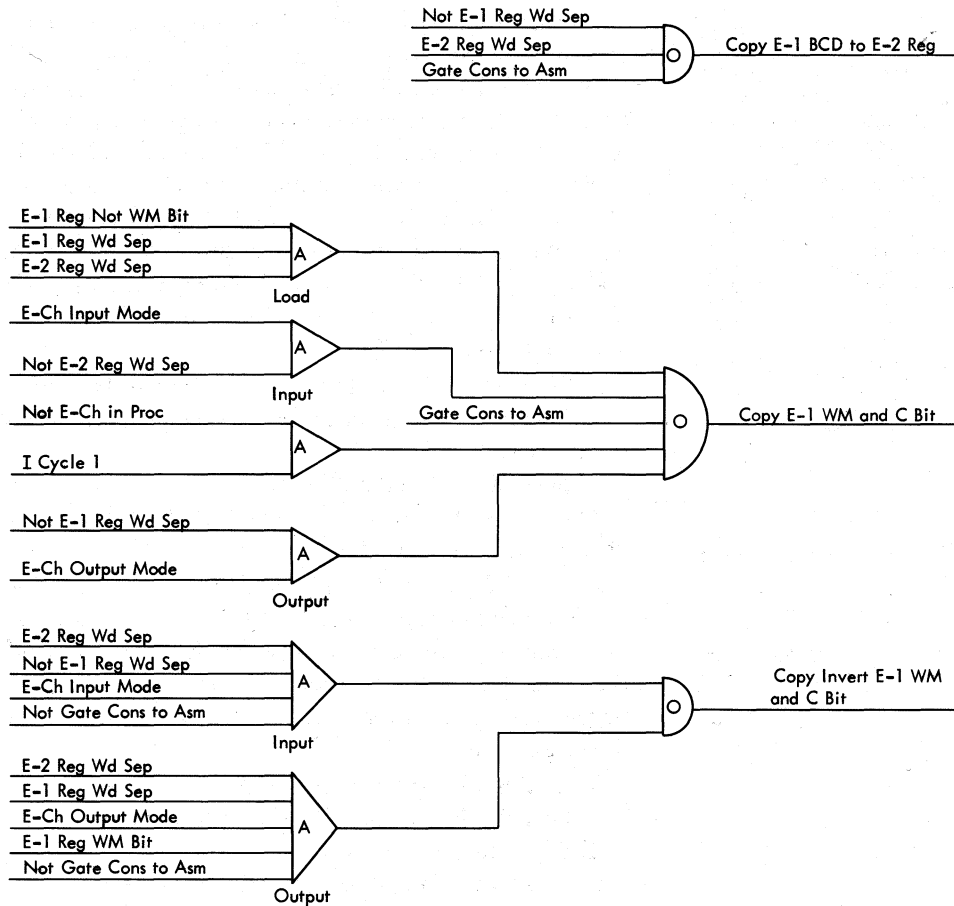
During input mode i-o operation, an input character on the channel input lines is transferred through the channel data registers, the A-channel, assembly channel, and into 1411 core storage.

Assume an input data transfer operation on E-channel is starting and the following copy control lines are active:

Copy E-1 BCD to E-2 Reg (Figure 17)
 Copy E-1 WM and C-Bit (Figure 17)

An E-channel Reset (Figure 18) occurs at the beginning of an i-o operation, resetting the channel controls. The two channel data registers are considered empty (not full) because the E-channel reset turns off the E-1 reg full latch and the E-2 reg full latch. (See Figure 19.)

Strobe: The input device generates strobe, signalling the channel controls that a character is on the channel input data lines (Figure 20).



15.62.06

Figure 17. E-Channel Data Flow Controls

E-channel Strobe Trigger: The rise of the strobe signal from the input device turns on the E-channel strobe trigger which removes the collector pullover from the E-channel clocked strobe trigger. The rise of the next 2nd clock pulse turns on the trigger.

E-channel Clocked Strobe Trigger: "Clocked strobe" AND's with "input mode" and "not E-1 reg full" to remove the collector pullover from the "set E-1 reg trigger," permitting the trigger to turn on at the rise of the next 1st clock pulse (Figures 15 and 16).

Set E-1 Reg Trigger: The on output of this trigger:

1. Sets the E-1 register to the bit configuration of the input lines.
2. Sets the E-1 register full latch.
3. Pulls over (off) the E-channel strobe trigger which in turn pulls over (off) the E-channel clocked strobe trigger.

The following clock pulse (2nd clock pulse) turns off the set E-1 reg trigger. Note that the collector pullover circuit is AND'ed with the off output of the trigger. This prevents the trigger from being pulled off but permits the trigger to be held off once it is turned off

by a 2nd clock pulse. The AND circuit insures that the trigger remains on for a full clock pulse.

E-1 Full Latch: This latch is turned on when E-1 is set, indicating that E-1 contains a new character. With the E-1 full latch on and the E-2 full latch off, the collector pullover is removed from the set E-2 reg trigger and the rise of the next 1st clock pulse turns the trigger on.

Set E-2 Reg Trigger: The on output of this trigger:

1. Sets the E-2 register to the data gated from E-1 to E-2 by the copy control lines.
2. AND's with "not E-1 reg wd sep" to set the E-2 reg full latch, and reset the E-1 reg full latch.

The next 2nd clock pulse turns off the set E-2 reg trigger and it is held off by the collector pullover circuit.

E-2 Reg Full Latch: The on output of this latch AND's with "E-channel in process" and other conditions to bring up "E-cycle required." The CPU takes an I-O data cycle (E-cycle) and the data from E-2 is gated to the A-channel, assembly channel, and into core storage. Near the end of the E-cycle, "early last gate I-O" AND's with other conditions to remove the collector

E Ch Not Ready latch	12,62,01	E Channel Reset	15,41,12
E Ch Busy latch	12,62,02	E-1 Reg Word Sep latch	15,41,11
E Ch Condition latch	12,62,04	E-2 Reg Word Sep latch	15,41,11
E Ch Check latch	12,62,04	E Ch Unit Sel Reg	15,55,08-09
E Ch No Transfer latch	13,72,04	E Ch Unit Num Reg	15,55,01-02
E Ch WLR latch	13,63,03	E Ch Int End of Tran Delay latch	13,65,05
E Ch CLR latch (special reset)	13,63,03	E Ch Int End of Tran	13,63,01
		E Ch End of Record latch	13,63,01
Input Mode latch	15,62,01	E Ch Ext End of Tran Ctrl latch	13,42,11
Output Mode latch	15,62,01	E Ch Ext End of Tran Trigger	13,42,11
E Ch Move Mode latch	15,62,02	E Ch Disc latch	13,42,11
E Ch Load Mode latch	15,62,02		
		File Start latch	13,72,01
E Ch Strobe trigger	15,62,03	2nd Addr Tran latch	13,72,01
E Ch clocked Strobe trigger	15,62,03	1st Char 2nd Addr Ctrl latch	13,72,01
Set E-1 Reg trigger	15,62,04	1st Char 2nd Addr latch	13,72,01
Set E-2 Reg trigger	15,62,04	E Ch End Addr Tran latch	13,72,01
Reset E-2 Full Latch trigger	15,62,05	File Strobe latch	13,72,02
E-1 Reg Full latch	15,41,10	File Addr Tran Gate latch	13,72,02
E-2 Reg Full latch	15,41,10	1st Data Strobe latch	13,72,04

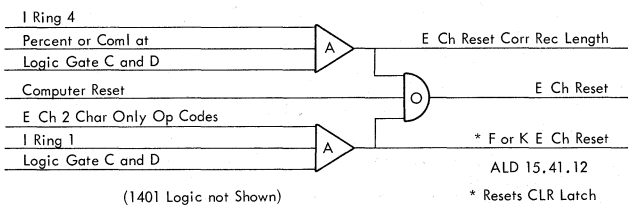


Figure 18. E-Channel Reset

pullover from the reset E-2 reg full latch trigger, permitting the next 1st clock pulse to turn the trigger on.

Reset E-2 Full Latch Trigger: The on output of this trigger resets the E-2 reg full latch and the following clock pulse (2nd clock pulse) turns off the reset E-2 full latch trigger.

The sequence is complete; both data registers are empty (not full) and ready to receive another input character. Note that both registers do not have to be empty for the channel to receive another input character. Only E-1 must be empty in order to accept another character from the channel input data lines.

Output Mode

During output mode operation (Figure 21), an output character in core storage is transferred to the channel data registers via the B-channel and assembly channel. The character in E-2 appears on the channel output data lines which are sampled by the output device (Figure 22).

Assume the following:

- E-channel Reset has occurred (Figure 17)
- Copy E-1 BCD to E-2 Reg line is active (Figure 18)
- Copy E-1 WM and C-Bit line is active (Figure 18)
- E-1 and E-2 are not full

E-cycle Required: This line becomes active at the end of I-phase when "E-channel in process" AND's with "not E-1 reg full" and other conditions to request the CPU to take an I-O data cycle (E-cycle) to transfer an output character to E-1. Near the end of the E-cycle, when the output character is on the assembly channel and available to E-1, "early last gate I-O" AND's with "output mode" and other conditions to remove the collector pullover from the set E-1 reg trigger, permitting the trigger to turn on at the rise of the next 1st clock pulse (Figure 100).

Set E-1 Reg Trigger: The on output of this trigger:

1. Sets the E-1 register to the bit configuration of the input lines.
2. Sets the E-1 reg full latch.

The following clock pulse (2nd clock pulse) turns off the set E-1 reg trigger.

E-1 Reg Full Latch: This latch is turned on when E-1 is set, indicating that E-1 contains a new character. With the E-1 full latch on and the E-2 full latch off, the collector pullover is removed from the set E-2 reg trigger and the rise of the next 1st clock pulse turns the trigger on.

Set E-2 Reg Trigger: The on output of this trigger:

1. Sets the E-2 register to the data gated from E-1 to E-2 by the copy control lines.
2. AND's with "not E-1 reg wd sep" to set the E-2 reg full latch and reset the E-1 reg full latch. The next 2nd clock pulse turns off the set E-2 reg trigger and it is held off by the collector pullover circuit.

E-2 Reg Full Latch: The on output of this latch:

1. Prevents the turn on of the set E-2 reg trigger (by collector pullover).
2. Conditions the AND circuit in the collector pullover circuit of the reset E-2 full latch trigger so that a strobe from an output device will initiate an E-1 to E-2 data transfer.

E-cycle Required: With the first output character transferred from E-1 to E-2, the E-1 reg full latch is off, and another I-O data cycle (E-cycle) is requested. CPU brings the second output character to the channel, so both E-1 and E-2 are full. No further action occurs until a strobe from the output device signals that the character on the output data lines has been received and a new character is needed.

Strobe: The output device sends a strobe signal to the channel controls requesting a new character to be placed on the channel output lines. The rise of the strobe signal turns on the E-channel strobe trigger and the on output of the trigger removes the collector pullover from the E-channel clocked strobe trigger.

E-channel Clocked Strobe Trigger: With the collector pullover removed, the trigger is turned on by the rise of the next 2nd clock pulse. The on output of the

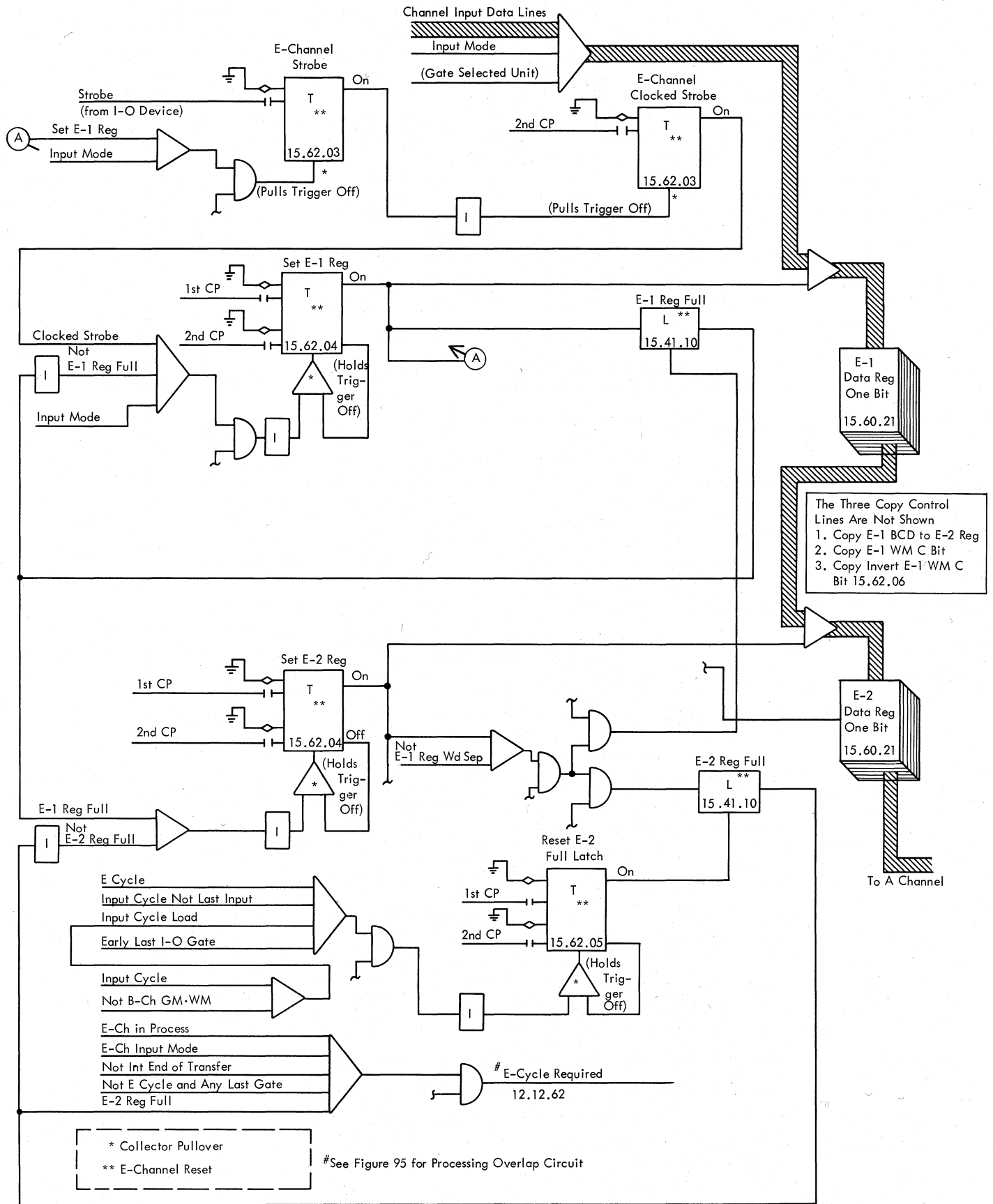


Figure 19. E-1 and E-2 Input Timing Chart

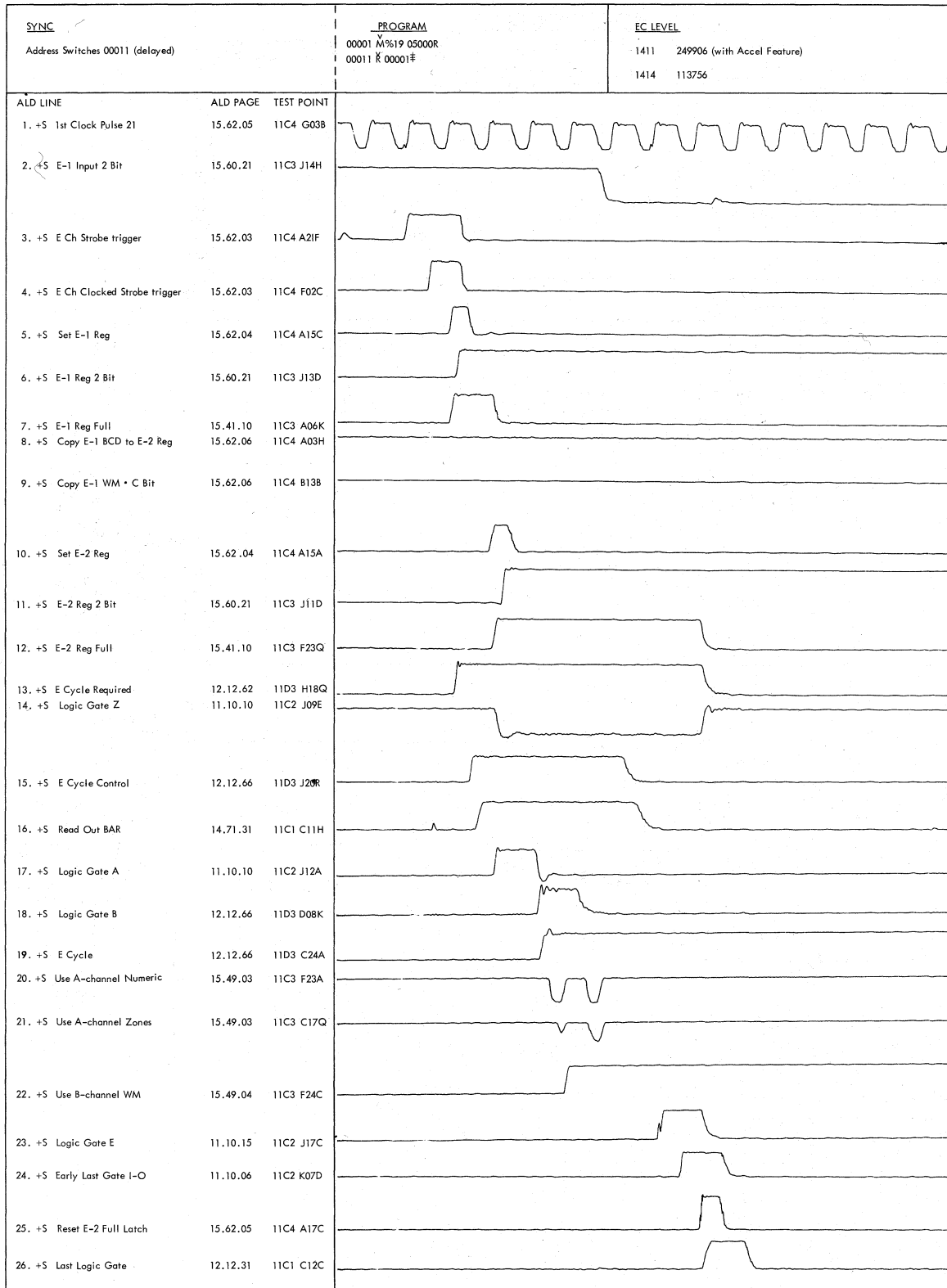


Figure 20. Channel Register Operation – Input Move Mode

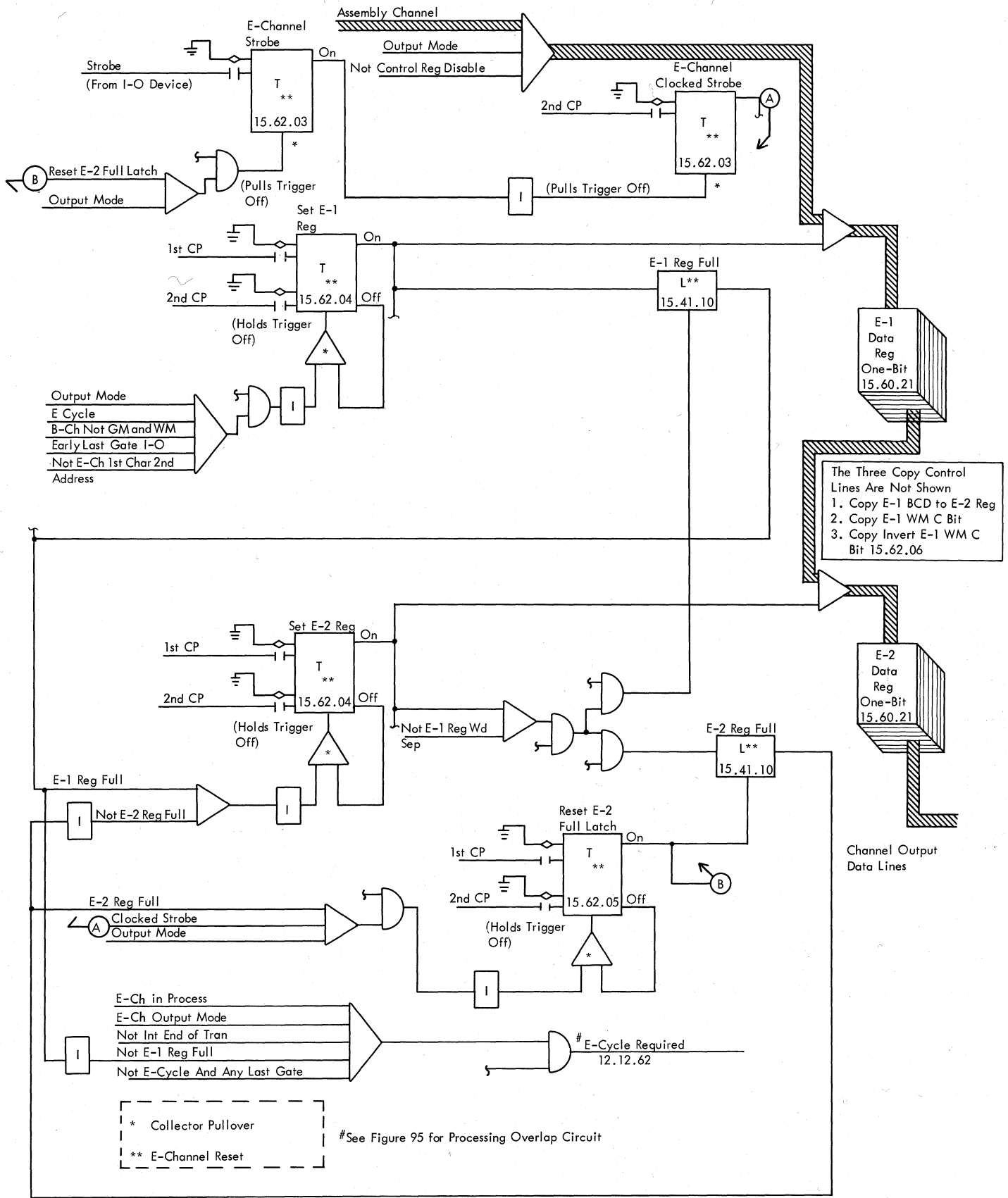


Figure 21. Channel Register Operation – Output Move Mode

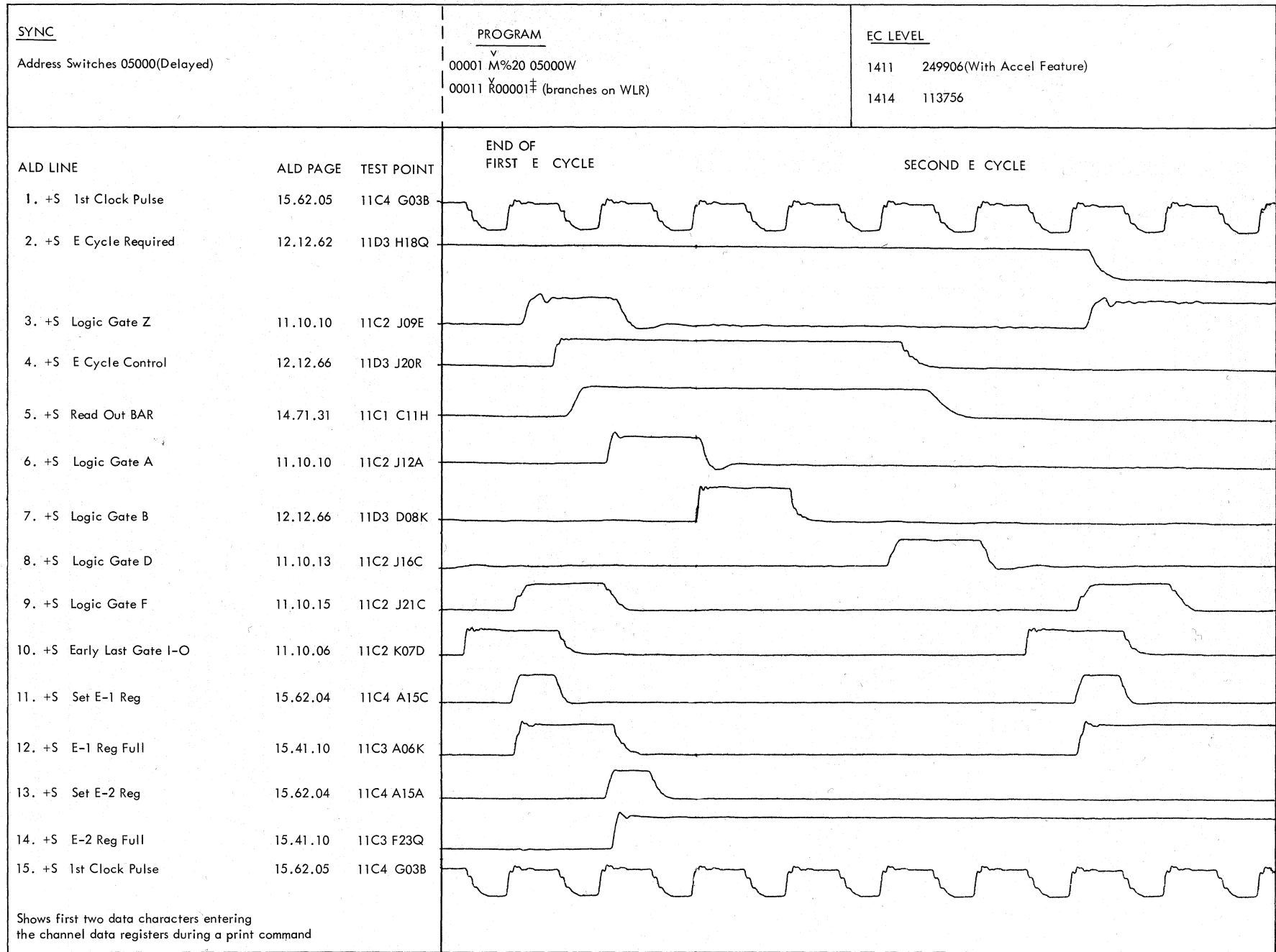


Figure 22. E-1 and E-2 Output Timing Chart

trigger AND's with "output mode" and "E-2 reg full" to remove the collector pullover from the reset E-2 full latch trigger, allowing the trigger to turn on with the rise of the next 1st clock pulse.

Reset E-2 Full Latch Trigger: The on output of the trigger:

1. Resets the E-2 full latch.
2. Pulls over (off) the E-channel strobe trigger which in turn pulls over (off) the E-channel clocked strobe trigger.

E-2 Reg Full Latch: With the E-2 reg full latch off and the E-1 reg full latch on, an E-1 to E-2 data transfer occurs, the E-2 reg full latch is turned back on and the E-1 reg full latch is turned off.

E Cycle Required: "Not E-1 reg full" AND's with "E-channel in process" and other conditions to bring up "E-cycle required." Another E-cycle is taken by CPU to bring the next output character from core storage to the channel data registers. When the new character is set into E-1, the E-1 reg full latch is turned on and no further action occurs until a strobe from the output unit calls for a new character on the output lines.

Load Mode Operation

The channel operates in word separator mode only during a load mode operation with a seven-bit I-O de-

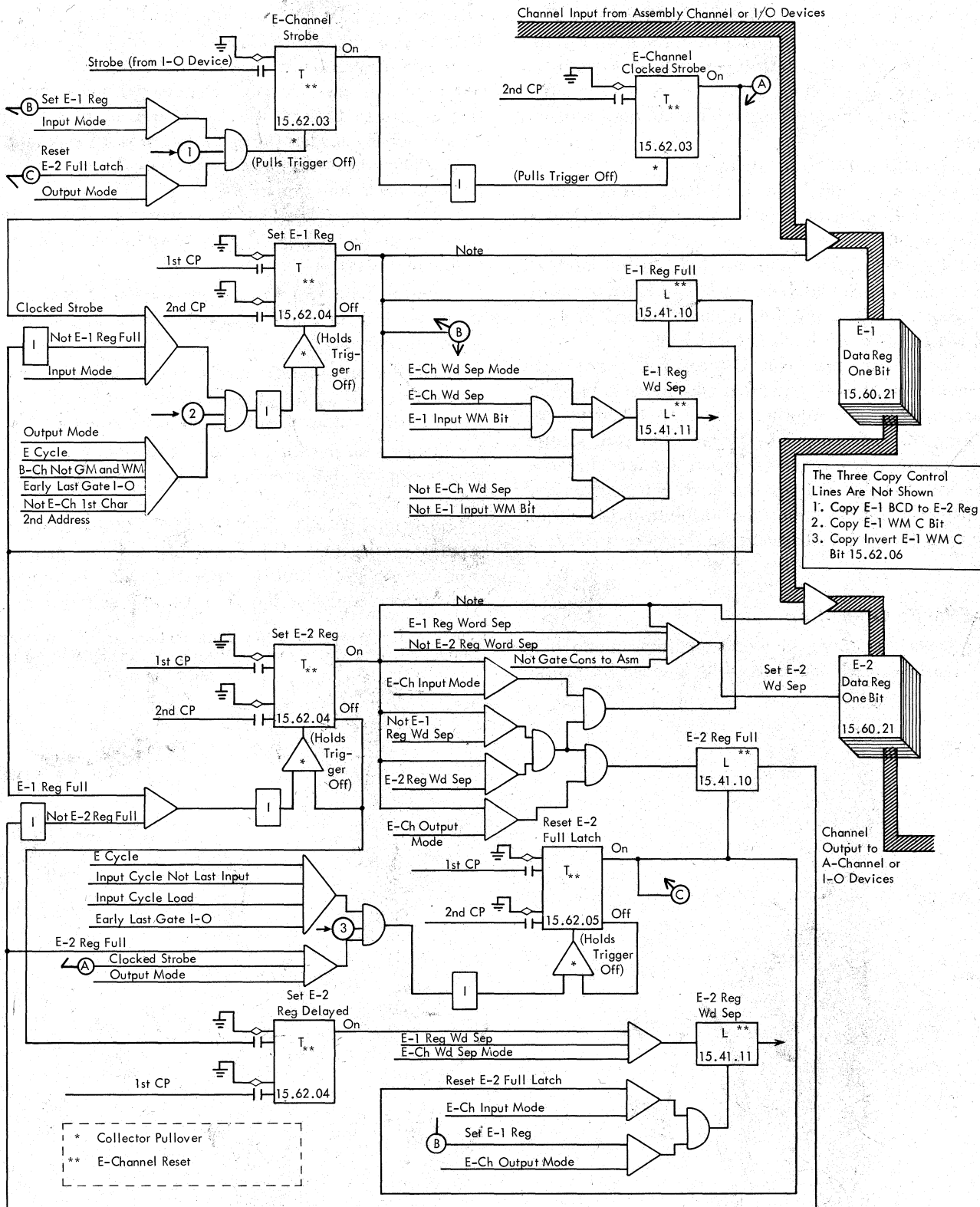
vice. Review "Data Transmission" and "Channel Data Registers" in the Input-Output Principles of Operation section before studying word separator logic.

Figure 23 shows the same channel register controls that appear in Figures 19, 20, 21, and 22, plus additional controls needed for operation in word separator mode. The additional circuitry enables the channel to perform these four functions:

1. During input load mode, conversion of a single word separator character to a word mark over the following character.
2. During input load mode, conversion of two consecutive word separator characters into a single word separator character.
3. During output load mode, conversion of a WM character (e.g., Å) into two characters (WM, A); the word mark becomes a word separator character.
4. During output load mode, conversion of a single word separator character into two word separator characters.

Use figures 17, 23, 24, 25, and 26 to learn word separator operation. When troubleshooting channel troubles, I-O data transfer operation can be caused without mechanical action of an I-O unit as follows:

Input	Use an M%19 (B)R	Program loop
Output	Use an M%20 (B)W	Program loop (no GM-WM in the output field)



Note: For Console Input Operation "Gate Console to Assembly" forces the "Set E1 Reg" and "Set E2 Reg" lines because no clock pulses are available to turn on the triggers.

Figure 23. Channel Register Operation — Load Mode

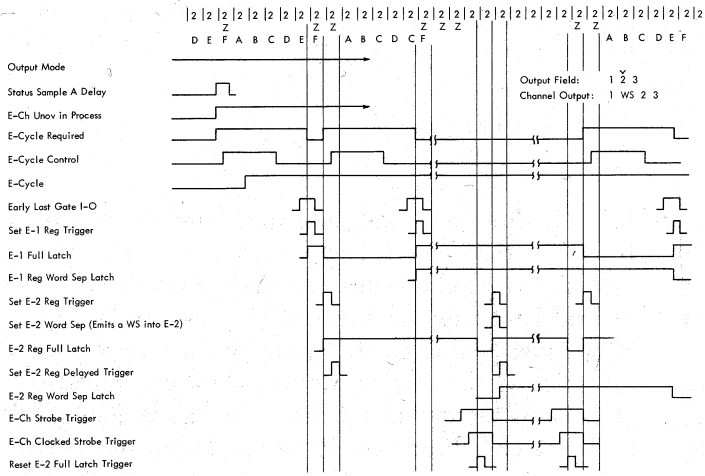


Figure 24. E-1 and E-2 Sequence Chart – Output Load Mode

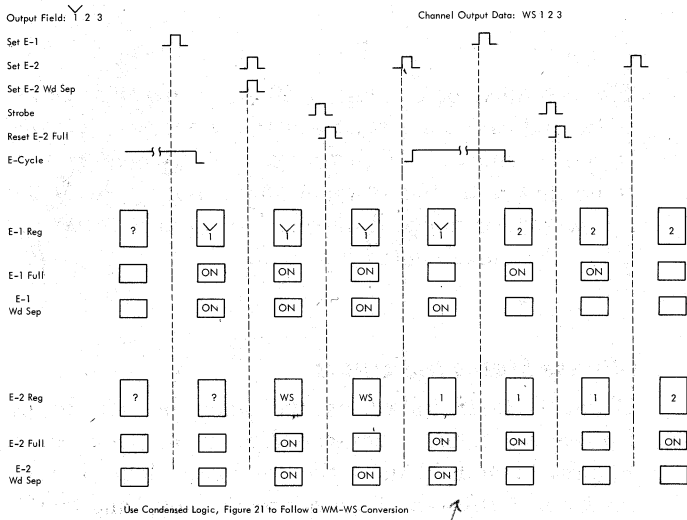


Figure 25. Word Separator Processing – Output

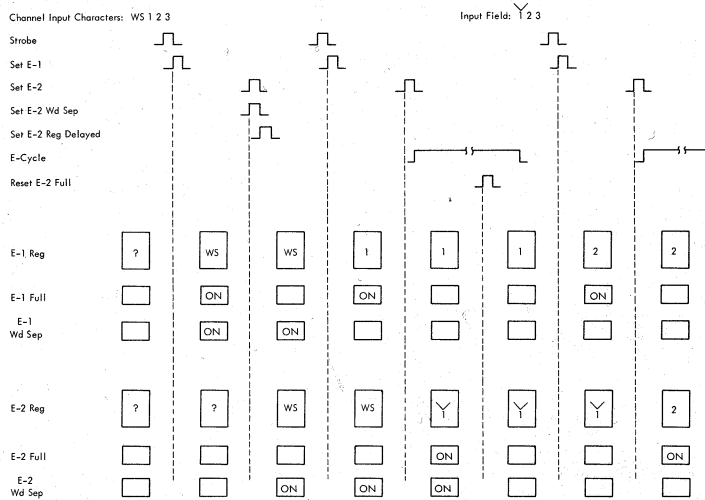


Figure 26. Word Separator Processing – Input

I-O Sequence

This section presents the CPU functions and machine logic for the basic I-O command (move or load) which is common to all I-O devices. Although a 1402 reader move operation is used as an example, the emphasis is placed on the CPU logic that is common to all move or load operations. Reader operation is described in detail in a later section of this manual.

The condensed logic diagrams in this section (Figure 27) are an instructional type of diagram, showing only partial circuitry. For reference purposes (troubleshooting) more comprehensive condensed logic diagrams are included in the reference section at the back of the manual.

The following presentation assumes the reader understands the information presented in the Input-Output Principles of Operation and Channel Data Register Controls sections of this manual.

Suggested review: "Channel Status Indicators" in the Input-Output Principles of Operation section.

I-Phase Functions

Two functions of the M/L are: selection and sensing. Figures 28 and 29 show the basic logic flow and timing for an M/L command.

Selection

The channel select character (a 1 in the example for card reader) reads out at I-3 time and is placed in the I-O channel select register. (Because the X-control field

has only three positions, the I-ring is rapidly advanced from I-op time to I-3 time.)

With a channel selected, the channel interlock (move or load latch) for the selected channel can be tested. If the interlock is on, the program has not properly interrogated the channel status indicators, and master error stops the CPU at I-3 time with the system check I-O interlock indicator on. If the interlock is off, a channel reset is generated for the selected channel, resetting the channel control and status latches.

The unit select character reads out and is set into the unit select register for the selected channel, selecting the desired I-O unit.

SENSING

The simplified logic in Figure 30 shows that the channel status indicators are reset at early I-phase of a move or load command. With an I-O unit selected and its status gated to the channel status buses, the buses are sensed, or sampled, during late I-phase to set the selected channel status indicators.

I-Phase Status Indicators

Channel status indicators that may be set during I-phase are called A-status indicators in the manual. Figures 31 and 32 show the condensed logic for the reader A-status indicators: not ready, busy, and condition. A-status indicators are set with a pulse called status sample A that occurs during the last instruction

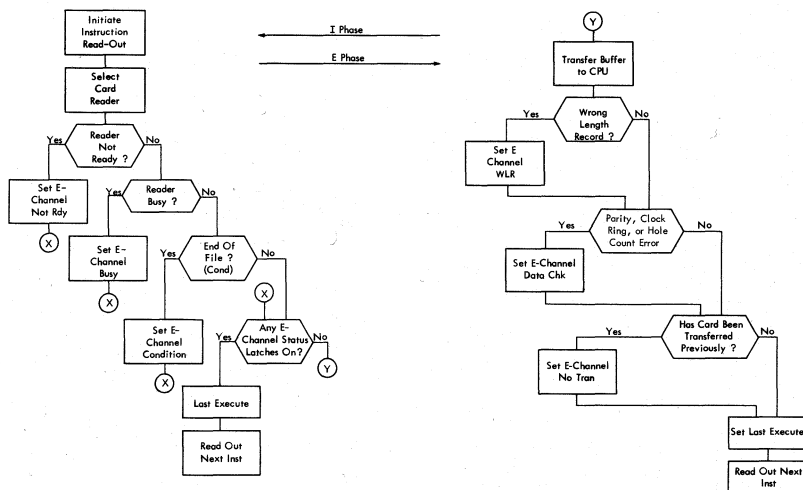
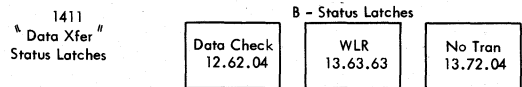
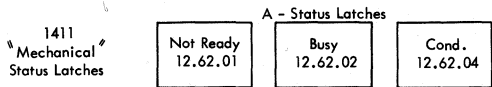
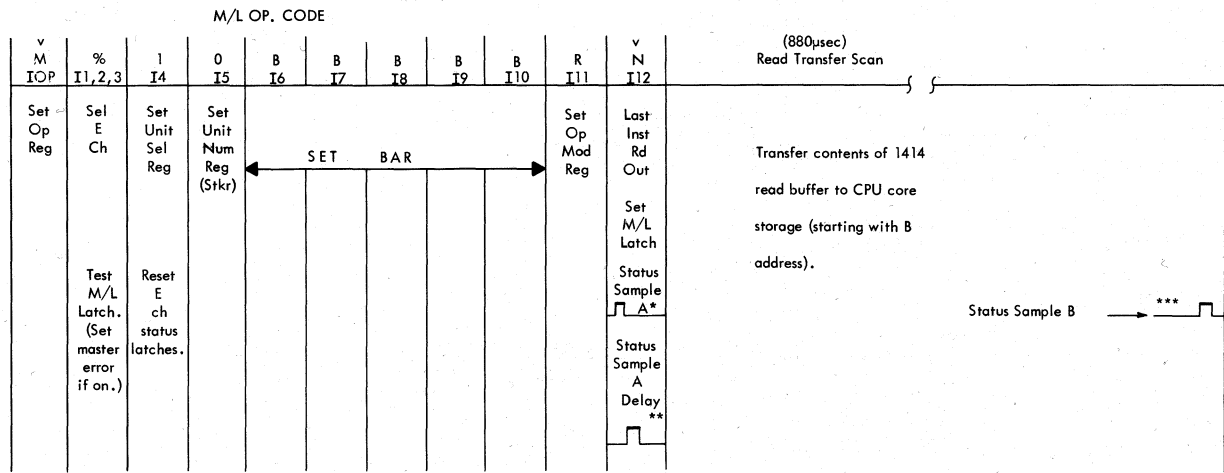


Figure 27. Condensed Logic Symbols



- *1. Set at status sample A time.
- **2. Tested at status sample A delay time.
- 3. When on, instruction is ignored.
- 4. Reset at I4 time of each M/L inst.

- ***1. Set at status sample B time.
- 2. Tested with R-type branch instr.
- 3. Reset at I4 time of each M/L inst.

Figure 28. Channel Status Checking – Basic Logic Flow

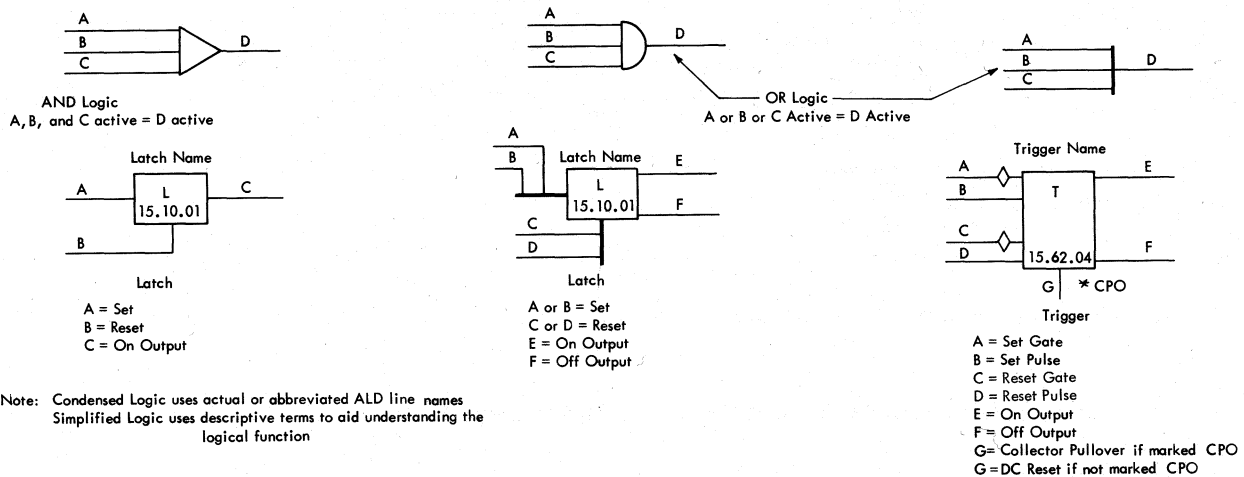


Figure 29. Channel Status Checking – Basic Timing

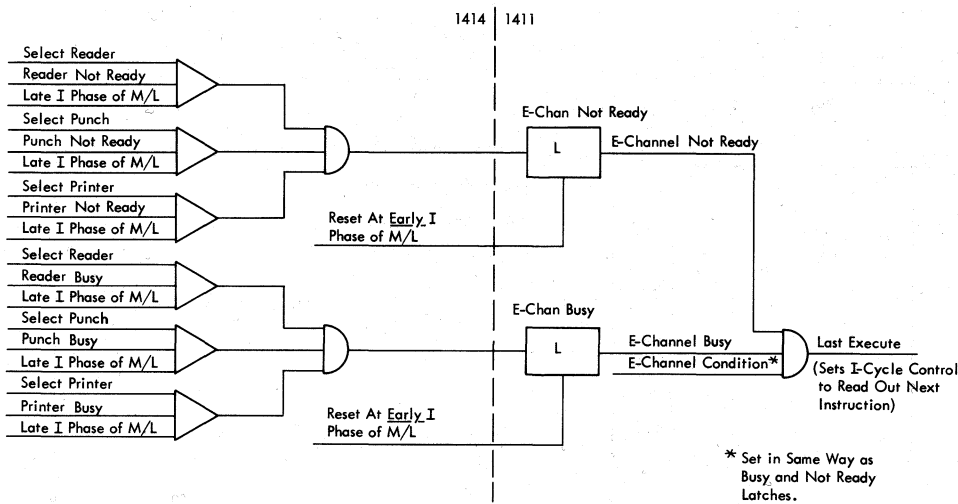


Figure 30. Channel Not Ready and Busy – Simplified Logic

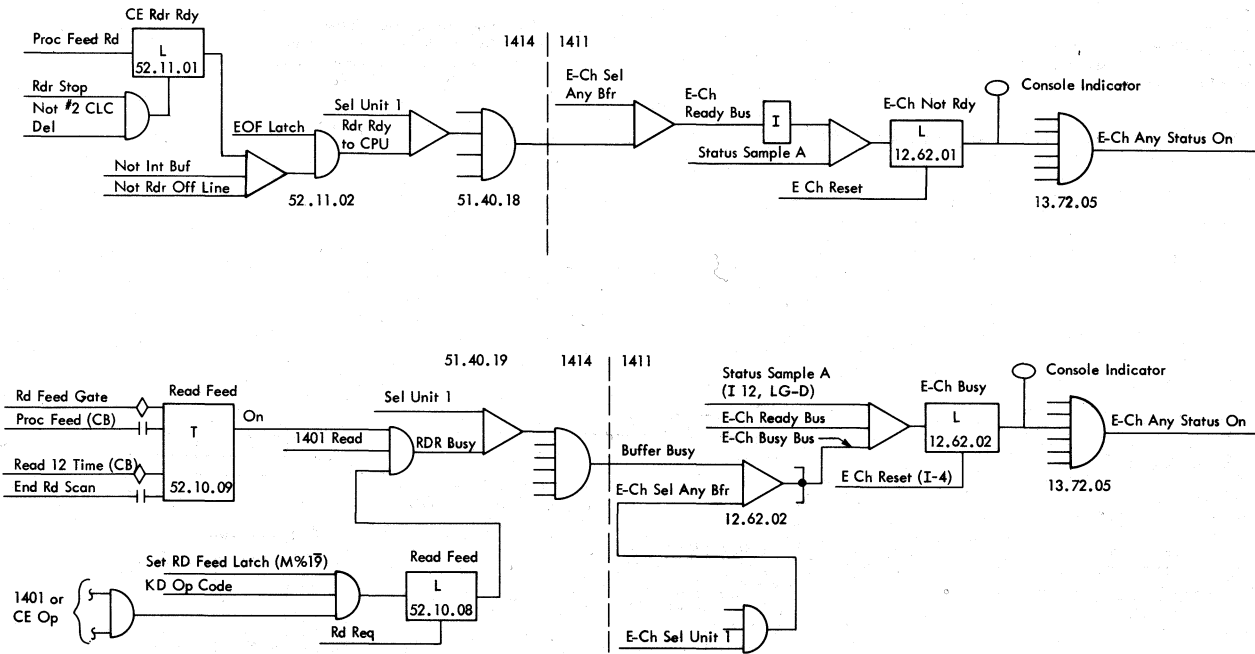


Figure 31. Channel Not Ready and Busy – Condensed Logic

read-out cycle (LIROC). Status sample A delay tests the outputs of the indicators.

Status Sample A I-12 LG D
 Status Sample A Delay I-12 LG E

If any status indicators are set during LIROC, last execute cycle is generated and the operation is terminated at the end of I-phase. If no indicators are set, one of the four channel in process latches is set and E phase occurs. Figure 33 shows the set of the channel 1 unoverlap in process latch, which controls an E-channel unoverlapped operation.

I-Phase Logic Flow

Figure 34 is a logic chart for instruction read out of a move or load command. The overall logic flow is the same for any move or load command. Variations are shown for IBM 1301, IBM 1405, IBM 1402, and tape move or load commands.

Use Figure 34, Sheet 5 in conjunction with the logic flow chart.

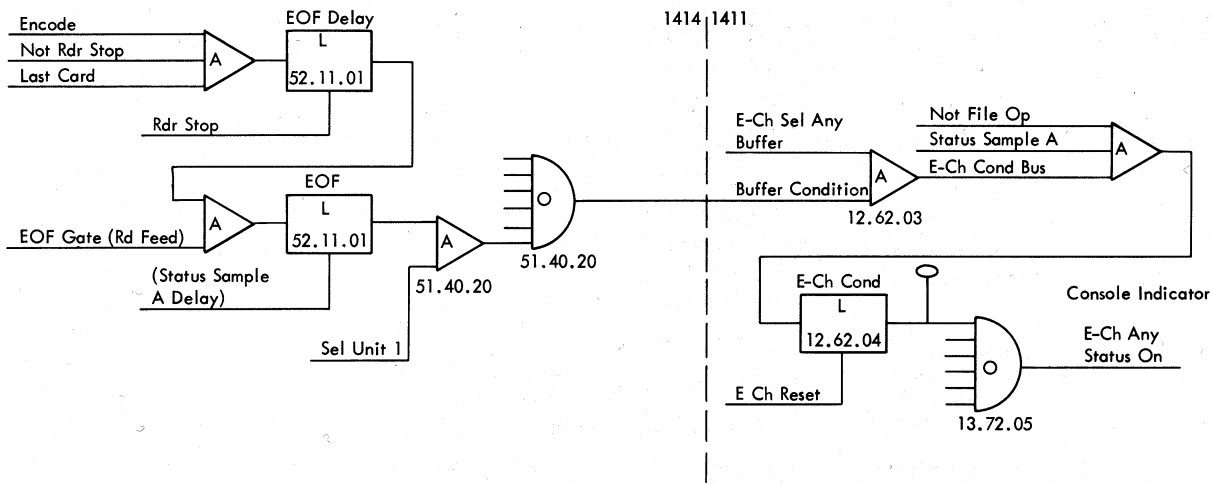


Figure 32. Channel Condition

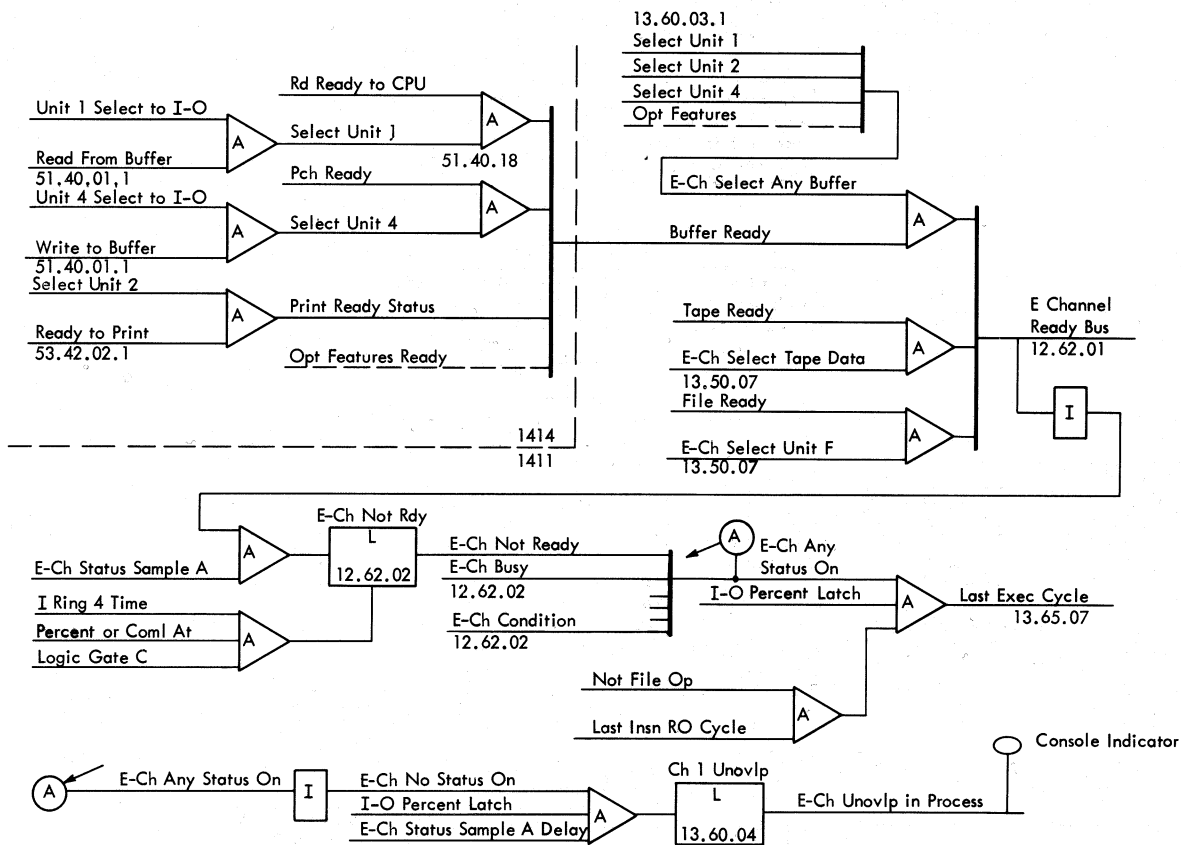


Figure 33. Any Status On

E-Phase Functions

The intent here is to acquaint the Customer Engineer (CE) with the key latches and signals that are associated with E-phase. A thorough understanding of these highlights of E-phase provides the CE with a broad concept of E-phase functions before studying a detailed operation for a specific i-o device.

E- and F-channel operations are similar; only E-

channel operation is described here. E-phase may be divided into three parts: Initiation (partly accomplished during LIROC); i-o data cycles; and termination.

Initiation

On an overlapped move or load command, the contents of the op register, i-o channel select register, and the op modifier register may be lost when the next instruc-

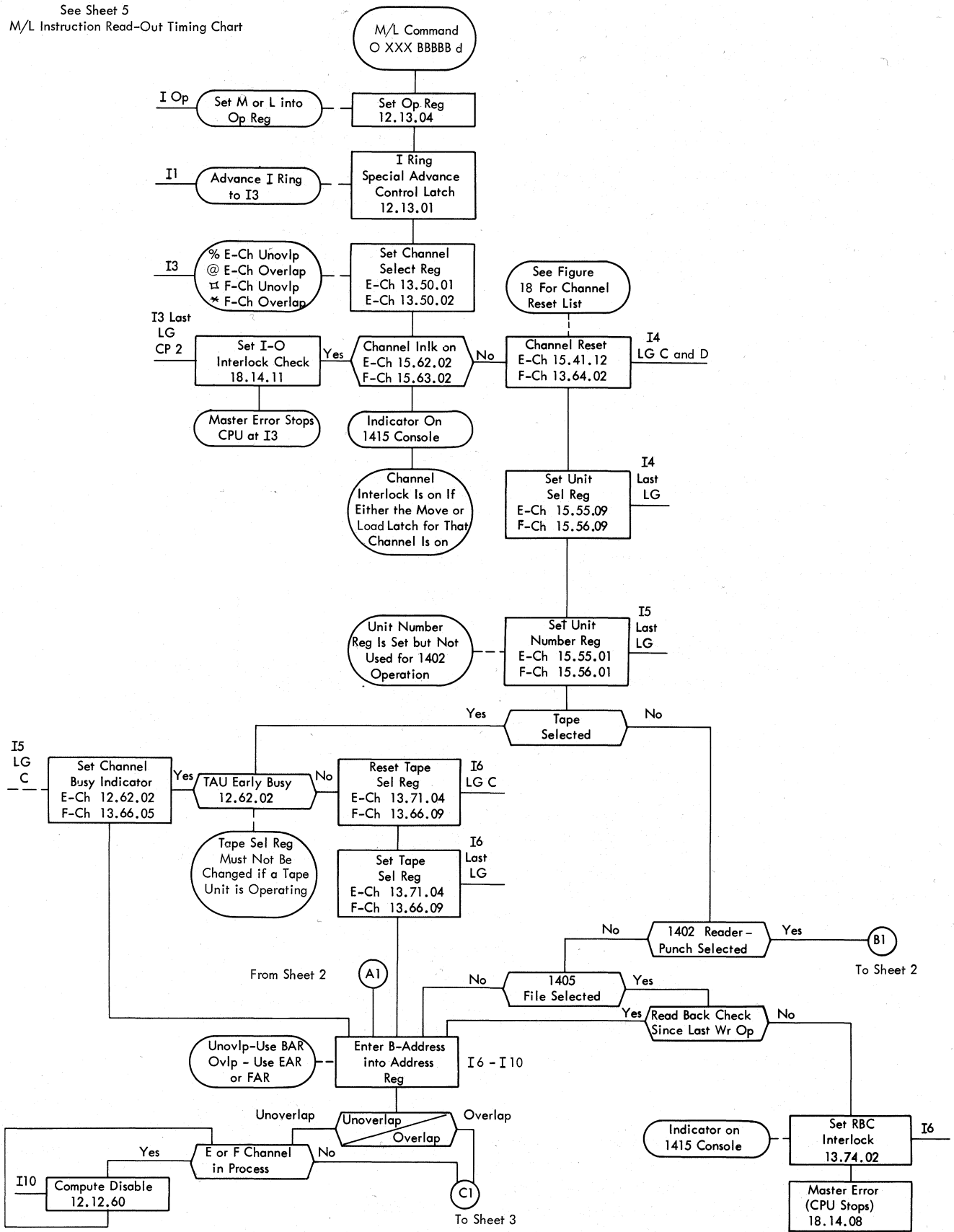
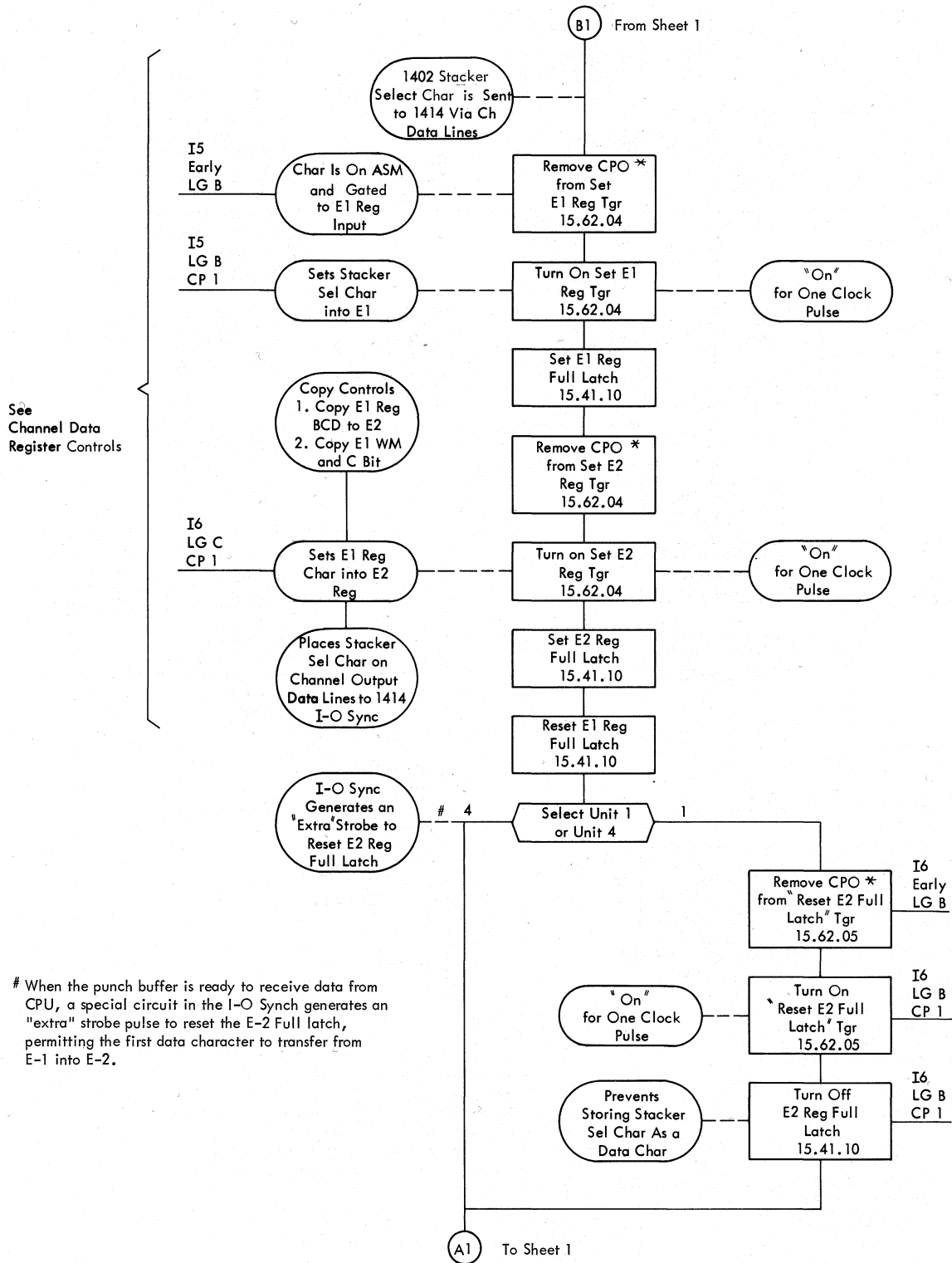


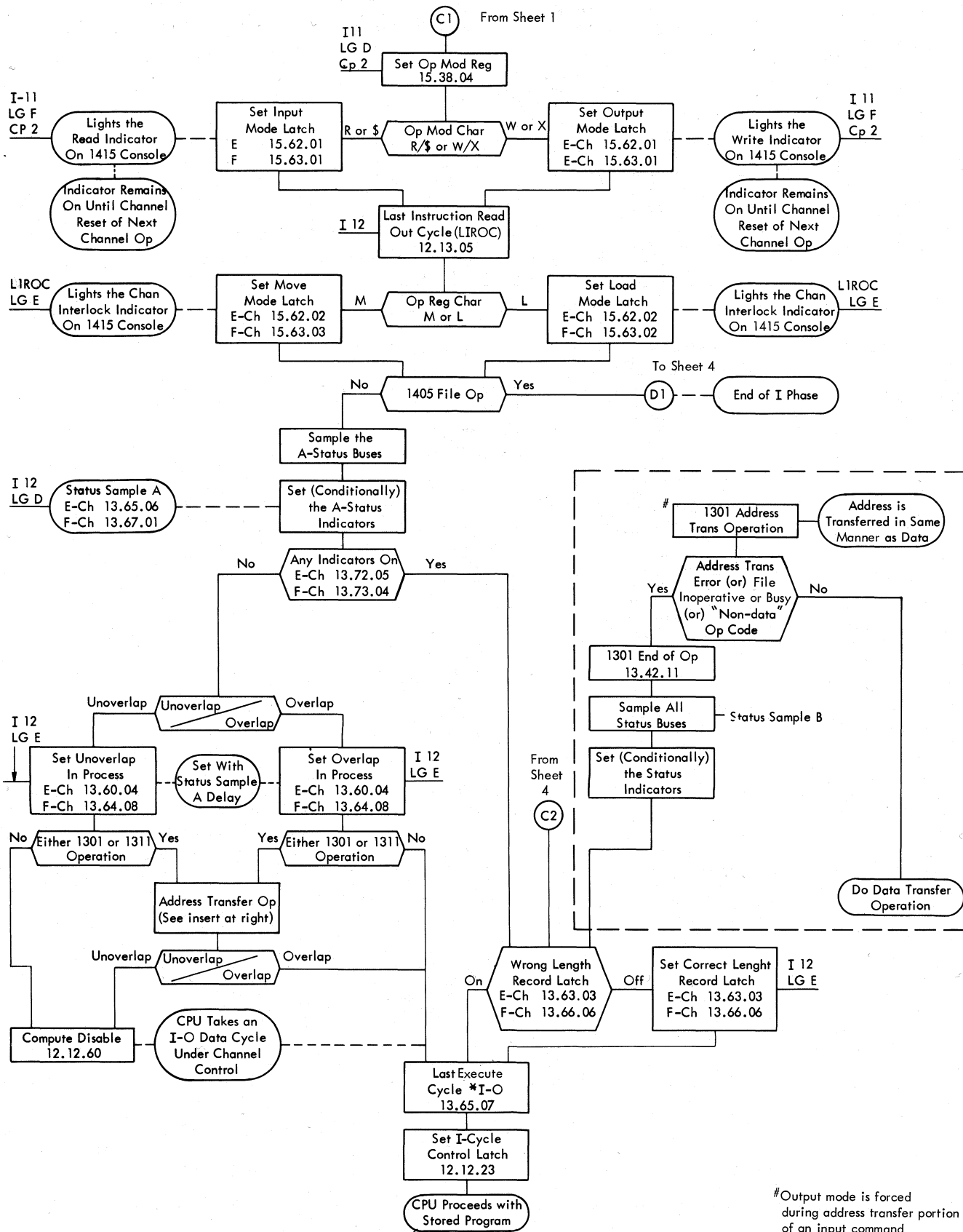
Figure 34. Move or Load Instruction Read-out (Sheet 1 of 5)



When the punch buffer is ready to receive data from CPU, a special circuit in the I-O Synch generates an "extra" strobe pulse to reset the E-2 Full latch, permitting the first data character to transfer from E-1 into E-2.

* Collector Pullover

Figure 34. Move or Load Instruction Read-out (Sheet 2 of 5)



#Output mode is forced during address transfer portion of an input command

Figure 34. Move or Load Instruction Read-out (Sheet 3 of 5)

Note: See 1405 Customer Engineering Manual of Instruction, Form 227-5542 for detailed flow charts of 1405 operations.

See 1405 Disk Control Commands section of this manual

#Output mode is forced during address transfer

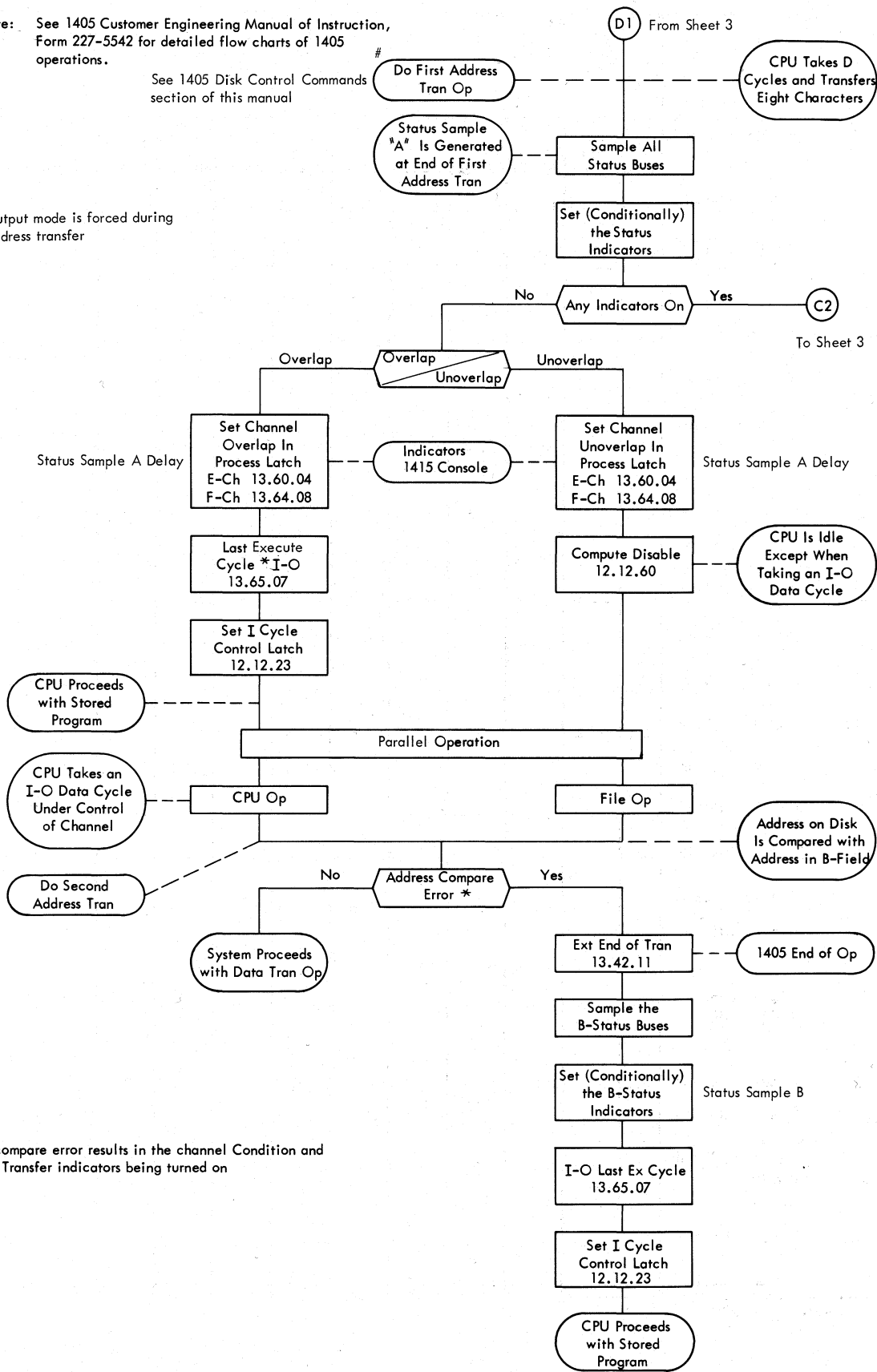
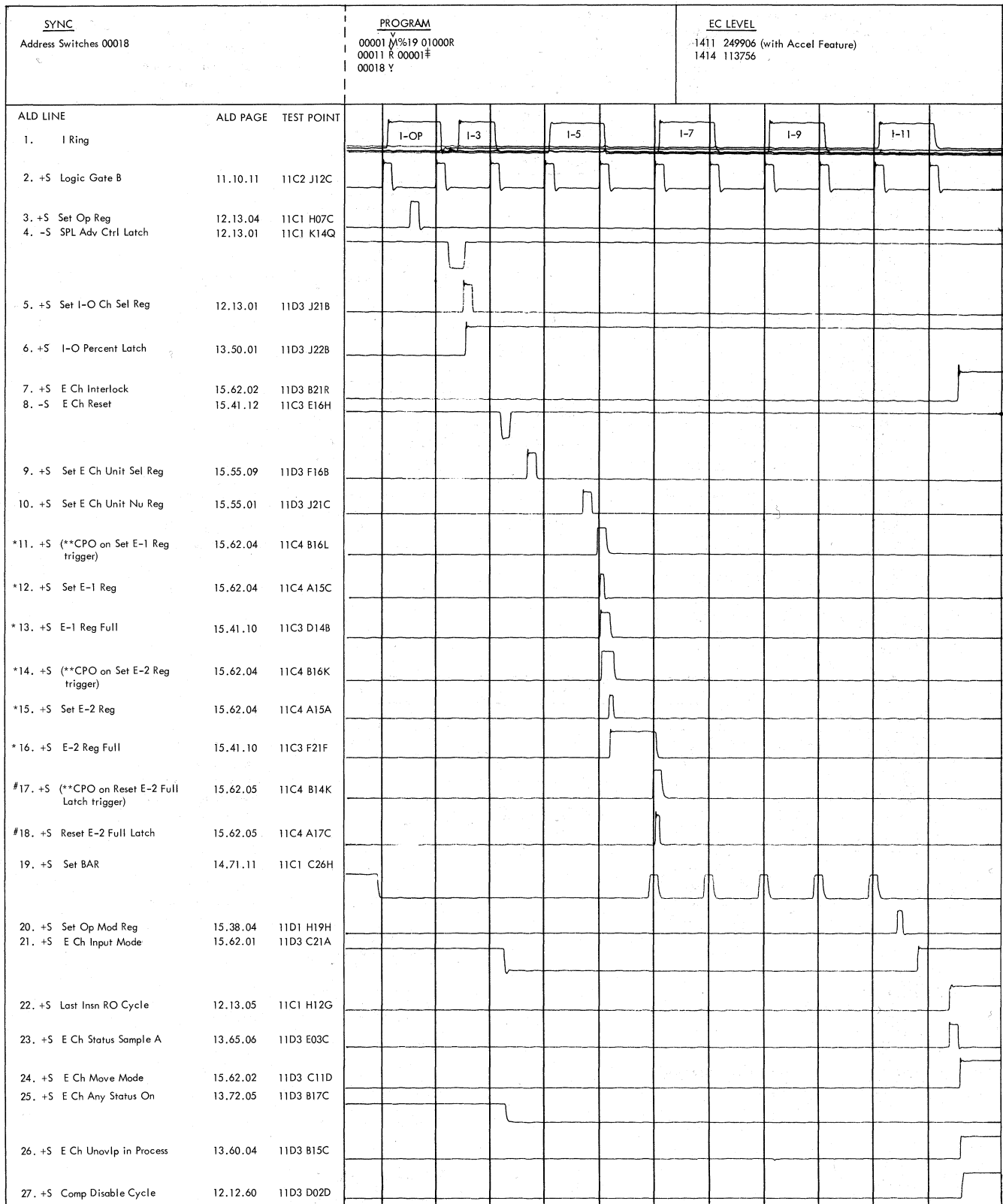


Figure 34. Move or Load Instruction Read-out (Sheet 4 of 5)



* 1402 Card Read-Punch only (for stacker select character)
 ** CPO - collector pullover
 # 1402 Card Read only

Figure 34. Move or Load Instruction Read-out (Sheet 5 of 5)

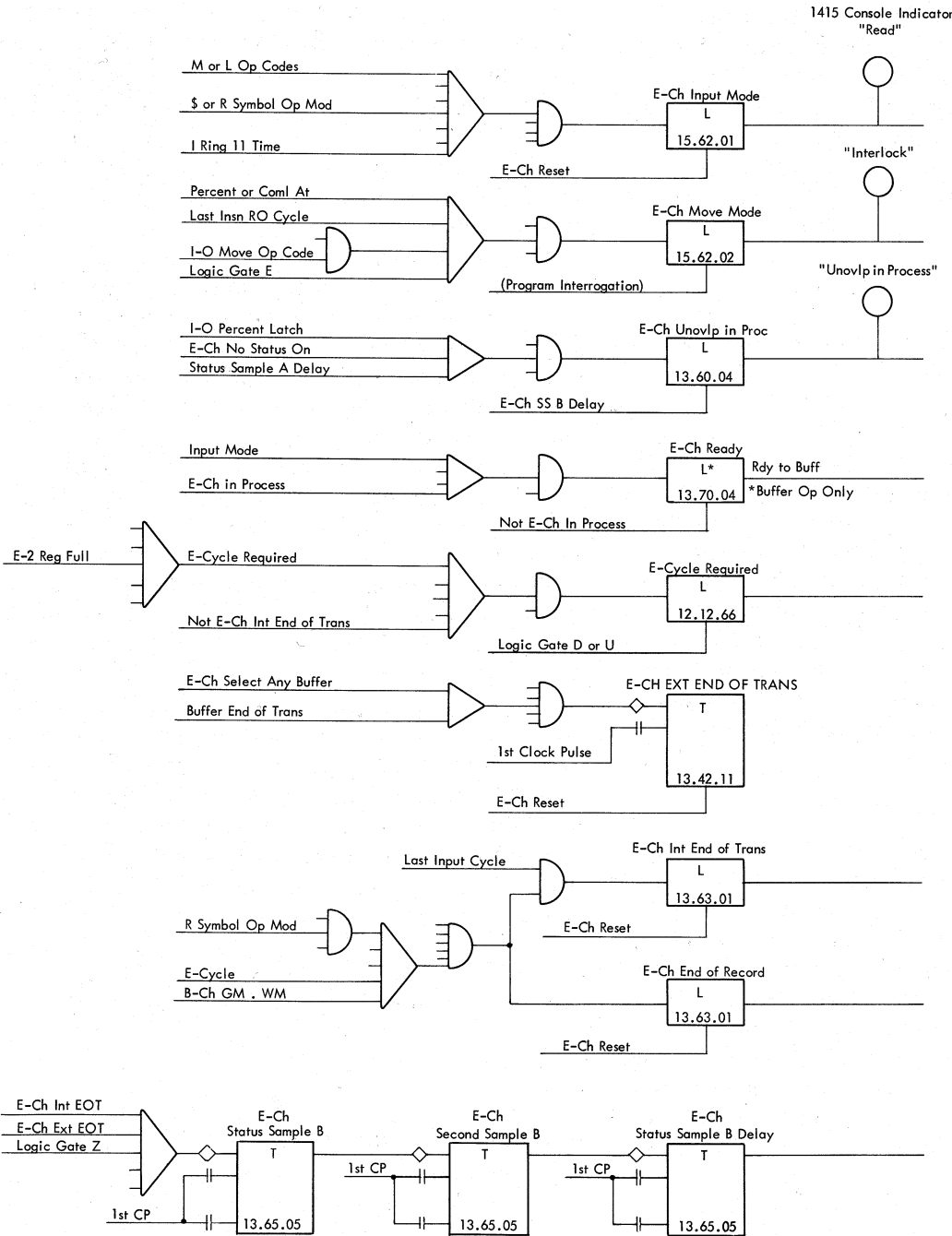
tion word is read out. Therefore, the information from these registers is stored in the channel control latches so the overlapped operation may occur while the computer continues with the stored program. The information is stored in the channel control latches for both overlapped and unoverlapped commands. The control latches are:

- | | |
|------------------------|------------------|
| E-ch unovlp in process | E-ch move mode |
| E-ch ovlp in process | E-ch load mode |
| E-ch input mode | E-ch output mode |

F-channel has a similar set of latches. Figure 35 shows the control latches turned on for an input move mode command. The E-channel ready latch is used only for a buffer operation (IBM 1414 I-O Synchronizer, Models 3, 4, or 5) or IBM 1442-3 Card Read Punch operation.

I-O DATA CYCLES

Data transfer operation is primarily a function of the channel data registers and is covered in the previous



Key latches and triggers that control E phase of a buffer input operation

Figure 35. Channel Control Latches – Simplified Logic

section. (See Figures 99, 114, 115, and 116 in the reference section).

TERMINATION

To terminate E-phase of any E-channel move or load command, two lines must be active: E-channel Internal end of transfer and E-channel External end of transfer. See Figures 35 and 36. With both internal and external end of transfer, three successive pulses, each two clock pulses in duration, are generated.

1. E-channel Status sample B samples the B-status buses and sets, conditionally, selected channel status indicators. During unoverlapped commands it sets the I-O last execute cycle latch (Figure 120).

2. E-channel second sample B is used to sample the outputs of selected channel status indicators. The signals generated vary with the different operation.

3. E-channel status sample B delay turns off the channel in process latch (Figure 35).

E-Phase Status Indicators

Status indicator charts for the various I-O devices are shown in the reference section.

E-CHANNEL DATA CHECK

Figure 37 shows the read check latch in the IBM 1414 gated to the check bus by select unit 1 (reader). At status sample B time, a reader error status is transferred to the channel (data) check status indicator.

During input operation, a parity error input character may appear on the A-channel. Because this is a transient error condition, it must be sampled immediately. The bottom input to the E-channel check latch (Figure 37) provides a turn on for the latch during every E-cycle if there is a parity error (I-O check) on the A-channel.

E-CHANNEL WRONG LENGTH RECORD

During the input operation with a GM-WM properly positioned in the input field, the turn on of the E-channel wrong length record (WLR) latch is blocked as follows: after external end of transfer occurs and the last input character is stored, E-cycle required is generated by a special circuit (Figure 38) forcing an extra E-cycle to test the B-channel for a GM-WM. During this E-cycle, a GM-WM on the B-channel sets both the end of record latch and the internal end of transfer latch. The inverted output of the end of record latch blocks the turn on of the E-channel WLR latch. See Figure 36.

If the E-channel WLR latch is not turned on, then the E-channel correct length record (CLR) is turned on (Figure 90). The two latches, WLR and CLR, must be in agreement at the end of an I-O operation or a sub-

sequent programmed test of the WLR indicator (BWL1 - R IIII -) results in a mismatch between the branch latch and the no branch latch. An instruction check occurs during a branch operation if the branch and no branch latches do not match.

The last input cycle latch is turned on during input operations where an extra E-cycle is taken to check for a B-channel GM-WM. The two cases where the latch is turned on are:

1. a. The input move or load command has an R d-character.

- b. All input characters have been stored and neither a GM-WM or wrap-around (end of storage) has been sensed.

2. a. The input move or load command has a \$ d-character.

- b. All input characters have been stored and a wrap-around condition has not been sensed (this is a WLR condition).

The on output of the latch:

1. Sets the internal end of transfer latch (if no GM-WM is sensed on the extra cycle to turn on the internal end of transfer latch).

2. Blocks the set of the end of record latch from a wrap-around condition during the extra E-cycle (input field is one position too long).

3. Blocks the A-channel VC error circuits.

4. Conditions the assembly controls to use the B-channel character (to regenerate the character read out on the extra E-cycle).

During output mode operation with a fixed-length record I-O device, if the GM-WM is located too early in the output field (short field), "E-channel strobe" causes a WLR indication (Figure 38). If there is no GM-WM, or it is located too late in the output field, "E-2 reg full" causes a WLR indication. If there is no GM-WM in the output field and the I-O device selected is a fixed-length record device, external end of transfer forces internal end of transfer to end the operation (Figure 101).

If the E-channel ready bus becomes inactive while the E-channel is in process, the external end of transfer trigger is turned on, ending the operation (Figure 101).

E-CHANNEL NO TRANSFER

Because the use of this indicator varies with the selected unit, no attempt is made here to describe the no transfer indicator. See Figure 105.

Processing Overlap Logic

The processing overlap feature allows the IBM 1410 Data Processing System to take compute cycles during much of the time an I-O instruction is being executed.

Consider first a read operation involving an IBM 1414 Synchronizer and IBM 1402 Card Read Punch. The

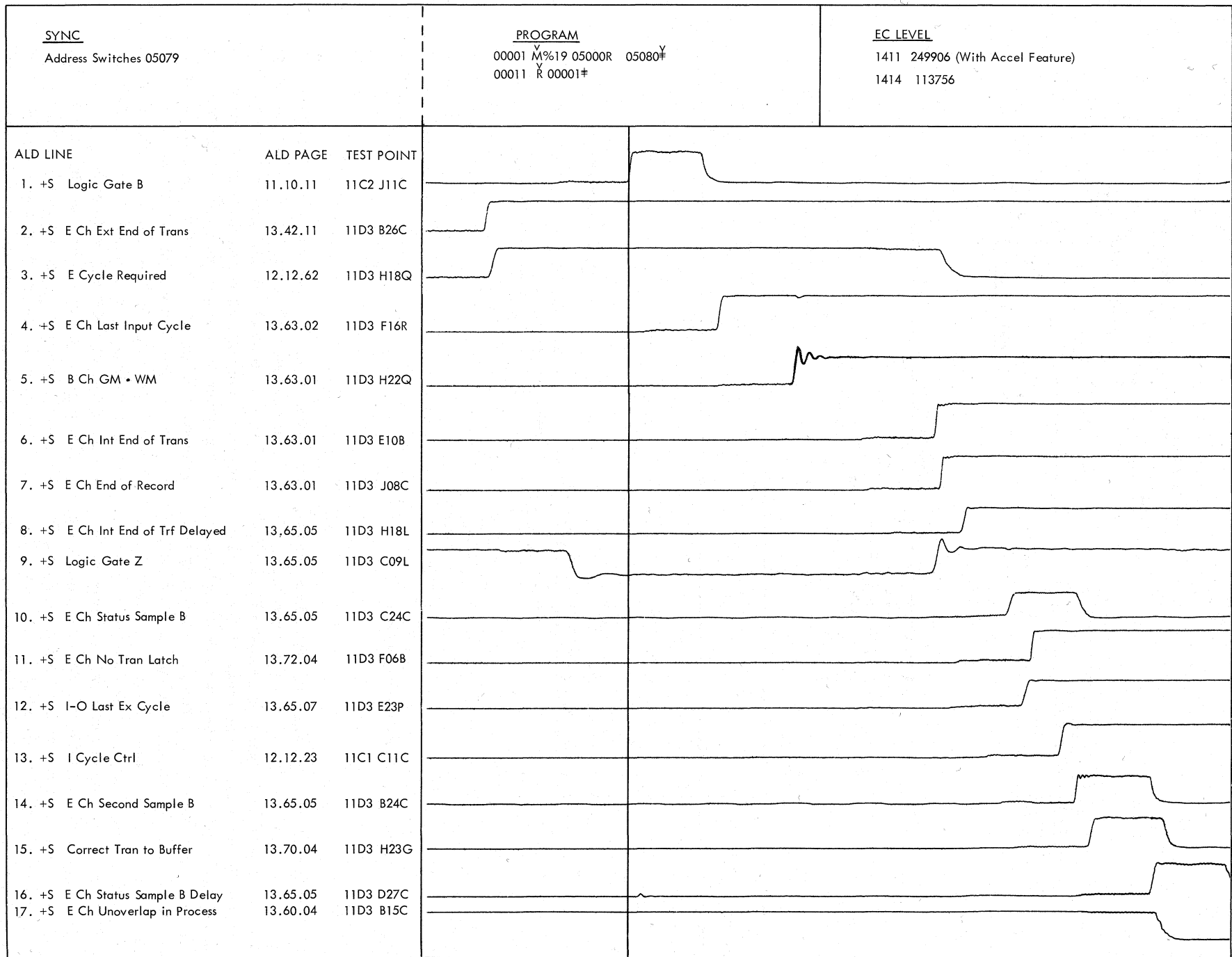


Figure 36. Input End of Transfer Timing Chart

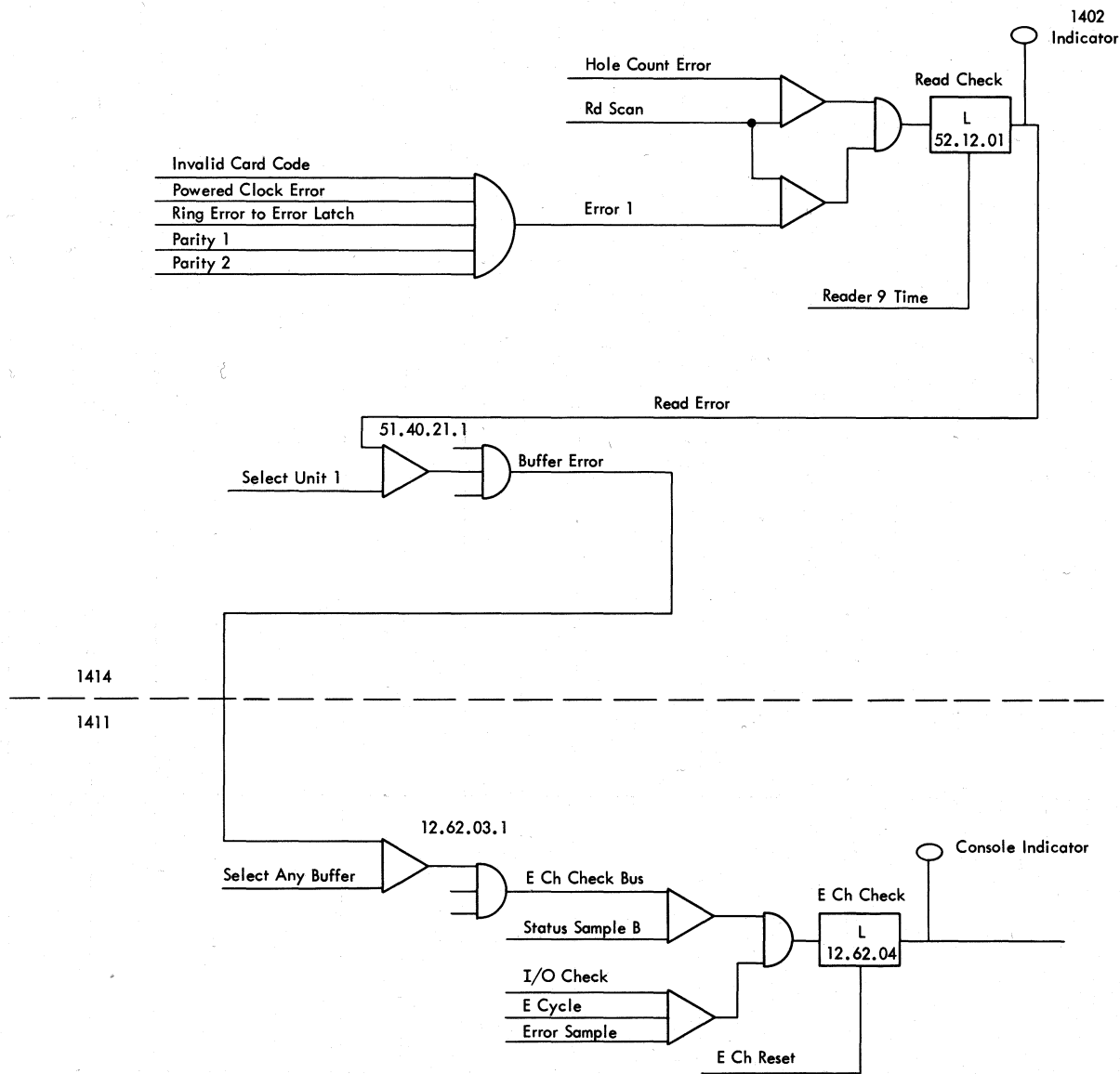


Figure 37. Channel Data Check – Condensed Logic

1414 can process one character every 11 microseconds. The 1410, however, can accept a character in just 4.5 microseconds (4.0 microseconds with Accelerator Feature). Without the processing overlap feature, the 1410 would be idle 6.5 microseconds out of every 11 microseconds whenever an i-o instruction was being executed. With the processing overlap feature, however, the idle time can be used for compute cycles if the i-o instruction is given in overlap mode.

The time saving becomes even more important when a tape operation is considered. Because transferring data to or from a magnetic tape unit is an essentially unbuffered operation, the data transfer must wait from read (or write) call time until the tape unit gets up to full speed. For an IBM 729-II Magnetic Tape Unit

this starting time is approximately 7.5 milliseconds. With the processing overlap feature, this time can be used to take compute cycles; also, because the tape operation is unbuffered, the data transfer character rate is dependent on the tape unit and not the 1414; for instance, a 729-II reads or writes one character every 67 microseconds (or two characters every 134 microseconds). Most of this time can be used for compute cycles if overlap mode is specified since the 1410 can handle a character in 4.5 microseconds.

When an i-o instruction is given, the second character of the instruction specifies which channel to use and whether or not the instruction is to be overlapped. For the E-channel, a percent sign (%) specifies unoverlap mode, and a commercial at sign (@) specifies

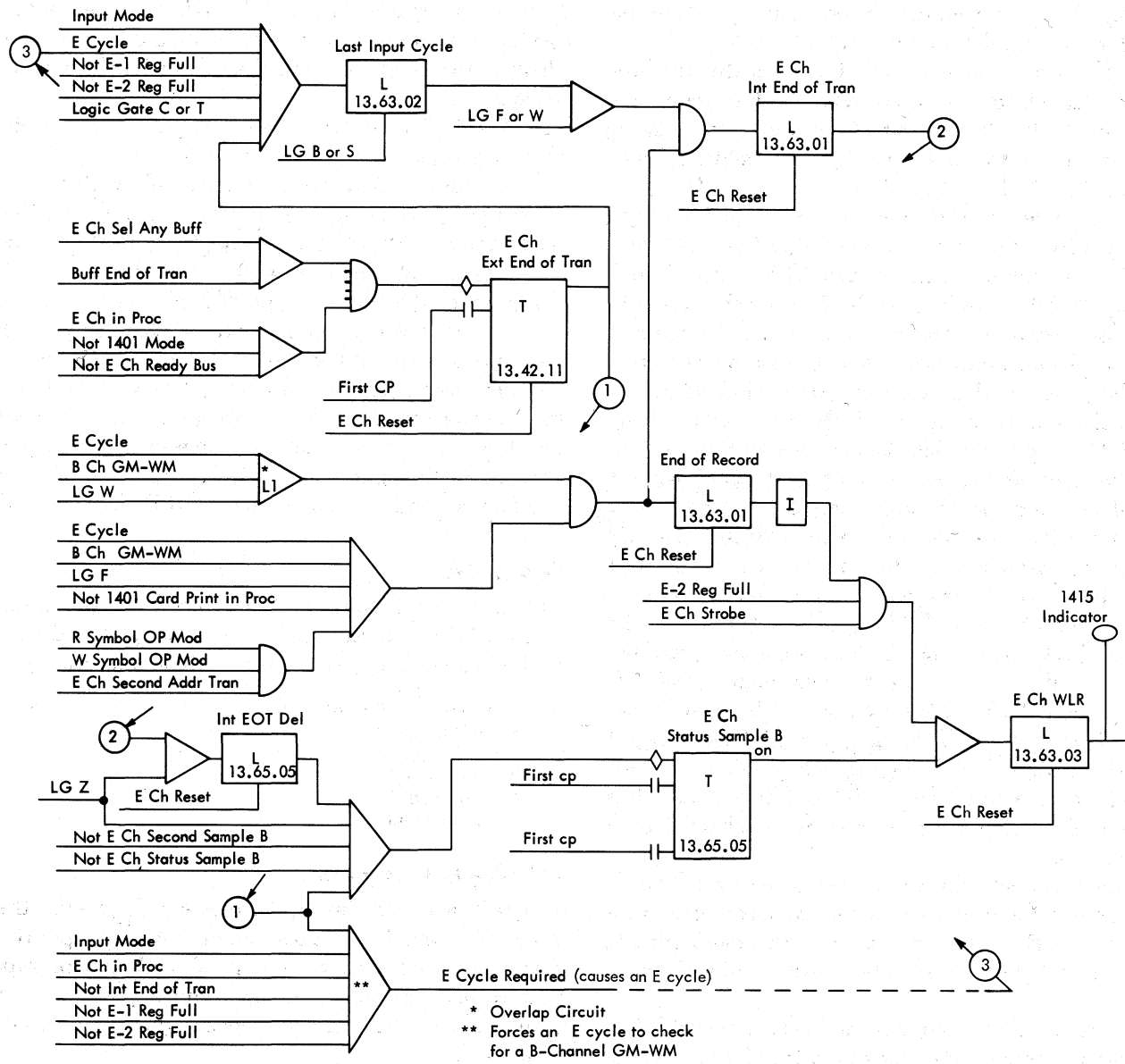
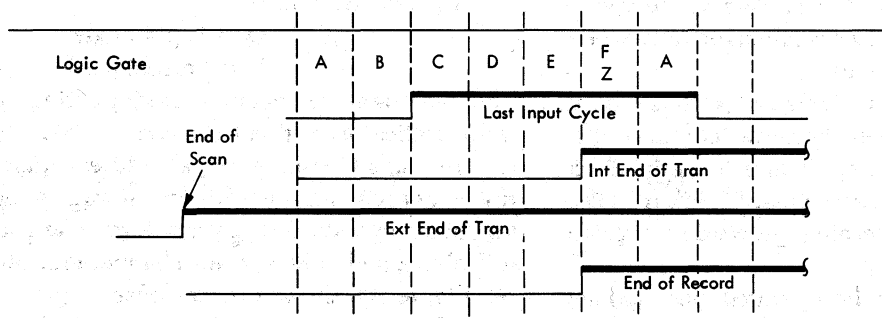


Figure 38. Channel Wrong Length Record



overlap. For the F-channel, the characters used are the asterisk (*) and the lozenge (◻).

If the instruction is an overlapped instruction for the E-channel, the EAR is set with the instruction address by mixing the output of the I-O commercial at latch with "B-chan not WM-bit," "2nd address," and "insn no gate" (logic 14.71.15).

At I-12 time, the E-channel overlap in process latch sets by mixing the I-O commercial at latch output with "E ch status sample A delay" and "E ch no status on" (logic 13.50.01). As long as the E-channel overlap in process latch is on, another E-channel instruction or F-channel unoverlap instruction cannot be executed.

When the I-O data transfer operation begins, the channel controls bring up "E-cycle required" (logic 12.12.62), requesting that the CPU take an E-cycle. The channel controls also cause "compute disable" to come up which interrupts the logic clock ring by not allowing logic gate A to come on (logic 11.10.10). "E-cycle required" permits the extension clock ring to start when logic gate Z comes on (logic 11.10.20).

For output cycles, "E cycle required" (logic 12.12.63) is set by ANDING "E ch output mode" with "not E-2 reg full" on logic 12.12.63. For input cycles, "E-cycle required" is set by ANDING "E ch input mode" with "E-1 reg full." "E-cycle required," then, sets just as E-1 transfers to E-2 when in output mode, and just as E-1 transfers to E-2 when in input mode. Data flow through E-1 and E-2 is discussed in the Channel Data Registers section.

Only one clock may run at any given time. During overlap execute cycles either the extension clock runs to time the E- or F-cycles, or the main clock runs to time the compute cycles taken between the E- or F-cycles.

To insure that each channel gets serviced often enough to complete an overlapped instruction successfully, priority is assigned to the E-channel, followed by the F-channel. Compute cycles are taken only when the channels require no service.

A branch on channel status cannot be made until the I-O instruction is complete because "compute disable" is brought up by mixing "I-ring 5" with "E ch in process" and "branch on status chan 1" (Figure 117).

Some general rules concerning processing overlap are:

1. Only one I-O unit can be operated per channel at any given time, whether or not overlap mode is being used.
2. If one channel is operating in overlap mode, the other channel may not operate in unoverlap. However, both channels may operate in overlap mode simultaneously.
3. Status indicators should be tested for the last I-O instruction before executing another I-O instruction.

If program attempts to check the indicators before the channel operation is complete, "compute disable" interrupts the program until the channel operation is finished.

4. The E-channel has priority unless the last cycle was an E-cycle.

5. A \$ or X d-character is effective only with an un-overlapped command. For example, an overlapped read command using an \$ d-character is treated as an overlapped read command with an R d-character.

Figure 13 illustrates a typical application of processing overlap. A reel of tape on the E-channel is being copied onto a reel of tape on the F-channel. The reading and writing is done in overlap mode so that the time between the E- and F-cycles can be used to move the data from an input area of memory to an output area. Refer to Figures 115, 116, 117, 119, and 120 for overlapped read command with an R d-character.

Service Note

Because close timing conditions occur in the areas listed below, excessive delay or accumulated delays in the logic circuits may cause machine failures.

CHANNEL REGISTERS AND CONTROLS

E-cycle required
F-cycle required
E-cycle control
F-cycle control
Address channel

I-O No-Op Command

IBM 1410 Data Processing Systems equipped with the processing overlap feature often have the priority feature as well. Systems equipped with the priority feature may use an I-O no-op command, which is a standard M/L command with special d-characters. For example:

M/L xxxBBBBB b

Q = Input mode

V = Output mode

The I-O no-op command permits setting of channel status indicators without transfer of data (Exception: In a disk storage operation, an address transfer operation may occur.) Except for disk storage operation, the I-O no-op operation is always terminated at the end of I-phase, and only A-status channel indicators can be set. Figure 105 shows the condensed logic for termination of an I-O no-op command. "Q + V Symbol op mod" AND's with "not E ch sel unit F" and "E ch status sample A" to set the CLR latch. The output of the CLR latch brings up "any status on" which develops "last execute cycle * I-O" (Figure 120).

During file operation of the IBM 1405 Disk Storage, "status sample A" does not occur until the end of first address transfer (Figure 101). At that time, the opera-

tion is terminated (by turning on the CLR latch) for any of the following lines that are active (Figure 105):

- Q + V symbol op mod
- E-channel check bus
- E-channel unit number 0

During 1301-1311 operation, "status sample A" occurs at the normal time (I-12). If no status indicators are turned on at status sample A time, a channel in process latch is turned on and second address transfer occurs. (There is no first address transfer in 1301 operation.) At the end of second address transfer of an I-O no-op command, the 7631 (1301 control unit) generates "1301 end of operation" which turns on the external end of transfer trigger to end the operation (Figure 101).

Summary: Use of the I-O No-Op Command

With other than disk storage devices

1. No data transfer occurs
2. No E-phase occurs
3. Only A-status indication may be set
4. Operation is terminated at end of I-phase.

With 1405 Disk Storage

1. No data transfer occurs
2. E-phase does occur
3. First address transfer follows I-phase
4. Status sample A occurs at end of first address transfer
5. Only A-status indicators can be set
6. No channel in process latch is set
7. Operation is terminated at end of first address transfer.

With 1301/1311 Disk Storage

1. No data transfer occurs
2. Status sample A occurs at end of I-phase
3. E-phase occurs (if no status indicators on)
4. A channel in process latch sets (if no status indicators on)
5. Second address transfer occurs
6. Operation is terminated at end of address transfer
7. Status sample B occurs at end of address transfer
8. Both A-status and B-status indicators can set.

Refer to IBM 1411 Processing Unit Instructions and Special Features, Customer Engineering Instruction-Reference Manual, Form 223-2698, and IBM 1410 Priority Feature, Systems Reference Library Publication, Form A22-0530, for additional information on the 1410 priority feature.

1411-1402 Reader Operation

For ease in understanding the following operations, you should be familiar with the information in the Input-Output Principles of Operation, Channel Data Register Controls, and I-O Sequence sections of this manual.

Information on the operation of the IBM 1402 Card Read Punch and the IBM 1414 I-O Synchronizer is contained in *IBM 1402 Card Read Punch Customer Engineering Instruction-Reference Manual, Form 231-0002*, and *IBM 1414 Input-Output Synchronizer, Customer Engineering Instruction-Reference Manual, Form 223-2590*.

Two commands are used with the 1402 Reader:

Read a card Mnemonic: R (move mode) RW (load mode)
 Example: M%1002000R
 Transfer buffer data to the CPU; take a card-feed cycle and reload buffer
 Example: M%1902000R
 Transfer buffer data to the CPU (no card-feed cycle)
 Select stacker and feed Mnemonic: SSF
 Example: K2
 Take a card feed cycle and load the buffer

Reader Move or Load Command

For instructional purposes, the diagrams are referred to at the appropriate points in the text. For reference purposes (trouble-shooting) refer to Figures 34, 39, 40, 41, 42, and 43.

INSTRUCTION FORMAT: O XXX BBBB R

Figure 44 shows the instruction format for a reader move or load op code. The hundreds position of the X-control field must contain one of these four characters or an instruction check occurs at the end of I-phase:

Percent sign	%	E-channel unoverlap
Commercial at	@	E-channel overlap
Asterisk	*	F-channel unoverlap
Lozenge	□	F-channel overlap

The units position of the X-control should contain one of these four characters:

0	Stack card in the normal read (NR) pocket
1	Stack card in the 1 pocket
2	Stack card in the 8/2 pocket
9	Transfer buffer data to CPU — Do not feed a card

If a read check occurs, the stacker select latches are reset and the error card is stacked in the normal read (NR) pocket.

The d-character must be one of the two following characters or a channel not ready indication occurs:

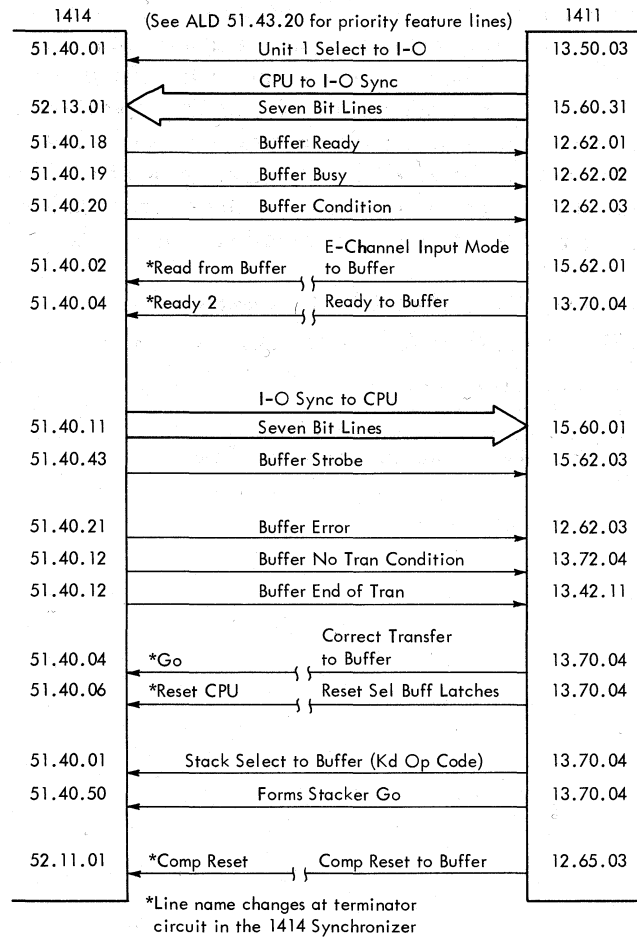


Figure 39. Channel Lines — Reader

- R Set input (read) mode and accept channel input characters until a GM-WM is sensed (read out of storage) or the end of storage (wrap-around) is sensed.
- \$ Set input (read) mode and accept channel input characters until the end of storage is sensed.

A dollar sign d-character is used to permit reading GM-WM characters into 1411 core storage without clearing the input field between read commands. A GM-WM character read into 1411 core storage could cause a premature termination of data transfer on the following read command if an R is used as the d-character.

If the reader terminates data transfer before the CPU senses a GM-WM or the end of storage, the end of trans-

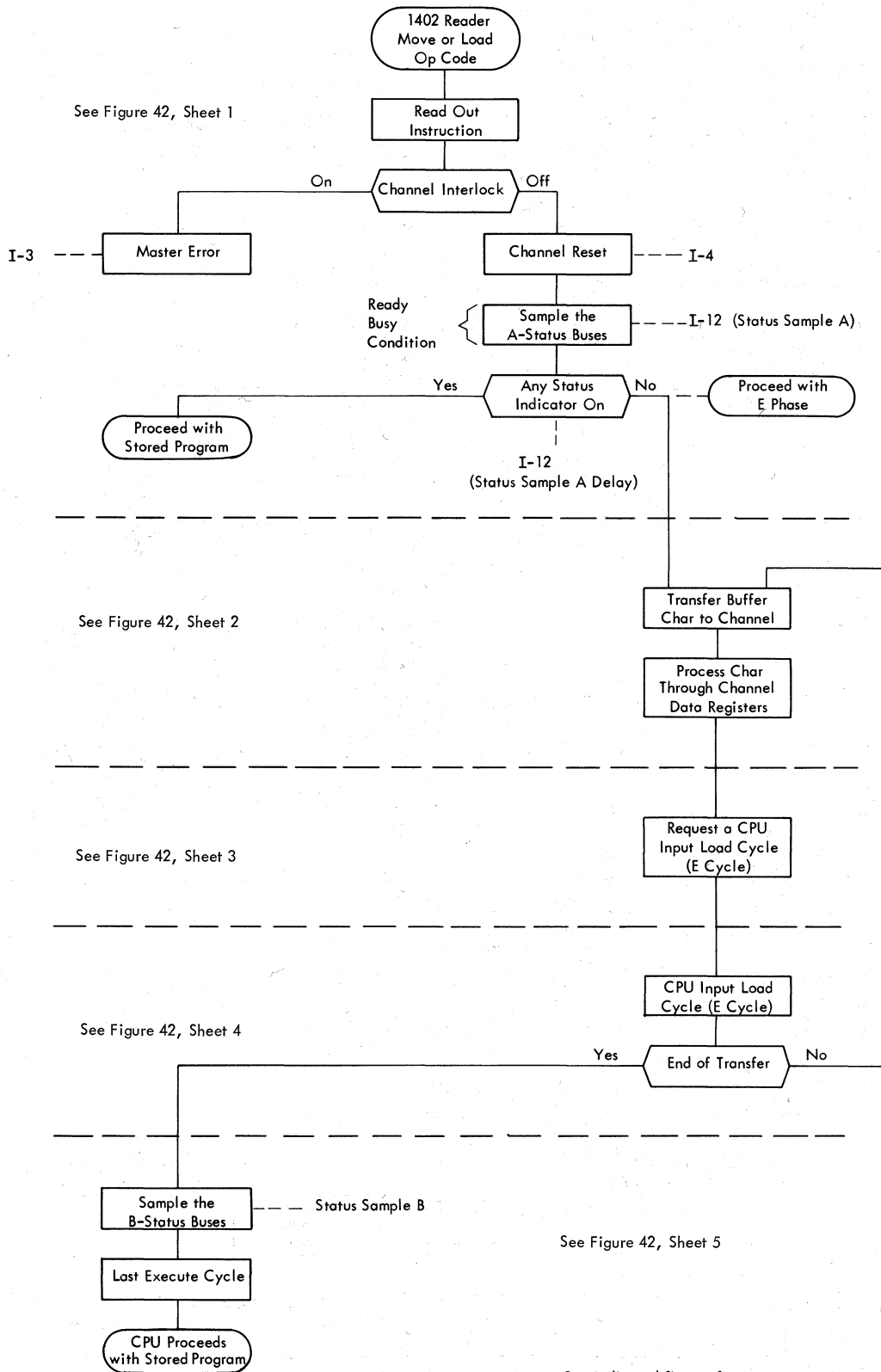


Figure 40. 1411-1402 Reader Operation – Basic Logic

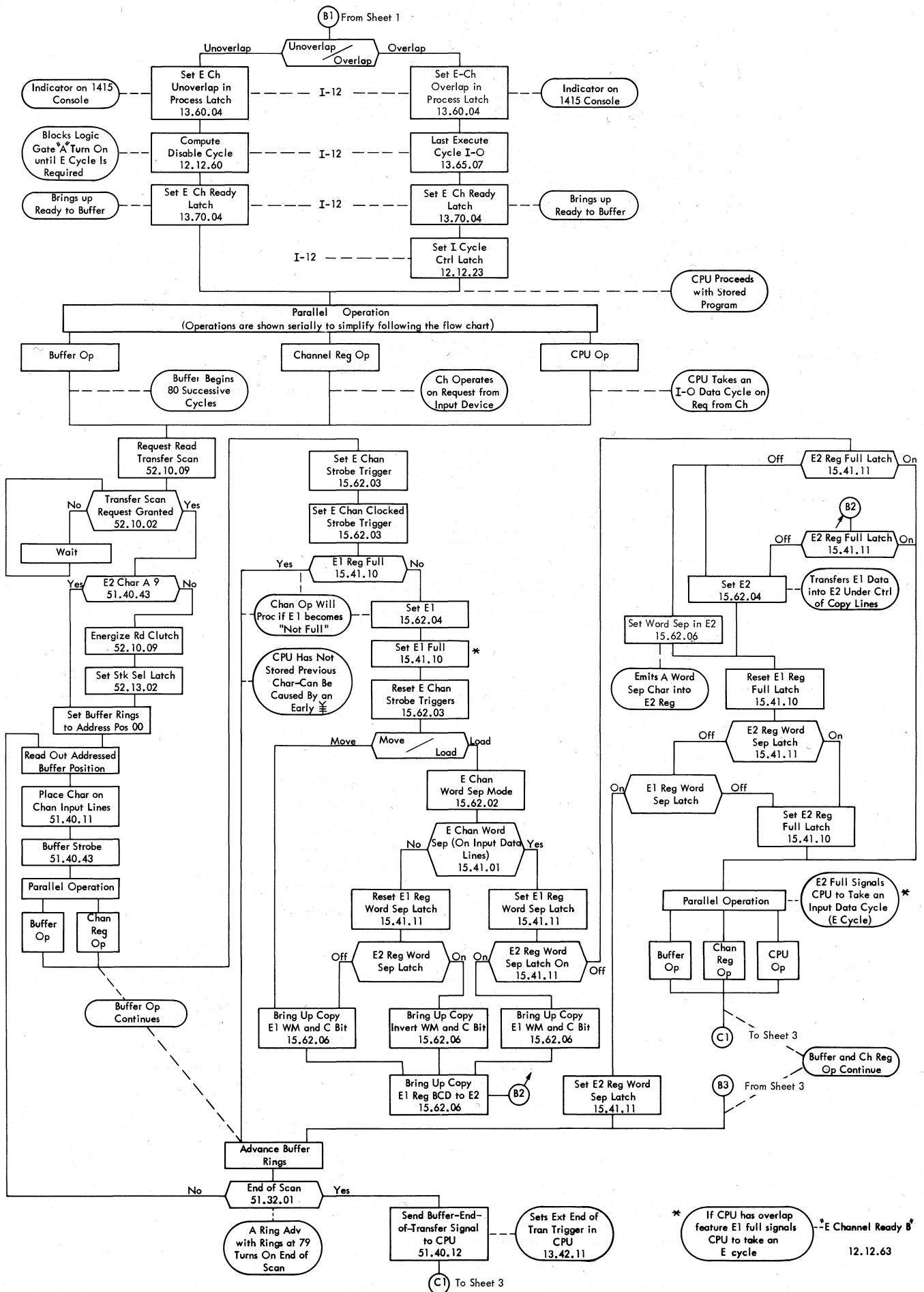


Figure 41. 1411-1402 Reader Operation – Logic Flow (Sheet 2 of 5)

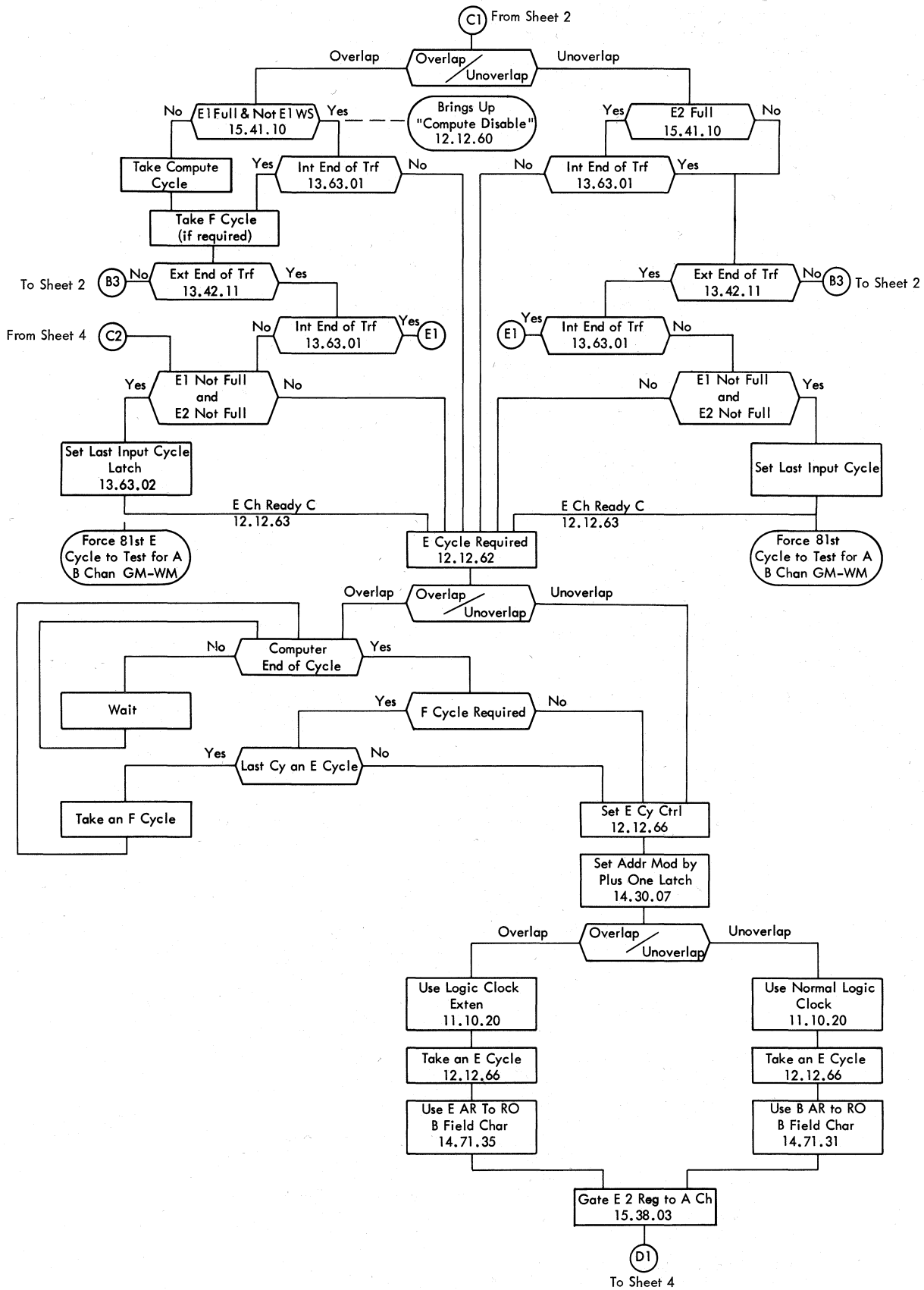


Figure 41. 1411-1402 Reader Operation – Logic Flow (Sheet 3 of 5)

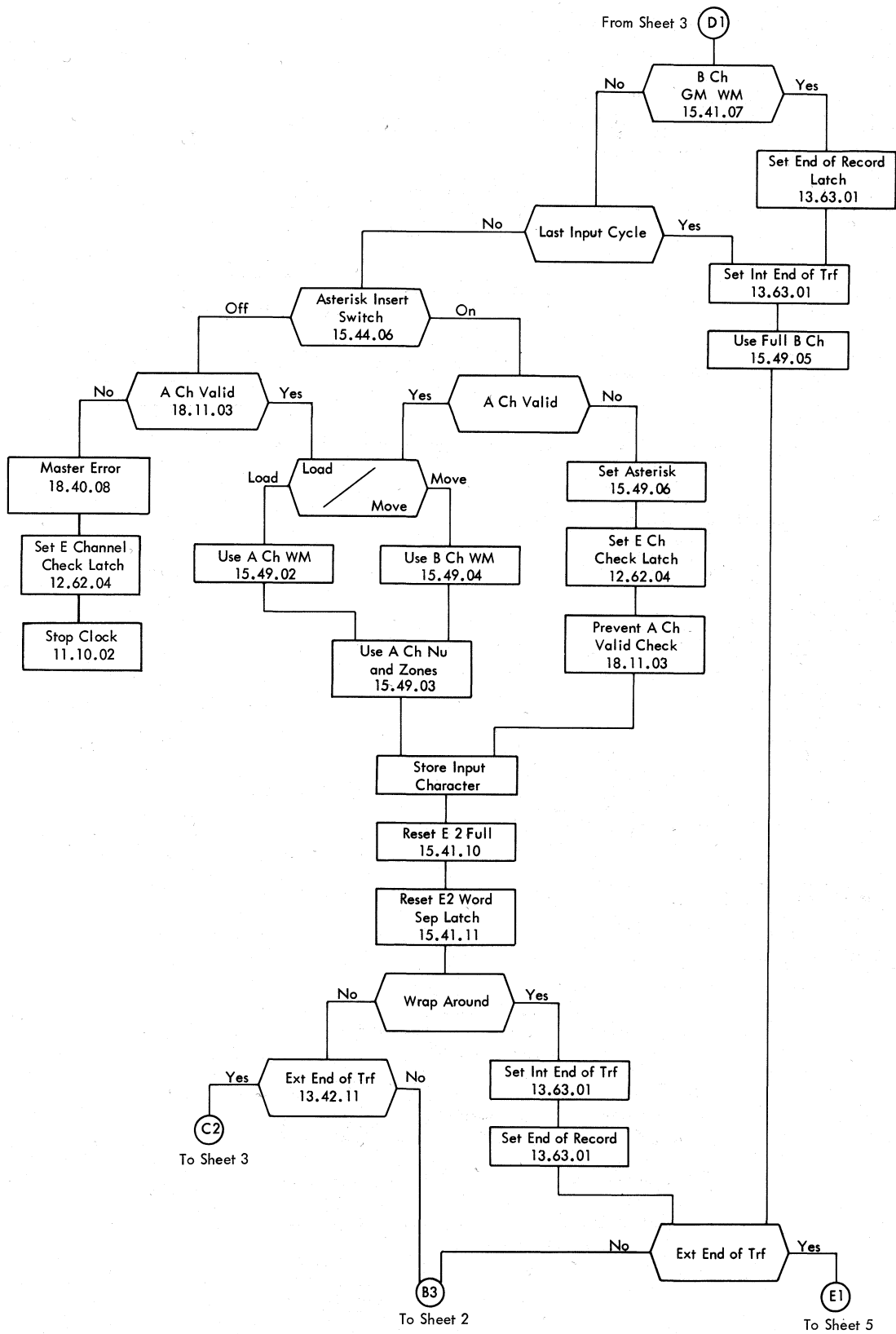


Figure 41. 1411-1402 Reader Operation – Logic Flow (Sheet 4 of 5)

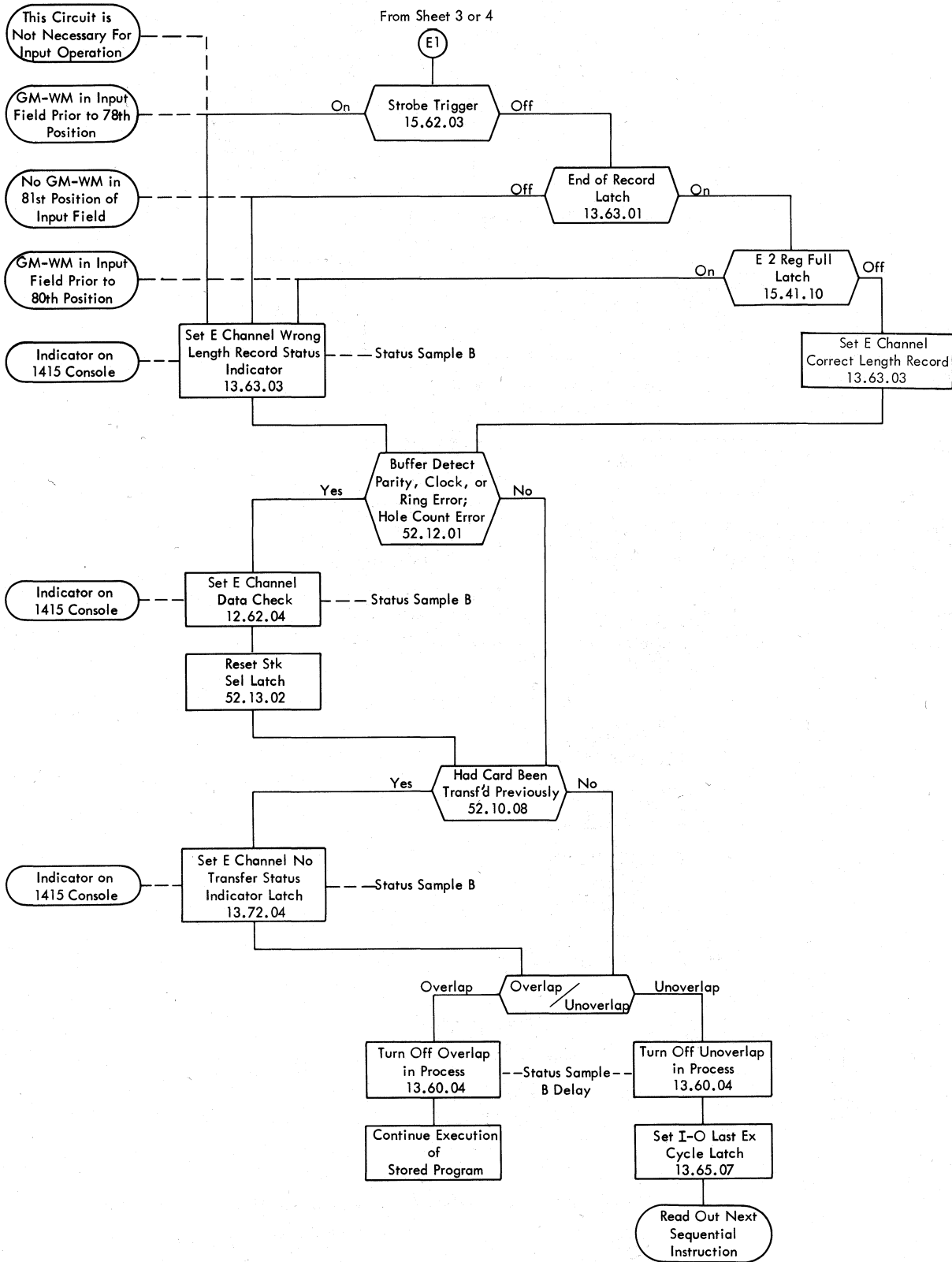


Figure 41. 1411-1402 Reader Operation – Logic Flow (Sheet 5 of 5)

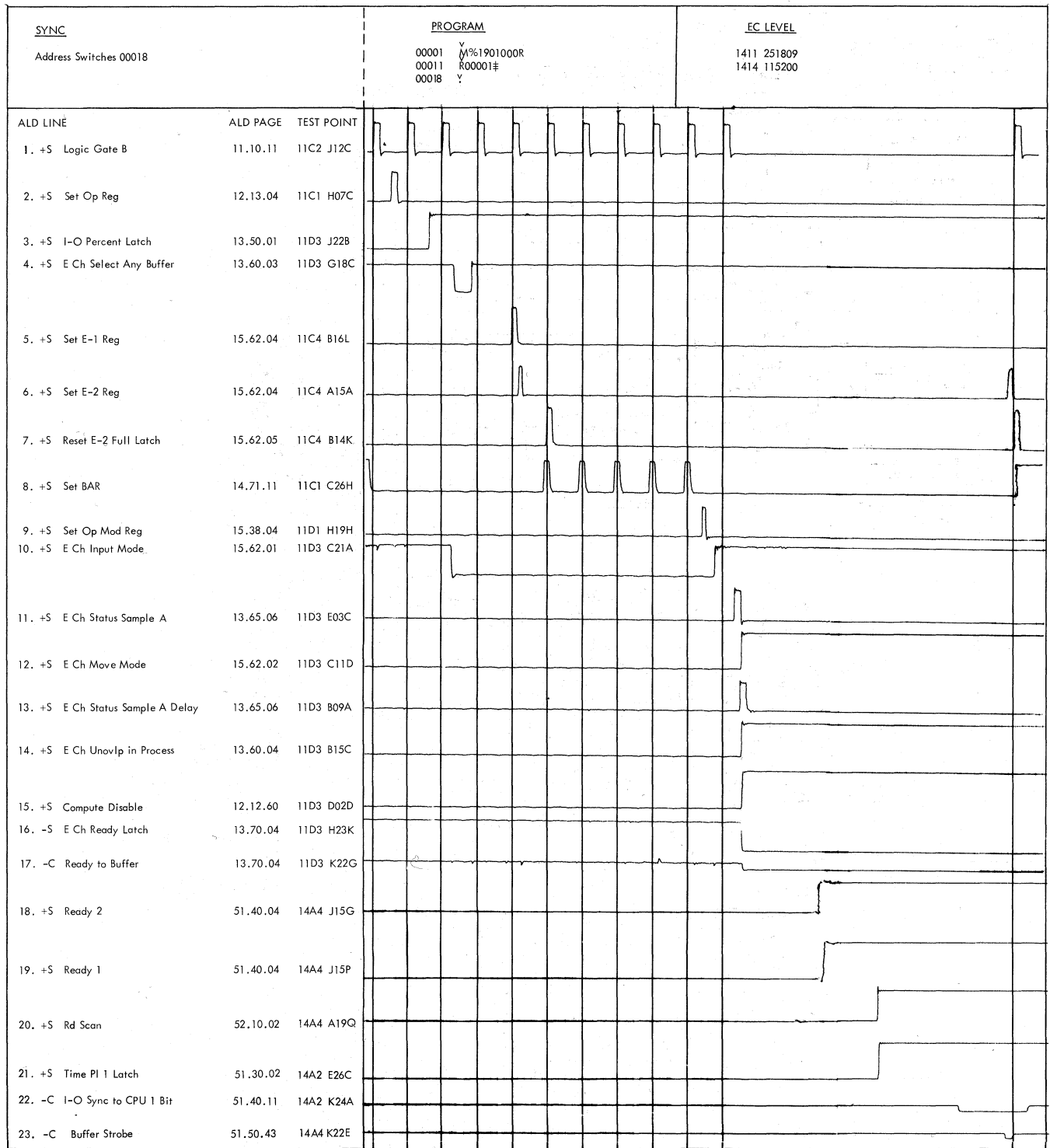


Figure 42. 1402 Read Command Timing Chart

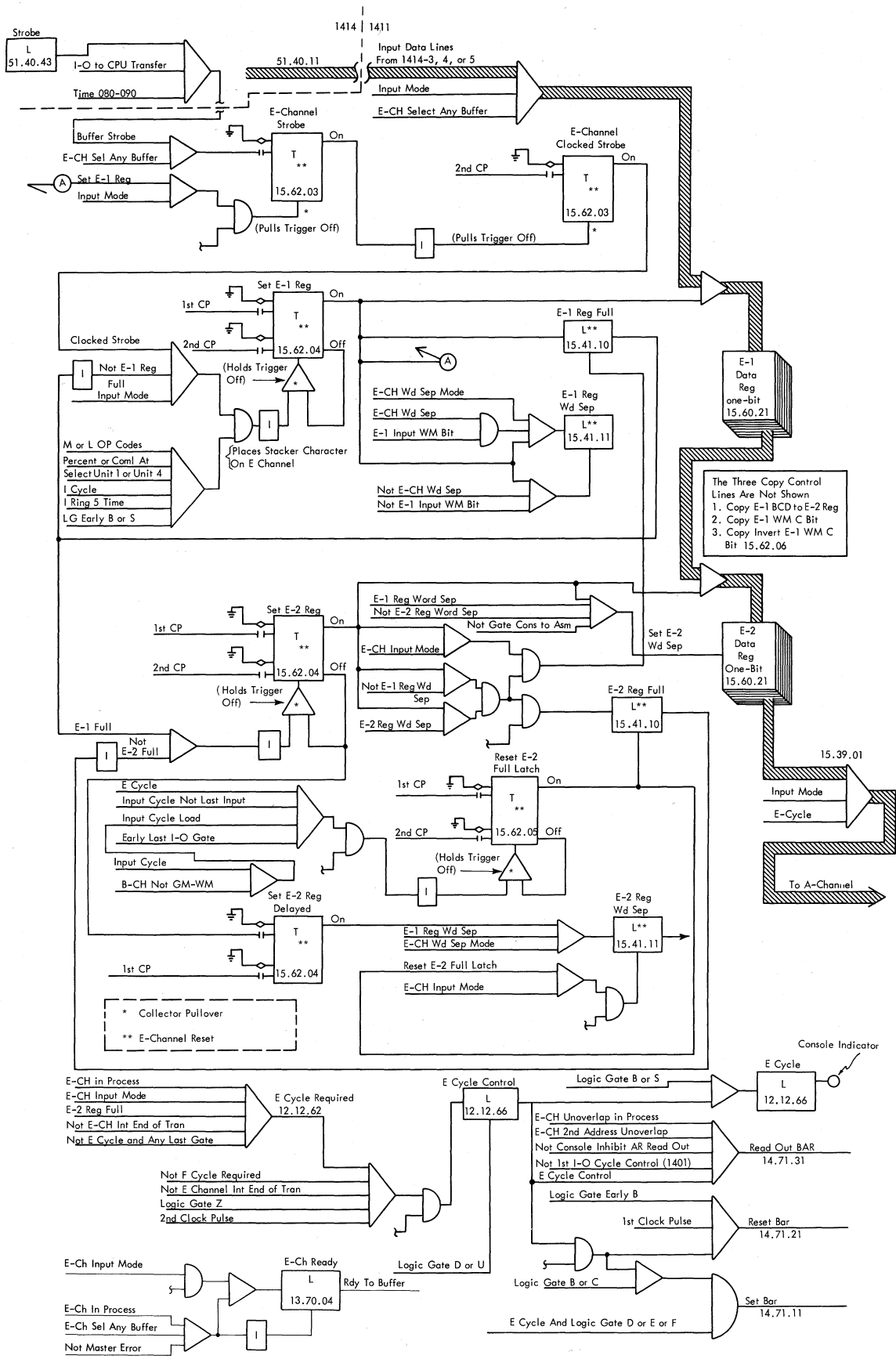


Figure 43. Channel Register Operation – Reader

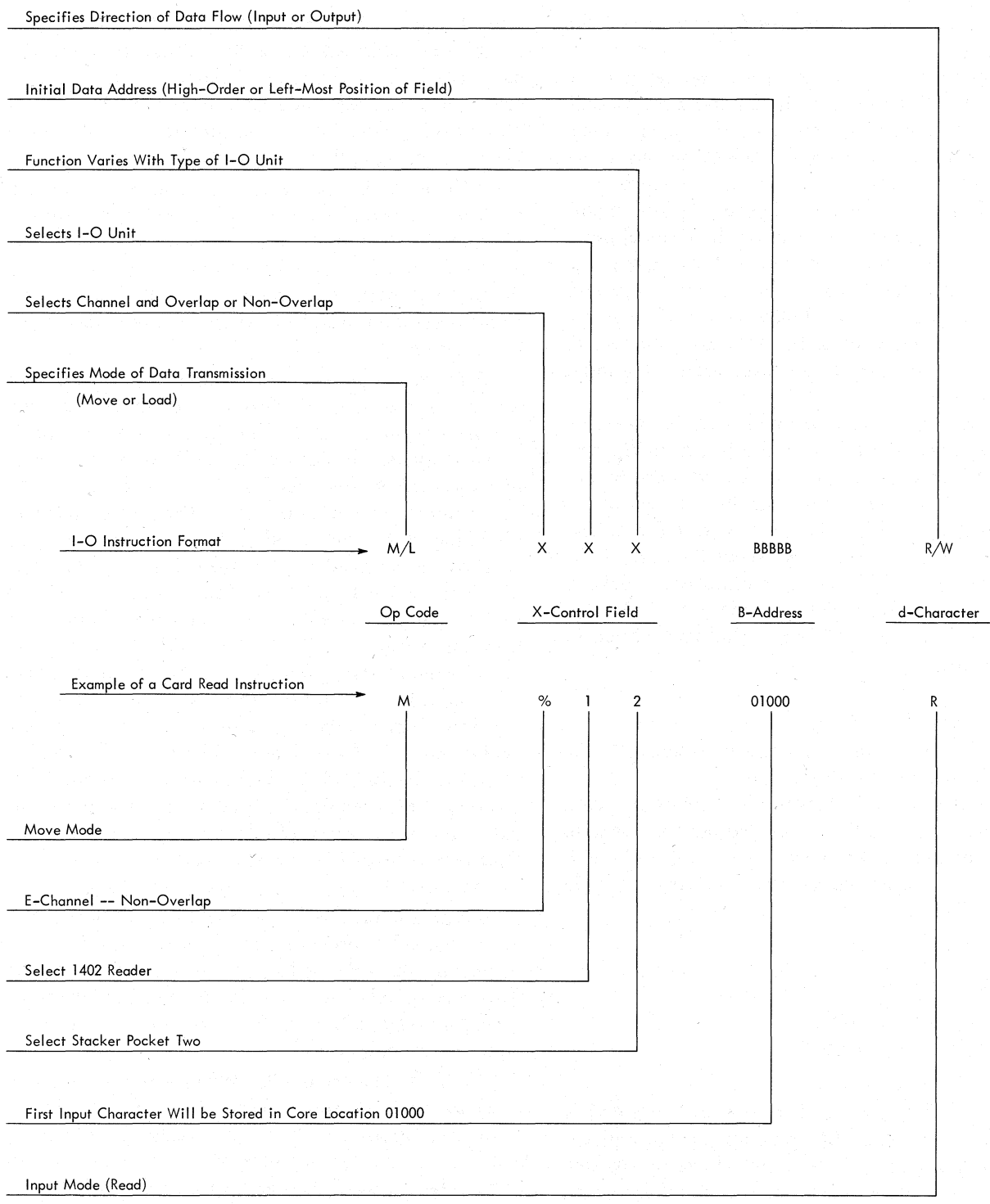


Figure 44. Reader Move or Load Command

fer signal from the reader causes the CPU to end the I-O operation.

If the op code character is an M, specifying move mode, the data in the reader buffer transfers as is to the CPU. That is, word separator characters are transferred, unchanged, just as any other character. Existing word marks in the input field are undisturbed. If the op code character is an L, specifying load mode, a single word separator character on the channel input lines is converted into a word mark and placed over the next input character. Two successive word separator characters from the reader buffer appear as a single word separator character in the 1411 core storage. In load mode operation, existing word marks in the input field are removed.

If the character in the units position of the X-control field is a 9, data transfer from the buffer to the CPU but no card feed cycle occurs and the old data remains in the buffer. The same data can be transferred repeatedly to the CPU but a channel no transfer indication will occur for all transfers except the first. If the character is other than a 9, the transfer of data is followed by a card feed cycle and the buffer is loaded with new data as the card passes the read station in the 1402 reader.

I-Phase Sequence

Details of I-O instruction read-out are presented in the I-O Sequence section. See Figure 34.

Instruction read-out causes the instruction word characters to be placed in the various registers to control the execution of the read command. An M or L in the op register brings up the following op code grouping lines:

- M or L op codes
- Percent type op codes
- Address type op codes
- Two address op codes
- 2 address plus mod op codes
- No index on 1st addr op codes
- No branch op codes
- Not address dbl op codes

I-Op Time: The op code character reads out and is set into the op register, bringing up the appropriate op code grouping lines. The output of the op register is used later in I-phase to gate the turn on of the channel move mode or load mode latch. The channel select registers (both E-channel and F-channel) are reset at logic gate E.

I-1 Time: The special advance control latch turns on to gate two extra advance pulses (logic gate C and logic gate D) that advance the I-ring to I-3.

I-3 Time: The channel select character is set into the I-O channel select register. With a channel selected, the I-O Interlock test is made to see if the stored program has interrogated the channel status indicators

since the last command to the selected channel. A satisfactory interrogation of the indicators resets the move (or load) mode latch. Therefore, if the channel move mode or load mode latch is still on, the system check I-O Interlock indicator is turned on, master error becomes active, and the CPU stops at I-3 time.

I-4 Time: A channel reset is generated to reset the control and status latches for the selected channel (Figure 17). The unit select character reads out and is gated into the channel unit select register. A 1 in the register gates the reader status to the channel status buses later in I-phase when the input mode latch is turned on.

I-5 Time: The unit-number character reads out and is sent to the channel registers and appears on the channel output data lines. The data lines are sampled, during E-phase, by the reader synchronizer to condition the card stacker selection and card feed circuits. The character remains in the channel data registers (E-1 and E-2 or F-1 and F-2) until the first data character is received on the channel input data lines. The E-2 (or F-2) Full latch, however, is reset at I-6 time to prevent the unit number character from being transferred from E-2 (or F-2) to 1411 core storage as the first input data character. (During input mode, "E-2 reg full" calls for an input load cycle E-cycle to transfer the character in E-2 into 1411 core storage.)

I-6 through I-10 Time: The B-address reads out and is placed in the B- and D-address registers. If the command specifies overlap, the B-address is also placed in the E-address register (E-channel operation) or the F-address register (F-channel operation).

I-10 Time: During an unoverlapped operation, the computer is interrupted (disabled) at I-10 time if the other channel is executing an I-O operation. In other words, an unoverlapped operation cannot be started if an overlapped operation is in process. The computer is kept disabled only until the channel in process completes its operation.

I-11 Time: The op-modifier character reads out and is set into the op-mod register. Because of the processing overlap feature, the op-mod register, op register, and the I-O channel select register must be free to accept characters of the next instruction word. Therefore, the information in these registers must be stored in the channel control latches.

During I-11 time, the R (or X) in the op-mod register gates the set of the channel input mode latch (E-channel) or the channel read latch (F-channel). The output of the latch lights the read indicator, for that channel, on the 1415 console.

The output of the input mode latch is also sent to the 1414 synchronizer as "input mode to buffer" where it AND's with "unit 1 select to I-O." The resulting signal,

“select unit 1,” gates the reader and buffer status to the channel status buses. (Figure 102).

Within CPU, “input mode” gates the E-2 register to the A-channel. It also AND’s with “E-cycle” or “F-cycle” to produce “input cycle” (ALD 13.60.06). “Input cycle” conditions the assembly controls and develops “load memory” (ALD 12.50.01). If the B-channel is not a GM-WM, “input cycle load” becomes active to gate the input character from E-2 into 1411 core storage (ALD 12.50.01).

I-12 Time: I-12 is last instruction read-out cycle during which the channel move or load latch is set, according to the character in the op register. The status sample pulses are generated during I-12 time.

Last Execute Cycle: During last instruction read out of an overlapped command, “last execute cycle *I-O” becomes active, gating the set of the I-Cycle Control latch (Figure 120).

Status Sample A: This pulse occurs at logic gate D of I-12 time and it is used to sample the A-status buses. Condensed logic (Figure 101) shows generation of the status sample pulses.

Status Sample A Delay: This pulse occurs at logic gate E of I-12 time and it is used to sample the output of the channel status indicators. If any status indicators are on at status sample A delay time, the operation is terminated (no E-phase) and the program proceeds to the next sequential instruction.

I-Phase Channel Status Indicators

Channel status indicators that can be set at the end of I-phase (status sample A time) are referred to in this manual as A-status indicators. For an M%10 or an M%19 op code, the A-status indicators for the reader are:

Not Ready	(Requires manual intervention)
Busy	Reader is reloading the buffer
Condition	Reader end of file

Only one of the above indicators can be set during a given command, in the priority shown. If no status indicators are set, “status sample A delay” turns on one of the four channel in process latches, according to the character in the I-O channel select register.

Percent sign	%	E-channel unoverlap in process
Commercial at	@	E-channel overlap in process
Asterisk	*	F-channel unoverlap in process
Lozenge	◻	F-channel overlap in process

Each latch has an indicator on the 1415 console. If the read command specifies overlap, the CPU proceeds with the next sequential instruction after setting a channel in process latch. If any status indicator was turned on, the CPU does not execute the read command and proceeds with the stored program.

If no “channel in process” latch is set to bring up “compute disable cycle” (ALD 12.12.60), the logic gate

ring will continue to run. With no cycle control latch on (ALD 12.12.46), an instruction check occurs.

Not Ready: Figure 103 shows the reader status gated to the CPU by “select unit 1.” In CPU, “buffer ready” is gated to the channel ready bus by “E-channel select any buffer.” With the ready bus active, the input to the channel not ready latch is blocked, preventing the status sample A pulse from turning on the latch.

Busy: Figure 103 shows the reader busy status gated to the CPU by “select unit 1.” If the reader is busy, the channel busy bus becomes active, ANDing with “E-channel ready bus” and “status sample A” to set the channel busy indicator.

Condition: When the end of file latch in the 1414 is on, the data from the last card has been transferred to CPU and the last card has been stacked. “Select unit 1” gates the output of the end of file latch to the CPU as “buffer condition,” making the channel condition bus active (Figure 89). At status sample A time, “E-channel condition bus” AND’s with “not file op” to set the channel condition latch. The CPU sends reset select buffer latches to the 1414 synchronizer to turn off the end of file latch (Figure 112).

E-Phase Sequence

During E-phase, the CPU transfers characters from E-2 (or F-2) to the 1411 core storage on request from the channel controls. Use Figures 40, 41, and 44 to follow the data transfer operation.

Channel In Process Latch: With no status indicators on at the end of I-phase, one of the four channel in process latches is turned on. The latch output AND’s with “input mode” to turn on the E-channel ready latch (assume an E-channel operation). Note that this latch has no connection with the channel ready bus that is sampled to set the not ready status latch. The output of the E-channel ready latch brings up the “ready to buffer” line to the synchronizer.

E-Channel Ready Latch: The output of the latch, “ready to buffer” turns on the ready 2 latch in the 1414 synchronizer. If no scan is in progress, the ready 1 latch is turned on and the output AND’s with “reader ready,” “reader not busy,” and “select unit 1” to turn on the read transfer request latch. (See the appropriate condensed logic diagram in the *IBM 1414 Input-Output Synchronizer*, Customer Engineering Instruction-Reference Manual, Form 223-2590.)

Read Feed Latch: When the synchronizer buffer priority circuits honor the read transfer request, “read transfer scan” becomes active, AND’s with the unit number character not a 9 and other conditions to bring up “set read feed latch.” The output of the read feed latch provides a gate for the read feed trigger to be turned on with a 1402 reader CB impulse (–W Proc Feed). The output of the trigger energizes the reader

card feed clutch magnet to initiate a feed cycle. Note that the card feed cycle is initiated before the data transfer from buffer to CPU. Due to the delay in the card feed clutch and magnet operation, the data transfer is completed long before the card transport mechanism is set in motion.

Stacker Select Latches: The line "set read feed latch" described earlier, is used to set the stacker select latches. The I-O channel output data lines are sampled and the appropriate latches are set.

Read Priority Request Trigger: "Read transfer request," developed earlier, provides a gate for the turn-on of the read priority request trigger. The output of this trigger AND's with not "some scan" to gate the turn-on of the read scan trigger, which starts the buffer operation.

Channel Operation: During each buffer cycle, a character is read out of the buffer and placed on the channel input data lines. A strobe signal generated by the synchronizer causes the channel controls to sample the input data lines and set the data into E-1. The character transfers from the E-1 register to the E-2 register under supervision of the register transfer and data flow controls.

Unoverlapped Operation: The CPU is idle (logic clock ring is disabled) except when the channel controls request CPU to take an I-O data cycle (E-cycle) to transfer an input character from the channel register to 1411 core storage.

Overlapped Operation: At the end of I-phase of the read command, the CPU proceeds with the next sequential instruction. Processing (computing) continues until the channel controls request the CPU to take an I-O data cycle to transfer a character from the channel register to 1411 core storage. Computing is interrupted (disabled) while the CPU stores the input character. Computing is then resumed (Figure 113).

External End of Transfer Trigger: Once the buffer operation is initiated the operation continues until all 80 characters have been transferred to the input data lines. The synchronizer signals CPU that the transfer is complete by generating "buffer end of transfer" which turns on the external end of transfer trigger in the CPU (Figure 100). If the ready bus becomes inactive during a buffer transfer operation, the external end of transfer trigger is turned on immediately. See Figure 36.

Internal End of Transfer Latch: A GM-WM in the input field, or a core storage wrap-around condition, turns on the internal end of transfer latch, blocking the CPU from taking any more I-O data cycles. With the GM-WM correctly positioned in the input field, the external end of transfer trigger is turned on before the internal end of transfer latch.

Last Input Cycle Latch: If the internal end of transfer latch is off during the I-O data cycle that stores the last input character, "E-cycle required" becomes active. This forces an extra E-cycle to check for a GM-WM in the input field. During this extra E-cycle, the last input cycle latch is turned on, forcing on the internal end of transfer latch. If a GM-WM appears on the B-channel, the end of record latch is turned on. The wrong length record status indicator is subsequently turned on if the end of record latch is not turned on (Figure 100). See the I-O Sequence section of this manual.

Status Sample B Trigger: With both the external end of transfer trigger and the internal end of transfer latch on, the status sample B trigger is turned on at the end of the last I-O data cycle (E-cycle). The trigger is on for two clock pulses and the output of the trigger is used to set the B-status channel indicators (Figure 101).

Second Sample B Trigger: This trigger is turned on the next 1st clock pulse after the status sample B trigger is turned on. The trigger is on for two clock pulses and the output of the trigger is used to sample the outputs of the B-status indicators.

Status Sample B Delay Trigger: This trigger is turned on the next 1st clock pulse after the second sample B trigger is turned on. The trigger is on for two clock pulses and the output of the trigger is used to reset the channel in process latch.

E-Phase Channel Status Indicators

Channel status indicators that can be set at the end of E-phase (status sample B time) are referred to in this manual as B-status indicators. For an M%10 or an M%19 op code, the B-status indicators for the reader are:

Data Check	Figure 104 (condensed logic)
No Transfer	Figure 45 (simplified logic)
	Figure 46 (condensed logic)
Wrong Length Record	Figure 105 (condensed logic)
See the status indicator chart, Figure 86.	

Data Check: This indicator can be set in two ways during input operation:

1. If a parity error character is detected on the A-channel during an I-O data cycle (E-cycle), the data check indicator is turned on immediately.
2. If the read check latch is on in the 1414 synchronizer, the output of the latch is gated to the channel check bus and status sample B turns on the data check indicator.

No Transfer: Primary use of this indicator during reader operation is to detect unusual programming sequences, although a machine malfunction may also cause a no transfer indication. A programming se-

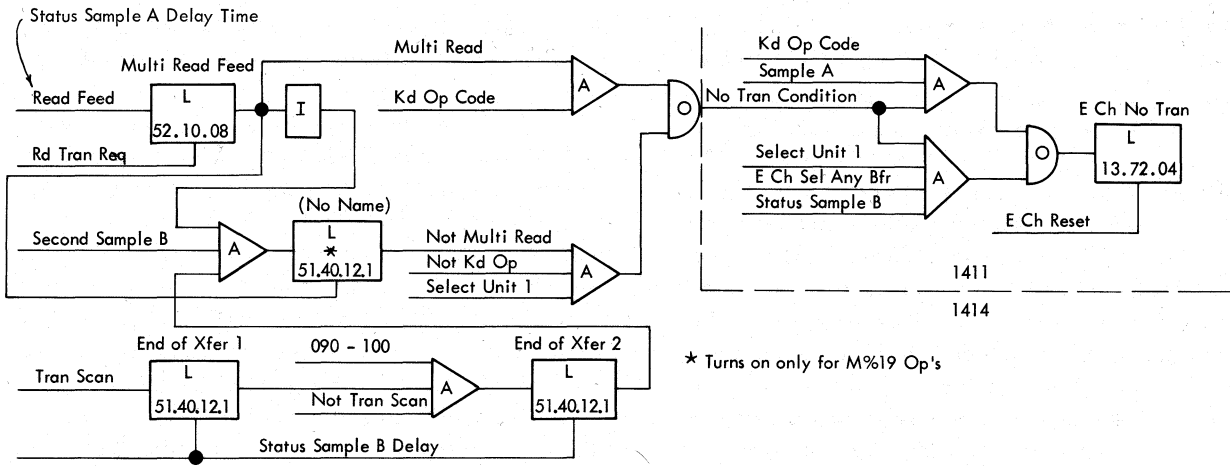


Figure 45. Reader No Transfer – Simplified Logic

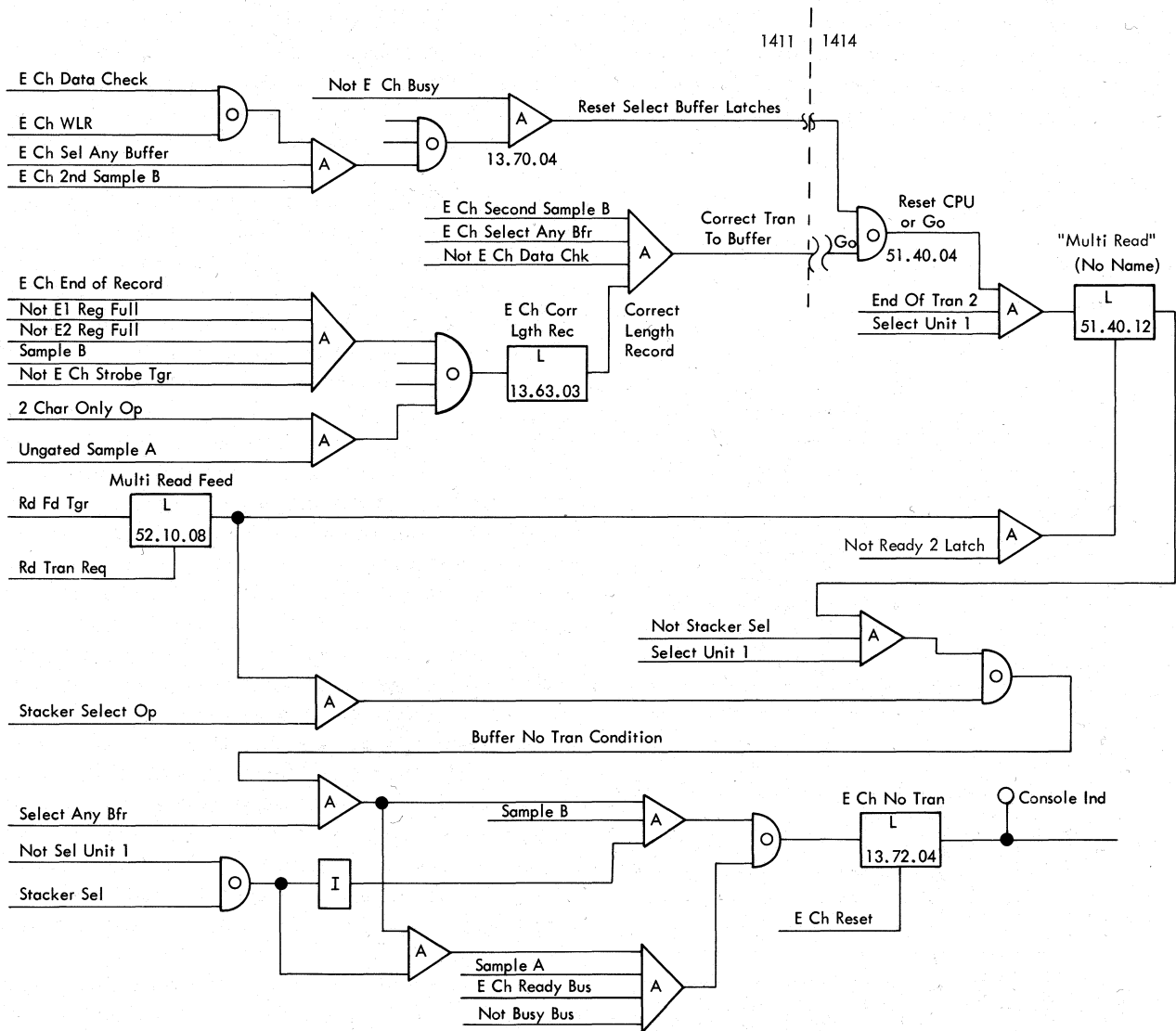


Figure 46. Reader No Transfer – Condensed Logic

quence for the reader that produces a no transfer indication must have one of these two reader op codes:

M%19 Buffer to CPU data transfer (no card feed cycle)
 Kd Select a stacker pocket, feed a card, and load the buffer (no buffer to CPU data transfer)

The principle of the no transfer indicator for reader operation is simply this: Commands to the reader must result in alternate buffer to CPU data transfers and reader card-feed cycles. Any combination of op codes that command two buffer to CPU data transfers without a reader card feed cycle between the data transfers will result in a no transfer indication. If the reader is commanded to take two successive feed cycles without an intervening buffer to CPU data transfer, a no transfer indication occurs. Programming sequence 1, Figure 47, employs all three reader commands without producing a no transfer indication. Programming sequences 2 through 5 show the four combinations of reader op codes that produce a no transfer indication. Note that multiple Kd op codes are not executed because the no transfer is recognized during I-phase (status sample

A time). Multiple buffer to CPU data transfer, however, are executed regardless of the no transfer indicator.

Figure 45 shows the simplified logic of the no transfer indicator. Functional line names, rather than actual line names, are used to simplify presentation. Actual line names are used in Figure 46. Programming sequence 2 in Figure 47 shows two successive Kd commands. After the first Kd command, the multi-read feed latch is on (Figure 45) (the latch stays on until a buffer to CPU transfer brings up "read transfer request"). When the next Kd command is given, the output of the multi-read feed latch is gated to the CPU as "buffer no transfer condition." At status sample A time, the channel no transfer indicator is set. There is no E-phase (data transfer) for a Kd op code and hence no status sample B time. Any status indicators for Kd commands are set at status sample A time. If the no transfer, busy, or not ready indicator is on, blocking the input to the forms-stacker go single-shot (ALD 13.70.04), the command is not executed.

Refer to Reader Stacker Select and Feed Command section.

Programming sequence 4 in Figure 41 shows two successive M%19 op codes. When the first M%19 command is given, a buffer to CPU data transfer occurs and "read transfer request" turns the multi-read feed latch off. The inverted on output of the latch (Figure 45) AND's with "second sample B" and "end of transfer 2" to turn on the multi-read (no name) latch. Although the output of the latch is gated to the no transfer status bus, the no transfer indicator cannot be turned on because "status sample B" is no longer active. However, at status sample B time of the next M%19 command, the channel no transfer indicator is turned on. Figure 46 shows that the CPU generates "correct transfer to buffer" (go) only if no channel data check occurred. Because of punch and printer operation, a channel data check or a channel wrong length blocks "correct transfer to buffer" to prevent punching (or printing) the record transferred to the buffer. To permit recognition of a reader no transfer status during multiple buffer to CPU transfers of data check or wrong length records, the "reset select buffer latches" line (ALD 13.70.04) is sent to the 1414 synchronizer instead of "correct transfer to buffer." Either line develops "reset CPU or go" to gate the set of the multi-read (no-name) latch (ALD 51.40.12) during multiple transfers (Figure 46).

Wrong Length Record: A GM-WM must appear in the 81st position of the input field or a channel wrong length (WLR) record indication occurs (Figure 100). A WLR indication has no effect on reader operation except through programming. See "Channel Status Indicators" in the I-O Principles of Operation section.

	Op Code	Set No Transfer?	At Status Sample A or B? Executed?	Buffer-to-CPU Transfer?	Card-Feed Cycle?
Sequence 1 *	M%10	No		Yes	Yes
	M%10	No		Yes	Yes
	M%19	No		Yes	Yes
	Kd	No		Yes	No
	M%19	No		Yes	Yes
	Kd	No		Yes	No
	M%19	No		Yes	Yes
	Kd	No		Yes	No
	M%10	No		Yes	Yes
Sequence 2 *	M%19	No		Yes	Yes
	Kd	No		Yes	No
	Kd	Yes	A	No	No
Sequence 3 *	M%10	No		Yes	Yes
	Kd	Yes	A	No	No
Sequence 4 *	M%19	No		Yes	Yes
	M%19	Yes	B	Yes	Yes
Sequence 5 *	M%19	No		Yes	Yes
	M%10	Yes	B	Yes	Yes

* (Assume that an R (I) GM instruction clears the interlock between read commands)

Figure 47. Reader Programming — Channel No Transfer Indicator

Last Execute Cycle: "E-channel status sample B" AND's with "E-channel unoverlap in process" to bring up "I-o last execute cycle" and turn on the I-cycle control latch (Figure 120). Status sample B delay resets the E-channel unoverlap in process latch, or the E-channel overlap in process latch.

Reader Select Stacker and Feed Command

INSTRUCTION FORMAT	MNEMONIC
Kd (E-Channel)	SSF
4d (F-Channel)	SSF

This op code causes the card reader to take a card feed cycle, read and check cards passing the read station and the read check station, and select a stacker. The card that is stacked on this card feed cycle is the card loaded into the buffer on the previous card feed cycle.

Assume the operator has made the reader ready by loading cards into the hopper and depressing the start key. At the end of the run-in operation (three card feed cycles), card A (Figure 48) has passed the read station and is now at the stacker select station. Card B has passed the read check station and is now between the read station and the read check station. Card C is just entering the card transport area. Assume the CPU stored program issues an M%19 command followed by a stacker select and feed command; for example:

K2 Select reader stacker 2 and feed a card.

During the resulting card feed cycle, card A is selected into the 2 stacker and card B moves past the read station where the information in the card is read and sent to the read buffer. Card C moves past the read check station and another card enters the card transport area from the hopper.

A 0, 1, or 2, as the d-character selects the normal read (NR), 1, or 2 stacker, respectively. See Figures 49, 50, and 51.

I-Phase Sequence

A K in the op register brings up the following op code grouping lines to control the operation:

- Not Addr Dbl Op Codes
- 2 Char Only Op Codes
- No Branch Op Codes
- Op Mod to A-Ch on B Cy Ops
- Regen Mem on B-Cy Op Codes

I-Op Time: The op code character (K) reads out and is set into the op register, bringing up the op code grouping lines and the "stacker select op code" line. The channel interlock is tested to see if the stored program has satisfactorily interrogated the channel status indicators since the last command to the channel. If the interlock is on, "master error" stops the CPU with the I-o interlock indicator glowing (red) on the 1415 console. "Stacker select op code" sets the E-channel input mode latch, which is used to gate the reader status to the CPU.

I-1 Time: An E-channel reset is generated (Figure 17) and a 1 is set into the unit select register (Figure 51). The output of the unit select register switches with the output of the E-channel input mode latch to generate "select unit 1" in the 1414 synchronizer. "Select unit 1" gates the reader status to the channel status buses. The d-character is set into the op-modifier register and gated to the input of E-1. At the end of I-1 time, "logic gate early B or S" sets the stacker select character into E-1. Normal register operation transfers the character to E-2, and it appears on the channel output data lines.

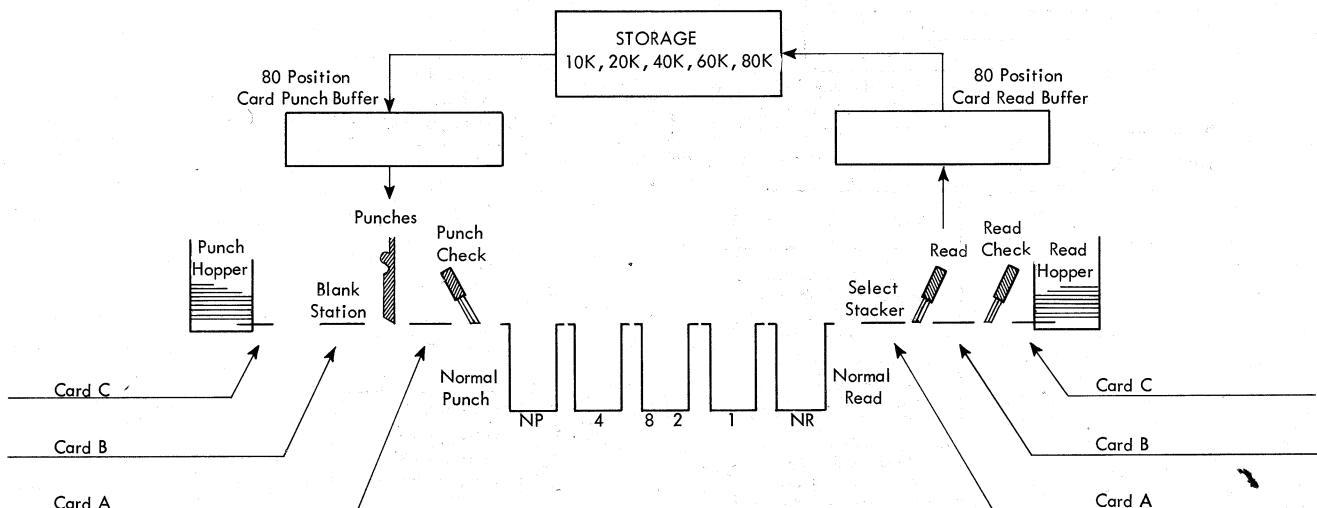


Figure 48. 1402 Card Transport

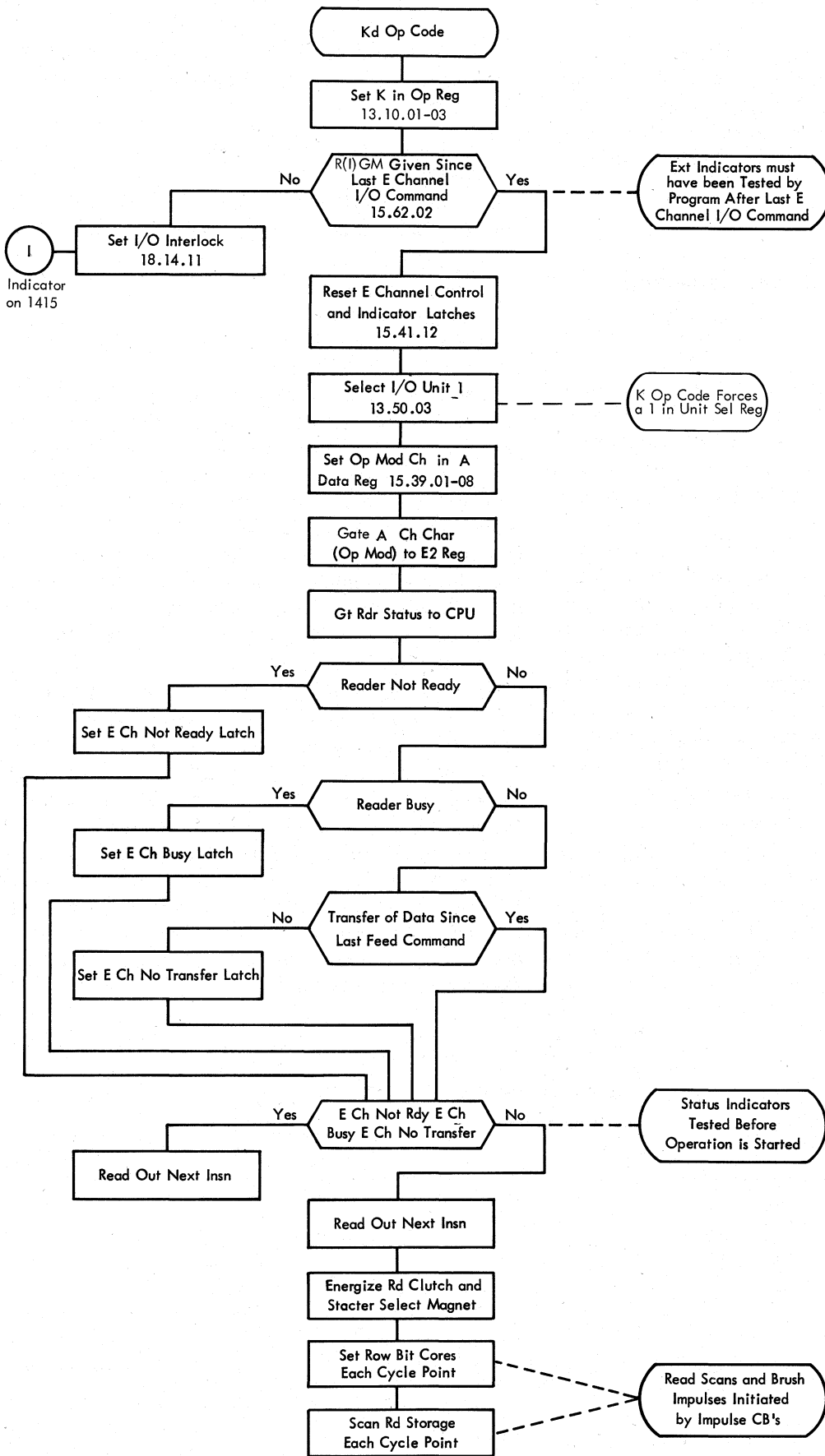


Figure 49. 1411-1402 Reader Feed Command Logic Flow

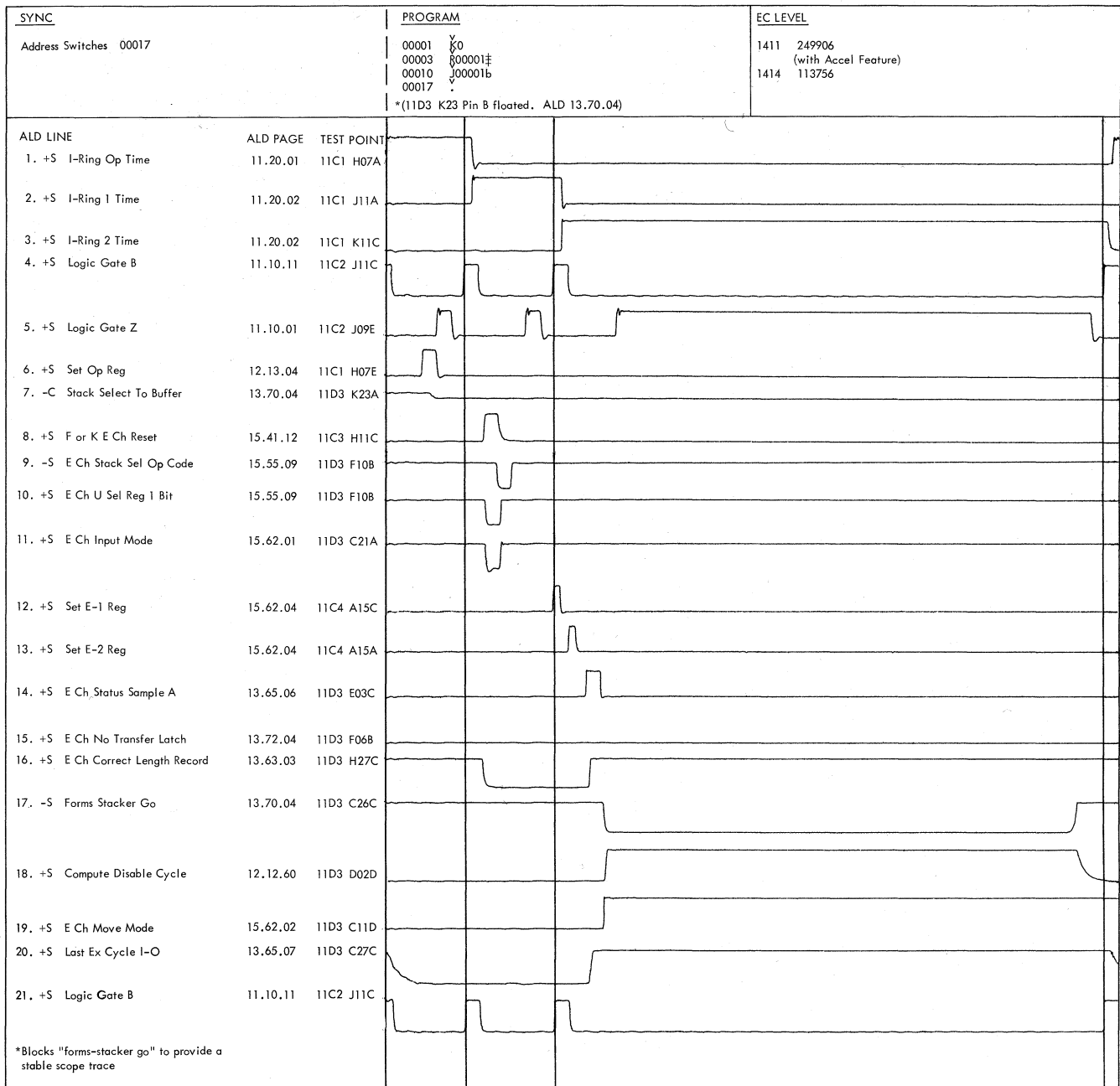


Figure 50. 1402 Feed Command Timing Chart

I-2 Time: The A-status buses are sampled at status sample A time and if no channel status indicators have been set, the command is executed by triggering the forms stacker go singleshot (Figure 51). The output of the singleshot initiates action in the 1414 synchronizer and also generates "compute disable" to interlock the CPU for twenty microseconds, preventing the conditioning lines from falling. Because a Kd

command is terminated at the end of I-phase regardless of whether or not the command is executed, "last execute cycle * i-o" is always generated during the last instruction read-out cycle. The channel move mode latch is turned on to develop the channel interlock which forces the program to interrogate the channel status indicators between channel commands.

I-Phase Channel Status Indicators

Because no E-phase occurs for Kd commands, no status sample B time occurs and hence no E-phase, or B-status, channel indicators are used. The I-phase, or A-status, indicators for a Kd command are:

Not Ready	Requires manual intervention
Busy	Reader is reloading the buffer
No Transfer	Usually caused by improper programming. See Figure 45 for information on the channel no transfer indicator.

See Figures 86, 102, and 103 in the reference section.

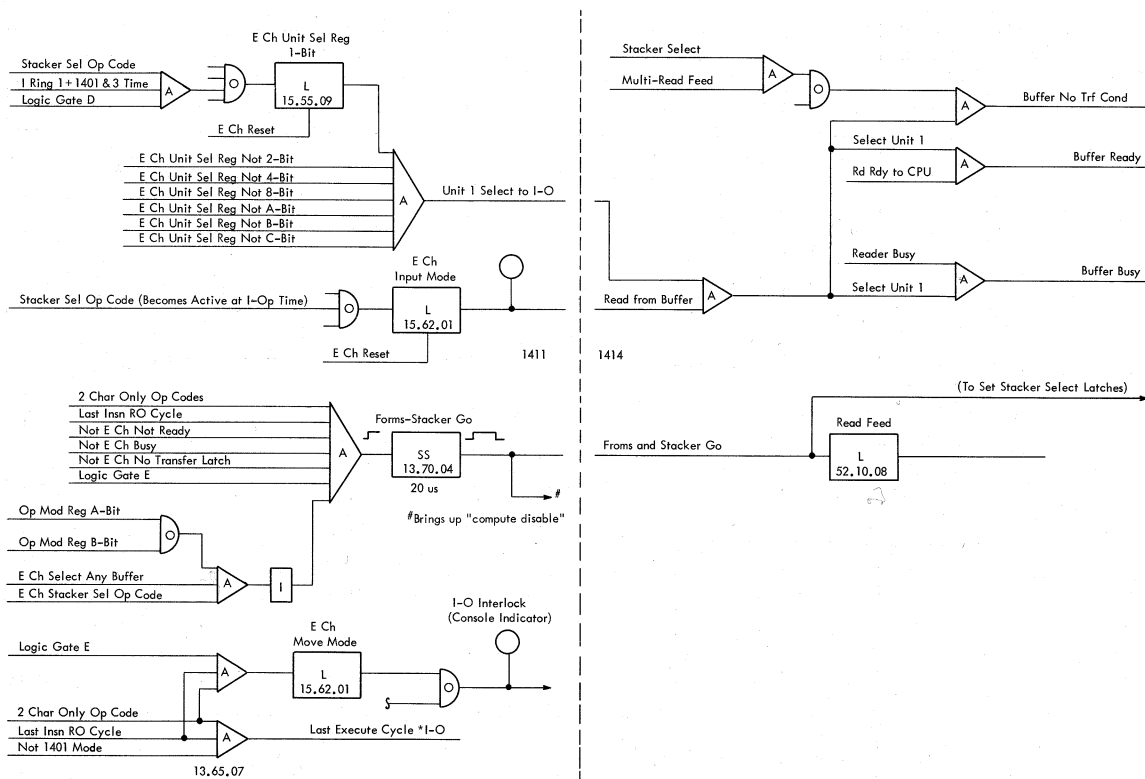


Figure 51. 1411-1402 Reader Feed Command – Condensed Logic

For ease in understanding the operations in this section, you should be familiar with three other sections of this manual: Input-Output Principles of Operation; Channel Data Register Controls; and I-O Sequence.

Information on the operation of the IBM 1402 Card Read Punch and the IBM 1414 I-O Synchronizer is contained in the *IBM 1402 Card Read Punch, Customer Engineering Instruction-Reference Manual, Form 231-0002*, and *IBM 1414 Input-Output Synchronizer 3, 4, 5, and 6, Customer Engineering Instruction-Reference Manual, Form 223-2590*.

One command is used with the 1402 punch.

Punch a card. Mnemonic: P (move mode) PW (load mode)
Example: M %48 02000 W

Transfer data from CPU to buffer, punch record (if correct), and stack card in the eight (8/2) pocket.

Punch Move or Load Command

For instructional purposes, diagrams are referred to at the appropriate point in the text. For reference purposes (trouble-shooting), Figures 34, 52, 53, 54, 55, and 56 are useful.

Instruction format: O XXX BBBB d
Example: M%48 00000 W

The hundreds position of the X-control field must contain one of these four characters or an instruction check occurs at the end of I-phase:

Percent sign	%	E-channel unoverlap
Commercial at	@	E-channel overlap
Asterisk	*	F-channel unoverlap
Lozenge	□	F-channel overlap

The units position of the X-control field usually contains one of the following characters:

0	Stack card in the normal punch (NP) pocket.
4	Stack card in the 4 pocket.
8	Stack card in the 8 pocket.

Cards are not actually stacked until a card feed cycle occurs from the next punch command. The d-character must be one of two characters or a channel not ready indication occurs:

W: Transfer output characters from core storage to channel until a CM-WM or end of storage is sensed.

X: Transfer output characters (up to 80) until the end of storage is sensed.

The X is useful in punching out fields that contain CM-WM characters.

Figure 53 shows basic logic flow for a punch move or load op code. Note that the punch command is

Note: See ALD 51.43.20 for a "feed-through" list

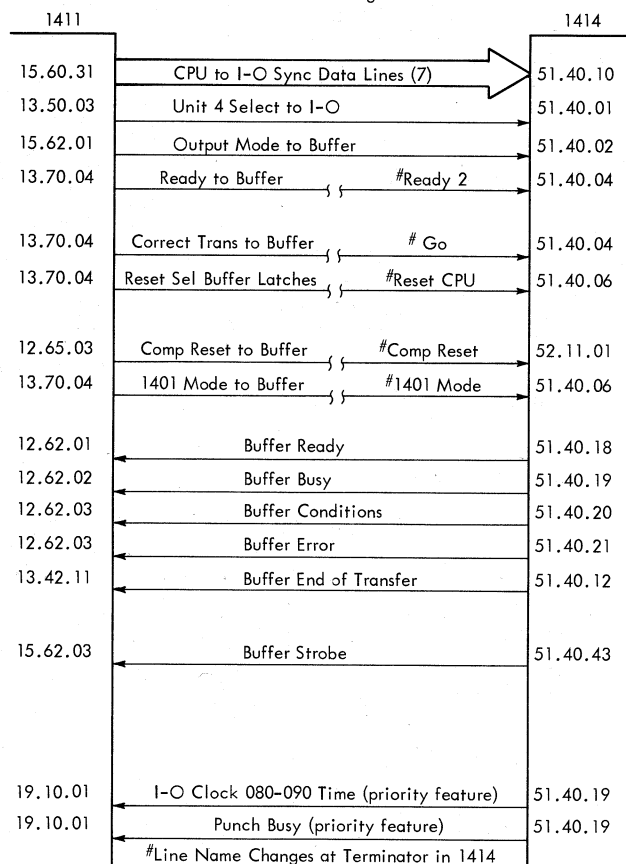
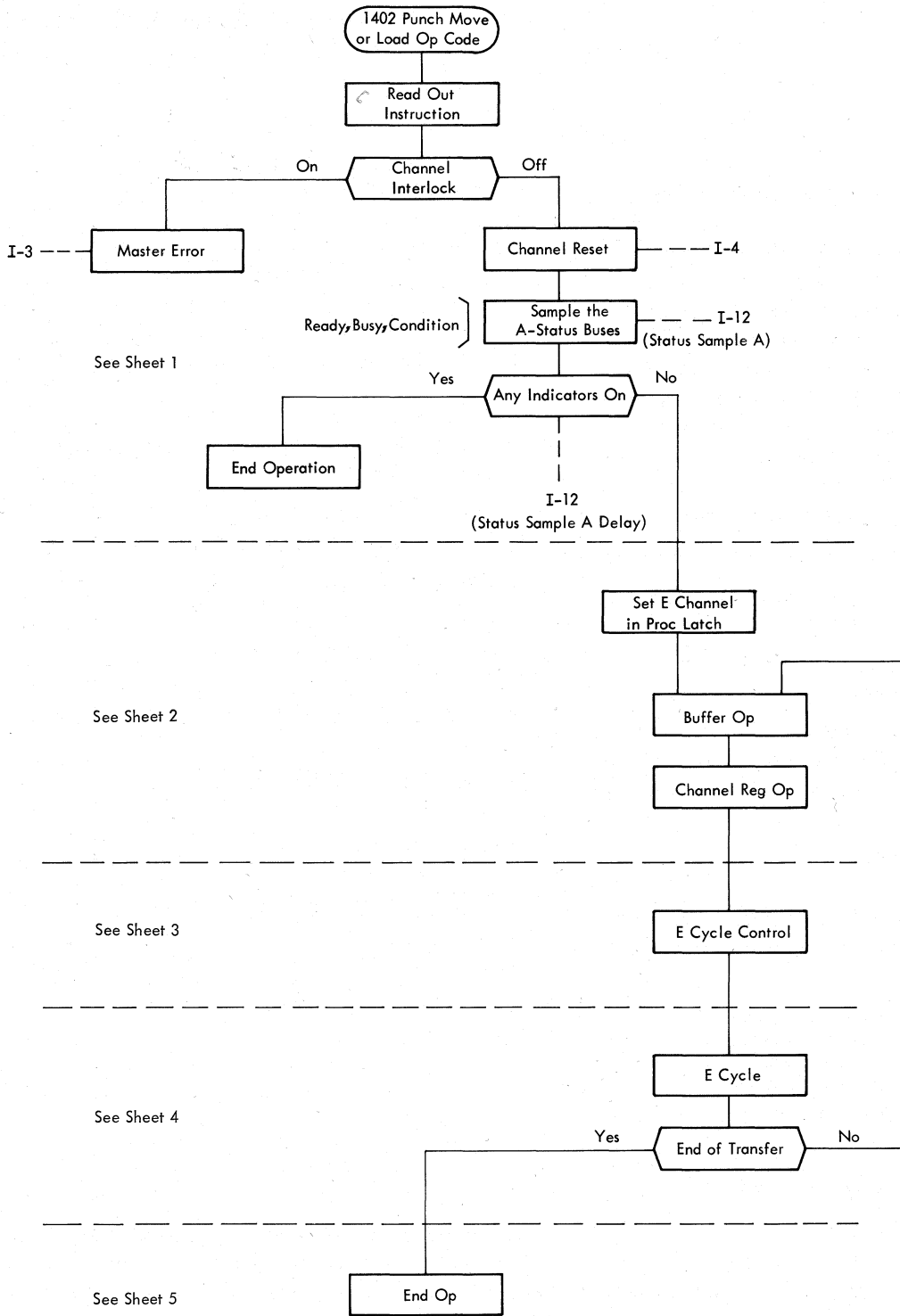


Figure 52. Channel Lines - Punch

not executed if any channel status indicators are on at the end of I-phase (status sample A time). If no channel status indicators are on at the end of I-phase, the punch command is executed and the data in the output field in 1411 core storage are transferred to the punch storage (buffer) in the 1414 synchronizer.

If the op code is an M, specifying move mode, the data in the output field (except word marks) are transferred as is to the punch buffer. That is, word separator characters are transferred, unchanged, just as any other character. If the op code is an L, specifying load mode, a word mark over a character in the output field is converted to a word separator char-



See the indicated Figures for a more detailed flow chart

Figure 53. 1411-1402 Punch Operation – Basic Logic Flow

See Figure 34 for detailed flow chart of M/L Instruction Read-Out

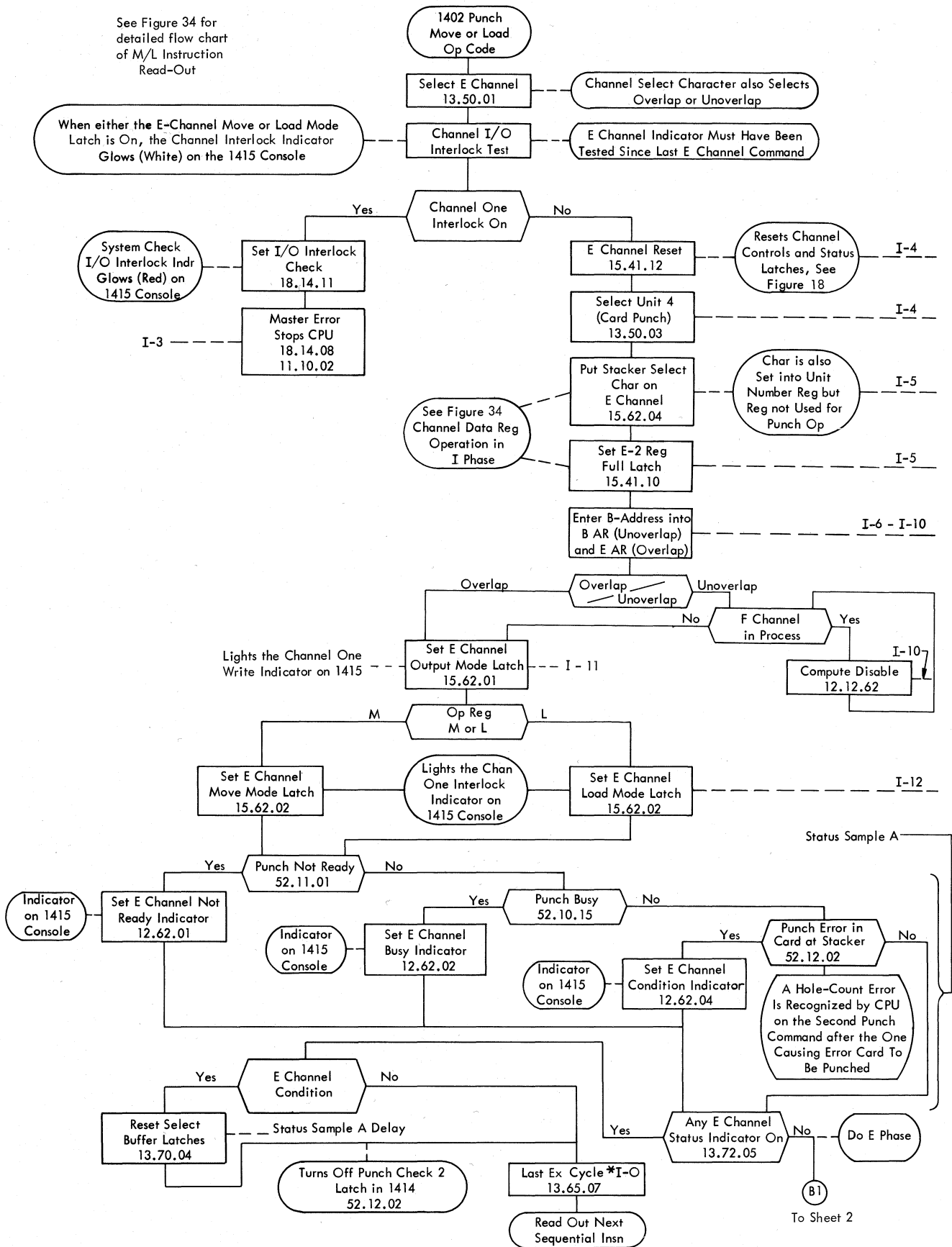


Figure 54. 1411-1402 Punch Operation – Logic Flow (Sheet 1 of 5)

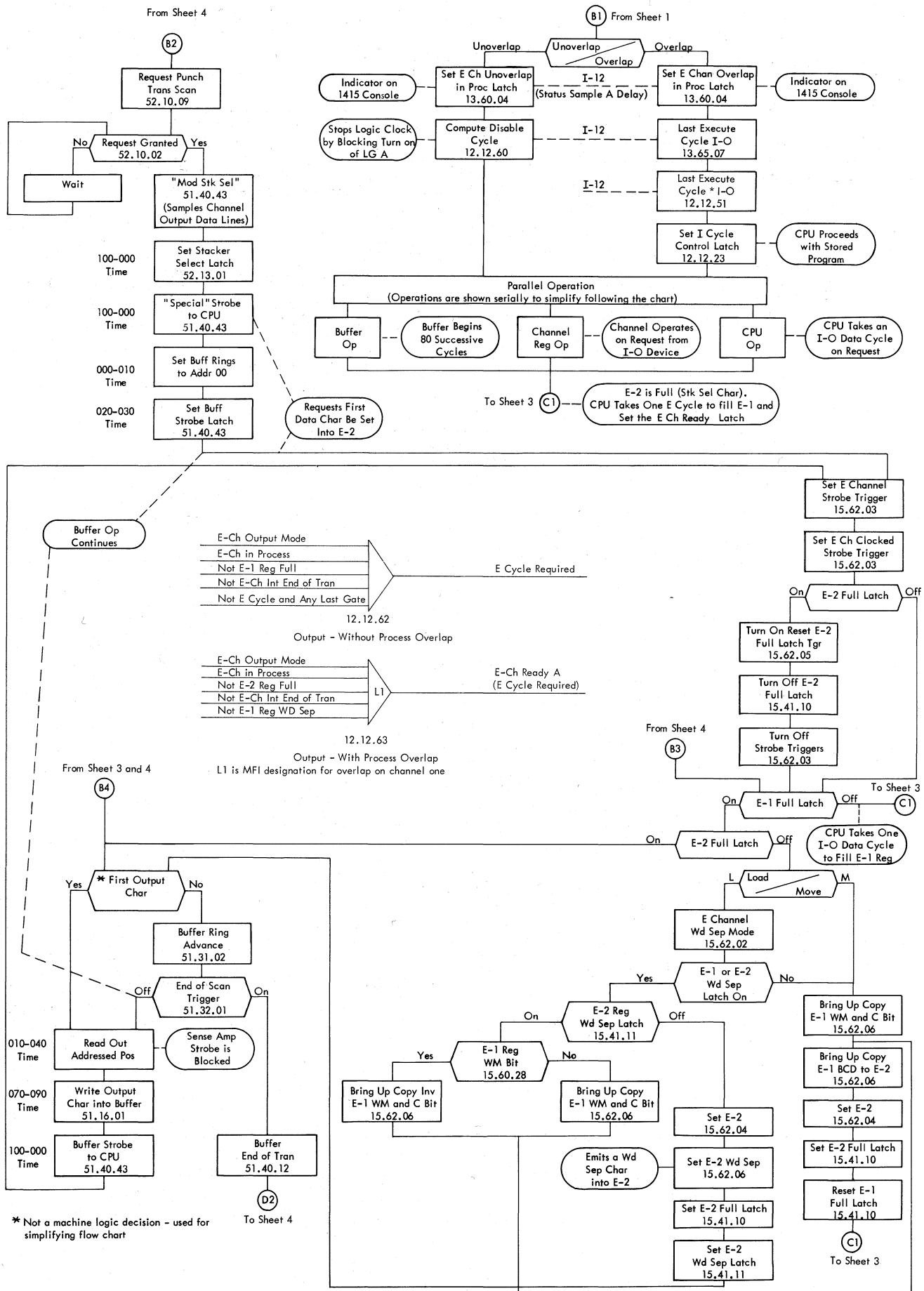


Figure 54. 1411-1402 Punch Operation – Logic Flow (Sheet 2 of 5)

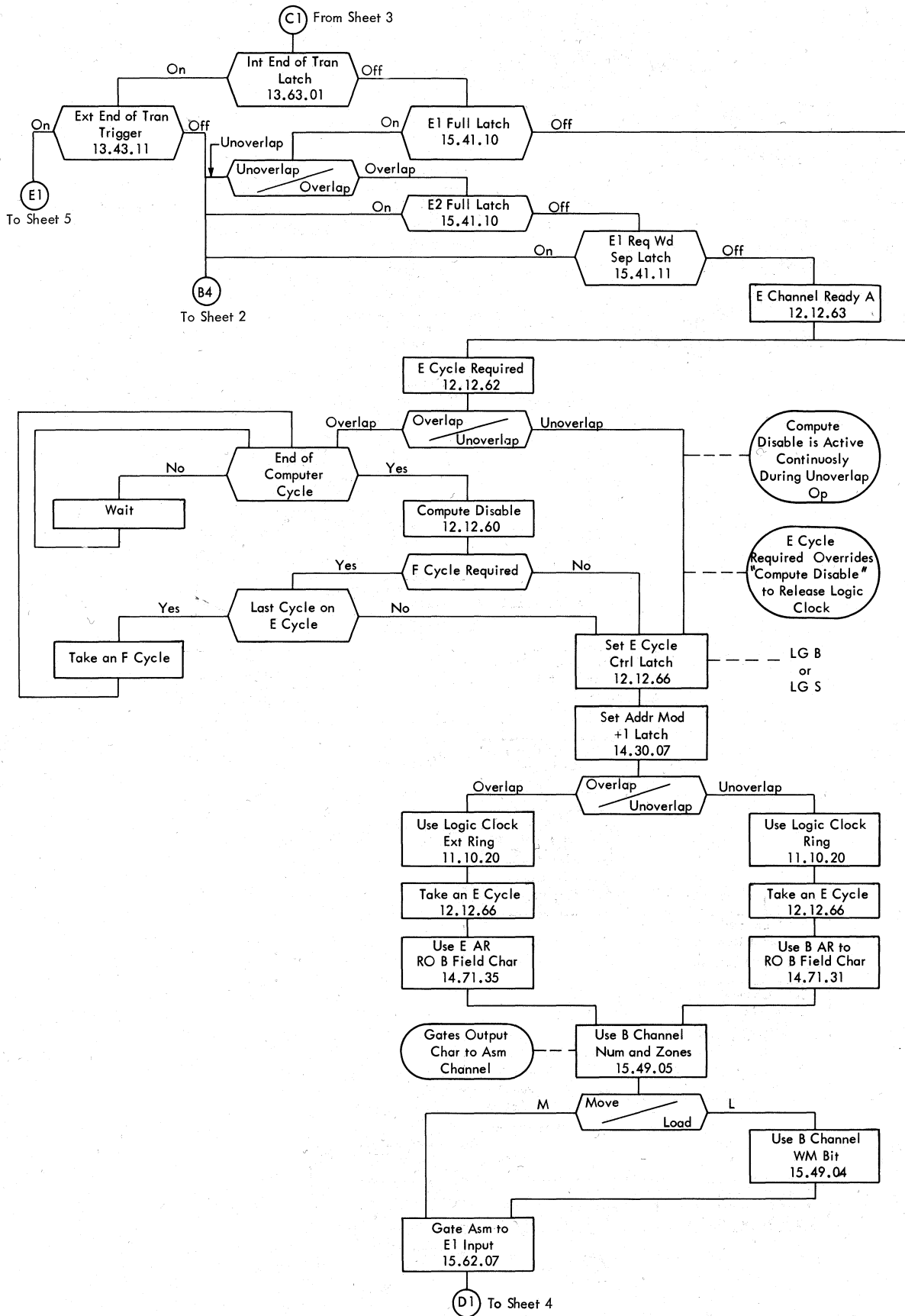


Figure 54. 1411-1402 Punch Operation — Logic Flow (Sheet 3 of 5)

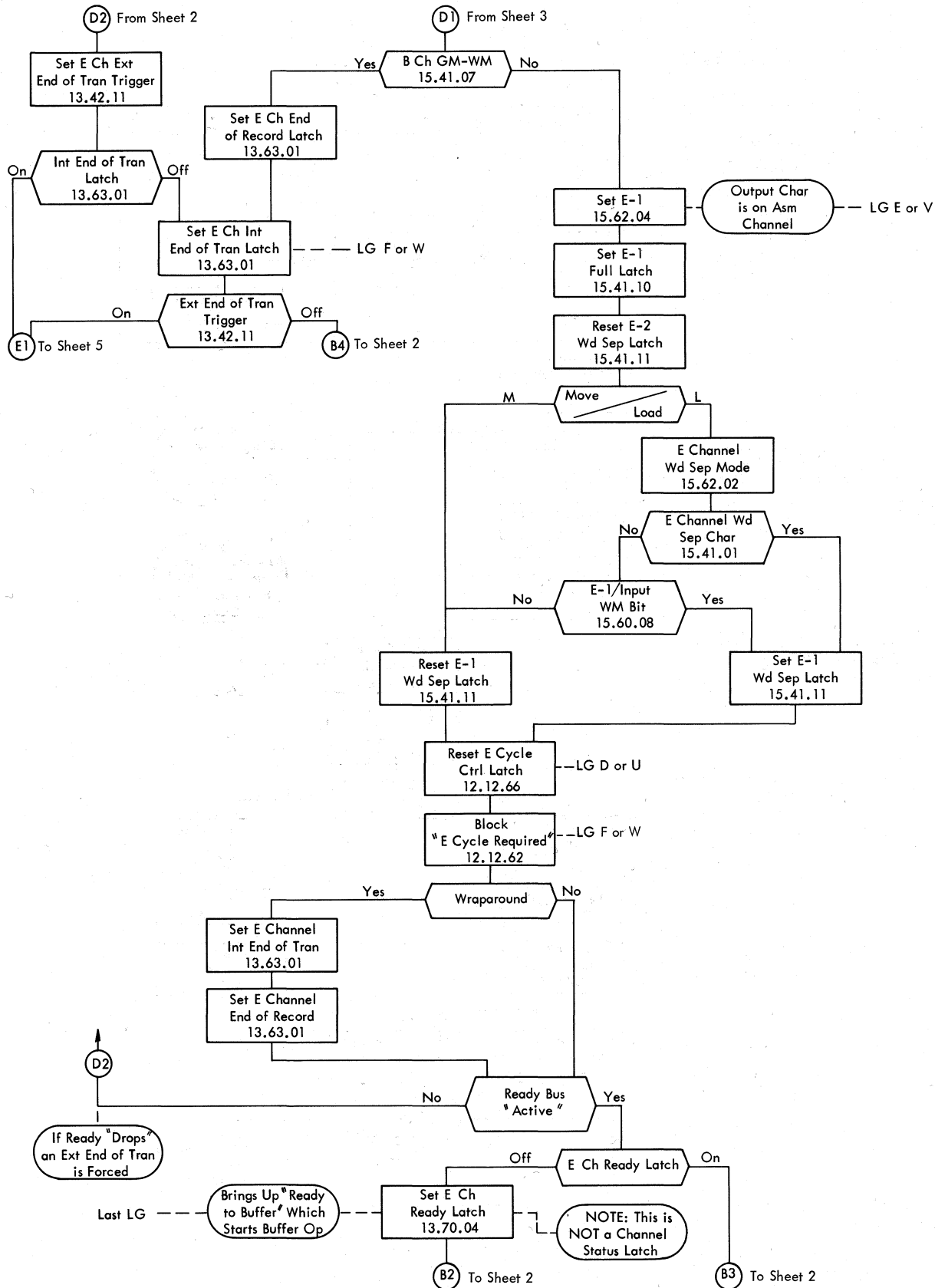


Figure 54. 1411-1402 Punch Operation — Logic Flow (Sheet 4 of 5)

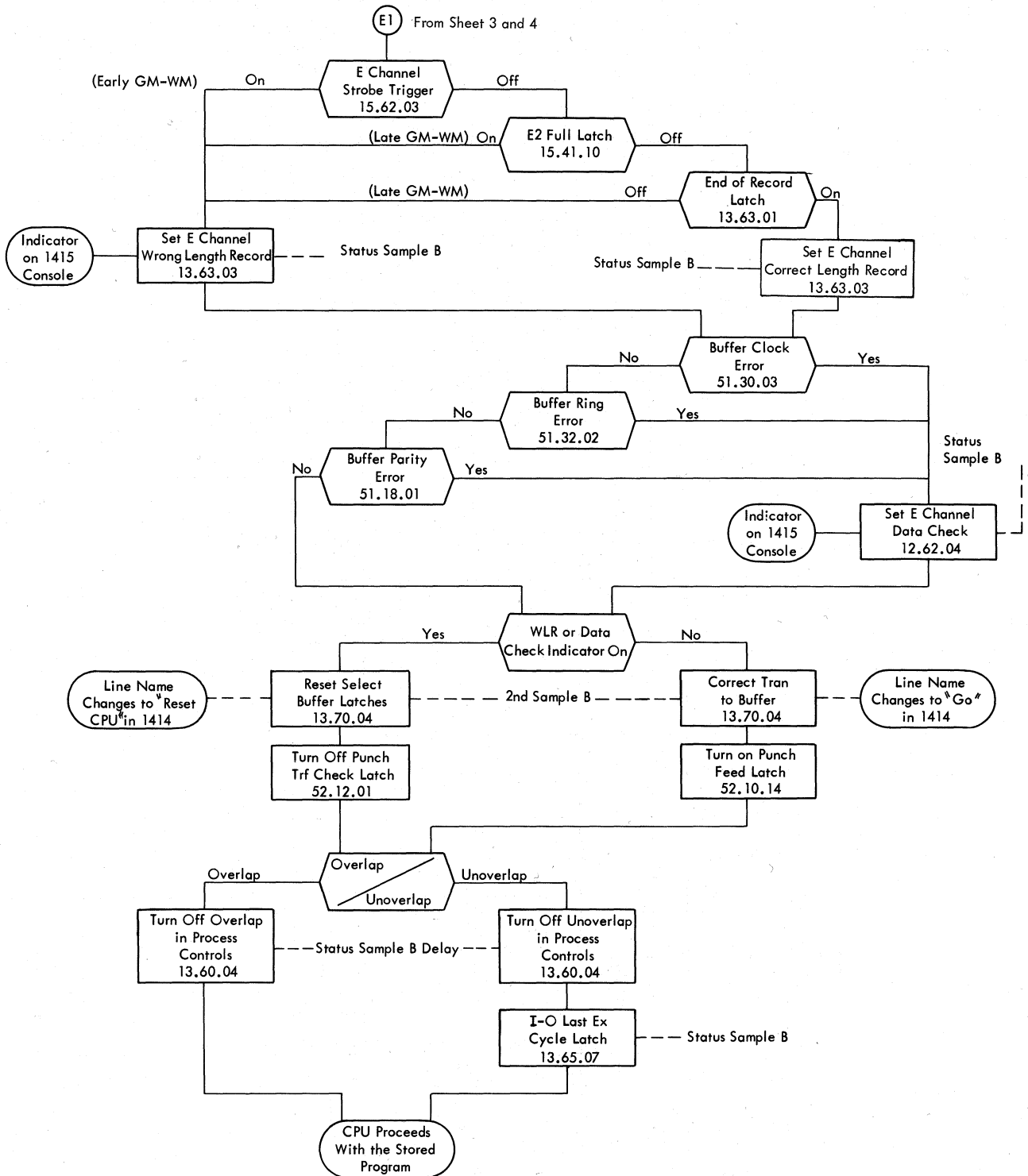


Figure 54. 1411-1402 Punch Operation – Logic Flow (Sheet 5 of 5)

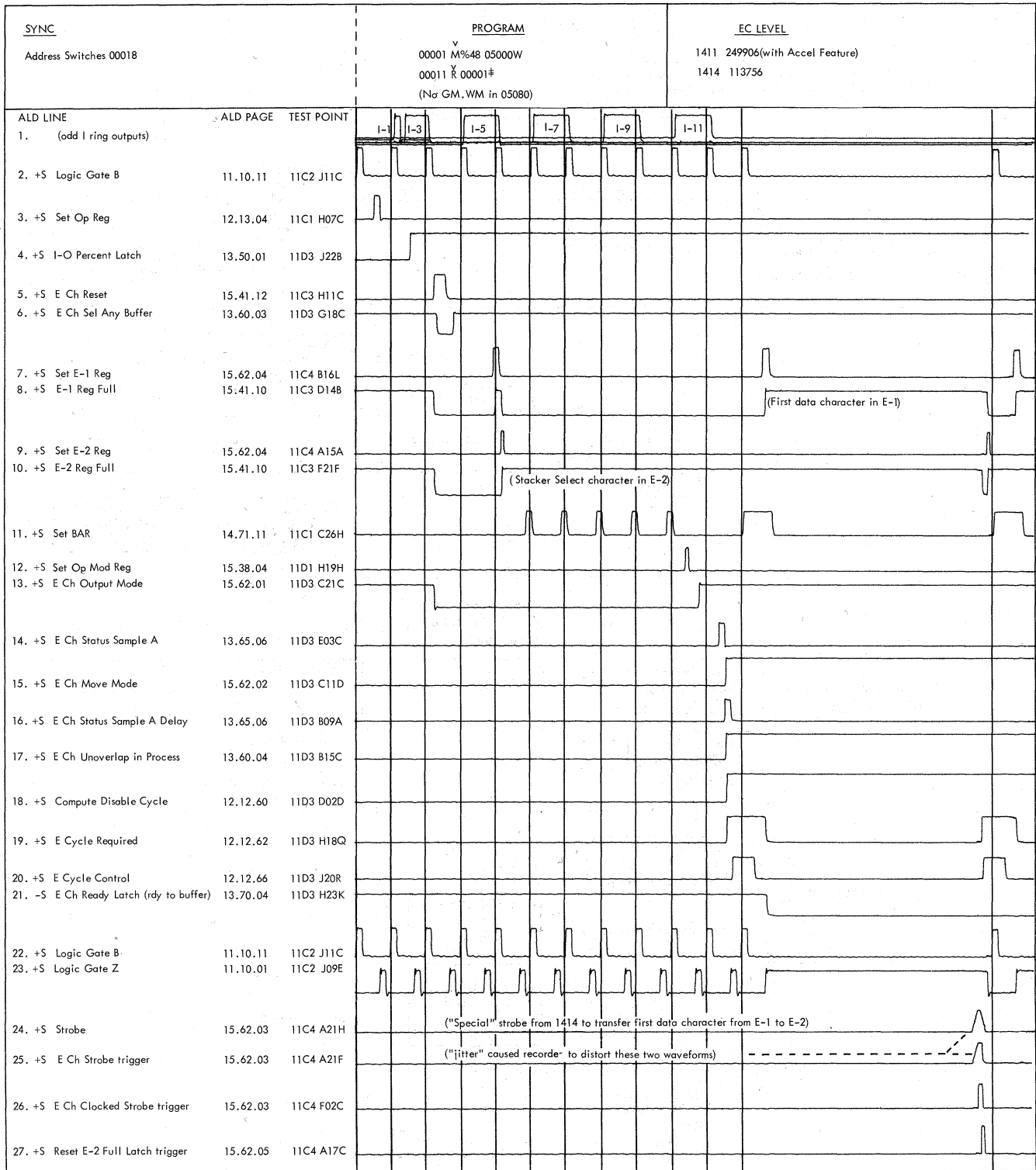


Figure 55. 1402 Punch Command Timing Chart

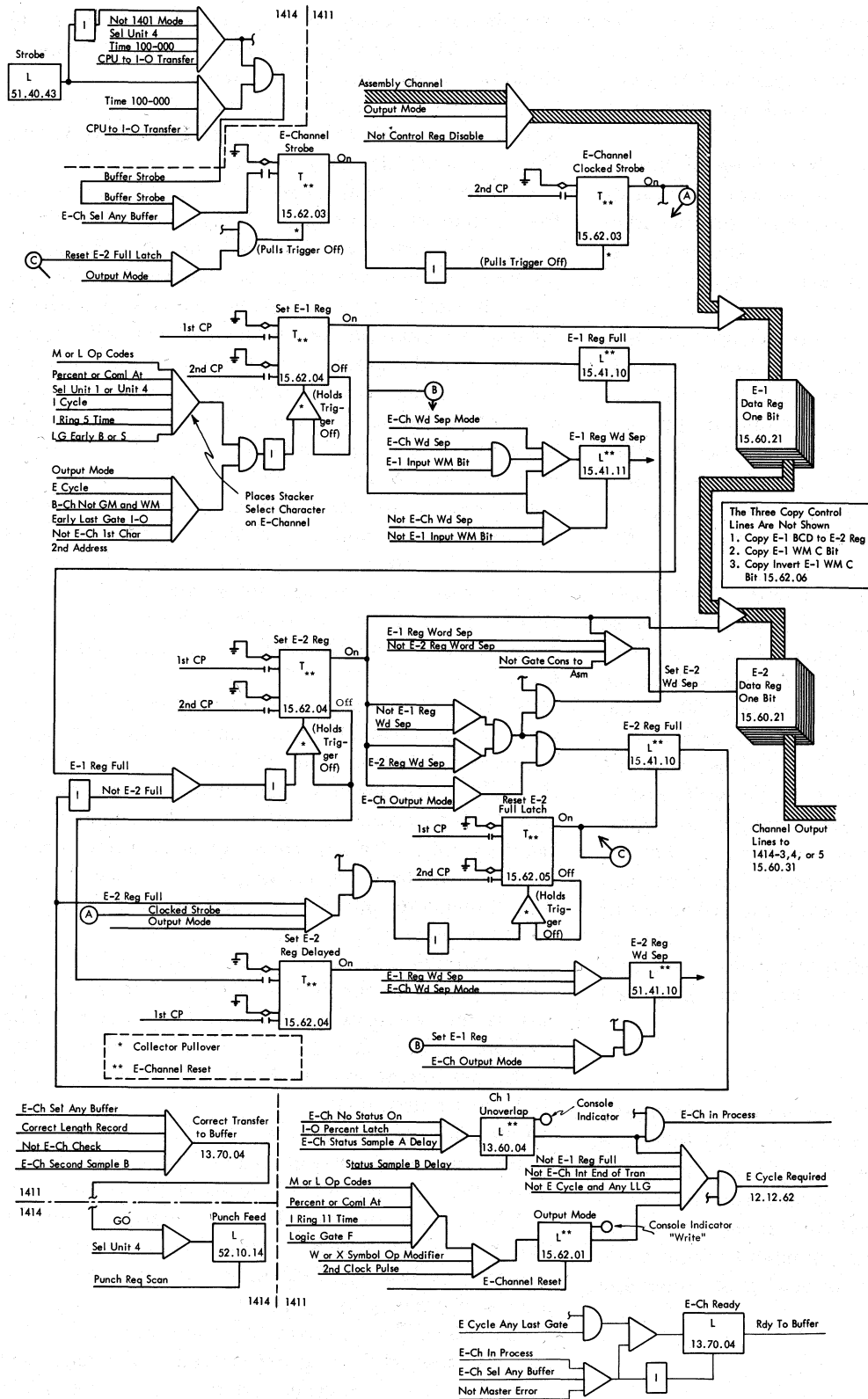


Figure 56. Channel Register Operation - Punch

acter in the channel data registers and sent to the punch buffer as a word separator character. A single word separator character in the output field is transferred to the punch buffer as two word separator characters.

The character in the hundreds position of the X-control field indicates the channel as well as indicating if the operation is to be in overlap or unoverlap mode, as shown earlier. The tens position of the X-control field contains the unit-select character; a 4 selects the 1402 punch. The units position of the X-control field contains the unit number character which is placed on the channel output data lines during I-phase. The 1414 synchronizer samples the data lines at the beginning of E-phase to condition the card stacker selection circuits. If the unit number is either a 0, 4, or 8, the card is stacked into the NP, 4, or 8 pocket, respectively. If an error is detected during card punching or card checking, the card is stacked in the NP pocket.

The B-address specifies the high-order (left) position of the output field because the record is reverse scanned (left to right) from the core storage unit; For example, if the B-address specified address 00000, the first character would be taken from address 00000 and the second character from address 00001, and so on.

The d-character should be W to indicate a write, or output, operation. A GM-WM must be positioned in the output field so that exactly 80 characters are transferred or a wrong length record (WLR) indication occurs and the card is not punched (no card feed cycle). If an X d-character is used, the B-address of the command must be selected so that exactly 80 characters are transferred before the end of storage is sensed or the record is not punched (no card feed cycle), and a WLR indication results.

I-Phase Sequence

Details of M/L instruction read-out are presented in the I-O Sequence section of this manual. The following presentation assumes a knowledge of M/L instruction read-out. Instruction read-out causes the instruction word characters to be placed in various registers to control execution of the punch command (Figure 54). An M or L in the op register brings up the following op code grouping lines:

- M or L op codes
- Percent type op codes
- Address type op codes
- Two address op codes
- 2 Addr Plus Mod Op Codes
- No Index on 1st addr ops
- No branch op codes
- Not addr dbl op codes

I-Op Time: The op code character reads out and is placed into the op register, bringing up the op code

grouping lines. Later in the cycle, the character in the op register conditions the set of the channel move mode or channel load mode latch.

I-1 Time: The special advance control latch is turned on to gate two extra pulses (logic gates C and D) to advance the I-ring to I-3.

I-3 Time: The channel select character is placed in the I-O channel select register. With a channel selected, the channel interlock test is made to see if the stored program has interrogated the channel status indicators since the last command to the selected channel. A satisfactory interrogation of the channel status indicators resets the move, or load, latch for that channel. Therefore, if the move or load latch is on at the start of another channel operation, the I-O interlock check indicator on the 1415 console is turned on, master error becomes active, and the CPU stops at I-3.

I-4 Time: A channel reset is generated, resetting the channel controls and the channel status indicators (Figure 17). The unit-select character reads out and is gated to the channel unit-select register. A 4 in the register gates the punch status to the channel status buses later in I-phase when the output mode latch is set.

I-5 Time: The unit-number character reads out and is sent to the channel register, appearing on the channel output data lines. The lines are later sampled by the 1414 synchronizer to condition the card stacking circuits. The character remains in the channel data registers until a special strobe signal is received from the 1414 synchronizer, causing CPU to place the first output character into E-2. A character in E-2 appears on the channel output data lines.

I-6 through I-10 Time: The B-address reads out and is placed in the B-address and D-address registers. If the command specifies overlap operation, the B-address is also placed in the E-address register (for E-channel operation), or the F-address register (for F-channel operation).

I-10 Time: If the command specifies unoverlap operation, the computer is interrupted (disabled) at I-10 time if the other channel is executing an I-O operation. In other words, an unoverlapped operation cannot be started if an overlapped operation is in process. The computer is kept disabled only until the channel in process completes its operation.

I-11 Time: The d-character reads out and is set into the op-modifier register. Because of overlapped operation, the op register, op-mod register and the I-O channel select register must be free to accept characters of the next instruction word. Therefore, the information in these registers must be stored in the channel control latches. During I-11 time, the W (or X) in the op-mod register gates the set of the output mode latch (E-channel), or the write latch

(F-channel). The output of the latch lights the write indicator, for that channel, on the 1415 console. The output mode latch also gates the assembly channel to E-1 input, and switches with E-cycle or F-cycle (systems 13.60.06) to produce output cycle. Output cycle brings up "regen memory" and also conditions the B-channel and assembly controls.

If the d-character is not a W or X, output mode to buffer is not active and the punch ready status is not gated to the channel ready bus. A channel not ready indication results. See Figures 102 and 103.

I-12 Time: I-12 is the last instruction read-out cycle, during which the channel move or channel load latch is set according to the character in the op register. The status sample pulses are generated during I-12 time.

Last Execute Cycle: During the last instruction read-out cycle of an overlapped command, "last execute cycle *I-O" becomes active, gating the set of the I-cycle control latch (Figure 120).

Status Sample A: This pulse occurs at logic gate D of I-12 time, and samples the A-status buses. Figure 86 (condensed logic) shows generation of the status sample pulses.

Status Sample A Delay: This pulse occurs at logic gate E of I-12 time and samples the output of the channel status indicators. If any status indicators are on at status sample A delay time, the operation is terminated (no E-phase) and the program proceeds to the next sequential instruction (Figure 120).

I-Phase Channel Status Indicators

Channel status indicators that can be set at the end of I-phase (status sample A time) are referred to as A-status indicators. For an M%40 op code, the A-status indicators for the punch are:

Not Ready	(Requires manual intervention)
Busy	Punch is unloading the buffer (punching a card)
Condition	Last card in NP stacker is an error card

See the status indicator chart Figure 86.

Not Ready: Figure 102 shows the punch status gated to the CPU by "select unit 4." In CPU, "buffer ready" is gated to the channel ready bus by "E-channel select any buffer." With the ready bus active, the input to the channel not ready latch is blocked, preventing the status sample A pulse from turning on the latch.

Busy: If a punch command is issued to the IBM 1402 Card Read Punch while it is unloading the buffer (punching a card), a channel busy indication occurs and the command is not executed. Either the punch feed latch or the punch feed trigger being on causes the channel busy indicator to be set at status sample A time. See Figures 102 and 103.

Condition: This indicator is set for one of two types of errors that may occur during punch commands:

Latent errors	Sets the channel condition indicator.
Immediate errors	Sets the channel data check indicator, described later.

A latent punch error is any error resulting from a punch command where the error is not detected by the CPU until some later punch command; for example, in the following program assume that a latent error results from the command to punch card A.

00001	M%4803000W	Command to punch card A
00011	R000012	If busy, try again
00018	R010008	Branch to 01000 if condition indicator on
00025	R02000 ≠	Branch to 02000 if any indicator on
(Processing routine)		Card A is punched while CPU proceeds with program
00101	M%4804000W	Command to punch card B
00111	R001012	If busy, try again
00118	R010008	Branch to 01000 if condition indicator on
00125	R02000 ≠	Branch to 02000 if any indicator on
(Processing routine)		Card B is punched while CPU proceeds with program
00201	M%4805000W	Command to punch card C
00211	R002012	If busy, try again
*00218	R010008	Branch to 01000 if condition indicator on
01000	.05000	Halt

*At this point, the CPU detects the latent error that occurred as a result of the command to punch card A, and branches to 01000; assume a halt at 01000.

The following conditions exist when the stored program is halted following a channel condition indication from the punch:

1. The last punch command (the command to punch card C in the preceding program sequence) is not executed.
2. The error card is the top card in the normal punch (NP) stacker.
3. The record following the error record has been punched.
4. If the operator clears the punch feed, the last record punched will not be checked at the punch check station.

If the CPU is not programmed to halt on a channel condition indication from the punch, the punch will respond to the next punch command. That is, the punch command following the one in which the error was detected.

Four different errors cause a channel condition indication; and cause the error card to be selected into the NP stacker:

1. Parity error during the punching card feed cycle

2. Buffer clock error during the punching card feed cycle
3. Buffer ring error during the punching card feed cycle
4. Hole-count error during the checking card feed cycle

Figure 57 shows that a card passes through the punch check station one card feed cycle after it passes through the punching station. A card is stacked on the same card feed cycle that it passes through the punch check station.

Referring to the program sequence, and Figure 57, assume that an error was detected by the 1414 synchronizer when card A was being punched. Because card A will not reach the stacker until the following card feed cycle, the error condition must be retained for one card feed cycle before it is sent to the CPU. Condensed logic Figure 104 shows that a parity error during a punch request scan sets the punch check 1 latch.

When the next card feed cycle occurs, the output of the punch check 1 latch AND's with "punch feed gate" to set the punch check 2 latch. During this card feed cycle, card A passes through the punch check station into the NP stacker. The error card always is selected into the NP pocket because the output of the punch check 2 latch brings up "-W stack inh" (ALD 52.13.01) to pick relay 35 in the 1402 Card Read Punch, opening the circuit to both stack select magnets. With the punch check 2 latch on and the error card in the NP stacker, the next punch command from the CPU results in the set of the channel condition indicator at status sample A time and the punch command is not executed. The CPU acknowledges the error by generating "reset select buffer latches" which goes to the 1414 synchronizer to reset the punch check 2

latch, permitting the next punch command to be executed (Figure 112).

A hole-count error is detected on the same card feed cycle that the error card enters the stacker. Consequently, the error condition does not need to be retained for a card feed cycle as described earlier. Figure 104 shows that a hole-count error sets the punch check 2 latch directly so that the next punch command will result in a channel condition indication.

Customer program routines may punch from three rotating output areas so that a record resulting in a channel condition indication is available for repunching. Program routines may also issue a final punch command to punch 80 blanks, causing the last data card to be checked and moved to the stacker.

E-Phase Sequence

If no status indicators are set at status sample A time, "status sample A delay" turns one of the four channel in process latches, according to the character in the i-o channel select register.

Percent sign	%	E-channel unoverlap in process
Commercial at	@	E-channel overlap in process
Asterisk	*	F-channel unoverlap in process
Lozenge	◻	F-channel overlap in process

Each latch has an indicator on the 1415 console. If the punch command specifies overlap, the CPU proceeds with the next sequential instruction after setting a channel in process latch. If any status indicator was turned on, the CPU does not execute the punch command and proceeds with the stored program.

During E-phase, the CPU transfers characters from core storage to the i-o channel on request from the channel controls. Use Figures 53, 55, and 56 to follow the data transfer operation.

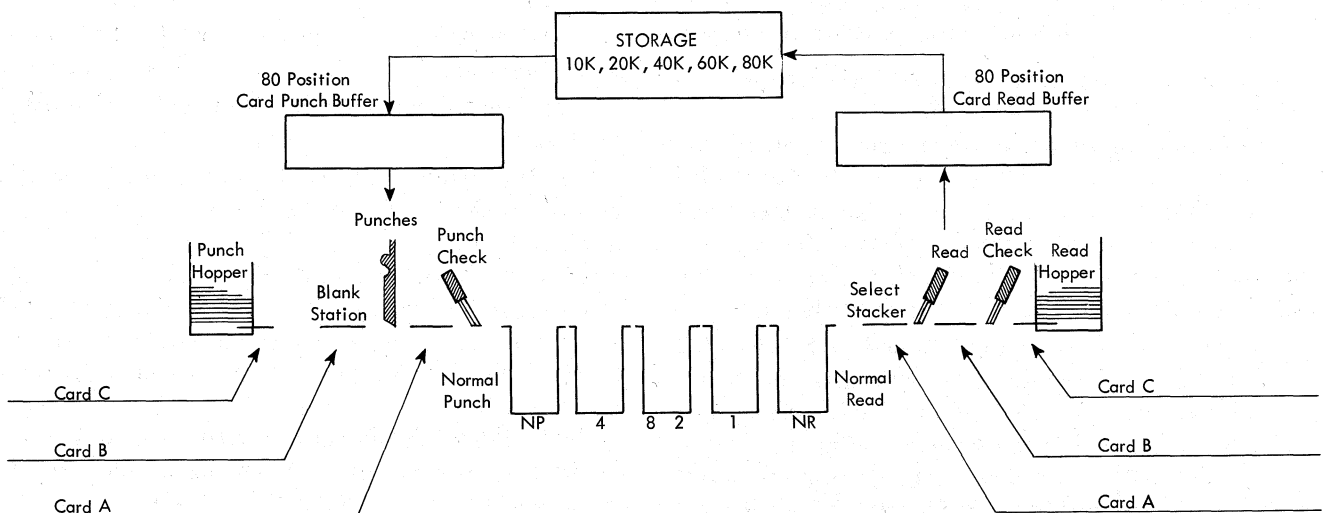


Figure 57. 1402 Card Transport

Channel In Process Latch: With no status indicators on at the end of I-phase, one of the four channel in process latches is turned on. "E-ch in process" AND's with "not E-1 reg full" and other conditions (Figure 56) to bring up "E-cycle required," causing an E-cycle that brings the first output character from core storage to E-1. At this point, the E-2 full latch is on because E-2 contains the stacker select character. During this E-cycle, the E-channel ready latch (not the channel status indicator) is turned on, bringing up "ready to buffer" which initiates buffer operation.

E-Channel Ready Latch: The output of the latch, "ready to buffer" turns on the ready 2 latch in the 1414 synchronizer. If no scan is in progress, the ready 1 latch is turned on and the output AND's with "punch ready," "punch not busy," and "select unit 4" to turn on the punch transfer request latch. See the appropriate condensed logic diagram in the *IBM 1414 Input Output Synchronizer 3, 4, 5, and 6*, Customer Engineering Instruction-Reference Manual, Form 223-2590.

Punch Priority Request Trigger: "Punch transfer request," developed earlier, provides a gate for the turn on of the punch priority request trigger. The output of this trigger AND's with not "some scan" to gate the turn on of the Punch scan trigger, which starts the buffer operation.

Punch Scan Latch: The latch sets at 030-040 time and turns on the time P1 1 latch, starting buffer ring operation at the next 000 time.

Mod Stk Select: At 100-000 time, just before the start of the first buffer cycle, "mod stk sel" samples the channel output data lines (E-2 character) and sets stacker select latches. The same signal is gated to the CPU as a special strobe, causing the first data character to transfer from E-1 to E-2.

Strobe Latch: At 020-030 time of the first buffer cycle the buffer strobe latch turns on to gate every 100-000 time pulse to CPU as "buffer strobe." The strobe latch is turned off when "punch trans scan" falls at the end of scan.

Channel Operation: During each buffer cycle, the character on the channel output lines is written into the punch buffer. A strobe signal generated by the synchronizer causes the channel controls to set the next output character into E-2. The character transfers from the E-1 register to the E-2 register under supervision of the register transfer and data flow controls. An E-cycle is taken to bring a new character from core storage to E-1 (Figure 56). See Figure 115 for processing overlap circuit for E-cycle required.

Unoverlapped Operation: The CPU is idle (logic clock ring is disabled) except when the channel controls request the CPU to take an I-O data cycle (E cycle)

to transfer an output character from core storage to E-1 (Figure 118).

Overlapped Operation: At the end of I-phase of the read command, the CPU proceeds with the next sequential instruction. Processing (computing) continues until the channel controls request the CPU to take an I-O data cycle to transfer a character from core storage to E-1. Computing is interrupted (disabled) while the CPU brings a new output character to E-1; computing is then resumed (Figure 118).

External End of Transfer Trigger: Once the buffer operation is initiated, the operation continues until all 80 positions have been written with data from the channel output data lines. The synchronizer signals CPU the end of buffer operation by generating "buffer end of transfer" which turns on the external end of transfer trigger in the CPU. If the ready bus becomes inactive during a buffer transfer operation, the external end of transfer trigger is turned on immediately. If an early GM-WM prematurely terminates transfer of output characters, the remainder of the buffer is filled with the last output character, which remains in E-2.

Internal End of Transfer Latch: A GM-WM in the output field, or a core storage wrap-around condition, turns on the internal end of transfer latch, blocking the CPU from taking any more I-O data cycles. With the GM-WM correctly positioned in the output field, the internal end of transfer trigger is turned on before the external end of transfer latch. "External end of transfer" forces "internal end of transfer" when no GM-WM appears in the output field (Figure 101).

Status Sample B Trigger: With both the external end of transfer trigger and the internal end of transfer latch ON, the status sample B trigger is turned on at the end of the last I-O data cycle (E-cycle). The trigger is on for two clock pulses and the output of the trigger is used to set the B-status channel indicators (Figure 101).

Second Sample B Trigger: This trigger is turned on the next 1st clock pulse after the status sample B trigger is turned on. The trigger is on for two clock pulses and the output of the trigger samples the outputs of the B-status indicators.

Status Sample B Delay Trigger: This trigger is turned on the next 1st clock pulse after the second sample B trigger is turned on. The trigger is on for two clock pulses and the output of the trigger resets the channel in process latch.

E-Phase Channel Status Indicators

Channel status indicators that can be set at the end of E-phase (status sample B time) are referred to in this manual as B-status indicators.

The B-status indicators for the punch are:

Data Check Figure 104 (condensed logic)

Wrong Length Record Figure 105 (condensed logic)

See also the status indicator chart, Figure 86.

Data Check: If the punch transfer check latch is on in the 1414 synchronizer, the output of the latch is gated to the channel check bus and status sample B turns on the data check indicator.

Wrong Length Record: A GM-WM must be positioned in the output field so that exactly 80 characters are transferred to the punch buffer or a wrong length record (WLR) indication occurs. During load mode operation, WM and WS characters must be considered when computing the number of output characters. See "Channel Status Indicators" in the I-O Principles of Operation section.

Correct Transfer To Buffer: If neither the channel wrong length record or channel data check indicator is turned on at status sample B time, correct trans to buffer is sent from the CPU to the 1414 synchronizer. "Correct trans to buffer" ("go" in the 1414) AND's with "select unit 4" to turn on the punch feed latch, initiating a punch feed cycle. Note that the record is not punched if a channel WLR or a channel data check occurred (Figure 56).

Reset Select Buffer Latches: If a buffer clock, buffer ring, or a buffer data error occurs during a CPU to buffer transfer, the punch transfer check latch is set, sending "buffer error" to the CPU. Buffer error gates the turn on of the channel data check indicator at status sample B time. CPU acknowledges the buffer error by generating "reset select buffer latches" ("reset CPU" in 1414) at second sample B time. The "reset CPU" line resets the punch trf check latch, preventing a false error indication on the next CPU to buffer transfer (Figure 112).

If a hole-count error sets the punch check 2 latch, "buffer condition" is gated to CPU during I-phase of the next punch command. Status sample A sets the channel condition latch, and status sample A delay sends "reset select buffer latches" to the 1414 synchronizer, acknowledging the error. The command is not executed, but the "reset CPU" line turns off the punch check 2 latch, permitting the next command to be executed (if no indicators are turned on).

Last Execute Cycle: "E-channel status sample B" AND's with "E-channel unoverlap in process" to set the I-O last execute cycle latch which gates the turn on of the I-cycle control latch. "Status sample B delay" resets the E-channel unoverlap in process or E-channel overlap in process latch (Figure 120).

1411-1403 Printer Operation

For ease in understanding the following operations, you should be familiar with the information in the Input-Output Principles of Operation, Channel Data Register Control, and I-O Sequence sections of this manual.

Information on the operation of the IBM 1403 Printer and the IBM 1414 I-O Synchronizer is contained in *IBM 1403 Printer*, Customer Engineering Manual of Instruction, Form 225-6492, *IBM 1403 Printer*, Customer Engineering Reference Manual, Form 225-6493; and *IBM 1414 Input-Output Synchronizer*, Customer Engineering Instruction-Reference Manual, Form 223-2590.

Three types of commands are used with the 1403 printer. Two are variations of the basic I-O command used with all I-O devices. Using E-channel overlapped operation as an example, the three commands are:

\checkmark M %20 BBBB W

Transfer data to print buffer and initiate a print operation (if data transfer is correct).

\checkmark M %21 BBBB W

Transfer a 1 to the print buffer for each word mark in the output field (no data is transferred) and initiate a print operation (if data transfer is correct).

\checkmark Fd

Move forms under control of d-modifier character.

Printer Load Command

Load mode operation is seldom used with the 1403 printer because a word separator (ws) character is not a printable character. If an output field containing word marks or word separator characters is transferred to the print buffer in load mode, each word mark appears in the buffer as a word separator character. Each word separator character in the output field appears in the buffer as two word separator characters. A blank space appears in the printed line in place of each word separator character in the print buffer.

A GM-WM must be positioned in the output field so that exactly 100 characters (for the IBM 1403, Model I) are transferred to the print buffer or a wrong length record indication results and the record is not printed. When using load mode, word mark-word separator conversion must be considered when determining the number of output characters.

Note: See ALD 51.43.20 for a feed-through list

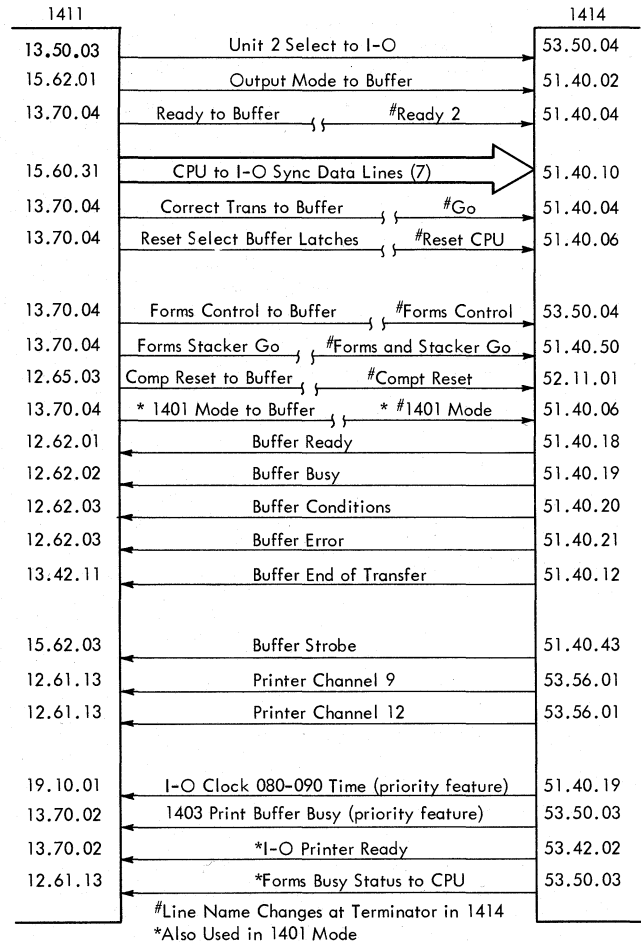


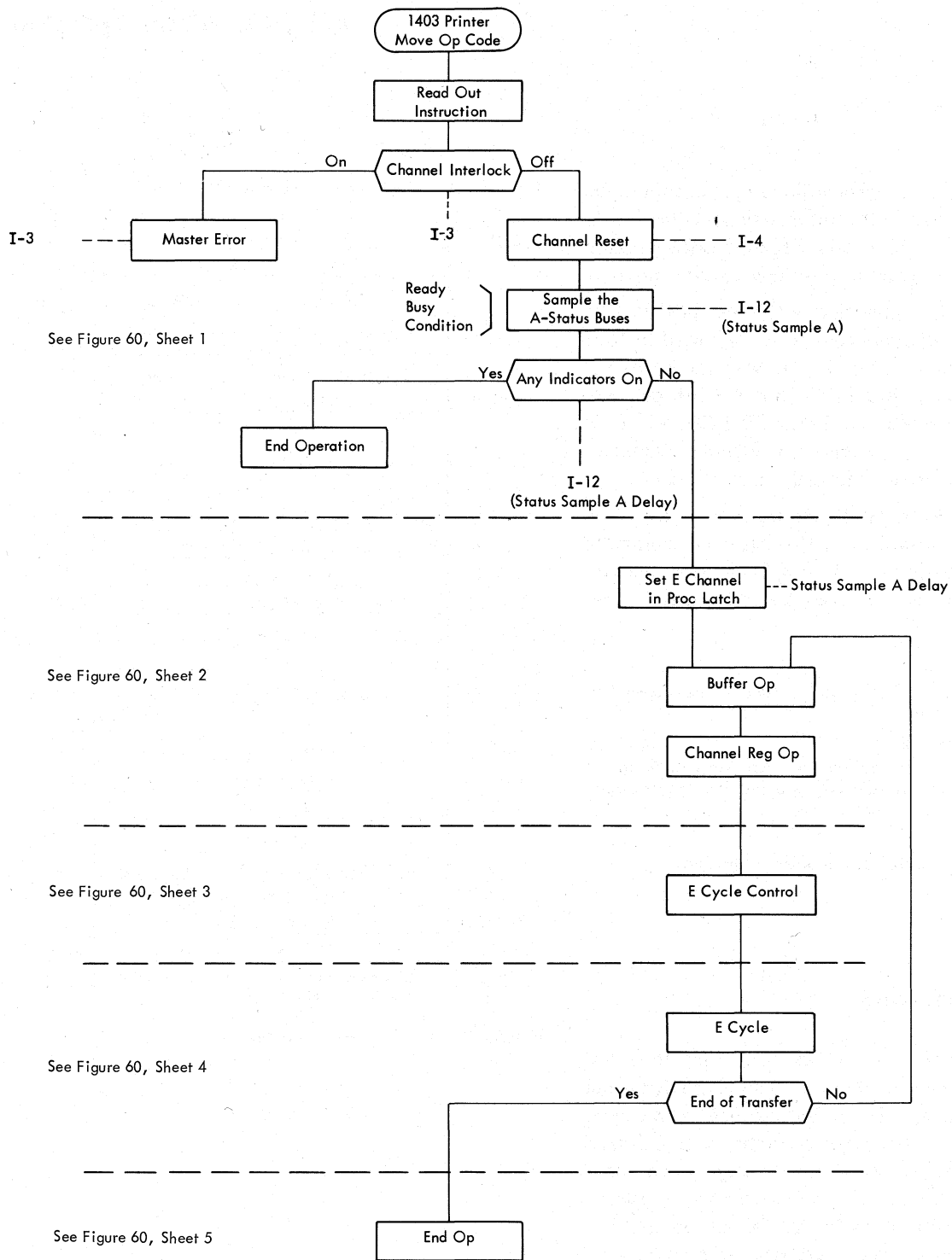
Figure 58. Channel Lines - Printer

Printer Move Command

Instruction format: O XXX BBBB W

For instructional purposes, diagrams are referred to at the appropriate point in the text. Use Figures 34, 58, 59, 60, 61, and 62 for reference purposes.

The basic I-O instruction format is used for 1403 printer move or load operation. The hundreds position of the X-control field must contain one of the following characters or an instruction check occurs:



See the indicated figures for a more detailed flow chart

Figure 59. 1411-1403 Printer Operation – Basic Logic Flow

See Figure 34 for a detailed flow chart of an M/L Instruction Read-Out Operation

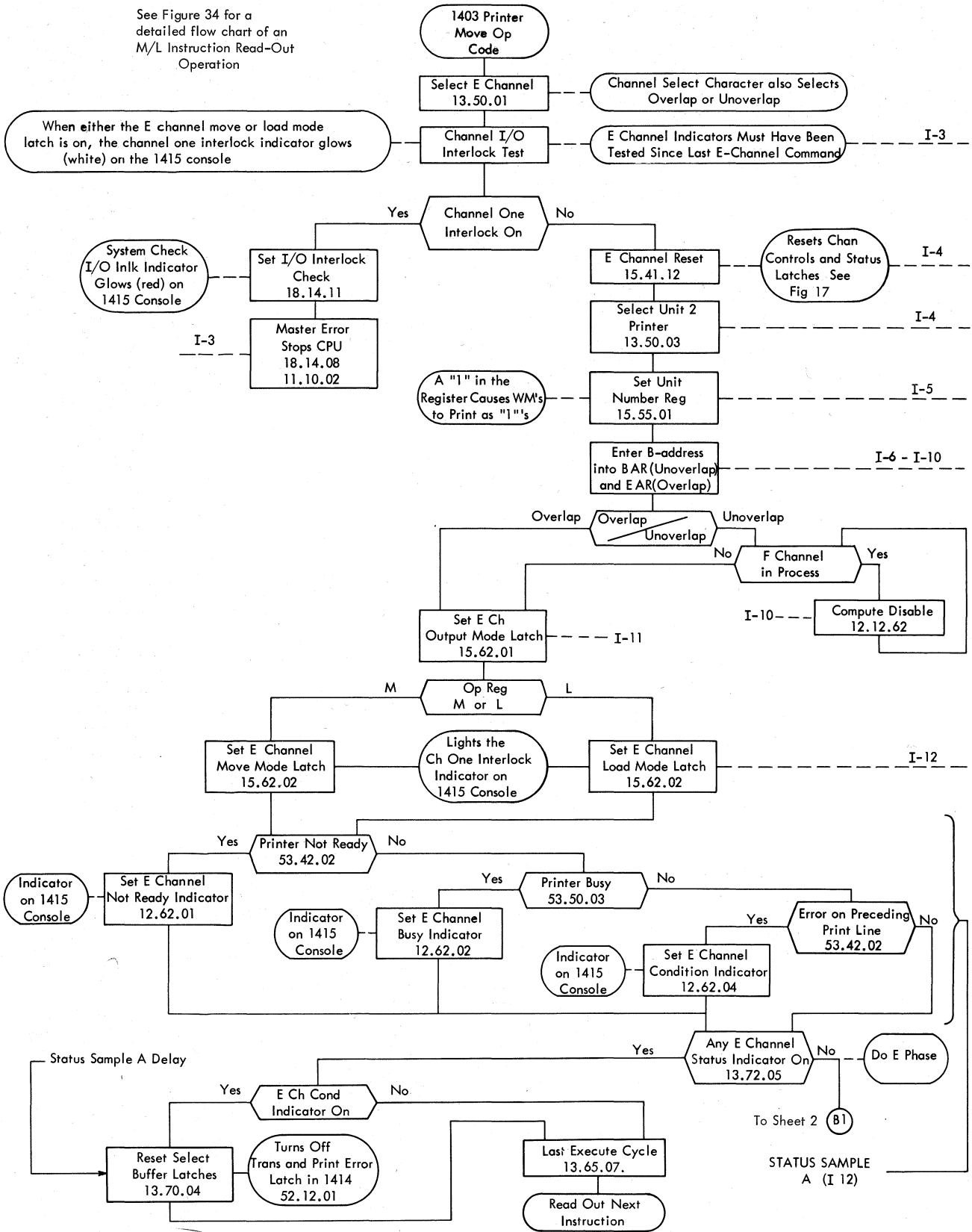


Figure 60. 1411-1403 Printer Operation – Logic Flow (Sheet 1 of 5)

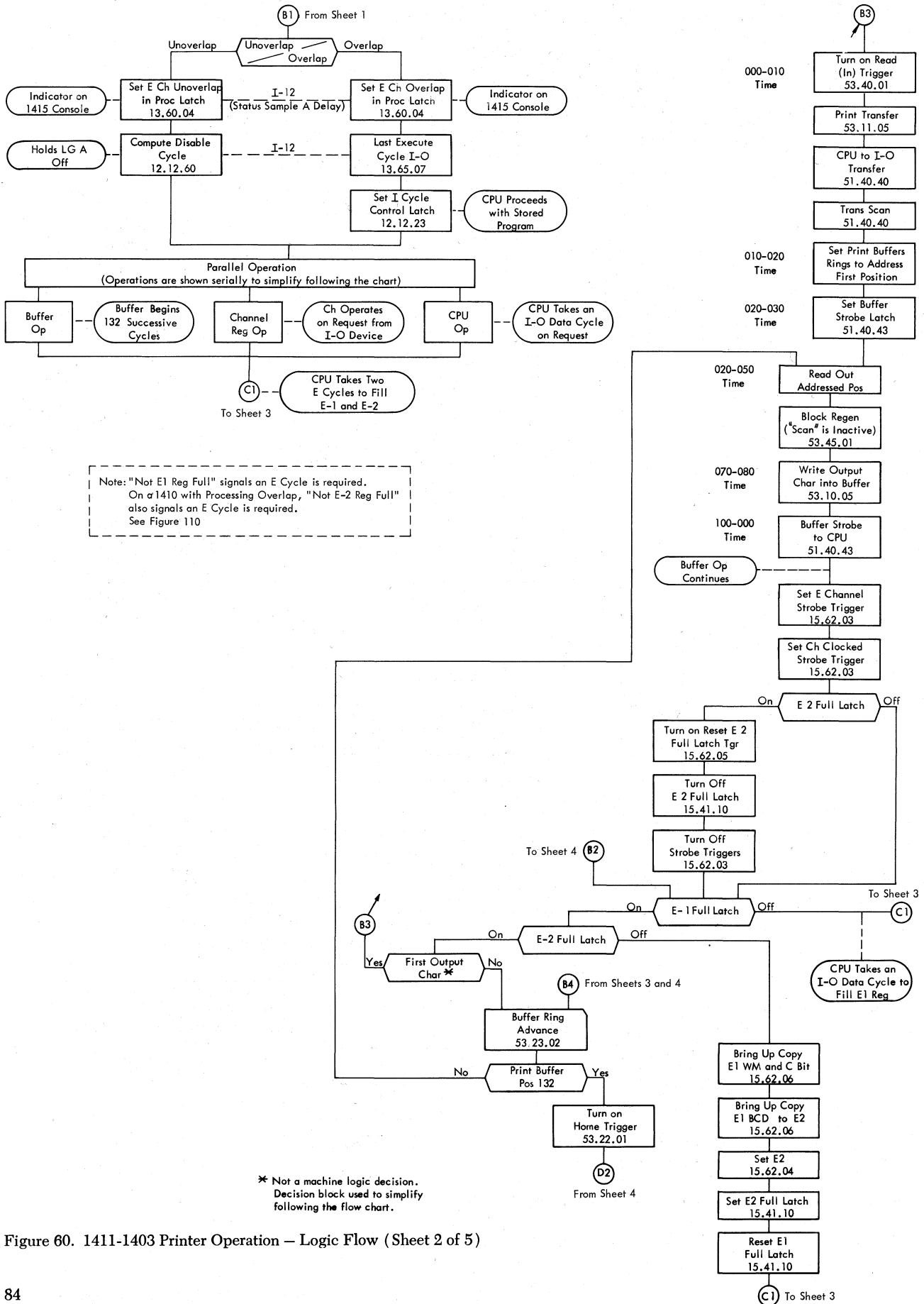


Figure 60. 1411-1403 Printer Operation – Logic Flow (Sheet 2 of 5)

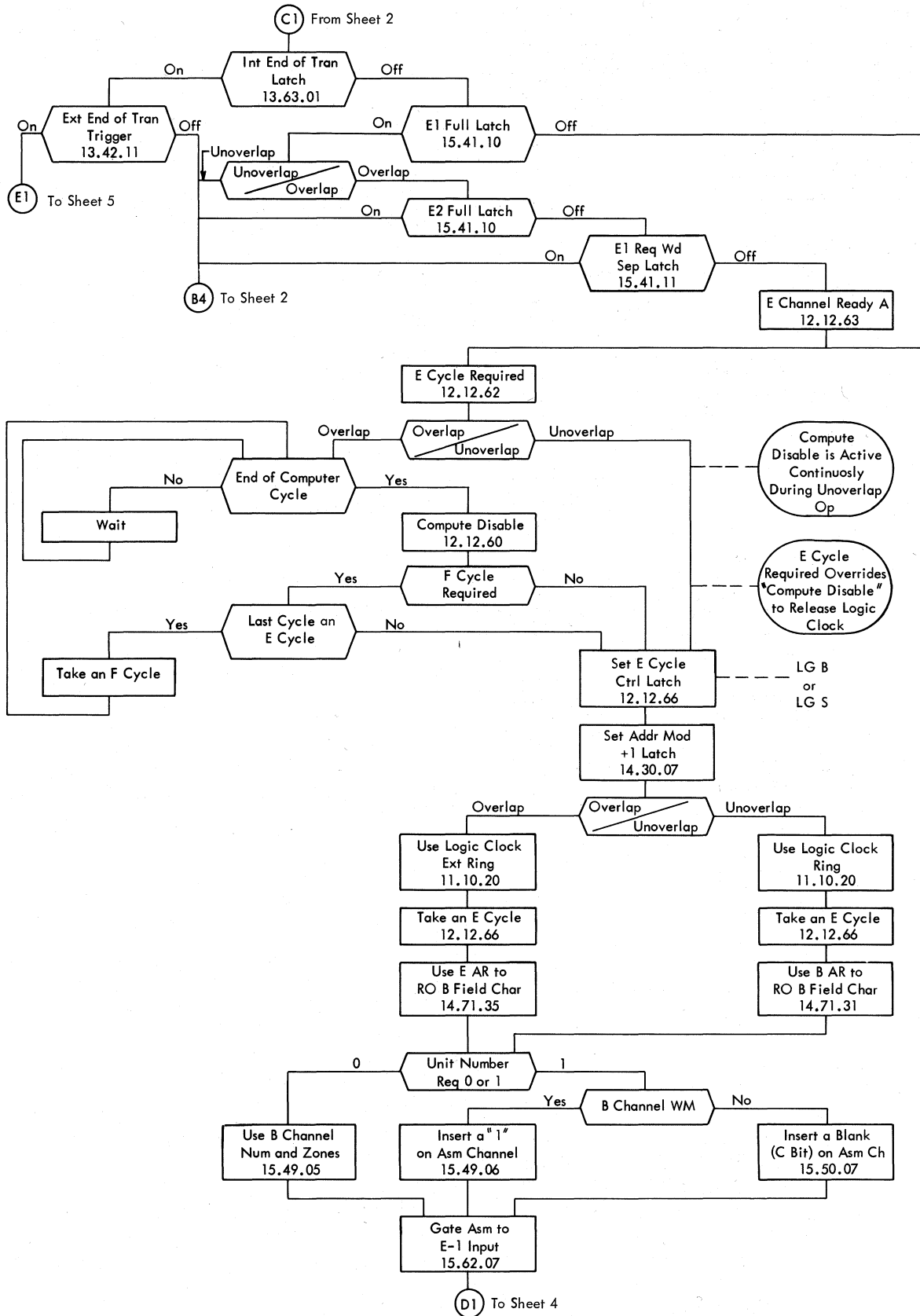


Figure 60. 1411-1403 Printer Operation – Logic Flow (Sheet 3 of 5)

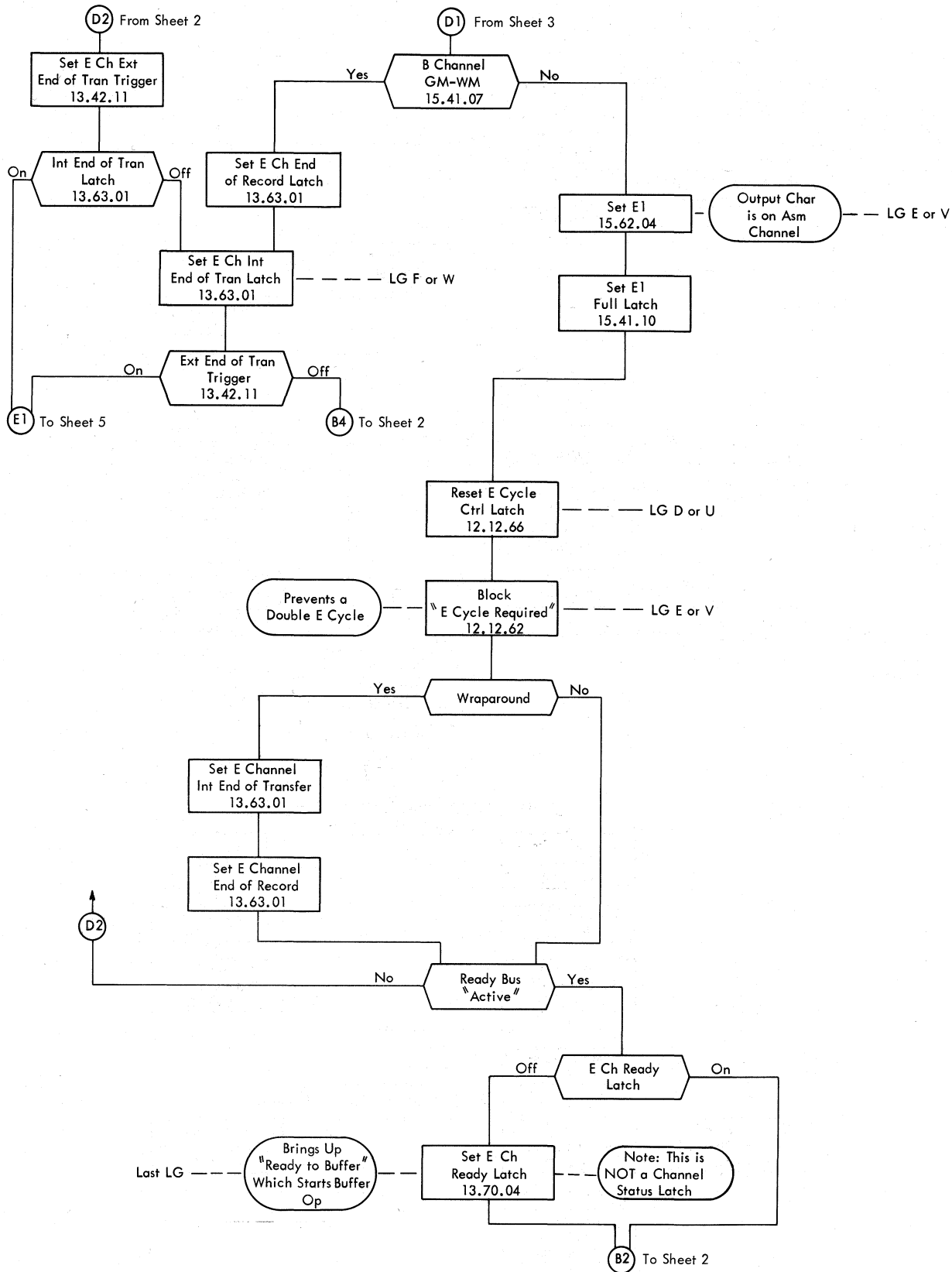


Figure 60. 1411-1403 Printer Operation – Logic Flow (Sheet 4 of 5)

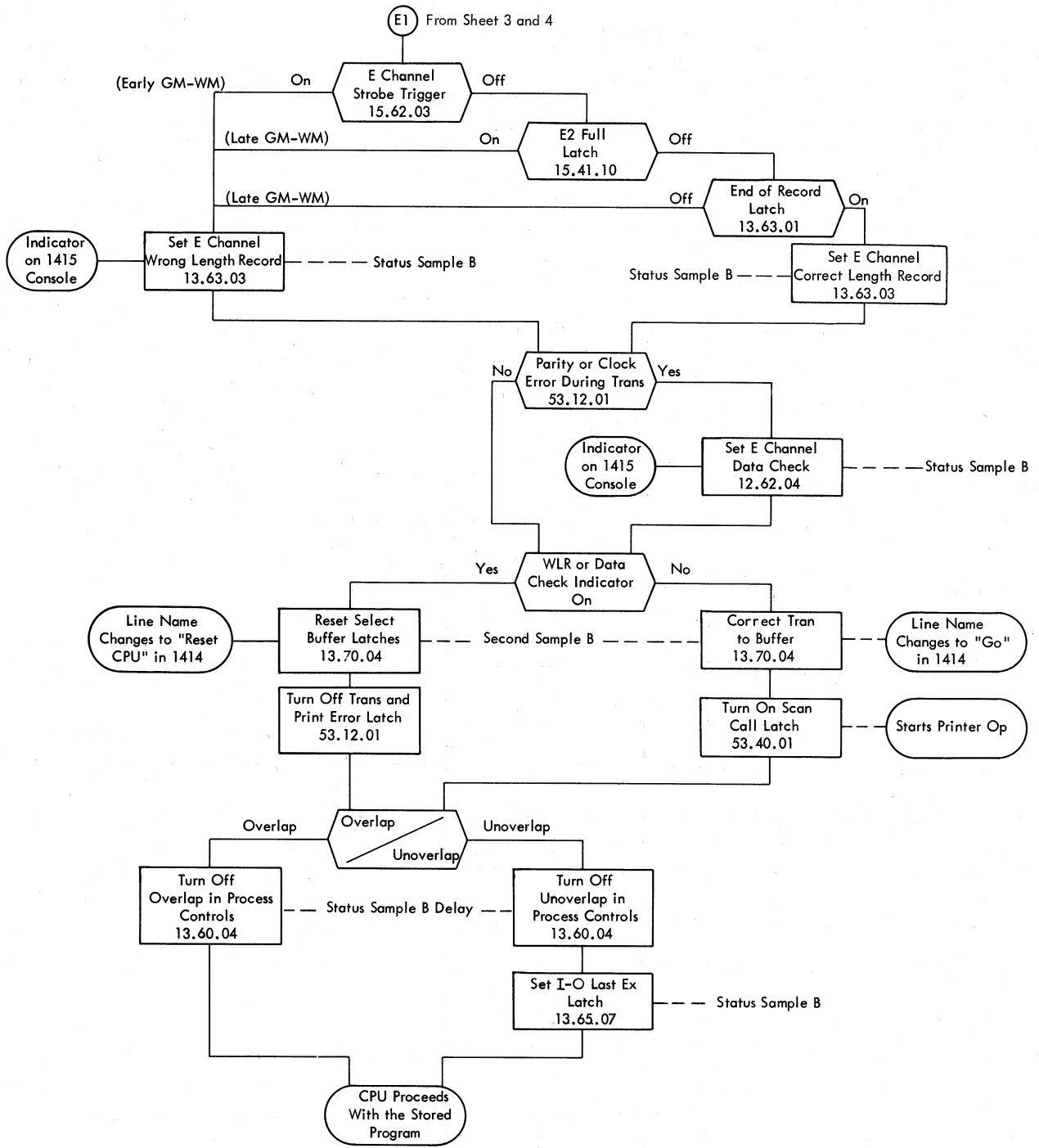


Figure 60. 1411-1403 Printer Operation – Logic Flow (Sheet 5 of 5)

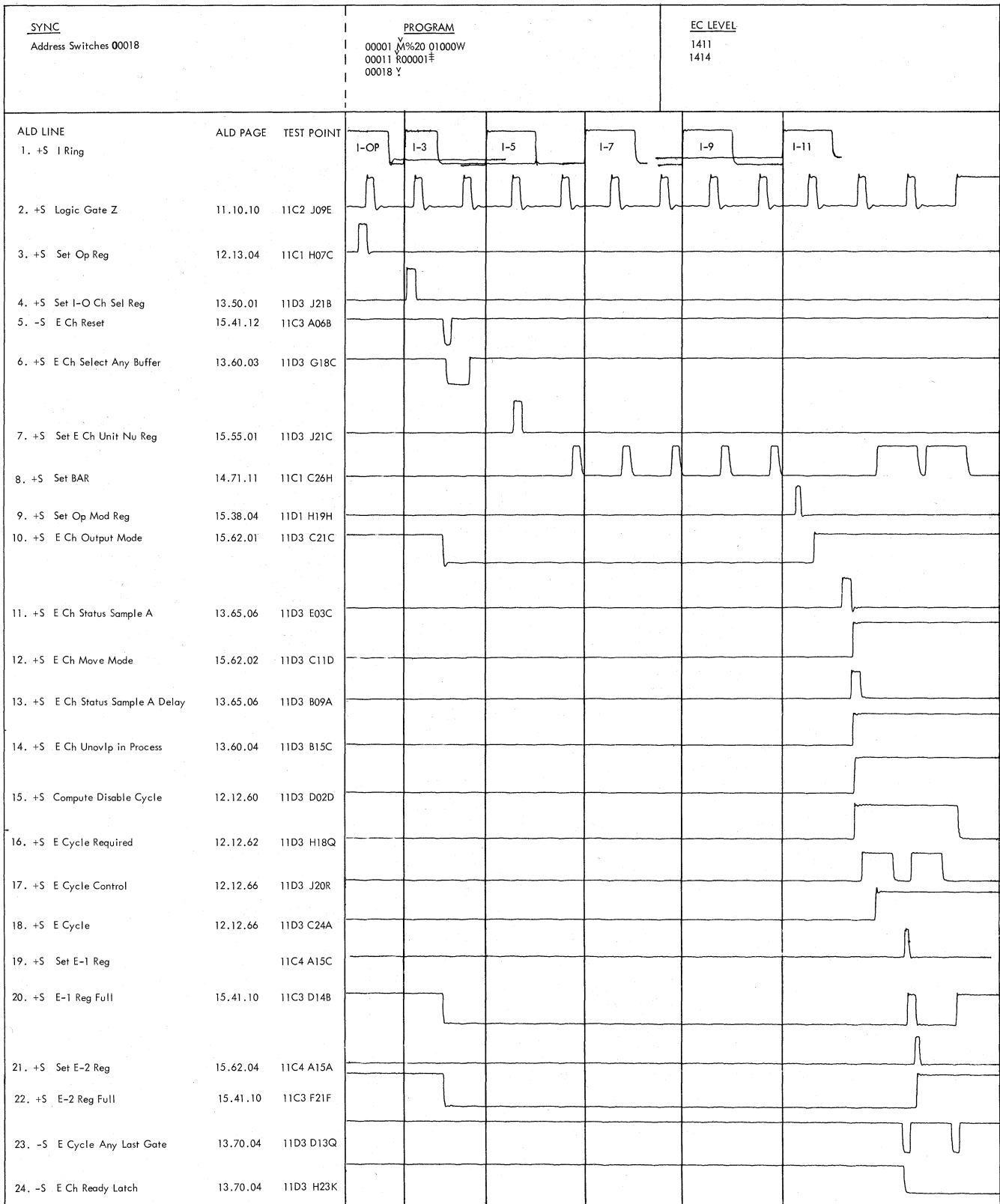


Figure 61. 1403 Print Command Timing Chart

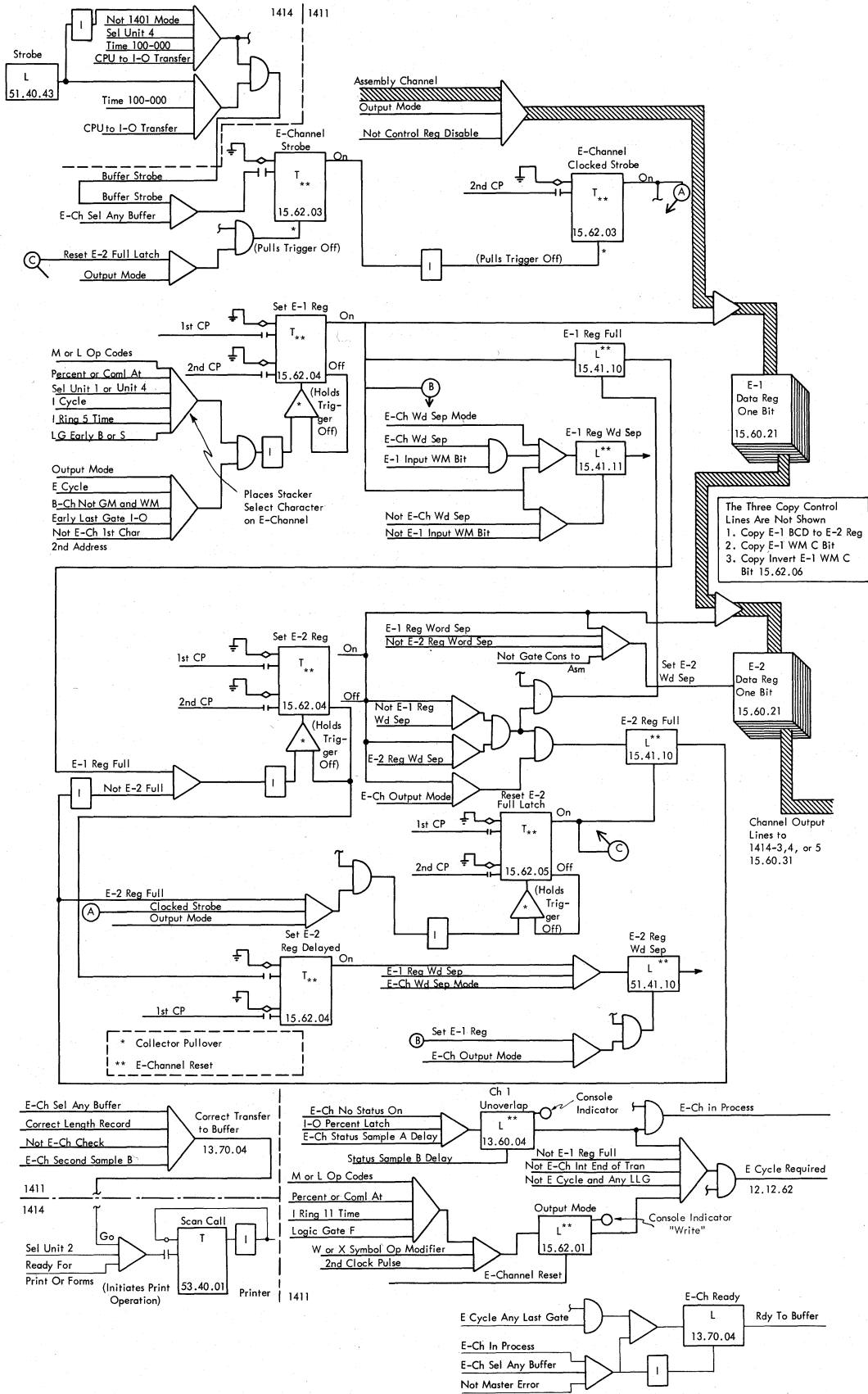


Figure 62. Channel Register Operation — Printer

Percent sign	%	E-channel unoverlap
Commercial at	@	E-channel overlap
Asterisk	*	F-channel unoverlap
Lozenge	□	F-channel overlap

The tens position of the X-control field contains a 2 to select the printer. The units position of the X-control field should contain one of these two characters:

0	Print data (ignore word marks in the output field)
1	Print a 1 for word marks in the output field (ignore data)

Figure 99 shows the assembly controls for printing 1's for word marks.

Figure 59 shows basic logic flow for a printer move op code. Note that the command is not executed if any channel status indicators are on at the end of I-phase (status sample A time). If no channel status indicators are on, the command is executed and the output field in the CPU is transferred to the printer storage (buffer) in the 1414 synchronizer. The B-address specifies the high-order (left) position of the output field, because the record is reverse scanned (left to right) from the core storage unit. The d-character may be a W or an X indicating a write, or output, operation. If an X d-character is used (write to end of storage) the initial data address must be selected so that the correct number of characters are transferred to the printer or the 1403 will not print.

The write word marks command, M%21, is used in a program printout, for example, where it is necessary to identify word mark characters. The 1403 printer can print neither word marks or word separator characters so the write word marks command permits the printer to print a 1 in place of a word mark in the output field.

SAMPLE PROGRAMMING SEQUENCE		
00001	M%2101000W	Write word marks
00011	R000012	If busy, try again
00018	R02000⊥	Branch on any status indicator (to any routine)
00025	M%2001000W	Write a record
00035	R000252	If busy, try again
00042	R02000⊥	Branch on any status indicator (to any routine)
(main routine)		Process data
(branch to print routine)		Print next record
↓ OUTPUT FIELD ↓		
01000	A0800008010D0881008710LJ etc	
01132	⊥	
PRINTED RESULT		
(first line)		1 1 1
(second line)		A0800008010D0881008710LJ etc

I-Phase Sequence

Details of I-O instruction read-out are presented in the I-O Sequence section. See Figure 34. The following presentation assumes a knowledge of I-O instruction read-out, and shows only the more important aspects of the instruction read-out.

During I-phase, the instruction word characters are read out of the 1411 core storage unit and placed in various registers to control the execution of the print command. An M or L in the op register brings up the following op code grouping lines:

M or L Op Codes
 Percent Type Op Codes
 Address Type Op Codes
 Two Address Op Codes
 2 Addr Plus Mod Op Codes
 No Index on 1st Addr Ops
 No Branch Op Codes
 Not Addr Dbl Op Codes

I-Op Time: The op code character reads out and is placed into the op register (Figure 54), bringing up the necessary op code grouping lines. An M in the op register specifies move mode. Load mode is seldom used in 1403 printer operation and is not described.

I-1 Time: The special advance control latch turns on to gate two extra advance pulses (LG C and LG D) that advance the I-ring to I-3.

I-3 Time: The channel select character reads out and is placed in the I-O channel select register. With a channel selected, the I-O channel interlock test is made to see if the stored program has interrogated the channel status indicators since the last channel command for the selected channel. A satisfactory interrogation of the channel status indicators resets the move (or load) latch for that channel. Therefore, if the channel move or load latch is on at the start of another operation, a satisfactory test was not made, the I-O Interlock check indicator (on the 1415 console) is turned on, "master error" becomes active, and the CPU stops at I-3.

I-4 Time: A channel reset is generated, resetting the channel controls and the channel status indicators (Figure 17). The unit-select character reads out and is gated to the channel unit-select register. A 2 in the register gates the printer status to the channel status buses later in I-phase when the output mode latch is set.

I-5 Time: The unit number character reads out and is set into the unit-number register. The character conditions the assembly controls. A 0 in the register permits data in the output field, except word marks, to be transferred to E-I. A 1 in the register causes insertion of a 1 on the assembly channel for each position of the output field that contains a word mark. If no word mark is present, a blank (C-bit) is inserted on the assembly channel.

I-6 through I-10 Time: The B-address reads out and is placed in the B-address and D-address registers. If the command specifies overlap operation, the B-address is also placed in the E-address register (for E-channel operation), or the F-address register (for F-channel operation).

I-10 Time: If the command specifies unoverlap operation, the computer is interrupted (disabled) at I-10 time if the other channel is executing an I-O operation. In other words, an unoverlapped operation cannot be started if an overlapped operation is in process. The computer is kept disabled only until the channel in process completes its operation.

I-11 Time: The d-character reads out and is set into the op modifier register. Because of overlapped operation, op mod register, op register, and the I-O channel select register must be free to accept characters of the next instruction word. Therefore, the information in these registers must be stored in the channel control latches. During I-11 time, the W in the op mod register gates the set of the output mode latch (E-channel), or the write latch (F-channel). The output of the latch lights the write indicator, for that channel, on the 1415 console. The output mode latch also gates the assembly channel to E-1 input, and switches with E-cycle or F-cycle (ALD 13.60.06) to produce "output cycle." Output cycle brings up regen memory and also conditions the B-channel and assembly controls. If no W (or X) is present in the op modifier register, "output mode to buffer" does not become active, and a channel not ready indication occurs (Figures 102 and 103).

I-12 Time: I-12 is the last instruction read-out cycle, during which the channel move or channel load latch is set according to the character in the op register. The status sample pulses are generated during I-12 time.

Last Execute Cycle: During the last instruction read-out cycle of an overlapped command, "last execute cycle * I-O" becomes active, gating the set of the I-cycle control latch (Figure 120).

Status Sample A: This pulse occurs at logic gate D of I-12 time, and samples the A-status buses. Condensed logic, Figure 101, shows generation of the status sample pulses.

Status Sample A Delay: This pulse occurs at logic gate E of I-12 time and samples the output of the channel status indicators. If any status indicators are on at status sample A delay time, the operation is terminated (no E-phase) and the program proceeds to the next sequential instruction (Figure 120).

I-Phase Channel Status Indicators

Channel status indicators that can be set at the end of I-phase (status sample A time) are referred to in this manual as A-status indicators. For an M%2 op code, the A-status indicators (Figure 87) for the printer are:

Not Ready	(Requires manual intervention)
Busy	Printer is unloading the buffer (printing a line)

Condition Error detected during printing of line from a previous command

Not Ready: Figures 102 and 103 show the printer status gated to the CPU by "select unit 2." In CPU, "buffer ready" is gated to the channel ready bus by "E-channel select any buffer." With the ready bus active, the input to the channel not ready latch is blocked, preventing the status sample A pulse from turning on the latch.

Busy: Figures 102 and 103 show the printer busy status gated to the CPU by "select unit 2." If the printer is busy, the channel busy bus becomes active, AND'ing with "E-channel ready bus" and "status sample A" to set the channel busy indicator.

Condition: This indicator is set for one of two types of errors that may result from print commands: "latent" errors set the channel condition indicator and "immediate" errors set the channel data check indicator (described later). Either type of error sets the transfer and print error latch (ALD 53.12.01) in the 1414 synchronizer. A latent print error is any error resulting from a print command where the error is not detected by the CPU until another print command is given. In the following program, for example, assume that a latent error results from the command to print record A.

00001	M%2003000W	Command to print record A
00011	R000012	If busy, try again
00018	R010008	Branch to 01000 if channel condition indicator on
00025	R02000≠	Branch to 02000 if any channel indicator on
(processing routine)		(Record A is printed while CPU proceeds with program)
00101	M%2004000W	Command to print record B
00111	R001012	If busy, try again
*00118	R010008	Branch to 01000 if any channel indicator on
01000	05000	Halt

*At this point, the CPU detects the latent error that occurred as a result of the command to print record A, and the program branches to 01000. Assume a halt at 01000. The command to print record B is not executed.

When the channel condition indicator is set, the CPU generates reset select buffer latches to turn off the transfer and print error latch in the 1414 synchronizer (Figure 112). This permits the next print command to be executed (if no status indicators are set at status sample A time).

A channel condition indication (Figure 104) may be caused by any of the following errors:

- Buffer clock error
- Syn check
- C-Bit check (buffer parity error)
- Print line complete error
- Print equal compare error
- Hammer fire check
- Delay error (printer to buffer timing error)
- Print control error (hammer reset error)

For additional information on printer errors, see the *1414 Input-Output Synchronizer*, Customer Engineering Instruction-Reference Manual, Form 223-2590.

The output of the transfer and print error latch is gated to the CPU during I-phase of the printer command, the channel condition indicator is set at status sample A time, and the command is not executed. CPU acknowledges the error indication by AND'ing "E Ch condition" with "E Ch select any buffer" at status sample A delay time to generate "reset select buffer latches" (Figure 112). This line becomes "reset CPU" in the 1414 synchronizer and resets the transfer and print error latch, permitting the next print command to be executed.

If no status indicators are set, "status sample A delay" turns on one of the four channel in process latches, according to the character in the I-O channel select register (Figure 62).

Percent sign	%	E-channel unoverlap in process
Commercial at	@	E-channel overlap in process
Asterisk	*	F-channel unoverlap in process
Lozenge	◻	F-channel overlap in process

Each latch has an indicator on the 1415 console. If the print command specifies overlap, the CPU proceeds with the next sequential instruction after setting a channel in process latch. If any status indicator was turned on, the CPU does not execute the print command and proceeds with the stored program.

E-Phase Sequence

During E-phase, the CPU transfers characters from core storage to the I-O channel on request from the channel controls. Use Figures 59 and 62 to follow the data transfer operation.

Channel In Process Latch: With no status indicators on at the end of I-phase, one of the four channel in process latches is turned on. "E Ch in process" AND's with "not E-1 reg full" and other conditions (Figure 62) to bring up "E-cycle required," causing an E-cycle that brings the first output character from core storage to E-1. At this point, the E-2 full latch is off and the character transfers from E-1 to E-2. During this E-cycle, the E-channel ready latch (not the channel status indicator) is turned on, bringing up "ready to buffer" which initiates buffer operation. The CPU takes another E-cycle to fill E-1.

E-Channel Ready Latch: The output of the latch, "ready to buffer" brings up "ready 2" in the 1414 synchronizer. "Ready 2" AND's with "select unit 2 powered," "ready for CPU transfer," and the off output of the read latch to turn on the read trigger. See the appropriate condensed logic diagram in the *1414 Input-Output Synchronizer*, Customer Engineering Instruction-Reference Manual, Form 223-2590.

Read Trigger: The output of the trigger, called read in, turns on the print buffer ring advance triggers, initiating a print buffer read in operation. "Trans scan" is active during the read in operation.

Strobe Latch: At 020-030 time of the first buffer cycle the buffer strobe latch turns on to gate every 100-000 time pulse to CPU as "buffer strobe." The strobe latch is turned off when trans scan falls at the end of scan.

Channel Operation: During each buffer cycle, the character on the channel output lines is written into the print buffer. A strobe signal generated by the synchronizer causes the channel controls to set the next output character into E-2. The character transfers from the E-1 register to the E-2 register under supervision of the register transfer and data flow controls. An E-cycle is taken to bring a new character from core storage to E-1 (Figure 62).

Unoverlapped Operation: The CPU is idle (logic clock ring is disabled) except when the channel controls request the CPU to take an I-O data cycle (E-cycle) to transfer an output character from core storage to E-1 (Figure 119).

Overlapped Operation: At the end of I-phase of the print command, the CPU proceeds with the next sequential instruction. Processing (computing) continues until the channel controls request the CPU to take an I-O data cycle to transfer a character from core storage to E-1. Computing is interrupted (disabled) while the CPU brings a new output character to E-1. Computing is then resumed (Figure 118).

External End of Transfer Trigger: Once the buffer operation is initiated, the operation continues until all 132 buffer positions (IBM 1403 Model II) have been written with data from the channel output data lines. The synchronizer signals CPU at the end of buffer operation by generating "buffer end of transfer" which turns on the external end of transfer trigger in the CPU (ALD 51.40.12 and 13.42.11). If the ready bus becomes inactive during a buffer transfer operation, the external end of transfer trigger is turned on immediately. If an early GM-WM prematurely terminates transfer of output characters, the remainder of the buffer is filled with the last output character, which remains in E-2.

Internal End of Transfer Latch: A GM-WM in the output field, or a core storage wrap-around condition, turns on the internal end of transfer latch, blocking the CPU from taking any more I-O data cycles. With the GM-WM correctly positioned in the output field, the internal end of transfer trigger is turned on before the external end of transfer latch. "External end of transfer" forces "internal end of transfer" when no GM-WM appears in the output field (Figure 101).

Status Sample B Trigger: With both the external end of transfer trigger and the internal end of transfer latch

on, the status sample B trigger is turned on at the end of the last I-O data cycle (E-cycle). The trigger is on for two clock pulses and the output of the trigger is used to set the B-status channel indicators. (Figure 101).

Second Sample B Trigger: This trigger is turned on the next 1st clock pulse after the status sample B trigger is turned on. The trigger is on for two clock pulses and the output of the trigger samples the outputs of the B-status indicators.

Status Sample B Delay Trigger: This trigger is turned on the next 1st clock pulse after the second sample B trigger is turned on. The trigger is on for two clock pulses and the output of the trigger resets the channel in process latch.

E-Phase Channel Status Indicators

Channel status indicators that can be set at the end of E-phase (status sample B time) are referred to in this manual as B-status indicators. The B-status indicators for the printer are:

Data Check	Figure 104 (condensed logic)
Wrong Length Record	Figure 105 (condensed logic)

See also the status indicator chart, Figure 88.

Data Check: This indicator is set if one of two errors occurs during a CPU to buffer transfer: parity error in the print buffer or a buffer clock error. The transfer or print error latch (53.12.01) is turned on by either of these errors, and the output of the latch is sampled at status sample B time. No printing occurs if the data check indicator is set.

Wrong Length Record: A GM-WM must be positioned in the output field so that exactly 132 (or 100) characters are transferred from the CPU to channel or a wrong length record (WLR) indication occurs. During load mode operation, WM and WS characters must be considered when computing the number of output characters. No printing occurs if the WLR indicator is set (Figure 105). See "channel status indicators" in the I-O Principles of Operation section.

Correct Transfer To Buffer: If neither the channel wrong length record or channel data check indicator is turned on at status sample B time, "correct trans to buffer" is sent from the CPU to the 1414 synchronizer. "Correct trans to buffer" ("go" in the 1414) AND's with "select unit 2 powered" and "ready for forms or print" to turn on the scan call trigger. Scan call (ALD 53.40.01) initiates a print operation. Note that the record is not printed if a channel WLR or a channel data check occurred (Figure 112).

Reset Select Buffer Latches: If a buffer clock or a buffer data error occurs during a CPU to buffer transfer, transfer or print error latch is set, sending "buffer error" to the CPU. "Buffer error" gates the turn on of the channel data check indicator at status sample B time. The CPU acknowledges the buffer error by gen-

erating "reset select buffer latches" ("reset CPU" in 1414) at second sample B time. The "reset CPU" line resets the transfer and print error latch, preventing a false error indication on the next CPU to buffer transfer (Figure 112).

Following a correct transfer to buffer, the print operation begins. While printing, any error sets the transfer and print error latch. As a result "buffer condition" is gated to CPU during I-phase of the next print command. Status sample A sets the channel condition latch, and status sample A delay sends "reset select buffer latches" to the 1414 synchronizer, acknowledging the error. The command is not executed, but the "reset CPU" line turns off the transfer and print error latch, permitting the next command to be executed (if no indicators are turned on).

Last Execute Cycle: E-channel status sample B AND's with "E-channel unoverlap in process" to set the I-O last execute cycle latch which gates the turn on of the I-cycle control latch. "Status sample B delay" resets the "E-channel unoverlap in process" latch. See Figure 120.

Printer Forms Control Command

Instruction format: Fd (E-Channel) Mnemonic: CC
2d (F-Channel) CC

This op code causes the 1403 printer carriage to take a single, double, or triple space; or skip to the next hole in a designated tape channel. The spacing or skipping can be executed immediately or after the next print command is executed. If printing is taking place when the forms command is initiated, the carriage operation is delayed until the line is printed. If an after-print forms command is given, the carriage operation is delayed until after the next line is printed.

The zone bit configuration of the d-character determines the type of operation:

No zone bits	Immediate skip
B-bit	Immediate space
A-bit	Space after print
A- and B-bits	Skip after print

The numeric bit structure of the d-character indicates the channel hole to stop a skip operation or the number of spaces to take on a space operation (1, 2, or 3 spaces). See Figures 63, 64, 65, 66, and 120.

I-Phase Sequence

An F in the op register brings up the following op code grouping lines to control the operation:

- Not Addr Dbl Op Codes 13.14.14
- 2 Char Only Op Codes - 13.14.12
- No Branch Op Codes - 13.14.04
- Op Mod to A-Ch on B Cy Ops - 13.14.07
- Regen Mem on B-Cy Op Codes 13.14.08

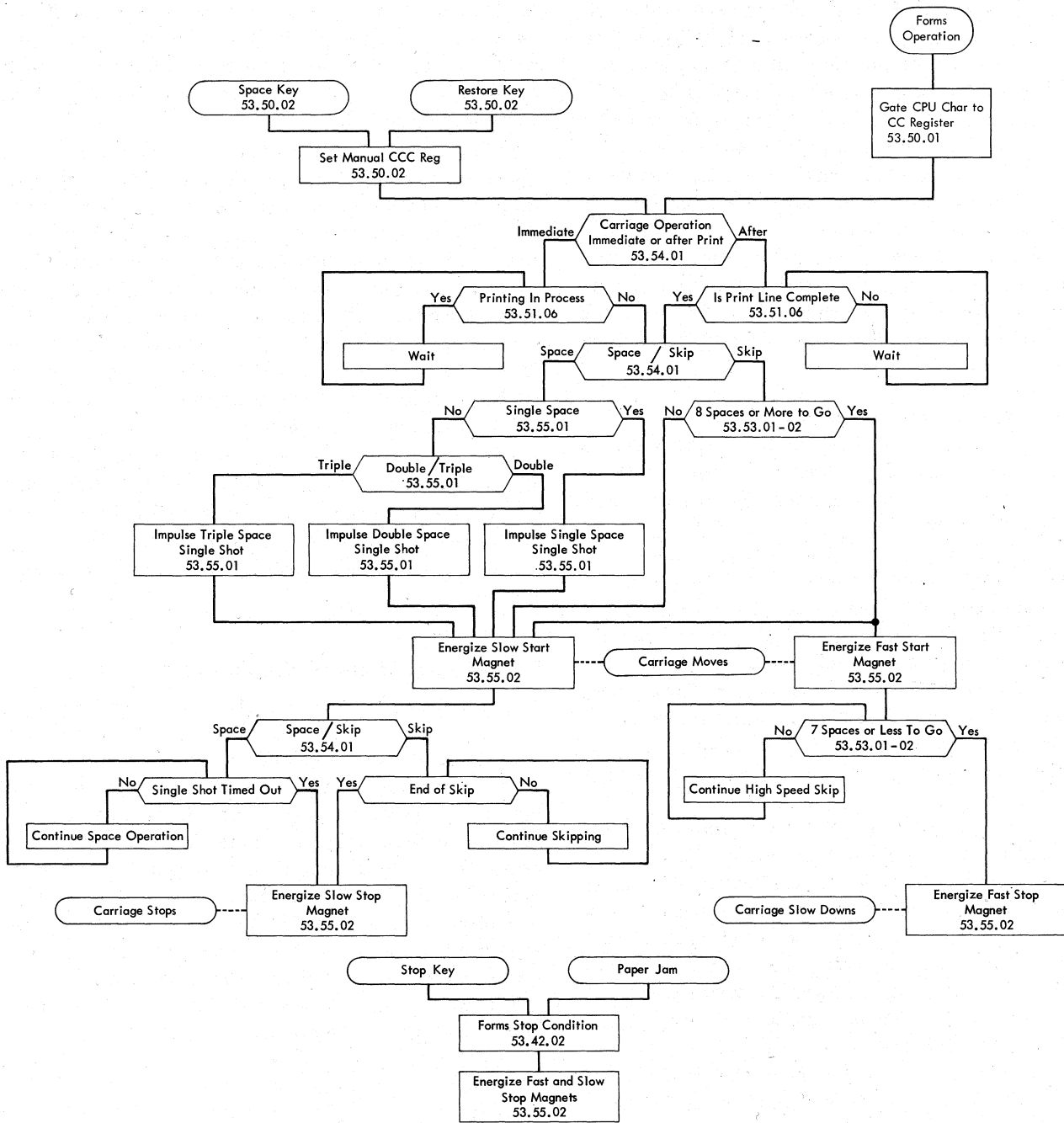
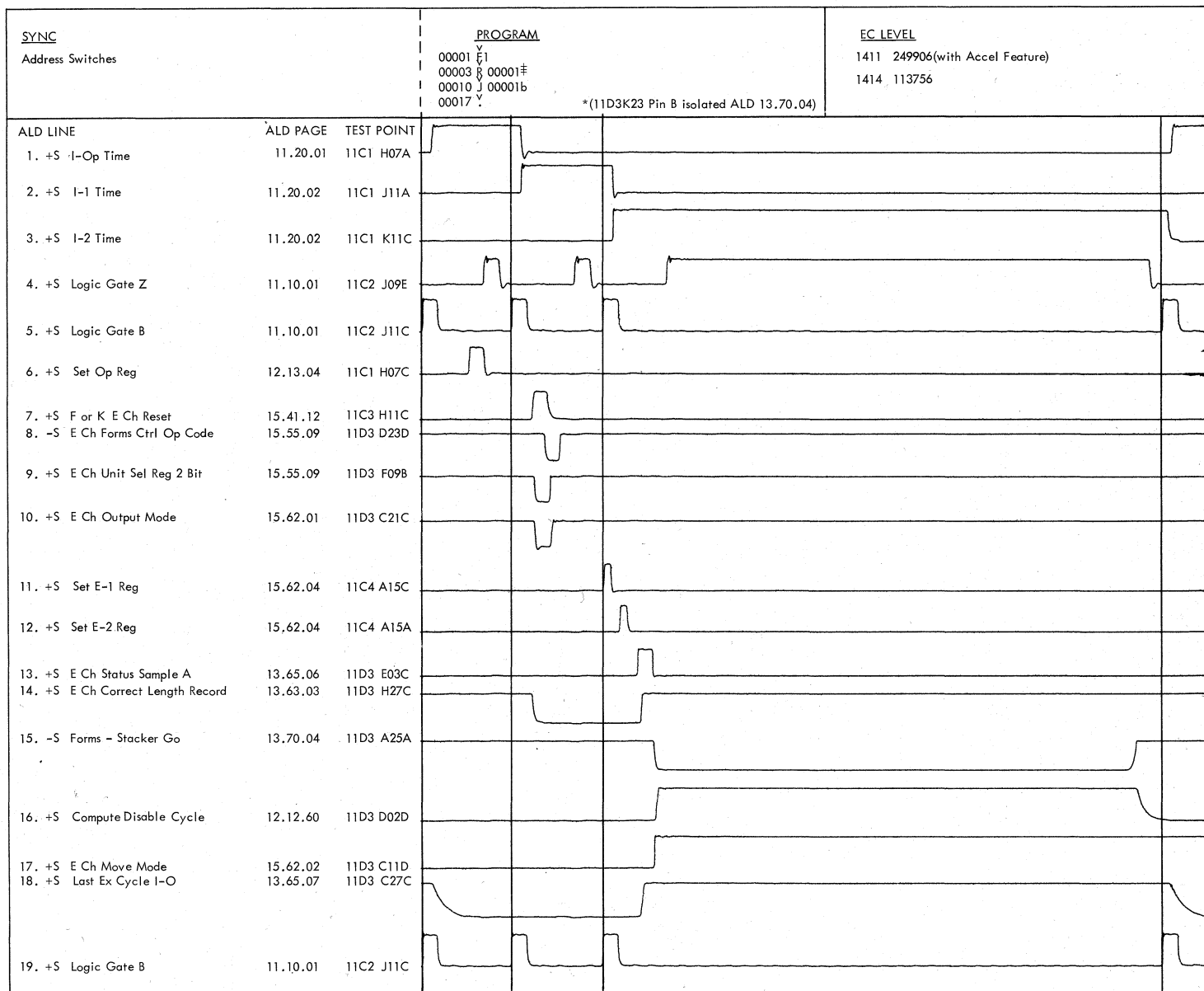


Figure 63. 1411-1403 Printer Forms Control Logic Flow



*Prevents "forms-stacker go" signal to 1414, providing a stable scope trace

Figure 64. 1403 Forms Control Timing Chart

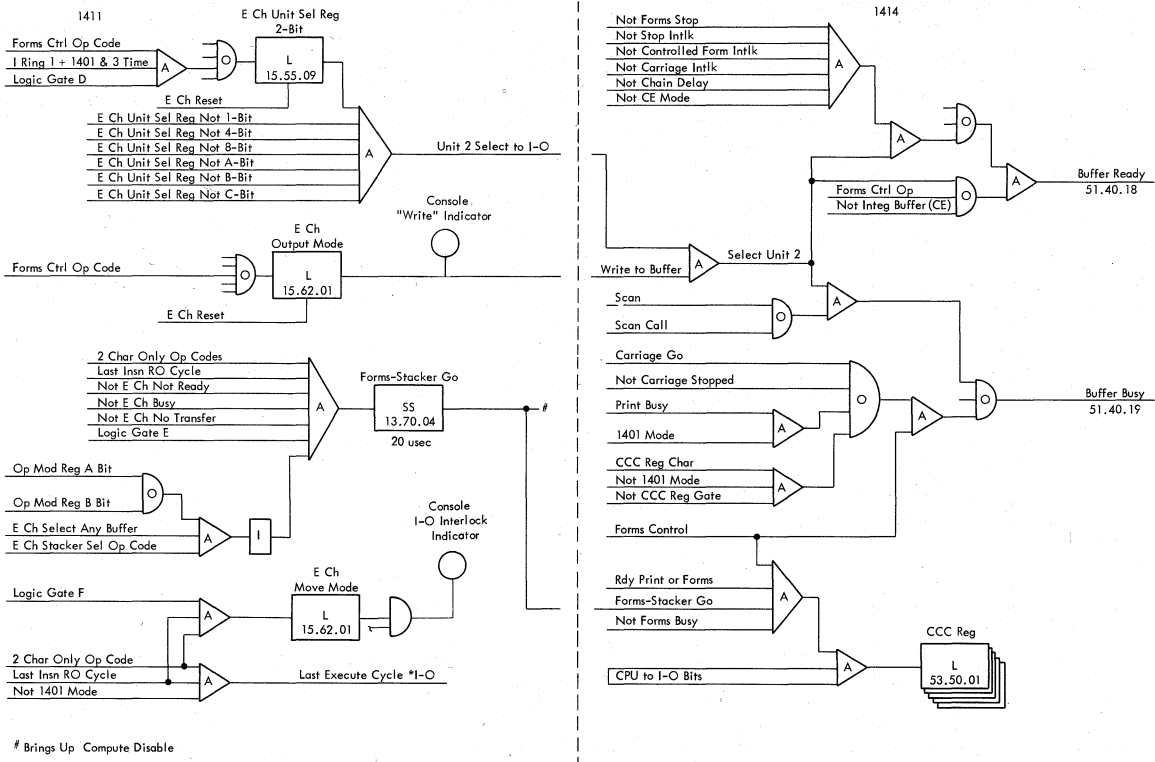


Figure 65. 1411-1403 Printer Forms Control – Condensed Logic

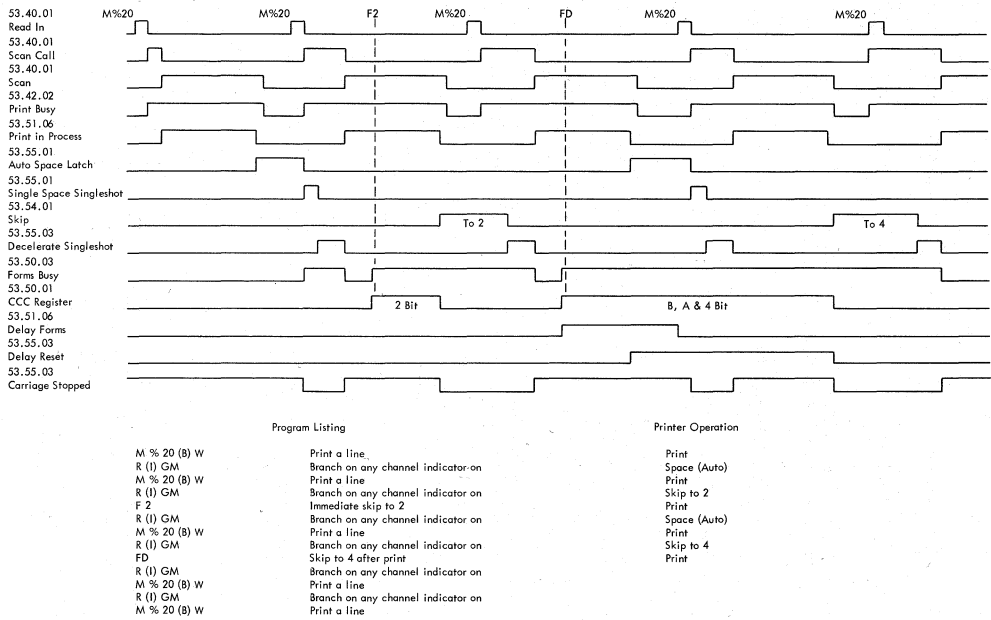


Figure 66. 1403 Printer Carriage Sequence Chart

I-Op Time: The op code character (F) reads out and is set into the op register, bringing up the op code grouping lines and the "forms control op code" line. The channel interlock is tested to assure that the stored program has checked the channel status indicators since the last command to the channel. If the inter-

lock is on, "master error" stops the CPU with the I-O Interlock indicator glowing (red) on the 1415 console. Forms control op code sets the E-channel output latch which is used to gate the printer and carriage status to CPU.

I-1 Time: An E-channel reset is generated (Figure 17) and a 2 is set into the unit select register (Figure 65). The output of the unit select register switches with the output of the E-channel output mode latch to generate select unit 2 in the 1414 synchronizer. Select unit 2 gates the printer and carriage conditions to the E-channel status buses. The d-character is set into the op-modifier register and into the A-data register and gated to the input of E-1. At the end of I-1 time, "logic gate early B or S" sets the forms control character into E-1 from the assembly channel. Normal register operation transfers the character to E-2 and it appears on the channel output data lines.

I-2 Time: The A-status buses are sampled at status sample A time and if no channel status indicators have been set the command is executed by triggering the forms-stacker go single shot (Figure 65). The output of the single shot causes the forms control character on the channel output lines to be set into the ccc register where it is decoded to determine the type of carriage operation to be performed. The single shot also generates compute disable to interlock cpu for twenty microseconds to prevent the conditioning lines from falling. "Last execute cycle * I-O" is generated on the last instruction read-out cycle and the Fd command is terminated whether or not the command is executed. The channel move mode latch is turned on to provide the channel "interlock" which forces program interrogation of the channel status indicators prior to another channel command.

I-Phase Channel Status Indicators

No status sample B time occurs because there is no E-phase. Therefore no E-phase, or B-status, channel indicators are used. The I-phase, or A-status, channel indicators for a Fd command are:

Not Ready	Printer not ready, chain not running, out of forms, etc.
Busy Condition	Previous carriage operation in progress Not used

If either the E-channel not ready or the E-channel busy latch is on, the Fd command is not executed. Failure to execute is detected by a subsequent command testing the channel indicators (Figure 102).

Branch If Printer Carriage Busy Command

Instruction format: J (I) R Mnemonic: BPCB

This test and branch command is used to determine whether the printer carriage is busy or not. It may be used to assure that the carriage is stopped before a test is made of the carriage channel 9 or channel 12 (overflow) indicators.

Without the use of this command there are two possible errors that can occur in a program:

1. A carriage channel 9 or channel 12 indication may be missed, or detected at different times in the program.
2. A second detection of a channel 9 or channel 12 indication may occur. (The overflow indicator may still be on when the second overflow indicator test is made.)

Assume the following program:

Proc	BCV	Skip	Processing (time variable)
	CC	S	Branch if overflow indicator on
	BA1	Error	Double space after print
Print	W	Printout	Error test
	BA1	Error	Error
	B	Proc	Branch to processing
Skip	CC	A	Skip to 1 after print
	BA1	Error	Error test
	B	Print	Branch to print

If the processing time is very short, the overflow test could come before the double space after print is complete (carriage busy). During the completion of the double space a channel 9 or channel 12 (overflow) could be encountered and the overflow condition would not be detected until after another line is printed.

Now add a branch if printer carriage busy BPCB command to the program:

Proc			Processing (time variable)
Spin	BPCB	Spin	Loop, if carriage busy
	BCV	Skip	Branch if overflow indicator on
	Remainder of program is the same		

With this addition, if the processing time is very short, the BPCB command causes a branch back to itself as long as the carriage is busy (moving). The program advances normally when the carriage is no longer busy.

1411-1011 Paper Tape Reader Operation

The IBM 1011 Paper Tape Reader is used in conjunction with the 1414 synchronizer to provide a buffered paper tape input to the IBM 1411 CPU.

Paper Tape Reader Move or Load Command

Instruction format: O XXX BBBB R

The paper tape (PT) reader move or load op code transfers the contents of PT storage to the CPU. The move op code transfers the data exactly as it appears in PT storage. If the instruction is given in the load mode, a single word separator character from PT storage causes a word mark to be placed over the next character that is read into CPU. Two successive word separator characters from PT storage cause a single word-separator character to be placed in core storage in the CPU.

I-Phase Sequence (Figure 67)

Details of I-O instruction read-out are presented in the I-O Sequence section. See Figure 34. Instruction read-out causes the instruction word characters to be placed in various registers to control the execution of the PT reader op code.

M or L in the op register brings up the following op code grouping lines:

- M or L Op Codes
- Percent Type Op Codes
- Address Type Op Codes
- Two Address Op Codes
- 2 Addr Plus Mod Op Codes
- No Index on 1st Addr Op
- No Branch Op Codes
- Not Addr Dbl Op Codes

I-Op Time: The op character reads out and is placed into the op register (Figure 67, Sheet 1), bringing up the necessary op code grouping lines. An M in the op register specifies move mode; an L specifies load mode.

I-1 Time: The I-O channel select character reads out. The I-ring advances to I-3, and the channel select character is placed into the I-O channel select register.

I-3 Time: The I-O channel interlock test is made to see if the stored program has interrogated the channel status indicators since the last channel command for the selected channel. The check is made by testing the move or load latch. A satisfactory interrogation of the channel status indicators resets the move or load latch for that channel and they should be off at I-3 time. If either latch is on at I-3 time the I-O interlock

check indicator (on the 1415 console) is turned on, master error becomes active and the CPU stops.

I-4 Time: The unit select character reads out and is placed in the channel unit select register. Unit select character P gates the PT reader status to the CPU. A channel reset is developed to reset the control and status indicator latches for the associated channel.

I-5 Time: Unit number character 0 reads out and is placed into the channel unit number register.

I-6 through I-10 Time: The B-address reads out and is placed in the B-address and D-address registers. If the command specifies overlap operation the B-address is also placed in the E-address register (for E-channel operation).

I-11 Time: The d-character reads out and is set into the op modifier register. For the PT reader op code, the d-modifier character is an R to specify a read (input) operation.

I-12 Time: This is the last instruction read-out cycle. If this command is overlapped, the op register, the op mod register and the I-O channel select register must be free to accept the characters of the next instruction word. The information in these registers is translated and stored in the channel move or load latch, and the input latch to control the execution of this I-O command and the registers are freed for the following instruction.

Status Sample A: This pulse is developed to sample the channel-status buses and set the channel status indicators to reflect the PT reader status. If the PT reader is not ready, the channel not-ready indicator is set. If the PT reader is busy, the channel-busy indicator is set.

Status Sample A Delay: If either indicator has been set, the CPU does not execute the instruction, but proceeds to the next sequential instruction. If no indicators have been set, the status sample A delay pulse sets either the overlap in process or the unoverlap in process latch and the PT storage is conditioned to send its contents to CPU by a request for a PT read transfer scan. When the scan request is granted, the PT storage reads out, and sends PT storage characters to CPU.

E-Phase Sequence (Figure 67)

During each PT storage cycle, a character reads out and is sent to the CPU, where it is set into the E-1 data register. Transfer of the character from E-1 to E-2 is controlled by the word-separator control circuit. If the instruction is given in the load mode, a single word-

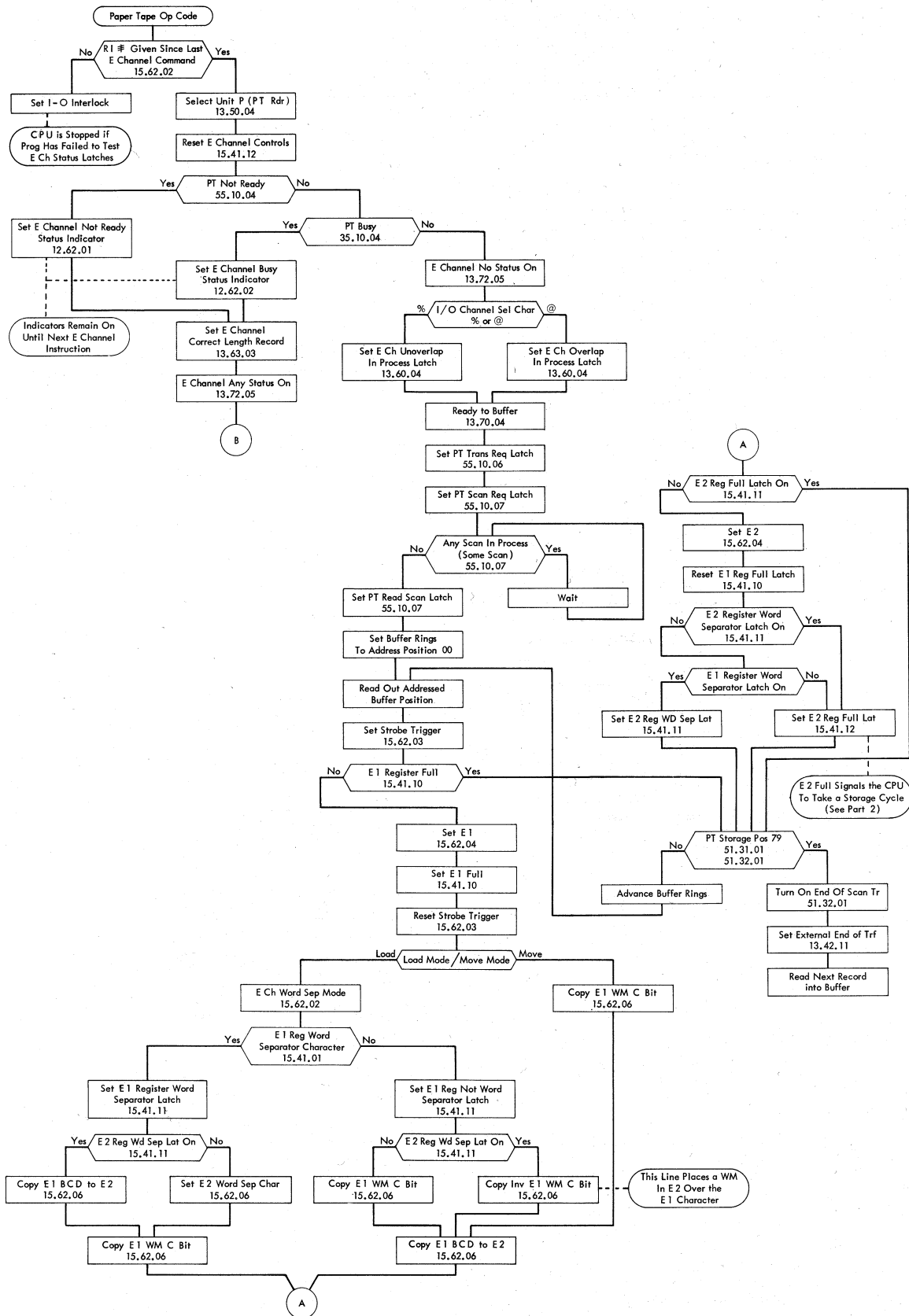


Figure 67. Paper-Tape Move or Load (Sheet 1 of 3)

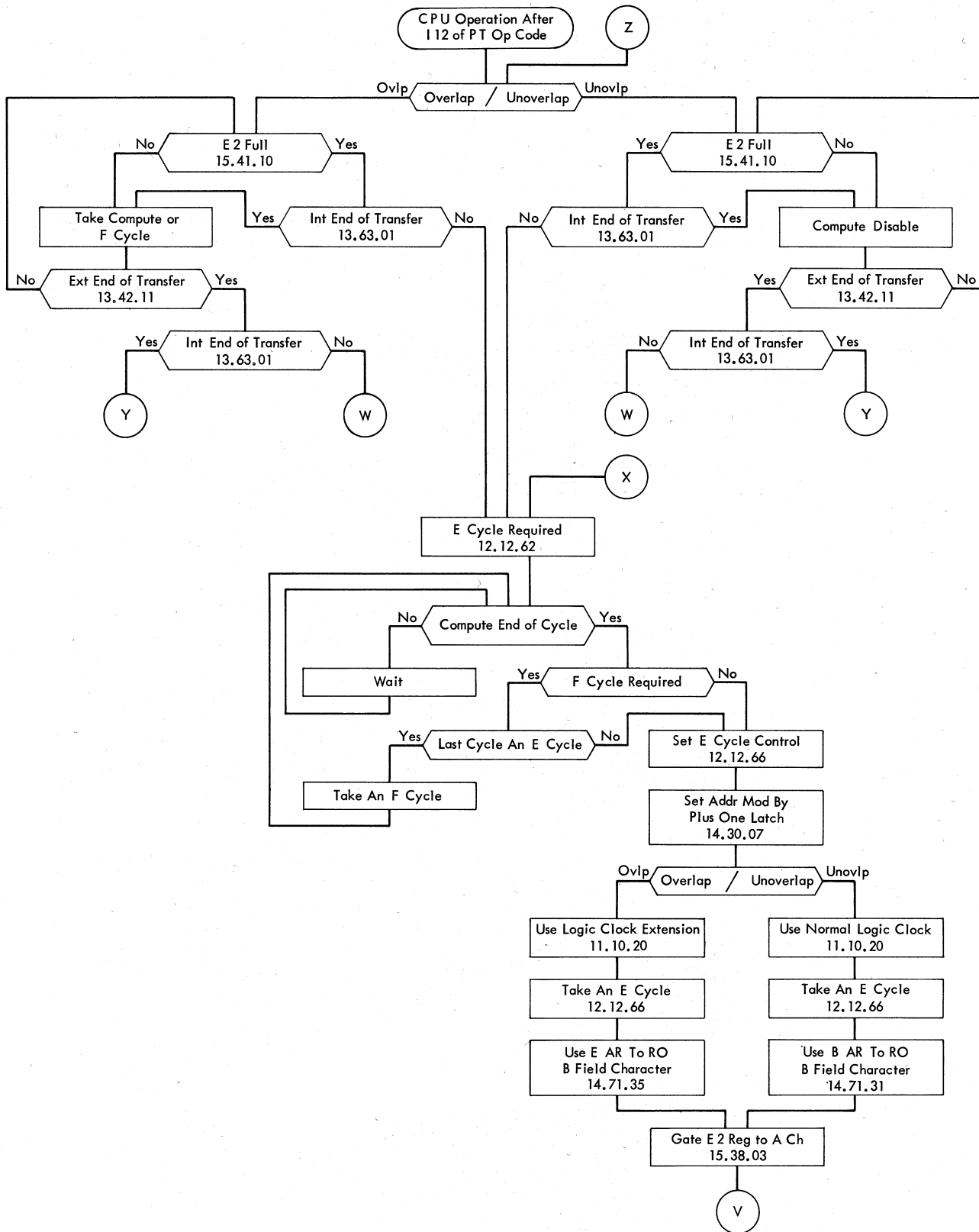


Figure 67. Paper-Tape Move or Load (Sheet 2 of 3)

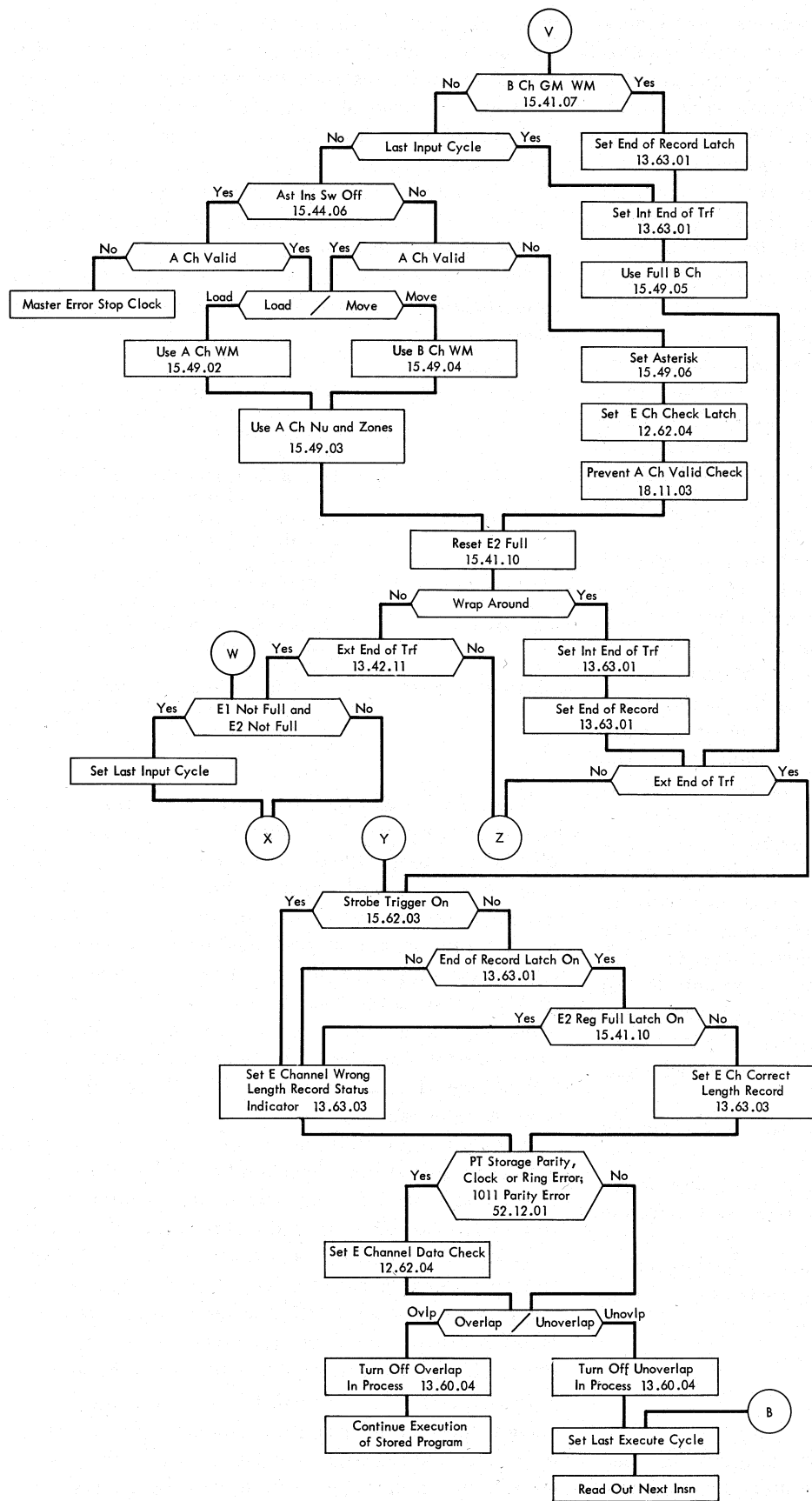


Figure 67. Paper-Tape Move or Load (Sheet 3 of 3)

separator character from the reader places a word mark over the following character. A pair of word-separator characters causes a single word-separator character to be written in storage. If the instruction is given in the move mode, a word-separator character from PT storage is stored as a word-separator character in the CPU.

If the command is unoverlapped, the CPU takes an E-cycle only when necessary to store the E-2 character. During the time E-2 is not full, the CPU is disabled. If the command is overlapped, the CPU stores the E-2 characters with E-cycles and continues to process subsequent instructions during the time E-2 is not full.

Once the read-transfer scan is initiated, the PT storage-scan circuitry runs continuously to read out each position of PT storage and send it to the CPU. The transfer continues until all 80 positions of the PT storage are transferred. As each PT storage character reads out, a control bit (LY core plane) is placed in that position in preparation for the next PT read in.

When a group mark with a word mark is detected in a storage position, or if a wrap-around condition is detected, the internal transfer is ended and the CPU waits for the external end of transfer. If the external end of transfer is detected before the internal end of transfer, an extra cycle is taken after the E-1 and E-2 data registers are emptied to search for the group mark with a word mark. During this last input cycle, the internal end of transfer is forced whether or not the group mark with a word mark is detected.

Status Sample B: With both the external end of transfer and the internal end of transfer complete, the status sample B pulse tests for transfer errors and whether or not the record length was correct. Any PT storage error during the transfer causes the channel data-check status indicator to be turned on. A wrong length record causes the channel wrong-length record status to be turned on. A parity error in the 1011 PT reader (8 channel tape only) also causes the channel data-check indicator to be turned on.

Second Sample B: This pulse is used to sample the outputs of the B-status indicators.

Status Sample B Delay: This pulse resets the "channel in process" latch and the CPU is released to continue with the stored program.

As soon as the transfer is complete, the PT storage circuitry sends a "go" signal to the PT reader to cause the next record to be loaded into PT storage.

Buffer Operation

The 1414 integrated synchronizer (Figure 68) can have eight 80-position core storage units. One of these storage units can be assigned to the paper tape reader. Eighty characters for the PT reader are stored in the

PT storage unit. When the unit is filled, the contents can be transferred to the CPU. PT storage has eight planes; seven planes store the characters in BCD form, the eighth, or control plane, (LY) locates the storage position for incoming characters. PT storage uses the same addressing system, data register, and clock as the other integrated synchronizer storage units.

When used with the integrated synchronizer, the PT reader uses the circuitry assigned to option 4.

There are 13 lines that connect the 1011 and the 1414 synchronizer for control. The names and functions of these lines are:

LINE	FUNCTION
Paper tape ready	Output line from the 1011. Indicates that power is on, that tape is properly loaded, and that the start key was pressed.
PT parity error	Output line from the 1011. Indicates an 8-channel tape parity error.
End of record	Output line from the 1011. Indicates that the end of record character was detected.
Data output (7 lines)	Output lines from the 1011 output data register (register B).
Data sync	Output line from the 1011. Indicates that a character is present on the data output lines.
Character received	Input line to the 1011. Indicates that the character on the data output lines was received and stored.
Go	Input line to the 1011 that requests a character.

Paper-Tape Read-In (Figure 69): Paper tape read in is initiated by the "go" signal from the 1414 synchronizer. The go signal is generated with a power-on reset, or after a read transfer scan takes place. When the 1011 receives the go signal, the drive mechanism is set in motion, and as each character becomes available at the output bit lines, a data-sync pulse is sent to the paper-tape storage circuitry. The data-sync pulse requests a serial scan to store the incoming character. Requesting the scan gates the character into a data register, and then signals the 1011 that the character is received.

After priority conditions are satisfied, a scan is initiated to locate the first blank position. When the correct position is located, the character is stored and the rings reset. After 80 data-sync pulses are received, or if the 1011 signals an end of record, the go line is dropped to stop paper tape reading. These conditions also reset the paper tape busy latch to allow a paper tape read transfer instruction to be executed. Figure 70 shows the relative timings involved in storing a character.

Input-Serial-Scan Control: Once the go signal is received, the PT reader sends a character to PT storage every two milliseconds. Each time a character is received, the addressing rings locate the next storage position in sequence. The character is stored and the rings reset. As soon as the rings reset, they can be used

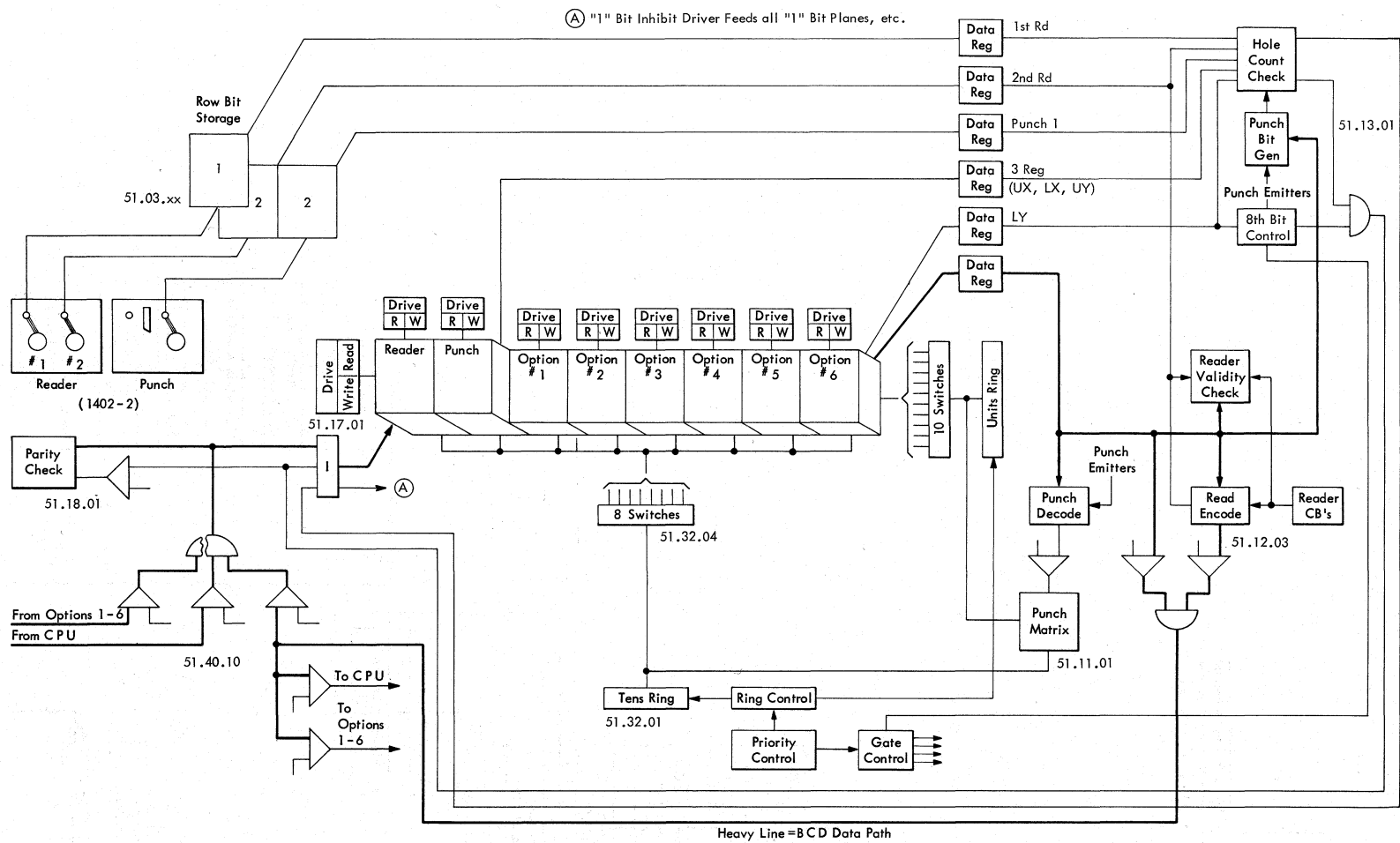


Figure 68. IBM 1414 Integrated Synchronizer Data Flow

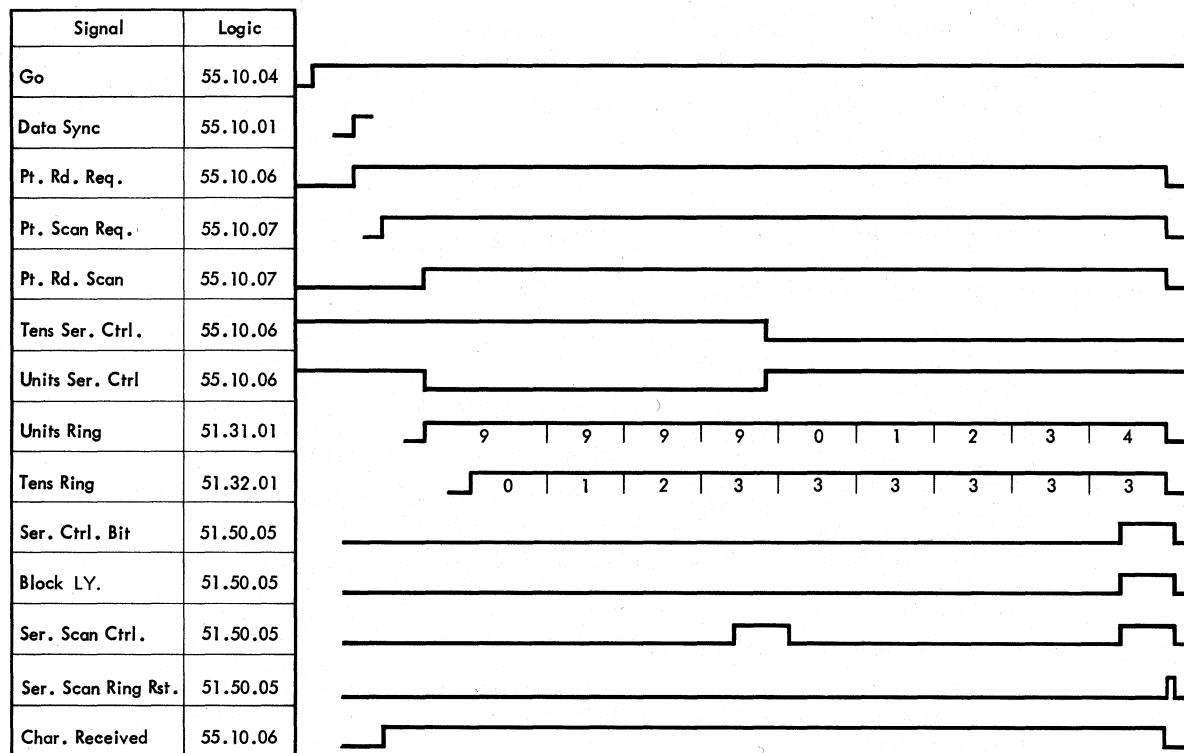


Figure 70. Paper-Tape Character Storage

to scan other storage units until the next PT character is received.

PT read in begins with all 8-bit (LY) cores set ON. When a character is written into a PT storage position the corresponding LY core is set OFF. For example, assume a PT read in is in process and positions 1 through 33 have characters in them with their corresponding LY cores off. Positions 34 through 79 have the LY cores on. A data-sync pulse from the PT reader requests a serial scan (Figure 70). The scan starts with the rings addressing position 09. Position 09 reads out, and because there is no LY bit, the character is regenerated. The tens ring advances and position 19 reads out. Again there is no LY bit and that character is regenerated. The tens ring advances and position 29 reads out. Again there is no LY bit and that character is regenerated. The tens ring advances to address position 39. When position 39 reads out a LY bit is detected. This indicates that the desired position is somewhere between position 30 and 39. The tens ring is prevented from advancing and the units ring is allowed to advance to address and read out positions 30, 31, 32, and 33 before the next LY bit is detected. When position 34 reads out, the presence of the LY bit brings up the gate that allows the incoming character to be written into this position during the write portion of

the storage cycle. The LY control bit is not regenerated in order to indicate that this position is filled. The rings are reset and the PT storage circuitry waits for the next data-sync pulse.

Circuits

Common op code grouping lines are:

- Percent type op codes
- Not addr dbl op codes
- 2 Addr plus mod op codes
- 2 Address op codes
- Address type op codes
- No-index on 1st addr ops
- No-branch op codes
- M or L op codes

SIGNAL	CONTROL	LOGIC
1. Set the E-channel not-ready indicator, if the PT reader is not ready.		
(Not) PT ready	(Not) PT ready to adapter	55.10.01
PT rd not ready	(Not) PT ready (or off-line CE mode)	55.10.02
PT rd op	Select unit P	55.10.04
(Not) 14C5-A rdy status	Read from buffer	
	PT rd not ready	55.10.04
	PT rd op	
(Not) Buffer ready	(Not) 14C5 rdr status	51.40.18
(Not) E-ch ready bus	(Not) buffer ready	12.62.01
	E-ch sel any buffer	

SIGNAL	CONTROL	LOGIC
E-ch status sample A	M or L op codes I-ring 12 time (not) E-ch sel unit F I-cycle percent or coml at (not) File op Logic gate D	13.65.06
E-ch not ready	E-ch status sample A (not) E-ch ready bus	12.62.01

2. Set the E-channel busy indicator, if the PT reader is busy.

Busy	End PT scan or PT busy or PT rd req	55.10.04
14C5-A busy status	Busy PT rd op	55.10.04
Buffer busy	14C5-A busy status	51.40.19
E-ch busy bus	Buffer busy	12.62.02
E-ch busy	E-ch select any buffer E-ch status sample A E-ch ready bus E-ch busy bus	12.62.02

3. If any status indicator is ON, go to the next instruction.

E-ch correct length record	Set E-ch busy or Set E-ch not ready	13.63.03
E-ch any status (on)	E-ch correct-length record	13.72.05
Last execute cycle I/O	E-ch any status (on) Last insn RO cycle (not) File op I/O percent latch	13.65.07
Last execute cycle	Last execute cycle I/O	12.12.51

4. Initiate a PT read-transfer scan.

Ready to buffer	(not) Clock stopped E-ch in-process E-ch select any buffer E-ch input mode	13.70.04
Ready	Ready to buffer	51.40.04
PT rd trans	Ready PT rd op	52.10.09
Gate on PT scan req	PT rd trans	55.10.06
PT scan req	Gate on PT scan req Time 080-090	55.10.07
PT rd scan	PT scan req (not) Same scan Time 030-040	55.10.07

5. Read out the addressed PT storage position.

Time Pl 1 latch (on)	Opt no 4 scan (not) Single cycle mode	51.30.02
Time Pl 2 latch (on)	Time Pl 1 latch (on) Time 000-010	51.30.02
Timing pulse gate	Time Pl 2 latch (on)	51.30.02
Rd pulse L latch (on)	Time 000-010 Not clock 2	51.30.05
Rd pulse L latch (off)	Time 040-050	51.30.05
Rd pulse S latch (on)	Time 010-020	51.30.05
Rd pulse S latch	Time 040-050	51.30.05
Read pulse 1 010-040	Rd pulse S latch	51.30.05
Read pulse 2 005-040	Timing pulse gate Rd pulse L latch Timing pulse gate	51.30.05

6. Set the strobe trigger.

Trans scan	14C5-A trans scan	51.40.40
Strobe latch	Trans scan Time 020-030	51.40.43

SIGNAL	CONTROL	LOGIC
I/O to CPU trans	Trans scan	51.40.40
Buffer strobe	Read from buffer I/O to CPU trans Time 080-090 Strobe latch	51.40.43
E-ch strobe trigger	Buffer strobe E-ch select any buffer	15.62.03

7. Set E-1 register; set E-1 full latch; reset the strobe trigger.

Set E-1	2nd clock pulse E-ch strobe trigger E-ch input mode (not) E-1 reg full	15.62.04
E-ch strobe trigger (off)	E-ch input mode Set E-1 reg	15.62.03
E-1 full	Set E-1	15.41.10

8. Analyze the E-1 input character, and set up controls for the E-1 to E-2 transfer.

E-ch select 7-bit unit	E-ch select unit 1	13.62.03
E-ch word-separator mode	E-ch select 7-bit unit E-ch load mode	15.62.02
E-ch word separator	E-1 input C · B · 4 · 2 · 1 · A · B-bits	15.41.01
E-1 reg word separator latch (on)	E-ch word separator E-ch word-separator mode Set E-1	15.41.11

9. Transfer E-1 to E-2. If the instruction is given in the move mode, set E-2 with E-1 BCD.

E-ch reset	I-ring 4 time Percent or coml at Logic gate C	15.41.12
(not) E-1 reg word separator	E-ch reset	15.41.11
Copy E-1 BCD to E-2	(not) E-1 reg word separator	15.62.06
E-2 reg full latch (off)	E-ch reset	15.41.10
Set E-2 reg	E-1 reg full latch (on) E-2 reg full latch (off)	15.62.04
E-2 reg full latch (on)	Set E-2 reg (not) E-1 reg word separator	15.41.10
E-1 reg full latch (off)	E-ch input mode Set E-2 reg	15.41.10

10. Transfer E-1 to E-2. If the instruction is given in the load mode, and the E-1 reg not-word-separator latch is ON, copy E-1 BCD to E-2.

(not) E-1 reg word separator	E-ch not-word separator Set E-1 reg	15.41.11
Copy E-1 BCD to E-2	(not) E-1 reg word separator	15.62.06
E-2 reg full latch (on)	Set E-2 reg E-1 reg not-word separator	15.41.10
E-1 reg full latch (off)	E-ch input mode Set E-2 reg	15.41.10

11. Transfer E-1 to E-2. If the instruction is given in the load mode with a word-separator character in E-1 and no word separator in E-2, generate a word-separator character and set it into E-2 with a C-bit. The E-2 full latch is not set because the next character from read storage must be combined with the E-2 character before the contents of E-2 can be stored.

SIGNAL	CONTROL	LOGIC
Set E-2 word separator	Set E-2 reg (not) Gate console to assembly E-1 reg word separator (not) E-2 reg word separator	15.62.06
Copy E-1 WM • C-bit	(not) E-2 reg word separator E-ch input mode	15.62.06
Set E-2 reg delayed	Set E-2 reg (off)	15.62.04
E-2 reg word separator	Set E-2 reg delayed E-ch word-separator mode E-1 reg word separator	15.41.11

12. Transfer E-1 to E-2. If the instruction is given in the load mode with a word separator character in E-2 and no word separator in E-1, copy E-1 BCD and generate a word mark in E-2.

Copy inv E-1 WM • C-bit	E-2 reg word separator (not) E-1 reg word separator E-ch input mode (not) Gate console to assembly	15.62.06
Copy E-1 BCD to E-2 reg	E-2 reg word separator	15.62.06
E-2 reg full latch (on)	Set E-2 reg E-1 reg not word separator	15.41.10

13. Transfer E-1 to E-2. If the instruction is given in the load mode with a word separator character in E-1 and E-2, set E-2 with E-1 BCD and C-bit.

Copy E-1 BCD to E-2 reg	E-2 reg word separator	15.62.06
Copy E-1 WM • C-bit	E-2 reg word separator E-1 reg word separator E-1 reg not WM bit	15.62.06

14. Initiate a storage cycle in the CPU whenever E-2 is full (E-2 full latch on). If the command is unoverlapped, take an E-cycle and read out the BAR.

E-cycle required	E-ch in process E-ch output mode (not) E-ch int end of transfer E-1 reg full latch (off) (not) E-cycle • any last gate	12.12.62
(Start logic clock)	E-cycle required	11.10.10
E-cycle ctrl	E-ch unovlp in process E-cycle required 2nd clock pulse Logic gate Z (not) E-ch int end of transfer (not) F-cycle required	12.12.66
E-cycle	E-cycle control	12.12.02
RO BAR	Logic gate B or S E-cycle ctrl E-ch unovlp in process (not) Console inhibit AR RO (not) E-ch 2nd address unovlp (not) 1st I/O cycle control	14.71.31

15. Initiate a storage cycle in the CPU whenever E-2 is full (E-2 full latch on). If the command is overlapped, take an E-cycle and read out EAR.

SIGNAL	CONTROL	LOGIC
E-cycle required	E-ch in process E-ch output mode (not) E-1 reg full (not) E-ch int end of transfer (not) E-cycle • Any last gate	12.12.62
(Start logic extension clock)	E-cycle required	11.10.20
E-cycle ctrl	E-ch overlap in process E-cycle required 2nd clock pulse Logic gate Z (not) E-ch int end of transfer (not) F-cycle required	12.12.66
E-cycle	E-cycle ctrl	12.12.66
RO EAR	Logic gate B or S E-cycle ctrl E-ch ovlp in process (not) Console inhibit AR RO (not) E-ch 2nd addr ovlp	14.71.35

16. Gate the E-2 character to the A-channel.

Gate E-2 data reg to A-ch	E-ch input mode E-cycle (not) Control reg disable	15.38.03
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17. End the internal transfer, if the B-channel character is a group mark with a word mark.

B-ch group mark • WM	B-Ch 1 • 2 • 4 • 8 • A • B • WM	15.41.07
E-ch end of record latch	E-cycle B-cy group mark • WM Logic gate F R-symbol op modifier (not) 1401 card print in process	13.63.01

18. End the internal transfer, if a wrap-around condition occurs.

E-ch end of record latch	(not) E-ch last input cycle Wrap-around conditions Logic gate F or W 2nd clock pulse 2 E-cycle	13.63.01
E-ch int end of transfer	E-cycle (not) E-ch last input cycle Wrap-around conditions Logic gate F or W 2nd clock pulse 2	13.63.01

19. End internal transfer. If the external end of transfer occurs before the internal end of transfer, take an extra input cycle to search for the group-mark with a word-mark, and end internal transfer.

E-ch last input cycle	E-ch ext end of transfer (not) E-1 reg full (not) E-2 reg full E-cycle E-ch input mode Logic gate C or T	13.63.02
E-ch int end of transfer	E-ch last input cycle Logic gate F or W	13.63.01

SIGNAL	CONTROL	LOGIC
20. Develop assembly controls. If the asterisk insert switch is ON and the A-channel character is invalid, set an asterisk.		
In cy GM • WM ctrl	B-ch not group mark • WM Input cycle (not) Any last input cycle	15.49.02
A-ch invalid	(Invalid bit configuration)	18.11.03
Set asterisk	In cy GM • WM ctrl A-ch invalid (not) 1 asterisk ins console sw (off)	15.49.06

21. Develop assembly controls. If the asterisk insert switch is OFF, and the A-channel character is invalid, stop the clock.

Master error	A-channel VC error Logic gate A or R	18.14.08
Stop latch	Master error	12.15.04

22. Develop assembly controls. If the instruction is given in the load mode with a valid A-channel character, use the A-channel numerical bits, word mark bit, and zone bits.

A-ch valid + asterisk switch (off)	A-ch valid or Ast ins console sw (off)	15.49.02
E-ch select odd parity unit	E-ch select unit 1	13.60.03
Odd parity cycle	E-ch select odd parity unit E-cycle	13.60.02
Use A-ch zones	In cy GM • WM ctrl A-cy valid + asterisk switch (off) Odd-parity cycle	15.49.03
Use A-ch nu	In cy GM • WM ctrl A-ch valid + asterisk switch (off) Odd-parity cycle	15.49.03
Use A-ch WM	In cy GM • WM ctrl A-ch valid + asterisk switch (off) Load cycle	15.49.02

23. Develop assembly controls. If the instruction is given in a move mode with a valid A-channel character, use the A-channel numerical bits and zone bits and the B-channel word mark bit.

Use a-ch zones	In cy GM • WM ctrl A-ch valid + asterisk switch (off) Odd-parity cycle	15.49.03
Use A-ch nu	In cy GM • WM ctrl A-ch valid + asterisk switch (off) Odd-parity cycle	15.49.03
Use B-ch WM	Move cycle Input cycle	15.49.04

24. Develop assembly controls. If the internal end of transfer is detected, use the full B-channel character.

I/O grp mk • WM stop ctrl	E-ch ovlp in process E-cycle or E-ch unovlp in process	13.65.04
---------------------------	--	----------

SIGNAL	CONTROL	LOGIC
Use full B-ch	E-cycle R-symbol op modifier I/O grp mk • WM stop ctrl B-ch group mark • WM Input cycle (not) 1401 card print in process	15.49.05

25. Develop assembly controls. If the CPU is in the last input cycle, use the full B-channel character.

Any last input cycle	E-ch last input cycle	13.63.02
Any last in cycle not 1401	Any last input cycle (not) 1401 mode	15.49.05
Use B-ch nu	Any last in cycle not 1401	15.49.05
Use B-ch zones	Any last in cycle not 1401	15.49.05
Use B-ch WM	Any last in cycle not 1401	15.49.04

26. Reset the E-2 full latch after each input cycle.

Reset E-2 full latch	Any last gate E-ch cycle In cy GM • WM ctrl 2nd clock pulse (inverted)	15.62.05
----------------------	--	----------

27. After both internal and external transfers end, develop a sample pulse for setting the E-channel status indicators.

E-ch int end of transfer delayed	Logic gate Z	13.65.05
E-ch status sample B	E-ch int end of transfer E-ch ext end of transfer E-ch int end of transfer delayed Logic gate Z 2nd clock pulse 1 (inverted)	13.65.05

28. Set the E-channel wrong length record status indicator, if the record length was incorrect.

E-ch wrong-length record	E-ch status sample B E-ch strobe trigger or E-2 reg full or (not) E-ch end of record latch	13.63.03
--------------------------	---	----------

29. Set the E-channel data-check status indicator, if any error occurred during the transfer.

Errors 2	Pwr'd clock error or Ring error to error latch or Parity 1 or Parity 2	52.12.01
PT errors	Errors 2 PT rd scan or Parity error to adapter or PT ready error	55.10.06
14C5-A ext error status	PT rd op PT errors	55.10.04
Buffer error	14C5-A ext error status	51.40.21
E-ch check bus	Buffer error E-ch select any buffer	12.62.03
E-ch check	E-ch check bus E-ch status sample B	12.62.04

SIGNAL CONTROL LOGIC
 30. Continue with the stored program. If the command is unoverlapped, set last execute cycle and reset the unoverlap in process latch.

Last execute cycle I/O	E-ch unovlp in process (not) 1401 card or print op code	13.65.07
E-ch second sample B	E-ch status sample B E-ch status sample B 2nd clock pulse (inverted)	13.65.05

SIGNAL	CONTROL	LOGIC
E-ch status sample B-delay	E-ch second sample B 2nd clock pulse (inverted)	13.65.05
(Reset) E-ch unovlp in process	E-ch status sample B-delay	13.60.04

31. Continue with the stored program. If the command is overlapped, reset the overlap in process latch.

(Reset) E-ch ovlp in process	E-ch status sample B-delay	13.60.04
------------------------------	-------------------------------	----------

1411-1405 Disk Storage Operation

This section explains the control of the IBM 1405 Disk Storage by the IBM 1410 Data Processing System. Included are instruction read-out and control circuits in the 1410. Information on the mechanical and electronic operation of the Disk Storage may be found in the *IBM 1405 Disk Storage*, Customer Engineering Manual of Instruction, Form 227-5542.

Disk control commands make it possible to seek a disk record, to read and write a single record or a full track (with or without word marks), and to check for accurate results. The various parts of a disk-unit instruction-word are:

1. *Mode of operation — move (M), or load (L)*: The move mode records data on, or reads data from, the disk unit in 7-bit coding (no word marks). The load mode records data on, or reads data from, the disk unit in 8-bit coding (with word marks). Data must read from the disk unit in the same mode (move or load) in which it is written.

2. *X-control field*: This three-position field selects the transmission channel, the disk storage unit, and the specific type of operation.

a. The hundreds position of the X-control field defines which data transmission channel is to be used, and whether the operation is to be performed with or without overlapping.

b. The tens position of the X-control field must contain the character F to specify the disk storage unit as the active input-output device.

c. The units position of the X-control field specifies the type of operation to be performed. The characters used in this position are: 0, seek operation; 1, single-record operation; 2, full-track operation; 3, write-check operation; and 4, write-address operation.

3. *B-address*: This address specifies the high-order core storage position of the field that contains the 8-character disk unit address and the record data.

4. *d-modifier character*: This position specifies a read (R) or write (W) operation.

Timings for instruction read out of a disk unit instruction are shown in Figure 71.

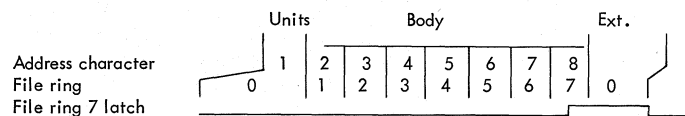
The 8-character disk unit address is used to locate the specific area of disk storage for the read or write operation. The format for the disk unit address is shown in Figure 72.

Seek-Disk Record

Function

The M/L % F 0 (B) R command (Figure 73) causes the selected access mechanism to seek the disk and track that are specified by the disk-unit address. The instruction sends the 8-character address to the file control unit (FCU). After the FCU receives the address, the CPU continues on with the next instruction in sequence while the access mechanism moves to the desired disk and track. Access time varies from 100 to 800 milliseconds.

The address must be 8-characters, followed by a group mark with a word mark. The file digit ring is an eight-position ring that is used to count the characters in the address. The digit ring is at position 0 while the first character reads out and is sent to the FCU. The ring advances to position 1, and the second character reads out and is sent to file, etc.



Two D-cycles are required to read out each character and to send it to file. During the first D-cycle, the character reads out of storage and is gated to the E-2 register (Figures 74 and 75). Also, during this cycle the B-channel is analyzed to determine whether the character is a GM-WM. If there is no GM-WM, and the file ring 7 latch is OFF, the character is sent to the FCU during the second D-cycle. If there is a B-channel GM-WM or the file ring 7 latch is ON, the second D-cycle develops status sample A to set the status indicators with file not ready, busy, or data check if a validity check error of a character that is sent to file occurred. During this cycle the B-channel must be a GM-WM and file ring 7 latch must be ON to set correct length record. Status sample A is not developed at last instruction read-out as in other I-O Instructions. It will be brought up at the end of first address transfer after access and file have been selected.

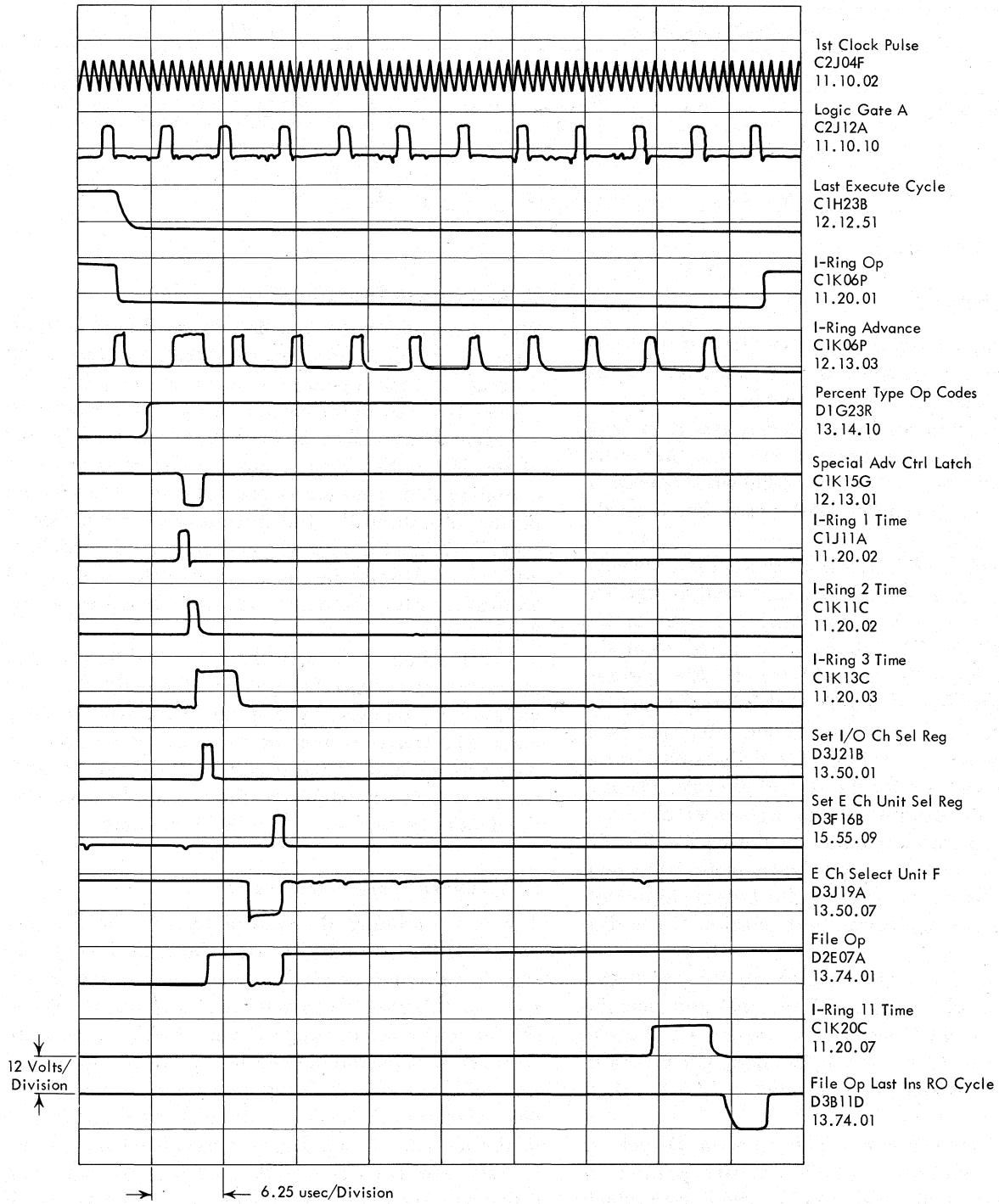


Figure 71. 1405 Disk Storage Instruction Read-out Timing Chart

Address Field In Core Storage									Record Input or Output Area	∨ ≠
Access Select X	Indelible Address In Disk Storage								200 Characters - 1 Record Move Mode 176 Characters - 1 Record Load Mode 1000 Characters - 1 Track Move Mode 880 Characters - 1 Track Load Mode	X ∨ ≠
	Disk Unit X	Disk X	Face X	Track X	Sector X	Constant X	End Address Transfer X ∨ ≠			
0 - 2	0 - 4	00 - 99	00 - 99	0 - 9	0					

Figure 72. Disk Unit Address

Operation (Figure 73)

During instruction read-out, after the i-o interlock check, the E-channel controls and status latches are reset and a "seek call" is sent to file.

At I6 time, with all file op codes, the read back check (RBC) interlock is checked to insure that a RBC was given as the first file op after a file write operation. If an RBC was not given, the master error line is conditioned to stop the CPU.

The first cycle after instruction read-out is a D-cycle, with the no-scan latch ON. The DAR is used to read out the high-order (access mechanism) character of the disk unit address. The character is gated from the B-channel through the assembly to the E-1 register. The E-1 register full latch gates "set E-2 reg" to set the character into the E-2 register. There must not be a B-channel GM-WM at this time. The body latch and the 2nd scan latch are set for the second D-cycle. The DAR still contains the address of the high-order character because the no-scan latch was set during the first D-cycle. The DAR is used to read the character out again. The 2nd scan latch is ON during this D-cycle to modify the address in the DAR to the next position of the disk address.

A strobe pulse is sent to the file to indicate that a character is available on the E-channel and that the body and no scan latches are set for the next D-cycle.

During this no scan D-cycle, the body latch is ON to gate a digit advance pulse to advance the file digit ring to position 1.

The operation continues. The no scan D-cycle is followed by a 2nd scan D-cycle for each position of the file address. At the 2nd scan D-cycle during which the 8th character of the file address is sent to file, file ring 7 latch sets. The next character reads from storage, and should be a GM-WM.

During the final D-cycle, status sample A is developed to set the status indicators. The presence of a GM-WM without the file ring 7 latch or vice versa, results in a wrong length address, and sets the E-channel wrong length record indicator.

The "Addr TFR" gate and file ring 7 latch are reset by status sample A delay and last execute cycle is conditioned to initiate the next instruction.

Disk-Address Transfer (Figure 76)

The address portion of the data in the B-field is transferred to the file before the actual data transfer during all read or write operations. After the first time the address transfers to the file, the various error conditions are checked, as well as the busy status and ready status of the file. If the file is ready for the read or write operation and if no errors are indicated, the address portion of data in the B-field transfers for the second time. This time the address compares with the indelible address read from the file location. After the second address transfer, the data reads from or writes on the file location.

The location of storage that the B-address of the instruction word specifies, contains the eight-character file address followed by a group mark with a word mark. The area of storage that follows the group mark with a word mark contains either the data to be written for a write operation, or the storage locations for the data to be read into on a read operation.

First Address Transfer (Figure 77)

The CPU conditions the control lines to the file unit as soon as the instruction word is decoded. Load-mode signals, full-track or single-record signals, and input-mode or output-mode signals are sent to the file. When the file unit receives these signals, control circuits are established to handle the address and data transfers. If the operation that is being performed is write disk check (read back check), a write check signal is sent to the file and the read back check latch in the CPU is reset. The latch sets at the end of a normal write disk operation. If any disk instruction, except write disk check, is attempted with this latch on, the master error line stops the CPU. The CPU uses the D-address register, and executes D-cycles for the first address transfer. Two D-cycles are necessary to transfer one address character during the first address transfer. The no scan and 2nd scan latches control modification of the D-address register.

The no scan D-cycle reads the disk address characters out of the storage locations. The character is checked to determine if it is the group mark with a word mark. If the group mark with a word mark is

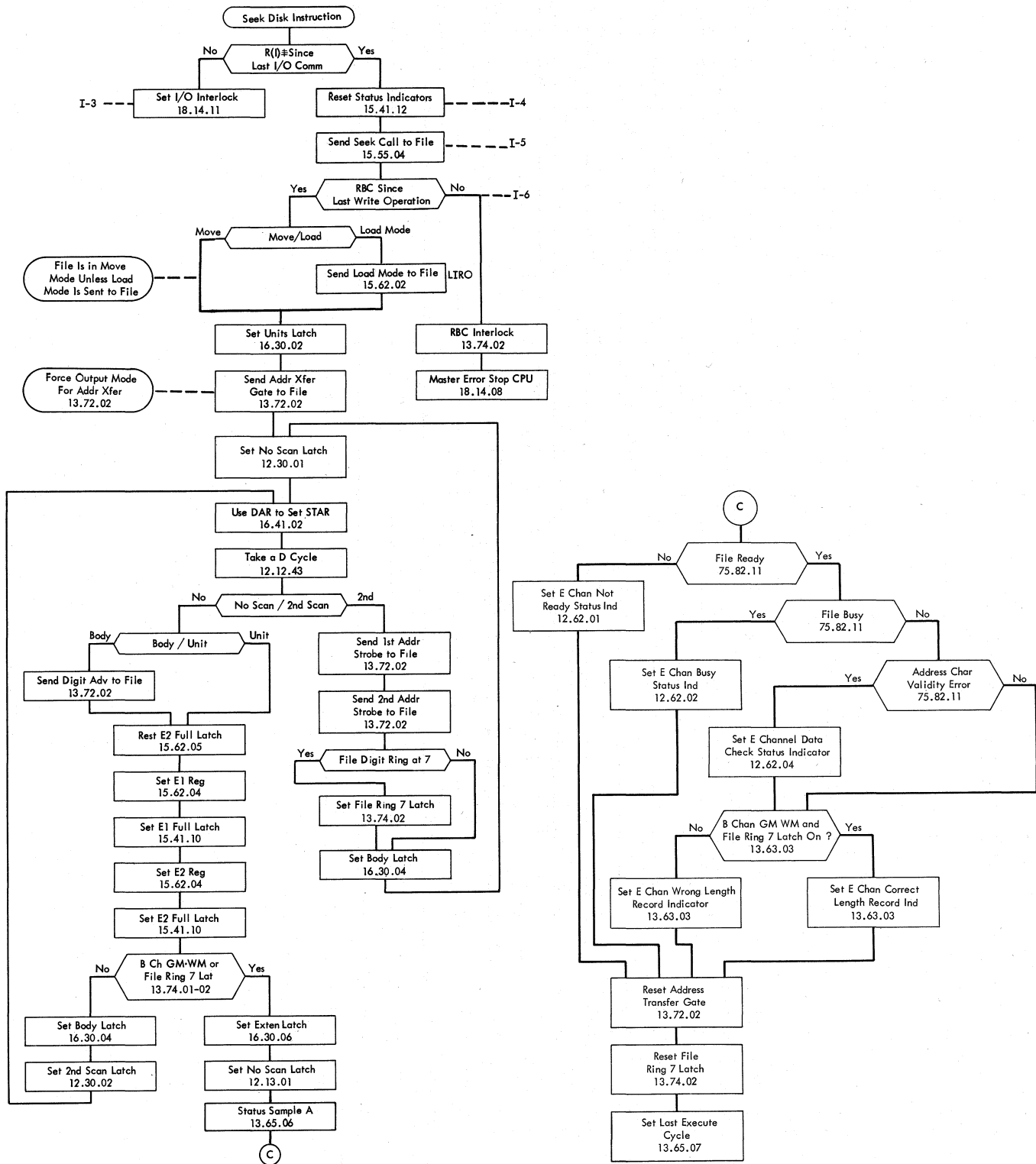


Figure 73. Disk Seek Operation

Seek Disk Record \checkmark M % F001000R 1000 \checkmark 01234560 \checkmark or (ARM0, Unit 1, Disk 23, Track 45, Sector 6)

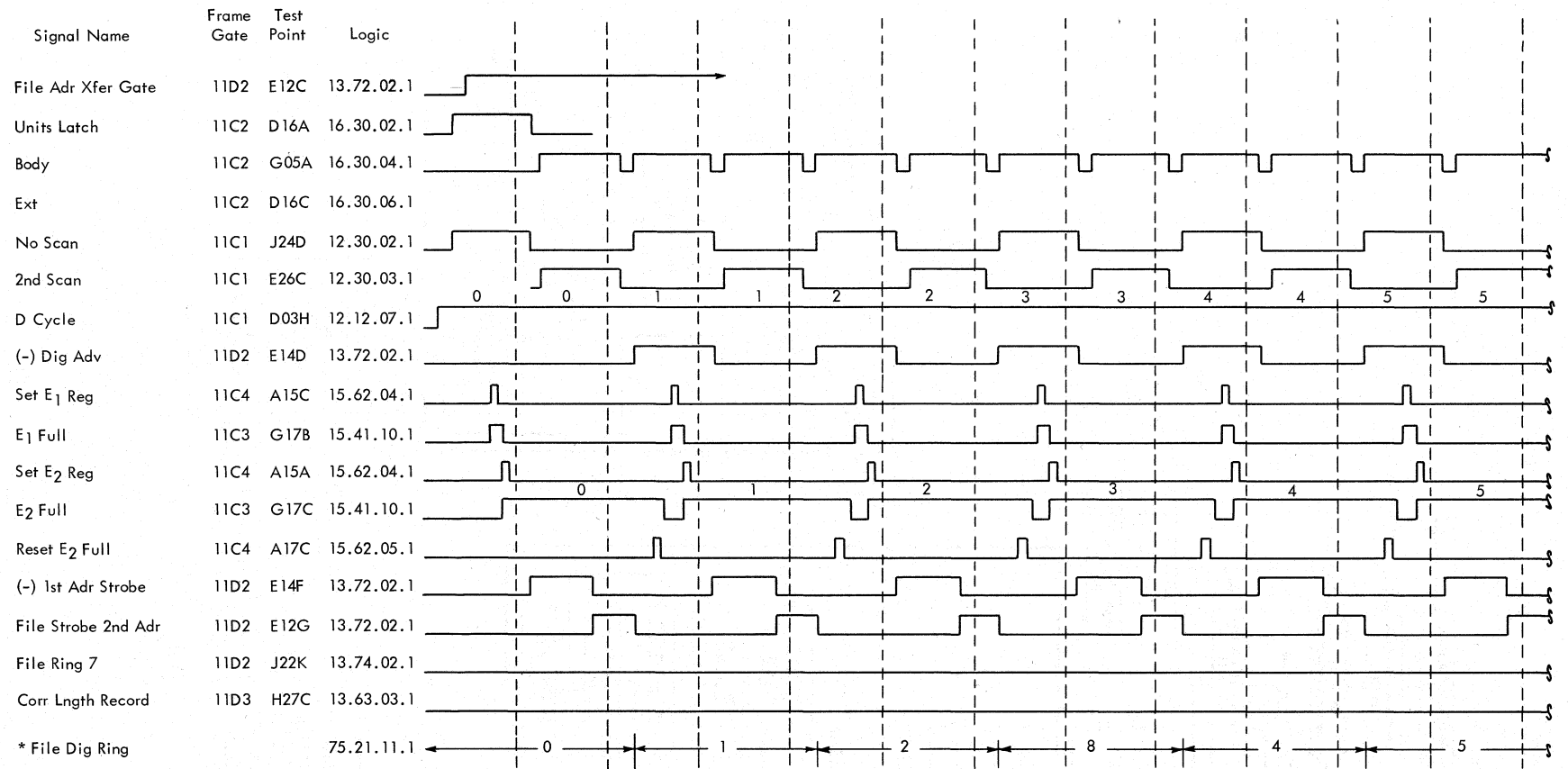


Figure 74. 1405 Seek Disk Record Timing Chart

Seek Disk Record M % F001000R 1000 01234560 ¥ or (ARMO, Unit 1, Disk 23, Track 45, Sector 6)

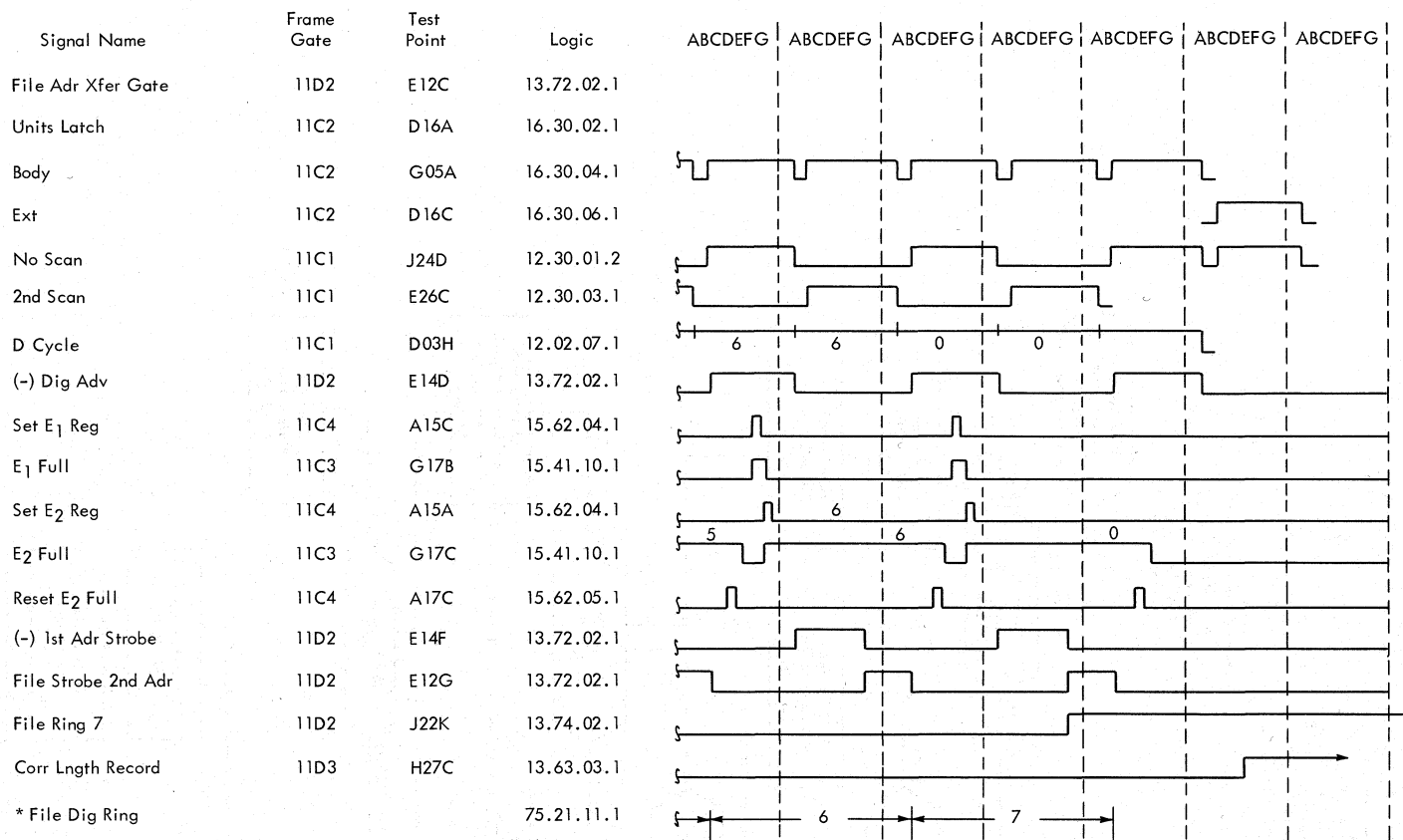


Figure 75. 1405 Seek Disk Record Timing Chart, Type 2

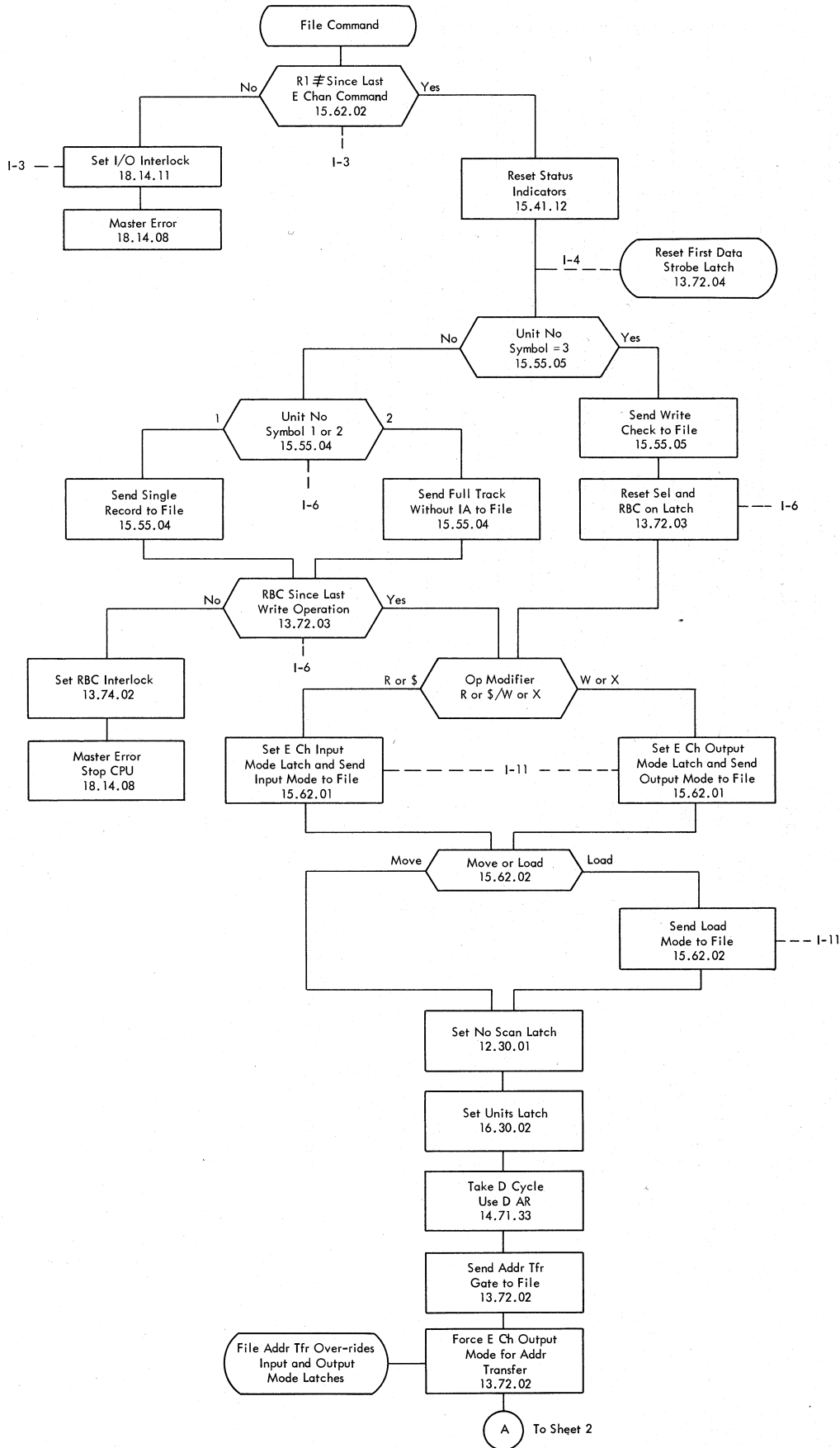


Figure 76. Disk Address Transfer (Sheet 1 of 4)
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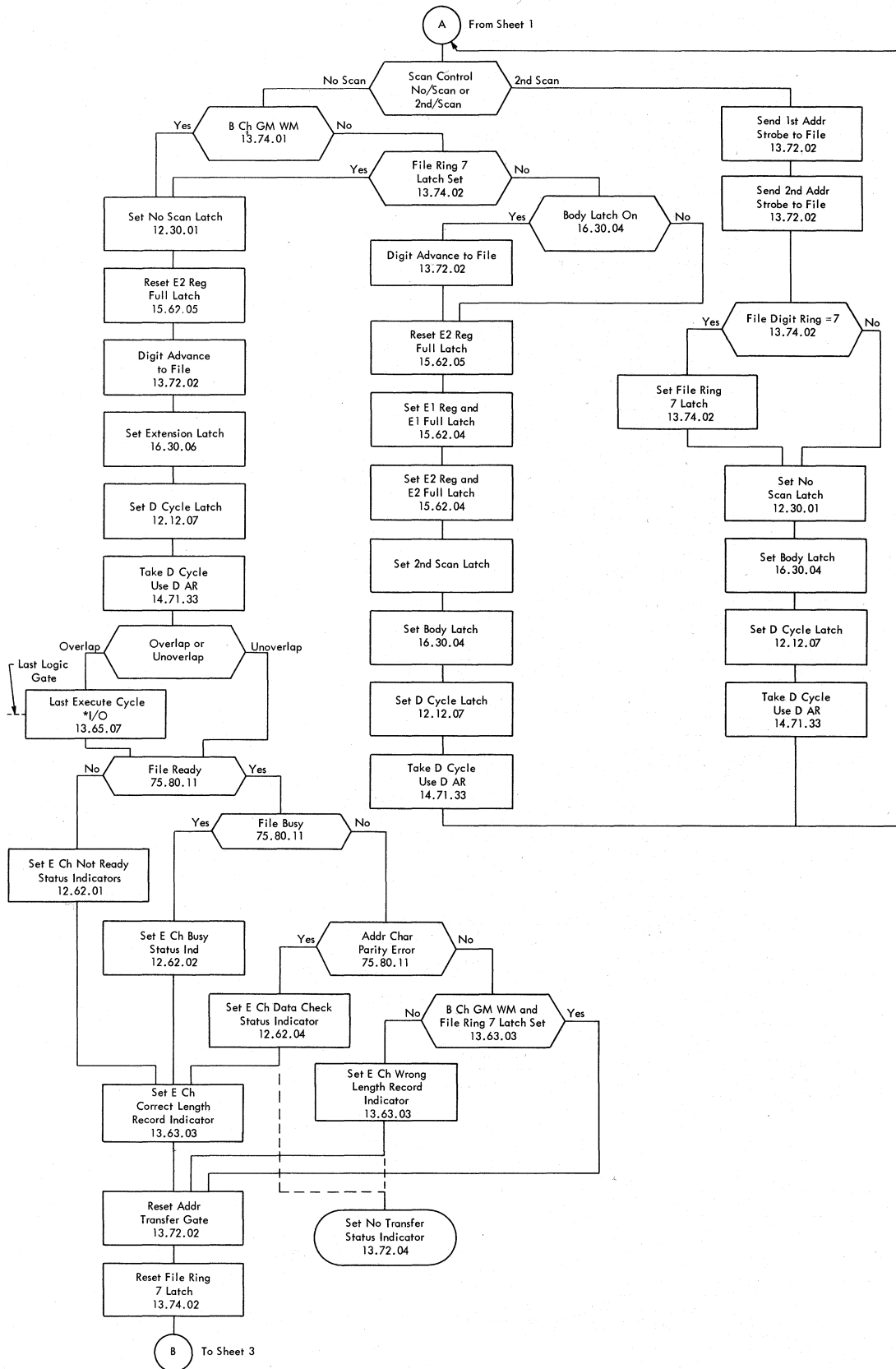


Figure 76. Disk Address Transfer (Sheet 2 of 4)

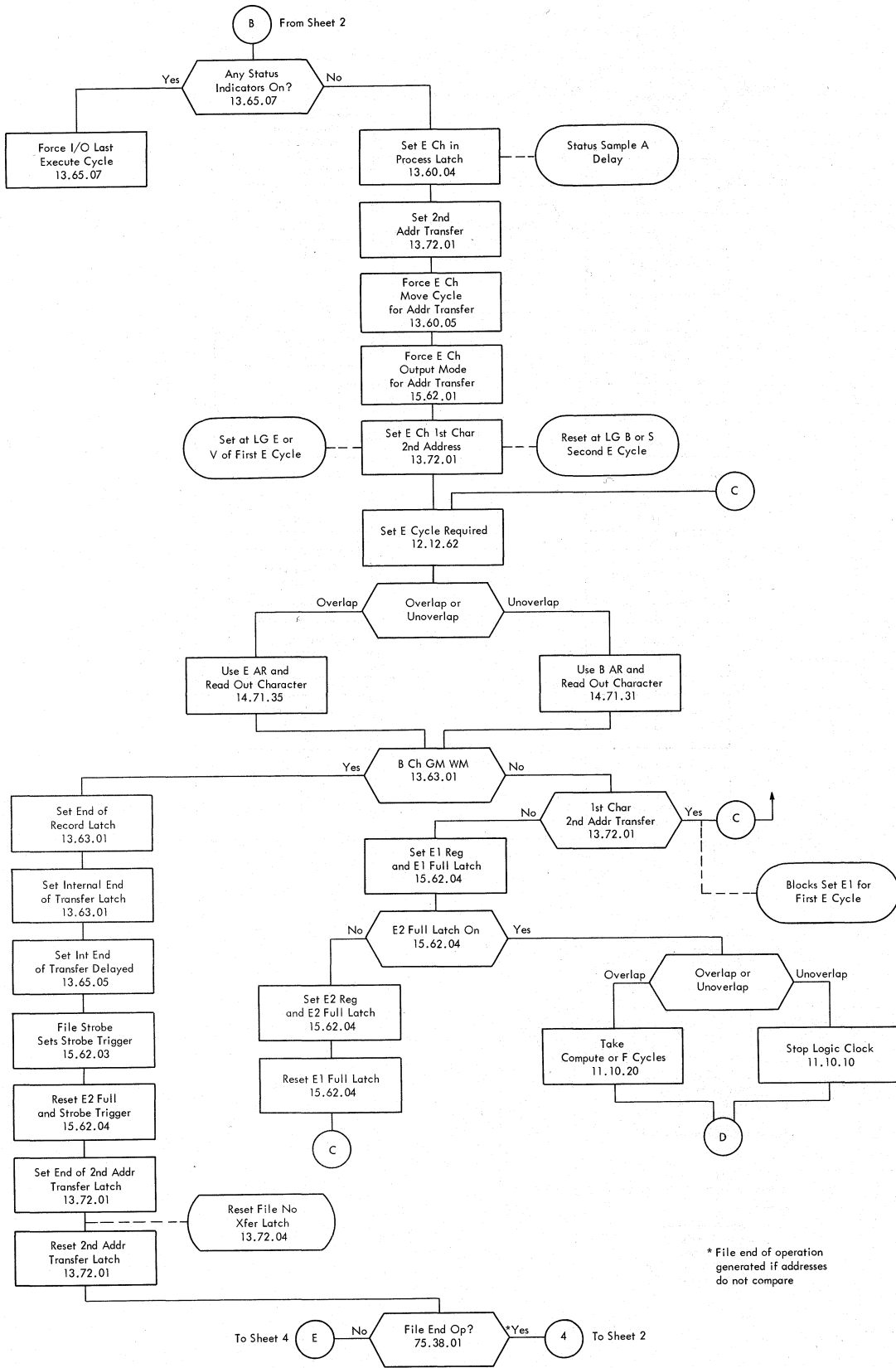
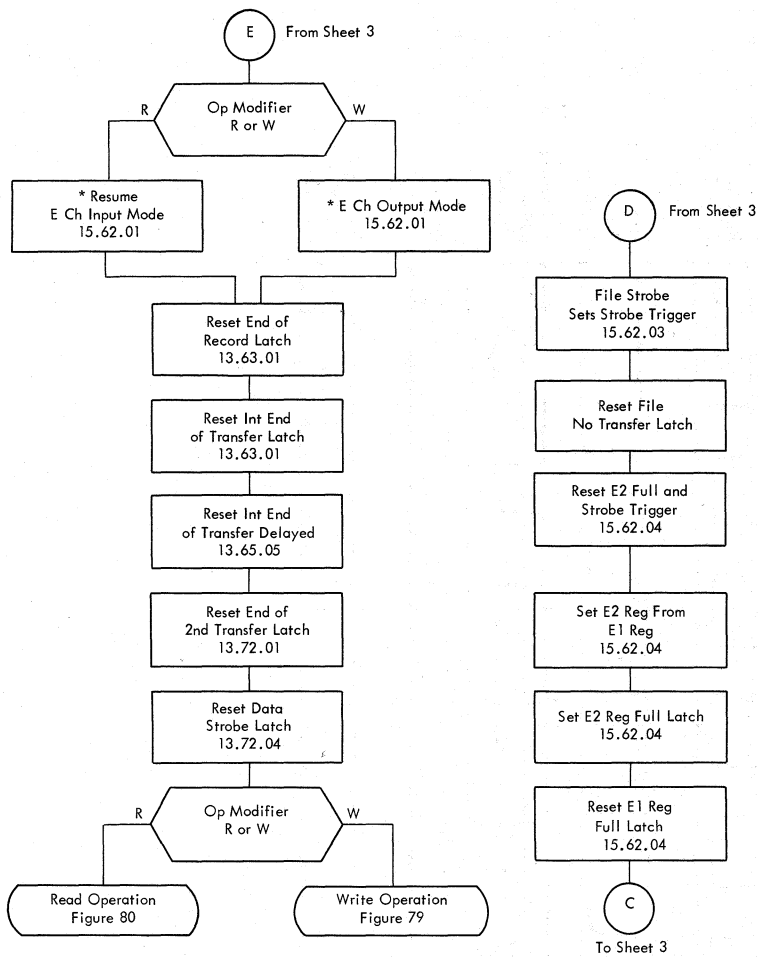


Figure 76. Disk Address Transfer (Sheet 3 of 4)



*Output mode is forced during first and second address transfer. Mode required by the instruction is effective here.

Figure 76. Disk Address Transfer (Sheet 4 of 4)

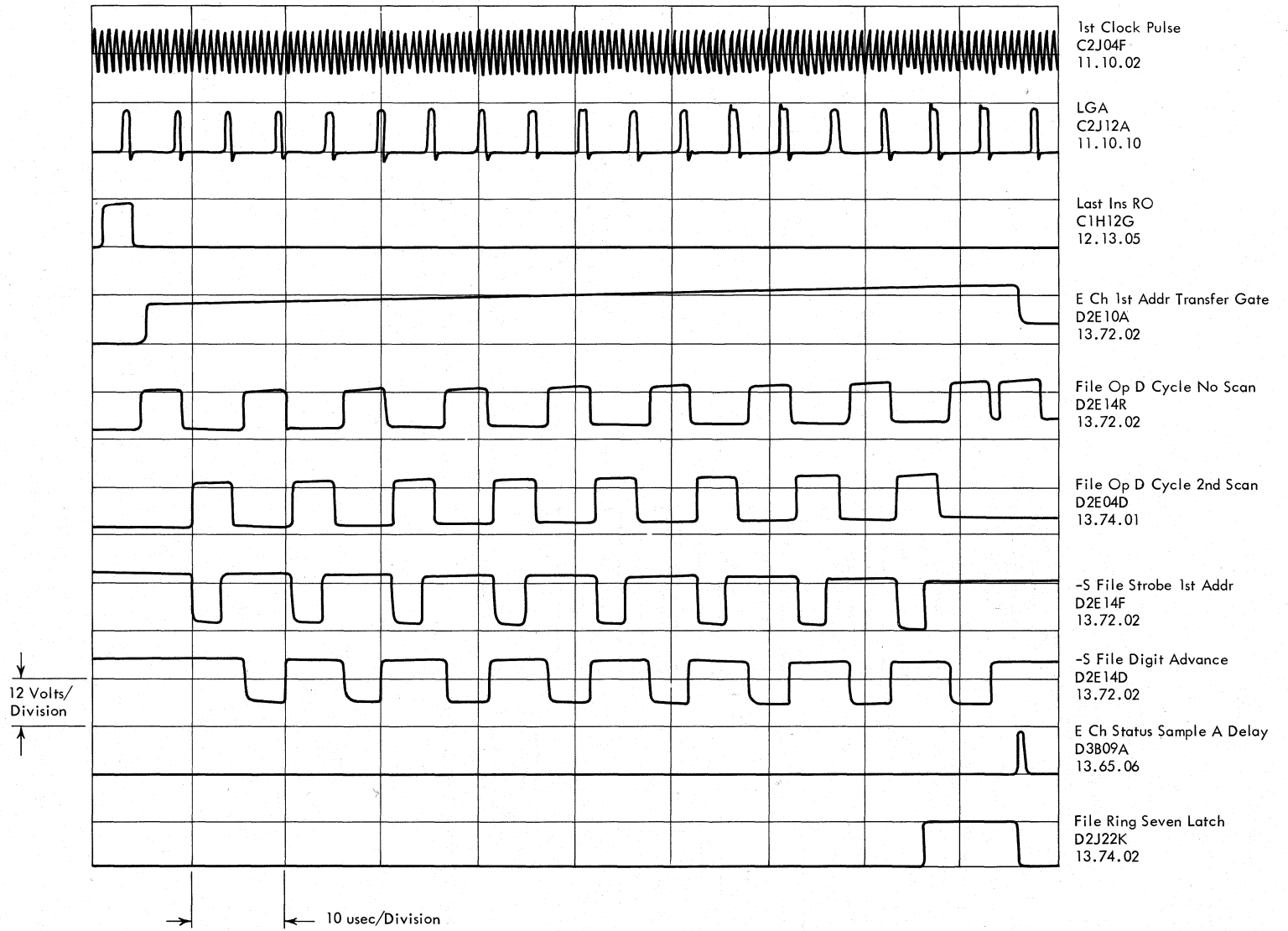


Figure 77. 1405 Disk Storage First Address Transfer Timing Chart

sensed, the end of the first address transfer is initiated. The error lines are tested and the not ready and busy conditions of the file are checked.

If the group mark with a word mark is not sensed, the file ring 7 latch is checked. As each character in the body of the address field reads out of storage, the CPU sends a digit-advance pulse to the file. The digit-advance pulse steps the file ring. As the eighth and final character of the address field reads out of storage, the file ring steps to 7 and turns file ring 7 latch ON in the CPU. This latch initiates the end of first address transfer in the same manner as sensing the group mark with a word mark. If the character that reads from storage is not a group mark with a word mark, and if the file ring is not at 7, the character sets into the E-1 register and then transfers to the E-2 register. The 2nd scan latch sets and another D-cycle is taken.

The 2nd scan D-cycle transfers the address character from the E-2 register to the file. The CPU generates an address-strobe pulse to signal the file that a character is ready for transfer. The file samples the character in the E-2 register each time an address-strobe pulse is received. During the 2nd scan D-cycle, the D-address register is modified. The file ring in the file unit is sampled, and if it is equal to seven, the file ring 7 latch in the CPU is conditioned. The no scan latch is turned ON and another D-cycle starts.

At the end of the first address transfer, the file is checked to determine whether it is ready and not busy. The characters in the address field are checked for parity, and the field is checked for proper length.

Second Address Transfer (Figure 78)

The second address transfer is necessary to compare the address portion of the B-field to the indelible address that reads from the file. If the addresses do not compare, a file end of operation signal is generated and no data transfers. The second address transfer occurs in the move mode, and the E-channel is in output mode. These conditions are forced regardless of the instruction word. Only seven address characters transfer during the second address transfer. The first address character (access arm identification) does not transfer. As the address characters read out of storage, they are sensed to determine if the group mark with a word mark has been reached. The group mark with a word mark starts the end of the second address transfer. This transfer is in an overlap or unoverlap mode. The characters read out, using the E- or B-address registers on E-cycles. An E-cycle is required when the E-1 register is not full.

Strobe pulses, that are generated in the file, control address-character movement from storage to E-1 and E-2 registers. The strobe pulse indicates to the CPU that

the file has accepted the E-2 register character. The E-1 register character transfers to the E-2 register, and the next storage character reads to the E-1 register. The first strobe pulse from the file resets the no transfer latch.

When the character that reads out from storage is sensed as the group mark with a word mark, the end of the second address transfer starts. Control circuits for the second address transfer reset and the conditions that the instruction words call for are resumed. If the addresses compare, the CPU is now ready to transfer data to or to receive data from the file.

Disk Write (Figure 79)

There are three basic disk write operations: write a single record, write a full track, and write disk check. Each operation can be given in either the move mode or the load mode, overlapped or unoverlapped. Data flow within the CPU is similar for each operation. Data transfers from the storage location to the E-1 register. If the E-2 register is not full, the data transfers from the E-1 register to the E-2 register. A character reads out of storage whenever the E-1 register is not full.

Write a Single Record

The write a single record operation causes a single record to write on disk storage from core storage. The data in core storage should fill the entire disk unit sector area to prevent a CPU wrong-length record indication. As each character reads from storage, it is checked for the group-mark with a word mark or wrap around condition. The d-modifier of the instruction word determines which condition (GM-WM or wrap-around) causes the internal end of transfer. If the character is normal (not GM-WM or wrap-around) it is transferred to the E-1 register, and then, to the E-2 register, if the E-2 register is not full. In the overlap mode, the computer takes compute or F-cycles while waiting for the file strobe. The file unit samples the output lines from the E-2 register, and generates a file-strobe pulse to send to the CPU. The file-strobe pulse indicates that the file unit has accepted the character from the E-2 register. Upon receiving the strobe pulse, the computer transfers a new character from storage.

The CPU senses the GM-WM or wrap-around condition after the last character of the record reads out of storage. The internal end of transfer is established and a disconnect signal is sent to the file. The file unit senses the end of the record and sends an end of operation signal to the CPU. The data is checked for proper parity and correct length.

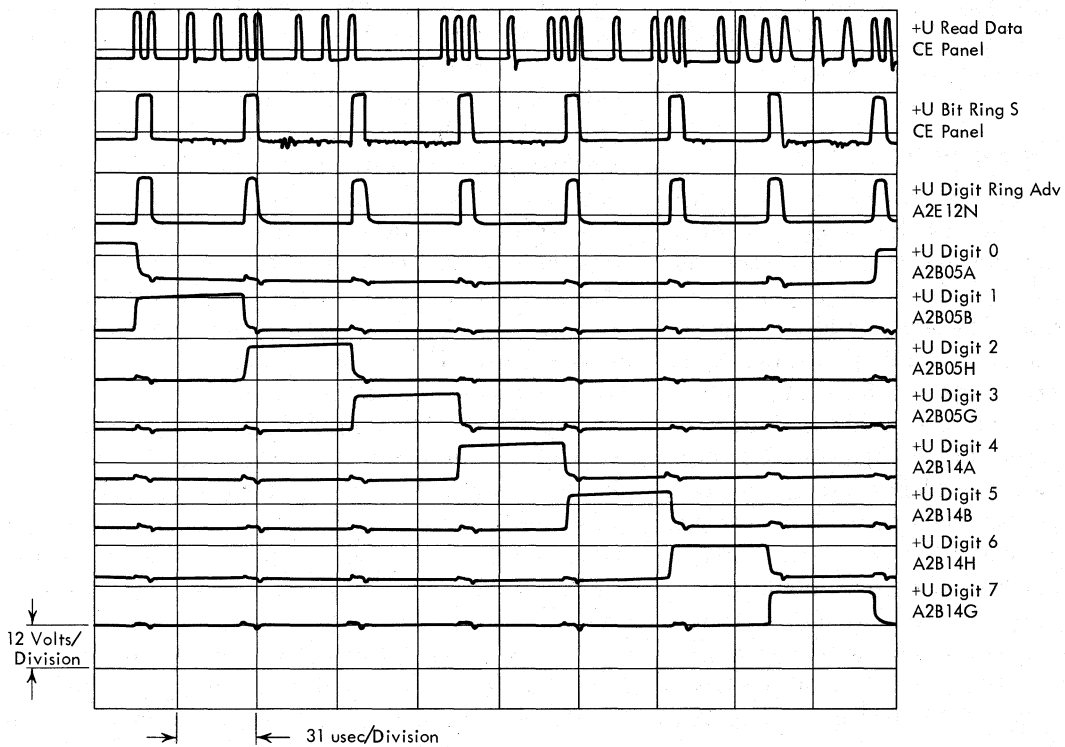
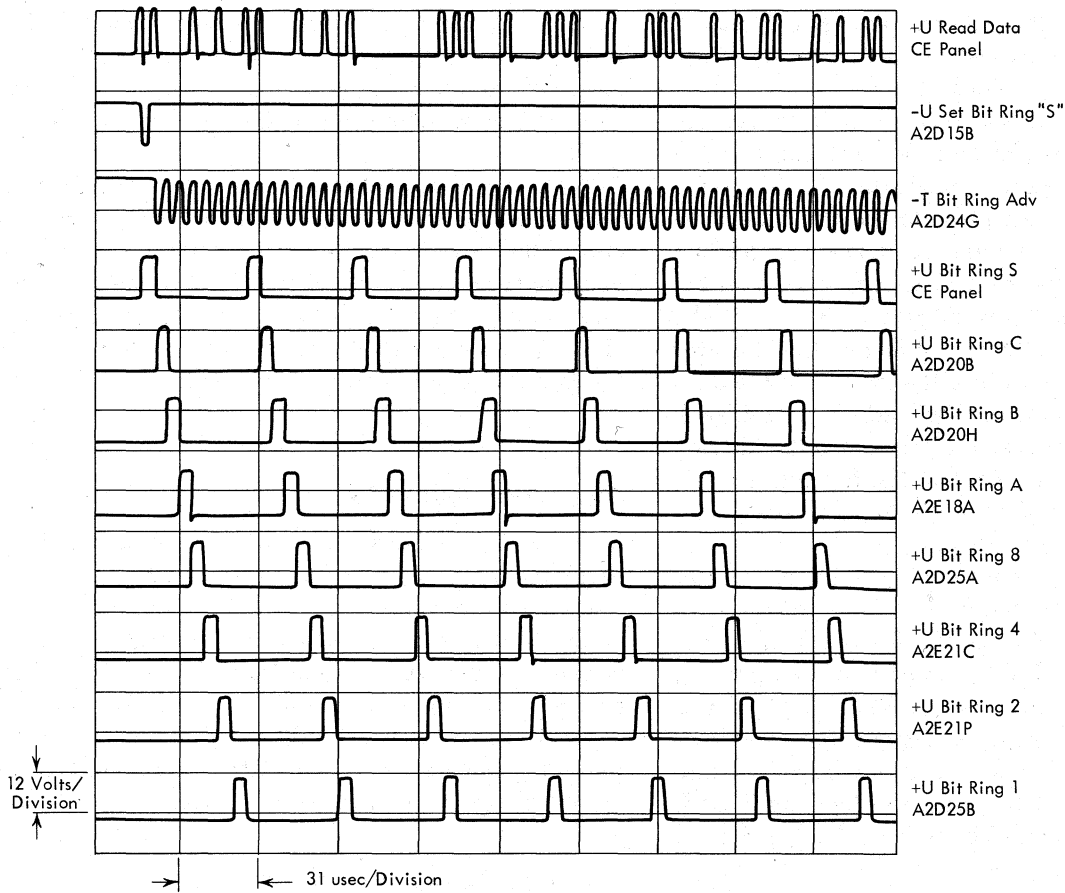


Figure 78. 1405 Disk Storage Second Address Transfer Timing Chart

From Figure 64, Sheet 4
and Figure 79 Sheet 2

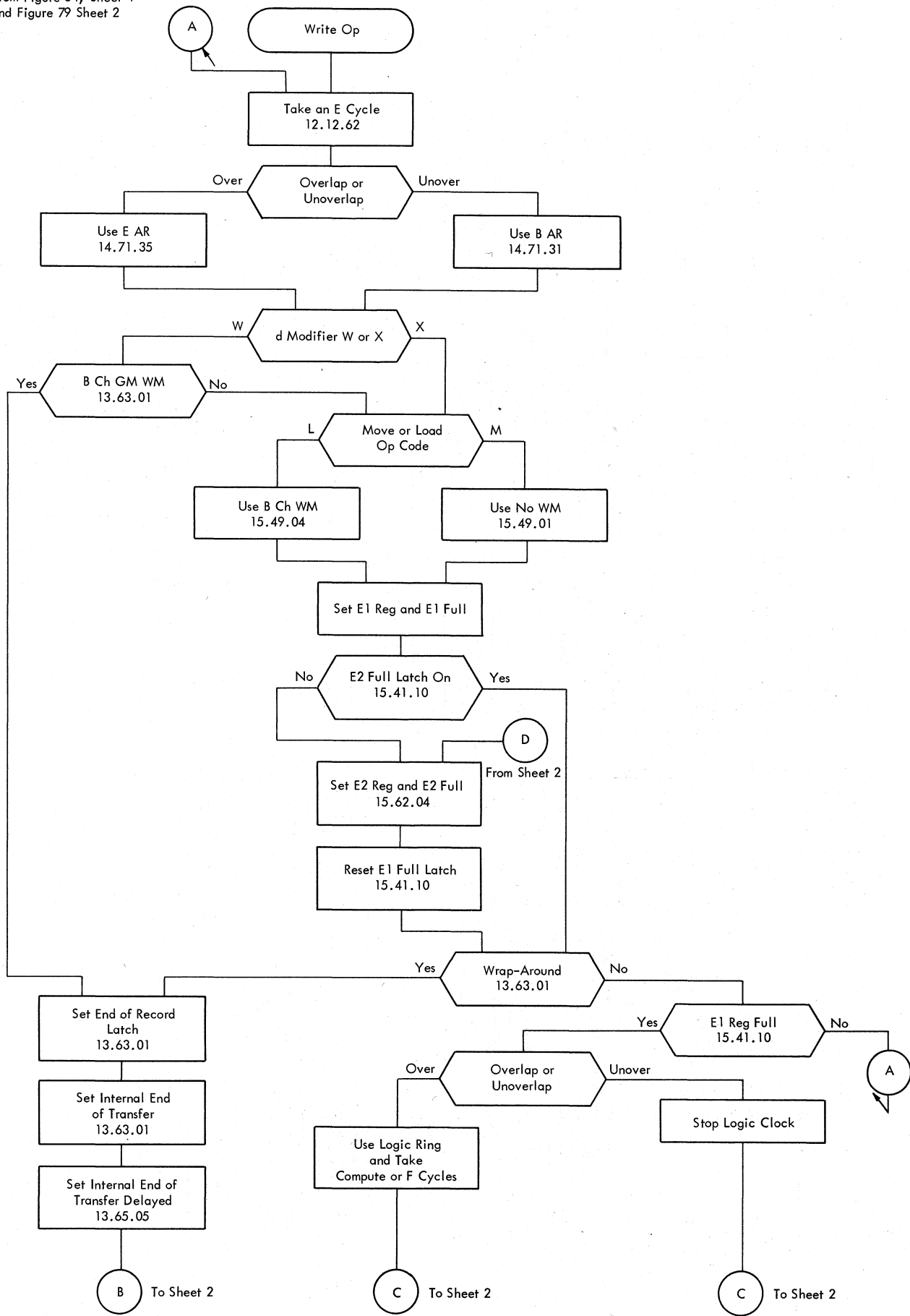


Figure 79. Write Operation (Sheet 1 of 2)

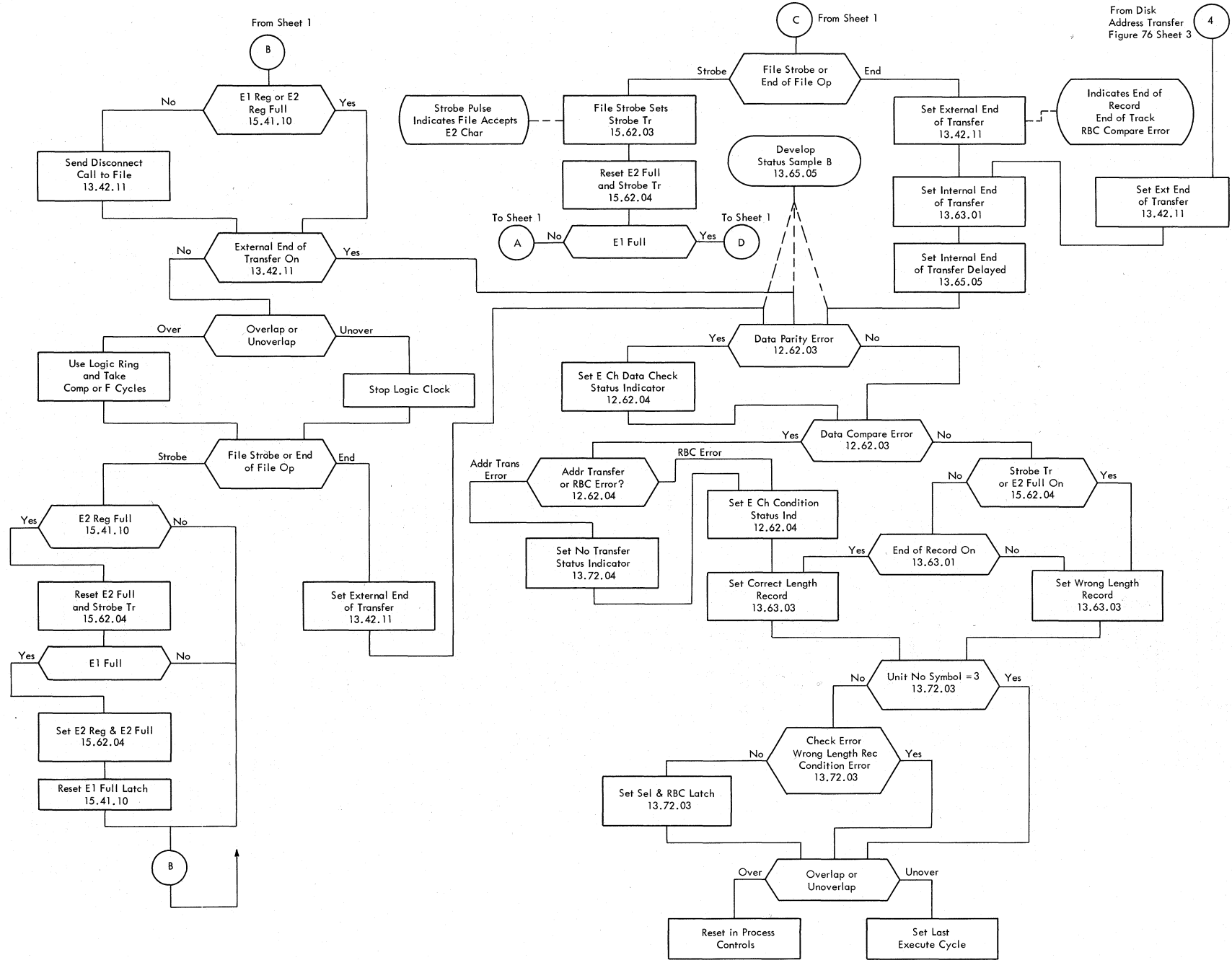


Figure 79. Write Operation (Sheet 2 of 2)

Disk Read (Figure 80)

Function

The disk read command causes the information that is available at the access arm in the file to read out and transfer to the CPU. The command is given in either the move or load mode. All information must be read in the same mode in which it is written.

During instruction read-out, the hundreds-position character of the X-control field defines the type of operation (overlap or unoverlap), as well as the data channel to use (E or F).

The tens position of the X-control field is always an F to specify a disk operation.

If the units position of the X-control field is a 1, a single record (200 characters) transfers to the CPU. A 2 in the units position of the X-control field causes an entire track (1000 characters) to read and transfer to the CPU.

The information that reads from the file is stored in the core storage unit of the CPU starting at the high order position that is specified by the B-field address which is in the B-address register at the end of second address transfer. The d-modifier character must be an R to specify a read or input operation.

Operation

If the address transfer is made correctly (see "Disk-Address Transfer" in this section), the transfer of file data to the CPU begins. Each time a character is sent to the CPU, a strobe pulse is sent to signify the presence of a character on the associated data channel (E or F). When the strobe is received, the character is placed in the proper data register (E-1 or F-1).

Assume that E-channel is used, the character transfers to the E-2 register, if E-2 is not full. When the E-2 register is full, the CPU starts an E-cycle (overlap) or a B-cycle (unoverlap) to transfer the character to core storage. This sequence of transfers continues until the end of the record or the end of the track.

The file unit detects the end of record or end of track and generates a file end of operation signal to send to the CPU. The file end of operation signal sets the external end of transfer in the CPU. The CPU stores the

character in E-1 or E-2 registers and senses a group mark with a word mark. The group mark with a word mark indication causes the end of record and internal end of transfer set. If the GM-WM is not sensed on this cycle, only the internal end of transfer sets, and a wrong length record indication is established at status sample B-time. The wrong length record also sets, if the GM-WM is sensed before external end of transfer.

With both internal and external transfers complete, the status sample B-pulse checks to determine whether a parity error occurred in the CPU or in the file unit. If an error occurred, the data check status indicator sets. The status sample B-pulse also checks for wrong length record. After the indicators are set, the CPU is released to continue with the stored program.

Disk-Write Address

Function

The write address command allows the customer engineer to write a single, indelible address on a disk. The write address key that is located on the disk control unit CE panel, must be ON, before the instruction is executed.

Operation

The write address operation (Figure 76) starts with a first address transfer (see "Disk Address Transfer" in this section). When the "addr tfr" gate to the file drops after the first address transfer, the write gate is brought up to allow the file to write the address that transferred during second address transfer.

At the end of the second address transfer, unit number 4 prevents setting "end of 2nd addr tfr" latch. This prevents the reset of "end of record," "int end of tfr," and "int end of tfr delayed." The file sends "end of op" after the address writes. This sets "ext end of tfr." Any parity error that is detected in the file, sets the data-check latch at status sample B-time. Status sample B also brings up the last execute cycle, if un-overlapped, to allow the program to proceed to the next instruction.

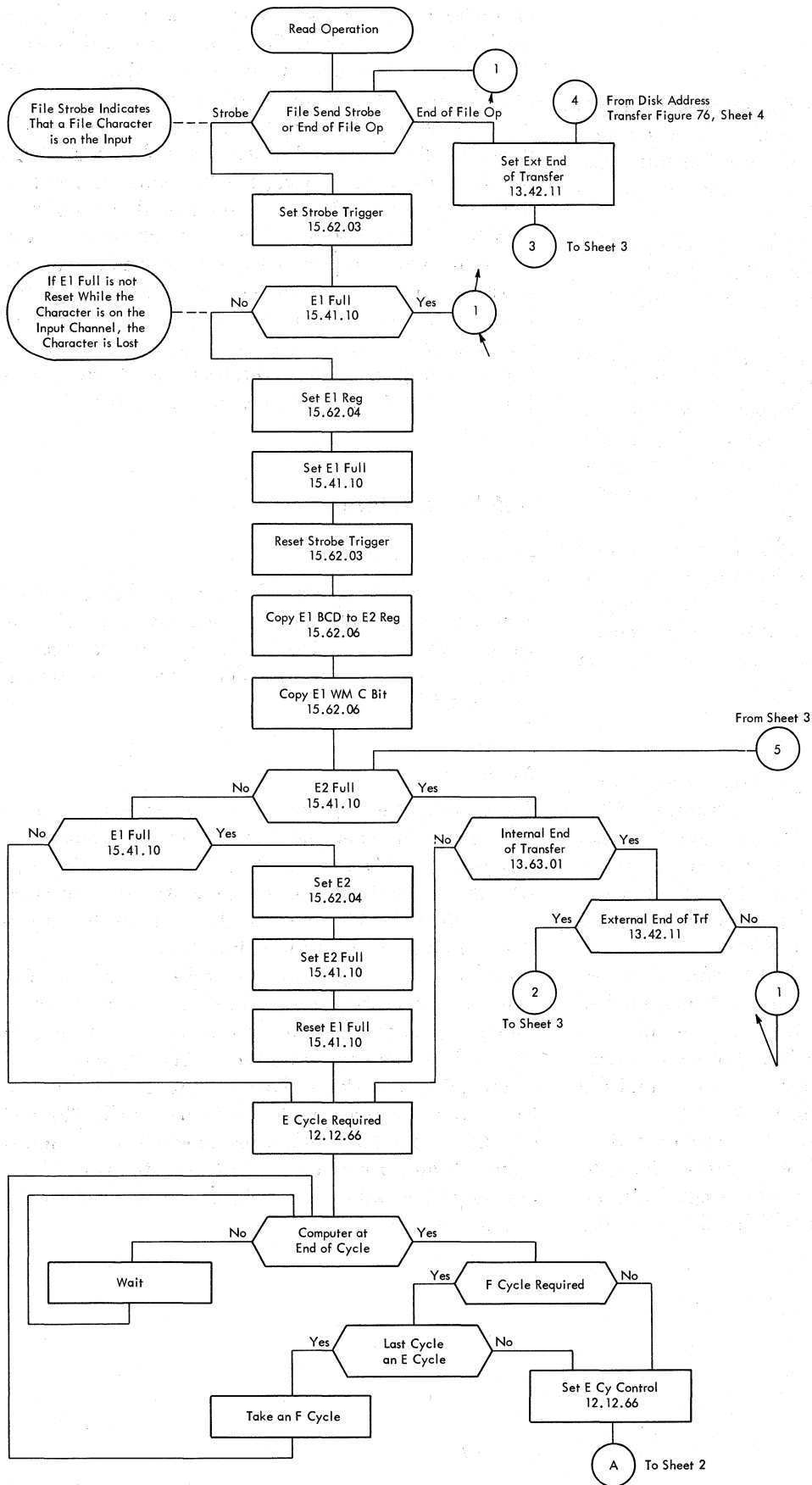


Figure 80, File Read Operation (Sheet 1 of 3)
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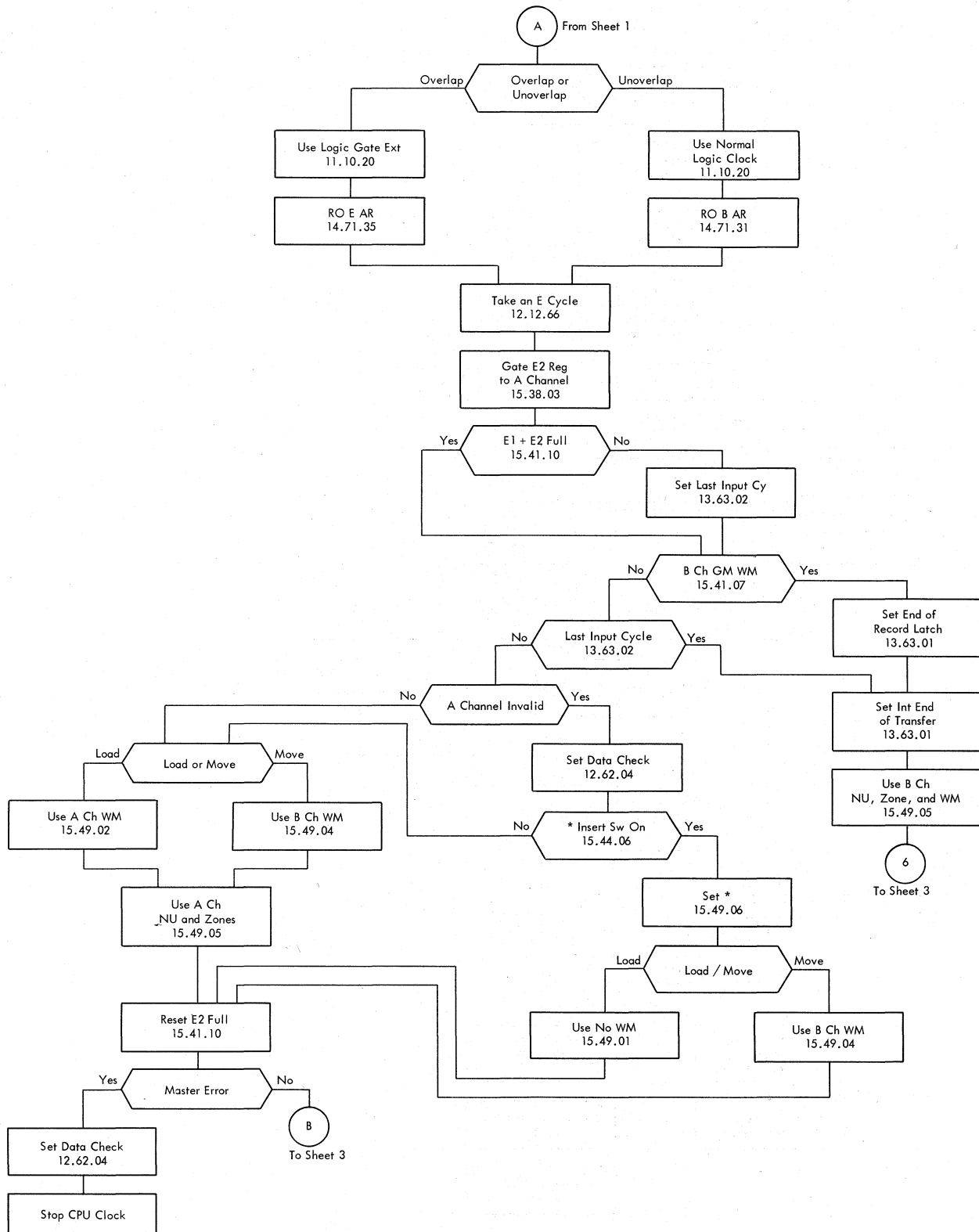


Figure 80. File Read Operation (Sheet 2 of 3)

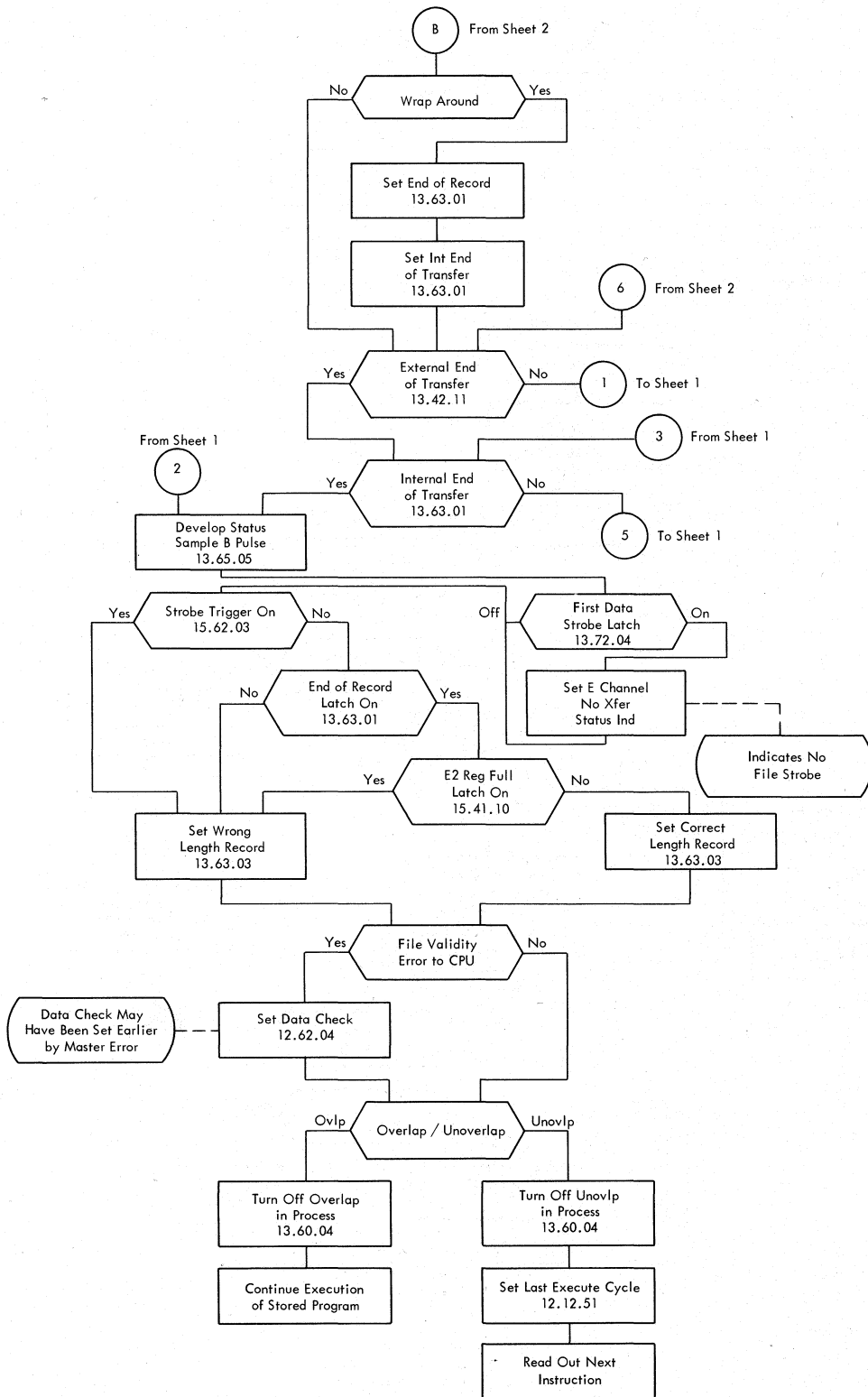


Figure 80. File Read Operation (Sheet 3 of 3)

1410 Data Processing System Operation with 1311 Disk Storage

The IBM 1410 Data Processing System controls as many as five IBM 1311 Disk Storage Drives per channel, one master and up to four satellites. The 1311-5 is the master module for the 1410 system. The 1311-2 is the satellite module and is powered and controlled through the master module.

Six instructions are used for basic 1311 operation; an additional five instructions are used for special features. Briefly, the instructions are used to:

1. Position 1311 read-write heads.
2. Read or write data.
3. Compare a 1410 data field with recorded 1311 data.
4. Check the accuracy of the recorded data.
5. Request and store 1311 address data (disk control field data) in 1411 core storage.

The operations performed by the 1311 disk storage are started by the 1410 instruction shown in Figure 81. The function of each part of the 1410 instruction is explained in the following section.

Instruction Format

Figure 81 shows the format for 1410-1311 disk storage control instructions.

Operation Code

Disk storage operations are initiated by a move (M) or load (L) instruction. The move instruction specifies that data are to be read or written in the seven-bit mode. The load instruction designates eight-bit mode. To insure the proper coding relationship between data in core storage and disk storage, data written with a move instruction must be read with a move instruction. Data written by a load instruction must be read with a load instruction. The two modes should not be mixed on the same track.

X-Control Field

The high-order character of the X-control field specifies which data transmission channel is to be used and

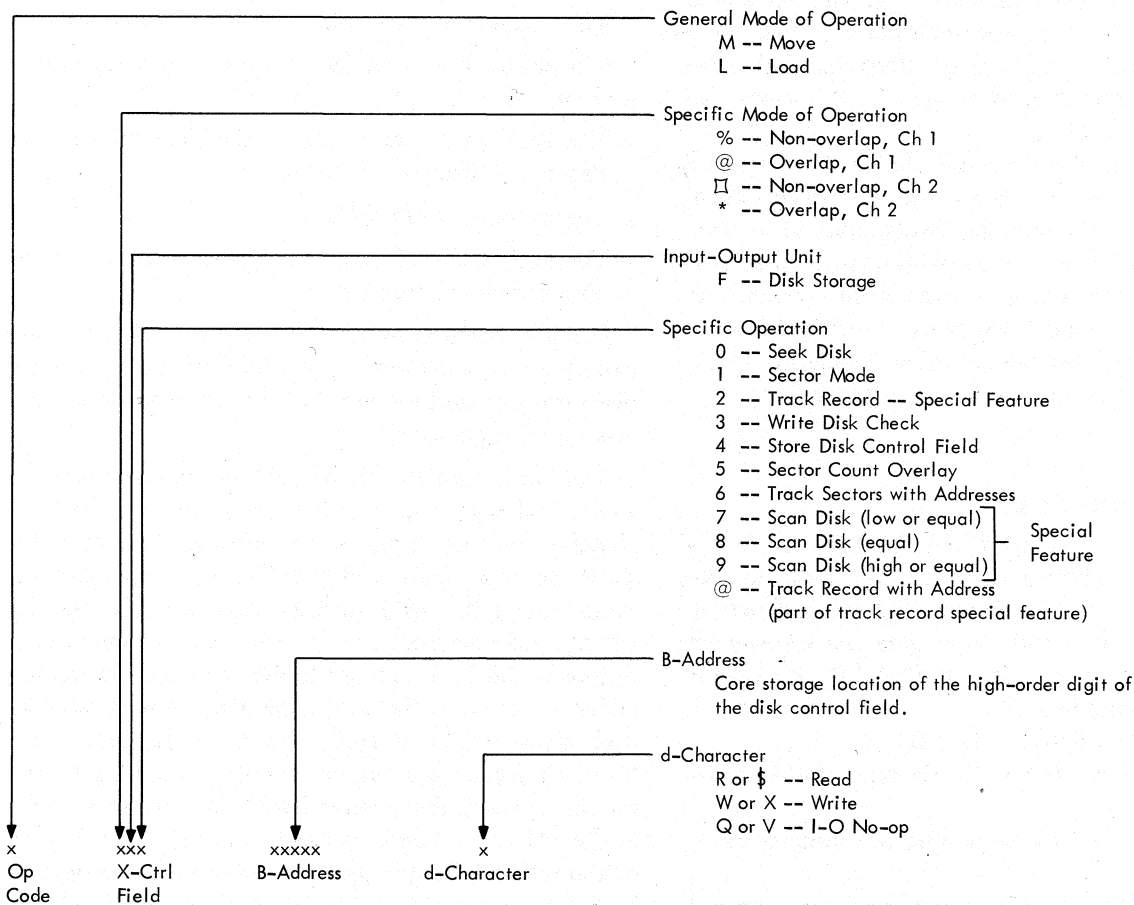


Figure 81. 1410 Op Codes for 1311

specifies the overlap or non-overlap status of the operation.

The second character (F) specifies 1311 disk storage as the input or output device for the operation.

The low-order position specifies which operation is to be performed (Figure 81).

B-Address

The B-address portion of the instruction addresses the high-order position of the disk control field. Data to be written on disk storage must be preceded in core storage by their disk control field. Data read from disk storage are placed in core storage following their associated disk control field. Disk control fields and data are separated in core storage by a group-mark/word-mark (GM-WM). A GM-WM must appear in the core storage position to the immediate right of the last character of the core storage data field to be written or the data area used to receive data from disk. The core storage location of a disk control field, with its related data area (and required GM-WM's) is determined by the user.

d-Character

This portion of the instruction specifies whether a read operation (R or \$) or a write operation (W or X) is to take place. Read or write instructions that define the limit of a core storage field or area by a GM-WM use the R or W d-character.

Read or write instructions that define the limit of a core storage field or area by the end-of-storage indication use the \$ or X d-character. Explanation of instructions in this publication assumes the use of the R or W d-character for reading or writing operations. The Q or V d-characters are used with the special feature priority processing r-o no-operation functions; Q indicates input status and V indicates output status.

1410/1311 Instructions

File operations are started when the 1411 issues the required signals, operation code, and data to the 1311. When the 1411 processes a 1311 file instruction, the signals, operation code, and data are transferred via the 1410 r-o interface. In a typical 1311 file operation the 1411 usually issues:

Control Signals to activate the 1311.

An Operation Code to specify the type of 1311 operation.

A Disk Control Word containing ten address characters.

The majority of the 1311 instructions are executed in three phases of 1411 operation. The first phase of

1411 operation is instruction read-out. During instruction read-out, the 1411 activates signal lines to the 1311, issues the operation code, and generates status sample A. With status sample A, the 1411 determines 1311 readiness. If the 1311 is not ready, file operation is discontinued and the 1411 processes the next instruction. If the 1311 is ready, the 1411 prepares to execute a second address transfer cycle.

The second phase of operation is the second address transfer cycle. During the second address transfer cycle, the 1411 uses the B-address to transfer the ten character disk control field to the 1311. The ten character B-field transferred to the 1311 is used to position read-write heads or to identify read or write data areas. To successfully complete the second address transfer, the 1411 must recognize the group mark with a word mark adjacent to the last B-field character and the 1311 must signal end of address transfer. The 1411 GM-WM causes internal end of transfer, and the 1311 end of address transfer signal causes end of second address transfer.

Following the second address transfer, the 1311 issues end op to the 1411 if:

The instruction is seek.

The instruction is modified by a Q or V op-modifier.

The 1311 is busy because the access mechanism is in motion.

The 1311 is not ready because the write address key is off when writing sector addresses.

The sector control field is 0.

The end op signal causes the 1411 to drop the file op line and end file operation.

If the instruction is store disk control field, the 1411 completes instruction read-out, inhibits the second address transfer, and follows the instruction read-out with input mode operation.

The third phase of 1411 operation is the data transfer cycle. Following the second address transfer, the 1411 switches to either input or output mode and waits for the 1311 to compare address. Failure to compare address causes the 1311 to issue end op. The end op signal causes external and internal end of transfer conditions in the 1411 ending the file operation. When the address compares, the 1311 generates a data strobe for each character transferred to or from the 1411. Data transfers continue in input or output mode until the operation end is determined by internal end of transfer in the 1411 or the end op signal from the 1311. Figure 82 shows the 1410 operation phases required to process 1311 instructions; 1311 file instructions are listed following Figure 82.

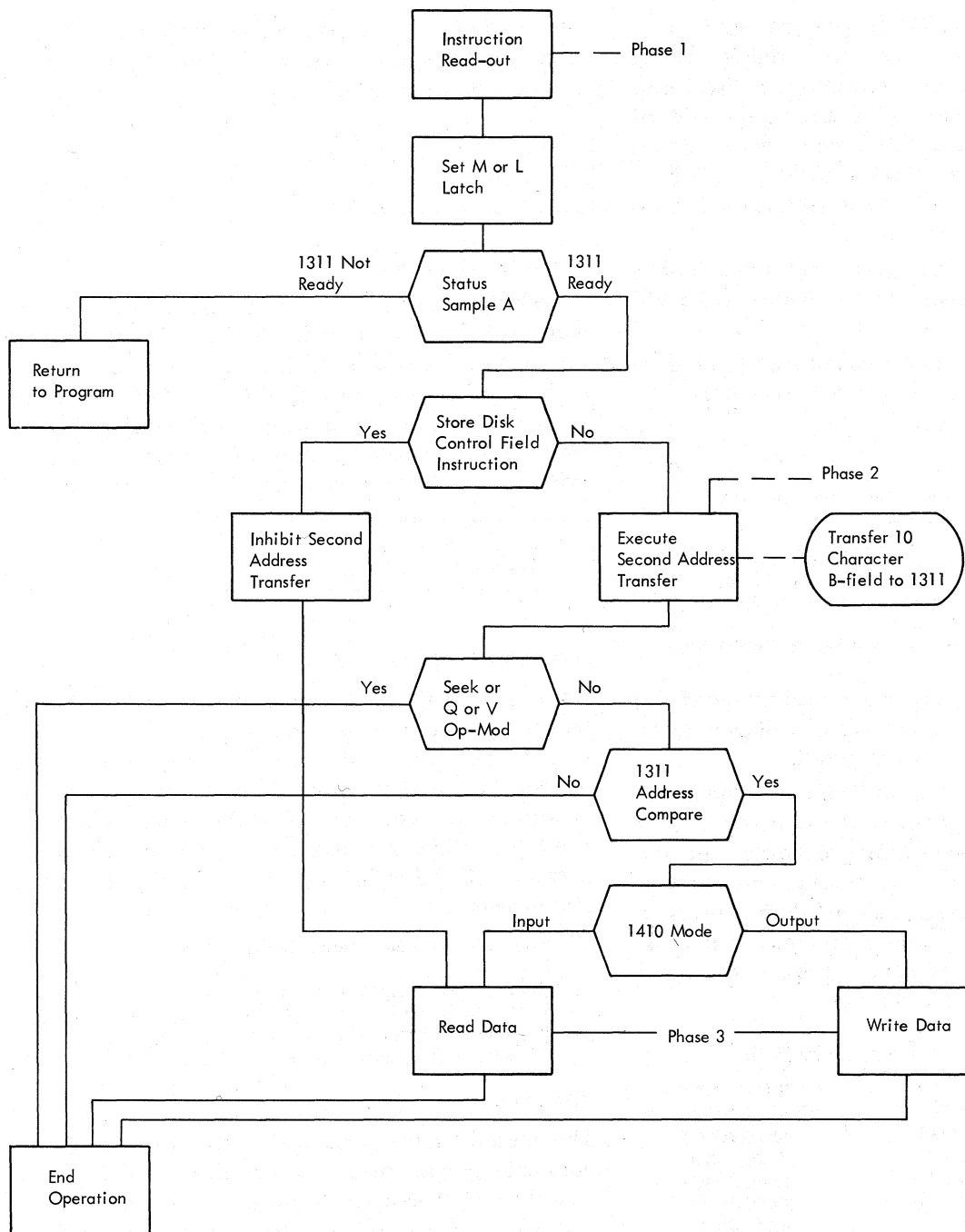


Figure 82. 1410-1311 Simplified Operation

Seek Disk

OP CODE	X-CONTROL FIELD	B-ADDRESS	d-CHARACTER
M or L	XF0	XXXX	R, \$, W, or X

This instruction is used to position an access assembly at a particular cylinder of a disk pack. The number of tracks the access assembly is to be moved is specified by the disk control field contained in core storage at the B-address. A CM-WM follows the disk control field in core storage. Any one of four d-characters (R, \$, W,

or X) may be used; their presence in the instruction is necessary only to establish a valid instruction length.

An interrupt on completion of a seek disk operation occurs if the system is equipped with the special priority feature and is in priority alert mode.

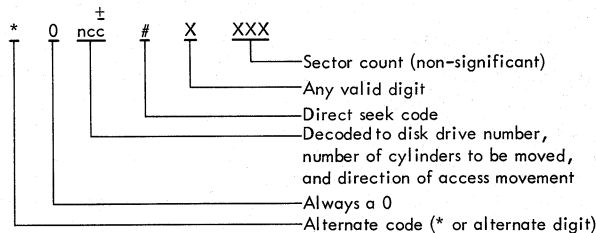
DIRECT SEEK

Direct seek operations move the access assembly directly from any position to the desired cylinder. The program must keep track of each access assembly location and provide the necessary information for direct

seek operations. Specifically, the program must calculate the direction of access movement, the number of cylinders to be moved, and generate the direct seek address to be used. Note that a direct seek address specifies a new access assembly location that is always in relation to the present location. If the present location is unknown, a return to home seek is used to establish a known cylinder location.

Average access time for direct seek operations is 150 milliseconds; maximum access time is about 250 milliseconds.

A direct seek address has a pound sign in its sixth digit position to specify a direct seek operation. The direct seek address format is:



The three digits (ncc) are determined by specifying the drive number and the number of cylinders to be moved and multiplying this number by 2.

The sign accompanying the fifth digit of a direct seek address indicates the direction of access motion. A plus sign or the absence of sign causes motion toward the center of the disks. A minus sign causes motion toward the outer edge of the disks. A signed digit appears in standard interchange BCD code as an alphameric character; in the following examples, 2 appears without sign and 6 appears as alphabetic O.

Example 1: Direct seek inward one cylinder.

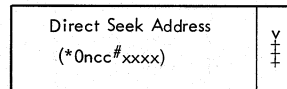
DISK DRIVE	DIRECT SEEK ADDRESS	DIRECT SEEK ADDRESS USING ALTERNATE CODE
0	*0002#0000	00002#0000
1	*0202#0000	20002#0000
2	*0402#0000	40002#0000
3	*0602#0000	60002#0000
4	*0802#0000	80002#0000

Example 2: Direct seek outward 53 cylinders.

DISK DRIVE	DIRECT SEEK ADDRESS	DIRECT SEEK ADDRESS USING ALTERNATE CODE
0	*0100#0000	00100#0000
1	*0300#0000	20100#0000
2	*0500#0000	40100#0000
3	*0700#0000	60100#0000
4	*0900#0000	80100#0000

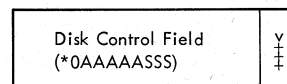
In both examples, alternate code direct seek addresses use position 1 to specify twice the number of the drive and positions three, four, and five to specify twice the number of cylinders the access assembly is to be moved.

The direct seek address format is used only for direct seek operations; it is not used to address data for read or write operations. The format is:



RETURN TO HOME SEEK

A seek that causes the access assembly to move outward past cylinder 00 (to home position) before moving to the desired cylinder is called a return to home seek. A seek instruction with a disk control field at the B-address causes a return to home seek. Average access time is 250 milliseconds; maximum access time is about 400 milliseconds. The format is:



SEEK DISK CHECKING

An unsuccessful seek becomes known when the subsequent read or write operation causes a condition signal. This can indicate that the access assembly is at an unknown location; a return to home seek is necessary to position the access assembly at the desired cylinder.

A typical series of instructions for programming non-overlap seek and subsequent read or write operations is as follows:

```

Branch if I-O channel status indicator ON
Seek Disk
Branch if I-O channel status indicator ON
Read or write disk } (Loop until channel
Branch on I-O channel busy } not busy)
Branch if I-O channel status indicator ON
  
```

SEEK OVERLAP

This special feature permits simultaneous seek operations to be programmed for any or all of the disk drives on a channel, thereby achieving a considerable savings in the time required for operations involving more than one disk pack. Direct seek or return to home seek instructions are used.

Sector Mode

OP CODE	X-CONTROL FIELD	B-ADDRESS	d-CHARACTER
M or L	XF1	xxxxx	R or W

This instruction transfers one or more sectors without sector addresses to or from a 1311 drive. The number of sectors transferred is determined by the sector count of the disk control field.

The disk control field (*0AAAASSS) is sent to the 1311-5 from the computer. The format is:

Disk Control Field	V ⋮	One to 200 Sectors	V ⋮
--------------------	--------	--------------------	--------

The 1311-5 decodes *0AAAAA to select the correct disk drive and read-write head, stores the core sector address in its sector address register, stores the sector count in its sector count register, and stores the alternate code position.

The addressed 1311 then begins a search of the selected surface for a sector address that matches the contents of the sector address register. Sector addresses on the track are compared to the sector address register until a match occurs or until two index pulses have been sensed. An index pulse indicates the beginning of a track. If a match does not occur before two index pulses are sensed, the 1311-5 transmits an end signal and a condition signal to the computer. If a match does occur, data are transferred.

The total number of sectors to be transferred is controlled by the contents of the sector count register. As each sector is transferred, the contents of the sector count register is decremented by one, and the sector address register is incremented by one. The next sector address is then compared with the updated sector address register. When the sector count register becomes 000, the operation terminates.

The incrementing of the sector address register at the end of the last sector on that track causes the next read-write head (for the next track in the cylinder) to be selected. Following the selection of the new read-write head, the first sector address on disk is compared to the sector address register. If it matches, sectors of data continue to be transferred. Upon completion, the 1311-5 sends an end signal to the computer. If any sector address does not match, the 1311-5 transmits an end signal and a condition signal to the computer.

Transfer of data is stopped by:

Sensing a CM-WM in storage.

Reducing the sector count register in the 1311-5 to 000.

End of cylinder.

Failure of the sector address to compare equal with the updated address register contents.

Records less than 90 or 100 characters in length must be filled out with dummy characters to avoid wrong length record (WLR) indication.

If more sectors are to be transferred when the end of a cylinder is reached, the sector address register is incremented to the first sector address in the next cylinder. This address does not compare equally because the access mechanism has not moved to the new cylinder. The non-compare causes the 1311-5 to send an end signal and a condition signal to the computer.

Additional seek and sector instructions are necessary to move the access assembly and transfer the remaining sectors of information in the new cylinder.

Write Disk Check

OP CODE	X-CONTROL FIELD	B-ADDRESS	d-CHARACTER
M or L	XF3	XXXXX	W or X

The write disk check operation provides a method of checking data previously written on disk. Data recorded on disk storage are read and compared bit for bit by the 1311-5 with the data in core storage previously written on disk.

The type of write check operation (sector mode, track sectors, track record, or sector count overlay) performed depends on the preceding mode of operation; if a sector mode operation preceded the write disk check instruction, it will be a write disk check in sector mode.

An unsuccessful write disk check causes the data check I-O channel status indicator in the computer to be set on.

The op code, B-address, and the d-character for the write disk check instruction must be the same as the operation code, B-address, and d-character of the instruction used to write the data that are to be checked.

Store Disk Control Field

OP CODE	X-CONTROL FIELD	B-ADDRESS	d-CHARACTER
M or L	XF4	XXXXX	R

This instruction causes the ten characters in the 1311-5 registers (*0AAAAAASSS) to be transferred to the computer and stored in the location specified by the B-address. This instruction may be used after any 1311 operation. The format is:

Disk Control Field (*0AAAAAASSS)	V ⋮
----------------------------------	--------

Track Sectors with Addresses

OP CODE	X-CONTROL FIELD	B-ADDRESS	d-CHARACTER
M or L	XF6	XXXXX	R or W
Move mode - 2,120 characters			
Load mode - 1,920 characters			

This instruction transfers a full track of data with sector addresses to and from 1311 disk storage. The format is:

Disk Control Field	V ⋮	Sector 0 Address	Sector 0	Sector 1 Address	Sector 1	Last Sector (19)	V ⋮
--------------------	--------	------------------	----------	------------------	----------	------------------	--------

The core sector address portion of the disk control field transferred to the 1311-5 is compared to the sector addresses on the associated track. When a match occurs, the transfer of data is initiated by the next track index pulse. The transfer starts with the first sector address on the selected track. Transfer continues until 20 sectors of addresses and data have been transferred.

This mode of operation permits sector addresses to be read, rewritten, or changed.

For a write track sectors with addresses operation, desired or fictitious records must be supplied for each existing sector area in core storage to insure that sector addresses will be properly written.

The sector count field must be 020 for this operation. The 1311-5 sector address register is not incremented for this operation. If two index pulses are sensed before an address match occurs, an end signal and a condition signal are sent to the computer.

If the GM-WM is sensed prior to the disk end-of-track, the WLR indicator in the computer is set on and data transfer stops. If disk end-of-track is sensed prior to the GM-WM in core storage, data transmission stops and the WLR indicator is set on.

NOTE: The write address key light, located on the 1311-5, must be on to write track sectors with addresses.

Track Record with Address

OP CODE	X-CONTROL FIELD	B-ADDRESS	d-CHARACTER
M or L	XF@	xxxxx	R or W

This special feature instruction transfers 2,980 seven-bit or 2,682 eight-bit characters to or from 1311 disk storage as a single track sector record with sector address. The format is:

Disk Control Field	Y +	Sector Address	Track Sector (2980 or 2682 Characters)	Y +
--------------------	-------------	----------------	---	-------------

The write address key light must be on for a write track record with address operation.

The sector count specified in the disk control field must be 001. The core sector address for the track record is written in the normal first address position after the index pulse, and may be any sector address in the block of 20 that designates the normal sector addresses on that track. Only one sector address is recorded.

Data transfer begins at index pulse time after a successful sector address compare. If the sector address does not match, a condition signal is sent to the computer.

Tracks adjacent to a track having track record format must also have track record format if they are to be used.

If the GM-WM is sensed before the end-of-track, the WLR indicator in the computer is set on and the operation terminates. If the disk end-of-track is sensed before the GM-WM, the WLR indicator is set on and the operation stops.

Track Record

OP CODE	X-CONTROL FIELD	B-ADDRESS	d-CHARACTER
M or L	SF2	xxxxx	R or W

This instruction is part of the track record with address special feature. It functions the same as the track record with address instruction except that the address is not handled. The format is:

Disk Control Field	Y +	Track Sector (2980 or 2682 Characters)	Y +
--------------------	-------------	---	-------------

One disk revolution is avoided because the data transfer begins immediately after a successful sector address compare.

Sector Count Overlay

OP CODE	X-CONTROL FIELD	B-ADDRESS	d-CHARACTER
M or L	XF5	xxxxx	R or W

Read sector count overlay operations enable data recorded on disk to specify the number of sectors to be transferred. The format is:

Disk Control Field	Y +	xxx	Number of sectors read, less one, is specified by first three positions	Y +
--------------------	-------------	-----	---	-------------

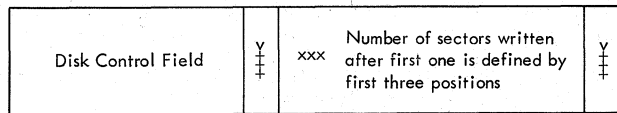
This facilitates operations involving an unknown number of sectors. The sector count must be at least one.

The first three digits of the first sector (specifying the additional number of sectors to be read) are automatically placed in the sector count register in the 1311-5 when the first sector is read. This register is decremented by one for each additional sector transferred until it reaches 000 causing the operation to terminate. The first three digits of the first sector are read into computer core storage in the usual manner.

Space must be provided in the B-field for the maximum number of records expected. Fewer records cause a WLR indication. A WLR indication can be expected when the length of the record is unknown.

A write sector count overlay operation is the same as a sector mode operation with the following differ-

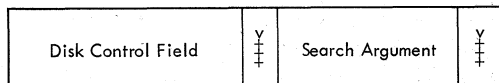
ence. As the first three digits of the first record are written on disk, they are also placed in the sector count register in the 1311-5. This allows the first three data characters to specify the additional number of sectors to be written. The number of sectors written is the value of the first three data digits plus 1. The sector count in core storage must be at least one. The format is:



Scan Disk

OP CODE	X-CONTROL FIELD	B-ADDRESS	d-CHARACTER
M or L	XF7 (Low or equal) XF8 (Equal) XF9 (High or equal)	xxxxx	W

This special feature operation scans a specified number of sectors for a compare with a search argument in core storage up to one sector in length. The format is:



The first sector to be scanned and the number of sectors to be scanned are specified in the disk control field of the scan disk instruction. The search argument follows this disk control field in core storage. Scanning must be done in the same mode (M or L) as that in which the sectors were recorded. Data recorded in track record mode cannot be scanned.

The argument in core storage is the B-field and the data on the disk pack are the A-field. A GM-WM placed after the last character in the search argument conserves storage space if the search argument is less than one sector in length. Skip codes (\$) in core storage can be used to blank out character positions not used in the search argument:

\$\$A\$123\$\$456

After a successful sector address compare, the argument from the 1410 is compared character by character with the data from disk storage (skip codes are not compared).

A scan operation terminates when:

The desired sector is found; the sector count register in the 1311-5 may or may not have reached 000.

End of cylinder occurs before completion of the scan causing a condition signal to the computer; the sector count register will not contain 000.

A scan is completed without finding the desired data; the sector count register will be 000.

After a successful scan, the address of the sector that satisfies the search argument is in the sector address register where it is available to a store disk control field operation. The result of the scan is learned by testing the computer compare indicators (Hi-Lo-Eq) with the appropriate branch if indicator on instruction.

High indicates that the B-field (argument) is higher than the A-field (disk storage). Low indicates that the B-field is lower than the A-field. Scan operation cannot be executed in overlap mode; overlapped scan operation causes an instruction check.

I-O No Operation

OP CODE	X-CONTROL FIELD	B-ADDRESS	d-CHARACTER
M or L	xFx	xxxxx	Q or V

This instruction is used on a 1410 system equipped with the priority processing special feature. Its primary purpose is to set the I-O channel status indicators for an I-O unit, so that the status of the unit can be tested by a branch if I-O channel status indicator on instruction: R(I)d or X(I)d. No data transfer occurs with this instruction; for example, assume that a 1311-5 with the seek overlap special feature has issued seek instructions to several access assemblies. The first access assembly to reach its destination will cause an interrupt to the system. It is necessary to determine which access assembly caused the interrupt.

The I-O no disk control field selects a particular access assembly. A branch on busy instruction (R(I)d) is used to determine if that access assembly is busy. If the access assembly is in motion, a busy condition will result. If the access assembly is not in motion, a busy condition will not result (seek completed) and it can be assumed that the access assembly addressed is the one that caused the interrupt. Each of the moved access assemblies can be tested in this manner.

The seek complete signal that caused the interrupt is terminated by a read, write, or I-O no operation instruction that addresses the access assembly that caused the signal.

When the I-O no op instruction is being used to set the I-O channel status indicators, the op code can be M or L, the units position of the X-control field can be any valid character, and the d-character can be either Q or V. Q is used for input status; V is used for output status.

1410 Operation

All 1410-1311 disk instructions can be divided into two or three phases of 1410 operations:

Instruction Read-out.

Second Address Transfer (occurs for all 1311 instructions except store disk control field).

Read or Write Data Transfer (occurs for all instructions except seek, or those instructions with a Q or V op-modifier).

Figure 82 shows the phases of 1411 operation required to execute 1311 instructions.

Instruction Read-out

To start a 1311 operation, the 1411 must read out a 1311 instruction. During M or L instruction read-out, the I-ring is advanced rapidly from I-op to I-3. The channel select character is read out and stored in the channel select register at I-3 time. Next, the selected channel interlock, move or load latch, is tested to determine if the program has properly interrogated the channel status indicators. Instruction read-out is shown on Figure 83. If the interlock is on, master error stops the CPU at I-3 time, with the system check I-O interlock on. If the channel interlock is off, a channel reset is generated; as a result, the channel control and status latches are reset.

Following channel reset, the unit select character is read out and stored in the unit select register. The unit select character for file is F. At I-5 time, the unit number character is read out and stored in the unit number register. The unit number register outputs are decoded in the 1311. The character decoded determines the type of file operation. Figure 81 shows the character required for each type of file operation.

Starting with I-6 time and ending with I-10, the five character B-address is read out and stored in the address register. The B-address refers to the starting location of a ten character field; the ten character field is the disk control field. The disk control field is a ten character address that is used by the 1311 file control unit to address disk storage. The disk control field is transferred to the 1311 during the 1411 second address transfer.

At I-11 time, the op-modifier character is read out and stored in the op-mod register; in addition, the move or load latch is set. Following I-11, the 1411 generates status sample A. With the file selected, status sample A is used to determine if the file is ready. If the file is not ready, the selected channel not ready status causes last execute cycle. Last execute cycle sets the I-cycle control latch causing the CPU to process the next instruction. If no status occurs, the 1411 proceeds to the next phase of operation.

Second Address Transfer

The second phase of 1410 operation is the second address transfer (Figure 82). During the second address transfer, the 1411 operates in output mode to transfer the ten character disk control field to the 1311. The second address transfer is the last phase of 1411 operation for seek and instructions modified by Q or V. Instructions used to read, write, compare, or write check data follow the second address transfer cycle with either read or write data transfers.

The second address transfer latch is set to start the second address transfer cycle if:

The file is ready.

The unit number register is not set to 4.

Second address transfer is shown on Figure 84.

If the unit number register is set to 4, the instruction in process is store disk control field; the 1311 does not need a disk control field to execute this instruction. Because the disk control field is not required, the second address transfer is inhibited when the unit number register contains a 4.

Any instruction, except store disk control field, requires a disk control field; therefore, the second address transfer follows instruction read-out. When second address transfer latch is set, its output is used to force output mode. In output mode, the 1411 takes two E-cycles to fill the E registers with the first two disk control field characters. When E-2 is full, the 1411 issues a file start gate to the 1311. Receipt of the file start gate signals the 1311 to start an address transfer operation.

During a 1311 address transfer, the disk control unit issues one data strobe for each character transferred from the read-write bus into storage. Ten disk control characters must be transferred to successfully complete the address transfer. Data flows from 1411 core storage, through the E registers, onto the 1410 read-write bus and into the 1311 I-O register.

SECOND ADDRESS TRANSFER END CONDITIONS

After the tenth 1411 E-cycle, the 1411 recognizes the GM-WM; this causes the 1411 to set internal end of transfer. With internal end set, the 1411 waits for the 1311 end of address transfer or end op signal.

If the instruction processed is seek, or modified by a Q or V op-modifier, or if the 1311 is busy, not ready, or the sector count equals zero, the 1311 issues end op to set the 1411 external end of transfer latch. When internal and external end of transfer conditions AND, the 1411 generates status sample B and drops file op. Thus, for these conditions, the file operation ends after the second address transfer cycle.

If the instruction processed is not seek or not modified by the Q or V op-modifier (or the file is not ready,

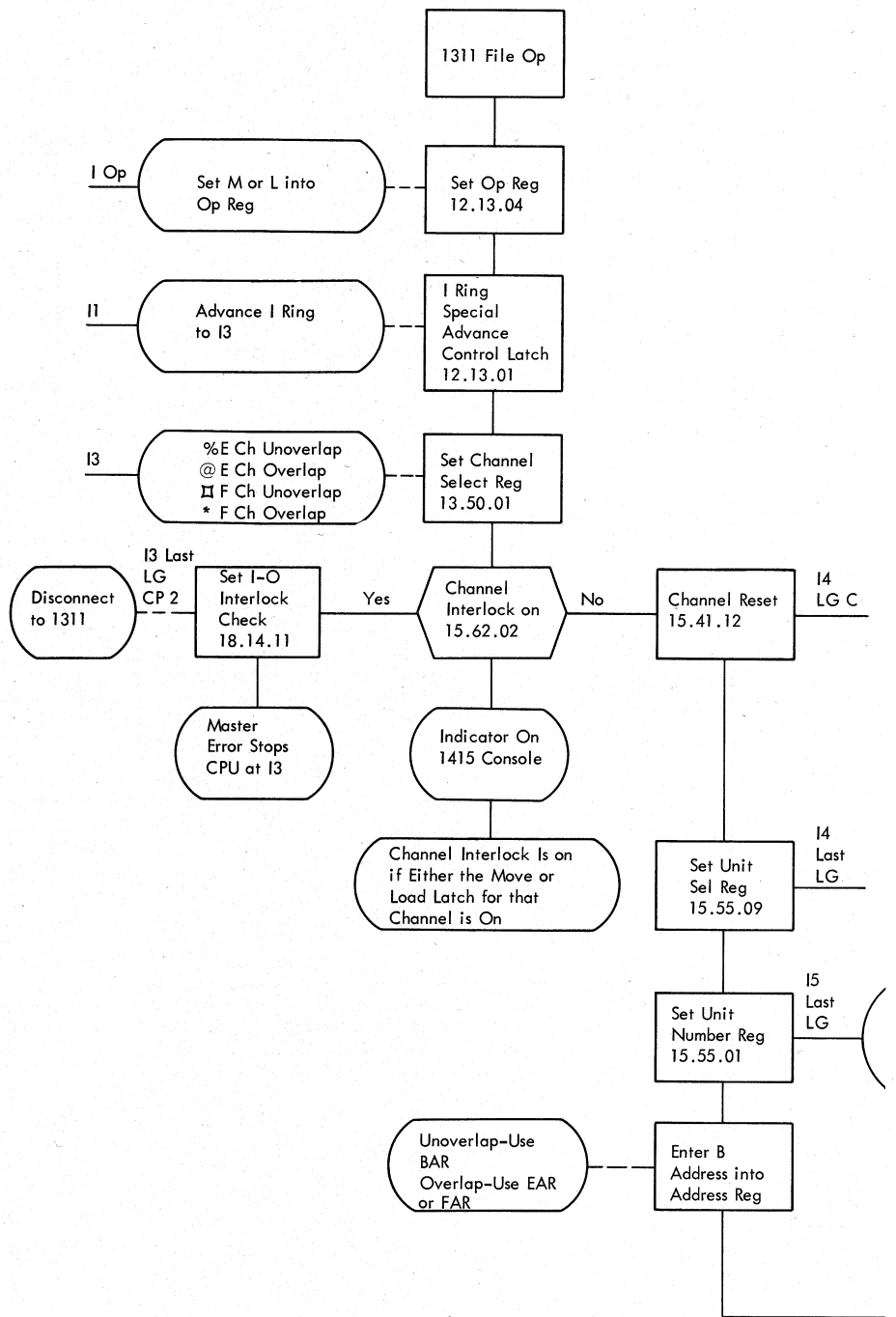
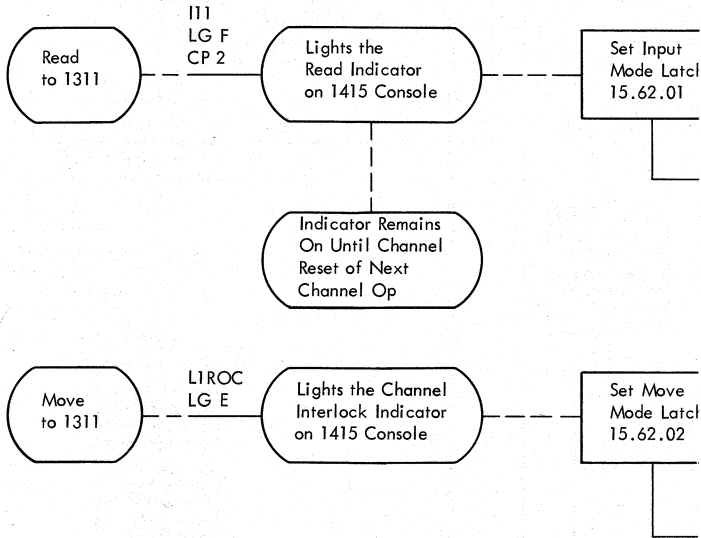
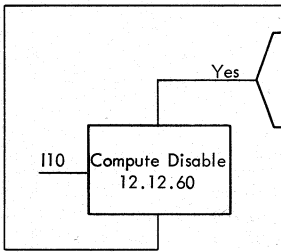
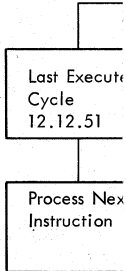
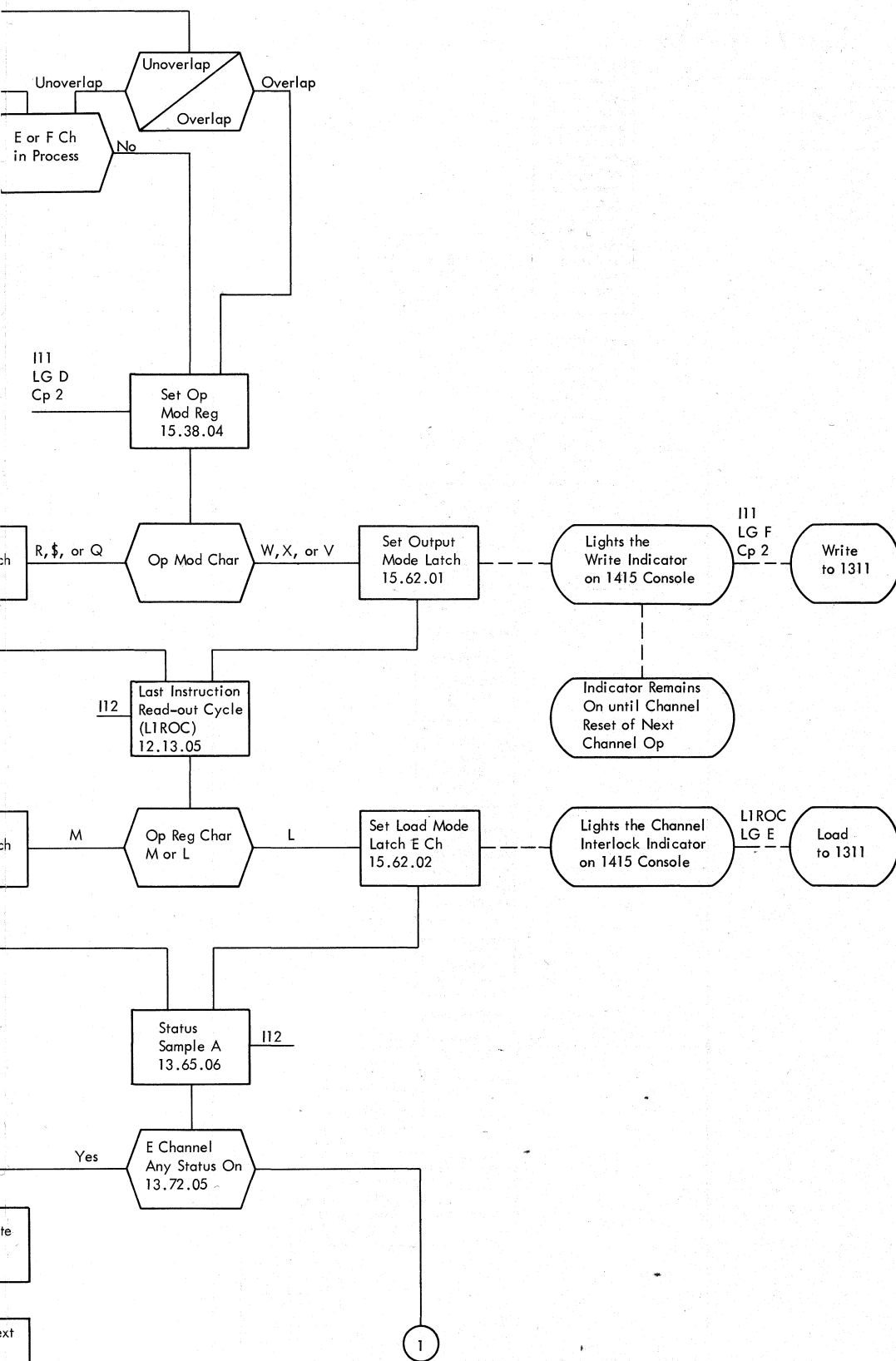


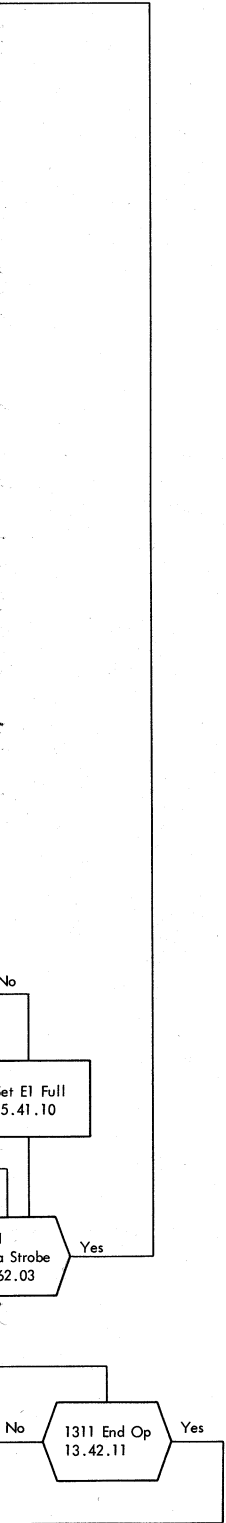
Figure 83. Instruction Read-Out

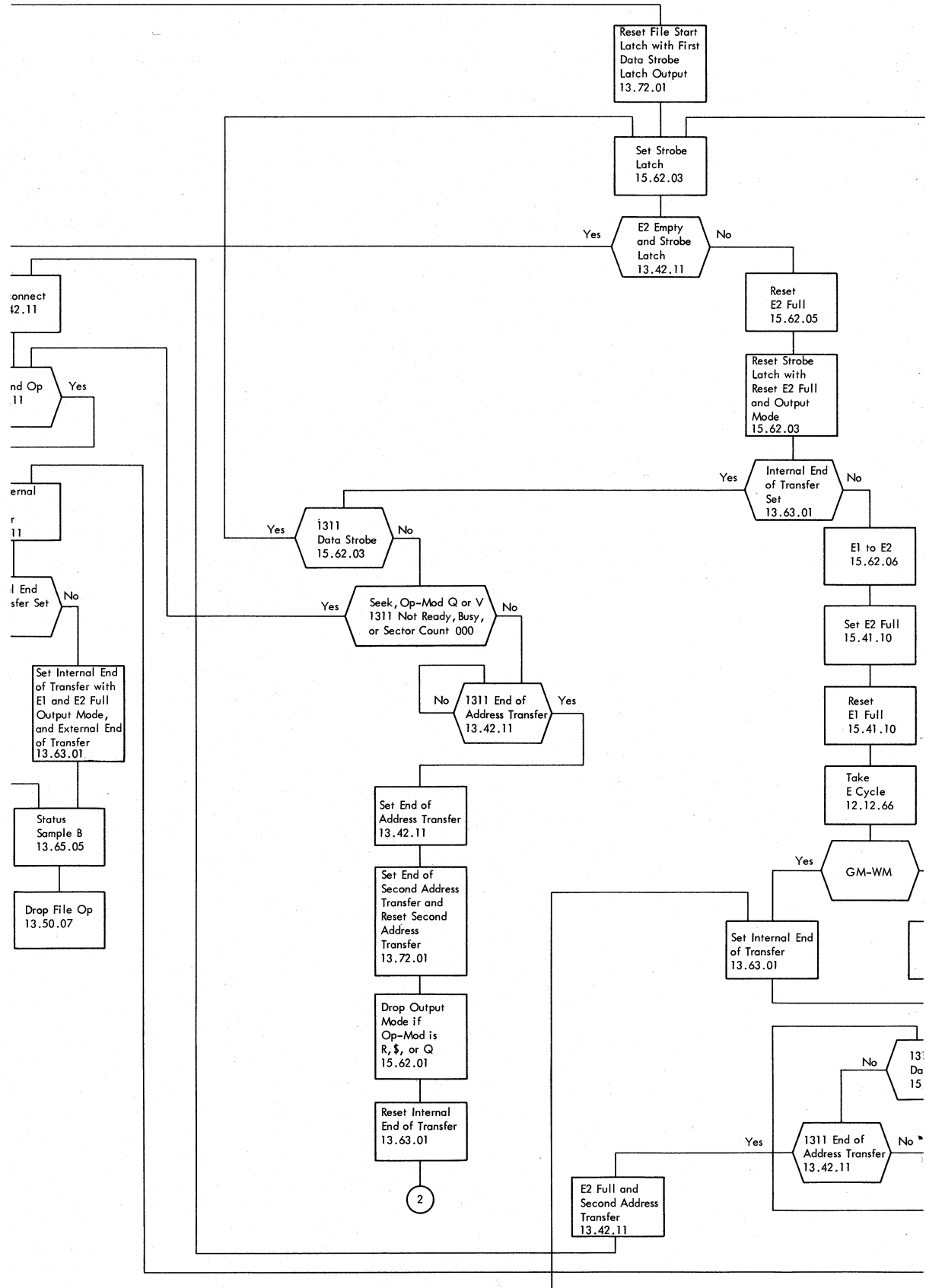


File Op to 1311.
Unit Number Register
Output to 1311.









Connect 12.11

End Op 11

Yes

External

Transfer Set

No

Set Internal End of Transfer with E1 and E2 Full Output Mode, and External End of Transfer 13.63.01

Status Sample B 13.65.05

Drop File Op 13.50.07

E2 Full and Second Address Transfer 13.42.11

2

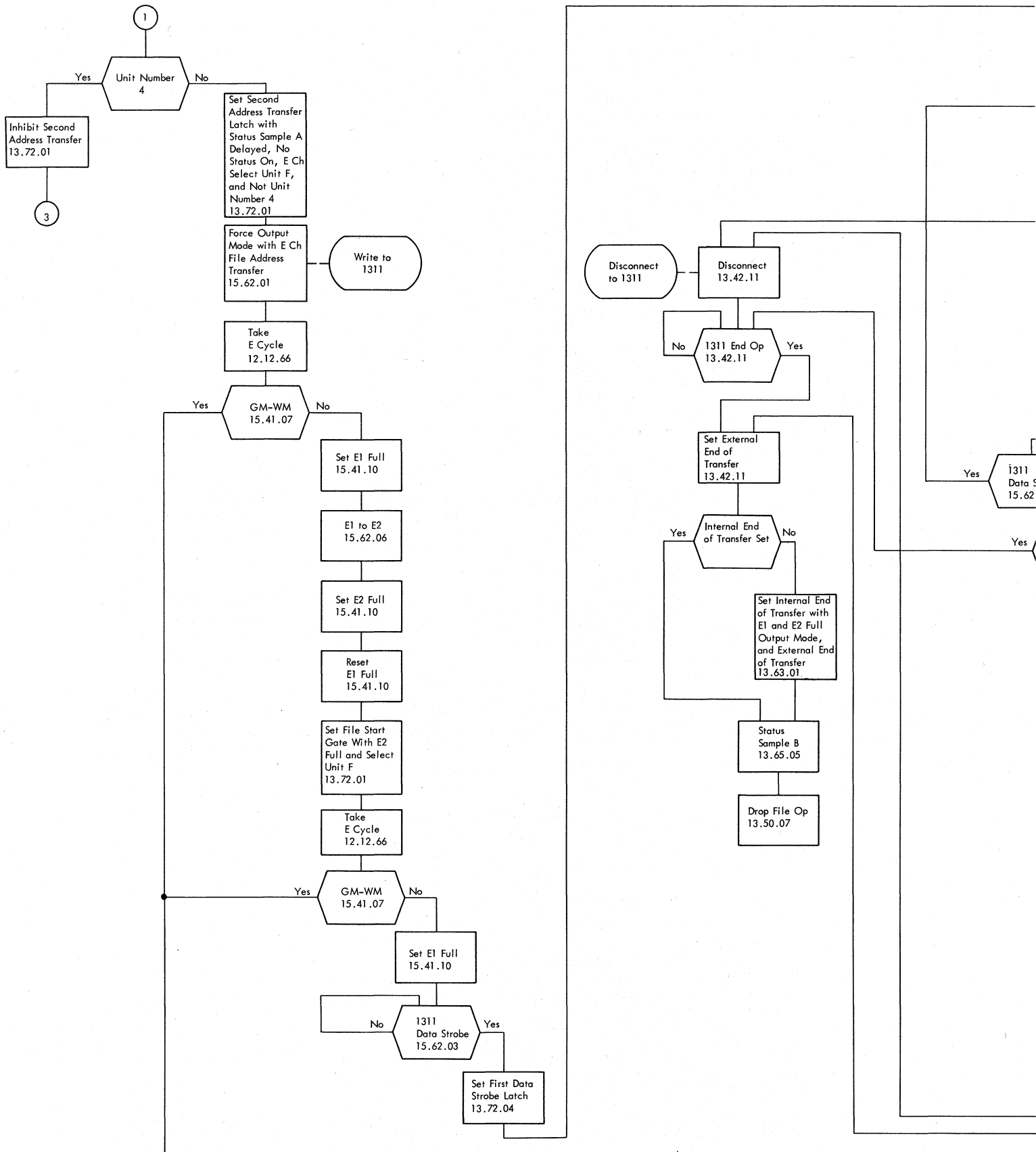


Figure 84. Second Address Transfer

busy, sector count is not 000) the 1311 issues end of address transfer. End of address transfer causes the 1411 second address transfer latch to reset. Because end op was not issued, the 1411 external end of transfer is not set; therefore, the 1411 prepares to continue file operation. The next phase of 1411 file operation is either a read or a write data transfer; this is determined by the 1311 file instruction op-modifier.

If the 1411 B-field is too short, internal end of transfer with E-1 and E-2 empty occurs prior to receipt of the 1311 end of address transfer or end op signals. In this case, the 1411 issues a disconnect to the 1311; disconnect then causes the 1311 to issue end op. The 1411 external end of transfer latch is set with end op; this causes the 1411 to generate status sample B and end file operation.

If the B-field is too long, there are two ways to end file operation. If the 1311 issues end of address transfer prior to internal end, E-2 full and end of address transfer cause the 1411 to issue disconnect. The 1311 issues end op in response to the disconnect; end op causes external end of transfer to set. External end of transfer with E-1 and E-2 full causes the 1311 internal end of transfer latch to set. Internal and external end of transfer cause the 1411 to generate status sample B and end file operation.

If the 1311 issues end op prior to internal end, the disconnect is not issued. End op causes the external end of transfer latch to set; external end of transfer with E-1 and E-2 full cause the internal end of transfer latch to set. Internal and external end of transfer cause the 1411 to generate status sample B and end file operation.

Data Transfers

During any operation, data transfers between the 1311 and 1411 are synchronized by data strobes generated in the 1311. The direction of data transferred is determined by the mode of 1411 operation. File instructions with the R or \$ op-modifiers cause the 1411 to operate in input mode; file instructions with the W or X op-modifiers cause the 1411 to operate in output mode. Data transfers can be terminated by the 1311 or the 1411.

With the exception of the store disk control field instruction, the remaining read or write instructions are preceded by a second address transfer. Before any data transfer, the 1311 uses the disk control field to select the correct access mechanism and to verify the sector address. No data are transferred to or from the disk until the disk control field is successfully compared with the disk address.

READ DATA TRANSFER

Read data operations start after the 1311 end of address transfer signal resets the 1411 second address transfer and internal end of transfer latches; as a result, the 1411 sets the input mode latch and waits for the 1311 to compare address. If the disk address does not compare, the 1311 issues end op; this signal sets the 1411 external end of transfer latch. External end of transfer causes the 1411 to force last input cycle and to set the internal end of transfer latch. When internal and external end of transfer AND, the 1411 generates status sample B to complete the file operation. Input mode operation is shown in Figure 85. If the disk address compares, the 1311 issues one data strobe for each character placed on the read-write bus. The read data is transferred from the read-write bus into E-1, and from E-1 to E-2; the contents of E-2 are stored in core storage with each E-cycle. Data transfers and E-cycles continue until either the 1311 or the 1411 causes the operation to end.

Several read data transfer end conditions are possible. In most operations, after the last data strobe, the 1411 receives end op prior to the internal end of transfer, the 1411 then takes one more E-cycle to detect end of storage or end of field. End of field or end of storage causes the internal end of transfer latch to set. When internal and external end of transfer AND, status sample B is generated to complete the file operation. If end of field or end of storage does not occur on the last E-cycle, "last input cycle" causes the internal end of transfer latch to set. When internal and external end of transfer AND, status sample B is generated to complete the file operation.

If 1411 end of storage or end of field condition causes the internal end of transfer latch to set before the end op signal, the 1411 issues disconnect and waits for the 1311 end op signal. End op sets the external end of transfer latch; with external and internal end of transfer latches set, the 1411 generates status sample B to complete the file operation.

WRITE DATA TRANSFER

Write data operations start after the 1311 end of address transfer signal resets the 1411 second address transfer and internal end of transfer latches. The W or X op-modifiers cause the output mode latch to set. In output mode, the 1411 takes two E-cycles to fill the E registers. The 1411 waits for data strobes from the file to start the write data transfers. Output mode operation is shown in Figure 85.

Before issuing data strobes and writing data, the 1311 uses the disk control field to compare address. If the address does not compare, the 1311 issues end op. End op sets the 1411 external end of transfer latch;

with external end of transfer set and E-1 and E-2 full, the 1411 sets internal end of transfer. When internal and external end of transfer AND, the 1411 generates status sample B to end the file operation.

If the address compares, the 1311 issues data strobes to maintain data transfer synchronization with the 1411. Data is transferred until either the 1311 or the 1411 ends the write operation.

In most cases, the 1411 recognizes end of storage or end of field and sets the internal end of transfer latch. If E-1 and E-2 are empty, the 1411 issues disconnect. If a scan operation is not in process, the 1311 issues end op to set the 1411 external end of transfer. Internal and external end of transfer cause the 1411 to generate status sample B to end file operation.

If a scan operation is in process and the scan conditions have not been met, the 1311 issues scan restart

instead of end op. Scan restart causes the 1411 to continue in output mode and to repeat the record transfer. To transfer the same record in response to the scan restart signal, the 1411 uses the AAR contents on the first E-cycle; as a result, the EAR is updated for the remaining E-cycles and this assures the same record is transferred to the 1311 for each scan. The scan operation ends when the scan conditions have been met or if the sector count is 0. The 1311 signals end with the end op signal; end op causes the 1411 to complete the file operation. When the 1311 issues end op prior to internal end of transfer, the end sequence starts when the external end of transfer latch is set. External end of transfer, E-1 and E-2 full, and output mode AND to set internal end of transfer. Internal and external end of transfer cause the 1411 to generate status sample B to complete the write operation.

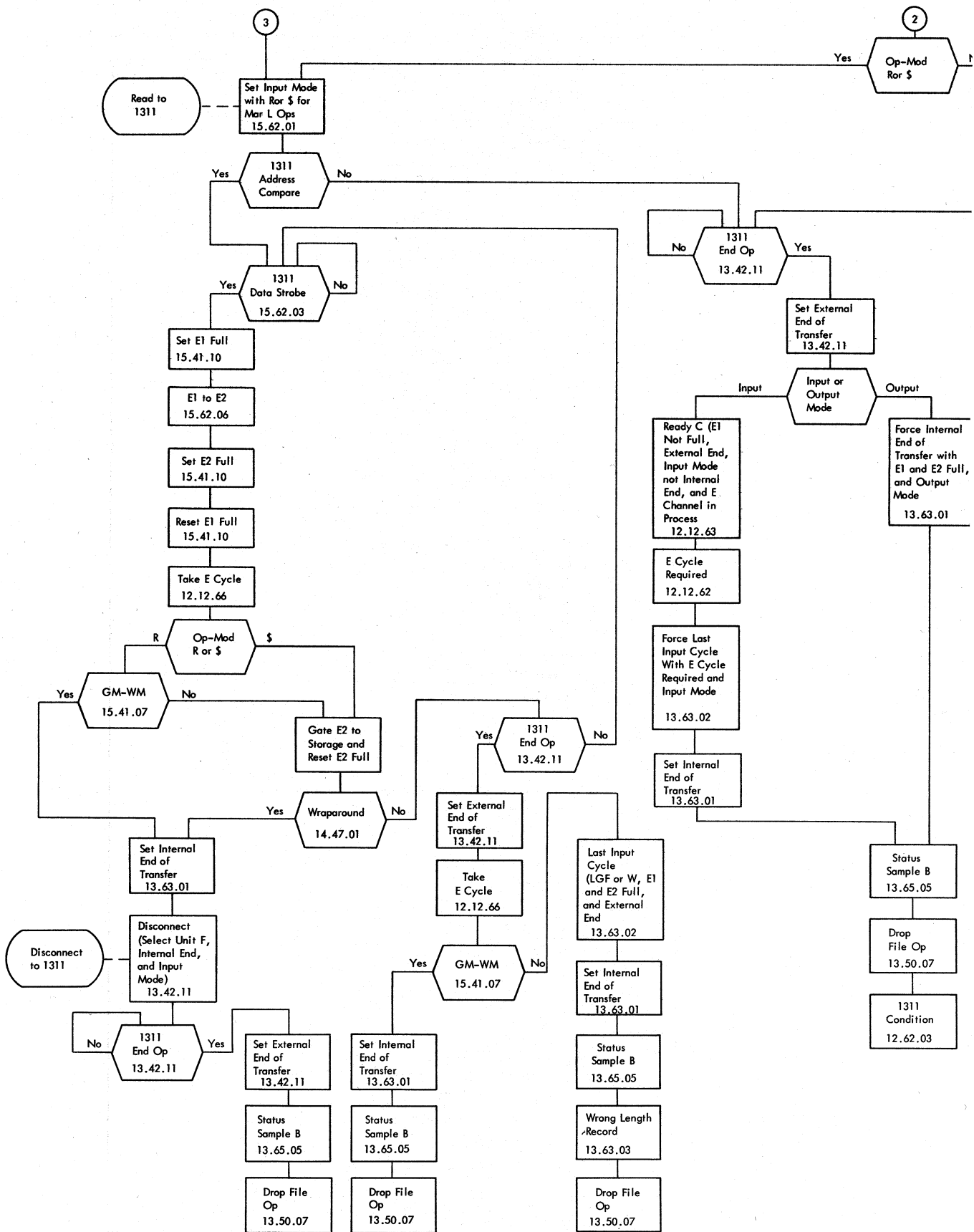


Figure 85. Input and Output Mode Operation

Scan Op Restart
Resets: Internal
End, End of
Record, Internal
End of Transfer,
Disconnect and
First Data Strobe
Latches. Use
AAR on First E
Cycle to Update
the Address
Register.
13.74.03

Continue
in Output
Mode

Take E Cycle
(Use BAR or
EAR)
12.12.66

Set E1
Full
15.41.10

E1 to E2
15.62.06

Set E2
Full
15.41.10

Reset E1
Full
15.41.10

Set File Start
Latch with
E2 Full
13.72.01

Take E
Cycle
12.12.66

No Yes
1311
Address
Compare

No Yes
1311
Data Strobe
15.62.03

Set Strobe
Latch
15.62.03

Yes No
E1 and E2
Empty and
Internal End of
Transfer
13.42.11

Disconnect
13.42.11

No Yes
1311
End Op
13.42.11

1311 Scan
Restart Latch
with
Unoverlap and
E Channel
Disconnect
Causes Scan
Op Restart
13.74.05

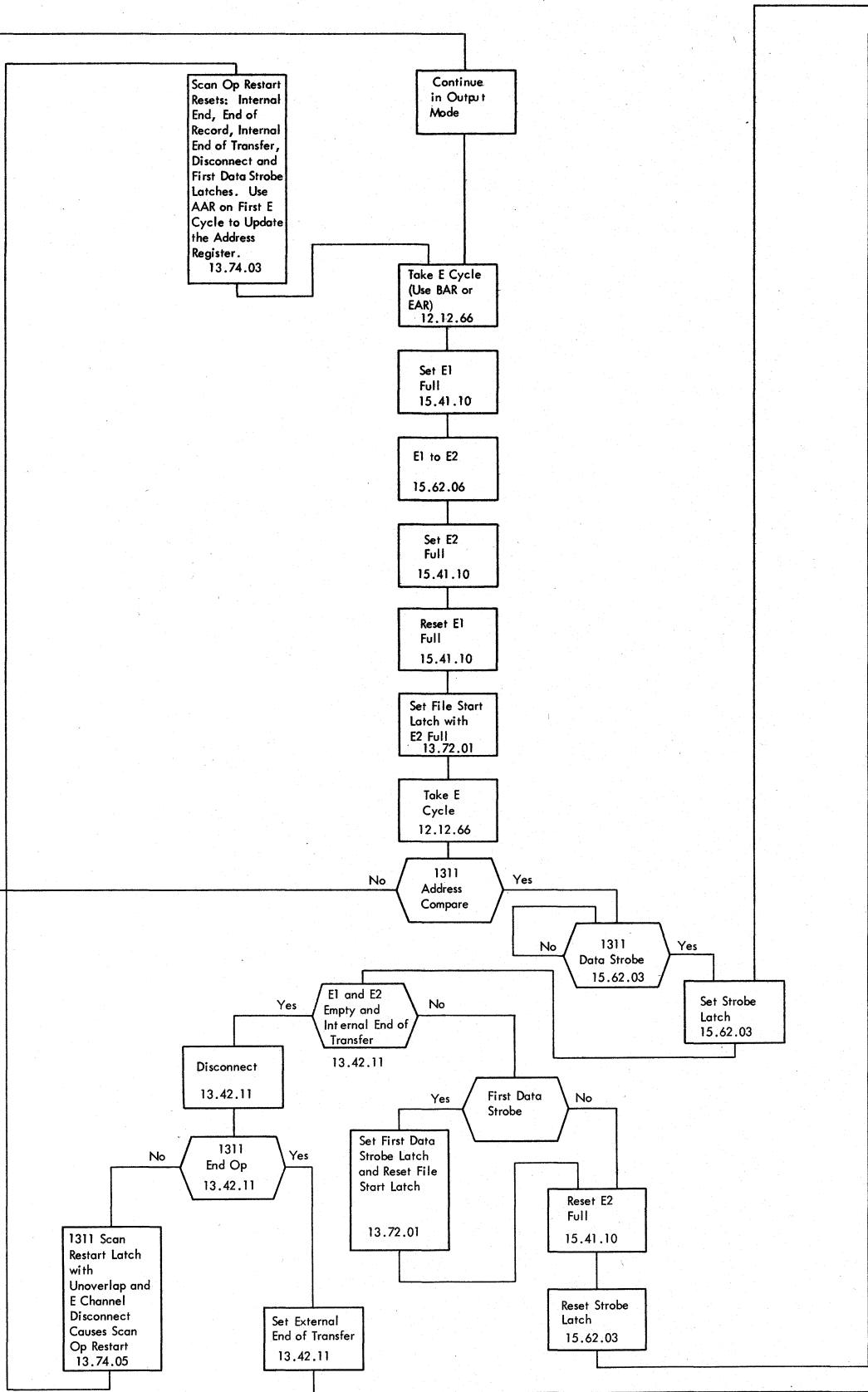
Set External
End of Transfer
13.42.11

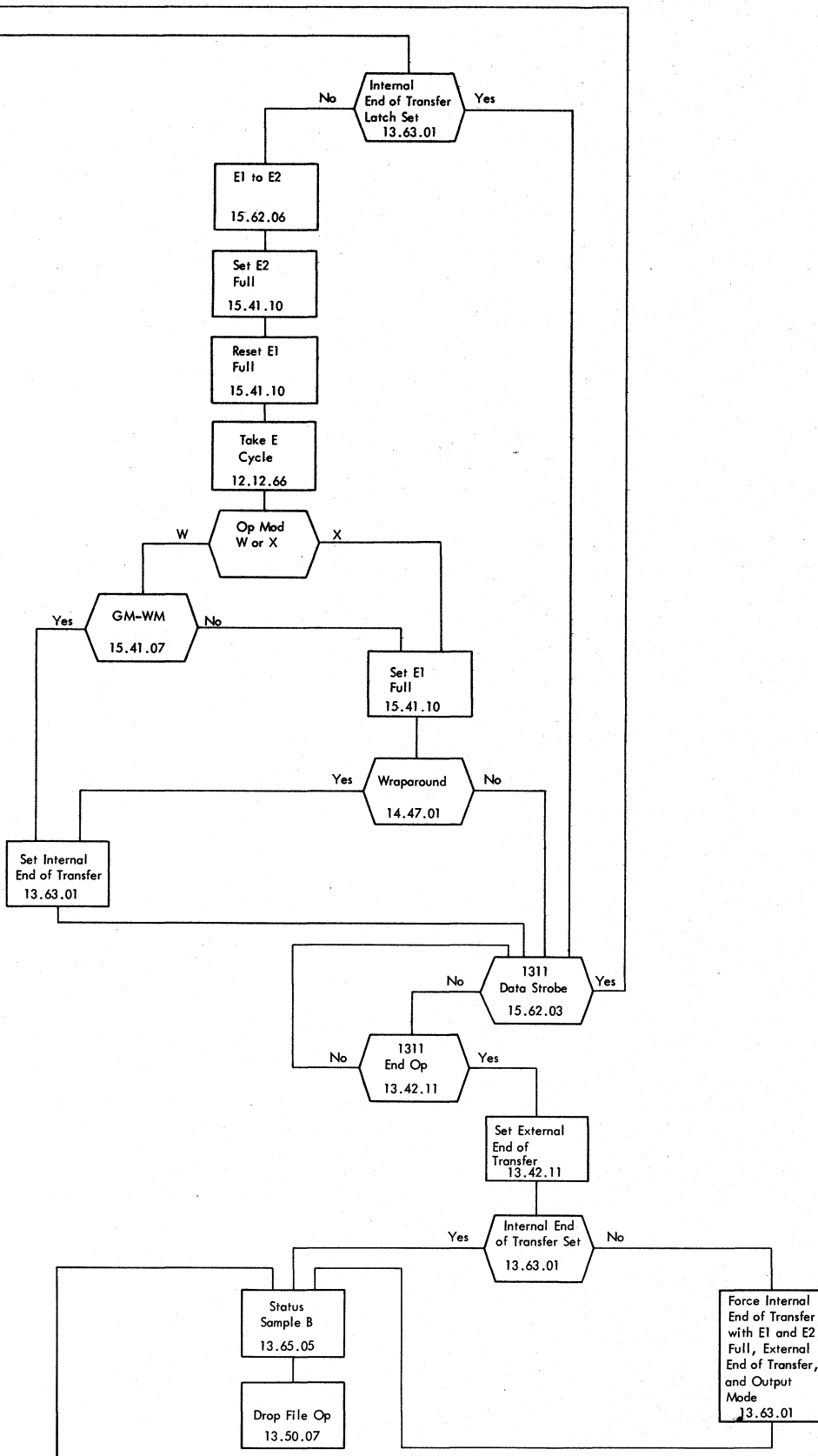
Yes No
First Data
Strobe

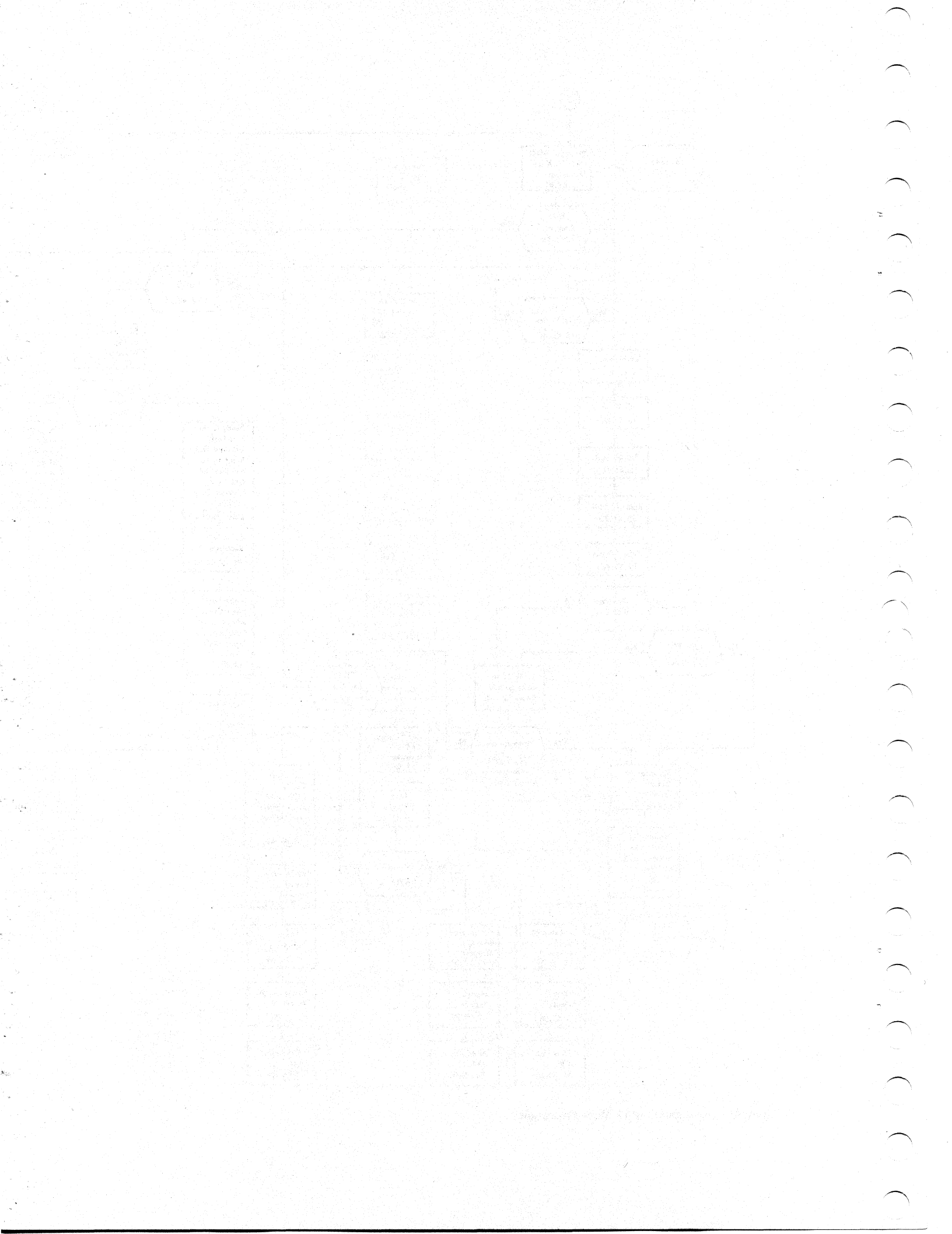
Set First Data
Strobe Latch
and Reset File
Start Latch
13.72.01

Reset E2
Full
15.41.10

Reset Strobe
Latch
15.62.03







Reference Section

INDICATOR	1402 CARD READER	1402 CARD PUNCH
Not Ready (A-Status Indicator)	Card jam Reader out of cards (not EOF) Reader not on line Reader power off Reader stacker full Cover interlock open Feed clutch failure (clutch check) Joggle switch open (file feed door) Input-Output synchronizer off line Input-Output synchronizer power off	Card jam Punch out of cards Punch stacker full Punch power off Punch not on line Chip basket full or not in place Cover interlock open
Busy (A-Status Indicator)	Read synchronizer being filled Card being stacked	Previous card still being punched
Data Check (B-Status Indicator)	Hole count check Input-Output synchronizer detects parity error Input-Output synchronizer detects timing error Processing unit detects parity error Never set on stacker select and feed instruction	Input-Output synchronizer detects one of the following errors during CPU-to-synchronizer data transfer: Parity Error Clock Error Ring Error (card is not punched)
Condition (A-Status Indicator)	EOF (last card has been stacked) (EOF latch turned off as this indicator turned on) Never set on stacker select and feed instruction	Hole count check-detected during the punch cycle of the following card. If error card is stacked, a blank card (second card behind error card) is fed. Parity error detected during punching.
No Transfer (B-Status Indicator) (A-Status Indicator for Kd Command)	Card has been transferred previously. This indicator will be set ON if two select stacker and feed instructions are given without an intervening read a card instruction with a 9 in the units position (n) of the X-control field. It will also be set ON if two read a card instructions with a 9 in the units position of the X-control field are given without an intervening select stacker and feed instruction	Never set
Wrong Length Record (B-Status Indicator)	Wrong Length record Never set on stacker select and feed instruction	Wrong length record (this card not punched)

Figure 86. Status Indicator Chart – 1402 Card Read Punch

Not Ready (A-Status Indicator)	Out of cards (not EOF) Feed check Stop key depressed Full stacker Power-off
Busy (A)	Card in motion between read cycle
Condition (A)	Last card data transferred on previous instruction
Wrong Length Record	Incorrectly located GM-WM Feed-ck
No-Xfer	Miss-feed from Hopper
Data Check	Invalid card punch Crooked feeding (skew ck) Photo-cell malfunction

Figure 87. Status Indicator Chart – 1442-3 Card Reader

INDICATOR	1403 PRINTER	
	M/L OP	F/2 OP
Not Ready (A-Status Indicator)	Printer not ready, printer not on line, printer power off, printer out of forms	Printer not ready, printer not on line, printer power off, printer out of forms
Busy (A-Status Indicator)	Previous line still being printed	Forms in motion, forms instruction waiting to be executed
Data Check (B-Status Indicator)	I-O Synchronizer detects a parity or clock error during CPU-to-Synchronizer (line is not printed)	Never set
Condition (A-Status Indicator)	I-O Synchronizer detected one of following errors during printing of line from previous print command Hammer check Parity error Hammer fire Synch Check check (chain timing) Equal compare Print ctrl error check (hammer reset) Print line Delay ctrl error compare check (ring timing) (present command is terminated--no data transfer)	Never set
No Transfer	Never set	Never set
Wrong Length Record (B-Status Indicator)	Wrong length record (line is not printed)	Never set

Figure 88. Status Indicator Chart – 1403 Printer

INDICATOR	1403 CONSOLE OPERATIONS
Not Ready	Never set
Busy (A-Status Indicator)	Never set (read operation) Carriage returning (write operation)
Data Check (B-Status Indicator)	Processing unit detects input character validity error (read) I-O printer detects output character validity error (write)
Condition (A-Status Indicator)	Cancel key operated during inquiry (read) Never set (write)
No Transfer (A-Status Indicator)	No message request--cancel key operated before inquiry (read) Never set (write)
Wrong Length Record (B-Status Indicator)	Wrong length record (read) Never set (write)

Figure 89. Status Indicator Chart – 1415 Console

INDICATOR	729-7330 TAPE OPERATIONS	
Not Ready (A-Status Indicator)	Tape unit not ready No such tape unit selected Tape adapter unit not on line Tape adapter unit power off	} Read, Write, and Unit Control
Busy (A-Status Indicator)	Tape adapter unit busy	} Read, Write, and Unit Control
Data Check (B-Status Indicator)	Processing unit received wrong parity character Tape adapter unit sent wrong parity character Tape mark read in odd parity mode Tape adapter unit received wrong parity character Tape adapter unit detects rbc parity error Set if write tape mark in odd parity	Read Read Read Write Write Unit Control
Condition (B-Status Indicator)	1st character of record was tape mark Foil strip detected Never set (unless tape mark read)	Read Write Unit Control
No Transfer	Never set	Read Write, and Unit Control
Wrong Length Record (B-Status Indicator)	Wrong length record (WLR set if a write command addresses a GM-WM) Never set	Read and Write Write Unit Control

Figure 90. Status Indicator Chart – 729-7330 Tape Units

INDICATOR	7750 PROGRAMMED TRANSMISSION CONTROL
Not Ready	7750 not ready
Busy	Not used
Data Check	1. Unusual end signal from 7750 2. Input parity error in 1410
Condition	1. 7750 failed to terminate previous operation correctly 2. 7750 unable to initiate operation
No Transfer	Data transfer incomplete. 7750 became inoperative during data transfer
Wrong Length Record	Data field actually transferred was different in length from either the field in storage or field in 7750. On input data is stored to $\frac{1}{2}$ - remainder lost

Figure 91. Status Indicator Chart – 7750 PTC

INDICATOR	1014 READ	1014 WRITE	1011 READ
Not Ready (A-Status Indicator)	Power off in 1414 or buffer not on line. (No data transfer)	Power off in 1414 or buffer not on line. (No data transfer)	Power off in 1414, buffer not on line. 1011 out of tape or tape is broken, or 1011 not attached to 1414 (no data transfer)
Busy (A-Status Indicator)	Not applicable	Buffer emptying	Buffer filling
Data Check (B-Status Indicator)	79 characters entered or parity error between 1414 and core storage. If parity error, incorrect data stored as * if asterisk switch is on	Parity error between core storage and 1414. No transfer to 1014	Parity error between 1414 and core storage. Incorrect data stored as * if asterisk switch is on
Condition (A-Status Indicator)	Machine check within 1414	Preceding message in error as received at station. Current message not transmitted	Not applicable
No Transfer (A-Status Indicator)	Buffer not full	Preceding message not transmitted; station inoperative (non-existent station power off, station out of forms, or station did not acknowledge preceding message)	Not applicable
Wrong Length Record (B-Status Indicator)	Incorrectly placed GM-WM. Data stored only to GM-WM. Remainder lost	Incorrectly placed GM-WM. Data transfer up to GM-WM, but only to 1414	Incorrectly placed GM-WM. Data stored only to GM-WM. Remainder lost

Figure 92. Status Indicator Chart – 1014 Inquiry Station, 1011 Paper Tape Reader

INDICATOR	TELEGRAPH READ	TELEGRAPH WRITE	1009 READ	1009 WRITE
Not Ready	Power off in 1414 or buffer not on line. (No data transfer)	Power off in 1414, buffer not on line, or local telegraph not ready. (No transfer of data)	Power off in 1414, buffer not on line, 1009 not on line, or power off. No transfer of data.	Power off in 1414, buffer not on line, 1009 not on line or power off. No transfer of data.
Busy	Buffer filling	Buffer emptying	Buffer filling	Both buffers have data; one is emptying. Or, last segment of message is in 1 buffer.
Data Check	Parity error, format check, or character pile-up between telegraph unit and 1414 or parity error between 1414 and 1410. Incorrect data stored as *, if asterisk switch is on.	Parity error between 1410 core storage and 1414. No transfer to telegraph.	Parity error between 1414 and core storage. Incorrect data stored as * if asterisk switch is on.	Parity error between core storage and the 1414. Incorrect data arrived in 1414. (No transfer to local 1009)
Condition	Missed message Buffer not emptied in time.	Preceding message had parity or translate error between 1414 and telegraph.	Missed message (buffer not emptied in time) or transmission error. (Indicator comes on only after end-of-message condition is recognized by the 1414)	Current message in error Transmitted to local 1009, but not successfully to remote 1009.
No Transfer	No request. No message in buffer to be read.	Preceding message transmitted but received incorrectly or not at all because of invalid format line failure, or excessive delay in getting characters to the output line, or no group mark following the EOM sequence.	End of message	End of message. (This comes on only after busy goes off.)
Wrong Length Record	Incorrectly placed GM-WM. Data stored only to GM-WM. Remainder lost.	Incorrectly placed GM-WM. Data transfer up to GM-WM, but only to the 1414 (not to telegraph)	Incorrectly placed GM-WM. Data stored only to GM-WM. Remainder lost.	Incorrectly placed GM-WM. Data transfer up to GM-WM, but only to 1414, not to local 1009.

Figure 93. Status Indicator Chart – Telegraph and 1009 DTU

INDICATOR	7631/1301
Not Ready	Access inoperative or 7631 off-line 7631 power off Home address switch check
Busy	Access in motion 7631 not available (model 3)
Data Check	Parity check Check character code check Write disk check Format character check Invalid track number
Condition	Wrong length format No record found Write check without mode setting Disk storage circuit check File control circuit check Invalid operation code
No Transfer	No read or write operation performed (No data or address is transferred)
Wrong Length Record	Short or long record

Figure 94. Status Indicator Chart – 1301 Disk Storage

INDICATOR	1412 MAGNETIC CHARACTER READER, MODEL 1
Not Ready	Not feeding documents
Busy	Document in wrong position for reading
Data Check	Any I-O 3, 4, 5, 6 or 7 indicator on I-O 3 read check indicator I-O 4 amount field indicator I-O 5 control field indicator I-O 6 account number indicator I-O routing field indicator
No Transfer	Late read condition
Wrong Length Record	Wrong length record condition

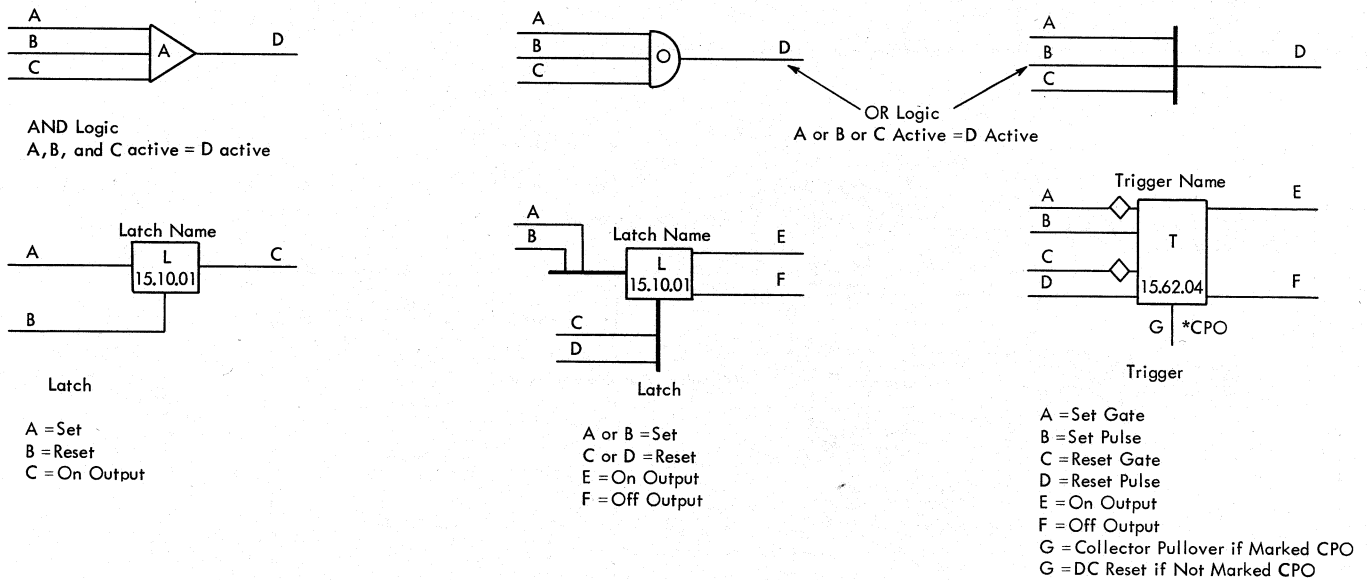
Figure 95. Status Indicator Chart – 1412 MCR

INDICATOR (d-character)	1419
Not Ready (1)	Sort/Compare Error Jam Condition No Read Field Selected Empty Hopper Full Pocket Cover Interlock Open
Data Check (4)	One of the following indicators is NOT on: Amount Field Valid Process Control Field Valid Account No Field Valid Transit Field Valid Serial No Field Valid
Wrong Length Record (B)	Wrong Length Record

Figure 96. Status Indicator Chart – 1419 MCR

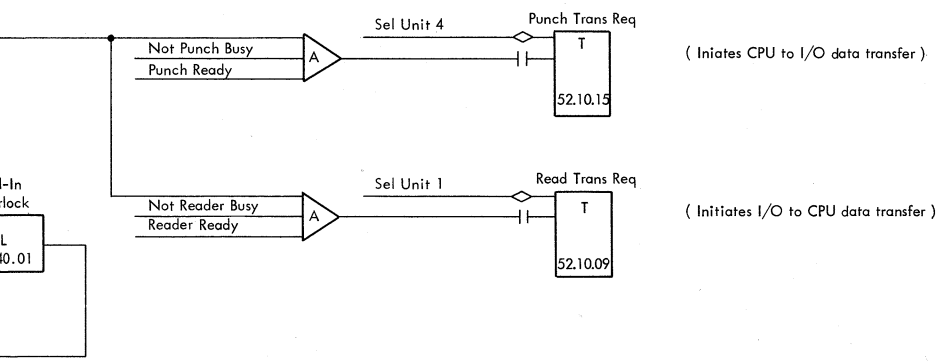
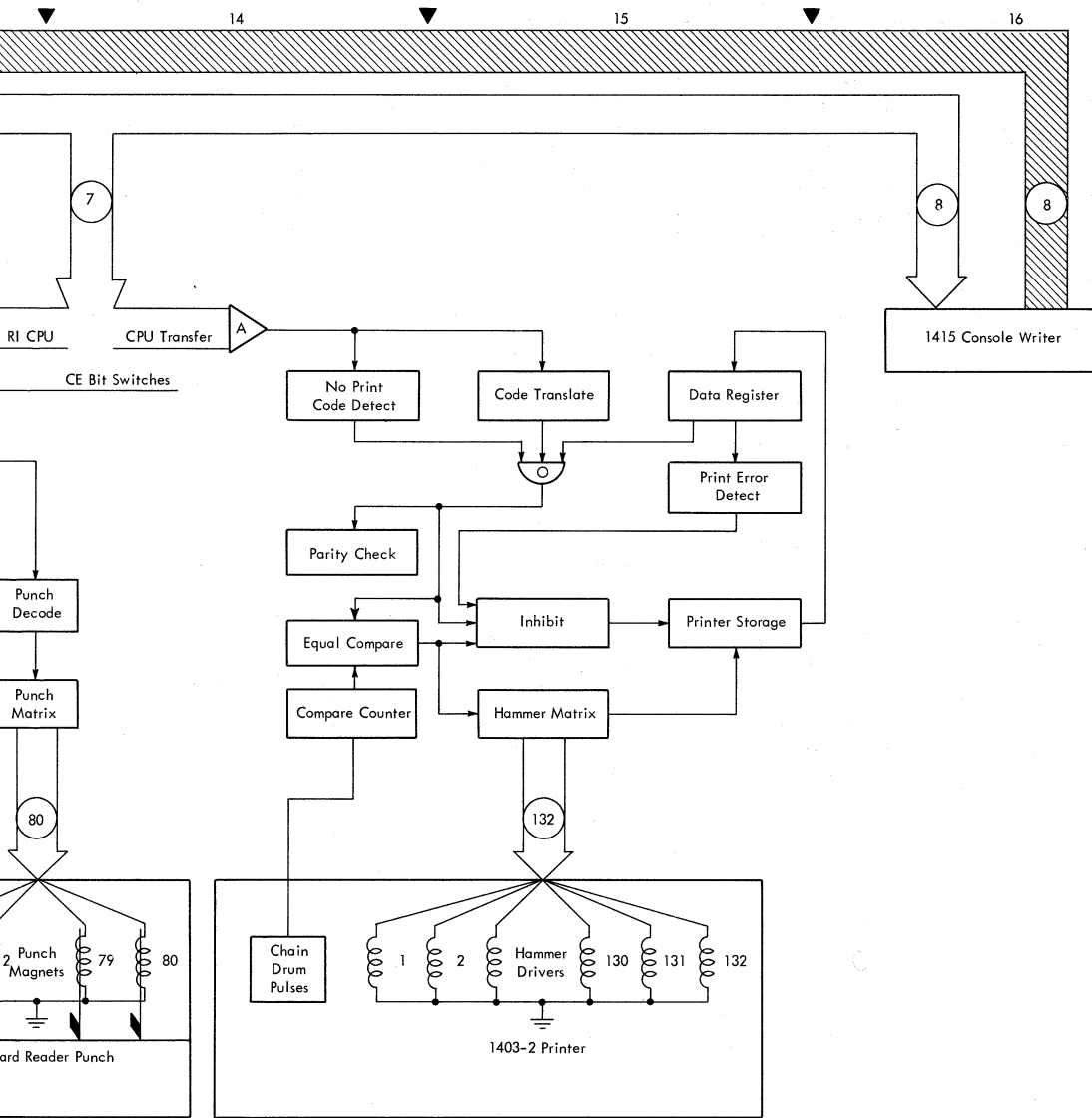
d-CHARACTER & INDICATOR INTERROGATED	OPERATION			
	SEEK DISK	READ SINGLE RECORD READ FULL TRACK	WRITE DISK CHECK	WRITE SINGLE RECORD WRITE FULL TRACK WRITE ADDRESS
1 NOT READY	No such address No such access arm 1405 power off 1405 off line Access arm inoperative	No such address No such access arm 1405 power off 1405 off line Access arm inoperative	No such address No such access arm 1405 power off 1405 off line Access arm inoperative	No such address No such access arm 1405 power off 1405 off line Access arm inoperative
2 BUSY	Access arm still in motion from previous operation	Access arm still in motion from previous operation	Access arm still in motion from previous operation	Access arm still in motion from previous operation
4 DATA CHECK	1405 unit detects wrong parity character in address	1405 unit detects wrong parity character in address	1405 unit detects wrong parity character in address	1405 unit detects wrong parity character in address
8 CONDITION	Never set	Read operation address does not compare with indelible address on disk	Data in core storage does not compare with data in disk storage Write disk check address does not compare with indelible address on disk	Write operation address does not compare with indelible address on disk (Except write address operation)
- (B-bit) WRONG LENGTH RECORD	Wrong length address	Wrong length address Wrong length record	Wrong length address Wrong length record	Wrong length address Wrong length record (except write address operation)
(A-bit) NO TRANSFER	Wrong length address. 1405 unit detects wrong parity character in address	Wrong length address 1405 unit detects wrong parity character in address Read operation address does not compare with indelible address on disk	Wrong length address. 1405 unit detects wrong parity character in address Write disk check address does not compare with indelible address on disk	Wrong length address 1405 unit detects wrong parity character in address Write operation address does not compare with indelible address on disk (Except write address operation) Disk write inhibit switch on

Figure 97. Status Indicator Chart – 1405 Disk Storage



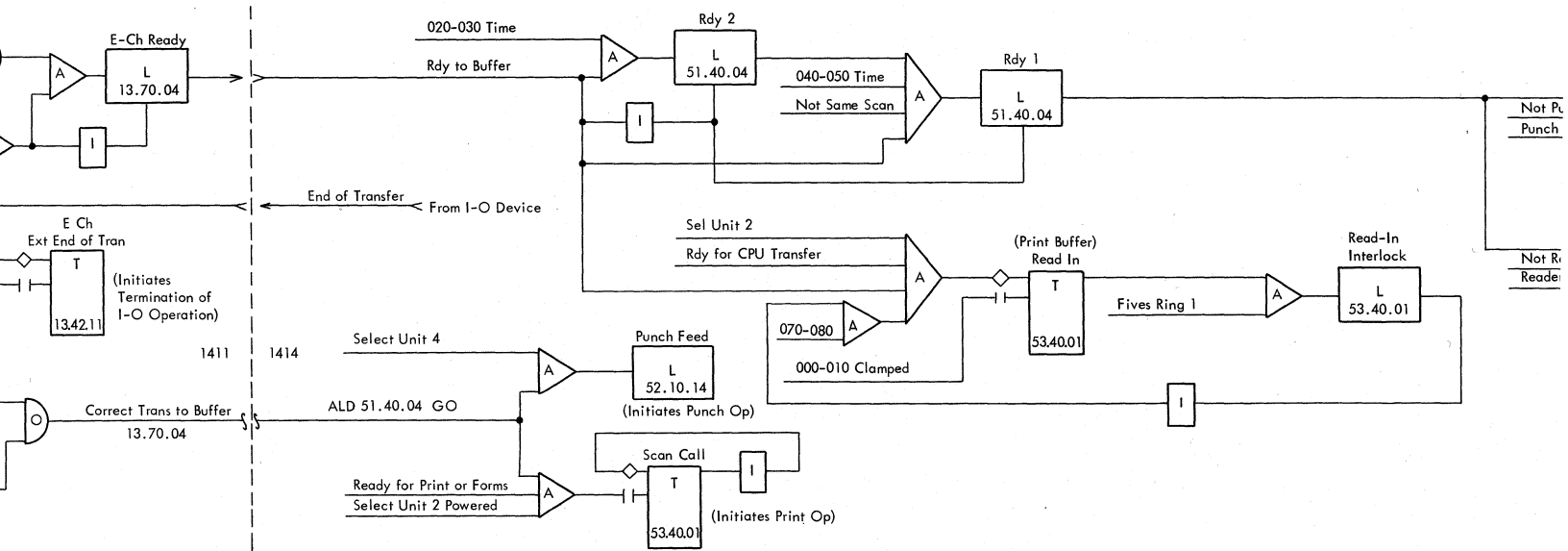
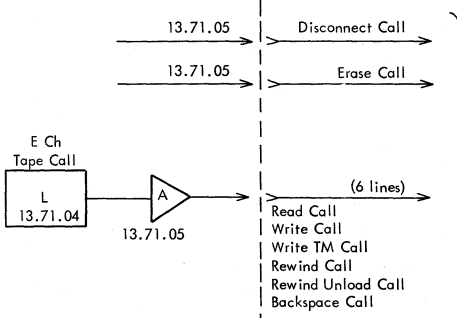
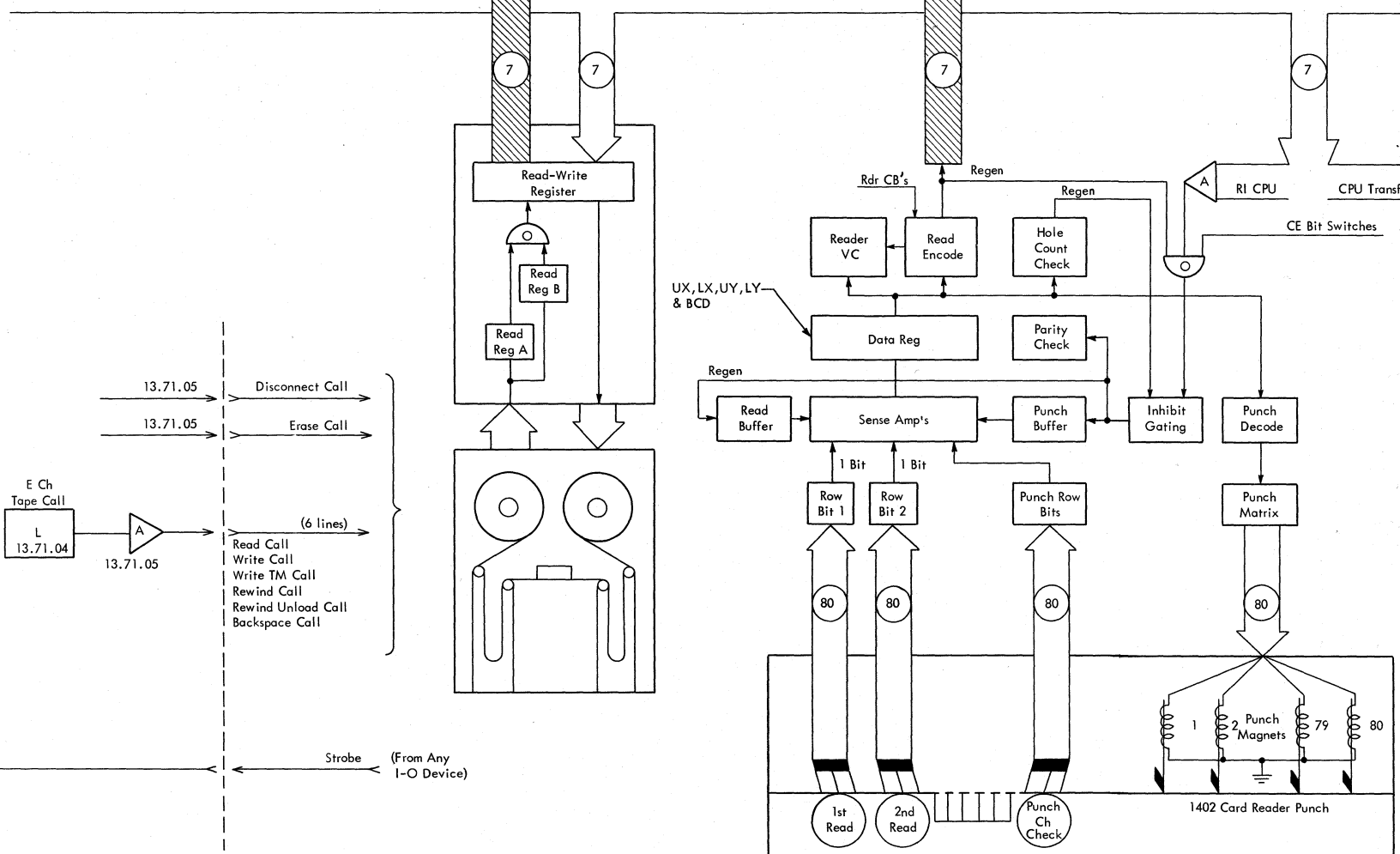
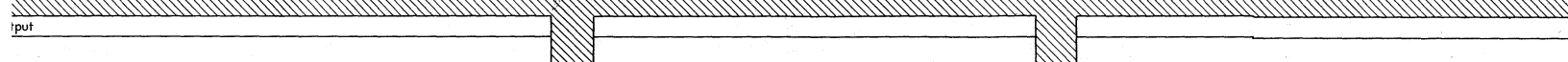
Note: Condensed Logic uses actual or abbreviated ALD line names
Simplified Logic uses descriptive terms to aid understanding the logical function

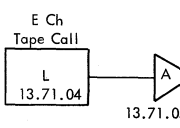
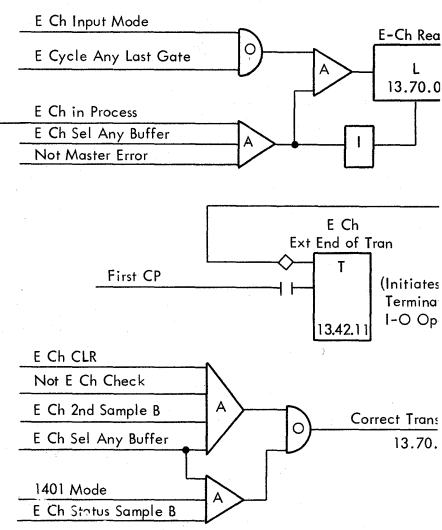
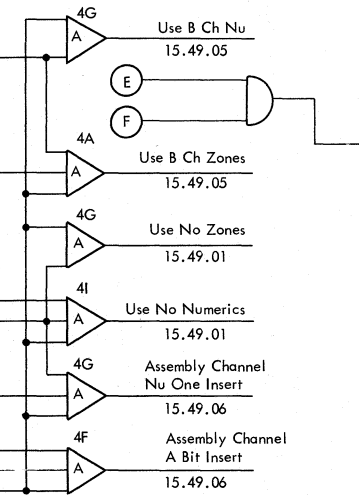
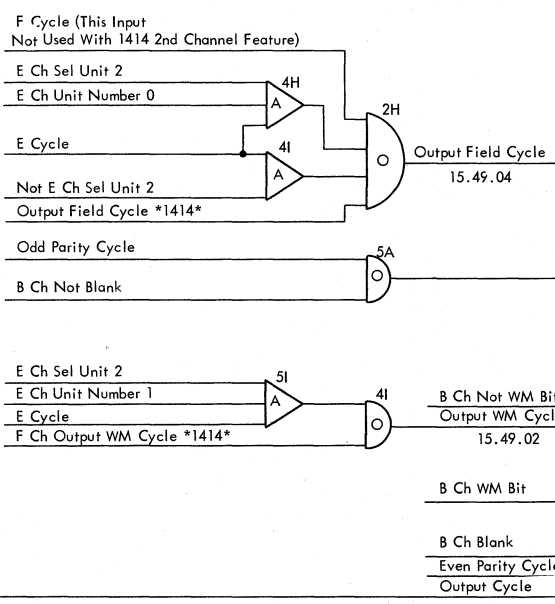
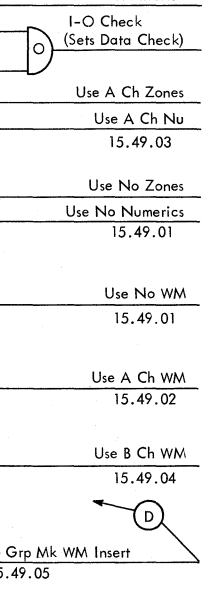
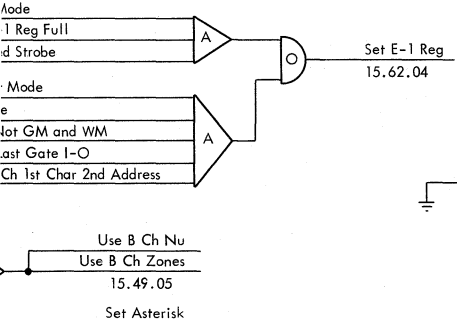
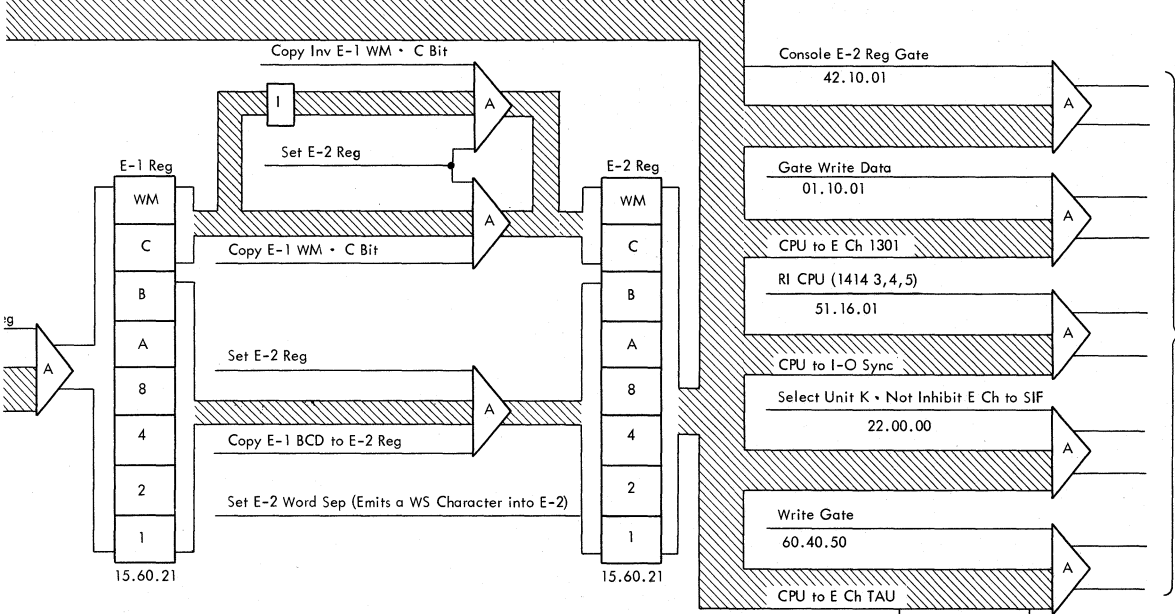
Figure 98. Condensed Logic Symbols



(Initiates CPU to I/O data transfer)

(Initiates I/O to CPU data transfer)



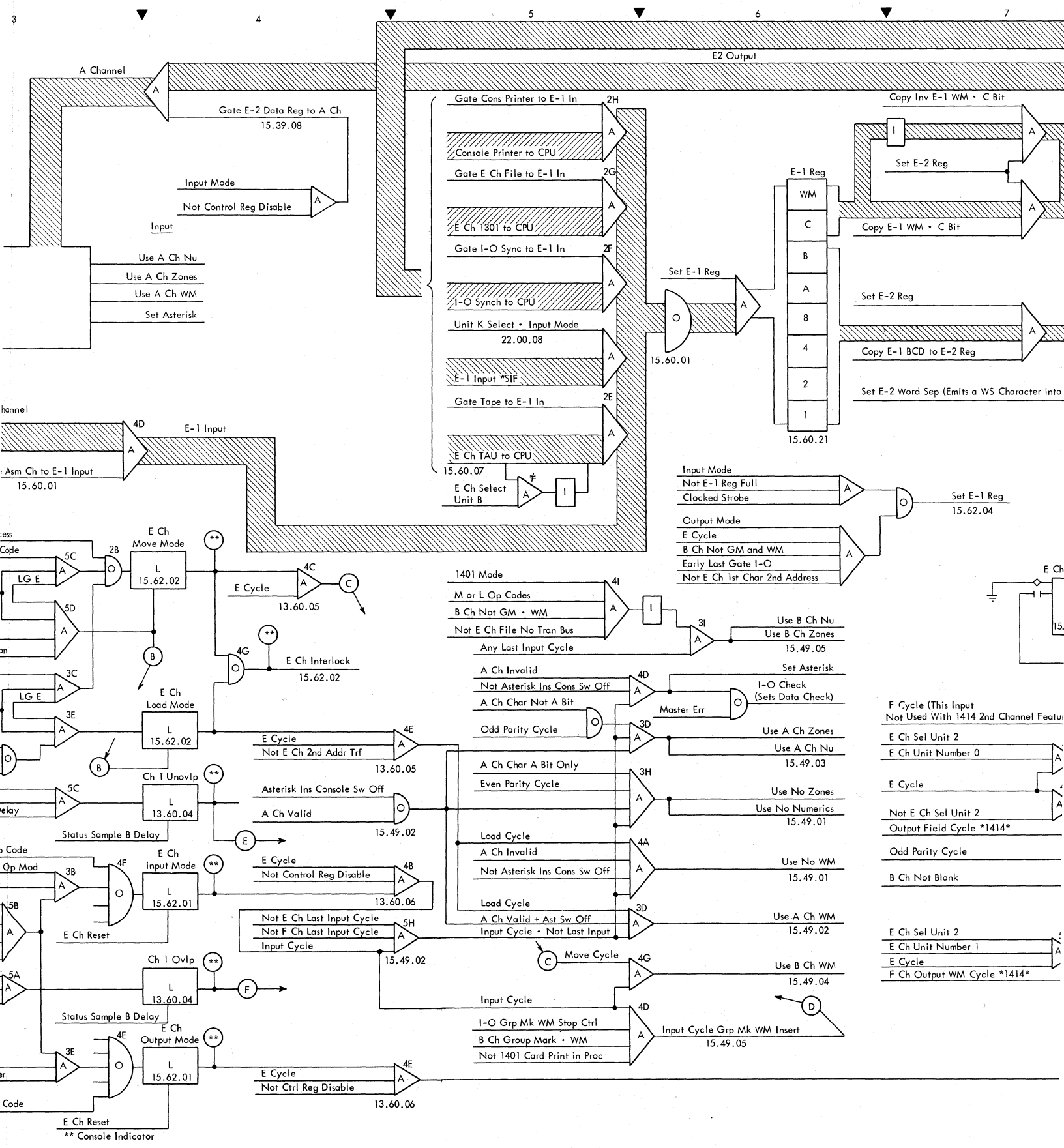


13
13

13.70.0

(Initiates Termina I-O Op

13.70.



A Channel

Gate E-2 Data Reg to A Ch
15.39.08

Input Mode
Not Control Reg Disable
Input

Use A Ch Nu
Use A Ch Zones
Use A Ch WM
Set Asterisk

E2 Output

Gate Cons Printer to E-1 In 2H
Console Printer to CPU
Gate E Ch File to E-1 In 2G
E Ch 1301 to CPU
Gate I-O Sync to E-1 In 2F
I-O Sync to CPU
Unit K Select - Input Mode 22.00.08
E-1 Input *SIF
Gate Tape to E-1 In 2E
E Ch TAU to CPU
E Ch Select Unit B

Copy Inv E-1 WM * C Bit

Set E-2 Reg

Copy E-1 WM * C Bit

Set E-2 Reg

Copy E-1 BCD to E-2 Reg

Set E-2 Word Sep (Emits a WS Character into

E-1 Reg
WM
C
B
A
8
4
2
1
15.60.21

Set E-1 Reg

15.60.01

Input Mode
Not E-1 Reg Full
Clocked Strobe
Output Mode
E Cycle
B Ch Not GM and WM
Early Last Gate I-O
Not E Ch 1st Char 2nd Address
Set E-1 Reg
15.62.04

Channel

E-1 Input

Asm Ch to E-1 Input
15.60.01

E Ch Move Mode
L
15.62.02

E Cycle
13.60.05

E Ch Interlock
15.62.02

E Ch Load Mode
L
15.62.02

E Cycle
Not E Ch 2nd Addr Trf
13.60.05

Asterisk Ins Console Sw Off
A Ch Valid
15.49.02

Ch 1 Unovlp
L
13.60.04

E Cycle
Not Control Reg Disable
13.60.06

Not E Ch Last Input Cycle
Not F Ch Last Input Cycle
Input Cycle
15.49.02

E Ch Input Mode
L
15.62.01

E Cycle
Not Ctrl Reg Disable
13.60.06

Ch 1 Ovlp
L
13.60.04

E Cycle
Not Ctrl Reg Disable
13.60.06

E Ch Output Mode
L
15.62.01

1401 Mode
M or L Op Codes
B Ch Not GM - WM
Not E Ch File No Tran Bus
Any Last Input Cycle
Use B Ch Nu
Use B Ch Zones
15.49.05
Set Asterisk
I-O Check
(Sets Data Check)

A Ch Invalid
Not Asterisk Ins Cons Sw Off
A Ch Char Not A Bit
Odd Parity Cycle
A Ch Char A Bit Only
Even Parity Cycle
Use A Ch Zones
Use A Ch Nu
15.49.03
Use No Zones
Use No Numerics
15.49.01

Load Cycle
A Ch Invalid
Not Asterisk Ins Cons Sw Off
Load Cycle
A Ch Valid + Ast Sw Off
Input Cycle * Not Last Input
Use No WM
15.49.01
Use A Ch WM
15.49.02

Input Cycle
I-O Grp Mk WM Stop Ctrl
B Ch Group Mark * WM
Not 1401 Card Print in Proc
Move Cycle
4G
Use B Ch WM
15.49.04

Input Cycle
4D
Input Cycle Grp Mk WM Insert
15.49.05

F Cycle (This Input Not Used With 1414 2nd Channel Feature)

E Ch Sel Unit 2
E Ch Unit Number 0

E Cycle
Not E Ch Sel Unit 2
Output Field Cycle *1414*

Odd Parity Cycle
B Ch Not Blank

E Ch Sel Unit 2
E Ch Unit Number 1
E Cycle
F Ch Output WM Cycle *1414*

** Console Indicator

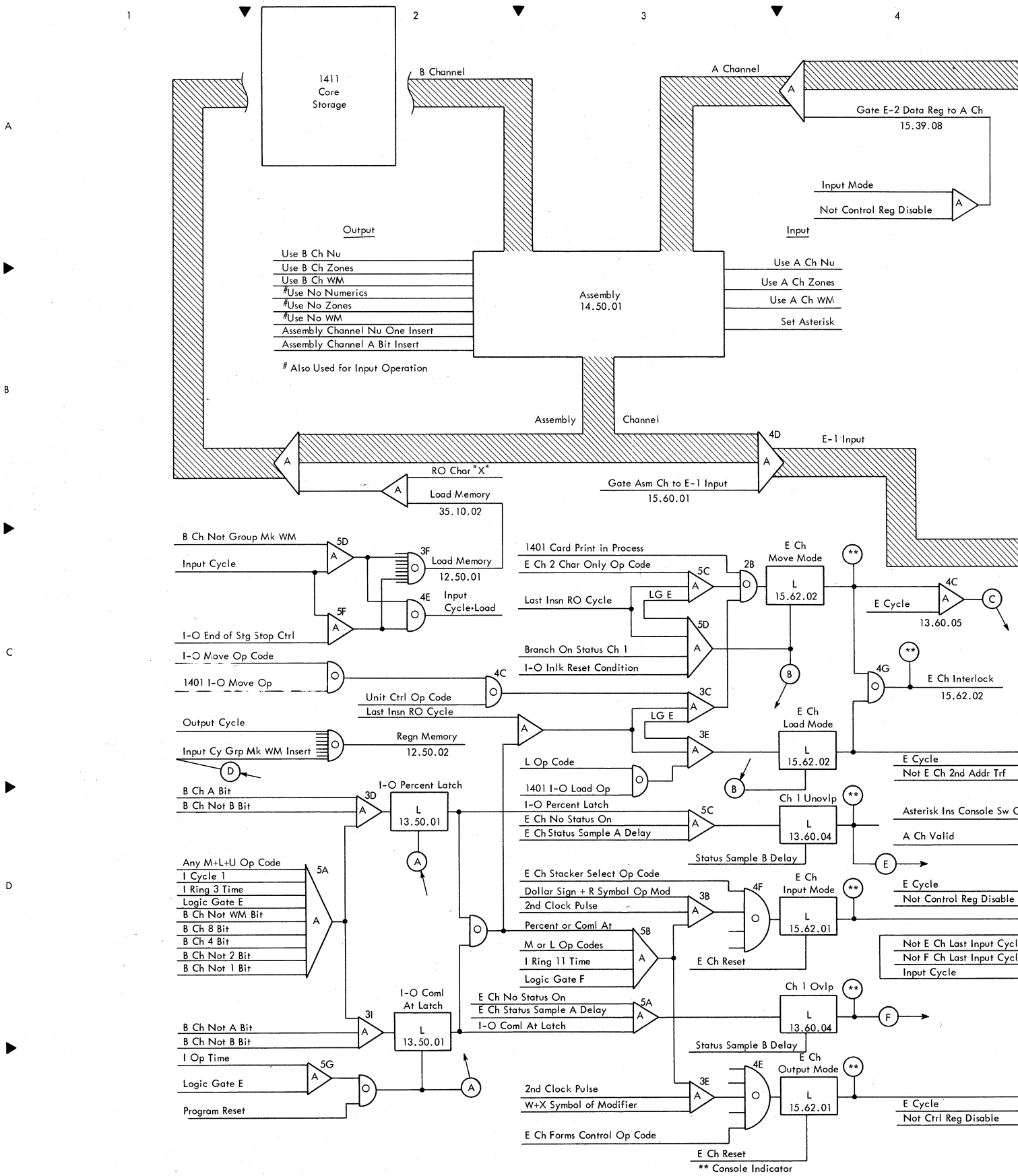


Figure 99. I-O Data Flow Controls

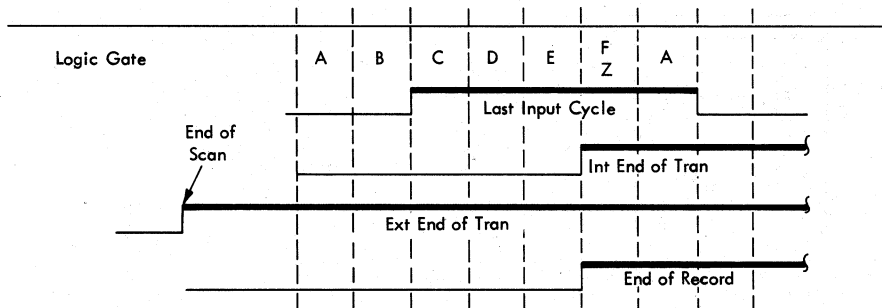
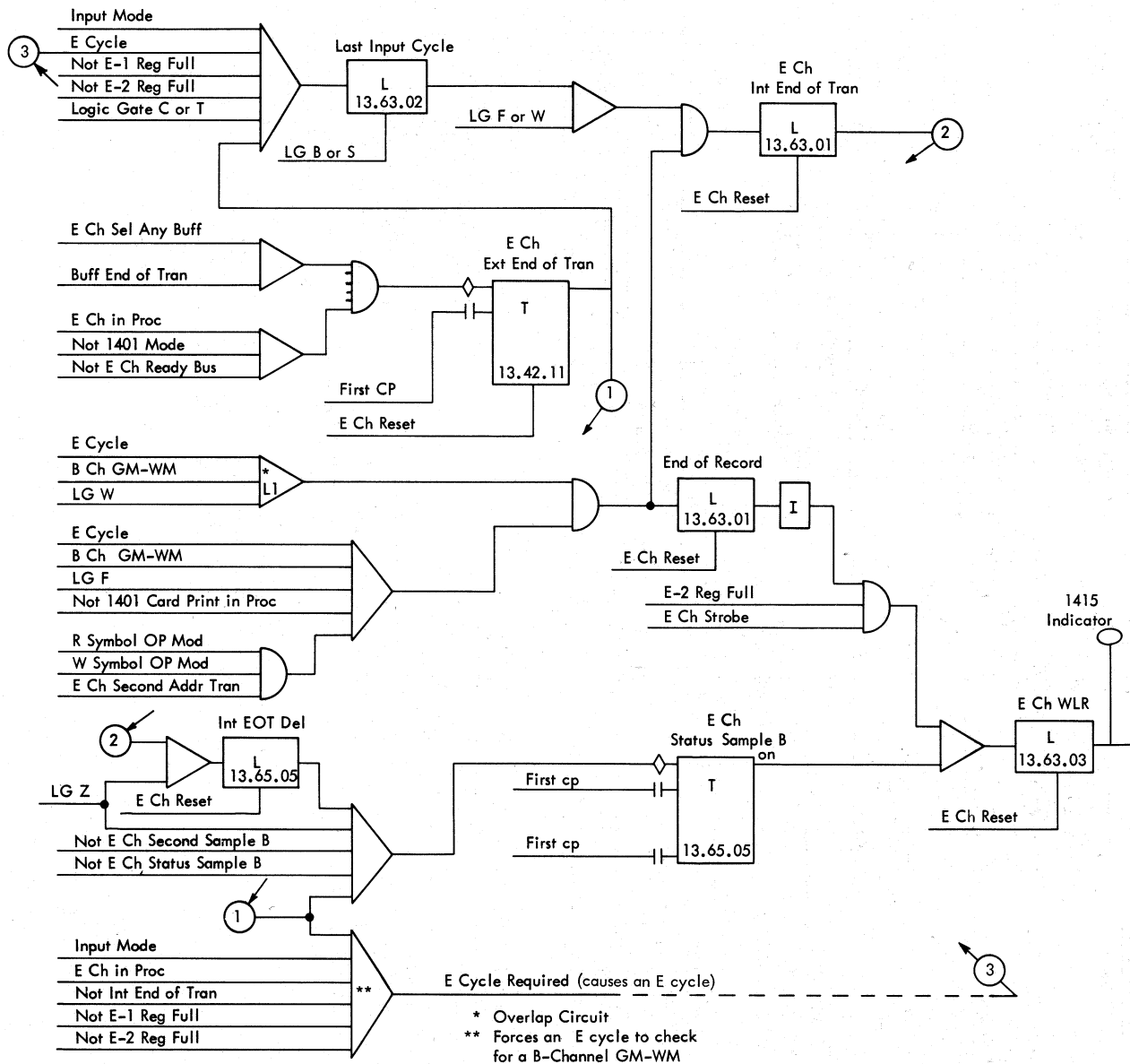


Figure 100. Last Input Cycle

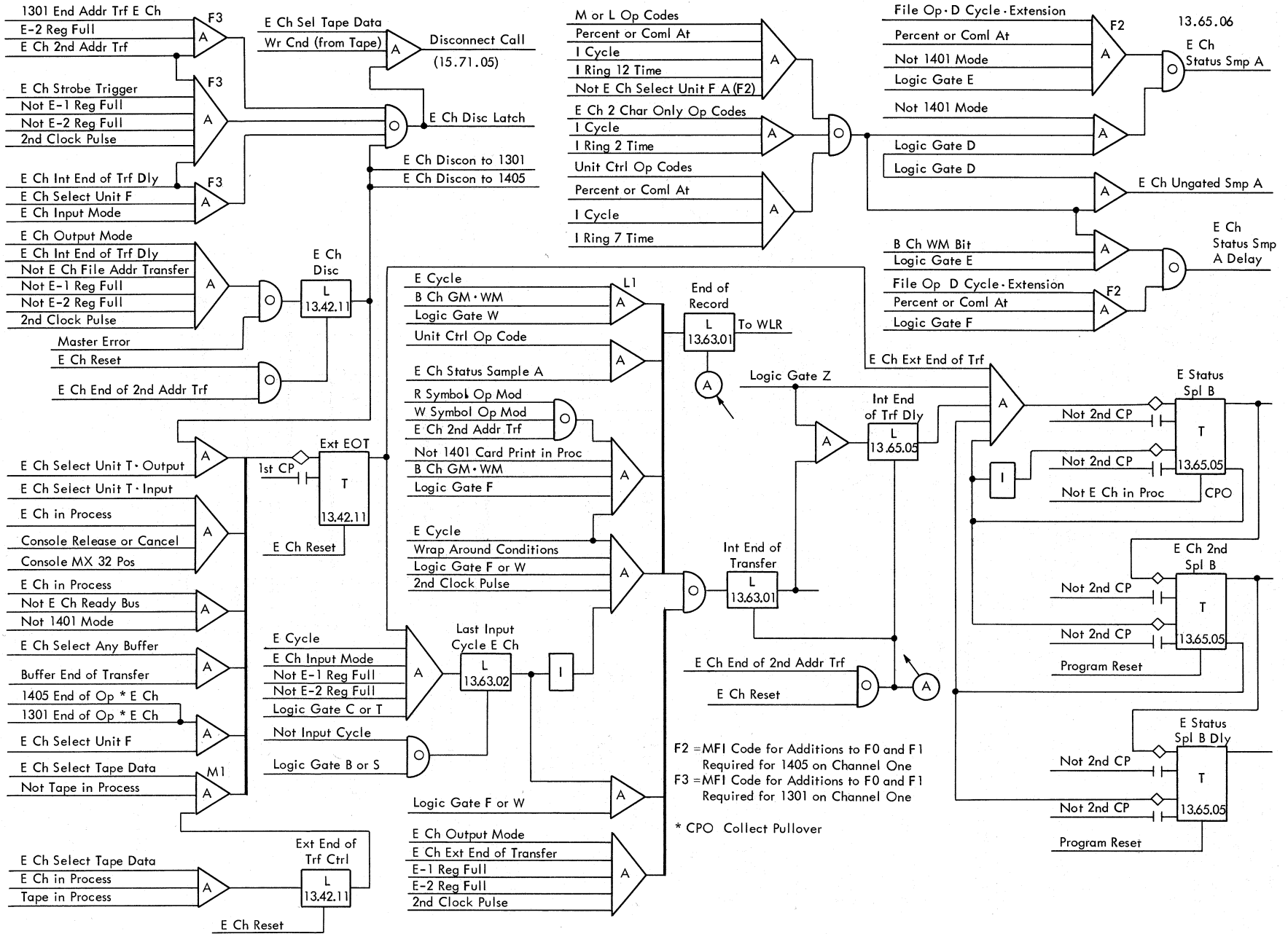


Figure 101. E-Channel Status Sample A and B

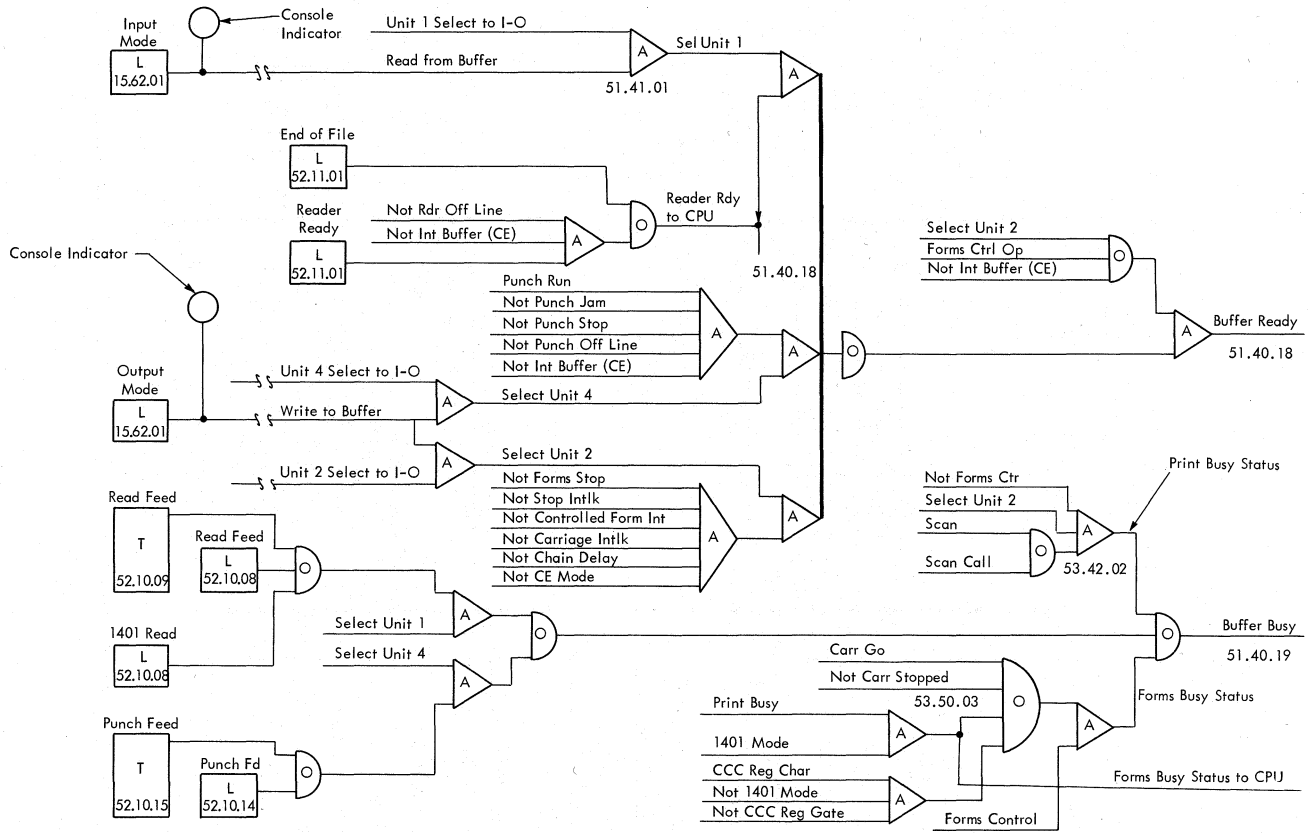


Figure 102. E-Channel Buffer Ready and Busy

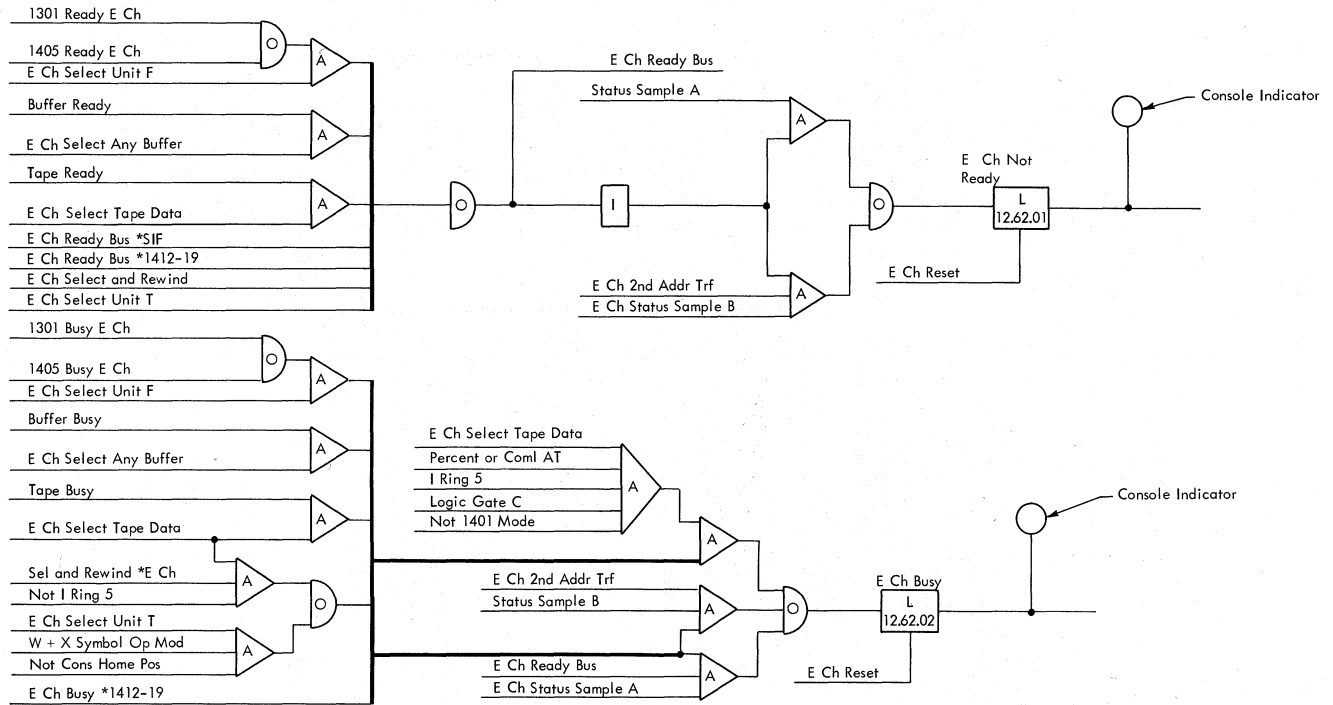


Figure 103. E-Channel Not Ready and Busy

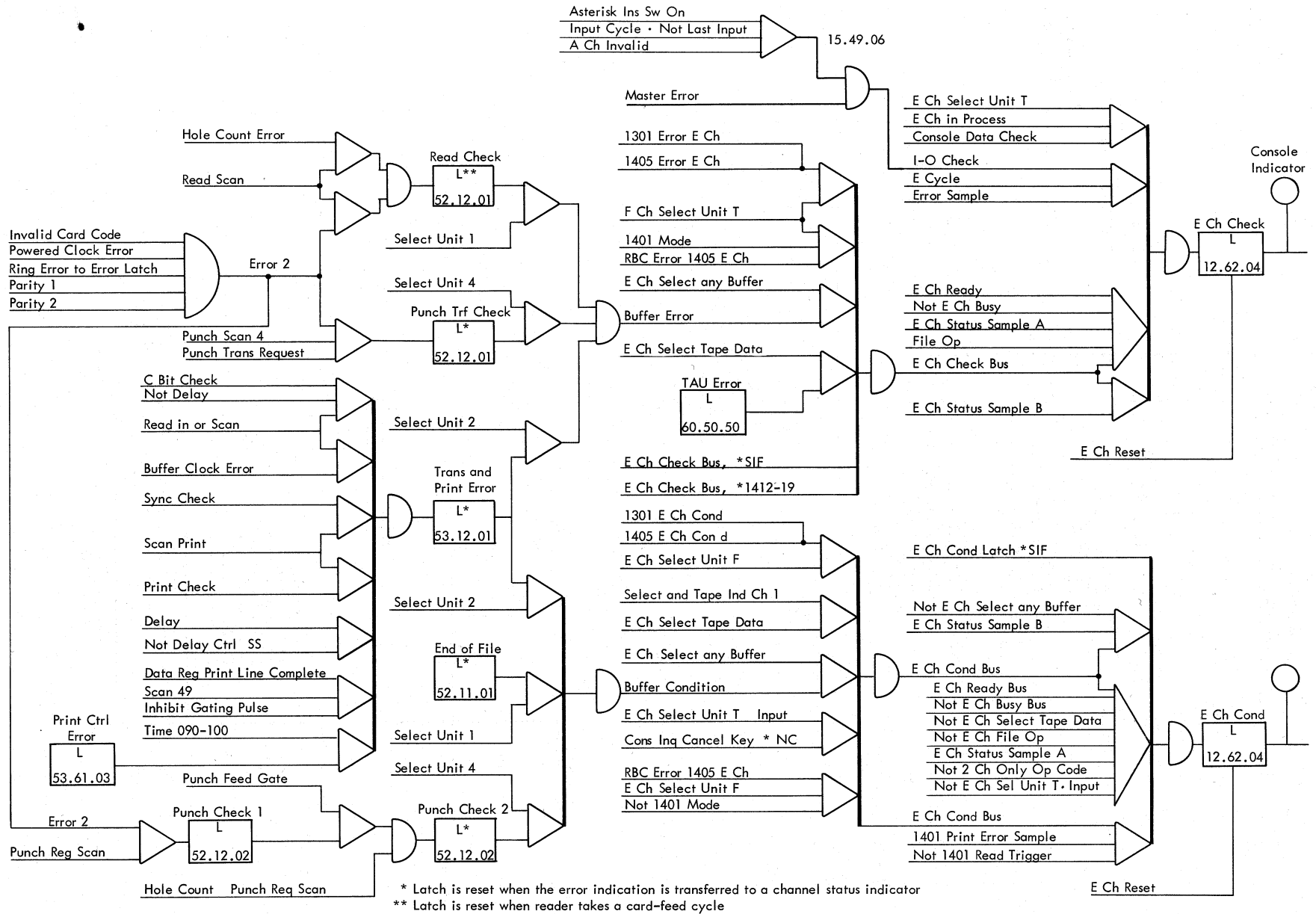
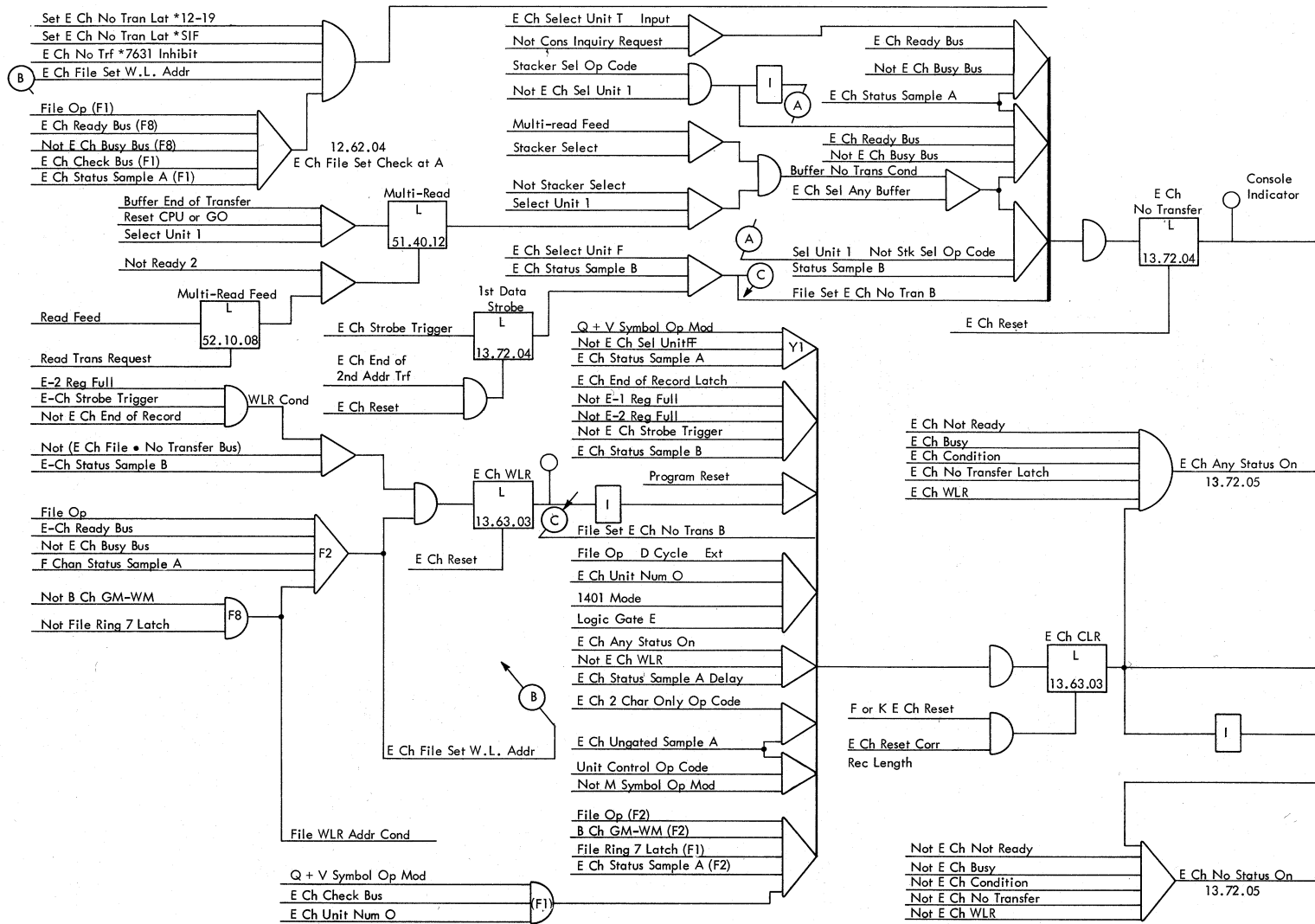


Figure 104. E-Channel Check and Condition



Y1 = Priority Feature
 F8 = Additions to FO common to 1405 on either channel
 F2 = Additions to FO and FZ required for 1405 on channel one
 F1 = Additions required for 1405 or 1301 on channel one

Figure 105. E-Channel WLR and No Transfer

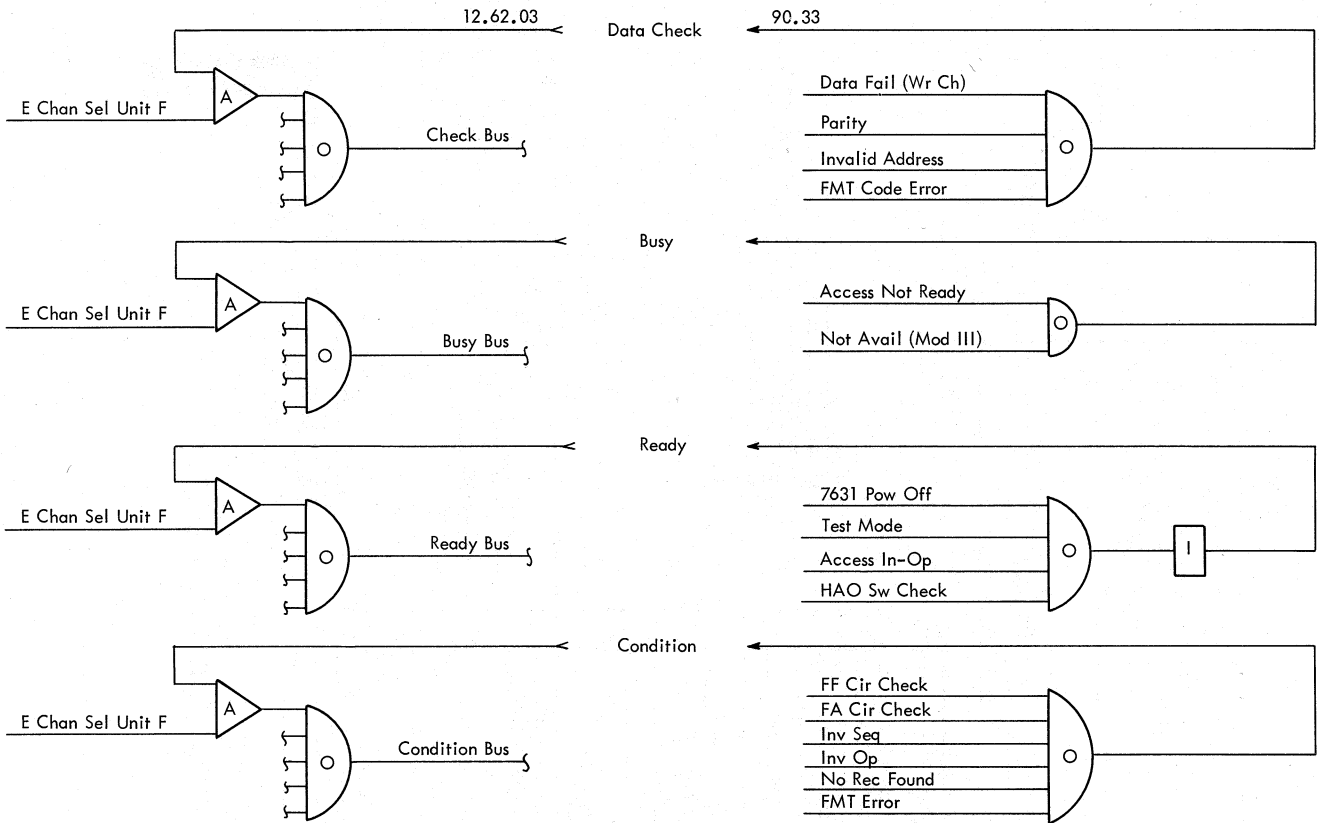


Figure 106. 1411-7631 Channel Status Lines

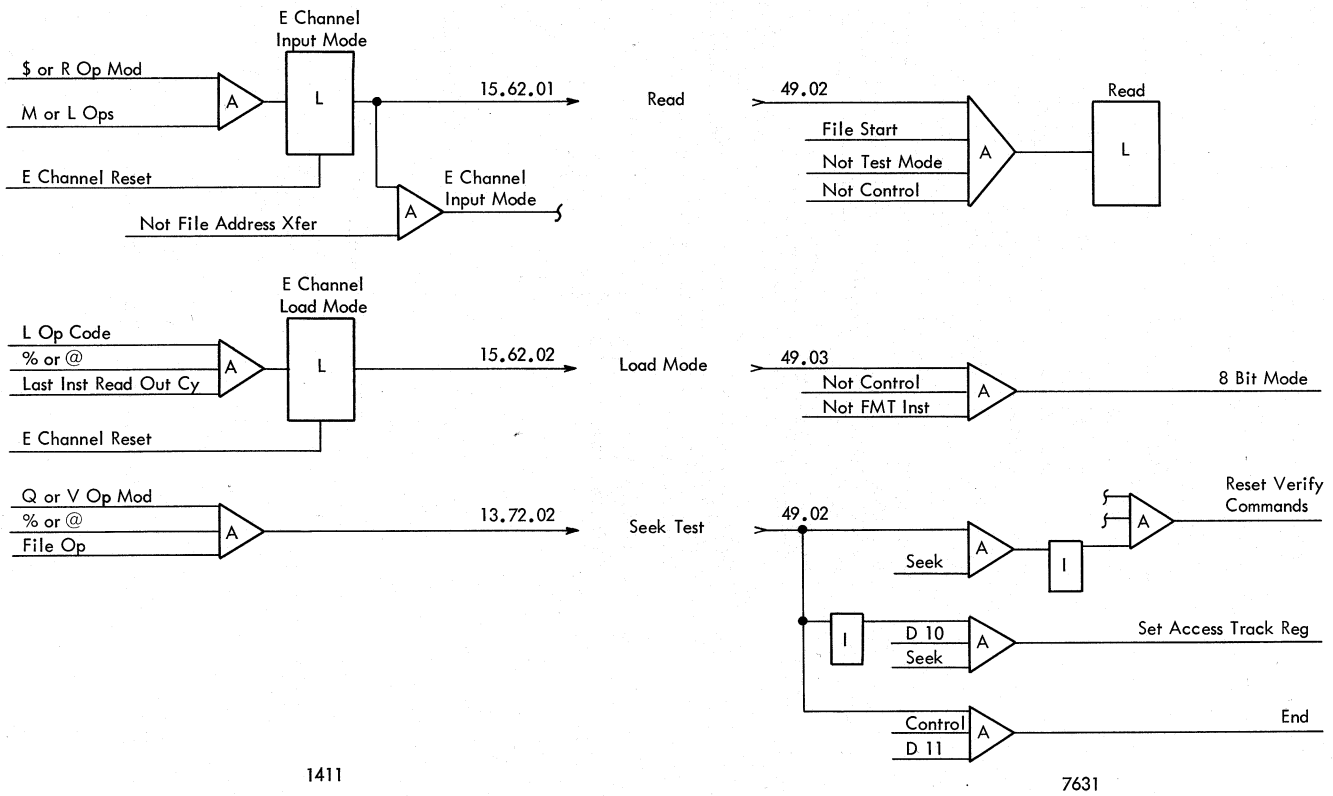


Figure 107. 1411-7631 Read Control

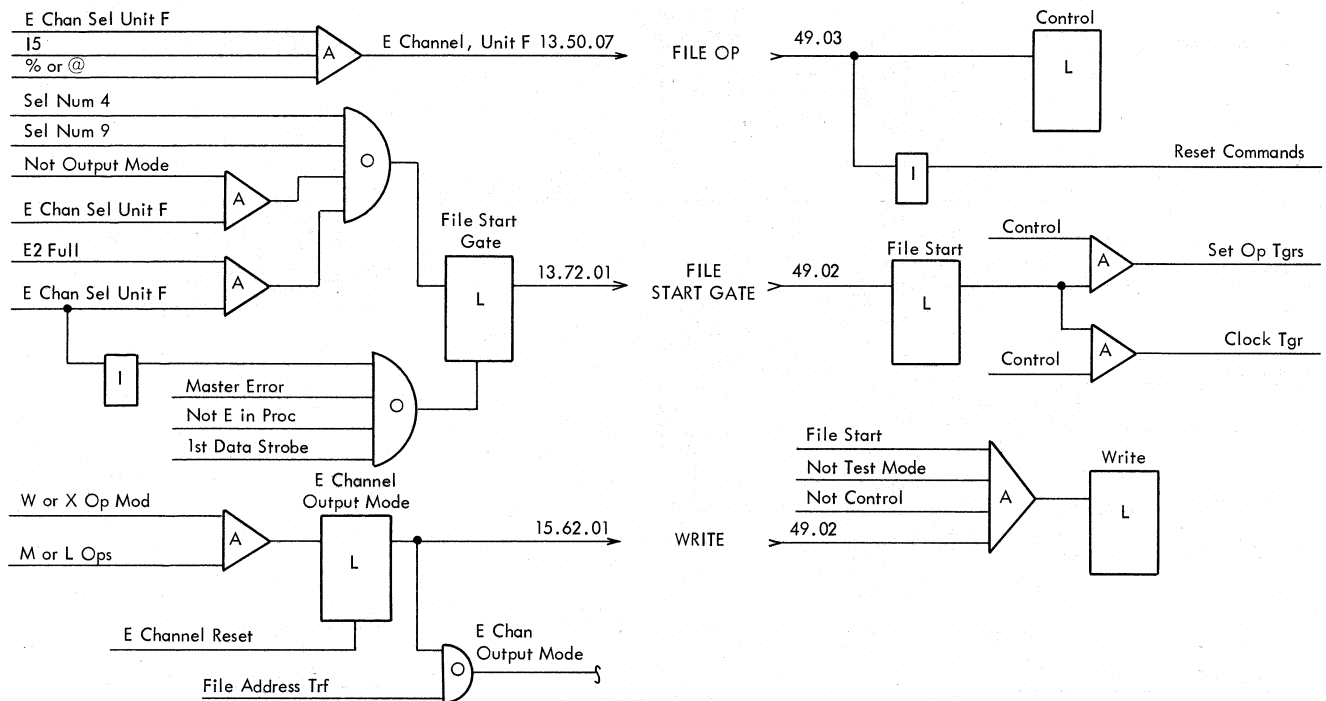


Figure 108. 1411-7631 Write Control

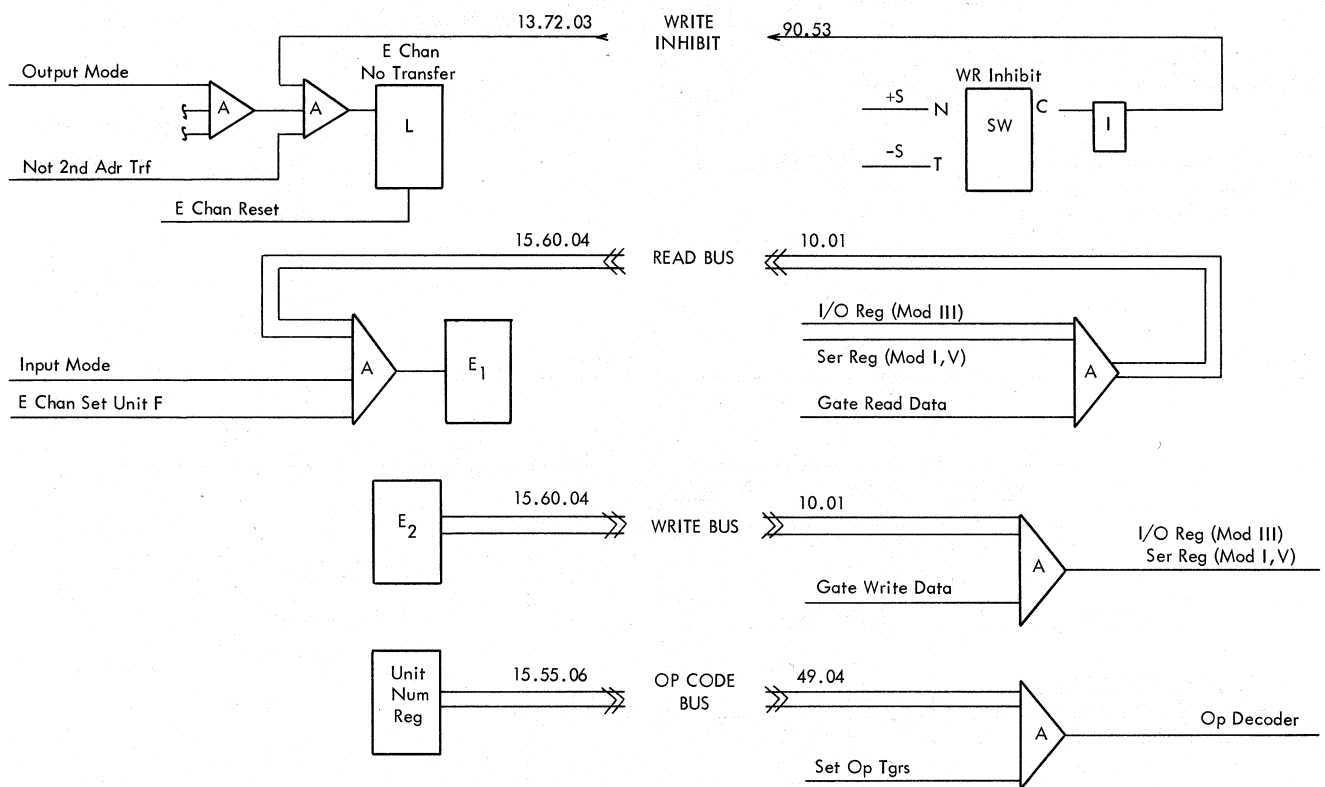


Figure 109. 1411-7631 Read and Write Busses

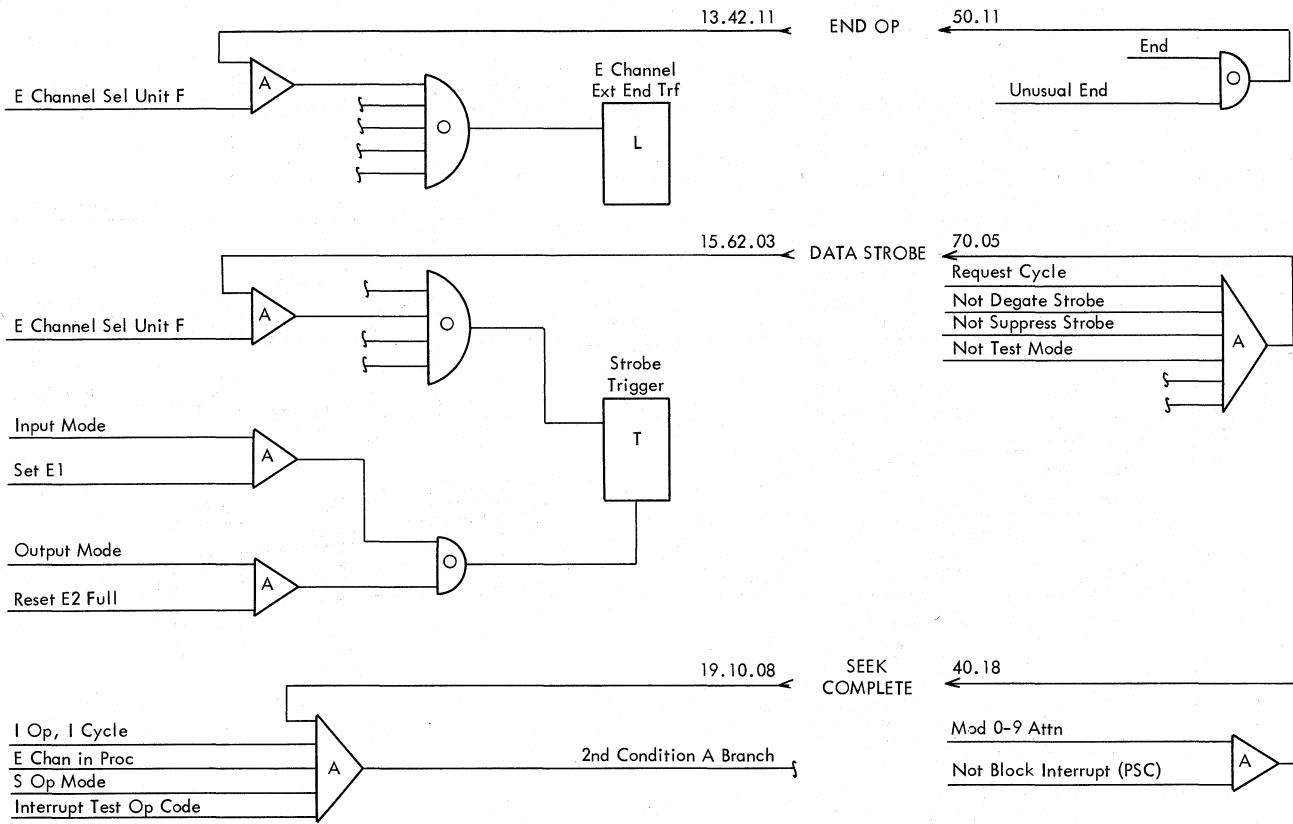


Figure 110. 1411-7631 Channel Strobe

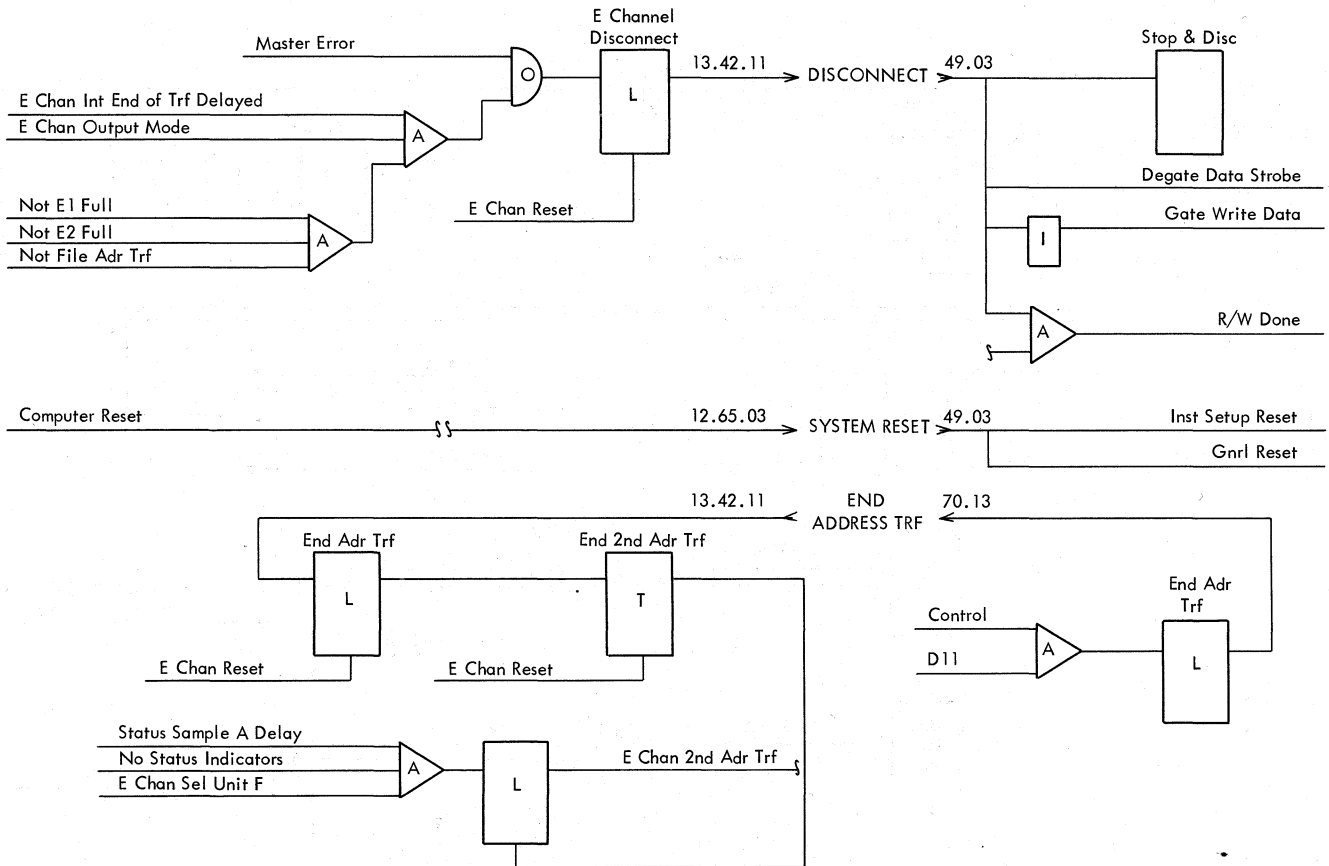


Figure 111. 1411-7631 Channel Disconnect

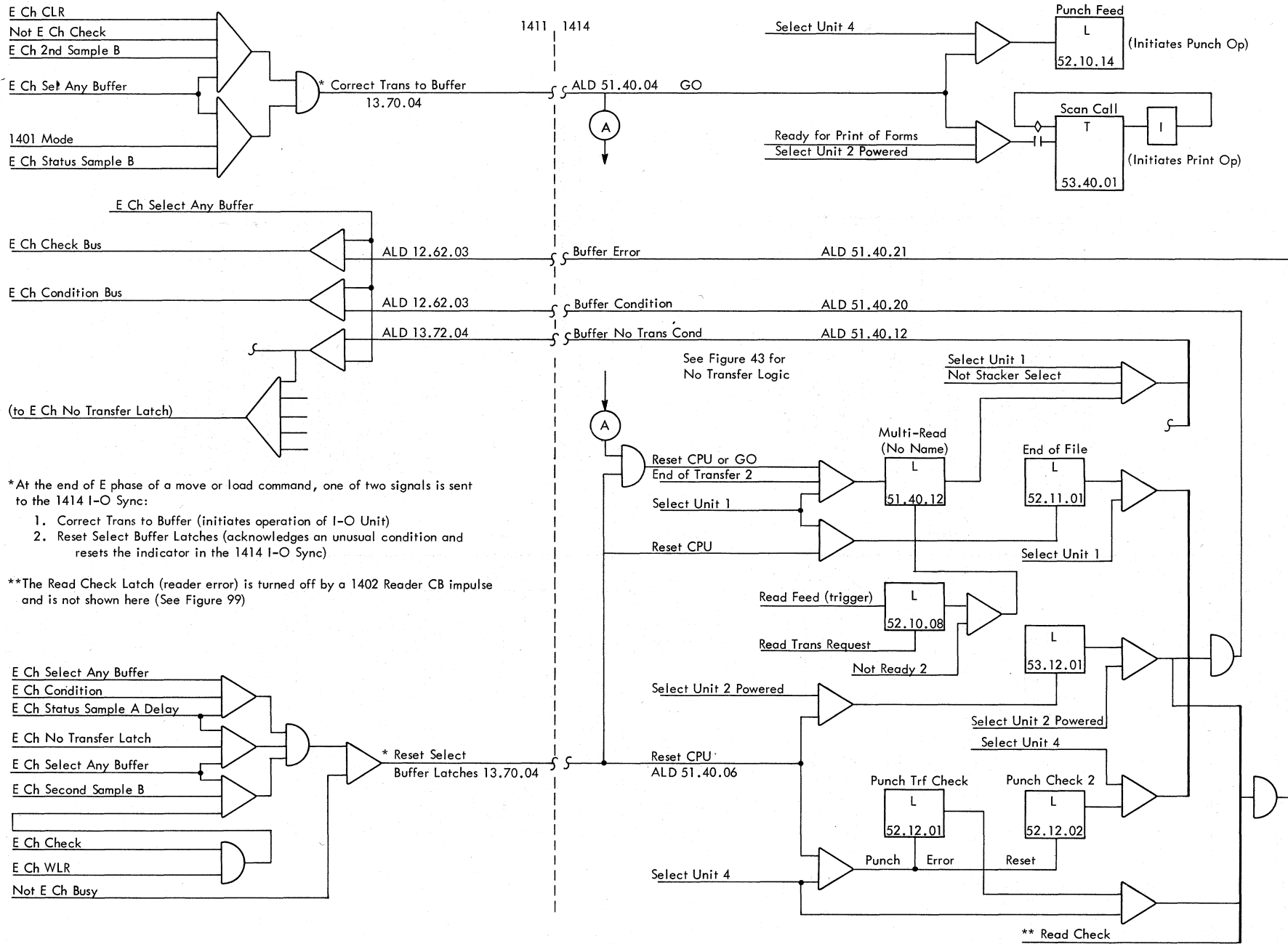


Figure 112. 1411-1414 Error Resets

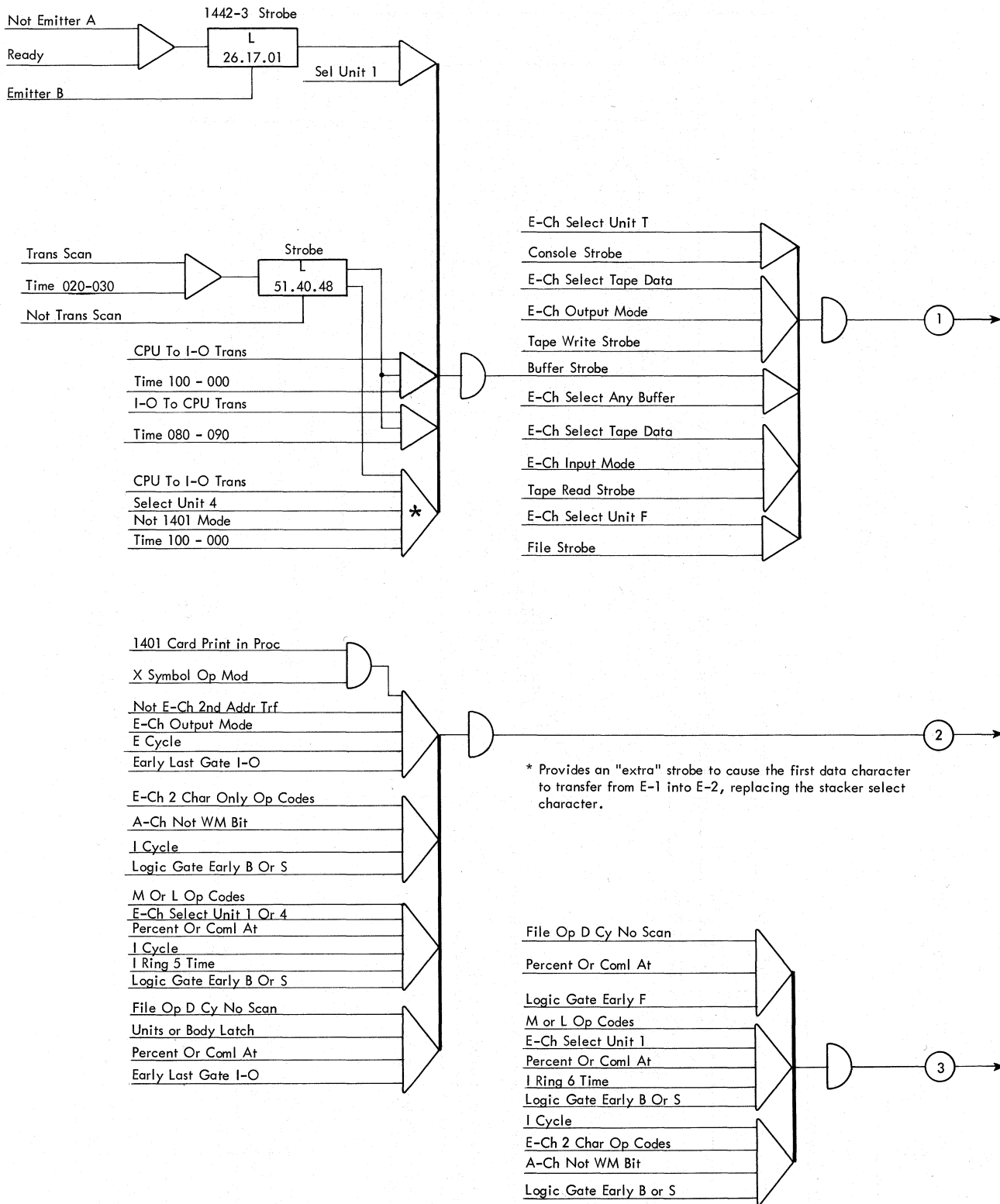
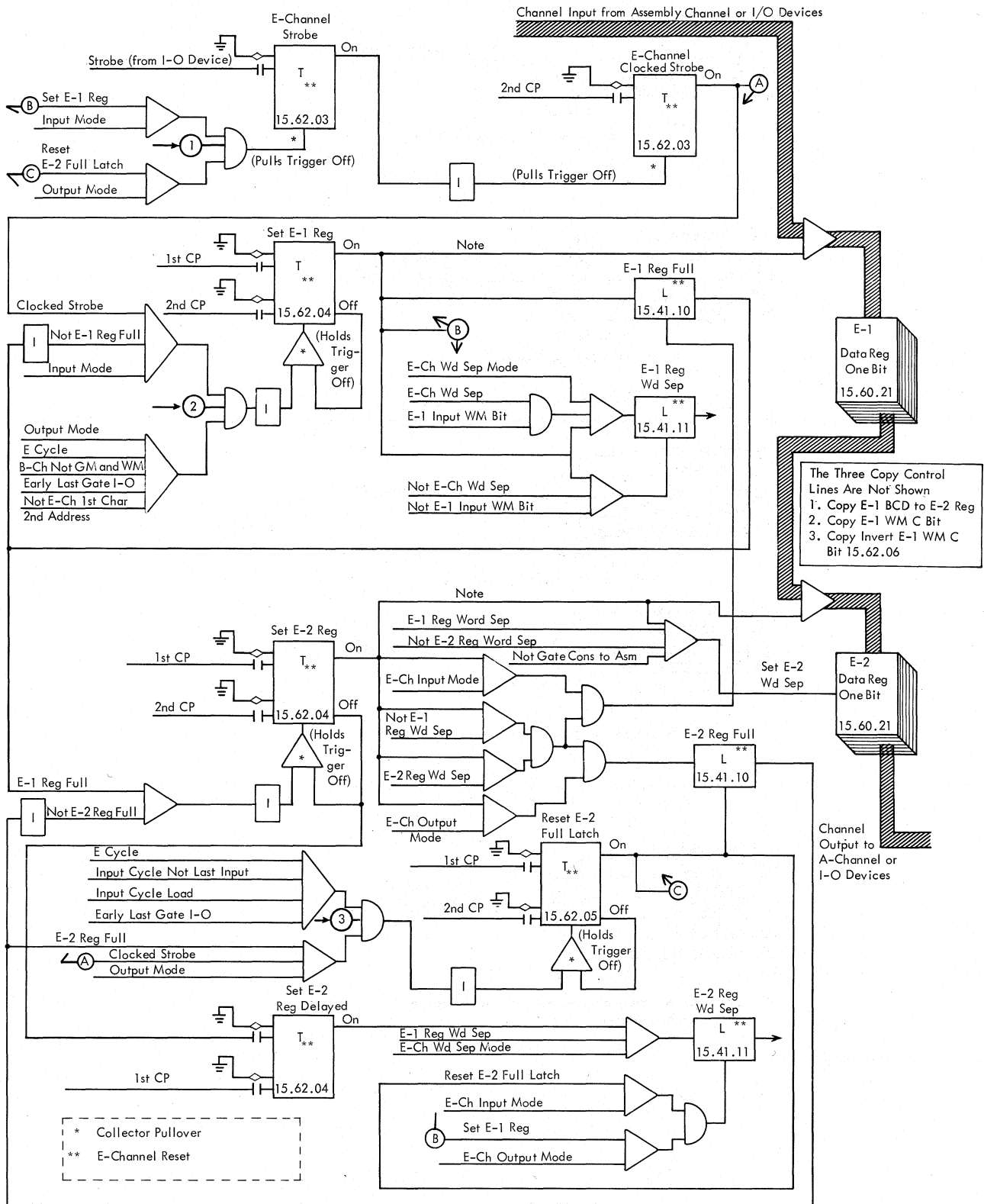
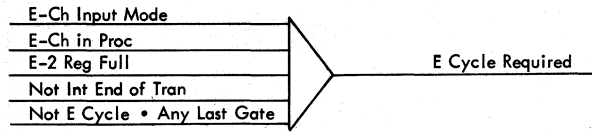


Figure 113. E-Channel Strobe

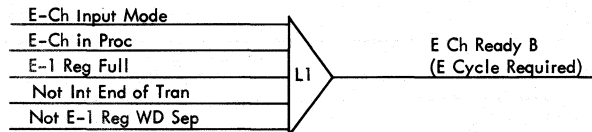


Note: For Console Input Operation "Gate Console to Assembly" forces the "Set E1 Reg" and "Set E2 Reg" lines because no clock pulses are available to turn on the triggers.

Figure 114. Channel Register Operation

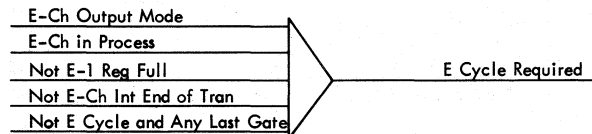


Input - With or Without Process Overlap

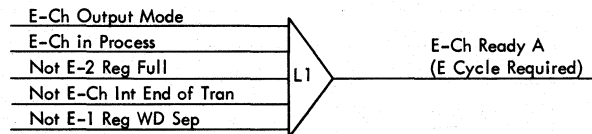


Input - With Process Overlap

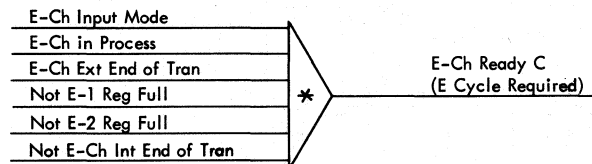
L1 is MFI designation for overlap on channel one



Output - With or Without Process Overlap

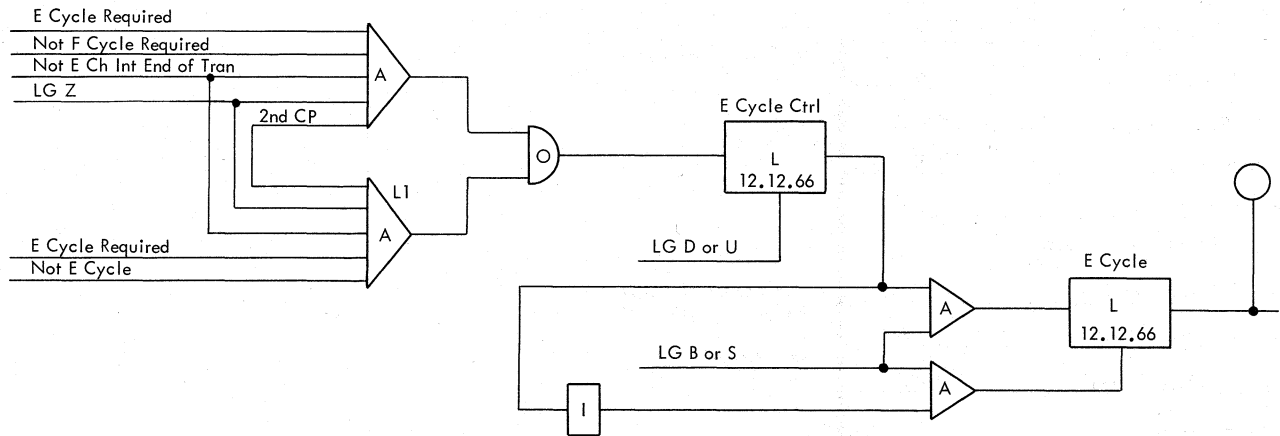


Output - With Process Overlap



* Forces an extra E cycle to check for a GM - WM at end of input field in core storage

Figure 115. E-Cycle Required



(E Cycle has priority over F Cycle unless previous cycle was an E Cycle)

L1 = MFI code for overlap on channel one.

L2 = MFI code for overlap on channel two

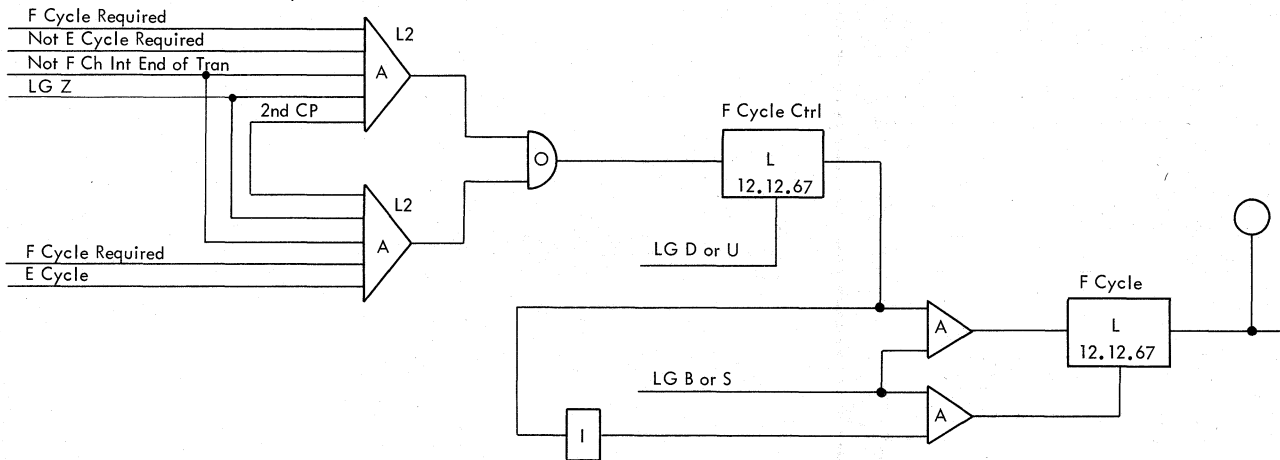


Figure 116. E- and F-Cycle Control

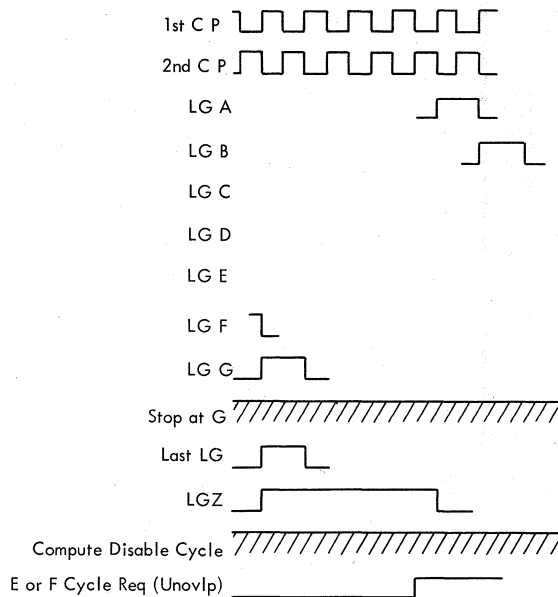


Figure 117. Compute Disable Cycle

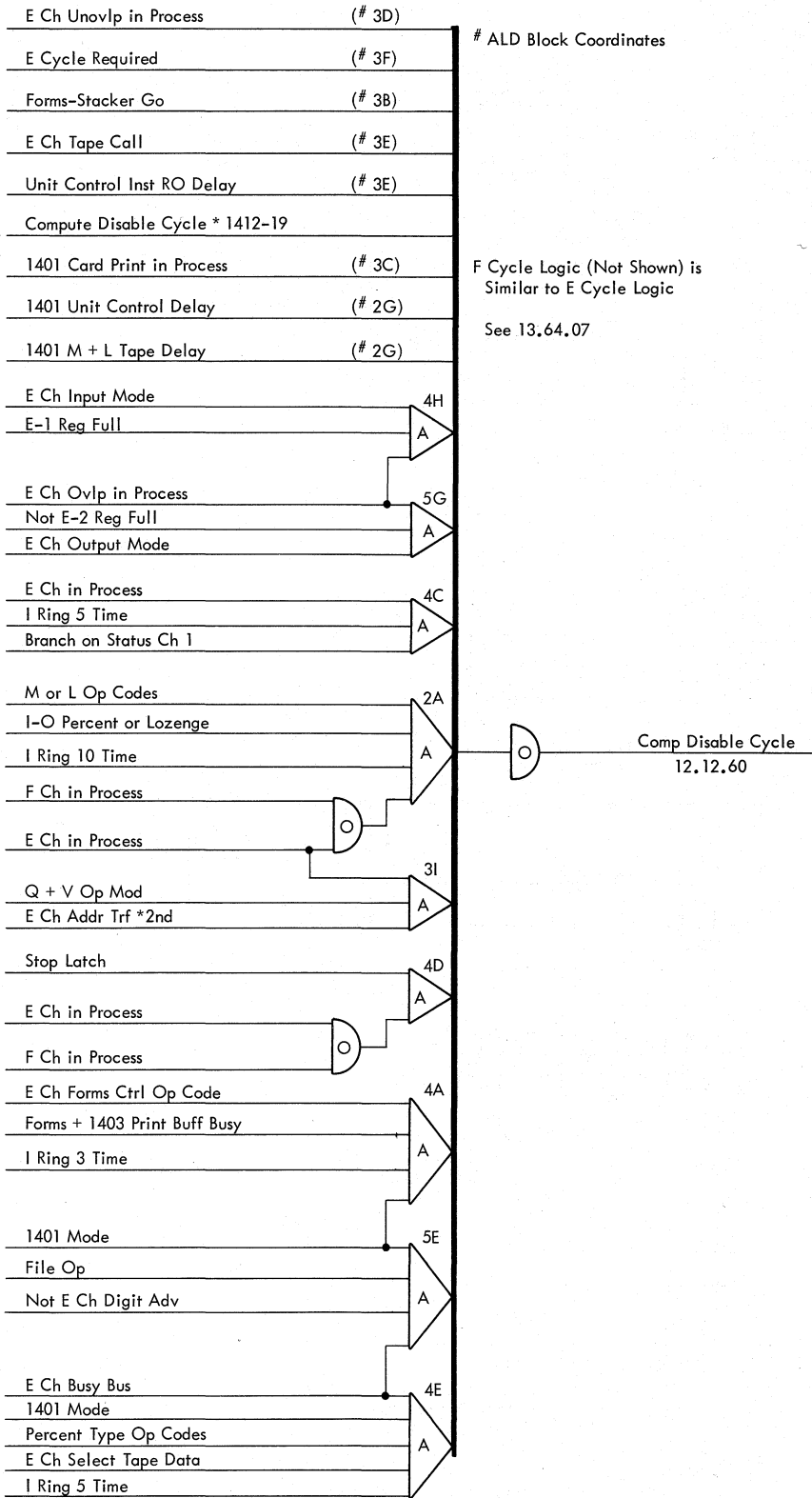


Figure 118. Compute Disable

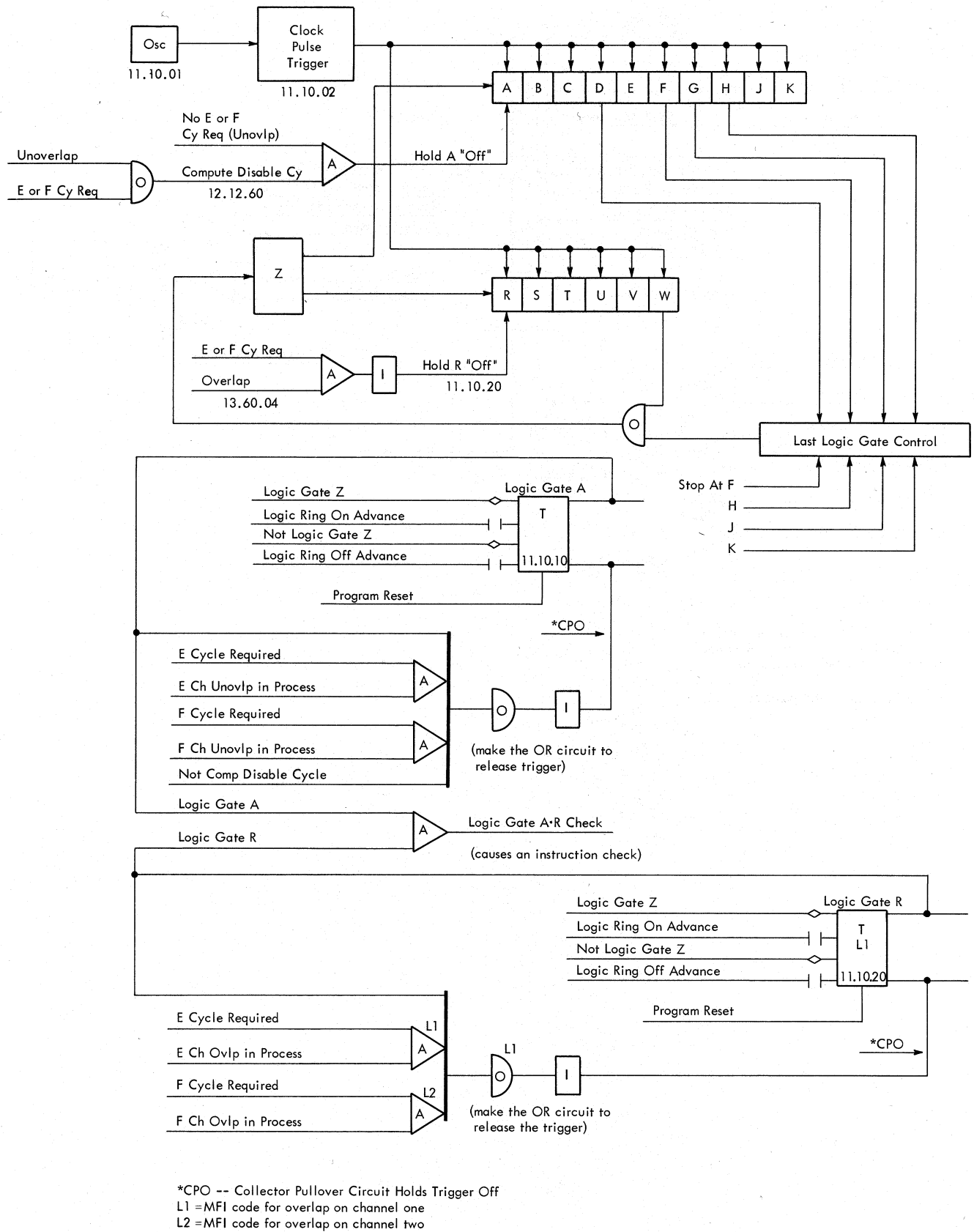
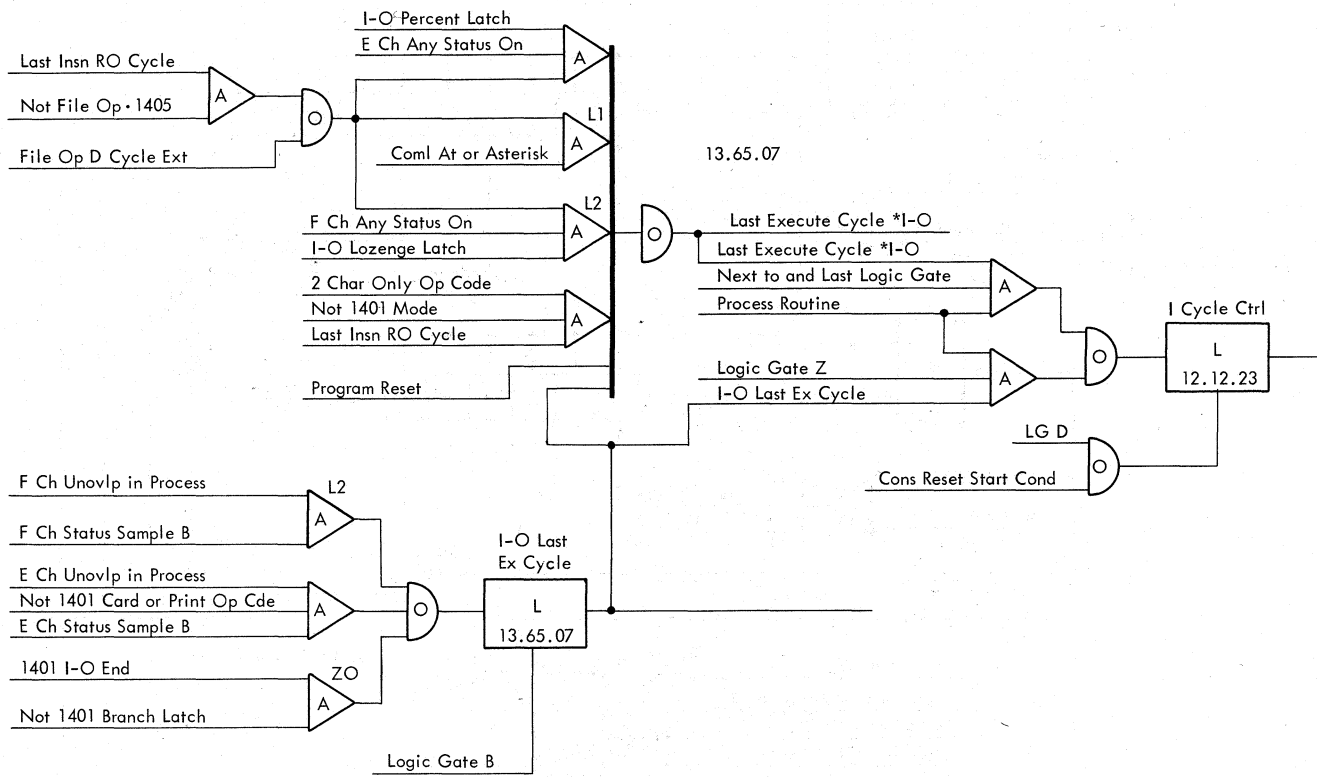


Figure 119. Logic Ring Control



L1 =MFI code for overlap on channel one
 L2 =MFI code for overlap on channel two
 ZO=MFI code for 1401 compatibility

Figure 120. I-O Last Execute

COMMENT SHEET

I411 INPUT-OUTPUT OPERATIONS

CUSTOMER ENGINEERING INSTRUCTION-REFERENCE, 223-2692

FROM

NAME _____

OFFICE NO. _____

FOLD

CHECK ONE OF THE COMMENTS AND EXPLAIN IN THE SPACE PROVIDED

FOLD

- SUGGESTED ADDITION (PAGE _____, TIMING CHART, DRAWING, PROCEDURE, ETC.)
- SUGGESTED DELETION (PAGE _____)
- ERROR (PAGE _____)

EXPLANATION

CUT ALONG LINE

FOLD

FOLD

NO POSTAGE NECESSARY IF MAILED IN U. S. A.
FOLD ON TWO LINES, STAPLE, AND MAIL

FOLD

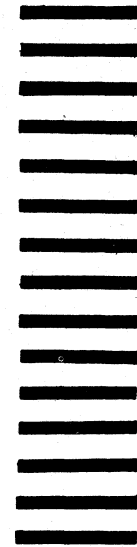
FOLD

FIRST CLASS
PERMIT NO. 81
POUGHKEEPSIE, N. Y.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN U. S. A.

POSTAGE WILL BE PAID BY
IBM CORPORATION
P. O. BOX 390
POUGHKEEPSIE, N. Y.

ATTN: CE MANUALS, DEPARTMENT B96



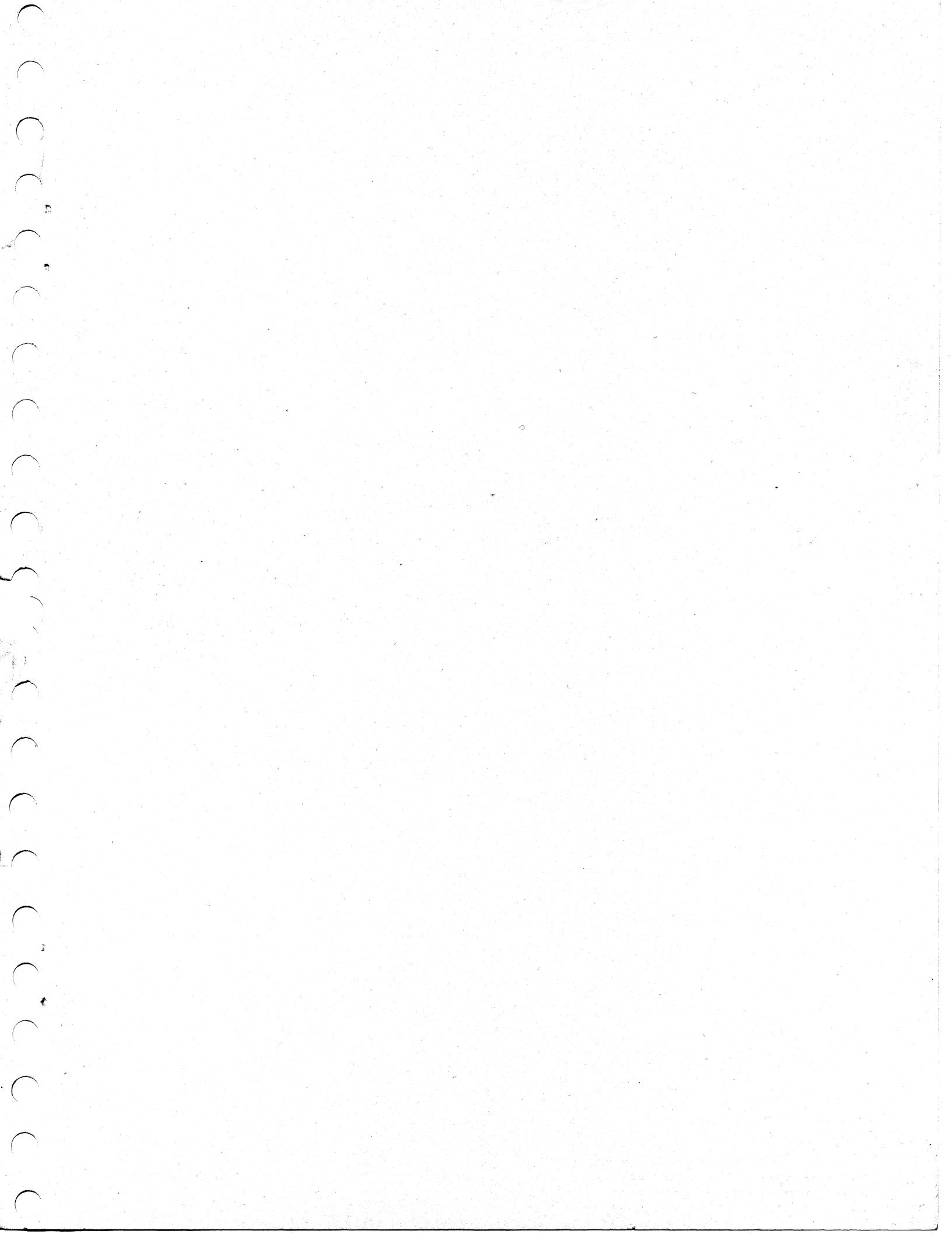
CUT ALONG LINE

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FOLD



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Data Processing Division
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