

OPERATING AND SERVICE MANUAL

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MANUAL

**2767A**

LINE PRINTER

Serial Numbers Prefixed: 976-, 1309-

Manual Part No. 02767-90002

Microfiche Part No. 02767.90002

*Pataprodukte  
2310 printer*

*Pataprodukte  
ribbon # 212738*

HEWLETT  PACKARD

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MANUAL**

**2767A**

**LINE PRINTER**

Serial Numbers Prefixed: 976-, 1309-

Manual Part No. 02767-90002

Microfiche Part No. 02767-90008

## FOREWORD

This manual contains operating and service information for the Hewlett-Packard 2767A Line Printer. The model number 2767A is the HP designation for the standard model 2310 Line Printer manufactured by the Data Products Corporation and modified by Hewlett-Packard. This manual also applies to HP option 015, which is the 230-volt 50-hertz version of the line printer.

The content of this manual was prepared by the Data Products Corporation.

### MANUAL CHANGE

Page 1-4, table 1-3. In the ITEM column under "Ribbon" add the following: Hewlett-Packard part no. 9300-0427 or Data Products part no. 212738-1 may be used as a replacement ribbon.

1	AM 21 or AM 10	character memory
2	AG 17	logic gate
3	AG 18	
4	AG 19 or AG 45	
5	AG 20	
6	AT 13	timing control
7	_____	delay control
8	_____	
9	AG 32	
10	_____	
11	AS 11 or AS 14	positive driver
12	_____	receiver
13	_____	
14	AK 10	
15	AS 13	transducer
16	AZ 19	hammer interlock
17	<del>AH 10</del> AZ 18	hammer driver
18	<del>AZ 18</del> AH 10	
19	AH 10	
20	AH 10	

## LIST OF EFFECTIVE PAGES

Total number of effective pages is 399, as follows:

Page No.	Issue	Page No.	Issue
<u>Vol. I</u>		4-54 thru 4-57	Original
Title	Revision J	4-58	Revision B
i	Revision F	4-59 and 4-60	Original
ii	Original	5-1	Revision G
iii	Revision D	5-2	Revision F
iv thru vi	Original	5-3	Revision F
vii	Revision J	5-4	Original
viii thru xi	Revision H	5-5 thru 5-7b	Revision G
1-1	Revision F	5-8	Revision H
1-2 thru 1-6	Original	5-9 thru 5-17	Original
1-7	Revision G	5-18	Revision H
1-8 thru 1-14	Original	5-19 and 5-20	Original
1-15	Revision H	5-21 and 5-22	Revision H
1-16	Revision A	5-23 thru 5-26	Original
1-17	Revision E	5-27	Revision H
1-18	Original	5-28	Revision H
1-19 and 2-1	Revision B	5-29	Original
2-2	Original	5-30	Revision H
3-1	Original	5-31 and 5-32	Original
3-2	Revision G	5-33	Revision H
3-3	Revision H	5-34	Original
3-4	Revision G	5-35	Revision J
3-5 thru 3-7	Original	5-36 and 5-37	Revision H
3-8	Revision H	5-38	Original
3-9 and 3-10	Original	5-39	Revision H
4-1	Original	5-39a	Revision F
4-2	Revision A	5-40	Revision H
4-3 thru 4-8	Original	5-41 and 5-42	Revision B
4-9 and 4-10	Revision B	5-43 and 5-44	Revision F
4-11 thru 4-19	Original	5-45 and 5-46	Original
4-20	Revision B	5-47	Revision B
4-21	Original	5-48	Original
4-22 thru 4-26	Revision B	6-1 thru 6-5	Original
4-27 thru 4-33	Original	6-6	Revision F
4-34	Revision B	6-7	Original
4-35 thru 4-37	Original	6-8	Revision E
4-38	Revision B	6-9	Original
4-39	Original	6-10 thru 6-12	Revision B
4-40 thru 4-42	Revision B	6-12a and 6-12b	Original
4-43 thru 4-48	Original	6-13 thru 6-15	Revision B
4-49	Revision B	6-16	Revision D
4-50	Original	6-17	Revision E
4-51 and 4-52	Revision B	6-18 and 6-19	Original
4-53	Revision B	6-20 thru 6-22	Revision B
		6-23 thru 6-24	Original

## LIST OF EFFECTIVE PAGES (Cont'd)

Page No.	Issue	Page No.	Issue
6-25	Revision E	<u>Vol. II</u>	
6-26	Original	Title	Revision J
6-27 and 6-28	Revision B	i	Revision F
6-29	Original	ii and iii	Revision G
6-30	Revision B	9-1/2	Revision F
6-31 thru 6-33	Original	9-3/4 and 9-5/6	Revision G
6-34	Revision D	9-7/8	Revision F
6-35 and 6-36	Revision E	9-9/10	Revision G
6-37	Original	9-11 and 9-12	Revision F
6-38	Revision J	9-13/14	Revision G
6-39	Revision B	9-15 thru 9-27	Revision F
6-40 and 6-41	Original	9-28	Revision G
6-42	Revision B	9-29 and 9-30	Revision F
6-43 and 6-44	Original	9-31/32	Revision G
6-45	Revision B	9-33/34 thru 9-48	Revision F
7-1	Revision H	9-49/50	Revision G
7-2 and 7-3	Original	9-51 thru 9-125	Revision F
7-4 and 7-5	Revision B	9-126 and 9-127	Revision J
7-6 and 7-7	Original	9-128 thru 9-135	Revision F
7-8 and 7-9	Revision B	9-136 thru 9-138	Revision G
7-10	Revision F	9-139 and 9-140	Revision F
7-11	Original		
7-12	Revision B		
7-13 and 7-14	Original		
7-15	Revision A		
7-16	Revision B		
7-17	Revision D		
7-18 and 7-19	Original		
7-20 and 7-21	Revision B		
7-22 and 7-23	Original		
7-24 thru 7-30	Revision H		
7-31 and 7-31a	Original		
7-32 thru 7-41	Original		
8-1 and 8-2	Revision B		
8-3 thru 8-8	Original		
8-9	Revision B		
8-10 and 8-11	Original		
8-12	Revision B		
8-13 thru 8-20	Original		
8-21	Revision B		
8-22 thru 8-24	Original		
8-25	Revision A		

## CHANGE RECORD

REVISION LEVEL	DATE	CHANGES INCORPORATED		PAGE NOS. AFFECTED	BRIEF DESCRIPTION
		E.O. NO.	DPC REVISION PACKAGE NO.		
E	5-73	NA	P2310-4	5-39a, 6-17 and 6-26	Correct figure references and procedure.
		19211	P2310-5	6-25	Circuit change (Fig. 6-14)
		19210	P2310-6	5-35 and 5-36	Adjustment tolerance change.
		19246 and 19296	P2310-7	1-17 and 6-8	Circuit and part number change.
F	7-28	NA	P2310-8	viii, 5-3, 5-18, 5-22, 5-27, 5-37, 5-39, 6-15, 7-1, and 7-30	Circuit card replacement.
		NA	P2310-9	1-1, 5-21, 5-39a, 5-43, 5-44, and 7-27	Change to reflect addition of Volume II
G	9-19	19770	P2310-10	9-13/14	Part change.
		NA	NA	Vol. I: Title, viii, x, xi, 1-7, 3-2, 3-4, 3-9, 5-1, 5-5 thru 5-7b Vol. II: Title, ii, iii, 9-3/4, 9-5/6, 9-9/10, 9-13/14, 9-28, 9-31/32, 9-49/50, 9-136 thru 9-138	Record change.

## CHANGE RECORD

REVISION LEVEL	DATE	CHANGES INCORPORATED		PAGE NOS. AFFECTED	BRIEF DESCRIPTION
		E.O. NO.	DPC REVISION PACKAGE NO.		
H	11-9 73	19906	P2310-11, 12,13	vii, viii, ix, x, xi, 1-15, 3-3, 3-8, 5-8, 5-18, 5-21, 5-22, 5-27, 5-28, 5-30, 5-33, 5-35, 5-36, 5-37, 5-39, 5-40, 7-1, 7-24, 7-25, 7-26, 7-27, 7-28, 7-29, 7-30	
J	4-22 74	23278	P2310-14	vii, 6-38, 9-126, 9-127	Circuit change
		23442	P2310-15	5-35	Adjustment tolerance change

## VOLUME I

## TABLE OF CONTENTS

Section	Title	Page
I	GENERAL DESCRIPTION .....	1-1
	1-1 Introduction .....	1-1
	1-3 Purpose of Equipment .....	1-1
	1-5 Specifications and Leading Particulars .....	1-1
	1-7 Physical Description .....	1-6
	1-9     Mechanics A2 .....	1-6
	1-11         Drum Gate A2A1 .....	1-9
	1-14         Hammer Bank A2A2 .....	1-13
	1-17         Paper Feed A2A3 .....	1-13
	1-21         Card Cage A3 .....	1-13
	1-23         Power Supply A4 .....	1-16
	1-25         Control Panel A5 .....	1-17
	1-27     Functional Description .....	1-17
	1-29         Print Cycle .....	1-17
	1-31         Character Drum .....	1-19
	1-33         Interlock .....	1-19
II	INSTALLATION .....	2-1
	2-1 Introduction .....	2-1
	2-3 Space Requirements .....	2-1
	2-5 Unpacking .....	2-1
	2-7 Preliminary Operation .....	2-1
III	OPERATING INSTRUCTIONS .....	3-1
	3-1 Introduction .....	3-1
	3-3 Operating Controls and Indicators .....	3-1
	3-4     Control Panel A5 Controls and Indicators .....	3-1
	3-6     Power Supply A4 Maintenance Panel Controls and Indicators .....	3-2
	3-8     Mechanics A2 Controls and Adjustments .....	3-3
	3-10    Operating Procedures .....	3-3
	3-12    Preliminary Procedures .....	3-3
	3-13    Ribbon Installation .....	3-3
	3-15    Paper Loading .....	3-8
	3-17    Paper Positioning (Vertical) .....	3-8
	3-19    On-Line Startup Procedure .....	3-9
	3-21    Shutdown Procedure .....	3-10
IV	PRINCIPLES OF OPERATION .....	4-1
	4-1 Introduction .....	4-1
	4-3 General Description .....	4-1



## TABLE OF CONTENTS (Continued)

Section	Title	Page
4-11	Interface .....	4-3
4-13	Printer/User System Interface Signals .....	4-5
4-15	Coded Character Set .....	4-5
4-17	Format Control .....	4-7
4-19	On-Line Printer Operation .....	4-8
4-21	Printer Power .....	4-8
4-23	Power Supply A4 .....	4-8
4-29	Voltage Regulator AV-10 .....	4-11
4-38	Overtemperature Sensor TB1 .....	4-13
4-39	Ribbon Control AZ-15 .....	4-14
4-48	Paper Feed Control AP-10 .....	4-16
4-51	Ramp Generator Operation .....	4-16
4-53	Paper Feed Amplifier Operation .....	4-19
4-55	Top-of-Form Cam .....	4-20
4-58	Overspeed Detector .....	4-20
4-60	Interlock and Fault Detect .....	4-20
4-62	Hammer Interlock AZ-19 .....	4-20
4-63	Drum Gate (Closed) .....	4-23
4-68	Drum Gate (Open) .....	4-23
4-69	Paper Out .....	4-23
4-74	VCL and +5V Supplies .....	4-24
4-79	VCL Regulator .....	4-24
4-82	Print Inhibit .....	4-24
4-83	Printer States .....	4-25
4-87	Clock Generation .....	4-25
4-91	Master Clear State .....	4-26
4-93	Master Clear Operation .....	4-26
4-94	Power On .....	4-26
4-104	Drum Speed Monitor .....	4-28
4-105	Manual Input .....	4-28
4-107	Load Data State.....	4-28A
4-110	On-Line Enable .....	4-28A
4-113	Interface Timing .....	4-33
4-122	Load Data Operation .....	4-34
4-124	Twenty Printable Characters .....	4-34
4-138	Less Than 20 Printable Characters and Control Character .....	4-36
4-144	Control Character Only .....	4-36
4-146	PF Command .....	4-36
4-154	FF Command .....	4-37
4-155	CR Command .....	4-38
4-160	Scan and Print State .....	4-38
4-162	Scan and Print Operation .....	4-38
4-170	Character Clock Fan-Out .....	4-41
4-173	Character Clock Sync .....	4-41
4-179	Nonprintable Code Detector .....	4-43
4-182	Comparator .....	4-43
4-191	Character Counter .....	4-44

## TABLE OF CONTENTS (Continued)

Section	Title	Page
4-199	Hammer Register and Driver .....	4-48
4-209	Paper Advance State .....	4-49
4-211	Paper Advance Operation .....	4-52
4-217	Line Strobe Sync .....	4-52
4-222	Delay Counter .....	4-53
4-227	Zone Change State .....	4-56
4-229	Zone Change Operation .....	4-56
4-232	Zone Control AZ-18 .....	4-56
4-242	CR Command .....	4-58
4-244	Off-Line Printer Operation .....	4-59
4-246	Paper Step Switch .....	4-59
4-248	Paper Step Operation .....	4-59
4-251	Top Of Form Switch .....	4-59
4-253	Top-Of-Form Operation .....	4-59
4-255	Drum Gate Open .....	4-59
4-259	Drum Gate Closed .....	4-60
4-260	Print Cycle Initiate .....	4-60
V	MAINTENANCE AND TROUBLESHOOTING .....	5-1
5-1	Introduction .....	5-1
5-6	Inspection and Preventive Maintenance .....	5-1
5-8	Maintenance Test .....	5-1
5-10	Equipment Required .....	5-1
5-12	Preliminary Checkout Procedure .....	5-8
5-14	Performance Checkout Procedure .....	5-9
5-17	Calibration .....	5-18
5-19	Calibration of Power Supply A4 .....	5-18
5-20	+5V Calibration .....	5-18
5-22	+12V Calibration .....	5-18
5-24	+28V Calibration .....	5-19
5-26	Calibration of Driver A3A11 Reference Voltage .....	5-19
5-28	Calibration of Receiver A3A14 Reference Voltage.....	5-19
5-30	Calibration of Hammer Driver Current .....	5-20
5-32	Calibration of Hammer Flight Time .....	5-22
5-34	Calibration of Paper Feed Velocity Command .....	5-26
5-36	Mechanical Adjustments .....	5-27
5-38	Paper Drive Belt Tension Adjustment .....	5-28
5-40	Drum Motor Belt Tension Adjustment .....	5-28
5-42	Tractor Adjustment .....	5-28
5-44	Paper Tension Bar and Spring Adjustment .....	5-33
5-46	Line Strobe Pickup Adjustment .....	5-35
5-48	Character Pickup Adjustment .....	5-35
5-50	Index Pickup Adjustment .....	5-36
5-52	Character Code Wheel Adjustment .....	5-37
5-54	Index Wheel Adjustment .....	5-39
5-55A	Top Of Form Cam Switch Adjustment .....	5-39
5-56	Removal and Replacement of Assemblies .....	5-39A
5-58	Preliminary Procedure .....	5-40

## TABLE OF CONTENTS (Continued)

Section	Title	Page
5-60	Hammer Assembly .....	5-40
5-62	Drum Motor Conversion to 50 Hz Operation .....	5-43
5-64	Lubrication .....	5-43
5-66	Troubleshooting .....	5-44
VI	DRAWINGS.....	6-1
6-1	Introduction.....	6-1
6-3	Drawings.....	6-1
6-5	Logic Symbols.....	6-1
6-8	Active State Indicator.....	6-3
6-12	J-K Master/Slave Flip-Flop.....	6-3
6-16	J-K Flip-Flop Operation.....	6-4
6-18	Dc Set.....	6-4
6-20	Dc Reset.....	6-4
6-22	Set With Clock.....	6-4
6-26	Reset With Clock.....	6-5
6-30	Inputs J and K High.....	6-5
6-32	Inputs J and K Low.....	6-5
6-34	Inputs E and P Low.....	6-5
VII	OPTIONS.....	7-1
7-1	Introduction.....	7-1
7-3	Negative Logic.....	7-1
7-6	Calibration of Inverting Receiver AK-11 Reference Voltage.....	7-6
7-8	Calibration of Negative Driver AJ-10 Reference Voltage.....	7-7
7-10	Zone Select.....	7-7
7-13	Zone Select Implementation.....	7-8
7-15	Zone Select Operation.....	7-8
7-18	Data Not In Memory - Paper Not Moving.....	7-8
7-29	Data Not In Memory - Paper Moving.....	7-13
7-37	Data In Memory.....	7-13
7-46	Parity Check.....	7-14
7-51	Parity Check Implementation.....	7-15
7-53	Parity Check Operation.....	7-15
7-60	Code Conversion.....	7-18
7-62	Code Conversion Implementation.....	7-18
7-64	Code Conversion Operation.....	7-18
7-77	Self-Test.....	7-24
7-79	Self-Test Procedure.....	7-24
7-81	Self-Test Operation.....	7-30
7-83	Zone 1 - Shifting Pattern.....	7-30
7-91	Zones 1 and 2 - Shifting Pattern.....	7-34
7-94	Zones 1 Thru 3 - Shifting Pattern.....	7-34
7-97	Zones 1 Thru 4 - Shifting Pattern.....	7-34
7-100	E Pattern.....	7-35
7-102	Zone Select.....	7-35

## TABLE OF CONTENTS (Continued)

Section	Title	Page
7-104	Parity Generator.....	7-35
7-106	Character Fonts.....	7-35
7-108	96-Character Set.....	7-35
7-110	Coded Character Set.....	7-36
7-112	Nonprintable Code Detector.....	7-36
7-114	Static Eliminator.....	7-36
7-116	Static Eliminator Installation.....	7-36
7-118	Ground and Cable Check.....	7-38
7-120	Paper Receptacle.....	7-41
7-122	Pedestal.....	7-41
VIII	GLOSSARY.....	8-1
8-1	Introduction.....	8-1
8-3	Signal Identification List.....	8-1
8-5	Glossary.....	8-13

## LIST OF ILLUSTRATIONS

Figure	Title	Page
1-1	✓ LINE/PRINTER Model 2310.....	1-2
1-2	LINE/PRINTER, Rear View.....	1-3
1-3	LINE/PRINTER, Front Door Open (Drum Gate Unlatched).....	1-7
1-4	LINE/PRINTER, Rear Door Open (Card Cage Unlatched).....	1-8
1-5	Drum Gate and Drum Motor Interlock, and Top-of-Form Cam Switch Locations (Mechanics A2 Assembly Removed).....	1-9
1-6	Character and Index Magnetic Pickup Locations.....	1-10
1-7	Line Strobe Magnetic Pickup Location.....	1-11
1-8	Drum Gate A2A1, Ribbon Installed.....	1-12
1-9	Paper Tractors and Egress Slot.....	1-14
1-10	LINE/PRINTER, Paper Installed.....	1-14
1-11	Paper Out Switch S4 and S5 Locations.....	1-15
1-12	LINE/PRINTER Model 2310, Simplified Block Diagram.....	1-18
2-1	LINE/PRINTER Model 2310 Installation.....	2-2
3-1	Control Panel A5, Controls and Indicators.....	3-1
3-2	Power Supply A4 Maintenance Panel, Controls and Indicators.....	3-2
3-3	Mechanics A2 Controls.....	3-4
3-4	Mechanics A2 Adjustments.....	3-5
3-5	Drum Gate A2A1 Ribbon Installation.....	3-6
3-6	Installation of Ribbon Core on Fixed Ribbon Holder.....	3-7
3-7	Paper Alignment to Top-of-Form Indicators.....	3-9
4-1	LINE/PRINTER Model 2310 System Block Diagram.....	4-2
4-2	Printer/User System Simplified Interface Diagram.....	4-4
4-3	Interface Signal Lines Timing Diagram.....	4-6
4-4	Power Supply A4 Simplified Block Diagram.....	4-9
4-5	Power Supply A4 Regulation Simplified Block Diagram.....	4-10
4-6	Voltage Regulator AV-10 Functional Block Diagram.....	4-12
4-7	Overtemperature Sensor TB1 .....	4-13

## LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
4-8	Ribbon Control AZ-84 Functional Block Diagram.....	4-15
4-9	Paper Feed Control AP-10 Functional Block Diagram.....	4-17
4-10	Paper Feed Control Timing Diagram.....	4-18
4-11	Top-of-Form Advance Timing Diagram.....	4-21
4-12	Hammer Interlock AZ-19 Functional Block Diagram.....	4-22
4-13	Master Clear State (Power On Sequence) Flow and Timing Diagram...	4-27
4-14	On-Line Enable and Interface Timing Diagram.....	4-29
4-15	Load Data State (20 Printable Characters) Flow and Timing Diagram.....	4-30
4-16	Load Data State (Less Than 20 Printable Characters and Control Character) Flow Diagram.....	4-31
4-17	Load Data State (Control Character Only) Flow and Timing Diagram.	4-32
4-18	Scan and Print State Flow and Timing Diagram.....	4-39
4-19	Time Slot Decode Timing Diagram.....	4-40
4-20	25-Character Buffer Memory Loaded.....	4-41
4-21	Character Counter Reset Timing Diagram.....	4-48
4-22	Hammer and Zone Select Matrix Diagram.....	4-50
4-23	Paper Advance State Flow and Timing Diagram.....	4-51
4-24	Line Strobe Sync Timing Diagram.....	4-54
4-25	Delay Counter Timing Diagram.....	4-55
4-26	Zone Change State Flow and Timing Diagram.....	4-57
5-1	LINE/PRINTER Model 2310 Interconnecting Diagram.....	5-2
5-2	Card Location Chart.....	5-3
5-3	Power Transformer A4T1 Primary Winding Wiring Diagram.....	5-4
5-4	Power Supply A4, Test Jacks and Adjustment Locations.....	5-14
5-5	Hammer Driver Current Test Probe Connection.....	5-15
5-6	Hammer Driver Current Waveform.....	5-16
5-7	Printout Quality Check.....	5-17
5-8	Card Cage A3 Adjustment Locations.....	5-21
5-9	Hammer Adjustment and Mounting Screw Locations (Hammer Bank, Rear View).....	5-23
5-10	Hammer Flight Time Waveform.....	5-25
5-11	Hammer Flight Time Waveform Magnified.....	5-26
5-12	Paper Feed Velocity Command Waveform.....	5-27
5-13	Paper Drive Belt Tension Adjustment Location.....	5-29
5-14	Paper Drive Belt Tension Adjustment.....	5-30
5-15	Drum Belt Tension Adjustment Location.....	5-31
5-16	Tractor Adjustment Locations.....	5-32
5-17	Tractor Alignment Gauge Installation.....	5-32
5-18	Paper Tension Bar Adjustment.....	5-34
5-19	Test Strip Placement for Paper Tension Spring Adjustment.....	5-34
5-20	Spring Gauge Test of Paper Tension Spring.....	5-34
5-21	Paper Tension Spring Adjustment.....	5-34
5-22	Line Strobe Pickup Adjustment.....	5-36
5-23	Character Code Wheel and Index Wheel Adjustment.....	5-38
5-24	Hammer Bank A2A2 Cover (Top Cover Shown Removed).....	5-40
5-25	Hammer Assembly Taper Pin Removal.....	5-42

## LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
5-26	Hammer Assembly.....	5-42
5-27	Hammer Assembly Taper Pin Installation.....	5-43
6-1	LINE/PRINTER Model 2310 Harness Assembly Schematic Diagram.....	6-6
6-2	Hammer Bank A2A2 Harness Assembly Schematic Diagram.....	6-7
6-3	Drum Gate A2A1 Schematic Diagram (Printer Serial Numbers 026 Thru 128).....	6-8
6-4	Input/Output Harness Assembly Schematic Diagram.....	6-9
6-5	Control Panel A5 Schematic Diagram.....	6-10
6-6	25-Character Memory AM-10 Logic Diagram.....	6-11
6-6a	32-Character Memory AM-21 Logic Diagram.....	6-12a
6-7	Logic Gate I AG-17 Logic Diagram.....	6-13
6-8	Logic Gate II AG-18 Logic Diagram.....	6-14
6-9	Logic Gate III AG-45 Logic Diagram.....	6-15
6-10	Logic Gate IV AG-20 Logic Diagram.....	6-16
6-11	Timing Control AT-13 Logic Diagram.....	6-17
6-12A	Positive Driver AJ-11 Schematic Diagram.....	6-18
6-12B	Positive Driver AJ-14 Schematic Diagram.....	6-20
6-13	Receiver AK-10 Schematic Diagram.....	6-22
6-14	Transducer Amplifier AS-13 Logic Diagram.....	6-24
6-15	Hammer Interlock AZ-19 Logic Diagram.....	6-26
6-16	Zone Control AZ-18 Logic Diagram.....	6-27
6-17	Hammer Driver AH-10 Logic Diagram.....	6-29
6-18	Cable Plug Card AZ-14 Schematic Diagram.....	6-31
6-19	Drum Gate A2A1 Schematic Diagram (Printer Serial Number 129 and Up).....	6-32
6-20	Drum Motor Interlock Schematic Diagram.....	6-33
6-21	Hammer Interlock AZ-19 Schematic Diagram.....	6-34
6-22	Paper Feed Control AP-10 Schematic Diagram.....	6-35
6-23	Voltage Regulator AV-10 Schematic Diagram.....	6-36
6-24	Ribbon Control AZ-84 Logic Diagram.....	6-37
6-25	Power Supply A4 Schematic Diagram.....	6-39
6-26	Hammer Drivers To Cable Plug Cards Interconnecting Diagram.....	6-40
6-27	Hammer Driver Register Logic Diagram.....	6-41
6-28	Delay Control and Gates AG-32 Logic Diagram.....	6-42
6-29	J-K Flip-Flop Logic Diagram.....	6-44
6-30	+12V Monitor Schematic Diagram.....	6-45
7-1	Inverting Receiver AK-11 Schematic Diagram.....	7-2
7-2	Negative Driver AJ-10 Schematic Diagram.....	7-4
7-3	Zone Select Option Interconnecting Diagram.....	7-9
7-4	Zone Select AL-12 Logic Diagram.....	7-10
7-5	Zone Select Option Timing Diagram.....	7-11
7-6	Parity Option Interconnecting Diagram.....	7-16
7-7	Parity AL-11 Logic Diagram.....	7-17
7-8	Code Conversion Option Block Diagram.....	7-19
7-9	Matrix Driver AZ-67 Logic Diagram.....	7-20
7-10	Example of Decode Matrix Mechanization.....	7-23
7-11	Negative Logic Self-Test Adapter Schematic Diagram.....	7-26
7-12	Self-Test AL-27 Card Installed (Negative Logic).....	7-28
7-13	Self-Test AL-27 Card Installed (Positive Logic).....	7-29
7-14	Self-Test AL-27 Logic Diagram.....	7-31
7-14a	Self-Test AL-27 Logic Diagram.....	7-31a

## LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
7-15	Shifting Pattern Printout (Zones 1 Thru 4).....	7-33
7-16	Portion of Logic Gate I AG-17 Schematic Diagram.....	7-37
7-17	Static Eliminator Assembly Installed (Printer Serial Numbers 012 Thru 200).....	7-39
7-18	Static Eliminator Assembly Installed (Printer Serial Number 201 and Up).....	7-40
7-19	Model 2310 LINE/PRINTER Paper Receptacle and Pedestal Mount Installation.....	7-41

## LIST OF TABLES

Table	Title	Page
1-1	Power Requirements.....	1-3
1-2	Environmental Requirements.....	1-4
1-3	Paper and Ribbon Requirements.....	1-4
1-4	Physical Characteristics.....	1-5
1-5	Performance Characteristics.....	1-5
1-6	Card Cage A3 Standard Complement.....	1-15
1-7	Card Cage A4A4 Complement.....	1-16
1-8	Power Supply Fuse Complement.....	1-17
1-9	Character Font and Sequence of Standard 64-Character Drum.....	1-19
3-1	Control Panel A5 Controls and Indicators.....	3-2
3-2	Power Supply A4 Maintenance Panel Controls and Indicators.....	3-3
3-3	Mechanics A2 Controls and Adjustments.....	3-5
4-1	Receiver/Driver Characteristics.....	4-3
4-2	Interface Signal Definitions.....	4-5
4-3	Coded Character Set.....	4-7
4-4	Example of DR and CC Complementary Pairs.....	4-44
4-5	Code/Character Relationship.....	4-45
5-1	Inspection and Preventive Maintenance Schedule.....	5-5
5-2	Test Equipment and Special Tools Required.....	5-6
5-3	Preliminary Checkout Procedure.....	5-8
5-4	Performance Checkout Procedure.....	5-10
5-5	Hammer Flight Time Adjustment Test Points.....	5-24
5-6	Troubleshooting Chart.....	5-44
6-1	Common Functions of Two Variables.....	6-3
7-1	Card Cage A3 Option Complement.....	7-1
7-2	Negative Logic Receiver/Driver Characteristics.....	7-6
7-3	Card Cage A6 Complement.....	7-18
7-4	Self-Test AL-27 Switch Functions.....	7-30
7-5	Printer Performance Characteristics (With 96-Character Drum).....	7-35
7-6	Coded Character Set (Standard 96-Character Set).....	7-37
8-1	Signal Identification List (Card Cage A3).....	8-1
8-2	Signal Glossary.....	8-13

VOLUME II  
TABLE OF CONTENTS

<u>Section</u>	<u>Title</u>	<u>Page</u>
IX	MECHANICAL ILLUSTRATIONS	
	Introduction .....	9-1/2

LIST OF ILLUSTRATIONS

<u>Figure</u>	<u>Title</u>	<u>Page</u>
9-1	Line/Printer Assembly .....	9-3/4
9-2	Mechanics Assembly .....	9-9/10
9-3	Mechanics Frame Assembly .....	9-13/14
9-4	Control Panel Assembly .....	9-17
9-5	Top of Form Assembly .....	9-19
9-6	Female Latch Sub-Assembly .....	9-21
9-7	Paper Drive Sub-Assembly .....	9-23
9-8	Vertical Paper Adjust Assembly .....	9-25
9-9	Power Supply Assembly .....	9-27
9-10	Drum Gate Assembly, 64-Character .....	9-33/34
9-11	Drum Sub-Assembly, 64-Character .....	9-39
9-12	Drum Gate Assembly, 96-Character .....	9-41/42
9-13	Drum Sub-Assembly, 96-Character .....	9-47
9-14	Card Cage Assembly .....	9-49/50
9-15	Hammer Bank Assembly .....	9-52
9-16	Hammer Bank Harness Assembly .....	9-54
9-17	Main Harness Assembly .....	9-56
9-18	In/Out Harness Assembly .....	9-58
9-19	Static Eliminator Assembly .....	9-60
9-20	Character Memory, AM-10, Circuit Card Assembly .....	9-62
9-21	Character Memory, AM-21, Circuit Card Assembly .....	9-66
9-22	Logic Gate I, AG-17, Circuit Card Assembly .....	9-68
9-23	Logic Gate II, AG-18, Circuit Card Assembly .....	9-70
9-24	Logic Gate III, AG-45, Circuit Card Assembly .....	9-72
9-25	Logic Gate IV, AG-20, Circuit Card Assembly .....	9-74
9-26	Timing Control, AT-13, Circuit Card Assembly .....	9-76
9-27	Delay Control and Gates, AG-32, Circuit Card Assembly ..	9-78
9-28	Driver, AJ-21, Circuit.....	9-80
9-29	Not Assigned	
9-30	Not Assigned	
9-31	Receiver, AK-10, Circuit Card Assembly .....	9-89
9-32	Inverting Receiver, AK-11, Circuit Card Assembly .....	9-92
9-33	Transducer Amplifier, AS-13, Circuit Card Assembly .....	9-95



## CONTENTS (Cont'd)

## LIST OF ILLUSTRATIONS (Cont'd)

<u>Figure</u>	<u>Title</u>	<u>Page</u>
9-34	Hammer Interlock, AZ-19, Circuit Card Assembly .....	9-98
9-35	Zone Control, AZ-18, Circuit Card Assembly .....	9-102
9-36	Hammer Driver, AH-10, Circuit Card Assembly .....	9-105
9-37	Cable Plug, AZ-14, Circuit Card Assembly .....	9-109
9-38	Cable Plug, AZ-85, Circuit Card Assembly .....	9-110
9-39	Self Test, AL-27, Circuit Card Assembly .....	9-111
9-40	Parity, AL-11, Circuit Card Assembly .....	9-113
9-41	Zone Select, AL-12, Circuit Card Assembly .....	9-115
9-42	Paper Feed Control, AP-10, Circuit Card Assembly .....	9-117
9-43	Voltage Regulator, AV-10, Circuit Card Assembly .....	9-121
9-44	Ribbon Control, AZ-84, Circuit Card Assembly .....	9-125
9-45	SCR Commutating Board, AZ-79, Circuit Card Assembly ....	9-128
9-46	Power Amplifier, AZ-49, Circuit Card Assembly .....	9-130
9-47	Negative Paper Feed Power Amplifier, AZ-51, Circuit Card Assembly .....	9-132
9-48	Bridge Board, AZ-78, Circuit Card Assembly .....	9-134
9-49	Not Assigned	9-136
9-50	Code Conversion, AD-28, Circuit Card Assembly .....	9-139

## LIST OF TABLES

<u>Table</u>	<u>Title</u>	<u>Page</u>
9-1	Line/Printer Assembly .....	9-7/8
9-2	Mechanics Assembly .....	9-11
9-3	Mechanics Frame Assembly .....	9-15
9-4	Control Panel Assembly .....	9-18
9-5	Top of Form Assembly .....	9-20
9-6	Female Latch Sub-Assembly .....	9-22
9-7	Paper Drive Sub-Assembly .....	9-24
9-8	Vertical Paper Adjust Assembly .....	9-26
9-9	Power Supply Assembly .....	9-30
9-10	Drum Gate Assembly, 64-Character .....	9-37
9-11	Drum Sub-Assembly, 64-Character .....	9-40
9-12	Drum Gate Assembly, 96-Character .....	9-45
9-13	Drum Sub-Assembly, 96-Character .....	9-48
9-14	Card Cage Assembly .....	9-51
9-15	Hammer Bank Assembly .....	9-53
9-16	Hammer Bank Harness Assembly .....	9-55
9-17	Main Harness Assembly .....	9-57
9-18	In/Out Harness Assembly .....	9-59
9-19	Static Eliminator Assembly.....	9-61

## CONTENTS (Cont'd)

## LIST OF TABLES (Cont'd)

<u>Table</u>	<u>Title</u>	<u>Page</u>
9-20	Character Memory, AM-10 Assembly Replaceable Parts .....	9-63
9-21	Character Memory, AM-21 Assembly Replaceable Parts .....	9-67
9-22	Logic Gate I, AG-17 Assembly Replaceable Parts .....	9-69
9-23	Logic Gate II, AG-18 Assembly Replaceable Parts .....	9-71
9-24	Logic Gate III, AG-45 Assembly Replaceable Parts .....	9-73
9-25	Logic Gate IV, AG-20 Assembly Replaceable Parts .....	9-75
9-26	Timing Control, AT-13 Assembly Replaceable Parts .....	9-77
9-27	Delay Control and Gates, AG-32 Assembly Replaceable Parts .....	9-79
9-28	Positive Driver, AJ-14 Assembly Replaceable Parts .....	9-81
9-29	Positive Driver, AJ-11 Assembly Replaceable Parts .....	9-84
9-30	Negative Driver, AJ-10 Assembly Replaceable Parts .....	9-87
9-31	Receiver, AK-10 Assembly Replaceable Parts .....	9-90
9-32	Inverting Receiver, AK-11 Assembly Replaceable Parts ...	9-93
9-33	Transducer Amplifier, AS-13 Assembly Replaceable Parts .....	9-96
9-34	Hammer Interlock, AZ-19 Assembly Replaceable Parts .....	9-99
9-35	Zone Control, AZ-18 Assembly Replaceable Parts .....	9-103
9-36	Hammer Driver, AH-10 Assembly Replaceable Parts .....	9-106
9-37	Self Test, AL-27 Assembly Replaceable Parts .....	9-112
9-38	Parity, AL-11 Assembly Replaceable Parts .....	9-114
9-39	Zone Select, AL-12 Assembly Replaceable Parts .....	9-116
9-40	Paper Feed Control, AP-10 Assembly Replaceable Parts ...	9-118
9-41	Voltage Regulator, AV-10 Assembly Replaceable Parts ....	9-122
9-42	Ribbon Control, AZ-84 Assembly Replaceable Parts .....	9-126
9-43	SCR Commutating Board, AZ-79 Assembly Replaceable Parts .....	9-129
9-44	Power Amplifier, AZ-49 Assembly Replaceable Parts .....	9-131
9-45	Negative Paper Feed Power Amplifier, AZ-51 Assembly Replaceable Parts .....	9-133
9-46	Bridge Board, AZ-78 Assembly Replaceable Parts .....	9-135
9-47	Not Assigned	
9-48	Code Conversion, AD-28 Assembly Replaceable Parts .....	9-137 9-140

SECTION I

GENERAL DESCRIPTION

1-1 INTRODUCTION

1-2 This technical manual describes the Model 2310 LINE/PRINTER (hereafter called the printer) manufactured by Data Products Corporation, Woodland Hills, California. The manual contains installation, operating, and maintenance information, and is divided into nine sections as follows:

VOLUME I

- a. Section I - General Description
- b. Section II - Installation
- c. Section III - Operating Instructions
- d. Section IV - Principles of Operation
- e. Section V - Maintenance and Troubleshooting
- f. Section VI - Drawings
- g. Section VII - Options
- h. Section VIII - Glossary

VOLUME II

- a. Section IX - Mechanical Illustrations

1-3 PURPOSE OF EQUIPMENT

1-4 The printer (figures 1-1 and 1-2) is desk-mounted and designed to operate on-line with digital data systems of all types or off-line with paper tape readers, magnetic tape units, card readers, or communication terminals. Reliable and high quality impact line printing is provided with speeds ranging from 356 lines per minute, and 80 columns, to 1110 lines per minute, and 20 columns of printed characters from a 64-character set.

1-5 SPECIFICATIONS AND LEADING PARTICULARS

1-6 Tables 1-1 through 1-5 list the power requirements, environmental requirements, paper and ribbon requirements, physical characteristics, and performance characteristics for the printer.

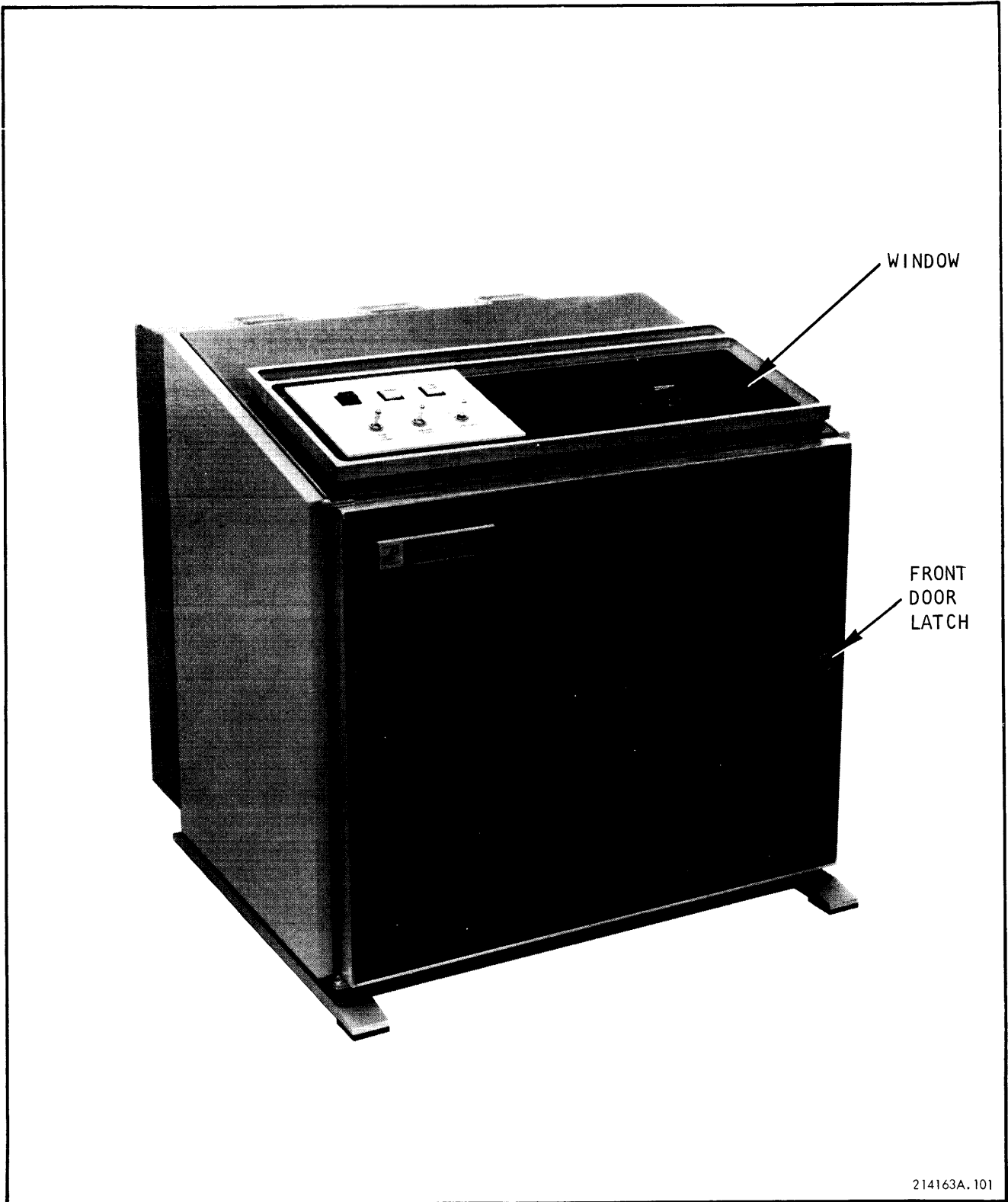


Figure 1-1. LINE/PRINTER Model 2310

Table 1-4. Physical Characteristics

Item	Specification
Dimensions	
Height	22.75 inches
Width	23.5 inches
Depth	22.0 inches
Weight	185 pounds

Table 1-5. Performance Characteristics

Item	Specification
Printable characters	
Number	64 (63 characters and space)
Type	ASCII open Gothic print
Size	Typically 0.095 inches high and 0.065 inches wide
Characters per line	80 (maximum)
Character drum	
Characters	64
Speed	1760 rpm
Print rate	
64-character drum	356 Lines per minute - 80 columns (4 zones) 460 Lines per minute - 60 columns (3 zones) 650 Lines per minute - 40 columns (2 zones) 1110 Lines per minute - 20 columns (1 zone)
Format	Top-of-form control, single line advance with perforation stepover, and carriage return

Table 1-5. Performance Characteristics (Continued)

Item	Specification
Paper slew speed	13 inches per second (minimum)
Print area	8 inches wide, left-justified
Character spacing (horizontal)	0.100 ( $\pm 0.005$ ) inch between centers
Line spacing (vertical)	0.167 ( $\pm 0.010$ ) inch (6 lines per inch); each character within $\pm 0.010$ inch from mean line through the character
Line advance time	20 milliseconds
Hidden lines	Line visible after 8 lines of print
Character synchronization	Variable reluctance pick-offs sense drum position
Signals	
Input	7 data lines 1 strobe line
Output	1 ready line 1 demand line 1 on-line line
Logic levels	
Logic 0	0 volt (unless otherwise specified)
Logic 1	+5 volts (unless otherwise specified)

1-7 PHYSICAL DESCRIPTION

1-8 The printer consists of four major assemblies (figures 1-3 and 1-4): mechanics A2, card cage A3, power supply A4, and control panel A5. The front and rear cabinet doors provide easy access to all printer assemblies.

## 1-9 MECHANICS A2

1-10 The mechanics A2 assembly contains drum gate A2A1, hammer bank A2A2, and paper feed A2A3 subassemblies. It also provides the printer with signals from interlock switches A2S1 (drum gate) and A2S2 (drum motor) (figure 1-5), cam switch A2S3 (top-of-form) (figure 1-5), and magnetic pickups A2A1PU1 (character), A2A1PU2 (index) (figure 1-6), A2A3PU1 (line strobe) (figure 1-7), and tachometer A2A3G1 (figure 1-4).

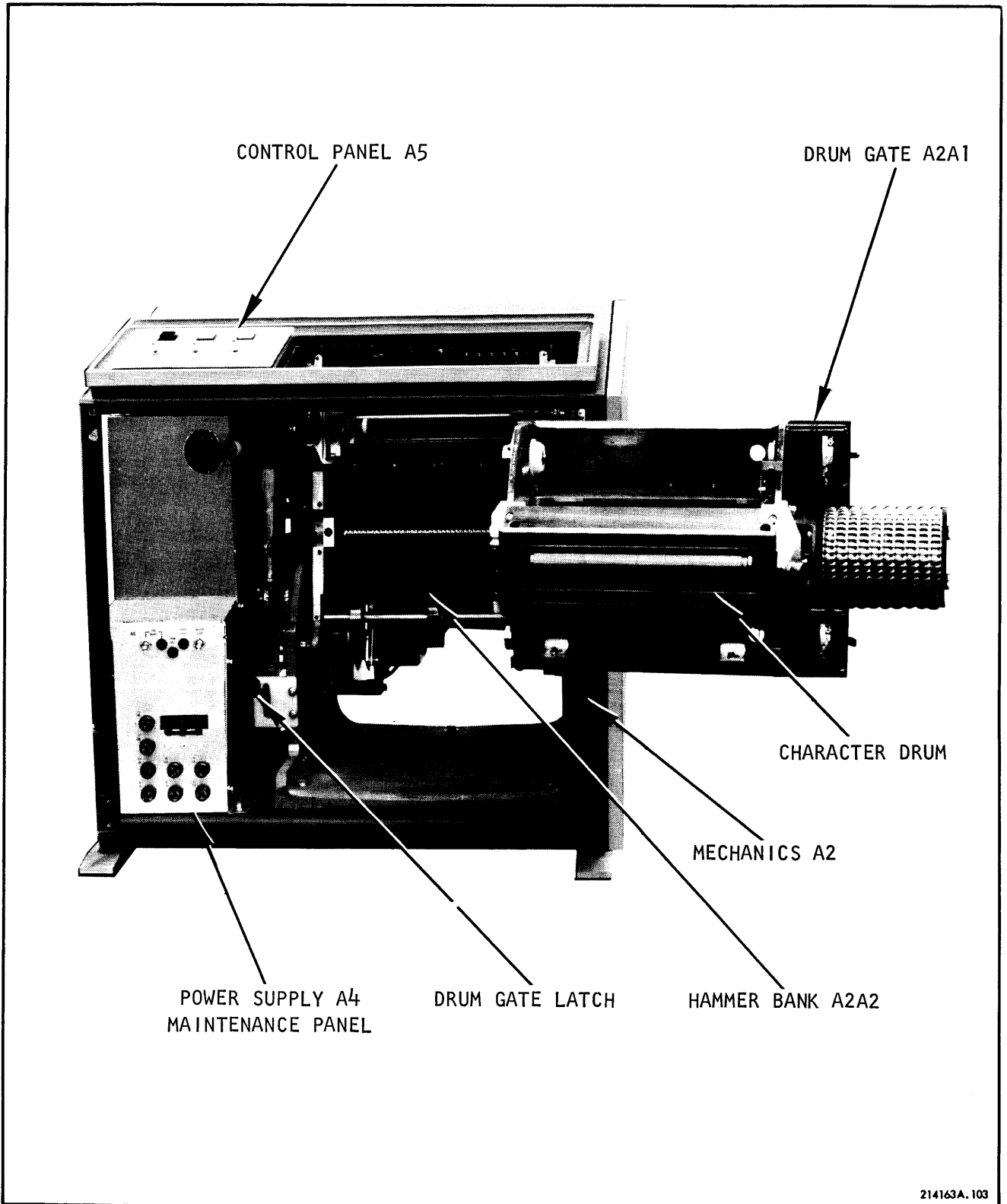


Figure 1-3. LINE/PRINTER, Front Door Open (Drum Gate Unlatched)

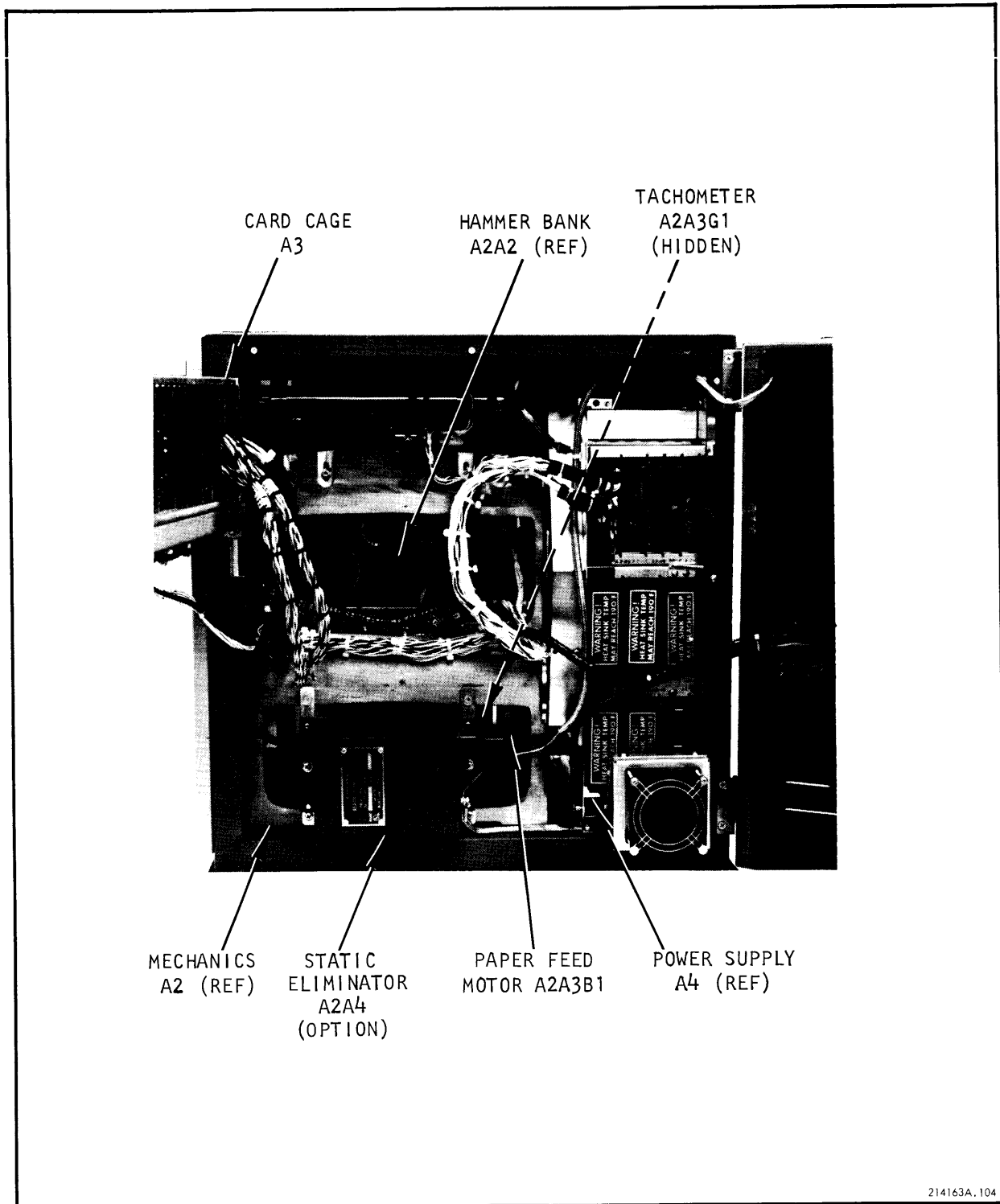


Figure 1-4. LINE/PRINTER, Rear Door Open (Card Cage Unlatched)



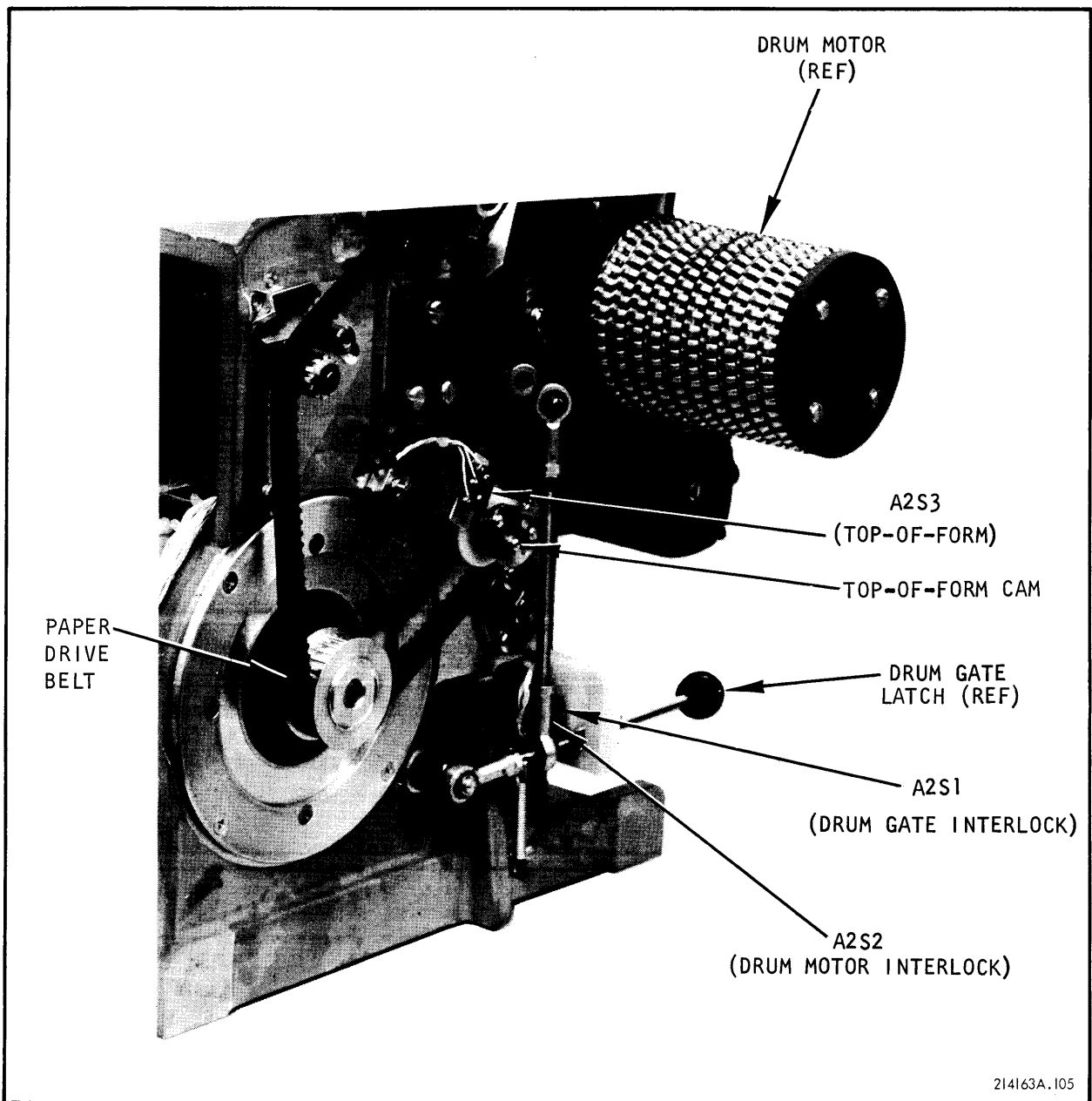


Figure 1-5. Drum Gate and Drum Motor Interlock, and Top-of-Form Cam Switch Locations (Mechanics A2 Assembly Removed)

1-11 Drum Gate A2A1 (Figure 1-8)

1-12 Drum gate A2A1 contains the print ribbon, ribbon motors and switches, drum motor and belt assembly, and ribbon guide and paper tension bar assembly. The drum gate swings out 180°, giving complete access to both the print ribbon and paper loading area.

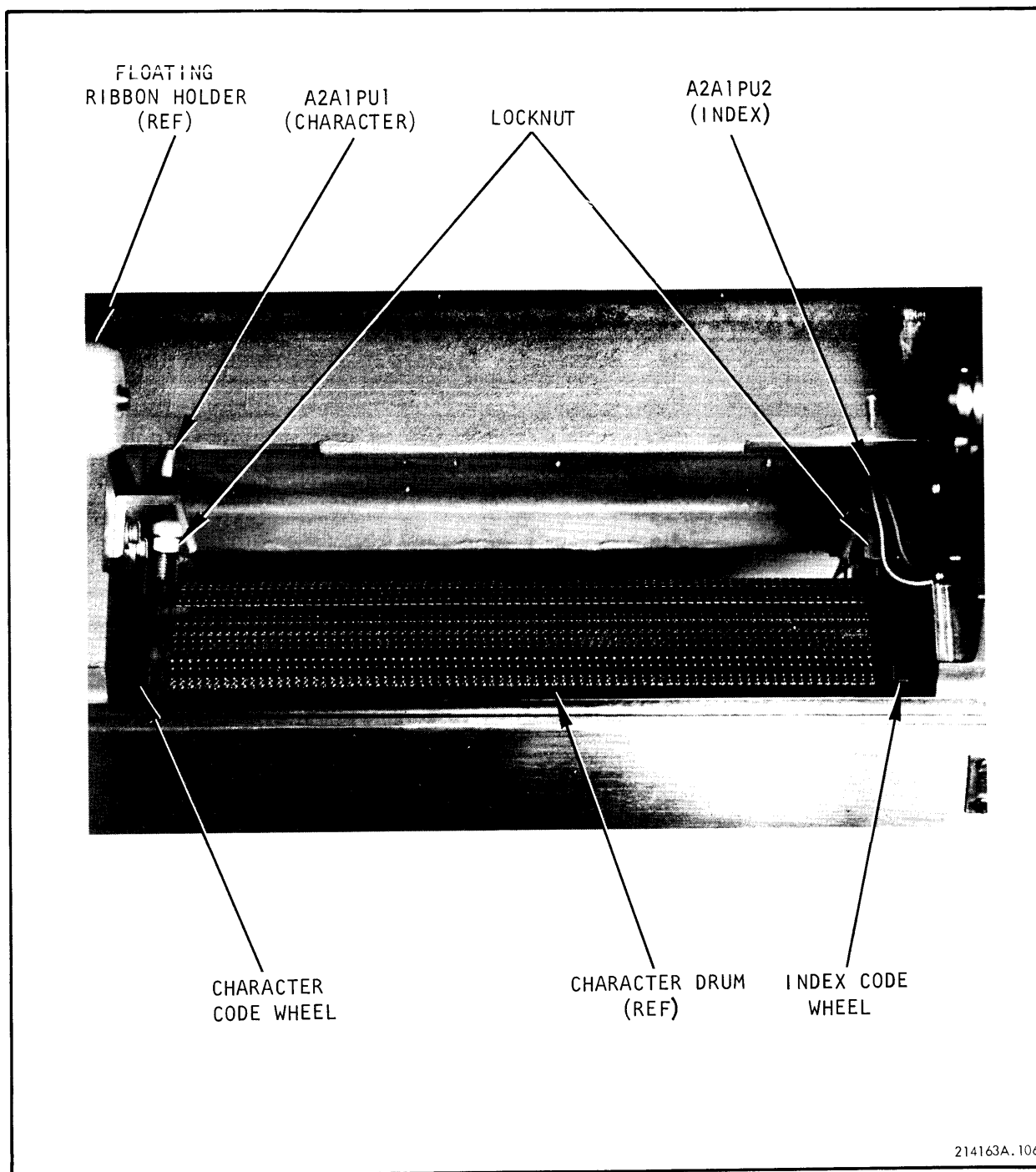


Figure 1-6. Character and Index Magnetic Pickup Locations

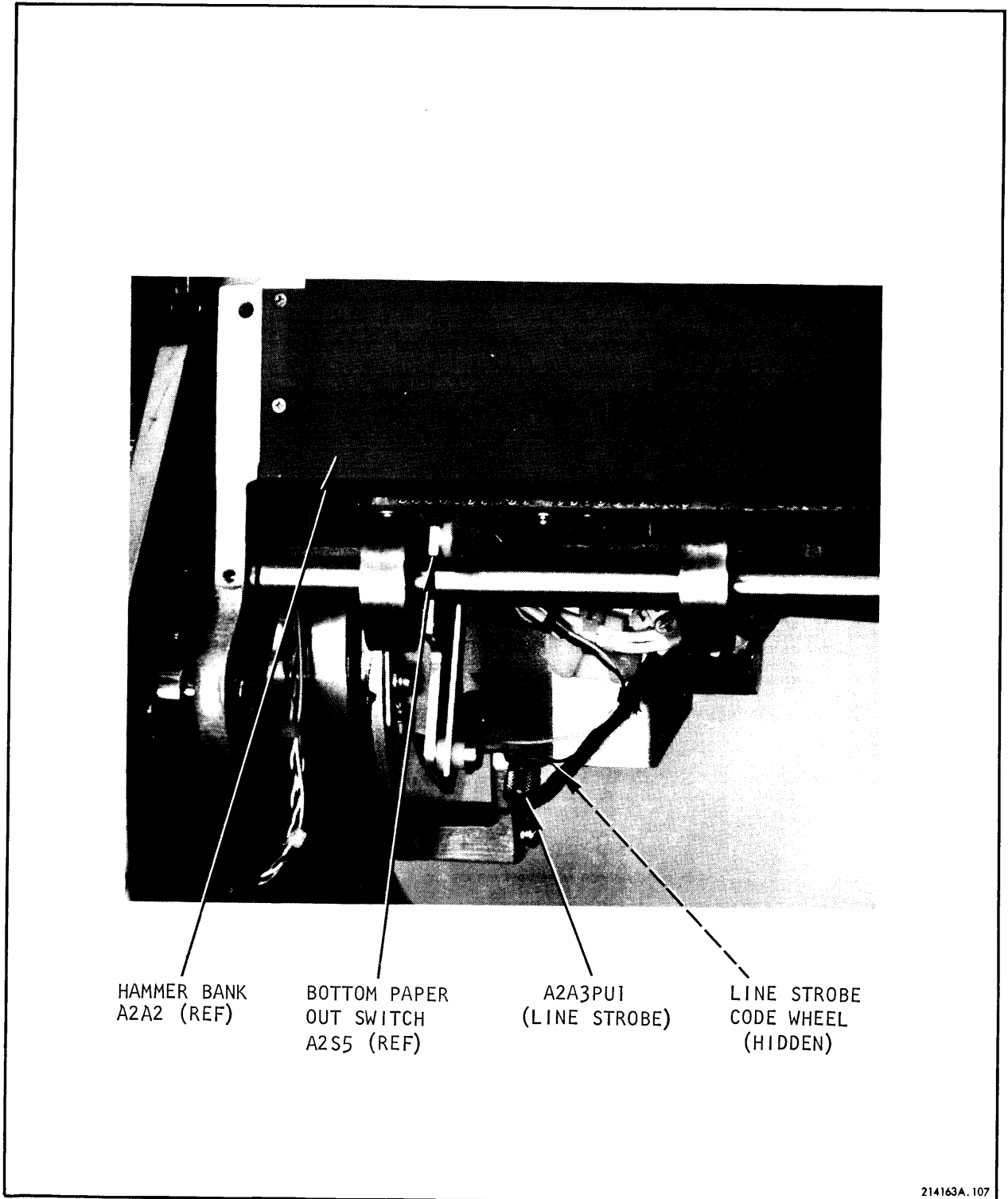


Figure 1-7. Line Strobe Magnetic Pickup Location

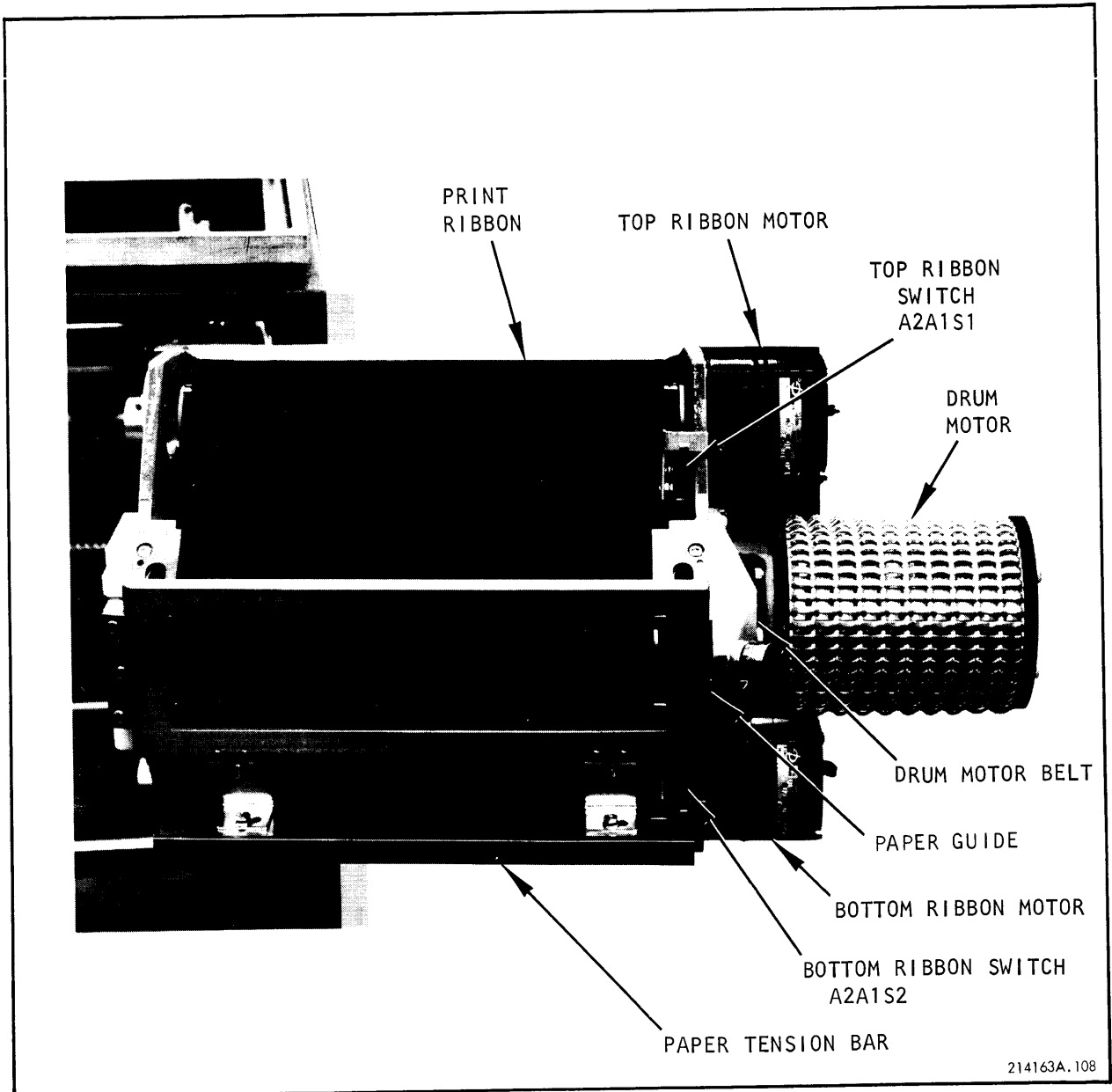


Figure 1-8. Drum Gate A2A1, Ribbon Installed

1-13 The print ribbon is mounted on the drum gate and travels vertically between the character drum (figure 1-3) and the paper. It is driven first in one direction and then the other by opposing motors. The end of ribbon travel is sensed by switches A2A1S1 and A2A1S2 which are actuated by ribbon-mounted bars. As the ribbon reaches the end of travel in one direction, it actuates the appropriate switch, power is transferred to the opposite motor, and the ribbon is driven back in the other direction. Ribbon travel is inhibited during periods when the printer is not in a print mode.

1-14 Hammer Bank A2A2

1-15 Hammer bank A2A2 contains 80 Mark IV impact hammer flags in an assembly consisting of an upper and lower bank containing 40 hammers each. The top bank contains the even-numbered hammers and the bottom bank the odd-numbered hammers.

1-16 The Mark IV hammer flag is a molded assembly containing a hammer tip and coil cantilevered from a mounting block with two leaf springs. The springs also act as current conductors to the coil. Two hammer flags are assembled into a module for hammer bank installation, and hammer bank A2A2 contains 40 hammer modules. Removal and replacement is simple as each hammer module is secured by a single mounting screw.

1-17 Paper Feed A2A3

1-18 Paper feed A2A3 contains paper feed motor A2A3B1 (figure 1-4), tachometer A2A3G1 (figure 1-4), and line strobe pickup A2A3PU1.

1-19 The paper drive belt (figure 1-5) couples the paper drive motor to a pin-feed tractor (figure 1-9) on each edge of the paper. The paper is loaded directly onto the tractors from the supplier box on the floor beneath the cabinet. The left tractor is factory-adjusted for proper horizontal positioning of standard fanfold paper, and the right tractor adjusts for various paper widths and provides an adjustment for proper horizontal paper tension. Vertical paper tension is provided by a spring-loaded friction device which is automatically positioned upon closing the drum gate. This simplifies loading and eliminates the need for vertical tension adjustment. The bottom edge of the front door is notched to permit the paper to feed with the door closed (figure 1-10).

1-20 Paper-out sensors A2S4 and A2S5 (figure 1-11) are located above and below hammer bank A2A2. The top sensor consists of a mercury switch mounted on a pendulum-type bracket, and the bottom sensor is a microswitch actuated by a pendulum-type bracket. Both brackets rest against the back of the printout paper as it travels past the hammer bank. An absence of paper at either sensor allows the bracket to swing forward, open the switch, and disable the printer. The upper switch actuates if the paper tears between the tractors and hammers, and the lower switch actuates when the paper supply is exhausted or there is a tear in the stored paper.

1-21 CARD CAGE A3

1-22 Card cage A3 swings out 90° from the rear of the printer and contains a standard complement of 17 printed circuit cards and 4 cable plug cards. See table 1-6 for the card cage standard complement.

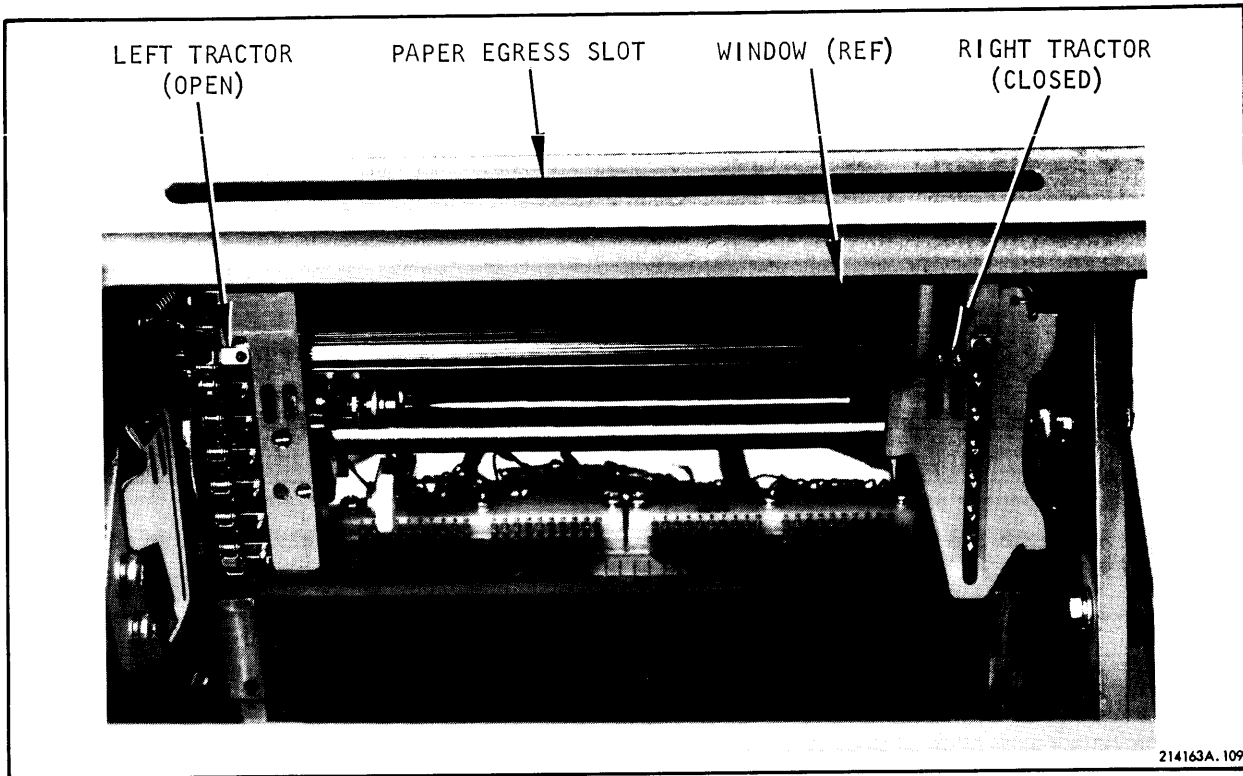


Figure 1-9. Paper Tractors and Egress Slot

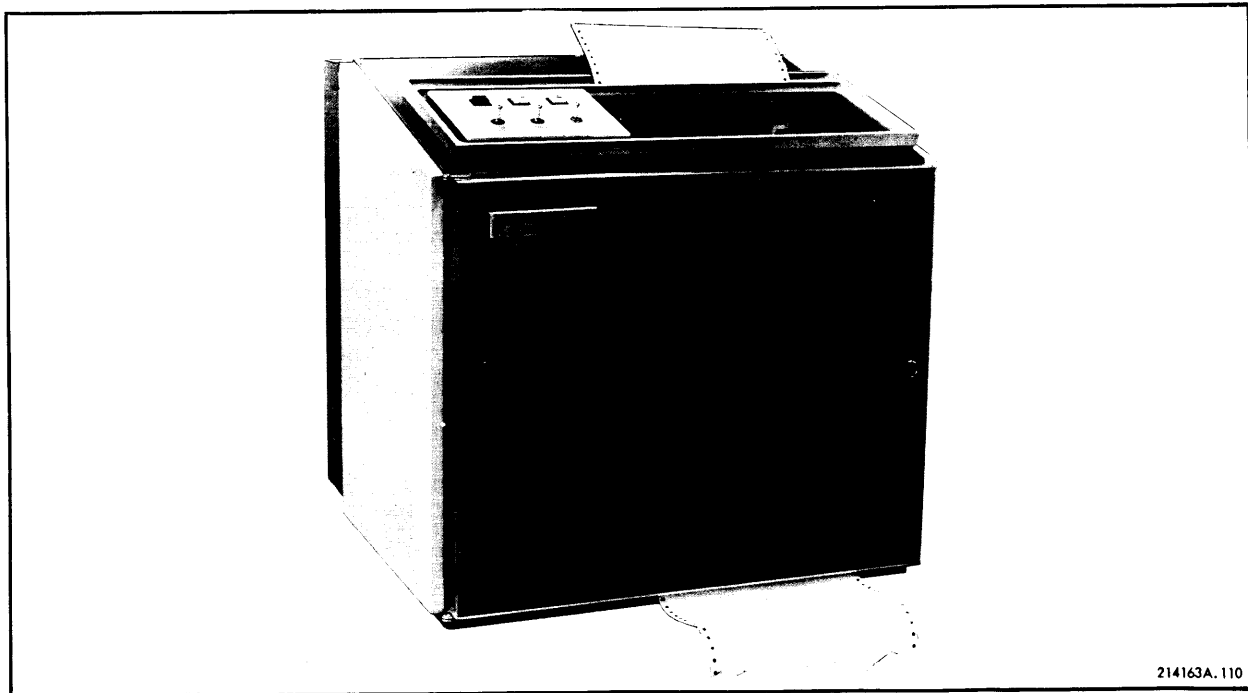


Figure 1-10. LINE/PRINTER, Paper Installed

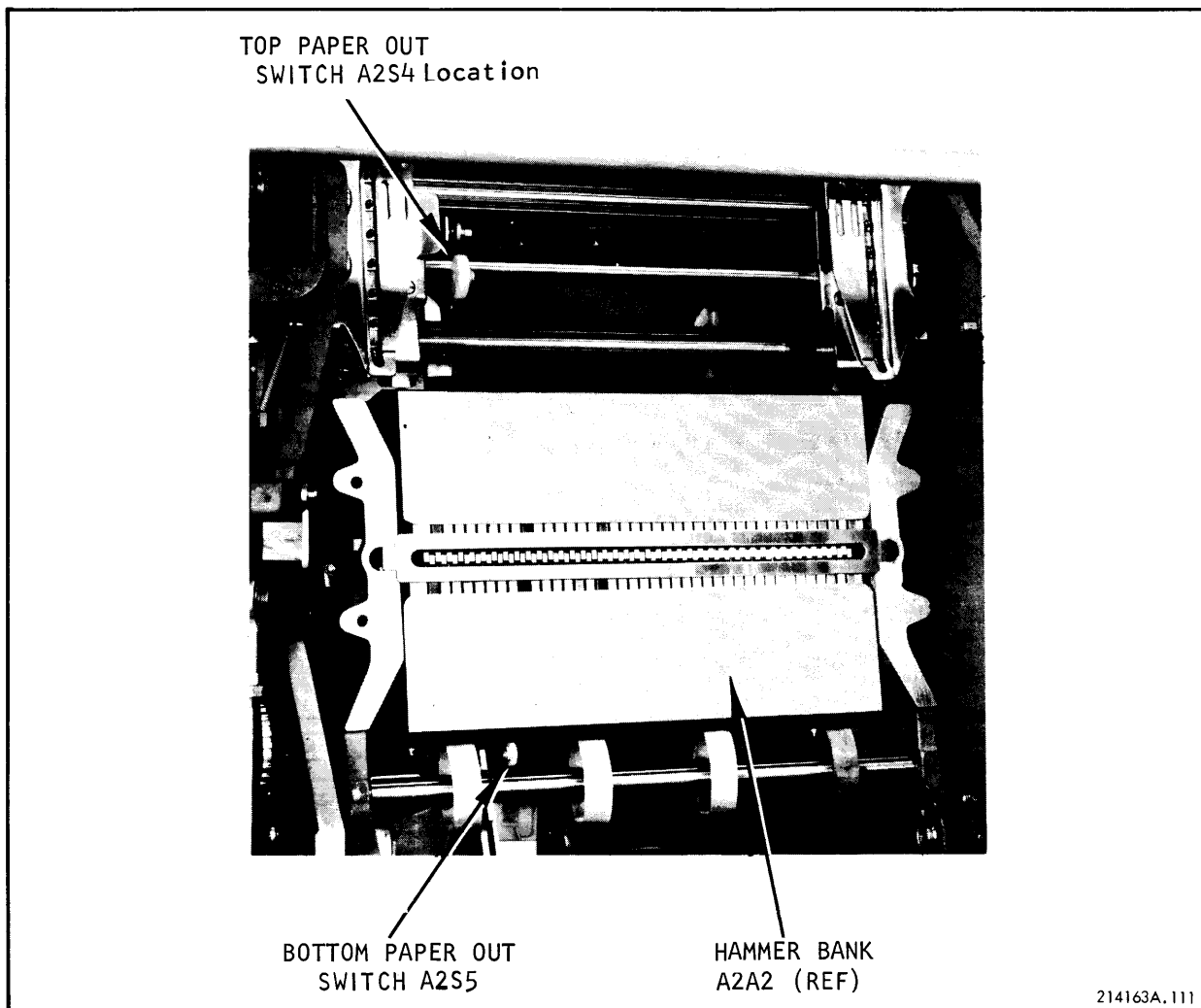


Figure 1-11. Paper Out Switch S4 and S5 Locations

Table 1-6. Card Cage A3 Standard Complement

Card Type	Description	Quantity	Reference Designator	Slot
AM-10 or AM-21	25-Character Memory (20 locations used) or 32-Character Memory (20 locations used)	1	A3A1	1
AG-17	Logic Gate I	1	A3A2	2
AG-18	Logic Gate II	1	A3A3	3
AG-45	Logic Gate III	1	A3A4	4
AG-20	Logic Gate IV	1	A3A5	5

Table 1-6. Card Cage A3 Standard Complement (Continued)

Card Type	Description	Quantity	Reference Designator	Slot
AT-13	Timing Control	1	A3A6	6
AG-32	Delay Controls and Gates	1	A3A9	9
AJ-11/AJ-14	Positive Driver	1	A3A11	11
AK-10	Receiver	1	A3A14	14
AS-13	Transducer Amplifier	1	A3A15	15
AZ-19	Hammer Interlock	1	A3A16	16
AZ-18	Zone Control	1	A3A17	17
AH-10	Hammer Driver	5	A3A18 thru A3A22	18 thru 22
AZ-14	Odd Hammers Cable Plug Card	1	A3P23	23
AZ-14	Even Hammers Cable Plug Card	1	A3P24	24
AZ-14	Input/Output Cable Plug Card	1	A3P25	25
AZ-14	Internal Interface Cable Plug Card	1	A3P26	26

## 1-23 POWER SUPPLY A4

1-24 Power supply A4 provides the printer with operating voltages of -12v, +5v, +22V, +12v, +28v, +65v, and 115 vac. The power supply card cage contains ten printed circuit cards and one cable plug card. Card connectors and test jacks are located on mother board, and input power circuit breaker, fuses, checkout switches, and fault indicators are located on the maintenance panel. See table 1-7 for the power supply card cage complement, and table 1-8 for fuse complement.

Table 1-7. Power Supply A4 Card Cage Complement


Card Type	Description	Quantity	Reference Designator	Slot
AZ-85	Cable Plug Card	1	A4P1	See figure 5-2
AP-10	Paper Feed Control	1	A4A1	
AV-10	Voltage Regulator	1	A4A2	
AZ-84	Ribbon Control	1	A4A3	
AZ-79	SCR Commutating	1	A4A4	
				See figure 5-2



Table 1-7. Power Supply A4 Card Cage Complement (Continued)

Card Type	Description	Quantity	Reference Designator	Slot
AZ-51	Reverse Paper Feed Power Amplifier	1	A4A5	See figure 5-2 ↑ ↓ See figure 5-2
AZ-49	Forward Paper Feed Power Amplifier	1	A4A6	
AZ-49	+12V Series Regulator Power Amplifier	1	A4A7	
AZ-49	+5V Series Regulator Power Amplifier	1	A4A8	
AZ-49	+28V Series Regulator Power Amplifier	1	A4A9	
AZ-78	Bridge	1	A4A10	

Table 1-8. Power Supply A4 Fuse Complement

Designation	Location	Protects	Rating	Quantity
F1	+5V	Logic	8A	1
F2	+22V	Paper Feed Drive	8A	1
F3	+28V	Memory and Hammer Interlock	2A	1
F4	115 VAC	Top Ribbon Motor	.5A	1
F5	115 VAC	Bottom Ribbon Motor	.5A	1
F6	115 VAC	Drum Motor	3A	1
F7	-12V	Logic	1A	1
F8	+65V	Hammers	.75A	1

## 1-25 CONTROL PANEL A5

1-26 Control panel A5 contains state indicators and a minimum of operator controls to simplify operation. The controls enable the operator to place the printer in ON LINE or OFF LINE mode, and control paper feed in the OFF LINE mode.

1-27 FUNCTIONAL DESCRIPTION

1-28 The printer receives data from the user system and stores up to 20 characters in the buffer memory. A print cycle is initiated and the stored data is scanned, compared, and then printed in lines of 80 columns or less. The printer generates timing, control, sync, hammer drive, paper feed servo, ribbon control, zone control, and interlock signals, during operation. A full line of data is printed in four zones, each zone having 20 consecutive print positions. In this

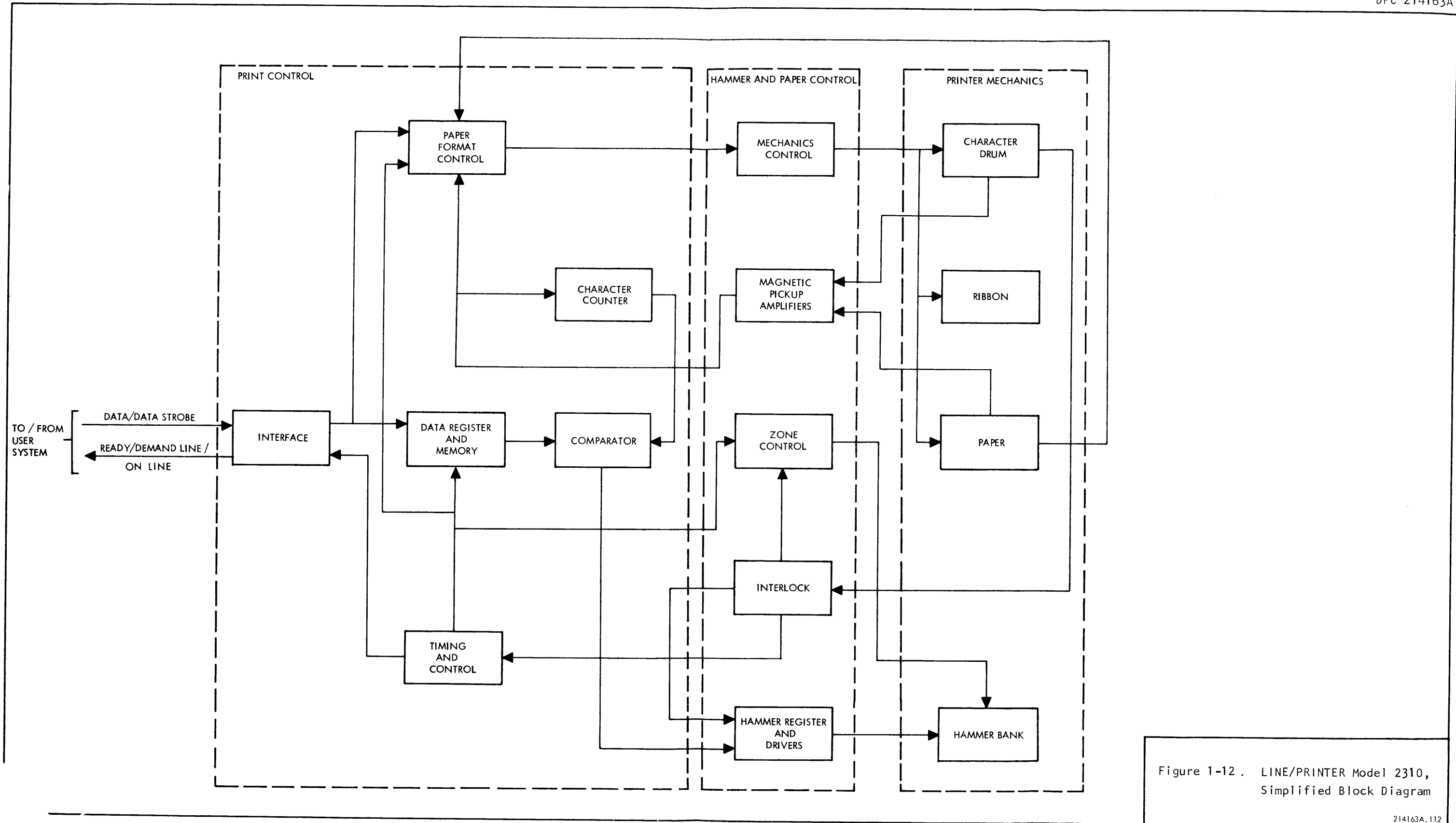


Figure 1-12 . LINE/PRINTER Model 2310, Simplified Block Diagram

manner, the printer's 20 hammer drivers can be time-shared among the 80 print positions. See figure 1-12 for a simplified block diagram of the printer.

1-29 PRINT CYCLE

1-30 During the print cycle the paper and inked ribbon pass between the 80 hammers and the continuously rotating character drum. The stored characters are scanned in synchronism with the rotating characters and the print control system actuates the appropriate hammer as the desired character approaches the print position.

1-31 Character Drum

1-32 The standard character drum contains 64 different characters consisting of 26 uppercase alphabets, 10 numerals, and 28 other symbols. See table 1-9 for the order in which the rows of characters appear on the drum.

1-33 Interlock

1-34 The interlock and fault detect circuits protect the printer in case certain conditions exist. The printer is inhibited from printing under the following conditions:

- a. Paper out or torn
- b. Drum gate open or improperly closed
- c. Paper feed motor overtemperature or overspeed
- d. VCL, +5V and +12V supplies fault

Note

With all interlocks satisfied, the printer is inhibited from printing if power supply switch PRINT INHIBIT is on.

When all interlocks are satisfied, a ready signal is transmitted to the user.

Table 1-9. Character Font and Sequence of Standard 64-Character Drum

Rows 1-16	Rows 17-32	Rows 33-48	Rows 49-64
Space (f)	Ø	@	P
!	1	A	Q
"	2	B	R
#	3	C	S
\$	4	D	T
%	5	E	U
&	6	F	V
'	7	G	W
(	8	H	X
)	9	I	Y
*	:	J	Z
+	;	K	[
,	<	L	◇
-	=	M	]
.	>	N	^
/	?	O	♥

SECTION II  
INSTALLATION

2-1 INTRODUCTION

2-2 This section contains space requirements, unpacking, and preliminary operation information for the printer.

2-3 SPACE REQUIREMENTS

2-4 Figure 2-1 shows the physical size and shape of the printer and the clearance required for opening the front and rear doors, drum gate A2A1, and card cage A3. In planning the installation, allow additional space for personnel involved with the maintenance and operation of the printer. The printer is provided with an 8-foot long primary power cable (figure 1-2) for connection to an ac power source as specified in table 1-1.

2-5 UNPACKING

2-6 Locate printer near power source and unpack as follows:

- a. Remove carton or plastic cover.
- b. Cut straps securing bubble pack to printer.
- c. Remove protective bubble pack surrounding the printer.
- d. Cut straps securing printer to pallet.



Support for printer should be capable of supporting a minimum of 300 pounds.

e. Lift printer carefully from pallet and place on table or support such as pedestal option (Section VII).

2-7 PRELIMINARY OPERATION

2-8 After unpacking printer and placing in operating position, proceed as follows:

- a. Open front door of cabinet and set circuit breaker CB1 (6, figure 3-2) on power supply A4 maintenance panel to OFF.

- b. Connect primary power cable plug A4P1 to the ac power source.
- c. Connect interface cable connector P1 (Winchester MRAC 50P-JTCH) to connector J1 (figure 1-2); see figure 6-4 for input connector signal list.
- d. Perform maintenance test portion of section V before proceeding further.

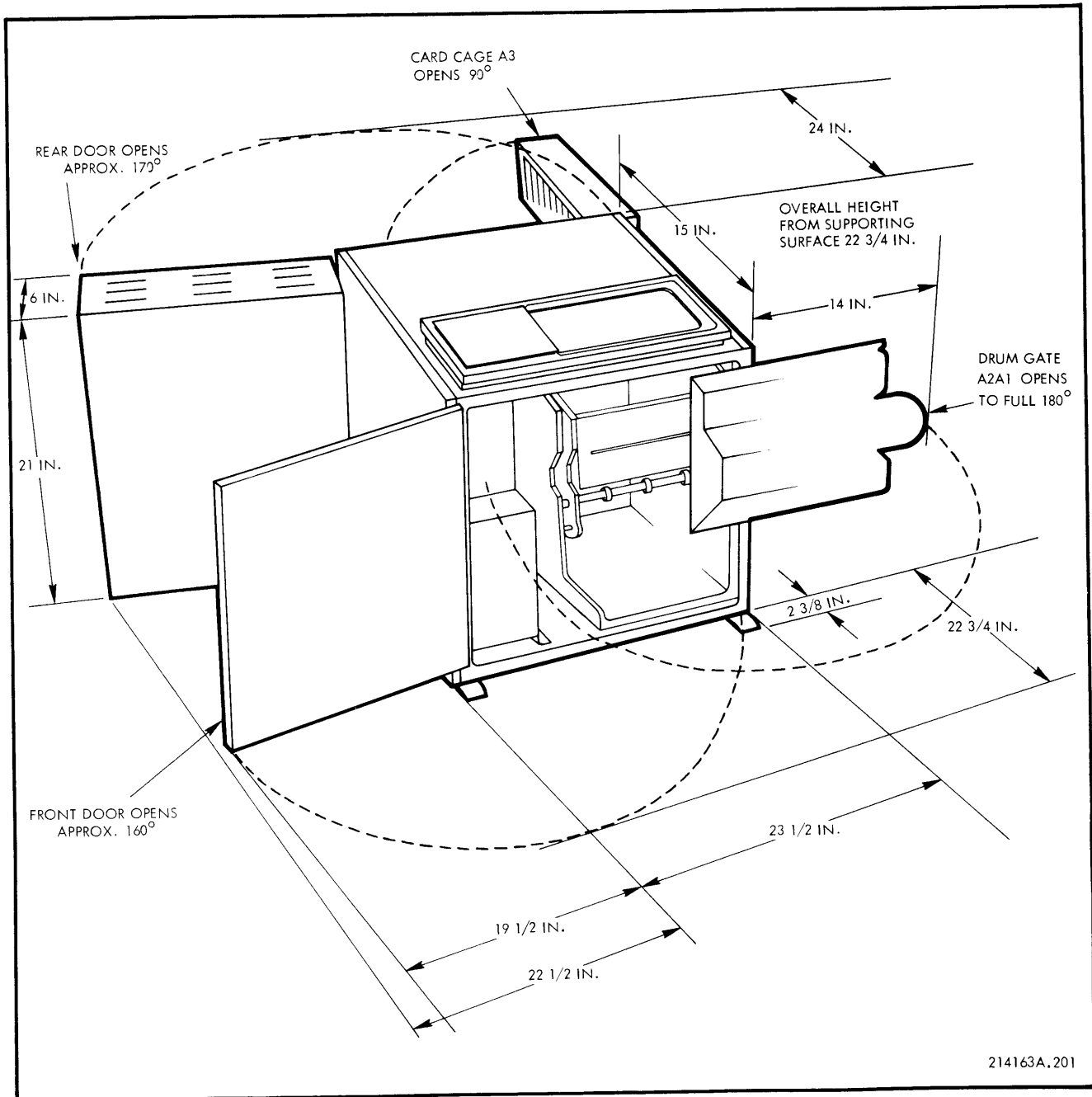


Figure 2-1. LINE/PRINTER Model 2310 Installation

SECTION III  
OPERATING INSTRUCTIONS

3-1 INTRODUCTION

3-2 This section contains operating instructions plus a description of operating controls and indicators. The operating instructions also include procedures for ribbon installation and paper loading.

3-3 OPERATING CONTROLS AND INDICATORS

3-4 CONTROL PANEL A5 CONTROLS AND INDICATORS

3-5 Control panel A5 controls and indicators are externally located on top of the printer cabinet. See figure 3-1 and table 3-1.

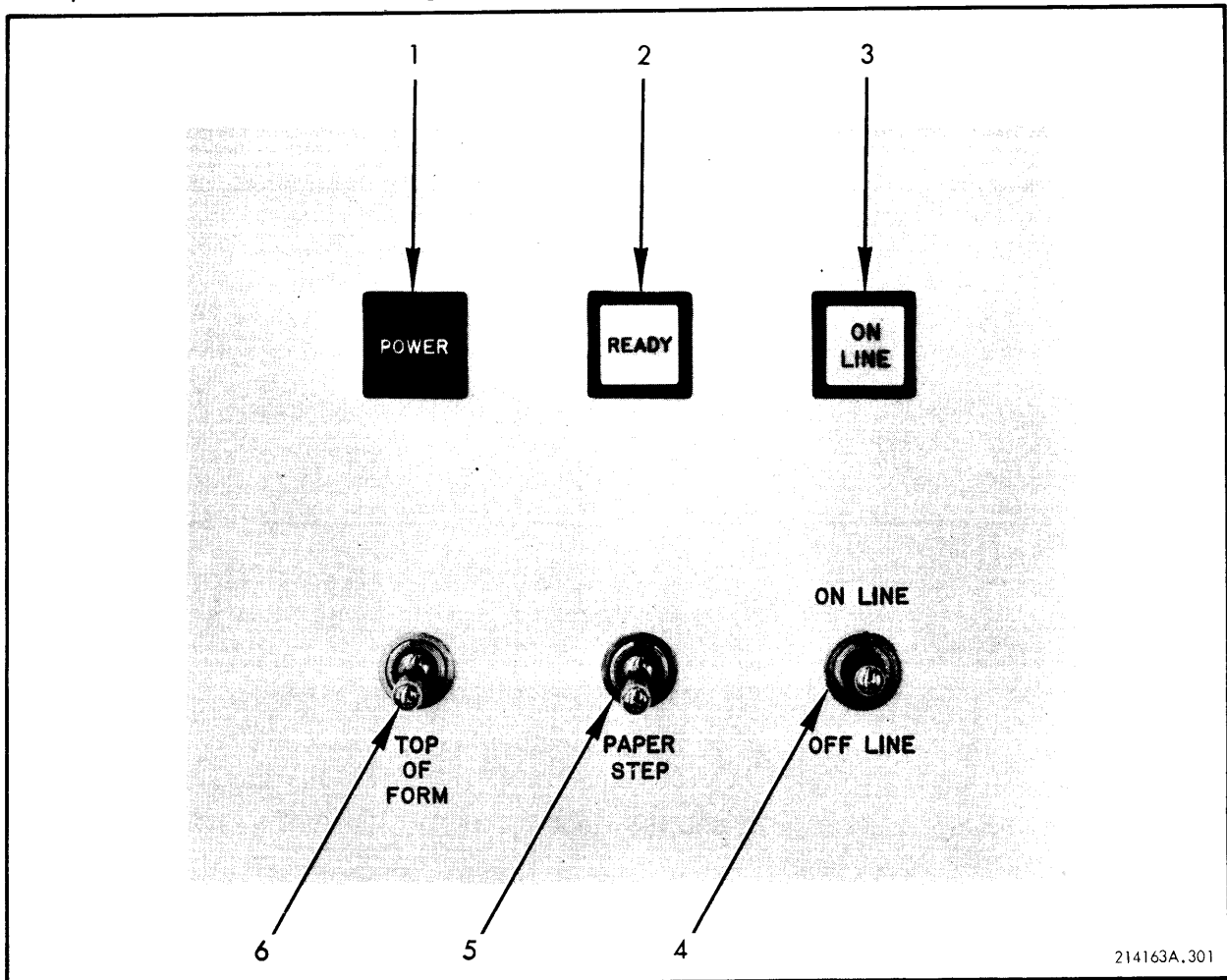


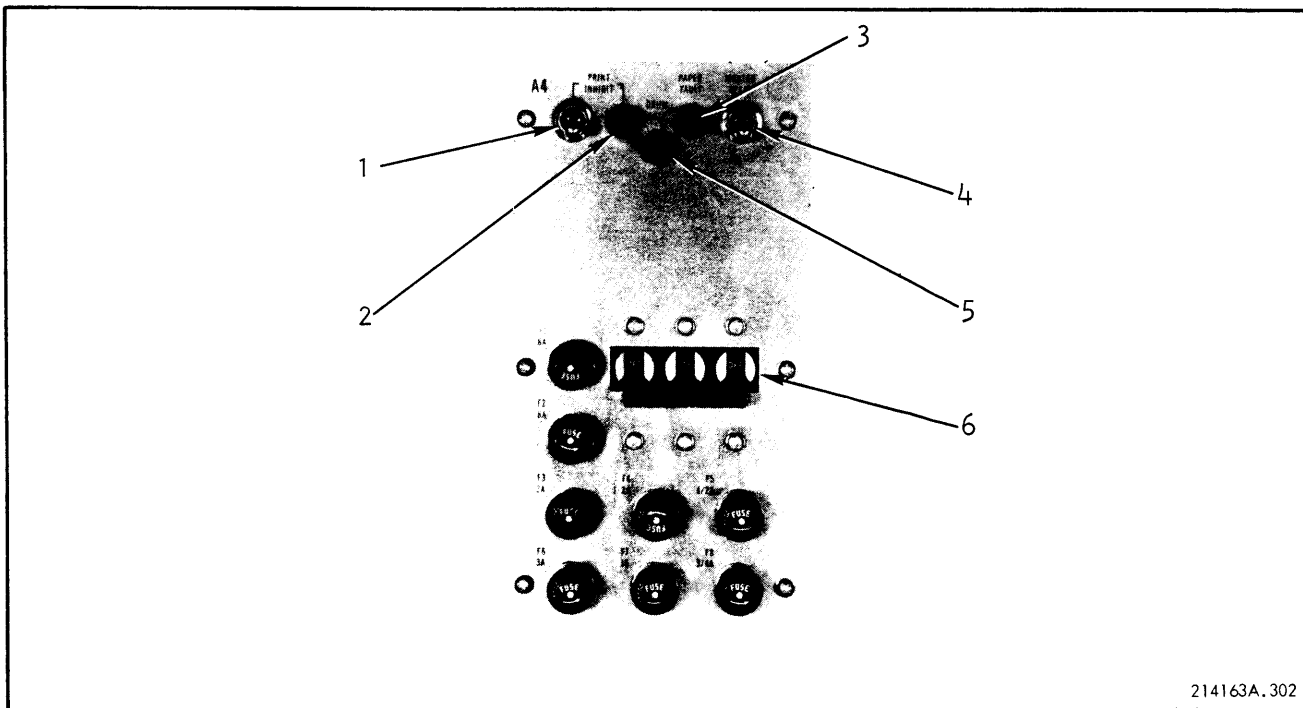
Figure 3-1. Control Panel A5, Controls and Indicators

Table 3-1. Control Panel A5 Controls and Indicators

Index No.	Control or Indicator	Function
1	POWER indicator	Lights when ac power is applied to printer
2	READY indicator	Lights when printer power is up, interlocks are satisfied, and PRINT INHIBIT switch is off
3	ON LINE indicator	Lights when printer is in ON LINE mode of operation and PRINT INHIBIT switch is off
4	ON LINE/OFF LINE switch	Selects mode of operation for printer
5	PAPER STEP switch	Advances paper one line; disabled in master clear and ON LINE modes
6	TOP OF FORM switch	Advances tractors to top-of-form position; disabled in ON LINE mode

3-6 POWER SUPPLY A4 MAINTENANCE PANEL CONTROLS AND INDICATORS

3-7 Power supply A4 maintenance panel is located on the forward face of the power supply chassis and is readily accessible upon opening the front door of the printer cabinet. See figure 3-2 and table 3-2.



214163A.302

Figure 3-2. Power Supply A4 Maintenance Panel, Controls and Indicators

Table 3-2. Power Supply A4 Maintenance Panel Controls and Indicators

Index No.	Control or Indicator	Function
1	PRINT INHIBIT switch	Inhibits hammer drivers during maintenance
2	PRINT INHIBIT indicator	Lights when PRINT INHIBIT switch is in on position
3	PAPER FAULT indicator	Lights when paper is torn or missing
4	MASTER CLEAR switch	Initializes the printer to ensure that logic elements are in proper state
5	DRUM GATE indicator	Lights when drum gate is unlatched
6	Ac power circuit breaker	Applies ac power to power supply

3-8 MECHANICS A2 CONTROLS AND ADJUSTMENTS

3-9 Mechanics A2 controls and adjustments are readily accessible upon opening the front door of the printer cabinet. See figures 3-3 and 3-4, and table 3-3.

3-10 OPERATING PROCEDURES

3-11 Operation of the printer consists of performing preliminary procedures, on-line startup procedure, and shutdown procedure.

3-12 PRELIMINARY PROCEDURES

3-13 Ribbon Installation

3-14 Install ribbon as follows:

NOTE

Use plastic gloves supplied with ribbon when installing or replacing ribbon.

- a. Open cabinet front door and set circuit breaker (6, figure 3-2) to OFF.
- b. Move drum gate latch (figure 3-3) to the left and up.
- c. Swing drum gate A2A1 fully open.

CAUTION

Wait for line printer drum to stop rotating before proceeding to the next step.

- d. Grasp corner of paper guide (figure 3-5) and swing open.
- e. Hold ribbon cores together and remove ribbon from box.
- f. Place fully wound ribbon core over top floating ribbon holder (figure 3-5).



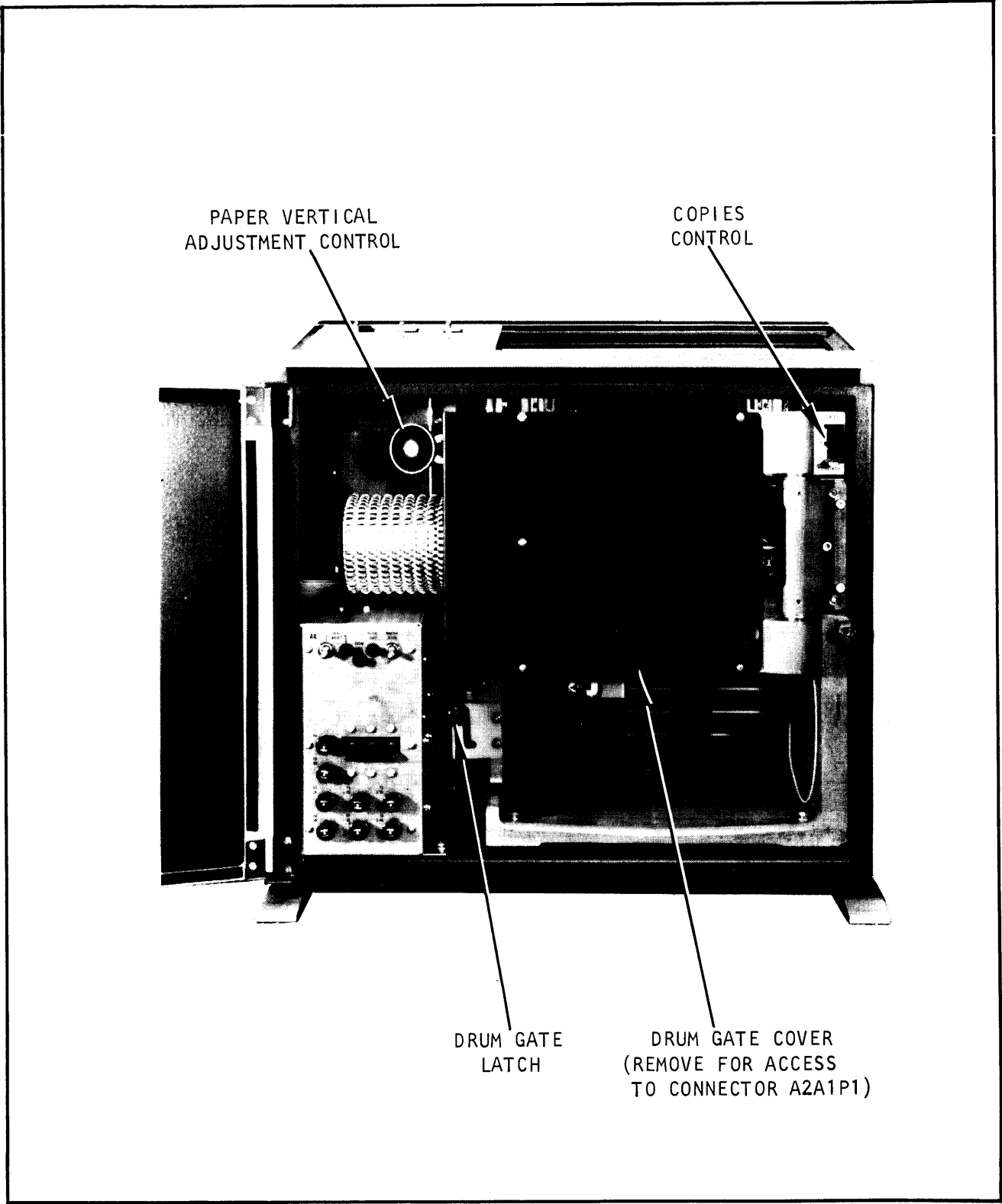
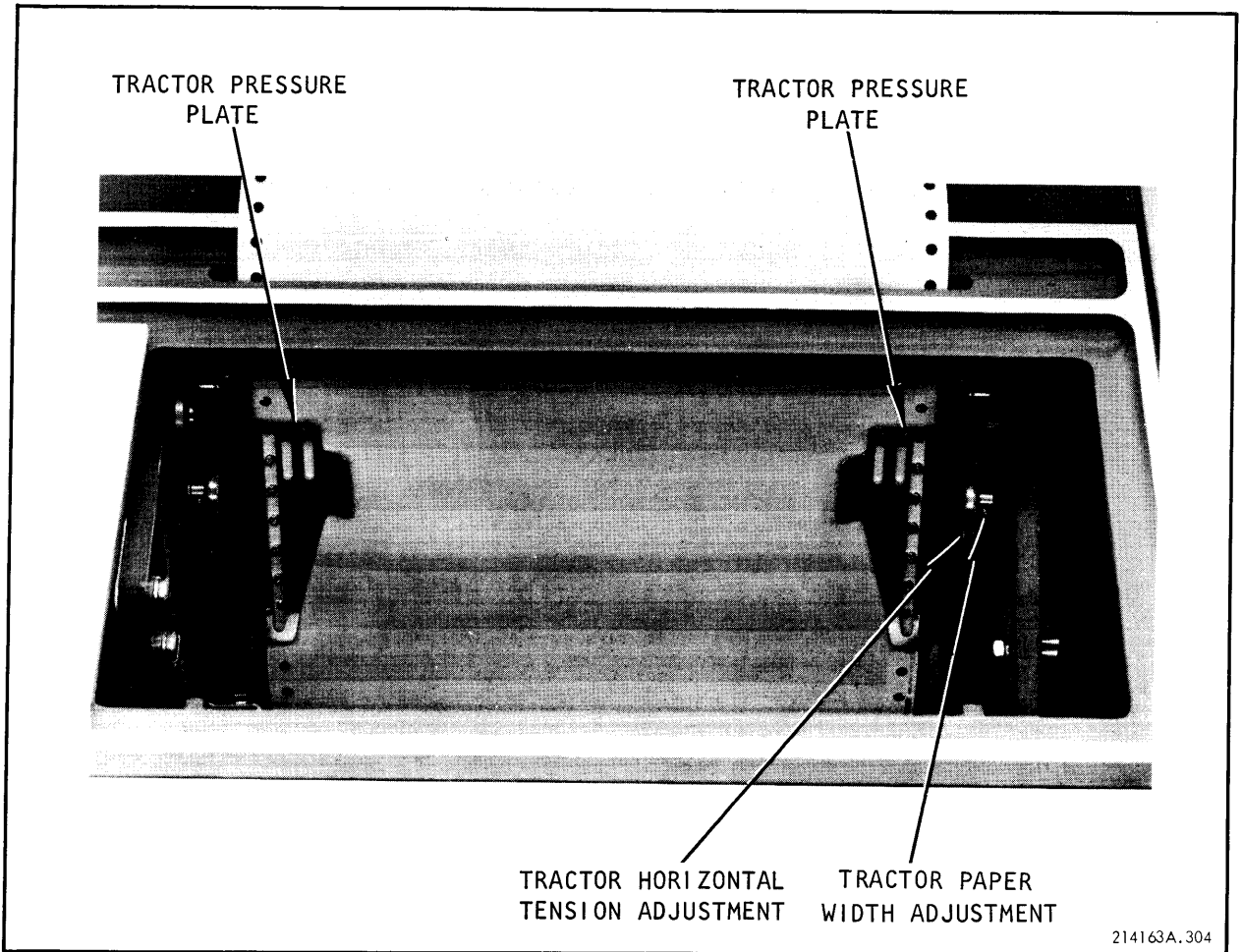


Figure 3-3. Mechanics A2 Controls



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Figure 3-4. Mechanics A2 Adjustments

Table 3-3. Mechanics A2 Controls and Adjustments

Control	Function
Paper vertical adjustment control	Adjusts vertical alignment of printing form to plus or minus one line; can be adjusted during printing if desired
COPIES CONTROL lever	Adjusts the distance between hammer bank and character drum for different numbers of print copy
Tractor paper width adjustment	Adjusts right tractor for various paper widths; left tractor is factory adjusted
Tractor horizontal tension adjustment	Adjusts horizontal tension of paper

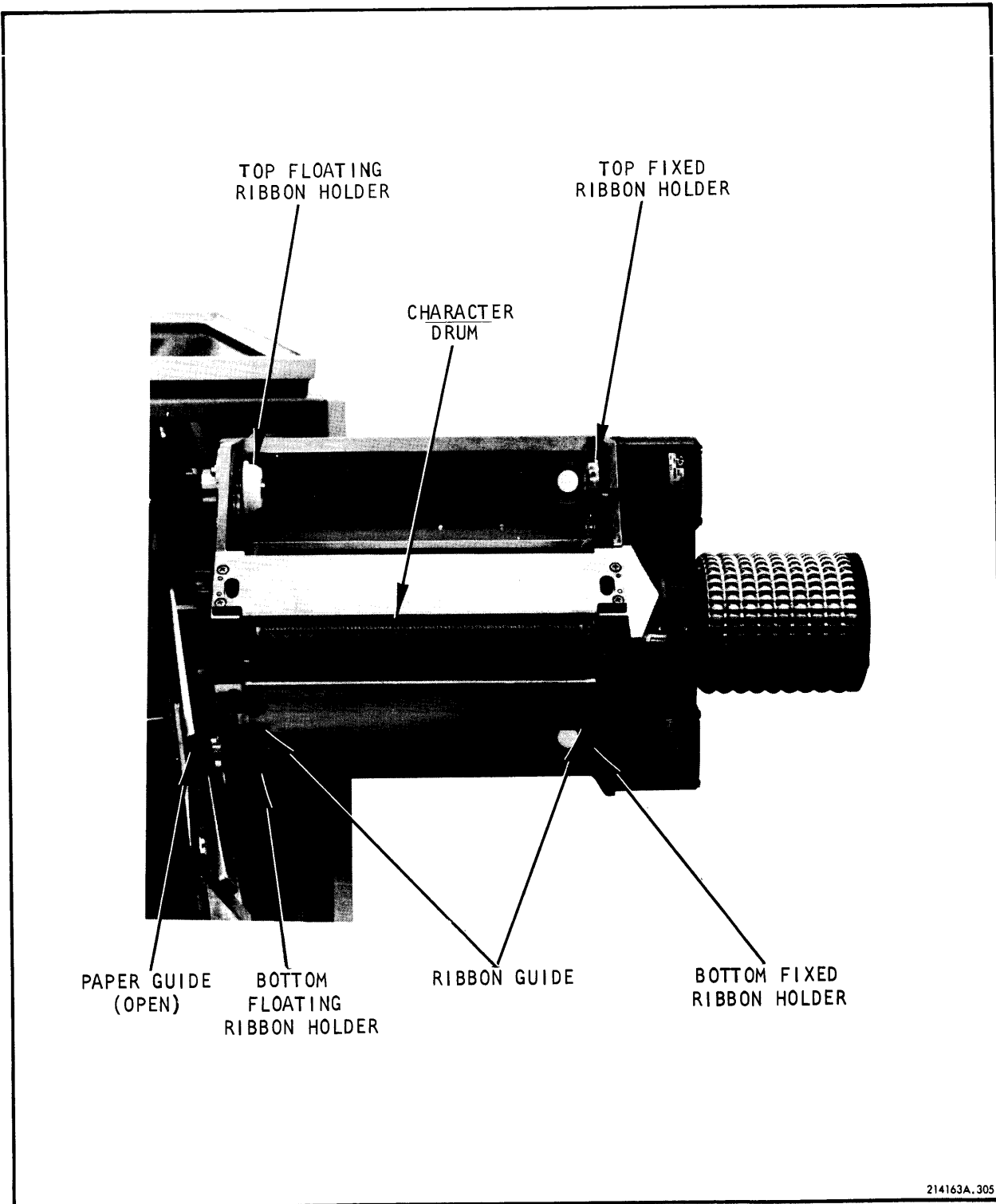


Figure 3-5. Drum Gate A2A1 Ribbon Installation

g. Push against floating holder spring and place opposite core end over top fixed ribbon holder (figure 3-5); ensure holder guide pin slips into slot on core end (figure 3-6).

h. Unwind second ribbon core and bring ribbon down and over character drum (figure 3-5). Place ribbon under ribbon guides (figure 3-5); ensure it tracks properly.

i. Place core on bottom ribbon holders (figure 3-5) as in step g for top holders.

j. Close paper guide.

Note

See figure 1-8 for view of drum gate A2A1 with ribbon installed.

k. Close drum gate A2A1; move drum gate latch down and to the right.

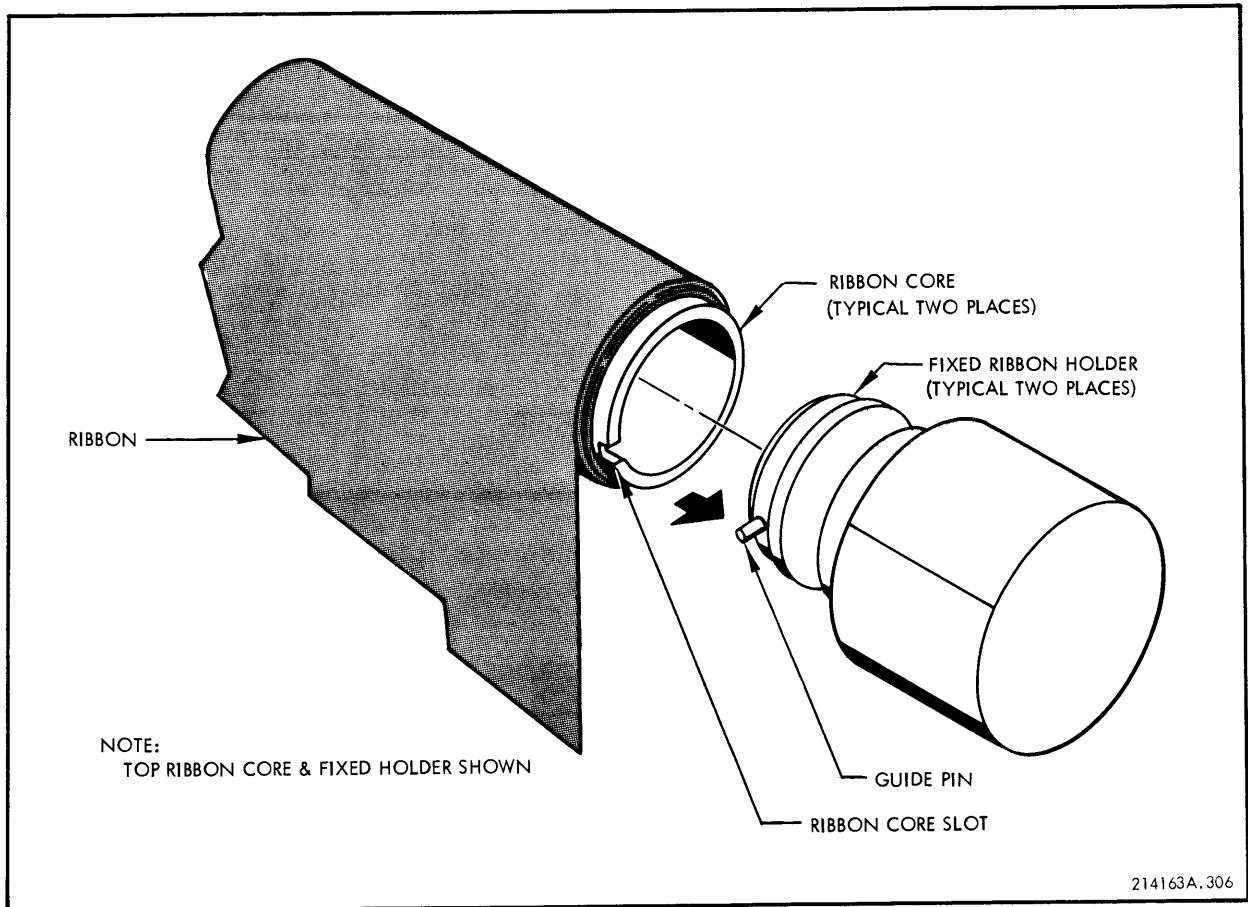


Figure 3-6. Installation of Ribbon Core on Fixed Ribbon Holder

3-15 Paper Loading

3-16 When paper is properly loaded, the top-of-form cam allows the printer to print all lines on the 11-inch page, except one line preceding and two lines following each perforation. A subsequent form-feed signal to the printer automatically advances the paper so that the next line occurs two lines past the perforation on the next sheet. Load the paper as follows:

- a. Open printer cabinet front door and set circuit breaker (6, figure 3-2) to OFF.
- b. Connect primary power cable to ac source specified in table 1-1.
- c. Connect input cable from data source to connector J1 (figure 1-2).
- d. Set circuit breaker to ON; ensure POWER indicator (1, figure 3-1) and PAPER FAULT indicator (2, figure 3-2) light.
- e. Unlatch and open drum gate A2A1; ensure DRUM GATE indicator (1, figure 3-2) lights.

CAUTION

Wait for line printer drum to stop rotating before proceeding to the next step.

- f. Set TOP OF FORM switch (figure 3-1) to up position and release.
- g. Set COPIES CONTROL lever (figure 3-3) to number of copies desired.
- h. Open the spring-loaded pressure plates on both tractors (figure 3-4).
- i. Place paper on tractor pins (figure 3-4); perform step j if adjustment of right tractor for paper width is required.
- j. Loosen paper width adjustment setscrew (figure 3-4); set right tractor to correct paper width; tighten setscrew.
- k. Align paper perforation to top-of-form indicators on hammer bank (figure 3-7).
- l. Close the pressure plates on both tractors (figure 3-4).
- m. Use the horizontal tension adjustment (figure 3-4) for proper paper tension.
- n. Close and latch drum gate A2A1; ensure PAPER FAULT and DRUM GATE indicators go off.

3-17 Paper Positioning (Vertical)

3-18 When lined paper is used, the characters being printed can be set to appear directly on the print line by adjusting the paper vertical adjustment control (figure 3-3).

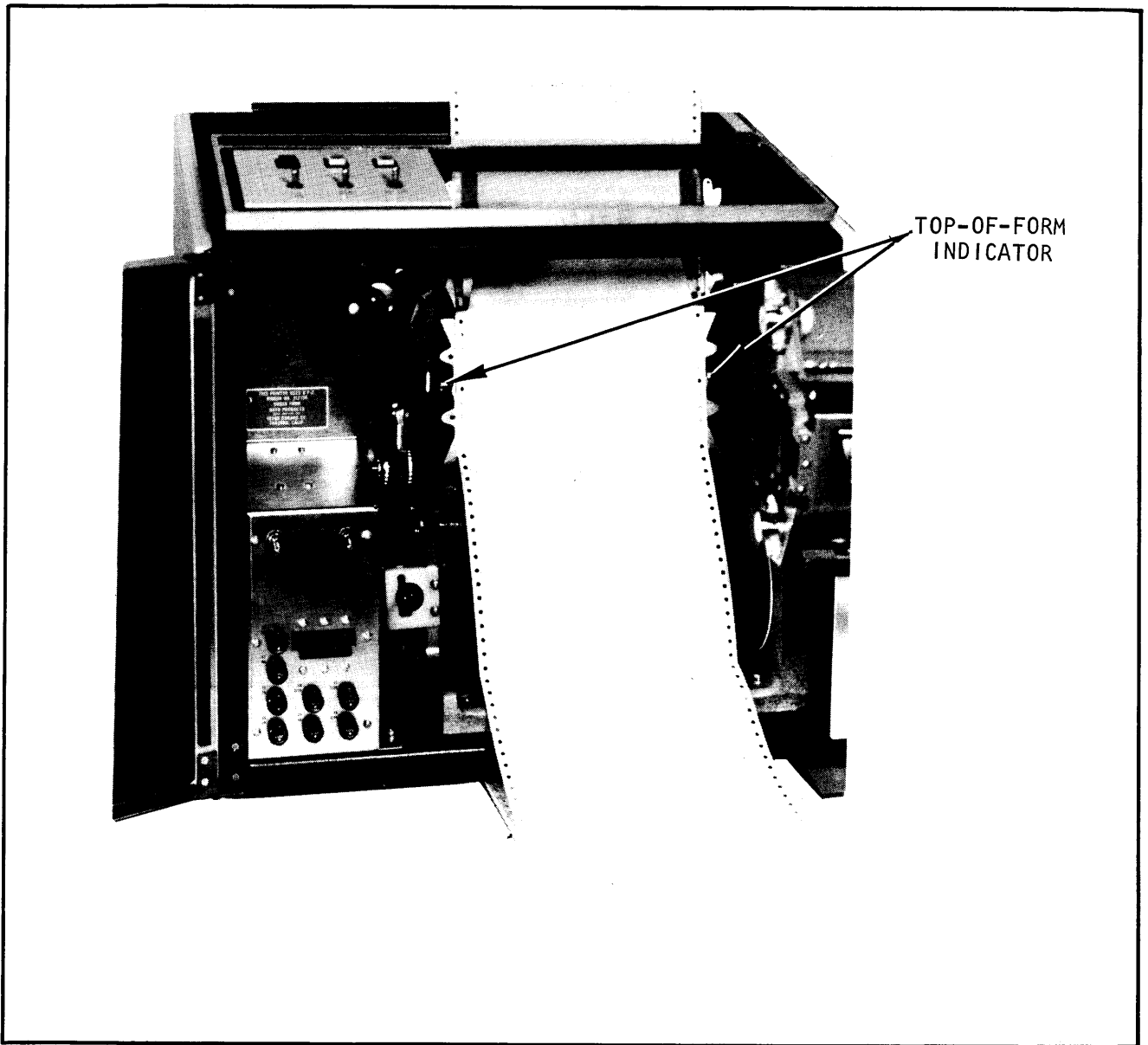


Figure 3-7. Paper Alignment to Top-of-Form Indicators

3-19 ON-LINE STARTUP PROCEDURE

3-20 Place printer in on-line operation as follows:

- a. Wait for READY indicator (2, figure 3-1) to light (approximately 10 seconds after drum gate is closed).
- b. Ensure PRINT INHIBIT switch (4, figure 3-2) is down, and PRINT INHIBIT indicator (3, figure 3-2) is off.

c. Set ON LINE/OFF LINE switch (4, figure 3-1) to ON LINE position and release; ensure ON LINE indicator (3, figure 3-1) lights.

d. Observe printer operation; make paper adjustments if necessary.

3-21 SHUTDOWN PROCEDURE

3-22 Shut down printer as follows:

a. Set ON LINE/OFF LINE switch to OFF LINE and release.

b. Set circuit breaker to OFF.

SECTION IV  
PRINCIPLES OF OPERATION

4-1     INTRODUCTION

4-2     This section describes the interface, print control logic, and hammer and paper control logic of the printer. A general description of the printer operation is given first, followed by a detailed description of the major functional areas, and the operating states.

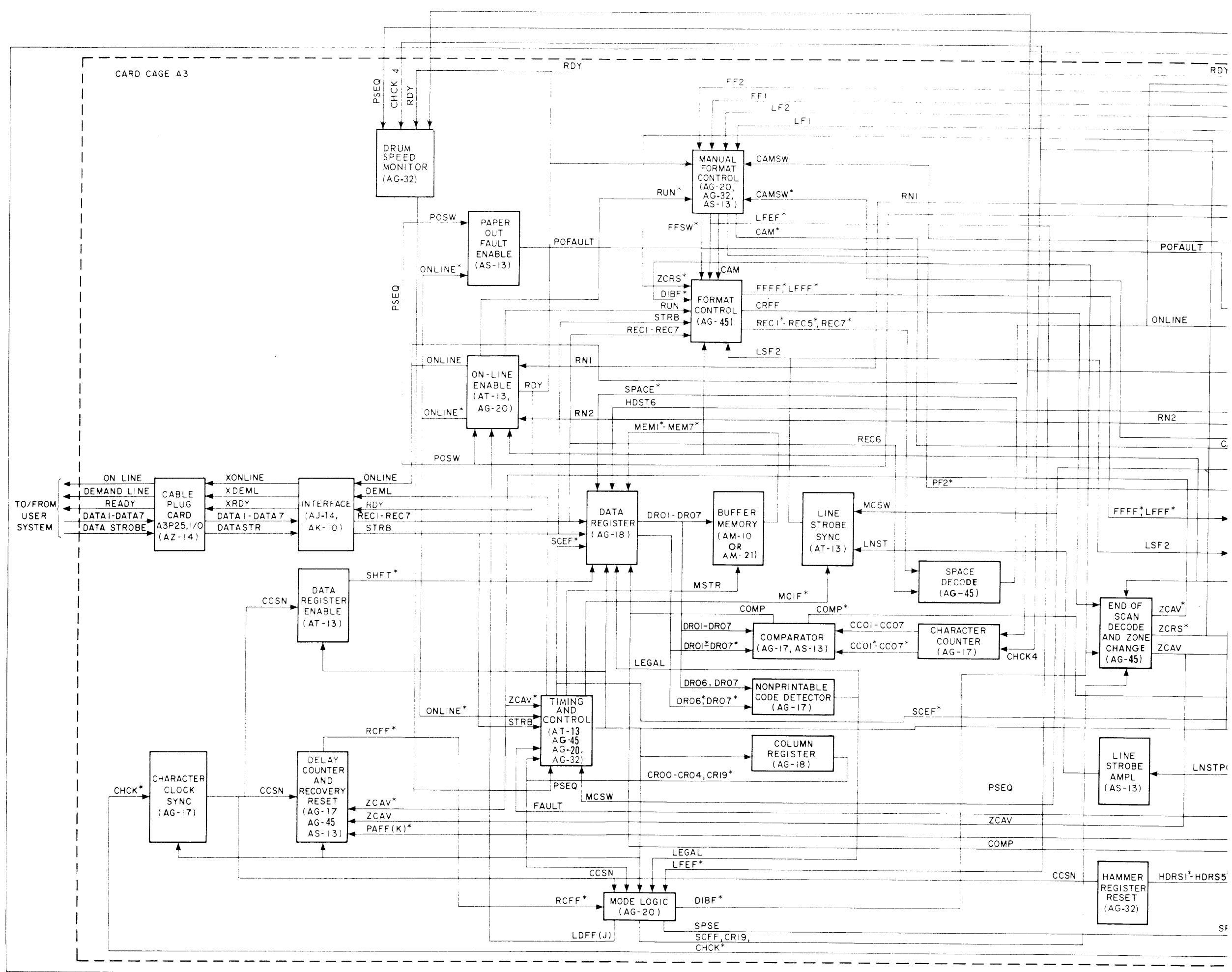
4-3     GENERAL DESCRIPTION (See figure 4-1)

4-4     The printer is an impact printer with 80 print positions, and a 64-character rotating drum. Each print position has an associated print hammer which is activated by a flip-flop-controlled hammer driver during the print cycle. The 80 print positions are divided into four zones, each having 20 consecutive print positions. The 20 hammer drivers of the printer are then time-shared by the four zones.

4-5     When the printer is initialized, the print paper positioned, and all interlocks satisfied, the 20 hammer drivers are switched to their respective hammers in zone 1, and the printer is ready to operate ON LINE in a demand/response sequence. When initialized, all printer registers are reset and signal DEMAND LINE is enabled. On receipt of DEMAND LINE, the user system transmits coded information over data lines DATA1 through DATA7. The coded data contains the characters to be printed as well as paper format control characters. The characters are sent serially and each is followed by signal DATA STROBE. On receipt of DATA STROBE, the printer samples the data lines and disables DEMAND LINE. If the character is not a format control, it is transferred from the data register to memory. Storing a character in memory increments the column register by 1 and enables DEMAND LINE. Up to 20 characters can be received and stored in this manner, and the print cycle is started on receipt of either the 20th character or a format control character. Signal DEMAND LINE remains disabled during the print cycle.

4-6     On entering the print cycle, the characters in memory are checked for nonprintable characters and scanned and compared against the output of the character counter. Nonprintable characters are immediately erased from memory. The character counter output corresponds to the character currently adjacent to the print station. Signal CIND, generated by magnetic pickup A2A1PU2, which monitors an index code wheel on the drum, initializes the counter once each drum revolution. Signals CHCK4 and CCSN are generated by magnetic pickup A2A1PU1 which monitors a character code wheel on the drum. CHCK4 clocks the counter, and CCSN initiates the scan period. Each character is scanned, and if a comparison occurs, signal COMP sets the hammer register flip-flop for that print position and erases the character from memory.







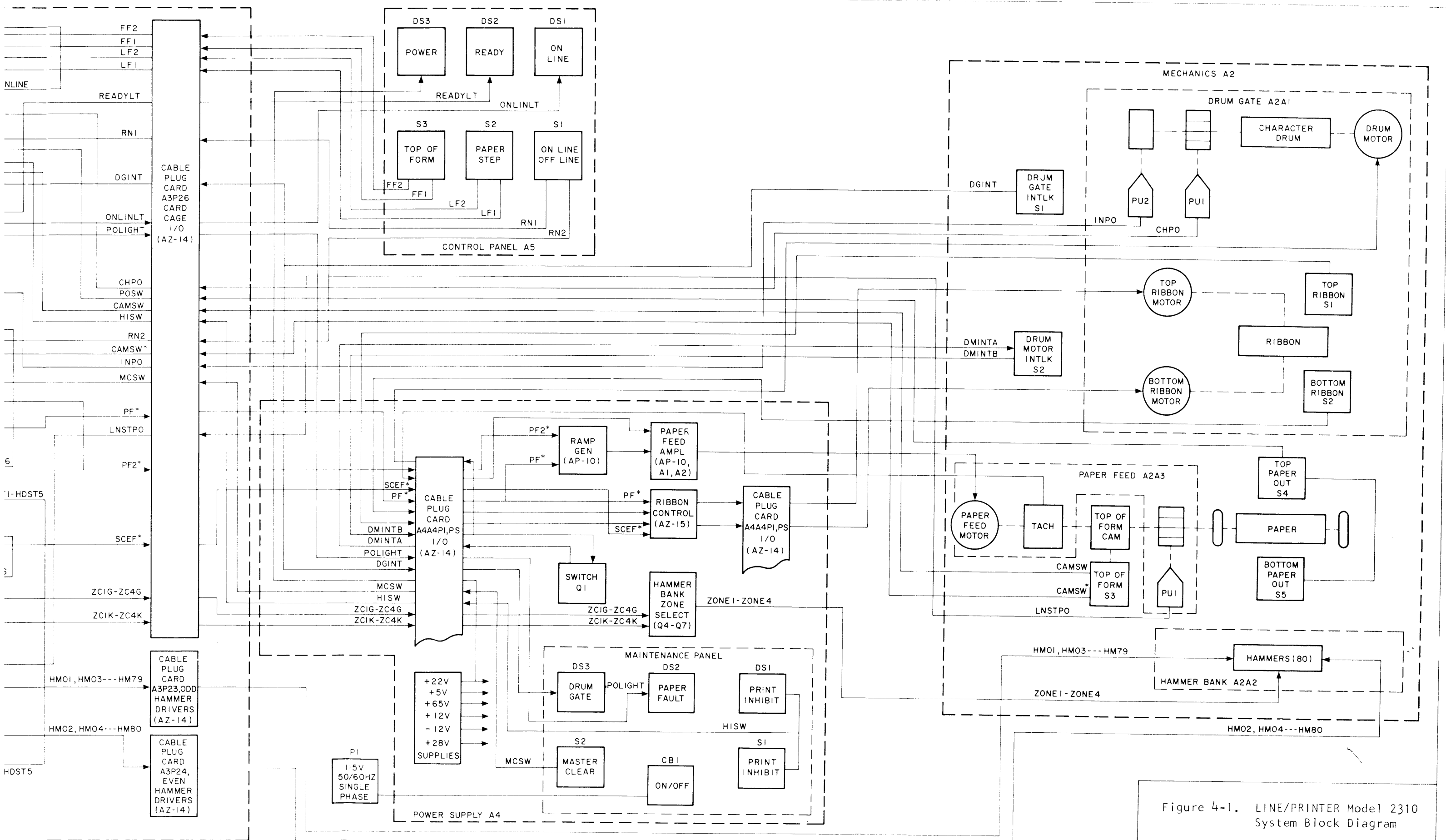


Figure 4-1. LINE/PRINTER Model 2310 System Block Diagram

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4-7 Signals CHCK1, CHCK2, and CHCK3 enable those hammer drivers whose flip-flops have been set, and the characters in those print positions are printed. CCSN then initiates another scan period and the remaining characters in memory are scanned and compared as before. This operation is repeated until all characters in memory have been compared and printed.

4-8 If the print cycle is originally initiated on receipt of the 20th printable character, then signal ZCAV is generated upon completion of printing. The zone control register is incremented by 1 and DEMAND LINE enabled. The next printable character received will be printed in the leftmost position of zone 2.

4-9 If the print cycle is initiated instead by a format control command, then upon completion of printing, the column register is reset to the leftmost position (column 1) and the command executed. The demand line is enabled and the printer remains in zone 1.

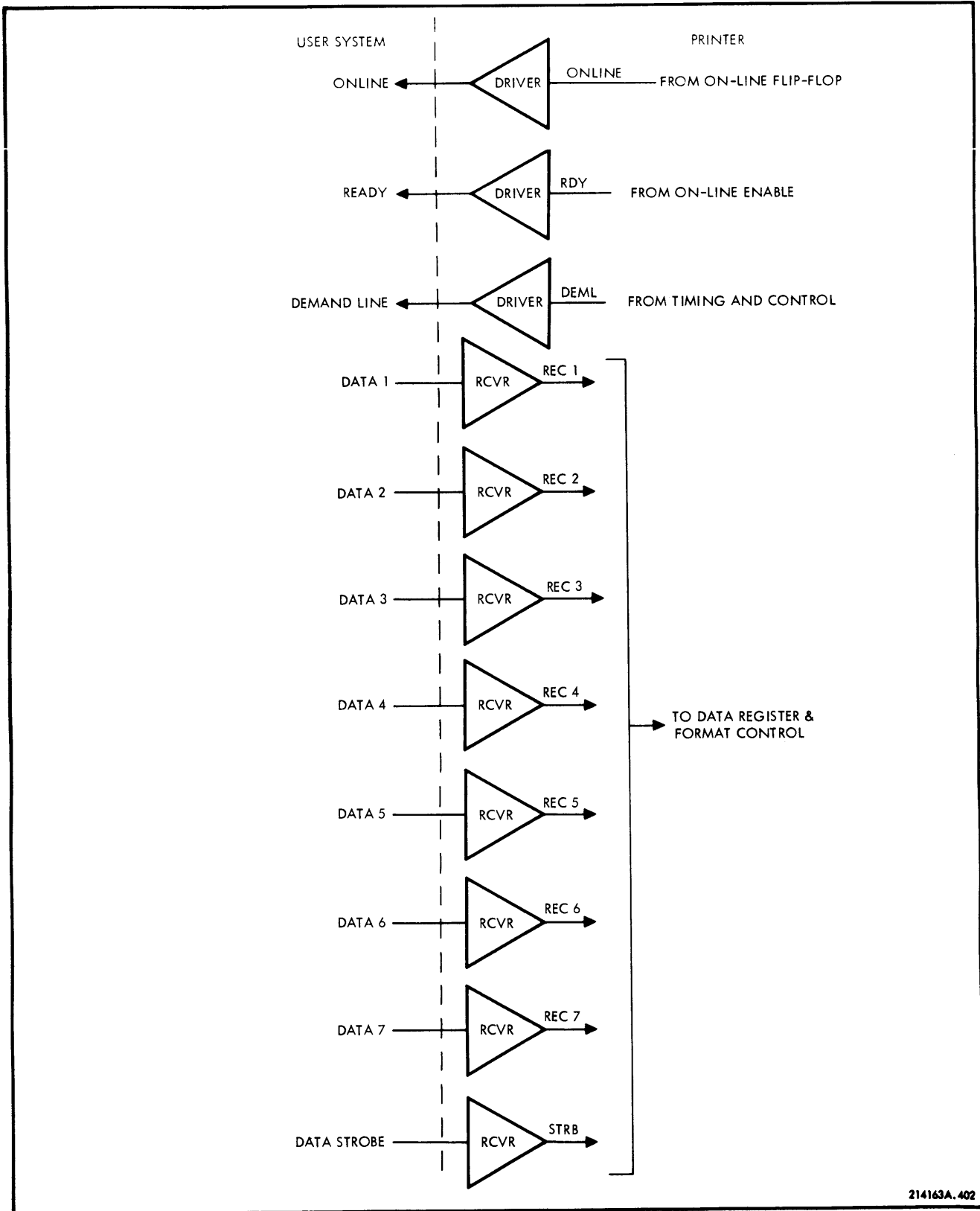
4-10 Assuming a normal print operation of 80 characters per line, the hammer drivers switch to zone 2 and memory is loaded with another set of characters from the user system. The print cycle sequence described for zone 1 is then repeated for zone 2, and again for zones 3 and 4.

4-11 INTERFACE

4-12 Signals between the printer and user system are interfaced through eight receivers and three drivers. See figure 4-2 for a simplified printer/user system interface diagram. See table 4-1 for the receiver and driver characteristics.

Table 4-1. Receiver/Driver Characteristics

Item	Receiver	Driver
Input Impedance	10K	
Output Impedance		100 ohms
Load Resistance		10K to ground
Load Capacitance		220 pf
Signal Transition Rate		40v/usec (typical)
Logic 1	Adjustable from +10.0v max to + 3.0v min	Adjustable from +8.0v max to +3.0v min
Logic 0	+1.0v max 0.0v min	+1.0v max (AJ-11) +0.4v max (AJ-14)
Threshold Voltage	1/2 of logic 1	



214163A.402

Figure 4-2. Printer/User System Simplified Interface Diagram

## 4-13 PRINTER/USER SYSTEM INTERFACE SIGNALS

4-14 Table 4-2 lists and defines the interface signals between the printer and user systems. The timing diagram in figure 4-3 shows the relationships of the signals on the interface lines.

4-15 Coded Character Set

4-16 A 7-bit code is used to transmit information to the printer on data lines DATA1 thru DATA7. The code is derived from a modified version of the American Standard Code for Information Interchange (ASCII). Table 4-3 shows the allowable printable character codes, and the three format control character codes. Non-printable bit combinations received by the printer result in a space.

Table 4-2. Interface Signal Definitions

Signal	Definition	Source
READY	Indicates to the user system that printer is ready to be put ON LINE by the printer operator  When READY is true, the following are true: (a) Power is on (b) The printer drum gate is closed (c) Paper is loaded (d) A fault condition does not exist	Printer
ON LINE	Indicates to the user system that printer is ON LINE	Printer
DEMAND LINE	Synchronizes data transmission between the printer and user system. DEMAND LINE signal requests a character from the user and remains true until signal DATA STROBE is received. It is disabled while the character is stored in memory and during the print operation. DEMAND LINE can only come true if READY is true and the operator has placed the printer ON LINE	Printer
DATA STROBE	Indicates when printer is to accept the information on the data lines. Each time signal DATA STROBE occurs, the printer samples the data lines and DEMAND LINE goes false while the character is stored.	User
DATA1 THRU DATA7	Coded information transmitted from user system to printer on seven data lines. Each character of the ASCII character set is transmitted as a 7-bit DATA signal.	User

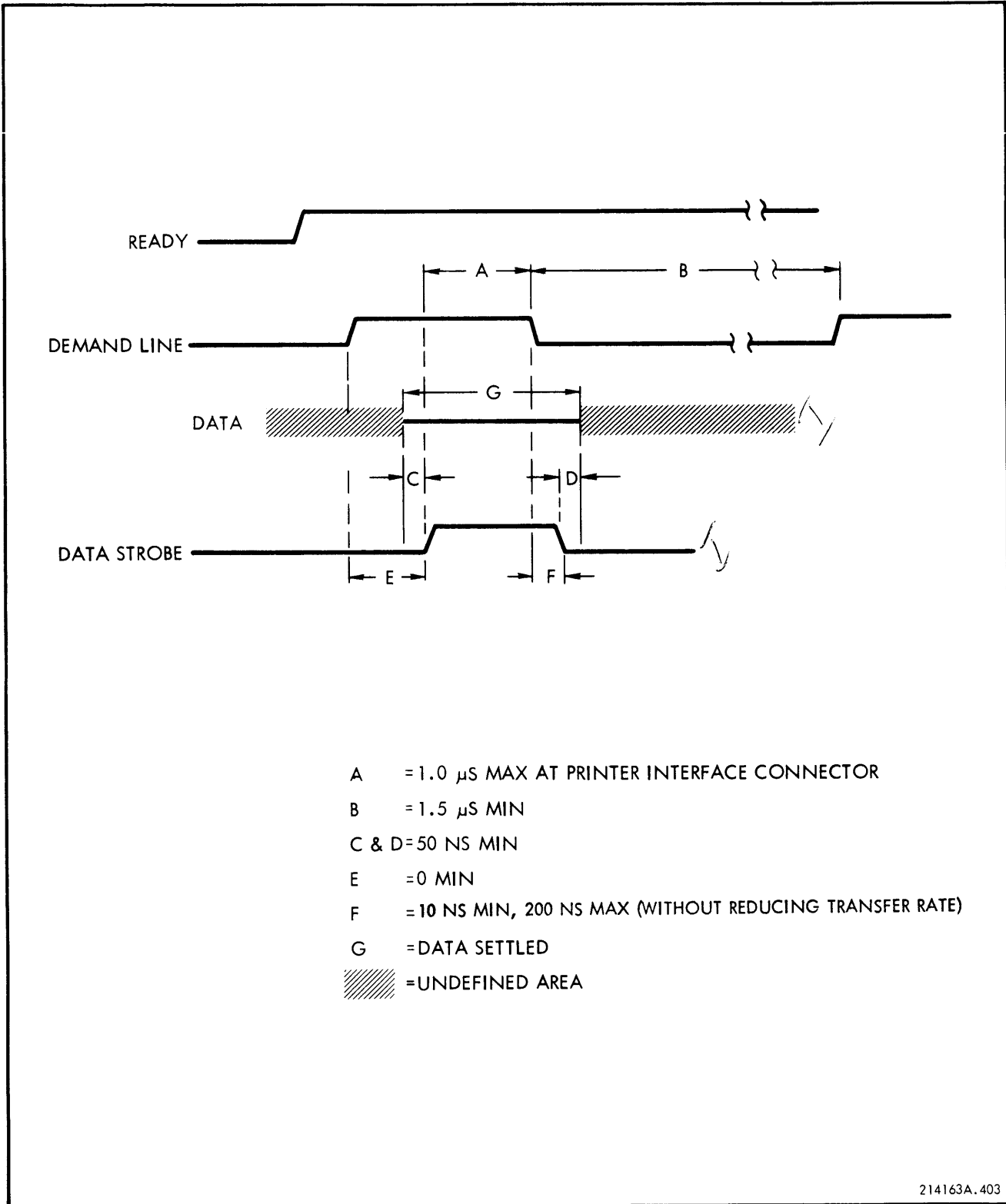


Figure 4-3. Interface Signal Lines Timing Diagram

4-17 FORMAT CONTROL

4-18 Characters PF, CR, and FF, in table 4-3, are the three characters available to the user for format control. Each is a command that places the printer in the print mode, and upon completion of printing is executed as follows:

a. PF (Paper Feed). The PF command advances the paper one line, clears the column register, returning it to the leftmost print position, and initializes the zone control register. DEMAND LINE is enabled before the paper comes to a stop, and the printer accepts the next set of characters. If the first character in the new set is another PF instruction, DEMAND LINE is disabled and the paper continues slewing for another line. Slewing will continue, one line for every PF command, as long as PF commands are transmitted. A top-of-form cam output during a given paper feed will cause the paper to slew for 3 lines and thus skip over perforations.

b. CR (Carriage Return). The CR command clears the column register, and initializes the zone control register.

c. FF (Form Feed). The FF command advances the paper to the third line of the next form, clears the column register, and initializes the zone control register. DEMAND LINE is enabled before the paper is stopped.

Table 4-3. Coded Character Set

b7 b6 b5	0 0 0	0 1 0	0 1 1	1 0 0	1 0 1
b4 b3 b2 b1					
0 0 0 0		Space	Ø	@	P
0 0 0 1		!	1	A	Q
0 0 1 0		"	2	B	R
0 0 1 1		#	3	C	S
0 1 0 0		\$	4	D	T
0 1 0 1		%	5	E	U
0 1 1 0		&	6	F	V
0 1 1 1		'	7	G	W
1 0 0 0		(	8	H	X
1 0 0 1		)	9	I	Y
1 0 1 0	PF	*	:	J	Z
1 0 1 1		+	;	K	[
1 1 0 0	FF	,	<	L	Ø
1 1 0 1	CR	-	=	M	]
1 1 1 0		.	>	N	^
1 1 1 1		/	?	O	∞



4-19 ON-LINE PRINTER OPERATION

4-20 The following paragraphs are a detailed description of the on-line printer operation, using functional block diagrams, flow diagrams, timing diagrams, and logic diagrams as an aid to understanding. In describing logic levels, the terms true and high are used interchangeably, as are false and low.

## 4-21 PRINTER POWER

4-22 Power is applied to the printer when circuit breaker CB1, on power supply A4, is ON.

4-23 Power Supply A4 (See figure 4-4)

4-24 Power supply A4 provides the printer with operating voltages, ribbon control, paper feed motor drive, and hammer bank zone selection. Power supply A4 contains the following card types:

- a. Voltage Regulator AV-10
- b. Ribbon Control AZ-84
- c. Paper Feed Control AP-10
- d. Power Amplifier AZ-49 (4)
- e. Power Amplifier AZ-51
- f. SCR Commutating AZ-79
- g. Bridge AZ-78

4-25 The input to power supply A4 is normally 115v, 50/60 Hz, single-phase power. It is applied through circuit breaker CB1 to the multiple-tapped primary of transformer T1. The primary of T1 can be connected for a wide range of input voltages (see table 1-1), and its secondary outputs are rectified and filtered to provide the following operating voltages:

- a. +5v
- b. +12v
- c. -12v
- d. +22v
- e. +28v
- f. +65v

4-26 The drum and ribbon motors require 115 vac operating voltage. The drum motor is supplied from the primary side of transformer T1 through an interlock consisting of switch A2S2 and triac switch Q5. The top and bottom ribbon motors are supplied from secondary outputs of transformer T1. When the drum gate is closed and latched, switch Q5 is triggered each time the 115 vac input goes through the crossover point. This closes the drum motor input line and completes the circuit (figure 6-20). If the drum gate is open or improperly latched, interlock switch A2S2 deactivates, removing the trigger potential from switch S5. The drum motor input line now remains open, preventing the motor from running.

4-27 Regulation of the +12v, +5v, and +28v outputs is provided by series regulator circuits A7 thru A9, and card type AV-10. See figure 4-5 for a simplified block diagram of the regulator circuitry.

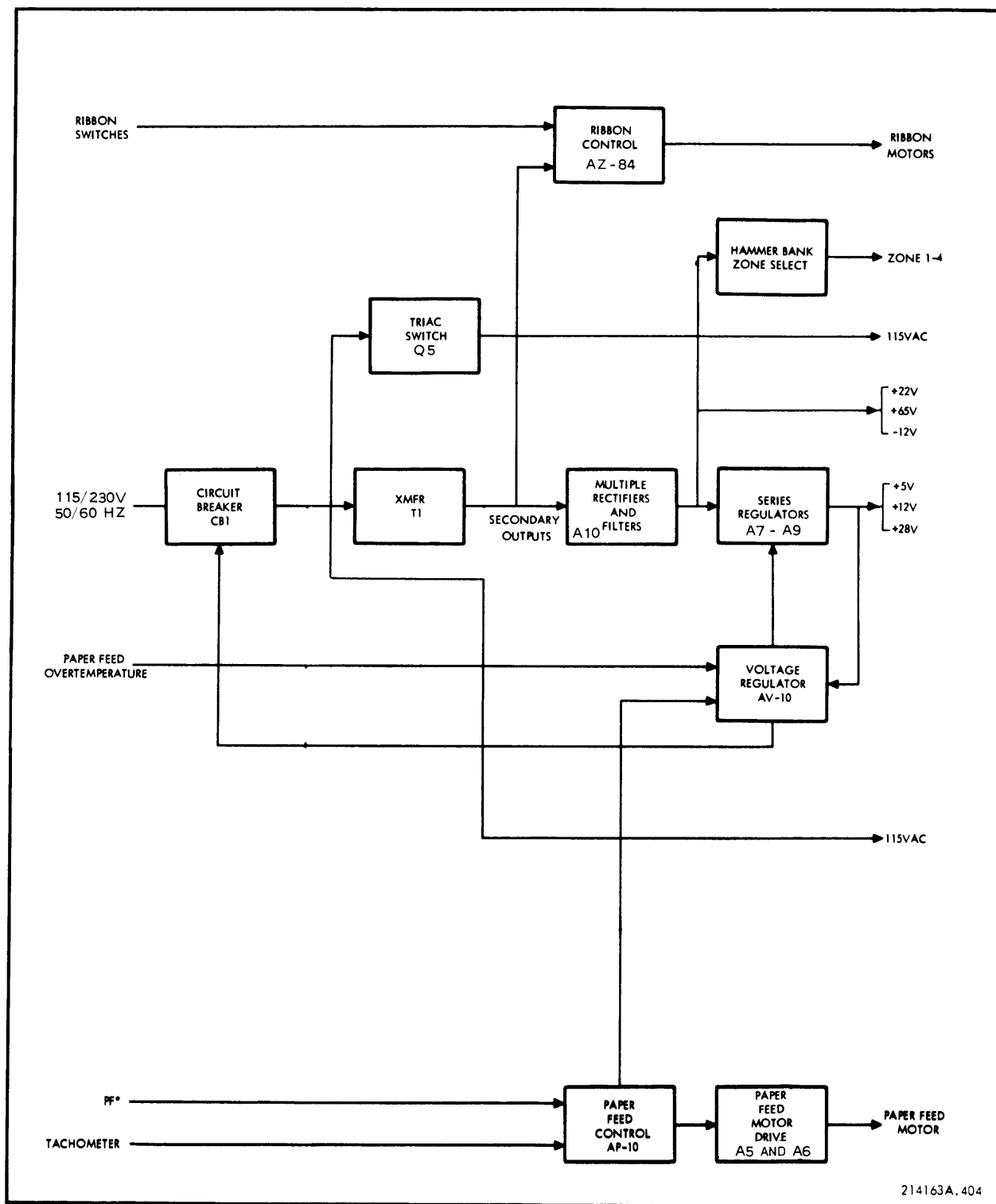
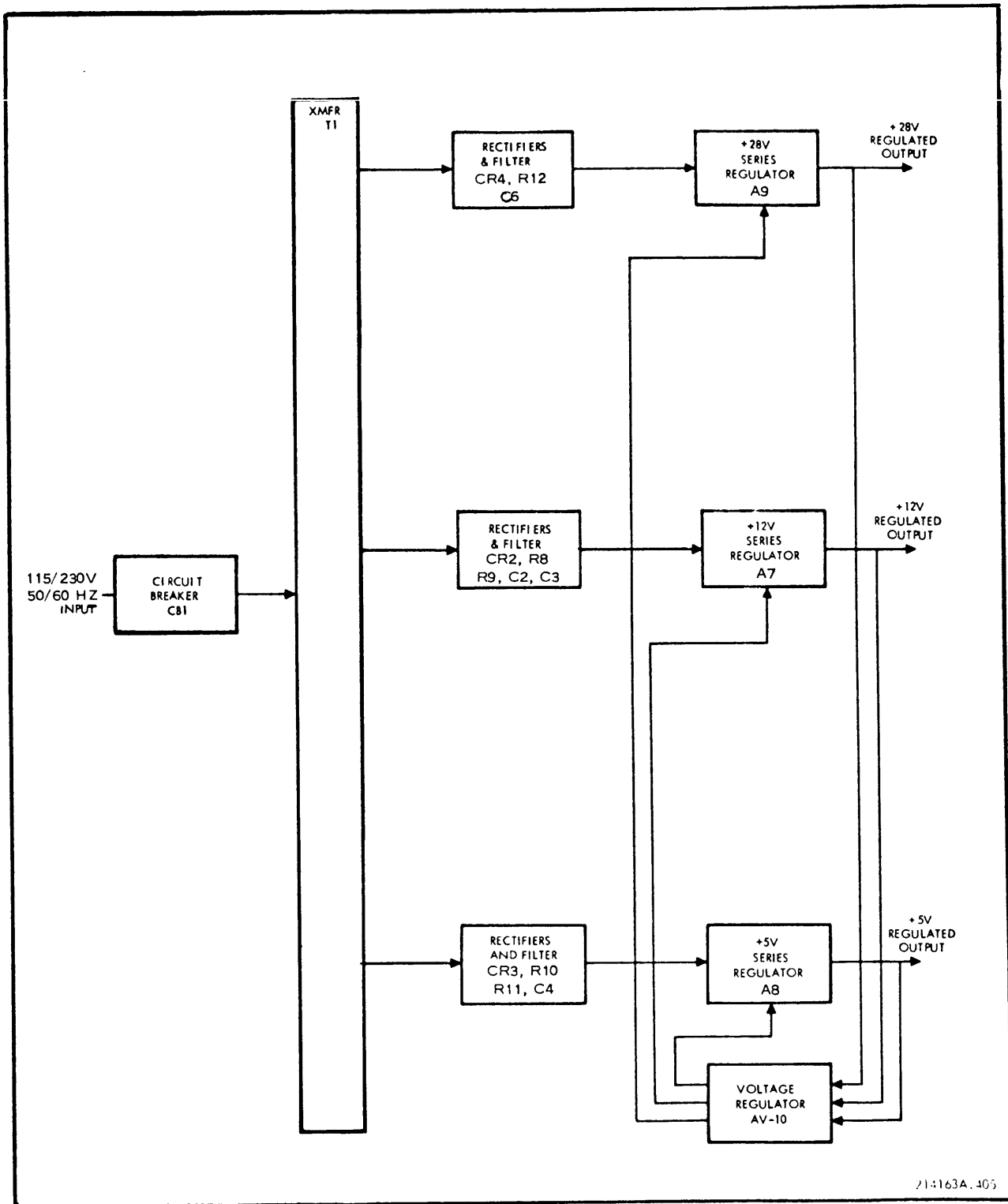


Figure 4-4. Power Supply A4 Simplified Block Diagram



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Figure 4-5. Power Supply A4 Regulation Simplified Block Diagram

4-28 Paragraphs 4-29 through 4-59 contain a functional description of card types AV-10, AZ-15, and AP-10 on a block diagram level.

4-29 VOLTAGE REGULATOR AV-10. Voltage regulator AV-10 contains control circuitry for the +5v, +12v, and +28v series regulators. It also has protect circuits for the +5v, and +12v supplies and can shut down power supply A4 in the event of a paper feed motor overtemperature or overspeed condition. See figure 4-6 for a functional block diagram of voltage regulator AV-10.

4-30 The +5v series regulator control consists of differential amplifier Q1/Q2, and driver Q3. Regulator diode VR1 references Q1, and potentiometer R2 sets the +5v series regulator output. The regulator output is returned from card cage A3 as signal +5v REF and applied to the input of Q2. A change in the +5v REF signal causes the differential amplifier to develop an output signal proportional to the difference between the +5v REF signal and the reference voltage provided by VR1. This signal is applied through driver Q3 to the regulator, and regulates the +5v output by controlling the current through the series regulator. As the regulator output returns to the desired level, the difference is nulled out. The feedback loop ensures that a change in the +5v output is reflected in a counteracting change in the control signal.

4-31 The +5v supply is protected against an overcurrent condition by current monitor Q5 and thyristor (SCR) Q4. An overcurrent condition turns Q5 on and its output triggers Q4. Q4 shorts the +5v drive current to ground, and the +5v output drops to zero.

4-32 The +5v supply is protected against an overvoltage condition by detector Q6 and thyristor (SCR) A4Q6. An overvoltage condition turns detector Q6 on and its output triggers A4Q6. A4Q6 shorts the +16v supply current to ground and fuse F1 blows.

4-33 The +12v series regulator control consists of differential amplifier Q7/Q8, and driver Q9. Regulator diode VR3 references Q7, and potentiometer R22 sets the +12v series regulator output. The regulator output is returned from card cage A3 as signal +12v REF and applied to the input of Q8. A change in the +12v REF signal causes the differential amplifier to develop an output signal proportional to the difference between the +12v REF signal and the reference voltage provided by VR3. This signal is applied through driver Q9 to the regulator, and regulates the +12v output by controlling the current through the series regulator. As the regulator output returns to the desired level, the difference input is nulled out. The feedback loop ensures that a change in the +12v output is reflected in a counteracting change in the control signal.

4-34 The +12v supply is protected against an overcurrent condition by current monitor Q11 and thyristor (SCR) Q10. An overcurrent condition turns Q11 on and its output triggers Q10. Q10 shorts the +12v drive current to ground, and the +12v output drops to zero.

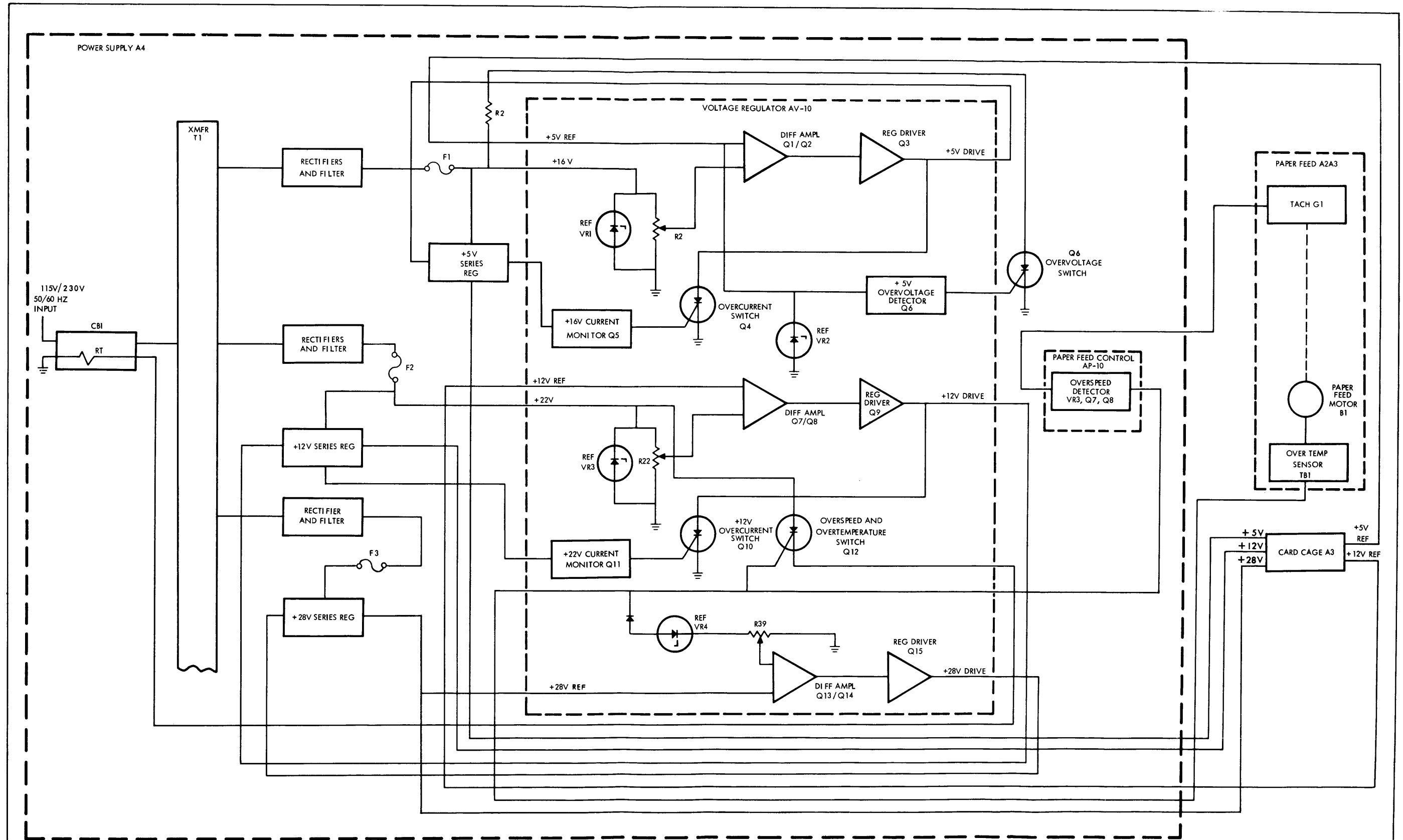


Figure 4-6. Voltage Regulator AV-10 Functional Block Diagram

4-35 The +28v series regulator consists of differential amplifier Q13/Q14, and driver Q15. Regulator diode VR4 references Q13, and potentiometer R39 sets the +28v series regulator output. The regulator output is applied to the input of Q14. A change in the +28v output causes the differential amplifier to develop an output signal proportional to the difference between the input to Q14 and the reference voltage provided by VR4. This signal is applied through driver Q15 to the regulator, and regulates the +28v output by controlling the current through the series regulator. As the regulator output returns to the desired level, the difference input is nulled out. The feedback loop ensures that a change in the +28v output is reflected in a counteracting change in the control signal.

4-36 Paper feed motor B1 is protected against an overspeed condition by thyristor (SCR) Q12 and detector Q7/Q8 located in card type AP-10. An overspeed condition turns the detector on (see paragraph 4-56) and its output triggers Q12. Q12 shunts +22v to relay coil RT in circuit breaker CB1. The relay energizes and opens CB1, removing input power from power supply A4.

4-37 Paper feed motor B1 is protected against an overtemperature condition by SCR Q12 and overtemperature sensor TB1. In an overtemperature condition, the sensor output triggers Q12. Q12 shunts +22v to relay coil RT in circuit breaker CB1. The relay energizes and opens CB1, removing input power from power supply A4.

4-38 Overtemperature Sensor TB1 (see figure 4-7). Overtemperature sensor TB1 contains a heat sensor element consisting of thermostat S1 and coil HR1. The thermal constants of this combination approximate those of paper feed motor B1 and motor current passing through coil HR1 causes heat to be coupled to thermostat S1. The temperature at which thermostat S1 closes is  $265 (\pm 8)^{\circ}\text{F}$ . A temperature of  $265^{\circ}\text{F}$  is excessive, but well below the level at which motor damage can occur. As the sensor and motor track together, an excessive rise in motor temperature immediately actuates thermostat S1 and removes printer power as described in paragraph 4-37.

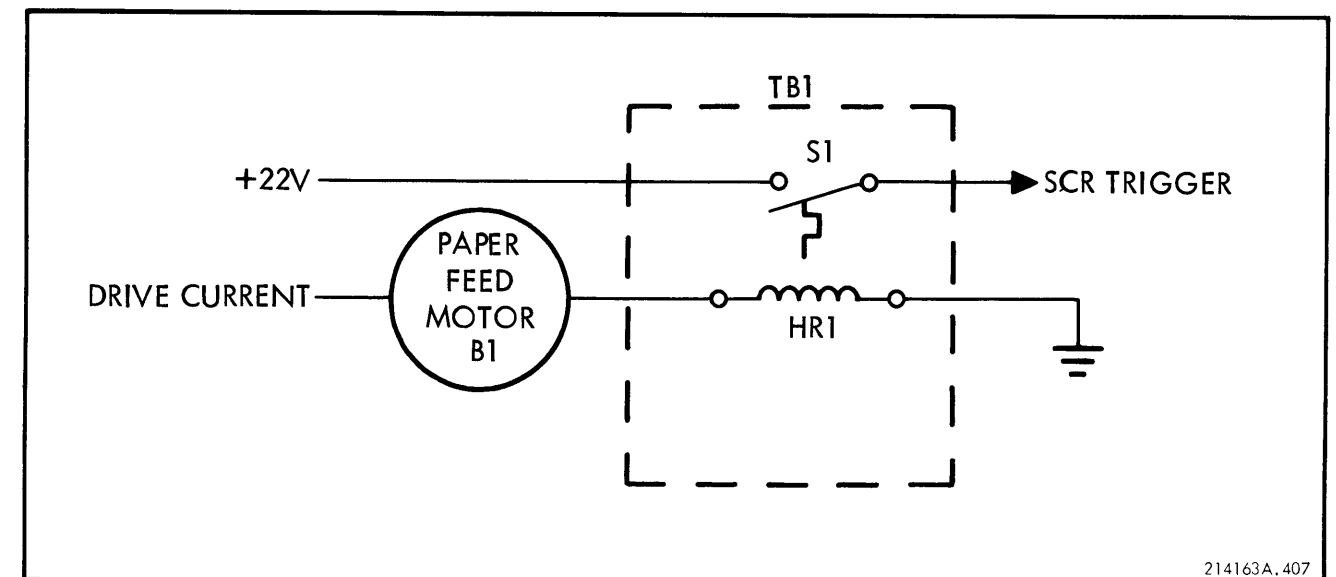


Figure 4-7. Overtemperature Sensor TB1

4-39 RIBBON CONTROL AZ-84. Ribbon control AZ-84 contains logic for the control and direction of print ribbon motion. See figure 4-8 for a functional block diagram of ribbon control AZ-84.

4-40 Print ribbon start and stop motion is synchronized to the zero crossover point of the 60 Hz line voltage, and controlled by flip-flop RUN. Direction of motion is determined by flip-flop DIR.

4-41 The set input of flip-flop RUN is held true and the reset input false. The clear input to flip-flop RUN is provided by a 0.25 second r-c time delay circuit consisting of Q1, Z1, and Q2, and flip-flop RUN is cleared when the printer is initialized. Ribbon switches S1 and S2 provide set and reset inputs, respectively, to flip-flop DIR. The clock inputs to flip-flops RUN and DIR are provided by waveshaper Q1, which converts a 3 vac input signal to a logic level output. The fall of the clock occurs at the zero crossover point of the 3 vac input signal.

4-42 Flip-flop RUN remains cleared, inhibiting ribbon motion, for as long as the printer remains in a nonprint state. Assuming the ribbon is not fully wound when the printer is initialized, the state of flip-flop DIR can be either set or reset because both inputs are false.

4-43 During a print cycle, signal PF\* or SCEF\* goes false and the clear input to flip-flop RUN goes true. On the fall of the next clock, flip-flop RUN sets. Assuming flip-flop DIR is in a reset state, gate 1 is now enabled. The output of gate 1 is applied to trigger Q301/Q302, and the trigger output fires thyristors (SCR) Q303 and Q304.

4-44 The ribbon motor excitation is 115v, 60 Hz, and is applied to the bottom ribbon motor through SCR motor drive switches Q303 and Q304. SCR Q304 switches the drive current to the ribbon motor on the 115 vac positive half-cycle, and Q303 switches the drive current on the negative half-cycle. The ribbon is driven downward until the end of travel is reached, at which time the top ribbon bar actuates top ribbon switch S1. When switch S1 closes, the output of inverter Z2A goes true and at the next clock time, flip-flop DIR sets. The set output of flip-flop DIR enables gate 2 and the reset output goes false disabling gate 1. Disabling gate 1 removes the trigger voltage from SCR switches Q303 and Q304. The switches open and cut off drive current to the bottom ribbon motor. Enabling gate 2 applies a trigger voltage to SCR motor drive switches Q403 and Q404. The SCR switches fire, and apply excitation to the top ribbon motor in the manner described for the bottom ribbon motor. As the ribbon is driven upward, switch S1 opens and the set input to flip-flop DIR goes false. When the ribbon again reaches the end of travel, bottom ribbon switch S2 is actuated by the bottom ribbon bar. When switch S2 closes, the output of inverter Z2B goes true and flip-flop DIR resets at the next clock time. Gate 1 is again enabled, and gate 2 disabled, and the operation previously described is repeated.

4-45 When the printer enters a nonprint state, signals PF\* and SCEF\* go true, are inverted by Z2D, and applied to the input of transistor Q1. The output of Q1 goes high and activates the r-c time delay. If PF\* and SCEF\* stay true for a minimum of 0.25 seconds, the output of operational amplifier Z1 will go high at the end of that time. The output of Q2 then goes low and clears flip-flop RUN. Clearing flip-flop RUN disables gates 1 and 2 and inhibits ribbon motion. While

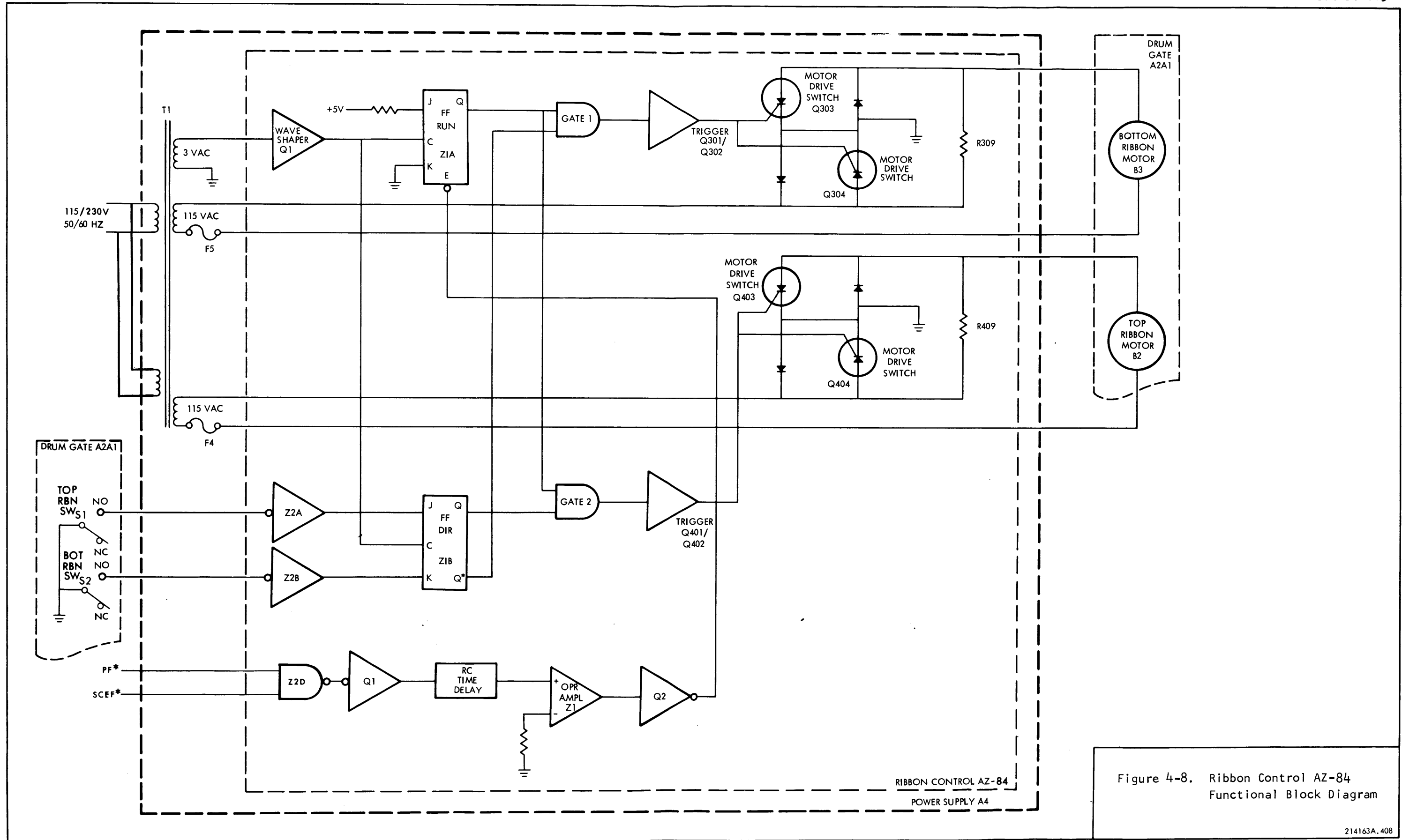


Figure 4-8. Ribbon Control AZ-84 Functional Block Diagram



PF\* and SCEF\* remain true, the clear input stays low, and flip-flop RUN cannot be set. When PF\* or SCEF\* goes false the r-c time delay is discharged and the output of Q2 immediately goes true. At the next clock time, flip-flop RUN is set, and the ribbon is driven as previously described.

4-46 Resistors R309 and R409 allow a small amount of residual current to flow through each ribbon motor after its associated SCR switches are turned off. As the ribbon motors drive in opposite directions, the result is a slight drag which keeps the ribbon taut when not in motion. The drag current through either motor is easily overcome by the drive current through the opposing motor.

4-47 The use of ac voltage excitation for the ribbon motors provides an automatic extinction feature when gate potential is removed from the SCR switches. The extinction voltage for an SCR is very low, and ac drops to zero twice in every cycle. For this reason flip-flops RUN and DIR are synchronized to the 60 Hz line. Initiating or terminating drive power exactly as the ac line voltage passes through zero volt ensures that transients will not be generated at these times.

4-48 PAPER FEED CONTROL AP-10. Paper feed control AP-10 contains a ramp generator and paper feed amplifier which advances printer paper by providing and controlling the paper feed motor drive. Card type AP-10 also contains a detector circuit to protect the paper feed motor against an overspeed condition. See figure 4-9 for a functional block diagram of paper feed control AP-10, and figure 4-10 for a timing diagram of paper feed control.

4-49 To advance paper one line during a print cycle signal PF\* goes false, is inverted by paper advance amplifier Q1, and applied to the input of a ramp generator consisting of comparator amplifier Z1 and integrator amplifier Z2. The ramp generator provides a velocity command input signal, set by potentiometer R18, to a paper feed amplifier consisting of error amplifier Z3, positive driver Q3/Q5, negative driver Q4/Q6, forward power amplifier A6, and reverse power amplifier A5. The power amplifiers are card types AZ-49 and AZ-51, respectively, and provide drive current to paper feed motor B1. In the time required to advance the paper one line, the motor is accelerated to a constant velocity, decelerated, and stopped.

4-50 Under static conditions, a fixed (holding) voltage on the inverting input of error amplifier Z3 produces an output sufficient to cut off positive driver Q3/Q5, and turn negative driver Q4/Q6 on slightly. The small drive input to reverse power amplifier A5 produces a slight reverse current through the motor. A unidirectional clutch mounted on the motor shaft locks the shaft as the motor is driven in the reverse direction. Thus, the reverse current maintains paper tension and prevents paper movement between paper feed commands.

4-51 Ramp Generator Operation. When PF\* goes false the output of paper advance amplifier Q1 goes true and is applied to the inverting input of comparator Z1. The output of Z1 is a negative-going step applied to switch network CR1-CR4. The diode network provides the means to switch a plus or minus 9v input to integrator Z2. Prior to PF\* going false, diodes CR1 thru CR4 are on, and the voltages cancel each other. Thus, the initial voltage level at junction CR1 and CR2, and junction

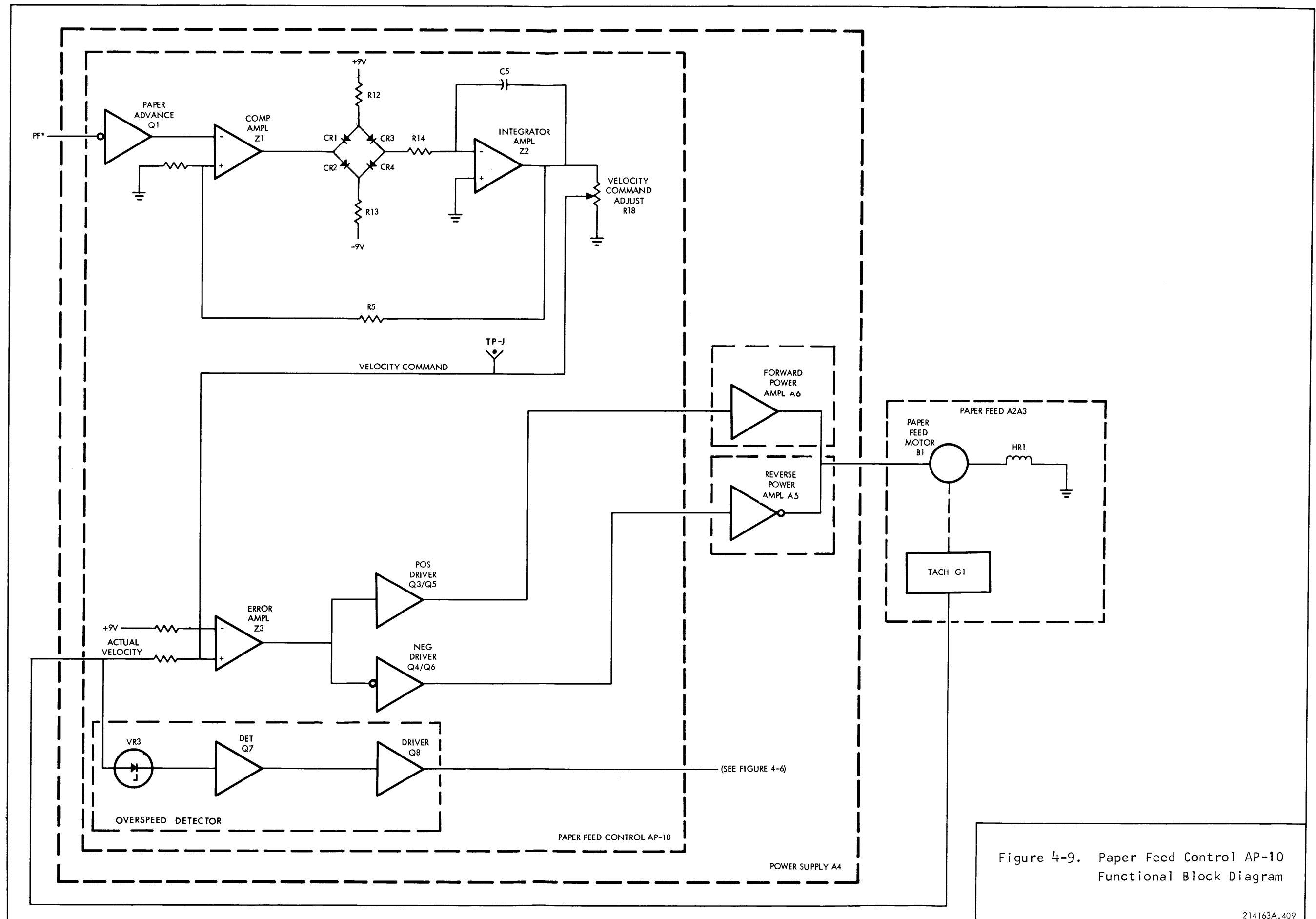


Figure 4-9. Paper Feed Control AP-10 Functional Block Diagram

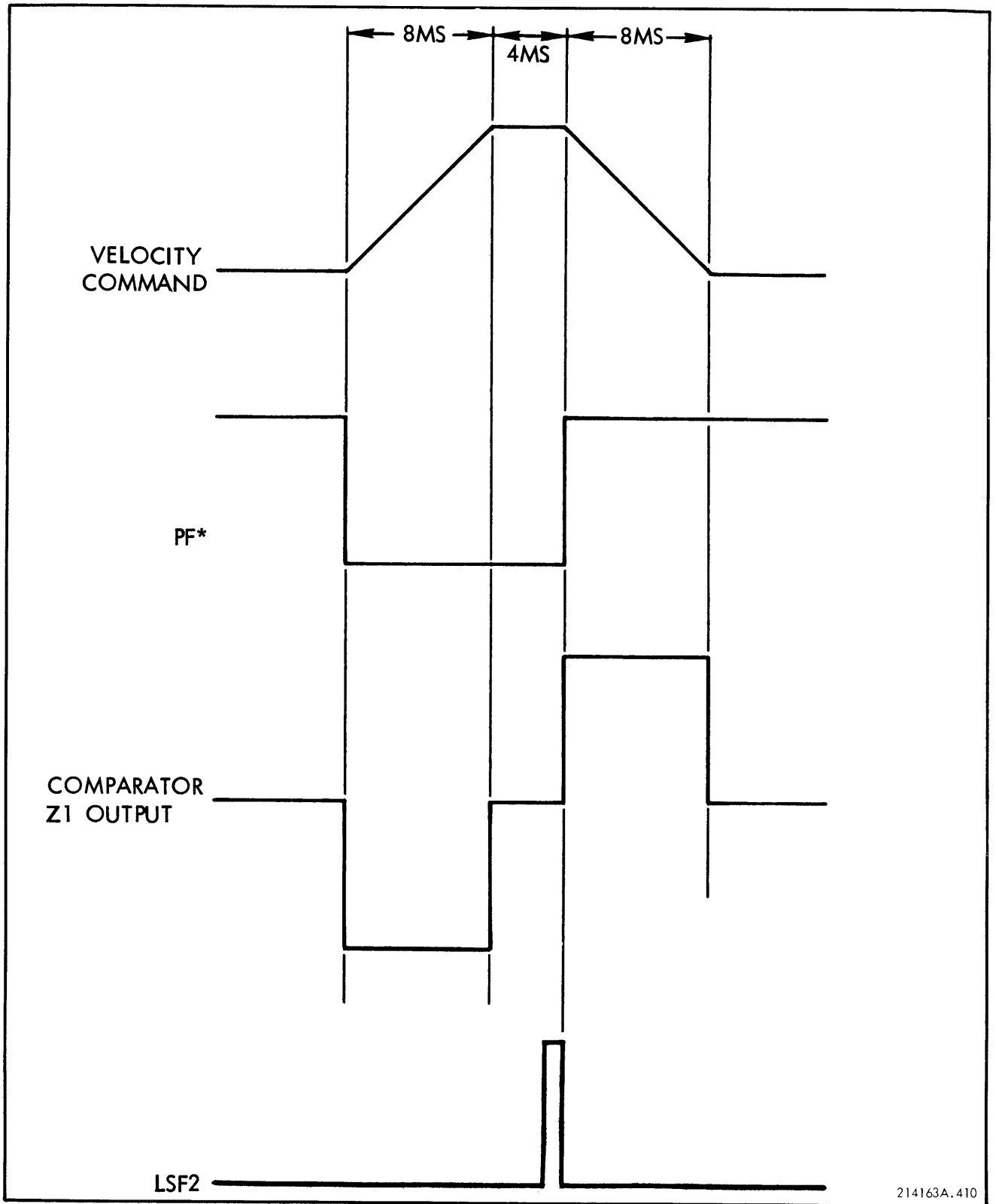


Figure 4-10. Paper Feed Control Timing Diagram

CR3 and CR4 is zero. The negative-going output of Z1 cuts off diodes CR2 and CR3, and the -9v is now applied through R13, CR4, and R14 to the inverting input of integrator Z2. The integrating action of Z2 is due to feedback capacitor C5, and its output is a positive-going linear ramp directly proportional in amplitude to the desired paper velocity. The ramp output of Z2 is fed back through resistor R5, to the noninverting input of Z1. In 8 ms, the feedback input is equal to the signal at the inverting input of Z1, and the two cancel at the output of Z1. When this occurs the output of Z1 goes to zero, and diodes CR2 and CR3 turn on. The +9v and -9v again cancel and the input to Z2 goes to zero. Z2 stops integrating and maintains a constant output level until PF\* goes true. This occurs 12 ms after PF\* initially went false.

4-52 When PF\* goes true, the output of Q1 goes false and the output of Z1 becomes a positive-going step. This is applied to switch network CR1-CR4 and cuts off diodes CR1 and CR4. The +9v is now applied through R12, CR3, and R14 to the inverting input of Z2. Z2 begins integrating and its output is now a negative-going linear ramp. In 8 ms the feedback input at Z1 is again equal to the inverting input and the two cancel at the output of Z1. The output of Z1 drops to zero and diodes CR1 and CR4 turn on, removing the input from Z2. The output of Z2 is now at zero and remains so until it is again time to advance paper and PF\* goes false.

4-53 Paper Feed Amplifier Operation. The paper feed amplifier, motor, and motor driven tachometer form a closed loop servo system. The tachometer develops an output signal directly proportional to the actual velocity of the motor. The tachometer output and the ramp generator output are summed at the noninverting input of error amplifier Z3. Initially, the tachometer output is at zero, and when the ramp generator begins velocity command integration, an error voltage develops sufficient to overcome the holding voltage at the inverting input. The result is a positive-going error signal at the output of Z3 which cuts off negative driver Q4/Q6 and reverse power amplifier A5. Positive driver Q3/Q5, and in turn forward power amplifier A6, are turned on enough to overcome the reverse current and start the motor and tachometer rotating. The tachometer rotation produces an actual velocity negative-going voltage which continually subtracts from the velocity command voltage, reducing the error signal and maintaining a constant rate of acceleration. When velocity command integration ceases, the error signal that remains maintains the motor at a constant velocity capable of advancing paper at the rate of 13 inches per second.

4-54 A line strobe code wheel on the motor is monitored by magnetic pickup A2A3PU1 which generates signals LNSTP0 and LSF2 each time the paper is advanced one line. When LSF2 occurs, PF\* goes true and the velocity command input to Z3 starts integrating down. When this occurs the actual velocity voltage from the tachometer becomes greater than the velocity command voltage and the output of Z3 reverses polarity, becoming a negative-going error signal. This cuts off positive driver Q3/Q5 and forward power amplifier A6. It turns on negative driver Q4/Q6 and reverse power amplifier A5. Reverse current is now applied to the motor and it begins to decelerate. The motor decelerates to a complete stop in the time it takes the velocity command voltage to reach zero. The holding voltage on the inverting input of Z3 takes over and locks the motor shaft as previously described.

4-55 Top-of-Form Cam. The top-of-form cam is driven by the motor and actuates cam switch S3 (figure 1-5) each time 11 inches of paper is advanced. The state of switch S3 is indicated by signals CAM and CAM\*.

4-56 The cam is advanced one line, as is the paper, with each paper feed command. During this time CAM is false and CAM\* is true. If during a paper feed command the bottom of the form is reached (11 inches advanced) the cam actuates switch S3 and CAM goes true and CAM\* goes false. When CAM\* goes false, PF\* is unable to go true when LSF2 occurs. As a result, the paper feed amplifier continues to drive the motor and advance the paper. The paper is advanced three additional lines; past the paper perforations and to the third line of the next form. The cam then releases switch S3 and CAM goes false and CAM\* goes true. When CAM\* goes true, PF\* goes true on the next LSF2, and the motor is decelerated and stopped as previously described.

4-57 If a form-feed command is given, PF\* is held false and the paper advanced until the cam actuates switch S3 and initiates the sequence described above. See figure 4-11 for a timing diagram of the top-of-form function.

4-58 Overspeed Detector. The overspeed detector monitors the tachometer output during paper advance, and consists of regulator diode VR3, detector Q7, and driver Q8.

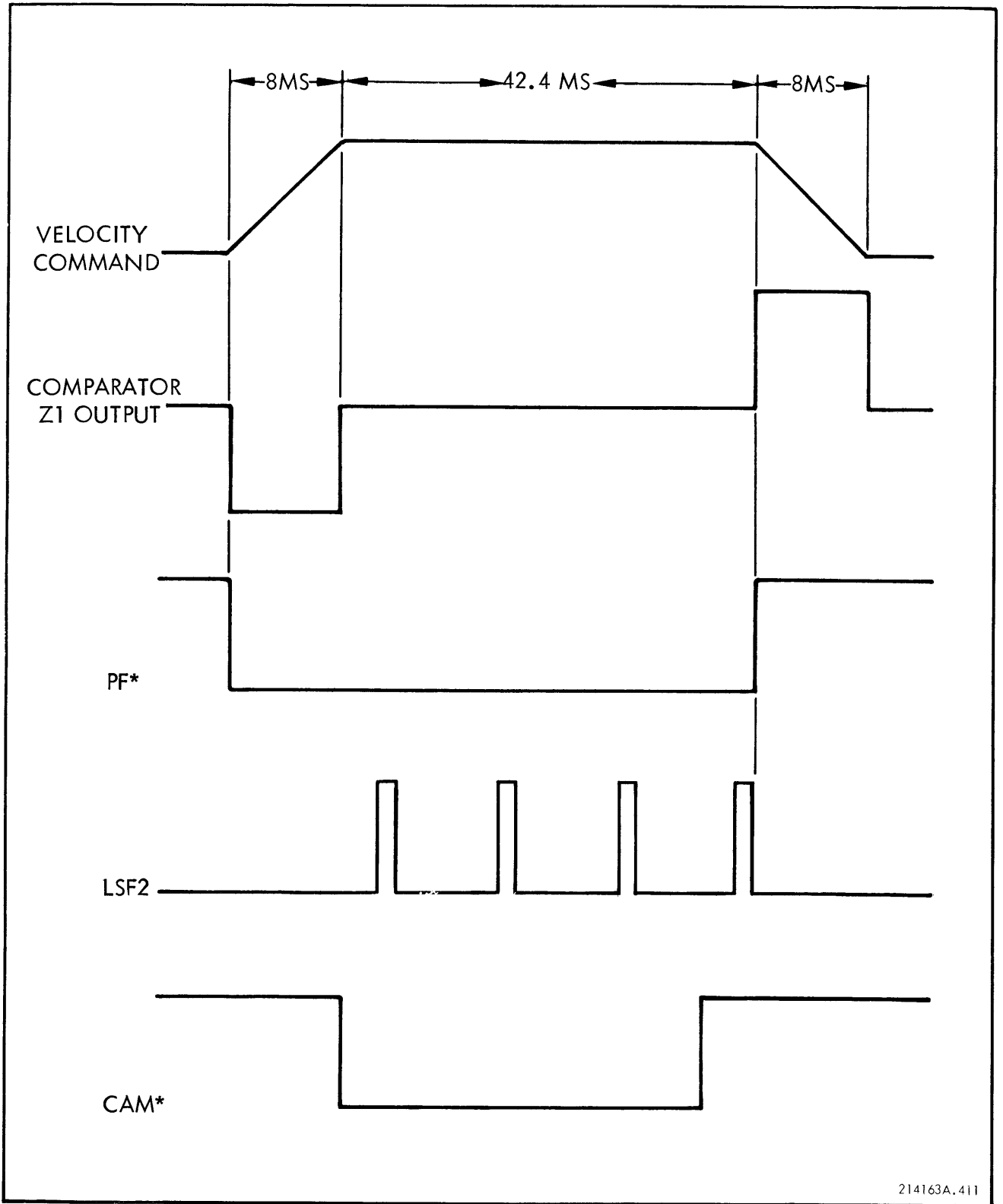
4-59 At normal motor speeds, regulator diode VR3 is cut off, detector Q7 is on, and driver Q8 is off. If motor speed becomes excessive, the tachometer output reaches the breakdown voltage of VR3. VR3 conducts, dropping the input of Q7 to zero, and Q7 turns off. Driver Q8 now turns on and its output fires SCR Q12 in voltage regulator AV-10. Q12 shunts +22v to relay coil RT in circuit breaker CB1 (see figure 4-6). The relay energizes and opens CB1, removing input power from power supply A4.

4-60 Interlock and Fault Detect

4-61 The printer is inhibited from printing if certain conditions exist or occur during printer operation. The logic necessary to perform this function is provided by hammer interlock AZ-19 and associated circuits. See figure 4-12 for a functional block diagram of hammer interlock AZ-19 and associated circuits.

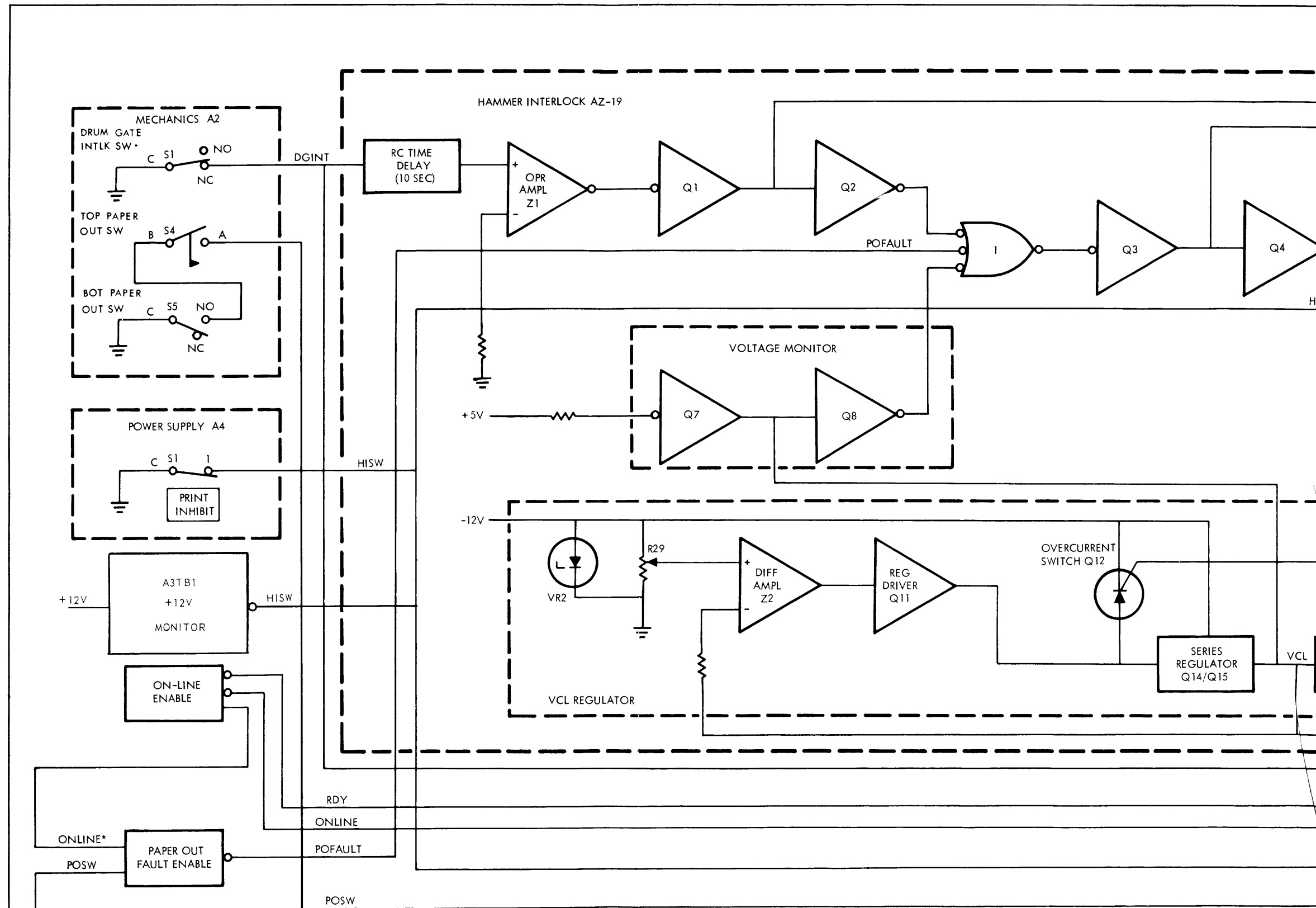
4-62 HAMMER INTERLOCK AZ-19. Hammer interlock AZ-19 contains a 10-second delay, voltage monitor, voltage clamp (VCL) control and regulator, associated logic, and three lamp driver circuits. These perform the following interlock and fault detect functions:

- a. Drum gate
- b. Paper out
- c. VCL, +5V, and +12V supplies
- d. Print inhibit



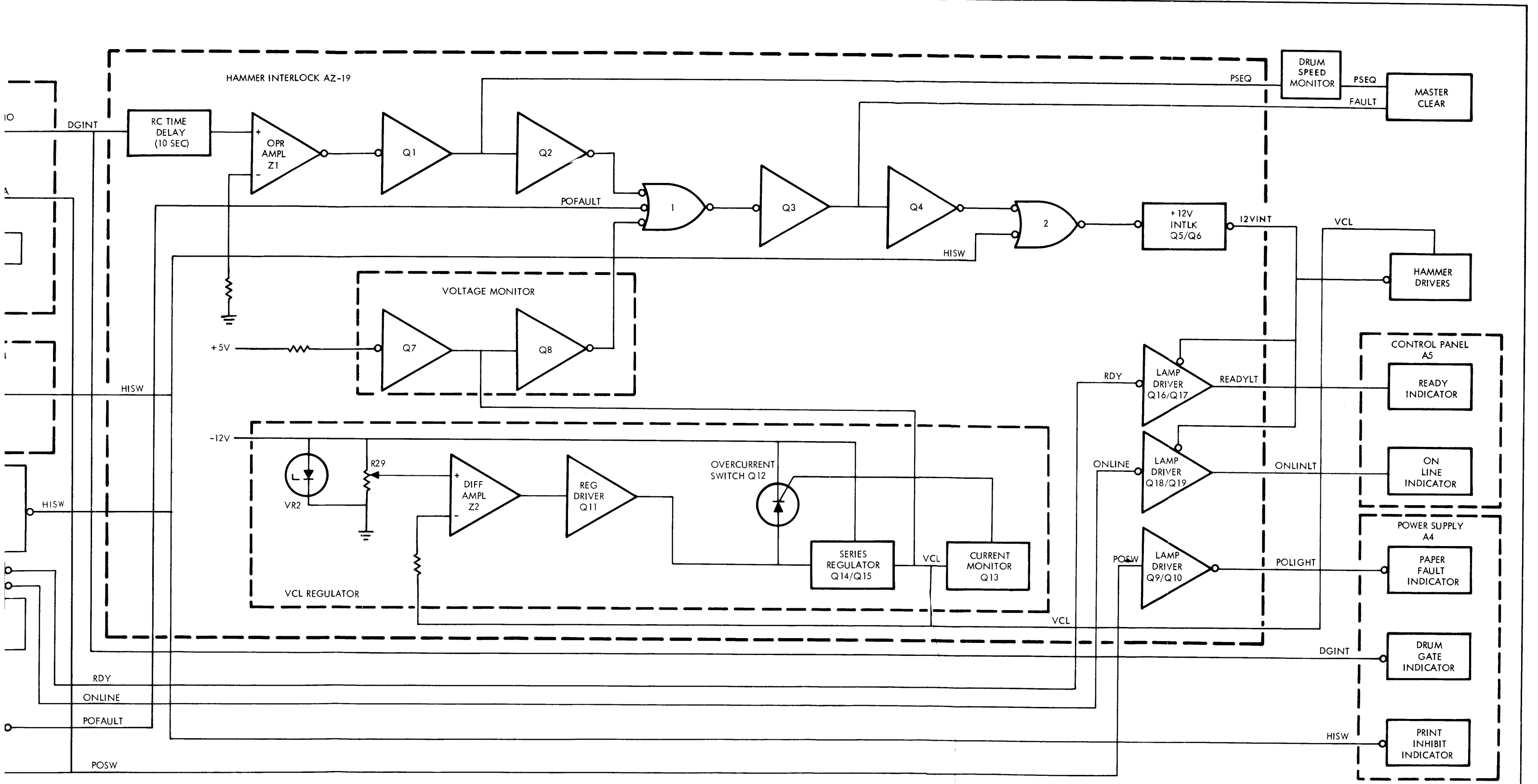
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Figure 4-11. Top-of-Form Advance Timing Diagram



NOTE:

1. SWITCHES A2S1, A2S4, AND A2S5 ARE SHOWN DEACTIVATED. SWITCH A4S1 IS SHOWN ACTIVATED.
2. THE STATE OF THE INTERLOCK AND FAULT SIGNALS IS SHOWN FOR A FAULT CONDITION.



, AND A255 ARE SHOWN  
H A451 IS SHOWN ACTIVATED.  
INTERLOCK AND FAULT SIGNALS  
IN LT CONDITION.

Figure 4-12. Hammer Interlock AZ-19  
Functional Block Diagram



4-63 Drum Gate (Closed). Drum gate interlock switch A2S1 (figure 1-5) is activated when the drum gate is closed and latched. If activated when the printer is energized, interlock signal DGINT goes high and starts the 10-second r-c time delay. At the start of the 10-second period, the output of operational amplifier Z1 goes low, is inverted by Q1, and applied as signal PSEQ to inverter Q2 and through the drum speed monitor logic to the master clear logic. PSEQ enables master clear, and the printer registers and mode flip-flops are initialized.

4-64 Simultaneously, the output of Q2 goes false and is applied to OR gate 1. The output of OR gate 1 is inverted by Q3, and signal FAULT goes true. FAULT is inverted by Q4 and applied to OR gate 2. FAULT is an additional input to the master clear logic, but does not affect master clear during the 10-second delay period. The output of OR gate 2 is applied to +12v interlock amplifier Q5/Q6. The amplifier output, 12VINT (+12v) goes low, disabling hammer drivers, and the ready and on-line lamp drivers.

4-65 At the end of the 10-second delay period, the output of operational amplifier Z1 goes high and PSEQ goes low. If drum is up to speed, master clear is disabled and the printer registers and mode flip-flops become operational. Assuming that other interlock and fault detect functions are normal, when PSEQ goes low, FAULT goes low and 12VINT goes high. Hammer drivers, and lamp drivers are enabled.

4-66 With master clear disabled, signal RDY goes true and is applied to ready lamp driver Q16/Q17. The lamp driver output, READYLT, goes low and provides a return for the READY indicator on control panel A5. The READY indicator lights.

4-67 If the printer is operated on-line, signal ONLINE goes true and is applied to on-line lamp driver Q18/Q19. The lamp driver output, ONLINLT, goes low and provides a return for the ON LINE indicator on control panel A5. The ON LINE indicator lights.

4-68 Drum Gate (Open). When drum gate is open or improperly latched, interlock switch A2S1 is deactivated. Signal DGINT goes low when the printer is energized, and the r-c time delay is discharged. The output of operational amplifier Z1 goes low and signal PSEQ goes high. Master clear is enabled, and zone control, hammer drivers, and lamp drivers are disabled, as described in paragraphs 4-63 and 4-64. DGINT also provides a return for the DRUM GATE indicator on power supply A4 maintenance panel, and it lights at this time. The printer remains in a disabled state until the drum gate is closed and latched.

4-69 Paper Out. Paper out switches A2S4 and A2S5 (figure 1-11) are activated when print paper is properly installed.

4-70 If paper tears between the tractors and hammer bank, top switch A2S4 deactivates and signal POSW goes high.

4-71 POSW is applied to paper fault lamp driver Q9/Q10, off-line enable logic and paper out fault enable logic. The lamp driver output, POLIGHT, goes low and provides a return for the PAPER FAULT indicator on power supply A4 maintenance panel. The PAPER FAULT indicator lights. On completion of the zone print cycle, signal ONLINE goes false and ONLINE\* goes true. Signal POFAULT then goes false and is applied to OR gate 1.

4-72 When POFAULT goes false, signal FAULT goes true, enabling master clear, and as previously described, 12 VINT goes low, disabling hammer drivers and ready and on-line lamp drivers.

4-73 If the paper supply is exhausted or tears, bottom switch A2S5 deactivates, and POSW goes high. What occurs at this time is as previously described for top switch A2S4.

4-74 VCL and +5V Supplies. The VCL (-4.5v) and +5v supplies are monitored by a voltage monitor consisting of Q7 and Q8.

4-75 When both supplies are normal, Q7 turns on and its output goes low. The output of Q7 added to VCL cuts off Q8, causing the voltage monitor output to go high.

4-76 If the +5v supply drops, Q7 cuts off and its output goes high. The output of Q7 is sufficient to overcome VCL and turn on Q8. The voltage monitor output goes low and is applied to OR gate 1.

4-77 When the voltage monitor output goes low, signal FAULT goes true enabling master clear, and as previously described, 12VINT goes low, disabling hammer drivers, and ready and on-line lamp drivers.

4-78 If the VCL supply drops, it effectively goes positive and in so doing turns on Q8. The voltage monitor output goes low and the result is as described in paragraph 4-77.

4-79 VCL Regulator. The VCL regulator contains a controlled series regulator, and a current monitor to protect the VCL supply. VCL provides the hammer driver current control and is derived from -12v.

4-80 The VCL series regulator control consists of differential amplifier Z2 and driver Q11. Regulator diode VR2 references the noninverting input of Z2 and the output of series regulator Q14, Q15, is fed back to the inverting input of Z2 as a reference signal. A change in the VCL reference signal causes the differential amplifier to develop an output signal proportional to the difference between the VCL reference signal and the reference voltage provided by VR2. This signal is applied through driver Q11 to the regulator, and regulates the VCL output by controlling the current through the series regulator. As the regulator output returns to the desired level, the difference input is nulled out. The feedback loop ensures that a change in the VCL output is reflected in a counteracting change in the control signal.

4-81 The VCL supply is protected against an overcurrent condition by current monitor Q13 and thyristor (SCR) Q12. An overcurrent condition turns Q13 on and its output triggers Q12. Q12 shorts the VCL drive current to -12v and the VCL output drops to zero.

4-82 Print Inhibit. Switch S1 (PRINT INHIBIT) on power supply A4 maintenance panel enables the printer operator to manually disable zone control, hammer drivers, ready and on-line lamp drivers. When switch S1 is activated, signal HISW goes low

and is applied to OR gate 2. As previously described, 12VINT goes low, and printer operation is inhibited. HISW also provides a return for the PRINT INHIBIT indicator on power supply A4 maintenance panel, and it lights at this time. The +12V monitor (A3TB1 figure 6-30) also drops HISW and initiates the print inhibit sequence in the event the +12V supply drops to approximately 8V.

#### 4-83 PRINTER STATES

4-84 During operation, the printer sequences through the following states:

- a. Master clear
- b. Load data
- c. Scan and print
- d. Paper advance or zone change

4-85 Clocks and other necessary timing signals for printer operation are generated within the printer.

4-86 In the paragraphs that follow, a figure reference is given if the logic functions being described are contained on the same card type. When the logic functions described are contained on more than one card type, each logic reference designation is then prefixed with the designation of the card type that contains it. The card type reference designations and their figure numbers are as follows:

<u>Reference Designator</u>	<u>Figure Number</u>
A2	6-7
A3	6-8
A4	6-9
A5	6-10
A6	6-11
A9	6-28
A15	6-14
A18 thru A22	6-27

#### 4-87 Clock Generation (See figure 6-11)

4-88 The printer clock signals are 1 mHz and 2 mHz, derived from a 2 mHz oscillator. The oscillator output is inverted by Z2A and used to clock flip-flop 1CLK. It also undergoes two more inversions, by Z2D and Z2B, to produce the 2 mHz clock signal, 2CLK.

4-89 Since the flip-flop inputs are tied together and always true, the flip-flop toggles continuously on each fall of its clock input and divides down by 1/2 to produce the 1 mHz clock signal, 1CLK. The 1CLK\* output is fed to a fan-out consisting of inverters Z1A thru Z1D, to produce clock signals 1CLK1 thru 1CLK4.

4-90 In the description of operating states that follow, it is understood that all flip-flops toggle on the fall of the clock. Clock signals 1CLK, and 1CLK1 thru 1CLK4, can be considered as one clock signal, and unless otherwise indicated, toggle all flip-flops.

4-91 Master Clear State

4-92 In the master clear state, all registers, mode flip-flops, and time slot decode flip-flops are cleared and on termination of the master clear state, a ready condition is indicated. See figure 4-13 for a flow and timing diagram of the master clear state.

4-93 MASTER CLEAR OPERATION (See figure 6-11). The master clear operation is initiated under the following conditions:

- a. Power applied to printer
- b. Fault condition occurs
- c. Manual input from MASTER CLEAR switch

4-94 Power On. Assuming paper is loaded, drum gate closed, and printer ready for normal operation, signal PSEQ goes high when the printer is energized, and is applied through the drum speed monitor logic to NOR gate Z11C. Output MCA\* goes low and presets flip-flop MC1F, and output MC1F goes true. MC1F is applied to the set input of flip-flop MC2F and a fan-out consisting of inverters Z5A thru Z5D. The inverter outputs, MC1\* thru MC4\* go false, and together with MC1F\* provide the clear inputs to registers and flip-flops. MC1F also enables Nor Gate A4Z 16A, and MLPD\* goes low, raising set input LDFF(J) to flip-flop A5Z2A LDFF.

4-95 If drum is up to speed, PSEQ from the drum speed monitor goes low after 10 seconds and MCA\* goes high, allowing flip-flops MC1F and MC2F to come under clock control.

4-96 On the next clock, flip-flop MC2F sets. Output MC2F goes true and is applied to the set input of flip-flop RDY and the reset input of flip-flop MC1F. Output MC2F\*, now false, presets flip-flop DLFF.

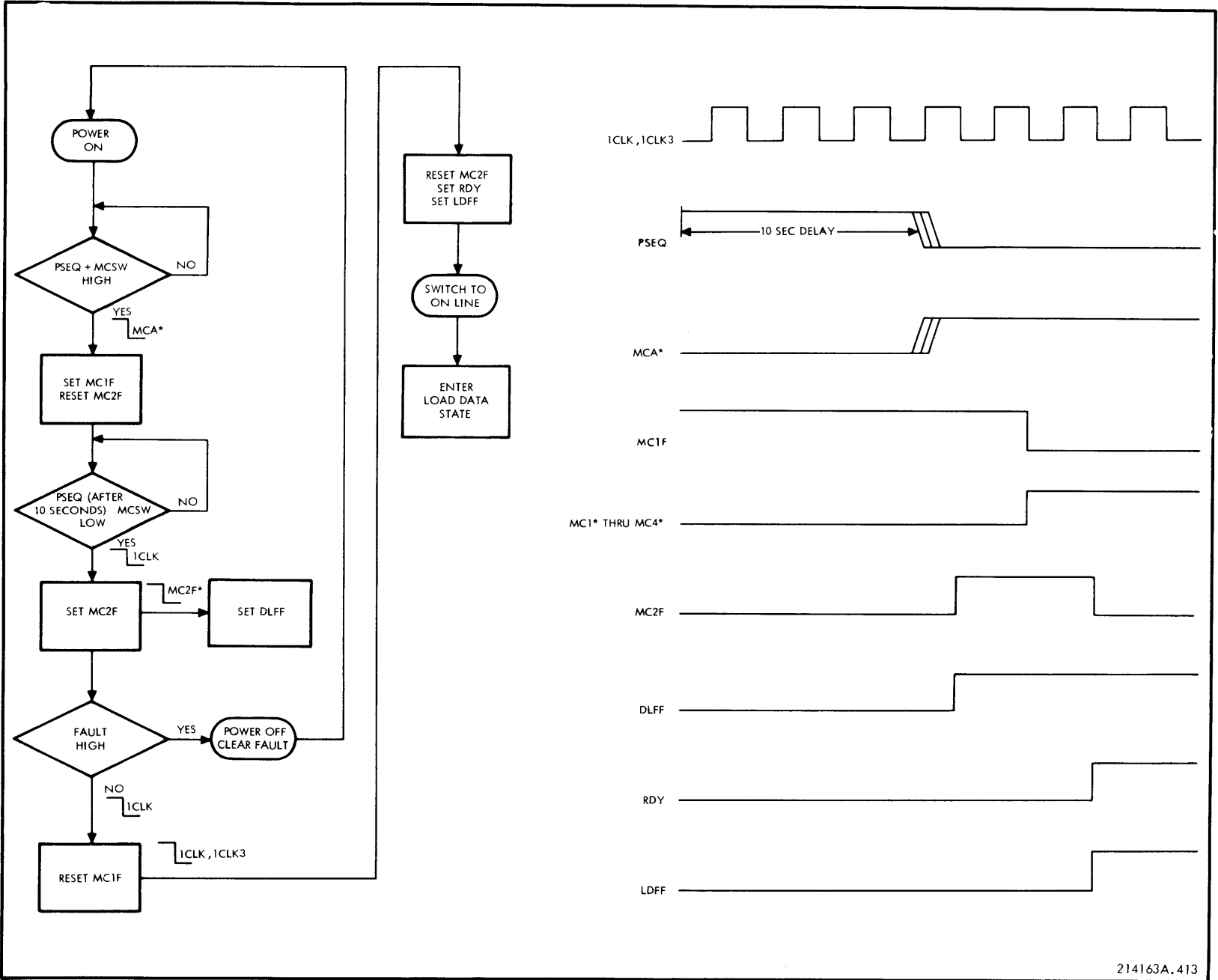
4-97 On the next clock, if a fault condition does not exist at this time, flip-flop MC1F resets and MC1F goes false. MC1F\* and MC1\* thru MC4\* go true, allowing the registers and flip-flops to come under clock control.

4-98 On the next clock, flip-flop MC2F resets and flip-flops LDFF and RDY set. Output RDY, which held flip-flop ONLINE clear, goes true and as previously described (paragraph 4-66), is applied to a lamp driver (see figure 6-15) and the READY indicator lights. RDY is also applied to an interface driver (see figure 6-12), and signal READY is transmitted to the user system to indicate the operational readiness of the printer. The printer is now switched manually to on-line operation.

4-99 If during printer operation the paper supply tears or is exhausted, or a fault occurs in the +5v or VCL supplies, signal FAULT goes high and a master clear sequence is initiated.

4-100 FAULT is applied to the set input of flip-flop MC1F and on the next clock, flip-flop MC1F sets. Output MC1F goes true and is applied to the set input of flip-flop MC2F. Clear signals MC1F\* and MC1\* thru MC4\* go false. The registers and flip-flops are cleared and the READY and ONLINE indicators go out.

Figure 4-13. Master Clear State (Power on Sequence) Flow and Timing Diagram



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4-101 On the next clock, flip-flop MC2F is set and output MC2F goes true.

4-102 If the fault condition is due to paper out, it is necessary to open the drum gate to replace paper. Upon closing the drum gate, the master clear operation again goes through a power-on sequence.

4-103 If the fault condition is due to other than paper out and can be corrected without opening the drum gate or removing power, then on the clock following the time FAULT goes low, flip-flop MC1F resets, and the master clear operation is then as described in paragraphs 4-96 and 4-97. If it is necessary to remove power to clear the fault, then the master clear operation is a power-on sequence when power is again applied.

4-104 Drum Speed Monitor (Figure 6-28). When the printer is turned on, the 10-second delay starts and PSEQ goes high. PSEQ is inverted by Z6E, and the output of NAND gate Z3A then goes high, applying PSEQ to the master clear logic as previously described. The output of Z3A is crosscoupled to NAND gate Z2B. Since the CARRY output of up/down counter Z8 is initially high, gate Z2B is enabled and PSEQ is latched. During the 10-second delay period, the following sequence repeats over and over as the drum comes up to speed. As signal RDY is initially low, single-shot Z7 triggers the first time index signal CIND goes high after power is applied. Output Z7Q\* goes low, removing the clear input from counter Z8, and remains low for 10 milliseconds. As the drum revolves, counter Z8 advances one count for each character clock (CHCK4) generated. If the counter advances 15 counts in 10 milliseconds, output CARRY goes low, disabling gate Z2B and removing the latch from PSEQ. At the end of 10 milliseconds, single-shot Z7 resets. The counter is cleared and output CARRY again goes high. On the next CIND pulse, single-shot Z7 triggers again and the counter sequence repeats. At the end of 10 seconds, the output of inverter Z6E goes high. If the drum is up to speed, the counter has advanced 15 counts in 10 milliseconds, CARRY is low, disabling the latch and PSEQ goes low, disabling the master clear logic. If the drum is not up to speed, CARRY is still high when single-shot Z7 resets and PSEQ is still latched, keeping the printer in the master clear state. The counter sequence continues to repeat until the drum reaches proper speed and PSEQ is unlatched.

4-105 Manual Input. During printer operation a master clear sequence can be initiated at any time by pressing switch MASTER CLEAR on power supply A4. When this is done, signal MC goes high and is applied to NOR gate Z11C. Output MCA\* goes low and presets flip-flop MC1F and clears flip-flop MC2F. The registers and flip-flops are cleared and READY and ONLINE indicators go out.

4-106 The printer remains in the master clear state as long as MASTER CLEAR switch is pressed. When the switch is released, MC goes low, MCA\* goes high, and the master clear operation is then as described in paragraphs 4-95 thru 4-97. The READY indicator lights and the printer can be switched to on-line operation.

4-107 Load Data State

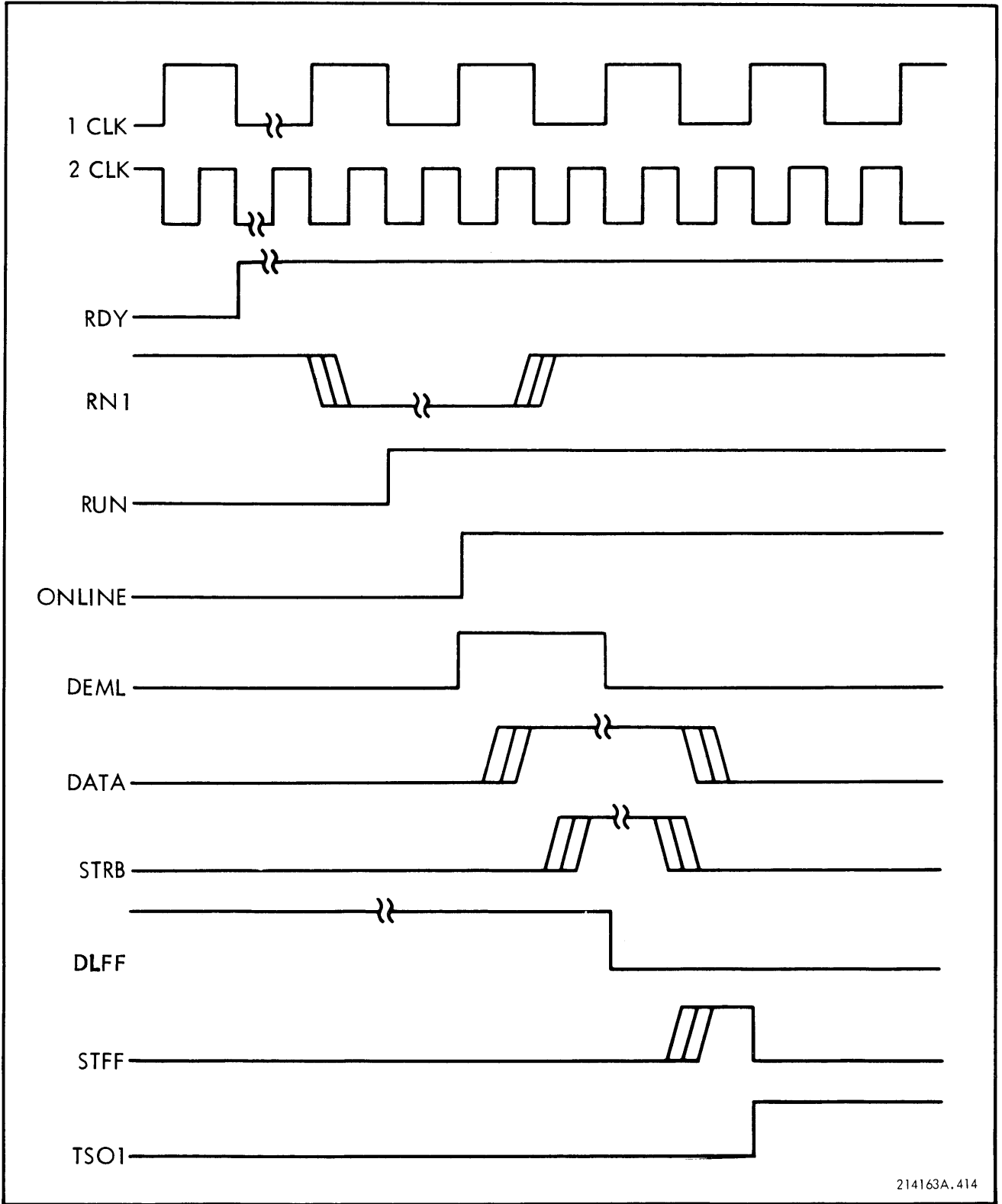
4-108 After leaving the master clear state, the printer cannot enter the load data state until it is manually switched to on-line operation. This initiates the on-line enable and interface timing and the printer enters the load data state. See figure 4-14 for an on-line enable and interface timing diagram, and figures 4-15 thru 4-17 for flow and timing diagrams of the load data state.

4-109 In the load data state, the incoming data is sampled one character at a time, and if printable, stored in memory. The data can consist of 20 printable characters, less than 20 printable characters and a control character, or a control character only. A maximum of 20 characters can be received and stored in memory, and on receipt of the 20th character or a control character, the printer enters the scan and print state.

4-110 ON-LINE ENABLE. When the ON LINE/OFF LINE switch is set to ON LINE, signal RN1 momentarily goes low, is inverted by Z8A (figure 6-11), and applied to the set input of flip-flop RUN.

4-111 On the next clock flip-flop RUN sets, and output RUN goes true and is applied to the set input of flip-flop ONLINE (figure 6-10).

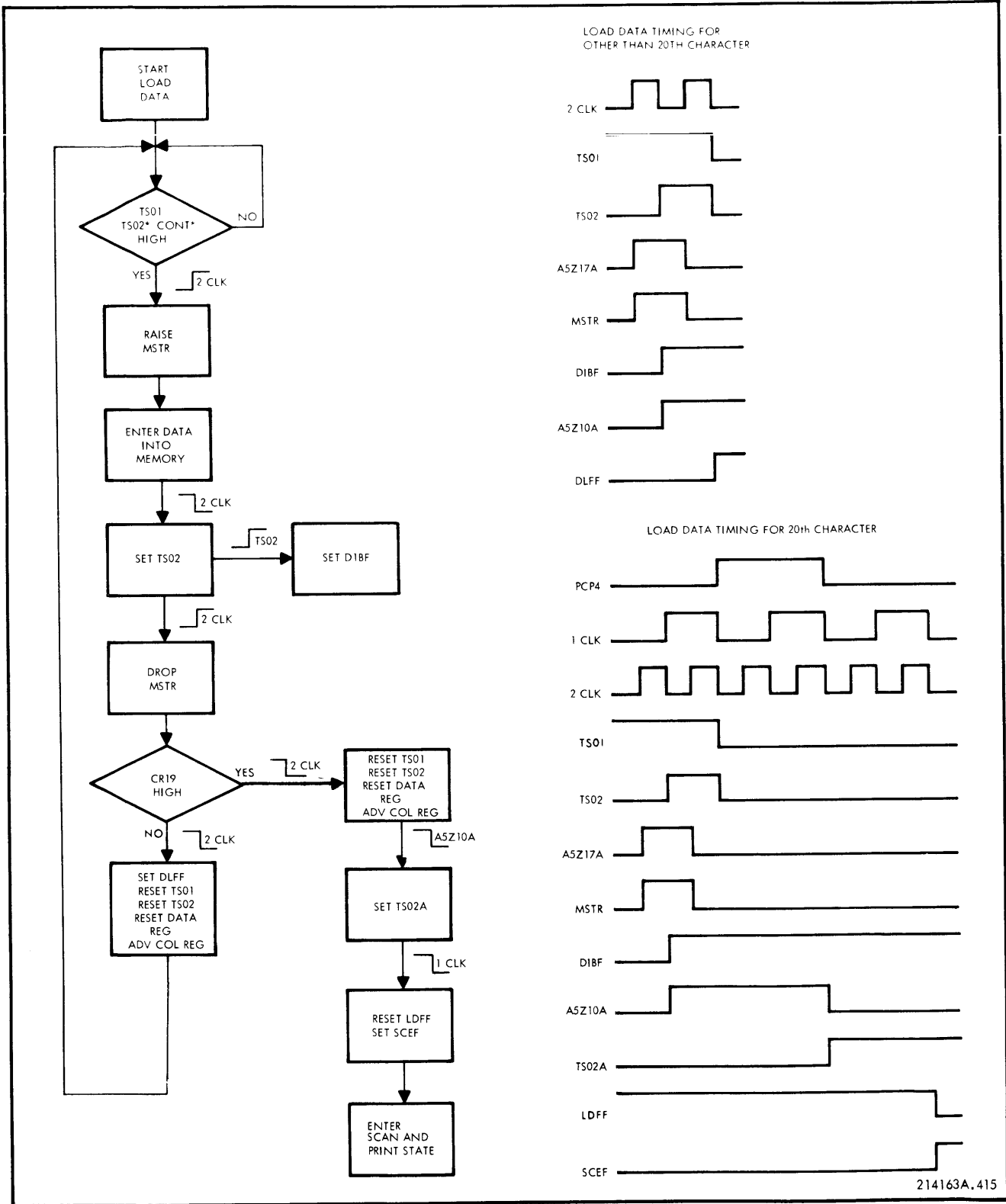
4-112 On the next clock (2CLK), flip-flop ONLINE sets and output ONLINE goes true. ONLINE is applied to a lamp driver (figure 6-15), and the ONLINE indicator lights.



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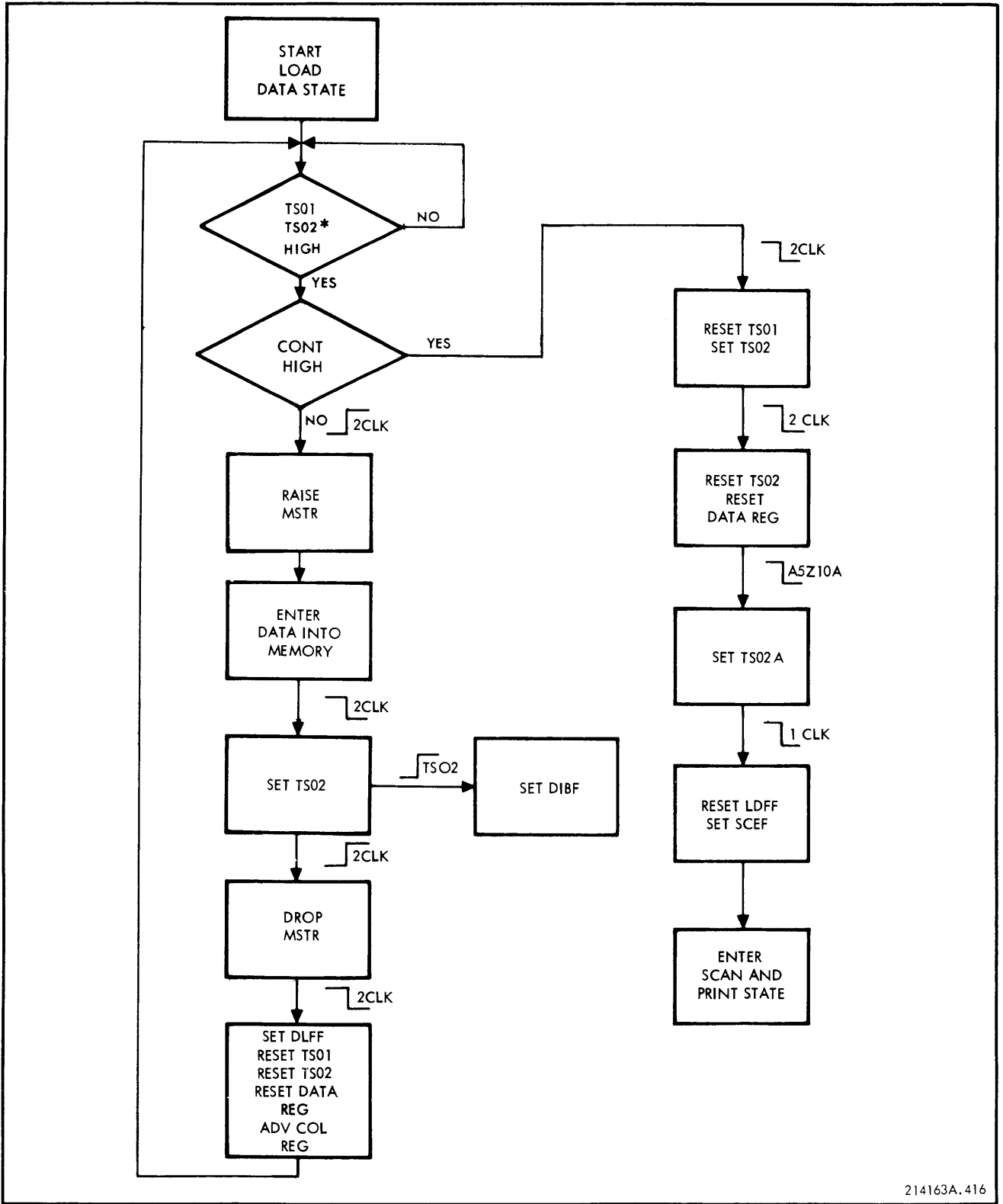
Figure 4-14. On-Line Enable and Interface Timing Diagram





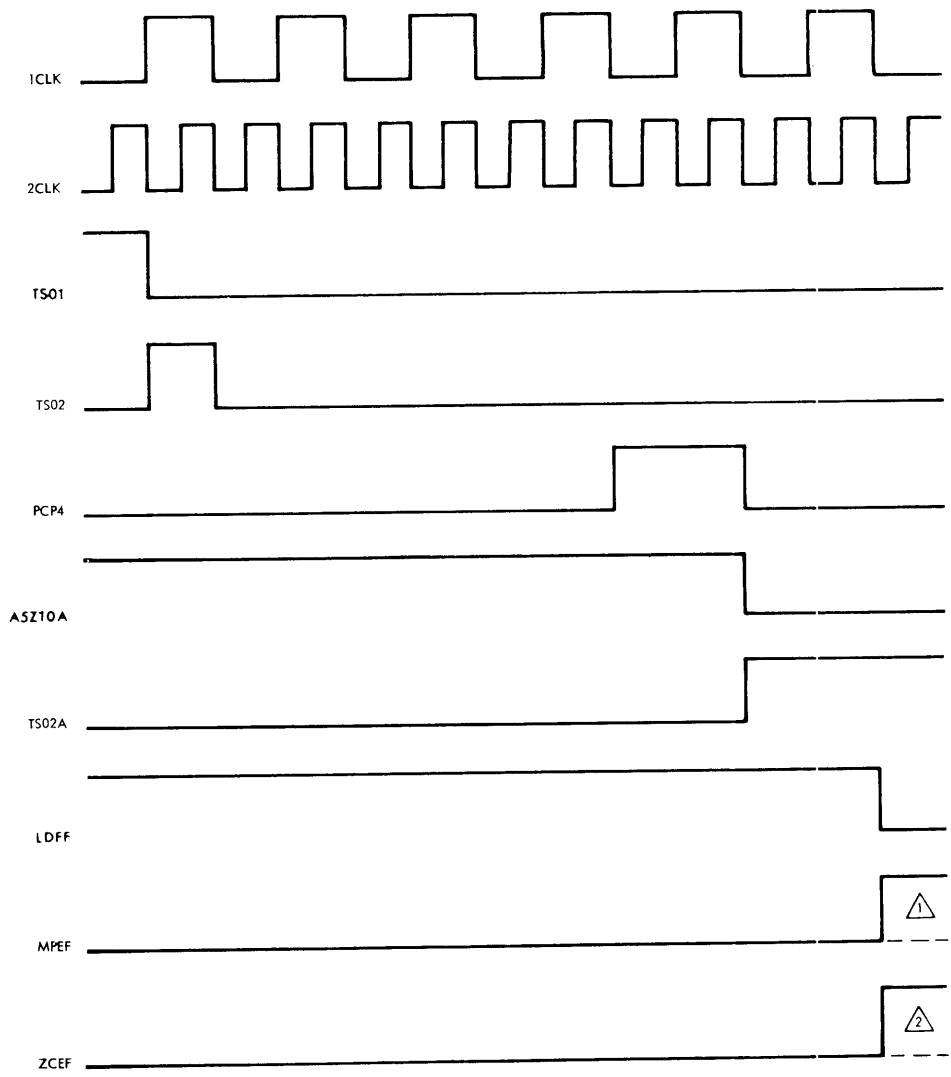
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Figure 4-15. Load Data State (20 Printable Characters) Flow and Timing Diagram



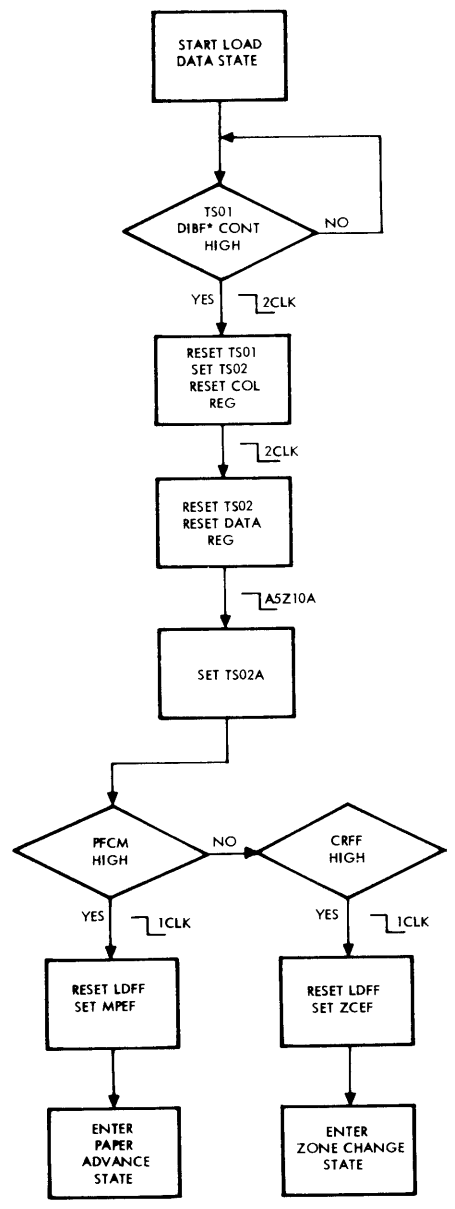
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Figure 4-16. Load Data State (Less Than 20 Printable Characters and Control Character) Flow Diagram



NOTES: DASHED LINE --- INDICATES STATE WITH CRFF HIGH.  
 DASHED LINE --- INDICATES STATE WITH PFCM HIGH.

Figure 4-17. Load Data State (Control Character Only) Flow and Timing Diagram



4-113 INTERFACE TIMING. The printer raises signal READY to indicate operational readiness, and requests data by raising signal DEMAND LINE.

4-114 Signal ONLINE\*, now false, is applied to NOR gate Z11A (see figure 6-11) and since DLFF\* had previously gone false, gate output DEML goes true. DEML is applied to the set input of flip-flop STFF and an interface driver (see figure 6-12). DEMAND LINE goes high and is transmitted to the user system as a request for data.

4-115 The user system transmits data to the printer over data lines DATA1 thru DATA7. Data can be one character or a series of 20 characters, each consisting of seven bits, as previously described in paragraph 4-15. Each character is followed by a DATA STROBE signal and both are interfaced to the printer logic through interface receivers (see figure 6-13).

4-116 Receiver outputs REC1 thru REC7 are applied to format control logic and data register NAND gates Z6C, Z9D, Z9C, Z16C, Z16D, Z13C, and Z12D, respectively (see figure 6-8). Receiver output STRB is a common enable input for the above NAND gates, and the format control decode gates. It is also the clock for flip-flop STFF and the reset input for flip-flop DLFF.

4-117 Assuming a transmitted character is the letter 0, the code on the data lines is as follows:

```
DATA1 = 1 (LSB)
DATA2 = 1
DATA3 = 1
DATA4 = 1
DATA5 = 0
DATA6 = 0
DATA7 = 1
```

4-118 On receiving the character code for 0, receiver outputs REC1, REC2, REC3, REC4, and REC7 go high. Signal DATA STROBE then follows and receiver output STRB goes high, enabling gates Z6C, Z9D, Z9C, Z16C, and Z12D. The gate outputs go low and preset flip-flops DR01, DR02, DR03, DR04, and DR07. Since receiver outputs REC5 and REC6 remain low, gates Z16D and Z13C are not enabled and flip-flops DR05 and DR06 remain in a clear state. The data register now contains the character code for the letter 0 as follows:

```
DR01 = 1 (LSB)
DR02 = 1
DR03 = 1
DR04 = 1
DR05 = 0
DR06 = 0
DR07 = 1
```

4-119 On the first clock (2CLK) after STRB goes high, flip-flop DLFF resets and output DLFF\* goes true, disabling gate Z11A. DEML goes false and DEMAND LINE is dropped.

4-120 When DATA STROBE drops, STRB goes low and flip-flop STFF sets. Output STFF goes true and is applied to the set input of flip-flop TS01.

4-121 On the next clock (2CLK), flip-flop TS01 sets and a load data operation begins.

4-122 LOAD DATA OPERATION. A load data operation is initiated for each of the following conditions:

- a. Data consists of 20 printable characters
- b. Data consists of less than 20 printable characters and a control character
- c. Data consists of control character only

4-123 The following paragraphs describe the three types of load data operations.

4-124 Twenty Printable Characters. Flip-flops A6Z14A (TS01) and A6Z14B (TS02) provide timing signals for all load data operations. When flip-flop TS01 sets, output TS01 goes true enabling NAND gate A6Z16B, as input TS02\* is also true. The gate output goes low, clears flip-flop A6Z15A (STFF), and output STFF goes false. TS01 is also applied to NAND gates A6Z9B and A5Z4B.

4-125 The inputs to gate A5Z4B are TS02\*, CONT\*, TS01, and 2CLK. TS02\* is true, CONT\* is true, as we have not received a control character, and TS01 is now true. On the rise of the first clock (2CLK) after TS01 goes true, the gate output goes low and presets flip-flop A5Z17A. The Q\* output of flip-flop A5Z17A goes low, is applied to NAND gate A5Z16B, and strobe signal MSTR goes high. MSTR is applied to the memory clock drivers (figure 6-6) and data register outputs DR01 thru DR07 are inverted and entered into memory.

4-126 The memory consists of seven serial-in/serial-out shift registers, one for each character bit held in the data register. The registers require a 2-phase clock for each shift operation. When MSTR goes high, phase 1 clock goes low and phase 2 clock goes high. At this time the character 0, represented by DR01 thru DR07, transfers from the data register to memory. Each character bit is entered into the highest order bit location of its corresponding register. Data previously stored in these locations is shifted into the next location, and so forth. The data entry and internal shift sequence is completed during the time MSTR is high.

4-127 On the fall of the first clock (2CLK) after TS01 goes true, flip-flop TS02 sets. Output TS02 goes true and is applied to NAND gates A6Z9B, A5Z11D, A5Z16C, and A3Z4B. TS02 enables gates A6Z9B, A5Z11D, and A3Z4B.

4-128 The output of A5Z11D goes low, presets flip-flop A5Z17B (DIBF), and output DIBF goes true.

- 4-129 TS02 enables gate A6Z9B, since inputs TS01 and CR19\* are also true. CR19\* is true because the column register is not at count 19. The gate output goes low and is applied to NAND gate A6Z9C. The output of A6Z9C goes high and is applied to the set input of flip-flop A6Z15B (DLFF).
- 4-130 The output of gate A3Z4B goes low, is applied to NAND gate A3Z5A, and clock signal ADVC goes high. ADVC is the clock for column register flip-flops A3Z3A (CR00), A3Z3B (CR01), A3Z1B (CR02), A3Z1A (CR03), and A3Z10A (CR04). CR24\*, the set input to flip-flop CR00 is true at this time since the column register is not at count 24. Flip-flop CR00 holds the least significant bit.
- 4-131 TS02\*, now false, enables NAND gates A6Z2C, and A3Z6A, and presets flip-flop A5Z10A. Output Q of flip-flop A5Z10A goes true and is applied to the clock input of flip-flop A5Z10B (TS02A). The output of A6Z2C goes high and is applied to the reset input of flip-flop TS01. The output of A3Z6A goes high, is applied to NOR gate A3Z18B, whose output goes low and is applied to NOR gate A3Z18A.
- 4-132 The rise of the next clock (2CLK) enables gates A5Z16C and A3Z18A. The output of A5Z16C goes low, clears flip-flop A5Z17A and MSTR drops. The output of inverter A3Z13A goes low on the rise of the clock, enabling A3Z18A, and signal CLK goes high. CLK is the clock for the data register flip-flops. Since signal SHFT\* is high at this time, the outputs of inverters A3Z14C, A3Z7D, A3Z16B, A3Z16A, A3Z7A, A3Z12B, and A3Z12A are high and applied to the reset inputs of the data register flip-flops. On the fall of the clock (2CLK), the clear input to flip-flop A5Z17A is disabled, and data register flip-flops DR01, DR02, DR03, DR04, and DR07, which had previously set on receipt of character 0, reset. Flip-flop DLFF sets, and flip-flops TS01 and TS02 reset. When flip-flop TS02 resets, output TS02 goes false and ADVC drops, clocking flip-flop CR00. Output CR00 goes true, and the column register count at this time is 00001, indicating one character stored in memory. DEML is again high and DEMAND LINE is raised. The user system then transmits another character code and the operation described in the preceding paragraphs is repeated until the 20th character is received. During this time, the column register advances one count for each character stored in memory.
- 4-133 After the 19th character has been received and stored, the column register count is as follows:
- CR00 = 1 (LSB)  
 CR01 = 1  
 CR02 = 0  
 CR03 = 0  
 CR04 = 1
- 4-134 Since the column register outputs CR00\* and CR01\* are false, the output of NOR gate A3Z14A goes true and is applied to the set and reset inputs of flip-flop A3Z1B (CR02) and NAND gates A3Z2A and A3Z4D. Both inputs to gate A3Z4D are now true and CR19\* goes low. CR19\* is inverted by A5Z16D, and CR19 is applied to NOR gate A5Z9B. The gate output goes low and is applied to NOR gate A5Z9A.
- 4-135 When the load data operation for the 20th character is completed, the data register and flip-flops TS01 and TS02 reset. When TS02 resets, the column register advances one count to 10100 (20).

4-136 On the first concurring PCP4 and clock time after TS02\* goes true, flip-flop A5Z10A resets and output Q goes false. As it goes false it clocks and sets flip-flop A5Z10B (TS02A). Output TS02A\* goes false and enables NOR gate A5Z9A. The gate output goes high and is applied to the reset input of flip-flop A5Z2A (LDFF). Output TS02A goes true and enables NAND gate A5Z8C as inputs CR02 and CR04 previously went true when the column register count reached 20. The gate output goes low and is applied to NAND gate A5Z8B. The output of this gate goes high and is applied to the set input of flip-flop A5Z2B (SCEF).

4-137 On the next clock, flip-flop LDFF resets and flip-flop SCEF sets. The printer now enters the scan and print state.

4-138 Less Than 20 Printable Characters and Control Character. For less than 20 printable characters and a control character, the load data operation is as previously described, until receipt of a control character.

4-139 On receipt of a control character, CONT\* goes low, and the reset input to flip-flop TS01 goes high.

4-140 On the next clock (2CLK) flip-flop TS01 resets, and flip-flop TS02 sets. On the following clock (2CLK) flip-flop TS02 and the data register are reset.

4-141 As previously described, flip-flop TS02A is clocked and set on the first concurring PCP4 and clock time after TS02\* goes true. NOR gate A5Z9A is enabled and the reset input to flip-flop LDFF goes high.

4-142 TS02A\* is now low and applied to NAND gate A5Z7C. Gate output SPSE goes high and enables NAND gate A5Z8A. The gate output goes low and is applied to NAND gate A5Z8B. The output of this gate goes high and is applied to the set input of flip-flop SCEF.

4-143 On the next clock, flip-flop LDFF resets and flip-flop SCEF sets. The printer now enters the scan and print state.

4-144 Control Character Only. The user system transmits the control character, and the printer format control decodes determine if it is a PF, FF, or CR command.

4-145 As previously described, all received characters are simultaneously applied to the data register and the format control logic (figure 6-9). Receiver outputs REC1 thru REC7 are applied to format control receivers Z5C, Z11D, Z11B, Z5A, Z11C, Z5D, and Z11A, respectively. The outputs of these receivers are REC1\* thru REC7\*, and a combination of these and the REC1 thru REC7 signals are applied to format control decodes Z1 (PF), Z2 (FF), and Z3 (CR). The output of each decode goes low only when its respective control character code is received.

4-146 PF Command (See figure 6-9). If the transmitted control character is a PF command, the input to the format control receivers is as follows:

REC1 = 0

REC2 = 1

REC3 = 0

REC4 = 1

REC5 = 0

REC6 = 0

REC7 = 0

4-147 The REC1 thru REC7 signals are inverted and the input to decode Z1 is as follows:

REC1\* = 1

REC2 = 1

REC3\* = 1

REC4 = 1

REC5\* = 1

REC6\* = 1

REC7\* = 1

4-148 On receipt of DATA STROBE, STRB goes high and enables Z1. Decodes Z2 and Z3 remain disabled when Z1 is enabled since the inputs to neither one are all true at this time. The output of Z1 goes low and presets flip-flop LFFF. Output LFFF\* goes false and is applied to NAND gate Z12B. Gate output PFCM goes high, and is applied to NAND gate Z19A and NOR gate Z17D. CONT\* goes low and disables the pre-set input to flip-flop DIBF. CONT\* is inverted by Z13B and CONT is applied to NOR gate A5Z9B.

+149 On the next clock (2CLK) after CONT\* goes low, flip-flop TS01 resets, and flip-flop TS02 sets. Since DIBF\* is true, NAND gate A3Z5B is enabled, and the gate output goes low. It is applied to NAND gate A3Z5C, whose output goes high and is inverted by A3Z6D. Signal CRRS\* goes low and clears column register flip-flops CR00 thru CR04.

4-150 On the following clock (2CLK) flip-flop TS02 and the data register are reset.

4-151 Flip-flop TS02A sets on the first concurring PCP4 and clock times after TS02\* goes true, and SPSE and the reset input to flip-flop LDFF both go high.

4-152 With inputs PFCM and DIBF\* already true, SPSE enables NAND gate A4Z19A. The gate output goes low, is applied to NAND gate A4Z14A, and the set input to flip-flop A4Z9A (MPEF) goes high.

4-153 On the next clock, flip-flop LDFF resets and flip-flop MPEF sets. The printer now enters the paper advance state.

4-154 FF Command (see figure 6-9). If the transmitted control character is a FF command, decode Z2 is enabled by STRB and decodes Z1 and Z3 remain disabled. The output of Z2 goes low, presets flip-flop FFFF, and output FFFF\* goes false.



FFFF\* is applied to NAND gate Z12B, and PFCM goes high. The operation that follows is as previously described for a PF command.

4-155 CR Command (see figure 6-9). If the transmitted control character is a CR command, decode Z3 is enabled by STRB and decodes Z1 and Z2 remain disabled. The output of Z3 goes low, presets flip-flop CRFF and output CRFF goes true. CRFF is applied to NAND gate Z19B. It is also supplied to NOR gate Z17D and CONT\* goes low.

4-156 On the next clock (2CLK), flip-flop TS01 resets, flip-flop TS02 sets, CRRS\* goes low, and the column register is cleared.

4-157 On the following clock (2CLK), flip-flop TS02 and the data register are reset.

4-158 Flip-flop TS02A sets on the first concurring PCP4 and clock time after TS02\* goes true. The reset input to flip-flop LDFD goes high and NAND gate Z19B is enabled by TS02A. The gate output goes low, is applied to NAND gate Z5B and the set input to flip-flop ZCEF goes high.

4-159 On the next clock, flip-flop LDFD resets, and flip-flop ZCEF sets. The printer now enters the zone change state.

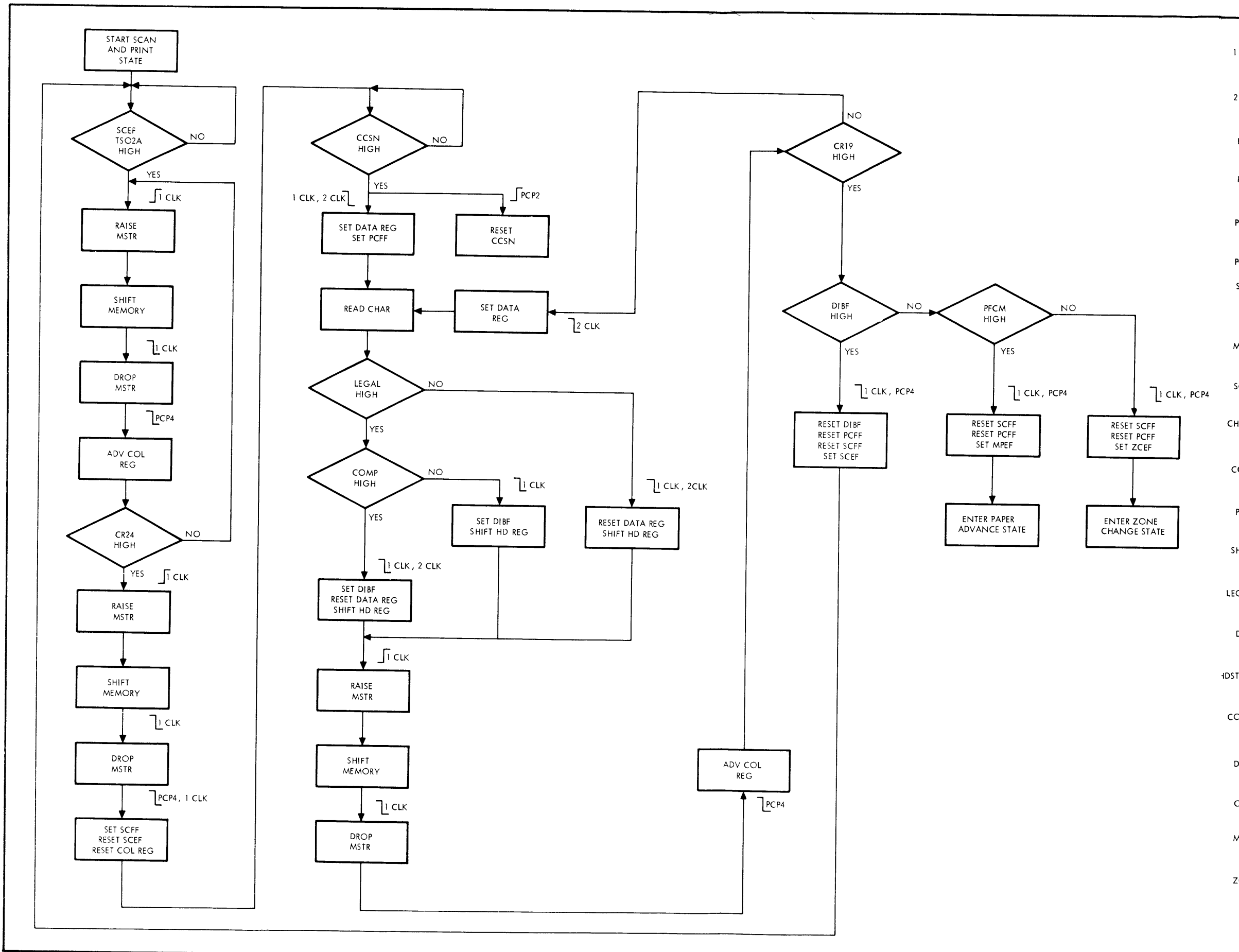
#### 4-160 Scan and Print State

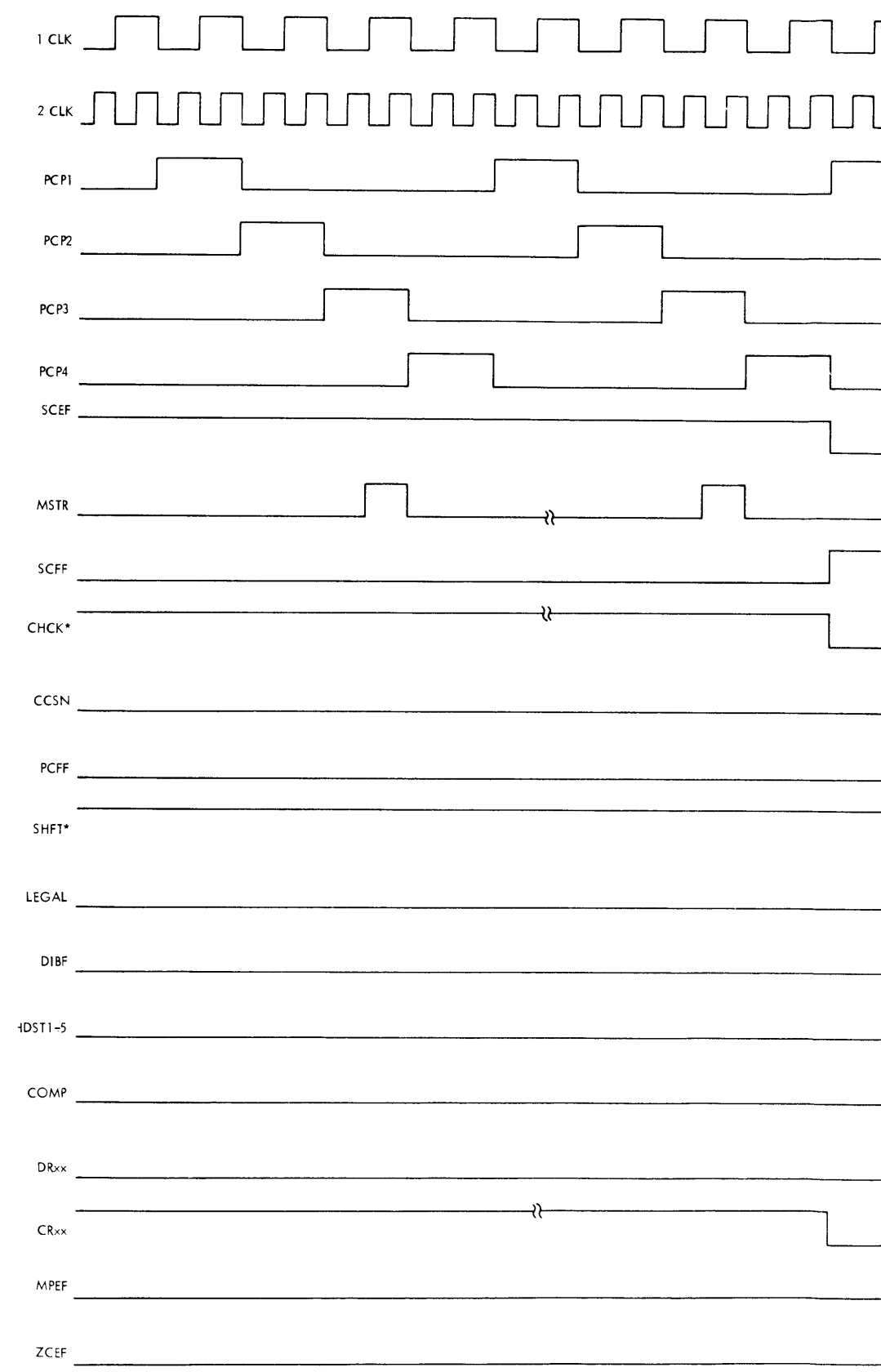
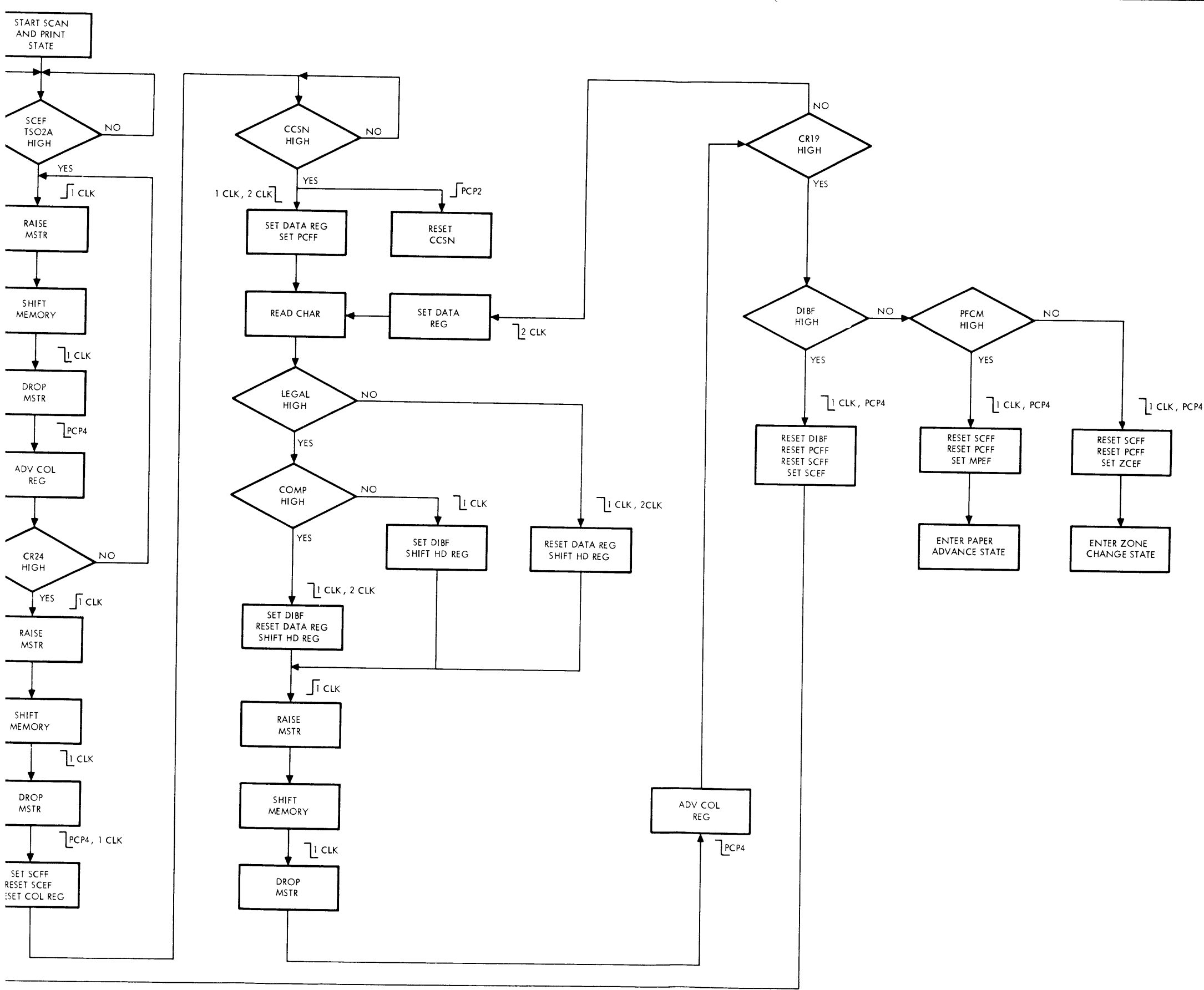
4-161 In the scan and print state, the printer initiates scan cycles in which each character in memory is compared with the current output of the character counter. The character counter output corresponds to the drum character which is adjacent to the print station during the scan cycle. All characters which compare are erased from memory and simultaneously printed prior to the start of the next scan cycle. The sequence is repeated until all characters in memory are compared, erased, and printed. See figure 4-18 for a flow and timing diagram of the scan and print state.

4-162 SCAN AND PRINT OPERATION. Timing for the scan and print operation, as well as for the paper advance and zone change operations, is provided by printer clock pulses (time slot decode) PCP1 thru PCP4 (figure 6-11). The time slot decode pulses are derived from clock pulse 1CLK and continually generated by flip-flops PCT, ODD and EVEN. See figure 4-19 for a timing diagram of the PCP1 through PCP4 generation.

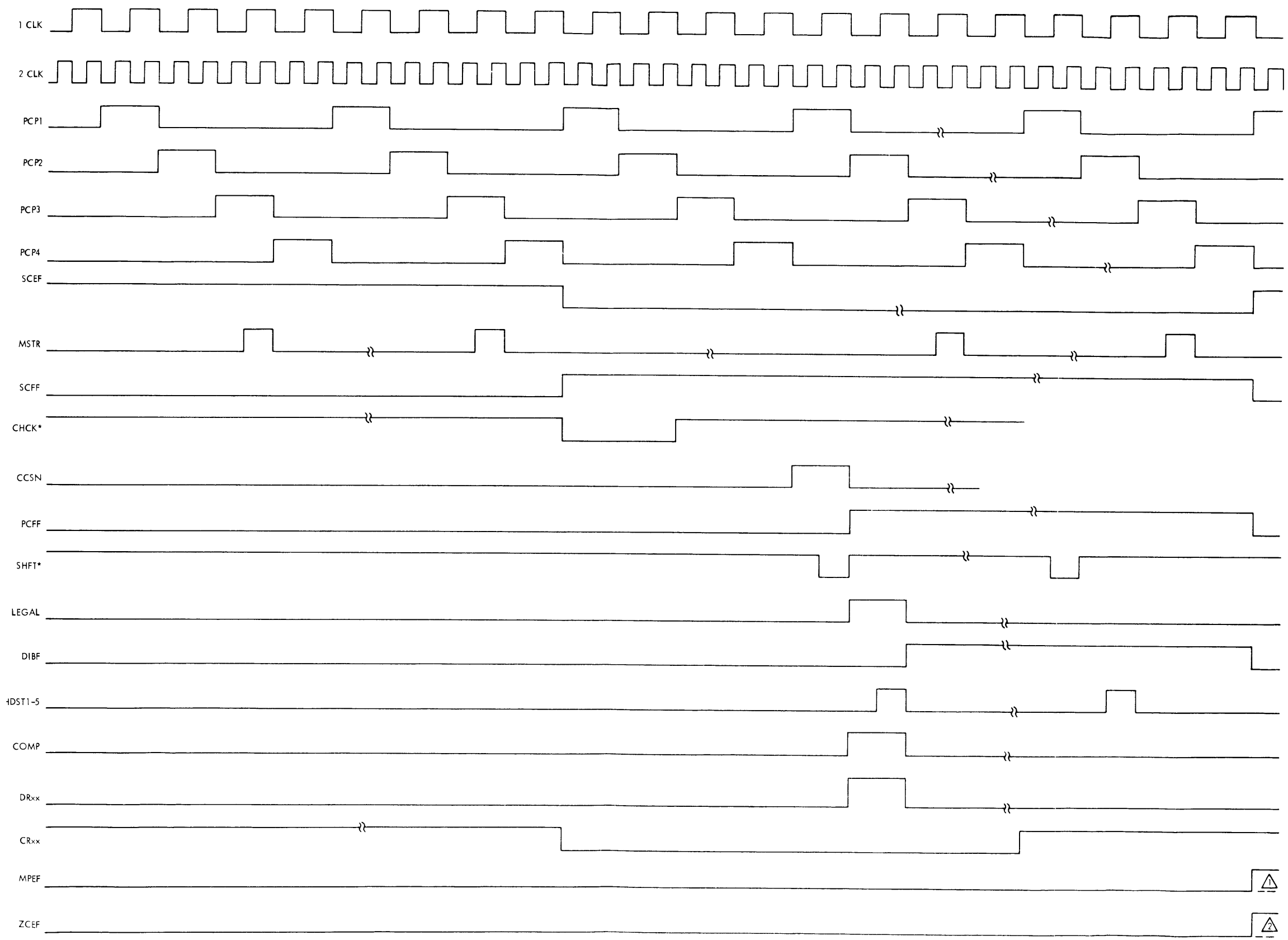
4-163 When flip-flop SCEF sets, the printer enters the scan and print state and the operation starts if SCEF and TS02A remain high.

4-164 Each of the memory shift registers contain 25 or 32 bit locations depending upon printer use of the AM-10 (25 character) or the AM-21 (32 character) memory circuit card (figure 4-20). The first character to be stored in memory enters the highest bit location (25 or 32) and is shifted down one location each time a character is stored. It is necessary that bit location 1 be occupied when the scan and compare operation begins, as the characters are shifted out of memory into the data register and back into memory if a compare does not occur. Since only a maximum of 20 characters can be received and stored, it is obvious that bit location 1 will not be occupied at this time, unless additional shifts are made prior to the start of the scan and compare operation. This is accomplished in the 25 character memory or the 32 character memory in the sequence that follows.





NOTES: DASHED LINE --- INDICATES STATE WITH ZCEF HIGH  
 DASHED LINE --- INDICATES STATE WITH MPEF HIGH



NOTES: DASHED LINE --- INDICATES STATE WITH ZCEF HIGH  
 DASHED LINE --- INDICATES STATE WITH MPEF HIGH

Figure 4-18. Scan and Print State Flow and Timing Diagram

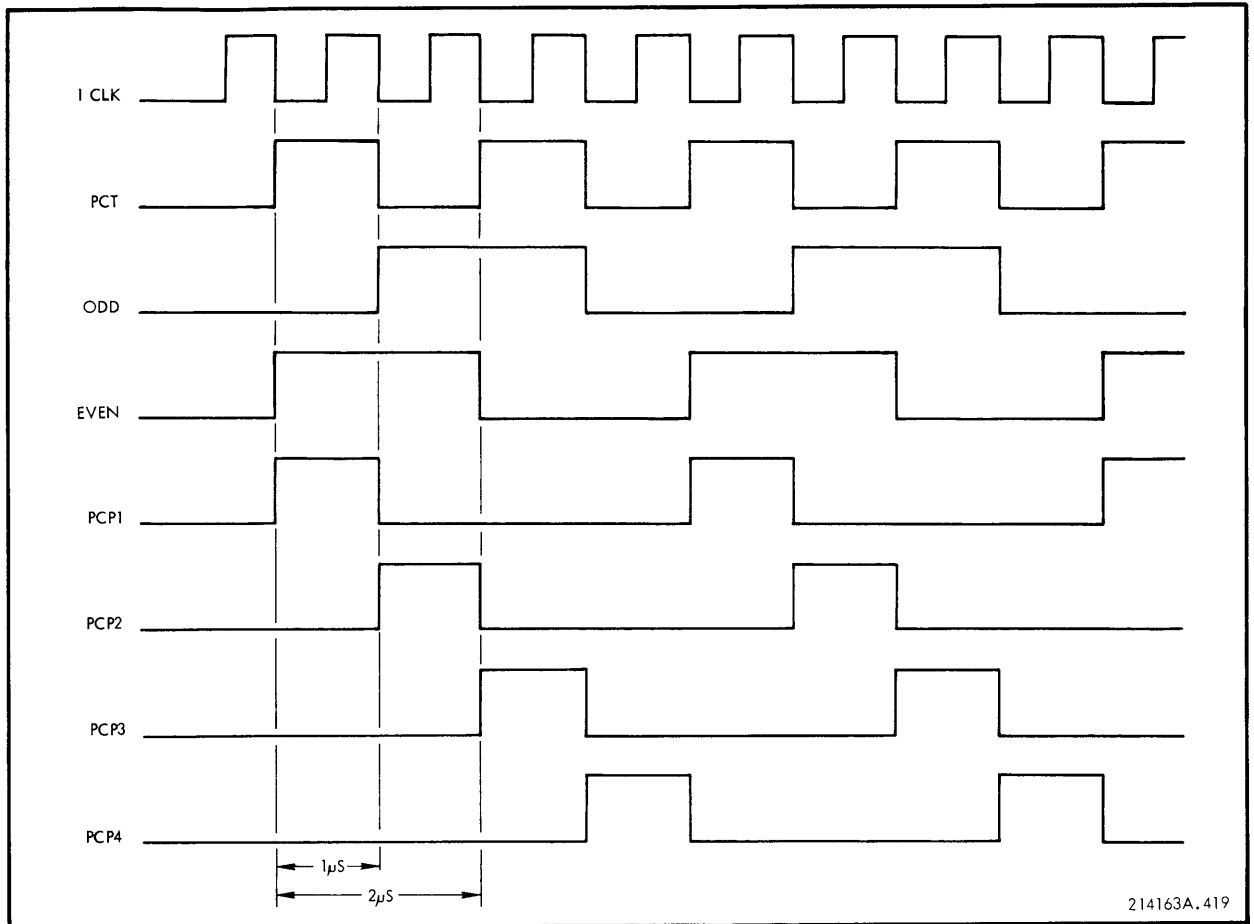


Figure 4-19. Time Slot Decode Timing Diagram

4-165 25-CHARACTER MEMORY (figure 6-6). At PCP3 and clock time, NAND gate A5Z15B (figure 6-10) is enabled, memory strobe MSTR goes high, the data stored in memory shifts one location, and MSTR goes low.

4-166 At PCP4 time NAND gate A3Z4A (figure 6-8) is enabled, raising ADVC, and the column register is clocked and advanced one count when ADVC drops. This sequence is repeated until the column register reaches a count of 24.

4-167 At count 24, flip-flops CR00, CR01, and CR02 are reset and CR03 and CR04 are set, enabling NAND gate A5Z7B. Gate output CR24\* goes low, and CRTC (column register top count) goes high. CR24\* is applied to NAND gates A3Z2B and Z3Z2C. The gate outputs go high and are applied to the set and reset inputs of flip-flops CR03 and CR04. CRTC is applied to the set input of flip-flop A5Z13B (SCFF), inverted by A5Z3C and applied to NOR gate A5Z9C. On the following PCP3 and clock time, the data in memory shifts again and the first character stored in memory is now in bit location 1 (figure 4-20).

4-168 32 CHARACTER MEMORY (figure 6-6a). NAND gate A5Z15B (figure 6-10a) is enabled, memory strobe MSTR goes high, the data stored in memory shifts one location, and MSTR goes low.

4-168a At PCP4 time NAND gate A3Z4A (figure 6-8) is enabled, raising ADVC, and the column register is clocked and advanced one count when ADVC drops. This sequence is repeated until the column register reaches a count of 31.

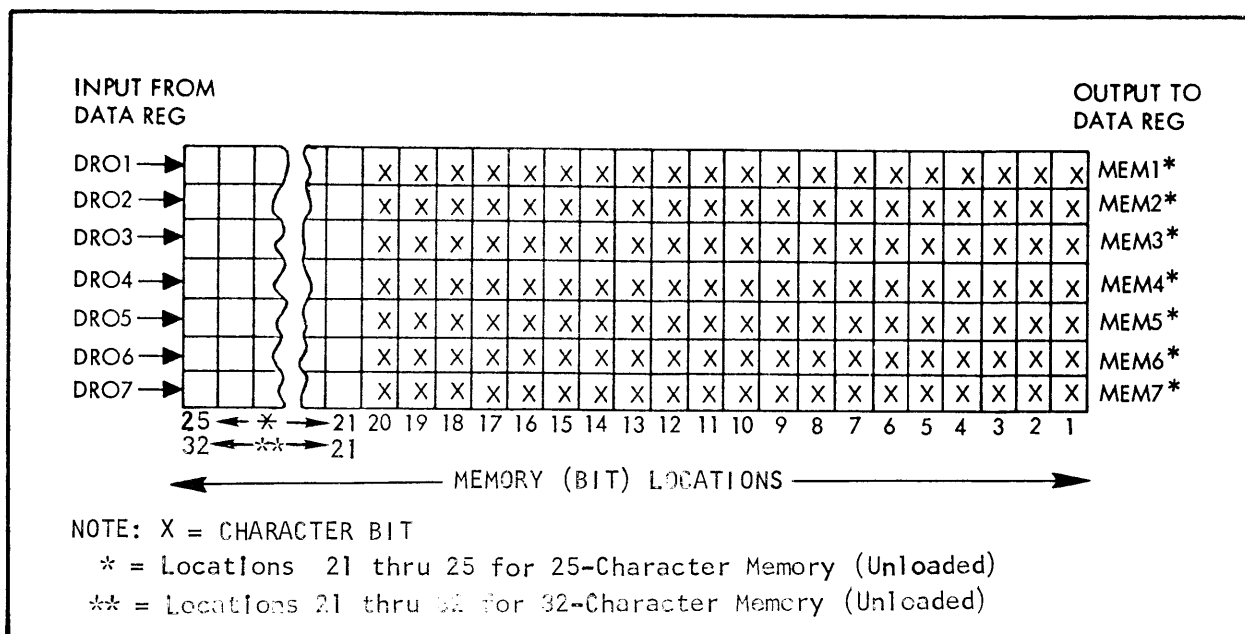


Figure 4-20. Character Buffer Memory Loaded

4-168b At count 31, flip-flops CR00, CR01, and CR02 are set and, with Mod 32 (figure 6-10) set high, enable NAND gate Z1. CRTC (column register top count) goes high. CRTC is applied to the set input of flip-flop A5Z13B (SCFF), inverted by A5Z3C, and applied to NOR gate A5Z9C. On the following PCP3 and clock time, the data in memory shifts again and the first character stored in memory is now in bit location 1 (figure 4-20).

4-169 On the rise of PCP4, the reset input to flip-flop SCFF goes high. At PCP4 and clock time, flip-flop SCFF sets and flip-flops SCEF, CR03, and CR04 reset. The column register is now completely reset, and the scan operation begins on receipt of character clock signal CHCK\*.

4-170 Character Clock Fan-Out (Figure 6-14). Magnetic pickup A2A1P1 monitors the drum code wheel and generates sinusoidal pulse CHP0 for each character on the drum. CHP0 is applied to the inverting input of differential comparator Z301A which functions as a detector and waveshaper.

4-171 A fixed threshold voltage of 2 to 3 volts, set by the feedback and input resistors on the noninverting input of Z301A, separates valid CHP0 pulses from noise or other extraneous pulses. During the duration of CHP0, the fixed output of Z301A goes low and is inverted by Z6C. The inverter output, a logic level square-wave pulse, is applied to adjustable delay circuit Q1-Q4, which determines the hammer firing time. The output of the delay circuit is inverted by Z3C and inverter output CHCK\* is applied to a fan-out consisting of inverter Z1B, and NAND gates Z1A, Z1C, and Z1D, which produce character clocks CHCK1 thru CHCK4. CHCK4 is the character counter clock input, and CHCK1, CHCK2, and CHCK3 are enable inputs to the hammer drivers.

4-172 CHCK\* goes low every 535 microseconds and remains low for 2 microseconds. If ONLINE is high at that time, CHCK1, CHCK2, and CHCK3 go high for 2 microseconds and then drop. If ONLINE goes low, CHCK1, CHCK2, and CHCK3 are inhibited and remain high, disabling the hammer drivers.

4-173 Character Clock Sync (Figure 6-7). When CHCK\* goes low, flip-flop Z5A is preset and the clock input to flip-flop Z5B (CCSN) goes high. At PCP4 and clock time, flip-flop Z5A resets and flip-flop CCSN sets. Output CCSN goes high, is applied to NAND gate A5Z14B and enables NAND gate A6Z8C. On the rise of the following clock, NAND gate A6Z16D is enabled and SHFT\* goes low.

4-174 SHFT\* is applied to data register (figure 6-8) NAND gate Z6A, and NOR gates Z14D, Z7B, Z7C, Z17B, Z17A, Z17C, and Z17D. An additional input to each NOR gate is memory output MEM1\* thru MEM7\*, respectively.

4-175 The buffered memory outputs are an inverted form of the data entered into memory. Assuming character 0, as previously described, was the first character entered into memory, it is now the first character to be shifted out of memory into the data register for comparison. The memory outputs are as follows:

MEM1\* = 0 (LSB)  
 MEM2\* = 0  
 MEM3\* = 0  
 MEM4\* = 0  
 MEM5\* = 1  
 MEM6\* = 1  
 MEM7\* = 0

4-176 The set inputs to data register flip-flops DR01, DR02, DR03, DR04, and DR07 go high. With SHFT\* low, the output of NAND gate Z6A goes high, NOR gate Z18B goes low, and inverter Z13A goes low on the rise of 2CLK. Signal CLK then goes high and on the fall of 2CLK, CLK goes low and the data register flip-flops set. The data register again contains the character code for 0 as follows:

DR01 = 1 (LSB)  
 DR02 = 1  
 DR03 = 1  
 DR04 = 1  
 DR05 = 0  
 DR06 = 0  
 DR07 = 1

4-177 At the time that the set inputs to the data register flip-flops go high, the set input to flip-flop A5Z13A (PCFF) also goes high and at the next clock, which concurs with 2CLK, flip-flop PCFF sets. Thus the data register and flip-flop PCFF are set in one PCP1 time. At PCP2 time flip-flop CCSN resets and CCSN goes low.

4-178 The character in the data register is now checked by the nonprintable code detector and compared in the comparator against the character counter output.

4-179 Nonprintable Code Detector (Figure 6-7). For character 0, the data register outputs to the detector are:

DR06\* = 1  
 DR07\* = 0  
 DR06 = 0  
 DR07 = 1

Since one input to each AND gate is low, the inputs to the NOR gate are low and LEGAL goes high. As it is PCP2 time, the output of NAND gate A5Z15C goes low, is inverted, and applied to the set input of flip-flop DIBF. On the next clock, flip-flop DIBF sets.

4-180 If the character checked is nonprintable, LEGAL goes low and is applied to inverter Z13B in the data register (figure 6-8). Inverter Z13B goes high, NOR gate Z14B goes low, and as NAND gate Z6B is also low at this time, NOR gate Z18C goes high. NOR gate Z18B goes low and on the rise of 2CLK, CLK goes high. With SHFT\* high, all reset inputs to the data register flip-flops are high. On the fall of 2CLK, CLK goes low and the flip-flops are reset. At this time a zero is shifted into the hammer driver register. At PCP3 and clock time, MSTR goes high, enters a zero into memory location 25, shifts the memory and places the second character in location 1. At PCP4 time, NAND gate A3Z4C is enabled, ADV C goes high, and the column register advances to count 1 when ADV C drops.

4-181 At the time the character is checked by the detector it is also simultaneously entered into the comparator for comparison to the current output of the character counter.

4-182 Comparator (Figure 6-7). The data register and character counter outputs are entered into the comparator in complementary pairs. If the drum character currently at the print station and the character in the data register are the same, a match occurs and comparator output COMP\* goes low.

4-183 As the first character in the description is 0, assume that the character counter output is also the code for 0. The complementary pairs entered into the comparator at PCP2 time are shown in table 4-4.

4-184 As each AND gate has one input low, their outputs are low and the outputs of gates Z9B, Z10B, Z10A, Z11B, Z11A, Z12B, and Z12A are high. Since the printer is not in the master clear state, all inputs to NAND gate Z15 are high and COMP\* goes low. In the master clear state MC1\* goes low and inhibits the comparator output.

4-185 COMP\* is applied to inverter A15Z4A and COMP goes high. COMP is applied to the set input of hammer register flip-flop 20, and NOR gate A3Z14B. COMP\* is applied to the reset input of flip-flop 20.

4-186 Hammer driver strobe HDST (figure 6-10) is now high, and on the rise of the clock, HDST\* (figure 6-14) goes low and hammer register strobes HDST1 thru HDST6 go high. On the fall of the clock, HDST1 thru HDST6 go low, strobe the hammer register, and set flip-flop 20. At the same time, the data register is reset in the manner previously described for a nonprintable character.



Table 4-4. Example of DR and CC Complementary Pairs

Data Register	Character Counter
DR01 = 1	CC01* = 0
DR01* = 0	CC01 = 1
DR02 = 1	CC02* = 0
DR02* = 0	CC02 = 1
DR03 = 1	CC03* = 0
DR03* = 0	CC03 = 1
DR04 = 1	CC04* = 0
DR04* = 0	CC04 = 1
DR05 = 0	CC05* = 1
DR05* = 1	CC05 = 0
DR06 = 0	CC06* = 1
DR06* = 1	CC06 = 0
DR07 = 1	CC07* = 0
DR07* = 0	CC07 = 1

4-187 At PCP3 and clock time, MSTR goes high, enters a zero into memory location 25, shifts the memory and places the second character in location 1.

4-188 At PCP4 time, NAND gate A3Z4C is enabled, ADV C goes high, and the column register advances to count 1 when ADV C drops.

4-189 If the character counter output is a code other than the one in the data register, a match does not occur and COMP stays low. A zero is shifted into the hammer register and the character in the data register is returned to memory location 25 and another character shifted into location 1.

4-190 Each character stored in memory is scanned and compared to the same drum character in the manner described in the preceding paragraphs. Each time a comparison occurs, the flip-flop in the hammer register corresponding to that character position is set. It requires only 80 microseconds to scan 20 characters. When CHCK\* again goes low, 535 microseconds later, it fires those hammers whose respective hammer register flip-flops have been set, and prints those column positions. Another scan and print operation is initiated and any remaining characters in memory are compared to the next character counter output.

4-191 Character Counter (Figure 6-7). During each scan cycle, the character counter provides the comparator with the code of the drum character currently entering the print station. Each character stored in memory is compared to it,

and if identical, printed. As each succeeding drum character enters the print station it increments the counter and initiates a scan cycle. During each scan, characters remaining in memory are compared and printed if identical. The sequence of scan, compare, and print is repeated until the memory is cleared and all characters are printed.

4-192 The drum contains 64 characters, each one appearing in a continuous row 80 columns wide across the surface of the drum. As the drum revolves, magnetic pickup A2A1PU1 generates 64 CHPO pulses during one complete revolution, or each time a character row enters the print station. Thus, character clock CHCK4 is generated each time and applied to gate Z9A, NAND gates Z13D and Z13A, and the clock input of flip-flop CC01 (LSB).

4-193 Magnetic pickup A2A1PU2 monitors the index code wheel and generates one sinusoidal INP0 pulse for each complete drum revolution. INP0 is applied to the inverting input of differential comparator Z201A (figure 6-14) which functions as a detector and waveshaper.

4-194 A fixed threshold voltage of 1 to 1.5 volts, set by the feedback and input resistors on the noninverting input of Z201A, separates valid INP0 pulses from noise or other extraneous pulses. During the duration of INP0, the fixed output of Z201A goes low and is inverted by Z6B. Inverter output CIND, a logic level squarewave pulse, is also applied to gate Z9A.

4-195 The relationship between input character code, drum row position, and character counter output is shown in table 4-5.

4-196 Since the input code for printable characters ranges from 32 to 95 (SPACE is considered a printable character), it is necessary to preset the character counter to 32 at the start of a drum revolution, and count up to 95 during one complete revolution. The positioning of the index code wheel ensures that index pulse CIND goes high prior to the 63rd CHCK4 pulse. As it does, the output of inverter Z13C goes high and is applied to the clock input of flip-flop LISN. CIND goes low after the 63rd CHCK4 pulse and flip-flop LISN is clocked and set. Output LISN goes true and is applied to gate Z9A and NAND gates Z13D and Z13A. When the 64th CHCK4 pulse goes high, it enables gate Z9A and NAND gates Z13D and Z13A. The clock input to flip-flop LISN again goes high and gate outputs CCR1 and CCR2 go low, clearing flip-flops CC01, CC02, CC03, CC04, CC05, and CC07. Flip-flop CC06 presets and the counter goes to count 32. When the 64th CHCK4 pulse goes low, flip-flop LISN is clocked and reset. The timing for this sequence is shown in figure 4-21.

Table 4-5. Code/Character Relationship

Input Character		Row On Drum	Character Counter	Remarks
Decimal Code	Drum Character			
0-9	-	-	-	Nonprintable
10	-	-	-	PF Command - Nonprintable

Table 4-5. Code/Character Relationship (Continued)

Input Character		Row On Drum	Character Counter	Remarks
Decimal Code	Drum Character			
11	-	-	-	Nonprintable
12	-	-	-	FF Command - Nonprintable
13	-	-	-	CR Command - Nonprintable
14-31	-	-	-	Nonprintable
32	SPACE	1 <sup>†</sup>	32	Inhibit Print
33	!	2	33	Printable Character
34	"	3	34	
35	#	4	35	
36	\$	5	36	
37	%	6	37	
38	&	7	38	
39	'	8	39	
40	(	9	40	
41	)	10	41	
42	*	11	42	
43	+	12	43	
44	,	13	44	
45	-	14	45	
46	.	15	46	
47	/	16	47	
48	Ø	17	48	
49	1	18	49	
50	2	19	50	
51	3	20	51	
52	4	21	52	
53	5	22	53	
54	6	23	54	
55	7	24	55	
56	8	25	56	
57	9	26	57	
58	:	27	58	
59	;	28	59	
60	<	29	60	
61	=	30	61	
62	>	31	62	
63	?	32	63	
64	@	33	64	
65	A	34	65	
66	B	35	66	
67	C	36	67	
68	D	37	68	Printable Character

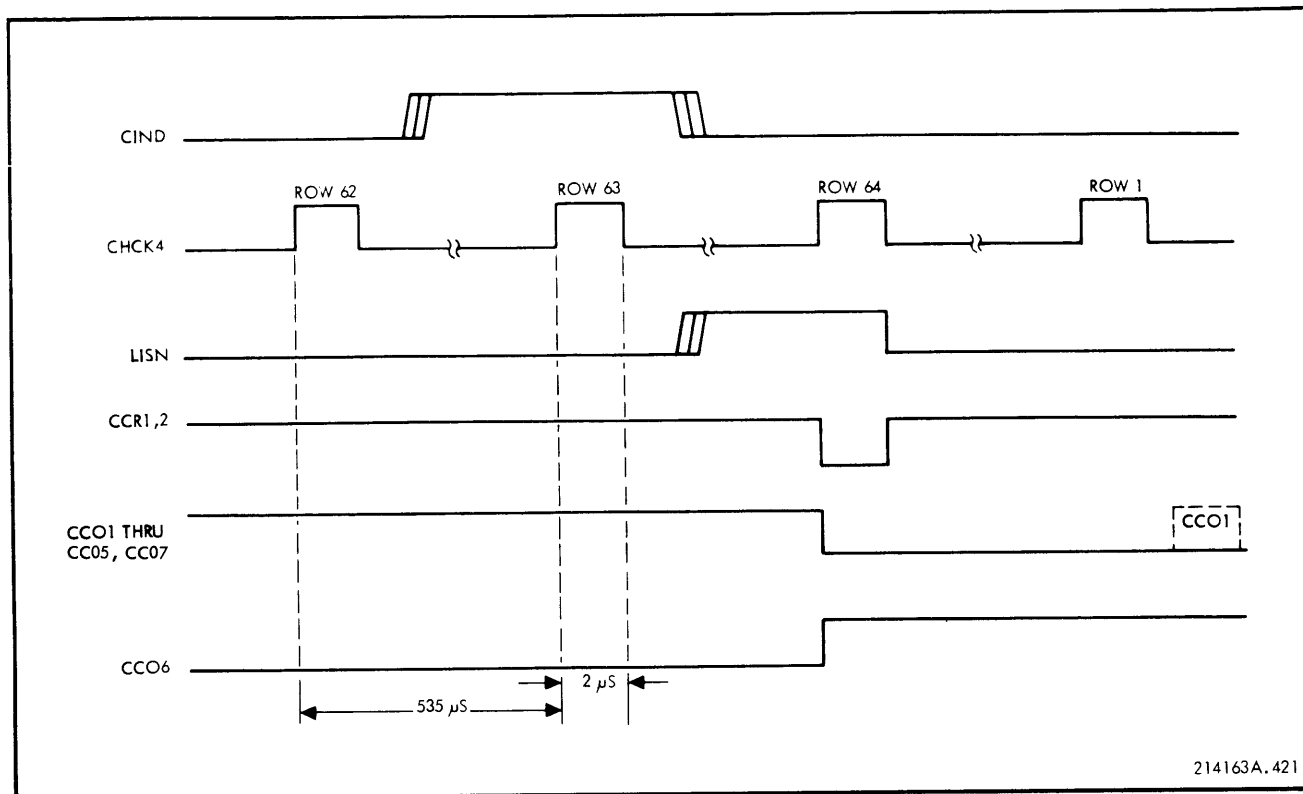
<sup>†</sup>The drum character f in row 1 is inhibited by the SPACE code.

Table 4-5. Code/Character Relationship (Continued)

Input Character		Row On Drum	Character Counter	Remarks
Decimal Code	Drum Character			
69	E	38	69	Printable Character ↑ ↓ Printable Character Nonprintable
70	F	39	70	
71	G	40	71	
72	H	41	72	
73	I	42	73	
74	J	43	74	
75	K	44	75	
76	L	45	76	
77	M	46	77	
78	N	47	78	
79	O	48	79	
80	P	49	80	
81	Q	50	81	
82	R	51	82	
83	S	52	83	
84	T	53	84	
85	U	54	85	
86	V	55	86	
87	W	56	87	
88	X	57	88	
89	Y	58	89	
90	Z	59	90	
91	[	60	91	
92	◇	61	92	
93	]	62	93	
94	^	63	94	
95	♥	64	95	
96-127	-	-	-	

4-197 Each time a character row passes the print station, as the drum revolves, CHCK\* initiates a new scan cycle and CHCK4 increments the counter one count. At count 79 (character O) the first comparison is made and hammer register flip-flop 20 is set. One by one, the remaining characters in memory are compared for code 79 and if comparisons are made, their respective hammer register flip-flops are set. The next CHCK4 increments the counter to 80 and CHCK1 thru CHCK3 fire those hammers whose respective hammer register flip-flops have been set. In this manner, all columns containing the character O are printed simultaneously.

4-198 Each time the counter is incremented, another scan cycle is initiated and all comparisons are printed. The count continues to 95 (64th row), the counter resets to 32, and the operation described is repeated until all characters in memory are printed.



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Figure 4-21. Character Counter Reset Timing Diagram

4-199 Hammer Register and Driver (Figure 6-27). The hammer register is a 20-bit shift register, formed by five hammer driver AH-10 cards, which is initially cleared by HDCL\* during the master clear state. In the scan and print state, the contents of the register shift during each character scan when strobes HDST1 thru HDST5 go low.

4-200 The first time the contents of the data register and character counter compare, COMP goes high, and flip-flop 20 sets when HDST1 goes low at PCP2 and clock time. After the next character scan, flip-flop 19 sets and flip-flop 20 either sets if there was a comparison or resets if there was not. As each character is scanned, the contents of the register shifts.

4-201 Assuming two comparisons were made during a scan cycle, the first and tenth characters, only flip-flops 1 and 10 are set at completion of the cycle. When CHCK\* goes low, CHCK2 and CHCK3 go high, enabling NAND gates A20Z3C and A22Z3D.

4-202 The following description of hammer driver operation applies to all drivers. See figure 6-17 for the circuitry involved.

4-203 When gate Z3C goes low, it triggers single-shot Q1/Q2. The single-shot output is 2 microseconds wide, as determined by the duration of CHCK\*. The single-shot output couples through transistor Q3 and turns on Darlington pair Q4 and Q5 for 1.5 milliseconds. Resistor R10 provides linear feedback to Q3 and ensures a constant current at the output of Q5. Assuming zone 1 is being printed, zone control signals ZC1K goes low and ZC1G goes high which triggers SCR A4Q1 (figure 4-22) and puts +65v on one side of hammer coils 1 thru 20. To energize the hammers, the opposite side of each coil must be returned to ground. The hammer drivers, essentially switches, act as current sinks when turned on at CHCK\* time, and a current pulse of 1.8 amperes is supplied to each hammer for 1.5 milliseconds.

4-204 Since in our description only flip-flops 1 and 10 are set, only hammers 1 and 10 fire at CHCK\* time. At PCP4 and clock time following CHCK\*, CCSN goes high and is inverted by A9Z5A thru A9Z5D, and A9Z6A. Outputs HDRS1\* thru HDRS5\* go low, clearing flip-flops 1 and 10.

4-205 The column register advances one count for each character scanned. At count 19, if memory still contains characters, the reset inputs to flip-flops DIBF, PCFF, and SCFF go true, and the set input to flip-flop SCEF goes true. At PCP4 and clock time, flip-flops DIBF, PCFF, and SCFF reset. Flip-flop SCEF sets, initiating another scan and print cycle.

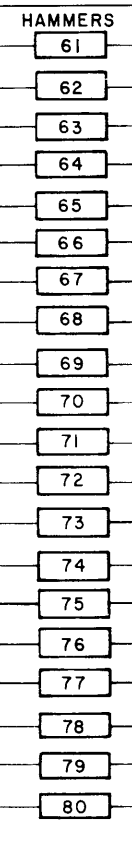
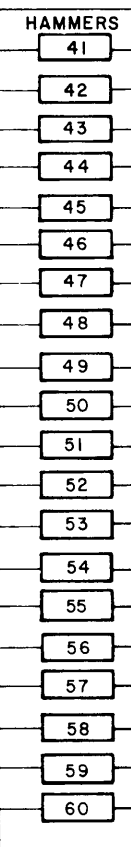
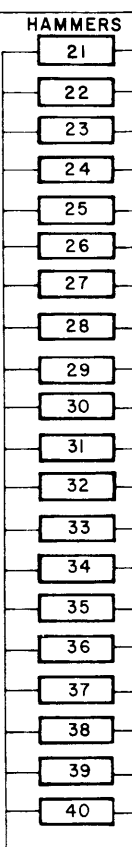
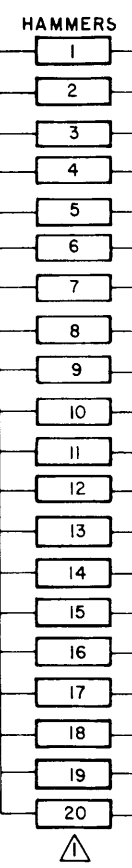
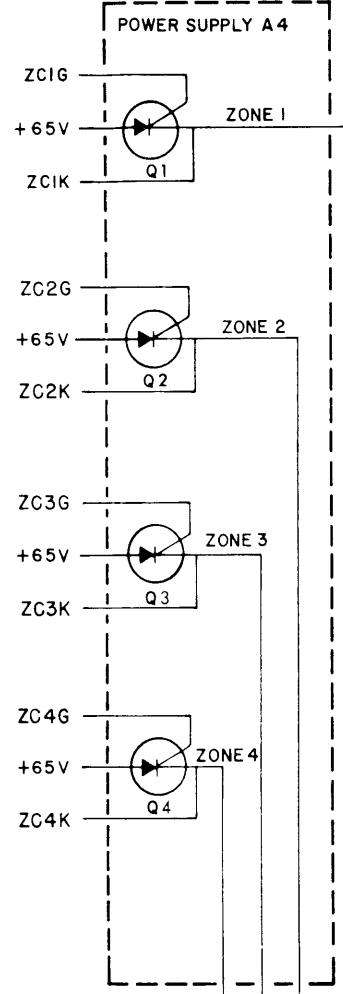
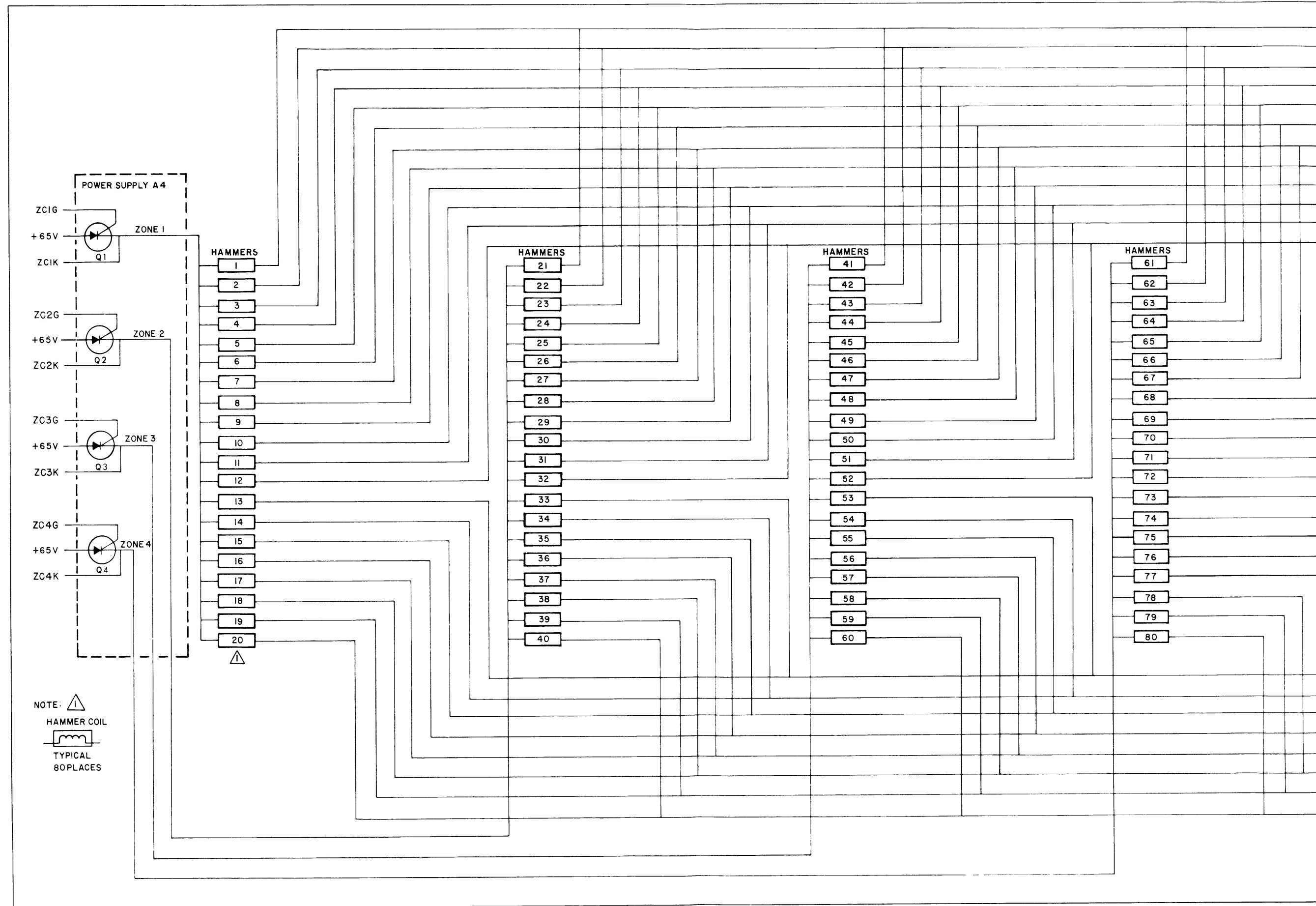
4-206 The scan and print cycle repeats until all characters in memory are compared, erased, and printed. When the last character is printed, a final scan is initiated. Since the memory now contains all zeros, COMP and LEGAL remain low and flip-flop DIBF does not set. At column register count 19, the printer determines if it must execute a paper feed command or zone change.



4-207 If a PF or FF command had been received with the input data, paper feed command PFCM will be high and PFCM\* low. The output of end of scan decode NAND gate Z18B (figure 6-9), goes low, enables NOR gate Z17C, and the set input to flip-flop MPEF goes true. The reset inputs to flip-flops SCFF and PCFF also go true. At PCP4 and clock time, flip-flops SCFF and PCFF reset and flip-flop MPEF sets. The printer now enters the paper advance state.

4-208 If PFCM is not high at count 19, then NOR gate Z17A is enabled by the output of gate Z18B and the set input to flip-flop ZCEF goes true. The reset inputs to flip-flops SCFF and PCFF also go true. At PCP4 and clock time, flip-flops SCFF and PCFF reset and flip-flop ZCEF sets. The printer now enters the zone change state.

#### 4-209 Paper Advance State

4-210 In the paper advance state, the printer executes a PF or FF command, clears the column register, and raises DEMAND LINE to request new data. See figure 4-23 for a flow and timing diagram of the paper advance state.



NOTE:  HAMMER COIL  
 TYPICAL  
 80PLACES

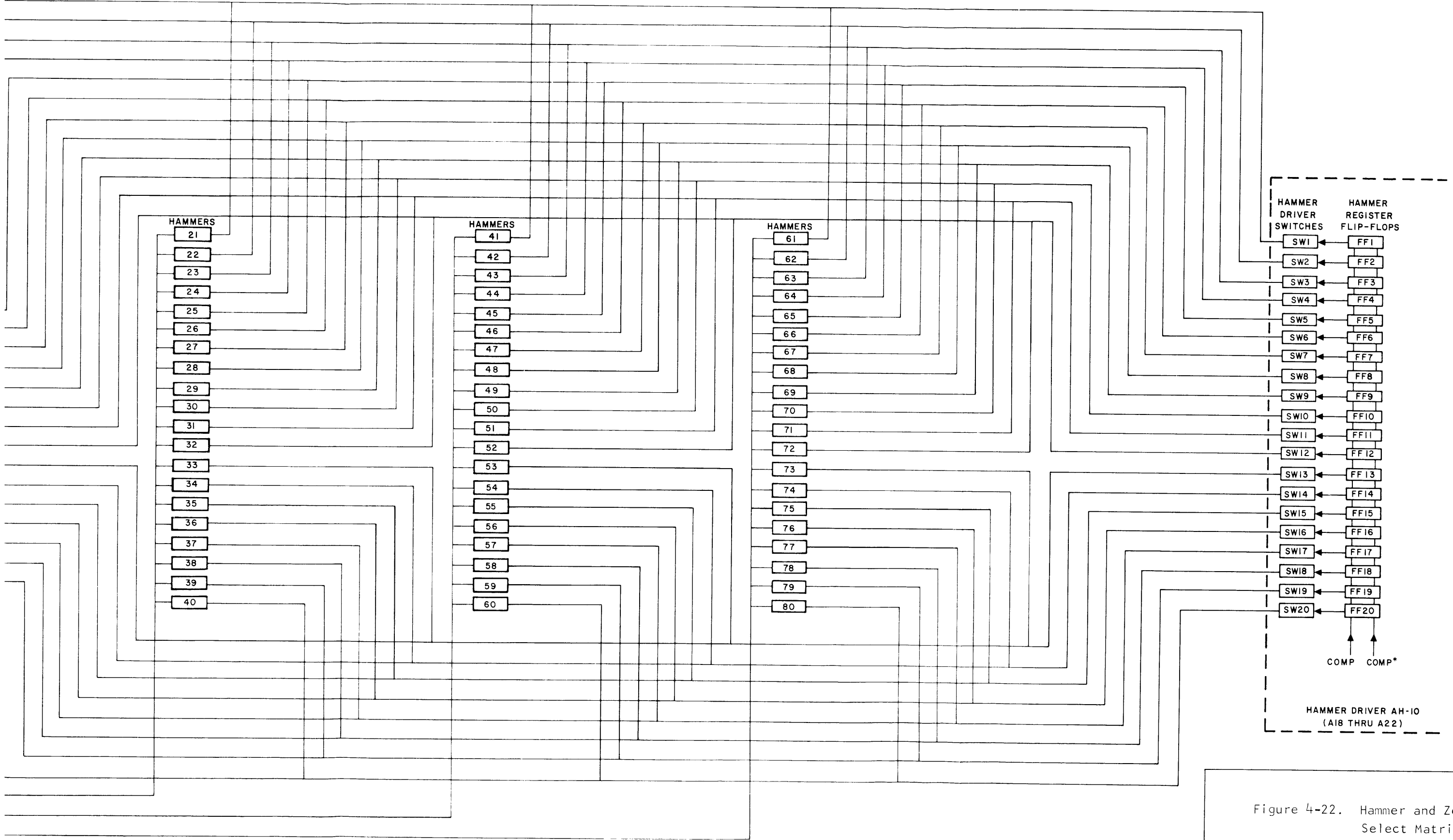


Figure 4-22. Hammer and Zone Select Matrix



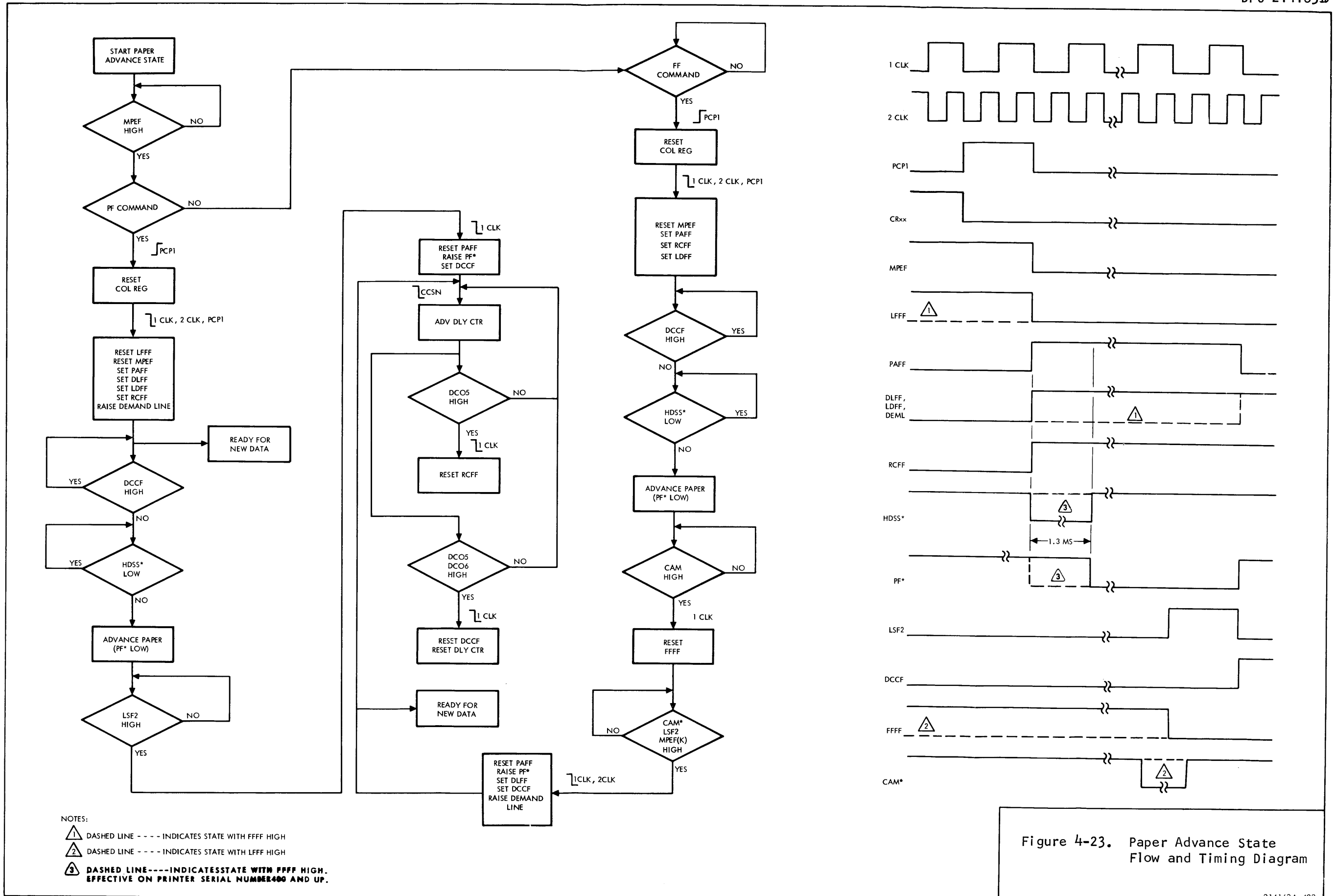


Figure 4-23. Paper Advance State Flow and Timing Diagram

4-211 PAPER ADVANCE OPERATION (Figure 6-9). If a PF command is to be executed, flip-flop LFFF is preset by the output of decode Z1, as previously described and flip-flop MPEF is set. At PCP1 time, NAND gates Z15C and Z8B are enabled and the reset inputs to flip-flops LFFF and MPEF go true. Reset input MPEF(K) enables NOR gates Z16A and Z16B and signals ZCRS\*, MPLD\*, and CRRS1\*, all go low. CRRS1\* is applied to column register NAND gate Z5C (figure 6-8), which goes high and is inverted by Z6D. The inverter output, CRRS\*, clears the column register. MPLD\* is applied to NAND gates A6Z9C and A5Z7A. The set inputs to flip-flops DLFF and LDFE go true. ZCRS\* clears the zone control flip-flops, and starts a 2.2-milli-second delay which drops HDSS\* and disables NAND gate Z15B. This allows the hammers sufficient time to strike the paper before paper advances.

4-212 At PCP1, clock and 2CLK time, flip-flops LFFF and MPEF reset, flip-flops PAFF, DLFF, and LDFE set, and flip-flop RCFF presets. When flip-flop DLFF sets, signal DEML goes high, DEMAND LINE is raised, and new data can be accepted by the printer.

4-213 When flip-flop PAFF sets, output PAFF goes true and is applied to NAND gate Z15B. When 1.3 milliseconds have elapsed, HDSS\* goes high, enabling NAND gate Z15B and output PF\* goes low, to initiate paper advance as previously described. Zone control is also reset to zone 1 at the end of the delay time.

4-214 When flip-flop RCFF presets, output RCFF\* goes false, inhibits NAND gate Z14B, and prevents flip-flop PCFF from being set during paper advance.

4-215 To advance paper more than one line after completion of a scan and print operation, it is necessary that the first character received after DEMAND LINE is raised, be a PF command. If this occurs, flip-flops LFFF and MPEF are set, as previously described in the load data operation for control character only.

4-216 During execution of the first PF command, flip-flop LFFF presets on receipt of the second PF command. PFCM goes high, enables NAND gate Z19A, and the set input to flip-flop MPEF goes high. On the next clock, flip-flop MPEF sets, and output MPEF\* goes false, disabling NAND gate Z18A. The reset input remains false and flip-flop PAFF does not reset on completion of the first line advance. Since PAFF remains true, PF\* stays low, and the paper continues to advance another line.

4-217 Line Strobe Sync (Figure 6-11). Magnetic pickup A2A3PU1 monitors the line strobe code wheel and generates one sinusoidal LNSTP0 pulse each time the paper advances one line. LNSTP0 is applied to the inverting input of differential comparator Z101A (figure 6-14) which functions as a detector and waveshaper. A fixed threshold voltage of 50 to 120 millivolts, set by the feedback and input resistors on the noninverting input of Z101A, separates valid LNSTP0 pulses from noise or other extraneous pulses. During the duration of LNSTP0, the fixed output of Z101A goes low and is inverted by Z6A. Inverter output LNST, a logic level squarewave pulse, is applied to the clock input of flip-flop LSFF.

4-218 On completion of a PF command flip-flop LSFF sets and output LSFF goes true. On the next clock, flip-flop LSF2 sets, output LSF2 goes true, enables NOR gate Z11B and flip-flop LSFF is cleared. LSF2 also enables NAND gate A9Z1C. The gate output is applied to inverter A9Z6D and LSF2CM is applied to NAND gate A4Z19C.

- 4-219 When a PF command is not followed by another, flip-flop PAFF normally resets on the clock after LSF2 goes true. If a successive PF command is given, flip-flop MPEF is set, as previously described, and when LSF2 goes high on completion of the first line advance, flip-flop PAFF does not reset but NAND gate Z19C is enabled. Gate output FFLS\* goes low and the reset input to flip-flops LFFF and MPEF go true.
- 4-220 On the next clock, flip-flops LFFF and MPEF reset. When LSF2 goes high on completion of the second line advance, NAND gate Z18A is enabled, and gate output PAFF(K)\* goes low. When PAFF(K)\* goes low the reset input to flip-flop PAFF goes true, and the set input to delay counter flip-flop DCCF goes true.
- 4-221 On the next clock, flip-flop PAFF resets, and flip-flop DCCF sets, disabling NAND gate Z15B. Output DCCF goes true, and is applied to the delay counter. See figure 4-24 for a diagram of the line strobe sync timing.
- 4-222 Delay Counter (Figure 6-7). On completion of the paper advance operation, the delay counter initiates a 26-millisecond delay which keeps NAND gate Z15B disabled and prevents another paper advance during that time. Due to the large amount of power required to start and stop the paper feed motor, the delay between paper advances is necessary to prevent overheating of the motor. See figure 4-25 for a delay counter timing diagram.
- 4-223 The counter is initially cleared by flip-flop DCCF being reset. When flip-flop DCCF sets, output DCCF goes true and is applied to NAND gate Z14D. The gate is enabled when CCSN goes high, and the clock input to flip-flop DC01 goes high. When CCSN goes low, flip-flop DC01 is clocked and set. The counter is incremented one count for each succeeding CCSN pulse.
- 4-224 At count 16, flip-flop DC05 is set and output DC05\* goes false. DC05\* is applied to recovery reset NAND gate Z4B (figure 6-14) and output RCRS goes true. RCRS is applied to the reset input of flip-flop RCFF. On the next clock, flip-flop RCFF resets and flip-flop PCFF is no longer inhibited.
- 4-225 At count 48 flip-flops DC05 and DC06 are set and outputs DC05 and DC06 go true, enabling NAND gate Z13B. Output DCTC\* goes low, is applied to delay counter logic NAND gate Z14D (figure 6-9) and the reset input to flip-flop DCCF goes true. On the next clock, flip-flop DCCF resets, the delay counter is cleared, and paper feed is no longer inhibited.
- 4-226 Execution of a FF command is basically the same operation as described for a PF command. Flip-flop FFFF is preset by the output of decode Z2, as previously described and flip-flop MPEF is set. CRSS1\* goes low but NAND gate Z13A is inhibited by the output of NOR gate Z16D and MPLD\* remains high. CRRS1\* is applied to NAND gate Z7A (figure 6-10) and the set input to flip-flop LDFF goes high. The column register is cleared, and at PCP1, clock and 2CLK time, flip-flop MPEF resets, flip-flops PAFF and LDFF set, and flip-flop RCFF presets. PF\* goes low and paper advance is initiated. With FFFF and DIBF\* both high, the output of NAND gate Z8D goes low, disabling NAND gate Z18A, and inhibiting the reset of flip-flop PAFF when LSF2 goes high. The paper continues to advance, top-of-form cam switch is actuated and CAM goes true. On the next clock flip-flop FFFF resets and FFFF goes low, enabling NAND gate Z8D. The paper advances to the third line of the next form, releases the cam switch, and CAM\* goes true. When LSF2 and LSF2CM go high, NAND gates Z18A and Z19C are enabled. FFLS\* goes low, ZCRS\* goes low, initiating the reset to zone 1. The output of gate Z16D goes high, enables gate Z13A and MPLD\* goes low. At clock and 2CLK clock time, flip-flop PAFF resets, and flip-flops LDFF and DLFF set. The DEMAND LINE is raised and the 26 millisecond delay is initiated. The completion of the operation is now as described for a PF command.

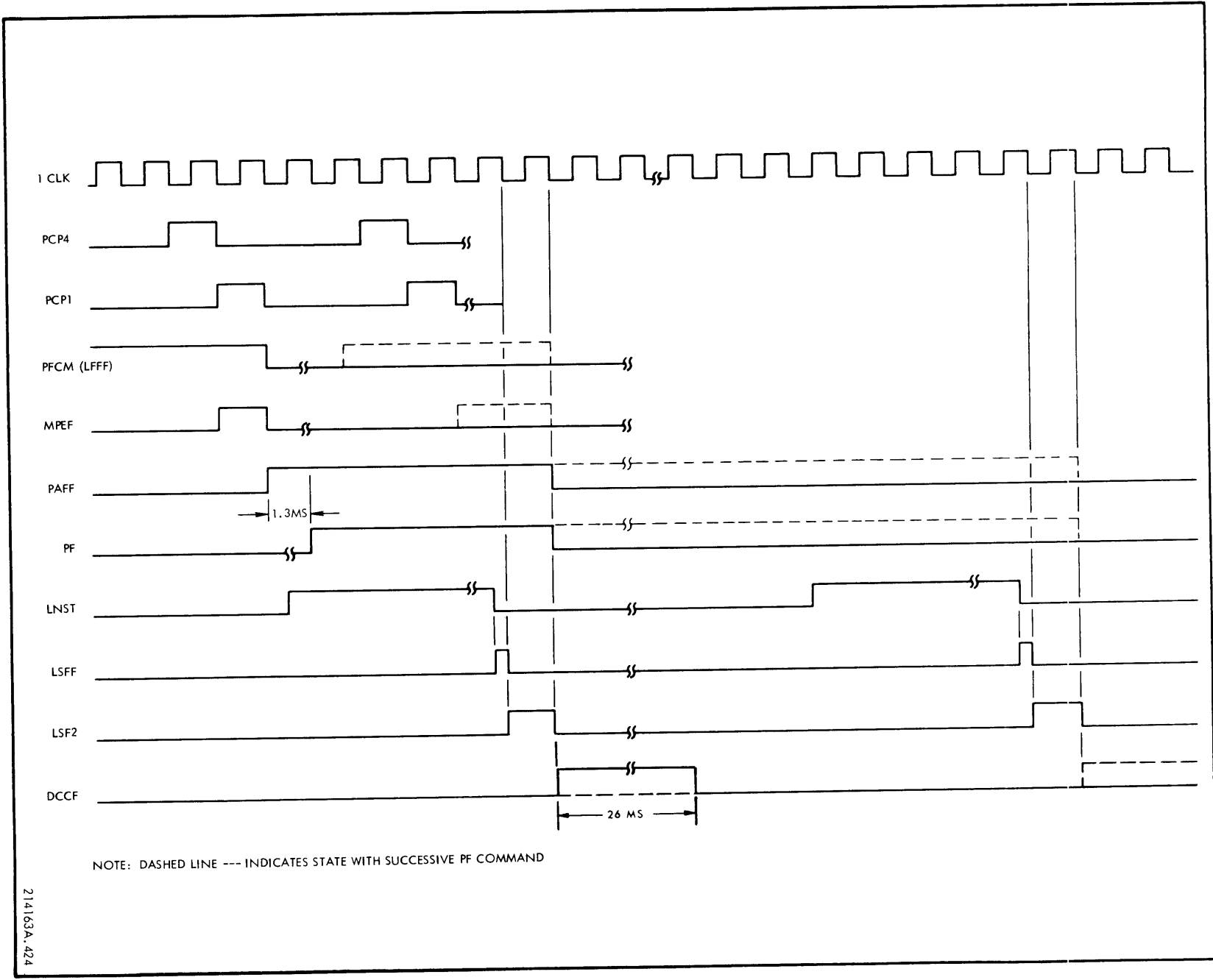


Figure 4-24. Line Strobe Sync Timing Diagram

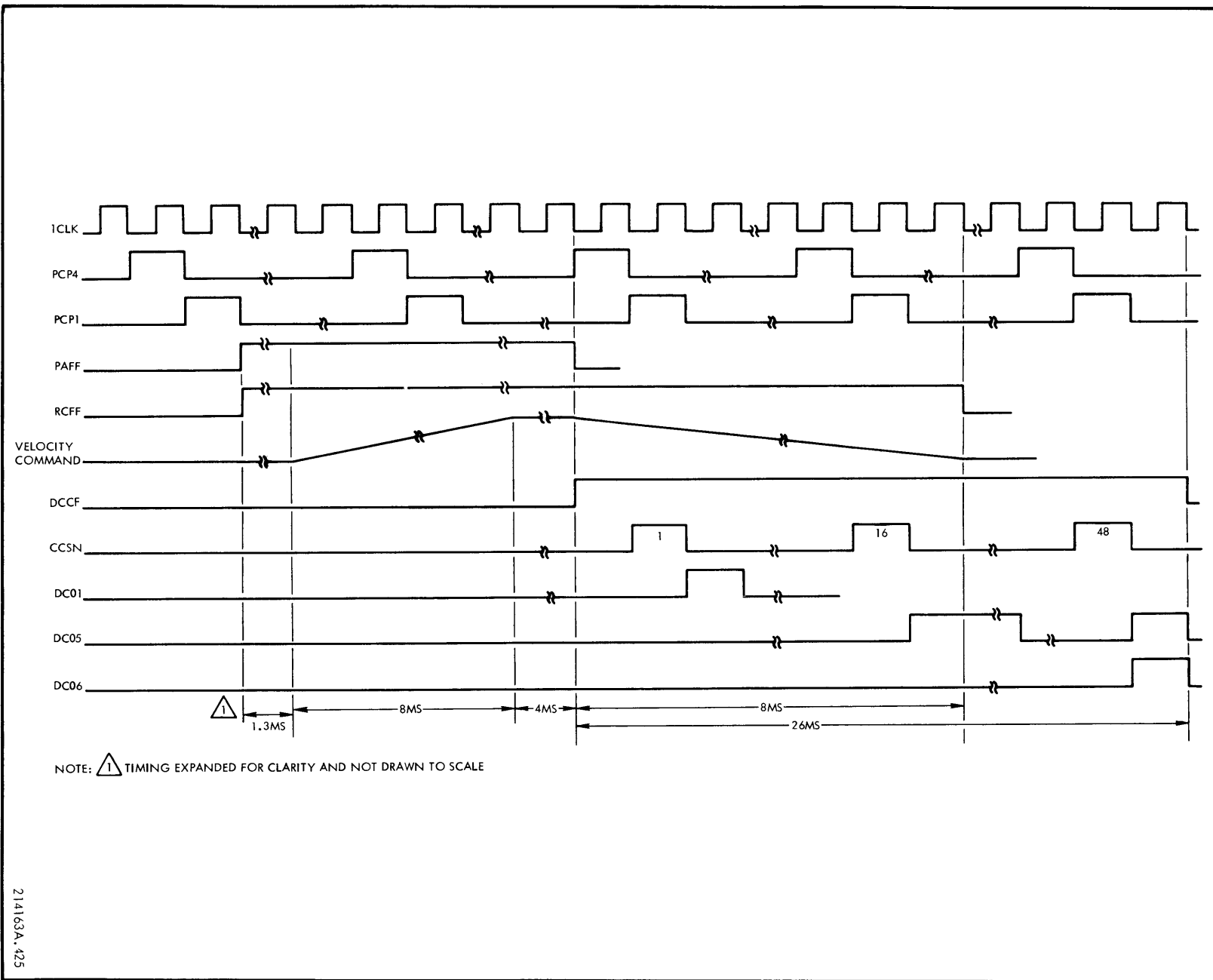


Figure 4-25. Delay Counter Timing Diagram

4-227 Zone Change State

4-228 In the zone change state the printer switches the hammer excitation to the next zone to be printed, or back to zone 1 after a PF, CR, or FF command is executed. See figure 4-26 for a flow and timing diagram of the zone change state.

4-229 ZONE CHANGE OPERATION (Figure 6-9). Assuming four zones are to be printed and zone 1 is now completed, flip-flop ZCEF is set, as previously described, and output ZCEF\* goes false. ZCEF\* is inverted by Z20A and on the rise of PCP1, NAND gate Z15A is enabled and ZCAV\* goes low. ZCAV\* is inverted by Z13D and ZCAV goes high. ZCAV\* is also applied to NAND gates Z20B, A5Z7A, and A6Z9C. The set inputs to flip-flops DCCF, RCFF, LDFF, and DLFF go true. ZCAV is applied to NOR gate Z16B, the reset input of flip-flop ZCEF, the set input of flip-flop A15Z5A (ZCFF) and zone control AZ-18.

4-230 Gate output CRRS1\* is applied to column register NAND gate Z5C (figure 6-8) and, as previously described, CRRS\* goes low and clears the column register.

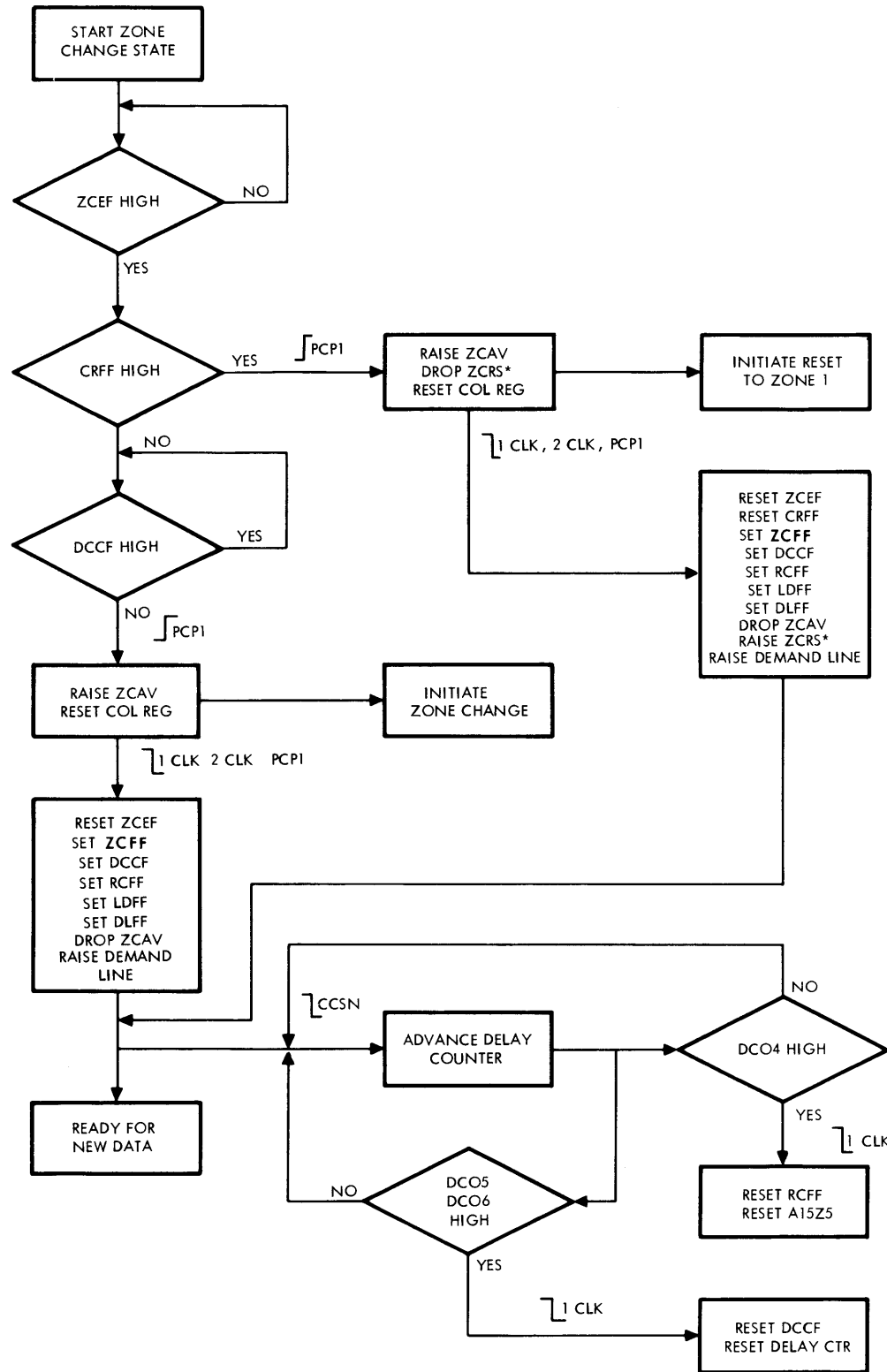
4-231 At PCP1, clock and 2CLK time, flip-flop ZCEF resets, and flip-flops ZCFF, DCCF, RCFF, LDFF, and DLFF set. As previously described, the DEMAND LINE is raised, print control flip-flop PCFF is inhibited, and the delay counter is enabled. Output DCCF\* is false, inhibiting NAND gate Z15A, and preventing another zone change until flip-flop DCCF resets. This occurs after 26 milliseconds. The delay is necessary to give the hammer excitation voltage time to recover, as it is dragged down when the hammers fire. During the delay counter operation, output DC04 goes true at a count of 8 and NAND gate A15Z4C is enabled. RCRS goes true and is applied to the reset inputs of flip-flops ZCFF and RCFF. On the next clock, flip-flops ZCFF and RCFF reset. Flip-flop PCFF is no longer inhibited. The delay is not necessary if a PF, CR, or FF command, or option signal ZONE SELECT, is the first character received after DEMAND LINE is raised. When this occurs, CONT goes high, enables NAND gate A9Z4A, and output DCRS\* goes low. DCRS\* is applied to NAND gate A4Z14D and the reset input to flip-flop DCCF goes high. On the next clock, flip-flop DCCF resets and the delay counter is cleared. Thus the 26-millisecond delay is cancelled and the command can be executed immediately.

4-232 Zone Control AZ-18 (Figure 6-16). In the master clear state, ZCRS\*, MC2\*, and MC3\* are low. Flip-flop Z4A is preset and flip-flops Z1A, Z1B, Z4B, Z5A, and Z5B are cleared.

4-233 Since flip-flop Z4A is initially preset, output Z4AQ\* goes false and is applied to transistor Q1 of CKT 100. The inverted output of Q1 is applied to transistor Q3 and appears high at point B (ZCIG) and low at point C (ZCIK). ZCIK and ZCIG provide cathode and trigger potentials respectively, for SCR A4Q1, switching +65v excitation to the hammers in zone 1. Transistor Q4 provides holding current for SCR A4Q1 while it is turned on.

4-234 To initiate the change from zone 1 to zone 2, ZCAV goes high as previously described. It is applied to the clock input of flip-flop Z1A and starts the 2.2-millisecond one-shot and delay in CKT 500.

4-235 ZCAV goes low after 1 microsecond and flip-flop Z1A is clocked and set. Output Z1AQ goes true and is applied to the clock input of flip-flop Z1B and enables NAND gate Z2C. The gate output goes low, is inverted by Z2B, and the set input to flip-flop Z4B goes true. NAND gate Z2D is disabled and the reset input to flip-flop Z4A is true.



NOTE:  
 DASHED LINE --- INDICATES ALTERNATE STATE

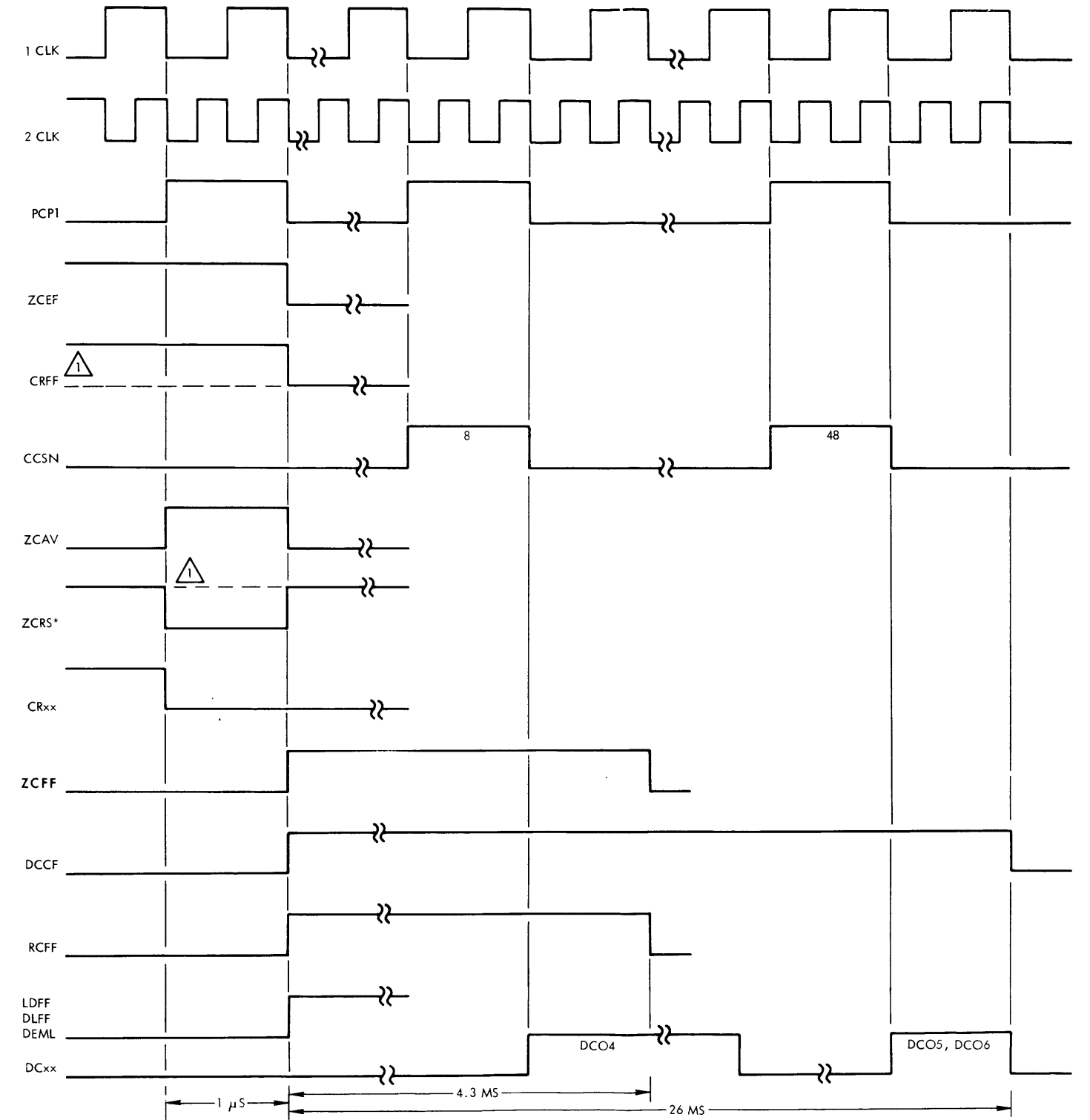


Figure 4-26. Zone Change State Flow and Timing Diagram

- 4-236 When ZCAV is applied to CKT 500, the output at point G (HDSS) goes high and the output at point H (ZCCK) remains low. HDSS remains high for 2.2 milliseconds and is applied to inverter A6Z16C. HDSS\* goes low and inhibits NAND gate A4Z15B, preventing a paper advance during zone change.
- 4-237 When 2.2 milliseconds has elapsed, HDSS goes low, and ZCCK goes high for approximately 2 microseconds. When ZCCK drops, it clocks and sets flip-flop Z4B and resets flip-flop Z4A. ZC1K goes high, ZC1G goes low, the holding current is removed and SCR A4Q1 is turned off. Output Z4BQ\* goes false and is applied to CKT 200. The outputs of CKT 200 are ZC2K and ZC2G. ZC2K goes low and ZC2G goes high, triggering SCR A4Q2 which switches +65v excitation to the zone 2 hammers. A holding current is also applied to SCR A4Q2.
- 4-238 To initiate the change from zone 2 to zone 3, ZCAV goes high and starts the 2.2-millisecond one-shot and delay. Flip-flop Z1A is clocked and reset when ZCAV goes low and flip-flop Z1B is clocked and set when Z1AQ goes false. Output Z1BQ goes true, disables NAND gate Z2C and enables NAND gate Z3D. The reset input to flip-flop Z4B goes true, and the set input to flip-flop Z5A goes true. When ZCCK goes low, it clocks and resets flip-flop Z4B and sets flip-flop Z5A. SCR A4Q2 is cut off and the outputs of CKT 300 turn on SCR A4Q3, switching +65v excitation to the zone 3 hammers.
- 4-239 To initiate the change from zone 3 to zone 4, ZCAV goes high and starts the 2.2-millisecond one-shot and delay. When ZCAV goes low, flip-flop Z1A is clocked and set and output Z1AQ goes true. NAND gate Z3D is disabled and NAND gate Z3C is enabled. The reset input to flip-flop Z5A goes true and the set input to flip-flop Z5B goes true. When ZCCK goes low, it clocks and resets flip-flop Z5A and sets flip-flop Z5B. SCR A4Q3 is cut off and the outputs of CKT 400 turn on SCR A4Q4, switching +65v excitation to the zone 4 hammers.
- 4-240 After the four zones have been printed and during the paper advance operation, ZCRS\* goes low, clears flip-flops Z1A and Z1B, and starts the 2.2-millisecond one-shot and delay. NAND gate Z3C is disabled and only NAND gate Z2D is enabled. The reset input to flip-flop Z5B goes true, and the set input to flip-flop Z4A goes true. When ZCCK goes low, flip-flop Z5B resets and flip-flop Z4A sets. The +65v excitation is switched back to the zone 1 hammers.
- 4-241 The zone change operation described is repeated for each complete line of data. In a paper advance operation, zone control AZ-18 is always reset to zone 1.
- 4-242 CR COMMAND (Figure 6-9). If a CR command is to be executed, flip-flop CRFF is preset by the output of decode Z3 and flip-flop ZCEF is set. On the rise of PCP1, NAND gate Z15A is enabled and ZCAV\* goes low. The set inputs to flip-flops DCCF, RCFF, LDFF, and DLFF go true. ZCAV goes high, enables NAND gate Z12D and NOR gate Z16B. The reset inputs to flip-flops ZCEF and CRFF go true and the set input to flip-flop ZCFF goes true. CRRS1\* goes low and clears the column register. ZCRS\* goes low, clears zone control flip-flops Z1A and Z1B and starts the 2.2-millisecond one-shot and delay.
- 4-243 At PCP1, clock and 2CLK time, flip-flops ZCEF and CRFF reset and flip-flops ZCFF, DCCF, RCFF, LDFF, and DLFF set. DEMAND LINE is then raised, print control flip-flop PCFF is inhibited, delay counter is enabled, and zone control AZ-18 is reset to zone 1.



4-244 OFF-LINE PRINTER OPERATION

4-245 The off-line printer operation consists only of advancing paper through use of manual format control switches PAPER STEP and TOP OF FORM. In the event data transmission is incomplete or interrupted, either switch can be used to initiate the print cycle.

## 4-246 PAPER STEP SWITCH

4-247 The PAPER STEP switch is a momentary contact switch that advances paper one line when pressed and released.

4-248 Paper Step Operation (Figure 6-10)

4-249 Assuming power on, paper loaded, all interlocks satisfied, and printer off-line, signal LF1 goes high when the PAPER STEP switch is pressed, and remains high until the switch is released.

4-250 The switch outputs are applied to a debounce network consisting of NAND gates Z6C and Z6D. When LF1 goes high, LF2 goes low and the output of gate Z6D goes high. Output LFSW enables gate Z6C and LFSW\* goes low. When LFSW\* goes low, the clock input to flip-flop LFEF goes high. Since it is initially cleared by LDFF(J) during master clear operation, flip-flop LFEF is in the reset state at this time. Set input RUN\* is high and when switch PAPER STEP is released, the clock falls and flip-flop LFEF sets. Output LFEF\* goes low and is applied to NAND gates Z7C and A4Z8A. The set input to flip-flop LFFF and gate output SPSE go high. SPSE is applied to NAND gate A4Z19A. On the next clock, flip-flop LFFF sets, output LFFF\* goes low, and PFCM goes high. PFCM enables gate A4Z19A and the set input to flip-flop MPEF goes high. On the next clock flip-flop MPEF sets and initiates the paper advance operation.

## 4-251 TOP OF FORM SWITCH

4-252 The TOP OF FORM switch is a momentary contact switch that advances tractors to the top-of-form position when pressed and released.

4-253 Top-Of-Form Operation (Figure 6-10)

4-254 The TOP OF FORM switch advances tractors to top-of-form position with drum gate open or closed, and with or without paper loaded.

4-255 DRUM GATE OPEN. When power is initially applied, input RDY at inverter A9Z6B is low. Inverter output RDY\* is delayed by resistor A9R2 and capacitor A9C2 from going high for 47 milliseconds. RDY\* thus remains low long enough to clear manual form feed flip-flop A15Z5B (PF2). It then goes high and remains high until all interlocks are satisfied. Assuming power on, only power and paper feed motor interlocks satisfied, and printer off-line, signal FF1 goes high when TOP OF FORM switch is pressed, and remains high until the switch is released.

4-256 The switch outputs are applied to a debounce network consisting of NAND gates Z6A and Z6B. When FF1 goes high, FF2 goes low and the output of gate Z6A goes high. Output FFSW enables gate Z6B and FFSW\* goes low. FFSW\* is applied to NAND gates A9Z2A and A9Z1D. The output of gate A9Z2A goes high, is inverted by A9Z6C, and flip-flop A9Z9B presets. Output FFCL of gate A9Z1D also goes high, and is applied to the clock input of flip-flop PF2.

4-257 When switch TOP OF FORM is released, the clock falls, flip-flop PF2 sets, and output PF2 is applied to NAND gate A9Z2D. Output PF2\* goes low, energizes paper feed control, and the tractors advance towards top-of-form. As the tractors advance, the top-of-form cam switch is actuated and signal CAMSW goes high.

4-258 The top-of-form cam switch outputs are applied to a debounce network consisting of NAND gates A9Z1A and A9Z1B. When CAMSW goes high, CAMSW\* goes low and output CAM of gate A9Z1A goes high. CAM is applied to the clock input of flip-flop A9Z9B and also enables gate A9Z1B. CAM\* goes low, disabling NAND gate A9Z1C. When the tractors reach top-of-form, releasing the cam switch, CAM goes low, and flip-flop A9Z9B resets. Output A9Z9BQ\* goes high and is applied to NAND gate A9Z3B. Line strobe signal LNST now goes high and enables gate A9Z2D. Output LNSTPF2\* is inverted by A9Z5E and gate A9Z3B is enabled by LNSTPF2. FFCL again goes high, and when LNST goes low, FFCL drops and flip-flop PF2 resets and paper feed control is deenergized. When all interlocks are satisfied and RDY goes high, RDY\* goes low, flip-flop A9Z9B presets and gate A9Z3B and flip-flop PF2 are disabled.

4-259 DRUM GATE CLOSED. Assuming power on, paper loaded, all interlocks satisfied and printer off-line, signal FF1 goes high and FF2 low when switch TOP OF FORM is pressed, and remains so until the switch is released. Both switch outputs are applied to the debounce network and output FFSW\* goes low. When FFSW\* goes low the clock input to flip-flop LFEF and the set input to flip-flop FFFF go high. On the next clock, flip-flop FFFF sets, output FFFF\* goes low, and PFCM goes high. When switch TOP OF FORM is released, the clock falls and flip-flop LFEF sets. The paper advance operation is then initiated in the manner described for the PAPER STEP switch operation.

4-260 PRINT CYCLE INITIATE

4-261 The PAPER STEP and TOP OF FORM switches are normally inoperative in on-line operation, but the printer cannot be placed off-line until all data in memory is printed. If an incomplete or interrupted transmission of data, consisting of less than 20 characters and no control character is received, a print cycle cannot be initiated. Thus the reset conditions for flip-flop ONLINE cannot be satisfied until a print cycle or master clear operation is initiated. If it is desired to print the stored data, switch ON LINE/OFF LINE is first set to OFF LINE and either switch PAPER STEP or TOP OF FORM is then pressed and released.

4-262 When switch ON LINE/OFF LINE is set to OFF LINE, signal RN2 momentarily goes low, is inverted by A6Z8B and the reset input to flip-flop RUN goes high. On the next clock, flip-flop RUN resets and the set input to flip-flop LFEF goes high.

4-263 When either switch PAPER STEP or TOP OF FORM is pressed and released, flip-flop LFEF sets. The set input to either flip-flop LFFF or FFFF goes high. Signal SPSE is also high and applied to NAND gate Z8A.

4-264 On the next clock, flip-flop LFFF or FFFF sets and PFCM goes high. PFCM is applied to NOR gate A4Z17D and CONT goes high, enabling gate Z8A. The set input to flip-flop SCEF then goes true and on the next clock flip-flop SCEF sets, initiating a scan and print operation.

4-265 On completion of the scan and print operation, the output of NAND gate A4Z18B goes low and initiates a paper advance operation. During the paper advance operation, MPEF(K) goes high, enables NOR gate A4Z16A and MPLD\* goes low. MPLD\* is applied to NAND gate Z7A and gate output LDFF(J) goes high. The reset conditions for flip-flop ONLINE are now satisfied and on the next clock (2CLK), flip-flop ONLINE resets and the printer goes off-line.

SECTION V  
MAINTENANCE AND TROUBLESHOOTING

5-1     INTRODUCTION

5-2     This section contains maintenance and troubleshooting information.

5-3     Maintenance information includes inspection, preventive maintenance, maintenance test, calibration, mechanical adjustments, and removal and replacement procedures for proper field maintenance of the printer.

5-4     Troubleshooting instructions are used in conjunction with the performance checkout procedure, and consists of isolating a trouble to an assembly or card type. Any trouble or suspected trouble encountered during printer operation requires that the checkout procedure be performed.

5-5     Figures 5-1 through 5-3 are provided as maintenance aids. Logic diagrams and schematics are contained in section VI. Figure 5-1 lists major assemblies and their reference designations. Figure 5-2 lists the location of circuit cards. Figure 5-3 lists power transformer taps for various AC inputs.

5-6     INSPECTION AND PREVENTIVE MAINTENANCE

5-7     Scheduled items of inspection and preventive maintenance are listed in table 5-1.

5-8     MAINTENANCE TEST

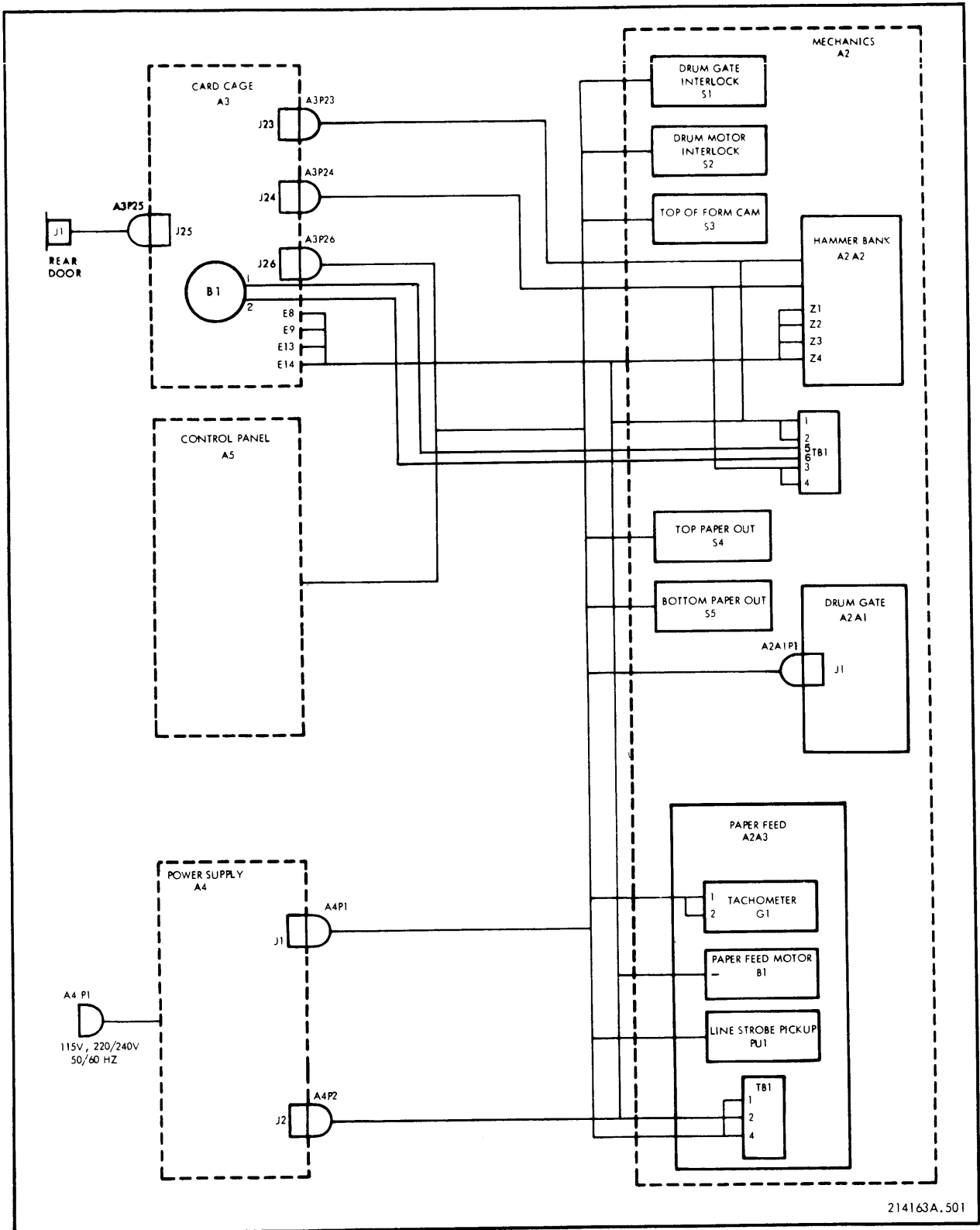
5-9     The maintenance test, consisting of preliminary and performance checkout procedures, is performed to ensure that the printer meets performance standards. The maintenance test should be performed following initial installation, maintenance, extended periods of nonoperation, and after calibration. The maintenance test may also be performed as a basis for troubleshooting when printer trouble exists.

5-10    EQUIPMENT REQUIRED

5-11    Test equipment and special tools required for maintenance are listed in table 5-2.

5-11A   PRINTER INSPECTION

5-11B   Printer electronic and mechanical inspection procedures are performed in accordance with the following paragraphs.



214163A.501

Figure 5-1. LINE/PRINTER Model 2310 Interconnecting Diagram

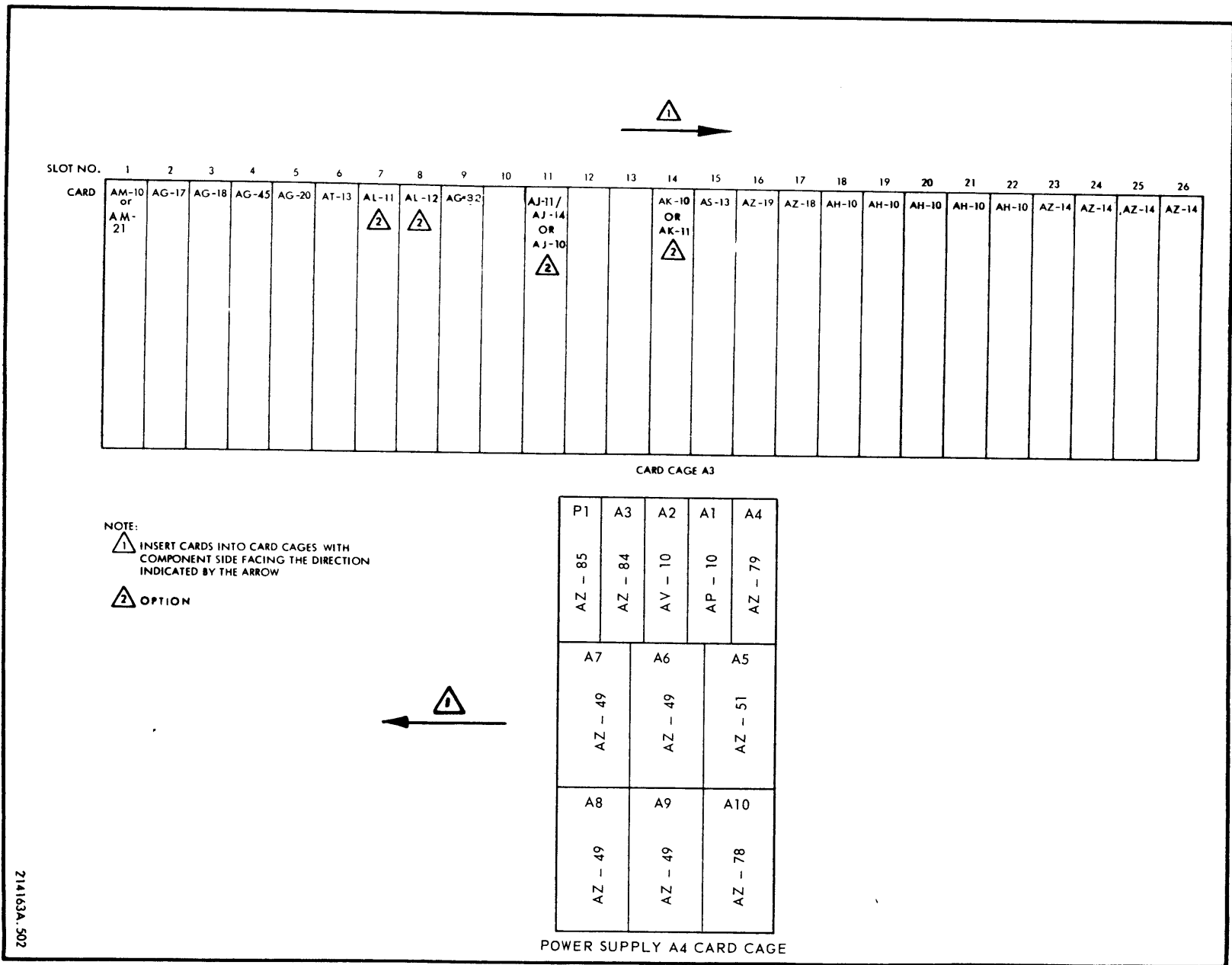
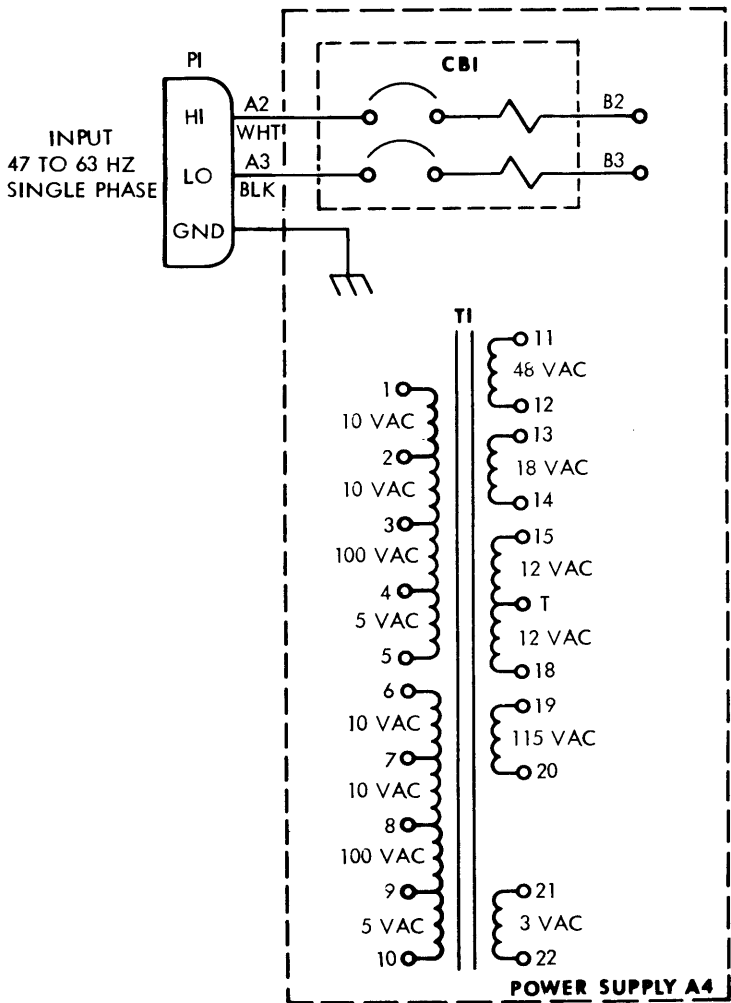


Figure 5-2. Card Location Chart



FOR INPUT VOLTAGE OF	WIRE CB1-B2 TO	WIRE CB1-B3 TO	JUMPER	
			FROM	TO
100	T1-3	T1-4	T1-3	T1-8
			T1-4	T1-9
105	T1-3	T1-5	T1-3	T1-8
			T1-5	T1-10
110	T1-2	T1-4	T1-2	T1-7
			T1-4	T1-9
115	T1-2	T1-5	T1-2	T1-7
			T1-5	T1-10
120	T1-1	T1-4	T1-1	T1-6
			T1-4	T1-9
125	T1-1	T1-5	T1-1	T1-6
			T1-5	T1-10
200	T1-3	T1-9	T1-4	T1-8
210	T1-2	T1-9	T1-4	T1-8
220	T1-1	T1-9	T1-4	T1-8
230	T1-1	T1-9	T1-4	T1-7
240	T1-1	T1-9	T1-4	T1-6
250	T1-1	T1-10	T1-5	T1-6

Figure 5-3. Power Transformer A4T1 Primary Winding Wiring Diagram

TABLE 5-1. INSPECTION AND PREVENTIVE MAINTENANCE SCHEDULE

FREQUENCY	DESCRIPTION	PARAGRAPH REFERENCE
Daily	Cleaning	5-11F(a) (1), 5-11F(b)
Weekly	Mechanical Inspection	5-11D(a) (1), 5-11D(b)
Weekly	Cleaning	5-11F(c), 5-11F(d), 5-11F(e)
Bi-Monthly	Electronic Inspection	5-11C
Monthly	Mechanical Inspection	5-11D(a) (2), 5-11D(a) (3), 5-11D
Monthly	Lubrication	5-11H
Monthly	Electronic Inspection	5-11C(c), 5-11C(d)
Semi Annually	Mechanical Inspection	5-11D(d)

Item	Name	Manufacturer	Part No. or Model	Alternate	Use and Application
1	Digital multimeter	Data Technology	DT360	Commercial equivalent	Measures power supply A4 output voltages
2	Oscilloscope with 1A2 dual-trace plug-in unit	Tektronix	545B	Commercial equivalent	Checks receiver and driver reference voltages and hammer driver current and hammer flight time waveforms
3	Probe 10X	Tektronix	P6006 with 013-0071-00 and 206-0134-03 screw-on tips and ground lead	Commercial equivalent	Used with oscilloscope
4	Card extractor	Flowtron	DPC 800258-001	Model 30, A series 4 $\frac{1}{4}$ x 4-3/4	Extracts cards for troubleshooting
5	Extender board	DPC	DPC 800580-001	None	Extends cards for troubleshooting
6	Mechanical force gauge	Hunter Division of Amtek	Type L-30M, 0-30 pounds	Commercial equivalent	Sets paper drive and drum motor belt tension
6A	Self Test Card A132	DPC	230240	None	Exercises printer for testing printer operation. Refer to section 7 for operating procedure.

Table 5-2. Test Equipment and Special Tools Required



Item	Name	Manufacturer	Part No. or Model	Alternate	Use and Application
7	Preset torque screwdriver	Hank Thron	DPC T-2267 Preset to 4.8-5 inch-pounds	Commercial equivalent	Remove and replace hammer modules
8	Allen driver 5/64	Hunter	5B	Commercial equivalent	Adjust hammer flight time
9	Tractor alignment gauge	DPC	DPC T-2308	None	Align tractor sprocket pins
10	Thickness gauge	Starett	66	Commercial equivalent	Adjust line strobe, character, and index pickups and paper tension bar
11	Spring (gram) gauge	Hunter	0-200 grams	Commercial equivalent	Adjust paper tension springs
12	Wire wrap gun (battery operated) with 30 gauge bit	Gardner Denver	14R2 with 507063 bit	Commercial equivalent	Replace card cage jumper wires
13	Unwrap tool	Gardner Denver	505084-491	Commercial equivalent	Remove card cage jumper wires
14	Taper pin removal tool	AMP	91012-2	Commercial equivalent	Remove hammer assembly taper pins
15	Taper pin insertion tool	AMP	811167-1 with F395005 tip	Commercial equivalent	Replace hammer assembly taper pins
16	Taper pin removal tool	AMP	91012-1	Commercial equivalent	Remove hammer bank jumpers
17	Taper pin insertion tool	AMP	380310-4 with G395042 tip	Commercial equivalent	Replace hammer bank jumpers

Table 5-2. Test Equipment and Special Tools Required (Continued)

5-11C Electronic Inspection. Electronic inspection consists of the following steps:

- (a) Apply printer power.
- (b) Check operator's panel indicator lamps. Replace any lamp that does not illuminate.
- (c) Check power supply calibration and perform any necessary adjustments.
- (d) Check +12V Monitor.

CAUTION

If during this check the +12V interlock stays high, turn power off immediately. Remove +12V fuse, F2, from power supply and verify that the +12V interlock, A3A16-11, goes to 0V.

5-11D Mechanical Inspection. Mechanical inspection consists of the following steps:

- (a) Printout. Check a shift test pattern and horizontal and vertical hammer phasing.

NOTE

A shift test pattern consists of a repetitive printout where all characters are printed in one line, and the characters are then shifted one position to the left for each succeeding line. For example:

1st LINE: A B C D E (etc. for a full line)  
2nd LINE: B C D E F (etc. for a full line)  
3rd LINE: C D E F G (etc. for a full line)

(1) Shift Test. Set up data source to execute an 80 column shift test routine, and check for correct printout (as described in preceding note).

(2) Vertical Hammer Phasing. Print out several lines of the character "E" and check for the following discrepancies:

a. If the tops or bottoms of all characters appear faint or are missing, correct by performing the character sync pulse phasing procedure.

b. If one or more characters are slightly out of line with other characters, correct by performing the hammer adjustment procedure.

(3) Horizontal Hammer Phasing. Print out one 80-column line of the character "H".

a. Check the entire line to determine if consistent clipping of character sides occurs. If this fault occurs, perform horizontal adjustment of hammer bank.

(b) Ribbon. Check sample of last printout for adequate ink transfer, also check ribbon for tearing or stretching. If ribbon does not warrant changing, switch ribbon spools (end for end); this will increase the life of the ribbon.

(c) Tractors. Check tractors for alignment and tension.

(d) Belts. Check belts for wear and tension.

#### 5-11E PRINTER CLEANING

5-11F Cleaning is performed periodically in accordance with the following paragraphs:

(a) Cabinet. Using damp cloth, wipe off any dust, stains, or fingerprints.

(b) Window. Using damp cloth, clean print-out viewing window.

(c) Printer Mechanics. Remove ribbon spools and use vacuum cleaner and damp cloth to clean printer mechanics area of paper dust.

(d) Character Drum. Frequency of cleaning the character drum depends upon the extent of printer activity. This may best be determined by inspection of printout quality and inspection of the drum itself. Recommended frequency of cleaning is every 20 hours of actual printing. Clean with isopropyl alcohol using stiff bristle brush. Place cloth beneath drum to prevent solvent contact with painted parts.

(e) Ribbon Guide. The ribbon guide should be cleaned at the same time the character drum is cleaned by wiping with a cloth dampened with isopropyl alcohol.

#### 5-11G PRINTER LUBRICATION

5-11H The only lubrication required is the periodic application of a silicone-type dry spray to areas such as splined shafts and paper position adjustments.

5-12 PRELIMINARY CHECKOUT PROCEDURE

5-13 Perform steps in table 5-3 in the order given. If an abnormal indication is observed, refer to the applicable step in troubleshooting table 5-6 for corrective action.



Do not operate power supply A4 outside of printer cabinet without connecting a ground lead between power supply chassis and printer frame.

Table 5-3. Preliminary Checkout Procedure

Step	Procedure	Normal Indication	Table 5-6 Step
a	Open printer cabinet front door; set circuit breaker CB1 to OFF and PRINT INHIBIT switch to down position		
b	Open printer cabinet rear door; swing card cage A3 out to 90° position.		
c	Ensure all cards are correctly located and seated securely		
d	Connect primary power cable plug A4P1 to ac power source		
e	Set circuit breaker CB1 to ON  Note  Perform steps f and g if printer does not have paper	POWER indicator lights	1
f	Ensure PAPER FAULT indicator lights		2
g	Unlatch and swing open drum gate A2A1  Note  Perform step h if printer does not have ribbon  Caution  Wait for line printer drum to stop rotating before proceeding to the next step.	DRUM GATE indicator lights	3

Table 5-3. Preliminary Checkout Procedure (Continued)

Step	Procedure	Normal Indication	Table 5-6 Step
h	Install ribbon per ribbon installation procedure in section III		
i	Load paper per paper loading procedure in section III		
j	Close and latch drum gate A2A1	DRUM GATE indicator goes out READY indicator lights after 10 (+2) seconds	4
k	Press and release TOP OF FORM switch	Paper moves to top-of-form	5
l	Press and release PAPER STEP switch	Paper advances one line	6
m	Set PRINT INHIBIT switch to up position	PRINT INHIBIT indicator lights	7
n	Set PRINT INHIBIT switch to down position	PRINT INHIBIT indicator goes out	

## 5-14 PERFORMANCE CHECKOUT PROCEDURE

5-15 Perform steps in table 5-4 in the order given. If an abnormal indication is observed, refer to the applicable step in troubleshooting table 5-6 for corrective action. Do not continue performance checkout procedure until the trouble is corrected. After a trouble is corrected, repeat all steps previously performed.

5-16 In the performance checkout and calibration procedures, test connections to card test points are called out as follows:

Sample Callout

A3-11X

Definition

A3 = Card cage A3

11 = Card location  
(slot)

X = Card test point

Test	Step	Procedure	Normal Indication	Table 5-6 Step
1		POWER SUPPLY A4 OUTPUT VOLTAGE CHECK  NOTE  For access to power supply A4 test jacks, unlatch and swing card cage A3 out to 90° position.	NOTE	
	a	Connect lead from digital multimeter (DVOM) (1, table 5-2) COM jack to test jack TP6 (GND) on rear of power supply A4 (figure 5-4); press DC function switch and range switch 200	Line voltage tolerances can influence -12 volts and +65 volts output indications. Tolerances specified in procedure assume primary power input as specified in table 1-1	
	b	Connect lead between DVOM VOLTS jack and test jack TP1 (+65v)	DVOM indicates +65 ( <u>±</u> 6.5) volts	8
	c	Remove lead from test jack TP1; connect to test jack TP4 (+28v)	DVOM indicates +28 ( <u>±</u> 0.1) volts	9
	d	Remove lead from test jack TP4; connect to test jack TP7 (+22v)	DVOM indicates +22 ( <u>±</u> 3) volts	1
	e	Remove lead from test jack TP7; connect to test jack TP2 (+12v)		
	f	Press DVOM range switch 20	DVOM indicates +12 ( <u>±</u> 0.01) volts	10
	g	Remove lead from test jack TP2; connect to test jack TP3 (+5v)	DVOM indicates +5 ( <u>±</u> 0.01) volts	11
	h	Remove lead from test jack TP3; connect to test jack TP5 (-12v)	DVOM indicates between -12 and -16 volts	12
	i	Remove DVOM leads from power supply A4 test jacks		

Table 5-4. Performance Checkout Procedure

Test	Step	Procedure	Normal Indication	Table 5-6 Step																		
2	a	<p>DRIVER A3A11 REFERENCE VOLTAGE CHECK</p> <p>Note</p> <p>Verify calibration of oscilloscope before using. Insert probe into CAL OUT jack; rotate AMPLITUDE CALIBRATOR through several settings and insure that undistorted square-wave output of correct amplitude appears. Adjust oscilloscope and probe if necessary.</p> <p>Set oscilloscope (2, table 5-2) controls and switches as follows:</p> <table border="1" data-bbox="457 922 982 1219"> <thead> <tr> <th><u>Switch or Control</u></th> <th><u>Setting</u></th> </tr> </thead> <tbody> <tr> <td>MODE</td> <td>CH1</td> </tr> <tr> <td>VOLTS/CM</td> <td>.5</td> </tr> <tr> <td>VARIABLE</td> <td>CALIBRATED</td> </tr> <tr> <td>STABILITY</td> <td>full clockwise</td> </tr> <tr> <td>TRIGGERING LEVEL</td> <td>full clockwise</td> </tr> <tr> <td>TRIGGERING MODE</td> <td>AC</td> </tr> <tr> <td>TRIGGER SLOPE</td> <td>INT +</td> </tr> <tr> <td>AC-DC-GND</td> <td>DC</td> </tr> </tbody> </table>	<u>Switch or Control</u>	<u>Setting</u>	MODE	CH1	VOLTS/CM	.5	VARIABLE	CALIBRATED	STABILITY	full clockwise	TRIGGERING LEVEL	full clockwise	TRIGGERING MODE	AC	TRIGGER SLOPE	INT +	AC-DC-GND	DC		
<u>Switch or Control</u>	<u>Setting</u>																					
MODE	CH1																					
VOLTS/CM	.5																					
VARIABLE	CALIBRATED																					
STABILITY	full clockwise																					
TRIGGERING LEVEL	full clockwise																					
TRIGGERING MODE	AC																					
TRIGGER SLOPE	INT +																					
AC-DC-GND	DC																					
	b	Connect CHANNEL 1 probe (3, table 5-2) to A3-11X, and probe ground lead to A3-11Z	Oscilloscope displays 1 cm (+5.0V) deflection if logic 1 equals +5 volts	13																		
	c	Remove probe from A3-11X and A3-11Z	<p>Note</p> <p>Voltage displayed at A3-11X is always equal to logic 1 voltage level</p>																			

Table 5-4. Performance Checkout Procedure (Continued)

Test	Step	Procedure	Normal Indication	Table 5-6 Step																	
3		RECEIVER A3A14 REFERENCE VOLTAGE CHECK																			
	a	Set oscilloscope (2, table 5-2) controls and switches as follows:																			
		<table border="0"> <thead> <tr> <th><u>Switch or Control</u></th> <th><u>Setting</u></th> </tr> </thead> <tbody> <tr> <td>MODE</td> <td>CH1</td> </tr> <tr> <td>VOLTS/CM</td> <td>.5</td> </tr> <tr> <td>VARIABLE</td> <td>CALIBRATED</td> </tr> <tr> <td>STABILITY</td> <td>full clockwise</td> </tr> <tr> <td>TRIGGERING LEVEL</td> <td>full clockwise</td> </tr> <tr> <td>TRIGGERING MODE</td> <td>AC</td> </tr> <tr> <td>TRIGGER SLOPE</td> <td>INT +</td> </tr> <tr> <td>AC-DC-GND</td> <td>DC</td> </tr> </tbody> </table>	<u>Switch or Control</u>	<u>Setting</u>	MODE	CH1	VOLTS/CM	.5	VARIABLE	CALIBRATED	STABILITY	full clockwise	TRIGGERING LEVEL	full clockwise	TRIGGERING MODE	AC	TRIGGER SLOPE	INT +	AC-DC-GND	DC	<p>NOTE</p> <p>Voltage displayed at A3-14M is always equal to <math>\frac{1}{2}</math> of logic 1 voltage level.</p>
<u>Switch or Control</u>	<u>Setting</u>																				
MODE	CH1																				
VOLTS/CM	.5																				
VARIABLE	CALIBRATED																				
STABILITY	full clockwise																				
TRIGGERING LEVEL	full clockwise																				
TRIGGERING MODE	AC																				
TRIGGER SLOPE	INT +																				
AC-DC-GND	DC																				
4	b	Connect CHANNEL 1 probe to A3-14M, and probe ground lead to A3-14Z	Oscilloscope displays 0.5 cm (+2.5V) deflection if logic 1 equals +5 volts	14																	
	c	Remove probe from A3-14M and A3-14Z HAMMER DRIVER CURRENT CHECK																			
	a	Set circuit breaker CB1 to OFF																			
	b	Set oscilloscope switches and controls as follows:																			
		<table border="0"> <thead> <tr> <th><u>Switch or Control</u></th> <th><u>Setting</u></th> </tr> </thead> <tbody> <tr> <td>VOLTS/CM</td> <td>.1</td> </tr> <tr> <td>TIME/CM</td> <td>.5 mSEC</td> </tr> <tr> <td>VARIABLE</td> <td>CALIBRATED</td> </tr> </tbody> </table> <p style="text-align: center;"><b>CAUTION</b></p> <p>Ensure probe ground lead is connected to side of resistor shown in figure 5-5.</p>	<u>Switch or Control</u>	<u>Setting</u>	VOLTS/CM	.1	TIME/CM	.5 mSEC	VARIABLE	CALIBRATED											
<u>Switch or Control</u>	<u>Setting</u>																				
VOLTS/CM	.1																				
TIME/CM	.5 mSEC																				
VARIABLE	CALIBRATED																				

Table 5-4. Performance Checkout Procedure (Continued)



Test	Step	Procedure	Normal Indication	Table 5-6 Step
4		<p>HAMMER DRIVER CURRENT CHECK (Continued)</p> <p>c Connect CHANNEL 1 probe and ground lead across resistor R112 as shown in figure 5-5</p> <p>d Set circuit breaker CB1 to ON</p> <p>e Set ONLINE/OFFLINE switch to ON LINE and release; ensure ON LINE indicator lights</p> <p>NOTE</p> <p>Refer to section VII for AL-14 card operating procedure.</p> <p>f Enter E pattern from self test AL-14 card or user system to start print cycle</p> <p>g Remove probe from across resistor R112</p>		
5	a	<p>PRINTOUT QUALITY CHECK</p> <p>Enter E pattern from self test AL-14 card or user system; print one form</p>	<p>Printout quality is similar to figure 5-7</p>	16

Table 5-4. Performance Checkout Procedure (Continued)

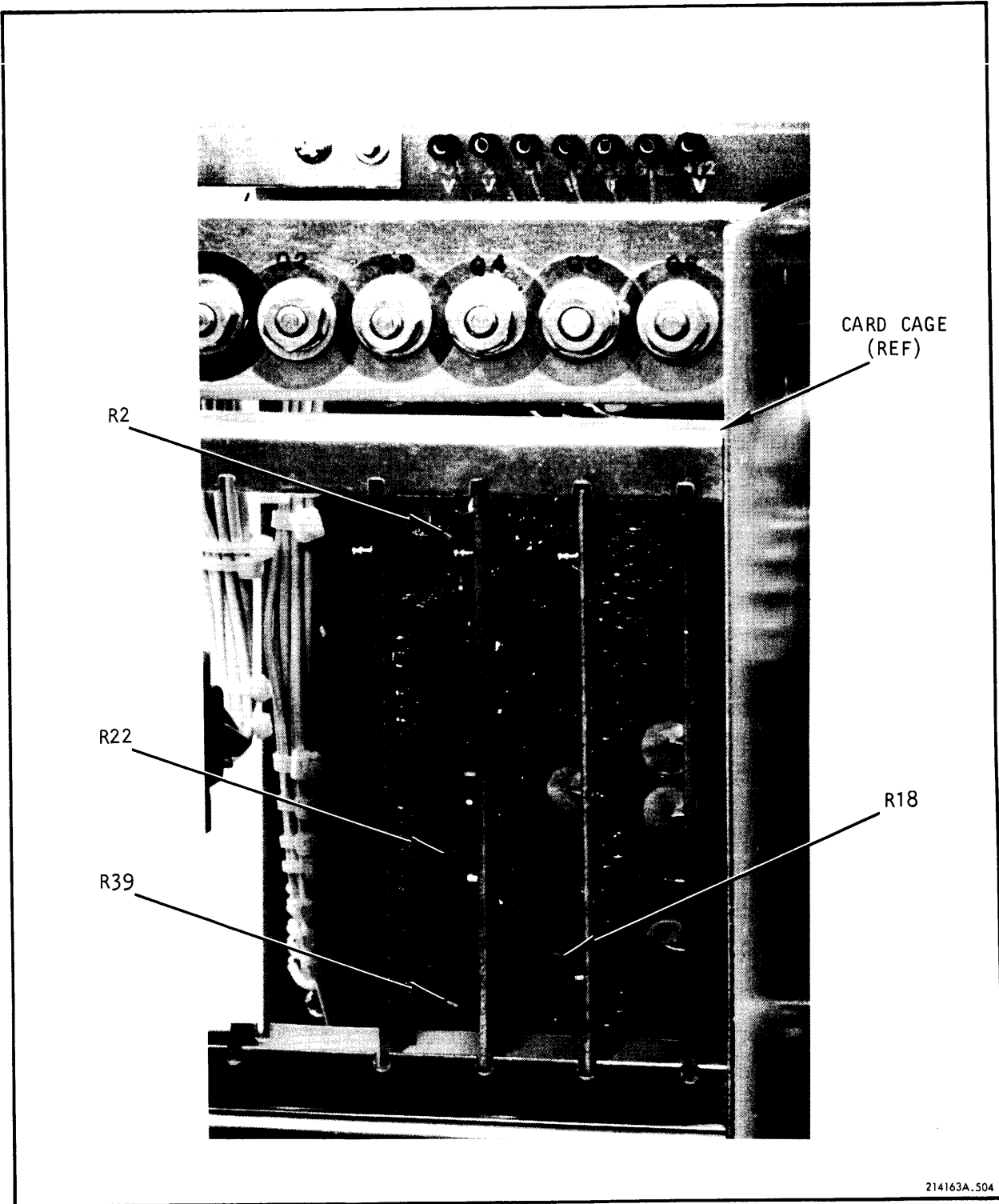


Figure 5-4. Power Supply A4, Test Jacks and Adjustment Locations

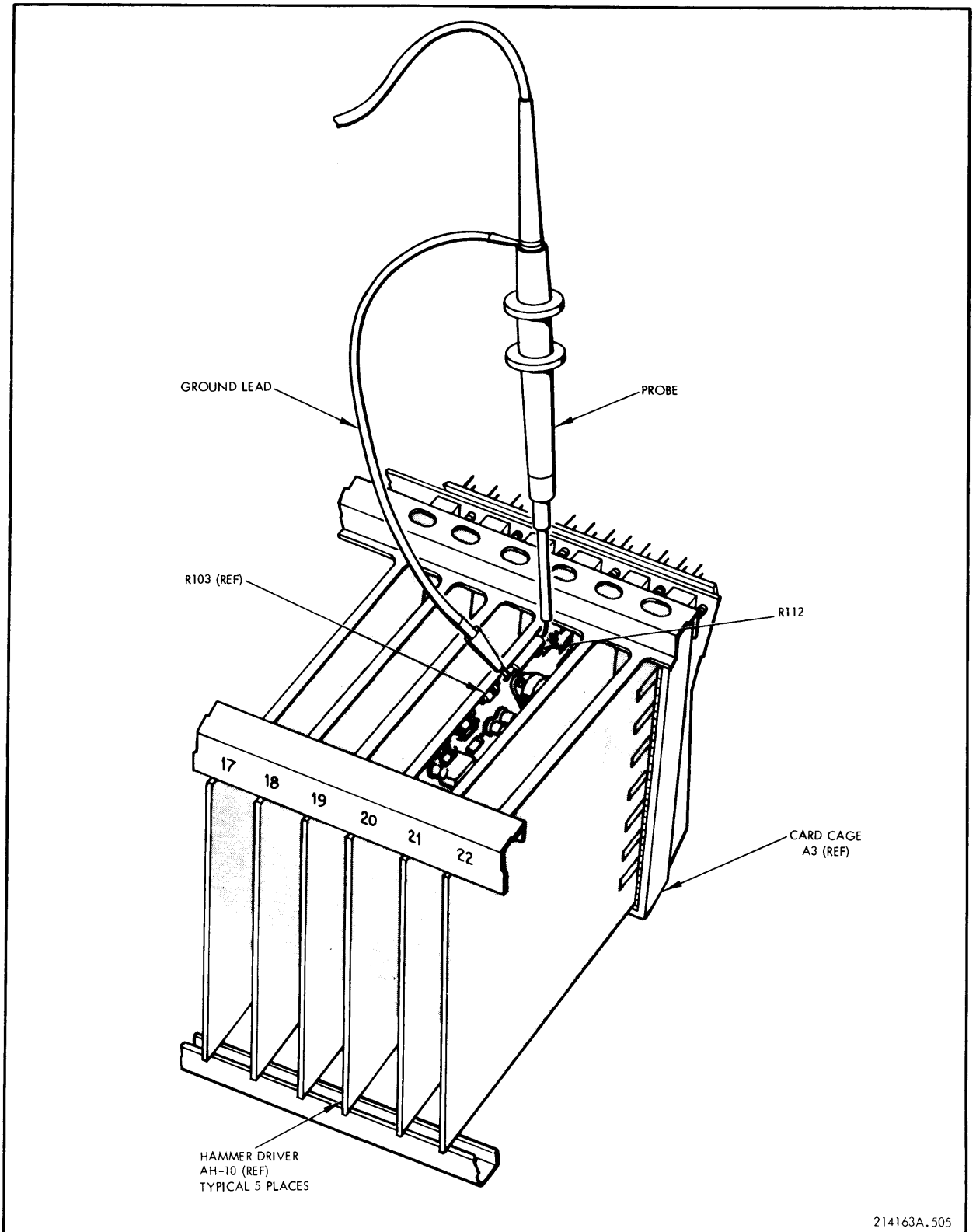
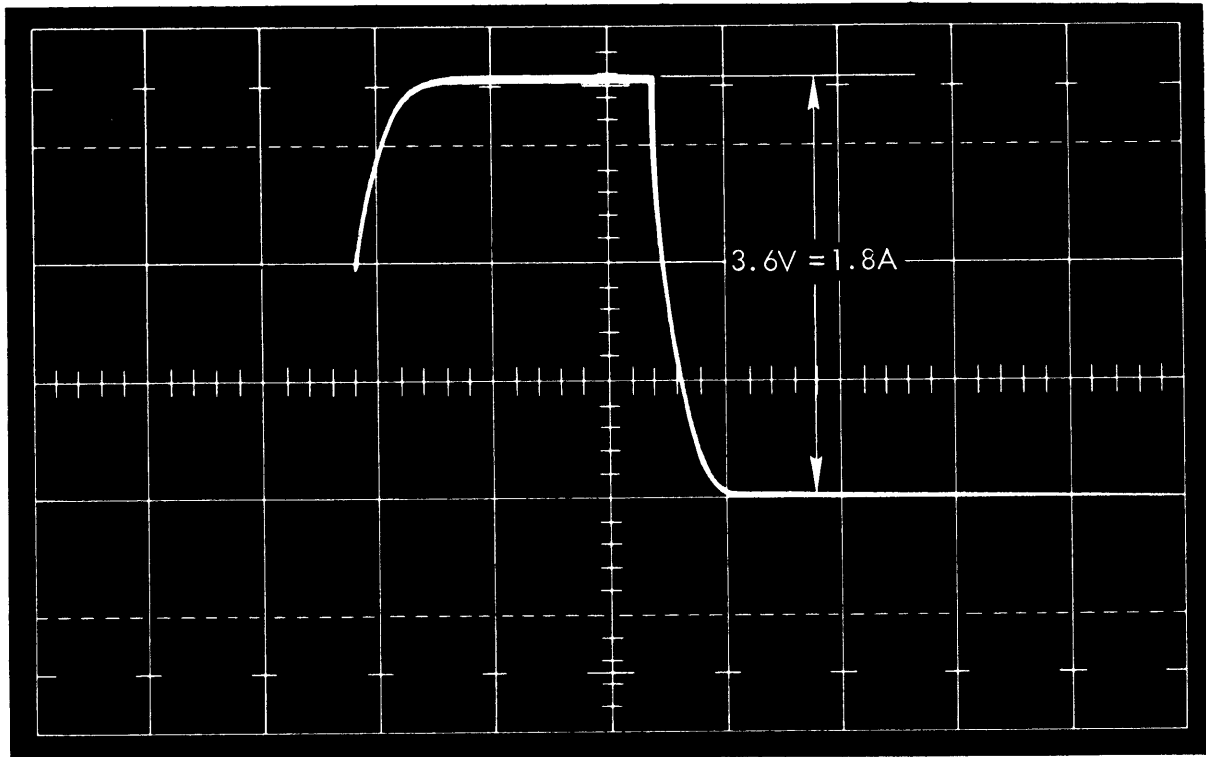


Figure 5-5. Hammer Driver Current Test Probe Connection



214163A.506

Figure 5-6. Hammer Driver Current Waveform

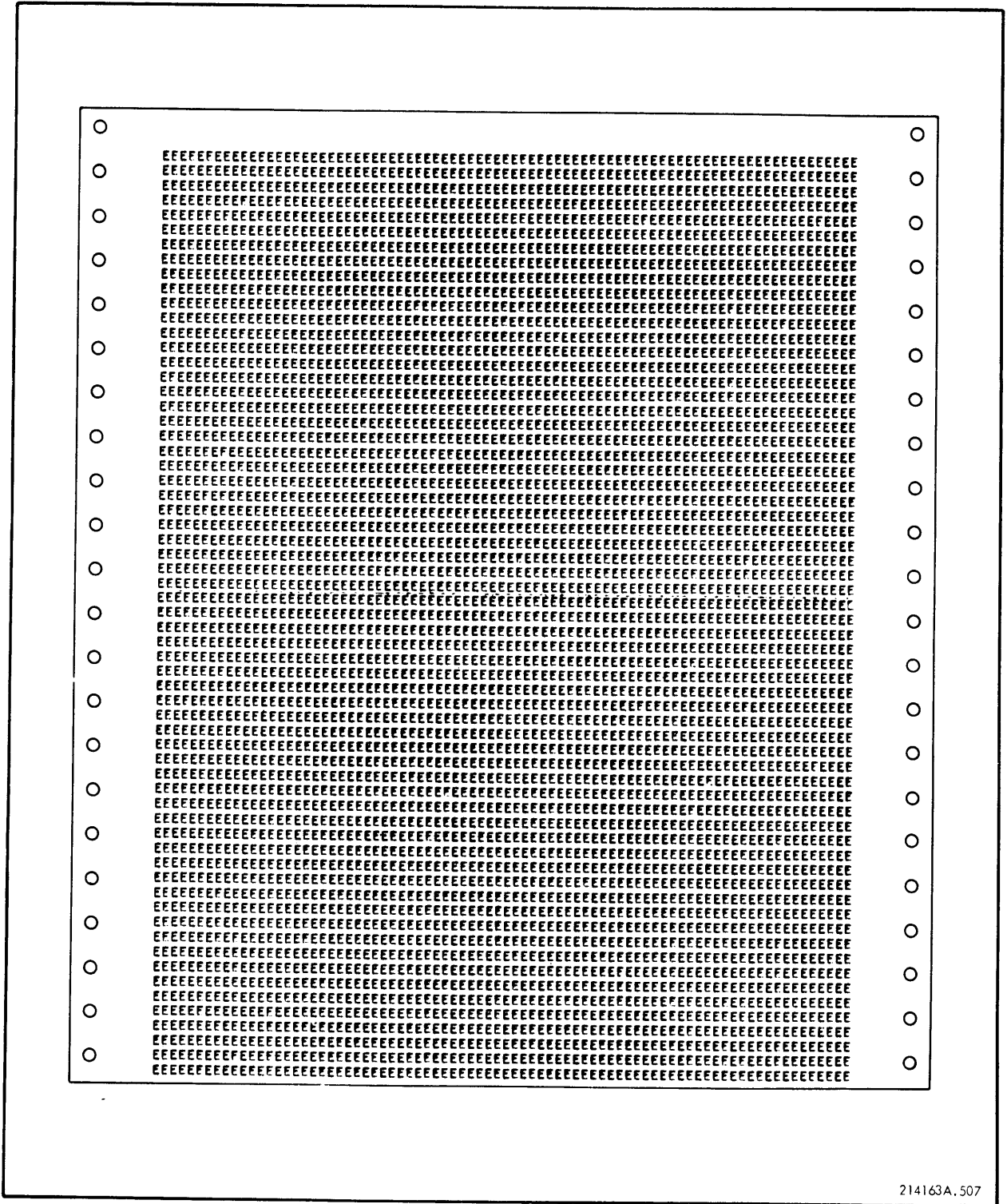


Figure 5-7. Printout Quality Check

5-17 CALIBRATION

5-18 The printer does not require periodic calibration. Calibration procedures should be performed only when indicated as a possible remedy for a printer trouble and, if applicable, after rework or repair. Refer to section VII for self test AL-27 card operating procedure.

Note

Verify calibration of oscilloscope when use is required. Insert probe into CAL OUT jack; rotate AMPLITUDE CALIBRATOR through several settings and insure that undistorted squarewave output of correct amplitude appears. Adjust oscilloscope and probe if necessary.

5-19 CALIBRATION OF POWER SUPPLY A4

5-20 +5V Calibration

5-21 Calibrate +5V supply as follows:

- a. Connect lead from digital multimeter (DVOM) (1, table 5-2) COM jack to GRD test jack on rear of power supply A4 (figure 5-4).
- b. Press DVOM DC function switch and range switch 20.
- c. Connect lead between DVOM VOLTS jack and power supply A4 +5V test jack.
- d. Adjust potentiometer R2 (figure 5-4) as required to obtain DVOM indication of +5 ( $\pm 0.01$ ) volts.
- e. Remove DVOM leads from power supply A4.

5-22 +12V Calibration

5-23 Calibrate +12V supply as follows:

- a. Connect lead from digital multimeter (DVOM) (1, table 5-2) COM jack to GRD test jack on rear of power supply A4 (figure 5-4).
- b. Press DVOM DC function switch and range switch 20.
- c. Connect lead between DVOM VOLTS jack and power supply A4 +12V test jack.
- d. Adjust potentiometer R22 (figure 5-4) as required to obtain DVOM indication of +12 ( $\pm 0.01$ ) volts.
- e. Remove DVOM leads from power supply A4.

5-24 +28V Calibration

5-25 Perform +12V calibration and calibrate +28V supply as follows:

- a. Connect lead from digital multimeter (DVOM) (1, table 5-2) COM jack to GRD test jack on rear of power supply A4 (figure 5-4).
- b. Press DVOM DC function switch and range switch 200.
- c. Connect lead between DVOM VOLTS jack and power supply A4 +28V test jack.
- d. Adjust potentiometer R39 (figure 5-4) as required to obtain DVOM indication of +28 ( $\pm 0.1$ ) volts.
- e. Remove DVOM leads from power supply A4.

5-26 CALIBRATION OF DRIVER A3A11 REFERENCE VOLTAGE

5-27 Calibrate driver A3A11 reference voltage as follows:

- a. Set oscilloscope (2, table 5-2) controls and switches as follows:

<u>Switch or Control</u>	<u>Setting</u>
MODE	CH1
VOLTS/CM	.5
VARIABLE	CALIBRATED
STABILITY	full clockwise
TRIGGERING LEVEL	full clockwise
TRIGGERING MODE	AC
TRIGGER SLOPE	INT+
AC-DC-GND	DC

- b. Connect CHANNEL 1 probe (3, table 5-2) to A3-11X, and probe ground lead to A3-11Z.

c. Adjust potentiometer R1 (figure 5-8) as required to obtain oscilloscope deflection of 1 cm (+5.0V), if logic 1 equals +5 volts.

Note

Potentiometer R1 is always adjusted until the voltage displayed at A3-11X equals the printer logic 1 voltage level.

- d. Remove probe from A3-11X and A3-11Z.

5-28 CALIBRATION OF RECEIVER A3A14 REFERENCE VOLTAGE

5-29 Calibrate receiver A3A14 reference voltage as follows:

- a. Set oscilloscope (2, table 5-2) controls and switches as follows:

<u>Switch or Control</u>	<u>Setting</u>
MODE	CH1
VOLTS/CM	.5
VARIABLE	CALIBRATED
STABILITY	full clockwise
TRIGGERING LEVEL	full clockwise
TRIGGERING MODE	AC
TRIGGER SLOPE	INT +
AC-DC-GND	DC

b. Connect CHANNEL 1 probe (3, table 5-2) to A3-14M, and probe ground lead to A3-14Z.

c. Adjust potentiometer R2(14) (figure 5-8) as required to obtain oscilloscope deflection of 0.5 cm (+2.5V), if logic 1 equals +5 volts.

Note

Potentiometer R2(14) is always adjusted until voltage displayed at A3-14M is equal to 1/2 of the printer logic 1 voltage level.

d. Remove probe from A3-14M and A3-14Z.

5-30 CALIBRATION OF HAMMER DRIVER CURRENT

5-31 Calibrate hammer driver current as follows:

a. Set circuit breaker CB1 to OFF.

b. Set oscilloscope (2, table 5-2) switches and controls as follows:

<u>Switch or Control</u>	<u>Setting</u>
MODE	CH1
TRIGGERING MODE	AC
TRIGGER SLOPE	INT +
VOLTS/CM	.1
TIME/CM	.5 mSEC
VARIABLE	CALIBRATED
AC-DC-GND	DC

**CAUTION**

Ensure probe ground lead is connected to side of resistor shown in figure 5-5.

c. Connect CHANNEL 1 probe (3, table 5-2) and ground lead across resistor R112 as shown in figure 5-5.

d. Set circuit breaker CB1 to ON.

e. Set ON LINE/OFF LINE switch to ON LINE and release; ensure ON LINE indicator lights.



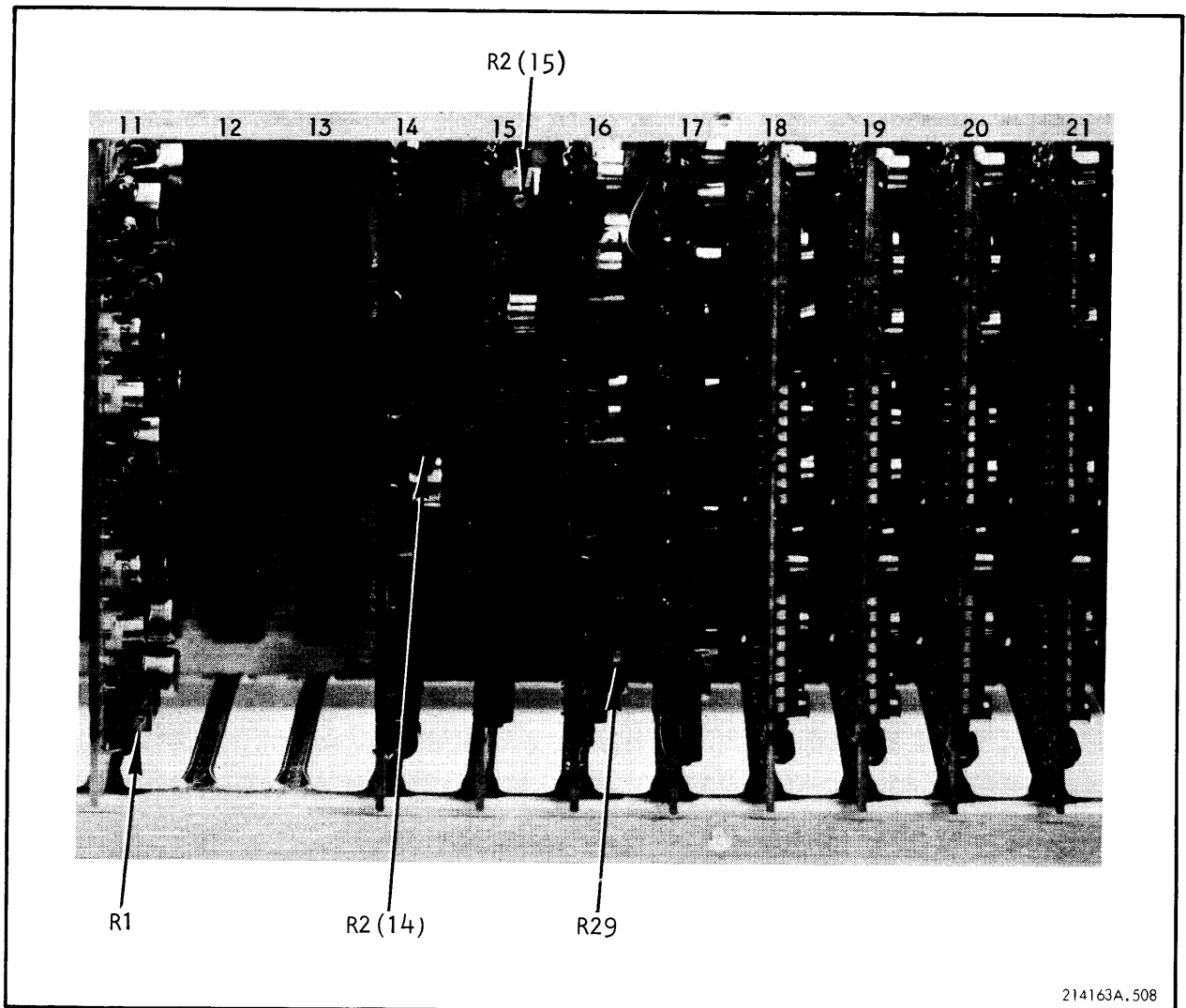
Note

Ensure paper is loaded, ribbon installed, and drum gate closed.

f. Enter E pattern from self test AL-27 card or user system to start print cycle.

g. Adjust potentiometer R29 (figure 5-8) as required to obtain waveform in figure 5-6.

h. Remove probe from across resistor R112.



214163A.508

Figure 5-8. Card Cage A3 Adjustment Locations

5-32 CALIBRATION OF HAMMER FLIGHT TIME

5-33 Calibrate hammer flight time as follows:

a. Set oscilloscope (2, table 5-2) CHANNELS 1 and 2 switches and controls as follows:

<u>Switch or Control</u>	<u>Setting</u>
MODE	CHOP
TRIGGERING MODE	AC
TRIGGER SLOPE	INT +
VOLTS/CM	1
TIME/CM	.2 mSEC
VARIABLE	CALIBRATED
AC-DC-GND	DC

Note

Ensure paper is loaded, ribbon installed, and drum gate closed.

b. Set printer ON LINE/OFF LINE switch to ON LINE position and release; ensure ON LINE indicator lights.

c. Proceed with hammer flight time calibration as follows:

Note

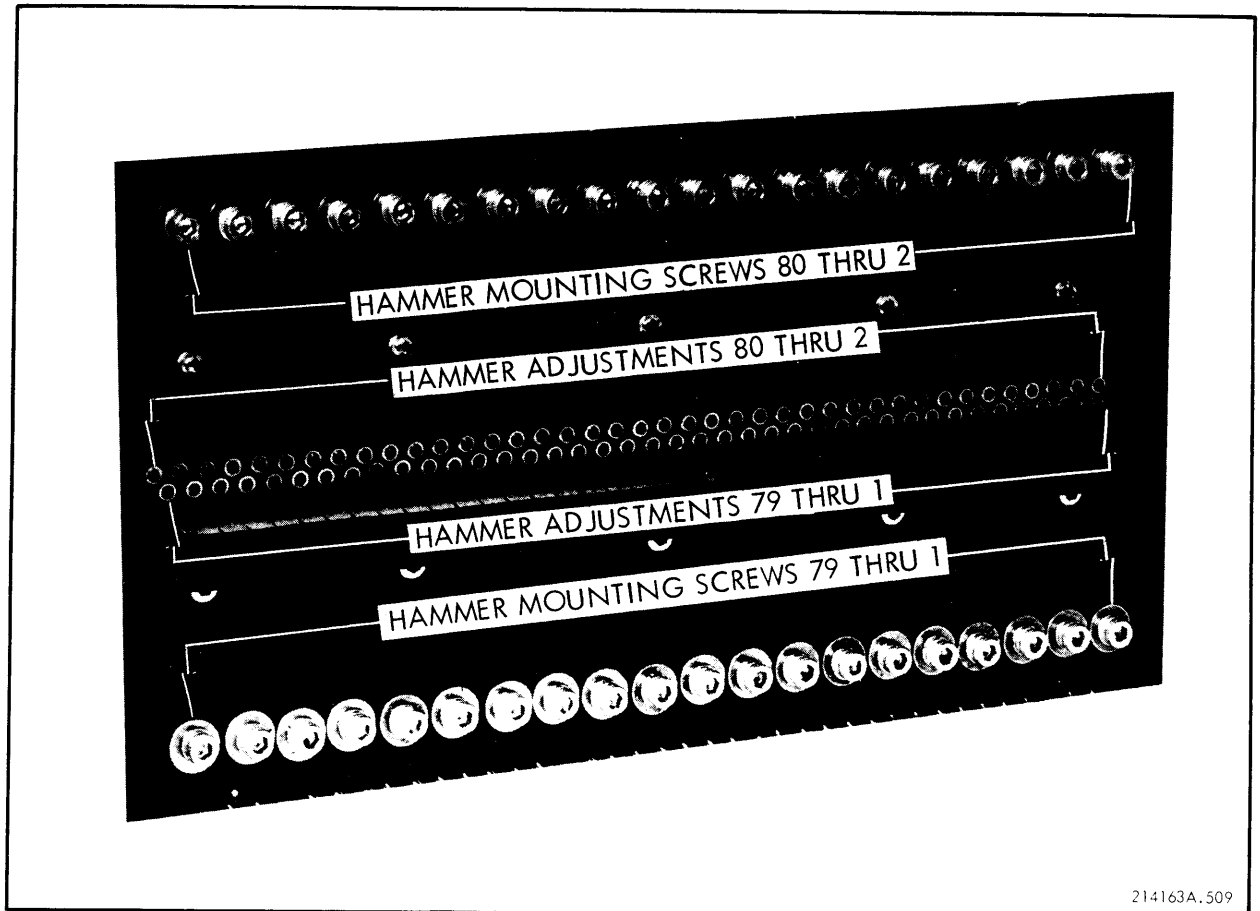
Hammers are adjusted sequentially, starting with number 1 (figure 5-9).

1. Enter E pattern from self test AL-27 card or user system to start print cycle for zone 1 only.

2. Connect CHANNEL 1 probe (3, table 5-2) to A3-22B; connect probe ground lead to A3-22Z.

Note

Use Allen driver (8, table 5-2) for hammer adjustments.



214163A.509

Figure 5-9. Hammer Adjustment and Mounting Screw Locations  
(Hammer Bank, Rear View)

- 5-10. 3. Adjust hammer 1 as necessary to obtain reference waveform in figure 5-10.
4. Set oscilloscope MAGNIFIER switch to 5X.
5. Adjust oscilloscope HORIZONTAL POSITION control until trace A is as shown in figure 5-11.
6. Refer to table 5-5 and connect CHANNEL 2 probe (3, table 5-2) to applicable test point for each hammer adjustment. Connect probe ground lead to A3-20Z.
7. Adjust hammers 2 through 20 until trace B in figure 5-11 is similar and coincident with reference trace A for each individual hammer.
8. Repeat step 1 and add zone 2.

	Zone 1																			
Hammer	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Test Point A3-	22B	22H	22R	22Y	21B	21H	21R	21Y	20B	20H	20R	20Y	19B	19H	19R	19Y	18B	18H	18R	18Y
	Zone 2																			
Hammer	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
Test Point A3-	22B	22H	22R	22Y	21B	21H	21R	21Y	20B	20H	20R	20Y	19B	19H	19R	19Y	18B	18H	18R	18Y
	Zone 3																			
Hammer	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
Test Point A3-	22B	22H	22R	22Y	21B	21H	21R	21Y	20B	20H	20R	20Y	19B	19H	19R	19Y	18B	18H	18R	18Y
	Zone 4																			
Hammer	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
Test Point A3-	22B	22H	22R	22Y	21B	21H	21R	21Y	20B	20H	20R	20Y	19B	19H	19R	19Y	18B	18H	18R	18Y

Table 5-5. Hammer Flight Time Adjustment Test Points

Note

Multiple waveforms will be observed as zones are added.

9. Repeat step 7 for hammers 21 thru 40.
  10. Repeat step 1 and add zone 3.
  11. Repeat step 7 for hammers 41 thru 60.
  12. Repeat step 1 and add zone 4.
  13. Repeat step 7 for hammers 61 thru 80.
- d. Remove probes from card cage A3.

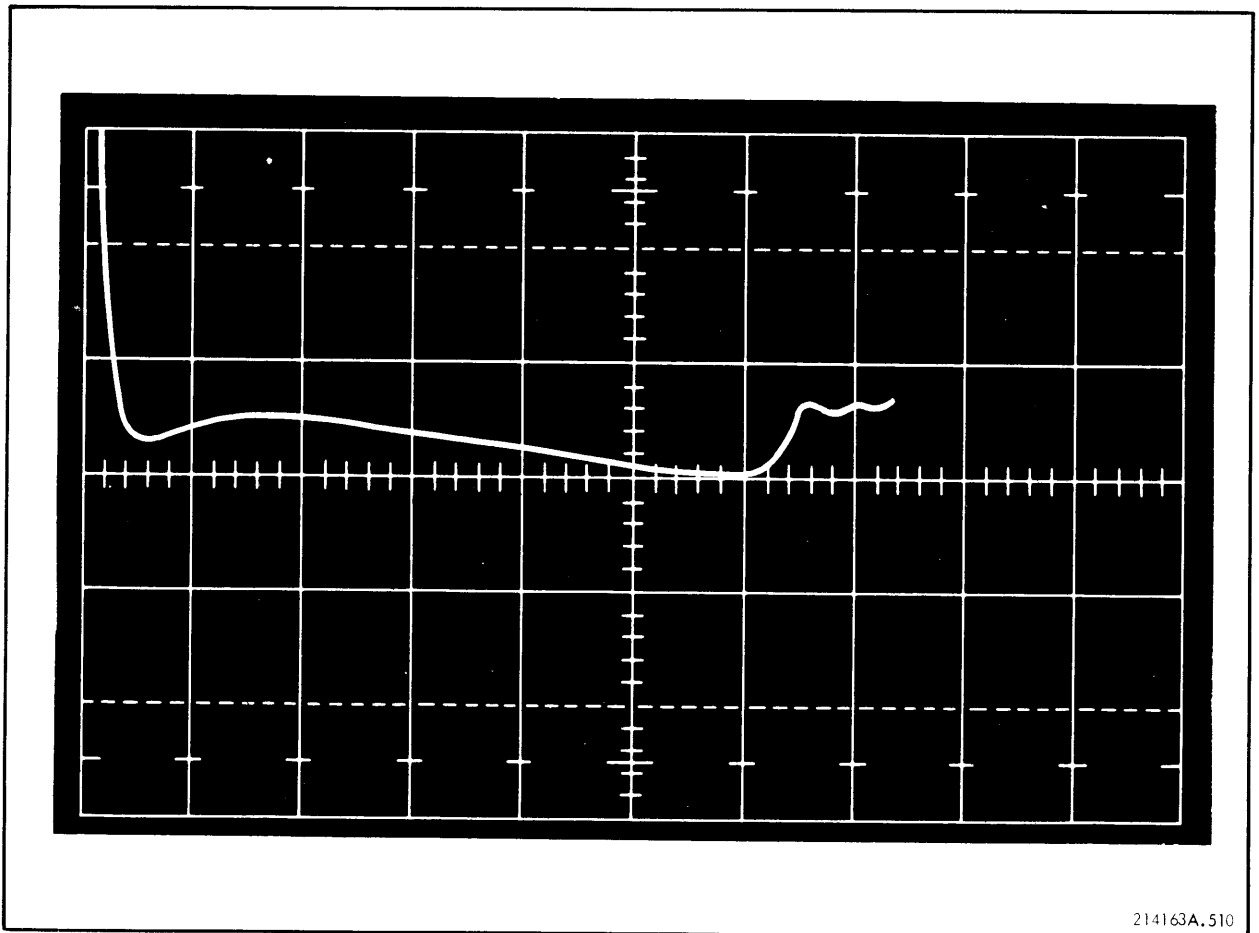


Figure 5-10. Hammer Flight Time Waveform

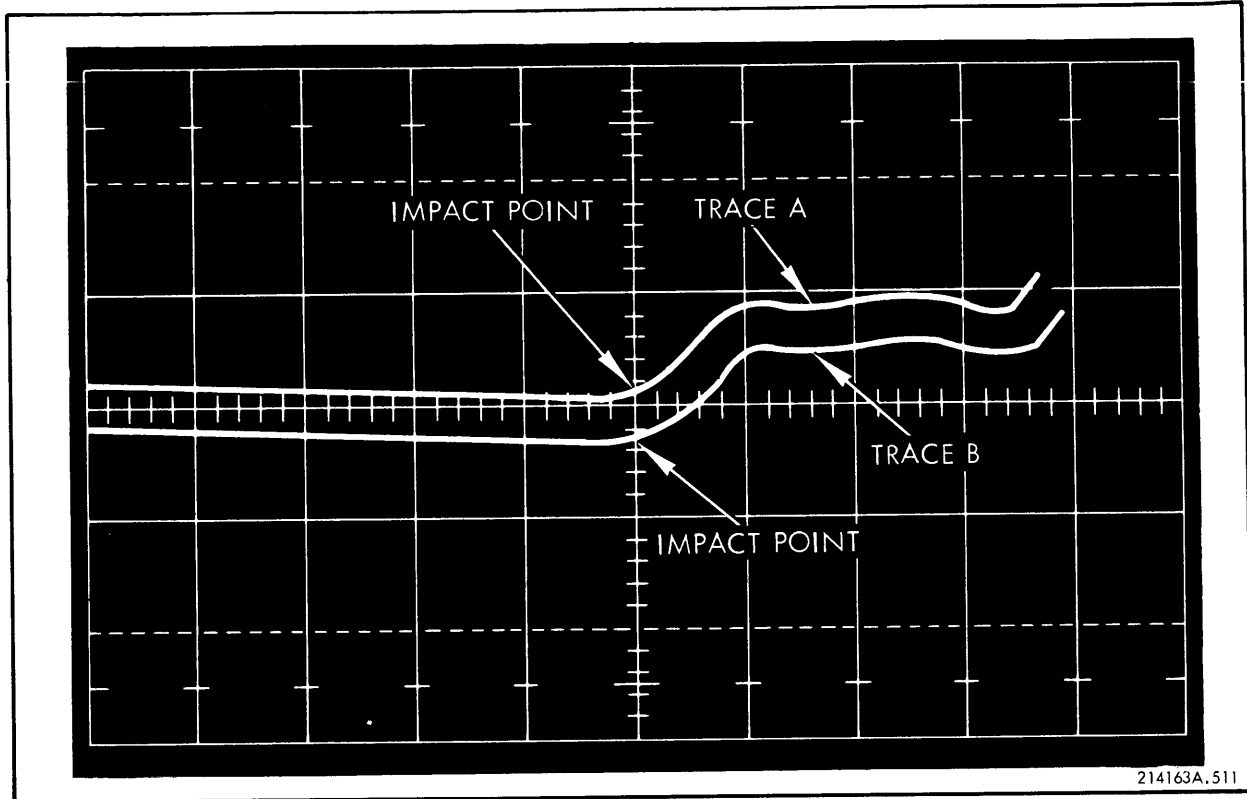


Figure 5-11. Hammer Flight Time Waveform Magnified

## 5-34 CALIBRATION OF PAPER FEED VELOCITY COMMAND

5-35 Calibrate paper feed velocity command as follows:

- a. Set oscilloscope (2, table 5-2) switches and controls as follows:

<u>Switch or Control</u>	<u>Setting</u>
MODE	CH1
TRIGGERING MODE	DC
TRIGGER SLOPE	EXT +
VOLTS/CM	.1
VARIABLE	CALIBRATED
TIME/CM	2 mSEC
VARIABLE	CALIBRATED
AC-DC-GND	DC

- b. Connect CHANNEL 1 and TRIGGER INPUT probes (3, table 5-2) to A4A1-J; connect probe ground leads to A4A1-Z.

Note

Ensure paper is loaded, ribbon installed, and drum gate closed.

- c. Enter PF commands from self test AL-27 card or user system to move paper.
- d. Adjust potentiometer R18 (figure 5-4) as required to obtain waveform in figure 5-12.

5-36 MECHANICAL ADJUSTMENTS

5-37 Mechanical adjustment procedures should be performed only when indicated as a possible remedy for a printer trouble and, if applicable, after rework or repair. Unless otherwise indicated, procedures are performed with power off.

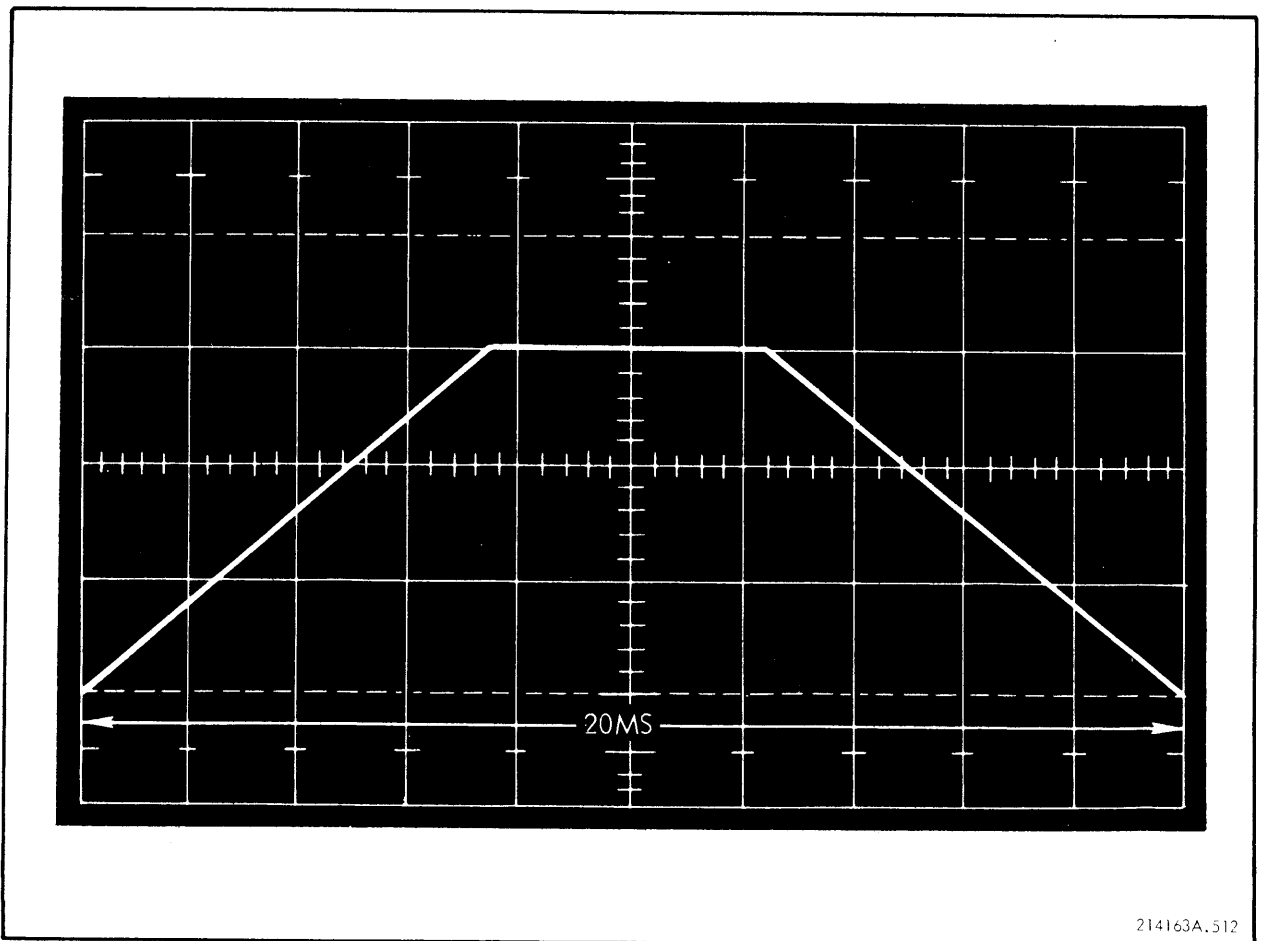


Figure 5-12. Paper Feed Velocity Command Waveform

5-38 PAPER DRIVE BELT TENSION ADJUSTMENT

5-39 Adjust paper drive belt tension as follows:

- a. Open printer cabinet rear door.
- b. Unlatch and swing card cage A3 out to 90° position.

CAUTION

If power was applied wait for line printer drum to stop rotating before proceeding to the next step.

- c. Remove belt guard holding screws (4 and 6, figure 5-13); remove belt guard (1, figure 5-13).
- d. Slightly loosen belt tensioner bracket pivot screw and locking nut (2 and 3, figure 5-13).
- e. Set force gauge (6, table 5-2) pointer to zero.
- f. Insert gauge hook into bracket hole (5, figure 5-13) as shown in figure 5-14.
- g. Grasp gauge firmly; pull until gauge indicates 19 (±2) pounds.
- h. Maintain 19 (±2) pounds pull; tighten bracket locking nut and pivot screw in that order.
- i. Replace belt guard and holding screws.
- j. Close and latch card cage A3; close cabinet door.

5-40 DRUM MOTOR BELT TENSION ADJUSTMENT

5-41 Adjust drum motor belt tension as follows:

- a. Open printer cabinet front door.
- b. Ensure drum gate A2A1 is securely latched.

CAUTION

If power was applied wait for line printer drum to stop rotating before proceeding to the next step.

- c. Remove drum gate cover (3, figure 5-15). Slightly loosen belt tensioner bracket locking screw (1, figure 5-15).
- d. Set force gauge (6, table 5-2) pointer to zero.
- e. Place gauge hook into adjustment slot of bracket (2, figure 5-15).
- f. Grasp gauge firmly; pull until gauge indicates 5.5 (±0.5) pounds.
- g. Maintain 5.5 (±0.5) pounds pull; tighten bracket locking screw.
- h. Replace drum gate cover; close cabinet door.

5-42 TRACTOR ADJUSTMENT

5-43 Adjust tractors as follows:



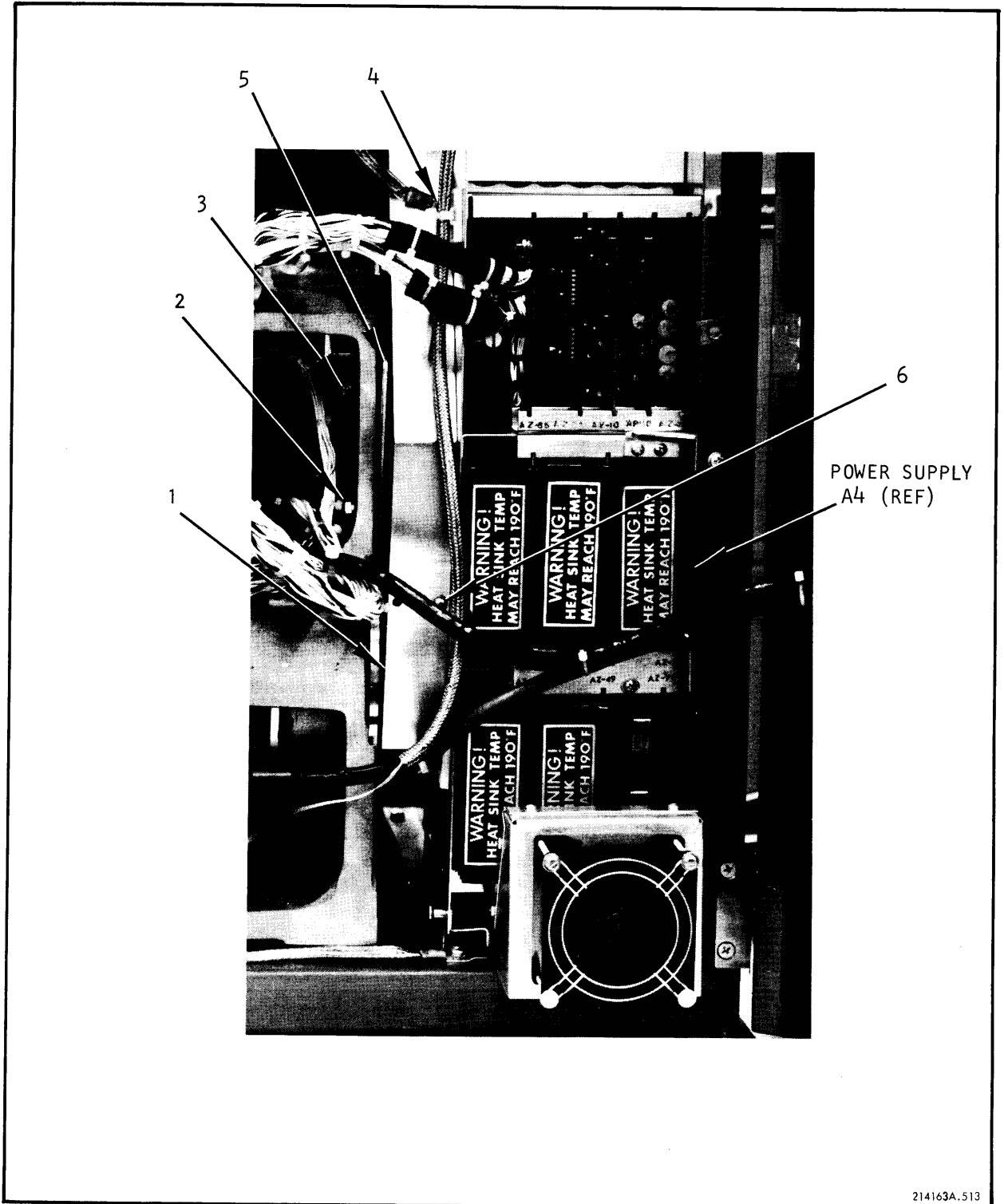
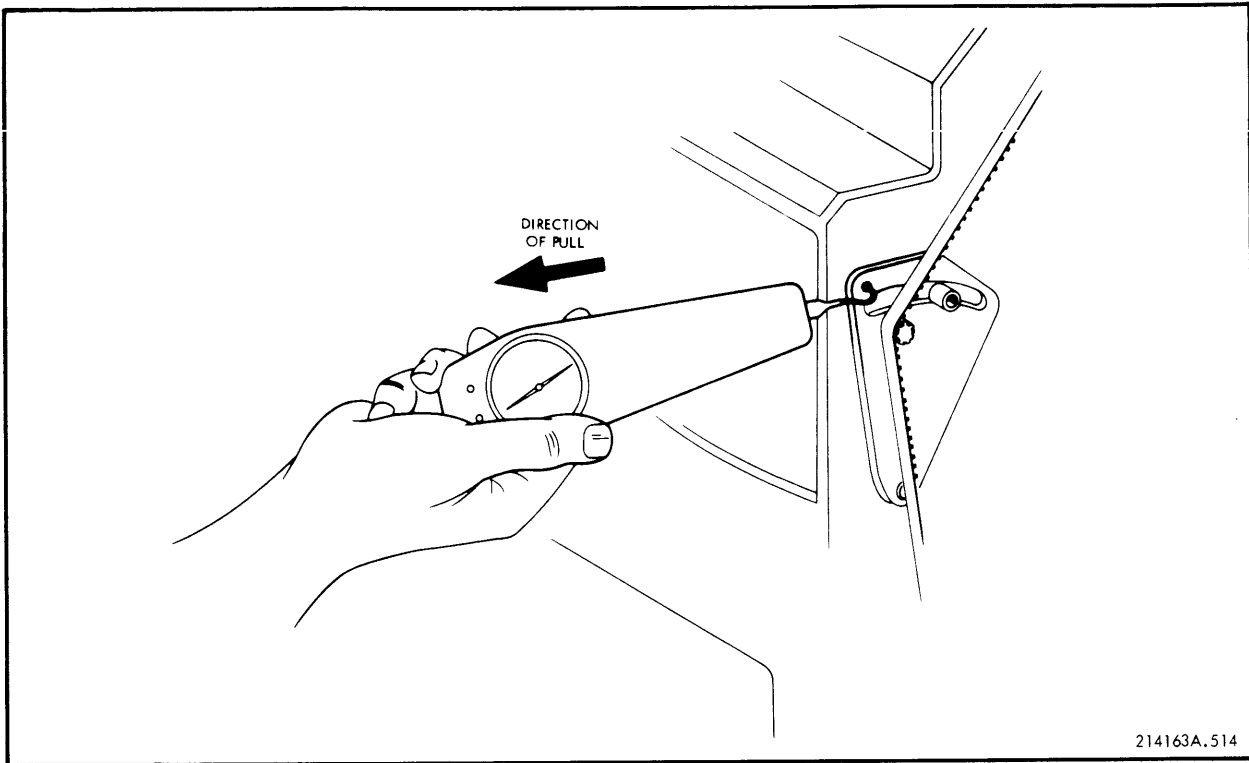


Figure 5-13. Paper Drive Belt Tension Adjustment Location



214163A.514

Figure 5-14. Paper Drive Belt Tension Adjustment

- a. Open printer cabinet front door.
- b. Unlatch and swing drum gate A2A1 out to 180° position.

## CAUTION

If power was applied wait for line printer drum to stop rotating before proceeding to the next step.

- c. Remove paper. Loosen tractor locking screws (1, figure 5-15).
- d. Loosen the sprocket adjustment screws (3, figure 5-16).
- e. Position tractors approximately 5 inches apart and center on shaft.
- f. Lift tractor pressure plates (2, figure 5-16) to 90° position.
- g. Position tractor alignment gauge (9, table 5-2) into hammer bank A2A2 pilot holes and over the tractor sprocket pins (figure 5-17).
- h. Adjust right tractor sprocket and chain so that gauge properly engages sprocket pins; tighten the sprocket adjustment screws.
- i. Remove gauge.
- j. Using printout paper, reposition tractors so that paper lies evenly over face of hammer bank (figure 3-4); tighten tractor locking screws.
- k. Close and latch drum gate; close cabinet door.

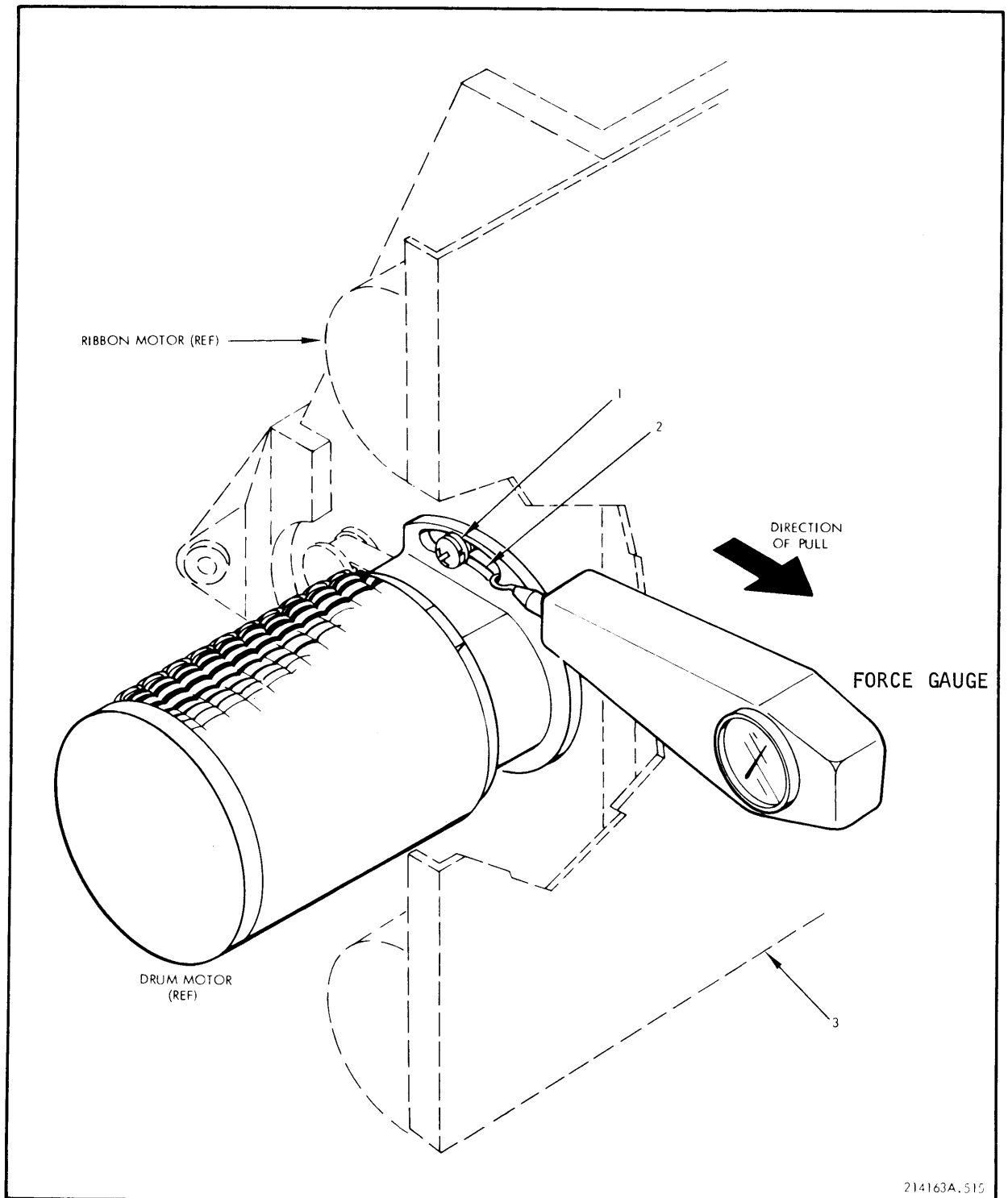


Figure 5-15. Drum Belt Tension Adjustment Location

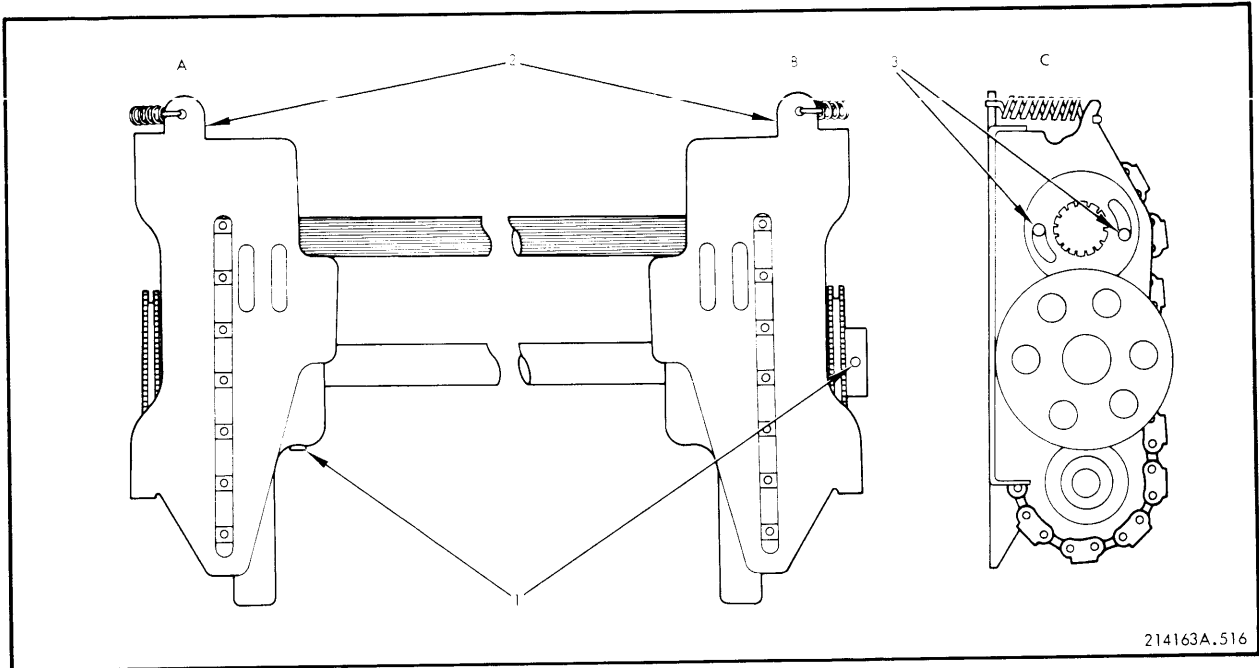


Figure 5-16. Tractor Adjustment Locations

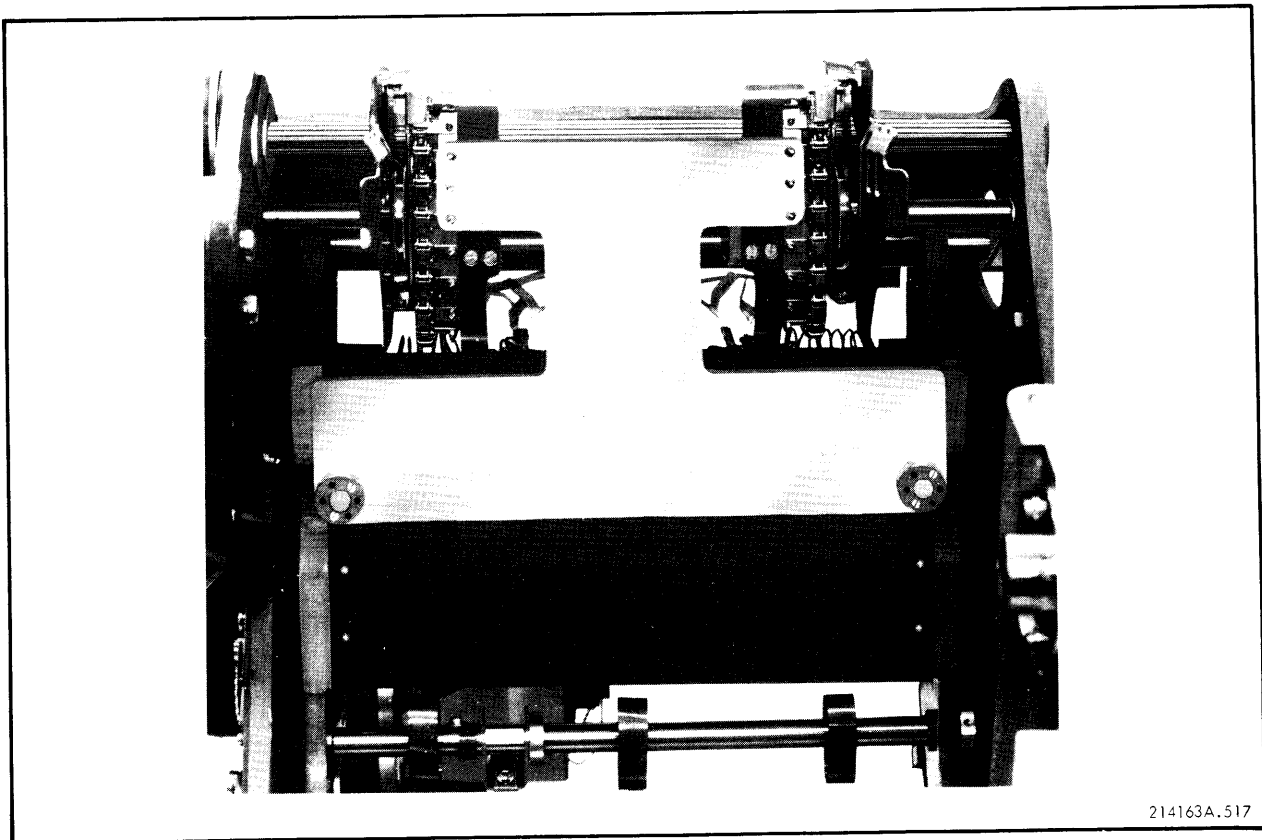


Figure 5-17. Tractor Alignment Gauge Installation

5-44 PAPER TENSION BAR AND SPRING ADJUSTMENT

5-45 Adjust paper tension bar and springs as follows:

- a. Open printer cabinet front door.
- b. Unlatch and swing drum gate A2A1 out to 180° position.

CAUTION

If power was applied wait for line printer drum to stop rotating before proceeding to the next step.

c. Place straight edge on face of ribbon guide, and insert 0.120 to 0.125 thickness gauge (10, table 5-2) between straight edge and tension bar (figure 5-18); ensure fit of gauge is snug but not tight.

NOTE

Do not perform steps d thru f if step c can be successfully performed.

- d. Loosen adjustment screws (figure 5-18) on each end of paper tension bar.
- e. Using thickness gauge, set distance between straight edge and paper tension bar to 0.120 to 0.125 inch; tighten adjustment screws.
- f. Repeat step c, and if necessary, steps d and e, to ensure proper adjustment.
- g. Cut a test strip 1-1/2 inches wide from the printout paper; place on face of hammer bank and over one paper tension spring (figure 5-19).
- h. Close and latch drum gate; set copies control lever to 1-2 position.
- i. Attach spring gauge (11, table 5-2) to test strip (figure 5-20) and pull gently on test strip.
- j. Observe if gauge indicates 62.5 ( $\pm 12.5$ ) grams, when test strip pulls free of drum gate.

NOTE

Perform steps k thru m only if step j cannot be successfully performed.

CAUTION

Avoid excessive distortion of paper tension spring.

- k. Open drum gate; grasp spring between thumb and forefinger (figure 5-21) and apply slight pressure to distort spring shape.
- l. Repeat steps g thru j.

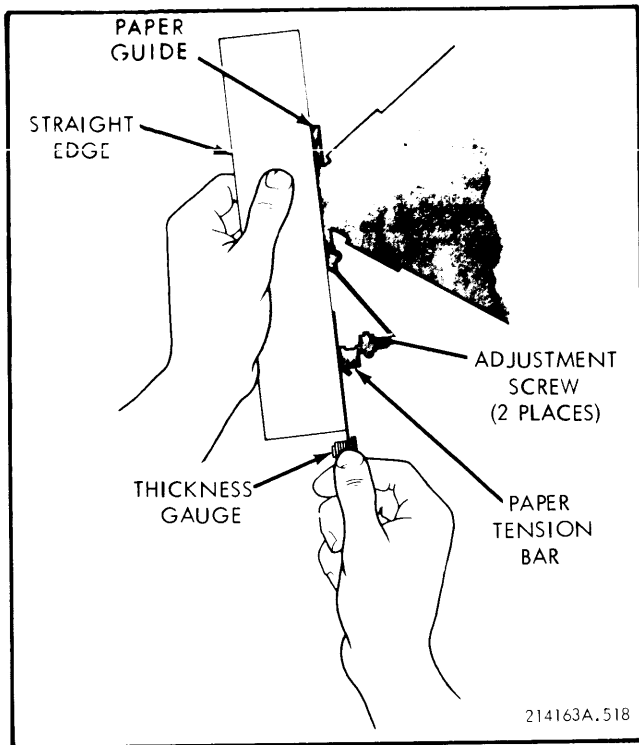


Figure 5-18. Paper Tension Bar Adjustment

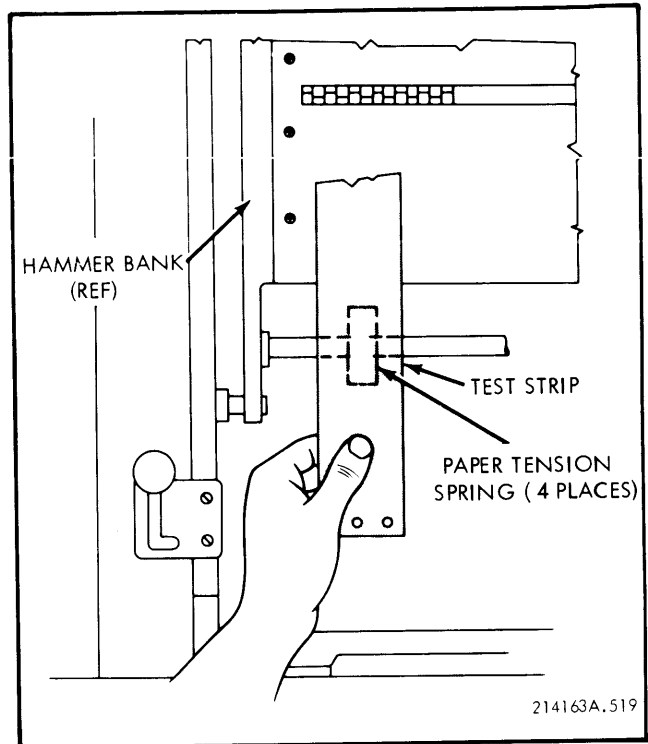


Figure 5-19. Test Strip Placement For Paper Tension Spring Adjustment

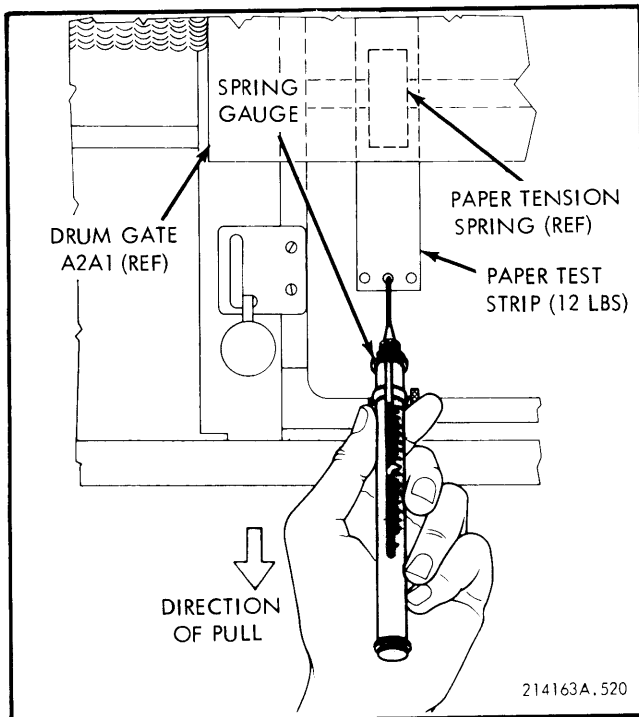


Figure 5-20. Spring Gauge Test of Paper Tension Spring

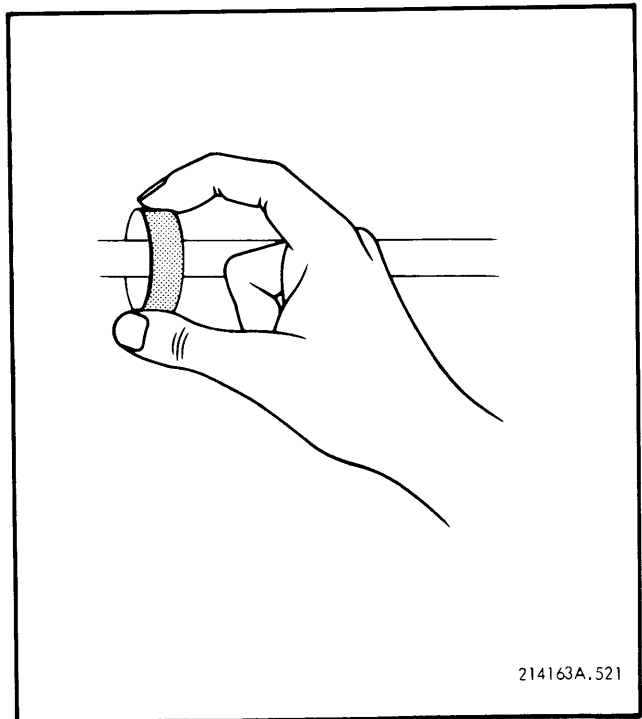


Figure 5-21. Paper Tension Spring Adjustment

NOTE

Adjust the paper tension springs to within 10 grams of each other.

- m. Repeat steps g thru j for the remaining tension springs.
- n. Open drum gate; replace paper.
- o. Close drum gate and cabinet door.

5-46 LINE STROBE PICKUP ADJUSTMENT

5-47 Adjust line strobe pickup as follows:

- a. Open printer cabinet rear door; loosen locknut on pickup (figure 5-22).
- b. Using thickness gauge (10, table 5-2) inserted between pickup and code wheel, thread pickup in or out until gap is 0.005 ( $\pm 0.001$ ) inch.

CAUTION

Do not overtighten locknut as damage can occur.

- c. Tighten locknut; ensure gap does not change.
- d. Close cabinet door.

5-48 CHARACTER PICKUP ADJUSTMENT

5-49 Adjust character pickup as follows:

- a. Open printer cabinet front door.
- b. Unlatch drum gate A2A1 and swing out to 180° position.

CAUTION

If power was applied wait for line printer drum to stop rotating before proceeding to the next step.

- c. Remove print ribbon.
- d. Loosen locknut on pickup (figure 1-6).
- e. Using thickness gauge (10, table 5-2) inserted between pickup and code wheel, thread pickup in or out until gap is 0.005 ( $\pm 0.001$ ) inch.
- f. Tighten locknut; ensure gap does not change.
- g. Replace ribbon.
- h. Close and latch drum gate and cabinet door.

5-50 INDEX PICKUP ADJUSTMENT

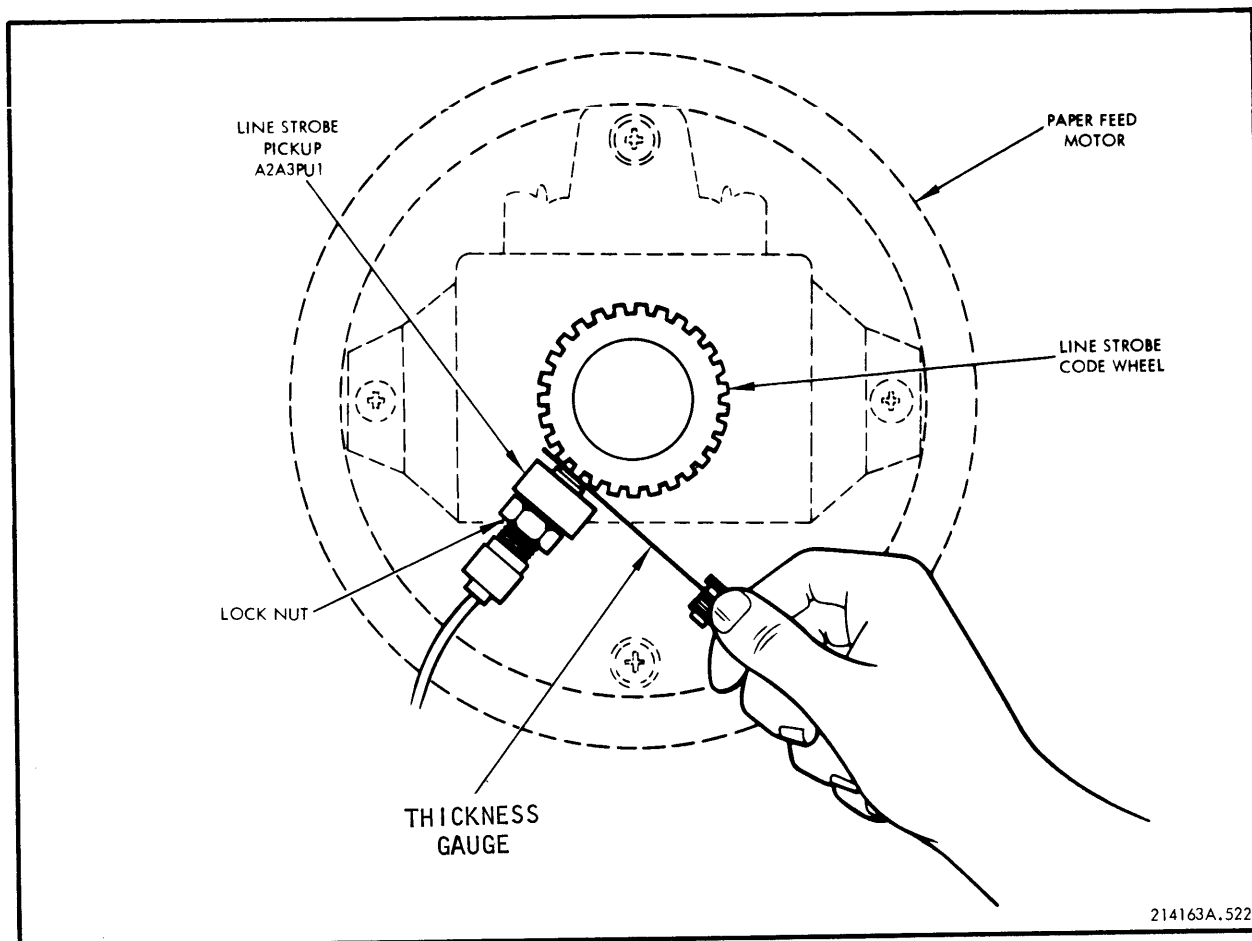


Figure 5-22. Line Strobe Pickup Adjustment

5-51 Adjust index pickup as follows:

- a. Open printer cabinet front door.
- b. Unlatch and swing drum gate A2A1 out to 180° position.

CAUTION

If power was applied wait for line printer drum to stop rotating before proceeding to the next step.

- c. Remove print ribbon.
- d. Loosen locknut on pickup (figure 1-6).
- e. Using thickness gauge (10, table 5-2) inserted between pickup and code wheel index pin, thread pickup in or out until gap is 0.011 ( $\pm 0.001$ ) inch.
- f. Tighten locknut; ensure gap does not change.
- g. Replace ribbon.
- h. Close and latch drum gate and cabinet door.



5-52 CHARACTER CODE WHEEL ADJUSTMENT

5-53 Adjust character code wheel as follows:

Note

Ensure paper is loaded, ribbon installed, and drum gate closed.

a. Enter several lines of E pattern from self test AL-27 card or user system; observe if character is whole and appears as in figure 5-7.

Note

Do not perform steps b thru k if appearance and placement of character is similar to figure 5-7.

b. Open printer cabinet rear door; unlatch and swing card cage A3 out to 90° position.

c. Set potentiometer R2 (15) (figure 5-8) to center position.

d. Open printer cabinet front door; unlatch drum gate A2A1 and swing out to 180° position.

e. Remove print ribbon.

f. Loosen code wheel locking nuts (1, figure 5-23).

g. Move code wheel (2, figure 5-23) up or down; tighten locking nuts.

h. Replace ribbon.

i. Repeat steps a, f, and g until printout is similar to figure 5-7.

j. Enter E pattern to start print cycle.

k. Adjust potentiometer R2 (15) clockwise until bottom portion of character is first cut off.

Note

Carefully note number of turns required to perform step l.

l. Adjust potentiometer R2 (15) counterclockwise until upper portion of character is first cut off.

m. Adjust potentiometer R2 (15) clockwise 1/2 the number of turns noted in step l.

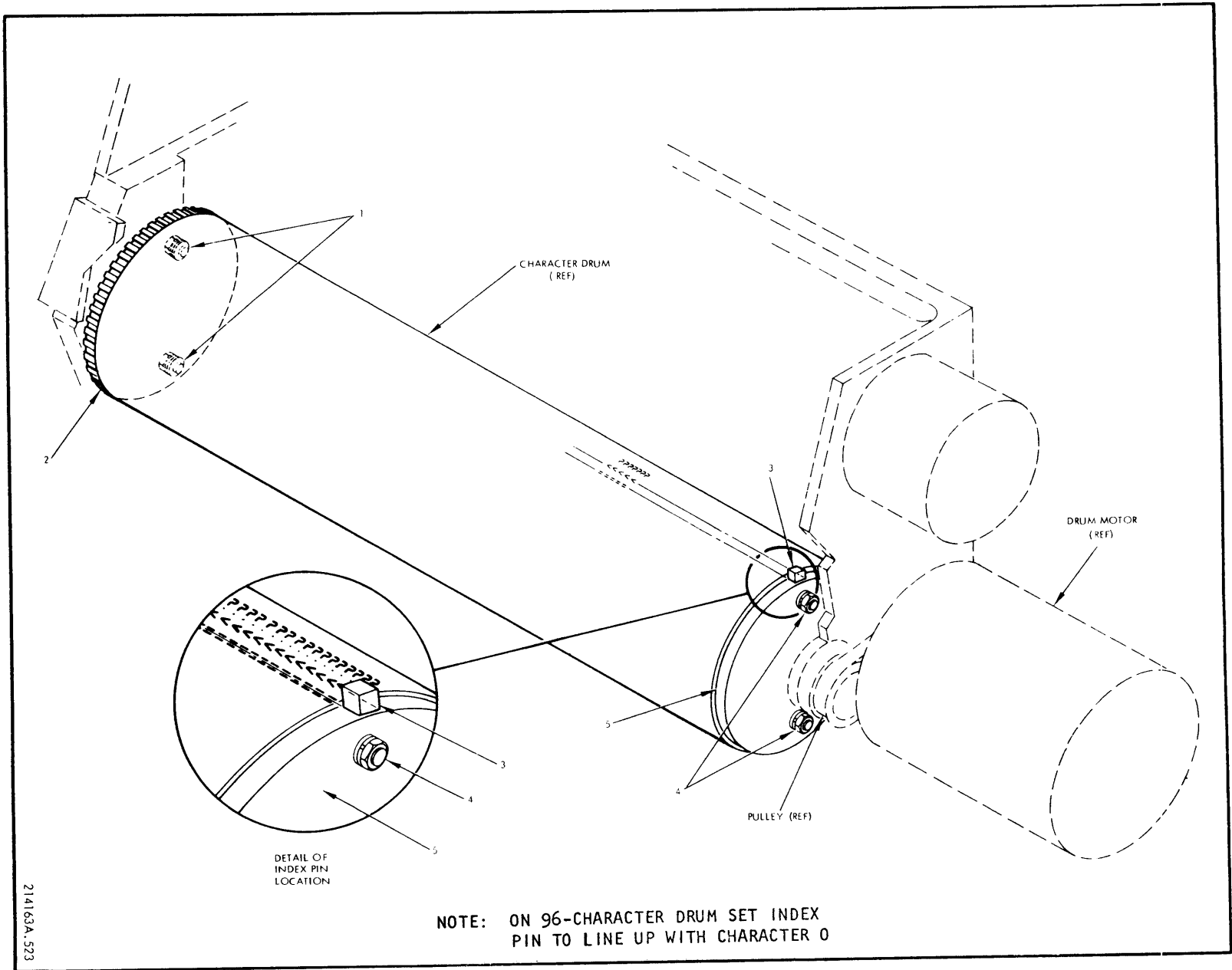


Figure 5-23. Character Code Wheel and Index Wheel Adjustment

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- n. Close and latch card cage A3, and cabinet rear door.
- o. Close and latch drum gate and cabinet front door.

5-54 INDEX WHEEL ADJUSTMENT

5-55 Adjust index wheel as follows:

Note

Ensure paper is loaded, ribbon installed, and drum gate closed.

- a. Enter E pattern from self test AL-27 card or user system; observe if character other than E appears on printout.

Note

Do not perform steps b thru g if character E does appear.

- b. Open printer cabinet front door; unlatch and swing drum gate A2A1 out to 180° position.
- c. Remove print ribbon.
- d. Loosen index wheel locking nuts (4, figure 5-23).
- e. Move index wheel (5, figure 5-23) until edges of index pin (3, figure 5-23) line up with centers of characters = and < on drum (figure 5-23); tighten locking nuts.
- f. Replace ribbon; repeat step a.

Note

If character E still does not appear, repeat step d and adjust index pin from reference point set in step e until E does appear on printout.

- g. Close and latch drum gate and cabinet door.

5-55A TOP OF FORM CAM SWITCH ADJUSTMENT

5-55B Adjust the top of form cam switch as follows:

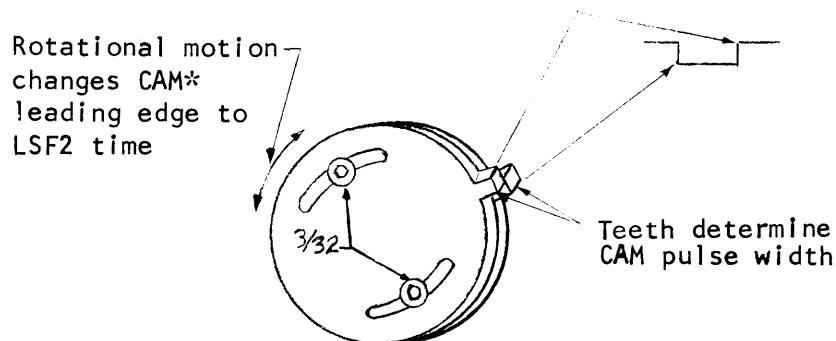
- a. Connect scope channel A to A4-25 (CAM\*) and channel B to A4-28 (LSF2).
- b. Sync negative on channel A.

c. Load paper in printer (paragraph 3-16). Vertical paper adjustment knob must be centered (fig. 3-3). If paper perforations do not line up, loosen two screws on the cam tooth assembly (figure below), hold assembly in place and move the paper drive belt until the paper perforations line up.

d. Tighten the screws and turn the printer on.

e. Activate Top Of Form switch on Operator's panel and observe the channel B pulses (LSF2) that occur during the time that channel A is low (CAM\*) (see figure 4-11).

f. LSF2 should be low when CAM\* goes low. If it is not, the cam tooth assembly (figure below) must be rotated slightly. This is done by loosening the two 3/32 socket head cap screws, moving the device slightly and retightening the screws.



g. Perform step e. again. The number of pulses (LSF2) that occur while channel A is low (CAM\*) will be the number of lines that are skipped. (The number of lines actually moved will be one greater than the number skipped.)

#### Note

If channel A signal (CAM\*) returns to +5 volts during an LSF2 pulse or if it is desirable to change the number of lines skipped, perform the following adjustments:

h. Loosen the two 3/32 socket head cap screws in the above figure and carefully change the relationship of the two teeth. The more in line that the teeth are, the shorter the CAM pulse.

i. Rotate the teeth apart to increase CAM\* - the number of lines to be skipped.

j. Tighten the two screws and recheck steps f through j as required to obtain proper signal relationship and line skips.

#### 5-56 REMOVAL AND REPLACEMENT OF ASSEMBLIES

5-57 The following paragraphs contain the removal and replacement procedure for a hammer assembly in hammer bank A2A2. To replace an assembly, reverse the sequence of the removal procedure. To remove and replace other printer assemblies, sub-assemblies, and detail parts, refer to Volume II of this manual. Before removing any assembly from the printer, the following preliminary procedure must be performed.

5-58 PRELIMINARY PROCEDURE

5-59 Perform preliminary procedure as follows:

- a. Set circuit breaker CBI to OFF.
- b. Disconnect primary power cable from ac source.

5-60 HAMMER ASSEMBLY

5-61 Remove hammer assembly from hammer bank A2A2 as follows:

- a. Open printer cabinet front door; unlatch and swing drum gate A2A1 out to 180° position.

CAUTION

If power was applied wait for line printer drum to stop rotating before proceeding to the next step.

- b. Remove paper.

NOTE

Even-numbered hammers are located in top hammer bank, and odd-numbered hammers in bottom hammer bank.

- c. Loosen screw at each end of A-MP block (figure 5-24) securing applicable hammer bank cover; remove cover (figure 5-24).

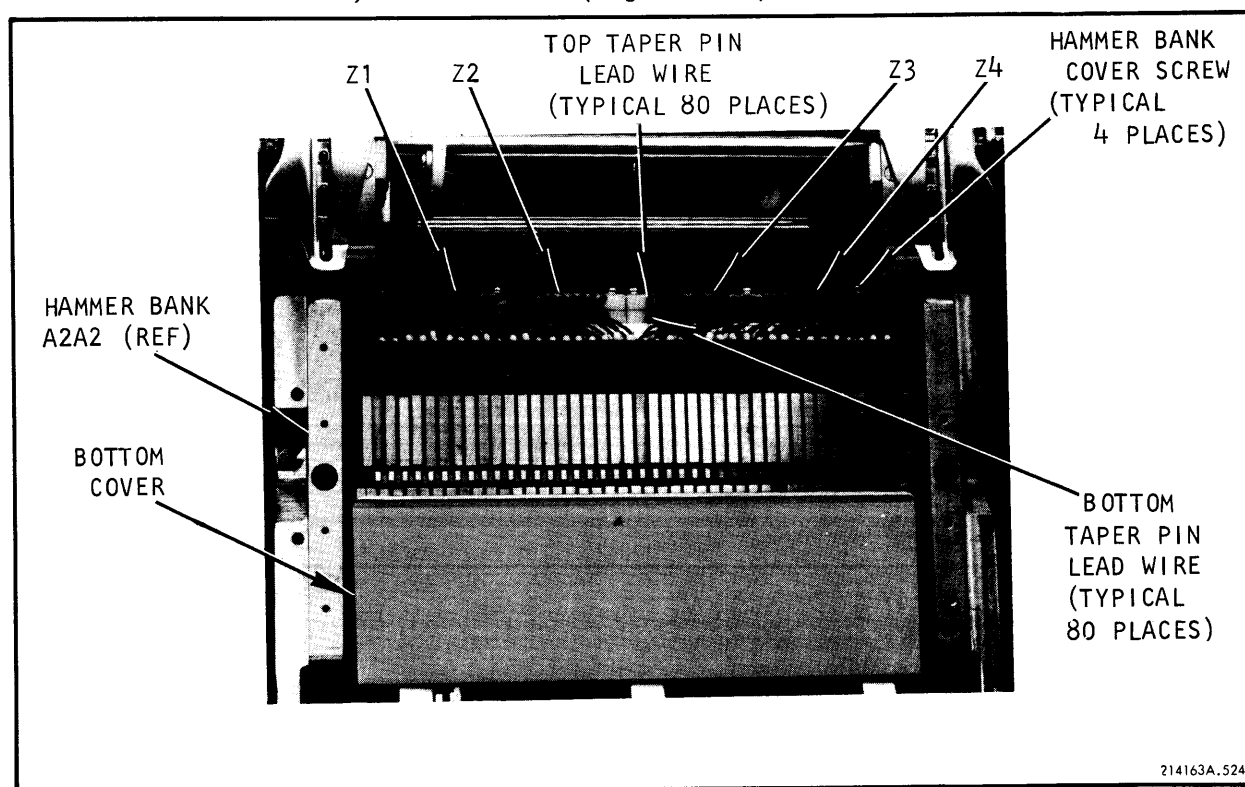


Figure 5-24. Hammer Bank A2A2 Cover (Top Cover Shown Removed)

**CAUTION**

Keep taper pin removal tool at same angle as taper pin during lead wire removal, to avoid damage to wire or pin. Note location of wire being removed.

d. Remove hammer assembly top (2) and bottom (2) lead wires from the A-MP block as follows:

1. Place taper pin removal tool (14, table 5-2) against underside of a top taper pin (figure 5-24), and engage pin in notch of tool shaft (figure 5-25).

2. Gently squeeze tool trigger.

e. Repeat step d for remaining top taper pin and two bottom taper pins.

f. Open printer cabinet rear door.

g. Using torque screwdriver (7, table 5-2), preset to 4.8 to 5 inch-pounds, remove mounting screw (figure 5-9) from hammer to be removed.

**CAUTION**

Handle hammer assembly carefully and never by flag, or serious damage can result.

h. Carefully grasp foot of assembly (figure 5-26) and slide out until free of hammer bank.

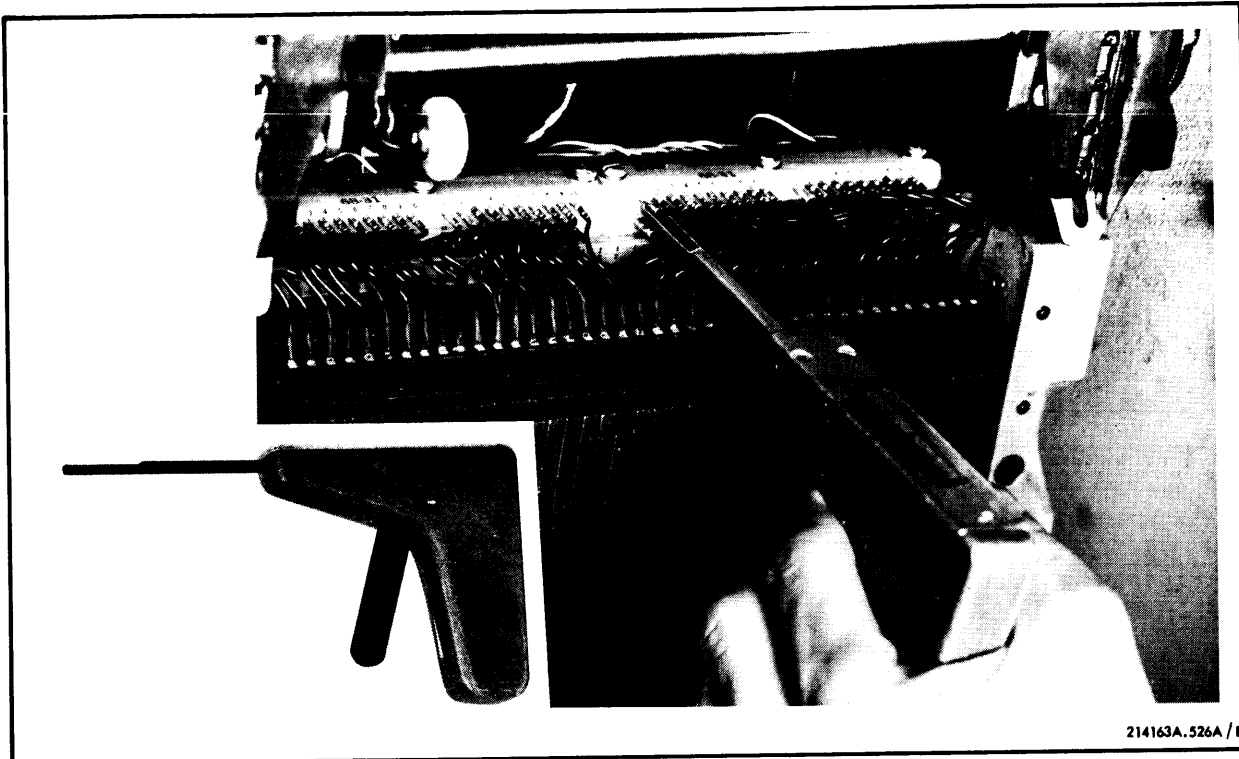
i. After replacing hammer assembly, install lead wires into A-MP block as follows:

Note

For ease of operation, replace the bottom taper pins first and then the top pins.

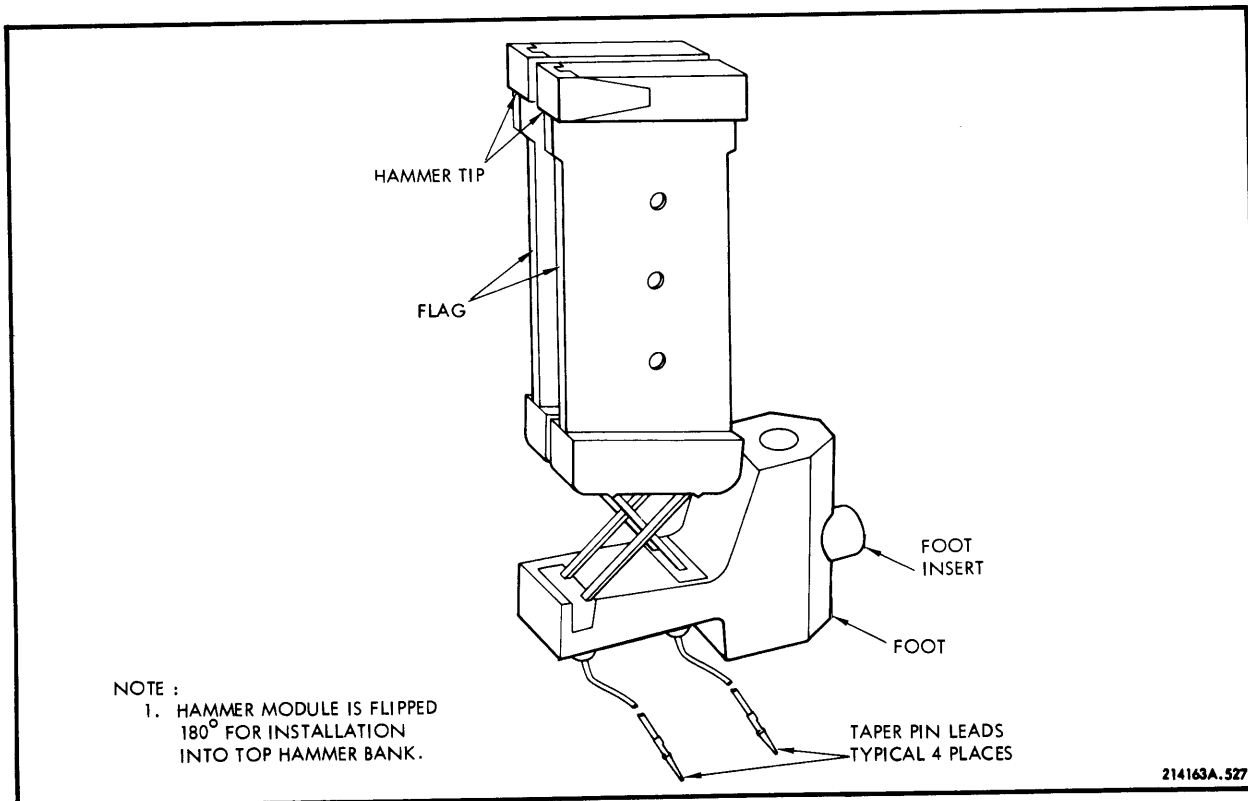
1. Place each taper pin into proper A-MP block receptacle.

2. Position taper pin insertion tool (15, table 5-2) to engage each taper pin in notched portion of tool shaft (figure 5-27); push tool firmly inward until snap is heard and then repeat until snap is heard again.



214163A.526A/B

Figure 5-25. Hammer Assembly Taper Pin Removal



NOTE :  
1. HAMMER MODULE IS FLIPPED  
180° FOR INSTALLATION  
INTO TOP HAMMER BANK.

214163A.527

Figure 5-26. Hammer Assembly

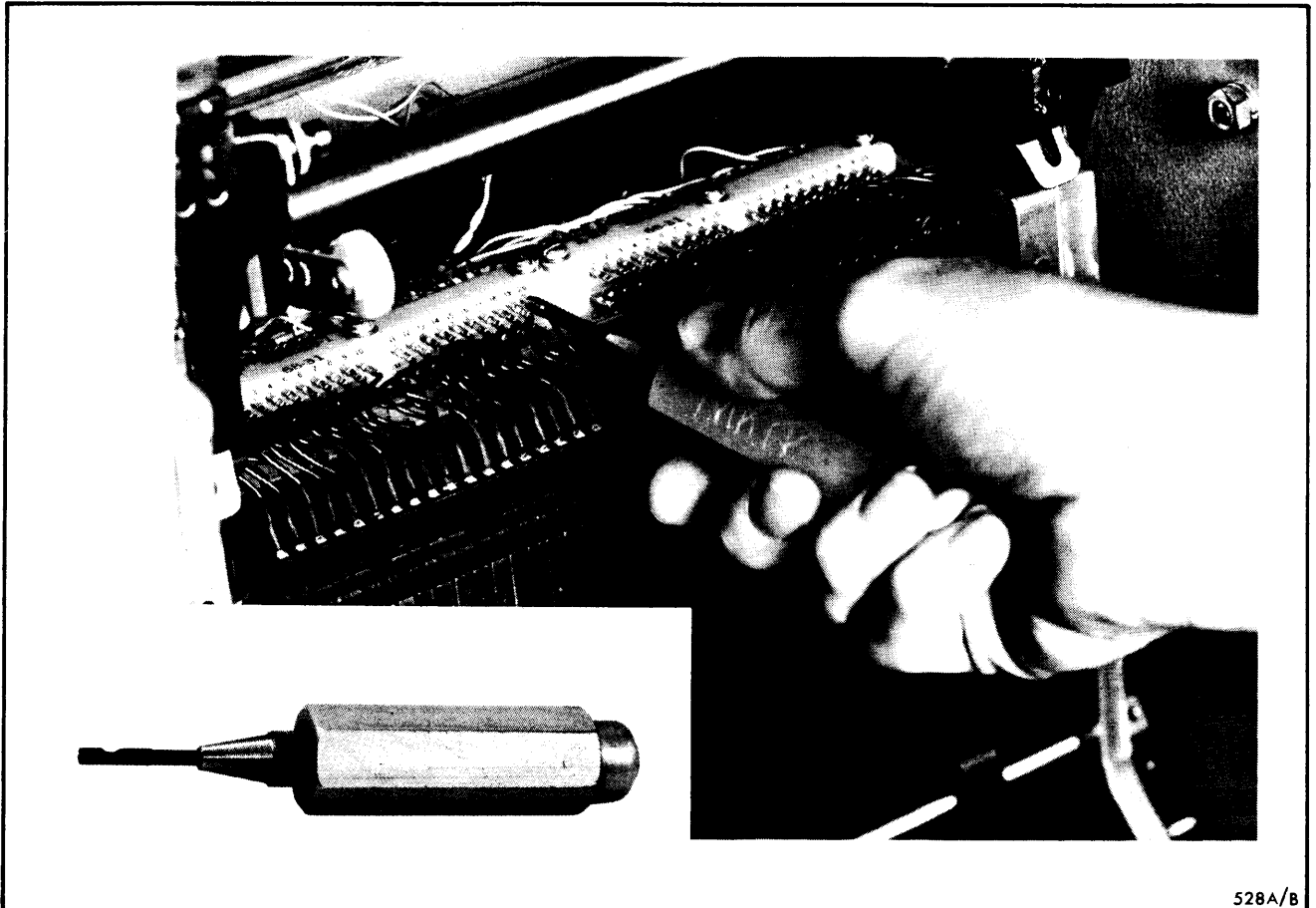


Figure 5-27. Hammer Assembly Taper Pin Installation

5-62 DRUM MOTOR CONVERSION TO 50 HZ OPERATION

5-63 Convert drum motor to 50 Hz operation as follows:

a. Refer to Volume II of this manual to remove drum motor belt and pulleys and replace with 50 Hz pulleys.

b. Refer to figure 5-3 if wiring change is required on power transformer A4T1.

5-64 LUBRICATION

5-65 The printer does not require lubrication.



5-66 TROUBLESHOOTING

5-67 Troubleshooting table 5-6 is used in conjunction with the maintenance test to isolate a trouble to an assembly or card type. Table 5-6 lists the troubles (in the order in which the maintenance tests are performed), probable causes, and remedies. Component causes of troubles should be verified if possible before replacement. If the probable cause listed is not the cause or complete cause of the trouble, standard electronic troubleshooting techniques may be used to locate and isolate the actual cause. Obvious troubles (broken or shorted wires, loose harness assembly connections, improperly seated cards, and defective indicators) are not included in table 5-6. When a part has been determined to be defective, remove and replace it with an identical part. Refer to Volume II of this manual for ordering replacement parts.

Table 5-6. Troubleshooting Chart

Step	Trouble	Probable Cause	Remedy
1	POWER indicator does not light  DVOM does not indicate +22 ( <u>±</u> 3) volts  Note  Step 2 not applicable if paper installed.	Fuse A4F2 (+22V) Circuit breaker A4CB1 Card AZ-78 +22V filter capacitors  Transformer A4T1	Replace A4F2 Replace A4CB1 Replace AZ-78 (A4A10) Replace A4C2 and/or A4C3  Replace A4T1
2	PAPER FAULT indicator does not light	Switches A2S4 and/or A2S5 Card AZ-19	Replace A2S4 and/or A2S5 Replace AZ-19 (A3A16)
3	DRUM GATE indicator does not light	Switch A2S1	Replace A2S1
4	READY indicator does not light	Card AZ-19 Card AT-13	Replace AZ-19 (A3A16) Replace AT-13 (A3A6)
5	Paper does not move to top-of-form when TOP OF FORM switch is pressed	Card AP-10, AG-20, or AG-45  Card AZ-49 (Paper feed forward power amplifier)  Paper feed motor A2A3B1	Replace AP-10 (A4A1), AG-20 (A3A5), or AG-45 (A3A4) Replace AZ-49 (A4A6) Replace A2A3B1

Table 5-6. Troubleshooting Chart (Continued)

Step	Trouble	Probable Cause	Remedy
6	Paper does not advance one line when PAPER STEP switch is pressed	Switch A5S2 Card AG-20	Replace A5S2 Replace AG-20 (A3A5)
7	PRINT INHIBIT indicator does not light	Switch A4S1	Replace A4S1
8	DVOM does not indicate +65 ( $\pm 6.5$ ) volts	Card AZ-78 +65V filter capacitor Transformer A4T1	Replace AZ-78 (A4A10) Replace A4C1 Replace A4T1
9	DVOM does not indicate +28 ( $\pm 0.1$ ) volts	Fuse A4F3 (+28V) Potentiometer A4A2R39 out of adjustment Card AV-10 Card AZ-49 (+28V series regulator power amplifier) +28V filter capacitor Transformer A4T1	Replace A4F3 Perform +28V calibration Replace AV-10 (A4A2) Replace AZ-49 (A4A9) Replace A4C6 Replace A4T1
10	DVOM does not indicate +12 ( $\pm 0.01$ ) volts	Potentiometer A4A2R22 out of adjustment Card AV-10 Card AZ-49 (+12V series regulator power amplifier)	Perform +12V calibration Replace AV-10 (A4A2) Replace AZ-49 (A4A7)
11	DVOM does not indicate +5 ( $\pm 0.01$ ) volts	Fuse A4F1 (+5V) Potentiometer A4A2R2 out of adjustment Card AV-10 Card AZ-49 (+5V series regulator power amplifier) Card AZ-78 +5V filter capacitor SCR A4Q6 Transformer A4T1	Replace A4F1 Perform +5V calibration Replace AV-10 (A4A2) Replace AZ-49 (A4A8) Replace AZ-78 (A4A10) Replace A4C4 Replace A4Q6 Replace A4T1
12	DVOM does not indicate between -12 and -16 volts	Fuse A4F7 (-12V) -12V filter capacitor	Replace A4F7 Replace A4C5

Table 5-6. Troubleshooting Chart (Continued)

Step	Trouble	Probable Cause	Remedy
13	Oscilloscope does not display 1 cm (+5.0V) deflection or logic 1 voltage level if other than +5.0V	Potentiometer A3A11R1 out of adjustment  Card AJ-14	Perform calibration of driver A3A11 reference voltage  Replace AJ-14 (A3A11)
14	Oscilloscope does not display 0.5 cm (+2.5V) deflection or 1/2 of logic 1 voltage level if other than +5.0V	Potentiometer A3A14R2 out of adjustment  Card AK-10	Perform calibration of receiver A3A14 reference voltage  Replace AK-10 (A3A14)
15	Oscilloscope does not display waveform similar to figure 5-6	Potentiometer A3A16R29 out of adjustment  Card AZ-19  Card AH-10	Perform calibration of hammer driver current  Replace card AZ-19 (A3A16)  Replace AH-10 (A3A18, A3A19, A3A20, A3A21, or A3A22)
16	Printout quality is not similar to figure 5-7 as follows:  a. Hammer(s) do not fire  b. Paper tears or jams  c. Paper does not stop (slew is constant)	Card AH-10  Hammer(s) defective Card AS-13  Tractor out of adjustment  Line strobe pickup out of adjustment  Pickup A2PU1 Switch A2S3 Card AS-13	Replace applicable AH-10 (A3A18, A3A19, A3A20, A3A21, or A3A22)  Replace hammer(s) Replace AS-13 (A3A15)  Perform tractor adjustment  Perform line strobe pickup adjustment  Replace A2PU1 Replace A2S3 Replace AS-13 (A3A15)

Table 5-6. Troubleshooting Chart (Continued)

Step	Trouble	Probable Cause	Remedy
	d. Character embossed/paper tears	Card AT-13 Card AG-45 Wrong paper used COPIES CONTROL lever set incorrectly for paper being used	Replace AT-13 (A3A6) Replace AG-45 (A3A4) See table 1-3 Check setting of COPIES CONTROL lever
	e. Upper or lower portion of character missing	Potentiometer A3A15R2 out of adjustment Character code wheel out of adjustment	Perform character code wheel adjustment Same as above
	f. Character other than E is printed	Pickup A2A1PU1 Card AS-13 Index wheel out of adjustment	Replace A2A1PU1 Replace AS-13 (A3A15) Perform index wheel adjustment
	g. Character prints too dark	Pickup A2A1PU2 Card AS-13 Ribbon overinked	Replace A2A1PU2 Replace AS-13 (A3A15) Replace ribbon
	h. Character prints too light	Hammer flight time incorrect Ribbon worn Hammer flight time incorrect	Perform calibration of hammer flight time Replace ribbon Perform calibration of hammer flight time
	i. Characters in some print positions not clearly defined, or portion missing	Character drum dirty Hammer(s) damaged or misaligned	Clean drum with isopropyl alcohol Replace hammer(s)

Table 5-6. Troubleshooting Chart (Continued)

Step	Trouble	Probable Cause	Remedy
	j. Line-to-line spacing incorrect	Potentiometer A4A1R18 out of adjustment  Card AP-10	Perform calibration of paper feed velocity command  Replace AP-10 (A4A1)
	k. Characters do not print in all zones	Zone select SCR open	Replace applicable SCR (A4Q1, A4Q2, A4Q3, or A4Q4)
	l. Characters print in two or more zones simultaneously	Zone select SCR shorted	Replace applicable SCR (A4Q1, A4Q2, A4Q3, or A4Q4)

SECTION VI  
DRAWINGS

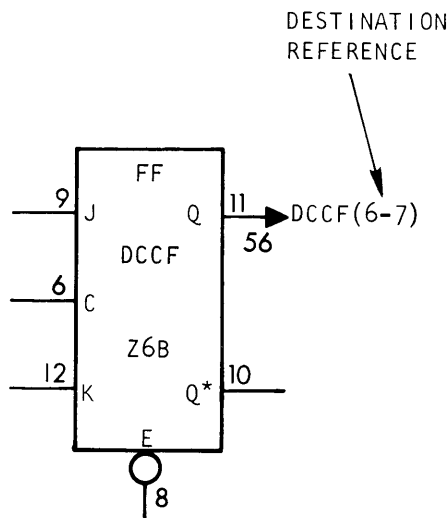
6-1 INTRODUCTION

6-2 This section contains a complete complement of printer logic and schematic diagrams, and a description of the J-K master/slave flip-flop.

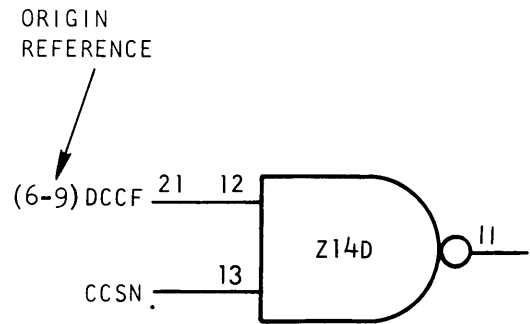
6-3 DRAWINGS

6-4 To aid in troubleshooting, figures 6-1 thru 6-28 are cross-referenced so signals can be followed from point of origin to destination. This is illustrated in the example below with signal DCCF which is an output of flip-flop DCCF on figure 6-9 and an input to NAND gate Z14D on figure 6-7.

Example:



Portion of  
Figure 6-9



Portion of  
Figure 6-7

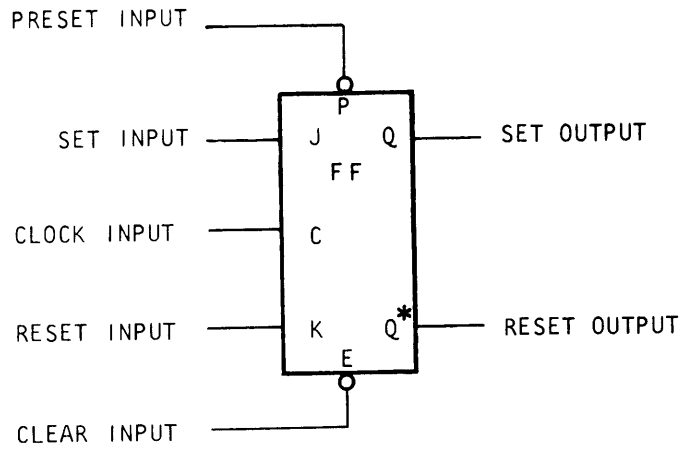
6-5 LOGIC SYMBOLS

6-6 With two exceptions, the logic symbols in the drawings throughout this manual are standard and described in MIL-STD-806B. The exceptions are:

- a. An asterisk (\*) replaces the overbar used to denote the inverted or not function of a term. Example: CHCK\* = CHCK.

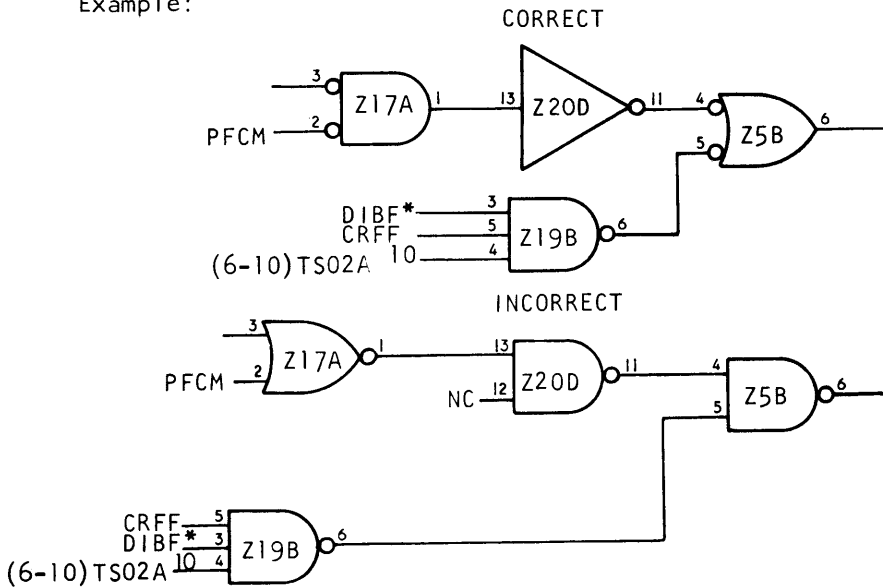
b. The symbol for a J-K flip-flop is shown in the example below.

Example:



6-7 The AND and OR logic symbols as used in this manual show the intended logical combination of the input signals rather than the hardware mechanization.

Example:



6-8 Active State Indicator

6-9 A small circle(s) at the input(s) to any element (logic or nonlogic) indicates that the relatively low (L) input signal activates the function. Conversely, the absence of a small circle indicates that the relatively high (H) input signal activates the function.

6-10 A small circle at the element output indicates that the output of the activated function is relatively low. Conversely, the absence of a small circle indicates that the output of the activated function is relatively high.

6-11 In table 6-1, examples are given of some common functions of two variables and their equivalents.

Table 6-1. Common Functions of Two Variables

AND Symbol	OR Symbol	Inputs		Output
		A	B	X
		H	H	L
		H	L	H
		L	H	H
		L	L	H
		H	H	L
		H	L	L
		L	H	L
		L	L	H
		H	H	H
		H	L	L
		L	H	L
		L	L	L
		H	H	H
		H	L	H
		L	H	H
		L	L	L

6-12 J-K MASTER/SLAVE FLIP-FLOP (Figure 6-29)

6-13 The following paragraphs are intended as an aid in understanding and troubleshooting the J-K master/slave flip-flop (hereafter called the J-K flip-flop) used throughout the printer logic.

6-14 Two J-K flip-flops, each consisting of two distinct flip-flops (master/slave) and associated gates and diodes, are housed in one integrated circuit chip.



6-15 Each J-K flip-flop has five distinct inputs and two outputs as follows:

- a. J = Set input with clock
- b. K = Reset input with clock
- c. E = DC clear (reset) input without clock
- d. P = DC set input without clock
- e. C = Clock input (clocks on trailing edge of positive pulse)
- f. Q = Set output
- g. Q\* = Reset output

#### 6-16 J-K FLIP-FLOP OPERATION

6-17 Since the J-K flip-flop consists of two flip-flops (master and slave), the master is conditioned first and the slave flip-flop is conditioned at a later time to reflect the initial state of the master flip-flop. The conditioning of the master and subsequent transferring of intelligence to the slave flip-flop is accomplished under the control of the clock input. The possible operating conditions of the J-K flip-flop are described in the following paragraphs, and reference is made to figure 6-29.

#### 6-18 DC Set

6-19 If input P goes low, NAND gates 2 and 6 are inhibited and NAND gates 3 and 7 are enabled, setting both the master and slave flip-flops. Output Q goes high and remains high until P goes high and another operating state is initiated.

#### 6-20 DC Reset

6-21 If input E goes low, NAND gates 1 and 5 are inhibited, and NAND gates 4 and 8 are enabled, resetting both the master and slave flip-flops. Output Q\* goes high and remains high until E goes high and another operating state is initiated.

#### 6-22 Set With Clock

6-23 Assuming input J is high, all other inputs are inhibited, and the J-K flip-flop is at present reset, the following takes place.

6-24 Since J, E, and Q\* are high, NAND gate 1 is enabled when C (clock) goes high and the master flip-flop is set. The output of the clock inverter goes low and disables NAND gate 5. The slave flip-flop is thus prevented from responding to the master flip-flop output for the duration of the clock. Once the master flip-flop is set, J can go low as it has no further effect on the J-K flip-flop state in this operation.

6-25 When C goes low, the clock inverter output goes high, enabling NAND gate 5 and setting the slave flip-flop. Output Q goes high and remains high until another operating state is initiated. Since Q\* is now low, NAND gate 1 is inhibited and the present state is maintained if J again goes high. To change state requires that K go high or E go low.

6-26 Reset With Clock

6-27 Assuming input K is high, all other inputs are inhibited, and the J-K flip-flop is at present set, the following takes place.

6-28 Since K, P, and Q are high, NAND gate 2 is enabled when C (clock) goes high and the master flip-flop is reset. The output of the clock inverter goes low and disables NAND gate 6. The slave flip-flop is thus prevented from responding to the master flip-flop output for the duration of the clock. Once the master flip-flop is set, K can go low as it has no further effect on the J-K flip-flop state in this operation.

6-29 When C goes low, the clock inverter output goes high, enabling NAND gate 6 and resetting the slave flip-flop. Output Q\* goes high and remains high until another operating state is initiated. Since Q is now low, NAND gate 2 is inhibited and the present state is maintained if K again goes high. To change state requires that J go high or P go low.

6-30 Inputs J and K High

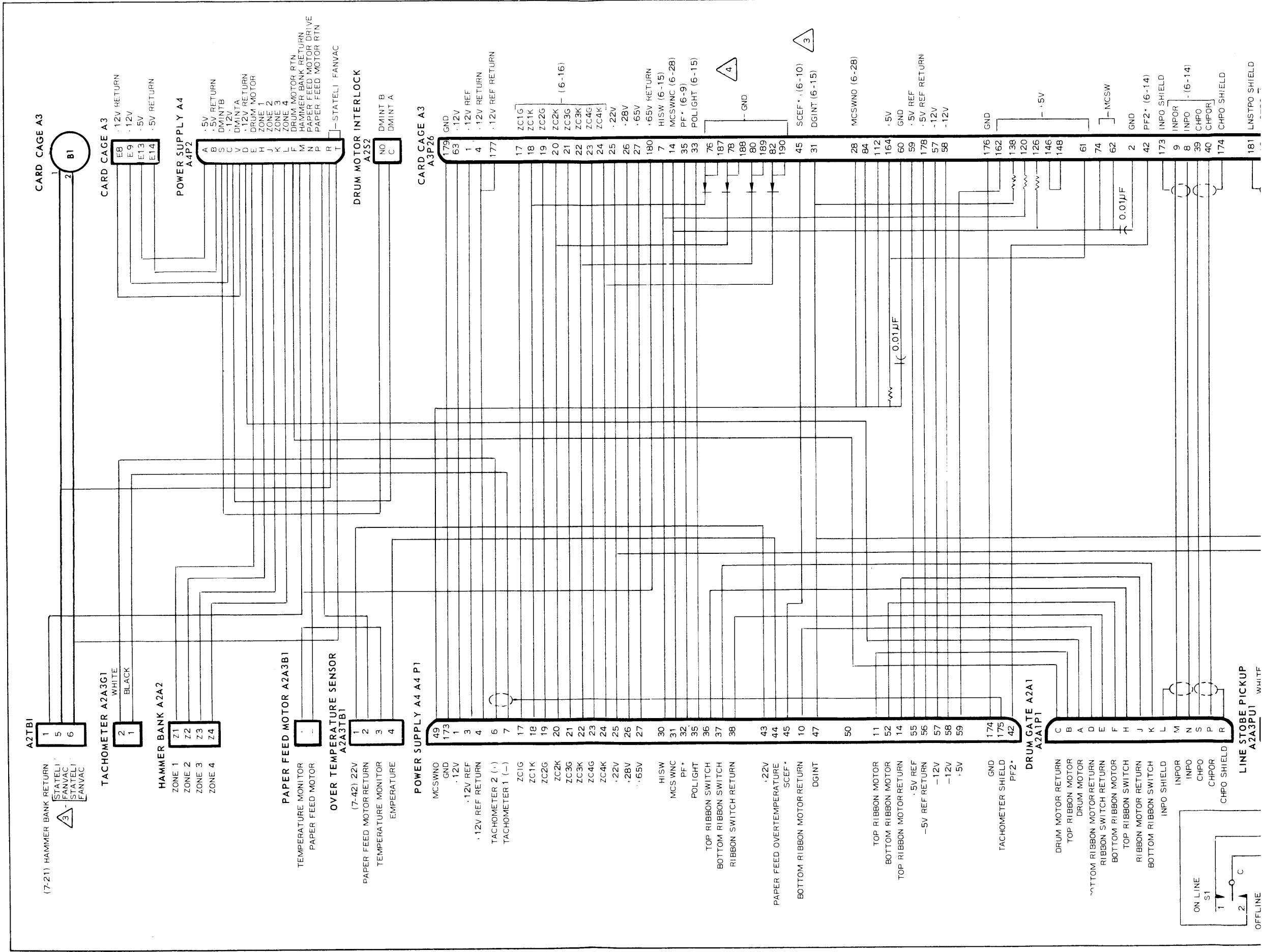
6-31 If J and K are high simultaneously, and E and P are inhibited, then the J-K flip-flop toggles to the state opposite that which it was prior to the arrival of the clock.

6-32 Inputs J and K Low

6-33 If J and K are low simultaneously and E and P are inhibited, then the J-K flip-flop cannot toggle and remains at the state that it was prior to the arrival of the clock.

6-34 Inputs E and P Low

6-35 This is an abnormal operating condition but if E and P should go low simultaneously, the J-K flip-flop acts on both conditions and outputs Q and Q\* go high at the same time.



A2TB1

(7-21) HAMMER BANK RETURN  
 STATELI FANVAC  
 STATELI FANVAC

TACHOMETER A2A3G1

WHITE  
 BLACK

HAMMER BANK A2A2

ZONE 1  
 ZONE 2  
 ZONE 3  
 ZONE 4

PAPER FEED MOTOR A2A3B1

TEMPERATURE MONITOR  
 PAPER FEED MOTOR

OVER TEMPERATURE SENSOR A2A3TB1

(7-42) 22V  
 PAPER FEED MOTOR RETURN  
 TEMPERATURE MONITOR  
 TEMPERATURE

POWER SUPPLY A4 A4 P1

MCSWNO  
 GND  
 .12V  
 .12V REF  
 .12V RETURN  
 .12V REF RETURN  
 TACHOMETER 2 (-)  
 TACHOMETER 1 (-)

CARD CAGE A3

B1

CARD CAGE A3

E8 .12V RETURN  
 E9 .12V  
 E13 .5V  
 E14 .5V RETURN

POWER SUPPLY A4 A4P2

A .5V RETURN  
 B .5V RETURN  
 C DMINT B  
 D DMINT A  
 V DMINT A  
 D .12V RETURN  
 E DRUM MOTOR  
 H ZONE 1  
 J ZONE 2  
 K ZONE 3  
 L ZONE 4  
 M DRUM MOTOR RTN  
 N HAMMER BANK RETURN  
 O PAPER FEED MOTOR DRIVE  
 P PAPER FEED MOTOR RTN  
 R  
 T -STATELI FANVAC

DRUM MOTOR INTERLOCK A2A2

NO  
 DMINT B  
 DMINT A  
 C

CARD CAGE A3 A3P26

179 GND  
 63 .12V  
 1 .12V REF  
 4 .12V RETURN  
 177 .12V REF RETURN

17 ZC1G  
 18 ZC1K  
 19 ZC2G  
 20 ZC2K  
 21 ZC3G  
 22 ZC3K  
 23 ZC4G  
 24 ZC4K  
 25 .22V  
 26 .28V  
 27 .65V  
 180 .65V RETURN  
 7 HISW (6-15)  
 14 MCSWNC (6-28)  
 35 PF\* (6-9)  
 33 POLIGHT (6-15)

76  
 187  
 78  
 188  
 80  
 189  
 82  
 190  
 45 SCEF\* (6-10)  
 31 DGINT (6-15)

28 MCSWNO (6-28)  
 84  
 112  
 164 .5V  
 60 GND  
 59 .5V REF  
 178 .5V REF RETURN  
 57 -12V  
 58 -12V

176 GND

162  
 138  
 120  
 126  
 146  
 148  
 61  
 74  
 62

2 GND  
 PF2\* (6-14)  
 173 INPO SHIELD  
 9 INPOR  
 8 INPO (-6-14)  
 39 CHPO  
 40 CHPOR  
 174 CHPO SHIELD  
 181 LNSTPO SHIELD

DRUM GATE A2A1 A2A1P1

C  
 B  
 A  
 D  
 E  
 F  
 H  
 J  
 K  
 L  
 M  
 N  
 S  
 P  
 R

LINE STROBE PICKUP A2A3PUI WHITE

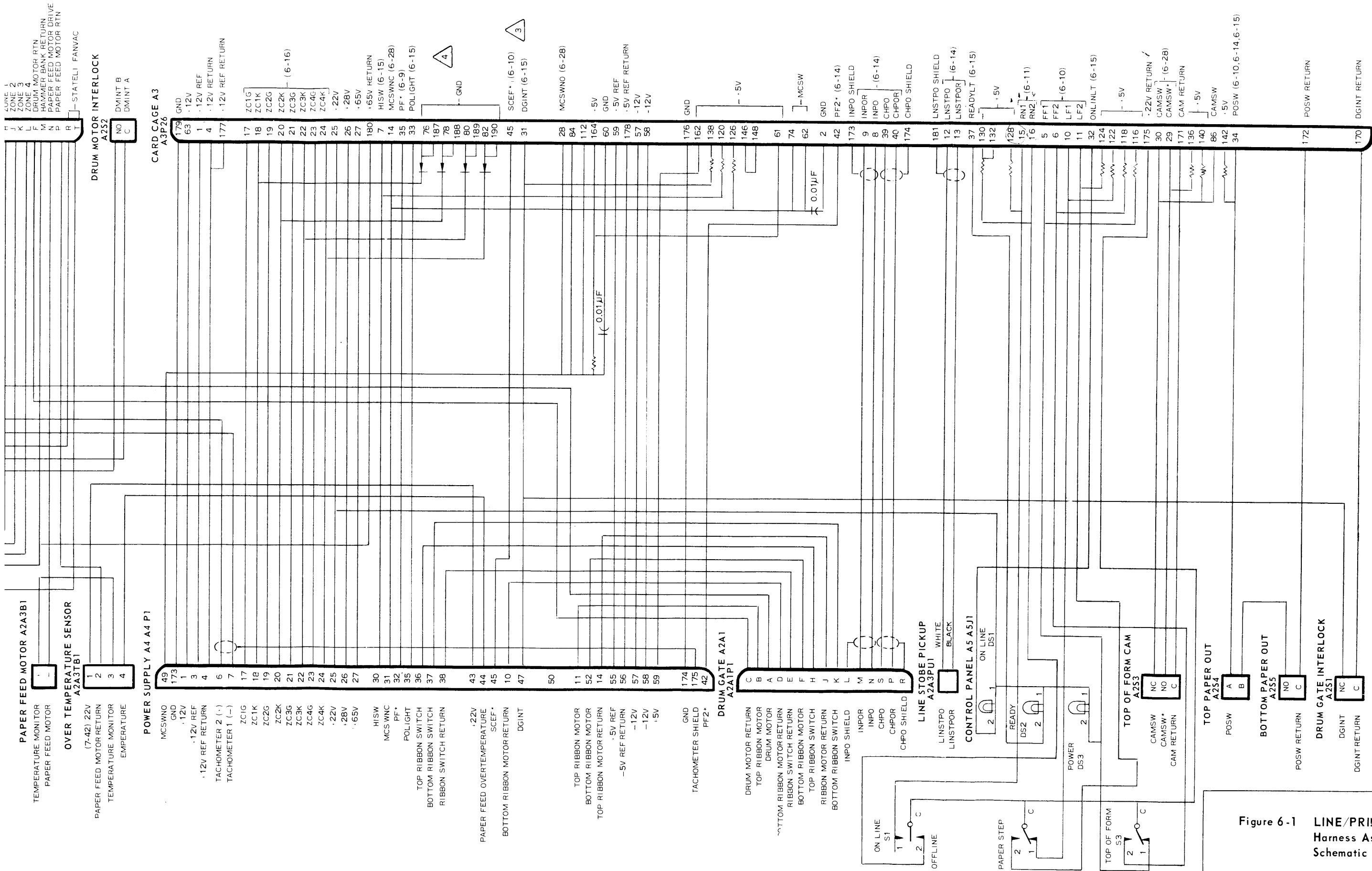


Figure 6-1 LINE/PRINTER Model 2310  
 Harness Assembly  
 Schematic Diagram

- NOTE:
1. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1K, 5%, 1/4 WATT
  2. REF DPC WL216492B
  3. EFFECTIVE ON PRINTER SERIAL NUMBER 201 AND UP
  4. UNLESS OTHERWISE INDICATED ALL DIODES ARE DPC 600095-001

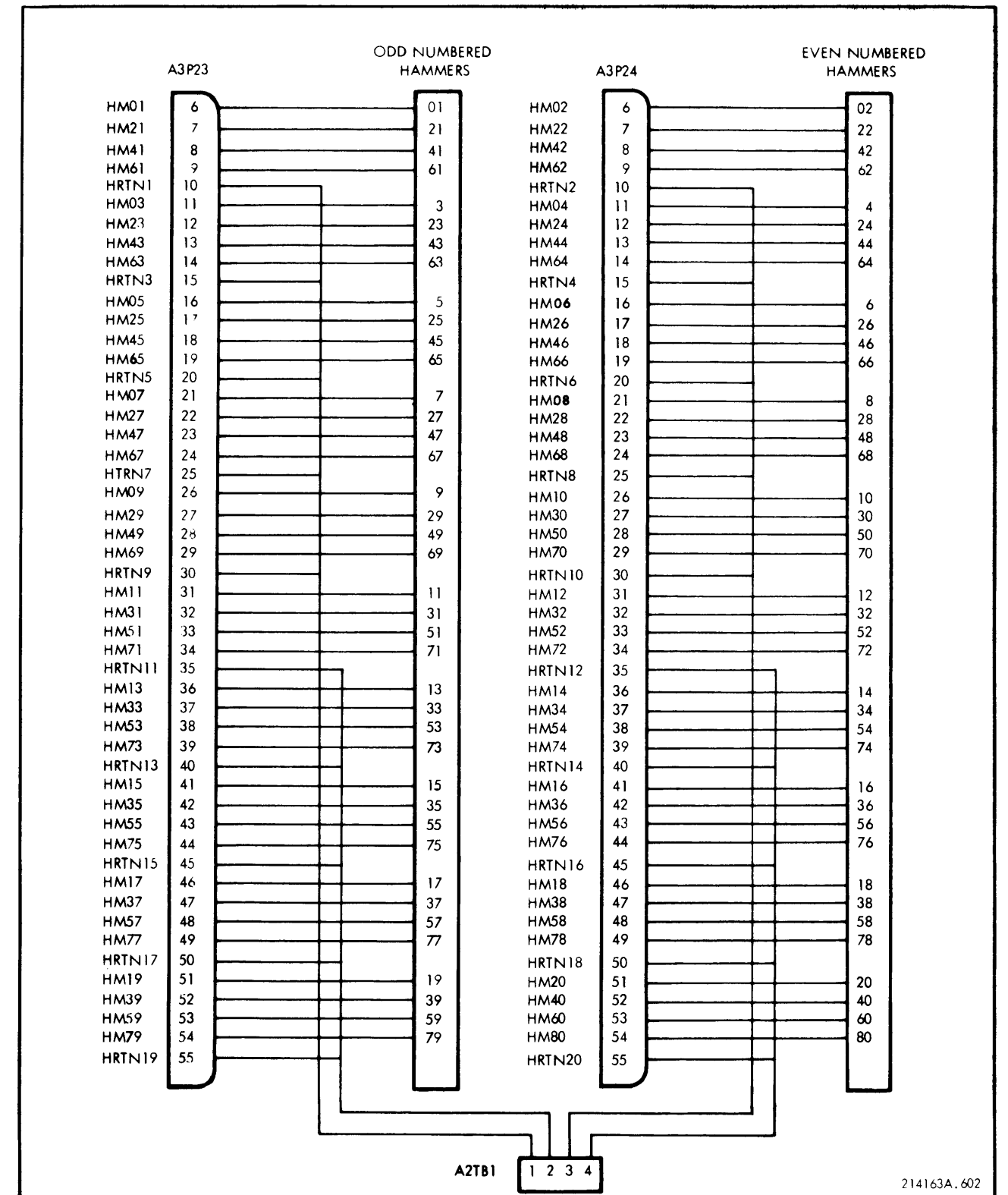


Figure 6-2. Hammer Bank A2A2 Harness Assembly Schematic Diagram

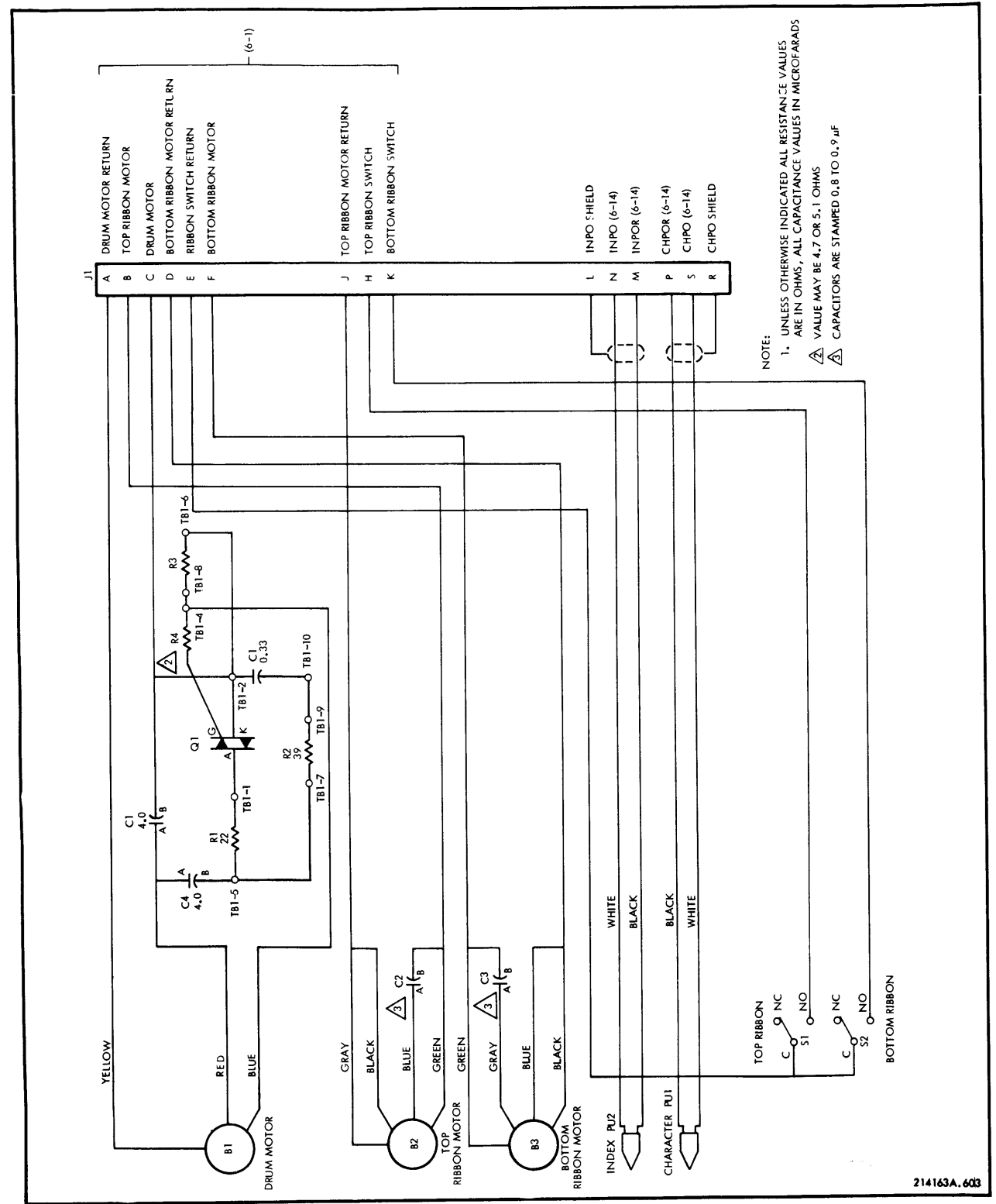
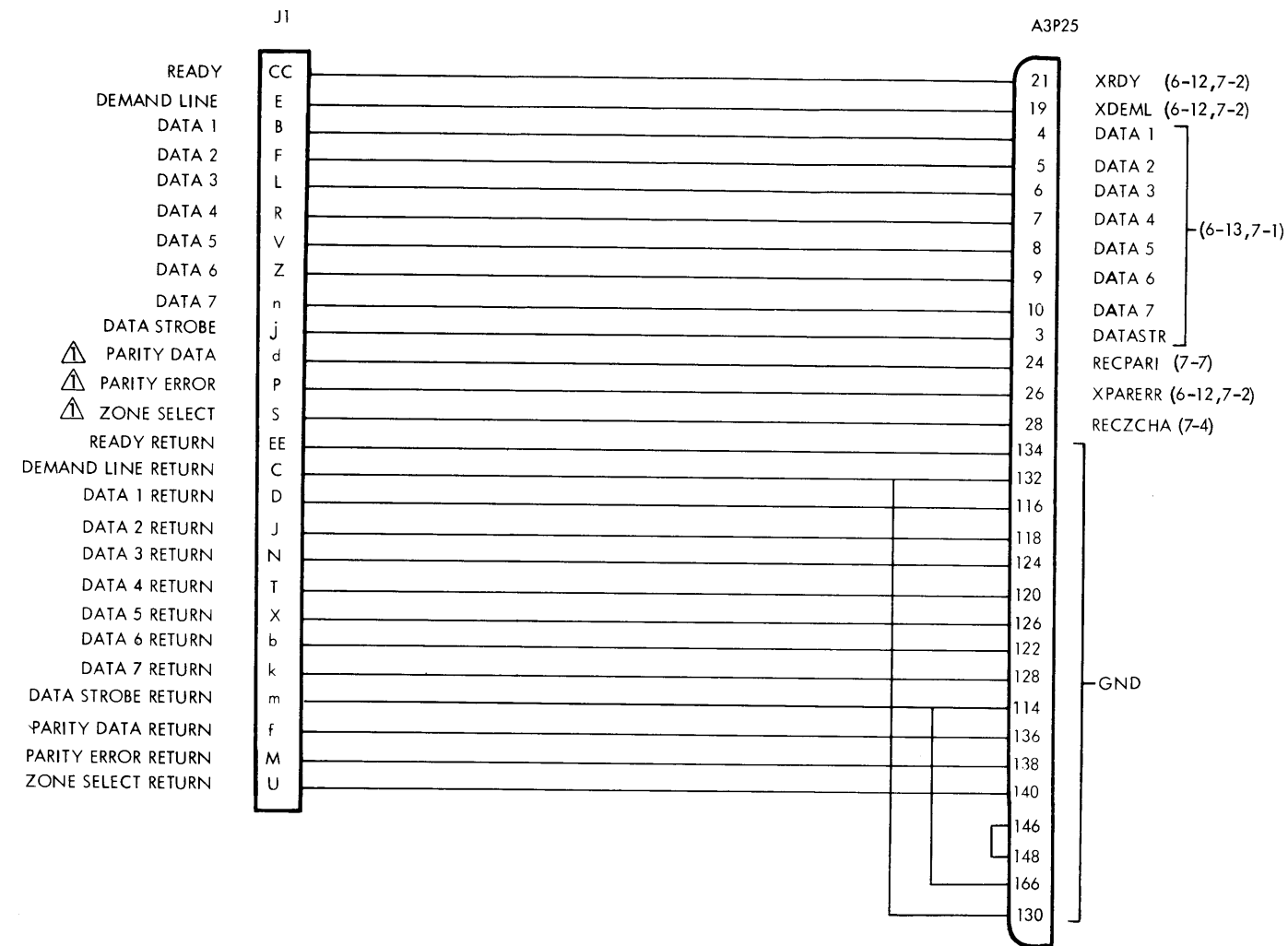
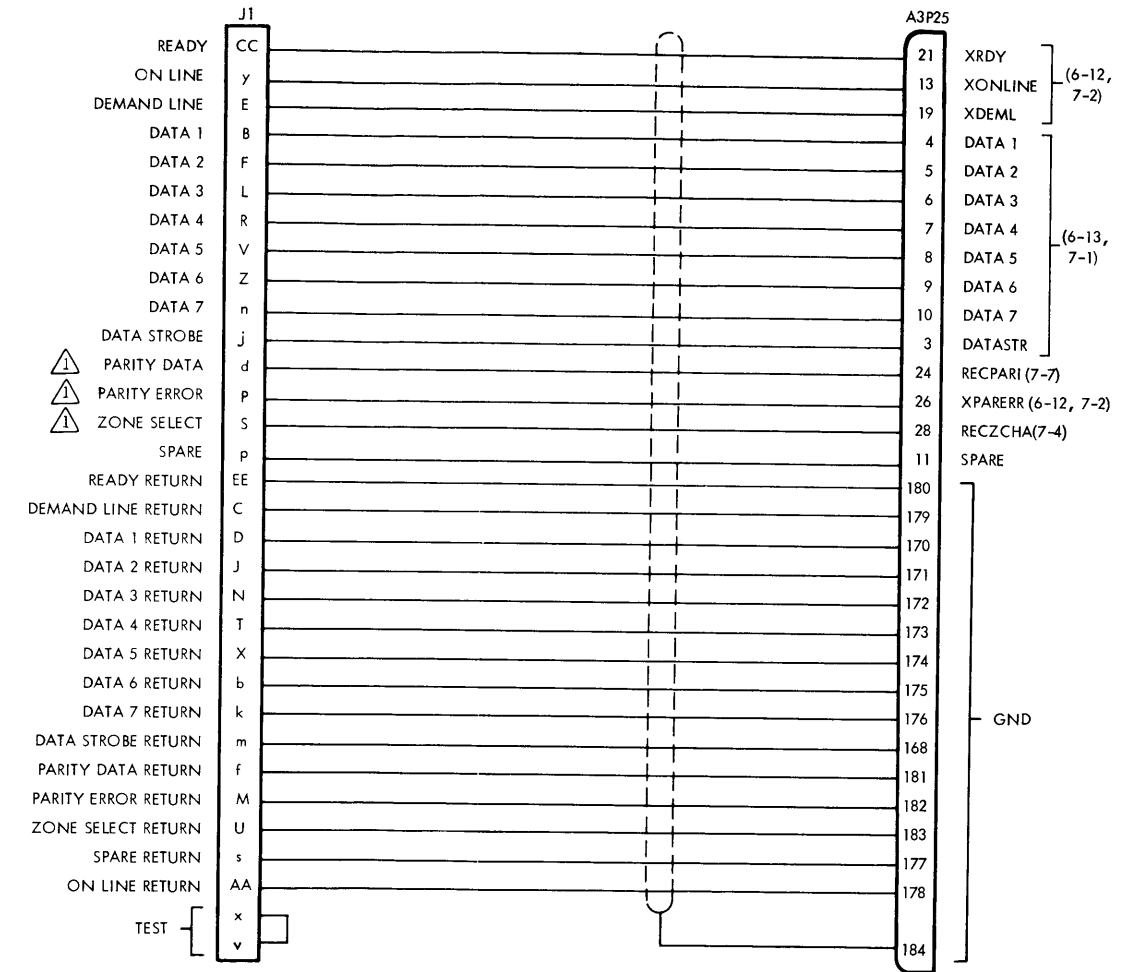


Figure 6-3. Drum Gate A2A1 Schematic Diagram (Printer Serial Numbers 026 Thru 128)



NOTE:  
 1. AVAILABLE AS OPTIONS  
 2. REF DPC WL212639-1E  
 3. EFFECTIVE ON PRINTER SERIAL NUMBERS 012 THRU 555



NOTE:  
 1. AVAILABLE AS OPTIONS  
 2. REF DPC WL212639-2E  
 3. EFFECTIVE ON PRINTER SERIAL NUMBER 556 AND UP

Figure 6-4. Input/Output Harness Assembly Schematic Diagram

DPC 214163 B

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(Reference Figure 6-1 for Details )

Figure 6-5



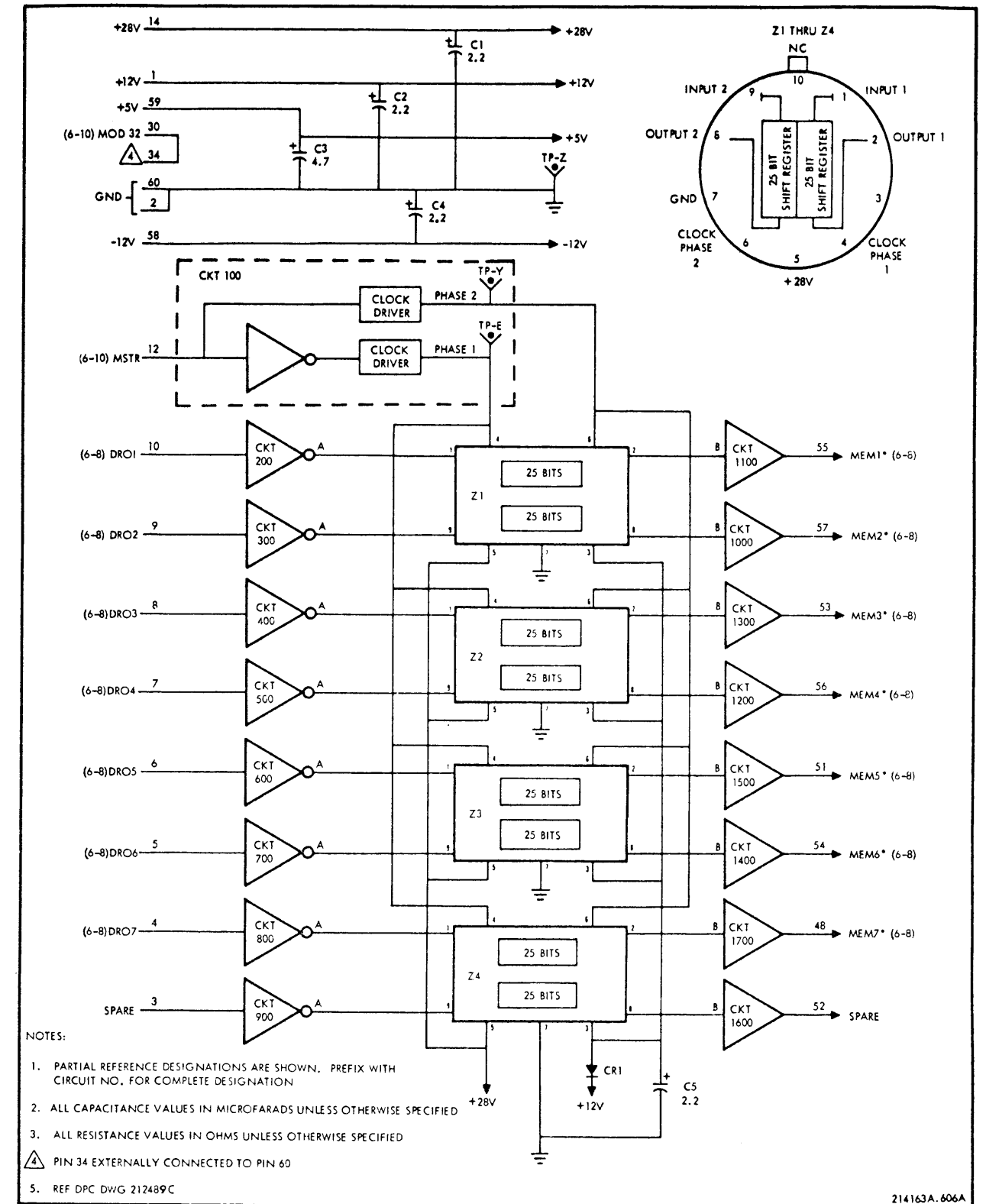


Figure 6-6. 25-Character Memory AM-10 Logic Diagram (Sheet 1 of 2)

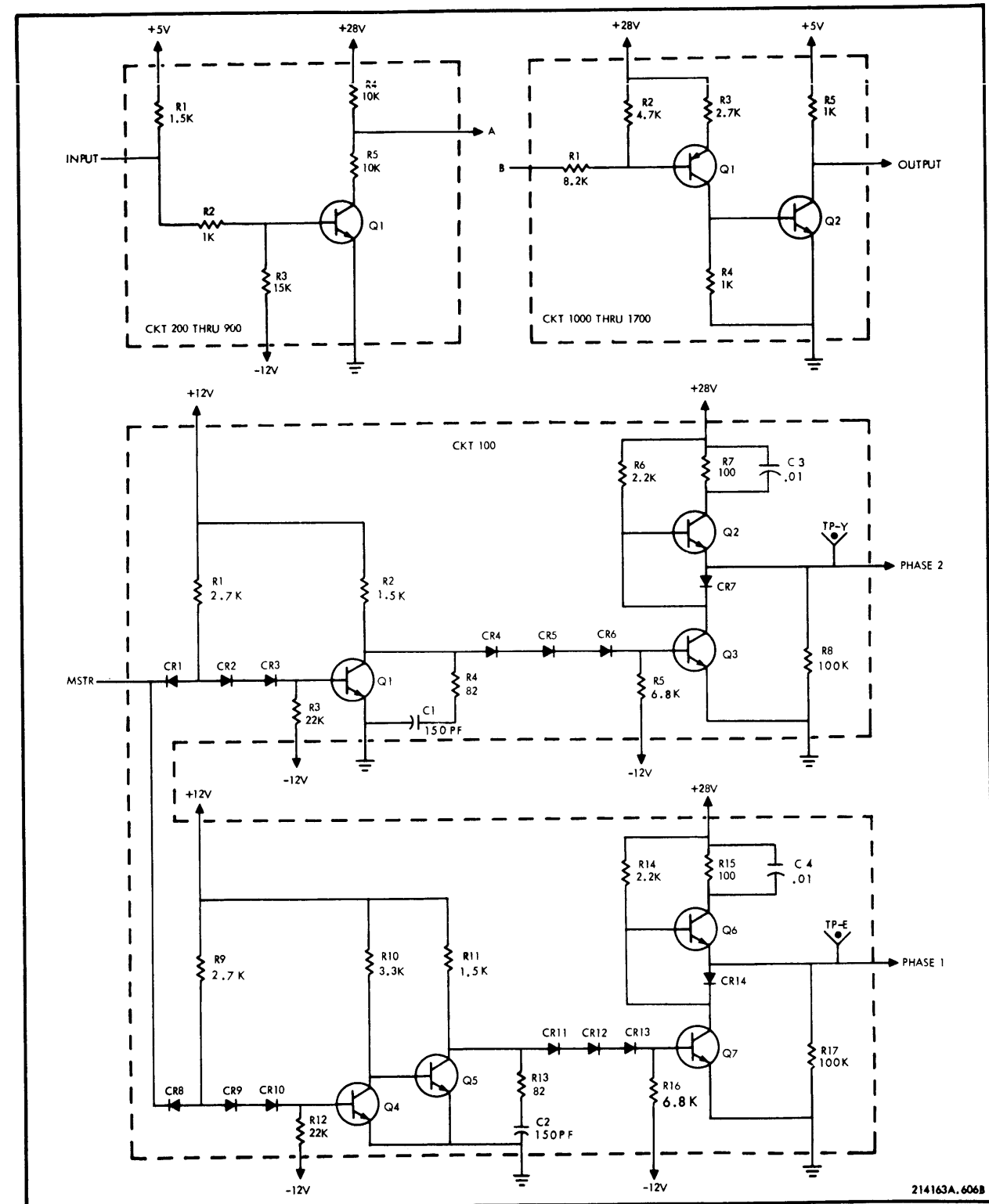
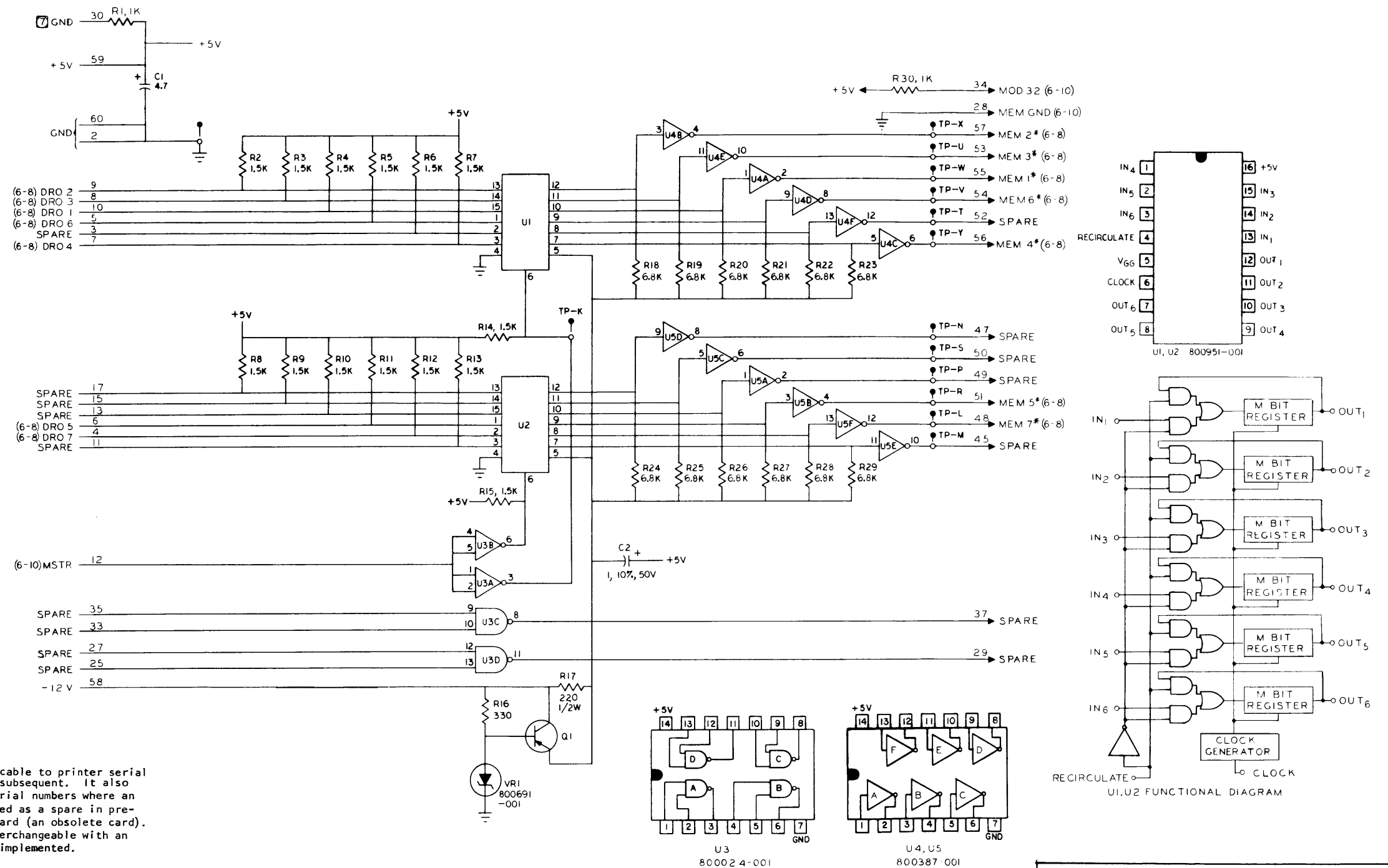


Figure 6-6. 25-Character Memory AM-10 Logic Diagram (Sheet 2 of 2)

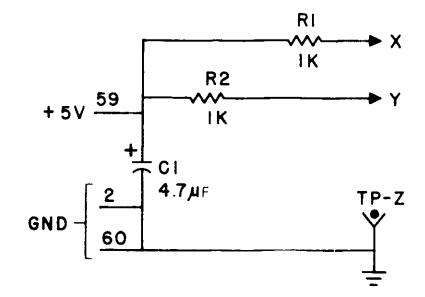
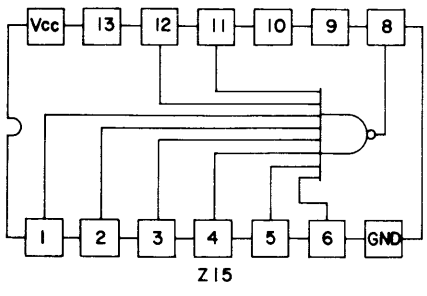
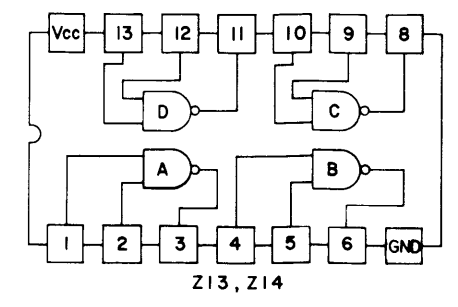
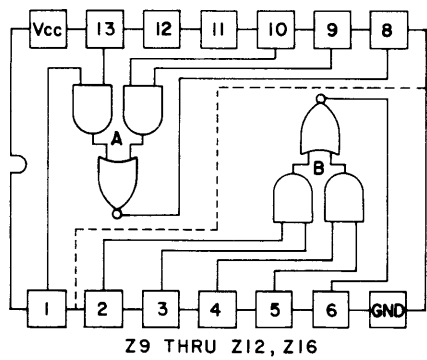
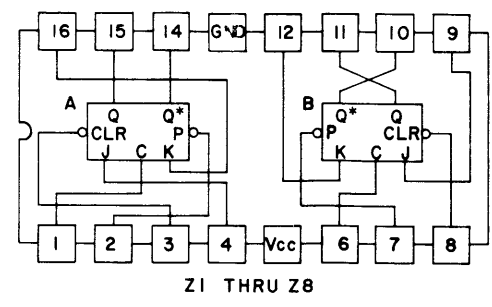
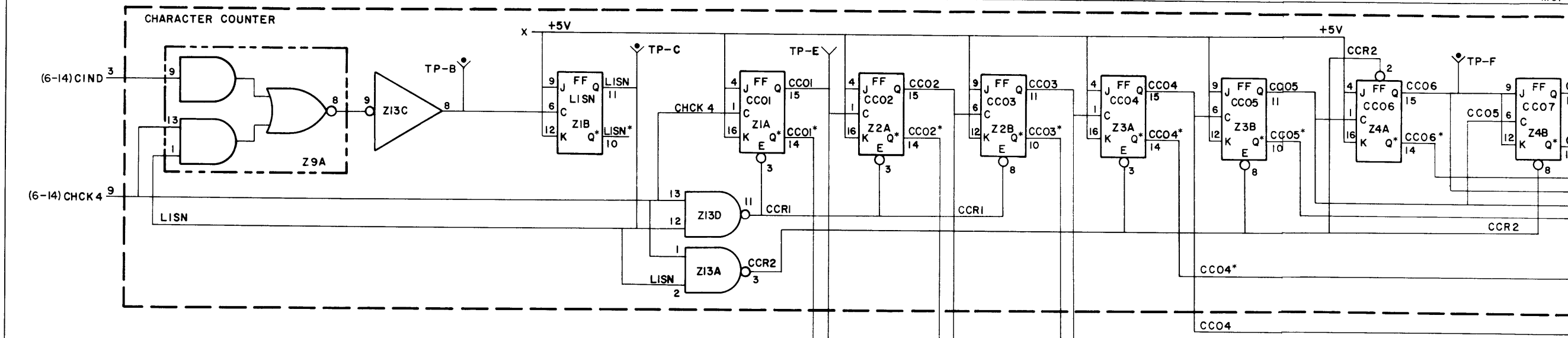
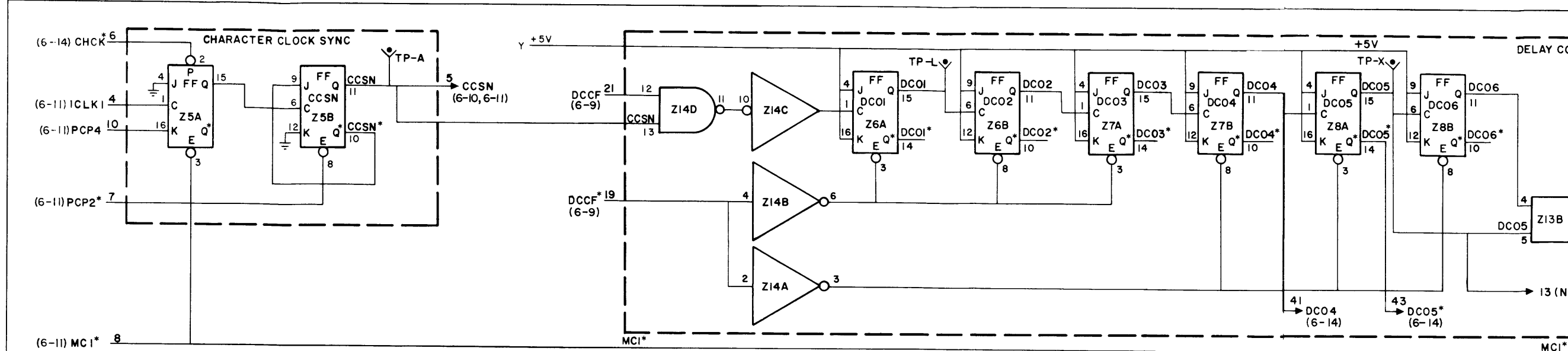


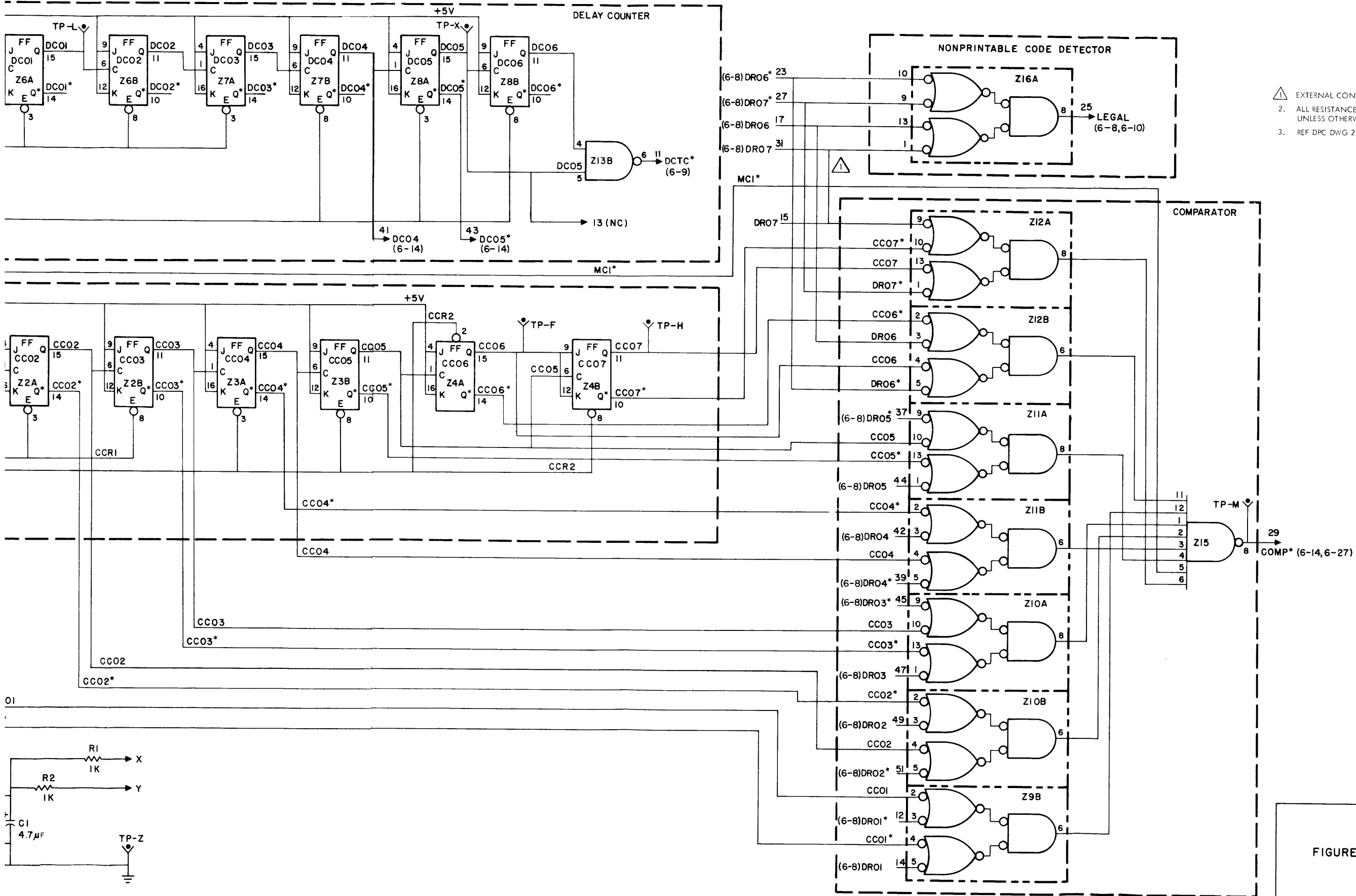
8. This drawing is applicable to printer serial numbers S/N 1739 and subsequent. It also applies to earlier serial numbers where an AM-21 card is furnished as a spare in preference to an AM-10 card (an obsolete card). AM-21 is directly interchangeable with an AM-10 if FC0 6331 is implemented.

- 7. PIN 30 CONNECTED EXTERNALLY TO PIN 2.
- 6. ASSEMBLY DRAWING NUMBER 233715
- 5. INTERPRET ELECTRONIC SYMBOLS PER 850026.
- 4. INTERPRET REFERENCE DESIGNATIONS PER 850027.
- 3. ALL TRANSISTORS ARE 800515-001
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 20%, 10 VOLTS.
- 1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES:

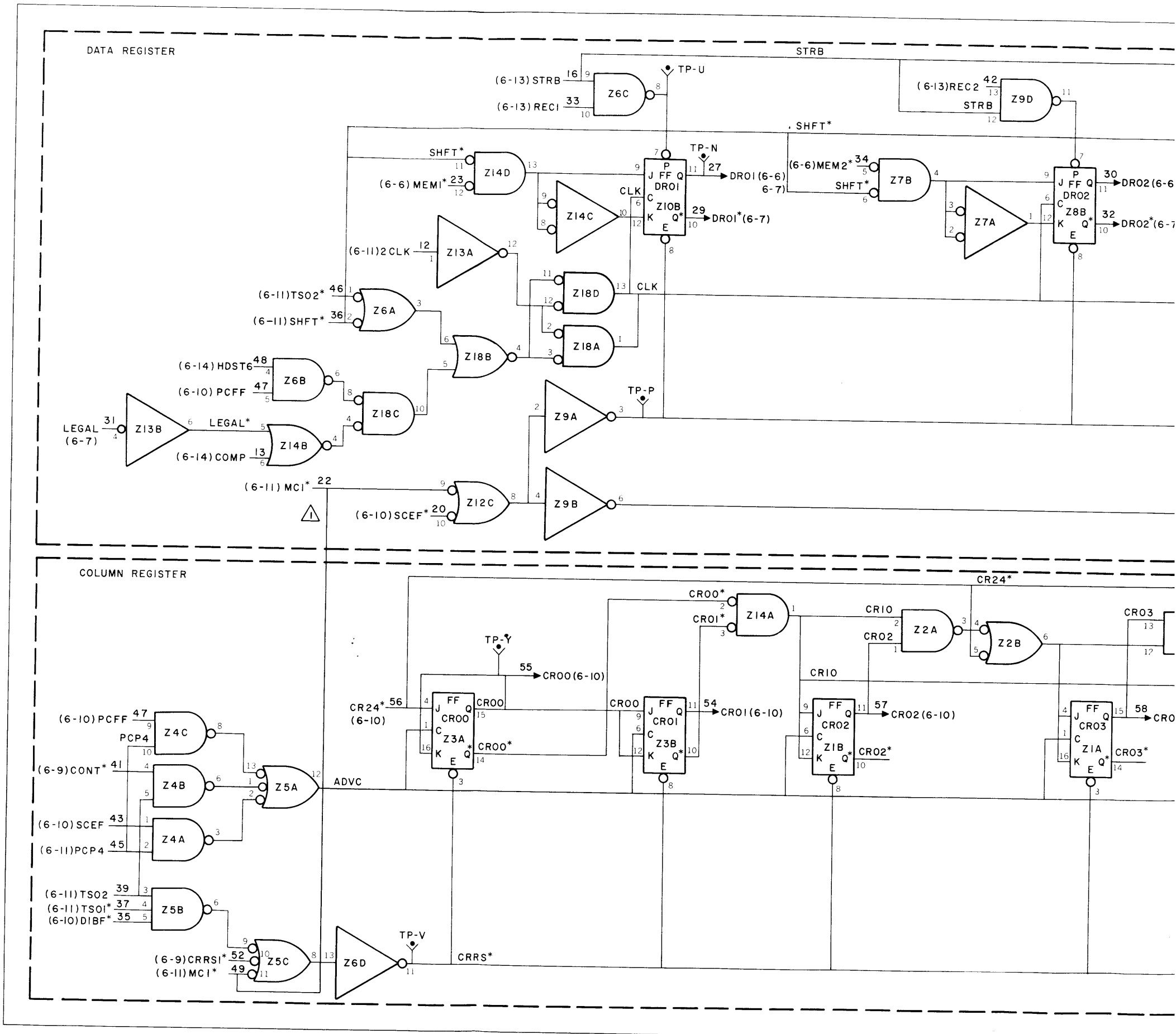
214163.606C  
 Figure 6-6a. 32-Character Memory AM-21 Logic Diagram (Ref. Des. A3A25)

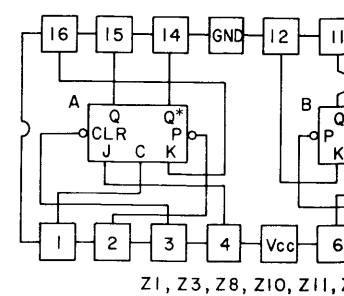
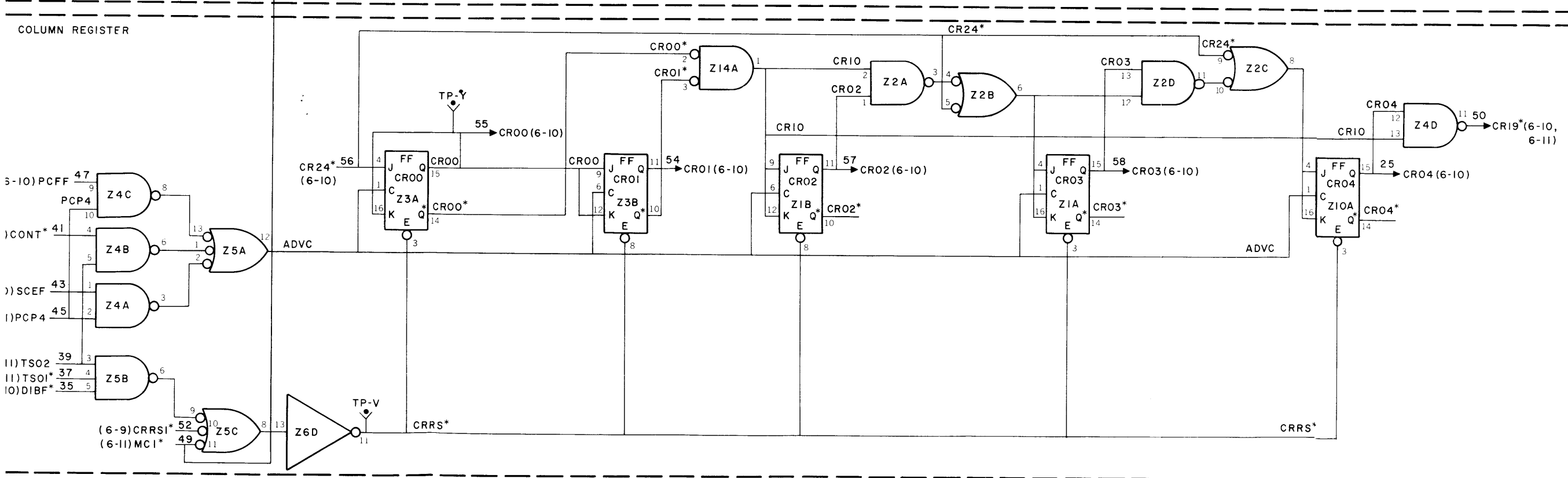
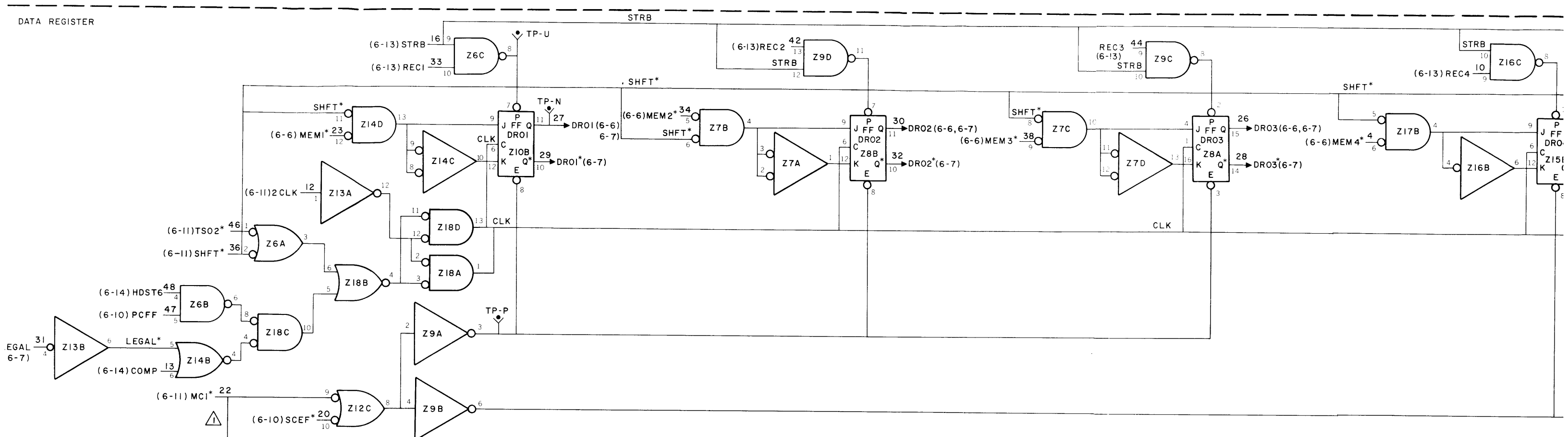




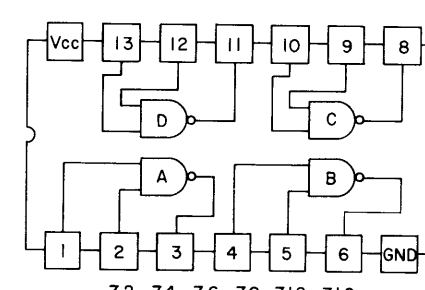
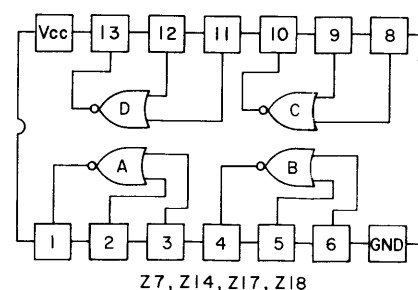
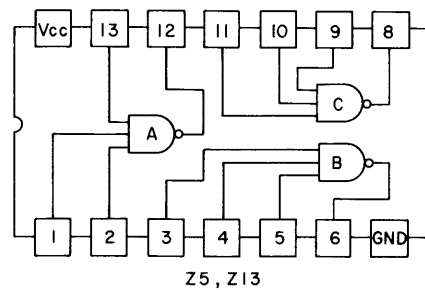
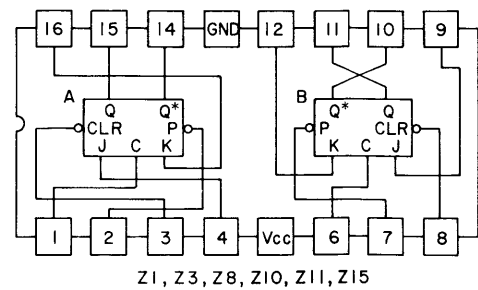
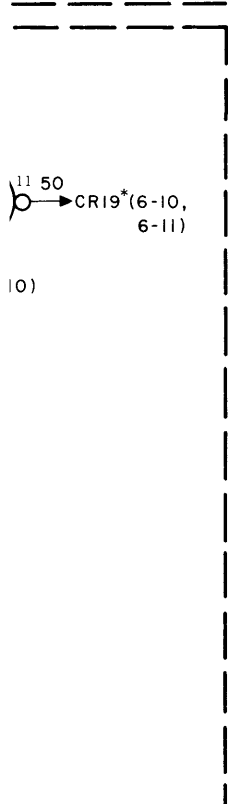
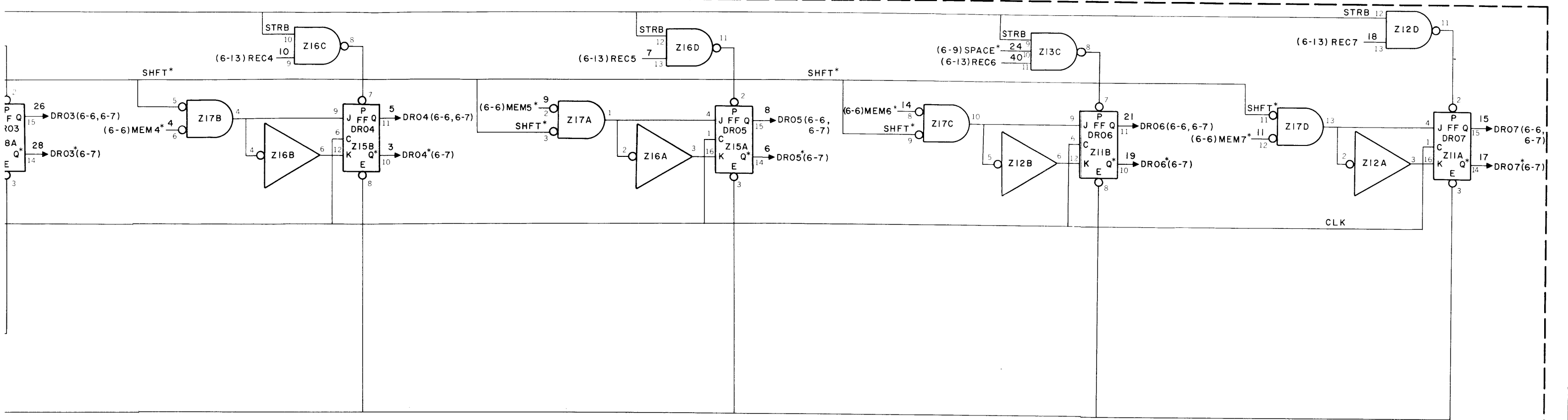
- 1. EXTERNAL CONNECTION
- 2. ALL RESISTANCE VALUES IN OHMS UNLESS OTHERWISE SPECIFIED
- 3. REF DPC DWG 212524B

FIGURE 6-7. LOGIC GATE I AG-17 LOGIC DIAGRAM





NOTES:  
 1. EXTERNAL CONNECTION  
 2. REF DPCDWG 212529A



NOTES:  
 ▲ EXTERNAL CONNECTION  
 2. REF DPCDWG 212529A

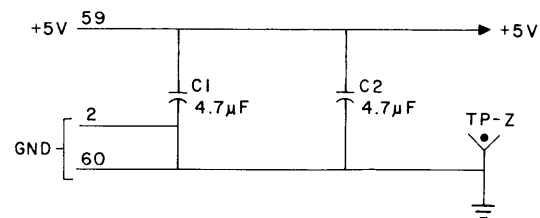
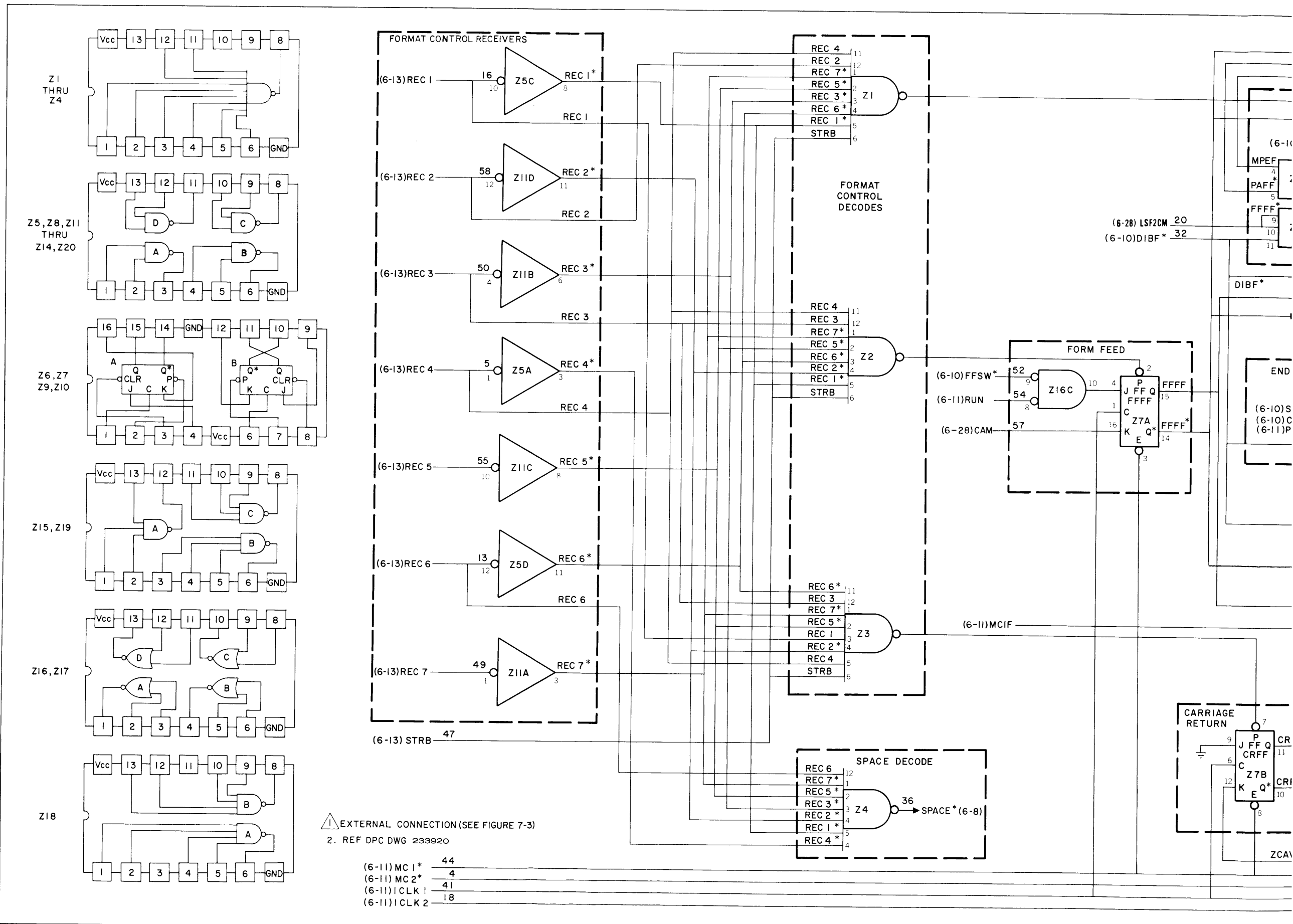


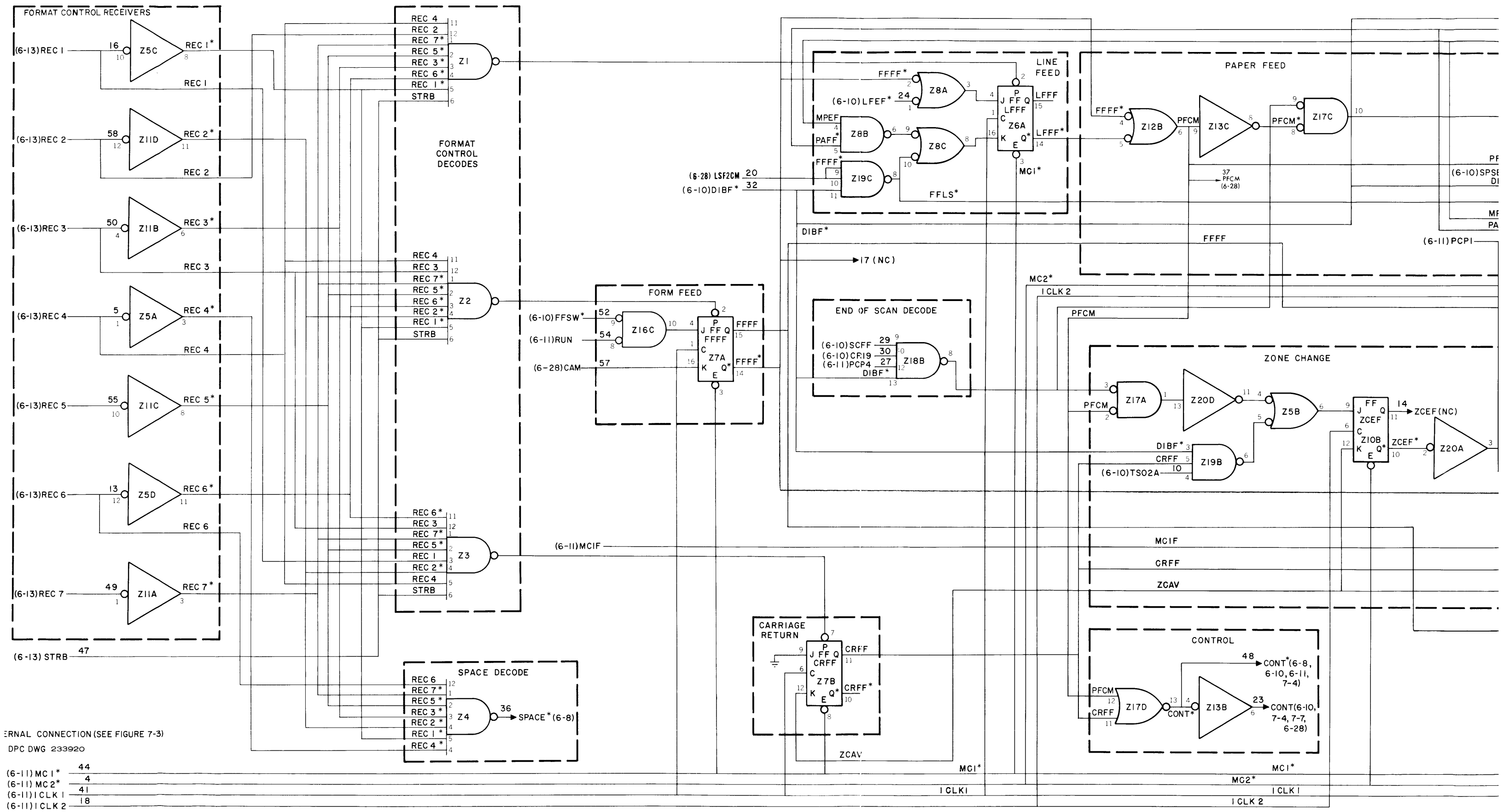
FIGURE 6-8. LOGIC GATE II AG-18, LOGIC DIAGRAM



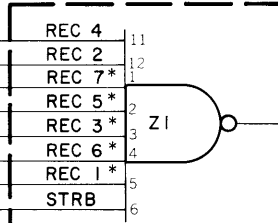
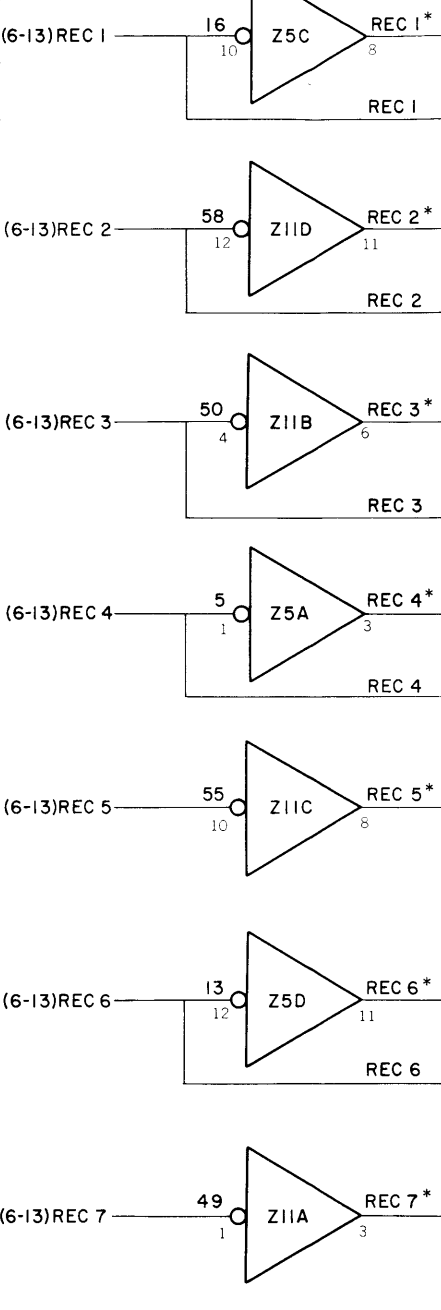


⚠ EXTERNAL CONNECTION (SEE FIGURE 7-3)  
 2. REF DPC DWG 233920

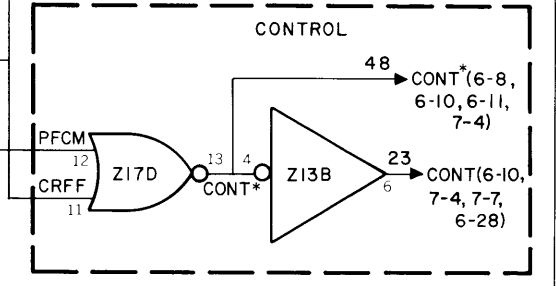
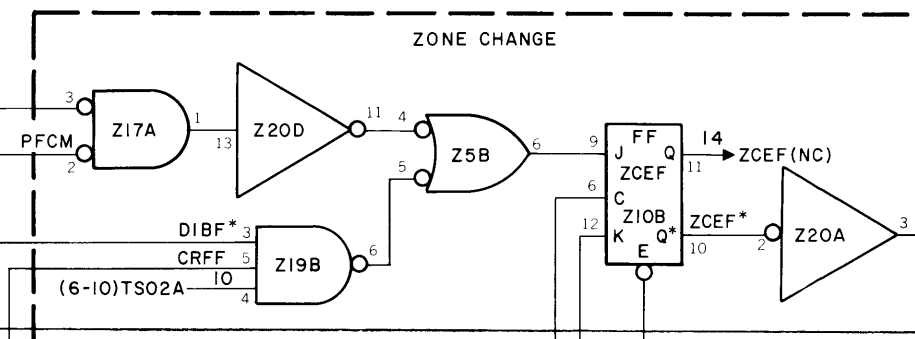
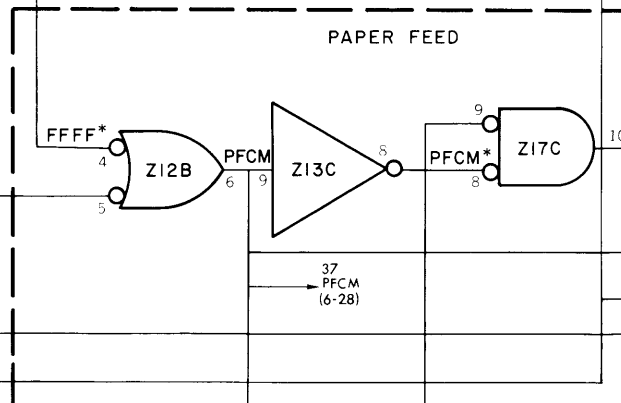
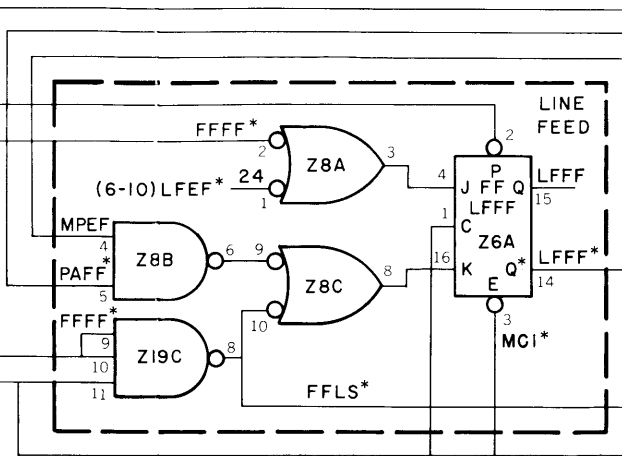
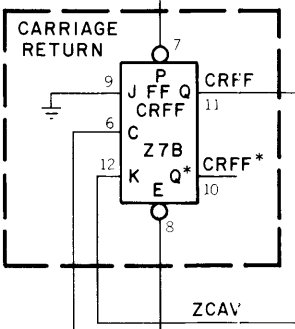
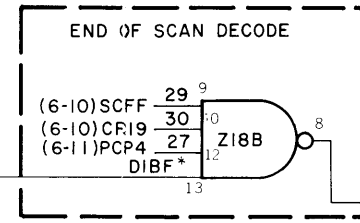
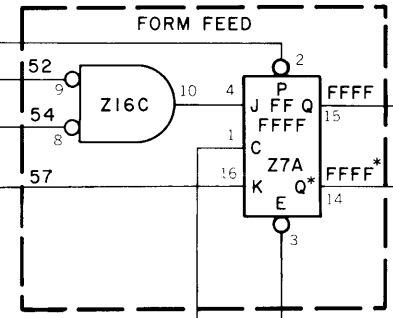
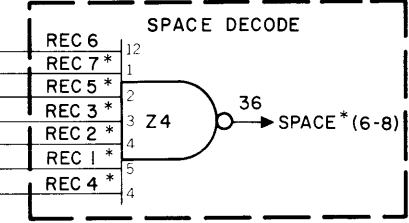
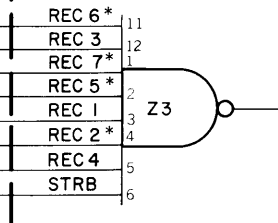
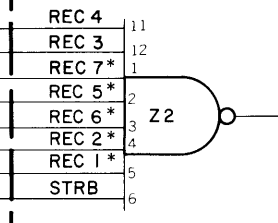
- (6-11) MC 1\* 44
- (6-11) MC 2\* 4
- (6-11) CLK 1 41
- (6-11) CLK 2 18



FORMAT CONTROL RECEIVERS



FORMAT CONTROL DECODES



INTERNAL CONNECTION (SEE FIGURE 7-3)  
DPC DWG 233920

(6-11) MC 1*	44
(6-11) MC 2*	4
(6-11) ICLK 1	41
(6-11) ICLK 2	18

PF  
(6-10) SPSE  
DI  
MF  
PA

I CLK 1  
I CLK 2  
MC 1\*  
MC 2\*  
ZCAV  
CRFF  
MCIF  
PFCM

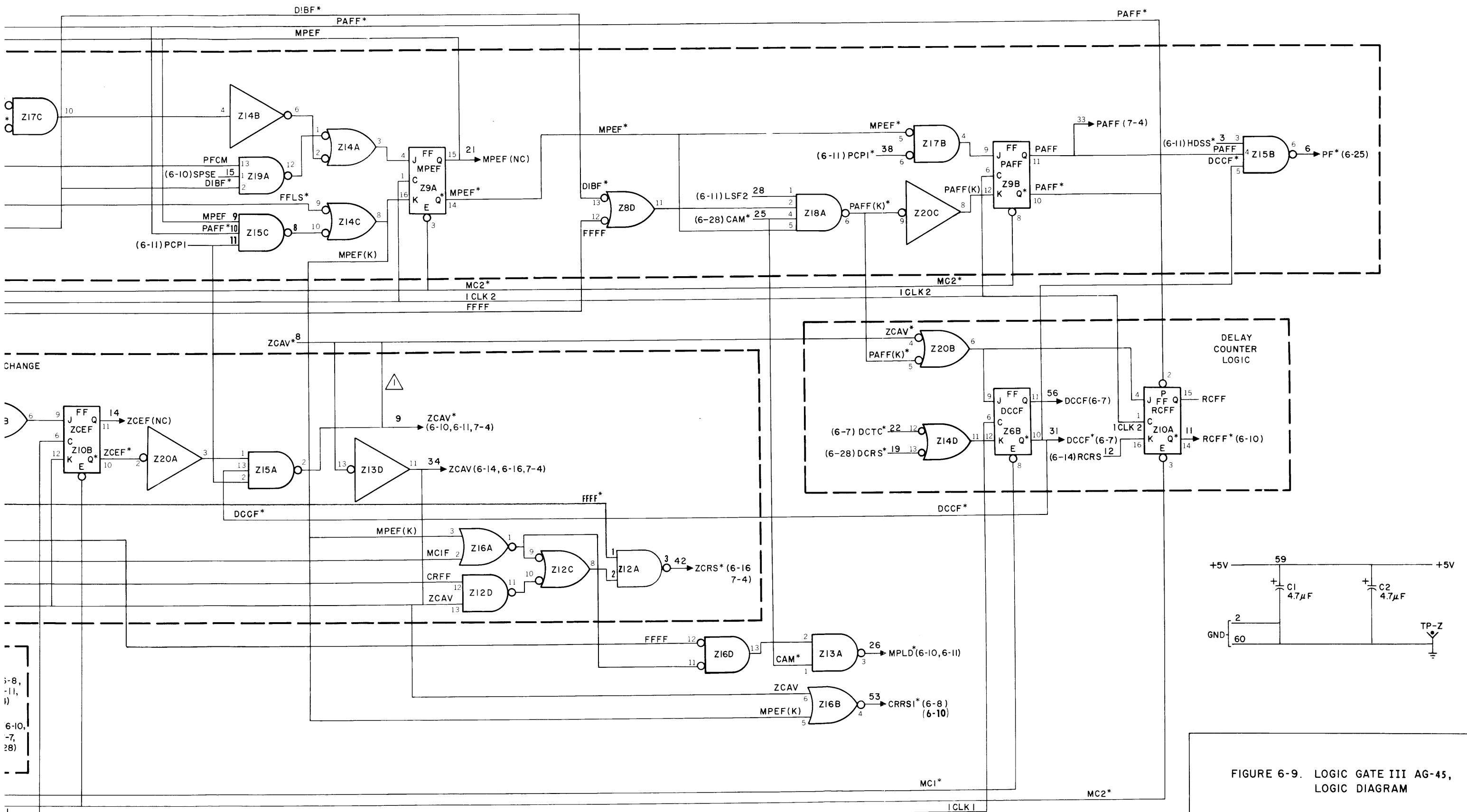
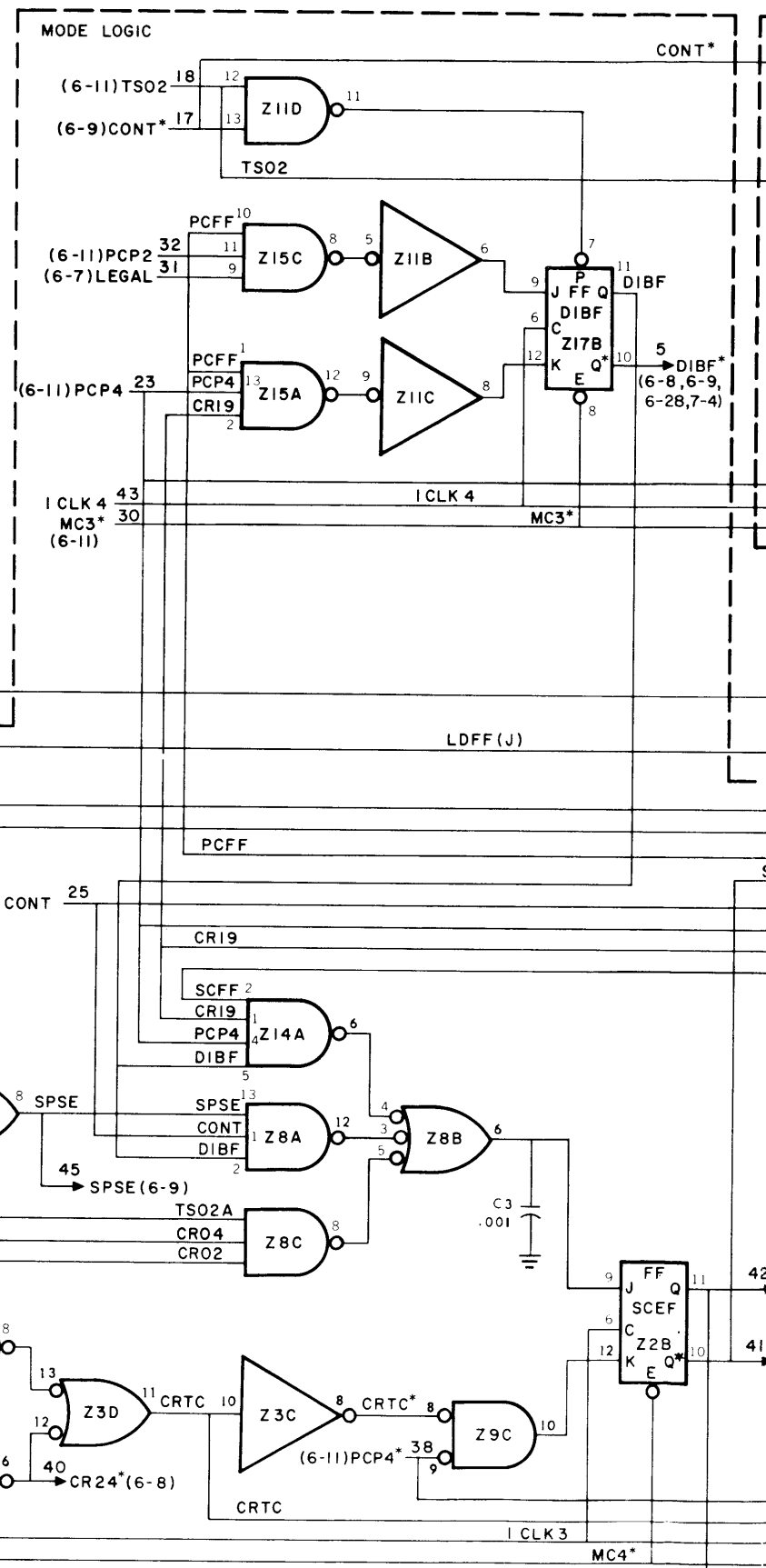
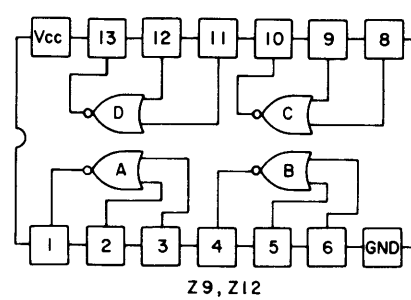
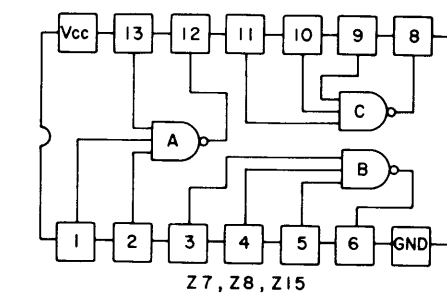
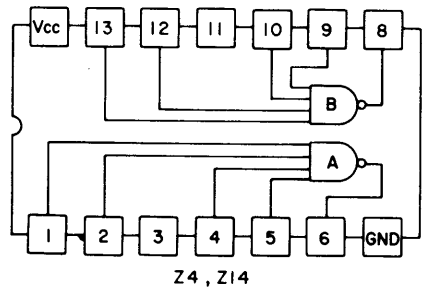
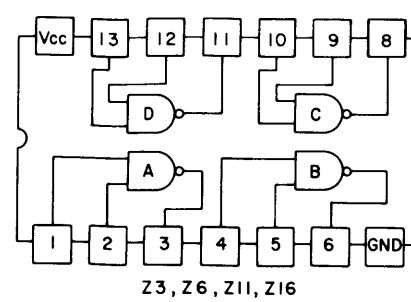
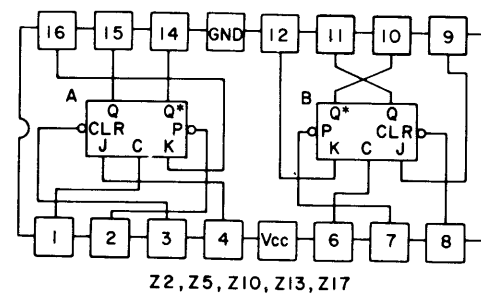
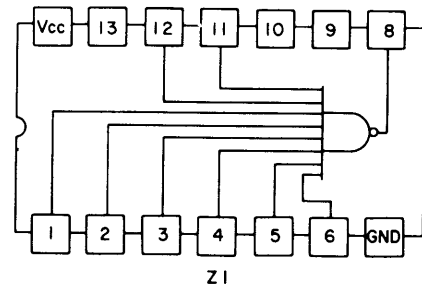
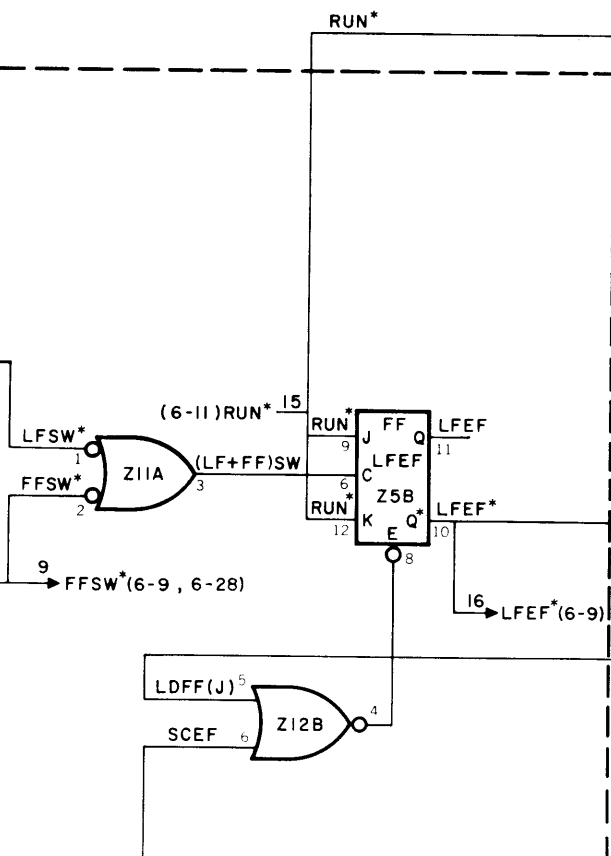
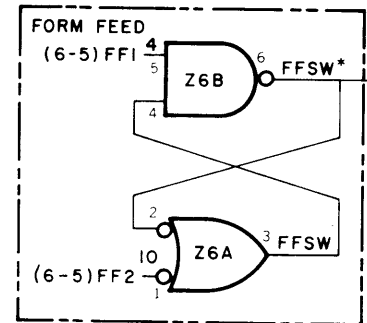
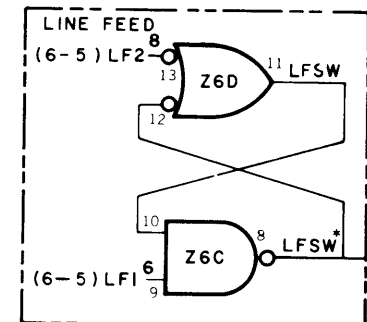


FIGURE 6-9. LOGIC GATE III AG-45, LOGIC DIAGRAM



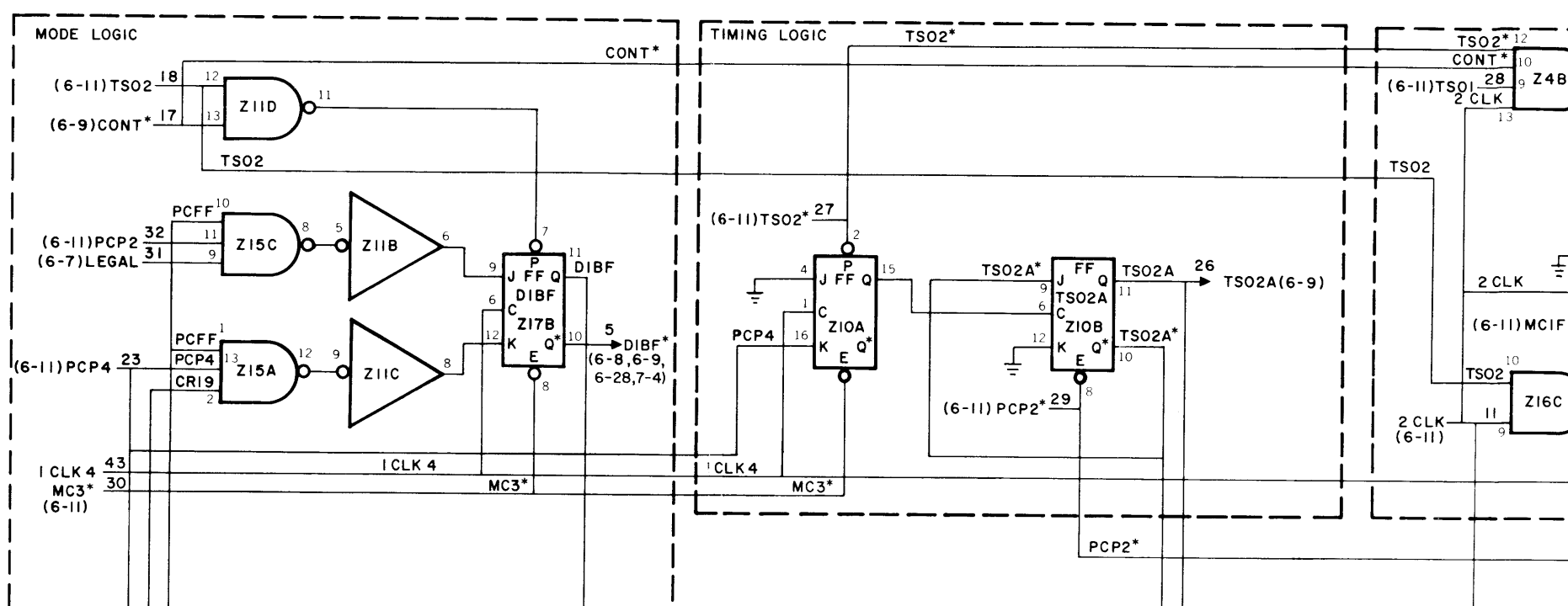
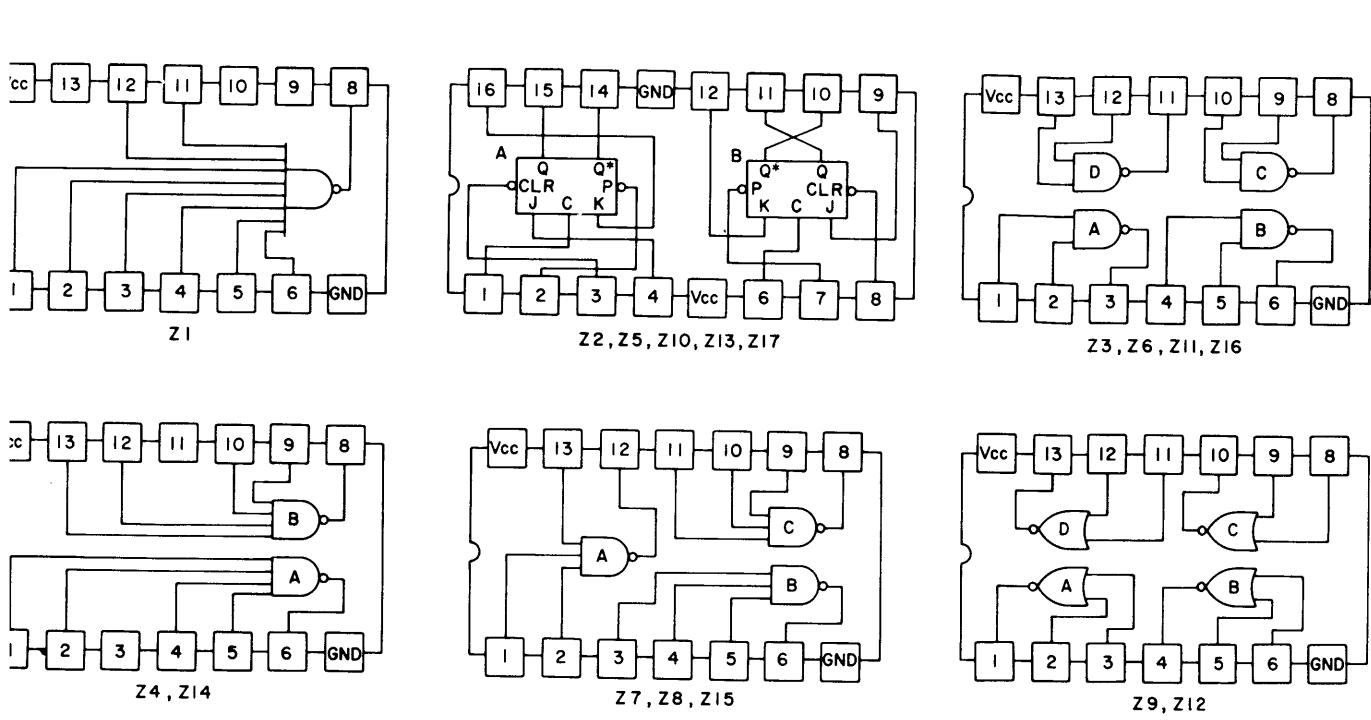
MANUAL FORMAT CONTROL



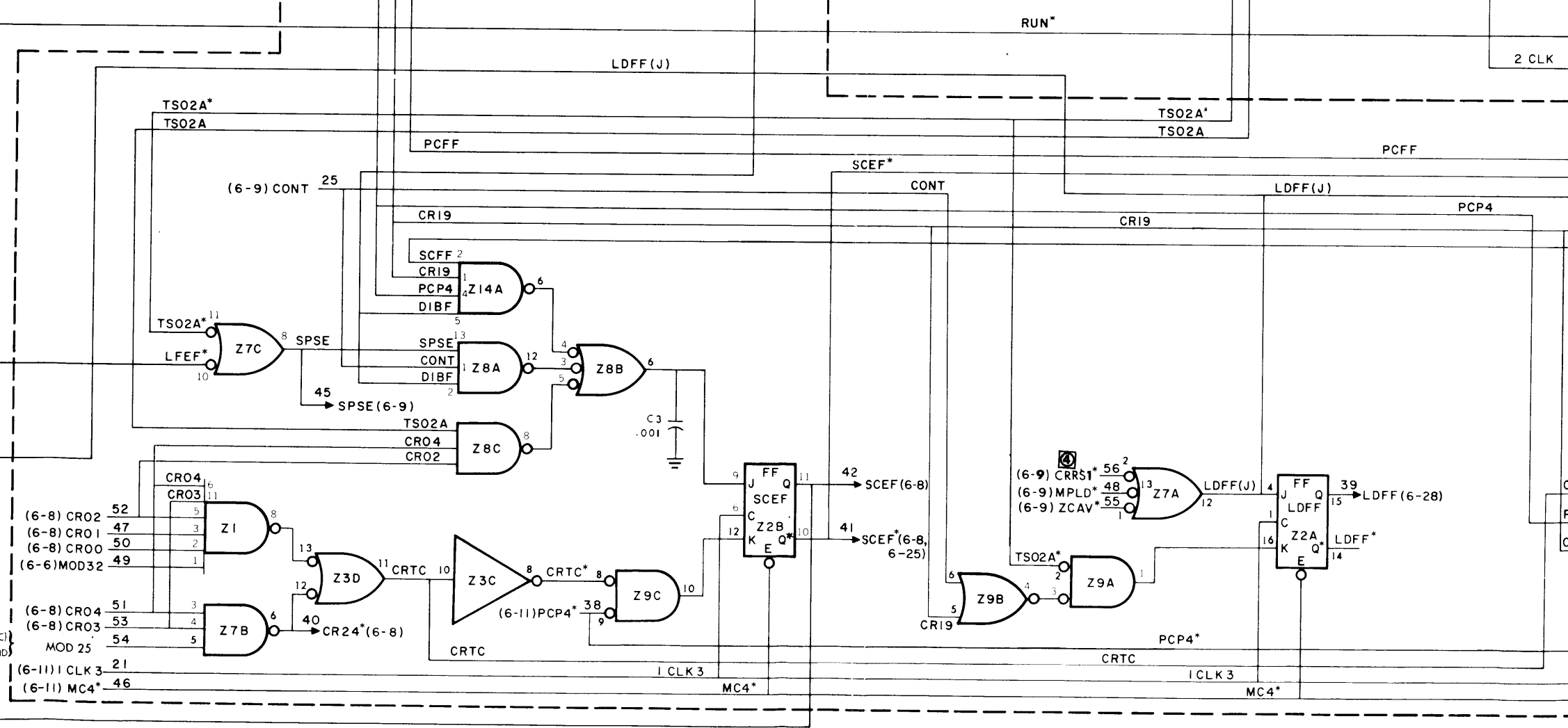
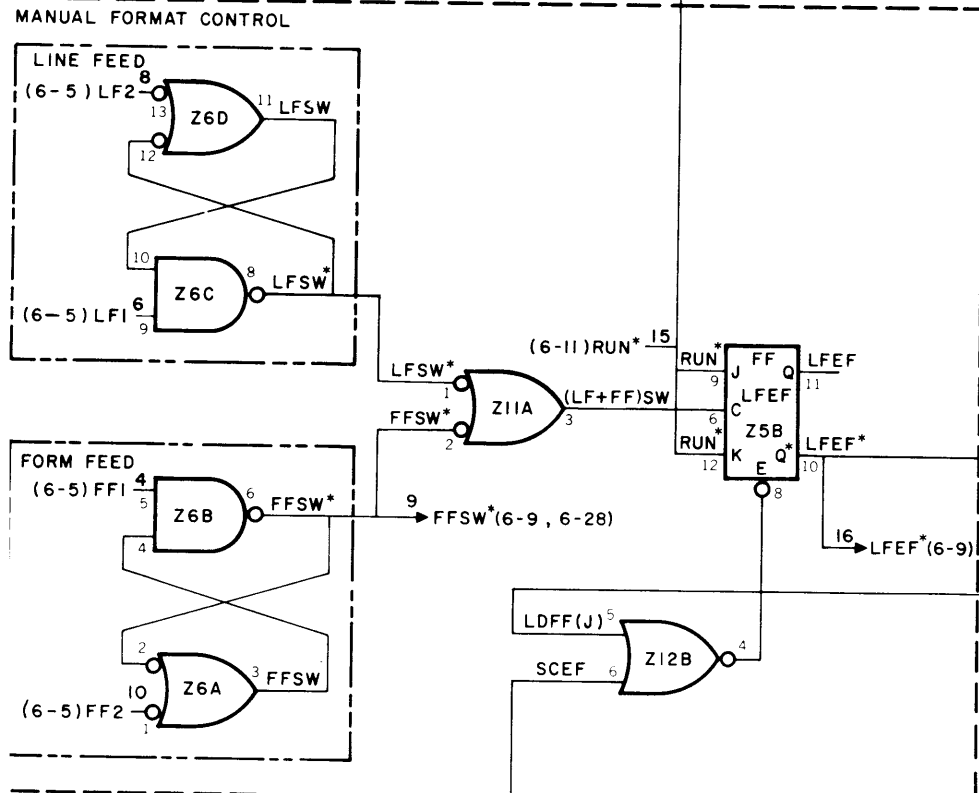
NOTES:

- 1 REF DPC DWG 212539B
- 2 APPLICABLE WITH AM-10 CIRCUIT TYPE
- 3 APPLICABLE WITH AM-21 CIRCUIT TYPE
- 4 EFFECTIVE ON PRINTER SERIAL NUMBER 326 AND UP

(6-6A) MEM GND



**MANUAL FORMAT CONTROL**



TES:  
 REF DPC DWG 212539B  
 APPLICABLE WITH AM-10 CIRCUIT TYPE  
 APPLICABLE WITH AM-21 CIRCUIT TYPE  
 EFFECTIVE ON PRINTER SERIAL NUMBER 326 AND UP

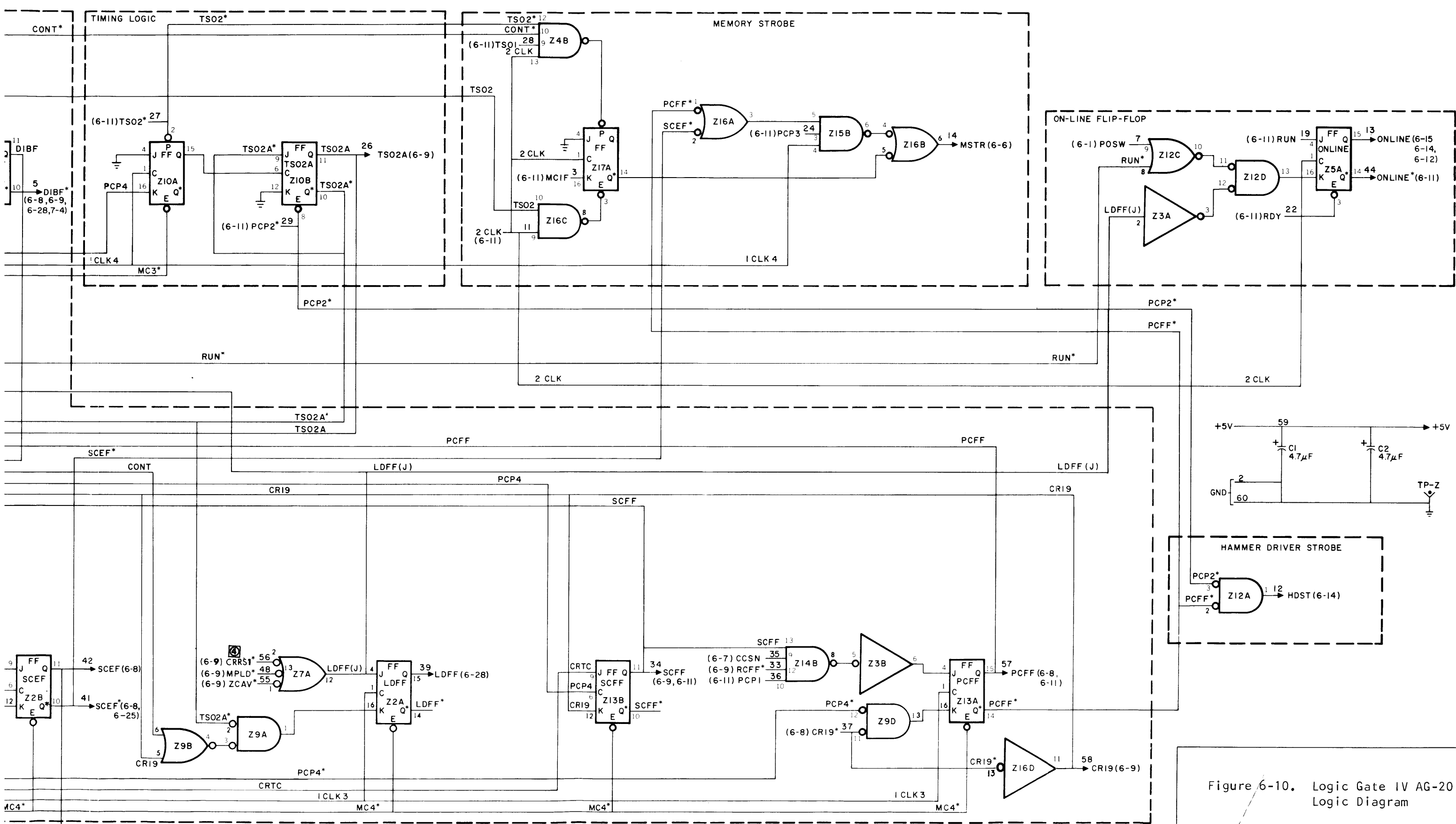
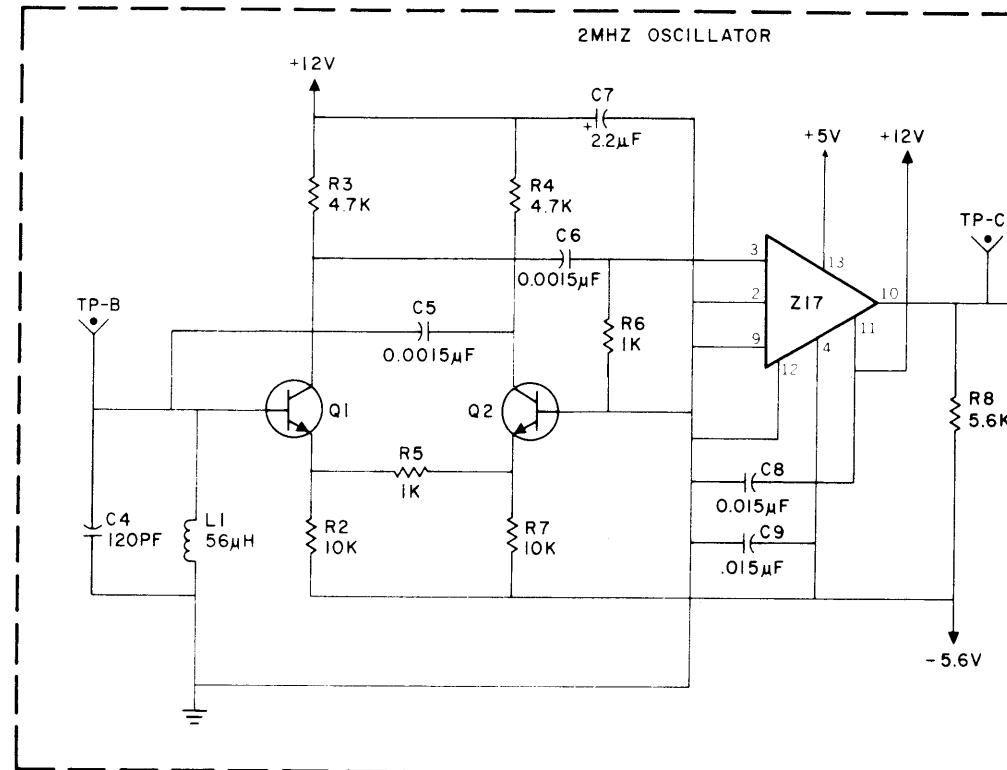
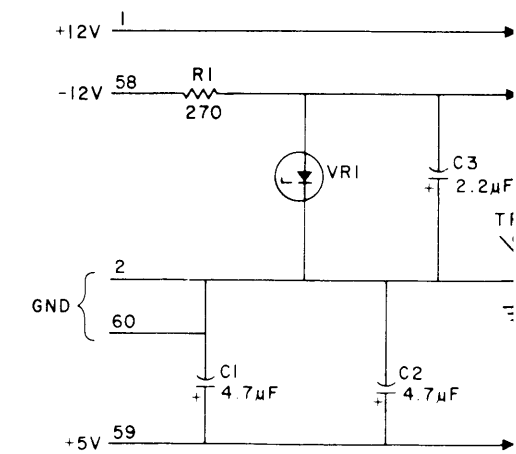
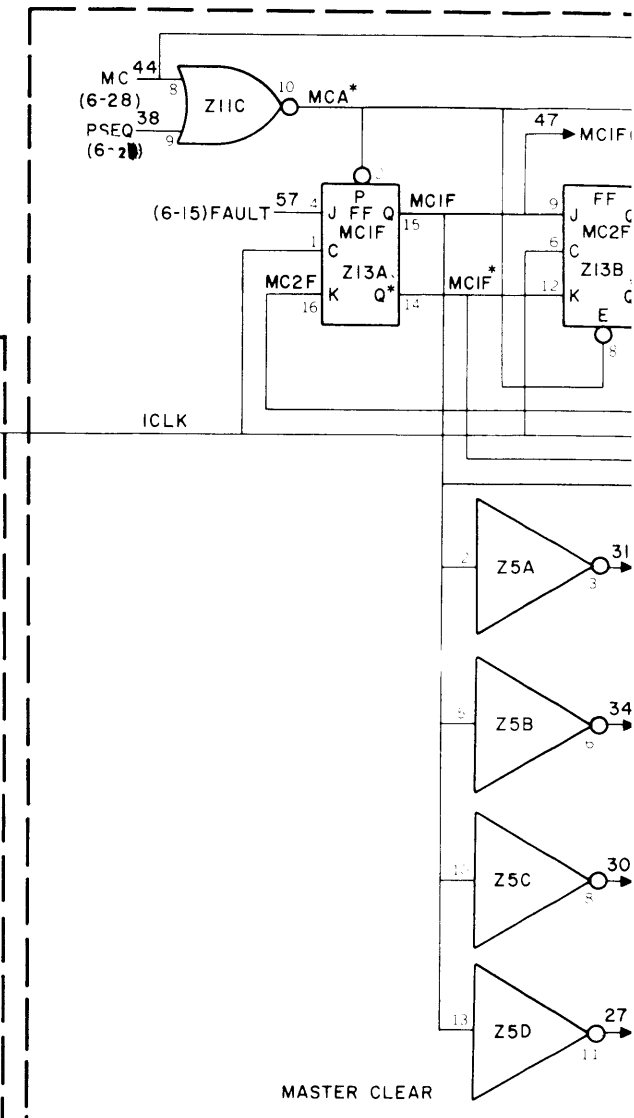
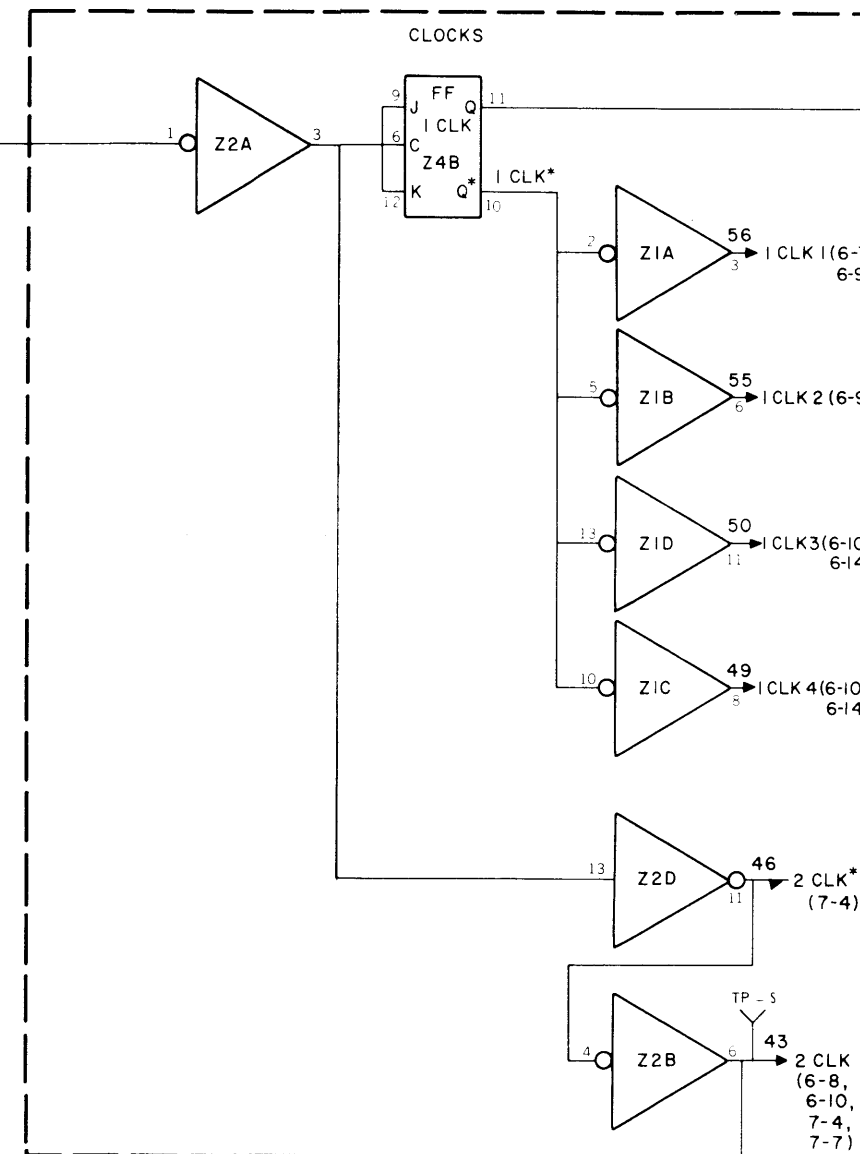
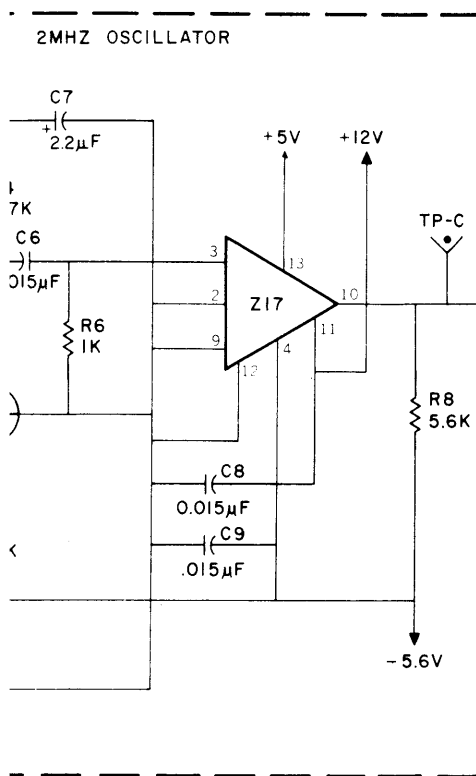


Figure 6-10. Logic Gate IV AG-20 Logic Diagram

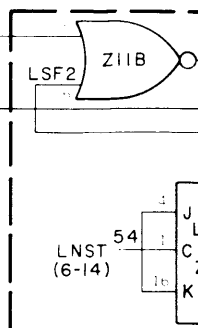
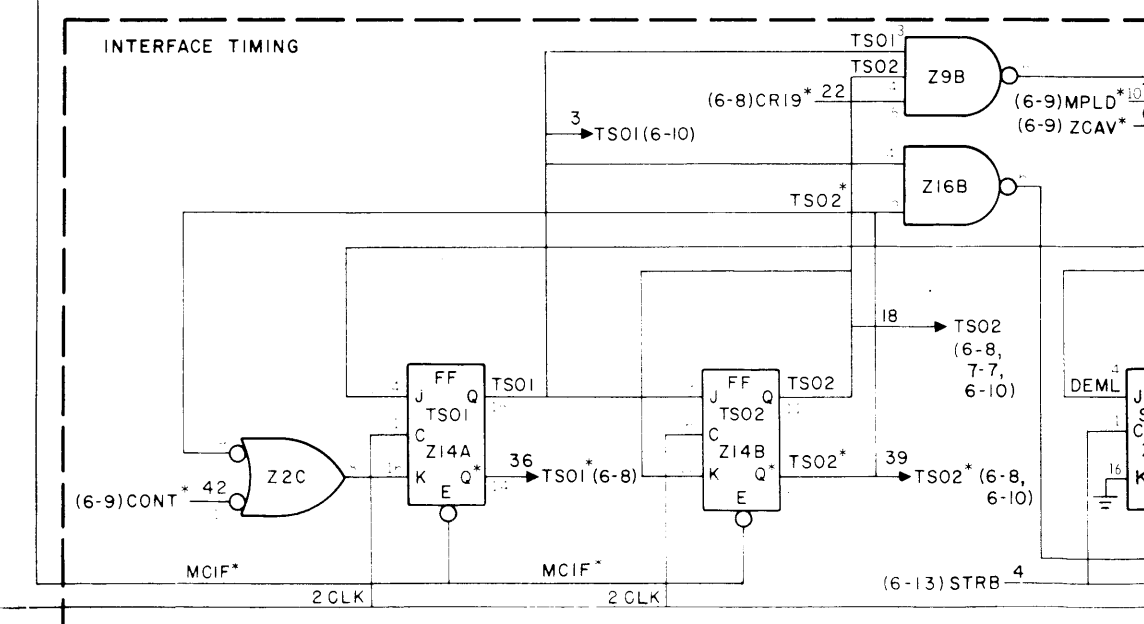
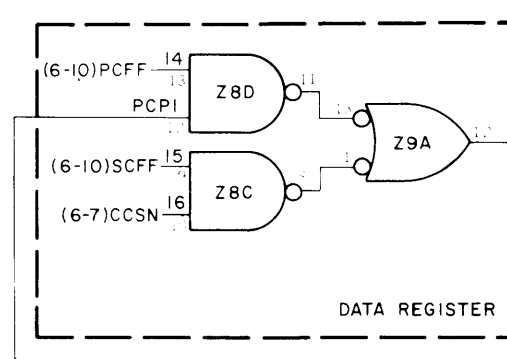
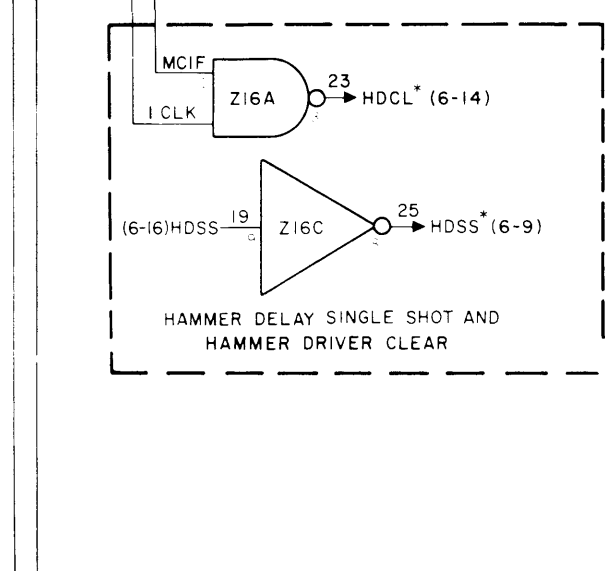
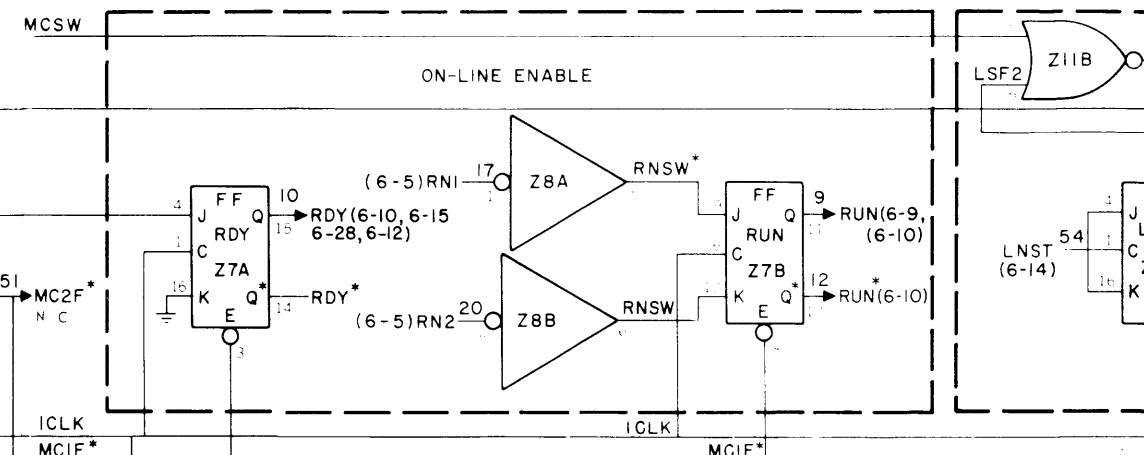
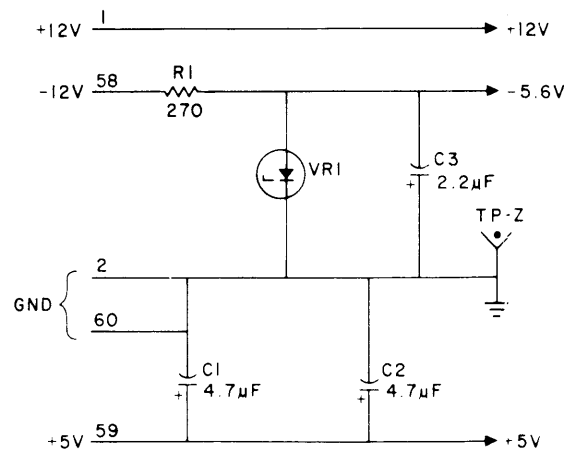
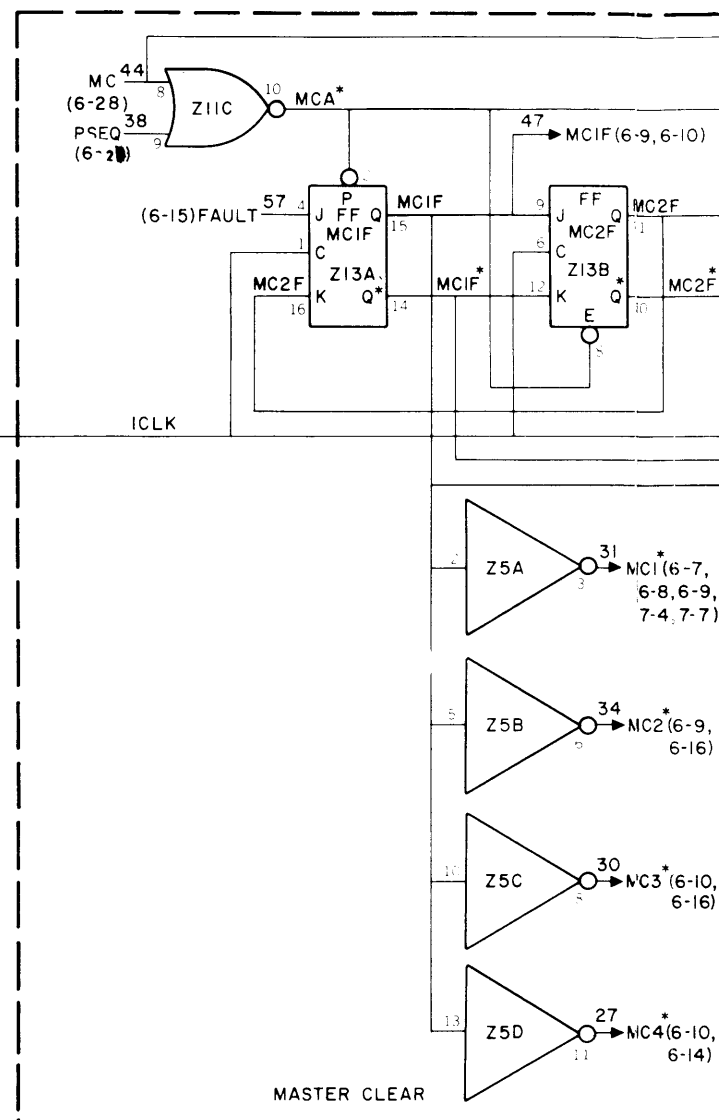
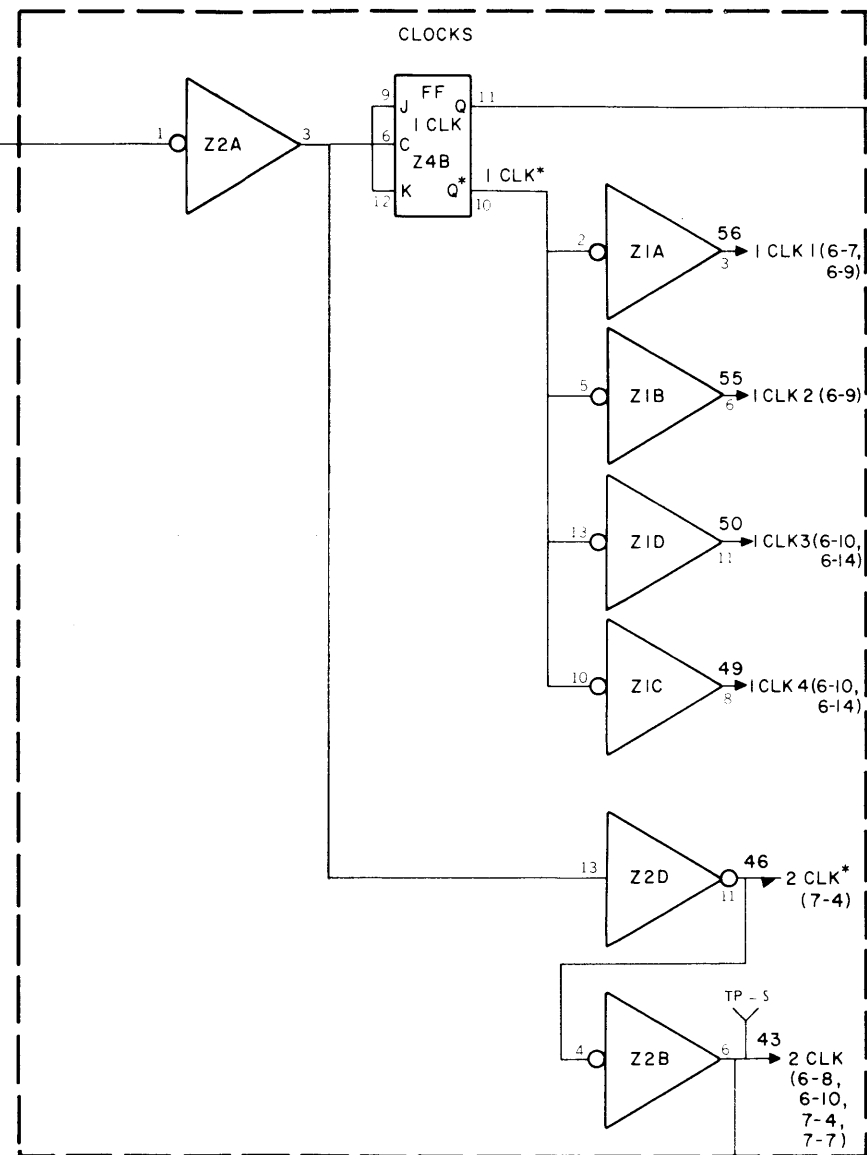


**NOTES:**  
 1. ALL RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED  
 2. REF DPC DWG 212514B





OHMS, UNLESS OTHERWISE SPECIFIED





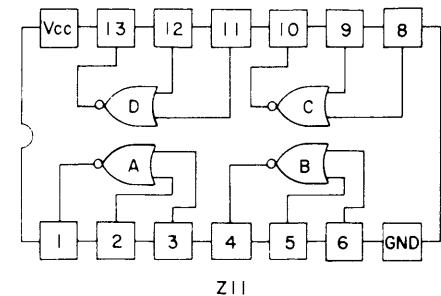
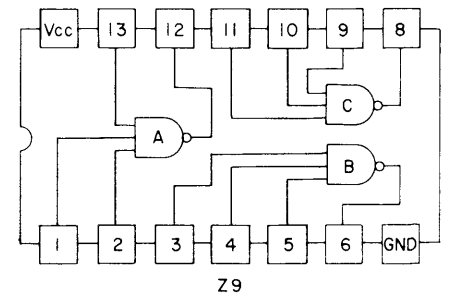
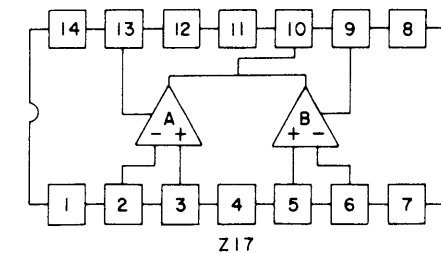
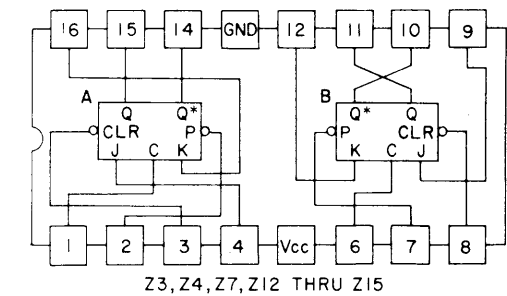
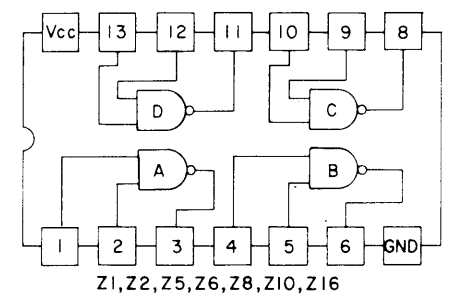
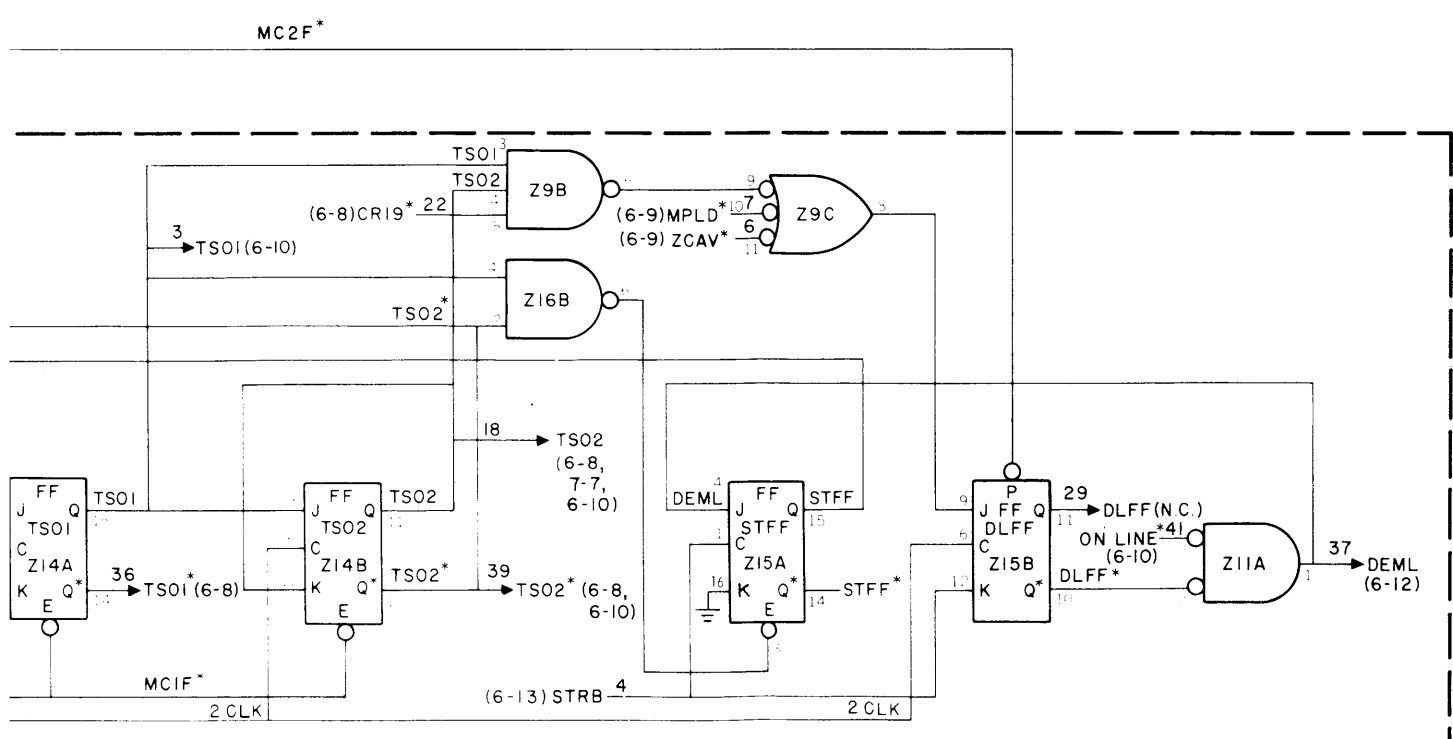
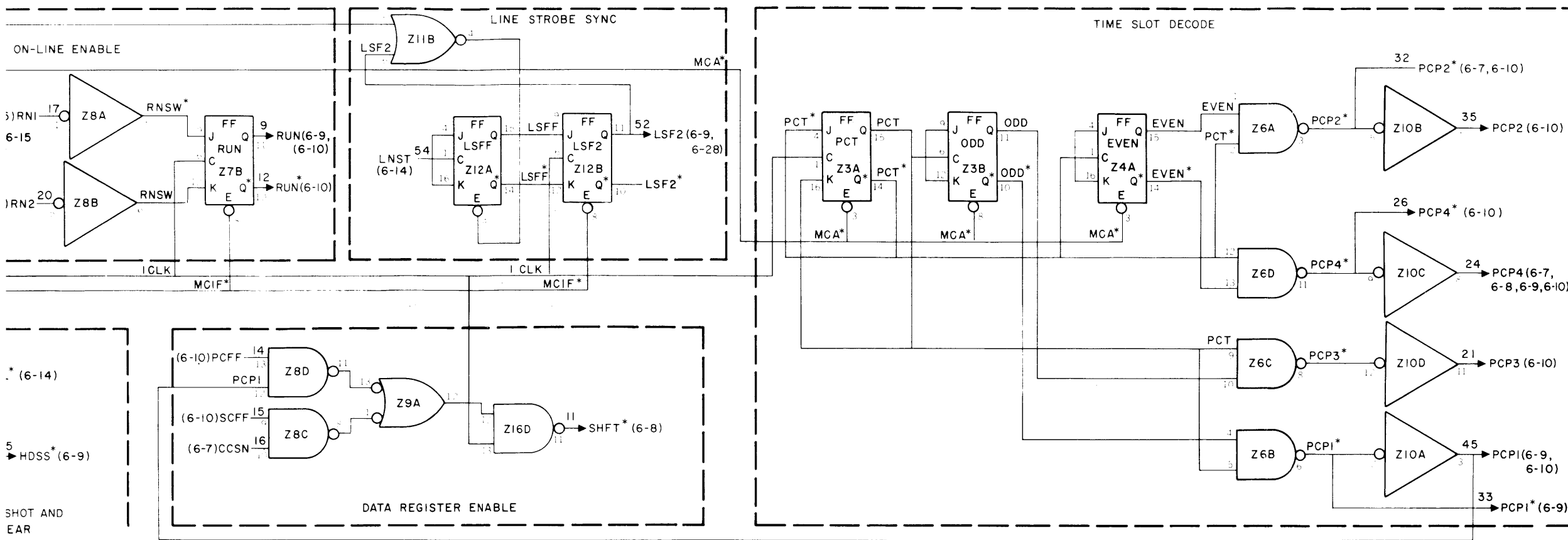


FIGURE 6-11. TIMING CONTROL AT-13, LOGIC DIAGRAM

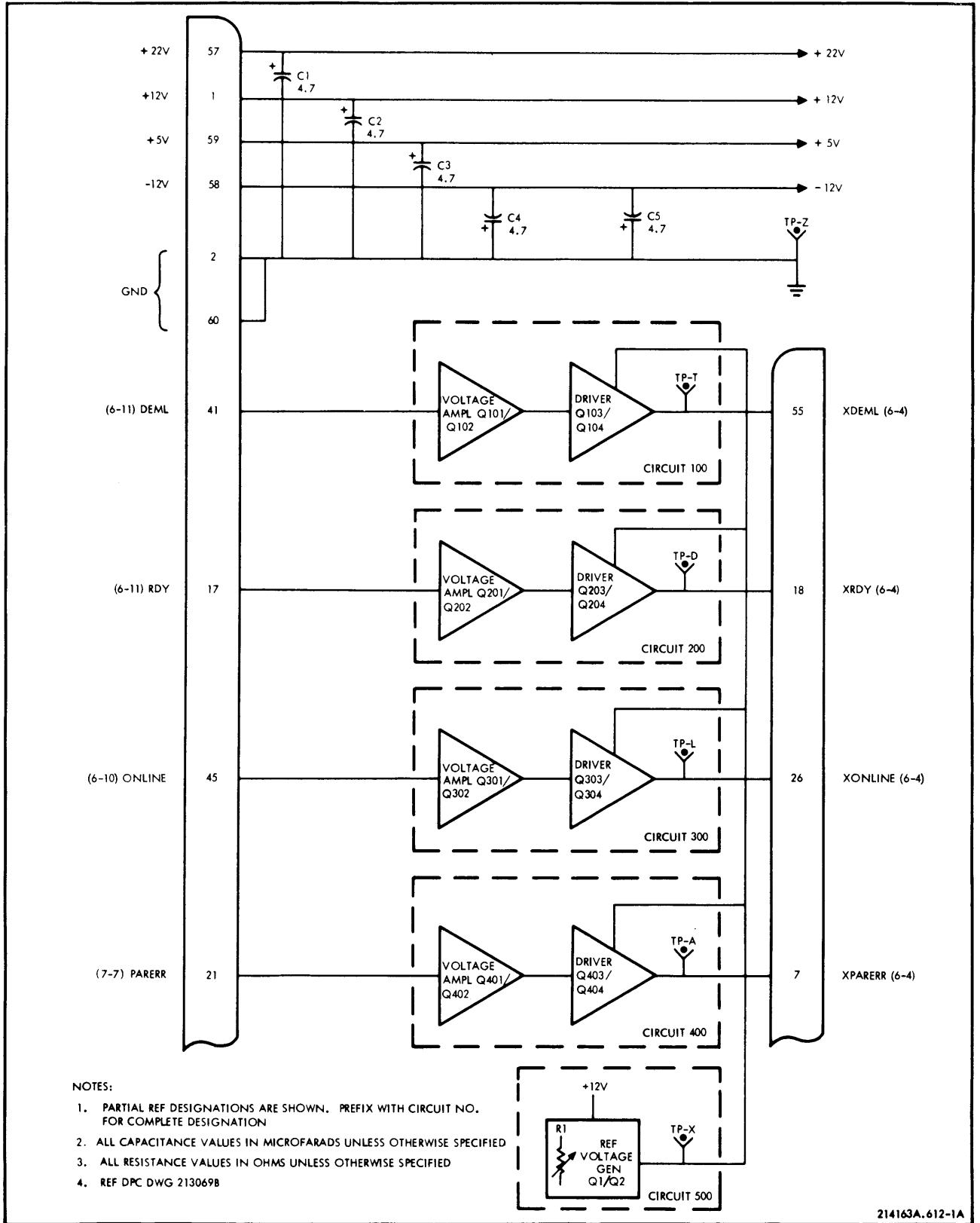
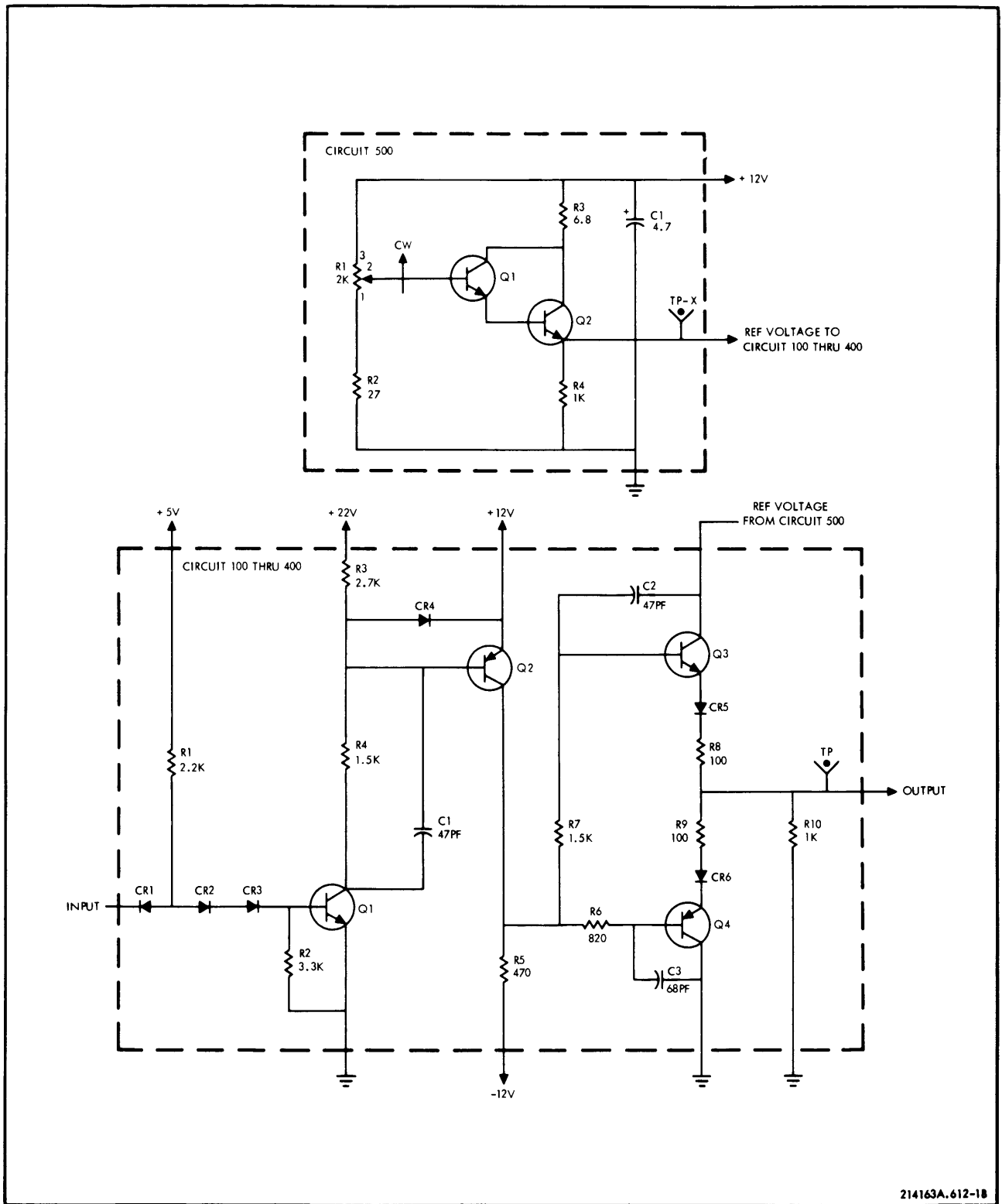
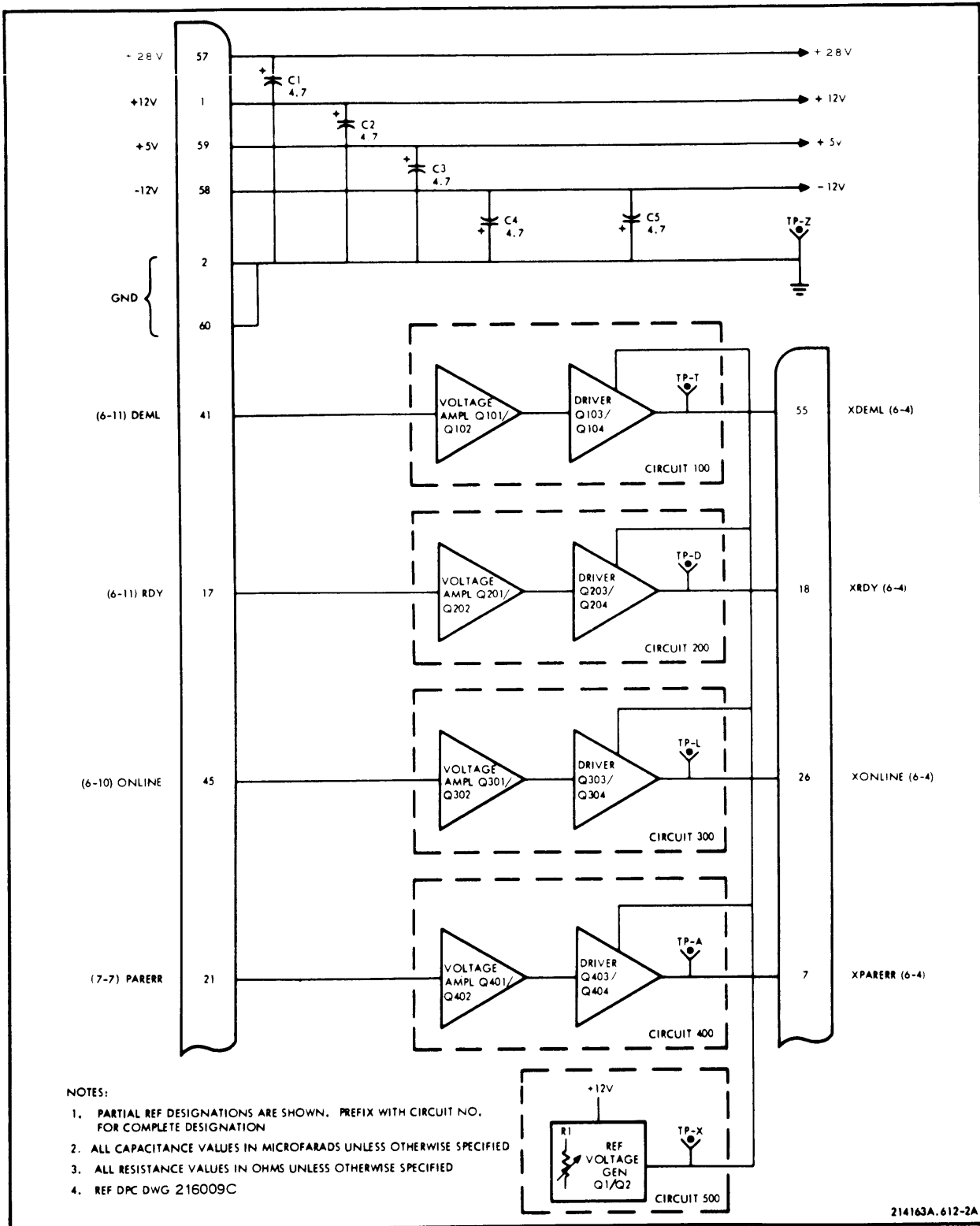


Figure 6-12A. Positive Driver AJ-11 Schematic Diagram (Sheet 1 of 2)



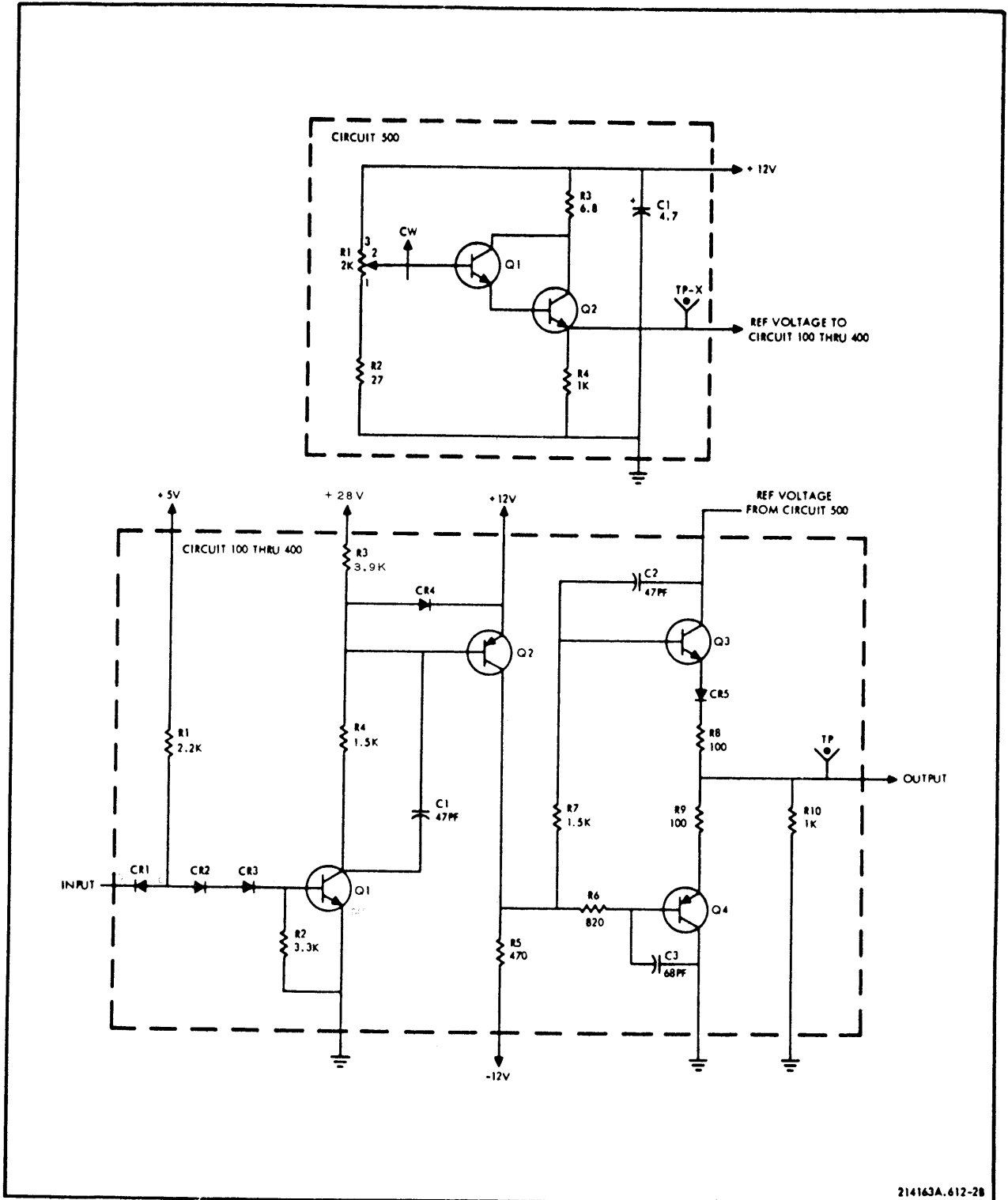
214163A.612-1B

Figure 6-12A. Positive Driver AJ-11 Schematic Diagram (Sheet 2 of 2)



214163A.612-2A

Figure 6-12B. Positive Driver AJ-14 Schematic Diagram (Sheet 1 of 2)



214163A.612-28

Figure 6-12B. Positive Driver AJ-14 Schematic Diagram (Sheet 2 of 2)

DPC 214163B

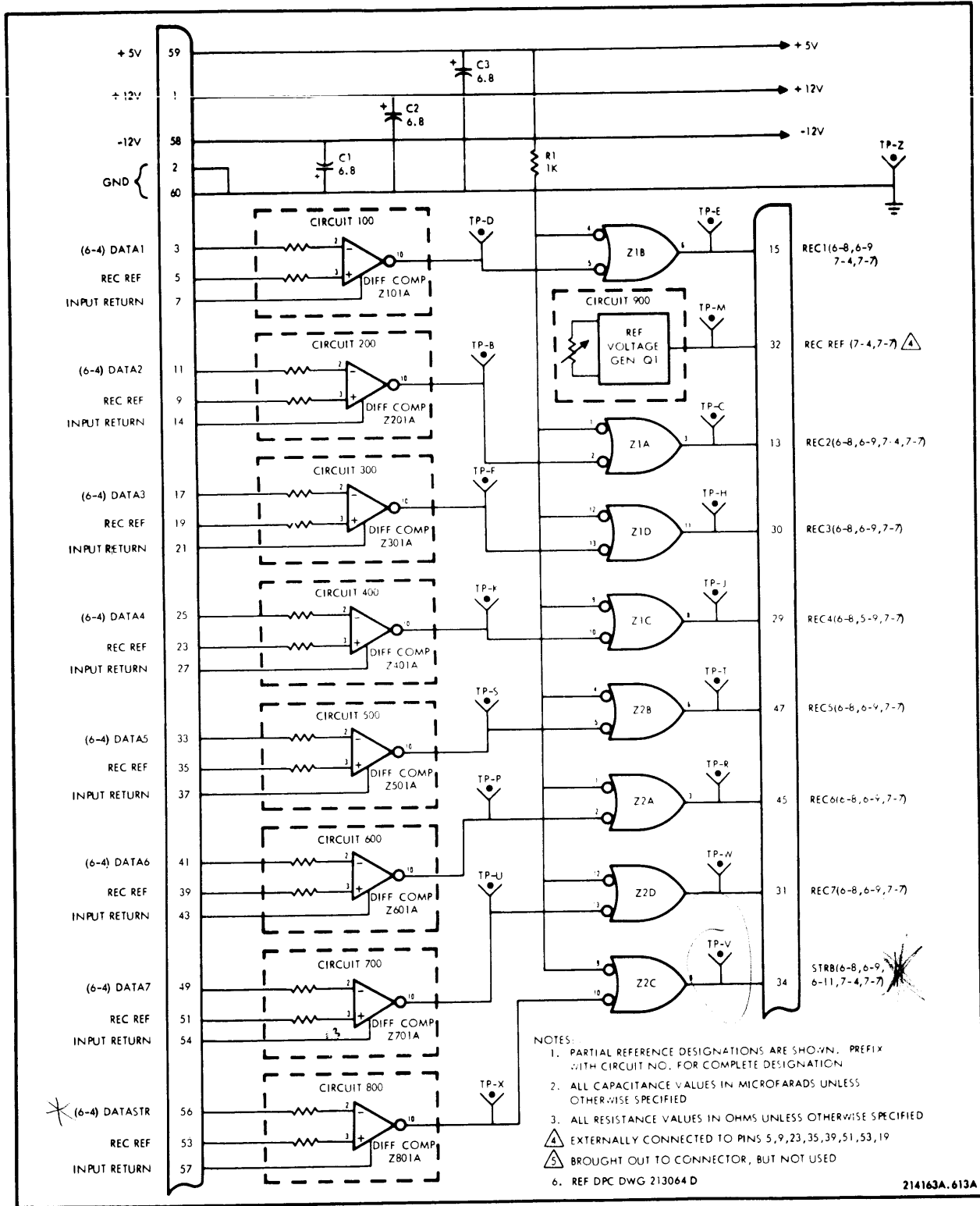


Figure 6-13. Receiver AK-10 Schematic Diagram (Sheet 1 of 2)

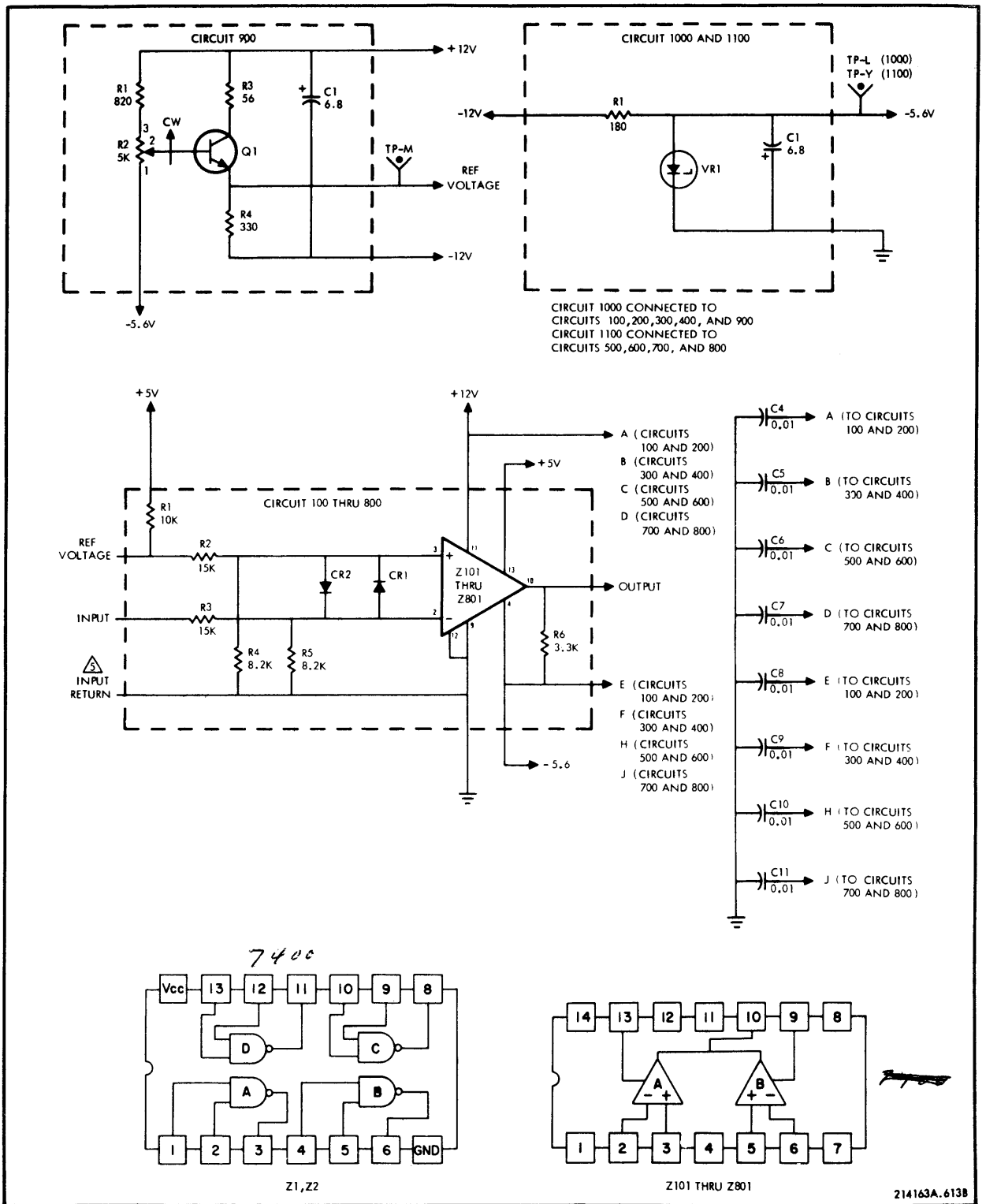
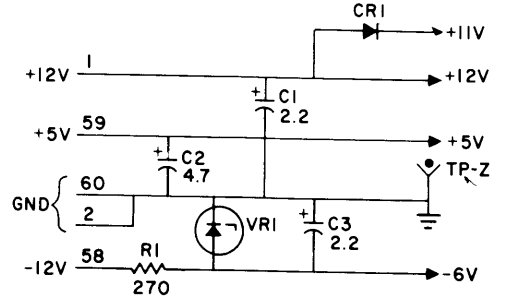
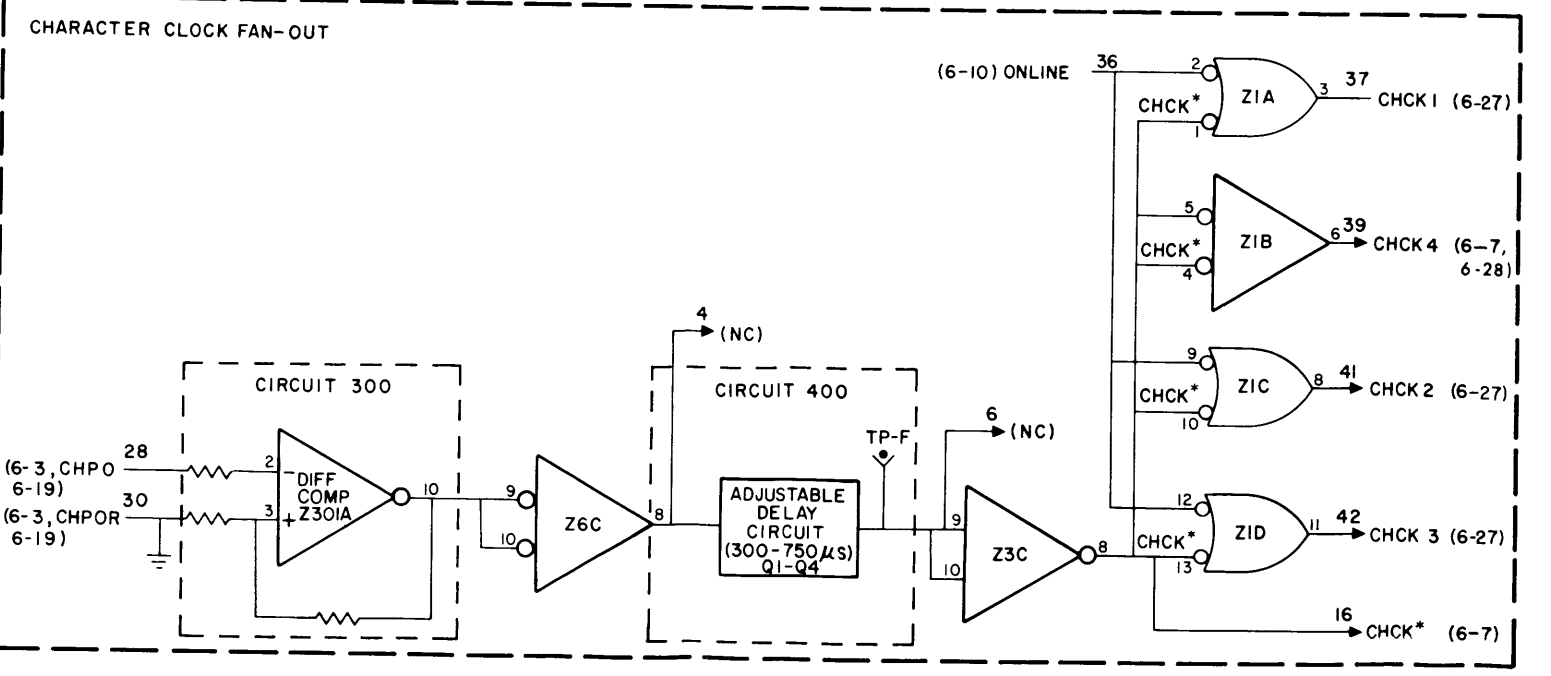
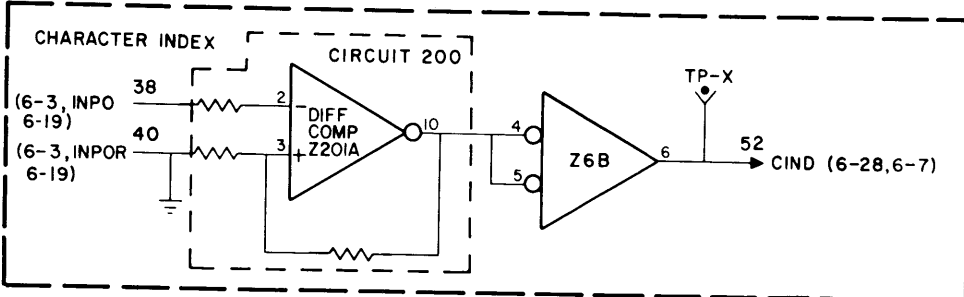
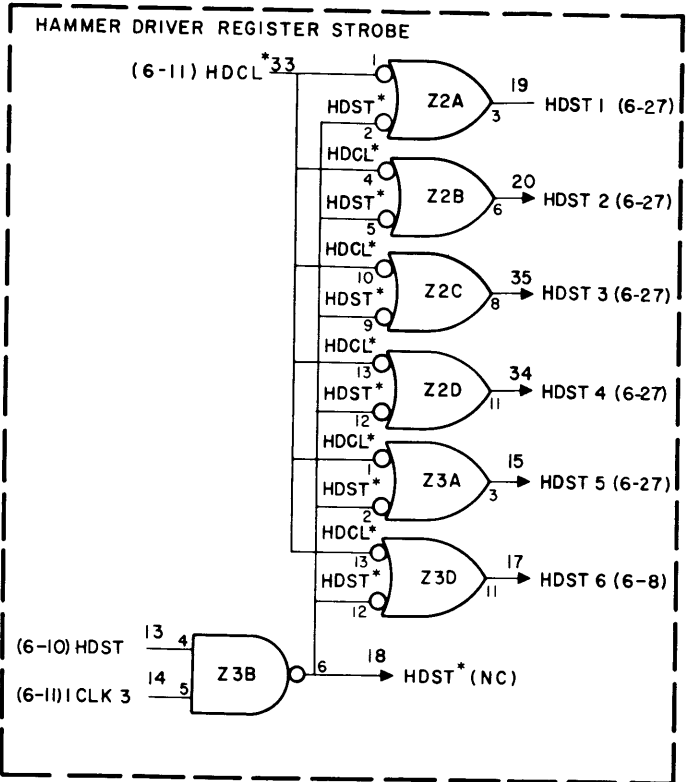
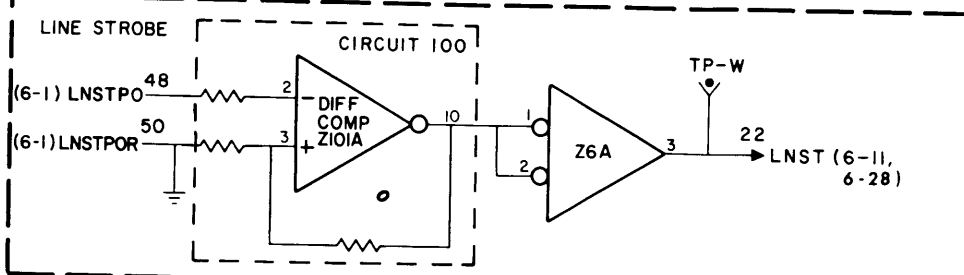
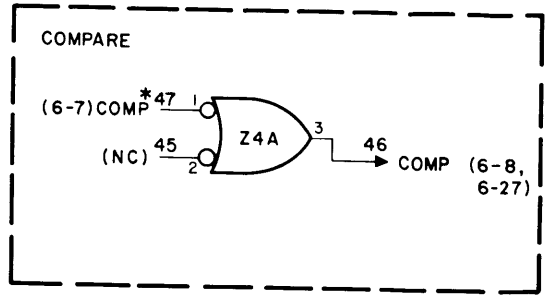
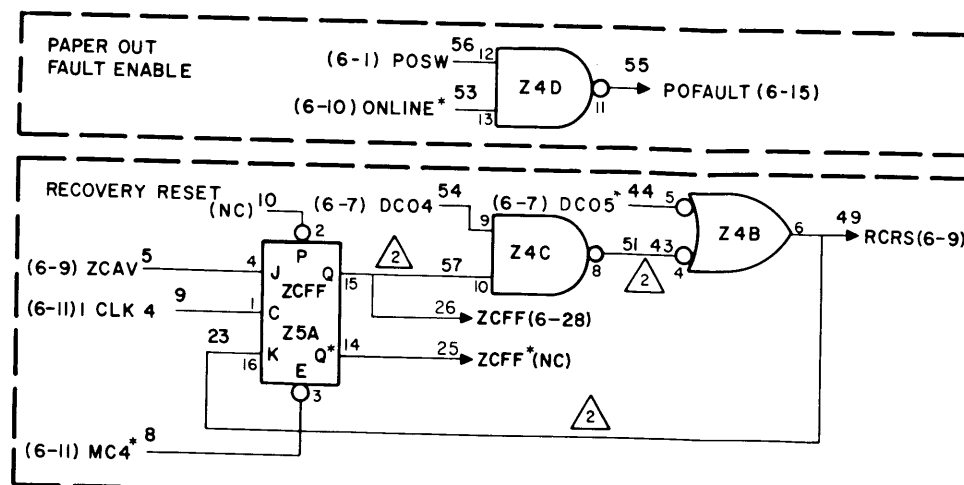
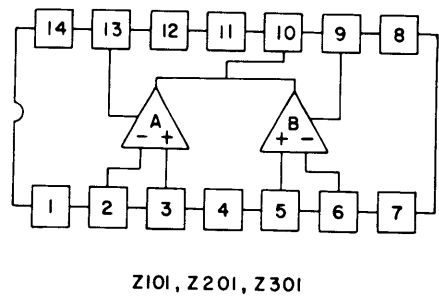
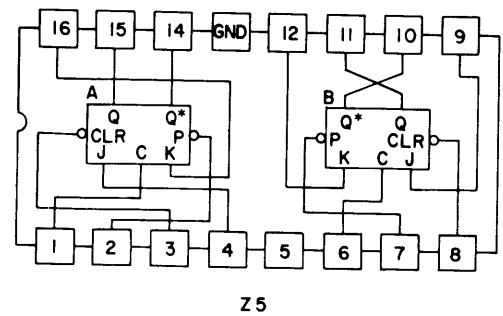
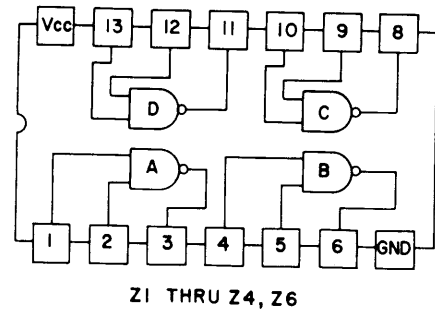


Figure 6-13. Receiver AK-10 Schematic Diagram (Sheet 2 of 2)



- NOTES:
- PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH CIRCUIT NO. FOR COMPLETE DESIGNATION
  - EXTERNAL CONNECTION
  - ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
  - ALL RESISTANCE VALUES IN OHMS UNLESS OTHERWISE SPECIFIED
  - REF. DPC DWG 212479C

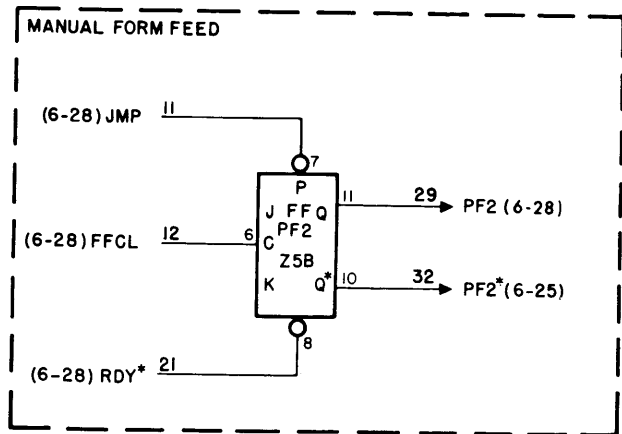


Figure 6-14. Transducer Amplifier AS-13 Logic Diagram (Sheet 1 of 2)



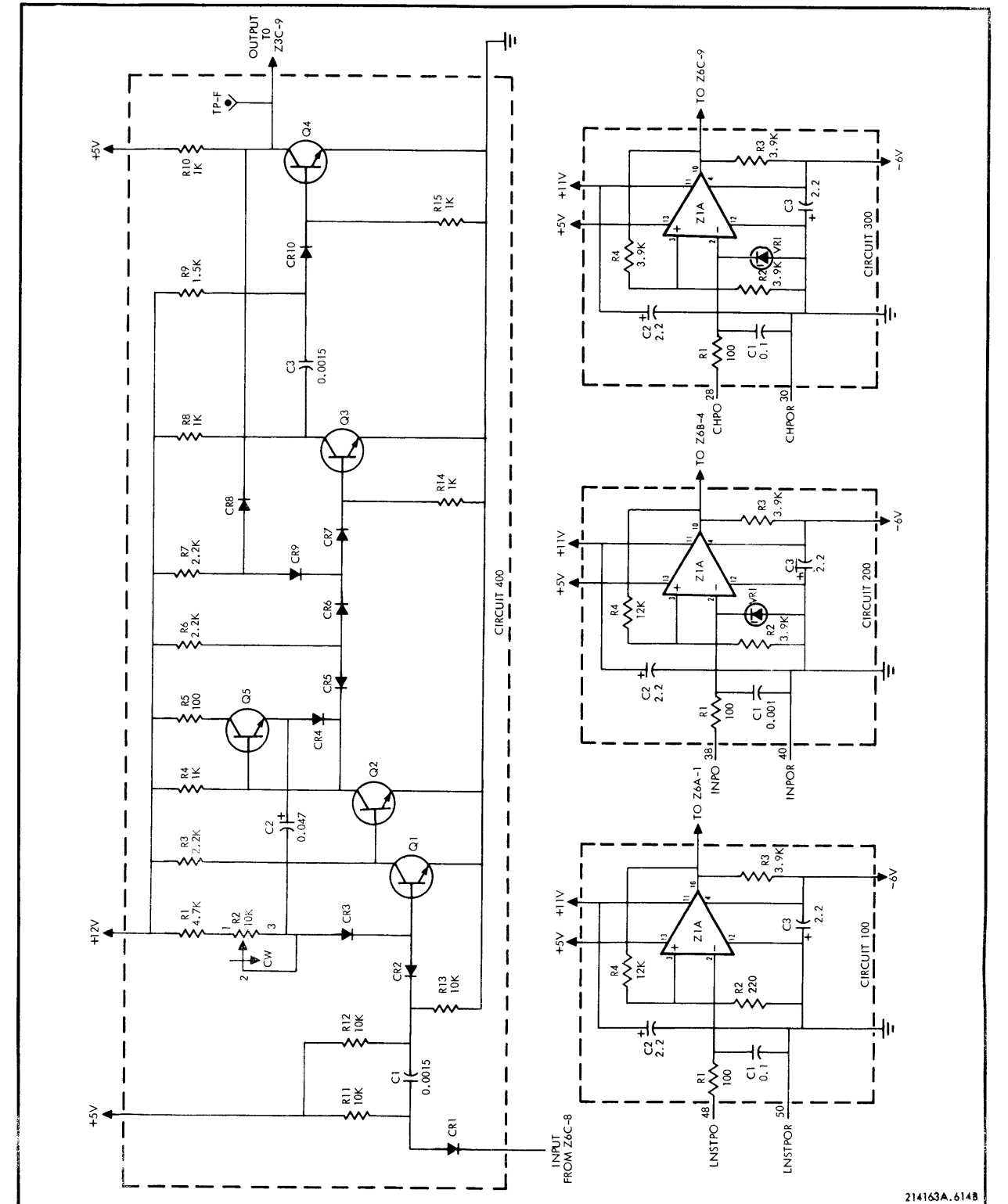
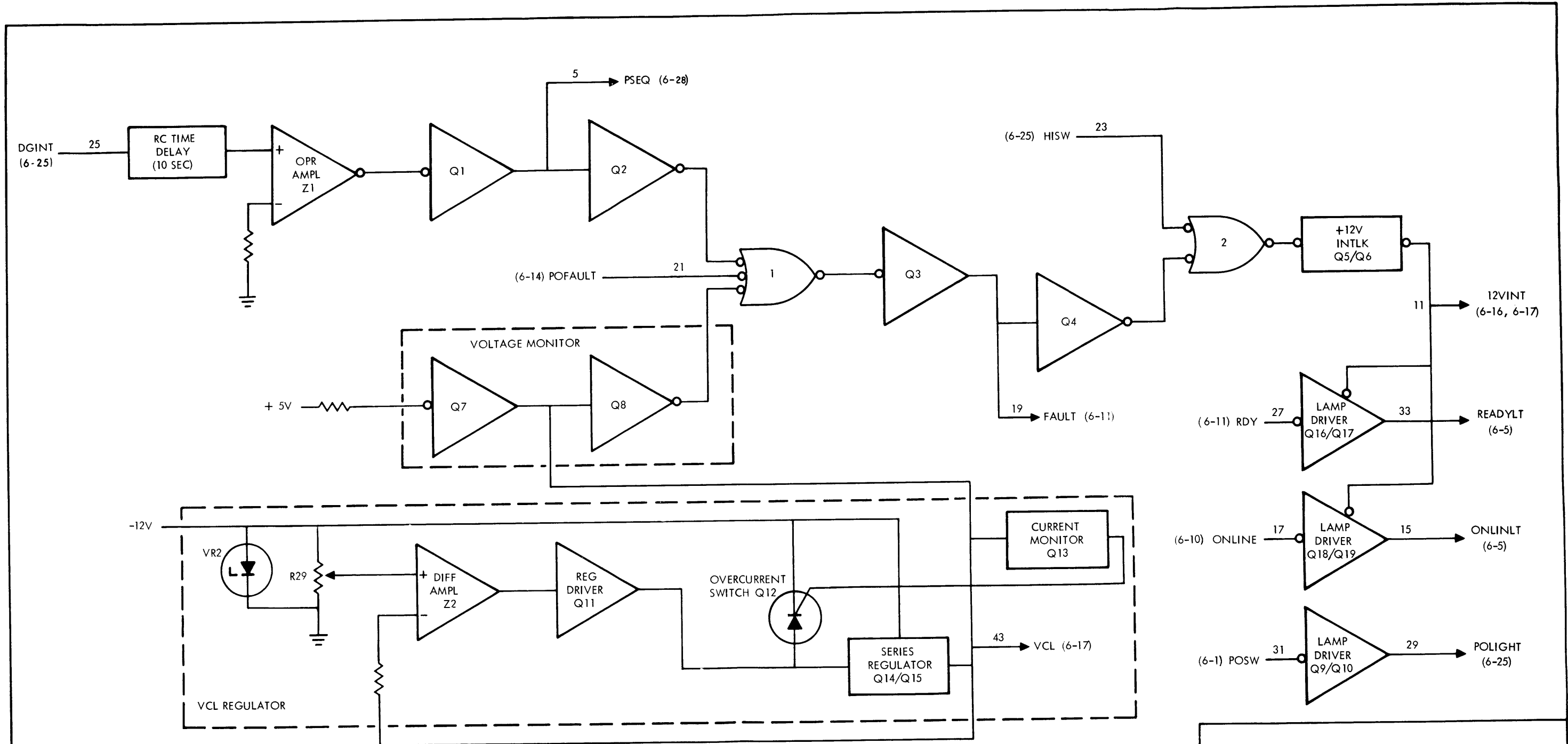


Figure 6-14. Transducer Amplifier AS-13 Logic Diagram (Sheet 2 of 2)



NOTE:  
 1. THE STATE OF THE INTERLOCK AND FAULT SIGNALS IS SHOWN FOR A FAULT CONDITION.  
 2. REFER TO SCHEMATIC (fig 6-21)

Figure 6-15. Hammer Interlock AZ-19 Logic Diagram

DPC 214163B

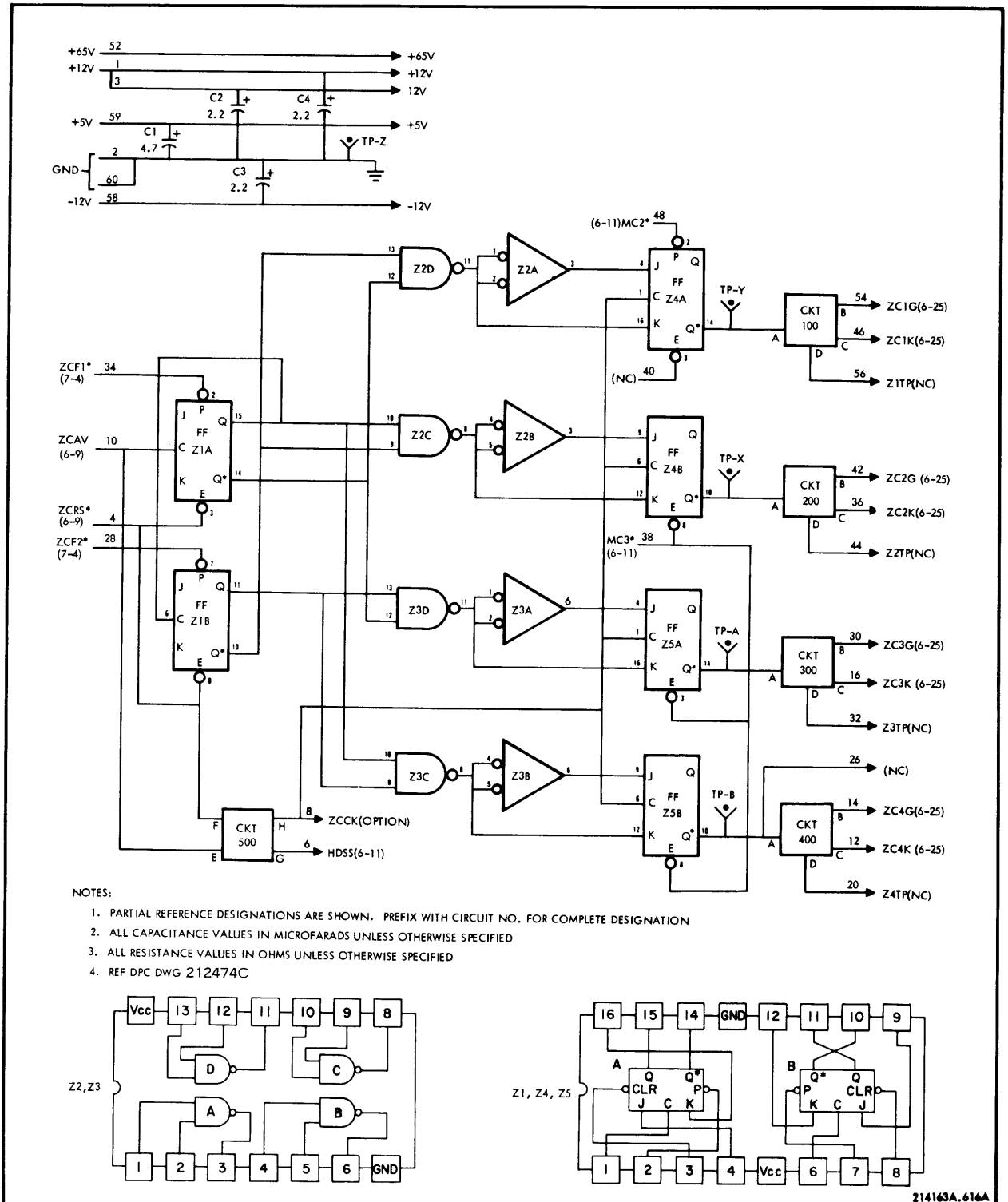
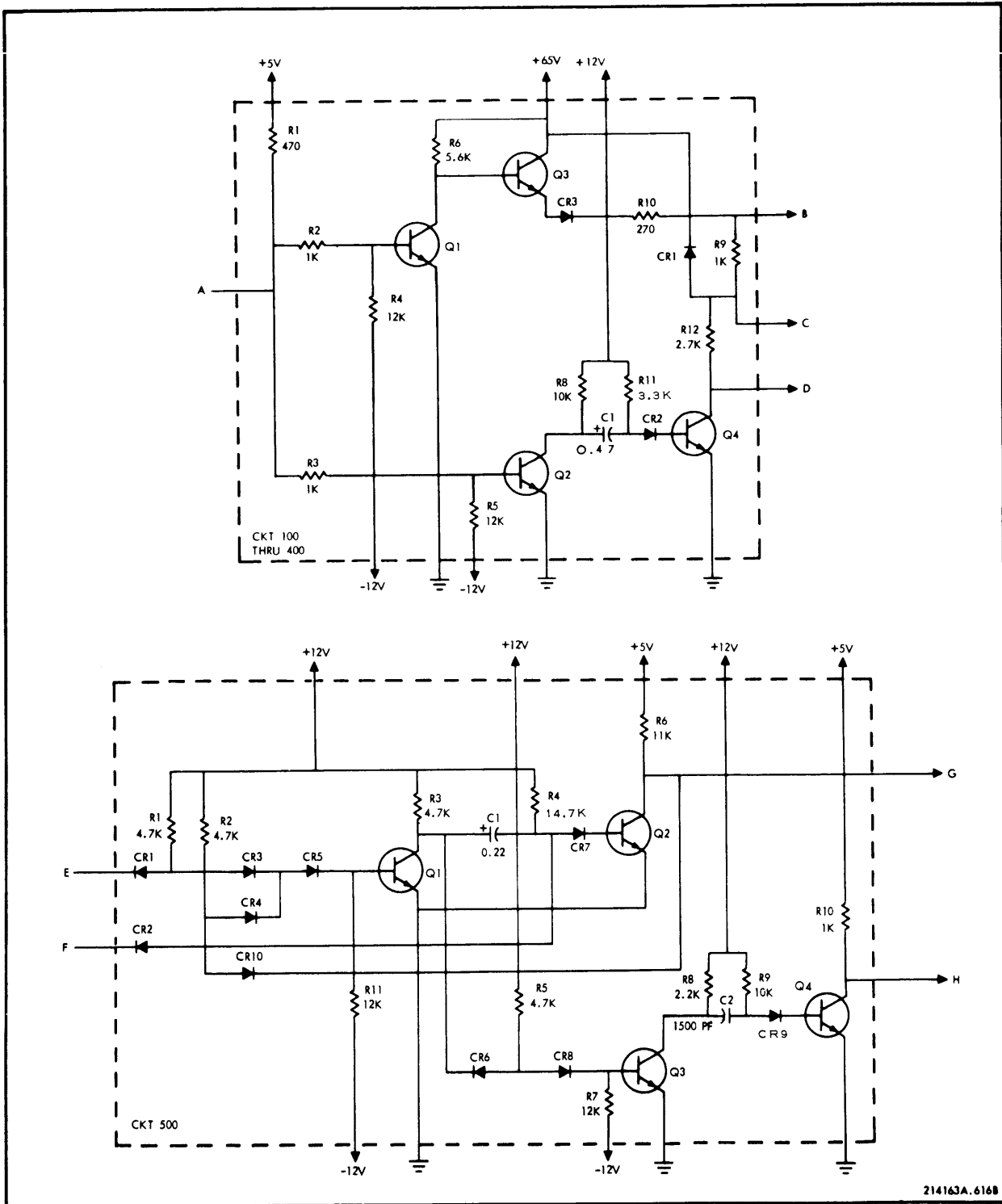


Figure 6-16. Zone Control AZ-18 Logic Diagram (Sheet 1 of 2)

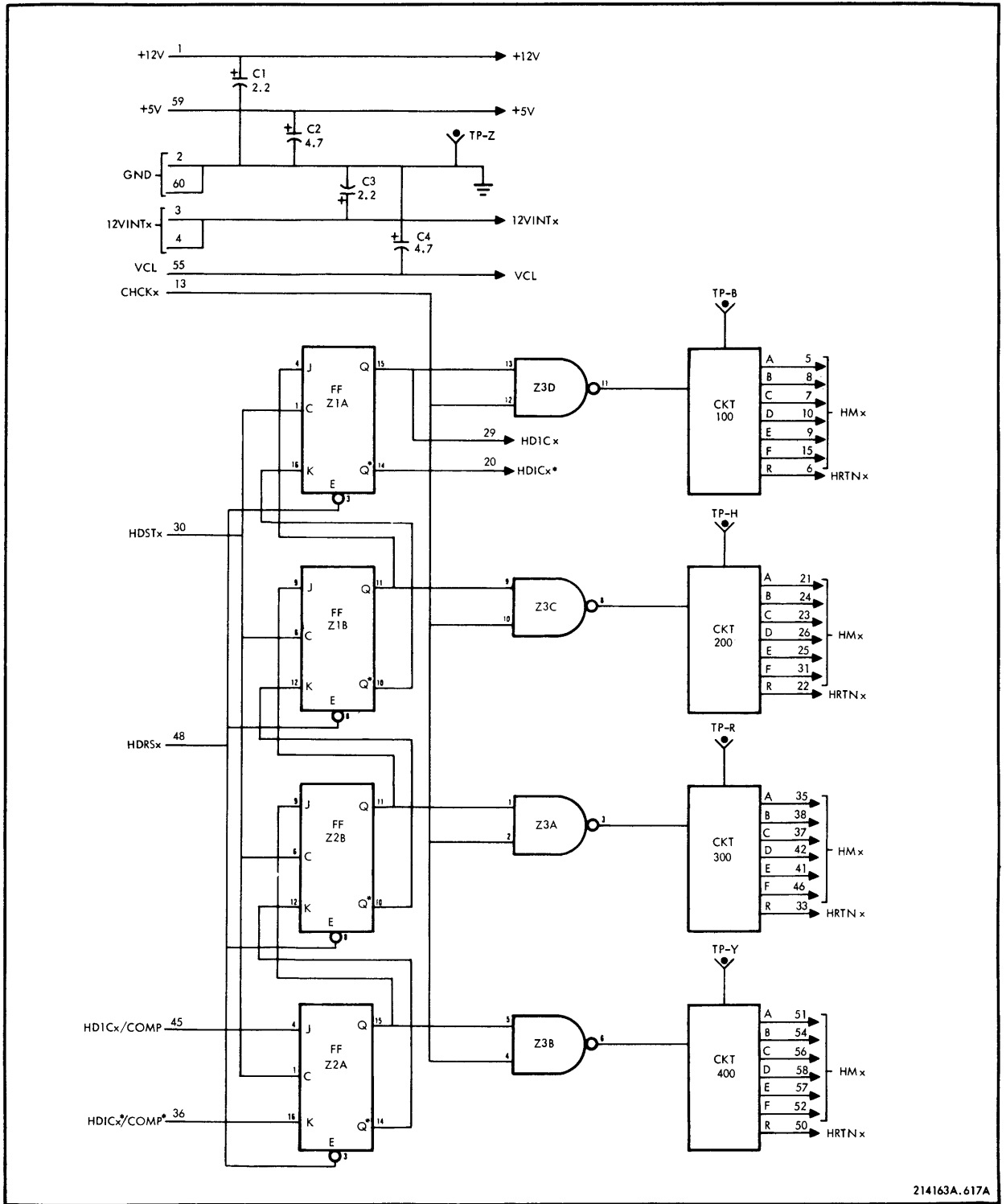
DPC 214163B



214163A.6168

Figure 6-16. Zone Control AZ-18 Logic Diagram (Sheet 2 of 2)

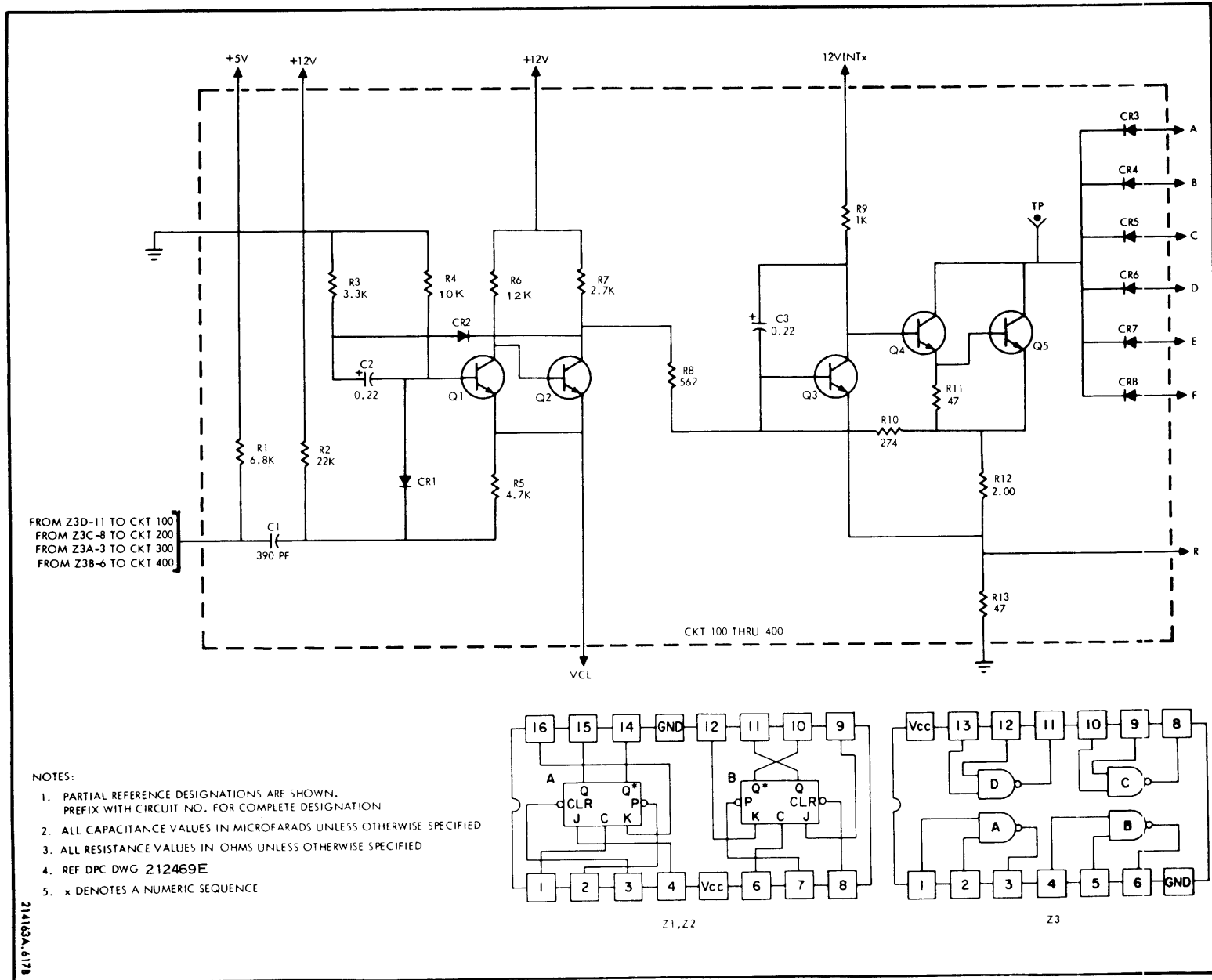
DPC 214163

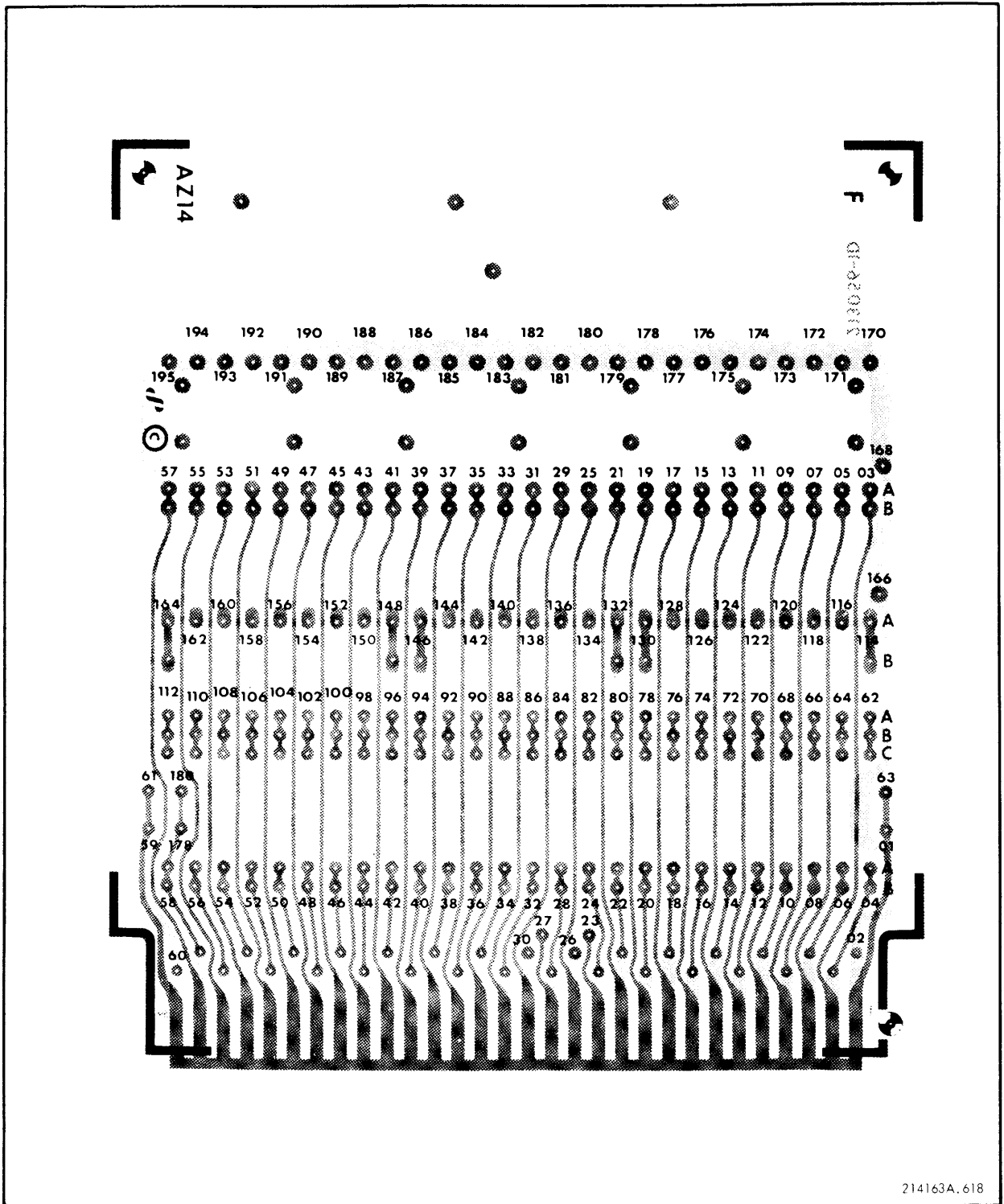


214163A.617A

Figure 6-17. Hammer Driver AH-10 Logic Diagram (Sheet 1 of 2)

Figure 6-17. Hammer Driver AH-10 Logic Diagram (Sheet 2 of 2)





214163A, 618

Figure 6-18. Cable Plug Card AZ-14 Schematic Diagram

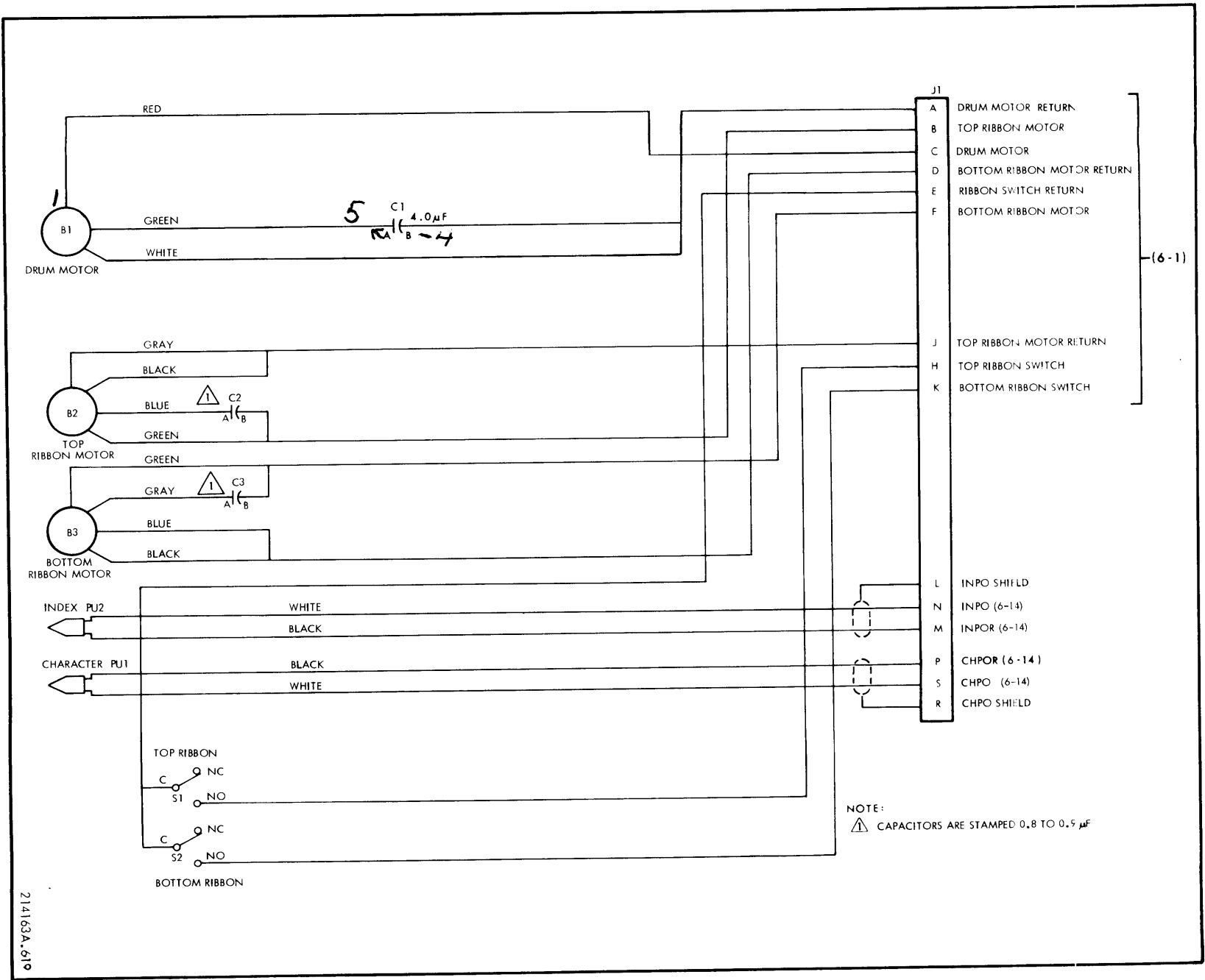


Figure 6-19. Drum Gate A2A1 Schematic Diagram (Printer Serial Number 129 and up)



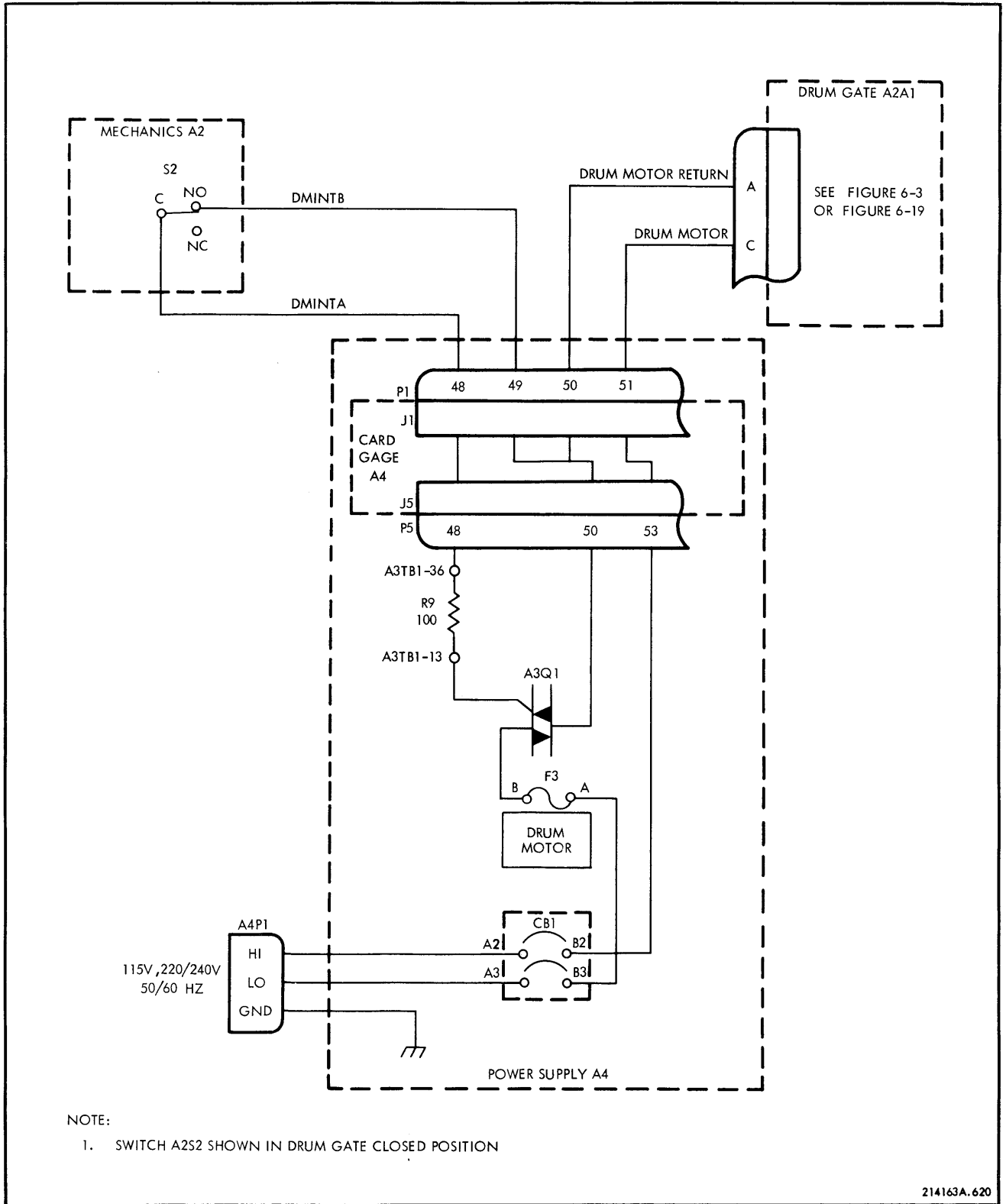
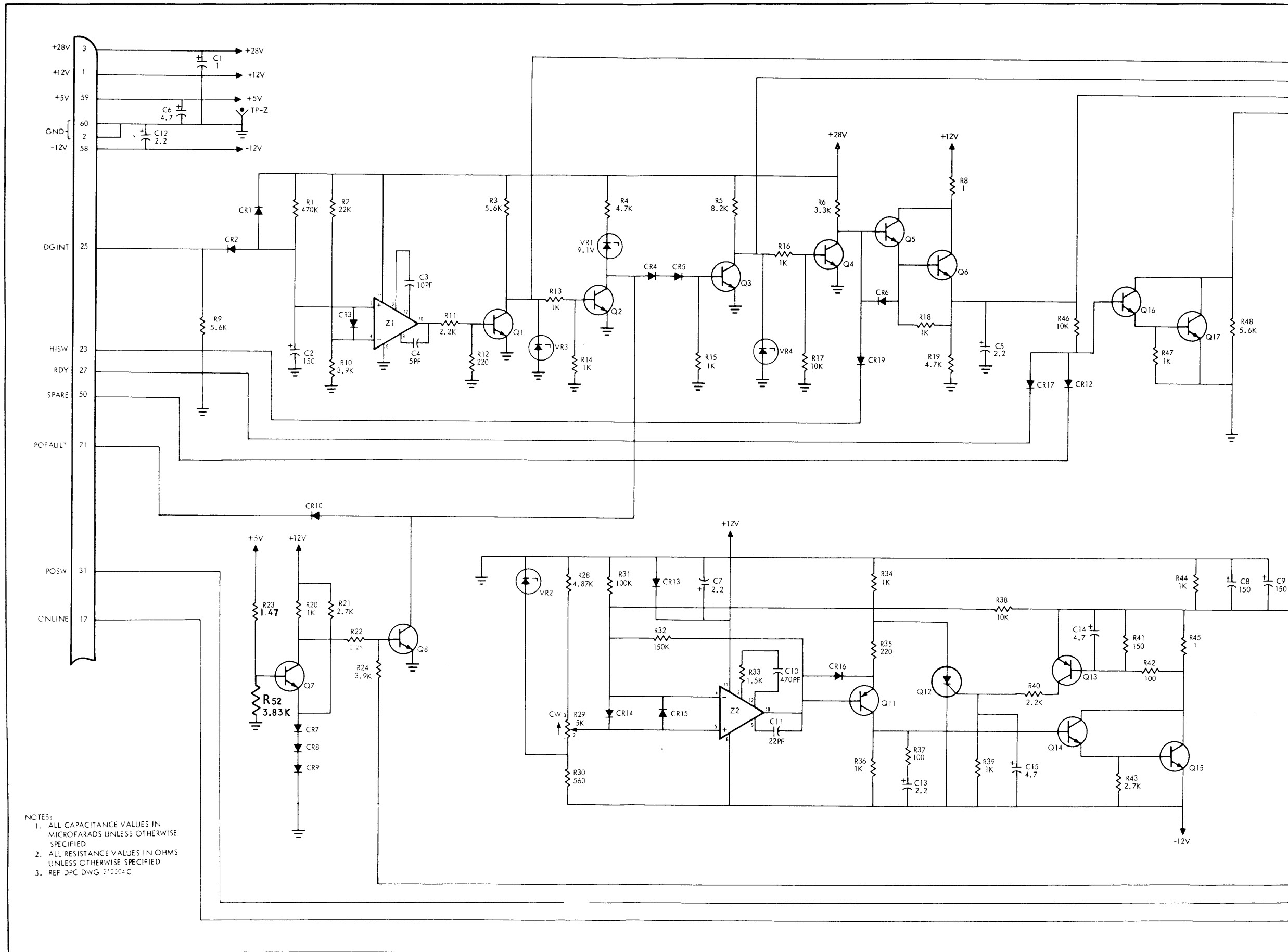


Figure 6-20. Drum Motor Interlock Schematic Diagram



- NOTES:
1. ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
  2. ALL RESISTANCE VALUES IN OHMS UNLESS OTHERWISE SPECIFIED
  3. REF DPC DWG 212504 C

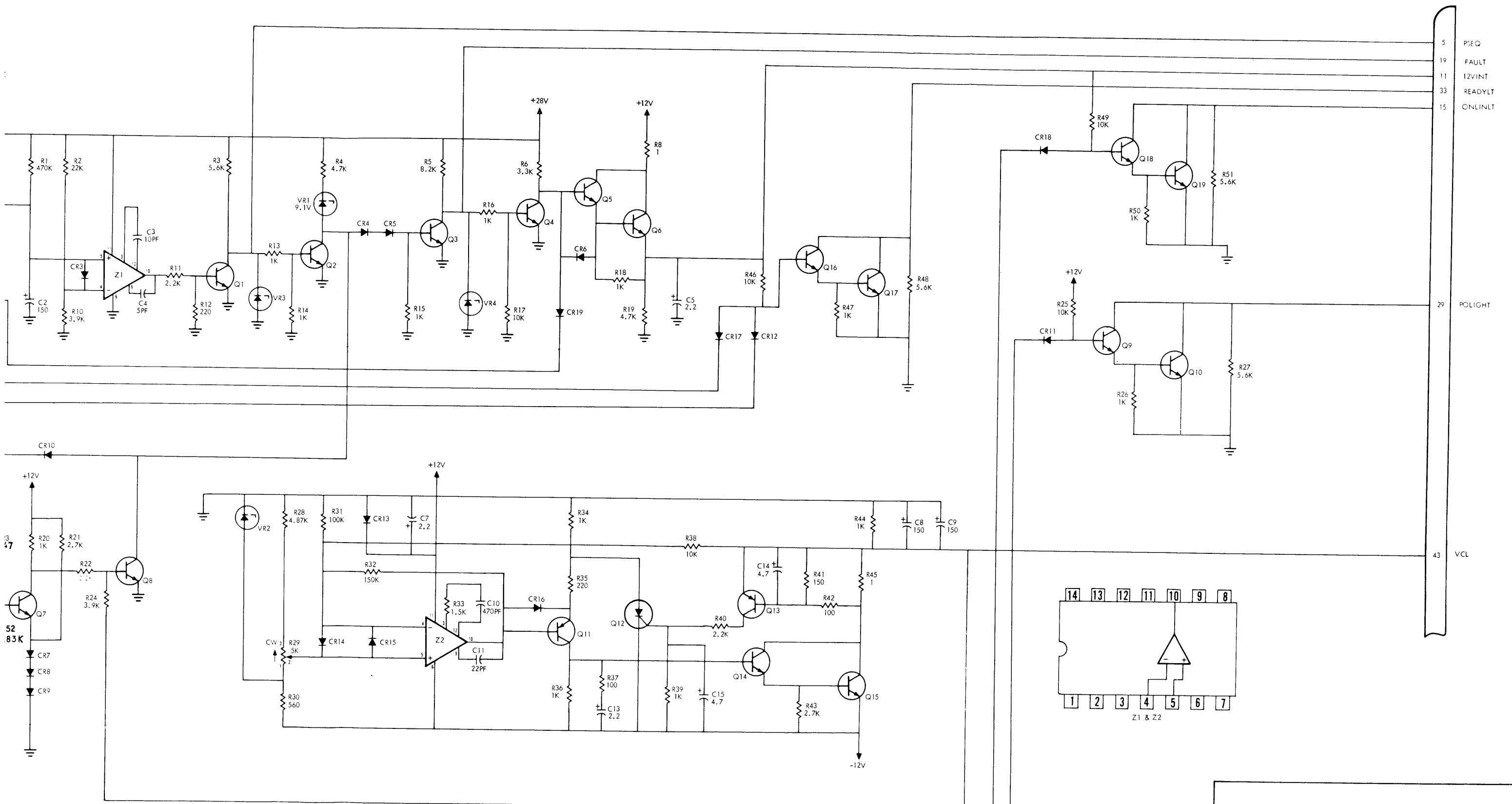
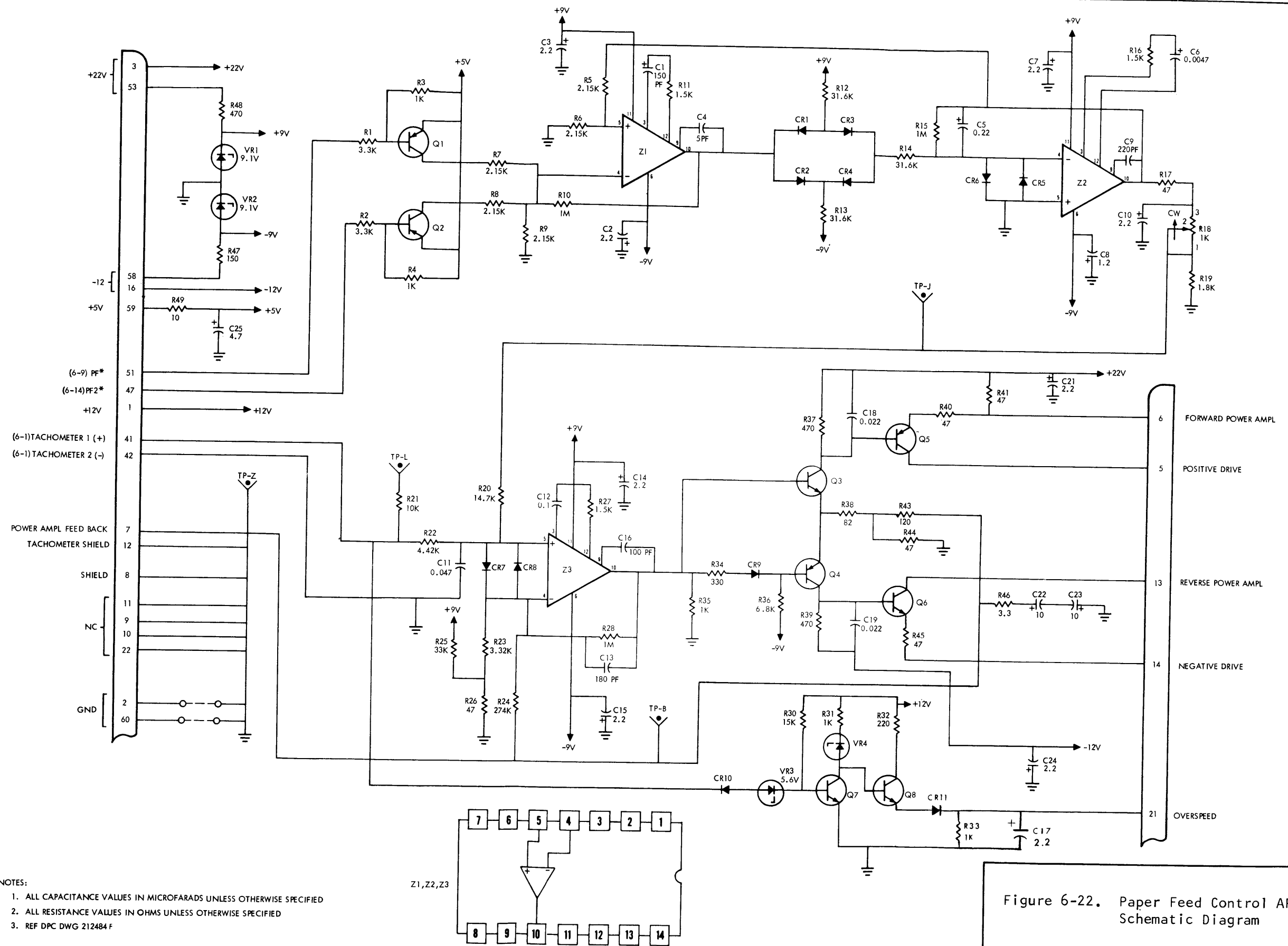
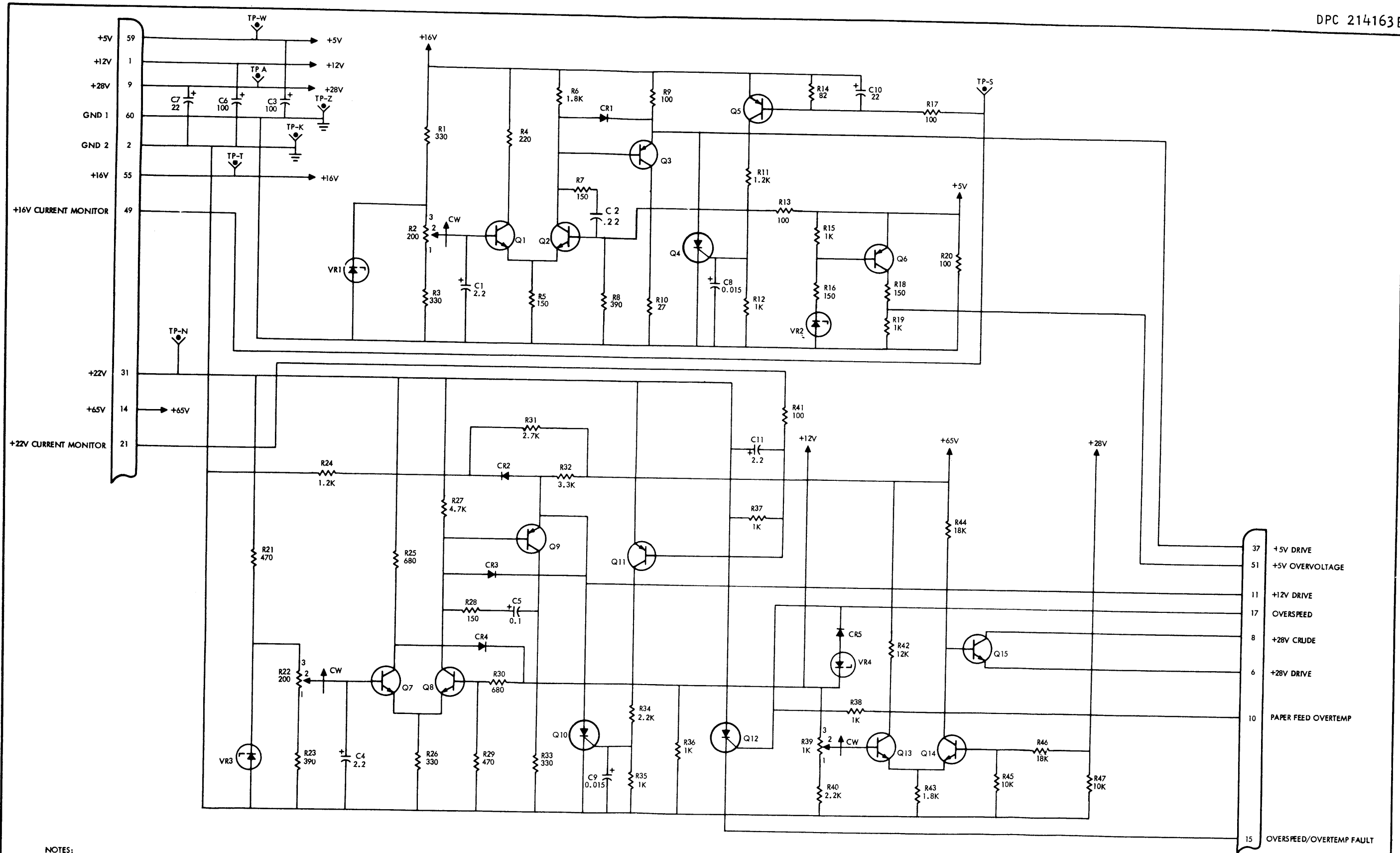


Figure 6-21. Hammer Interlock AZ-19 Schematic Diagram



- NOTES:
1. ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
  2. ALL RESISTANCE VALUES IN OHMS UNLESS OTHERWISE SPECIFIED
  3. REF DPC DWG 212484 F

Figure 6-22. Paper Feed Control AP-10 Schematic Diagram



NOTES:

1. ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. ALL RESISTANCE VALUES IN OHMS UNLESS OTHERWISE SPECIFIED
3. REF DPC DWG 212499 F

Figure 6-23. Voltage Regulator AV-10 Schematic Diagram

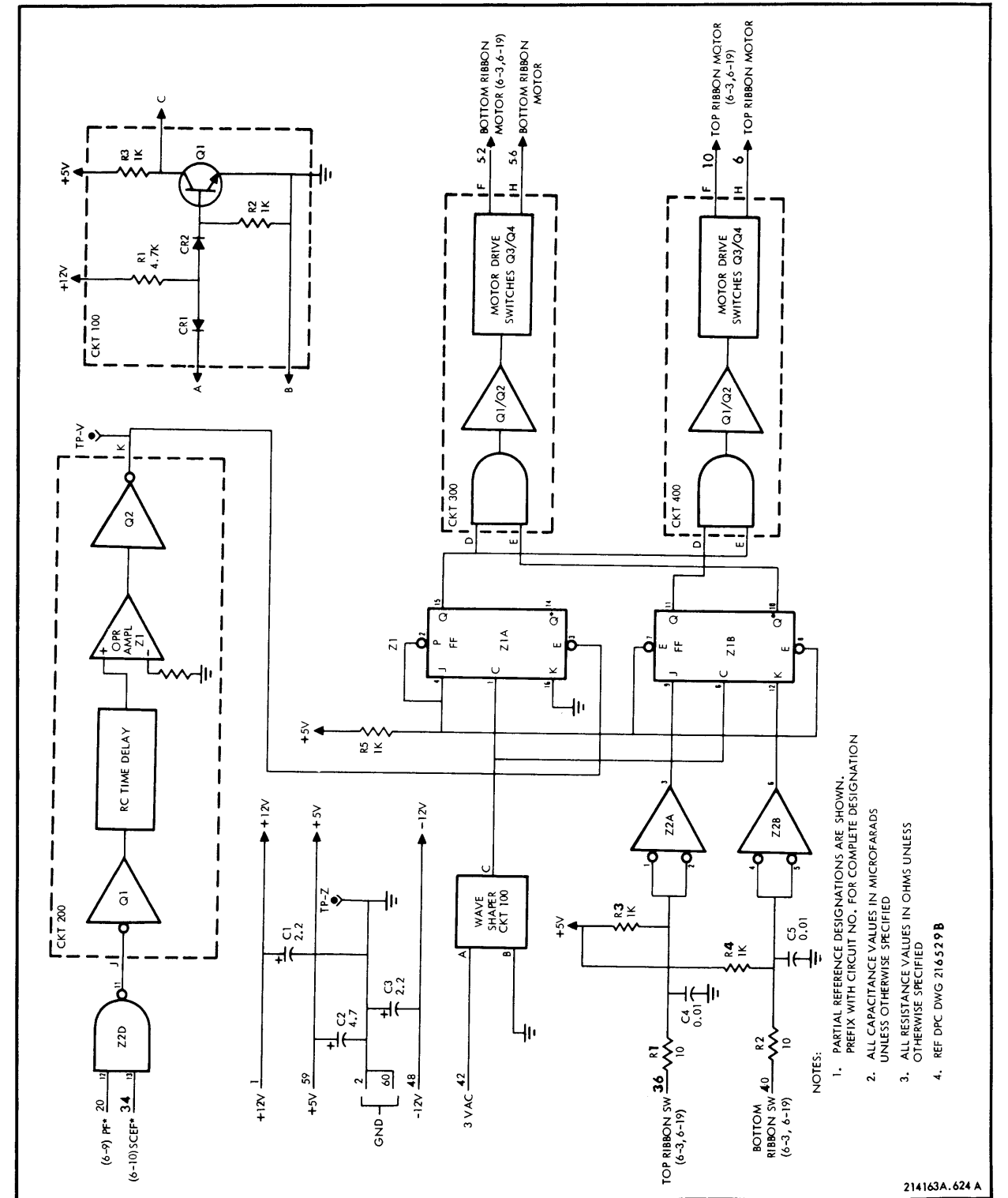


Figure 6-24. Ribbon Control AZ-84 Logic Diagram (Sheet 1 of 2)

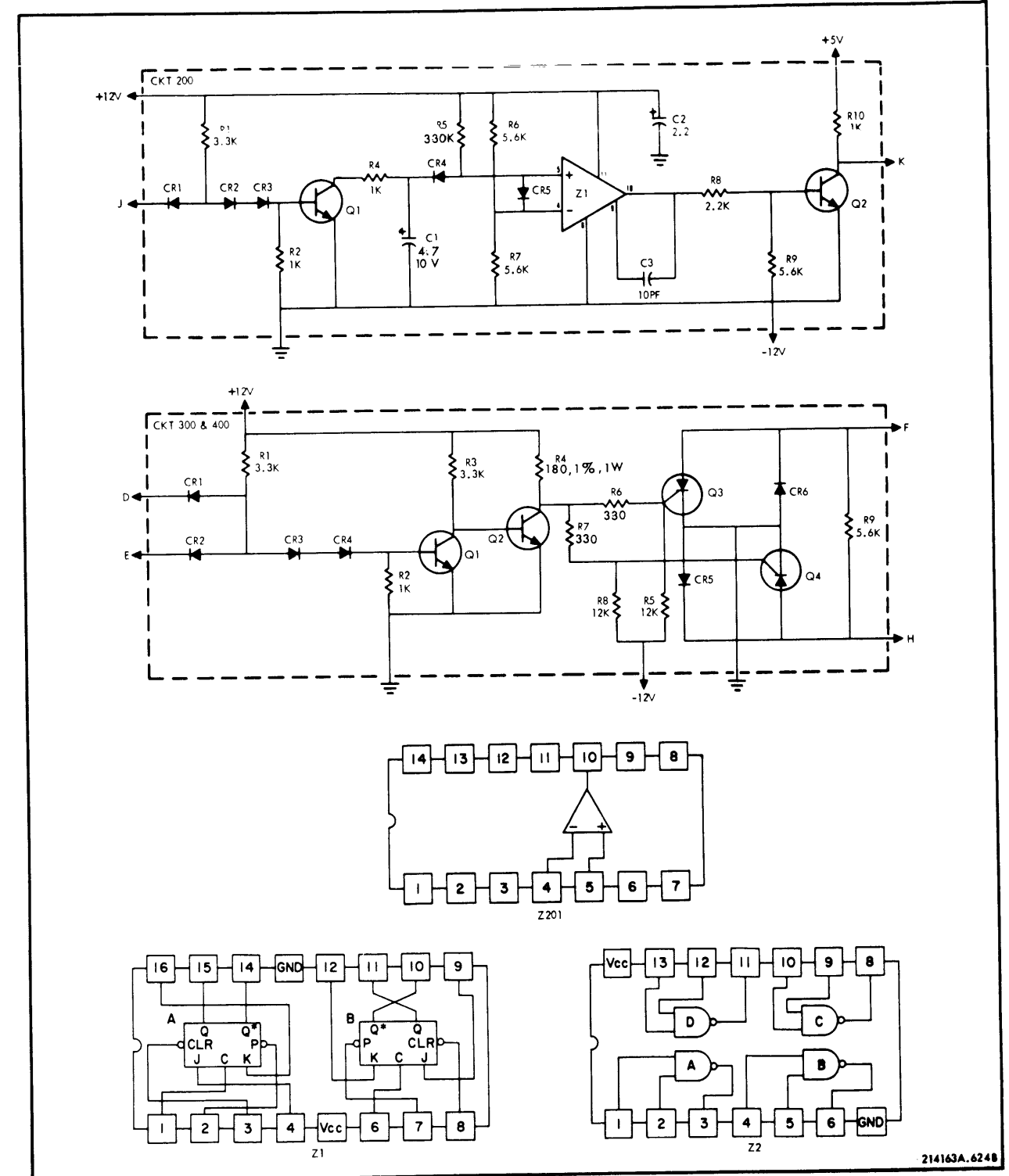
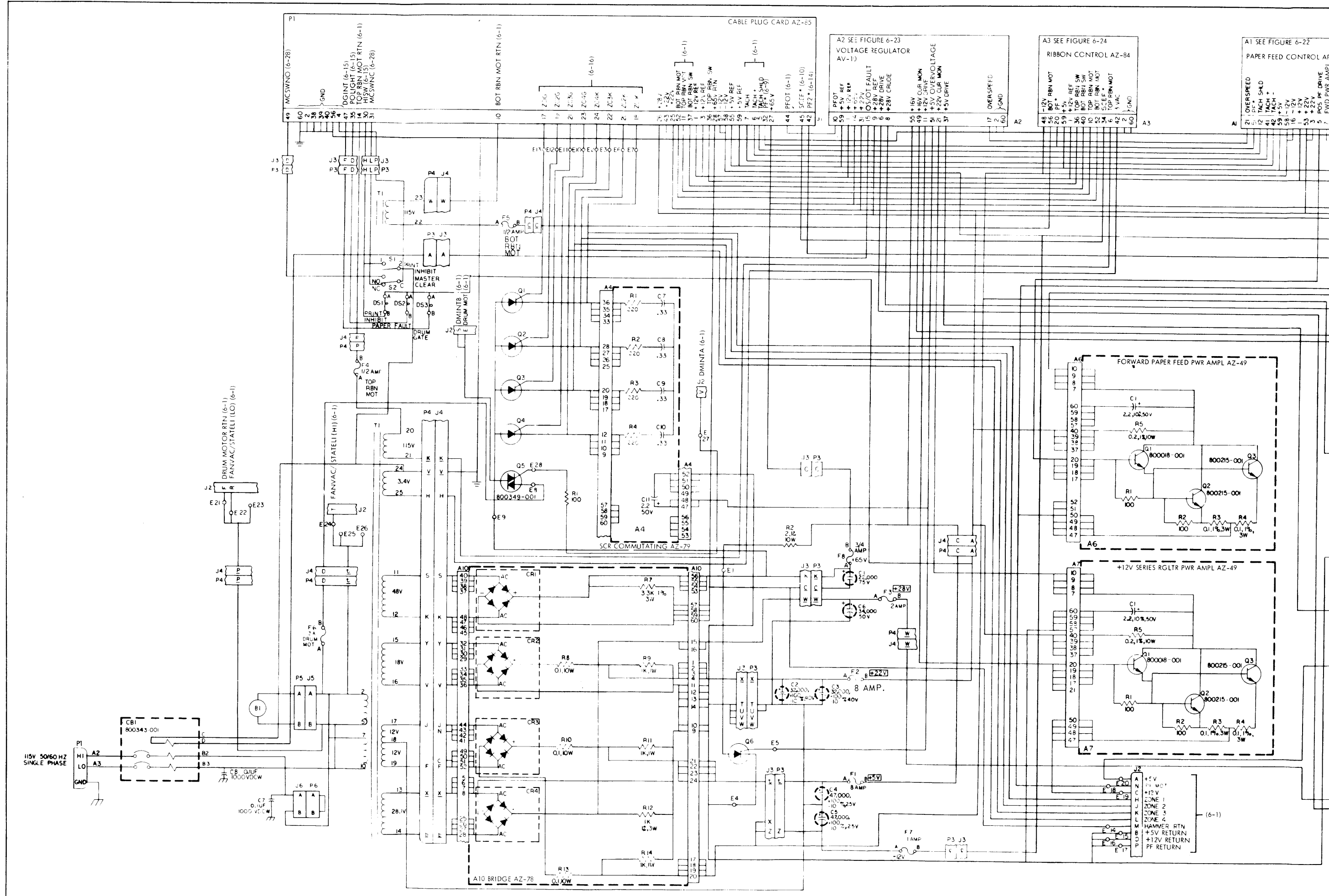


Figure 6-24. Ribbon Control AZ-84 Logic Diagram (Sheet 2 of 2)



P1 CABLE PLUG CARD AZ-65

A2 SEE FIGURE 6-23  
VOLTAGE REGULATOR  
AV-1

A3 SEE FIGURE 6-24  
RIBBON CONTROL AZ-84

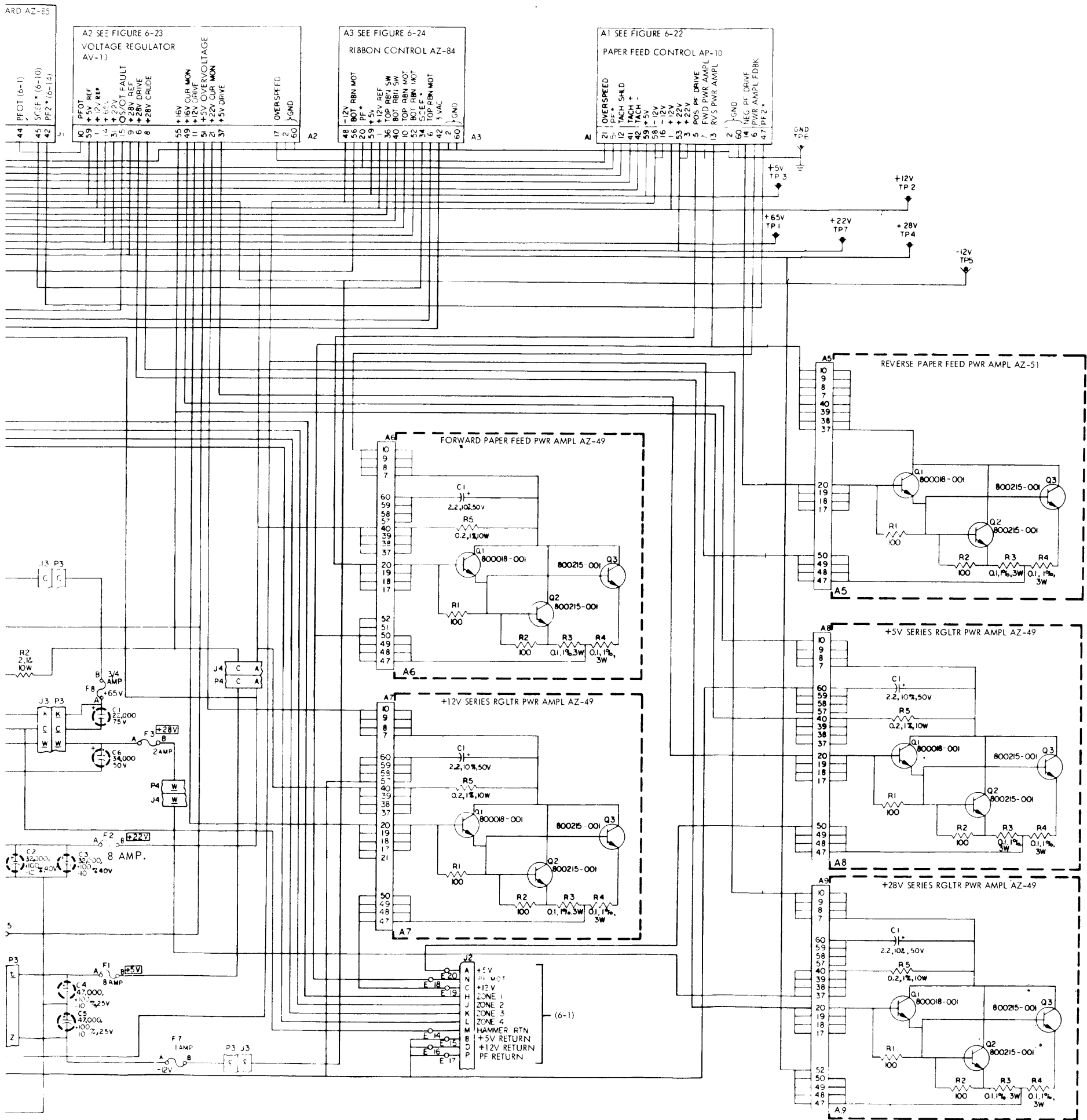
A1 SEE FIGURE 6-22  
PAPER FEED CONTROL AP

115V 50/60 HZ  
SINGLE PHASE

A10 BRIDGE AZ-78

(6-1)  
+5V  
+12V  
ZONE 1  
ZONE 2  
ZONE 3  
ZONE 4  
HAMMER RTN  
+5V RETURN  
+12V RETURN  
PF RETURN





CONN	REF	DES	PIN NO																									
			15	17	18	19	20	23	24	31	32	39	40	44	46	48	49	52	54	57								
XA1			15	17	18	19	20	23	24	31	32	39	40	44	46	48	49	52	54	57								
XA2			3	4	5	7	12	13	16	18	19	20	22	23	25	26	30	31	32	39	40	41	42	44	45	46	47	
XA3			3	13	14	15	16	17	19	21	22	23	24	25	26	29	30	31	32	35	39	43	44	45	46	47	49	57
XA4			2	8	13	14	15	16	23	24	57	58	59	60														
XA5			1	2	5	6	23	25	26	27	28	31	32	33	34	36	52											
XA6			4	5	6	13	14	15	21	22	23	25	26	27	31	32	7	7	7	7	7	7	7	7	7	7	7	
XA7			3	31	33	51	52																					
XA8			53																									
XA9			2	55																								
J1			15	29	33	41	48	53																				

1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 100 VOLT
3. ALL DIODE BRIDGES ARE 800516-001
4. ALL SCR'S ARE 800192-001
5. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH CIRCUIT NO.
6. COMPONENTS NOT MOUNTED ON MOTHER BOARD: C7, C8, CB1, B1, J5, J6, S1, S2, DS1, DS2, DF3, F1, F2, F3, F4, F5, F6, F7, F8, Q1, Q2, Q3, Q4, Q5, J1, T1, C1, C2, C3, C4, C5, C6, J2.
7. REFERENCE DPC DWG 216464C

Figure 6-25. Power Supply A4 Schematic Diagram

NOTES: UNLESS OTHERWISE SPECIFIED

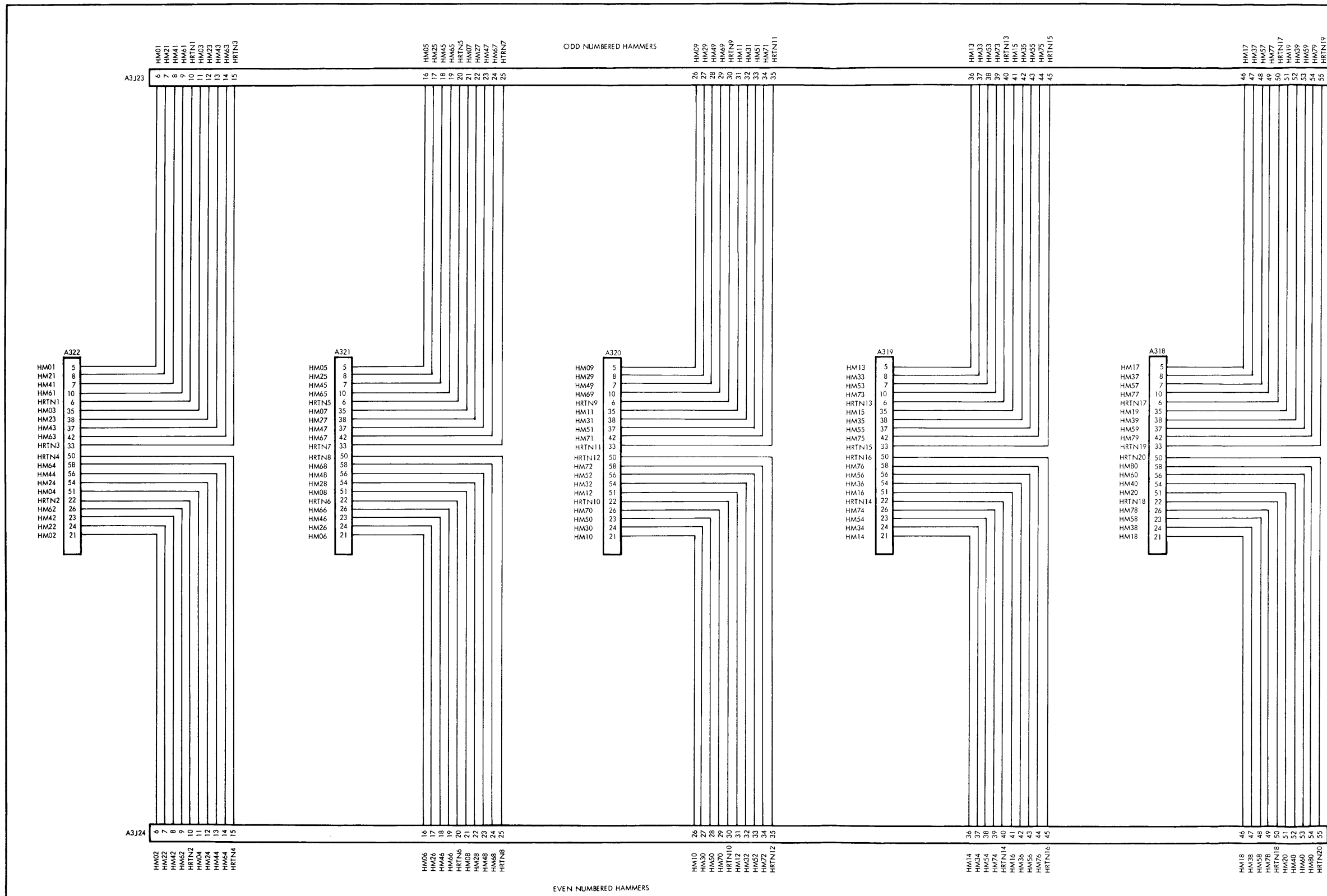


Figure 6-26. Hammer Drivers To Cable Plug Cards Interconnecting Diagram

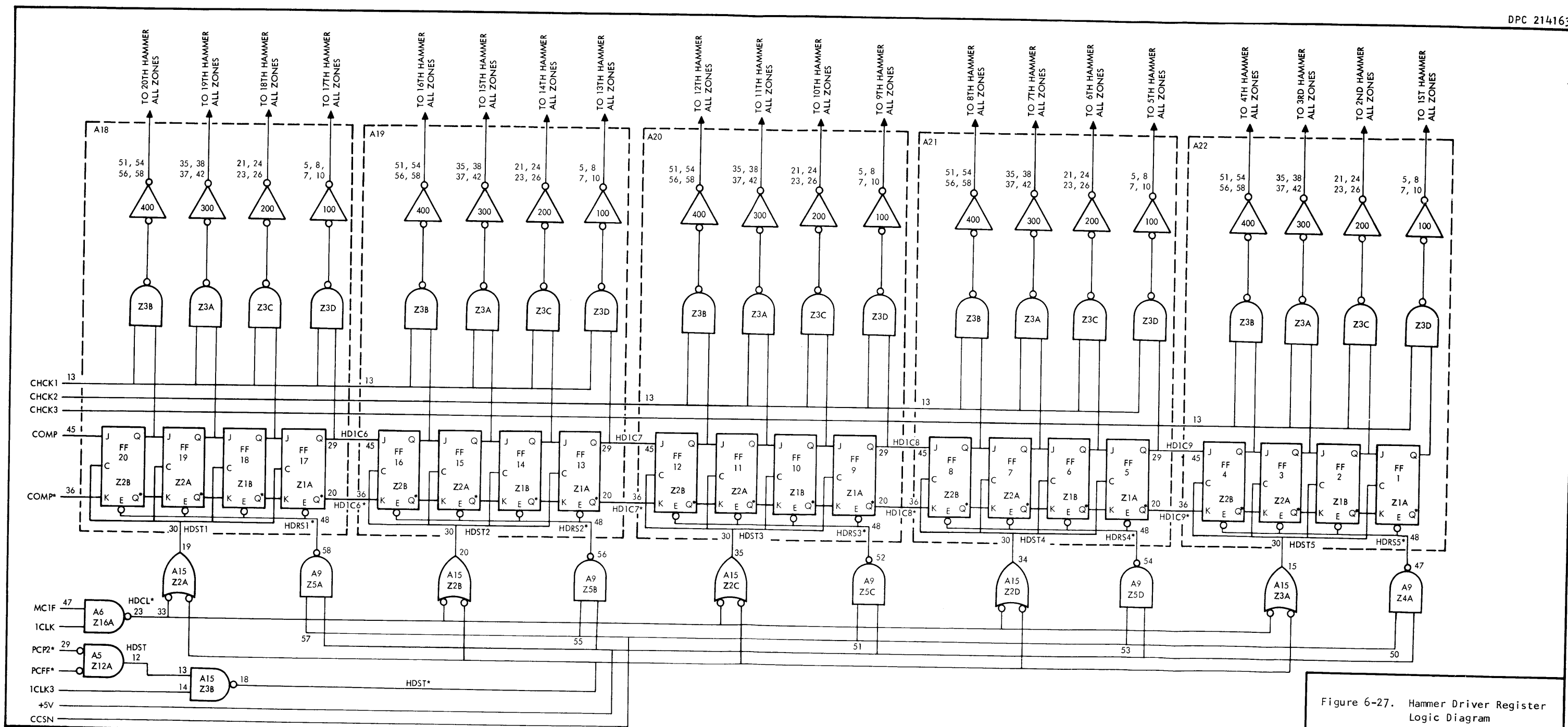


Figure 6-27. Hammer Driver Register Logic Diagram

DPC 214163B

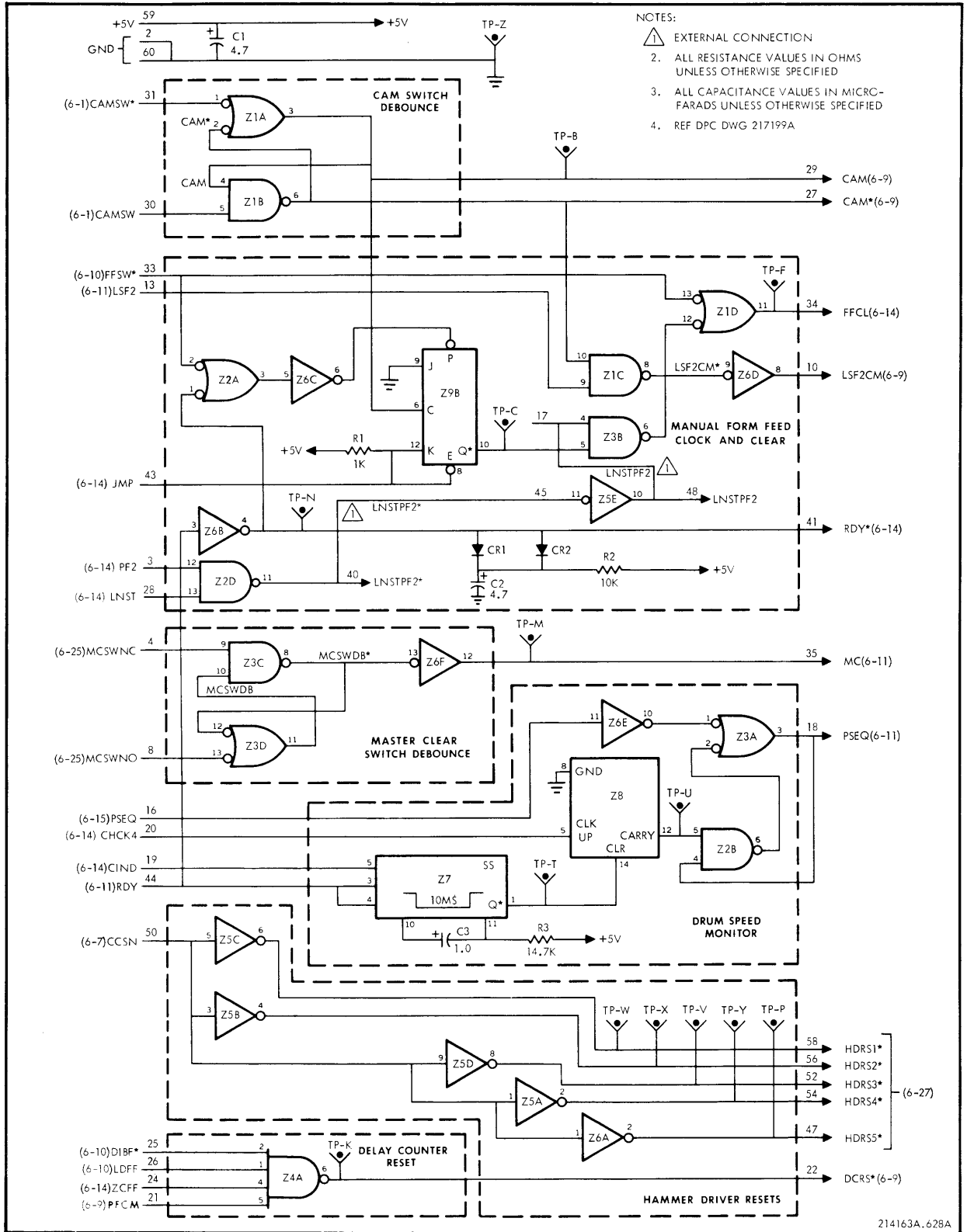


Figure 6-28. Delay Control and Gates AG-32 Logic Diagram (Sheet 1 of 2)

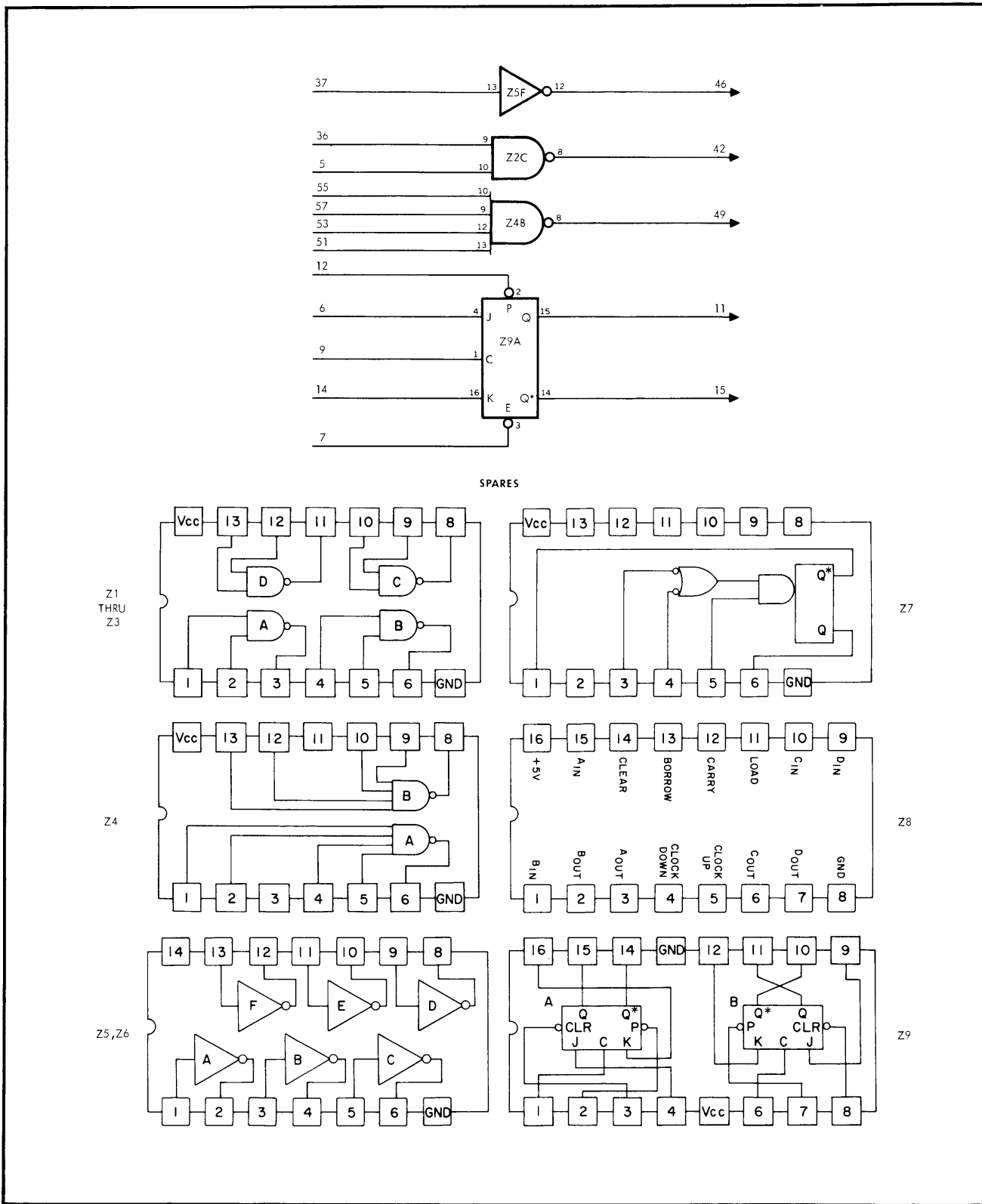
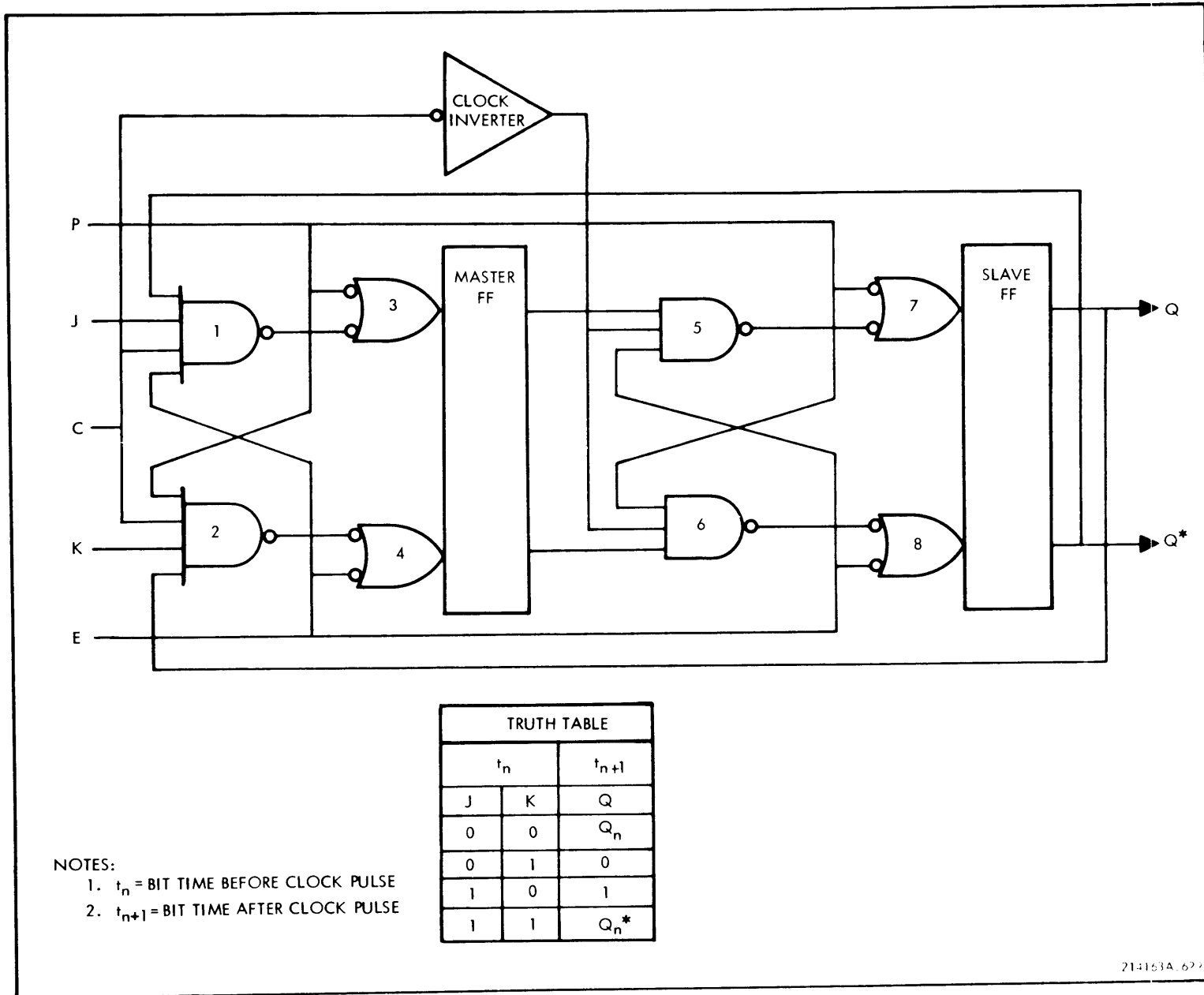


Figure 6-28. Delay Control and Gates AG-32 Logic Diagram (Sheet 2 of 2)

Figure 6-29. J-K Flip-Flop Logic Diagram



NOTES:

1.  $t_n$  = BIT TIME BEFORE CLOCK PULSE
2.  $t_{n+1}$  = BIT TIME AFTER CLOCK PULSE

TRUTH TABLE		
$t_n$		$t_{n+1}$
J	K	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$Q_n^*$

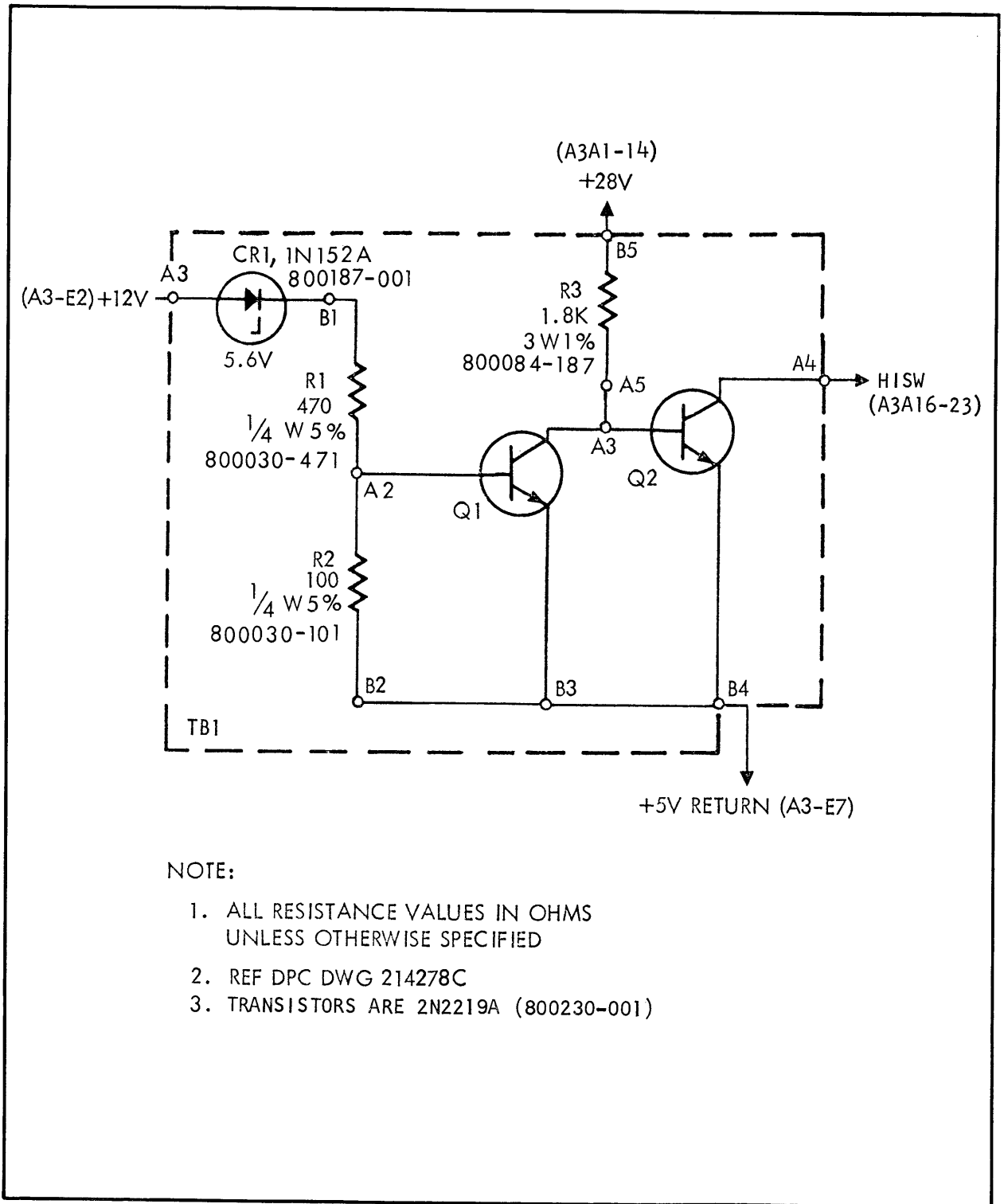


Figure 6-30. +12V Monitor Schematic Diagram

SECTION VII  
OPTIONS7-1 INTRODUCTION

7-2 This section describes the options that are available with the printer. See table 7-1 for the complement of printed circuit cards and cable plug cards necessary to implement the following options.

Table 7-1. Card Cage A3 Option Complement

Card Type	Description	Quantity	Reference Designator	Slot	Option
AL-11	Parity	1	A3A7	7	Parity
AL-12	Zone Select	1	A3A8	8	Zone Select
AJ-10	Negative Driver	1	A3A11	11	Negative Logic
AK-11	Inverting Receiver	1	A3A14	14	Negative Logic
AZ-14	Card Cage Interface Cable Plug Card	1	A3P14	14	Code Conversion
AL-27	Self Test	1	A3A25	25	Self Test

7-3 NEGATIVE LOGIC

7-4 As described in section IV, the printer is interfaced to the user system through eight receivers and two drivers (figure 4-2). To interface negative logic it is necessary to substitute inverting receiver AK-11 (figure 7-1) and negative driver AJ-10 (figure 7-2) for receiver AK-10 and positive driver AJ-11 normally supplied with the printer. See table 7-2 for the negative logic receiver and driver characteristics.



DPC 214163

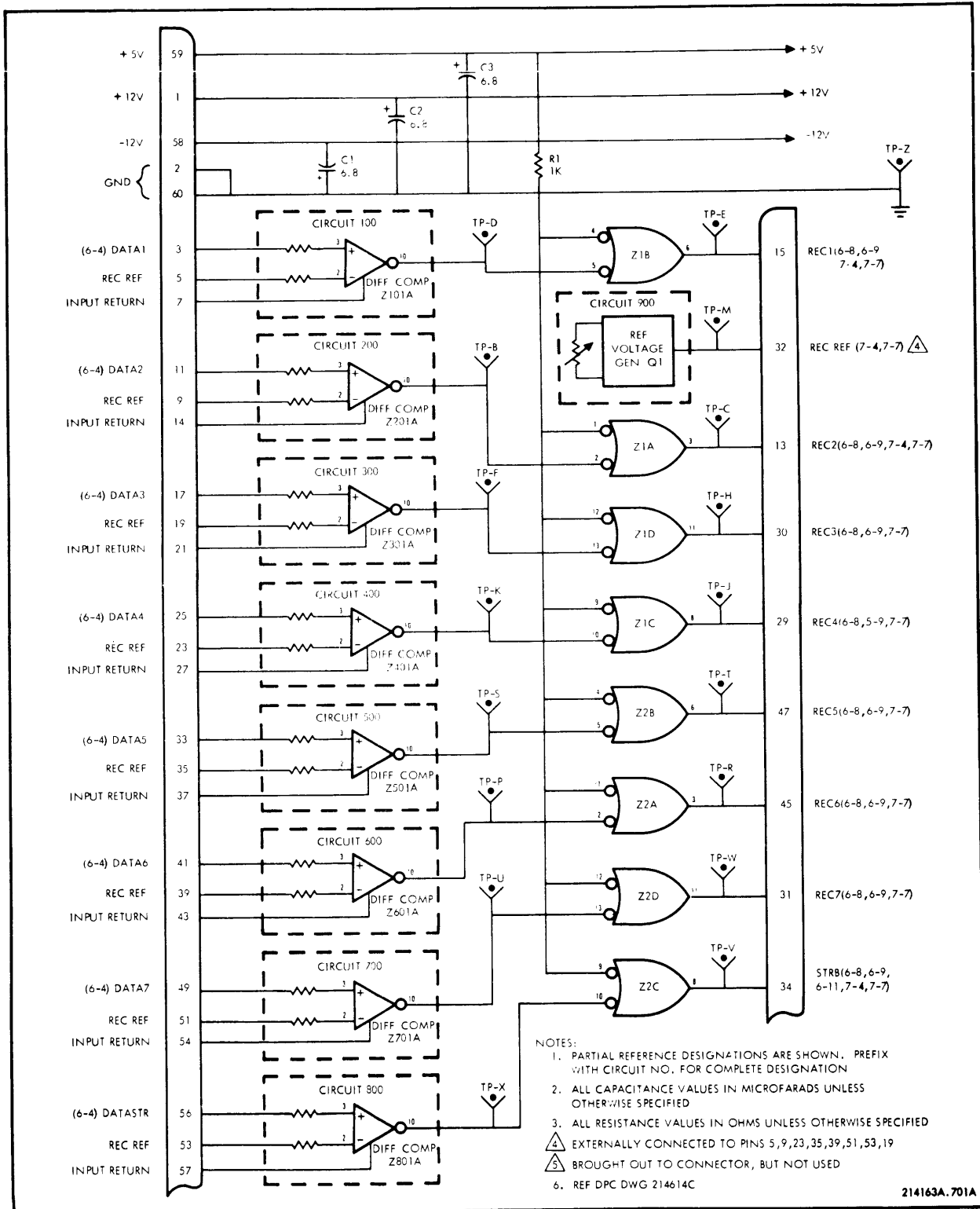


Figure 7-1. Inverting Receiver AK-11 Schematic Diagram (Sheet 1 of 2)

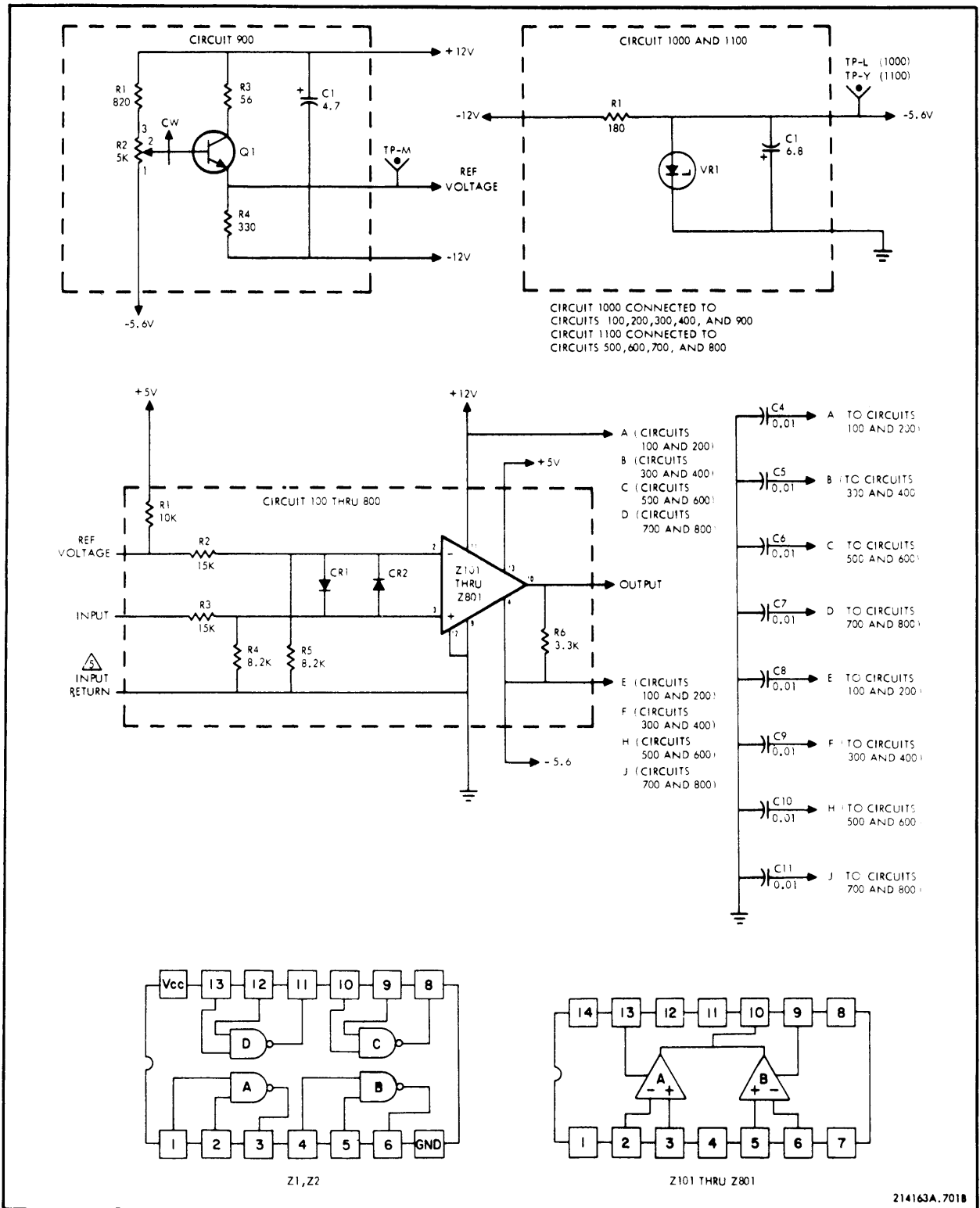
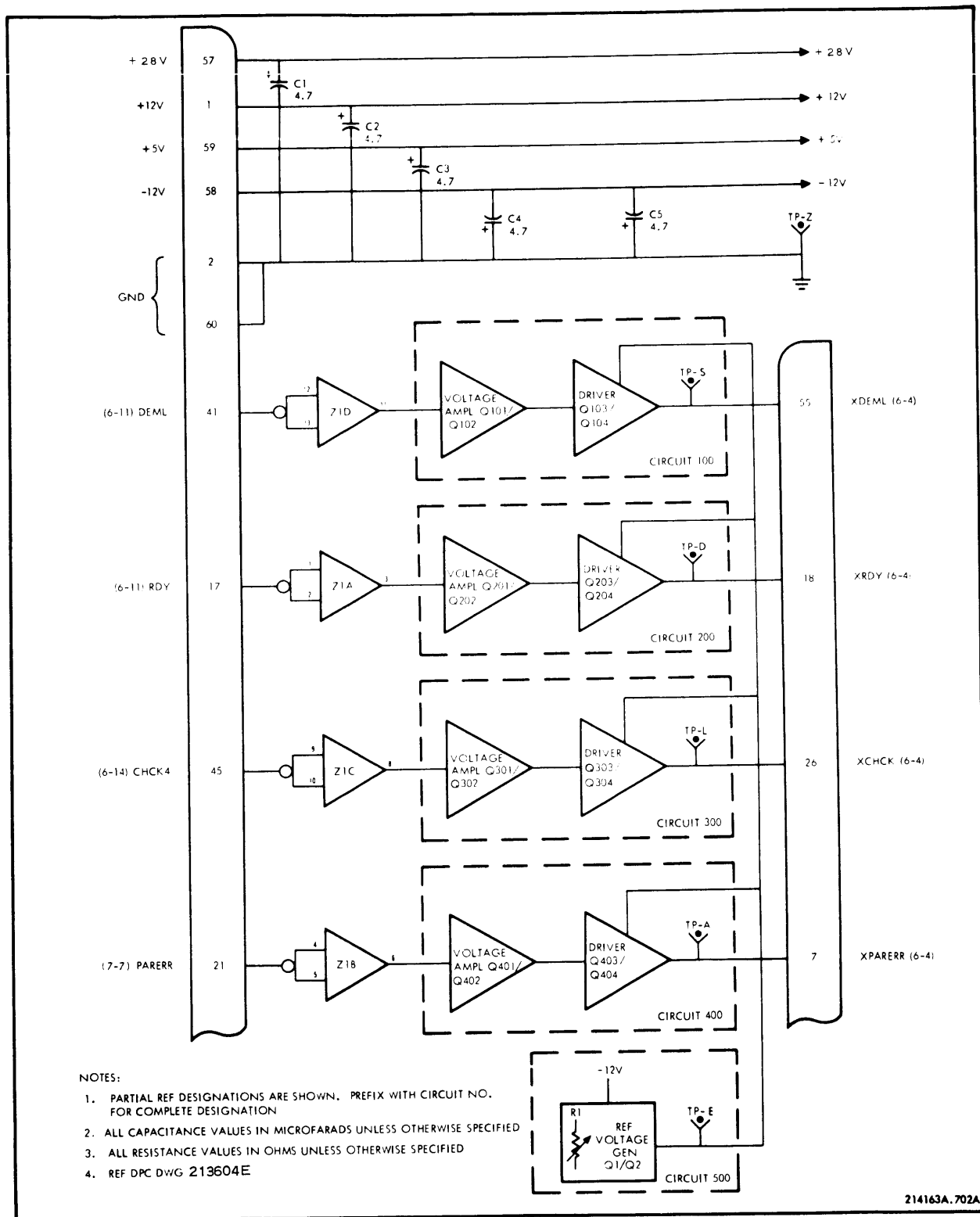


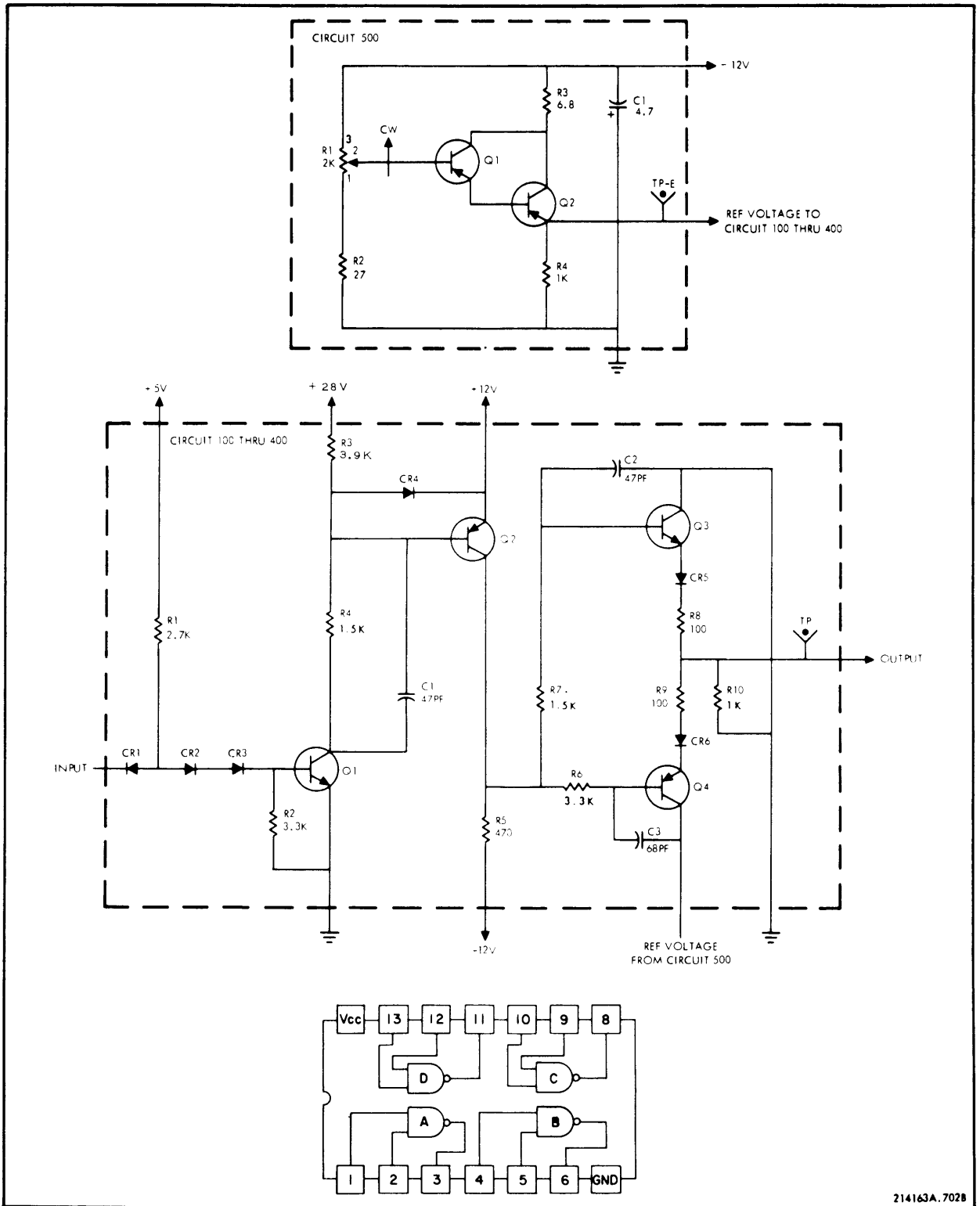
Figure 7-1. Inverting Receiver AK-11 Schematic Diagram (Sheet 2 of 2)

DPC 214163B



214163A.702A

Figure 7-2. Negative Driver AJ-10 Schematic Diagram (Sheet 1 of 2)



214163A.702B

Figure 7-2. Negative Driver AJ-10 Schematic Diagram (Sheet 2 of 2)

Table 7-2. Negative Logic Receiver/Driver Characteristics

Item	Receiver	Driver
Input Impedance	10K	
Output Impedance		100 ohms
Load Resistance		10K to ground
Load Capacitance		220 pf
Signal Transition Rate		40v/usec (typical)
Logic 1	Adjustable from -10.0v max to - 3.0v min	Adjustable from -8.0v max to -3.0v min
Logic 0	-1.0v max 0.0v min	-1.0v max
Threshold Voltage	1/2 of logic 1	

7-5 The negative logic receiver and driver reference voltages are adjusted relative to the printer logic 1 voltage levels. In the calibration procedures that follow, test connections to card test points are called out as follows:

Sample Callout

A3-14M

Definition

A3 = Card cage A3

14 = Card location (slot)

M = Card test point

7-6 CALIBRATION OF INVERTING RECEIVER AK-11 REFERENCE VOLTAGE

7-7 Calibrate inverting receiver AK-11 reference voltage as follows:

a. Set oscilloscope (2, table 5-2) controls and switches as follows:

Switch or Control

MODE  
VOLTS/CM  
VARIABLE  
STABILITY  
TRIGGERING LEVEL  
TRIGGERING MODE  
TRIGGER SLOPE  
AC-DC-GND

Setting

CH1  
.5  
CALIBRATED  
full clockwise  
full clockwise  
AC  
INT +  
DC

b. Connect CHANNEL 1 probe (3, table 5-2) to A3-14M, and probe ground lead to A3-14Z.

c. Adjust potentiometer R2(14) (figure 5-8) until voltage displayed at A3-14M is equal to 1/2 of the printer logic 1 voltage level.

d. Remove probe from A3-14M and A3-14Z.

#### 7-8 CALIBRATION OF NEGATIVE DRIVER AJ-10 REFERENCE VOLTAGE

7-9 Calibrate negative driver AJ-10 reference voltage as follows:

a. Set oscilloscope (2, table 5-2) controls and switches as follows:

<u>Switch or Control</u>	<u>Setting</u>
MODE	CH1
VOLTS/CM	.5
VARIABLE	CALIBRATED
STABILITY	full clockwise
TRIGGERING LEVEL	full clockwise
TRIGGERING MODE	AC
TRIGGER SLOPE	INT +
AC-DC-GND	DC

b. Connect CHANNEL 1 probe (3, table 5-2) to A3-11E, and probe ground lead to A3-11Z.

c. Adjust potentiometer R1 (figure 5-8) until the voltage displayed at A3-11E equals the printer logic 1 voltage level.

d. Remove probe from A3-11E and A3-11Z.

#### 7-10 ZONE SELECT

7-11 The zone select option allows users, with requirements for short lines that are not left-justified, to operate at increased rates. Zone select card AL-12 and interface signal, ZONE SELECT, are necessary to implement the option. Signal ZONE SELECT, when true, indicates that information on data lines 1 and 2 defines the zone in which the subsequent data is to be printed. This information is strobed by the user in the same manner as normal data, and if there is no data in memory at this time, the printer advances to the selected zone and accepts data to be printed in that zone. If data is present in memory, it is printed prior to completion of the zone select operation.

7-12 The user should not follow a zone select code on the data lines with a format control code (PF, CR, or FF) since these signals initiate the print cycle and clear the column register, returning it to the leftmost print position. The data line codes for ZONE SELECT are as follows:

DPC 214163B

	<u>DATA LINE 2</u>	<u>DATA LINE 1</u>	<u>COLUMNS</u>
Zone 1	0	0	1 thru 20
Zone 2	0	1	21 thru 40
Zone 3	1	0	41 thru 60
Zone 4	1	1	61 thru 80

7-13 ZONE SELECT IMPLEMENTATION (Figure 7-3)

7-14 To implement the zone select option, set circuit breaker CB1 to OFF and install card AL-12 (A3A8) in slot 8 of card cage A3. Delete and add the following jumpers:

<u>Delete Following Jumpers</u>	<u>Add Following Jumpers</u>
J8-8 to J8-40	J11-45 to J8-26
J8-9 to J8-41	J15-55 to J5-44
J8-10 to J8-46	J8-28 to J6-41
J8-11 to J8-45	
J8-12 to J8-47	
J6-41 to J5-53	
J6-41 to J5-44	

Note

If printer is used with negative logic system, ensure card AL-12 is wired for same (figure 7-4).

7-15 ZONE SELECT OPERATION (Figure 7-4)

7-16 The zone select operation is initiated by the user system and can occur with the printer in any of the following conditions:

- a. Data not in memory - paper not moving
- b. Data not in memory - paper moving
- c. Data in memory

7-17 The following paragraphs describe the zone select operation for each condition. See figure 7-5 for a timing diagram of the zone select operation.

7-18 Data Not In Memory - Paper Not Moving

7-19 For all operating conditions, flip-flops Z3A, Z3B, Z4A, Z4B, Z8B, and Z10A are initially cleared when MC1\* goes low in the master clear state.

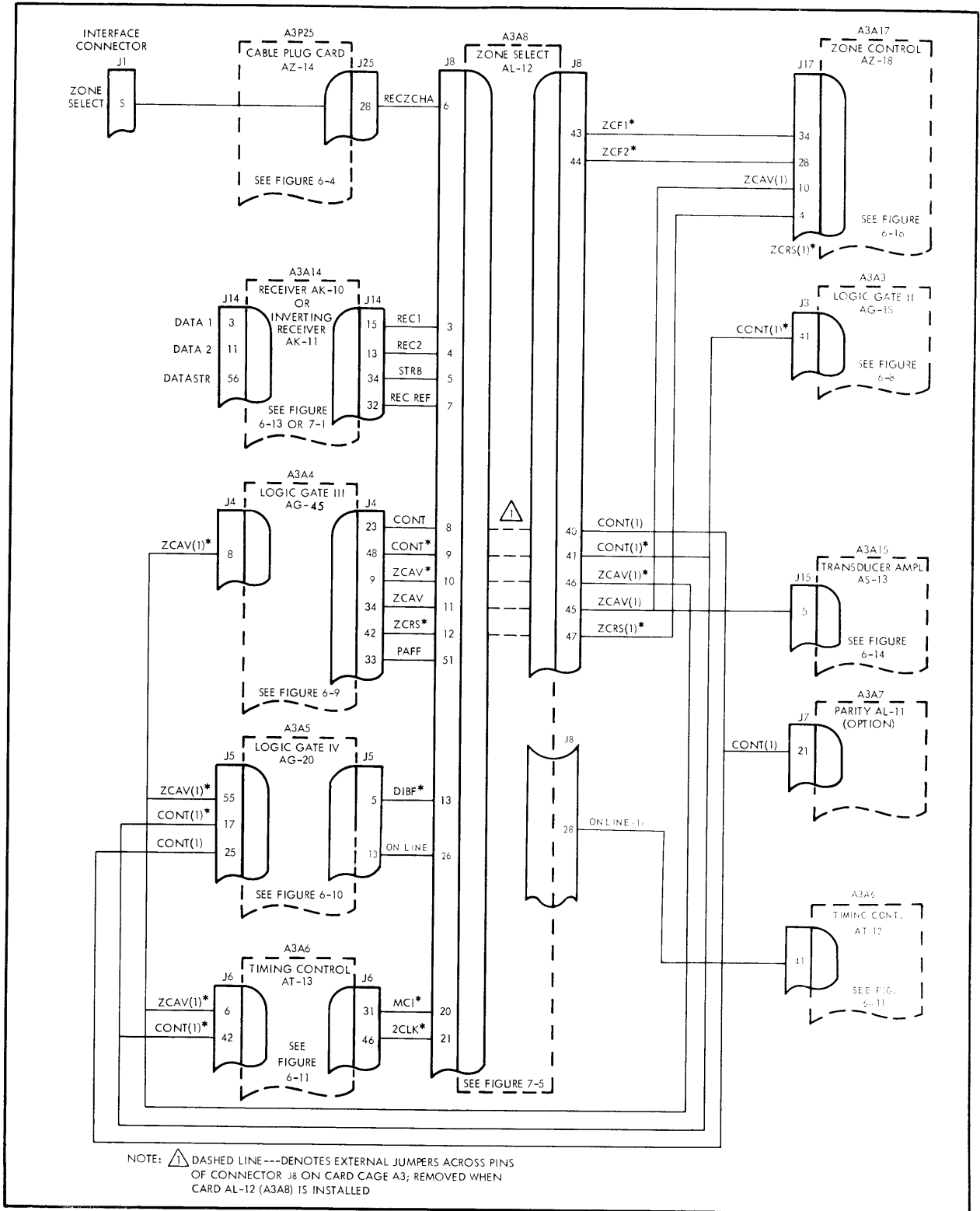
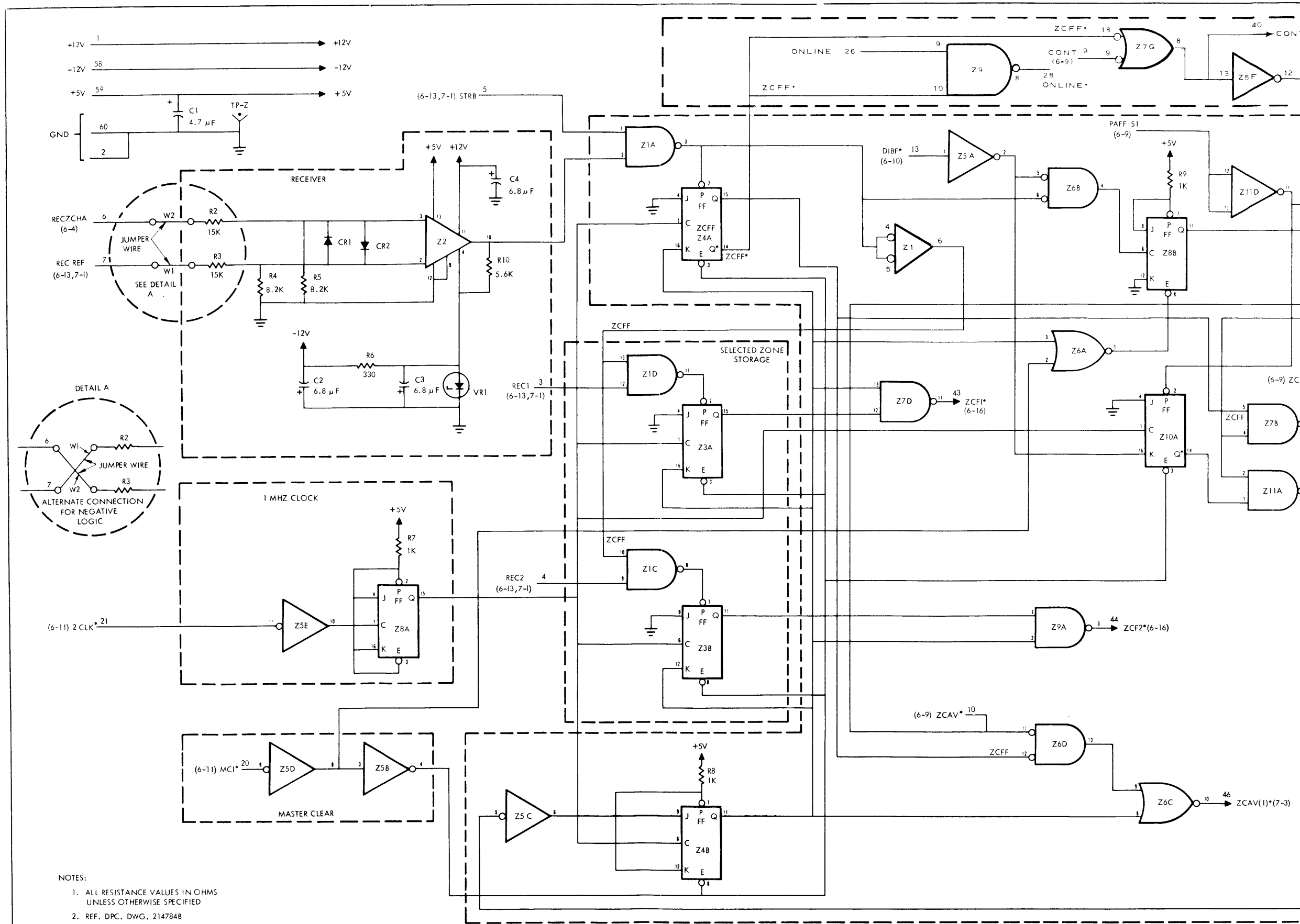


Figure 7-3. Zone Select Option Interconnecting Diagram





- NOTES:
1. ALL RESISTANCE VALUES IN OHMS UNLESS OTHERWISE SPECIFIED
  2. REF. DPC. DWG. 2147848



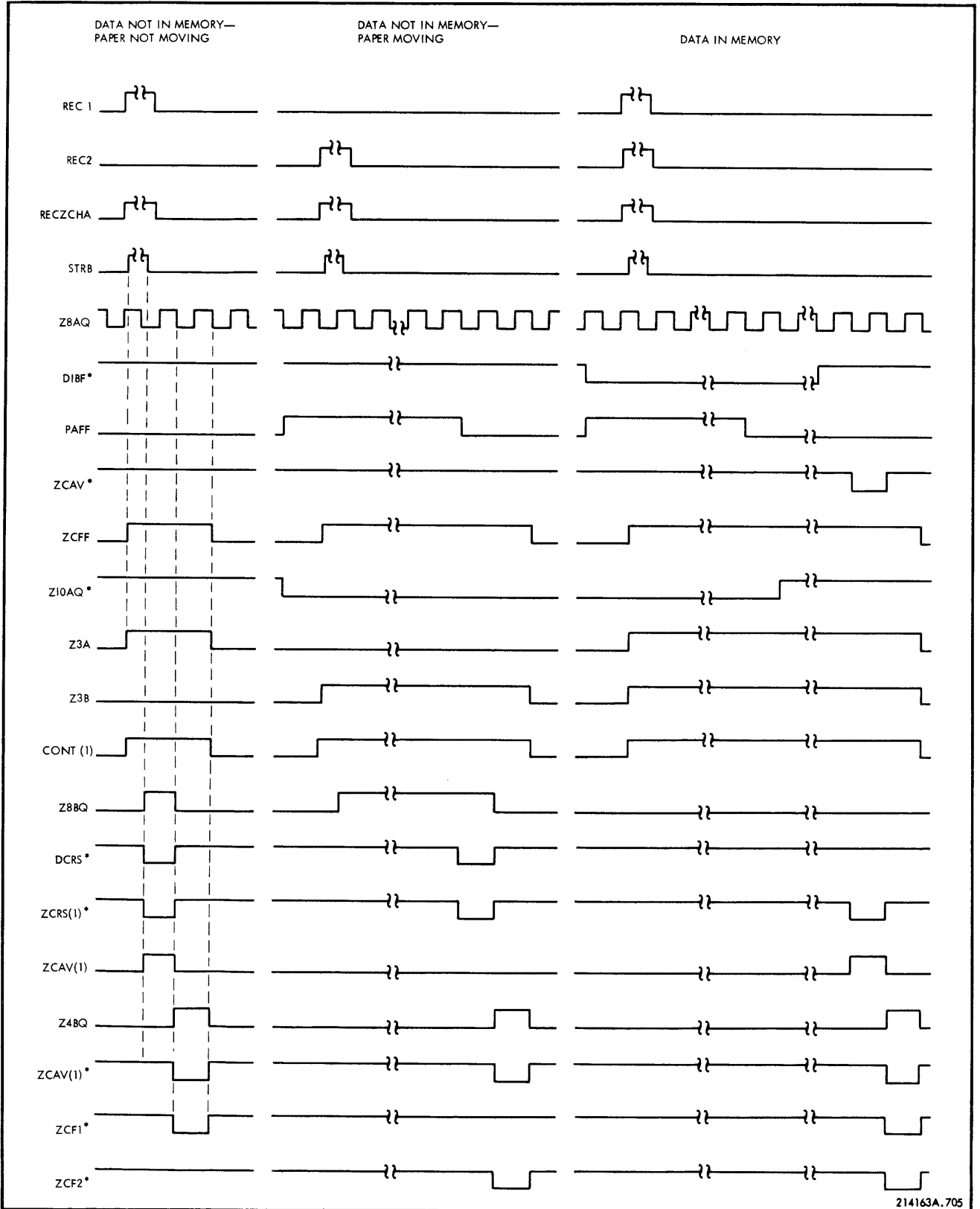


Figure 7-5. Zone Select Option Timing Diagram

7-20 The clock inputs for flip-flops Z3A, Z3B, Z4A, Z4B, and Z10A are provided by flip-flop Z8A. Printer clock signal ZCLK is inverted by Z5E and applied to the clock input of flip-flop Z8A. Since the flip-flop inputs are tied together and always true, the flip-flop toggles continuously on each fall of its clock input and divides down by 1/2 to produce a 1 MHz clock signal for the zone select logic.

7-21 Assuming the user raises signal ZONE SELECT and transmits the code for zone 2, inputs RECZCHA and REC1 go high and are applied to receiver Z2 and NAND gate Z1D, respectively. The receiver output goes high and is applied to NAND gate Z1A. The user follows the code with signal DATA STROBE and STRB goes high enabling NAND gate Z1A. The gate output goes low, presets flip-flop Z4A (ZCFF) and is also applied to NOR gate Z6B and Z1B. Z1B output goes high, enables gate Z1D and flip-flop Z3A is preset. Output ZCFF\* goes low, is applied to NAND gates Z7G and Z9-10. CONT(1) goes high and CONT(1)\* goes low.

7-22 CONT(1) and CONT(1)\* and on-line \*(1) are applied to the printer logic in the same manner as CONT and CONT\* and on-line\*(1). At this time the column and data registers and flip-flop LDFF are reset.

7-23 Since input DIBF\* is high, (no data in memory), the output of inverter Z5A is low and applied to gate Z6B. With both inputs to gate Z6B low, the clock input to flip-flop Z8B goes high.

7-24 As input PAFF is low (paper not moving), the output of NAND gate Z11D is high and applied to NAND gate Z11C. The preset input to flip-flop Z10A is disabled. At the completion of DATA STROBE, STRB goes low, the output of gate Z1A goes high and the clock input to flip-flop Z8B falls. Flip-flop Z8B sets, enables gate Z11C, and output DCRS\* goes low.

7-25 When DCRS\* goes low, the output of NAND gate Z9D goes high. NAND gates Z7B and Z11A are enabled and ZCRS(1)\* goes low and ZCAV(1) goes high. ZCRS(1)\* and ZCAV(1) are applied to the printer logic in the same manner as ZCRS\* and ZCAV. ZCRS(1)\* clears zone control flip-flops A17Z1A and A17Z1B (figure 6-16) and starts the 1.3 millisecond one-shot and delay in CKT500. ZCAV(1) is applied to the set input of recovery reset flip-flop A15Z5A (figure 6-14) and on the next clock (1CLK4), flip-flop A15Z5A sets. The output of gate Z7B is also applied to inverter Z5C and the set input to flip-flop Z4B goes high.

7-26 On the first clock after its set input goes high, flip-flop Z4B sets and output Z4BQ goes high. Output Z4BQ enables NAND gate Z7D and NOR gates Z6A and Z6C. It is also applied to the reset inputs of flip-flops Z3A, Z3B, and ZCFF. The output of gate Z6A goes low and clears flip-flop Z8B, disabling gate Z11C. DCRS\* and ZCRS(1)\* go high and ZCAV(1) goes low. The outputs of gates Z7D and Z6C, ZCF1\* and ZCAV(1)\* also go low at this time. When ZCF1\* goes low, flip-flop A17Z1A is preset, enabling NAND gate A17Z2C. The output of gate A17Z2C goes low, is inverted by A17Z2B and applied to the set input of flip-flop A17Z4B. ZCAV(1)\* is applied to the printer logic in the same manner as ZCAV\* and initiates that portion of the zone change operation (section IV) in which flip-flops LDFF and DLFF are set, and DEMAND LINE is raised.

7-27 On the next clock, flip-flops Z3A, Z4B, and ZCFF reset. If flip-flop Z3B had previously been set, it too would reset at this time.

7-28 When the 1.3 millisecond one-shot and delay sequence, previously started, is completed, flip-flop A17Z4B is clocked and set, and the flip-flop set for the previous zone is reset. The +65v excitation is switched to the zone 2 hammers, completing the zone select operation.

7-29 Data Not In Memory - Paper Moving

7-30 The following operation is basically as previously described for the data not in memory - paper not moving condition.

7-31 Assuming ZONE SELECT is raised and the code for zone 3 is transmitted, inputs RECZCHA and REC2 go high. On receipt of DATA STROBE, STRB goes high, flip-flop ZCFF is preset and CONT(1) goes high and CONT(1)\* goes low. NAND gate Z1C is also enabled, and the gate output goes low, presetting flip-flop Z3B. When STRB goes low, flip-flop Z8B is clocked and set.

7-32 As input PAFF is high (paper moving) the output of NAND gate Z11D goes low, presetting flip-flop Z10A. When paper stops moving, PAFF goes low and the output of gate Z11D goes high. NAND gates Z11C and Z7B are then enabled. DCRS\* and ZCRS(1)\* go low and the set input to flip-flop Z4B goes high. The zone control flip-flops are cleared and the 1.3 millisecond one-shot and delay is started.

7-33 On the next clock, flip-flop Z4B sets. NAND gate Z9A, and NOR gates Z6A and Z6C are enabled, and flip-flop Z8B is cleared. DCRS\* and ZCRS(1)\* go high, and ZCAV(1)\* and ZCF2\* go low. As previously described, ZCAV(1)\* initiates a portion of the zone change operation.

7-34 When ZCF2\* goes low, flip-flop A17Z1B is preset, enabling NAND gate A17Z3D. The output of gate A17Z3D goes low, is inverted by A17Z3A and applied to the set input of flip-flop A17Z5A.

7-35 On the following clock, flip-flops Z3B, Z4B, and ZCFF reset.

7-36 On completion of the 1.3 millisecond one-shot and delay sequence, flip-flop A17Z5A is clocked and set, and the flip-flop set for the previous zone is reset. The +65v excitation is switched to the zone 3 hammers, completing the zone select operation.

7-37 Data In Memory

7-38 The zone select operation with data in memory is basically as described for the other conditions.

7-39 Assuming ZONE SELECT is raised and the code for zone 4 is transmitted, inputs RECZCHA, REC1 and REC2 go high. On receipt of DATA STROBE, STRB goes high and as previously described, flip-flops ZCFF, Z3A, and Z3B preset. CONT(1) goes high and CONT(1)\* goes low. Assuming paper is moving at this time, PAFF is high and flip-flop Z10A also presets. When CONT(1) goes high, the printer enters the scan and print state (section IV), and waits for paper to stop moving.

7-40 Since DIBF\* is low (data in memory) the output of inverter Z5A is high and applied to the reset input of flip-flop Z10A. When paper stops moving, PAFF goes low, the output of gate Z11D goes high and the preset input to flip-flop Z10A is disabled. On the next clock flip-flop Z10A resets.

7-41 On completion of the delay counter sequence (section iv) the scan and print operation continues and DIBF\* goes high when all data in memory is printed. A zone change operation is then initiated by the printer logic and ZCAV\* goes low. ZCAV\* is applied to NAND gate Z9D. The gate output goes high, enables NAND gates Z7B and Z11A and ZCRS(1)\* goes low and ZCAV(1) and the set input to flip-flop Z4B go high. The zone control flip-flops are cleared and the 1.3 millisecond one-shot and delay is started.

7-42 On the next clock, flip-flop Z4B sets and NAND gates Z9A and Z7D and NOR gate Z6C are enabled. ZCAV\* and ZCRS(1)\* go high, and ZCAV(1), ZCAV(1)\*, ZCF1\*, and ZCF2\* go low.

7-43 When ZCF1\* and ZCF2\* go low, flip-flops A17Z1A and A17Z1B are preset, enabling NAND gate A17Z3C. The output of gate A17Z3C goes low, is inverted by A17Z3B and applied to the set input of flip-flop A17Z5B.

7-44 On the following clock, flip-flops Z3A, Z3B, Z4B, and ZCCF reset.

7-45 On completion of the 1.3 millisecond one-shot and delay sequence, flip-flop A17Z5B is clocked and set, and the flip-flop set for the previous zone is reset. The +65v excitation is switched to the zone 4 hammers, completing the zone select operation.

#### 7-46 PARITY CHECK

7-47 The parity check option assures the user that the printout is an accurate reproduction of the input data. The user is alerted when erroneous data is received.

7-48 A 7-bit code is used to transmit information to the printer on data lines DATA1 thru DATA7. A parity bit is added to the 7-bit code and transmitted to the printer on data line PARITY DATA. Each printable character is now represented by an odd number binary code and an even number code becomes a nonprintable character.

7-49 The eight data lines connect through interface receivers to a parity generator whose output remains low if the incoming character code is decoded as an odd number binary input. If a bit is dropped in transmission, it is decoded as an even number binary input. The parity generator then raises signal PARITY ERROR to the user and the erroneous code is cleared from the data register. PARITY ERROR remains high until receipt of a control character.

7-50 When PARITY ERROR is raised, the user can choose to do one of the following:

- a. Send CR command and retransmit and overprint the line of data in which the error was detected.
- b. Send PF command and reprint data on the following line.

## DPC 214163A

c. Ignore parity error and continue printing. A space then appears in the location the erroneous character would have occupied.

### 7-51 PARITY CHECK IMPLEMENTATION (Figure 7-6)

7-52 To implement the parity check option, set circuit breaker CB1 to OFF and install card AL-11 (A3A7) in slot 7 of card cage A3. Remove the jumper across pins 23 and 40 of connector J8.

#### Note

If printer is used with negative logic system, ensure card AL-11 is wired for same (figure 7-7).

### 7-53 PARITY CHECK OPERATION (Figure 7-7)

7-54 The following paragraphs describe the parity check operation for each character received.

7-55 Flip-flops PARERR and DRRS are initially cleared when MC1\* goes low in the master clear state.

7-56 Parity bit RECPAR1 is applied to receiver Z5 and the receiver output goes to parity generator Z1.

7-57 If an odd number of inputs are high, the received character code is correct and the parity generator output stays low, inhibiting NAND gate Z2D.

7-58 If an even number of inputs are high, the received character code is erroneous and the parity generator output goes high. When signal DATA STROBE is raised, STRB goes high and enables gate Z2D. The gate output goes low and presets parity error flip-flop PARERR and data register reset flip-flop DRRS. Output PARERR goes high, is applied to a driver, and raises signal PARITY ERROR to the user. Output DRRS goes high, enables NOR gate Z4A, and MC1(1)\* is applied to NAND gate A3Z12C (figure 6-8) and the clear inputs to the data register flip-flops go low. When STRB goes low, the data register resets, erasing the erroneous code. The data register is held in the reset state until TS02 goes high. On the next clock, flip-flop DRRS resets and MC1(1)\* goes high, removing the clear input from the data register.

7-59 On receipt of a control character, CONT goes high and on the next clock flip-flop PARERR resets. The parity check operation is completed.

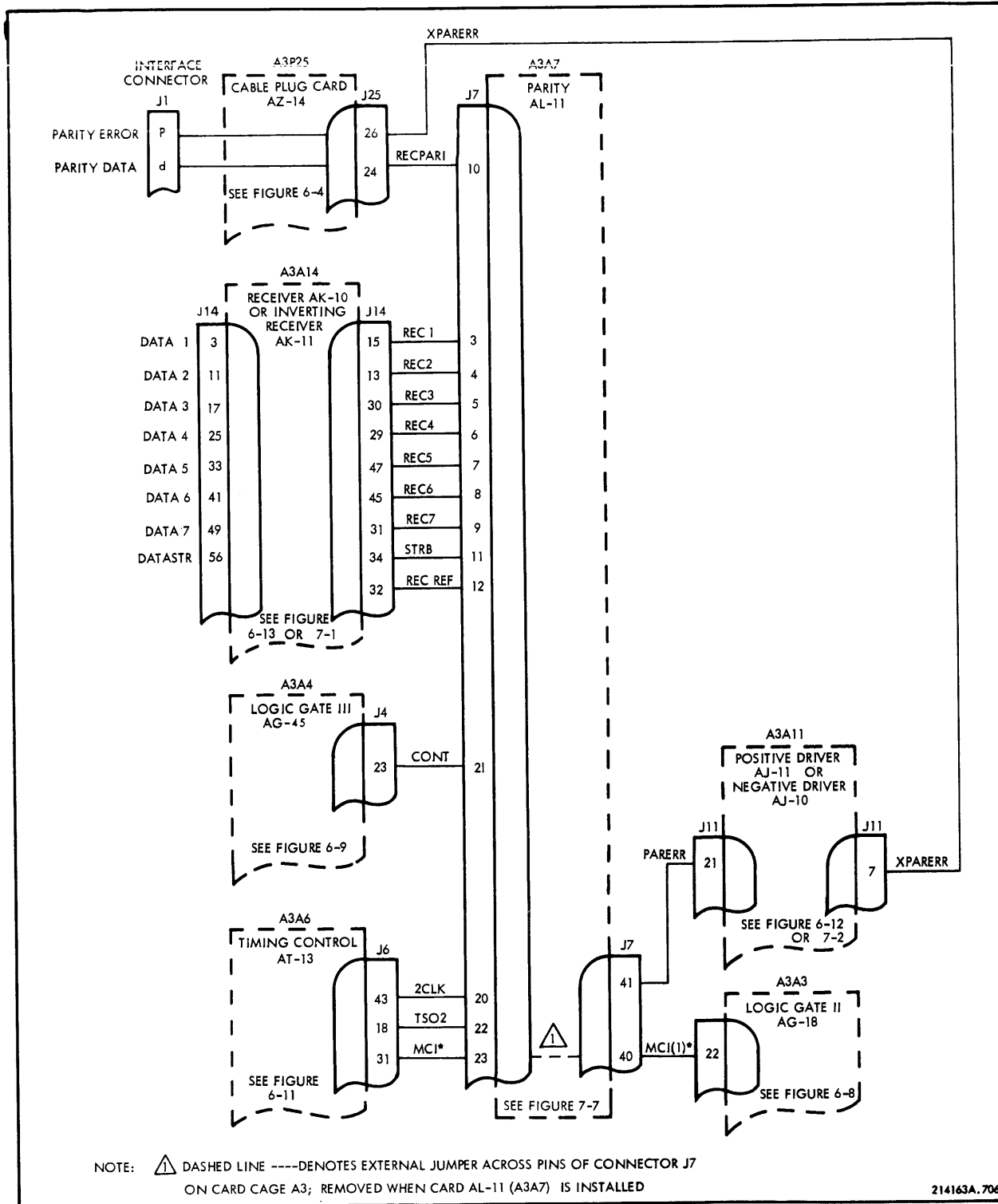


Figure 7-6. Parity Option Interconnecting Diagram



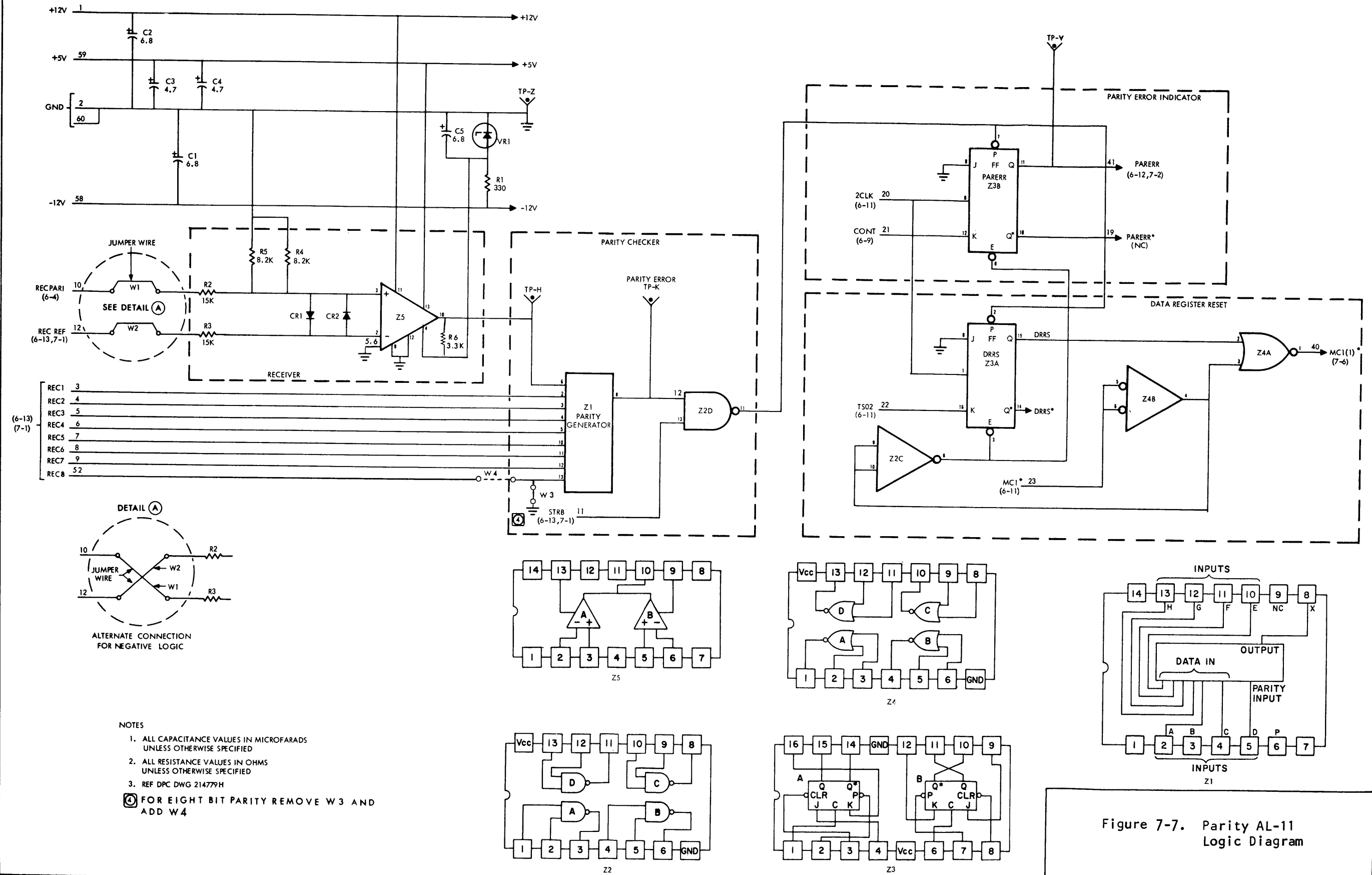


Figure 7-7. Parity AL-11 Logic Diagram

7-60 CODE CONVERSION

7-61 The code conversion option permits the user to transmit a unique 6, 7, or 8-bit code with or without parity, and convert it to the internal printer code. To allow time for conversion, the maximum transfer rate is reduced from 500 kHz to 250 kHz.

## 7-62 CODE CONVERSION IMPLEMENTATION (Figure 7-8)

7-63 Implementation of the code conversion option requires the addition of card cage A6 and the card complement listed in table 7-3.

Table 7-3. Card Cage A6 Complement

Card Type	Description	Quantity	Reference Designator	Slot
AZ-14	Card Cage Interface Cable Plug Card	1	A6B14	14
AK-10*	Receiver	2	A6B15 and A6B22	15 and 22
AK-11*	Inverting Receiver (Negative Logic Systems)	1	A6B15	15
AZ-67	Matrix Driver	1	A6B16	16
AZ-56	Diode Matrix	5(max)**	A6B17 thru A6B21	17 thru 21
*Removed from Card Cage A3				
**64-character printer uses A6B17 thru A6B19 96-character printer uses A6B17 thru A6B21				

## 7-64 CODE CONVERSION OPERATION

7-65 Signals DATA1 thru DATA7 and DATASTR are interfaced to receiver A6B15 (AK-10/AK-11). The receiver outputs, DATA1 thru DATA7 and STRB, are fed to a matrix driver.

7-66 Matrix driver AZ-67 (figure 7-9) inverts the DATA signals in a manner which provides a high and low output for each DATA input. The matrix driver outputs are then fed to a diode matrix for decoding.

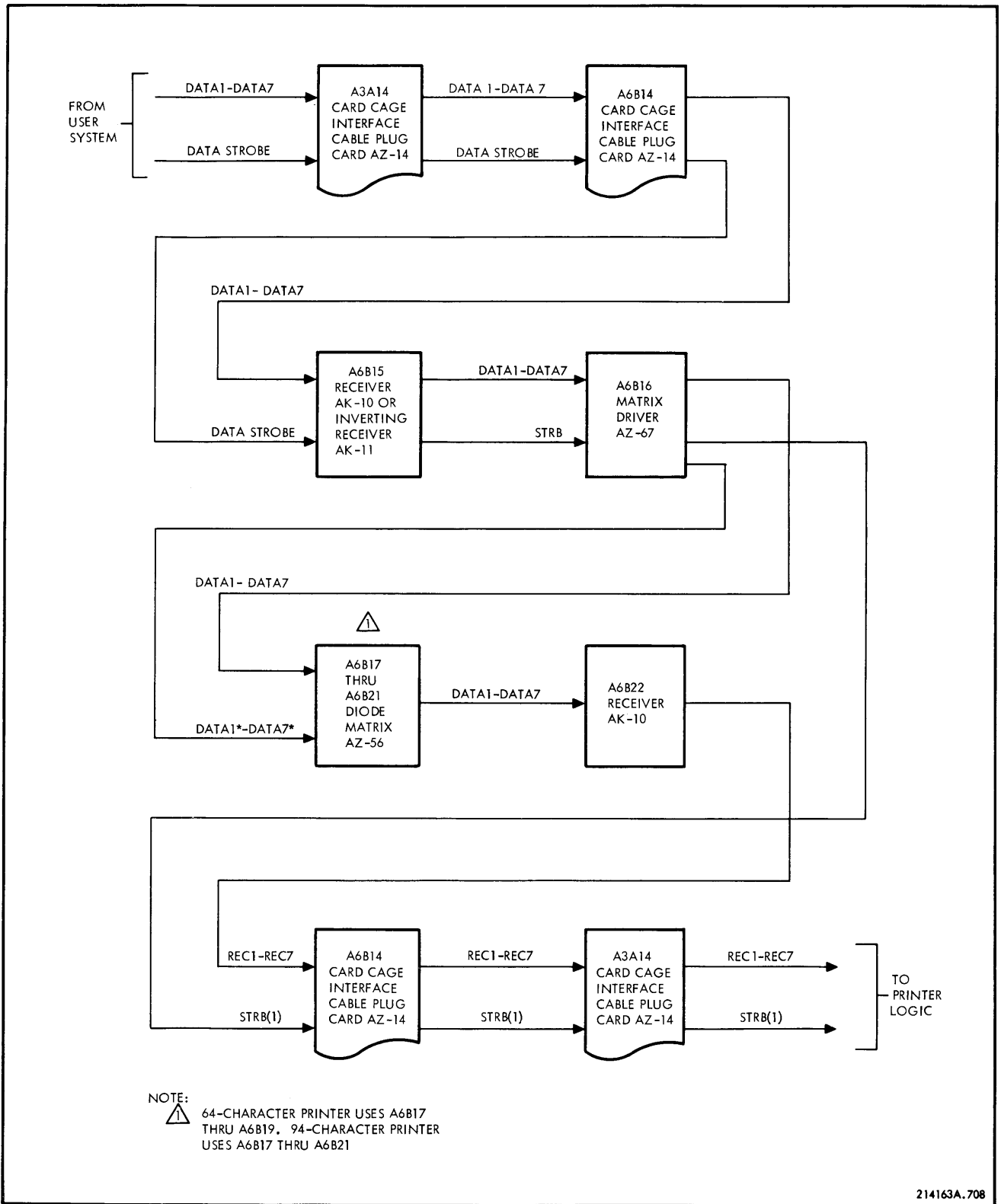


Figure 7-8. Code Conversion Option Block Diagram

DPC 214163B

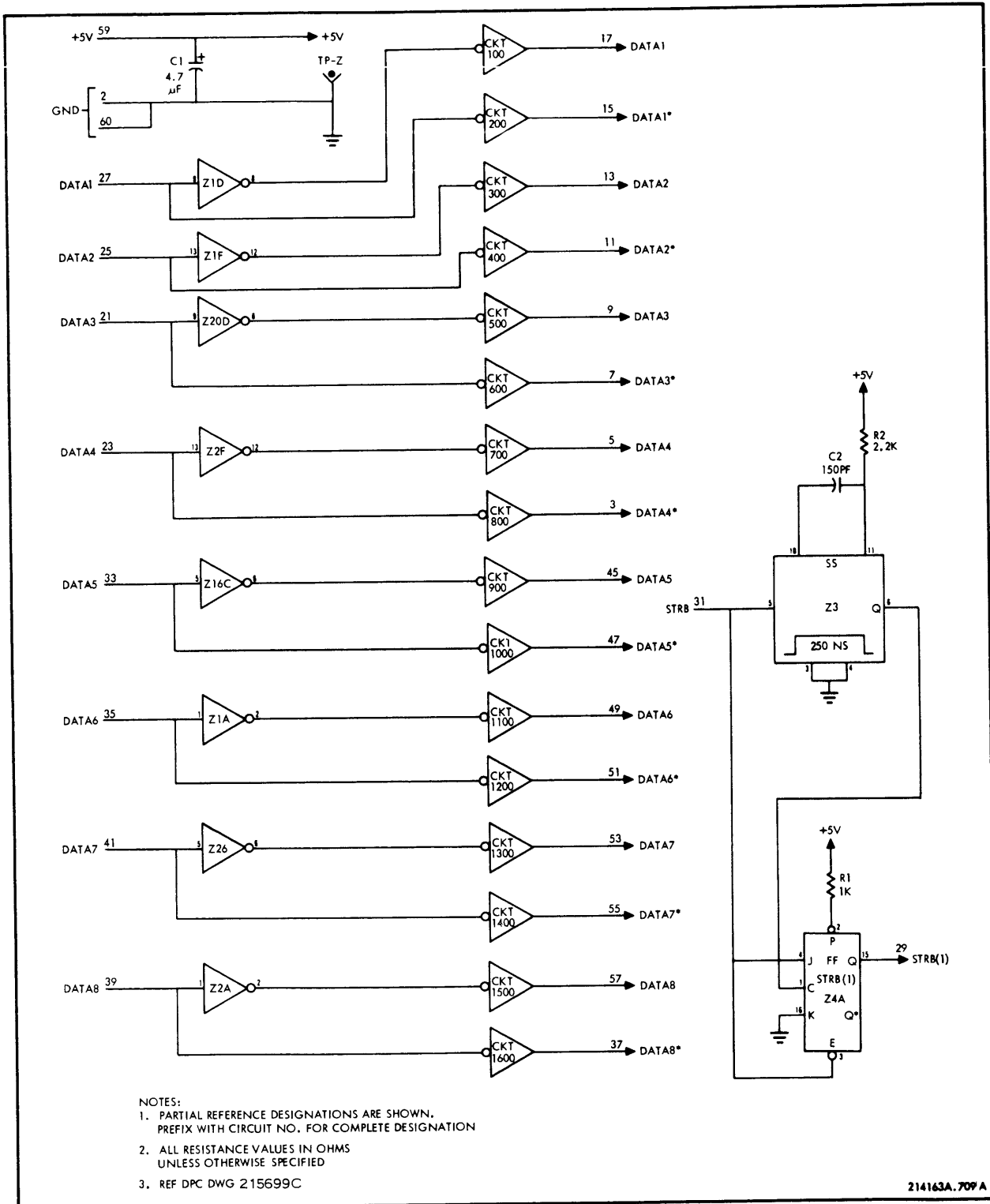


Figure 7-9. Matrix Driver AZ-67 Logic Diagram (Sheet 1 of 2)

DPC 214163B

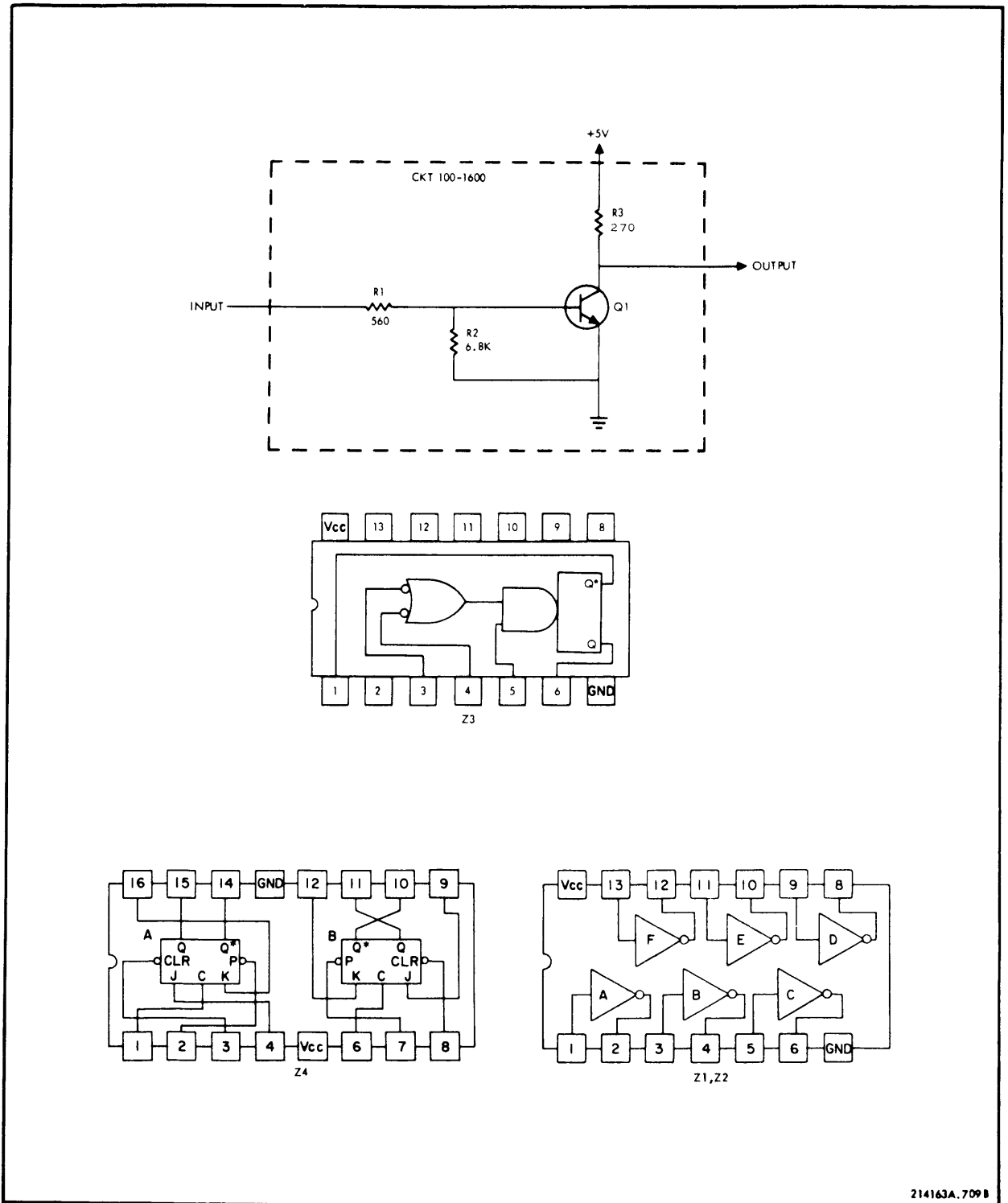


Figure 7-9. Matrix Driver AZ-67 Logic Diagram (Sheet 2 of 2)

7-67 Signal STRB is applied to single-shot Z3 and the clear and set inputs of flip-flop Z4A (STRB(1)). STRB is low at this time and flip-flop STRB(1) is held in the clear state. When the user raises DATA STROBE, STRB goes high and triggers single-shot Z3. Output Z3Q goes high for 250 nanoseconds. At the end of that period, Z3Q goes low and flip-flop STRB(1) is clocked and set. Output STRB(1) goes high and is applied to the printer logic. When DATA STROBE drops, STRB goes low and flip-flop STRB(1) is again cleared until the next DATA STROBE.

7-68 The decoding matrix consists of three diode matrix AZ-56 cards for a 64-character printer, or five matrix cards for a 96-character printer. The matrix cards are connected in parallel to the outputs of the matrix driver. The outputs of the matrix cards are connected in parallel to receiver A6B22 (AK-10).

7-69 Diode matrix AZ-56 contains a printed circuit grid pattern consisting of 23 lines horizontally and 23 lines vertically. The horizontal lines are pulled up to +5v through resistors R1 thru R23. Vertical lines 1 thru 16 are input lines from the matrix driver, and lines 17 thru 23 are output lines to the receiver. The output lines are pulled down to -12v through external resistors.

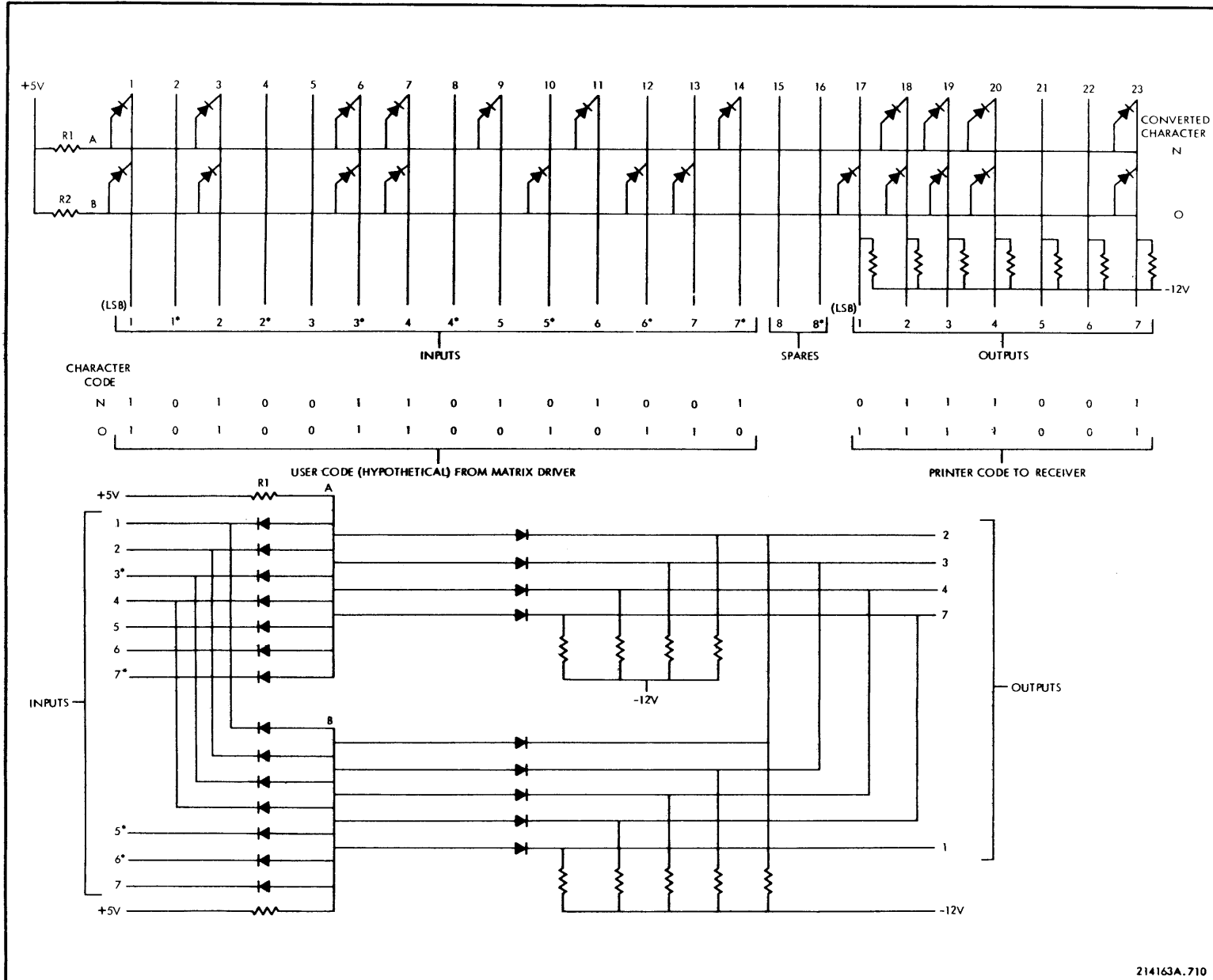
7-70 Each printable character and the three control characters are represented by a horizontal line. Three matrix cards provide 67 character lines for a 64-character system, and five cards provide 99 character lines for a 96-character system. The incoming user code and the outgoing printer code appear on the vertical lines, and the code is determined by the location of diodes connected between the horizontal and vertical lines. A hypothetical matrix and a schematic representation are shown in figure 7-10 for characters N and O. Other characters would be similarly mechanized.

7-71 Assuming a hypothetical user code for the letter N, the transmitted code on the data lines is as follows:

DATA1 = 1 (LSB)  
 DATA2 = 1  
 DATA3 = 0  
 DATA4 = 1  
 DATA5 = 1  
 DATA6 = 1  
 DATA7 = 0

7-72 The received data is fed to the matrix driver whose outputs can be considered as DATA and DATA\* signals. The user code appears on inputs 1 thru 7 of the matrix and its inverse appears on inputs 1\* thru 7\*. If a data line is high (1), a diode is connected between the applicable input and character lines. If it is low (0) the diode is connected between the applicable inverse input and character lines.

Figure 7-10. Example of Decode Matrix Mechanization



7-73 Outputs 1 thru 7 of the matrix are applied through the receiver to the printer logic. The printer character code for N is as follows:

REC1 = 0  
REC2 = 1  
REC3 = 1  
REC4 = 1  
REC5 = 0  
REC6 = 0  
REC7 = 1

7-74 If a REC line is high (1), a diode is connected between the applicable output and character lines. The absence of a diode indicates the output line is low.

7-75 If the user code for N is transmitted correctly, input lines 1, 2, 3\*, 4, 5, 6, and 7\* go high, and the diodes are reverse biased. The matrix performs an AND function and outputs 2, 3, 4, and 7 go high while 1, 5, and 6 stay low. The printer logic then stores the character code for N in memory.

7-76 If the user code for N is transmitted incorrectly, and the result is not a printable or control code, then a space code will be stored in memory by the printer logic.

#### 7-77 SELF-TEST

7-78 The self-test option enables the printer to be exercised during checkout and maintenance, independently of the user system. The self-test circuitry is contained on printed circuit card AL-27 which replaces input/output cable plug card AZ-14 during checkout and maintenance.

#### 7-79 SELF-TEST PROCEDURE

7-80 To self-test printer, proceed as follows:

- a. Open printer cabinet rear door; unlatch and swing card cage A3 out to 90° position.



Operation of self-test card with logic 1 levels above +5v will result in damage to card. For these systems only perform steps b and c prior to installing self-test card. Refer to calibration, section V, for an applicable adjustment procedure. Proceed to step d for logic 1 levels of +5v or less.



DPC 214163A

- b. Set driver A3A11 reference voltage at +4 to +4.5v.
- c. Set receiver A3A14 reference voltage to +2v.
- d. Open printer cabinet front door; set circuit breaker CB1 to OFF.
- e. Remove input/output cable plug card AZ-14 from card cage A3, location 25.

Note

Perform steps f and g for negative logic systems only. Proceed to step h for positive logic systems.

- f. Insert negative logic self-test adapter board (figure 7-11, part no. 216495) into location 25.
- g. Insert self-test AL-27 card (switch S1 at top), into self-test adapter board (figure 7-12).
- h. Insert self-test AL-27 card into location 25 (figure 7-13).
- i. Set AL-27 switches S1 thru S4 to down position.
- j. Set circuit breaker CB1 to ON.
- k. Refer to table 7-4 for switch functions.
- l. On completion of checkout or maintenance, set circuit breaker CB1 to OFF.
- m. Remove self-test card(s); replace cable plug card.

Note

On completion of checkout or maintenance, perform steps n and o only if steps b and c were previously performed.

- n. Set circuit breaker CB1 to ON.
- o. Set driver A3A11 and receiver A314 reference voltages to original levels.
- p. Close and latch card cage A3; close cabinet rear door.

DPC 214163A

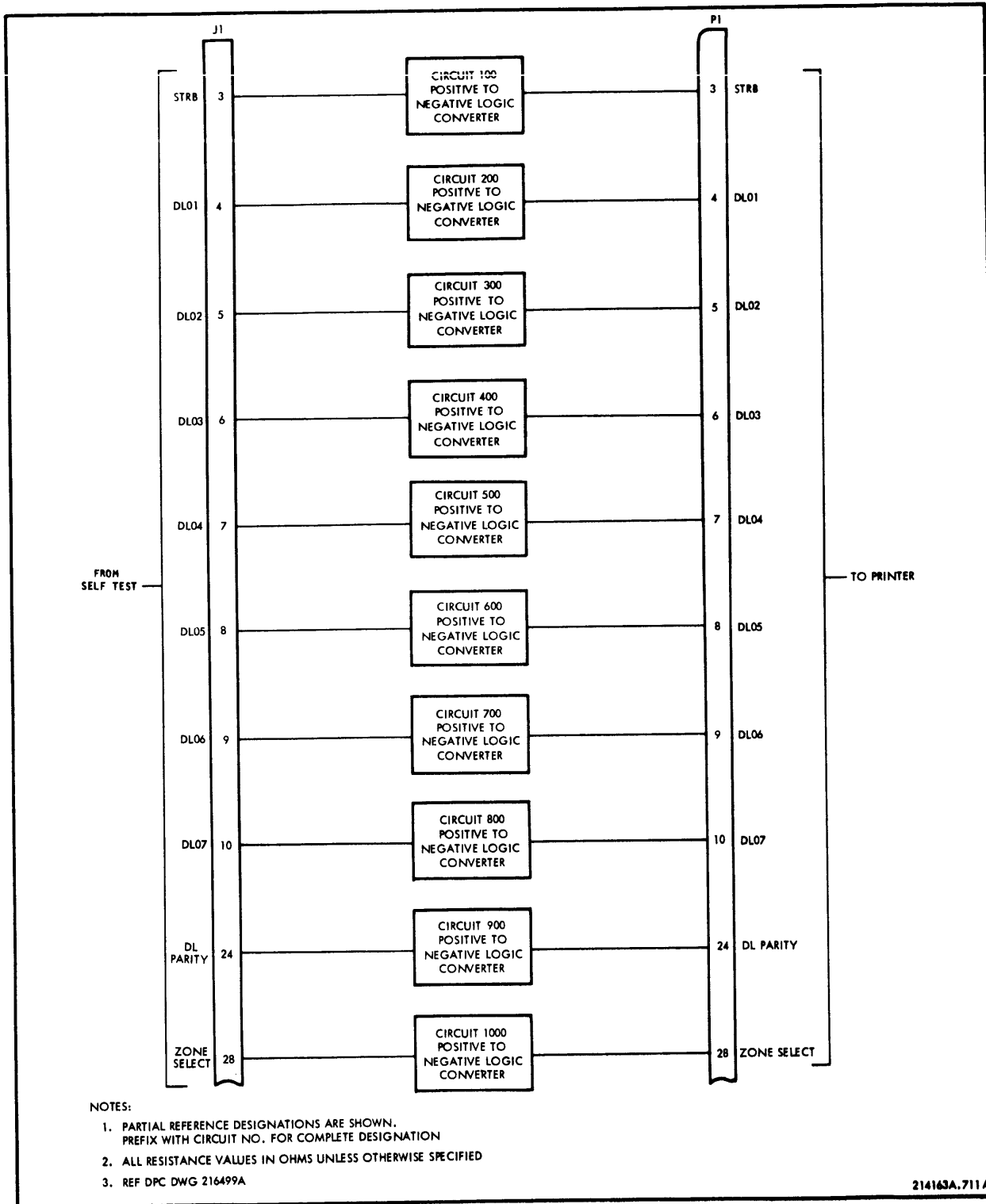
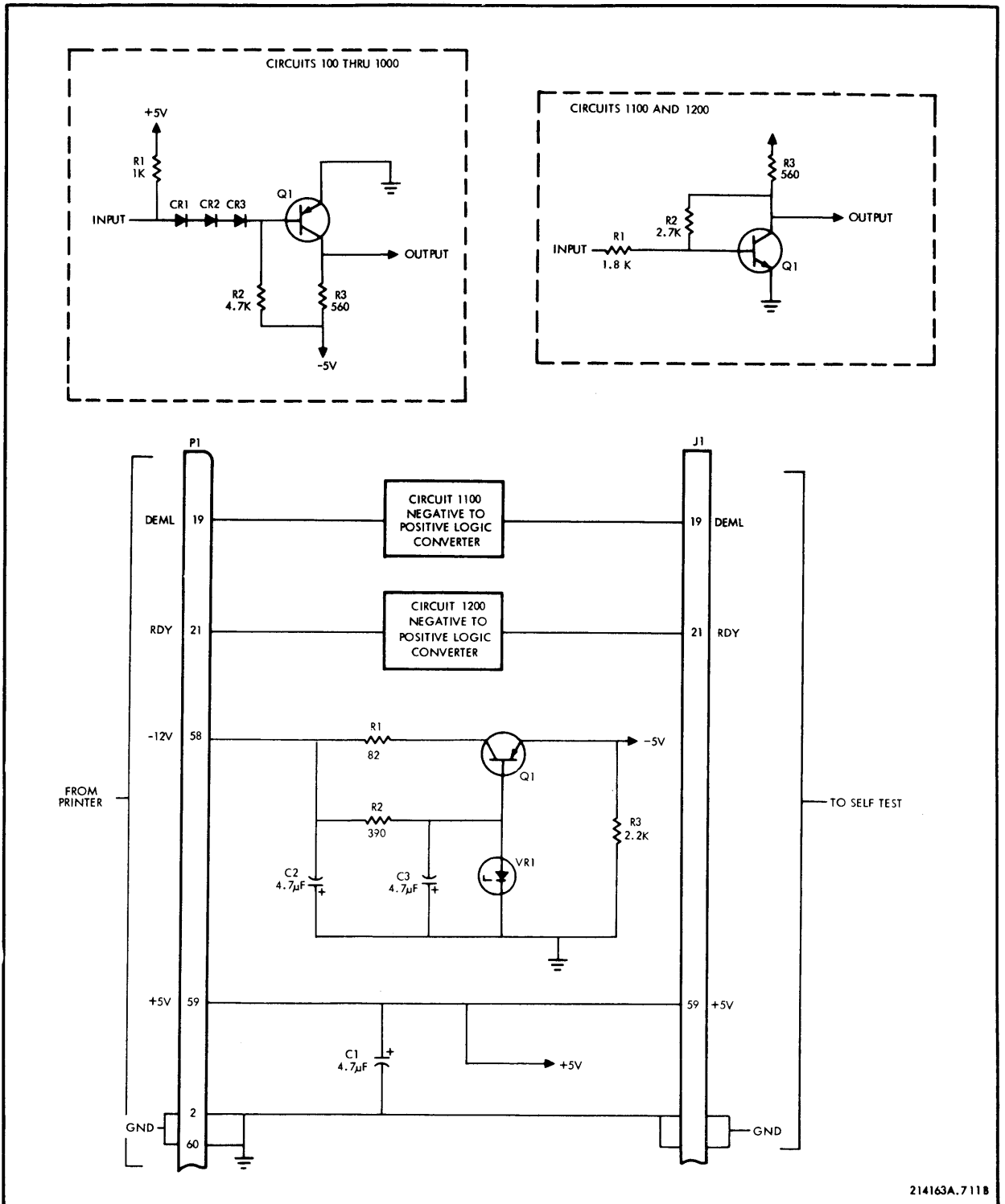


Figure 7-11. Negative Logic Self-Test Adapter Schematic Diagram (Sheet 1 of 2)



214163A.7118

Figure 7-11. Negative Logic Self-Test Adapter Schematic Diagram (Sheet 2 of 2)

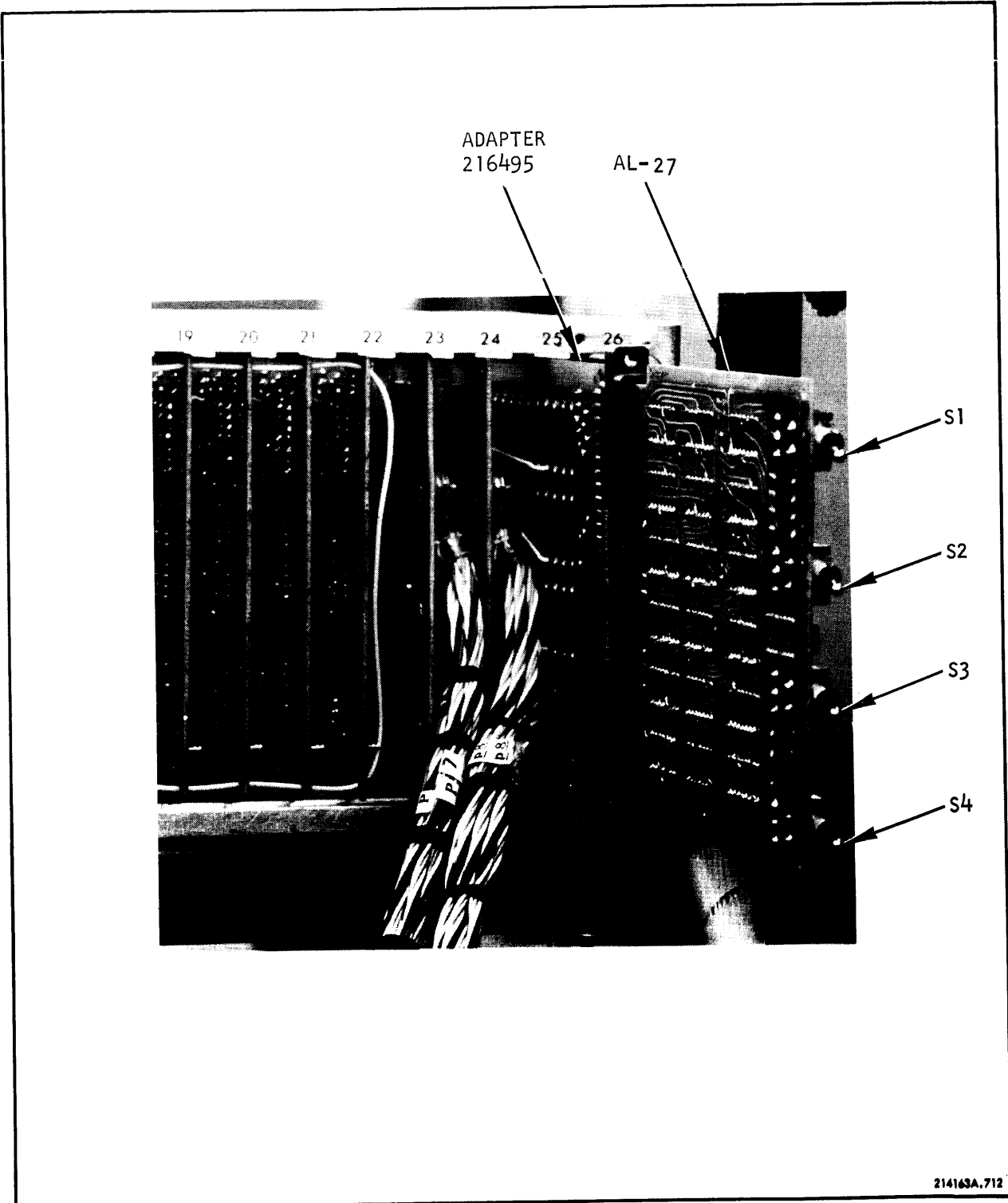


Figure 7-12. Self-Test AL-27 Card Installed (Negative Logic)

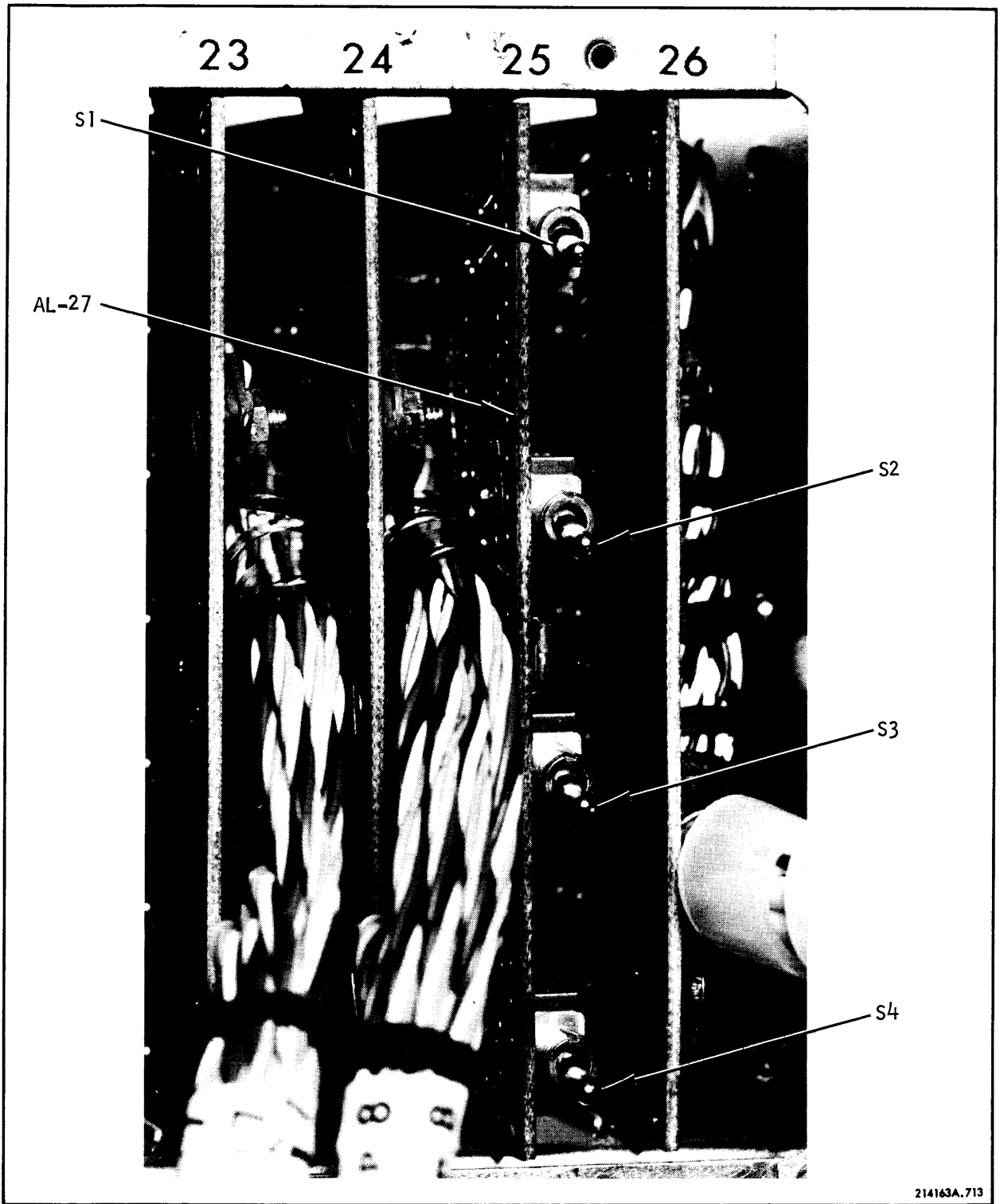


Figure 7-13. Self-Test AL-27 Card Installed (Positive Logic)

Table 7-4. Self-Test AL-27 Switch Functions

Switch Combinations	Position	Printout
S1 S2	Down Down	Columns 1 thru 19
S1 S2	Up Down	Columns 1 thru 39
S1 S2	Down Up	Columns 1 thru 59
S1 S2	Up Up	Columns 1 thru 80
S3	Up	E only
S3	Down	Shifting Pattern
S4*	Down	Normal
S4*	Up	Zone 4 first
*Switch S4 used with zone select option only.		

## 7-81 SELF-TEST OPERATION (Figure 7-14)

7-82 Card AL-27 contains a line length counter, character generator, parity generator, associated logic, and switches S1 thru S4. Switches S1 thru S4 enable the user to select an E or a shifting pattern, print one to four zones, and check the operation of the zone select option. The parity generator provides the parity bit for use with the parity check option.

7-83 Zone 1 - Shifting Pattern

7-84 Switches S1 and S2 determine the number of zones to be printed by selecting the character line length. Switch S3 selects an E or shifting pattern. For a shifting pattern in zone 1 only, the three switches are placed in the down position to generate continuously 19 printable characters and a PF command.

7-85 When the printer is operationally ready, RDY goes high and remains high for the duration of the operation. With switches S1 and S2 down, the output of NOR gate Z2A goes high and is applied to NAND gates Z5C and Z5B. Each time the printer raises DEMI, the output of NAND gate Z3C goes low, is applied to the clear input of flip-flop Z17B, and inverter Z9D. Signal STRB and the clock input to the 7-bit character generator go high.

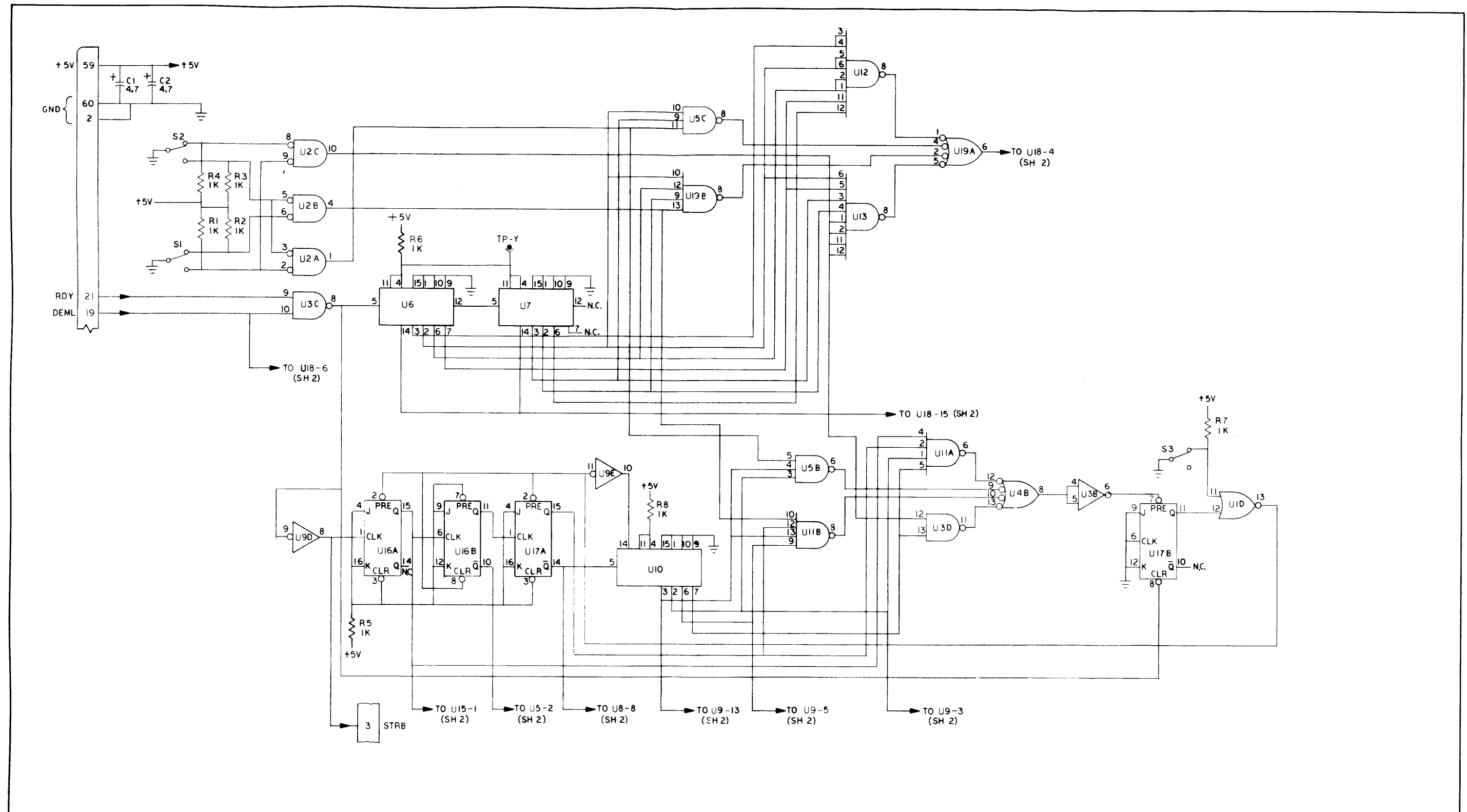
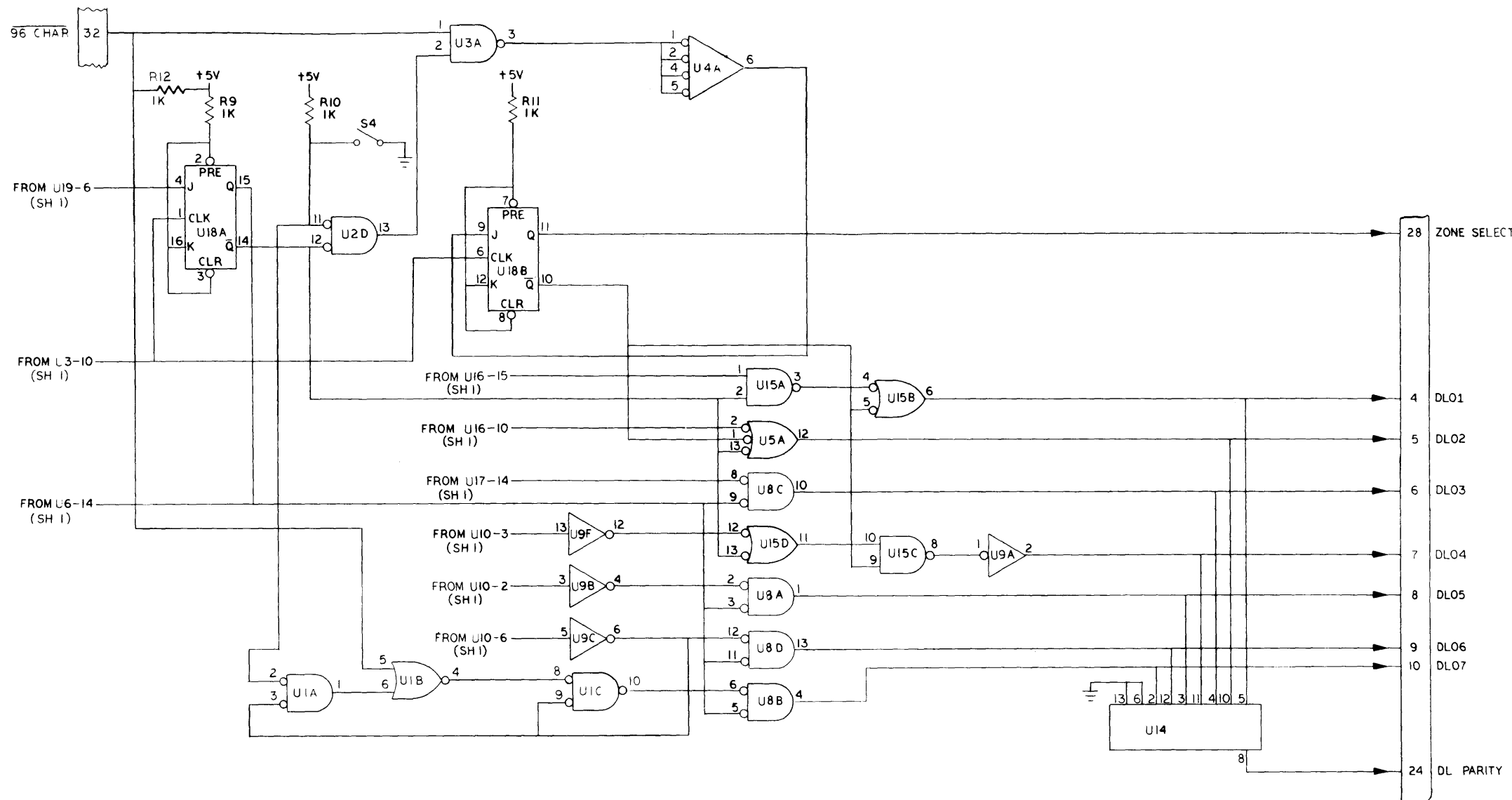


Figure 7-14

<b>data products</b> <small>WOODLAND HILLS, CALIFORNIA</small>			
TITLE SCHEMATIC, AL-32 SELF TEST			
SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	19790	230244	A
SCALE	SHEET 1 OF 2		
NONE			



- 28 ZONE SELECT
- 4 DL01
- 5 DL02
- 6 DL03
- 7 DL04
- 8 DL05
- 9 DL06
- 10 DL07
- 24 DL PARITY

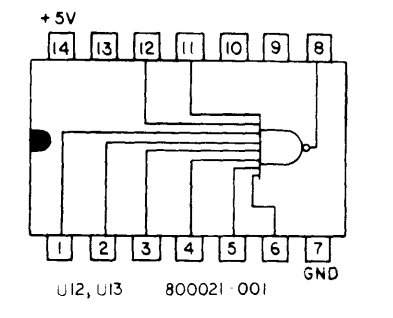
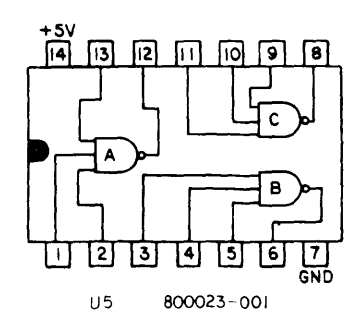
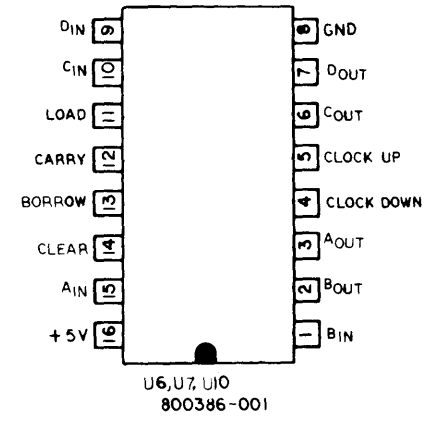
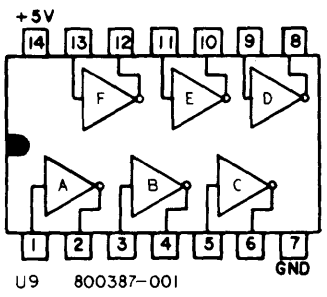
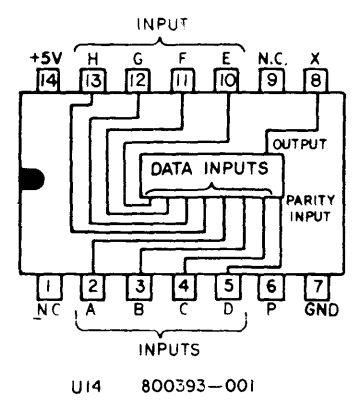
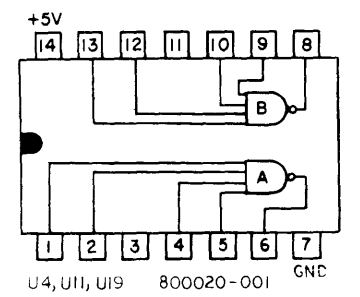
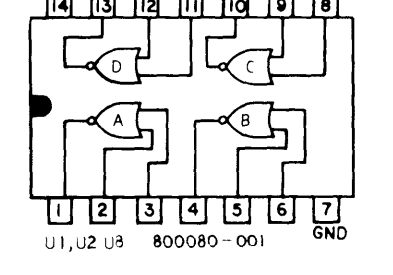
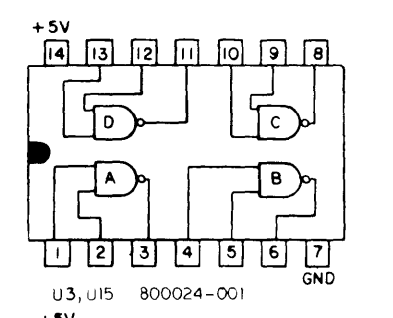
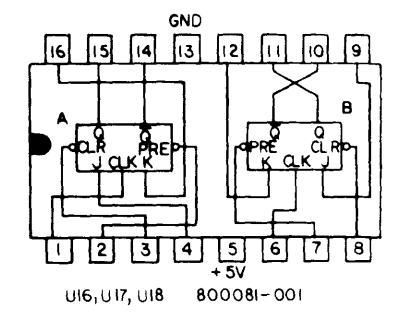


Figure 7-14a

<b>data products</b> WOODLAND HILLS, CALIFORNIA			
TITLE SCHEMATIC, AL-32 SELF TEST			
SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	19790	230244	A
SCALE	NONE		SHEET 2 OF 2



7-86 The character generator consists of flip-flops Z16A (LSB), Z16B, Z17A, and up/down counter Z10. The 7-bit code for each character is derived from bits 1 thru 6 of the generator. Bit 6 is inverted to also provide bit 7 of the character code. The generator output is applied to the data lines through NAND gates Z15A and Z5A, NOR gates Z8C and Z8B, inverters Z9F, Z9B, and Z9C and associated logic. Each time STRB goes high, the character present in the generator output is strobed into the printer data register.

7-87 Each time DEML goes low, the generator and the line length counter are incremented one count. The counter consists of up/down counters Z6 and Z7, and maintains a count of the generated characters. Since neither the generator or the counter is initialized at the start of the operation, the start count is random and the first line in the printout may contain less than 19 characters. The shifting pattern may also be unorganized for one or two lines. The generator start count for the shifting pattern is 05, which appears on the data lines as the character code for E (69). The following description assumes an ideal situation in which the operation begins with the counter at zero, and the generator preset to 05. The first character in the line will be E (1, figure 7-15), and the code appears on the generator output and the data lines as follows:

<u>Generator Output</u>	<u>Data Lines</u>
B1 = 1 (LSB)	DL01 = 1 (LSB)
B2 = 0	DL02 = 0
B3 = 1	DL03 = 1
B4 = 0	DL04 = 0
B5 = 0	DL05 = 0
B6 = 0	DL06 = 0
B7 = 0	DL07 = 1

7-88 When the counter reaches 18, gate Z5C is enabled and the output of NAND gate Z19A goes high and is applied to the set input of flip-flop Z18A. On the 19th count the character code for W is strobed into the printer data register, the generator increments to count 24, and flip-flop Z18A is clocked and set. Output Z18AQ goes high, clears the line length counter, and is also applied to NOR gates Z8A thru Z8D. Output Z18AQ\* goes low and is applied to NOR gate Z2D and NAND gates Z5A, Z15A, and Z15D. With switch S4 down, gate Z2D remains low and flip-flop Z18B stays reset. The outputs of gates Z15A, Z5A, and Z15D go high. The outputs of gates Z8A thru Z8D go low, and the PF command code appears on the data lines as follows:

DL01 = 0 (LSB)  
 DL02 = 1  
 DL03 = 0  
 DL04 = 1  
 DL05 = 0  
 DL06 = 0  
 DL07 = 0

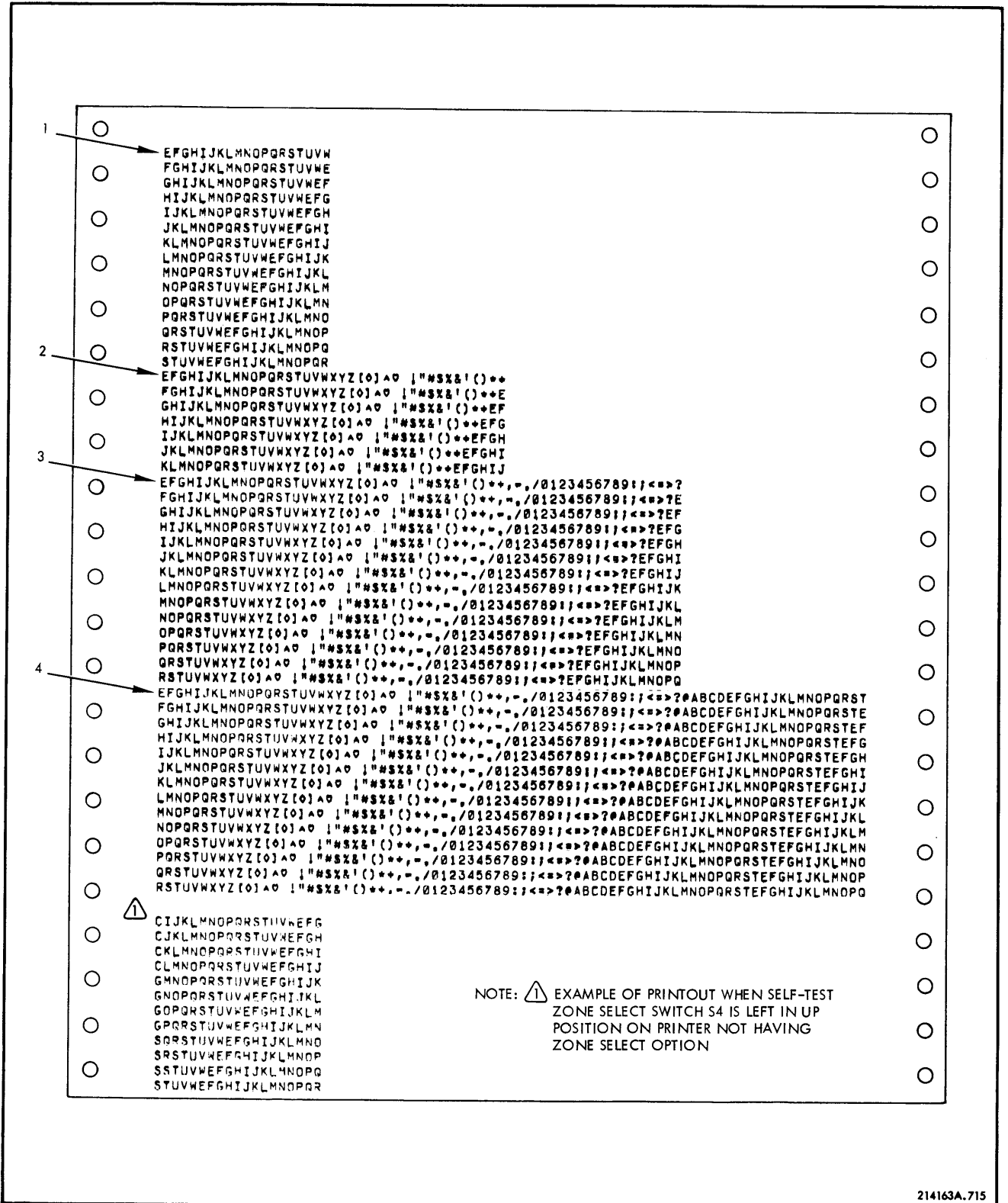


Figure 7-15. Shifting Pattern Printout (Zones 1 Thru 4)

7-89 When the generator reaches 24, gate Z5B is enabled, presetting flip-flop Z17B. Output Z17BQ goes high, enabling NOR gate Z1D. Flip-flops Z16A and Z17A are preset, and flip-flop Z16B and counter Z10 are cleared. Thus the generator is preset to count 05, and the character code for E (69). On the following DEML, the PF command is strobed into the printer data register, flip-flop Z18A resets, and the generator is incremented to the code for F (70).

7-90 On the first DEML after printer execution of the PF command, F is strobed into the printer data register, and the counter and generator are incremented one count. Thus the first character in the next line is F, and the operation described in the preceding paragraphs repeats continuously. Each time it does, the first character in each line is shifted sequentially one character (figure 7-15).

#### 7-91 Zones 1 and 2 - Shifting Pattern

7-92 With switch S1 up and switch S2 down, 39 printable characters and a PF command are continuously generated.

7-93 The output of NOR gate Z2B goes high and is applied to NAND gates Z19B and Z11B. When the counter reaches 38, gate Z19B is enabled and the set input to flip-flop Z18A goes high. Assuming that the generator count starts at E (2, figure 7-15), on the 39th count the character code for + is strobed into the printer data register and flip-flop Z18A is clocked and set. The generator increments to count 44, enables gate Z11B, and flip-flop Z17B is preset. Thus the counter is cleared, the generator preset to E and a PF command generated. The operation then continues as described for zone 1.

#### 7-94 Zones 1 Thru 3 - Shifting Pattern

7-95 With switch S1 down and switch S2 up, 59 printable characters and a PF command are continuously generated.

7-96 The output of NOR gate Z2C goes high and is applied to NAND gates Z13 and Z3D. When the counter reaches 58, gate Z13 is enabled and the set input to flip-flop Z18A goes high. Assuming that the generator count starts at E (3, figure 7-15), on the 59th count the character code for ? is strobed into the printer data register and flip-flop Z18A is clocked and set. The generator increments to count 64, enables gate Z3D, and flip-flop Z17B is preset. Thus the counter is cleared, the generator preset to E, and a PF command generated. The operation then continues as described for zone 1.

#### 7-97 Zones 1 Thru 4 - Shifting Pattern

7-98 With switches S1 and S2 up, 80 printable characters and a PF command are continuously generated.

7-99 When the counter reaches 79, NAND gate Z12B is enabled and the set input to flip-flop Z18A goes high. Assuming that the generator count starts at E (4, figure 7-15), on the 80th count the character code for T is strobed into the printer data register and flip-flop Z18A is clocked and set. The generator increments to count 85, enables gate Z11A, and flip-flop Z17B is preset. Thus the

counter is cleared, the generator preset to E, and a PF command generated. The operation then continues as described for zone 1.

#### 7-100 E Pattern

7-101 Switch S3 determines if the printout is to be an E or shifting pattern. Placing switch S3 up enables NOR gate Z1D and presets the generator to 69 (E). The generator is held at this count as long as switch S3 remains up, and only the code for E is generated. The operation is otherwise the same as described for the shifting pattern.

#### 7-102 Zone Select

7-103 Switch S4 is placed in the up position when the printer contains the zone select option. The operation is as previously described, but with switch S4 up, the output of NOR gate Z2D goes high when flip-flop Z18A sets. On the following DEML, the PF command is strobed into the printer data register, flip-flop Z18A resets, flip-flop Z18B sets, and ZONE SELECT is raised. Output Z18Q\* goes low, is applied to NAND gates Z5A and Z15B, and data lines DL01 and DL02 go high. On the first DEML after printer execution of the PF command, the zone 4 code is strobed into the zone select logic, and flip-flop Z18B resets. Assuming the line length selected is for one zone, the next and subsequent lines appear in zone 4 on the printout as each PF command is followed by ZONE SELECT. As zones are added, zone 4 prints first, then zones 1 through 3.

#### 7-104 Parity Generator

7-104A The parity generator provides the odd parity bit for use with the parity check option.

#### 7-105 96-CHARACTER PRINTER TEST

7-105A Implementation of the 96-character test is automatic with a 96-character printer. The 96-character modification kit adds the ground to pin 32 of the AL-32 card. This disables AL-32 gate U3A thus altering the character sequence to include additional 32 characters. All other functions of the self-test card are unchanged.

#### 7-106 CHARACTER FONTS

7-107 A variety of font and character sets will be supplied on request.

#### 7-108 96-CHARACTER SET

7-109 A larger character drum with a 96-character set is available as an option. Table 7-5 shows those printer performance characteristics that apply to the 96-character drum.

Table 7-5. Printer Performance Characteristics (with 96-Character Drum)

Item	Specification
Printable characters	
Number	96 (95 characters and space)
Type	ASCII open Gothic print
Size	Typically 0.095 inches high and 0.065 inches wide

Table 7-5. Printer Performance Characteristics  
(With 96-Character Drum) (Continued)

Item	Specification
Characters per line	80 (maximum)
Character drum	
Characters	96
Speed	1170 rpm
Print rate	
96-character drum	253 Lines per minute - 80 columns (4 zones)
	330 Lines per minute - 60 columns (3 zones)
	478 Lines per minute - 40 columns (2 zones)
	843 Lines per minute - 20 columns (1 zone)

#### 7-110 Coded Character Set

7-111 A 7-bit code is used to transmit information to the printer on data lines DATA1 thru DATA7. The code is derived from a modified version of the American Standard Code for Information Interchange (ASCII). Table 7-6 shows the allowable printable character codes, and the three format control character codes. Non-printable combinations received by the printer result in a space.

#### 7-112 NONPRINTABLE CODE DETECTOR

7-113 The nonprintable code detector is located on card Logic Gate 1 AG-17 (figure 6-7). For the 96-character drum option input DR07 is grounded and the equation for LEGAL is as follows:

$$\text{LEGAL} = \text{DR06} + \text{DR07}$$

Figure 7-16 shows the schematic change for card AG-17 (A2).

#### 7-114 STATIC ELIMINATOR

7-115 The static eliminator option improves printer paper handling in areas of extremely low humidity.

#### 7-116 STATIC ELIMINATOR INSTALLATION

7-117 The static eliminator transformer, wand, and cable shield should be grounded securely to the printer frame, and the cable connections securely fastened, to ensure proper operation of the printer.

Table 7-6. Coded Character Set (Standard 96-Character Set)

b7 b6 b5	0 0 0	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4 b3 b2 b1							
0 0 0 0		Space	Ø	@	P	↖	p
0 0 0 1		!	1	A	Q	a	q
0 0 1 0		"	2	B	R	b	r
0 0 1 1		#	3	C	S	c	s
0 1 0 0		\$	4	D	T	d	t
0 1 0 1		%	5	E	U	e	u
0 1 1 0		&	6	F	V	f	v
0 1 1 1		'	7	G	W	g	w
1 0 0 0		(	8	H	X	h	x
1 0 0 1		)	9	I	Y	i	y
1 0 1 0	PF	*	:	J	Z	j	z
1 0 1 1	FF	+	;	K	[	k	[
1 1 0 0	CR	,	<	L	◇	l	]
1 1 0 1		-	=	M	]	m	]
1 1 1 0		.	>	N	^	n	
1 1 1 1		/	?	O	♥	o	■

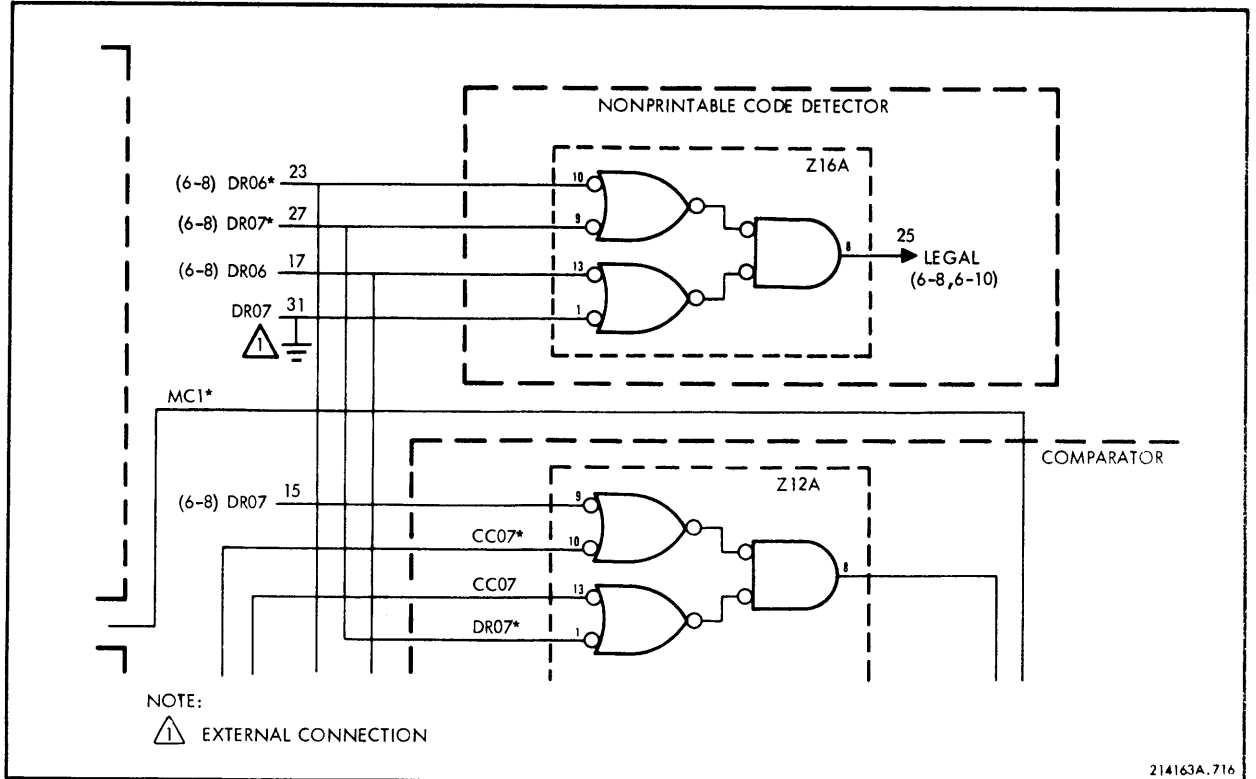


Figure 7-16. Portion of Logic Gate 1 AG-17 Schematic Diagram

7-118 Ground and Cable Check

7-119 Perform the following procedure as part of the normal inspection and preventive maintenance procedure (section V):

Note

Perform steps a thru h for printer serial numbers 001 thru 200. Proceed to step i for printer serial number 201 and up.

- a. Open printer cabinet front door; set circuit breaker CB1 to OFF.
- b. Open printer cabinet rear door; unlatch and swing card cage A3 out to 90° position.
- c. Set VOM (Triplett 630-A or equivalent) to X1 ohms.
- d. Check continuity between metal sleeve of wand (1, figure 7-17) and frame ground lug (5, figure 7-17).
- e. Check continuity between cable shield (3, figure 7-17) and frame ground lug.
- f. Remove transformer and wand cover plugs (2 and 4, figure 7-17).
- g. Check cable continuity by placing VOM probes into the wand and transformer cover plug receptacles, and firmly against cable connection points.
- h. On completion of step g, replace cover plugs.
- i. Check continuity between metal sleeve of wand (1, figure 7-18) and frame ground lug (3, figure 7-18).
- j. Check continuity between cable shield (2, figure 7-18) and frame ground lug.

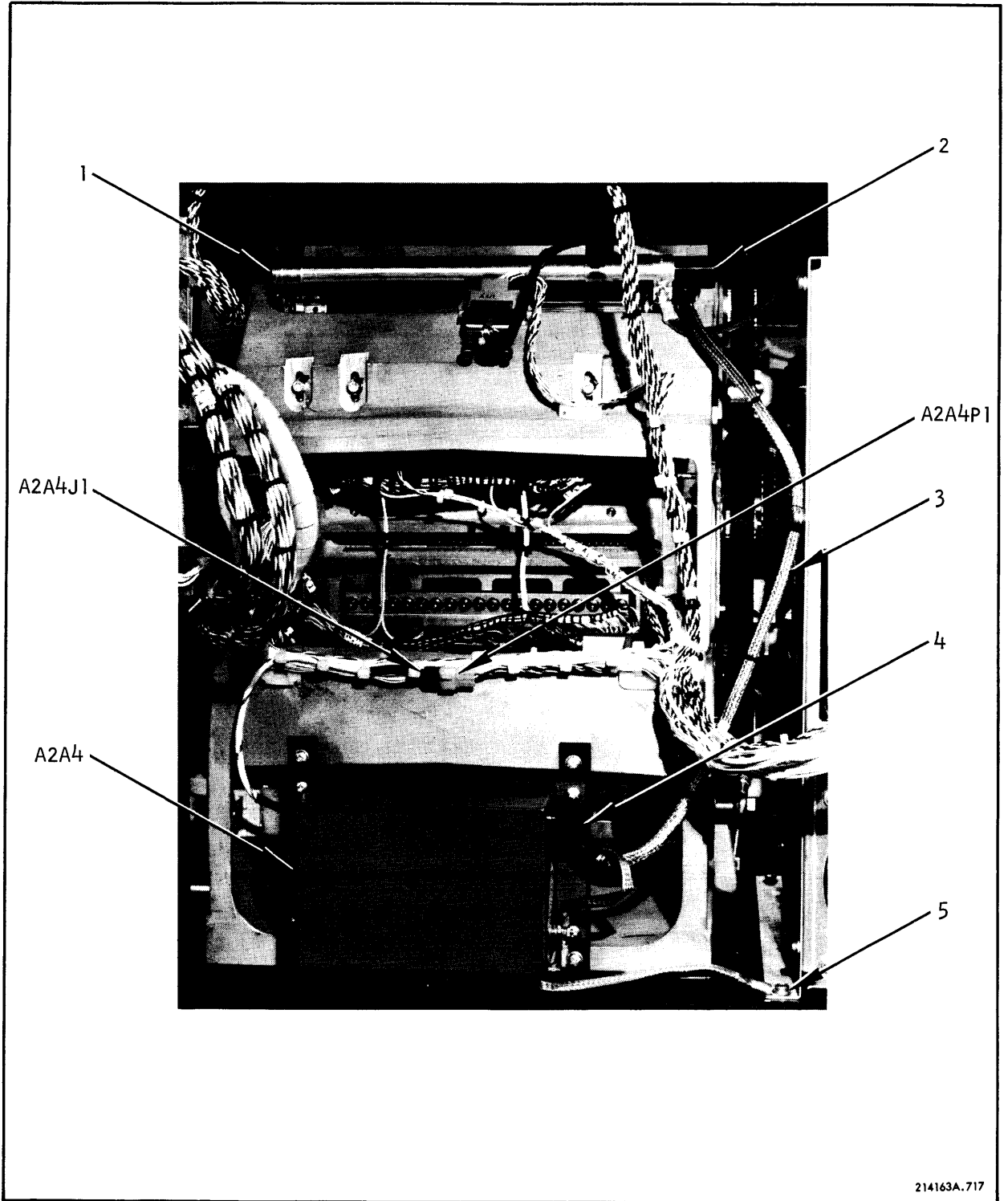


Figure 7-17. Static Eliminator Assembly Installed  
(Printer Serial Numbers 012 Thru 200)



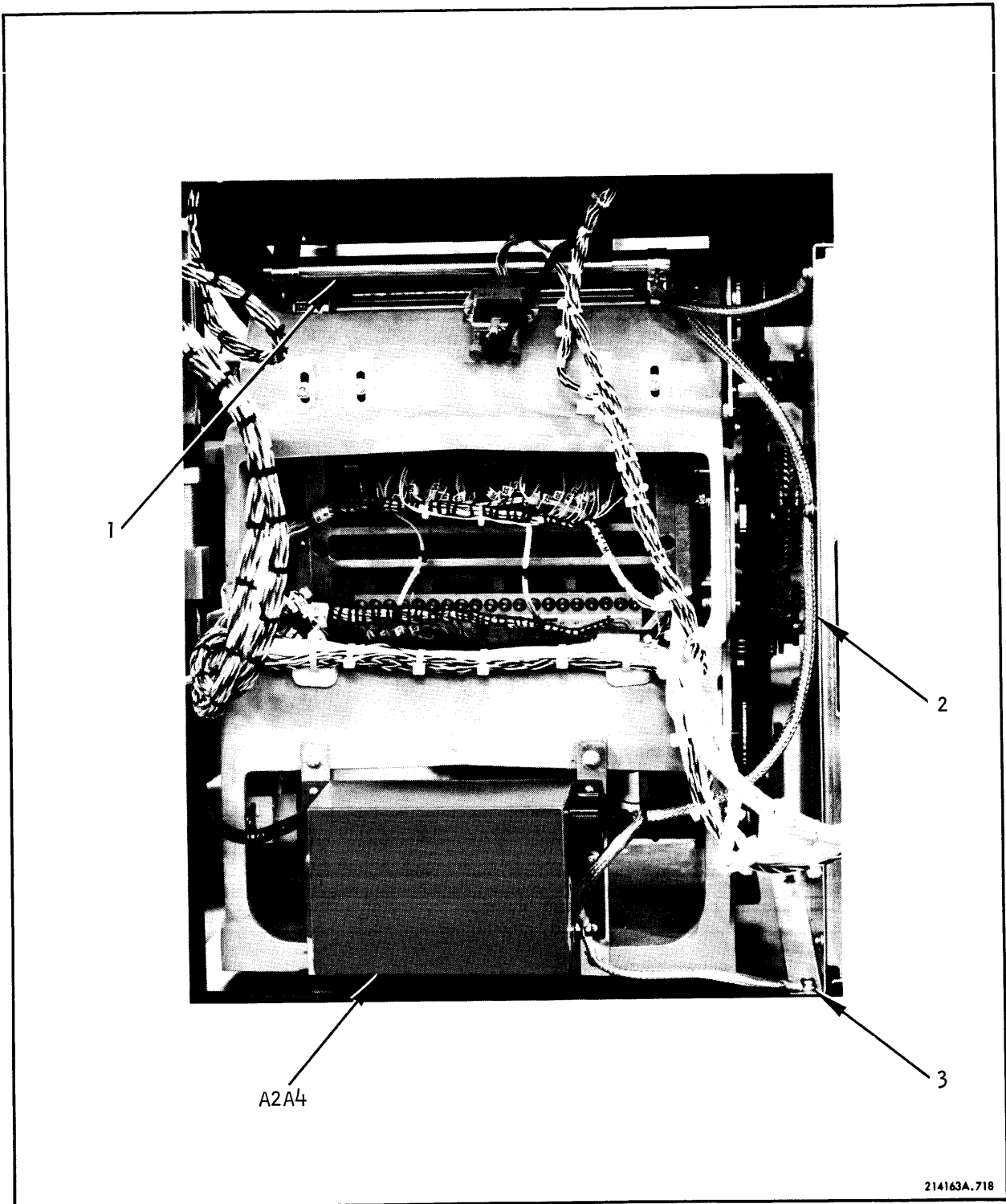


Figure 7-18. Static Eliminator Assembly Installed  
(Printer Serial Number 201 and Up)

7-120 PAPER RECEPTACLE

7-121 The paper receptacle (figure 7-19) mounts on the printer cabinet and collects the printer output.

7-122 PEDESTAL

7-123 A pedestal mount (figure 7-19) is available when desk mounting is not desired.

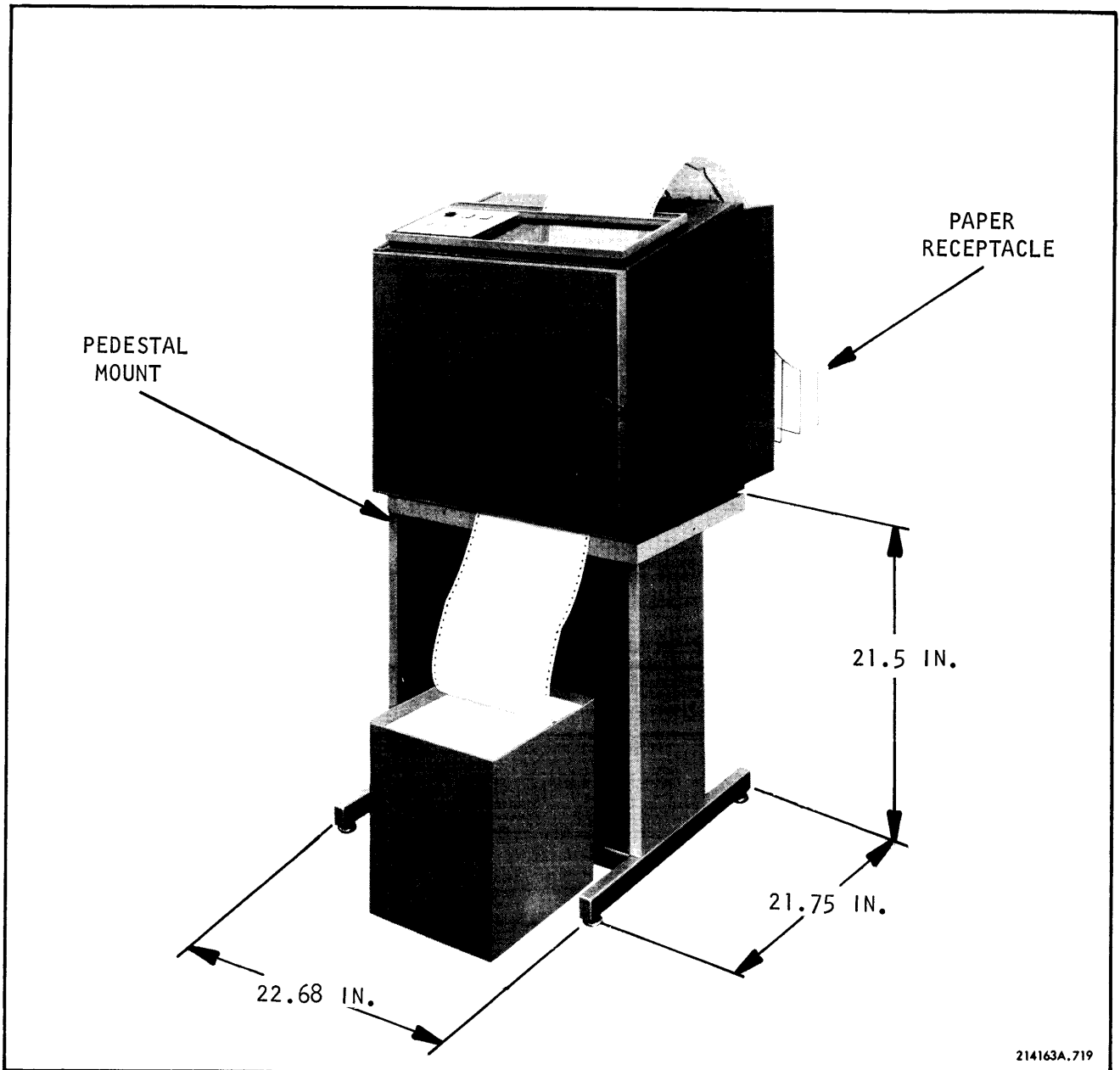


Figure 7-19. Model 2310 LINE/PRINTER Paper Receptacle and Pedestal Mount Installation

SECTION VIII

GLOSSARY

8-1 INTRODUCTION

8-2 This section contains a complete signal identification list and a glossary of signal terms and definitions.

8-3 SIGNAL IDENTIFICATION LIST

8-4 Table 8-1 provides a complete alphabetical listing of the signals in card cage A3 by connector and pin number. Column S gives the source or origination point for the signal fan-out.

Table 8-1. Signal Identification List (Card Cage A3)

Signal	Connector	Pin	S
-12VA	001	58	
	006	58	
	007	58	
	008	58	
	010	58	
	011	58	
	012	58	
	026	57	
-12VB	013	58	
	014	58	
	015	58	
	016	58	
	017	58	
	026	58	
+12	017	01	S
	017	03	

Signal	Connector	Pin	S
+28V	001	14	
	016	03	
	026	26	
	011	57	
	010	57	
+65V	017	52	S
	026	27	
CAM	004	57	
	009	29	
CAM*	004	25	S
	009	27	
CAMSW	009	30	S
	010	41	
	026	30	

Table 8-1. Signal Identification List (Card Cage A3) (Continued)

Signal	Connector	Pin	S
CAMSW*	009	31	S
	026	29	
CCSN	002	05	S
	005	35	
	006	16	
	009	50	
CHCK*	002	06	S
	015	16	
CHCK1	015	37	S
	018	13	
	019	13	
CHCK2	015	41	S
	020	13	
	021	13	
CHCK3	015	42	S
	022	13	
CHCK4	002	09	S
	015	39	
	009	20	
CHPO	015	28	S
	026	39	
CHPOR	015	30	S
	026	40	
CIND	002	03	S
	009	19	
	010	21	
	015	52	
COMP	015	46	S
	018	45	
	003	13	

Signal	Connector	Pin	S
COMP*	002	29	S
	013	13	
	015	47	
	018	36	
CONT	004	23	S
	008	08	
	008	40	
	007	21	
	005	25	
	009	21	
CONT*	004	48	S
	008	09	
	008	41	
	006	42	
	005	17	
CR00	003	55	S
	005	50	
	003	52	
CRRS1*	004	53	S
	005	56	
	003	54	
CR01	003	54	S
	005	47	
CR02	003	57	S
	005	52	
CR03	003	58	S
	005	53	
CR04	003	25	S
	005	51	
CR19	004	30	S
	005	58	
CR19*	003	50	S
	005	37	
	006	22	

Table 8-1. Signal Identification List (Card Cage A3) (Continued)

Signal	Connector	Pin	S
CR24*	003	56	S
	005	40	
DATASTR	014	56	S
	025	03	
DATA1	014	03	S
	025	04	
DATA2	014	11	S
	025	05	
DATA3	014	17	S
	025	06	
DATA4	014	25	S
	025	07	
DATA5	014	33	S
	025	08	
DATA6	014	41	S
	025	09	
DATA7	014	49	S
	025	10	
DCCF	002	21	S
	004	56	
DCCF*	002	19	S
	004	31	
DCRS*	004	19	S
	009	22	
DCTC*	002	11	S
	004	22	
DC04	002	41	S
	015	54	
DC05*	002	43	S
	015	44	
DEML	006	37	S
	011	41	

Signal	Connector	Pin	S
DGINT	016	25	S
	026	31	
DIBF*	003	35	S
	004	32	
	008	13	
	005	05	
DR01	009	25	S
	001	10	
	002	14	
DR01*	003	27	S
	002	12	
DR02	003	29	S
	001	09	
DR02*	002	49	S
	003	30	
	002	51	
DR03	003	32	S
	001	08	
DR03*	002	47	S
	003	26	
	002	45	
DR04	003	28	S
	001	07	
DR04*	002	42	S
	003	05	
	002	39	
DR05	003	03	S
	001	06	
DR05*	002	44	S
	003	08	
	002	37	
DR06	003	06	S
	001	05	
	002	17	
	003	21	S

Table 8-1. Signal Identification List (Card Cage A3) (Continued)

Signal	Connector	Pin	S
DR06*	002	23	S
	003	19	
DR07	001	04	S
	002	15	
	002	31	
	003	15	
DR07*	002	27	S
	003	17	
FAULT	006	57	S
	016	19	
FFCL	009	34	S
	015	12	
FFSw*	004	52	S
	005	09	
	009	33	
FF1	005	04	S
	026	05	
FF2	005	10	S
	026	06	
HDCL*	006	23	S
	015	33	
HDIC6	018	29	S
	019	45	
HDIC6*	018	20	S
	019	36	
HDIC7	019	29	S
	020	45	
HDIC7*	019	20	S
	020	36	
HDIC8	020	29	S
	021	45	
HDIC8*	020	20	S
	021	36	

Signal	Connector	Pin	S
HDIC9	021	29	S
	022	45	
HDIC9*	021	20	S
	022	36	
HDRS1*	009	58	S
	018	48	
HDRS2*	009	56	S
	019	48	
HDRS3*	009	52	S
	020	48	
HDRS4*	009	54	S
	021	48	
HDRS5*	009	47	S
	022	48	
HDSS	006	19	S
	017	06	
HDSS*	004	03	S
	006	25	
HDST	005	12	S
	013	30	
	015	13	
HDST1	015	19	S
	018	30	
HDST2	015	20	S
	019	30	
HDST3	015	35	S
	020	30	
HDST4	015	34	S
	021	30	
HDST5	015	15	S
	022	30	

Table 8-1. Signal Identification List (Card Cage A3) (Continued)

Signal	Connector	Pin	S
HDST6	003	48	S
	015	17	
HISW	016	23	S
	026	07	
HM01	022	05	S
	023	06	
HM02	022	21	S
	024	06	
HM03	022	35	S
	023	11	
HM04	022	51	S
	024	11	
HM05	021	05	S
	023	16	
HM06	021	21	S
	024	16	
HM07	021	35	S
	023	21	
HM08	021	51	S
	024	21	
HM09	020	05	S
	023	26	
HM10	020	21	S
	024	26	
HM11	020	35	S
	023	31	
HM12	020	51	S
	024	31	
HM13	019	05	S
	023	36	
HM14	019	21	S
	024	36	

Signal	Connector	Pin	S
HM15	019	35	S
	023	41	
HM16	019	51	S
	024	41	
HM17	018	05	S
	023	46	
HM18	018	21	S
	024	46	
HM19	018	35	S
	023	51	
HM20	018	51	S
	024	51	
HM21	022	08	S
	023	07	
HM22	022	24	S
	024	07	
HM23	022	38	S
	023	12	
HM24	022	54	S
	024	12	
HM25	021	08	S
	023	17	
HM26	021	24	S
	024	17	
HM27	021	38	S
	023	22	
HM28	021	54	S
	024	22	
HM29	020	08	S
	023	27	
HM30	020	24	S
	024	27	

Table 8-1. Signal Identification List (Card Cage A3) (Continued)

Signal	Connector	Pin	S
HM31	020	38	S
	023	32	
HM32	020	54	S
	024	32	
HM33	019	08	S
	023	37	
HM34	019	24	S
	024	37	
HM35	019	38	S
	023	42	
HM36	019	54	S
	024	42	
HM37	018	08	S
	023	47	
HM38	018	24	S
	024	47	
HM39	018	38	S
	023	52	
HM40	018	54	S
	024	52	
HM41	022	07	S
	023	08	
HM42	022	23	S
	024	08	
HM43	022	37	S
	023	13	
HM44	022	56	S
	024	13	
HM45	021	07	S
	023	18	
HM46	021	23	S
	024	18	

Signal	Connector	Pin	S
HM47	021	37	S
	023	23	
HM48	021	56	S
	024	23	
HM49	020	07	S
	023	28	
HM50	020	23	S
	024	28	
HM51	020	37	S
	023	33	
HM52	020	56	S
	024	33	
HM53	019	07	S
	023	38	
HM54	019	23	S
	024	38	
HM55	019	37	S
	023	43	
HM56	019	56	S
	024	43	
HM57	018	07	S
	023	48	
HM58	018	23	S
	024	48	
HM59	018	37	S
	023	53	
HM60	018	56	S
	024	53	
HM61	022	10	S
	023	09	
HM62	022	26	S
	024	09	



Table 8-1. Signal Identification List (Card Cage A3) (Continued)

Signal	Connector	Pin	S
HM63	022	42	S
	023	14	
HM64	022	58	S
	024	14	
HM65	021	10	S
	023	19	
HM66	021	26	S
	024	19	
HM67	021	42	S
	023	24	
HM68	021	58	S
	024	24	
HM69	020	10	S
	023	29	
HM70	020	26	S
	024	29	
HM71	020	42	S
	023	34	
HM72	020	58	S
	024	34	
HM73	019	10	S
	023	39	
HM74	019	26	S
	024	39	
HM75	019	42	S
	023	44	
HM76	019	58	S
	024	44	
HM77	018	10	S
	023	49	
HM78	018	26	S
	024	49	

Signal	Connector	Pin	S
HM79	018	42	S
	023	54	
HM80	018	58	S
	024	54	
HRTN1	022	06	S
	023	10	
HRTN10	020	22	S
	024	30	
HRTN11	020	33	S
	023	35	
HRTN12	020	50	S
	024	35	
HRTN13	019	06	S
	023	40	
HRTN14	019	22	S
	024	40	
HRTN15	019	33	S
	023	45	
HRTN16	019	50	S
	024	45	
HRTN17	018	06	S
	023	50	
HRTN18	018	22	S
	024	50	
HRTN19	018	33	S
	023	55	
HRTN2	022	22	S
	024	10	
HRTN20	018	50	S
	024	55	
HRTN3	022	33	S
	023	15	

Table 8-1. Signal Identification List (Card Cage A3) (Continued)

Signal	Connector	Pin	S
HRTN4	022	50	S
	024	15	
HRTN5	021	06	S
	023	20	
HRTN6	021	22	S
	024	20	
HRTN7	021	33	S
	023	25	
HRTN8	021	50	S
	024	25	
HRTN9	020	06	S
	023	30	
INPO	015	38	S
	026	08	
INPOR	015	40	S
	026	09	
JMP	009	43	S
	015	11	
J2	015	43	S
	015	51	
LDFF	005	39	S
	009	26	
LEGAL	002	25	S
	003	31	
	005	31	
LFEF*	004	24	S
	005	16	
LF1	005	06	S
	026	10	
LF2	005	08	S
	026	11	

Signal	Connector	Pin	S
LNST	006	54	S
	010	17	
	015	22	
	009	28	
LNSTPF2	009	48	S
	009	17	
LNSTPF2*	009	40	S
	009	45	
LNSTP0	015	48	S
	026	12	
LNSTPOR	015	50	S
	026	13	
LSF2	006	52	S
	004	28	
	009	13	
LSF2CM	004	20	S
	009	10	
MC	006	44	S
	009	35	
MCSWNC	009	04	S
	026	14	
MCSWNO	009	08	S
	026	28	
MC1*	006	31	S
	004	44	
	003	49	
	002	08	
	008	20	
	007	23	
	007	40	
003	22		
MC1F	004	51	S
	005	03	
	006	47	

Table 8-1. Signal Identification List (Card Cage A3) (Continued)

Signal	Connector	Pin	S
MC2*	006	34	S
	004	04	
	017	48	
MC3*	006	30	S
	005	30	
	017	38	
MC4*	006	27	S
	005	46	
	015	08	
MEM1*	001	55	S
	003	23	
MEM2*	001	57	S
	003	34	
MEM3*	001	53	S
	003	38	
MEM4*	001	56	S
	003	04	
MEM5*	001	51	S
	003	09	
MEM6*	001	54	S
	003	14	
MEM7*	001	48	S
	003	11	
MOD25	001	30	S
	005	49	
MOD32	001	34	S
	001	60	
MPLD*	004	26	S
	005	48	
	006	07	
MSTR	001	12	S
	005	14	

Signal	Connector	Pin	S
ONLINE	005	13	S
	011	45	
	016	17	
	015	36	
ONLINE*	005	44	S
	006	41	
	015	53	
ONLINLT	016	15	S
	026	32	
PAFF	004	33	S
	008	51	
PARERR	007	41	S
	011	21	
PCFF	005	57	S
	003	47	
	006	14	
PCP1	004	07	S
	005	36	
	006	45	
PCP1*	004	38	S
	006	33	
PCP2	005	32	S
	006	35	
PCP2*	002	07	S
	005	29	
	006	32	
PCP3	005	24	S
	006	21	
PCP4	002	10	S
	003	45	
	004	27	
	005	23	
PCP4*	006	24	S
	005	38	
	006	26	S

Table 8-1. Signal Identification List (Card Cage A3) (Continued)

Signal	Connector	Pin	S
PF*	004	06	S
	013	05	
	026	35	
PF2	015	29	S
	009	03	
PF2*	015	32	S
	026	42	
POFAULT	015	55	S
	016	21	
POLIGHT	016	29	S
	026	33	
POSW	005	07	S
	015	56	
	016	31	
	026	34	
PSEQ1	016	05	S
	009	16	
PSEQ2	009	18	S
	006	38	
RCFF*	004	11	S
	005	33	
RCHDDA	013	11	S
	025	11	
RCHDST	013	17	S
	025	12	
RCRS	004	12	S
	015	23	
	015	49	
RCZCAV	012	03	S
	013	25	
RCZCRS	012	11	S
	013	33	
	025	15	
RDY	006	10	S
	005	22	
	011	17	

Signal	Connector	Pin	S
RDY	016	27	
	009	44	
RDY*	009	41	S
	015	21	
READYLT	016	33	S
	026	37	
REC REF	014	32	S
	014	05	
	014	09	
	014	19	
	014	23	
	014	35	
	014	39	
	014	51	
RECPARI	008	07	S
	007	10	
	025	24	
RECZCHA	008	06	S
	025	28	
REC1	003	33	S
	004	16	
	007	03	
	008	03	
	014	15	
REC2	003	42	S
	004	58	
	007	04	
	008	04	
	014	13	
REC3	003	44	S
	004	50	
	007	05	
	014	30	
REC4	003	10	S
	004	05	

Table 8-1. Signal Identification List (Card Cage A3) (Continued)

Signal	Connector	Pin	S
REC4	007	06	
	014	29	S
REC5	003	07	
	004	55	
	007	07	
	014	47	S
REC6	003	40	
	004	13	
	007	08	
	014	45	S
REC7	003	18	
	004	49	
	007	09	
	014	31	S
RN1	006	17	
	026	15	S
RN2	006	20	
	026	16	S
RUN	004	54	
	005	19	
	006	09	S
RUN*	005	15	
	006	12	S
SCEF	003	43	
	005	42	S
SCEF*	003	20	
	005	41	S
	026	45	
SCFF	005	34	S
	004	29	
	006	15	
SHFT*	003	36	
	006	11	S
SPACE*	003	24	
	004	36	S

Signal	Connector	Pin	S
SPSE	004	15	
	005	45	S
STRB	003	16	
	004	47	
	006	04	
	007	11	
	008	05	
	014	34	S
TS01	005	28	
	006	03	S
TS01*	003	37	
	006	36	S
TS02	003	39	
	005	18	
	007	22	
	006	18	S
TS02*	003	46	
	005	27	
	006	39	S
TS02A	004	10	
	005	26	S
VCL	016	43	S
	018	55	
	019	55	
	020	55	
	021	55	
	022	55	
XCAM	010	55	S
	025	16	
XCIND	010	07	S
	025	18	
XDEML	011	55	S
	025	19	
XLNST	010	18	S
	025	20	

Table 8-1. Signal Identification List (Card Cage A3) (Continued)

Signal	Connector	Pin	S
XONLINE	011	26	S
	025	13	
XPARERR	011	07	S
	025	26	
XRDY	011	18	S
	025	21	
XZCCK	010	26	S
	025	22	
ZCAV*	004	09	S
	008	10	
	008	46	
	004	08	
	006	06	
ZCAV	005	55	S
	004	34	
	008	11	
	008	45	
	012	15	
	013	29	
	015	05	
017	10		
ZCCK	010	45	S
	017	08	
ZCFF	009	24	S
	015	26	
	015	57	
ZCF1*	008	43	S
	017	34	
ZCF2*	008	44	S
	017	28	
ZCRS*	004	42	S
	008	12	
	008	47	
	005	20	
	012	13	
	013	47	
	017	04	

Signal	Connector	Pin	S
ZC1G	017	54	S
	026	17	
ZC1K	017	46	S
	026	18	
ZC2G	017	42	S
	026	19	
ZC2K	017	36	S
	026	20	
ZC3G	017	30	S
	026	21	
ZC3K	017	16	S
	026	22	
ZC4G	017	14	S
	026	23	
ZC4K	017	12	S
	026	24	
1CLK1	002	04	S
	004	41	
	006	56	
1CLK2	004	18	S
	006	55	
1CLK3	006	50	S
	005	21	
	015	14	
1CLK4	006	49	S
	005	43	
	015	09	
12VINT	016	11	S
	018	03	
12VINT1	018	04	S
	019	03	

Table 8-1. Signal Identification List (Card Cage A3) (Continued)

Signal	Connector	Pin	S
12VINT2	019	04	S
	020	03	
12VINT3	020	04	S
	021	03	
12VINT4	021	04	S
	022	03	

Signal	Connector	Pin	S
2CLK	006	43	S
	005	11	
	003	12	
	007	20	
2CLK*	006	46	S
	008	21	

8-5 GLOSSARY

8-6 Table 8-2 provides a glossary of signal terms and definitions arranged in alphabetical order. An asterisk (\*) replaces the overbar used to denote the inverted or not function of a term. Example: CHCK\* = CHCK. The glossary also provides the equation, when applicable, from which the term is derived, and the figure number from which the term originates. (K) denotes flip-flop reset term; x denotes numeric sequence.

Table 8-2. Signal Glossary

Term	Equation	Figure No.	Definition
ADVC		6-8	Column register advance
ADVC	= PCFF PCP4 + CONT* TS02 + SCEF PCP4		Increment column register during scan Count input data characters Advance to count 24 and clear
CAM		6-28	Top-of-form cam switch debounced
CAM	= CAMSW		Top-of-form cam switch actuated
CAMSW and CAMSW*		6-1	Top-of-form cam switch outputs
CCSN		6-7	Character clock sync
CCSN J	= CCSN* PCP4 1CLK1		During first PCP1 after CHCK
CCSN K	= PCP2		Reset at end of 1st PCP1
CHCK1 thru CHCK4		6-14	Character clocks

Table 8-2. Signal Glossary (Continued)

Term	Equation	Figure No.	Definition
CHPO		6-3	Character clock pickoff
CHPOR		6-3	Character clock pickoff return
CIND		6-14	Character index
COMP		6-14	Compare (character counter vs data register)
COMP*	$= CC01* DR01$ $+ CC01 DR01*$ $+ CC02* DR02$ $+ CC02 DR02*$ $+ CC03* DR03$ $+ CC03 DR03*$ $+ CC04* DR04$ $+ CC04 DR04*$ $+ CC05* DR05$ $+ CC05 DR05*$ $+ CC06* DR06$ $+ CC06 DR06*$ $+ CC07* DR07$ $+ CC07 DR07*$ $+ MC1$	6-7	No comparison made No comparison made No comparison made No comparison made No comparison made No comparison made No comparison made No comparison made No comparison made No comparison made No comparison made No comparison made No comparison made No comparison made No comparison made No comparison made No comparison made No comparison made Master clear
CONT		6-9	Control
CONT	$= CRFF$ $+ PFCM$		Carriage return Form feed or line feed
CROO		6-8	Column register flip-flop (LSB)
CROO J	$= CR24* ADV C$		Increment counter
CROO K	$= CROO ADV C$ $+ CRRS$		Increment counter Column register reset
CR01		6-8	Column register flip-flop
CR01 J	$= CR01* CROO ADV C$		Increment counter
CR01 K	$= CR01 CROO ADV C$ $+ CRRS$		Increment counter Column register reset



Table 8-2. Signal Glossary (Continued)

Term	Equation	Figure No.	Definition
CR02		6-8	Column register flip-flop
CR02 J	= CR02* CR01 CR00 ADVC		Increment counter
CR02 K	= CR02 CR01 CR00 ADVC + CRRS		Increment counter Column register reset
CR03		6-8	Column register flip-flop
CR03 J	= CR03* CR02 CR01 CR00 ADVC		Increment counter
CR03 K	= CR03 CR02 CR01 CR00 ADVC + CR24 ADVC + CRRS		Increment counter Reset from count 24 to 00 Column register reset
CR04		6-8	Column register flip-flop
CR04 J	= CR04* CR03 CR02 CR01 CR00 ADVC		Increment counter
CR04 K	= CR04 CR24 ADVC + CRRS		Reset from count 24 to zero Column register reset
CRRS		6-8	Column register reset
CRRS	= DIBF* TS01* TS02 + CRSS1 + MC1		Received only control character Column register reset no. 1 Master clear
CRRS1		6-9	Column register reset no. 1
CRRS1	= ZCAV + MPEF(K)		Reset at zone change Reset during paper advance
CRTC		6-10	Column register top count
CRTC	= CR04 CR03 MOD25		Top count 24
CR19		6-10	Column register count at 19
CR19	= CR04 CR01 CR00	6-8	Count 19
CR24		6-10	Column register count at 24
CR24	= CR04 CR03 MOD25		Top count for 25 character memory
DATASTR		6-4	Data strobe line from user system

Table 8-2. Signal Glossary (Continued)

Term	Equation	Figure No.	Definition
DATA1 thru DATA7		6-4	Data lines from user system
DC01		6-7	Delay counter flip-flop (LSB)
DC01 J	= DCCF CCSN		Increment counter
DC01 K	= DC01 DCCF CCSN + DCCF*		Increment counter Delay counter reset
DC02		6-7	Delay counter flip-flop
DC02 J	= DC02* DC01		Increment counter
DC02 K	= DC02 DC01 + DCCF*		Increment counter Delay counter reset
DC03		6-7	Delay counter flip-flop
DC03 J	= DC03* DC02		Increment counter
DC03 K	= DC03 DC02 + DCCF*		Increment counter Delay counter reset
DC04		6-7	Delay counter flip-flop
DC04 J	= DC04* DC03		Increment counter
DC04 K	= DC04 DC03 + DCCF*		Increment counter Delay counter reset
DC05		6-7	Delay counter flip-flop
DC05 J	= DC05* DC04		Increment counter
DC05 K	= DC05 DC04 + DCCF*		Increment counter Delay counter reset
DC06		6-7	Delay counter flip-flop (MSB)
DC06 J	= DC06* DC05		Increment counter
DC06 K	= DC06 DC05 + DCCF*		Increment counter Delay counter reset
DCCF		6-9	Delay counter control flip-flop
DCCF J	= ZCAV 1CLK1 + PAFF(K) 1CLK1		Start delay after zone change Start delay after paper advance
DCCF K	= DCTC 1CLK1 + DCRS 1CLK1 + MC1		End of 26-ms delay at count 48 Delay counter reset Master clear

Table 8-2. Signal Glossary (Continued)

Term	Equation	Figure No.	Definition
DCRS		6-28	Delay counter reset
DCRS	= DIBF* LDFF ZCFF CONT		Cancel delay after zone change
DCTC		6-7	Delay counter top count
DCTC	= DC05 DC06		Count 48
DEML		6-11	Demand line enable
DEML	= ONLINE DLFF		Request for data input
DGINT		6-1	Drum gate interlock
DIBF		6-10	Data in buffer flip-flop
DIBF J	= CONT* TS02		Data entered into memory
	+ LEGAL PCP2 PCFF 1CLK4		Character in scan printable
DIBF K	= PCFF CR19 PCP4 1CLK4		End of scan reset
	+ MC3		Master clear
DLFF		6-11	Demand line flip-flop
DLFF J	= MC2F		Initial demand
	+ CR19* TS02 TS01		New demand after previous character
	+ ZCAV 2CLK		New demand during zone change
	+ MPLD 2CLK		New demand during paper advance
DLFF K	= STRB 2CLK		Character entered in data register and demand line inhibited
DR01		6-8	Data register flip-flop (LSB)
DR01 thru DR05 J	= RECx STRB		Enter input data
	+ MEMx SHFT 2CLK		Enter data from memory
DR01 thru DR05 K	= MEMx* SHFT 2CLK		Enter data from memory
	+ SHFT* TS02 2CLK		Reset after data transfer to memory
	+ PCFF HDST6 COMP 2CLK		Compare reset
	+ HDST6 PCFF LEGAL* 2CLK		Nonprintable character reset
	+ SCEF		Reset before scan
	+ MC1		Master clear

Table 8-2. Signal Glossary (Continued)

Term	Equation	Figure No.	Definition
DR06		6-8	Data register flip-flop
DR06 J	= REC6 SPACE* STRB		Do not set if space
	+ MEM6 SHFT 2CLK		Enter data from memory during scan
DR06 K	= Same as DR01 thru DR05		Same as DR01 thru DR05
DR07		6-8	Data register flip-flop (MSB)
DR07 J	= Same as DR01 thru DR05		Same as DR01 thru DR05
DR07 K	= Same as DR01 thru DR05		Same as DR01 thru DR05
FAULT		6-15	Indicates abnormal condition
FFFF		6-9	Form feed flip-flop
FFFF J	= FF command		Form feed control character
	+ FFSW RUN* 1CLK1		Manual form feed command
FFFF K	= CAM 1CLK1 + MC1		Cam at top-of-form Master clear
FFSW		6-10	TOP OF FORM switch debounced
FFSW	= FF1 FF2*		TOP OF FORM switch activated
FFSW*	= FF1* FF2		TOP OF FORM switch deactivated
FF1 and FF2		6-5	TOP OF FORM switch outputs
HDCL	= MC1F 1CLK	6-11	Hammer driver clear during master clear
HDRS1 thru HDRS5	= CCSN	6-28	Hammer driver resets
HDSS		6-16	Hammer delay single shot
HDST		6-10	Hammer driver strobe
HDST	= PCFF PCP2		Strobe hammer driver register
HDST1 thru HDST6		6-14	Hammer driver strobes

Table 8-2. Signal Glossary (Continued)

Term	Equation	Figure No.	Definition
HDIC6 thru HDIC9		6-27	Hammer driver register interconnects
HISW		6-25	Print inhibit signal from switch PRINT INHIBIT
HM01 thru HM80		6-17	Hammer driver outputs to hammer coils
HRNT1 thru HRNT20		6-26	Hammer driver returns
INP0		6-3	Index pickoff
INPOR		6-3	Index pickoff return
LDFE		6-10	Load data flip-flop
LDFE J	= CRRS1 1CLK3 + MPLD 1CLK3 + ZCAV 1CLK3		Master clear Paper advance Zone change
LDFE K	= TS02A CR19 1CLK3 + TS02A CONT 1CLK3 + MC4		Reset at end of load data operation Control character only reset Master clear
LEGAL		6-7	Printable character
LEGAL	= DR06 DR07* + DR06* DR07		Character code $\geq 32 \leq 63$ Character code $\geq 64 \leq 95$
LFEF		6-10	Line feed enable flip-flop
LFEF J	= RUN* LFSW + RUN* FFSW		Manual paper feed command Manual form feed command
LFEF K	= CRRS1 1CLK3 + MPLD 1CLK3 + ZCAV 1CLK3 + SCEF		Master clear Paper advance Zone change Scan enable
LFFF		6-9	Line feed flip-flop
LFFF J	= PF command + FFFF 1CLK1 + LFEF 1CLK1		Paper feed control character Form feed control character Manual form or paper feed command

Table 8-2. Signal Glossary (Continued)

Term	Equation	Figure No.	Definition
LFFF K	$= \text{MPEF PAFF}^* 1\text{CLK1}$ $+ \text{LSF2CM DIBF}^* 1\text{CLK1}$  $+ \text{MC1}$	6-10	Paper feed enabled Multiple line advance complete to line n-1 Master clear
LFSW			PAPER STEP switch debounced
LFSW	$= \text{LF1 LF2}^*$		PAPER STEP switch activated
LFSW*	$= \text{LF1}^* \text{LF2}$		PAPER STEP switch deactivated
LF1 and LF2		6-5	PAPER STEP switch outputs
LNST		6-14	Line strobe
LNSTP0		6-1	Line strobe pickoff
LNSTPOR		6-1	Line strobe pickoff return
LSF2		6-11	Line strobe flip-flop no. 2
LSF2 J	$= \text{LSFF } 1\text{CLK}$		Sync on line strobe
LSF2 K	$= \text{LSFF}^* 1\text{CLK}$  $+ \text{MC1F}$		Master clear
LSF2CM		6-28	Multiple line advance without top-of-form
LSF2CM	$= \text{LSF2 CAM}^*$		Reset flip-flop LFFF after successive PF command
MC		6-28	Master clear
MC	$= \text{MCSWDB}$		Initiate master clear
MCSWDB		6-28	MASTER CLEAR switch debounced
MCSWDB	$= \text{MCSWNC MCSWNO}^*$		MASTER CLEAR switch activated
MCSWDB*	$= \text{MCSWNC}^* \text{MCSWNO}$		MASTER CLEAR switch deactivated
MCSWNC and MCSWNO		6-25	MASTER CLEAR switch outputs
MC1F		6-11	Master clear flip-flop no. 1
MC1F J	$= \text{MC}$  $+ \text{PSEQ}$   $+ \text{FAULT } 1\text{CLK}$		Hold in master clear Master clear for 10 seconds after turnon Clear system on fault

Table 8-2. Signal Glossary (Continued)

Term	Equation	Figure No.	Definition
MC1F K	$= MC * PSEQ * MC2F$ $1CLK$	6-11	End master clear
MC2F			Master clear flip-flop no. 2
MC2F J	$= MC1F 1CLK$		Terminate clear and enable RDY
MC2F K	$= MC1F * 1CLK$ $+ MC$ $+ PSEQ$		RDY enabled Initiate master clear Initiate master clear
MC1* thru MC4*		6-11	Master clear signals
MEM1* thru MEM7*		6-6	Buffer memory outputs
MOD25		6-10	Modulo 25 for 25 character memory
MOD32		6-10	Modulo 32 for 32 character memory
MPEF		6-9	Move paper enable flip-flop
MPEF J	$= PFCM SPSE DIBF * 1CLK2$ $+ PFCM SCFF CR19$ $DIBF * PCP4 1CLK2$		Enable paper advance after PF or FF command Enable paper advance after scan and print
MPEF K	$= FFLS 1CLK2$ $+ MPEF PAFF * PCP1 1CLK2$ $+ MC2$		Multiple paper advance complete to line n-1 Paper advance enabled Master clear
MPLD		6-9	Move paper and load data
MPLD	$= FFFF * CAM * MPEF(K)$		Raise demand line during paper advance
MSTR		6-10	Memory strobe
MSTR	$= PCFF PCP3 1CLK4$ $+ SCEF PCP3 1CLK4$ $+ CONT * TS02 * TS01 2CLK$		Shift stored data during scan Shift data to memory location 1 Strobe input data from data register to memory
ONLINE		6-10	On-line flip-flop
ONLINE J	$= RUN RDY 2CLK$		Printer ready and ON LINE/OFF LINE switch pressed to ON LINE

Table 8-2. Signal Glossary (Continued)

Term	Equation	Figure No.	Definition
ONLINE K	= POSW LDFJ(J) 2CLK		Paper fault-wait till end of print cycle
	+ RUN* LDFJ(J) 2CLK		OFF LINE switch-wait till end of print cycle
	+ RDY*		System in master clear state
PAFF		6-9	Paper advance flip-flop
PAFF J	= MPEF PCP1 1CLK2		Advance paper
PAFF K	= MPEF* FFFF* CAM* LSF2 1CLK2		Paper advance completed
	+ MC2		Master clear
PARERR		7-7	Parity error
PCFF		6-10	Print control flip-flop
PCFF J	= SCFF CCSN RCFF* PCP1 1CLK3		Start scan and print cycle
PCFF K	= CR19 PCP4 1CLK3		Scan completed
	+ MC4		Master clear
PCP1 thru PCP4		6-11	Printer clock pulses for state timing
PF		6-9	Paper feed advance
PF	= HDSS* PAFF DCCF*		Advance paper 1.3 milliseconds after hammers fire
PFCM		6-9	Paper feed command
PFCM	= FFFF		Form feed (FF) command
	+ LFFF		Line feed (PF) command
POFAULT		6-14	Paper out fault
POSW		6-1	Fault signal from paper out switches
PSEQ		6-15	Power sequence (10-second delay signal)
RCFF		6-9	Recovery control flip-flop
RCFF J	= ZCAV 1CLK2		Inhibit print during zone change
	+ PAFF		Inhibit print during paper advance
RCFF K	= RCRS 1CLK2		Delay completed
	+ MC2		Master clear



Table 8-2. Signal Glossary (Continued)

Term	Equation	Figure No.	Definition
R CRS		6-14	Recovery control flip-flop reset
R CRS	= ZCFF DC04 + DC05		4.3 ms delay after zone change 8.0 ms delay after paper advance
RDY		6-11	Ready flip-flop
RDY J	= MC2F 1CLK		Printer ready after master clear
RDY K	= MC1F		Inhibit printer during master clear
READYLT		6-15	Ready light
RECPAR1		6-4	Receiver parity
REC REF		6-13	Receiver reference
RECZCHA		6-4	Receiver zone change
REC1 thru REC7		6-13	Input data to data register
RN1		6-5	ON LINE/OFF LINE switch in ON LINE position
RN2		6-5	ON LINE/OFF LINE switch in OFF LINE position
RUN		6-11	Run flip-flop
RUN J	= RN1* 1CLK		On-line mode
RUN K	= RN2* 1CLK + MC1F		Off-line mode Master clear
SCEF		6-10	Scan enable flip-flop
SCEF J	= CR04 CR02 TS02A 1CLK3 + SPSE CONT DIBF 1CLK3 + SCFF CR19 DIBF PCP4 1CLK3		Enter scan and print state on 20th character Enter scan and print state on control character Initiate new scan and print cycle
SCEF K	= CRTC PCP4 1CLK3 + MC4		Initiate scan at column register top count Master clear
SCFF		6-10	Scan control flip-flop
SCFF J	= CRTC PCP4		Begin scan operation
SCFF K	= CR19 PCP4 + MC4		Scan completed Master clear


Table 8-2. Signal Glossary (Continued)

Term	Equation	Figure No.	Definition
SHFT		6-11	Data register shift
SHFT	= SCFF CCSN 1CLK		Enter first character from memory during scan
	+ PCFF PCP1 1CLK		Enter following characters from memory during scan
STFF		6-11	Strobe flip-flop
STFF J	= DEML STRB		Load data
STFF K	= TS02* TS01		Data loaded
SPACE		6-9	Space code
SPACE	= REC1* REC2* REC3* REC4* REC5* REC6 REC7*		Decimal 32 code
SPSE		6-10	Step paper step enable
SPSE	= TS02A		Enable SCEF
	+ LFEF		Enable MPEF
STRB		6-13	Data strobe
TS01		6-11	Time slot flip-flop no. 1
TS01 J	= STFF 2CLK		Start load data timing
TS01 K	= CONT 2CLK		Control code detected
	+ TS02 2CLK		Complete load data timing
	+ MC1F		Master clear
TS02		6-11	Time slot flip-flop no. 2
TS02 J	= TS01 2CLK		Enable DIBF
TS02 K	= TS02 2CLK		Load data timing complete
	+ MC1F		Master clear
TS02A		6-10	Time slot no. 2 synchronized
TS02A J	= TS02A* PCP4 1CLK4		Sync time slots to PCP1 thru PCP4 timing
TS02A K	= PCP2		Sync complete
VCL		6-15	Voltage clamp
XDEML		6-12	Transmitter demand line
XONLINE		6-12	Transmitter on line

Table 8-2. Signal Glossary (Continued)

Term	Equation	Figure No.	Definition
XPARERR		6-12	Transmitter parity error
XRDY		6-12	Transmitter ready
ZCAV		6-9	Zone change advance
ZCAV	= DCCF* ZCEF PCP1		Initiate zone change
ZCCK		6-16	Zone change clock
ZCEF		6-9	Zone change enable flip-flop
ZCEF J	= PFCM* SCFF CR19 DIBF* PCP4 1CLK2  + DIBF* CRFF TS02A 1CLK2		Scan and print operation completed  Execute CR command
ZCEF K	= ZCAV 1CLK2		Zone change completed
ZCFF		6-14	Zone change flip-flop
ZCFF J	= ZCAV 1CLK4		Zone change initiated
ZCFF K	= RCRS 1CLK4  + MC4		4.3 ms delay after zone change Master clear
ZCF1*		7-4	Zone control preset no. 1
ZCF2*		7-4	Zone control preset no. 2
ZCRS		6-9	Zone control reset
ZCRS	= MPEF(K) FFFF  + ZCAV CRFF FFFF  + MC1F		Paper advance CR command Master clear
ZC1G thru ZC4G		6-16	Select signals to zone control SCR gates
ZC1K thru ZC4K		6-16	Select signals from zone control SCR cathodes
1CLK1 thru 1CLK4		6-11	1 mHz clocks
12VINT		6-15	+12 volt interlock
12VINT1 thru 12VINT4			+12 volt interlocks
2CLK		6-11	2 mHz clock

REVISIONS				
LTR	DESCRIPTION	CHECK	DATE	APPROVED
A	INITIAL RELEASE	<i>ferk</i>	9/6/73	<i>J.C. Limback</i>

SUPPLEMENTARY INFORMATION					
FIRST USED ON MODEL	DR				TITLE
2310	CHK <i>Heskus</i> 7/6/73	ADDENDUM			
NEXT ASSEMBLY	APP <i>J.C. Limback</i> 9/6/73	HEWLETT-PACKARD 2310			
	APP	SIZE	CODE IDENT NO.	DRAWING NO.	REV
	APP	A	19790	234876	A
	MATL	SCALE	SHEET 1 OF		
	FINISH				

1.0 INTRODUCTION

1.1 This addendum serves as a supplement to the standard 2310 LINE/PRINTER Technical Manual 214163 Volumes I and II to provide compatibility with the printer configuration supplied to Hewlett Packard.

1.2 This addendum contains information that provides for implementing changes and corrections to the standard 2310 LINE/PRINTER Technical Manual.

2.0 DESCRIPTION

2.1 The Hewlett Packard version of the 2310 LINE/PRINTER differs from the standard printer in the following areas:

- a. Specific drum characters have been replaced.
- b. The number of lines skipped at paper perforation (Top-Of-Form) has been increased to six (6).
- c. Self Test Circuit Card AL-32 has been replaced by Self Test Circuit Card AL-27.
- d. Positive Driver AJ-14 has been replaced by Open Collector Driver AJ-21.

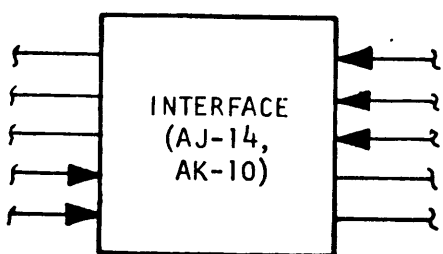
3.0 CONTENTS

3.1 This addendum contains the following material:

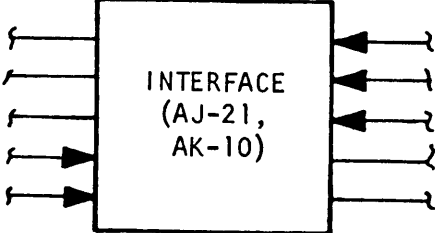
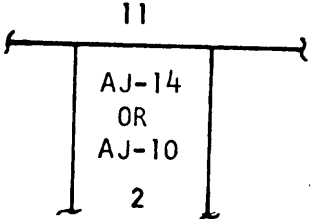
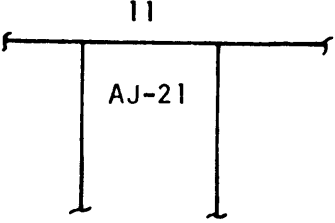
- a. Changes to existing manual pages.
- b. Replacement pages for existing manual pages.

4.0 CHANGES

4.1 Implement changes to existing manual pages per following table:

Item	Page	Changes
1.	4-2	Figure 4-1: WAS: 

DRAWING NO.			REV
234876			
SHEET	2	OF	SHEETS
			A

Item	Page	Changes
1.	4-2	<p>IS:</p> 
2.	5-3	<p>Figure 5-2; A3 Card Cage Slot 11: WAS:</p>  <p>IS:</p> 

DRAWING NO. 234876	REV A
SHEET 3 OF SHEETS	

Item	Page	Changes																												
3.	5-46	Table 5-6: Delete Step 13.																												
4.		<p>Change Self Test Card reference from AL-32 to AL-27 on the pages listed below:</p> <table border="1"> <thead> <tr> <th data-bbox="581 541 651 573">Page</th> <th data-bbox="802 541 943 573">Paragraph</th> </tr> </thead> <tbody> <tr> <td data-bbox="581 621 646 653">5-18</td> <td data-bbox="740 621 805 653">5-18</td> </tr> <tr> <td data-bbox="581 684 646 716">5-21</td> <td data-bbox="740 684 862 716">5-31, f.</td> </tr> <tr> <td data-bbox="581 747 646 779">5-22</td> <td data-bbox="740 747 927 779">5-33, c., l.</td> </tr> <tr> <td data-bbox="581 810 646 842">5-27</td> <td data-bbox="740 810 862 842">5-35, c.</td> </tr> <tr> <td data-bbox="581 873 646 905">5-37</td> <td data-bbox="740 873 862 905">5-53, a.</td> </tr> <tr> <td data-bbox="581 936 646 968">5-39</td> <td data-bbox="740 936 862 968">5-55, a.</td> </tr> <tr> <td data-bbox="581 999 630 1031">7-1</td> <td data-bbox="740 999 878 1031">Table 7-1</td> </tr> <tr> <td data-bbox="581 1062 646 1094">7-24</td> <td data-bbox="740 1062 805 1094">7-78</td> </tr> <tr> <td data-bbox="581 1125 646 1157">7-25</td> <td data-bbox="740 1125 1049 1157">7-80, g., h., and i.</td> </tr> <tr> <td data-bbox="581 1188 678 1262">7-26 &amp; 7-27</td> <td data-bbox="740 1188 911 1220">Figure 7-11</td> </tr> <tr> <td data-bbox="581 1293 646 1325">7-28</td> <td data-bbox="740 1293 911 1325">Figure 7-12</td> </tr> <tr> <td data-bbox="581 1356 646 1388">7-29</td> <td data-bbox="740 1356 911 1388">Figure 7-13</td> </tr> <tr> <td data-bbox="581 1419 646 1451">7-30</td> <td data-bbox="740 1419 992 1451">Table 7-4 &amp; 7-82</td> </tr> </tbody> </table>	Page	Paragraph	5-18	5-18	5-21	5-31, f.	5-22	5-33, c., l.	5-27	5-35, c.	5-37	5-53, a.	5-39	5-55, a.	7-1	Table 7-1	7-24	7-78	7-25	7-80, g., h., and i.	7-26 & 7-27	Figure 7-11	7-28	Figure 7-12	7-29	Figure 7-13	7-30	Table 7-4 & 7-82
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5-18	5-18																													
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7-28	Figure 7-12																													
7-29	Figure 7-13																													
7-30	Table 7-4 & 7-82																													
5.		Delete pages 9-82 thru 9-88.																												

<b>DRAWING NO.</b>		<b>REV</b>
234876		A
<b>SHEET</b>	4 OF	<b>SHEETS</b>

5.0 REPLACEMENTS

5.1 Replace existing manual pages per the following list:

Existing Page No.	Replacement Page No. (Attached)
VOL I	
vii	vii
viii	viii
ix	ix
x	x
xi	xi
1-16	1-16
1-19	1-19
4-3	4-3
4-7	4-7
4-20	4-20
4-21	4-21
4-47	4-47
6-18	
6-19	6-18/19
6-20	
6-21	6-20/21
7-31 &	
7-32	Schematic 219089
VOL II	
i	i
ii	ii
iii	iii
9-19	9-19
9-20	9-20
9-80	9-80
9-81	9-81
9-111	9-111
9-112	9-112

<b>DRAWING NO.</b>		<b>REV</b>
234876		
<b>SHEET</b>	5	<b>OF</b>
		<b>SHEETS</b>
		A



5.2 The replacement pages attached are part of this addendum.

6.0 ATTACHMENTS

6.1 Schematic AL-27, Self Test, 219089.

<b>DRAWING NO.</b>	234876	<b>REV</b>
<b>SHEET 6 OF SHEETS</b>		A

## LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
5-26	Hammer Assembly.....	5-42
5-27	Hammer Assembly Taper Pin Installation.....	5-43
6-1	LINE/PRINTER Model 2310 Harness Assembly Schematic Diagram.....	6-6
6-2	Hammer Bank A2A2 Harness Assembly Schematic Diagram.....	6-7
6-3	Drum Gate A2A1 Schematic Diagram (Printer Serial Numbers 026 Thru 128).....	6-8
6-4	Input/Output Harness Assembly Schematic Diagram.....	6-9
6-5	Control Panel A5 Schematic Diagram.....	6-10
6-6	25-Character Memory AM-10 Logic Diagram.....	6-11
6-6a	32-Character Memory AM-21 Logic Diagram .....	6-12a
6-7	Logic Gate I AG-17 Logic Diagram .....	6-13
6-8	Logic Gate II AG-18 Logic Diagram .....	6-14
6-9	Logic Gate III AG-45 Logic Diagram .....	6-15
6-10	Logic Gate IV AG-20 Logic Diagram .....	6-16
6-11	Timing Control AT-13 Logic Diagram .....	6-17
6-12	Open Collector Driver AJ-21 Schematic Diagram .....	6-18/19
6-13	Receiver AK-10 Schematic Diagram.....	6-22
6-14	Transducer Amplifier AS-13 Logic Diagram.....	6-24
6-15	Hammer Interlock AZ-19 Logic Diagram.....	6-26
6-16	Zone Control AZ-18 Logic Diagram.....	6-27
6-17	Hammer Driver AH-10 Logic Diagram.....	6-29
6-18	Cable Plug Card AZ-14 Schematic Diagram.....	6-31
6-19	Drum Gate A2A1 Schematic Diagram (Printer Serial Number 129 and Up).....	6-32
6-20	Drum Motor Interlock Schematic Diagram.....	6-33
6-21	Hammer Interlock AZ-19 Schematic Diagram.....	6-34
6-22	Paper Feed Control AP-10 Schematic Diagram.....	6-35
6-23	Voltage Regulator AV-10 Schematic Diagram.....	6-36
6-24	Ribbon Control AZ-15 Logic Diagram.....	6-37
6-25	Power Supply A4 Schematic Diagram.....	6-39
6-26	Hammer Drivers To Cable Plug Cards Interconnecting Diagram.....	6-40
6-27	Hammer Driver Register Logic Diagram.....	6-41
6-28	Delay Control and Gates AG-32 Logic Diagram.....	6-42
6-29	J-K Flip-Flop Logic Diagram.....	6-44
6-30	+12V Monitor Schematic Diagram.....	6-45
7-1	Inverting Receiver AK-11 Schematic Diagram.....	7-2
7-2	Negative Driver AJ-10 Schematic Diagram.....	7-4
7-3	Zone Select Option Interconnecting Diagram.....	7-9
7-4	Zone Select AL-12 Logic Diagram.....	7-10
7-5	Zone Select Option Timing Diagram.....	7-11
7-6	Parity Option Interconnecting Diagram.....	7-16
7-7	Parity AL-11 Logic Diagram.....	7-17
7-8	Code Conversion Option Block Diagram.....	7-19
7-9	Matrix Driver AZ-67 Logic Diagram.....	7-20
7-10	Example of Decode Matrix Mechanization.....	7-23
7-11	Negative Logic Self-Test Adapter Schematic Diagram.....	7-26
7-12	Self-Test AL-27 Card Installed (Negative Logic).....	7-28
7-13	Self-Test AL-27 Card Installed (Positive Logic).....	7-29
7-14	Self-Test AL-27 Schematic Diagram.....	7-31
7-14a	Self-Test AL-27 Schematic Diagram.....	7-31a

## LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
7-15	Shifting Pattern Printout (Zones 1 Thru 4).....	7-33
7-16	Portion of Logic Gate i AG-17 Schematic Diagram.....	7-37
7-17	Static Eliminator Assembly Installed (Printer Serial Numbers 012 Thru 200).....	7-39
7-18	Static Eliminator Assembly Installed (Printer Serial Number 201 and Up).....	7-40
7-19	Model 2310 LINE/PRINTER Paper Receptacle and Pedestal Mount Installation.....	7-41

## LIST OF TABLES

Table	Title	Page
1-1	Power Requirements.....	1-3
1-2	Environmental Requirements.....	1-4
1-3	Paper and Ribbon Requirements.....	1-4
1-4	Physical Characteristics.....	1-5
1-5	Performance Characteristics.....	1-5
1-6	Card Cage A3 Standard Complement.....	1-15
1-7	Card Cage A4A4 Complement.....	1-16
1-8	Power Supply Fuse Complement.....	1-17
1-9	Character Font and Sequence of Standard 64-Character Drum.....	1-19
3-1	Control Panel A5 Controls and Indicators.....	3-2
3-2	Power Supply A4 Maintenance Panel Controls and Indicators.....	3-3
3-3	Mechanics A2 Controls and Adjustments.....	3-5
4-1	Receiver/Driver Characteristics.....	4-3
4-2	Interface Signal Definitions.....	4-5
4-3	Coded Character Set.....	4-7
4-4	Example of DR and CC Complementary Pairs.....	4-44
4-5	Code/Character Relationship.....	4-45
5-1	Inspection and Preventive Maintenance Schedule.....	5-5
5-2	Test Equipment and Special Tools Required.....	5-6
5-3	Preliminary Checkout Procedure.....	5-8
5-4	Performance Checkout Procedure.....	5-10
5-5	Hammer Flight Time Adjustment Test Points.....	5-24
5-6	Troubleshooting Chart.....	5-44
6-1	Common Functions of Two Variables.....	6-3
7-1	Card Cage A3 Option Complement.....	7-1
7-2	Negative Logic Receiver/Driver Characteristics.....	7-6
7-3	Card Cage A6 Complement.....	7-18
7-4	Self-Test AL-27 Switch Functions.....	7-30
7-5	Printer Performance Characteristics (With 96-Character Drum).....	7-35
7-6	Coded Character Set (Standard 96-Character Set).....	7-37
8-1	Signal Identification List (Card Cage A3).....	8-1
8-2	Signal Glossary.....	8-13

## CONTENTS

### VOLUME II

<u>Section</u>	<u>Title</u>	<u>Page</u>
IX	MECHANICAL ILLUSTRATIONS	
	Introduction .....	9-1/2

### LIST OF ILLUSTRATIONS

<u>Figure</u>	<u>Title</u>	<u>Page</u>
9-1	Line/Printer Assembly .....	9-3/4
9-2	Mechanics Assembly .....	9-9/10
9-3	Mechanics Frame Assembly .....	9-13/14
9-4	Control Panel Assembly .....	9-17
9-5	Top of Form Assembly .....	9-19
9-6	Female Latch Sub-Assembly .....	9-21
9-7	Paper Drive Sub-Assembly .....	9-23
9-8	Vertical Paper Adjust Assembly .....	9-25
9-9	Power Supply Assembly .....	9-27
9-10	Drum Gate Assembly, 64-Character .....	9-33/34
9-11	Drum Sub-Assembly, 64-Character .....	9-39
9-12	Drum Gate Assembly, 96-Character .....	9-41/42
9-13	Drum Sub-Assembly, 96-Character .....	9-47
9-14	Card Cage Assembly .....	9-49/50
9-15	Hammer Bank Assembly .....	9-52
9-16	Hammer Bank Harness Assembly .....	9-54
9-17	Main Harness Assembly .....	9-56
9-18	In/Out Harness Assembly .....	9-58
9-19	Static Eliminator Assembly .....	9-60
9-20	Character Memory, AM-10, Circuit Card Assembly .....	9-62
9-21	Character Memory, AM-21, Circuit Card Assembly .....	9-66
9-22	Logic Gate I, AG-17, Circuit Card Assembly .....	9-68
9-23	Logic Gate II, AG-18, Circuit Card Assembly .....	9-70
9-24	Logic Gate III, AG-45, Circuit Card Assembly .....	9-72
9-25	Logic Gate IV, AG-20, Circuit Card Assembly .....	9-74
9-26	Timing Control, AT-13, Circuit Card Assembly .....	9-76
9-27	Delay Control and Gates, AG-32, Circuit Card Assembly ..	9-78
9-28	Driver, AJ-21, Circuit Card Assembly .....	9-80
9-29	Not Assigned	
9-30	Not Assigned	
9-31	Receiver, AK-10, Circuit Card Assembly .....	9-89
9-32	Inverting Receiver, AK-11, Circuit Card Assembly .....	9-92
9-33	Transducer Amplifier, AS-13, Circuit Card Assembly .....	9-95

# DATA PRODUCTS CORPORATION

Woodland Hills - California 91364

CODE IDENT

19790

DRAWING NO.

234801

REV.

A

SHEET 1 OF 2

TITLE

**WIRE LIST,** DELETE/ADD HEWLETT PACKARD

REVISIONS

REV.	E.O. NO.	DESCRIPTION	CHK.	APPD.	DATE
A	18551	PRODUCTION RELEASE	JED	Ch	11-2-72

NOTES: UNLESS OTHERWISE SPECIFIED

A - STRANDED INSULATED	S1 - SHIELDED SINGLE COND. WITH JACKET	ASSEMBLY	232630
B - SOLID INSULATED	S2 - SHIELDED TW. PAIR WITH JACKET	SCHEMATIC	
C - SOLID BARE	T1 - SOLID TW. PAIR	MODEL	2310
D - COAX	T2 - STRANDED TW. PAIR	DR	J.E. Duda 11-2-72
E -	S - SOLDER	CHK.	<i>J. E. Duda</i> 11-2-72
F -	T - CRIMP	APP.	C. <i>[Signature]</i> 11/2/72
G -	U - WIRE WRAP	APP.	<i>[Signature]</i> 11/2/72
H -	V - CLAMP		

CONTENTS (Cont'd)

LIST OF ILLUSTRATIONS (Cont'd)

<u>Figure</u>	<u>Title</u>	<u>Page</u>
9-34	Hammer Interlock, AZ-19, Circuit Card Assembly .....	9-98
9-35	Zone Control, AZ-18, Circuit Card Assembly .....	9-102
9-36	Hammer Driver, AH-10, Circuit Card Assembly .....	9-105
9-37	Cable Plug, AZ-14, Circuit Card Assembly .....	9-109
9-38	Cable Plug, AZ-85, Circuit Card Assembly .....	9-110
9-39	Self Test, AL-27, Circuit Card Assembly .....	9-111
9-40	Parity, AL-11, Circuit Card Assembly .....	9-113
9-41	Zone Select, AL-12, Circuit Card Assembly .....	9-115
9-42	Paper Feed Control, AP-10, Circuit Card Assembly .....	9-117
9-43	Voltage Regulator, AV-10, Circuit Card Assembly .....	9-121
9-44	Ribbon Control, AZ-84, Circuit Card Assembly .....	9-125
9-45	SCR Commutating Board, AZ-79, Circuit Card Assembly .....	9-128
9-46	Power Amplifier, AZ-49, Circuit Card Assembly .....	9-130
9-47	Negative Paper Feed Power Amplifier, AZ-51, Circuit Card Assembly .....	9-132
9-48	Bridge Board, AZ-78, Circuit Card Assembly .....	9-134
9-49	Not Assigned	9-136
9-50	Code Conversion, AD-28, Circuit Card Assembly .....	9-139

LIST OF TABLES

<u>Table</u>	<u>Title</u>	<u>Page</u>
9-1	Line/Printer Assembly .....	9-7/8
9-2	Mechanics Assembly .....	9-11
9-3	Mechanics Frame Assembly .....	9-15
9-4	Control Panel Assembly .....	9-18
9-5	Top of Form Assembly .....	9-20
9-6	Female Latch Sub-Assembly .....	9-22
9-7	Paper Drive Sub-Assembly .....	9-24
9-8	Vertical Paper Adjust Assembly .....	9-26
9-9	Power Supply Assembly .....	9-30
9-10	Drum Gate Assembly, 64-Character .....	9-37
9-11	Drum Sub-Assembly, 64-Character .....	9-40
9-12	Drum Gate Assembly, 96-Character .....	9-45
9-13	Drum Sub-Assembly, 96-Character .....	9-48
9-14	Card Cage Assembly .....	9-51
9-15	Hammer Bank Assembly .....	9-53
9-16	Hammer Bank Harness Assembly .....	9-55
9-17	Main Harness Assembly .....	9-57
9-18	In/Out Harness Assembly .....	9-59
9-19	Static Eliminator Assembly.....	9-61

## CONTENTS (Cont'd)

### LIST OF TABLES (Cont'd)

<u>Table</u>	<u>Title</u>	<u>Page</u>
9-20	Character Memory, AM-10 Assembly Replaceable Parts .....	9-63
9-21	Character Memory, AM-21 Assembly Replaceable Parts .....	9-67
9-22	Logic Gate I, AG-17 Assembly Replaceable Parts .....	9-69
9-23	Logic Gate II, AG-18 Assembly Replaceable Parts .....	9-71
9-24	Logic Gate III, AG-45 Assembly Replaceable Parts .....	9-73
9-25	Logic Gate IV, AG-20 Assembly Replaceable Parts .....	9-75
9-26	Timing Control, AT-13 Assembly Replaceable Parts .....	9-77
9-27	Delay Control and Gates, AG-32 Assembly Replaceable Parts .....	9-79
9-28	Driver, AJ-21, Assembly Replaceable Parts.....	9-81
9-29	Not Assigned	9-84
9-30	Not Assigned	9-87
9-31	Receiver, AK-10 Assembly Replaceable Parts .....	9-90
9-32	Inverting Receiver, AK-11 Assembly Replaceable Parts ...	9-93
9-33	Transducer Amplifier, AS-13 Assembly Replaceable Parts .....	9-96
9-34	Hammer Interlock, AZ-19 Assembly Replaceable Parts .....	9-99
9-35	Zone Control, AZ-18 Assembly Replaceable Parts .....	9-103
9-36	Hammer Driver, AH-10 Assembly Replaceable Parts .....	9-106
9-37	Self Test, AL-32 Assembly Replaceable Parts .....	9-112
9-38	Parity, AL-11 Assembly Replaceable Parts .....	9-114
9-39	Zone Select, AL-12 Assembly Replaceable Parts .....	9-116
9-40	Paper Feed Control, AP-10 Assembly Replaceable Parts ...	9-118
9-41	Voltage Regulator, AV-10 Assembly Replaceable Parts ....	9-122
9-42	Ribbon Control, AZ-84 Assembly Replaceable Parts .....	9-126
9-43	SCR Commutating Board, AZ-79 Assembly Replaceable Parts .....	9-129
9-44	Power Amplifier, AZ-49 Assembly Replaceable Parts .....	9-131
9-45	Negative Paper Feed Power Amplifier, AZ-51 Assembly Replaceable Parts .....	9-133
9-46	Bridge Board, AZ-78 Assembly Replaceable Parts .....	9-135
9-47	Not Assigned	9-137
9-48	Code Conversion, AD-28 Assembly Replaceable Parts .....	9-140





Table 1-6. Card Cage A3 Standard Complement (Continued)

Card Type	Description	Quantity	Reference Designator	Slot
AT-13	Timing Control	1	A3A6	6
AG-32	Delay Controls and Gates	1	A3A9	9
AJ-21	Open Collector Driver	1	A3A11	11
AK-10	Receiver	1	A3A14	14
AS-13	Transducer Amplifier	1	A3A15	15
AZ-19	Hammer Interlock	1	A3A16	16
AZ-18	Zone Control	1	A3A17	17
AH-10	Hammer Driver	5	A3A18 thru A3A22	18 thru 22
AZ-14	Odd Hammers Cable Plug Card	1	A3P23	23
AZ-14	Even Hammers Cable Plug Card	1	A3P24	24
AZ-14	Input/Output Cable Plug Card	1	A3P25	25
AZ-14	Internal Interface Cable Plug Card	1	A3P26	26

1-23 POWER SUPPLY A4

1-24 Power supply A4 provides the printer with operating voltages of -12v, +5v, +12v, +28v, +65v, and 115 vac. The power supply card cage contains ten printed circuit cards and one cable plug card. Card connectors and test jacks are located on mother board, and input power circuit breaker, fuses, checkout switches, and fault indicators are located on the maintenance panel. See table 1-7 for the power supply card cage complement, and table 1-8 for fuse complement.

Table 1-7. Power Supply A4 Card Cage Complement

Card Type	Description	Quantity	Reference Designator	Slot
AZ-85	Cable Plug Card	1	A4P1	See figure 5-2 ↑ ↓ See figure 5-2
AP-10	Paper Feed Control	1	A4A1	
AV-10	Voltage Regulator	1	A4A2	
AZ-84	Ribbon Control	1	A4A3	
AZ-79	SCR Commutating	1	A4A4	

manner, the printer's 20 hammer drivers can be time-shared among the 80 print positions. See figure 1-12 for a simplified block diagram of the printer.

1-29 PRINT CYCLE

1-30 During the print cycle the paper and inked ribbon pass between the 80 hammers and the continuously rotating character drum. The stored characters are scanned in synchronism with the rotating characters and the print control system actuates the appropriate hammer as the desired character approaches the print position.

1-31 Character Drum

1-32 The standard character drum contains 64 different characters consisting of 26 uppercase alphabets, 10 numerals, and 28 other symbols. See table 1-9 for the order in which the rows of characters appear on the drum.

1-33 Interlock

1-34 The interlock and fault detect circuits protect the printer in case certain conditions exist. The printer is inhibited from printing under the following conditions:

- a. Paper out or torn
- b. Drum gate open or improperly closed
- c. Paper feed motor overtemperature or overspeed
- d. VCI, +5V and +12V supplies fault

Note

With all interlocks satisfied, the printer is inhibited from printing if power supply switch PRINT INHIBIT is on.

When all interlocks are satisfied, a ready signal is transmitted to the user.

Table 1-9. Character Font and Sequence of Standard 64-Character Drum

Rows 1-16	Rows 17-32	Rows 33-48	Rows 49-64
Space (f)	Ø	@	P
!	1	A	Q
"	2	B	R
#	3	C	S
\$	4	D	T
%	5	E	U
&	6	F	V
'	7	G	W
(	8	H	X
)	9	I	Y
*	:	J	Z
+	;	K	[
,	<	L	\
-	=	M	]
.	>	N	↑
/	?	O	←

4-7 Signals CHCK1, CHCK2, and CHCK3 enable those hammer drivers whose flip-flops have been set, and the characters in those print positions are printed. CCSN then initiates another scan period and the remaining characters in memory are scanned and compared as before. This operation is repeated until all characters in memory have been compared and printed.

4-8 If the print cycle is originally initiated on receipt of the 20th printable character, then signal ZCAV is generated upon completion of printing. The zone control register is incremented by 1 and DEMAND LINE enabled. The next printable character received will be printed in the leftmost position of zone 2.

4-9 If the print cycle is initiated instead by a format control command, then upon completion of printing, the column register is reset to the leftmost position (column 1) and the command executed. The demand line is enabled and the printer remains in zone 1.

4-10 Assuming a normal print operation of 80 characters per line, the hammer drivers switch to zone 2 and memory is loaded with another set of characters from the user system. The print cycle sequence described for zone 1 is then repeated for zone 2, and again for zones 3 and 4.

4-11 INTERFACE

4-12 Signals between the printer and user system are interfaced through eight receivers and three drivers. See figure 4-2 for a simplified printer/user system interface diagram. See table 4-1 for the receiver and driver characteristics.

Table 4-1. Receiver/Driver Characteristics

Item	Receiver	Driver
Input Impedance	10K	To be determined by user  Output is open collector transistor:  $V_{ce0} = 15v$  $I_c \text{ max} = 40 \text{ ma}$  $+0.4v \text{ max}$
Output Impedance		
Load Resistance		
Load Capacitance		
Signal Transition Rate		
Logic 1	Adjustable from +10.0v max to + 3.0v min	
Logic 0	+1.0v max 0.0v min	
Threshold Voltage	1/2 of logic 1	

4-17 FORMAT CONTROL

4-18 Characters PF, CR, and FF, in table 4-3, are the three characters available to the user for format control. Each is a command that places the printer in the print mode, and upon completion of printing is executed as follows:

a. PF (Paper Feed). The PF command advances the paper one line, clears the column register, returning it to the leftmost print position, and initializes the zone control register. DEMAND LINE is enabled before the paper comes to a stop, and the printer accepts the next set of characters. If the first character in the new set is another PF instruction, DEMAND LINE is disabled and the paper continues slewing for another line. Slewing will continue, one line for every PF command, as long as PF commands are transmitted. A top-of-form cam output during a given paper feed will cause the paper to slew for 6 lines and thus skip over perforations.

b. CR (Carriage Return). The CR command clears the column register, and initializes the zone control register.

c. FF (Form Feed). The FF command advances the paper to the third line of the next form, clears the column register, and initializes the zone control register. DEMAND LINE is enabled before the paper is stopped.

Table 4-3. Coded Character Set

b7 b6 b5				0 0 0	0 1 0	0 1 1	1 0 0	1 0 1
b4	b3	b2	b1					
0	0	0	0		Space	Ø	@	P
0	0	0	1		!	1	A	Q
0	0	1	0		"	2	B	R
0	0	1	1		#	3	C	S
0	1	0	0		\$	4	D	T
0	1	0	1		%	5	E	U
0	1	1	0		&	6	F	V
0	1	1	1		'	7	G	W
1	0	0	0		(	8	H	X
1	0	0	1		)	9	I	Y
1	0	1	0	PF	*	:	J	Z
1	0	1	1		+	;	K	[
1	1	0	0	FF	,	<	L	\
1	1	0	1	CR	-	=	M	]
1	1	1	0		.	>	N	^
1	1	1	1		/	?	O	␣

4-55 Top-of-Form Cam. The top-of-form cam is driven by the motor and actuates cam switch S3 (figure 1-5) each time 11 inches of paper is advanced. The state of switch S3 is indicated by signals CAM and CAM\*.

4-56 The cam is advanced one line, as is the paper, with each paper feed command. During this time CAM is false and CAM\* is true. If during a paper feed command the bottom of the form is reached (11 inches advanced) the cam actuates switch S3 and CAM goes true and CAM\* goes false. When CAM\* goes false, PF\* is unable to go true when LSF2 occurs. As a result, the paper feed amplifier continues to drive the motor and advance the paper. The paper is advanced six additional lines; past the paper perforations and to the fifth line of the next form. The cam then releases switch S3 and CAM goes false and CAM\* goes true. When CAM\* goes true, PF\* goes true on the next LSF2, and the motor is decelerated and stopped as previously described.

4-57 If a form-feed command is given, PF\* is held false and the paper advanced until the cam actuates switch S3 and initiates the sequence described above. See figure 4-11 for a timing diagram of the top-of-form function.

4-58 Overspeed Detector. The overspeed detector monitors the tachometer output during paper advance, and consists of regulator diode VR3, detector Q7, and driver Q8.

4-59 At normal motor speeds, regulator diode VR3 is cut off, detector Q7 is on, and driver Q8 is off. If motor speed becomes excessive, the tachometer output reaches the breakdown voltage of VR3. VR3 conducts, dropping the input of Q7 to zero, and Q7 turns off. Driver Q8 now turns on and its output fires SCR Q12 in voltage regulator AV-10. Q12 shunts +22v to relay coil RT in circuit breaker CB1 (see figure 4-6). The relay energizes and opens CB1, removing input power from power supply A4.

4-60 Interlock and Fault Detect

4-61 The printer is inhibited from printing if certain conditions exist or occur during printer operation. The logic necessary to perform this function is provided by hammer interlock AZ-19 and associated circuits. See figure 4-12 for a functional block diagram of hammer interlock AZ-19 and associated circuits.

4-62 HAMMER INTERLOCK AZ-19. Hammer interlock AZ-19 contains a 10-second delay, voltage monitor, voltage clamp (VCL) control and regulator, associated logic, and three lamp driver circuits. These perform the following interlock and fault detect functions:

- a. Drum gate
- b. Paper out
- c. VCL and +5v supplies
- d. Print inhibit

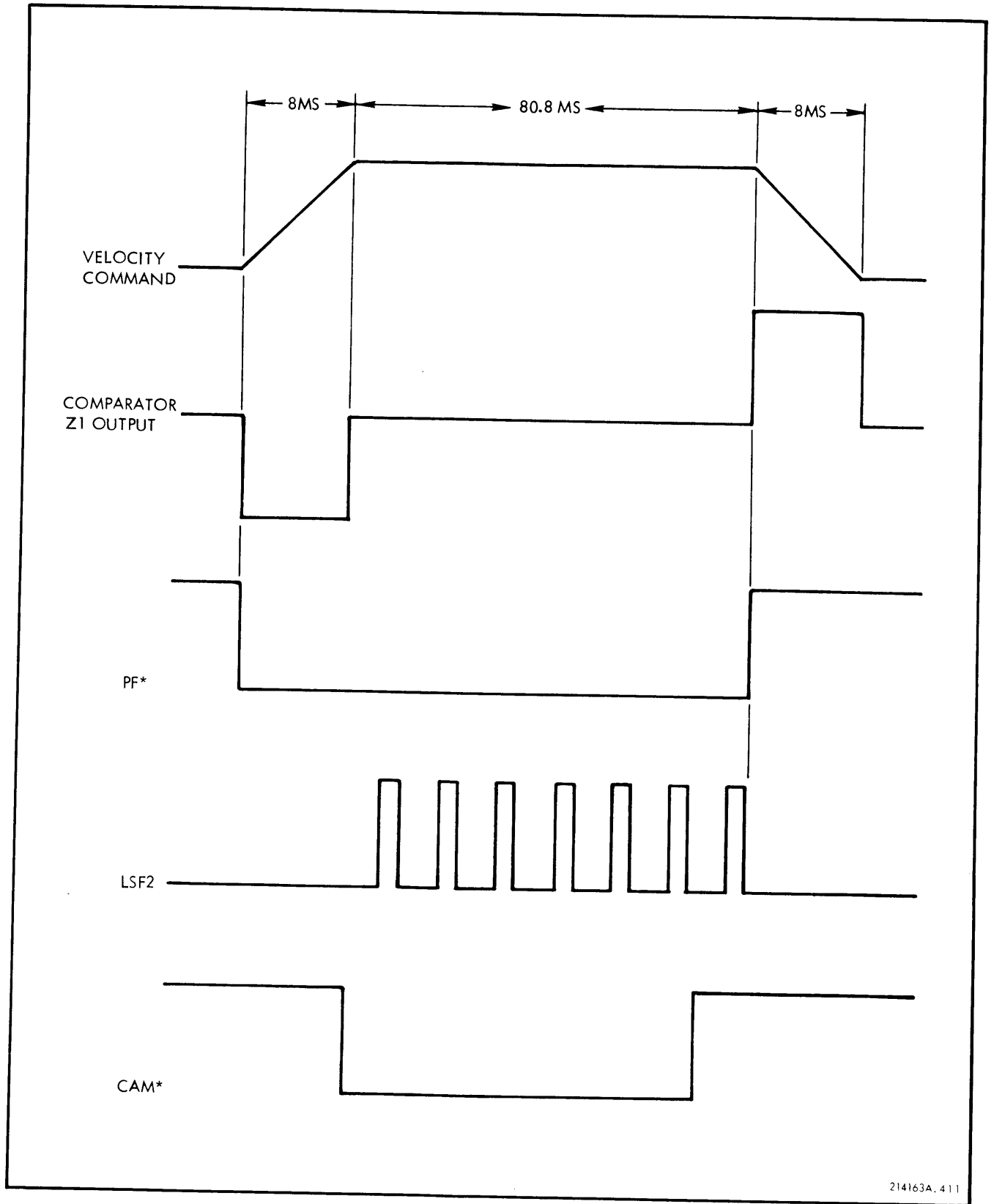


Figure 4-11. Top-of-Form Advance Timing Diagram

Table 4-5. Code/Character Relationship (Continued)

Input Character		Row On Drum	Character Counter	Remarks
Decimal Code	Drum Character			
69	E	38	69	Printable Character ↑ ↓ Printable Character Nonprintable
70	F	39	70	
71	G	40	71	
72	H	41	72	
73	I	42	73	
74	J	43	74	
75	K	44	75	
76	L	45	76	
77	M	46	77	
78	N	47	78	
79	O	48	79	
80	P	49	80	
81	Q	50	81	
82	R	51	82	
83	S	52	83	
84	T	53	84	
85	U	54	85	
86	V	55	86	
87	W	56	87	
88	X	57	88	
89	Y	58	89	
90	Z	59	90	
91	[	60	91	
92	\	61	92	
93	]	62	93	
94	↑	63	94	
95	←	64	95	
96-127	-	-	-	

4-197 Each time a character row passes the print station, as the drum revolves, CHCK\* initiates a new scan cycle and CHCK4 increments the counter one count. At count 79 (character 0) the first comparison is made and hammer register flip-flop 20 is set. One by one, the remaining characters in memory are compared for code 79 and if comparisons are made, their respective hammer register flip-flops are set. The next CHCK4 increments the counter to 80 and CHCK1 thru CHCK3 fire those hammers whose respective hammer register flip-flops have been set. In this manner, all columns containing the character 0 are printed simultaneously.

4-198 Each time the counter is incremented, another scan cycle is initiated and all comparisons are printed. The count continues to 95 (64th row), the counter resets to 32, and the operation described is repeated until all characters in memory are printed.

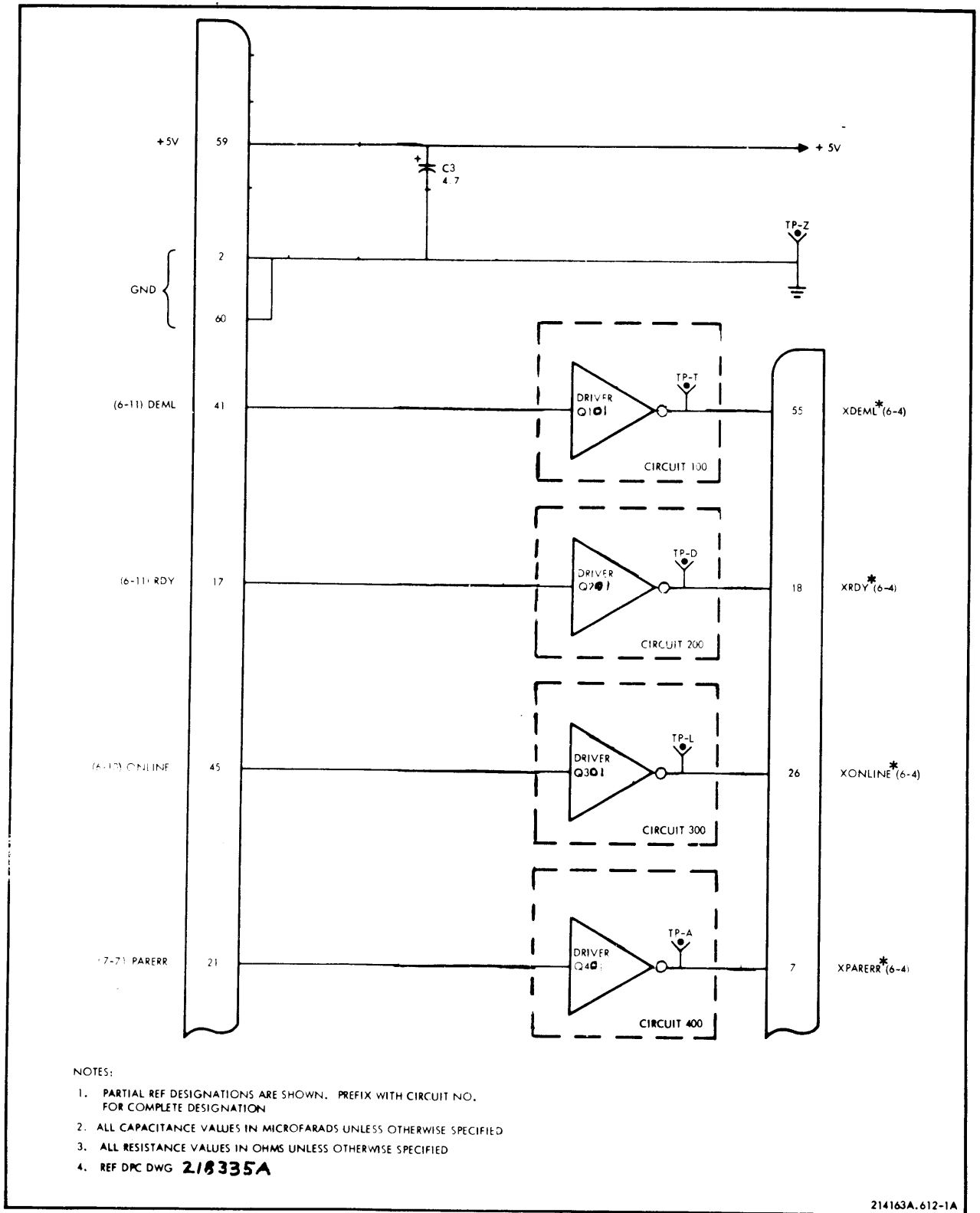
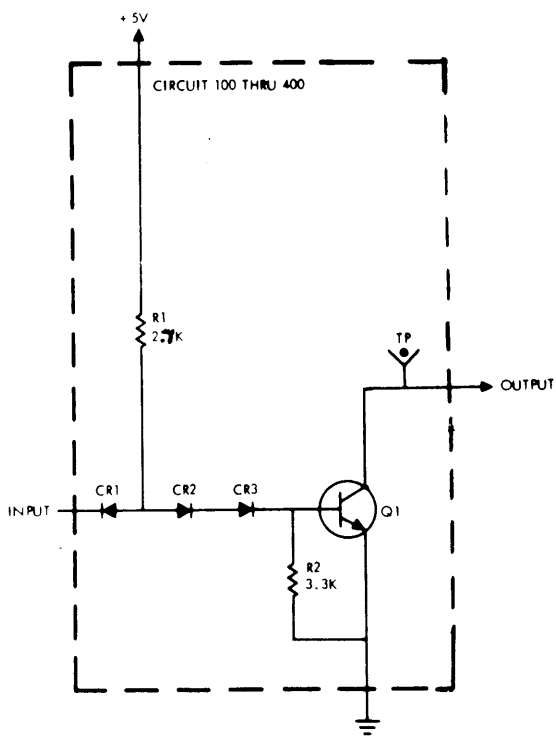


Figure 6-12. Open Collector Driver AJ-21 Schematic Diagram (Sheet 1 of 2)





214163A.612-28

Figure 6-12. Open Collector Driver AJ-21 Schematic Diagram (Sheet 2 of 2)

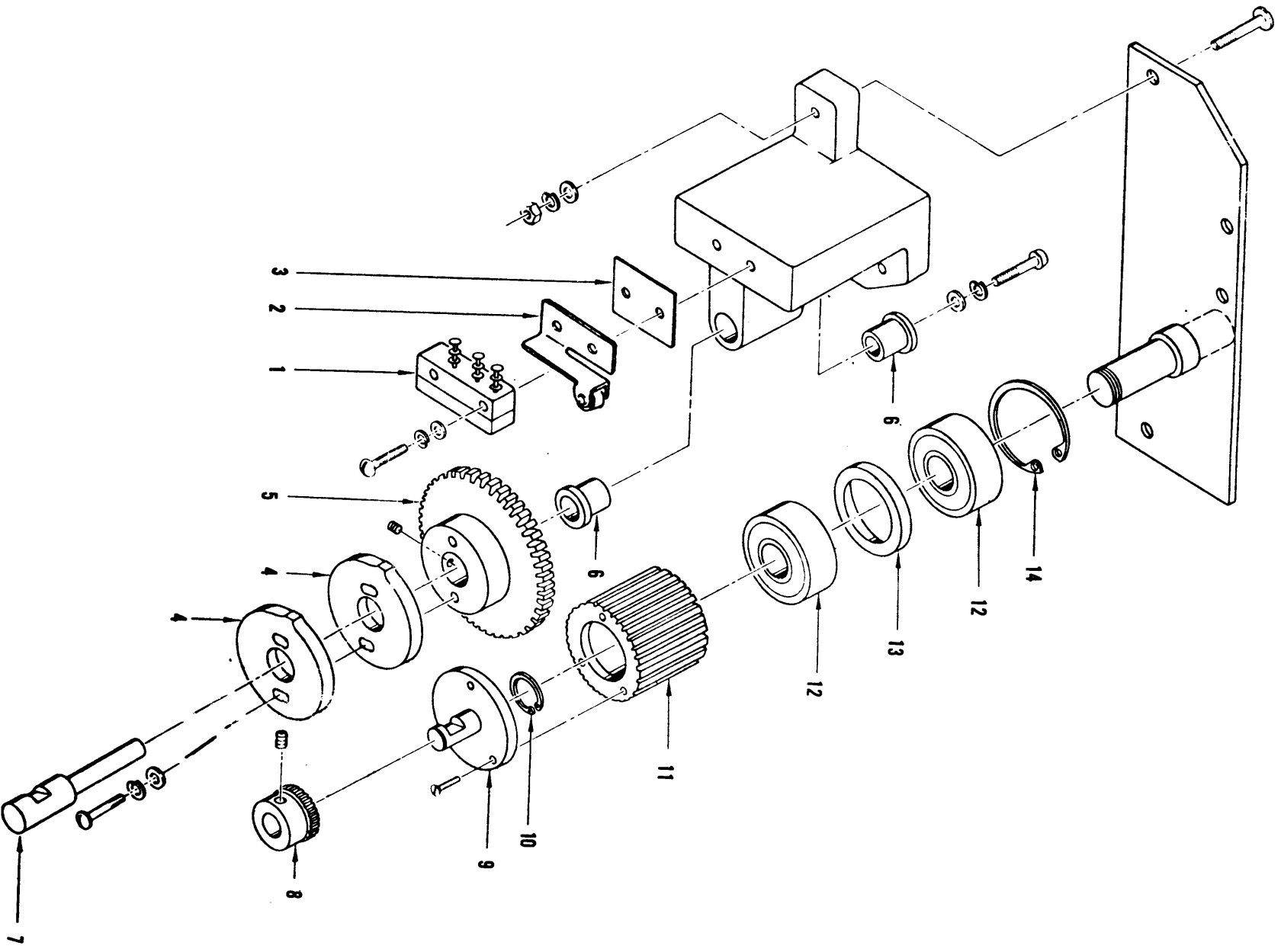


Figure 9-5. Top of Form Assembly

TABLE 9-5. TOP OF FORM SUB-ASSEMBLY

Figure & Index No.	Description	Reference Designator	Part No.	Qty
Fig. 9-5	Top Of Form Sub-Assembly		212660-1	1
-1	Switch, Micro, SPDT		800129-001	1
-2	Actuator, Leaf & Roller		800130-001	1
-3	Insulator, Switch		800129-001	
-4	Cam, Top Of Form		212663-1	2
-5	Gear, Spur, Delrin, 108-Teeth		214837-1	1
-6	Bushing, Flanged, Oilless		800185-002	2
-7	Shaft, Top Of Form		212668-1	1
-8	Gear, Spur, 44-Teeth		800508-044	1
-9	Mount, Gear		212666-1	1
-10	Ring, Retaining, External		800253-035	1
-11	Sprocket, 22G, Top Of Form		212664-1	1
-12	Bearing, Ball, Radial, Type 30		800181-001	2
-13	Spacer, Bearing, Top Of Form		212665-1	1
-14	Ring, Retaining, Internal		800252-102	1

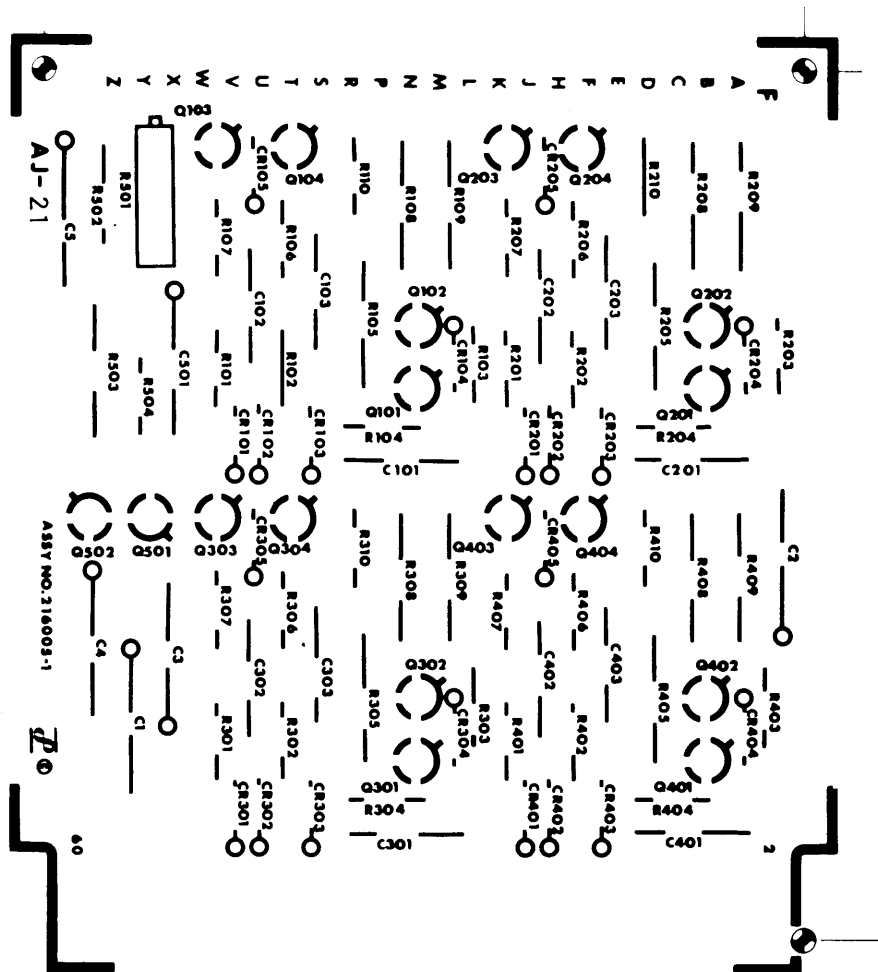


Figure 9-28. Driver, AJ21, Circuit Card Assembly

TABLE 9-28. DRIVER AJ-21 ASSEMBLY REPLACEABLE PARTS

Figure & Index No.	Description	Reference Designator	Part No.	Qty
Fig. 9-28	Circuit Card Assembly, AJ-21 Driver		218334-1	Ref
	Printed Wiring Board		216006-1	1
	Capacitor, 4.7 Uf, ±10%, 20V	C3	800041-475	1
	Resistor, 2.7K, ±5%, 1/4W	R101, R201, R301, R401	800030-272	4
	Resistor, 3.3K, ±5%, 1/4W	R102, R202, R302, R402	800030-332	4
	Transistor	Q101, Q201, Q301, Q401	800132-001	4
	Diode	CR101, CR201, CR301, CR401, CR102, CR202, CR302, CR402, CR103, CR203, CR303, CR403	800093-001	12
	Wire, Insulated, 30 AWG	W1, W2, W3, W4	800069-630	A/R
	Terminal	TP-Z	800155-002	1

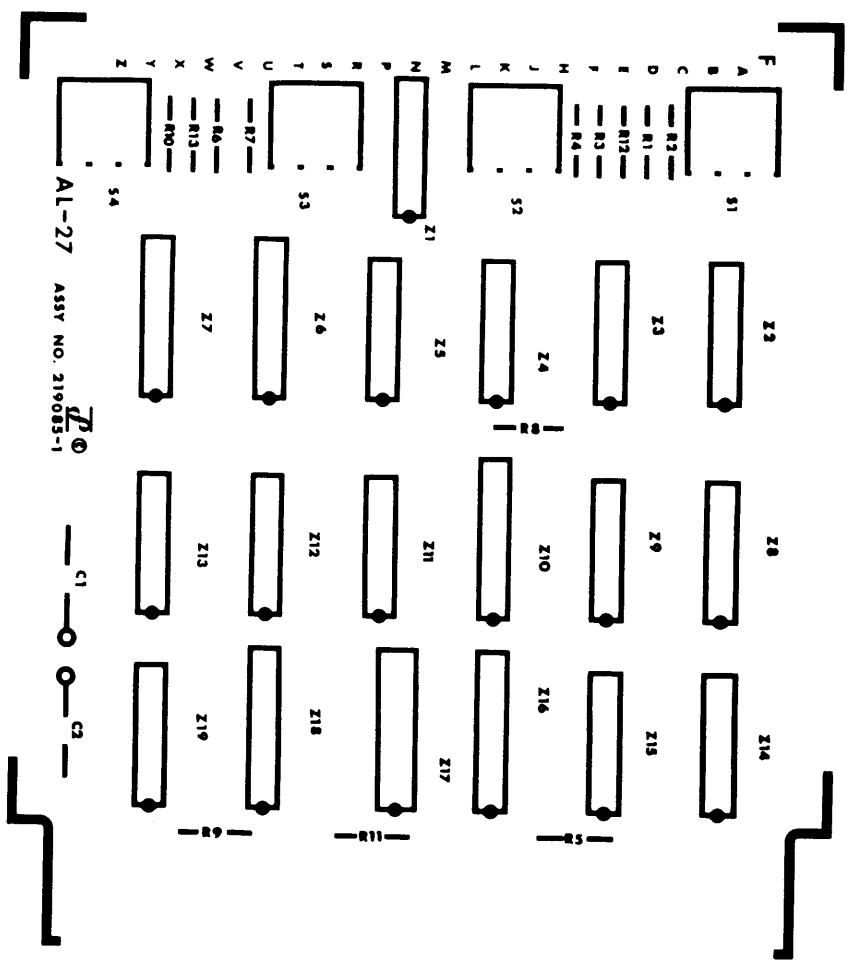
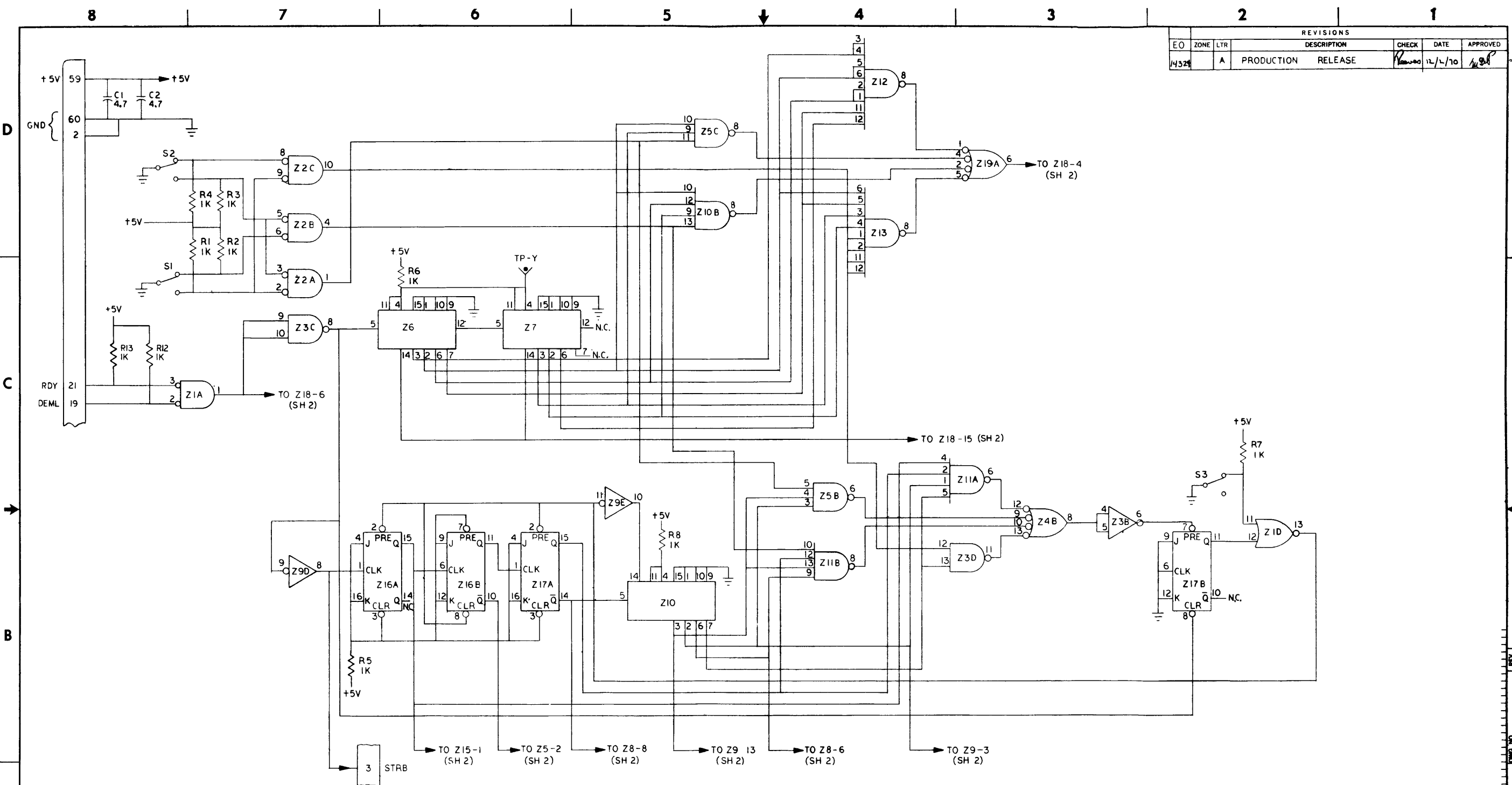


Figure 9-39. Self Test, AL-27, Circuit Card Assembly

TABLE 9-37. SELF-TEST AL-27 ASSEMBLY REPLACEABLE PARTS

Figure & index No.	Description	Reference Designator	Part No.	Qty
Fig. 9-39	Circuit Card Assembly, AL-27 Self Test		219085-1	Ref
	Printed Wiring Board		219086-1	1
	Capacitor, 4.7 Uf, $\pm 20\%$ , 10V	C1,C2	800091-475	2
	Resistor, 1K, $\pm 5\%$ , 1/4W	R1,R2,R3,R4, R5,R6,R7,R8, R9,R10,R11, R12,R13	800030-102	13
	Switch	S1,S2,S3,S4	800502-001	4
	Integrated Circuit	U1,U2,U8	800080-001	3
	Integrated Circuit	U3,U15	800024-001	2
	Integrated Circuit	U4,U11,U19	800020-001	3
	Integrated Circuit	U5	800023-001	1
	Integrated Circuit	U6,U7,U10	800386-001	3
	Integrated Circuit	U9	800387-001	1
	Integrated Circuit	U12,U13	800021-001	2
	Integrated Circuit	U14	800393-001	1
	Integrated Circuit	U16,U17,U18	800081-001	3
Wire, Solid, 24 AWG	W1,W2	800156-024	A/R	
Tubing, 24 AWG		800157-024	A/R	



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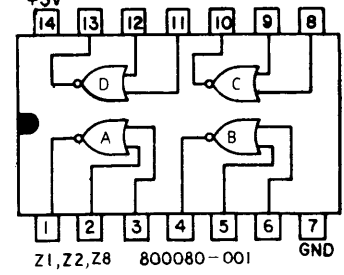
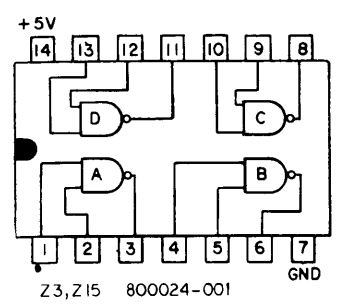
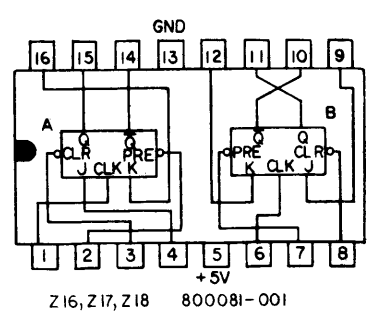
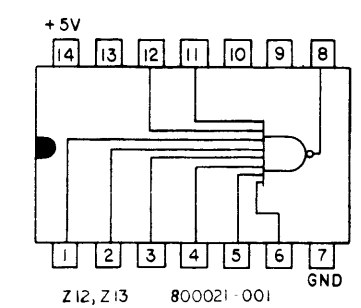
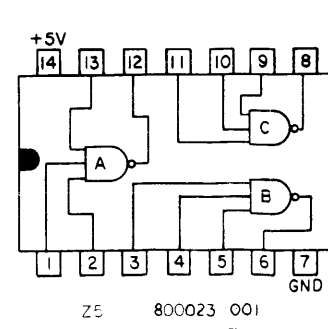
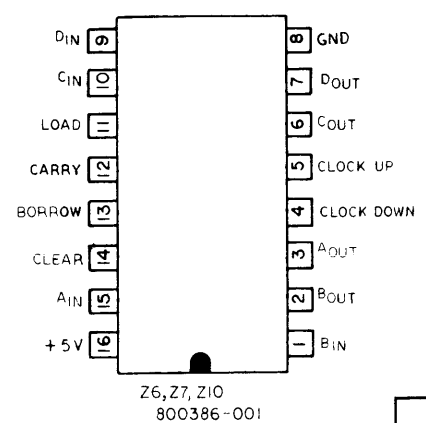
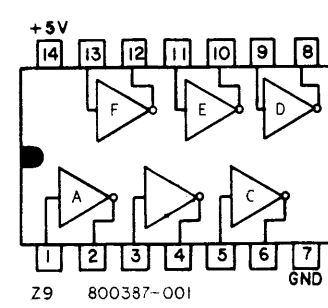
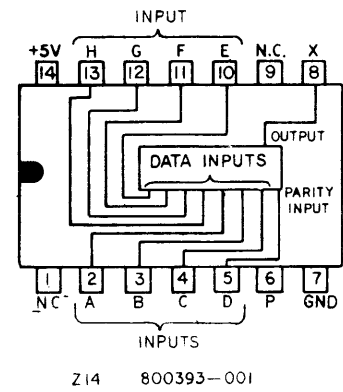
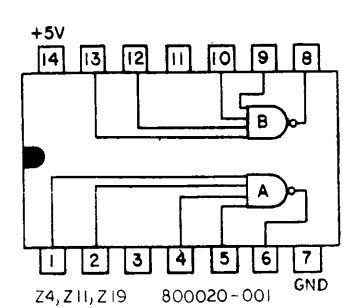
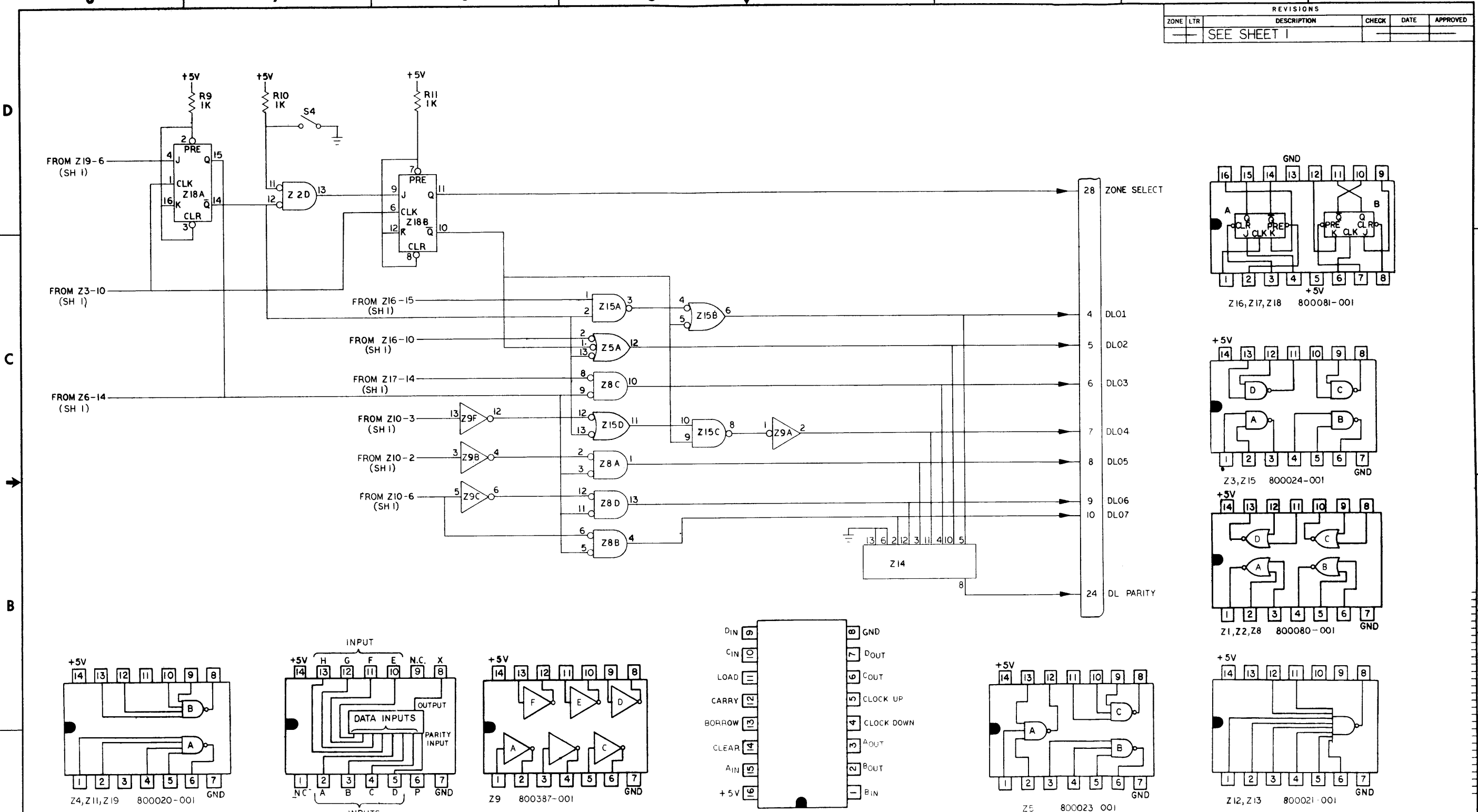
9. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH CIRCUIT NO.
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 1, 11 THRU 18, 20, 22, 23, 25, 26, 27, 29 THRU 58.
7. ASSEMBLY DRAWING NUMBER 219085
6. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
4. ~~ALL TRANSISTORS ARE~~
3. ~~ALL DIODES ARE~~
2. AL. CAPACITANCE VALUES ARE IN MICROFARADS, 20%, 10 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.
- NOTES: UNLESS OTHERWISE SPECIFIED**

SUPPLEMENTARY INFORMATION FIRST USED ON MODEL <p style="text-align: center;">2310</p> NEXT ASSEMBLY		DO NOT SCALE DRAWING UNLESS OTHERWISE NOTED: 1. COM. TO L. APPLY TO STOCK SIZES. 2. ALL DIMENSIONS ARE IN INCHES. 3. BREAK ALL SHARP EDGES. 4. DIMENSIONS APPLY AFTER FINISHING, HEAT TREATING AND PLATING. 5. TOLERANCES: XX ± .03 ANGULAR ± 1/2° XXX ± .010 6. MACH SURFACE ✓		<table border="1"> <tr> <td>DR</td> <td>[Signature]</td> <td>11-19-70</td> </tr> <tr> <td>CHK</td> <td>[Signature]</td> <td>12/1/70</td> </tr> <tr> <td>APP</td> <td>[Signature]</td> <td>12/1/70</td> </tr> <tr> <td>APP</td> <td></td> <td></td> </tr> <tr> <td>MATL</td> <td></td> <td></td> </tr> <tr> <td>FINISH</td> <td></td> <td></td> </tr> </table>		DR	[Signature]	11-19-70	CHK	[Signature]	12/1/70	APP	[Signature]	12/1/70	APP			MATL			FINISH			<table border="1"> <tr> <td colspan="2" style="text-align: center;"><b>data products</b></td> </tr> <tr> <td colspan="2" style="text-align: center;">WOODLAND HILLS, CALIFORNIA</td> </tr> <tr> <td colspan="2" style="text-align: center;">TITLE</td> </tr> <tr> <td colspan="2" style="text-align: center;">SCHEMATIC, AL-27 SELF TEST</td> </tr> <tr> <td>SIZE</td> <td>CODE IDENT NO.</td> <td>DRAWING NO.</td> <td>REV</td> </tr> <tr> <td>D</td> <td>19790</td> <td>219089</td> <td>A</td> </tr> <tr> <td colspan="2">SCALE NONE</td> <td colspan="2">SHEET 1 OF 2</td> </tr> </table>		<b>data products</b>		WOODLAND HILLS, CALIFORNIA		TITLE		SCHEMATIC, AL-27 SELF TEST		SIZE	CODE IDENT NO.	DRAWING NO.	REV	D	19790	219089	A	SCALE NONE		SHEET 1 OF 2	
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REV. A  
 219089



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		SEE SHEET 1			



SUPPLEMENTARY INFORMATION FIRST USED ON MODEL <b>2310</b> NEXT ASSEMBLY		DO NOT SCALE DRAWING UNLESS OTHERWISE NOTED: 1. COML TOL APPLY TO STOCK SIZES. 2. ALL DIMENSIONS ARE IN INCHES. 3. BREAK ALL SHARP EDGES. 4. DIMENSIONS APPLY AFTER FINISHING, HEAT TREATING AND PLATING. 5. TOLERANCES: XX ± .03 ANGULAR ± 1/2° XXX ± .010 6. MACH SURFACE ✓		DR: <i>M. L. Kon</i> 11-19-70 CHK: APP: APP: MATL: FINISH:		 WOODLAND HILLS, CALIFORNIA TITLE <b>SCHEMATIC, AL-27 SELF TEST</b> SIZE: <b>D</b> CODE IDENT NO.: <b>19790</b> DRAWING NO.: <b>219089</b> REV: <b>A</b> SCALE: NONE SHEET 2 OF 2	
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CONTENTS

VOLUME 11

<u>Section</u>	<u>Title</u>	<u>Page</u>
IX	MECHANICAL ILLUSTRATIONS	
	Introduction .....	9-1/2

LIST OF ILLUSTRATIONS

<u>Figure</u>	<u>Title</u>	<u>Page</u>
9-1	Line/Printer Assembly .....	9-3/4
9-2	Mechanics Assembly .....	9-9/10
9-3	Mechanics Frame Assembly .....	9-13/14
9-4	Control Panel Assembly .....	9-17
9-5	Top of Form Assembly .....	9-19
9-6	Female Latch Sub-Assembly .....	9-21
9-7	Paper Drive Sub-Assembly .....	9-23
9-8	Vertical Paper Adjust Assembly .....	9-25
9-9	Power Supply Assembly .....	9-27
9-10	Drum Gate Assembly, 64-Character .....	9-33/34
9-11	Drum Sub-Assembly, 64-Character .....	9-39
9-12	Drum Gate Assembly, 96-Character .....	9-41/42
9-13	Drum Sub-Assembly, 96-Character .....	9-47
9-14	Card Cage Assembly .....	9-49/50
9-15	Hammer Bank Assembly .....	9-52
9-16	Hammer Bank Harness Assembly .....	9-54
9-17	Main Harness Assembly .....	9-56
9-18	In/Out Harness Assembly .....	9-58
9-19	Static Eliminator Assembly .....	9-60
9-20	Character Memory, AM-10, Circuit Card Assembly .....	9-62
9-21	Character Memory, AM-21, Circuit Card Assembly .....	9-66
9-22	Logic Gate I, AG-17, Circuit Card Assembly .....	9-68
9-23	Logic Gate II, AG-18, Circuit Card Assembly .....	9-70
9-24	Logic Gate III, AG-45, Circuit Card Assembly .....	9-72
9-25	Logic Gate IV, AG-20, Circuit Card Assembly .....	9-74
9-26	Timing Control, AT-13, Circuit Card Assembly .....	9-76
9-27	Delay Control and Gates, AG-32, Circuit Card Assembly ..	9-78
9-28	Driver, AJ-21, Circuit Card Assembly .....	9-80
9-29	Not Assigned	
9-30	Not Assigned	
9-31	Receiver, AK-10, Circuit Card Assembly .....	9-89
9-32	Inverting Receiver, AK-11, Circuit Card Assembly .....	9-92
9-33	Transducer Amplifier, AS-13, Circuit Card Assembly .....	9-95

CONTENTS (Cont'd)

LIST OF ILLUSTRATIONS (Cont'd)

<u>Figure</u>	<u>Title</u>	<u>Page</u>
9-34	Hammer Interlock, AZ-19, Circuit Card Assembly .....	9-98
9-35	Zone Control, AZ-18, Circuit Card Assembly .....	9-102
9-36	Hammer Driver, AH-10, Circuit Card Assembly .....	9-105
9-37	Cable Plug, AZ-14, Circuit Card Assembly .....	9-109
9-38	Cable Plug, AZ-85, Circuit Card Assembly .....	9-110
9-39	Self Test, AL-27, Circuit Card Assembly .....	9-111
9-40	Parity, AL-11, Circuit Card Assembly .....	9-113
9-41	Zone Select, AL-12, Circuit Card Assembly .....	9-115
9-42	Paper Feed Control, AP-10, Circuit Card Assembly .....	9-117
9-43	Voltage Regulator, AV-10, Circuit Card Assembly .....	9-121
9-44	Ribbon Control, AZ-84, Circuit Card Assembly .....	9-125
9-45	SCR Commutating Board, AZ-79, Circuit Card Assembly ....	9-128
9-46	Power Amplifier, AZ-49, Circuit Card Assembly .....	9-130
9-47	Negative Paper Feed Power Amplifier, AZ-51, Circuit Card Assembly .....	9-132
9-48	Bridge Board, AZ-78, Circuit Card Assembly .....	9-134
9-49	Not Assigned	9-136
9-50	Code Conversion, AD-28, Circuit Card Assembly .....	9-139

LIST OF TABLES

<u>Table</u>	<u>Title</u>	<u>Page</u>
9-1	Line/Printer Assembly .....	9-7/8
9-2	Mechanics Assembly .....	9-11
9-3	Mechanics Frame Assembly .....	9-15
9-4	Control Panel Assembly .....	9-18
9-5	Top of Form Assembly .....	9-20
9-6	Female Latch Sub-Assembly .....	9-22
9-7	Paper Drive Sub-Assembly .....	9-24
9-8	Vertical Paper Adjust Assembly .....	9-26
9-9	Power Supply Assembly .....	9-30
9-10	Drum Gate Assembly, 64-Character .....	9-37
9-11	Drum Sub-Assembly, 64-Character .....	9-40
9-12	Drum Gate Assembly, 96-Character .....	9-45
9-13	Drum Sub-Assembly, 96-Character .....	9-48
9-14	Card Cage Assembly .....	9-51
9-15	Hammer Bank Assembly .....	9-53
9-16	Hammer Bank Harness Assembly .....	9-55
9-17	Main Harness Assembly .....	9-57
9-18	In/Out Harness Assembly .....	9-59
9-19	Static Eliminator Assembly.....	9-61

CONTENTS (Cont'd)

LIST OF TABLES (Cont'd)

<u>Table</u>	<u>Title</u>	<u>Page</u>
9-20	Character Memory, AM-10 Assembly Replaceable Parts .....	9-63
9-21	Character Memory, AM-21 Assembly Replaceable Parts .....	9-67
9-22	Logic Gate I, AG-17 Assembly Replaceable Parts .....	9-69
9-23	Logic Gate II, AG-18 Assembly Replaceable Parts .....	9-71
9-24	Logic Gate III, AG-45 Assembly Replaceable Parts .....	9-73
9-25	Logic Gate IV, AG-20 Assembly Replaceable Parts .....	9-75
9-26	Timing Control, AT-13 Assembly Replaceable Parts .....	9-77
9-27	Delay Control and Gates, AG-32 Assembly Replaceable Parts .....	9-79
9-28	Driver, AJ-21, Assembly Replaceable Parts.....	9-81
9-29	Not Assigned	9-84
9-30	Not Assigned	9-87
9-31	Receiver, AK-10 Assembly Replaceable Parts .....	9-90
9-32	Inverting Receiver, AK-11 Assembly Replaceable Parts ...	9-93
9-33	Transducer Amplifier, AS-13 Assembly Replaceable Parts .....	9-96
9-34	Hammer Interlock, AZ-19 Assembly Replaceable Parts .....	9-99
9-35	Zone Control, AZ-18 Assembly Replaceable Parts .....	9-103
9-36	Hammer Driver, AH-10 Assembly Replaceable Parts .....	9-106
9-37	Self Test, AL-27 Assembly Replaceable Parts .....	9-112
9-38	Parity, AL-11 Assembly Replaceable Parts .....	9-114
9-39	Zone Select, AL-12 Assembly Replaceable Parts .....	9-116
9-40	Paper Feed Control, AP-10 Assembly Replaceable Parts ...	9-118
9-41	Voltage Regulator, AV-10 Assembly Replaceable Parts ....	9-122
9-42	Ribbon Control, AZ-84 Assembly Replaceable Parts .....	9-126
9-43	SCR Commutating Board, AZ-79 Assembly Replaceable Parts .....	9-129
9-44	Power Amplifier, AZ-49 Assembly Replaceable Parts .....	9-131
9-45	Negative Paper Feed Power Amplifier, AZ-51 Assembly Replaceable Parts .....	9-133
9-46	Bridge Board, AZ-78 Assembly Replaceable Parts .....	9-135
9-47	Not Assigned	9-137
9-48	Code Conversion, AD-28 Assembly Replaceable Parts .....	9-140

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