HP 3000 Computer Systems

HP 3000 SERIES 44
AND HP 3000 SERIES 40
COMPUTER SYSTEMS

Reference/Training Manual

COMPUTER SYSTEMS DIVISION, 19447 PRUNERIDGE AVE., CUPERTINO, CALIFORNIA 95014

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PREFACE

This manual contains hardware information for the HP 3000 Series 44 and HP 3000 Series 40 Computer Systems. Specifically, this manual contains perequisite reading material for all personnel that attend Hewlett-Packard training courses related to these systems. Since the information contained in this manual is approximately the same as that presented during classroom lectures, this manual should be retained for classroom reference, review, and note-taking purposes.

The HP 3000 Series 44 and HP 3000 Series 40 Computer Systems are functionally the same, differing only in physical characteristics and power supplies. Since both systems utilize the same hardware and operating system, and can be operated identically, this manual is divided into two parts. Part 1 consists of detailed information for HP 3000 Series 44 and that which is common to both systems. Part 2 contains information that applies only to the HP 3000 Series 40. References are made from Part 2 to Part 1 for information common to both systems.

Additional Hewlett-Packard documents that may be used during the training course and for on-site references are:

HP 3000 Series 40 Installation Manual, P/N 30090-90002

HP 3000 Series 40 System Block Diagram, P/N 30090-90003

HP 3000 Series 40 U Code Listing, P/N 30090-90004

HP 3000 Series 40 CMP Self Test Manual, P/N 30090-90005

HP 3000 Series 40 CMP Remote Maintenance Manual, P/N 30090-90006

HP 3000 Series 40 CMP Maintenance Mode Manual, P/N 30090-90007

HP 3000 Series 40 Pronto Memory Diagnostic Manual, P/N30090-90001

HP 3000 Series 40 Upgrade Installation Manual, P/N 30090-90008

HP 3000 Series 40 Engineering Diagram Set, P/N 30090-90009

HP 3000 Series40 Memory Add-On Installation Manual,P/N30090-90002

HP 3000 Series 40 30087A Upgrade Kit Installation Guide,
m85 P/N 30079A-90002

HP 3000 Series 40 300079A Add-On Installation Manual,
P/N 30079A-90002

HP 3000 Series 44 Installation Manual, P/N 30170-90002

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GENERAL SPECIFICATIONS

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SECTION I

HP 3000 SERIES 44

GENERAL SPECIFICATIONS

1-1. PHYSICAL DIMENSIONS

Height	28.5 in. (72.4 cm)
Depth	31.25 in. (79.4 cm)
Width	72.25 in. (183.5 cm))
Weight (uncrated)	240 lbs (109 kg)
Weight (shipping)	310 lbs (141 kg)g)

1-2. POWER REQUIREMENTS

Voltages	200 to 240 VAC in 10 volt steps (+4%, -10%)
Frequency	60 and 50 Hz (+/- 0.5 Hz)
Current (at full load)	
Single Card Cage:	8.3A at 208 VAC for 60 Hz, 8.1A at 220 VAC for 50 Hz
Dual Card Cage:	13.1A at 208 VAC for 60 Hz 12.4A at 220 VAC for 50 Hz
Power (at full load)	
Single Card Cage:	1280 watts at 60 Hz, 1400 watts at 50 Hz
Dual Card Cage:	2160 watts at 60 Hz, 2220 watts at 50 Hz
Circuit Breaker Rating	24A
Power Connection	Power cord supplied with 60 Hz models. No power cord supplied with 50 Hz models.

1-3. ENVIRONMENTAL

Temperature

Operating

System (recommended):	68 to 78 deg F (20 to 25.5 deg C)
(maximum, 48 hrs):	86 deg F (30 deg C)
(minimum, 48 hrs):	55 deg F (15 deg C)
Non-operating (maximum):	167 deg F (75 deg C)
(minimum):	-40 deg F (-40 deg C)
Rate of Change	10 deg F/hr (4.5 deg C/hr)

Relative Humidity

Recommended operating:	40 to 60 percent (no condensation)
Non-operating	5 to 80 percent

Altitude

Operating	Sea level to 4600m (15,000 ft)
Non-operating	Sea level to 15,300m (50,000 ft)

1-4. PROCESSOR

Word Length	16 bits
Number of instructions	195
Minor clock cycle time	26.3 ns
Microinstruction Cycle Time	105 ns (four minor clocks)
Physical Address Space	18 Mbytes
Maximum Code Segment Size	16 Kwords
Maximum Data Segment Size	32 Kwords
Maximum Number of User Code Segments	63
Maximum Number of User Data Segments	256
Decimal Precision	28 digits
Major Clock Cycle Time	100 ns
Minor Clock Cycle Time	25 ns
Real-Time Clock Resolution	1 ms

Note: The microinstructions require four major clock cycles, however, each microinstruction overlaps so that a new one starts every major clock cycle.

1-5. MEMORY

Semiconducor memory with single-bit error correction and double-bit error detection.

Word Length	39 bits (32 + 7 for error correction/detection)
Error Detection	2 bits per 32-bit word
Error Correction	1 bit per 32-bit word
Memory Module Size	256 kbyte (using 16k RAMS) 1 Mbyte (using 64k RAMS)
Maximum Memory Size per card cage	2 Mbyte (using 16K RAMS)
Per System	8 Mbyte (using 64k RAMS)
Maximum Modules per Controller	8
Read Access Time	300 ns (worst case ADO to DDN)
Battery Backup Time	15 minutes

1-6. INPUT/OUTPUT STRUCTURE

Common asynchronous bus structure with individual data channels.

Maximum Number of Data Channels	15
Channel Types:	
General I/O Channel (for HP-IB compatible devices)	5 per system, maximum
Maximum number of devices	8 per channel
Maximum transfer rate	980 kbytes/s
Maximum total cable length	13m (50 ft)
Asynchronous Data Communication Channel (for asynchronous RS-232-C compatible devices)	16 maximum
Maximum number of ports per system	60
Number of ports per channel	8 (4 on Main and 4 on Extender)
Data rates	50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600 Baud
Maximum data cable length	30.5m (100 ft)

SECTION II

SYSTEM CONTROL PANEL AND SYSTEM CONSOLE

FUNCTIONAL DESCRIPTION

2-1. INTRODUCTION

This section describes the system control panel and the system console keys that relate to the control panel functions.

2-2. SYSTEM CONTROL PANEL

The system control panel (figure 2-1) is a module that contains the necessary circuits on two PCAs to perform the control and monitoring functions of the HP 3000/44 Computer System. The module is located behind the front door, which is normally locked. A beveled slot in the front door exposes two indicators, the POWER indicator and the REMOTE CONSOLE indicator.

The system control panel contains hardware-related and software-related controls. Also, indicators monitor the status of the system and power supplies. The two hardware-related controls are RUN and HALT. While the system is running, the CPU will respond only to the HALT control. The software-related controls are START (warmstart), DUMP (memory dump), and LOAD (cold-load). Up to eight channels and eight devices on each channel can be addressed for a cold-load, warmstart, or memory dump. The channel and device addresses are set by the thumbwheel switches located directly under the START, DUMP, and LOAD switches. The addresses are gated out when the respective momentary switch is pressed.

The system control panel includes four other switches. These switches are used to configure the system disc, enable or disable maintenance mode on the system console, enable or disable the remote console capability, and enable or disable the system console functions that duplicate the control functions on the system control panel.

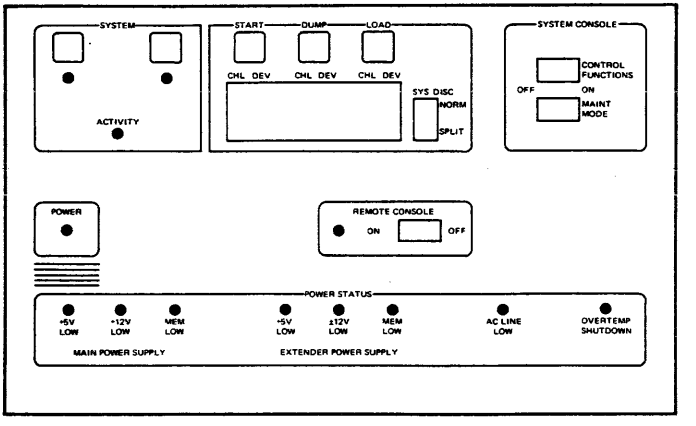

Figure 2-1. System Control Panel

2-3. Switch Functions

- HALT Switch

  This is a momentary switch that causes the CPU to halt if it is in the run state. There is no response if the CPU is halted.

Control Panel/Console

- RUN Switch

  This is a momentary switch that causes the CPU to go from the halt state to the rin state. There is no response if the CPU is in the run state.

- LOAD, START, and DUMP Switches

  Each function has one momentary switch and two associated thumbwheel switches. The thumbwheel switches select the channel and device addresses, and the momentary switch gates the selected address out on the channel and device lines to the CPU. Each channel switch wheel is marked 4 through 11. The corresponding BCD outputs sent to the CPU will be 0 through 7. The CPU adds 4 to the channel number so that the result will be the same as the switch marking. This numbering scheme is used so that channels 0 through 3 can be reserved for terminal use. The device number switches are marked 0 through 7 and the corresponding BCD outputs are also 0 through 7.

- SYS DISC Switch

  This is a two-position switch that configures either a fixed disc or removable discs as the warmstart devices of the system disc. For example, with the switch set to NORMAL the warmstart microcode will address head zero of the system disc drive. When the switch is set to SPLIT, the microcode addresses head two of the system disc drive.

- CONTROL FUNCTIONS Switch

  This is a two-position switch that, when set to ON, enables the console functions. These functions include the system control panel functions, such as START, DUMP, LOAD, RUN, and HALT. When set to OFF, the console functions are disabled.

- MAINT MODE Switch

  The output of this switch is sent to the Control and Maintenance Processor to enable the system console maintenance mode.

- REMOTE CONSOLE Switch

  This switch enables the remote console capability.

2-4. Indicator Lights

Three SYSTEM indicators display system status. The RUN indicator is a yellow LED that is lit when the CPU is operating. The ACTIVITY indicator is also a yellow LED that provides a visual indication of IMB activity. The HALT indicator is a red LED that lights when the CPU is in the halt state.

The POWER and REMOTE CONSOLE indicators are visible through the front panel door window when lit. The POWER indicator is a yellow LED and represents DC power integrity. The REMOTE CONSOLE indicator is a red LED that is lit when the remote console facility is enabled.

Two warning indicators are included on the front panel. The AC LOW indicator is a red LED that lights when the system switches to battery backup power. The OVERTEMP indicator lights red when the temperature exceeds the threshold (135 degrees F/57.3 degrees C) of any temperature transducer in either card cage. The LED is reset by momentarily turning off then on the AC circuit breaker.

Two groups of power supply LEDs provide status of the power supplies for the main card cage and the extender card cage. The LEDs are off during normal operation. If a failure occurs in a particular power supply, the corresponding LED lights.

2-5. SYSTEM CONSOLE

The system console may be any of the 264X or 262X terminals, or an HP hard copy terminal such as the HP 2635 printing terminal. The system console appears to the operating system as a standard system console and displays normal MPE console information. The console can also be used as a session device. In addition, system status is displayed, and the console keys can be used for duplicating certain control panel functions.

The console control functions that include the system control panel functions are implemented by entering CNTL B, waiting for a prompt " -> ", then entering the command. The commands are entered fully spelled out. When the system is halted, the prompt is automatically displayed.

Console operator commands, session modes, and system manager operations are the same as that for all previous HP 3000 computer system operations.

2-6. Console Control Functions

The console control functions are listed as follows:

- HELP — This command prints a list of control and maintenance processor (CMP) commands.

- HALT — This causes the CPU run/hat flip-flop to be set to HALT. This function duplicates the halt function on the system control panel.

- RUN — This causes the CPU run/halt flip-flop to be set to RUN. This function duplicates the the run function on the system control panel.

- DUMP — This initiates the dump command, loading the soft-dump facility from the device specified by the thumbwheel switch. When the command is entered and the system is in the run mode, the following message will be displayed:

  "IS IT OK TO ABORT THE OPERATING SYSTEM?"

  The user must respond "YES" to perform the dump. This command duplicates the same command on the system control panel.

- LOAD — This causes the cold load function to be performed from the channel and device thumbwheel switches. When this command is entered and the system is in the run mode, the following message will be displayed:

  "IS IT OK TO ABORT THE OPERATING SYSTEM?"

  The user must enter "YES" to perform the load. This command duplicates the same command on the system control panel.

- START — This causes the warmstart function to be performed from the device specified by the thumbwheel switches. When this command is entered and the system is in the run mode, the following message will be displayed:

  "IS IT OK TO ABORT THE OPERATING SYSTEM?"

  The user must enter "YES" to perform the warmstart. This command duplicates the same command on the system control panel.

- SELFTEST — This command initiates the system selftest function. When this command is entered and the system is in the run mode, the following message will be displayed:

  "IS IT OK TO ABORT THE OPERATING SYSTEM?"

  The user must enter "YES" to perform the system selftest.

- LOG — This command displays a log of actions performed or detected by the CMP. These events are:

Display On	DISPLAY command entered
Dump	DUMP command entered
Halt	CPU went to halt
Halt Command	The HALT command was used
Iomap	IOMAP command entered
Load	LOAD command entered
Power On	Power-on reset to CMP when battery power was lost
Power Fail/Reset	A power fail occurred or the PON signal went low without loss of memory backup power
Run	CPU wne to run
Selftest OK	System selftest passed
Selftest Failed	System selftest failed
Shuttest	Power shutown test performed
Shuttest Failed	Power shuttdown test failed
Start	START command entered

These events are listed with the elapsed time (excluding power off duration) since the event occurred. The last 63 events are displayed. An example is:

```
      Event Log
Days Hrs Min       Since Event
  2   23  05       Power On
       3  20       Overtemp Shutdown
       3  20       Power Fail/Reset
       2  25       Halt
       2  20       Start Failed
       2  05       Halt
       2  03       Load Failed
       1  51       Halt
       1  50       Cold Load
       1  50       Selftest Failed
          03       Cold Load
          02       Load
```

- DISPLAY This command causes the maintenance display to appear on the screen.

- SPEED This command allows the user to change the baud rates when MPE is not running. The receive and transmit are specified in the command as follows:

  SPEED <RATE>,<RATE>

- :SPEED This command is identical to the SPEED command but allows the CMP and MPE to be set to the same speed simultaneously. This command is used when MPE is running.

- SHUTTEST This command test the power fail and overtemp shutdown circuitry on the CMP and power supply. When the command is entered, the message "Cycle Power to Restart System" is displayed. This shuts down all power except memory power. To bring the system up after this test cycle the main power breaker on system. If the test fails, the message "Test Failed" will appear on the screen.

- DCTEST This commands performs testing of the RS232 signals on the CMP. A special test adapter must be installed between J3 on the CMP and the standard CMP cable. The CMP cannot be in the remote mode while performing this test.

- IOMAP This command printsd the current system configuration. The memory size, control panel switches, and all channels and devices in the system are identified.

Invalid command names will cause the message "INVALID COMMAND, USE HELP FOR INFO" to be displayed.

SYSTEM OVERVIEW

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SECTION III

HP 3000 SERIES 44

SYSTEM OVERVIEW

3-1. INTRODUCTION

This section describes the HP 3000 Series 44 Computer System (figure 3-1). An overall system hardware description is provided with a description of the bus system and the I/O elements included. Bus control and command structure are also described.

The HP 3000/44 is designed around independent elements that are organized together through a communication network. The elements of the system consist of a central processor, memory arrays with a memory controller, I/O channels, and a bus system that enables communications between the elements. Also, the system includes a system console, system control panel, and a control and maintenance facility. Peripheral elements attach to the system through the I/O channels.

3-2. BUS SYSTEM

The elements that make up the bus system include the intermodule bus (IMB), the Hewlett-Packard Interface Bus (HP-IB), and the RS-232-C Data Communication Line.

3-3. Intermodule Bus

3-4. Bus Control. Communication between the CPU, Memory and I/O modules is carried over the IMB. Because the CPU generates greater than 90 percent of the Bus activity, it is given continuous access to the bus and relinquishes control to the I/O channels only on request.

The IMB has separate address and data paths each with handshake controls that operate in a master/slave mode to transfer data between modules. The CPU talks to memory and to the I/O system and always functions as a master. The GIC channels function as masters to memory but become slaves when talking with the CPU. To access memory, the I/O channels must request the bus through a priority structure. Any channel request will cause the CPU to reliquish control of the IMB so that the request can be serviced.

3-4. Bus Control. The bus control signals control access to the IMB and include the bus handshake signals. The lines that control bus access are BRQ (bus request), BACK (bus acknowledge), PRO (priority out), PRI (priority in), and PRCY (priority carry), the latter three of which are the priority tree signals for bus access. The handshake signals are discussed in later sections.

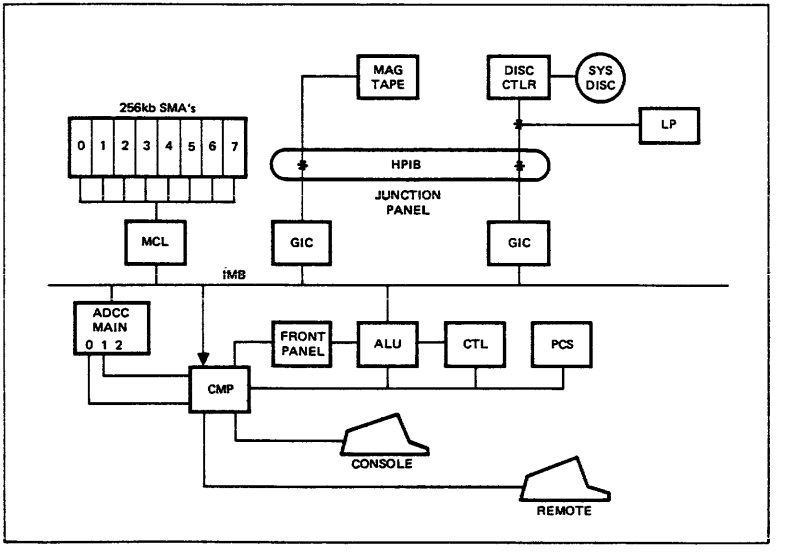


Figure 3-1. HP 3000 Series 44 Simplified Block Diagram

BRQ (Bus Request) Low True Open Collector

This is an OR-tieable line asserted by any channel to request access to the bus from the CPU. A true PRI input priority and BRQ high are required to assert a bus request.

BACK (Bus Acknowledge)

This is a unidirectional line that is driven by the CPU to acknowledge release of the bus to the channel asserting BRQ. The CPU releases BACK at the termination of the BRQ signal. Simultaneous bus requests are resolved by delaying the response to BRQ to allow for propogation through the priority chain for disabling the lower priority module.

PRI (Priority In) High True

The PRI's are input signals to the I/O channel and the AND of all ten must be true to be given access to the bus for memory service. On the channel card each PRI is pulled high to +5 volts through a 10K pull up resister. A tree structure is built into the backplane to establish priority as a function of physical location on the bus.

PRO (Priority Out) High True

This a normally true output signal from a module indicating lack of interest in the bus. This signal becomes one of the ten input PRI's to lower priority modules. By pulling PRO low, a channel requesting the bus can prevent access to the bus by lower priority channels.

PRCY (Priority Carry) High True

This is an output signal representing the AND of PRO of that module and the ten input PRI'S to the module. This signal is used on the backplane to restart the priority tree when the input PRI number reaches ten.

3-5. IMB I/O Commands. Interpretation of a channel instruction generally results in several transactions with a channel. It is necessary to specify IMB I/O commands in order to communicate the desired action to the channel. When the IMB operation is related to I/O (rather than memory), the sixteen low order IMB address lines assume a fixed format which is interpreted by the channel. (Refer to tables 3-1 and 3-2.)

The Addressing Mode indicates whether the command is addressed to a single channel or whether it is global and affects all channels. If bit 0 is a one the command is global. Commands that share code values are discerned by the three Bus Operation Code lines of the IMB, which specifies whether the operation is an I/O Read or an I/O Write.

The bus operation code lines are multiple source three-bit bus that carries the operation to be executed by the slave. The operations and their opcodes are as follows:

Operation	Opcode
Memory read word	000
Memory read/write 1's	001
Memory write word	010
Memory control/read status	101
I/O read	100
I/O write	110

Table 3-1. IMB I/O Commands

IMB Command	Mnemonic	IMB Operation	Opcode
Read Data	RIOC	read	0000
Obtain Interrupt Info	OBII	read	0010
Obtain Service Info	OBSI	read	0100
Service Poll 1	SPOLL1	read	1100
Write Data	WIOC	write	0000
Initialize Channel	INIT	write	0010
Start I/O Program	SIOP	write	0100
Halt I/O Program	HIOP	write	0110
I/O Clear	IOCL	write	1010

Table 3-2. IMB Command Code Format

0 3	4 7	8	9 12	13	14	15
Command Code	Register No.	x	Channel No.	x	x	x

Read Data (RIOC) and Write Data (WIOC)

The RIOC and WIOC commands are associated with several machine instructions as well as assorted tasks such as serial polling of devices on the GIC. These commands transport the information on the the IMB data lines from or to a particular channel. The commands are also used to select the source or destination (Register Number) of the data at the channel controller.

Interrupt Poll and Obtain Interrupt Information (OBII)

Interrupt Poll and OBII commands are issued by the CPU interrupt processing microcode to determine the number of the device whose interrupt request will be serviced. Interrupt Poll is issued in response to the IMB IRQ line being asserted. This IMB global command causes each channel to assert a logical 1 on its assigned IMB data line if it is asserting IRQ, and to assert logical 0 on that line otherwise. The interrupt processing microcode determines the highest priority requesting channel, then issues OBII to the channel. The channel returns the number of the highest priority device which had an interrupt pending and its channel number. The returned word will be used to vector through the DRT entry for the device to the device software driver.

Initialize Channel

Initialize Channel causes a particular channel's hardware to be reset to a known state. I/O Clear causes a similar resetting action to all channels simultaneously. The specific actions which results from these commands are dependent upon the channel hardware.

Start I/O Program (SIOP) and Halt I/O Program (HIOP)

The SIOP and HIOP commands I/O Program provide the link between software control of channel programs and the execution of those programs. When software causes a change in the running status of a device channel program, the channel will request service by asserting CSRQ. The CPU microcode will subsequently perform the

tasks required to inititate or terminate execution of the channel program.

During a SIOP or a HIOP, the IMB data lines contain the status change information which enables the channel to request service because of a change in running status. However, certain instances occur during the execution of channel programs which require the interpreting microcode to change the running status of a program without also causing a channel service request. If the proper bit is set, the Status Change condition is cleared and no service request results from the SIOP or HIOP command.

3-7. IMB Access. Bus access is achieved on a priority basis. There are three priority structures: slot, channel, and device. Each I/O PCA that can access the IMB must request bus access either using the slot or channel priority. Devices are serviced in the order of device priority. The CPU has the lowest priority, and is responsible for controlling IMB access. Different I/O PCA's may request control of the IMB for different reasons and one may retain control by continuing to request after having been granted access.

3-8. Slot Priority. Slot priority is used only for the General I/O Channels (GIC) during DMA transfer. The highest priority in this structure is assigned to the GIC that is physically closest to the CPU.

3-9. Channel Priority. Any combination of channels may be asserting IRQ, or CSRQ at one time. When the channels are polled, the lowest channel number has the highest request priority on each request line.

3-10. Device Priority. Within the highest priority requesting channel device priorities are:

IRQ: If several device interrupt bits are set the lowest numbered device will be serviced first.

CSRQ-parallel poll: If CSRQ is due to an affirmative poll response or a change in channel program status, then the device on the highest DIO line (lowest device number) has the highest priority.

CSRQ-serial poll: If a serial poll must be conducted to determine which device is serviced, then the device priority is determined by the poll table. The first device polled has highest priority, and polling stops at the first device requiring channel program service.

3-11. HP-IB

The HP-IB is the standard interface bus between a GIC and devices on a channel. The bus consists of eight data lines and eight control lines. One end connects to the side or rear junction panels and the other end employs multiple connectors to attach to devices.

3-12. Commands. The HP-IB protocol specifies the command structure which can be used for device control. Before a device can accept data over the HP-IB, it must receive an Address-To-Listen command containing its device number. Likewise, data cannot be acquired from a device that has not received an Address-ToTalk command. The HP-IB channel instructions invoke these commands for all write and read operations, with the device number derived from the polling sequence. Enabling a device to talk or listen is generally insufficient. A listener must be told whether the forthcoming information is data or control; a talker must be told to output either data or status information. While several methods of sending this modifying information are available, the channel instructions utilize the HP-IB message, My Secondary Address. The secondary address is sent to the device in a command cycle immediately following the primary message My-Talk-Address or My-Listen-Address. The data is then transmitted and is interpreted as either data or control information. The final action resulting from HP-IB channel instructions is the unaddressing of the device, so the HP-IB is left in a well defined state.

3-13. Device Service Requests. The Parallel Poll function allows up to eight devices to assert separate lines on the HP-IB for service request. In this case, the bus controller (GIC) periodically puts the HP-IB into a parallel poll mode, and each device then uses one of the eight data lines to indicate its need for service. Since one device is assigned to each line, the controller can immediately determine which devices are requesting service.

3-14. Additional Talker Function. The HP 3000/44 utilizes devices that can identify themselves so that the system drivers may be configured without user inputs. However, if the user has attached a device which cannot identify itself it would return random data when addressed in the normal manner. To resolve this problem, the identification process will assume that the devices recognize another talker address (31) in addition to the one normally used for data transfers.

3-15. HP-IB Protocol. An attachment which obeys the HP-IB protocol is called an HP-IB device and has the following properties:

a. It recognizes the Identify directive through implementation of an extra extended talker (TE) function.

b. It accepts command information through MY-Secondary-Address messages.

c. It utilizes a parallel poll line uniquely determined by the device address on the HP-IB; asserts a low voltage on this line to request service; and is the sole user of this line Since there are eight data lines HP-IB device addresses are numbered from 0 through 7.

3-16. RS-232-C Data Communication Line

This bus specifies 25 dedicated lines as the standard interface in data communication. Pin assignments are set aside for ground, data, control, and timing circuits. Transmission over this bus is bit-serial and is reserved for terminal operation.

3-17. PROCESSOR ELEMENTS

The processor elements determine the basic characteristics of the computer system hardware and consist of the ALU, CTL, and PCS PCA's. The CPU interfaces with other elements in the system through the IMB.

The ALU contains the arithmetic logic unit, data registers, IMB interface, clock circuitry, and shift logic. The CTL PCA contains four kilowords of microcode instruction decoding circuitry and program control entry. The PCS PCA provides ROM storage for the main microcode, decimal, 64-bit floating point, and COBOL. The three PCA's operate together to translate received instruction words into microprogram starting addresses, decode microprograms into fixed control signal sequences, and execute various arithmetic functions. The processor is microprogrammable and has a 64-bit wide control store, a 16-bit wide arithmetic path, and a 16-bit wide memory address path (7 bits are used for check bits).

3-18. I/O ELEMENTS

The I/O elements for the HP 3000/44 consist of two channels, the General I/O Channel (GIC) and the Asynchronous Data Communication Channel (ADCC). The GIC is the hardware I/O channel which provides the electrical interface between the computer system via the IMB and peripheral devices connected to the HP-IB. The ADCC provides a bit-serial data interface between the computer system

and peripheral devices. The two channels operate in a similar manner, however, the GIC has a DMA facility to permit high-speed transfer of large blocks of data and the ADCC can transfer data only one character at a time.

3-19. General I/O Channel

The GIC is a controller of the HP-IB and translates I/O commands from the CPU into the proper HP-IB protocol. Nearly all transactions with I/O devices are accomplished without software interrupts, since I/O is achieved with channel programs. Software is responsible for setting up a channel program, but the execution of this program is performed by the CPU channel microcode. The CPU channel microcode is devoted to I/O tasks and implements the necessary algorithms for decoding the channel instructions and effecting the required I/O operations. Once the channel program is running, device control and data flow are normally carried to completion with no software intervention and without altering the system environment. If special situations arise, software may alter the program or even halt execution.

Several devices may simultaneously need service, and the CPU must decide which one will receive attention. First, all channels are polled, and the highest priority GIC with a device request pending is chosen. The CPU then obtains from that channel the number of the highest priority device needing service. Once the device number is determined, execution of the channel program will begin. The CPU fetches each channel instruction and breaks them down into several IMB commands addressed to the proper GIC. The GIC interprets these commands and directs them onto the HP-IB device.

The GIC contains DMA (Direct Memory Access) hardware which allows large records of data to be transfered at the maximum speed of the HP-IB. The channel microcode enables the device and then initializes the DMA hardware on the GIC. On a read operation the DMA hardware will read the bytes, pack them into words and place them directly into memory, all without assistance from the CPU. The CPU is free to service other devices while DMA is in progress.

3-20. Asynchronous Data Communication Channel

The Asynchronous Data Communication Channel (ADCC) is the second channel type used in the system. This channel performs essentially the same functions as the GIC but not in the same manner. Data is transfered from memory to an ADCC device (terminal) in parallel form, then converted to a serial bit stream for trans-

mission over the RS-233-C lines. Information being read from a device is in serial form and is converted to eight-bit bytes for transfer to memory.

Two ADCC boards may be used, the Main ADCC and the Extender ADCC. Each board contains four ports for connection to devices through RS-232C data communication lines. The Main ADCC is used when four or less devices are connected to a channel. The Extender ADCC extends the device capability of channel to eight. All circuitry except data handling circuits are on the Main ADCC. For this reason, the Extender ADCC connects to the Main ADCC to control signal information.

When more than eight devices are to be attached to ADCC channels, additional Main ADCC's are required, since each ADCC can accommodate only one Extender.

Unlike the GIC, the ADCC does not have a DMA facility and therefore cannot be a master of the IMB or memory. As a result, the ADCC is always a slave and must be directly controlled by the CPU through the use of channel programs. Circuitry on the ADCC decodes address information relating to channel and devices and select the correct device for operation.

The ports on the ADCC (Main and Extender) may be either hardwired to devices or to modems. Currently, the only modems to be considered are the Bell Models 103 and 202.

3-21. MAIN MEMORY ELEMENTS

The memory is a high speed, high density memory system that is compatible with IMB protocol. Memory arrays are 256 kbyte or one Mbyte, using 16k or 64k RAM's, respectively. The maximum memory configuration is 4 Mbytes. The minimum memory configuration consists of one MCL and one SMA. One MCL controls up to eight controls up to eight SMA's; however, the system can operate with two MCL's. This means that each MCL will then provide for two Mbytes of memory using 16k RAM's.

3-22. MAINTENANCE/CONTROL ELEMENTS

The control and maintenance processor (CMP) is a single PCA that provides control functions to perform warmstarts, cold loads, and memory dumps and aids in system maintenance by including a system selftest and a maintenance display. These functions allow the system to have a consistent and friendly user interface. When the operating system or the CPU fails, the user can use commands from the system console to bring the system up if a software error occurred, or to help diagnose hardware problems. The CMP also has a HELP feature to assist untrained operators in bringing the

system up. In addition, the CMP provides the capability for remote maintenance which allows diagnosis of software and hardware problems from a remote location.

3-23. System Console

The system console is a terminal that is the main interface between the operator and the system. The console displays normal MPE console information and can also be used as a session device. In addition, it is the front panel for the system and contains controls for operation. Various types of diagnostics can be initiated from the system console. The system console can be any of the 264X, 262X or printing terminals.

3-24. System Control Panel

The system front panel allows the system operator to perform the control and monitoring functions of the system. Control functions on the system front panel enable direct access to major functions through the use of the system console, activate the maintenance mode, enable hardware-related functions such as RUN and HALT, and software-related functions such as warm start, memory dump, and cold load. Also, since the system console utilizes the same control functions for hardware, the system front panel can be used as a backup panel if the console is down.

3-25. PERIPHERAL ELEMENTS

The peripheral elements used with the HP 3000/44 are connected primarily to GIC's while the ADCC is reserved solely for terminals. Peripherals attached to GICs through the HP-IB include disc drives, line printers and magnetic tape drives. The GIC's are used for all peripherals, except terminals. For a listing of the supported peripherals used in the HP 3000/44, refer to the current Price/Configuration Guide.

SECTION IV

CENTRAL PROCESSOR UNIT

4-1. INTRODUCTION

This section describes the Central Processor Unit (CPU), which includes a functional description, system component description (registers, etc.), and the CPU implementation of hardware. (See the HP 3000 Series 44 Block Diagram, part no. 30090-90003, for for component and functional references.)

The Series 44 CPU is a microprogrammed pipeline processor that executes the current 3000 instruction set through the use of microinstructions. The processor consists of three PCA's, the CTL, ALU, and the PCS. The CTL PCA contains 4 kilowords of microcode, instruction decoding circuitry and program control entry. The CTL provides control for the ALU, sequences the Control Store Address Register (CSAR), and controls test functions. The microcode consists of the channel program processor (CPP) code and selftest.

The ALU contains the Arithmetic Logic Unit, data registers, IMB interface, clock circuitry, and shift logic. The PCS provides an additional 8k X 48 bits of ROM storage. The microcode in the ROM storage consists of the main microcode, decimal, 64-bit floating point, and COBOL.

The processor is a fully synchronous machine, operating with a major clock cycle of 105 nanoseconds.

4-2. FUNCTIONAL DESCRIPTION

4-3. Instruction Execution

The processor indirectly executes instructions. Each macroinstruction causes a microprogram, which resides in ROM on the CTL and PCS PCA's, to be executed. The 16-bit macroinstructions are obtained from memory over the IMB and loaded into the Next Instruction Register (NIR). When the CPU completes current microprograms and is ready to execute the next instruction, the instruction is loaded from the NIR into the Current Instruction Register (CIR) and the Look-Up Table (LUT), which maps the instruction into a microprogram starting address to implement that instruction.

Once the starting address is dertermined, the control store presents a 48-bit microinstruction which is latched in the Microinstruction Register (MIR). This is where the various instruction fetch and execute fields are inputted and decoded. This decoded information is then passed to the ALU PCA which properly fetches registers and then executes the given function.

After executing the function, the results are stored into registers specified by the CTL PCA. The CTL circuitry then executes the next microinstruction or performs the necessary microprogram jumps, which store the address in either the Subroutine Return Register (SRR) or Slow Jump Register (SJR). When the microprogram is finished, the last microinstruction will have the NEXT instruction in the Special field. This informs the CTL PCA that it is ready to load the next macroinstruction from the NIR into the CIR and repeat the process.

The primary operation of the NEXT branch field option is to provide transfers to location 0 in ROM. This line gates the current macroinstruction in the NIR into the CIR (and LUT), fetches a macroinstruction memory fetch over the IMB using the P register and loads the next instruction into the NIR. Also,This line increments the P register and tests for any pending interrupts, and initializes the CTR and SP0 registers and flags F1, F, F3, and F4. These operations are performed simultaneously.

4-3. Microinstructions

The Series 44 microinstruction are 48 bits in length and are divided into 8 fields. These fields are listed as follows:

```
0....6...10.....16.....22.....28..31....36..........47
A    B   FUNC    STOR    SPEC    BR  COND  TARGET
```

In addition, there is the LITERAL field which is composed of the B and TARGET fields.

The A, B, FUNC, and STOR fields control the data paths. The A and B fields provide the data source registers for the ALU, and the FUNC field specifies the type of arithmetic operation and also controls the shifting of the ALU output. The STOR field specifies possible store locations.

The BR, COND, and TARGET fields control the sequencing of the microinstruction. These fields determine what type of branch is specified, the condition on which it will be taken, and the target address it will jump to on the true condition. The SPEC field handles miscellaneous functions including IMB operations and flag manipulations.

The execution of most microinstructions requires four clock cycles, which are referred to as ranks 0 through 3. Because of the pipelining effect, there is always a microinstruction in each of the four ranks. The major clock cycle is 105 nanoseconds. Although a new microinstruction is loaded every 105 nanoseconds, it actually takes 420 nanoseconds to completele execute a single microinstruction. However, the four ranks of the pipeline each contain an instruction. Therefore, after the initial first four are loaded, a microinstruction is executed every 105 nanseconds.

Parts of the microinstruction execution is completed in each of the four ranks. Rank 0 is the microinstruction fetch cycle, during which the CTL PCA supplies a micro-address and receives the corresponding microinstruction from either its own ROM or from ROM on the PCS PCA. At the transition time from rank 0 to rank 1, this data is latched into the MIR.

Most decoding of a microinstruction and some of its execution occurs in rank 1. All fields, except for some SPEC field options which require additional decoding during rank 2, are decoded and set up. The A and B operands are detched during rank 1 for use in rank 2. During rank 2, ALU functions are completed and IMB operations are initiated. At the end of rank 2 and during the beginning of rank 3, the data is stored in the proper registers. Only those microinstructions storing into the register files require action in rank 3.

4-4. DATA PATHS

4-5. General

Figures 4-1 and 4-2 illustrate the data paths of the processor. There are 64 registers that supply the A field, and 16 registers that feed the B register. The outputs of the A and B registers drive the ALU inputs. The F-bus, which is the output of the ALU, drives the shifter. The output of the shifter is the U-bus, which is fed back to to allow storage into the processor registers.

The B-register file duplicates the first 15 registers in the A-register file. Thus, a store into any of these registers will write into both simultaneously. These registers can then be called up individually for the A-field and B-field inputs to the ALU. The value on the U-bus and literal values can also be addressed as a source on the B-field. On the A-field, there are 10 special hardware-implemented registers that replace the A-register file registers and eight bank registers that store into both the A-register file and a special bank register file (but is fetched from the A-register file).

Ten special registers are available on the A-bus, as follows:

CIR	Current Instruction Register
USWP	The U-bus with the left and right bytes exchanged
SIR	Status and Interrupt Register
SWCH	Switch Register
CTR	Eight-bit counter
SR	Number of valid TOS registers
SP0	Shift register used for double shifts, multiply, etc.
STA	Status Register
OPND	Memory Data Register
REGN	Used for indirect register access.

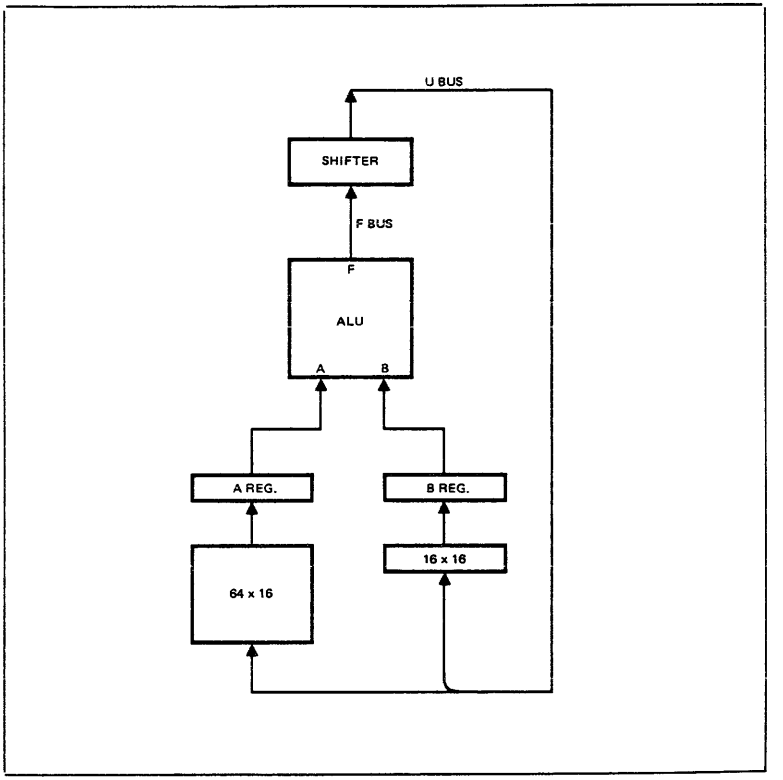


Figure 4-1. Basic Data Paths

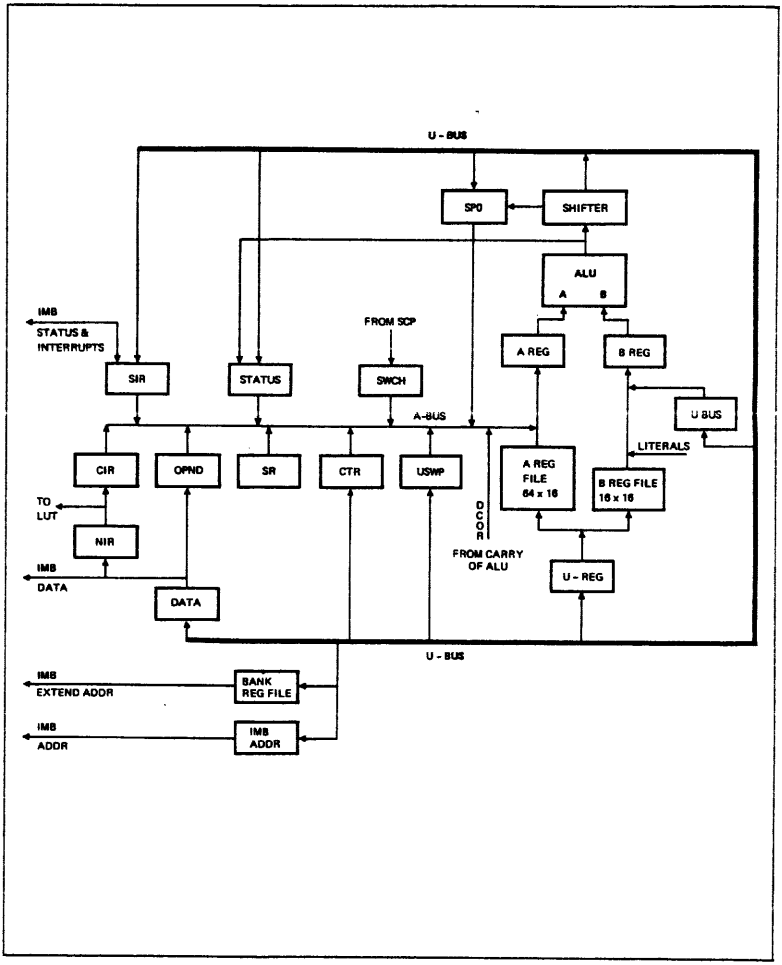


Figure 4-2. Main Data Paths

These registers map on top of the register file locations, and become inaccessable. Another special register (R14Z) is in the register file and is permanently assigned the value of zero. This register is used for NOP's. The first eight (0:7) of the status register are kept in specially controlled registers.

The first four registers in the register file are the Top-of-Stack (TOS) registers. The TOS registers function with two other registers, the Namer register and the four-bit SR register, which is available on the A-bus. The Namer cannot be written into or read. These registers are controlled from the SPEC field so that the four TOS registers behave as a circular stack, with the SR register indicating the number of valid elements on the stack and the Namer register pointing to the current top element. The register specified in a microinstruction field (A, B, or STOR) is a TOS register if the high order four bits of the A- or storefield, or upper two bits of the B-filed are zero. The physical register is determined by subtracting the lower two bits from the Namer register. Thus, incrementing the Namer and SR register causes a "push", and a "pop" occurs when both are decremented.

REGN may be placed in the A or STOR fields to indirectly specify a register. In effect, the low order six bits of the counter (CTR) replace the six bits of the field specifying REGN. This substitution is transparent in the sense that all registers function the same way whether accessed directly or through the REGN feature. Because there is only one level of indirectly specifying, when the REGN points to itself it makes R63, an otherwise inaccessible file register, available. The REGN is useful in TOS register manipulations, such as filling or emptying them.

The contents of the A and B registers and the operation codes from the CTL PCA are the inputs to the ALU. The ALU performs arithmetic (including A - B and B - A) and boolean functions. The outputs of the ALU are the F-bus, which drvices the shifter, and the carry, overflow, and zero status signals.

The shifter is a combinational shift network which connects the F-bus to the U-bus. It provides single precision rotates and logical and arithmetic shifts. When coupled with scratch pad 0 (SP0), it can perform a limited number of double-length shifts. The shifting is controlled from the FUNC field. The shifter can also mask left and right bytes, a feature which is enabled by the SPEC field.

Since the FUNC field is decoded by PROM. Flag 1 and Flag 2 are two of the address bits on the PROM's which control the ALU. This makes it possible to have ALU operations dependent upon the state of the two flags. This dependency can be utilized in conjunction with the automatic flag initialization which occurs as part of the macroinstruction sequencing.

Storing results occurs during the first half of rank 3 if the destination is a file register, or at the second half of rank 2 for the special registers [SIR, CTR, SP0, and STA(0:7), the destination of STA(8:15) is a file register]. Certain bits of the STA can also be stored under control of the SPEC field.

4-6. Operand Sources

As previously stated, there are two types of operand sources, the register files and the special registers. There are three register files, the A-file, the B-file, and the BANK-file. The A-file register has 64 locations for storing data, the B-file has 16 locations, and the BANK-file has eight locations. The B-file and BANK-file registers are copies of equivalent registers in the A-file. Several of the file registers are used for defining the limits and operating elements of the code and data segments.

The Code Segment Pointers are:

PB	Program Base
P	Program Counter
PL	Program Limit
PBNK	Bank Register that contains the upper 16 bits of the PB address

The Data Segment (Stack) Pointers are:

DL	Data Limit
DB	Data Base
Q	Current Stack Marker
SM	Memory Top of Stack
SR	Defines numbr of valid TOS registers
Z	Stack Limit
DBNK	Bank Register that contains the upper 16 bits of DB address
SBNK	Bank Register that contains the upper 16 bits of the DL address

The four top-of-stack (TOS) registers RA, RB, RC, and RD have special addressing properties. The value of the NAMER defines which register is to be top of stack. RA is defined to be top of stack, followed by RB , then RC, and RD. For example, if a POP microoperation is executed, the NAMER and SR registers are decremented and cause RB to become RA. This is prevent having to move data from register to register. Therefore, the four TOS locations are simply renamed so that RB becomes RA, the TOS, and so on. The TOS circuitry is a mapping algorithm that accepts a microcode request for a stack element, adds the value of the NAMER register, and points to a physical register. The TOS registers can be accessed through two different paths, the REGN which uses the CTR, and MIR which specifies the TOS directly.

Other file registers include the Index Register (X), the Scratch Bank Registers (ABNK and BBNK), and 35 unassigned scratchpad registers (R4 through R39).

The special source registers include 10 hardware registers that are available on the A-bus and one hardware register on the B-bus. The registers that are available on the A-bus map on top of the register file locations, making the corresponding file registers inaccessible. These registers are:

CIR	Current Instruction Register
USWP	UBUS with the left and right bytes swapped
SIR	Status and Interrupt Register
SWCH	Switch Register
CTR	Eight-bit Counter
SR	Number of valid TOS registers
SP0	Scratchpad 0; shift register used for 32-bit shifting
STA	Status Register
OPND	Memory Operand Register
REGN	Used for indirect addressing

Scratchpad 0 (SP0) is used for functions in addition to 32-bit shifting. These include multiply and divide functions, and system halts and CPU selftest hardware failures. Prior to each selftest section, the low-order and high-order bytes of SP0 are loaded with a failure code. If the test section fails, the Command and Maintenance Processor (CMP) can then read the lower byte of SP0 for the failure code. This failure code is displayed on the ALU LED's, which is the high-order byte of SP0.

The only special source register available on the B-bus is the FAST UBUS register. Because of the Processor's pipelining, the results of one line are not available to the next line of microcode unless called for as a FAST UBUS or USWP.

4-7. MICROINSTRUCTION SEQUENCING OPTIONS

The sequencing, or branch, options are determined by the BR field. The COND field selects the condition to be examined, and the TARGET field provides any required microaddress. Because of the pipelining, each microinstruction specifies a primary path to keep the pipeline full. Most BR functions provide a secondary path that is always defined by the TARGET field. The possible branches, controlled by the BR field, and the corresponding primary and secondary paths are given as follows:

BR Function	Primary Path	Secondary Path
JMP (Jump)	F	TARGET
JMPU (Jump in User Mode)	F	TARGET
JSB (Jump to Subroutine)	F	TARGET
RSB (Return)	R	TARGET
SKIP (Following Line)	F	F
NEXT (next macroinstruction)	OVH	TARGET
REP (Repeat)	C/F	TARGET
jump/jsb unconditional	TARGET	-

where: F: the following line
R: the contents of the subroutine return register
OVH: the overhead line (location 0000)
C/F: the current line unless the counter (CTR) is zero, then it is the following line

The last BR function, jump/jsb unconditional, is used for unconditional jumps and jump subroutines, where a new target is set at the beginning of rank 1. The target of this microinstruction is fetched without any lines of overhead.

4-8. Jumps (Conditional 000)

Conditional jumps require one line of overhead to determine if the target is to be fetched. If the condition is true, the single line that entered the pipeline must be cancelled. This is done by preventing all rank 2 and rank 3 stores from occurring. There are two types of conditional jumps, data dependent and nondata dependent. Data dependent jumps test the output of the ALU from the previous microinstruction if that instruction was executed. Nondata dependent jumps test the current flag status.

4-9. Skips

Skips disable the STORE, SPECIAL, and BRANCH field options on the following line if the condition is true. All skips require one line of overhead.

4-10. Repeats

The repeat function is similar to a three-way branch. As long as the counter (CTR) is nonzero and the condition is met, the microinstruction register is held fixed and contains the line with the REP. If the repeat has been made conditional by specifying a path other than UNC, the secondary path will normally be taken if the condition is true. Otherwise, if the counter reaches zero, the next line in sequence will be taken.

4-11. Next

The NEXT option is used to start the next macroinstruction. This option has no overhead line to force the CSAR to 000 on the next cycle. If a condition is included, the NEXT will be taken if the condition is not true. If the condition is true, the target will be taken. Conditional NEXT options can only be specified in the lower bank of microcode because the high order bank bits are cleared when the NEXT enters the pipeline, (i.e., it has one line of overhead when conditional, which is 0000).

4-12. MACROINSTRUCTION SEQUENCING

Macroinstruction sequencing is initiated by executing a NEXT branch field option. The primary operation is to transfer to the entry point of the macroinstruction in the Next Instruction Register (NIR) and fetch the following macroinstruction into the NIR. This process also includes initializing the CTR, SP0 registers and flags F1, F2, F3, and F4, updating the CIR and P registers, testing for interrupts, and providing for paired stack operations.

4-13. Operation

While the NEXT is rank 1, the overhead line is fetched from control store address 0. If the NEXT line was inhibited by a branch or SKIP on the preceding line, the branch target would be fetched instead of the overhead line. Execution of this line allows the normal control and data paths of the processor to be used to increment P, fetch of the macroinstruction following the current one to be started from memory, and transfer pending interrupts to the interrupt handler.

If a memory fetch into the NIR is not completed during the second quarter of a NEXT in rankl (and the NEXT is not inhibited), the processor freezes. If a fetch is being started in rank 2 and an uninhibited NEXT is in rank 1, the processor waits for the fetch to complete. If a fetch into the NIR and a NEXT are on the same line, the NEXT proceeds without the fetch.

While the overhead line (location 0000) is in rank 1, the first line of the new macroinstruction is fetched from the control store. Its address is obtained from the Lookup Table (LUT) on the CTL PCA. Each entry in the LUT contains a 12 bit starting address and 4 bits that initialize flags F1, F2, F3, and F4. The LUT allows most of the macroinstructions to be fully decoded. Some macroinstructions have duplicate entries and others require further decoding by microcode. When the overhead line is read from the control store, the upper 4 bits of the control address are set to zero. Since the LUT supplies only the lower 12 bits, all macro-

instruction entry points must be in the first 4k of control store.

A conditional branch can be specified by the NEXT line. If this branch is taken, execution of the overhead line is inhibited and the branch target is fetched instead of the first line of the new macroinstruction. If a branch specified with a NEXT is taken, it branches into the first 4k of the control store regardless of the location of the NEXT line, since the upper 4 bits are set to zero when the overhead line is fetched.

4-14. Single Macroinstructions

The CMP initiates execution of a single instruction and then signals a RUN/HALT interrupt. The CPU fetches the single instruction into the NIR, adjusts P if necessary, sets RUN and DISABLE, and then clears DISABLE on the same line as a NEXT. This inhibits the JMP TEST on the overhead line since the decision to branch is determined as the overhead enters rank 2, but allows TEST to be true thereafter. Therefore, the RUN/HALT from the CMP will cause the CPU to halt when a single instruction executes a NEXT. The macroinstruction XEQ must use DISABLE in this manner in order to allow single cycling of a macroinstruction.

4-15. IMB INTERFACE

The processor uses a four-wire, processor-master IMB interface. The four-wire handshake and the bus-granting logic are the similar to the HP 3000/30 and HP 3000/33. The CPU has an internal synchronous IMB state machine which receives the bus granting signals, synchronizes them, and uses the signals to advance to the next state.

The IMB state machine has four basic states, Hold, Request, Address Done Wait, and Data Done Wait. In the Hold state, the IMB state machine does not initiate a read or write operation. If the CPU issues an IMB request, the state machine will move to the request state where it can request the IMB. In the Address Done Wait (ADNW) state, the CPU asserts ADO and DDO, and remains in this state until ADN is returned. The IMB state machine moves to the Data Done Wait (DDNW) state and remains in this state until DDN is returned, then returens to the Hold state. If there is a CPU request pending, the IMB state machine will move immediately to the request state.

4-16. CPU Memory Read Operation

When the CPU initiates a memory read operation, the CPU microcode issues a CPUREQ signal to the IMB state machine, when it is the

Hold state. If the state machine is not currently processing a bus request, it accepts the CPUREQ signal and enters the Request state . In the Request state, the IMB state machine waits until the IMB is clear and the CPU can have control of the bus. As soon as the IMB is clear, the CPU gains control of the IMB. At this time , the state machine advances to the ADNW state and the SPBUS (synchronized processor bus) logic asserts DDN, and the AOUT logic asserts the ADO and AOUT signals. The AOUT signal enables the opcode and address onto the IMB.

The state machine remains in the ADNW state until ADN is returned from memory, then it advances to the DDNW state. The ADN signal resets the AOUT logic, which in turn deasserts the ADO signal.

When DDN is asserted by memory, the state machine resets the SPBUS logic which deasserts the DDO signal. The SPBUS logic generates the DDNW signal and the AOUT logic generates the ADNW signal. These signals reset the timeout logic so that an IMB timeout does not occur.

The state machine then sets the HOLD flip-flop (in the SPBUS logic) which indicates that the CPU has the OPERAND in the OPND register. At this time, the state machine returns to the Hold state and waits for a new request.

4-17. Other Operations

A CPU memory write operation is identical to a read operation except that data is written onto the bus when enabled by the WRITE and SPBUS signals. Also, I/O reads and writes function in the same manner as that for memory reads and writes, except that the IMB opcodes are different and the bank registers are not used.

IMB operations are controlled through the SPEC field, which selects the function and the bank register. The lower address bits and the data for a write operation are obtained from the UBUS. Once initiated, IMB operations (whether from memory or I/O) proceed automatically. The CPU freezes only if the data is requested before the operation is completed.

A special capability is provided to implement the Global IMB commands. The Global option in the STOR field generates ADN and DDN on the IMB for approximately one millisecond, completing the Global handshake.

4-18. Processor Freeezes

There are three types of IMB-related processor freezes, the IMB is not available, the NIR is not ready, and the OPND is not

ready. For the IMB not available, there are two conditions that will causes a freeze:

a. An ADDR FREEZE will occur if an IMB operation is initiated before the address register has been released.

b. A DATA FREEZE occurs if a write is in progress and another IMB operation is about to be started before the slave has signaled DDN.

A NEXT FREEZE will occur if a microinstruction saying NEXT is in rank 1 (NIR not set) and a read into NIR is in progress.

The OPND FREEZE will occur if the memory has not returned the data requested by a read.

4-19. Error Conditions

The CPU can detect two IMB error conditions. The first is a device timeout that occurs when the addressed device does not respond within one millisecond. The second error condition is a memory parity error which is detected by the memory controller. These errors and a reset of PON are the conditions that can cause microinterrupt.

4-20. COMPONENT DESCRIPTION

Refer to the system block diagram for the discussions of the components.

4-21. Next Instruction Register (NIR)

The NIR is located on the ALU PCA. It is a 16-bit register that contains the next software instruction to be processed and is loaded from memory. This regiater is located on the ALU PCA.

4-22. Current Instruction Register (CIR)

The CIR is a 16-bit register that contains the current software instruction being processed. The contents of this register is loaded from the NIR. This register is located on the ALU PCA.

4-23. Look Up Table (LUT)

The LUT is addressed by the NIR, and outputs a 12-bit address which is applied to MUX 1. MUX 1 generates a 16-bit output which addresses the initial microcode instruction that implements the

the microprogram for the instruction currently in the CIR. This component is located on the CTL PCA.

4-24. Multiplexers 1, 2, and 3 (MUX 1, MUX 2, MUX 3)

MUX 1 multiplexes one of four inputs when enabled by the Branch Control. These inputs are the LUT address, the contents of UBUS during rank 3 (R3UBUS), and the outputs from MUX 2 and MUX3. The output of MUX 1 is a 16-bit ROM address.

MUX 2 multiplexes one of two inputs when enabled by the Branch Control. These are the Fast Jump (or Target) address and the Slow Jump Address. MUX 3 multiplexes one two inputs when enabled by the Branch Control, the contents of the control store address register (CSAR) and the contents of subroutine return register (SRR). These multiplexers are located on the CTL PCA.

4-25. Incrementer (INC)

The output of MUX 1 is placed on the Control Store Address Bus. This address is applied to the INC which increments the address by one and latches the new address in the CSAR. The INC is on the CTL PCA.

4-26. Branch Control Logic

The Branch Control Logic enables the selected MUX, depending upon how the microcode decodes the Branch, Condition, and Target fields. If the microcode is executing a NEXT instruction, the Branch Control Logic must know what the SPEC field conditions are. The Branch Control Logic is on the CTL PCA.

4-27. Condition Branch Logic

Because the Target field is only 12 bits wide, the normal branches are confined to the PCS PCA. To allow access to the CTL PCA, an option is provided in the SPEC field. Arithmetic conditions are tested together with an input from the Shifter and with ordinary conditions. This logic is on the CTL PCA.

4-28. ROM

Microcode is stored in ROM on the CTL and PCS PCA's. The 48-bit microinstruction words are divided into eight fields, each field containing from three to 12 bits. Each decoded field produces a set of microcode signals that control the operation of the CPU. The output of ROM is loaded into the MIR on each 105 nanosecond clock cycle.

4-29. Microinstruction Register (MIR)

The MIR contains the current executing microinstruction after latching the output of ROM. This register is on the CTL PCA.

4-30. CPU Data Registers

Most of the data registers are located on the ALU PCA. These registers are the A-Bus and B-Bus registers. The A-Bus registers are special hardware registers that can be selectively loaded onto the A-Bus through the use of the Special Register Select logic. The A-file registers are selected for access to the A-Bus by the A-Address logic.

The B-Bus registers are special hardware registers (FASTUBUS) that are selectively loaded onto the B-Bus through the use of the Special Register Select logic. B-file registers are selected for access to the B-Bus by the B-Address logic. Literals are also addressed on the B-bus.

4-31. A-File and B-File Register Store Logic

This logic is used during rank 3 to store the contents of the UBUS into a specified A-File or B-File location. The control logic is contained mostly on the CTL PCA.

4-32. Address, Data, and Bank Registers, and Opcode Latch

During and IMB operation, the opcode latch, address register, and bank register determine the type of operation to be performed, and the address including bank bits. If an IMB write is to be done, then the data register provides the appropriate data.

4-33. HARDWARE IMPLEMENTATION

The CPU consists of three PCA's, the CTL, ALU, and PCS. Each PCA's specific functions of the CPU are discussed and illustrated in the following paragraphs.

4-34. CTL PCA

The CTL contains sockets for four kwords of microcode, without parity, that can be loaded in one kword increments. (See figure 4-3.) The two-position jumper W1 selects the microcode options the HP 300 and HP 3000 microcode. The firmware on the CTL can be disabled by switch S1, located on the front of the PCA. However, the controlling function remains active. Switch S1 is normally positioned inward toward the stiffener. This PCA is placed in card cage slot location 11.

4-35. ALU PCA

The ALU contains Self Test switch S1 on the front of the PCA. (See figure 4-4.) This switch initiates the CPU micro diagnostic. Self test errors are displayed on the LED's, also on the front of the PCA. The error code is shown on the upper seven LED's with the eigth LED providing odd parity over all eight LED's. When the seven LED's are not lit, no errors are found. However the eighth LED will light for odd parity.

The ALU also contains the system clocks. A 38 MHz clock provides a major clock cycle of 105 nanoseconds. The minor clock cycle is approximately of 26 nanseconds. The second clock is a 256 kHz clock that provides date, time of day, etc. The ALU is placed in the card cage slot location 12.

4-36. PCS PCA

The PCS contains sockets for eight kwords of microcode, without parity, that can be loaded in one kword increments. (See figure 4-5.) The address space of the PCS can be configured to begin at 0, 4k, 8k, ... 60k for up to eight kwords by 16-position switch S1, located on the front of the PCA. In the normal position, the switch is set to 0 (zero). Jumpers W1, W2, and W3 are used for proper addressing space. This PCA is placed in card cage slot location 13.

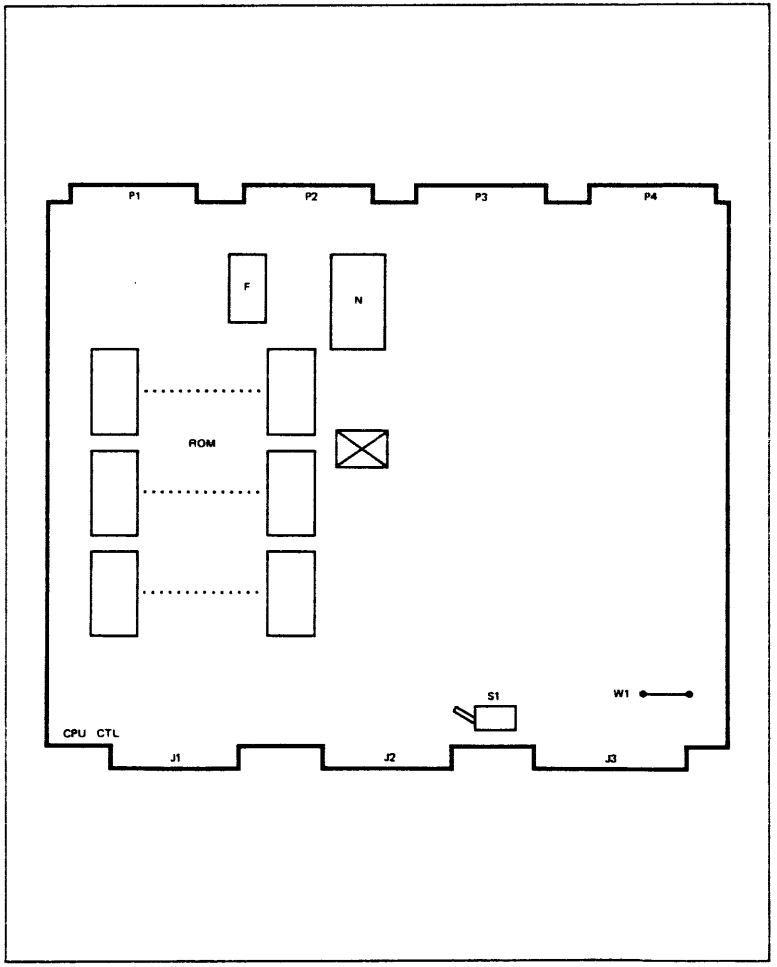


Figure 4-3. CTL PCA

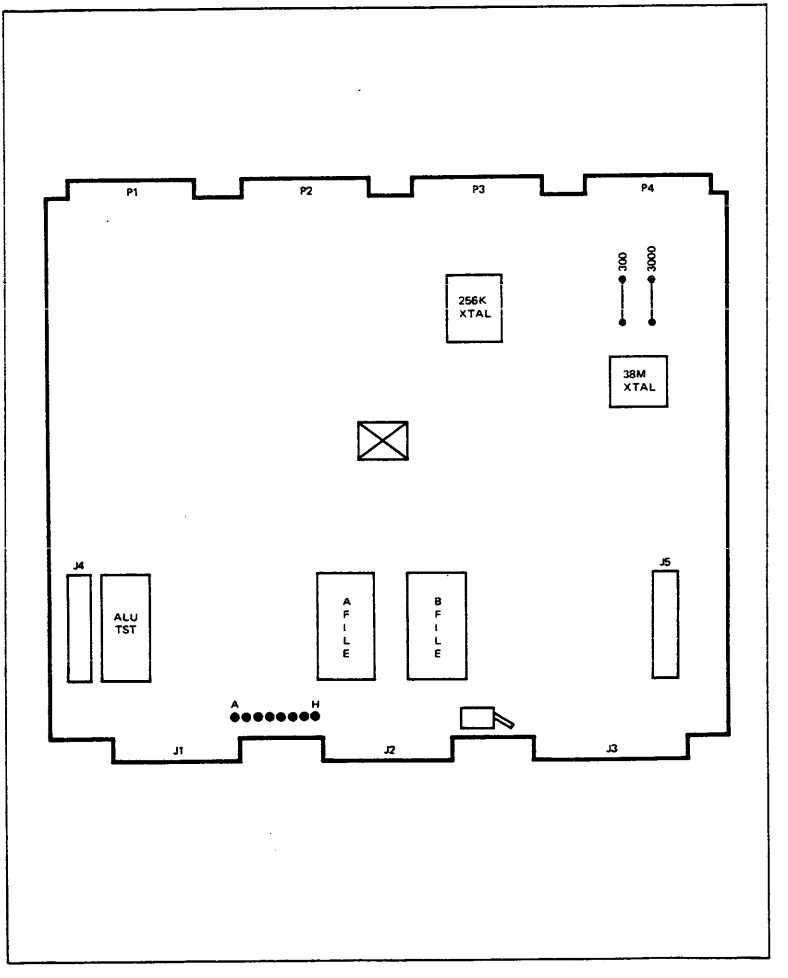


Figure 4-4. ALU PCA

CPU

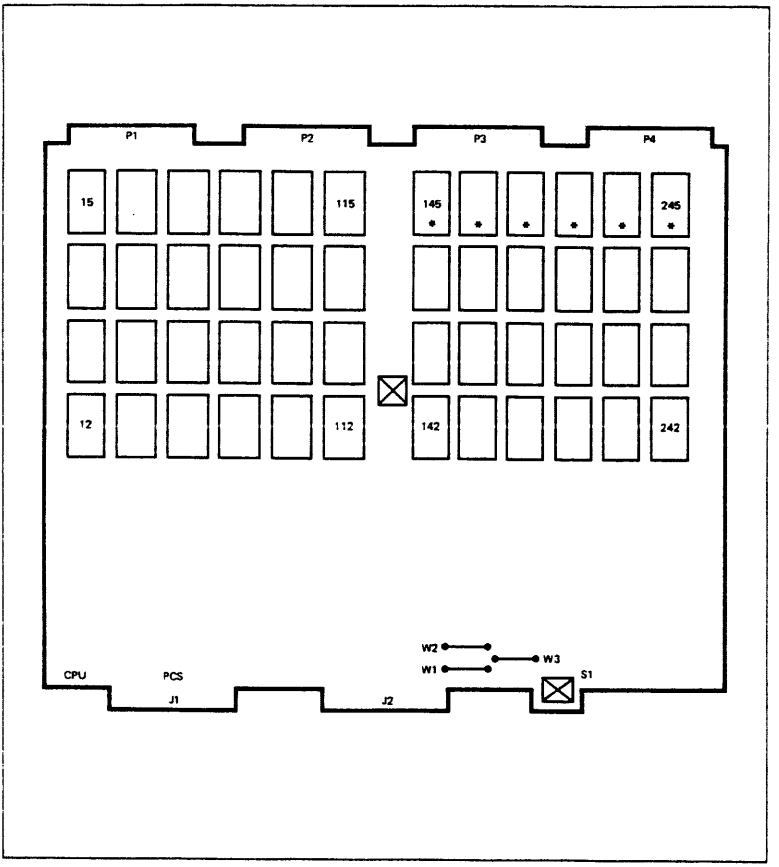


Figure 4-5. PCS PCA

SECTION V

CONTROL AND MAINTENANCE PROCESSOR

FUNCTIONAL DESCRIPTION

5-1. INTRODUCTION

This section contains the description of the HP 3000/44 Control and Maintenance Processor (CMP). The description includes the hardware and firmware of the CMP.

5-2. GENERAL

The CMP provides control functions to perform warmstart, cold-load, and memory dump functions as well as aiding in system maintenance by including a system selftest, an IOMAP display, and a maintenance display.

Even when the operating system or CPU fails, it is still possible to use commands from the system console to bring the system back up if a software error occurred, or to help diagnose system hardware problems. The CMP provides the capability for a remote console to allow remote diagnosis of hardware and software problems.

The CMP increases the availability of the system by decreasing the time to diagnose hardare and software failures.

The CMP is a standard size board that contains approximately 11K 16-bit words of code.

5-3. CMP HARDWARE FUNCTIONAL DESCRIPTION

The following paragraphs contain descriptions of the CMP interfaces, LED indicators, cabling, and power supply requirements.

5-4. RS-232 Interfaces

The CMP is connected to ADCC ports 0 and 1, the system console, and the remote console (via modem) through RS-232 interfaces. During normal operation (remote disabled) ADCC port 0 is connected to the system console and ADCC port 1 is connected to the modem. This allows the modem to be used for dial-in sessions to MPE. (See figure 5-1.)

When REMOTE is enabled, the modem is connected in parallel with the system console to allow remote console capability. When the CMP is communicating with the console(s), ADCC port 0 is temporarily disconnected from the console(s). With REMOTE enabled, the two consoles appear as one to the ADCC and MPE. The Data Terminal Ready (DTR) signal from the system console is displayed on an LED on the CMP front plane edge to indicate when the console is properly connected.

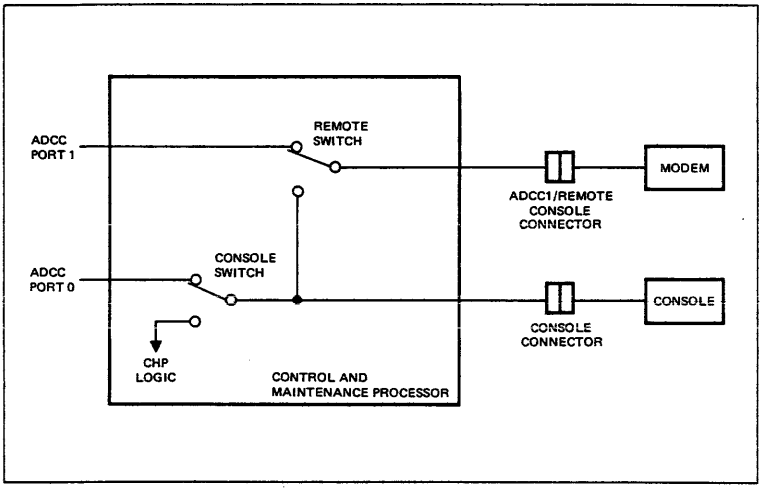


Figure 5-1. CMP Interconnect Diagram

A special ADCC/CMP cable is used to connect the ADCC and CMP at one end of the cable to a standard ADCC junction panel connector at the other end. The ADCC junction panel connectors are for:

- Port 0 - System Console.
- Port 1 - Remote Console
- Port 2 - Terminal
- Port 3 - Terminal

The system console junction panel connector is not modem compatible and must be direct connected to the console.

A terminal can be connected to port 1 of ADCC channel 1 using a standard extension cable or a four conductor cable containing Ground, Transmit Data, Receive Data, and Data Terminal Ready.

To connect a terminal to port 1 of ADCC channel 1 use only the standard extension cable (30062-60006) or a direct connection using a 13232M (13232N in U.S.) cable to 264X terminals or a 13222M modem cable to 262X terminals.

Connection to a modem should be made using an 25-foot modem cable (30062-60020). Only a full duplex modem may be connected to port 1 of ADCC channel 1.

Placing the REMOTE CONSOLE switch to OFF connects port 1 of ADCC channel 1 to the remote console connector which allows normal logon sessions by a remote terminal. When the switch is in the ON position the remote terminal is connected in parallel with the system console at port 0 of ADCC channel 1. This allows the remote terminal to act as a duplicate system console for maintenance purposes.

The modem connected to the ADCC channel 1 remote console connector should have call-originating and automatic-answering capabilities.

The ADCC channel 1 port 2 and port 3 connectors are connected through the ADCC/CMP cable to the ADCC.

All data and modem control lines use Motorola MC1488L or MC1489AL for the RS-232C (CCITT V.24) interface. The signals at the ADCC channel 1 ports 2 and 3 connectors are generated by the ADCC and are unchanged by the CMP.

To prevent the remote console modem from hanging up when the system is powered down, the user at the local site must lift the receiver on the modem and press the TALK button. The modem at the remote site must be configured such that it does not automatically hang up upon loss of carrier. While the system is powered down, the modem line can be used for voice communication.

When REMOTE is enabled, data from the consoles are mixed at the CMP logic. When the ADCC sends an ENQ character to the consoles they will simultaneously respond with an ACK character. Any difference in timing between the two responses could cause the mixed bit patterns of the ACK characters to be erroneously received at the ADCC.

This problem is overcome by detecting the ENQ character from the ADCC and enabling logic which will cause the first ACK character to arrive from a console to be ignored. The second ACK character will be sent to the ADCC. As a result the ADCC will wait for the slowest console to respond. The local and remote consoles, as well well as the CMP and MPE, must be set at the same baud rate.

The modem for the remote console must be full duplex. Half duplex modems are not supported. It is desirable to have the modem at the customer site be auto-answer so that it can be used for dial in sessions to MPE and, when desired, auto-answer for maint-

enance or remote operator calls. The modem at the service center should have originate capability. Acoustic couplers can also be used at the service center but they are unreliable on noisy phone lines.

When the modem on ADCC channel 1 remote console connector is being used for a normal dial-up session on the system the modem control signals will be controlled by the ADCC. In this mode the modem control sequence will be identical to the ADCC except SCA (Secondary Request to Send) is not connected and CH (Data Rate Selector) is controlled by a switch on the CMP.

When the modem is being used for the remote console the CMP starts a connection sequence by turning on CD (Data Terminal Ready) and CA (Request To Send). SCA is not connected and CH is controlled by the Data Rate switch on the CMP.

After the line has been established, CF (Carrier Detect) and CB (Clear To Send) are monitored to be sure a signal is being received from the remote modem. If CF or CB make more then 50 on-to-off transitions or if either goes off and remains off for 10 seconds a disconnect will occur. This feature will assure that an improper call to the computer or a line breakage will always result in a disconnect.

If CC (Data Set Ready) goes off the CMP will turn off CA and CD after a short time delay to terminate the connection. After 10 seconds with CD and CA off, the CMP will re-assert these signals to allow a new phone connection to be made.

For baud rate detection, upon power-on the CMP speed senses the console by sending ENQ characters at different baud rates until the CMP receives an ACK character. If the CMP never receives an ACK, the CMP assumes the baud rate of the console is 2400 baud. This allows non-HP terminals to be used as the system console if the regular system console fails, but baud rate detection is less reliable with non-HP consoles.

The user must use the CMP ->:SPEED command to change baud rates while running MPE. The CMP also accepts the SPEED command and will change baud rates at the same time as MPE. If MPE is not operating, the CMP will accept the ->SPEED command.

5-5. CPU Interface

The CMP interfaces to the ROM data lines of the CPU to allow reading the current instruction and forcing an instruction to be executed by the CPU. The CMP also has read capability on the 16 ROM address lines. This allows reading the address of the current instruction and (using CMPFDR-) reading the data on the CPU UBUS. The following special purpose lines are used by the CMP and the CPU.

GO — This output of the CMP is used to microhalt the CPU.

STOP — This output of the CPU is a request to halt the CPU.

TIMDIS- — This output of the CMP disables the CPU timer.

DISTO- — This output of the CMP disables CPU IMB timeouts.

CMPEN- — This output of the CMP disconnects the CPU PROMS from driving the ROM data lines. It allows the CMP to supply a microinstruction.

CMPFDR- — This output of the CMP places the CPU UBUS onto the ROM address lines.

MQ — This output from the CPU is used to generate a clock for latching ROM address and ROM data.

5-6. IMB Interface

The CMP has an IMB breakpoint function which can microhalt the CPU upon the occurance of a breakpoint. The IMB interface also allows the CMP to read the lower 21 bits of the address plus the opcode for the last IMB operation. The address is latched in on the IMB handshake signal ADO.

The CMP also can drive and read the Power Fail Warning (PWF) line on the backplane. This allows the CMP to shut down power in the system. The CMP also monitors PON and Parity Error (PER) on the IMB.

5-7. System Control Panel Interface

The CMP interfaces to the control panel using the following four special purpose lines.

FPCON- — This output of the CMP is used to supply command data to the control panel.

FPSHIFT- — This output of the CMP is used to shift commands into

the control panel and to shift status out of the control panel.

FPLOAD- This output of the CMP is used to cause commands from the CMP to be executed by the control panel and to load status into the control panel status shift register.

FPSTATUS- This output of the control panel supplies status to the CMP.

CPUA- This output of the CMP is the handshake signal ADO which is buffered on the CMP. This indicates IMB activity.

5-8. CMP LED Indicators

The CMP contains its own LED status indicators which are mounted at the front plane of the CMP. These LEDs are labeled on the board stiffener and are adjacent to switch SW1. Normal indicais all LEDs on. The indicators are described below.

A - External Register 3, bit 11. This LED is used by Selftest and is normally on.

B - External Register 3, bit 12. This LED is used by Selftest and is normally on.

D - Console Ready - DSR, DTR from the system console. This LED is the Data Terminal Ready (DTR) signal from the console. The presence of this signal indicates that the cable to the local console is connected and the console is powered on.

T - CMP Active - 10 ms timer interrupt not pending. This LED indicates that the CMP processor is executing normally.

5-9. CMP Cabling

All signals between the ADCC/CMP and the terminal junction panel are via the ADCC/CMP cable. This cable has a 56 pin and a 50 pin connector at one end. These connect to the ADCC and CMP respectively. The other end is the same as a standard ADCC cable.

The CMP connects to the CPU via two 50-pin ribbon cables which mount on J1 and J2.

5-10. CMP Power Supply Requirements

The CMP power requirements are +5 volts at 2.6 amperes, +12 volts at .06 amperes, and -12 volts at 0.06 amperes. The Power On (PON) signal is used to reset the CMP interface logic. The CMP uses 200 milliamperes of +5V battery backup power.

When PON is de-activated, it must remain so for a minimum of two microseconds to properly reset the microprocessor (MC5) and UARTS on the CMP. All power voltages must also remain stable during this two-microsecond interval. Connecting PON directly to a switch can cause noise on the PON line which does not meet the two-microsecond requirement and the MC5 or UARTS may be damaged.

5-11. CMP FIRMWARE FUNCTIONAL DESCRIPTION

The following paragraphs contain detailed descriptions the CMP firmware functions. The descriptions include system console interface, remote console (modem) interface, ADCC-system interface, control panel functions, overtemp shutdown, security specifications, and installation and configuration specifications.

5-12. Console Interface

5-13. Entering Commands. The CMP is connected only to the terminal at the lowest address (Channel 1 Device 0). This is the standard device for use by all diagnostics. If under MPE the MPE console is switched to another terminal, the user must realize that all diagnostics and communication with the CMP must be from the channel 1 device 0 terminal.

When the CPU is in the RUN state and MPE is operating correctly the CMP will usually be inactive except for special functions for use by the system engineer. The user will be able to enter console commands and also run a session from the console.

When MPE is running or the CPU hung is in the RUN state, the user can get the attention of the CMP by entering a CONTROL B character from the system or remote console. The only function of the CONTROL B character is to cause the CMP to prompt the user at the system console or remote console for a command. The user can then, invisible to the operating system, use the functions of the CMP.

When the CPU is halted and the CMP is enabled, the CMP will automatically prompt the user for a command.

If the CMP control functions are disabled, when the user enters a LOAD, START, DUMP, RUN, HALT, IOMAP, DISPLAY, or SELFTEST command the CMP will print the message 'DISABLED'. Set the CONTROL FUNC-

TIONS switch on the system control panel to ON before re-entering the command.

If the CMP maintenance functions are disabled, the CMP will print the message 'DISABLED' whenever the DISPLAY command is entered. Set the MAINT MODE switch on the system control panel to the ON position before re-entering the command.

5-14. Command List. The following list gives the commands accepted by the CMP operating system. CMP Maintenance Display commands are not included (refer to CMP Maintenance Mode manual, P/N 30090-90007).

HELP - This command prints the list of CMP commands. If the Maintenance Display is present, Maintenance Display commands are also listed.

HALT - This command causes the CPU run/halt flip-flop to be set to halt. This performs the same function as the HALT pushbutton on the system control panel.

RUN - This command causes the CPU run/halt flip-flop to be set to run. This performs the same function as the RUN pushbutton on the system control panel.

DUMP - This command will cause a dump to be performed to the dump device by reading the soft dump facility from the disc whose channel and device numbers are specified in the control panel DUMP thumbwheel switches. If the system is in RUN state the message "IS IT OK TO ABORT THE SYSTEM?" will be displayed. The user must enter YES to perform the dump.

LOAD - This command causes a cold load to be performed from cold load device specified by the control panel LOAD thumbwheel switches. If the system is in the RUN state the message "IS IT OK TO ABORT THE SYSTEM?" will be displayed. The user must enter YES to perform the load.

START - This command causes a warm start to be performed. If from the start device specified by the control panel START thumbwheel switches. If the system is in the RUN state the message "IS IT OK TO ABORT THE SYSTEM?" will be displayed. The user must enter YES to perform the start.

SELFTEST - This command initiates a selftest of the system from the system is in the RUN state the message "IS IT OK TO ABORT THE SYSTEM?" will be displayed. The user must enter YES to continue the selftest. Refer to the

CMP/System Selftest manual (P/N 30090-90005) for more information on selftest.

SHUTTEST - This command tests the power fail and overtemp shutdown circuitry on the CMP and in the power supply. The command causes the message 'Cycle Power To Restart System' and then pulls PFW- low on the backplane. This should cause all power to be shut off in the system except the memory supply. To bring the system up after this test, cycle the system main power breaker. If the test fails, the CMP prints the message 'Test Failed'.

DCTEST - This command causes testing of the RS-232C signals on the CMP. A special test adapter (P/N 30090-60052) must be installed between J3 on the CMP and the standard CMP cable. The CMP cannot be in remote mode while performing this test. See the CMP/System Selftest manual (P/N 30090-90005) for more DCTEST information.

LOG - This command causes a display of actions performed or detected by the CMP. The items which are entered in the log are:

Display On	'Display' command entered.
Dump	'Dump' command entered.
Halt	CPU went to halt.
Halt Command	The Halt command was used.
IOMAP	'IOMAP' command entered.
Load	'LOAD' command entered.
Power On	Power-on reset to CMP when battery power was lost.
Powerfail/Reset	A powerfail occurred or the PON signal went low without loss of memory backup power.
Run	CPU went to run.
Selftest OK	System selftest passed.
Selftest Failed	System selftest failed.
Shuttest	Power shutdown test performed.

Shuttest Failed Poser shutdown test failed.

Start 'START' command entered.

These events are listed along with the elapsed time (not including power off time) since the event occured. The last 63 events are shown. The log is retained during a power failure since it is stored in memory which is on battery backup. An example is:

EVENT LOG

Days	Hrs	Min	Since Event
2	23	05	Power On
	3	20	Overtemp Shutdown
	3	20	Powerfail/Reset
	2	25	Halt
	2	20	Start Failed
	2	05	Halt
	2	03	Load Failed
	1	51	Halt
	1	50	Cold Load
	1	50	Selftest Failed
		03	Load

DISPLAY - This command causes the Maintenance Display to appear on the screen. See the CMP Maintenance Mode manual (P/N 30090-90007) for more information.

HARDCOPY - This command causes the maintenance display to be printed without using the cursor addtressing and memory lock functions present on most CRT terminals. The display will be reprinted completely after every screen update.

SPEED - This command allows the user to change baud rates when MPE is not running. The receive and transmit baud rates are specified in the command (i.e. SPEED <rate> <rate>). The receive and transmit baud rates must be identical to be compatible with MPE and the ADCC. This command is identical to the MPE command to change baud rates.

:SPEED - This command is identical to the standard SPEED command but it allows the CMP and MPE to be set to the same speed simultaneously. Use this command when MPE is running.

IOMAP - This command causes the current system configuration to be printed. The memory size, control panel switch settings, and all channels and devices in the system are identified.

Invalid command names will cause the following message to be displayed:

'INVALID COMMAND, USE HELP FOR INFO'

5-15. Halt Messages. When the system halts, the CMP will output a message. The possible messages are:

Halt - This indicates a halt caused by the CMP or system control panel.

Halt XX - This indicates the CPU executed a HALT instruction. The parameter (XX) is the halt parameter from the instruction in decimal. The normal halt after a =SHUTDOWN is HALT 15.

System Halt XXX - This indicates a system halt. The halt number (XXX) is in decimal. The following is a list of standard system halt numbers:

1 STTV with source seg<2 (including internal and external interrupt setup).

2 Absence on ICS.

3 Trace or absence with nseg#<2.

4 Sys CSTL=0.

5 Stack overflow on ICS.

6 Load/Start/Dunp - channel program timeout.

7 Load/Start/Dump - bootstrap channel program checksum error.

8 Load/Start/Dump - bootstrap channel program abort.

9 PSEB Macro Found.

Hardware Failure XXX - This indicates an error was detected by the CPU resident section of selftest. The number (XXX) is in decimal. See the CMP/System Selftest manual for descriptions of the number.

The halt numbers are read from SP0 in the CPU. Only the lower eight bits of SP0 are examined. Values in the range !1 - !1F indicate system halt numbers. Values in the range !20 - !EF indicate hardware failure numbers. Numbers in the range !F0 - !FF indicate halt instruction numbers and only the lower four bits

are used to generate the halt number. In this case a halt instruction can be seen in the CIR. Zero indicates a halt from the CMP or System Control Panel.

5-16. Debug Commands. Several commands exist for CMP test and debug. These commands are not for use by customers and are not listed by the HELP command. Each command must be preceeded by a CONTROL Z. The commands are:

P <hex number>. This command causes the microprocessor (MC5) on the CMP to start executing code at the address specified by the hex number.

R <hex number>. This command does a memory read from the address specified. The value stored at that memory adress is printed. Note that reading from the UARTS is done with the R command since the UARTS exist in memory space.

W <hex number> <hex number>. This command does a memory write to the address specified by the first hex number. The second hex numbergives the data to write to that location.

I. This command prints the value read from all eight CMP external registers.

O <hex number> <hex number>. This command performs an I/O write to the external register specified by the first hex number (0-7). The second hex number gives the data to write.

S. This command sets CMP memory locations !700-!7FF to zero. Then the first failure detected during SELFTEST or IOMAP will cause the current stack area starting at location 0 to be moved to the stack buffer area starting at location !700. Only the first failure will be logged. The "S" command must be re-entered to log the next failure.

5-17. Remote Console (Modem) Interface

The remote console operates in parallel with the local console. The CMP firmware makes absolutely no distinction between remote and local commands. All events are displayed on both consoles. Use of the :SPEED or SPEED command should be used to ensure that the baud rate of the system console is the same as that of the remote console.

5-18. ADCC-System Interface

The ADCC and the system will never see any effect of the CMP except under one situation. When the user enters a CONTROL B char-

acter, it is sent to both the CMP and ADCC. Hence the ADCC will receive a CONTROL B character when the system is operating and the user wishes to suspend the operating system. Upon receipt of the CONTROL B character, the CMP will disable the ADCC from sending or receiving from the local and remote consoles until the user has entered their command followed by a carriage return. The CMP will delete the CONTROL B character from the system buffer by sending a backspace to the ADCC.

5-19. System Control Panel Functions

The CMP communicates commands and gets status from the control panel serially. The commands to the control panel are: HALT, RUN, START, DUMP, and LOAD. The status from the control panes includes START, DUMP, LOAD, RESET, OVERTEMP, MAINTENANCE DISPLAY ENABLE, CONTROL FUNCTIONS ENABLE, and REMOTE ENABLE.

5-20. Overtemp Shutdown

The CMP monitors the overtemp warning indicator from the control panel. If an overtemp conditin occurs, the CMP logs the event so that it can be read out in the log at a later time. Then the CMP will print a message to the system console stating that the system is being shut down due to overheating. The CMP then asserts PFW (Power Fail Warning) which causes the power control board to shut down all DC power except memory power. The user must cycle the system main power breaker to restore power.

5-21. Security Specifications

Security with the CMP is similar to security on the HP 3000/33. Switches exist behind a locked door to allow three levels of security. In the first level of security the system can be locked off or on, with no capability for RUN, HALT, WARMSTART etc. except for the MPE SHUTDOWN command if the system is running MPE.

The second level of security allows the RUN, HALT, IOMAP, SELFTEST, DUMP, WARMSTART, and COLDLOAD capabilities but does not allow the Maintenance Display.

The third level of security allows everything the second does and allows the Maintenance Display also. The switches that allow these functions are on the control panel. The CMP examines the control panel status to determine what capabilities to allow.

Remote capability is disabled by a switch on the system control panel. Thus the user must remember to reset the switch after use to prevent unauthorized persons from calling in from a remote location and acting as the system console operator.

5-22. Installation and Configuration Specifications

The CMP is adjacent to the CPU and is connected to the CPU by two ribbon cables. The CMP contains a bank of eight switches on the board edge. Unused switches should be in the down (closed) position. The switches have been assigned the following functions where B1 is the uppermost switch:

B1 - Automatic Warm Start. When the switch is in the up (open) position, the CMP will cause an automatic warm start whenever the system is powered on. When the switch is in the down (closed) position, the CMP will not cause an automatic warm start.

B3 - CMP Disable. When the switch is in the up (open) position, the CMP will be disabled. It will not enable any of its interface circuitry. Two of the LEDs on the edge of the CMP will blink while the switch is up. The console to ADCC path will still be operable.

B8 - Loop Selftest. Setting this switch to up (open) will cause SELFTEST and DCTEST commands to cause the test to loop regardless of errors. In the down (closed) position the DCTEST will not loop and the SELFTEST will halt on first failure.

There is a package of eight switches on the PCA. These switches should normally be in the closed position. (See figure 5-2.)

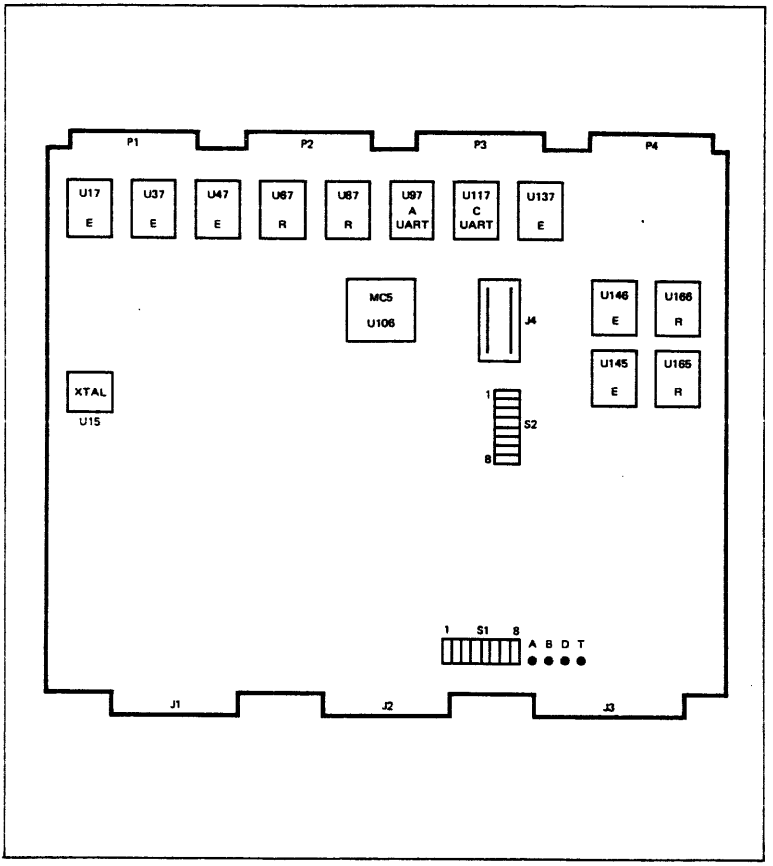


Figure 5-2. CMP PCA

SECTION VI

MEMORY SUBSYSTEM

FUNCTIONAL DESCRIPTION

6-1. INTRODUCTION

This section contains the description of the HP 3000/44 Memory Subsystem. This description includes the memory arrays and the memory control and logging PCA. The system block diagram is used as a guide for the following discussions of the Memory Subsystem.

6-2. GENERAL

The HP 3000/44 Memory Subsystem (figure 6-1) provides high-speed, error-correcting main memory storage. Data is stored in 39-bit words; 32 data bits and 7 error detecting and correcting bits. The memory subsystem consists of a memory control and logging (MCL) PCA and up to eight semiconductor memory arrays (SMA). The MCL can control up to eight SMAs for a total of 2 megabytes of main memory when 16k RAMS are used, or up to 4 megabytes when 64k RAMS are used. However, a system may operate with one or two MCLs. This provides for up to 4 megabytes of memory. The LOWER/-UPPER switch on the MCL sets the lower or upper MCL at the two-megabyte boundary.

The subsystem functions in one of four operations; Read, Write, Read and Write Ones, and Memory Command Status. The Read operation reads out a 32-bit data word to the MCL which, in turn, places the addressed 16-bit data word onto the Intermodule Bus (IMB). The Write operation consists of a read before write. The 32-bit word is read from memory and the 16-bit word being written replaces the appropriate half of the 32-bit word. The 32-bit word is then rewritten into memory. The Read and Write Ones operation performs a standard read from a memory location, after which time, that memory location is written with all ones. The Memory Command Status (MCS) command provides for error logging, error correction and detection, refresh, initialization, disabling parity checking and error correction.

Operating power for the refresh and power fail circuits of the MCL is supplied by a rechargable battery pack in the power supply. The power supply can support up to two megabytes of memory (using 16K RAMs). Two power supplies are required for additional memory. When AC power is removed or lost, power is obtained from the battery. Power from the battery is available a minimum of 15 minutes, depending upon memory size and battery condition, to maintain memory data.

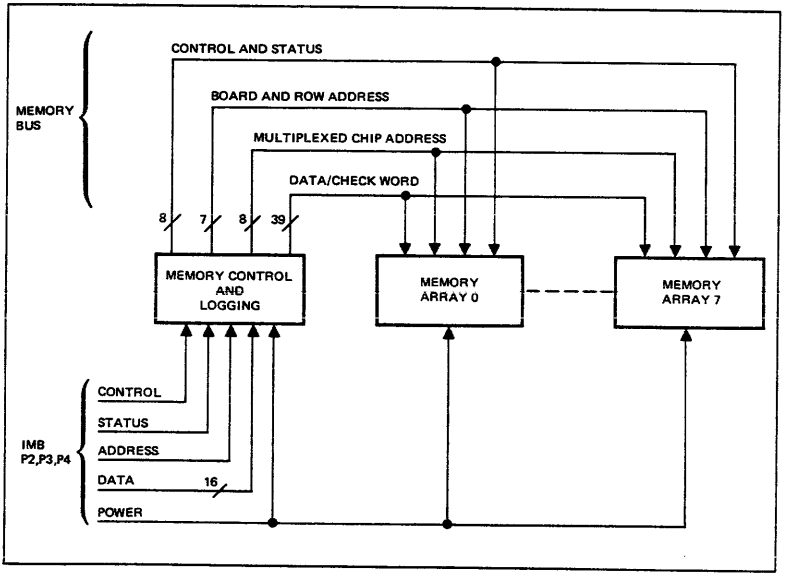


Figure 6-1. Memory Subsystem Block Diagram

6-3. Memory Control and Logging

The memory control and logging (MCL) PCA contains the read/write control circuits, address and data registers, refresh circuits, error detection/correction logic, and error logging array.

The MCL is responsible for all IMB handshake protocol, timing generation, address multiplexing, parity code generation, refresh operation, error detection, and error correction and logging. The MCL talks directly to the the IMB, relaying data, address, and control information to the memory arrays through the memory bus. The memory bus is reserved solely for the memory subsystem. The MCL automatically initiates the refresh cycle every 16 to 31 microseconds, depending upon temperature. Duration of the refresh period is approximately 550 nanoseconds.

The MCL also contains and updates an error logging array (ELA), which is a 4K static RAM, for all correctable and double-bit data errors that have occurred in all 16K RAM chips. The contents of the ELA are available to te software by means of the memory command/status (MCS) command.

6-4. Semiconductor Memory Arrays

The semiconductor memory array (SMA) contains the circuits that provide module address decoding. All communications with the memory arrays are governed by the MCL.

The individual memory chip is a 16K by 1 storage device. The chips are physically arranged on each SMA in eight rows, and grouped into four logical rows. (See figure 6-2.) Each RAM in a logical row contains one bit for each storage word (B0-B31), and the check bits (C0-C6). This arrangement provides for 256 Kbytes of storage per SMA.

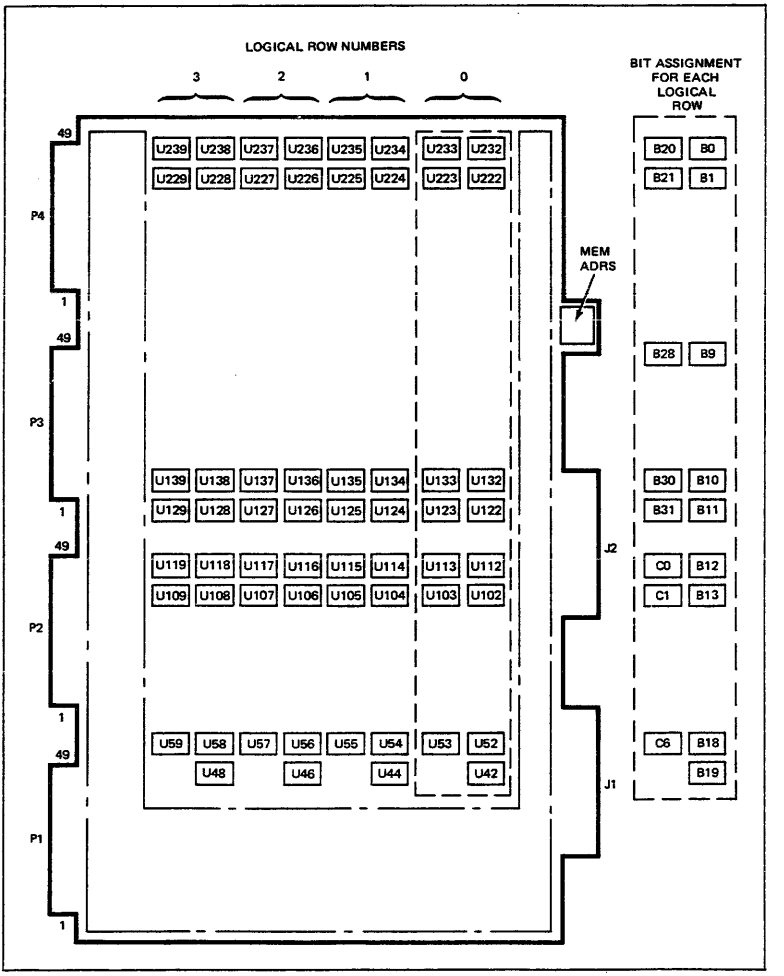


Figure 6-2. RAM Matrix Organization

6-5. Data Word

Internally the memory functions as a 39-bit word, 32 data bits and 7 check bits. All single-bit errors are detected, corrected, and logged. All double-bit errors are detected and logged. Odd parity is used on all the check bits. The internal 32-bit data word contains two 16-bit CPU words, with the least significant bit A15 of the IMB address being used to identify each. The even word (A15=0) designates the A-word and the odd word (A15=1) designates the B-word. The internal data bus from the MCL to the SMA's is 39 bits wide. The format is shown in figure 6-3.

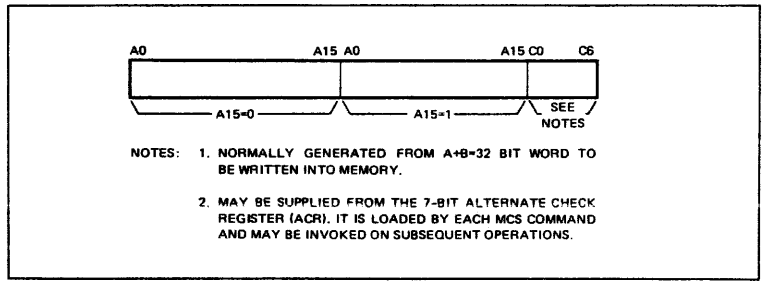


Figure 6-3. Data Word Format

6-6. Address Word

The MCL accepts 22-bit addresses across the IMB, address bits A0 through A15 and extended address bits E1 through E6. Bits E8 and E7 are are not used. Each address corresponds to one 32-bit data word stored in a memory location.

Each memory array module stores 256 Kbytes in four logical rows of 16K RAM chips. Two buses are used to address the SMAs, the board and row address bus and the multiplexed chip address bus. Bits A0, and E1 through E6 address an SMA and the logical row on that SMA. (See figure 6-4.) Bit E5 is used to identify the first or second MCL, in the event two are used. These two bits are not passed on to the SMAs. The chip row and column addresses are two seven-bit words that are time multipexed onto the multiplexed chip address bus. Bit A15 indicates the A and B words. Each address represents one 16-bit CPU word.

If non-existent memory is addressed, all ones are returned without parity. When non-existent memory chips are addressed on a memory array, all zeros are returned without parity. An example of the latter is when a memory board is only partially loaded.

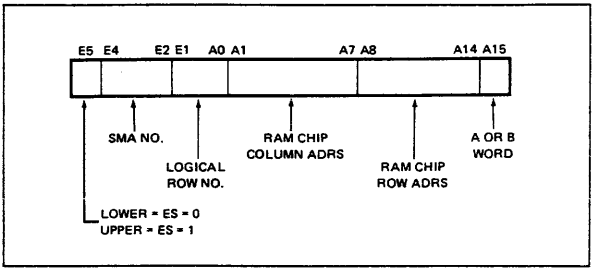


Figure 6-4. Address Word Format

6-7. MEMORY OPERATIONS

The memory subsystem functions in the following four operations:

Operation	Symbol	IMB Opcode
Read Word	R	000
Read Word and Write Ones	RW1	001
Write Word	W	010
Memory Command and Status	MCS	101

Read and write allow reading data from or writing data to the memory by any bus controller such as the CPU or an I/O channel. Read and write ones is an operation whereby a memory location is read and then ones are written into that location. This is used only when two CPUs are available and indicates to either CPU that the location read no longer has useful data stored. The memory command and status allows control, modifying, and reading of the read, write, and read and write ones operations, reads or modifies the contents of the error logging array, and retrieves status information.

6-8. Read and Write

The read cycle reads out a 32-bit data word with the checkbits onto the memory bus from the address supplied on the IMB. The MCL reads the checkbits for error status, unpacks the 32-bit word

into two 16-bit data words (A and B), and places the addressed data word onto the IMB. If A15=0, word A is addressed. If A15=1, word B is addressed.

If a correctable error is detected during the read operation, the internal cycle is transformed into a write-type operation in which the corrected 32 data bits are rewritten with correct check bits into the same address. If a double-bit error is detected, it is logged in the ELA and the IMB-PER line is asserted on the IMB.

Since there are two IMB data words per one memory word, address bit A15 is used to identify the A and B words. Table 6-1 summarizes error conditions and address for read and write ones operations. The MCS command is used to retrieve error status.

In the write operation, the full 32-bit data word plus 7 check bit contents of the internal addressed word must be read, checked for data errors, correct single-bit errors, and latched before the writing phase can take place. Hence, every memory write operation is internally a read-modify-write operation. This is also true of RW1. Since a parity error on the read part of a write operation is just as much a disaster as on a read opcode, it is logged in the ELA, stored in the WPER, and asserted on the IMB-PER line on the next read operation.

Table 6-1. Error Conditions and Actions

Memory Condition	Error Condition	Error Logged	IMB Assert	Set MCL Status Bits	Internal Action
Read A/B	None	No	-	-	Data to IMB
	Single bit	Yes	-	E	Corrected data to IMB with write
	Double bit	Yes	PER-L	P	Uncorrected data to IMB
Read and write ones A/B	None	No	-	-	Data to IMB and write ones
	Single bit	Yes	-	E	Corrected data to IMB and write ones
	Double bit	Yes	PER-L	P	Uncorrected data to IMB and abort write ones
Write A/B	None	No	-	-	Read data, replace A/B word and write
	Single bit	Yes	-	E	Corrected data, replace A/B word, and write
	Double bit	Yes	-	P,WPER	Read data, no correction, and abort write
Initialize	-	No	All Reset	Ignore read data, force A=B, and write	

On writes, the bus handshake precludes asserting parity error (PER-L) during the write operation. It is stored (WPER) and the IMB-PER-L is asserted once on the very next read or read and write ones operation. WPER being set does not inhibit any of the operations indicated, but forces the PER-L on the following read or read and write ones. Also error logging is not duplicated when PER-L is forced on.

6-9. Memory Status and Command

The memory and command operation enables the software to set up special conditions within the MCL as follow:

- The MCL can modify the normal patterns of read, write, and read and write ones. This is accomplished with two independent registers on the MCL, the alternate check register (ACR) and the altered status register (ASR). These registers are loaded on the execution of each MCS operation. Only the ASR is cleared by PON, IMB SRST-L, or the MCL RESET switch. The subsequent use of the ACR is controlled by the ASR, which for example, can disable error correction or inhibit error logging.

- The contents of the error logging array (ELA) on the MCL can be interrogated and modified.

- Status information can be retrieved for diagnostics and system operation.

All information from the CPU to the MCL is sent over the IMB address bus while the status information back to the CPU is sent on the IMB data bus. Since the status word contains information from a specific address, the content of the address bus is functioning as a normal address. At the same time, the ASR is loaded from the address and the ELA is modified (if necessary) according to the information on the address bus. Therefore, the content of the address bus is acting simultaneously as both an address and an instruction. The result of this is that when executing an MCS operation, four actions always occur simultaneously:

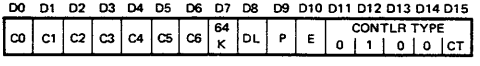
1. A 16-bit status word is returned. The contents of the status word are defined in figure 6-5. (Execution of an MCS command reads only the check bits from an array board.)

2. The content of the location addressed by bits E5 through A7 in the ELA is read out and returned as status bit D8. (See figure 6-6.)

3. Address bits A0 through A6 are loaded into the alternate check register (ACR) for possible use on subsequent writes.

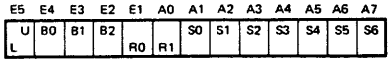
4. Address bits A10 through A15 are loaded into the altered status register (ASR). (See figure 6-7.) Zeros in the ASR define normal operation, hence, an MCS with bits A10 through A15=0 restores memory to normal. All ones in the ASR for bits A10 through A13 modify subsequent reads, reads and writes ones, and writes until an MCS with all zeros is executed, or the ASR is reset.

INITIALIZATION - Bits A10 and A12 in the ASR set up an initialize state for writes that forces the data word from the IMB into both A and B memory words. This enables known data and the proper check bits to be written into every 39-bit memory word from a condition of random data. This must precede normal use of memory.



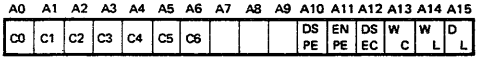
Bits D0 thru D6	Check bits from the location addressed by bits E6 thru A14 of the address word (A15 is not used).
Bit D7	Memory chip type from the accessed SMA 1 = 64K bit RAM 0 = 16K bit RAM
Bit D8	Data bit from the ELA for ELA address bits E4 thru A7 1 = Error logged 0 = No error
Bit D9	Noncorrectable error since last MCS
Bit D10	Correctable error since last MCS
Bits D11 thru D15	Controller type - octal 10 = 0 to 8 Mbyte or first 2 Mbytes 11 = second contrlr 2 to 4 Mbytes

Figure 6-5. Status Word Definition



Bit E5	Second controller select bit when there are two Mbytes per controller. MCL select switch must be correctly set on both controllers. If bit E5=1 and the second MCL is present, bits E4 thru A7 of the address word address the second controller ELA. Bit E5 is in the don't care state for a single MCL with the select switch in the middle position.
Bits E4 thru E2	SMA number (0 to 7)
Bits E1 and A0	Logical row number on SMA (0 to 3)
Bits A1 thru A7	Syndrome code bits

Figure 6-6. Error Logging Array Address Bits E4 thru E7



Bits A0 thru A6	Each MCS instruction loads address bits A0-A6 into the alternate check register, which supplies the check bits on subsequent writes if bit A13 was set on the last MCS.
Bit A10 (see note)	Disables PER. Only single-bit errors are logged. Double bit errors are latched into bit D9 (P) of the status word. Resets the WPER bit.
Bit A11	Disables the logging of all errors on R, RW1, and W. Single-bit errors are latched into bit D10 (E) and double-Bit errors are latched into bit D9 (E) of the status word.
Bit A12 (see note)	Disables error correction on a read. No rewrite occurs on single-bit errors on a read.
Bit A13	Use the ACR on subsequent writes including the initialize write.
Bit A14	Write bit A15 into the ELA address which is specified by bits E4-A7. Previous value is returned in bit D8 (DL) of the status word. This makes the MCS into a "read the ELA and leave alone" (A14=0), or "read-modify-write" (A14=1).
Bit A15	DL - Data bit to be written into the ELA.

Figure 6-7. Altered Status Command Bits

Note. If bits A10 and A12 are both set, then:

1. On subsequent write instructions, the memory locations are initialized to both words equal to the data supplied, with the check bits generated by the memory parity trees.

2. All error logging is inhibited on writes.

3. On read and read and write ones, bits A10 and A12 exert normal functions.

4. The ACR is used (if bit A13 is set) to supply the check bits instead of the parity trees. This provides total control for writing into the 39-bit word.

Figure 6-7. Altered Status Command Bits (Continued)

6-10. Refresh

The RAM chips in the memory arrays are dynamic in nature and require periodic refreshing to prevent stored data from decaying away. The chips are refreshed by the MCL at the same time. Refresh occurs at a rate based upon the temperature of the array. At 25 degrees C (77 degrees F), the refresh occurs once 31 microseconds. At 70 degrees C (158 degrees F), refresh occurs once every 16 microseconds. The refresh period is approximately 550 nanoseconds in duration. At 70 degrees C, a 3.4 percent loss of memory availability is expected, while at 25 degrees C, the memory is unavailable for 1.7 percent of the time.

6-11. ERROR DETECTION AND CORRECTION

Error detection is accomplished by adding seven parity bits to the 32 data bits so that a single data error generates an odd number of signals in the seven outputs of the parity tree. Also, a unique seven-bit syndrome error code is produced for each of the 32 data bits and a unique code for specific groups of double-bit error pairs. This error code is decoded to one in 32 and is the means for correcting (complementing) single-bit errors. Any double-bit error (data and/or check bits) generates an even number of signals in the parity tree outputs and will result in the

assèrtion of parity error PER-L to the IMB for 500 nanoseconds. Detection and correction do not occur within the normal memory cycle. Read access time is 70 nanoseconds longer with correction. Any single-bit error sets the E-status bit and any double-bit error sets the P-status bit. The full 32-bit error detection code and resulting octal syndrome error code are shown in figure 6-8.

6-12. ERROR LOGGING

All detected errors are recorded according to chip location in an error logging array (ELA) static 4K RAM. The RAM is located on the MCL. Seven bits of syndrome error code and five bits of memory address determine the error logging address in which a one is stored in the ELA.

The ELA is organized in a 4096 x 1 bit array so there are 12 bits of address. The five most significant bits represent the five most significant bits of an SMA memory address (B0, Row 0, etc.). The seven least significant bits of the error logging address represent the error syndrome code (S0 through S6).

The ELA must be cleared to all zeros (after initialization) using 4096 MCS commands before valid logging starts. The ELA is later read under program control by means of the MCS command. Any ELA location containing a one means that an error was detected.

Table 6-1 is the complete table of all possible (128) syndrome error codes. There are 39 possible single-bit errors and 63 possible error codes for various groups of error pairs. One code represents the no-error condition and the remaining 25 error codes are for three-bit (or more) errors.

The size of the ELA permits a unique code for each single-bit error and a unique code for double-bit error pairs. Any one error pair will cause its group syndrome error code to supply the S0 through S6 part of the ELA address for logging. With a known or suspected single-bit error, a second bad bit can be located, using the data given in table 6-1. A normal functioning memory should never log errors that occur in the 25 multiple-bit error category.

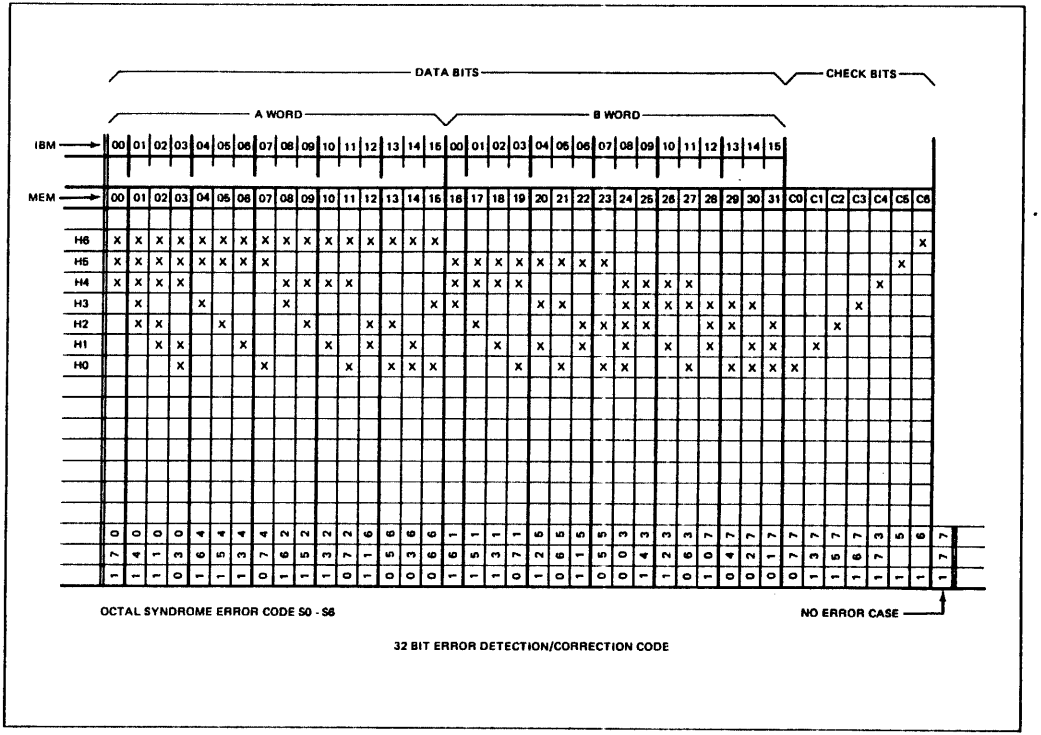


Figure 6-8. 32-Bit Error Detection/Correction Code

Table 6-2. Octal Syndrome Error Codes

OCTAL SYNDROME ERROR CODE	
104	NOT A SINGLE OR DOUBLE BIT ERROR
103	1/ 6 2/ 4 8/ 12 16/22 17/20 24/32 25/33 27/31 28/36
102	NOT A SINGLE OR DOUBLE BIT ERROR
101	NOT A SINGLE OR DOUBLE BIT ERROR
100	0/28 1/33 2/35 3/29 5/26 6/25 7/24 8/22 9/20 12/16
077	32
076	0/19 3/18 4/21 5/23 7/37 8/27 11/36 12/31 13/34 14/33 15/35 32/38
075	0/11 3/10 4/15 5/13 6/14 7/38 16/27 19/36 20/30 21/35 22/31 23/34 32/37
074	7
073	0/ 7 3/ 6 8/15 9/13 10/14 11/30 16/21 17/23 19/37 24/28 25/29 26/30 27/35 32/36
072	11
071	19
070	0/32 1/29 2/31 3/33 4/27 7/36 8/21 9/23 11/37 13/17 14/18 15/16 19/38
067	4/ 7 8/11 15/38 16/19 21/37 27/36 28/31 29/34 30/33 32/35
066	15
065	21
064	0/27 2/24 3/26 4/32 5/29 6/30 7/35 8/19 11/16 14/20 15/37 21/38
063	27
062	0/21 1/23 3/20 4/19 7/16 8/32 9/29 10/30 11/35 12/24 13/25 14/26 15/36 27/38
061	0/15 1/13 4/11 7/ 8 16/32 17/29 18/30 19/35 21/36 22/24 23/25 27/37
060	NOT A SINGLE OR DOUBLE ERROR
057	2/ 3 5/ 7 9/11 12/14 13/30 17/19 23/37 24/26 25/27 28/30 29/35 31/33 32/34
056	13
055	23
054	1/27 4/29 5/32 6/31 7/34 9/19 11/17 13/37 14/22 23/38
053	NOT A SINGLE OR DOUBLE BIT ERROR
052	0/23 1/21 3/22 5/19 7/17 8/29 9/32 10/31 11/34 13/36 15/25
051	0/13 1/15 2/14 3/12 5/11 7/ 9 16/29 17/32 18/31 19/34 20/24 21/25 23/36
050	NOT A SINGLE OR DOUBLE BIT ERROR
047	29
046	1/19 4/23 5/21 9/27 10/24 11/25 12/30 13/35 14/28 15/34 29/38
045	1/11 4/13 5/15 17/27 18/24 19/25 20/31 21/34 22/30 23/35 29/37
044	NOT A SINGLE OR DOUBLE BIT ERROR
043	1/ 7 8/13 9/15 16/23 17/21 24/33 25/32 26/31 27/34 29/36
042	NOT A SINGLE OR DOUBLE BIT ERROR
041	NOT A SINGLE OR DOUBLE BIT ERROR
040	0/29 1/32 2/30 3/28 5/27 6/24 7/25 8/23 9/21 13/16 15/17
037	0/ 3 6/ 7 10/11 12/13 14/38 18/19 20/21 22/23 24/25 26/27 28/29 30/35 31/34 32/33
036	14
035	NOT A SINGLE OR DOUBLE BIT ERROR
034	1/24 3/36 4/30 5/31 6/32 7/33 10/19 11/18 12/23 13/22 14/37 15/20
033	NOT A SINGLE OR DOUBLE BIT ERROR
032	2/23 3/37 6/19 7/18 8/30 9/31 10/32 11/33 14/36 15/26
031	0/14 2/13 3/38 6/11 7/10 16/30 17/31 18/32 19/33 20/27 21/26
030	3
027	30
026	3/16 6/21 7/20 9/24 10/27 11/26 12/29 13/28 14/35 15/33 30/38
025	3/ 8 4/14 6/15 17/24 18/27 19/26 20/32 21/33 22/29 23/28 30/37
024	NOT A SINGLE OR DOUBLE BIT ERROR
023	3/ 4 8/14 10/15 18/21 19/20 24/34 25/31 26/32 27/33 30/36
022	NOT A SINGLE OR DOUBLE BIT ERROR
021	NOT A SINGLE OR DOUBLE BIT ERROR
020	0/30 1/31 2/29 3/35 5/24 6/27 7/26 10/21 11/20 14/16 15/18
017	31
016	2/19 3/17 6/23 7/22 8/24 12/32 13/33 14/34 15/28 31/38
015	2/11 3/ 9 5/14 6/13 7/12 16/24 20/29 21/28 22/32 23/33 31/37
014	NOT A SINGLE OR DOUBLE BIT ERROR
013	2/ 7 3/ 5 9/14 10/13 11/12 18/23 19/22 24/35 25/30 26/29 27/28 31/36
012	NOT A SINGLE OR DOUBLE BIT ERROR
011	NOT A SINGLE OR DOUBLE BIT ERROR
010	0/31 1/30 2/32 3/34 4/24 10/23 11/22 12/19 13/18 14/17
007	1/ 3 12/15 20/23 21/22 24/36 28/32 29/33 30/34 31/35
006	NOT A SINGLE OR DOUBLE BIT ERROR
005	NOT A SINGLE OR DOUBLE BIT ERROR
004	0/24 2/27 3/25 4/31 5/30 6/29 7/28 12/21 13/20 15/22
003	24
002	2/21 8/31 9/30 10/29 11/28 12/27 13/26 14/25 24/38
001	1/14 2/15 16/31 17/30 18/29 19/28 22/27 23/26 24/37
000	NOT A SINGLE OR DOUBLE BIT ERROR

LIST OF ALL POSSIBLE SYNDROME ERROR CODES FOR SINGLE ERRORS (39) AND DOUBLE BIT ERROR PAIRS (63)

LEGEND:

0	=	D0
31	=	D31
32	=	C0
33	=	C1
34	=	C2
35	=	C3
36	=	C4
37	=	C5
38	=	C6

Table 6-2. Octal Syndrome Error Codes (Continued)

OCTAL SYNDROME ERROR CODE														
177	NO ERROR													
176	38													
175	37													
174	0/36	1/25	4/35	5/34	6/33	7/32	8/16	9/17	10/18	11/19	12/22	13/23	15/21	37/38
173	36													
172	0/37	2/22	4/16	5/17	6/18	7/19	8/35	9/34	10/33	11/32	15/27	36/38		
171	0/38	2/12	3/14	4/ 8	5/ 9	6/10	7/11	16/35	17/34	18/33	19/32	20/26	21/27	36/37
170	0													
167	35													
166	0/16	1/17	4/37	6/20	7/21	8/36	9/25	10/26	11/27	12/28	13/29	14/30	15/32	35/38
165	0/ 8	1/ 9	4/38	7/15	16/36	17/25	18/26	19/27	20/33	21/32	22/28	23/29	35/37	
164	4													
163	0/ 4	1/ 5	8/38	11/15	16/37	18/20	19/21	24/31	25/34	26/33	27/32	35/36		
162	8													
161	16													
160	0/35	1/34	2/28	3/30	4/36	4/36	5/25	6/26	7/27	8/37	10/20	11/21	15/19	16/38
157	34													
156	0/17	1/16	2/18	5/37	6/22	7/23	8/25	9/36	12/33	13/32	14/31	15/29	34/38	
155	0/ 9	1/ 8	2/10	5/38	6/12	7/13	16/25	17/36	20/28	21/29	22/33	23/32	34/37	
154	5													
153	0/ 5	1/ 4	2/ 6	9/30	10/12	11/13	17/37	18/22	19/23	24/30	25/35	26/28	27/29	34/36
152	9													
151	17													
150	0/34	1/35	2/33	3/31	4/25	5/36	9/37	10/22	11/23	12/18	13/19	17/38		
147	0/ 1	4/ 5	8/ 9	13/15	16/17	20/22	21/23	25/36	28/33	29/32	30/31	34/35		
146	NOT A SINGLE OR DOUBLE BIT ERROR													
145	NOT A SINGLE OR DOUBLE BIT ERROR													
144	0/25	1/36	2/26	3/24	4/34	5/35	6/28	7/29	8/17	9/16	12/20	13/21	15/23	
143	25													
142	1/37	2/20	4/17	5/16	8/34	9/35	10/28	11/29	12/26	13/27	14/24	25/38		
141	1/38	4/ 9	5/ 8	16/34	17/35	18/28	19/29	22/26	23/27	25/37				
140	1													
137	33													
136	0/18	2/17	3/19	4/20	5/22	6/37	8/26	10/36	12/34	13/31	14/32	15/30	33/38	
135	0/10	2/ 9	3/11	5/12	6/38	7/14	16/26	18/36	20/35	21/30	22/34	23/31	33/37	
134	6													
133	0/ 6	2/ 5	3/ 7	9/12	10/38	11/14	16/20	17/22	18/37	24/29	25/28	26/35	27/30	33/36
132	10													
131	18													
130	0/33	1/28	2/34	3/32	4/26	6/36	8/20	9/22	10/37	12/17	14/19	18/38		
127	1/ 2	4/ 6	8/10	14/15	16/18	20/37	26/36	28/34	29/31	30/32	33/35			
126	NOT A SINGLE OR DOUBLE BIT ERROR													
125	20													
124	0/26	2/25	3/27	4/33	5/20	6/35	7/30	8/18	10/16	14/21	20/38			
123	26													
122	0/20	1/22	3/21	4/18	6/16	8/33	9/28	10/35	11/30	12/25	13/24	14/27	26/38	
121	1/12	3/15	4/10	6/ 8	16/33	17/28	18/35	19/30	20/36	22/25	23/24	26/37		
120	NOT A SINGLE OR DOUBLE BIT ERROR													
117	0/ 2	5/ 6	9/10	12/30	13/14	17/18	22/37	24/27	25/26	28/35	29/30	31/32	33/34	
116	12													
115	22													
114	1/26	2/36	4/28	5/33	6/34	7/31	9/18	10/17	12/37	14/23	22/38			
113	NOT A SINGLE OR DOUBLE BIT ERROR													
112	0/22	1/20	2/37	3/23	5/10	6/17	8/20	9/33	10/34	11/31	12/36	15/24		
111	0/12	2/38	3/13	5/10	6/ 9	16/28	17/33	18/34	19/31	20/25	21/24	22/36		
110	2													
107	28													
106	1/18	2/16	4/22	5/20	9/26	10/25	11/24	12/35	13/30	14/29	15/31	28/38		
105	1/10	2/ 8	4/12	17/26	18/25	19/24	20/34	21/31	22/35	23/30	28/37			

32 = C0
33 = C1
34 = C2
35 = C3
36 = C4
37 = C5
38 = C6

6-13. CONFIGURATION GUIDE

6-14. Switch Settings

Memory Array (See figure 6-2.)

- MEMORY ADDR — An eight-position thumbwheel switch that sets the memory array address.

Memory Controller (See figure 6-9.)

- RESET (S1) — A momentary switch that forces all control logic and the E and P status bits to the reset state. This is equivalent to IMB PON (low) and SRST (low). The switch may be depressed with the memory active because the switch can only be active during memory refresh cycles.

- B-M-A — A three-position switch that sets the MCL for controlling the upper two megabytes of memory (B), the lower two megabytes of memory (A), or is set to the M-position when 64k RAM's are installed.

6-15. Test Lights

Five test lights on the MCL are service aids that indicate the following:

- Activity - Lights when the memory is active, including refresh

- Initialize Write - Lights when the memory is active doing writes in the initialize state.

- C Bit - When lit, indicates that the second MCL is installed, which addresses the upper 2 to 4 Mbytes of memory (16K RAMs only).

- E Bit - Lights when one or more correctable error has occurred.

- P Bit - Lights when one or more uncorrectable error has occurred.

Note: The E and P bits are latched until reset by one of the following actions:

1. The MCL RESET switch is depressed
2. The system reset SRST-L is activated
3. PON is activated when system power is turned on
4. An MCS command is executed

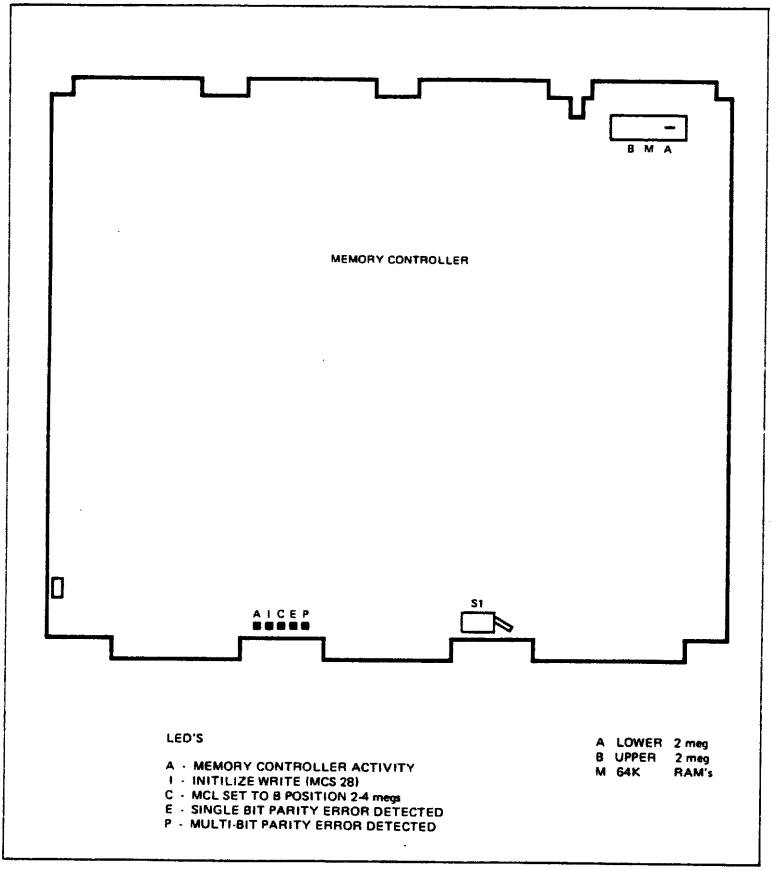


Figure 6-9. Memory Controller PCA

6-16. MEMORY ERROR LOGGING FACITLITY

The memory error logging facility allows the CE or system manager to examine the error history of memory. The facility consists of the following elements:

- Error correcting memory
- Memory error logging system process (MEMLOGP)
- Memory error log analysis program (MEMLOGAN)
- Memory error logging internal update program (MEMTIMER)

Memory error logging functions independent of standard system logging. The operator interfaces to system logging have no effect on memory logging.

6-17. Memory Error Logging System Process (MEMLOGP)

MEMLOGP is a system process that runs under MPE. Once initiated, MEMLOGP interrogates the MCL to obtain the latest information.

MEMLOGP is activated only during the inialization phase of MPE (warmstart, coldstart, reload, and update). If MEMLOGP cannot be activated during initialization, another attempt cannot be made until the system is brought up again.

MEMLOGP attempts to open the system memory error disc file MEMLOG (MEMLOG.PUB.SYS). A new file is created if one does not exist. If MEMLOG exists, the file will be opened without altering the information contained in the file. The file remains open as long as the system remains up. During the periods when MEMLOGP is accessing the file, it will lock and unlock the file as necessary to avoid multiple access. The log analysis program (MEMLOGAN) similarly locks and unlocks the file during access periods.

If an operational error is encountered by MEMLOGP, the process will display and error message and terminate. The message displayed is:

```
ST/<TIME>/MEMORY LOGGING ERROR#<ERRNUM>.LOGGING STOPPED
```

The range and definitions for <ERRNUM> are:

1-10	Internal MEMLOGP errors
1	FLOCK error on MEMLOG file
2	FUNLOCK error on MEMLOG file
20-500	File system errors involving MEMLOG file. All file errors encountered by MEMLOGP are fatal to the process and cause it to terminate.

Once the MEMLOG file has been opened, MEMLOGP periodically interrogates the error logging array (ELA). If errors have occurred, the MEMLOG file is updated. The ELA is interrogated and updated when MEMLOG is first activated and thereafter approximately once every hour. MEMLOGP prforms the following operations:

- Reads the appropriate MEMLOG record from disc
- Scans the ELA for errors
- Updates the error counter in the MEMLOG record for each location where an error occurred.
- Resets the ELA to a no-error condition
- Writes the updated MEMLOG record to disc.

6-18. Memory Error Logging Internal Update Program (MEMTIMER)

MEMTIMER (MEMTIMER.PUB.SYS) is the utility program that allows the user to modify the interval of time between successive memory log updates. The normal default interval is 60 minutes. This interval provides the average installation with an adequate log of the memory system. For other reasons, it may be desirable to modify the interval to allow increased monitoring of the memory performance.

MEMTIMER alters the current timing interval to a new value and terminates the current interval. This causes MEMLOGP to update the memory log file immediately and at the new specified interval.

A new timing interval is specified through the PARM parameter of the RUN command. There is no user dialogue with MEMTIMER. The PARM value is given as a positive integer greater than zero which

represents the number of seconds between log file updates. To begin memory logging at 10-second intervals, the following RUN command would be entered:

```
:RUN MEMTIMER;PARM=10
```

To return logging to the default interval (60 minutes), the following RUN command would be entered:

```
:RUN MEMTIMER;PARM=3600
```

Three error conditions are detected by MEMTIMER. If the PARM parameter of the RUN command is equal to or less than zero, then MEMTIMER will terminate after printing the following message:

```
** INVALID PARM (DELAY) VALUE **
```

The current time interval remains unchanged.

If MEMLOGP has been terminated, then MEMTIMER will terminate after printing:

```
** MEMORY LOGGING PROCESS NOT ACTIVE **
```

In this case there is no timing interval update.

If MEMLOGP is currently updating the memory log file, the following message will appear:

```
** MEMLOGP TIMER ENTRY NOT FOUND **
```

When this message appears, the timing interval will be updated. MEMTIMER should be run again to ensure that MEMLOGP will recognize the updated interval immediately.

Note that the default timing interval will become the current timing each time the system is brought up. Therefore, if a nondefault timing interval is desired, MEMTIMER must be run after each initialization of the system.

6-19. Memory Error Log Analysis Program (MEMLOGAN)

MEMLOAN (MEMLOGAN.PUB.SYS) is the utility that reads and interprets the error information logged and kept in the MEMLOG file. Because of the security placed on the MEMLOG file by the system, MEMLOGAN can successfully from an account other than PUB.SYS if:

The RELEASE command was entered for MEMLOG by the system manager.

MEMLOGAN will read MEMLOG and direct the contents to an output device. To direct the output to the line printer, the following

file equation must be entered:

```
:FILE OUT;DEV=LP
```

There is no user dialogue with MEMLOGAN. However, certain MEMLOG file handling operations are available through the PARM parameter of the RUN command. The following PARM values are recognized by MEMLOGAN:

PARM=0. Causes the current contents of MEMLOG to be printed on the output device. The contents of the file will not be changed. This is the default PARM value.

PARM=1. Causes the current contents of MEMLOG to be printed on the output device after which the file is reset to a no-error state. All previously logged errors are deleted from the log file.

NOTE

When a system is initialized for the first time or the memory size is changed, MEMLOGAN should be run with PARM=1 as soon as the system is up and running. This will ensure a clean MEMLOG file and that subsequent error counts are valid.

PARM=2. Causes the current contents of MEMLOG to be printed on the output device after which the file is deleted from the system. (This is the only way to remove the MEMLOG file from the system and normally only the system manager would use this PARM value.)

6-20. Output. MEMLOGAN output will vary according to whether the MEMLOG file is null or updated, and if updated, whether errors occur.

If the MEMLOG file is not empty, MEMLOGAN will print the date and time of the first and last log updates. If errors have been logged, the date and time of the first and last error logged will

also be printed. If no errors have been logged, MEMLOGAN will terminate after displaying the message:

```
LOGGING STARTED    -DATE:
LAST LOG UPDATED   -DATE:
 ***NO ERRORS LOGGED ***
```

If errors have been logged, MEMLOGAN will continue by printing a tabular interpretation of the information in the MEMLOG file. The format of the printout is shown in figure 6-10.

NOTE

When a system is initialized by MPE, (START or LOAD) the error logging array is cleared as part of this initialization. This keeps false errors from being logged by MPE after a power on. This also prevents parity errors causing a system failure from being logged on the disc. PRMDIAG (on the DUS) should be run immediately after a system failure where a multi-bit error is suspected to interrogate the ELA.

6-21. Errors. If an operational error is encountered by MEMLOGAN, the program will print the appropriate error information and terminate. A non-file system error causes the following message to be displayed:

```
*MEMLOGAN ERROR: <ERRNUM>:
```

Where <ERRNUM> 1= FLOCK ERROR ON MEMLOG FILE
2= FUNLOCK ERROR ON MEMLOG FILE

When a file system error occurs, an error tombstone is displayed, followed by *OUT FILE ERROR* or *LOG FILE ERROR*.

6-22. CE Operating Procedures. The following commands are suggested for CE use to obtain hard copy output of memory errors:

```
:HELLO FIELD.SUPPORT
:FILE OUT;DEV=LP
:RUN MEMLOGAN.PUB.SYS
```

The line printer will then reproduce a copy of the log file.

ADDRESS			ERROR TYPE			ERROR
CONTROLLER	BOARD	ROW	TYPE	BIT	CHIP	COUNT
<CONTROLLER>	<BOARD>	<ROW>	<TYPE>	<BIT>	<CHIP>	<CNT>

WHERE:

<CONTROLLER> = CONTROLLER A OR CONTROLLER B

<BOARD> = 0-7. <BOARD> IS AN INTEGER WHICH CORRESPONDS TO THE MEMORY MODULE ADDRESS

<ROW> = 0-3. <ROW> IS AN INTEGER WHICH CORRESPONDS TO THE ROW DESIGNATION ON THE BOARD IN WHICH THE FAILING CHIP IS LOCATED.

<TYPE> = CHECK. CHECK BIT ERROR OCCURRED;

<BIT> = 0-5. <BIT> REFERS TO THE FAILING CHECK BIT.

<CHIP> = U <N> WITH <N> = CHIP NUMBER

= DATA. DATA BIT ERROR OCCURRED;

<BIT> = 0-15. <BIT> REFERS TO THE FAILING DATA BIT

<CHIP> = U <N> WITH <N> = CHIP NUMBER

<CNT> = AN INTEGER REPRESENTING THE NUMBER OF TIMES THIS ERROR WAS DETECTED AND LOGGED.

147014-75

Figure 6-10. Error Printout Format

SECTION VII

I/O SYSTEM

FUNCTIONAL DESCRIPTION

7-1. I/O SYSTEM OVERVIEW

This section contains an overview of the computer's I/O system which includes discussions on the file sytem operation, I/O elements, channel programs, and the General I/O Channel (GIC).

The primary purpose of any computer is to input, process, and output information. Under MPE, this information may be created and used by the operating system, by compilers or other systems, by user programs, or by the users themselves. To handle all information in a uniform, efficient manner, MPE treats it as groups of data called files. Specifically, a file is a collection of information or data identified by a name recognized by MPE. MPE uses media such as disc, diskettes, and tape for storing the information. On any of these media, a file may contain MPE commands, system or user programs, or data; alone or in any combination. Within a file, all information is organized into units of related data called logical records that for most applications are similar in form, purpose and content. The records in the file can be arranged in almost any order; alphabetically, numerically, chronologically, by subject matter, etc. The logical record is the smallest grouping of data that MPE can address directly; you specify a file when you create the file. Individual subsystems and user programs, however, can also recognize fields for data items within each record. In addition, programs can also recognize and manipulate individual words, eight-bit bytes, and bits within a byte.

Data is transferred to and from files in units called blocks. These are the basic units that are physically transferred between main memory and the peripheral device on which the file resides. On disc and magnetic tape files, a block consists of one or more logial records; for files on other media, a block normally is equivalent to one logical record (unless you request input/output under the multi-record mode). To summarize the interrelation of files, logical records, and blocks: a file is a collection of records treated as a unit and recognized by a name; a logical record is a collection of fields treated as a unit, residing in a file; and a block is a group of one or more logical records transmitted to or from a file by an input/output operation. The purpose of the I/O system, then, is to perform actual physical input/output operations for the file system of the MPE operating system. The user normally does not interact directly with the I/O system; only indirectly through the file system as shown in figure 7-1. Normally, all I/O operations are invisible to the user. However, privileged users may access the I/O system directly.

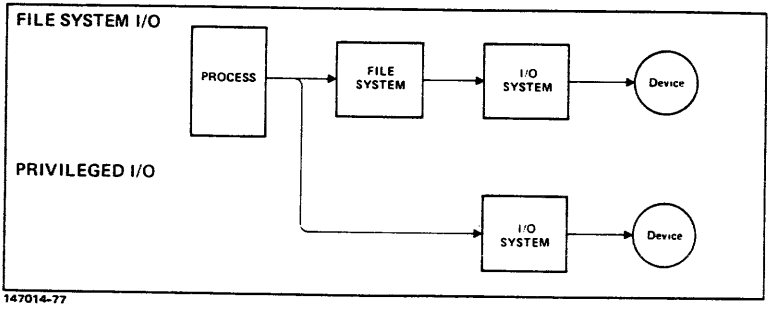


Figure 7-1. Basic I/O Access Methods

7-2. FILE SYSTEM OPERATION

Figure 7-2 illustrates the function of the I/O system in the overall handling of the files. The I/O system is part software and part hardware. Several peripheral devices are shown connected to the I/O system, each of which has some capability for handling files; entering files, storing files, or both. Of particular interest are the files stored on disc. Each disc file is broken up into one or more extents. (Disc extents are composed of a number of blocks.) When the file system causes the I/O system to transfer data to or from the disc, it does so one block at a time. The blocks are further subdivided into records and then into individual words. When the file system processes user file requests, it does so on the basis of records.

The memory management routine is also depicted in figure 7-2 since it frequently makes its own requests to the I/O system. Memory management calls the I/O system in order to bring code and data segments into main memory where they can be accessed by the user processes. In a typical operation a user process might request the file system to read a file using the file request (FREAD) intrinsic. The file system reads the stack associated with the user process. In this example, no input/output has taken place because the named record is already present in a buffer (buffer 0) in Main Memory.

If the requested record is not present, the file system makes a request to the I/O system to read the block containing the particular record. The I/O system reads this block from the disc and loads it into one of the buffers (Buffer 1) allocated to the named file. The file system can now complete the request. During the preceding operations, the user process did not specify a device. An actual I/O operation may or may not have occurred and the user is completely unaware of the occurrence. The operating

system, however, allows devices to be specified either by class name or by a specific logical device number. This would permit inputting or outputting files via a specific terminal or line printer.

7-3. FUNDAMENTAL ELEMENTS OF THE I/O SYSTEM

As shown in figure 7-3, a Device Controller and General I/O Channel comprise the hardware I/O linkage between the CPU and I/O device. It typically consists of one or more logic cards housed either within the main chassis or separately with its associated device (such as the HP 7920 disc drive). Depending on particular controllers, the Device Controller may drive only one peripheral (such as a line printer) or may be capable of driving several peripherals (such as disc units). Figure 7-3 illustrates some of the important elements of the I/O system but is by no means complete; it is intended to show the chain of linkages that are basic to the I/O system. For each Device Controller there is a four-word entry in the Device Reference Table (DRT). Word two in the four-word table entry contains a pointer to a data area uniquely associated with that table entry. The data area consists of an Interrupt Linkage Table (ILT), one or more Device Information Tables (DIT) (depending on how many units the Device Controller is driving), and an I/O program area. Along with various other information, the Driver Linkage Table (DLT) contains Code Segment Table (CST) and Segement Transfer Table (STT) values for defining the location of the driver routines associated with that particular Device Controller. The DIT contains information relevant to one physical I/O device and is configured differently for each type of device. In each case, however, the third word of this table points to an entry in the I/O Queue (IOQ) when a request is being made.

The IOQ is a single table (only one per system) containing a fixed number of entries having a fixed number of words per entry. If there are no I/O requests pending in the system, none of the DIT entries will be pointing to the IOQ. In this case, all entries of the IOQ are unused, and the second word of each entry points to the first word of the next entry. Thus, all unused entries are linked together. If that file system makes a request to use Unit 1 of the Device Controller, the I/O system will unlink the first free entry in the IOQ and fill it with information pertaining to the request (including buffer address and logical device number). Assume that the next request is for Unit 2 (uses the next available entry), followed by a second request for Unit 1. This second request for Unit 1 causes the first word of the initial request to point to the next unused entry, which is then filled with information pertaining to the second request.

Therefore, eventually the IOQ will contain a queue of requests for Unit 1, a separate queue for Unit2, and so on, plus a linked list of free entries.

Next, an I/O driver is executed to initiate the request. An I/O program will then be run on a device, using the request parameters given in the IOQ. When the request is fulfilled, the IOQ entry is returned to the free list. The IOQ only establishes the priority of requests for each device on a first-in, first-out basis. Questions of priority in executing I/O drivers are resolved by the Dispatcher. Once several Device Controllers are running I/O programs, priority conflicts are resolved by hardware service priority.

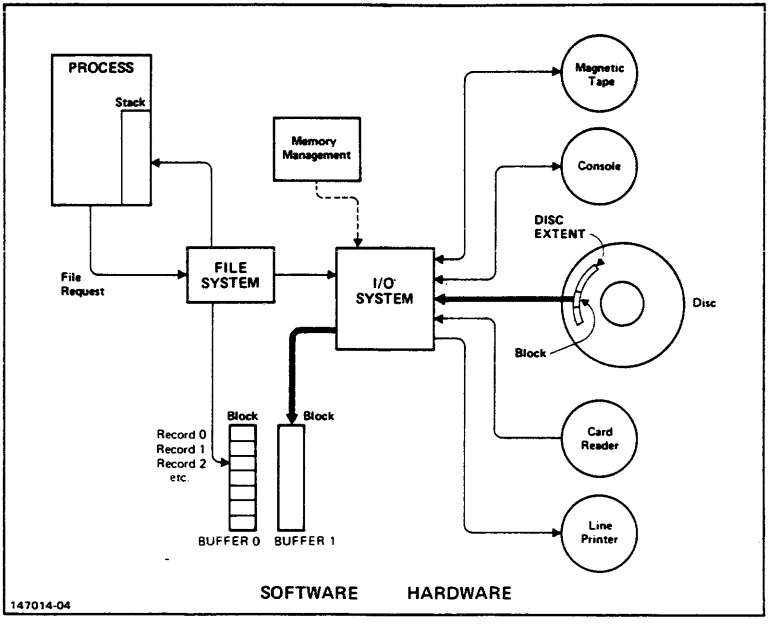


Figure 7-2. File System Basic Operation

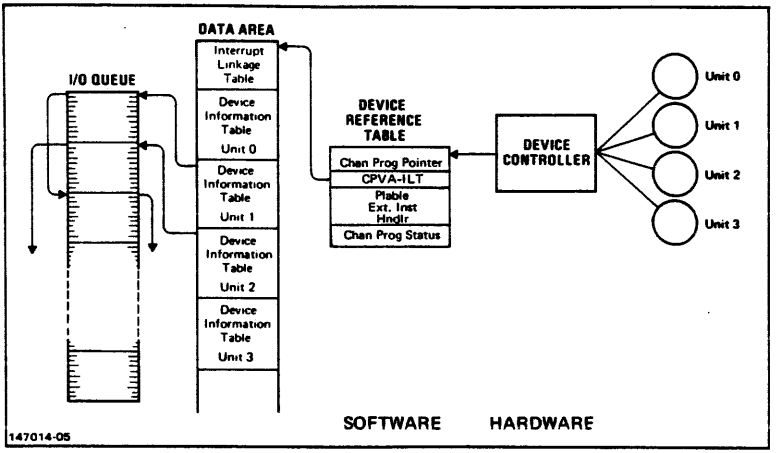


Figure 7-3. I/O System Fundamental Elements

The DRT consists of a number of four-word entries corresponding to the number of Device Controllers present in the system. The DRT is located in fixed memory locations beginning at octal address 40. The upper limit for the table is location 777 which limits the maximum number of four-word enties to 120 (decimal). Because each DRT entry is always four words in length, it is convenient for the hardware to map device numbers to DRT addresses simply by multiplying by four. Thus the entry for device number 10 begins at octal location 40 [i.e., %(10 x 4) = %40]. Because the DRT begins at location %40, device number 10 is the lowest device number.

NOTE

The device number associated with a particular DRT entry defines a Device Controller, and not necessarily an actual physical device. Also, some controllers identified by one device number are capable of driving several physical devices. Individual identification of physical devices is mae by logical device numbers. The logical device number is the value used by the file system in requesting I/O, and the I/O system software performs the logical-to-physical device number translation.

7-4. GENERAL I/O OPERATION

A general overview of the I/O System's operations for I/O transfers is illustrated in figure 7-4. To provide a complete sequence of operations, it is assumed that the file request results in a need for physical I/O to be performed, which may not always be the results. The sequence of operations is as follows:

a. An executing user process generates a file request to the file system.

b. The file system then tests the validity of the request and calls the Attach I/O (ATTACHIO) intrinsic. This is the entry point to the I/O system.

c. The Attach I/O intrinsic inserts the request parameters into the IOQ for the requested device.

d. When all prior requests for a particular device have been completed, the I/O monitor process begins execution of the request.

e. The I/O monitor verifies that the data buffer for the file is available and present in memory. Then, it issues a procedure call (PCAL) to the initiator section of the device software driver which processes the IOQ pointed to by the DIT.

f. The channel program is assembled by the initiator section (using the information in IOQ) of the device driver, and then issues a Start I/O Program (SIOP) instruction to the General I/O Channel (GIC) and exits back to the I/O monitor. The SIOP instruction initializes the DRT to point to the starting location of the channel program.

g. The channel program issues commands to the GIC, which enables the device controller.

h. When the device controller receives a read or write command from the channel program, it transfers a block of data to or from the data buffer. The length of the block is specified by the I/O command.

i. Upon completion of the data transfers, the channel program causes an interrupt to be generated. The channel program then ends.

j. The interrupt routine checks for an error and calls the driver again if there was. If no error occurred, it calls the monitor.

k. When the I/O monitor program is executed again, it recognizes that an interrupt has occurred and calls the completion section of the device software driver.

l. The completion section updates the I/O queue with information regarding results of the original request. The file system may then check results.

m. When the user process is dispatched again, a return is made to a point following the file request, depending on whether blocked or unblocked I/O was specified.

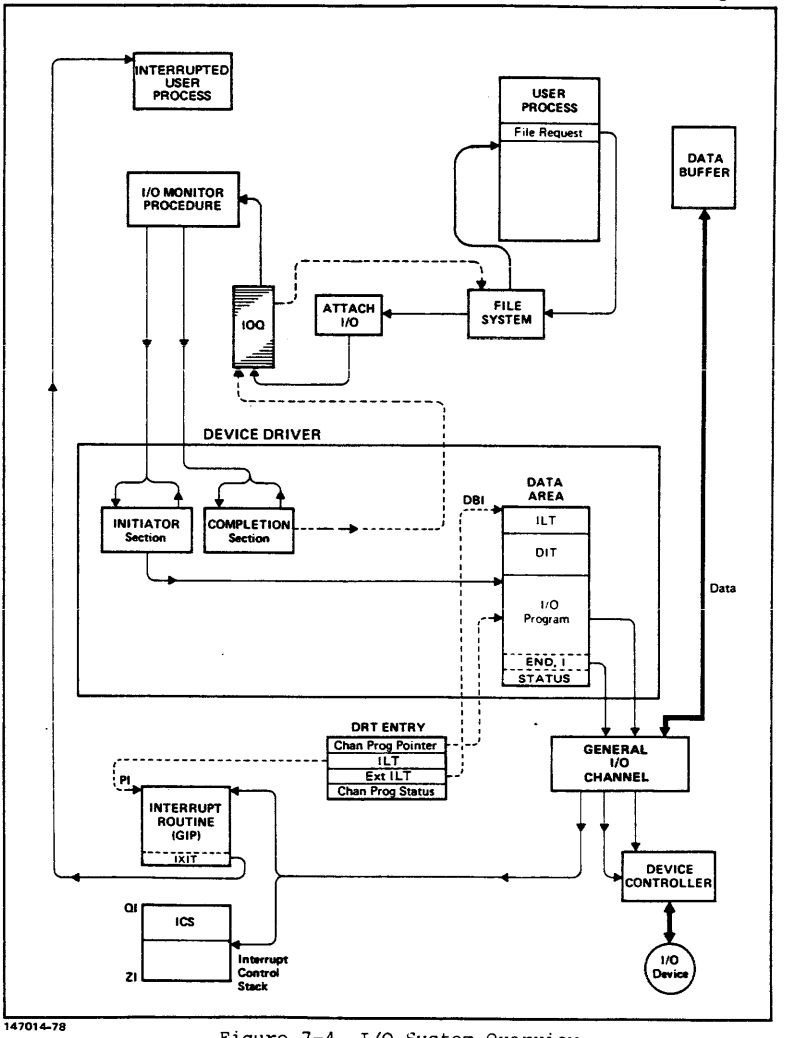


Figure 7-4. I/O System Overview

7-5. I/O RELATED MEMORY STRUCTURE

Each device has a four word Device Reference Table (DRT) entry in memory. A DRT entry contains information for interrupt and channel program processing.

7-6. Word 0 of the DRT Entry

This is the 16 bit absolute memory address of the next channel program instruction to be executed. Since this is only a 16 bit address, all channel programs must reside in the lowest 64KB of main memory. This address is loaded by the channel microcode. When the program halts, the address will be pointing to the next instruction to be executed when the program is started again.

7-7. Word 1 of the DRT Entry

This is the 16 bit absolute address of the start of Channel Program Variable Area (CPVA) and Interrupt Handler data area. All CPVA's must reside in the lowest 64KB of main memory. The organization of the area beginning at this address is:

Words 0-3: These words will contain information describing reasons for external interrupts for this device.

Word 4: The number of serial poll devices. This can be non-zero only in the CPVA of device 0 of the channel, and its value is the length of the serial poll table, which follows in the next consecutive words.

7-8. Word 2 of the DRT Entry

This the label for the software external interrupt driver for the device.

7-9. Word 3 of the DRT Entry

After the device's channel program is started, this word should interpreter to store status relevant to channel program execution.

7-10. SOFTWARE I/O

Even though I/O tasks are normally handled with channel programs, software is still responsible for managing the I/O activity. A limited number of software I/O instructions are provided for this purpose and to allow software to control interrupts, and start or

halt channel programs, determine which channel addresses are occupied, and initialize or reset the I/O hardware. In addition, there may be unusual circumstances which require direct communications between software and a channel or device.

Some of the I/O instructions are global in nature, since they affect and interact with all I/O channels simultaneously. Other instructions are addressed to a specific channel. There are no software I/O instructions which are intended exclusively for direct transactions with a device.

7-11. I/O INSTRUCTION SET

The I/O instructions provide the following capabilities:

a. Control of all channel registers, including HP-IB functions.

b. Start/Halt control of channel programs.

c. Identification of channels on the IMB.

d. Control of the I/O interrupt system.

e. Initialization and reset of I/O channels.

There are two categories of instructions in the set, global and addressed. Global instructions involve data transfers to all channels simultaneously whereas addressed instructions involve data transfers between the CPU and a single addressed I/O channel.

7-12. ADDRESSED I/O INSRUCTIONS

These instructions involve data transfers between the CPU and a single selected I/O channel, and provides software with full control of channels and devices. The CPU condition codes will be set as follows (Condition Codes are physically a part of the CPU status register):

CCL: Data-Not-Valid line set by the channel during operation (reference to empty or illegal registers).

CCE: Instruction completed successfully.

CCG: Some channel programs for the channel are active, operation not done.

7-13. Initialize Channel (INIT)

This instruction prepares a channel for use by initializing the channel hardware and memory locations dedicated to that channel. Basically the instruction:

a. Issues the IMB Initialize Channel command to the selected channel, which terminates all channel operations and presets all registers. A GIC is forced offline from the HP-IB.

b. Clears the bit in memory location 7 associated with the selected channel.

c. Clears the fourth word of each DRT entry for the channel, so no trace of previous channel program activity remains.

d. Writes 0010 to channel register 6, waits 100 microseconds then writes 0000 to register 6, to generate an Interface Clear (IFC) message to the HP-IB to insure that the HP-IB is cleared and that the GIC is Controller-In=Charge of the HP-IB (The System Controller switch S3 on the GIC must be set to the in position).

e. Writes 0010 to channel register 7 to connect the channel to its I/O bus (puts the GIC online on the HP-IB).

f. Writes FFFF to register 2 to clear any interrupt conditions created in the process of getting online.

7-14. Start I/O Program (SIOP)

The TOS contains the 16 bit address of the first channel instruction of the channel program. TOS-1 contains the channel and device numbers. This instruction does the following:

a. Loads the TOS into DRT entry word 0 for the selected device.

b. Set bits 0,1 of DRT entry word 3 to 1,1.

c. Sets a bit on the channel to cause the channel to begin requesting channel program service for the device.

d. Pops two words from the stack.

NOTE: This instruction does not begin execution of the channel program immediately, but merely causes the channel to start requesting service. If the channel program for the device is not inactive, then the instruction is not executed, and the CPU indicators are set to CCG.

7-15. Halt I/O Program (HIOP)

The TOS stack contains a channel and device number. This instruction does the following:

a. Sets bits 0,1 of word 3 of the DRT entry for the selected device to 0,1.

b. Sets a bit on the channel (via the Halt I/O Program IMB command) to cause the channel to request a channel program halt on behalf of the selected device. When the program has been completely halted, bits 0 and 1 of DRT entry word 3 will be set to 0,0.

c. Pops the stack.

With its channel program halted, a device may not request any new system interrupts, but any interrupts pending at the time the program halts will be serviced.

NOTE: The program might not halt immediately, as there are places in the channel program where it is not advisable (during DMA transfers, for example). In general, a halt will not complete until a Wait instruction is encountered, or the program halts itself.

7-16. Read I/O Channel (RIOC)

This instruction performs one IMB read command, which is specified completely in the TOS. Either global or addressed commands may be done. The programer specifies the channel number, device number, I/O command, and register number. The data returned by the operation is saved on the TOS after the command specification are popped.

The primary purpose of this instruction is to allow software to read registers on the I/O channels. The ability to perform any single IMB command is intended to be a diagnostic tool.

7-17. Write I/O Channel (WIOC)

This instruction performs one IMB write command, which is completely specified in the top of stack. Either global or addressed commands may be done. The programmer specifies the channel and device numbers, I/O command, and register number (for the Write Data command), and the data to be sent. The entire specification is popped on successful completion of the command.

The primary purpose of this instruction is to allow software to write to channel registers. The ability to perform any single IMB command is intended to be a diagnostic tool.

7-18. CHANNEL PROGRAM CHARACTERISTICS

Each channel on the IMB may support up to eight devices (numbered 0 through 7), and each of these devices will have a unique dedicated channel program controlling its I/O operations. These programs reside in the system's virtual memory, but consist of specialized channel instructions which are completely unrelated to the machine instructions of the main CPU. All eight programs for a given channel may be simultaneously "running", even though actual execution at any time is dedicated to only one of those programs. When service to an HP-IB device is suspended, execution transfers to another program based on device demand and priority. This priority is established during a parallel poll response from a device which is requesting service, at that time, execution will begin (resume) on the lowest numbered device requesting service. Thus, device 0 has the highest priority on any channel.

7-19. CHANNEL PROGRAM INTERPRETATION

Interaction of the main CPU software with a device running under channel program control is limited to alteration of the program and starting/halting the program execution through the SIOP and HIOP machine instructions. That is, the main software does not interpret or execute the channel instructions, and the consequences of a channel program must generally be brought to the attention of software by an interrupt from the channel program.

7-20. CHANNEL PROGRAM MANAGEMENT

Each of the eight programs on a channel has a four-word Device Reference Table (DRT) entry in main memory. This table entry is initialized by the main software prior to starting the desired channel program. Since several programs may exist for a device, software is responsible for setting the DRT entries and selecting a program for the I/O task at hand.

Channel program execution is enabled with the SIOP machine instruction. When the channel program interpreter (CPU microcode) detects the request to start, it will set bits 0, 1 of word 3 of the DRT entry to 1,0 and begins program execution. The program then runs until halted by the program itself, by an abort condition or by an HIOP machine instruction. The HIOP instruction sets bits 0, 1 of word 3 to 0,1 and sets a bit in the channel to cause the device to request service for the change in program status. The CPU will service the request by terminating the

channel program for the device and clearing bits 0,1 in word 3. An HIOP does not halt the program immediately, but sets a request to halt the program. The channel program will complete the current instruction and possibly execute a few more, but it is guaranteed to halt by the next WAIT instruction. There could also be a delay if the program which is issued HIOP is of lower priority than other devices requesting service on the channel. Software cannot assume a program is no longer being serviced until bits 0, 1 in DRT entry word 3 are both 0. If a program halts or aborts itself, then it will clear the DRT bits immediately. Thus, bit 0 of word 3 gives the requested running status, where as bit 1 indicates that a change is running status is pending.

Word 0 of the DRT entry is the channel program pointer and indicates the address in main memory of the next channel instruction to be executed. The pointer is updated by the program interpreter at certain times during channel program execution. Software should attempt to alter the pointer only after the program has actually been halted as indicated by the DRT bits mentioned above. Otherwise, if an instruction is in execution when software alters the pointer, the program interpreter would destroy the new information upon completion of the execution. This restriction does not preclude the alteration of instructions within a running channel program, although this technique should be used with caution.

7-21. CHANNEL INSTRUCTION SET

The HP-3000/44 channel instructions fall into three categories: Channel Functional, Interactive, and Non-Interactive. The Channel Functional group permits the program to exercise the most basic functions of the I/O channel and the HP-IB. All data transfers and control functions may be effected with these instructions, providing the programmer has some knowledge of the HP-IB protocol and the channel hardware. HP-IB interface commands may be sent with the Command HP-IB instruction, and data transfers may be controlled with Execute DMA.

The Non-Interactive instructions enhance the utility of the channel program concept by providing linkage between various segments of the program and allowing orderly communication with software. These instructions produce no interaction with the device and thus may be used with any device irrespective of its protocol.

The Interactive instructions may be viewed as macroinstructions for use with devices that obey the HP-3000/44 protocol. That is, transactions that may be accomplished with several instructions from the Channel Functional group are combined into a fixed sequence under a single Interactive instruction. These sequences assume that the device recognizes not only an HP-IB primary ad-

dress, but also a secondary address which contains a directive or command modifier.

All Interactive instructions send a secondary address message to the device immediately following the address to talk or listen. These secondary addresses direct the device to interpret the subsequent data in a particular manner. The HP-IB standard defines the secondary address format as X11SSSSS where X is a don't care bit and SSSSS refers to the application-dependent bits of the message. HP-3000/44 protocol uses the left-most S bit to distinguish the operation as either Data or Control. In this context, a control operation is one which indicates or affects the status of the device or its channel program.

0110SSSS = Data Secondary
0111SSSS = Control Secondary

The various channel instructions which fall into the Control category all have their values of SSSS predefined. Two of the control secondaries may be identical, but the operations are nonetheless distinguishable since the device will be addressed to talk in one case and addressed to listen in the other. The Read and Write instructions produce Data operations, and the programmer is free to specify the remaining four bits of the secondary.

CHANNEL INSTRUCTION SET CATEGORIES

INSTRUCTION	TYPE
Relative Jump	Non-Interactive
Interrupt	"
Wait	"
Read	Interactive
Write	"
Device Specified Jump	"
Identify	"
Read Control	"
Write Control	"
Clear	"
Read Modify Write	Channel Functional
Read Register	"
Write Register	"
Command HP-IB	"
Execute DMA	"
Write Relative Immediate	"
CRC initialize	"
CRC Compare	"

CHANNEL PROGRAM INSTRUCTIONS

Hex Code	Instruction	No. of Words	Comments
0000	Relative Jump	2	
01XX	Interrupt	2	018X-with halt 010X-with run
020X	Wait	2	
03XX	Read	5	If data chained, 00X0, where X= Blocks left
04X0	Write	5	
05XX	DSJ	2+XX	
0600	Identify	2	
07XX	Read Control	5	
08XX	Write Control	5	
09XX	Clear	2	
0A0X	Read Modify Write	2	
0B0X	Read Register	2	
0C0X	Write Register	2	
0D0X	Command HP-IB	5	
0E00	Execute DMA	5	
0FXX	Write Relative Immediate	2	
10XX	CRC Initialize	2	
11XX	CRC Compare	2	

7-22. I/O REQUESTS AND INTERRUPTS

The HP-3000/44 I/O interrupt system provides a hierarchical framework for devices and channels to request machine program interrupts and channel program service. This section defines device/channel interaction only for the HP-IB oriented channels (e.g., the GIC) although other types of interface protocols will be permitted between channel and device. All channels must follow the same IMB protocol for requesting service.

HP 3000 applicable devices make service requests to the channel by the parallel poll interface function. The channel determines when a device receives service or if some condition on the channel requires service, sorts out reasons and priorities for requesting, and requests service on the IMB on behalf of itself or its devices. I/O requests for external interrupts are made to the CPU via the IRQ line, and channel program service requests are made to the CPU over the CSRQ line. The CPU obtains information from the highest priority requesting channel, then executes an appropiate service algorithm.

7-23. Request Facilities

		Priority
SRQ	Device Request for Service Shared line Serial Poll Required	Low
Parallel Poll	Device Request for Service Poll Done When Channel Not Busy Parallel Requests	
CSRQ	Channel Request For CPU Service Transparent To Software, Non-Maskable	
IRQ	Channel Request For Interrupt New Environment For Software Maskable At Channel Or System Level	High

7-24. SRQ. SRQ is a unique line on the HP-IB. Devices should not use this facility on an HP-3000/44 system, since it is much slower than parallel poll.

The channel will assert CSRQ on behalf of an SRQ assertion only if there is no other reason for the channel to assert CSRQ, and a Parallel Poll is being conducted. SRQ is the lowest priority reason for requesting service.

In order to determine which device was asserting SRQ, a serial poll must be conducted on the HP-IB. This done by the CPU during servicing of a CSRQ caused by an SRQ. The number of serial poll devices on a channel is in word 4 of that CPVA, and the HP-IB device addresses to be polled are found one per word in the next several words. The byte returned by the device is examined to determine if the device requires service. The poll is continued through the table until either the SRQ line goes false, the table is exhausted, or a device is found whose channel program needs service.

7-25. Parallel Poll. When no other operations are being performed on HP-IB, the channel puts the bus into the parallel poll state (asserting ATN and EOI simultaneously). All devices must assert a logical one for an affirmative response. Although the HP-IB protocol allows any device to be assigned to any DIO line for polling, the DIO poll assignment determines which device will be serviced. A device asserting PPR8 (requesting on DIO8) has the highest priority and is considered to have device number 0. When the GIC detects an affirmative poll response and no actions of higher priority are occurring on the GIC, CSRQ will be asserted.

7-26. CSRQ. CSRQ is an OR-tieable line on the IMB which channels assert to request channel service program service for their devices. A channel may be assigned by a switch on the PCA to one of these lines.

Priorities may vary from channel to channel between reasons for asserting CSRQ, but for the GIC, the following conditions will cause the channel to assert CSRQ:

a. Termination of a DMA transfer
b. An interrupt condition in the HP-IB interface logic
c. A request to start or halt a device's channel program
d. An affirmative parallel poll response on the HP-IB

Software cannot prevent CSRQ from being recognized and serviced by the CPU, although some control is provided for selecting the reason a channel may assert CSRQ. Conditions a, b, and c are not requests from devices, but are generated by the GIC on behalf of a device.

CSRQ generates a macrointerrupt in the CPU. This class of interrupt causes a microcode trap when an attempt is made to do an instruction fetch. It is disabled during a power fail interrupt. CSRQ will interrupt normal machine operation independent of the state of the external interrupt system (IRQ).

CSRQ may not be the only reason the CPU was interrupted. Some testing is done to determine if CSRQ is the highest priority interrupt at the time (there are also IRQ, parity errors, and power fail interrupts). If a channel program for a device is halted when a request occurs for it, then the channel will look for the request from other devices. Servicing of CSRQ is transparent to the software environment.

7-27. IRQ. IRQ is an OR-tieable line on the IMB, which is connected to the CPU and all I/O channels. It is asserted to generate a CPU external interrupt requests. Each channel has an interrupt register which contains one bit per device, and an interrupt mask bit, which is set and cleared by the SMSK machine instruction. If any bit is set in the interrupt register and the interrupt mask bit is set, then the channel will assert IRQ. When a bit is to be set in the interrupt register, information relating to the reason for the interrupt should be stored into the first four words of the CPVA for the device. The interrupt register bits may be set for the following reasons:

a. Occurrence of a memory error during a DMA transfer on the channel.

b. Execution of an Interrupt channel program instruction.

c. Direct setting of bits in the interrupt register by software or channel programs.

d. Anytime the channel program for the device is aborted.

The interrupt register on the GIC is set only by the CPU. Devices and channels conditions requiring service will first have the channel assert CSRQ on their behalf. The CSRQ microcode service routines will decide whether a software interrupt is required, and will store information into the CPVA and set interrupts bits on the channel. The GIC cannot decide itself when to assert IRQ. Clearing of the interrupt mask bit will prevent the channel from asserting IRQ, even if bits are set in the interrupt register.

For IRQ to interrupt the CPU status bit number one must be set (by the ION instruction). Then IRQ will cause the CPU microcode to enter an interrupt service routine when the current machine instruction is complete.

The IRQ service routine in microcode does the following:

a. Polls each channel on the IMB to get a poll of all channels asserting IRQ.

b. Issues an OBII command to the lowest channel number responding affirmatively to IPOLL, which tells the CPU the lowest device number on that channel whose interrupt bit is set (the channel priority-encodes device requests, the CPU priority encodes channel requests).

c. Clears the interrupt bit on the channel for the device which obtains service.

d. Creates a normal four-word stack marker and establishes the interrupt environment.

e. Disables further external interrupts.

f. The third word of the device's DRT entry is used as a label to branch software to the interrupt handler for that device.

It is software's responsibility to prevent lower priority channels from interrupting higher priority channels by using the SMSK instruction to mask off IRQ from higher numbered channels than the one being serviced.

7-28. PRIORITY

Within the I/O system, there are request structures with priorities established between board position, channel numbers, device numbers and reason for service.

7-29. IMB Request Priority

Each I/O board which can act as master of the bus must request bus access on a priority basis. The highest priority channel has slot priority next to the CPU, with lower priority at each position further from the CPU. The CPU has lowest priority, and is responsible for controlling IMB access. Different I/O boards may request control of the IMB for different reasons and one may retain control by continuing to request after having been granted access.

7-30. Channel Priority

Any combination of channels may be asserting IRQ, or CSRQ at one time. When the channels are polled, the lowest channel number has the highest request priority on each request line.

7-31. Device Priority

Within the highest priority requesting channel device priorities are:

IRQ: If several device interrupt bits are set the lowest numbered device will be serviced first.

CSRQ-parallel poll: If CSRQ is due to an affirmative poll response or a change in channel program status, then the device on the highest DIO line (lowest device number) has the highest priority.

7-32. GENERAL I/O CHANNEL INTRODUCTION

The following paragraphs provides a block diagram description of the General I/O Channel (GIC). The system block diagram illustrates the major function of the GIC. Physical characteristics and system configuration are also included.

7-33. GIC BLOCK DIAGRAM OVERVIEW

The General I/O Channel (GIC) is the primary channel for communication between the CPU and I/O devices. Each GIC may have up to eight devices. All data that passes to and from devices (except terminals) is handled by the GIC in one of two methods.

The first method is used when the CPU interrogates or requests service from a channel or a device on that channel. In this mode, the GIC acts as a slave and cannot gain access to the IMB until the CPU tells the channel to respond and allows access to the IMB. Operations in this category include 1) the CPU directs a channel to request service, 2) the CPU requests status, and 3) the CPU addresses a channel/device to talk or listen.

The second mode is used for high speed transfer of data between memory and a device. For this mode, the GIC has a direct memory access (DMA) capability which allows direct memory reading and writing. After initial addressing of a device to talk or listen, the CPU relinquishes control of the IMB and allows the GIC to perform its function through DMA operation. During this time the GIC becomes the master of the bus and memory and controls traffic flow. Upon completion of a DMA transfer, the GIC returns to a slave conditon and awaits the next operation. In other words, all commands decoded from the current channel program instruction, including HP-IB commands, are sent to the GIC from the CPU and all data to be transfered over one byte is read from or written to memory directly by the GIC using its DMA hardware.

Since more than one channel is connected to the common IMB, and more than one device may be on a channel, a priority structure is used to maintain orderly communications.
The GIC contains the circuitry to accomplish its prescribed tasks. Part of the logic is used for DMA, including some of the channel registers. Another section is set aside for conditioning the HP-IB and providing for data transfer, and finally, logic is included for operation in either slave or master modes. (See figure 7-5.)

In either the slave or master mode, the GIC must condition the I/O devices and correctly select a device for operation, and then proceed with data transfers. The HP-IB logic contains most of the circuitry required for this purpose.

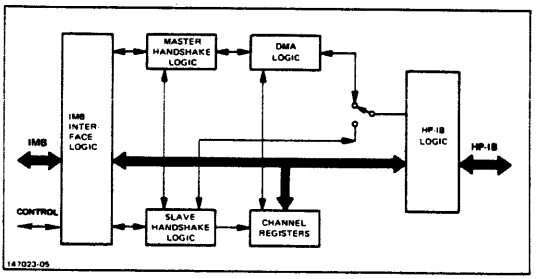


Figure 7-5. General I/O Channel, Simplified Block Diagram

Refer to the system block diagram for the subsequent discussions of each function contained on the GIC.

7-34. Command Decoding and Execution Logic (CDEL)

When initiated by the Slave, this logic controls the sequencing of IMB command execution on the GIC. It must perform several types of sequences for reading and writing the registers and responding to the global IMB commands.

When the OBSI IMB command is issued to obtain channel service information, the CDEL decides from examination of the CSRQ logic whether there might be a Parallel Poll response on the HP-IB. If so, then the Parallel Poll result is read from the Processor-to-HP-IB Interface (PHI), encoded and checked by the CDEL and CSRQ logic before completing the OBSI. If not, then the CDEL accesses other information for the returned data.

For reads, CDEL enables the Global Response Logic, which decides whether the channel should assert true in response. If so, it pulls low on the IMB data line corresponding to the channel number in the Channel Select Switch. For writes, CDEL generates a write pulse.

7-35. Data-Not-Valid Logic (DNV)

This logic is designed to prevent invalid data reads if the inbound FIFO buffer in the PHI is empty when an access of it is attempted. It operates with the Command Decoding and Execution logic. It requires that bit 14 of register 6 be zero except during DMA transfers. Then if a read of register 0 is attempted and the GIC is not performing a parallel poll and the inbound FIFO is empty, the command will be performed by:

a. Preventing any handshake with the PHI,

b. Immediately flagging the slave handshake to complete, and

c. Asserting the DNV IMB line during the Slave handshake.

This sequence also occurs if DMA is active and the PHI registers are referenced.

7-36. Master Handshake

This logic executes data transfers between buffers on the GIC and main memory at the request of the DMA logic. When the DMA logic requests a memory read or write cycle, the Master Handshake logic requests control of the IMB, then performs the required IMB mem-

ory handshake. When it completes, the Master notifies DMA by asserting a single completion bit, which is cleared only after DMA removes its request lines. The memory address accessed is contained in the DMA Address and DMA Extended Address registers. The data from a memory read is stored in the Left Byte Out and Right Byte Out registers. Data for a memory write is obtained from the Left Byte In and Right Byte In registers. The Master Handshake coordinates with the Slave Handshake to avoid conflicts, and assures selection of the proper registers and data set-up times during the memory access.

The Master Handshake logic also detects errors which occur during the memory cycle. If a parity error occurs during a memory cycle performed by the GIC, a status bit is set in register B and DMA is aborted. If any memory handshake takes over about 20 microseconds once started, then another status bit is set and DMA and the memory cycle are aborted. If the DMA Address register rolls over (--FFFF to --0000) then no more memory accesses can begin, another status bit is set, and DMA aborts.

7-37. Slave Handshake

The Slave handshake logic performs detection and handshaking of IMB commands which are addressed to the GIC. It is a three-wire class IMB I/O slave. It will signal the Command Decoding and Execution Logic to start when it detects a command addressed to it, at which time it compares the channel number specified on the address lines of the IMB with the channel number set by the switch on the GIC. Global IMB commands do not require a channel number, so if one is present, the Slave will trigger the Command Decoding and Execution Logic, but will not participate in an IMB handshake.

The Slave also latches the IMB address lines at the start of a handshake. When the command has been executed, the execution logic signals the Slave to complete the IMB handshake. The Slave is also coordinated with the Master Handshake to prevent conflicts between the two, since they are asynchronous. If the IMB handshake should terminate during Slave operation, the Slave will return to a passive state and will become ready for the next IMB command.

7-38. Processor-to-HP-IB Interface

The processor-to-HP-IB interface (PHI) chip provides a high-speed interface between the HP-IB and the GIC. The PHI chip appears to the GIC as a bank of eight addressable registers. All interaction with the HP-IB is performed by reading and writing these registers. The capabilities provided by these registers allow the computer to connect to the HP-IB as a device responding to inter-

face commands from remote devices, or as the controller of the HP-IB. In addition, the PHI chip provides buffering for inbound and outbound data through two FIFOs which are accessed by the computer.

The pins provided by the PHI chip for interfacing include:

- A 10-bit wide data bus
- Three register-select lines for selecting among the eight registers
- A data direction line to specify either reading or writing to the selected register
- Two handshake lines to coordinate data transfer
- An interrrupt line to alert the computer, through the GIC, of selected events
- A DMA request line for use with the DMA machine

7-39. Direct Memory Access (DMA) State Machine

General Description.

This is a 27-state synchronous Algorithmic State Machine which is part of a facility to manage data transfers, with byte packing and unpacking, between the HP-IB and memory on the IMB, after the transfer has been initiated by a sequence of IMB commands to the GIC.

Basic Operation

a. Idle State: In this mode, DMA allows direct access to the PHI and affects nothing on the GIC. It is waiting to be activated.

b. DMA Active: DMA is activated when it is idle and a write is done to register B. At that time, DMA blocks all access to the PHI by the slave, selects register 0 of the GIC (PHI data buffers), and has exclusive use of the PHI until it goes inactive again. Slave Handshakes to the PHI will activate the Data-Not-Valid logic. Other channel registers are still accessible, however. As long as DMA is active, Channel Service Requests cannot be generated until DMA generates it at its termination. However, Interrupt requesting and servicing may proceed.

c. DMA Control Registers: Registers 8,9,A,B, and E are associated with DMA. They specify the memory address of the data buffer, the number of bytes to be transferred, and DMA control options. Any write to register E will abort DMA.

d. First/Last Byte: Transfers may begin and end on the left or right byte of a word, but DMA does only full-word operations with memory. To insure that the unaddressed byte in a word containing the first or last byte of an input transfer is not lost, DMA reads that whole word and preserves the unaddressed byte in the Byte In buffers before writing back into that memory address.

e. Input Transfer: The DMA machine waits for the PHI to indicate that it has a byte available in its inbound first-in,first-out (FIFO). If the byte is for the left byte of a memory word, the byte is handshaked from the PHI and is latched in the Left Byte In register. If the byte is for the right byte of a memory word, the byte is handshaked from the PHI and a memory write is requested. The PHI data is passed through the Right Byte In register and both Byte In registers are switched out together as data for the memory write. At the end of the memory cycle, the memory address is incremented and DMA waits for the next PHI request. The remaining byte count is decremented before each byte is received.

f. Output Transfer: The DMA machine requests a memory read cycle, which puts data into the Byte Out registers. Then DMA waits for the PHI to indicate there is room available in its outbound data FIFO. Then the Left Byte Out register is handshaked to the PHI. Then DMA waits for the PHI to indicate more room available in its outbound FIFO, when the Right Byte Out register is handshaked to the PHI and the memory address is incremented and the next memory read is started. The byte count register is decremented before each byte is sent. The last byte out may be tagged with the HP-IB "END" message, or not, depending on an option bit in register B.

g. Termination: A DMA transfer may terminate for several normal or abnormal reasons. It will terminate only after completion of the current byte transaction. However, the byte count and address registers might be incorrect by one byte if an abort occurs before the last byte is transferred. On input, since byte packing is done on the GIC, an abort could cause not writing the left and right bytes to memory.

h. Service Request: When the DMA transfer terminates, a CSRQ is generated for the device number loaded into register B when DMA was started. DMA will continue to assert CSRQ until after the end of the next OBSI command to the GIC, since that is the first indication DMA has that its CSRQ has been recognized. DMA will continue to prevent access to the PHI until

it reaches its idle state. After an output transfer, DMA cannot generate CSRQ until the PHI Interrupt line is asserted, so the PHI must be set up before the transfer to assert INTERRUPT on outbound FIFO empty.

7-40. Left and Right Byte Out Registers (LBOR, RBOR)

These are tri-state single byte registers. They are loaded from the buffered IMB data lines. The Left Byte Out register is loaded from bits 0-7 of the data, and the Right Out register is loaded from bits 8-15 of the data. During Slave writes, the RBOR is enabled onto the PHI data lines 8-15 and bits 0,1 of PHI data are taken from bits 0,1 of the buffered IMB data. LBOR is not used by the Slave. LBOR and RBOR are both loaded during a Master memory read. Then the DMA machine switches one or the other onto the PHI data lines during output sequences. DMA controls bits 0,1 separately.

7-41. Left and Right Byte in Registers (LBIR, RBIR)

These are single byte registers. Each is loaded from the PHI data lines. LBIR is a edge-clocked register and is used only by DMA for byte packing. Its data is switched onto IMB data bits 0-7 during Master writes to memory. The RBIR is a latched register. During most slave and DMA operations, data passes directly through it. It is used to latch data only during an OBSI when parallel poll response is being checked or during DMA input termination when the right byte of the last memory address must be saved before rewriting with the left byte obtained from the PHI. During Slave reads, PHI data bits 0,1 drive IMB data bits 0,1 and bits 2-7 are forced to 0, while the RBIR drives bits 8-15 for both Slave and Master operations. During DMA inputs, PHI bits 0,1 are examined by DMA but are not written to memory.

7-42. CSRQ Logic

This logic is responsible for generating Channel Service Requests and selecting what information is to be returned when the next OBSI IMB command occurs. Inputs to this logic are:

a. DMA activity.

b. PHI INTERRUPT, CONTROLLER-IN-CHARGE, DMA REQUEST lines.

c. Contents of the New Status Register (NSR).

d. HP-IB lines ATN, EOI, SRQ as seen by the PHI.

e. Flags to indicate occurrence of OBSI.

f. Bits 8, 13-15 in register B. Bits 13-15 contain the device number last written to these bits, and are jointly referred to as "DMDEV" in the flowchart.

The New Status register has one bit for every device number (0-7), which is set whenever a channel program for the respective device is issued SIOP or HIOP. The PHI Interrupt line is latched during OBSI, and parallel poll responses are latched after they are obtained from the PHI to prevent logic races in the circuitry.

7-43. Interrupt Request Logic

The Interrupt register is an addressible channel register (C) which has one bit per device which is set to queue an interrupt request for that device. When the Interrupt Mask Bit is set by an SMSK command, then if any bit is set in the Interrupt register, the IMB IRQ line is asserted to request a CPU external interrupt. The output of the Interrupt restister is priority encoded and the device number is sent back as data of the OBII IMB command. When the mask bit is cleared by SMSK, no IRQ can be asserted. When an interrupt request for a device has been recognized, its bit in the Interrupt register will be cleared by another write to register C. Device 0 has highest interrupt priority.

NOTE

Devices cannot cause IRQ; channel program processors and diagnostic software are the only means intended to be allowed to set an interrupt request for a device. Devices directly generate CSRQ only.

7-44. Timeout Logic

This logic is provided to insure against channel lock-ups waiting for conditions which will never occur. The timeout logic consists of a 15 Hz clock and a counter. When the channel is waiting for a specified condition, the counter decrements. If the counter reaches 0 before being reset to 15 by occurrence of the required condition, then a timeout flag is set which will force a CSRQ and set a bit in the GIC's OBSI response. Thus, the timeout interval is about one second.

7-45. GIC Registers

Sixteen registers in the GIC are used for initiating and controlling data transfers between memory and devices on the HP-IB. Also, status conditions are indicated and acted upon according type and priority. Some of the registers are used in conjunction with the PHI chip and the HP-IB, and the others are used for DMA operation. Eight registers are contained in the PHI chip while the remaining eight are located on the GIC board. Table 7-1 lists the registers and the following paragraphs provide a brief description of each register.

Table 7-1. GIC Registers

Register Number	Function
0	HP-IB FIFOs (Data Buffers)
1	HP-IB Status (Monitors Interface Operation)
2	HP-IB Interrupt Register
3	HP-IB Interrupt Mask
4	HP-IB Parallel Poll Mask
5	HP-IB Parallel Poll Normalize
6	HP-IB Control
7	HP-IB Address
8	DMA Extended Address
9	DMA Address
A	DMA Byte Count
B	DMA Control/DMA Status
C	Interrupts
D	Interrupt Information
E	Channel Configuration/DMA Abort
F	Channel Service Information

Table 7-2. GIC Register Formats

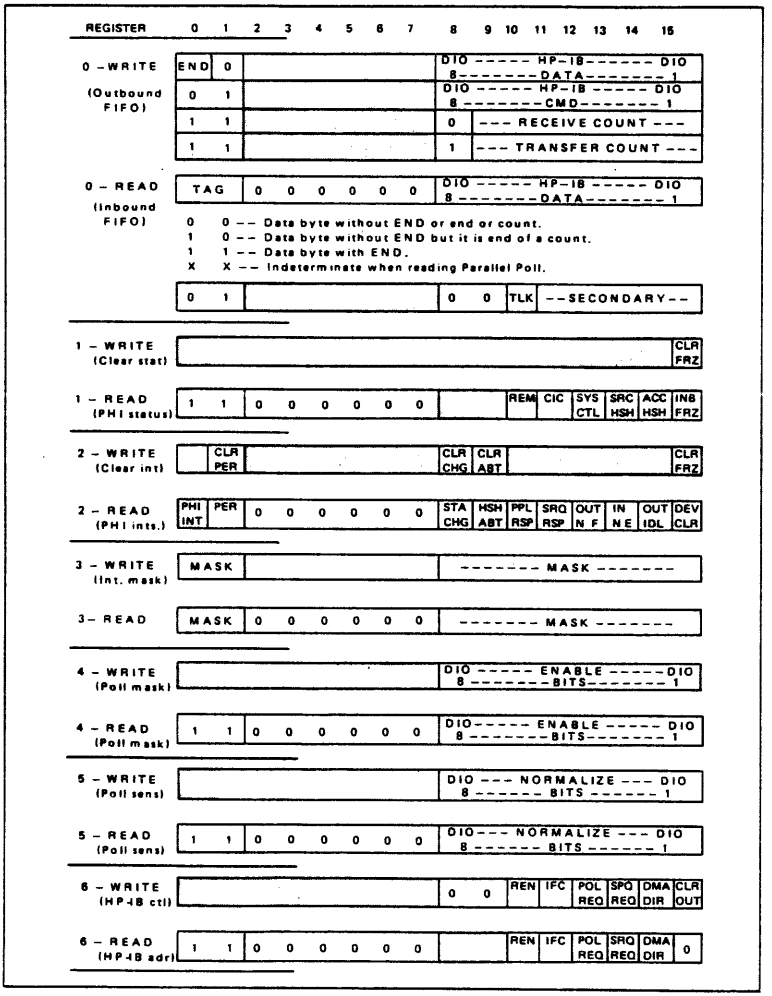
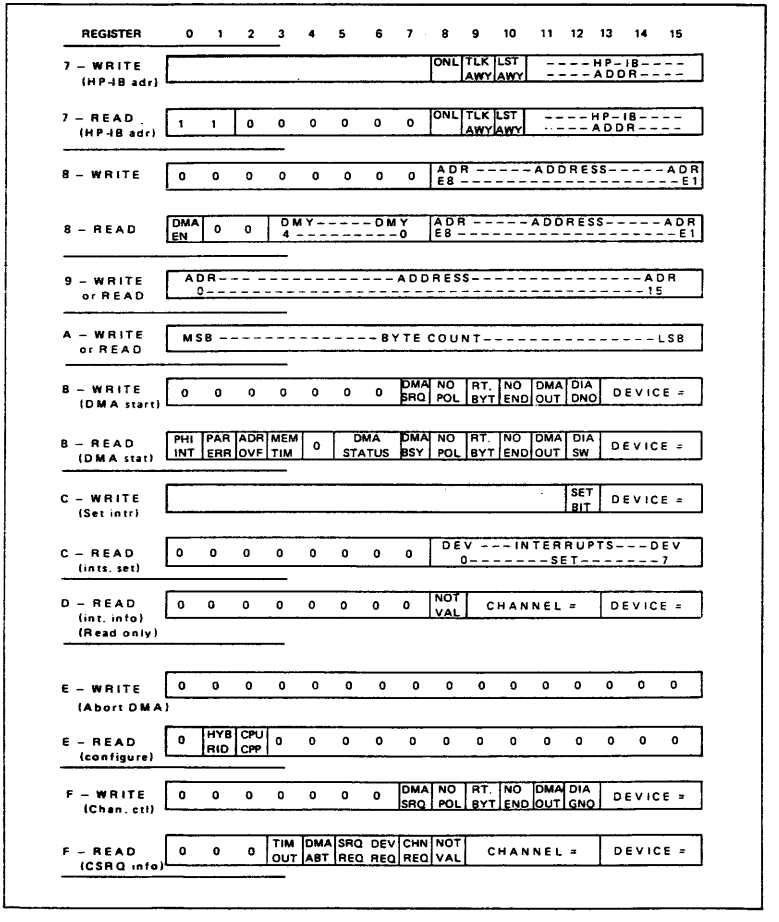


Table 7-2. GIC Register Formats (Continued)



7-46. Register 0 - HP-IB FIFO. Register 0 provides the means for all byte transfers to and from the HP-IB. Each write into the register by the computer causes a word to be placed into an eight-byte long outbound FIFO (first in, first-out). A read from this register obtains a byte from an eight-byte long inbound FIFO, in which incoming bytes are stored upon receipt from the HP-IB. The PHI regulates byte transfer through the handshake cycle. Outbound FIFO entries are used to determine the nature of these transfers. Each entry causes the required handshake(s) to be performed to allow a single byte to be sent out of the outbound FIFO, or one or more bytes to be received into the inbound FIFO. When the outbound FIFO is empty, the PHI automatically conducts a continuous parallel poll on the HP-IB. During this condition, a read from Register 0 obtains the normalized and masked values of the current parallel poll responses being received through the Data Input/Output (DIO) lines of the HP-IB.

If the GIC is Controller-in-Charge, then the PHI will automatically conduct a continuous Parallel Poll on the HP-IB whenever its outbound FIFO is empty. The poll terminates whenever the outbound FIFO is not empty.

A PHI interrupt bit is available to signal an affirmative response to this poll. More specifically, that bit will be set if all of the following conditons are met:

a. The GIC is Controller-in-Charge of the HP-IB and is online,

b. A Parallel Poll is in progress,

c. The inbound FIFO is also empty, and

d. At least one of the devices on the HP-IB is responding affirmatively to the poll.

The GIC's CSRQ logic reads the Parallel Poll response during the IMB OBSI command if:

a. The PHI is online and the GIC is Controller-in-Charge,

b. The PHI Interrupt line is true,

c. DMA is inactive,

d. A Parallel Poll has been in progress for over 2 usec,

e. The PHI DMA REQUEST line is false (inbound FIFO empty), and

f. Bit 8 of register B is 0.

7-47. Register 1 - PHI Status. This register contains the bits which indicate the major states of the HP-IB interface. For example, the status is indicated as to whether or not the PHI is controller-in-charge of the HP-IB.

7-48. Register 2 - PHI Interrupts. This register indicates PHI conditions which can cause assertion of the PHI Interrupt line. Types of interrupts are parity error, status change, handshake abort, parallel poll, service request, state of the FIFOs, and device clear.

7-49. Register 3 - PHI Interrupt Mask. Setting a 1 in a bit position in this register will enable the corresponding bit in register 2 to be set when its condition occurs. A bit set to 0 will prevent that condition from setting the bit in register 2, but will not prevent occurrence of the condition or FIFO freezes performed when that condition occurs. For example, with bit 15=0, and a Device Clear interface is received, both FIFO's would freeze, but the PHI INTERRUPT line would not be asserted.

7-50. Register 4 - Parallel Poll/First Identify Byte. When the GIC is Controller-in-Charge, the value of bits 8-15 are ANDed with the normalized values of DIO8-DIO1 lines, respectively. This is a mask for parallel poll responses. If the register is 0, then no affirmative Parallel Poll responses can be recognized.

When the GIC is being used as an HP 3000/44 device on the HP-IB, bits 8-15 of this register contain the first identify byte.

7-51. Register 5 - Parallel Poll Normalize/Second Identify Byte. When the GIC is Controller-in-Charge, this register is used to normalize Parallel Poll responses on the HP-IB, where bits 8-15 of the register correspond to DIO8-DIO1 lines, respectively. Normalized responses are ANDed with register 4 to mask out selected responses, and the remaining 1's are allowable device requests, which will appear as 1's when register 0 is read for Parallel Poll responses.

If the GIC is not Controller-in-Charge, this register is used as the second byte sent over the HP-IB, tagged with END, when the GIC is Addressed to Identify.

7-52. Register 6 - HP-IB Control. This register provides some control functions for the HP-IB interface. These control functions include parity freeze enable when a parity error occurs, keeps the Remote Enable (REN) and Interface Clear (IFC) lines asserted when the GIC is Controllerin-Charge, responds to a par-

allel poll of the HP-IB, requests service from the Controller-in-Charge, and indicates to the DMA logic the direction of traffic.

7-63. Register 7 - HP-IB Address. This register is used to specify the HP-IB device address of the GIC when it is not Controller-in-Charge. If it is Controllerin-Charge, then it does not respond to this address, but instead:

a. It is always addressed to Listen.
b. Its Talk address is 30.

7-54. Register 8 - DMA Extended Address/DMA Status. Register 8 is used to specify the extended memory address bits of the data buffer for the current DMA transfer (extends addressing range from 16 bits to 24 bits).

7-55. Register 9 - DMA Memory Address. Before a DMA transfer begins, this register must be loaded with the memory word address of the first data byte to be transferred (byte position is specified in register B). This register will be incremented once for every two data bytes transferred during DMA. When DMA terminates, the value read will be the memory address containing the next byte after the last byte transferred. This register may be read during DMA transfers.

7-56. Register A(10) - DMA Byte Count. Before a DMA transfer begins, this register must be loaded with the total number of bytes to be transferred in the current DMA operation (zero means 64 kbytes, but during channel programming, zero is not allowed). This register is decremented before each byte is transferred by DMA. For an input transfer, if counted Receive Data Requests are loaded into the outbound FIFO of the PHI, then be sure that the value of this register is set equal to the sum of the number of bytes specified in all such requests. This is important, since DMA terminates on the END message, or byte count = 0, and not on the last byte of a Receive Data Request although the PHI tag bits 0,1 of the last byte read when the byte count goes to 0 are used to establish the termination status of DMA.

After conclusion of a DMA transfer, this register contains the number of bytes not transferred. If DMA was aborted, then the byte count may be one less than the number of bytes not transferred, or it could be correct depending on where the state machine is when the abort occurs.

7-57. Register B(11) - DMA Status/DMA Control. A write causes DMA control parameters to be loaded and DMA operation to start. A read returns DMA status information and some bits previously written.

7-58. Register C(12) - Interrupt Register. This register has one bit for each of the eight device numbers. When bits are set for devices, and the Interrupt Mask is set, the GIC will assert the IMB IRQ line to request an External Interrupt of the computer system.

7-59. Register D(13) - Interrupt Information. This register is read only and is referenced as a channel register, or with the Obtain Interrupt Information IMB command during External Interrupt processing with the CPU system microprograms.

7-60. Register E(14) - Channel Configuration/DMA Abort. A read of this register identifies the GIC uniquely to the computer system and describes its options in conformance with I/O system design specifications (i.e., channel or device).

7-61. Register F(15) - Channel Service Information. The OBSI IMB command references the same information as a read of this register, but when the register is read directly, Parallel Poll responses will not be checked but will be treated as a PHI Interrupt line assertion. The CSRQ logic controls this register. A write has the same effect as a write to register B. This register is used during channel program execution to set up the channel to generate CSRQ if a particular condition occurs within the PHI, prior to a channel program suspend.

7-62. PHYSICAL CHARACTERISTICS

The GIC circuitry is contained on a single, 7-layer printed-circuit assembly that inserts into its assigned slot in the I/O card cage. The backplane of the PCA has four edge connectors that connect into mating receptacles in the card cage. Connectors P2, P3, and P4 are used for interfacing with the IMB and the power buses. Connector P1 is not used. The frontplane edge connectors are reserved for connecting to external devices. Connector J1 is a test connector which is used for maufacturing testing. Connector J2 is a 30-pin connector used for connecting to the HP-IB through a two-meter long cable. Connector J3 is 27-pin connector that attaches to a flat, ribbon cable for connecting to peripheral interface PCAs that reside in the mainframe (i.e., INP). Figure 7-6 depicts the physical arrangement of the PCA and table 7-3 lists the pin assignments for each connector.

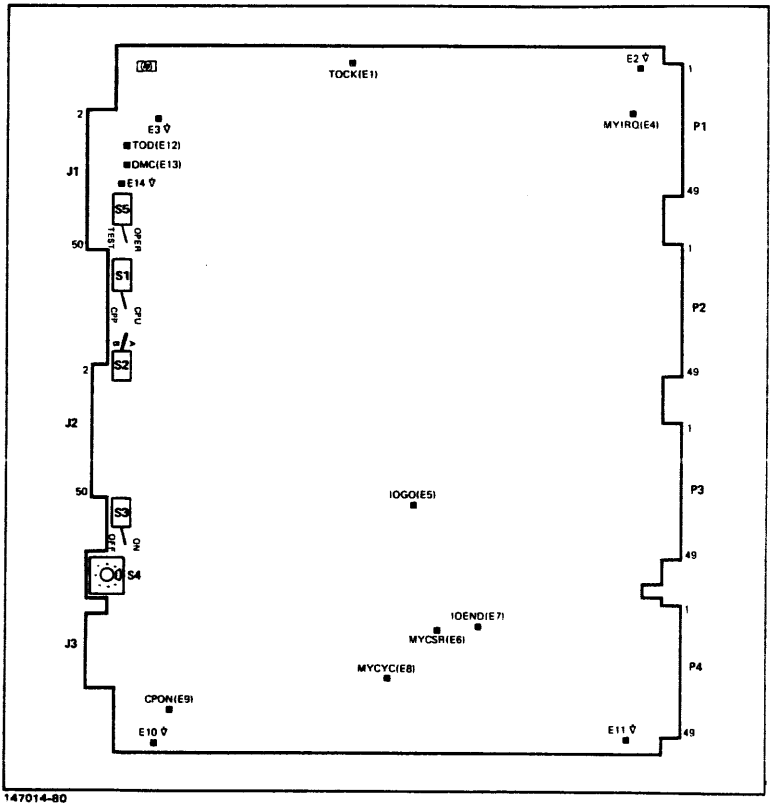


Figure 7-6. GIC Printed Circuit Assembly

Table 7-3. GIC Connector Pin Assignments

Conn. Pin No.	P2 IMB 50	P3 IMB 50	P4 IMB 50	J3 HP-IB 26	J2 HP-IB 30	J1 TEST 50
1	+5v	ADR-7	+5v		DIO1	COM
2	+5v	ADR-6	+5v		DIO2	PLY4
3	+5v	ADR-5	+5v	COM	DIO3	COM
4	+5v	COM	+5v	COM	DIO4	PLY3
5	DATA-15	ADR-4		COM	EOI	COM
6	DATA-14			ATN	DAV	PLY2
7		DNV		COM	NRFD	COM
8		DATA-7		SRQ	NDAC	PLY1
9	DATA-13	DATA-6	CSRQ1	COM	IFC	COM
10	DATA-12	COM	CSRQ2	IFC	SRQ	PLY0
11		DATA-5		COM	ATN	COM
12		DATA-4		NDAC	COM	PLAEN
13		DATA-3	+12v	COM		COM
14		DATA-2	+12v	NRFD	COM	DIAGCK
15	DATA-11	DATA-1	BRQ	COM	COM	COM
16	DATA-10	COM	COM	DAV	DIO5	XDMCKAF
17	DATA-9	DATA-0	BACK	REN	DIO6	COM
18	COM		COM	EOI	DIO7	TOCLK
19	DATA-8	ADR-3	WAIT	DIO8	DIO8	COM
20	ADR-15	ADR-2	COM	DIO4	REN	DIAG
21		ADR-1	ADN	DIO7	COM	COM
22		COM	COM	DIO3	COM	
23	ADR-14	ADR-0	ADO	DIO6	COM	COM
24	ADR-13	ADR-E1	COM	DIO2	COM	MEREN
25		ADR-E2	DDO	DIO5	COM	COM
26		ADR-E3	COM	DIO1	COM	DMCNTEN
27	ADR-12	ADR-E4	DDN		COM	COM
28	COM	COM	COM			TODIS
29	ADR-11	ADR-E5	IRQ		COM	COM
30	ADR-10	ADR-E6	PER		COM	

Table 7-3. GIC Connector Pin Assignments (Continued)

Conn. Pin No.	P2 IMB 50	P3 IMB 50	P4 IMB 50	J3 HP-IB 26	J2 HP-IB 30	J1 TEST 50
31		ADR-E7				COM
32		ADR-E8				
33	ADR-9	OP-2	SRST			COM
34	ADR-8	COM	PFW			XSLAVEF
35	COM	OP-1	COM			COM
36		OP-0	PON			
37		COM				COM
38		PRI				
39		PRI				COM
40		PRI				
41		PRI				COM
42		PRI				
43		PRI				COM
44		PRI				HYBRID
45	COM	PRI	COM			COM
46	COM	PRI	COM			CSRQ2
47		PRI				COM
48		PRO				SYSCON
49		COM				COM
50		PCRY				

7-63. SYSTEM CONFIGURATION

The GIC contains five switches used in configuring and controlling the GIC functions. Table 7-4 describes the functions of the switches.

Table 7-4. Switch Functions

SWITCH	FUNCTION
PROCESSOR Switch S1	A two-position toggle switch that allows the GIC to generate channel service requests (CSRQ) when set to the CPU position. The CPP position is not used.
DEVICE TYPE Switch S2	A two-position (A and B) toggle switch In the normal (A) position, the system performs unit identification during power up (PON). Position B is not used.
SYS CTRL Switch S3	A two-position toggle switch (ON and OFF). When set to ON, the GIC is designated as system controller, and the GIC is controller-in-charge of the HP-IB.
	When the switch is set to OFF, the GIC operates as an HP-IB device. In this mode the GIC controls only peripheral devices, and then only upon command from another GIC that is controller-in-charge.
CHAN ADDR Switch S4	A thumbwheel switch that configures the GIC to an identifying channel number. This channel number establishes IMB priority and the GIC responds accordingly when addressed.
MODE Switch S5	A two-position toggle switch that places the GIC in the operate mode (OPER) or test mode (TEST). When set to TEST the GIC diagnostic can be run. Also, this mode allows the DMA state machine to be singlestepped by clocking the slave flip-flop, prevents a CSRQ command from being issued, and disables the one-second timeout.

SECTION VIII

ASYNCHRONOUS DATA COMMUNICATION CHANNEL

FUNCTIONAL DESCRIPTION

8-1. INTRODUCTION

This section describes the Asynchronous Data Communication Channel (ADCC). The system block diagram illustrates the major functions in the ADCC. The physical characteristics are included with a brief description of each function.

8-2. BLOCK DIAGRAM OVERVIEW

The ADCC provides a bit-serial data interface between the HP 3000 Series 44 Computer System and external peripherals. All data is transmitted and reveived asynchronously, through the use of large integrated circuits called UARTs (Universal Asynchronous Receiver and Transmitter).

The ADCC consists of two PCAs. The first PCA is referred to as the Main ADCC and the second is referred to as the ADCC Extender. The Main ADCC provides up to four RS-232-C ports, each of which contain the serial input and output data lines, and the control lines necessary to interface with devices connected on the RS-232-C lines. The ADCC Extender is added to the Main ADCC to provide an additional four ports, for a total of eight RS-232-C ports. Control for the ADCC Extender is located on the Main ADCC, therefore the ADCC Extender is essentially a slave to the Main ADCC. If more than eight ports are needed, a second Main ADCC must be installed in the system.

The ADCC interfaces between the IMB and RS-232-C lines to provide an orderly flow of data between the computer and devices connected to the RS-232-C lines. Unlike the GIC, the ADCC is an IMB slave only, therefore, it can respond to IMB handshakes but not initiate a handshake. Also, the ADCC can never control the bus.

8-3. IMB Handshake Control

The ADCC will participate in an IMB handshake only if all previous handshakes have been completed and both the address and data are valid for the present operation. The IMB handshake control logic responds to the ADO and DDO commands by setting up the circuitry for transfer, establishing a time frame in which the transfer occurs,handshaking using ADN and DDN, and releasing the handshake upon completion of the transfer. In addition, this logic detects global and nonglobal operations. When an operation is not global, the IMB handshake control enables an address comparator which compares the IMB address with that set by the channel address switch S1 on the front plane. If the addresses compare, then the handshake control logic allows the handshake to occur.

8-4. IMB Command Decoding

The IMB command decoders produce signals that tell the circuitry how to react to various operations. Part of the IMB operation code is used to indicate read and write operations. The appropriate decoder is enabled from the handshake control when the operation is intended for this channel. The decoder outputs then directly select and enable the various circuit modules on the ADCC. During a read, the enabling signal remains valid until the IMB master accepts the ADCC information. For a write, the outputs remain valid only until the ADCC has processed the information.

8-5. IMB Register Decoding

The register decoding logic decodes part of the IMB address to determine which channel register the cycle is to be directed. Writing a specific register will either be used for data transfer, examine service requests and channel configuration, or to access the channel interrupt logic.

8-6. Device Address Latches

When a device is addressed to talk or listen, or when a secondary address is issued, the ATN line on an HP-IB will be asserted to signify a command. If EOI also asserted, a command is not being sent. The ADCC uses the ATN and EOI to know when to interpret the IMB data as addressing information and latch it for use during subsequent IMB cycles. The device address latch distinguishes between operations that are not legal for the ADCC, an address to talk, an address to listen, or a secondary address which contains modifier information. This circuitry also prevents the ADCC from latching talk or listen commands which are sent to the PHI on the GIC when a device transfer is being set up. Other bits in the IMB address are decoded to determine whether the addressed device is connected to the the Main ADCC or Extender ADCC device lines, in order to select a particular device.

8-7. Identify Logic

The Identify instruction causes the device to return two bytes of information which identify the device type. The most significant byte identifies the device as being a data communications classification and the least significant byte says that this is an ADCC. The identify command also sends an Untalk command, followed by a secondary address that contains the device number (0-7).

NOTE

The UARTS on the ADCC are considered to be HP-IB devices, not the RS-232 peripherals connected to the ADCC.

8-8. Channel Program Status Registers

When the IMB command decoder detects an SIOP or HIOP operation, latches in this circuitry enable the program run status information to be stored from the data in (DI) bus. The information contained in this status word includes the device number, location to which the information is going, and indicates whether the command is to start or stop a program. Also, changes in the channel program are noted by a new status register. This means that a change in the device channel program has occurred that has not been processed by the channel program microcode. A change of this nature causes the channel to request service on behalf of the device so that the program can be properly started or stopped.

8-9. Channel Serivce Request Logic

This logic will request service by asserting CSRQ when a change in the channel program occurs, or when the program is running and any of the following conditions are present:

a. The UART for a device has a an empty transmit buffer and the transmit buffer empty service condition is masked on.

b. The UART for a device has a nonfull transmit buffer and the transmit buffer not empty service condition is masked on.

c. The UART for a device has an unread character and no framing error has occurred.

d. A condition is pending, the status of which should be read. For example, if a change in the modem status has occurred, this condition should be read.

8-10. Device Specified Jump Logic

The Device Specified Jump (DSJ) instruction obtains one byte of information from the device in order to calculate a jump in the channel program. The device is addressed to to talk and is sent a secondary address. The ADCC device latches these commands which are not altered until more commands of the same type are received. After the secondary command, the device sends its byte and is then issued an Untalk command. There are four types of responses to a DSJ:

a. Read Request. The device is requesting service because it has received a serial data character that can be read into memory.

b. Write Request. This response occurs if the device is requesting service because its UART can be loaded with a data byte for serialization and transmission over the RS-232C output.

c. Read Status. This response will occur if the UART or modem status should be read.

d. No Request and No Error Pending. The device will return a DSJ byte if there is no service request or uncleared error at the time the DSJ is executed.

8-11. Global Response Logic

The global response logic responds to global commands issued over the IMB. When a command is read, this logic conditions the ADCC to return the proper response. For example, if the global command is a channel roll call, this logic causes the IMB data line that corresponds to the channel address to be asserted. If not, the channel address comparator then compares the IMB address with the channel address.

8-12. Interrupt Logic

When the ADCC is initialized or there has been an I/O Clear command issued, the interrupt register is cleared and the interrupt mask is reset. Interrupts are received by the ADCC and queued into the the interrupt logic, then an interrupt request is asserted onto the IMB IRQ line. The CPU then issues the IPOLL global command to determine which channel has an interrupt pending. After an affirmative response from the highest priority channel with the pending interrupt request(s), the OBII command is issued. The response to the OBII command indicates to the CPU the lowest device number on that channel whose interrupt bit is set. The channel priority-encodes the device requests according to device number, which means that the lowest-numbered device receives the highest priority. After the OBII operation is complete, the interrupt bit is cleared and the CPU microcode enters an interrupt service handling routine. Also, the interrupt mask is cleared to prevent the channel from asserting IRQ.

8-13. Univeral Asynchronous Receiver/Transmitter

The universal asynchronous receiver/transmitter (UART) is a general purpose programmable device that interfaces an asynchronous

serial data device with parallel data of the computer, through the ADCC channel. The UART contains a transmitter section and a receiver section. The transmitter section converts parallel into a serial word containing start, data, parity, and stop bits. The receiver section converts a serial word containing start, data, parity, and stop bits into parallel data. The receiver section also verifies proper code transmission by checking parity and receipt of a valid stop bit. There is one UART assigned to each device on the ADCC. With the Extender ADCC connected to allow a total of eight devices on the channel, there are eight UARTs assigned to associated devices.

8-14. Baud Rate Clock

The baud rate clock consists of circuitry that stores the baud rate for each device, provisions for changing the code when a change is written to it, an internal clock that provides clock rates corresponding to the baud rates, and a rate generator that scans the baud rate codes and selects a corresponding internal clock.

8-15. Special Character Detection

The special characters used in the ASCII code are detected and decoded in this circuitry. Also, when a byte containing a special character is written, it is stored with the the device's list of special characters. When this byte is received on the serial input line and read by the channel program, the byte will be tagged with an END meassage to prevent the instruction immediately following the Read from being skipped. If the device is to recognize more than one special character a separate Write is required to place each one on the list.

8-16. Modem Controls

If the ADCC is connected to a device through a modem, that is, not hardwired, then the ADCC must indicate to the CPU that a modem is being used. Also, the control logic conditions the modem for data transmission or reception.

8-17. Modem Status

Each device has five input lines which can be used to monitor the status of the device. These lines are normally used with modems to detect changes in the modem status or communication line. The input lines are designated Clear To Send (CB), Data Set Ready (CC), Signal Detect (CF), and Secondary Signal Detect (SCF), which correspond to standard modem signals. The modem status

logic contains programmable references and masks. If any of the status signals disagrees with its reference and its mask is enabled, the device will request service. The service request will continue until the signal changes to agree with its reference, the reference is changed, the signal is masked off, or the device channel program is halted.

8-18. Break Detection Logic

When a break occurs, this logic allows the device to request service after the serial data line has returned to the MARK condition. If a framing error occurs, the logic will hold off a service request for a period of time to allow the character to be read. A framing error may be detected if the proper stop bits were not tagged onto the the character bits, or were lost in transmission.

8-19. PHYSICAL CHARACTERISTICS

The Main ADCC contains two switches on the front plane. Connectors J1 and J2 are on the front plane. Connector J1 on each PCA are interconnected by a flat cable when the Extender ADCC is used. Connector J2 is a 56-pin connector that contains all the RS-232-C signals for four devices. Figures 8-1 and 8-2 depict the PCAs, location of test points, connectors, and switches. Tables 8-1 through 8-3 identify pin assignments for all edge connectors on the PCA. Pin assignments are the same for both PCAs.

8-20. SYSTEM CONFIGURATION

Two switches mounted on the front plane configure the ADCC. These switches are described as follows:

WPLS Switch S1.

This is a 16-position rotary switch that selects the IMB channel address of the ADCC. Positions 1 through 15 are usable for address numbers. Position 0 is not used.

CPU/CPP Switch S2.

A toggle switch that selects whether the channel programs for the ADCC are executed by the CPU or not. Since the CPP position is not used, the switch must always be set to CPU for operation.

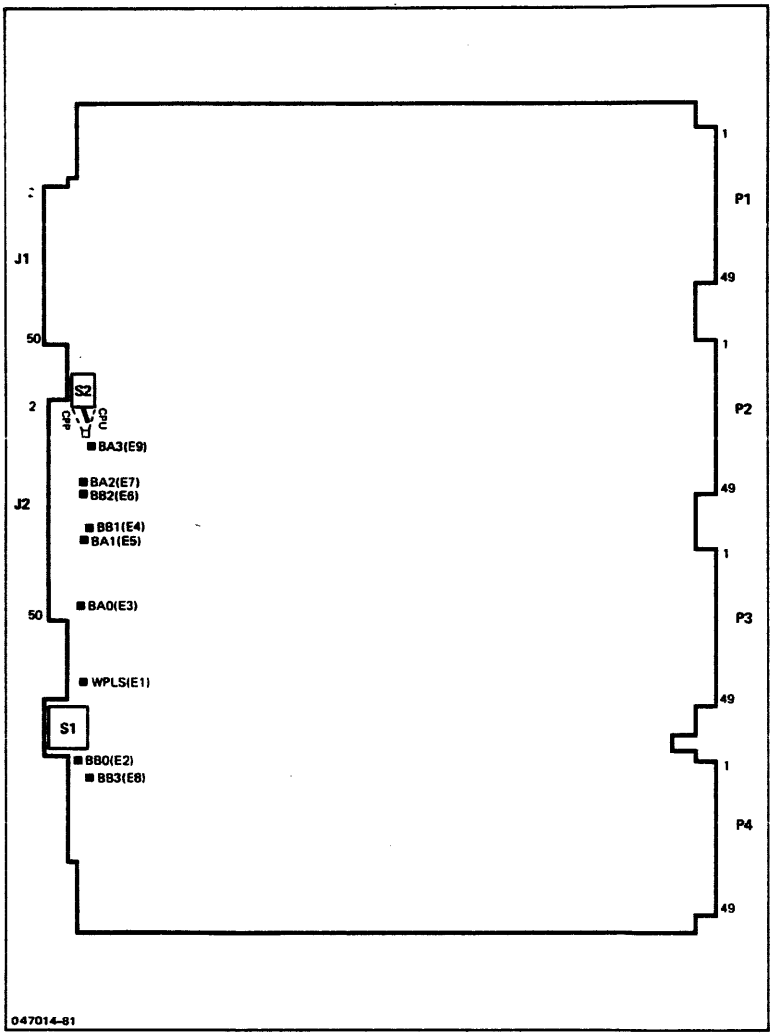


Figure 8-1. ADCC Main PCA

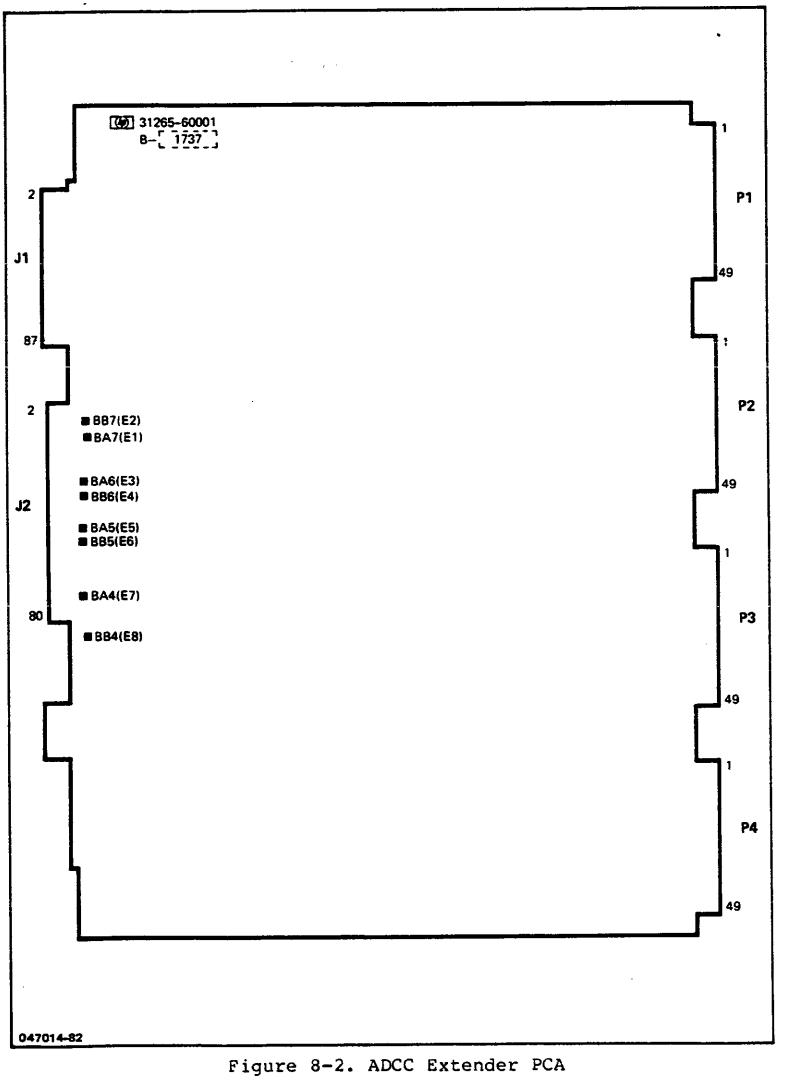


Figure 8-2. ADCC Extender PCA

Table 8-1. Connectors P2 Through P4 Pin Assignments

P2				P3				P4			
Pin	Sig	Pin	Sig	Pin	Sig	Pin	Sig	in	Sig	Pin	Sig
1	+5V	2	+5V	1	ADR7	2	ADR6	1	+5V	2	+5V
3	+5V	4	+5V	3	ADR5	4		3	+5V	4	+5V
5	D15	6	D14	5	ADR4	6		5		6	
7	-12V	8	-12V	7	DNV	8	D7	7	-12V	8	-12V
9	D13	10	D12	9	D6	10	GND	9	CSRQ1	10	CSRQ2
11	FPLD	12	FPRST	11	D5	12	D4	11		12	
13	+12V	14	+12V	13	D3	14	D2	13	+12V	14	+12V
15	D11	16	D10	15	D1	16	GND	15	BRQ	16	GND
17	D9	18	GND	17	D0	18	PAR BIT	17	BACK	18	GND
19	D8	20	A15	19	ADR3	20	ADR2	19	WAIT	20	GND
21	-12M	22	-12M	21	ADR1	22	GND	21	ADN	22	GND
23	A14	24	A13	23	ADR0	24	E1	23	ADO	24	GND
25	+5M	26	+5M	25	E2	26	E3	25	DDC	26	GND
27	ADR12	28	GND	27	E4	28	GND	27	DDN	28	GND
29	ADR11	30	ADR10	29	E5	30	E6	29	IRQ	30	PER
31	+12M	32	+12M	31	E7	32	E8	31	+12M	32	+12M
33	ADR9	34	ADR8	33	OP2	34	GND	33	SRST	34	PFW
35	GND	36	PON	35	OP1	36	OP0	35	GND	36	PON
37		38	FPDMP	37	GND	38		37		38	
39	FPHLT	40	FPRUN	39		40		39		40	
41	FPIO	42	FPLED	41		42		41		42	REMOTEN

Table 8-1. Connectors P2 Through P4 Pin Assignments (Continued)

P2				P3				P4			
Pin	Sig	Pin	Sig	Pin	Sig	Pin	Sig	Pin	Sig	Pin	Sig
43	CHL2	44	CHL1	43		44		43		44	
45	GND	46	GND	45		46		45	GND	46	GND
47	DEV1	48	CHL3	47		48		47		48	
49	DEV3	50	DEV2	49		50		49		50	

Table 8-2. Connector J1 Interconnect Wiring

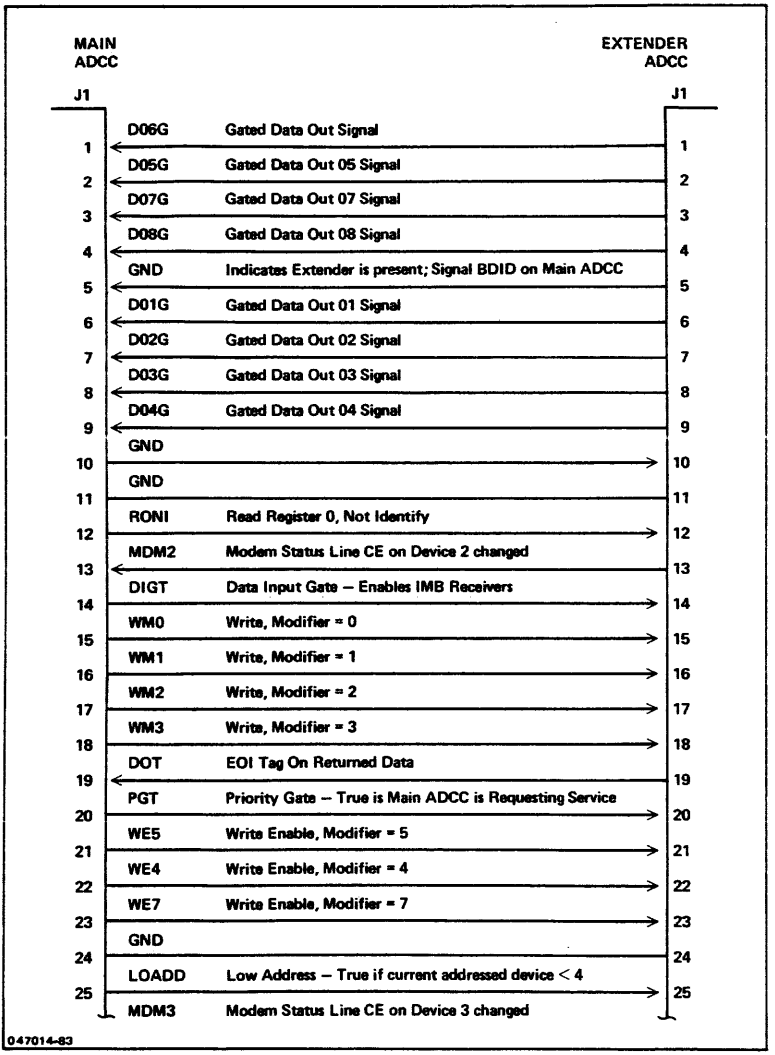


Table 8-2. Connector J1 Interconnect Wiring (Continued)

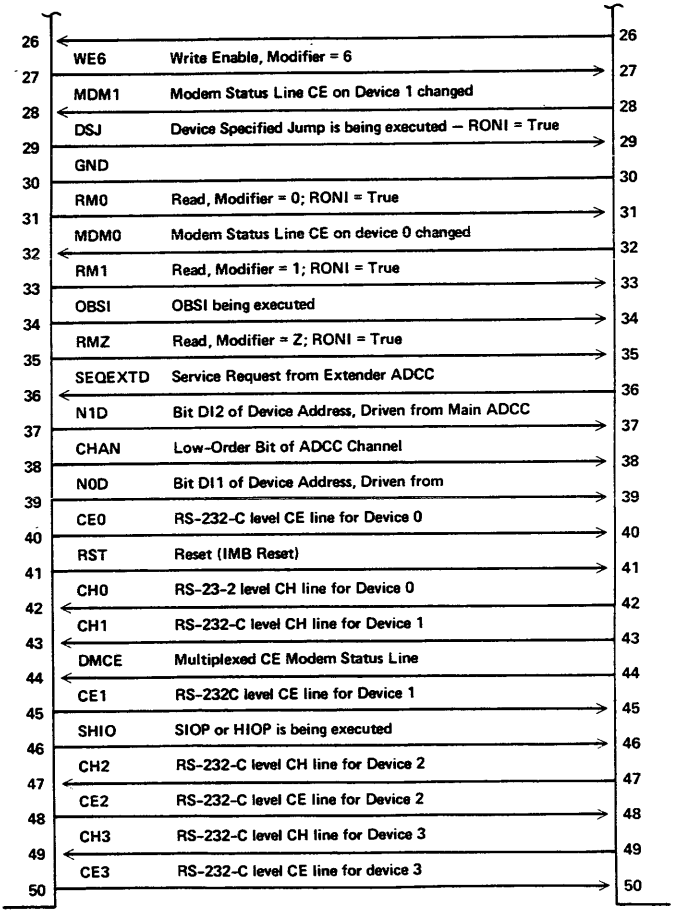


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Table 8-3. Connector J2 Pin Assignments

Pin	Signal	Dev/Pin	(J2) Pin	Signal	Dev/Pin
1	CE3(7)	3-32	26	SCF0(4)	0-12
2	CC3(7)	3-6	27	CA0(4)	0-4
3	BB3(7)	3-3	28	CD0(4)	0-20
4	SCF3(7)	3-12	A	CH3(7)	3-23
5	CA3(7)	3-4	B	CB3(7)	3-5
6	SCA3(7)	3-11,19	C	CF3(7)	3-8
7	AB3(7)	3-7	D	BA3(7)	3-2
8	CH2(6)	2-23	E	CB3(7)	3-20
9	CB2(6)	2-5	J	CE2(6)	2-22
10	CC2(6)	2-6	K	AB2(6)	2-7
11	BA2(6)	2-2	L	CF2(6)	2-8
12	CA2(6)	2-4	M	SCF2(6)	2-12
13	SCA2(6)	2-11,19	N	BB2(6)	2-3
14	CB1(5)	1-5	P	CD2(6)	2-20
15	CC1(5)	1-6	R	CE1(5)	1-22
16	CF1(5)	1-8	S	CH1(5)	1-23
17	BA1(5)	1-2	T	AB1(5)	1-7
18	CD1(5)	1-20	U	BB1(5)	1-3
19	SCF1(5)	1-12	V	CA1(5)	1-4
20	CH0(4)	0-23	W	SCA1(5)	1-11,19
21	AB0(4)	0-7	X	CE0(4)	0-22
23	CB0(4)	0-4	DD	BA0(4)	0-2
24	CC0(4)	0-6	EE	SCA0	0-11,19
25	CF0(4)	0-8	FF	BB0(4)	0-3

NOTE: Numbers in parentheses indicate device numbers and signals connected to the Extender ADCC. For example, Pin 1 of J2 is connected to CE3 on Main ADCC and to CE7 on Extender ADCC. This signal connects Main ADCC to device 3, and to device 7 from Extender ADCC.

SECTION IX

POWER DISTRIBUTION

FUNCTIONAL DESCRIPTION

9-1. INTRODUCTION

This section describes the power distribution for the HP 3000/44 Computer system. The description includes ac power distribution, dc power distribution, power supply units, and service information. Also, the battery backup is discussed.

9-2. AC POWER DISTRIBUTION

The AC power distribution for the HP 3000/44 consists of an isolation transformer and one of two types of power control modules. Table 9-1 lists the input AC power requirements.

Table 9-1. AC Input Specifications

POWER REQUIREMENTS	
Line Voltage:	200,210,220,230,240 VAC, single phase
Voltage Tolerance:	+4% to -10%
Line Frequency:	50 Hz or 60 Hz +/- 0.5Hz
Power Consumption (less peripherals)	
One Card Cage:	1280 watts at 60 Hz, 1400 watts at 50 Hz
Two Card Cages:	2160 watts at 60 Hz, 2220 watts at 50 Hz
Input Current Rating (at full load, no devices connected to receptacles at rear of cabinet)	
One Card Cage:	8.3A at 208 VAC, 60 Hz; 8.1A at 220 VAC, 50 Hz
Two Card Cages:	13.1A at 208 VAC, 60 Hz; 12.4A at 220 VAC, 50 Hz
Current Available to Peripherals:	20A at 120 VAC, 50 or 60 Hz
Circuit Breaker Rating:	24A

9-3. Power Control Module

The Power Control module (PCM) is used to provide AC power distribution and line protection for the HP 3000/44 computer system. The PCM is located at the bottom right rear of the system cabinet.

9-4. AC Distribution. The distribution of AC power is available to operate the system power supplies (30090-60035), cooling fans, and auxiliary equipment (system disc, system console, mag. tape). Two types of PCM's are designed to provide the necessary power distribution media, both TYPE 1 (for use in USA, Canada, Japan, etc.) and TYPE 2 (for use in most European countries and other countries) are the same except that NEMA 5-15R receptacles are used for Type 1 and CEE 22-VI receptacles are used for Type 2. In addition, circuit breakers CKB 2 and CKB 3 have different ratings for the two types of PCM; a 15 amp breaker is utilizied in the TYPE 1 PCM, while the TYPE 2 PCM uses 10 amp breakers. For detailed block diagrams see figure 9-1 for the TYPE 1 PCM and figure 9-2 for the TYPE 2 PCM.

9-5. AC Line Protection. The primary AC line protection is provided by a 24-ampere breaker on the main AC input to the the HP 3000/44 mainframe. This breaker can also be used to simulate a power-fail condition to test the functional operation of the battery backup facility.

The secondary breakers (CKB 2 and CKB 3) provide circuit protection for the external receptacles used by the peripheral equipment, such as the system disc, system console, etc..

Another secondary breaker (CKB 4), which is 20 amperes for both TYPE 1 and TYPE 2, is located in the side panel (adjacent to the operators right knee). This circuit breaker is used to switch ON and OFF the mainframe power only, and it also provides circuit protection for the internal system components such as the power supply units and the air plenums.

NOTE

The two auxiliary switches, integrated with CKB 4, are used to switch the batteries off line. This is necessary during transportation of the HP 3000/44 computer system or during extended periods of service to prevent the batteries from discharging.

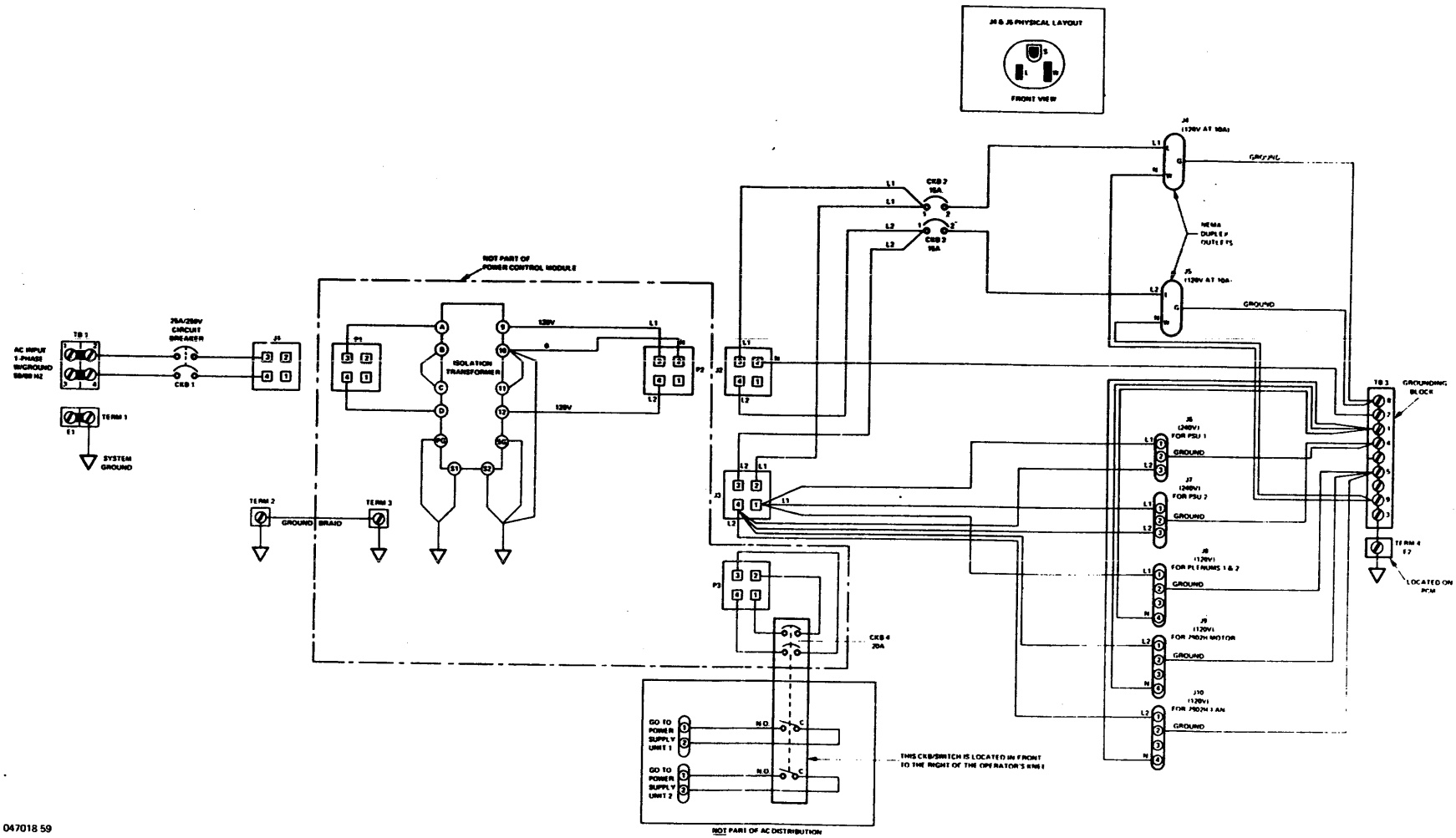

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Figure 9-1. Type 1 PCM

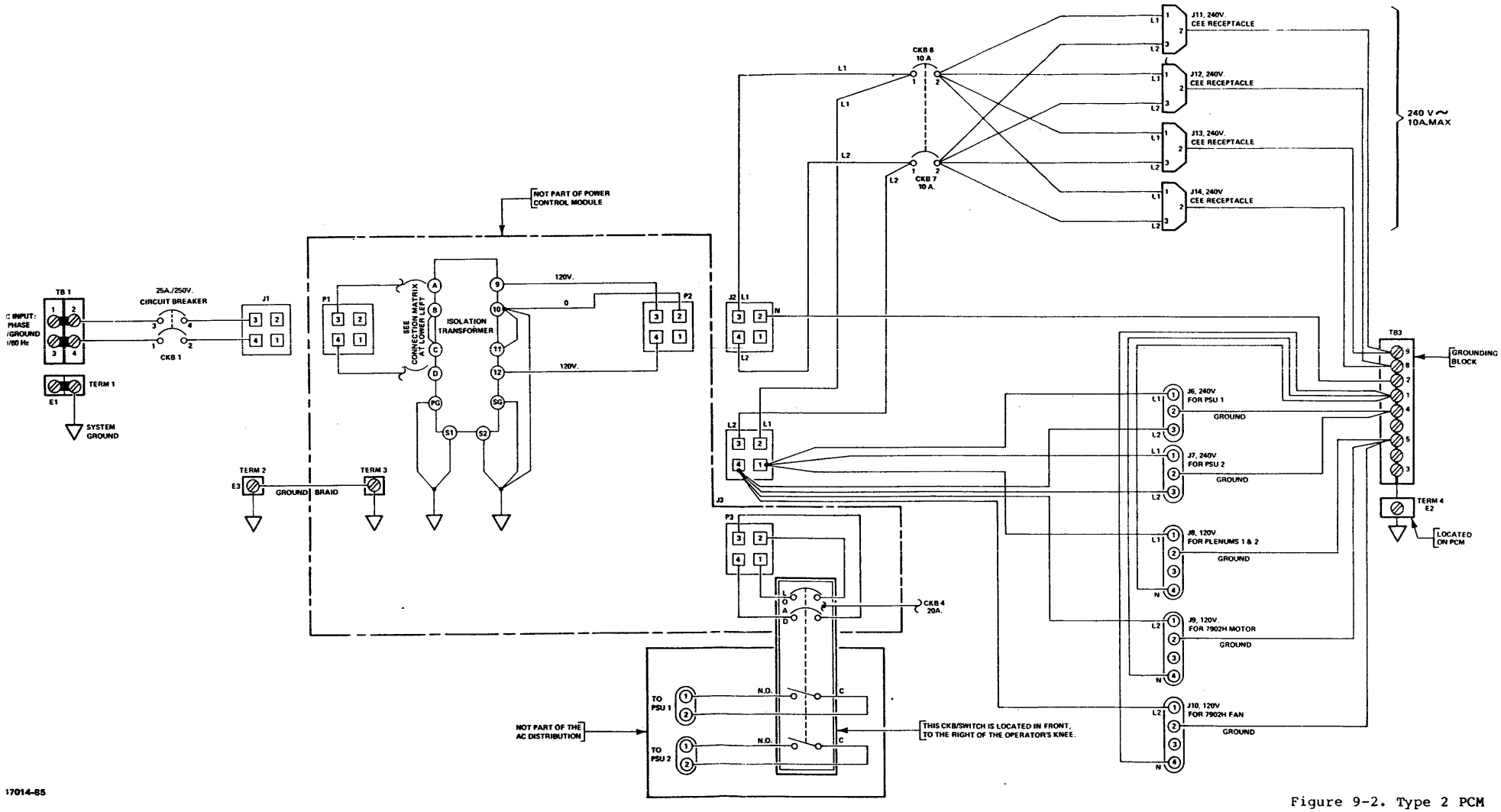

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Figure 9-2. Type 2 PCM

9-6. AC Isolation Transformer

The isolation transformer is used to protect the computer system from the effects of transient voltages and line noise caused by other equipment and power disturbances.

The isolation transformer has a rating of 5000 volt-amperes and weighs 112 pounds. It has five voltage strappings (200-240 volts in 10 volt steps) on the primary input windings. The secondary has two 120 volt windings, which are connected in series with grounded center tap to give a 120/240 volt output. The line to neutral voltage of 120 VAC is connected to the outlets (60 Hz system) or the line to line voltage of 240 volts (50 Hz systems) for external power needs.

Isolation Transformer Specifications:

* >125 decibels for Common-Mode noise rejection
* 20 decibels per decade attenuation at frequencies greater than 100 Hz, for Differential-Mode noise rejection
* 0.001 picofarad interwinding capacitance; primary to secondary.

Table 9-2. shows the strapping information for converting the isolation transformer primary windings input.

Table 9-2. Isolation Transformer Jumpers

Input Voltage	Jumpers	
	Jumper	Line Voltage
200	2-5	1-6
210	3-5	1-6
220	3-5	1-7
230	4-5	1-7
240	4-5	1-8

9-7. DC POWER DISTRIBUTION

The Series 44 Computer System contains at least one 30090-60035 power supply to power the processor unit PCA's. A second power supply is added when when the second card cage is installed in the system. Figures 9-3 and 9-4 show single and dual power supply configurations.

9-8. DC Indicators and Test Points

The indicators mounted on the front panel of the power supply and on the respective card cage backplanes are provided to monitor the power supply status. The system control panel provides power-on status through the use of a POWER LED and power low indicators for DC power failures, AC low conditions, and overtemperature conditions. In addition, test points on the power supply front panel are provided as an aid in troubleshooting.

9-9. Test Points and Indicator. There is one LED and eight test points located on the front of the PSU. The LED indicates that the +5V from the HP 63909F is on. The test points +5, +12, and -12 indicate the voltages from the HP 63909F, while the test points +5M, +12M, and -12M indicate the voltages from the memory supply. The test point BATT indicates the battery voltage and PON indicates the power on condition. All of the DC test points are return from the backplane and reflect the voltage drop from the power supply to the backplane. Figure 9-5 shows the location of the indicators and test points on the power supply front panel.

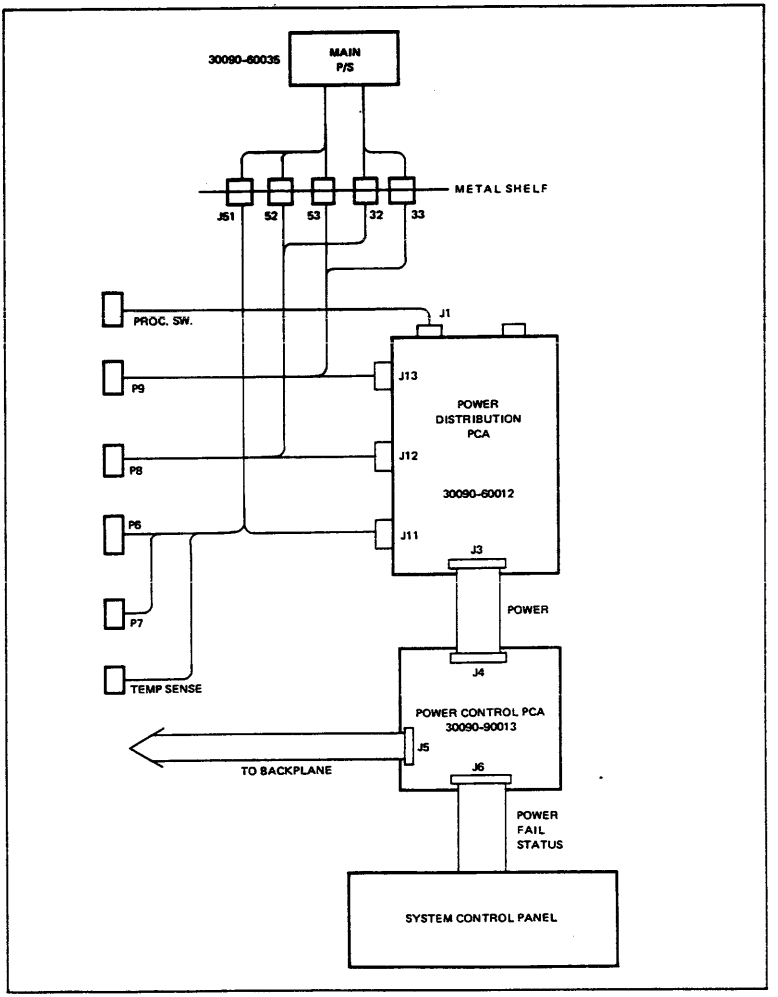

Figure 9-3. DC Power Distribution (Single Power Supply)

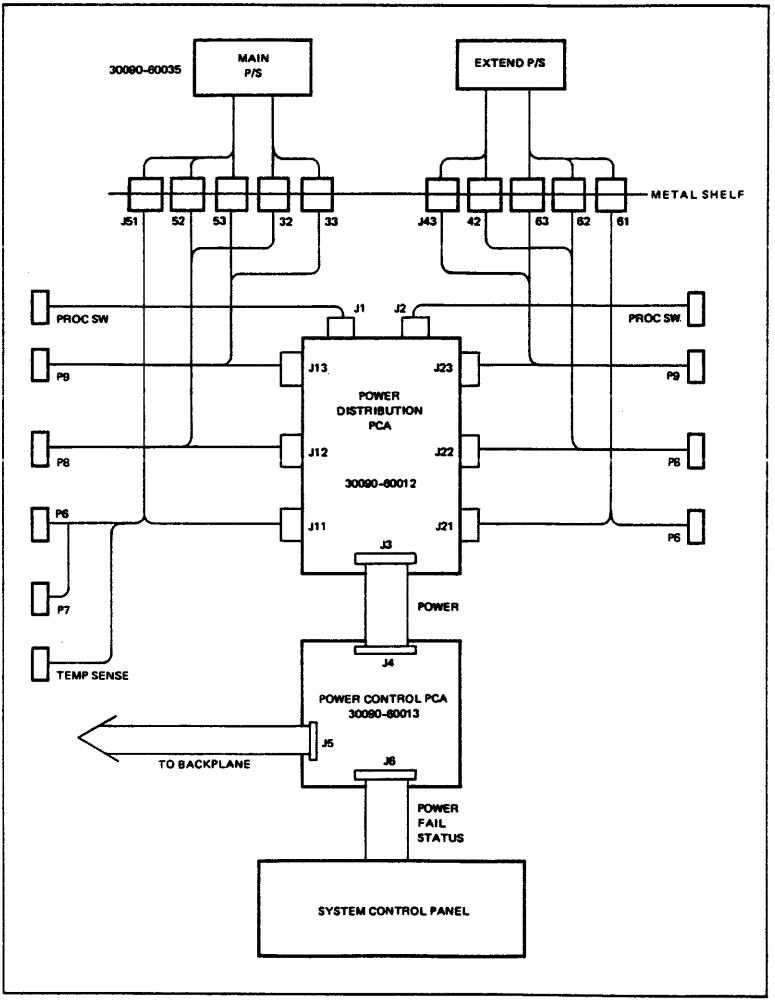

Figure 9-4. DC Power Distribution (Dual Power Supplies)

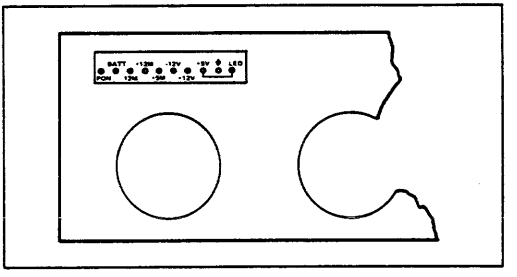

Figure 9-5. Power Supply, Front View

9-10. Battery Charge/Discharge Indicators. To indicate proper operation of the charge circuitry or warn of the memory backup battery discharging into a load, two LED's are incorporated on the memory preregulator board. A green LED, indicating charging current, is at its brightest when the battery is charging and dims as the charge current lowers and battery approaches maximum charge. The red LED indicates that the battery is discharging and supplying current to the load. Both LED's are off during normal operation with a fully charged battery.

9-11. Backplane LED's. There two LED's on the lower left corner of the backplane. The LED's are +12 volts (red) and +12M volts (yellow) indicators for the DC voltages of the power supply unit. Should any of the main power supply output fail the +12 volt (red) LED will be out or should any of the memory supply outputs fail the +12M volt (yellow) LED will be out.

NOTE

These indicators are only a convenient way to quickly indicate the operation of the power supply unit. The power supply unit must be checked using the procedures outlined in the power supply service information part of this section.

Figure 9-6 shows the location of the indicators on the card cage backplane.

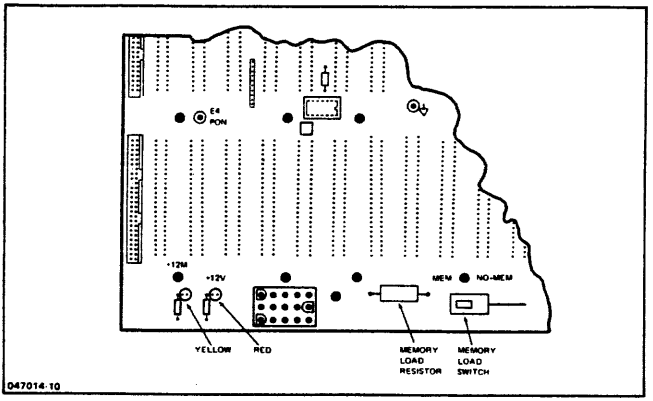

Figure 9-6. Card Cage Backplane

9-13. SYSTEM POWER SUPPLY UNIT

Each card cage in the HP 3000/44 processor unit is supplied power from a single power supply that provides both main and memory power. When two card cages are used in a system, two power supplies are installed and operate independent of one another.

The power supply consists of a 545-watt power supply module (63909F) and a 98-watt memory supply which has a battery backup of approximately 15 minutes. These components are packaged in a single unit and operates from 240-VAC single-phase power. Figure 9-7 depicts the functional areas of the power supply.

9-15. Main Power Supply

The HP 63909F main power supply is a switching-regulator style supply, providing three different DC voltage outputs to the system. They are +5 volts, +12 volts, and -12 volts. The maximum currents available from each of the output voltages are 85A, 5A, and 5A respectively. The total output power limitation is 545 watts over the temperature range of 0 to 40 degrees C. Remote voltage sensing is used for all outputs to the system backplane. The remote sensing of all three output voltages is necessary in order to maintain good voltage regulation at the load by reducing the degradation that would occur due to the voltage drop in the cables between the power supply and the backplane.

9-13. PCA Power Consumption

Table 9-3. shows the current and power consumption of all HP 3000/44 PCA's.

Table 9-3. PCA Power Consumption

P.C. Boards	Current Drain (Amperes)						Total Power (watts)
	+5V	+12V	-12V	+5M	+12M	-12M	
GIC	4.37	0.05					22.45
ADCC-Main	2.19	0.10	0.07				12.99
ADCC-Extender	1.73	0.10	0.06				10.57
ALU	8.35						41.75
CTL (fully loaded)	11.80						59.0
PCS (fully loaded)	8.92						44.6
CMP	2.07	0.05	0.05	0.09			12.0
Memory Cntlr	5.20			0.63			29.15
Memory Array (active)	0.74			0.53	1.54	0.018	25.046
Control Panel	0.29						1.45
INP	2.44	0.50	0.12	0.24	0.36	0.008	25.26
Printer Interface	2.30	0.03					11.86

9-16. Memory Power Supply

The Memory supply consists of the memory preregulator PCA, a 14 volt, 7-cell, lead-acid battery, and the memory regulator PCA. The input power to the memory supply is from the 28.27 VAC output of 240 volt AC transformer, T1, to provide power for the memory regulator and the charge current to the battery. The voltage is rectified and filtered to provide 40 VDC input to the memory preregulator at normal line voltage.

During normal operation, the memory voltages are supplied by the memory preregulator and memory regulator boards. The battery backup in the memory power supply is always connected on-line when the system ON/OFF switch is turned ON.

NOTE

The system ON/OFF switch in the OFF position will automatically open the battery line. This will avoid unnecessary voltage discharge of the battery during shipment of the system or during service.

When a line voltage failure occurs, the battery provides the power to the memory regulator to maintain the memory voltages. The power supply will not function properly without the battery.

9-17. Memory Preregulator. The memory pregulator is a switching regulator of 40 kHz rate to provide power to the memory regulator, and also provides a constant source mode to charge the battery at about 650 MA maximum and provide power to the memory regulator. The preregulator output voltage is determined by the state of charge and temperature of the battery. The thermistor in contact with the battery monitors its temperature and adjusts the output voltage of the preregulator. When the battery reaches full charge at any given temperature, the voltage limit mode of the charger dominates and the charge current is reduced to a very low level.

The output voltage from the preregulator is normally set (by R10) to about 16.45 volts at room-temperature.

9-18. Battery Pack. The battery pack is a 14 Volt, 7-cell lead acid battery. At room temperature (23 degrees C) the battery no-load voltage should be about 2.35 volts per cell or 16.45 volts DC for the entire battery pack at full charge.

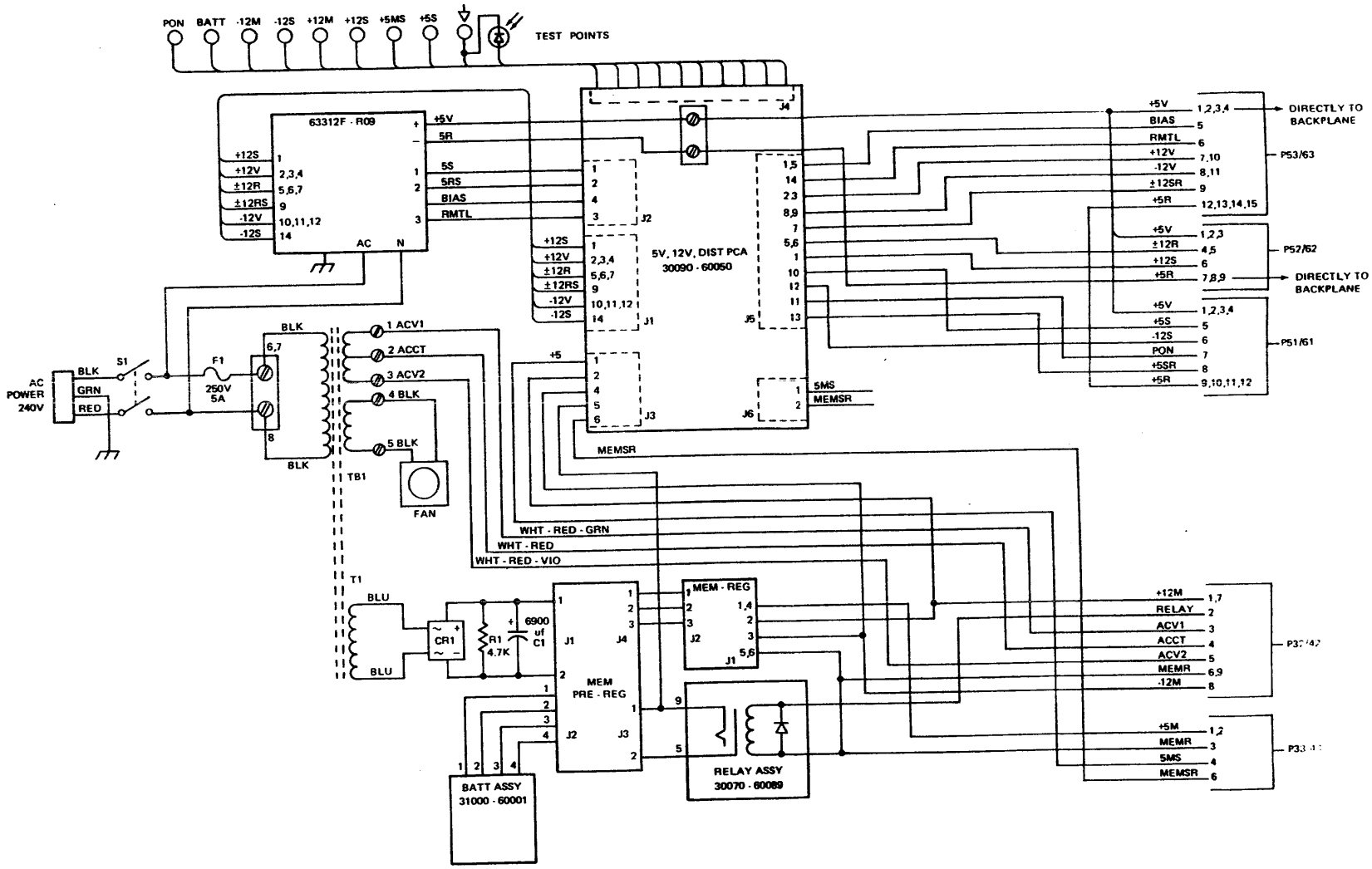

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Figure 9-7. Power Supply Block Diagram

9-19. Memory Regulator. The memory regulator assembly has a series regulator for the +12M volt output and a switching regulator for the +5M and -12M outputs. The input voltage (approx. 16.45 volts) to the memory regulator is the same whether the power is derived from the battery during a power failure or the preregulator when the input line voltage is normal. In the absence of AC line voltage the battery will continue to provide input power to the memory regulator until a preset voltage (about 12 volts) is reached, at which time the memory regulator will sense the battery condition and shut off all output voltages, this will keep the battery from further discharging to zero volt.

The memory regulator assembly circuitry is designed to bring up the +5M and -12M voltages prior to the +12M volts. The +12M voltage is held at zero until the -12M supply exceeds about -9 volts, thus preventing possible damage to the memory RAM chips. There is a minimum load (0.5 A) required on the +5M output in order for the +12M and -12M to be present or regulated. Hence, in the HP 3000/44 system, a minimum load is provided at the card cage backplane with a switchable load resistor. When there is no memory in the card cage, switch to the NO MEM position; otherwise switch to the MEM position.

9-20. POWER CONTROL

9-21. General Description

The power control PCA contains undervoltage sensing circuits to protect the computer system hardware in the event the main power supply voltages fall below the preset level. (See figures 9-8.) This PCA also contains a low-line detector that monitors the AC input voltage. Two signals are generated on this PCA, Power Fail Warning PFW- and Power On (PON). The circuits on this PCA disable system operation when the input AC line voltage is too low, or when an overtemperature condition exists. Also, the circuits shut down the DC power supplies if a DC undervoltage fault occurs.

9-22. Operation

Two signals to the system backplane provide power status information to the system. These are high-true Power On (PON) and low-true Power Fail Warning (PFW-). When low level, PON is used by the system hardware for system reset and initialization. When true, PFW- indicates that the input AC power is above 85 percent of nominal rating, and that the power supplies are on. PFW- is a power status signal that alerts the system of an impending power failure before the DC output voltages actually go off. The CPU uses this to initiate an oderly shutdown of the operating system.

The power supply Remote Disable (RMTL) signal is asserted low to shut off all DC outputs if an overtemperature, AC low or DC low conditions occurs. In the event of any of these failure states, the power control PCA will send power status information to the system control panel display.

The AC low-line detector uses two comparators and a low-pass filter to detect the average of the line voltage waveform. These circuits trigger on each half cycle of the waveform and are referred to as VON and VOFF. VOFF triggers at 85 percent of the nominal rating of the AC line voltage, and VON triggers at 90 percent. This provides hysteresis between turn-on and turn-off voltage levels.

At initial turn-on, PFW-, PON, and RMTL are low, thus the DC voltage outputs are initially disable until the AC line voltage is more than 90 percent of its rated nominal value, which triggers VON. Then, the DC supplies are enabled when RMTL goes to the high state. If the line voltage remains above the VON level with the added load of the power supplies, PFW- goes high, and approximately 1.5 seconds later PON also goes high, thereby allowing system operation to begin.

Continuous normal operation is allowed ad long as the input AC line voltage remains above the lower low-lime detector level VOFF. If the line voltage drops below VOFF for a full cycle or longer, PFW- is asserted low, and at a minimum of two milliseconds later, PON also goes low to indicate the the DC voltages may be going down. The AC line voltage must return to above the higher low-line detector VON to restart the system. If the line voltage remains below the VOFF level for 25 ms or longer, RMTL goes low, disabling the power supplies (main and extend, if two card cages are installed). The line voltage must return to above the VON threshold before the power supplies will be allowed to turn on.

The hysteresis provided by the two low-line detector levels is needed to prevent a system restart just after shutdown. With only one low-line detector, the small increase in the the AC line voltage could trigger a system restart. An oscillating condition of attempted restarts and power fail shutdowns would result.

At initial turnon, the power supplies are prevented from turning on for 20 ms. PFW- and PON are low while the DC supply voltages are coming up and settling. A minimum of 50 ms after the input line voltage exceeds 189 VAC, PFW- goes high. Approximately one to two seconds later PON goes high, allowing the system to operate.

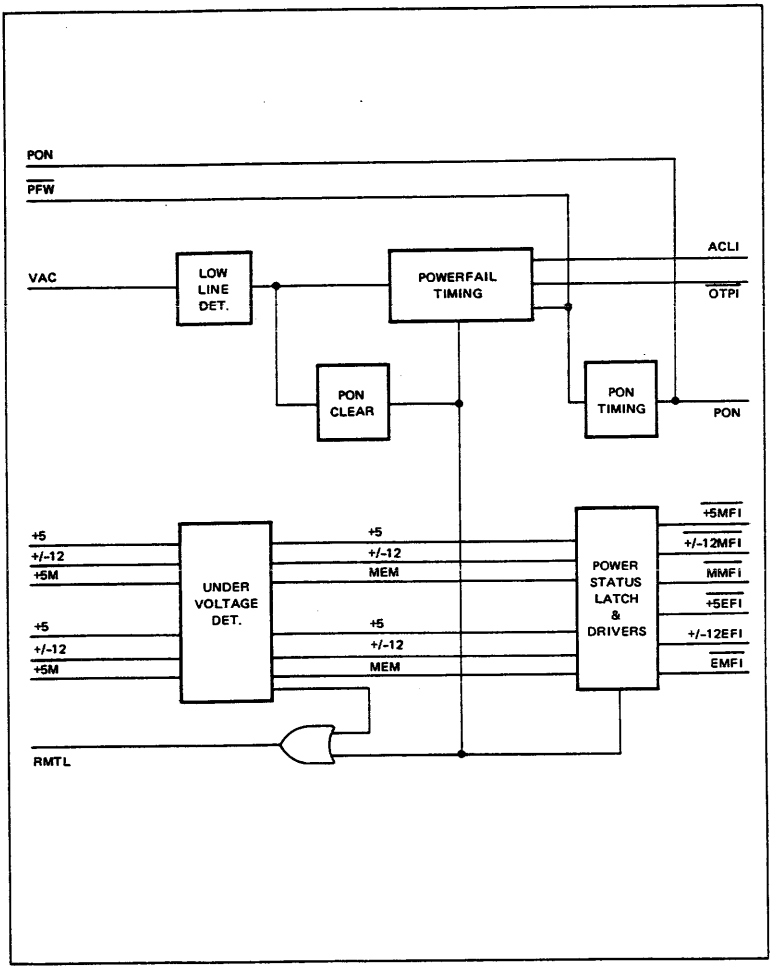

Figure 9-8. Power Control PCA, Block Diagram

If the AC line voltage drops below the minimum specified value for longer than 28 ms, PFW- will be asserted low which initiates a power down sequence. A minimum of two milliseconds later, PON goes low and the DC voltages may begin to drop. The two milliseconds is the time available for system shutdown.

9-23. DC Undervoltage Shutdown. Undervoltage detection is provided for the +5, -12, +12, and +5M volt DC outputs from the power supplies. The undervoltage detector circuit is powered from the +15volt bias supply. The +5-volt output undervoltage detection level is approximately 4.17 volts. The +12 volts is divided down to +4.86 volts and compared to the 4.17 volts in the undervoltage detection circuitry. The -12 volts is divided down from the +12 sense so tha an undervoltage will be detected if the -12 volts drops to -10 volts. If both the +12 volts and -12 volts drop, the +9-volt undervoltage detector will be enabled. It also trips when both +12 volts and -12 volts exceed 14.7 volts and provides an overvoltage protection in addition to that in the main power supply.

The outputs of the undervoltage detection circuitry are stored in a status latch and also sent to failure detection circuitry which detemines if any supply is undervoltage. The status latch indicates which supply failed to reach its operating voltage by lighting the corresponding LED on the system control panel. At initial power-on, the status latch and overtemperature latch are cleared and a fixed time of two seconds is provided to allow the supplies to settle before PON can go high.

9-22. Overtemperature Shutdown. In the event one of the card-cage temperature sensors detects an overtemperature condition, the CMP logs the condition, prints a message on the console screen, and shuts down the main power supply(s). If the CMP is defective and does not shut off main power within 2 ms of the overtemperature indication, the power control PCA will shut off main power (but without logging or console messages).

Once main power is shut down, the system behaves as if there was an AC power failure, except that the batteries continue to be charged and the system fans continue to operate. The operator can leave the system in this state as long as desired without danger to the components while room temperature and fan operation are checked, and makes an necessary calls for a customer engineer.

After the condition has been corrected and the machine cools down, the operator can turn the main power circuit breaker on the PCM off, then on, to start the system and resume operation as though only a short power failure had occurred.

The CMP SHUTTEST command can be issued at any time to simulate the CMP shutting down the power supplies as it would on an over-temperature condition.

9-25. Power Turn-On Sequencing. At initial turn-on, the power supplies are prevented from turning on for 20 milliseconds. PFW and PON are low while the DC supply voltages are rising to the rated values and settling. A minimum of 50 milliseconds after the input AC line voltage exceeds 189 volts , PFW goes high, and one to two seconds later PON goes high allowing the system to operate. (See figure 9-9.)

If the AC line voltage drops below the minimum specification for longer than 28 milliseconds, PFW will be asserted low activating a power down sequence. Two milliseconds later, PON goes low and DC voltages may begin to drop. This two-millisecond period is available for system shutdown.

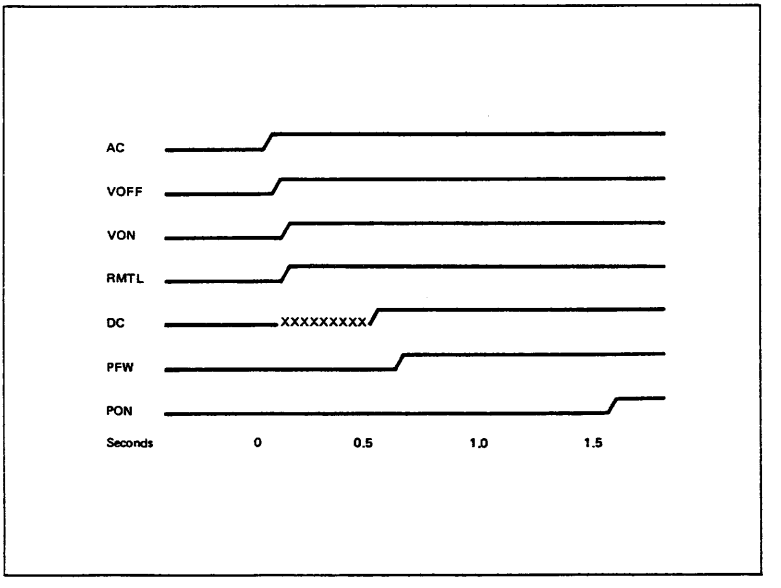

Figure 9-9. Functional Timing Diagram

Power

9-26. Power Distribution PCA's

The power distribution assembly is a sheet metal assembly mounted

Some of the output voltages of the power supply are distributed through the second power distribution PCA (part no. 30090-60050), which is edge-connected to the 63909F power supply. This assembly is mounted securely with five screws on the rear of the power supply. The +5-volt output from the 63909F power supply is connected directly to the power supply cable.
behind the system control panel. This assembly contains the power control PCA (part no. 30090-60013) and the main power distribution PCA (part no. 30090-60012). All DC power for both the main and extend card cages is provided through this assembly from both the main and extend power supplies.

9-27. POWER SUPPLY SERVICE INFORMATION

Preventive maintenance and troubleshooting procedures for the power supply are contained in the following paragraphs. The preventive maintenance procedures must be performed on the power supply at scheduled intervals to prevent or minimize equipment deterioration.

WARNING

Line voltage of 240 VAC exposed when covers are removed from the power supply . Use extreme caution when working inside the power supply. Heed all warning labels.

Use caution when manipulating metal tools or probes near exposed conductors and terminals. Extra care should be exercised to prevent the possibility of shorting the output lines of the battery pack.

WARNING

Serious injury may occur if the following precautions are not observed:

While the input power is connected, use caution when working inside the power supply. Many exposed components and conductors carry low level DC voltages which are capable of supplying heavy currents if short-circuited, resulting in high heat and the possibility of painful burns. Use caution when manipulating metal tools or probes. Wrist watches, metal necklaces, bracelets, or rings must not be worn. Avoid dropping tools, screws or other metal objects onto conductors or PCAs. Remove power and recover dropped objects at once; if forgotten damage could result later.

If feasible, before performing any work inside the power supply turn off system power switch and unplug the AC power cord and wait about four minutes to allow all filter capacitors to discharge.

9-28. Preventive Maintenance

The power supply preventive maintenance consists of measuring the DC voltages at the test jacks on the power supply front panel and performing the battery test procedure.

Perform the preventive maintenance procedure as follows:

a. Remove dust

b. Check cooling fans operation

c. Check proper seating of all connectors

d. Check the DC operating voltages at the power supply front panel.

To gain access to the first power supply, open the rear door of the electrical mainframe cabinet bay. The power supply is on slide-out rails for ease of access by removing the four retaining screws, the power supply may be extended on its rails. In this position, the power supply top can be removed for maintenance and testing.

In those systems containing both card cages, the second power supply is located behind the front door of the electrical mainframe. This power supply is mounted on sliding rails, however the unit can be removed and set on the floor in front of the system.

While the power supply is ON, check the cooling fans for proper operation. Ensure that no objects interfere with fan blade rotation.

If required, use a vacuum cleaner to remove dust from the power supply. Loosen encrusted dust with a soft bristled brush. With the top cover of the power supply removed, check all connectors on the PCA's for proper seating.

9-29. Voltage Checks

Measure the six voltages listed in table 9-4 using a digital voltmeter. If any voltage is out of tolerance, make the necessary corrective action as described in the following paragraphs.

Perform the voltage checks as follows:

a. Stop any computer programs.

b. Measure the six DC voltages listed in table 9-4. These voltages are available for measurement at the test jacks mounted on the power supply front panel.

c. Set the oscilloscope for checking AC voltage. Check each of the six voltages listed in table 9-4 for ripple, for each voltage the indicated ripple should be less than that listed. If any voltage is not within specified limits make the necessary repairs.

Table 9-4. DC Output Voltages

Voltage Test Jacks	Min. Reading	Max. Reading	Ripple Voltage
+5 Volts	+4.9	+5.1	0.05 V p.p.
+12 Volts	+11.8	+12.2	0.075V p.p.
-12 Volts	-12.2	-11.8	0.075V p.p.
+5M Volts	+5.0	+5.2	
+12M Volts	+11.86	+12.34	
-12M Volts	-13.8	-10.2	
BATT	+16.45 volts		
PON	approx. +5.0 volts		

9-30. Memory Power Supply Adjustments

There are three adjustments for service purposes. One adjustment is on the memory preregulator PCA , and two are on the memory Regulator PCA . These adjustments are accessible by removing the top cover of the power supply unit.

9-31. Preregulator Adjustment. The +16.45 volt (BATT) supply voltage output is controlled by the memory preregulator adjustment potentiometer R13. (See figure 9-10.) The BATT level will vary with charge rate and temperature. However, when the battery is fully charged and stabilized at room temperature, the voltage is approximately +16.45 volts. Check and adjust the battery voltage as follows:

a. Set the power supply switch to ON and set the processor switch to ON.

b. Connect the voltmeter between the common terminal test point (on the front panel) and the BATT TEST jack. While observing the voltmeter, adjust VOUT potentiometer R10 until the battery level is approximately +16.45 volts.

c. Proceed with the regulator adjustment procedure.

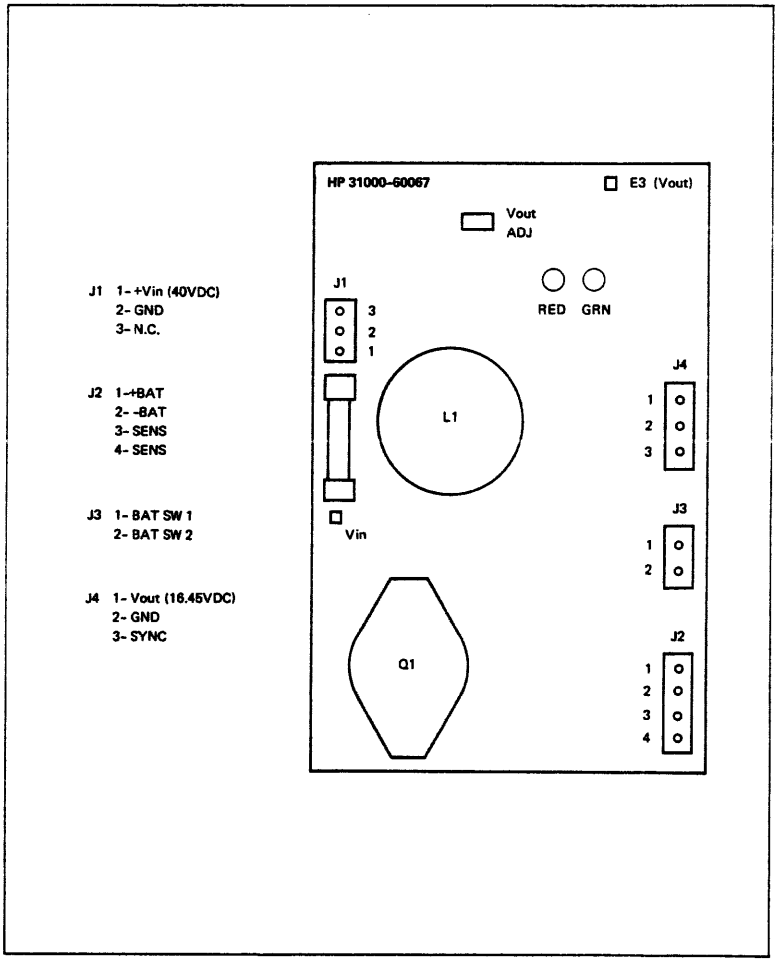

Figure 9-10. Memory Preregulator PCA

9-32. Regulator Adjustments. The +5M, +12M, -12M supply outputs are controlled by the memory regulator adjustment potentiometers R27 (+5M ADJ) and R17 (+12M, -12M ADJ) which are located on the regulator PCA. (See figure 9-11.) If one or more of these voltages are not within specified tolerances (given in table 9-4), adjust the regulator as follows:

a. Set the power supply switch to ON and the processor switch to ON.

b. Connect the voltmeter between the common terminal test point on the power supply front panel and the +5M TEST jack. While observing the voltmeter, adjust the +5M ADJ potentiometer until the voltage measures +5.1 volts.

c. Using the same common point as the return, connect the other lead to the +12M TEST jack. While observing the voltmeter, adjust +12M ADJ potentiometer until the output is +12.1 volts.

d. Connect the positive lead to the -12M TEST jack and verify that the output voltage is within limits as specified in table 9-4.

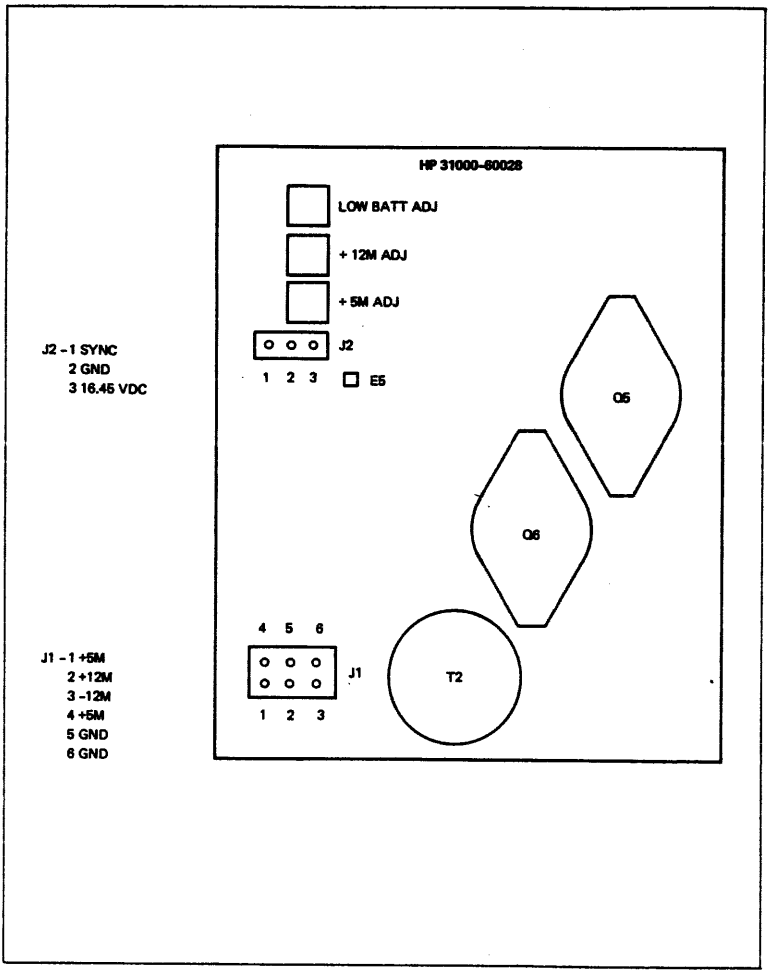

Figure 9-11. Memory Regulator PCA

9-33. Main Power Supply Adjustments (63909F)

The following adjustments should be performed only after replacing the main power supply that is within the power supply unit. Since the output voltage levels are self-sensing, further adjustments are unnecessary.

The +5, +12, -12 volt supply outputs are adjusted by potentiometers that are accessible through the power supply back panel. Adjust the voltages as follows:

a. Set the power supply switch to ON and the processor switch to ON.

b. Connect the voltmeter between the common test point on the power supply front panel and the +5V test jack. While observing the voltmeter, adjust the +5V ADJ potentiometer (shown in figure 9-5) until the voltage measures within the limits specified in table 9-4.

c. Using the same common as a return, connect the positive lead of the voltmeter to the +12V TEST jack. While observing the voltmeter, adjust the +12V ADJ potentiometer (shown in figure 9-5) until the voltage is within the limits specified in table 9-4.

d. Using the same common as a return, connect the voltmeter to the -12V TEST jack and verify that the output is within the limits specified in table 9-4.

e. Set the power supply switch to OFF and disconnect the voltmeter.

9-34. Power Control PCA Adjustment

The low line detector adjustment is located on this PCA. To adjust the low line detector, proceed as follows:

a. Rotate potentiometer R56 fully counterclockwise. (See figure 9-12.)

b. With a jumper, connect Test point E2 to ground.

c. Rotate potentiometer R56 clockwise until a system power fail occurs. The PFW LED will light at this point.

d. Remove the jumper from test point E2. The power fail setting will cause a power fail to occur at an input voltage of approximately 180 volts RMS.

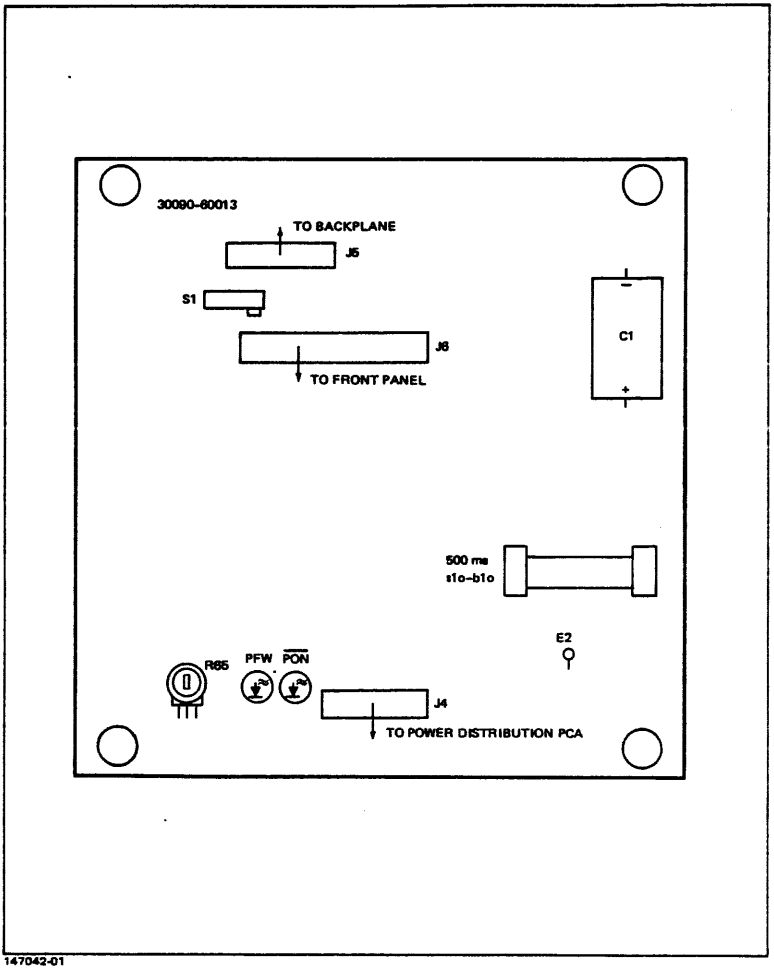

Figure 9-12. Power Control PCA.

9-35. Battery Test

The battery test certifies that the backup capability of the memory power supply is functioning normally. The system should be halted before performing this test, then proceed as follows:

a. Extend the 30090-60035 power supply unit and remove the top panel.

b. On the power control module, set the main breaker to OFF.

c. The discharge indicator (red) on the memory preregulator PCA should light and the +12M LED (yellow) on the card cage backplane should have stayed lighted.

d. Allow approximately four minutes of discharge time.

e. On the power control module, set the main breaker to the ON.

f. The charge indicator (green) on the memory preregulator PCA should light.

9-36. Troubleshooting

Power supply operation is monitored at the system control panel. When a failure occurs, observe the LED's for either the main or extend power supply and proceed with troubleshooting the failure mode indicated by the status of the LED's. Some common failure modes associated with the power supply unit are:

Mode One: The main power supply output level is low or zero (+12V LED located on card-cage backplane is off). The power supply voltages should first be measured at the test points provided on the power supply front panel. There are three different possible conditions which can cause this failure, as follows:

a. System PCA Overloading. Turn system power off and pull all PCAs from the affected card cage except the CPU processor PCA (for proper operation a small load must be maintained on the main power supply). Turn system power on and check voltages. If the voltage recovers, one of the removed PCAs is causing the overload, or the main power supply is incapable of providing the needed load current. Reinstall the PCAs, one at a time, and note voltages. However, if the power supply is still not functioning after removing all PCAs it may indicate that either the CPU processor PCA, or that the power supply is defective.

b. Main Power Output Sags. If the voltage levels sag (drops to 0.1 volt) each time some new component is added, the power supply should be changed.

c. Main Power Supply Output Zero. Power supply defective.

Mode Two: The memory power supply level is low or zero (+12M LED located on card-cage backplane is off). This problem can be caused by one of three conditions:

a. Memory P/S Overload. Turn system power off (including battery power) and remove all memory array PCAs from effected card cage. Then on the card cage backplane place the memory load switch to the NO MEM position and turn power back on. At this time the voltage levels of the memory power supply do not respond normally (allowing 10 seconds after power on) the trouble may be within the power supply unit (memory power supply).

   If the memory supply did respond properly (output levels within ranges), this indicates a PCA caused the overload. Start reinstalling, one at a time, (power off and on each time) each PCA to see which is causing overload.

NOTE

After reinstalling first PCA the memory load switch located on backplane should be switched to MEM position.

b. The output of the preregulator should be within the specified limits of +16.45 volts to +14.30 volts at 23 degrees C. If the output voltage is considerably below that range (example +10 volts), the possible causes are a) defective preregulator PCA, b) battery temperature sense thermister, c) Battery pack.

c. If output of Preregulator is within specified limits and output voltages of memory power supply are still outside adjustable limits the memory regulator should be replaced.

SECTION X

HP 3000 SERIES 40 SUPPLEMENT

10-1. INTRODUCTION

This section describes the HP 3000 Series 40 Computer System. The Series 40 is functionally the same as the Series 44, with the chief difference being that the Series 40 is housed in a smaller cabinet than the Series 44. This restricts the Series 40 to fewer PCA's than that for the Series 44, thereby reducing the I/O and memory capacity. Also, the power supply is modified somewhat from that in the Series 44. This section explains only that which is different from the Series 44. Where functions are the same in both systems, references are made to the appropriate sections for descriptive information.

10-2. GENERAL SPECIFICATIONS

These models are the processing unit for the HP 3000 Series 40 Computer System. The processing unit is designed to use most of the available PCA set that is used in the Series 44 and the main-frame design is that of the Series 30. It operates with IMB version of the MPE IV operating system. The standard configuration of the processing unit includes the following:

A CPU set which consists of the CTL, ALU, and the PCS (which includes microcode extensions for COBOL, decimal, and four-word Floating Point).

One CMP

Up to four 256 kbytes memory arrays; up to two 1 Mbytes memory arrays

Two General I/O Channels (GIC)

One Asynchronous Data Communications Channel-Main (ADCC-M) ordered separately

10.3. Processor Specifications

Word Length	16 bits
Number of Instructions	195
Microinstruction Cycle Time	105 ns
Physical Address Space	16 Mbytes
Maximum Code Segment Size	16 kwords
Maximum Data Segment Size	32 kwords
Maximum Number of User Code Segments	63
Maximum Number of User Data Segments	256
Decimal Precision	28 digits
Real-Time Clock Resolution	1 ms

10-4. Memory Specifications

Word Length	32 data bits plus 7 error detections and correction bits
Error Detection	2 bits per 39-bit word
Error Correction	1 bit per 39-bit word
Memory Array Module Size	256 kbyte (16k RAM) 1 Mbyte (64k RAM)
Maximum Number of Memory Array Modules	4-256 kbytes; 2-1 Mbytes
Read Access Time	300 ns (ADO to DDN)
Cycle Time - Read/Write	417/543 ns
Minimum Battery Backup Time	30 minutes @ 20-30 deg C

10-5. I/O Specifications

Maximum No. of I/O slots	13

General I/O Channel (GIC) Specifications:

Maximum No. of GIC's per System	4
Maximum No. of Device Loads per GIC	8
Maximum Data Transfer Rate	980 kbytes/s
Maximum Cable Length per GIC	7 m plus 1 m/device load (includes all internal cabling.)

Asynchronous Data Communication Channel (ADCC) Specifications:

RS-232-C Ports per Channel	8 (4 on ADCC Main and 4 on ADCC Extend)
Maximum Number of Ports per System	32 (uses 8 I/O slots)
Data Transfer Rates	50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600 Baud
Maximum RS-232-C Cable Length per Port	30 m

10-5. SYSTEM CONTROL PANEL

The system control panel mounts within the bezel at the top of the processor cabinet. The left half of the panel contains the system nameplate and the POWER and REMOTE LED's exposed through the nameplate. The right half of the panel (figure 10-1) contains the remaining controls and indicators, and is concealed behind an unlockable door. Desired security levels are selected with a key-operated switch.

The system control panel is intended for use by both the customer and HP customer engineer. The key-operated switch selects the degree of security desired for the panel and the system console.

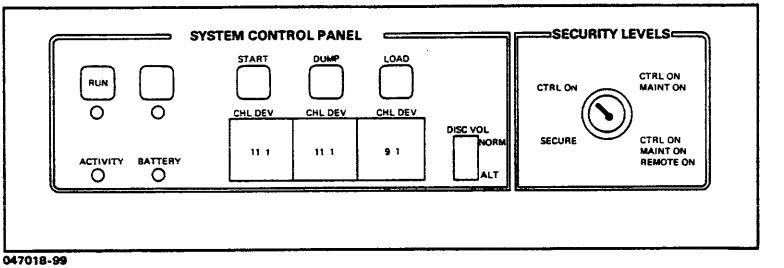

Figure 10-1. System Control Panel

10-6. Panel Controls

The panel controls perform the functions as described in the following:

- RUN
  This is a momentary switch that causes the CPU to enter the run state from a halt state. There is no response when the CPU is already in the run state.

- HALT
  This is a momentary switch that causes the CPU to halt. When the CPU is already halted, no response is given.

- LOAD, START, and DUMP
  These are momentary switches that gate the selected channel and device numbers out on the channel and device lines to the CPU.

- CHANNEL and DEVICE
  Three sets of thumbwheel switches are associated with the load, start, and dump functions. The switches select the channel and device numbers for each function. The number wheel for each channel switch is marked 4 through 11. The corresponding BCD levels sent to the CPU will be 0 through 7. The CPU adds four to the channel number so that the result will be the same as the switch marking. The device number switches are marked 0 through 7 and their corresponding outputs are 0 through 7.

- DISC VOL(Volume)
  This switch selects the normal or alternate disc. For all currently supported discs, the switch should be in the NORM position. ALT selects Volume 1.

10-3. Panel Indicators

The panel indicators are described as follows:

- POWER
  This is a yellow LED which is driven by a signal derived from the PON signal. This indicates that the power supplies are on and AC line is up. The indicator is located in the nameplate.

- REMOTE CONSOLE
  This is a yellow LED that is lit when the security switch is set to enable the use of a remote console. It is located in the nameplate.

- RUN
  This a yellow LED that is lit when the CPU is in the run state.

- HALT
  This a red LED that lights when the CPU is halted.

- ACTIVITY
  This is a yellow LED that lights when the ADO signal from the CPU is active. It provides a visual indication of CPU activity.

- BATTERY
  This is a red LED that lights when a power failure occurs and memory is being sustained by the backup battery.

10-7. Security Switch

The security switch is key-operated and provides four levels of security. Table 10-1 shows which functions are enabled in each position of the security switch.

Table 10-1. Security Switch Functions

Security Switch Position	Panel and Console Functions								
	START	DUMP	RUN	LOAD	HALT	IOMAP	SELF TEST	DISPLAY	REMOTE ENABLE
SECURE	-	-	-	-	-	-	-	-	-
CRTL ON	X	X	X	X	X	X	X	-	-
CTRL ON MAINT ON	X	X	X	X	X	X	X	X	-
CTRL ON MAINT ON REMOTE ON	X	X	X	X	X	X	X	X	X

"X" indicates that function is enabled.

10-8. SYSTEM OVERVIEW

The functional operation of the Series 40 is the same as that for the Series 44. Refer to Section III of this manual for a description of the Series 44.

10-9. CENTRAL PROCESSOR UNIT

The Series 40 Central Processor Unit (CPU) is the same as that for the Series 44. Refer to Section III of this manual for a description of Series 44.

10-10. CONTROL AND MAINTENANCE PROCESSOR

The Series 40 uses the same control and maintenance processor (CMP) as that used in the Series 44. Refer to Section V for a description of the CMP.

10-11. MEMORY SUBSYSTEM

The memory and associated controller in the Series 40 is the same as that used in the Series 44. The only difference is that the Series 40 can have only one controller and up to four 256 kbytes memory arrays or two 1 Mbytes memory arrays. Refer to Section VI for a description of the memory subsystem.

10-12. I/O SYSTEM

The I/O system in the Series 40 is the same as in the Series 44. Refer to Section VII for a description of the I/O system. Channel limitations for the Series 40 are given in paragraph 10-5 of this section describing I/O specifications.

10-13. ASYNCHRONOUS DATA COMMUNICATION CHANNEL

The asynchronous data communication channel (ADCC) used in the Series 40 is the same as that used in the Series 44. Refer to Section VIII for a description of the ADCC.

10-14. CONFIGURATION INFORMATION

10-15. Card Cage Configuration Rules

The following rules apply to all Series 40 systems:

1. The first memory array PCA must be installed in slot 1 and the memory controller in slot 5 to prevent the memory front-plane cable from hanging free.

2. The CMP is installed in slot 6, and the PCS, ALU, and CTL PCA's are installed in slots 7, 9, and 11, respectively, to provide for adequate cooling. No PCA's are to be installed in slots, 8, 10, 12. The ALU and CTL PCA's must be positioned adjacent to one another to allow installation of the front-plane flat cable.

3. The first ADCC MAIN must be installed in slot 13 so that it can be reached by the CMP cable. Slot 14 is reserved for ADCC-Extend.

4. The ADCC MAIN and ADCC EXTEND PCA's must be installed in adjacent slots to allow interconnection.

5. The first GIC must be installed. (such as another GIC) is installed in the higher priority slot 15.

6. Internal HP-IB devices such as INP's or printer interfaces must be installed adjacent to their controlling GIC. This allows the internal HP-IB flat cable to connect to these PCA's without passing over other PCA's.

7. The GIC used for the system disc(s) may also be used for internal devices only. Additional external HP-IB devices, such as printers, must be connected to a separate GIC to avoid compromising the total system ESD susceptibiliy.

10-16. Sample Card-Cage Configuration

The following provides a sample card cage configuration for the Series 40:

Slot No.	PCA
1	Memory Array (0-256 kbytes) or (0-1 Mbytes)
2	Memory Array (256-512 kbytes) or (1-2 Mbytes)
3	Memory Array (512-768 kbytes)
4	Memory Array (768-1024 kbytes)
5	Memory Controller
6	CMP
7	PCS
8	(empty)
9	ALU
10	(empty)
11	CTL
12	(empty)
13	ADCC-Main (CH 1)
14	ADCC-Extend
15	GIC (CH 11) to disc controllers (2 max.) and to internal peripherals
16	INP
17	INP
18	GIC (CH 9) to magnetic tape (1 master and 3 slaves)
19	GIC (CH 10) to 2nd magnetic tape or external peripherals
20	Printer Interface
21	ADCC-Main (CH 2)
22	ADCC-Extend
23	ADCC-Main (CH 3)
24	ADCC-Extend
25	ADCC-Main (CH 4) or GIC (CH 13) to HP 2680A Printer

10-17. INPUT AC POWER

The power supply unit is capable of operating at one of four primary voltages. These values, with operating tolerances and voltage limits are as follows:

Nominal Voltage	Specified Tolerance	Voltage (RMS) Limits Upper	Lower
100*	+8%, -10%	108	90
120	+5%, -10%	126	108
220	+5%, -10%	231	198
240	+4%, -10%	250	216

* Requires hardware modification to Power Control PCA.

The input voltage range is selected by three toggle switches on the top front of the unit, which are labeled as shown below:

Switch	S1	S2	S3
Position 1	100/220	220/240	220/240
Position 2	120/240	100/120	100/120

CAUTION

Switches S2 and S3 must be in the same position or serious circuit failure may occur.

Fuse F1 is a 3-ampere slow-blow and fuse F2 is a 15-ampere normal-blow which are used for the 100/120-VAC rages. (See figure 10-2.) When the 220/240-VAC ranges are used, Fuse F1 must be changed to a 1.5-ampere slow-blow, and fuse F2 must be an 8-ampere normal-blow.

10-18. Line Current and Power

The input line current and power for each of the voltage ranges are given as follows:

Voltage (VAC)	Current (RMS) (amperes)	VA (E x I)	Power (watts)
100	9.65	965	810
120	8.15	980	810
220	4.45	978	775
240	4.10	983	775

10-19. Turn-on Inrush Current

At turn-on, the maximum peak inrush current is 100 amperes, decaying to 20 amperes with a time constant of less than 50 milliseconds.

10-20. Input Primary Circuit Functional Description

Primary AC input power enters the power unit at the power receptacle on the rear of the unit and connects to the line filter PCA. (See figure 10-2.) Power then connects from the line filter to rotary POWER ON/OFF switch S4. The line and neutral wires connect through the switch. From the switch, the AC line connects through fuse F2 to the 63909F power supply and to the pimary of transformer T1 through fuse F1.

The voltage range to the 63909F main power supply is selected by switch S2. In the 100/120-volt position, terminals E1 and E2 on the main power supply are connected together. Continuity should be checked to verify correct switch wiring. With switch S2 in the 100/120-volt position, E2 will show connection to to E1, and E3 is open. When switch S2 is in the 220/240-volt position, E1 will be open and E3 will be connected to E2.

CAUTION

Remove any straps that may exist on the main power supply terminal block to prevent damage to the power supply.

The voltage ranges for transformer T1 are selected by switch S3 which connects the primary windings in parallel for 100/120-volt operation, or in series for 220/240-volt operation. Switch S1 connects the line to a lower tap on one of the primary windings to step up secondary voltage slightly for 100- and 220-volt inputs. Fuse F1 protects the transformer from short circuits in the secondary winding.

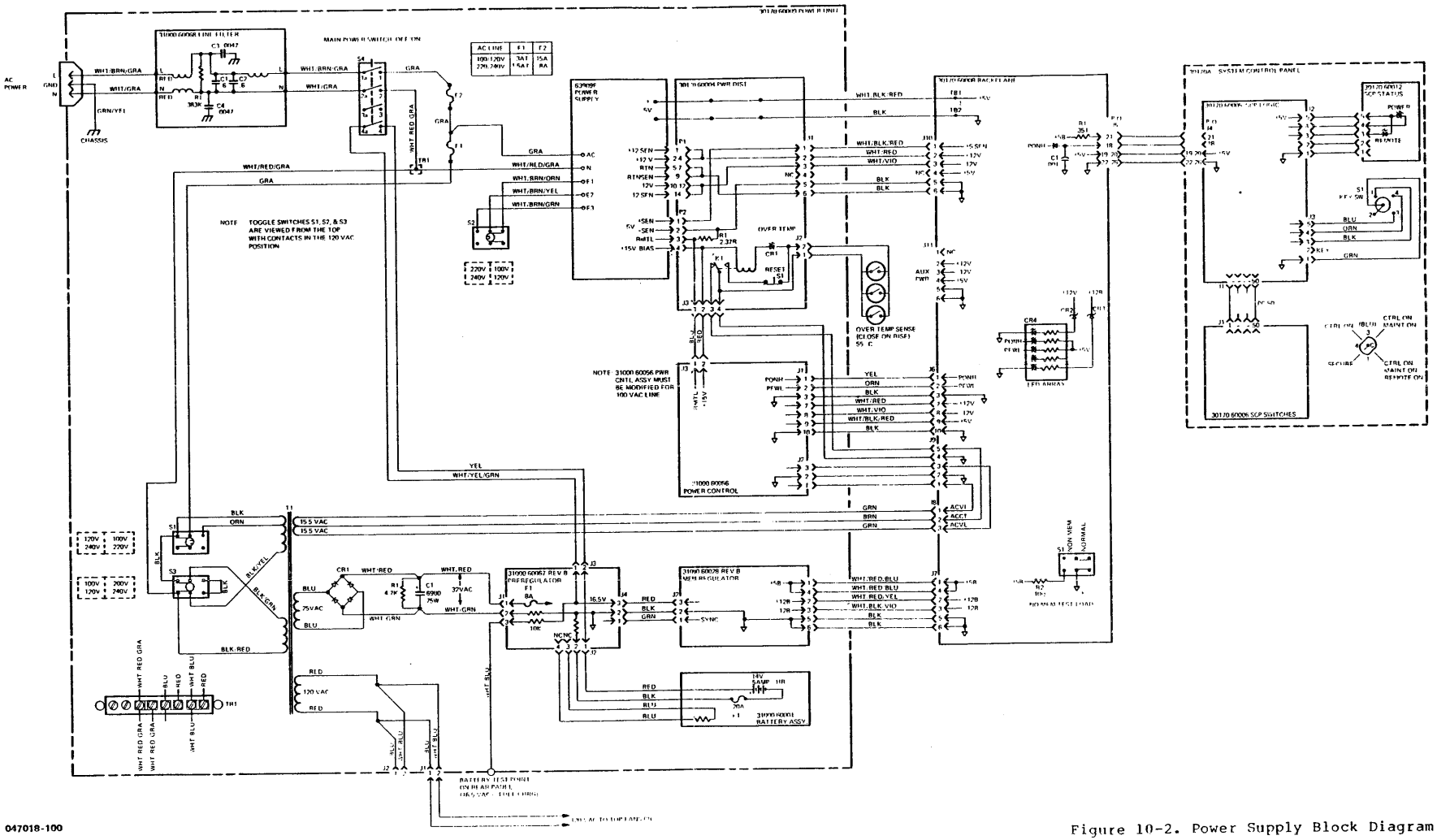

Figure 10-2. Power Supply Block Diagram

10-21. POWER SUPPLY UNIT

The power supply unit (part no. 30170-60009) contains the 63909F main power supply, and the memory supply with battery backup. The unit provides DC power to the processor backplane. The main power supply provides +5 V, +12V, and -12V. The 60-watt memory supply, with battery backup, provides the memory voltages +5M, +12M, and -12M.

10-22. Main Power Supply

The 63909F main power supply is a switching-regulator type supply, providing three different DC voltage outputs to the processor. These voltages are +5 volts, +12 volts, and -12 volts. The maximum currents available from each of the output voltages are 85A, 5A, and 5A, respectively. The total output power limitation is 545 watts over the temperature range of 0 to 40 degrees C. Remote voltage sensing is used for all outputs to the processor backplane. The remote sensing of all three output voltages is necessary in order to maintain good voltage regulation at the load by reducing the degredation that would occur due to the voltage drop in the cables between the power supply and the backplane.

10-23. Protection Features

Current limits are on the +5-volt, +12-volt, and -12-volt outputs to protect the power supply. Undervoltage and overvoltage detectors on the regulated outputs shut down the supply in case of an output fault or improper voltage setting. To restart from a shutdown, the input AC voltage must be cycled off and then on.

10-24. Voltage Adjustments

Voltages are adjusted by the power supply front panel controls. A load is unnecessary to adjust the voltages. The +5 volts is adjusted by the Vi VOLTAGE ADJ potentiometer. The +12 volts and -12 volts are adjusted by the V2,V3 VOLTAGES ADJ potentiometer. The +12-volt output is slaved to the -12-volt output; therefore, adjust the +12-volt output to exactly +12.0 volts. The -12-volt output should be within +/-0.25 volt of its nominal value.

10-25. MEMORY SUPPLY

The memory supply consists of the Memory Preregulator PCA, a 14-volt, 7-cell, lead-acid battery pack, and a Memory Regulator PCA. Input power is received from the 25 VAC winding on transformer T1. This voltage is full-wave rectifer and filtered to produce 32 VDC input to the Preregulator at the nominal rated line voltage. The output voltages are listed below:

Voltage (VDC)	Voltage Range (VDC)	Ripple (mV p-p)
+5M	+4.95 to +5.15	100
+12M	+11.9 to +12.1	100
-12M	Unregulated	150

During normal operation, the memory voltages are supplied by the Memory Preregulator and Memory Regulator PCA's. Battery backup sustains these voltages during power line failures.

10-26. Memory Preregulator

The Memory Preregulator assembly is a switching regulator that operates in the current source mode to charge the battery at approximately 600 mA maximum and provide power to the Memory Regulator. The Preregulaor output voltage is determined by the state of the charge and temperature of the battery. A thermistor in contact with the battery monitors battery temperature and adjusts the output of the preregulator. When the battery reaches full charge at any given temperature, the voltage limit mode dominates , and the charge current is reduced to a very low level.

10-27. Battery Pack

The battery pack is a 14-volt, 7-cell, lead-acid battery. Maximum charge time for a discharged battery is 24 hours. If a power interruption occurs, the battery (when fully charged) will sustain memory voltages for the following times:

One 256 kByte Memory Array - - 0.5+ hours
Two 256 kByte Memory Arrays - 0.5+ hours
Four 256 kByte Memory Arrays - 0.5 hour

10-28. Memory Regulator

The memory regulator has a series regulator for the +12M output and a switching regulator for the +5M and -12M outputs. Operation of the regulator is the same whether the input power is obtained from the battery pack or from the preregulator. Also, the regulator contains circuitry for overvoltage and undervoltage sensing, overcurrent protection, and voltage sequencing for the memory supply. The memory regulator is connected to the positive battery terminal and ground, therefore, it sees the same voltage as the battery charge voltage from the memory preregulator.

Battery cutoff circuitry on the memory regulator is used to sense battery voltage and shut the memory supply down when the battery reaches the minimum allowable discharge level of +12.5 volts. During standby operation from the battery, the battery voltage is sensed and if it falls below +12.5 volts, the memory regulator is shut down. This is necessary to prevent deep discharge damage to the battery. If the battery is fully charged to +12.5 volts, it takes a maximum of 16 hours to recharge. The system can operate normally if the AC input line voltage is at the rated level even though the battery may be discharged.

In the memory regulator circuitry, there is approximately 2 volts of hystersis between the charge and discharge voltage levels of the battery. When power fails, the memory preregulator no longer powers the memory regulator, and power is obtained from the battery. When the battery voltage decreases to +12.5 volts, the memory supply is turned off. With the memory supply turned off, the battery will recover, partly rising to less than +14 volts. Several ON-OFF cycles of the Discharge and Charge LED's may occur before the battery is fully discharged. The memory supply will remain off until the AC line voltage is applied and the battery voltage rises above the upper hysteresis limit of +14 volts.

10-29. Memory Power Supply Voltage Sequencing

The memory supply contains circuitry that is designed to bring up the +5M and -12M voltages before the +12M. The +12M is held at zero volt until the -12M supply exceeds approximately -9 volts. This prevents damage to the RAM chips.

10-30. Memory Power Supply Switch

The positive output voltages of the preregulator and battery is switched by the fourth section of the main power switch so that the battery is disconnected when the systen power is switched off. This section of the main power switch is used only as a switch, therefore, it will not trip if a high current overload occurs. The battery maintains the input voltage to the memory regulator only when the switch is on and the input line voltage is below the required minimum.

NOTE

If the computer system is turned off from a wall panel circuit breaker in the main input power line, the battery will continue to power the memory until it is discharged. The system must be turned on and off with the processor's main power switch. Continued discharge of the battery reduces battery life.

10-31. POWER CONTROL

10-32. General Description

The power control PCA disables system operation when the input AC line voltage is too low, and shuts down the main power supply if a DC undervoltage fault occurs.

Two signals are connected to the backplane which provide power status information to the system. These are high true Power On (PONH) and low-true Power Fail Warning (PFWL). When PONH is low, it is used by the system for hardware reset and initialization. When true, PONH indicates that the power is in the normal operating range and the power supply voltages are up. PWFL is a power status signal that alerts the system of an impending power failure before the output voltages actually go down. The CPU uses this signal to initiate an orderly system shut-down. Figure 10-3 depicts the timing sequence of these signals.

The remote disable signal RMTL from the power control to the main power supply is asserted low to shut off all DC outputs if the AC line is too low or if a DC output undervoltage fault occurs on +5V, +12V, or -12V.

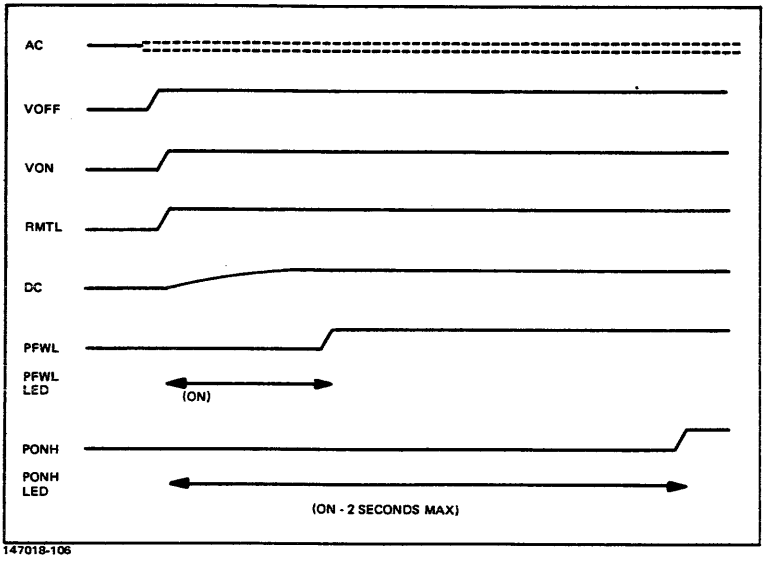

Figure 10-3. Power And System Turn-on Sequence

10-33. Operation

The AC low-line detector has two Scmitt triggers that detect the peaks of the line voltage waveform. These trigger on each half-cycle of the waveform and are referred to as VON and VOFF. VON triggers at 90 percent of peak voltage to turn the system on, and VOFF triggers at approximately 85 percent. Input levels that fail to trigger VOFF cause the system to be turned off. The 5 percent difference between VON and VOFF provides hysteresis between the turn-on and turn-off levels.

The hysteresis provided by the two low-line detector levels is needed to prevent a turn-off-turn-on type of oscillating condition. When PONH goes low as in a partial AC power failure, the system is turned off. This turn-off condition reduces the load on the main power supply at the time it being turned off, and subsequently allows the line voltage to rise slightly. If there was only one low-line detection level, this rise would be enough for an attempted system restart and later drop again from system loading. An oscillating condition of attempted restarts and power fail shutdowns would result.

At inital turn-on the two signals to the system (PFWL and PONH) are low, and the disable signal RMTL to the main power supply is low true. Thus, the DC outputs are initially disabled until the AC line voltage is up to more than 90 percent of its rated value, which triggers VON. Then the main power supply is enabled by the releasing of the RMTL signal to the high state. If the line voltage remains above the VON level with the added load of the main power supply on, PFWL goes high, and about 2 seconds later, PONH goes high, allowing system operation to begin.

Continuous normal operation is allowed as long as the input AC line voltage remains above the lower low-line detector level VOFF. If the line drops below VOFF for 27 ms or longer, PFWL is asserted low, and a minimum of 2 ms later PONH also goes low to indicate to the system that the DC voltages may be going down. The AC line voltage must return to above the higher level of VON to restart system operation. If the line voltage remains below the VOFF level for about 37 ms or longer, the main power supply is disabled by the RMTL going low. The line voltage must return to above VON for the main power supply to be turned on. Figure 10-4 depicts the power fail and turn-on sequence.

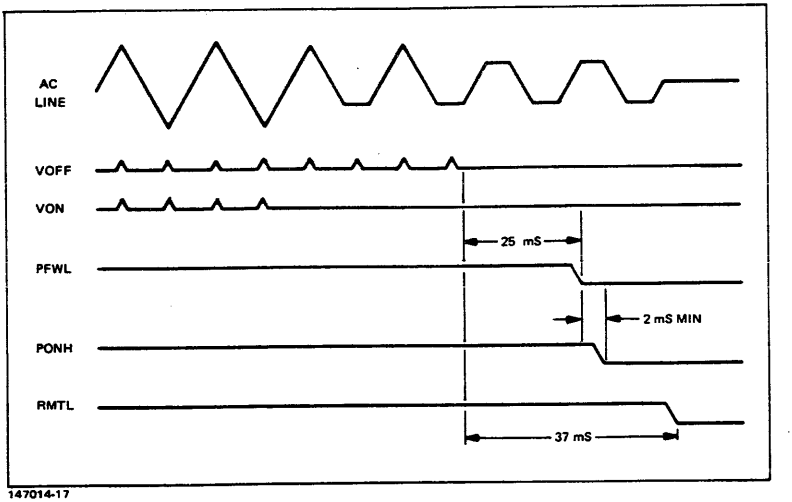

Figure 10-4. AC Power Failure Sequence

10-34. PROTECTION CIRCUITRY AND SWITCH RESETS

10-35. Replaceable Fuses

The following is a list of replaceable fuses in the power supply:

Fuse	Location	Rating
F1	Adjacent to three toggle switches on top-front of power supply.	3A slo-blo for 100/120 VAC; 1.5A slo-blo for 220/240 VAC
F2		15A normal-blo for 100/120 VAC; 8A normal-blo for 220/240 VAC
F1	Memory Preregulator PCA	8A normal-blo
F1	Inside battery pack	20A normal-blo

10-36. Protection Circuitry

Table 10-2 lists the protection circuits and the required reset for a particular type of system fault.

Table 10-2. Protection Circuitry Summary

Supply Measured	Device Pro-tected	Type of Protection (location)	Protection Circuitry	Type of Reset Required
AC Input Current	System Main-frame	Main Ckt Bkr (frnt pnl of mainframe)	Trips at I > 12A for 100/120 or I > 6A for 220/240	Turn Ckt Bkr on.
AC Input Current	Xfmr T1	Fuse F1 (Beside S1, S2, S3)	3A slo-blow for 100/120; 1.5A slo-blow for 220/240. Blows before Ckt Bkr trips.	Replace Fuse
AC input Under-voltage	Main Power Supply	Low Voltage Detectors (Power Cntrl PCA)	Shuts off Power Supply when AC input is less than required minimum	None. When AC input > low limit, system turns on.
+5 +12 -12 -40 Current	Power Supply	Internal fuses (Inside Power Supply)	Shuts off Power Supply	Replace Power Supply
+5 +12 -12 Current	Power Supply	Current Overload in system (inside Power Supply)	Power Supply is shut off if excessive current load on +5, +12, or -12	Turn off Ckt Bkr; no wait required; turn on. Ckt Bkr.
+5 +12 -12 Over-voltage	Power Supply	Crowbar-Overload (inside Power Supply)	Output voltages clamped to zero if any exceeds high limit.	Turn off Ckt Bkr; wait 15 seconds; turn on Ckt. Bkr.

Table 10-2. Protection Circuitry Summary (Continued)

Supply Measured	Device Protected	Type of Protection (location)	Protection Circuitry	Type of Reset Required
Power Supply Over-Temp	Power Supply	Temperature thermosat (inside Power Supply)	Turns off all outputs from Power Supply if there is heat overload.	Self-restoring if heat overload corrected
+12 Current	Power Supply	Fuse F1 (Power Dist. PCA)	5A normal-blow protects +12 on backplane.	Replace fuse
-12 Current	Power Supply	Fuse F2 (Power Dist. PCA)	5A normal-blow protects -12 on backplane.	Replace fuse
-40 Current	Power Supply	Fuse F3 (Power Dist. PCA)	3/4A normal-blow protects -40	Replace fuse
Memory Prereg. output voltage	Memory Prereg. PCA	Fuse F1 (Memory Prereg. PCA)	8A normal-blow Memory Prereg. output voltage >19 volts causes fuse to blow.	Replace fuse
+5M +12M Over-voltage	Memory Power Supply	Crowbar-overvoltage (Memory Regulator PCA) Note; -12M is Not sensed.	All Memory output voltages clamped to zero if output voltage exceeds high limit.	Turn off Ckt Bkr: wait 15 seconds; turn on Ckt Bkr.

Table 10-2. Protection Circuitry Summary (Continued)

Supply Measured	Device Protected	Type of Protection (location)	Protection Circuitry	Type of Reset Required
+5M +12M -12M Current	Memory Power Supply	Crowbar-current overload (Memory Regulator PCA)	All Memory output voltages clamped to zero if output current exceeds high limit.	Turn off Ckt Bkr; wait 15 seconds; turn on Ckt Bkr.
Battery Voltage Discharge	Battery Pack	Cutoff circuitry (Memory Regulator PCA)	All Memory output voltages reduces to zero if battery pack voltage drops below +12.5 volts.	Recharge battery
Battery Voltage No-voltage	Battery Pack	Fuse F1 (inside battery Pack)	20A normal-blow protects battery for shorts or overload.	Replace fuse

10-37. SERVICE

10-38. Test Lights

10-39. Charge/Discharge Indicators. Two LED's are incorporated on the memory pregulator PCA to indicate proper operation of the charge circuitry or warn of the memory backup battery discharging into the load. These indicators are visible through the bottom empty slot to the left of slot 1.
The green LED indicates charging current and is brightest when charging current is maximum, and dims as the battery reaches full charge.

The red LED indicates that the battery is discharging and supplying current to the load. Also, if fuse F1 (next to the voltage select switches) or fuse F1 on the memory preregulator PCA blows, or any other condition occurs where the battery is discharging, this LED will light.

Both LED's are off during normal operation with a fully charged battery.

10-40. Backplane LED's. There are five LED's mounted on the lower left of the backplane and are visible from the rear of the the mainframe. The +12 and +12M LED's are the only indicators for the DC voltages on the power supply unit. The following shows the function of each of the five LED's for normal conditions during startup, operation, and shutdown (the LED's are listed in the order of physical location):

Name	Startup	Operation	Shutdown
+12	1	1	X
PFWL	*	0	*
PONH	*	0	*
not used	0	0	0
+12M	1	1	X

1 = on
0 = off
* = momentarily on then turns off
X = on then off

The PFWL and PONH LED's turn on momentarily and then go off when the system power is turned on, and the system initialization and operation are normal. If PONH remains on after power is turned on, the system did not initialize properly. If system AC power input goes below the acceptable input value (low-line), both LED's will turn on until the system is automatically turned off by the low-line detectors on the power control PCA. The LED's will then turn off.

10-41. Self-Test

Forcing a PFW-PON cycle tests the system software shutdown. To force a PFW-PON without turning off the entire system, test pad 7 on the power control PCA may be momentarily grounded. This action affects only the Power Fail Warning circuitry just as a very short duration (half cycle) power failure would.

10-42. Low-Line Detector Test and Adjustment

NOTE

If switches S1, S2, and S3 are set for 100 VAC, measure the input voltage before proceeding. The value should be within one percent of the specified voltage set by the switches. If not, a Variac must be used on the input line voltages to obtain 100 VAC to prevent the low-line threshold from being set lower than the required minimum input voltage. For the 100 VAC setting, check the power control PCA to ensure that resistor R23 is 121kilohms and R21 is 90.9kilohms.

To adjust the low-line detector, short test point E1 on the power control PCA to ground and adjust potentiometer R1 clockwise until the PONH and PFWL LED's turn on. This indicates a system power fail. Remove the ground jumper from test point E1. The LED's will then turn off and the setting will be approximately 10 percent below the AC line voltage.

10-43. ADJUSTMENTS

There are two adjustments provided for the main power supply and one for the memory power supply. Potentiometer adjusts the +5V and the other adjusts both the +12V and -12V. The memory power supply adjustment is available for +5M.

To adjust the main power supply voltages, proceed as follows:

a. Remove the lower front panel of the processor cabinet.

b. On the backplane, connect the voltmeter to the +5V test point. Adjust the V1 potentiometer to obtain a meter reading of +4.990 to +5.010 volts.

c. Connect the voltmeter to the +12V test point on the backplane. Adjust the +12 VOLT potentiometer to obtain a meter reading of +12.00 volts. Measure the -12V test point and check that the voltage is within -12.250 to -11.750 volts.

NOTE

The V1, V2, and -12 I limit are preadjusted at the factory. Since special test setups are required, do not attempt to make these adjustments.