INSTALLATION AND SERVICE MANUAL

HP 30360A HARDWIRED SERIAL INTERFACE

(For HP 3000 Series II and Series III Computer Systems)

Manual No. 30360-90001
Microfiche No. 30360-90005

Printed: Mar 1977
Update No. 1: May 1979

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Printed-Circuit Assembly 30360-60001

HEWLETT-PACKARD COMPANY
19447 PRUNERIDGE AVENUE, CUPERTINO, CALIFORNIA 95014

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PREFACE

This manual contains installation and servicing information for the HP 30360A Hardwired Serial Interface Printed-Circuit Assembly (HSI PCA). The HSI PCA provides I/O capability between multiple HP 3000 Series II/III Computer Systems, or between HP 3000 Series II/III and HP 1000 Computer Systems.

This manual was written with the assumption that the reader has a thorough knowledge of the HP 3000 Series II or Series III I/O system hardware and is familiar with binary synchronous communication techniques.

This manual is organized in four sections as follows:

Section I, General Information describes the main features of the HSI PCA, briefly explains how it operates, and describes how the HSI PCA could be used in the computer system.

Section II, Installation, provides the unpacking, initial inspection, and installation procedures for installing an HSI PCA and HSI cable assembly into an existing HP 3000 Series II/III Computer System.

Section III, Principles of Operation, contains information on the hardware operation of the HSI PCA. An overview of the I/O system is given, as well as a block-level description of the HSI PCA.

Section IV, Maintenance, contains general servicing information. Also included is an alphabetic listing of HSI PCA input and output signals and a schematic diagram of the HSI cable assembly.

The titles and part numbers of other documents related to the HSI PCA are:

HP 30360A Hardwired Serial Interface Stand-Alone Diagnostic Program (D432) Manual, part number 30360-90007.

HP 3000 Series II/III Computer System Reference Manual, part number 30000-90020.

HP 3000 Series II/III Computer System Service Manual, part number 30000-90018.

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GENERAL INFORMATION

SECTION I

1-1. INTRODUCTION

1-2. This section describes the functional and physical characteristics of the HP 30360A Hardwired Serial Interface (HSI) PCA, see figure 1-1. Related publications that may be required to service the HSI PCA are listed in the preface to this manual.

1-3. GENERAL DESCRIPTION

1-4. The HSI PCA provides the HP 3000 Computer System with four high-speed data communication channels between multiple HP 3000 Computer Systems, or between HP 3000 and HP 1000 Computer Systems. Communication between systems is by coax cable. In this manual, the discussions assume the HP 3000 and the HSI PCA to be the master station or system, and the HP 1000 or HP 3000 on the other end of the channel to be the external or remote station.

1-5. With four channels available for communication, each channel may be used independently, that is, channel 0 may be connected to an HP 3000 Computer System, channel 1 may be connected to a HP 1000 Computer System, channel 2 may be connected to an HP 3000 Computer System, and channel 3 may be unused. Any configuration of channel connections may be used, each channel is not restricted to a particular use and operates independently of the others.

1-6. Communications on the channel is in a serial data format while communication between the HSI PCA in the master station and the CPU is in 16-bit parallel format.

1-7. TYPICAL USES

1-8. Two typical uses are discussed in the following paragraphs, that is, point-to-point and multi-channel operation.

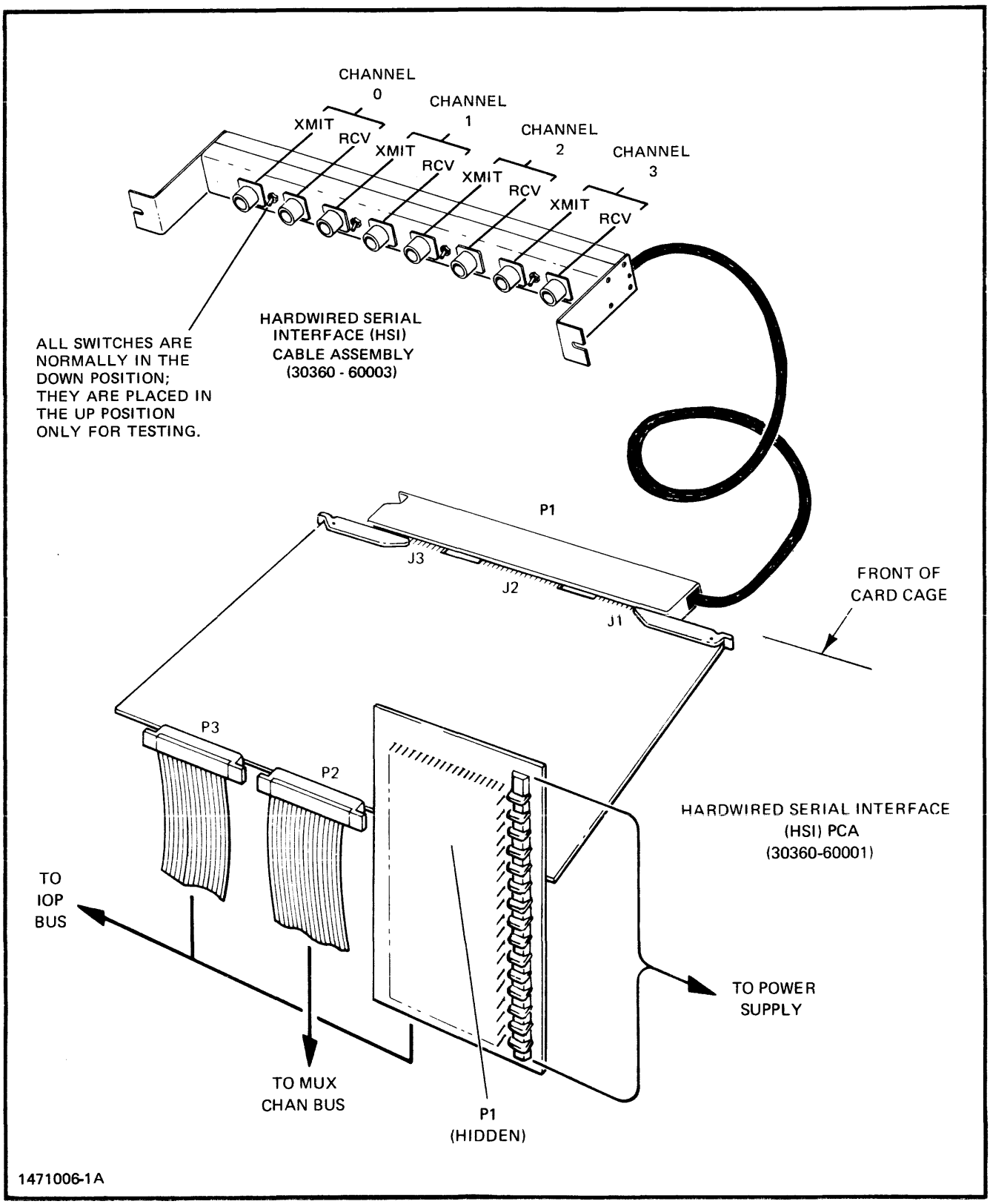

Figure 1-1. Hardwired Serial Interface (HSI) PCA

1-9. Point-To-Point Operation

1-10. Point-to-point operation (see figure 1-2) is the simplest method of communication. It requires one HSI PCA at the master station and a compatible I/O board at the remote station. If communication is between HP 3000 Computer Systems, an HSI PCA is required at each station. If communication is between an HP 3000 and an HP 1000 Computer System, an HSI PCA is required at the master station and an HP 12889A Hardwired Serial Interface Kit is required at the HP 1000 station.

1-11. Multi-Channel Operation

1-12. Multi-channel operation (see figure 1-3) is the configuration used when more than one channel of the HSI PCA is connected, that is, channel 0 is connected to an HP 3000, channel 1 is connected to an HP 1000, channel 2 is connected to an HP 3000, and channel 3 is connected to an HP 1000.

1-13. Multi-Drop Operation

1-14. Current software configuration does not support multi-drop operation.

1-15. FEATURES

1-16. The important features of the HSI PCA are:

* Programmable bit rate.
* Transmission speeds of 2.5 megabits/second via coax cable for distances up to 1000 feet (304.8 meters) or 1.25 megabits/second for distances up to 2000 feet (609.6 meters) are possible.
* Uses a pair of unidirectional coax cables for communication.
* SIO program operation.
* Direct program operation.
* Handshake operation. (Word rate determined by the receive station.)
* Block Check Character-Cyclic Redundancy Checking method to check the block of data after it is received.

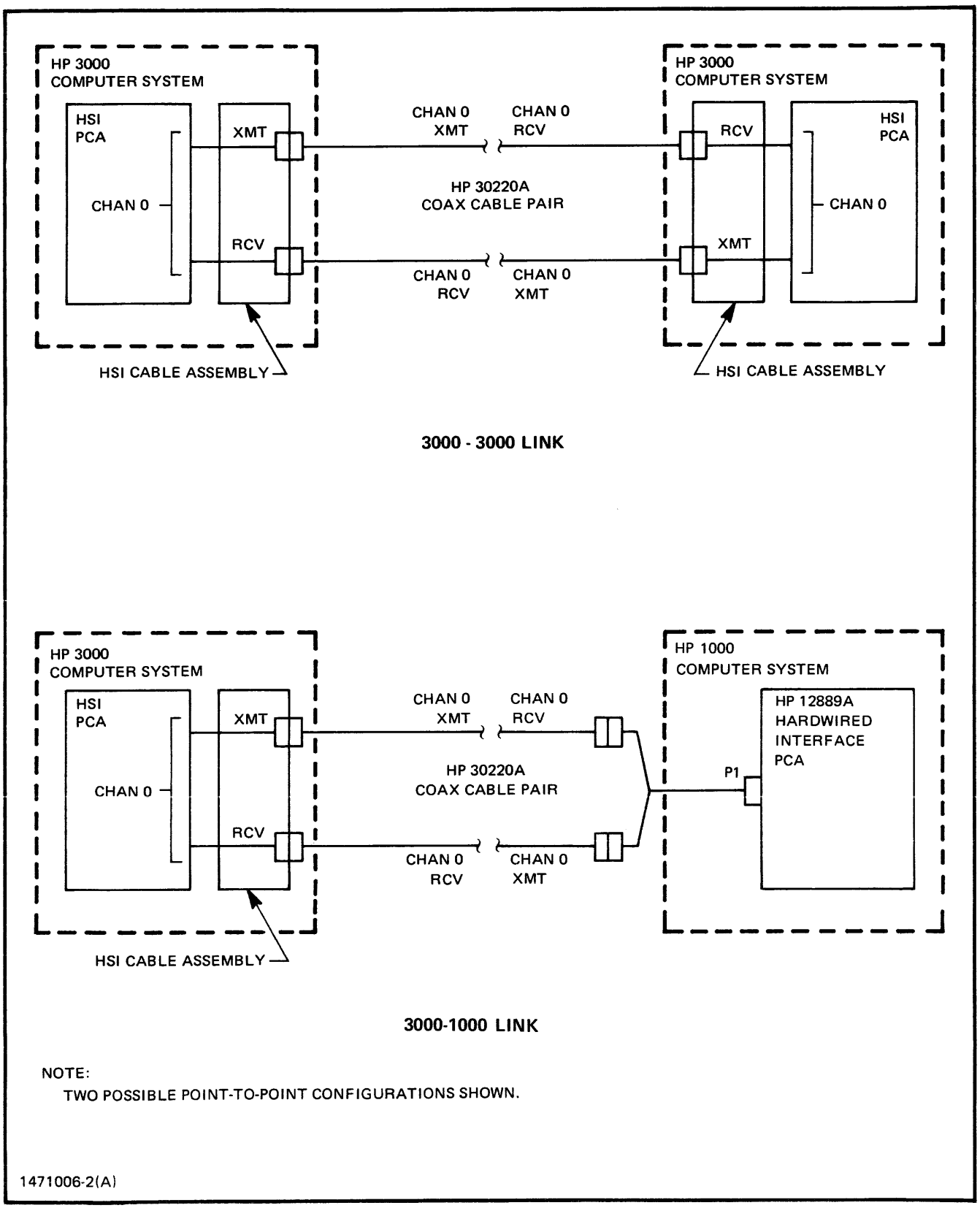

Figure 1-2. Point-To-Point Operation

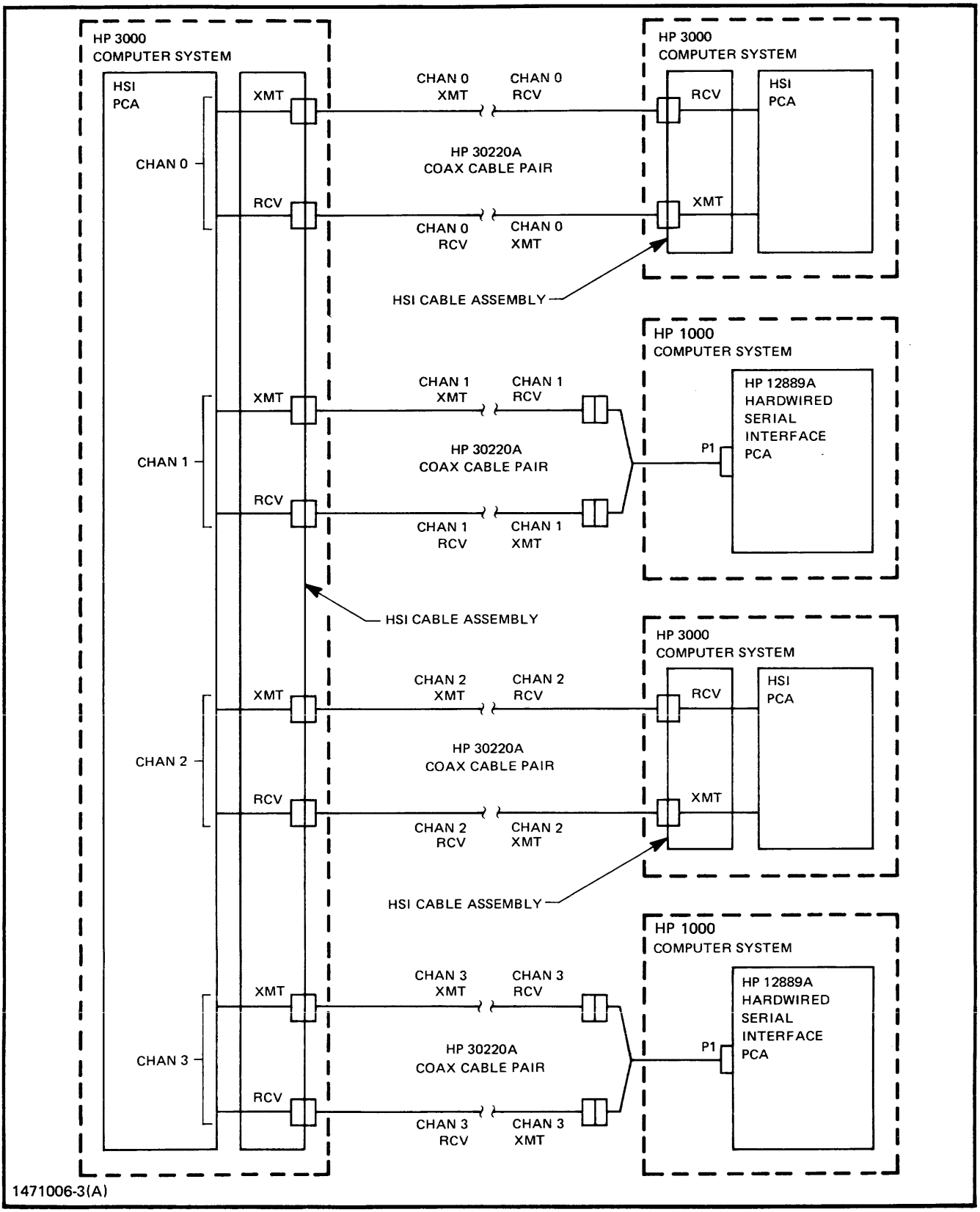

Figure 1-3. Multi-Channel Operation

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1-17. EQUIPMENT SUPPLIED

1-18. The HP 30360A HSI PCA consists of the following items:

* One Hardwired Serial Interface PCA, part number 30360-60001.

* One HSI Cable Assembly, part number 30360-60003.

* One Installation and Service Manual, part number 30360-90001.

* One HP 30360A Hardwired Serial Interface Stand-Alone Diagnostic Program (D432) Manual, part number 30360-90007.

1-19. In addition, an HP 30220A Hardwired Communications Cabling Kit is available for interconnecting two HSI PCA's. Each kit contains the necessary coax cables and connector components. One to four kits may have been ordered, depending upon the number of hardwired channels that have to be configured. Several cable length options are available, from 25 to 2000 feet. Cable length cannot exceed 2000 feet. Table 1-1 lists the available cable length options.

Table 1-1. Cable Length Options

OPTION	LENGTH	
	FEET	METERS
Standard	25	7.62
001	100	30.48
002	250	76.20
003	500	152.40
004	1000	304.80
005	2000	609.60

1-20. IDENTIFICATION

1-21 Printed-circuit assemblies (PCA's) are identified by a part number etched on the PCA. Revisions to the PCA are identified by a letter, a series code, and a division code (A-0000-00) marked beneath the part number of the PCA. The letter identifies the version of the etched trace pattern on the unloaded PCA. The four-digit series code pertains to the electrical characteristics and the positions of the components on the PCA. The two-digit division code identifies the division of Hewlett-Packard that manufactured the PCA.

INSTALLATION

SECTION II

2-1. INTRODUCTION

2-2. This section contains information regarding the unpacking, initial inspeciton, and installation procedures of an HSI PCA and HSI cable assembly into an existing HP 3000 Computer System.

2-3. UNPACKING AND INITIAL INSPECTION

2-4. If the HSI PCA and HSI cable assembly are received separately from the computer system, inspect the carton containing the items before opening. If there is evidence of external damage, or if the carton rattles, notify the nearest HP Sales and Service Office and request that the carrier's agent be present when the carton is opened.

2-5. Inspect each component as the carton is unpacked. If the HSI PCA or HSI cable assembly is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office, immediately. Retain the shipping carton and packing material for the carrier's inspection. The HP Sales and Service Office will arrange for repair or replacment of the damaged part without waiting for any claims against the carrier to be settled.

2-6. PREPARATION FOR INSTALLATION

2-7. Power Requirements

2-8. The HSI PCA obtains operating power directly from the computer system power supply. Before installing the HSI PCA into the computer system card cage, determine that the additional current requirements will not overload the power supply. The HSI PCA requires:

+5V at 4.5A

+15V at 260mA

-15V at 40mA

2-9. PCA Jumpers

2-10. Configure the HSI PCA jumpers as specified on the subsystem configuration form and file this form in the System Support Log for future reference. See figure 2-1 for the location of the jumpers.

a. SERVICE REQUEST PRIORITY (W2). Jumper wire W2 selects one of 16 service request lines to the multiplexer channel. Each controller serviced by a particular multiplexer channel must be connected through a separate service request number. The HSI PCA service request connection should be of a lower priority than the magnetic tape controller (i.e., higher service request line numerically).

b. GROUP INTERRUPT MASK (W1). Jumper wire W1 selects the group interrupt mask bit that the HSI PCA responds to during a SMSK instruction. The jumper can be associated with any of the 16 bits of the transmitted mask word, to a permanent enable position, or a permanent disable position. For this application, place the jumper in the ENABLE position.

c. DEVICE NUMBER (W3B through W3H). The configuration of these seven jumper wires determines the device number and, therefore, the DRT address associated with the HSI PCA. A logic 1 is represented by the absence of a jumper wire and, conversely, a logic 0 is represented by the installation of a jumper wire. Check with the system manager to determine the device number.

d. DRT ADDRESS PARITY (W3A). Jumper wire W3A selects the DRT address parity depending on the configuration of jumper positions W3B through H (device number jumpers). This jumper is removed or installed so that the total number of jumpers removed in positions W3A and W3B through H is odd.

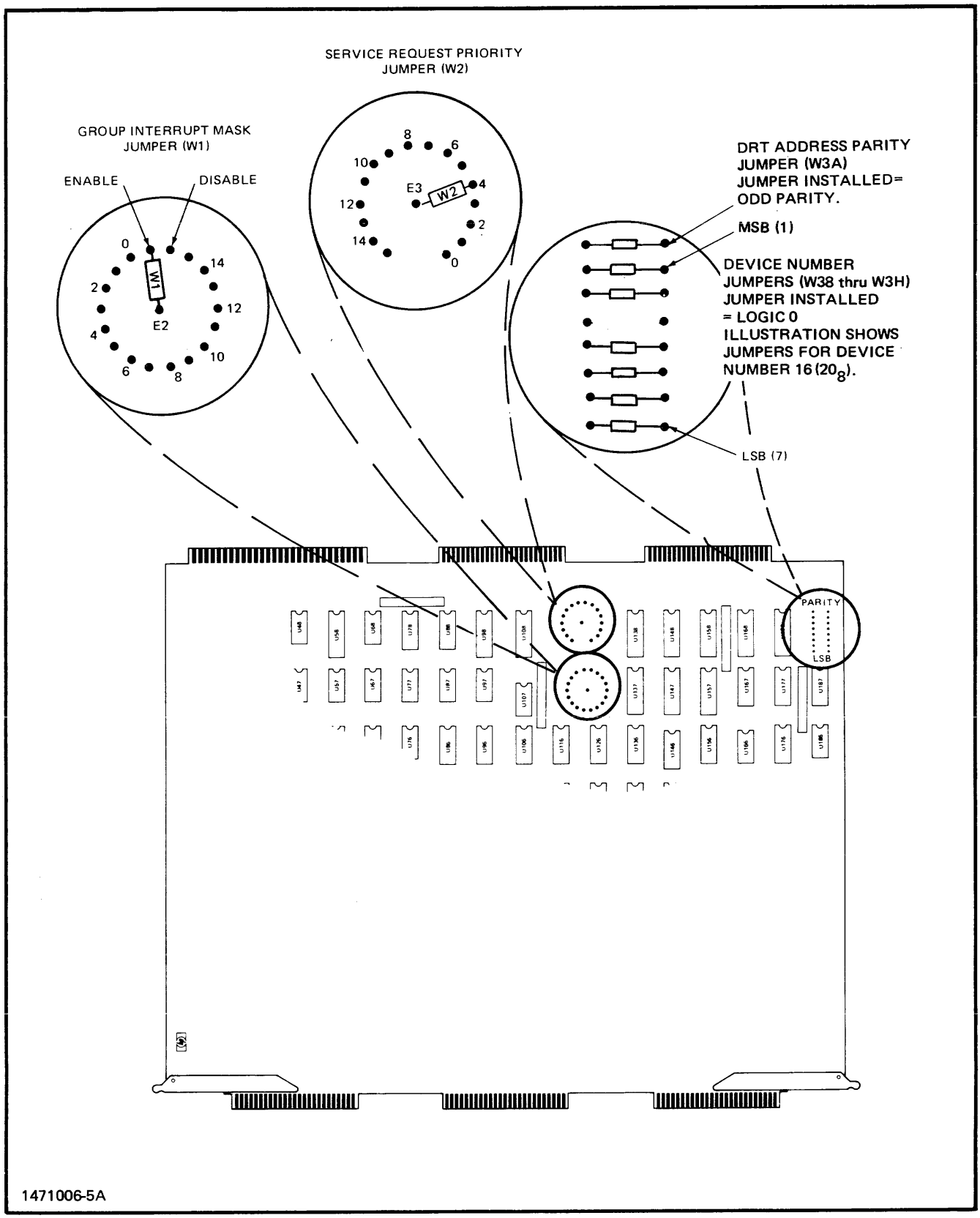
2-11. INSTALLATION

2-12. Installation consists of fabricating connectors on the customer's coax cables, installing the HSI PCA in the card cage associated with the multiplexer channel, and mounting the HSI cable assembly.

2-13. Cable Fabrication

2-14. The customer is responsible for laying his own coax cable pairs, but not for connector fabrication. Refer to your system's Site Preparation and Installation Manual for further details regarding site preparation.

2-15. To identify each coax cable pair, short one end of one cable. Then, use an ohmmeter (not a light) at the other end to identify matching ends.



May 1979 Figure 2-1. HSI PCA Jumper Locations

2-16. For a 3000-3000 link, each cable will have a two-contact connector on one end and a three-contact connector on the other end. The part numbers of the connectors used are shown in figure 2-2. Note that at the HP 3000, the two-contact female connector always connects to the HSI cable assembly connector labeled RCV, and the three-contact female connector always connects to the HSI cable assembly connector labeled XMT.

2-17. For a 3000-1000 link, one cable will have a two-contact connector on one end and a three-contact connector on the other end. The other cable will have a two-contact connector on each end, one male and the other female. The part numbers of the connectors used are shown in figure 2-2. Note that at the HP 3000, the two-contact female connector always connects to the HSI cable assembly connector labeled RCV, and the three-contact female connector always connects to the HSI cable assembly connector labeled XMT.

2-18. Supplied components for connector fabrication are listed in table 2-1.

Table 2-1. Connector Components

ITEM	PART NO.	QUANTITY
Cable Clamp	1251-2689	4
3-Pin Female Connector	1251-2760	2
2-Pin Female Connector	1251-4749	2
2-Pin Male Connector	1251-4847	1
Bare No. 26 Wire	8151-0030	1.5 ft

2-19. The connectors used with the HP 30220A coax cables pairs are assembled as described in figure 2-3. These connectors are specially designed to provide a greater degree of noise immunity than a conventional coax connector, because the outer conductor cannot come in contact with other conducting material.

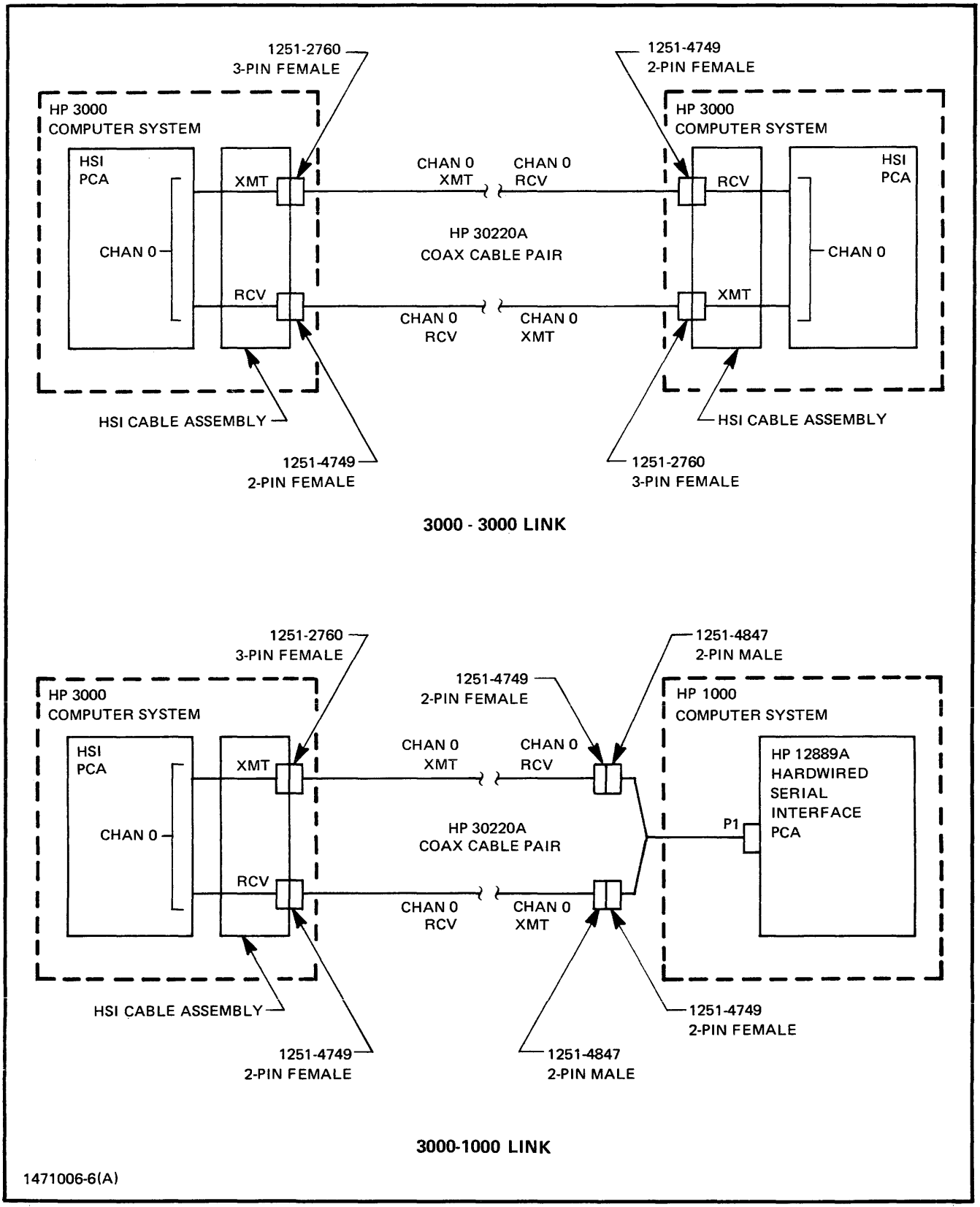
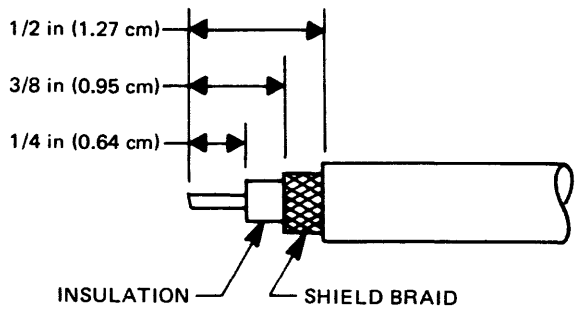


Figure 2-2. Connector Identification

(1) Strip the coax cable to the indicated dimensions.

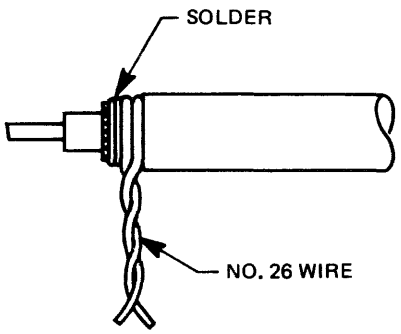


(2) A. Cut a 3 inch length from the No. 26 wire.

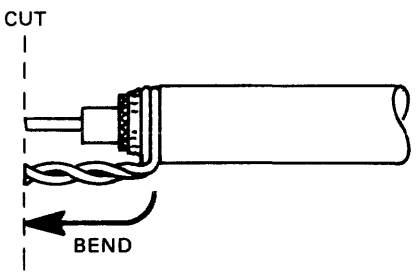
B. Wrap it around the shield twice, then twist the ends.

C. Next to the wire, wrap solder around the shield once or twice, depending on thickness.

D. Holding cable vertical, solder the wire to the to the shield. (Beware of melting the insulation.)



(3) Bend the twisted ends, then cut them even with the end of the center conductor.



(4) Discard the rubber sleeve from the cable clamp.

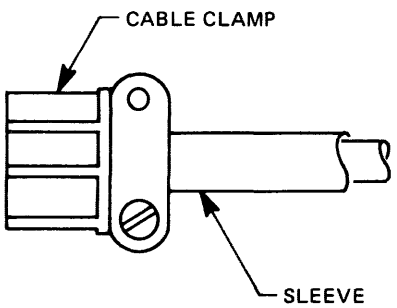


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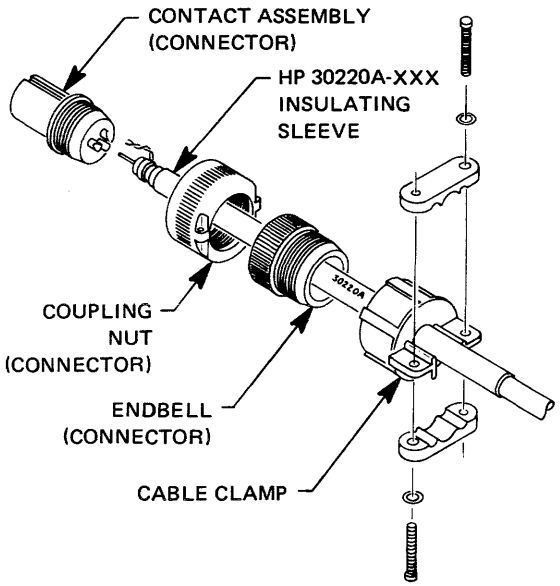
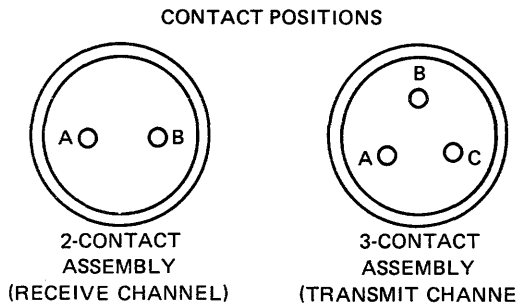
Figure 2-3. Connector Fabrication

(5) Assemble the connector parts, insulating sleeve, and cable clamp on the coax cable in the sequence shown here. Note that the numbered end of the sleeve is located away from the cable end. The contact assembly and coupling nut may be separate (as shown here) or may be pre-assembled into one unit.

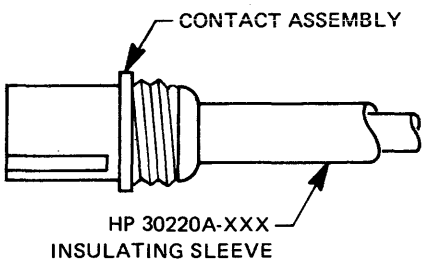
OPTION (HP 30220-XXX)	LENGTH		INSULATING SLEEVE PART NO.
	FEET	METERS	
Standard	25	7.62	30220-80001
-001	100	30.48	30220-80002
-002	250	76.20	30220-80003
-003	500	152.40	30220-80004
-004	1000	304.80	30220-80005
-005	2000	609.60	30220-80006



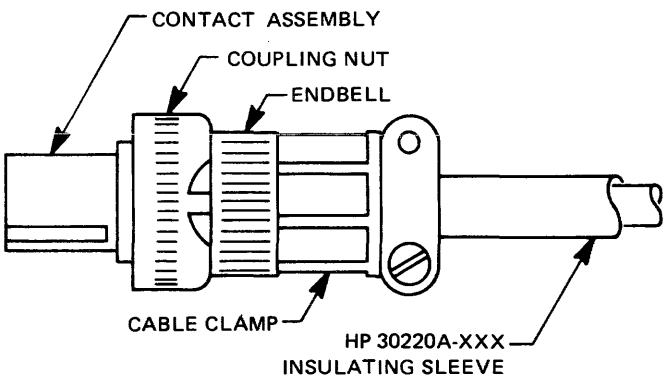
(6) Solder the twisted wire to socket contact A, and the center conductor to socket contact B. (Contact C of 3-contact assemblies is not used.)



(7) Slide the insulating sleeve over the soldered connections so they are fully covered.



(8) Assemble the connector and clamp as shown here, then tighten the clamp enough to firmly grip the cable.



(9) Repeat this procedure for remaining connectors.

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Figure 2-3. Connector Fabrication (Continued)

2-20. HSI PCA Installation

2-21. Install the HSI PCA as follows:

a. Have the system operator back-up the system files before proceeding with the installation.

b. Ensure that the HSI PCA jumpers are configured as outlined in paragraph 2-9.

c. Unlock and open the door of the card cage associated with the multiplexer channel.

d. Set the SYSTEM DC POWER switch to the STANDBY position.

e. Install the HSI PCA into the card cage associated with the multiplexer channel.

f. Record the location of the HSI PCA in the configuration section of the System Support Log.

2-22. HSI Cable Assembly Installation

2-23. Install the HSI cable assembly as follows:

a. Remove the rear door from the appropriate bay. Figure 2-4 illustrates the locations for installing the HSI cable assembly.

b. Mount the HSI cable assembly inside the rear door frame at the appropriate location using the hardware supplied.

c. Route the hood end of the HSI cable assembly to the front of the card cage that contains the HSI PCA.

d. Connect the cable hood to the HSI PCA. Figure 4-1 illustrates the connector numbering scheme.

e. Install the interrupt poll (twisted-pair) observing the polarity of the wires. The HSI PCA should come after the disc, before the magnetic tape controller, and after the synchronous single-line controller in the interrupt poll series.

f. Connect the fabricated HP 30220A coax cable pairs to the HSI cable assembly. See figures 1-2 through 1-3 for possible connection configurations.

g. Set the SYSTEM DC POWER switch to the ON position.

h. Run the stand-alone diagnostic for the HSI PCA as outlined in the HP 30360A Hardwired Serial Interface Stand-Alone Diagnostic Program (D432) Manual, part number 30360-90007.

NOTE

Correct any problems indicated by the diagnostic.

i. Ensure that all four NORMAL/TEST switches on the HSI cable assembly are set to the NORMAL position.

j. Have the system operator return the system files from back-up.

k. Return the system to the customer.

2-24. RESHIPMENT

2-25. If the HSI PCA or HSI cable assembly is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the part number and date code of the item.

2-26. Package the item in the original factory packaging material, if available. If the original material is not available, standard factory packaging material can be obtained from a local Hewlett-Packard Sales and Service Office.

2-27. If standard factory packaging material is not used, wrap the item in Air Cap TH-240 cushioning (or equivalent) manufactured by Sealed Air Corp., Hawthorne, N.J. and place in a corrugated carton (200-pound test material). Seal the carton securely and mark it ''FRAGILE'' to ensure careful handling.

NOTE

In any correspondence, identify the item by part number and date code. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

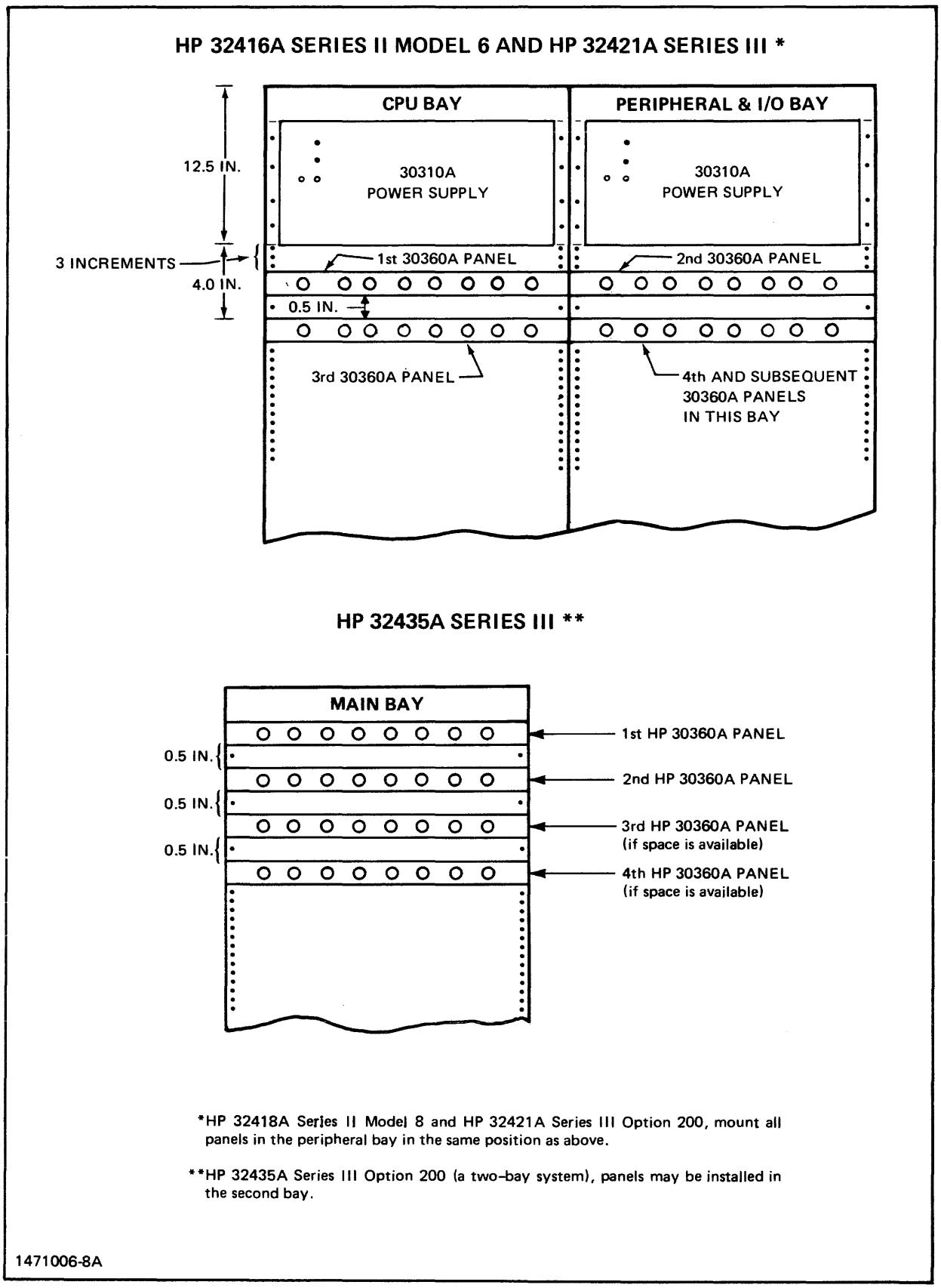


Figure 2-4. HSI Cable Assembly Physical Placement

PRINCIPLES OF OPERATION

SECTION III

3-1. INTRODUCTION

3-2. This section contains system-level and functional level descriptions of operation for the HP 30360A Hardwired Serial Interface (HSI) PCA. The system-level description briefly describes the operation of the HSI PCA in relation to the HP 3000 Computer System. The functional-level description divides the HSI PCA into functional circuit groups and provides a description of operation for each group.

3-3. SYSTEM-LEVEL DESCRIPTION

3-4. The HSI PCA is combined with the HSI cable assembly to form a subsystem of the HP 3000 Computer System (see figure 3-1). This subsystem can be any of sixteen subsystems connected to each multiplexer channel in the overall system. Operation of the subsystem requires the transfer of commands, data, and status information between the HSI PCA and the following system components:

* Memory Module
* Central Processor Unit (CPU)
* Input/Output Processor (IOP)
* Multiplexer Channel
* Remote stations via coax cable

3-5. The memory module contains the I/O drivers that are executed by executed by the CPU, I/O programs that are transferred by the IOP to the multiplexer channel, and the device reference tables (DRT).

3-6. The multiplexer channel is a controller for up to 16 subsystems and contains a one-word storage location for each subsystem. Program instructions from the IOP are stored one at a time in the storage location for the addressed subsystem. Each program word is then decoded by the multiplexer channel and sent through the MUX CHAN bus to the appropriate I/O PCA. When the I/O PCA accepts the decoded program instruction, it returns an acknowledge signal to the IOP and performs the instruction. The HSI PCA and multiplexer channel exchange signals to control and monitor instruction execution.

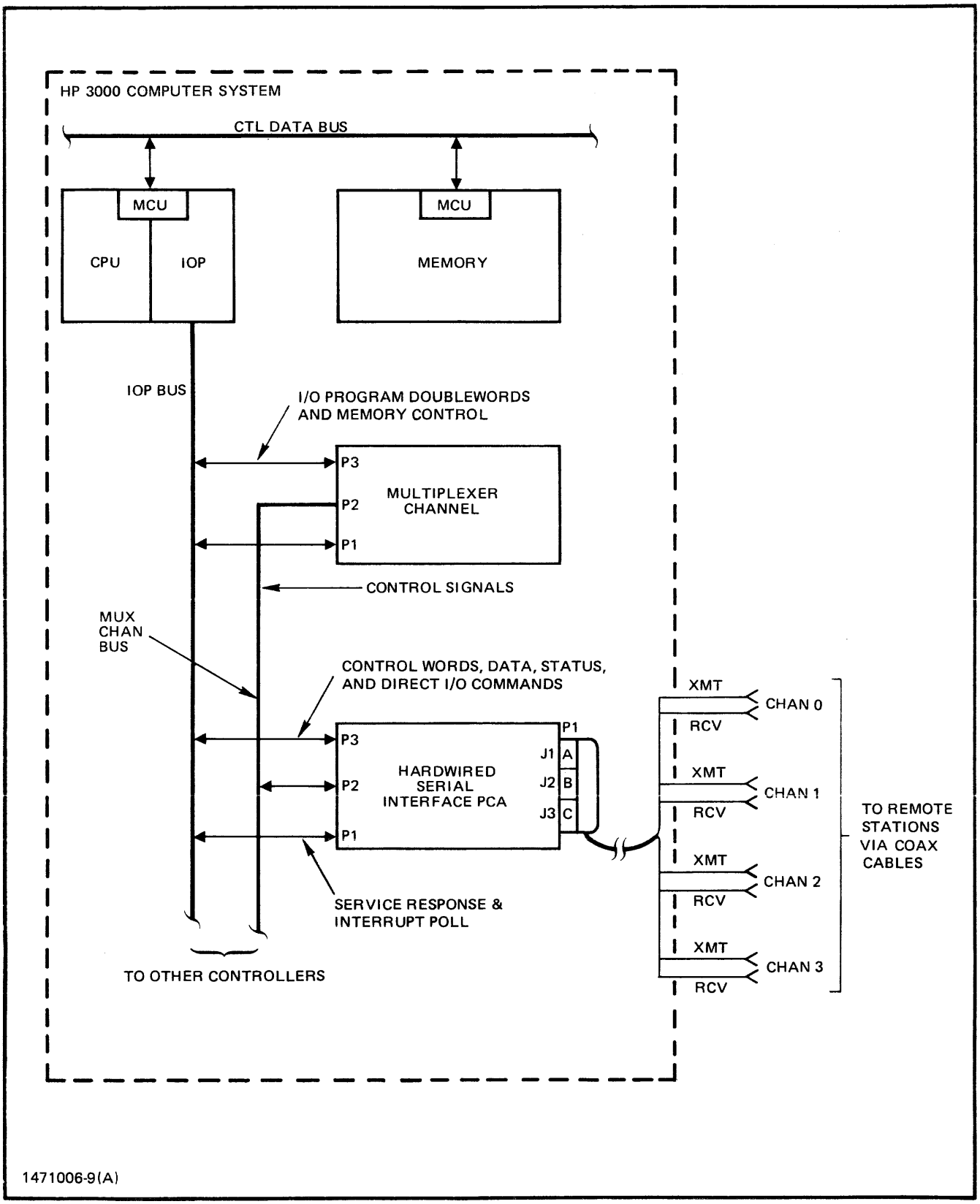


Figure 3-1. Interface to System

3-7. Data is transferred to and from the remote stations through the HSI PCA via the IOP bus. This transfer occurs in response to either direct or SIO program instructions. The device number (address) and interrupt priority are determined by relocatable jumpers on the HSI PCA. An interrupt to transfer data to or from the remote station can be initiated by the operating program or by an interrupt request from the remote station and the HSI PCA. Interrupt requests are also initiated due to several different status conditions.

3-8. Status conditions for the HSI PCA and remote stations, including the conditions that cause an automatic request for interrupt, are transferred from the HSI PCA through the IOP bus data lines. These status conditions are transferred as a 16-bit status word.

3-9. Eight control words can be sent to the HSI PCA through the IOP bus data lines. Each control word consists of 16-bits, three bits are used for determinimg the function, the remaining 13-bits are used as required to set the various conditions of the function. The control word bit configurations and functions are described later in this section.

3-10. The HSI PCA bus logic (see figure 3-2) provides the interface between the IOP and multiplexer channel and the circuits of the HSI PCA. All commands, data, status, and control information pass through the bus logic.

3-11. Programmed instructions are applied to the control circuits through the bus logic to manage the functional operation of the HSI PCA. The control circuits decode the instructions and issue signals to the other functional circuits to control transmit, receive, status, error detection, and channel selection.

3-12. The receive section assembles the serial data from the input/output select section into a 16-bit parallel word for transmission through the bus logic to the IOP. Double buffering is used in the receive section so that one word can be shifted to the buffer register while another word is being received. When a word is ready in the buffer register, control is flagged to begin transfer of that word to the CPU or memory.

3-13. Parallel 16-bit words for transmission are sent to the transmit section from the bus logic where they are assembled into serial format for transmission. Control receives a flag that a word is ready for transmission, and sends a signal to shift the transmit data to the input/output select section and enter another word into the transmit register. Double buffering is also used in the transmit section. Along with the 16-bit data word, one tag bit, one start and two stop bits are also present. Figure 3-3 illustrates the data word format. Also shown is the control word format. It is discussed in detail later on in this section.

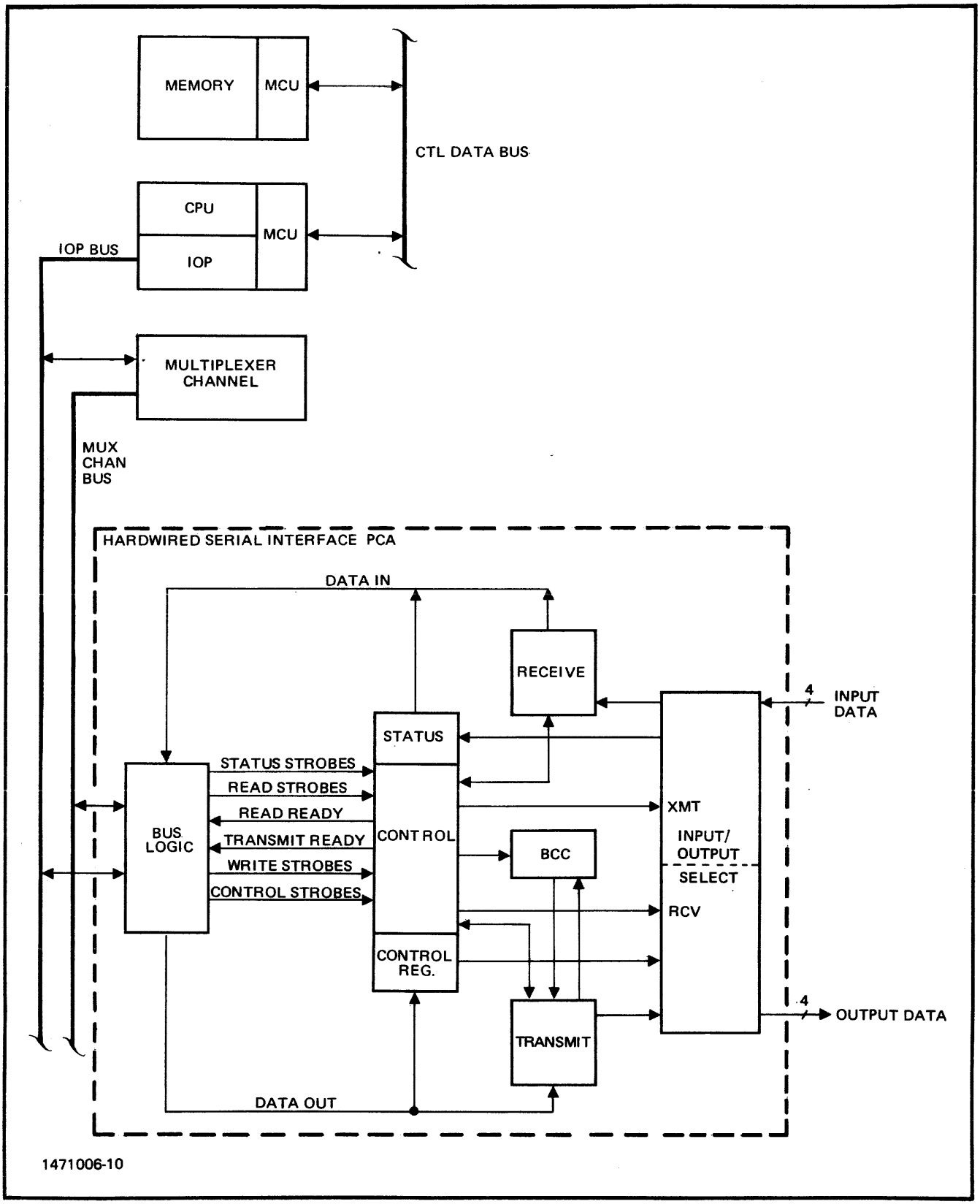


Figure 3-2. System Block Diagram

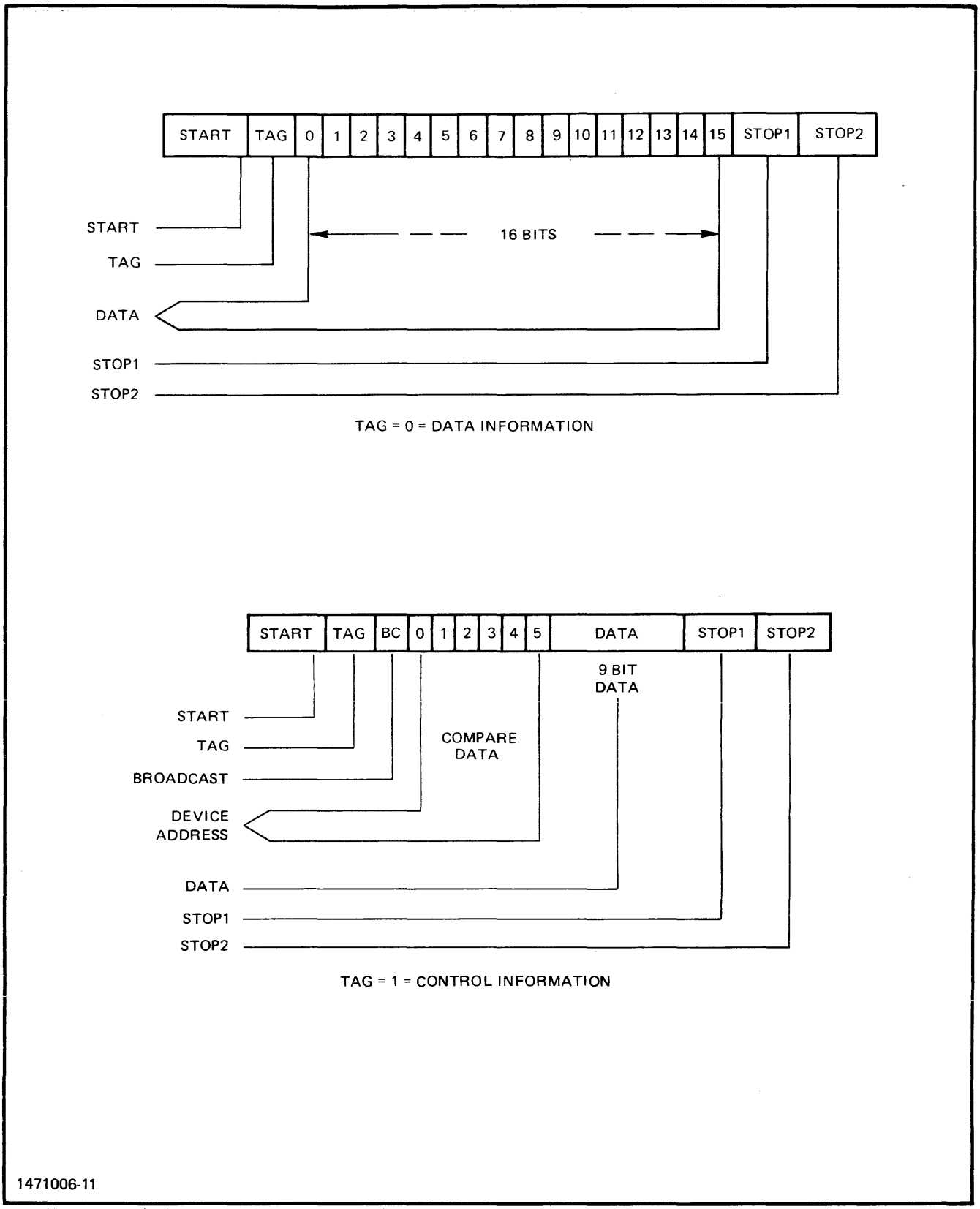


Figure 3-3. Data and Control Word Formats

3-14. Error detection is checked in the block check character (BCC) section. The cyclic redundancy check (CRC) method is used for error detection which checks the block after it has been received. Cyclic redundancy checking is a division performed by both the transmitting and receiving stations using the numeric binary value of the message as a dividend, which is divided by a constant derived from the CRC polynominal. The quotient is discarded and the remainder serves as the check character. The receiving station compares the transmitted remainder to its own computed remainder, and finds no error if they are equal. If a CRC error has been detected, a status bit and interrupt will be set.

3-15. The input/output select section selects one of four channels to transmit and receive with a two-bit command code from the control section. Each channel of the input/output select section is connected to a coax cable for receive and a coax cable for transmit. The four coax inputs are detected through optical isolators; the four coax outputs are capable of driving 75-ohm coax cables.

3-16. System I/O Modes

3-17. The HSI PCA can be operated in one of two system I/O modes:

* Direct

* SIO

3-18. DIRECT MODE. In the direct mode of operation, the CPU executes the I/O instruction stored in memory and issues direct I/O commands through the IOP via the IOP bus directly to the addressed HSI PCA. When the HSI PCA accepts a command, it returns an acknowledge signal and performs the command. The CPU is involved in considerable overhead handling each instruction in this operating mode.

3-19. SIO MODE. An SIO instruction calls a routine that permits the IOP to transfer an I/O program, one instruction at a time from the memory module to the multiplexer channel. The multiplexer channel then controls operation of the HSI PCA. Instructions contained in the I/O program are similar to the instructions contained in the direct I/O mode and they perform many of the same functions such as Read I/O and Write I/O. When the multiplexer channel assumes control of the HSI PCA for I/O operation, the CPU is free to perform other functions. The control functions discussed later in this section are used in the IOAW position of the SIO order pair. The IOCW position is unused except as defined by the multiplexer channel.

3-20. Data Transmission Modes

3-21. The HSI PCA can be operated in one of two data transmission modes:

* Repeat

* Acknowledge

3-22. REPEAT MODE. In the repeat mode of operation, the incoming information to the HSI PCA may be disregarded except for special tag words. Tag words may convey data or control information depending on the condition of the tag bit. Figure 3-3 illustrates the word format. When the word is received with the tag bit set (1), the word is compared with a pre-programmed word. If a comparison exists, an interrupt request is sent to the IOP and the received tag word is transmitted two bit times later to the originating station. The status register of the HSI PCA is updated to signify a tag bit has been received and that the tag word and pre-programmed word compared. The IOP will then request a status of the HSI PCA and process the interrupt request according to the information contained in the status word.

3-23. ACKNOWLEDGE MODE. The acknowledge mode of operation is also called handshake and may be used either transmitting or receiving. When operating in the transmit acknowledge mode, the station will not transmit the second word of a message until it has received some word from the receiving station. This signifies that the first word transmitted has been received and the second word is then sent. This acknowledge scheme continues for each word to be transmitted. When operating in the receive acknowledge mode, the first word received causes some word to be sent to the transmitting station to signify that the word has been received. The transmit station then sends the next word and the acknowledge or handshake exchange continues until the end of message.

3-24. Functional-Level Description

3-25. The HSI PCA performs seven interrelated functions. These functions are input/output selection, transmit, receive, control, block check character, status reporting, and communication with the IOP and multiplexer channel through the bus logic. Each of these functions is divided into circuit groups and operation of the circuit groups is described in the following paragraphs.

3-26. Bus Logic

3-27. The HSI PCA bus logic is functionally identical to the bus logic used by other HP 3000 controllers on the multiplexer channel. The IOP issues direct I/O commands to the bus logic to initiate the execution of an I/O program stored in memory. The I/O program, containing I/O program doublewords, runs independently of the CPU under control of the multiplexer channel and the HSI PCA. The bus logic controls the application of control signals from the multiplexer

channel to the rest of the HSI circuitry. It also contains the circuitry to process interrupt requests from the control section logic, and to control the transfer of control, data, and status between the IOP and the HSI PCA over the IOP bus. Refer to the HP 3000 Series II Computer System Reference Manual for additional information on the bus logic.

3-28. DIRECT I/O OPERATION. Direct I/O operations are under control of the CPU. Instructions are issued to the IOP to send a direct I/O command to a specific device on the IOP bus. The HSI PCA (along with all other devices on the IOP bus) receives a 3-bit direct I/O command (IOCMD), an 8-bit device number (DEVNO), and a service out bit (SO). The IOCMD bits indicate which operation is to be performed, the DEVNO bits indicate the device being addressed, and the SO bit indicates that the direct I/O command and device number are on the IOP bus. The HSI PCA bus logic will decode the direct I/O command provided its jumper-selectable device number compares with the device number on the IOP bus. The HSI PCA can respond to all eight direct I/O commands. These commands are listed in table 3-1. After a series of interlocking operations, the HSI PCA bus logic will acknowledge receipt of the direct I/O command by returning a service in signal (SI) on the IOP bus.

Table 3-1. Direct I/O Commands

IOCMD BITS			I/O DRIVER	DECODED COMMAND	
00	01	02	COMMAND	NAME	ABBREVIATION
1	1	1	SIN	SET INTERRUPT	SET INT
0	1	1	RESET INT	RESET INTERRUPT	RESET INT
1	0	1	SIO	START INPUT/OUTPUT	SIO
0	0	1	SMSK	SET MASK	SMSK
1	1	0	CIO	DIRECT CONTROL STROBE	D CONT STB
0	1	0	TIO	DIRECT STATUS STROBE	D STATUS STB
1	0	0	WIO	DIRECT WRITE STROBE	D WRITE STB
0	0	0	RIO	DIRECT READ STROBE	D READ STB

3-29. I/O PROGRAM OPERATION. Execution of an I/O program is initiated when the IOP issues a direct Start I/O command to the HSI PCA. Once initiated, the I/O program is controlled by the multiplexer channel through the IOP over the IOP bus. The I/O program consists of a number of I/O program doublewords. Each doubleword consists of an I/O command word (IOCW) and an I/O address word (IOAW). Contained in the IOCW is an I/O program order. The order specifies the operation to be performed. The multiplexer channel accepts I/O program doublewords, one word at a time, from the IOP, decodes the order and sends control signals to the bus logic of the HSI PCA over the MUX CHAN bus.

3-30. Control Section

3-31. The control section logic is divided into two functional areas; command control (see figure 3-4) and service request and interrupt control.

3-32. COMMAND CONTROL. The command control logic decodes the functional commands into eight separate control functions. The sixteen-bit control word from the I/O program is loaded into the Control Function Decoder (see figure 3-4) of the command control circuits with the SO and P CONT STB signals. Bits 0, 1, and 2 of the control word are decoded in the Control Function Decoder. The decoded control function number produces a clock signal that is sent to specific portions of the Control Function Shift Registers to shift out only the bits associated with the decoded control function. The P CONT STB or PCMD1 signals produce an ACK1 signal that causes the bus logic to send a SI signal to the IOP to acknowledge receipt of the first part of the I/O program doubleword.

3-33. Figure 3-5 is a summary of the eight control functions showing bit patterns.

3-34. The following paragraphs and diagrams illustrate the bit configurations and explain the functions performed by each of the eight control functions.

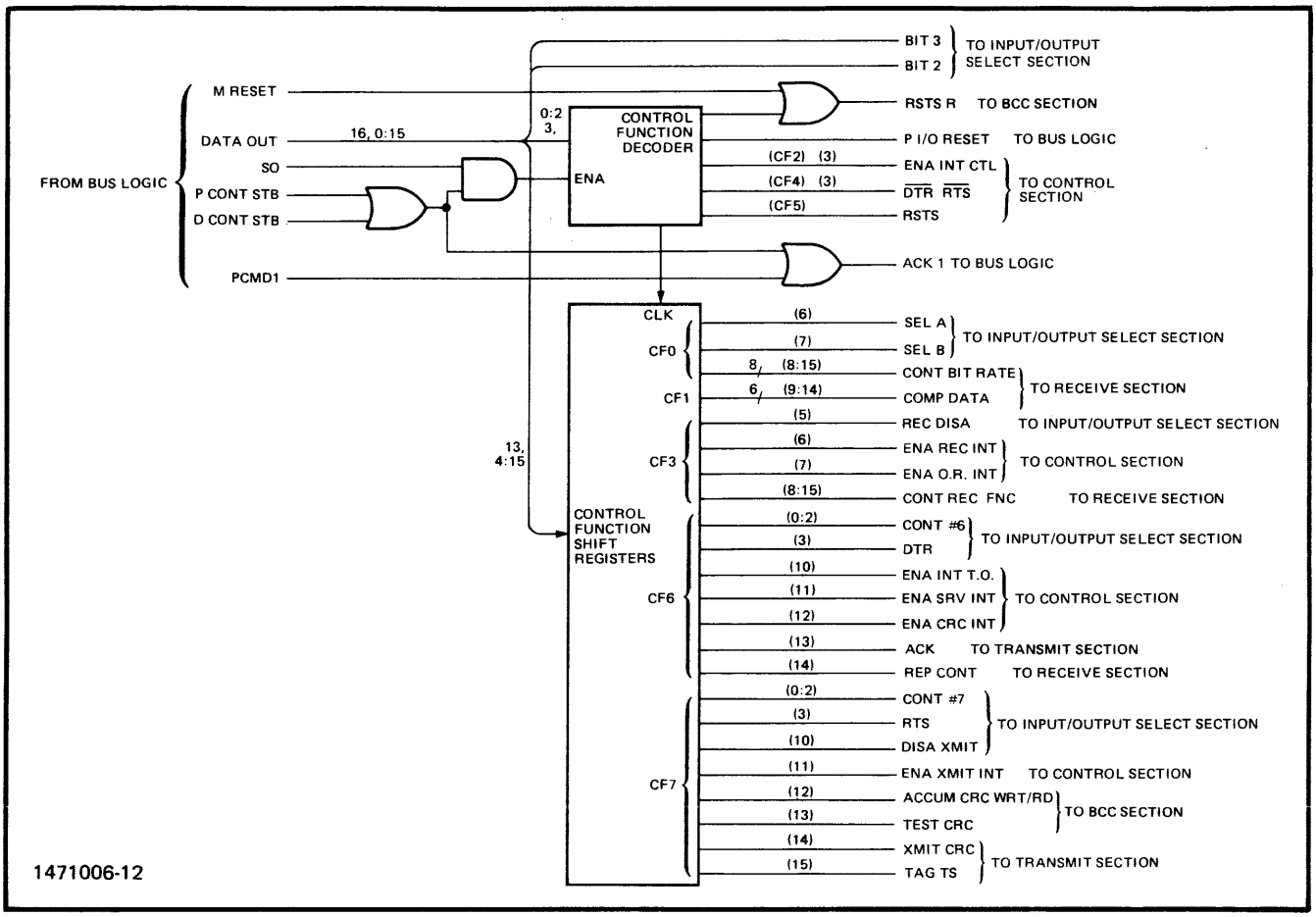
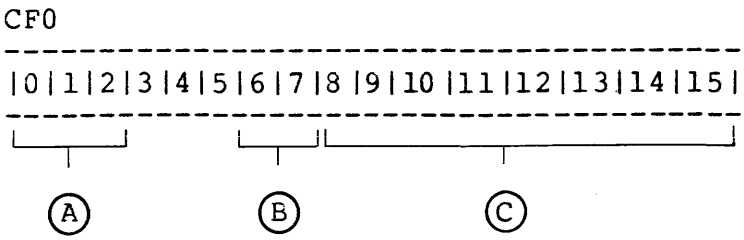


Figure 3-4. Control Section (Command Control)

CONTROL FUNCTION NO.	FUNCTION			BIT CONFIGURATION															
	REC	XMIT	MODE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0			X	0	0	0	X	X	X	CHAN SEL		BIT RATE SELECT							
1	X			0	0	1	X	X	X	X	X	X	COMPARE TAG WORD						X
2			X	0	1	0	INT CONT ENA	X	X	X	X	X	X	X	X	X	X	X	X
3	X			0	1	1	X	X	REC DISA	ENA REC INT	ENA O.R. INT	BC/COMP				TAG WORD			
												DSR	DE	CJ	INT	DSR	DE	CJ	INT
4			X	1	0	0	$\overline{RTS}$ $\overline{DTR}$	P I/O RESET											
								X	X	X	X	X	X	X	X	X	X	X	X
5			X	1	0	1	RESET XMIT/REC & CRC REG												
							X	X	X	X	X	X	X	X	X	X	X	X	X
6	X			1	1	0	DTR	X	X	X	X	X	X	INT	SR INT	CRC ERR	ACK	REP CONT	X
7		X		1	1	1	RTS	X	X	X	X	X	X	DISA XMIT	ENA XMIT INT	ACCUM CRC XMIT	TEST CRC	XMIT CRC	TAG

1471006-13

Figure 3-5. Control Function Bit Configuration Summary



(A) Control function number

(B) Channel Select. These two bits select the channel (0-3).

(C) Bit Rate. The bit rate is determined by bits 8-15. Bit rate can be varied in discrete steps between 2.5M bits/sec down to 9.804K bits/sec. The bit rate is determined by the following method:

a. Divide 2.5×10^6 by the desired bits/sec.

b. Convert the result of the above step (a) to binary form.

c. Calculate the two's complement of the binary number.

d. Reverse the order of the binary bits (MSB on right).

Example: Determine the bit configuration for 10K bits/sec.

$$\frac{2.5 \times 10^6}{1.0 \times 10^4} = 2.5 \times 10^2 = 250$$

Binary equivalent for 250 = 11111010

Two's complement of 11111010 = 00000110

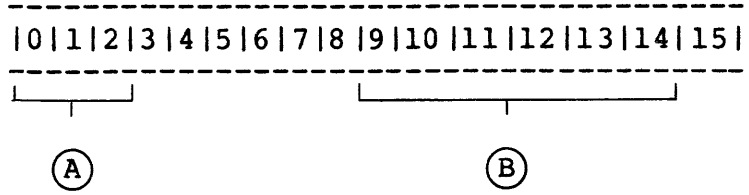
MSB on right = 01100000

8	9	10	11	12	13	14	15
0	1	1	0	0	0	0	0

=%140

Current software configuration supports only 250,000 and 125,000 characters per second; however the DSLINE speed parameter may be used to provide reduced speeds.

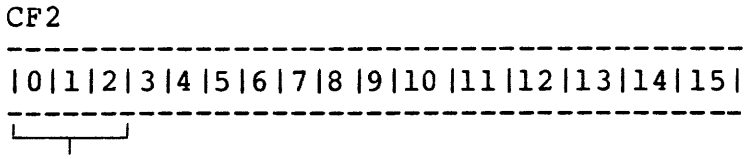
CF1



(A) Control function number

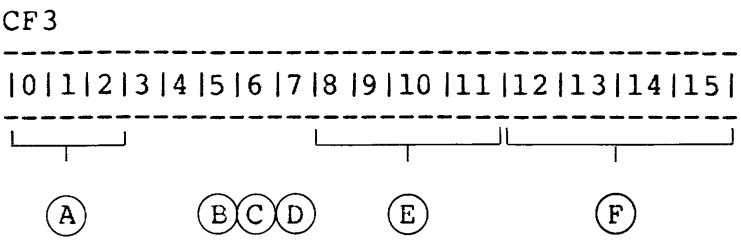
(B) Six bit sequence compared to the six bits of a tag word

CF2



(A) Control function number

(B) Interrupt Control bit. A logic 1 will enable all interrupts and also enable all interrupts that were stored during the disable interrupt period. A logic 0 will reset and disable all interrupts.



(A) Control function number

(B) Receive Disable. A logic 1 disables the input to the input register of the receive section.

(C) Enable Receive Interrupts. A logic 1 allows interrupts to be generated by the HSI PCA when a word is received.

(D) Enable Overrun Interrupt. A logic 1 allows an Over Run error to generate an interrupt if a second word is received before the first word is serviced (overrun condition).

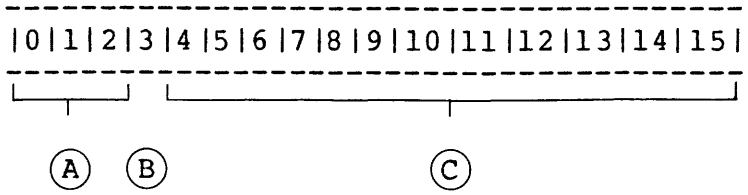
(E) Broadcast/Compare. Bits 8-11 when set to a logic 1 can be compared to specific functions of the broadcast or compare word that has been received.

Bit 8	Disable Service Request
Bit 9	Device End
Bit 10	Conditional Jump
Bit 11	Interrupt

(F) Tag Word. A tag word without a compare or broadcast bit will cause the following functions if the bits are set to a logic 1:

Bit 12	Disable Service Request
Bit 13	Device End
Bit 14	Conditional Jump
Bit 15	Interrupt

CF4

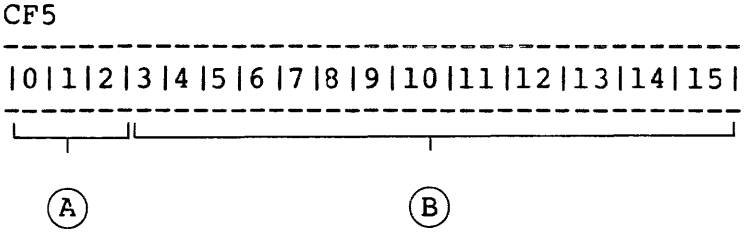


(A) Control function number. A control function 4 is a P I/O Reset function that resets circuits of the HSI PCA and generates a Clear Interrupt signal. It generates the same function as if the I/O Reset switch on the front panel were depressed. However, the reset function applies only to the HSI PCA for CF4.

(B) Bit three, when set, performs all of the above functions except DTR and RTS for all channels.

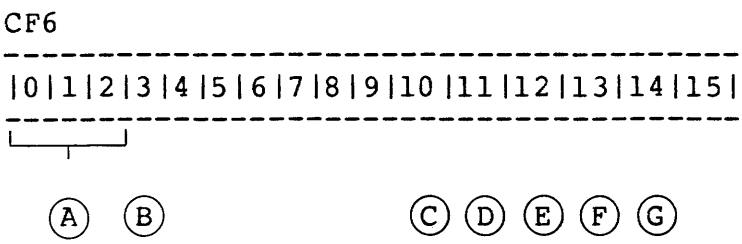
(C) Bit pattern is irrelevant.

CF5



(A) Control function number

(B) Bit pattern is irrelevant. A control function 5 will reset only the transmit-receive and CRC registers.



Ⓐ Control function number

Ⓑ Data Terminal Ready (DTR). A logic 1 asserts a DTR to the channel selected by CF0.

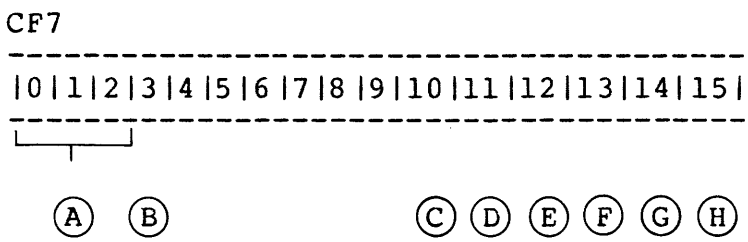
Ⓒ Interrupt. A logic 1 will cause an interrupt if there is no data transfer between the HSI PCA and the CPU within approximately 15 msec. Each data transfer resets the Time Out one-shot, preventing an interrupt from occuring.

Ⓓ SR Interrupt. A logic 1 allows a remote station to interrupt the CPU at the master station when a Service Valid (SRVAL) status signal is present.

Ⓔ CRC Error. A logic 1 causes an interrupt when a CRC error has been detected.

Ⓕ Acknowledge. A logic 1 causes the HSI PCA to operate in the acknowledge or handshake mode of operation.

Ⓖ Repeat Control. A logic 1 causes the HSI PCA to detect only tag words, and transmits the received word two bit-times later.



Ⓐ Control function number

Ⓑ Request To Send (RTS). A logic 1 asserts RTS to be sent to the channel selected by CF0.

Ⓒ Disable Transmit. A logic 1 disconnects the transmit line placing a logic 0 on the line. Used when short time-outs are to be programmed and an output is not desirable.

Ⓓ Enable Transmit Interrupt. A logic 1 will enable an interrupt to be generated from the leading edge of a write flag when the transmitter is ready for another word.

Ⓔ Accumulate CRC on Transmit. A logic 1 causes CRC to be accumulated while the transmit register is shifting. A logic 0 causes CRC to be accumulated when the receive register is shifting information.

Ⓕ Test CRC. A logic 1 causes a test of the CRC register to see if it is a logic 1 by outputting one dummy word and then checking CRC status for an error. The dummy word will be transmitted unless bit 10 is a logic 1.

Ⓖ Transmit CRC. A logic 1 commands the HSI PCA to transmit from the CRC register instead of from the transmit (data) register. Bit 14 will be a logic 1 when outputting the generated CRC or when checking the incoming CRC by transmitting a dummy word.

Ⓗ Tag. A logic 1 causes a 1 to be transmitted as a tag bit in the transmitted word, indicating the word is a control word when received at the station. A logic 0 in the tag bit position indicates the transmitted word is a data word rather than a control word.

3-35. SERVICE REQUEST AND INTERRUPT. The service request logic is used only when data transfers are controlled by the I/O program. The service request logic provides a DEV SR signal to the bus logic for transmission to the multiplexer channel for each of the following conditions:

a. The last command sent by either a PCMD1 or P CONT STB has been executed.

b. The HSI PCA has data ready to transfer to memory.

c. The HSI PCA is ready to receive data from memory.

d. When the transfer in or out operation is finished and the HSI PCA is ready for the next command.

3-36. The interrupt request circuits provide the Interrupt Request signal to the bus logic for transmission to the CPU. The CPU will then service the HSI PCA interrupt. An interrupt request can be initiated by six different conditions on the HSI PCA and the same conditions also provide status information for the status word.

a. Transfer Error. The multiplexer channel sends a T.F. ERR signal because of an error in data transfer between the HSI PCA and IOP.

b. I/O System Interrupt. A SET INT signal is initiated by the control circuits because of a programmed interrupt request.

c. Transfer Ready. The HSI PCA produces a R BUF RDY signal when it has a word in its buffer ready for transfer to memory and receives interrupt enable, a T BUF RDY signal when a word in the transmit buffer is ready for transmission and transmits interrupt enable.

d. Overrun. An OVRN signal is generated when a second word has been received before the first word was processed.

e. Status Change. When a remote station changes status and requires servicing, SRVAL is produced to handle the request.

3-37. Status Section

3-38. The status section contains the circuits that transfer the HSI PCA status to the IOP bus because of a TIO instruction. The status word is sent to one of three possible storage locations. The storage location is determined by the instruction used to fetch the 16-bit status word. A direct TIO instruction pushes the status word to the top of the stack. A microcode TIO instruction comes from assembling direct I/O commands such as WIO and RIO and results in sending the status word to scratch pad 2 in the CPU. I/O program orders, such as SENSE and END, store the status word in the second part of the same doubleword.

3-39. Table 3-2 illustrates the status word format and explains the significance of each bit in the word.

Table 3-2. HSI PCA Status Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Bit 0	SIO OK. A logic 1 indicates the HSI PCA is ready to execute an SIO program. A logic 0 indicates an SIO program is being executed.
Bit 1	Read/Write OK. A logic 1 indicates the receive or transmit section is not busy. Bits 3 and 4 are ORed to form this status bit.
Bit 2	Interrupt Pending. A logic 1 indicates a condition for an interrupt exists.
Bit 3	Read Buffer Ready. A logic 1 indicates the receive buffer has data present and is ready for processing.
Bit 4	Write Buffer Ready. A logic 1 indicates the write buffer is ready to receive more data.
Bit 5	Transfer Error. A logic 1 indicates a transfer error has occurred between the IOP and the HSI PCA.
Bit 6	Time Out. A logic 1 indicates the time-out generator has timed out after approximately 15 msec because of a lack of data transfer.
Bit 7	Service Request Valid (SRVAL). A logic 1 indicates that a Data Set Ready (DSR) input is asserted (positive) and that the Receive Data signal from the selected channel is in a high (space) state with receive enabled.
Bit 8, 9, and 10	Channel Service. Bits 9 and 10 indicate which channel (0-3) is requiring service. Bit 8 determines if the interrupt is from a DSR or Data-In condition (DSR = 0).
Bit 11	Sense. A logic 1 indicates one of the four channels is in service.
Bit 12	CRC Error. A logic 1 indicates an error exists after a CRC check is made.
Bit 13	Over-Run Error. A logic 1 indicates another word has been received before the first word was serviced.
Bit 14	Tag Bit Detected. A logic 1 indicates a tag bit has been detected.
Bit 15	Compare Detected. A logic 1 indicates that either a compare of the six bit address of a tag, or a broadcast bit has been detected.

3-40. **Receive Section**

3-41. The receive section (see figure 3-6) assembles the asynchronous serial data from the input/output select section into a 16-bit parallel word for transmission to memory via the bus logic. The receive word consists of twenty bits, one start bit, one tag bit, 16 data bits, and two stop bits (see figure 3-3). The second stop bit is not used, and only the 16-bit data word is sent to memory.

3-42. CF0 presets the Baud Counter to the bit-rate of the receive data with the CONT BIT RATE code. The Baud Counter is clocked by a 15 MHz Oscillator and the combined output clocks the REC SYNC FF in sync with the RECEIVE DATA. The Decade Counter counts at the receive bit rate and produces the RCLK OUT signal to the input/output select section, which is returned as the RCLK in signal. The RECEIVE DATA is clocked through the REC DATA FF into the Receive Register until the start bit sets the START FF, the 16 data bits will have been shifted into the Receive Register, and the first stop bit sets the REC DATA FF.

3-43. The Baud Counter and the 15 MHz Oscillator continue counting at a rate faster than the Decade Counter and sequentially clock the REC BUF and ASSOC DEC FF's set. Setting the ASSOC DEC FF issues a STAT CLK to the control section and also clocks the receive word from the Receive Register into the Receive Buffer. Bits 9 through 14 of the receive word are compared to the COMP DATA function of CF1 in the Address Comparator. When the bits compare, a COMPARE signal is generated and sent to the status section and to the Associate Function Decoder. The Decoder is strobed when a tag bit is present in the receive word. The Associate Function Decoder will decode the CONT REC FNC of CF3 if the tag bit was set, to determine the operation to be performed when the tag word compares. CF3 also determines the operation to be performed when the tag word does not compare. When a DSR (Disable Service Request) is programmed in CF3, it is gated to the READ RDY FF after the Baud Counter clocks the REC RESET FF set. The DSR signal sets the READ RDY FF, and sends a false READ BFR RDY signal to the control section so that a service request will not be generated by the HSI PCA. The DEVICE END, CONDITIONAL JUMP, and INTERRUPT signals decoded by the Associate Function Decoder are sent to the control section for processing. The conditonal jump, controlled by bits 10 and 14 of CF3, depends on the state of the SIO status bit (1 = jump met, 0 = jump not met).

3-44. When the tag bit in the receive word is not set, the information received is a data word, and a true READ BFR RDY signal is sent to the control section to indicate that a data word is present in the Receive Buffer, ready for servicing. Two RESET signals are generated (A and B) to reset the Receive Register and its associated circuits so that a second word can be received before the first word is transferred out to the bus logic.

3-45. When the REP CONT (repeat control) operation of CF6 is programmed, the RECEIVE DATA is clocked through the REC DATA FF and gated to the transmit section where it is transmitted two bit times later.

3-46. Transmit Section

3-47. The transmit section (see figure 3-7) assembles the 16-bit parallel transmission word from the bus logic into a 20-bit asynchronous serial word. See figure 3-3 for the word format.

3-48. The Transmit Register is loaded with the TRANSMIT DATA or CRC word by the P WRITE STB or D WRITE STB signal from the bus logic. The strobe signal also sets the T BUF RDY FF to update the status section indicating the Transmit Buffer is not ready for more data.

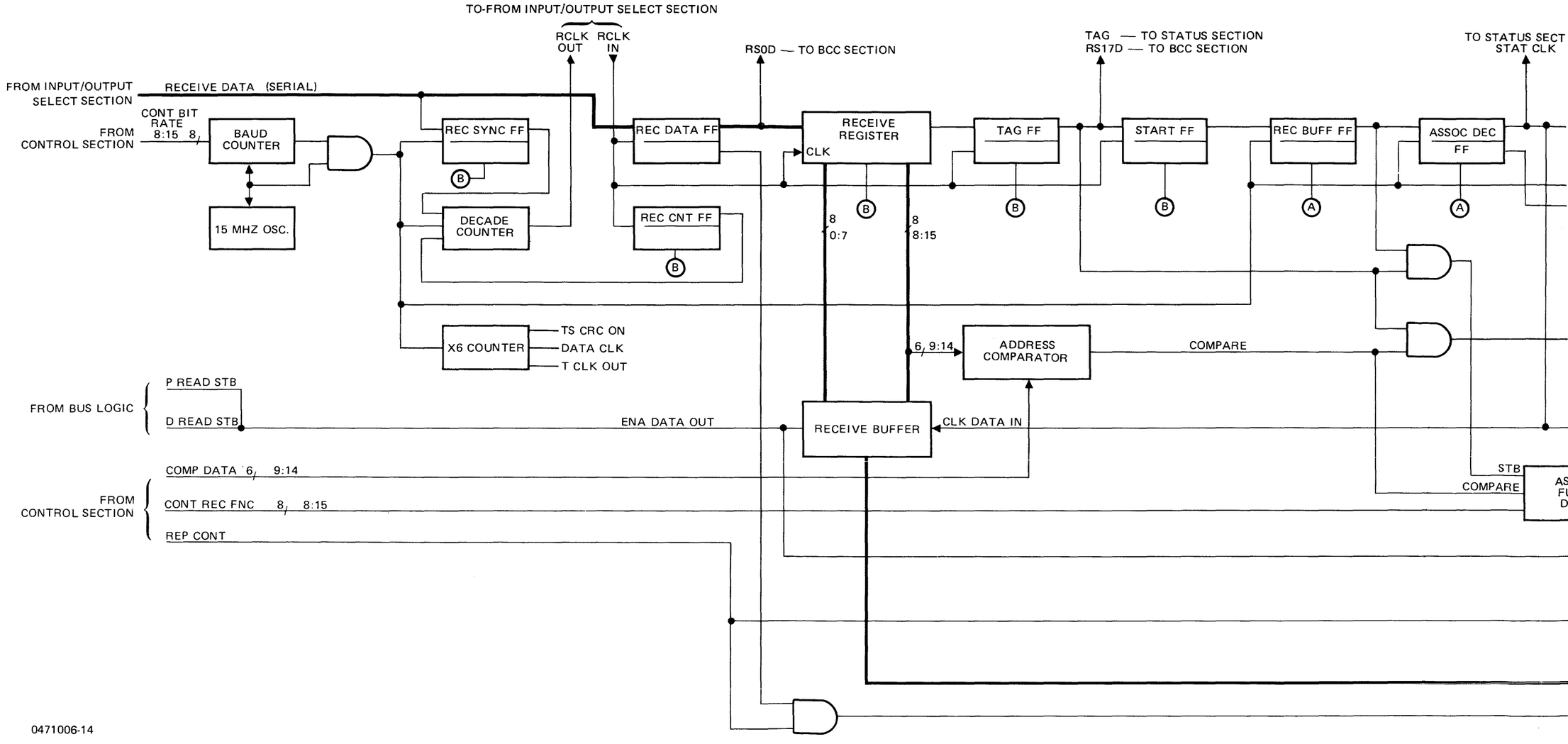
3-49. When the input/output select section returns the CTOS (Clear To Send) signal, the Transmit Counter is enabled to count the T CLK IN clocks. The data is serially shifted out of the Transmit Buffer as TRANSMIT DATA to the output select section for transmission on the selected channel. When the twentieth bit is shifted out of the Transmit Buffer, the T BUF RDY FF resets, indicating that the Transmit Buffer is ready for more data.

3-50. When CF6 activates the repeat data operation, the information from the receive section is applied to the Transmit Buffer as REPEAT DATA, and is transmitted two bit times later.

3-51. To transmit a control function rather than a data word, the control section activates the TAG TS signal and sets the tag bit of the transmitted word. TS CRC ON, TS CRC OFF, and TS19D signals are sent to the BCC section to accumulate a CRC word for the transmitted word.

3-52. Input/Output Select Section

3-53. The input/output select section (see figure 3-8) selects one of four channels (0-3) to transmit and receive data. Channel selection is determined by a two bit code contained in CF0. The input/output select section also detects interrupts from channels not selected, and allows the software to process these interrupts. The input/output select section routes the data between the coax cables and other functional areas of the HSI PCA.


TO-FROM INPUT/OUTPUT SELECT SECTION
RCLK OUT
RCLK IN
RS0D — TO BCC SECTION
TAG — TO STATUS SECTION
RS17D — TO BCC SECTION
TO STATUS SECT
STAT CLK
FROM INPUT/OUTPUT SELECT SECTION
RECEIVE DATA (SERIAL)
CONT BIT RATE 8:15 8
FROM CONTROL SECTION
BAUD COUNTER
15 MHZ OSC.
REC SYNC FF
DECADE COUNTER
REC DATA FF
REC CNT FF
RECEIVE REGISTER
CLK
TAG FF
START FF
REC BUFF FF
ASSOC DEC FF
8 0:7
8 8:15
X6 COUNTER
TS CRC ON
DATA CLK
T CLK OUT
6, 9:14
ADDRESS COMPARATOR
COMPARE
FROM BUS LOGIC
P READ STB
D READ STB
ENA DATA OUT
RECEIVE BUFFER
CLK DATA IN
COMP DATA 6, 9:14
FROM CONTROL SECTION
CONT REC FNC 8, 8:15
REP CONT
STB
COMPARE
0471006-14

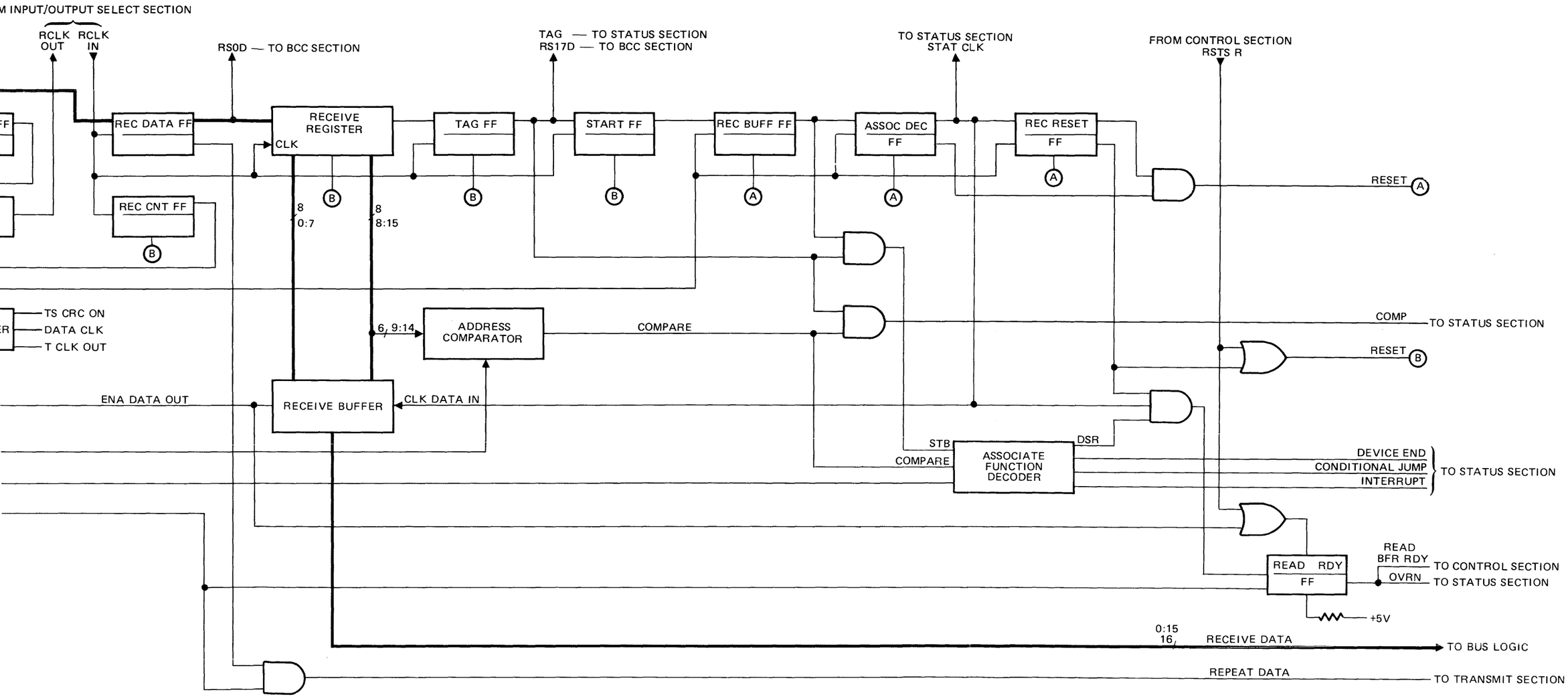


Figure 3-6. Receive Section

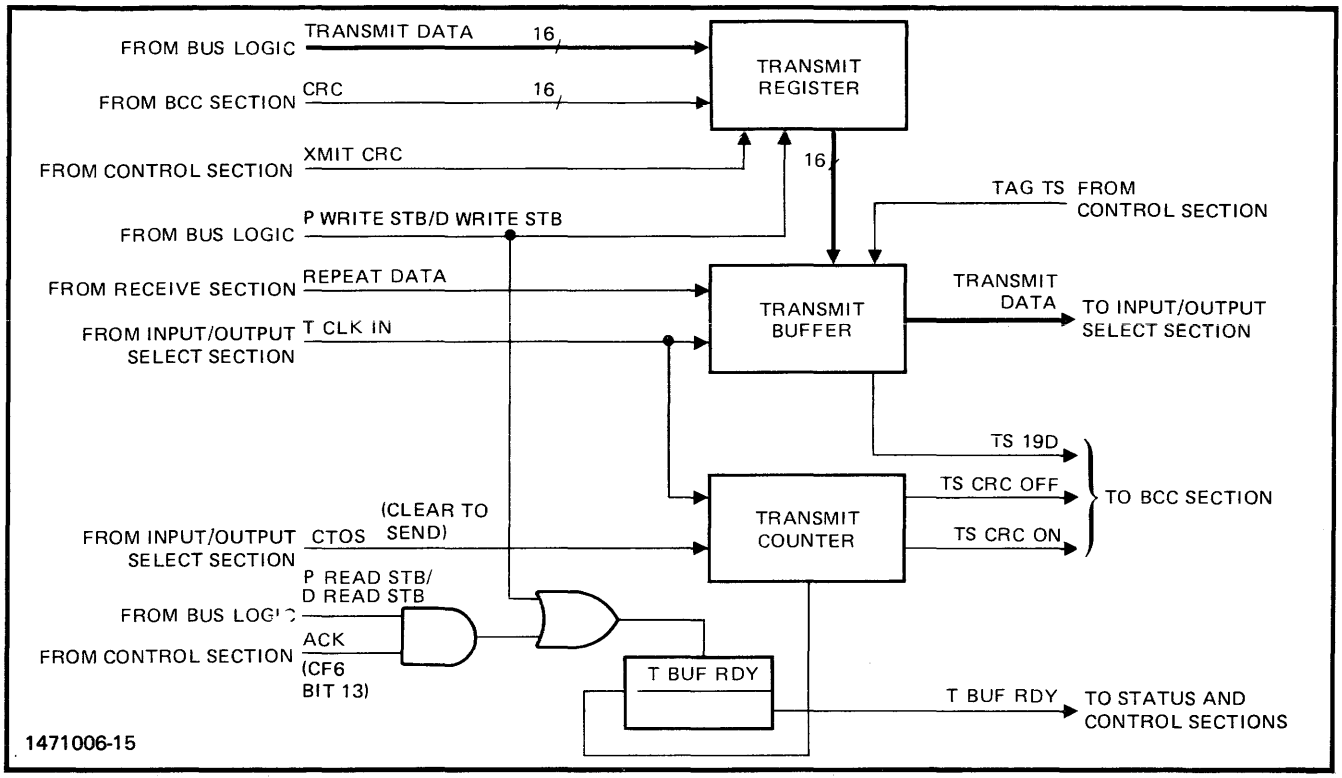


Figure 3-7. Transmit Section

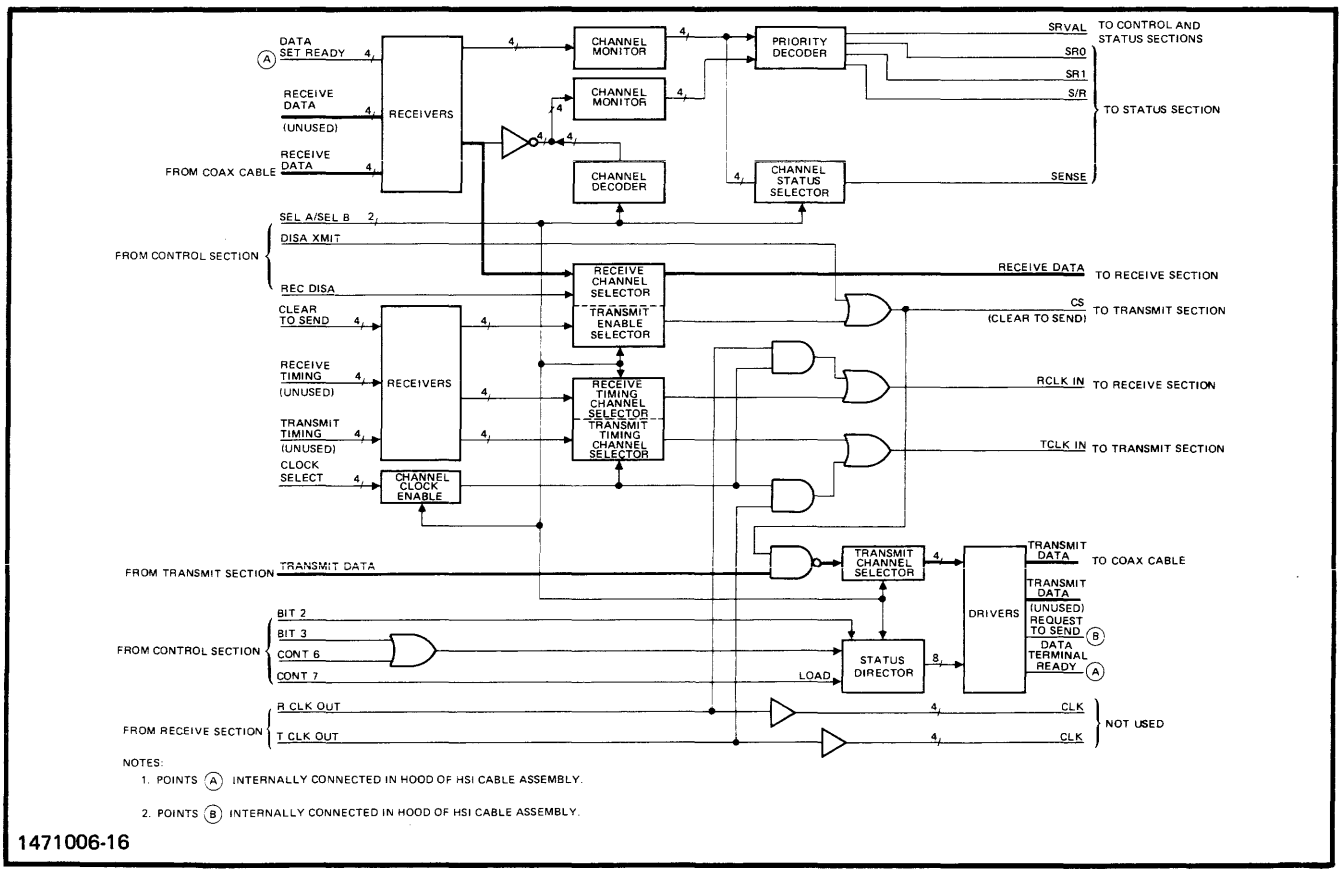


Figure 3-8. Input/Output Select Section

3-54. TRANSMIT. Prior to the actual transmission of data, an exchange of signals between the transmit and receive sections of the HSI PCA must occur. CF6 loads the Status Director with BIT 3 of the control word which is stored in a register selected by the combination of SEL A, SEL B (CF0), and BIT 2. The stored bit is a Data Terminal Ready signal that is sent through the Drivers on the selected channel. It is returned (via a jumper in P1 of the HSI cable assembly) as a Data Set Ready (DSR) signal through the Receivers and the Channel Monitor to the Priority Decoder and Channel Status Selector. The Priority Decoder encodes the number of the channel returning the DSR signal and sends four coded lines that signify a Service Request Valid (SRVAL) signal, which channel returned the DSR signal (coded as SR0 and SR1), and whether a send or receive process was attempted (S/R). The Channel Status Selector sends a SENSE signal to the status section to indicate that some channel is in service. SRVAL is sent to the control section to generate an interrupt and also to the status section along with the SR0, SR1, and S/R signals for a status update.

3-55. After the interrupt is processed, the Status Director is again loaded with BIT 3 of CF7 which is a Request To Send (RTS) signal. This signal is sent through the Drivers on the selected channel. It is returned (via a jumper in P1 of the HSI cable assembly) as a Clear To Send signal which goes through the Receivers to the Transmit Enable Selector.

3-56. RECEIVE. The receive operation of the input/output select section is very similar to the transmit operation. The channel containing the receive information is selected by CF0. The RECEIVE DATA is passed through the Receivers and the Receive Channel Selector before being sent to the receive section.

3-57. INTERRUPTS. Interrupts are initiated in the input/output select section by the Channel Monitors, Priority Decoder, Channel Status Selector, and Channel Decoder circuits. The Channel Decoder decodes the SEL A and SEL B signals of CF0 and activates the selected channel line. The Channel Monitors sense changes on their input lines and activate the Priority Decoder whenever another channel starts to send data, or the active channel drops the DATA SET READY signal. The Priority Decoder outputs a SRVAL signal, SR0 and SR1, and S/R signals. These signals are sent to update the status section and the SRVAL signal is also sent to the control section to generate an HSI PCA interrupt. Whenever a channel is in service, the SENSE signal is produced by the Channel Status Selector and it is send to the status section.

3-58. BCC Section

3-59. The Block Check Character (BCC) section (see figure 3-9) checks the transmitted or received data for errors using the Cylic-Redundancy Checking (CRC) method. The CRC circuits effectively divide the binary value of the message by a constant, discards the quotient and uses the remainder as the CRC word. CRC is accumulated over 16 bits of data, and does not include the start, tag, or stop bits.

3-60. The accumulated CRC word can be transmitted to the receive station which accumulates CRC on the received word. At the receive station, the CRC word is tested by shifting out the accumulated word. If a CRC error exists, the CRC word would be something other than zero, the status section would be updated, and an interrupt would be generated.

3-61. CF7 bit 12 controls the ACCUM CRC WRT RD signal that directs the Data Selector to select the transmit or receive inputs. The CRC CNT FF follows the input signal and clocks the word into the CRC accumulator.

3-62. CF7 bit 13 generates the TEST CRC signal to shift out the accumulated CRC word and enable the CRC ERR FF to set if the accumulated word contains something other than zero. CRC ERR is then sent to update the status section and to the control section to generate an interrupt. The CRC Accumulator provides the CRC word to the transmit section on 16 lines (CRC1 through CRC16).

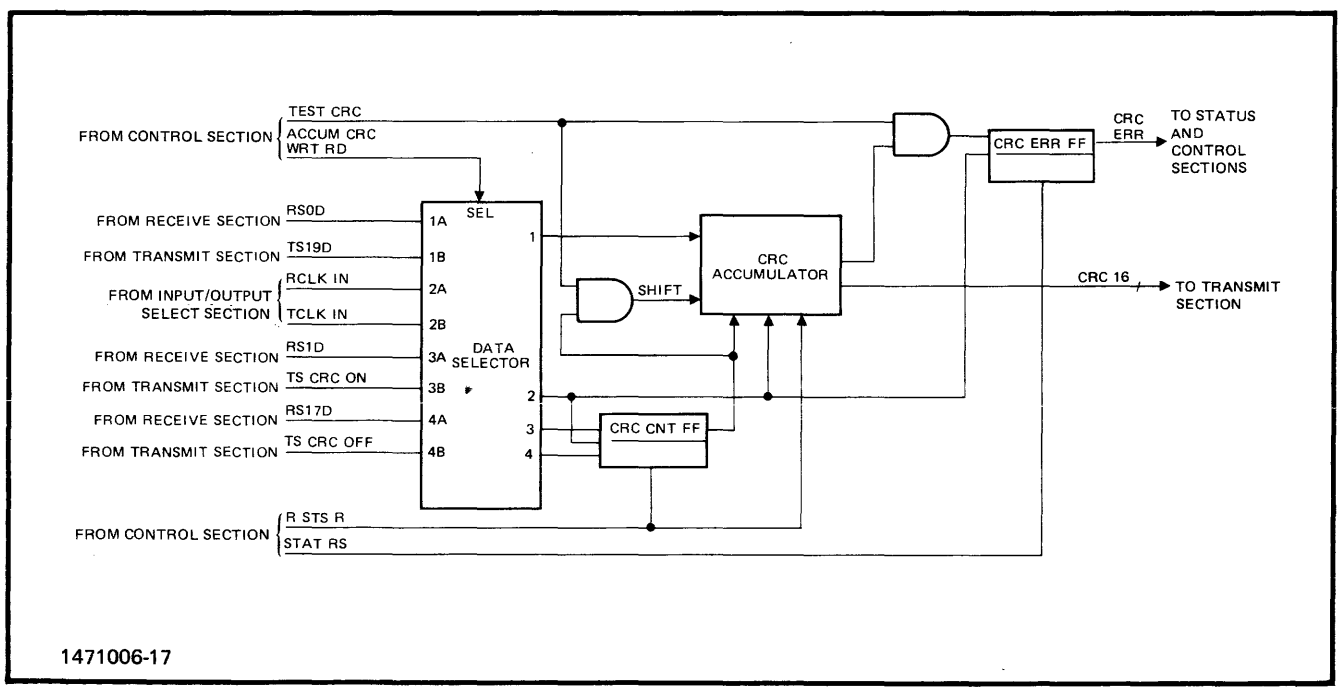


Figure 3-9. BCC Section

MAINTENANCE

SECTION IV

4-1. INTRODUCTION

4-2 This section contains general servicing information for the HSI PCA and HSI cable assembly. Included are some safety precautions, wiring and signal information, servicing equipment and principal servicing points, preventive and corrective maintenance information, troubleshooting information, the repair philosophy, and diagrams information.

4-3. GENERAL SERVICING INFORMATION

4-4. Paragraphs 4-5 through 4-21 contain servicing information that may be commonly referred to from other areas of this manual.

4-5. Safety Precautions

4-6. When performing maintenance on the HSI PCA and HSI cable assembly observe the following warning and caution.

WARNING

Dangerous voltages are present in the HP 3000 Computer System power control module and the cabinet ac distribution system. Use caution when working on the subsystem components installed in this bay. Observe all cautions and warnings placarded in the cabinet and included in this manual. Failure to heed the warnings could result in injury or death.

CAUTION

Before removing the HSI PCA from a card cage, set the SYSTEM DC POWER switch for the computer system to STANDBY. Failure to set the switch to STANDBY could damage the HSI PCA.

4-7. Wiring And Signal Information

4-8. Wiring and signal information for the HSI PCA and HSI cable assembly is provided in table 4-1 and figures 4-1 and 4-2. Table 4-1 provides a complete alphabetic listing of HSI PCA input and output signals. Figure 4-1 illustrates the numbering scheme used for the HSI PCA and its mating connector on the HSI cable assembly. Figure 4-2 provides a schematic representation of the HSI cable assembly.

4-9. Servicing Equipment

4-10. No servicing equipment is required for testing the HSI PCA and HSI cable assembly.

4-11. Principal Servicing Points

4-12. Principal servicing points for the HSI PCA are the edge connectors J1, J2, and J3. These connectors carry all of the signals transferred between the HSI PCA and the remote stations via the HSI cable assembly.

4-13. The HSI PCA and HSI cable assembly do not contain any fuses or adjustable controls.

4-14. Preventive Maintenance

4-15. Preventive maintenance for the HSI PCA and HSI cable assembly should be performed when the preventive maintenance routines for the HP 3000 Series II/III Computer System are performed. Preventive maintenance consists of inspecting the HSI PCA and HSI cable assembly for burned or broken components, loose connections, and deteriorated insulating materials.

4-16. Corrective Maintenance

4-17. Corrective maintenance, as applicable to the HSI PCA, is performed in the same manner as corrective maintenance for other printed-circuit assemblies in the HP 3000 Series II/III Computer System. No special procedures are required for the HSI PCA or HSI cable assembly.

4-18. Troubleshooting

4-19. The HSI PCA and HSI cable assembly may be checked using the Stand-Alone Hardwired Serial Interface Diagnostic (D432), manual part number 30360-90007. The NORMAL/TEST switches on the HSI cable assembly must be set to TEST during checking.

4-20. Repair Philosophy

4-21. The HSI PCA is not a field-repairable item, therefore, it must be maintained on an exchange basis. To verify proper operation, set each NORMAL/TEST switch on HSI cable assembly to TEST and perform the HP 30360A Hardware Serial Interface Diagnostic (D432), manual part number 30360-90007. If a manfunction is detected, the HSI PCA should be removed from the system and prepared for reshipment following the procedures contained in section II. Reset each NORMAL/TEST switch to NORMAL after testing.

Table 4-1. HSI PCA Input/Output Signals

MNEMONIC	CONN & PIN	SIGNAL NAME	FUNCTION
$\overline{\text{ACK SR}}$	P2-7	Acknowledge Service Request	Acknowledges receipt of a service request from the HSI PCA
C10 thru C13	J1-29,33,27, 31	Chan 0-3 Data Terminal Ready	Internally connected in hood of HSI cable assembly to simulate Data Set Ready signals.
C20 thru C23	J1-1, 7,3,5	Chan 0-3 Request to send	Internally connected in hood of HSI cable assembly to simulate Clear to Send signals.
$\overline{\text{CHAN ACK}}$	P2-9	Channel Acknowledge	Used during DEVICE END from multiplexer channel to HSI PCA to inform of an address transfer sequence
$\overline{\text{CHAN SO}}$	P2-1	Channel Service Out	Enables MUX CHAN bus gates on HSI PCA
CLK IN	J2-11	Clock Input	Clock Output signal internally connected in hood of HSI cable assembly to produce Clock Input signal
CLK OUT	J2-3	Clock Output	Clock output from programmable clock generator.
CLKR0 thru CLKR3	J3-35,31,37, 33	Chan 0-3 Receive Clock	Unused
CLKX0 thru CLKX3	J3-21,15,19, 17	Chan 0-3 Transmit Clock	Unused
CLR0 thru CLR3	J3-40,42,44, 46	Receive Clock Out	Unused
CLX0 thru CLX3	J3-48,50,49 47	Transmit Clock Out	Unused
CTOS	J2-41	Clear To Send	Starts transmit counter circuits
DATA CLK	J2-2	Data Clock	Unused
$\overline{\text{DATA CLK}}$	J2-5	$\overline{\text{Data Clock}}$	Unused
$\overline{\text{DEVNO 00}}$ thru $\overline{\text{DEVNO 07}}$	P3-8,9,11,12 14,15,17,18	Device Number 00 thru 07	HSI PCA device number
$\overline{\text{DEV END}}$	P2-5	Device End	Indicates termination of data transfer by HSI PCA
$\overline{\text{DEVNO DB}}$	P2-11	Device Number Data Bus	Causes HSI PCA to gate its DRT address (DEVNO x4) onto IOP data bus
$\overline{\text{EOT}}$	P2-13	End Of Transfer	Informs HSI PCA at end of a data transfer
$\overline{\text{INT ACK}}$	P3-50	Interrupt Acknowledge	HSI PCA informs IOP that INT POLL has been received and the HSI PCA DEVNO is on the line
INT POLL IN Sig Gnd	P1-48 P1-47	Interrupt Poll In	Polling signal to determine which interface PCA requested an interrupt

Table 4-1. HSI PCA Input/Output Signals (Continued)

MNEMONIC	CONN & PIN	SIGNAL NAME	FUNCTION
INT POLL OUT Sig Gnd	P1-44 P1-43	Interrupt Poll Out	Signal sent to next device in the polling sequence if HSI PCA has not requested an interrupt
$\overline{\text{INT REQ}}$	P3-44	Interrupt Request	Signals the IOP that the HSI PCA requests service
$\overline{\text{IOCMD}}$ 00,01, 02	P3-4,5,6	Input/Output Command bits 00, 01, 02	Command information from IOP to HSI PCA
$\overline{\text{IOD 00}}$ thru $\overline{\text{IOD 15}}$	P3-20,21,23, 24,26,27,29 30,32,33,35 36,38,39,41 42	Input/Output Data bits 00 thru 15	Input/Output data lines
$\overline{\text{IOD PRTY}}$	P3-1	Input/Output Data Parity	Odd parity bit
$\overline{\text{IORESET}}$	P1-11	Input/Output Reset	Reset to HSI PCA
$\overline{\text{JMP MET}}$	P2-14	Jump Met	Indicates that HSI PCA can proceed with a jump command
$\overline{\text{MCUCLKS}}$ Sig Gnd	P1-13 P1-14	Module Control Unit Clock	System clock signal line
$\overline{\text{P CMD 1}}$	P2-43	Program Command 1	Multiplexer channel tells HSI PCA to strobe in IOCW bits (4 thru 12)
$\overline{\text{P CONT STB}}$	P2-46	Program Control Strobe	Multiplexer channel tells HSI PCA to strobe in the IOAW
$\overline{\text{P READ STB}}$	P2-50	Program Read Strobe	Gates received data to IOP bus
$\overline{\text{P STAT STB}}$	P2-45	Program Status Strobe	Gates HSI PCA status to IOP bus
$\overline{\text{P WRITE STB}}$	P2-48	Program Write Strobe	Gates IOP bus data to HSI PCA transmit section
RCLK in	J2-7	Receive Clock Input	Unused
RCLK OUT	J2-1	Receive Clock Output	Unused
REC DATA	J2-37	Received Data	Unused
$\overline{\text{REQ}}$	P2-22	Request	Signals multiplexer channel to initiate its device controller RAM's
R0 thru R3	J3-45,41,43 39	Receive Data	Unused
R0' Ret R1' Ret R2' Ret R3' Ret	J3-30 J3-29 J3-28 J3-27 J3-26 J3-25 J3-24 J3-23	Receive Data	Data received from coax lines

Table 4-1. HSI PCA Input/Output Signals (Continued)

MNEMONIC	CONN & PIN	SIGNAL NAME	FUNCTION
S_{10} thru S_{13}	J3-9,7,13,11	Chan 0-3 Data Set Ready	Data Set Ready
S_{20} thru S_{23}	J3-3,2,5,1	Chan 0-3 Clear to Send	Clear To Send
SENSE	J2-39	Sense	Indicates a status change on some channel
$\overline{\text{SET INT}}$	P2-49	Set Interrupt	Causes HSI PCA to generate an interrupt to the CPU
$\overline{\text{SET JMP}}$	P2-44	Set Jump	Sets JUMP MET flip-flop if conditions met and returns JMP MET to multiplexer channel
SI Sig Gnd	P1-49 P1-50	Service In	Acknowledges receipt of SO signal
$\overline{\text{SIO ENABLE}}$	P2-12	Start Input/Output Enable	Indicates that multiplexer channel is in the system
$\overline{\text{SO}}$ Sig Gnd	P1-53 P1-54	Service Out	Indicates that direct I/O command and DEVNO are on the IOP bus. Also issued to initiate a data transfer during SIO program operation
$\overline{\text{SR0}}$ thru $\overline{\text{SR15}}$	P2-24 thru 29, 31 thru 35, 37 thru 41	Service Request 0-15	Indicates to multiplexer channel that HSI PCA wants service and has priority
ST0 thru ST3	J3-36,38,34 32	Chan 0-3 Clock Select	Selects internal or external clock
T_0 thru T_3	J1-19,21,25 23	Transmit Data	Unused
T_0' Ret T_1' Ret T_2' Ret T_3' Ret	J1-13 J1-14 J1-11 J1-12 J1-15 J1-16 J1-17 J1-18	Transmit Data	Data to be transmitted over coax cable
TCLK IN	J2-35	Transmit Clock Input	Unused
TCLK OUT	J2-9	Transmit Clock Output	Unused
TOGGLE IN XFER	P2-16	Toggle In Transfer	Read operation still in progress
TOGGLE OUT XFER	P2-18	Toggle Out Transfer	Write operation still in progress
TOGGLE SIO OK	P2-19	Toggle SIO OK	Toggles SIO OK flip-flop on HSI PCA during an End order

Table 4-1. HSI PCA Input/Output Signals (Continued)

MNEMONIC	CONN & PIN	SIGNAL NAME	FUNCTION
TOGGLE SR	P2-17	Toggle Service Request	Toggles SR flip-flop on HSI PCA during a Read, Write, or End order.
$\overline{\text{XFER ERROR}}$	P2-21	Transfer Error	Multiplexer channel informs HSI PCA that a parity error has occurred in the data transfer
+5V Ret	P1,2,3,4 J2-23,24 P1-15,16,19,20,29,30 J1-20,22,24,26 J2-27,28		
+15V	P1-21,22,23,24		
-15V	P1-25,26,27,28		
GND	P2-2,4,6,8,10,15,20,23,30,36,42 P3-3,7,10,13,16,19,22,25,28,31,34,37,40,43,46,49		

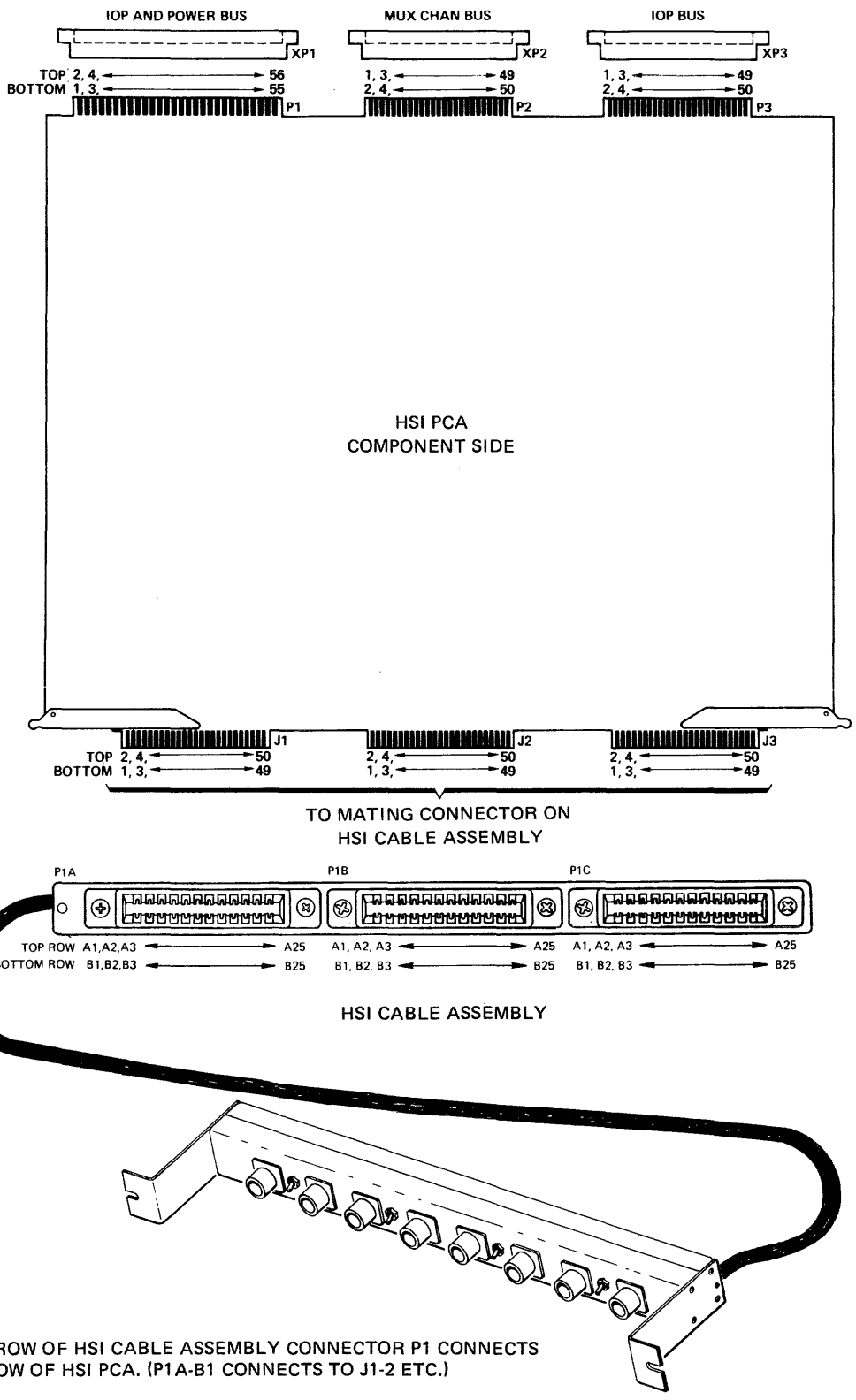
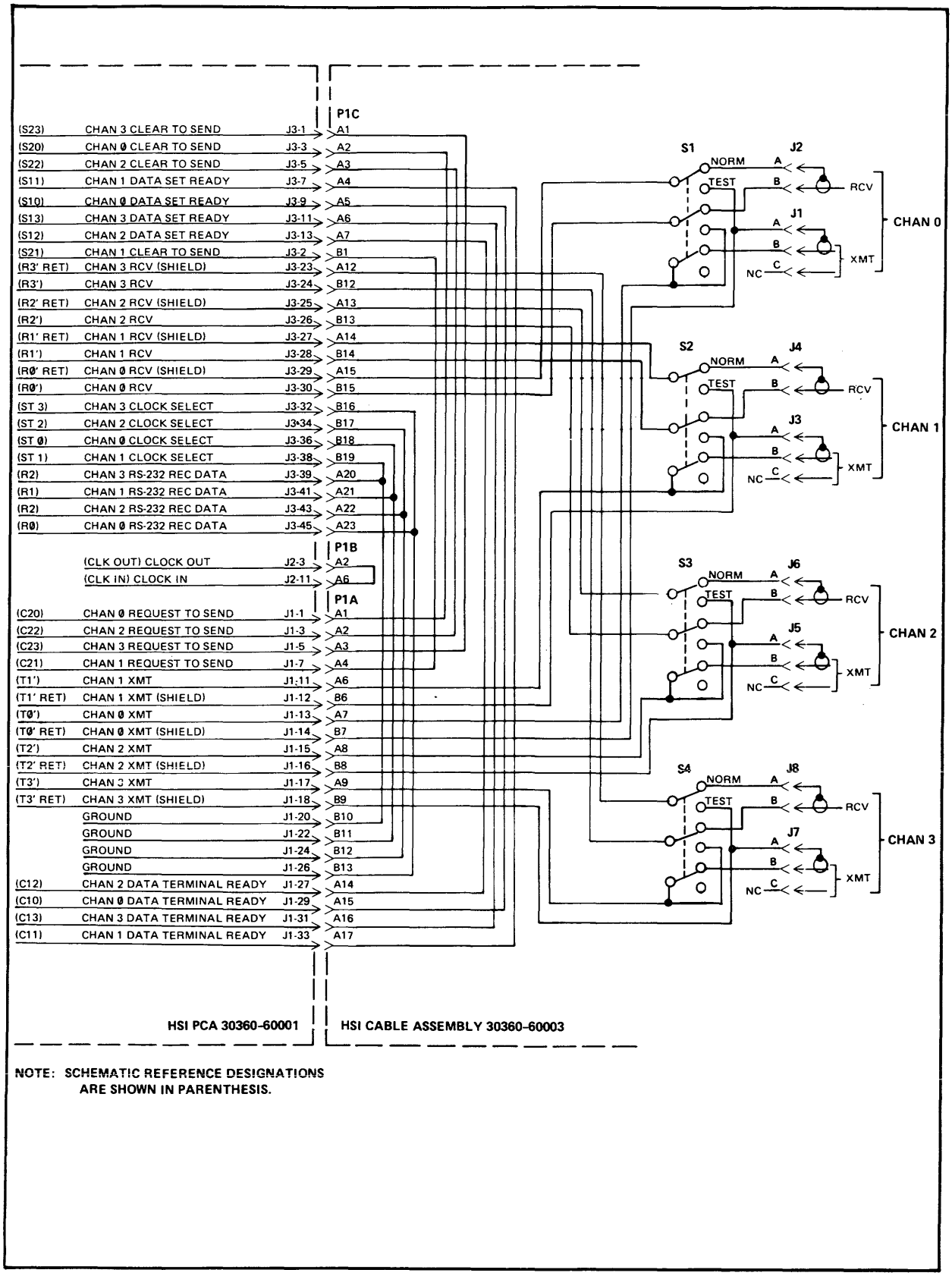


Figure 4-1. Connector Numbering Scheme



NOTE: SCHEMATIC REFERENCE DESIGNATIONS ARE SHOWN IN PARENTHESIS.

Figure 4-2. HSI Cable Assemmbly, Schematic Diagram

No technical change;
format change only.

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HP 30360A
HARDWIRED SERIAL INTERFACE
INSTALLATION AND SERVICE MANUAL
30360-90001 May 1979

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Are the concepts and wording easy to understand?	**Yes** ☐ **No** ☐	(If no, explain under Comments, below.)
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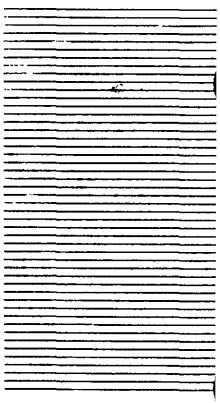

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