HEWLETT PACKARD

INSTALLATION AND SERVICE MANUAL

30032B ASYNCHRONOUS TERMINAL CONTROLLER

(For HP 3000 Computer Systems)

Manual Part No. 30032-90004
Microfiche Part No. 30032-90006

Printed in U.S.A. 1/74
Updates 1 and 2 Incorporated 2/77

Printed-Circuit Assemblies:

30032-60001
30061-60001
30062-60001
30062-60017

Options Covered

This manual covers options 001, 002, and 003 in addition to the standard HP 30032B Asynchronous Terminal Controller.

HEWLETT-PACKARD COMPANY
GENERAL SYSTEMS DIVISION
19447 PRUNERIDGE AVENUE
CUPERTINO, CA 95014

NOTICE

The information contained in this document is subject to change without notice.

HEWLETT-PACKARD MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance or use of this material.

LIST OF EFFECTIVE PAGES

The List of Effective Pages gives the most recent date on which the technical material on any given page was altered. If a page is simply re-arranged due to a technical change on a previous page, it is not listed as a changed page. Within the manual, changes are marked with a vertical bar in the margin.

Pages	Effective Date
Title	Jul 1976
ii	May 1976
iii	Jul 1976
iv	May 1976
v	May 1976
vi	Jul 1976
vii	May 1976
ix	Jul 1976
1-0	Jul 1976
1-1	Jan 1974
1-2	Jul 1976
1-3	Jul 1976
1-4	Jan 1974
2-1	Jan 1974
2-2	Jul 1976
2-3	Jan 1974
2-4 thru 2-9	Jul 1976
2-10 thru 2-12	Jan 1974
3-1	Jul 1976
3-2	Jan 1974
3-3	Jul 1976
3-4 thru 3-6	Jan 1974
3-7	Jul 1976
Blank	Jan 1974
3-9	Jan 1974
3-10	Jan 1974
3-11	Jul 1976
3-12 thru 3-14	Jan 1974
3-15	Jul 1976
3-16	Jul 1976
3-17 thru 3-19	Jan 1974
3-20	Jul 1976
3-21	Jan 1974
3-22	Jan 1974
3-23	Jul 1976
Blank	Jan 1974
3-25	Jan 1974
Blank	Jan 1974
3-27	Jan 1974
Blank	Jan 1974
3-29	Jan 1974
Blank	Jan 1974
3-31	Jan 1974
Blank	Jan 1974
3-33	Jan 1974
Blank	Jan 1974

Pages	Effective Date
3-35	Jan 1974
Blank	Jan 1974
3-37	Jan 1974
Blank	Jan 1974
3-39	Jan 1974
Blank	Jan 1974
3-41	Jan 1974
Blank	Jan 1974
3-43	Jan 1974
Blank	Jan 1974
3-45	Jan 1974
Blank	Jan 1974
3-47	Jan 1974
Blank	Jan 1974
3-49	Jan 1974
Blank	Jan 1974
3-51	Jan 1974
Blank	Jan 1974
3-53	Jul 1976
Blank	Jan 1974
3-55	Jan 1974
Blank	Jan 1974
3-57	Jan 1974
Blank	Jan 1974
4-0 thru 4-12	Jan 1974
4-13	Jul 1976
Blank	Jan 1974
4-15	Jan 1974
Blank	Jan 1974
4-17 thru 4-20	Jan 1974
4-21	Jul 1976
4-22	Jul 1976
4-23	Jul 1976
Blank	Jan 1974
4-25	Jan 1974
Blank	Jan 1974
4-27 thru 4-31	Jan 1974
Blank	Jan 1974
4-33	Jan 1974
Blank	Jan 1974
4-35 thru 4-41	Jan 1974
Blank	Jan 1974
4-43 thru 4-52	Jan 1974
4-53	Jul 1976
Blank	Jan 1974
5-1	Jul 1976
Blank	Jul 1976

PRINTING HISTORY

30032B

New editions incorporate all update material since the previous edition. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The date on the title page and back cover changes only when a new edition is published. If minor corrections and updates are incorporated, the manual is reprinted but neither the date on the title page and back cover nor the edition change.

First edition	1/74	
Update # 1	5/76	This update is for the purpose of referencing the HP 3000 Series II documentation.
Update # 2	7/76	This update is for the purpose of: a. incorporating 30062-60017 type Connector Panel. b. providing new model designators for modem, extender, and hardwired cables.
Updates 1 and 2 Incorporated	2/77	

This manual provides maintenance information for the HP 30032B Asynchronous Terminal Controller and options. This manual consists of four sections as follows:

a. Section I, General Information. This section provides a general description of the asynchronous terminal controller and options, including an equipment description, specifications, and PCA identification information.

b. Section II, Operating Parameters. This section describes the I/O instructions and commands that affect the asynchronous terminal controller and the related data, control, status, and parameter words. Signal lines between the asynchronous terminal controller and the terminals or data sets are also described in this section.

c. Section III, Theory of Operation. This section contains the general and detailed theory of operation of the asynchronous terminal controller, supported by overall block diagrams and simplified logic diagrams.

d. Section IV, Maintenance. This section provides maintenance data including safety precautions, preventive maintenance information, wiring diagram, and signal indexes. Timing diagrams and flowcharts in this section illustrates the operation of the asynchronous terminal controller at the functional level.

This manual is intended for use along with the operation and maintenance documentation for the terminals and/or data sets controlled by the asynchronous terminal controller. Additional information on the HP 30032B Asynchronous Terminal Controller is also available in the related documentation for the HP 3000 Series II/III Computer System or the pre-series II HP 3000 Computer System. The related documentation for the HP 3000 Series II/III Computer System includes the following:

a. HP 3000 Series II Computer System Service Manual, part no. 30000-90018.

b. HP 3000 Computer Systems Support Log, part no. 03000-90117;

c. HP 3000 Series II Computer System Installation Manual, part no. 30000-90019.

d. HP 3000 Series III Computer System Installation Manual, part no. 30000-90147.

Related documentation for the pre-Series II HP 3000 Computer System includes the following:

a. HP 3000 Detailed Diagrams Manual, part no. 03000-90023, set numbers 507 and 509.

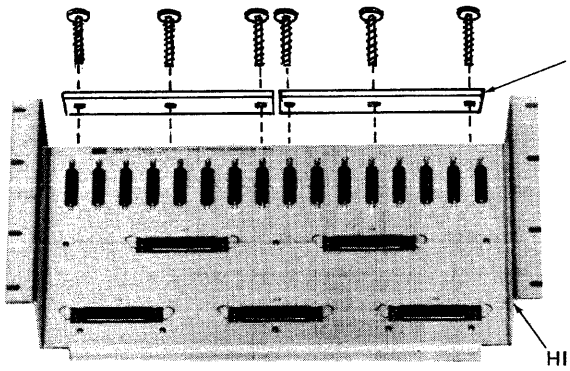
b. HP 3000 Illustrated Parts Breakdown (IPB) Manual, part no. 03000-90021.

CONTENTS

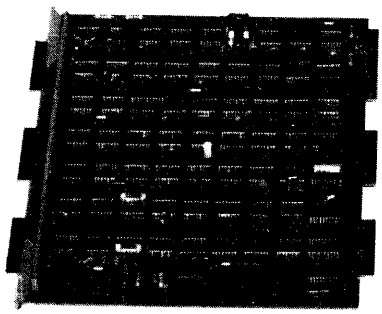
CONTENTS (Continued)

ILLUSTRATIONS

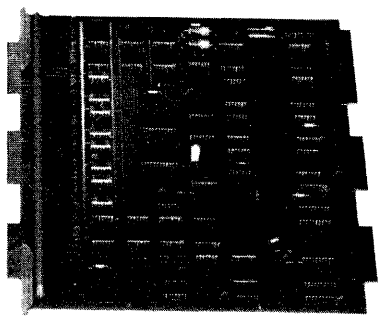
TABLES



CONNECTOR PANEL*
30062A
(30062-60017)

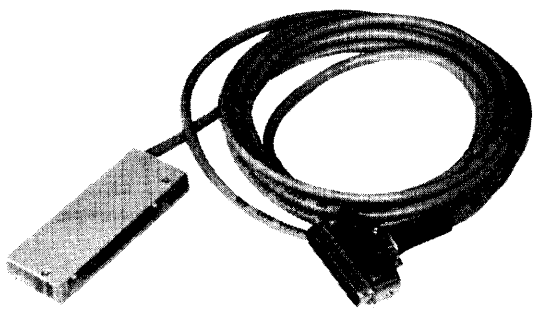


TERMINAL DATA INTERFACE PCA
30032-60001

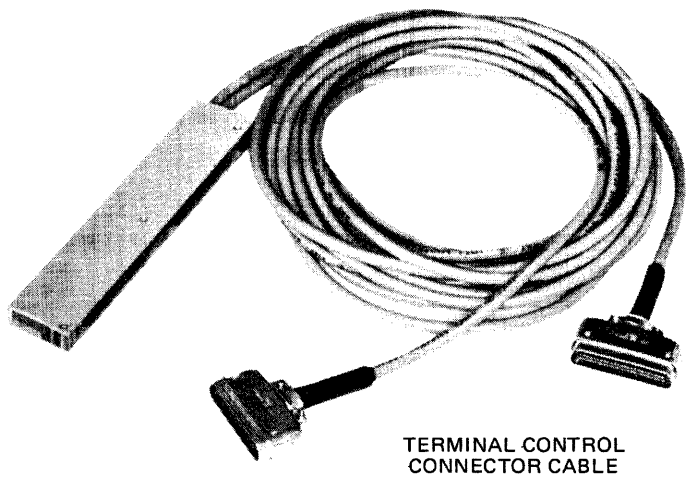


TERMINAL CONTROL INTERFACE PCA
30061-60001

TEST CABLE
30062-60003



TERMINAL DATA
CONNECTOR CABLE
30060-60003



TERMINAL CONTROL
CONNECTOR CABLE
30061-60003

* AN EARLIER VERSION 30062-60002 WAS WITHOUT HINGE AND STRAIN RELIEF BRACKETS.

2249-24

Figure 1-1. HP 30032B Asynchronous Terminal Controller

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This section contains the general description, option data, equipment description, cabling information, specifications, and means of identification for the HP 30032B Asynchronous Terminal Controller (figure 1-1). Included in this section are descriptions of the major components of the controller and permissible hardware configurations.

1-3. GENERAL DESCRIPTION.

1-4. The HP 30032B Asynchronous Terminal Controller for the HP 3000 Computer System is a control interface for low-speed bit-serial devices. The HP 30032B can control data transfers over a total of 37 channels, 16 send, 16 receive, and 5 special-purpose receive-only. The 16 send and 16 receive channels are separately programmable as to baud rate and character size to accommodate full-duplex and split-speed devices. The 5 receive-only channels are also fully programmable but are available for internal diagnostic purposes only and have no external interface capability. All operations are under direct I/O control of the CPU/IOP.

1-5. The 16 send channels have data transfer rates programmable from 75 to 2400 bits per second. Send channel character sizes are programmable from 5 to 12 bits per character including start, stop, and data bits.

1-6. The 16 receive channels are similarly programmable to data transfer rates from 75 to 2400 bits per second. However, the programmable character size range is from 5 to 11 bits per character including start, stop, and data bits. Only in special applications that do not require break-condition detection can a 12-bit character be received. The stop bit will not be detected and a break condition cannot be verified.

1-7. The basic configuration of the HP 30032B Asynchronous Terminal Controller provides full-duplex I/O transfers for up to 16 hardwired bit-serial terminals such as teletypes, card readers, visual display terminals, or similar devices; or any combination of the above totalling 16 devices. The HP 30032B-001 option extends subsystem capability to data handling and transfers for up to 16 type 103 data sets and hardwired devices. The HP 30032B-002 option provides data control and handling for up to 16 type 202 data sets or eight type 801 automatic dialing units or hardwired devices.

1-8. EQUIPMENT DESCRIPTION.

1-9. The HP 30032B Asynchronous Terminal Controller has three primary components: the terminal data interface PCA, the terminal control interface PCA, and the connector panel.

1-10. TERMINAL DATA INTERFACE PCA.

1-11. The terminal data interface (TDI) accepts and stores parameters such as baud rate, character size, parity, etc, for each of the 37 channels. The terminal data interface also maintains and controls the 16 data-out lines to the devices, the 16 data-in lines from the devices to the CPU/IOP, and the inputs to the five diagnostic channels. For a send channel, the TDI accepts direct I/O commands, stores the parameters specified for that channel, accepts and temporarily stores parallel data to be output to that channel, puts this data on-line to the device on that channel at the required rate, and generates an interrupt at the completion of character transmission. For a receive channel, the TDI accumulates bit-serial data received from a device into characters and generates an interrupt when a complete character is ready for transfer. The TDI also maintains status for all channels available on demand by the CPU. The start bit (space) of each character and the stop bit(s) (mark) are the sole means recognized by the TDI to control character transfers. The TDI can service 16 hardwired devices if those devices require no control lines other than the data-in and data-out lines.

1-12. TERMINAL CONTROL INTERFACE PCA.

1-13. The terminal control interface (TCI) PCA is required for all data set applications to provide and monitor the necessary control and status signals to operate up to 16 type 103 data sets. (Two terminal control interface PCA's are required to operate up to 16 type 202 data sets or up to eight type 801 automatic dialing units.) The TCI accepts direct I/O control words from the CPU/IOP that contain internal function commands and device status and control signals. The TCI stores the current status of device control signals, sequentially scans the status and control lines of each channel, compares the values with those stored, and generates an interrupt to the CPU/IOP when a change is detected.

1-14. CONNECTOR PANEL.

1-15. The connector panel is a PCA mounted at the rear of the equipment rack. This connector panel is the termination point of five 50-pin cables from the computer and sixteen 25-pin connectors from the data sets or hardwired devices. In all cases except type 801 automatic dialing units, up to 16 cables are connected directly from the connector panel to the associated devices. The connector panel jacks are designated J0 through J15 to correspond to device I/O channel numbers 0 through 15.

1-16. For type 801 automatic dialing units, the cables for up to eight data sets are connected directly to the connector panel using the even-numbered connectors. All

even-numbered connectors carry the data, control, and status lines for the assigned channel as well as several control and status lines for the subsequent odd-numbered channel. For instance, connector J0 carries all the signals required for channel 0 plus several lines for channel 1. Connector J1 carries signals for channel 1 only. Connector J2 carries signals for channels 2 and 3, while connector J3 carries signals for channel 3 only, and so on. Since type 801 automatic dialing units require more control lines than one channel provides, each unit utilizes an even-numbered channel plus the next odd-numbered channel. Any mix of devices can be achieved keeping this in mind.

1-17. EQUIPMENT SUPPLIED.

1-18. Table 1-1 shows the major components supplied with the HP Asynchronous Terminal Controller (ATC) and its option -001 and -002. The -003 option of the table furnishes the components listed if option -152 of the HP 30409A Upgrade Kit is specified. The Upgrade Kit converts an existing pre-Series II system to a modified Model 9 version of the Series II Systems. Option -152 is specified where it is necessary to replace a 30060-60001 Terminal Data Interface of an HP 30032A Asynchronous Terminal Controller with a 30032-60001 Terminal Data Interface of the Series II HP 30032B. (The 30032-60001 Terminal Data Interface is a component of option -152 and not of option -003 in table 1-1.) Table 1-2 lists the manuals furnished for both pre-Series II and Series II.

1-19. EXTENDER AND DATA SET CABLES.

1-20. The cables required to interconnect data sets or terminals to the controller connector panel depend entirely upon the number and type of terminals or data sets. The extender and data set cables available and recommended for use with the asynchronous terminal controller are as follows:

a. Type 103 and 202 Data Set cables

The 30062B Modem Cable consists of 25-foot cable part No. 30062-60004.

The 30062B-001 Modem Cable consists of 50-foot cable part No. 30062-60007.

b. Device extender cables

The 30062C Extender Cable consists of 25-foot cable part No. 30062-60006.

The 30062C-001 Extender Cable consists of 50-foot cable part No. 30062-60009.

The 30062C-002 Extender Cable consists of 100-foot cable part No. 30062-60012.

c. System console hardwired cable

The 30062D Hardwired Terminal Cable which consists of 25-foot cable part No. 30062-60018 is furnished to hardwire the system console to J0 of the HP 30062A Connector Panel. If there are more than one connector panel, it connects to J0 of the one with the lowest I/O system device number.

Table 1-1. Equipment Supplied

DESCRIPTION	PART NUMBER	HP 30032B	-001	-002	-003
Terminal Data Interface PCA	30032-60001	1	1	1	—
Terminal Control Interface PCA	30061-60001	—	1	2	—
Terminal Connector Panel (new hinged version) or	30062-60017	1	1	1	1
Terminal Connector Panel (original)	30062-60002	1	1	1	—
TDI PCA Connector Cable	30060-60003	1	1	1	1
TCI PCA Connector Cable	30061-60003	—	1	2	—
Test Cable	30062-60002	1	1	1	1

*30062-60002 is no longer available.

Table 1-2. Manuals Supplied

DESCRIPTION	PART NUMBER	HP 30032B	-001	-002
PRE-SERIES II				
Maintenance Manual	30032-90004	1	1	1
Detailed Diagrams Manual DD-507	30032-90002	1	1	1
Detailed Diagrams Manual DD-509	30061-90002	—	1	1
On-Line Terminal Data Interface Test	30060-90003	1	1	1
On-Line Terminal Control Interface Test	30061-90002	—	1	1
SERIES II				
Maintenance Manual	30032-90004	1	1	1
Stand-Alone Terminal Data Interface Test	30032-90011	1	1	1
Stand-Alone Terminal Control Interface Test	30061-90003	—	1	1

1-21. For certain device/cable configurations, noise pickup on status lines must be taken into account. In such cases, unused lines must not be permitted to float and must be either driven, tied high, or tied low. (See tables 4-1 through 4-4A for PCA and cable signal indexes.)

1-22. SPECIFICATIONS.

1-23. Specifications and characteristics of the HP 30032B Asynchronous Terminal Controller are presented in table 1-3.

1-24. IDENTIFICATION.

1-25. Printed-circuit assemblies (PCA's) are identified by a part number etched on the PCA. Revisions to the PCA are identified by a letter, a four-digit series code, and a two-digit division code marked beneath the part number on the PCA. The letter identifies the revision of the etched trace pattern on the unloaded PCA. The four-digit series code pertains to the electrical characteristics and positions of components on the PCA. The two-digit division code identifies the division of Hewlett-Packard that manufactured the PCA.

Table 1-3. Asynchronous Terminal Controller Subsystem Specifications

INTERFACE PRINTED-CIRCUIT ASSEMBLIES	
Power Requirements:	
30032-60001	+5V 3.25A -5V 100 mA +15V 70 mA -15V 105 mA
30061-60001	+5V 1.5A -5V 0 +15V 85 mA -15V 210 mA
Logic Levels:	
To and from CPU/IOP :	
"1" State	+0.4V (maximum)
"0" State	+3.0V (minimum)
To Data Set :	
Control Lines / Data Lines	
"1" State / "0" State	+7V ± 3V @ 2 mA
"0" State / "1" State	-7V ± 3V @ 2 mA
From Data Set :	
Status Lines / Data Lines	
"1" State / "0" State	+ 3V @ 1 mA (minimum) +15V @ 5 mA (maximum)
"0" State / "1" State	- 3V @ 1 mA (minimum) -15V @ 5 mA (maximum)
Signal Interfacing from IOP Bus and Interface Cable:	TTL output drivers and receivers
INTERFACE CABLES	
30060-60003 Cable:	
Type of connectors:	
Interface PCA	50-pin female
Connector Panel	50-pin male
Number of conductors:	36
30061-60003 Cable:	
Type of connectors:	
Interface PCA	100-pin female
Connector Panel	Two 50-pin male connectors
Number of conductors:	72

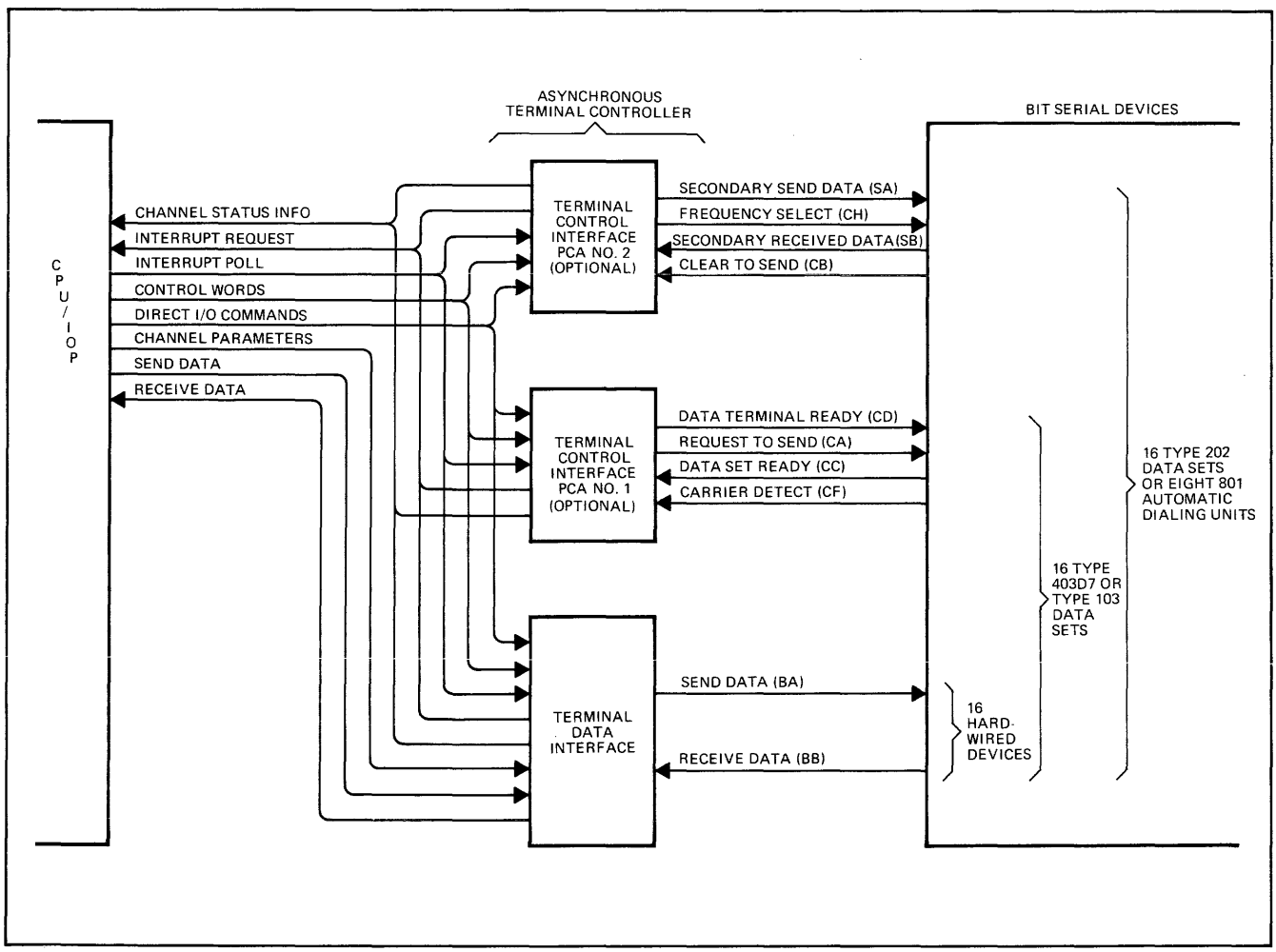
SECTION II OPERATING PARAMETERS

2-1. INTRODUCTION.

2-2. This section contains information regarding the HP 30032B Asynchronous Terminal Controller as a control interface and means of bidirectional data transfer between the HP 3000 Computer System and peripheral devices. This information includes a description of system parameters; a description of the direct I/O instructions as they pertain to subsystem functions; descriptions of the control, status, parameter, and data word formats exchanged between the asynchronous terminal controller and the computer system; descriptions of the control signals between the asynchronous terminal controller and peripheral devices; and descriptions of the means and types of interrupts generated by the subsystem.

2-3. GENERAL INFORMATION.

2-4. There are two functional components of the asynchronous terminal controller that are physically and functionally independent: the terminal data interface (TDI) and the terminal control interface (TCI). (See figure 2-1.) These components interface with the HP 3000 Computer System under direct I/O control via parallel transfers on the IOP bus. These components also generate and monitor control signals for up to 16 bit-serial peripheral devices (TCI PCA) and provide asynchronous, simultaneous, bidirectional, bit-serial data transfers for these peripherals which may have varying bit rates and character lengths (TDI PCA). Each PCA contains unique interrupt logic and accepts unique word formats. Each PCA also contains a group interrupt mask jumper and device address number assignment jumpers.



2249-9

Figure 2-1. Asynchronous Terminal Controller Subsystem Block Diagram

2-5. SYSTEM PARAMETERS.

2-6. The asynchronous terminal controller PCA's are controlled by direct I/O instructions. These instructions are executed after a sequence of events from the user program through the operating system to the I/O driver. The user initially makes a file request to the file system which ascertains that the file is associated with a terminal. The file system passes the request to the terminal processor. This system intrinsic contains direct I/O instructions which initialize the asynchronous terminal controller PCA's with the correct parameters for the type of device connected to the controller. Status conditions are checked on the TCI to make sure that the data sets are in the correct mode. Then the user program advances to the wait function.

2-7. Initialized to send or receive, the TDI interrupts and the CPU hardware automatically vectors execution to the Interrupt routine. This routine contains additional direct I/O instructions which send or receive characters. After each interrupt, the interrupt routine exits back to the Dispatcher. If the transfer is not complete, the Dispatcher returns control to the interrupted process. When the interrupt routine decides that the transfer is complete, it exits through the Dispatcher back to the terminal processor. This either starts a new transfer or exits back to the file system.

NOTE

The DEVAD mnemonics of this manual are the same signals as the DEVNO mnemonics used in most other documentation.

2-8. The wait function halts user program execution. The user program advances to this function when a transfer of characters is initiated. User program execution remains at the wait function until transfer of characters is complete or some channel status changed.

2-9. Each direct I/O instruction causes a three-bit I/O command (IOCMD), a seven-bit device address (DEVAD), and a Service Out (SO) signal to be placed on the IOP bus. The IOCMD specifies the operation to be performed. The DEVAD alerts the appropriate subsystem (in this case one of the two asynchronous terminal controller PCA's). The SO indicates to the addressed PCA that a valid command requiring attention is on the IOP bus. Receipt of this command is acknowledged by the addressed PCA by returning a Service In (SI) signal to the CPU/IOP via the IOP bus. Table 2-1 provides a summary of the direct commands used by the asynchronous terminal controller. Most of these commands require that a 16-bit word be transferred between the CPU and the subsystem. Table 2-1 states this requirement as applicable and provides a reference to a figure showing the content and format of the applicable word.

2-10. CIO INSTRUCTION.

2-11. The CIO instruction is recognized by both the TDI and TCI PCA's. The CIO instruction causes three CIO command bits, the eight-bit DEVAD, and SO to be placed on the IOP bus and a 16-bit control word to be sent from the top-of-stack (TOS) register in the CPU to the IOP bus. When either the TDI or TCI decodes the IOCMD and accepts the control word, an SI is returned to the CPU/IOP to acknowledge the instruction.

Table 2-1. Direct Command Bit Configuration/Summary

COMMAND	IOCMD 0	IOCMD 1	IOCMD 2	DESCRIPTION
TIO	0	1	0	Test I/O. Transfers 16-bit status word from subsystem to the CPU (figures 2-3 and 2-8).
CIO	1	1	0	Control I/O. Transfers 16-bit control word (TDI and (TCI) from the CPU to the subsystem (figures 2-2 and 2-7).
RIO	0	0	0	Read I/O. Transfers 16-bit data word (TDI) or status word (TCI) from the subsystem to the CPU (figures 2-5 and 2-8).
WIO	1	0	0	Write I/O. Transfers 16-bit parameter or data word from the CPU to the subsystem (TDI only, figures 2-4 and 2-6).
SMSK	0	0	1	Set Mask. Transfers 16-bit mask word to all I/O subsystems.
SIN	1	1	1	Set Interrupt. Sets the subsystem interrupt logic and status word interrupt bit (TDI and TCI).
RESET INT	0	1	1	Reset Interrupt. Clears the subsystem interrupt logic and status word interrupt bit (TDI and TCI).

2-12. RIO INSTRUCTION.

2-13. For the TDI, an RIO instruction causes first a TIO command, DEVAD, and SO to be placed on the IOP bus to see if the TDI is available for a read operation. If the status word indicates that the TDI is available, the CPU/IOP then places an RIO command, DEVAD, and SO on the IOP bus. This command strobes a data word and channel address from the TDI up-address and data-in buffers to the computer system memory. For the TCI, an RIO command on the IOP bus performs the same function as a TIO command - strobes a status word onto the IOP bus from the TCI to the CPU/IOP.

2-14. TIO INSTRUCTION.

2-15. The TIO instruction causes a TIO command that is recognized by both PCA's. The command causes a 16-bit status word to be strobed from the PCA onto the IOP bus and sent to the TOS register in the CPU/IOP.

2-16. WIO INSTRUCTION.

2-17. The WIO instruction causes a WIO command that is recognized only by the TDI. During WIO instruction execution, a TIO command, DEVAD, and SO are placed on the IOP bus to determine if the TDI is available for a write operation. If the status returned indicates that such is the case, a WIO command, DEVAD, and SO, and a 16-bit parameter or data word from CPU/IOP TOS are put on the IOP bus for the TDI.

2-18. SIN INSTRUCTION.

2-19. This instruction is recognized by both the TDI and TCI and causes the addressed PCA to request an interrupt.

2-20. SMSK INSTRUCTION.

2-21. The SMSK instruction is recognized by both the TDI and TCI. This instruction sends a 16-bit mask word from the TOS register in the CPU/IOP to all PCA's of a mask group to enable interrupts. The mask group for the TCI and TDI is determined by the location of the group interrupt mask jumper on each PCA.

2-22. EXIT INSTRUCTION.

2-23. This instruction is the last instruction of the TDI and TCI interrupt routines. During execution of EXIT, the CPU/IOP generates an RST INT command that clears interrupt logic on the applicable PCA.

2-24. TDI I/O INSTRUCTIONS.

2-25. The controller TDI accepts control, parameter, and output data words from the CPU/IOP under CIO and WIO instructions and returns status and input data words under TIO and RIO instructions. The following paragraphs present the word formats and word bit definitions for the exchanges between the CPU/IOP and the TDI.

2-26. CONTROL WORD FORMAT.

2-27. The control word is a 16-bit word sent from the CPU to the TDI during execution of direct command CIO. A control word must follow every WIO instruction and is also used to initialize TDI logic. Figure 2-2 shows the TDI control word format.

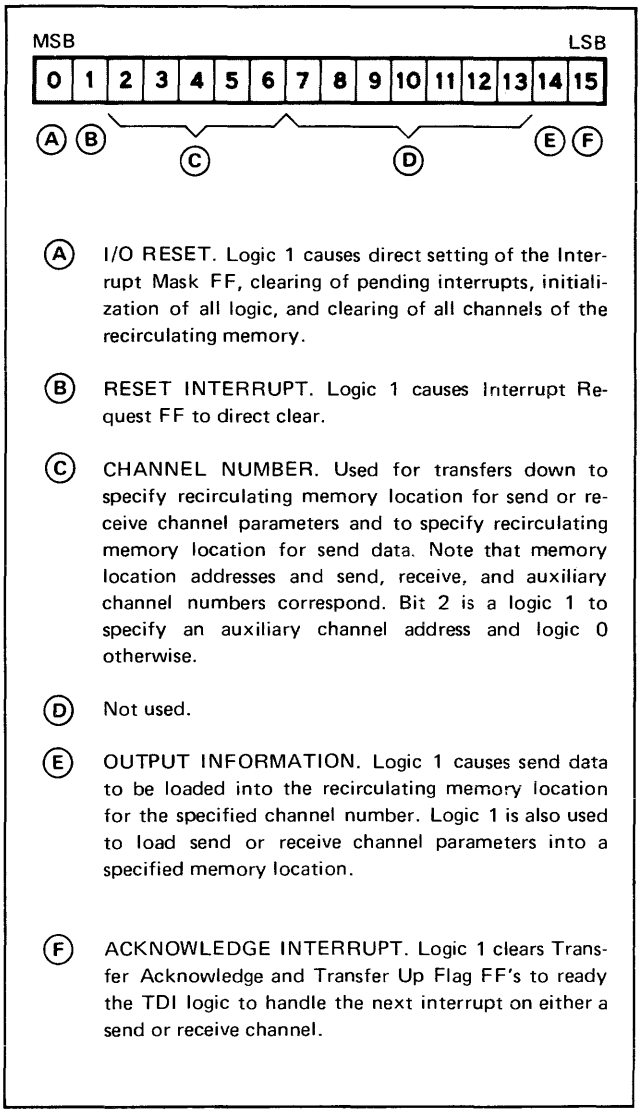


Figure 2-2. TDI Control Word Format

2-28. CONTROL WORD FIELD DEFINITIONS.

2-29. There are five control word fields that are used to perform specific functions. These are I/O Reset (bit 0), Reset Interrupt (bit 1), Channel Number (bits 2 through 6), Output Information (bit 14), and Acknowledge Interrupt (bit 15).

2-30. I/O RESET. A control word with this bit set (logic 1) initializes all logic, including the recirculating memory, on the TDI PCA.

2-31. RESET INTERRUPT. A control word with this bit set (logic 1) causes direct clearing of the Interrupt Request FF. The TDI status word bit 2 should be low following this input.

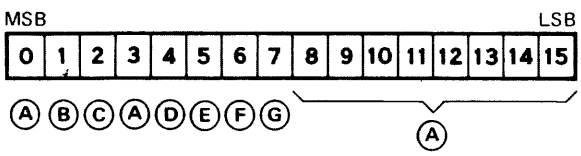
2-32. CHANNEL NUMBER. There are 21 programmable channels of the TDI. Channels 0 through 15 are full-duplex channels that can be connected to external devices or data sets via the connector panel. Channels 16 through 20, called auxiliary or diagnose channels, are receive-only channels that cannot be connected to external devices. Bits 2 through 6 address these channels. To specifically address one of the five receive-only channels, bit 2 must be set (logic 1). To address a send or receive channel, bit 2 must be clear (logic 0). Data over send or receive channels can also be routed to all the receive-only channels without specifically addressing the channels; however, this data is intelligible only to the receive-only channel that is configured with the same parameters as the send or receive path. This is further described in paragraph 2-54. Note that bits 3 through 6 specify only a given channel number and do not specify send or receive path. Bit 1 of the parameter and output data words is used for this. Refer to the applicable paragraphs for details.

2-33. OUTPUT INFORMATION. This bit, when set (logic 1), enables TDI logic to load parameters into either a send or receive channel memory location. This bit also enables send data to be loaded into the recirculating memory and subsequently to be put on-line to the receiving peripheral.

2-34. ACKNOWLEDGE INTERRUPT. A control word with this bit set (logic 1) must follow every device service program. This bit is used to clear and re-enable the TDI functions that generate interrupts to the CPU/IOP upon completion of a character transmission or reception. This releases the CPU while the TDI controls data I/O. For example, on a send channel the CPU can issue a WIO command and a 16-bit output data word, a CIO command and a control word with bit 14 set (paragraph 2-33), and then ignore this channel until the TDI generates an interrupt to flag transmission complete. A control word with this bit set (ACK INT) must now be sent to the TDI to clear this interrupt so the next send or receive channel requiring service can interrupt.

2-35. STATUS WORD FORMAT.

2-36. The status word is a 16-bit word fetched from the TDI during the execution of either a microprogrammed (part of an RIO or WIO) or program code TIO instruction. Figure 2-3 shows the TDI status word format.



(A) SIO OK. Always logic 0 to indicate that SIO operations are not valid for TDI PCA.

(B) READ/WRITE OK. Becomes logic 0 for a maximum of 69.4 microseconds following TDI receipt of a CIO with bit 14 set to indicate to CPU that TDI is not available for read or write operations.

(C) INTERRUPT REQUEST. Logic 1 indicates that an interrupt is pending.

(D) FLAG BIT. Becomes logic 1 upon completion of a character send or receive operation. Must be cleared to logic 0 by a CIO command with bit 15 (ACK INT) set.

(E) R/S BIT. Logic 0 indicates that interrupt is from a receive channel upon completion of a character reception. Logic 1 indicates that interrupt is from a send channel upon completion of character transmission.

(F) CHARACTER LOST. Logic 1 indicates that the TDI received two characters on a receive channel without the computer responding to the interrupt generated upon receipt of the first character, which is now lost.

(G) BREAK. Logic 1 when a break character (all spaces) has been sent or received by the TDI.

2249-20

Figure 2-3. TDI Status Word Format

2-37. STATUS WORD FIELD DEFINITIONS.

2-38. There are six status word fields that inform the CPU/IOP of various TDI conditions. These are Read/Write OK (bit 1), Interrupt Request (bit 2), Flag (bit 4), S/R (bit 5), Character Lost (bit 6), and Break (bit 7).

2-39. READ/WRITE OK. This bit informs the CPU/IOP whether or not the TDI is available for read or write operations. The R/W OK bit is low for a maximum of 69.4 microseconds following TDI receipt of an output data word to indicate to the CPU/IOP that the TDI is still seeking the addressed memory location (send channel number) of the last word received. If a non-existent channel number was sent to the TDI, the logic will continue indefinitely to seek a memory location in which to load the output data word.

2-40. INTERRUPT REQUEST. This bit is high to indicate that the Interrupt Request FF is set and an interrupt is pending.

2-41. FLAG. This bit goes low to indicate the completion of a character transmission or reception on a particular channel. The Flag must be cleared following CPU servicing of the interrupting channel by a CIO control word with bit 15 (ACK INT) set. If this bit is not cleared, other TDI channels cannot interrupt.

2-42. R/S. This bit indicates whether it is the send or receive path of a given channel causing an interrupt. A low bit indicates that the interrupt is from a receive channel, a high bit indicates a send channel.

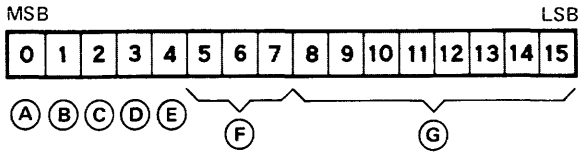
2-43. CHARACTER LOST. This status bit goes low to indicate that the TDI has received two or more characters on a receive channel without generating an interrupt. Each channel has a one-character buffer that allows the CPU/IOP at least one complete character time for interrupt processing and acknowledging the TDI interrupt (control word bit 15). When two characters are received without being serviced, the first character is lost and the Character Lost bit is set.

2-44. BREAK. This bit goes high when a break character (all spaces) is transmitted or received. A continuous spacing input is accepted and handled by the TDI as a character but the break flag is set if no marking bit appears in the entire character. Note that this is an unbuffered status bit. At high character rates (see table 1-1), this bit should be verified since the start of the next character being received may be causing invalid break status for the character previously received.

2-45. PARAMETER WORD FORMAT.

2-46. The parameter word is a 16-bit word sent to the TDI during execution of a WIO instruction. A CIO and a control word must then specify the send or receive channel memory location into which the parameter word is to be loaded. This parameter word is used by the TDI to establish the bit rate and character length of the specified channel. The TDI cannot send or receive data on a channel that is not configured with parameters. Note also that the channel parameter configuration must comply with the speed and

size requirements of the peripheral device or data set on that channel. Figure 2-4 shows the TDI parameter word format.



(A) DATA/PARAMETER. This bit must be logic 1 to indicate that this word contains parameters; logic 0 indicates data.

(B) R/S BIT. Logic 1 specifies that the word contains information for a send channel, and logic 0 specifies receive channel. When configuring an auxiliary channel, this bit should be a logic 0, and a CIO must be received with bit 2 set to indicate that the channel number specified in the control word is one of auxiliary channels 0 through 4.

(C) ENABLE INTERRUPT. This bit must be logic 1 to enable the TDI mini-interrupt system, which allows a given channel to generate an interrupt upon completion of character transmission or reception. If this bit is logic 0 for a given channel, the interrupts for that channel are masked.

(D) PARITY. On a send channel, logic 1 causes even parity to be generated, and logic 0 does not. This parity is even parity computed on bits 8 thru 15 of each send character, and replaces bit 8 of each send character. Either odd or even parity can be generated for bits 9 thru 15.

ECHO. On a receive channel, if this bit is a logic 1, each bit received by the TDI from a device is echoed back to that device. This is useful for such devices as teletypes and visual display terminals. However, when the CPU/IOP is transmitting to such a device over a send channel, the echo bit on the corresponding receive channel must be turned off to avoid interference between data echoed and characters transmitted.

(E) DIAGNOSE. Logic 1 causes data sent or received over a given channel to be routed to the five auxiliary channels. If all five auxiliary channels are configured to the same parameters as the given channel, all will receive intelligible data. If only one auxiliary channel is so configured, only that channel will receive intelligible data, on the others the data will be garbled.

(F) CHARACTER SIZE. These three bits specify the bits per character for a given channel. Refer to paragraph 2-55 for details.

(G) BAUD RATE. These eight bits specify, in octal, the serial bit stream bit rate for a given channel. Bit rate is programmable from 75 to 2400 bps. Refer to paragraph 2-56 for details.

2249-21

Figure 2-4. TDI Parameter Word Format

2-47. PARAMETER WORD FIELD DEFINITIONS.

2-48. The parameter word has eight fields that are used to perform specific functions. These are Parameter/Data (bit 0), S/R (Bit 1), Enable Interrupt (bit 2), Parity/Echo (bit 3), Diagnose (bit 4), Character Size (bits 5 through 7), and Baud Rate (bits 8 through 15). Table 2-3 lists some typical parameter words.

2-49. DATA/PARAMETER. This bit must be a logic 1 to inform the TDI logic that the word is a parameter word; otherwise it will be interpreted as an output data word.

2-50. R/S. This bit is a logic 1 to indicate that the parameters are for a send channel and a logic 0 for a receive channel. This bit qualifies the channel number specified in the CIO control word which states a channel number without indicating whether the channel is a send or receive path. (The send and receive paths of the same channel have different TDI memory locations.)

2-51. ENABLE INTERRUPT. This bit is the controlling input for the TDI mini-interrupt system. Just as the CPU can set subsystem group interrupt masks, so it can also individually enable or mask off each of the 16 send and 16 receive TDI channels by using this bit. A logic 1 input enables a given channel to interrupt on completion of a character transmission or reception. A logic 0 disables the interrupt function of that channel.

2-52. PARITY/ECHO. This bit specifies parity for a send channel and enables or disables echo for a receive channel. On a send channel, if the parity bit is set (logic 1), then the eighth data bit transmitted will be the exclusive-or of the bits 8-15 output from the computer. This represents even parity for a 7-bit ASCII character, or if bit 8 of the output data is a 1, the parity sense is inverted and is odd parity for an ASCII character. On a receive channel, this bit controls the hardware echo of characters back to the terminal.

2-53. On a receive channel, each bit shifted into the interface is echoed back to the device if the echo bit is set. Some devices, such as the teletype, have an independent keyboard and printer. The printer operates upon data from the computer only. In order to print a typed character, the computer must echo back the character. The computer program could echo back each character after it was received, but this would introduce a one character delay between typing of the character and printing on the teletype. Using bit-by-bit echo, this delay is eliminated. When the computer is transmitting characters, the echo bit on the corresponding receive channel must be turned off to avoid interference between the data echoed and characters transmitted.

2-54. DIAGNOSE. When this bit is set (logic 1) for a given channel, data transfers over that channel are routed both to their ultimate destination and to each of the five auxiliary channels. For this data to be intelligible, however, one or all (as desired) of the auxiliary channels must be

configured with parameters identical to those of the channel having the diagnose parameter set. Most of the TDI logic can be checked by setting the diagnose bit of a send channel, wrapping the send data around, and comparing the data received on the auxiliary channel(s) with that sent.

2-55. CHARACTER SIZE. Bits 5 through 7 specify the character size. These three bits are the least significant bits of the number of data bits and stop bits, in a character. For instance, a teletype transmits a start bit, 7 data bits, a parity bit, and two stop bits so that the character size is $1010_{(2)}$. The character size parameter is the three least significant bits or $010_{(2)}$. Table 2-2 lists some typical character lengths and corresponding character size parameters.

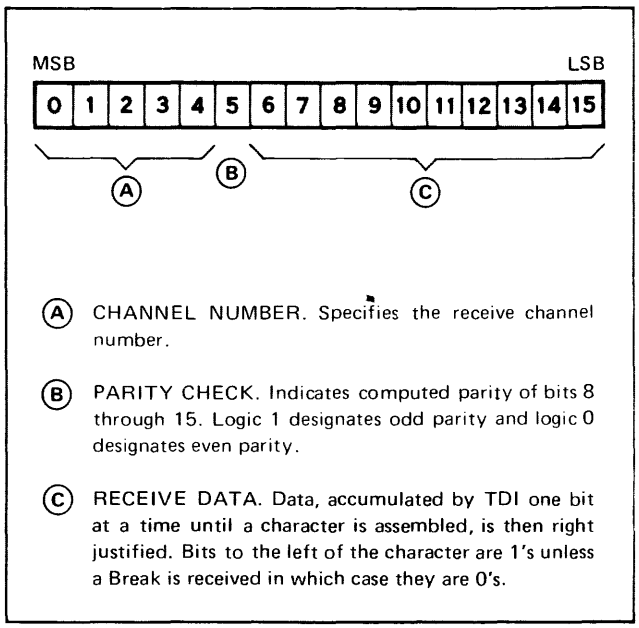
2-56. BAUD RATE. Bits 8 through 15 contain the bits used to determine the bit rate of the serial bit stream. The baud rate parameter is in octal and is one less than the number which divides 14,400 to give the bit rate of the device. The equation to compute the baud rate is as follows:

$$\text{Baud Rate Parameter} = \left[\frac{14{,}400_{10}}{\text{Device Bit Rate}} \right] - 1$$

For baud rates that do not divide evenly, pick the divisor most nearly correct.

2-57. INPUT DATA WORD FORMAT.

2-58. The input data word is a 16-bit word fetched from the TDI following execution of an RIO direct instruction. The TDI accumulated this 16-bit word, bit by bit, from a peripheral device or data set and generated an interrupt when the complete character was assembled and ready to be read into the computer. Figure 2-5 shows the input data word format.



2249-22

Figure 2-5. TDI Input Data Word Format

2-59. INPUT DATA WORD FIELD DEFINITIONS.

2-60. There are three fields to the input data word: Channel Number (bits 0 through 4), Parity Check (bit 5), and Receive Data (bits 6 through 15).

2-61. CHANNEL NUMBER. This field specifies the number of the receive channel. Bit 0, when high, indicates that channel number 0 through 4 specified in the remaining bits is that of an auxiliary channel rather than one of receive channels 0 through 4.

2-62. PARITY CHECK. Bit 5 is the computer parity of bits 8 through 15. The parity check bit is low for odd parity and high for even. A low for even parity or a high for odd parity is a transmission error.

Table 2-2. Typical Character Lengths and Parameters

DEVICE	CHARACTER LENGTH	CHARACTER SIZE PARAMETER (BINARY)
HP 2749B Teleprinter	11 bits = 1 start, 7 data, 1 parity, 2 stops.	010
IBM 2741 SDI II	9 bits = 1 start, 6 data, 1 parity, 1 stop.	000
HP 2761A Automatic Optical Mark Reader	10 bits = 1 start, 7 data, 1 parity, 1 stop.	001
Baudot Code Devices	7-1/2 bits = 1 start, 5 data, 1-1/2 stop (send 2; receive 1).	111 send 110 receive

Table 2-3. Typical Parameter Words

DEVICE	PARAMETER WORD*
OUTPUT	
TTY ASR 33 (11 bit format, ASCII) (110 baud).	161202
IBM 2741 Selectric (9 bit format, PTTC/BCD) (134.5 baud).	160157
30 cps terminal (10 bit format).	160457
60 cps terminal.	160427
120 cps terminal.	160413
240 cps terminal.	160405
150 baud Baudot code terminal.	163537
TTY with parity (110 baud).	171202
TTY with diagnose (data is routed to auxiliary channels).	165202
INPUT	
TTY ASR 33 (with echo) (110 baud).	131202
IBM 2741 Selectric (134.5 baud).	120157
30 cps terminal (with echo).	130457
60 cps terminal (without echo).	120427
120 cps terminal.	120413
240 cps terminal.	120405
TTY with diagnose (input data routed to auxiliary channels) (110 baud).	135202
150 baud terminal (Baudot code).	133537
STOP BIT FORMATS (to be "or" gated with the character before output)	
TTY (ASCII) (without parity or with odd parity.	43600
TTY with even parity.	43400
Selectric.	43600
Baudot code.	43740
Time delay character on channel configured without parity.	47777
Time delay character on channel configured with parity.	47577

*Note that baud rate parameter is in octal.

2-63. RECEIVE DATA. Bits 6 through 15 contain one character received from an external device or data set. The character bits are right justified.

2-64. OUTPUT DATA WORD FORMAT.

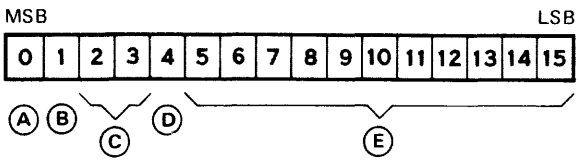
2-65. The output data word is a 16-bit word sent to the TDI during the execution of a WIO direct instruction. The TDI then requires a subsequent CIO instruction to load the word into TDI memory for transmission to a device. Figure 2-6 shows the output data word format.

2-66. OUTPUT DATA WORD FIELD DEFINITIONS.

2-67. The output data word has four fields: Parameter/Data (bit 0), S/R (bit 1), Sync (bit 4), and Send Data (bits 5 through 15).

2-68. DATA/PARAMETER. This bit must be a logic 0 to indicate a data word; otherwise, the TDI will interpret the word as a parameter word.

2-69. R/S. This bit must be logic 1 to specify that the channel number in the subsequent CIO control word designates the send path of that channel. A logic 0 is illegal and



(A) DATA/PARAMETER. This bit must be a logic 0 to indicate that word contains data, a logic 1 indicates that the word contains parameters.

(B) R/S BIT. This bit must be logic 1 to specify output to a send channel, logic 0 is illegal in an output data word.

(C) Not used.

(D) SYNC BIT. This bit is usually a logic 0 character start bit, but can be a logic 1 to allow transmission of an all-mark character.

(E) SEND DATA. One character, right justified, packed with trailing "1's".

2249-23

Figure 2-6. TDI Output Data Word Format

may cause destruction or modification of data on the receive path of the designated channel.

2-70. SYNC. This bit is usually the start bit of the character contained in bits 5 through 15, and is used to synchronize transmissions. The Sync bit can also be a logic 1 to allow transmission of an all-mark character period.

2-71. SEND DATA. Bits 5 through 15 contain one character, right justified, and packed with trailing "1's." Bit 15 is the data LSB. This data is loaded in parallel into a given TDI memory location and put on line to the device on that channel one bit at a time.

2-72. TCI I/O INSTRUCTIONS.

2-73. The controller TCI accepts control words from the CPU/IOP under CIO instructions, generates and monitors control signals to peripheral devices or data sets, and returns status words to the CPU/IOP under TIO instruction. The following paragraphs present the control and status word formats and word bit definitions.

2-74. CONTROL WORD FORMAT.

2-75. The TCI control word is a 16-bit word sent from the CPU/IOP to the TCI during the execution of direct command CIO. The format of the control word is illustrated in figure 2-7.

2-76. CONTROL WORD FIELD DEFINITIONS.

2-77. The 13 fields of the control word each perform a specific function. These are Clear (bit 0), Reset Request (bit 1), Scan (bit 2), Update (bit 3), Channel Number (bits 4 through 7), Control Line 2 Enable EC2 (bit 8), Control Line 1 Enable EC1 (bit 9), Control Line 2 C2 (bit 10), Control Line 1 C1 (bit 11), Status 2 Enable ES2 (bit 12), Status 1 Enable ES1 (bit 13), Status Line 2 S2 (bit 14), and Status Line 1 S1 (bit 15).

2-78. CLEAR. A CIO command and control word with bit 0 set (logic 1) initializes all TCI logic.

2-79. RESET REQUEST. A CIO command and control word with this bit at logic 1 provides direct clearing of the Interrupt Request FF.

2-80. SCAN. When Scan bit 2 is a logic 1, the TCI channel counter scan operation is activated. During scan, the S1 and S2 status lines from the peripheral devices or data sets are sequentially selected and compared with the S1 and S2 status values of each channel stored in the RAM. If the S1 and S2 status lines are enabled to interrupt (ES1 and/or ES2 at logic 1), a difference in the stored and actual status line values cause scan operation to halt and an interrupt to be sent to the CPU/IOP. Scan bit 2 and Update bit 3 must be set in the control word used to resume scanning following an interrupt.

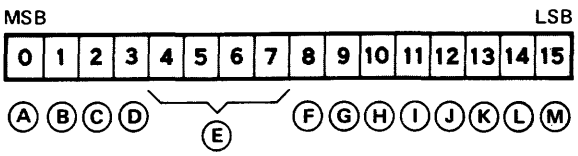
2-81. UPDATE. A control word with this bit set (logic 1) enables the write function of the TCI 64-bit RAM. During a write function, the stored status values S1 and S2 and the interrupt enable inputs for S1 and S2 for a designated channel can be loaded or changed in RAM.

2-82. CHANNEL NUMBER. Bits 4 through 7 are used to address a control word to a specific channel 0 through 15. For updating channel status data, these bits specify a RAM location. For generating or changing control line outputs to a device or data set, the bits specify the channel output lines to be affected.

2-83. CONTROL LINE 2 ENABLE, EC2. Bit 8 must be a logic 1 to enable control line C2 output to a specified channel.

2-84. CONTROL LINE 1 ENABLE, EC1. Bit 9 must be a logic 1 to enable control line C1 output to a specified channel.

2-85. CONTROL LINE 2, C2. The value of C2 (bit 10) determines the state of the Request-to-Send EIA interface signal (CA) on TCI no. 1 and Frequency Select (CH) on TCI no. 2. A logic 1 C2 input produces a high (ON) output on the addressed EIA interface line to the external device providing EC2 is also a logic 1. A logic 0 C2 input produces a low (OFF) output providing EC2 is a logic 1. The C2 output can be enabled, disabled, or changed without affecting the RAM stored status values for a given channel and without affecting scan operation.



(A) MASTER CLEAR. Logic 1 causes TCI logic to be initialized.

(B) RESET INTERRUPT. Logic 1 clears Interrupt Request FF.

(C) SCAN. Logic 1 enables TCI logic to sequentially scan the S1 and S2 status lines from data sets and compare stored status values with actual status values. When the stored and actual status values for a particular channel do not compare, and the status lines for that channel are enabled to interrupt upon change in status values, an interrupt is generated and scan is disabled. Scan must be reactivated via a control word to the TCI following an interrupt.

(D) UPDATE. Logic 1 enables the updating of stored status (S1 and S2) and stored status interrupt enable (ES1 and ES2) bits contained in the TCI 64-bit RAM for any given channel.

(E) CHANNEL NUMBER. Specifies number of the channel to be affected by the contents of the particular control word.

(F) EC2. This bit is the output enable for control line C2. When EC2 is a logic 1, C2 is output to the TCI on the specified channel.

(G) EC1. This bit is the output enable for control line C1. When EC1 is a logic 1, C1 is output to the TCI on the specified channel.

(H) C2. This signal controls EIA interface signal Request to Send, CA, on TCI no. 1 and Frequency Select, CH, on TCI no. 2, the logic 1 and logic 0 states of C2 are used to select one of two ranges of data signalling rates. C2 output must be enabled by EC2.

(I) C1. This signal controls EIA interface signal Data Terminal Ready, CD, on TC1 no. 1 and Secondary Send Data, SA, on TCI no. 2. On TCI no. 1, a logic 1 C1 input produces an EIA bus positive (ON) output. On both TCI nos. 1 and 2, C1 output must be enabled by EC1.

(J) ES2. This bit is the interrupt enable bit for status line S2, and is stored in the TCI 64-bit RAM under channel number specified. When ES2 is a logic 1, a difference between stored status S2 and actual status S2 from the data set can generate an interrupt.

(K) ES1. This bit is the interrupt enable bit for status line S1, and is stored in the TCI 64-bit RAM under channel number specified. When ES1 is a logic 1, a difference between stored status S1 and actual status S1 from the data set can generate an interrupt.

(L) S2. This bit is the status bit to be stored in the TCI 64-bit RAM for the S2 interface line for a given channel. When the ES2 bit is logic 1, the value of this S2 status bit and the value of the actual S2 status line from the data set are compared and an interrupt is generated if the stored and actual S2 values differ. This S2 bit is the stored status bit for EIA interface signal Carrier Detect, CF, on TCI no. 1 and for Clear to Send, CB, on TCI no. 2.

(M) S1. This bit is the status bit to be stored in the TCI 64-bit RAM for the S1 interface line for a given channel. When the ES1 bit is a logic 1, the value of this S1 status bit and the value of the actual S1 status line from the data set are compared and an interrupt is generated if the stored and actual S1 values differ. This S1 bit is the stored status bit for EIA interface signal Data Set Ready, CC, on TCI no. 1 and Secondary Received Data, SB, on TCI no. 2.

2249-17

Figure 2-7. TCI Control Word Format

2-86. CONTROL LINE 1, C1. The value of C1, bit 11, determines the state of the Data Terminal Ready (CD) EIA interface signal on TCI no. 1 and Secondary Send Data (SA) on TCI no. 2. A logic 1 C1 input produces a high (ON) output on the addressed EIA interface line to the external device providing EC1 is also logic 1. A logic 0 C1 input produces a low (OFF) output providing EC1 is a logic 1. The C1 output can be enabled, disabled, or changed without affecting either scan operation or the RAM stored status values for a given channel.

2-87. ENABLE STATUS LINE 2, ES2. This bit (bit 12) is the stored interrupt enable for status line S2 that is stored in RAM for each channel. When bit 12 is a logic 1, a difference in value between the actual S2 input from a particular channel and the stored value of status S2 for that channel generates an interrupt. When bit 12 is a logic 0, a change in status values cannot create an interrupt.

2-88. ENABLE STATUS LINE 1, ES1. This bit (bit 13) is the stored interrupt enable for status line S1 that is

stored in RAM for each channel. When bit 13 is a logic 1, a difference in value between the actual S1 input from a particular channel and the stored value of status S1 for that channel generates an interrupt. When bit 13 is a logic 0, a change in status values cannot create an interrupt.

2-89. STATUS LINE 2, S2. Bit 14 is the value stored in RAM for status line S2. During scan operation, providing ES2 (bit 12) is a logic 1, the stored status S2 and the actual S2 device input of each channel are sequentially compared and an interrupt generated when a difference is detected. On TCI no. 1, S2 is the stored status of EIA interface signal Carrier Detect (CF); on TCI no. 2, Clear to Send (CB). A logic 1 S2 is input from CPU/IOP when it is desired that an interrupt be generated when the actual S2 input from the device goes low (EIA OFF condition), and conversely.

2-90. STATUS LINE 1, S1. Bit 15 is the value stored in RAM for status line S1. During scan operation, providing ES1 (bit 13) is a logic 1, the stored status S1 and the actual status S1 device input of each channel are compared sequentially and an interrupt generated when a difference is detected. On TCI no. 1, S1 is the stored status of EIA interface signal Data Set Ready (CC); on TCI no. 2, Secondary Received Data (SB). A logic 1 S1 is input from CPU/IOP and stored when it is desired that an interrupt be generated when the actual S1 input from the device goes low (EIA OFF condition), and conversely.

2-91. STATUS WORD FORMAT.

2-92. The TCI status word is a 16-bit word fetched from the TCI following the execution of direct command TIO or RIO. The format of this status word is illustrated in figure 2-8.

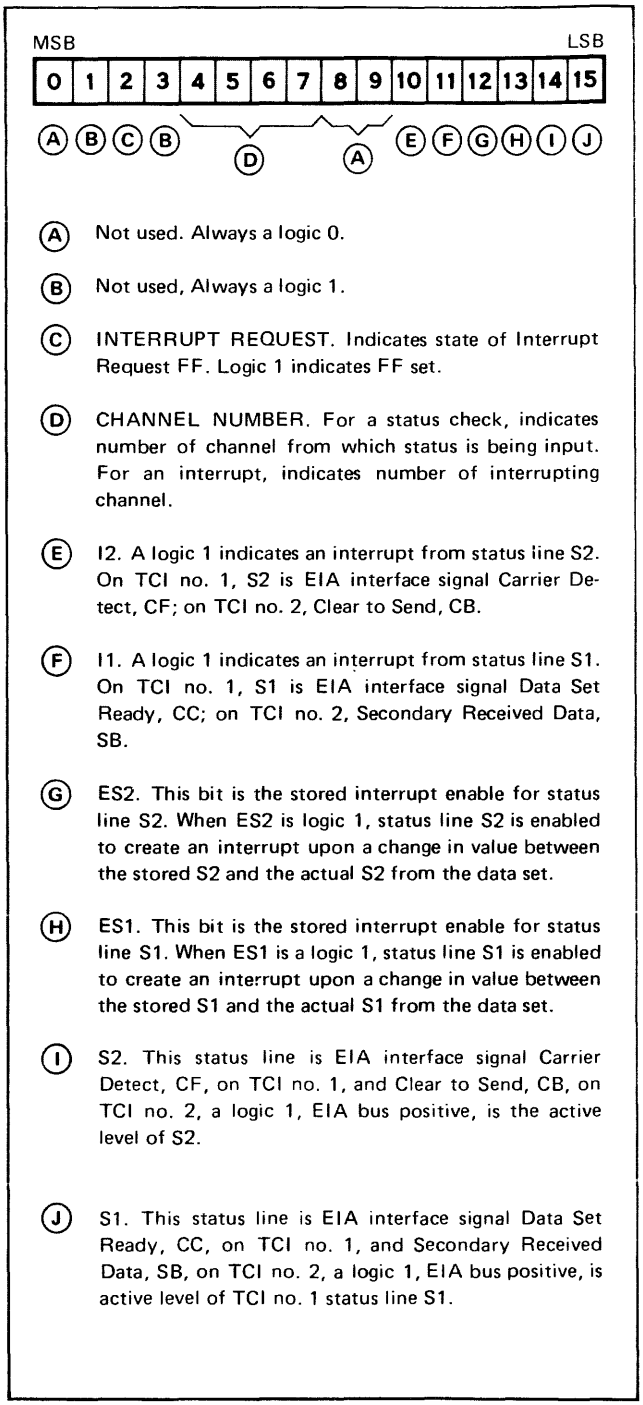


Figure 2-8. TCI Status Word Format

2-93. STATUS WORD FIELD DEFINITIONS.

2-94. The status word has eight fields, each of which specify unique status information. These fields are Interrupt Request (bit 2), Channel Number (bits 4 through 7), status line 2 interrupt 12 (bit 10), status line 1 interrupt (bit 11), status line 2 stored interrupt enable ES2 (bit 12), status line 1 stored interrupt enable ES1 (bit 13), actual status S2 (bit 14), and actual status S1 (bit 15).

2-95. INTERRUPT REQUEST. This bit indicates whether or not an interrupt is pending. A logic 1 indicates that the Interrupt Request FF is set and an interrupt is pending.

2-96. CHANNEL NUMBER. Bits 4 through 7 of a status word designate either the number of the interrupting channel 0 through 15 or the number of the channel from which status is being fetched.

2-97. I2. Bit 10 indicates the interrupt status of status line S2. If a change between the stored and actual S2 values is detected this bit is a logic 1.

2-98. I1. Bit 11 indicates the interrupt status of status line S1. If a change between the stored and actual S1 values is detected this bit is a logic 1.

2-99. ES2. Bit 12 of the status word reflects the state of the stored interrupt enable bit for status line S2. A logic 1 indicates that status line S2 is enabled to interrupt upon a detected change between the stored and actual values.

2-100. ES1. Bit 13 of the status word reflects the state of the stored interrupt enable bit for status line S1. A logic 1 indicates that status line S1 is enabled to interrupt upon a detected change between the stored and actual values.

2-101. S2. Bit 14 of the status word is the actual S2 status being received from a device on a given channel. A logic 0 in this bit position indicates Carrier Detect OFF on TCI no. 1 and Clear to Send OFF on TCI no. 2.

2-102. S1. Bit 15 of the status word is the actual S1 status being received from a device on a given channel. A logic 0 in this bit position indicates Data Set Ready OFF on TCI no. 1, and a mark (low) condition for Secondary Receive Data on TCI no. 2.

2-103. DEVICE PARAMETERS.

2-104. Both PCA's of the HP 30032B Asynchronous Terminal Controller have PCA-to-external device signal lines that comply with EIA specification RS-232C for serial device communications. Such standardization allows a wide range of devices to be operated either hardwired or through data sets.

2-105. DATA INTERFACE SIGNALS.

2-106. The TDI handles all data interface between external devices and the CPU/IOP. The two (EIA) data lines between the TDI and the external devices bear EIA designations BA and BB.

2-107. BA is the serial data line to the device or data set. This line represents a logic 1 when at a low level (negative) and a logic 0 when high (positive). When used with a data set, a logic 1 causes the data set to generate a mark frequency and a logic 0 causes the data set to generate a space frequency. When used with an active data set, it will carry either the delayed (echoed) BB line intelligence or the transmitted data from the device.

2-108. BB is the serial data line from the device or data set. It provides serial data transmitted by the device using the same logic levels as the BA line. If the data set is inactive, the BB line is a logic 1.

2-109. CONTROL INTERFACE SIGNALS.

2-110. The TCI handles the control signals for the peripheral devices or data sets. Either one or two PCA's may be used. Note however that whether one or two PCA's are used, the only difference is in signal names and functions: the TCI logic functions the same, regardless, to monitor two lines (S1 and S2) and provide outputs on two lines (C1 and C2) under CPU/IOP control. On TCI no. 1 the two monitored lines are Data Set Ready (S1) and Carrier Detect (S2) bearing EIA designations CC and CF, respectively. On TCI no. 1 the control lines are Data Terminal Ready (C1) and Request-to-Send (C2) bearing EIA designations CD and CA, respectively. On TCI no. 2 the two monitored lines are Secondary Receive Data (S1) and Clear-to-Send (S2) bearing EIA designations SB and CB, respectively. On TCI no. 2 the two control lines are Secondary Send Data (C1) and Frequency Select (C2) bearing EIA designations SA and CH, respectively.

2-111. CC. On TCI no. 1, status line S1 is CC, Data Set Ready or Data Terminal Ready. When this line is ON (positive), the data set is in the data mode. When the data set is out of the data mode either because the data set automatically disconnects or the call is terminated, the CC line goes OFF (negative).

2-112. CF. On TCI no. 1, status line S2 is CF, Carrier Detect. From a hardwired terminal this is Request-to-Send. This is a status line from the data set that indicates, when ON (positive), that a carrier signal from another data set is being received. On the model 103 data set it should remain on for the duration of the call. On a model 202 data set, in the receive mode, CF indicates the presence of the other data set carrier but in the send mode it indicates the presence of its own carrier. During line turn around CF goes off then on again. A loss of CF during a reception indicates a line fault.

2-113. CD. On TCI no. 1, control line C1 is CD, Data Terminal Ready and appears as Data Set Ready to a terminal. This is a control line to the data set. When ON (positive), the data set will answer a call, send data, and receive data. When it is dropped to OFF (negative), the data set disconnects and will not answer a call.

2-114. CA. On TCI no. 1, control line C2 is CA, Request-to-Send. This control line appears as Carrier Detect to a terminal. When used with a type 202 data set, ON (positive) on this line puts the data set in the send mode and OFF (negative) puts the data set in the receive mode. This line must be toggled when a line turnaround is desired. On some type 103 data sets, this line is used to turn the transmitter on and off.

2-115. CB. On TCI no. 2, status line S2 is CB, Clear-to-Send. This is actually the request to send (CA) signal brought back through a delay circuit. The delay is of sufficient length to allow for line turnaround time.

2-116. CH. On TCI no. 2, control line C2 is CH, Frequency Select. This line can be used to select between two data signalling rate ranges. Although this line is not generally used in the United States, it is used in some European installations.

2-117. SA. On TCI no. 2, control line C1 is SA, Secondary Send Data. This line provides a reverse channel low speed line to transmit information opposite the direction of the data path. On a type 202 data set, it uses off-on keying of a 387 hertz tone to provide a maximum 5 baud transfer rate.

2-118. SB. On TCI no. 2, status line S2 is SB, Secondary Receive Data. This is the reverse channel low speed receive line for information transmitted on the distant data set SA line.

2-119. For additional information on the use of these lines, refer to the documentation supplied with the data set or terminal being used and to EIA standard RS-232-C.

2-120. INTERRUPTS.

2-121. Both asynchronous terminal controller PCA's have main and mini-interrupt capabilities. The main interrupt logic is fairly standard, having the usual set, reset, and group mask features. The TDI, however, provides for CPU interrupt for each channel upon completion of character transmission or reception. This includes a provision to mask off any one or all of the channels. There is no interrupt priority structure for these channels, however. If all channels were enabled to interrupt and all were to become ready to interrupt at the same time (which cannot happen), each channel would be serviced in random sequence. While the CPU is recognizing and acknowledging the interrupt of one channel the other channels simply await their turn. All other channels hold their mini-interrupt flags raised until they each gain access to the main interrupt logic. Note that the CPU must acknowledge each device interrupt within one character time or no other channel can interrupt and characters may be lost.

2-122. The mini-interrupt logic of the TCI is similar. The TCI monitors two status lines from each of 16 channels. Each status line of each channel has a corresponding interrupt enable bit. If either or both of these interrupt enable bits are set for a given channel, a change in the corresponding status line can cause an interrupt. Note that the TCI channels interrupt in channel number sequence. Note also that if an interrupt enable bit for a status line is not set, value changes on that line are ignored.

SECTION III THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. Information presented in this section includes a description of the HP 30032B Asynchronous Terminal Controller within the HP 3000 Computer System, a general description of the subsystem components, and a functional description of subsystem components in terms of operational sequences. The general description is supported by overall and detailed block diagrams in this section. The more detailed functional description is supported by simplified logic diagrams. Applicable detailed logic diagrams are sets 507 and 509 in the *Detailed Logic Diagrams Manual* for the HP 3000 Computer System. Also refer, as necessary, to the timing diagrams and flowcharts in section IV.

3-3. SYSTEM INTERFACE.

3-4. The HP 30032B Asynchronous Terminal Controller provides the command, control, and data interface between the computer system and up to 16 bit-serial, low-speed terminals such as hardwired visual displays, printers, card readers, etc., or type 103 or 202 data sets. The asynchronous terminal controller and any permissible mix of peripheral devices comprise a subsystem of the HP 3000 Computer System. This subsystem functions under direct I/O control of the CPU/IOP to transfer information to or from the top of stack in the CPU via the IOP bus and processor. This information can be device status, control signals, or data. The description of the direct command, device address, and service out signals and the 16-bit control, parameter, status, and data words are detailed in section II of this manual. Of prime importance here are the means provided by the asynchronous terminal controller to recognize, process, and acknowledge these transfers. The functional components that are responsible for these operations are the physically and functionally independent terminal data interface (TDI) printed-circuit assembly (PCA) and the terminal control interface (TCI) PCA.

3-5. TDI PCA BLOCK-LEVEL DESCRIPTION.

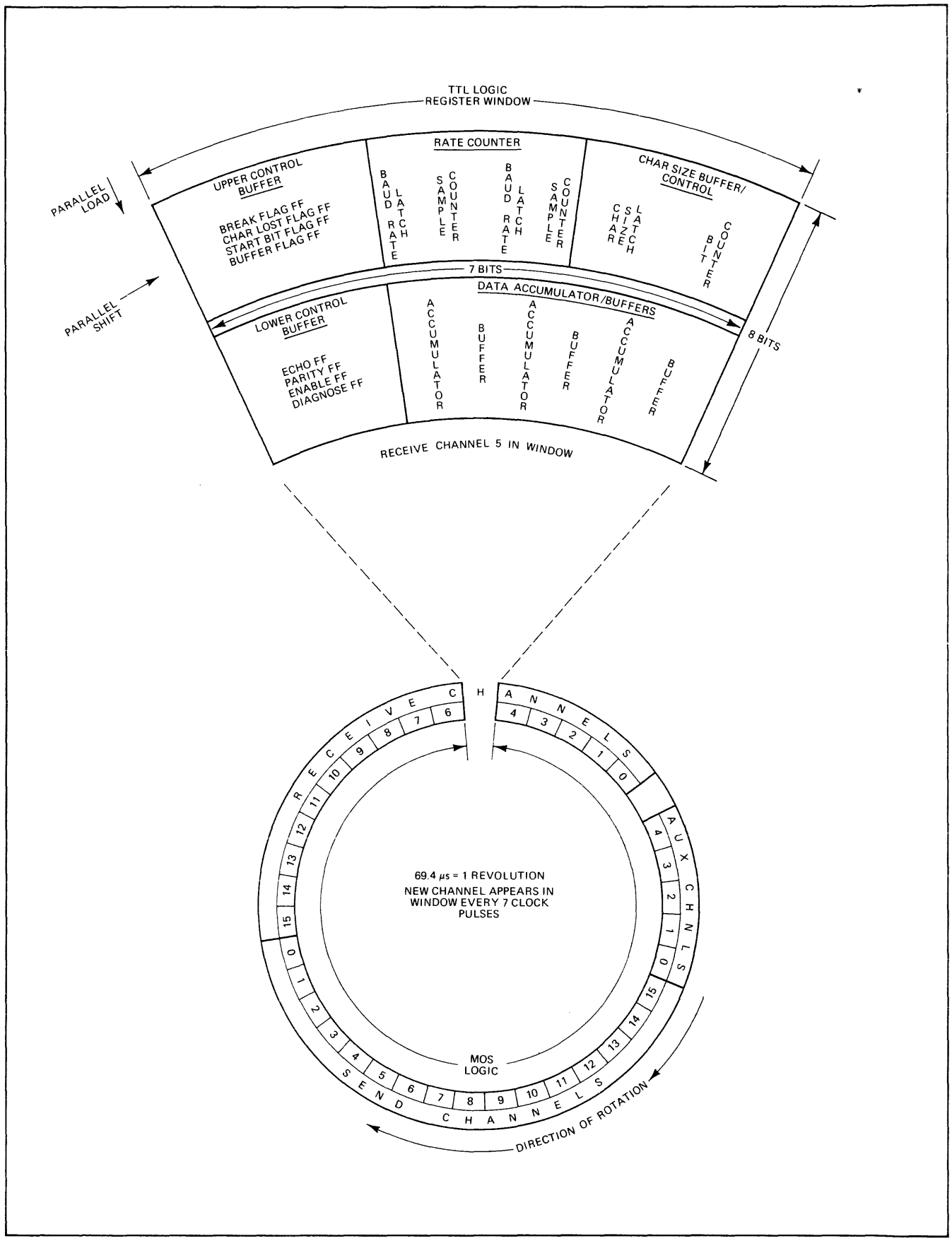
3-6. The TDI, as its name implies, provides all asynchronous, bidirectional data transfer functions between the CPU and up to 16 peripheral devices. The TDI accepts control, parameter, and output data words from the CPU/IOP under CIO and WIO direct commands and returns status and input data words fetched by TIO and RIO direct commands.

3-7. There are a total of 37 TDI channels: 16 full-duplex device I/O channels and 5 receive-only channels called auxiliary or diagnose channels. The five auxiliary channels do not have access to external interfaces. Each half (send or receive) of each of the 16 full-duplex channels and each of the five auxiliary channels must be configured by the CPU/IOP with parameters. These parameters are the baud rate and character length required by the particular device on that path. Note that the send and receive paths of the same channel need not be configured with identical parameters although they may be if required.

3-8. When the CPU/IOP sends an output data word for a particular channel to the TDI, that word is accepted and placed in a storage location assigned to the send path of that channel. Note that this storage location must also contain previously assigned baud rate and character length parameters for this send channel. The TDI then puts the word on line to the device one bit at a time until the entire character is sent. Then the TDI generates an interrupt to inform the CPU/IOP that transmission of the word for that channel is complete.

3-9. The process of receiving data from a device destined for the CPU is very nearly the reverse of the send operation just described. The TDI accumulates one bit at a time on a particular channel, temporarily stores these bits as they are received in a storage location assigned to the receive path of that channel, and generates an interrupt to the CPU when a complete character is assembled and ready for transfer to memory. As for the send channel, the receive channel storage location must contain the bit rate and character size parameters for the device on that path. These parameters are received from the CPU/IOP by means of a WIO direct command and a 16-bit parameter word followed by a CIO direct command and a 16-bit control word. The TDI cannot process send or receive data unless the various storage locations are pre-configured with the required parameter information.

3-10. An important aspect of TDI operation is the fact that it contains one storage location for each of the 16 send paths or half-duplex channels, 16 receive paths or half-duplex channels, and five auxiliary channels for a total of 37 memory locations. Figure 3-1 is a pictorial representation of this memory showing the memory locations and the sequence in which they are ordered. Note that 36 locations are MOS integrated circuits that cannot be accessed by any of the other logic on the TDI. Note also that one location consists of TTL integrated circuits that can be accessed by the other TDI logic. This location is called the window. Each memory location has a seven-bit by eight-bit capacity. A clock is applied to this memory so that all bits parallel-shift for seven clock times, wait for one, parallel-shift seven clock times, wait for one, and so on. For this reason the memory is termed recirculating. A given channel storage location is shifted into the TTL logic window during the seven clocks, held there for one clock period, and then



2249-13

Figure 3-1. TDI Recirculating Memory

shifted out by the next seven clocks while the next sequential location is shifted in by those same clocks. It is during the time that a location is held in the TTL logic register window that that location can be loaded or unloaded or some function be performed by the TTL logic on the contents of that location. Note that the upper and lower control buffers, the rate counter, and the character size control buffer are the fields of the location that must contain parameters. Data transfers are made directly to and from the data accumulator/buffers.

3-11. As can now be seen, the TDI is capable of a parallel load, parallel unload, serial bit send, or serial bit receive for each of the 37 channels once per memory revolution. However, because of the tremendous disparity in rate between the 4.32-MHz memory clock and the 75-to-2400 bits per second rate range of the external devices, the duration of one bit sent or received is equal in time to six or more memory revolutions. For the TDI to send or receive one serial bit at the highest available device speed, 2400 bits per second, requires six memory revolutions. One bit is either received for six revolutions or one bit is taken from storage, placed in latches, and sent to the device for six revolutions. Note that the TDI is doing something on each of however many channels are active (data I/O in process) once per revolution.

3-12. DESCRIPTION OF COMPONENTS.

3-13. Figure 3-2 is a functional block diagram that shows each group of logic and its signal interface with other groups. Some blocks shown are self-explanatory and not detailed in the following paragraphs. Note that a barred signal ($\overline{XYZ}$) indicates that the low level of that signal is its true state.

3-14. LINE RECEIVERS AND DRIVERS. All TDI inputs and outputs are routed through either line receivers or line drivers to condition the signals and, except for the data in line drivers, convert the I/O bus logic levels to those used on the interface. A low input to the inverting line receivers, I/O bus logic 1, is inverted and adjusted so that it is a high internal logic 1 of approximately 5 volts. Conversely a high input, I/O bus logic 0, becomes a low internal logic 0 of approximately 0 volts. A similar level change and inversion process is performed by the inverting line drivers. The non-inverting line drivers that pass bits from the status, address, and data-in buffers accept a low internal logic 0 from the respective gating and load this level onto the I/O bus as a low I/O bus logic 1.

3-15. ADDRESS GENERATOR AND COMPARATOR. The address generator consists of seven jumper positions, the loading of which determines the device address and interrupt priority of the TDI. These seven jumpered levels provide one set of inputs to the address comparator. The second set of inputs is the Device Address (DEVAD 1:7) signals from the IOP bus. When the two sets compare and the Service Out ($\overline{SO}$) signal indicates that a valid direct command on the bus requires attention, the command decoder is enabled.

3-16. COMMAND DECODER AND DECODER ENABLE GATING. The Service Out signal and the output of the address comparator are "anded" to provide an Enable ($\overline{ENABLE}$) signal to the command decoder. The command decoder then provides one of six possible outputs depending on the coded I/O Command ($\overline{IOCMD\ 0:2}$) inputs. Note that I/O commands SIO and SMSK are not decoded by the command decoder.

3-17. SERVICE-IN GENERATOR. The service-in generator provides a Service In ($\overline{SI}$) signal upon receipt of an Enable signal from the decoder enable circuits and one of the following signals: I/O Command 2 ($\overline{IOCMD2}$), Direct Control Strobe ($\overline{D\ CONT\ STRB}$), Direct Write Strobe ($\overline{D\ WRITE\ STRB}$), Direct Status Strobe ($\overline{D\ STAT\ STRB}$), or Direct Read Strobe ($\overline{D\ READ\ STRB}$). Note that the Service In signal is returned to the IOP bus for any of the direct commands addressed to the TDI except SMSK.

3-18. INTERRUPT LOGIC AND SET MASK FF COMMAND GATE. The Service Out signal and a Set Mask (SMSK) I/O command are "anded" at the set mask flip-flop command gate. The output of this gate disables the interrupt logic for two input conditions. One disable condition is satisfied when the Service Out signal, the Set Mask command, and the TDI group interrupt mask word are on the IOP bus. The second disable condition is satisfied when the TDI group interrupt mask jumpers are loaded to respond to all Set Mask commands. When enabled, the interrupt logic provides three outputs to the CPU/IOP: Interrupt Request ($\overline{INT\ REQ}$), Interrupt Acknowledge ($\overline{INT\ ACK}$), and the address of the interrupting device (DEVINTAD). Interrupt Request is generated by the Flag input from the up/down transfer control logic or by direct I/O command Set Interrupt ($\overline{SET\ INT}$). Interrupt Request is cleared by direct I/O command Reset Interrupt ($\overline{RST\ INT}$), the Reset input from the reset logic, or upon receipt of a CIO direct command and a control word with bit 1 (DO1) set. Interrupt Acknowledge and the Device Interrupt Address occur as a result of TDI response to the Interrupt Poll ($\overline{IPOLL}$).

3-19. When any one of the TDI send or receive channels completes transmission or reception of a character, the Flag input from the up/down transfer control logic causes an Interrupt Request to be sent to the CPU/IOP. The CPU/IOP responds by sending Interrupt Poll In (IPOLL IN) to the first controller or interface in the interrupt chain. (Any interface not requesting service accepts Interrupt Poll In and loops this signal out to the next interface address as Interrupt Poll Out (IPOLL OUT). The next interface accepts this signal as Interrupt Poll In and, if not requesting service, propagates Interrupt Poll Out. This propagation continues until the interrupting device responds to Interrupt Poll In by gating its Device Interrupt Address onto the IOP bus.) When the TDI receives Interrupt Poll In, the interrupt logic generates three signals: Enable, Interrupt Acknowledge, and Interrupt Active ($\overline{INT\ ACT}$). The Enable strobe gates the Device Interrupt Address onto the IOP bus. The Interrupt Acknowledge output indicates subsystem response to the interrupt poll. The Interrupt Active output

is sent to the reset logic where it generates the Reset signal. This signal is looped back to the interrupt logic to clear Interrupt Request at the time of Interrupt Acknowledge.

3-20. RESET LOGIC. This logic provides all the clear and reset signals used by the TDI. An I/O Reset ($\overline{\text{IORST}}$) command or a CIO direct command and a control word with bit 0 (DO0) set causes the reset logic to clear the TDI interrupt logic as well as generate the Master Reset ($\overline{\text{MR}}$) and Initialize signals that clear the remaining TDI logic. The receipt and decoding of direct command Reset Interrupt ($\overline{\text{RST INT}}$) provides direct clearing of the interrupt logic Interrupt Active FF (refer to paragraph 3-84). The Interrupt Active input to the reset logic at the time of Interrupt Acknowledge clears Interrupt Request.

3-21. UP/DOWN TRANSFER CONTROL LOGIC. The up/down transfer control logic generates the signals required to control transfers between the CPU/IOP and the TDI for both send and receive channels. This logic also generates the Flag and Read/Write OK signals. Flag, routed to the interrupt logic upon completion of transmission or reception of one character, generates Interrupt Request. Read/Write OK is a status signal used to tell the CPU/IOP whether or not the TDI is available for data transfers.

3-22. On a send channel, a CIO command and a control word with bit 14 set causes the up/down transfer control logic to generate Down Address Buffer Load (DN ADR BUFFER LOAD). This signal strobes the channel number contained in the control word into the down address buffer and causes Read/Write OK to inform the CPU/IOP via subsequent status checks that the TDI is busy. The Match signal input from the channel number compare logic occurs within the next 69.4 microseconds if the control word channel address is valid. The input of the Match signal generates the Transfer Down (XFR DN) pulse. This pulse strobes the CPU output word into the recirculating memory location assigned to the addressed send channel. After the Transfer Down pulse, the Read/Write OK status bit informs the CPU that the TDI is no longer busy. When all bits of the output word have been put on-line to the external device, the Buffer Flag input from the upper control buffer causes the Flag signal to be generated, causing a subsequent CPU/IOP interrupt. A CIO command and a control word with bit 15 set is required to clear the Flag signal.

3-23. On a receive channel, the Buffer Flag signal is routed to the up/down transfer control logic when a complete character has been received and is ready to be sent to memory. In this case, Buffer Flag causes the generation of Transfer Up ($\overline{\text{XFR UP}}$), Up Latch Load, and Flag signals. The Up Latch Load pulse strobes the word from memory into the data-in buffer, loads the receive channel number into the up address buffer, and loads the status bits of that channel into the status-in buffer. Subsequent RIO and TIO direct commands to the TDI are decoded and used to fetch the input data and status words. As for a send channel, a CIO command and a control word with bit 15 set must be received to clear the Flag signal.

3-24. CLOCK AND TIMING GENERATOR. The clock and timing generator provides two slightly asymmetrical 4.32-MHz clocks, 180 degrees out of phase, a Decision Pulse strobe (DP,$\overline{\text{DP}}$) which occurs every eighth clock period for the duration of that period (230 ns), and Transfer Clock. Part of this logic functions in conjunction with the channel number compare logic to provide two least significant bits of the channel number and Carry, discussed in paragraph 3-25. (Figure 4-8 shows the clocks, strobes, and various control signal relationships.)

3-25. CHANNEL NUMBER COMPARE LOGIC. The channel number compare logic continuously steps through receive channel numbers 0 through 15, send channel numbers 0 through 15, and auxiliary channels 0 through 4. Whenever this logic is on a given count or channel number, the memory location assigned to that channel is in the recirculating memory TTL logic register window. (Figure 4-9 shows the count sequence and address generation of this logic.)

3-26. On a transfer down, this logic generates a Match signal when the storage location of an addressed channel is in the window of the recirculating memory. The desired storage location is addressed by the control word channel number held in the down address buffer. The bit 1 position (DO1) of the data out holding register indicates whether the channel number is that of a send or a receive channel. (Only parameters can be sent to a receive channel.) On a receive channel transfer up, the channel number bits from this logic and from the clock and timing generator are loaded into the up address buffer by an Up Latch Load signal. The Send/Receive bit is also sent to the status-in buffer. There it becomes the status word bit that informs the CPU/IOP whether the channel number in the up address buffer is that of a send or receive channel.

3-27. The Carry input to the channel number compare logic is used to enable this logic to step to the next channel address after every eighth clock period. This allows for the parallel shifting of the seven fields of the memory location into the register window and the holding of that location in the window for one period (refer to paragraph 3-10). The Last Channel Detect output of this compare logic is used as a channel number count preset-to-1 after the thirty-seventh address (the end of each memory revolution) is stepped through. The Last Channel Detect signal is also used as a strobe by the main/diagnose channel select logic (refer to paragraph 3-28) and the output registers and buffers (refer to paragraph 3-29). The Main Channel strobe disables the input multiplexer while the auxiliary channels are passing through the memory window (addresses 33 through 37). At the same time, this signal is also sent to the main/diagnose channel select logic where it is used to disable the clock to the output registers and buffers while the diagnose channels are passing through the memory window.

3-28. MAIN/DIAGNOSE CHANNEL SELECT LOGIC. The main/diagnose channel select logic has several functions. For receive channel addresses 0 through 15, this logic routes Device Data from the input multiplexer and

makes it available as the serial Line input. A second function is to disable the clock to the output registers and buffers during auxiliary channel addresses 32 through 36. A third function is performed when data transferred over a send or receive channel is also to be routed to the auxiliary channels. This third function is enabled when the Diagnose bit in the parameter word for a channel is set. (Refer to paragraphs 2-54 and 3-42.) Under these circumstances, each bit sent (New Bit) or received (Device Data) is sampled and temporarily stored until the auxiliary channels pass through the memory window. At such time, this logic sends the sampled bit as the serial Line input to the data accumulator/buffers of all fice auxiliary channels. Whether or not this data is intelligible depends upon whether or not one or all auxiliary channels were configured with parameters that correspond to the data being sampled. The Last Channel Detect input clears the main/diagnose channel select logic at the end of each memory revolution.

3-29. OLD/NEW BIT SELECT LOGIC AND OUTPUT REGISTERS. The old/new bit select logic can best be understood if it is considered as part of a closed loop between the serial input and serial output of the output registers. The contents of this loop are circulated by a clock that occurs during the Decision Pulse (DP) which occurs once per channel number for a total of 37 times per memory revolution. Now, the main/diagnose channel select logic, as stated in the previous paragraph, disables this clock during the five auxiliary channel numbers. So there are only 32 output register clocks per memory revolution. This means that the register contents are looped twice per revolution synchronously with each channel storage location that passes through the memory window. On the send channels, a new bit from a given memory location can replace an old bit already in the output register if the required output bit time for the old bit has elapsed, as indicated by the occurrence of a Shift pulse. Shift allows the new bit to replace the old bit. At the end of each memory revolution, Last Channel Detect strobes the output register contents into the output buffers. If the old bit of a given channel has not been replaced, there is no change in the line output to the device on that channel. If there was a replacement, the new bit is put on line.

3-30. On a receive channel configured for echo such as for teletype, the bit received from the device is looped, loaded in the output register, and returned to the device. Note that the bit received is both clocked in and looped back to the device simultaneously.

3-31. RECIRCULATING MEMORY. Compare the pictorial illustration of this memory in figure 3-1 with the layout and signal flow shown in figure 3-2. The lower control buffer, the rate counter, and the character size buffer/control are the storage locations that the CPU/IOP must load (configure) with device parameters. Parameter loading is performed by the issuance of a WIO direct command and a 16-bit parameter word, and then a CIO direct command and a control word with bit 14 set. (A TIO command precedes the WIO to check the status of Read/Write OK.) Details of these parameters and the word formats employed are covered in section II of this manual.

3-32. Upper Control Buffer and Flag Control Logic. The contents of the upper control buffer are governed by the flag control logic. This flag control logic monitors the transfers and functions performed by the TTL register window logic each time a channel storage location is in the window during a Decision Pulse. Only one event can occur at framing and Decision Pulse time because only one clock, either serial or parallel, is applied to the TTL window logic. This means that one character is loaded or unloaded in parallel, one flag bit is raised or lowered, or counters are stepped once. (The contents of each memory location are in some pattern when they are shifted into the window. There, one operation is performed and a changed pattern is shifted out and circulated through the MOS logic.) There are four flag signals having specific functions: Buffer Flag, Start Bit Flag, Character Lost Flag, and Break Flag.

3-33. The Buffer Flag is set on either a send or receive channel when a complete character has either been sent or received, providing that the mini-interrupt logic for that channel is enabled to interrupt. The mini-interrupt is enabled when the Enable parameter bit in the lower control buffer is set, as it should be for any active channel. Buffer Flag is routed to the up/down transfer control logic where it ultimately generates the Flag signal that initiates Interrupt Request.

3-34. The Start Bit Flag is used by the TDI logic to verify receipt of a valid start bit on a receive channel. This flag is set at the beginning of a seeming start bit on a receive channel by Receive Start. If Receive Start does not remain true for one-half bit duration the Start Bit Flag clears the character size buffer/control and then is cleared itself.

3-35. The Character Lost Flag is set to indicate that the Buffer Flag was raised to generate an interrupt to the CPU/IOP but was not acknowledged and thereby cleared. Therefore the first character that should have been fetched by the CPU/IOP is lost.

3-36. The Break Flag is set at the time of start-of-character and remains set until a marking bit occurs in the character being transferred, indicating that the character is not a Break character. Since this flag is set at the start of a character, at high character rates, an invalid break status bit may be generated for the previously received character and should be verified.

3-37. Rate Counter and Character Size Buffer/Control. The rate counter determines the bit interval of data being transferred. This is accomplished by presetting the rate counter, at the beginning of a character start bit to a count based upon the baud rate parameter received from the CPU/IOP. The time then required for the rate counter to reach its maximum count is the duration of one bit at the specified baud rate. Each time the rate counter reaches its maximum count, a Shift pulse is sent to the character size buffer/control logic, shift control logic, flag control logic, and old/new bit select logic. The Shift pulse is also looped back to the rate counter to cause the rate counter to be re-preset at the end of each bit interval. On a send channel, the Shift pulse occurs on the lagging edge of the send bit.

On a receive channel, the bit interval count is offset during reception of the character start bit so that thereafter, for each bit, the Shift pulse occurs mid-bit rather than on the lagging edge. This ensures serial loading of a valid bit by avoiding edge transients.

3-38. At the shift control logic, the Shift pulse is used to disable the Parallel Clock input to the data accumulator/buffers. When this occurs the serial Logic Clock causes serial shifting of a bit into (receive) or out of (send) the data accumulator/buffers.

3-39. At the flag control logic, the only time the Shift pulse input is used is to clear the Start Bit Flag after receiving a character start bit of the proper duration (refer to paragraph 3-34).

3-40. At the old/new bit select logic, the Shift pulse is used on a send channel to replace an old bit with a new bit from the data accumulator/buffers. The Shift pulse is also used on a receive channel using echo to loop the received Line input back to the device via the output registers and buffers.

3-41. Operation of the character size buffer/control is similar to that of the rate counter. The character size buffer bit counter is preset at the beginning of a character start bit to the complement of the character size parameter received from the CPU/IOP. The bit counter steps once for each Shift pulse from the rate counter. The number of Shift pulses required for the bit counter to reach its maximum count is the number of bits per character programmed for transfer over that channel. Note that the Bit Count > 0 output to the rate counter enables the rate counter when the bit counter is preset or at a count greater than 0. The sample counter is disabled when the bit count is equal to zero.

3-42. Lower Control Buffer. The lower control buffer is used to store the Echo, Parity, Enable, and Diagnose parameters. Echo, used for receive channels only, causes received data to be returned to the sending device bit by bit as received. Parity enables the generation of parity on a send channel only. Enable, the mini-interrupt enable bit, is used to enable generation of Buffer Flag. Diagnose causes data being transferred to also be routed to and stored in the memory locations for the auxiliary channels.

3-43. Data Accumulator/Buffers. The data accumulator/buffers are used for data accumulation and temporary storage. For a send channel, a right-justified character is loaded in parallel and then serially shifted out, bit by bit. For a receive channel, data is serially accumulated, held, and then shifted in parallel into the data-in buffer where it is available for transfer to the CPU/IOP. Parallel and serial clocks to this logic are enabled or disabled during Decision Pulse by the shift control logic.

3-44. The Transfer Down input to the shift control logic enables the Parallel Clock to the data accumulator/buffers during Decision Pulse. This causes the contents of the data out holding register to be loaded in parallel into the data accumulator/buffers. Once loaded, only the serial Logic Clock is enabled during Decision Pulse, and only when a Shift pulse occurs, until all bits of the character loaded are put on-line to the external device.

3-45. For transfer up operation, the serial Logic Clock loads the accumulators. Then the contents of the accumulators are strobed into the data-in buffer during Decision Pulse by the Up Latch Load signal.

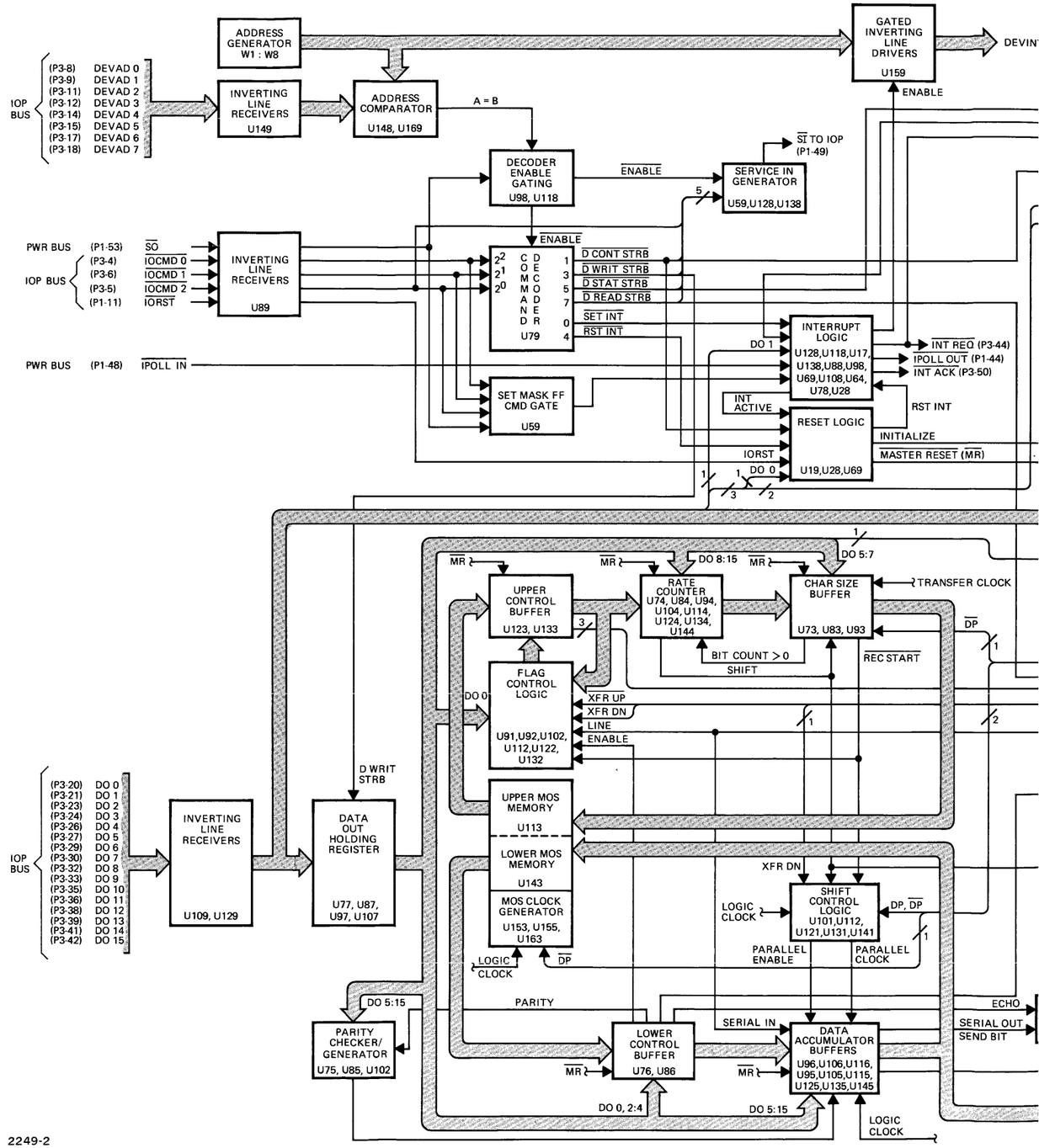
3-46. CHANNEL CONFIGURATION.

3-47. As already stated, the recirculating memory location for every active channel must be configured with the parameters required on that channel. A channel is configured by a transfer down operation. Figure 4-10 shows the timing for this operation and figure 3-3 the simplified signal flow. A WIO command, decoded as Direct Write Strobe, loads a 16-bit parameter word into the data-out holding register. Then a CIO command and a control word with bit 14 set causes a Transfer Down signal to be generated when the addressed memory location is in the memory window (at Match time). The Transfer Down signal, in turn, causes the complement of the data-out holding register contents to be selected at the time of Transfer Clock by the Parameter Mux Load signal and transferred into the baud-rate and character-size latches. These parameters are held in the latches and used for all transfers over that channel.

3-48. SEND OPERATION.

3-49. Figure 3-3 shows the data flow over a send channel, Figure 4-14 provides detailed timing for the transmission of one character, and figure 4-15 provides a flowchart of send events. The timing shown is typical, and the highest baud rate (2400 bits per second) is used. Signals shown can be located on figure 3-2 as well as on the simplified and detailed logic diagrams.

3-50. The baud rate multiplexer and latch and the sample counter are the components of the rate counter previously discussed. The character size multiplexer and latch and the bit counter are the components of the character size buffer/control, also previously discussed. Data is strobed into the data-out holding register via the decoding of the WIO command. A subsequent CIO command and control word with bit 14 (and usually bit 15) set generates Transfer Down. This signal causes parallel data transfer into the data accumulator/buffers. Transfer Down also causes presetting of the sample and bit counters to the contents of their respective latches. The sample counter then proceeds to count up, once per memory revolution, until its maximum count is reached. At that time, the Shift pulse steps the bit counter once, causes the first bit (New Bit) of the character in the accumulator to replace the Old Bit that was in the output register, and re-presets the sample counter. This New Bit now in the output register is loaded into the output latches at the end of that particular memory revolution. This serial shifting and data output continues until the bit counter reaches its maximum count. When the bit


ADDRESS GENERATOR W1 : W8
GATED INVERTING LINE DRIVERS U159
DEVINT
IOP BUS
(P3-8) DEVAD 0
(P3-9) DEVAD 1
(P3-11) DEVAD 2
(P3-12) DEVAD 3
(P3-14) DEVAD 4
(P3-15) DEVAD 5
(P3-17) DEVAD 6
(P3-18) DEVAD 7
INVERTING LINE RECEIVERS U149
ADDRESS COMPARATOR U148, U169
A = B
ENABLE
DECODER ENABLE GATING U98, U118
ENABLE
SERVICE IN GENERATOR U59,U128,U138
SI TO IOP (P1-49)
5
PWR BUS (P1-53) SO
IOP BUS (P3-4) IOCMD 0
(P3-6) IOCMD 1
(P3-5) IOCMD 2
(P1-11) IORST
INVERTING LINE RECEIVERS U89
ENABLE
COMMAND DECODER U79
D CONT STRB
D WRIT STRB
D STAT STRB
D READ STRB
SET INT
RST INT
PWR BUS (P1-48) IPOLL IN
INTERRUPT LOGIC U128,U118,U17, U138,U88,U98, U69,U108,U64, U78,U28
INT REQ (P3-44)
IPOLL OUT (P1-44)
INT ACK (P3-50)
DO 1
SET MASK FF CMD GATE U59
INT ACTIVE
RESET LOGIC U19,U28,U69
RST INT
INITIALIZE
MASTER RESET (MR)
IORST
DO 0
1
3
2
1
DO 5:7
MR
DO 8:15
MR
MR
UPPER CONTROL BUFFER U123, U133
RATE COUNTER U74, U84, U94, U104, U114, U124, U134, U144
CHAR SIZE BUFFER U73, U83, U93
TRANSFER CLOCK
3
BIT COUNT > 0
SHIFT
REC START
DP
1
FLAG CONTROL LOGIC U91,U92,U102, U112,U122, U132
DO 0
XFR UP
XFR DN
LINE
ENABLE
1
2
D WRIT STRB
IOP BUS (P3-20) DO 0
(P3-21) DO 1
(P3-23) DO 2
(P3-24) DO 3
(P3-26) DO 4
(P3-27) DO 5
(P3-29) DO 6
(P3-30) DO 7
(P3-32) DO 8
(P3-33) DO 9
(P3-35) DO 10
(P3-36) DO 11
(P3-38) DO 12
(P3-39) DO 13
(P3-41) DO 14
(P3-42) DO 15
INVERTING LINE RECEIVERS U109, U129
DATA OUT HOLDING REGISTER U77, U87, U97, U107
UPPER MOS MEMORY U113
LOWER MOS MEMORY U143
MOS CLOCK GENERATOR U153, U155, U163
XFR DN
SHIFT CONTROL LOGIC U101,U112, U121,U131,U141
LOGIC CLOCK
DP, DP
1
PARALLEL ENABLE
PARALLEL CLOCK
LOGIC CLOCK
DP
DO 5:15
PARITY
ECHO
SERIAL OUT
SEND BIT
SERIAL IN
PARITY CHECKER/ GENERATOR U75, U85, U102
LOWER CONTROL BUFFER U76, U86
DATA ACCUMULATOR BUFFERS U96,U106,U116, U95,U105,U115, U125,U135,U145
MR
MR
DO 0, 2:4
DO 5:15
LOGIC CLOCK

2249-2

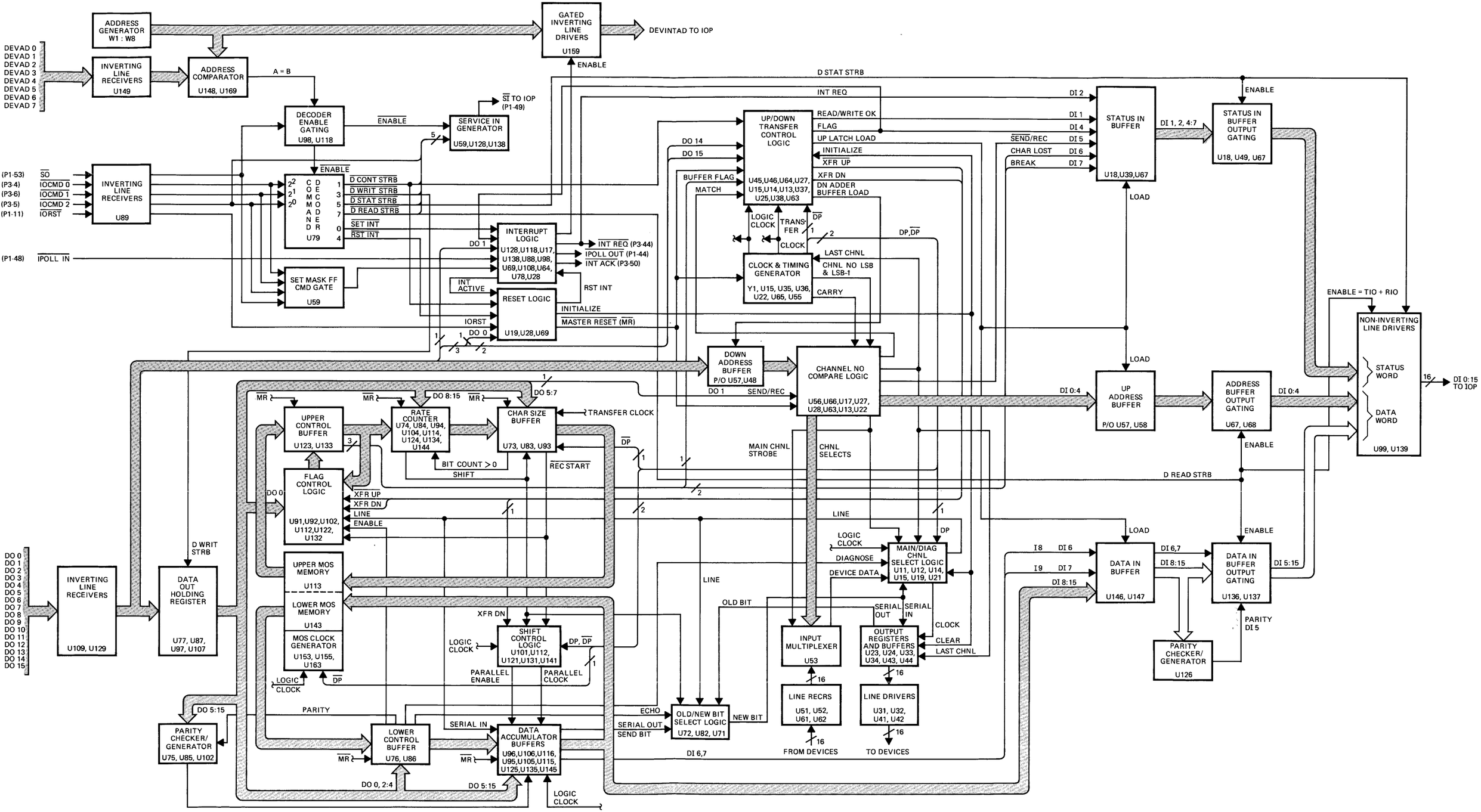
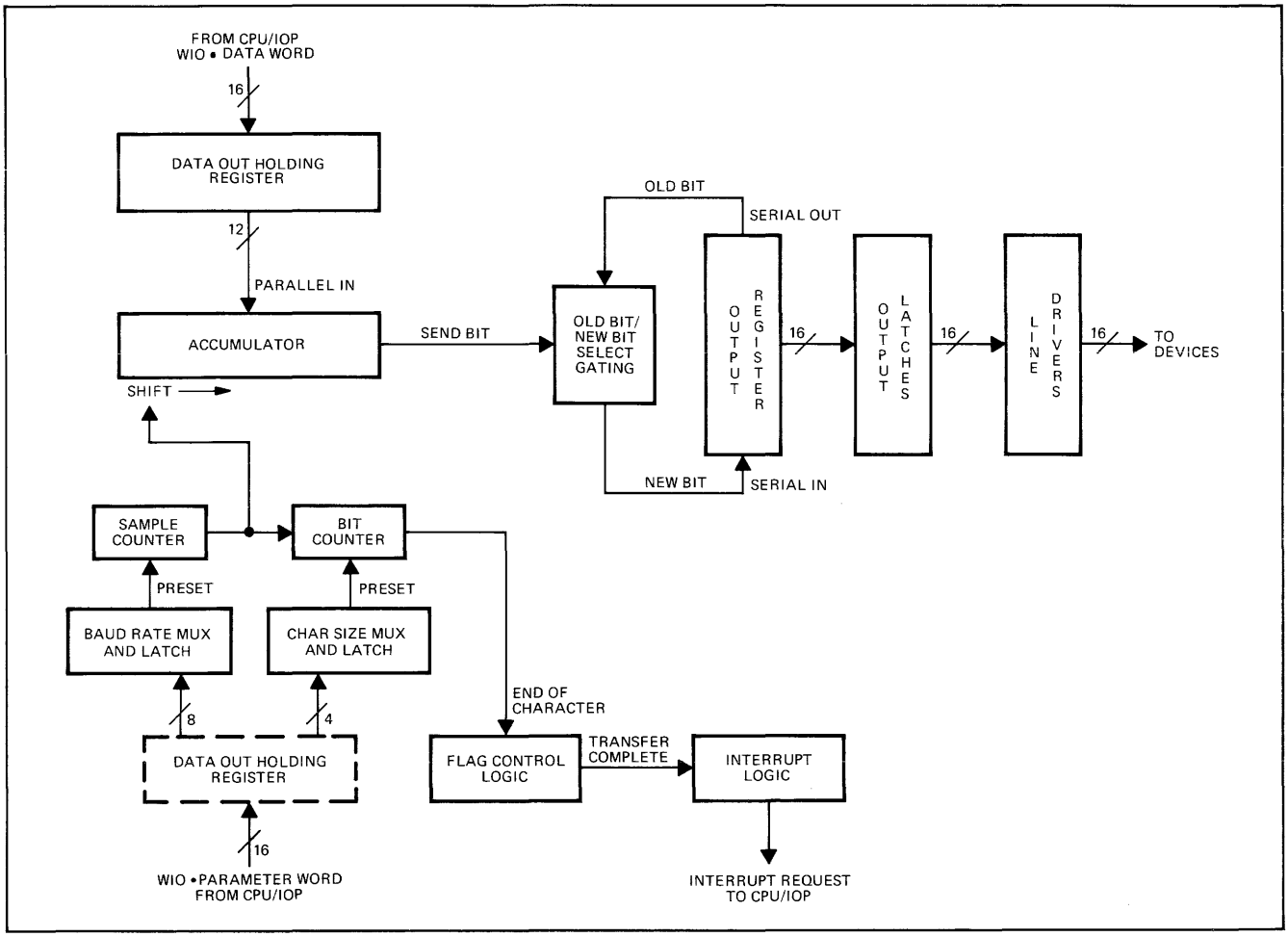


Figure 3-2. TDI Functional Block Diagram



2249-11

Figure 3-3. TDI Send Channel Simplified Signal Flow

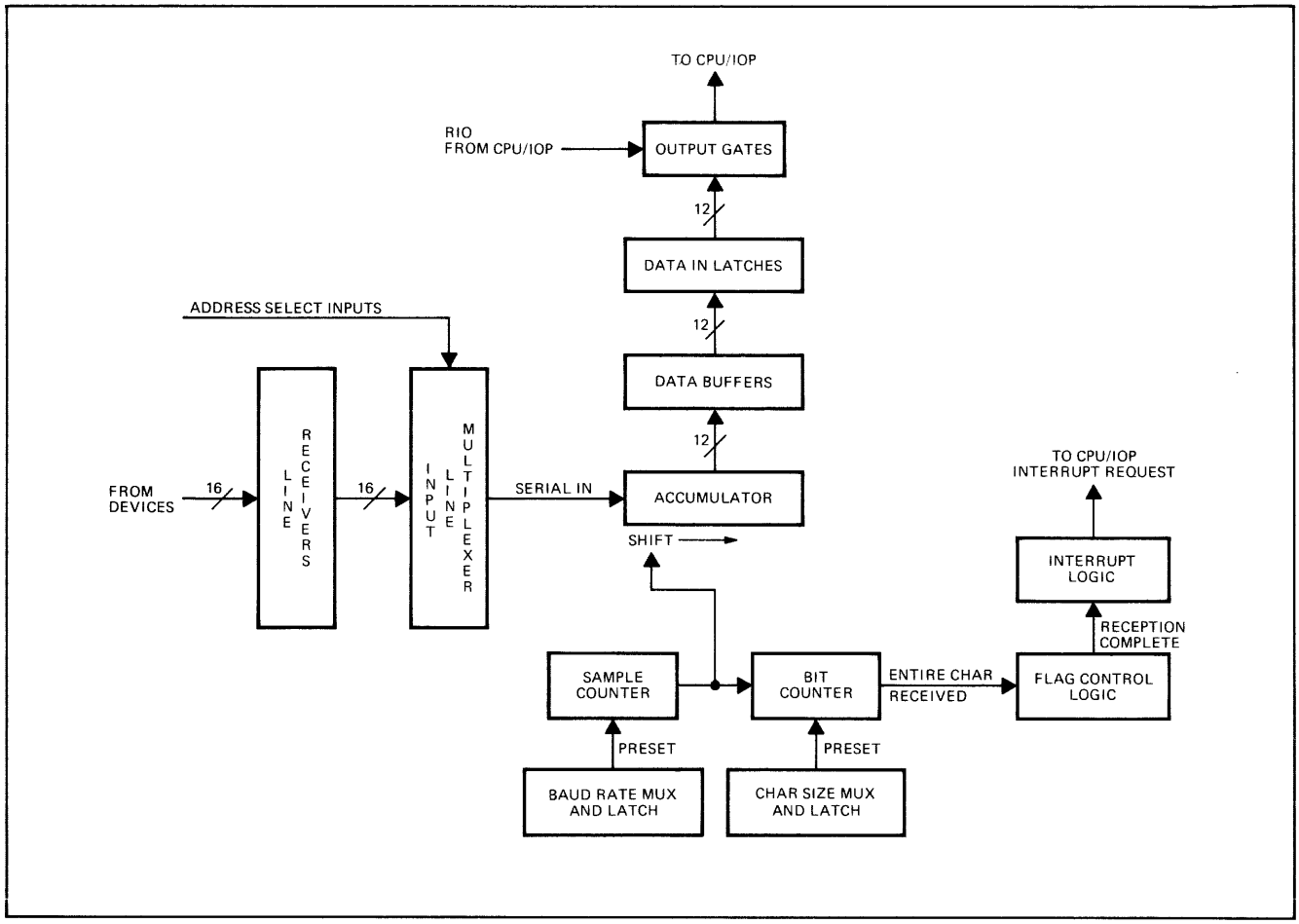
counter reaches its maximum count, Stop is generated to indicate end-of-character. On the following revolution, the Stop signal causes the flag control logic to generate Buffer Flag to indicate that transfer is complete. Providing the interrupt logic is in its initial state, meaning that no other channel is currently either requesting interrupt or being serviced, this channel generates an Interrupt Request.

3-51. RECEIVE OPERATION.

3-52. Figure 3-4 shows the data flow over a receive channel. Figure 4-16 provides detailed timing for the reception of one character with echo at 2400 bits per second, and figure 4-17 is a receive events flowchart. Signals shown can be located on figure 3-2 as well as on the simplified and detailed logic diagrams.

3-53. As previously noted, the baud-rate and character-size latches contain the assigned channel parameters. When a character start bit is detected, the bit counter is preset to the count held in the character-size latch. The sample counter is also preset at this time, but is preset to a count derived from the contents of the baud-rate latches. For all bits after the start bit, the sample counter is preset to the count in the baud-rate latches. No count derivation is performed. In send operation, the Shift pulse occurred to serially shift the accumulator contents at the end of a bit. Now in receive, by off-setting the sample count by one-half of a bit time at the start of a character, the Shift pulse occurs and allows serial shifting of data into the accumulator in what is approximately the middle of a received bit.

3-54. When the sample counter reaches its maximum count, the Shift pulse is generated to serially load the start bit received into the accumulator, step the bit counter once, and re-preset the sample and bit counters to the baud-rate and character-size latch contents. Each received bit is sampled and loaded and the entire character right-justified until the start bit is detected in the most significant accumulator position. Note that the bit counter must reach its maximum count before right-justification occurs. The right-justify operation requires that the maximum bit count disable the sample counter. This permits the Shift pulse to enable the serial Logic Clock to the accumulators. The Logic Clock to the accumulators is held enabled for every memory revolution thereafter until the character received is right-justified. This is indicated by the start bit being detected in its accumulator bit position. Then this Stop output to the flag control logic sets Buffer Flag. Buffer Flag, in turn, is routed to the up/down transfer



2249-12

Figure 3-4. TDI Receive Channel Simplified Signal Flow

control logic to generate an interrupt if no other channel is currently requesting interrupt or being serviced. The Stop signal also causes the character in the accumulator to be loaded in parallel into the data buffer. If the Buffer Flag for this channel can initiate Interrupt Request generation at this time, an Up Latch Load signal is generated to strobe the buffer contents into the data-in latches. When the CPU/IOP acknowledges the interrupt, an RIO command is issued to fetch the character in the latches via the output gates. Note that if the Buffer Flag is not able to initiate an Interrupt Request, it waits for the next revolution to try again.

3-55. TCI PCA BLOCK-LEVEL DESCRIPTION.

3-56. The TCI functions under direct control of the CPU/IOP to generate and monitor control signals required to operate peripheral devices or datasets. The TCI accepts control words from the CPU/IOP containing internal function commands and peripheral or data set status and control signals and generates and monitors these status and control signals. The TCI also maintains control line status for each of the 16 channels available for transfer to the CPU/IOP on request.

3-57. The TCI has two modes of operation: scan and update. During scan operation, the TCI, in sequence by channel number, selects and samples the two status lines for each channel that it monitors. The current values of these status lines are compared with status values for these lines stored by channel number in the TCI 64-bit random access memory (RAM). This 64-bit RAM is in read mode during scan operation. If either or both lines change status, the stored and current status line values do not compare. If the status interrupt enable bits also stored in RAM are set to allow change-in-status interrupts on the channel, the TCI proceeds to generate an interrupt. Note that these interrupt enable bits should be set for each active channel to permit interrupt. If they are not set a change in status goes undetected. When an interrupt is generated, however, the CPU/IOP fetches the status word with either an RIO or TIO command.

3-58. During update operation, the 64-bit RAM is in write mode. In this mode, the two stored status line values and the interrupt enable bit for each for a particular channel can be changed. This is done by CPU/IOP issuance of a control word containing the channel number that requires updating along with the new status and enable bits to be stored.

3-59. In addition to the status storage and monitoring functions, the TCI is responsible for the output of two control signals for each of 16 channels. Each of the control

signals have enable bits. The control line(s) for any channel can be enabled, disabled, or changed without affecting TCI scan or update operations.

3-60. DESCRIPTION OF COMPONENTS.

3-61. Each of the logic groups of the TCI, their functions, and their functions as they affect other groups must be considered. Figure 3-5 is a detailed functional block diagram that shows each group of logic and its signal interface with other groups. Note that a barred signal (XYZ) indicates that the low level of that signal is its true state. Note also that certain blocks are self-explanatory or are covered sufficiently under the discussion of interfacing logic groups and are not detailed separately.

3-62. LINE RECEIVERS AND DRIVERS. All TCI inputs and outputs are routed through either line receivers or line drivers to condition the signals and, except for the data-in line drivers, convert the I/O bus logic levels to those used on the PCA. A low input to the inverting line receivers, I/O bus logic 1, is inverted and adjusted so that it is a high internal logic 1 of approximately 5 volts. Conversely a high input, I/O bus logic 0, becomes a low internal logic 0 of approximately 0 volts. A similar level change and inversion process is performed by the inverting line drivers.

3-63. ADDRESS GENERATOR AND COMPARATOR. The address generator consists of seven jumper positions, the loading of which determines the device address and interrupt priority of the TCI. These seven jumpered levels provide one set of inputs to the address comparator. The second set of inputs is the Device Address (DEVAD 1:7) signals from the IOP bus. When the two sets compare and the Service Out (SO) signal indicates that a valid direct command on the bus requires attention, the command decoder is enabled.

3-64. COMMAND DECODER AND DECODER ENABLE GATING. The Service Out signal and the output of the address comparator are "anded" to provide an Enable (ENABLE) signal to the command decoder. The command decoder then provides one of six possible outputs depending on the coded I/O Command (IOCMD 0:2) inputs.

3-65. SERVICE-IN GENERATOR. The service-in generator provides a Service In (SI) signal upon receipt of an Enable signal from the decoder enable circuits and one of the following signals: I/O Command 2 (IOCMD2), Direct Control Strobe (D CONT STRB), Direct Write Strobe (D WRITE STRB), Direct Status Strobe (D STAT STRB), or Direct Read Strobe (D READ STRB).

3-66. INTERRUPT LOGIC AND SET MASK FF COMMAND GATE. The Service Out signal and a Set Mask (SMSK) I/O command are "anded" at the set mask flip-flop command gate. The output of this gate disables the interrupt logic for two input conditions. One disable condition is satisfied when the Service Out signal, the Set Mask command, and the TCI group interrupt mask word are on the IOP bus. The second disable condition is satisfied when the TCI group interrupt mask jumpers are loaded to respond to all Set Mask commands. When enabled, the interrupt logic provides three outputs to the CPU/IOP: Interrupt Request (INT REQ), Interrupt Acknowledge (INT ACK), and the address of the interrupting device (DEVINTAD). Interrupt Request is generated by the Δ Status input from the status decode logic or by direct I/O command Set Interrupt (SET INT). Interrupt Request is cleared by direct I/O command Reset Interrupt (RST INT), the Reset input from the reset logic, or upon receipt of a CIO direct command and a control word with Interrupt Request Reset bit 1 (DO1) set. Interrupt Acknowledge and the Device Interrupt Address occur as a result of TCI response to the Interrupt Poll (IPOLL).

3-67. When a change in one or both status lines of a TCI-monitored channel is detected, the Δ Status input from the status decode logic causes an Interrupt Request to be sent to the CPU/IOP. The Stop Counter signal is also generated and sent to the control logic to disable the channel counter clock. This stops the channel counter at the address of the channel causing the interrupt because of a status line change. The CPU/IOP responds by sending Interrupt Poll In (IPOLL IN) to the first controller or interface in the interrupt chain. (Any interface not requesting service accepts Interrupt Poll In and loops this signal out to the next interface address as Interrupt Poll Out (IPOLL OUT). The next interface accepts this signal as Interrupt Poll In and, if not requesting service, propagates Interrupt Poll Out. This propagation continues until the interrupting device responds to Interrupt Poll In by gating its Device Interrupt Address onto the IOP bus.) When the TCI receives Interrupt Poll In, the interrupt logic generates two signals: Enable, and Interrupt Acknowledge. The Enable strobe gates the Device Interrupt Address onto the IOP bus. The Interrupt Acknowledge output indicates subsystem response to the interrupt poll. The CPU/IOP subsequently performs a status fetch, updates the stored status bits of the interrupting channel, and clears the Interrupt Request. Then channel counter scan operation resumes.

3-68. RESET LOGIC. This logic provides all the required clear and reset signals. An I/O Reset (IORST) command or a CIO direct command and a control word with bit 0 (DO0) set causes the reset logic to clear the interrupt logic and generate Master Reset (MR) to clear the remaining TCI logic. The receipt and decoding of direct command Reset Interrupt (RST INT) provides a direct clear input to the interrupt logic that disables TCI ability to respond to an interrupt poll. The Interrupt Active input to the reset logic causes Reset to be looped back to the interrupt logic to clear Interrupt Request at the time of Interrupt Acknowledge.

3-69. STATUS DECODE LOGIC. The status decode logic is used during scan operation to compare the monitored (actual) S1 and S2 status line values with the S1 and S2 values stored in RAM. The actual S1 and S2 inputs are status signals received from each device on each channel by the device control input scan logic. As the channels are sequentially scanned, each pair of status inputs are selected and routed to the status decode logic for status-change

comparisons. Whether or not a difference between the stored and actual values can be detected and used to initiate an interrupt depends upon the stored interrupt enable bit inputs to this logic. If interrupt enable bits ES1 and ES2 enable status comparison and decoding, a detected difference between the stored and actual values causes a Δ Status signal to be routed to the interrupt logic. (The Δ Status output is disabled during update operation.) Note that the Δ Status signal also causes the channel scan to stop at the address of the channel causing the interrupt. Two other outputs of the status decode logic are the I1 and I2 bits. These signals are used to indicate the status line(s) that changed. When the CPU/IOP fetches a status word after an interrupt, the channel number, I1 and I2 bits, and actual S1 and S2 values are part of that word.

3-70. CHANNEL COUNTER. The channel counter operates at approximately 1.25 MHz and provides the sequential channel address scanning. The Clock/4 input is derived from the 5-MHz system clock and has a duration of approximately 400 ns. During scan operation, the channel counter steps sequentially through channel addresses 0 through 15 and provides these channel select outputs to the RAM, device control output latches, device control input scan logic, and the data-in line drivers. During update operation, the Direct Control Strobe enables the counter load input, presetting the counter to the channel address contained in the control word to select the RAM address for that channel. Note that if the control word specifies update and resume scan rather than update only, the Clock/4 signal is re-enabled by the control logic following the updating of the RAM storage location.

3-71. CONTROL LOGIC. The control logic performs gating and delay functions to ensure proper sequence of events following receipt of a CIO command and control word. The control logic is also responsible for disabling the channel counter clock at the time of Δ Status from the status decode logic via the Stop Counter input from the interrupt logic.

3-72. During scan operation, the Read output to the RAM maintains read mode. During update operation, the control logic asserts the Write ($\overline{\text{WRITE}}$) signal to permit RAM-content updating. The control logic Scan output enables the scan decode logic Δ Status output to the interrupt logic during scan operation, and disables it during update operation.

3-73. SCAN, CONTROL SIGNAL OUTPUT, AND STATUS INPUT.

3-74. The TCI performs scanning, control signal output, and status maintenance functions. Figure 3-6A shows the signal flow for these operations. Refer to Section II for the EIA interface signal designations for C1, C2, S1, and S2 since they differ between TCI No. 1 and No. 2.

3-75. The decoding of the CIO command strobes the control word into the control data holding register. (See figure 3-6A.) At the same time, the channel counter is preset to the count of the channel address specified in the control word. Control signals C1 and C2, if enabled by control enable signals EC1 and EC2, are loaded into the device control output latch selected by the channel counter outputs. Aside from presetting the channel counter and stopping scan momentarily, scan operation remains in effect and the RAM status storage register remains in read mode. The channel counter resumes counting after the output latches are loaded.

3-76. During scan operation, the actual S1 and S2 device status inputs and the RAM-stored S1 and S2 values for each channel are compared. When the stored and actual values do not compare a change-in-status signal, Δ Status, is sent to the interrupt logic. Note that the status interrupt enable bit also in RAM for each stored status value for each channel must be set to enable interrupt. Otherwise, the status decode logic cannot compare the status values and any status change goes undetected. However, when a change in status is detected, an Interrupt Request is generated and the channel counter is stopped at the interrupting channel address. The CPU/IOP then gates the line drivers via an RIO or TIO command to fetch the status word. Subsequent CPU/IOP commands to the TCI update the channel status values in RAM and clear the Interrupt Request

3-77. UPDATING.

3-78. During update operation, the decoding of the CIO command strobes the control word into the control data holding register (figure 3-6B). At the same time the channel counter is preset to the count of the channel address specified in the control word. The control word Update bit causes the RAM status storage register to be placed in write mode. The control word S1 and S2 values and the corresponding status interrupt enable bits ES1 and ES2 are loaded into the RAM address selected by the channel counter outputs. Since updating usually follows a status-change interrupt, the Write signal also clears the interrupt logic. If the control word Scan bit is set, scan operation resumes after updating the RAM. Otherwise, another CIO command and control word must be sent to the TCI to resume scan operation.

3-79. TDI PCA FUNCTIONAL-LEVEL DESCRIPTION.

3-80. The TDI logic performs twelve functions. Each of these are discussed in the following paragraphs and are supported by simplified logic diagrams. Note that the logic shown on the simplified diagrams is keyed by set and grid reference numbers to a location on detailed logic diagram set 507. For example, 507C7 translates as set number 507, and represents logic found in grid coordinate C7.

3-81. COMMAND DECODING FUNCTIONS.

3-82. The command decoding function is performed by six units. These are the address generator, address comparator, decoder enable gating, service-in generator, command decoder, and set mask command decoder. These six units are shown in simplified form in figure 3-7.

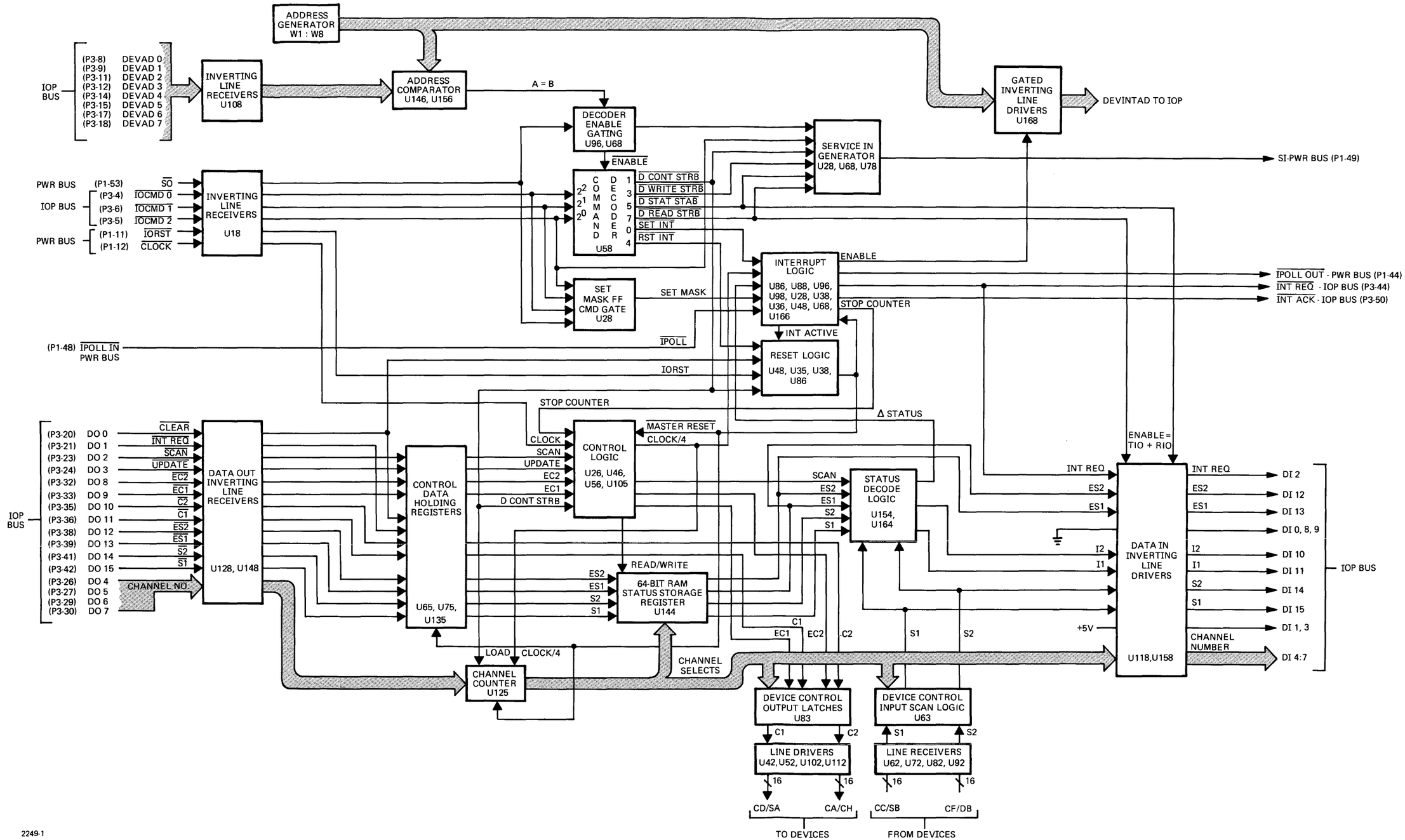
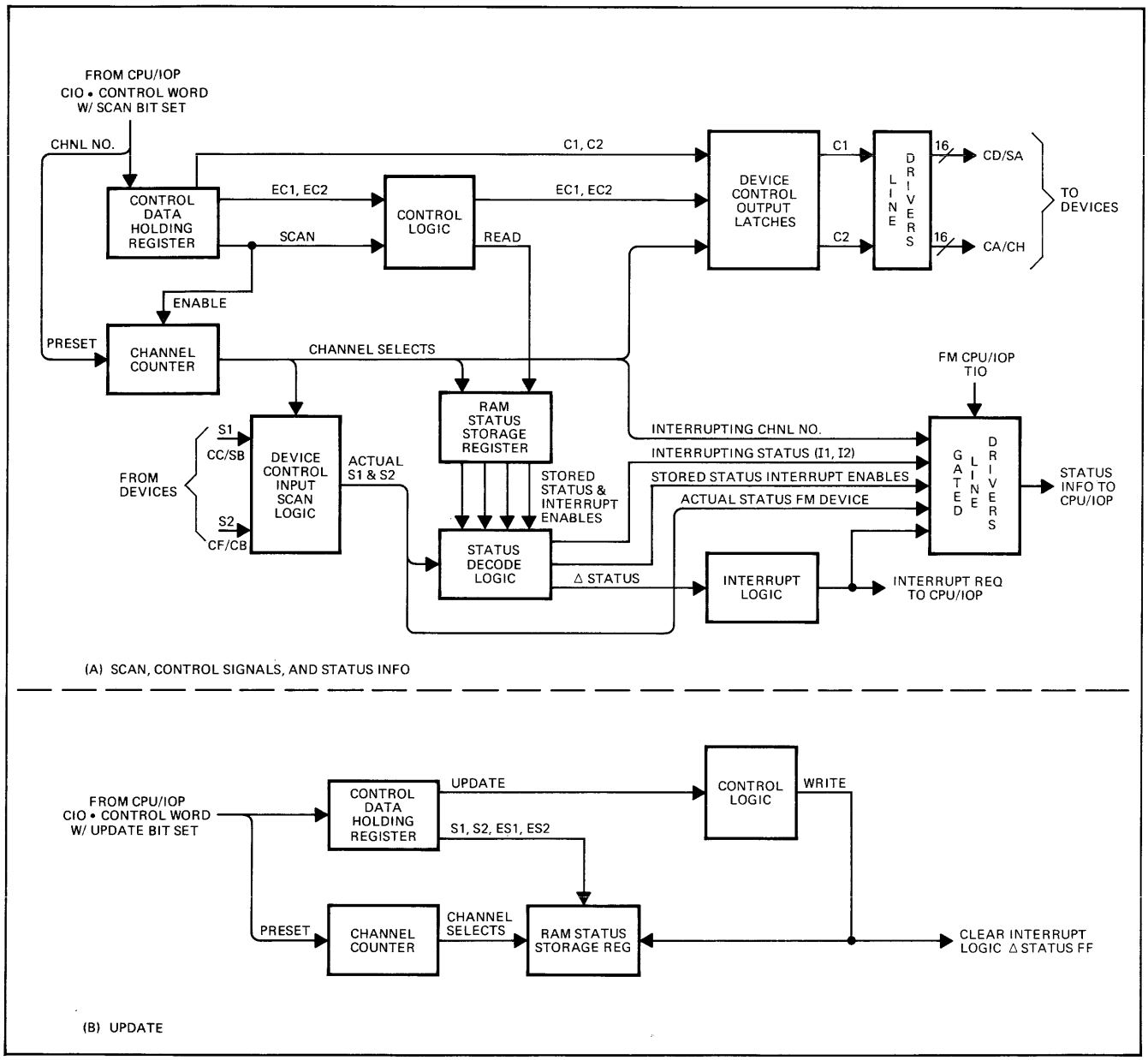


Figure 3-5. TCI Functional Block Diagram



2249-10

Figure 3-6. TCI Simplified Signal Flow

3-83. The three direct I/O command bits (IOCMD 0:2) are routed to the BCD-to-decimal command decoder via inverting line receivers. When the eight bits of the device address on the IOP bus correspond to the eight address bits from the address generator, the address comparator generates a true compare (A=B) signal. This signal and the Service Out signal are "anded" to provide an Enable signal to the command decoder. The decimal equivalents of the BCD inputs are shown beside each of the six possible decoder outputs. Four of the decoder outputs and I/O Command bit 2 are "or-ed" to provide the Service In acknowledgment signal required by the CPU/IOP. Note that RIO and TIO direct commands, decoded as Direct Read and Direct Status Strobes, are also "or-ed" to derive the Data In Driver Enable signal. For a read or a status-fetch operation, this signal gates data and/or status signals onto the IOP bus for transfer to the CPU/IOP.

3-84. INTERRUPT GENERATION AND PROCESSING.

3-85. The TDI interrupt processing logic consists of four flip-flops and associated gates. As shown in simplified logic diagram figure 3-8, these flip-flops are called Interrupt Mask, Interrupt Request, Interrupt Latch, and Interrupt Active. Setting the Interrupt Mask FF qualifies one condition for setting the Interrupt Latch FF. If the Interrupt Mask FF is cleared, interrupts cannot occur. The Interrupt Mask FF input is connected to a jumper wire at the interface PCA side of the data out (from CPU) line receivers. These line receivers are always enabled, but do provide isolation between the interface PCA and IOP bus data lines. Connections are provided to connect the jumper wire from the Interrupt Mask FF input to any of the 16 I/O data lines, to +5 Vdc, or to a signal ground. A +5 Vdc connection

or a connection to any I/O data line that is high allows the Interrupt Mask FF to set on the positive-going edge of the Set Mask FF signal (clock input) from the command decoding logic. The flip-flop can be preset by a Master Reset signal that occurs following an I/O Reset signal from the IOP or following a Direct Control Strobe with control word bit 0 set. Clearing the Interrupt Mask FF requires an input connection to signal ground or to any I/O data line that is low when the clock input occurs. Connecting the Interrupt Mask FF to an I/O data line allows the I/O driver Set Mask (SMSK) instruction to control the state of the flip-flop. When the Set Mask instruction is executed, the 16-bit word on top of the stack is output over the IOP bus to the I/O data out line receivers. The resulting Set Mask command is decoded and combined with the Service Out signal to clock the Interrupt Mask FF. This allows the Interrupt Mask FF to be set and/or cleared by any selected bit of the 16-bit word on the IOP bus.

3-86. The set-side output from the Interrupt Mask FF is combined with the output of the Interrupt Request FF and the resulting signal is applied to the input of the Interrupt Latch FF. (Note that the state of the Interrupt Request FF is determined by set or reset direct commands, or by the Flag input from the up/down transfer control logic.) Output from the Interrupt Latch FF follows the input as long as the clock input remains high. When the clock input goes low, the flip-flop is latched in the state indicated by the last input signal level. A high input signal, when the clock input goes low, latches the flip-flop in the set state. The clock input to the Interrupt Latch FF is provided by the Interrupt Poll In signal from the IOP bus. As long as the flip-flop input remains low, the Interrupt Poll In signal propagates through one gate on the interface PCA and is returned to the IOP bus as the Interrupt Poll Out signal. If the Interrupt Latch FF is latched in the set state, the clear-side output inhibits the Interrupt Poll Out signal. This prevents an interrupt from any lower priority device until the Interrupt Latch FF is cleared.

3-87. The outputs from the Interrupt Mask and Interrupt Request FFs are also combined and inverted and then sent to the IOP as the Interrupt Request signal. This signal, when generated, is responded to by the IOP sending the Interrupt Poll to all interface PCA's. On the interface PCA that is requesting an interrupt, the signal latches the Interrupt Latch FF and, after a short delay, enables the device address enable gate. The device interrupt address output is sent through IOP bus lines to the IOP. The delayed Interrupt Poll In signal is also inverted to direct set the Interrupt Active FF. Setting the Interrupt Active FF sends an Interrupt Acknowledge signal to the IOP to indicate that the device requesting an interrupt has its address available on the IOP bus lines.

3-88. The IOP drops the Interrupt Poll signal upon receipt of the Interrupt Acknowledge signal. The clear-side output from the Interrupt Active FF is sent to the Interrupt Latch FF to clear it, and generate a reset signal to the Interrupt Request FF. However, the Interrupt Active FF remains set until the interrupt request is serviced and the IOP sends an I/O Reset signal or a Reset Interrupt direct command.

3-89. The Flag input from the up/down transfer control logic that serves to clock the Interrupt Request FF must be cleared before any other channel can generate an Interrupt Request. The Flag signal is cleared upon receipt of a CIO direct command with bit 15 of the control word set. Refer to paragraph 3-90 for additional details.

3-90. UP/DOWN TRANSFER CONTROLS.

3-91. The up/down transfer control logic is shared by all TDI channels and generates the control signals for all word transfers. This logic, as shown on simplified logic diagram figure 3-9, consists of four flip-flops and associated gating. Note that the Initialize FF (part of the reset logic group of figure 3-2) is included in figure 3-9 for clarity.

3-92. The Initialize FF is set on receipt of a CIO command (decoded as Direct Control Strobe) and a control word with I/O Reset bit 0 set. The Initialize signal thus generated clears the up/down transfer control logic and is routed as a clear signal to other logic groups.

3-93. For transfer down operations, the Direct Control Strobe and control word bit 14 set start transfer control functions. Down Address Buffer Load results from the "anding" of these two signals and serves to strobe the control word channel address into the down address buffer shown in figure 3-16. The trailing edge of Down Address Buffer Load sets the Request Down Transfer FF. This causes Read/Write OK to inform the CPU/IOP that the TDI is busy. When Transfer Clock occurs the Transfer Down Flag FF is set, maintaining the Read/Write OK disable and clearing the Request Down Transfer FF. The logic remains in this state until Match occurs. Match is the true compare between the control word channel number in the down address buffer and the TDI address counter outputs. Match occurs within 69.4 microseconds for valid channel numbers and is "anded" with the set-side output of the Transfer Down Flag FF to generate Transfer Down. When the next Transfer Clock occurs, the Transfer Down Flag FF is cleared. Now Read/Write OK informs the CPU/IOP that the TDI is available for data transfers.

3-94. The Buffer Flag input to the Transfer Up Flag FF occurs at the end of either character transmission or reception. When Buffer Flag, Decision Pulse, and Logic Clock occur, the Transfer Up and Up Latch Load pulses are generated. Then Transfer Clock sets the Transfer Up Flag FF, generating the Flag signal. The Transfer Up pulse is looped to the flag control logic to clear Buffer Flag. The Up Latch Load pulse strobes the current (interrupting) channel number into the up address buffer and strobes the status input buffer and data input buffer. The leading edge of the Flag signal is routed to the interrupt logic to set the Interrupt Request FF.

3-95. The Transfer Up Flag FF remains set until the interrupt is acknowledged by a CIO command and a control word with bit 15 set. When this occurs, the Transfer Acknowledge FF is cleared. The next Transfer Clock clears the Transfer Up Flag FF which loops back to preset the Transfer Acknowledge FF.

3-96. MAIN/DIAGNOSE CHANNEL LOAD CONTROLS.

3-97. Receive channel and auxiliary channel loading is handled by an input multiplexer and the main/diagnose channel select logic shown on simplified logic diagram figure 3-10. The Auxiliary Channel input from the timing and address control logic enables the input multiplexer and disables the Auxiliary Channel Memory FF output during main channel window times. Simultaneously, the Main Channel input enables the output of the Input Buffer FF. Thus, for auxiliary channel window times, the Line signal is the bit contained in the Auxiliary Channel Memory FF. For the main receive channel window times, the Line signal is the bit received via the input multiplexer and Input Buffer FF on the leading edge of Decision Pulse.

3-98. Assume that a receive channel has its Diagnose parameter bit set. One output of the Input Buffer FF is "anded" with the Receive, Diagnose, and Decision Pulses and loaded into the Auxiliary Channel Memory FF by Logic Clock. When the diagnose channels start to pass through the memory window, Auxiliary Channel allows the received bit stored in the Auxiliary Channel Memory FF to be routed as the serial Line input and loaded into each auxiliary memory location. Last Channel Detect occurs at the end of each memory revolution. At this time, it provides a clearing input to the Auxiliary Channel Memory FF.

3-99. Assume now that a send channel has its diagnose parameter bit set. The New Bit (least significant bit in the memory location), Send, Decision Pulse, and Diagnose signals are "anded" and loaded into the Auxiliary Channel Memory FF by Logic Clock. When Auxiliary Channel occurs the stored bit is passed as the Line input to each auxiliary channel memory location. Again, Last Channel Detect clears the Auxiliary Channel Memory FF at the end of the memory revolution.

3-100. FLAG CONTROLS.

3-101. The flag control logic performs the flag control functions. The logic consists of gating networks that function as shown in simplified logic diagram figure 3-11.

3-102. On a receive channel, Stop is generated when the bit counter has reached its maximum count and the start bit of the character received is located in the least significant bit position in the accumulator (character is right-justified). On a send channel Stop is generated when the bit counter reaches its maximum count. Stop, therefore, can be interpreted as end-of-character sent or received. Stop is "anded" with Enable (individual channel interrupt enable parameter bit) to generate Set Buffer Flag providing that Buffer Flag is not already set. If Buffer Flag is already set, the Character Lost Flag is set. When Transfer Up occurs, both of these flags are cleared.

3-103. The Break Flag is set upon receipt of a start bit (Start) on a received channel. The Break Flag remains set until the Line input indicates a marking bit in the received character, at which time the Break Flag is cleared. At high character rates this flag may cause invalid break status to be generated for the previous character.

3-104. The Start Bit Flag is set by Receive Start and held set until the Shift pulse occurs one-half bit-time after the beginning of the start bit. This logic is used to ensure receipt of a valid start bit.

3-105. SHIFT CONTROLS.

3-106. The shift control logic consists of a series of gating networks used to generate loading and serial or parallel shift control signals to the memory window logic for both send and receive channels. Figure 3-12 is a simplified logic diagram of this function.

3-107. For transfer down operations, bit 0 of the word strobed into the data-out holding register defines whether the word contains parameters or data. When Transfer Down is generated (by a CIO command and control word with bit 14 set) and bit 0 in the holding register specifies data, Data Transfer is generated. When Decision Pulse occurs: (1) Data Mux Enable enables the data multiplexers; (2) Data Mux Load selects the outputs of the holding register for input to the accumulators; and (3) Parallel Clock strobes the multiplexer selections into the accumulators. During ensuing bit-by-bit transmission of the word just loaded, the Parallel Clock is disabled during each Decision Pulse to hold the window contents static for the duration of the Decision Pulse. Each time both Shift pulse and Decision Pulse occur, however, Parallel Enable is disabled. At the memory window logic, this disables the Parallel Clock and enables the Serial Clock, causing a serial shift of one bit position in the accumulators.

3-108. For transfer down operations where bit 0 specifies a parameter word is in the holding register, Parameter Transfer is generated at the time Transfer Down is generated. Parameter Transfer and Decision Pulse generate Parameter Mux Load, enabling the parameter multiplexers in the memory window to select the holding register contents. Parameter Transfer holds Parameter Latch Clock enabled during Decision Pulse to strobe the holding register contents into the parameter latches. At subsequent Decision Pulse times, Parameter Latch Clock is disabled to prevent the parameter latch contents from parallel-shifting.

3-109. Buffer Clock is disabled during every Decision Pulse period except when Stop is generated at end-of-character times. When Buffer Clock occurs, the outputs of the accumulators are strobed, in parallel, into the buffers.

3-110. On receive channels, when Receive Start is generated, the data multiplexers are disabled (via disabling Data Mux Load) and Parallel Clock is enabled. The purpose of this is to clear the accumulators preparatory to loading bit serial data from a device.

3-111. START, STOP, COUNT, AND RIGHT-JUSTIFY CONTROL FUNCTIONS.

3-112. The start, stop, count, and right-justify control signal generation is performed by the logic shown in simplified logic diagram figure 3-13.

3-113. Consider first the signals generated on a receive channel. In sequence they are Receive and Line which generate Start Condition; Start Condition and Active to generate Start; Start, Decision Pulse, and Receive to generate Receive Start; Transfer Clock, Start Bit Flag, and Line to generate Noise Reset (bit counter clear) if the seeming start bit received is not of at least one-half bit-time duration; Bit Counter and Sample Counter Preset Enables; Shift pulse; and Start Bit Detect and Bit Counter Carry that generate either Right justify and then Stop or only Stop.

3-114. The Receive signal is present when the address counter is stepping through the 16 receive channel addresses. A start-bit-level Line input during Receive generates Start Condition. If the bit counter count is at zero, the Active and Start Condition signals generate Start. This Start signal performs three functions: (1) "anded" with Receive and Decision Pulse generates Receive Start; (2) generates Bit Counter and Sample Counter Preset Enables; and, (3) at the flag control logic causes Start Bit Flag to be generated and looped back to this logic to generate Noise Reset if necessary.

3-115. When Receive Start is generated, one of its functions is to enable multiplexers in the memory window to derive a sample counter preset count based upon the contents of the baud-rate latches. (Normally, these multiplexers simply form a path between the baud-rate latches and the sample counters.) Then when Sample Counter Preset Enable occurs, the counters are preset to the derived count rather than the stored parameter. Thus, the Shift pulse (sample counter carry output) occurs approximately one-half bit-time after the beginning of a start bit. Following the start bit, since Receive Start is no longer present, the sample counter is preset to the stored count and full one-bit intervals are counted out thereafter. Note that the Shift pulse generates Sample Counter Preset Enable for all but the start bit.

3-116. The Bit Counter Carry Out signal occurs during the presence of the Shift pulse. If the start bit of the received character is detected (accumulator LSB+1 position), and if Receive is present, the Start Bit Detect signal is generated. This signal and the Bit Counter Carry Out input generate the Stop output to the shift control logic. If the Bit Counter Carry Out input occurs and Start Bit Detect does not, Right Justify is generated. The Right Justify signal prevents the Shift signal from presetting the sample counter. So Shift remains present and Bit Counter Carry Out remains present until Start Bit Detect occurs. The Right Justify signal, routed to the shift control logic, causes serial-shifting of the accumulator contents every revolution until Start Bit Detect can be generated.

3-117. The functions of this logic for a send channel are quite similar. The Data Transfer input (Transfer Down and holding register bit 0) and Send (address counter output) generate Start Condition. The Receive Start, Noise Reset, and Right Justify signals are not generated for a send channel. Only the Bit Counter Carry Out is used to generate Stop. All other functions are the same.

3-118. ECHO AND SEND DATA OUTPUT CONTROLS.

3-119. The echo and send data output functions are performed by the logic shown in simplified logic diagram figure 3-14. The logic consists of the gating networks of the old/new bit select logic and the output shift registers and output latches.

3-120. On a receive channel configured for echo (Echo parameter bit in memory set), a bit received from a device is buffered at the Input Buffer FF, routed to this logic, loaded into the output registers, and sent back to the device after approximately a one-half bit-time delay. The Line input from the Input Buffer is "anded" with the Echo, Shift, and Receive signals and loaded (New Bit) serially into the output register by the Output Register Clock. Note that if the Echo bit is not set, when the Shift pulse occurs, the Old Bit which is the output register serial output is looped back and reloaded into the output register.

3-121. On a send channel when a Shift pulse occurs, the bit occupying the LSB accumulator position (Send Bit) is "anded" with the Shift and Send signals. This New Bit is loaded serially into the output register and replaces the Old Bit. When the Shift pulse is not present, the Old Bit loops from the output register serial output and is reloaded into the serial input.

3-122. Note that the Output Register Clock results from the "anding" of Decision Pulse, Main Channel, and Logic Clock signals. When the address counter is stepping through the addresses of the auxiliary channels the Output Register Clock is disabled by the absence of the Main Channel signal. Thus, each of the bits are situated in their respective output register locations for each channel at the time of the Last Channel Detect strobe. This strobe occurs at the end of each memory revolution to load the output latches for each channel with the contents of the output registers.

3-123. LOGIC TIMING AND ADDRESS CONTROLS.

3-124. The logic timing and address control signals are generated by the logic shown in simplified logic diagram figure 3-15. This logic consists of a 4.32 MHz crystal oscillator, a one-shot multivibrator; two four-bit binary counters; a comparator; a flip-flop; and associated gates. (Refer to figures 4-8 and 4-9 for clock relationships and address generation timing.)

3-125. The field counter outputs are used to derive the Decision Pulse every count of seven for the duration of one clock period (230 nanoseconds). One field counter output (2^3) and three address counter outputs (2^0:2^2) are used as the Address Select signals. The state of the address counter 2^3 output specifies whether the address is that of a send or a receive channel. The count sequence is receive channels 0 through 15, (memory addresses 0 through 15), send channels 0 through 15 (memory addresses 16 through 31), and auxiliary channels 0 through 4 (memory addresses 32 through 36). The carry (C_N) outputs of the field and address counters are "anded" to set the Auxiliary/Main FF

during addresses 32 through 36. This enables the Auxiliary Channel strobe and disables the Main Channel strobe. The Last Channel Detect strobe is count 37 decoded. It is used to preset the field and address counters to count 1 and clear the Auxiliary/Main FF.

3-126. The address comparator Match output is generated when the A- and B-sets of inputs compare. The B-set of inputs consist of Send/Receive from data out holding register word bit 1, and control word bits 2 through 6 from the down address buffer. When Match occurs, the memory location of the comparing addresses is situated in the register window and available for loading or unloading.

3-127. DOWN BUFFER CONTROLS.

3-128. The two down buffers are the down address buffer and the data out holding register shown in figure 3-16. The down address buffer is controlled by the Down Address Buffer Load strobe derived from a decoded CIO command and a control word with bit 14 set. The down address buffer is used to hold the channel address of the control word. The outputs of this buffer are one set of inputs to the address comparator.

3-129. The data out holding register is used to hold parameter and data words transferred to the TDI from the CPU/IOP. The decoded WIO command provides the loading strobe. The bit 0 position (DO0) in this register specifies whether the register contains parameters or data. The bit 1 (DO1) position in this register specifies send channel or receive channel, and is used in conjunction with the channel number in the control word to address a channel. Bits 2 through 15 (DO2:DO15) contain parameters or data. If the parity parameter bit is set, the parity checker/generator computes the modulo 2 sum of bits 9 through 15 and replaces bit 8 with the result of this computation. If the parity bit is not set, bit 8 contains the parity for the word as received from the CPU/IOP.

3-130. UP BUFFER CONTROLS.

3-131. The up buffers are the up-address, data-in, and status input buffers shown in figure 3-17. The up-address and data-in buffers are loaded by the Up Latch Load strobe from the up/down transfer control logic. The output gates of these buffers require Direct Read Strobe (decoded RIO command) for output. The decoded RIO command also provides the Data In Driver Enable signal that enables information to be placed on the IOP bus.

3-132. A decoded TIO generates the Direct Status Strobe and the Data In Driver Enable to place status information on the IOP bus for transfer to the CPU/IOP.

3-133. RECIRCULATING MEMORY FUNCTIONS.

3-134. The recirculating memory is part MOS logic and part TTL logic as shown in figure 3-18. The clock for the MOS logic differs from that used for the TTL window logic: Transfer Clock 2 is used to derive the two-phase clock needed for the MOS logic.

3-135. The contents of the entire memory shift in parallel for seven clocks, remains static for one clock period (Decision Pulse time, 230 nanoseconds), and commences parallel-shift for another seven clocks. Transfers up or down on the IOP bus are in parallel. Transfers to or from a device are bit serial. The entire memory window is controlled by the shift control, flag control, and start-stop-count-right justify logic previously discussed.

3-136. TDI PCA DETAILED SEQUENCE OF OPERATION.

3-137. The following paragraphs contain the detailed operating sequences for parameter loading, character transmission, and character reception.

3-138. PARAMETER LOADING.

3-139. The CPU/IOP unloads a WIO command, DEVAD, SO, and parameter word onto the IOP bus after fetching a status word with a TIO command to see if the TDI is available for a write operation. Read/Write OK status word bit defines TDI status at the CPU/IOP. The TDI decodes WIO and returns Service In (SI). The WIO decoding generates Direct Write Strobe. The leading edge of Direct Write Strobe loads the parameter word into the data out holding register. The CPU/IOP then issues a CIO command, Device Address, Service Out, and a control word with bit 14 set. The TDI decodes the CIO command, returns Service In, and generates a Direct Control Strobe. This strobe and bit 14 generate the Down Address Buffer Load signal to load the control word channel address into the down address buffer. This signal is also routed to the up/down transfer control logic where it sets the Request Down Transfer FF. This causes Read/Write OK to inform the CPU/IOP upon any subsequent TIO, that the TDI is seeking the addressed channel memory location and has not as yet loaded the parameter word just received. (An improper channel address is indicated if Read/Write OK remains for more than 69.4 microseconds.) The next Transfer Clock occurring after Down Address Buffer Load sets the Transfer Down Flag FF, maintaining Read/Write OK, and clearing the Request Down Transfer FF.

3-140. Bit 1 (logic 1 for a receive channel, logic 0 for a send channel) in the data-out holding register and the contents of the down address buffer are the A-set of inputs to the address comparator. The field and address counter outputs are the B-set. When these compare, a Match signal is routed to the up/down transfer control logic where it and the set-side output of the Transfer Down Flag FF generate a Transfer Down signal until the next Transfer Clock.

3-141. Transfer Down is routed to the shift control logic where it and the data holding register bit 0 output are "anded" with Decision Pulse (DP) to generate Parameter Mux Load and then the Parameter Latch Clock signals. At the same time, the Data Mux Load and Parallel Clock

signals at the data accumulator/buffers are disabled since a parameter word, not data, is being loaded. At the time of Parameter Mux Load the parameter word being retained in the data out holding register is selected by the parameter, baud-rate, and character-size multiplexers. When Parameter Latch Clock occurs, the parameter word selected by the parameter multiplexers is strobed into the lower control buffer, rate counter, and character size buffer/control latches. Note that the preset enable inputs of the counters are disabled so the counters cannot be preset at this time.

3-142. The window time allotted to each address is approximately 230 ns, the pulsewidth of one Decision Pulse. The foredescribed functions were performed during the Decision Pulse that occurred while the Match signal was asserted. Now the parallel clock is re-enabled and the first field of the next address is being clocked in parallel into the window and the first field of the address just loaded with the parameter word is moving into the MOS logic.

3-143. Note that the CPU can configure any of the 16 send, 16 receive, or 5 auxiliary channels with specific parameters. This is done by issuing a logic 1 parameter word bit 1 to select a send channel or a logic 0 bit 1 to select a receive channel. To send parameters to an auxiliary receive-only channel, a logic 0 parameter word bit 1 must be issued along with a logic 1 bit 2 of the control word.

3-144. CHARACTER TRANSMISSION.

3-145. Assume now that the CPU wishes to send a word to a crt terminal. Assume also that the channel configured in the foregoing paragraphs was configured with the 2400-Hz baud rate and character size required by this terminal. The complement of the parameters in the data out holding register were loaded into the parameter latches, and are to be used to preset the sample and bit counters. The sample counters are to be set so that they must count up six times before a carry (Shift pulse) can be generated. The bit counter must count up once per sample counter carry for a total of 10 bits before the bit counter carry can occur. Thus, the sample counters are preset to 005_8 and the bit counter is preset to 001_2.

3-146. The CPU issues a WIO command and a data word and then a CIO command and a control word to the TDI. The WIO command generates a Direct Write Strobe to load the data word into the data out holding register. The CIO command is decoded as a Direct Control Strobe which, along with bit 14 of the control word, generates the Down Address Buffer Load signal. This signal strobes the channel address into the down address buffer and sets the Req Dn Xfr FF. (Transfer Down, Read/Write OK, and Match signals are generated per previous paragraphs.)

3-147. When the Transfer Down signal is generated and routed to the shift control logic, it is "anded" with data holding register bit 0 output and Decision Pulse to generate Data Mux Load at U131-3. Note that the data multiplexers are enabled by Data Mux Select at U101-1 when Data Mux Load is generated. Data Mux Select selects the contents of the data out holding register for input to the data accumulator/buffer. Data Mux Load strobes the contents into the latches. Transfer Down occurring for a data word on a send channel and the fact that the bit counter count is at zero generates Start (U103-1). Start and Decision Pulse preset the sample and bit counters to the counts in their respective latches.

3-148. Upon the absence of Decision Pulse, the Parallel Clock signal is re-enabled and the first field of the next address is clocked in parallel into the window while the first field of the address just loaded with data is clocked into the MOS logic. The data loaded into the crt terminal address is not put on line to the terminal for one bit time. During this bit time a stop bit belonging to the word previously transmitted to the terminal is maintained on-line to the terminal.

3-149. After the bit time, the sample counter carry output, Shift pulse is generated. At U82-6 the Shift inputs inhibit the Old Bit input and enable the Send Bit from the accumulator/buffers. The Send Bit then becomes the New Bit at U82-12. The first bit of the data word (New Bit) is loaded into the output register position for the crt terminal, replacing the stop bit (Old Bit) that was there. This bit, the sync or start bit, is loaded into the output latches and put on line to the crt terminal when the Last Channel Detect signal occurs at the end of that particular memory revolution. The Shift pulse also steps the bit counter once, enables one Serial Clock pulse to shift the accumulators at U131-6, and then presets the sample counters thereby clearing itself. Again, the sample counters proceed to count up once per revolution for the duration of another bit, six revolutions. Again, Shift pulse occurs to step the bit counter, replace the Old Bit with the Send Bit, allow serial-shifting in the accumulators one bit position, and re-preset the sample counters. Now the second bit of the data word received from the CPU is the New Bit and is loaded into the output latches and put on line to the crt terminal at the time of the next Last Channel Detect signal. The sample counters again proceed to count up for the second bit, once per revolution for the next six revolutions. This bit by bit transmission continues until the bit counter has been stepped ten times and the bit counter Carry Out output to U81-8 causes Stop to be generated.

3-150. Stop is routed to the flag control logic, gated with Buffer Flag (which should be clear), Transfer Up and Enable to generate Set Buffer Flag. (Note that if Buffer Flag was already set for this channel, the Character Lost Flag will be set.) The Buffer Flag signal is routed to the up/down transfer control logic where it is used to set the Transfer Up Flag FF and generate the Transfer Up and Up Latch Load signals. Transfer Up is routed to the flag control logic and used to clear Buffer Flag. (Transfer Up and Up Latch Load cannot be generated and Buffer Flag cannot be cleared if the Transfer Up Flag FF is already set. This situation could occur when some previous channel has generated an interrupt that has not been acknowledged. Acknowledgment entails CPU/IOP issuance of a CIO control word with bit 15 set to clear the Transfer Acknowledge and the Transfer Up Flag FFs. The Buffer Flag for this channel is held in memory and attempts to interrupt each

revolution until successful.) When the Up Latch Load signal is generated, the status bits and channel address are strobed into the status-in buffer. When the Transfer Up Flag FF is set, Flag sets the Interrupt Request FF. This interrupt sets up the chain of events described in paragraph 3-84.

3-151. CHARACTER RECEPTION.

3-152. Assume now that a receive channel is configured with the baud rate and character size parameters for the reception of one character with echo at 2400 bits per second. The complement of the specified parameters are stored in the parameter latches for the channel: 005_8 is stored in the baud rate latches and 001_2 is stored in the character-size latch.

3-153. A start bit input from the device on this channel is loaded into the Input Buffer FF by the Decision Pulse that occurs at the end of its address select period. The start bit is routed as the Line input to the flag control logic, old/new bit select logic, and data accumulator/buffer serial input. This Line input produces a Start Condition at U82-9. Start Condition and Active signals are "anded" to produce Start. This signal is then "anded" with Decision Pulse and Receive at U121-8 to generate Receive Start. The output of U103-4 provides the preset enable to the sample and bit counters. At the flag control logic, Start, Line and the absence of Break Flag cause Set Break Flag.

3-154. The Receive Start signal to multiplexers U84 and U124 alters the input to these devices. Instead of making the contents of the baud rate latches directly available as the preset inputs to the sample counters, the output of the latches is used to derive a count equal, approximately, to one-half bit-time. This occurs only for a received start bit. At the shift control logic, Receive Start and Decision Pulse are "anded" at U101-1 to disable the data multiplexers, while the absence of Transfer Down at U121-12 enables Parallel Clock. This results in clearing the accumulators by loading them with all zeros. At the flag control logic, Receive Start, the absence of Start Bit Flag, and Shift pulse are "anded" to generate a Set Start Bit Flag signal.

3-155. After three revolutions the sample counters reach maximum count and the Shift pulse occurs. At this time the bit counter is stepped once and the start bit Line input, gated at U71-8 and U72-8 with Shift pulse and Echo, is looped to the output registers as the New Bit. The Shift pulse also enables one Data Serial Clock pulse to the accumulators to load the serial Line input (start bit), and causes sample counter preset to the contents of the baud rate latches. At the flag control logic, the Shift pulse clears the Start Bit Flag.

3-156. Now, one bit, received from the device, is serially loaded into the accumulators and echoed back to the device every six revolutions until all ten bits are received. When Shift occurs for the tenth bit, the bit counter Carry Out is present at U81-10 and U81-5. At U81-8, Carry Out and Start Bit Detect are "anded" to produce Stop when the start bit occupies the next to last bit position in the accumulator. At U81-6, Carry Out and Start Bit Detect are "anded" to produce Right Justify when the start bit does not occupy the next to the last bit position in the accumulator. In the channel being described here, another serial clock is required to shift the character into the right justified position in the accumulator. Hence, Right Justify is generated to disable the bit and sample counters and maintain the carry outputs of each. The Shift output enables the Data Serial Clock on the next memory revolution. At this time, Start Bit Detect occurs to disable Right Justify and generate Stop.

3-157. The Stop signal enables Buffer Clock at U141-8 which loads the buffers with the contents of the accumulators. The Stop signal is also routed to the flag control logic and "anded" with Enable to generate Set Buffer Flag. (Note that if Buffer Flag is already set for this channel the Character Lost Flag will be set at this time.)

3-158. Buffer Flag is routed to the up/down transfer control logic. On the following revolution, provided that the Transfer Up Flag FF is not already set, the Buffer Flag signal causes the Up Latch Load, Transfer Up, and Flag signals to be generated. The Up Latch Load strobes the channel address and the data buffer contents into the up-address and data-in buffers respectively. The Transfer Up to the flag control logic clears Buffer Flag. And Flag sets the Interrupt Request FF.

3-159. TCI PCA FUNCTIONAL-LEVEL DESCRIPTION.

3-160. The TCI logic performs five functions: command decoding; interrupt generation and processing; status decoding, scanning, and updating; control signal generation; and device control signal generation. Each of these are discussed in the following paragraphs and are supported by simplified logic diagrams. Note that the logic shown on the simplified logic diagrams is keyed by set and grid reference numbers to a location on detailed logic diagram set 509. For example, 509C7 translates as diagram set 509, and represents logic found at grid coordinate C7.

3-161. COMMAND DECODING.

3-162. The command decoding function is performed by six units. These are the address comparator, address generator, decoder enable gating, service-in generator, command decoder, and set mask command decoder. These are shown in simplified logic diagram figure 3-19.

3-163. The three direct I/O command bits ($\overline{\text{IOCMD 0:2}}$) are routed to the BCD-to-decimal command decoder via inverting line receivers. When the eight bits of the device address on the IOP bus correspond to the eight address bits jumpered in the address generator, the address comparator generates a true compare (A=B) signal. This signal and the Service Out signal are "anded" to provide an Enable signal to the command decoder. The decimal equivalents of the

BCD inputs are shown beside each of the six possible decoder outputs. The four decoder strobe outputs are "or-ed" to provide the required Service-In acknowledgment signal. Note that the Direct Control Strobe (decoded CIO) is the only strobe output to the remaining TCI logic. The Direct Read and Status Strobes are "or-ed" to generate Data In Driver Enable. This signal is used for status fetch operations to gate the status word onto the IOP bus for transfer to the CPU/IOP.

3-164. INTERRUPT GENERATION AND PROCESSING.

3-165. The TCI interrupt generation and processing logic consists of five flip-flops and associated gates. As shown in figure 3-20, the flip-flops are called Interrupt Mask, Interrupt Latch, Interrupt Active, Status Change, and Interrupt Request.

3-166. The Interrupt Mask FF must be set in order to allow setting of the Interrupt Latch FF and generating of Interrupt Requests. The Interrupt Mask FF set-input is connected to a jumper wire at the interface PCA side of the data out (from CPU/IOP) line receivers. These line receivers are always enabled but do provide isolation between the TCI and the IOP bus data lines. Connections are provided to connect the jumper wire from the Interrupt Mask FF set input to any of the 16 I/O data lines, to 5 Vdc, or to signal ground. A 5 Vdc connection, or connection to any I/O data line that is high, allows the Interrupt Mask FF to be set on the positive-going edge of the Set Mask FF signal (clock input) from the command decoding logic. The flip-flop can be preset by the Master Reset signal. This signal occurs following an I/O Reset command from the CPU/IOP or following a Direct Control Strobe (decoded CIO command) with control word bit 0 set. The Interrupt Mask FF is cleared at the time of the clock input by connecting its set-input jumper wire to signal ground or to one of the 16 I/O data lines that is low at that time. Connected to one of the data lines, the state of that data line and the I/O driver Set Mask instruction can control the state of the Interrupt Mask FF. When the Set Mask instruction is executed, the 16-bit word on the top of the stack is sent via the IOP bus to the data out line receivers. The resulting Set Mask command is decoded and combined with the Service Out command to generate the Set Mask FF clock input. Hence, the Interrupt Mask FF can be set or cleared according to which bit of the 16-bit word its set-input is connected.

3-167. The set-side output of the Interrupt Mask FF is "anded" with the clear-side output of the Interrupt Request FF. The resulting signal is "anded" with the clear-side output of the Interrupt Active FF and the resulting signal is the input to the Interrupt Latch FF. The output of the Interrupt Latch FF follows this input as long as the clock input (Interrupt Poll In) is high. When the clock input goes low as a result of some device generating on Interrupt Request, one of two possible events occur. These events depend upon whether or not the Interrupt Latch FF is set or clear at the time of the clock. If the Interrupt Latch FF is set when the clock input (Interrupt Poll) occurs: (1) the TCI is requesting interrupt, (2) Interrupt Poll propagation stops, (3) the Interrupt Active FF is set, (4) the device interrupt address line drivers are enabled to place the device address on the IOP bus, (5) Interrupt Acknowledge is generated, and (6) the Interrupt Latch and Interrupt Request FFs are cleared. Once the Interrupt Active FF is set, it remains set until cleared by an I/O Reset command from the CPU/IOP, a Reset Interrupt command from the CPU/IOP, or a CIO command with control word bit 0 set. However, if the Interrupt Latch FF was clear at the time of the clock input, Interrupt Poll In and the clear-side outputs of the Interrupt Latch and Interrupt Active FFs propagate the poll and generate Interrupt Poll Out.

3-168. The TCI Interrupt Request FF is set by the clear-side output of the Status Change FF. This flip-flop, in turn, is set by the Δ Status input from the status decode logic. The Δ Status input occurs when one of the device status lines monitored by the TCI changes state. When a change-in-status interrupt occurs, the Status Change FF remains set until the status for the channel is updated. Note that the Stop Counter output stops the channel counter at the interrupting channel number until the Status Change FF is cleared. When a control word having the update bit set is received by the TCI, a Write signal is generated that clears the Status Change FF as well as performs updating functions for the status decode logic.

3-169. STATUS DECODE, SCAN, AND UPDATE OPERATIONS.

3-170. The status decoding, scanning, and updating is performed by the logic shown in simplified logic diagram figure 3-21. The major components of this logic are the control data holding register, the 64-bit status storage RAM, the status decode gating network, and two multiplexers. The purpose of this logic is to store four bits (two status bits and two status interrupt enable bits) for each of 16 channels, monitor the state of two status lines for each channel, and generate an interrupt (if enabled to do so) when a difference in state between the stored and actual status values is detected.

3-171. When a CIO command is decoded the control word is loaded into the control data holding register. If update bit 3 is set the Write signal is generated and control word bits 12 through 15 (S1, S2, ES1, ES2) are loaded into RAM in the location specified by the Channel Select inputs. (Note that control word bits 4 through 7 determine the channel selected for updating.) The complement of the four bits loaded are the RAM sense outputs to the status decode logic.

3-172. The RAM status storage register has two modes of operation, read and write. The write or update mode was just described. The read mode is the scan mode. During scan operation, the Channel Select inputs from the channel counter continuously sequence through the 16 channel addresses. During each address time the complement of the S1 and S2 status bits stored in RAM and the S1 and S2 inputs for that channel from the multiplexers are routed to the status decode logic. Here they are "exclusive-or-ed" to

verify that both S1 values compare and both S2 values compare. If, for instance, the S1 values are not comparable, and if the status interrupt enable bit (ES1) in RAM for S1 is set to enable an interrupt in the event of a change in status, the signal I1 is generated. (If the status interrupt enable bit for S1 is not set, no interrupt can be generated.) The Δ Status output to the interrupt logic is also generated because the Scan signal is present. The stored status for that channel must now be updated and scan resumed.

3-173. CONTROL FUNCTIONS.

3-174. The control logic shown in simplified logic diagram figure 3-22 is responsible for generating the control signals used by the TCI. The logic consists of the control data holding register, channel counter, Status Clear FF, Sync 1 and Sync 2 FF's, and the clock divider (÷4) consisting of two J-K flip-flops.

3-175. When Direct Control Strobe occurs (CIO command decoded), the control data holding register is loaded, the channel counter is preset to the channel number in the control word (DO4:7), and the Sync 1 FF is preset to disable the counter clock input. If control word Update bit 3 (DO3) is set, the Write signal is output to the 64-bit RAM status storage register when the Sync 2 FF is set. The set-side output of the Sync 2 FF enables the Write, EC1 and EC2 signals for one Clock/4 period. The clear-side output of the flip-flop clears the Sync 1 FF and maintains the counter clock disable. The next Clock/4 signal clears the Sync 2 FF. If the control word Scan bit 2 (DO2) is set, the holding register Scan output and the clear-side outputs of the Sync 1 and Sync 2 FF's are "anded" to enable the counter clock and scan operation resumes. If the Scan bit is not set the logic waits for another control word.

3-176. When the Master Reset is generated, the holding register and the channel counter are cleared and the Status Clear FF is preset. The clear-side output of the Status Change FF enables the counter clock for a complete count sequence, generates the Write signal to the RAM, and generates the EC1 and EC2 control signals to the device control signal output latches. This sequence causes the clearing of all RAM locations and all output latches.

3-177. DEVICE CONTROL FUNCTIONS.

3-178. The logic shown on simplified logic diagram figure 3-23 is responsible for the storage and output of the two control signals sent to each of 16 channels. The logic consists of part of the control data holding register used to temporarily store control word bits 10 and 11 (C1 and C2), four addressable output latches, and load enable gating. The Channel Select inputs address the output latch of a specific channel, EC1 and/or EC2 provide the load enable for that channel, and C1 and/or C2 are loaded into the addressed and load-enabled latch. Note that for the first eight addresses the counter MSB output enables one set of latches, and the other set of latches for the second eight addresses.

3-179. TCI PCA DETAILED SEQUENCE OF OPERATION.

3-180. The following paragraphs contain the detailed operating sequences for interface clearing and update and resume scan operation. Refer to detailed logic diagram set 509 and the flowchart (figure 4-15) in Section IV.

3-181. INTERFACE CLEARING.

3-182. A CIO direct command, Device Address, Service Out, and a control word with bit 0 set placed on the IOP bus for the TCI is acknowledged by Service In when the CIO command is decoded. Data-out bit 0 and the Direct Control Strobe are routed to the reset logic to generate Master Reset. Master Reset presets Status Clear FF U48-8 and clears the control data holding register, channel counter, and control logic system clock divider. See Figure 3-32.

3-183. The clear-side output of the Status Clear FF is routed to the control logic where it enables the channel counter clock for a count output of 0 to 15, generates Write signal to clear RAM, and generates EC1 and EC2 signals to enable clearing of the addressable output latches. The Status Clear FF is cleared on the trailing edge of the last channel address.

3-184. UPDATE AND RESUME SCAN.

3-185. A CIO command, Device Address, Service Out, and a control word with scan and update bits set placed on the IOP bus for the TCI is acknowledged by Service In when CIO is decoded. The Direct Control Strobe is used to load the control word into the control data holding register and to preset control logic Sync 1 FF. The clear-side output of the Sync 1 FF is used to temporarily disable the channel counter clock so that the address select outputs remain configured for the channel number specified in the control word. The next Clock/4 signal sets the Sync 2 FF. The Sync 2 FF set-side output along with the Update signal generates a Write signal to the RAM. The EC1 and EC2 input enables are also routed to the addressable output latches for one clock period, approximately 800 nanoseconds.

3-186. The Write signal causes the outputs of U135 to be stored in the Ram location specified by the outputs of the channel counter. The EC1 and EC2 signals enable the loading of the C1 and C2 outputs of U75 into the channel-counter-addressed output latch location. Meanwhile, the Sync 2 FF clear-side output continues the channel counter clock disable and has cleared the Sync 1 FF. When the Sync 2 FF is cleared by the next clock pulse, the Update and EC1 and EC2 outputs of U65 are disabled and the Scan outputs assume control. The channel counter commences counting and the status decode logic output to the Δ Status FF is enabled.

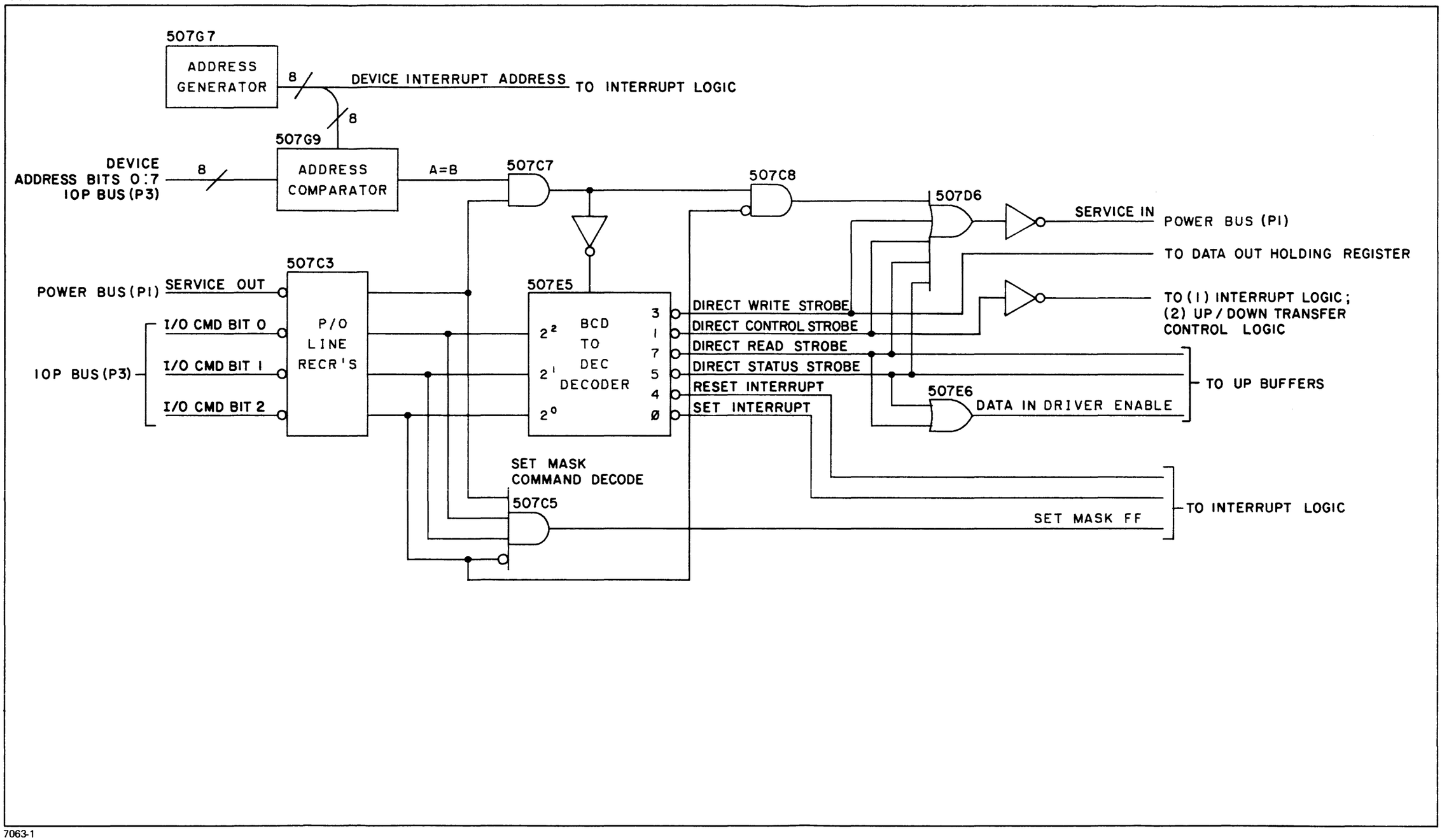
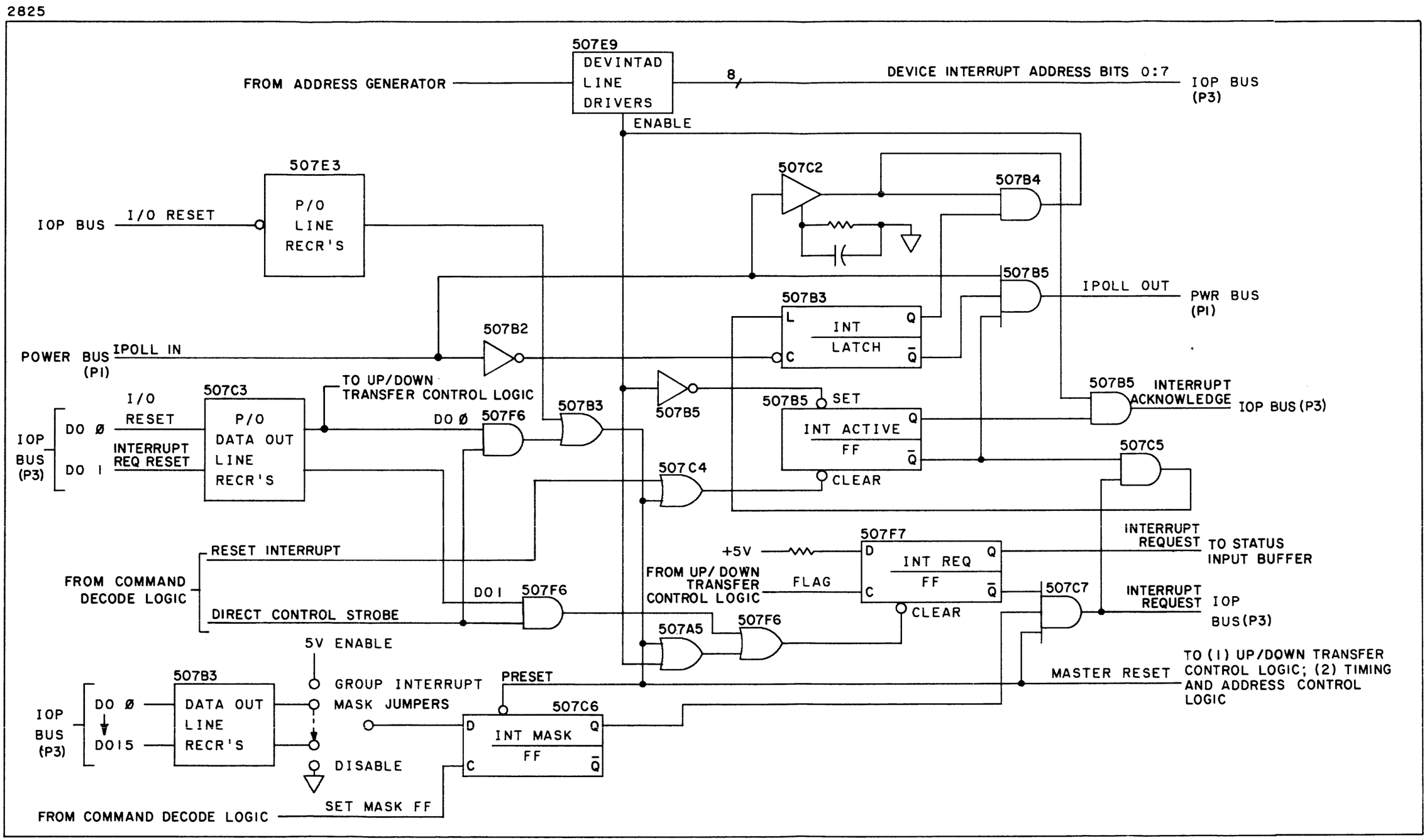


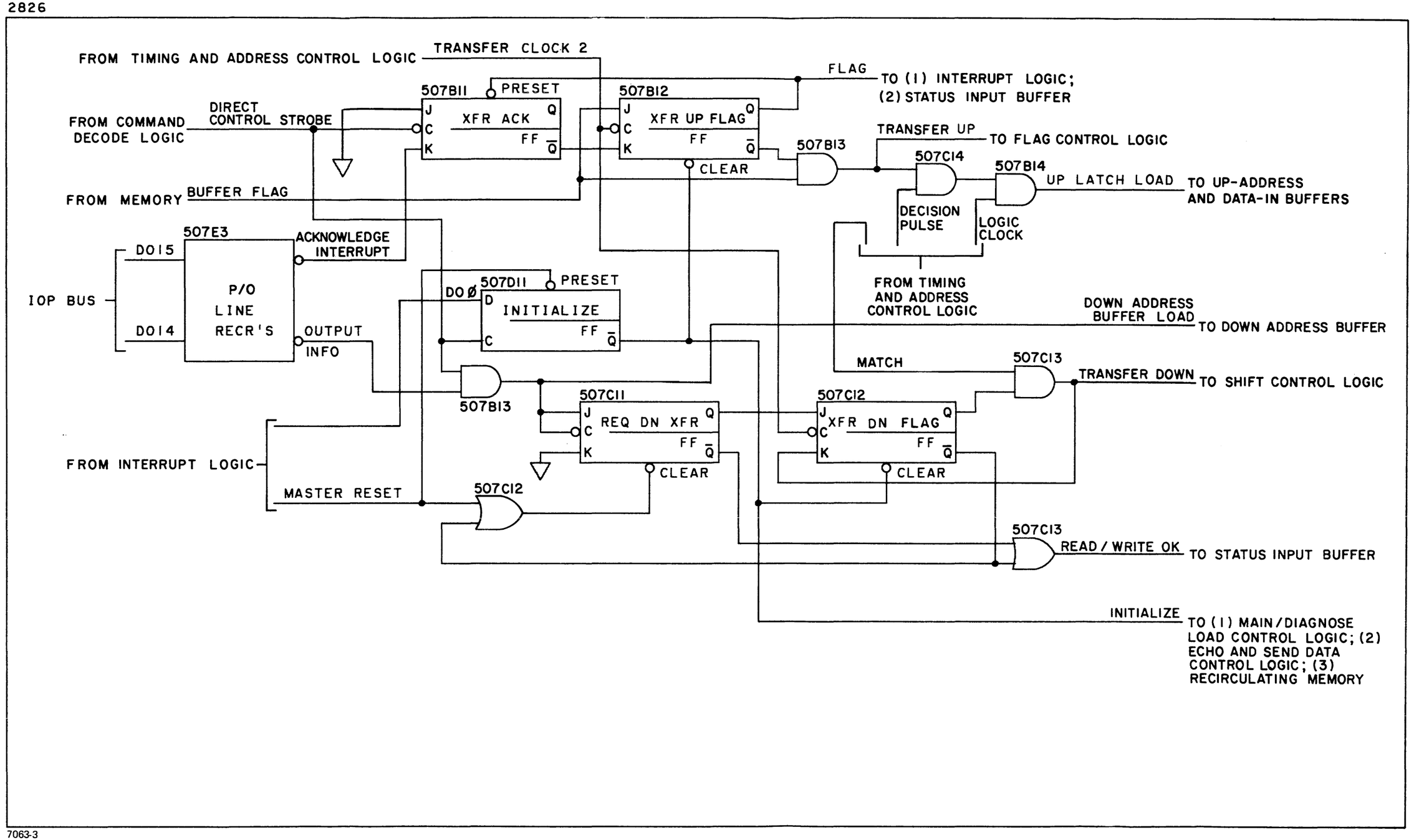
Figure 3-7. Terminal Data Interface Command Decoding



7063-2

Figure 3-8. Terminal Data Interface Interrupt Polling, Processing, and Acknowledge

2826



7063-3

Figure 3-9. Terminal Data Interface Up/Down Transfer Control Signal Generation

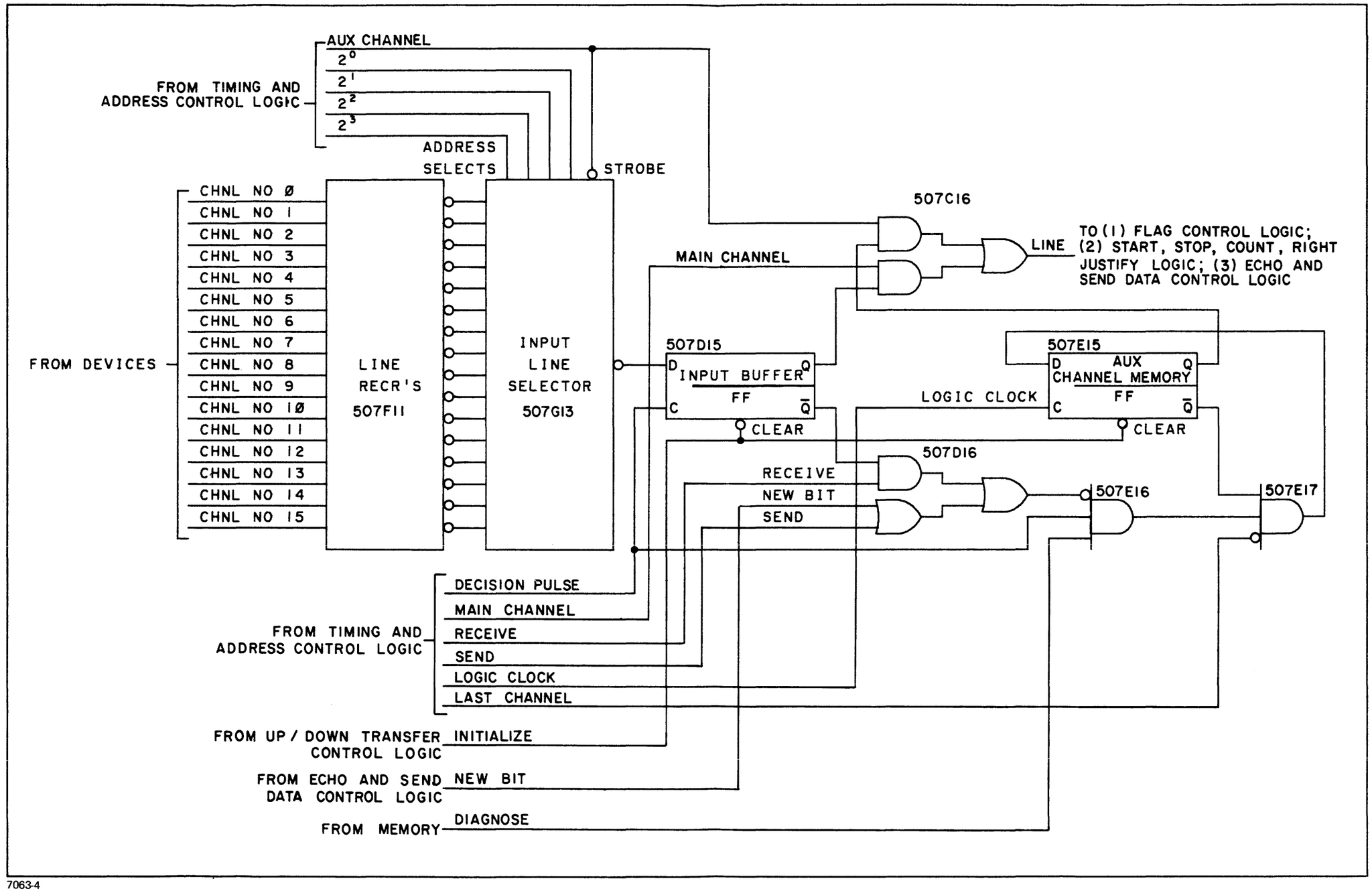


Figure 3-10. Terminal Data Interface Receive Buffer and Diagnose Channel Load Control

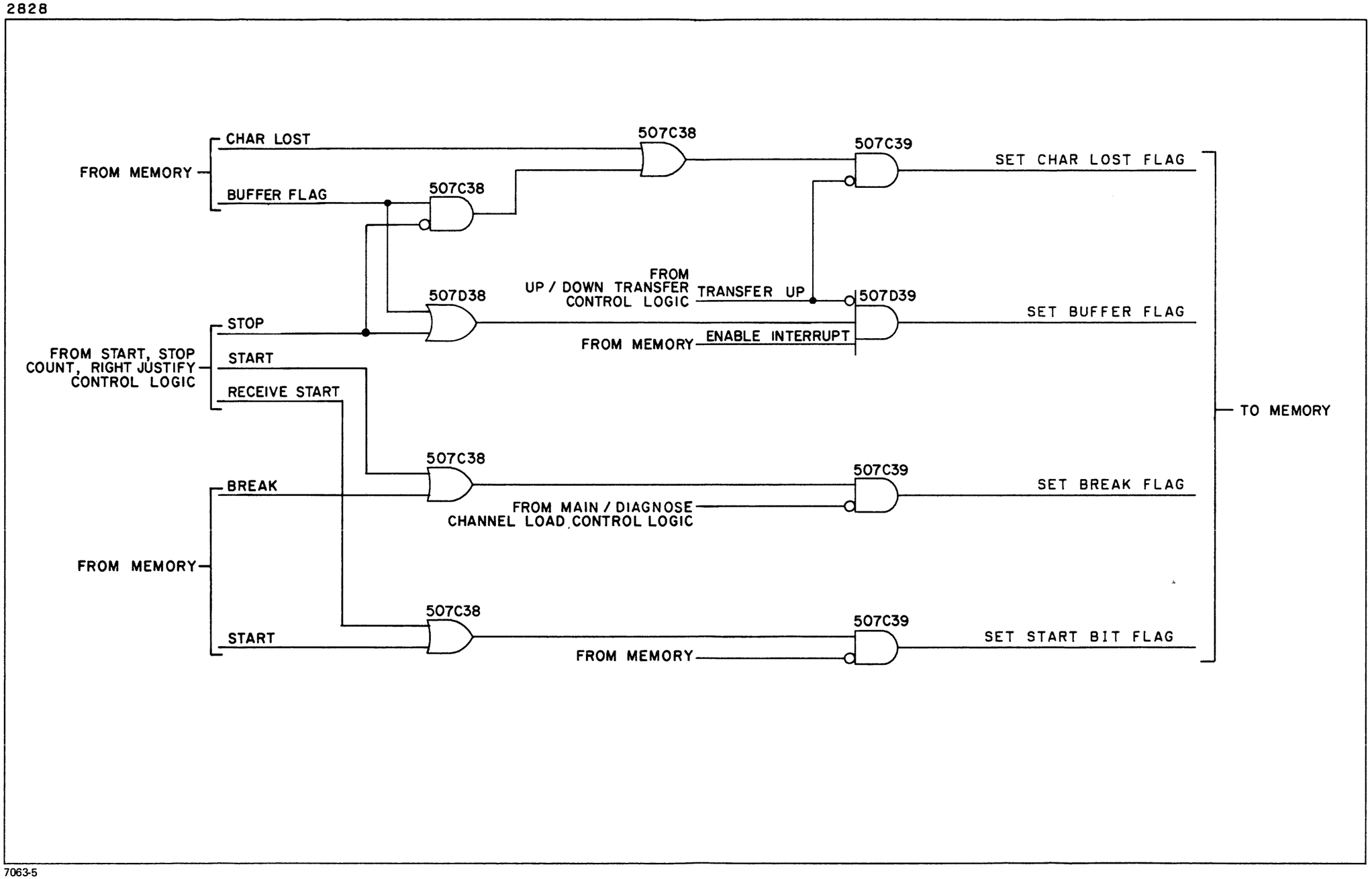


Figure 3-11. Terminal Data Interface Flag Control Signal Generation

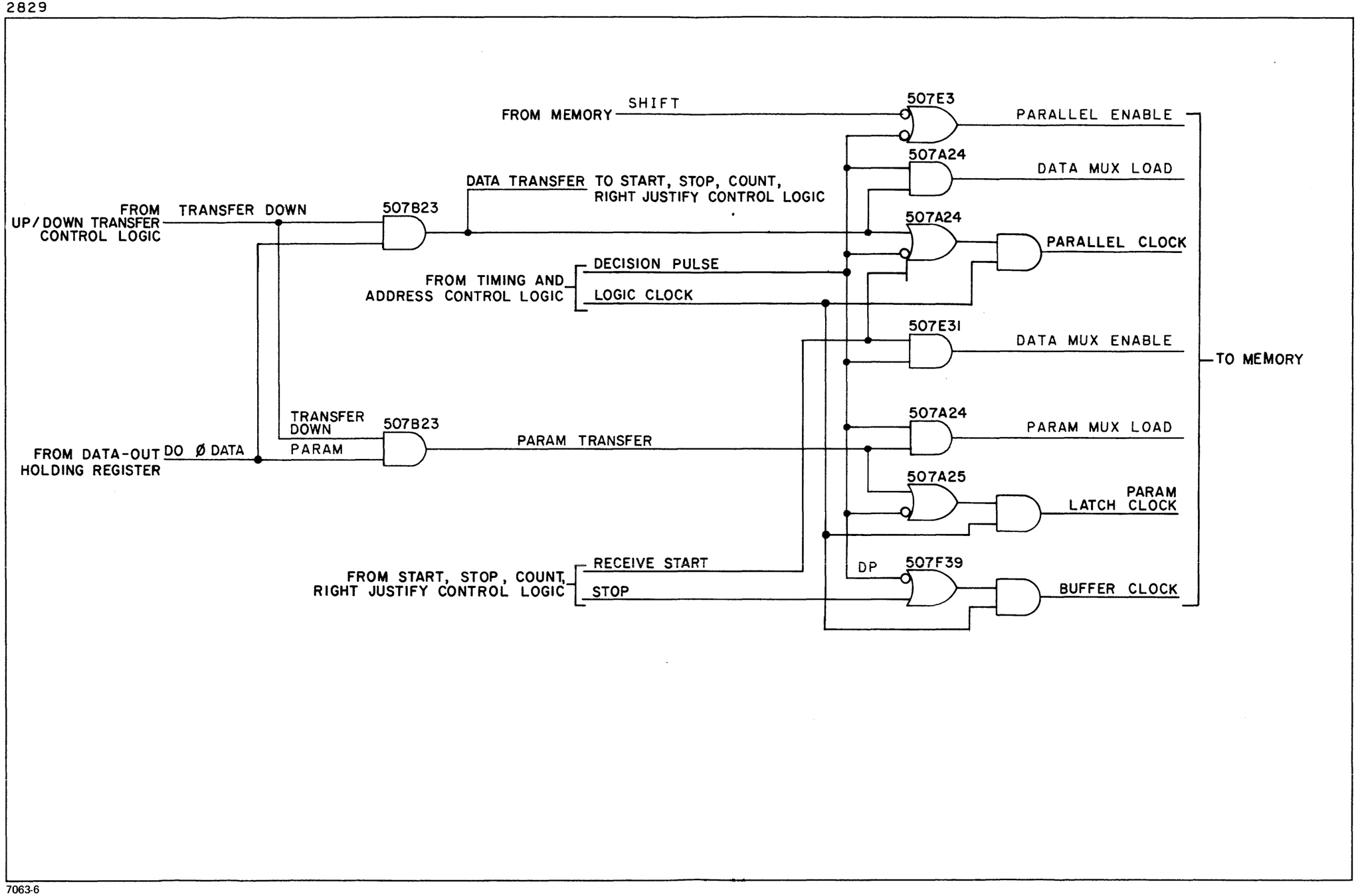
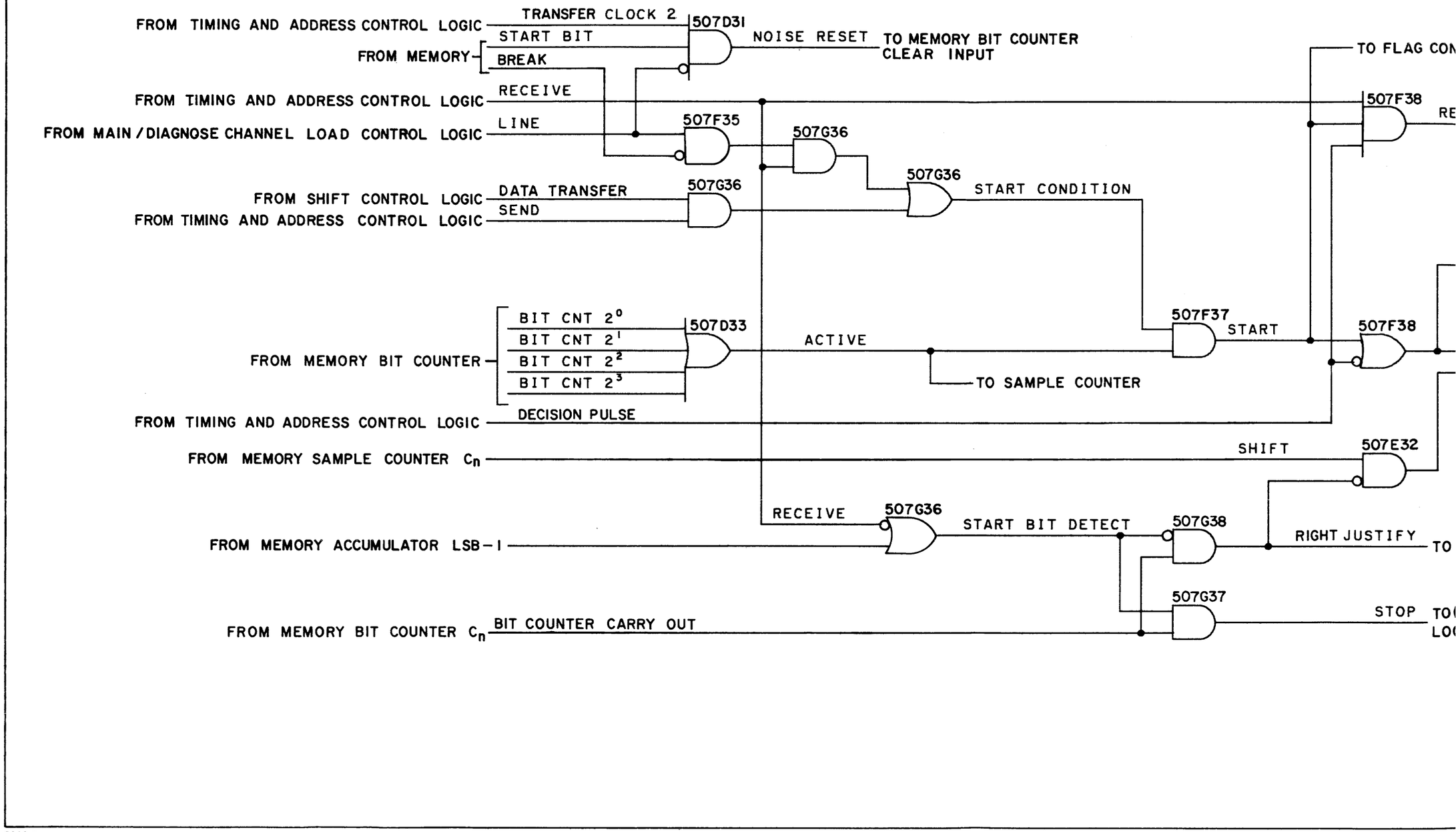


Figure 3-12. Terminal Data Interface Shift Control Signal Generation


FROM TIMING AND ADDRESS CONTROL LOGIC
TRANSFER CLOCK 2
START BIT
FROM MEMORY
BREAK
507D31
NOISE RESET
TO MEMORY BIT COUNTER CLEAR INPUT
TO FLAG CON
FROM TIMING AND ADDRESS CONTROL LOGIC
RECEIVE
FROM MAIN/DIAGNOSE CHANNEL LOAD CONTROL LOGIC
LINE
507F35
507G36
507F38
RE
507G36
FROM SHIFT CONTROL LOGIC
DATA TRANSFER
FROM TIMING AND ADDRESS CONTROL LOGIC
SEND
507G36
START CONDITION
BIT CNT 2⁰
BIT CNT 2¹
BIT CNT 2²
BIT CNT 2³
FROM MEMORY BIT COUNTER
507D33
ACTIVE
507F37
START
507F38
TO SAMPLE COUNTER
FROM TIMING AND ADDRESS CONTROL LOGIC
DECISION PULSE
FROM MEMORY SAMPLE COUNTER Cn
SHIFT
507E32
RECEIVE
507G36
START BIT DETECT
507G38
RIGHT JUSTIFY
TO
FROM MEMORY ACCUMULATOR LSB-1
507G37
STOP
TO
LO
FROM MEMORY BIT COUNTER Cn
BIT COUNTER CARRY OUT

7063-7

2830

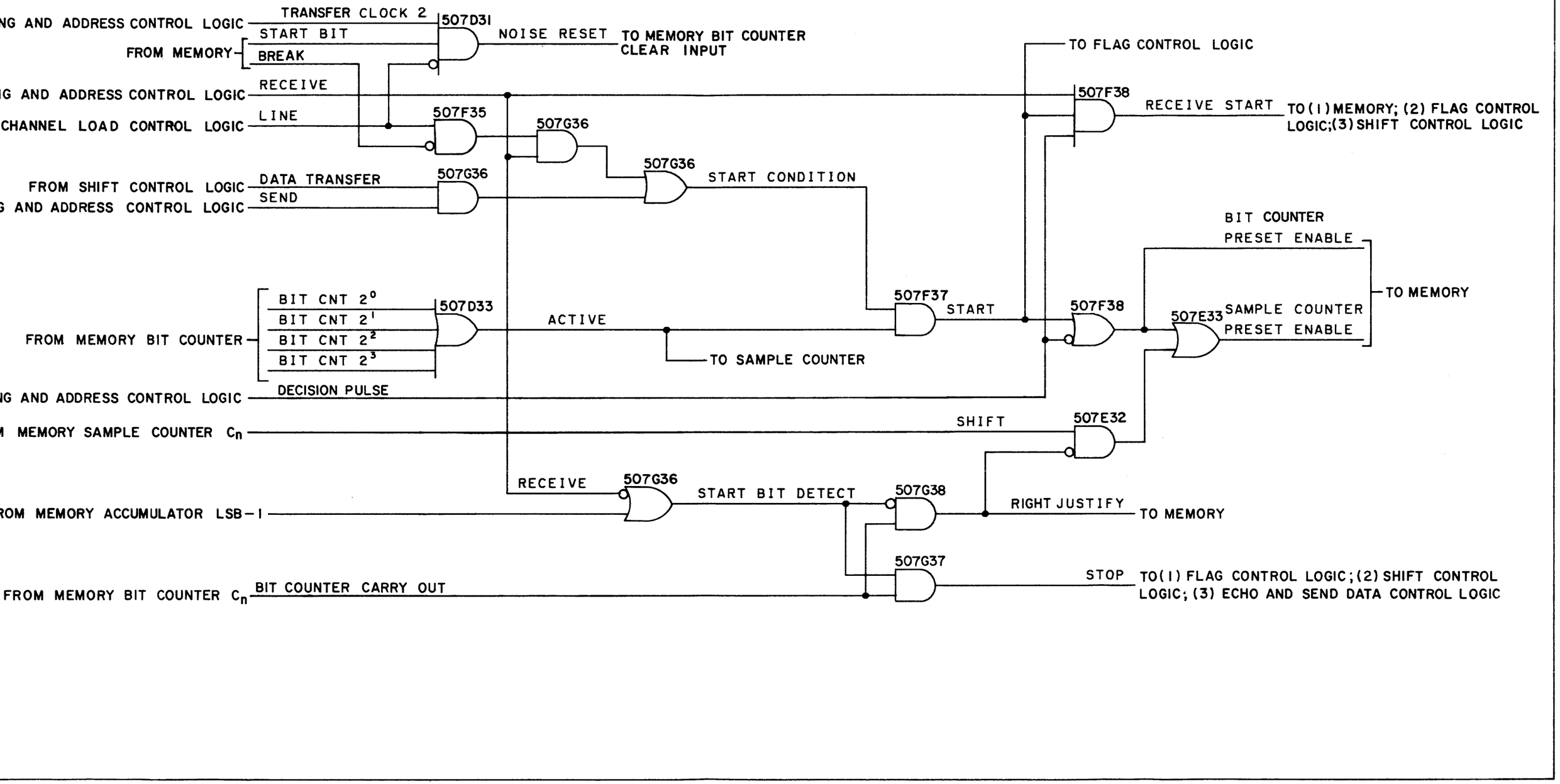
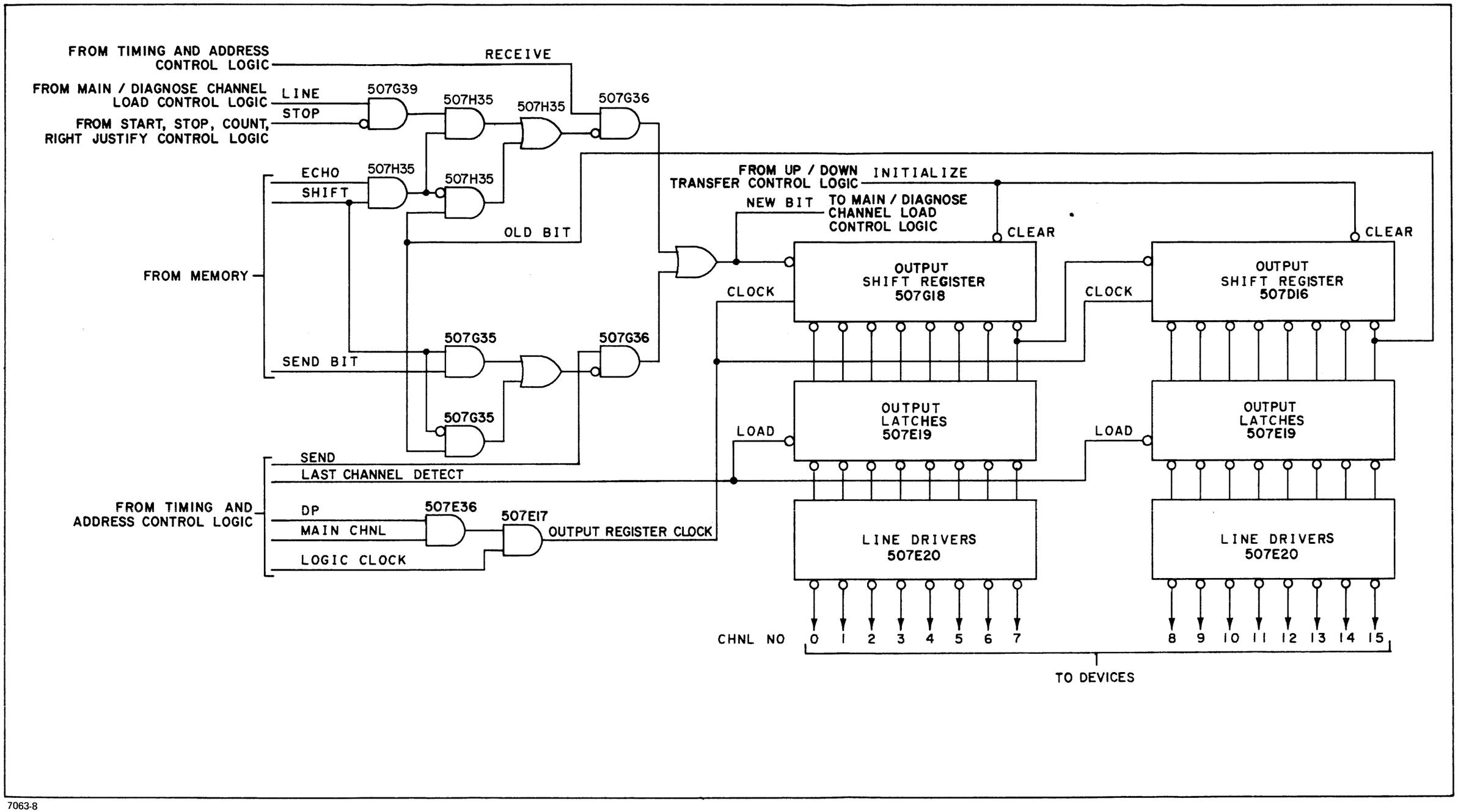


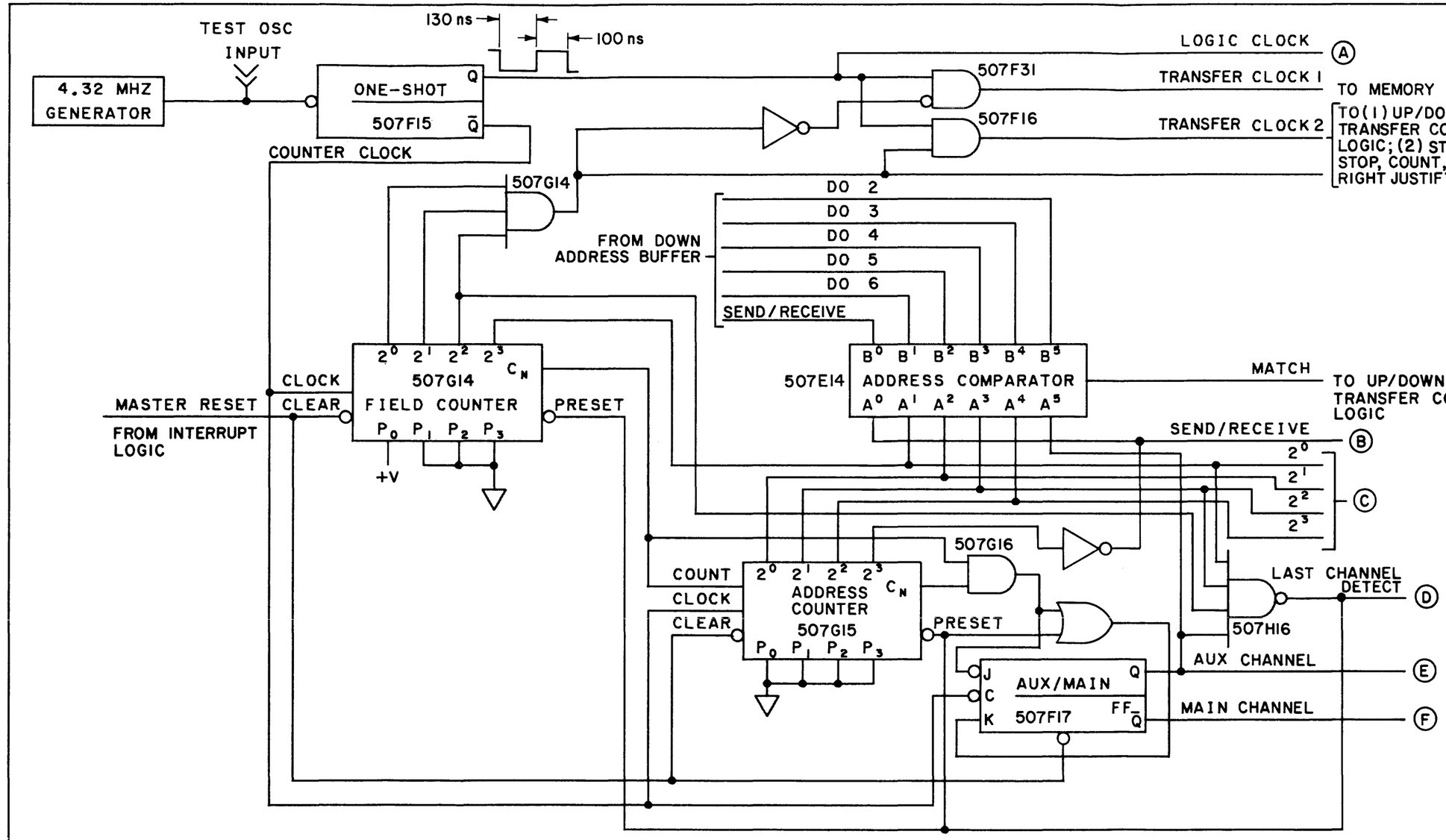
Figure 3-13. Terminal Data Interface Start, Stop, Count and Right-Justify Control Signal Generation

2831

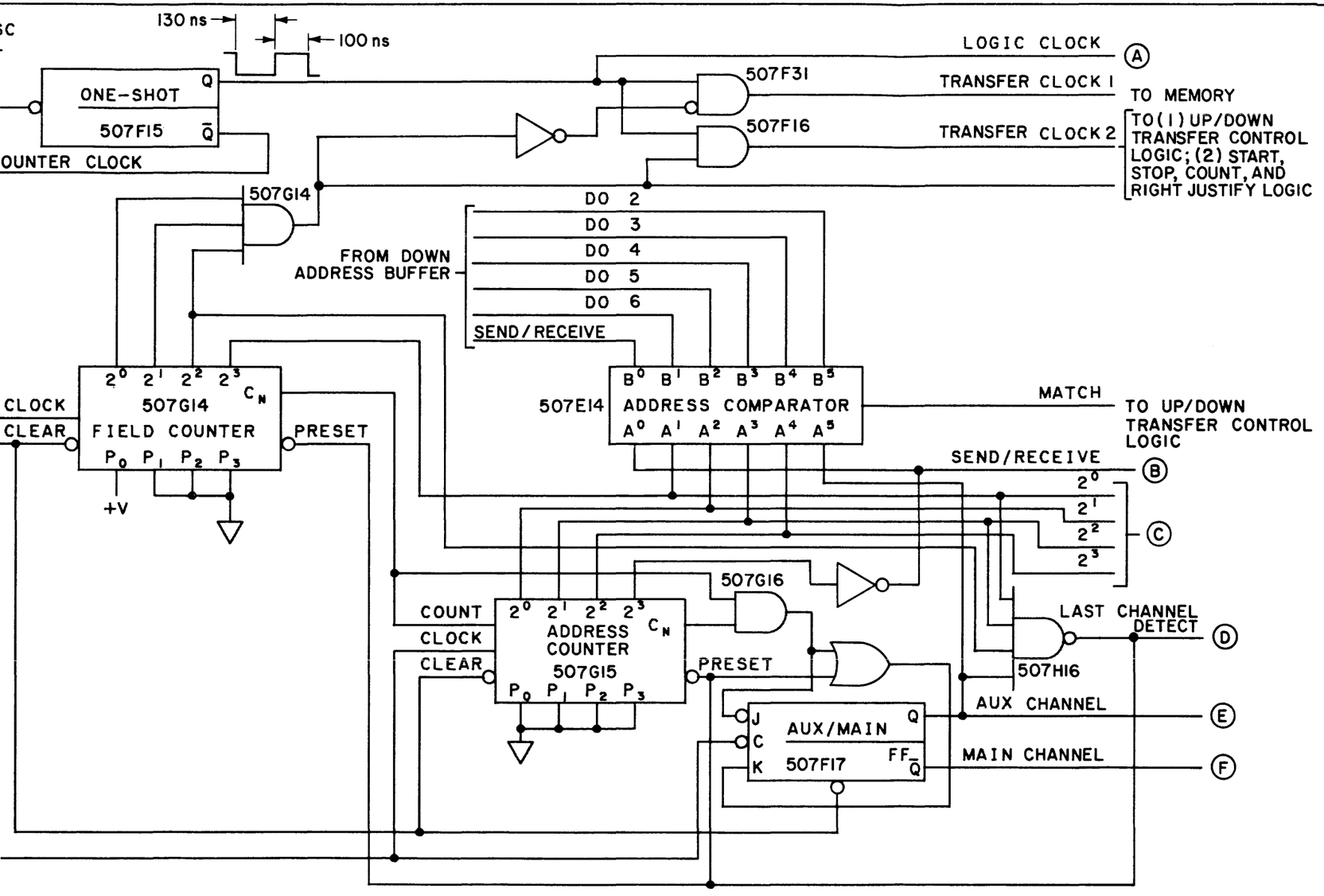


7063-8

Figure 3-14. Terminal Data Interface Echo and Send Data Output


TEST OSC INPUT
130 ns
100 ns
4.32 MHZ GENERATOR
ONE-SHOT
507F15
COUNTER CLOCK
LOGIC CLOCK
TRANSFER CLOCK 1
TO MEMORY
TRANSFER CLOCK 2
TO (1) UP/DOWN TRANSFER CONTROL LOGIC; (2) START, STOP, COUNT, AND RIGHT JUSTIFY LOGIC
507F31
507F16
507G14
FROM DOWN ADDRESS BUFFER
DO 2
DO 3
DO 4
DO 5
DO 6
SEND/RECEIVE
507G14
FIELD COUNTER
CLOCK
CLEAR
PRESET
MASTER RESET
FROM INTERRUPT LOGIC
+V
507E14
ADDRESS COMPARATOR
MATCH
TO UP/DOWN TRANSFER CONTROL LOGIC
SEND/RECEIVE
507G16
COUNT
CLOCK
CLEAR
ADDRESS COUNTER
507G15
PRESET
LAST CHANNEL DETECT
507H16
AUX CHANNEL
MAIN CHANNEL
AUX/MAIN
507F17
A
B
C
D
E
F

7063-9



(A) TO (1) UP/DOWN TRANSFER CONTROL LOGIC; (2) MAIN/DIAGNOSE CHANNEL LOAD CONTROL LOGIC; (3) SHIFT CONTROL LOGIC; (4) ECHO AND SEND DATA CONTROL LOGIC; (5) MEMORY

(B) TO (1) MAIN/DIAGNOSE CHANNEL LOAD CONTROL LOGIC; (2) START, STOP, COUNT, RIGHT JUSTIFY CONTROL LOGIC; (3) ECHO AND SEND DATA CONTROL LOGIC; (4) UP BUFFERS

(C) TO (1) MAIN/DIAGNOSE CHANNEL LOAD CONTROL LOGIC; (2) UP BUFFERS

(D)(F) TO (1) MAIN/DIAGNOSE CHANNEL LOAD CONTROL LOGIC; (2) ECHO AND SEND DATA CONTROL LOGIC

(E) TO (1) MAIN/DIAGNOSE CHANNEL LOAD CONTROL LOGIC; (2) DOWN BUFFERS; (3) UP BUFFERS

Figure 3-15. Terminal Data Interface Logic Timing and Address Control Signal Generation

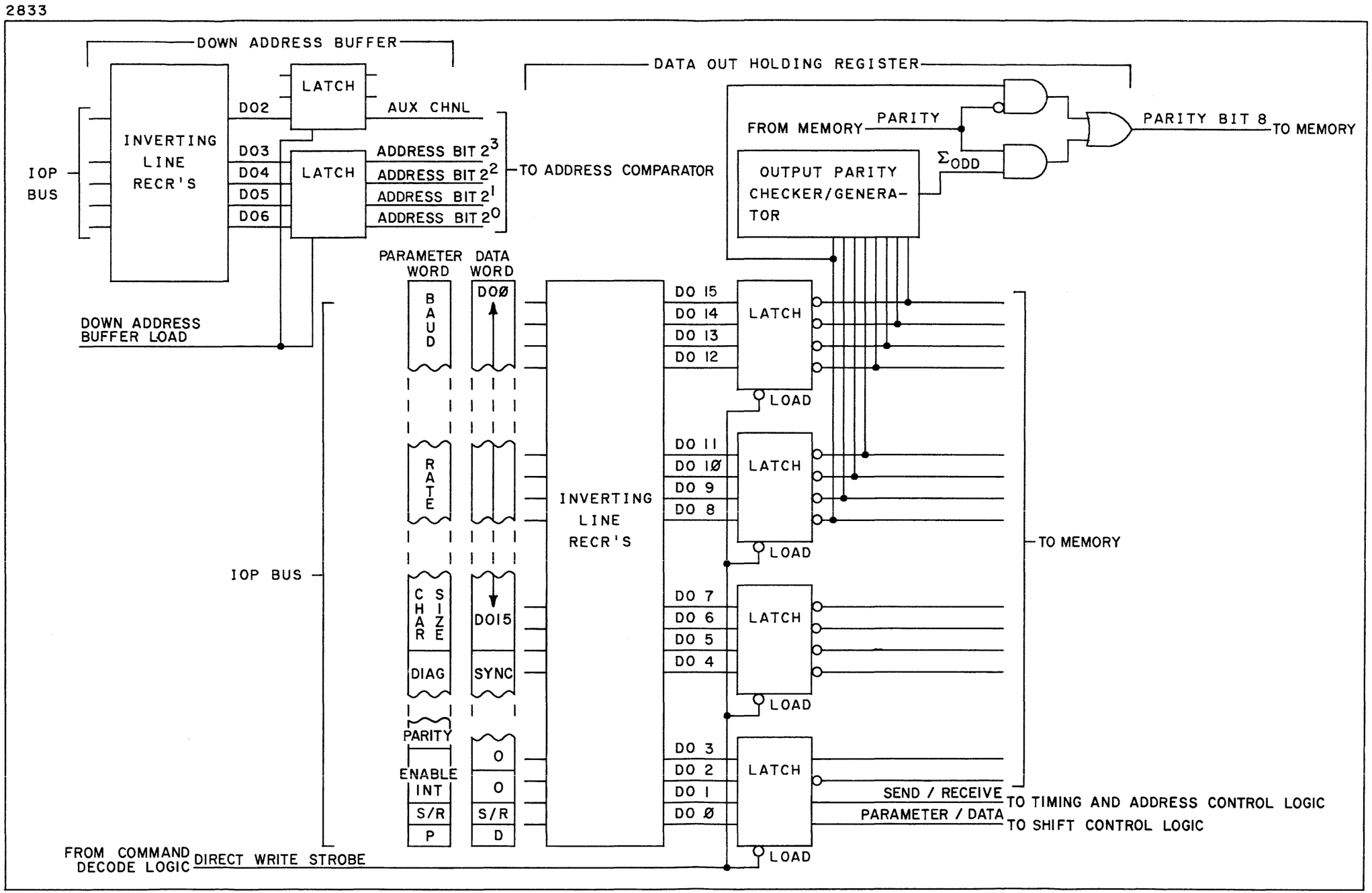
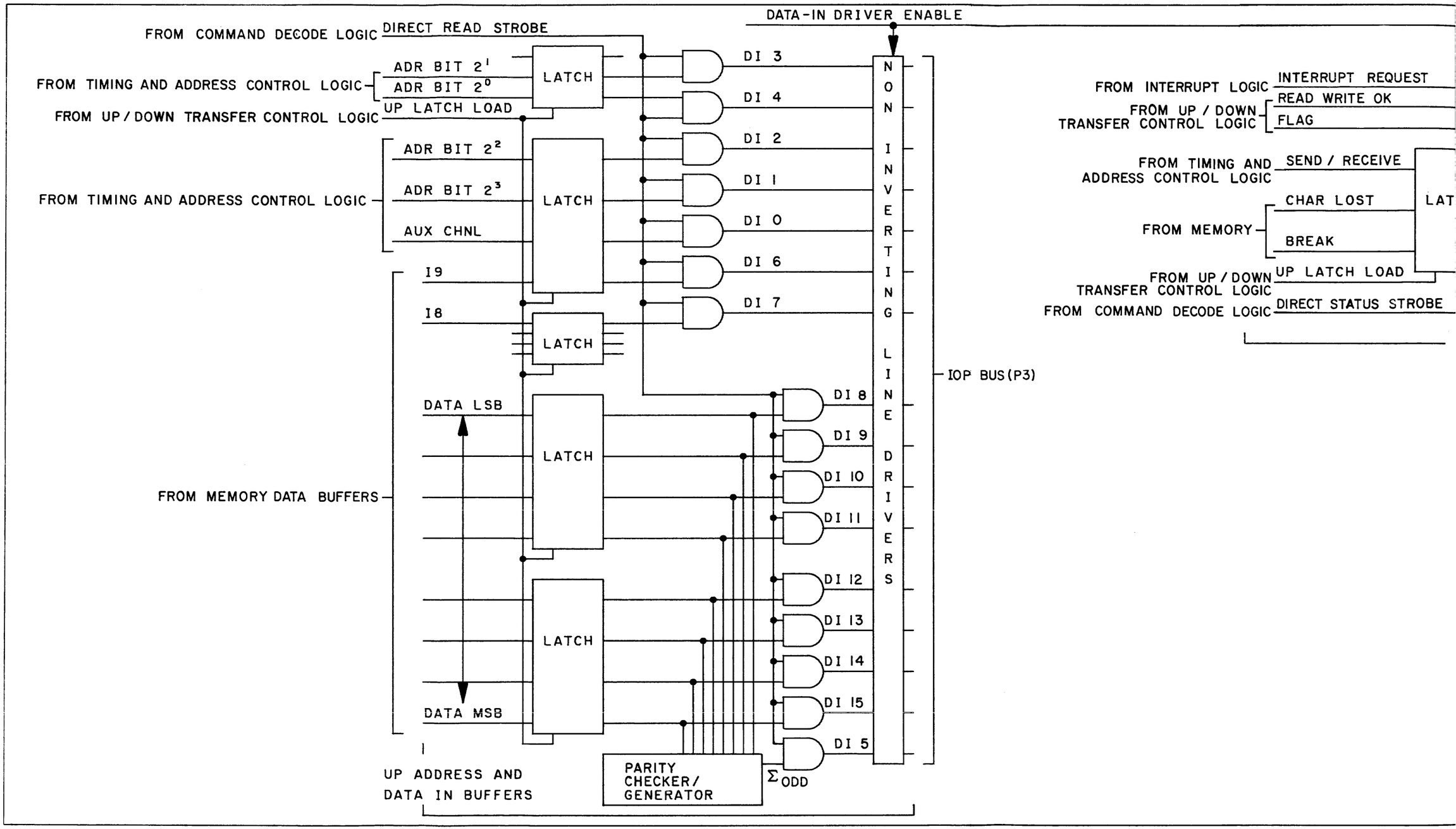


Figure 3-16. Terminal Data Interface Down Buffer Controls


DATA-IN DRIVER ENABLE
FROM COMMAND DECODE LOGIC
DIRECT READ STROBE
FROM TIMING AND ADDRESS CONTROL LOGIC
ADR BIT 2¹
ADR BIT 2⁰
FROM UP / DOWN TRANSFER CONTROL LOGIC
UP LATCH LOAD
FROM TIMING AND ADDRESS CONTROL LOGIC
ADR BIT 2²
ADR BIT 2³
AUX CHNL
I9
I8
DATA LSB
FROM MEMORY DATA BUFFERS
DATA MSB
LATCH
LATCH
LATCH
LATCH
LATCH
DI 3
DI 4
DI 2
DI 1
DI 0
DI 6
DI 7
DI 8
DI 9
DI 10
DI 11
DI 12
DI 13
DI 14
DI 15
DI 5
NONINVERTING LINE DRIVERS
IOP BUS (P3)
UP ADDRESS AND DATA IN BUFFERS
PARITY CHECKER/ GENERATOR
Σ ODD
FROM INTERRUPT LOGIC
INTERRUPT REQUEST
FROM UP / DOWN TRANSFER CONTROL LOGIC
READ WRITE OK
FLAG
FROM TIMING AND ADDRESS CONTROL LOGIC
SEND / RECEIVE
FROM MEMORY
CHAR LOST
BREAK
FROM UP / DOWN TRANSFER CONTROL LOGIC
UP LATCH LOAD
FROM COMMAND DECODE LOGIC
DIRECT STATUS STROBE
LAT

2249-54

2834

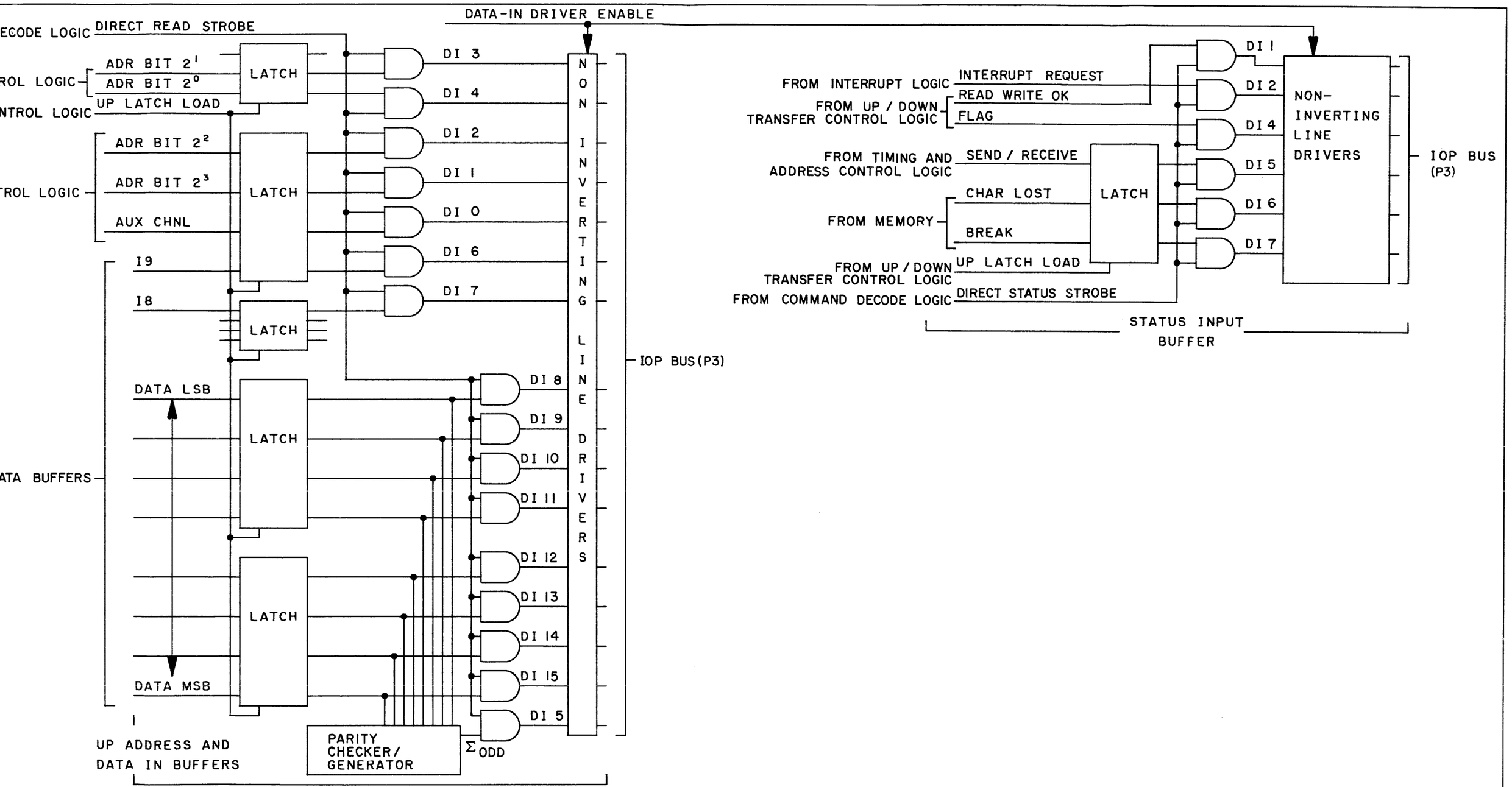
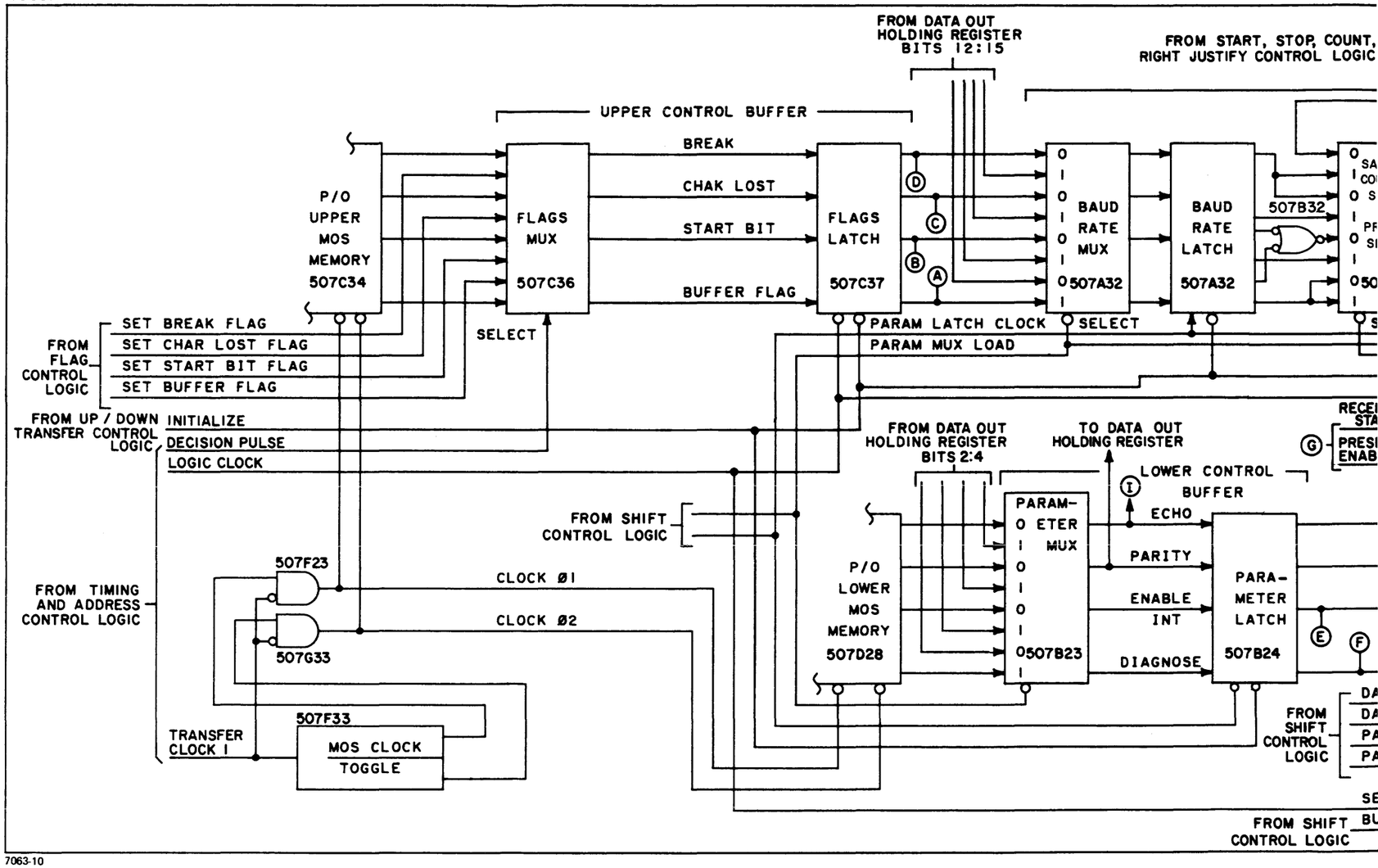
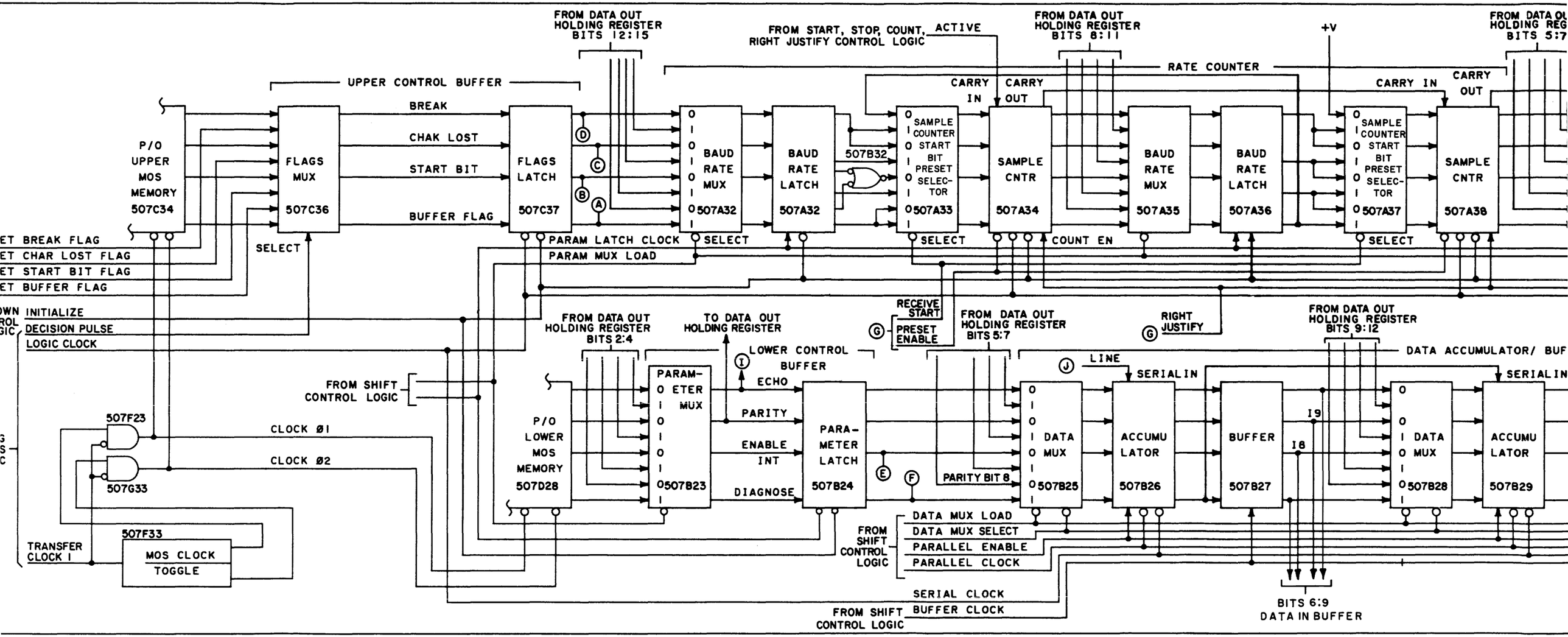


Figure 3-17. Terminal Data Interface Up Buffer Controls

2835A



7063-10


FROM DATA OUT HOLDING REGISTER BITS 12:15
FROM START, STOP, COUNT, ACTIVE RIGHT JUSTIFY CONTROL LOGIC
FROM DATA OUT HOLDING REGISTER BITS 8:11
+V
FROM DATA OUT HOLDING REG BITS 5:7
UPPER CONTROL BUFFER
RATE COUNTER
CARRY IN
CARRY OUT
CARRY IN
CARRY OUT
BREAK
CHAK LOST
START BIT
BUFFER FLAG
P/O UPPER MOS MEMORY 507C34
FLAGS MUX 507C36
FLAGS LATCH 507C37
BAUD RATE MUX 507A32
BAUD RATE LATCH 507A32
507B32
SAMPLE COUNTER START BIT PRESET SELECTOR 507A33
SAMPLE CNTR 507A34
BAUD RATE MUX 507A35
BAUD RATE LATCH 507A36
SAMPLE COUNTER START BIT PRESET SELECTOR 507A37
SAMPLE CNTR 507A38
SELECT
PARAM LATCH CLOCK
SELECT
SELECT
COUNT EN
SELECT
PARAM MUX LOAD
ET BREAK FLAG
ET CHAR LOST FLAG
ET START BIT FLAG
ET BUFFER FLAG
WN INITIALIZE
ROL DECISION PULSE
GIC LOGIC CLOCK
RECEIVE START
PRESET ENABLE
FROM DATA OUT HOLDING REGISTER BITS 2:4
TO DATA OUT HOLDING REGISTER
LOWER CONTROL BUFFER
FROM DATA OUT HOLDING REGISTER BITS 5:7
RIGHT JUSTIFY
FROM DATA OUT HOLDING REGISTER BITS 9:12
DATA ACCUMULATOR/ BUF
LINE
SERIAL IN
SERIAL IN
FROM SHIFT CONTROL LOGIC
PARAM-ETER MUX 507B23
ECHO
PARITY
ENABLE INT
DIAGNOSE
PARA-METER LATCH 507B24
P/O LOWER MOS MEMORY 507D28
PARITY BIT 8
DATA MUX 507B25
ACCUMU LATOR 507B26
BUFFER 507B27
I9
I8
DATA MUX 507B28
ACCUMU LATOR 507B29
507F23
507G33
CLOCK Ø1
CLOCK Ø2
507F33
TRANSFER CLOCK I
MOS CLOCK TOGGLE
DATA MUX LOAD
DATA MUX SELECT
PARALLEL ENABLE
PARALLEL CLOCK
FROM SHIFT CONTROL LOGIC
SERIAL CLOCK
BUFFER CLOCK
FROM SHIFT CONTROL LOGIC
BITS 6:9
DATA IN BUFFER

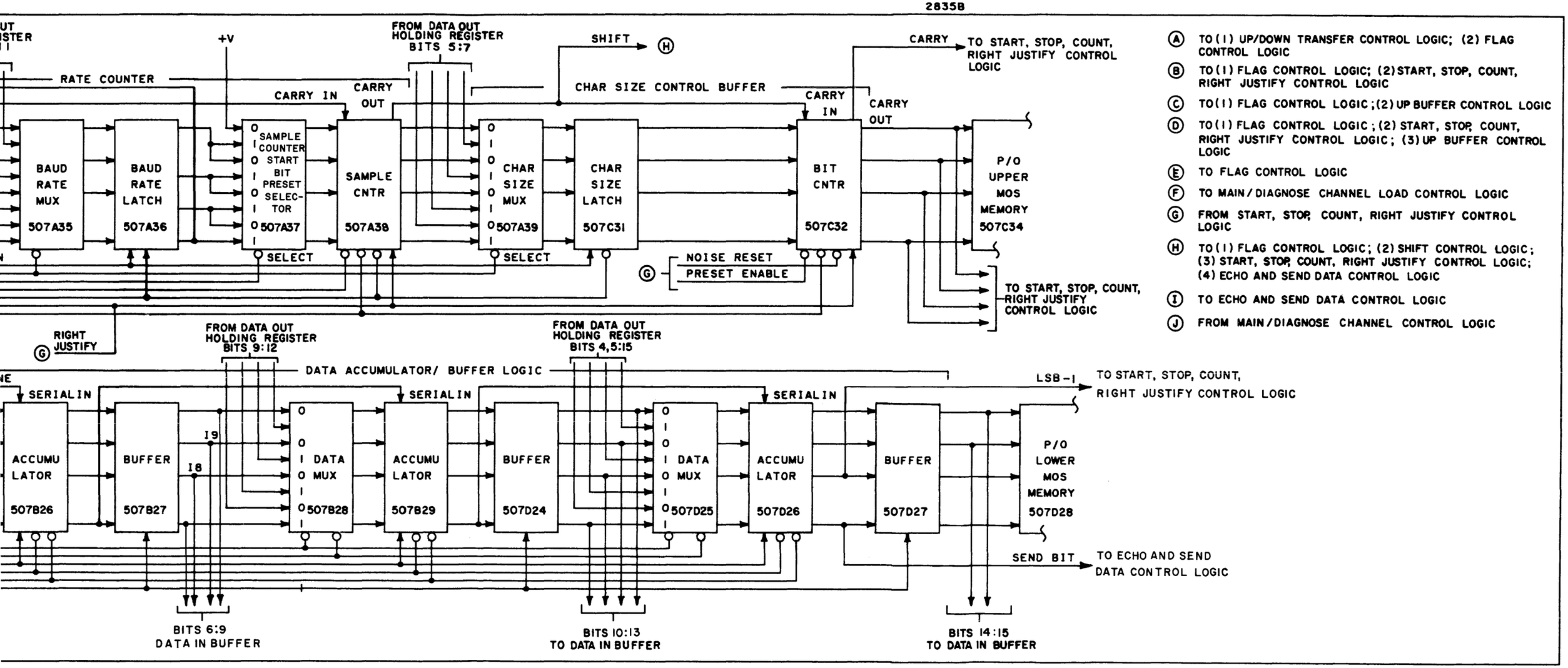
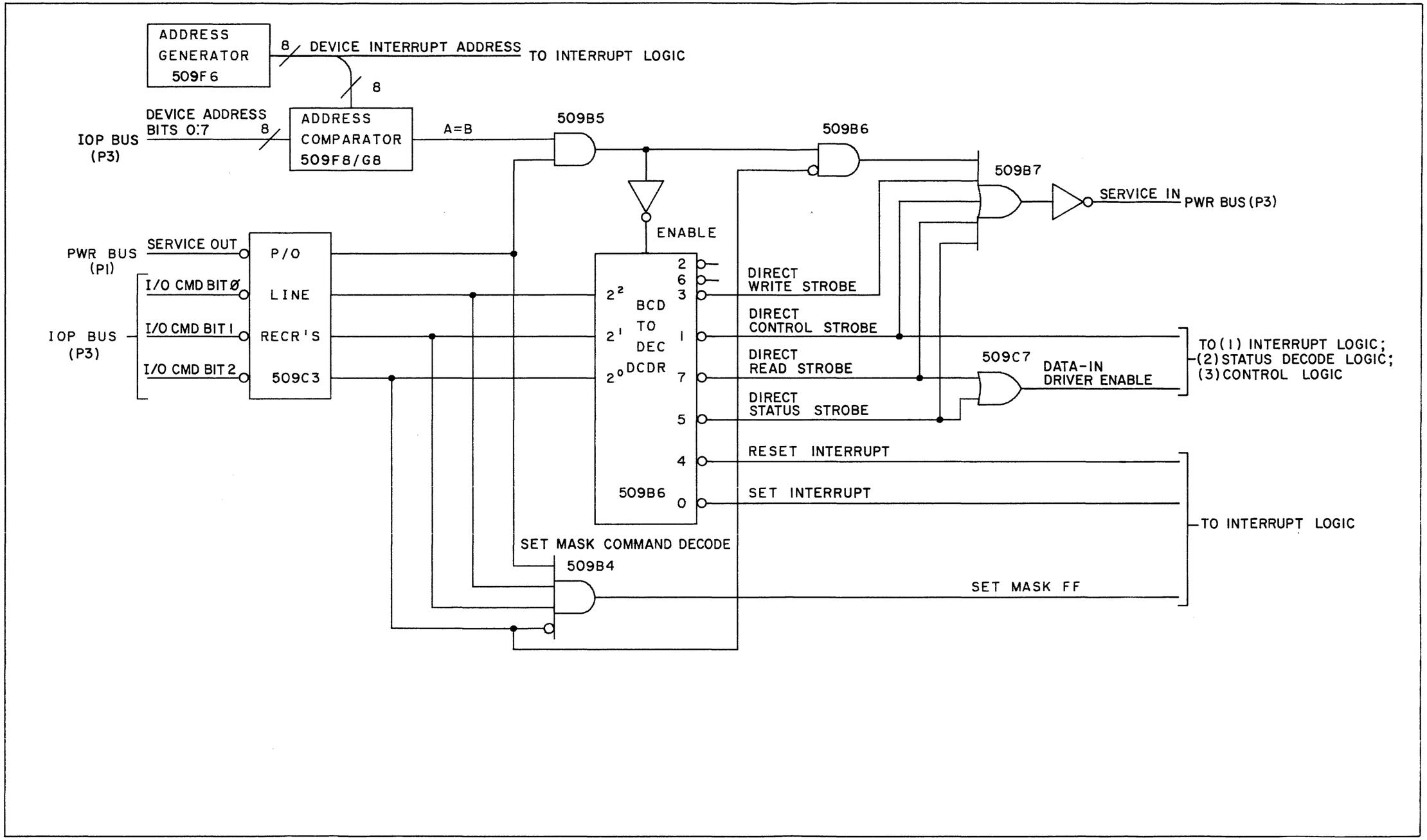


Figure 3-18. Recirculating Memory

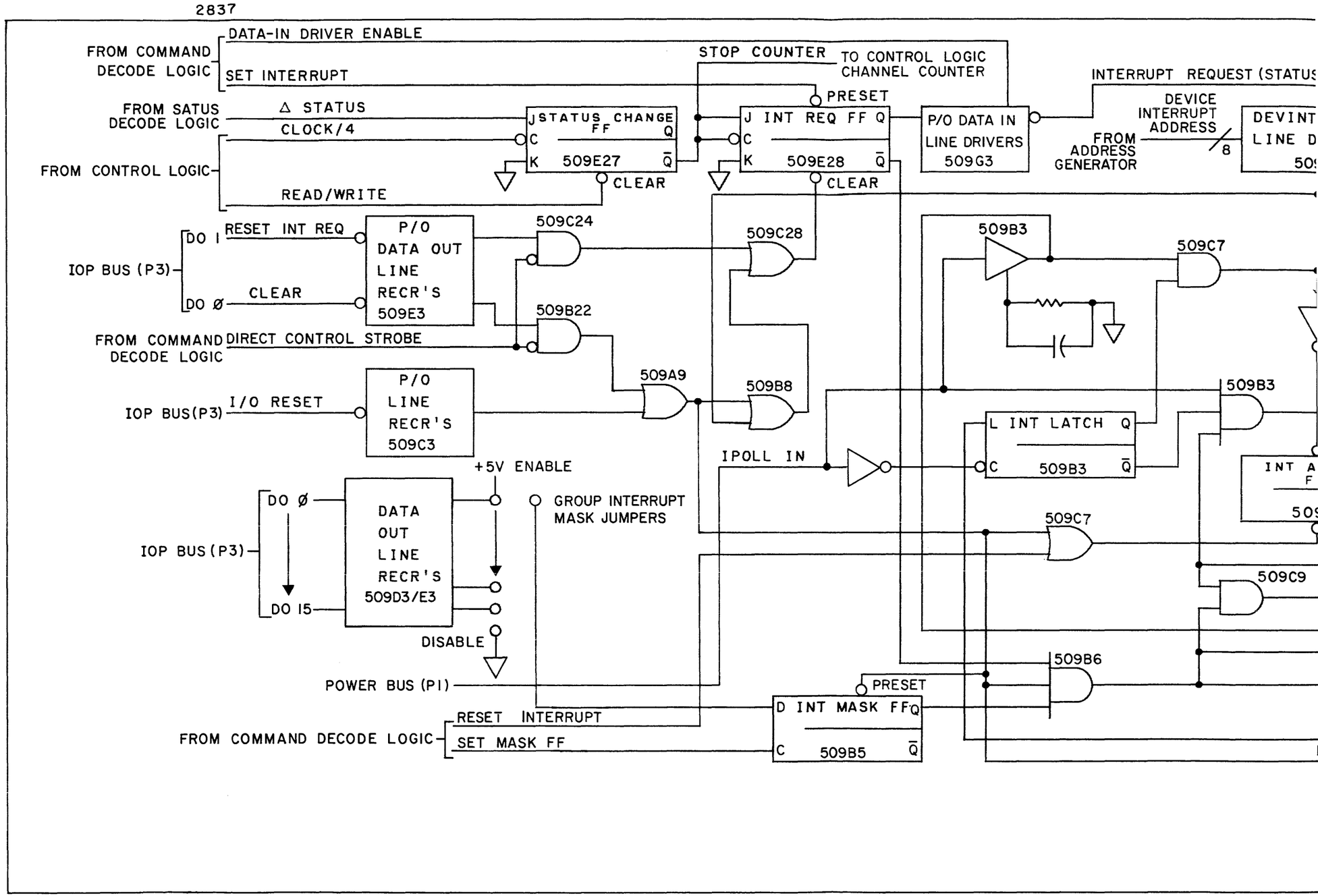
2836



2249-56

Figure 3-19. Terminal Control Interface Command Decoding

2837


DATA-IN DRIVER ENABLE
FROM COMMAND DECODE LOGIC
SET INTERRUPT
STOP COUNTER
TO CONTROL LOGIC CHANNEL COUNTER
INTERRUPT REQUEST (STATUS
PRESET
FROM SATUS DECODE LOGIC
Δ STATUS
CLOCK/4
J STATUS CHANGE FF Q
C
K 509E27 Q̄
CLEAR
J INT REQ FF Q
C
K 509E28 Q̄
CLEAR
P/O DATA IN LINE DRIVERS 509G3
DEVICE INTERRUPT ADDRESS
FROM ADDRESS GENERATOR
8
DEVINT LINE D
509
FROM CONTROL LOGIC
READ/WRITE
IOP BUS (P3)
DO 1
RESET INT REQ
DO Ø
CLEAR
P/O DATA OUT LINE RECR'S 509E3
509C24
509C28
509B3
509C7
509B22
FROM COMMAND DECODE LOGIC
DIRECT CONTROL STROBE
509A9
509B8
P/O LINE RECR'S 509C3
IOP BUS(P3)
I/O RESET
509B3
L INT LATCH Q
C 509B3 Q̄
IPOLL IN
INT A
F
+5V ENABLE
DO Ø
DATA OUT LINE RECR'S 509D3/E3
IOP BUS (P3)
DO 15
GROUP INTERRUPT MASK JUMPERS
509C7
509C9
DISABLE
509B6
POWER BUS (P1)
PRESET
D INT MASK FF Q
RESET INTERRUPT
FROM COMMAND DECODE LOGIC
SET MASK FF
C 509B5 Q̄

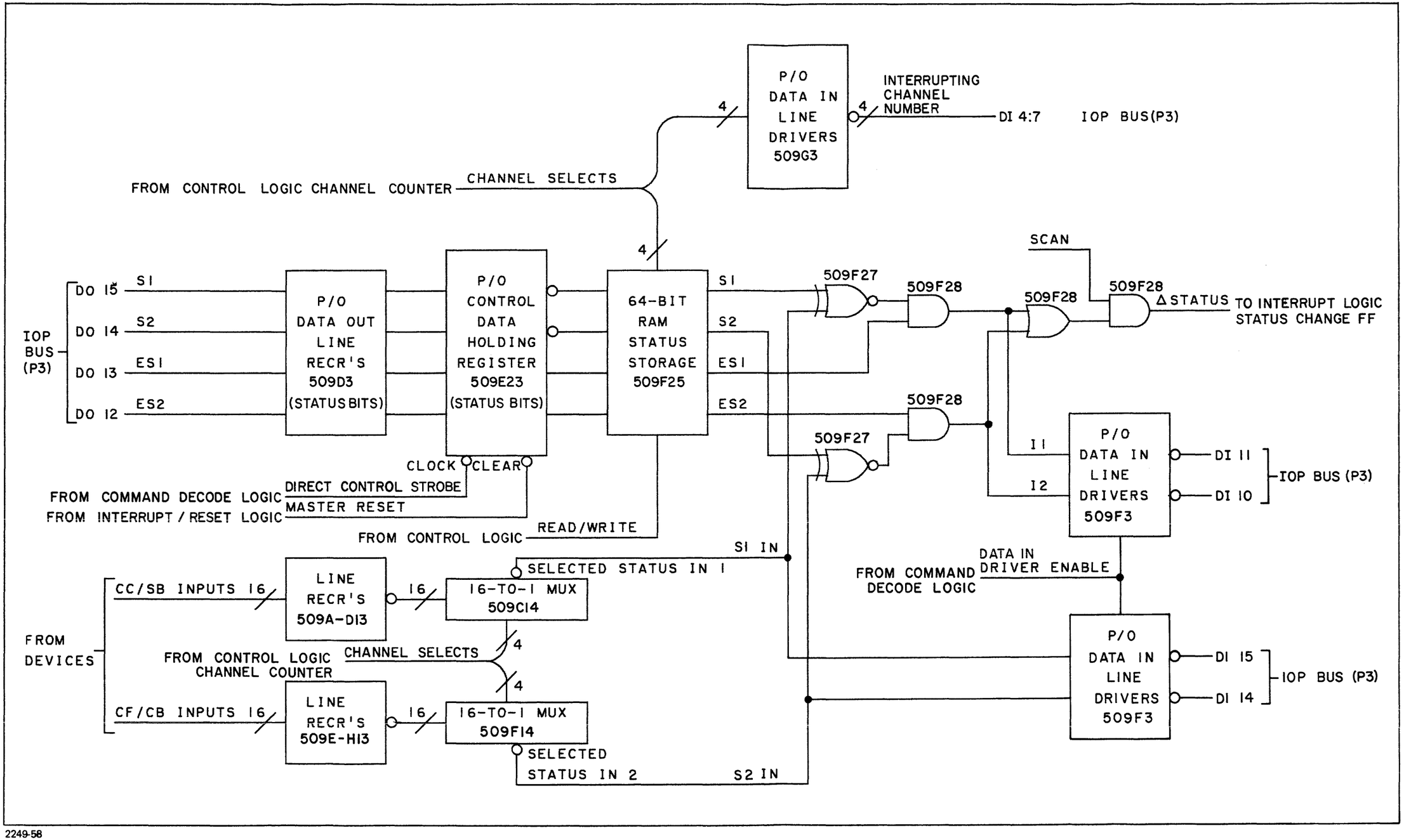
2249-57

2837

DATA-IN DRIVER ENABLE
FROM COMMAND DECODE LOGIC
SET INTERRUPT
STOP COUNTER
TO CONTROL LOGIC CHANNEL COUNTER
PRESET
INTERRUPT REQUEST (STATUS BIT)
DI 2
FROM SATUS DECODE LOGIC
Δ STATUS
CLOCK/4
JSTATUS CHANGE FF Q
C
K 509E27 Q̄
CLEAR
J INT REQ FF Q
C
K 509E28 Q̄
CLEAR
P/O DATA IN LINE DRIVERS 509G3
DEVICE INTERRUPT ADDRESS
FROM ADDRESS GENERATOR
8
DEVINTAD LINE DRIVERS 509D8
8
DEVICE INT ADDRESS BITS 0:7
IOP BUS (P3)
M CONTROL LOGIC
READ/WRITE
ENABLE
DO 1
RESET INT REQ
P/O DATA OUT LINE RECR'S 509E3
509C24
509C28
509B3
509C7
IOP BUS (P3)
DO Ø
CLEAR
509B22
FROM COMMAND DECODE LOGIC
DIRECT CONTROL STROBE
509A9
509B8
P/O LINE RECR'S 509C3
IOP BUS(P3)
I/O RESET
509B3
IPOLL OUT
POWER BUS (P1)
L INT LATCH Q
C 509B3 Q̄
SET
INT ACTIVE Q FF
509C8 Q̄
CLEAR
IPOLL IN
+5V ENABLE
DO Ø
GROUP INTERRUPT MASK JUMPERS
509C7
509C9
DATA OUT LINE RECR'S 509D3/E3
IOP BUS (P3)
DO 15
509C9
INTERRUPT ACKNOWLEDGE
DISABLE
509B6
IOP BUS (P3)
POWER BUS (P1)
PRESET
INTERRUPT REQUEST
D INT MASK FF Q
RESET INTERRUPT
FROM COMMAND DECODE LOGIC
SET MASK FF
C 509B5 Q̄
MASTER RESET
TO (1) STATUS DECODE LOGIC
(2) CONTROL LOGIC

Figure 3-20. Terminal Control Interface Interrupt Polling, Processing, and Acknowledge

2838



2249-58

Figure 3-21. Terminal Control Interface Status Decoding, Scanning, and Updating

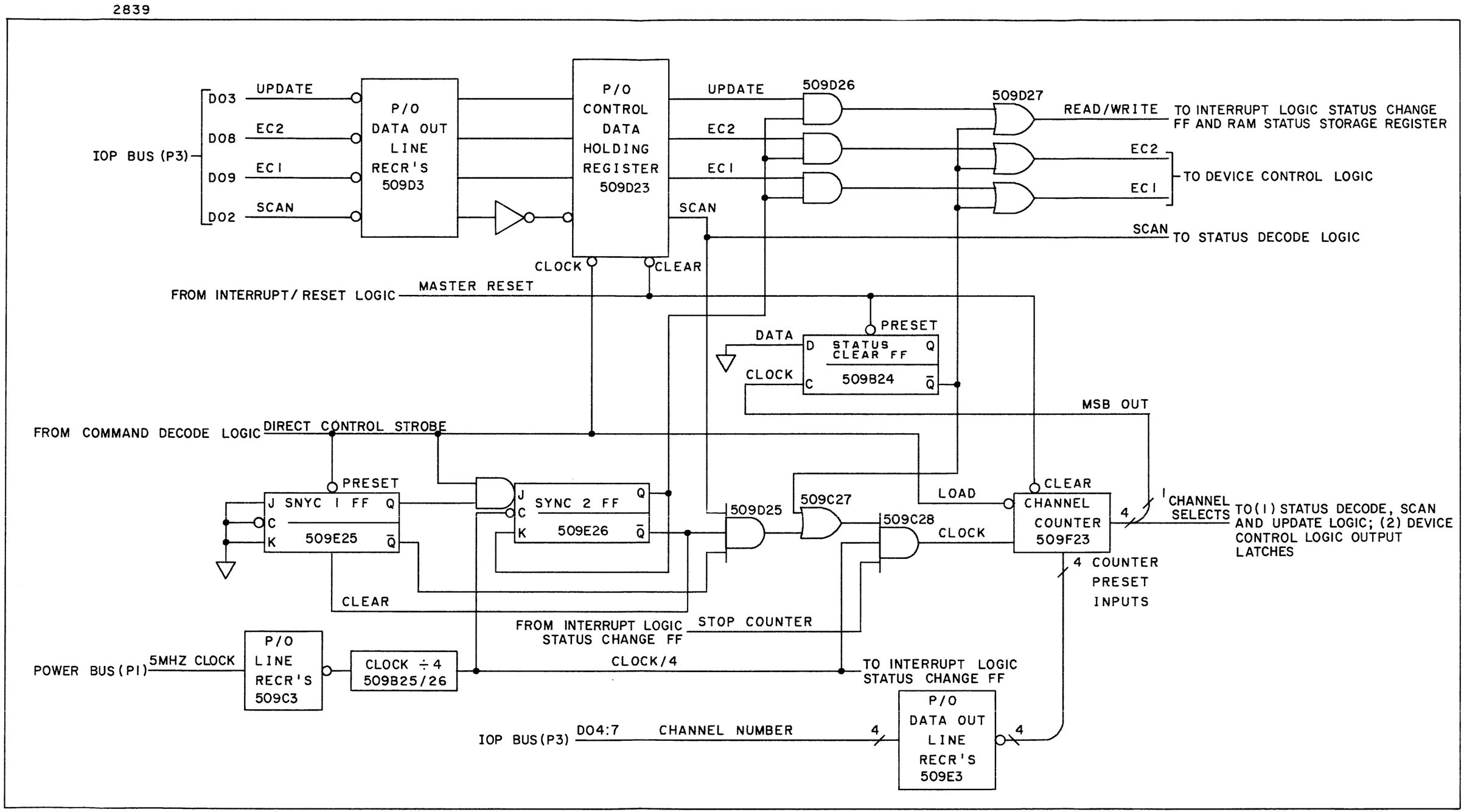


Figure 3-22. Terminal Control Interface Control Signal Generation

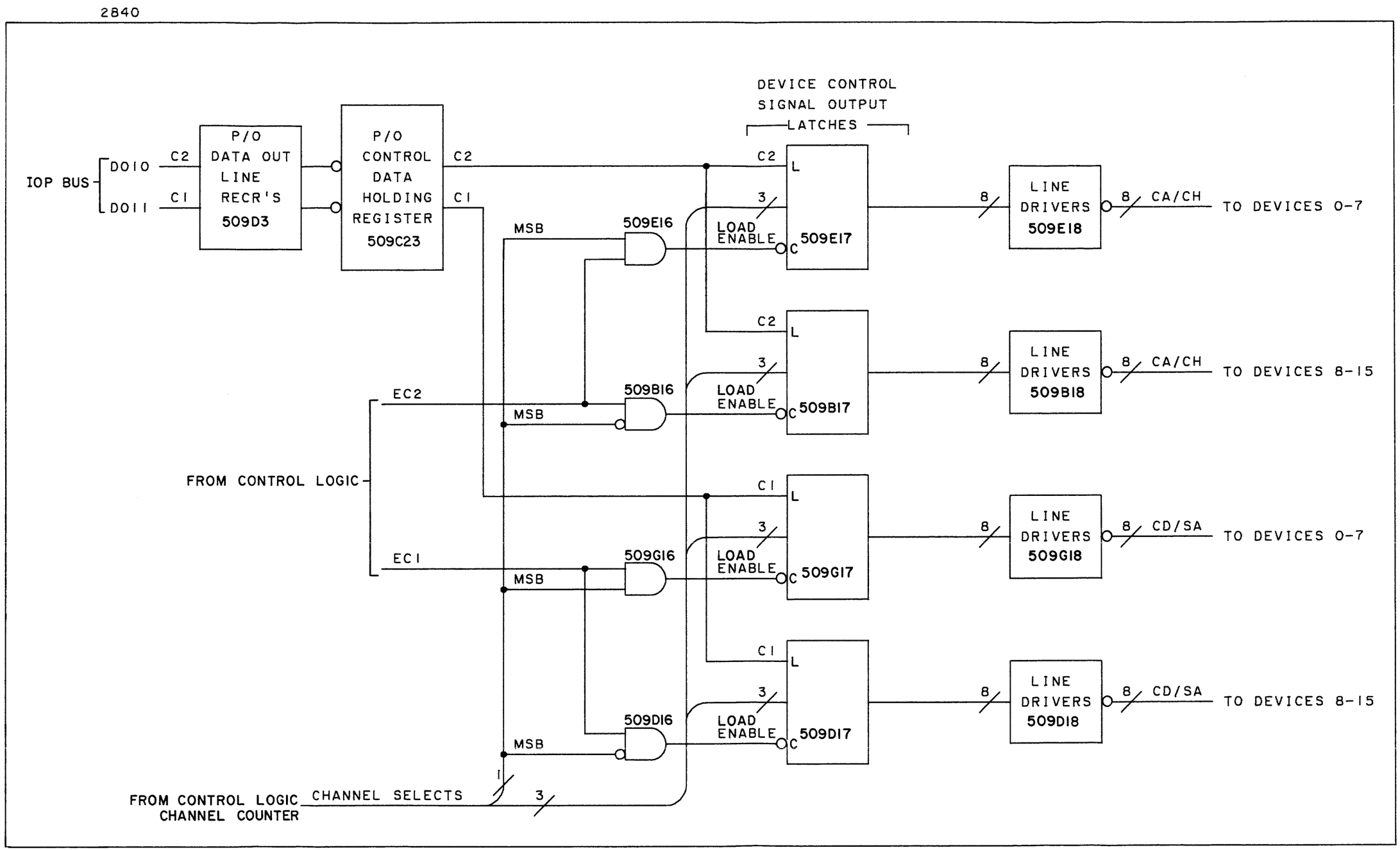


Figure 3-23. Terminal Control Interface Device Control Signal Generation

4-1. INTRODUCTION.

4-2. This section contains general servicing information for the HP 30032B Asynchronous Terminal Controller including signal index information. Detailed logic diagrams and parts location diagrams for the terminal data interface PCA and terminal control interface PCA are provided in set numbers 507 and 509 respectively of the *HP 3000 Computer System Detailed Diagrams Manual.* The diagrams manual also provides integrated circuit pack diagrams and descriptions for all integrated circuits used with the asynchronous terminal controller. A list of all component part numbers and component ordering information is provided in the *HP 3000 Computer System Illustrated Parts Breakdown Manual.*

4-3. GENERAL SERVICING INFORMATION.

4-4. General servicing information consists of information that is commonly referenced in this section or useful during servicing of the subsystem.

4-5. SAFETY PRECAUTIONS.

4-6. Dangerous voltages are present in the computer system cabinet. Observe all **WARNING** labels while servicing the equipment: failure to do so could result in injury or death.

CAUTION

Failure to observe the safety precautions can result in damage to components on the asynchronous terminal controller PCAs or to other components in the computer system.

4-7. When printed circuit assemblies are being removed, replaced, placed on PCA extenders, or connected to or disconnected from the connector panel, the computer system DC POWER switch must be placed in the STANDBY position to remove power from the PCA connectors.

4-8. REQUIRED SERVICING EQUIPMENT.

4-9. Equipment (PCA extenders, cables, etc.) required for servicing the asynchronous terminal controller subsystem is provided with the HP 30001A CPU/IOP Module, or is referenced in the manuals for the applicable peripheral devices or datasets.

4-10. MAINTENANCE DATA.

4-11. Maintenance data provided in this section consists of the following:

a. Macro-Level Send and Receive Operations, figure 4-1.

b. Intermediate-Level Receive Operation, figure 4-2.

c. Intermediate-Level Send Operation, figure 4-3.

d. Asynchronous Terminal Controller Interconnection Diagram, figure 4-4.

e. PCA-to-Connector Panel Interconnection Diagram, figure 4-5.

f. Terminal Control Interface PCA Connector Diagram, figure 4-6.

g. Terminal Data Interface PCA Connector Diagram, figure 4-7.

h. Terminal Control Interface PCA Signal Index, table 4-1.

i. Terminal Data Interface PCA Signal Index, table 4-2.

j. Extender Cable Signal Index, table 4-3.

k. Data Set Cable Signal Index, table 4-4.

l. Baud Rate/Bit Duration Reference, table 4-5.

m. TDI Major Clock and Control Signal Timing Relationships, figure 4-8.

n. TDI Clock, Decision Pulse, and Address Generation Timing Diagram, figure 4-9.

o. TDI Channel Configuration Timing Diagram, figure 4-10.

p. TDI Parameter Loading Events Flowchart, figure 4-11.

q. TDI Read and Status Fetch Events Flowchart, figure 4-12.

r. TDI CIO Command Events Flowchart, figure 4-13.

s. TDI Typical Send Operation Timing Diagram, figure 4-14.

t. TDI Send Events Flowchart, figure 4-15.

u. TDI Typical Receive Operation Timing Diagram, figure 4-16.

v. TDI Receive Events Flowchart, figure 4-17.

w. TCI Operational Flowchart, figure 4-18.

x. TDI and TCI Jumper Locations, figure 4-19.

4-12. PREVENTIVE MAINTENANCE.

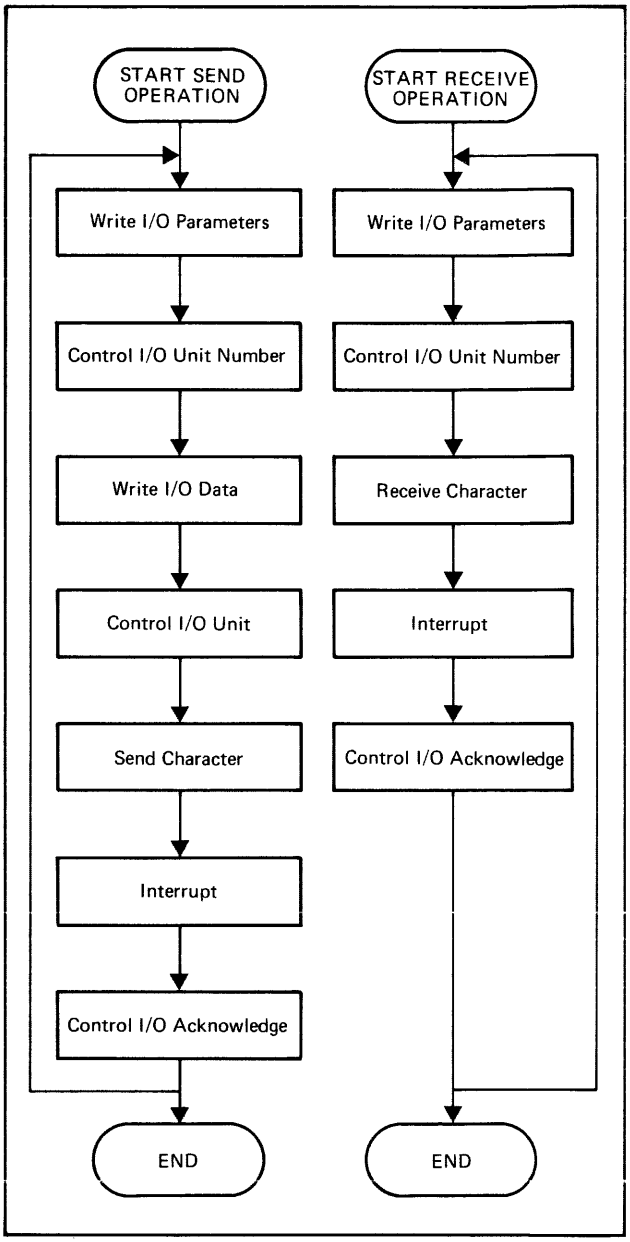
4-13. Normal preventive maintenance for the asynchronous terminal controller subsystem consists of periodically inspecting the subsystem components for damaged (burned or broken) components and insulation. This should be incorporated with the scheduled preventive maintenance for the computer system.

4-14. Performing the applicable diagnostic operating procedures will verify proper operation of the functions of the asynchronous terminal controller subsystem. Also refer to preventive maintenance data in applicable peripheral device or dataset equipment manuals.

4-15. TROUBLESHOOTING.

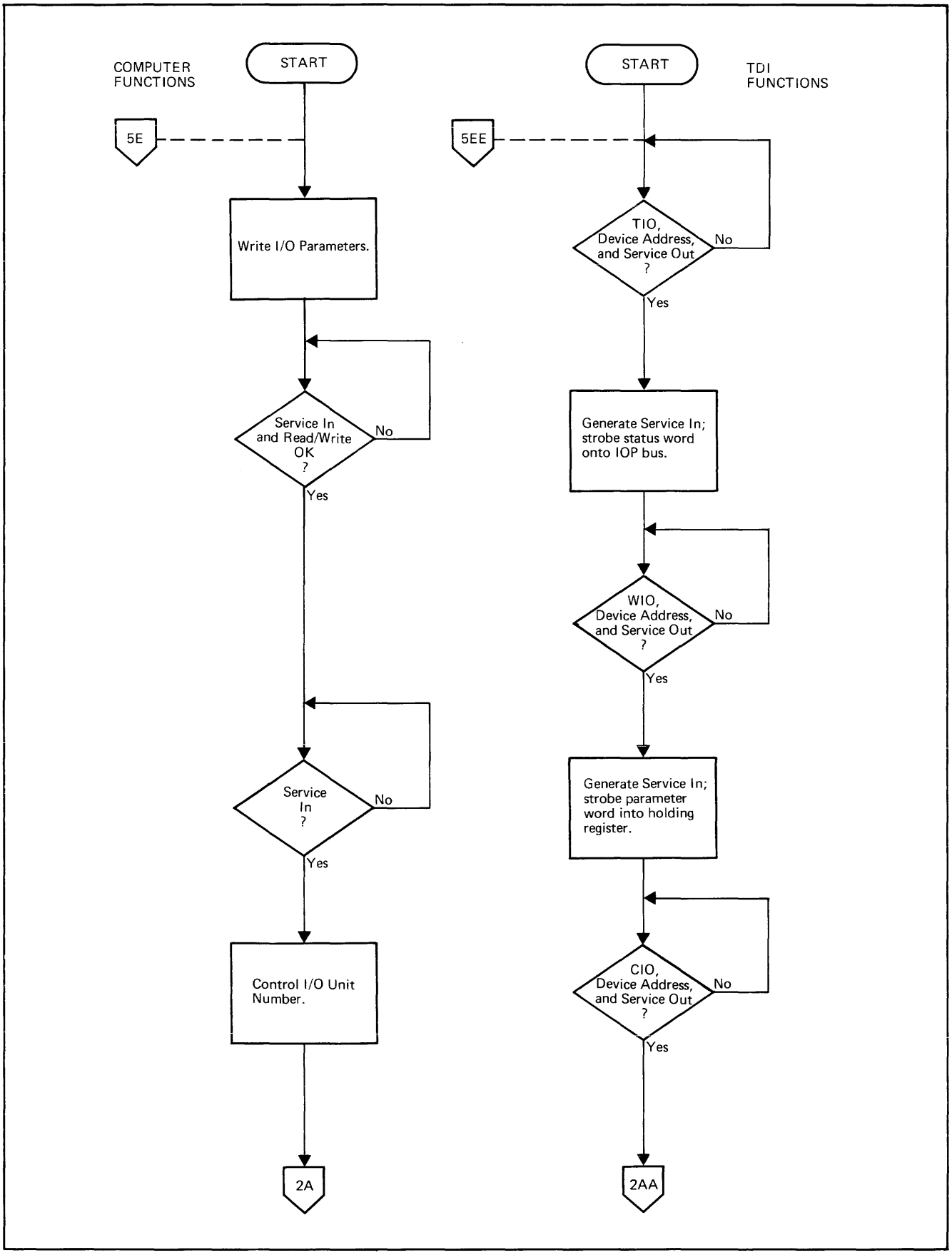
4-16. Troubleshooting the asynchronous terminal controller subsystem is accomplished by performing the diagnostic program procedures applicable to the subsystem and analyzing the error halts as they occur. Use the maintenance data contained in this section and the detailed logic diagrams to isolate the malfunction to a replaceable component.

4-17. Also note figure 4-1 that presents parameter loading and send and receive operations on a macro-level at the computer. Figures 4-2 and 4-3 present intermediate-level operations. Note that the computer macro-level is shown in time sequence to TDI functions. Figures 4-8 through 4-18 present detailed operational flow and timing.



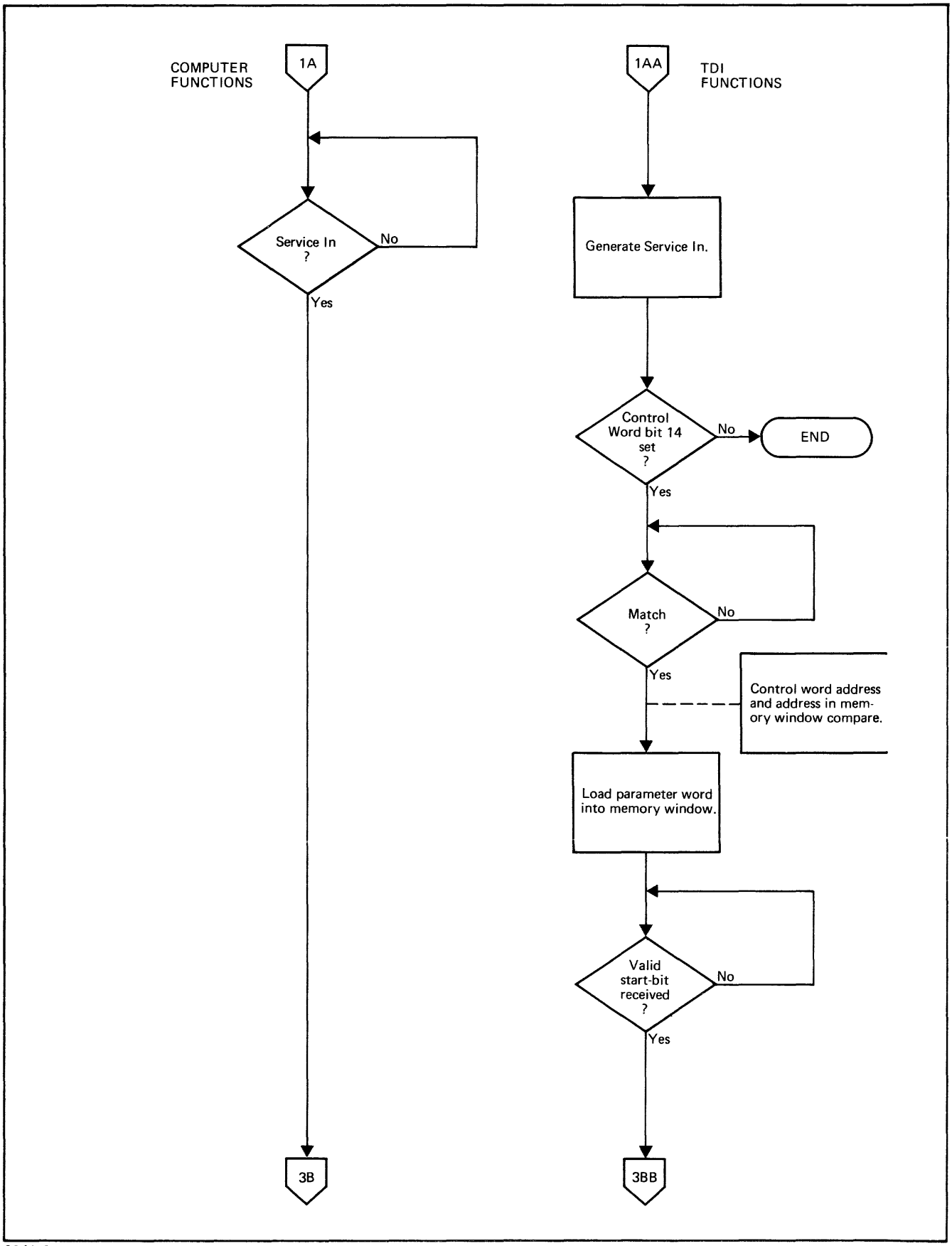
2249-66

Figure 4-1. Macro-Level Send and Receive Operations



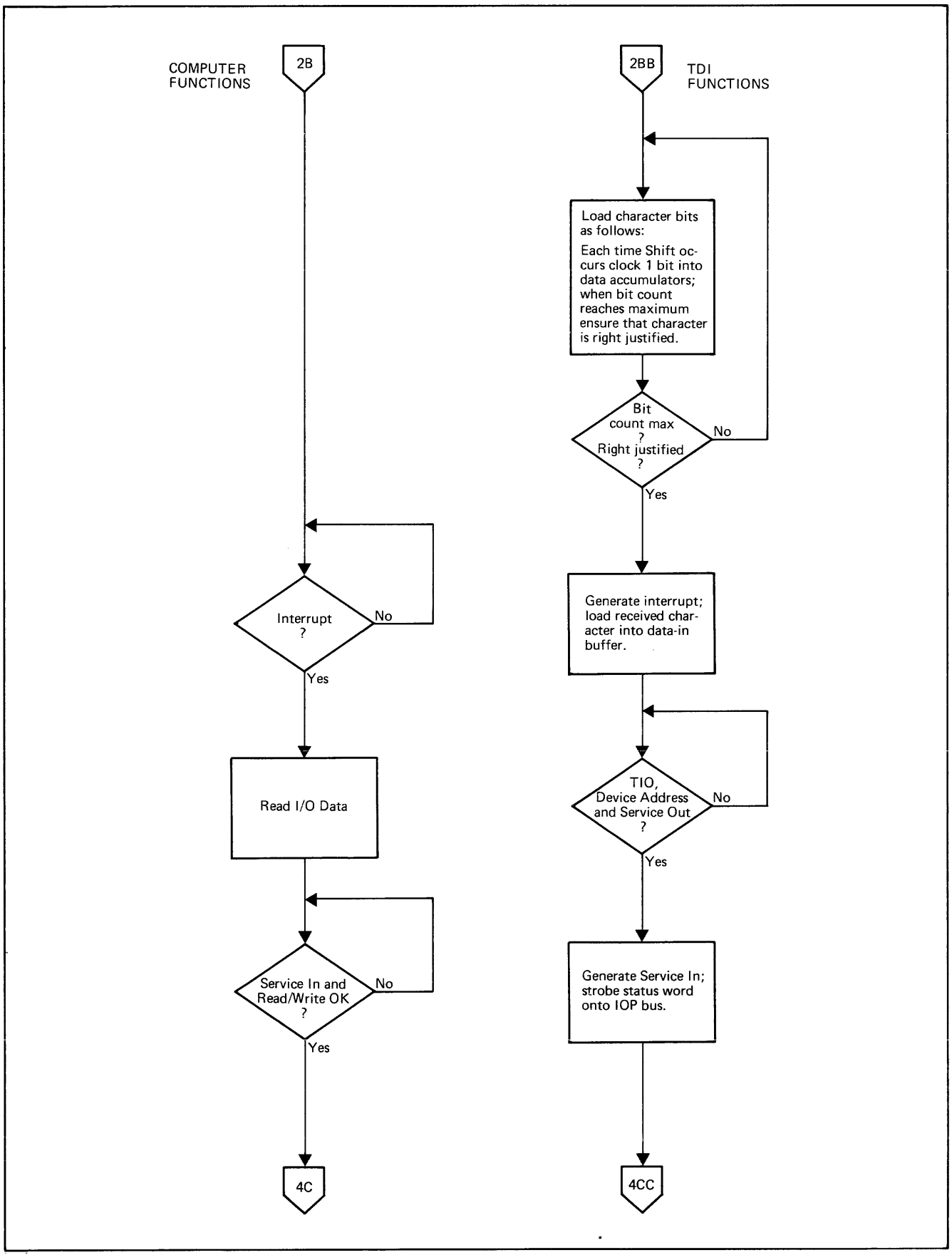
2249-61

Figure 4-2. Intermediate-Level Receive Operation (Sheet 1 of 5)



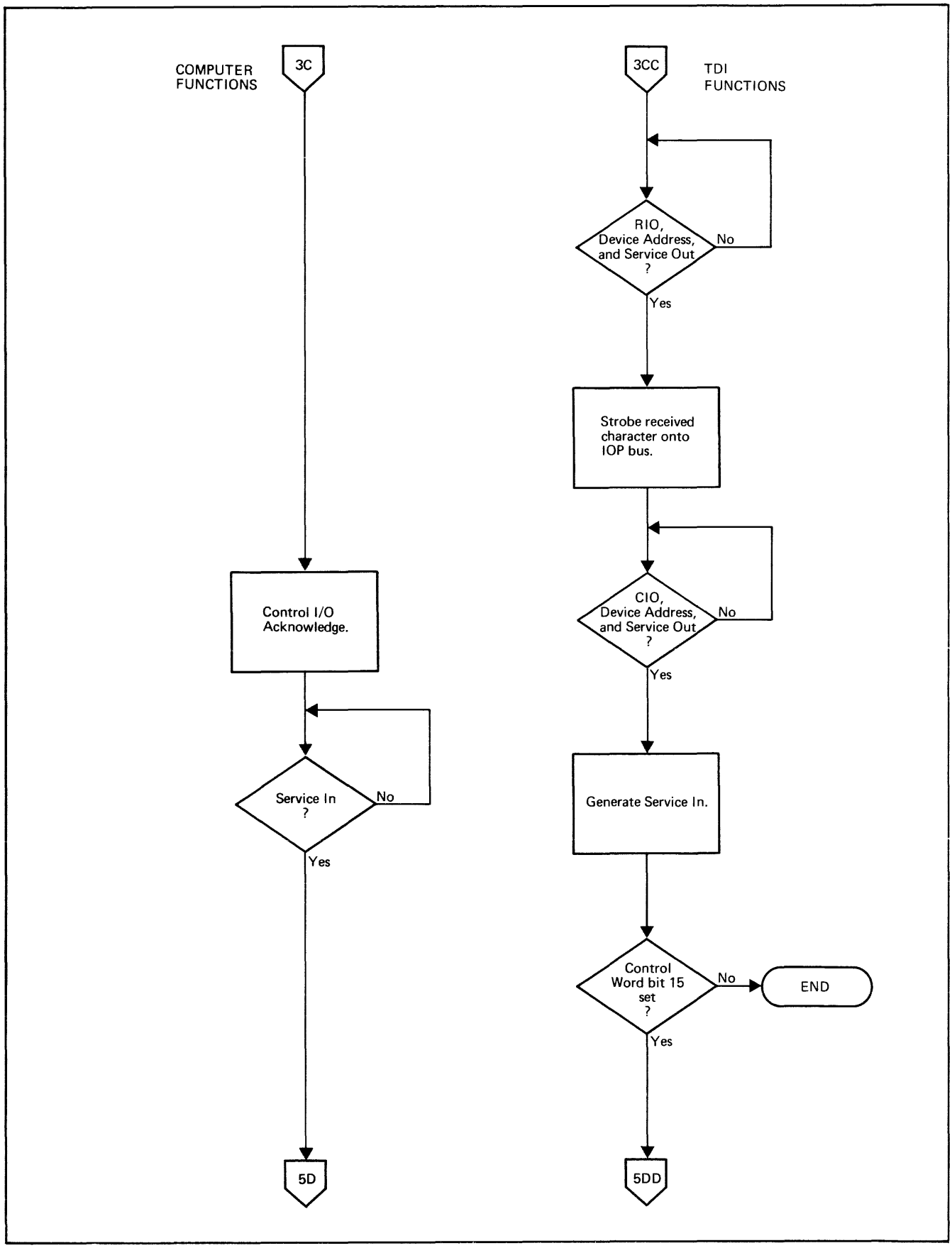
2249-62

Figure 4-2. Intermediate-Level Receive Operation (Sheet 2 of 5)



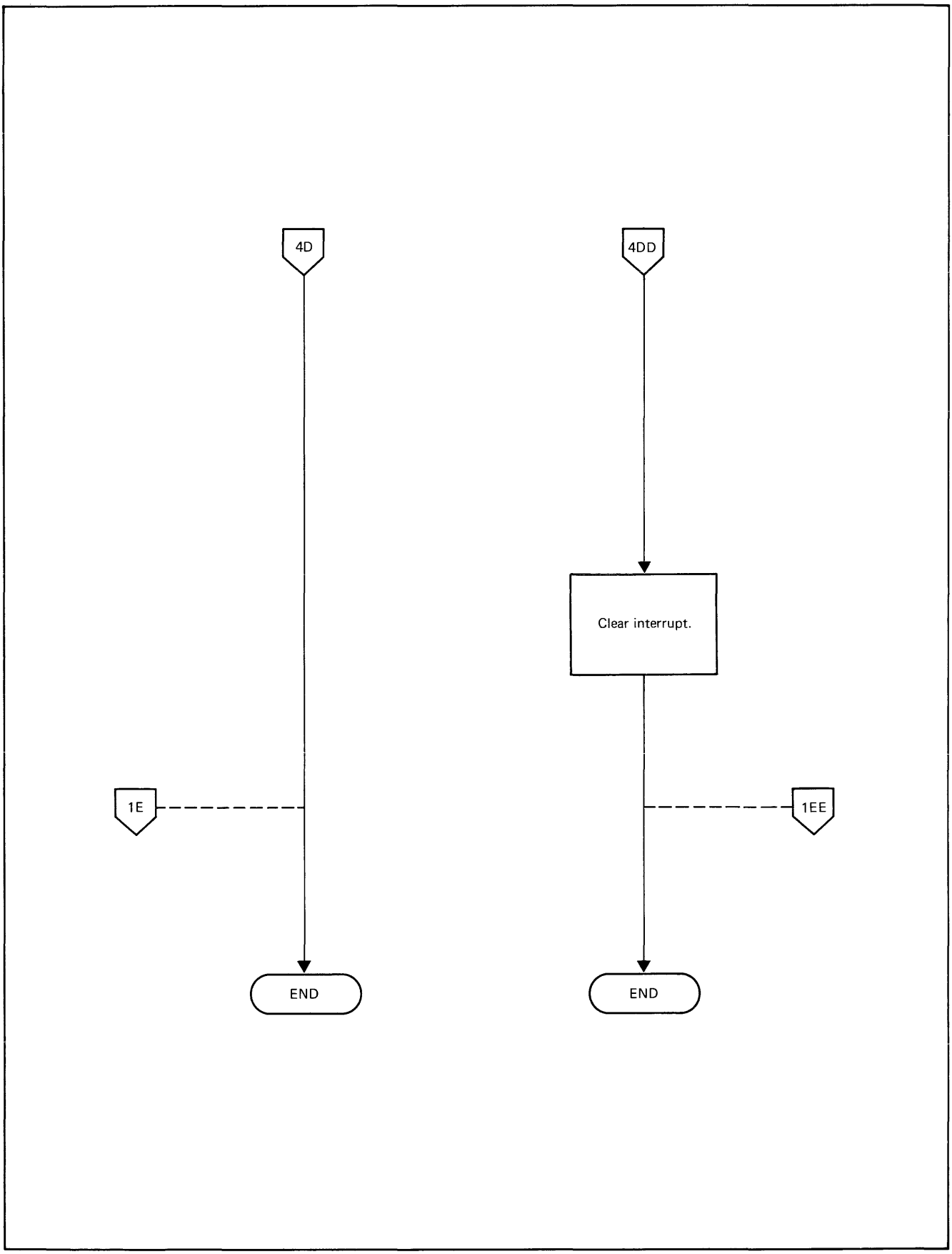
2249-63

Figure 4-2. Intermediate-Level Receive Operation (Sheet 3 of 5)



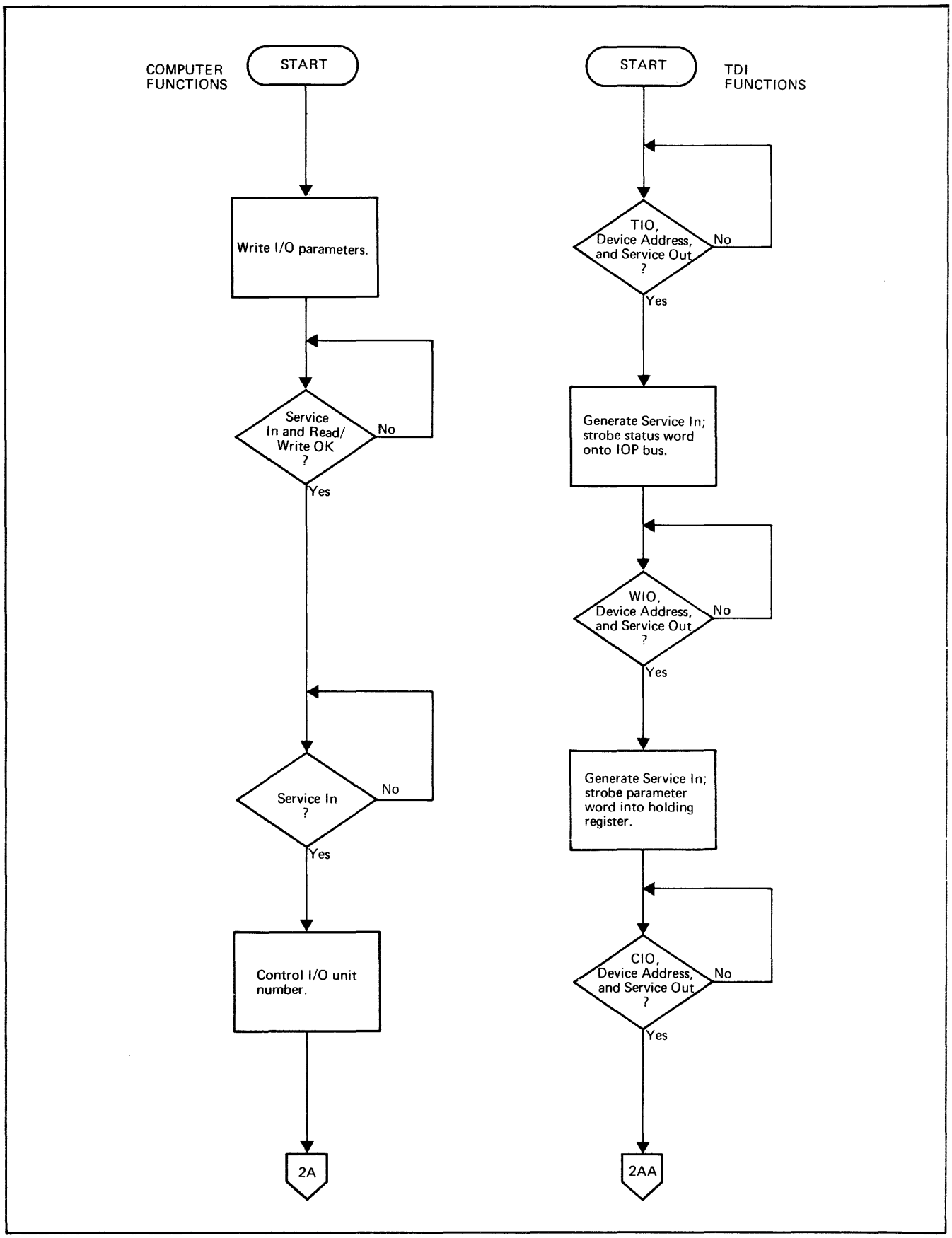
2249-64

Figure 4-2. Intermediate-Level Receive Operation (Sheet 4 of 5)



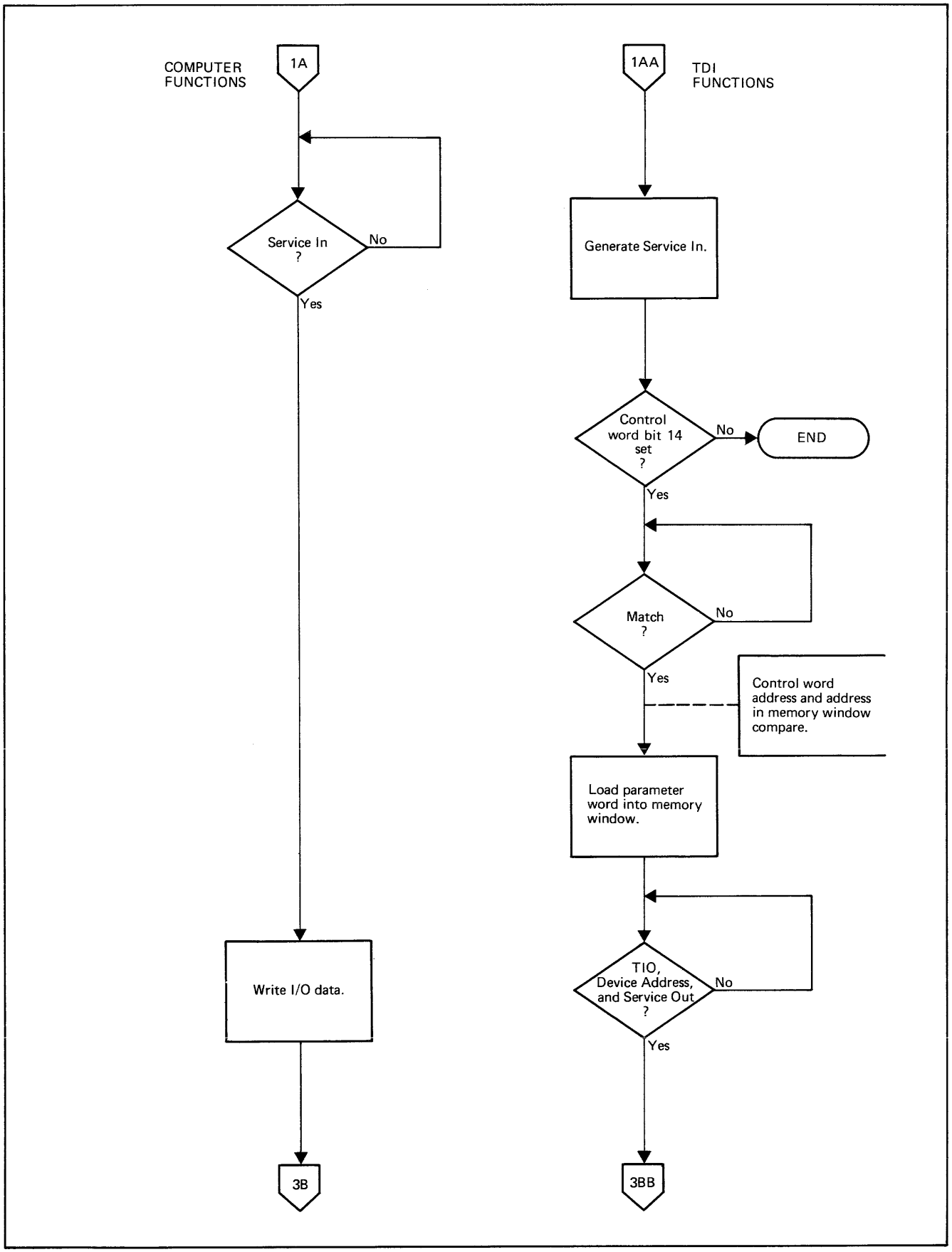
2249-65

Figure 4-2. Intermediate-Level Receive Operation (Sheet 5 of 5)



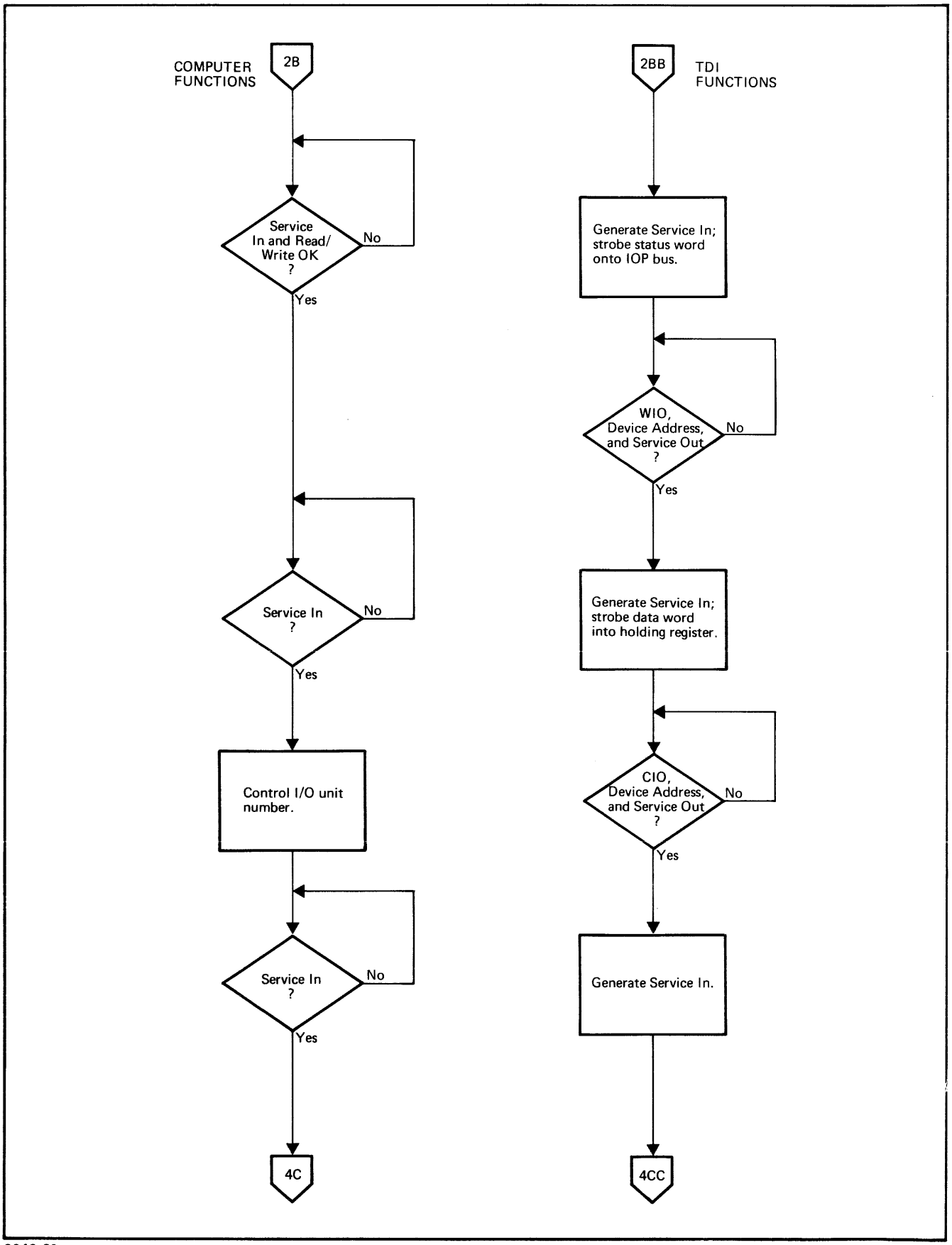
2249-67

Figure 4-3. Intermediate-Level Send Operation (Sheet 1 of 5)



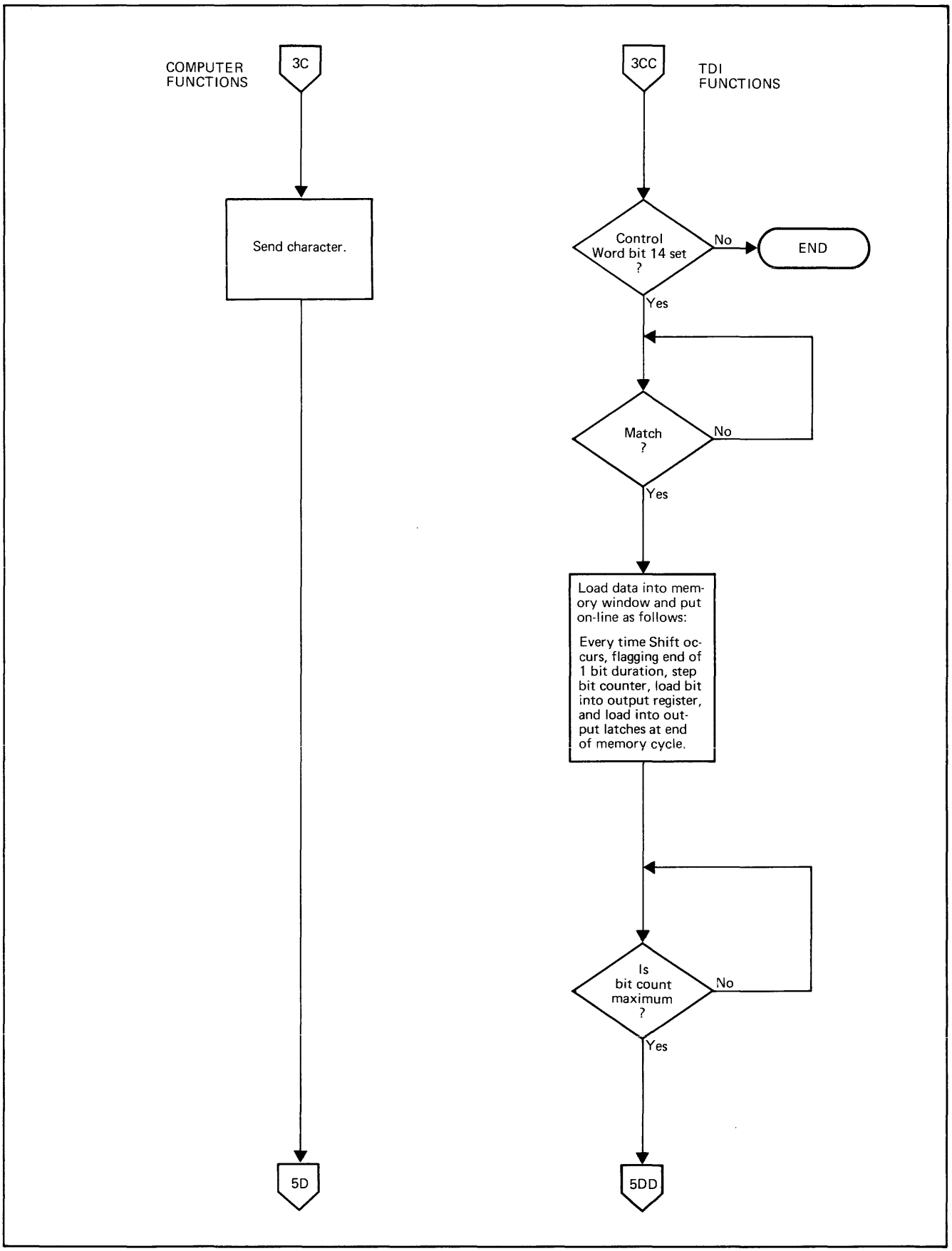
2249-68

Figure 4-3. Intermediate-Level Send Operation (Sheet 2 of 5)



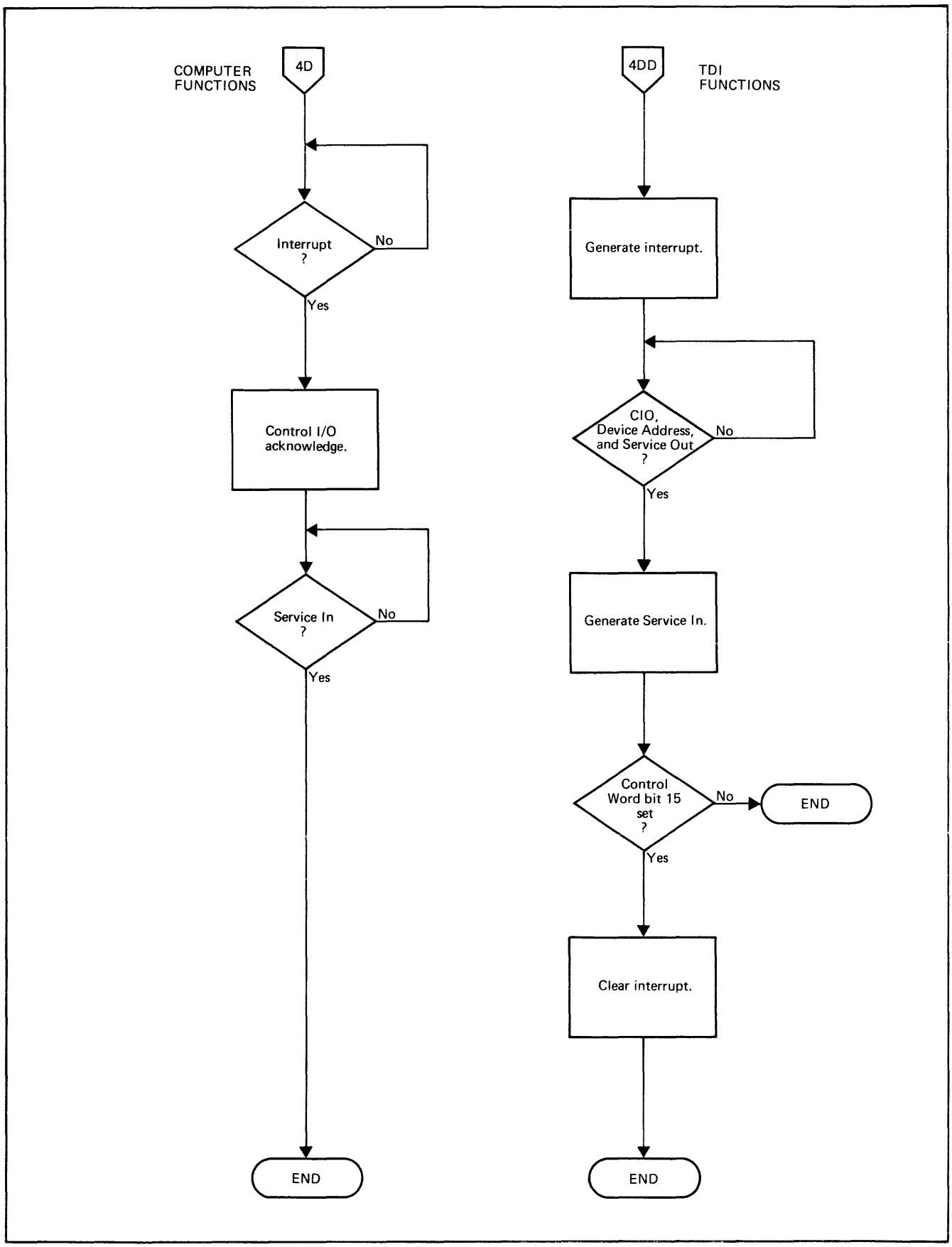
2249-69

Figure 4-3. Intermediate-Level Send Operation (Sheet 3 of 5)



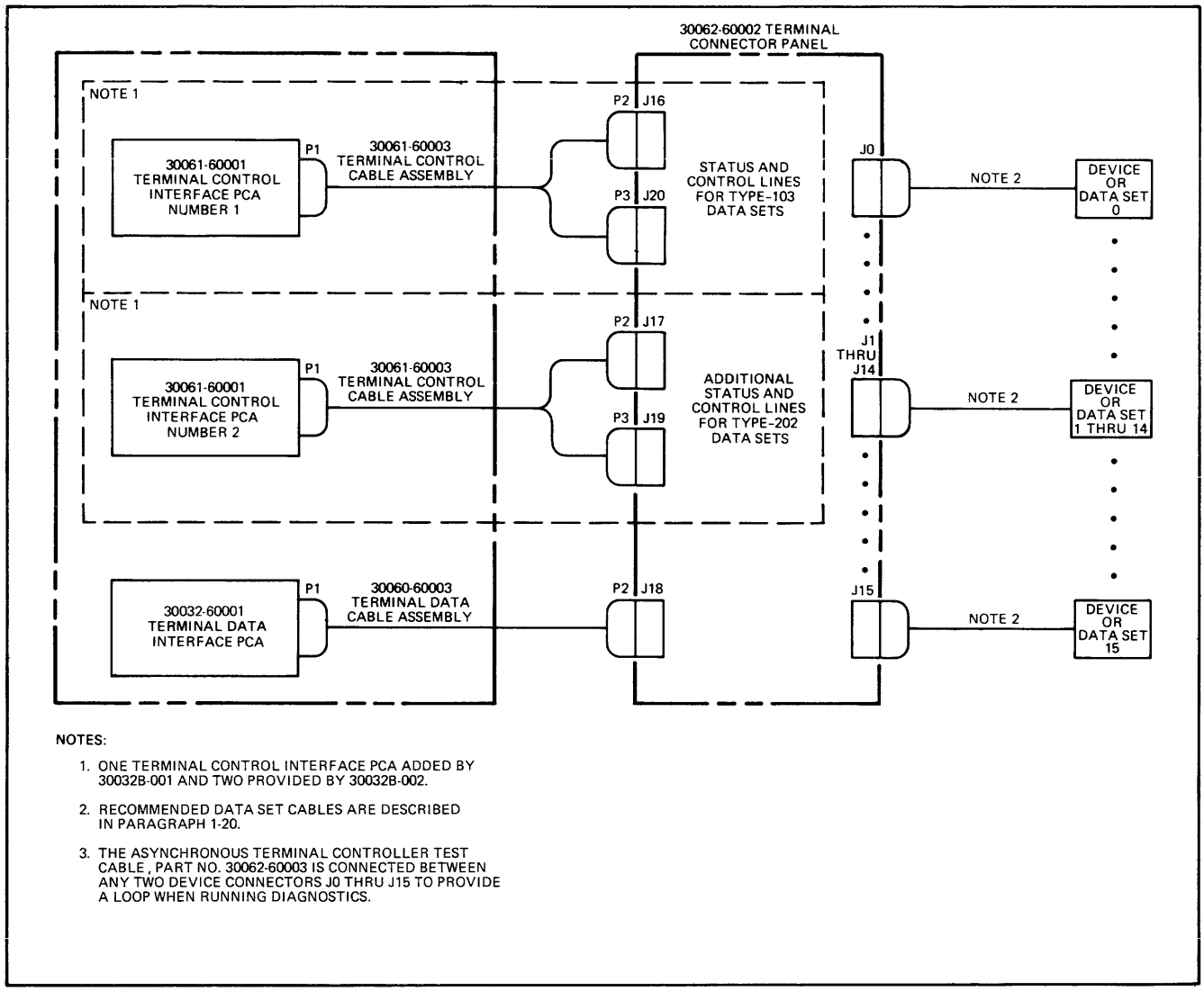
2249-70

Figure 4-3. Intermediate-Level Send Operation (Sheet 4 of 5)



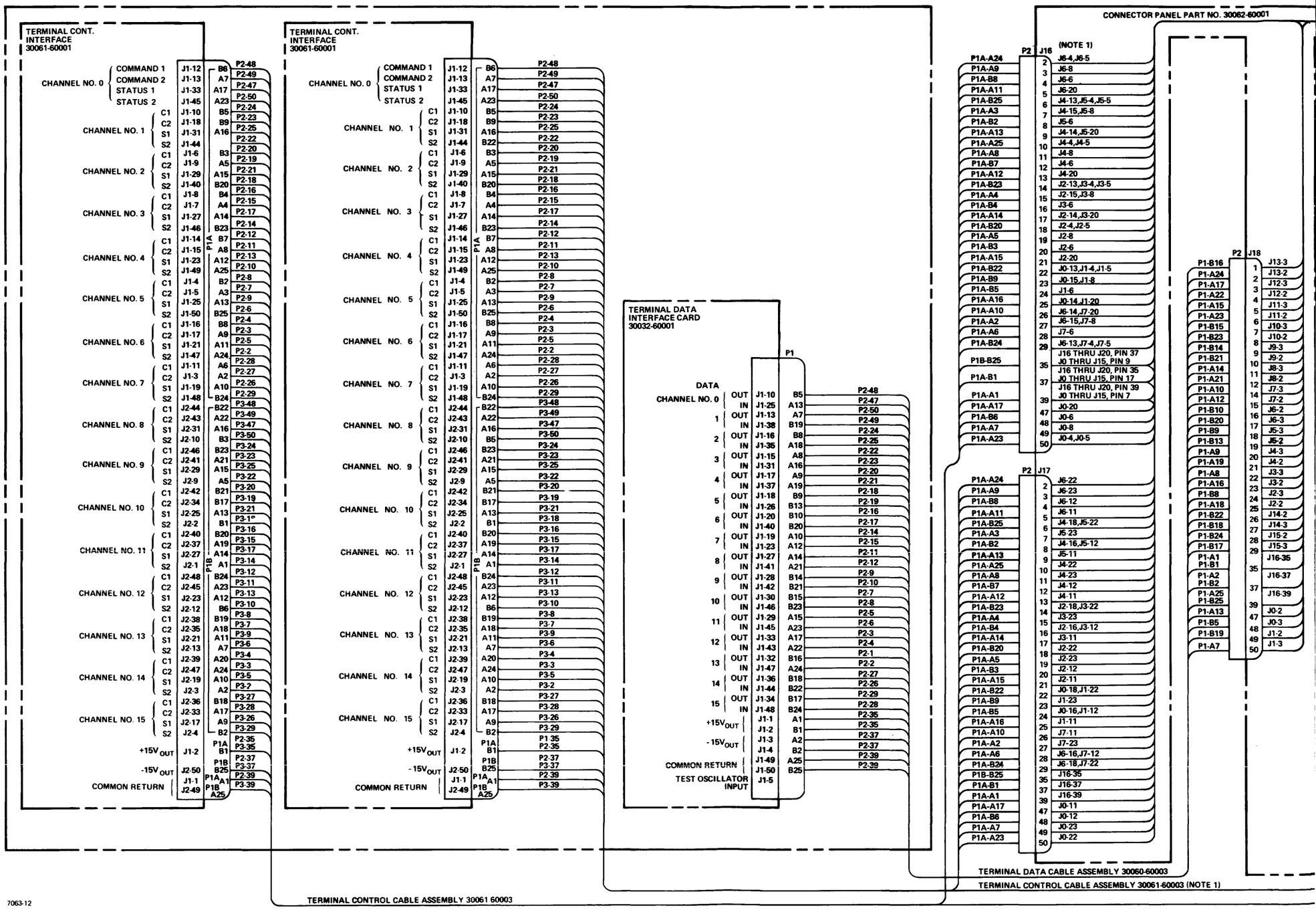
2249-71

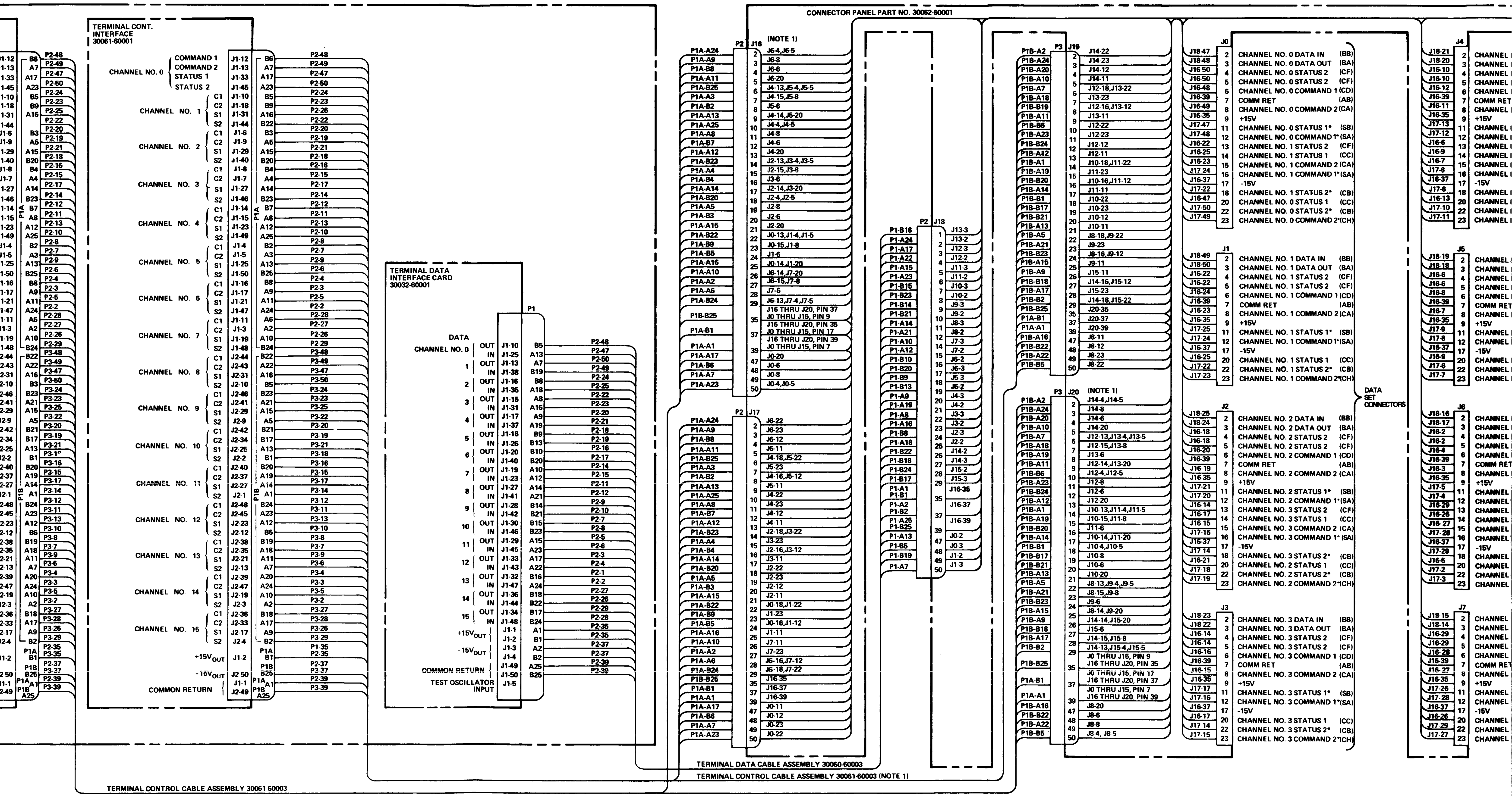
Figure 4-3. Intermediate-Level Send Operation (Sheet 5 of 5)



7063-11

Figure 4-4. Asynchronous Terminal Controller Interconnection Diagram


TERMINAL CONT. INTERFACE 30061-60001
CHANNEL NO. 0
COMMAND 1
COMMAND 2
STATUS 1
STATUS 2
CHANNEL NO. 1
CHANNEL NO. 2
CHANNEL NO. 3
CHANNEL NO. 4
CHANNEL NO. 5
CHANNEL NO. 6
CHANNEL NO. 7
CHANNEL NO. 8
CHANNEL NO. 9
CHANNEL NO. 10
CHANNEL NO. 11
CHANNEL NO. 12
CHANNEL NO. 13
CHANNEL NO. 14
CHANNEL NO. 15
C1
C2
S1
S2
P1A
P1B
+15V OUT
-15V OUT
COMMON RETURN
TERMINAL CONT. INTERFACE 30061-60001
TERMINAL DATA INTERFACE CARD 30032-60001
P1
DATA
OUT
IN
+15V OUT
-15V OUT
COMMON RETURN
TEST OSCILLATOR INPUT
CONNECTOR PANEL PART NO. 30062-60001
P2 J16
(NOTE 1)
P2 J17
P2 J18
TERMINAL DATA CABLE ASSEMBLY 30060-60003
TERMINAL CONTROL CABLE ASSEMBLY 30061-60003 (NOTE 1)
TERMINAL CONTROL CABLE ASSEMBLY 30061 60003
7063-12



TERMINAL CONT. INTERFACE 30061-60001
TERMINAL DATA INTERFACE CARD 30032-60001
CONNECTOR PANEL PART NO. 30062-60001
DATA SET CONNECTORS
TERMINAL DATA CABLE ASSEMBLY 30060-60003
TERMINAL CONTROL CABLE ASSEMBLY 30061-60003 (NOTE 1)
TERMINAL CONTROL CABLE ASSEMBLY 30061 60003
CHANNEL NO. 0
COMMAND 1
COMMAND 2
STATUS 1
STATUS 2
CHANNEL NO. 1
CHANNEL NO. 2
CHANNEL NO. 3
CHANNEL NO. 4
CHANNEL NO. 5
CHANNEL NO. 6
CHANNEL NO. 7
CHANNEL NO. 8
CHANNEL NO. 9
CHANNEL NO. 10
CHANNEL NO. 11
CHANNEL NO. 12
CHANNEL NO. 13
CHANNEL NO. 14
CHANNEL NO. 15
+15V OUT
-15V OUT
COMMON RETURN
DATA
TEST OSCILLATOR INPUT
(NOTE 1)
CHANNEL NO. 0 DATA IN (BB)
CHANNEL NO. 0 DATA OUT (BA)
CHANNEL NO. 0 STATUS 2 (CF)
CHANNEL NO. 0 COMMAND 1 (CD)
COMM RET (AB)
CHANNEL NO. 0 COMMAND 2 (CA)
+15V
-15V
CHANNEL NO. 1 DATA IN (BB)
CHANNEL NO. 1 DATA OUT (BA)
CHANNEL NO. 2 DATA IN (BB)
CHANNEL NO. 2 DATA OUT (BA)
CHANNEL NO. 3 DATA IN (BB)
CHANNEL NO. 3 DATA OUT (BA)
J16 THRU J20, PIN 37
J0 THRU J15, PIN 9
J16 THRU J20, PIN 35
J0 THRU J15, PIN 17
J16 THRU J20, PIN 39
J0 THRU J15, PIN 7

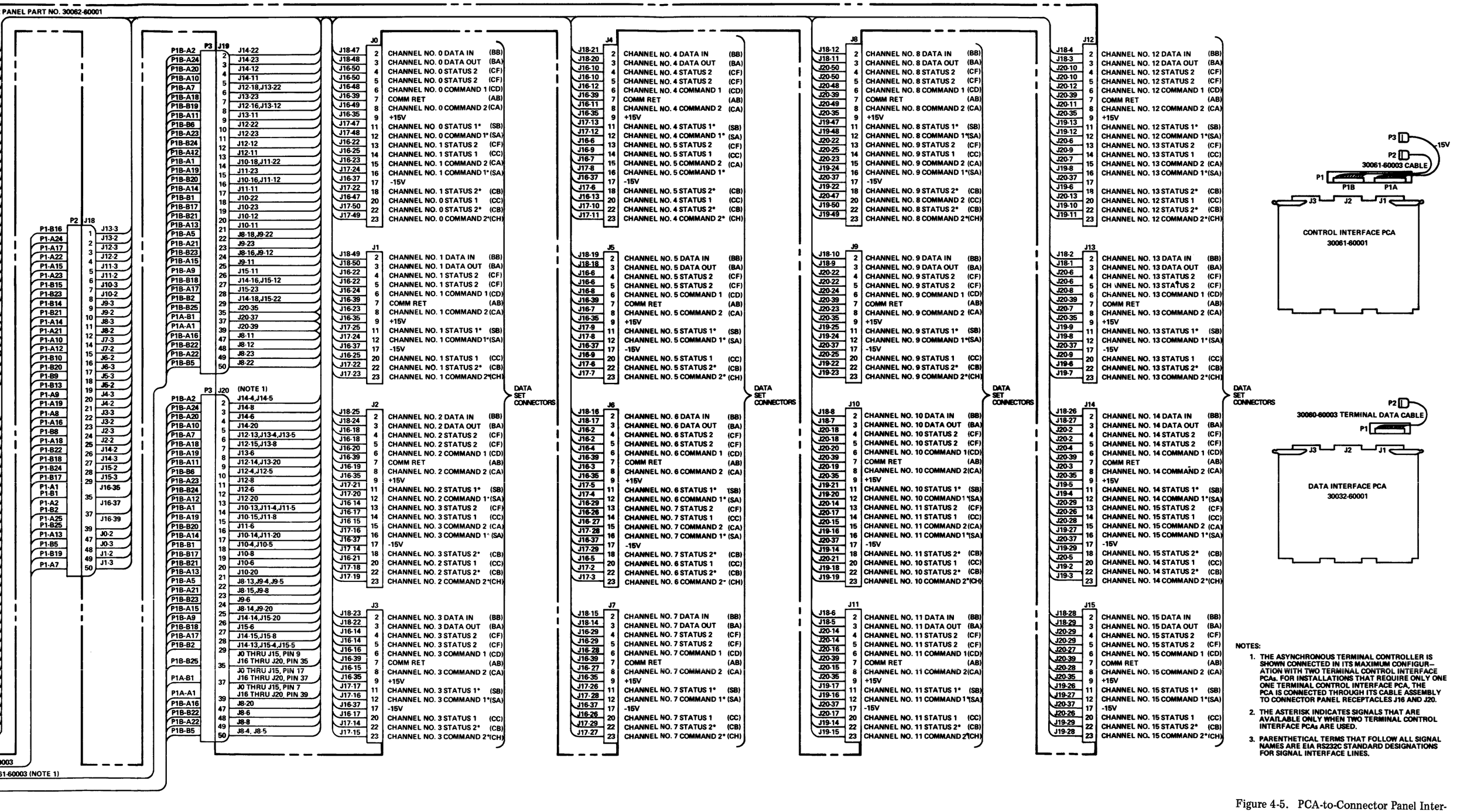
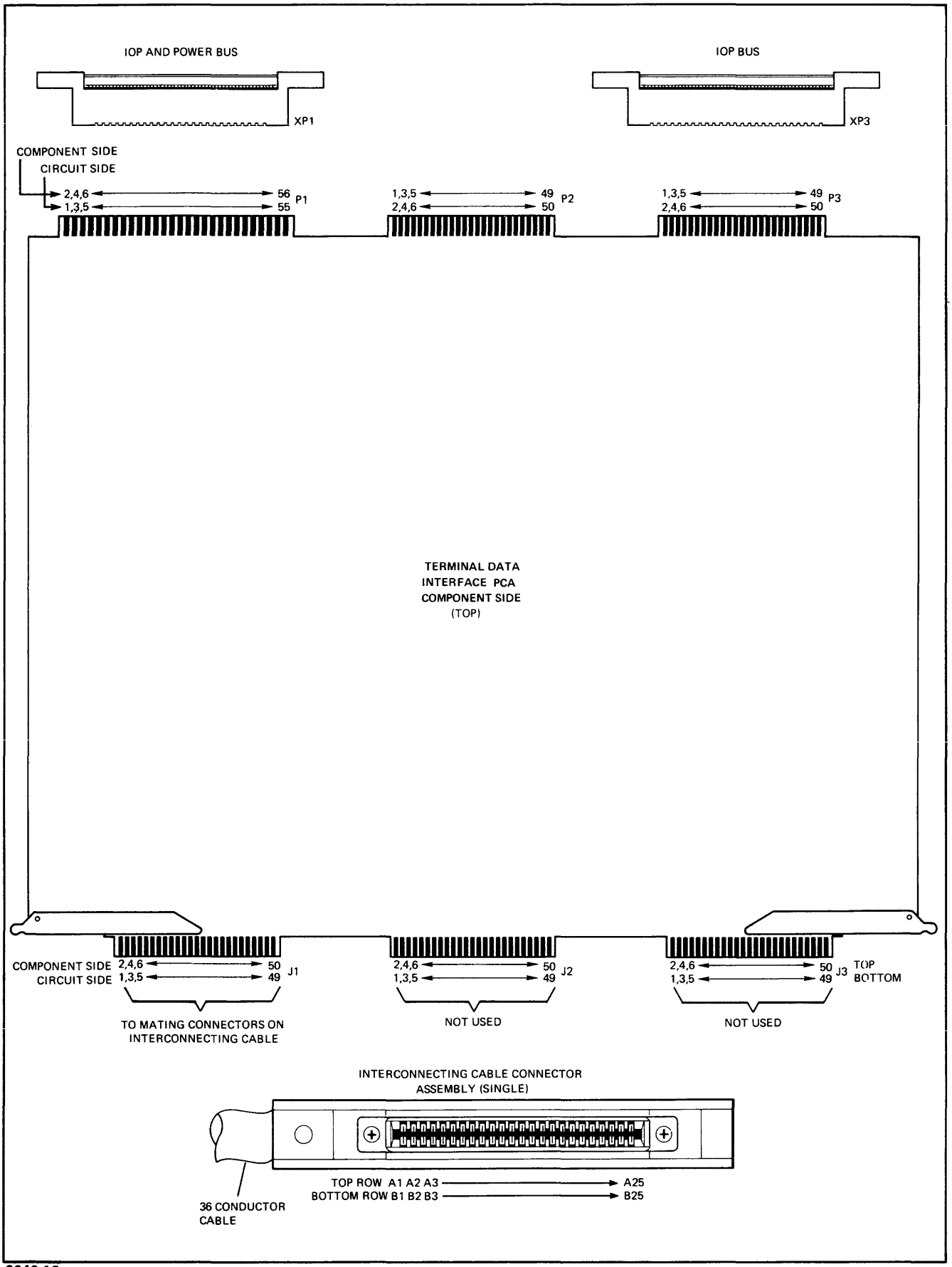
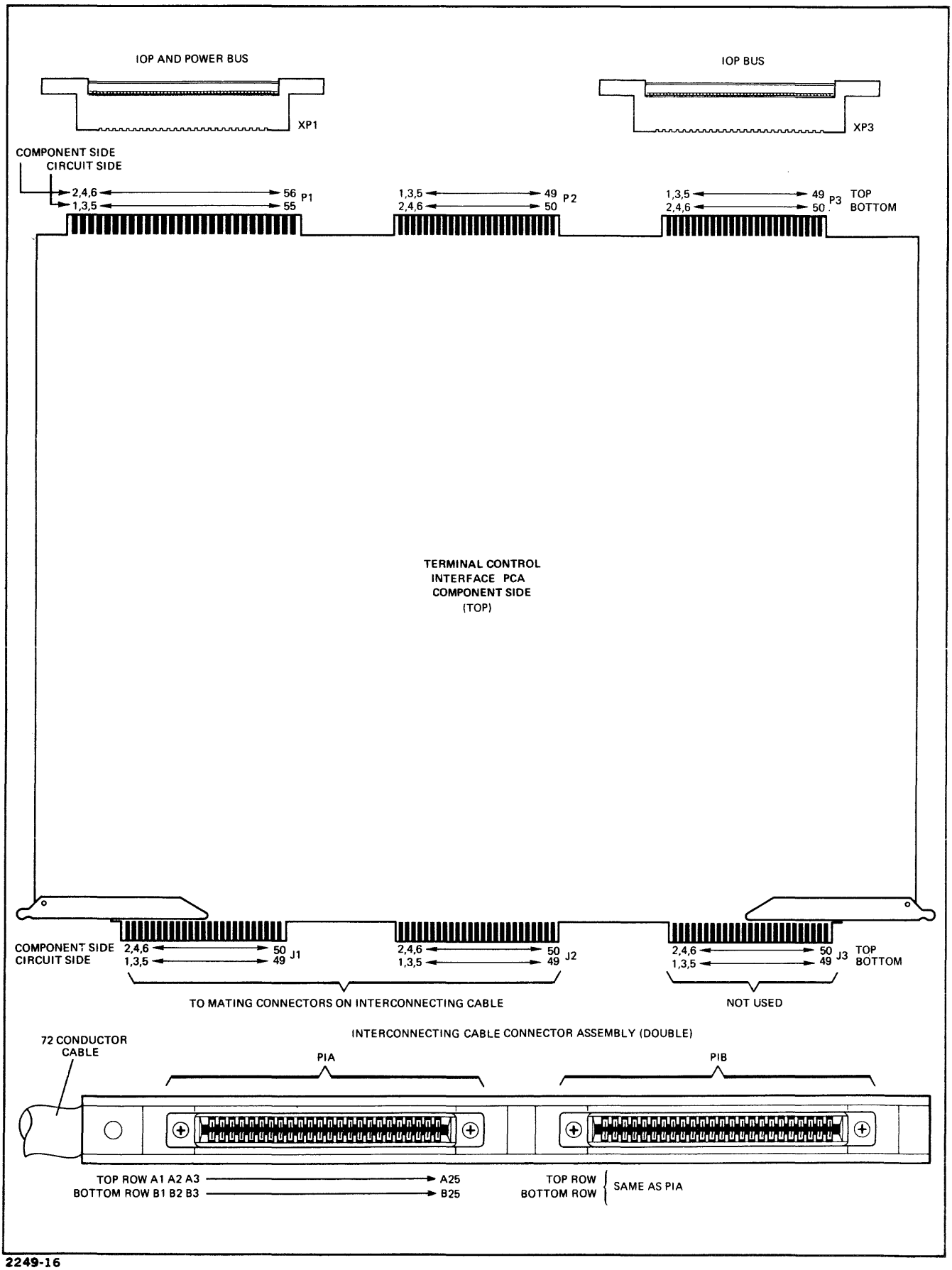


Figure 4-5. PCA-to-Connector Panel Interconnection Diagram



2249-15

Figure 4-6. TDI PCA Connector Diagram



2249-16

Figure 4-7. TCI PCA Connector Diagram

Table 4-1. Terminal Control Interface PCA Signal Index

INTERFACE CARD CONNECTOR J1				INTERFACE CARD CONNECTOR J2			
MATING CONNECTOR PIN NO.	J1 PIN NO.	FIRST PCA SIGNAL	SECOND PCA SIGNAL	MATING CONNECTOR PIN NO.	J2 PIN NO.	FIRST PCA SIGNAL	SECOND PCA SIGNAL
A1	1	Ground	Ground	A1	1	CF11	CB11
B1	2	+15 V_{OUT}	+15 V_{OUT}	B1	2	CF10	CB10
A2	3	CA7	CH7	A2	3	CF14	CB14
B2	4	CD5	SA5	B2	4	CF15	CB15
A3	5	CA5	CH5	A5	9	CF9	CB9
B3	6	CD2	SA2	B3	10	CF8	CB8
A4	7	CA3	CH3	B6	12	CF12	CB12
B4	8	CD3	SA3	A7	13	CF13	CB13
A5	9	CA2	CH2	A9	17	CC15	SB15
B5	10	CD1	SA1	A10	19	CC14	SB14
A6	11	CD7	SA7	A11	21	CC13	SB13
B6	12	CD0	SA0	A12	23	CC12	SB12
A7	13	CA0	CH0	A13	25	CC10	SB10
B7	14	CD4	SA4	A14	27	CC11	SB11
A8	15	CA4	CH4	A15	29	CC9	SB9
B8	16	CD6	SA6	A16	31	CC8	SB8
A9	17	CA6	CH6	A17	33	CA15	CH15
B9	18	CA1	CH1	B17	34	CA10	CH10
A10	19	CC7	SB7	A18	35	CA13	CH13
A11	21	CC6	SB6	B18	36	CD15	SA15
A12	23	CC4	SB4	A19	37	CA11	CH11
A13	25	CC5	SB5	B19	38	CD13	SA13
A14	27	CC3	SB3	A20	39	CD14	SA14
A15	29	CC2	SB2	B20	40	CD11	SA11
A16	31	CC1	SB1	A21	41	CA9	CH9
A17	33	CC0	SB0	B21	42	CD10	SA10
B20	40	CF2	CB2	A22	43	CA8	CH8
B22	41	CF1	CB1	B22	44	CD8	SA8
A23	45	CF0	CB0	A23	45	CA12	CH12
B23	46	CF3	CB3	B23	46	CD9	SA9
A24	47	CF6	CB6	A24	47	CA14	CH14
B24	48	CF7	CB7	B24	48	CD12	SA12
A25	49	CF4	CB4	A25	49	Ground	Ground
B25	50	CF5	CB5	B25	50	-15 V_{OUT}	-15 V_{OUT}

Table 4-2. Terminal Data Interface PCA Signal Index

MATING CONNECTOR PIN NO.	J1 PIN NO.	SIGNAL	MATING CONNECTOR PIN NO.	J1 PIN NO.	SIGNAL
A1, B1	1,2	+15 V_{OUT}	A16	31	BB3
A2, B2	3,4	-15 V_{OUT}	B16	32	BA13
A3	5	External Test Clock	A17	33	BA12
B5	10	BA0	B17	34	BA15
A7	13	BA1	A18	35	BB2
A8	15	BA3	B18	36	BA14
B8	16	BA2	A19	37	BB4
A9	17	BA4	B19	38	BB1
B9	18	BA5		40	BB6
A10	19	BA7	A21	41	BB8
B10	20	BA6	B21	42	BB9
A12	23	BB7	A22	43	BB12
A13	25	BB0	B22	44	BB14
B13	26	BB5	A23	45	BB11
A14	27	BA8	B23	46	BB10
B14	28	BA9	A24	47	BB13
A15	29	BA11	B24	48	BB15
B15	30	BA10	A25, B25	49,50	COMMON

Table 4-3. Extender Cable Signal Index

CONTROLLER CONNECTOR PANEL J0 THRU J15				DATA TERMINAL CONNECTOR		
PIN NO.	DESIGNATION	EIA DESIGNATION		PIN NO.	EIA DESIGNATION	
1				1	Protective Ground	(AA)
2	Data In	Receive Data	(BB)	2	Send Data	(BA)
3	Data Out	Send Data	(BA)	3	Receive Data	(BB)
4	Status 2	Carrier Detect	(CF)	4	Request to Send	(CA)
5	Status 2	Carrier Detect	(CF)	5	Clear to Send	(CB)
6	Command 1	Data Terminal Ready	(CD)	6	Data Set Ready	(CC)
7	Common Return	Signal Ground	(AB)	7	Signal Ground	(AB)
8	Command 2	Request to Send	(CA)	8	Carrier Detect	(CF)
9	+15 Volts			9	Not Used	
10				10	Not Used	
11	Status 1 *	Secondary Receive Data	(SB)	11	Secondary Send Data	(SA)
12	Command 1 *	Secondary Send Data	(SA)	12	Secondary Receive Data	(SB)
13				13	Not Used	
14				14	Not Used	
15				15	Not Used	
16				16	Not Used	
17	-15 Volts			17	Not Used	
18				18	Not Used	
19				19	Not Used	
20	Status 1	Data Set Ready	(CC)	20	Data Terminal Ready	(CD)
21				21	Not Used	
22	Status 2 *	Clear to Send	(CB)	22	Ring Indicator	(CE)
23	Command 2 *	Frequency Select	(CH)	23	Frequency Select	(CI)
24				24	Not Used	
25				25	Not Used	

NOTES:

1. The asterisk indicates signals which are connected to the second (optional) control card.
2. Applies to following cables: 25 ft. 30062-60006 (30062B)
   50 ft. 30062-60009 (30062B-001)
   100 ft. 30062-60012 (30062B-002)
3. Status 1 and 2 lines must be (a) driven, (b) tied to Common, or (c) have corresponding ES1 or ES2 in disable mode via software.

Table 4-4. Dataset Cable Signal Index

CONTROLLER CONNECTOR PANEL J0 THRU J15				DATASET CONNECTOR		
PIN NO.	DESIGNATION	EIA DESIGNATION		PIN NO.	EIA DESIGNATION	
2	Data In	Receive Data	(BB)	3	Receive Data	(BB)
3	Data Out	Send Data	(BA)	2	Send Data	(BA)
4	Status 2	Carrier Detect	(CF)	8	Carrier Detect	(CF)
6	Command 1	Data Terminal Ready	(CD)	20	Data Terminal Ready	(CD)
7	Common Return	Common Return	(AB)	7	Common Return	(AB)
8	Command 2	Request to Send	(CA)	4	Request to Send	(CA)
11	Status 1 *	Secondary Receive Data	(SB)	12	Secondary Receive Data	(SB)
12	Command 1 *	Secondary Send Data	(SA)	11	Secondary Send Data	(SA)
20	Status 1	Data Set Ready	(CC)	6	Data Set Ready	(CC)
22	Status 2 *	Clear to Send	(CB)	5	Clear to Send	(CB)
23	Command 2 *	Frequency Select	(CH)	23	Frequency Select	(CH)

NOTES:

1. The asterisk indicates signals required for 202-type datasets only: they are connected to the second (optional) control card.
2. Applies to following cables: 25 ft. 30062-60004 (30062B)
   50 ft. 30062-60007 (30062B-001)
3. Status 1 and 2 lines must be (a) driven, (b) tied to Common, or (c) have corresponding ES1 or ES2 in disable mode via software.

Table 4-4A. System Console Cable Signal Index

CONTROLLER CONNECTOR PANEL J0 THRU J15				SYSTEM CONSOLE CONNECTOR		
PIN NO.	DESIGNATION	EIA DESIGNATION		PIN NO.	EIA DESIGNATION	
2	Data In	Receive Data	(BB)	2	Receive Data	(BB)
3	Data Out	Send Data	(BA)	3	Send Data	(BA)
7	Common Return	Common Return	(AB)	7	Common Return	(AB)

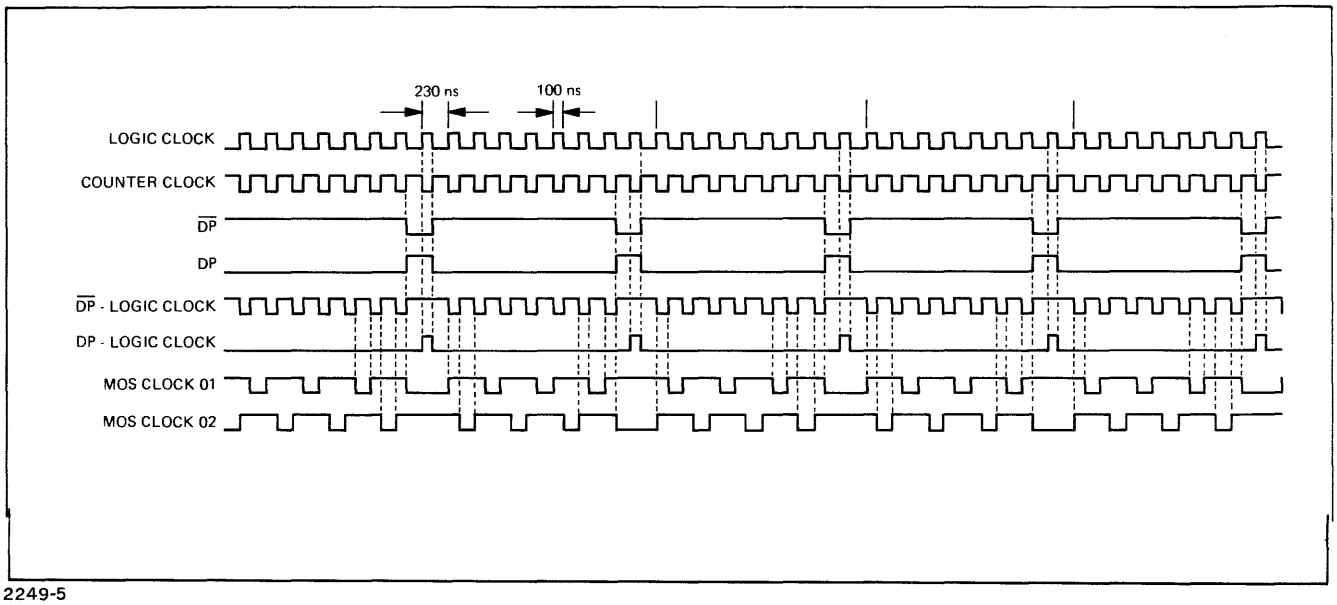
Applies to 25-foot 30062-60018 (30062D)
Pins 4 and 5 are jumpered at the system console end.

Table 4-5. Baud Rate/Bit Duration Reference

DEVICE*	CHARACTERS/SECOND	BAUD RATE	BIT DURATION**
HP 2640, 2644	10	110	9.09 msec
	15	150	6.67 msec
	30	300	3.33 msec
	120	1200	0.833 msec
	240	2400	0.467 msec
HP 2600A	10	110	9.09 msec
	15	150	6.67 msec
	30	300	3.33 msec
	60	600	1.67 msec
	120	1200	0.833 msec
	240	2400	0.467 msec
HP 2749B	10	110	9.09 msec
Memorex 1240	10	110	9.09 msec
	15	150	6.67 msec
	30	300	3.33 msec
	60	600	1.67 msec
IBM 2741		134.5	7.44 msec
ASR-33	10	110	9.09 msec
ASR-35	10	110	9.09 msec
ASR-37	15	150	6.67 msec
HP 2762A	10	110	9.09 msec
	15	150	6.67 msec
	30	300	3.33 msec
HP 2762B	10	110	9.09 msec
	30	300	3.33 msec
	120	1200	0.833 msec

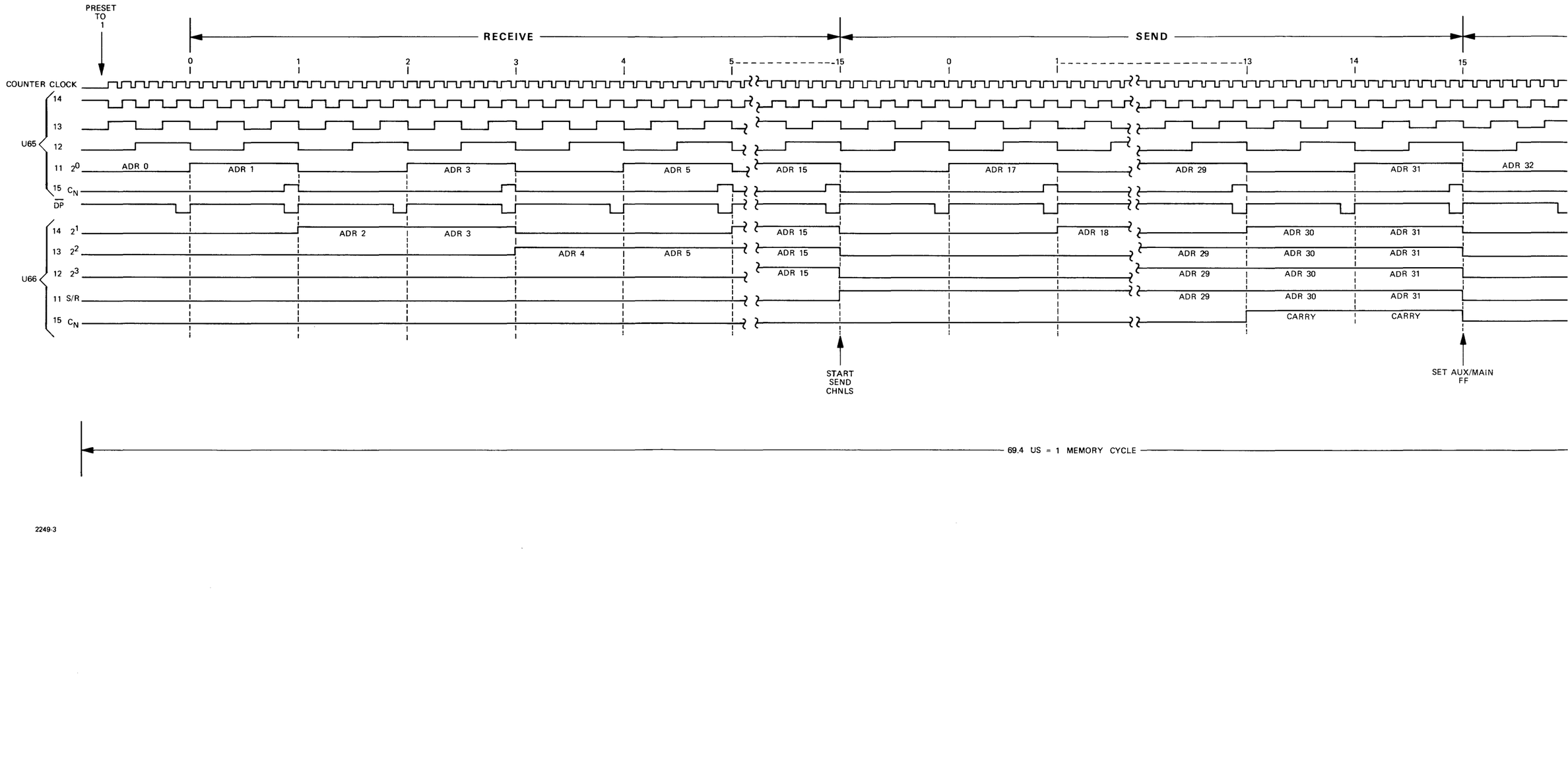
*Devices listed are those currently supported.

**Note: Observe scope trace of transmitted data at pin 2 of the channel connector in question on the connector panel (J0 through J15). Observe received data at pin 3 of the channel connector (J0 through J15) on the connector panel.



2249-5

Figure 4-8. TDI Major Clock and Control Signal Timing Relationships


ACK
PRESET TO 1
RECEIVE
SEND
0
1
2
3
4
5
15
0
1
13
14
15
COUNTER CLOCK
U65
14
13
12
11 2^0
15 C_N
$\overline{DP}$
ADR 0
ADR 1
ADR 3
ADR 5
ADR 15
ADR 17
ADR 29
ADR 31
ADR 32
U66
14 2^1
13 2^2
12 2^3
11 S/R
15 C_N
ADR 2
ADR 3
ADR 4
ADR 5
ADR 15
ADR 18
ADR 29
ADR 30
ADR 31
CARRY
START SEND CHNLS
SET AUX/MAIN FF
69.4 US = 1 MEMORY CYCLE

2249-3

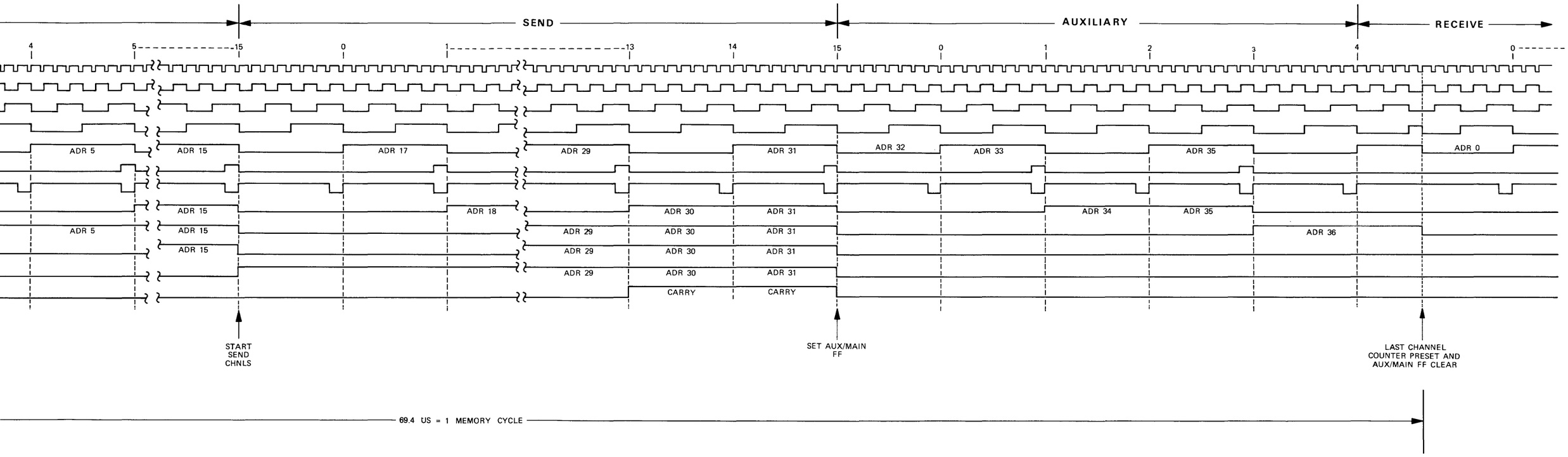
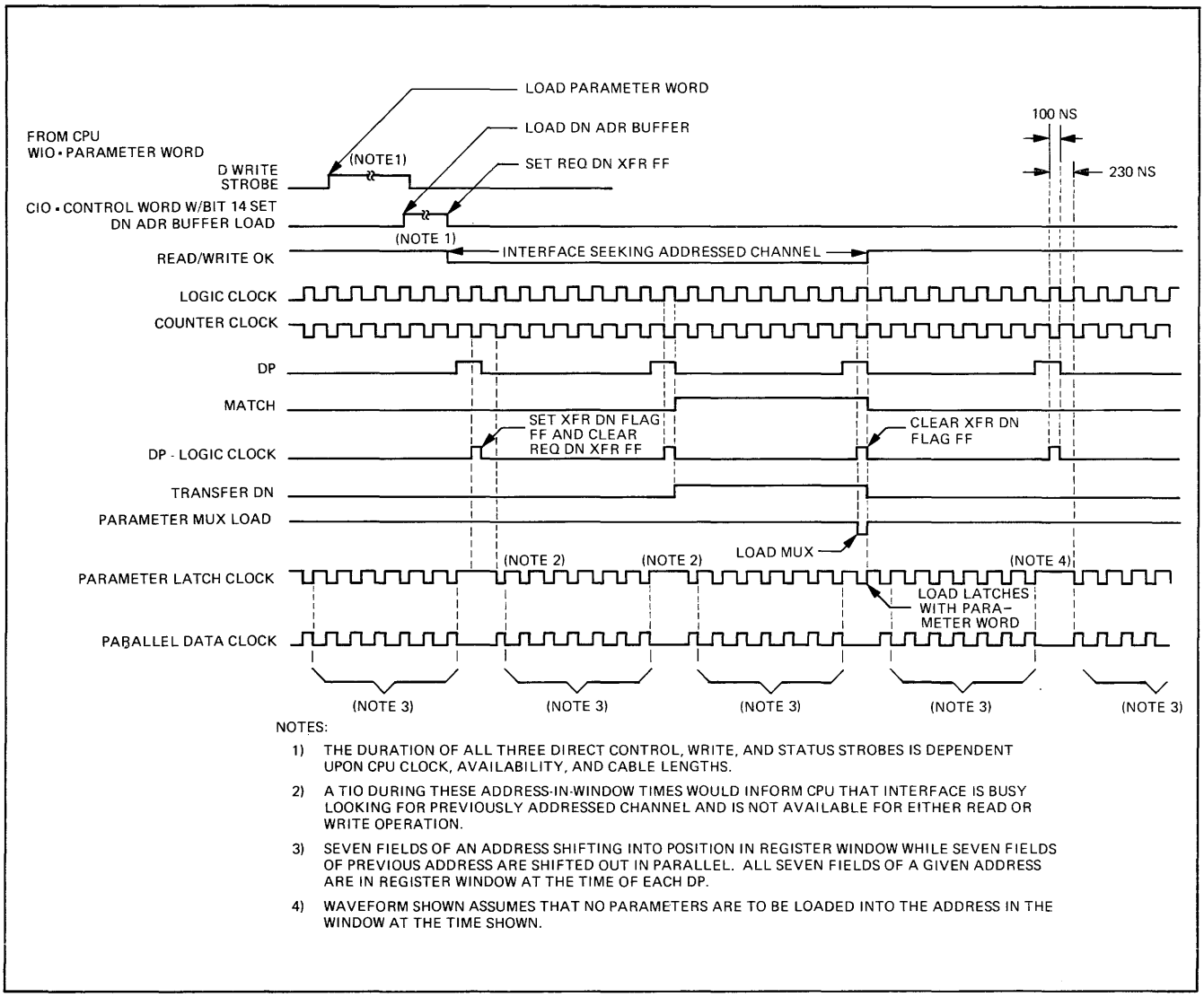


Figure 4-9. TDI Clock, DP, and Address Generation Timing



NOTES:

1) THE DURATION OF ALL THREE DIRECT CONTROL, WRITE, AND STATUS STROBES IS DEPENDENT UPON CPU CLOCK, AVAILABILITY, AND CABLE LENGTHS.

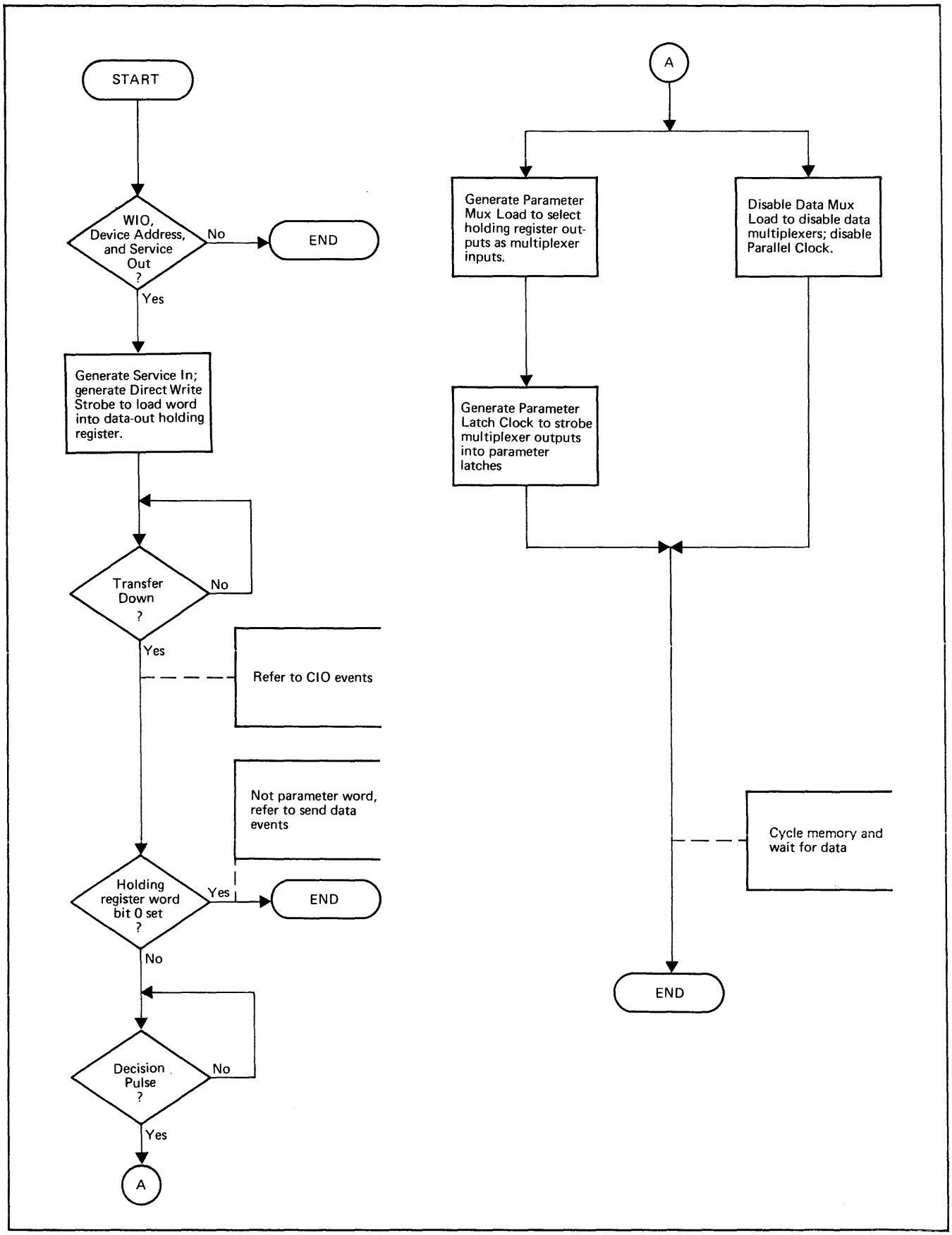
2) A TIO DURING THESE ADDRESS-IN-WINDOW TIMES WOULD INFORM CPU THAT INTERFACE IS BUSY LOOKING FOR PREVIOUSLY ADDRESSED CHANNEL AND IS NOT AVAILABLE FOR EITHER READ OR WRITE OPERATION.

3) SEVEN FIELDS OF AN ADDRESS SHIFTING INTO POSITION IN REGISTER WINDOW WHILE SEVEN FIELDS OF PREVIOUS ADDRESS ARE SHIFTED OUT IN PARALLEL. ALL SEVEN FIELDS OF A GIVEN ADDRESS ARE IN REGISTER WINDOW AT THE TIME OF EACH DP.

4) WAVEFORM SHOWN ASSUMES THAT NO PARAMETERS ARE TO BE LOADED INTO THE ADDRESS IN THE WINDOW AT THE TIME SHOWN.

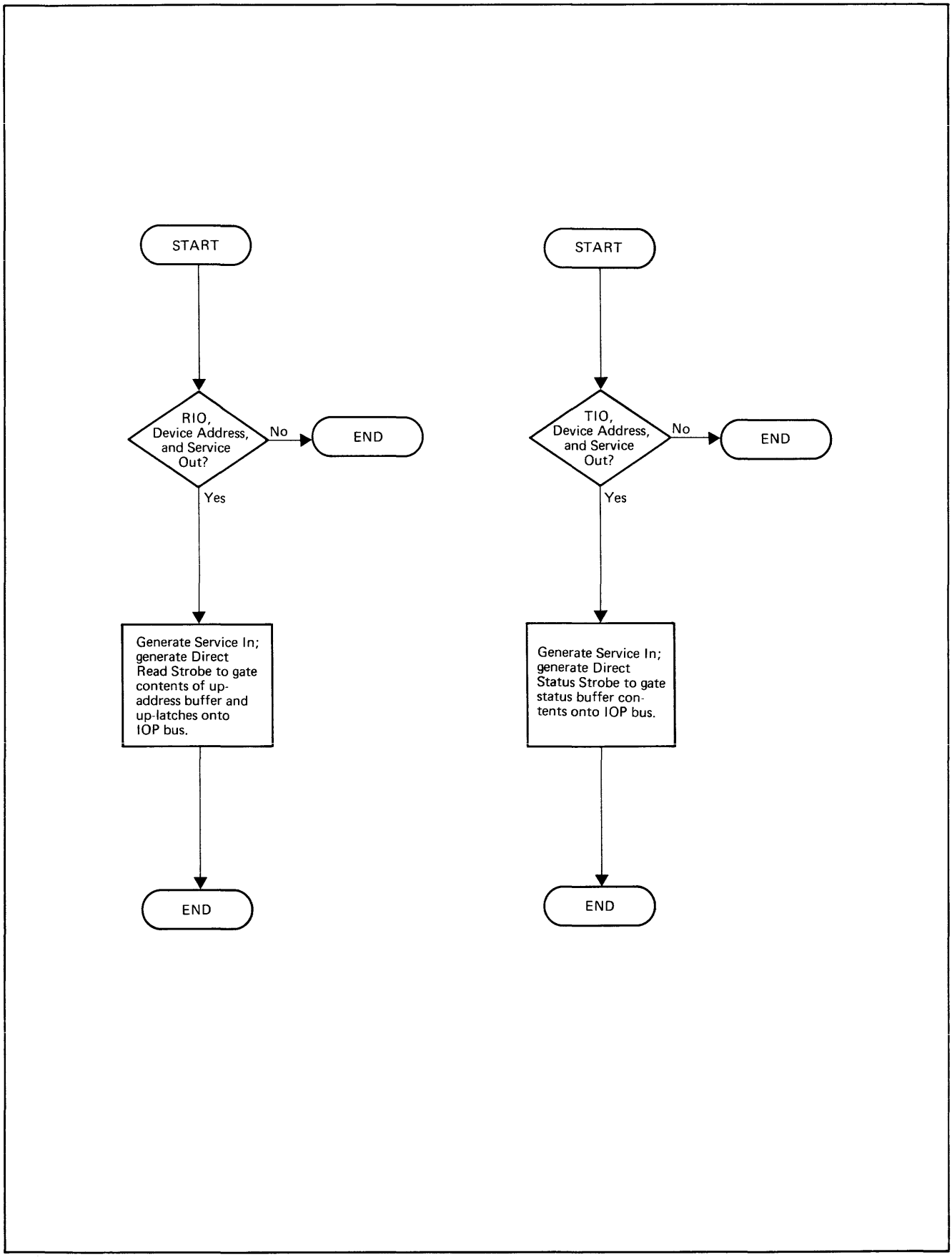
2249-6

Figure 4-10. TDI Channel Configuration Timing



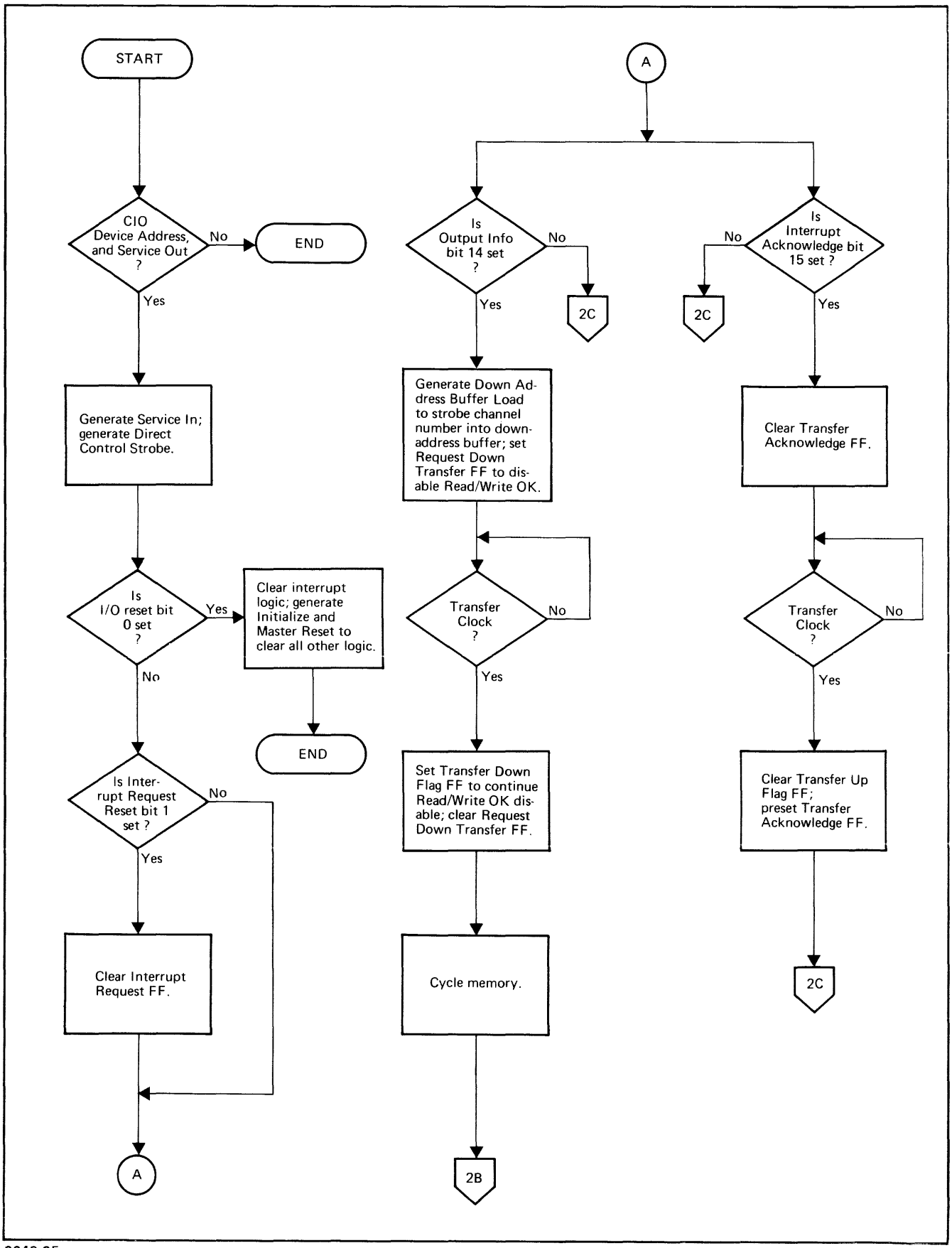
2249-28

Figure 4-11. TDI Parameter Loading Events Flowchart



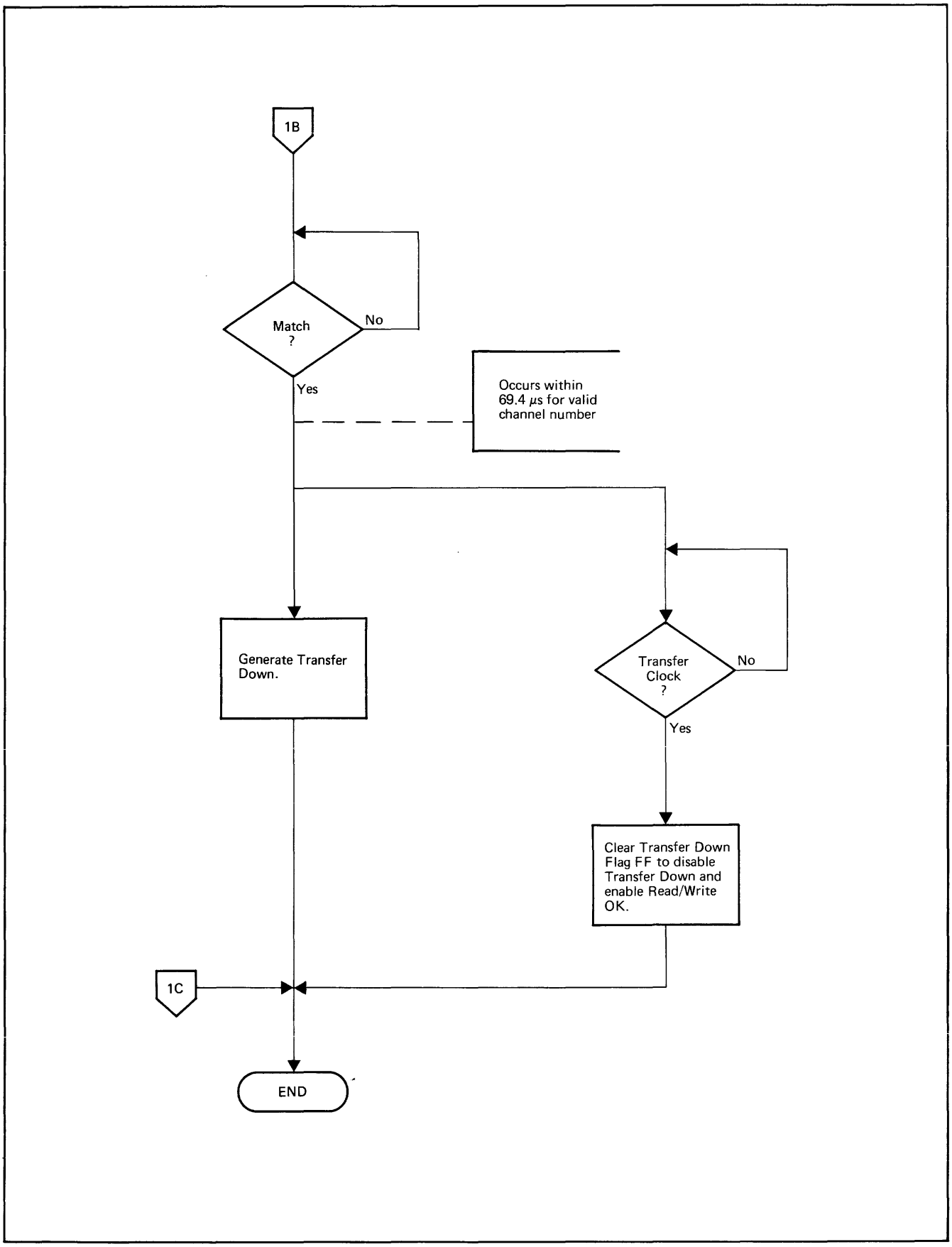
2249-27

Figure 4-12. TDI Read and Status-Fetch Flowcharts



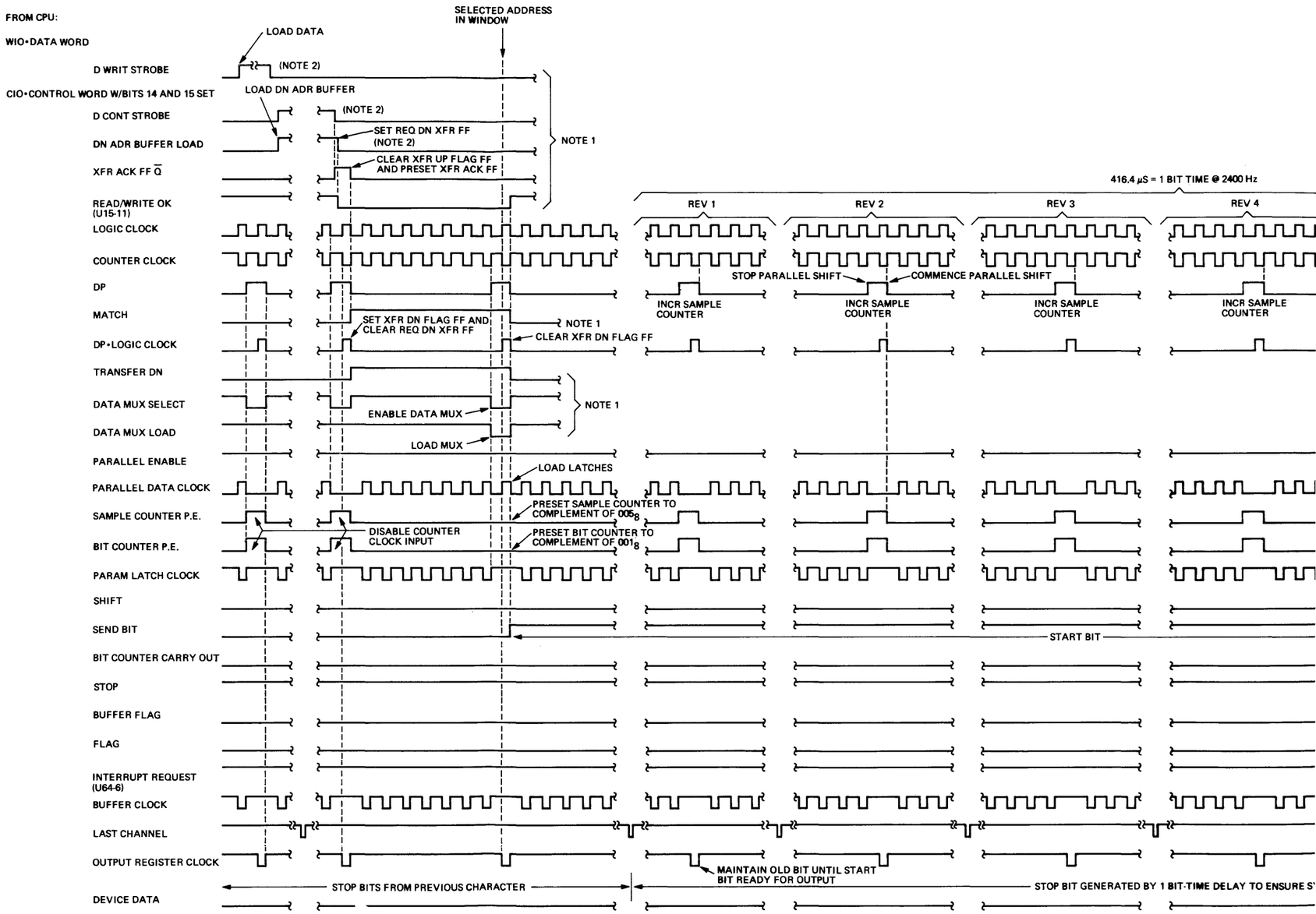
2249-25

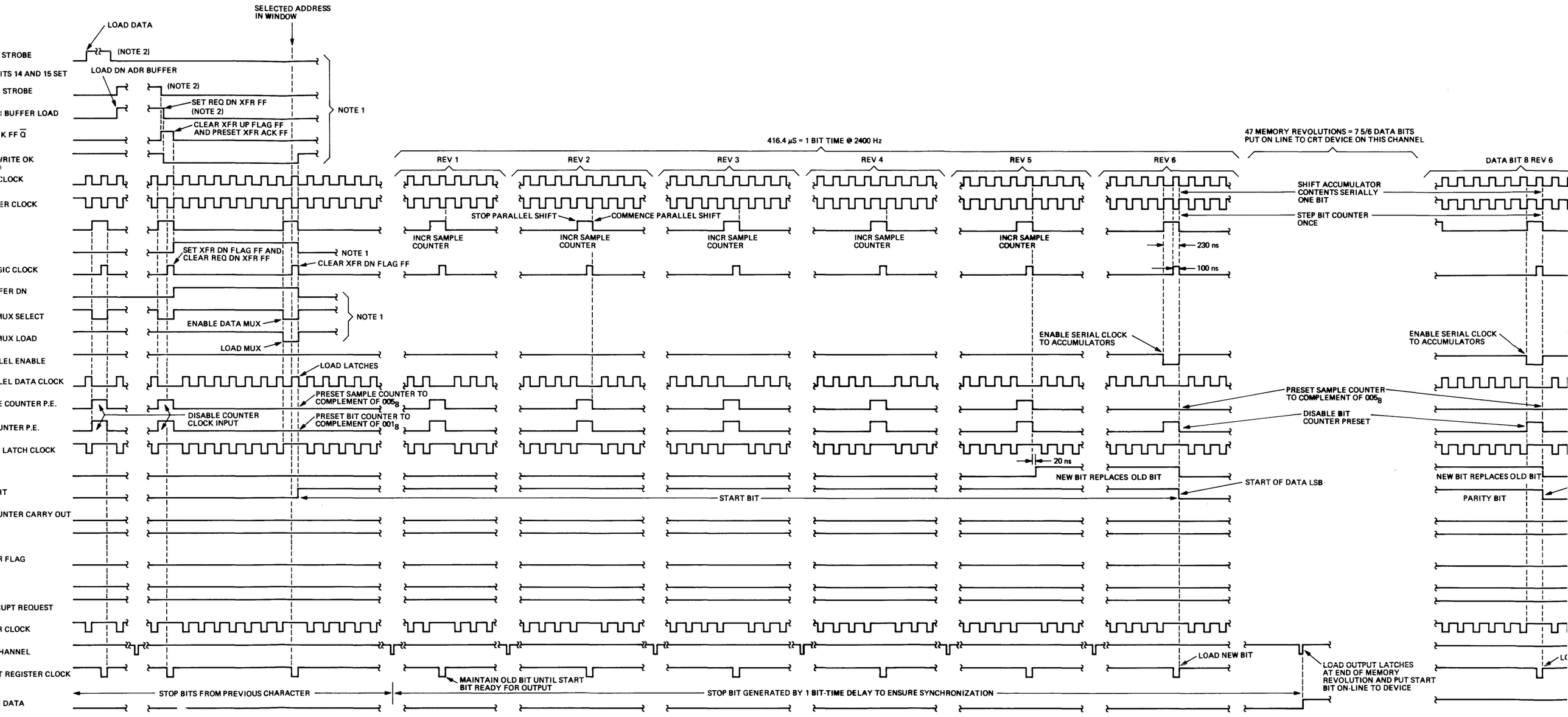
Figure 4-13. TDI CIO Events Flowchart (Sheet 1 of 2)



2249-26

Figure 4-13. TDI CIO Events Flowchart (Sheet 2 of 2)


FROM CPU:
WIO•DATA WORD
D WRIT STROBE
CIO•CONTROL WORD W/BITS 14 AND 15 SET
D CONT STROBE
DN ADR BUFFER LOAD
XFR ACK FF Q̄
READ/WRITE OK (U15-11)
LOGIC CLOCK
COUNTER CLOCK
DP
MATCH
DP•LOGIC CLOCK
TRANSFER DN
DATA MUX SELECT
DATA MUX LOAD
PARALLEL ENABLE
PARALLEL DATA CLOCK
SAMPLE COUNTER P.E.
BIT COUNTER P.E.
PARAM LATCH CLOCK
SHIFT
SEND BIT
BIT COUNTER CARRY OUT
STOP
BUFFER FLAG
FLAG
INTERRUPT REQUEST (U64-6)
BUFFER CLOCK
LAST CHANNEL
OUTPUT REGISTER CLOCK
DEVICE DATA
SELECTED ADDRESS IN WINDOW
LOAD DATA
(NOTE 2)
LOAD DN ADR BUFFER
(NOTE 2)
SET REQ DN XFR FF (NOTE 2)
CLEAR XFR UP FLAG FF AND PRESET XFR ACK FF
NOTE 1
416.4 μS = 1 BIT TIME @ 2400 Hz
REV 1
REV 2
REV 3
REV 4
STOP PARALLEL SHIFT
COMMENCE PARALLEL SHIFT
INCR SAMPLE COUNTER
SET XFR DN FLAG FF AND CLEAR REQ DN XFR FF
NOTE 1
CLEAR XFR DN FLAG FF
ENABLE DATA MUX
NOTE 1
LOAD MUX
LOAD LATCHES
PRESET SAMPLE COUNTER TO COMPLEMENT OF 005_8
DISABLE COUNTER CLOCK INPUT
PRESET BIT COUNTER TO COMPLEMENT OF 001_8
START BIT
MAINTAIN OLD BIT UNTIL START BIT READY FOR OUTPUT
STOP BITS FROM PREVIOUS CHARACTER
STOP BIT GENERATED BY 1 BIT-TIME DELAY TO ENSURE S


SELECTED ADDRESS IN WINDOW
LOAD DATA
(NOTE 2)
LOAD DN ADR BUFFER
(NOTE 2)
SET REQ DN XFR FF (NOTE 2)
CLEAR XFR UP FLAG FF AND PRESET XFR ACK FF
NOTE 1
STROBE
ITS 14 AND 15 SET
STROBE
BUFFER LOAD
K FF Q
RITE OK
CLOCK
ER CLOCK
416.4 μS = 1 BIT TIME @ 2400 Hz
REV 1
REV 2
REV 3
REV 4
REV 5
REV 6
47 MEMORY REVOLUTIONS = 7 5/6 DATA BITS PUT ON LINE TO CRT DEVICE ON THIS CHANNEL
DATA BIT 8 REV 6
SHIFT ACCUMULATOR CONTENTS SERIALLY ONE BIT
STEP BIT COUNTER ONCE
STOP PARALLEL SHIFT
COMMENCE PARALLEL SHIFT
INCR SAMPLE COUNTER
230 ns
100 ns
SET XFR DN FLAG FF AND CLEAR REQ DN XFR FF
NOTE 1
CLEAR XFR DN FLAG FF
GIC CLOCK
FER DN
UX SELECT
UX LOAD
ENABLE DATA MUX
LOAD MUX
NOTE 1
LEL ENABLE
LEL DATA CLOCK
LOAD LATCHES
ENABLE SERIAL CLOCK TO ACCUMULATORS
E COUNTER P.E.
UNTER P.E.
PRESET SAMPLE COUNTER TO COMPLEMENT OF 005₈
DISABLE COUNTER CLOCK INPUT
PRESET BIT COUNTER TO COMPLEMENT OF 001₈
DISABLE BIT COUNTER PRESET
LATCH CLOCK
20 ns
NEW BIT REPLACES OLD BIT
START OF DATA LSB
IT
START BIT
PARITY BIT
UNTER CARRY OUT
R FLAG
UPT REQUEST
R CLOCK
HANNEL
T REGISTER CLOCK
LOAD NEW BIT
LOAD OUTPUT LATCHES AT END OF MEMORY REVOLUTION AND PUT START BIT ON-LINE TO DEVICE
MAINTAIN OLD BIT UNTIL START BIT READY FOR OUTPUT
STOP BITS FROM PREVIOUS CHARACTER
STOP BIT GENERATED BY 1 BIT-TIME DELAY TO ENSURE SYNCHRONIZATION
DATA

NOTES:

1. THESE SIGNALS ARE GENERATED/REQUIRED ONCE PER CHARACTER TRANSMISSION.
2. THE DURATION OF DIRECT CONTROL AND WRITE STROBES AND SIGNALS GENERATED BY THESE STROBES IS DEPENDENT UPON CPU TIMING, AVAILABILITY AND CABLE LENGTHS.

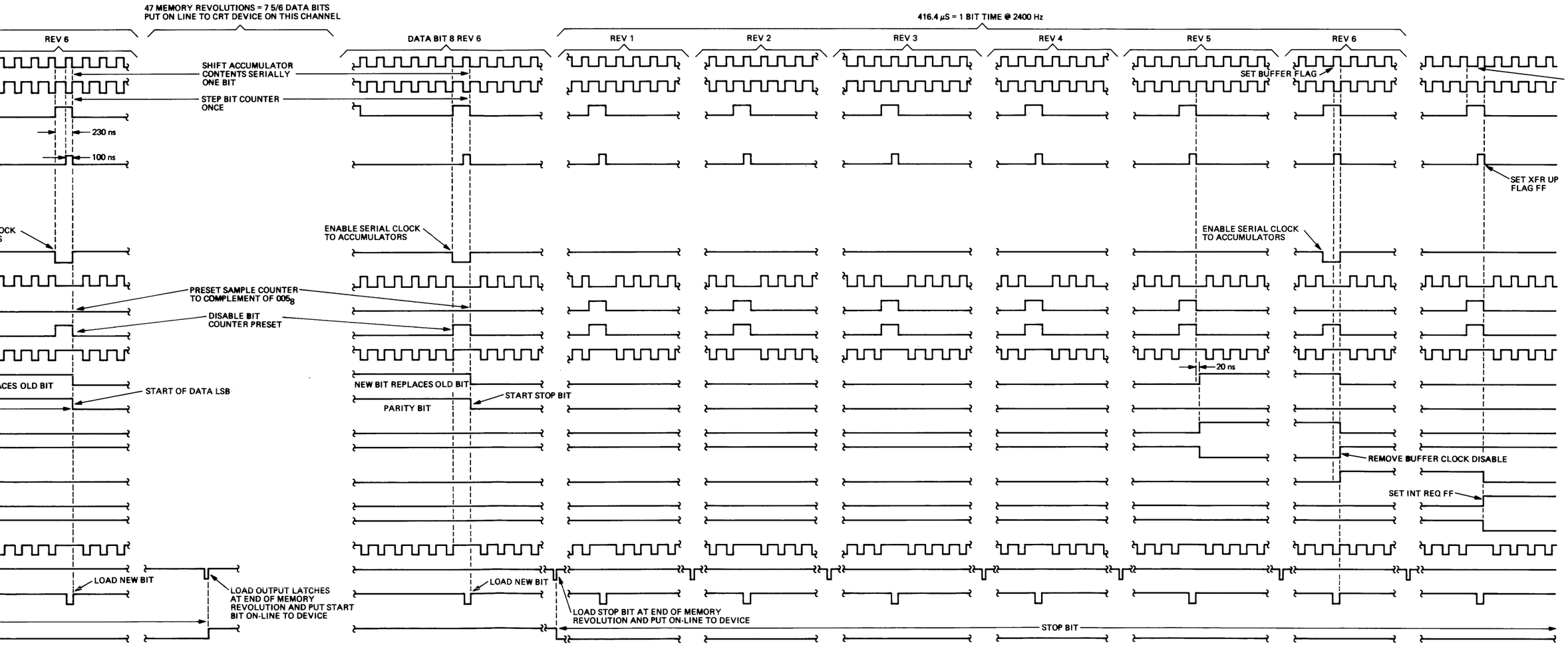
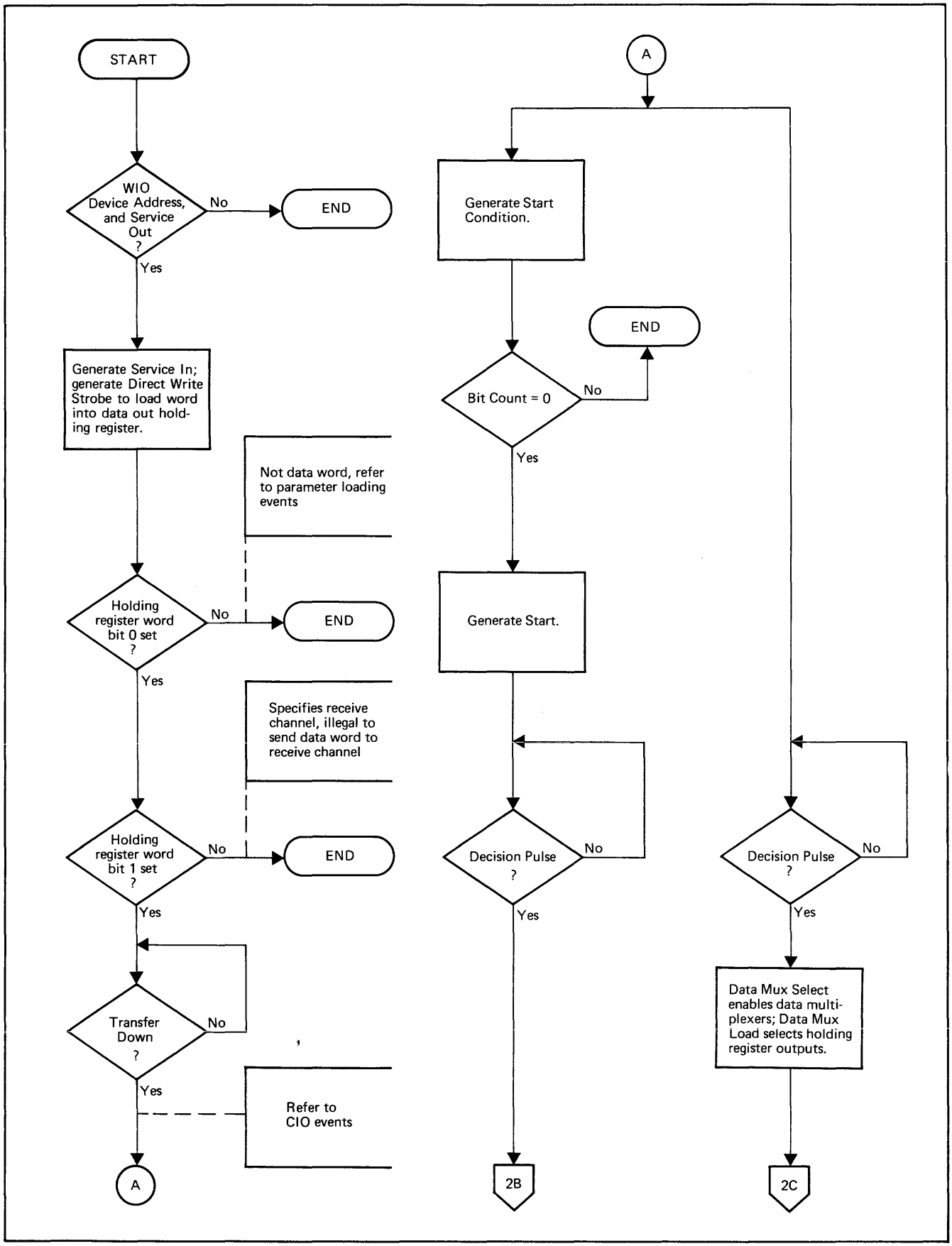
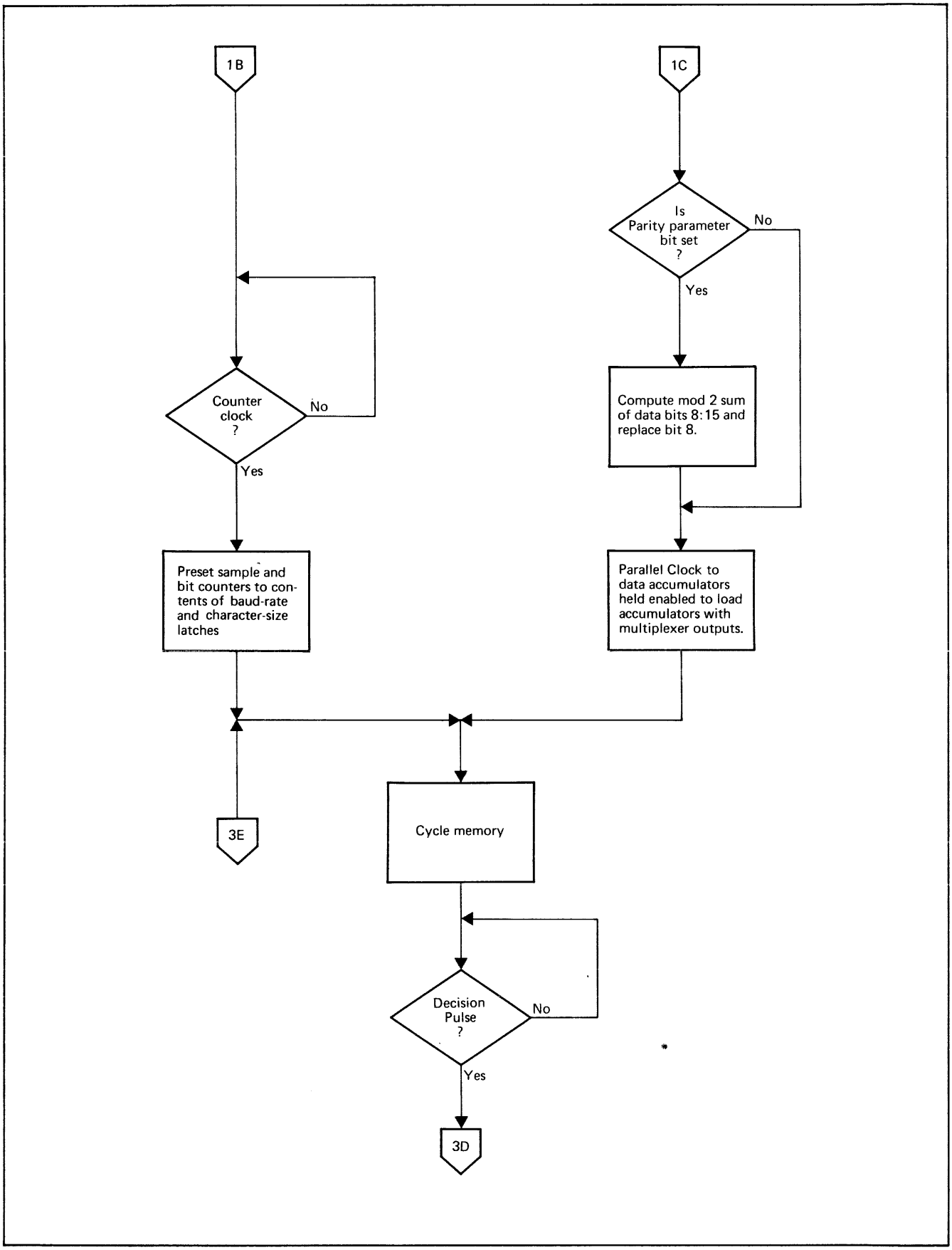


Figure 4-14. TDI Typical Send Operation Timing



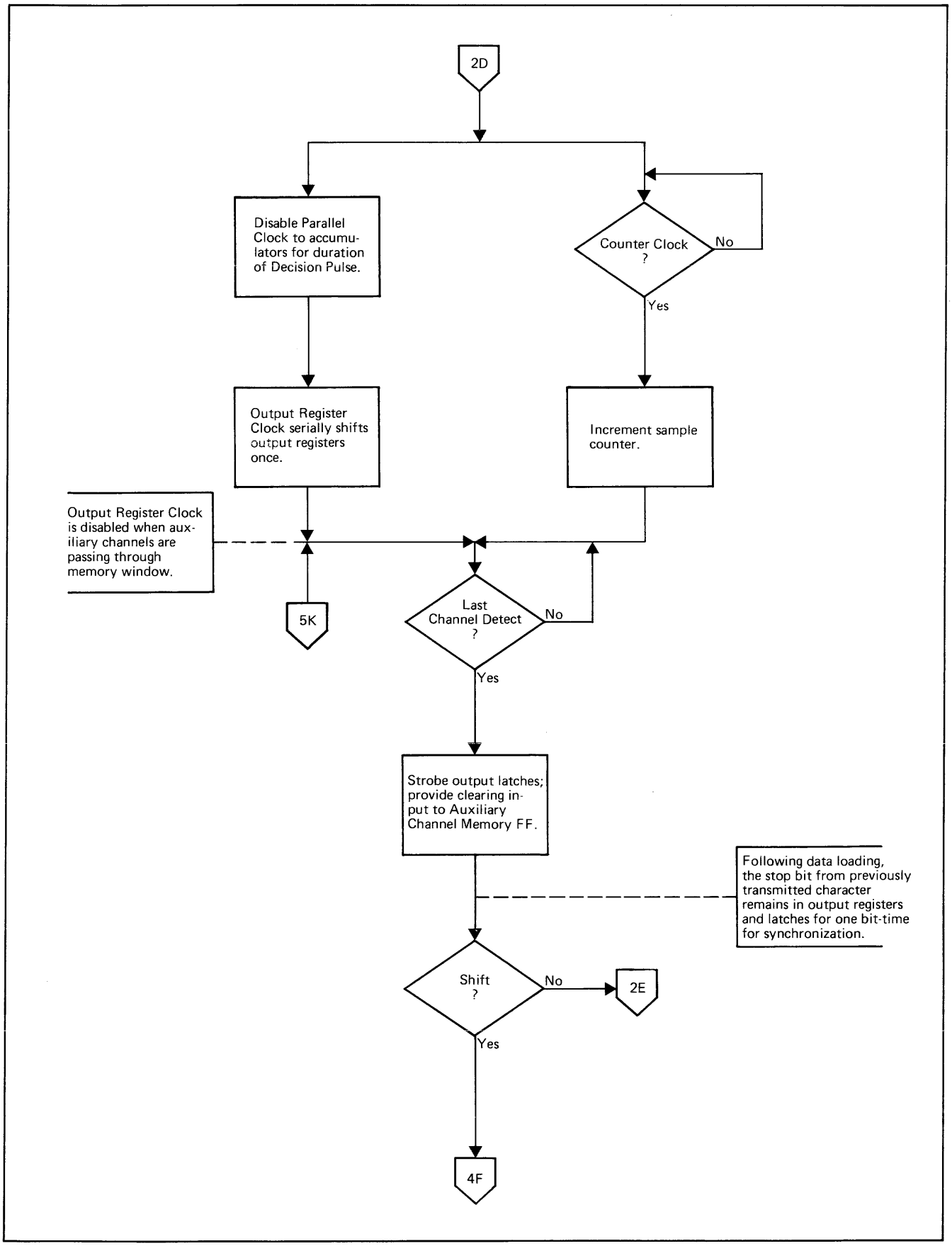
2249-29

Figure 4-15. TDI Send Events Flowchart (Sheet 1 of 6)



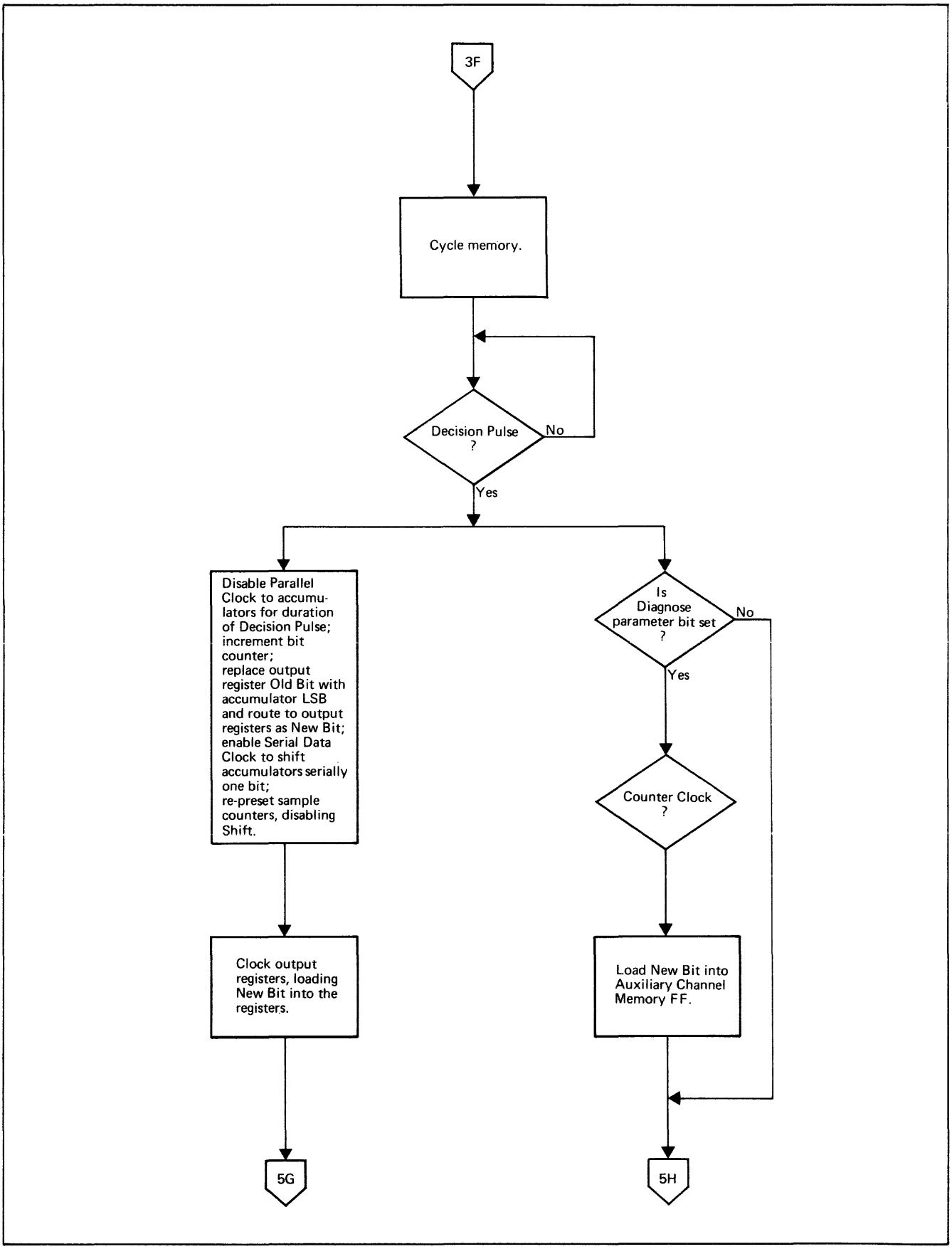
2249-30

Figure 4-15. TDI Send Events Flowchart (Sheet 2 of 6)



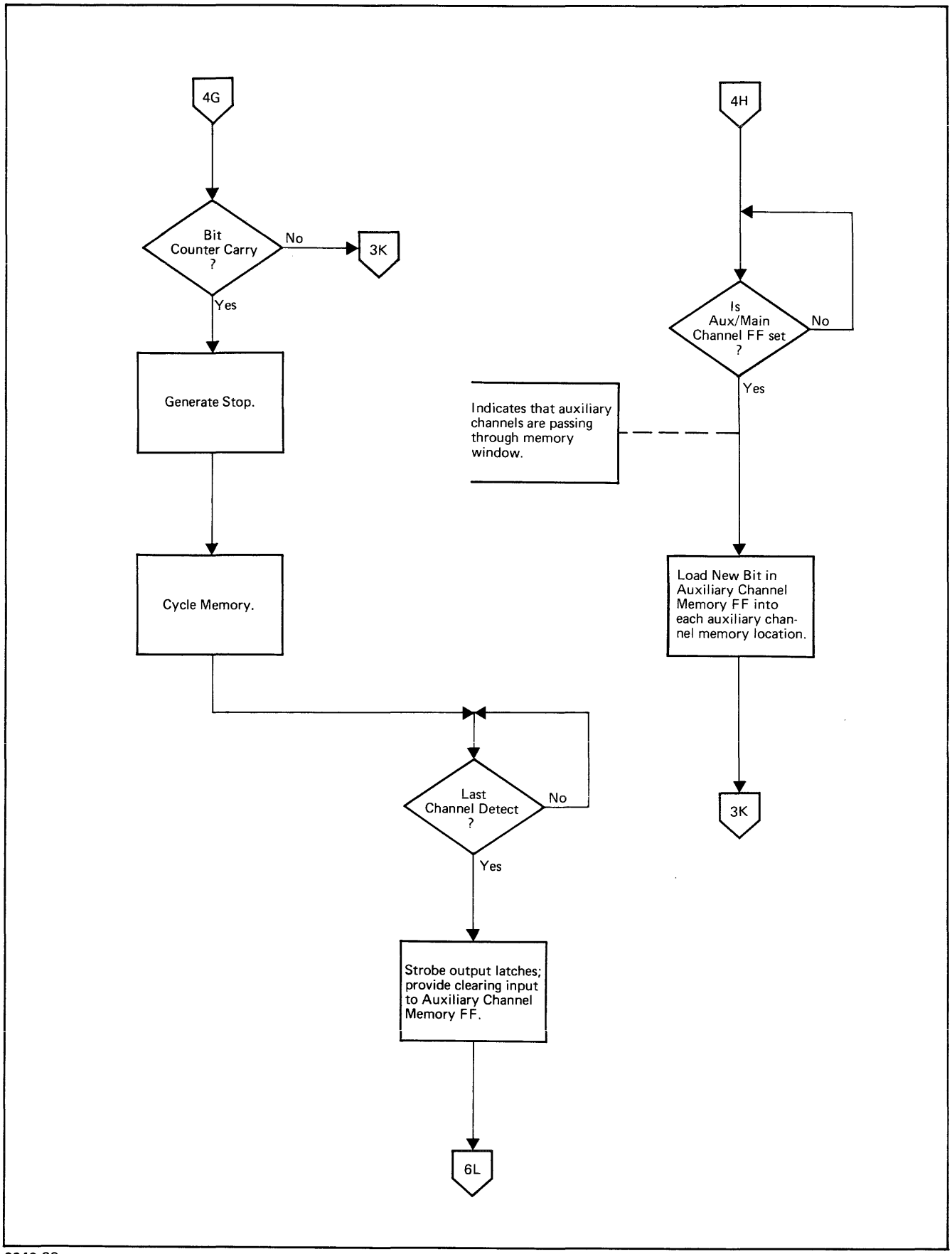
2249-31

Figure 4-15. TDI Send Events Flowchart (Sheet 3 of 6)



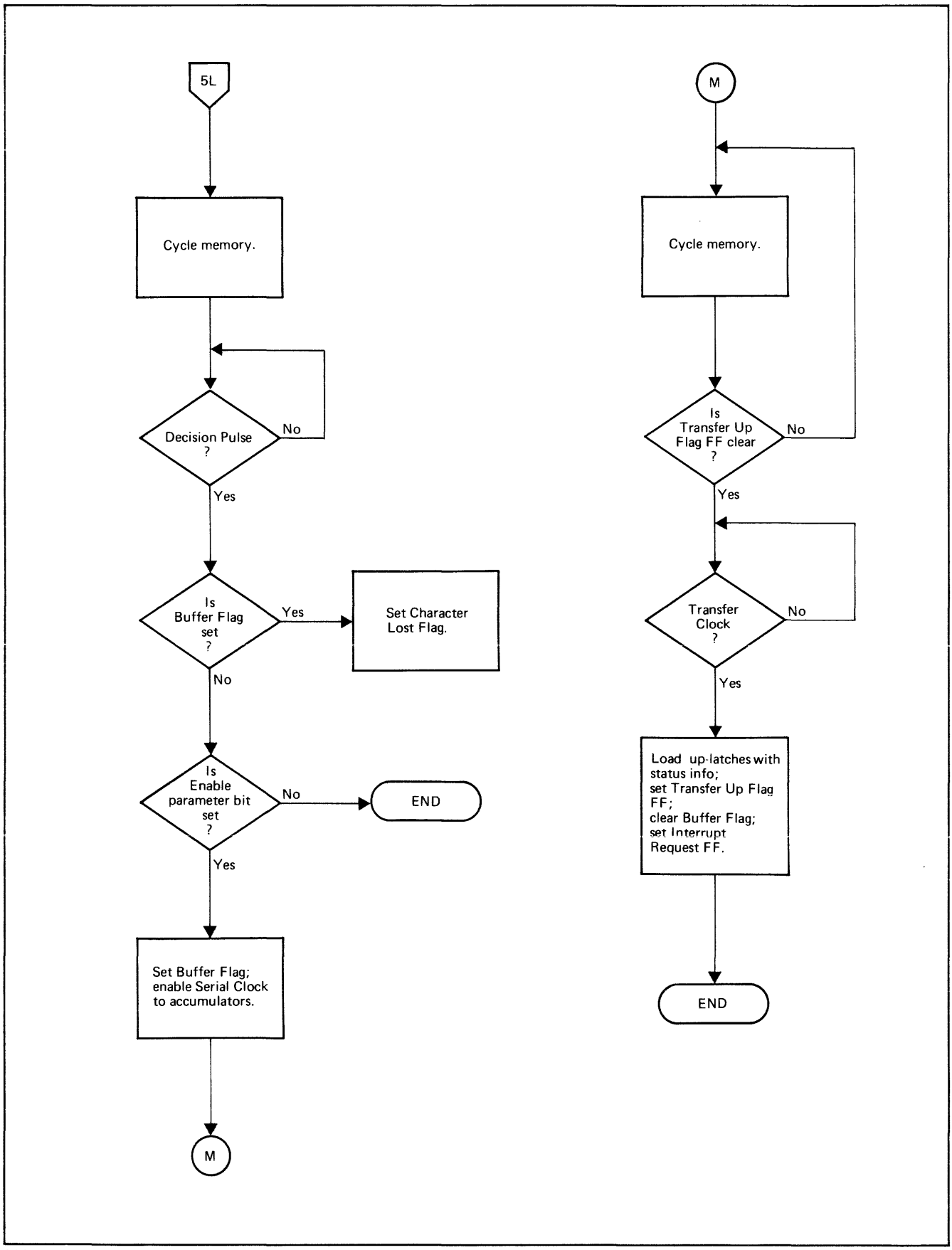
2249-32

Figure 4-15. TDI Send Events Flowchart (Sheet 4 of 6)



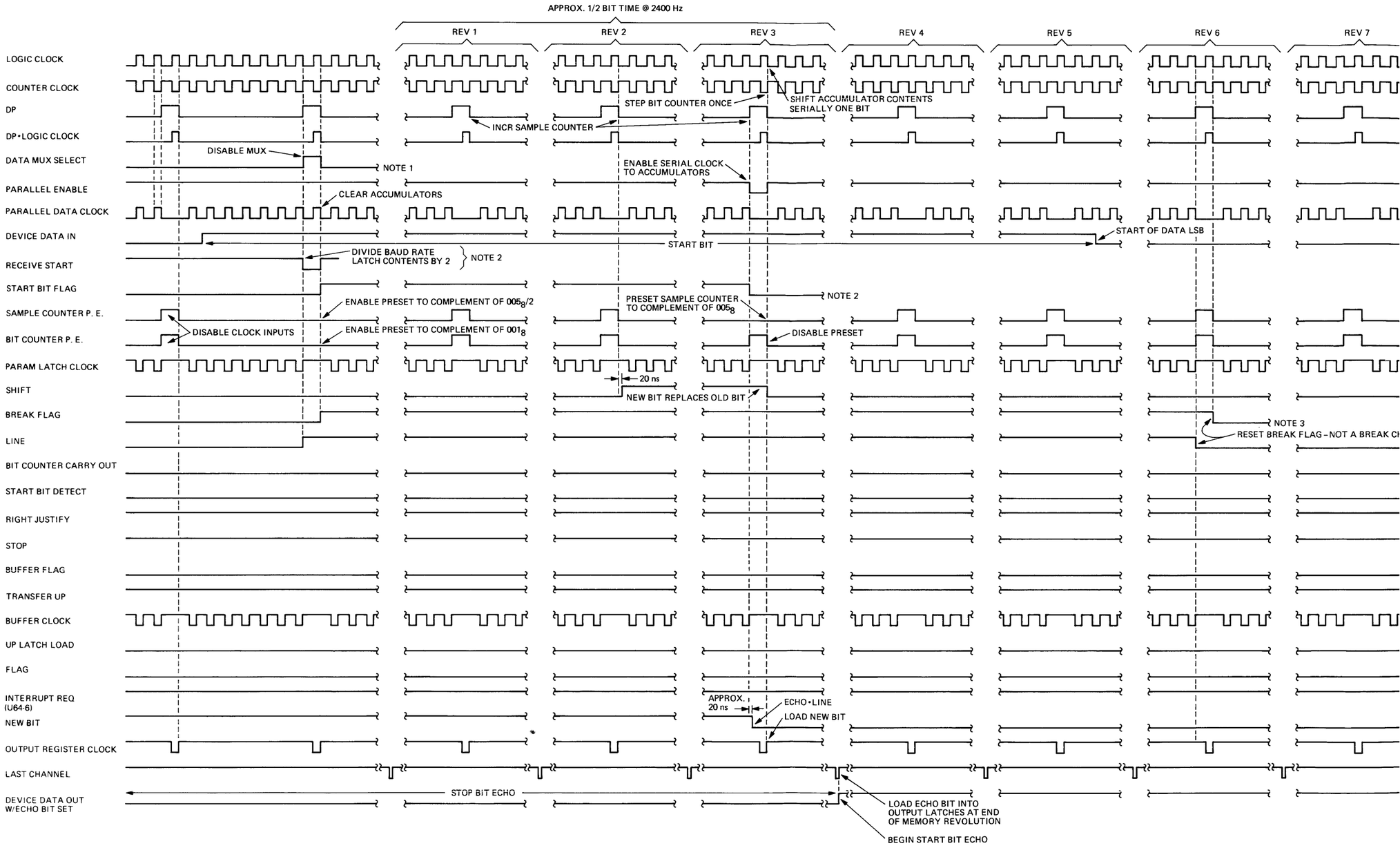
2249-33

Figure 4-15. TDI Send Events Flowchart (Sheet 5 of 6)

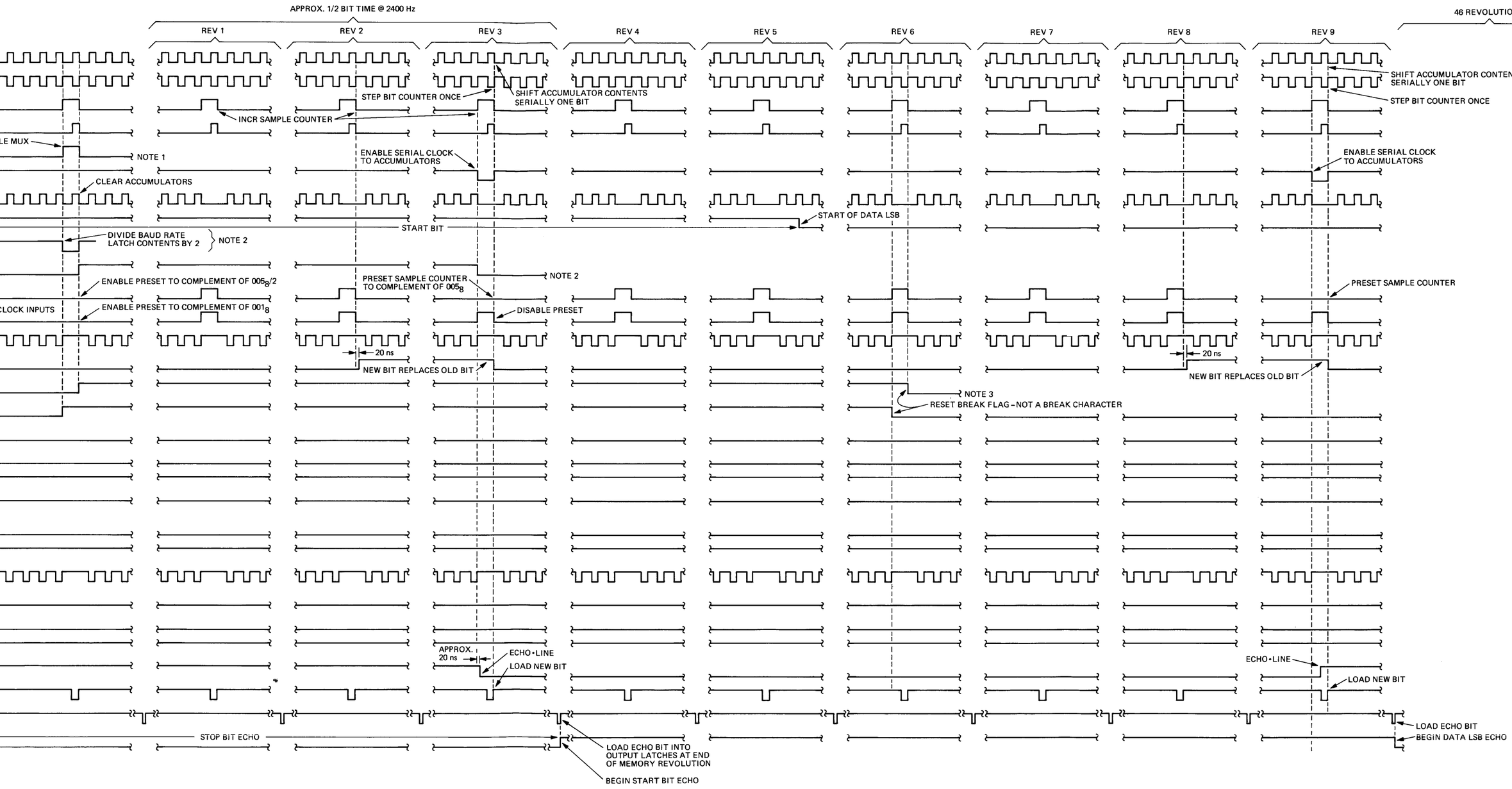


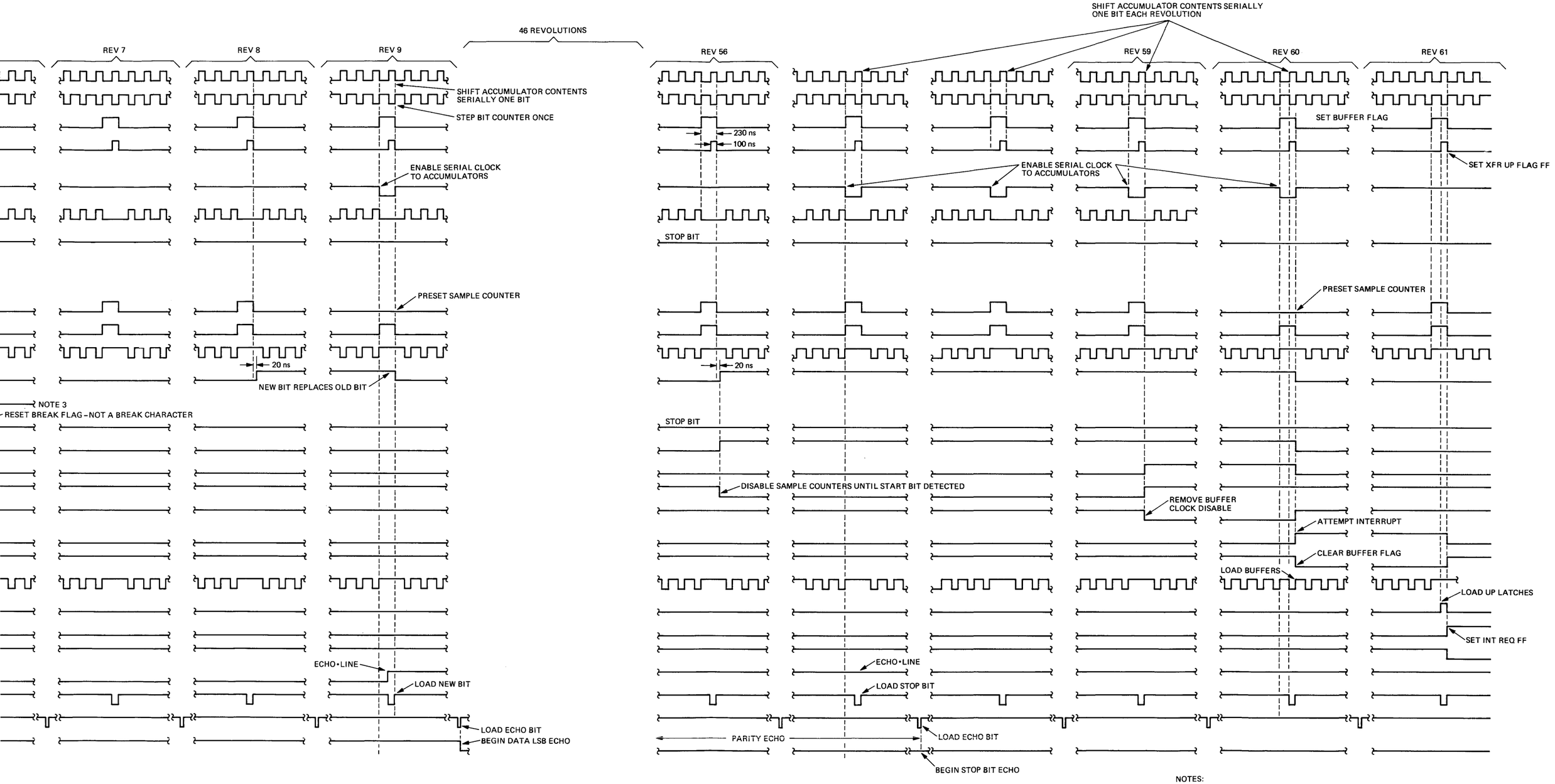
2249-34

Figure 4-15. TDI Send Events Flowchart (Sheet 6 of 6)


APPROX. 1/2 BIT TIME @ 2400 Hz
REV 1
REV 2
REV 3
REV 4
REV 5
REV 6
REV 7
LOGIC CLOCK
COUNTER CLOCK
DP
DP•LOGIC CLOCK
DATA MUX SELECT
PARALLEL ENABLE
PARALLEL DATA CLOCK
DEVICE DATA IN
RECEIVE START
START BIT FLAG
SAMPLE COUNTER P. E.
BIT COUNTER P. E.
PARAM LATCH CLOCK
SHIFT
BREAK FLAG
LINE
BIT COUNTER CARRY OUT
START BIT DETECT
RIGHT JUSTIFY
STOP
BUFFER FLAG
TRANSFER UP
BUFFER CLOCK
UP LATCH LOAD
FLAG
INTERRUPT REQ (U64-6)
NEW BIT
OUTPUT REGISTER CLOCK
LAST CHANNEL
DEVICE DATA OUT W/ECHO BIT SET
STEP BIT COUNTER ONCE
SHIFT ACCUMULATOR CONTENTS SERIALLY ONE BIT
INCR SAMPLE COUNTER
DISABLE MUX
NOTE 1
ENABLE SERIAL CLOCK TO ACCUMULATORS
CLEAR ACCUMULATORS
START OF DATA LSB
START BIT
DIVIDE BAUD RATE LATCH CONTENTS BY 2
NOTE 2
NOTE 2
ENABLE PRESET TO COMPLEMENT OF 005₈/2
PRESET SAMPLE COUNTER TO COMPLEMENT OF 005₈
DISABLE CLOCK INPUTS
ENABLE PRESET TO COMPLEMENT OF 001₈
DISABLE PRESET
20 ns
NEW BIT REPLACES OLD BIT
NOTE 3
RESET BREAK FLAG - NOT A BREAK CH
APPROX. 20 ns
ECHO•LINE
LOAD NEW BIT
STOP BIT ECHO
LOAD ECHO BIT INTO OUTPUT LATCHES AT END OF MEMORY REVOLUTION
BEGIN START BIT ECHO

2249-8

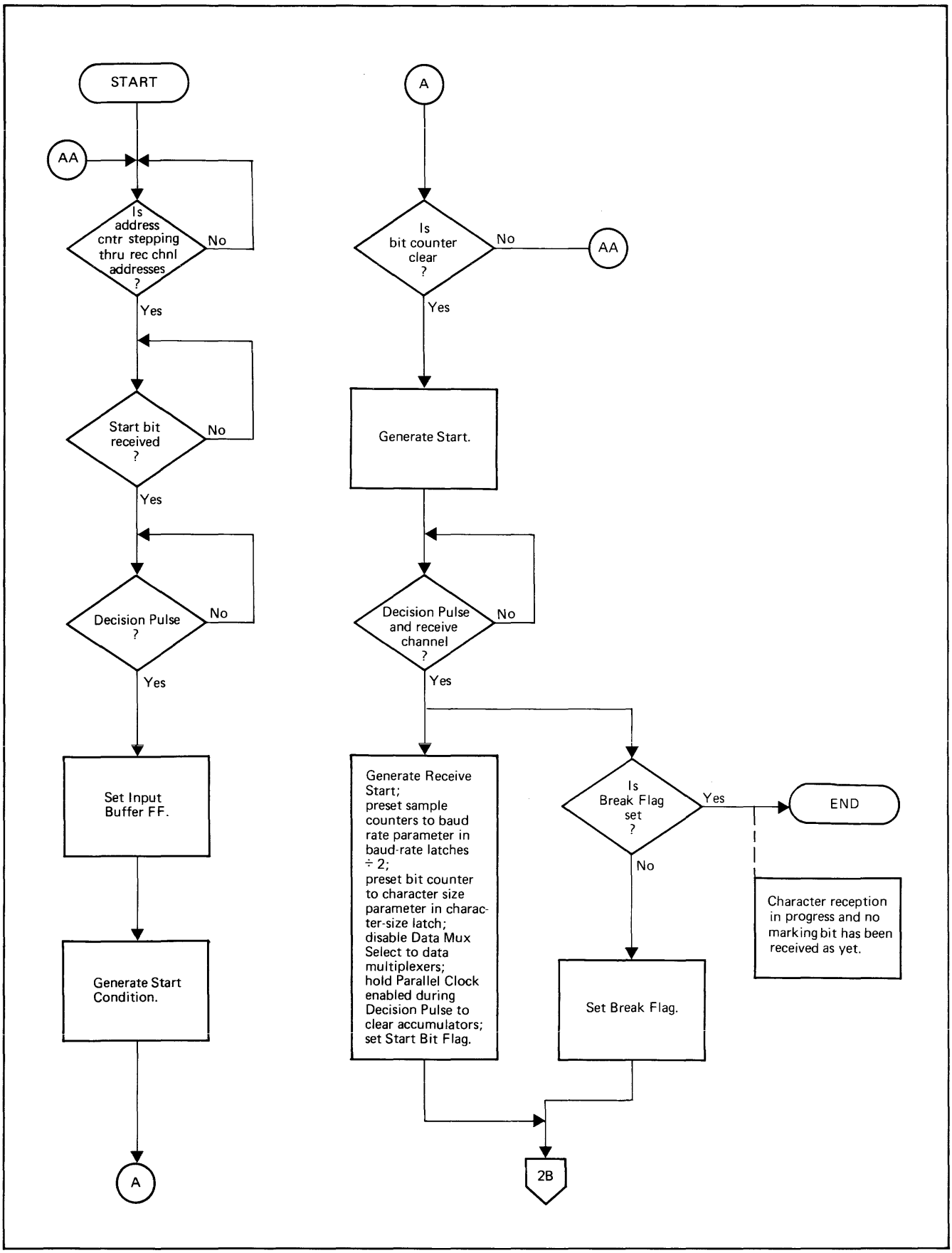

APPROX. 1/2 BIT TIME @ 2400 Hz
46 REVOLUTIONS
REV 1
REV 2
REV 3
REV 4
REV 5
REV 6
REV 7
REV 8
REV 9
STEP BIT COUNTER ONCE
SHIFT ACCUMULATOR CONTENTS SERIALLY ONE BIT
INCR SAMPLE COUNTER
LE MUX
NOTE 1
ENABLE SERIAL CLOCK TO ACCUMULATORS
CLEAR ACCUMULATORS
START OF DATA LSB
START BIT
STOP BIT
DIVIDE BAUD RATE LATCH CONTENTS BY 2
NOTE 2
ENABLE PRESET TO COMPLEMENT OF $005_8/2$
PRESET SAMPLE COUNTER TO COMPLEMENT OF 005_8
NOTE 2
CLOCK INPUTS
ENABLE PRESET TO COMPLEMENT OF 001_8
DISABLE PRESET
PRESET SAMPLE COUNTER
20 ns
NEW BIT REPLACES OLD BIT
NOTE 3
RESET BREAK FLAG - NOT A BREAK CHARACTER
STOP BIT
APPROX. 20 ns
ECHO • LINE
LOAD NEW BIT
STOP BIT ECHO
LOAD ECHO BIT INTO OUTPUT LATCHES AT END OF MEMORY REVOLUTION
BEGIN START BIT ECHO
LOAD ECHO BIT
BEGIN DATA LSB ECHO



NOTES:

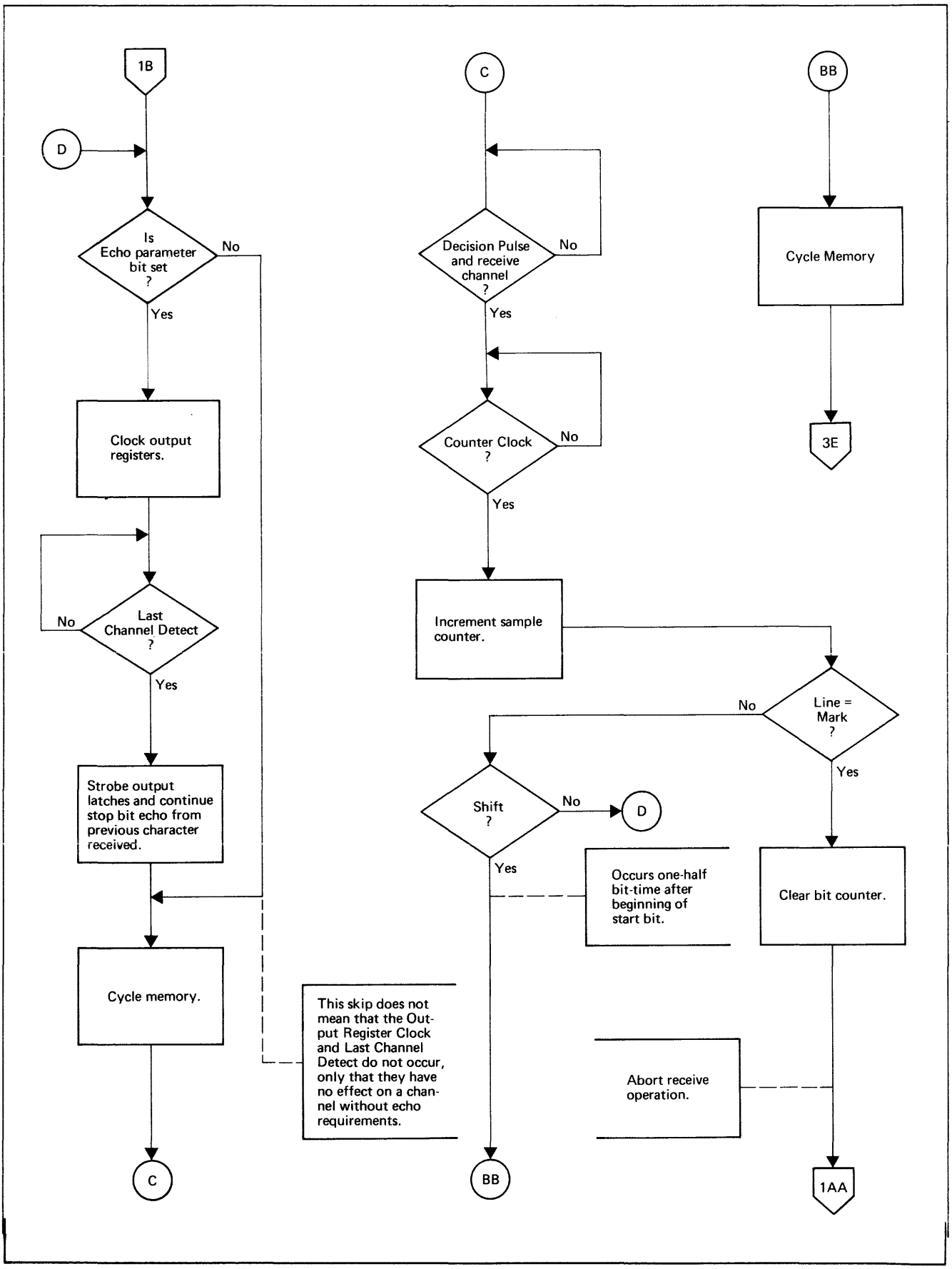
1. DATA MUX SELECT OCCURS ONLY ONCE AT THE START OF EACH CHARACTER RECEPTION.
2. BAUD RATE IS DIVIDED BY 2 ONLY FOR THE FIRST BIT (START BIT) RECEIVED. THIS IS DONE TO CAUSE BIT SAMPLING MID-BIT RATHER THAN ON EITHER BIT EDGE TO ELIMINATE POSSIBILITY OF NOISE SPIKE BEING LOADED INTO ACCUMULATORS AS A LOGIC 1.
3. BREAK FLAG IS RESET WHEN A MARKING BIT IS FOUND IN A CHARACTER BEING RECEIVED: A BREAK CHARACTER HAS NO MARKING BITS.

Figure 4-16. TDI Typical Receive Operation Timing



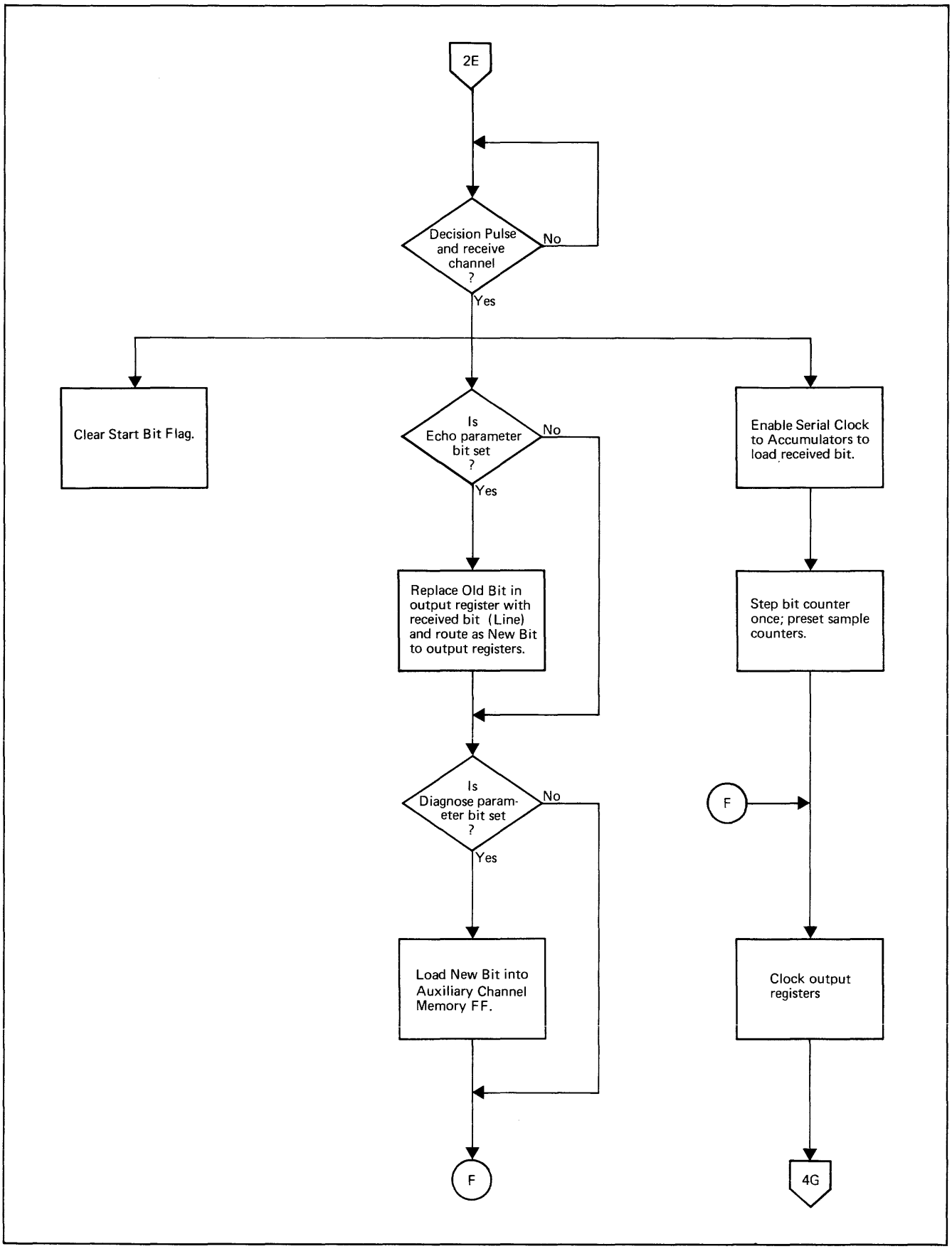
2249-35

Figure 4-17. TDI Receive Events Flowchart (Sheet 1 of 9)



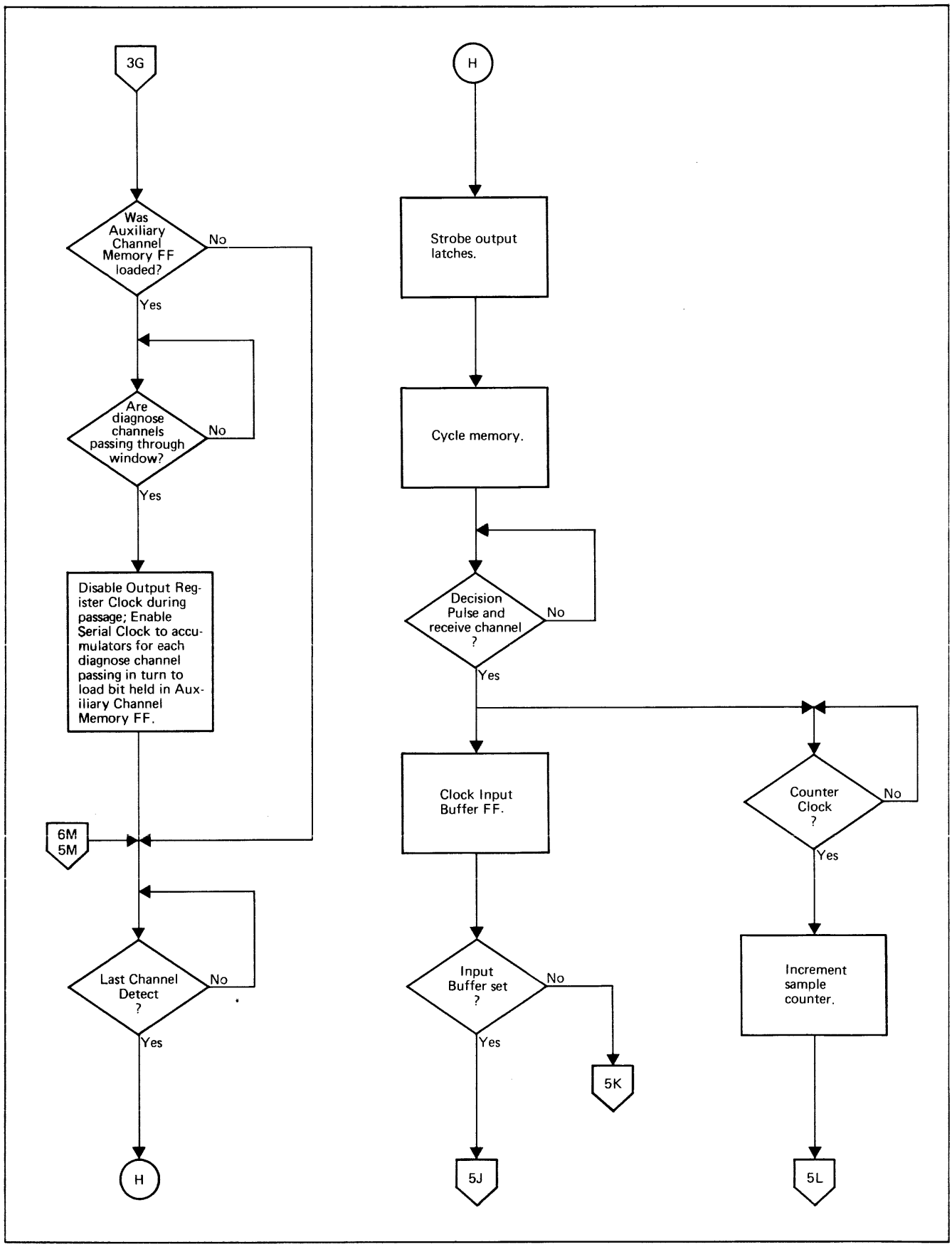
2249-36

Figure 4-17. TDI Receive Events Flowchart (Sheet 2 of 9)



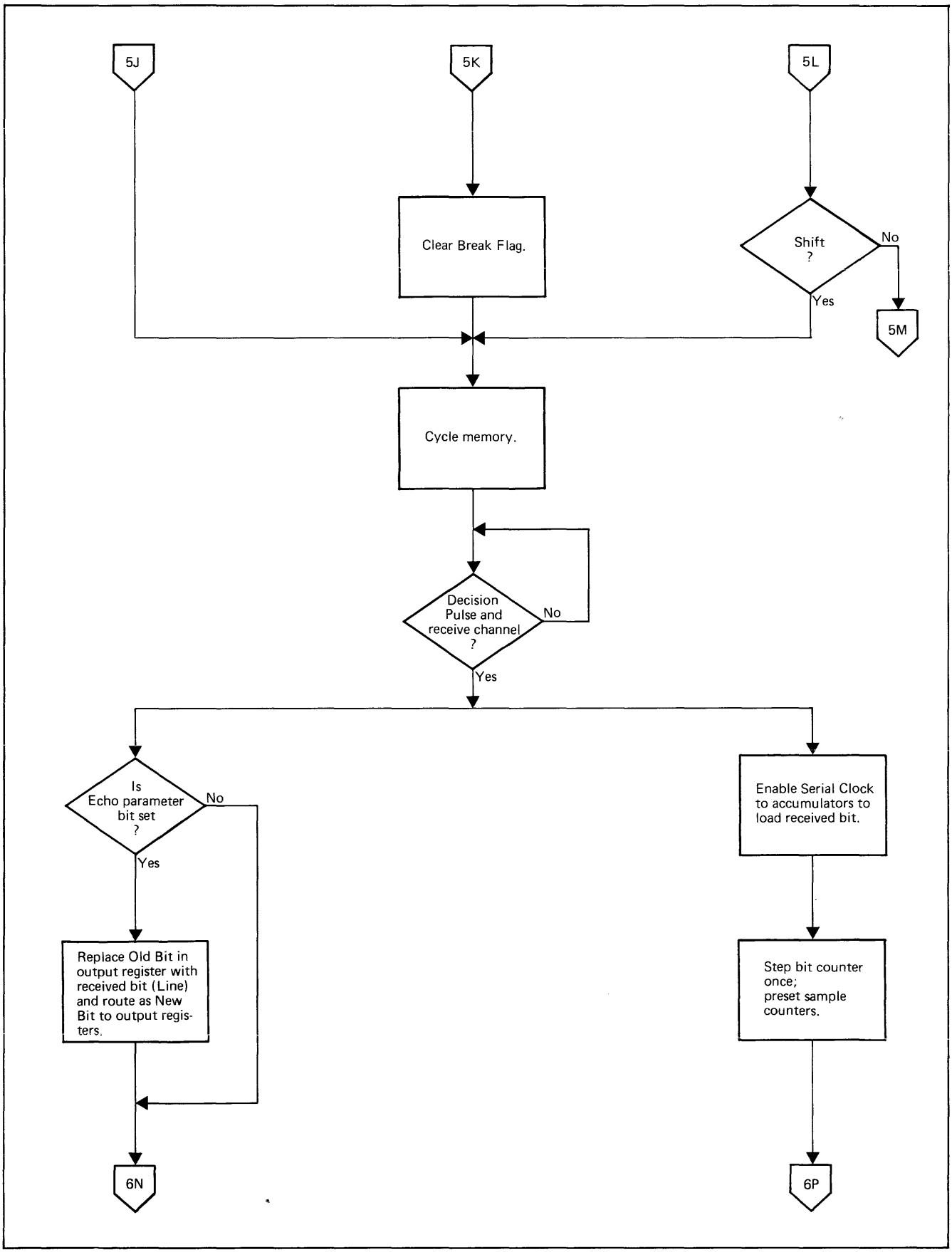
2249-37

Figure 4-17. TDI Receive Events Flowchart (Sheet 3 of 9)



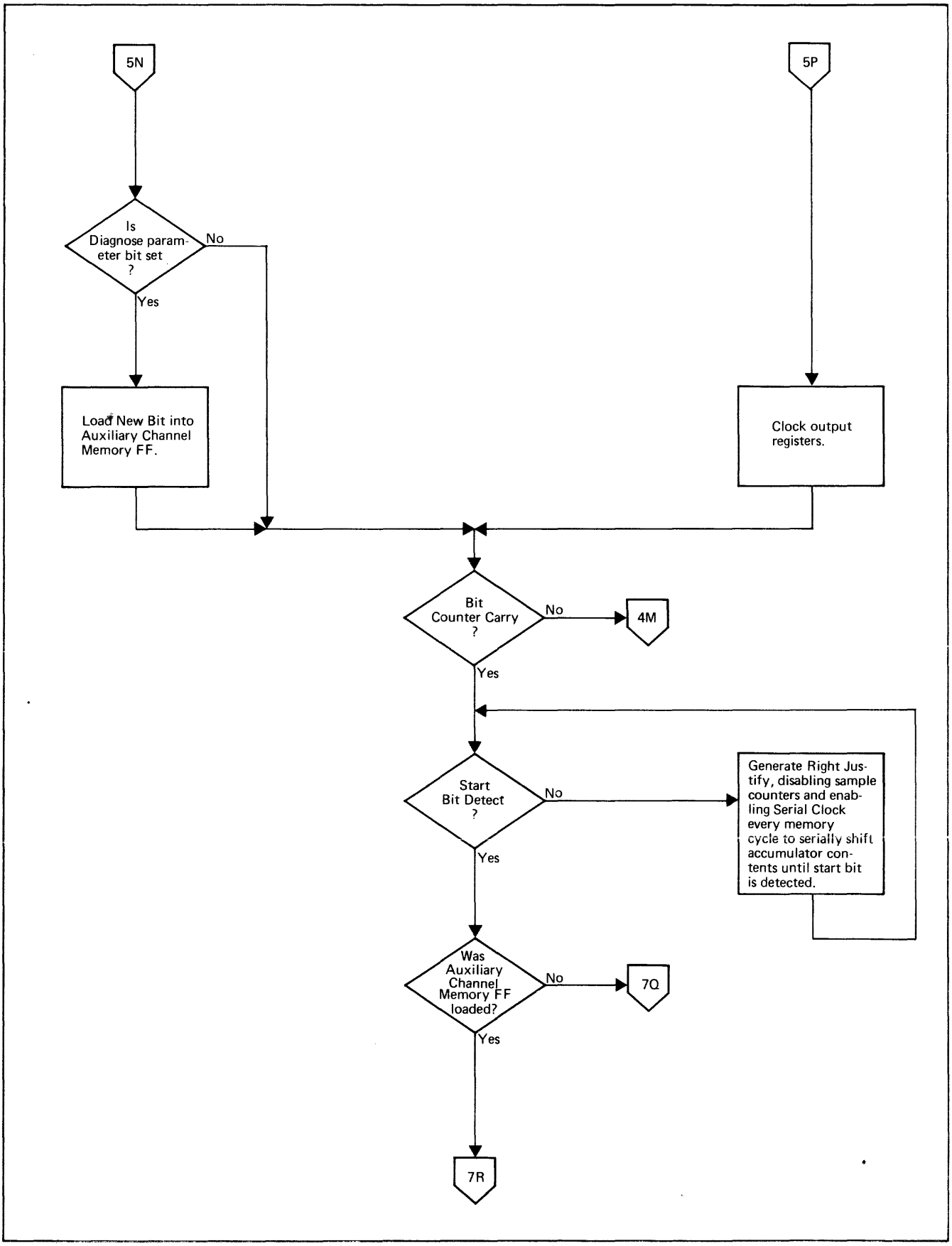
2249-38

Figure 4-17. TDI Receive Events Flowchart (Sheet 4 of 9)



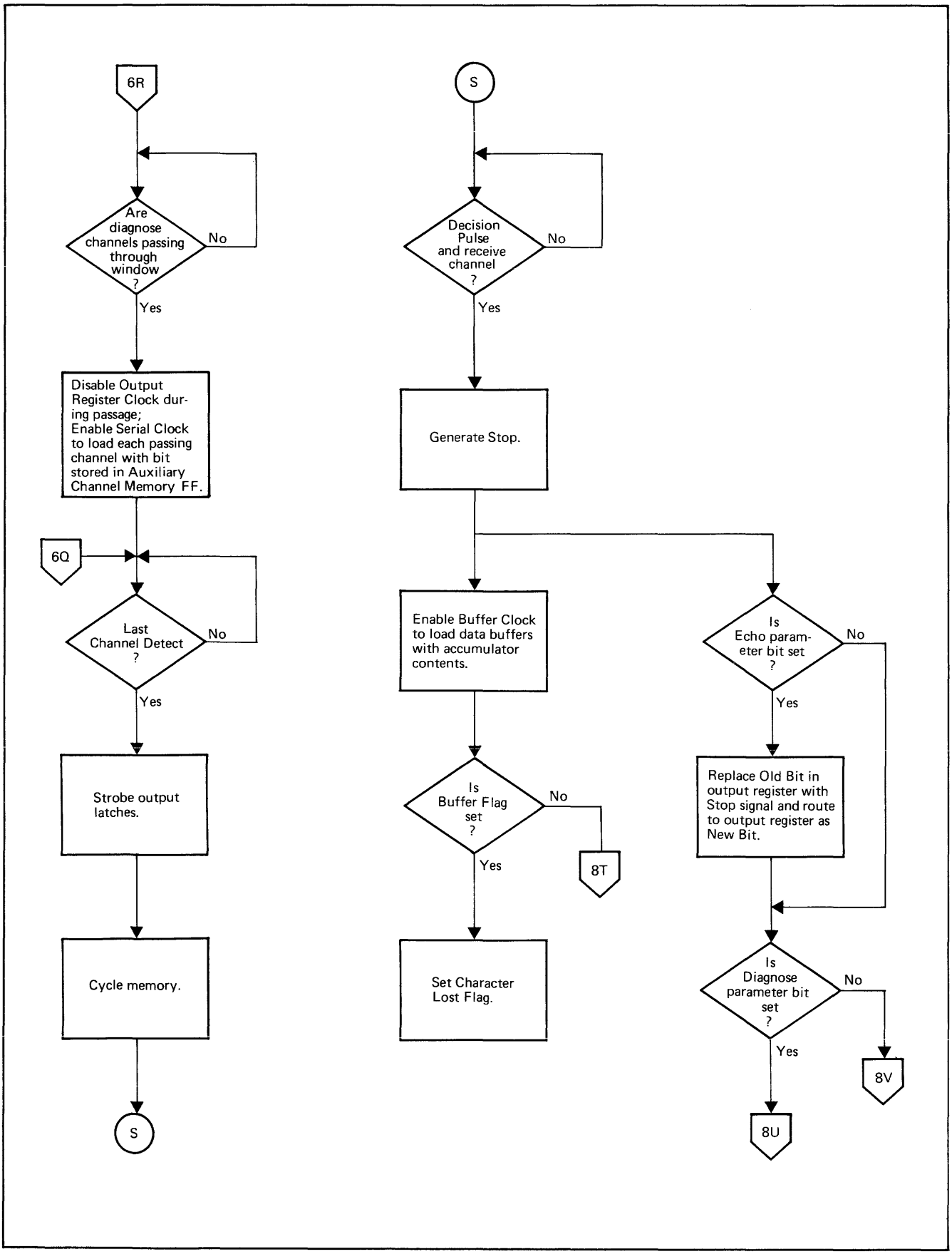
2249-39

Figure 4-17. TDI Receive Events Flowchart (Sheet 5 of 9)



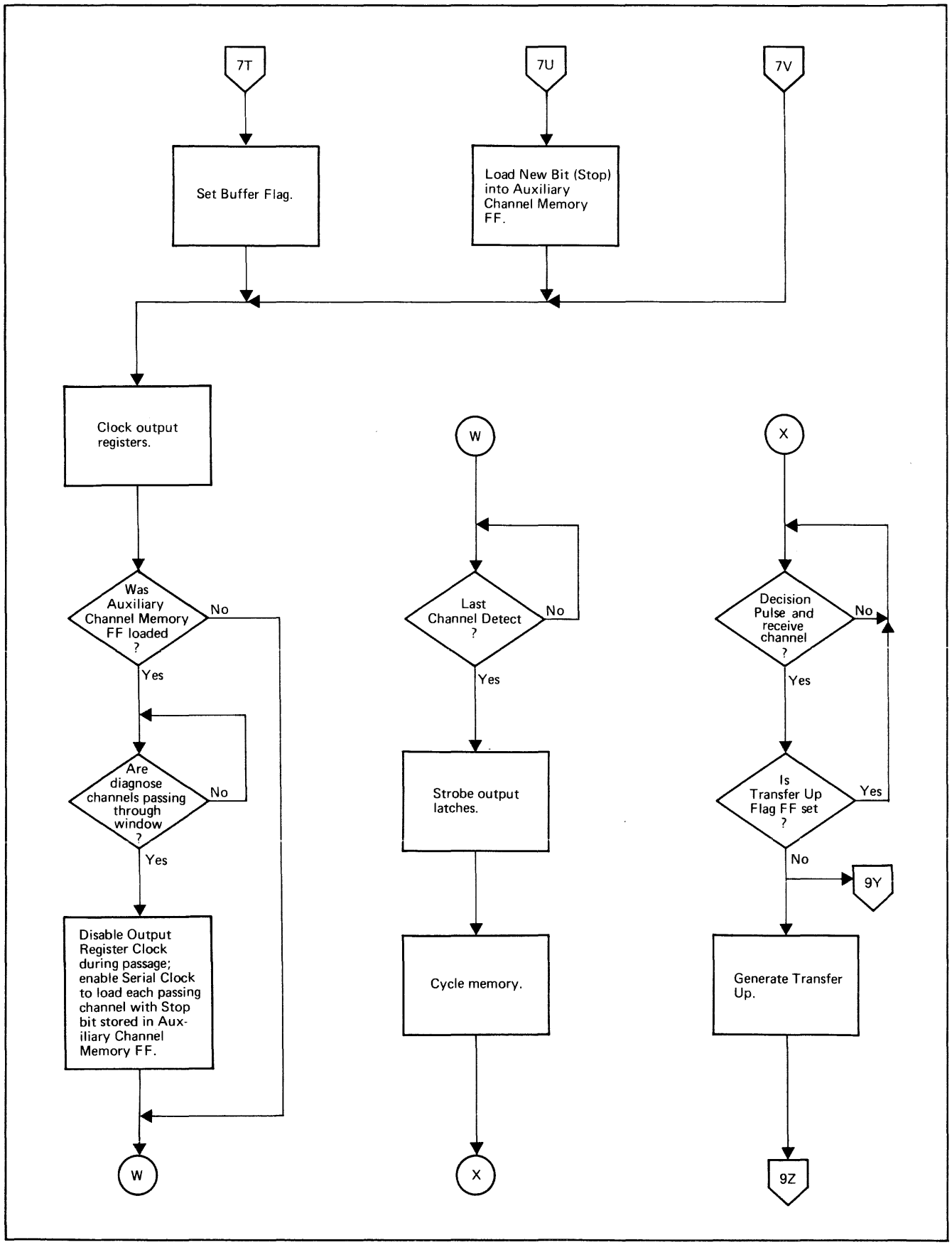
2249-40

Figure 4-17. TDI Receive Events Flowchart (Sheet 6 of 9)



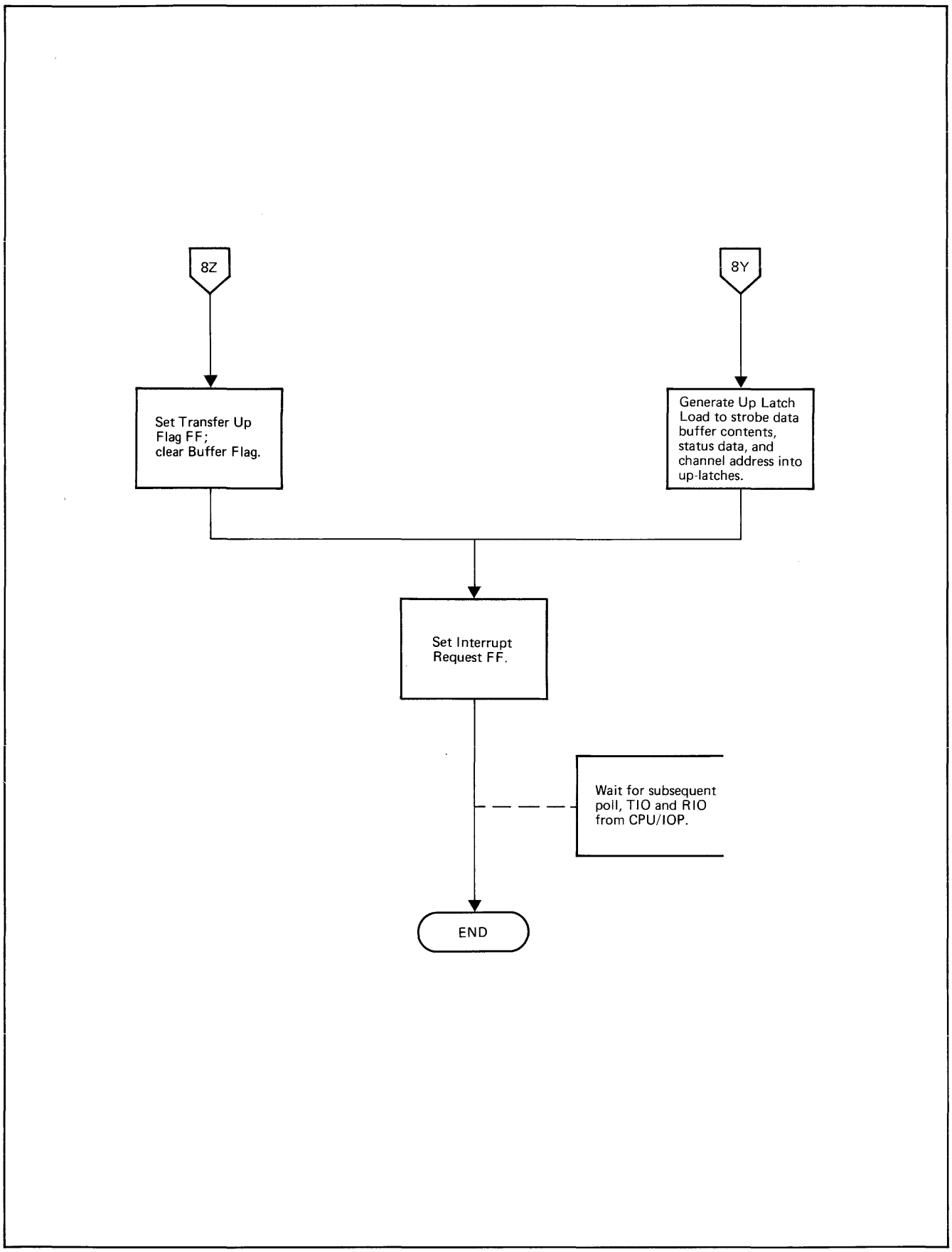
2249-41

Figure 4-17. TDI Receive Events Flowchart (Sheet 7 of 9)



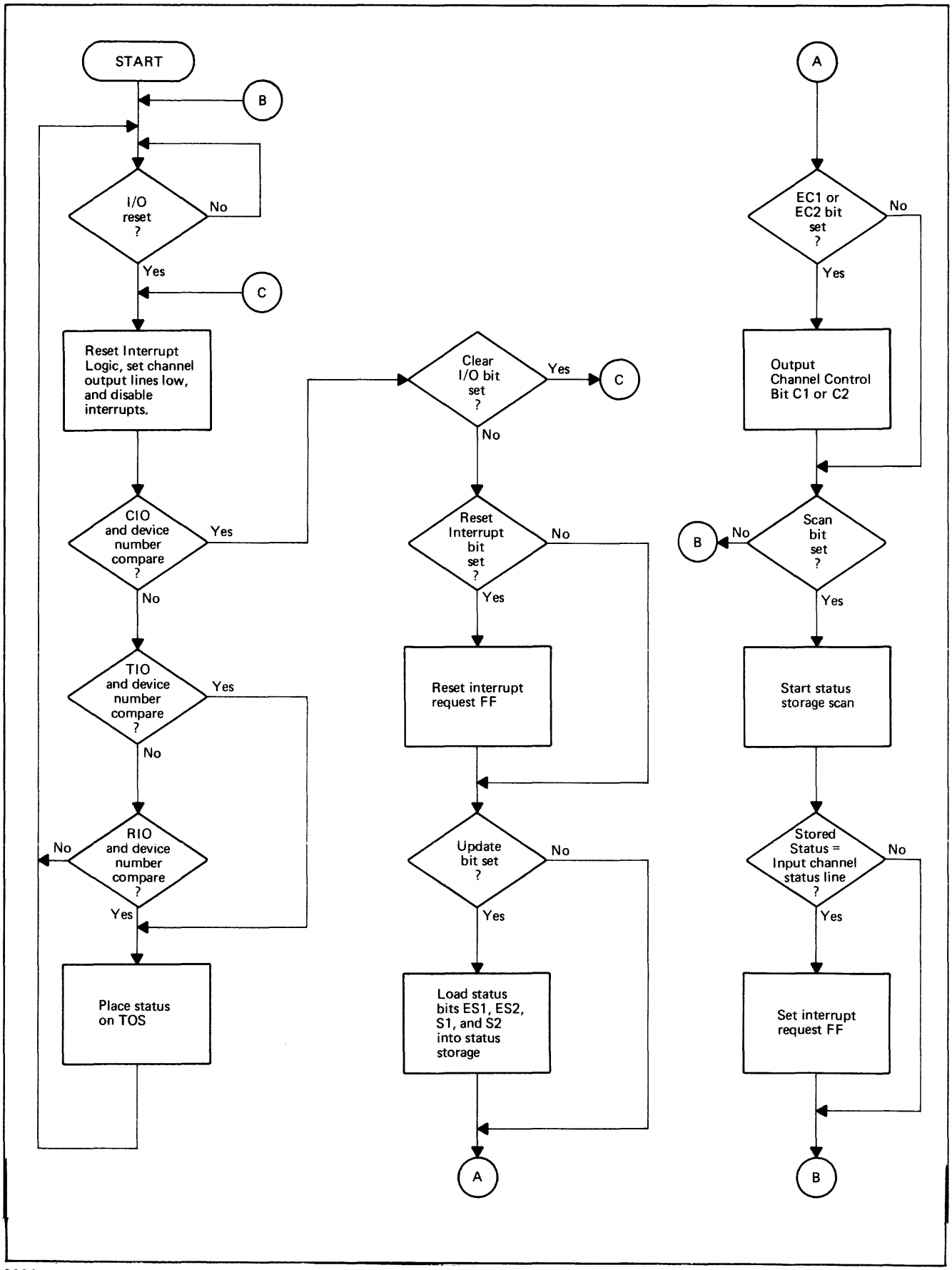
2249-42

Figure 4-17. TDI Receive Events Flowchart (Sheet 8 of 9)



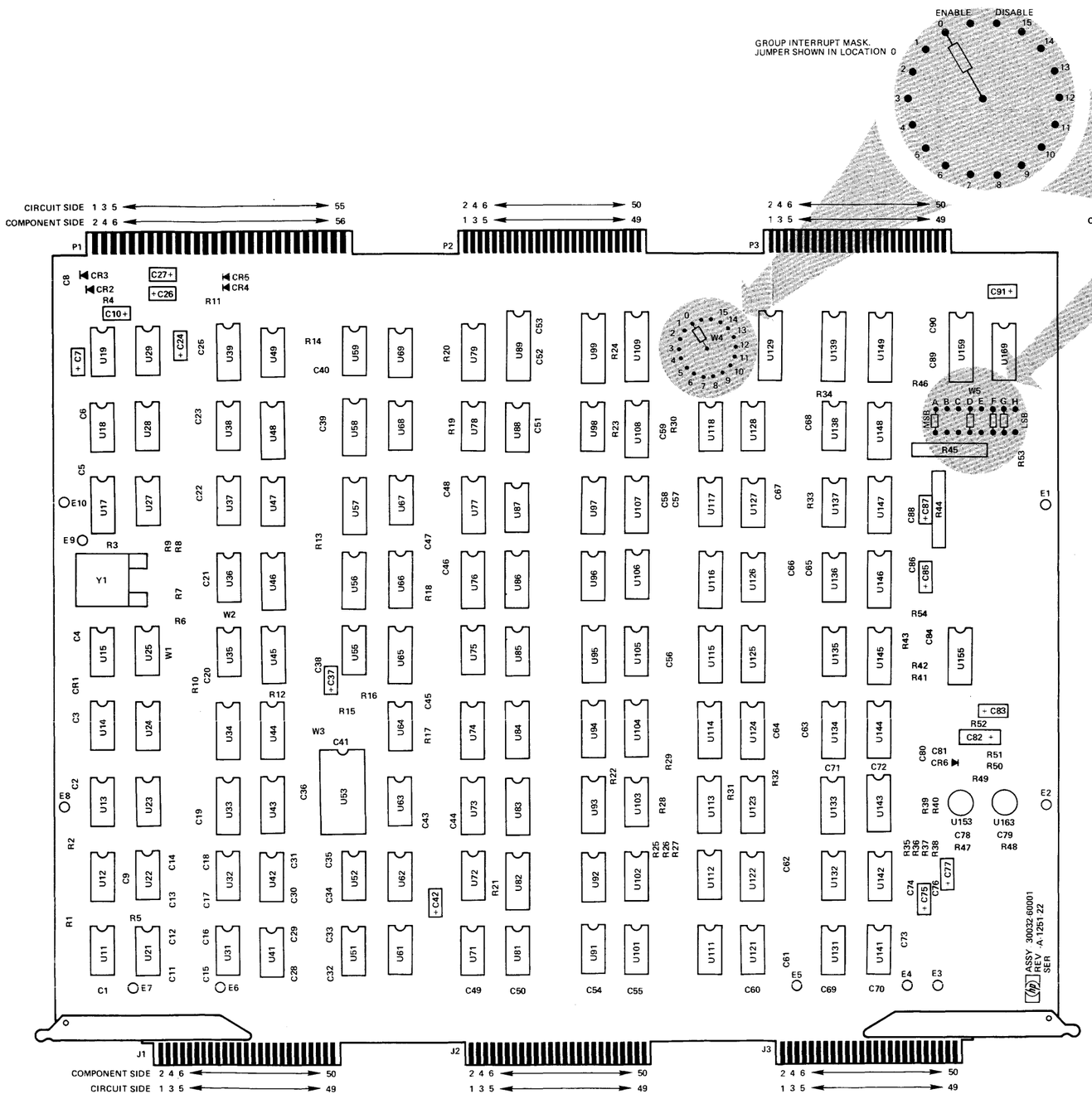
2249-43

Figure 4-17. TDI Receive Events Flowchart (Sheet 9 of 9)



2206-18

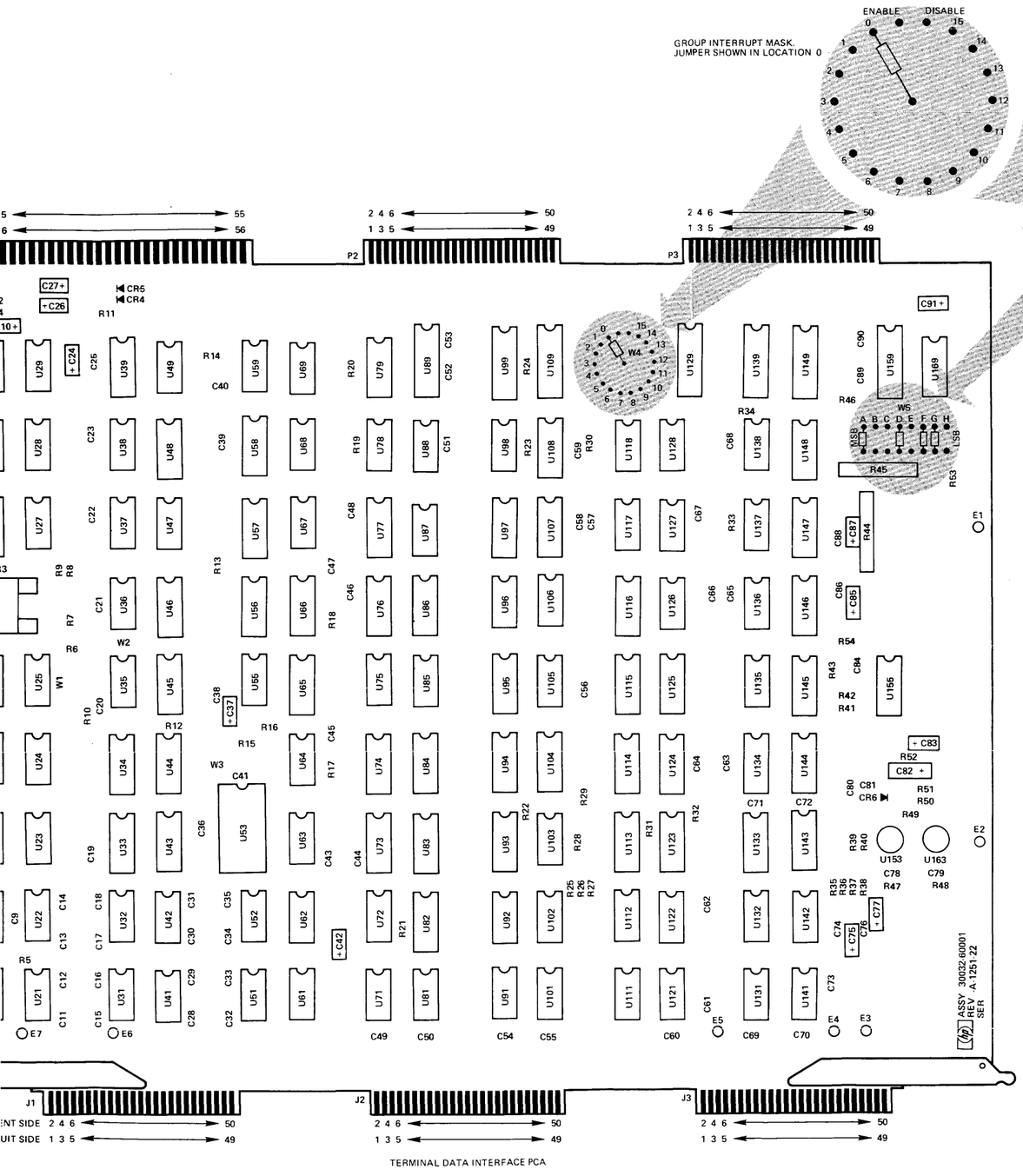
Figure 4-18. TCI Operational Flowchart



7063-13

TERMINAL DATA INTERFACE PCA

TERMINAL CONTROL INTERFACE PCA



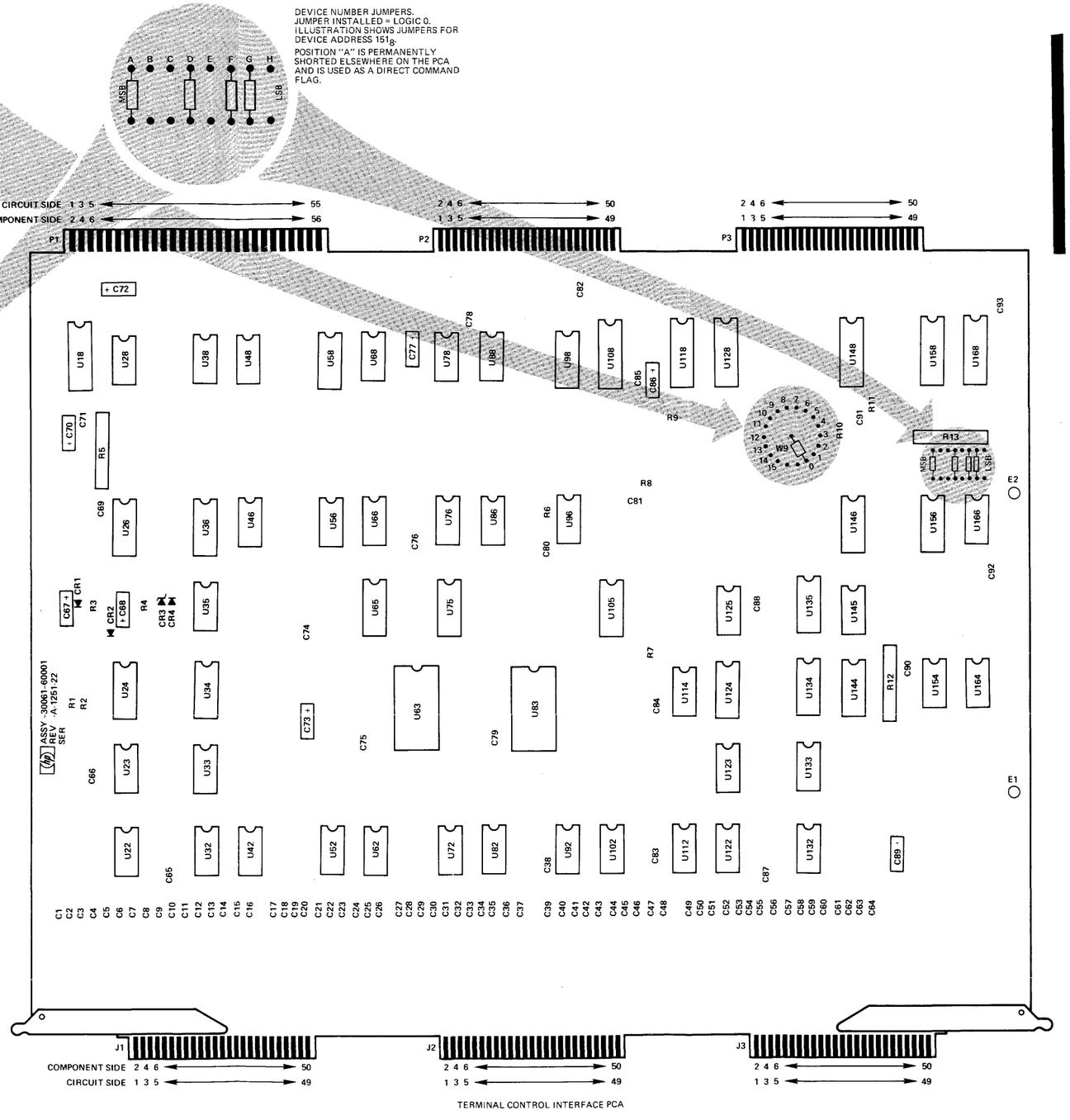


Figure 4-19. TDI and TCI Jumper Locations

5-1. PCA LOCATION.

5-2. In the Series II Computer System, memory occupies slots A4 through A10 of the CPU bay card cage No. 1. This left slots A1 through A3 available for device controllers capable of operating under control of direct I/O. Slot A1 was therefore reserved for the terminal data interface PCA and slots A2 and A3 are usually reserved for the optional terminal control interface PCAs.

5-3. A system may have as many as four HP 30032B Asynchronous Terminal Controllers. The first, as just described, occupies reserved PCA slot space in card cage No. 2. Any additional slots used for installation of optional controllers must have the IOP bus available to P3 of the PCAs. For the Models 5 and 7, this would be any available slots in card cages 4 and 7. For the Model 9, use the available slots of any I/O bay card cage.

5-4. CONNECTOR PANEL LOCATION.

5-5. The first connector panel is mounted just above the power control module on the rear of the CPU bay. The space above the power distribution unit in the I/O bay will accommodate another. The remaining two panels of a 4-panel system are located behind the magnetic tape unit of the first peripheral bay.

5-6. CABLING.

5-7. Terminal data connector cable 30060-60003 connects from J1 of the terminal data interface PCA to J18 of the connector panel. If the first terminal control interface PCA is present, terminal control connector cable 30061-60003 connects from J1 and J2 to J16 and J20 of the connector panel. The connector marked J16/J17 goes to J16; the connector marked J19/J20 goes to J20. If the second terminal control interface PCA is present, a second terminal control connector cable 30061-60003 connects from J1 and J2 to J17 and J19 of the connector panel. The connector marked J16/J17 goes to J17; the connector marked J19/J20 goes to J19.

5-8. Cabling from J0 to the system console is with cable 30062D installed by the customer engineer. Cabling from J1 through J15 of the first connector panel and from J0 through J15 of any additional connector panels to terminals and modems is a customer task. The User's Terminal Cabling Guide (part No. 30062-90002) provides the customer with suggested cabling methods and associated information.

5-9. INTERRUPT POLLING.

5-10. The interrupt polling sequence of devices is described in the Signal and Power Distribution Manual (30000-90021) and in the System Installation Manual (30000-90019). The terminal data interface PCAs are polled first. They are polled one at a time as a group. Similarly when multiple terminal control interface PCAs are polled, they are polled as a group in the sequence.

5-11. I/O CONFIGURATION.

5-12. In the standard Series II system, the terminal data interface is configured device number 7, the first terminal control interface is device number 8, and the second terminal control interface is device number 9. The 16 ports are configured logical devices 20 through 35. Port 0 is the system console's port. Device number jumpers on the three PCAs are set to reflect these configured device numbers.

5-13. Also in standard systems, a second terminal data interface is configured device number 10, its first terminal control interface is device number 11, and its second terminal control interface is device number 12. The 16 ports are configured logical devices 36 through 51. If device number jumpers are positioned on the PCAs the terminals are already configured when the hardware is installed.

5-14. Any additional asynchronous terminal controllers must be configured during the I/O configuration phase of system generation.