HP 12968A Asynchronous Communications Interface

Reference Manual

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PREFACE

This manual describes the Hewlett-Packard 12968A Asynchronous Communications Interface and provides installation instructions and programming information.

We assume that you are using this manual to code driver subroutines for this interface kit. You should know the following:

- HP 2100 Assembler Language programming, especially I/O programming, including interrupt and direct memory access (DMA) or dual channel port controller (DCPC) operations. Refer to the *HP Assembler Reference Manual*, part no. 24307-90014, for information.
- Computer data communications concepts.
- Your application, system organization, line protocol, and data communications equipment operation.

You will find useful information in the following publications:

- *HP Assembler Reference Manual*, part no. 24307-90014. (HP Assembler is the language you use to code the driver.)
- *HP Data Communications Training Manual*, part no. 22999-90010. (This training manual presents the basic concepts of synchronous and asynchronous data communications.)
- *HP Data Communications Modems Training Manual*, part no. 22999-90013. (This training manual presents the concepts of data communications modems.)
- *Data Sets 103A3, 103E, 103G, and 103H Interface Specification; Bell System Data Communications Technical Reference*, publication no. 41102, October 1973. (This publication gives you information on the data set interface requirements.)
- *Data Set 113A Interface Specification; Bell System Data Communications Technical Reference*, publication no. 41104, August 1973. (This publication gives you information on the data set interface requirements.)
- *Data Sets 202C and 202D Interface Specification; Bell System Data Communications Technical Reference*, publication no. 41202, May 1964. (This publication gives you information on the data set interface requirements.)
- *EIA Standard RS-232-C: Interface Between Data Terminal Equipment and Data Communications Equipment Employing Serial Binary Data Interchange* August 1969. (This publication describes the function of the control and status lines used in data communications and line protocol.)
- Martin, James. *Telecommunications and the Computer.* Englewood Cliffs: Prentice-Hall, Inc., 1969. (This text gives a description of the world's telecommunications links and their uses for data transmission.)

- Martin, James. *Teleprocessing Network Organization.* Englewood Cliffs: Prentice-Hall, Inc., 1970. (This text explains the many types of devices and procedures for controlling and organizing the flow of data on telecommunications lines.)

This manual is arranged in four sections. Section I describes the features of the 12968A and its specifications. Section II presents an overview of the principles of operation. Section III provides driver programming information. Section IV contains installation and checkout instructions.

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INTRODUCING THE HP 12968A

SECTION I

The HP 12968A Asynchronous Communications Interface is a hardware interface kit that provides half-duplex, asynchronous bit-serial data transfer between the CPU (HP 2116, HP 2100, or HP 21MX Computer) and asynchronous data sets or terminals which comply with Electronic Industries Association Standard RS-232-C.

The interface kit and its options provide cabling to HP 2600, HP 2615, and HP 2640 Terminals, HP 2749B Teleprinter, and asynchronous modems. The interface kit can also be connected to an HP 2752A Teleprinter by rewiring its interface cable. Instructions for rewiring the cable are provided in Section IV. The interface kit cannot be used with HP 2644 Terminals.

You can program the interface kit to transfer data under direct memory access (this is called "dual channel port controller" in the HP 21MX Computer), interrupt, or skip-on-flag program control.

Note: The term "direct memory access" or "DMA" is used throughout this manual and includes the dual channel port controller (DCPC).

The interface kit operates in character mode. In this mode, the interface kit accepts only one character at a time from the CPU (or device) before sending it to the device (or CPU). A detailed discussion of interface operation is presented in section II.

The interface provides parity (if selected), start, and stop bits to each character sent to the device. When data is received from the device, the interface strips these bits from each character so that only the character data bits are sent to the CPU.

1-1. FEATURES

The features of the interface include:

- You can select one of 16 baud rates (from 50 to 9600 baud, including an externally-supplied x16 clock), either through your program or by hardwiring jumpers in the cable connector.
- You can select character length (5 to 8 bits) and number of stop bits (1 or 2) through your program. (When a 5-bit character length is selected, the number of stop bits that you can select is either 1 or 1½.)
- You can select parity (on/off) and parity sense (odd/even) through your program.
- Interrupt Flags you can test for, indicating data buffer full, buffer empty, buffer overrun, and break condition.
- Continuous monitoring of RS-232-C status lines which allows you to program the HP 12968A to interrupt when any of the lines that you select change state.

1-2. KIT CONTENTS

1-3. Standard Version

The standard interface kit provides connection to an HP 2600 or HP 2615 Terminal and contains the following items:

a. Asynchronous Communications Interface Printed Circuit Assembly (PCA), part no. 12968-60001.
b. Interconnecting Cable Assembly, 50 feet, part no. 12966-60004.
c. Test Connector, part no. 12966-60003.
d. This Reference Manual, part no. 12968-90001.

1-4. Option 001 (Direct Cable to HP 2640)

Option 001 replaces the standard cable assembly with Interconnecting Cable Assembly, 50 feet, part no. 12966-60008. This cable interfaces the HP 2640 Terminal.

1-5. Option 002 (Modem Cable)

Option 002 replaces the standard cable assembly with Interconnecting Cable Assembly, 50 feet, part no. 12966-60006. This cable interfaces the 103 and 202 Data Sets.

1-6. Option 003 (Direct Cable to HP 2749B)

Option 003 replaces the standard cable assembly with Interconnecting Cable Assembly, 25 feet, part no. 12966-60007. This cable interfaces the HP 2749B Teleprinter.

1-7. SYSTEM CONFIGURATION

The interface printed circuit assembly (PCA) occupies one I/O slot and uses one I/O select code. An interface PCA is required for each communication channel. Two typical configurations are shown in figure 1-1. Connection to the computer is via the standard I/O bus. The interface PCA is driven by your coded software program which uses one of five control words, or one data word to transfer information from the CPU to the interface PCA. Information transfer from the interface PCA to your program is achieved with one status word or one data word. The interface PCA is byte oriented, inputting or outputting one byte of data per I/O transfer (LIA/B, OTA/B instructions).

1-8. SPECIFICATIONS

Specifications for the 12968A are given in table 1-1.

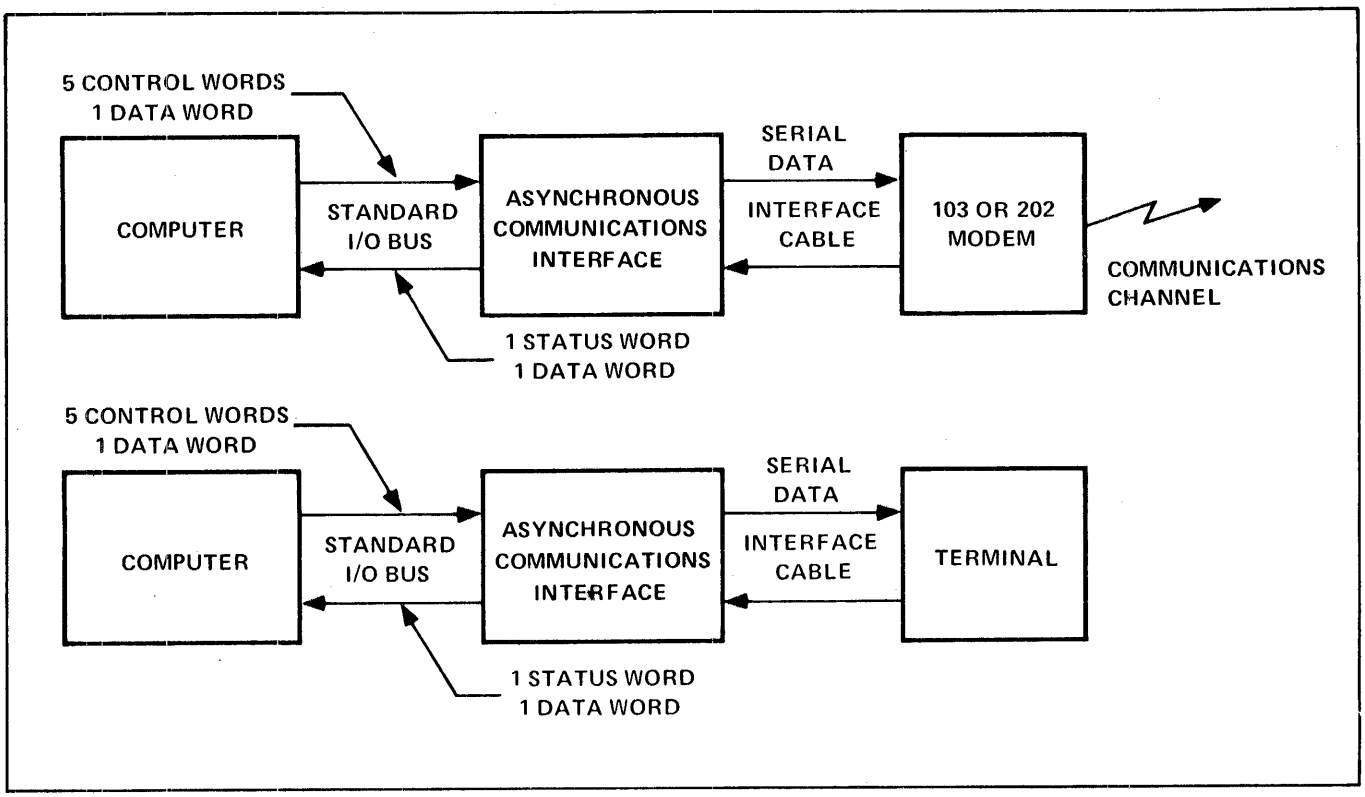


Figure 1-1. System Configurations Block Diagram

Table 1-1. Specifications

CHARACTERISTICS	SPECIFICATIONS
Function:	Asynchronous interface operating in half duplex mode that converts parallel data to serial data for transmission and converts received serial data to parallel data.
Compatibility:	Standard Kit: Used with HP2600 or HP2615 Terminals. Option 001: Used with HP 2640 Terminals. Option 002: Used with Bell Telephone System 103 or 202 type data sets. Option 003: Used with HP 2749B Teleprinter.
Device Interface Requirements:	Conforms to Electronic Industries Association Standard RS-232-C.

Table 1-1. Specifications (Continued)

CHARACTERISTIC	SPECIFICATION
Data Transfer Rate to/from Data Set Modem or Terminal:	Adjustable by program selection or hardware jumpers to discrete rates between 50 and 9600 baud. The rates are: 50 134.5 600 1800 4800 75 150 900 2400 7200 110 300 1200 3600 9600 An external x16 clock line can also be selected by your program or by hardware jumpers.
Character Size: (Input/Output of Computer)	Adjustable by program selection from five to eight bits (not including start, stop, and parity bits).
Stop Bits:	Adjustable by program selection to either 1 or 2 (when six, seven, or eight character bits are selected). When five character bits are selected, the selectable number of stop bits is either 1 or 1½.
Parity:	Programmable selection of parity function (on/off) and parity sense (odd/even).
Interrupt Flags:	Flag indication when: Buffer is full. Buffer is empty. Buffer Overrun/Parity Error. Break condition occurs. Device status line (CB, CC, CE, CF, SBB, or SCF) has changed state, if enabled by your program.
Power Consumption from Computer:	
+5 volt supply:	1.32A nominal
+12 volt supply:	12 mA nominal
-2 volt supply:	52 mA nominal
-12 volt supply:	35 mA nominal

PRINCIPLES OF OPERATION

SECTION II

This section gives an overview of the principles of operation of the interface. The HP 12968A operates in either of two selectable modes; transmit or receive. Figure 2-1 shows the nine words used to transfer data and control the HP 12968A. These words are described in detail in section III, Programming.

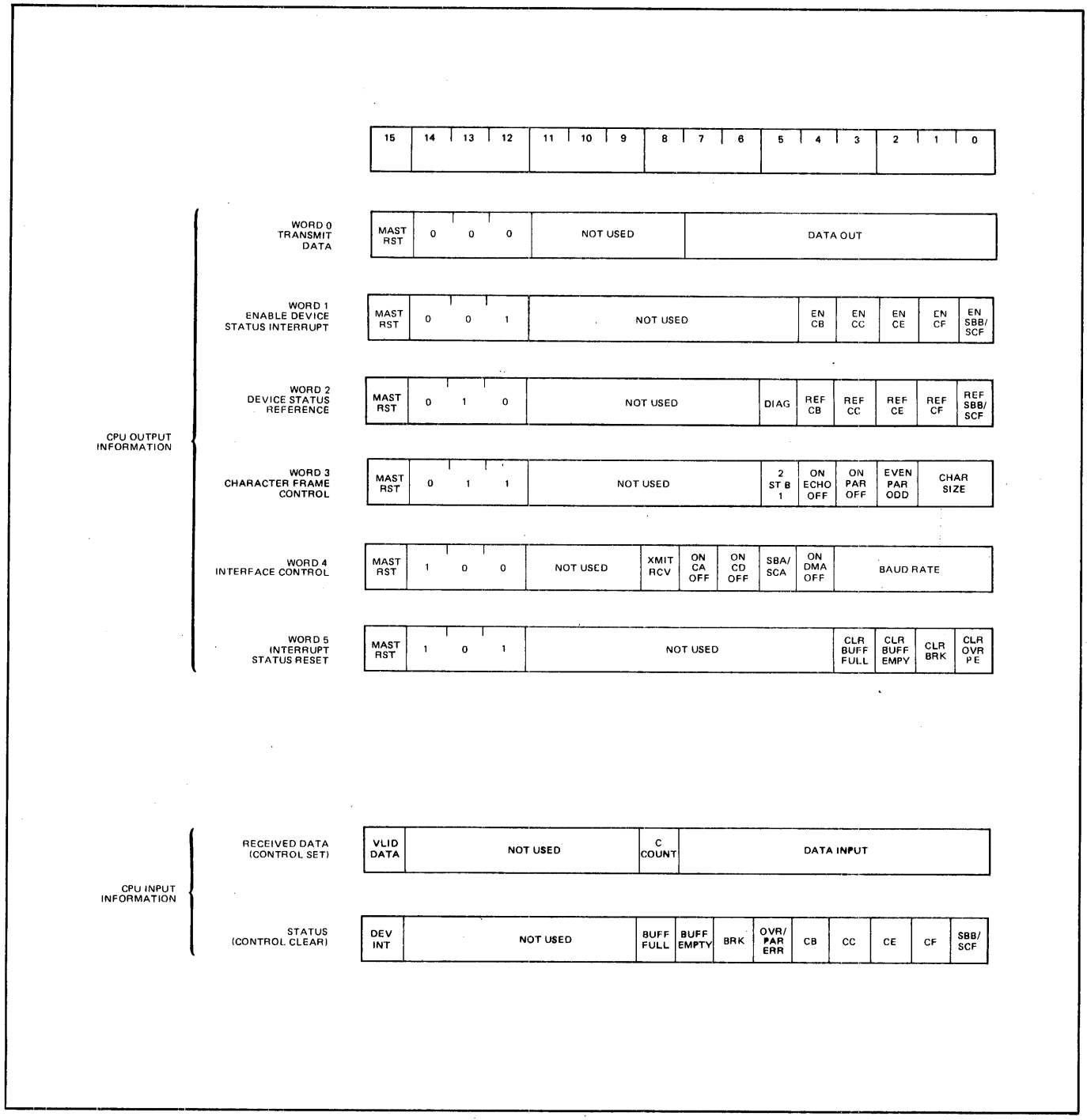


Figure 2-1. Data Transfer and Control Words

2-1. TRANSMIT MODE

In transmit mode data is transferred from the CPU to a terminal, either directly or through a modem. All data to be transmitted originates in the CPU. (You should refer to figure 2-2 while reading the discussion of the transmit mode.)

Prior to transferring data to the interface PCA for transmission, you must configure the PCA for the appropriate character size, parity, number of stop bits, and baud rate. Control Words 3 and 4, which are described in section III, configure the PCA, as well as select the transmit operating mode. Once the PCA has been configured, data transfer can be initiated.

Data transfer between the CPU and the interface PCA occurs in the form of 8-bit parallel bytes. No unpacking is provided by the PCA, that is, data cannot be sent to the PCA in the form of two data bytes in a 16-bit word because the PCA has no provision for separating the two bytes. Therefore, data must be transferred in the Word 0 format described in section III.

The data transfer may occur under program control (either interrupt or skip-on-flag) or direct memory access control. The type of control is set by Control Word 4 when you configure the PCA. The data byte (contained in Word 0) from the CPU is entered into an input buffer on the PCA. The output of the input buffer is transferred to a Universal Asynchronous Receiver/Transmitter (UART) which converts the parallel data byte into a serial word that contains the data bits along with start, parity, and stop bits. When parity is enabled, the UART automatically computes the parity bit of the specified sense (either odd or even) and adds it to the serial data being transmitted. The UART operates at the baud rate selected by Control Word 4 when the PCA is configured.

The Buffer Full Status Flag (bit 8 of the Status Word) is set when the data byte is transferred from the CPU to the UART. After the UART converts the parallel data byte to a serial word and transmits it to the device, the Buffer Empty Status Flag is set (bit 7 of the Status Word). Before transferring a data byte to the interface, the status flags should be cleared (by issuing Control Word 5 with bits 0 through 3 set) to ensure that an STC,C instruction will clear the interface prior to outputting the data byte. This will allow the Buffer Full Status Flag to set when the data byte is transferred from the CPU to the UART. Another Control Word 5 followed by an STC,C instruction should be issued to clear the interface and status flags to allow the Buffer Empty Status Flag to set when the data is transmitted to the device.

2-2. RECEIVE MODE

In receive mode data is transferred from a terminal, or modem, to the CPU (see figure 2-3). As in the transmit mode, you must configure the interface PCA for the appropriate character size, number of stop bits, and baud rate. Control Words 3 and 4, which are described in section III, configure the PCA and select the receive operating mode. Once the PCA is configured, data transfer can be initiated. The PCA does not need to be reconfigured each time the operating mode is changed if the character size, parity, number of stop bits, and baud rate are the same for both receive and transmit modes.

Data transfer between the PCA and the CPU occurs in the form of 8-bit parallel bytes. No packing is provided by the PCA, that is, data cannot be sent to the CPU in the form of two data bytes in a 16-bit word because the PCA has no provision for combining the two 8-bit bytes. Therefore, data is transferred in the Received Data Word format described in section III.

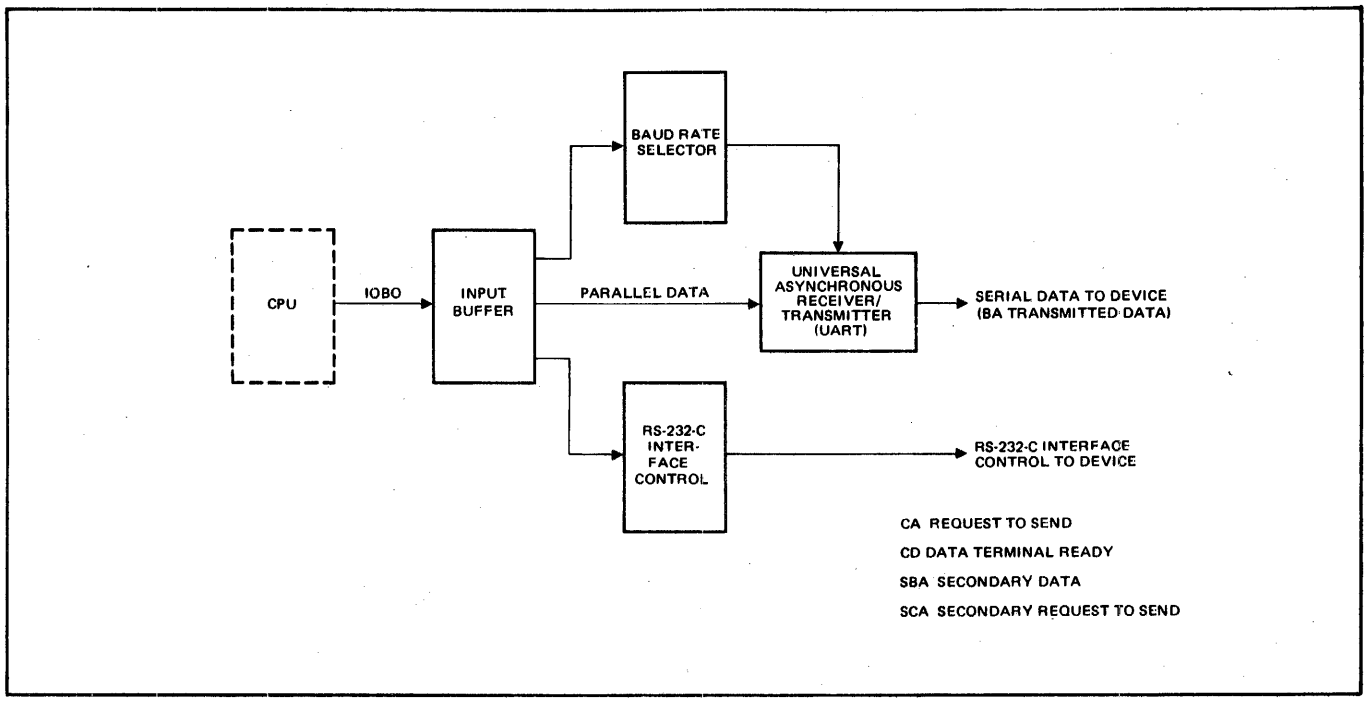


Figure 2-2. Transmit Mode Data Transfer

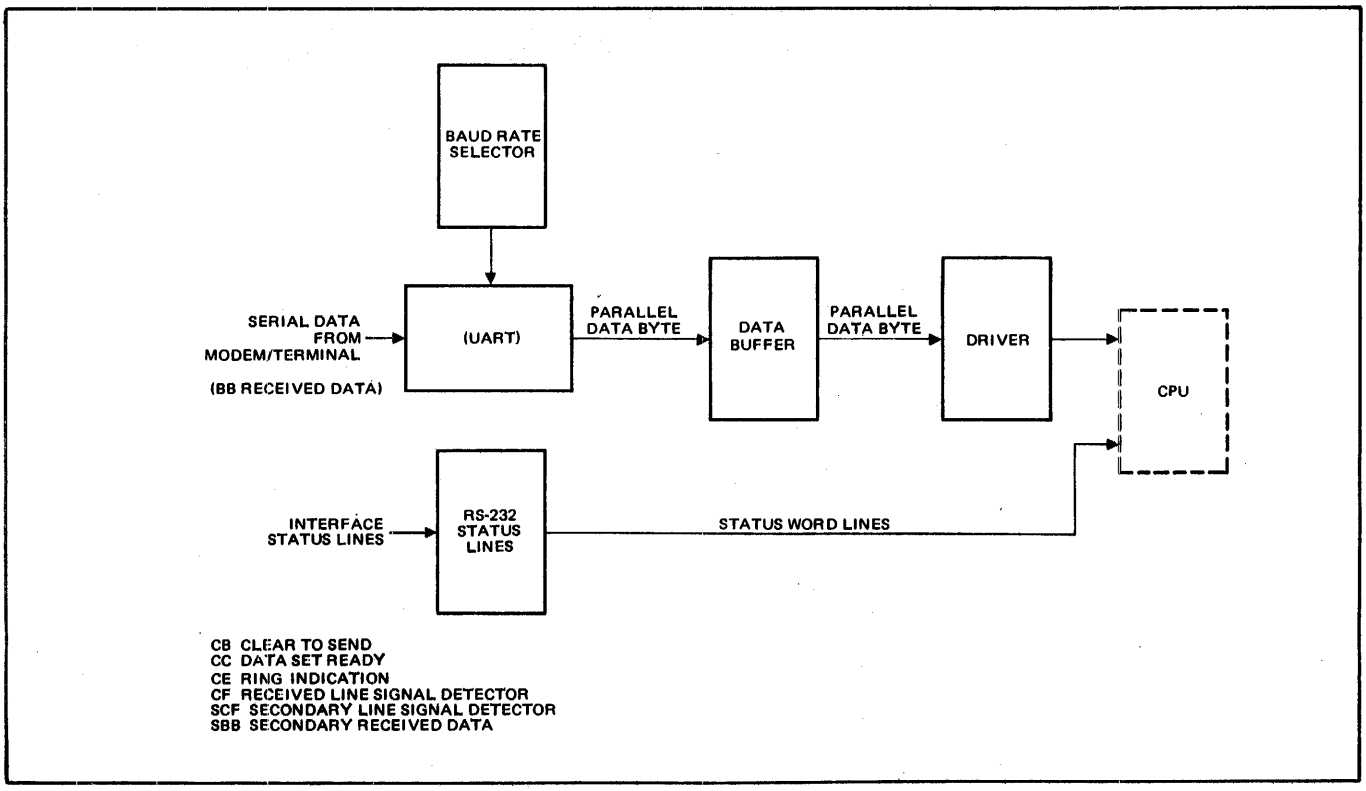


Figure 2-3. Receive Mode Data Transfer

The data transfer may be accomplished under either program control (interrupt or skip-on-flag) or direct memory access control. The type of control is set by Control Word 4 when you configure the PCA. The serial data received by the PCA from the terminal, or modem, is transformed into a parallel byte by the receiving portion of the UART. If ECHO is on (bit 4 of Control Word 3), the received serial data is also routed back to the terminal, or modem, over the transmit data line. If parity check is enabled, the UART calculates the correct parity and compares it with the parity bit in the received character bit stream. If the calculated parity bit does not match the received parity bit, a parity error interrupt is generated. Also, the Overflow/Parity Error bit is set in the Status Word. The received parity is stripped from the data byte and therefore is not available to the program. In addition to parity, the UART also tests for stop bits. The absence of stop bits and all zero data will result in a break condition which will set the Break bit in the Status Word.

After parity and stop tests, the parallel data byte from the UART is stored in a data buffer. The Buffer Full Status Flag is set, the Character Count bit of the Received Data Word is set, and the Valid Data bits of the Received Data and Status Words are set.

The CPU reads the data byte out of the buffer by executing an LIA/B instruction (with the Control FF set). The data byte along with the Character Count, Valid Data bits are sent to the CPU in the Receive Data Word. The Buffer Empty Status Flag is set and the Character Count bit is cleared. If another data byte is received from the terminal, or modem, before an LIA or LIB instruction is executed with Control FF set, the Overrun/Parity Error bit of the Status Word is set indicating a buffer overrun condition.

The setting of any one of the status flags or a change in the device status lines (specified by Control Words 1 and 2) will cause an interrupt or skip-on-flag condition. The status flags are:

a. Buffer Full
b. Buffer Empty
c. Buffer Overrun
d. Parity Error
e. Break

When under DMA control (set by Control Word 4), Buffer Full and Buffer Empty Status Flags cannot cause an interrupt or skip-on-flag condition. However, they still may be tested by examining bits 7 and 8 of the Status Word.

2-3. CPU-DEVICE INTERFACE DESCRIPTION

2-4. CPU Interface

The HP 12968A interfaces with the CPU via the I/O bus. You use standard I/O instructions to transfer information and control the interrupt protocol. Specific effects of each I/O instruction are discussed in section III, Programming.

The types of information transferred between the CPU and the asynchronous communications interface are:

a. Commands and Transmit Data from the CPU to the interface.
b. Status and Receive Data from the interface to the CPU.

Commands, transmit data, and receive data may be transferred under direct program control or direct memory access control. Status may be transferred under direct program control only. It is sent to the CPU with every LIA/B instruction whenever the Control FF is clear.

2-5. Device Interface

The HP 12968A -to-device interface consists of two data transfer lines, four modem/terminal control lines, and six modem/terminal status lines.

Note: The RS-232-C circuit designations appear in parenthesis after the signal line name. Line SBB is not connected to a device by the interface cables documented in tables 4-2 through 4-5.

The two data transfer lines are:

a. Transmitted Data (BA)
b. Received Data (BB)

The four modem/terminal control lines are:

a. Request to Send (CA)
b. Data Terminal Ready (CD)
c. Secondary Transmitted Data (SBA)
d. Secondary Request to Send (SCA)

These lines, defined in RS-232-C, are under program control. Only three of the four are used at any one time (CA, CD, and either SBA or SCA), as dictated by hardware jumpers on the cable connector. (Refer to tables 4-2 through 4-5.)

The six modem/terminal status lines are:

a. Clear to Send (CB)
b. Data Set Ready (CC)
c. Ring Indicator (CE)
d. Received Line Signal Detector (CF)
e. Secondary Received Line Signal Detector (SCF)
f. Secondary Received Data (SBB)

Five of the six status lines (CB, CC, CE, CF, and either SCF or SBB) from the modem/terminal are available to your program in the Status Word. (SCF or SBB is selected by hardware jumpers in the cable connector — refer to tables 4-2 through 4-5.) Also, the HP 12968A monitors these status lines to generate an interrupt if a change occurs. This interrupt capability is controlled by two commands (Control Words 1 and 2, which are defined in section III) which enable or disable interrupts from each status line, and which define what line sense should cause an interrupt to occur.

PROGRAMMING

SECTION III

This section provides you with the information necessary to code your driver program. Software interface characteristics are discussed first, followed by an explanation of various words used to control the PCA. A sample program flowchart and listing are given at the end of the section.

3-1. SOFTWARE INTERFACE CHARACTERISTICS

The HP 12968A Asynchronous Communications Interface follows the standard software protocol with a few exceptions:

a. STC,C is not required to initiate a character transfer.

b. STC is required to enable status interrupts (buffer full, buffer empty, etc.).

c. The Status Flags are always set for the following conditions when under direct memory access or program control:

DIRECT MEMORY ACCESS CONTROL		PROGRAM CONTROL	
TRANSMIT MODE	RECEIVE MODE	TRANSMIT MODE	RECEIVE MODE
Device Status Line Change	Device Status Line Change	Device Status Line Change	Device Status Line Change
	Break	Buffer Empty	Break
	Buffer Overrun	Buffer Full	Buffer Overrun
	Parity Error		Parity Error
			Buffer Empty
			Buffer Full

d. The Flag is not set on completion of a character output to the device or Input from the device.

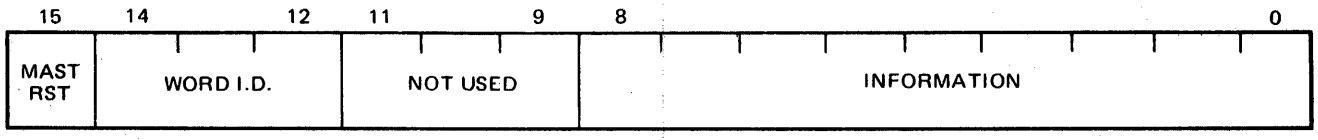
e. When operating under direct memory access control, a Service Request (SRQ) is generated whenever a data character is ready for input or output, providing that an interrupt condition listed in "c" above is not pending. The Flag and SRQ functions are separated to permit interrupts to occur during a direct memory access data transfer.

f. The interface is controlled with six control words.

3-2. WORD FORMATS

3-3. CPU Output Word Format

Information transfer from the CPU to the HP 12968A is implemented by six different words (five command words and one data word) in the following general format. The "information" and "not used" field lengths vary, depending upon the word type.

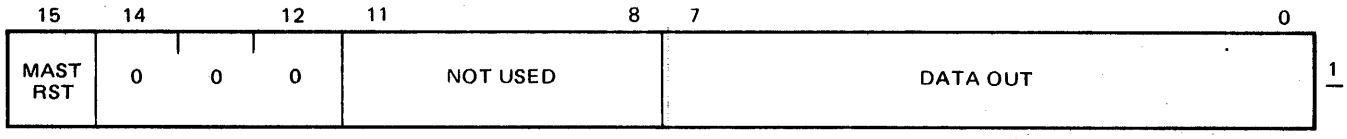


Bit 15 in all information transfer from the CPU to the HP 12968A is designated the Master Reset bit. This means that any OTA/B instructions to the interface with a "1" in bit 15 will result in a Master Reset which is described in detail later in this section. The Master Reset function is executed first, followed by transfer of the information part of the word (bits 0 — 8) to the designated destination. If, for example, word 4 is transferred to the interface with bit 15 a "1", the interface is reset first, then the baud rate, modem control bits, etc, are shifted into the correct registers. The Master Reset function is not recommended when coding the Transmit Data Word (Word 0).

Each command and data word is discussed in the following paragraphs.

3-4. Transmit Data Word (Word 0)

Word 0 is used to transfer one data byte from the CPU to the interface for transmission to the modem or terminal. The format of word 0 is as follows:

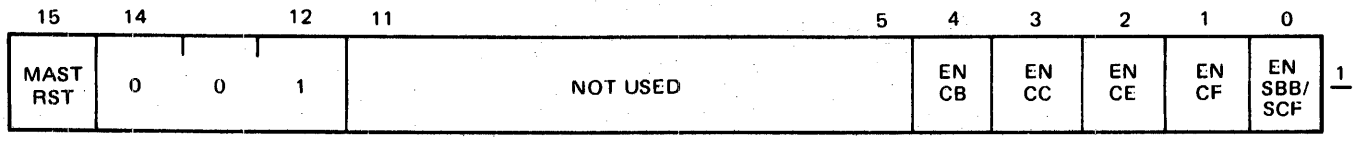


Transmit Data Word (Word 0)

BIT	DESIGNATION	DESCRIPTION
0 — 7	Data Byte	Data byte to be transmitted to modem or terminal.
12 — 14	Word Type	All three bits are "0"s to designate the transmit data word (word 0).
15	Master Reset	"0" = do not execute a master reset. "1" = execute a master reset. Note: Using Master Reset in Word 0 is not recommended; therefore, code "0" for bit 15.

3-5. Enable Device Status Interrupt Word (Word 1)

Word 1 enables, or disables, the interface to generate an interrupt whenever a device status line changes to a signal state different from that referenced in the device status reference word (word 2). The format of word 1 is as follows:

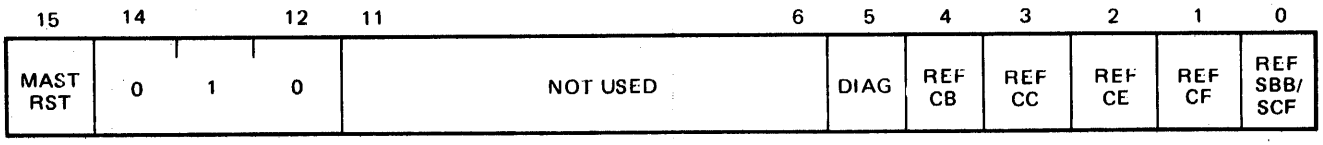


Enable Device Status Interrupt Word (Word 1)

BIT	DESIGNATION	DESCRIPTION
0	Enable SBB/SCF	"0" = will not set the device interrupt flag if the Secondary Receive Data line or the Secondary Received Line Signal Detector line changes state. "1" = will set the device interrupt flag if the Secondary Receive Data line or the Secondary Received Line Signal Detector line changes state.
1	Enable CF	"0" = will not set the device interrupt flag if the Receive Line Signal Detector line changes state. "1" = will set the device interrupt flag if the Receive Line Signal Detector line changes state.
2	Enable CE	"0" = will not set the device interrupt flag if the Ring Indicator line changes state. "1" = will set the device interrupt flag if the Ring Indicator line changes state.
3	Enable CC	"0" = will not set the device interrupt flag if the Data Set Ready line changes state. "1" = will set the device interrupt flag if the Data Set Ready line changes state.
4	Enable CB	"0" = will not set the device interrupt flag if the Clear to Send line changes state. "1" = will set the device interrupt flag if the Clear to Send line changes state.
12 – 14	Word Type	Bits are set to an octal "1" to designate the enable device status interrupt word (word 1).
15	Master Reset	"0" = do not execute a master reset. "1" = execute a master reset.

3-6. Device Status Reference Word (Word 2)

Word 2 sets up the reference state to which the corresponding device status input lines are compared. If any of the status lines differ from the reference and it has been enabled by the enable device status interrupt word (word 1), an interrupt is generated. The format of word 2 is as follows:

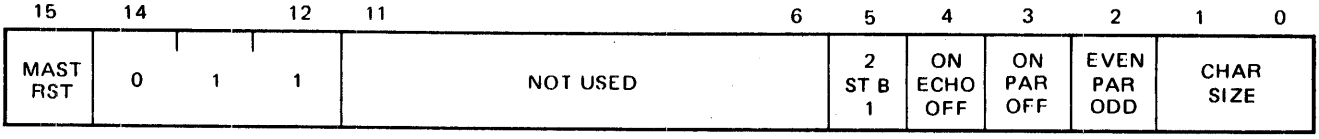


Device Status Reference Word (Word 2)

BIT	DESIGNATION	DESCRIPTION
0	Reference SBB/SCF	SBB (Secondary Received Data): "0" = binary "1" data. "1" = binary "0" data. SCF (Secondary Received Line Signal Detector): "0" = OFF. "1" = ON.
1	Reference CF	"0" = Received Line Signal Detector OFF. "1" = Received Line Signal Detector ON.
2	Reference CE	"0" = Ring Indicator OFF. "1" = Ring Indicator ON.
3	Reference CC	"0" = Data Set Ready OFF. "1" = Data Set Ready ON.
4	Reference CB	"0" = Clear to Send OFF. "1" = Clear to Send ON.
5	Diagnostic	This bit is available at the interface connector for diagnostic test purposes.
12 — 14	Word Type	Bits are set to an octal "2" to designate the device status reference word (word 2).
15	Master Reset	"0" = do not execute a master reset. "1" = execute a master reset.

3-7. Character Frame Control Word (Word 3)

Word 3, except for the ECHO bit, controls the operation of the Universal Asynchronous Receiver/ Transmitter (UART) by specifying the character size, number of stop bits, and parity. The ECHO bit enables the echo function when the interface is in the receive mode. (That is, the character is displayed on the terminal when it is received by the interface.) The format of word 3 is as follows:

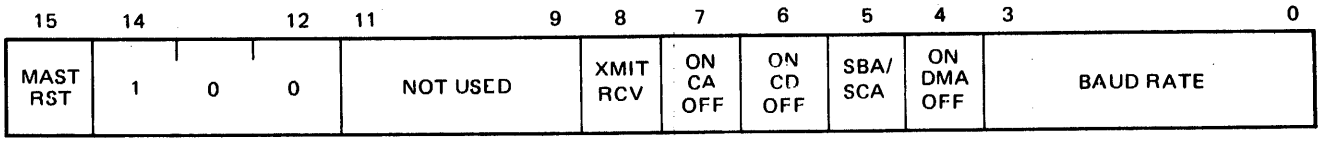


Character Frame Control Word (Word 3)

BIT	DESIGNATION	DESCRIPTION
0 — 1	Character Size	Bit 1 / Field 0 — Number of Bits/Character (Not Including Parity, Start, or Stop Bits) 0 0 — 5 0 1 — 6 1 0 — 7 1 1 — 8
2	Parity Odd/Even	"0" = odd parity. "1" = even parity.
3	Parity On/Off	"0" = parity generator/checker is OFF. "1" = parity generator/checker is ON.
4	Echo On/Off	"0" = echo is OFF. "1" = echo is ON. (Display the character at the terminal.)
5	Number of Stop Bits	"0" = one stop bit. "1" = two stop bits (one and one-half stop bits when character size is five).
12 — 14	Word Type	Bits are set to an octal "3" to designate character frame control word (word 3).
15	Master Reset	"0" = do not execute a master reset. "1" = execute a master reset.

3-8. Interface Control Word (Word 4)

Word 4 controls the RS-232-C output control lines, defines the baud rate, specifies DMA or program control for the upcoming data transfer, and places the interface in either transmit or receive mode. The format of word 4 is as follows:



Interface Control Word (Word 4)

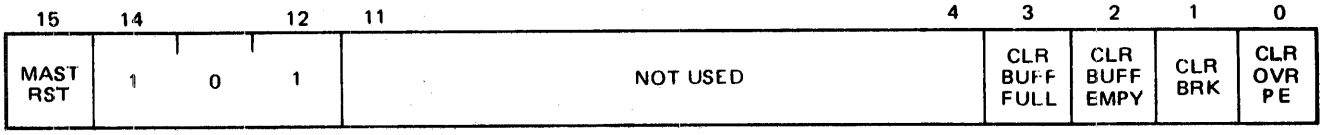
BIT	DESIGNATION	DESCRIPTION
0 — 3	Baud Rate	Bit Field 3 2 1 0 Baud Rate 0 0 0 0 External Clock (x16) 0 0 0 1 50 0 0 1 0 75 0 0 1 1 110 0 1 0 0 134.5 0 1 0 1 150 0 1 1 0 300 0 1 1 1 600 1 0 0 0 900 1 0 0 1 1200 1 0 1 0 1800 1 0 1 1 2400 1 1 0 0 3600 1 1 0 1 4800 1 1 1 0 7200 1 1 1 1 9600
4	DMA (Direct Memory Access)	"0" = program controlled data transfer. "1" = DMA controlled data transfer.
5	SBA/SCA	SBA (Secondary Transmit Data): "0" = binary "0" data. "1" = binary "1" data. SCA (Secondary Request to Send): "0" = OFF. "1" = ON.
6	CD	"0" = Data Terminal Ready OFF. "1" = Data Terminal Ready ON.
7	CA	"0" = Request to Send OFF. "1" = Request to Send ON.

Interface Control Word (Word 4) - Continued

BIT	DESIGNATION	DESCRIPTION
8	Transmit/Receive	"0" = receive mode. "1" = transmit mode.
12 — 14	Word Type	Bits are set to an octal "4" to designate the interface control word (word 4).
15	Master Reset	"0" = do not execute master reset. "1" = execute master reset.

3-9. Interrupt Status Reset Word (Word 5)

Word 5 permits the software driver to individually clear the source(s) of an interrupt. Once a condition on the interface results in an interrupt, the interrupt will remain until it is cleared by a specific bit in word 5, even if the causal condition may no longer be present. The format of word 5 is as follows:



Interrupt Status Reset Word (Word 5)

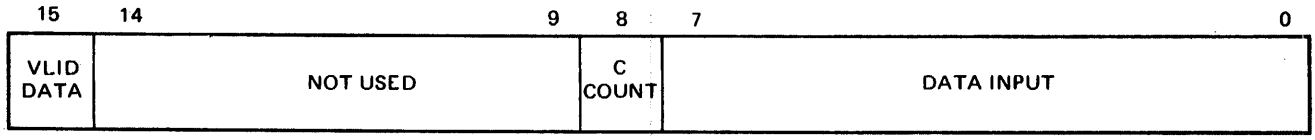
BIT	DESIGNATION	DESCRIPTION
0	Clear Overrun/Parity Error Status Flag	"0" = do not clear the flag. "1" = clear the flag.
1	Clear Break Status Flag	"0" = do not clear the flag. "1" = clear the flag.
2	Clear Buffer Empty Status Flag	"0" = do not clear the flag. "1" = clear the flag.
3	Clear Buffer Full Status Flag	"0" = do not clear the flag. "1" = clear the flag.
12 — 14	Word Type	Bits are set to octal "5" to specify the interrupt status reset word (word 5).
15	Master Reset	"0" = do not execute master reset. "1" = execute master reset.

3-10. CPU Input Word Format

Information transfer from the interface to the CPU is implemented with two words. The Received Data Word is available whenever the Control FF is set, and the Status Word is available whenever the Control FF is clear. The interface supplies these two words in the formats described below.

3-11. Received Data Word (Control FF Set)

This word contains a character/data byte (up to 8 bits), a valid data bit, and a character count bit indicating if a data byte is currently in the buffer.

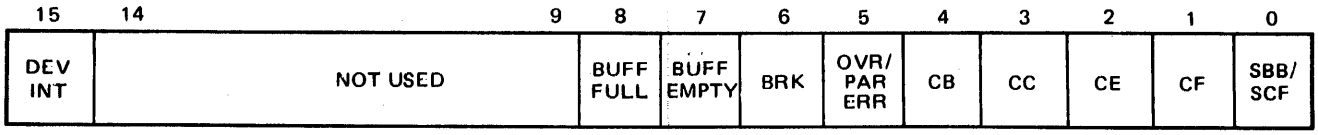


Received Data Word

BIT	DESIGNATION	DESCRIPTION
0 — 7	Received Data	A data byte (from 5 to 8 bits long) received from the modem or terminal.
8	Character Count	"0" = No data byte in buffer. "1" = Data byte in buffer.
15	Valid Data Marker	"0" = the character/data byte in bits 0 thru 7 is *not* a valid character/data byte. "1" = the character/data byte in bits 0 thru 7 is a valid character/data byte.

3-12. Status Word (Control FF Clear)

The Status Word is input when the Control FF is clear. This word contains the real-time modem/terminal status lines values. In addition to the status lines, the word contains flags which identify the cause of the interrupt. These flags must be cleared after reading them. If not, they may not represent current status when checked by your program the next time. The format of the Status Word is described below.



Status Word

BIT	DESIGNATION	DESCRIPTION
0	SBB/SCF	SBB (Secondary Received Data): "0" = binary "0" data. "1" = binary "1" data. SCF (Secondary Received Line Signal Detector): "0" = OFF. "1" = ON.
1	CF	"0" = Received Line Signal Detector OFF. "1" = Received Line Signal Detector ON.
2	CE	"0" = Ring Indicator OFF. "1" = Ring Indicator ON.
3	CC	"0" = Data Set Ready OFF. "1" = Data Set Ready ON.
4	CB	"0" = Clear to Send OFF. "1" = Clear to Send ON.
5	Overrun or Parity error	"0" = no data buffer overrun or parity error. "1" = data buffer overrun or parity error.
6	Break	"0" = no break condition present. "1" = break condition has been detected, no data is present, and no stop bits have been received.
7	Buffer Empty	"0" = buffer is not empty. "1" = buffer is empty.
8	Buffer Full	"0" = buffer is not full. "1" = buffer is full.
15	Device Interrupt	"0" = no device status line interrupt. "1" = a device status line (CB, CC, CE, CF, and SBB/SCF in bit field 0 thru 4 of this word) that has been enabled, has changed and is causing a device interrupt.

3-13. EFFECTS OF I/O INSTRUCTIONS

3-14. Master Reset

Master Reset is generated as a result of various I/O instructions or functions:

a. At power ON, or a front panel PRESET.

b. Issuing a CLC 0 instruction (turning off all I/O devices).

c. Bit 15 being a "1" in any of the information words transferred from the CPU to the interface (word 0 through word 6, which are described earlier in this section).

Master Reset places the interface in a known operating state as follows:

a. Receive operating mode.

b. Echo: OFF.

c. DMA: OFF. (DMA mode is not being used.)

d. Request to Send (CA): OFF.

e. Data Terminal Ready (CD): OFF.

f. Clears all data in the buffer.

g. Clears the Universal Asynchronous Receiver/Transmitter (UART), aborts transmission of any character immediately.

h. Clears the character count FF.

i. Clears Service Request (SRQ).

j. Clears Control FF.

k. Sets Flag.

l. Sets Lockout (inhibits any conditions on the interface to generate an interrupt).

m. Clears the Device Status Interrupt Enable register (which stores the conditions set forth in Control Word 1) thereby inhibiting any interrupt as a result of modem/terminal status change.

n. The following status flags are *not* affected: buffer empty, buffer full, buffer overrun, break, and parity error. (Word 5 must be issued to affect these status flags.)

o. The character size, number of stop bits, parity, and parity sense are *not* altered. (Word 3 must be issued to affect these.)

p. The baud rate is *not* affected. (Word 4 must be issued to affect baud rate.)

q. Clears the Device Status Reference register (which stores the conditions set forth in Control Word 2).

3-15. Set Control (STC) Instruction

STC enables interrupts from the interface, as with other 2100 Series Computer interfaces. But it also has two other important effects.

First, STC,C must be issued at the end of the service routine for each interface request (data or status), whether or not interrupts are being used. This is because of the interrupt interlock used by the interface to prevent interrupts occurring within interrupts (i.e., nested interrupts). In effect, the STC at the end of the service routine informs the interface that the current request has been serviced and that the program is ready to accept another request from the interface. Until the STC occurs, the interface will *not* be able to set its flag to request further service.

If it is necessary to operate the interface in an interrupt environment, but you do not want to use the interrupt method for servicing the interface (i.e., interrupt system is on, but the interface is using "skip-on-flag" method of servicing), unwanted interrupts can be prevented by following the STC immediately with the Clear Control (CLC) instruction.

Secondly, the STC is issued prior to requesting Received Data words.

3-16. Clear Control (CLC) Instruction

The CLC instruction is used to disable interrupts from the interface, as with other 2100 Series Computer interfaces. But it also affects the operation of the input word selector in the opposite manner as does the STC instruction. The Control FF must be clear in order to input the Status word.

Note: Because of the interrupt interlock on the interface, it is not necessary to "clear control" following an interrupt; Once an interrupt has occurred, no more interrupts can occur until an STC is issued. However, the CLC may be used for conformance with standard programming technique with no adverse effects.

3-17. Output A (OTA) Instruction

The OTA instruction is used to transfer information (CPU output Words 0 through 6) from the CPU to the interface. Word outputs with bit 15 set to a "1" are interpreted as Master Reset by the interface.

3-18. Load Into A (LIA) Instruction

The LIA instruction is used to transfer information (the Received Data and Status words) from the interface to the CPU. Because the interface uses two types of input information (received data and status), the program and the interface must be able to know which type is to be supplied for any particular transfer. The selection is controlled by the program through the STC and CLC instructions.

3-19. Set Flag (STF) Instruction

The STF instruction is used to "force" the interface to produce an interrupt request, providing that the interrupt system is on and that an STC instruction to the interface has been executed. This is the same function as with other 2100 Series Computer interfaces.

3-20. Clear Flag (CLF) Instruction

The CLF instruction clears the interface flag and disables the interrupt request from the interface, as with other 2100 Series Computer interfaces.

3-21. Sample Program

The sample program (see figures 3-1 and 3-2) demonstrates basic programming techniques for using the HP 12968A Asynchronous Data Communications Interface. This program can be used by the user as a test program to get started before writing his own program.

The user enters a character from a remote terminal (an HP 2640A, or equivalent). The character is loaded into the buffer of the interface. When the Buffer Full Status Flag is set, the character is transferred to a CPU buffer. The interface is then placed in the transmit mode, and the character is loaded back into the interface buffer from the CPU buffer. After the character is transferred, the interface transmits the character in the interface buffer to the terminal.

Data transfer to/from the terminal is at 1200 Baud, one stop bit, eight-bit ASCII, no parity, and Echo is on. The program assumes that the interface PCA is in select code 12_8; however, this can be changed easily in the program to fit the user's equipment configuration.

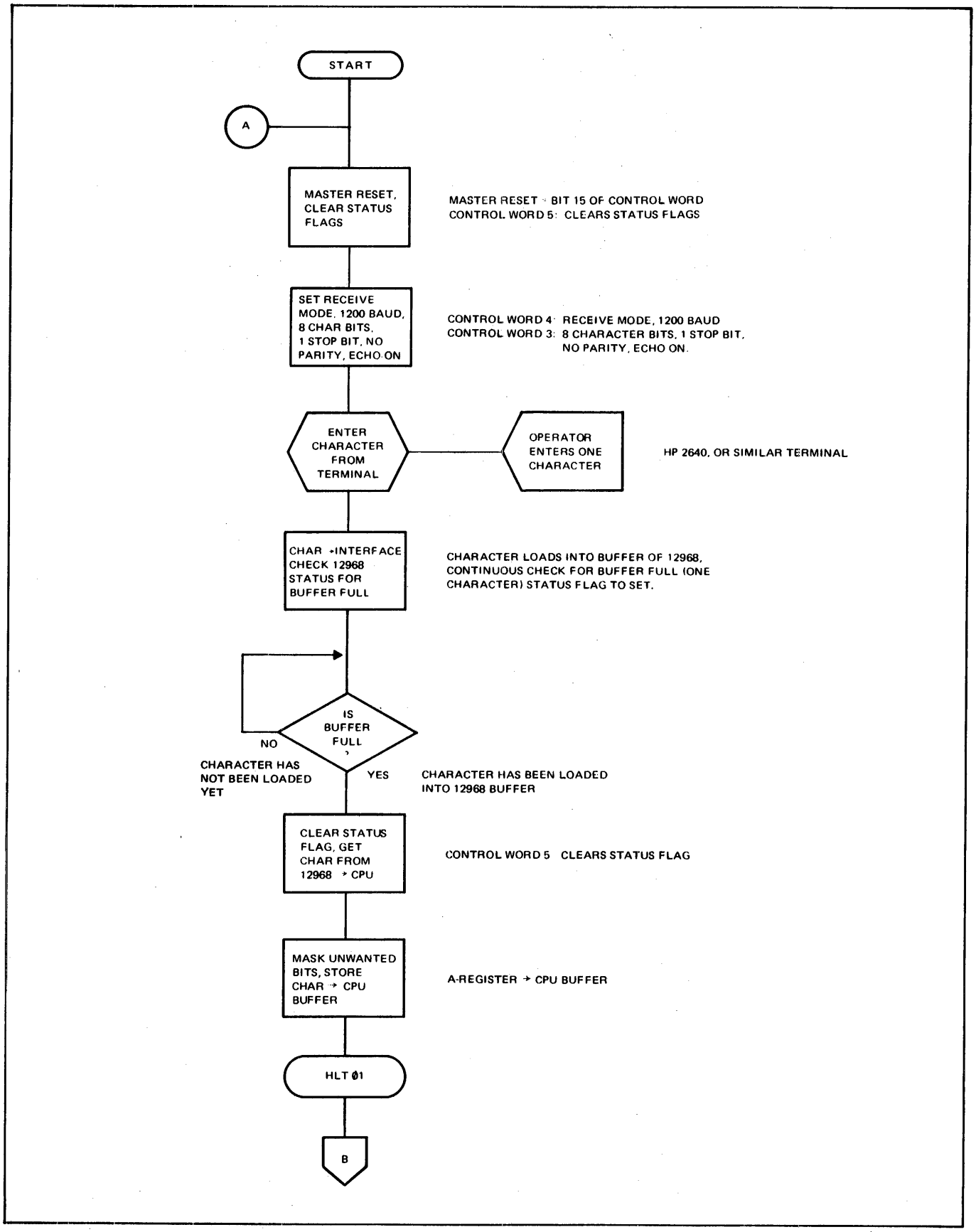


Figure 3-1. Sample Program Flowchart (Sheet 1 of 2)

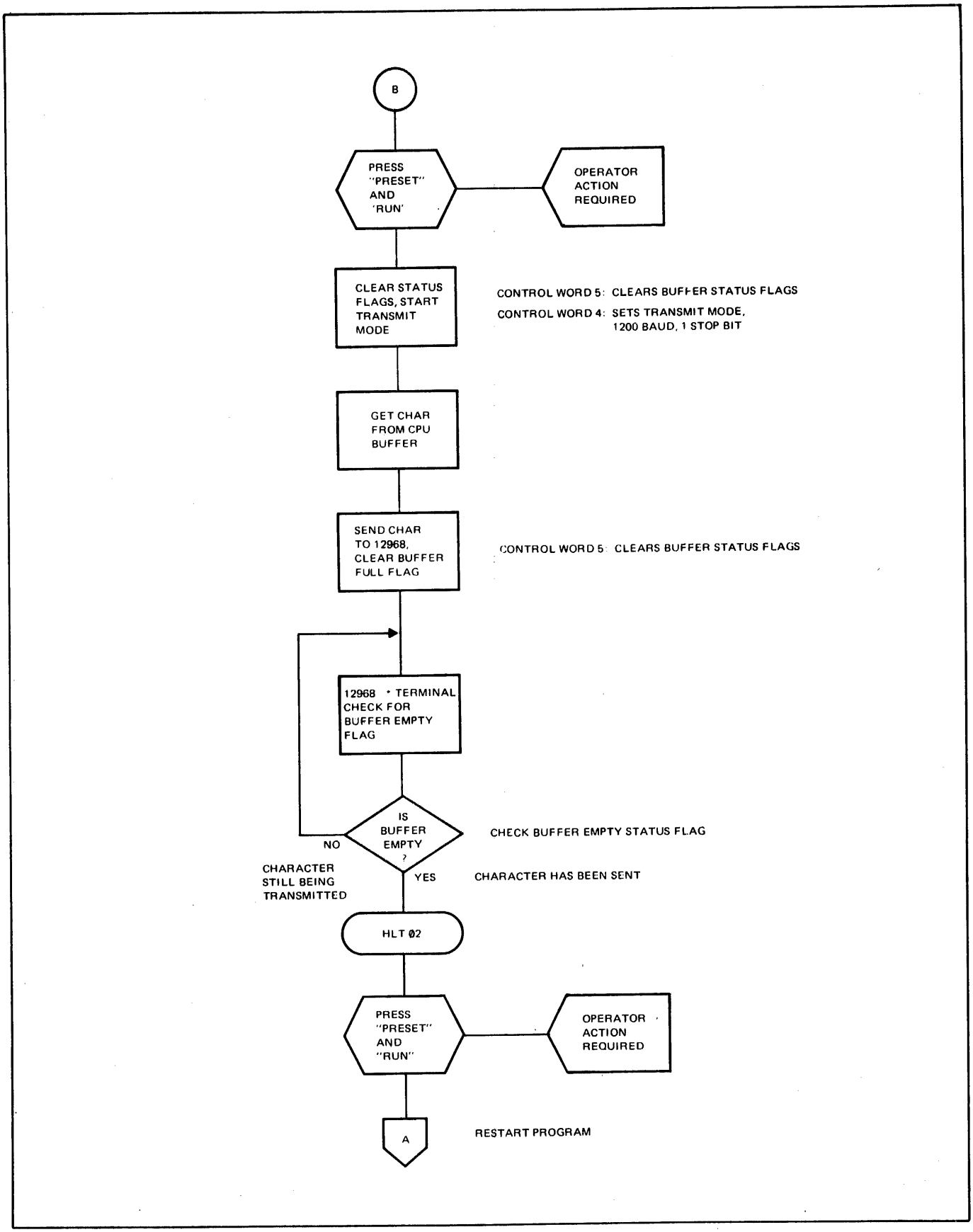


Figure 3-1. Sample Program Flowchart (Sheet 2 of 2)

```
0001  ASMB,A,B,L,T
0002        ORG 100B
0003  *
0004  ****12968 SAMPLE PROGRAM ****************************************
0005  *THE 12968 IS INITALIZED IN RECEIVE MODE,1200 BAUD.THE USER
0006  *ENTERS A CHARACTER FROM THE REMOTE TERMINAL(HP2640 OR EQUIV)
0007  *THE CHARACTER IS SENT TO THE 12968'S BUFFER.THE CHAR IS NEXT
0008  *TRANSFERRED TO THE CPU BUFFER AND THE CPU HALTS(HLT 01).PRESS
0009  *'PRESET' AND 'RUN' TO PLACE 12968 INTO THE TRANSMIT MODE.
0010  *THE CHAR IS SENT TO THE 12968 AND WHEN 'BUFFER FULL' IS SENSED
0011  *THE CHAR IS SENT TO THE TERMINAL.THE CPU THEN HALTS(HLT 02).
0012  *PRESSING 'PRESET' AND 'RUN' RESTARTS THE PROGRAM AGAIN.
0013  *
0014  *
0015  A     EQU 0
0016  B     EQU 1
0017  SCT   EQU 12B       12968 IS IN SELECT CODE 12B
0018  BUFF  BSS 1
0019  CW3   OCT 030023
0020  CW4R  OCT 040011
0021  CW4T  OCT 140411
0022  CW5   OCT 050077
0023  PAT   OCT 777
0024  CLEAR OCT 060400
0025  *
0026  *
0027        ORG 200B
0028  START LDA CW4T      MASTER RESET,INITIALIZE TRANSMIT
0029        OTA SCT
0030        LDA CW5       LOAD WORD 5,CLEAR FLAGS
0031        OTA SCT
0032        LDA CW3       LOAD WORD 3,1 STOP BIT,8 DATA BITS
0033        OTA SCT         ECHO ON,NO PARITY
0034        LDA CW4R      LOAD WORD 4,RECEIVE MODE,1200 BAUD
0035        OTA SCT
0036  CHECK STC SCT,C     SET CONTROL 12968
0037        SFS SCT       CHECK IF STATUS FLAG IS SET
0038        JMP *-1       BUFF FULL NOT YET SET
0039        CLC SCT       YES,FLAG HAS SET
0040        LDA CW5       BF SET,CLEAR STATUS FLAGS
0041        OTA SCT
0042        STC SCT,C     SET CONTROL 12968
0043        LIA SCT       GET CHARACTER FROM 12968
0044        AND PAT       MASK OUT UNWANTED BITS
0045        STA BUFF      STORE CHAR INTO CPU BUFFER
0046        HLT 01        YES,CPU BUFFER IS FULL
0047  ***PRESS 'PRESET' AND 'RUN' TO PUT 12968 INTO TRANSMIT
0048  *MODE.
0049  *
0050        NOP
0051        LDA CW4T      SETUP 12968 TO TRANSMIT @1200 BAUD
0052        OTA SCT
0053        LDA CW5       CLEAR BUFFERS
0054        OTA SCT
0055        STC SCT,C
0056        LDA BUFF      GET CHAR FROM CPU BUFFER
0057        OTA SCT       PUT IT IN 12968 BUFFER
0058        LDA CW5       YES,LOAD WORD 5 TO CLEAR BUFF
0059        OTA SCT             FULL
0060        STC SCT,C   SET CONTROL,START TRANSMIT
0061        SFS SCT       IS BUFFER EMPTY?
0062        JMP *-1       NO,NOT YET!!!
0063        HLT 02        YES,IT IS EMPTY,HALT CPU!!
0064        JMP START     RESTART 12968
0065        END
```

Figure 3-2. Sample Program Listing

INSTALLATION AND SERVICING

SECTION IV

4-1. UNPACKING AND INSPECTION

If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the kit is unpacked. Inspect the kit for damage (cracks, broken parts, etc.). If the kit is damaged and fails to function properly, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The HP Sales and Service Office will arrange for the repair or replacement of the damaged kit without waiting for any claims against the carrier to be settled.

4-2. PREPARATION FOR USE

4-3. Baud Rate Jumpers

Before installation of the kit it is necessary to determine if the baud rate should be selected by hardwiring in the cable connector, rather than selected by program control. If the hardwired method is preferred, disassemble the cable connector which fastens to the interface printed circuit assembly, and connect the jumpers for the required baud rate. Figure 4-1 and table 4-1 provide instructions to accomplish this.

4-4. Cabling For HP 2752A Teleprinter

The HP 2752A Teleprinter can be connected to the interface PCA by rewiring the existing teleprinter cable at its interface connector. The rewiring allows the teleprinter to operate in a current loop at 110 baud. To rewire the connector, unsolder the cable conductors from the interface connector, and resolder them, and jumper wires, as shown in figure 4-2. Figure 4-1 may be referred to for disassembling the connector.

4-5. INSTALLATION

4-6. Printed Circuit Assembly

The printed circuit assembly fits into an I/O slot of the computer's card cage. The I/O slots correspond to I/O select codes which are used during programming to address a particular I/O device. Further information on the computer's I/O system and select codes can be found in the following publications, as applicable:

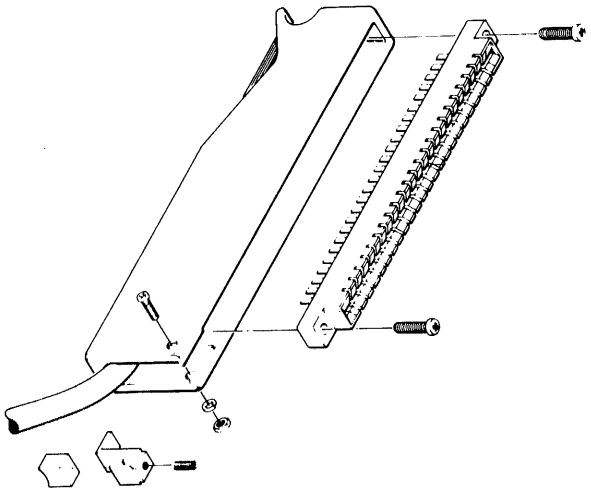
- *HP 21MX Computer Series Reference Manual*, part no. 02108-90002
- *HP 2100A Computer Reference Manual*, part no. 02100-90001
- *HP 2100S Computer Reference Manual*, part no. 02100-90160

Specific instructions for installing the printed circuit assembly into the computer are contained in the following manuals:

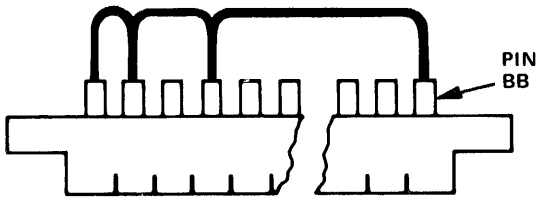
- *HP 21MX Computer Series Operator's Manual*, part no. 02108-90004
- *HP 2100A Computer Installation and Maintenance Manual*, part no. 02100-90002
- *HP 2100S Computer Installation and Maintenance Manual*, part no. 02100-90161

Table 4-1. Jumper Connections for Baud Transfer Rates

BAUD RATE	BIT PATTERN	CONNECT +5V (PIN 8) TO PINS:	CONNECT SIGNAL GROUND (PINS 1, A, 24, OR BB) TO PINS:
External Clock (X16)	0000	–	12,13,14,15
50	0001	14	12,13,15
75	0010	13	12,14,15
110	0011	13,14	12,15
134.5	0100	12	13,14,15
150	0101	12,14	13,15
300	0110	12,13	14,15
600	0111	12,13,14	15
900	1000	15	12,13,14
1200	1001	14,15	12,13
1800	1010	13,15	12,14
2400	1011	13,14,15	12
3600	1100	12,15	13,14
4800	1101	12,14,15	13
7200	1110	12,13,15	14
9600	1111	12,13,14,15	–



DISASSEMBLY AND ASSEMBLY



48-PIN CONNECTOR

1. DISASSEMBLE CABLE CONNECTOR P1 AS SHOWN IN TOP SECTION OF THIS FIGURE.
2. CONNECT PINS 12, 13, 14, AND 15 TO +5 VOLTS (PIN 8) OR SIGNAL GROUND (PINS 1, A, 24, OR BB, AS CONVENIENT) TO PRODUCE THE SELECTED BAUD RATE AS GIVEN IN TABLE 4-1. USE INSULATED WIRE AND CONNECT ONE PIN TO THE NEXT (OF THE SAME LEVEL: +5V OR GND) UNTIL ALL THE APPROPRIATE PINS ARE CONNECTED TOGETHER. REFER TO BOTTOM SECTION OF THIS FIGURE.

Figure 4-1. Baud Rate Jumper Instructions

4-7. Cable Installation

Connector P1 on the cable assembly connects to the asynchronous communications interface PCA. Be sure to position the connector in the proper direction on the PCA as described in manuals referenced above for installing the PCA.

Connector P2 on the cable assembly mates with a connector on the device for which the kit option is intended. The device connectors are located at the rear panel on the HP 2600 and HP 2615. For the HP 2640, the cable connector mates with a printed circuit assembly (PCA) edge connector inside the hinged rear panel of the terminal. The cable connector is polarized so that it can only be inserted onto the PCA connector in one direction.

Wire lists of the four kit cables are given in tables 4-2 through 4-5. Note that not all of the conductors are used in each cable. The cable for the HP 2749B Teleprinter has four conductors, the others have 15 conductors.

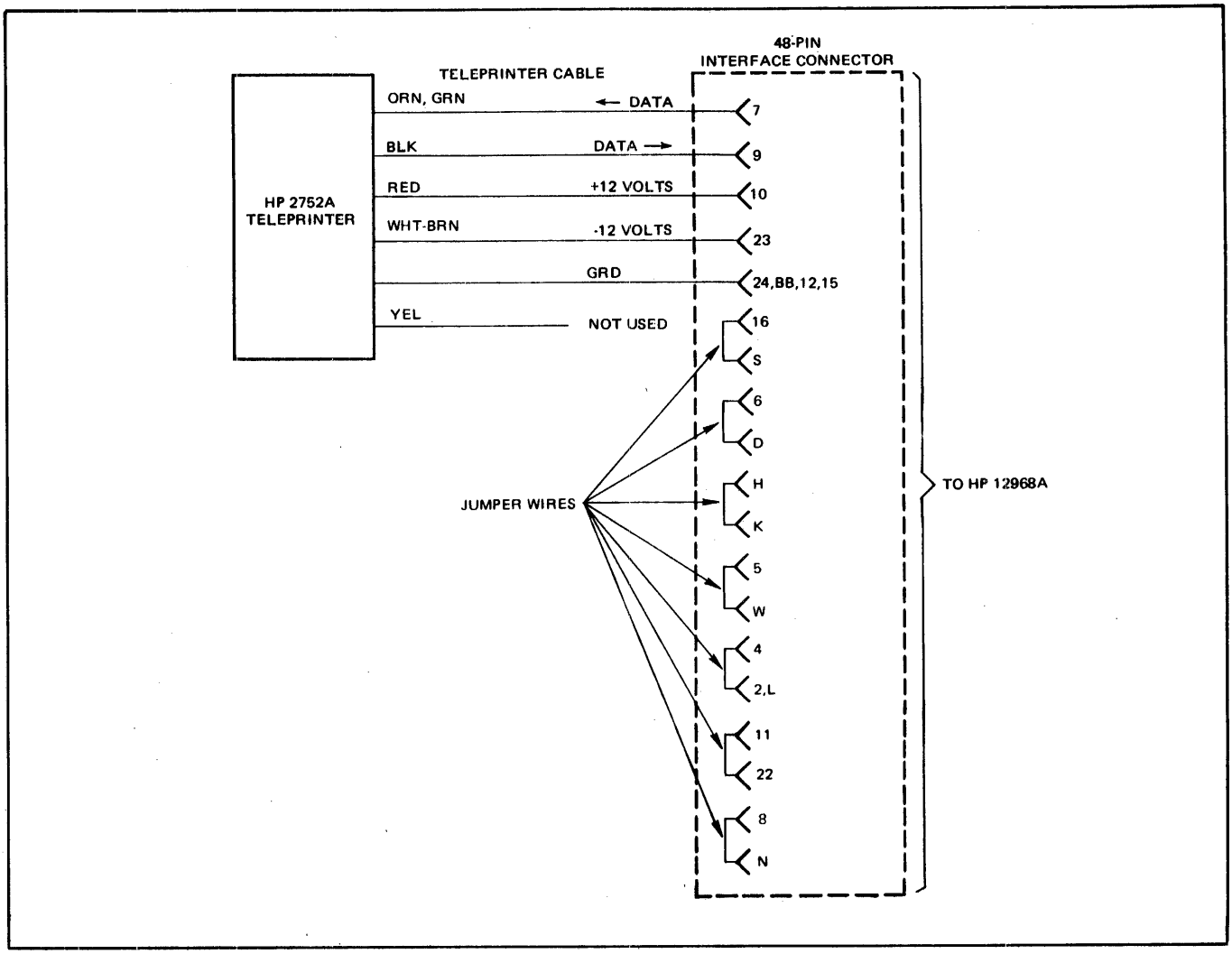


Figure 4-2. Interface Cable Connections for HP 2752A Teleprinter

4-8. Performance Test

After installing the kit, proper operation should be verified by performing the diagnostic test. The test connector supplied with the kit replaces the device and device cable during diagnostic testing. Procedures for performing the diagnostic tests are contained in the *HP 12968A Asynchronous Communications Interface Diagnostic for HP 2100 Series Computers Reference Manual*, part no. 12968-90003.

4-9. Driver Configuration and Installation

Refer to your operating system manual for driver configuration and installation.

4-10. SERVICING

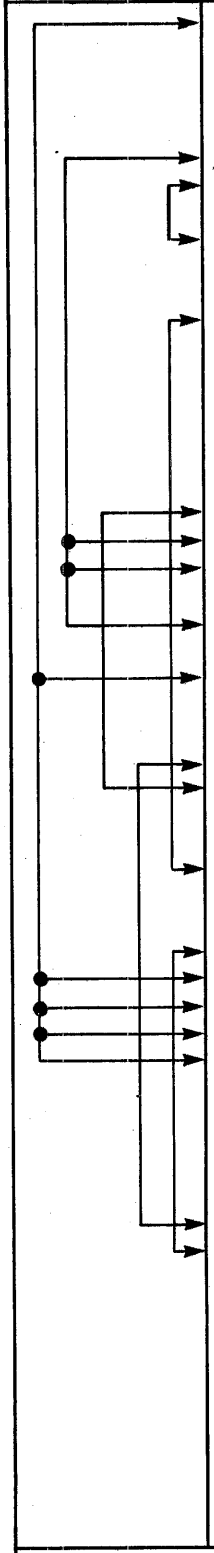
If the kit is not functioning properly, run the diagnostic to verify whether or not the cause is a hardware malfunction. If a hardware problem exists, call the nearest Hewlett-Packard Sales and Service Office and arrange for a board exchange. Continuity checks of the cable can be made using the appropriate wire list (see tables 4-2 through 4-5).

Table 4-2. Interface Cable (HP 2600 and HP 2615 Terminals), part no. 12966-60004, Wire List

HOOD CONNECTOR P1 JUMPERS	(PCA) P1 PIN	SIGNAL NAME (SEE NOTE)	(DEVICE) P2 PIN	WIRE COLOR	RS-232-C CIRCUIT	SIGNAL SOURCE
	A	Signal Ground (EIA)	7	GRN	AB	Common
	B	F				
	C	CA Inhibit				
	D	Transmit Data (EIA)	3	BRN	BA	Intfc
	E	Request to Send (EIA)			CA	
	F	Data Terminal Ready (EIA)			CD	
	H	Ext Freq				
	J	F/4				
	K	F/8				
	L	F/16				
	M	F/2				
	N	P/Ext				
	P	BSBA				
	R	Ext Clock	16	WHT/BLK		Device
	S	Received Data (EIA)	2	BLK	BB	Device
	T	Secondary Line Sig Det (EIA)			SCF	
	U	(spare) (EIA)				
	V	Secondary Receive Data (EIA)			SBB	
	W	BSCA				
	X	Clear to Send (EIA)			CB	
	Y	Data Set Ready (EIA)			CC	
	Z	Ring Indicator (EIA)			CE	
	AA	Receive Line Sig Det (EIA)			CF	
	BB	Signal Ground				
	1	Signal Ground				
	2	CCNT 7				
	3	SXX (Secondary Chan) (EIA)			SBA/SCA	
	4	BSCF				
	5	SIN				
	6	Xmit Data In				
	7	TTY OUT				
	8	+5 volts				
	9	TTY IN				
	10	+12 volts	5,6	ORN,YEL		Intfc
	11	UCLK0				
	12	CLKP2				
	13	CLKP1				
	14	CLKP0				
	15	CLKP3				
	16	Recd Data Out				
	17	BSBB				
	18	DIAG				
	19	Spare				
	20	Run Disable				
	21	BSXX				
	22	UCLK				
	23	-12 volts				
	24	Signal Ground				
	—		4	RED		
	—		8	BLU		
	—		12	VIO		
	—		15	WHT		
	—		17	WHT/BRN		
	—		19	WHT/RED		
	—		20	WHT/ORN		
	—		22	WHT/YEL		

Note: Signals identified by "(EIA)" after the signal name operate at signal levels specified by EIA Standard RS232C (i.e., OFF < -3V, ON > +3V). All other signals operate at TTL logic levels (i.e., approximately, OFF < +1V, ON > +1.5V).

Table 4-3. Interface Cable (HP 2640 Terminal), part no. 12966-60008 , Wire List



HOOD CONNECTOR P1 JUMPERS	(PCA) P1 PIN	SIGNAL NAME (SEE NOTE)	(DEVICE) P2 PIN	WIRE COLOR	RS-232-C CIRCUIT	SIGNAL SOURCE
	A	Signal Ground (EIA)	H	GRN	AB	Common
	B	F				
	C	CA Inhibit				
	D	Transmit Data (EIA)	C	RED	BA	Intfc
	E	Request to Send (EIA)			CA	
	F	Data Terminal Ready (EIA)			CD	
	H	Ext Freq				
	J	F/4				
	K	F/8				
	L	F/16				
	M	F/2				
	N	P/Ext				
	P	BSBA				
	R	Ext Clock	L	BLU		Device
	S	Received Data (EIA)	B	BRN	BB	Device
	T	Secondary Line Sig Det (EIA)			SCF	
	U	(spare) (EIA)				
	V	Secondary Receive Data (EIA)			SBB	
	W	BSCA				
	X	Clear to Send (EIA)			CB	
	Y	Data Set Ready (EIA)			CC	
	Z	Ring Indicator (EIA)	D	BRN/WHT	CE	Device
	AA	Receive Line Sig Det (EIA)				
	BB	Signal Ground				
	1	Signal Ground				
	2	CCNT 7				
	3	SXX (Secondary Chan) (EIA)	E,J	ORN	SBA/SCA	Intfc
	4	BSCF				
	5	SIN				
	6	Xmit Data In				
	7	TTY OUT				
	8	+5 volts				
	9	TTY IN				
	10	+12 volts				
	11	UCLK0				
	12	CLKP2				
	13	CLKP1				
	14	CLKP0				
	15	CLKP3				
	16	Recd Data Out				
	17	BSBB				
	18	DIAG				
	19	Spare				
	20	Run Disable				
	21	BSXX				
	22	UCLK				
	23	-12 volts				
	24	Signal Ground				

Note: Signals identified by "(EIA)" after the signal name operate at signal levels specified by EIA Standard RS232C (i.e., OFF $<-3V$, ON $>+3V$). All other signals operate at TTL logic levels (i.e., approximately, OFF $<+1V$, ON $>+1.5V$).

Table 4-4. Interface Cable (Modem), part no. 12966-60006, Wire List

HOOD CONNECTOR P1 JUMPERS	(PCA) P1 PIN	SIGNAL NAME (SEE NOTE)	(DEVICE) P2 PIN	WIRE COLOR	RS-232-C CIRCUIT	SIGNAL SOURCE
	A	Signal Ground (EIA)	7	GRN	AB	Common
	B	F				
	C	CA Inhibit				
	D	Transmit Data (EIA)	2	BLK	BA	Intfc
	E	Request to Send (EIA)	4	RED	CA	Intfc
	F	Data Terminal Ready (EIA)	20	WHT/ORN	CD	Intfc
	H	Ext Freq				
	J	F/4				
	K	F/8				
	L	F/16				
	M	F/2				
	N	P/Ext				
	P	BSBA				
	R	Ext Clock				
	S	Received Data (EIA)	3	BRN	BB	Device
	T	Secondary Line Sig Det (EIA)	12	VIO	SCF	Device
	U	(spare) (EIA)				
	V	Secondary Receive Data (EIA)			SBB	
	W	BSCA				
	X	Clear to Send (EIA)	5	ORN	CB	Device
	Y	Data Set Ready (EIA)	6	YEL	CC	Device
	Z	Ring Indicator (EIA)	22	WHT/YEL	CE	Device
	AA	Receive Line Sig Det (EIA)	8	BLU	CF	Device
	BB	Signal Ground				
	1	Signal Ground				
	2	CCNT 7				
	3	SXX (Secondary Chan) (EIA)		GRA	SBA/SCA	
	4	BSCF				
	5	SIN				
	6	Xmit Data In				
	7	TTY OUT				
	8	+5 volts				
	9	TTY IN				
	10	+12 volts				
	11	UCLK0				
	12	CLKP2				
	13	CLKP1				
	14	CLKP0				
	15	CLKP3				
	16	Recd Data Out				
	17	BSBB				
	18	DIAG				
	19	Spare				
	20	Run Disable				
	21	BSXX				
	22	UCLK				
	23	-12 volts				
	24	Signal Ground				
	–		15	WHT		
	–		16	WHT/BLK		
	–		17	WHT/BRN		
	–		19	WHT/RED		

Note: Signals identified by "(EIA)" after the signal name operate at signal levels specified by EIA Standard RS232C (i.e., OFF < -3V, ON > +3V). All other signals operate at TTL logic levels (i.e., approximately, OFF < +1V, ON > 1.5V).

Table 4-5. Interface Cable (HP 2749B Teleprinter), part no. 12966-60007, Wire List

HOOD CONNECTOR P1 JUMPERS	(PCA) P1 PIN	SIGNAL NAME (SEE NOTE)	(DEVICE) P2 PIN	WIRE COLOR	RS-232-C CIRCUIT	SIGNAL SOURCE
	A	Signal Ground (EIA)	1,7	BLK	AB	Common
	B	F				
	C	CA Inhibit				
	D	Transmit Data (EIA)	3	YEL	BA	Intfc
	E	Request to Send (EIA)			CA	
	F	Data Terminal Ready (EIA)			CD	
	H	Ext Freq				
	J	F/4				
	K	F/8				
	L	F/16				
	M	F/2				
	N	P/Ext				
	P	BSBA				
	R	Ext Clock				
	S	Received Data (EIA)	2	RED	BB	Device
	T	Secondary Line Sig Det (EIA)			SCF	
	U	(spare) (EIA)				
	V	Secondary Receive Data (EIA)			SBB	
	W	BSCA				
	X	Clear to Send (EIA)			CB	
	Y	Data Set Ready (EIA)			CC	
	Z	Ring Indicator (EIA)			CE	
	AA	Receive Line Sig Det (EIA)			CF	
	BB	Signal Ground				
	1	Signal Ground				
	2	CCNT 7				
	3	SXX (Secondary Chan) (EIA)			SBA/SCA	
	4	BSCF				
	5	SIN				
	6	Xmit Data In				
	7	TTY OUT				
	8	+5 volts				
	9	TTY IN				
	10	+12 volts				
	11	UCLK0				
	12	CLKP2				
	13	CLKP1				
	14	CLKP0				
	15	CLKP3				
	16	Recd Data Out				
	17	BSBB				
	18	DIAG				
	19	Spare				
	20	Run Disable				
	21	BSXX				
	22	UCLK				
	23	−12 volts				
	24	Signal Ground				

Note: Signals identified by "(EIA)" after the signal name operate at signal levels specified by EIA Standard RS232C (i.e., OFF < −3V, ON > +3V). All other signals operate at TTL logic levels (i.e., approximately, OFF < +1V, ON > +1.5V).

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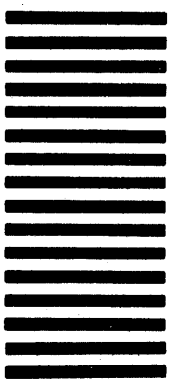

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