OPERATING AND SERVICE MANUAL

12926A

PAPER TAPE PUNCH SUBSYSTEM

(FOR THE HP 2100-SERIES COMPUTER SYSTEMS)

HP 12926A PAPER TAPE PUNCH SUBSYSTEM

GENERAL DESCRIPTION

The HP 12926A Paper Tape Punch Subsystem consists of all the equipment and software required to provide tape punching and spooling capability for the HP 2100-Series Computer Systems. Subsystem components consist of a 10-1/2-inch (266.7-mm) rack-mountable tape punch and accessories, an interface PCA, an interface cable, an interface test connector, and requisite software which includes diagnostics.

The subsystem provides five- or eight-track, 1-inch (25.4-mm) tape punching at a rate of 75 characters per second. Tape composition may be paper, plastic, or mylar. An additional feature of this subsystem is the switch-selectable power sources and frequencies. Power is selectable at 100-, 115-, 220-, and 240-volt positions. The usable frequency range is 47.5 to 100 hertz. Additional details regarding subsystem performance and capabilities are provided in the operating and service manuals supplied with the subsystem.

EQUIPMENT SUPPLIED

The following equipment and documentation are supplied with the subsystem:

- HP 2895B Tape Punch.

- HP 12597A-005 Tape Punch Interface Kit.

- *HP 2895B Tape Punch Operating and Service Manual*, part no. 02895-90008.

- *HP 12597A-005 Tape Punch Interface Kit Operating and Service Manual*, part no. 12597-90025.

ACCESSORIES

The following accessories are provided with each tape punch:

- Chad box with magnetic catch.
- Paper Tape, part no. 9280-0063.
- Chad hose and fittings.
- Power cable.
- Cardboard take-up bobbins (2).
- Rack mount assembly, 02895-60002, light gray; 02895-60003, moss gray.

1

HEWLETT *hp* PACKARD

OPERATING AND SERVICE MANUAL

12597A-005

TAPE PUNCH INTERFACE KIT

(FOR 2114, 2115, AND 2116 COMPUTERS)

Card Assembly
12597-6001, Rev 832

Note

This manual should be retained with Volume Three of
the Hewlett-Packard computer system documentation.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual provides general information, installation instructions, programming instructions, theory of operation, maintenance information, and replaceable parts information for the Hewlett-Packard (HP) 12597A-005 Tape Punch Interface Kit (see figure 1-1).

1-3. DESCRIPTION.

1-4. GENERAL.

1-5. The HP 12597A-005 Tape Punch Interface Kit is an option to the standard HP 12597A 8-Bit Duplex Register Interface Kit. This kit supplies the interfacing requirements for the addition of an HP 2895A Tape Punch to the user's computer system.

1-6. INTERFACE KIT CONTENTS.

1-7. The HP 12597A-005 Tape Punch Interface Kit consists of the following:

    a. Tape Punch Interface card (part no. 12597-6001).
    b. Interface cable (part no. 12597-60061).
    c. Test connector, 24-pin (part no. 1251-0332).
    d. Operating and service manual (part no. 12597-90025).

1-8. SPECIFICATIONS.

1-9. Table 1-1 lists the specifications for the HP 12597A-005 Tape Punch Interface Kit.

Table 1-1. Tape Punch Interface Kit Specifications

CHARACTERISTICS	SPECIFICATIONS

Output Levels:
   "1" state
   "0" state
	
	 0 to +0.5V, 12 mA sink maximum
	 +12V, 10K source

Input Levels:
   "1" state
   "0" state
	
	 0 to +0.5V, 12 mA sink maximum
	 +8V

Computer Power Supply
 Current Requirements:
   +12V
   −12V
   −2V
   +4.5V
	
	 0.05A
	 0.02A
	 0.05A
	 0.75A

Interface Card
 Dimensions:
   Width
   Height
	
	 7-3/4 inches (196,8 mm)
	 8-11/16 inches (220,7 mm)

Interface Kit Weight:
   Net Weight
   Shipping Weight
	
	 18 oz (675 gm)
	 4 lb (1,8 kg)
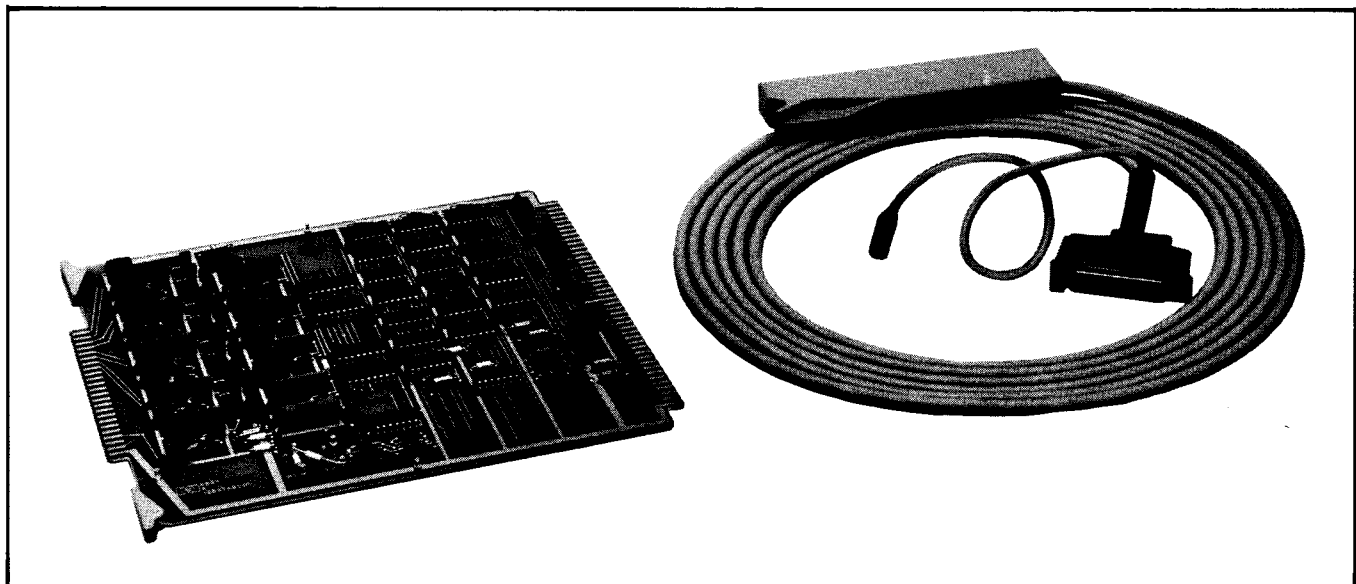
2158-1

Figure 1-1. HP 12597A-005 Tape Punch Interface Kit

1-10.   IDENTIFICATION.

1-11.   This operating and serivce manual is identified on the title page by interface kit designation and nomenclature, card assembly part number and revision code, manual part number, and publication date. Refer to the information presented in the following paragraphs and ensure that this manual applies to the equipment being serviced.

1-12.   Hewlett-Packard uses five digits and a letter (00000A) for standard interface kit designations and a 3-digit suffix (-000) for options to standard interface kits. If the designation of your kit does not agree with that on the title page of this manual, there are differences between your kit and the kit described in this manual. The appropriate manual or manual supplement is available at the nearest HP Sales and Service Office listed at the back of this manual.

1-13.   Printed-circuit cards used as plug-in card assemblies or fixed wired assemblies are identified by a letter, a revision code, and a division code stamped on the card (e.g., A-832-6). The letter identifies the version of the etched trace pattern on the unloaded card. The revision code (three middle digits) refers to the electrical characteristics of the loaded card. The division code (last digit) identifies the Hewlett-Packard division which manufactured the card. If the revision code on the printed-circuit card does not agree with the revision code shown on the title page of this manual, there are differences between your card and the card described in this manual. These differences are described in manual supplements available at the nearest HP Sales and Service Office.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2.   This section provides information on unpacking and inspection, reshipment, preparation for installation, and installation of the tape punch interface kit.

2-3. UNPACKING AND INSPECTION.

2-4.   If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the kit contents are unpacked. Inspect the card for damage (cracks, broken parts, etc.). If the card is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and packing material for the carrier's inspection. The HP Sales and Service Office will arrange for repair or replacement of the damaged card without waiting for any claims against the carrier to be settled.

2-5. RESHIPMENT.

2-6.   If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the model number of the kit.

2-7.   Pack the item in the original factory packing material if available. If the original material is not available, standard factory packing material can be obtained from the nearest Hewlett-Packard Sales and Service Office.

2-8.   If standard factory packing material is not used, wrap the item in Air Cap TH-240 cushioning (manufactured by Sealed Air Corporation, Hawthorne, New Jersey), or equivalent, and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to ensure careful handling.

2-9. PREPARATION FOR INSTALLATION.

2-10.   CURRENT REQUIREMENTS.

2-11.   The interface card in this kit obtains its operating current from the computer power supply. Before installing this interface card, determine the current requirements of this card in combination with all other interface or accessory cards already installed in the computer. Volume Three of the computer system documentation describes the procedure for calculating the total current requirements and lists the currents available from the computer. If the total current requirements exceed the limitations of the computer power supply, a Hewlett-Packard power supply extender unit or I/O extender unit must be used. See table 1-1 for the current requirements of the tape punch interface card.

2-12.   INTERFACE CARD JUMPERS.

2-13.   There are several jumper wires on the tape punch interface card. These jumpers are used to adapt the card for use with I/O devices other than the tape punch. Before installing the interface card, ensure that the jumpers are positioned as described in table 2-1 (see figure 5-2 for physical location of the jumpers).

Table 2-1. Interface Card Jumper Positions

JUMPER	POSITION
W1	A
W2	A
W3	Connected
W4	Connected
W5	Connected
W6	Connected
W7	Connected
W8	Disconnected
W9	Disconnected

2-14. INSTALLATION.

2-15.   To install the tape punch interface kit, proceed as follows:

a. Turn off power at the computer and the tape punch.

b. Insert the interface card in the computer I/O card slot corresponding to the desired select code (address).

c. Turn on power to the computer and perform the diagnostic program procedure, part number 12554-90023, located in the Manual of Diagnostics.

d. Turn off power at the computer and connect the interconnecting cable between the interface card and the tape punch. Then connect the POWER lamp wiring portion of interconnecting cable to the POWER lamp on the front panel of the tape punch drawer. (See figure 2-1.)

e. Perform the diagnostic program procedure, part number 02753-90092, located in the Manual of Diagnostics to verify proper operation of the interface card in conjunction with the tape punch.
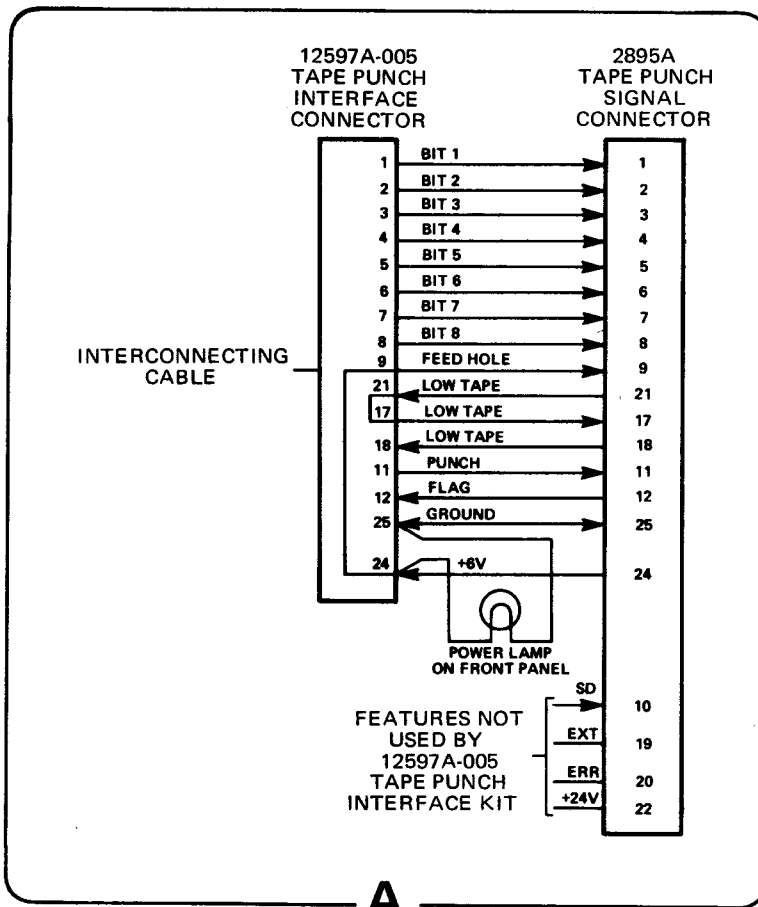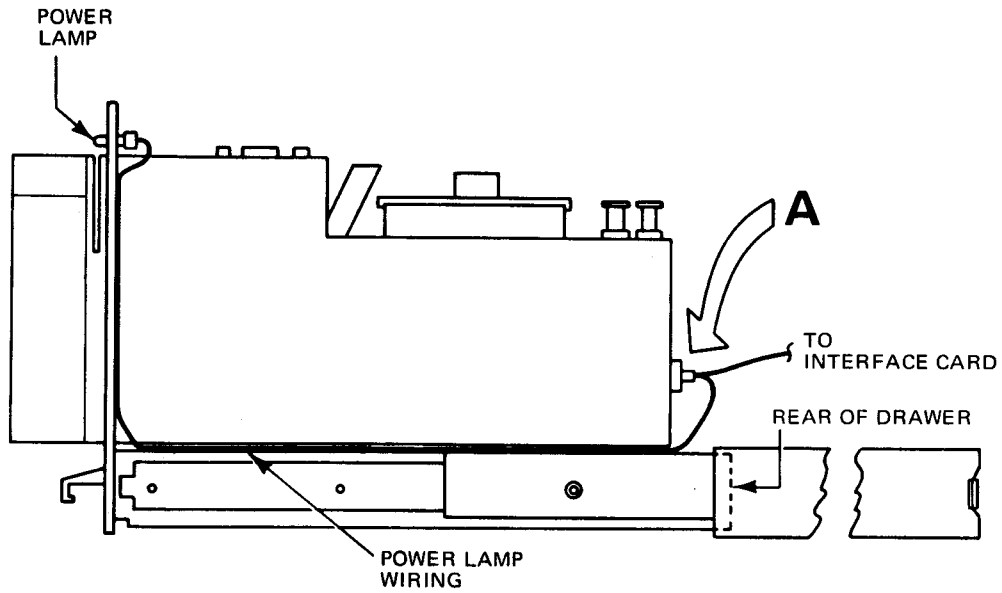
Figure 2-1. Power Lamp Wiring Diagram

SECTION III

PROGRAMMING

3-1. INTRODUCTION.

3-2.   This section provides programming information for the HP 12597A-005 Tape Punch Interface Kit.

3-3. GENERAL INFORMATION.

3-4.   The tape punch interface card provides command logic to start the tape punch and flag logic to signal the computer when the tape punch has completed a punch operation. An output storage register provides buffer storage for transfer of eight bits of data from the computer to the tape punch, and an input storage register provides buffer storage for transfer of status information from the tape punch to the computer. The following paragraphs provide information required to program the operation of the command, flag, input register, and output register logic on the tape punch interface card.

3-5. I/O ADDRESSING.

3-6.   Through the use of the I/O extender options, some HP computers are capable of operating up to 56 I/O devices. To provide orderly I/O operations, each I/O card slot is assigned a 2-digit octal address called a select code.

All program instructions calling for action by the tape punch interface card must include the select code of the interface card.

3-7. SAMPLE PROGRAM.

3-8.   Table 3-1 provides a sample program showing the use of the tape punch interface card to operate an HP 2895A Tape Punch. The sample is an actual program listing prepared on an HP computer system using the HP Assembler software package.

3-9.   Under control of the sample program, the tape punch will punch 100 8-bit data words as read from 100 consecutive memory locations. Prior to each data word transfer, the tape punch status will be checked for a possible low-tape condition. Low-tape is indicated by a logic 1 in bit 5 of the tape punch status word. To supply the I/O addressing requirements, the tape punch has been arbitrarily assigned a select code of 16 octal.

3-10.   The sample program does not use the computer interrupt system. If the interrupt system has been previously enabled, a CLF 00 instruction must be included at the start of the program to turn off the interrupt system.

Table 3-1. Sample Program

```
0001                        ASMB,A,B,L,T
0002*
0003*    THIS IS A SAMPLE PROGRAM DEMONSTRATING THE OPERATION OF THE
0004*    HP 12597A-005 TAPE PUNCH INTERFACE. UNDER CONTROL OF THIS
0005*    PROGRAM, THE TAPE PUNCH WILL PUNCH 100, 8-BIT CHARACTERS AS READ
0006*    FROM 100 CONSECUTIVE MEMORY LOCATIONS. THE TAPE PUNCH STATUS
0007*    WILL BE CHECKED PRIOR TO EACH OUTPUT OPERATION AND AN HLT 66B
0008*    DISPLAYED IF THE STATUS WORD INDICATES TAPE SUPPLY IS LOW.
0009*
0010   00400              ORG 400B    ASSIGN PROGRAM STARTING LOCATION
0011*                                  OF 400 OCTAL.
0012   00400 060432  START LDA CNT     INITIALIZE COUNT-TO-100 COUNTER
0013   00401 070430        STA CNTR     AND STORE IN LOCATION CNTR.
0014   00402 060433        LDA ITBL     GET STARTING ADDRESS OF DATA TO BE
0015   00403 070431        STA PNTR      PUNCHED AND STORE IN PNTR.
0016*
0017   00404 014417  CHECK JSB STAT     JUMP TO SUBROUTINE THAT WILL GET
0018*                                  STATUS WORD.
0019   00405 010434        AND MASK     REMOVE INSIGNIFICANT STATUS BITS.
0020   00406 050435        CPA LOW      IS TAPE SUPPLY LOW?
0021   00407 102066        HLT 66B      YES. HALT COMPUTER.
0022   00410 160431        LDA PNTR,I   NO. GET CHARACTER TO BE PUNCHED.
0023*
0024   00411 014422        JSB PUNCH    JUMP TO SUBROUTINE THAT WILL PUNCH
0025*                                  A CHARACTER.
0026   00412 034431        ISZ PNTR     MOVE POINTER TO NEXT CHARACTER.
0027   00413 034430        ISZ CNTR     INCREMENT COUNTER. 100 OPERATIONS?
0028   00414 024404        JMP CHECK    NO. CHECK STATUS AND PUNCH AGAIN.
0029   00415 102077        HLT 77B      YES. NORMAL END OF PROGRAM.
0030   00416 024400        JMP START    TO RERUN PROGRAM PUSH "RUN".
0031*
0032*  ** SUBROUTINE ** THIS ROUTINE GETS STATUS WORD FROM PUNCH.
0033*
0034   00417 000000  STAT  NOP
0035   00420 102516        LIA TPIF     PUT STATUS WORD IN A-REGISTER.
0036   00421 124417        JMP STAT,I   RETURN TO PROGRAM WITH STATUS WORD.
0037*
0038*  ** SUBROUTINE ** THIS ROUTINE PUNCHES CHARACTER.
0039*
0040   00422 000000  PUNCH NOP
0041   00423 102316        SFS TPIF     IS TAPE PUNCH READY?
0042   00424 024423        JMP *-1      NO. WAIT.
0043   00425 102616        OTA TPIF     YES. PUT CHARACTER IN INTERFACE
0044*                                  REGISTER.
0045   00426 103716        STC TPIF,C   START TAPE PUNCH.
0046   00427 124422        JMP PUNCH,I  RETURN TO PROGRAM.
0047*
0048*    CONSTANT AND STORAGE INFORMATION.
0049*
0050   00430 000000  CNTR  BSS 1        RESERVE ONE LOCATION FOR COUNTER.
0051   00431 000000  PNTR  BSS 1        RESERVE ONE LOCATION FOR POINTER.
0052   00432 177634  CNT   DEC -100     INITIAL COUNT FOR COUNTER.
0053   00433 000122  ITBL  OCT 122      STARTING LOCATION OF DATA BLOCK.
0054   00016           TPIF EQU 16B     TAPE PUNCH INTERFACE HAS S.C. 16B.
0055   00434 000040  MASK  OCT 40
0056   00435 000040  LOW   OCT 40       SAMPLE "LOW TAPE" STATUS WORD.
0057*
0058                       END START
**  NO ERRORS*
```

SECTION IV

THEORY OF OPERATION

4-1. INTRODUCTION.

4-2.   This section provides the theory of operation for the 12597-6001 Tape Punch Interface Card.

4-3. FUNCTIONAL THEORY OF OPERATION.

4-4.   Figure 4-1 is a flow chart showing the functional theory of operation for the tape punch interface card. The programmed instructions shown in the shaded area of the flow chart are the same as those used in the subroutine portions of the sample program (table 3-1) in Section III of this manual.

4-5.   The first programmed instruction (LIA) transfers the tape punch status word from the input storage register to the computer A-register. The status word consists of a single bit (bit 5) that becomes a logic 1 when the tape punch paper tape supply is low. The status word is then checked by software. The computer will normally be programmed to halt if a low-tape condition exists.

4-6.   Assuming that the status word does not indicate low tape (bit 5 is logic 0), the next step is to test the state (set or clear) of the Flag FF. If the Flag FF is in the clear state, the punch is busy from some previously programmed punch operation. If the Flag FF is set, the punch is ready to accept data for a new punch operation. An SFS instruction tests the Flag FF. If the Flag FF is clear, the next instruction (JMP *-1) causes the computer to again execute the SFS instruction. This loop continues until the Flag FF is set. An SFS instruction when the Flag FF is set causes the computer to skip the JMP *-1 instruction and continue with the program.

4-7.   The computer can also be signaled when the Flag FF is set via interrupt signals (FLG and IRQ) or a Service Request (SRQ) signal. These signals are discussed in detail in paragraphs 4-30 through 4-35.

4-8.   The next programmed instruction (OTA) transfers the data word that is to be punched from the computer A-register to the output storage register on the interface card. The tape punch now has data available and requires only that it be commanded to punch the data on paper tape.

4-9.   A combined Set Control and Clear Flag (STC xx,C) instruction sets the Control and Command FFs, and clears the Flag Buffer and Flag FFs. The Command FF provides a Punch signal which starts the operation of the tape punch. This completes the programmed instructions required for a punch operation. The computer is now free to perform other operations while the tape punch is completing its operation.

4-10.   The tape punch provides a Flag signal when it completes the punch operation. As shown by figure 4-1, the Flag signal sets the Flag Buffer FF and clears the Command FF. At the next computer time T2, an ENF signal sets the Flag FF to indicate that the tape punch is again ready for a new punch operation.

4-11. DETAILED THEORY OF OPERATION.

4-12.   GENERAL.

4-13.   Diagrams that support the detailed theory of operation for the tape punch interface card include the timing diagram in this section (figure 4-4) and the interface card logic diagram (figure 5-2) in Section V of this manual.

4-14.   For an index of signals at the 86-pin edge of the interface card, see Volume Three of the computer system documentation. For an index of signals at the 48-pin edge of the interface card, see table 5-2 in Section V of this manual.

4-15.   Logic levels between the computer and the interface card, and logic levels internal to the card are positive-true. The term "true" refers to a signal level of about +3.5 volts and "false" refers to a level of about ground. These signal levels vary somewhat depending on the integrated circuit package involved. Detailed signal level information for the various integrated circuit packages is provided in figure 5-1 in Section V of this manual.

4-16.   Signal levels to and from the tape punch are ground-true and are detailed in table 1-1 in Section I of this manual.

4-17.   POWER-ON LOGIC.

4-18.   When power is initially applied to the computer or the computer PRESET switch is pressed, the computer supplies a POPIO and a CRS signal to the interface card. The POPIO signal sets the Flag Buffer FF and the CRS signal clears the Control and Command FFs. The Control FF, in the clear state, disables the interrupt circuitry on the interface card. A cleared Command FF ensures that the tape punch will be receiving a false Punch signal. At time T2, the computer generates an ENF signal which is gated with the set-side of the Flag Buffer FF to set the Flag FF. The ENF signal also ensures that the IRQ FF is in the clear state.

4-19.   The initial operating conditions of the tape punch interface card after power-on are: Flag Buffer and Flag FFs set; Control, Command, and IRQ FFs cleared.
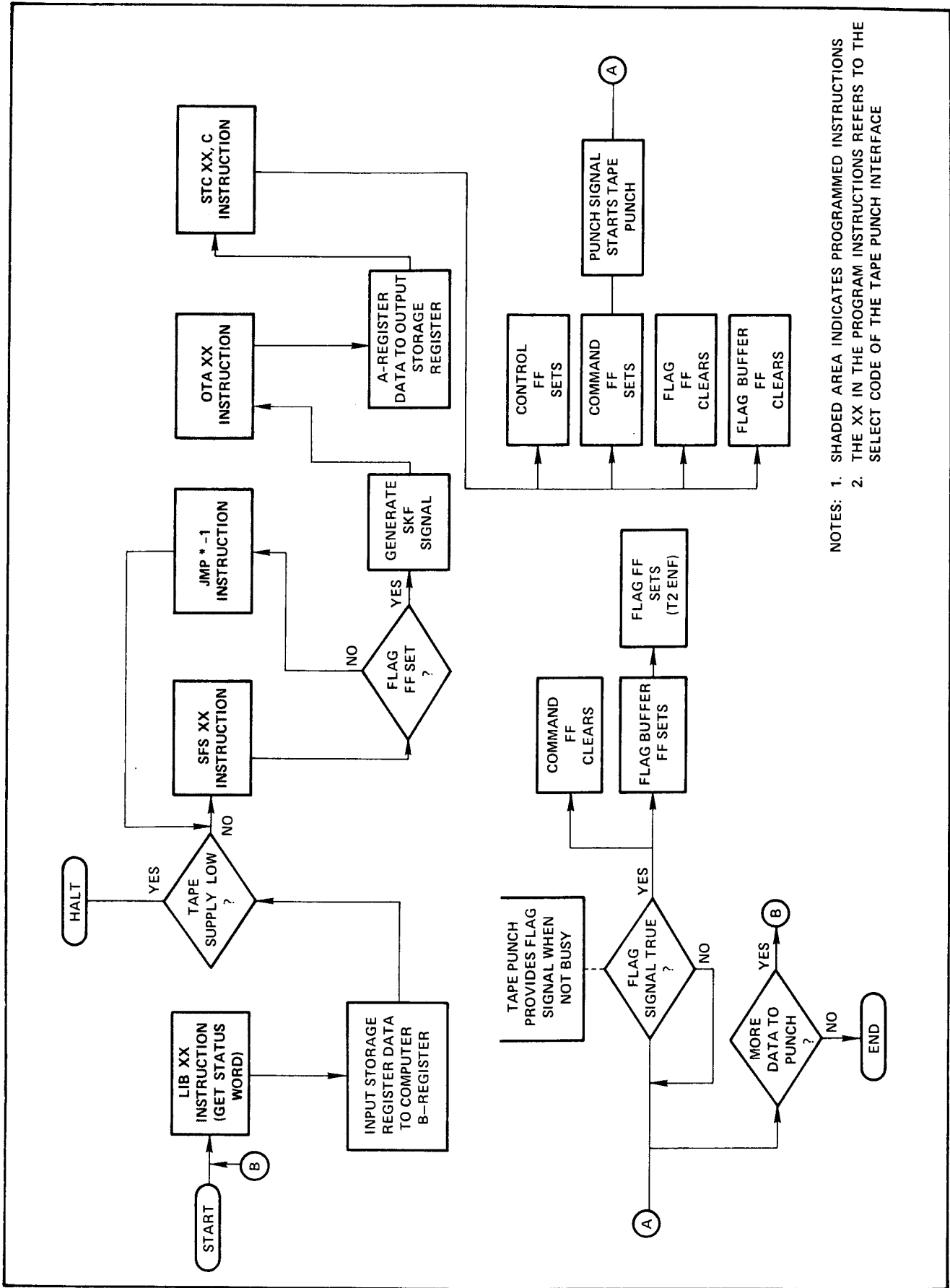
Figure 4-1. Tape Punch Interface Card Functional Operation Flow Chart

NOTES: 1. SHADED AREA INDICATES PROGRAMMED INSTRUCTIONS
2. THE XX IN THE PROGRAM INSTRUCTIONS REFERS TO THE SELECT CODE OF THE TAPE PUNCH INTERFACE

4-20. INPUT REGISTER LOGIC.

4-21.   The input storage register on the tape punch inter-face card stores the tape punch status word. Although a full eight bits are transferred to the computer, the status word consists of a single significant bit (bit 5) and, as a logic 1, indicates that the paper tape supply is low. When the interface cable is connected, a ground is applied to pin 21 of the 48-pin edge of the card. This provides a continuous enable to the input storage register so that any change in the status bit is immediately loaded into the bit 5 flip-flop of the register.

4-22.   A programmed LIA or LIB instruction addressed to the tape punch interface card provides true SCM, SCL, IOG, and IOI signals. The IOI signal strobes the status word onto the IOBI lines to the computer A- or B-register.

4-23. FLAG LOGIC.

4-24.   Before transferring a data word from the computer to the tape punch, the computer must be assured that the punch is not busy operating from some previous data trans-fer. The state of the Flag FF (set or clear) provides this information to the computer. If the tape punch has not been previously operated, and the state of the Flag FF has not been altered by some programmed instruction, the Flag FF will be in the set state due to the action described in paragraph 4-18. If the tape punch is busy, the Flag FF will be in the clear state due to a programmed Clear Flag instruction described in paragraph 4-39.

4-25.   At this point, the discussion of the flag logic assumes that the tape punch is busy and the Flag FF is in the clear state.

4-26.   When the tape punch completes an operation, it provides a Flag signal to the interface card. The interface card converts the Flag signal to a 300 nanosecond pulse which clears the Command FF and sets the Flag Buffer FF.

4-27.   The timing of the Flag logic at this point is depen-dent upon the timing of the tape punch and is not related to computer timing. An ENF signal, supplied by the computer every machine cycle at time T2, is gated with the output of the Flag Buffer FF (now in the set state) to set the Flag FF. This action synchronizes the effect of the Flag signal with the computer timing by allowing the Flag FF to be set only at computer time T2.

4-28.   When the Flag FF is in the set state, the interface card flag logic responds by generating SKF, FLG and IRQ, or SRQ signals to indicate to the computer that the tape punch is ready to accept a data transfer. The following paragraphs describe how these signals are generated and how they affect computer operation.

4-29.   SKIP-ON-FLAG SIGNAL. If the computer is programmed to wait for the Flag FF to be set (for example, an SFS instruction followed by a JMP *-1 instruction as shown in Figure 4-1), the resulting SFS signal gated with a true signal from the set side of the Flag FF generates an SKF signal. This causes the computer to skip the next instruction (in this case JMP *-1) and proceed with the program. Figure 4-2 illustrates the generation of an SKF signal by the interface card. Notice that an SKF signal can also be generated when the Flag FF is in the clear state by programming an SFC instruction. Either way, the state of the Flag FF is being tested and the computer must be programmed to respond accordingly.
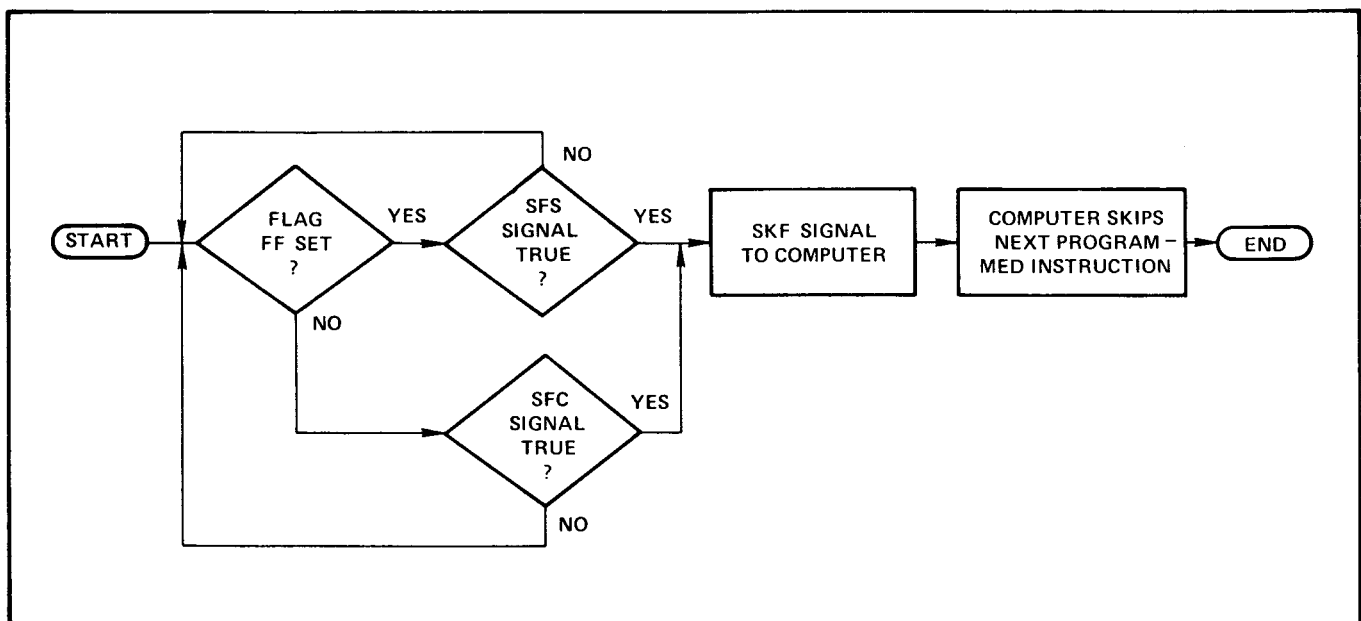

Figure 4-2. Skip-On-Flag Signal Generation Flow Chart

4-30. INTERRUPT SIGNALS. If the computer interrupt system has been enabled by an STF 00 instruction, the computer can be doing work in the main program rather than waiting for the Flag FF to be set. Figure 4-3 illustrates the functions involved in an interrupt operation. To interrupt the main program when the tape punch is ready, the following conditions must be met:

a. Control FF set (paragraph 4-39).
b. Flag Buffer FF set (paragraph 4-26).
c. Flag FF set (paragraph 4-27).
d. IEN signal true (interrupt system enabled).
e. PRH signal true (no higher priority interrupts).

4-31. When all of these conditions are established, an SIR signal from the computer at time T5 sets the IRQ FF which generates true FLG and IRQ signals. These signals are used by the computer I/O control and addressing circuits to generate an interrupt signal. The next machine cycle will then be an interrupt phase (phase 4).

4-32. At time T2 during the interrupt phase, an ENF signal clears the IRQ FF. An SIR signal again sets the IRQ FF at time T5 if the PRH signal is still true. The FLG and IRQ signals this time are used by the computer I/O control and addressing circuits to encode the interrupt address.

4-33. The next machine cycle is controlled by the instruction located at the interrupt address in memory. During this machine cycle, an IAK signal at time T1 clears the Flag Buffer FF and an ENF signal at time T2 clears the IRQ FF. The Flag FF remains set to inhibit lower priority interrupts by providing a false PRL signal. A CLF instruction must be programmed to clear the Flag FF and enable lower priority interrupts just before returning to the main program.

4-34. SERVICE REQUEST SIGNAL. If the computer is equipped with the Direct Memory Access (DMA) option, and if the DMA circuits have been initialized, an 8-bit word can be transferred directly from memory to the tape punch
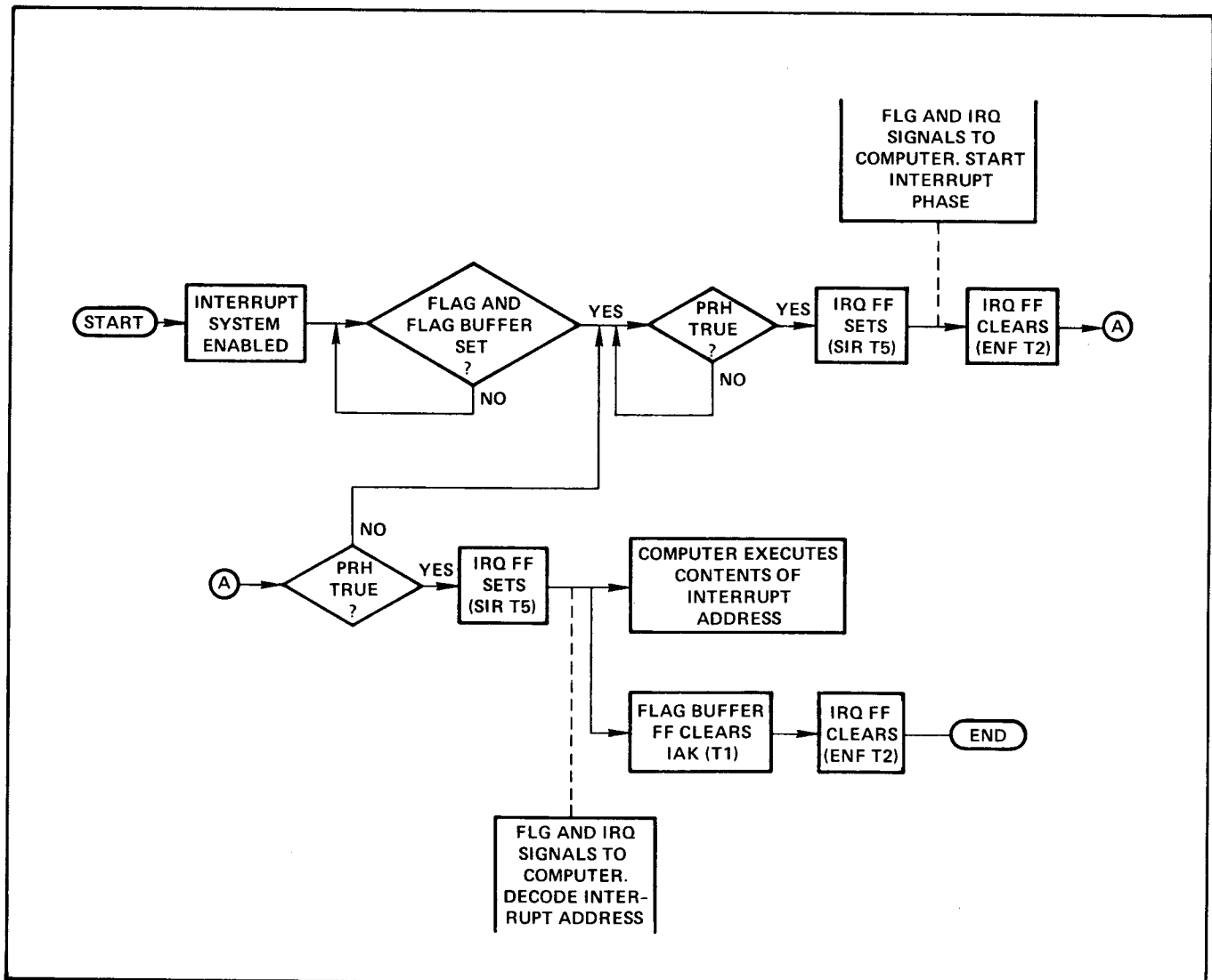

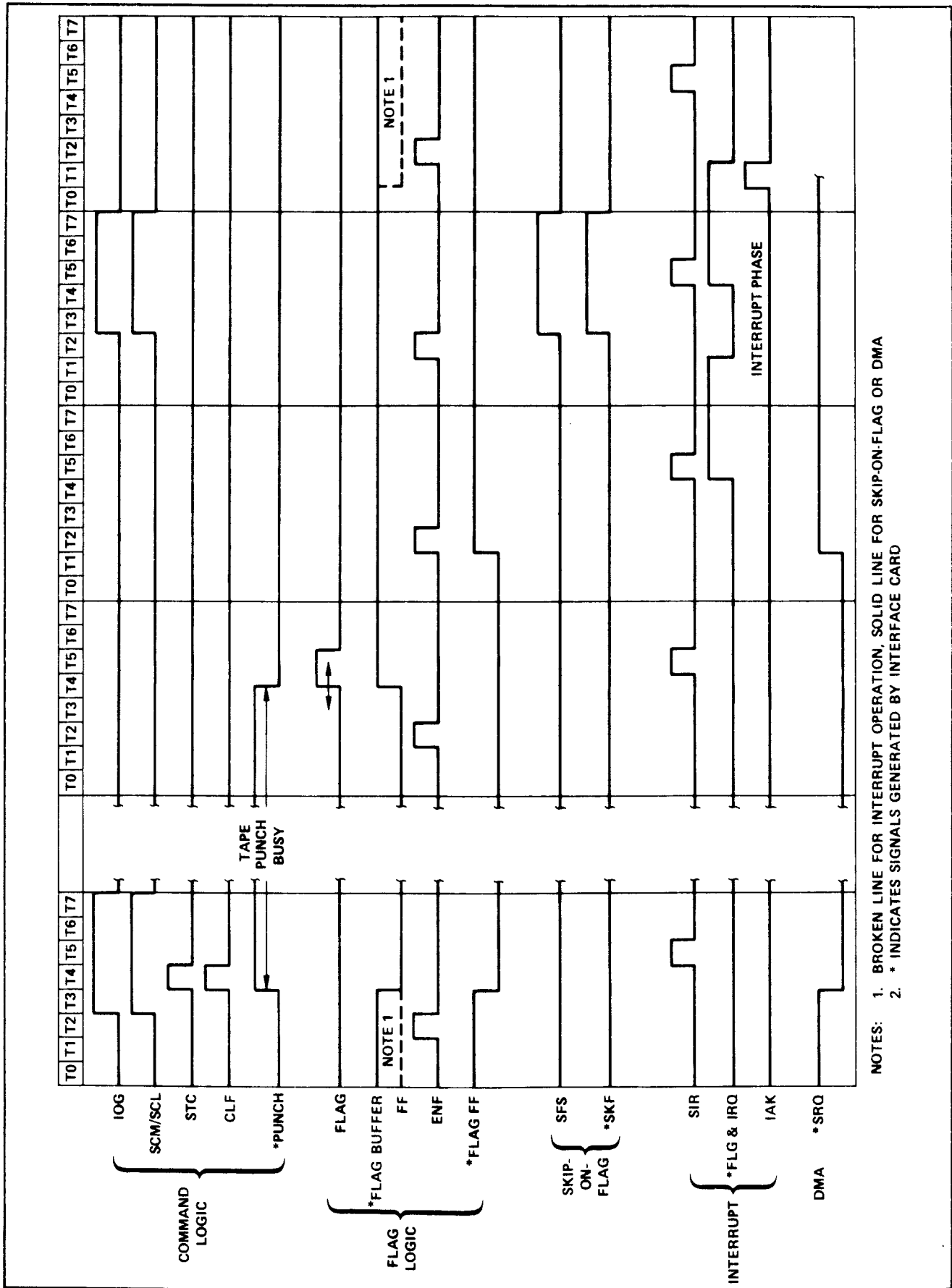Figure 4-3. Interrupt Operation Flow Chart

Figure 4-4. Overall Timing Diagram

NOTES: 1. BROKEN LINE FOR INTERRUPT OPERATION, SOLID LINE FOR SKIP-ON-FLAG OR DMA
        2. * INDICATES SIGNALS GENERATED BY INTERFACE CARD

in one machine cycle. When the Flag FF on the interface card is set, the interface card supplies a true SRQ signal which enables the DMA circuits. The DMA circuits suspend the computer program for one machine cycle and provide the necessary signals to transfer the 8-bit word and start the tape punch.

4-35.   Refer to the applicable DMA option operating and service manual for detailed information on DMA controlled I/O operations.

4-36.   OUTPUT REGISTER LOGIC.

4-37.   After the computer has been signaled that the tape punch is not busy, the output data word can be transferred to the interface card output storage register. This is accomplished with an OTA or OTB instruction (addressed to the tape punch interface card) in the main program or in an interrupt subroutine. Signals to the interface card resulting from an OTA or OTB instruction are SCM, SCL,

IOG, and IOO. The IOO signal latches the 8-bit data word into the output storage register.

4-38.   COMMAND LOGIC.

4-39.   With data in the interface card output storage register, the tape punch need only be commanded to punch the data on tape. An STC xx,C (combined Set Control and Clear Flag) instruction with the select code (xx) of the tape punch interface sets the Control and Command FFs and clears the Flag and Flag Buffer FFs. The set side of the Command FF is level-amplified and sent to the tape punch as a Punch signal.

4-40.   The set side of the Control FF provides one of the enabling signals for the interrupt logic (see paragraph 4-30). Flag and Flag Buffer FFs in the clear state enable the interface card flag logic. The tape punch will now punch the 8-bit data word and return a Flag signal when it is ready for another punch operation.

SECTION V

MAINTENANCE

5-1.   INTRODUCTION.

5-2.   This section provides maintenance information for the tape punch interface kit. Included are preventive maintenance instructions, troubleshooting instructions, and maintenance data consisting of a signal index for the interface cable (table 5-2), information pertaining to the integrated circuit characteristics and pin connections (figure 5-1), replaceable parts list for the interface card (table 5-1), and an interface card parts location and logic diagram (figure 5-2).

5-3.   PREVENTIVE MAINTENANCE.

5-4.   Preventive maintenance for the tape punch interface kit should be performed along with the preventive maintenance routines for the computer system.

5-5.   Preventive maintenance consists of running the combined tape punch and tape punch interface diagnostic program procedure, part number 02753-90092, as described in the Manual of Diagnostics. Also, visually inspect the interface card, cable, and connectors for burned or broken components, connections, and insulation.

5-6.   TROUBLESHOOTING.

5-7.   Troubleshooting the tape punch interface card is accomplished by running the diagnostic program procedure, part number 12554-90023, as described in the Manual of Diagnostics and analyzing error halts as they occur.

5-8.   Use the maintenance data contained in this section to further isolate faulty components.

Table 5-1. Tape Punch Interface Card Replaceable Parts List

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C8,18	0140-0198	Capacitor, Fxd, Mica, 200 pF, 5%	28480	0140-0198
C9 thru C16	0140-0191	Capacitor, Fxd, Mica, 56 pF, 5%	28480	0140-0191
C17	0140-0192	Capacitor, Fxd, Mica, 68 pF, 5%	28480	0140-0192
C19,22	0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	28480	0160-0153
C20,21	0160-0154	Capacitor, Fxd, My, 2200 pF, 10%	28480	0160-0154
C23 thru C32	0180-0197	Capacitor, Fxd, Elect, 2.2 uF, 10%, 20 VDCW	56289	150D225X9020A2
CR9 thru CR17	1901-0040	Diode, Si, 30 mA, 30 WV	07263	FDG 1088
MC15,36	1820-0068	Integrated Circuit, TTL	56289	USN7410A
MC16,26,47	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC17,25,27,37,46,57,86,94	1820-0054	Integrated Circuit, TTL	56289	USN7400A
MC34,44,64,74	1820-0301	Integrated Circuit, TTL	01295	SN7475N
MC35	1820-0069	Integrated Circuit, TTL	56289	USN7420A
MC45,55,65,75	1820-0974	Integrated Circuit, CTL	07263	SL4817
MC56,66	1820-0071	Integrated Circuit, TTL	56289	USN7440A
Q1 thru Q18	1854-0215	Transistor, Si, NPN	04713	SPS3611
R1 thru R8,18	0757-0417	Resistor, Fxd, Flm, 562 ohms, 1%, 1/8W	28480	0757-0417
R9 thru R17	0757-0442	Resistor, Fxd, Flm, 10.0k, 1%, 1/8W	28480	0757-0442
R19,22,23	0698-3445	Resistor, fxd, Flm, 348 ohms, 1%, 1/8W	28480	0698-3445
R20,30,31	0698-3440	Resistor, Fxd, Flm, 196 ohms, 1%, 1/8W	28480	0698-3440
R21	0698-0082	Resistor, Fxd, Flm, 464 ohms, 1%, 1/8W	28480	0698-0082
R24,25,28,32	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	28480	0757-0280
R26,27	0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8W	28480	0757-0401
R29	0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094
R101,103,105,107,109,111,113, 115,117,118	1810-0008	Resistor Network (6 fxd flm resistors)	28480	1810-0008
R119 thru R122	1810-0020	Resistor Network (7 fxd flm resistors)	28480	1810-0020
W1 thru W7	8159-0005	Jumper Wire	28480	8159-0005

Figure 5-1. Integrated Circuit Pin Connections and Characteristics
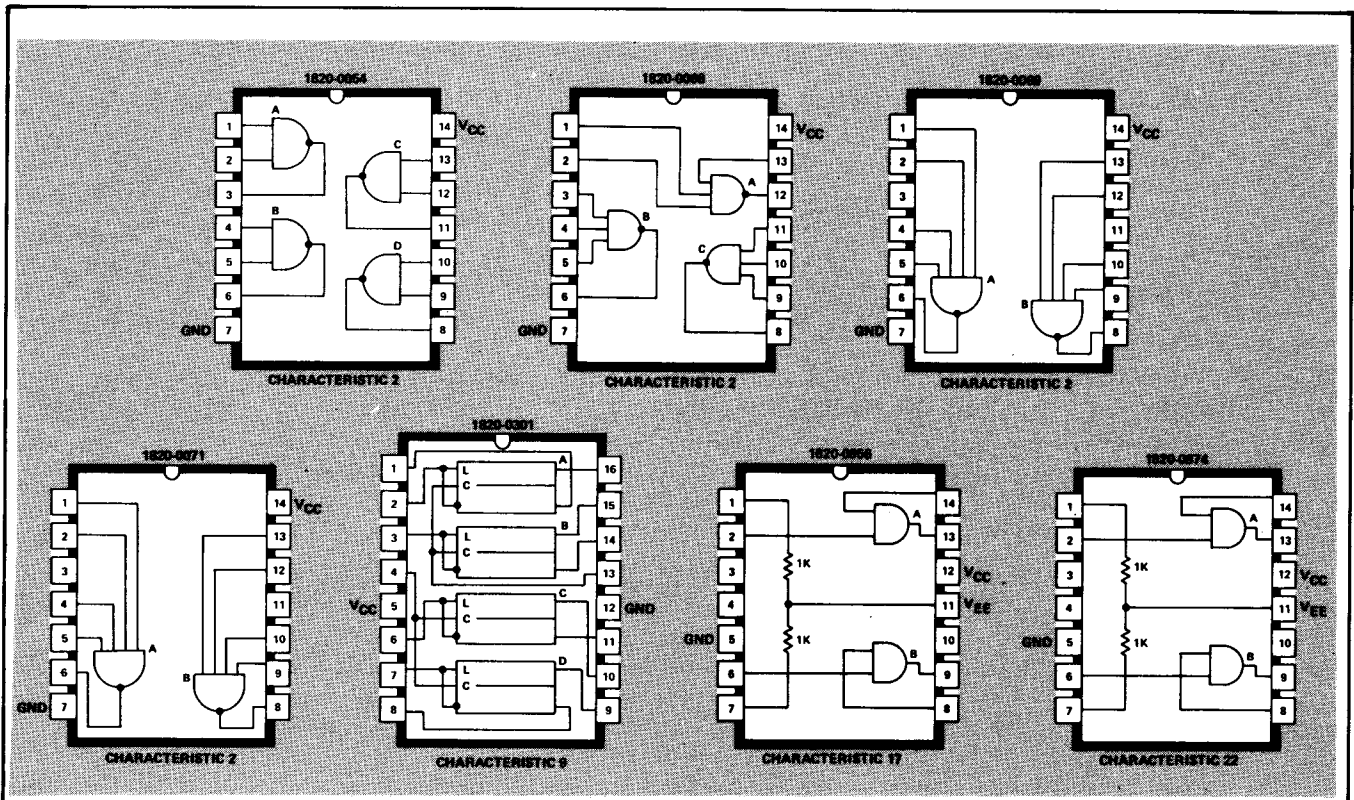
CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN INPUT ACTS AS:	MAXIMUM PROPAGATION DELAY	
	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)		TO LOGIC 1 (NANOSECONDS)	TO LOGIC 0 (NANOSECONDS)
2	+2.0	+0.8	+2.4	+0.4	1	29	15*
9	+2.0*	+0.8	+2.4	+0.4	1	40	25
17	+1.25	+0.5	+2.25	−0.36	0	18	18
22	+1.5	+0.4	+2.2	−0.3	0	24	24

NOTE:
   *Required pulse widths; clock 30 ns min., data 75 ns min.

Table 5-2. Interface Cable Signal Index

48-PIN CONNECTOR, PIN NO.	TAPE PUNCH CONNECTOR, PIN NO.	SIGNAL
A	1	Bit 1 (CH 1)
B	2	Bit 2 (CH 2)
C	3	Bit 3 (CH 3)
D	4	Bit 4 (CH 4)
E	5	Bit 5 (CH 5)
F	6	Bit 6 (CH 6)
H	7	Bit 7 (CH 7)
J	8	Bit 8 (CH 8)
AA	11	Punch (PI)
6	18	Low Tape (TL)
23	12	Flag (PR)
24,BB	25	Ground (0V)

NOTE: Pins 9 and 24, and pins 7 and 21 are jumpered in the tape punch connector of the interconnecting cable. (See figure 2-1.)

12597A-005

86-PIN
CONNECTOR

48-PIN
CONNECTOR

OMIT G,I,O,&Q
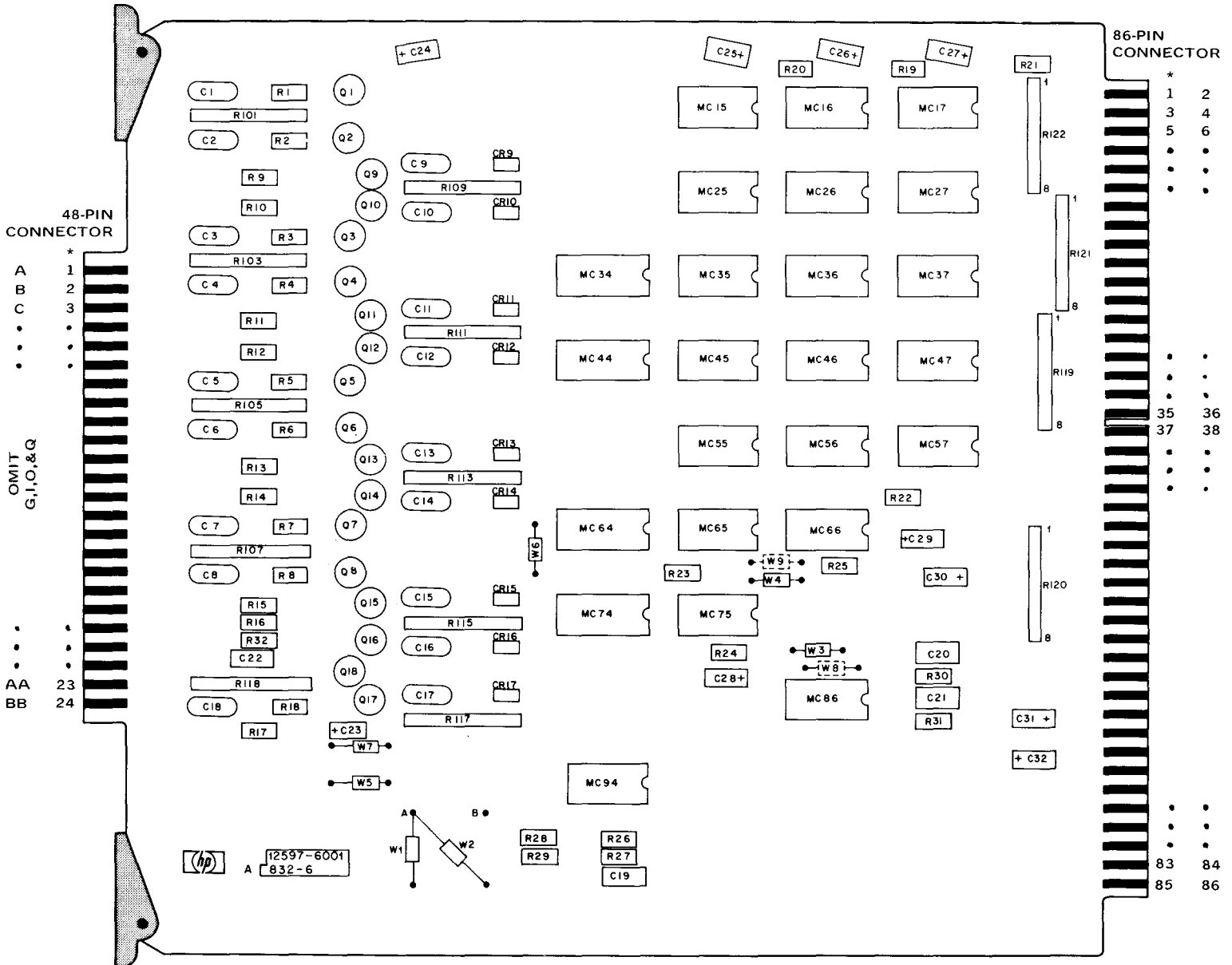
*DENOTES COMPONENT SIDE OF CARD FOR 48- AND 86-PIN
CONNECTOR DESIGNATIONS.

TAPE PUNCH INTERFACE CARD (12597-6001, REV 832)
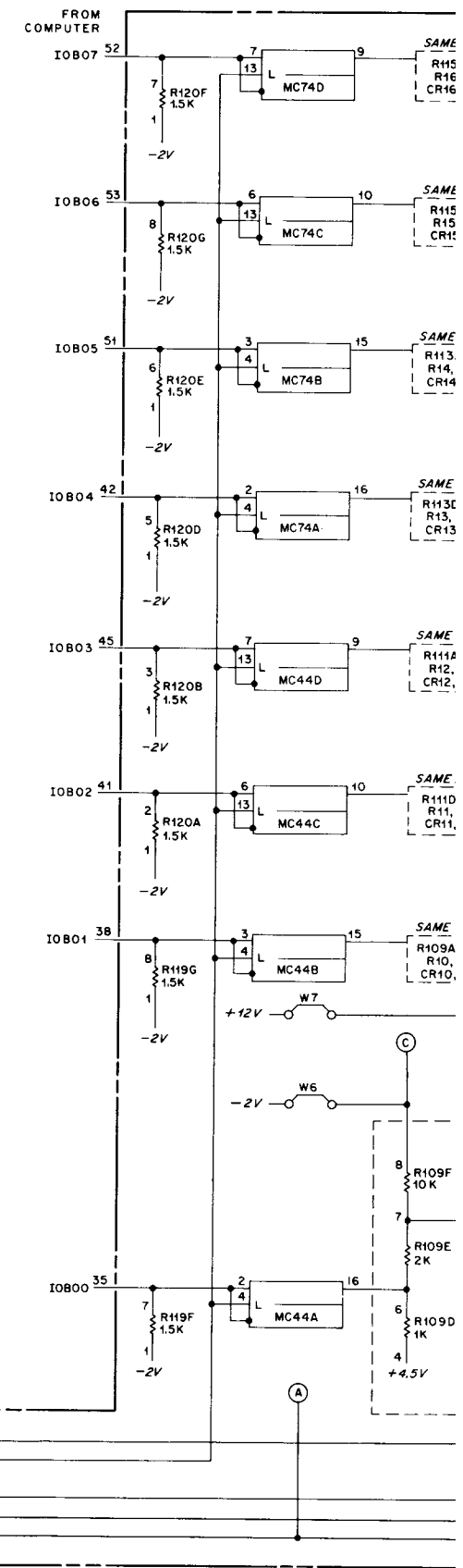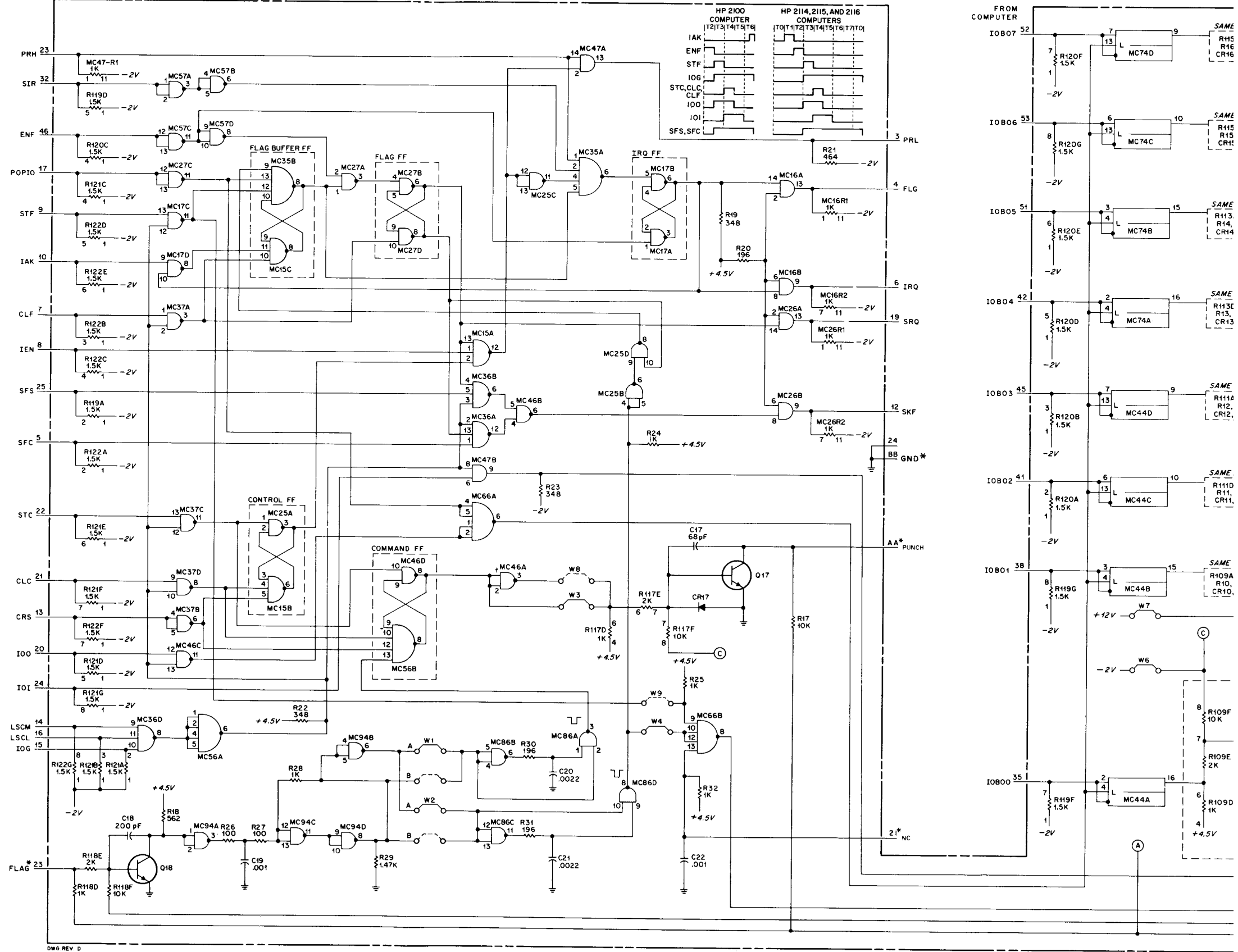
Figure 5-2. Tape Punch Interface Card Parts Location Diagram and Logic Diagram

SECTION VI

REPLACEABLE PARTS

6-1.   INTRODUCTION.

6-2.   This section provides information for ordering replacement parts for the 12597A-005 Tape Punch Interface Kit. Table 6-1 is a numerical listing of all replaceable parts in the interface kit.

6-3.   An interface card replaceable parts list (table 5-1) and parts location diagram (figure 5-2) are provided in Section V of this manual.
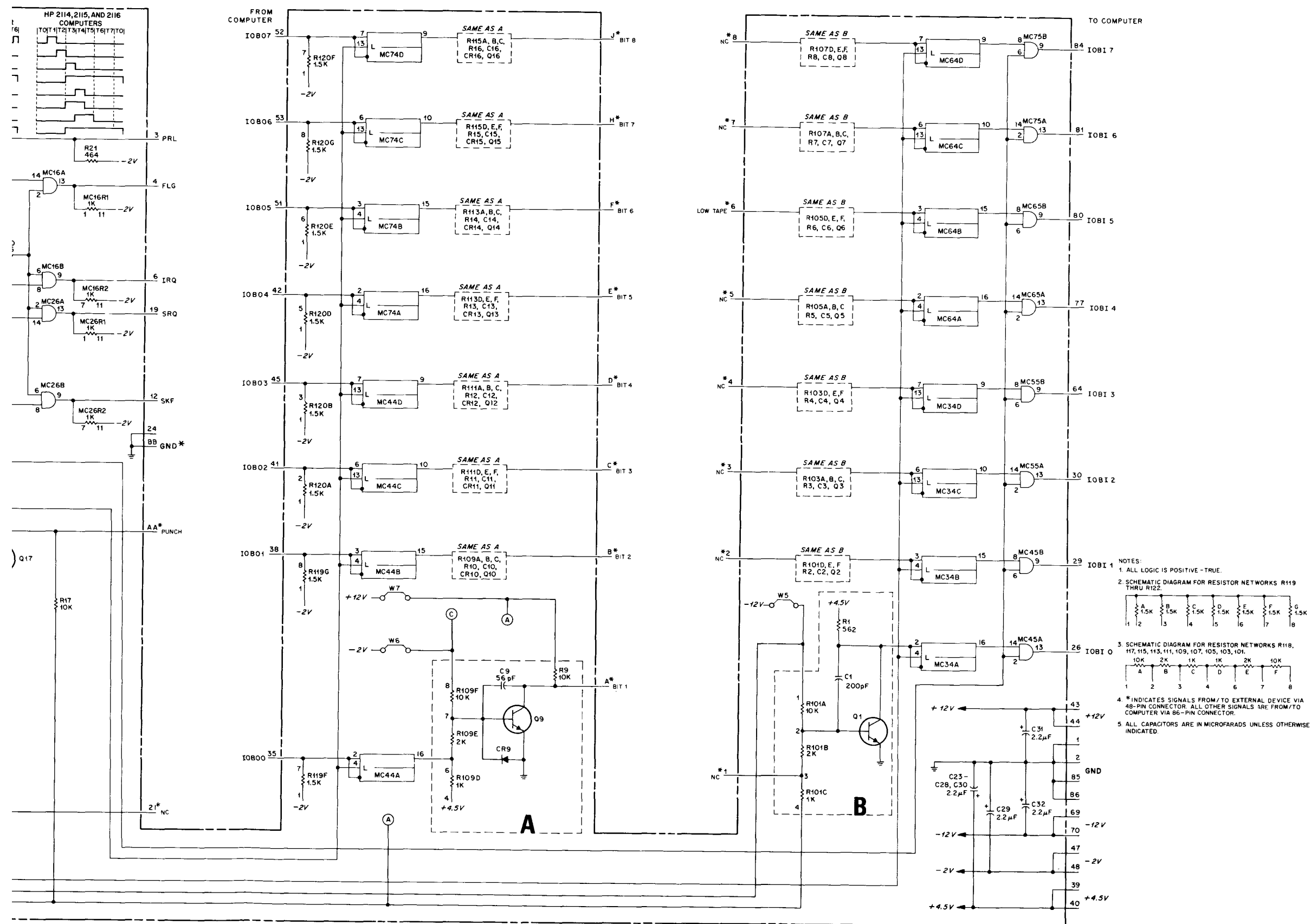
6-4.   Tables 5-2 and 6-1 list the following information for each replaceable part:

a.   Reference designation of the part (table 5-1 only). (Refer to table 6-2 for an explanation of the abbreviations used in the REFERENCE DESIGNATION column.)

b.   Hewlett-Packard part number.

c.   Description of the part. (Refer to table 6-2 for an explanation of the abbreviations used in the DESCRIPTION column.)

d.   A five digit code that corresponds to the manufacturer of the part. (Refer to table 6-3 for a code list of manufacturers.)

e.   Manufacturers part number.

f.   Total quantity (TQ) of each part used in the kit or assembly (table 6-1 only).

6-5.   ORDERING INFORMATION.

6-6.   To order replacement parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office. Refer to the list at the back of this manual for addresses. Specify the following information for each part ordered:

a.   Identification of the instrument, kit or assembly containing the part (refer to paragraph 1-8).

b.   Hewlett-Packard part number for each part.

c.   Description of each part.

d.   Circuit reference designation for each part (if applicable).

Table 6-1. Numerical Listing of Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0140-0191	Capacitor, Fxd, Mica, 56 pF, 5%	28480	0140-0191	8
0140-0192	Capacitor, Fxd, Mica, 68 pF, 5%	28480	0140-0192	1
0140-0198	Capacitor, Fxd, Mica, 200 pF, 5%	28480	0140-0198	9
0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	28480	0160-0153	2
0160-0154	Capacitor, Fxd, My, 2200 pF, 10%	28480	0160-0154	2
0180-0197	Capacitor, Fxd, Elect, 2.2 uF, 10%, 20 VDCW	56289	150D225X9020A2	10
0698-0082	Resistor, Fxd, Flm, 464 ohms, 1%, 1/8W	28480	0698-0082	1
0698-3440	Resistor, Fxd, Flm, 196 ohms, 1%, 1/8W	28480	0698-3440	3
0698-3445	Resistor, Fxd, Flm, 348 ohms, 1%, 1/8W	28480	0698-3445	3
0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	28480	0757-0280	4
0757-0401	Resistor, Fxd, Flm, 100 ohms, 1/8W	28480	0757-0401	2
0757-0417	Resistor, Fxd, Flm, 562 ohms, 1%, 1/8W	28480	0757-0417	9
0757-0442	Resistor, Fxd, Flm, 10.0 ohms, 1%, 1/8W	28480	0757-0442	9
0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094	1
1251-0332	Connector, PC	13511	143-024-08 (1158)	1
1810-0008	Resistor Network (6 fxd flm resistors)	28480	1810-0008	10
1810-0020	Resistor Network (7 fxd flm resistors)	28480	1810-0020	4
1820-0054	Integrated Circuit, TTL	56289	USN7400A	8
1820-0068	Integrated Circuit, TTL	56289	USN7410A	2
1820-0069	Integrated Circuit, TTL	56289	USN7420A	1
1820-0071	Integrated Circuit, TTL	56289	USN7440A	2
1820-0301	Integrated Circuit, TTL	01295	SN7475N	4
1820-0956	Integrated Circuit, CTL	07263	SL3459	3
1820-0974	Integrated Circuit, CTL	07263	SL4817	4
1854-0215	Transistor, Si, NPN	04713	SPS3611	18
1901-0040	Diode, Si, 30 mA, 30 WV	07263	FDG 1088	9
8159-0005	Jumper Wire	28480	8159-0005	7
12597-6001	Tape Punch Interface Card	28480	12597-6001	1
12597-60061	Cable	28480	12597-60061	1
12597-90025	Operating and Service Manual	28480	12597-90025	1

UPDATING SUPPLEMENT FOR OPERATING AND SERVICE MANUAL

24 July 1972

MANUAL IDENTIFICATION

Manual Serial No. Prefix: N/A

Manual Printed: MAR 1971

Manual Part Number: 12597-90025

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to adapt the manual to instruments containing production improvements made subsequent to the printing of the manual and to correct manual errors. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

INSTRUMENT CHANGES

Serial No. Prefix	Change

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Rev	Changes

Changes 1 through 12 dated 26 August 1971.
Changes 13 and 14 dated 24 July 1972.

CHANGE	DESCRIPTION

Note: Changes 1 through 12 provide coverage in the manual (part no. 12597-90025) for interfacing the 2895A Tape Punch with a 2100, 2114, 2115, or 2116 Computer.

1   Title page. Change the computer model numbers to read, "(FOR 2100, 2114, 2115, AND 2116 COMPUTERS)".

2   Title page. Change note to read as follows:

Note

This manual should be retained with the applicable computer system documentation.

3   Page 2-1, paragraph 2-15, step "c". Change the diagnostic program procedure part number to read, "(part number 12554-90023 for 2114, 2115, and 2116 Computers or part number 12554-90026 for 2100 Computers)."

4   Page 4-4, paragraph 4-31. Delete the third sentence and change the end of the second sentence to read, " . . . to generate an interrupt request signal."

5   Page 4-4, paragraph 4-32. Change the first sentence to read, "At time T2, after interrupt is initiated, an ENF signal clears the IRQ FF."

6   Page 4-4, paragraph 4-33. Change the second sentence by deleting the words "at time T1".

7   Page 4-4, figure 4-3. Make two deletions in the figure text as follows:

a.   At the upper right-hand side, delete the word PHASE from the annotation symbol. The remaining text reads "FLG AND IRQ SIGNALS TO COMPUTER, START INTERRUPT".

b.   At the lower center, delete "(T1)" from the process symbol so that the remaining text reads "FLAG BUFFER FF CLEARS IAK".

8   Page 4-5, figure 4-4. Add note 3 to the diagram as follows:

3.   This diagram shows interface card operation with 2114, 2115, and 2116 Computers. For operation with 2100 Computers, refer to updating supplement change 9.

9   Figure US-1 of this updating supplement. An overall timing diagram showing operation of the interface card with 2100 Computers is provided in figure US-1.

10   Page 5-1, paragraph 5-7. Change the diagnostic program procedure part number to read, "(part number 12554-90023 for the 2114, 2115, and 2116 Computers and part number 12554-90026 for 2100 Computers)."

11   Page 5-3, figure 5-2. At the top of the schematic diagram toward left-center, delete the waveform diagram and add the following reference.

"Refer to updating supplement change 12".

12   Figure US-2 of this updating supplement. A quick reference timing diagram is provided in figure US-2.
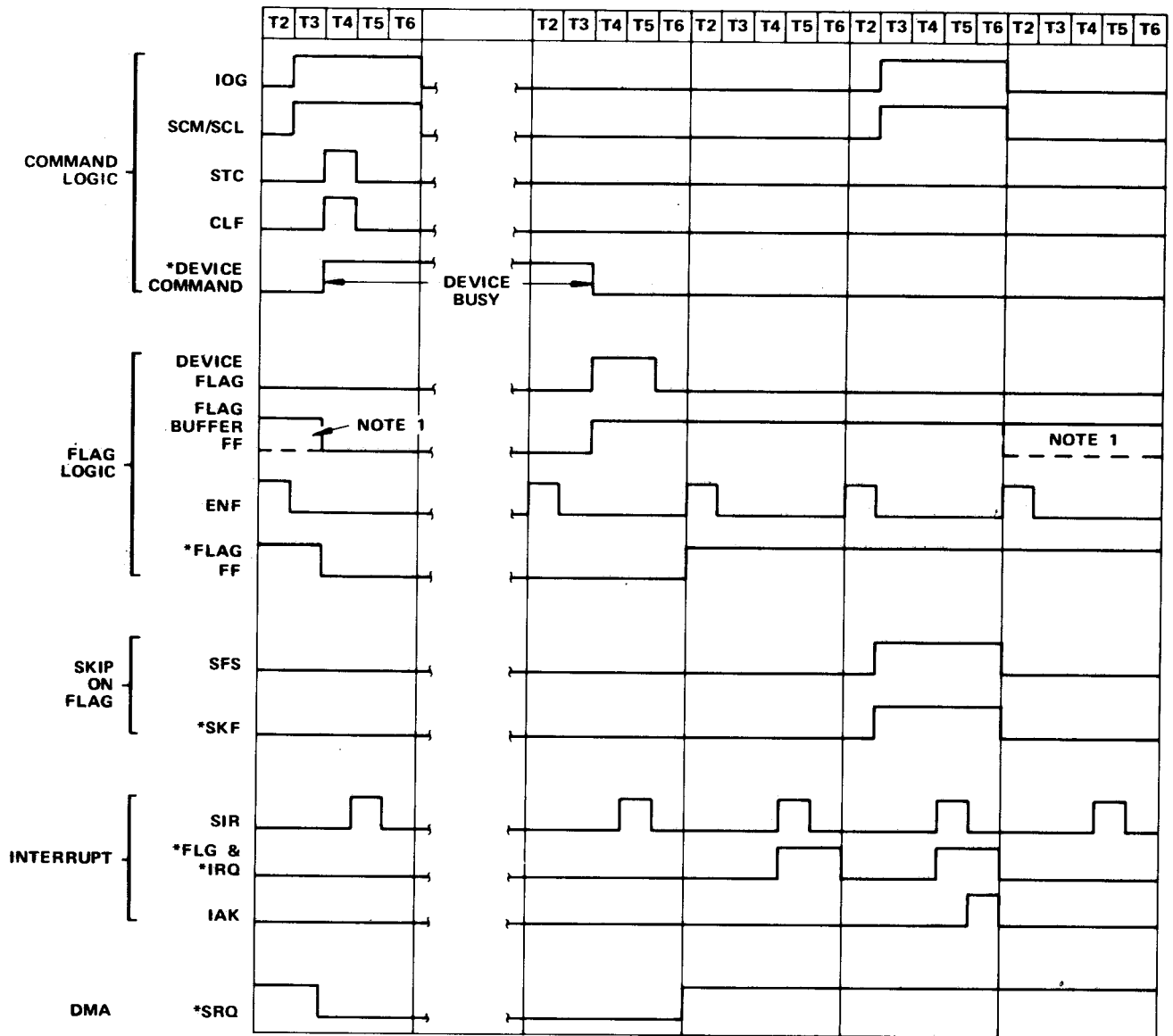
13   Page 1-1, paragraph 1-5. Change the second sentence to read: This kit supplies the interfacing requirements for the addition of an HP 2895A or HP 2895B Tape Punch to the user's computers system.

14   Page 2-2, figure 2-1. Change the Tape Punch model number to read: 2895A/B.

NOTES:
1. BROKEN LINE FOR INTERRUPT OPERATION, SOLID LINE FOR SKIP-ON-FLAG OR DMA.
2. * INDICATES SIGNALS GENERATED BY INTERFACE CARD.

2118-US1

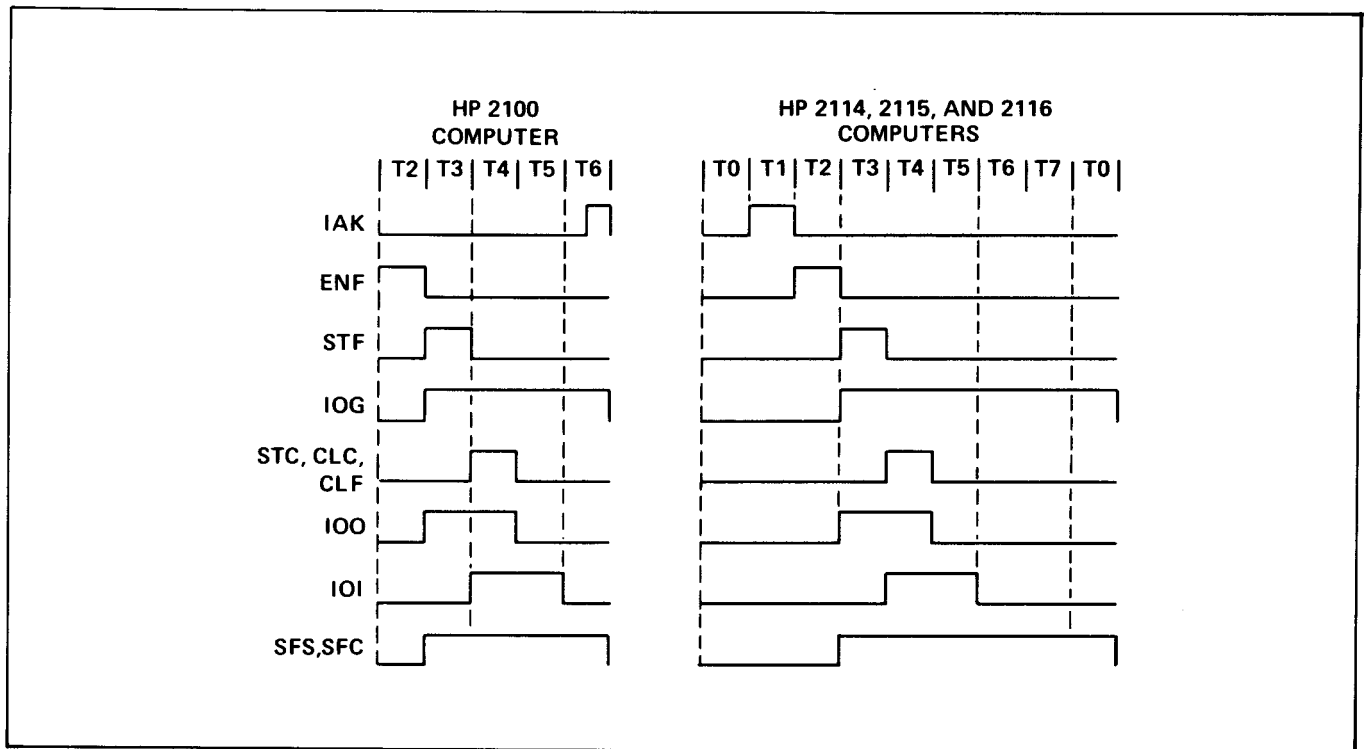Figure US-1. Overall Timing Diagram Showing Operation with 2100 Computer

Figure US-2. Quick Reference Timing Diagram

HP 2100A TAPE PUNCH TEST

Order No. HP 24190

HEWLETT **hp** *PACKARD*

11000 Wolfe Road
Cupertino, California 95014

HP 2100A TAPE PUNCH TEST

This diagnostic confirms proper operation of the HP 2753 High Speed Tape Punch with the 12597A-03 Interface Kit and the HP 2100A computer with 2K or larger memory by performing a complete functional check. The program also allows the user to generate tapes containing "worst case" data patterns and special characters to aid in hardware analysis.

HARDWARE CONFIGURATION

This diagnostic program requires a 2100A computer, a teleprinter, a 2753 High-Speed Tape Punch, and optionally an HP 2737, HP 2748, or an HP 2758 High Speed Tape Reader.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

To run the diagnostic, the operator selects the appropriate switch options from Table TP-1 and presses RUN.

If an error is detected, the program prints a message on the teleprinter. All messages and their meanings are listed in Table TP-2.

If a trap cell halt occurs, $1020xx_8$ is displayed. (xx is the trap cell location.) The cause of a trap cell halt must be determined by the user; after the error is corrected, the diagnostic program is restarted.

After the functional test is complete, the computer halts. The punch may now be used to generate a standard test tape from data in memory. This test tape is then read to check for proper operation of the tape punch.

A special test tape, consisting of a single character continuously punched may also be prepared, to diagnose specific malfunctions.

PROGRAM ORGANIZATION

ABLEX

Sets the I/O instructions to the Select Code for the High Speed Tape Punch.

FUNCTIONAL TEST

Checks the ability of the PRESET to initialize properly, then checks the punch and interrupt capabilities. The routine initializes a punch operation, forcing an immediate interrupt, and analyzes the response. A completion message is typed. Forty leader characters are punched to feed out the character (377) punched in the forced interrupt. The computer then halts with 102001_8 displayed to allow user analysis.

OPTION ANALYSIS

Allows the operator to use the switch register (Table TP-1) either at the start or end of the program to select these options: punching and/or reading the character stored in switches 8-15 of the switch register, running the punch test under Interrupt Control, and specifying the character to be punched or read.

SELECTED OPERATION

Performs the punching and reading for both special character and standard tapes. A special character tape contains a continuous punching of character set into switch register bits 8-15. A standard data tape contains data in seventeen foot sequences separated by a fifteen leader character gap called a resync point. This resync point provides a convenient starting point for tape testing. Also, when an extremely bad tape is encountered and no identifiable tape data pattern can be established (5 consecutive data errors), the tape forward spaces to a resync point before continuing the data test. The seventeen foot

area of tape is composed of eight groups of data each containing eight data blocks. The data blocks contain different numbers of characters as listed below:

Block	Characters
1	40
2	20
3	50
4	2
5	99
6	10
7	30
8	5

The data pattern of the data blocks is modified by the program using this character table:

001
200
002
100
004
040
010
020

The actual data starts with the character 377_8 (Ch. A1). 377 is modified by the addition of the first table character, 001_8. This character (Ch. A2) is punched, complemented, and its complement is punched. Character A2 is then modified by the next table entry, 200_8. This character (Ch. A3) is punched, complemented, and the complement is punched. This process is repeated until

the last character table entry, 020_8, is used. Then the table is referenced back to the character 001_8 and modification continues until character A_n. This entire process takes up seventeen feet of tape and is repeated after each resync point.

Example of initial data sequence:

Character

1	377	
2	000	(377 +1)
3	377	Complement
4	200	(000 + 200)
5	177	Complement
6	202	(200 + 002)
7	175	Complement
8	302	(202 + 100)
9	075	Complement
10	071	Complement

LIMITATIONS

The program does not test for low tape status while punching with switch seven set ON.

After a roll of tape has been punched the program detects the low tape status and prints the message TAPE LOW. Using a small roll of tape enables the user to test the low tape status sooner.

OPERATING INSTRUCTIONS

a. Set the teleprinter and high-speed tape punch ON.

b. Load the SIO Teleprinter driver using the Basic Binary Loader or the Basic Binary Disc Loader, then configure that driver.

c. If a high speed tape reader is to be used to check the punched test tape, load the SIO Tape Reader driver using the BBL or BBDL, then configure that driver.

d. Load the HP 2100A Tape Punch Test using the BBL or the BBDL.

e. Set a starting address 2_8.

f. Set the Tape Punch select code (I/O address) in bits 5-0 of the switch register.

g. Press RUN. The diagnostic halts with 102000 in MEMORY DATA when the configuration is complete.

h. If desired, use the SIO System Dump program to punch a copy of the configured teleprinter driver (and the tape reader driver if loaded) along with the configured diagnostic tape.

i. Set the starting address 100_8.

j. Press EXTERNAL PRESET and RUN to execute the functional test section.

k. At the completion of the functional test, the teleprinter types "FUNCTIONAL TEST COMPLETED" and the computer halts with 102001 in MEMORY DATA.

To punch a standard test tape and use it to test the punch unit, proceed as follows:

l. Set switch register bit 0 ON.

m. Press RUN. The tape punch punches out a standard test tape with six inches of leader and trailer. When sufficient tape has been punched, set switch register bit 7 on. Punching terminates at the next resync point.

n. Tear off the tape from the tape punch, rewind it and place it in the tape reader device.

o. Set switch register bit 0 OFF.

p. Press RUN. The test tape is read into the computer and checked. Errors are printed on the teleprinter.

q. When END OF TAPE or other termination conditions occur, the computer halts with 102001 in MEMORY DATA. Execute steps 1 through q for retesting.

To punch and check a special tape, containing only one puched character, perform the following steps:

r. Set switch register bit 2 ON.

s. Set the octal code of the character to be punched in switch register bits 15-8.

t. Press RUN. The special character test tape is punched with six inches of leader and trailer. To terminate the punching operation, set switch register bit 6 ON.

u. Tear off the tape from the tape punch device, rewind it and place it in the tape reader device.

v. Set switch register bit 2 OFF.

w. Press RUN. The tape is read by the computer and checked. Errors are reported as in the standard test tape except that no character number is reported.

To reconfigure the diagnostic, restart the program at address 2_8.

To start the functional tests, start the computer at address 100_8.

To execute at the option analysis section, start the program at address 110_8.

Table TP-1

Program Options--SWITCH REGISTER Settings

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bits	Function
0	If set ON, punch a standard or special data tape (according to bit 2) with or without interrupt control (according to bit 1). If set OFF, read either the standard test tape or the special test tape (according to bit 2) from the High Speed Tape reader or the Teleprinter Tape Reader.* Reading is not performed under interrupt control.
1	If set ON, punching operations are run under interrupt control. The operating procedure for the program is not changed. If set OFF, punching operations are run under non-interrupt control.
2	If set ON, punch the character stored in bits 8 through 15 (bit 0 ON), or read the character stored in bits 8 through 15 (bit 0 OFF). If set OFF, tape being punched or read is the standard test tape. Changing the content of the switches during program operation has no effect on the data pattern as the switches are only modified upon program start or TERMINATE.
3	Set ON to momentarily interrupt the test at any time without affecting the test or data sequence. Set OFF to continue the test.
4	Set ON to interrupt the test before processing the 15 leader characters (during either a punch or a read) that comprise a resync gap on the tape. Set OFF to continue the test. If an option change is desired, set the terminate switch (bit 6) ON before setting bit 4 OFF. Make the changes, then set bit 6 OFF to continue.

---

* The tape is read in four character blocks and then checked. Thus the character is error may not be the one under the read head during error printouts.

Table TP-1 (cont). Program Options--SWITCH REGISTER Settings

Bits	Function
5	Set ON to interrupt a read operation if an error is found during data tape analysis.
	Set OFF to continue reading, but set ON immediately thereafter to continue "error interrupt."
	If the tape is removed for inspection during an error pause, reload the tape carefully to insure that no data character is re-read or skipped.*
6	Set ON to terminate the current operation in an orderly manner. When termination occurs, a "TERMINATE" message is typed and the program halts with 102001_8 displayed. Make option changes at this time (if desired) as the program restarts at the option analysis section when RUN is pressed.
	Set OFF to continue testing at the option analysis section of the program.
7	Set ON to terminate punching or reading at the resync gap. The switch may be set at any time during the operation; the program terminates as described.
8-15	Set bits 8-15 to the special character to be punched in or read from the special test data tape (bit 2 set ON).

---

* The tape is read in four character blocks and then checked. Thus the character in error may not be the one under the read head during error printouts.

Table TP-2

Diagnostic Messages

Messages	Meaning	Action
CLF ERROR	The Punch Flag flip-flop is set but the CLF instruction did not clear it.	
EMBEDDED LEADER -TERMINATE-	Three consecutive leader characters read in a data block.	Space tape to next resync point. Press RUN.
FLAG CLEAR ON PRESET	The Punch Flag flip-flop is not set.	Set STARTING ADDRESS 100_8. Press EXTERNAL PRESET. Reset the options in the switch register. Press RUN.
FUNCTIONAL TEST COMP	Functional Test completed.	Check teleprinter messages for equipment status. a. To rerun the Functional routine: Set STARTING ADDRESS 100_8. Press EXTERNAL PRESET. Reset the options in the switch register. Press RUN. b. To continue the run of the program, set the desired switch options (see Table TP-1) and press RUN.
G *xxxxxxx* B *xxxxxxx xx xx*	Character error.	G *xxxxxxx* is a good data pattern where: *xxxxxxx* is a good character. B *xxxxxxx xx xx* is a bad data pattern where: *xxxxxxx* is a bad character. *xx* is the character of the data block that is an error. *xx* is the number of characters in the data block.

Table TP-2. (cont). Diagnostic Messages

Messages	Meaning	Action
INTERRUPT ON PRESET	Erroneous interrupt in Functional Test.	Set STARTING ADDRESS 100_8. Press EXTERNAL PRESET. Press RUN.
LONG LEADER	More than fifteen leader characters at a resync point.	Check tape for correct data resequencing. Press RUN.
NO INTERRUPT FLAG SET	An interrupt situation forced by the program did not occur.*	Terminate the diagnostic program.
RESYNC ERROR- 5 CONSECUTIVE ERRORS	Five consecutive errors are detected.	Space tape to next resync point. Restart routine.
SHORT LEADER -TERMINATE-	Fifteen leader characters have not been read at a resync point.	Backspace tape in the leader area and press RUN.
STF ERROR	The Punch Flag flip-flop is clear but the STF instruction did not set it. Program halts.	
SYSTEM CLF Ø ERROR	The system flag flip-flop is set but the CLF flag instruction did not clear it.	Check other error messages for possible failure association.
TAPE LOW	Tape supply is low.	Install a new tape supply.
-TERMINATE-	Diagnostic program is terminated, switch six is ON, bad data characters, embedded leader, "End-of-Tape" or "Tape Low."	Change any desired options or check the tape for positioning at the resync leader. Press RUN.

---

*At the time of the forced interrupt, the STF 0, STF (punch), CLF 0, CLF (punch), SFC 0, SFC (punch) and SFS (punch) commands have been tested. OTA and STC can be checked by looking for character of value 377 on the punch tape.