HP 12793A BISYNC MODEM INTERFACE KIT

INSTALLATION AND SERVICE MANUAL

PART NUMBER 12793-90001

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HP 12793A
BISYNC Modem Interface Kit
installation and service manual

Card Assembly: 5061-3418
Date Code: 2022

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PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this printing history page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past updates; however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual will contain new information, as well as all updates.

To determine what manual edition and update is compatible with your current software revision code, refer to the appropriate Software Numbering Catalog, Software Product Catalog, or Diagnostic Configurator Manual.

First Edition .....September 1980
Update 1 ..... March 1982

SAFETY CONSIDERATIONS

GENERAL - This product and relation documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

Some of the semiconductor devices used in this equipment are susceptible to damage by static discharge. Depending on the magnitude of the charge, device substrates can be punctured or destroyed by contact or mere proximity to a static charge. These charges are generated in numerous ways such as simple contact, separation of materials, and normal motions of persons working with static sensitive devices.

When handling or servicing equipment containing static sensitive devices, adequate precautions must be taken to prevent device damage or destruction. Only those who are thoroughly familiar with industry accepted techniques for handling static sensitive devices should attempt to service the cards with these devices. In all instances, measures must be taken to prevent static charge buildup on work surfaces and persons handling the devices. Cautions are included through this manual where handling and maintenance involve static sensitive devices.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

WARNING

EYE HAZARD

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

Definition of Terms

The following terms are defined as they are used in this manual.

ASCII - American Standard Code for Information Interchange.

asynchronous transmission - No timing signals are sent with the data. Start and stop bits serve to define transmitted words.

BISYNC (Binary Synchronous) - Hewlett-Packard's version of the Binary Synchronous Communications protocol.

block - A contiguous stream of data words. In BSC protocol, a block is usually referred to as a message.

BSC (Binary Synchronous Communications) - A standard data communications protocol developed by IBM.

buffer - A segment of contiguous random-access memory (RAM) locations used for temporary storage of input/output messages.

card - The interface printed circuit assembly (PCA).

CRC-16 (Cyclic Redundancy Check) - An error detection scheme used in data communications.

DIP (Dual In-line Package) - A type of integrated circuit package.

driver - In a hardware sense, a driver refers to a circuit which is capable of supplying specific current and voltage requirements. In a software sense, a driver is a program that is capable of controlling a specific input/output device.

DS (Distributed System) - A term used to refer to networks using Hewlett-Packard Distributed Systems hardware and software products.

firmware - Software code packaged in read-only memory (ROM).

full-duplex - Communications system or equipment capable of simultaneous two-way data communication.

half-duplex - Communications systems or equipment capable of transmission in either direction, but not both directions simultaneously.

handshaking - The alternating exchange of predetermined signals between two communicating devices for purposes of control.

host - The computer housing the communication card.

interface - A device providing electrical and mechanical compatibility between two communicating devices. The HP 12793A also provides other control features for the associated communication link.

LED (Light Emitting Diode) - A component used on many printed circuit assemblies to provide a visible indication of desired information.

link - Communication interfaces, lines, modems, and other equipment which permit the transmission of information in data format between two or more devices.

modem (modulator-demodulator) - Equipment capable of digital-to-analog and analog-to-digital signal conversion for transmission and reception via common carrier telephone lines.

PCA (Printed Circuit Assembly) - Interface cards are sometimes referred to as PCAs.

receiver - Any device capable of reception of electrically transmitted signals.

synchronous - Timing signals are transmitted with the data. No start and stop bits are used. Defined protocol characters must be used to delineate message blocks or frames.

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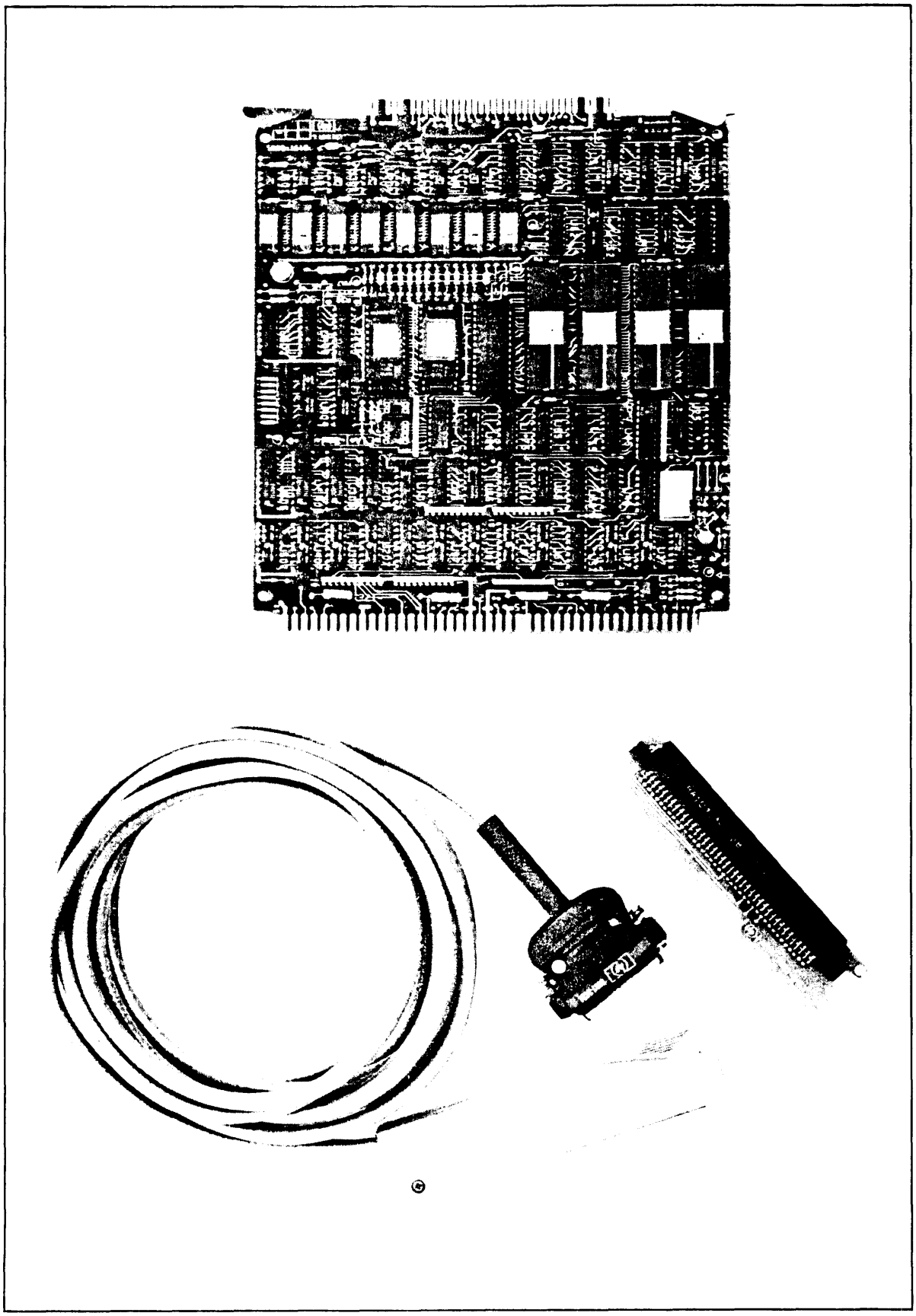


Figure 1-1. HP 12793A BISYNC Modem Interface Kit Contents

Section 1
General Information

Introduction

This manual provides general information, installation procedures, BISYNC protocol information, theory of operation, maintenance instructions, replaceable parts information, and servicing diagrams for the HP 12793A BISYNC Modem Interface Kit. This section contains general information for the HP 12793A, including a description and specifications.

Description

The HP 12793A (refer to Figure 1-1) provides an HP 1000 M/E/F-Series Computer with the capability to support a synchronous modem communications link to an HP 3000 System. It is used in conjunction with driver DVR66 of the HP 91750A DS/1000-IV Software.

The BISYNC interface card plugs into a single I/O slot of an HP 1000 M/E/F-Series Computer and is assigned a single select code. The card contains a Z-80A CPU chip with associated Z-80A support chips and two ROMs containing firmware to implement binary synchronous protocol. Due to this on-board intelligence, the card is able to relieve a large amount of CPU overhead. Functions such as BISYNC protocol generation, CRC-16 block check error control, modem control, and a hardware self-test are all handled on the interface card. The Z-80A and on-board RAM also enable the card to maintain long-term communications line statistics, and input and output data buffering.

Equipment Supplied

The standard HP 12793A BISYNC Modem Interface Kit consists of the following items (see Figure 1-1):

1. Programmable serial interface card, HP part number 5061-3418.
2. BISYNC firmware ROMs, HP part numbers 91750-80005 and 91750-80006.
3. EIA RS-232-C modem cable (5 meter, 16.4 feet), HP part number 5061-3424.
4. Modem diagnostic hood, HP part number 5061-3453.
5. Installation and Service Manual, HP part number 12793-90001.

The following options are available with the HP 12793A:

1. Option 001: Upgrade discount for latest revision of interface firmware (for previously purchased interfaces only).

2. Option 002: Replace the EIA RS-232-C cable with one EIA RS-449 modem cable (5 meter, 16.4 feet), HP part number 5061-3436.

Identification

The Product

Five digits and a letter (12793A in this case) are used to identify Hewlett-Packard products used with HP computers. The five digits identify the product and the letter indicates the revision level of the product.

The Circuit Card

The circuit card supplied with the kit is identified by a part number marked on the card. In addition to the part number, the card is further identified by a letter and a date code consisting of four digits (e.g., A-2013). This designation is placed below the part number. The letter identifies the version of the etched circuit on the card. The date code (the four digits following the letter) identifies the electrical characteristics of the card with components mounted. Thus, the complete part number on the interface card could be:

5061-3418
A-2013

If the date code stamped on the BISYNC interface card does not agree with the date code on the title page of this manual, there are differences between your card and the card described herein. These differences are described in manual supplements available at the nearest Hewlett-Packard Sales and Service Office (a list of Hewlett-Packard Sales and Service Offices is supplied at the back of this manual).

Installation and Service Manual

The manual supplied with the kit is identified by its name and part number. Part number, 12793-90001, and publication date are printed on the title page. If the manual is revised, the publication date is changed and the List of Effective Pages (page iii) reflects the pages involved in the change. The Print History page (ii) records the reprint dates.

Specifications

Table 1-1 lists the specifications of the HP 12793A BISYNC Modem Interface Kit.

Table 1-1. Specifications

TRANSMISSION MODE:	Bit serial; synchronous.
TRANSMISSION CODE:	ASCII
TRANSMISSION LINK:	Half-duplex over switched (direct distance dial) or private (leased) common carrier telephone line.
INTERFACE:	Conforms to EIA Standards RS-232-C and RS-449.
DATA TRANSFER LENGTH:	Variable block sizes: 1 to 3216 bytes.
DATA TRANSFER RATES:	Approximately 300, 1200, 2400, 4800, 9600, 19200, or 57600 bps with on-board timing (for use with a modem eliminator). External timing rates depend on the modem being used.
MODEM TYPES:	Synchronous only; half or full duplex (better line turnaround times with full duplex).
MODEM COMPATIBILITY:	Refer to the data sheet for the HP 12793A.
DATA ERROR DETECTION:	CRC-16 check controlled on the interface.
DATA ERROR CORRECTION:	Retransmission under firmware control.
POWER:	Supplied by host computer as follows: 1.923A at +5V, 0.315A at +12V, 0.175A at -12V. The total power dissipated 15.495 Watts.
SUPPORTED CONFIGURATION:	An HP 1000 can only have one link to an HP 3000. The HP 3000 can support up to 7 links to HP 1000s.

Section 2
Installation

Introduction

This section provides information on unpacking, inspecting, installing, and checking the operation of the HP 12793A BISYNC Modem Interface Kit.

Unpacking and Inspection

Inspect the shipping package immediately upon receipt to detect any evidence of mishandling during transit. If the package is damaged, ask that the carrier's agent be present when the kit is unpacked. Carefully unpack the card and accessories and inspect for damage (scratches, broken components, etc.). If damage is noticed, notify the carrier and the nearest Hewlett-Packard Sales and Service Office listed at the back of this manual. Return the carton and packing material for the carrier's inspection.

After inspecting all components, refer to Equipment Supplied information given in Section 1 to ensure that the kit is complete. Also check the part numbers listed in that paragraph against the part numbers on the kit components. If the kit is incomplete, or if an incorrect component has been furnished, notify the nearest Hewlett-Packard Sales and Service Office.

After unpacking, inspecting, and checking the part numbers of all parts of the kit, follow installation and checkout procedures as defined in this section.

Computation of Current Requirements

The circuit card included with the HP 12793A obtains its operating voltages from the computer power supply through the backplane. Before installing the card, it is necessary to determine whether the added current will overload the power supply. The current requirements of the HP 12793A are listed in the power entry of Table 1-1.

Firmware Installation

CAUTION

STATIC SENSITIVE DEVICES

THE ROMS, RAMS, AND Z-80A COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE REPLACING.

The firmware ROMs (part numbers 91750-80005 and 91750-80006) are factory installed in sockets on the card. Make sure that the ROMs are installed as shown in Figure 2-1, and that the part numbers on them match those given in this paragraph.

ROM Configuration Jumpers

A set of jumpers on the interface card provides the option of using different ROM parts in the future. The set consists of a 14-pin socket housing seven removable jumpers (XW1A through XW1G), and two hardwired jumpers on the card itself. Check to see that XW1A through XW1G are configured as described in Tables 2-1 and 2-2 for the specific ROMs that are installed. The hardwired jumpers, W5 and W6, are configured at the factory. W5 should be open (not installed) and W6 should be closed (installed). Refer to Figure 2-2 for the location of the socketed jumpers on the interface card, and the parts location diagram given in Section 7 for the location of the hardwired jumpers.

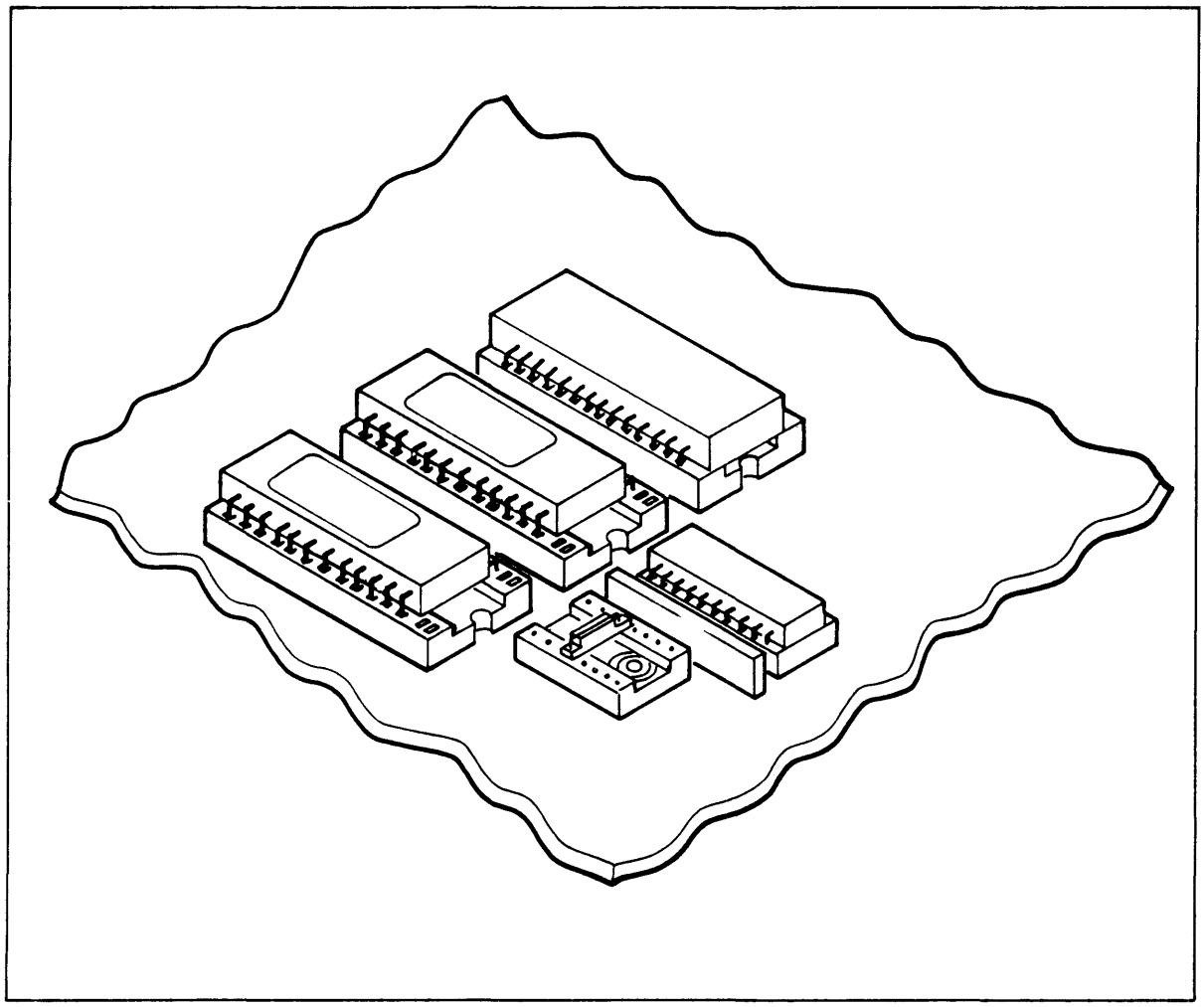


Fig. 2-1. ROM Installation

Table 2-1. ROM Categories According to Part Number

CATEGORY	HP PART #	PART TYPE
A	1818-0762	TI 2532
B	1818-0498	TI 2516 Intel 2716
C	1818-0850	Intel 2732 Intel 2332 Intel 2364

Table 2-2. Jumper Requirements for all ROM Combinations
(X denotes a required jumper)

ROM CATEGORY		XW1A	XW1B	XW1C	XW1D	XW1E	XW1F	XW1G
U93	U203							
C	C					X		
A	A				X	X	X	X
C	A			X		X	X	
B	A			X		X	X	X
B	B			X	X	X	X	X
A	C	X				X		X
C	B	X			X	X	X	
A	B	X		X	X	X	X	X
B	C	X		X		X		X

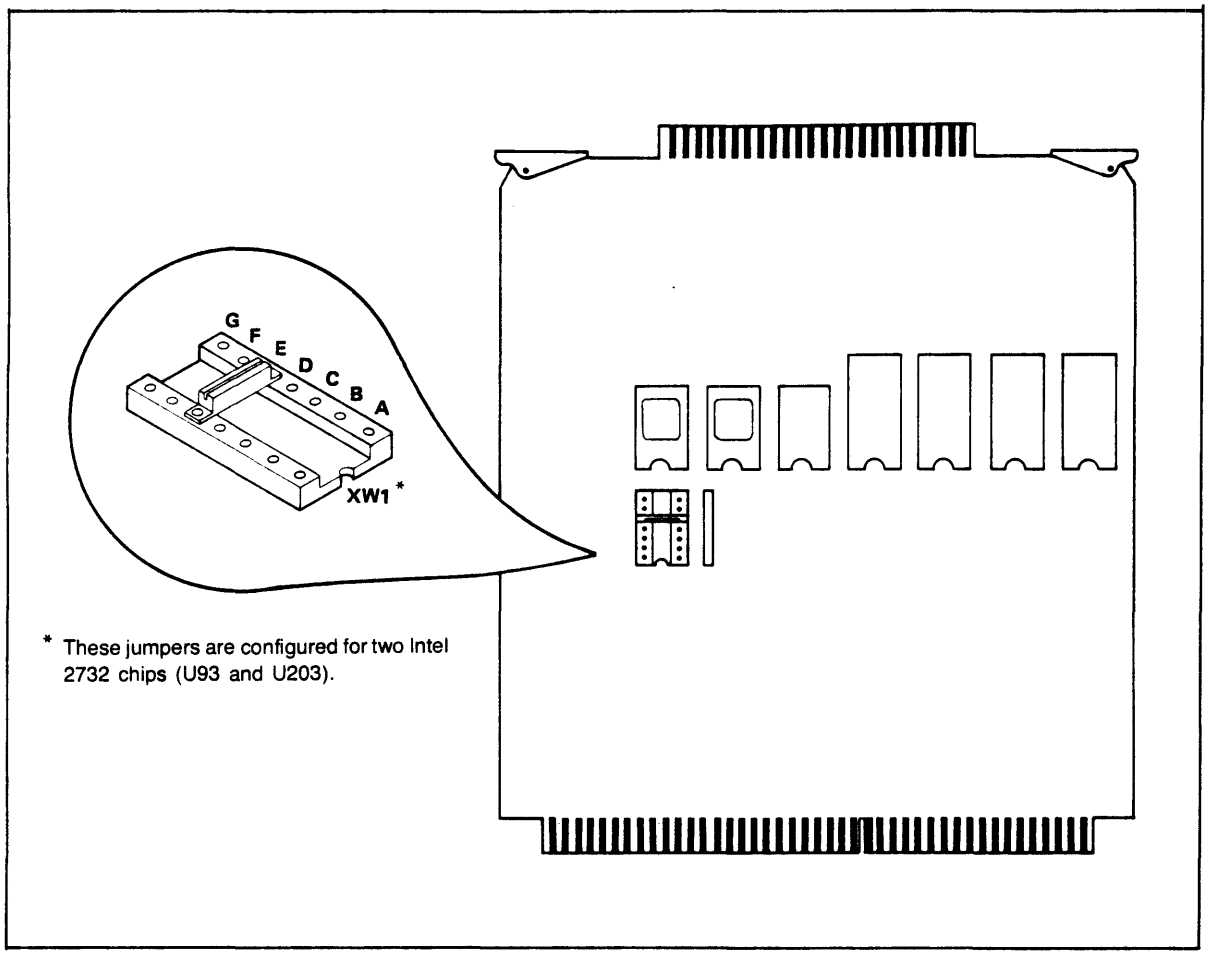


Fig. 2-2. ROM Configuration Jumper Positions

Dip Switch Configuration

The card provides a Dual In-line Package (DIP) containing eight switches which may be sensed by the firmware. This set of switches is used to determine whether the card is to supply a clock (for use with a modem eliminator) or not (for use with a synchronous modem), and at what rate that clock should be set if selected. Another switch in the set is used to define the initial state of modem control signal TR (unasserted for ring detect; asserted for auto-answer or modem eliminator configurations). Configure the DIP switch as necessary using the switch assignments given in Tables 2-3 and 2-4. Refer to Figure 2-3 for the switch positions on the card.

Table 2-3. Switch Assignments

SWITCH	FUNCTION
1	Must be open.
2	Closed for external clock (for use with a synchronous modem). Open for internal clock (for use with a modem eliminator).
3	Closed for Ring Detect. Open for immediate TR (auto-answer). For specific modem needs, refer to modem documentation. Must be open for use with a modem eliminator.
4,5	Not used.
6,7,8	Select clock rate. See Table 2-4.

Table 2-4. Clock Rate Selection
(Settings for Internal Clock Only)

SWITCH SETTINGS 6,7,8	CLOCK RATE (bps)	
OOO	300	NOTE:
OOX	1200	X = closed side depressed = logic "1"
OXO	2400	O = open side depressed = logic "0"
OXX	4800	
XOO	9600	
XOX	19200	
XXO	57600	
XXX	*230000	

* Not used with BISYNC firmware.

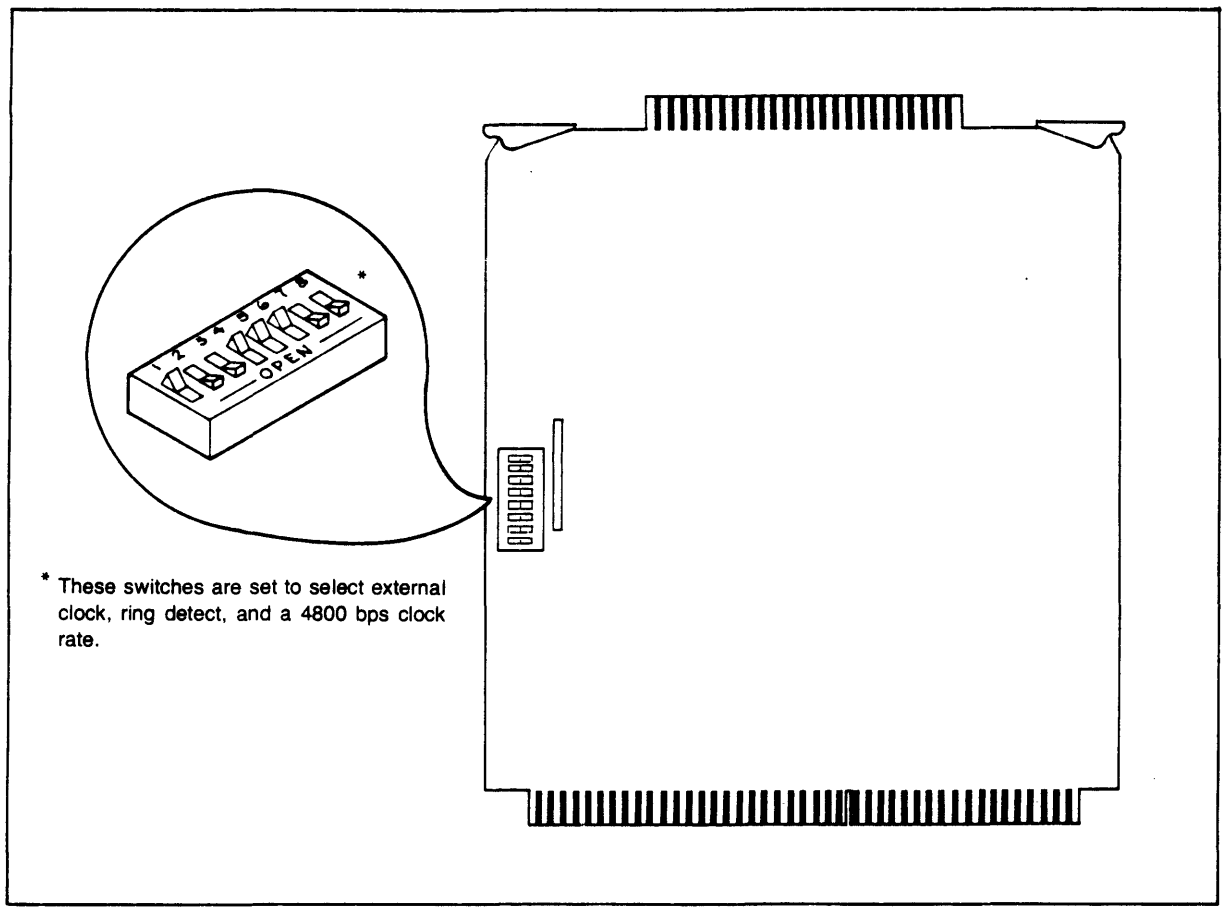


Figure 2-3. DIP Switch Position and Configuration

Card and Cable Installation

CAUTION

ALWAYS TURN POWER OFF TO THE COMPUTER AND OTHER ASSOCIATED EQUIPMENT WHEN INSERTING OR REMOVING INTERFACE CARDS OR CABLES. FAILURE TO FOLLOW THESE DIRECTIONS COULD RESULT IN DAMAGE TO THE EQUIPMENT.

After ensuring that the computer power supply can handle the added load, the ROMs are properly installed, and the DIP switch is configured properly, perform the following steps:

1. Turn off power at the computer and the modem. Install the interface card in the desired slot in the computer card cage, noting the select code. The card should be oriented the same as all other cards in the computer: components on the top side of the card. Press the card firmly into place.

2. Connect the cable supplied with the kit to the interface card and modem.

3. Restore power to the computer and modem.

4. Initialize the new link into the network as specified in the HP 91750A DS/1000-IV Network Manager's Manual.

5. Perform the checkout procedure on the card as specified in the next paragraph.

Check-Out Procedure

For checkout after installation, perform the interface card and communication link checks described below.

Interface Card Configuration Check

Since the interface card self-test is run each time that power is applied to the card or the card is reset, the first part of checkout is automatically performed. The following procedure will verify that the card passed the self-test and that the backplane interface circuitry is operational. It also provides a way to check the card configuration switch settings. To perform the check, enter the following commands:

1. RU,DSINF<cr>

   DSINF is a DS/1000-IV utility program that can be used to obtain information such as network configuration, communications parameters, card configuration, etc. For more information on DSINF, refer to the DS/1000-IV Network Manager's Manual, HP part number 91750-90003.

2. LU,##,AL<cr>

   LU will return information on the configuration of a specified DS/1000-IV interface card, where ## is the LU (Logical Unit number) of that card. Information will only be returned if the card passed the self-test.

In this way, DSINF will return card configuration information as well as other useful parameters. Compare the external/internal clock selection and clock rate returned with the desired values. If these values are unexpected, check the switch settings on the card. If in error, reconfigure the switch and reinstall the card, going through all checkout procedures again.

Communication Link Check

A good check of the communication link is accomplished by exercising a few RMOTE commands. To do this, dial up the remote station and type in the following commands after the system prompt (:):

1. :RU,RMOTE<cr>

   RMOTE is the program that handles operator commands for communications from an HP 1000 to an HP 3000 in a Distributed Systems network. It schedules the appropriate monitors to handle all outgoing and incoming requests. RMOTE will prompt with a dollar sign ($) when commands are referred to the local node only. When a remote node is referenced (the HP 3000 system), the prompt will become a number sign (#).

2. $SW<cr>

   The SW (Switch) instruction transfers command execution to the remote HP 3000 system. A second SW would transfer execution back to the local HP 1000 node.

3. #HELLO<ACCOUNT NAME><cr>

   The HELLO command executes a session log-on to the HP 3000. An account name can be obtained from the network manager. A log-on message should be displayed to indicate successful execution of this step.

4. #SHOWJOB<cr>

   The SHOWJOB command will display all sessions that are presently active at the HP 3000 node.

5. #EX<cr>

   The EX (Exit) command will automatically perform log-off from the HP 3000 and exit RMOTE.

If the above messages are sent successfully, the described results will be displayed with no error messages returned. If an error message is returned, refer to error code information supplied in the DS/1000-IV User's Manual, HP part number 91750-90002. For troubleshooting procedures, refer to Section 5 of this manual or the troubleshooting section of the Network Manager's Manual, HP part number 91750-90003.

Interface Card LED's

There are four LEDs installed on the interface card. Located on the left side of the card next to the front edge connector, the LEDs are visible when the card is installed in the computer. The LEDs are referenced as 0 through 3 with 0 being the LED on the right. Only LED3 is used during normal operation. LED3 being lit indicates that the external clock has been selected on the card (see the DIP Switch paragraph in this section); LED3 being off indicates that the internal clock has been selected. The LEDs are also used during the self-test. Upon successful completion of the self-test, LED0 through LED2 will be lit and LED3 will indicate the clock selection as described above.

Section 3
Protocol

Introduction

There are several levels of protocol involved in an HP DS/1000-IV communications link. Two of these levels are handled on the HP 12793A: line protocol and communications protocol. The first level involves timing and control signals, and electrical specifications for computer to modem connections. The second level involves the more complex set of rules used to control the flow of data over the communication link. Both line and communications protocols are firmware controlled on the HP 12793A. These two levels of protocol are discussed briefly in the following paragraphs of this section. Refer to the documentation on the specific modem being used with the HP 12793A for more line protocol information. The communications protocol implemented for this product is a version of BSC protocol. Refer to the IBM Systems Reference Library: General Information - Binary Synchronous Communications, Order No. GA27-3004-2, Third Edition, October, 1970 for an in-depth description of BSC.

Line Protocol

The HP 12793A BISYNC Interface Kit is capable of implementing line protocol compatible with EIA RS-232-C or CCITT V.24 interface standards (for current modems) and EIA RS-449 (for future modems). A brief description of the handshake control sequence between card and modem is presented in Section 5 of this manual. The tables in Section 7 of this manual provide pin numbers, mnemonics, and descriptions for all modem control lines implemented on the HP 12793A.

Communications Protocol

The HP 12793A is programmed via the read-only memory (ROM) on the card to implement BISYNC, derived from Binary Synchronous Communications (BSC) protocol. Developed by IBM, BSC is a synchronous, block oriented protocol designed for implementation over half-duplex communications channels. The following paragraphs discuss the main characteristics of BSC and BISYNC and the differences between them.

Control Handshaking

BISYNC employs handshaking as the method for interaction between communicating nodes in a network. Typically, the following information is exchanged:

* Message available for transmission
* Text transmission
* Acknowledgement or rejection of text
* Retransmission after error detection

Figure 3-1 illustrates a simplified handshaking sequence. Here the transmitter indicates a message is ready to be sent and the receiver sends a "GO AHEAD" message. After detecting an error in the received block, the receiver indicates that a retransmission is necessary. The retransmission is error-free and the receiver indicates it is ready for the next block to be sent by sending one itself. The transmitter sends an end of data message to acknowledge the last received block and both stations wait for the next transaction to occur.

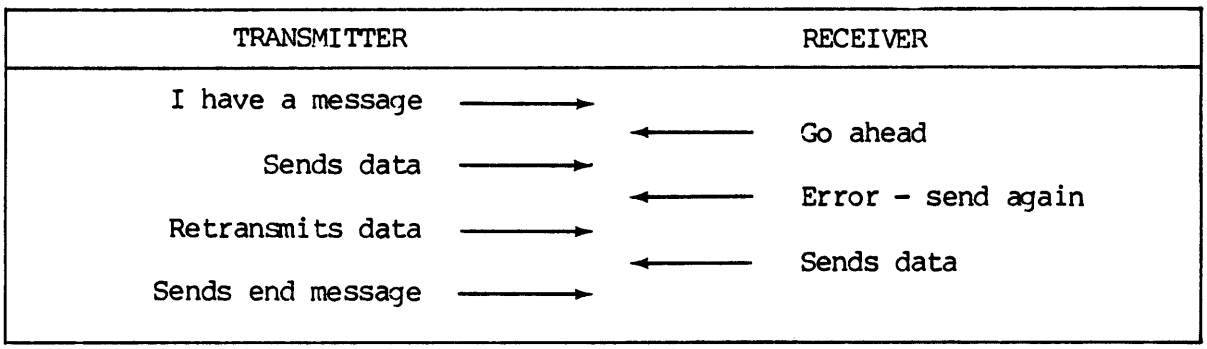


Figure 3-1. Simplified Handshaking Sequence

Transmission Initiation

For standard BSC, all data transmissions are organized in blocks. Special protocol characters are used to initiate and control these block transfers. Before beginning a transfer, it is necessary to synchronize the communicating stations. This can be accomplished by having the sending station transmit synchronizing characters (SYN). When the receiving station senses these characters, it will synchronize itself with the transmitter. A message exchange can then be initiated via an enquiry (ENQ) from the transmitting station and an acknowledgement (ACK) from the receiver. Throughout the ensuing handshaking data transfer, each acknowledgement is alternately numbered one (ACK1) and zero (ACK0).

BISYNC, like BSC, is block oriented and uses a synchronization sequence similar to the one just described. After the SYN characters, an enquiry (ENQ) is transmitted and acknowledged by the other station with an ACK0.

Throughout the ensuing handshaking sequence, messages received successfully are not acknowledged by alternating ACK0's and ACK1's as with BSC. The receiving station acknowledges correct reception of a message by transmitting a message block of its own. ACK1's are never sent to indicate correct reception of a block. They are only used during certain error recovery procedures. This mode of operation is referred to as full conversational mode. This allows a receiver the option of transmitting data before the transmitting station finishes its transmission.

Figures 3-2 and 3-3 illustrate standard BSC handshaking and BISYNC full conversational handshaking. The DLE characters shown in Figure 3-3 are BISYNC transparency mode control characters and are discussed in the section on transparency mode in this section.

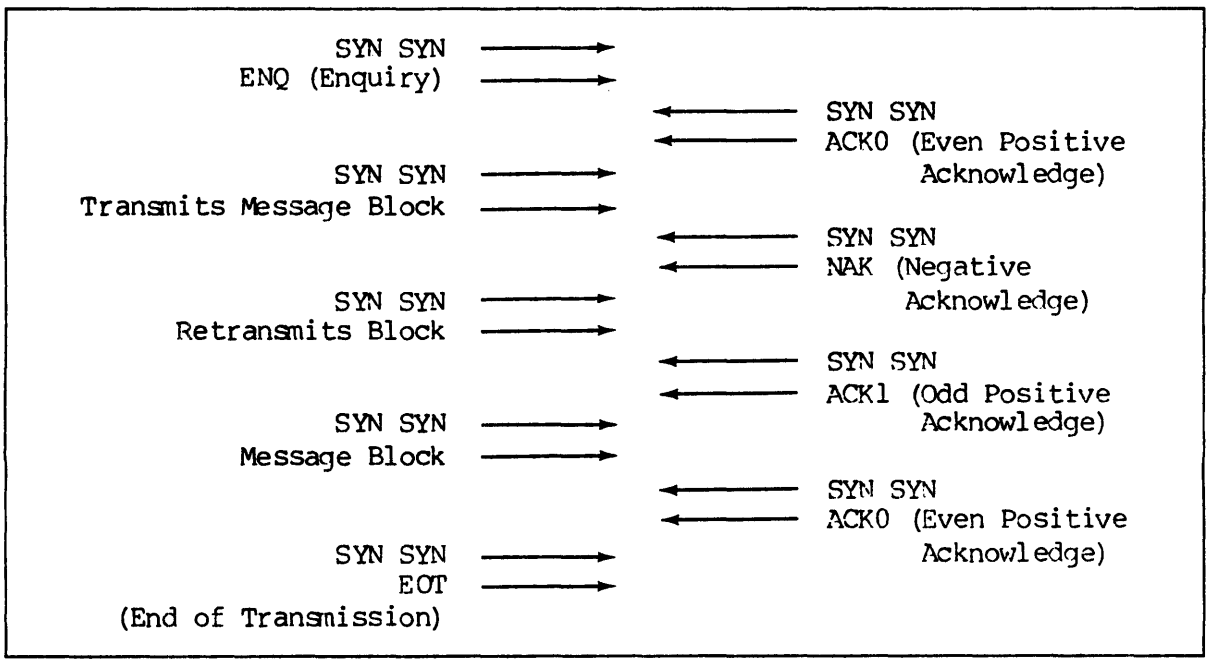


Figure 3-2. BSC Handshaking Sequence

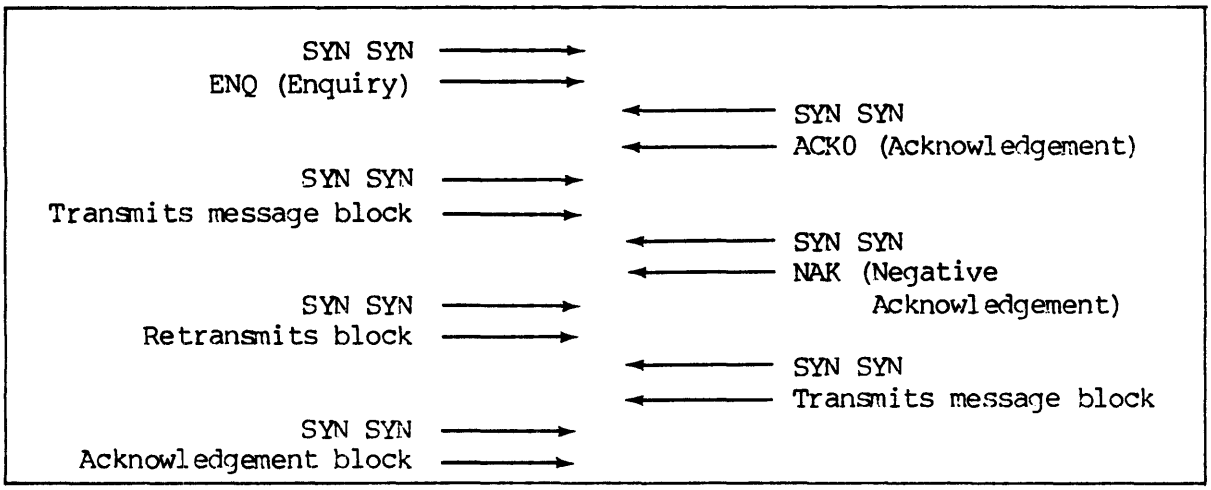


Figure 3-3. BISYNC Handshaking Sequence

Message Formats

After synchronization and enquiry handshaking, data and data control characters are transmitted in message blocks. A message block format for BSC is shown in Figure 3-4. The three elements that make up a BSC message are as follows:

1. Header

   Identified by a start of header (SOH) character, a header may contain destination information, transmission block size, or any other desired information.

2. Text

   A start of text (STX) character identifies the following bytes as transmitted text. Text may be transmitted in a single block, or in the case of long messages, it may be broken up into several blocks that are transmitted individually. The end of the text portion of a message is indicated by an end of text (ETX) character or by an end of text block (ETB) character. The ETB character indicates that the text in the current message is part of a large block to be completed with text from future messages.

   A large block of text can also be divided into several sub-blocks (for error checking purposes) within one message block. In this case, an intermediate text block (ITB) character is used to define the end of a sub-block in a message. Figure 3-5 illustrates this message format.

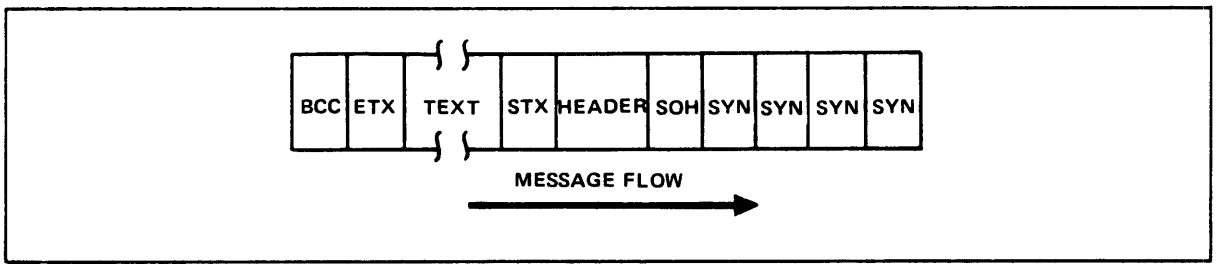


Figure 3-4. BSC Message Format

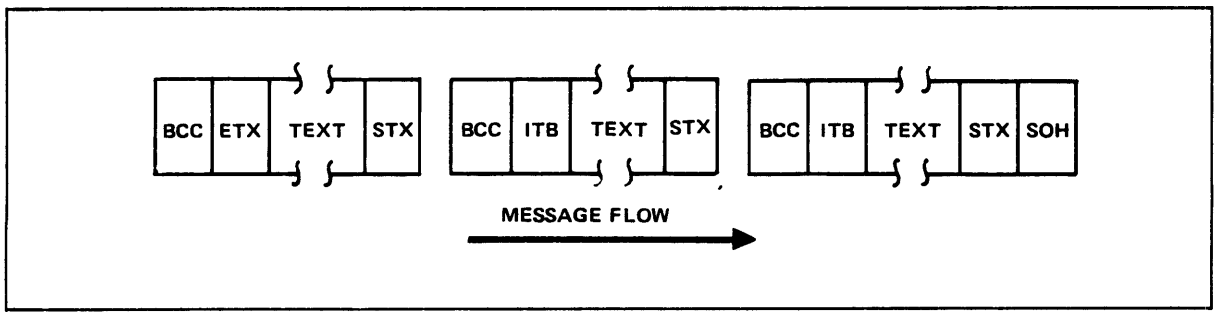


Figure 3-5. BSC Multi-block Message Format

3. Trailer

   The trailer consists of the block check character (BCC). For information on the type of error checking used by the 12793A, refer to the paragraph on error detection and correction.

BISYNC varies from standard BSC in several ways concerning message format. Headers (and, therefore, also the SOH character) are never used in BISYNC. Large blocks are never divided into more than one transmission (eliminating the use of the ETB character), or divided into sub-blocks within a single message (eliminating the use of the ITB character). The message format illustrated in Figure 3-6 is the only message format used for BISYNC transmissions.

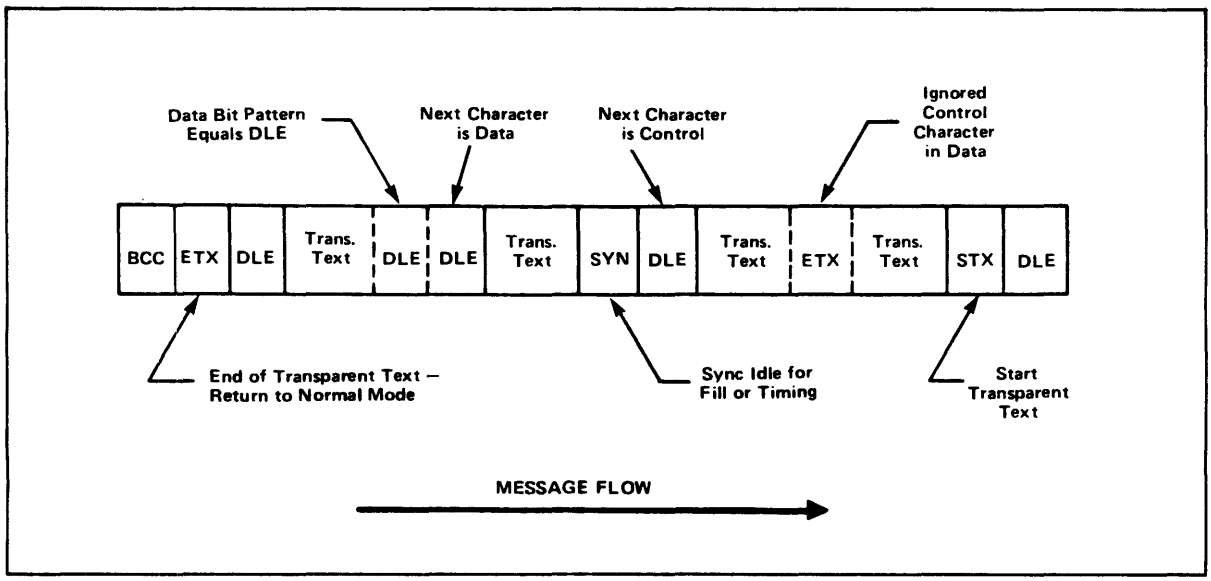


Figure 3-6. Transparent Text Message Blocks

Summary of Protocol Characters

Table 3-1 describes the meaning and function of each of the BSC protocol characters. Table 3-2 contains the ASCII code for each of the byte characters and shows which characters are not used in BISYNC protocol.

Transparency

The transparent mode of operation allows the sending of data bit patterns that would be interpreted otherwise as control characters. In order to distinguish authentic control characters from data of the same pattern, all control characters are preceeded by a single DLE character. BISYNC message blocks are always transmitted in the transparent mode. Figure 3-6 illustrates an example of BISYNC message format and Table 3-3 contains the control character sequences of transparent mode used with BISYNC.

Table 3-1. BSC Protocol Character Summary

Character	Meaning	Functions
SYN	Synchronizing Character	Establishes and maintains character synchronization prior to the message block and during transmission. Also used as time fill in the absence of control characters and data.
STX	Start of Text	Transmitted before the first data characters.
ETB	End of Transmission Block	Indicates the end of the text block starting with STX or SOH. BCC is sent after ETB, requiring the receiver to respond with ACK, NAK or optionally WACK or RVI.
US/ITB	End of Intermediate Transmission Block	Divides a message for error checking purposes without the turn-around required by ETB. BCC follows ITB and resets the block-check count to zero. STX or SOH is not required for following text blocks, but STX is required if a header is followed by text.
ETX	End of Text	Terminates a block begun with SOH or STX and the end of a sequence of blocks. BCC immediately follows ETX, requiring a receiver status reply.
EOT	End of Transmission	Concludes transmission, resets all stations to control mode (neither transmitter nor receiver). Also a non-transmit response to a poll and an abort signal for a malfunction.
ENQ	Enquiry	Bids for the line in a point-to-point and multipoint connection, and requests last acknowledgment retransmission or a preceding block to be ignored.
*ACK	Affirmative Acknowledgment	Previous block accepted and error-free, receiver ready for next block. Also a positive response to selection (multipoint) or line bid (point-to-point).
SOH	Start of Heading	Transmitted before the header characters. These contain information such as the routing and priority of the message.
NAK	Negative Acknowledgment	Previous block unacceptable and retransmission required. Also a negative response to a selection or line bid.
*TTD	Temporary Text Delay	Transmitter not ready to commence transmission but wants to maintain connection. Sent two seconds after message received to avoid three second timeout, also initiates an abort.
*RVI	Reverse Interrupt	Sent to a transmitter by a receiver in place of ACK, indicating the receiver has a high priority message waiting transmission.
*WACK	Wait Before Transmit Positive Acknowledgment	Previous block accepted and error-free, but receiver not ready for next block. Will continue to respond with WACK until ready to receive. Also a positive response to a text or heading block selection sequence (multipoint), line bid (point-to-point) or identification line bid sequence (switched network).
DLE	Data Link Escape	Prefix for control characters during transparent mode. Control characters have no control meaning unless prefixed by DLE.
DLE EOT	Disconnect Sequence for a Switched Line	Transmitted on a switched line when all message exchanges are complete. Can be transmitted at any time to cause a disconnect.
Pad(ϕ)		Added before (leading pad) and after (trailing pad) a transmission. This ensures the first character is not sent until the other station is prepared to receive, and the last character is properly transmitted before turnaround is initiated or the transmitter turns off.

*Two-character sequence.

Table 3-2. ASCII Octal Equivalents for BSC Protocol Characters

CONTROL CHARACTER	ASCII CODE (OCTAL)
SYN	026
STX	002
*ETB	227
*US/ITB	037
ETX	203
EOT	004
ENQ	205
ACK0 (DLE 0)	020 260
ACK1 (DLE 1)	020 061
*SOH	001
NAK	025
TTD (STX ENQ)	002 205
*RVI (DLE <)	020 274
WACK (DLE ;)	020 073
DLE	020
DLE EOT	020 004
PAD	377
* Not used in BISYNC protocol.	

Table 3-3. BISYNC Transparent Control Characters

CHARACTER SEQUENCES	FUNCTION
DLE STX	Starts transparency.
DLE ETX	Indicates end of transparent mode text.
DLE SYN	Allows one sync character to be sent.
DLE ENQ	Aborts current transmission. A BCC character is not expected.
DLE DLE	Allows one DLE character to be sent.

Error Detection and Correction

As mentioned earlier in this section, check characters (BCC) are transmitted with each block of text. The receiving station can then perform the error checking function on each block of received data and check to see that it matches the check character sent with the data. If it does not match, it will respond with a NAK and error correction will be accomplished by retransmitting the data until an error free block is received.

There are several accepted error checking functions being used in data communications. BSC and BISYNC implement the CRC-16 method of block checking with 8-bit codes, which consists of dividing a constant into the binary numeric value of the character being transmitted. The quotient is discarded and the remainder added to the next character, which is again divided by the same constant. This continues until a checkpoint character (ETX) appears. At that time, the remainder from the last division performed will be sent as the BCC.

Section 4
Principles of Operation

Introduction

This section contains a description of the operation of the interface card included in the HP 12793A BISYNC Modem Interface Kit. The hardware is described in terms of five major functional areas. A brief explanation of the command and status words used in communication between the card and the host computer is also given. The last part of this section is devoted to a functional-level description of the operation of the card.

Hardware Functional Description

The card, HP part number 5061-3418, includes the following major functional areas:

* HP 1000 M/E/F-Series Computer I/O backplane interface
* Z-80A Microprocessor family subsystem (CPU, SIO, DMA and CTC)
* Read-Only Memory (ROM)
* Random-Access Memory (RAM)
* Communication line interface

A block diagram illustrating the major functional areas of the card is presented in Figure 4-1.

Host Computer I/O Backplane Interface

The card communicates with the HP 1000 host computer over the I/O backplane. The backplane interface circuitry can be logically divided into two major sections: the I/O data latches and the control circuitry section.

The I/O data latches consist of two 8-bit input latches and two 8-bit output latches. The input latches hold 16-bit data or command words from the host computer until the card is ready to accept them. Likewise, the output latches hold 16-bit data or status words output from the card to the host computer.

The control circuitry is made up of five flip-flops and other gate-level logic elements. The primary function of this circuitry is to handle the control signals to and from the I/O backplane. These signals are used to generate and acknowledge interrupts, to handshake data between the host and the card and to conform to the standard HP 1000 computer I/O backplane signal conventions. For a more detailed discussion of these signals, refer to the HP 1000 I/O Interfacing Guide, HP part number 02109-90006.

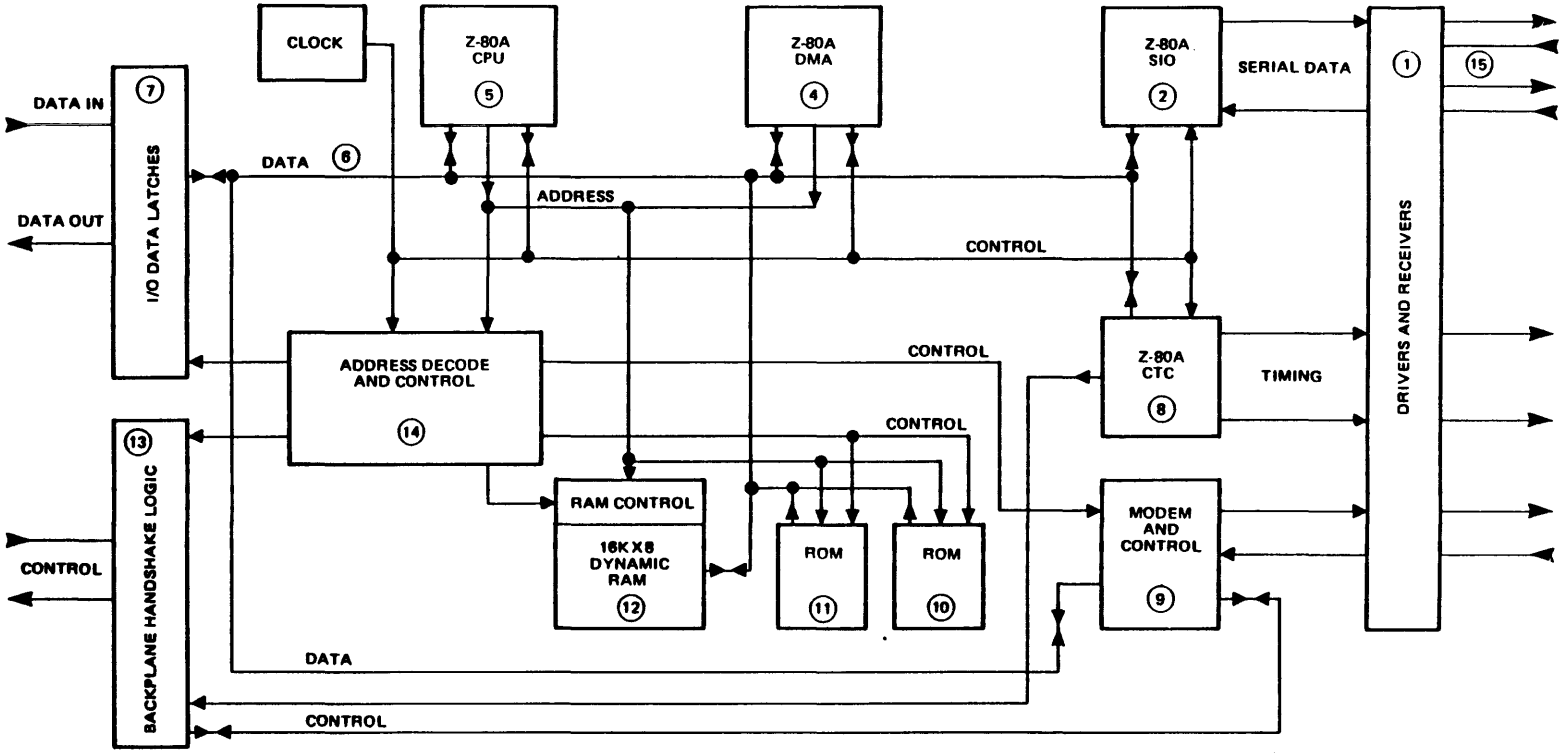


Figure 4-1. BISYNC Modem Interface Functional Block Diagram

The Z-80A Microprocessor Subsystem

The heart of the card is the Z-80A CPU (Central Processing Unit). This MOS LSI microprocessor operates from a single 5 volt supply, uses a single phase clock and has a typical instruction execution time of 1.0 microsecond. The data bus is eight bits wide and the address bus is 16 bits wide. All CPU pins are TTL compatible.

The Z-80A CPU employs a register-based architecture that includes two sets of six general-purpose registers which can be used as 8-bit registers or 16-bit register pairs. Additional 8-bit registers include two sets of accumulator and flag registers, and the interrupt vector and memory refresh registers. Additional 16-bit registers include the stack pointer, program counter and two index registers. The Z-80A CPU provides the intelligence for the card to function as a preprocessor to relieve the host computer of a majority of the protocol processing.

An important pin on the Z-80A as far as this card is concerned is the NMI (Non-Maskable Interrupt) input pin. By pulling this input low with an STC instruction, the host computer can "get the attention of" the Z-80A. An NMI is the highest priority interrupt to the Z-80A and forces it to start fetching and executing instructions from a predetermined location in the firmware. The host software driver uses this feature to inform the card that it requires service.

Various support chips are used in conjunction with the Z-80A CPU to facilitate card operation as an intelligent serial interface. These chips are discussed in the paragraphs that follow.

Serial Input/Output (SIO)

A Z-80A SIO chip is used on the card to provide the serial data communications channel. The major functions performed by the SIO chip are serial-to-parallel conversion of input data and parallel-to-serial conversion of output data.

Direct Memory Access (DMA)

The card uses a Z-80A DMA chip which is an LSI DMA controller. This chip is used to transfer data between the host computer and memory on the card. The function of the DMA logic is to transfer bytes of data in a manner that will be transparent to the Z-80A CPU software. This enables the interface to achieve higher throughput rates.

Counter Timer Circuit (CTC)

The card uses one Z-80A CTC chip which provides four independent counter/timers. One of the counter/timers is used as a data transfer rate generator and two are used as timers for the BISYNC protocol. The fourth is used to maximize the effective throughput of the card by controlling the frequency of DMA cycle stealing.

Read-Only Memory (ROM)

The card uses 8k bytes of ROM on two chips. All of the software required for the Z-80A CPU to implement the functions of BISYNC protocol generation, backplane interaction control, and modem control is contained in these ROMs and is referred to as firmware. The self-check routine is also contained in ROM.

Random-Access Memory (RAM)

The card has 16k bytes of dynamic RAM. This memory is used for data buffers and the storage of firmware variables. The refresh capability of the Z-80A CPU is used to provide the appropriate refresh signals to the dynamic RAM chips.

Communication Line Interface

The communication line interface is the point at which signals are received onto the card and driven from the card onto the communications line. The card is capable of supporting the EIA RS-232-C, CCITT V.24 and EIA RS-449 serial I/O standards. For the purposes of this discussion, the various communications circuits are referred to by their RS-449 names. A comparison of EIA RS-232-C, CCITT V.24 and EIA RS-449 circuits and their respective signal connector pin assignments are given in Section 7.

The EIA RS-449 interface standard specifies a combination of single-ended (EIA RS-423) and differential (EIA RS-422) drivers and receivers. The card uses both single-ended and differential drivers on some lines and only single-ended drivers on others. All of the receivers on the card are differential although some are connected in such a way that they can only receive single-ended signals. The manner in which each signal is driven or received is illustrated in Figure 4-2.

A single-ended driver produces one inverted output whereas the differential counterpart drives both the inverted and non-inverted signal. It is important to note that logical representations of the protocol are preserved in both cases. The advantages of differential drivers and receivers are that they offer higher noise immunity and allow longer cable lengths and higher data signalling rates.

When a differential receiver is connected to a single-ended driver, the remaining input is connected either to ground (RS-232) or to the Receiver Common (RC) circuit of the driving device (RS-449). The various driver/receiver combinations are illustrated in Figure 4-2. The combination used depends on the modem requirements. The receivers on the card can survive an input voltage range of +/- 25 volts and can operate with a maximum common mode input voltage of +/- 7 volts.

Command and Status Words

In addition to data words, command and status words are also exchanged between the host computer and the card. These additional words are transferred across the data bus and the data latches to aid in the process of communication between the host and the card.

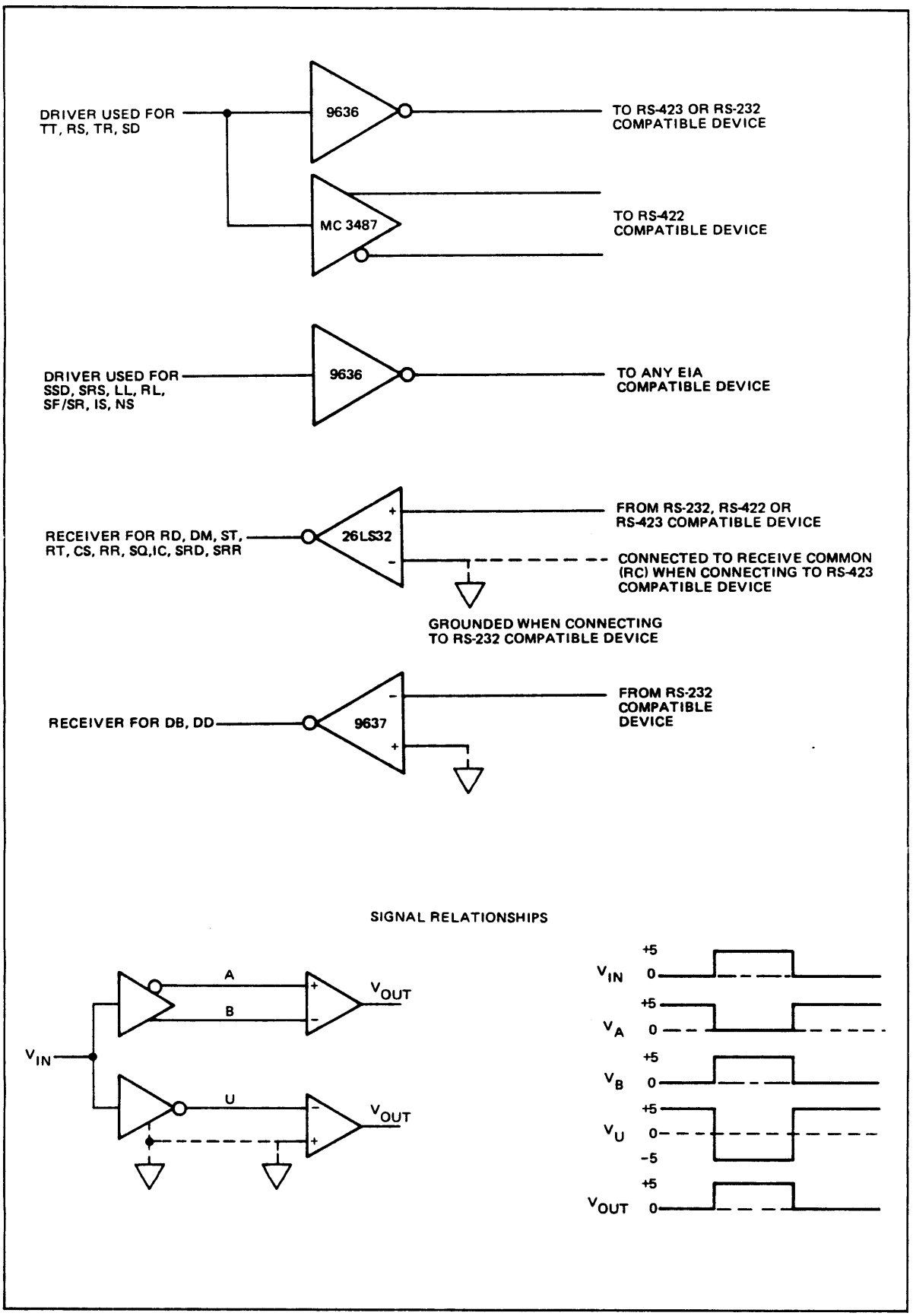


Figure 4-2. Driver/Receiver Combinations

Command words are initiated by the host driver and fall into the following four basic categories:

Type 0 - initiates a data transfer from a card buffer to a host computer buffer.

Type 1 - a single word command sent directly to the card firmware. Examples include disconnect and abort current operation.

Type 2 - initiates a data transfer from a host computer buffer to a card buffer.

Type 3 - specifies that a multiple-word command is to follow.

Status words are generated by the card to inform the host of events that have occurred, are occurring or will be occurring on the card or communications line. Examples of these messages include transfer buffer ready, connect complete, error condition, message block size and modem input line status.

Functional-Level Description

The description given in this section is of a typical operation of the card. The host computer assumed for this discussion is an HP 1000 Computer and the communications device is a modem.

Initially, the HP 1000 has been powered up and the communications line is not yet operational. The process of powering up the host computer resets the logic on the card and invokes a ROM-resident self-test program. The resulting pass/fail message is made available to the host.

The communications line is powered up with TR (Terminal Ready) asserted for those modems possessing an Auto-Answer feature. For modems that do not have this feature, TR is asserted only after receipt of IC (Incoming Call) from the modem. After TR has been asserted in the pertinent manner, the physical connection is made after the modem asserts DM (Data Mode). TR is dropped to disconnect.

After the connection has been made, the normal channel establishment sequence consists of asserting RS (Request to Send) and waiting for CS (Clear to Send) on the transmit side and waiting for assertion of the RR (Receiver Ready) line on the receive side. From this point on, the BISYNC protocol takes over on the entire communications line (from card to card). Refer to Section III for an explanation of the BISYNC protocol.

The steps involved in a transfer from the host computer to the communications line (i.e., an output transfer) are as follows (The numbers in parentheses reference the various data paths and functional areas in Figure 4-1.):

1. The host (software) driver issues a request for output buffers (command type 1) onto the data latches (7) and then causes a Z-80A NMI (5). Because of the NMI, the firmware interprets the data in the latches as a command.

2. When a buffer becomes available, the host driver requests a transfer (command type 2) and enables the DCPC (Dual Channel Port Controller) hardware of the host.

3. The card writes zeros to the output latches (7). This starts the DCPC transfer from the host involving the backplane latches (7), control logic (13), data bus (5), DMA chip (4) and RAM (12).

4. The card interrupts the host (13) when the data transfer is complete.

5. The host may transfer additional blocks of data to the card as buffer space becomes available. Steps 2 through 4 are repeated until the message is transferred from the host to the card in its entirety.

6. Each data block in the RAM buffer on the card is transferred by the card firmware to the SIO (2) when the SIO chip becomes ready for the transfer. BISYNC protocol characters and CRC-16 block check characters are generated by the firmware and transmitted with the data as required. The SIO transmits the data as it is received.

Keep in mind that the CPU (5) is controlling all of the processing on the card by executing instructions that it fetches from ROM (10) and (11).

The steps involved in a transfer from the communications line to the host computer (i.e., an input transfer) are as follows:

1. The host driver enables inputs from the card by enabling a command word (command type 1) into the data latches (7).

2. The card firmware then sends a status word via the data latches (7) to the host driver informing it that an input buffer is available.

3. The host driver issues a request for input data (command type 0) and enables the DCPC hardware of the host computer.

4. The card enables the first data word into the data latches (7) and asserts SRQ via the backplane logic (13).

5. The host driver begins the data transfer and the data block is transferred from the RAM (13) on the card to the host via a DMA chip (4), the data bus (6), the backplane latches (7) and the backplane handshake logic (13). Steps 2 through 5 are repeated until the entire message has been transferred.

6. The host is interrupted when the transfer is complete.

Section 5
Maintenance

Introduction

This section provides maintenance information for the HP 12793A BISYNC Modem Interface Kit. Included are preventive maintenance instructions and troubleshooting information.

Preventive Maintenance

There is no preventive maintenance (PM) necessary for the HP 12793A BISYNC Modem Interface Kit other than a routine inspection of the equipment which can be performed at the same time that PM is done for the entire system. The card and cables should be checked for broken components, or the presence of foreign objects.

A self-test, residing in the firmware, is executed each time that power is applied to the card or the card is reset. In this manner, the interface card is checked automatically and only requires more thorough testing when specific failures occur.

Troubleshooting Techniques

CAUTION

ALWAYS TURN POWER OFF TO THE COMPUTER AND OTHER ASSOCIATED EQUIPMENT WHEN INSERTING OR REMOVING INTERFACE CARDS OR CABLES. FAILURE TO DO SO COULD RESULT IN DAMAGE TO THE EQUIPMENT.

CAUTION

STATIC SENSITIVE DEVICES

THE ROMS, RAMS, AND Z-80A COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE REPLACING.

Once it has been determined that the hardware of the HP 1000-to-HP 3000 link is failing, proceed as follows to localize the failure to the specific component failing:

1. Run the following tests at the HP 1000 node:

   a. DSINF card configuration check. (Follow the procedure outlined in the interface card configuration check paragraphs in Section 2 of this manual.)

   b. Firmware Self-test.

   c. Modem Diagnostic Hood Test.

2. If the above procedures are carried out successfully, it is reasonably certain that the interface cards and software/firmware at the HP 1000 node are operational. This implies that the failure is due to the cabling, the modems used, the line quality, or the interface hardware at the HP 3000 node. The interface at the HP 3000 and the modem in the link should be checked out at this time if possible. Refer to the appropriate manuals for self-test/diagnostic information. Other troubleshooting aids for investigating line quality and use are discussed in the last paragraphs of this section.

3. If a failure is found using one of the above test procedures, replace the failing card or firmware and repeat the test that failed to verify that the problem has been properly corrected. If the problem is still present with new equipment, refer to the last paragraph of this manual for further troubleshooting procedures.

Firmware Self-Test

A self-test is available for the interface card included with the HP 12793A. The test examines CPU operation, on-board DMA operation, counter/timer chip performance, RAM and ROM memory, and some parts of the receiver/driver circuits and controller. The test does not check the backplane circuitry on the card.

The self-test is located in the firmware ROMs on the interface card and is run at power up, or whenever the card is reset (whenever a CLC 0 is sent to the card). Therefore it can be run by pushing the PRESET button on the front panel (such as during a re-boot procedure), or by cycling power on the system. Note that after cycling power, it will be required to reinitialize DS and system software. It is recommended that the node is quiesced before powering down to allow all pending DS transactions to be completed and prevent new ones from starting before running the self-test. To quiesce the node, enter the commands RU,DSMOD<cr> and, after DSMOD prompts for a command, enter /Q. (For a description of DSMOD, refer to the DS/1000-IV Network Manager's Manual, HP part number 91750-90003.) DSMOD prompts for the network security code which can be obtained from the network manager. The default security code is DS. Once the "NODE IS QUIESCENT" message appears on the screen, cycle the power on the computer.

Self-test results are made available to the driver once the test is complete. To find out if the card passed the self-test, try executing the LU command on that card after running DSINF, as described in the interface card configuration check given in Section 2. The LEDs on the card will also indicate successful completion of the tests with LED0 through LED2 being lit and LED3 indicating clock selection (lit for external clock; off for internal clock).

Modem Diagnostic Hood Test

It is possible for the firmware to sense the presence of the modem diagnostic hood when it is installed on the card in place of the normal modem cable. When present, the self-test does a check of all of the line drivers and receivers and the message sending capabilities of the card. To run the modem diagnostic hood test, proceed as follows:

1. Quiesce the local node. This allows all pending transactions to be completed and prevents new ones from starting before running the self-test. Follow the same procedure used in the self-test procedure for quiescing the node. Remove power from the computer and the modem once the node is quiescent.

2. Remove the modem cable from the interface card and install the modem diagnostic hood in its place, orienting the connector the same as all other connectors in the card cage.

3. Restore power to the system. When this occurs, the firmware self-test is automatically executed on the card. The results of the test are returned to the software driver. The LEDs on the card will also indicate successful completion of the self-test, but will not indicate that the hood was sensed. Restore the operating system and check that the self-test completed successfully and that the hood was sensed by running DSINF and checking the information returned with the LU command.

4. To remove the modem diagnostic hood, remove power from the computer and replace the hood with the modem cable.

5. Restore power to the computer and modem and reinitialize the system and DS software.

Since the self-test with the hood installed checks more areas of the card (specifically the line drivers and receivers area of the interface), it is possible for the card to pass the self-test without the hood installed and fail when the modem diagnostic hood is installed (indicating a hardware failure in the line drivers/receivers area). Therefore it is important that the test is run both with and without the modem diagnostic hood installed.

Other Troubleshooting Aids

If problems occur that cannot be identified using the hardware tests described above, there are other troubleshooting tools available. However, these tools require more familiarity with hardware operations, BISYNC protocol, and characteristics of line use for the link being tested. Therefore, a review of the Principle of Operation and Protocol sections of this manual is recommended before proceeding. Detailed troubleshooting techniques are further discussed in the DS/1000-IV Network Manager's Manual, HP part number 91750-90003. Refer to that manual for information on DS utility programs available and their use as troubleshooting aids.

Section 6
Replaceable Parts

Introduction

This section contains information for ordering replaceable parts for the HP 12793A BISYNC Modem Interface Kit. Table 6-1 gives a list of replaceable parts and Table 6-2 contains the names and addresses of the manufacturers of the parts.

Replaceable Parts

Table 6-1 contains a list of replaceable parts in reference designation order. The following information is listed for each part:

1. Reference designation of the part.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity (QTY).
5. Description of the part.
6. A five-digit manufacturer's code number of a typical manufacturer of the part. Refer to Table 6-2 for an explanation of the manufacturer codes.
7. The manufacturer's part number.

Ordering Information

To order replacement parts or to obtain information on parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office (Sales and Service Offices are listd at the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will insure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, specify the following information:

1. Identification of the kit containing the part (refer to Section 1 of this manual).
2. Description and function of the part.
3. Quantity required.

Table 6-1. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	5061-3418	5	1	MX PROGRAM SER IF	28480	5061-3418
CR5	1990-0662	0	1	LED=VISIBLE LUM=INT=200UCD IF=5MA=MAX	28480	1990-0662
Q1	1853-0015	7	1	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
Q2	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=300MW	28480	1854-0019
R5	1810-0276	2	3	NETWORK=RES 10=8IP1.5K OHM X 9	01121	210A152
R6	1810-0279	5	4	NETWORK=RES 10=8IP4.7K OHM X 9	01121	210A472
R7	1810-0279	5		NETWORK=RES 10=8IP4.7K OHM X 9	01121	210A472
R12	1810-0279	5		NETWORK=RES 10=8IP4.7K OHM X 9	01121	210A472
R13	1810-0279	5		NETWORK=RES 10=8IP4.7K OHM X 9	01121	210A472
R14	1810-0276	2		NETWORK=RES 10=8IP1.5K OHM X 9	01121	210A152
R16	1810-0276	2		NETWORK=RES 10=8IP1.5K OHM X 9	01121	210A152
R19	1810-0280	8	2	NETWORK=RES 10=8IP10.0K OHM X 9	01121	210A103
R39	1810-0280	8		NETWORK=RES 10=8IP10.0K OHM X 9	01121	210A103
S1	3101-1983	9	1	SWITCH=DIP, 8=ROCKER	28480	3101-1983
U11	1820-2203	0	4	IC RCVR TTL LS LINE RCVR QUAD	34335	AM26LS32PC
U12	1820-1729	3	2	IC LCH TTL LS COM CLEAR 8-BIT	01295	SN74LS259N
U13	1820-2300	8	1		28480	1820-2300
	1200-0654	7	4	SOCKET=IC 40=CONT DIP DIP=SLDR	28480	1200-0654
U15	1820-1430	3	1	IC CNTR TTL LS 4IN SYNCHRO POS=EDGE=TRIG	01295	SN74LS161AN
U21	1820-2203	0		IC RCVR TTL LS LINE RCVR QUAD	34335	AM26LS32PC
U22	1820-1298	1	1	IC MUXR/DATA=SEL TTL LS 8=TO=1=LINE	01295	SN74LS251N
U25	1820-1216	3	1	IC DCDR TTL LS 3=TO=8=LINE 3=INP	01295	SN74LS138N
U26	1813-0129	0	1	IC OSC HYBRID	34344	K1100A
	1200-0638	7	1	SOCKET=IC 14=CONT DIP DIP=SLDR	28480	1200-0638
U27	1820-1989	7	1	IC CNTR TTL LS 8IN DUAL 4=BIT	07263	74LS393PC
U31	1820-2203	0		IC RCVR TTL LS LINE RCVR QUAD	34335	AM26LS32PC
U33	1820-2299	4	2		28480	1820-2299
	1200-0654	7		SOCKET=IC 40=CONT DIP DIP=SLDR	28480	1200-0654
U35	5090-1614	0	1	IC=6309=1	28480	5090-1614
U36	1820-1197	9	3	IC GATE TTL LS NAND QUAD 2=INP	01295	SN74LS00N
U37	1820-1080	9	11	IC DRVR TTL LINE DRVR DUAL 6=INP	18324	N8T13N
U38	1820-0799	5	1	IC DRVR TTL NAND DUAL 2=INP	01295	SN754528P
U41	1820-2203	0		IC RCVR TTL LS LINE RCVR QUAD	34335	AM26LS32PC
U42	1820-1112	8	1	IC FF TTL LS D=TYPE POS=EDGE=TRIG	01295	SN74LS74AN
U43	1820-2299	4			28480	1820-2299
	1200-0654	7		SOCKET=IC 40=CONT DIP DIP=SLDR	28480	1200-0654
U45	1820-0693	8	2	IC FF TTL S D=TYPE POS=EDGE=TRIG	01295	SN74S74N
U46	1820-1201	6	2	IC GATE TTL LS AND QUAD 2=INP	01295	SN74LS08N
U47	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6=INP	18324	N8T13N
U51	1820-2145	9	1	IC DRVR TTL LINE DRVR QUAD	04713	MC3487P
U52	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U55	1820-0683	6	1	IC INV TTL S HEX 1=INP	01295	SN74S04N
U56	1820-1440	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
U57	1820-1197	9		IC GATE TTL LS NAND QUAD 2=INP	01295	SN74LS00N
U61	1820-1244	7	2	IC MUXR/DATA=SEL TTL LS 4=TO=1=LINE DUAL	01295	SN74LS153N
U62	1820-1729	3		IC LCH TTL LS COM CLEAR 8-BIT	01295	SN74LS259N
U63	1820-2298	3	1		28480	1820-2298
	1200-0654	7		SOCKET=IC 40=CONT DIP DIP=SLDR	28480	1200-0654
U65	1820-0693	8		IC FF TTL S D=TYPE POS=EDGE=TRIG	01295	SN74S74N
U66	1820-1416	5	1	IC SCHMITT=TRIG TTL LS INV HEX 1=INP	01295	SN74LS14N
U67	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6=INP	18324	N8T13N
U71	1820-1244	7		IC MUXR/DATA=SEL TTL LS 4=TO=1=LINE DUAL	01295	SN74LS153N
U72	1818-0341	8	8	IC NMOS 16384=BIT RAM DYN 200=NS 3=8	0003J	UPD416D-2
	1200-0607	0	8	SOCKET=IC 16=CONT DIP DIP=SLDR	28480	1200-0607
U74	1820-2301	9	1		28480	1820-2301
	1200-0567	1	3	SOCKET=IC 28=CONT DIP DIP=SLDR	28480	1200-0567
U75	1820-1208	3	2	IC GATE TTL LS OR QUAD 2=INP	01295	SN74LS32N
U76	1820-1202	7	1	IC GATE TTL LS NAND TPL 3=INP	01295	SN74LS10N
U77	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6=INP	18324	N8T13N
U81	1820-2198	2	1	IC RCVR TTL S LINE RCVR DUAL	07263	9637ATC
U82	1818-0341	8		IC NMOS 16384=BIT RAM DYN 200=NS 3=8	0003J	UPD416D-2
	1200-0607	0		SOCKET=IC 16=CONT DIP DIP=SLDR	28480	1200-0607
U85	1820-1208	3		IC GATE TTL LS OR QUAD 2=INP	01295	SN74LS32N
U86	1820-1201	6		IC GATE TTL LS AND QUAD 2=INP	01295	SN74LS08N
U87	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6=INP	18324	N8T13N
U91	1820-2117	5	6	IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U92	1818-0341	8		IC NMOS 16384=BIT RAM DYN 200=NS 3=8	0003J	UPD416D-2
	1200-0607	0		SOCKET=IC 16=CONT DIP DIP=SLDR	28480	1200-0607
	1200-0567	1		SOCKET=IC 28=CONT DIP DIP=SLDR	28480	1200-0567

Table 6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U95	5090-0599	8	1	IC-ROM	28480	5090-0599
U96	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U97	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U101	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U102	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
	1200-0483	0	1	SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0483
U106	1820-1184	4	1	IC BFR TTL NOR QUAD 2-INP	01295	SN7428N
U107	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U201	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U202	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
U206	1820-1997	7	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U207	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U301	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U302	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U303	1820-1470	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U304	1820-2075	4	1	IC MISC TTL LS	01295	SN74LS245N
U306	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U307	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U401	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U402	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U403	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U404	1820-1917	1	1	IC BFR TTL LS LINE DRVR UCTL	01295	SN74LS240N
U406	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U407	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U501	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U502	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U503	1820-1207	2	1	IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
U504	1826-0220	9	1	IC V RGLTR TO-39	27014	LM320H-05
	1200-0185	9	1	INSULATOR-XSTR NYLON	28480	1200-0185
U506	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U507	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
				MISCELLANEOUS PARTS		
	1480-0116	8	1	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
	5061-3431	2	1	AXIAL INSERTION	28480	5061-3431

Table 6-2. Manufacturer's Code List

CODE NO.	MANUFACTURER ADDRESS	CODE NO.	MANUFACTURER ADDRESS
0003J	Nippon Electric Co.	07263	Fairchild Semiconductor Div. ... Mt. View, CA 94042
01121	Allen-Bradley Co. ... Milwaukee, WI 53204	18324	Signetics Corp. ... Sunnyvale, CA 94086
01295	Texas Instr. Inc. Semicond. Cmpnt. Div. ... Dallas TX 75222	27014	Natl.Semiconductor Corp. ... Santa Clara, CA 95051
03508	General Electric Co., Semiconductor Prod. Dept. ... Syracuse, NY 13201	28480	Hewlett-Packard Co. Corporate Hq. ... Palo Alto, CA 94304
04713	Motorola Semiconductor Prod. .. Phoenix, AZ 85062	34335	Advanced Micro Dev. Inc. .... Sunnyvale, CA 94086
		34344	Motorola Inc. ... Franklin Park, IL 60131

Section 7
Servicing Diagrams and Information

Introduction

This section contains servicing diagrams and information for the HP 12793A BISYNC Modem Interface Kit.

Table 7-1. Backplane Connections (Connector P1)

PIN NO.	SIGNAL MNEMONIC	SIGNAL NAME
1	GND	Ground
2	GND	Ground
3	PRL	Priority Low
4	FLAGL	Flag Signal, Lower Select Code
5	SFC	Skip if Flag is Clear
6	IRQL	Interrupt Request, Lower Select Code
7	CLF	Clear Flag
8	IEN	Interrupt Enable
9	STF	Set Flag
10	IAK	Interrupt Acknowledge
11	T3	I/O Time Period 3
12	SKF	Skip on Flag
13	CRS	Control Reset
14	LSCM	Select Code Most Significant Digit (Lower Address)
15	IOG	I/O Group
16	LSCL	Select Code Least Significant Digit (Lower Address)
17	POPIO	Power On Preset to I/O
18	IOBI 16	I/O Bus Input, bit 16 (M-Series only)
19	SRQ	Service Request
20	IOO	I/O Data Output Signal
21	CLC	Clear Control
22	STC	Set Control
23	PRH	Priority High
24	IOI	I/O Data Input Signal
25	SFS	Skip if Flag is Set
26	IOBI 0	I/O Bus Input, bit 0
27	IOBI 8	I/O Bus Input, bit 8
28	IOBI 9	I/O Bus Input, bit 9
29	IOBI 1	I/O Bus Input, bit 1
30	IOBI 2	I/O Bus Input, bit 2
31	IOBI 10	I/O Bus Input, bit 10
32	SIR	Set Interrupt Request
33	IRQH	Interrupt Request, Higher Select Code

Table 7-1. Backplane Connector P1 (Continued)

34	HSCL	Select Code Least Significant Digit (Higher Address)
35	IOBO 0	I/O Bus Output, bit 0
36	+28 Volts	
37	HSCM	Select Code Most Significant Digit (Higher Address)
38	IOBO 1	I/O Bus Output, bit 1
39	+5 Volts	
40	+5 Volts	
41	IOBO 2	I/O Bus Output, bit 2
42	IOBO 4	I/O BUs Output, bit 4
43	+12 Volts	
44	+12 Volts	
45	IOBO 3	I/O Bus Output, bit 3
46	ENF	Enable Flag
47	-2 Volts	
48	-2 Volts	
49	FLGH	Flag Signal, Higher Select Code
50	RUN	Run
51	IOBO 5	I/O Bus Output, bit 5
52	IOBO 7	I/O Bus Output, bit 7
53	IOBO 6	I/O BUs Output, bit 6
54	IOBO 8	I/O Bus Output, bit 8
55	IOBO 11	I/O Bus Output, bit 11
56	IOBO 9	I/O Bus Output, bit 9
57	IOBO 12	I/O Bus Output, bit 12
58	IOBO 10	I/O Bus Output, bit 10
59	NOT USED	
60	IOBI 11	I/O Bus Input, bit 11
61	IOBO 13	I/O Bus Output, bit 13
62	EDT	End Data Transfer (DCPC)
63	NOT USED	
64	IOBI 3	I/O Bus Input, bit 3
65	IOBO 14	I/O Bus Output, bit 14
66	PON	Power On Normal
67	BIOO	"Not" Block I/O Output (E-Series only)
68	NOT USED	
69	-12 Volts	

Table 7-1. Backplane Connections (Connector P1) (Continued)

PIN NO.	SIGNAL MNEMONIC	SIGNAL NAME
70	-12 Volts	
71	NOT USED	
72	NOT USED	
73	SFSB	Skip if FLag is Set Buffered (M-Series only)
73	BIOI	"Not" Block I/O Input (E-Series only)
74	IOBO 15	I/O Bus Output, bit 15
75	NOT USED	
76	NOT USED	
77	IOBI 4	I/O Bus Input, bit 4
78	IOBI 12	I/O Bus Input, bit 12
79	IOBI 13	I/O Bus Input, bit 13
80	IOBI 5	I/O Bus Input, bit 5
81	IOBI 6	I/O Bus Input, bit 6
82	IOBI 14	I/O Bus Input, bit 14
83	IOBI 15	I/O Bus Input, bit 15
84	IOBI 7	I/O Bus Input, bit 7
85	GND	Ground
86	GND	Ground

Table 7-2. Communication Line Connector (Connector J1).

PIN NO.	SIGNAL MNEMONIC*	SIGNAL DEFINITION
1A	---	No Connection
1B	+12V	+12 Volts Power
2A	---	No Connection
2B	+12V	+12 Volts Power
3A	SSD	Secondary Send Data
3B	---	No Connection
4A	---	No Connection
4B	-12V	-12 Volts Power
5A	---	No Connection
5B	-12V	-12 Volts Power
6A	---	No Connection
6B	---	No Connection
7A	SRS	Secondary Request to Send
7B	TR(A)	Terminal Ready
8A	SD(U)	Send Data
8B	TT(B)	Terminal Timing
9A	RS(U)	Request to Send
9B	TT(U)	Terminal Timing
10A	TR(B)	Terminal Ready
10B	DAMPRT(B)	
11A	RS(A)	Request to Send
11B	TR(U)	Terminal Ready
12A	TT(A)	Terminal Timing
12B	---	No Connection
13A	SD(B)	Send Data
13B	SD(A)	Send Data
14A	---	No Connection
14B	RS(B)	Request to Send
15A	DAMPST(B)	
15B	RT(B)	Receive Timing
16A	CS(B)	Clear To Send
16B	DAMPRD(B)	
17A	CS(A)	Clear to Send
17B	---	No Connection
18A	SQ	Signal Quality
18B	RC	Receive Common
19A	ST(B)	Send Timing
19B	---	No Connection
20A	RD(B)	Receive Data
20B	ST(A)	Send Timing
21A	---	No Connection
21B	**BX16IN	
22A	SRR	Secondary Receiver Ready
22B	---	No Connection

Table 7-2. Communication Line Connector J1 (Continued)

PIN NO.	SIGNAL MNEMONIC*	SIGNAL DEFINITION
23A	RD(A)	Receive Data
23B	TM	Test Mode
24A	RR(B)	Receiver Ready
24B	IC	Incoming Call
25A	SG	Signal Ground
25B	SC	Signal Common
26A	RR(A)	Receiver Ready
26B	**BDATACLK+	
27A	DM(A)	Data Mode
27B	DM(B)	Data Mode
28A	SF/SR	Select Frequency/Signaling Rate
28B	DD	Receive Timing
29A	**ASYNCCLK+	
29B	DA	Terminal Timing
30A	**X16IN	
30B	RT(A)	Receive Timing
31A	SCS	Secondary Clear to Send
31B	DB	Send Timing
32A	SRD	Secondary Receive Data
32B	RL	Remote Loopback
33A	LL	Local Loopback
33B	NS	New Signal
34A	IS	Terminal In Service
34B	---	No Connection
35A	---	No Connection
35B	GND	Power Ground
36A	---	No Connection
36B	GND	Power Ground
37A	---	No Connection
37B	GND	Power Ground
38A	(SHIELD)	
38B	---	No Connection
39A	---	No Connection
39B	+5V	+5 Volts Power
40A	---	No Connection
40B	+5V	+5 Volts Power

* The (A) or (B) after a mnemonic indicates portions of a differential input or output.
The (U) after a mnemonic indicates a single ended version of a signal that appears elsewhere as differential.

** These are TTL level signals for compatibility, they should be used only to loop back for proper firmware operation.

Table 7-3. Serial I/O Circuits and Equivalents

SIGNAL RS-449	SIGNAL RS-232	CCITT V.24	DEFAULT VALUE*	FUNCTION
RD	BB	104	—	RECEIVE DATA
SD	BA	103	1	SEND DATA
CS	CB	106	—	CLEAR TO SEND
RS	CA	105	0	REQUEST TO SEND
TR	CD	108.2	0	TERMINAL READY
RR	CF	109	—	RECEIVER READY
ST	DB	114	—	SEND TIMING
RT	DD	115	—	RECEIVE TIMING
TT	DA	113	—	TERMINAL TIMING
IC	CE	125	—	INCOMING CALL
DM	CC	107	—	DATA MODE
TM	—	142	0	TEST MODE
LL	—	141	0	LOCAL LOOPBACK
RL	—	140	0	REMOTE LOOPBACK
SQ	CG	110	—	SIGNAL QUALITY
SF	CH	126	0	SELECT FREQUENCY
SR	CH	111	0	SELECT SIGNALING RATE
IS	—	—	1	TERMINAL IN SERVICE
NS	—	—	0	NEW SIGNAL
SRD	SBB	119	—	SEC. RECEIVE DATA
SSD	SBA	118	1	SEC. SEND DATA
SRS	SCA	120	0	SEC. REQUEST TO SEND
SCS	SCB	121	—	SEC. CLEAR TO SEND
SRR	SCF	122	—	SEC. RECEIVER READY
SG	AB	102	—	SIGNAL GROUND
SC	—	102a	—	SEND COMMON
RC	—	102b	—	RECEIVE COMMON
—	AA	101	—	PROTECTIVE GROUND

* Pertains to the HP 12793A Interface only.

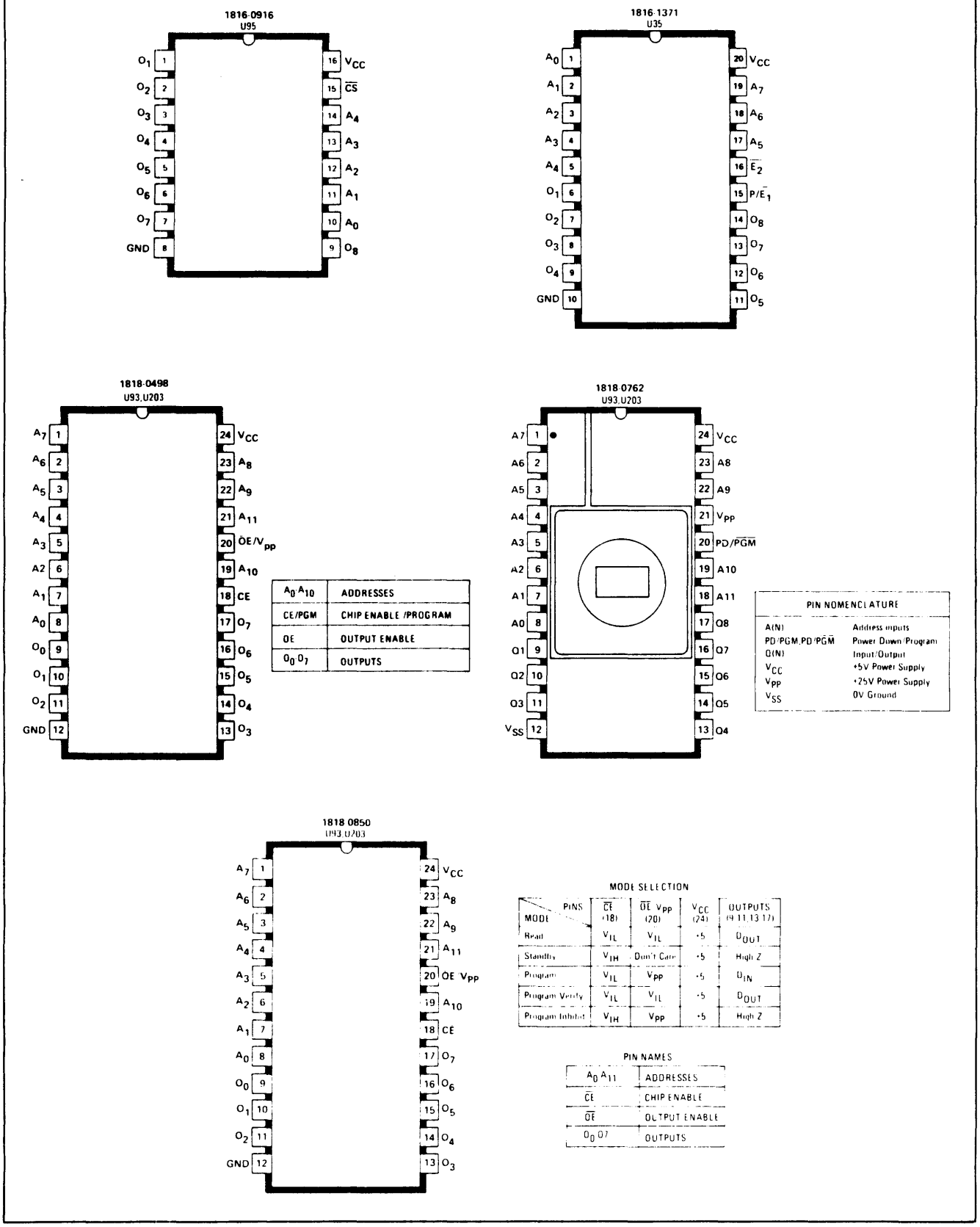


Figure 7-1. Integrated Circuit Base Diagrams.

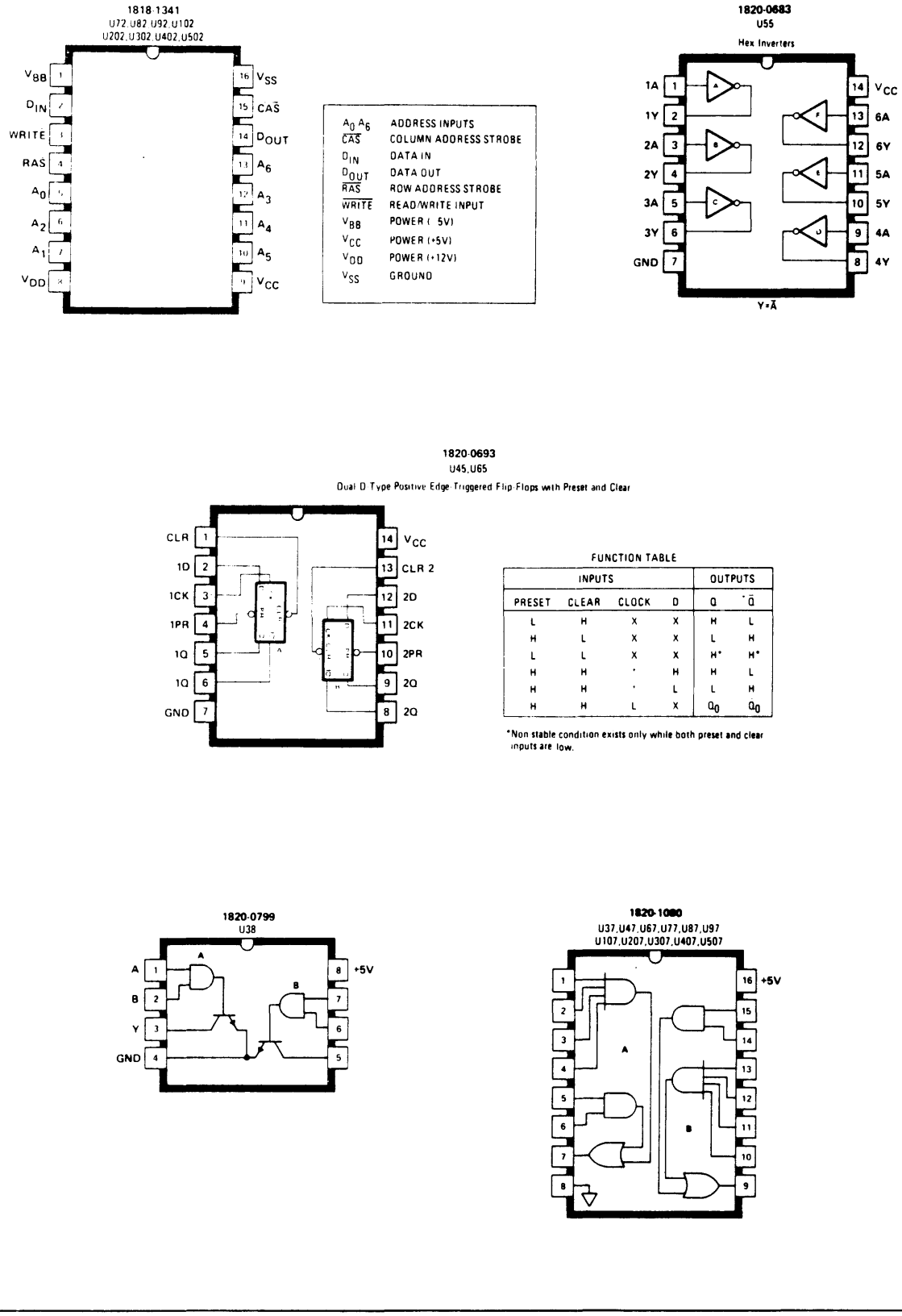
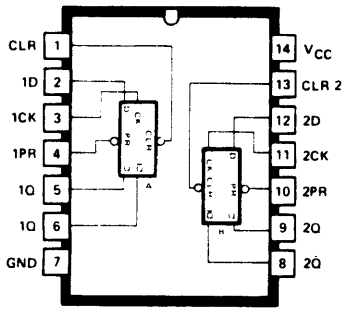


Figure 7-1. Integrated Circuit Base Diagrams (Continued)

1820-1112
U42

Dual D Type Positive-Edge-Triggered Flip Flops with Preset and Clear

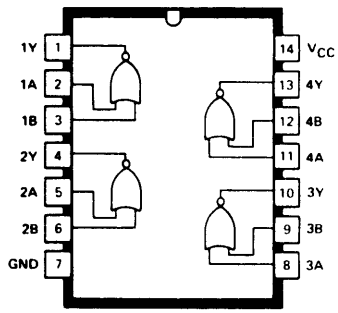


FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

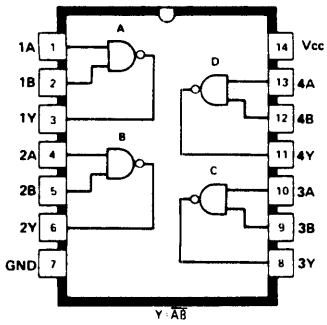
*Non-stable condition exists only while both preset and clear inputs are low.

1820-1184
U106



1820-1197
U36,U57,U96

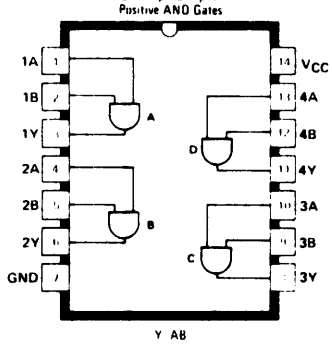
Quadruple 2-Input Positive-NAND Gates



Y = $\overline{AB}$

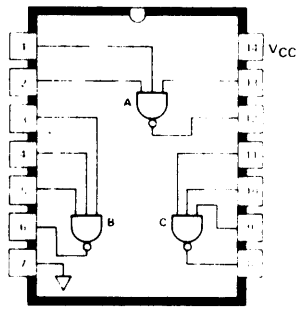
1820-1201
U46,U86

Quadruple 2-Input Positive AND Gates



Y = AB

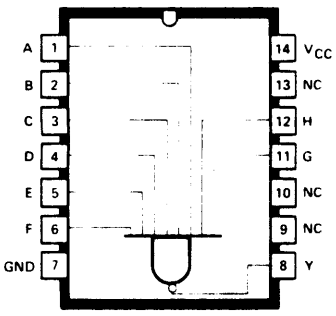
1820-1202
U76



1820-1207
U503

Type TTL Compatible

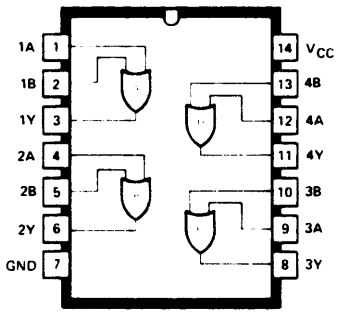
Description 8-input, positive NAND Gate



1820-1208
U75,U85

Type TTL Compatible

Description Dual-input, positive OR Gates



1820-1216
U25

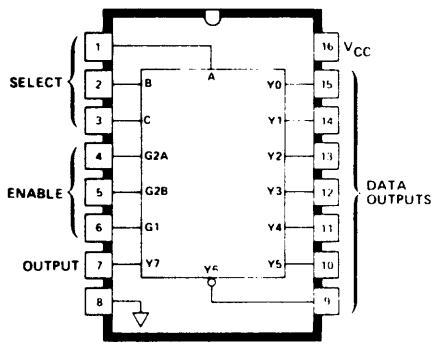
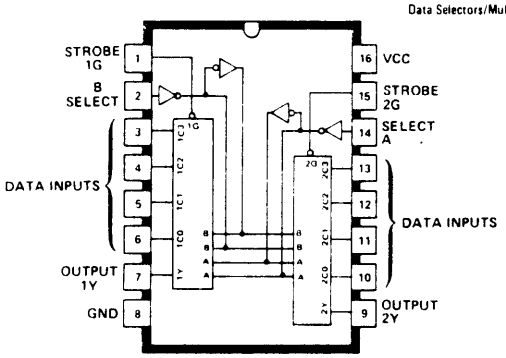


Figure 7-1. Integrated Circuit Base Diagrams (Continued)

1820-1244

U61,U71

Dual 4-Line to 1-Line
Data Selectors/Multiplexers



FUNCTION TABLE

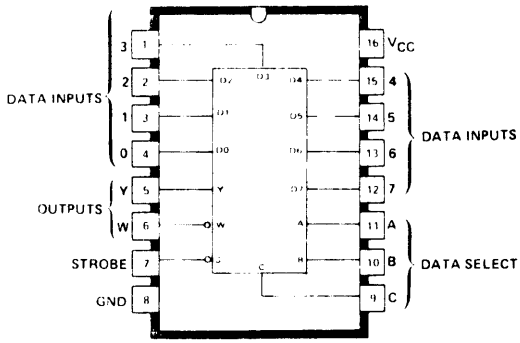
SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level
L = low level
X = irrelevant

1820-1298

U22

DATA SELECTORS/MULTIPLEXERS
WITH 3-STATE OUTPUTS



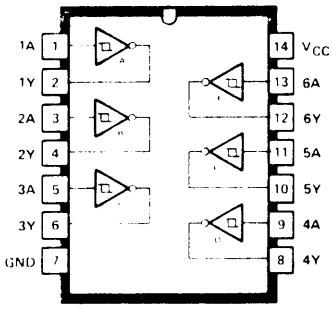
FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	D0
L	L	H	L	D1	D1
L	H	L	L	D2	D2
L	H	H	L	D3	D3
H	L	L	L	D4	D4
H	L	H	L	D5	D5
H	H	L	L	D6	D6
H	H	H	L	D7	D7

1820-1416

U66

Description: Hex Inverters.



1820-1430

U15

Description: Synchronous 4-Bit Counter with
Direct Clear

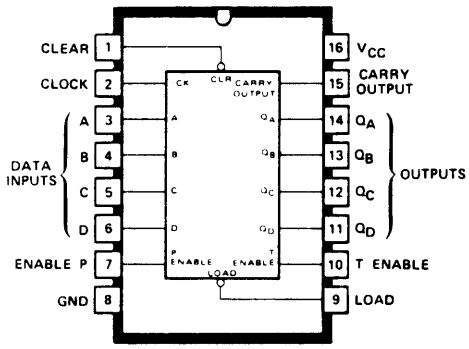


Figure 7-1. Integrated Circuit Base Diagrams (Continued)

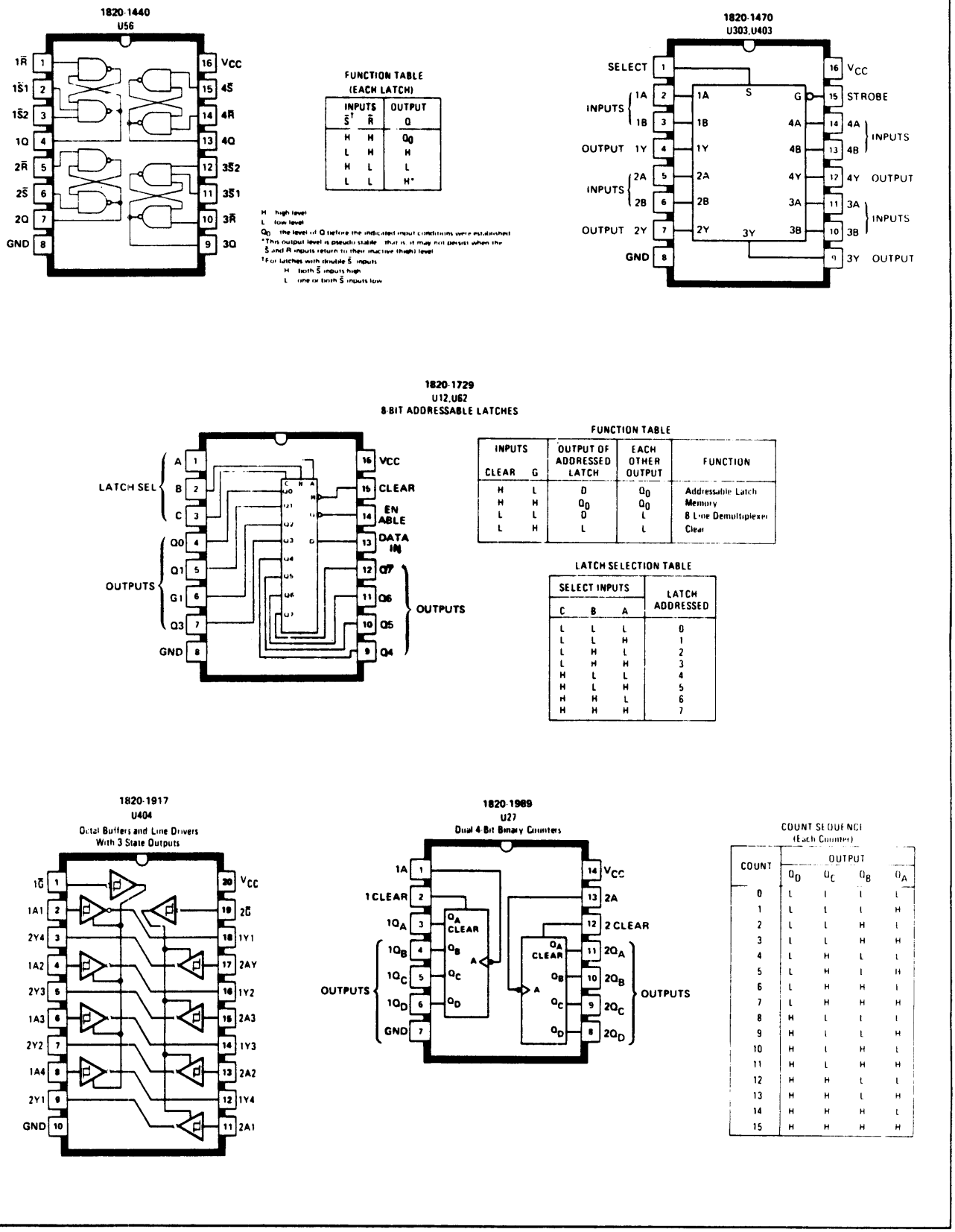


Figure 7-1. Integrated Circuit Base Diagrams (Continued)

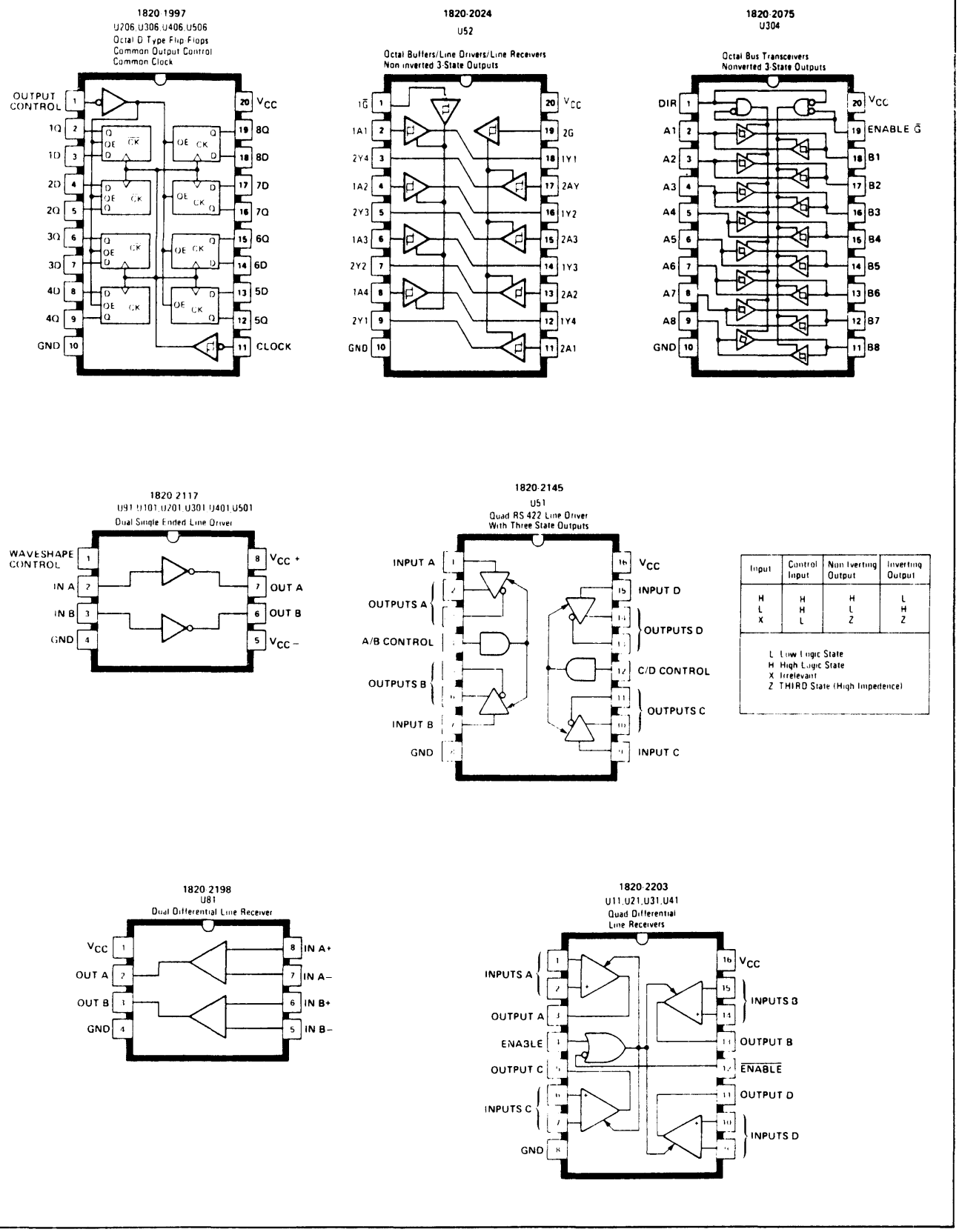


Figure 7-1. Integrated Circuit Base Diagrams (Continued)

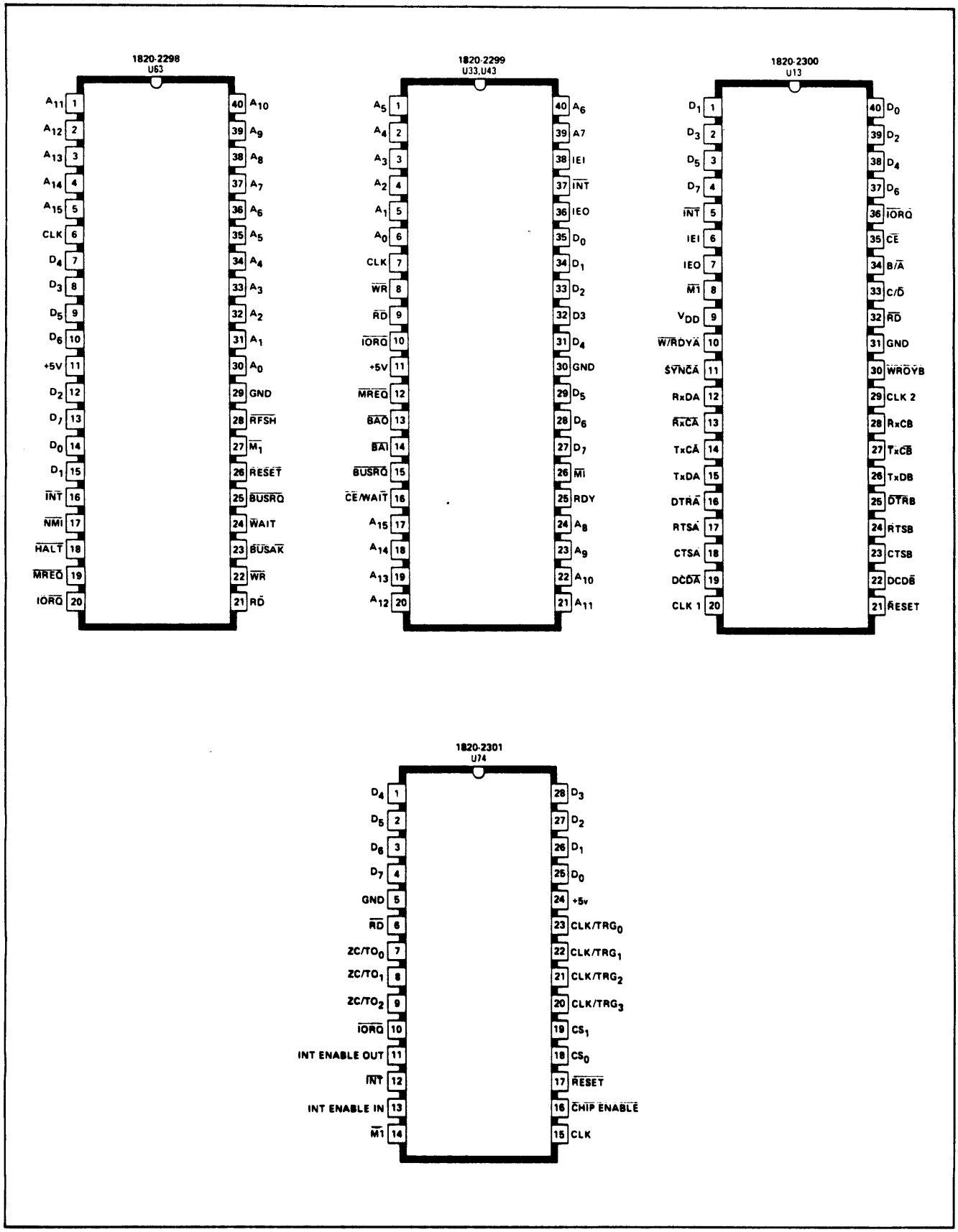


Figure 7-1. Integrated Circuit Base Diagrams (Continued)

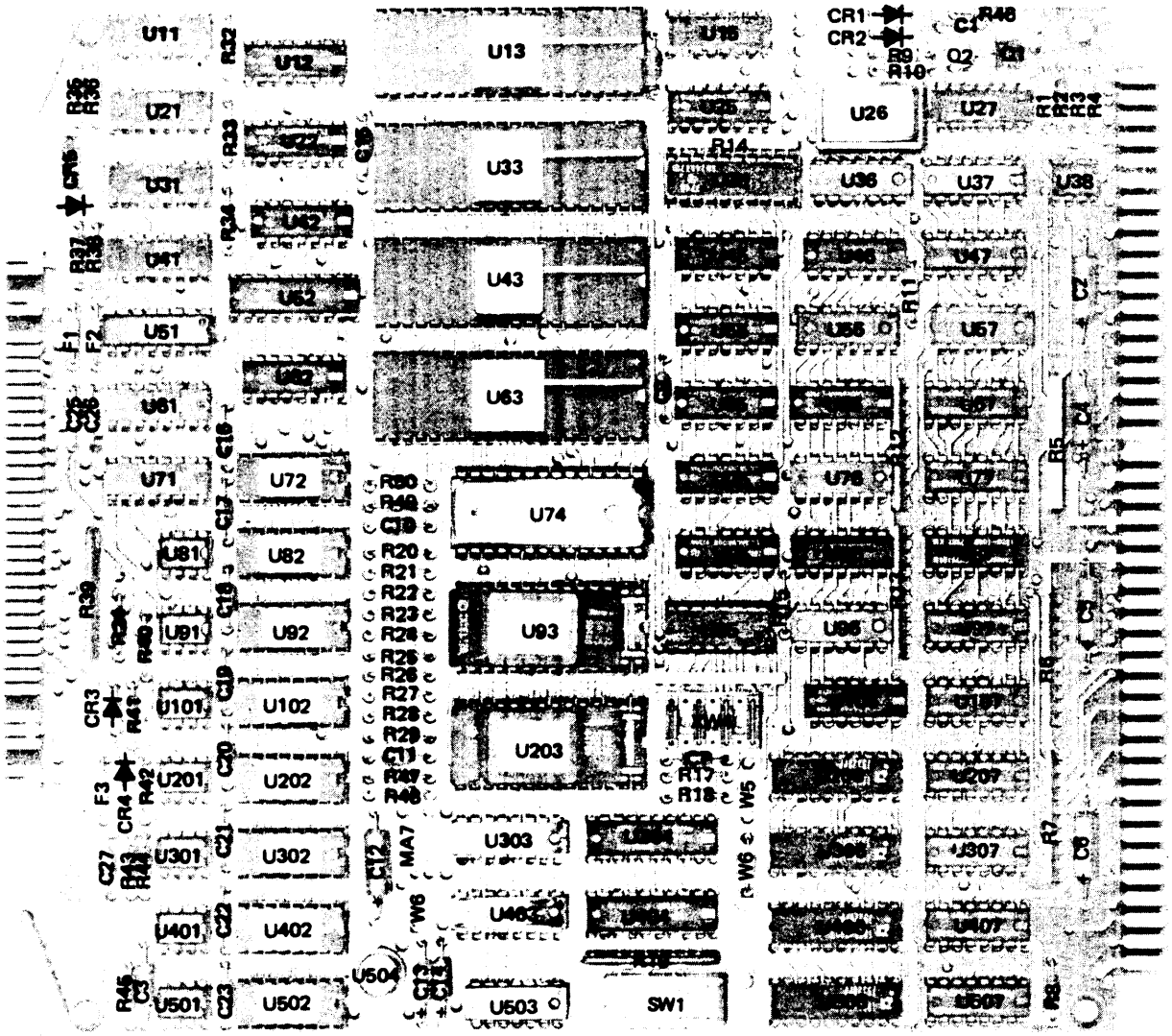


Figure 7-2. BISYNC Modem Interface Card Parts Location Diagram

Figure 7-3. HP 12794A HDLC Modem Interface Schematic Logic Diagram.

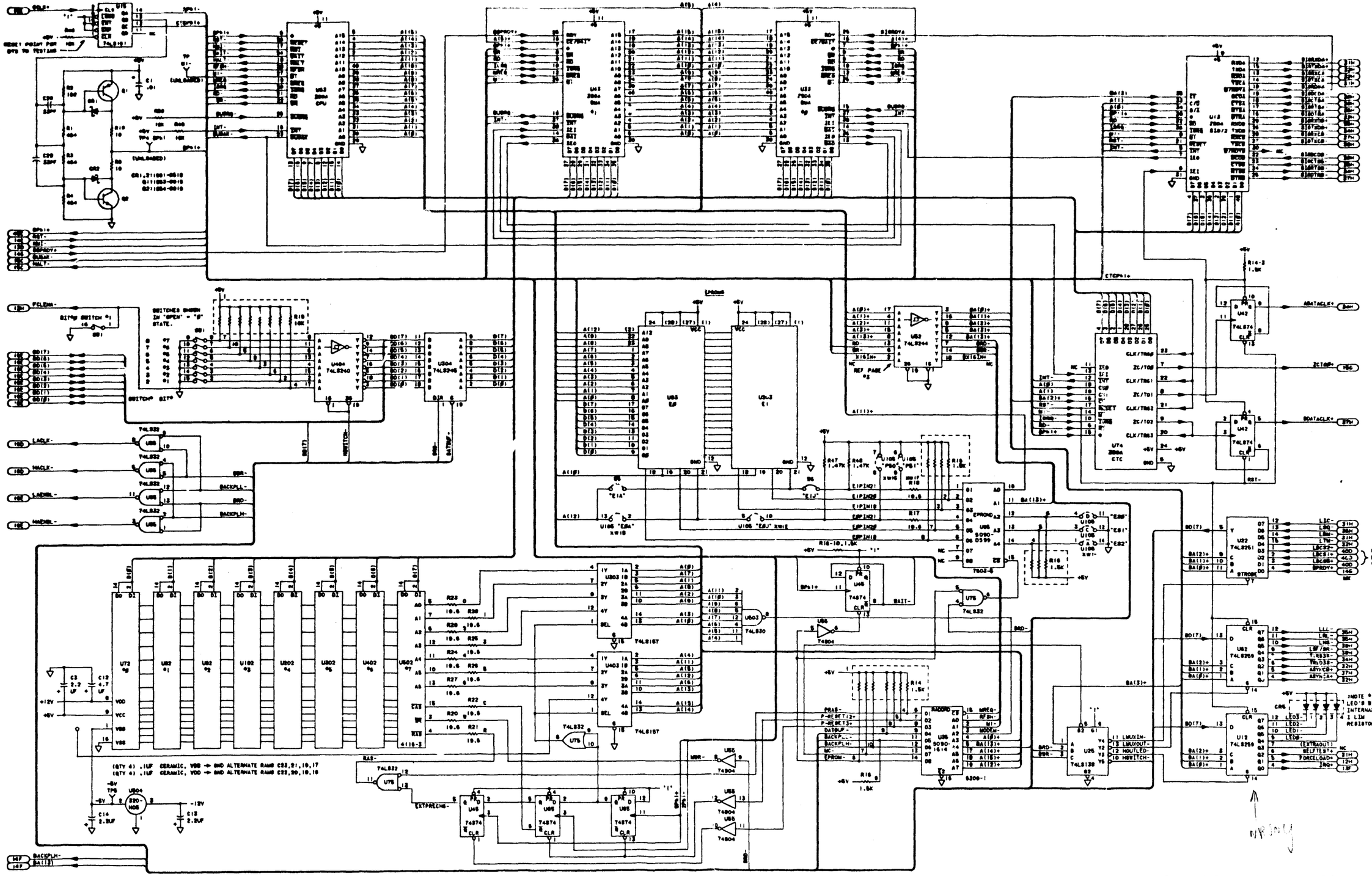


Figure 7-3. HP 12794A Interface Schematic Logic Diagram (Cont.)
7-19/7-20

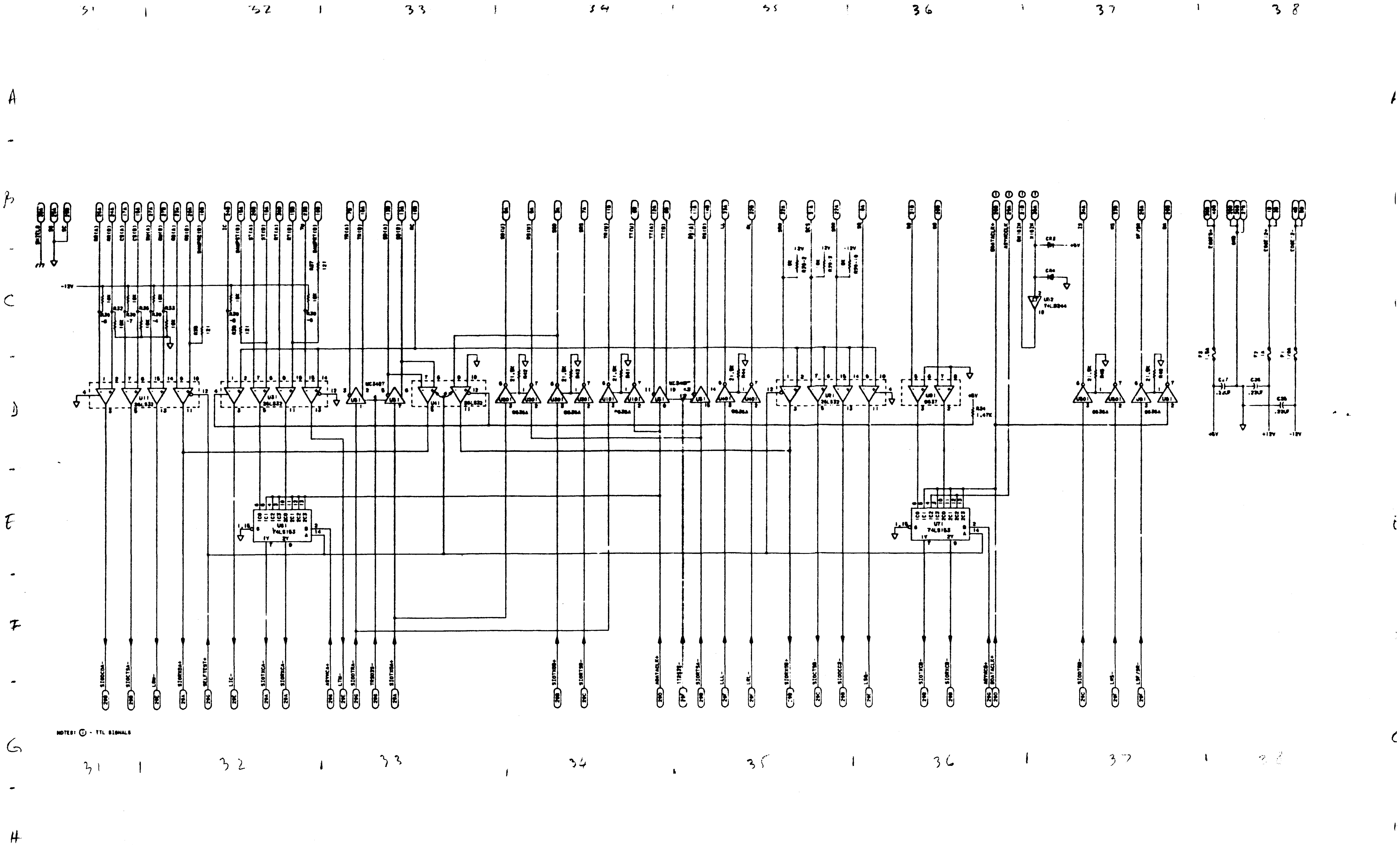


Figure 7-3. HP 12794A Interface Schematic Logic Diagram (Cont.)

Appendix A
Compatible Modems and Recommended Options

BELL TYPE 201C MODEM

The Bell type 201C Modem provides half- or full-duplex, synchronous communication via dial-up or leased lines at transfer rates up to 2400 bits per second. The options available and recommended for use with the HP 12793A BISYNC Modem Interface Kit are:

PUBLIC SWITCHED LINE RECOMMENDED OPTIONS

OPTION	DESCRIPTION	RECOMMENDATION
A1	Transmitter internally timed.	A1 (required)
A2	Transmitter externally timed.	
B3	Without 801 Automatic Calling Unit.	B3
B4	With 801 Automatic Calling Unit.	
C5	EIA interface.	C5 (required)
C6	Contact interface.	
D7	Without automatic answer.	
D8	With automatic answer.	D8
E9	Automatic answer permanently wired.	Either.*
E10	Automatic answer key-controlled.	

* If option D7 is selected, the E options have no meaning and should be ignored.

PRIVATE LEASED LINE RECOMMENDED OPTIONS

OPTION	DESCRIPTION	RECOMMENDATION
A1	EIA interface.	A1 (required)
A2	Contact interface.	
B3	Alternate voice.	Either
B4	Without alternate voice.	
C5	With new synch.	
C6	Without new synch.	C6
D7	2-wire circuit.	
D8	4-wire circuit.	D8 (required)
E9	4-wire private line continuous carrier: 7 millisecond delay 0 millisecond delay	E9
E10	4-wire private line switched wire	
	Transmitter internally timed.	Required
	Transmitter externally timed.	

BELL 208A MODEM

The Bell type 208A Modem provides full-duplex, synchronous communication via leased lines at transfer rates to 4800 bits per second. The options available and recommended for use with the HP 12793A BISYNC Modem Interface Kit are:

PRIVATE LEASED LINE RECOMMENDED OPTIONS

OPTION	DESCRIPTION	RECOMMENDATION
A1	Transmitter internally timed.	A1
A2	Transmitter externally timed.	
B3	Continuous carrier.	B3
B4	Switched carrier.	
C5	Switched REQUEST TO SEND.	C5
C6	Continous REQUEST TO SEND.	
D7	One second holdover used.	D7
D8	One second holdover not used.	
E9	With new synch.	
E10	Without new synch.	E10
F11	CC ON when analog loop is present.	F11
F12	CC OFF when analog is present.	

BELL 208B MODEM

The Bell type 208B Modem provides half-duplex, synchronous communication via dial-up lines at transfer rates to 4800 bits per second.

PUBLIC SWITCHED LINE RECOMMENDED OPTIONS

OPTION	DESCRIPTION	RECOMMENDATION
A1	Transmitter internally timed.	A1 (required)
A2	Transmitter externally timed.	
B3	Without 801 Automatic Calling Unit.	B3
B4	With 801 Automatic Calling Unit.	
C5	CC OFF when analog is present.	
C6	CC ON when analog loop is present.	C6
D7	Without automatic answer.	
D8	With automatic answer.	D8
E9	Desk mounting.	Either
E10	Rack or cabinet mounting.	

BELL 209A MODEM

The Bell type 209A Modem provides full-duplex, synchronous communication via leased lines at transfer rates to 9600 bits per second. Five jacks on the back of the 209A can be used for multiplexing the 9600 bits per second communication rate, permitting a choice of:

- One channel at 9600 bits per second, or
- One channel at 7200 bits per second and one at 2400, or
- Two channels at 4800 bits per second, or
- One channel at 4800 bits per second and two at 2400, or
- Four channels at 2400 bits per second.

The options available and recommended for use with the HP 12793A BISYNC Modem Interface Kit are:

PRIVATE LEASED LINE RECOMMENDED OPTIONS

OPTION	DESCRIPTION	RECOMMENDATION
A1	Transmitter timing is supplied by modem.	A1 (required)
A2	Transmitter timing is supplied by computer/terminal.	
B3	Data Set Ready interface lead ON for Analog Loop-back mode.	B3
B4	Data Set Ready interface lead OFF for Analog Loop-back mode.	
C5	Transmitter timing slaved by receiver.	
C6	Transmitter timing NOT slaved by receiver.	C6
D7	Elastic store option enabled (IN).	
D8	Elastic store option disabled (OUT).	D8
E9	Continuous carrier operation.	E9
E10	Switched carrier option.	
F11	Switched REQUEST TO SEND operation.	F11 *
F12	Continuous REQUEST TO SEND operation.	
	Grounding: Protective ground to signal ground.	AA to AB
	With alternate voice.	Either. **
	Without alternate voice.	

* If option E10 is selected, the F options have no meaning and should be ignored.

** The data set normally is supplied without a hand set.

HP 37210T MODEM

The Hewlett-Packard 37210T modem provides half- or full-duplex communication via dial-up or leased lines at transfer rates to 4800 bits per second. The options available (determined by assembly switches) and recommended for use with the HP 12793A BISYNC Modem Interface Kit are:

FUNCTION OF SWITCHES (O=OPEN, C=CLOSED)	4-WIRE (LEASED) LINE	2-WIRE (DIAL-UP) LINE
CONTROL ASSEMBLY		
Factory Set Switches. Must remain as set at factory.		
S10-1, S10-6, S10-7	O O O	O O O
S11-4, S11-5	O C	O C
S11-7, S11-8	C C	C C
S12-1 thru S12-4	O O O O	O O O O
Train Sequence.		
S10-2	C	C
Receiver Turn-on Delay.		
S10-3	N/A	C
External Rate Control Enable/Disable.		
S10-4	C	C
24 Pushbutton Enable/ Disable.		
S10-5	O	O* or C*
Auto Answer Telephone Select.		
S10-8, S10-9	N/A	O* or C*
Transmit Clock.		
S11-1, S11-9	O O	O O
Request-to-Send Delay.		
S11-2	O	O
2-wire/4-wire Mode.		
S11-3	O	C

FUNCTION OF SWITCHES (O=OPEN, C=CLOSED)	4-WIRE (LEASED) LINE	2-WIRE (DIAL-UP) LINE
Carrier Select.		
S11-6	C	N/A
DISPLAY/PROCESSOR ASSEMBLY		
Factory Set Switches. Must remain as set at factory.		
S1-1 thru S1-6	all OPEN	all OPEN
S1-7	C	C
S1-8, S1-9	O O	O O
ANALOG/MEMORY ASSEMBLY		
Amplitude and Delay Equalizers.		
S1-1, S1-2	O C	C O
S2-1 thru S2-4	C O O C	C O C O
Output Power Programming Resistor.		
S1-3	C	C**
Receiver Threshold Level.		
S1-4	O	O
Transmitter Output Power Level.		
S3-1 thru S3-4	C O C O	***
Secondary Channel Select.		
S4-1 thru S4-3	O C C	O C C
Phone Line Loop-back.		
S4-1	C	N/A
4-wire/2-wire Operation.		
wire link, P/R	R	P

FUNCTION OF SWITCHES (O=OPEN, C=CLOSED)	4-WIRE (LEASED) LINE	2-WIRE (DIAL-UP) LINE
SECONDARY CHANNEL		
All switches.	N/A	N/A
REMOTE COMMAND ASSEMBLY		
Receive Address. S1-1 thru S1-4	Master O O O O Slave any number	N/A
Receiver Input Attenuation. S2-1	O	N/A
Remote Command Transmitter Output Level. S2-2, S2-3, S2-4	C O O	N/A
Address Thumbwheel. Front Panel Control	O (Slave)	N/A

Notes:

* Refer to the HP 37210T Operating and Service Manual for the correct switch setting.

** OPEN - The modem has the auto-answer option (003).
CLOSED - The modem does not have auto-answer.

*** With auto-answer, always set to 0 dbm (C O C O).
Without auto-answer, refer to the HP 37210T Operating and Service Manual for the correct setting.

HP 37220T MODEM

The HP 37220T Modem provides full-duplex, synchronous communications via leased lines at transfer rates to 9600 bits per second. The options available (determined by strapping configurations) and recommended for use with the HP 12793A BISYNC Modem Interface Kit are:

SWITCH FUNCTION	SWITCH SETTINGS	(O=OPEN, C=CLOSED)
TRANSMITTER STRAPPING		
Factory Set Switches. Must remain as set at factory.	S1-1 S1-8, S1-9 S2-2, S2-3, S2-9	C O O O O O
Request-to-Send/ Clear-to-Send Delay.	S1-2, S1-3, S1-4	C O C
Data-Set-Ready Control.	S1-5, S1-6, S1-7	O C C
Auto-Retain Enable/ Disable.	S2-1	O
Transmit Clock.	S2-4, S2-5, S2-6	O C O
Remote Loop-back Selection.	S2-7, S2-8	O C
Transmit Power Level.	S3-1 thru S3-8	all OPEN
Telephone Line Loop-back Amplifier.	S3-9	O
RECEIVER STRAPPING		
Input Threshold Level.	S1-1, S1-2	C O
Factory Set Switches. Must remain as set at factory.	S1-3 thru S1-6 S1-7, S1-8, S1-9	O O O O C C O
EXTERNAL RATE SELECT VIA THE RS232C/V24 INTERFACE	Jumper Wire	Out (disabled)

HP 37230A MODEM

The HP 37230A Modem provides half- or full-duplex, synchronous communications via leased lines at transfer rates to 19200 bits per second. The options available and recommended for use with the HP 37230A are:

STRAP(S)	2-WIRE (HALF-DUPLEX)	4-WIRE (FULL-DUPLEX)
Data Rate (A)		
2400	a	a
4800	b	b
9600	c	c
19200	d	d
Test Links		
(H)	b	b
(C)	a	a
(N)	a	a
Clock		
(D)	b	b
(E)	b	b
(S)	b	b
Duplex		
(F)	b (half)	a (full)
Carrier Select		
(H)	b	a
Transmit Level		
(J)	a*	a*
For conformity to BSTR 41301 at:		
2400 baud	a	a
4800 baud	b	b
9600 baud	c	c
19200 baud	d	d
Receive Impedance		
(K)	c	a
Transmit Impedance, Non-transmitting		
(L)	a	a

STRAP(S)	2-WIRE (HALF-DUPLEX)	4-WIRE (FULL-DUPLEX)
Transmit Impedance, Transmitting (M)	a	a
Receive Level (P)	a*	a*
For conformity to BSTR 41301 at:		
2400 baud	a	a
4800 baud	b	b
9600 baud	c	c
19200 baud	d	d
Signal Ground (Q)	b	b

* The settings of straps (J) and (P) must match for the two modems on the link to communicate properly.

MANUAL UPDATE

MANUAL IDENTIFICATION

Title: HP12793A BISYNC Modem Interface Kit Installation and Service Manual

Part Number: 12793-90001

UPDATE IDENTIFICATION

Update Number: 1

This Update Goes With: First Edition (September 1980)

THE PURPOSE OF THIS MANUAL UPDATE

is to provide new information for your manual to bring it up to date. This is important because it ensures that your manual accurately documents the current version of the product.

THIS UPDATE CONSISTS OF

this cover sheet, a printing history page, all replacement pages, and write-in instructions (if any). Replacement pages are identified by the update number at the bottom of the page. A vertical line (change bar) in the outside margin indicates new or changed text material. The change bar is not used for typographical or editorial changes that do not affect the text.

TO UPDATE YOUR MANUAL

identify the latest update (if any) already contained in your manual by referring to the printing history page. Incorporate only the updates from this packet not already included in your manual. Following the instructions on the back of tnis page, replace existing pages with the update pages and insert new pages as indicated. If any page is changed in two or more updates, such as the printing history page which is furnished new for each update, only the latest page will be included in the update package. Destroy all replaced pages. If "write-in" instructions are included they are listed on the back of this page.

HEWLETT-PACKARD COMPANY
Roseville Division
8000 Foothills Boulevard
Roseville, California 95678

(12793-90001)

UPDATE NUMBER	DESCRIPTION
1	Replace the title page/ii with the page provided.

Page 1-2:

Under Equipment Supplied change the following:

the part numbers of the firmware ROMs in item 2 to 91750-80010 and 91750-80011.

in item 3, the RS-232-C Modem Cable to part number 5061-4914.

Page 1-2:

In the description of Option 002, change part number 5061-3436 to 5061-4923.

Page 1-3, Table 1-1:

Delete the reference to "modem eliminator".

Change the specification under SUPPORTED CONFIGURATION as follows:

HP 91750A software, date coded 2201 and later, with BISYNC firmware ROMS (91750-80010 and 91750-80011) will support an unlimited number of links to an HP 3000.

Page 2-2:

Change the ROM part numbers in the first sentence to 91750-80010 and 91750-80011.

Annotate figure 2-1 as follows: the leftmost ROM device should be labeled U203, 91750-80011; the adjacent ROM device is U93, 91750-80010. The jumper socket should be labeled XW1, with slot G at the top and slot A at the bottom.

Page 2-4:

Delete both references to a "modem eliminator".

Page 2-5, Table 2-3:

Substitute the following table for table 2-3 as it applies to BISYNC firmware date coded 2213 (HP part numbers 91750-80010 and 91750-80011).

SWITCH	FUNCTION
1	Not defined by BISYNC firmware.
2	Closed for external clock. Open for internal clock.
3	Closed for Ring Detect. Open for immediate TR (auto answer). For specific modem needs, refer to modem documentation.
4	Closed for Modem interface; 20 second connect timeout. Open for Direct connect interface (requires internal clock). No connect timeout.
5	Not used.
6,7,8	Select clock rate.

Page 2-5, Table 2-4:

Reverse the order of the switch segment numbers in th first column heading to read:

"8,7,6"

Page 2-6,

Change the paragraph enclosed in Figure 2-3 to read as follows:

> These switches are set to select external clock, ring detect, and a 57600 bps clock rate.

Page 2-7:

Change the part number of the Network Manager's Manual, in step 4, to 91750-90010 (Volume 1).

Change the part number of the Network Manager's Manual, in step 1, to 91750-90011 (volume 2).

Page 2-8:

In the paragraph following step 5, change the part number of the Network Manager's Manual to 91750-90011 (Volume 2).

Page 3-3:

In the second paragraph, change "Figure 3-3" to "Figure 3-6."

Page 3-7:

Add a note to indicate that the octal ASCII codes in table 3-2 include odd parity.

Page 5-3:

In the first paragraph, correct the part number of the Network Manager's manual to 91750-90010 (volume 1).

In step 3, delete the phrase "but will not indicate that the hood was sensed." And in the last sentence, insert the word "Diagnostic" in front of the word "hood".

Page 5-4:

In the last paragraph, correct the part number of the Network Manager's Manual to 91750-90011 (Volume 2).

Page 6-3, Table 6-1:

Change:

REF DES	HP PART NUMBER	C D	MANUF. CODE	MANUF. PART NO.
U27	1820-2096	9	01295	SN74LS393N
U72	1818-1396	4	50088	MK4116N-3
U82	1818-1396	4	50088	MK4116N-3
U92	1818-1396	4	50088	MK4116N-3
U102	1818-1396	4	50088	MK4116N-3
U202	1818-1396	4	50088	MK4116N-3
U302	1818-1396	4	50088	MK4116N-3
U402	1818-1396	4	50088	MK4116N-3
U502	1818-1396	4	50088	MK4116N-3

Add:

XW1	1200-0483	0		

Page 7-4:

Replace Table 7-2 with the table provided in replacement pages 7-3 through 7-6.

HEWLETT-PACKARD COMPANY
Data Systems Division
11000 Wolfe Road
Cupertino, California 95014

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