HP 12044A
HDLC Direct Connect Interface
installation and service manual

Card Assembly: 5061-3434
Date Code: 2022

HEWLETT PACKARD

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PRINTING HISTORY

New editions are complete revisions of the manual. Update packages contain replacement pages or write-in instructions to be merged into the manual by the customer. Manuals will be reprinted as necessary to incorporate all prior updates. A reprinted manual is identical in content (but not in appearance) to the previous edition with all updates incorporated. No information is incorporated into a reprinting unless it appears as a prior update. The edition does not change.

First Edition . . . . . Sept 1980

SAFETY CONSIDERATIONS

GENERAL - This product and relation documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

Some of the semiconductor devices used in this equipment are susceptible to damage by static discharge. Depending on the magnitude of the charge, device substrates can be punctured or destroyed by contact or mere proximity to a static charge. These charges are generated in numerous ways such as simple contact, separation of materials, and normal motions of persons working with static sensitive devices.

When handling or servicing equipment containing static sensitive devices, adequate precautions must be taken to prevent device damage or destruction. Only those who are thoroughly familiar with industry accepted techniques for handling static sensitive devices should attempt to service the cards with these devices. In all instances, measures must be taken to prevent static charge buildup on work surfaces and persons handling the devices. Cautions are included through this manual where handling and maintenance involve static sensitive devices.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

WARNING

EYE HAZARD

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

Definition of Terms

The following terms are defined as they are used in this manual.

asynchronous transmission - No timing signals are sent with the data. Start and stop bits serve to define transmitted words.

buffer - A segment of contiguous random-access memory locations used for temporary storage of input/output messages.

card - The interface PCA (Printed Circuit Assembly).

CRC-16 (Cyclic Redundancy Check) - An error detection scheme used in data communications.

DIP (Dual In-line Package) - A type of integrated circuit package.

driver - In a hardware sense, a driver refers to a circuit which is capable of supplying specific current and voltage requirements. In a software sense, a driver is a program that is capable of controlling a specific input/output device.

DS (Distributed System) - A term used to refer to networks using Hewlett-Packard Distributed Systems hardware and software products.

firmware - Software code packaged in read-only memory (ROM).

frame - A transmitted message that is formatted according to HDLC protocol.

full-duplex - Communications systems or equipment capable of simultaneous two-way data communication.

half-duplex - Communications system or equipment capable of transmission in either direction, but not both directions simultaneously.

handshaking - The alternating exchange of predetermined signals between two communicating devices for purposes of control.

host - The computer housing the communication card.

interface - A device providing electrical and mechanical compatibility between two communicating devices. The HP 12044A also provides other control features for the associated communication link.

LED (Light Emitting Diode) - A component used on many printed circuit assemblies to provide a visible indication of desired information.

link - Communication lines, modems, and other equipment which permit the transmission of information in data format between two or more devices.

PCA (Printed Circuit Assembly) - Interface cards are commonly referred to as PCAs.

primary - The portion of the interface responsible for transmission processes.

Primary System - A preconfigured operating system included with all HP 1000 Computer systems. It can be reconfigured to meet specific system I/O and memory requirements.

receiver - Any device capable of reception of electrically tansmitted signals.

secondary - The portion of the interface responsible for reception processes.

synchronous transmission - Timing signals are transmitted with the data. No start and stop bits are used. Defined protocol characters must be used to define message blocks or frames.

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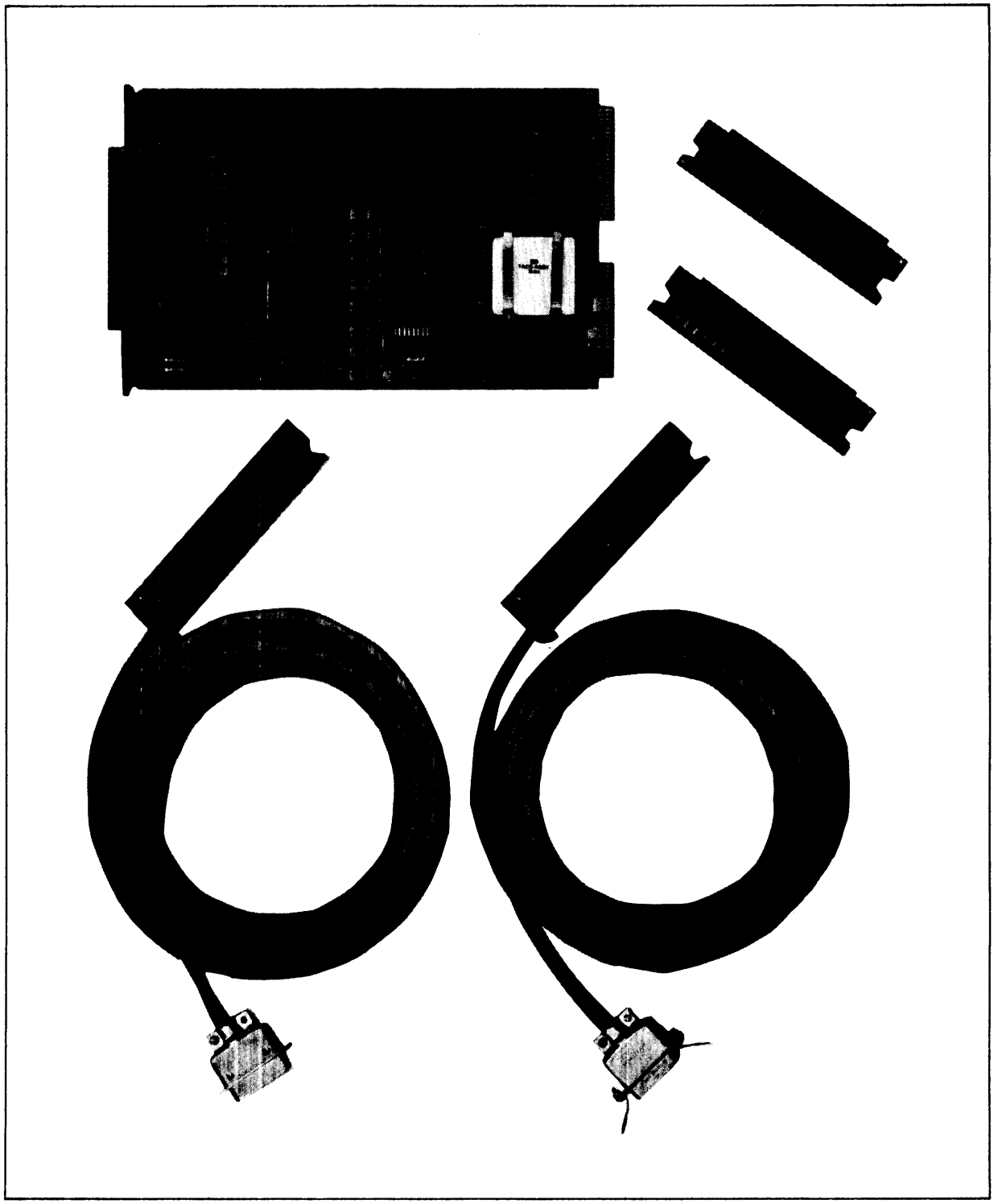


Fig. 1-1. HP 12044A HDLC Direct Connect Interface Contents

Section 1
General Information

Introduction

This manual provides general information, installation procedures, HDLC protocol information, principle of operation, maintenance instructions, replaceable parts information, and servicing diagrams for the HP 12044A HDLC Direct Connect Interface Kit. This section contains general information concerning the HP 12044A including a description and specifications.

Description

The HP 12044A (see Figure 1-1) provides an HP 1000 L-Series computer with the capability to support a direct connect (hardwired) communications link to another HP 1000 L-Series computer, or to an HP 1000 M/E/F-Series computer. It is used in conjunction with DVR66 of the HP 91750A DS/1000-IV Software.

The HP 12044A card plugs into a single I/O slot of an HP 1000 L-Series Computer and is assigned a single select code. The card contains a Z-80A CPU chip with associated Z-80A support chips and two ROMs containing firmware to implement HDLC protocol. Due to this on-board intelligence, the card is able to relieve a large amount of CPU overhead. Functions such as HDLC protocol generation, CRC-16 block check error control, and a hardware self-test are all handled on the interface card. The Z-80A and on-board RAM also enable the card to maintain long term communications line statistics, and input and output data buffering.

The HP 12044A can be configured to serve as the interface to the Vitual Control Panel (VCP) for an HP 1000 L-Series Computer. This capability allows remote VCP functions to be performed and is made possible via two remote VCP programs available with DS/1000-IV.

Equipment Supplied

The standard HP 12044A HDLC Direct Connect Interface Kit consists of the following items (see Figure 1-1):

1. Programmable serial interface card, HP part number 5061-3434.

2. HDLC firmware ROMs, HP part numbers 91750-80008 and 91750-80009.

3. Direct connect interface cable (5 meter, 16.4 feet) with assembled male connector, HP part number 5061-3422.

4. Direct connect interface cable (5 meter, 16.4 feet) with assembled female connector, HP part number 5061-3423.

5. Two loop-back verifier hood, HP part number 5061-3421.

6. Installation and Service Manual, HP part number 12044-90001.

The following options are available with the HP 12044A:

1. Option 001: Upgrade discount for latest revision of interface firmware (for previously purchased firmware only).

2. Option 002: Delete the cables, HP part numbers 5061-3422 and 5061-3423, and the two loop-back verifier hood, HP part number 5061-3421.

3. Option 003: Add an interconnection cable (75 meters, 246 feet) with assembled connectors (for extending the direct connect link an additional 75 meters), HP part number 5061-3437.

4. Option 004: Add a direct connect connector kit, HP part number 5061-3438, which includes one male and one female connector with hoods and clamps and a wiring diagram.

5. Option 005: Add a direct connect custom cable kit which contains one male and one female connector with hoods and clamps, a cable (304 meters,1000 feet), and a wiring diagram, HP part number 5061-3450.

Identification

The Product

Five digits and a letter (12044A in this case) are used to identify Hewlett-Packard products used with HP computers. The five digits identify the product and the letter indicates the revision level of the product.

The Circuit Card

The circuit card supplied with the kit is identified by a part number marked on the card. In addition to the part number, the card is further identified by a letter and a date code consisting of four digits (e.g., A-2013). This designation is placed below the part number. The letter identifies the version of the etched circuit on the card. The date code (the four digits following the letter) identifies the electrical characteristics of the card with components mounted. Thus, the complete part number on the interface card could be:

5061-3434
A-2013

If the date code stamped on the HDLC interface card does not agree with the date code on the title page of this manual, there are differences between your card and the card described herein. These differences are described in manual supplements available at the nearest Hewlett-Packard Sales and Service Office (a list of Hewlett-Packard Sales and Service Offices is supplied at the back of this manual).

Installation and Service Manual

The manual supplied with the kit is identified by its name and part number. Part number, 12044-90001, and publication date are printed on the title page. If the manual is revised, the publication date is changed and the List of Effective Pages (page iii) reflects the pages involved in the change. The Print History page (page ii) records the reprint dates.

Specifications

Table 1-1 lists the specifications of the HP 12044A HDLC Direct Connect Interface Kit.

Table 1-1. Specifications

TRANSMISSION MODE:	Bit serial; synchronous.
TRANSMISSION LINK:	Full-duplex over four individually-shielded twisted pairs. Lines are optically isolated at the receivers on the card.
ISOLATION PROVIDED:	1 kilovolt common mode.
MAXIMUM CABLE LENGTH:	230000 bps: 1 kilometer 57600 bps: 2.2 kilometer
INTERFACE:	EIA Standard RS-422 balanced drivers and receivers.
DATA TRANSFER LENGTH:	Selectable frame size (128 or 1024 byte information field length).
DATA TRANSFER RATE:	Approx. 300, 1200, 2400, 4800, 9600, 19200, 57600, or 230000 bps.
ERROR DETECTION:	CRC-16 check performed on I/F.
ERROR CORRECTION:	Retransmission under firmware control.

POWER REQUIREMENTS:

VOLTAGE	CURRENT	POWER DISSIPATION
+ 5 V	2.433 A	12.16 W
+12 V	0.308 A	3.69 W
-12 V	0.035 A	0.42 W
	Total:	16.27 W

PHYSICAL CHARACTERISTICS:	
Size:	17.15 by 28.91 centimeters (6.75 by 11.38 inches)
Backplane Interconnects:	Two 50-finger edge connectors plug into two sockets (P1 and P2) mounted on the backplane.
Device Interconnects:	One 80-finger edge connector (J1) on which a cable hood may be connected.

Section 2
Installation

Introduction

This section provides information on unpacking, inspecting, installing, and checking the operation of the HP 12044A HDLC Direct Connect Interface.

Unpacking and Inspection

Inspect the shipping package immediately upon receipt to detect any evidence of mishandling during transit. If the package is damaged, ask that the carrier's agent be present when the kit is unpacked. Carefully unpack the card and accessories and inspect for damage (scratches, broken components, etc.). If damage is noticed, notify the carrier and the nearest Hewlett-Packard Sales and Service Office listed at the back of this manual. Return the carton and packing material for the carrier's inspection.

After inspecting all components, refer to Equipment Supplied information given in Section 1 to ensure that the kit is complete. Also check the part numbers listed in that paragraph against the part numbers on the kit components. If the kit is incomplete, or if an incorrect component has been furnished, notify the nearest Hewlett-Packard Sales and Service Office.

After unpacking, inspecting, and checking part numbers of all parts of the product, follow installation and checkout procedures as defined in this section.

Computation of Current Requirements

The circuit card included in the HP 12044A obtains its operating voltages from the computer power supply through the backplane. Before installing the card, it is necessary to determine whether the added current will overload the power supply. The current requirements of the HDLC interface card are listed in the power specifications entry of Table 1-1. Current specifications for all other interfaces can be found in the appropriate Reference Manuals.

Firmware Installation

CAUTION

STATIC SENSITIVE DEVICES

THE ROMS, RAMS, AND Z-80A COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE REPLACING.

The firmware ROMs (HP part numbers 91750-80008 and 91750-80009) are factory installed in sockets on the card. Make sure that the ROMs are installed as shown in Figure 2-1, and that the part numbers on them match those given in this paragraph.

ROM Configuration Jumpers

A set of jumpers on the interface card provides the option of using different ROM parts in the future. The set consists of a 14-pin socket housing seven removable jumpers (XW1A through XW1G), and an 8-pin socket housing 4 removable jumpers (XW2A through XW2D). Check to see that all of these jumpers are configured as described in Tables 2-1 and 2-2 for the specific ROMs that are installed. Refer to Figure 2-2 for the location of the socketed jumpers on the interface card.

Table 2-1. ROM Categories According to Part Type

CATEGORY	HP PART #	PART TYPE
A	1818-0762	TI 2532
B	1818-0498	TI 2516 Intel 2716
C	1818-0850	Intel 2732 Intel 2332 Intel 2364

Check these

Table 2-2. Jumper Requirements for all ROM Combinations
(X denotes a required jumper; DC denotes a "don't care")

ROM CATEGORY 73?		X W 1 A	X W 1 B	X W 1 C	X W 1 D	X W 1 E	X W 1 F	X W 1 G	X W 2 A D	X W 2 B C	X W 2 C B	X W 2 D A
U93	U203											
C	C					X			X		DC	DC
A	A				X	X	X	X	X		DC	DC
C	A			X		X	X		X		DC	DC
* B	A			X		X	X	X	X		DC	DC
B	B			X	X	X	X	X	X		DC	DC
A	C	X				X		X	X		DC	DC
C	B	X			X	X	X		X		DC	DC
A	B	X		X	X	X	X	X	X		DC	DC
B	C	X		X		X		X	X		DC	DC

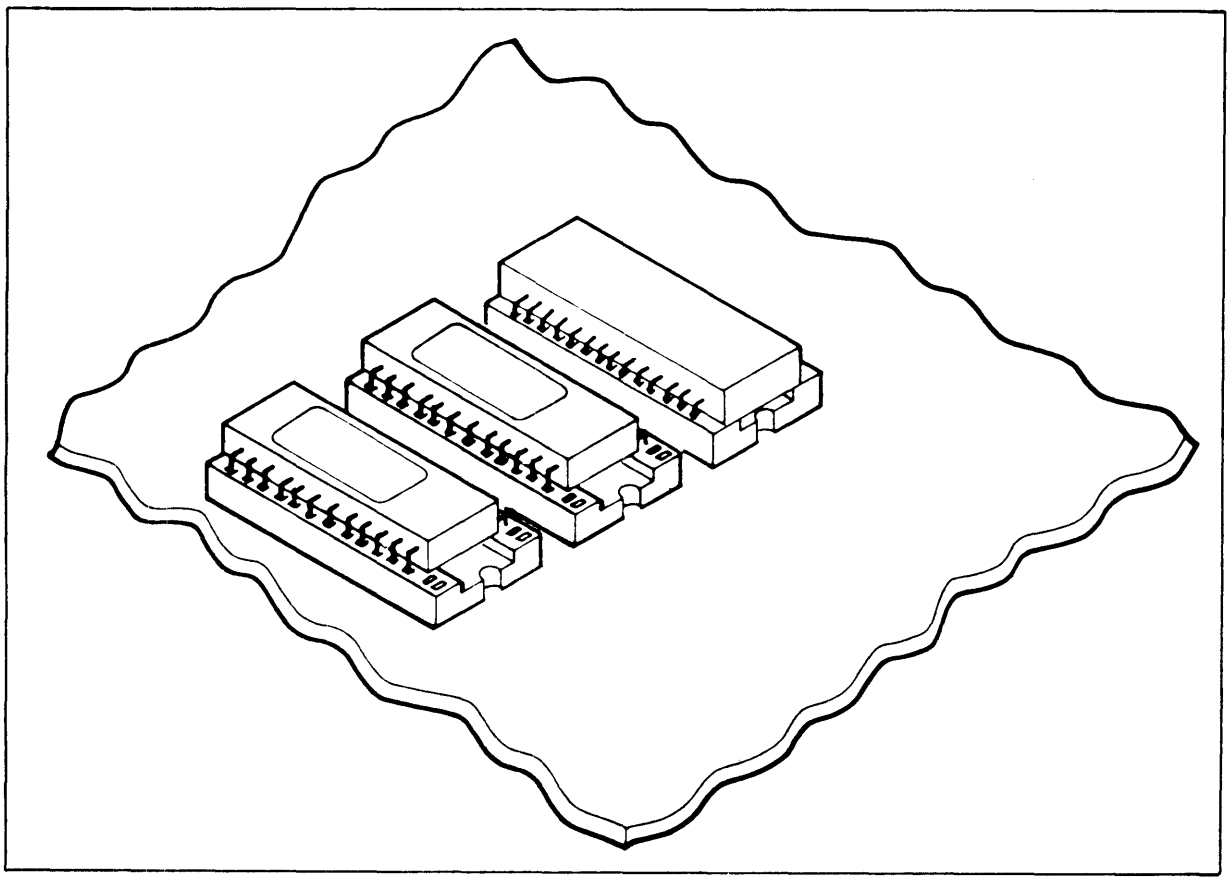


Fig. 2-1. ROM Installation

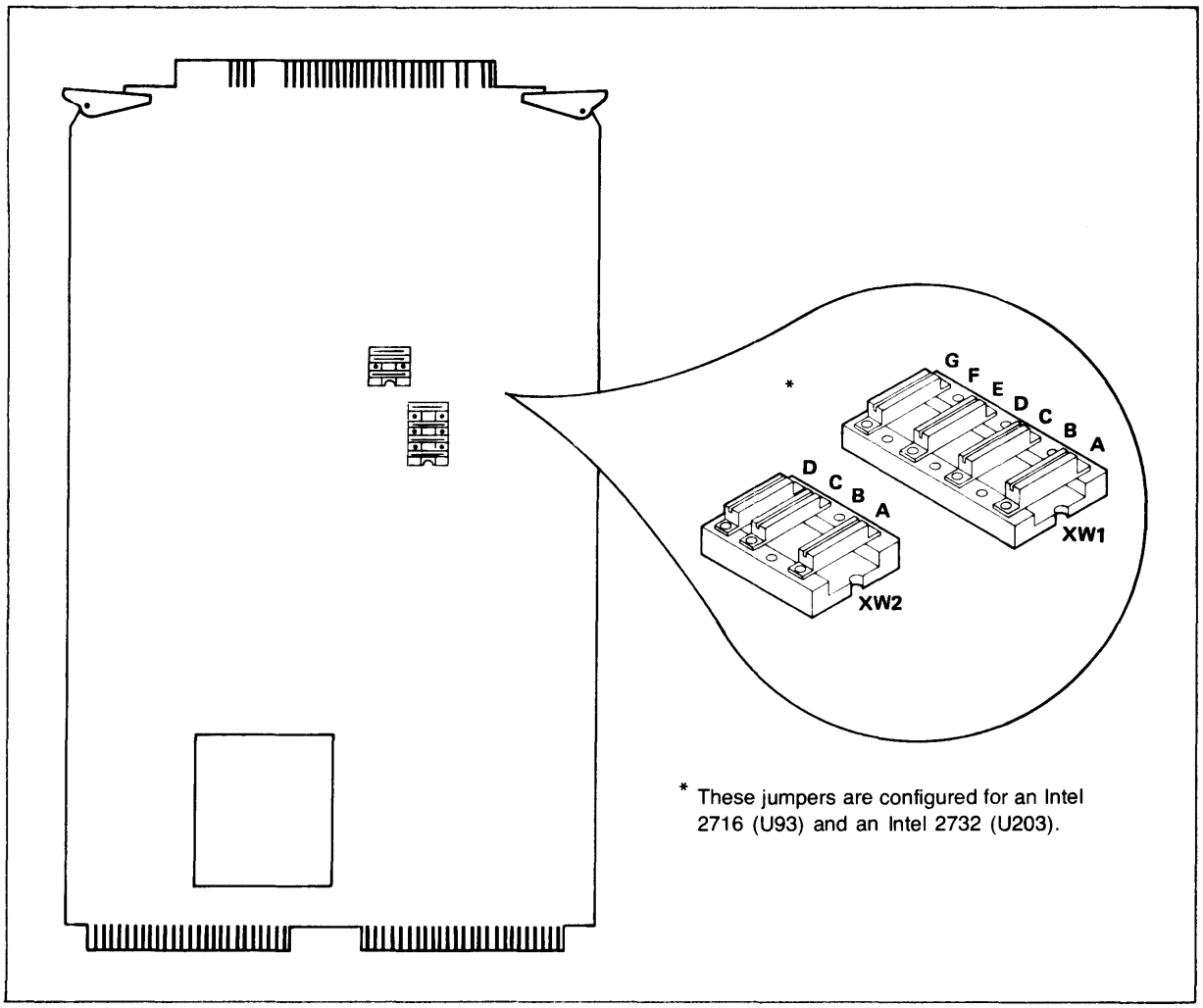


Fig. 2-2. ROM Configuration Jumper Positions

DIP Switch U15 Configuration

The card provides a Dual In-line Package (DIP), U15, containing eight switches which may be sensed by the firmware. This set of switches is used to determine the information field size, and the transmitting clock rate and associated time-out values (time-outs are firmware controlled and not user programmable). The card sends a clock with transmitted data and receives a clock with received data. Therefore, the two communicating cards can have different transmission rates as selected by this switch. The switch assignments for U15 are given in Tables 2-3 and 2-4. Refer to Figure 2-3 for switch position on the card.

Table 2-3. U15 Switch Assignments

SWITCH	FUNCTION
1	Not used.
2	Closed to select 1024 byte information field. Open to select *128 byte information field. BOTH SIDES OF THE LINK MUST HAVE THIS SWITCH SET THE SAME TO AVOID DATA OVERRUN.
3,4,5	Not used.
6,7,8	Select transmission clock rate. See Table 2-4.
* 128 byte information field is recommended to minimize frame retransmissions.	

Table 2-4. Transmission Clock Rate Selection

SWITCH SETTINGS 6,7,8	CLOCK RATE (bps)	
000	300	NOTE:
00X	1200	X = closed = logic "1"
0X0	2400	0 = open = logic "0"
0XX	4800	
X00	9600	
X0X	19200	
XX0	57600	
XXX	230000	

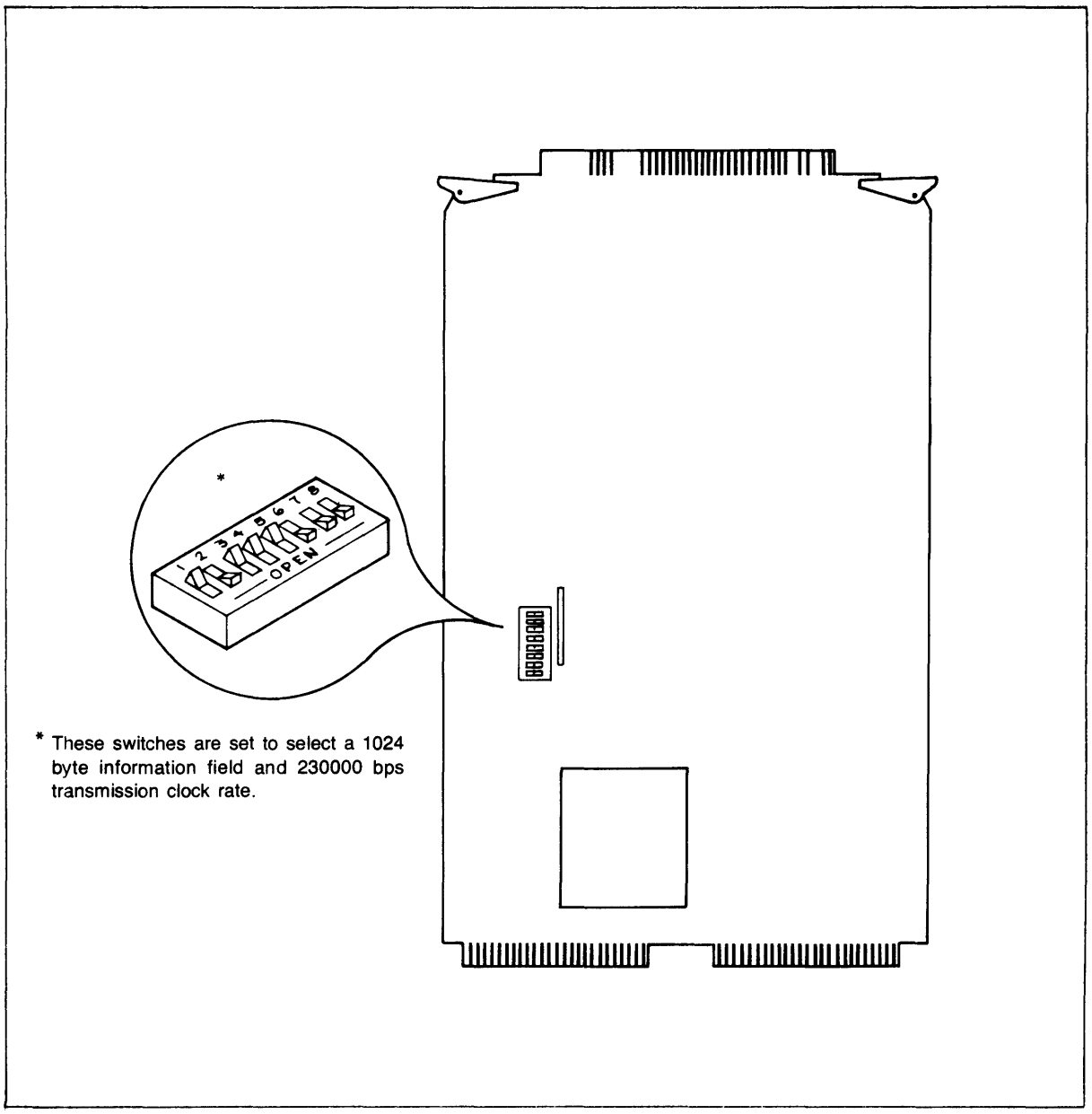


Figure 2-3. DIP Switch Position and Configuration

DIP Switch U1 Configuration

The card provides another pack of eight switches, U1, which is used to specify interface configuration information such as VCP interface selection and interface card select code. The switch is also used to specify grounding conditions. Under normal operation, the interface card circuitry obtains its ground reference via a ground clip on the cable which makes contact with the card cage door when it is shut. If the door is open, the card will not receive ground reference correctly. To operate with the door open, switch 2 being closed will provide the necessary ground connection. Switch 2 MUST BE OPEN if the door is closed to eliminate the possibility of conflicting ground references. Configure switch U1 as desired according to the switch assignments given in Table 2-5. Check to ensure that only one interface in the computer is configured as the VCP interface and also that the select code assigned to the HP 12044A card is unique.

Table 2-5. DIP Switch U1 Configuration

SWITCH	FUNCTION
1	Closed to enable VCP. Open to disable VCP.
2	MUST BE OPEN if card cage door is closed. MUST BE CLOSED if card cage door is open.
3 - 8	Card select code (octal).

Card and Cable Installation

CAUTION

ALWAYS TURN POWER OFF TO THE COMPUTER AND OTHER ASSOCIATED EQUIPMENT WHEN INSERTING OR REMOVING INTERFACE CARDS OR CABLES. FAILURE TO FOLLOW THESE DIRECTIONS COULD RESULT IN DAMAGE TO THE EQUIPMENT.

After ensuring that the computer power supply can handle the added load, the ROMs are properly installed, and the DIP switches are configured properly, perform the following steps:

1. Install all cables to be used to connect the two interface cards being installed. Wiring diagrams for the cables and for building extension cables are supplied in Section 7 of this manual.

2. Turn off power at the computer. Install the HDLC interface card in the desired slot in the computer card cage, noting the select code. The card should be oriented the same as all other cards in the computer: components on the top side of the card. Press the card firmly into place.

3. Connect all cables to be used with the interfaces. Power should be turned off at the remote computer also before installing cables on the remote interface.

4. Restore power to the computer.

5. Initialize the new link into the network as specified in the HP 91750A DS/1000-IV Network Manager's Manual, HP part number 91750-90003.

6. Perform the checkout procedure on the card as specified in the next paragraph.

Checkout Procedure

For checkout after installation, perform the interface card and communication link checks described below.

Interface Card Configuration Check

Since the interface card self-test is run each time that power is applied to the card or the card is reset, the first part of checkout is automatically performed. The following procedure will verify that the card passed the self-test and that the backplane interface circuitry is operational. It also provides a way to check the card configuration switch settings. To perform the check, enter the following commands:

1. RU,DSINF<cr>

   DSINF is a DS/1000-IV utility program that can be used to obtain information such as network configuration, communications parameters, card configuration, etc. For more information on DSINF, refer to the DS/1000-IV Network Manager's Manual, HP part number 91750-90003.

2. LU,##,AL<cr>

   LU will return information on the configuration of a specified DS/1000-IV interface card, where ## is the LU (Logical Unit number) of that card. Information will only be returned if the card passed the self-test.

In this way, DSINF will return card configuration information as well as other useful parameters. Compare the returned configuration with the desired configuration. If the values are unexpected, check the switch settings on the card. If in error, reconfigure the switches and reinstall the card, going through all checkout procedures again.

Communication Link Check

A good check of the communication link is accomplished by exercising a few REMAT commands. To do this, type in the following commands after the system prompt (:):

1. :RU,REMAT<cr>

   REMAT is the program that handles operator commands for communications from one HP 1000 to another in a Distributed Systems network. It schedules the appropriate monitors to handle all outgoing and incoming requests. REMAT will prompt with a dollar sign ($) when commands are referred to the local node only. When a remote node is referenced (another HP 1000), the prompt will become a number sign (#).

2. $SW,NODE1,NODE2,SC<cr>

   The SW (Switch) instruction defines the action and destination nodes. Set NODE1 to the node number of the neighbor node where the message will be sent. Set NODE2 to the local node's number. SC is the security code for the network. It is defined when the network is initialized.

3. #TI<cr> OR #TM<cr>

   The TI and TM (Time) commands will obtain the time from the remote node and display it on the local terminal being used for this exercise. The TI command should be used if the remote node is an HP 1000 M/E/F-Series computer. The TM command should be used if the remote node is an HP 1000 L-Series computer. If the remote node does not have the necessary monitor to handle the TI or TM command, or does not have a real-time clock, try a DL (Directory List) command or a CL (Cartridge List) command.

4. #EX<cr>

   The EX (EXit) command will end REMAT.

If the above message is sent successfully, the described results will be displayed with no error messages returned. If an error message is returned, refer to error code information supplied in the DS/1000-IV User's Manual, HP part number 91750-90002. For troubleshooting procedures, refer to Section 5 of this manual or the troubleshooting section of the DS/1000-IV Network Manager's Manual, HP part number 91750-90003.

Interface Card LEDs

There are four Light Emitting Diodes (LEDs) installed on the interface card. The LEDs are visible when the card is installed in the computer and are referenced as 0 through 3 with 0 being the LED on the right. During normal operation LED0 being lit indicates that the interface is logically connected to the other interface card on the link. LED1 being lit indicates that a transfer of data is taking place over the backplane. The LEDs are also used to indicate successful completion of the self-test with all four being off after the test and before DS software has been initialized.

Section 3
Protocol

Introduction

There are many levels of protocol involved in an HP DS/1000-IV communications link. Two of these levels are handled on the 12044A: line protocol and communications protocol. The first level involves timing and control signals, and electrical specifications for computer-to-computer connections. The second level involves the more complex set of rules used to control the flow of data over the communication link. Both line and communications protocols are firmware controlled on the HP 12044A. This section will present an abbreviated discussion of the communications protocol. For information on the line protocol, refer to the Communication Line Interface paragraphs in Section 4 of this manual. For a more thorough understanding of HDLC, refer to the HP Computer Systems Group Data Communications Standard, October 1977.

Communications Protocol

The HP 12044A is programmed via the read-only memory (ROM) on the card to implement High Level Data Link Control (HDLC) protocol. HDLC is an asynchronous, bit oriented protocol designed for use over full-duplex communications channels. The following paragraphs discuss the main characteristics of HDLC.

HDLC Frames

Data transfers using HDLC protocol are bit oriented as opposed to character oriented. Blocks of data are transmitted in frames, a frame being a bit stream starting and ending with a flag. For this implementation, the flag is the following bit pattern:

01111110

A frame may or may not contain data but always contains control information. There can be any number of frames in a single transmission.

A frame consists of several fields as illustrated in Figure 3-1 and described in the following paragraphs.

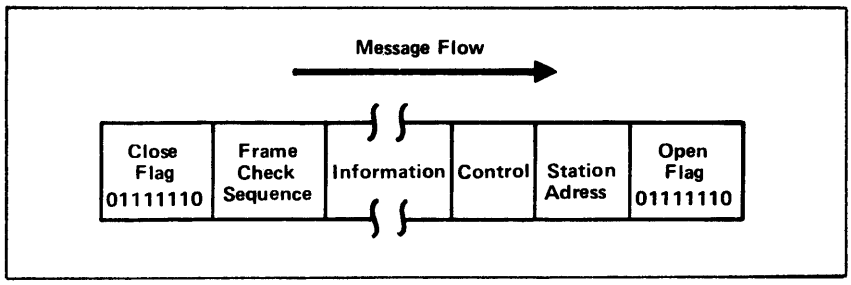


Figure 3-1. HDLC Frame Format

Flag Field

HDLC uses positional significance, not control characters, to identify the various elements of a message. The flag field is the first eight bits of a frame and the receiver uses it to count down the incoming bit stream to identify the other fields within the frame. The close flag is used to indicate the end of the frame. The firmware also uses the close flag to count back to the frame check sequence field.

Zeroes are inserted and deleted as required to prevent a flag bit pattern from appearing within the frame. When five 1's appear, a 0 is inserted in the bit stream after the last 1. The receiver detects the five 1's followed by a 0 and deletes the 0. The inserted and deleted zeroes are not included in the frame check sequence. This zero insertion/deletion scheme is controlled by the Z-80A SIO chip on the HP 12044A Interface card.

Each interface on the link is continuously seaching for the flag pattern. During lulls in message flow, a series of flags is transmitted to keep the link active and synchronized.

Station Address Field

Since all links in a DS network are point-to-point, station address information is not needed as such. Instead, this field is used to convey whether the frame contains a response or a command. This information is necessary due to the data handling organization at each station on the link. Outgoing commands and incoming responses are handled by the primary portion of the firmware driver. Incoming commands and outgoing responses are handled by the secondary portion of the driver. This primary/secondary scheme is one way of implementing a full-duplex communications protocol.

Control Field

The control field consists of eight bits containing a command or response pattern required for control of the data link. The primary station uses the field to command the secondary to perform an operation. The secondary uses it to respond to the primary. The control field has three formats, indicating the contents and purpose of the frame as follows (refer to Table 3-1 also):

1. Information Transfer. This control field format indicates that the present frame contains information being transfered from the local primary to the remote secondary.

2. Supervisory Response. A frame with a supervisory format in the control field contains no information (the information field is interpretted to be of zero length), and is used to regulate traffic and request retransmission of missed or erroneous frames.

3. Unnumbered Command/Response. This format consists of commands and responses used to establish or disconnect the communications channel, reject commands (those not recoverable by retransmission), or request a remote node to go into front panel mode.

Information Field

A non-zero length information field only exists in frames designated as information transfer frames by the control field. When used, the information field is the vehicle for moving data between stations and it is unrestricted in format and contents. Information field length is selected to be 128 or 1024 bytes using one of the configuration switches on the interface card.

Frame Check Sequence Field

This field is 16 bits in length and preceeds the closing flag. When information is present in the frame, it follows the information field, otherwise it follows the control field. Its purpose is to detect errors that occur during transmission. For the HP 12044A, the frame check sequence is computed under firmware control using the CRC-16, cyclic redundancy check, block check method. This consists of dividing a constant into the first group of bits being transmitted after the opening flag. The quotient is discarded and the remainder added to the next group of bits, which is again divided by the same constant. This continues until the closing flag is detected and the 16-bit CRC-16 remainder is sent in the frame check sequence field before the closing flag.

Table 3-1. HDLC Protocol Bytes (Control Field)

TYPE	MNEMONIC	DESCRIPTION	ENCODING							
			7	6	5	4	3	2	1	0
INFO.	I	Information	Nr			P	Ns			0
SUPRV.	RR	Receiver Ready	Nr			F	0	0	0	1
	RNR	Receiver Not Ready	Nr			F	0	1	0	1
	REJ	Reject	Nr			F	1	0	0	1
UNNUM.	SARM	Set Asynchronous	0	0	0	0	1	1	1	1
	DISC	Disconnect	0	1	0	0	0	0	1	1
	UA	Unnumbered Acknowl.	0	1	1	0	0	0	1	1
	CMDR	Command Reject	1	0	0	0	0	1	1	1
	SIM	Set Initial. Mode	0	0	0	0	0	1	1	1

Abbreviations:

P - Poll Bit
F - Final Bit
Nr - Receive Sequence Number
Ns - Send Sequence Number

Error Control

As described in a previous paragraph, CRC-16 is used by the HP 12044A to detect errors in transmitted frames. There are other types of error control methods used on an HDLC link as described in the following paragraphs.

Frame Sequencing Checks

Sequencing counts are kept on each interface card and transmitted as necessary to be used to acknowledge frames received correctly. The values of these counts are sent in the control field as the following variables:

Ns - Send Sequence Number.
Ns is only transmitted in information frame control words and is used to tell the receiver the number of the frame being sent.

Nr - Receive Sequence Number.
Nr is transmitted in the control field for supervisory and information frames only and is used to convey the number of frames received successfully. The value of Nr sent is equal to the number of the next frame that is expected.

The counts kept for Nr and Ns are only incremented when frames containing information are sent or received. Supervisory and unnumbered command/response frames do not affect these counts. These frames are acknowledged by proper response words. By keeping track of frames sent and received in this manner, it is possible for transmitting stations to transmit frames before the response is returned for previously transmitted frames. Also, one response can serve to acknowledge more than one received frame. This increases overall link throughput. The number of unacknowledged frames allowed in this implementation of HDLC is seven. After that, outgoing messages are put in a queue and sent only when the proper responses are received.

If a sequence error is detected by a transmitting station, it will retransmit the frame after the last acknowledged frame and set the P (Poll) bit to signal that it is a retransmission. The P bit set also demands that the receiving station respond with a supervisory frame instead of the standard information frame acknowledgement. In the response supervisory frame, the F (Final) bit is set to indicate that it is responding to a received poll.

Severe Error Processing

The HDLC interface card is capable of detecting other types of errors besides invalid frames (CRC-16 detected errors) and sequence errors. The other detectable errors are referred to as severe errors and include such cases as:

* Unknown frame type
* Information field larger than available frame buffer
* Ns greater than seven
* Failure to acknowledge after maximum allowable retries

These errors are reported to the software driver by the firmware on the card, and then an attempt is made to recover. For failure to acknowledge, the link is reset. This is similar to the original connect sequence (see Section 4, Principles of Operation, of this manual). For the other severe errors, a command reject frame is sent.

Section 4
Principles of Operation

Introduction

This section contains a description of the operation of the interface card included in the HP 12044A HDLC Interface. The hardware is described in terms of five major functional areas. A brief explanation of the command and status words used in communicatoin between the card and the host computer is also given. The last part of this section is devoted to a functional-level description of the operation of the card.

Hardware Functional Description

The card, HP part number 5061-3434, includes the following major functional areas:

* HP 1000 L-Series Computer I/O Master interface
* Z-80A Microprocessor family subsystem (CPU, SIO, DMA and CTC)
* Read-Only Memory (ROM)
* Random-Access Memory (RAM)
* Communication line interface

A block diagram illustrating the major functional areas of the card is presented in Figure 4-1.

I/O Master-Communications Card Interface

The card communicates with the HP 1000 host computer through the I/O Master circuitry physically implemented on the card. The I/O Master is the I/O Processor and related circuitry that appears on all HP 1000 L-Series interface cards. The circuitry that interfaces this card to the I/O Master can be divided into two major sections: the I/O data latches and the control circuitry section.

The I/O data latches consist of two 8-bit input latches and two 8-bit output latches. The input latches hold 16-bit data words or commands from the host computer until the card is ready to accept them. Likewise, the output latches hold 16-bit status words or data output to the computer.

The control circuitry is made up of two flip-flops, a bus control state latch and various other gate-level logic elements. The primary function of this section is to handle the control signals to and from the I/O Master. These signals are used to generate and acknowledge interrupts, to handshake data between the host and the card and to conform to the standard HP 1000 L-Series Computer I/O Master signal conventions. For a more detailed discussion of these and other I/O signals, refer to the HP 1000 L-Series I/O Interfacing Guide, HP part number 02103-90005.

The Z-80A Microprocessor Subsystem

The heart of the card is the Z-80A CPU (Central Processing Unit). This MOS LSI microprocessor operates from a single 5V supply, uses a single phase clock and has a typical instruction execution time of 1 microsecond. The data bus is eight bits wide and the address bus is sixteen bits wide. All CPU pins are TTL compatible.

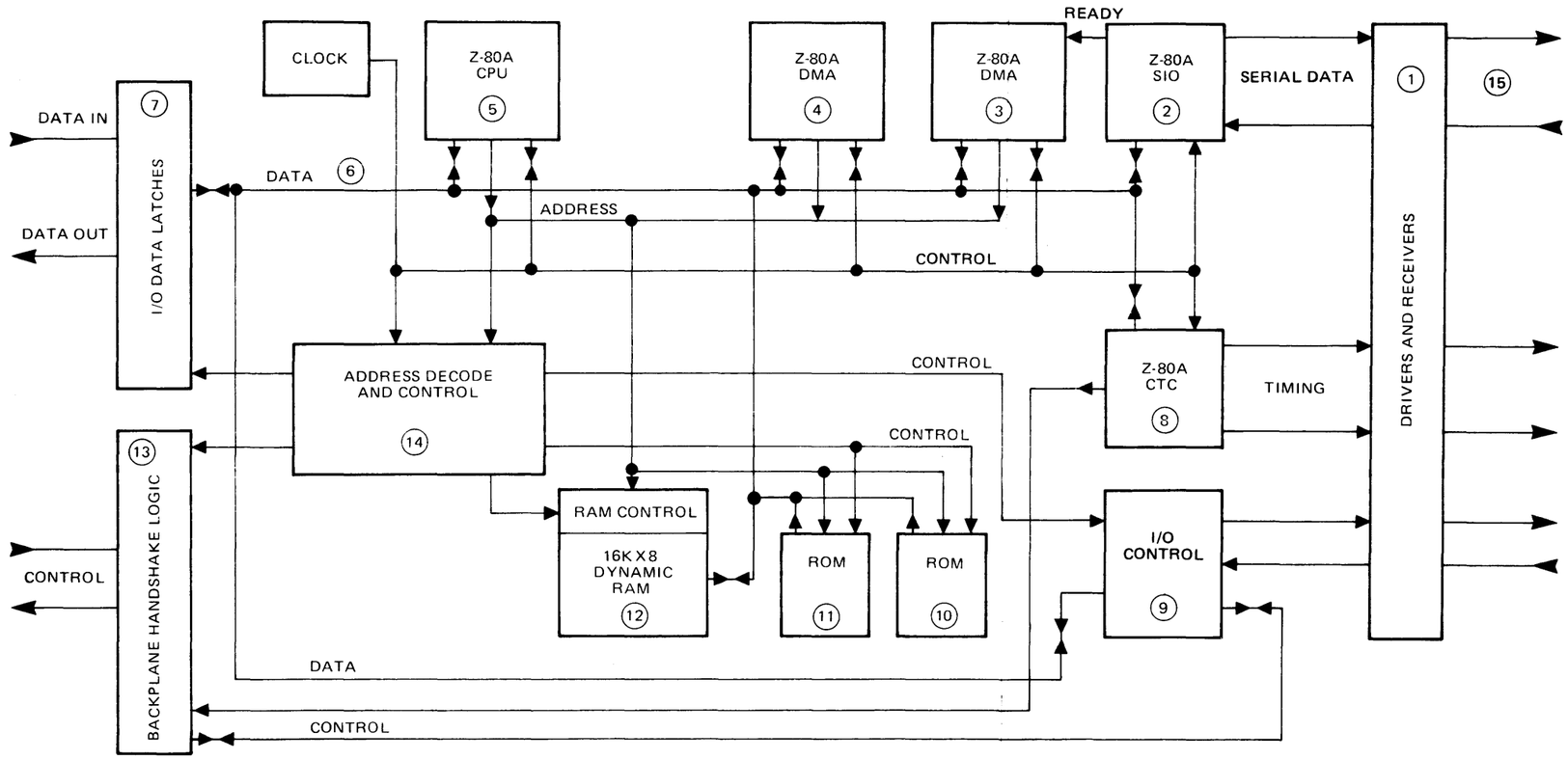
The Z-80A CPU (Central Processing Unit) employs a register-based architecture which includes two sets of six general-purpose registers which can be used as 8-bit registers or 16-bit register pairs. Additional 8-bit registers include two sets of accumulator and flag registers, and the interrupt vector and memory refresh registers. Additional 16-bit registers include the stack pointer, program counter and two index registers. The Z-80A CPU provides the intelligence for the card to function as a preprocessor to relieve the host computer of a majority of protocol processing.

An important pin on the Z-80A as far as this card is concerned is the NMI (Non-Maskable Interrupt) input pin. By pulling this input low with an STC instruction, the host computer can "get the attention of" the Z-80A. An NMI is the highest priority interrupt to the Z-80A and forces it to start fetching and executing instructions from a predetermined location in the firmware. The host software driver uses this feature to inform the card that it requires service.

Various support chips are used in conjunction with the Z-80A CPU to facilitate the cards operation as an intelligent serial interface. These chips are discussed in the paragraphs that follow.

Serial Input/Output (SIO)

A Z-80A SIO chip is used on the card to provide the serial data communications channel. The major functions performed by the SIO chip are serial-to-parallel conversion of input data and parallel-to-serial conversion of output data.



HP 12044A HDLC DIRECT-CONNECT INTERFACE

Figure 4-1. HDLC Interface Functional Block Diagram.

Direct Memory Access (DMA)

The card uses two Z-80A DMA chips which are LSI DMA controllers. One of these DMA chips is used to transfer data between the SIO channel and memory; the other is used to transfer data between the host computer and memory on the card. The function of the DMA logic is to transfer bytes of data in a manner that will be transparent to the Z-80A CPU. This enables the card to achieve higher throughput rates.

Counter Timer Circuit (CTC)

The card uses one Z-80A CTC chip which provides four independent counter/timers. Two of the counter/timers are used as a baud rate generators and one is used as a timer for the HDLC protocol. The fourth is used to maximize the effective throughput of the card by controlling the frequency of DMA cycle stealing.

Read-Only Memory (ROM)

The card uses 6k bytes of ROM on two chips. All of the software required for the Z-80A CPU to implement the functions of HDLC protocol generation and backplane interaction control is contained in these ROM's and is referred to as firmware. The self-check routine is also contained in ROM.

Random-Access Memory (RAM)

The card has 16k bytes of dynamic RAM. This memory is used for data buffers and the storage of firmware variables. The refresh capability of the Z-80A CPU is used to provide the appropriate refresh signals to the dynamic RAM chips.

Communication Line Interface

The communication line interface is the point at which the various signals used are received onto the card or driven onto the communications line. The signals sent from the card are Send Data (SD), Transmit Timing (TT), and Send Common (SC). The signals received are Receive Data (RD), Receive Timing (RT), and Receive Common (RC).

These signals are conveyed through the use of differential drivers and receivers (as per EIA RS-422) connected by four individually shielded, twisted pair cables. (This connection is illustrated in Section 7.) A differential driver drives both the inverted and non-inverted signal to a differential receiver. The advantage of the differential drivers and receivers is that they offer higher noise immunity than single-ended drivers and receivers, thus allowing longer cable lengths and higher data signalling rates. The receivers on the card can survive an input voltage range of +/- 25 volts. The receivers on the card can operate with a maximum common mode input voltage of +/- 7 volts. These voltages are with respect to Receive Common (RC). The card can operate with a 1.5 KV potential between the receiver portion of the card (RC) and the transmitter portion of the card (SC).

Command and Status Words

In addition to data words, command and status words are also exchanged between the host and the card . These additional words are transferred across the data bus and the data latches to aid in the process of communication between the host and the card.

Command words are initiated by the host driver and fall into the following four basic categories:

Type 0 - initiates a data transfer from a card buffer to a host computer buffer.

Type 1 - a single word command sent directly to the card firmware. Examples include disconnect, abort current operation, discard input buffer, etc.

Type 2 - initiates a data transfer from a host computer buffer to a card buffer.

Type 3 - specifies that a multiple-word command is to follow.

Status words are generated by the card to inform the host of events that have occurred, are occurring or will be occurring on the card or communications line. Examples of these messages include transfer buffer ready, connect complete, error condition and message block size.

Functional-Level Description

The description given in this section is of a typical operation of the card. The host computer assumed for this discussion is an HP 1000 L-Series Computer and the direct-connect is made to a HP 1000 M/E/F-Series Computer.

Power-Up

Initially, the HP 1000 has been powered up and the communications line is not yet operational. At power-up, a reset signal is asserted by the power supply and is released 1 millisecond after all supplies are stable. This signal resets all logic on the card, including the Z-80A system components. The resetting of the Z-80A CPU invokes a ROM-resident self-test routine which makes its pass/fail message available to the host driver.

Connect Sequence

The two ends of the communications line must be logically connected (physical connection is assumed at this point). The primary sends a SARM frame (refer to Section 3 for a desription of the HDLC protocol) and waits for a UA frame from the secondary. In our HP 1000-to-HP 1000 configuration, each card sends a SARM frame and waits for a UA frame. When this handshake sequence is complete, a logical connection exists between the two computers.

I/O Backplane Processing

The card communicates with the HP 1000 L-Series Computer through the I/O master that is physically located on the card. For the purposes of the functional-level descriptions given below, the I/O Master will remain transparent. All transfers should be thought of as occurring through the I/O backplane in the conventional manner. The functional-level descriptions of input (card-to-host) and output (host-to-card) data transfers reference the logic blocks and data paths by number according to Figure 4-1.

The steps involved in a transfer from the host computer to the communications line (i.e., an output transfer) are as follows (the numbers in parentheses reference the various data paths and functional areas in Figure 4-1):

1. The host (software) driver enables a request for output buffers (command type 1) onto the data latches (7) and then causes a Z-80A NMI (5). Because of the NMI, the firmware interprets the data in the latches as a command.

2. When a buffer becomes available, the host driver requests a transfer (command type 2) and enables the DMA hardware of the host.

3. The card writes zeros to the output latches (7). This starts the DMA transfer from the host involving the backplane latches (7), control logic (13), data bus (6), Z-80A DMA chip (4) and RAM (12).

4. The card interrupts the host (13) when the data transfer is complete.

5. The host may transfer additional blocks of data to the the card as buffer space becomes available. Steps 2 through 4 are repeated until the messsage is transferred from the host to the card in its entirety.

6. Each data block in the RAM buffer on the card is transferred via DMA (3) to the SIO (2) when the SIO chip becomes ready for the transfer. The SIO chip transmits the data as it is received via DMA. The CRC frame check sequence is sent as required.

Keep in mind that the Z-80A CPU (5) is controlling all of the processing on the card by executing instructions that its fetches from ROM (10) and (11). This is referred to as the card firmware.

The steps involved in a transfer from the communications line to the host computer (i.e., an input transfer) are as follows:

1. The host driver enables inputs from the card by writing a command word (command type 1) into the data latches (7).

2. The card firmware then sends a status word via the data latches (7) to the host driver informing it that an input buffer is available.

3. The host driver issues a request for input data (command type 0) and enables the host DMA hardware.

4. The card enables the first data word into the data latches (7) and asserts SRQ via the backplane logic (13).

5. The host driver begins the data transfer and the data block is transferred from the RAM (13) on the card to the host via a DMA chip (4), the data bus (6), the backplane latches (7) and the backplane handshake logic (13). Steps 2 through 5 are repeated until the entire message has been transferred.

6. The host driver re-enables the card for status inputs.

Disconnect Sequence

The communications line is logically disconnected after each station sends a DISC frame and receives a UA frame. Either end of the DS link can initiate the disconnect sequence.

Section 5
Maintenance

Introduction

This section provides maintenance information for the HP 12044A HDLC Direct Connect Interface. Included are preventive maintenance instructions and troubleshooting information.

Preventive Maintenance

There is no preventive maintenance (PM) necessary for the HP 12044A other than a routine inspection of the equipment which can be performed at the same time that PM is done for the entire system. The card and cables should be checked for broken components, or the presence of foreign objects.

A self-test, residing in the firmware, is executed each time that power is applied to the card or the card is reset. In this manner, the interface card is checked automatically and only requires more thorough testing when specific failures occur.

Removal and Installation Procedures for the IOP Chip

WARNING

OBSERVE EYE HAZARD SAFETY PRECAUTIONS
Wear safety glasses when removing or installing the retaining clips on the IOP chip.

CAUTION

STATIC SENSITIVE DEVICE
Use anti-static handling procedures when removing or installing the IOP chip. (See page vii.)

Removing the IOP Chip

The chip is removed from its socket as follows:

1. Remove the card from the computer and place it on a flat surface.

2. While pressing down on one of the retaining clips with a thumb, insert the flat blade of a screwdriver or similar instrument between the retaining clip and the side of the socket.

3. Twist the bottom portion of the blade away from the socket to free the retaining clip (A) from the bottom edge of the socket (see Figure 5-1).

4. When the retaining clip (A) is free, lift it up and over the chip.

5. Remove the second retaining clip by following steps 2 through 4.

6. Carefully tip the card on edge and remove the chip. Observe the anti-static handling precautions when handling the chip.

Installing the IOP Chip

The chip is installed in its socket as follows:

1. Observe the anti-static handling precautions when handling the chip.

2. Place the card on a flat surface with the component side up.

3. Remove both retaining clips from the socket, if they are in place (see Figure 5-1).

4. Place the chip in the socket, locating the two flat corners (B) of the socket facing the two flat corners of the chip. The trace side of the chip package must be on the bottom when the chip is placed in the socket.

5. Place the retaining clips in the two places provided for them in the side of the socket.

6. Press down with a thumb on the retaining clip (A) and press the retaining clip over the edge of the socket until it snaps under the bottom edge of the socket (B).

7. Install the second retaining clip, following steps 3 through 6.

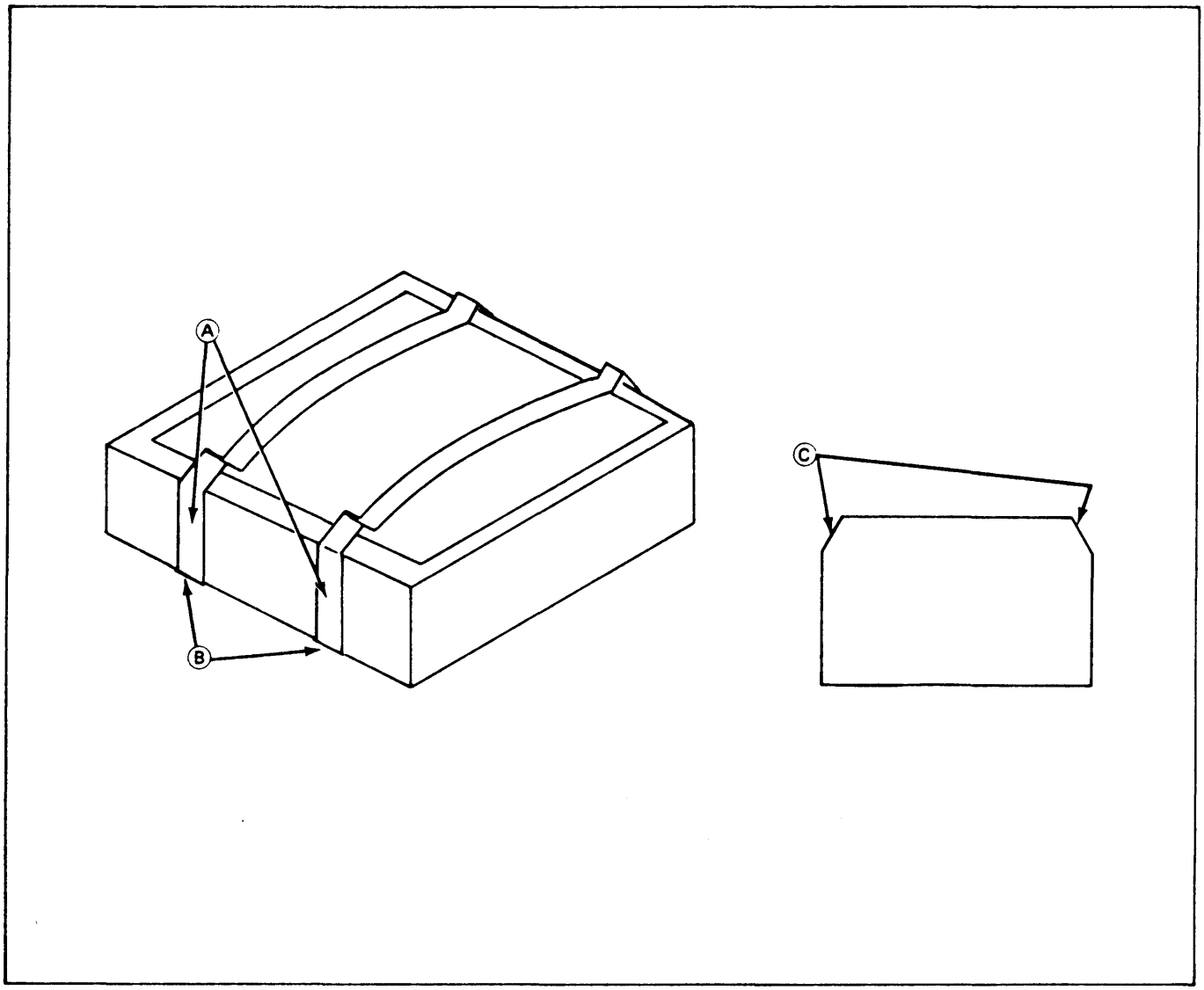


Figure 5-1. IOP Chip Socket With Retaining Clips

Troubleshooting Techniques

CAUTION

ALWAYS TURN POWER OFF TO THE COMPUTER AND OTHER ASSOCIATED EQUIPMENT WHEN INSERTING OR REMOVING INTERFACE CARDS OR CABLES. FAILURE TO DO SO COULD RESULT IN DAMAGE TO THE EQUIPMENT.

CAUTION

STATIC SENSITIVE DEVICES

THE ROMS, RAMS, AND Z-80A COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE REPLACING.

After it has been determined that the hardware of the HP 1000-to-HP 1000 link is failing, proceed as follows to localize the failure to the specific component failing:

1. Run the DSINF card configuration check. Follow the procedure outlined in the interface card configuration check paragraphs in Section 2 of this manual.

2. Run the computer self-test. Refer to the HP 1000 L-Series Computer Installation and Service Manual, part no. 02103-90003, or the HP 1000 L-Series Computer System Installation and Service Manual, part no. 02145-90003. This test will do a general check of system hardware and the Input Output Processor (IOP) chip and logic on each interface card installed in the computer.

3. Run the kernel diagnostic. Refer to the Kernel Diagnostic Operating Manual, part no. 24397-90002. This test will do a more thorough check of the IOP and associated logic on each interface card installed.

4. Run the interface card self-test. This test is located in the firmware of the HP 12044A. It examines Z-80A CPU operation, on-board DMA operation (channels 0 and 1), counter/timer chip performance, RAM and ROM memory, and some parts of the receiver/driver circuits and controller. The test does not check the backplane circuitry on the card.

   The self-test is run each time power is applied to the card or the card is reset. It can be run by cycling power on the system. Note that this procedure requires system and DS software reinitialization after running the test. It is recommended that the node is quiesced before running the self-test. This will allow all pending DS transactions to be completed and prevent new ones from starting. To quiesce the node, enter the commands RU,DSMOD<cr> and, after DSMOD prompts for a command, enter /Q. (For a description of DSMOD, refer to DS/1000-IV Network Manager's Manual, HP part number 91750-90003.) DSMOD prompts for the network security code which can be obtained from the network manager. The default security code is DS. Once the "NODE IS QUIESCENT" message appears on the screen, cycle the power on the computer.

   Self-test results are made available to the driver once the test is complete. To find out if the card passed the self-test, try executing the LU command on that card after running DSINF, as described in the interface card configuration check given in Section 2. The LEDs on the card will also indicate successful completion of the tests with all of them being turned off at the end of the self-test before DS software has been reinitialized.

5. Run the loop-back verifier hood test by proceeding as follows:

   a. Quiesce the node. This allows all pending transactions to be completed and prevents new ones from starting before running the test. Follow the same procedure used in step 4 for quiescing the node. Remove power from the computer once the node is quiescent.

b. Remove the cable from the front edge connector and install the loop-back verifier hood, HP part number 5061-3421, in its place, orienting the connector the same as all other connectors in the card cage.

c. Restore power to the system. When this occurs, the self-test is automatically executed on the card. The results of the test are returned to the software driver. Restore the operating system and check that the self-test completed successfully and that the hood was sensed by running DSINF and checking the information returned with the LU command.

d. Once it has been established that the card has passed the self-test and that the hood has been sensed, a further check of the card can be accomplished by sending a message to the card and having it looped back on itself. This will thoroughly check out all message sending and receiving capabilities of the card and card/computer interaction capabilities. To configure the card to talk to itself, start by running DSMOD. Enter the command CN. DSMOD will prompt for the network security code which can be obtained from the network manager. After that has been entered, DSMOD will prompt for the node number to be changed. Enter the local node number. DSMOD will display the current routing vector for the local node which should specify LU 0. Then after the prompt for the new configuration, enter the LU # of the card that has the loop-back verifier hood installed on it. Now enter /E in response to the prompt for the next node number to be changed, and another /E to exit DSMOD. The card is now configured to talk to the local node.

e. Run REMAT and execute some REMAT commands such as TI or DL. When this happens, the routing vector will specify that all commands to be executed at the local node should be sent out to the configured interface card. The card will transmit the data, it will be looped back through the hood, and the card will receive the data and send it back to the local CPU. If no errors are returned, this is a very good indication that the interface card and backplane circuitry are operational.

f. After the test is complete, run DSMOD and reconfigure the local node routing vector to again specify LU 0.

g. To remove the loop-back verifier hood, remove power from the system and replace the hood with the cable.

h. Restore power to the computer and reinitialize the system and DS software.

Since the loop-back verifier hood test checks more areas of the card (specifically the line drivers/receivers area of the interface, and the backplane interface circuitry), it is possible for the card to pass the self-test and fail the loop-back hood test. Therefore, it is important that both the self-test and loop-back verifier hood tests are run.

6. If the cables are suspected of causing the failure, it is possible to run the self-test with a test connector installed that jumpers the proper signals together (see Section 7 of this manual for wiring diagrams showing how to make one of these test connectors). To do this, install the connector at some point in the cabling used and run the self-test on the interface card. If the card passed the self-test without the connector installed and fails with the connector installed, it indicates a problem with the cables being used.

7. If a failure is found using one of the above described tests, replace the failing card, firmware, or IOP chip and re-run the test that failed to ensure that the problem has been corrected. For information on repair or replacement of the failing components, contact the nearest Hewlett-Packard Sales and Service Office. (Sales and Service offices are listed at the back of this manual.)

8. If desired, further isolation to a defective part (other than the firmware ROMs or IOP) may be performed. Refer to the Servicing Diagram information given in Section 7 of this manual and replaceable parts information given in Section 6.

Section 6
Replaceable Parts

Introduction

This section contains information for ordering replaceable parts for the HP 12044A HDLC Direct Connect Interface. Table 6-1 gives a list of replaceable parts, and Table 6-2 contains names and manufacturers of the parts.

Replaceable Parts

Table 6-1 contains a list of replaceable parts in reference designation order. The following information is listed for each part:

1. Reference designation of the part.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity (QTY).
5. Description of the part.
6. A five-digit manufacturer's code number of a typical manufacturer of the part.
7. The manufacturer's part number.

Ordering Information

To order replacement parts or to obtain information on parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office (Sales and Service Offices are listd at the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will insure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, specify the following information:

1. Identification of the kit containing the part (refer to the product identification information supplied in Section 2).

2. Description and function of the part.

3. Quantity required.

Table 6-1. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	5061-3434	5	1	LC PROGRAM SER IF	28480	5061-3434
C4	0160-0576	5	8	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
C5	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
C6	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
C7	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
C8	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
C9	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
C16	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
C17	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
CR3	1990-0662	0	1	LED-VISIBLE LUM-INT=200UCD IF=5MA-MAX	28480	1990-0662
Q1	1853-0015	7	1	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
Q2	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
Q3	1854-0467	5	1	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
R2	1810-0280	8	2	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R3	1810-0276	2	2	NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
R7	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
R33	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
S1	3101-2243	6	1	SWITCH-DIP, 8-ROCKER	28480	3101-2243
S2	3101-1983	9	1	SWITCH-DIP, 8-ROCKER	28480	3101-1983
T1	9100-2643	4	1	TRANSFORMER-DATA COMM	28480	9100-2643
U10	1820-2145	9	1	IC DRVR TTL LINE DRVR QUAD	04713	MC3487P
U11	1820-1729	3	2	IC LCH TTL LS COM CLEAR 8-BIT	01295	SN74LS259N
U12	1820-1298	1	1	IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS251N
U13	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U14	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U15	1820-1989	7	2	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U16	1820-1201	6	2	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U17	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U18	1820-1997	7	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U20	1820-1244	7	3	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
U21	1820-1729	3		IC LCH TTL LS COM CLEAR 8-BIT	01295	SN74LS259N
U22	1820-2024	3	5	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U23	5090-1614	0	1	IC-6309-1	28480	5090-1614
U24	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U25	1820-1440	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
U26	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U27	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U28	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U31	1820-2300	8	1		28480	1820-2300
	1200-0654	7	4	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
U32	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U33	1820-0693	8	2	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U34	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U35	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U36	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U37	1820-2102	8	4	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U38	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U40	1820-2203	0	2	IC RCVR TTL LS LINE RCVR QUAD	34335	AM26LS32PC
U44	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U45	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U46	1820-1240	3	1	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U47	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U48	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U50	1820-1244	7		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
U51	1820-2299	4	2		28480	1820-2299
	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
U53	5090-0599	8	1	IC-ROM	28480	5090-0599
U54	1818-0341	8	8	IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
	1200-0607	0	8	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U55	1820-1677	0	2	IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U56	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U57	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U58	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U60	1820-2117	5	1	IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U61	1820-2299	4			28480	1820-2299
	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
U63	1820-2301	9	1		28480	1820-2301
	1200-0567	1	3	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
U64	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U65	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N

Table 6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U66	1820-1322	2	2	IC GATE TTL S NOR QUAD 2-INP	01295	SN74802N
U67	1AC5-6001	7	1	21 I/O CHIP	28480	1AC5-6001
U70	1820-1244	7		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74L8153N
U71	1820-2298	3	1		28480	1820-2298
	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
U74	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U75	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74L8374N
U76	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74800N
U84	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U85	1820-2075	4	1	IC MISC TTL LS	01295	SN74L8245N
U86	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN748112N
	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
U94	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U95	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74L8240N
U96	1820-1451	8	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74838N
U101	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74L8161AN
U102	1820-1470	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74L8157N
U103	1820-1207	2	1	IC GATE TTL LS NAND 8-INP	01295	SN74L830N
U104	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U106	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74800N
U107	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74832N
U108	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN748240N
U110	1820-2203	0		IC RCVR TTL LS LINE RCVR QUAD	34335	AM26L832PC
U111	1990-0461	7	1	OPTO-ISOLATOR LED-IC GATE IF=10MA-MAX	28480	5082-4364
U113	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74L8157N
U114	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U116	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN748240N
U117	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74802N
U118	1820-1451	8		IC GATE TTL S NAND QUAD 2-INP	01295	SN74838N
U122	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U124	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U125	1820-0220	9	1	IC V RGLTR TO-39	27014	LM320H-05
	1200-0185	9	1	INSULATOR-XSTR NYLON	28480	1200-0185
XW1	1200-0483	0	1	SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0483
XW2	1200-0455	6	1	SOCKET-IC 8-CONT DIP-SLDR	28480	1200-0455
				MISCELLANEOUS PARTS		
	1200-0845	8	2	RETAINER-SUBSTRATE STEEL; NICKEL PLATE	28480	1200-0845
	1200-0848	1	1	SOCKET-SSTR 64-CONT CERAMIC DIP-SLDR	28480	1200-0848
	1480-0116	8	1	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
	5061-3435	6	1	AXIAL INSERTION	28480	5061-3435

Table 6-2. Manufacturer's Code List

CODE NO.	MANUFACTURER ADDRESS	CODE NO.	MANUFACTURER ADDRESS
0003J	Nippon Electric Co.	07263	Fairchild Semiconductor Div. ... Mt. View, CA 94042
01121	Allen-Bradley Co. ... Milwaukee, WI 53204	18324	Signetics Corp. ... Sunnyvale, CA 94086
01295	Texas Instr. Inc. Semicond. Cmpnt. Div. ... Dallas TX 75222	27014	Natl.Semiconductor Corp. ... Santa Clara, CA 95051
03508	General Electric Co., Semiconductor Prod. Dept. ... Syracuse, NY 13201	28480	Hewlett-Packard Co. Corporate Hq. ... Palo Alto, CA 94304
04713	Motorola Semiconductor Prod. .. Phoenix, AZ 85062	34335	Advanced Micro Dev. Inc. .... Sunnyvale, CA 94086
		34344	Motorola Inc. ... Franklin Park, IL 60131

Section 7
Servicing Diagrams and Information

Introduction

This section contains servicing diagrams and information for the HP 12044A HDLC Direct Connect Interface.

Table 7-1. Backplane Pin Connector P1.

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
1	ICHID-	Interrupt Chain In Disable
2	ICHOD-	Interrupt Chain Out Disable
3	MCHID-	Memory Chain In Disable
4	MCHOD-	Memory Chain Out Disable
5	MLOST-	Memory Lost
6	MCHODOC-	Memory Chain Out Disable Open Collector
7	PFW-	Power Fail Warning
8	(SPARE 1)	
9	SCB0	Select Code Bus Bit 0
10	SCB1	Select Code Bus Bit 1
11	SCB2	Select Code Bus Bit 2
12	SCB3	Select Code Bus Bit 3
13	GND	Ground
14	GND	Ground
15	(SPARE 2)	
16	GND	Ground
17	SCB4	Select Code Bus Bit 4
18	SCB5	Select Code Bus Bit 5
19	AB0	Address Bus Bit 0
20	AB1	Bit 1
21	AB2	Bit 2
22	AB3	Bit 3
23	AB4	Bit 4
24	AB5	Bit 5
25	AB6	Bit 6
26	AB7	Bit 7
27	AB8	Bit 8
28	AB9	Bit 9

Table 7-1. Backplane Pin Connector P1. (Continued)

29	AB10	Bit 10
30	AB11	Bit 11
31	AB12	Bit 12
32	AB13	Bit 13
33	AB14	Bit 14
34	WE-	Write Enable
35	DB0	Data Bus Bit 0
36	DB1	Bit 1
37	DB2	Bit 2
38	DB3	Bit 3
39	DB4	Bit 4
40	DB5	Bit 5
41	DB6	Bit 6
42	DB7	Bit 7
43	DB8	Bit 8
44	DB9	Bit 9
45	DB10	Bit 10
46	DB11	Bit 11
47	DB12	Bit 12
48	DB13	Bit 13
49	DB14	Bit 14
50	DB15	Bit 15

Table 7-2. Backplane Pin Connector P2.

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
1	(SPARE 3)	
2	ISOGND	Isolated Ground
3	REMEM-	Remote Memory
4	VALID-	Data Valid
5	IORQ-	I/O Handshake Request
6	INTRQ-	Interrupt Request
7	MP	Memory Protect
8	RNI	Read Next Instruction
9	MEMGO-	Memory Cycle Initiation
10	PE-	Parity Error
11	SCHID-	Slave Chain In Disable
12	SCHOD-	Slave Chain Out Disable
13	IAK-	Interrupt Acknowledge
14	IOGO-	I/O Handshake Request Acknowledge
15	ISOGND	Isolated Ground
16	SLAVE-	Slave Request
17	ISOGND	Isolated Ground

Table 7-2. Backplane Pin Connector P2. (Continued)

18	MRQ-	Memory Request
19	ISOGND	Isolated Ground
20	FCLK-	Fast Clock
21	ISOGND	Isolated Ground
22	CCLK-	Communications Clock
23	PS-	Parity Sense
24	SCLK-	System Clock
25	CRS-	Control Reset
26	PON	Power On
27	ISOGND	Isolated Ground
28	BUSY-	Memory Busy
29	GND	Ground
30	GND	Ground
31	GND	Ground
32	GND	Ground
33	GND	Ground
34	GND	Ground
35	+5V	
36	+5V	
37	+5V	
38	+5V	
39	+12V(MEM)	
40	-12V(MEM)	
41	+12V	
42	+12V	
43	-12V	
44	-12V	
45	+5V(MEM)	
46	+5V(MEM)	
47	25KHz	
48	25KHz	
49	25KHz	
50	25KHz	

Table 7-3. Communication Line Connector J1.

PIN NO.	*SIGNAL MNEMONIC	SIGNAL DEFINITION
1	SG	Signal Ground
2	SD (-)	Send Data
3	TR (-)	Terminal Ready
4	RS (+)	Request to Send
5	TT (+)	Terminal Timing
6	RD (-)	Receive Data
7	CS (+)	Clear to Send
8	SQ	Signal Quality
9	RT (+)	Receive Timing
10	ST (-)	Send Timing
11	RT (-)	Receive Timing
12	ST (+)	Send Timing
13	RR (+)	Receiver Ready
14	DM (+)	Data Mode
15	B DATA CLK	
16	DB	Send Timing
17	DA	Terminal Timing
18	**TT	Terminal Timing
19	SRD	Secondary Receive Data
20	BX16 IN	
21	**RS	Request to Send
22	SRS	Secondary Request to Send
23	LL	Local Loopback
24	NS	New Signal
A	(SHIELD)	
B	SD (+)	Send Data
C	TR (+)	Terminal Ready
D	RS (-)	Request to Send
E	TT (-)	Terminal Timing
F	RD (+)	Receive Data
H	RC	Receive Common
J	CS (-)	Clear to Send
K	SCS	Secondary Clear to Send
L	DM (-)	Data Mode
M	RR (-)	Receiver Ready
N	SRR	Secondary Receiver Ready
P	TM	Test Mode
R	IC	Incoming Call
S	ASYNC CLK	
T	DD	Receive Timing
U	SF/SR	Select Frequency/Signalling Rate
V	**TR	Terminal Ready
W	SG	Signal Ground
X	X16 IN	

Table 7-3. Communication Line Connector J1. (Continued)

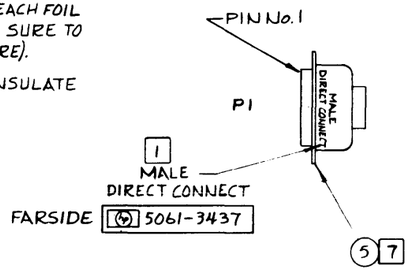
Y	**SD	Send Data
Z	SSD	Secondary Send Data
AA	RL	Remote Loopback
BB	IS	Terminal in Service

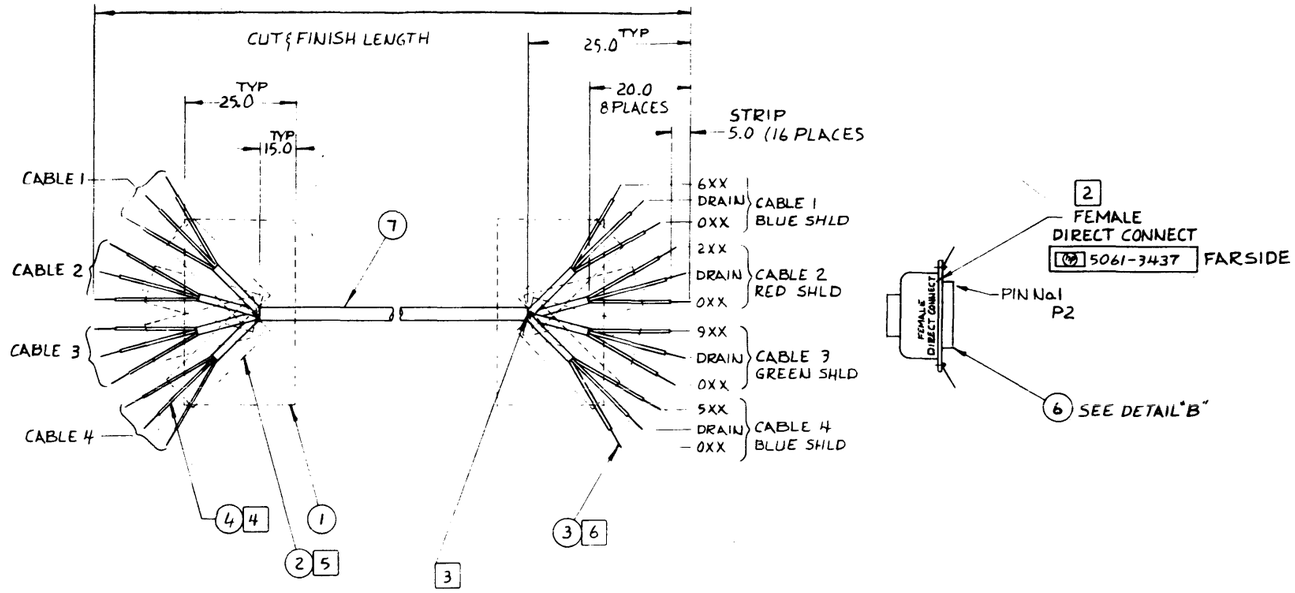
* The +/- sign associated with some signals indicates a +/- output(input) of a differential driver(receiver).

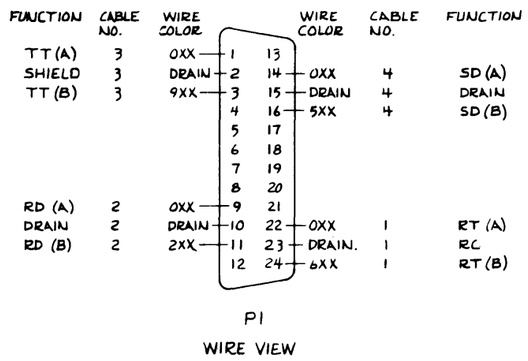
** Indicates that this signal is driven by a single-ended driver although it is available on different pins in a differentially driven version.

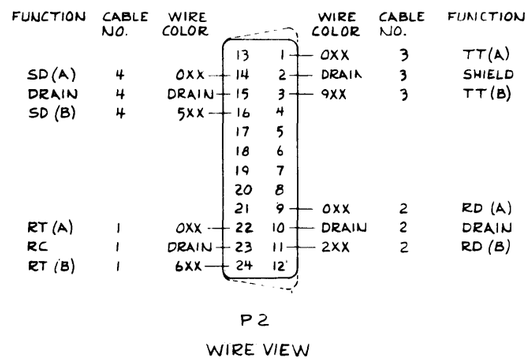
NOTES:

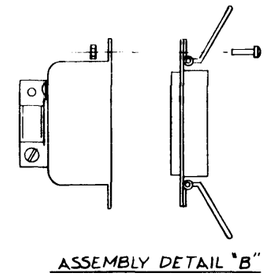
1. STAMP P1 HOOD AS SHOWN.
2. STAMP P2 HOOD AS SHOWN, BOTH SIDE.
3. IN CUTTING OUTER JACKET, PRACTICE CARE IN ORDER NOT TO NICK FOIL SHIELD, BOTH ENDS.
4. ⚠ PLACE A 15.0 PIECE OF SHRINK TUBING, ITEM ④ OVER BARE DRAIN WIRE AND SHRINK 8 PLACES, LEAVING 5.0 ENDS EXPOSED.
5. SLIDE A 20.0 PIECE OF SHRINK TUBING (ITEM 2) OVER EACH FOIL SHIELD, UP TO OUTER JACKET, AND SHRINK (MAKING SURE TO COVER ALL OF SHIELD AND APPROX 5.0 OF EXPOSED WIRE).
6. PLACE A 8.0 PIECE OF SHRINK TUBING (ITEM 3) TO INSULATE ADJACENT CONNECTION.
7. ASSEMBLE P1 PER A-5951-3043-1.





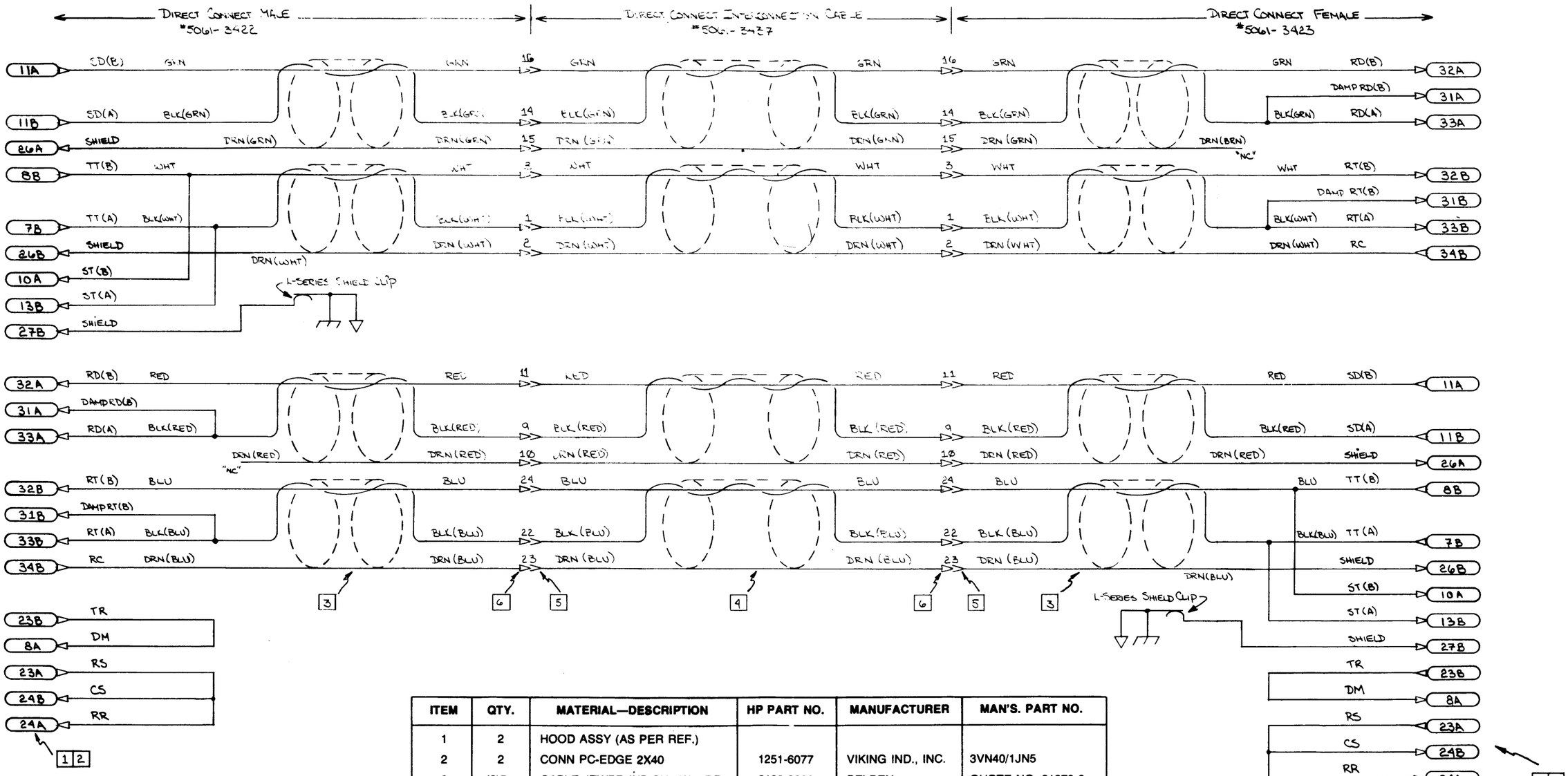






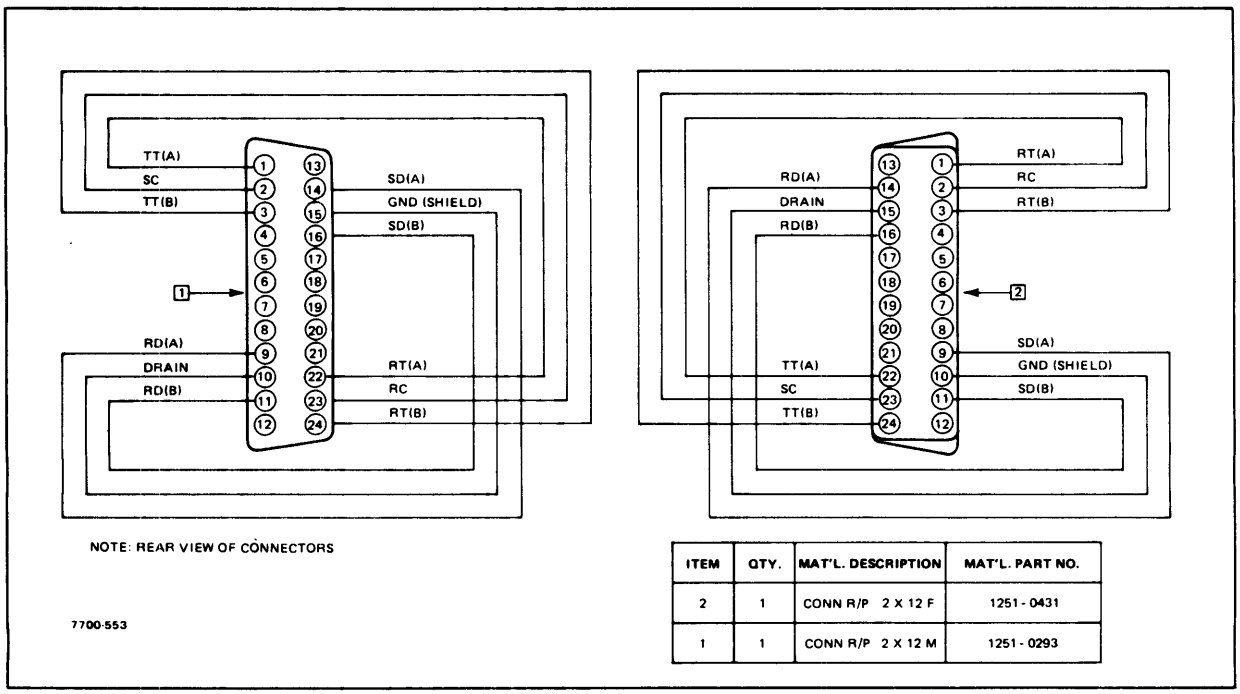
ITEM	QTY.	MATERIAL—DESCRIPTION	HP PART NO.	MANUFACTURER	MAN'S PART NO.
1	30mm	SHRINK TUBING	0890-0273	RAYCHEM CORP.	RNF-100-1/2-BLK
2	30mm	SHRINK TUBING	0890-0311	RAYCHEM CORP.	RNF-100-1/8-BLK
3	75mm	SHRINK TUBING	0890-0706	RAYCHEM CORP.	RNF-100-3/32-BLK
4	120mm	SHRINK TUBING	0890-0870	RAYCHEM CORP.	RNF-100-3/32-CLEAR
5	1	CONNECTOR 24 PIN MALE	1251-0293	AMPHENOL	57-30240
6	1	CONNECTOR 24 PIN FEMALE	1251-0431	AMPHENOL	57-60240
7	75m	CABLE	8120-3096	BELDEN	QUOTE NO. 81379-9

Figure 7-1. Direct-Connect Cable Schematic.



ITEM	QTY.	MATERIAL—DESCRIPTION	HP PART NO.	MANUFACTURER	MAN'S. PART NO.
1	2	HOOD ASSY (AS PER REF.)			
2	2	CONN PC-EDGE 2X40	1251-6077	VIKING IND., INC.	3VN40/1JN5
3	(2)5m	CABLE 4TWPR IND.SH. W 4DR.	8120-3096	BELDEN	QUOTE NO. 81379-9
4	75m	CABLE 4TWPR IND.SH. W 4DR.	8120-3096	BELDEN	QUOTE NO. 81379-9
5	2	CONN R&P 2X12 FEMALE	1251-0431	AMPHENOL	57-60240
6	2	CONN R&P 2X12 MALE	1251-0293	AMPHENOL	57-30240

Figure 7-2. Direct-Connect Cable Wiring Diagram.



ITEM	QTY.	MAT'L. DESCRIPTION	MAT'L. PART NO.
2	1	CONN R/P 2 X 12 F	1251-0431
1	1	CONN R/P 2 X 12 M	1251-0293

Figure 7-3. Loop-Back Test Connector Wiring Diagram.

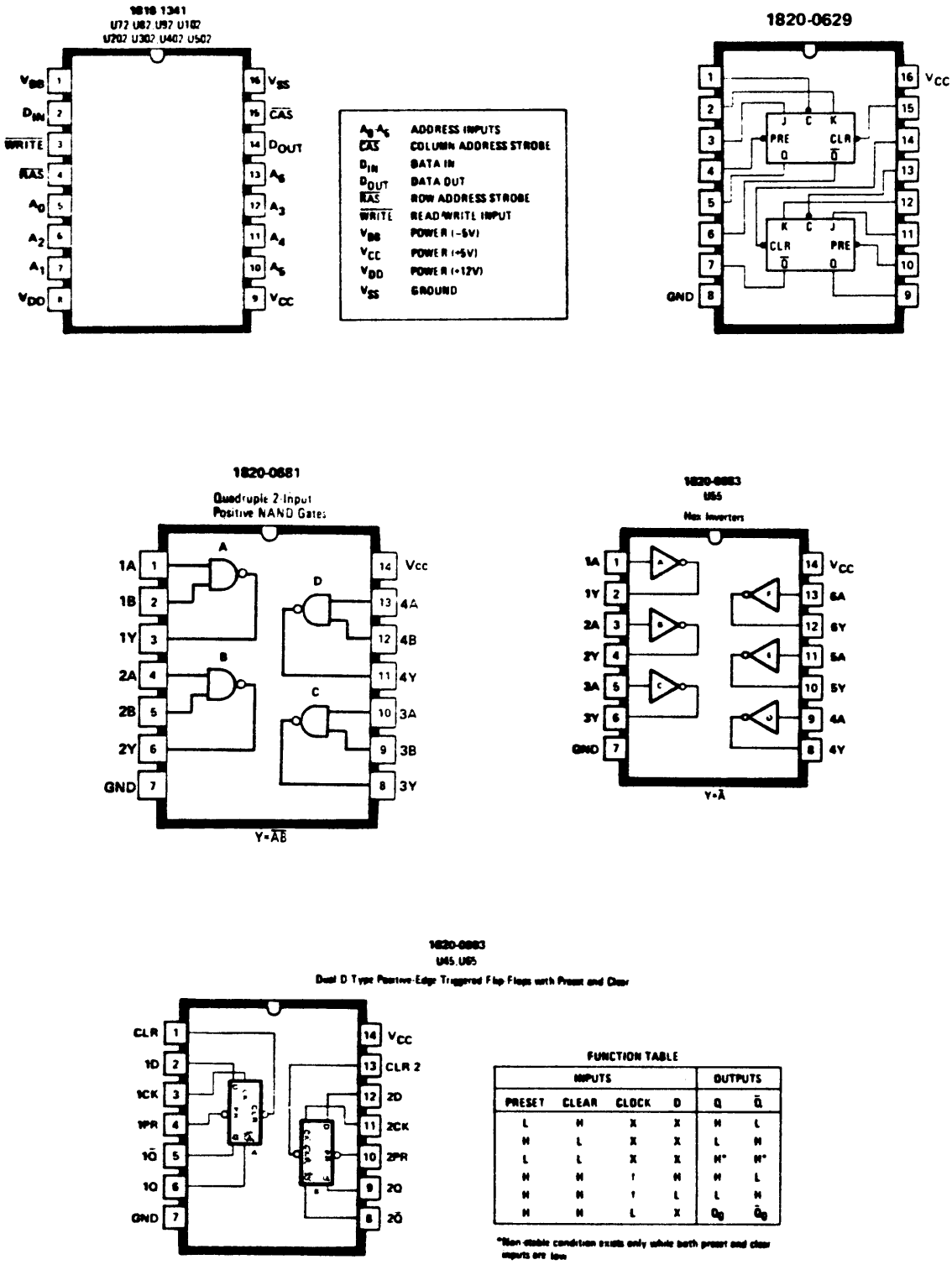


Figure 7-4. Integrated Circuit Base Diagrams.

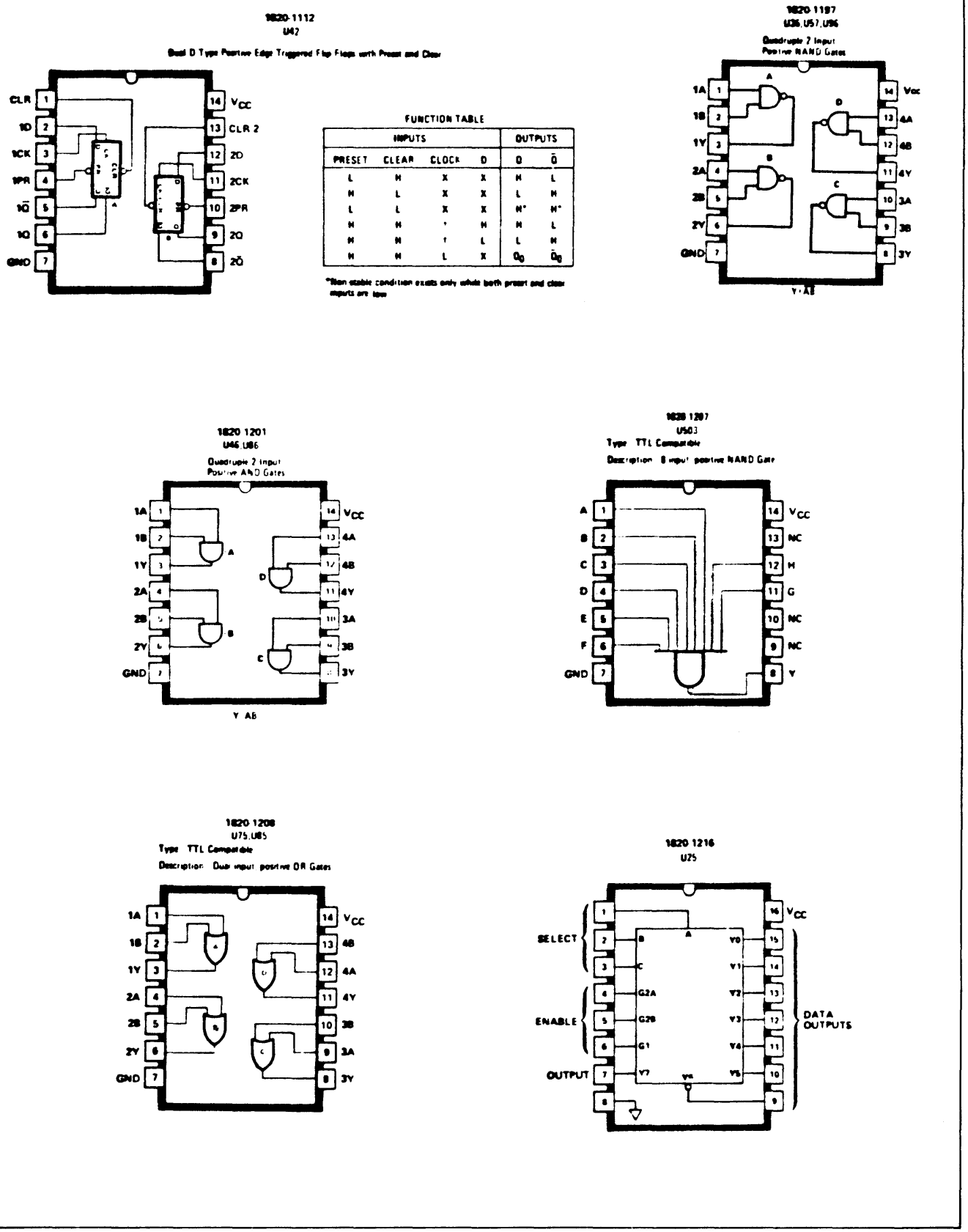


Figure 7-4. Integrated Circuit Base Diagrams (Continued)

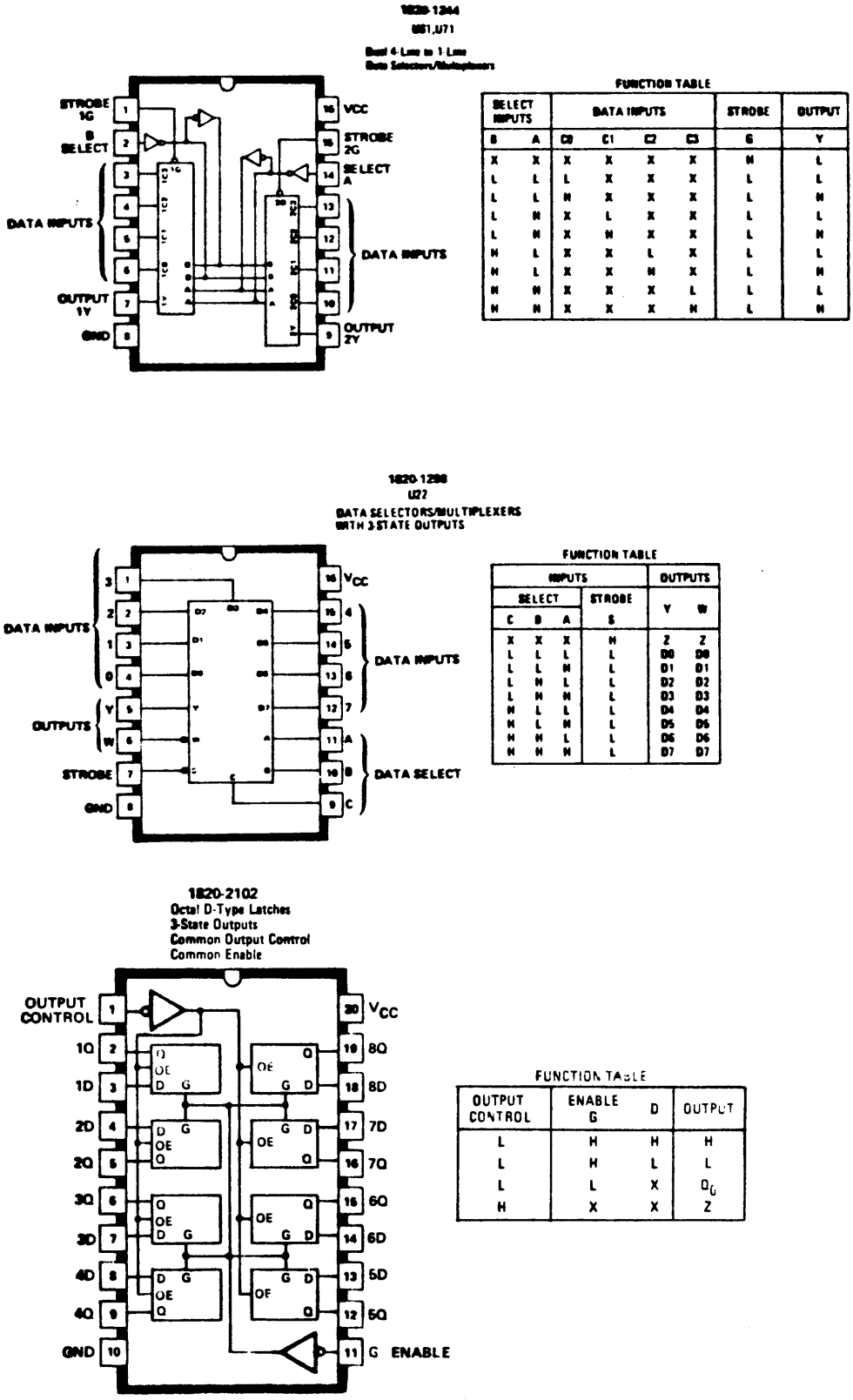


Figure 7-4. Integrated Circuit Base Diagrams (Continued)

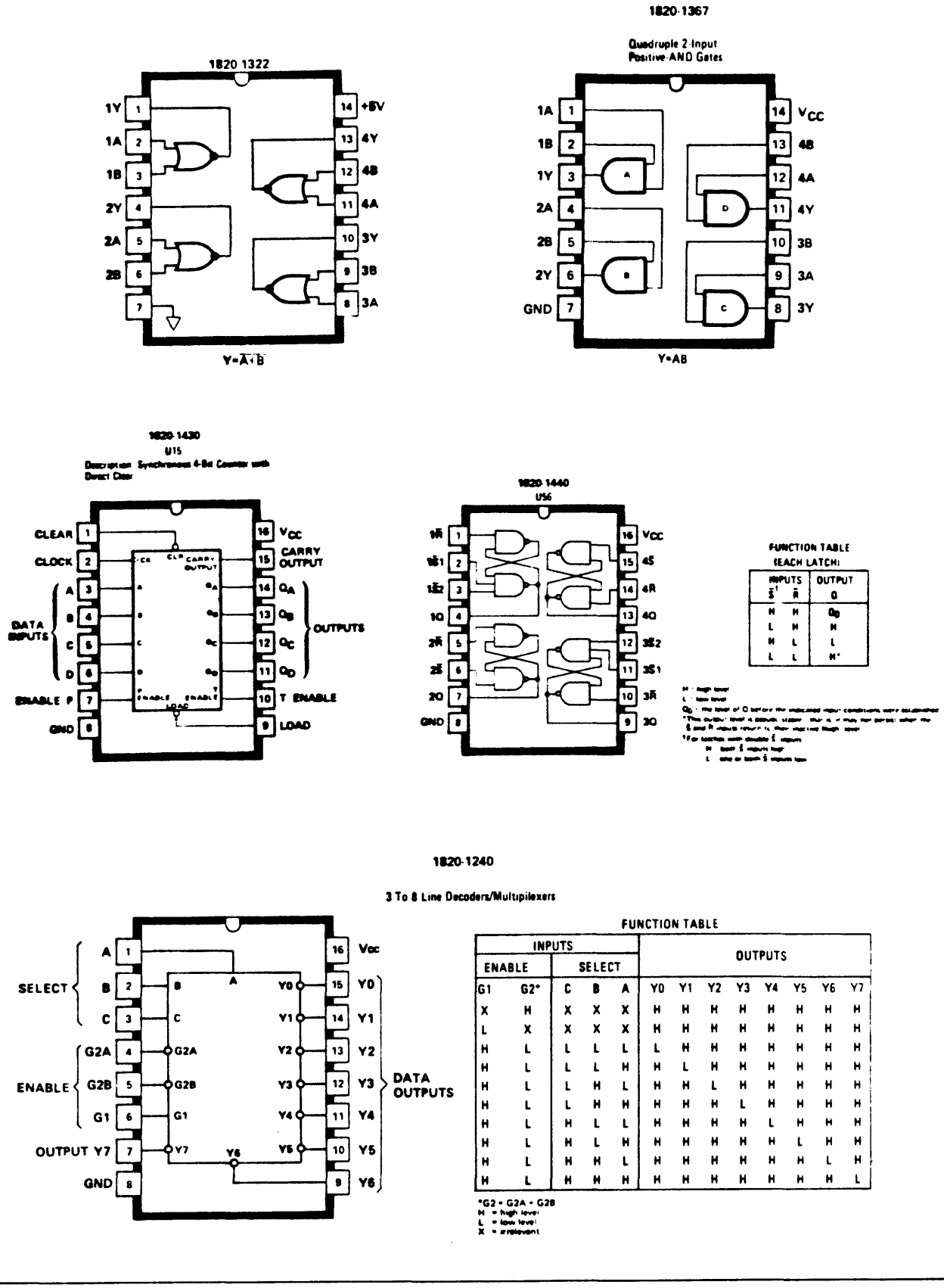
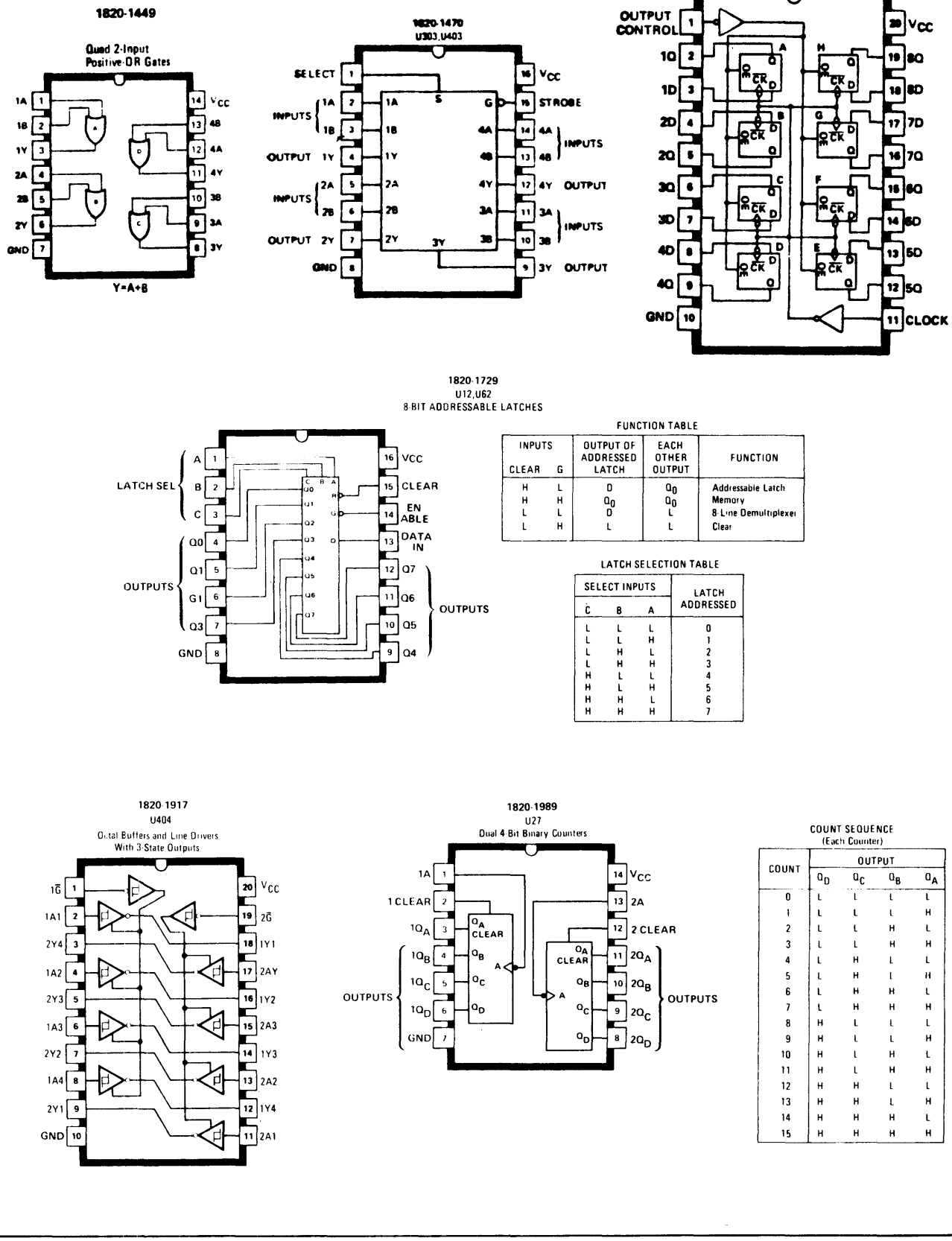


Figure 7-4. Integrated Circuit Base Diagrams (Continued)



FUNCTION TABLE

INPUTS CLEAR	INPUTS G	OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
H	L	D	Q_0	Addressable Latch
H	H	Q_0	Q_0	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

LATCH SELECTION TABLE

SELECT INPUTS C	B	A	LATCH ADDRESSED
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

COUNT SEQUENCE
(Each Counter)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Figure 7-4. Integrated Circuit Base Diagrams (Continued)

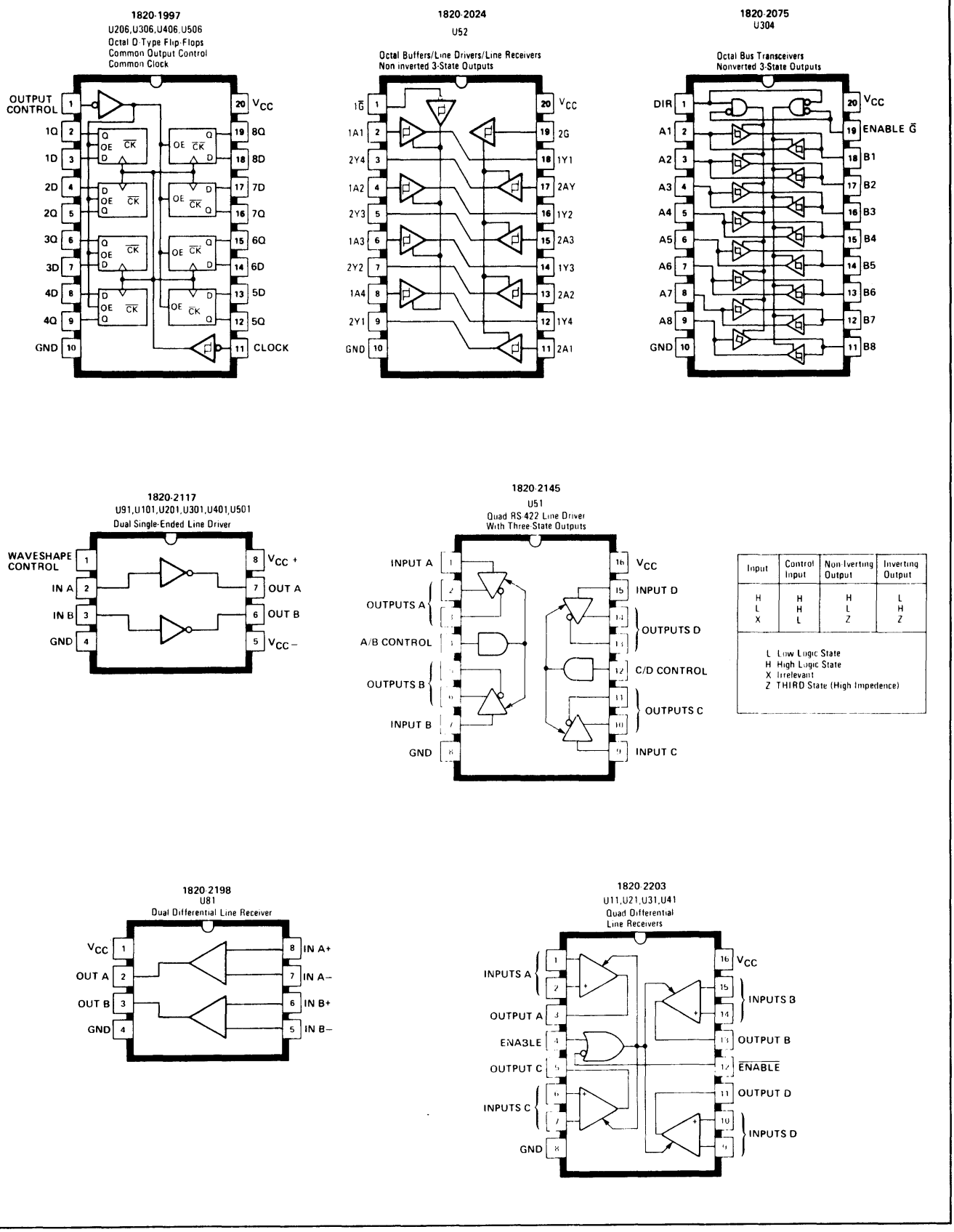


Figure 7-4. Integrated Circuit Base Diagrams (Continued)

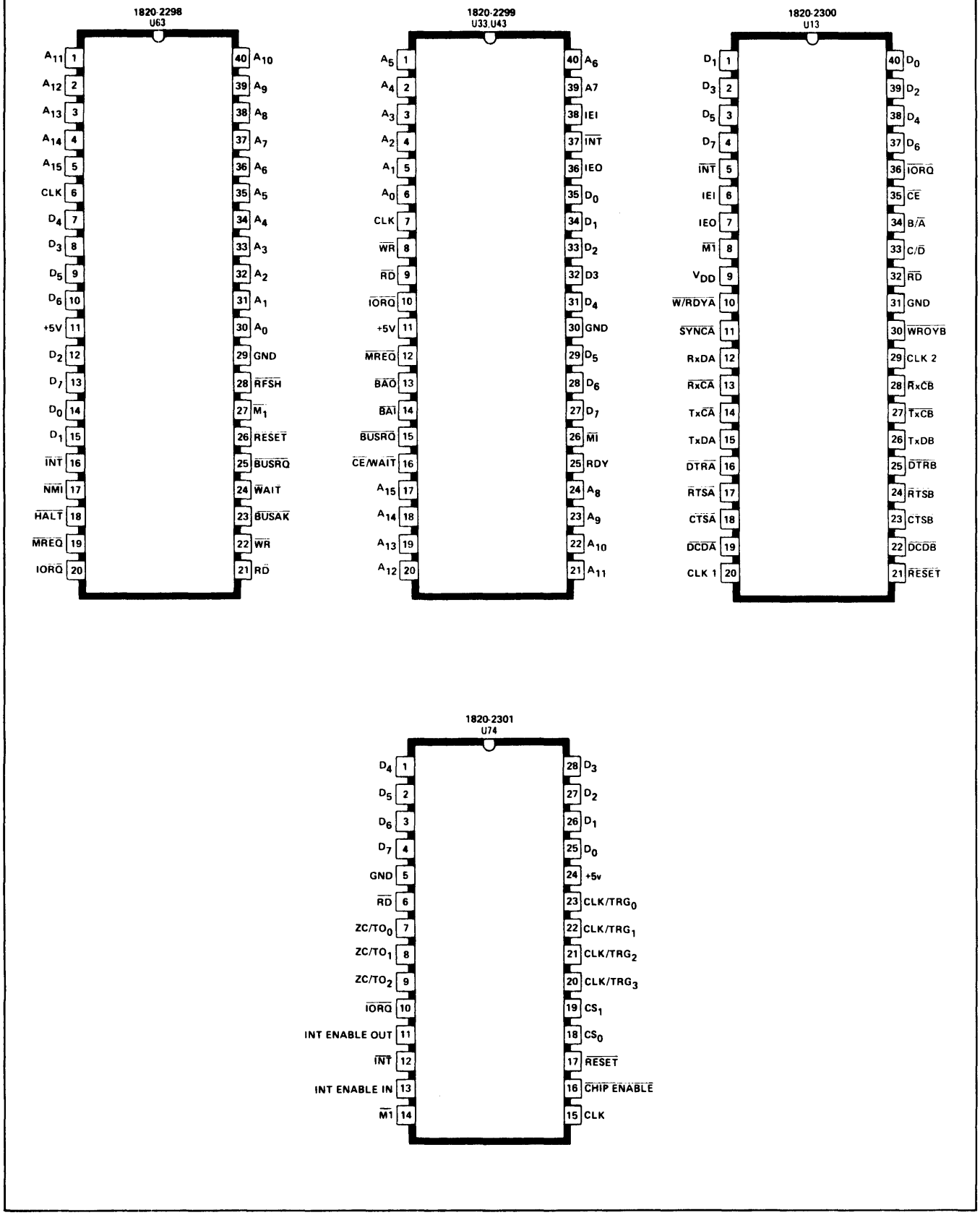
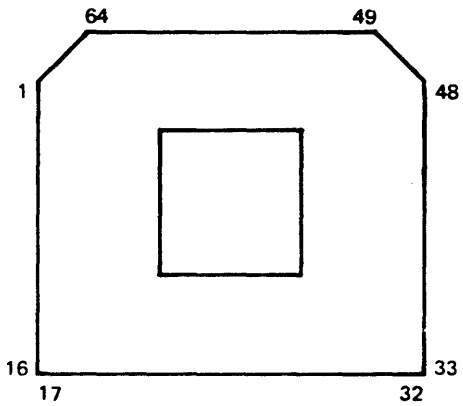


Figure 7-4. Integrated Circuit Base Diagrams (Continued)



1AC5-6001 I/O PROCESSOR (IOP) CHIP OUTLINE (COMPONENT SIDE)

PIN DEFINITIONS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	DMACYC –	17	GND	33	RNI +	49	VCC
2	LOADMAR +	18	VDD	34	CRS +	50	GND
3	SCEN –	19	CW1 –	35	IEN –	51	VDD
4	REMEM –	20	BCW2 +	36	DIAG –	52	CB7 +
5	INTCYC +	21	BCW1 +	37	DVCMD –	53	CB8 +
6	DMAEN –	22	BCW0 +	38	PULSLV +	54	CB9 +
7	LOBYT –	23	VALID +	39	PON +	55	CB10 +
8	SACK –	24	IOGO +	40	SLACK +	56	CB11 +
9	NC	25	ICHID –	41	SLRQ –	57	CB12 +
10	SCLK +	26	IAK +	42	CB0 +	58	CB13 +
11	LSBYT –	27	CFF –	43	CB1 +	59	CB14 +
12	PE +	28	IORQ –	44	CB2 +	60	CB15 +
13	MP –	29	IOEN –	45	CB3 +	61	MGO +
14	SRQ –	30	IOCLK +	46	CB4 +	62	MRQ +
15	IRQ –	31	PRDIS –	47	CB5 +	63	NC
16	VCC	32	GND	48	CB6 +	64	GND

Figure 7-4. Integrated Circuit Base Diagrams (Continued)

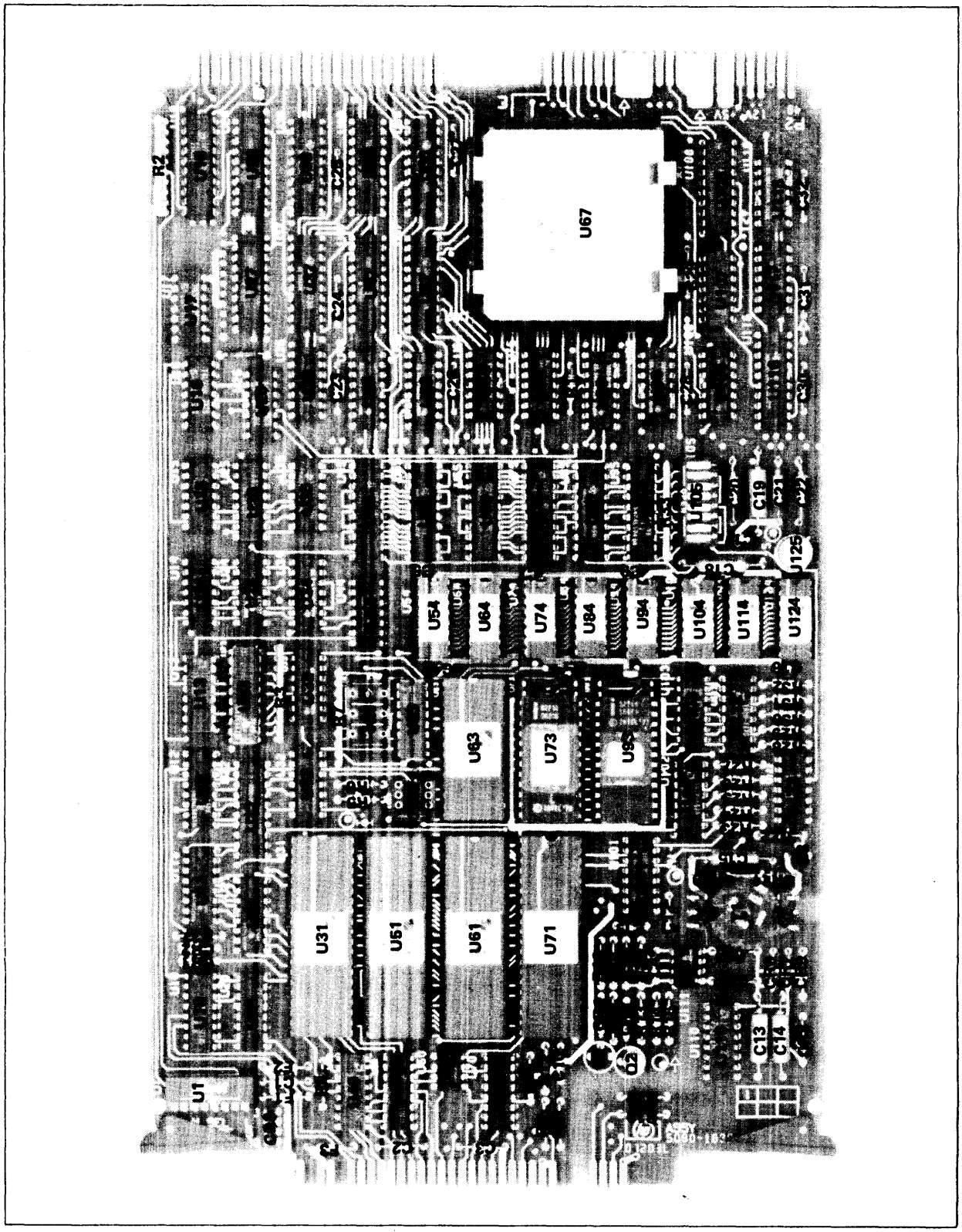


Figure 7-5. Parts Location Diagram.

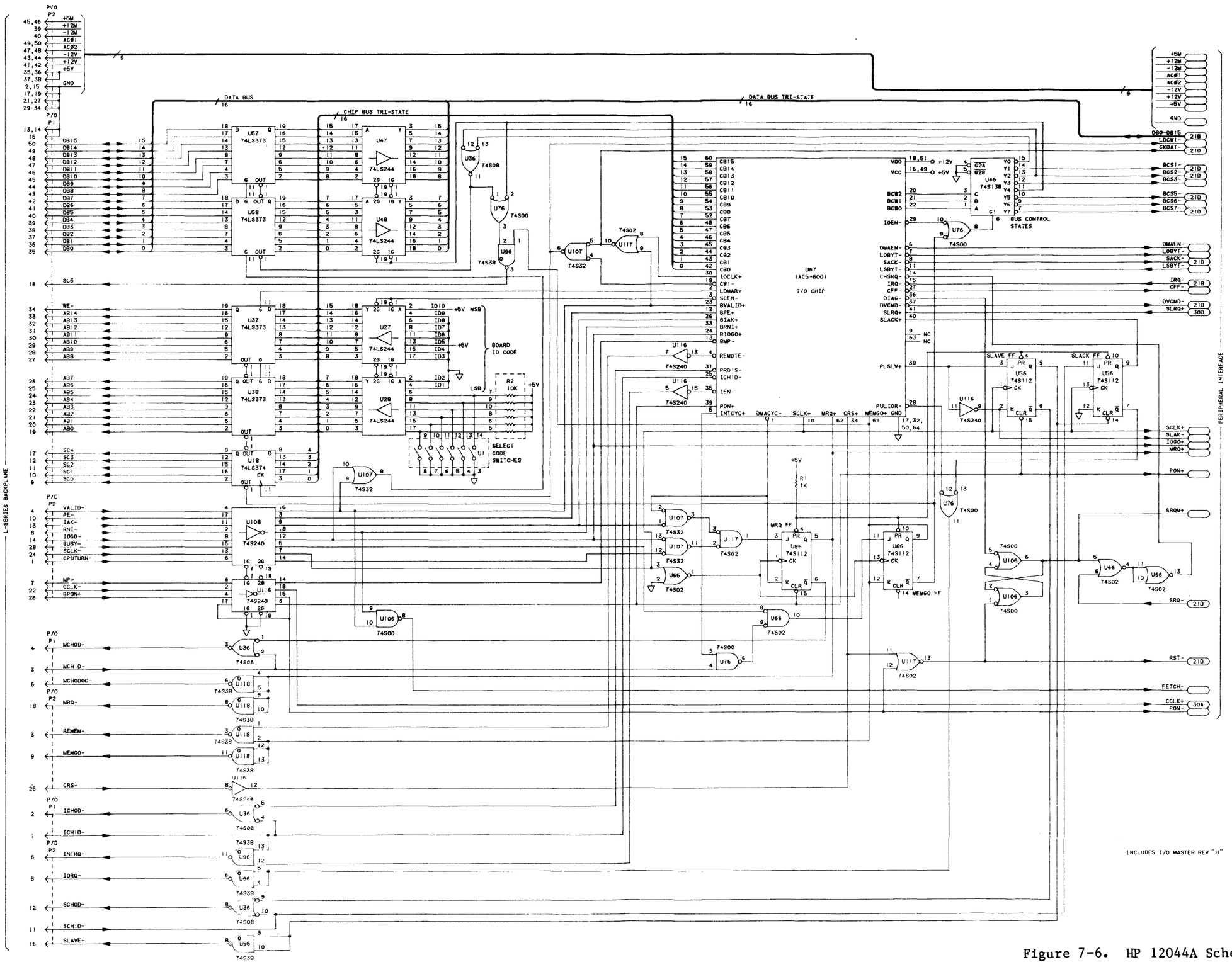


Figure 7-6. HP 12044A Schematic Logic Diagram.

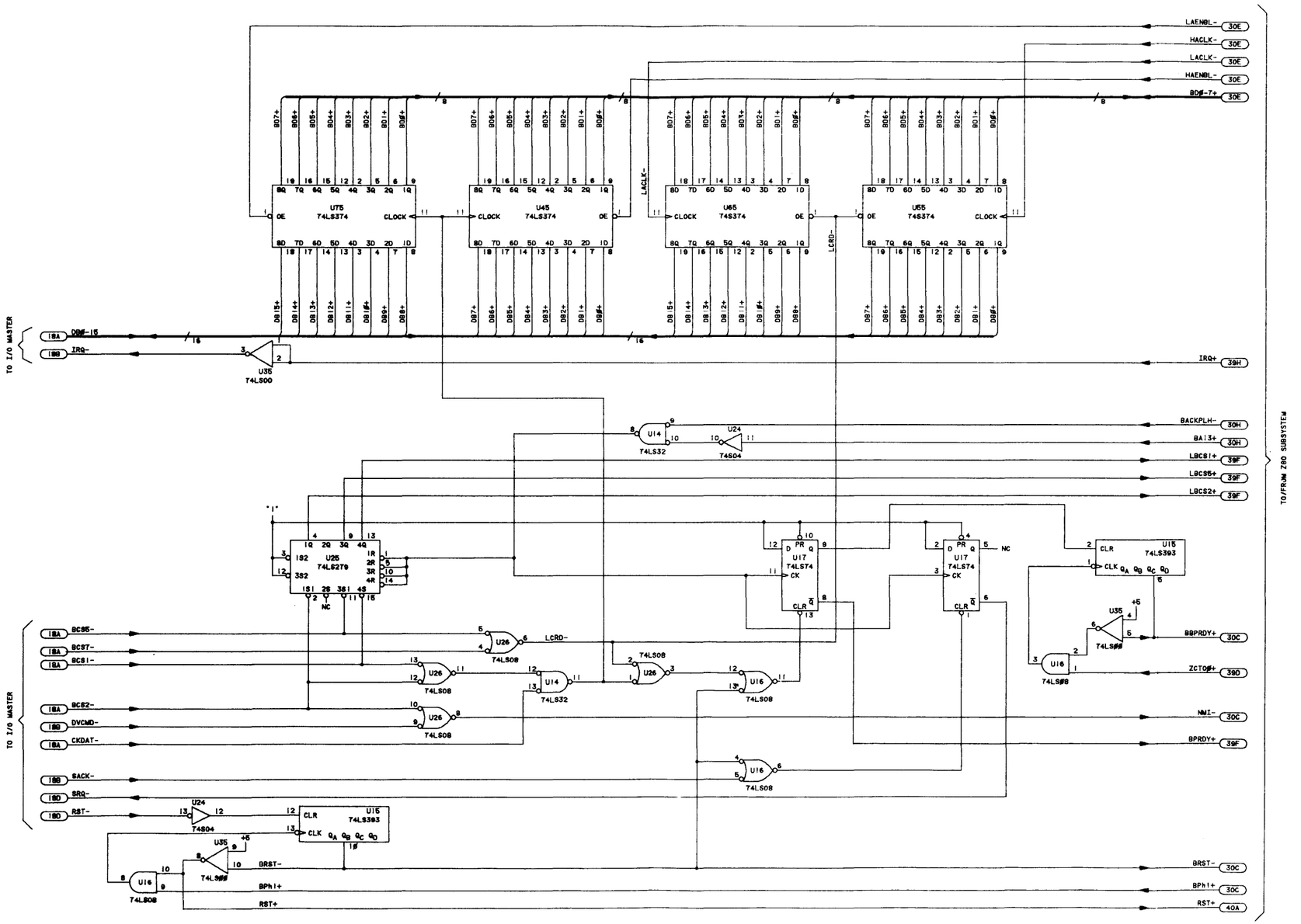
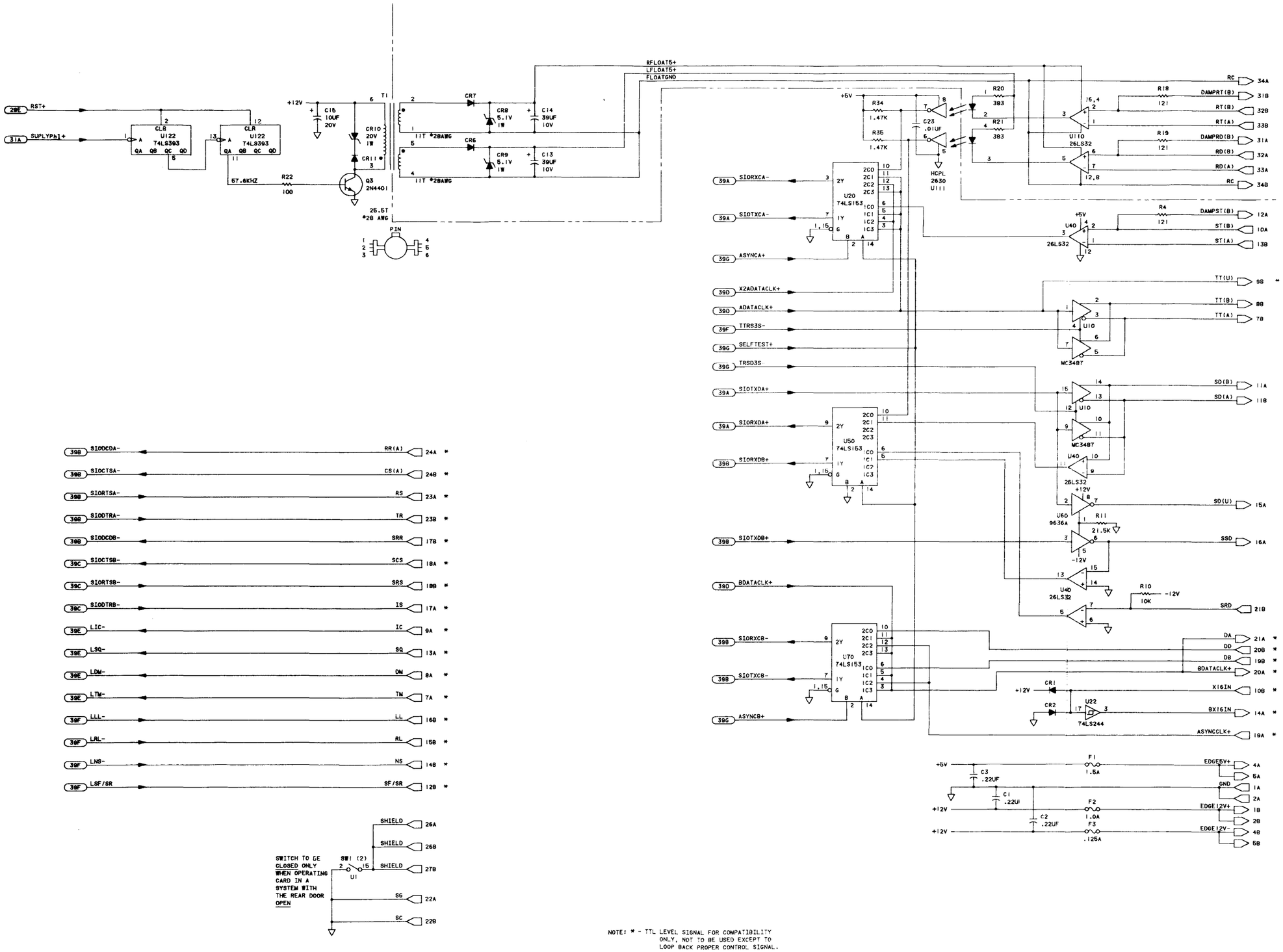


Figure 7-6. HP 12044A Schematic Logic Diagram. (Continued)

Figure 7-6. HP 12044A Schematic Logic Diagram. (Continued)



NOTE: * - TTL LEVEL SIGNAL FOR COMPATIBILITY ONLY, NOT TO BE USED EXCEPT TO LOOP BACK PROPER CONTROL SIGNAL.

Figure 7-6. HP 12044A Schematic Logic Diagram. (Continued)

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