HONEYWELL

HARDWARE BULLETIN

SERIES 200

201-2 CENTRAL PROCESSOR

In the Honeywell Series 200 Data Processing System, the 201-2 Central Processor is a computing and control center of the Model 200. It is subdivided into five major units: the arithmetic unit, the main memory, the control memory, the control unit, and the input/output traffic control. Under the direction of an internally stored program, the central processor monitors and coordinates the various activities of the entire system.

The arithmetic unit performs such operations as comparisons, binary and decimal addition/subtraction, and decimal multiplication/division.

The control memory is a magnetic core storage unit consisting of 16 individually addressable control registers. During a program run, the control registers are used to store the main memory addresses that direct the retrieval and execution of all instructions.

Using information stored in control memory, the control unit selects, interprets, and executes all of the instructions in the internally stored program. The Model 200 repertoire includes editing instructions, code translation instructions, a program interrupt instruction for automatic branching between a main program and servicing routines for all I/O devices, and two general-purpose input/output instructions, all in variable-length, two-address format.

The input/output traffic control directs the time sharing of the main memory among the central processor and as many as four simultaneously operating peripheral devices. The traffic control makes it possible, for example, to read cards, punch paper tape, print, read or write magnetic tape, and compute — all at the same time. Typically, the central processor is free to perform other operations during 80 to 99.9 percent of processing intervals shared with peripheral operations.

The basic 4,096-character, magnetic core main memory may be expanded initially by adding up to seven memory modules of 4,096 characters each, for a memory subtotal of 32,768 characters. Memory capacity may be further increased by adding up to four memory modules of 8,192 characters each, for a total capacity of 65,536 characters. Systems equipped with the indexed addressing ability include six index registers, plus nine more if the memory capacity exceeds 32,768 characters. There are no reserved input/output areas; the programmer has complete freedom in specifying both the sizes and the locations of these areas.

The interrupt processing facility of the 201-2 consists of a hardware program interrupt, which signals a particular condition in a peripheral control, and a set of instructions used in processing interrupts. A program interrupt may occur whenever a peripheral device has completed an input/output operation—for example, when a tape read or write operation is completed or after the receipt of a character from a remote station by a communication control. Peripheral interrupts can be inhibited by the program as necessary.

Specifications remain subject to change in order to allow the introduction of design improvements.

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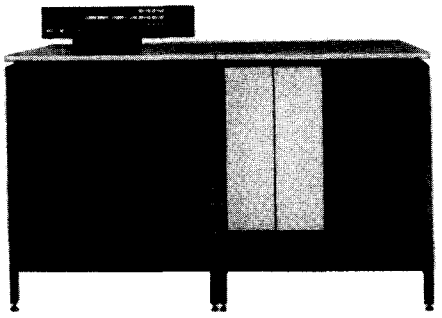

The multi-level code handling facility enables the processor to bring into memory and manipulate data in many different codes. This feature includes the ability to translate automatically between character codes of up to 12 levels and also to trap special code configurations of up to 12 levels.

An outstanding design feature of the Series 200 permits execution of stored programs in conjunction with a technique known as instruction bypass; this hardware facility provides for automatic changes in program sequence without executing programmed instructions to initiate such changes.

An integral part of the central processor is the operator's control panel. By using various control switches, the operator can start and stop the machine and can load and interrogate main and control memory locations. The control panel is equipped with four "sense switches" which can be used in conjunction with programmed instructions to control the path of program execution.

A significant structural feature is the use of integrated system modules. Each peripheral control and central processor logic unit is housed in a separate logic drawer which tilts out of the central processor housing for easy access.

SPECIFICATIONS

PROCESSING UNIT: Six-bit character.

DATA FORMAT: Variable-length data fields of from one to virtually the maximum number of characters in the main memory.

INSTRUCTION FORMAT: Variable-length, two-address instructions. Typical format consists of op code, two addresses, and a variant character.

MAIN MEMORY SIZE: Basic memory, 4,096 characters. Additional memory available consisting of up to seven 4,096-character modules, providing a memory size of 32,768 characters. Memory may be further enlarged with up to four 8,192-character modules, providing a total memory size of 65,536 characters.

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Honeywell

ELECTRONIC DATA PROCESSING

INTERNAL OPERATIONS: Decimal and binary add/subtract, decimal multiply/divide, logic, program control, peripheral control, and editing.

INPUT/OUTPUT TRUNKS: Eight, expandable to sixteen.

READ/WRITE CHANNELS: Three read/write channels are standard; an auxiliary channel is optional.

MAIN MEMORY CYCLE TIME: 2 microseconds.

CONTROL MEMORY ACCESS TIME: 250 nanoseconds.

CHECKING: Parity bit generated for each character as it is stored in memory. Character parity checked on readout.

ADDRESSING MODES: 2-character address specifies any of 4,096 memory locations, 3-character address specifies any of 32,768 memory locations, 4-character address specifies any of 65,536 memory locations.

TYPICAL OPERATING SPEEDS: 5-digit move A→B, 32 microseconds; 5-digit decimal add A+B→B, 44 microseconds; 5-digit decimal divide A/B→B, 215 microseconds; 5-digit compare A:B, 34 microseconds.

SPECIAL FEATURES: Silicon semiconductor circuitry, six (or fifteen) index registers, up to four simultaneous input/output operations concurrent with computing, program interrupt, indirect addressing, multi-level code handling.