M222XD2

Disk Drives
Customer Engineering Manual

FUJITSU

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CHAPTER 1 GENERAL DESCRIPTION

1 1 General Description

1.1.1 Introduction

The M222XD2 disk drive is a compact (3.5-inch micro-floppy size), and highly reliable fixed disk drive developed for random access data storage and retrieval in small computers, word processors, and terminals.
The storage capacities (unformatted) of the M2225D2, M2226D2 and M2227D2 are 25.62 MB, 38.43 MB and 51.24 MB respectively.

1.1.2 Features

(1) Compact size

Since the disks are 95 mm (3.74 in) in outer diameter and are driven by a DC motor directly connected to the spindle, the unit is extremely compact in size: 101.6 mm (4.00 in) (width) × 41.3 mm (1.63 in) (height) × 146 mm (5.75 in) (depth).

(2) High speed positioning

An optical encoder motor is used for head positioning to achieve fastest possible seek times.

(3) Large capacity

Up to four disks are assembled in the disk enclosure (DE), to provide a maximum unformatted storage capacity of 51.24 MB.

(4) High reliability

Heads, disks, and positioner are sealed to prevent contamination, and the air inside the DE is kept clean by a breather filter and recirculation filter. These features increase reliability by reducing the chance of contamination.

(5) No preventive maintenance

Preventive maintenance is not necessary.

(6) DC power

Only DC voltages of +12 V and +5 V are required.

(7) Vertical or horizontal installation

The drive may be installed in a system cabinet either vertically or horizontally. In the horizontal position, the PCB must be on the bottom. Vertically, it must not be mounted end above end.

(8) Low power consumption

The power consumption is 7.5 W (Steady State). This low power consumption enables the drive to be used in a very wide environmental temperature range (5 to 45°C).

(9) Low acoustic noise

The drive's low noise output, approx. 43 dB (A-scale weighting) even during seeking, makes it ideal for office use.

(10) Low vibration

The drive has four rubber vibration isolators, which minimize the transfer of motion.

(11) Highly integrated electronics

Microprocessor, LSIs and surface mount technology are utilized for the PCA to achieve high reliability and high integration. The head IC is located on head arms inside the DE to amplify the small signal. Read errors are reduced by increasing the signal to noise ratio.

1.2 Specification

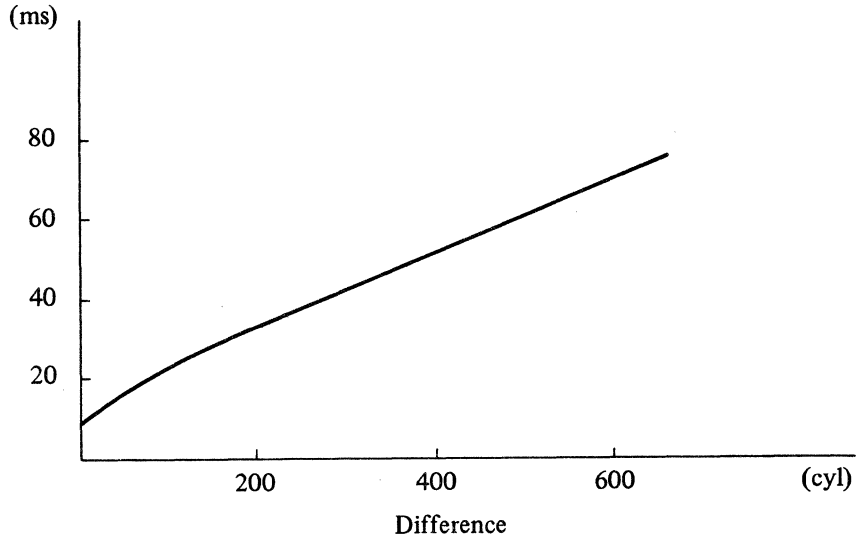
1.2.1 Functional specifications

Table 1.1 Functional specifications

Specifications \ Model		M2225D2	M2226D2	M2227D2
Total storage capacity				
Unformatted	(MB)	25.62	38.43	51.24
Formatted (*)	(MB)	20.15	30.22	40.30
Storage capacity/track				
Unformatted	(B)	10,416		
Formatted (*)	(B)	8,192		
Number of disks		2	3	4
Number of heads (R/W)		4	6	8
Number of cylinders		615		
Number of tracks/cylinder		4	6	8
Recording density	(BPI)	14,845		
Track density	(TPI)	834		
Transfer rate	(KB/s)	625		
Rotational speed	(rpm)	3,600		
Average latency time	(ms)	8.3		
Recording method		MFM		
Positioning time	Min (ms)	8		
	Ave (ms)	35		
	Max (ms)	75		
Input Voltage		+12 V±5% 0.45 A (max 2.0 A) + 5 V±5% 0.42 A		
External size				
Width × Height × Depth	(mm)	101.6×41.3×146 (W/O Panel dimension)		
Weight	(kg)	1.0		

(*) 256 bytes/sector for 32 sectors/track

(1) Positioning time



(2) Start and stop time

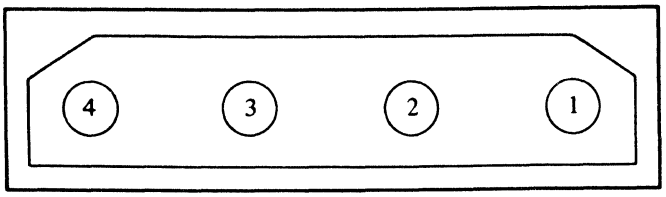
Start time (time from when power is turned on until the drive is ready) is 15 seconds or less and stop time (time to completely stop when power is turned off) is 25 seconds or less.

1.2.2 Environmental conditions

Temperature	Operating	5°C to 45°C
	Non-operating	-40°C to 60°C
	Gradient	15°C/h or less
Relative humidity	Operating	20% to 80% RH (Maximum wet bulb temp. 29°C)
	Non-operating	5% to 95% RH (Maximum wet bulb temp. 29°C) No condensation
Vibration	Operating	Less than 0.2G (3 to 60 Hz) 2 min × 30 cycles (sinusoidal waveform)
	Non-operating (power-off state after installation)	Less than 0.4G (3 to 60 Hz) 2 min × 30 cycles (sinusoidal waveform)
Shock	Operating	Less than 3G (maximum 10 ms)
	Non-operating During transportation and storage	Less than 40G (maximum 10 ms)
Altitude above sea level	Operating	3,000 m or below
	Non-operating time	12,000 m or below

1.2.3 Power requirements

(1) Power connector pin assignment



From cable side

1	+12 V
2	+12 V RTN
3	+5 V RTN
4	+5 V

(2) Input voltage tolerance and current

	Input Voltage	Peak Current	Average Current
+12 V	+12 V±5%	2.0 A max. (at seeking)	0.45 A_{TYP}
+5 V	+5 V±5%		0.42 A_{TYP}

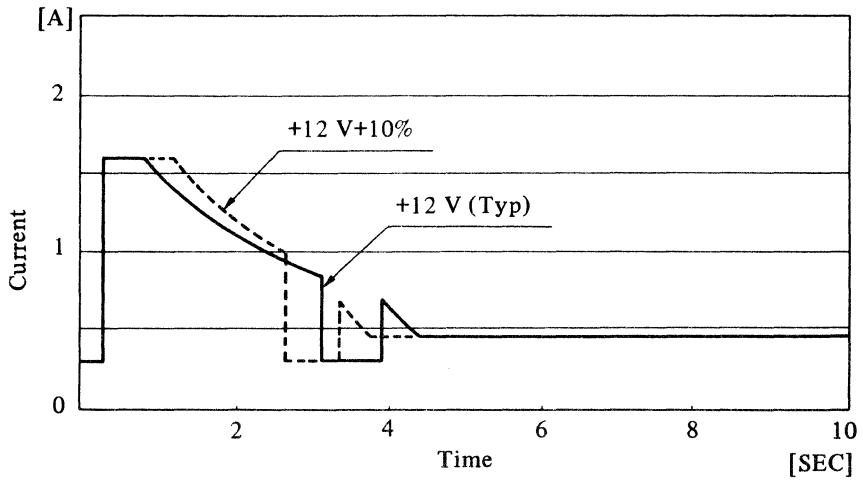
The above values are voltages at the power connector of the drive. Lower voltages will adversely affect the performance of the drive.

(3) Power consumption

Steady state 7.5 W

(4) Current waveform

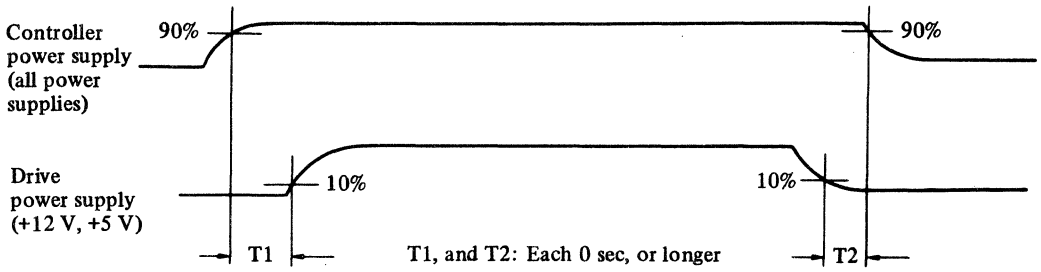
+12 V current waveform (for reference)



(5) Power on/off sequence

If the Write Gate signal from the controller is off before applying or removing power, the voltages (+12 V, +5 V) to the drive need not be sequenced. That is, recorded data will not be destroyed nor will mechanical or electric problems occur. To maintain the Write Gate signal in the off state at the time of drive power-on or -off, the basic sequence between the power supply of the controller and drive must be as follows:

(a) Basic sequence



Note:

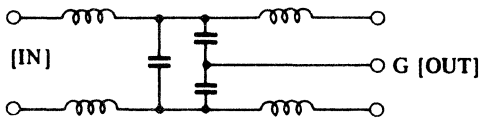
The power supplies of the drive (+12 V, +5 V) need not be sequenced.

(b) If the controller and the drive share a common supply and the Write Gate interface signal is determined only by +5 V, power sequencing is unnecessary. This is so because the +5 V level is monitored within the drive.

(6) Others

To eliminate AC line noise, a noise filter of the specifications given below should be incorporated in the AC input terminal of the drive power supply.

Attenuation characteristic; 40 dB or greater at 10 MHz
Circuit configuration; T type shown below is recommended.



1.2.4 Reliability

(1) Mean Time Between Failures (MTBF)

The estimated MTBF of this drive during its life time is 30,000 hours after an initial 3-month period.

Note:

The MTBF is defined as follows.

$$\text{MTBF} = \frac{\text{Operating time (hours)}}{\text{The number of equipment failures}}$$

Operating time is the total time duration during which the power is ON.

Failure of the equipment means failure that requires either repair, adjustments, or replacement. Mishandling by the operator, failures due to bad environmental conditions, power trouble, controller trouble, cable failures, or other failures not caused by the equipment are not included.

(2) Mean Time To Repair (MTTR)

MTTR is the average time taken by a well-trained service technician to diagnose and repair a unit malfunction. This drive is designed for a MTTR of 30 minutes or less.

(3) Service life

Overhaul of this drive is not required for the first five years.

(4) Power loss

Data will not be corrupted on the disk in the event of an abnormal power condition, unless a Write operation is in progress at the time of the event.

1.2.5 Error rate

Errors detected upon initialization and successfully replaced by an alternate record, are not included in the error rate.

(1) Recoverable error rate

A recoverable error is one which can be read correctly within 16 retries and should not exceed 10 errors per 10^{11} bits read.

(2) Non-recoverable error rate

Errors that cannot be recovered within 16 retries should not exceed 10 errors per 10^{13} bits read.

(3) Positioning error rate

The rate of positioning errors recoverable by one retry is 10 errors or less per 10^7 seeks.

(4) Media error

(a) Cylinder 0, Heads 0 ~ 7 are defect free.

(b) The number of defective sectors in the M222XD2 are as follows:

M2225D2 ..... maximum 25
M2226D2 ..... maximum 38
M2227D2 ..... maximum 51

(5) Media defect list

Media defects when shipping from the factory are listed on the MEDIA DEFECT LIST and this list is attached to each drive. The following figure shows an example of the MEDIA DEFECT LIST.

*** MEDIA DEFECT LIST ***

CUSTOMER: DATE: 87/08/25

MODEL: B03B-4815-B104A DE SERIAL NO. 000000

No.	CYLINDER	HEAD	POS/BYTES	LEN/BITS	SCT/032	PAGE-001
001	00EB (0235)	00 (00)	009F (00159)	00B (0008)	01A (026)	1
002	0115 (0277)	03 (03)	0120 (00288)	00B (0011)	00A (010)	1
003						
004						

Number of defective sector when 32-sector formatting; hexadecimal number (decimal number)

Length of defect (unit: byte); hexadecimal number (decimal number)

Position from index to lead bit of defect (unit: byte); hexadecimal number (decimal number)

Head address hexadecimal number (decimal number)

Cylinder address hexadecimal number (decimal number)

1.3 Cables

The recommended cable connector specifications are listed in Table 1.2.

Table 1.2 Cable connector specifications

Connector	Name	Spec. No.	Manufacturer
Cable A (34P)	Cable connector	FCN-767J034-AU/1 or 88373-3 or 3463-0001	FUJITSU AMP 3M
	Drive card edge	–	–
	Cable	455-248-34 or 171-34	SPECTRA-STRIP ANSLEY
Cable B (20P)	Cable connector	FCN-767J020-AU/1 or 88373-6 or 3461-0001	FUJITSU AMP 3M
	Drive card edge	–	–
	Cable	455-248-20 or 171-20	SPECTRA-STRIP ANSLEY
Power cable	Cable connector	1-480424-0	AMP
	Drive connector	68946	DUPONT
	Contact	170121-4	AMP
	Cable	AWG 18 (+5V, RTN) AWG 18 (+12V, RTN)	–

CHAPTER 2 INSTALLATION

This chapter describes unpacking, installation and cabling of the M222XD2.

2.1 Unpacking

The M222XD2 is packed in a carton. An exterior view of the carton is shown in Figure 2.1.

① Place the carton on a flat surface. Ensure that the top of the box, indicated by a "This Side Up" sign, is oriented correctly.

② Pull the drive out of the carton together with cushions. Handle the drive slowly and carefully, to prevent unnecessary shock.

③ Remove the cushions from the drive.

CAUTION:

When transporting, installing and maintaining the drive, do not shock or drop the drive, to prevent the heads and media in the DE from incurring damage. When transporting the drive, use only the specified carton.

2.2 Visual Inspection

After unpacking, check the following.

① There should be no cracks, rust or other damage.

② All parts should be firmly affixed, there should be no loose screw, etc.

③ The MEDIA DEFECT LIST should be attached.

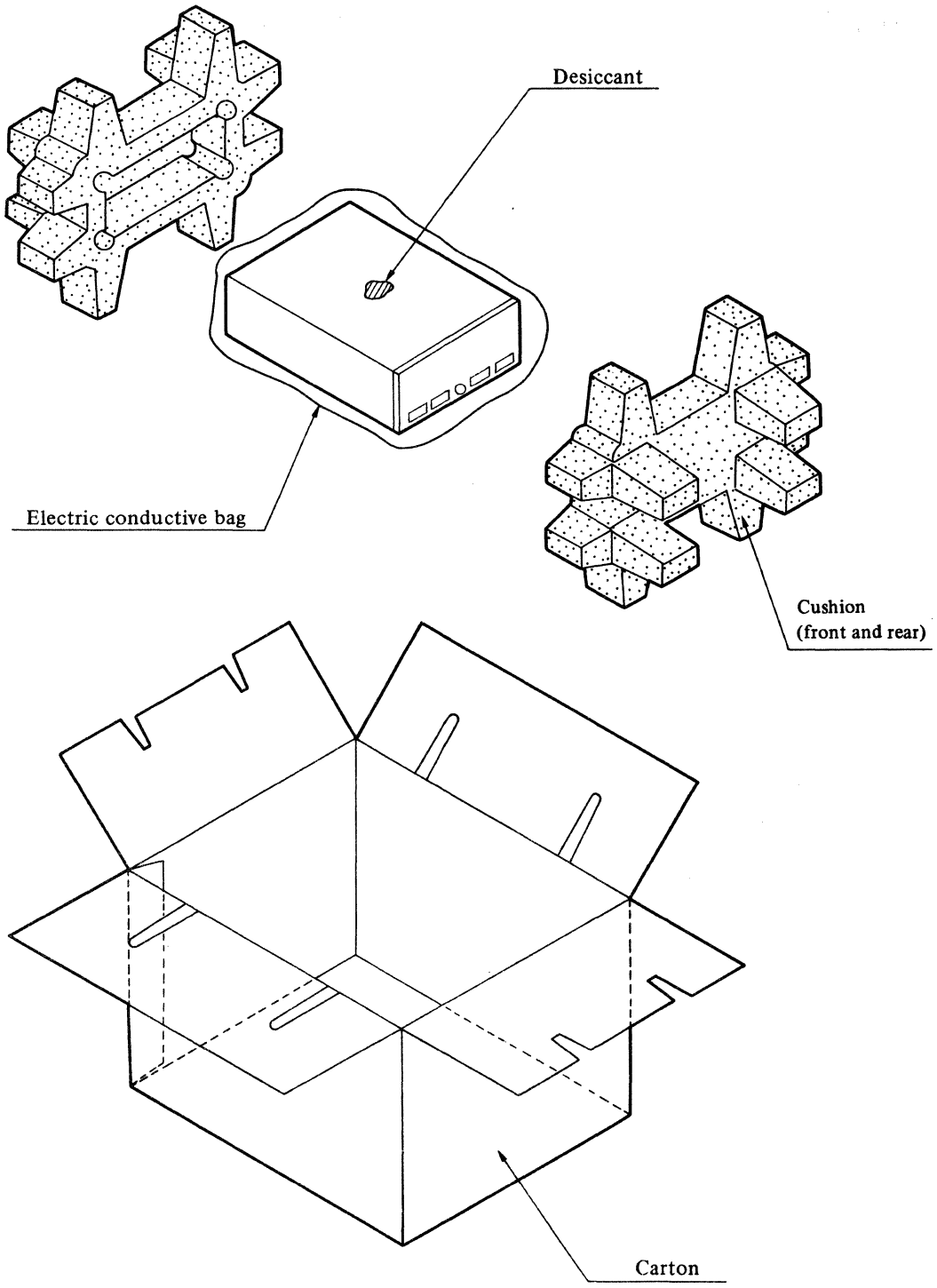


Figure 2.1 Exterior view of carton

2.3 Installation

2.3.1 Outer Dimensions

Figure 2.2 shows the outer dimensions and mounting dimensions.
All dimensions are in millimeters.

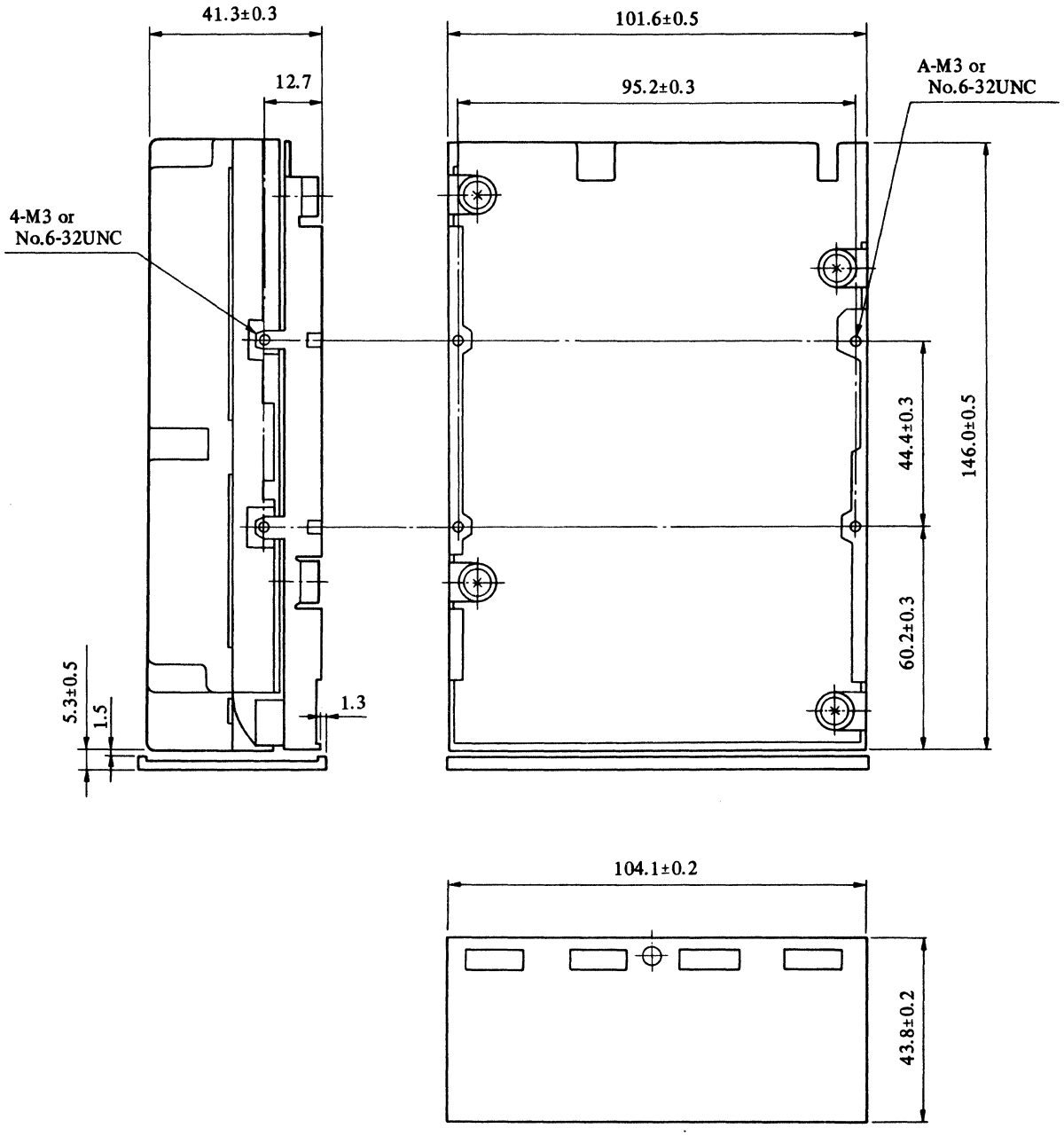


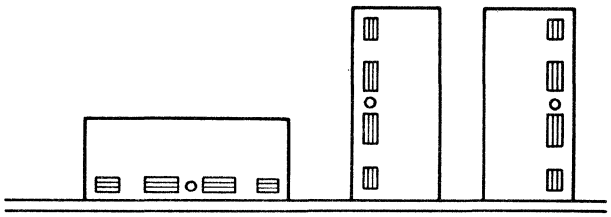
Figure 2.2 Outer dimensions

2.3.2 Notes on installation

(1) Installation directions

The drive may be installed as shown in the following figure.

In the horizontal position, the drive must be level to within 20 degrees and the PCB facing downwards. Vertically the drive must be true within 5 degrees and cannot be mounted end above end.

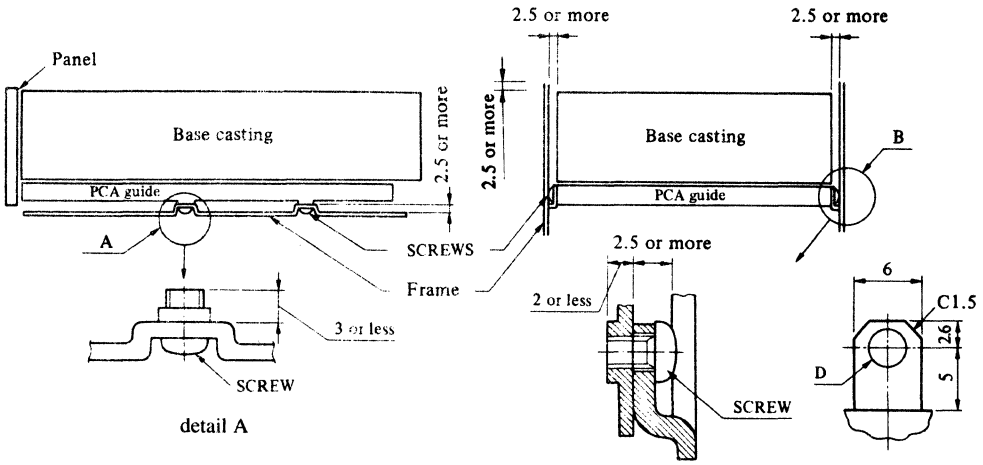


(2) Frame structure

When the drive is mounted with bottom threads, the embossed frame can be used as shown below (detail A). However, when the drive is mounted with the side threads, the frame should be designed according to detail B as shown below.

CAUTION:

Screw lengths for mounting drive differs, according to mounting method, it is important to use correct length of screw.



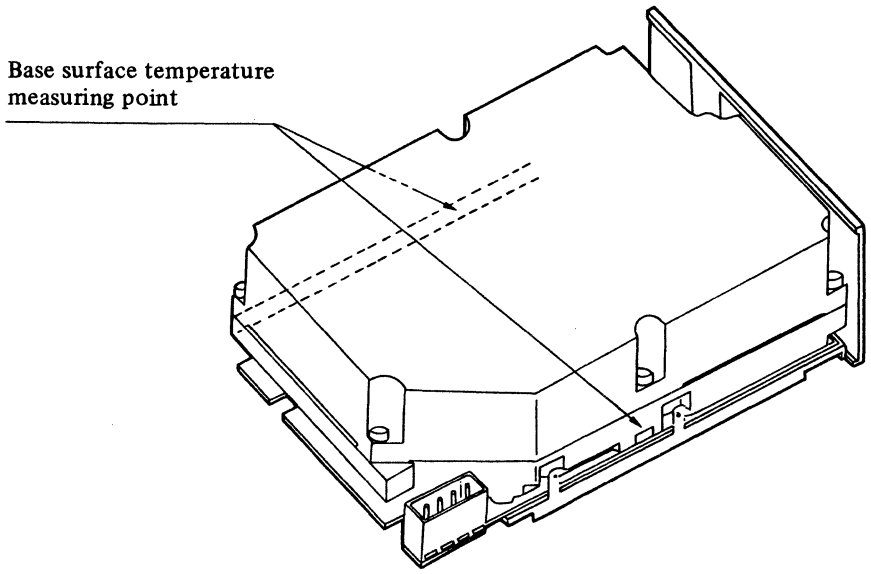
Screw	D (mm)
M3	3.6
No.6–32UNC	4

(3) Ambient temperature

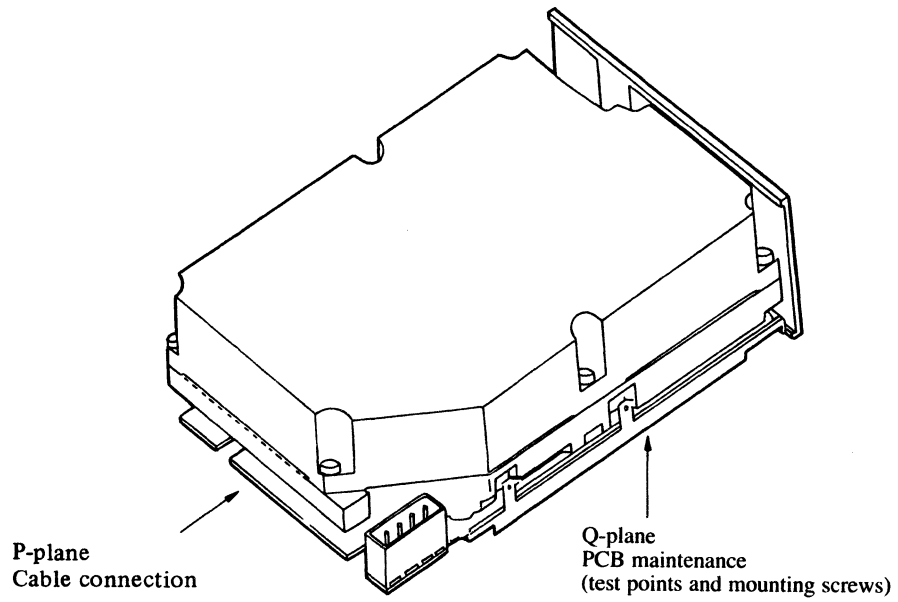
The operating temperature range of the drive is specified at a distance of 3 cm from the drive.

The operating temperature must not exceed 45°C at any time in operation. To satisfy this condition, the base surface temperature in the Ready condition must not exceed 60°C.

The PCB should be cooled with proper air circulation in the cabinet.



(4) Service area



2.4 Cable Connection

The drive is interfaced to a system through three connectors.

2.4.1 Drive connectors location

Figure 2.3 shows the location of A and B cable edge connectors and power connector.

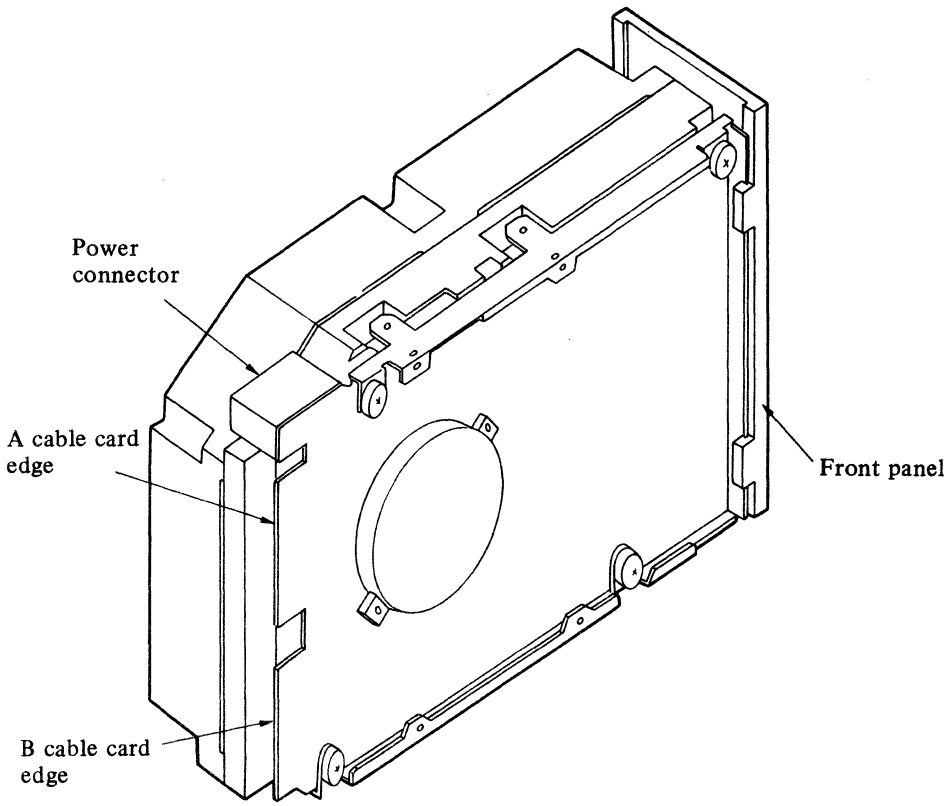


Figure 2.3 Drive connectors

2.4.2 Single drive connection

Figure 2.4 shows the connection of single drive to its controller.

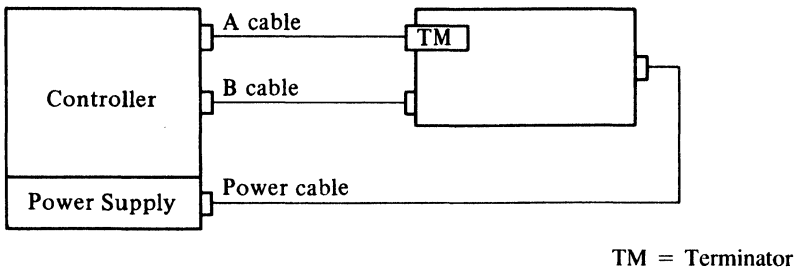


Figure 2.4 Single drive connection

2.4.3 Multiple drive connection

(1) Daisy chain connection

Connection of the drives to a controller is shown in Figure 2.5. The A Cable (control signals) must be connected in series and the B Cable (R/W signals) in parallel. The termination for the control signals must be performed only on the last drive in the chain.

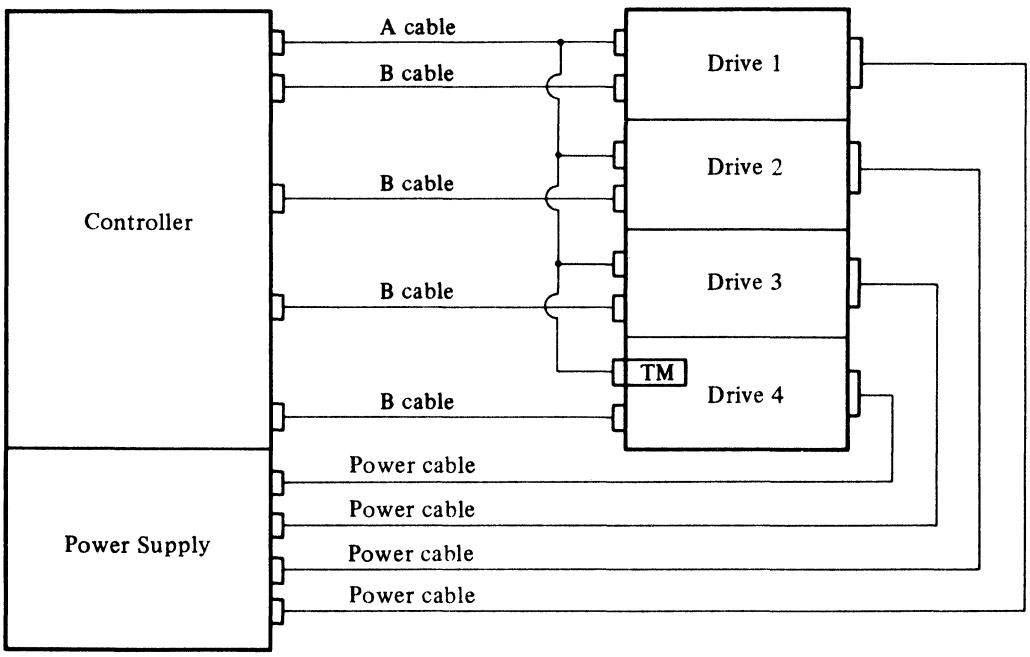


Figure 2.5 Daisy chain connection

(2) Radial connection

Connection of drive to its controller is shown in Figure 2.6. The A Cable (control signals) and the B Cable (R/W signals) must be connected in parallel. The termination of control signal must be performed at the all drives.

See paragrah 3.4.5 for A and B cable length specification.

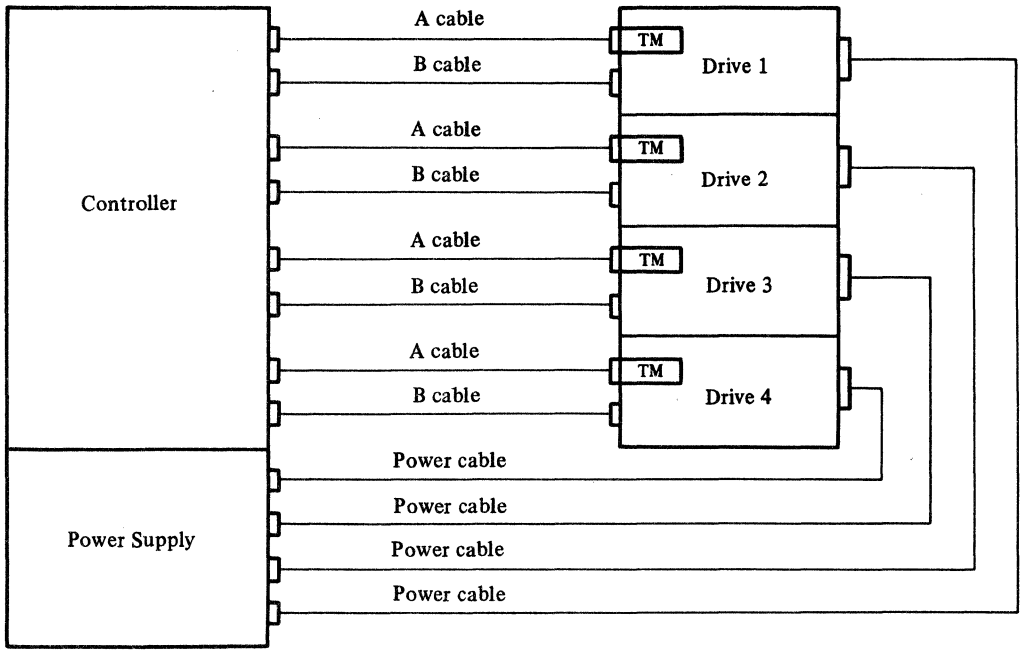
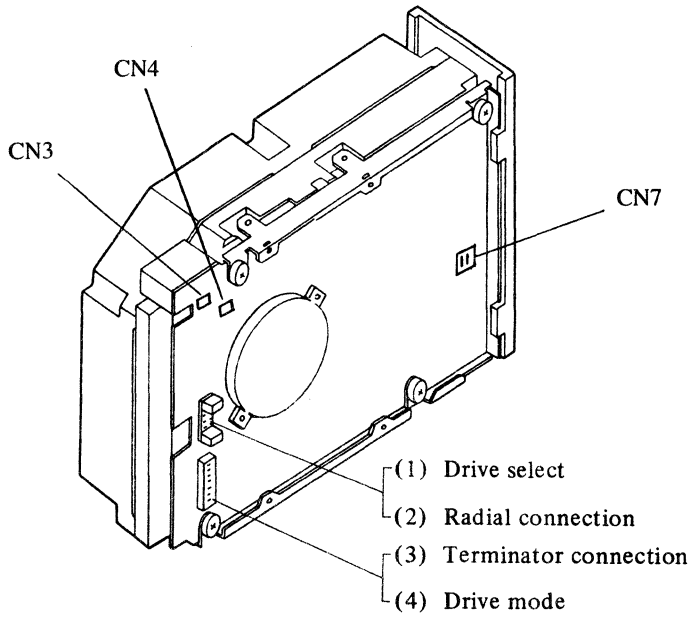


Figure 2.6 Radial connection

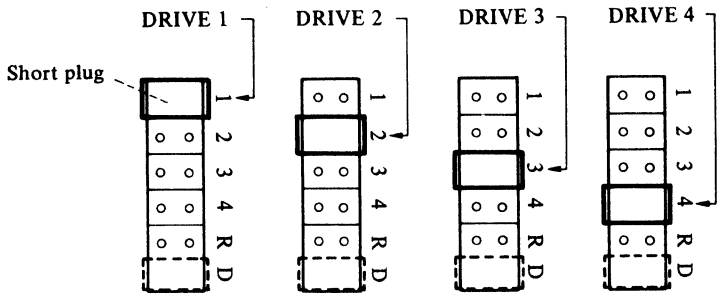
2.5 Switch Setting

The functions and assignment procedures of a switch are described below.



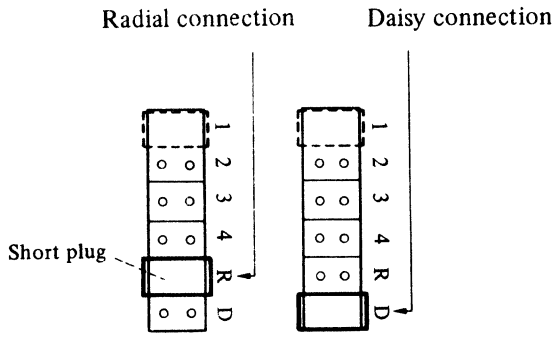
(1) Drive select

Set the drive number (1 to 4) with the short plug as follows.



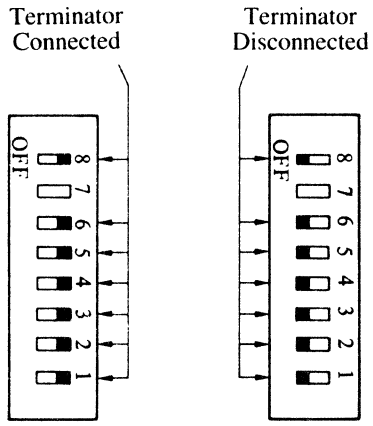
(2) Radial/daisy connection setting

Set either radial or daisy connection as follows.



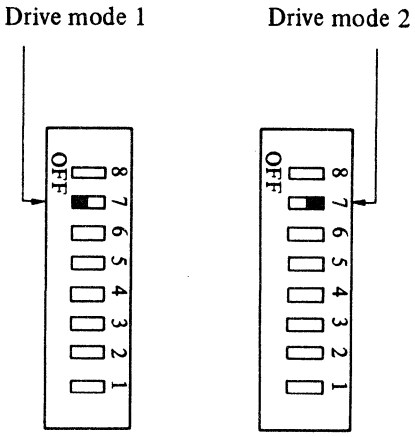
(3) Terminator connection

When all switches other than SW7 are set to ON, the terminator is connected.
When all switches other than SW7 are set to OFF, the terminator is not connected.



(4) Drive mode selection

Drive mode 1 is selected when SW7 is OFF and Drive mode 2 is selected when SW7 is ON.



See subsection 3.4.6 and 3.4.7 for description of mode 1 and mode 2.

(5) CN3 Write Enable

Removal of this short plug will inhibit writing data on the drive. (This facilitates an external write protect switch.)

(6) CN4 RINH signal

This short plug enables the internal "Read Inhibit" signal "RINH" to be presented on pin 5 of the data cable.

(7) CN7 external LED connector

This connector is provided to allow connection of an external "Drive Selected" LED.

CHAPTER 3 THEORY OF OPERATION

This chapter consists of 3 sections:

① Mechanical parts

② Recording media format

③ Interface and electrical control section

3.1 Mechanical Parts

The drive consists of disks, heads, spindle motor, actuator, cover, breather filter, recirculation filter, base, and control PCA.

Figure 3.1 shows the outer view of the drive.

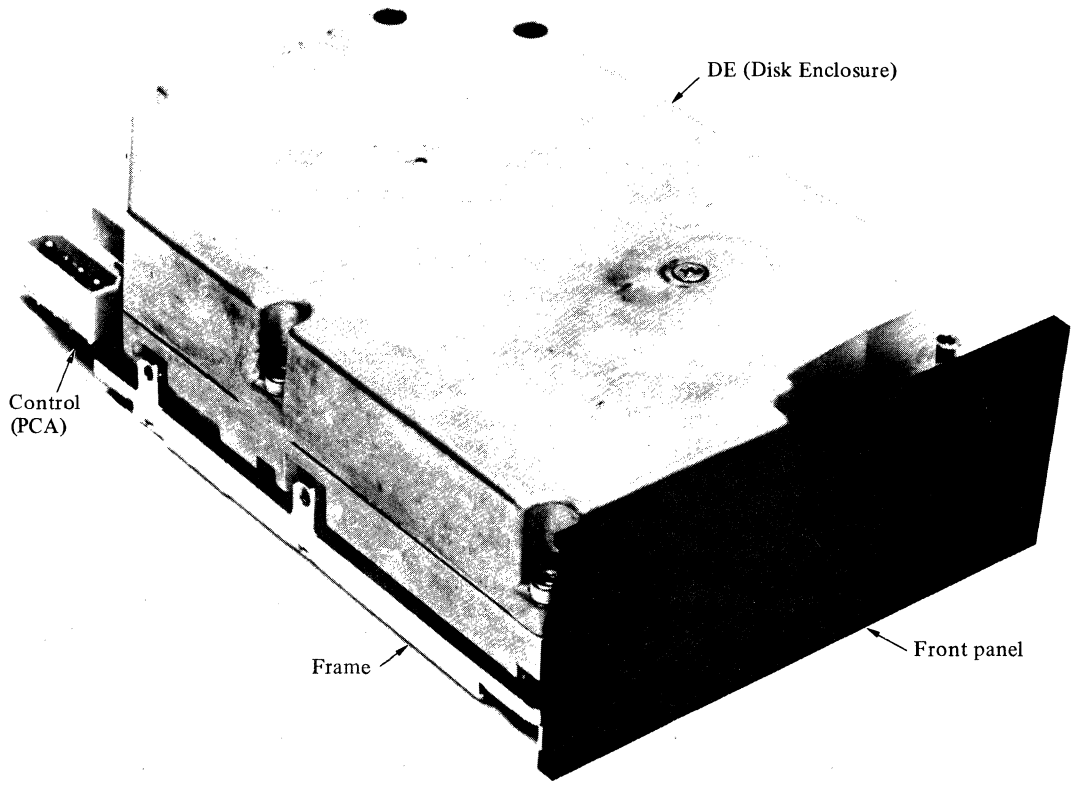


Figure 3.1 Outer view

(1) Disks

Disks are 95 mm in outer diameter and 25 mm in inner diameter and are coated with a special lubricating material. M2225D2, M2226D2 and M2227D2 have 2, 3 and 4 disks respectively. Durability is designed for over 10,000 start and stop cycles.

(2) Heads

The whitney heads are in contact with the disks when the disks are stationary, but automatically float when disk rotation reaches a certain speed. The number of heads (R/W) is four in the M2225D2, six in the M2226D2, and eight in the M2227D2.

(3) Spindle motor

The disks are turned by a direct-drive DC motor. The motor attains a very precise rotational speed: 3600 rpm, ±1%. This precision is achieved through a feedback circuit which includes a Hall IC, mounted within the motor assembly.

(4) Actuator

This assembly consists of an optical encoder motor, band actuator, and head arm.

The carriage working with the special drive circuit, gives increased reliability and a very short average positioning time of 35 ms.

3.2 Air Circulation

The heads, disks and actuator are sealed inside a cover to shut out any contamination. This head disk assembly has a closed-loop air recirculation system using the blower effect of the rotating disks to continuously cycle air through the recirculation filter. This filter traps any dust generated inside the enclosure. To prevent negative pressure in the vicinity of the spindle when the disks begin rotating, a breather filter is attached. This breather filter also equalizes the internal air pressure with the atmospheric pressure due to surrounding temperature changes.

3.3 Recording Media

Servo information is recorded on part of the data surfaces in this drive. The drive control circuit samples this servo information to position the heads on a data track precisely.

The data surface consists of 615 cylinders for data recording. Cylinder 0 is on the outermost radius of the disk and cylinder 614 is on the innermost radius.

3.3.1 Track format

The soft sector format, is the same as that for floppy disk drive units. Each sector consists of an identify (ID) field (for checking that the correct sector is read) and a data field for actually recording the data.

The sector format is determined by the controller. This subsection explains the format written at the factory.

A sector interleave format (factor = 4) is set at the factory. A track has 32 sectors.

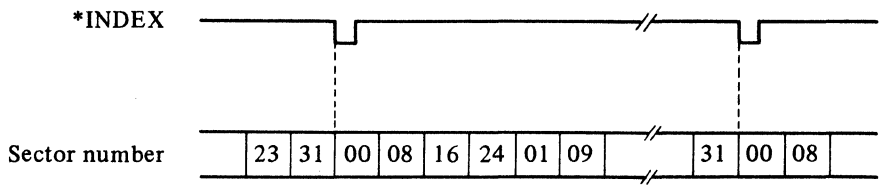
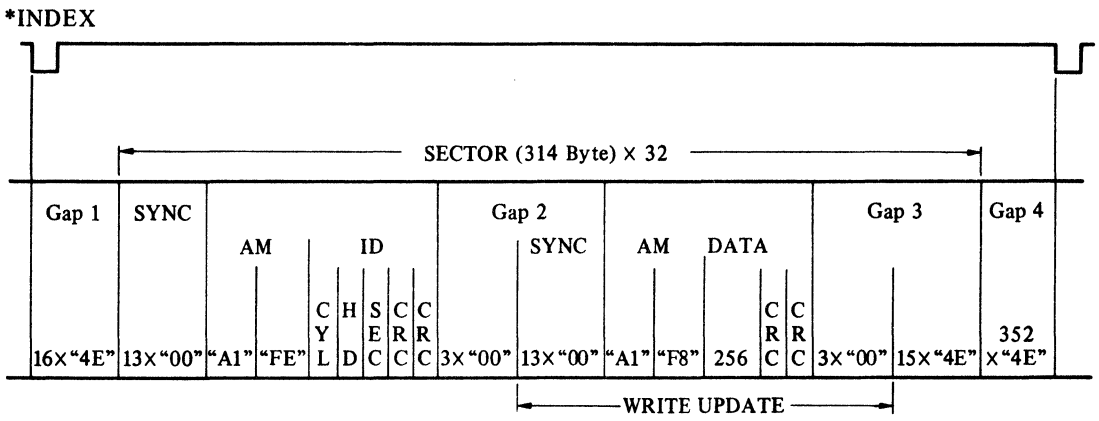


Figure 3.2 Sector interleave format



Notes:

1. The track capacity varies according to the motor rotation fluctuation. The nominal track capacity is 10,416 bytes.
2. The nominal capacity of gap 4 is 352 bytes.
3. 16 × "4E"
   - Indicates the hexadecimal bit pattern.
   - Indicates the number of bytes.

Figure 3.3 Track format

3.3.2 Format configuration

(1) Gap 1: ''4E''

Absorbs the index burst fluctuation. A 16-byte ''4E'' pattern is written in this gap.

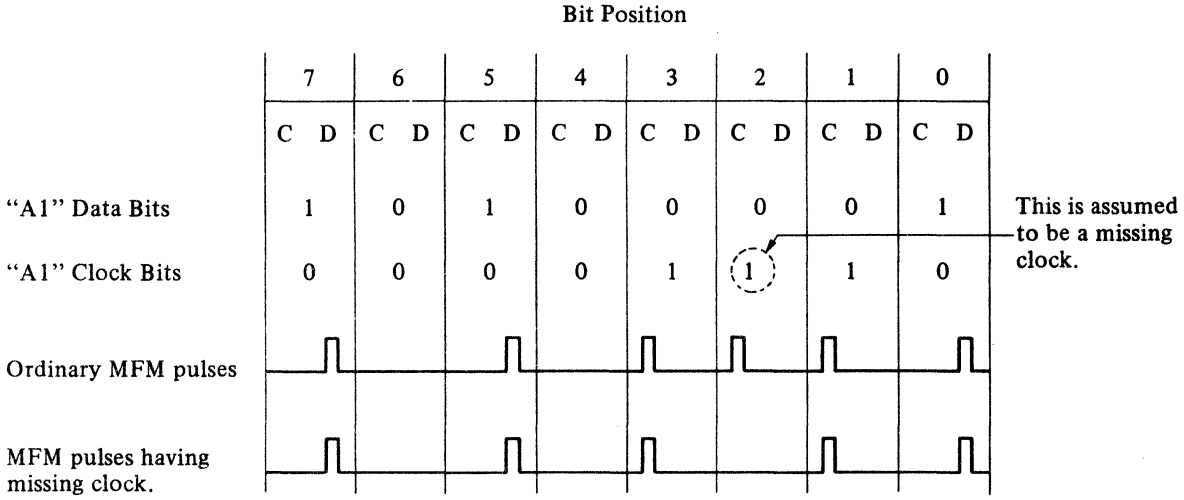
(2) Sync: "00"

The VFO synchronization area for reading the ID and data fields. A 13-byte ''00'' pattern is written in this field.

(3) Address Mark (AM): 2 Bytes

ID Field : "A1" "FE" (*)
Data Field : "A1 "F8"

Identifies the header part of the ID and data fields.
An ''A1'' pattern is written in the following missing clock format, to detect the AM:



(*) The data pattern of byte 2 succeeding the ''A1'' pattern of AM is as follows:

ID field: "FE" at cylinders 0 ~ 255

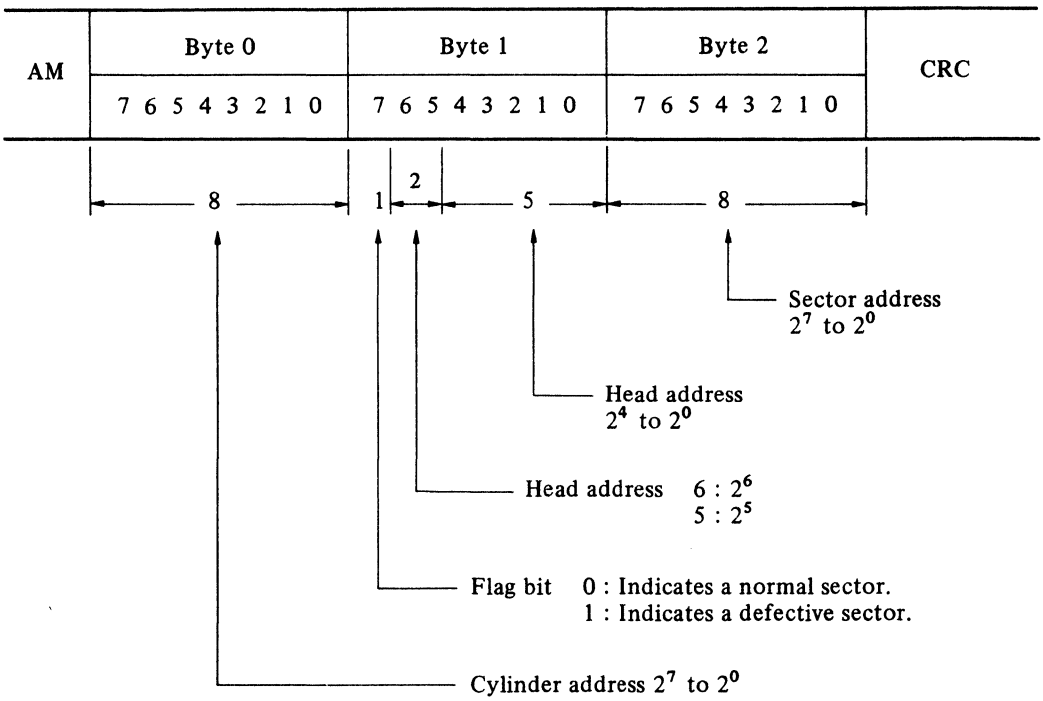
"FF" at cylinders 256 ~ 511

"FC" at cylinders 512 ~ 614

Data field: "F8"

(4) Identify Field (ID): 7 Bytes

The ID field consists of seven bytes, including AM and CRC. The three bytes other than AM and CRC have the following bit configurations:



(5) CRC field: 2 Bytes

Error detection code including AM (A1 pattern). The polynominal is as follows:

$$X^{16} + X^{12} + X^5 + 1$$

Note:

The CRC initial value is FF.

(6) Gap 2: 16 Bytes

Lead in area for reading/writing the data field. The data pattern for synchronizing the variable frequency oscillator (VFO) is "00".

(7) Data field: 256 Bytes

The user area follows the Data Address mark pattern of "A1F8" and in turn is followed by a 2 byte CRC field.

(8) Gap 3: 18 Bytes

Consists of 3-byte "00" patterns and 15-byte "4E" patterns for absorbing motor rotation fluctuation.

(9) Gap 4: 352 Bytes (nominal)

The area for absorbing motor rotation fluctuation used when formatting all sectors in a track at the same time. This area consists of 352-byte "4E" patterns (nominal rotation number).

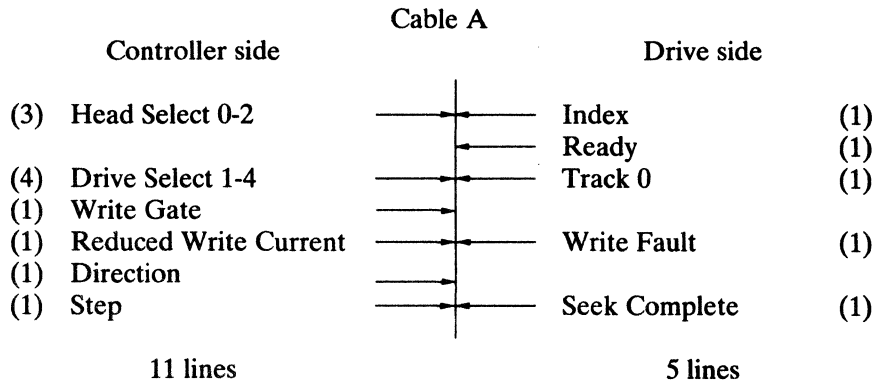
3.3.3 Write precompensation

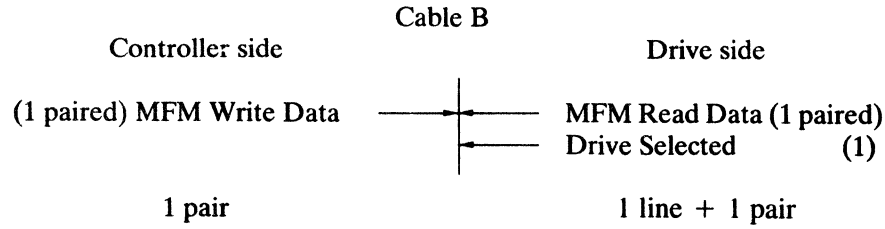
Write precompensation is not necessary. (Post compensation is automatically handled inside the drive logic by changing the read channel characteristics for the inner and outer cylinders.)

3.4 Interface

This section describes the physical and logical conditions of the signals transferred through the interface between the drive and the controller. The timing is specified at the driver/receivers of the drive.

3.4.1 Signal lines





3.4.2 Input signals

(1) Head Select 0 to 2

These signal lines are used to select one of the data heads in the drive.

(2) Drive Select 1 to 4

These signal lines are used to select one of four drives in a multi-drive configuration and validate the input/output signals of the selected drive.

(3) Direction

This signal line is used to determine the seek direction of the data heads when the step pulses are sent to the disk drive. When this signal is true, seek is performed inward (away from Track 0); when false, seek is performed outward (toward Track 0).

(4) Step

This signal moves the data heads one track per pulse in the direction indicated by the Direction signal. There are two stepping modes as follows:

(a) The drive supports step pulse rates between 5 kHz and 3 MHz and will automatically select either a ''full buffered'' or ''semi buffered'' mode of seek operation. In the full buffered mode, the actuator will not move until all of the step pulses have been received. At a lower step pulse rate, the actuator will start the seek after 12 step pulses have been received and before the last of the pulses have arrived. This is the semi-buffered seek mode and functions this way in order to maintain a higher average seek time.

(Step rates below 5 kHz are prohibited.)

(b) Return to zero mode

When 615 or more step pulses are issued, the data heads will move to Track 0.

If the controller does not use this mode, the recalibrate function should be performed per the following procedure.

① Set the Direction to false.

② Send one step pulse.

③ Wait until the Seek Complete signal is true.

④ Continue the procedure until the Track 0 signal is true.

(5) Write Gate

This signal line enables the write current to the selected data head in the drive. When this signal is false, the Read Data from the disk is transmitted to the interface.

(6) Reduced Write Current

This signal line is not used in this drive.

(7) MFM Write Data (balanced transmission)

This signal is a differential signal, and is used to determine the flux change point of the data bit written on the disk.

When +MFM Write Data goes more positive than −MFM Write Data while Write Gate is active, a flux change occurs.

During a Read, this signal should remain inactive (+MFM Write Data should be more negative than −MFM Write Data).

3.4.3 Output signals

(1) Index

This is a pulse signal transmitted once for every revolution of the disk in the selected drive.

(2) Ready

This signal is active or true when the voltages are within specification and the spindle motor has reached nominal speed. This signal is true approximately 15 seconds after power on.

(3) Track 0

This indicates the data head is stopped on track 0.

(4) Write Fault

This indicates that one of the following abnormal states occurred during writing.

(a) Either +5 V or 12 V dropped below specification.

(b) Write current was not applied to the head while Write Gate was enabled.

(5) MFM Read Data (balanced transmission)

This signal is a differential signal and is used to send the Read Data bit from the disk to the host side. When the Write Gate is inactive, the point which indicates +MFM Read Data goes more positive than −MFM Read Data represents a flux reversal on the track of the selected head.

(6) Seek Complete

This indicates that the selected data head is positioned at the requested track. This signal includes the settling time of the head, and when it is true, read/write operations are enabled.

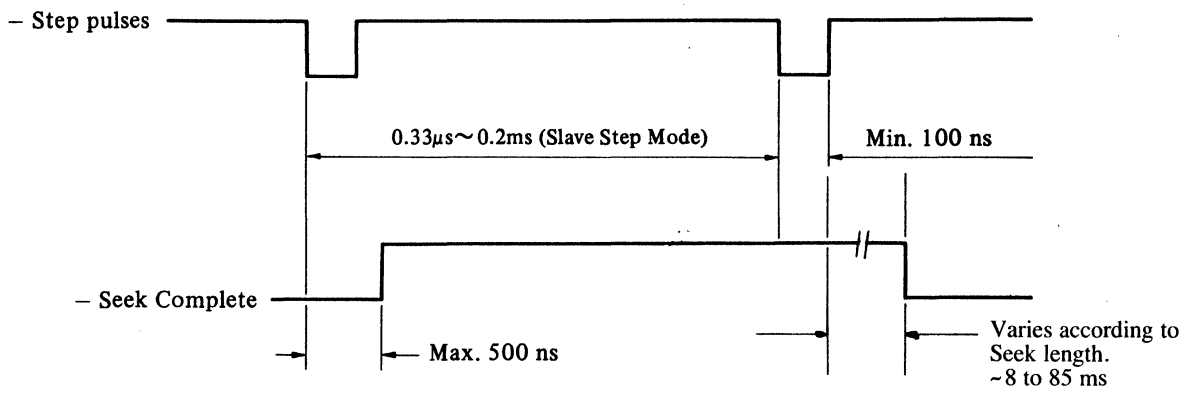
(7) Drive Selected

When the Drive Select 1-4 signals match the Drive Select Short Plugs on the drive side, the drive is selected.

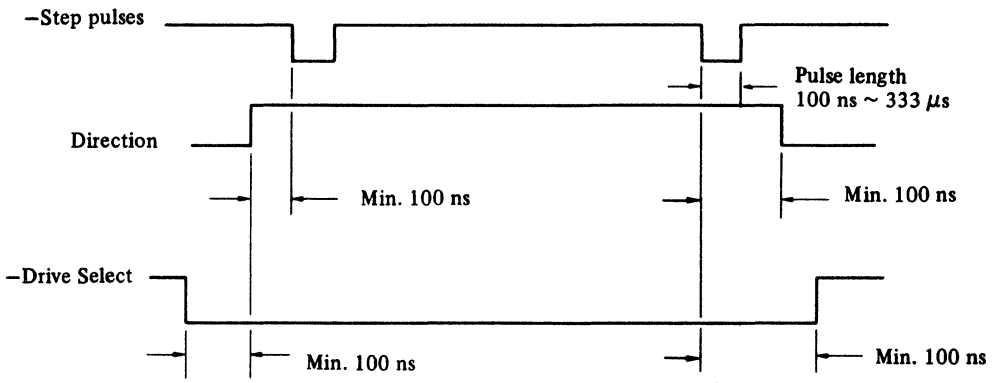
3.4.4 Timing Specifications

(1) Seek timing

(a) Step/Seek Complete relationship

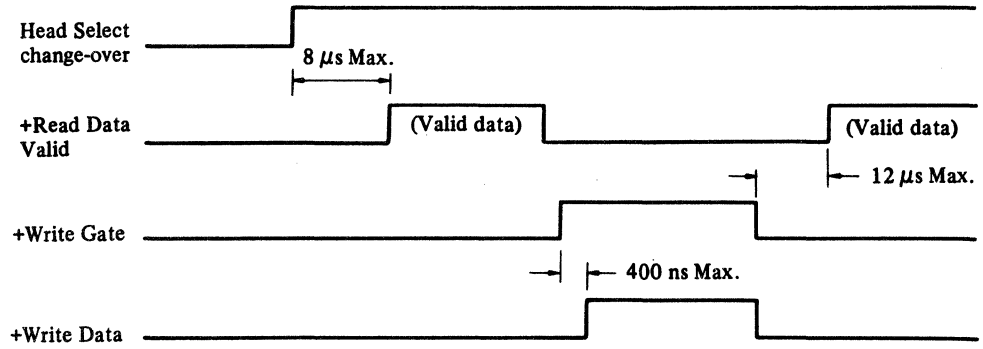


(b) Step/Direction and Drive Select relationship

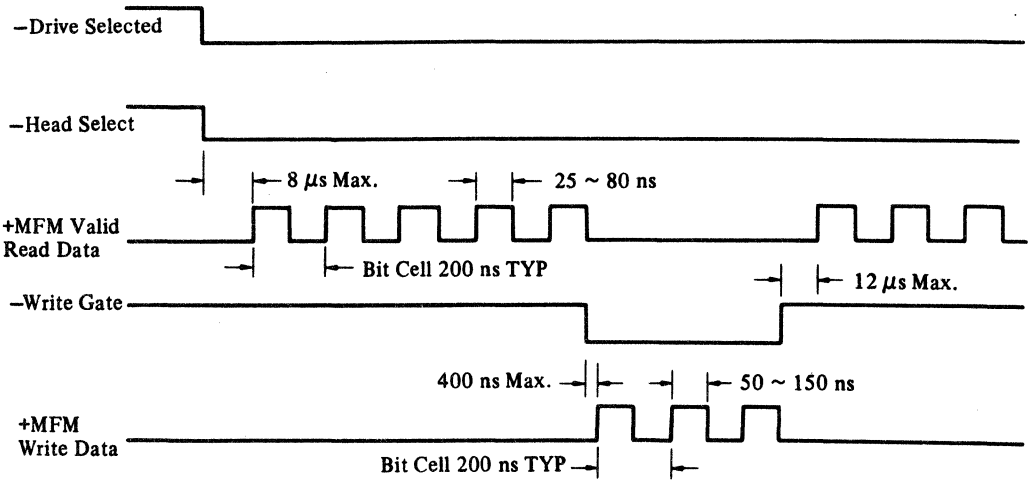


(2) Write/Read Data timing

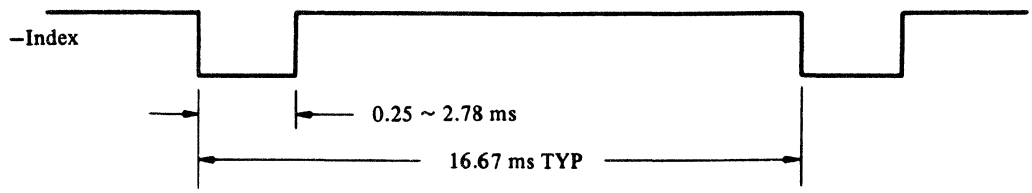
(a) Head change-over timing



(b) Read/Write Data timing



(3) Index signal timing



3.4.5 Driver/Receiver

The interface signals are terminated as in Figure 3.4. The total control cable length in a multi-drive configuration should not exceed the specification. (6 metres)

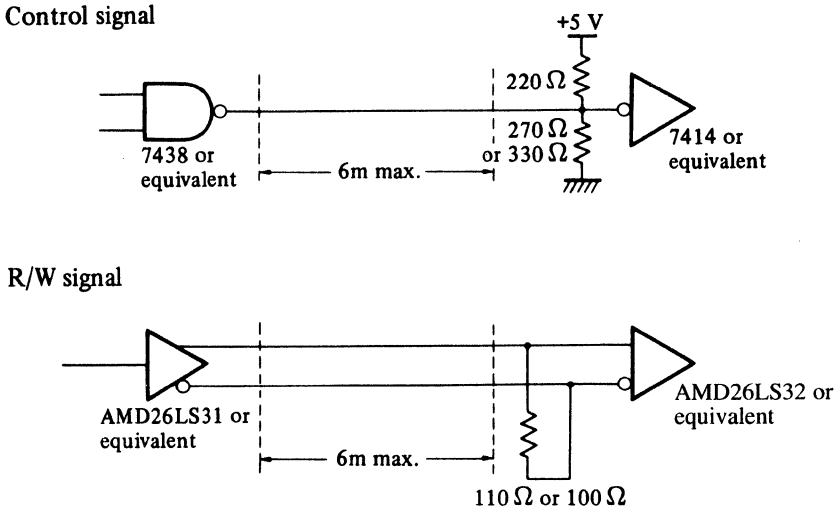


Figure 3.4 Driver/Receivers

3.4.6 Drive Mode

During operation the drive will automatically calibrate its optical cylinder reference (encoder) to fixed servo cylinders on the disk. This servo calibration, which is used to adjust for thermal changes, occurs during normal seek operations at predetermined intervals. In this manner, servo calibration is transparent to the drive controller and will result only in an occasional longer than average seek time.

In the event that servo calibration becomes necessary but no seek operation has been issued for a period of time, the position of the drive mode switch (SW7) determines what action will be taken.

① Drive mode 1

Drive mode 1 can only be used if the controller operations meet the two following conditions:

- If the drive is not being accessed, the drive select signal is not active.
- When the drive select signal is activated to access the drive, the controller must verify or wait for an active Seek Complete status.

In this mode, servo calibration is automatically performed while the drive is not selected. During calibration, the Seek Complete signal will not be active and the controller must verify this status line after selecting the drive.

(2) Drive Mode 2

Drive mode 2 is the factory set mode of operation and must be used if the controller does not meet the requirements of mode 1 operation.

In this mode, servo calibration is automatically performed regardless of the drive selection status. During calibration, the Read Data and Index signals will not be active and the Seek Complete signal will remain valid.

3.4.7 Details of Drive Mode

(1) Drive Mode 1

① Timing of compensation data renewal (Sampling seek)

The drive has an interval timer. This interval timer is preset, a value which depends on the elapsed time from power-on.

The renewal operation for the compensation data is made in the following two ways.

- A Seek instruction, (STEP pulse) is issued and the interval timer has overflowed.
- Drive Select is false when the interval timer overflows.

A timing chart of the renewal operation for the compensation data is as follows.

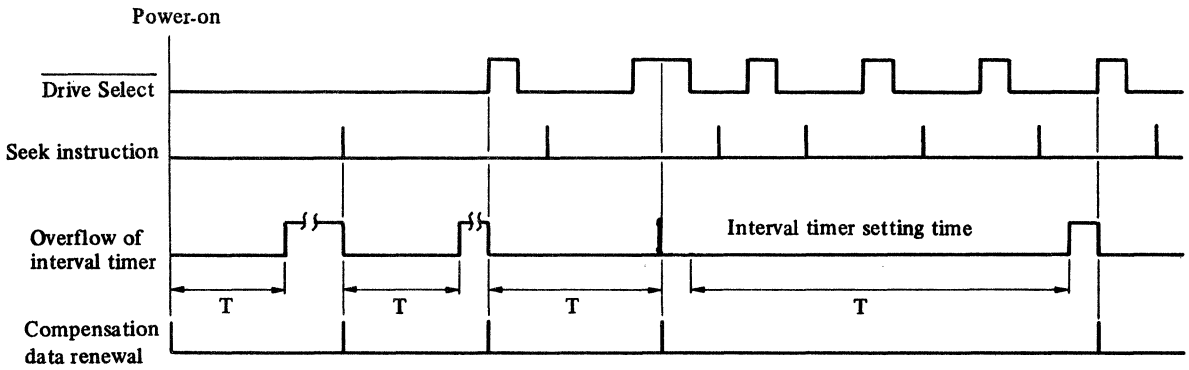


Figure 3.5 Timing of compensation data renewal (Drive Mode 1)

② When the interval timer overflows it may take up to 30 microseconds to check the status of the drive select line and then up to a further 30 microseconds to commence the internal seek operation. If within this time frame the drive select signal is asserted, then seek complete will be driven on the interface, up to 30 microseconds, until it is negated by the internal seek compensation data renewal operation.

When the host controller asserts the drive select signal, it must wait a minimum of 30 microseconds before checking if seek complete is true before initiating read/write operation. When the drive is deselected, it must remain deselected for a minimum of 30 microseconds, otherwise the internal compensation data renewal operation cannot commence.

If the timer overflows when the drive is selected, then the drive checks the condition of the select status, (selected) and then waits for a step pulse from the controller, to initiate the compensation data renewal seek.

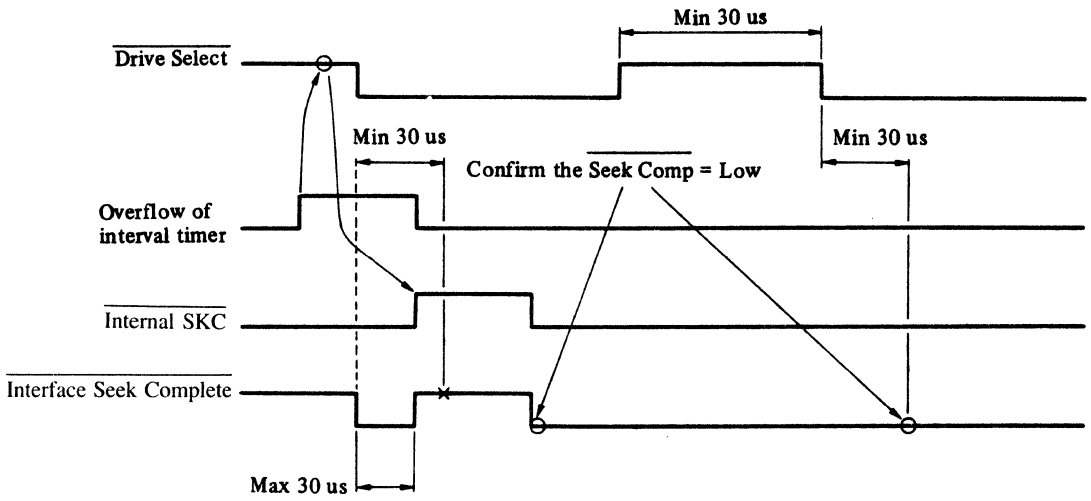


Figure 3.6 Drive Mode 1 timing

(2) Drive Mode 2

① Timing of compensation data renewal (Saving seek)

The drive has an interval timer. The interval timer is preset, a value which depends on the elapsed time from power-on.

The renewal operation of the compensation data is made when a Seek instruction (STEP pulse) is issued after the interval timer overflows.

② Read Data stop timing

If the seek instruction is not issued during five timeouts of the interval timer, then Read Data and Index signals are stopped, the internal seek is performed, compensation data is renewed, and then Read Data and Index signals are sent again. The recalibration or seek instruction (error recovery process) from the controller is executed after the internal seek.

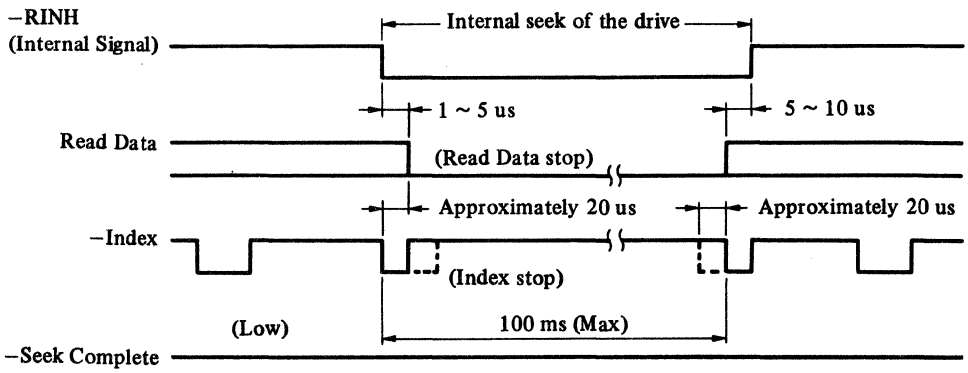


Figure 3.7 Read data stop timing

③ Step instruction during renewal of compensation data

When the retry instruction (step instruction) is issued from the controller, during internal seek operation, the retry instruction (step instruction) is executed after the internal seek.

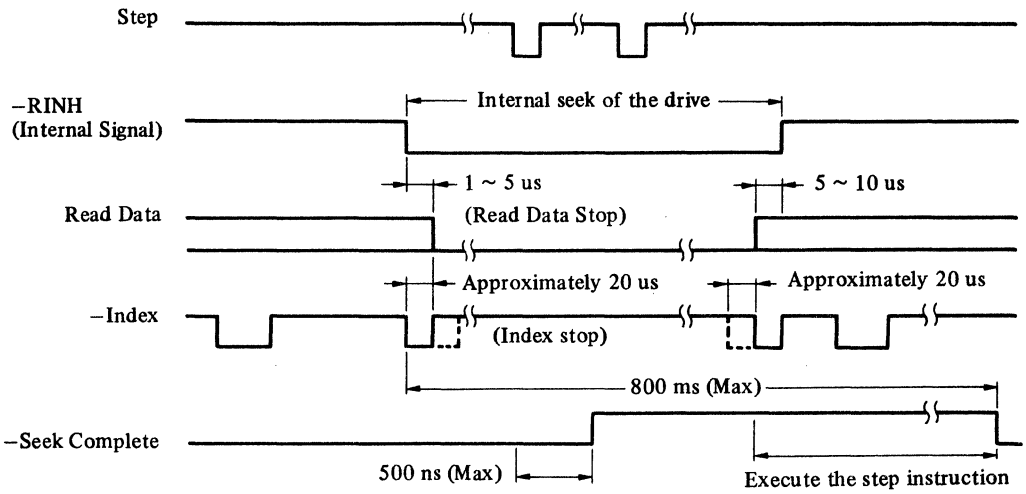


Figure 3.8 Step instruction during renewal of compensation data

④ Write instruction during renewing compensation data

When the write instruction (Write Gate: True) is issued during an internal seek operation, the Write Fault becomes true.

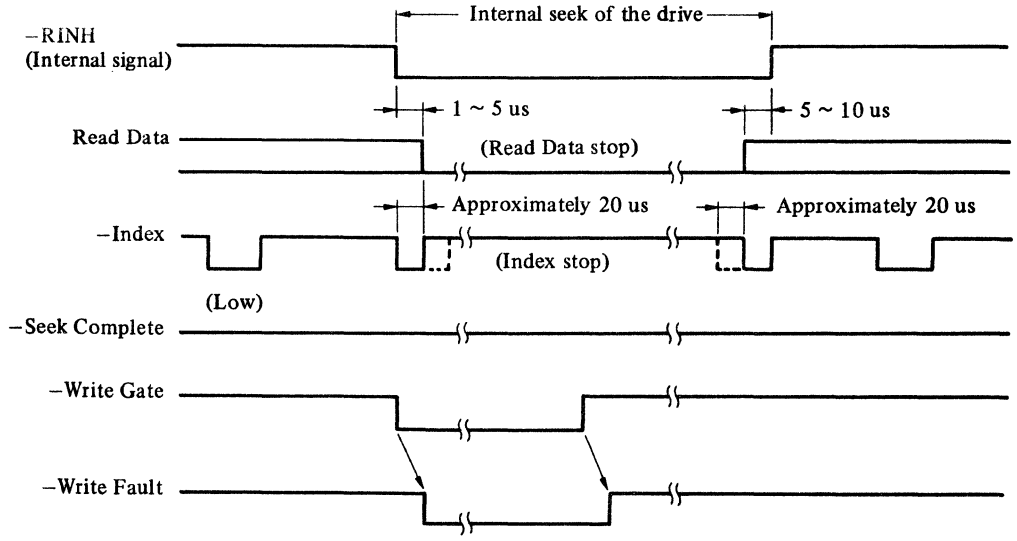


Figure 3.9 Write instruction during renewal of compensation data

3.5 Electrical Control Section

The M222XD2 is controlled by a MPU (Microprocessor, Intel 8031) and the sequencing program stored in the EPROM. This section explains the operation of the M222XD2 using the block diagram and the flowchart following.

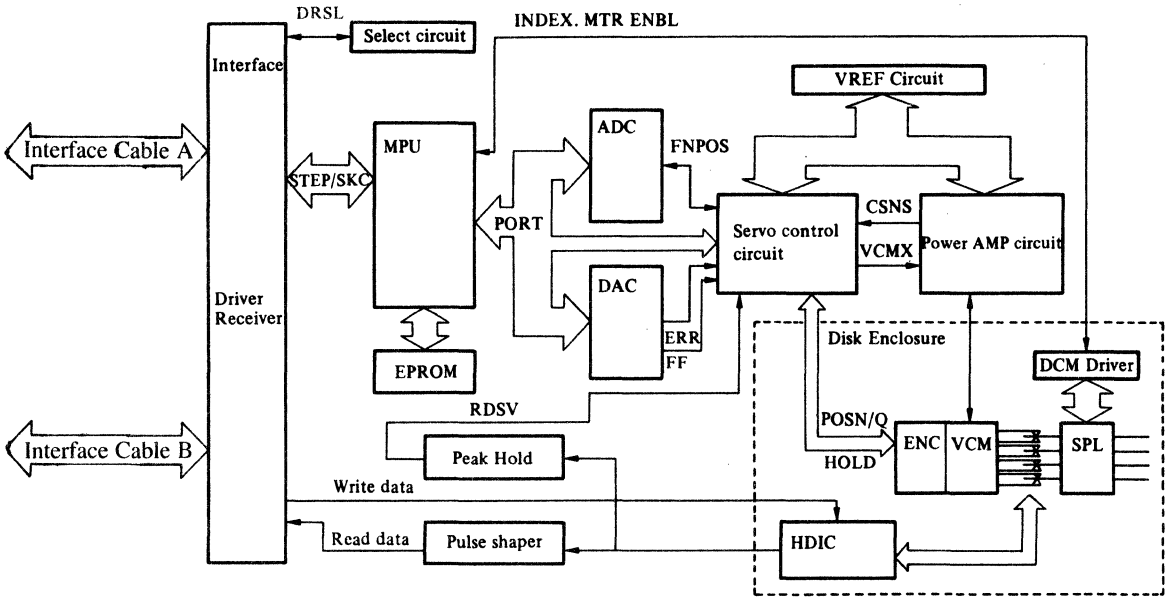


Figure 3.10 MPU control system block diagram

3.5.1 Sequence

Figure 3.11 shows the flowchart from power-on, to drive ready and the next Seek instruction sequences.

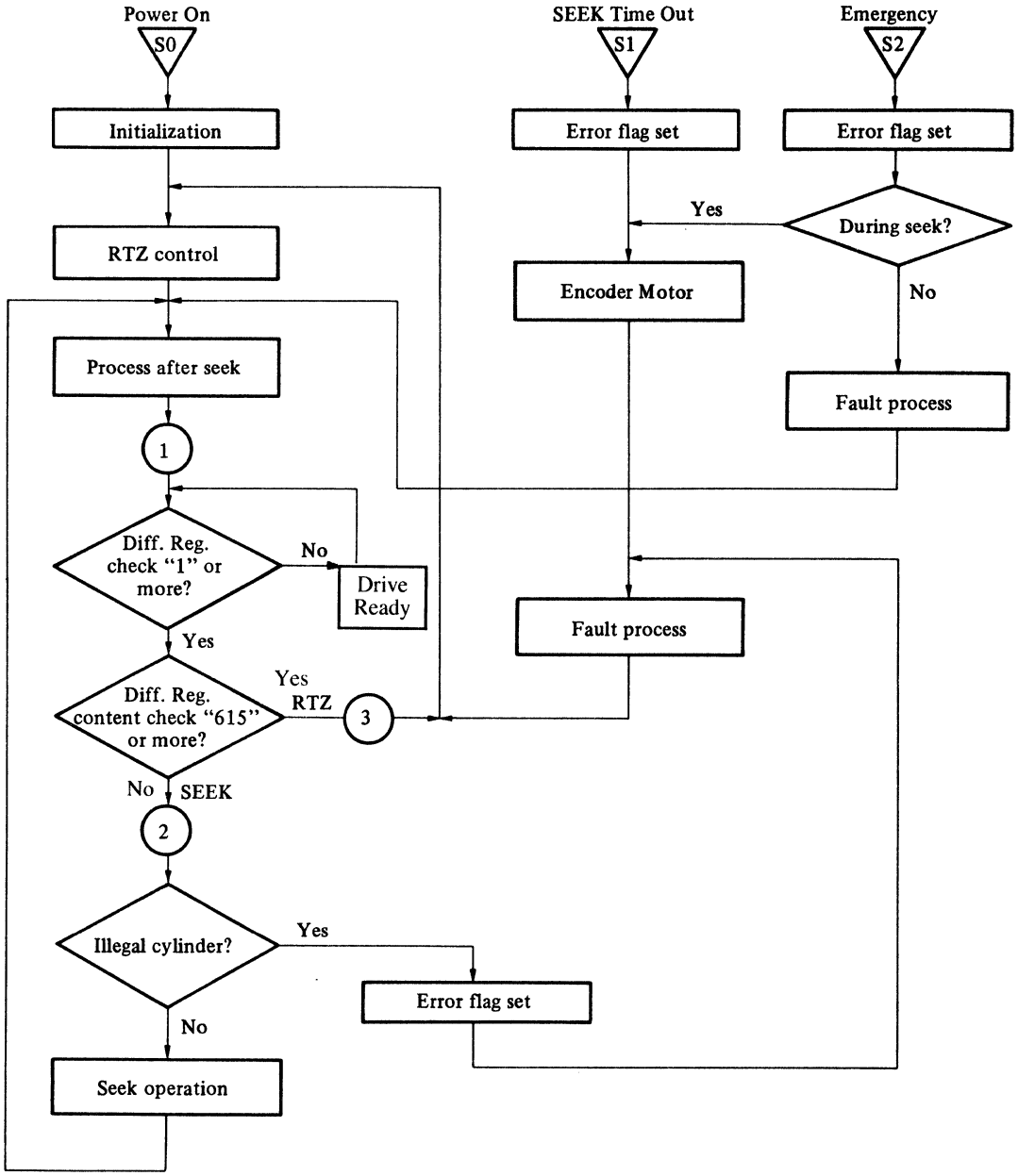


Figure 3.11 Control flowchart

As shown in Figure 3.11, on first powering on, an initialization sequence begins (zero-clearing each memory and register and RTZ initial seek). After the RTZ operation, several processes (Ready, SKC and Track 0 process) are performed and the flow enters into the routine indicated by ①. The Difference register check is idling and awaits the seek instruction from the controller. As mentioned in the Interface section, this register stores the number of step pulses (actually difference value) in slave mode, and sends it to the MPU. If that number is equal to or more than 615, the seek instruction is converted into a RTZ instruction ③. If less than 615, it is processed as a seek instruction ②.

This flowchart shows the basic operation. When a time out or emergency condition occurs the flow enters an abnormal process routine.

The MPU is not involved in the read/write operation directly.

3.5.2 Power-on sequence (initialization)

(1) When the +5 V power is turned on, the MPU begins to operate and performs the following.

- Resets each register in the MPU
- Resets the servo control register
- Resets each sequence register
- Resets each status register

The Motor Enable signal in the port register in MB63513 is set, and the spindle motor control circuit begins to operate. To time, the spin up, the 30 seconds counter is set in the MPU. The MPU checks rotational speed by observing the Index signal from the spindle motor.

After Speed OK becomes true, approximately 1 second later, the RTZ Initial Seek Sequence starts. If the Initial Seek is not completed within 30 seconds, after powering on, the MPU stops the spindle motor rotation and blinks the RDY LED.

This condition is reset by turning off and on the +5 V power supply. Figure 3.12 shows the flow from powering on, to the RTZ sequence.

(2) Servodata initialization

To initialize the servo data, the servo information on the disk is read, the initial value of the offset compensation is stored into the RAM in the MPU, and the offset compensation sequence is performed.

The data surface is divided into 8 zones. Each zone has a cylinder on its center position which records the servo information. The compensation data is generated by reading the cylinder sequentially.

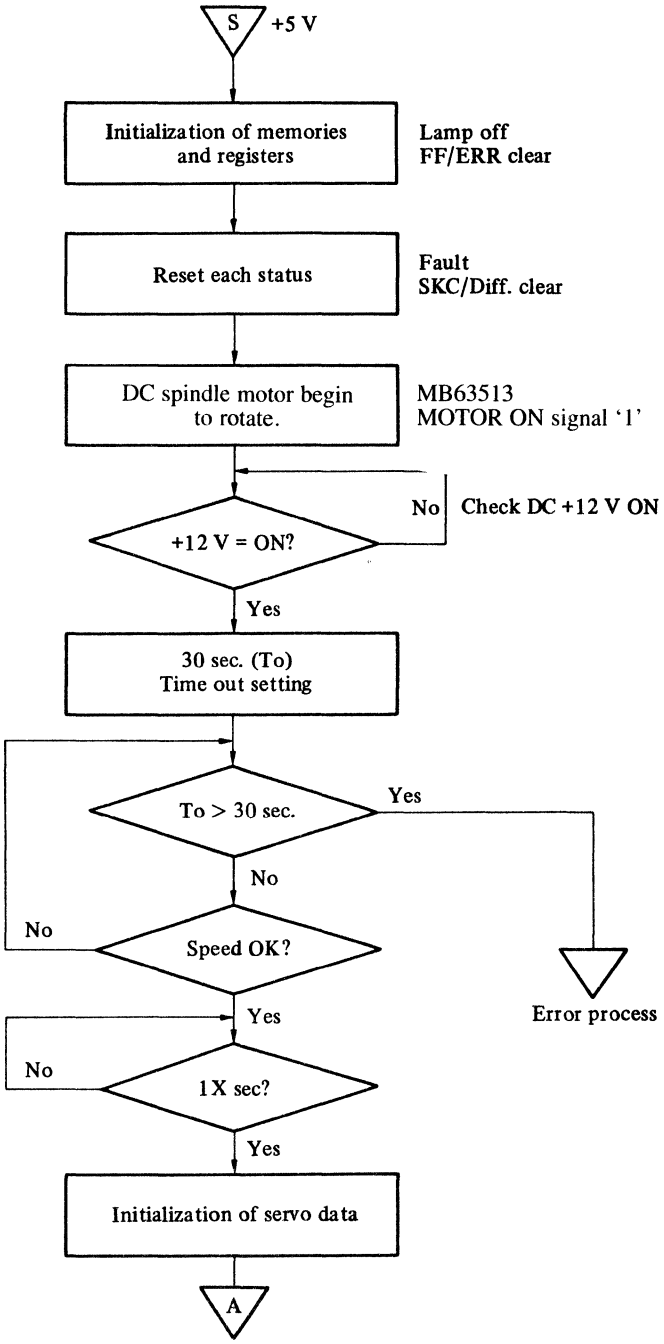


Figure 3.12 Power on sequence (Initialization)

3.5.3 RTZ sequence

The RTZ sequence makes the actuator move to cylinder 0, and is executed in 2 ways; initial sequence after power on and receiving the RTZ instruction.

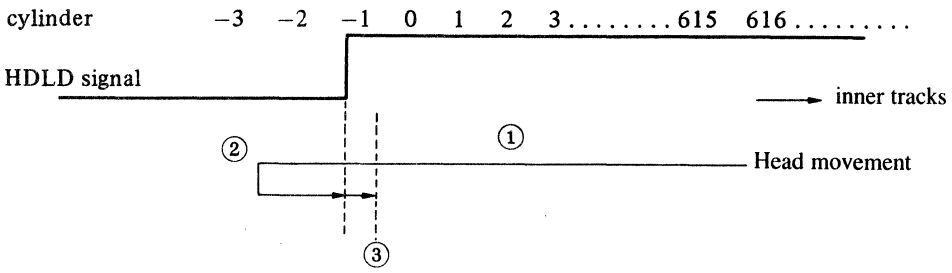
In the RTZ sequence, the following processes are performed.

① Time out setting (preparation for interrupt)

② SKC resetting

③ DRLM resetting

Next, confirmation of the HDLD signal is performed.



① Reverse Low Speed
② Forward High Speed
③ Forward Low Speed

In the RTZ sequence, the Reverse Low Speed signal, the speed control signal, is output, until the HDLD signal becomes false. Then, the speed control signal is changed from Reverse Low Speed, to Forward High Speed. When the HDLD signal becomes true, the speed control signal is changed to Forward Low Speed. When the head is in the proximity of cylinder 0 (SNN = 1), the speed control is changed to position control (LNMD = 1) and the head is positioned precisely to cylinder 0.

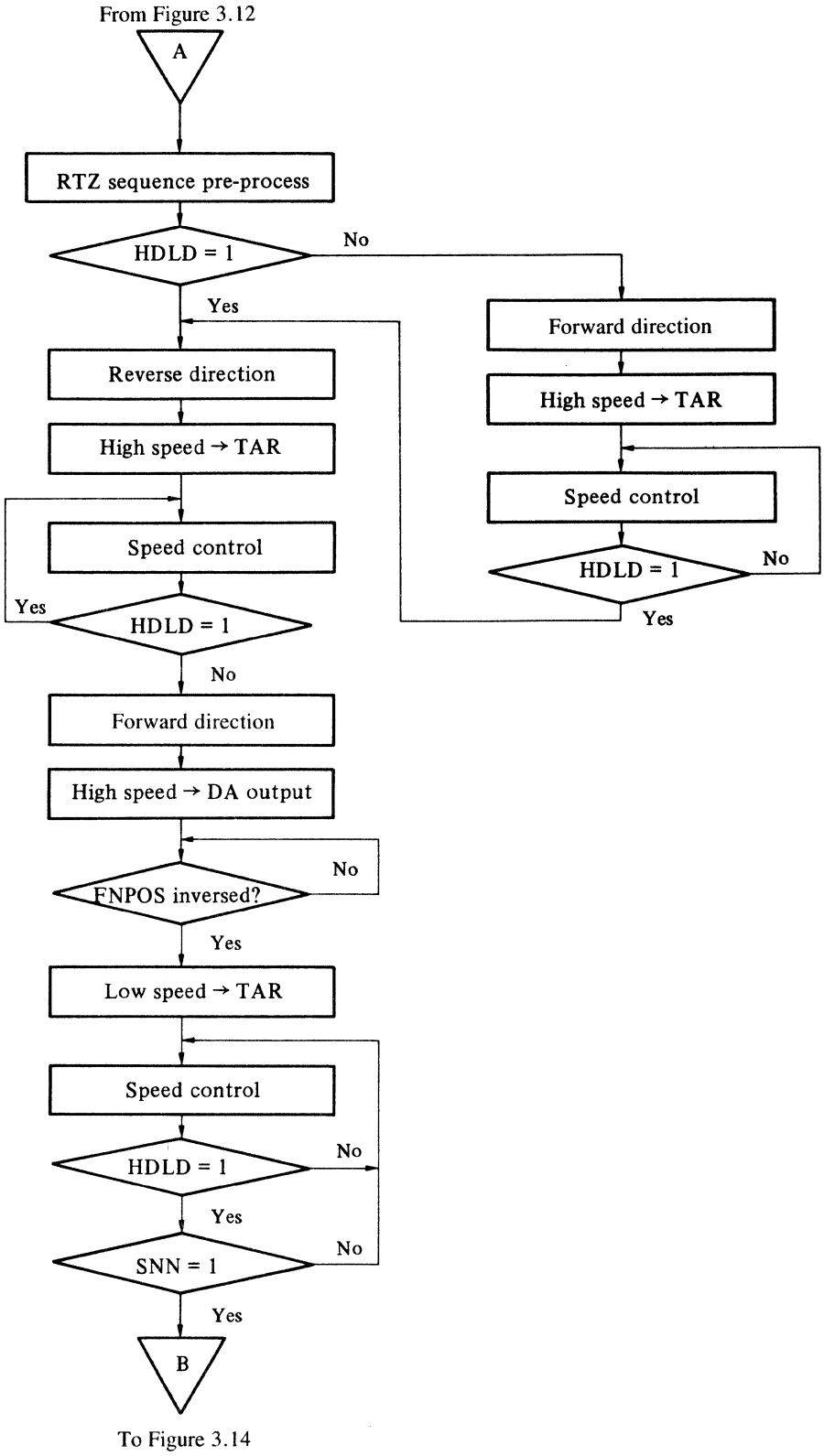
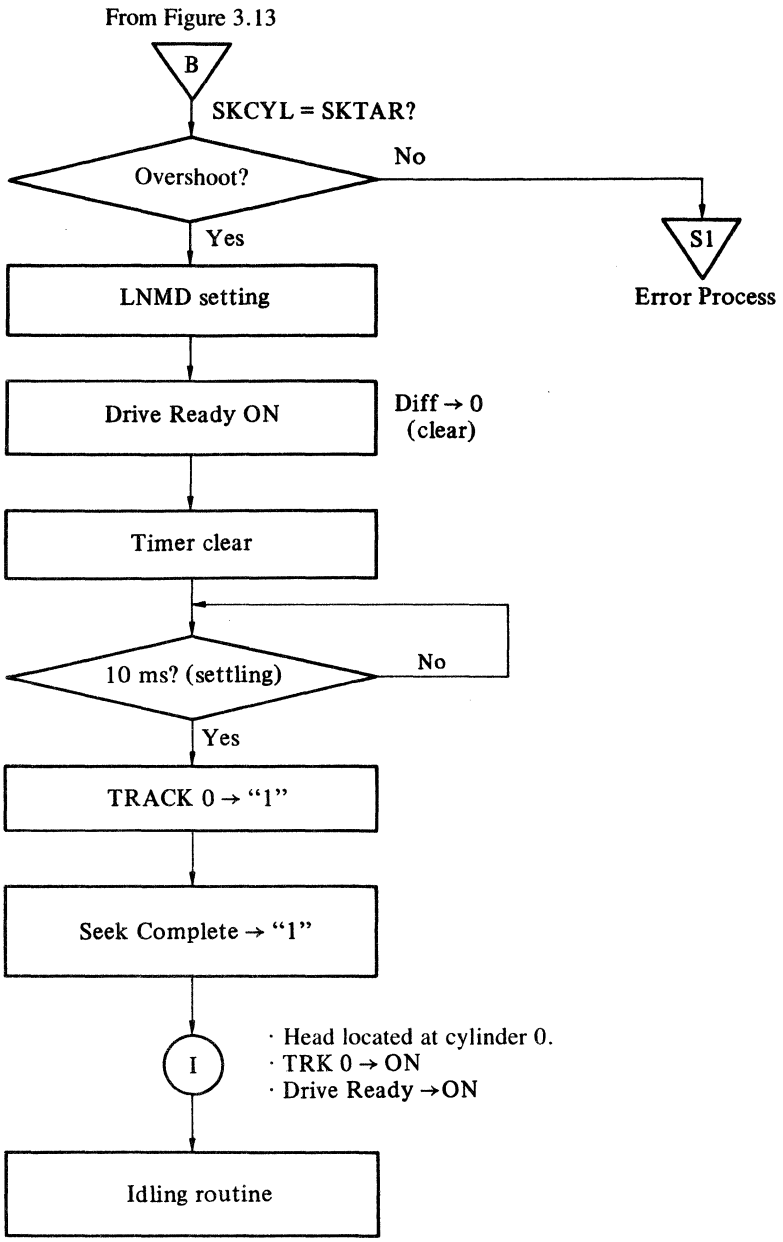


Figure 3.13 RTZ sequence



Note:

SKCYL: Current cylinder value
SKTAR: Target cylinder value
TAR: Target speed

Figure 3.14 After seek process

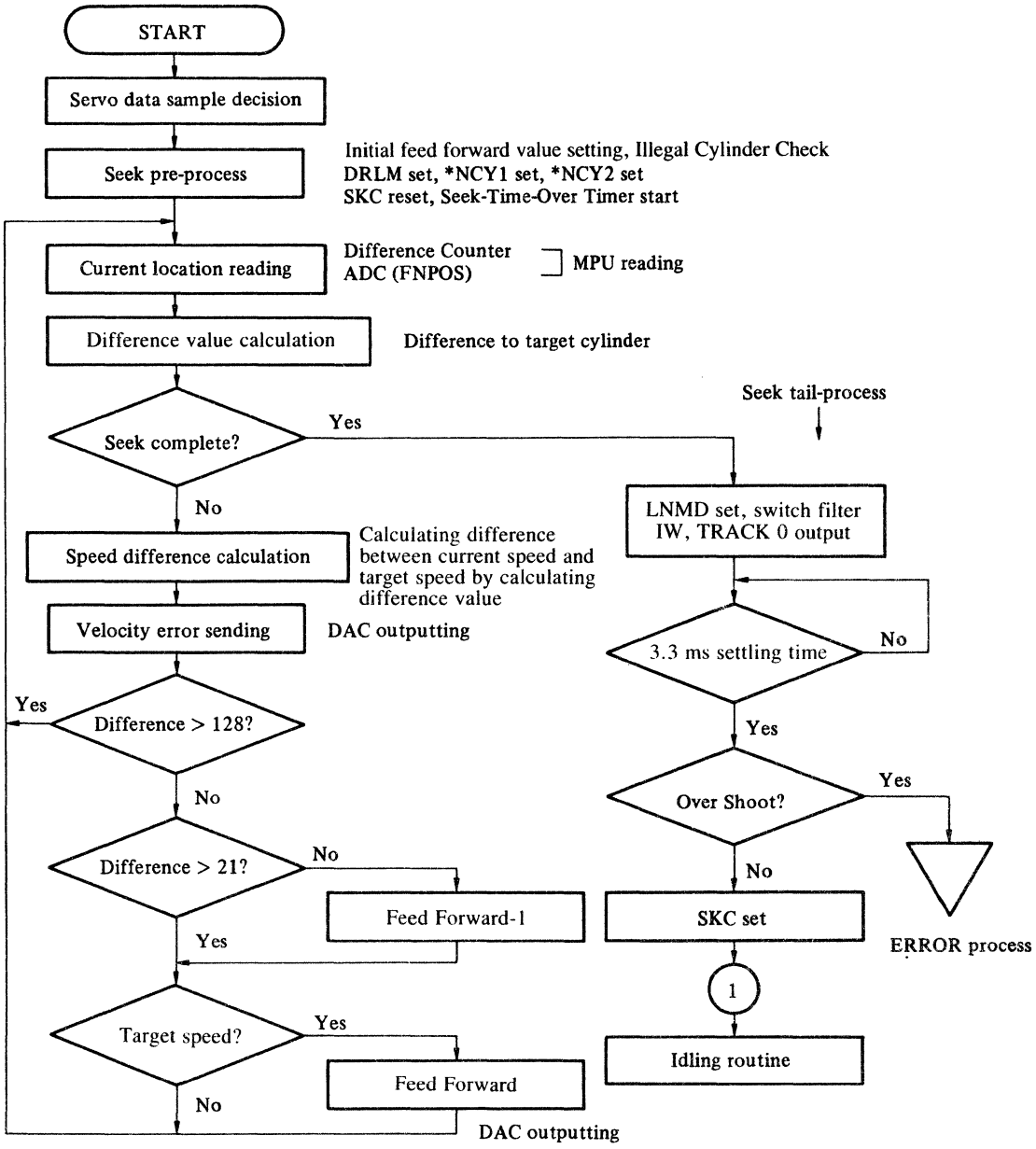


Figure 3.15 Seek sequence

(1) DC spindle motor control

Figure 3.16 shows the block diagram of the spindle motor control.

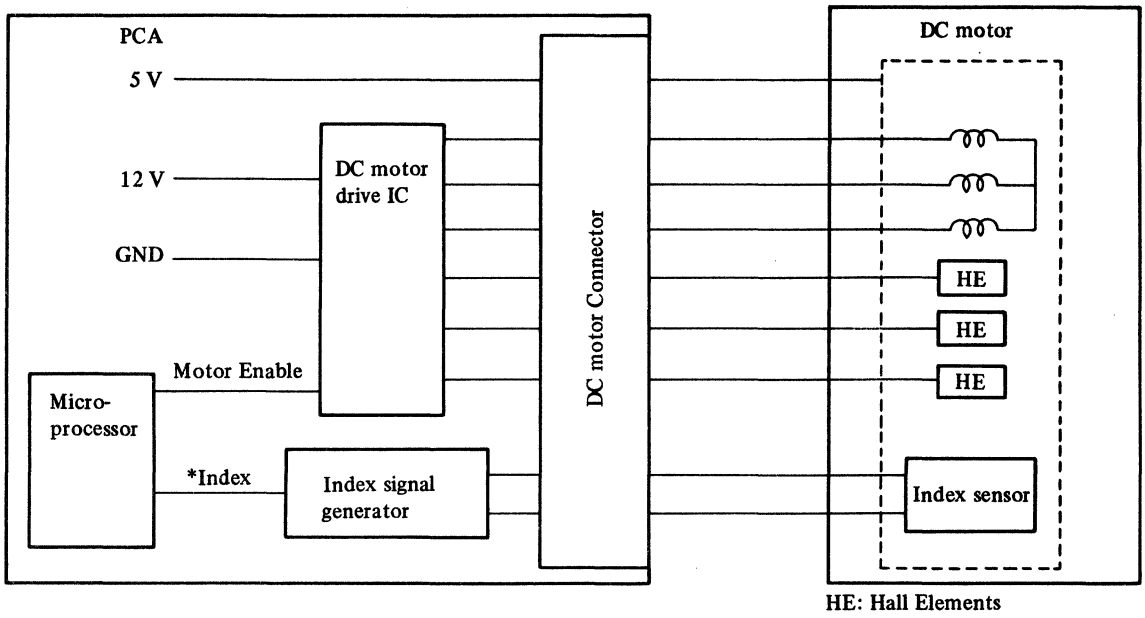


Figure 3.16 DC motor control block diagram

When power is turned on the MPU issues the motor start instruction (MTR Enable), the current control circuit drives the current to the phase selected by the phase control circuit. Phase control is performed by the hall sensor output signals (U/V/W). The DC spindle motor has the sensor to detect the Index signal.

3.5.4 Seek sequence

The Seek sequence is divided into 4 processes, servo data sample decision section, seek pre-process, seek speed control, and seek tail-process. In the seek pre-process, the following is performed according to the direction and number of stepping pulses given by the interface.

① Illegal Cylinder Check

② DRLM, SKC, *NCY1, and *NCY2 setup

③ Seek-Time-Over Timer start

④ Initial feed forward value set

In the servo data sample decision process, the following are performed.

① Checking whether the servo data sampling is necessary

② Checking the unsampled zone

③ Deciding whether to jump to the servo data sampling routine

In the seek speed control process, the current location is read and the difference value to the target cylinder is calculated. If the difference is 0, the flow enters into the seek tail-process. If the difference is not 0, then speed control is performed. The speed control is performed as follows:

① Calculate the difference between the current location and the last location

② Read the target speed corresponding to the difference value from EPROM

③ Set the speed of difference between the current speed and the target speed

The current location is given to read the value, by analog-to-digital converting the Fine Position signal indicated the detailed location between tracks, from the difference counter stored the track crossing pulse (TRXP).

To control the decreasing speed of the motor, the Feed Forward signal is output through the DA converter. This signal is not output when the difference value is more than 128, and is output from the point that the current speed exceeds the target speed. When the remaining difference value is less than 20, the feed forward value is decreased in each calculation cycle. So, it is available to decrease the speed in a gentle curve. The tail-process is a same process as a RTZ. Figure 3.18 shows the seek sequence flowchart.

3.5.5 Seek control circuit

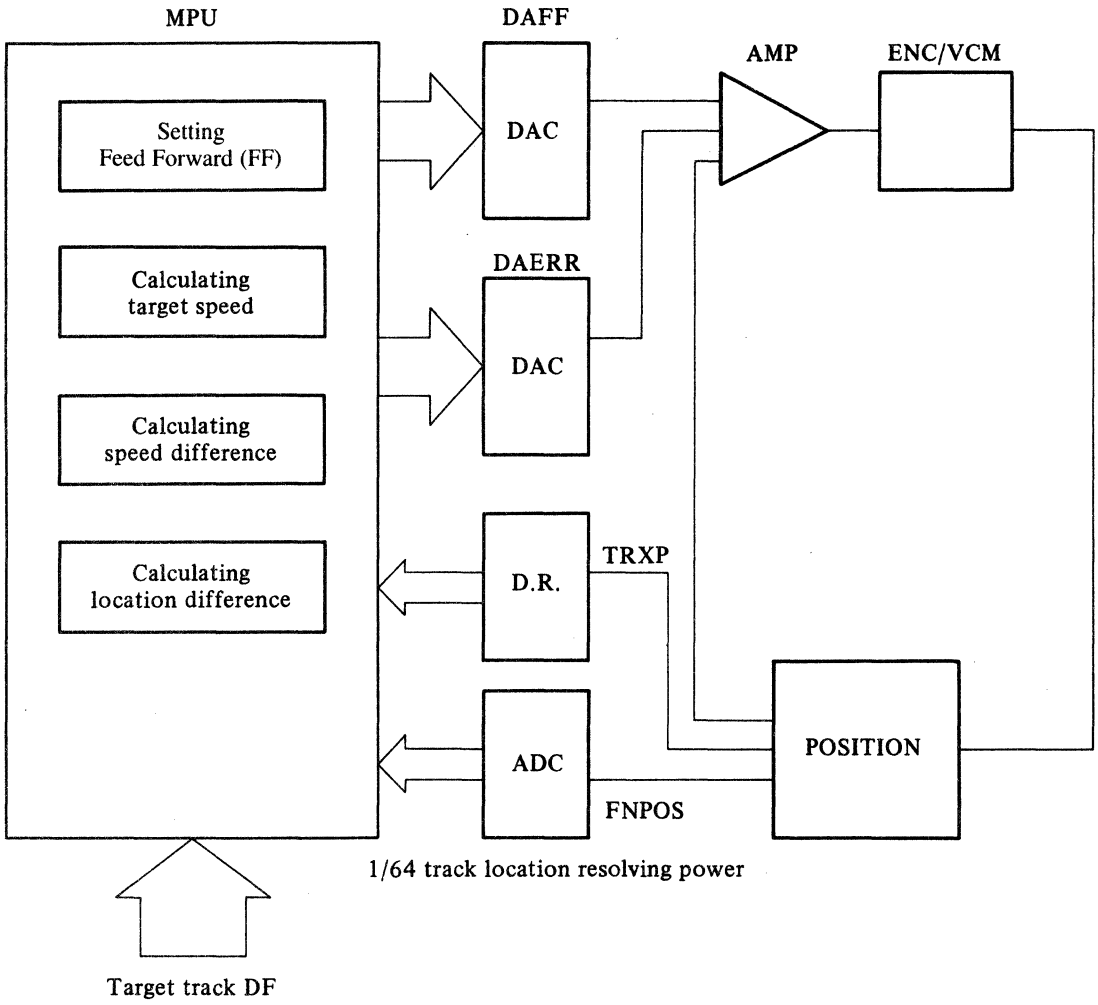


Figure 3.17 Seek block diagram

Figure 3.17 shows the block diagram of the seek circuit which performs the seek operation. The microprocessor (MPU) sets the feed forward value and flows the current to the actuator with DAERR signal. This feed forward value is an assumed preset value. The actuator accelerates and its actual speed is compared to the ideal speed by comparing the feedback (actual) speed with stored values. This produces a difference (DAERR) value which controls the current to the motor and through the deceleration phase, holds the target speed.

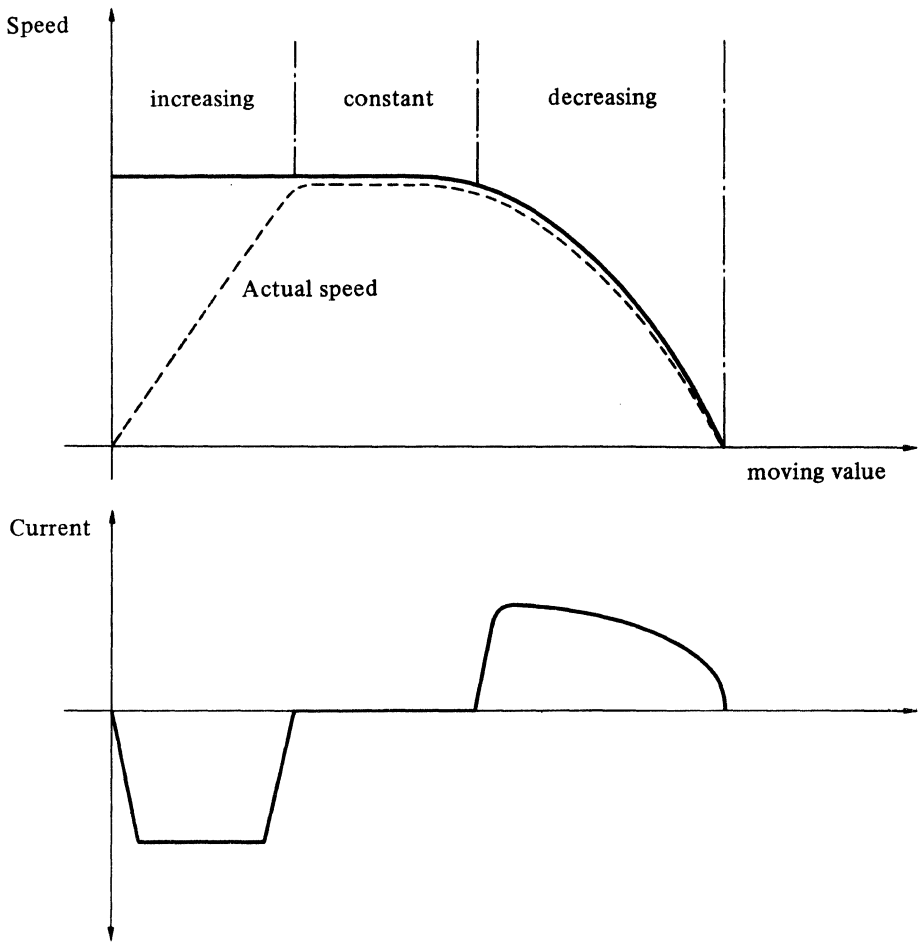
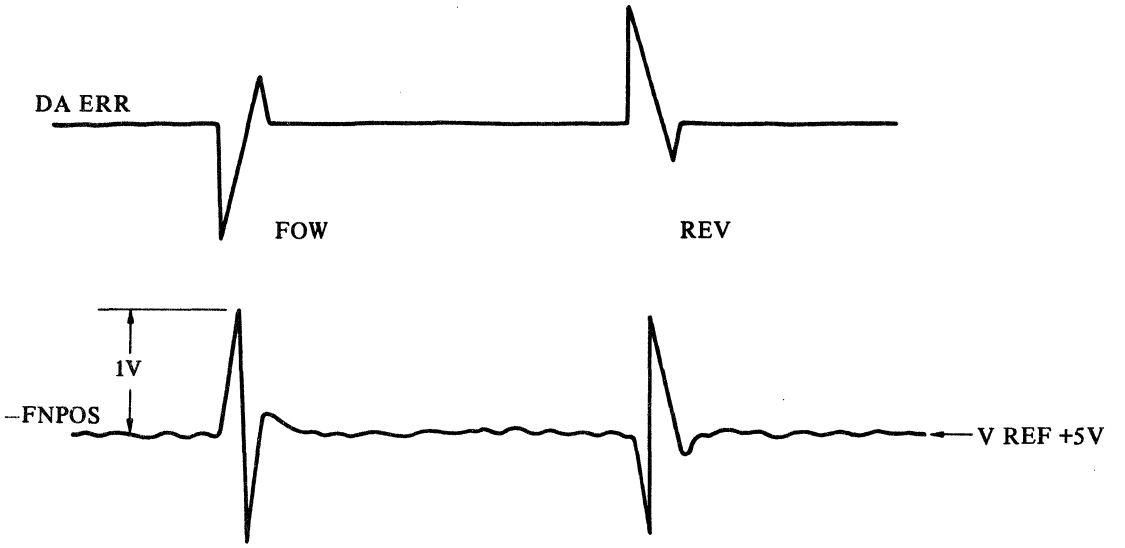
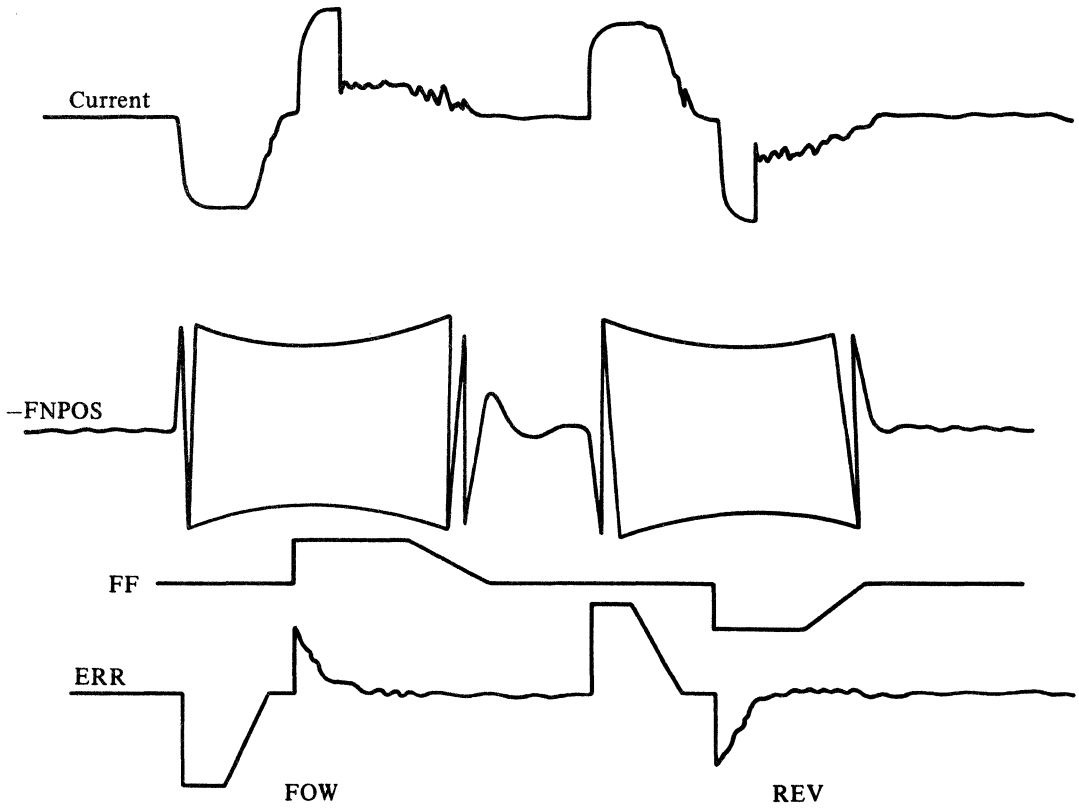


Figure 3.18 Seek current



1 position seek



256 position seek

Figure 3.19 Waveform during seek

3.5.6 Encoder

The encoder uses optical technology. Using a LED and photo sensors, the POSN and POSQ signals are generated by converting the quantity of light at the physically different locations into the electric signals. The FNPOS signal is generated by picking up the straight part of the POSN and POSQ signals in the electric circuit. The sensor for the HDLD signal, at another location, outputs the HDLD signal.

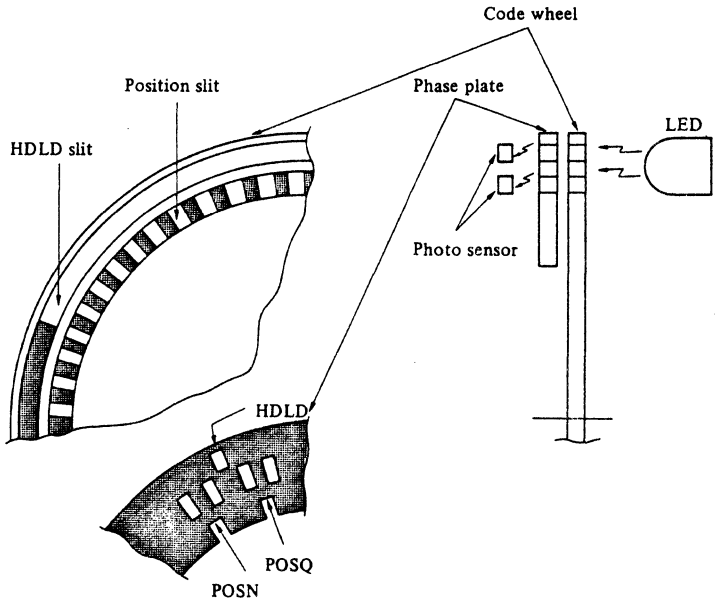


Figure 3.20 Encoder principle diagram

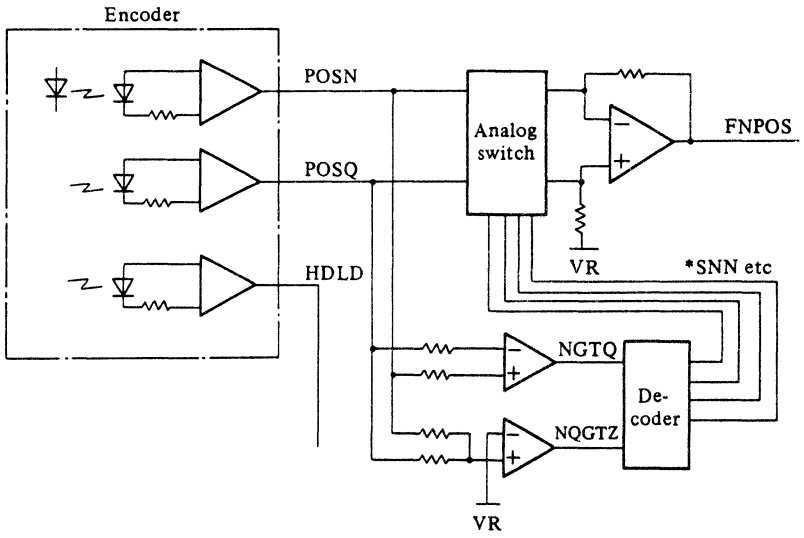


Figure 3.21 Fine Position signal generation circuit block diagram

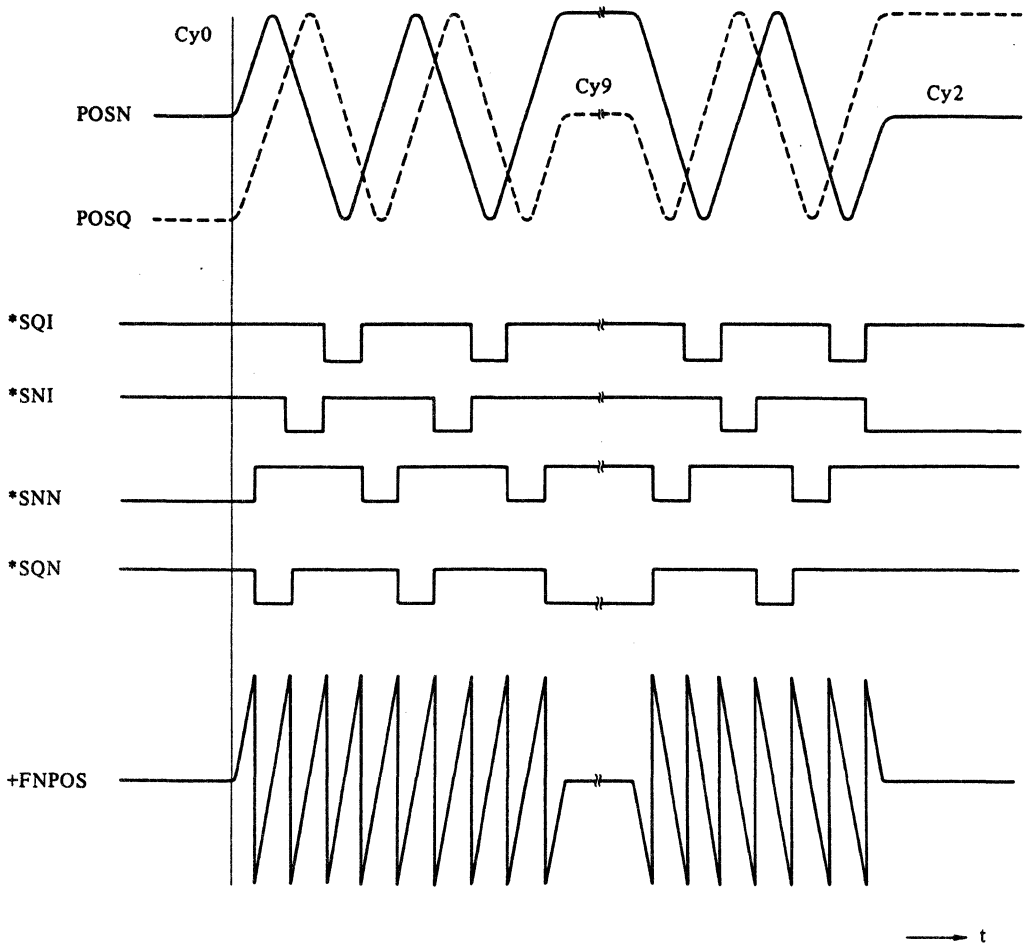


Figure 3.22 Waveform of each signal in Fine Position signal generation circuit

3.5.7 Clamp position

*EQUAL signal is active when a phase of current cylinder is the same as the phase of the target cylinder. When the phase of the current cylinder is different, the FNPOS signal is kept at the clamp level to extend the control range between +1.5 and −2.5 cylinders from the target cylinder. Figure 3.23 show the timing chart.

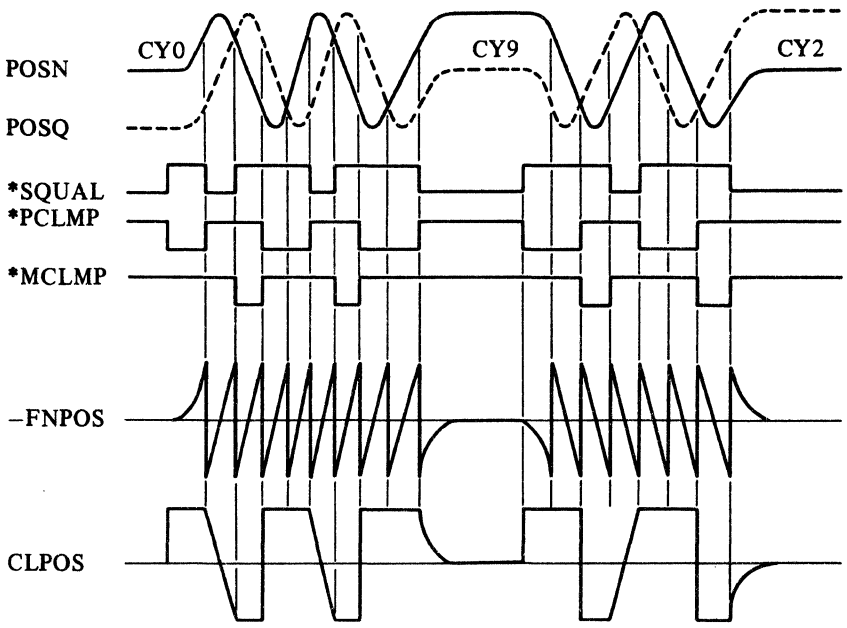


Figure 3.23 Clamp position timing chart

3.5.8 Fault detection during seek

(1) VCMHT (Encoder motor heat detection circuit)

If abnormal current flows into the Encoder motor, the heat detection circuit detects it and sends VCMHT signal to MPU. To detect, voltage, generated at resistor for current detection, is time-integrated.

(2) Seek time over

The timer/counter in the MPU is set before starting a seek. During this time, if seek is not completed, an internal interruption of the MPU occurs and the flow transfers from the seek operation routine to the time over routine.

(3) Over-shoot check

After a seek, a check is made to see if an overshoot has occurred. This is detected from the difference between the current position and the target position.

3.5.9 Read/write circuit

The read/write circuit consists of the head IC section inside the DE, the write circuit and the read circuit. Figure 3.24 shows the block diagram of the read/write circuit.

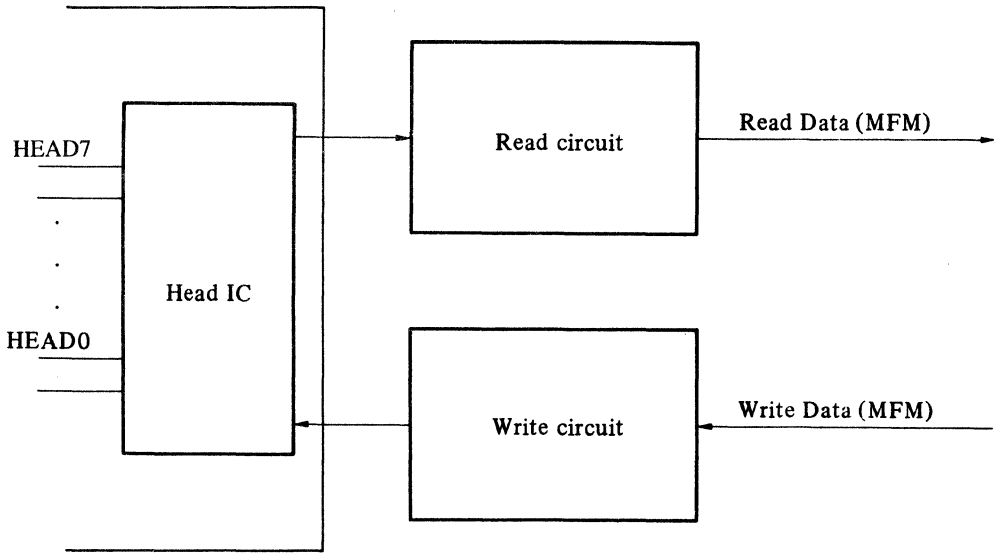


Figure 3.24 Read/write circuit block diagram

(1) Head IC section

The head IC section consists of 8 channel circuits, having the pre-amplifier and the write amplifier. Each channel is connected to a data head. The M2225D2, M2226D2 and M2227D2 drives have 1 head IC inside the DE.

(2) Write circuit

Figure 3.25 shows the block diagram of the write circuit.

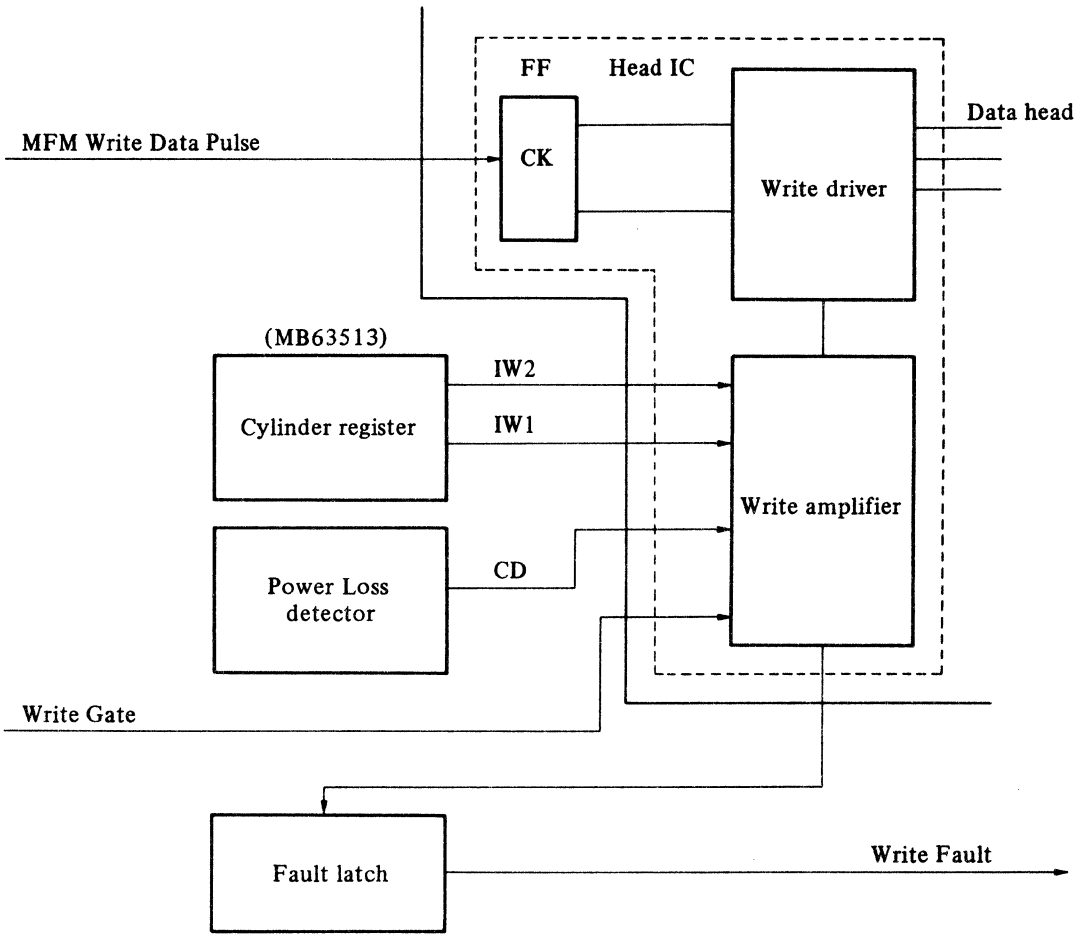


Figure 3.25 Write circuit block diagram

(a) Write amplifier

This is a write current source detection circuit that decides the correct write current value of the head. This circuit is set on/off with a write command signal "Write Gate" from the controller. The current value is changed according to the cylinder address of the head to flow the optimum current to the head. If an error is detected in the Write Fault or Power Loss detection circuit, the current source is cut off unconditionally.

(b) Write driver

This is included in the head IC. This receives current from the write amplifier and changes the current to be sent to the data head according to the write data pulse (WDP).

(c) Write Fault detection circuit

This circuit detects a fault during the write operation. This sets the Fault Latch and sends the Write Fault to the controller in the following cases.

① When write current is not supplied to the head.

② When the DC voltage is abnormal.

Fault Latch is held until the controller resets with Fault Clear.

(d) Power Loss detection circuit

When the power is switched on/off or a power hit occurs, an abnormal current may flow in the head because of a disturbance of the logic circuit, resulting in destruction of disk data. Therefore, the Power Loss detection circuit monitors the DC voltage level; if the voltage drops, the circuit clamps the write amplifier current source before the logic circuit is disturbed, to protect the head from abnormal current.

(3) Read circuit

Figure 3.26 shows a block diagram of the read circuit and waveforms.

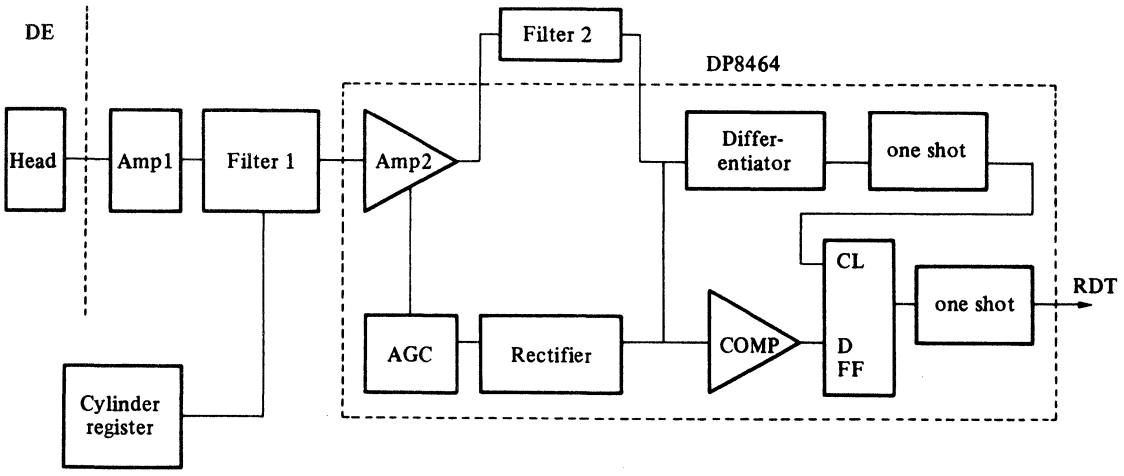


Figure 3.26 Read circuit block diagram

(a) Pre-amplifier

This is included in the head IC. The Read signal is generated by flux reversals on the disk and the detected head output signal is input to the pre-amplifier, and amplified approximately 100 times.

(b) Amplifier 1

This amplifies the read signal approximately 30 times.

(c) Filter 1/2

These filters eliminate high-frequency noise from read signals amplified by the pre-amplifier and main amplifier. The filter characteristics are changed according to the cylinder address of the head to compensate for the difference of head output signal characteristics between outer and inner cylinders.

(d) Amplifier 2

Amplifier 2 has an AGC amplifier function to keep a constant output waveform at the filter 2.

(e) Differentiator circuit

The peak position of the read signal output from the pre-amplifier indicates the flux reversal point. This circuit, including CR, converts flux points to zero-crossing points.

(f) Pulse shaper

This circuit detects zero-crossover points of the differentiated waveform amplified by the main amplifier, then converts them to TTL level.

(g) Shoulder noise elimination circuit

A read waveform sent from the head, has shoulders as shown in Figure 3.27. Differentiation of this waveform shows that the shoulders are close to the zero-cross line. External noise may add noise pulses to pulse shaper outputs. The shoulder noise elimination circuit selects signal and noise pulses according to the pulse width, and eliminates pulses narrower than the specified pulse width as noise pulses.

(h) Waveform shaping circuit

This circuit generates raw data having the specified pulse width from the leading and trailing edges of the shoulder noise elimination circuit outputs.

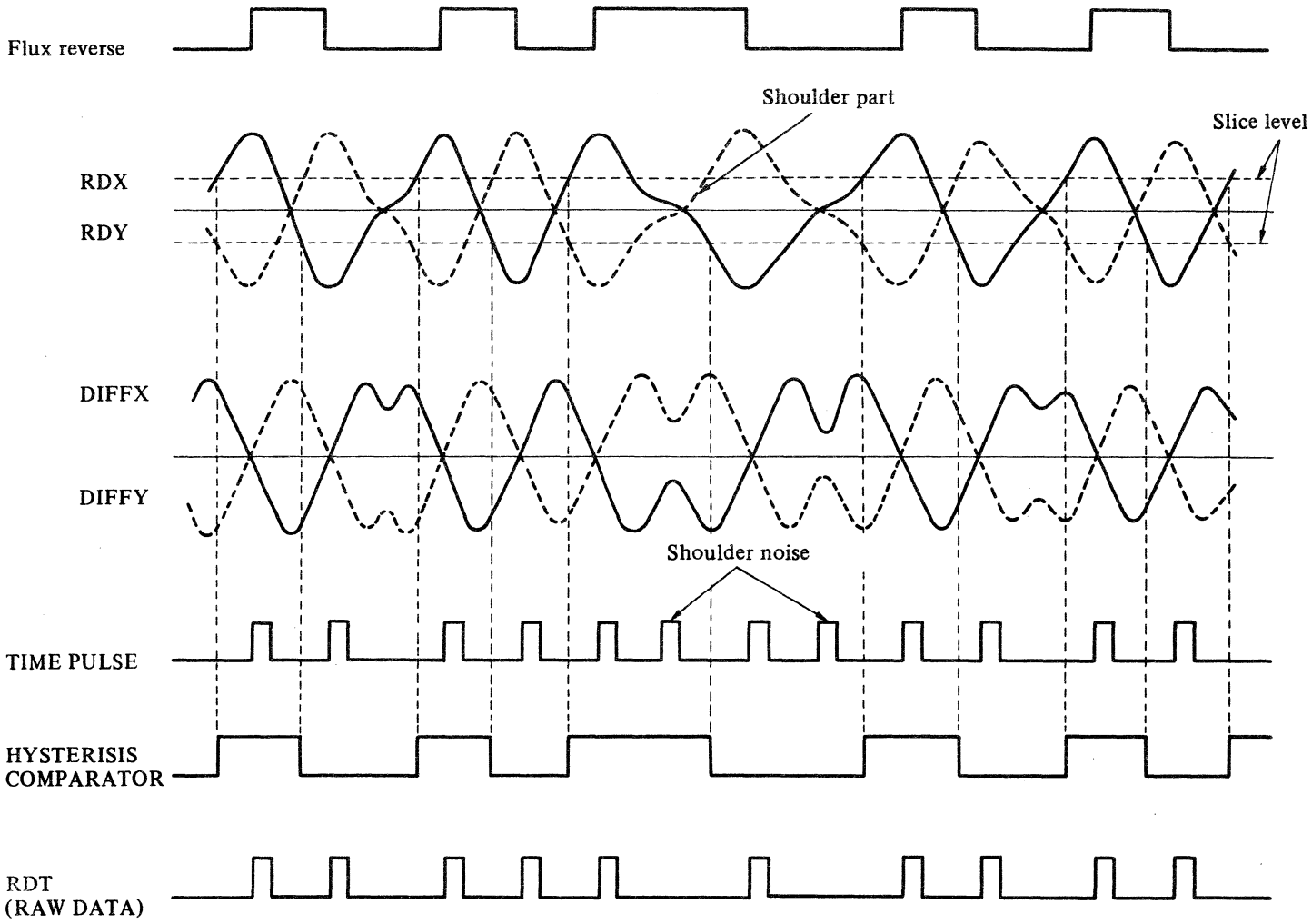


Figure 3.27 Read circuit waveforms

CHAPTER 4 TROUBLESHOOTING

This chapter explains a troubleshooting method.

A number in parentheses near the diamond indicates the check location in Figure 4.1.

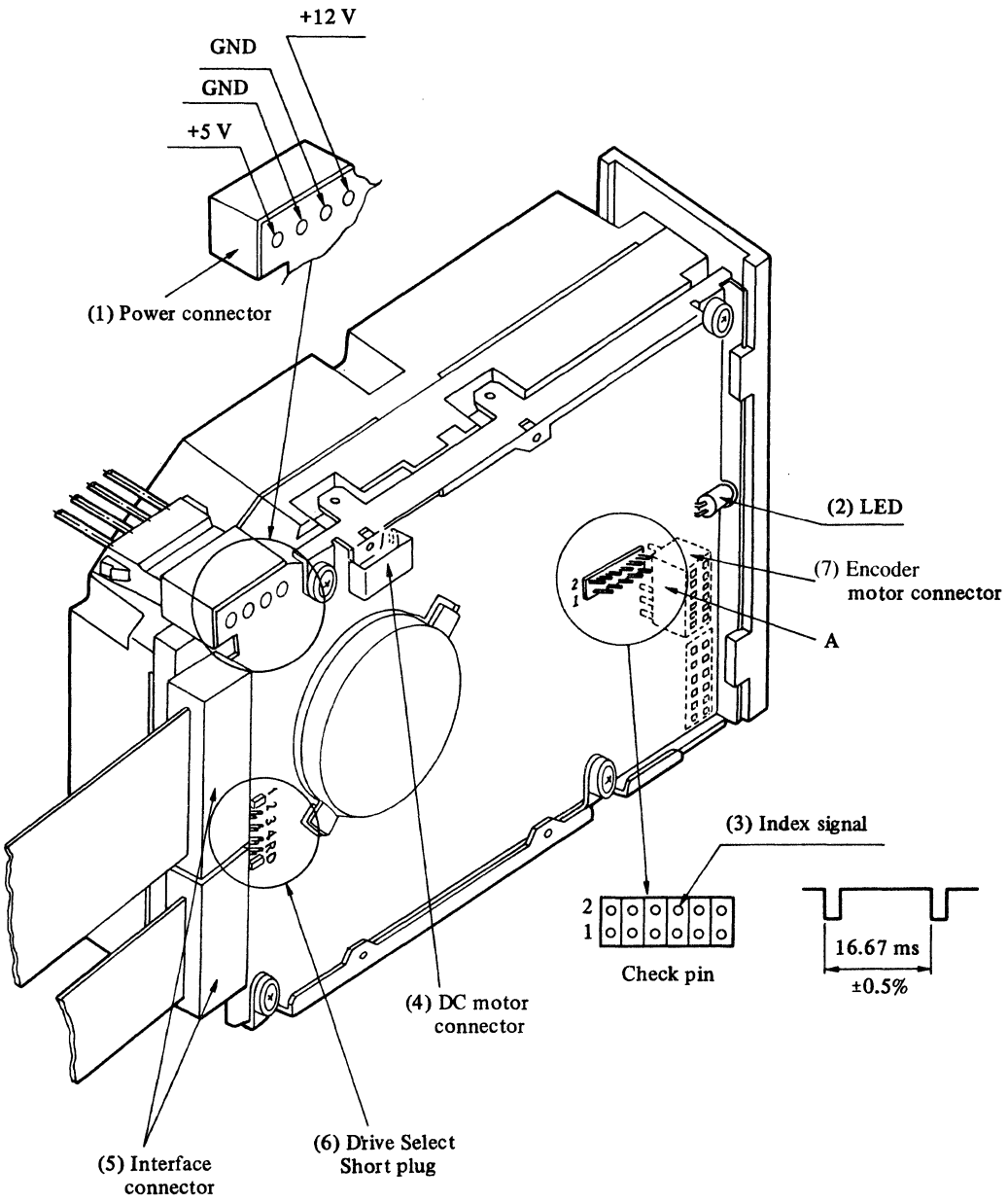
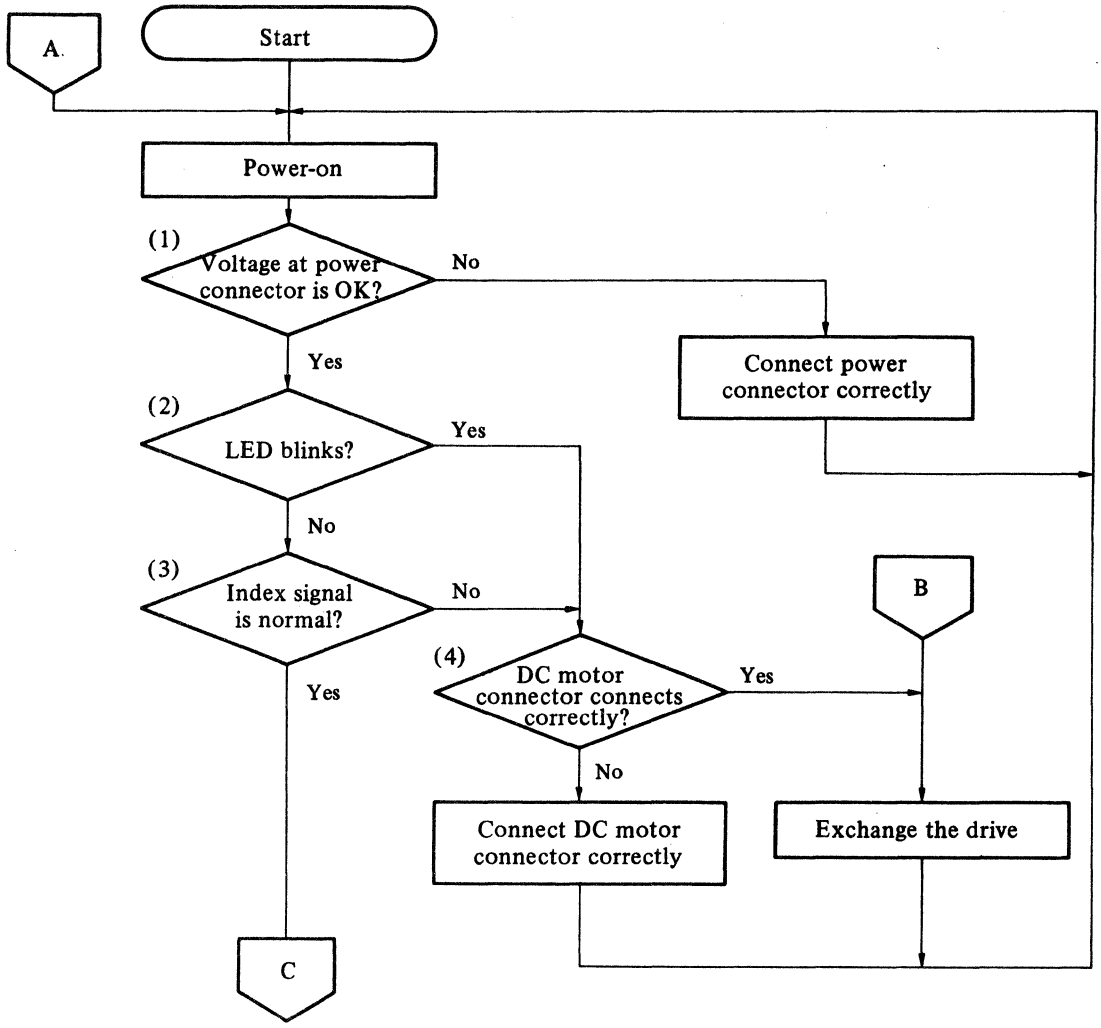
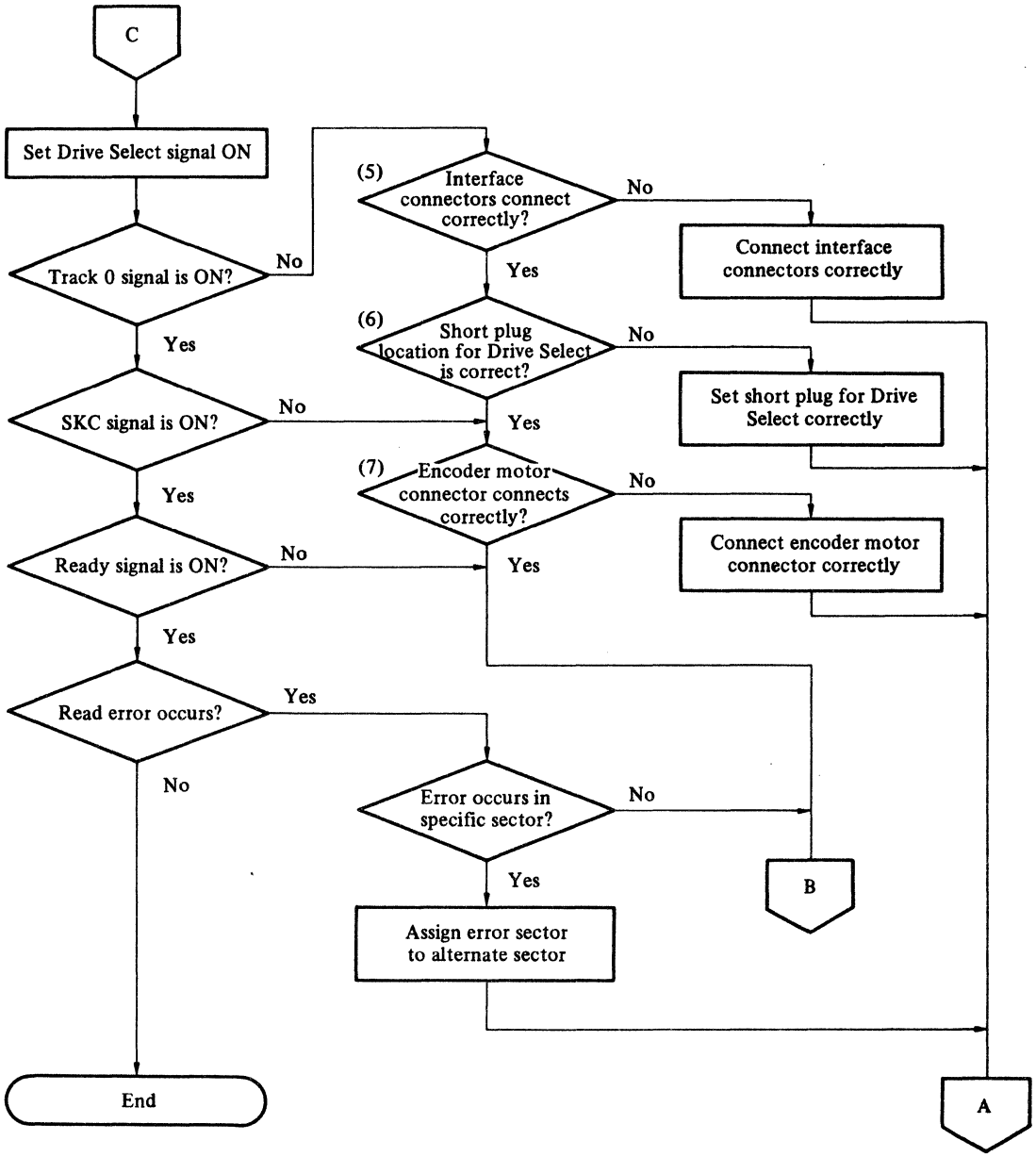


Figure 4.1 Check location


A.
Start
Power-on
(1)
Voltage at power connector is OK?
No
Connect power connector correctly
Yes
(2)
LED blinks?
Yes
No
(3)
Index signal is normal?
No
B
(4)
DC motor connector connects correctly?
Yes
Yes
No
Connect DC motor connector correctly
Exchange the drive
C


C
Set Drive Select signal ON
Track 0 signal is ON?
No
Yes
SKC signal is ON?
No
Yes
Ready signal is ON?
No
Yes
Read error occurs?
Yes
No
End
(5) Interface connectors connect correctly?
No
Connect interface connectors correctly
Yes
(6) Short plug location for Drive Select is correct?
No
Set short plug for Drive Select correctly
Yes
(7) Encoder motor connector connects correctly?
No
Connect encoder motor connector correctly
Yes
Error occurs in specific sector?
No
Yes
Assign error sector to alternate sector
B
A

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