M1053BD - DIF

Intelligent Disk Controller Engineering Specifications

FUJITSU

B05P-2180-0101A...01A

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PREFACE

This manual describes the M1053BD Intelligent Disk Controller which has been developed as the SCSI controller for Fujitsu micro-disk drives.

This manual provides a detailed explanation of the M1053BD Intelligent Disk Controller, including its specifications and functions.

This manual consists of the following:

Chapter 1 Outline

Introduces M1053BD Intelligent Disk Controller by describing its features and specifications.

Chapter 2 Installation

Illustrates controller configuration and cable connection. Also includes a description of installation and installation requirements (such as power requirements and the setting switches).

Chapter 3 Host Interface

Includes SCSI control procedures and electrical requirements for interfacing with the host system and the controller.

Chapter 4 Messages

Describes the definition and the functions of messages which are provided for controlling the host interface.

Chapter 5 Data Format and Addressing

Describes data structure and organization on the micro-disk drive and addressing method.

Chapter 6 Commands

Describes the definition and the functions of commands.

Chapter 7 Status Byte and Sense Data

Describes the status byte and sense data structure.

Chapter 8 Error Recovery

Describes the error recovery procedure taken by the controller.

Chapter 9 Diagnosis and Maintenance

Describes the diagnostic functions of the controller and the maintenance information.

Appendix A Drive Interface

Provides a brief explanation about the drive interface for reference.

Appendix B Command Processing Time

Provides a reference of the timing conditions to estimate performance.

Appendix C Options

Describes the optional accessories which are provided to facilitate disk subsystem integration.

For more detailed information about the host interface (SCSI) and the functionality of commands, to develop the host adapter for SCSI and host software, refer to the following manual:

SCSI Intelligent Disk Controller Functional Specification
(Secification No. B05P-2180-0011A)

For details about micro-disk drive function and operations, refer to the OEM manual dedicated to each micro-disk drive.

The M1053BD Intelligent Disk Controller may be abbreviated to 'controller' or 'IDC'. Also micro-disk drives may be referred to as drives, or devices.

CONTENTS

FIGURES

TABLE

CHAPTER 1 OUTLINE

1.1 Overview

The M1053BD Intelligent Disk Controller is a compact, high-performance, and highly-reliable SCSI controller for Fujitsu micro-disk drives.

The controller incorporates control circuits which form LSIs and a microprocessor within the PCA whose size meets the form-factor for 8-inch disk drive. The controller can control up to four drives.

The interface that connects the controller with the host system is based on the SCSI (Small Computer System Interface) standard.

The flexibility and expandability of SCSI, as well as the powerful command set, offered by this controller allow the user to construct a high-performance and highly-reliable disk subsystem with large storage capacity.

1.2 Features

(1) Employing LSI design

LSI technology is used to construct the compact, high-performance, and highly-reliable controller.

(2) Compact size

The controller is contained on a single PCA whose size meets the form-factor for an 8-inch disk drive. The controller can be directly mounted on the drive.

(3) Controlling four drives

Up to four drives can be controlled by one controller.

(4) SCSI

The interface between the host system and the controller meets SCSI standard. The following extended features are also provided:

- Arbitration
- Disconnection/reselection
- Synchronous data transfer with 4 MB/s maximum transfer rate

(5) Comprehensive command set which meets CCS requirements

All of SCSI standard commands and extended commands are provided and the command set meets the SCSI CCS (Common Command Set for Direct Access Device) requirements. In addition, powerful Vendor Unique Commands have been provided to improve data handling capability.

These commands can manipulate data through logical block addressing independent of the physical characteristics of the drive. This allows software to be fertile in flexibility for the future expansion.

(6) Contiguous block processing

Standard commands allow up to 256 blocks to be processed consecutively. Extended commands allow up to 65,535 blocks to be processed consecutively.

The host system software can handle logically-continous space without being aware of the physical boundaries because the switching between cylinders and tracks is automatically performed inside the controller.

(7) Reserve and release functions

Drive can be exclusively accessed in the multi-programming or multi-host system environment owing to the reserve and release functions.

(8) Data Buffer

The controller contains 16 KB data buffer and provides two types of buffer operation, Full Buffering Mode and Dual Sector Buffer Mode. The former aims at improvement of the total system throughout while the latter facilitates quick response time.

(9) Command Queuing

The controller can accept multiple commands from multiple hosts (up to seven hosts) for each attached disk drive.

(10) Sector interleaving

The sector interleaving function allows data on the drive to be accessed at specified sector intervals to match to host interface transfer performance.

The number of sector intervals (Interleave Factor) is user selectable. Together with the Dual Sector Buffering, the sector interleaving provides the appropriate data transfer speed for the host system's performance.

(11) Automatic data error correction

Correctable data error can be corrected in the data buffer so that error-free data is transferred to the host system.

(12) Internal retry

If a recoverable error occurs, this feature attempts to recover from errors inside the controller.

(13) Rotational position sensing (RPS)

RPS is provided for each drive. The amount of occupation of the host interface can be effectively reduced through the use of the disconnection/reselection function.

(14) Alternate block processing

Defective block are replaced by alternate blocks. Host system software can deal with the entire space of the drive as if it was defect-free. High-speed alternate block processing is available without seek operations, because an alternate block area is provided for each cylinder.

(15) Automatic alternate block assignment

Available alternate block area is automatically allocated to assign an alternate block for a defective block.

(16) Diagnosis

The controller has a diagnostic capability which checks internal controller functions and drive operations to facilitate testing and repair work.

1.3 Specifications

Table 1.1 lists the specifications of the controller. See Table 1.2 for the specifications of drives which can be attached to this controller.

Table 1.1 Specifications

Controller product number			B05B-2180-B101A (M1053BD)
Mounting frame (optional)			B05B-2180-H001A (M1053A11)
Host interface			Differential type SCSI •Cable length: 25 m max. •Asynchronous mode data transfer: 1.5 M bytes/s max. •Synchronous mode data transfer: 4.0 M bytes/s max.
Command processing	Command types		36 (25 CCS + 11 Vendor Unique)
	Data transfer	Without interleaving	4.0 M bytes/s max.
		In inter-leave mode	Less than 1.2 M byte/s typ. (depends on interleave factor)
Dimensions			196 × 330 × 19.1 mm
Usage conditions	Power requirements		+5 VDC ±5% 5.0 A max. −12 VDC ±5% 1.0 A max.
	Tempera-ture	Operating	5°C–40°C (41°F–104°F)
		Non-operating	−40°C–60°C (−40°F–140°F)
	Relative humidity	Operating	20%–80% RH
		Non-operating	5%–95% RH

Table 1.2 Specifications of controlled drive (1/2)

		M2333KS		
Storage capacity	Unformatted	337.1 MB		
	Formatted (user area)	245.9 MB	277.4 MB	294.2 MB
Number of disks		6		
Number of heads (R/W + SV)		10 + 1		
Number of cylinders		823		
Track format	Track capacity	40,960 bytes		
	Sectors per track	121	69	37
	Bytes per sector	256	512	1,024
Rotational speed		3,600 rpm		
Data transfer rate		2.458 MB/s		
Access time	Positioning time	Average 20 ms		
	Latency	Average 8.3 ms		
Dimensions		216 × 127 × 380 mm		

Table 1.2 Specifications of controlled drive (2/2)

		M2331KS		
Storage capacity	Unformatted	168.5 MB		
	Formatted (user area)	118.7 MB	134.5 MB	142.9 MB
Number of disks		3		
Number of heads (R/W + SV)		5 + 1		
Number of cylinders		823		
Track format	Track capacity	40,960 bytes		
	Sectors per track	121	69	37
	Bytes per sector	256	512	1,024
Rotational speed		3,600 rpm		
Data transfer rate		2.458 MB/s		
Access time	Positioning time	Average 20 ms		
	Latency	Average 8.3 ms		
Dimensions		216 × 127 × 380 mm		

Note: Disk Drive Order Specification (For Reference)

The disk drive to be attached to IDC must be preformatted in the prescribed data format.

Accordingly, the data format must be specified when the disk drive is ordered. The following shows how to specify a data format:

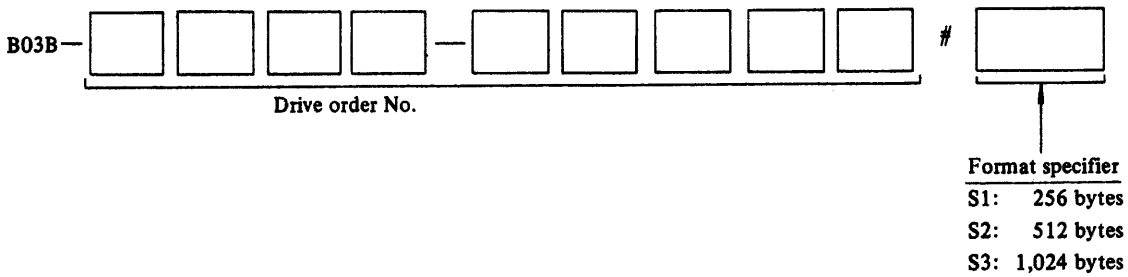


Table 1.3 lists the order specification. The data format is labeled on each disk drive product.

Table 1.3 Disk drive order specification

Model	Product No. (order specification)	Format (data length)	Remarks
M2333KS	B03B-4765-B043A #S1	256 (bytes)	
	B03B-4765-B043A #S2	512	
	B03B-4765-B043A #S3	1,024	
M2331KS	B03B-4765-B041A #S1	256 (bytes)	
	B03B-4765-B041A #S2	512	
	B03B-4765-B041A #S3	1,024	

CHAPTER 2 INSTALLATION

2.1 Controller Configuration

2.1.1 Physical configuration

The IDC consists of a single PCA whose size conforms to the form-factor for an 8-inch disk drive.

Figures 2.1 and 2.2 show the external view and dimensions of IDC.

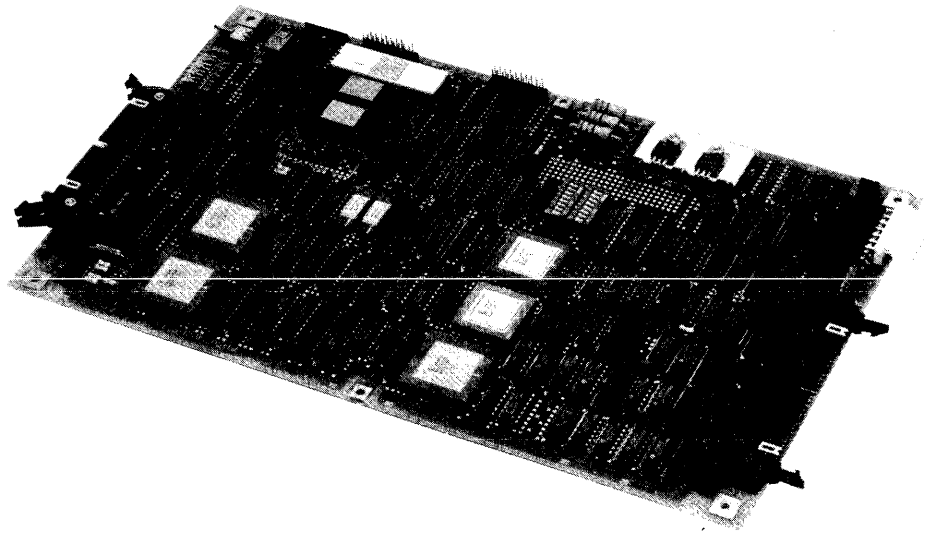


Figure 2.1 IDC external view

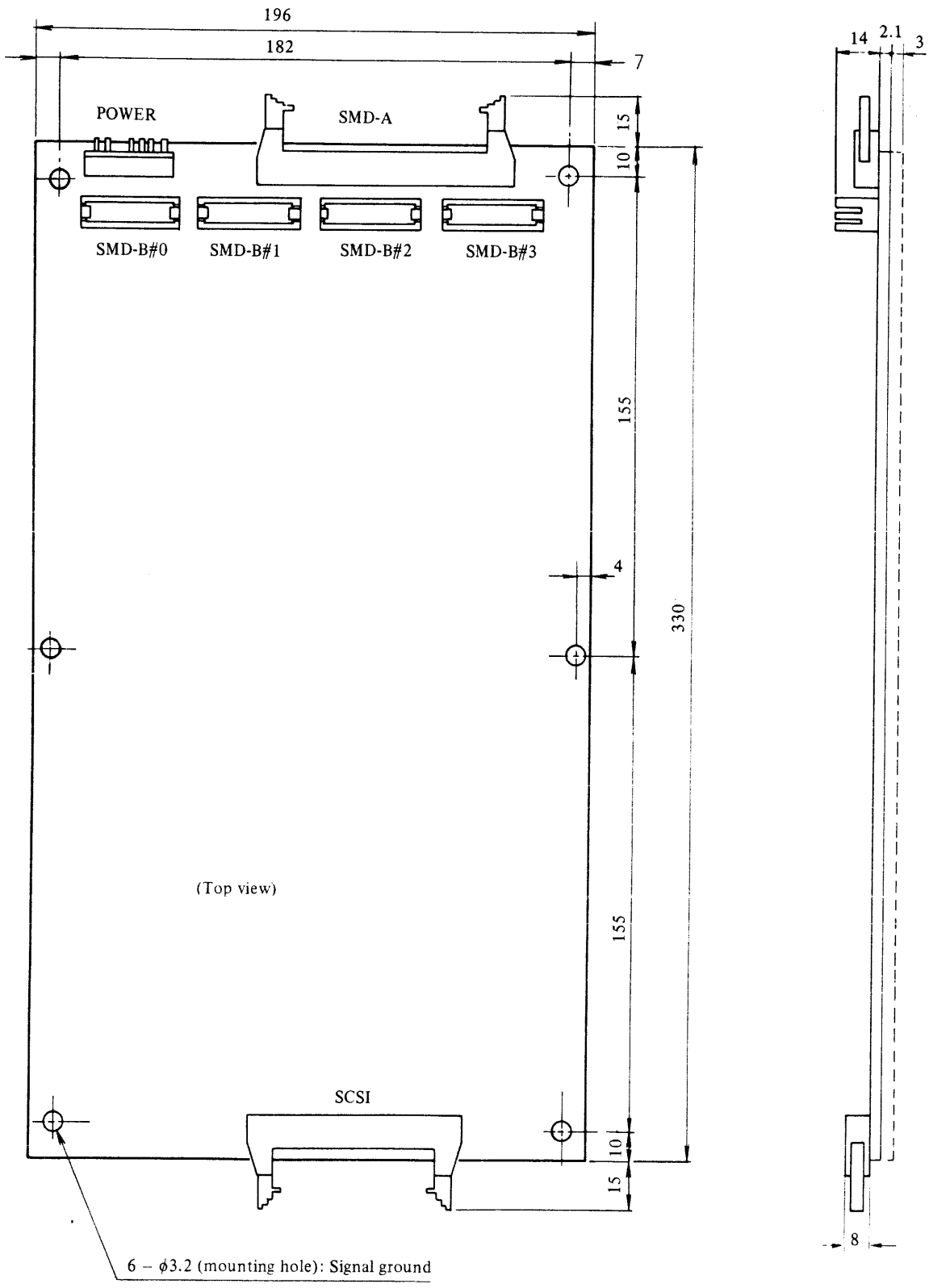


Figure 2.2 IDC dimensions

2.1.2 Circuit configuration

Figure 2.3 shows IDC circuit configuration. The basic IDC components include the following:

- Microprocessor
  - Host interface and drive interface control
  - Command execution, status information generation and error recovery
  - Self-diagnostic program execution
- Host interface
  - Differential driver and receiver circuits
- Drive interface
  - SMD interface driver and receiver circuits (for four drives)
- Data buffer
  - 8 KB × 2
  - Data transfer speed matching feature (sector interleaving)
  - Data error correction
- SPC
  - SCSI protocal control and data transfer timing control
  - Data register (FIFO)
- DBM
  - Data buffer and data path control
  - Data search control
- FMT
  - Sector format control and read/write control
  - Drive interface control
  - ID register
- SDC
  - SERDES
  - ECC (polynominal: $(X^{21} + 1)\ (X^{11} + X^2 + 1)$)
  - Data comparison
- RPS
  - Rotational position sensing for four drives

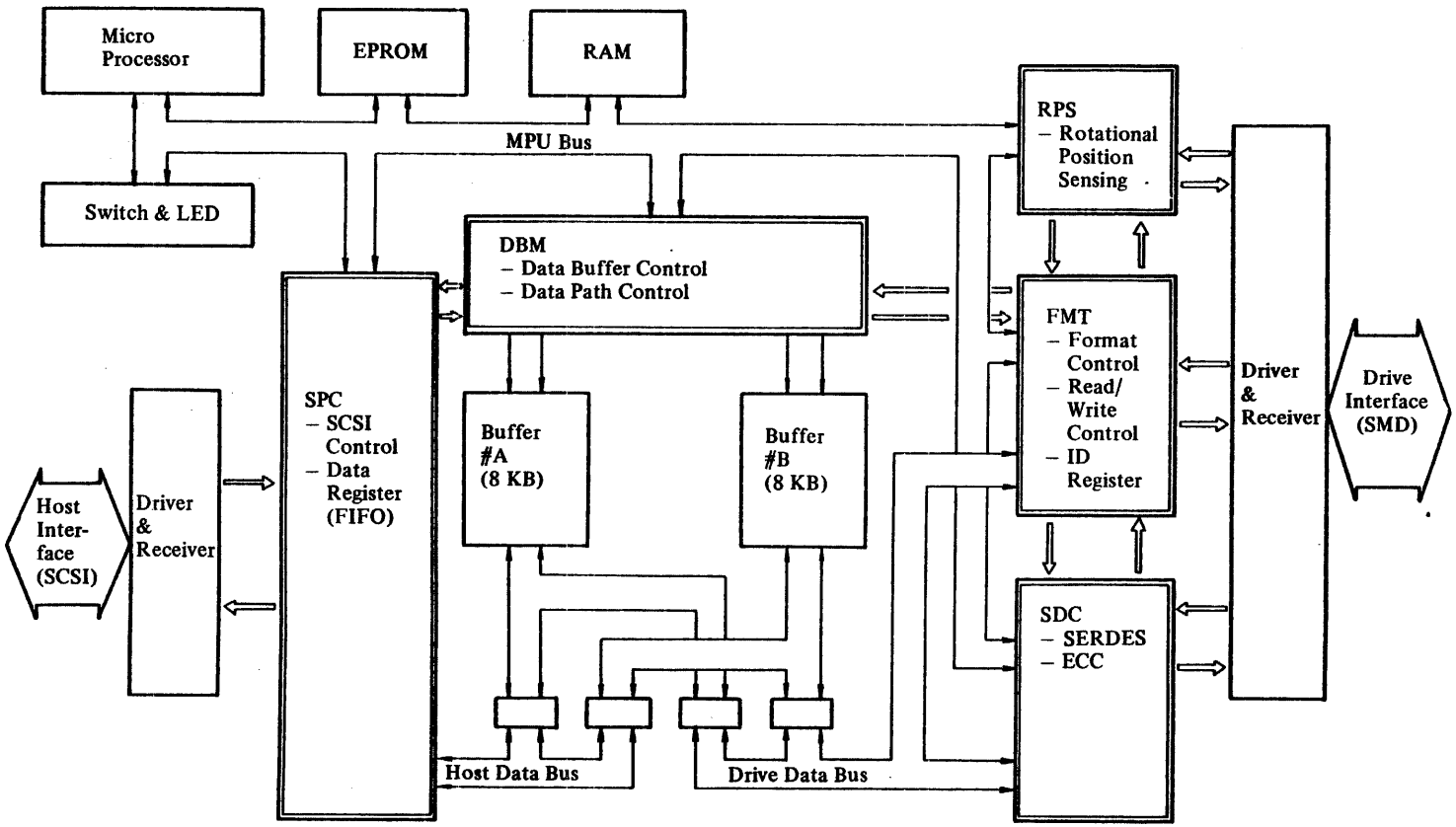


Figure 2.3 IDC circuit configuration

2.2 System Implementation

Up to four drives can be connected to an IDC. The drive interface is based on the SMD interface. The A cable is daisy-chained and the B cables are star-chained.

Host system(s), IDCs, and other SCSI controllers are connected (daisy-chained) to SCSI provided that the total number of connected SCSI devices, including the host system, is a maximum of eight.

The drives to be connected to IDC can vary in type or data format at the user's discretion.

Figure 2.4 shows the system configuration example.

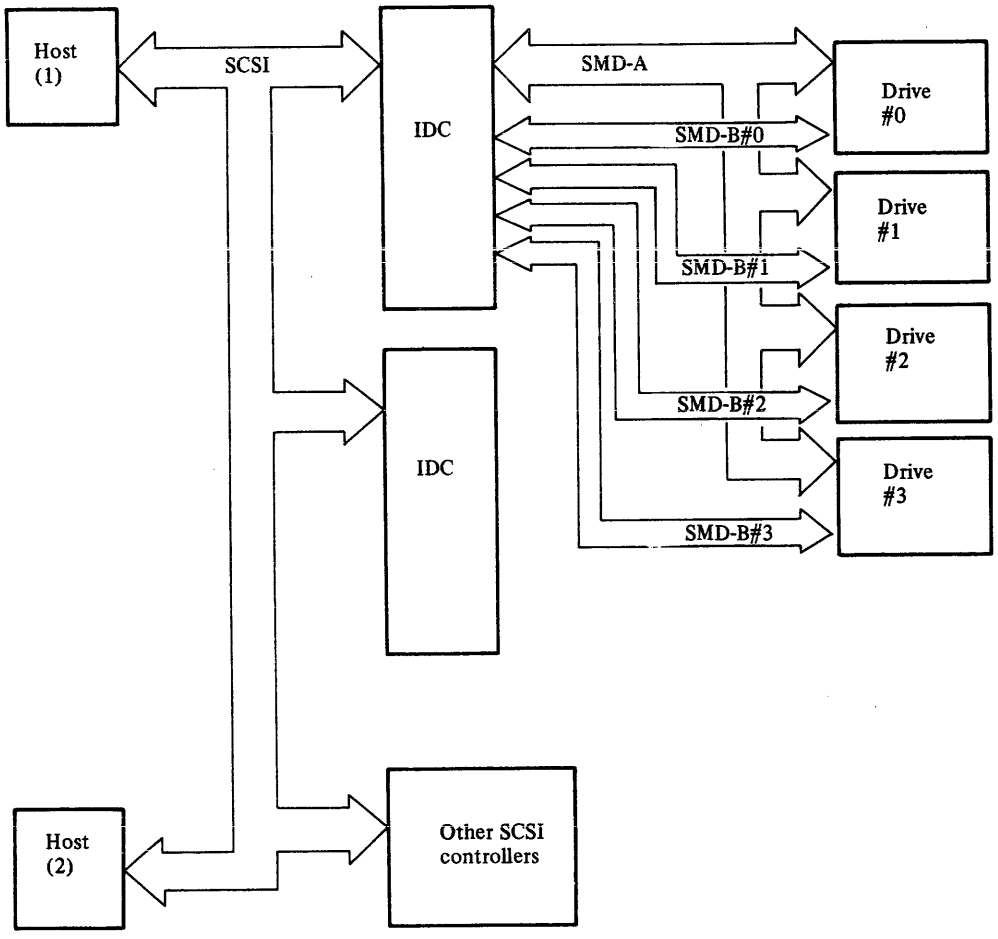


Figure 2.4 System configuration example

2.2.1 Connection of components

(1) Cable connection

Figure 2.5 shows cable connection between the IDC, host system, and drive. Tables 2.1 and 2.2 list the components and recommended parts required for installation.

The drives are numbered #0 to #3 (Drive address) and must be connected corresponding to the locations of B-cable connectors of the IDC.

(IDC B-cable connector)	(Drive address)
SMD-B#0	#0
SMD-B#1	#1
SMD-B#2	#2
SMD-B#3	#3

Total interface cable length must not exeed the following:

Host interface	SCSI	25 m max.
	(See Subsection 3.8.2 for details on cabling requirements.)	
Drive interface	SMD-A	15 m max.
	SMD-B	15 m max.

(2) Terminators

It is necessary to install the terminatiors for host interface and drive interface as described below.

- Host interface (SCSI)

  The terminators must be only installed in sockets on the IDC PCA when the IDC is connected in the beginning or ending position of SCSI cable (Figure 2.6).

- Drive interface (SMD)

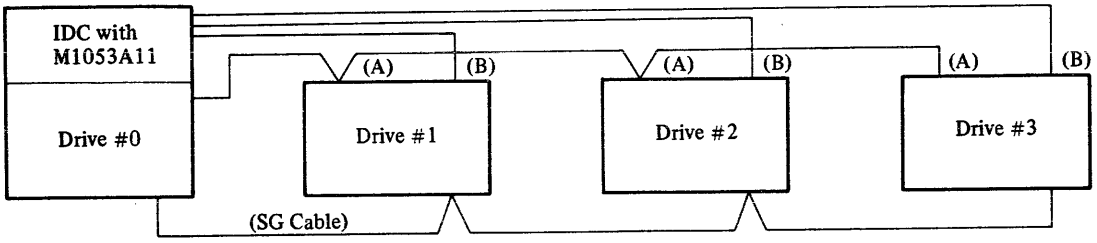
  For the A cable, terminators must be installed on the drive which is connected at the ending position of the cable (Figure 2.7). B cable does not need to install the terminators.

(3) System grounding

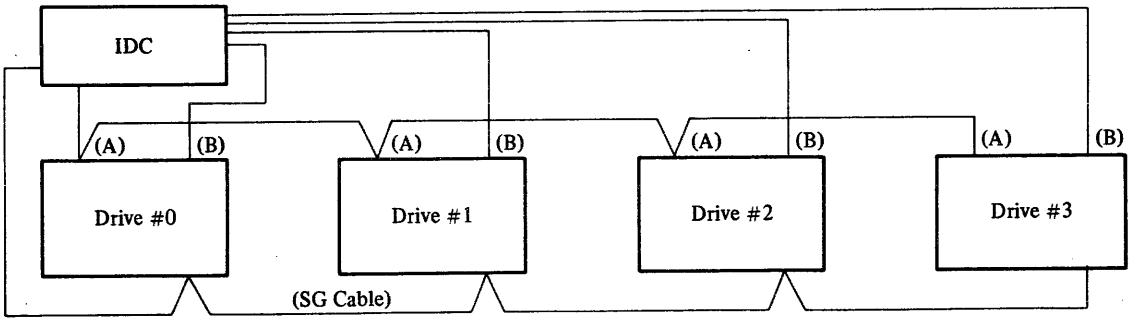
Connect the SG (Signal Ground) cable between the IDC and drives as follows:

- It is unnecessary to connect the SG cable between the IDC and drive on which the IDC is installed with the M1053A11 Mounting frame option. (refer to Subsection 2.2.2.)

  In this case, connect the SG cable between the drive with IDC and next drives.



- When the IDC is not installed on top of the drive with the M1053A11, connect the SG cable between the IDC and the drives. In this case, use one of the mounting holes of IDC PCA (see Figure 2.2) as an SG terminal.

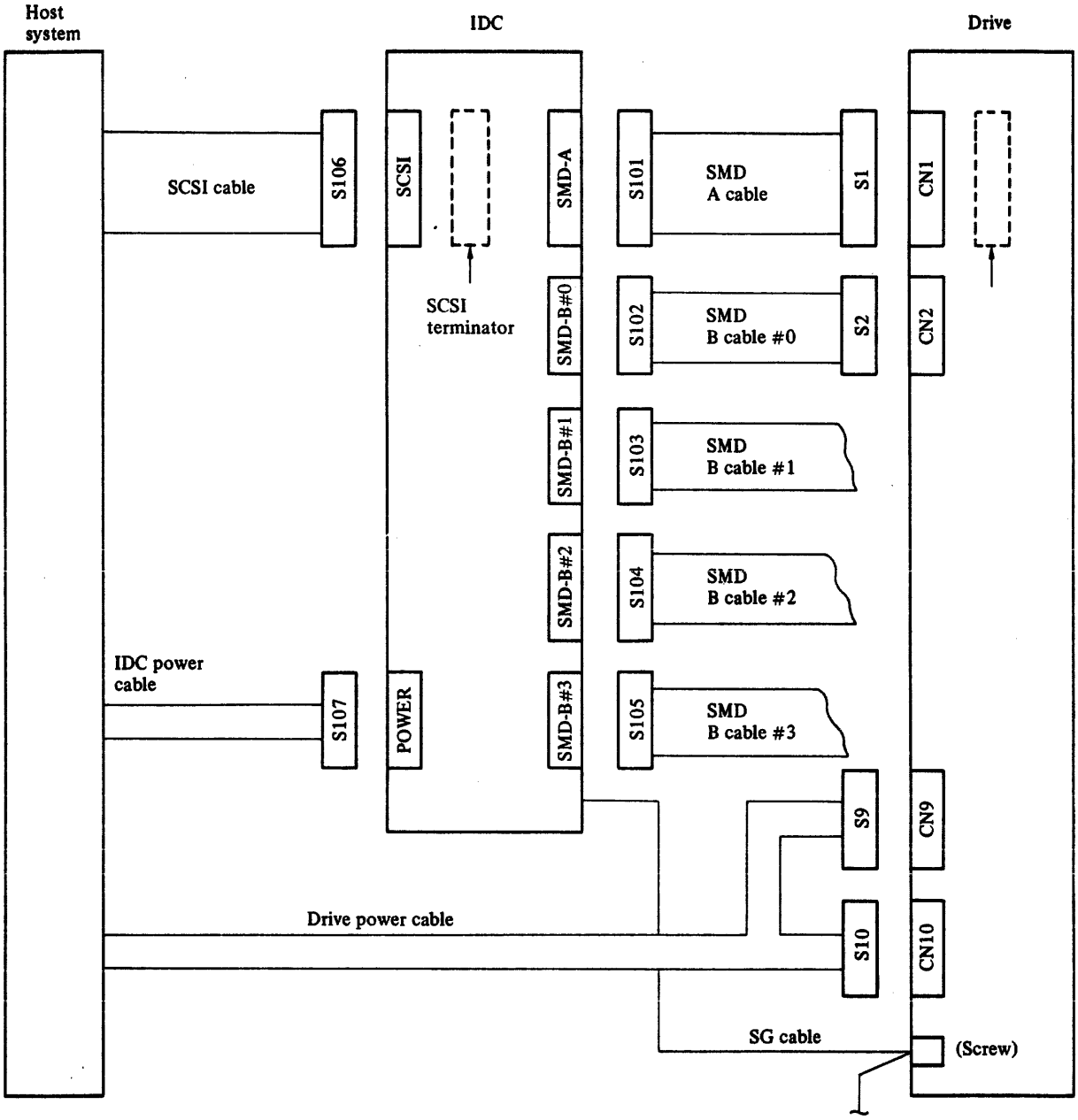


- Use the SG terminal of the drive for the SG cable connection between the drives. (For the location and shape of the SG terminal, refer to the Manual for that drive.)

- The SG cable must be AWG 12 or greater.

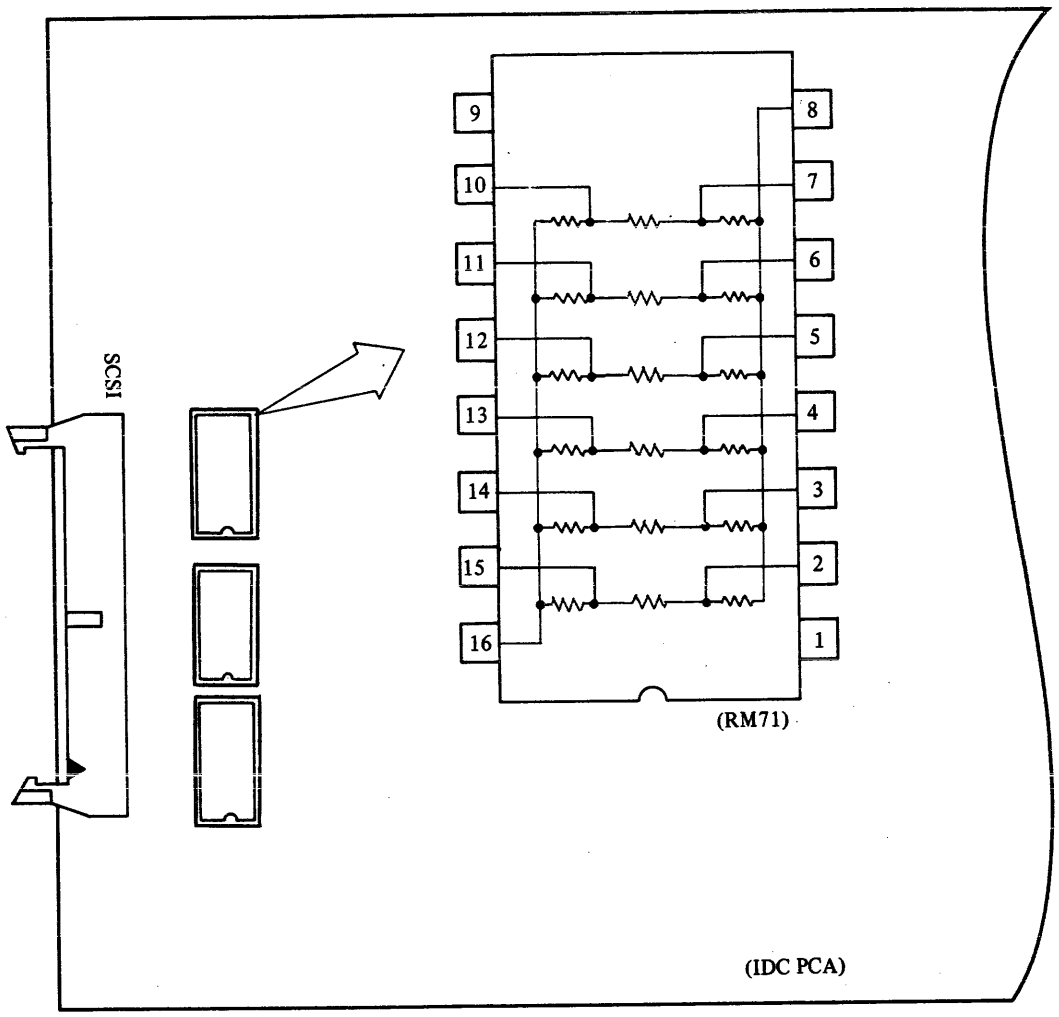
- The SG cable connection between drives, and IDC is a daisy chain connection, and its cable length must be less than 15 m.

Note: All six mounting holes of the IDC PCA (see Figure 2.2) are Signal Ground (SG) terminals.



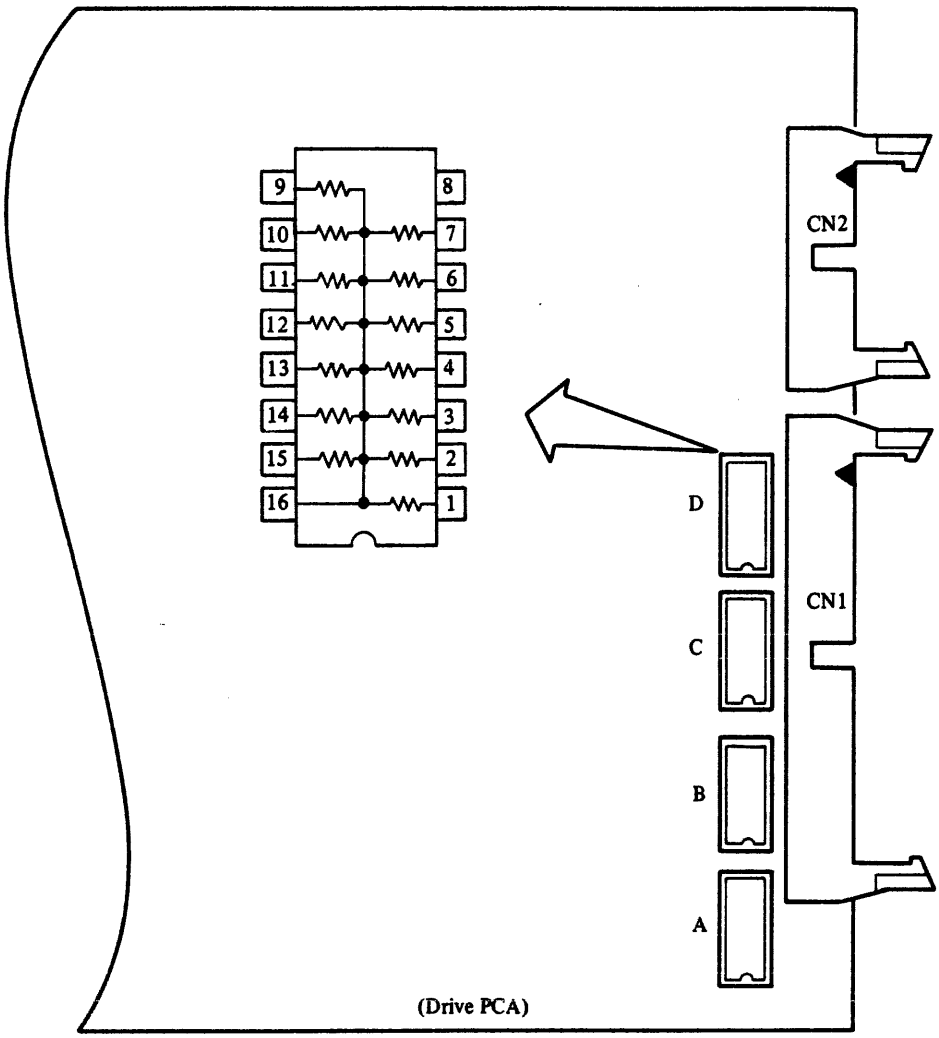
Note: Connector names for a drive may be different than the description in this figure, depending on the drive type. Refer to the Manual for the each drive to be connected for details.

Figure 2.5 Cable connection



Note: Terminators are already installed in IDC at shipment. Remove all terminators if the IDC does not require them.

Figure 2.6 SCSI terminator installation



Notes: 1. Remove all terminators if the device requires no terminators.

2. Connector names and locations and how and where terminators are installed may be different from the description in this figure, depending on the drive type. Refer to the Manual for the each drive to be connected for details.

Figure 2.7 SMD A cable terminator installation (for reference)

Table 2.1 System components

Equipment	Model	Remarks
Intelligent disk controller	M1053BD	
Micro-disk drive	M2331KS	
	M2333KS	
Mounting frame (optional)	M1053A11	Dedicated for installing IDC on top of a drive. (M2333KS/M2331KS only)

Note: See the Appendix C at the end of this manual for options such as power supply unit, fan unit, and cables.

Table 2.2 Recommended parts for installation

Name		Specification	Manufac-turer	Remarks (Figure 2.5)
Host interface (SCSI)	Cable connector (IDC, through-end)	FCN-707J050-AU/O	Fujitsu	S106
	Cable	455-248-50	SPECTRA -STRIP	
Drive interface (SMD)	A cable connector (IDC)	FCN-707J060-AU/B	Fujitsu	S101
	A cable connector (Drive, Through-end)	FCN-707J050-AU/O	Fujitsu	S1
	B cable connector (IDC)	FCN-747J026-AU/O or FCN-707J026-AU/B	Fujitsu	S102~S105
	B cable connector (Drive)	FCN-707J060-AU/B	Fujitsu	S2
	A cable	455-248-60	SPECTRA -STRIP	—
	B cable	174-26 or 3476-26	ANSLEY 3M	— —
IDC power supply	Cable connector	2139-7	Molex	S107
	Contact	2478-GL		
	Key	2560-1		
	Cable	AWG18	—	—
Drive power supply (reference for M2333KS/ M2331KS)	Cable connector	2139-7	Molex	S9, S10
	Contact	2478-GL		
	Key	2560-1		
	Cable	AWG16	—	—

2.2.2 Mounting frame (optional)

(1) Installation

IDC can be directly mounted on top of a drive using M1053A11 optional mounting frame. Figures 2.8 and 2.9 show the external view of on-drive-mounted IDC and the installation procedure.

The drive with or without IDC must be installed in the system to meet the drive installation requirements.

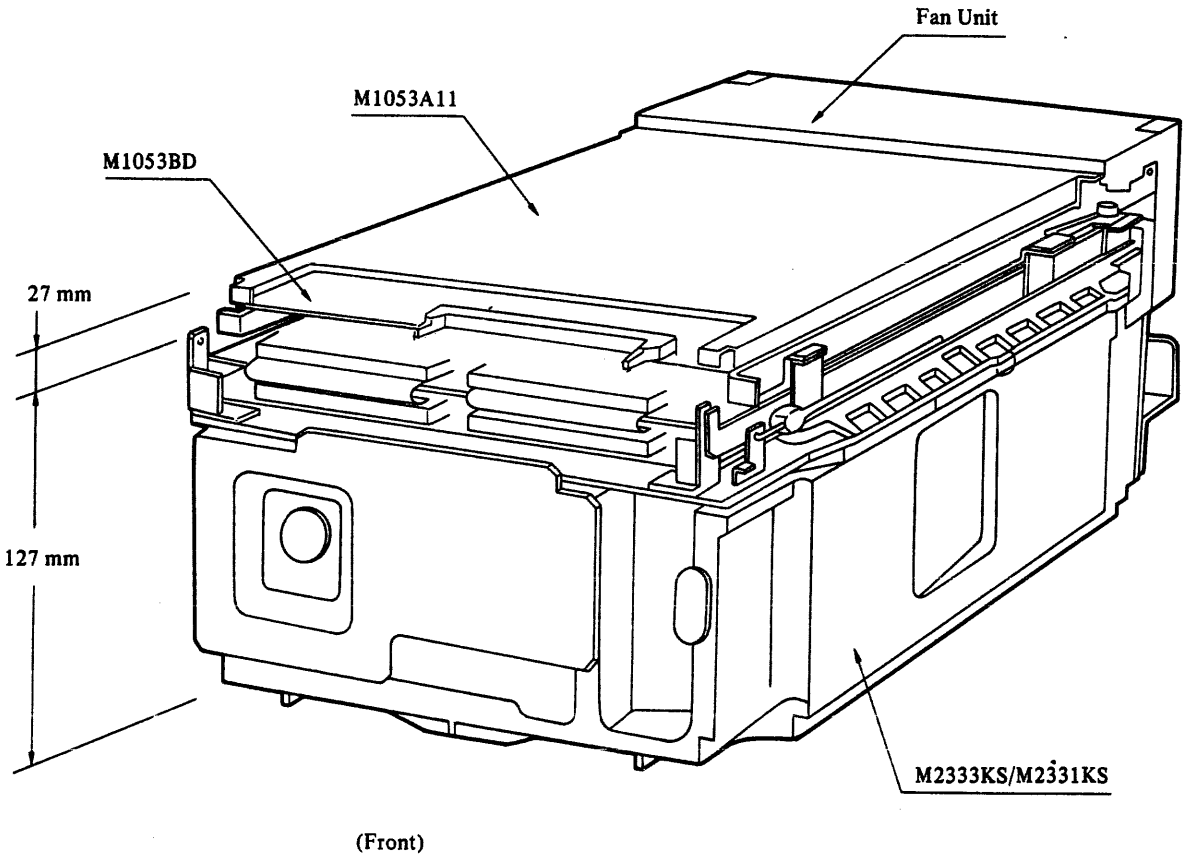


Figure 2.8 Installed IDC on top of drive

(a) Mounting the PCA to the frame

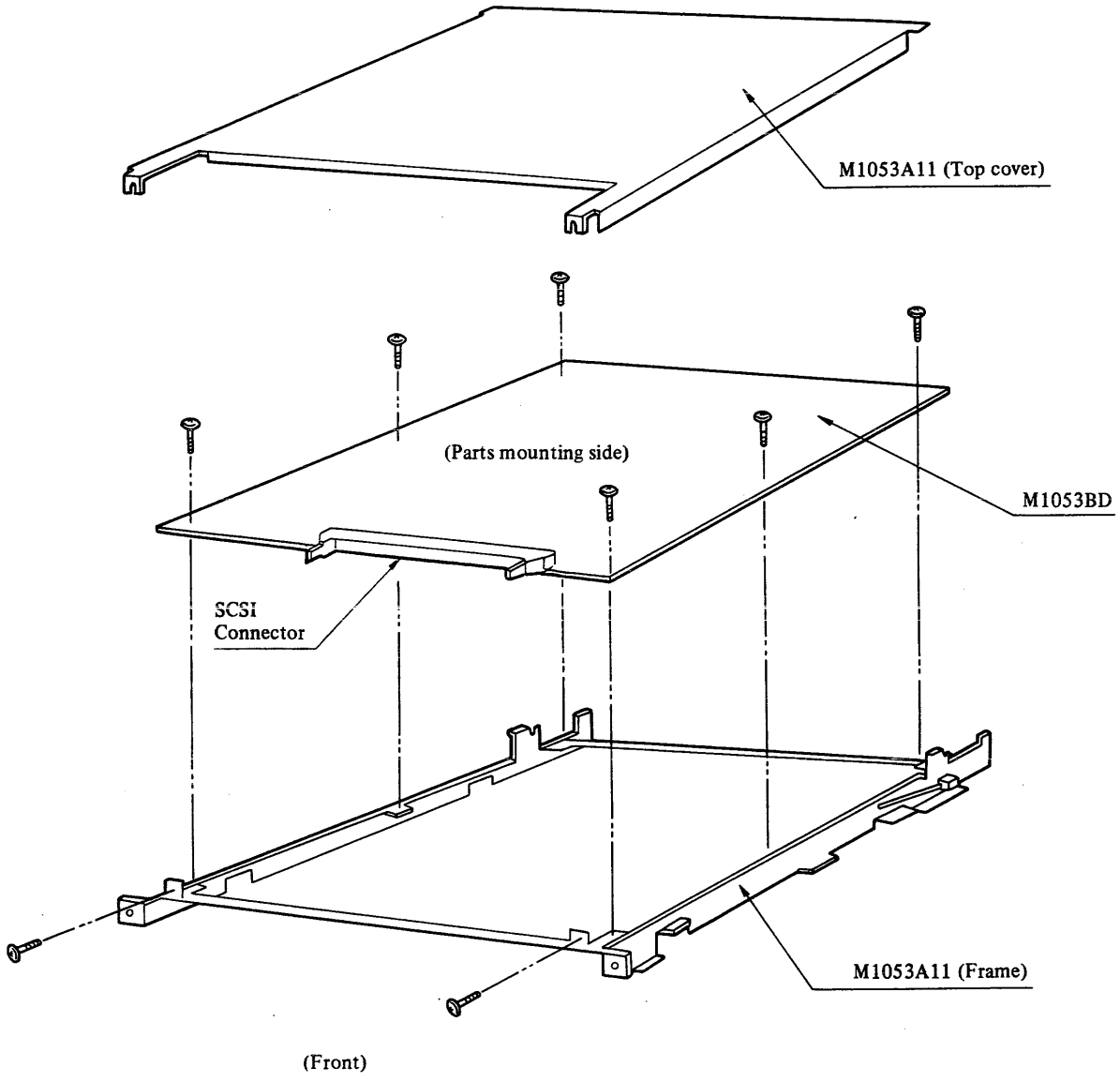
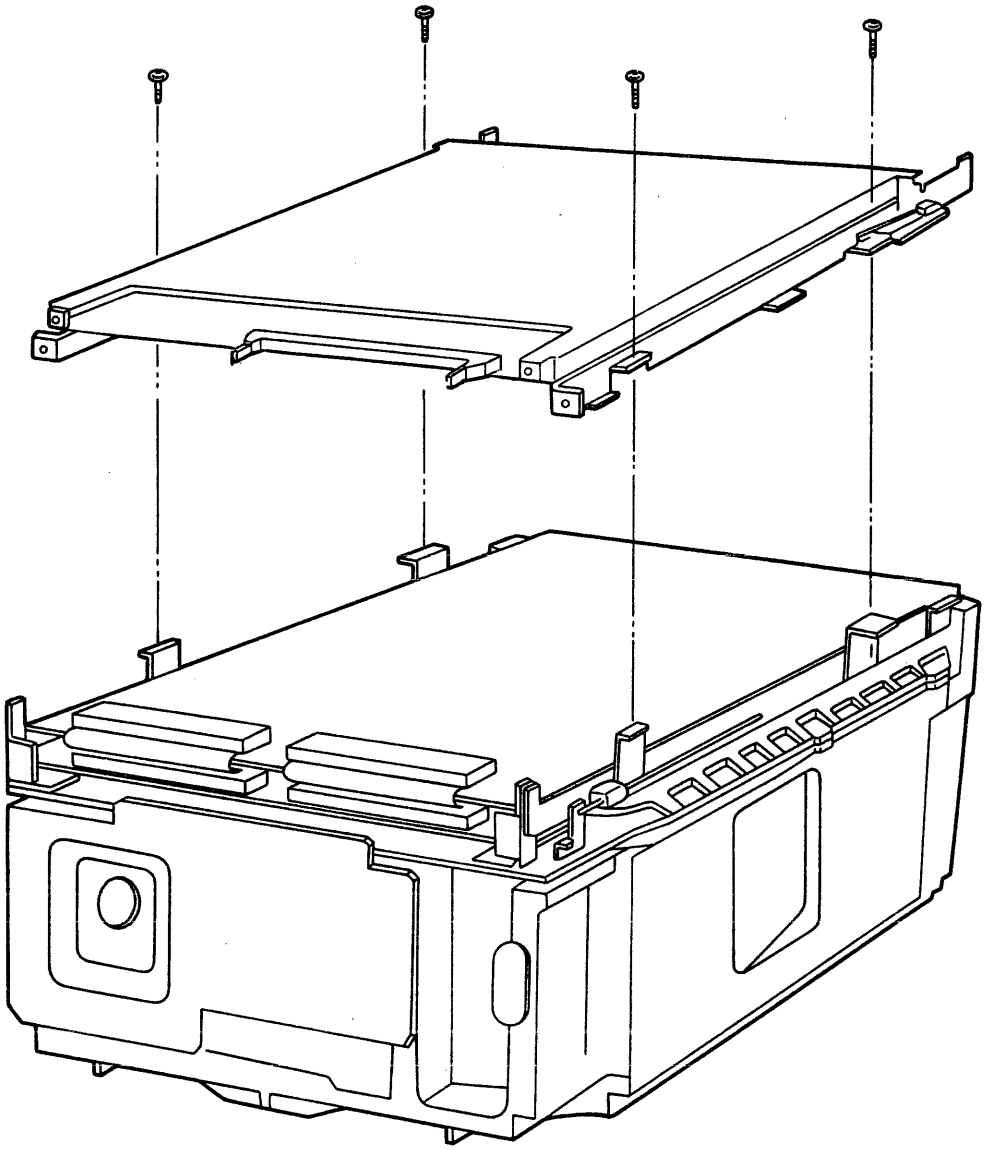


Figure 2.9 Installation procedure for mounting frame (1/2)

(b) Attaching the IDC on top of the drive



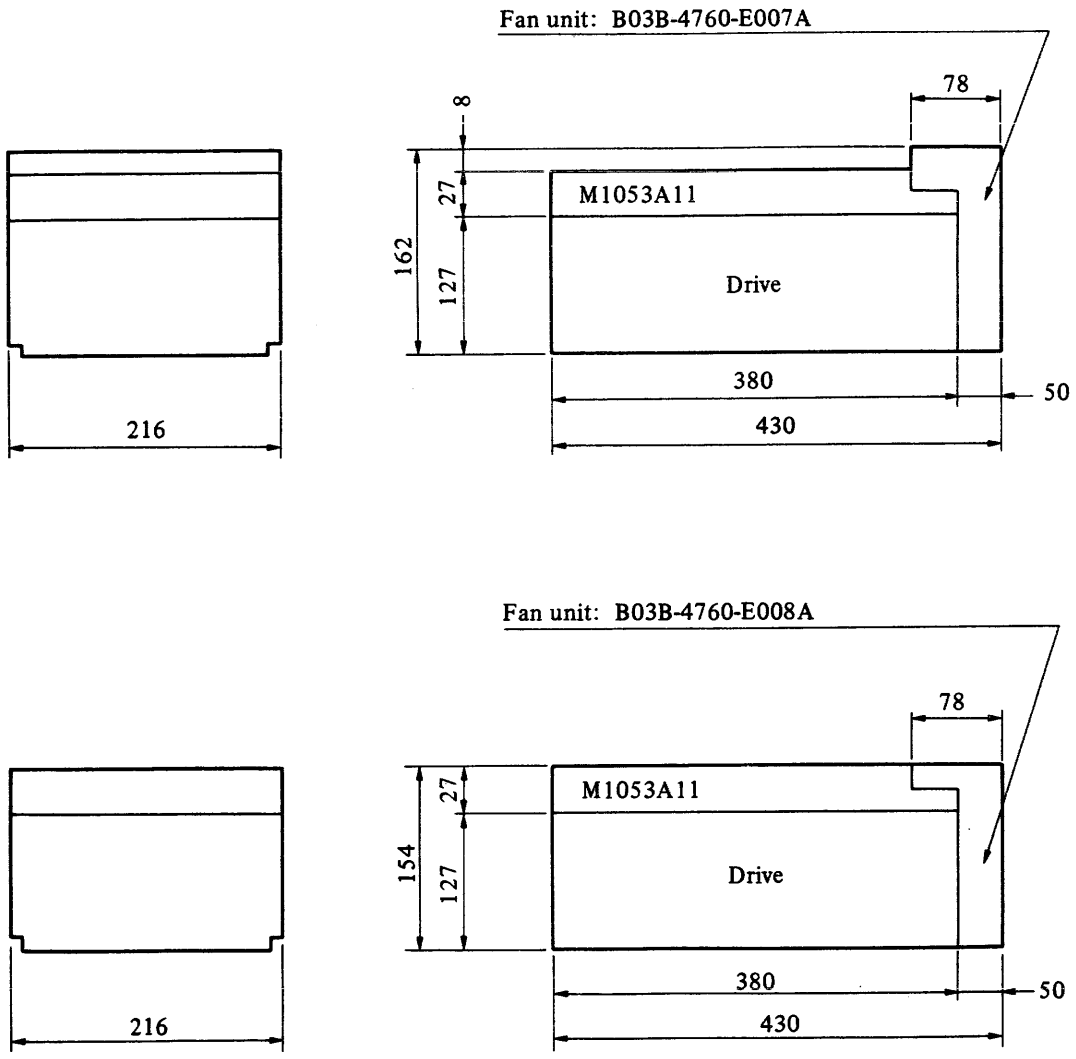
(Front)

Note: Remove the top cover of the drive. This cover is not used when an IDC is mounted on the drive.

Figure 2.9 Installation procedure for mounting frame (2/2)

(2) Outer dimensions

Figure 2.10 shows the outer dimensions when the IDC is installed on top of the drive. For installing the drive into a system, refer to the Manual for the drive.



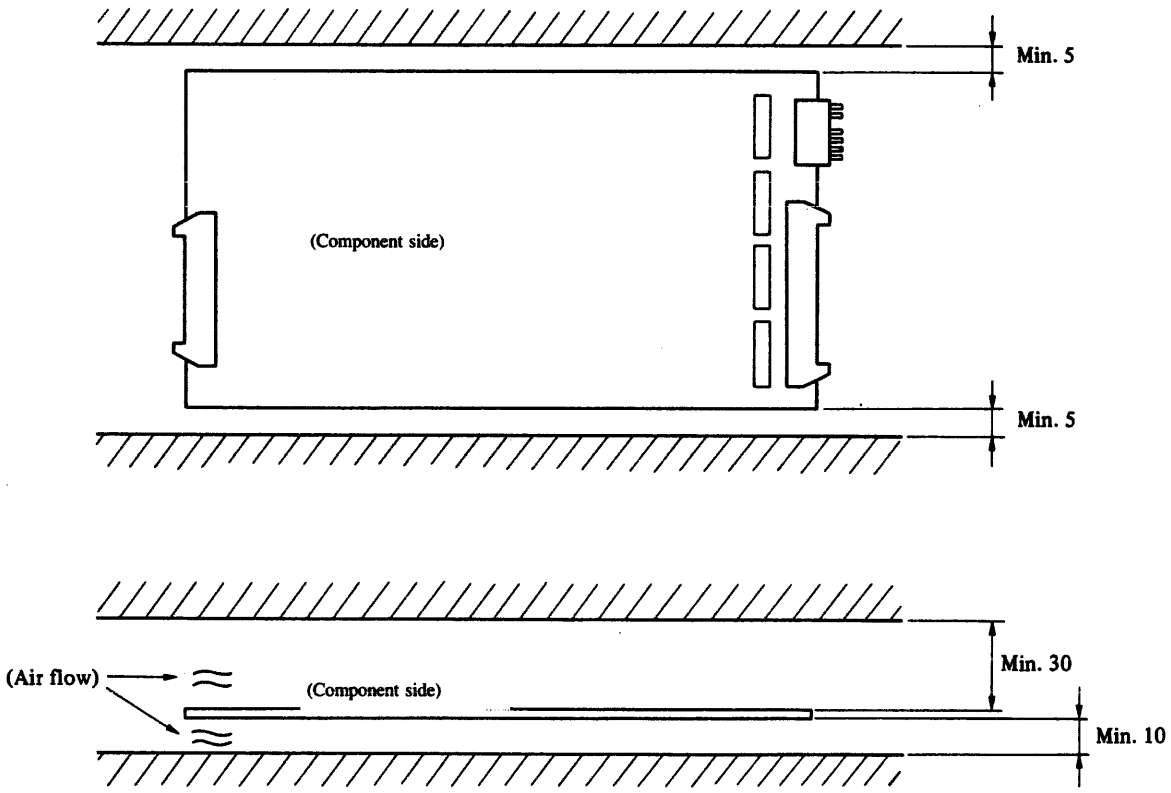
Notes: 1. Unit: mm
2. For the optional fan unit, refer to Appendix C.

Figure 2.10 Mounting dimensions

2.2.3 PCA installation requirements

If the IDC PCA is installed in a system cabinet without utilizing the optional M1053A11 mounting frame, spacing requirements shown in Figure 2.11 must be satisfied. Also, the following items must be considered.

- Mounting holes of the PCA are SG terminals (See and Figure 2.2).
- Cooling requirements (See Subsection 2.4)
- No cable shall touch the components on the PCA or soldering side of the PCA.



Note: Unit: mm

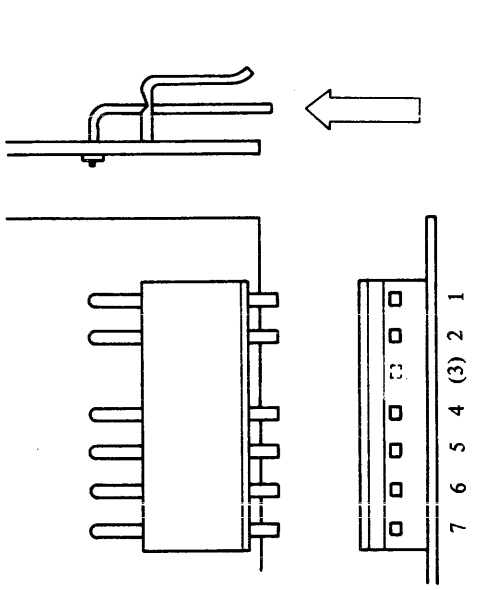
Figure 2.11 PCA installation requirements

2.3 Power Requirements

2.3.1 IDC power requirements

(1) Power connector

Figure 2.12 shows IDC power connectors and pin assignment.



PIN	Type
1	−12V
2	0V
3	(key)
4	0V
5	0V
6	+5V
7	+5V

Figure 2.12 Power connector pin assignments

(2) Power requirements

Power requirements:	+5 VDC ±5% (at the IDC)	5.0 A max.
	−12 VDC ±5% (at the IDC)	1.0 A max.

Power consumption: 39 W max.

2.3.2 Power supply sequence

(1) Supplying power to IDC

The power supply sequence between +5 VDC and −12 VDC for IDC must follow the requirements shown in Figure 2.13 (a).

(2) Between IDC and disk drive

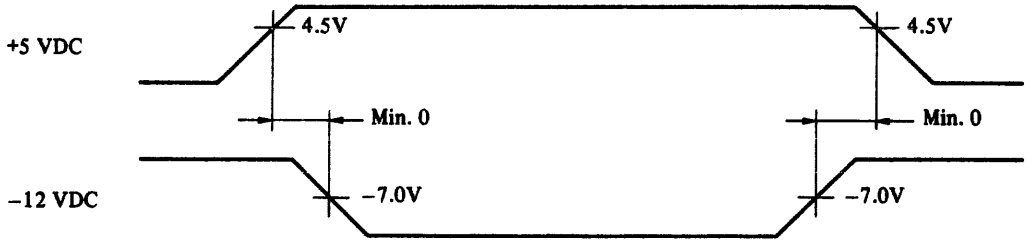
The power supply sequence between IDC and the drive need not be considered.

(3) Between host system and IDC

The power supply sequence between +5 VDC for SCSI connection circuits of the host system and +5 VDC for IDC is determined as follows:

- Follow the power supply sequence shown in Figure 2.13 (b) if the TERMPWR pin (SCSI connector) which supplies power to the terminator is not used.
- Follow the power supply sequence shown in Figure 2.13 (b) if the host system is not equipped with noise suppression feature which avoids noise to SCSI when power of the host is turned on or off.
- In cases other than above, the power supply sequence need not be considered.

(a) +5 VDC and −12 VDC for IDC



(b) +5 VDC for IDC and host system

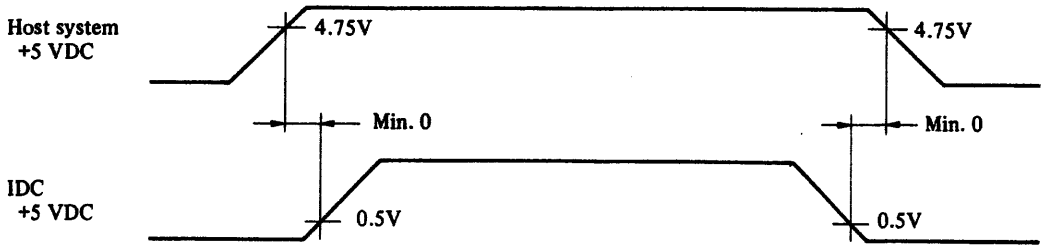


Figure 2.13 Power supply sequence

2.4 Cooling Requirements

The IDC PCA cannot be used without air circulation. A fan must be mounted inside the cabinet to generate air circulation on the surface of PCA.

Measure the surface temperature of IC mounted on PCA to determine whether the IDC is adequately cooled. The surface temperature of the device listed in Table 2.3 must not exceed the maximum value.

Table 2.3 Cooling requirements

Parts	Upper temperature limit	Remarks
MB114T026	Package surface temperature 70°C	PGA 64 pin LSI
8086-2	Package surface temperature 70°C	DIP 40 pin MPU

Note: The temperature shall be measured at center of the package surface.

2.5 IDC Setting Switches and LED Indicators

The IDC PCA is equipped with operational mode and SCSI ID setting DIP switches, a diagnostic program starting toggle switch, and LED indicators, as shown in Figure 2.14.

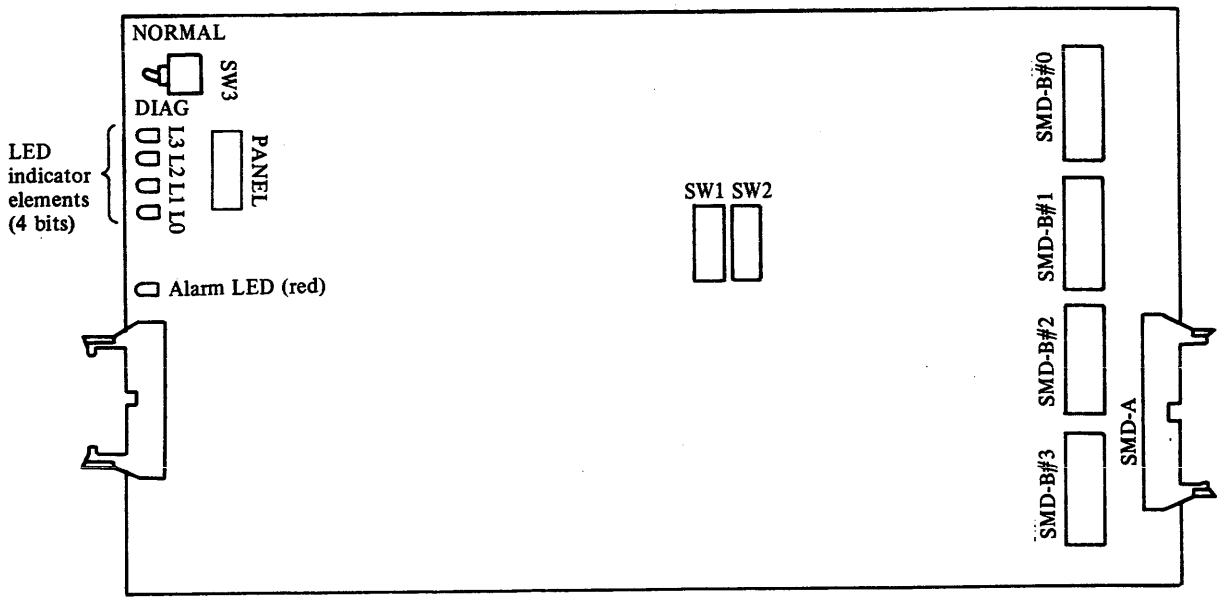


Figure 2.14 IDC switches and LED Indicators

2.5.1 IDC SCSI ID and operational mode (SW1)

SW1 is an 8-key DIP switch (keys 1 to 8) allowing the address (SCSI ID) of IDC and operational mode to be set.

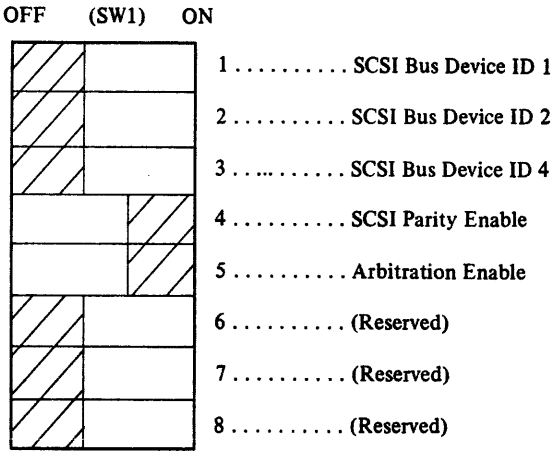


Figure 2.15 IDC SCSI ID/Operational mode setting switch

(1) IDC SCSI ID

The Bus Device ID of an IDC shall be set according to Table 2.4. Note the following points when setting an IDC SCSI ID:

- A specified ID must be unique on the SCSI bus.
- Priority in the Arbitration phase ascends in numerical order:
  7 > 6 > ..... > 1 > 0.

Table 2.4 IDC SCSI ID setting

IDC SCSI Bus Device ID	KEY		
	3	2	1
0	OFF	OFF	OFF
1	OFF	OFF	ON
2	OFF	ON	OFF
3	OFF	ON	ON
4	ON	OFF	OFF
5	ON	OFF	ON
6	ON	ON	OFF
7	ON	ON	ON

(2) SCSI parity option

This option specifies whether to enable or disable the SCSI data bus parity bit check facility, as shown in Table 2.5.

Table 2.5 SCSI parity check option setting

SCSI data bus parity check	KEY 4
Disable: IDC does not execute parity check	OFF
Enable: IDC executes a parity check	ON

(3) Arbitration option

This option specifies whether to enable or disable the Arbitration phase in SCSI according to Table 2.6. If the Arbitration phase is disabled, the Disconnect/ Reconnect function on SCSI is inhibited.

Table 2.6 Arbitration option setting

Arbitration phase	KEY 5
Disable	OFF
Enable	ON

(4) Keys 6 to 8

Keys 6, 7, and 8 are reserved for future definition. These keys must be set to 'OFF'.

2.5.2 SW2 (reserved)

SW2, 8-bit DIP switch, is reserved for future use. All keys of the SW2 must be set to 'OFF' position as shown in Figure 2.16.

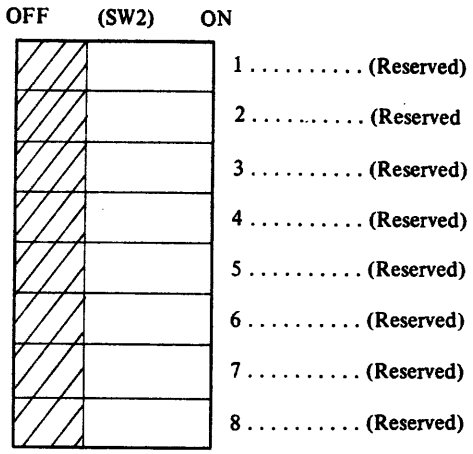


Figure 2.16 SW2 (reserved)

2.5.3 Diagnostic switch (SW3)

Toggle switch SW3 activates the IDC self-diagnostic programs. Setting this switch to 'DIAG' position causes the IDC to enter self-diagnostic mode and to test the IDC and disk drive(s) attached to it. See Chapter 9 for details about test items.

The IDC does not respond to the Selection or Reselection from SCSI during diagnosis.

Diagnostic operations are repeated until the switch is returned to the 'NORMAL' position, and the diagnostic results are indicated by the 4-bit LED indicator on the PCA.

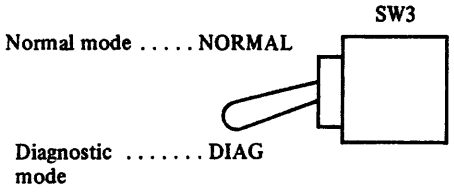


Figure 2.17 Diagnostic switch

2.5.4 LED indicators

(1) Status indicators

The 4-bit status indicator (L3 to L0) indicates the IDC operation status and results of diagnosis.

Table 2.7 lists combinations of the four bits and their corresponding states. Each LED indicator element turns on for '1' and turns off for '0'.

Table 2.7 Status indication and meaning

L3	L2	L1	L0	IDC state
0	0	0	0	Operating
0	0	0	1	Idle (IDC ready)
0	0	1	0	(Undefined)
0	0	1	1	In diagnosis
0	1	×	×	An error has been detected during the IDC hard core test: (L1) (L0) 0 0 ROM error 0 1 RAM error 1 0 Register error 1 1 Buffer error
1	0	×	×	An error has been detected while diagnosing a device: (L1) (L0) 0 0 Device #0 error 0 1 Device #1 error 1 0 Device #2 error 1 1 Device #3 error
1	1	0	0	(Undefined)
1	1	0	1	
1	1	1	0	
1	1	1	1	IDC hardware error was detected.

(2) Alarm LED

The red LED which is mounted near SCSI connector is an alarm LED for SCSI cable connection. If a single-ended SCSI connector is inadvertently attached, this LED turns on. In this case, all SCSI driver circuits of the IDC are disabled immediately.

When this LED lights, turn the system power off, then check the SCSI cable connection.

2.5.5 PANEL connector

PANEL connector enables the status indicator and the diagnostic switch (SW3) to be installed outside the IDC.

Figure 2.18 is signal assignments on PANEL connector. Figure 2.19 shows an example of an external circuit.

▶	01	G	02	$\overline{\text{DIAG}}$
	03	G	04	(Key)
	05	G	06	$\overline{\text{L3}}$
	07	G	08	$\overline{\text{L2}}$
	09	G	10	$\overline{\text{L1}}$
	11	G	12	$\overline{\text{L0}}$
	13	G	14	(Open)
	15	(Open)	16	(Open)
	17	(Open)	18	+5 V DC
	19	(Open)	20	+5 V DC

G : Ground

+5 V DC : +5 V DC power supply pin

Figure 2.18 PANEL connector signal assignments

(1) Pin 02: $\overline{\text{DIAG}}$ (Input)

This is an input pin for activation of the IDC self-diagnostic programs.

Setting this pin to the 'L' level is equivalent to setting diagnostic switch SW3 in IDC to 'DIAG' position. If an external panel is connected, IDC is set to self-diagnostic mode by either SW3 or this input pin setting. If SW3 is set to 'NORMAL' position and this input pin is open, IDC is returned to normal mode.

(2) Pins 06, 08, 10, 12: $\overline{\text{L3}}$ to $\overline{\text{L0}}$ (Output)

These output pins externally indicate the same states as the 4-bit status indicator on the PCA.

The open-collector buffer circuits are provided for these signals and each signal is true when driven to the 'L' level. Their driving capability are 72 mA in maximum I_{OL} for each signal.

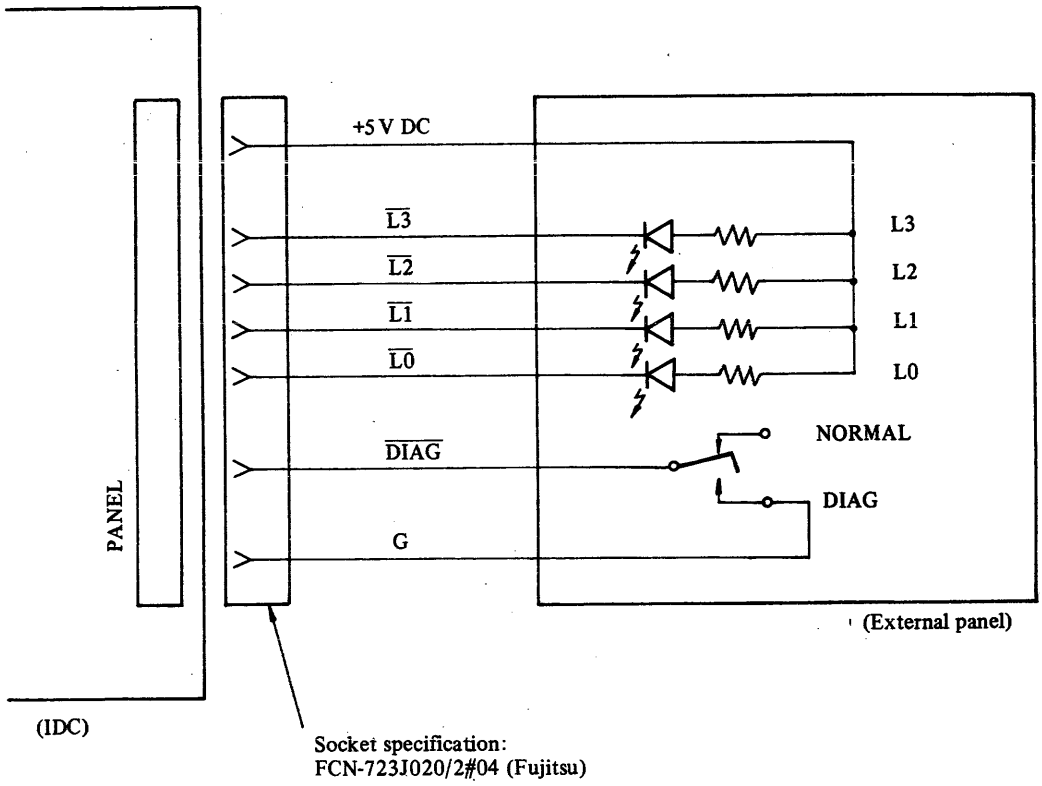


Figure 2.19 Example of external panel circuit

2.6 Disk Drive Setting Switches (for reference)

The disk drive has several setting switches to allow configuration for the best operating conditions. The following explains how to set the switches to connect each disk drive to an IDC.

2.6.1 M2333KS/M2331KS

Figure 2.20 shows the switch locations on the KGFM PCA. SW1 (Figure 2.21) must be set for the disk drive address, device type, and operational mode, and SW2 and SW3 (Figure 2.22) must be set for the sector size.

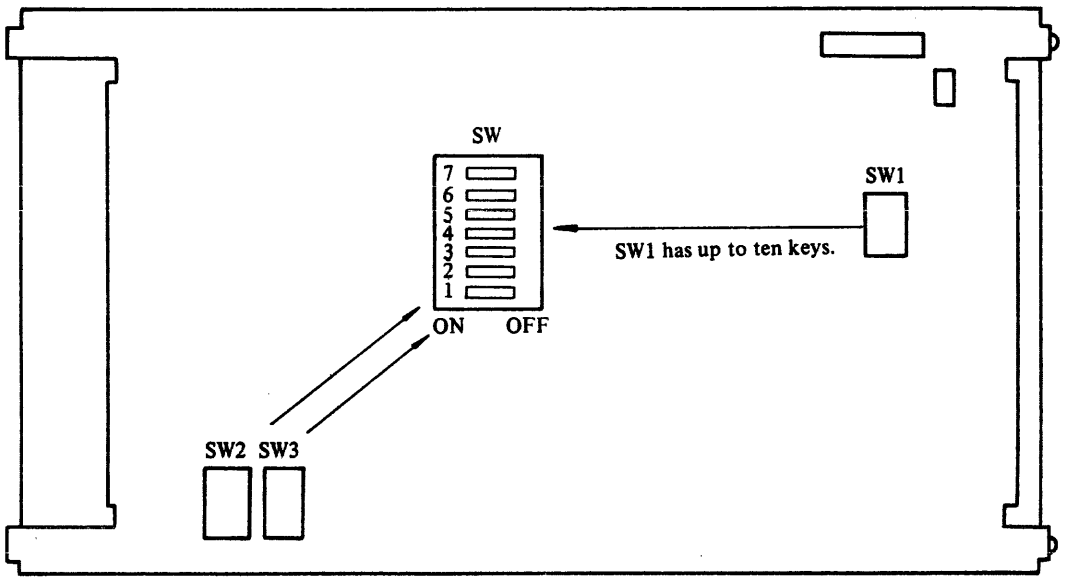


Figure 2.20 Setting switch locations (M2333KS/M2331KS)

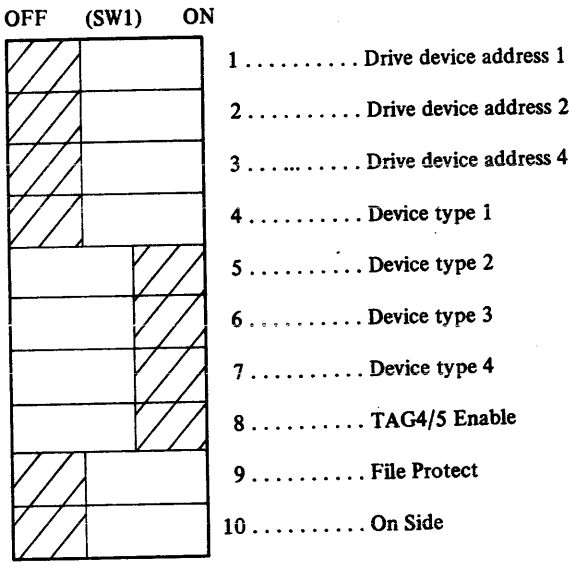


Figure 2.21 Drive address/type mode setting switch (M2333KS/M2331KS)

(1) Drive address

Keys 1 to 3 of SW1 enables a drive address to be set within the range of 0 to 3 according to Table 2.8.

Table 2.8 Drive address setting (M2333KS/M2331KS)

Drive Address	KEY		
	3	2	1
0	OFF	OFF	OFF
1	OFF	OFF	ON
2	OFF	ON	OFF
3	OFF	ON	ON

(2) Device type

Keys 4 to 7 of SW1 enables one of the device type listed in Table 2.9 to be set.

Table 2.9 Device type setting (M2333KS/M2331KS)

Device type	KEY			
	7	6	5	4
M2333KS	ON	ON	ON	OFF
M2331KS	ON	ON	OFF	OFF

(3) TAG 4/5 operational mode

Set key 8 of SW1 to 'ON' to enable TAG 4/5 to operate at the drive interface.

Table 2.10 TAG 4/5 setting (M2333KS/M2331KS)

TAG 4/5	KEY 8
Disable	OFF
Enable	ON

(4) FILE PROTECT switch

Key 9 of SW1 enables all write operation on a disk medium to be inhibited/enabled. Normally set this switch to 'OFF'.

Table 2.11 FILE PROTECT switch (M2333KS/M2331KS)

File protect	KEY 9
Write enable	OFF
Write inhibit	ON

(5) Installation type

Set key 10 of SW1 as to disk drive installation orientation see Table 2.12.

Table 2.12 Installation type setting (M2333KS/M2331KS)

Installation Method (*)	KEY 10
Horizontal installation	OFF
Vertical installation	ON

*: Refer to the M2333KS/M2331KS Manual.

(6) Sector size

SW2 and SW3 set the physical sector length depending on the data format used, as shown in Figure 2.22. These switches have been set to conform to the data format of the corresponding disk drive for shipment and must not be re-set for other data formats by the user.

Data format (data length)	Format denotation	SW3 KEY							SW2 KEY						
		7	6	5	4	3	2	1	7	6	5	4	3	2	1
		16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	1
256 Bytes	S1	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF
512 Bytes	S2	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF
1,024 Bytes	S3	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF

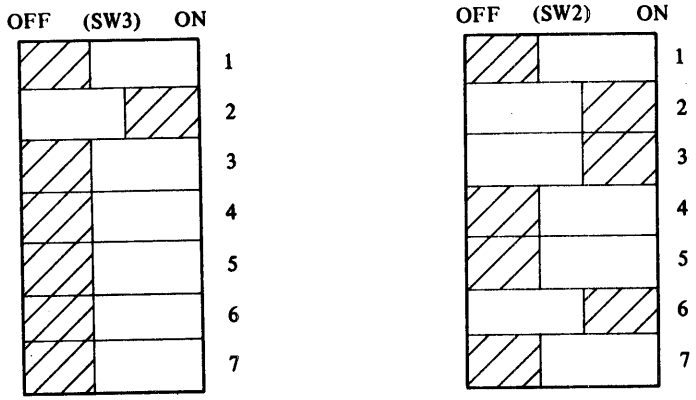


Figure 2.22 Sector size selection switches (M2333KS/M2331KS)

2.7 Initialization of Disk Drives

At the installation time, it is not necessary to initialize the disk drive if the sector interleaving feature is not used, because the disk drives listed in Tables 1.2 and 1.3 are already initialized (formatted) with no sector interleaving at shipment.

If it is required to use the sector interleaving, the disk drives must be initialized (formatted) according to the following procedure at installation.

(1) Connect the IDC and the disk drive to be formatted to the system as described in Section 2.2.

(2) Issue a Format Unit command specifying the disk drive. Figure 2.23 shows the CDB of the Format Unit command for initialization at installation. Specify the interleaving factor used in the system (Byte 4).

	Bit 7	6	5	4	3	2	1	0
BYTE 0	0	0	0	0	0	1	0	0
1	LUN			0	0	0	0	0
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	Interleaving Factor							
5	0	0	0	0	0	0	0	0

Figure 2.23 Format Unit command for initializing

The disk drive is initialized with the specified interleaving factor, and the alternate block assignment for the medium defects is performed according to the Primary Defect list.

CHAPTER 3 HOST INTERFACE

3.1 Terminology

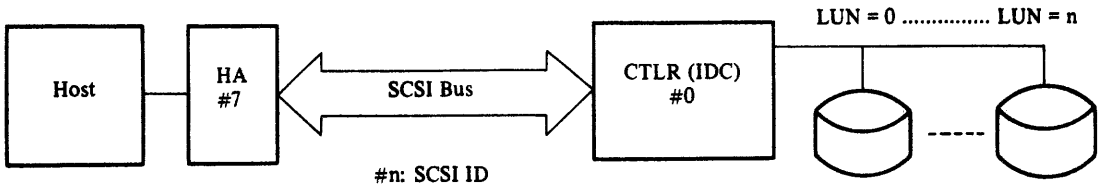
Bus Device or SCSI Device	Generic name for a host adapter or a peripheral controller attached to the SCSI bus.
Initiator (INIT)	An SCSI device that initiates an operation via the SCSI bus.
Target (TARG)	An SCSI device that performs an operation initiated by an INIT.
Unit	The unit of a peripheral device which is explicity accessible via the SCSI bus through a TARG.
Command Descriptor Block (CDB)	A block of data which specifies the command. The CDB is transferred from INIT to TARG.
Status	One byte of information transferred from a TARG to an INIT upon completion of each command.
Logical unit number (LUN)	Indicates an encoded three-bit identifier for the unit as well as the unit itself.
Bus Device ID or SCSI ID	An unique address assigned to an SCSI Device to identify each SCSI Device on the SCSI bus. The value is unique to each SCSI Device, ranges form 0 to 7, and is assigned in correspondence with the SCSI data bus bit.

Note: In the descriptions of the host interface protocol, the IDC may be referred to as TARG depending on the operation. However, in the place where the distinction is necessary, 'IDC' is used instead of that SCSI term.

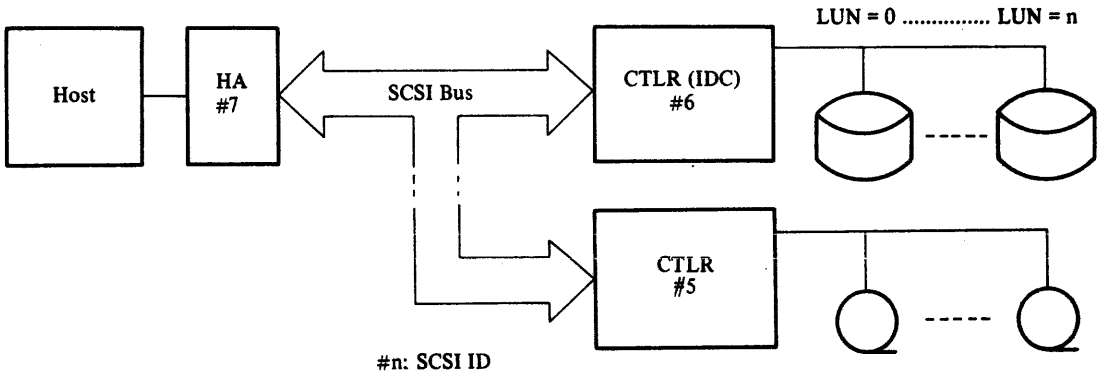
3.2 System Configuration

Up to eight SCSI devices can be connected to the SCSI bus. Figure 3.1 shows sample system configuration.

(1) Single INIT, Single TARG



(2) Single INIT, Multi TARG



(3) Multi INIT, Multi TARG

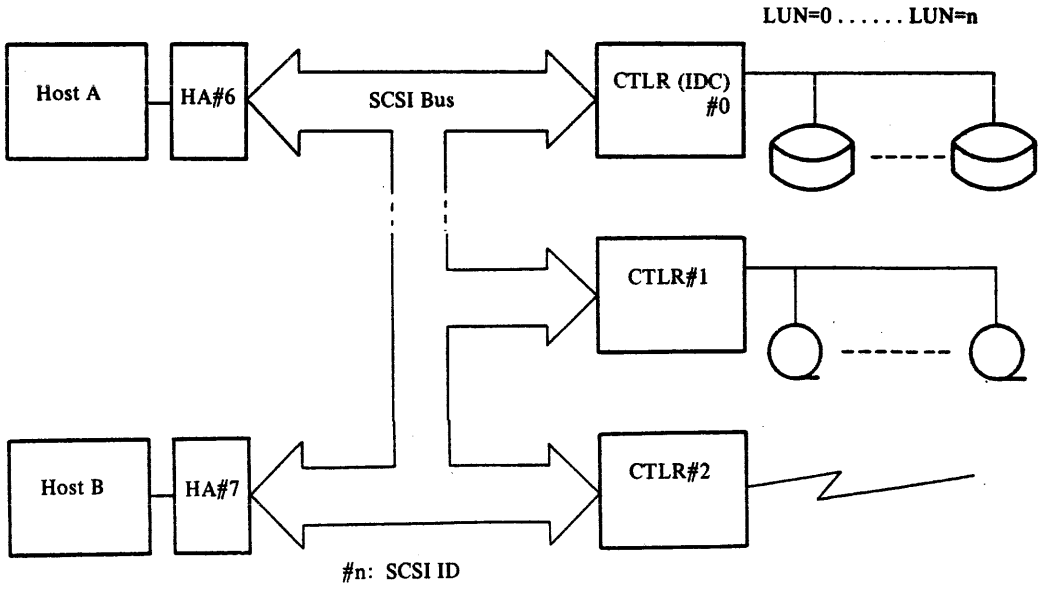


Figure 3.1 Example of SCSI configuration

3.3 Interface Signals

Figure 3.2 shows interface signal lines and Figure 3.3 shows the connector pin assignments.

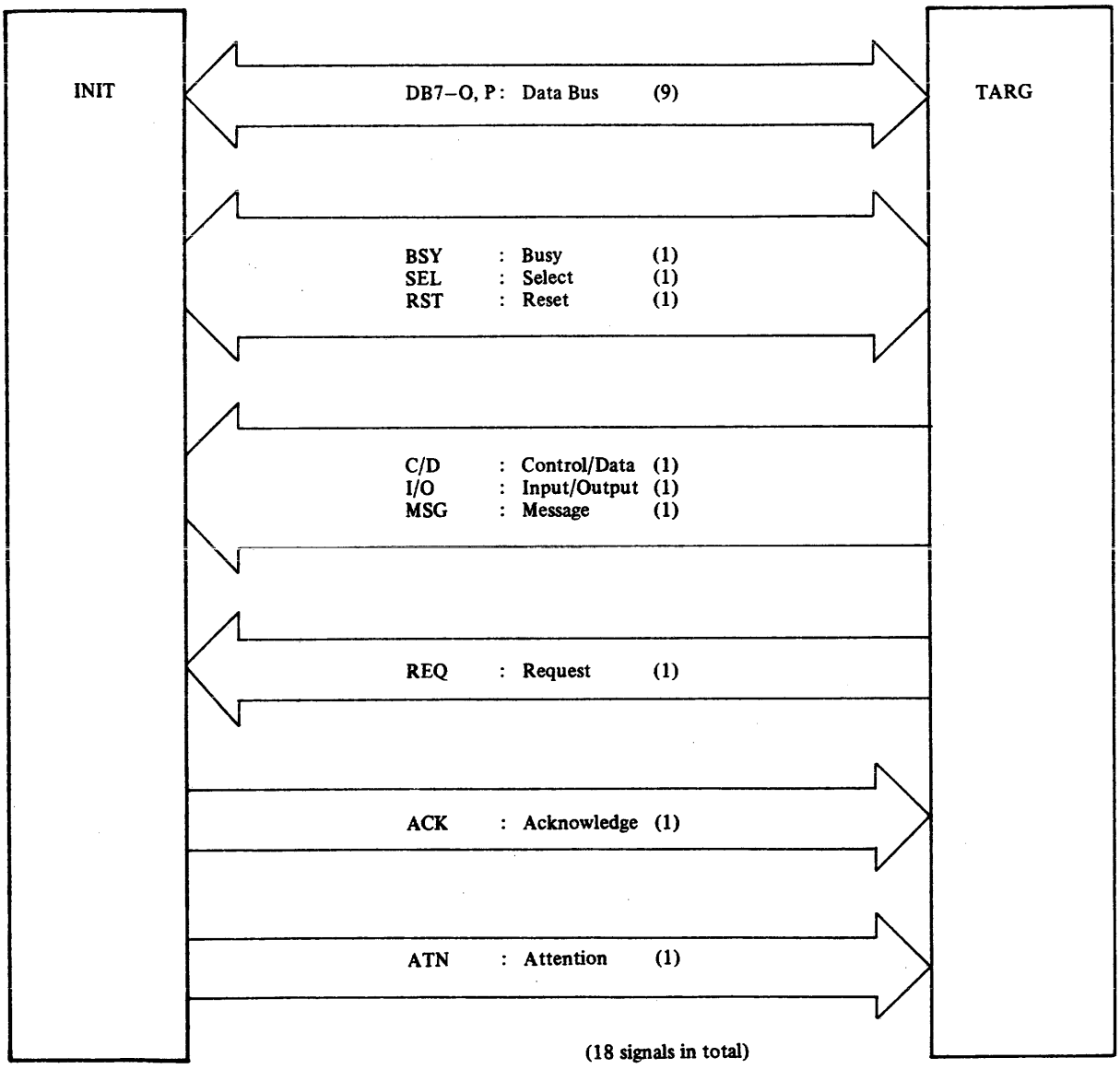


Figure 3.2 Host interface signals

01	(Open)	G	02
03	+DB0	−DB0	04
05	+DB1	−DB1	06
07	+DB2	−DB2	08
09	+DB3	−DB3	10
11	+DB4	−DB4	12
13	+DB5	−DB5	14
15	+DB6	−DB6	16
17	+DB7	−DB7	18
19	+DBP	−DBP	20
21	DIFFSENS*1	G	22
23	G	G	24
25	TERMPWR*2	TERMPWR*2	26
27	G	G	28
29	+ATN	−ATN	30
31	G	G	32
33	+BSY	−BSY	34
35	+ACK	−ACK	36
37	+RST	−RST	38
39	+MSG	−MSG	40
41	+SEL	−SEL	42
43	+C/D	−C/D	44
45	+REQ	−REQ	46
47	+I/O	−I/O	48
49	G	G	50

G: Ground
*1: Differential Driver protection signal
*2: Power supply for terminator (+5 VDC)

Figure 3.3 Host interface connector signal assignments

(1) DB 7 ~ 0, P

Bidirectional data bus consisting eight data bits and odd parity bit.

Data bus is used to transfer command, data, status, or message in Information Transfer phase. SCSI IDs are sent to the data bus in Arbitration phase for determining the priority of bus arbitration. In Selection or Reselection phase, SCSI IDs of the INIT and the TARG are indicated on the data bus.

The use of parity bit is a system option. IDC handles the parity as shown below:

- IDC implements the bus parity check feature, which can be enabled or disabled using the switch on the IDC PCA.
- Parity values are always guaranteed when valid data is transferred to the bus from IDC.

(2) BSY

This signal indicates that the bus is being used. In Arbitration phase, it indicates arbitration request.

(3) SEL

A signal used by an INIT to select a TARG or by a TARG to reselect an INIT.

(4) RST

This signal indicates the Reset condition which is used to clear all SCSI devices.

(5) C/D, I/O, and MSG

These signals are always driven by a TARG to distinguish between the different information transfer phases as shown below:

C/D	I/O	MSG	DB7–0, P	Direction	Phase
0	0	0	Data	INIT → TARG	Data Out
0	1	0	Data	INIT ← TARG	Data In
1	0	0	Command	INIT → TARG	Command
1	1	0	Status	INIT ← TARG	Status
0	0	1	—		
0	1	1	—		
1	0	1	Message	INIT → TARG	MSG Out
1	1	1	Message	INIT ← TARG	MSG In

I/O signal is also used to distinguish between Selection phase and Reselection phase.

(6) REQ

A signal driven by a TARG to indicate a transfer request in Information Transfer phase.

(7) ACK

A signal driven by an INIT to indicate a response to REQ signal in Information Transfer phase.

(8) ATN

A signal driven by an INIT to indicate the Attention condition which informs a TARG that the INIT has a message to be transferred to the TARG.

(9) TERMPWR: Power supply for terminator (+5 VDC)

TERMPWR pins of the interface connector are used to supply the power to the terminator.Figure 3.4 shows the terminator circuit configuration in the IDC.

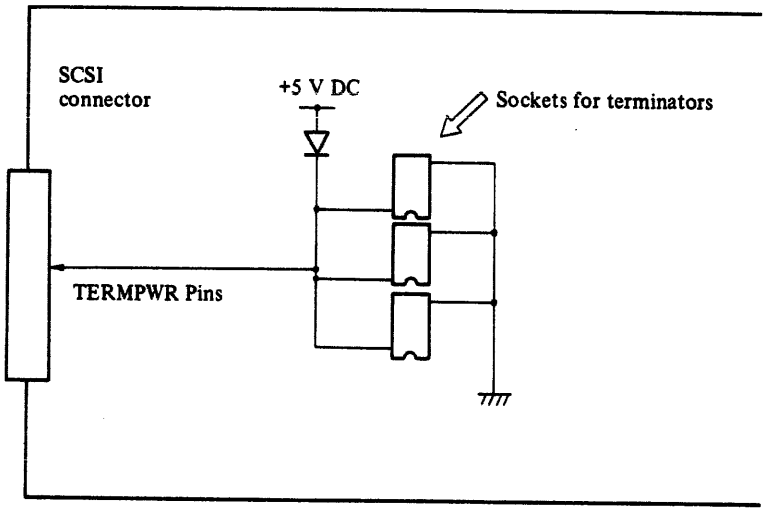


Figure 3.4 SCSI terminator circuit in IDC

(10) DIFFSENS: Differential Driver protection signal

The DIFFSENS signal is an active high enable for the differential drivers. If a single-ended connector is inadvertently attached, this signal is grounded, then disabling the drivers. Figure 3.5 shows the circuit configuration in the IDC for this signal.

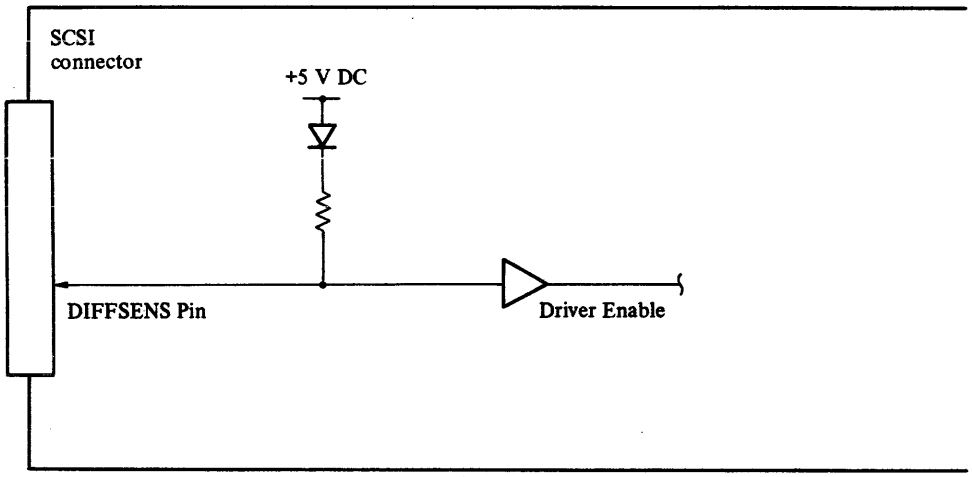


Figure 3.5 Differential Driver protection circuit in IDC

3.4 Bus Phases

3.4.1 Bus Free phase

No SCSI device uses the bus in Bus Free phase. SCSI devices shall detect Bus Free phase after SEL and BSY signals are both false for at least 400 ns (Bus Settle Delay).

SCSI devices which have detected the Bus Free phase shall release all bus signals within the 800 ns (Bus Clear Delay) after BSY and SEL become false for a Bus Settel Delay. The maximum time allowed for releasing the bus after both SEL and BSY become false is 1.2 μs.

3.4.2 Arbitration phase

The Arbitration phase allows one SCSI device to gain control of the SCSI bus so that an INIT starts the Selection phase or a TARG starts the Reselection phase.

Implementation of the Arbitration phase is a system option. This phase is required for system that have two or more INITs or use the Reselection phase. For the IDC, it is necessary to specify whether this phase is used by the setting switch on the IDC PCA.

The procedure for an SCSI device to obtain control of the SCSI bus is follows:

(1) The SCSI device shall wait for Bus Free phase.

(2) The SCSI device shall wait at least 800 ns (Bus Free Delay) after the Bus Free phase detection. Then the SCSI device that arbitrates the bus asserts the data bus bit corresponding to its own SCSI ID and BSY signal within 1.8 μs (Bus Set Delay).

(3) After waiting at least 2.2 μs (Arbitration Delay) since the SCSI device asserted BSY signal, the SCSI device shall examine the value on the data bus to determine the priority of the bus arbitration. The highest-priority is assigned to DB7 (ID=7) and the lowest-priority is assigned to DB0 (ID=0).

When the SCSI device detects any ID bit which is assigned higher priority than its own SCSI ID, the SCSI device shall release its signal then may return to step (1). The SCSI device has lost the arbitration.

The SCSI device which detects no higher SCSI ID bit on the data bus can obtain the bus control, then it shall assert SEL signal. The SCSI device has won the arbitration.

Any other SCSI device that is participating in the Arbitration phase shall release its signals (BSY and its SCSI ID) within 800 ns (Bus Clear Delay) after SEL signal becomes true, then may return to step (1). The SCSI device has lost the arbitration.

(4) The SCSI device which wins arbitration shall wait at least 1.2 μs (Bus Clear Delay + Bus Settle Delay) after asserting SEL signal before changing any signal state.

3.4.3 Selection phase

INIT selects a TARG in the Selection phase. In systems with the Arbitration phase not implemented, the INIT starts the Selection phase in the following sequence:

(1) The INIT shall wait for at least 800 ns (Bus Clear Delay) after Bus Free phase detection. Then the INIT asserts SCSI IDs of desired TARG and INIT itself on the data bus (*1).

(2) After waiting at least 90 ns (Deskew Delay ×2) the INIT asserts SEL signal.

In systems with Arbitration phase impelented, the INIT starts the Selection phase in the following sequence:

(1) The INIT shall wait for at least 1.2 μs (Bus Clear Delay + Bus Settle Delay) after turning SEL signal on. Then the INIT asserts SCSI IDs of the desired TARG and INIT itself on the data bus (*1).

(2) The INIT releases BSY signal after waiting at least 90 ns (Deskew delay × 2).

(3) The INIT shall then wait at least 400 ns (Bus Settle Delay) before looking for the response (BSY signal) from the TARG.

If an SCSI device (TARG to be selected) detects its SCSI ID bit on the data bus when the SEL signal is true and both BSY and I/O signals are false for at least 400 ns (Bus Settle Delay), the selected SCSI device shall assert BSY signal within 200 μs (Selection Abort Time) of its most recent detection of being selected in response to the INIT. The selected TARG may sample all bits on the data bus to identify the INIT's SCSI ID.

At least 90 ns (Deskew Delay × 2) after the BSY signal (asserted by the TARG) detection, the INIT shall release SEL signal.

If the INIT cannot detect the response from TARG when the Selection Timeout Delay (or longer) has passed after starting the Selection phase, the timeout procedure shall be performed through one of the following schemes (*2):

(1) The INIT asserts the RST signal.

(2) The INIT maintains SEL signal true and releases the data bus (SCSI IDs). Subsequently, the INIT waits for the response from TARG for at least 200 μs (Selection Abort Time) + 90 ns (Deskew Delay x 2). If no response is detected, the INIT releases the SEL signal.

*1: If single INIT operates without Reselection phase, it is allowed to assert only the TARG's SCSI ID.

*2: The recommended Selection Timeout Delay is 250 ms.

3.4.4 Reselection phase

A TARG which has disconnected an INIT can reconnect the INIT during the Reselection phase. A TARG performs the Reselection phase in the following sequence after obtaining control of the SCSI bus through the Arbitration phase:

(1) TARG asserts the I/O signal and the SCSI IDs of the TARG itself and INIT to the data bus when at least 1.2 μs (Bus Clear Delay + Bus Settle Delay) have passed after asserting the SEL signal.

(2) The TARG releases the BSY signal after waiting at least 90 ns (Deskew Delay × 2).

(3) The TARG shall then wait at least 400 ns (Bus Settle Delay) before looking for the response (BSY signal) from INIT.

If both the SEL and I/O signals are true and the BSY signal is false for at least 400 ns, the SCSI device (INIT to be reselected) which detected its SCSI ID bit on the data bus shall respond by asserting the BSY signal within 200 μs (Selection Abort Time) of its most recent detection of being reselected. The reselected INIT shall examine all the bits on the data bus to identify the TARG's SCSI ID which requests Reselection.

When the TARG detects a response (BSY signal) from the INIT, the TARG asserts BSY signal and waits at least 90 ns (Deskew Delay × 2), then the TARG releases SEL signal. The INIT shall release the BSY signal after making sure that the SEL signal becomes false.

If the TARG cannot detect a response from INIT after the Selection Timeout Delay (or longer) has passed after starting the Reselection phase, the timeout procedure shall be performed as follows (*1):

- The TARG maintains the SEL and I/O signals true and releases the data bus (SCSI IDs). Subsequently, the TARG waits for the response from INIT for at least 200 μs (Selection Abort Time) + 90 ns (Deskew Delay × 2). If no response is detected, the TARG releases the SEL and I/O signals.

*1: The IDC waits for at least 250 ms before starting the timeout procedure.

3.4.5 Information transfer phases

Data, command, status, or message is transferred via the data bus in the Information Transfer phase. The Information transfer phase type is specified by the combinations of C/D, I/O, and MSG signals.

Information transfer is controlled by one or more REQ and ACK signals.

Each REQ corresponds to one ACK (REQ/ACK handshake). 1-byte information is transferred through one REQ/ACK handshake. Two REQ/ACK handshake modes are available for data, Asynchronous mode and Synchronous mode.

(1) Information Transfer phase type

The TARG must establish the C/D, I/O, and MSG signals for at least 400 ns (Bus Settle Delay) before the leading edge of REQ signal which requests transfer of first byte and must retain the state of these control signals to the trailing edge of ACK signal which corresponds to the last byte.

(2) Asynchronous mode

Information is transferred by the interlocked REQ and ACK signals. Operation in this mode is available for Data, Command, Status, and Message phases.

Figure 3.6 shows timing requirements for interlocked REQ/ACK handshake at the IDC SCSI connector.

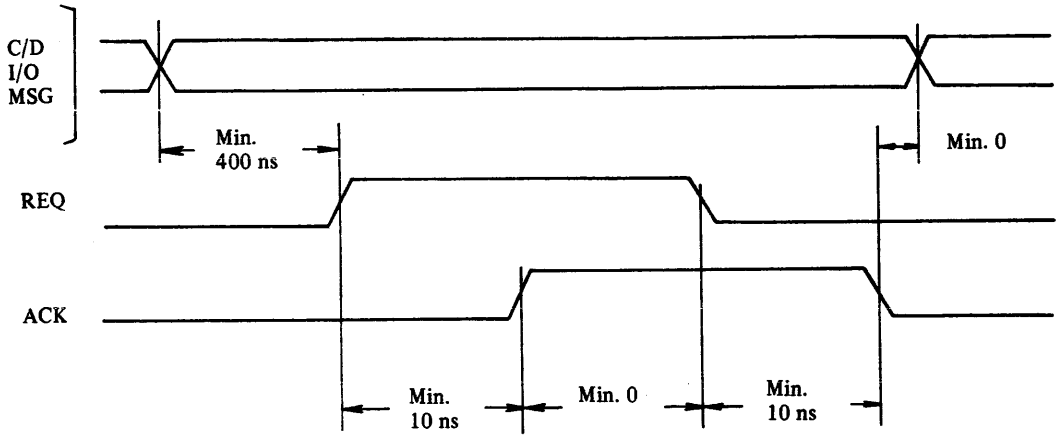


Figure 3.6 Transfer in asynchronous mode (REQ, ACK)

When the I/O signal is true, the TARG must retain the value on the data bus at the TARG's interface connector during the period shown in Figure 3.7.

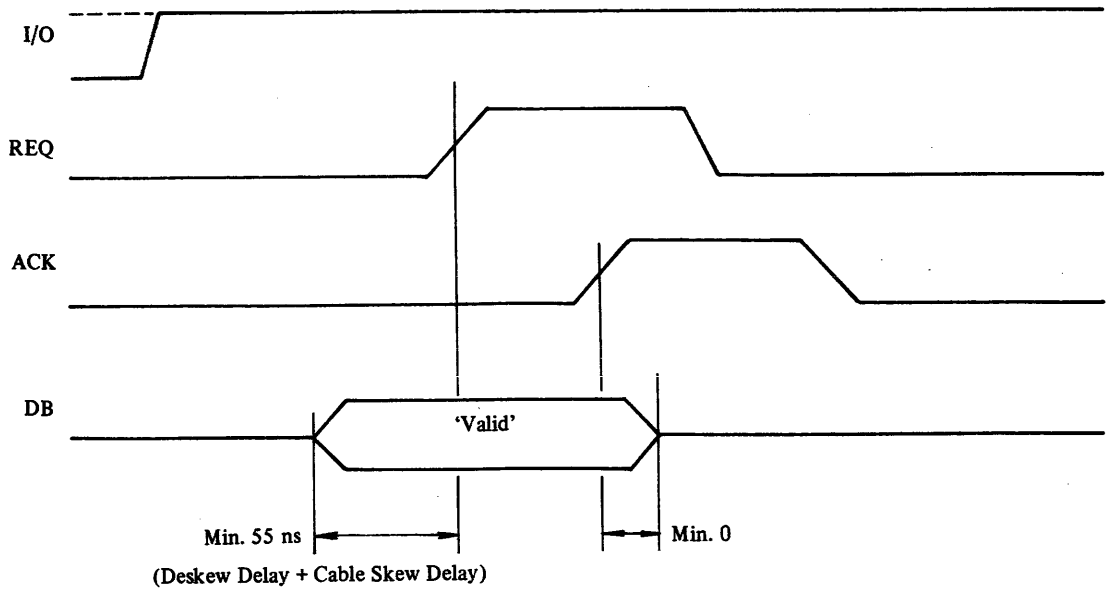


Figure 3.7 Transfer in asynchronous mode (TARG → INIT)

When the I/O signal is false, the INIT must retain the value on data bus at the INIT's interface connector during the period shown in Figure 3.8.

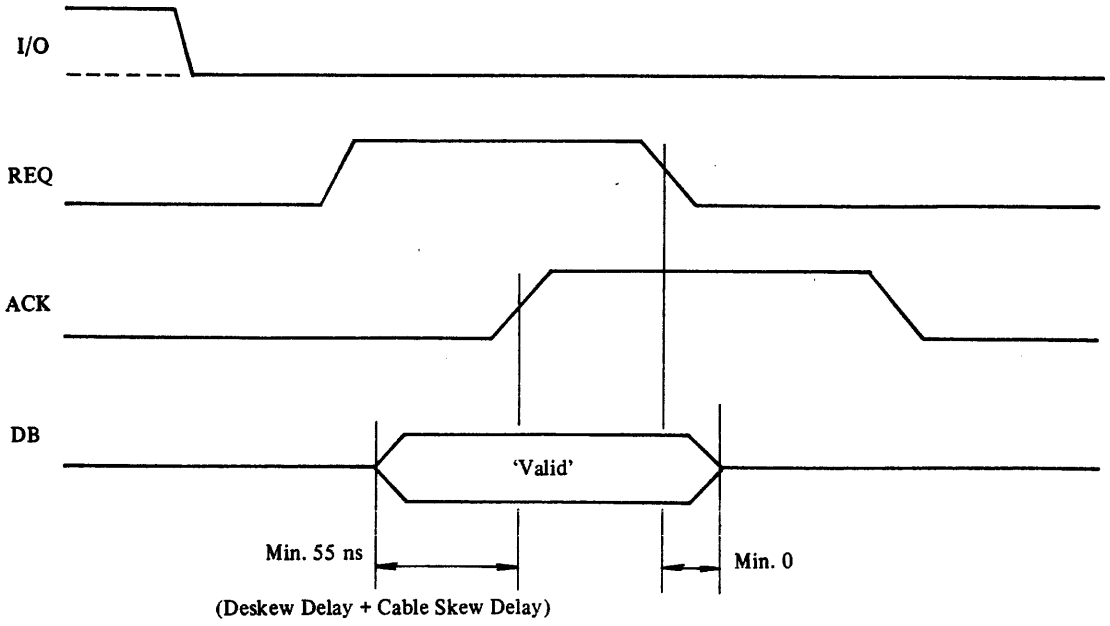


Figure 3.8 Transfer in asynchronous mode (INIT → TARG)

(3) Synchronous mode

Information is transferred through offset interlock of REQ/ACK handshake. Operation in this mode is only available for the Data phase.

Prior to using this mode, synchronous mode parameters shall be agreed by the INIT and the TARG. Parameter definition is established by exchanging a Synchronous Data Transfer Request message between the INIT and the TARG. The following parameters shall be defined:

- REQ/ACK Offset: Maximum number of REQ signals which can be sent by the TARG piror to receiving the ACK signal
- Transfer Period: Minimum interval of REQ and ACK pulses

The TARG can send as many REQ signals as defined by the 'REQ/ACK offset' value prior receiving the ACK signal. The INIT must respond ACK signal as an acknowledgement corresponding to the received REQ signal. To guarantee data transfer validity, the TARG must check that the number of REQ pulses is equal to that of ACK pulses.

Figure 3.9 shows timing requirements for REQ and ACK signals during synchronous mode transfer.

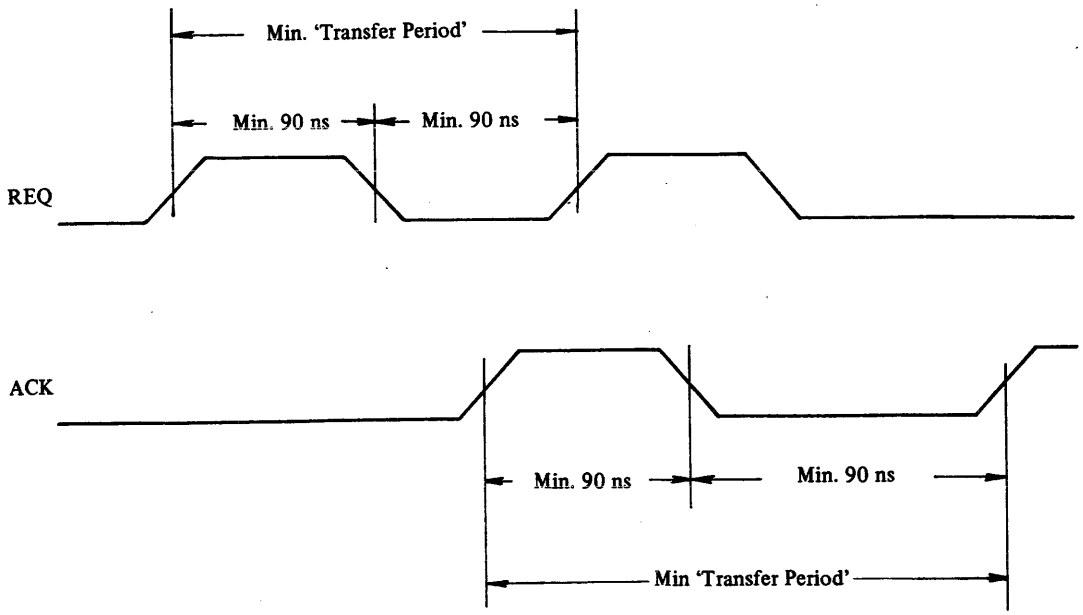


Figure 3.9 Transfer in synchronous mode (REQ, ACK)

If the I/O signal is true, the TARG must retain the value on data bus at the TARG's interface connector during the period shown in Figure 3.10.

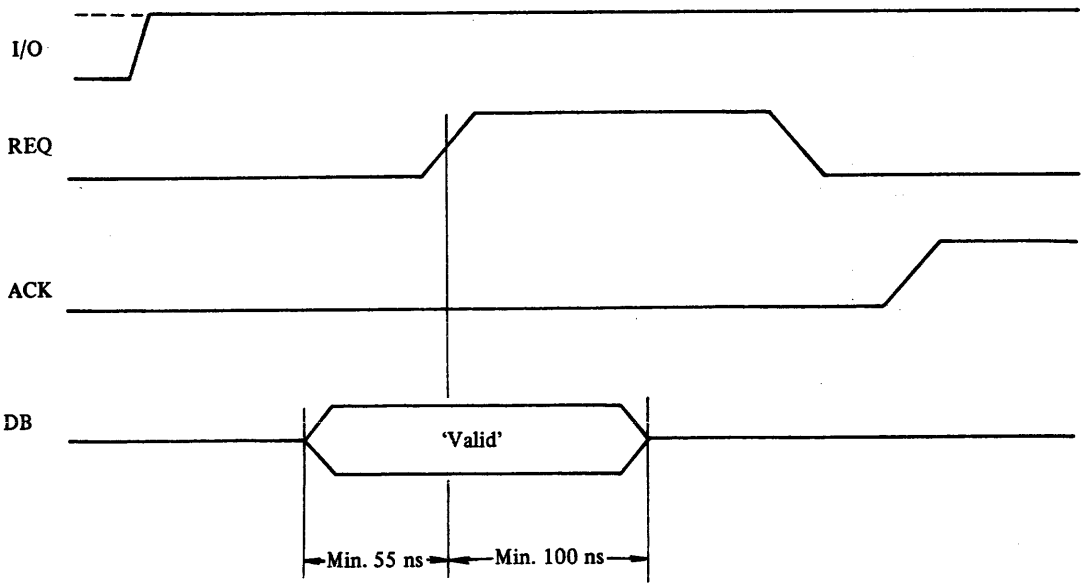


Figure 3.10 Transfer in synchronous mode (TARG → INIT)

If the I/O signal is false, the INIT must retain the value on data bus at the INIT's interface connector during the period shown in Figure 3.11.

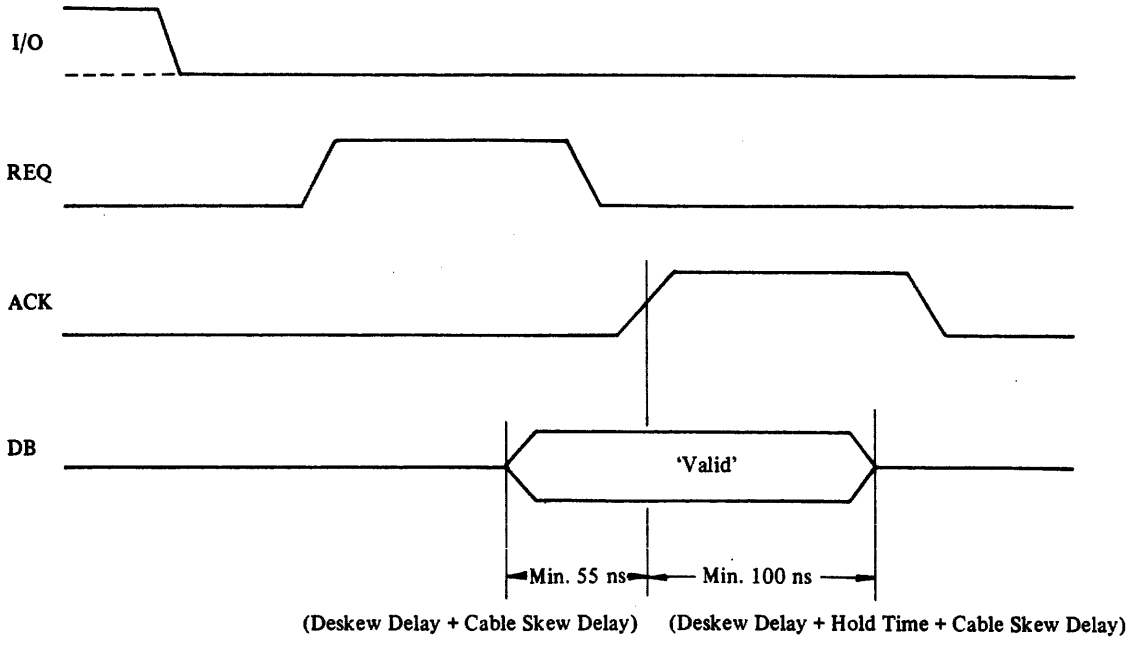


Figure 3.11 Transfer in synchronous mode (INIT → TARG)

Table 3.1 lists parameters used for data transfer in synchronous mode which can be executed by IDC. Synchronous Data Transfer Request messages are exchanged to determine which parameter values are actually used. See Chapter 4 for the detailed description about message exchange.

Table 3.1 Parameters used for synchronous mode data transfer

Parameter	Value
REQ/ACK Offset	1 to 8
Transfer Period (Minimum REQ/ACK interval to be received by IDC)	Min 248 ns
Transfer Period (Minimum REQ/ACK interval to be sent from IDC)	250 ns, 375 ns, 500 ns, or 625 ns

(4) Time supervision

When IDC is operating as a TARG, the IDC performes time supervision for approximately 30 sec to wait for an ACK signal in response to a REQ signal.

If the timeout is detected, the IDC causes the SCSI bus to go to Bus Free phase forcedly. The command which is being executed is aborted.

3.5 Bus Condititions

3.5.1 Attention condition

The Attention condition allows an INIT to inform the TARG that the INIT has a message to be sent to the TARG. By asserting the ATN signal, the INIT can create the Attention condition all the time except during the Arbitration or Bus Free phase.

The TARG may start the Message Out phase at its convention in response to the Attention condition to receive messages from the INIT.

The INIT must keep the ATN signal asserted while all message bytes are transferred. The INIT negates the ATN signal after receiving the REQ signal which corresponds to the last byte of message to be sent and before asserting the ACK signal.

If a parity error is detected in the received message, the TARG may retry the Message Out phase in the following sequence:

(1) The TARG asserts the REQ signal without changing the bus phase after detecting the ATN signal has gone false.

(2) The INIT shall resend all of the previous message bytes which have been transferred during this Message Out phase. The ATN signal shall be asserted prior to asserting the first ACK signal if two or more message bytes are to be resended.

If all message bytes are normally received by the TARG, the TARG changes the bus phase to any Information Transfer phase other than the Message Out phase and transfers at least one byte except that the TARG goes to Bus Free phase after receiving the message.

3.5.2 Reset condition

All SCSI devices are reset immediately and the SCSI bus goes to the Bus Free phase through the Reset condition. Any SCSI device may create the Reset condition at any time by asserting the RST signal. However, IDC does not create this condition.

The RST signal must be asserted for at least 25 μs (Reset Hold Time).

All SCSI devices must release all bus signals other than RST signal within 800 ns (Bus Clear Delay) after the RST signal becomes true.

The following operations which are being executed or preserved are affected by the Reset condition in the IDC ('Hard' Reset):

(1) All uncompleted commands are cleared.

(2) The reserve status for all drives is released.

(3) The sense data pending state is cleared and all preserved sense data are lost.

(4) Synchronous data transfer parameters which have been established between IDC and SCSI device(s) are reset so that data transfer mode for all SCSI device is initialized in asynchronous mode.

(5) Pending unit attention conditions are cleared and Not Ready to Ready unit attention conditions are created for all devices (LUN) which are in Ready state.

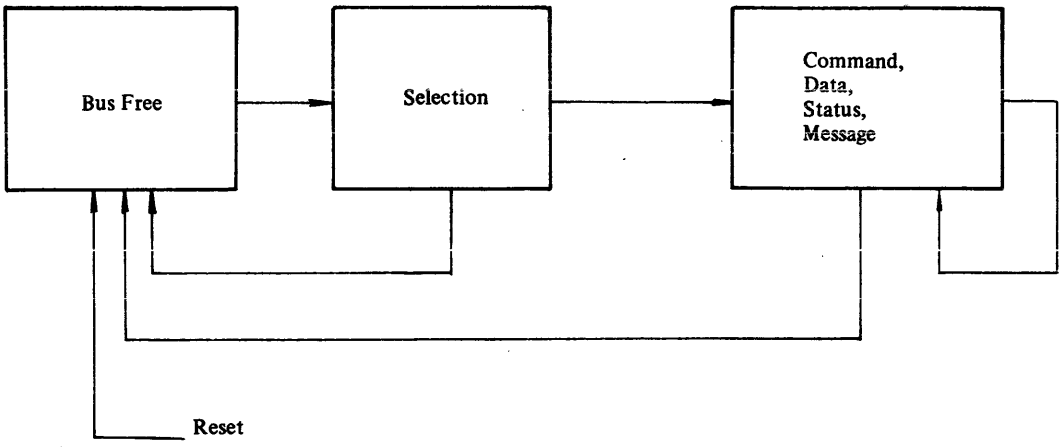
(6) Mode Select parameters which have been established are cleared, then the IDC sets the default values for all parameters.

3.6 Bus Phase Sequences

Figure 3.12 shows the allowable bus phase sequence applied to systems without the Arbitration phase and systems with the Arbitration phase. Figure 3.13 provides an example of bus phase sequence during single command execution.

After a TARG has asserted a BSY signal in the Selection or Reselection phase, the bus phase sequence other than Reset condition is controlled by the TARG.

When Arbitration is not used



When Arbitration is used

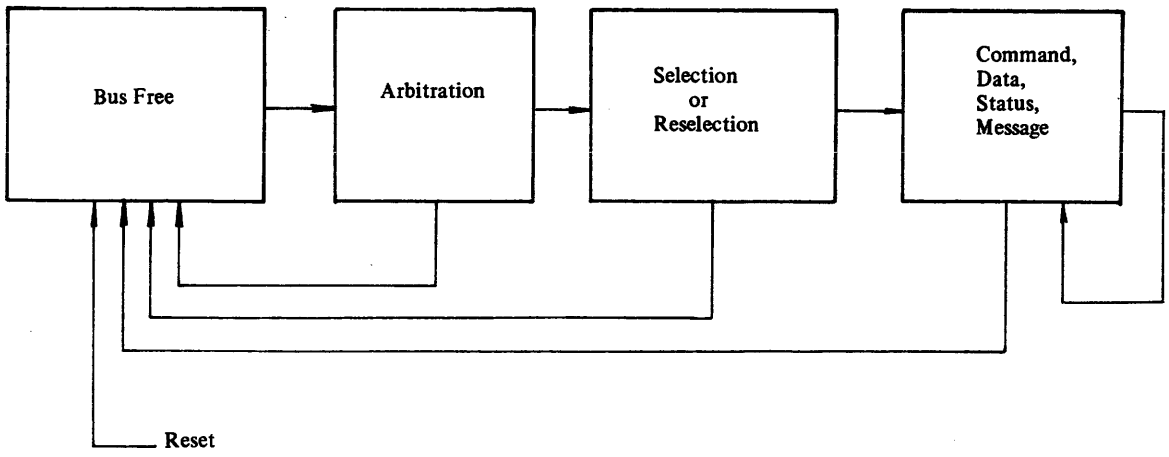


Figure 3.12 Bus phase sequences

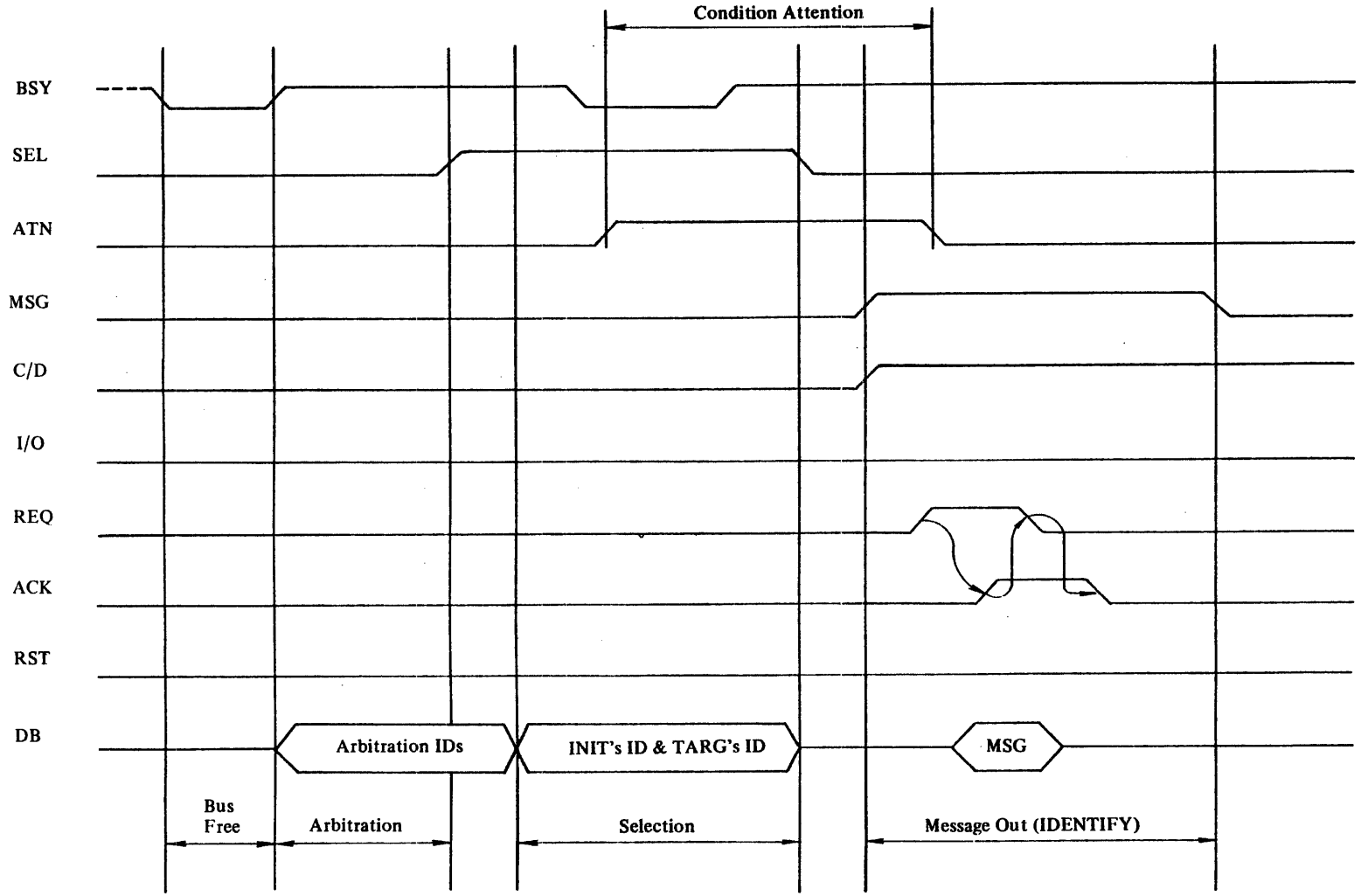


Figure 3.13 Bus phase sequence example (1/5)

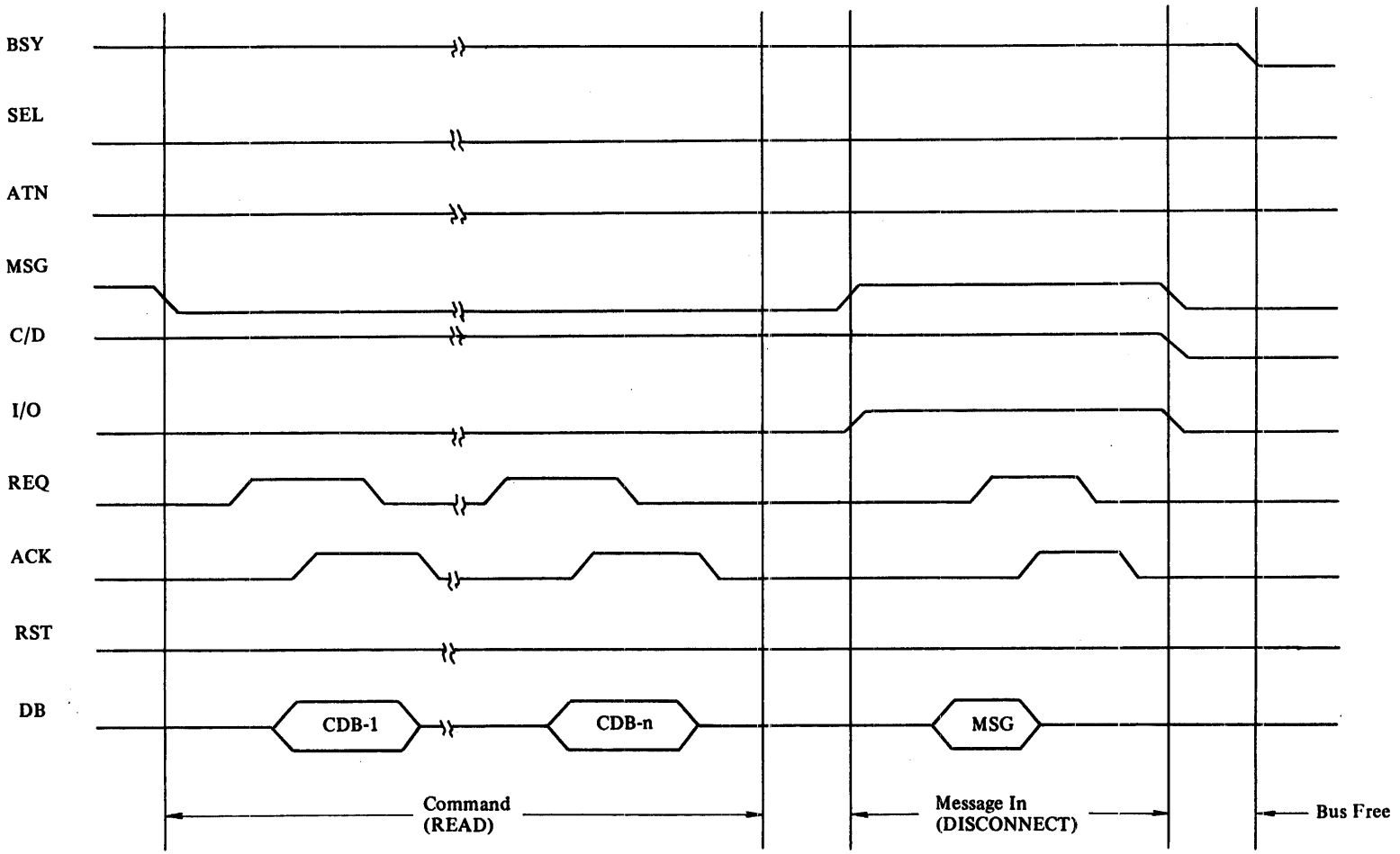


Figure 3.13 Bus phase sequence example (2/5)

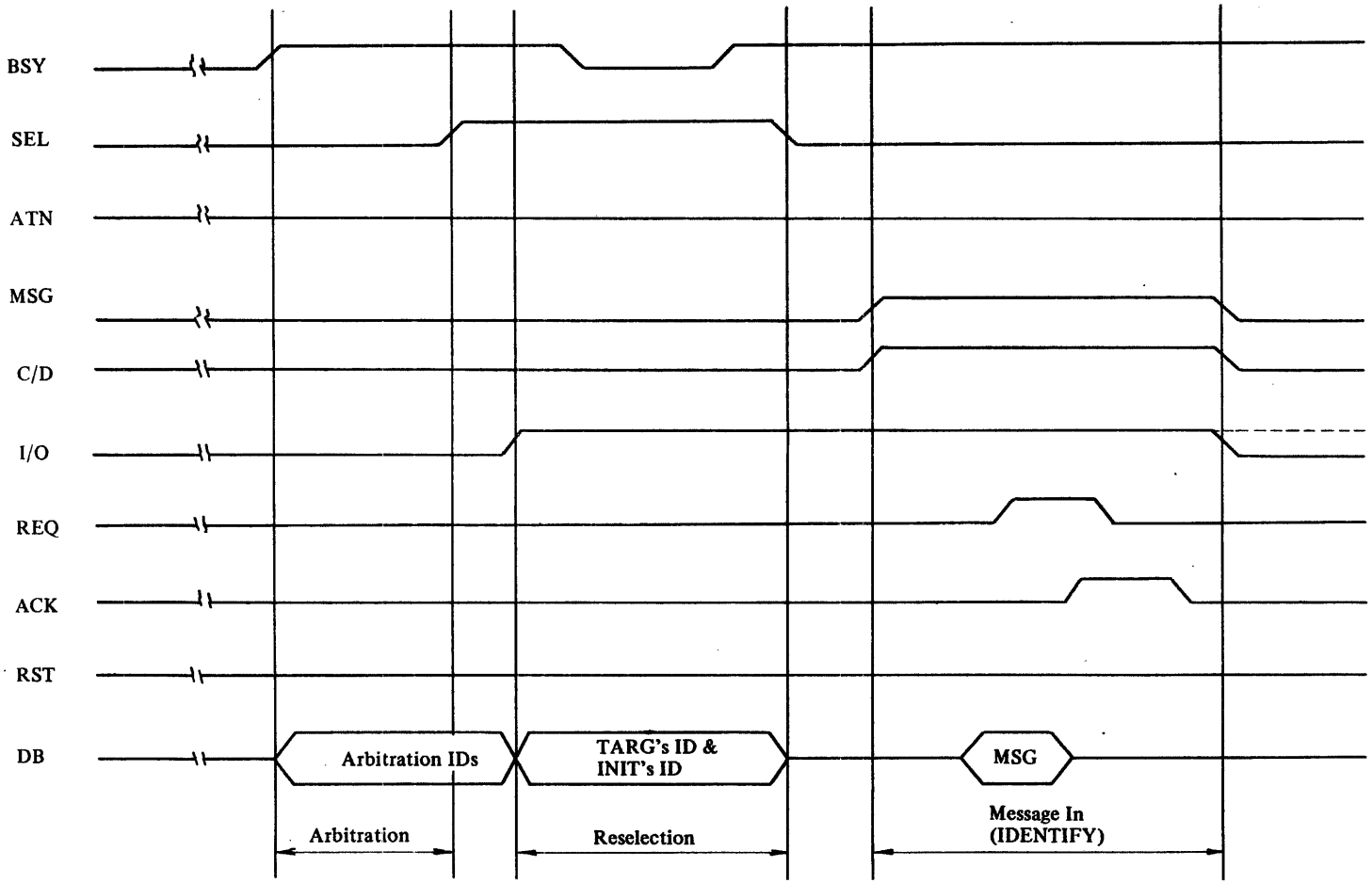


Figure 3.13 Bus phase sequence example (3/5)

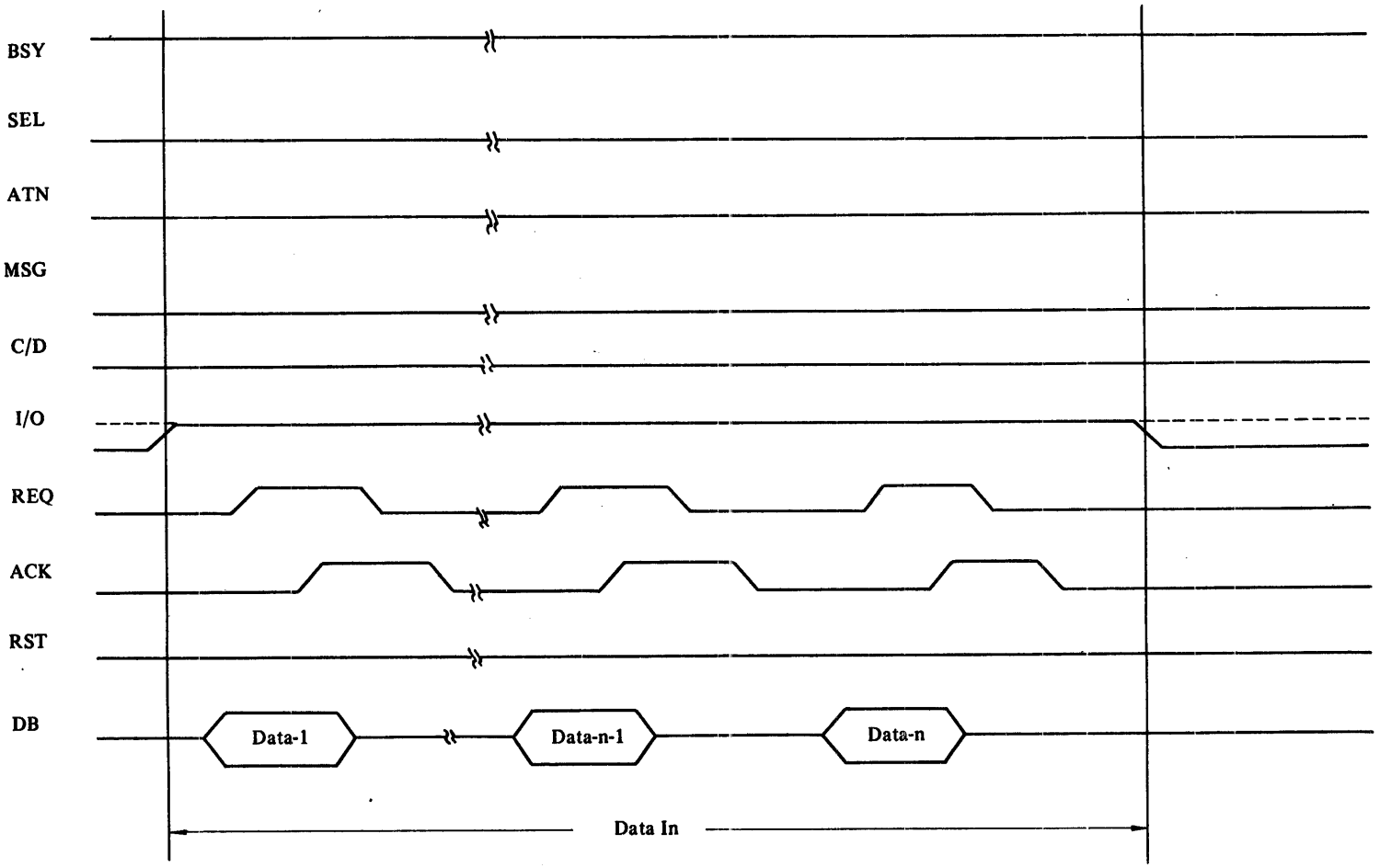


Figure 3.13 Bus phase sequence example (4/5)

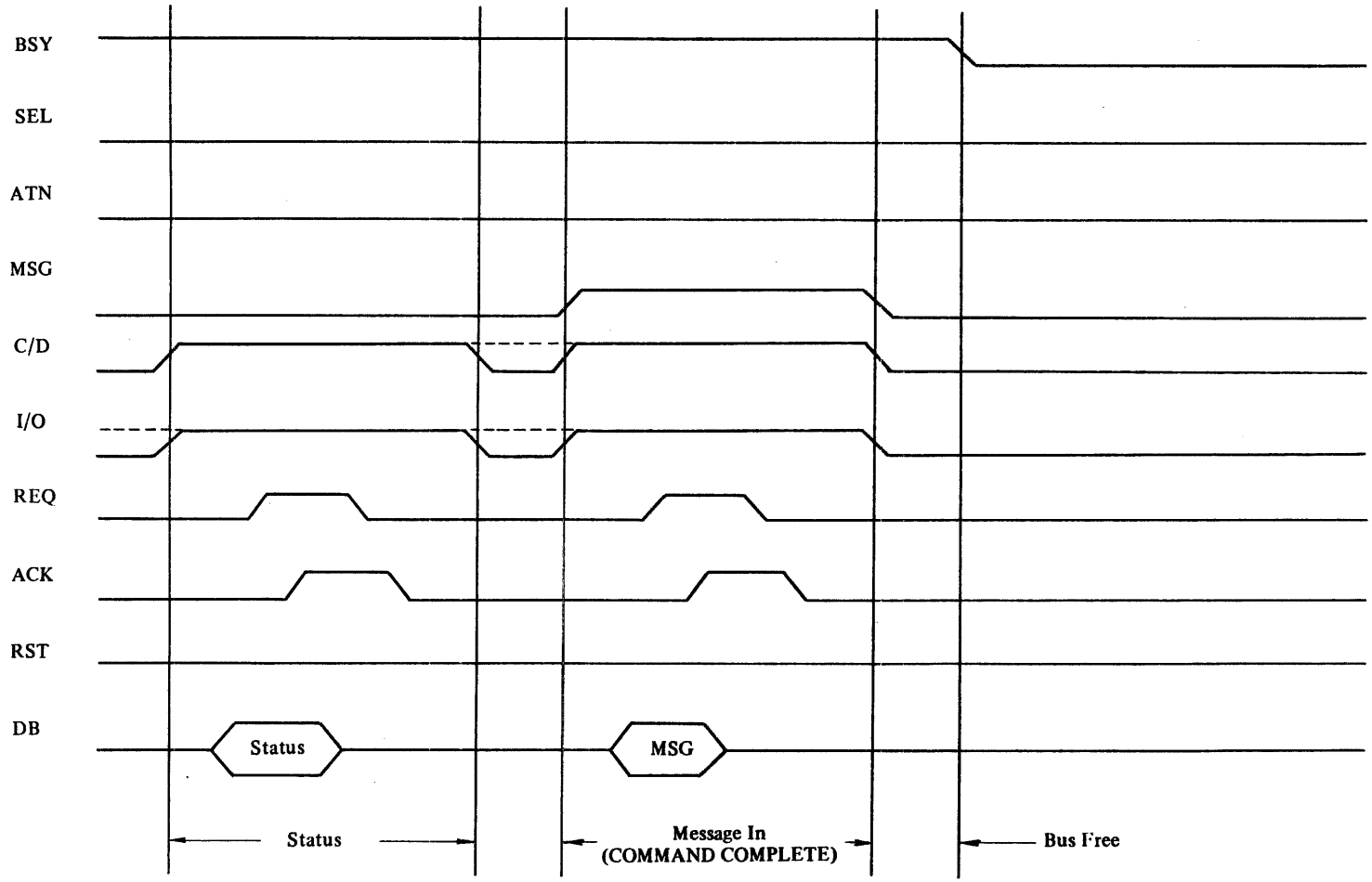


Figure 3.13 Bus phase sequence example (5/5)

3.7 Electrical Requirements

3.7.1 Electrical characteristics

Table 3.2 lists signal sources for each interface phase. And, Table 3.3 shows the signal value and electrical levels.

Table 3.2 Bus phase and signal sources

Signal / Bus Phase	BSY	SEL	C/D, I/O MSG, REQ	ACK, ATN	DB7~0, P	RST
Bus Free	N	N	N	N	N	N
Arbitration	A	W	N	N	ID	A
Selection	I & T	I	N	I	I	A
Reselection	I & T	T	T	I	T	A
Command	T	N	T	I	I	A
Data In	T	N	T	I	I	A
Data Out	T	N	T	I	T	A
Status	T	N	T	I	T	A
Message In	T	N	T	I	T	A
Message Out	T	N	T	I	I	A

N: Not be driven by any SCSI device. The terminator pulls the signal to the false state.

A: Any SCSI device can drive the signal. Two or more SCSI devices may drive the signal at the same time.

W: Only the SCSI device which wins arbitration can drive the signal.

ID: Each SCSI device which is arbitrating the bus drives a unique data bit (SCSI ID).

I: Only the SCSI device which operates as INIT can drive the signal.

T: Only the SCSI device which operates as TARG can drive the signal.

I & T: INIT, TARG or both can drive this signal according to the interface sequence.

Table 3.3 Signal values and electrical levels

Signal value	Electrical level
TRUE, asserted, on, or '1'	+SIGNAL is more positive than −SIGNAL
FALSE, negated, released, off, or '0'	−SIGNAL is more positive than +SIGNAL

3.7.2 Driver and receiver circuits

For all signals, the DS3695N (National Semiconductor) or equivalent is recommended.

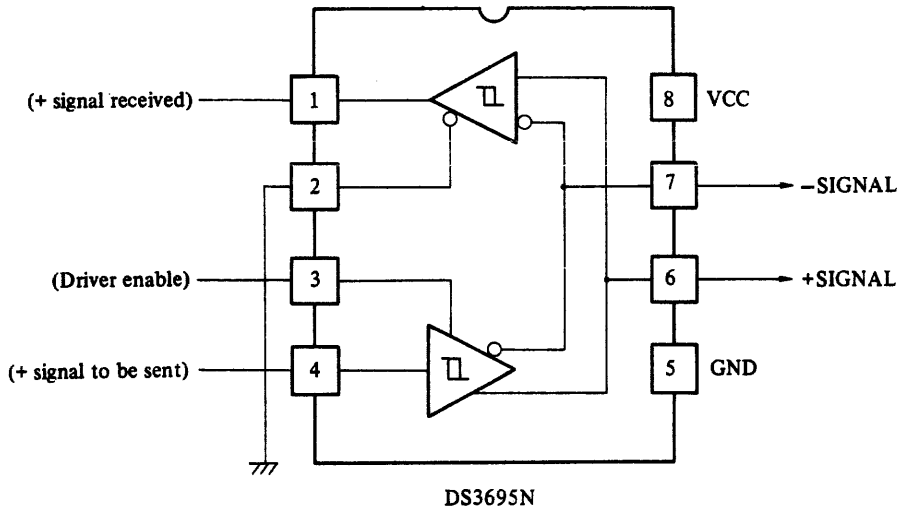


Figure 3.14 Differential driver/receiver circuit (recommended)

3.7.3 Termination circuit

The termination circuits shown in Figure 3.15 are installed in SCSI devices which are connected at either ends of the interface cable.

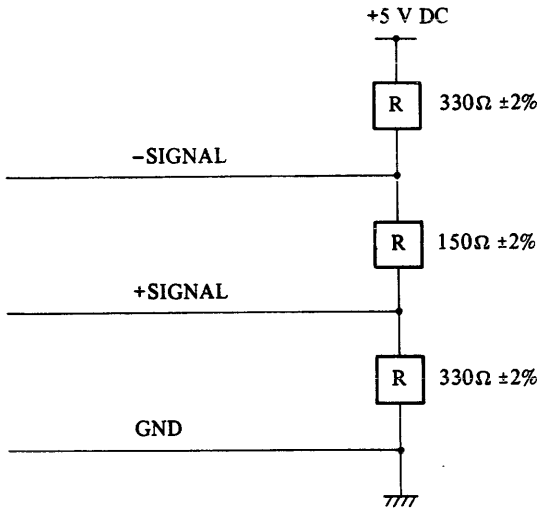


Figure 3.15 Differential SCSI termination circuit

3.8 Physical Requirements

3.8.1 Connector requirements

The nonshielded SCSI connector installed on the IDC is a 50-conductor connector consisting of two rows of 25 male pins with adjacent pins 2.54 mm (0.1 in) apart.

The nonshielded cable connector shall be a 50-conductor connector consisting of two rows of 25 female contacts with adjacent contacts 2.54 mm (0.1 in) apart. The use of keyed connectors is recommended to prevent accidental grounding or misconnection of terminator power because the IDC provides terminator power to its SCSI connector.

3.8.2 Cable requirements

A characteristic impedance of 100 ohms ± 10% is recommended for unshielded twisted-pair ribbon cable. A characteristic impedance greater than 90 ohms is preferred for shielded cable. A minimum conductor size of 28 AWG shall be employed.

It is recommended that shielded cable be used for connection outside of a cabinet.

To minimize discontinuities and signal reflections, cables of different impedance should not be used in the same bus. The maximum cable length is 25 m. 1 m or more cable length is required between SCSI devices.

CHAPTER 4 MESSAGES

4.1 Message System

The message system allows communication between SCSI devices. Messages are transferred via the SCSI data bus in the Message Out phase and Message In phase.

4.1.1 Message type

Byte 1 of each message contains the message code. Message code X'01' indicates the beginning of a multiple-byte extended message. Messages with other message codes are single-byte messages. Figure 4.1 shows the extended message format. Tables 4.1 and 4.2 list the messages which are implemented in IDC.

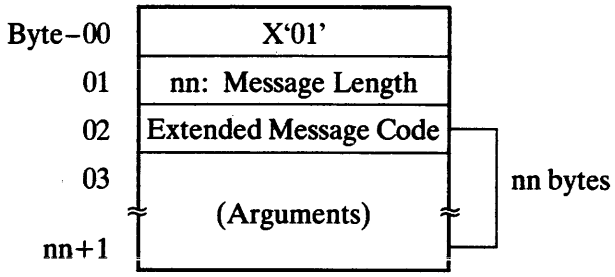


Figure 4.1 Extended message format

Table 4.1 Single byte messages

Code	Message	Transfer direction
00	Command Complete	TARG → INIT
02	Save Data Pointer	TARG → INIT
03	Restore Pointers	TARG → INIT
04	Disconnect	TARG → INIT
05	Initiator Detected Error	TARG ← INIT
06	Abort	TARG ← INIT
07	Message Reject	TARG ↔ INIT
08	No Operation	TARG ← INIT
09	Message Parity Error	TARG ← INIT
0A	Linked Command Complete	TARG → INIT
0B	Linked Command Complete with Flag	TARG → INIT
0C	Bus Device Reset	TARG ← INIT
80 | FF	Identify	TARG ↔ INIT

Table 4.2 Extended messages

Extended message code	Message	Length in bytes	Transfer direction
01	Synchronous Data Transfer Request	5	TARG ↔ INIT

4.1.2 Pointers

The following pointers are required to manage command execution on the SCSI:

- Command Pointer
- Data pointer
- Status pointer

The pointers reside in the SCSI device which operates as an INIT. There are two sets of pointers, active and saved.

The active pointers are used to control a command which is currently being executed on the SCSI. Each time a byte of command, data, or status is transferred in the Information Transfer phase, the corresponding active pointer is incremented.

The saved pointers are required to provide the following capability:

- Concurrent operation on two or more TARGs or multiple peripheral devices under SCSI control
- Retry on SCSI for command execution error recovery

If the INIT allows disconnection, the INIT must provide two or more sets of saved pointers. The INIT must set the active and saved pointers to the same value at the begining of each command.

The TARG can control saving and restoring pointers using the message system.

4.2 Message Explanation

Symbols:

(I → T): Message is sent from an INIT to a TARG.

(T → I): Message is sent from a TARG to an INIT.

(I ↔ T): Message is sent from an INIT to a TARG or from a TARG to an INIT.

(1) Command Complete message : X'00' (T → I)

This message indicates that the execution of single command or a series of linked commands has terminated and valid status has been sent to the INIT.

The TARG shall go to the Bus Free phase after this message is sent successfully.

(2) Save Data Pointer message : X'02' (T → I)

This message directs the INIT to save the active data pointer. In response to this message, the INIT stores the value of the active data pointer into the saved data pointer for the currently attached LUN.

(3) Restore Pointers message : X'03' (T → I)

This message directs the INIT to restore the most recently saved pointers to the active pointers (command pointer, data pointer, and status pointer). The INIT retrieves the saved pointers for the currently attached LUN and makes them active.

(4) Disconnect message : X'04' (T → I)

This message informs the INIT that the current operation is temporarily disconnected from the SCSI. After sending this message successfully, the TARG goes to the Bus Free phase. The TARG continues command processing within the TARG and reselects the INIT to complete command execution when the reconnection is needed.

The INIT does not save the active pointers through this message.

(5) Initiator Detected Error message: X'05' (I → T)

This message informs the TARG that the INIT has detected an error that does not preclude the TARG from retrying the operation. The validity of active pointer values is not assured. If the TARG retries the operation after receiving this message, the TARG should restore the pointers by sending Restore Pointers message or by disconnection followed by reconnection.

(6) Abort message : X'06' (I → T)

This message directs the TARG to perform the following:

- If an LUN has been identified, the TARG clears the I/O operation issued by the INIT and pending status for the INIT associated with the specified device (LUN). Then, the TARG enters the Bus Free phase.

Only one I/O operation associated with the INIT is cleared. This message does not affect I/O operations and pending statuses for other INITs. If an LUN has not been identified prior to this message, the TARG enters the Bus Free phase without any other operation.

(7) Message Reject message : X'07' (I ↔ T)

This message indicates that the message which is received immediately before is inappropriate or has not been implemented.

To identify the rejected message, the Message Reject message shall be transferred in the following sequence:

- If INIT sends this message, assert the ATN signal before negating the ACK signal for the last byte of received message.
- If TARG sends this message, change to the Message In phase immediately after the ACK signal is negated during the Message Out phase.

(8) No Operation message : X'08' (I → T)

This message does not result in any operation. The INIT sends this message in response to the message request from the TARG when the INIT does not currently have any other valid message to send.

(9) Message Parity Error message : X'09' (I → T)

This message indicates that the message received by the INIT contains the byte where a parity error was detected. To identify the message where an error was detected, the INIT shall assert the ATN signal before negating the last ACK signal which corresponds to the message containing the parity error.

(10) Linked Command Complete message : X'0A' (T → I)

This message indicates that the execution of a command which specifies a link bit one (flag bit = '0') has been completed and that valid status information has been sent to the INIT. After receiving this message, the INIT updates the pointers to the initial value for the next linked command.

(11) Linked Command Complete with Flag message : X'0B' (T → I)

This message indicates that the execution of a command which specifies a link bit one (flag bit = '1') has been completed and that valid status information has been sent to the INIT. After receiving this message, the INIT updates the pointers to the initial value for the next linked command.

(12) Bus Device Reset message : X'0C' (I → T)

This message directs the TARG to clear all I/O operations and all pending statuses. The TARG which receives this message clears not only I/O operations issued by the connected INIT, but also I/O operations issued by all INITs associating with any device (LUN) under the TARG, then the TARG goes to the Bus Free phase.

Data transfer mode among all SCSI devices is initialized to use the asynchronous mode. All pending unit attention conditions are cleared and Not Ready to Ready unit attention conditions are created for all devices (LUN) which are in Ready state.

(13) Identify message : X'80' to X'FF' (I ↔ T)

This message specifies the logical unit number (LUN) under the TARG to establish the path connection.

- Bit 6: D

  This bit can only be specified by the INIT. When this bit is set to one, it indicates that the INIT has the ability to accommodate Disconnection/Reconnection function.

- Bits 2 to 0: LUN

  The logical unit number is specified in these bits. In IDC, LUN is identifical to the physical unit address of the drive and ranges from 0 to 3.

Normally, the Identify message is sent from the INIT as the first message after the Selection phase to identify the LUN of the unit to be accessed.

Also, the TARG sends this message after the Reselection phase to notify the INIT of the LUN to be reconnected. After this message is received by the INIT, the data, command, and status pointers for the specified LUN are restored to active state.

(14) Synchronous Data Transfer Request message (I ↔ T)

	7	6	5	4	3	2	1	0
BYTE-00	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	1	1
02	0	0	0	0	0	0	0	1
03	mm: Transfer Period (4 × mm (ns))							
04	xx: REQ/ACK Offset							

The following parameters used for data transfer in synchronous mode are defined between the SCSI devices by exchanging this message:

- Transfer Period: Minimum time between leading edges of successive REQ pulses and of successive ACK pulses

- REQ/ACK Offset: Maximum offset value between the REQ and ACK pulses

  TARG can send up to xx REQ pulses before its corrsponding ACK pulse is received, where: xx = X'00' → Asynchronous transfer mode
  xx = X'FF' → Offset value is unlimited.

To transfer data in synchronous mode, the SCSI devices shall define parameters used for the synchronous mode transfer after power on, 'Hard' Reset condition, or Bus Device Reset message. The message exchange described below is performed to establish the transfer mode. Transfer Period and REQ/ACK Offset values are determined by exchanging messages and data transfer in synchronous mode is enabled.

If the INIT recognizes that a Synchronous Data Transfer Request mesage must be sent, it creates an Attention condition and requests the TARG to receive the message. The INIT specifies the REQ/ACK Offset value which does not cause its buffer overflow and the Transfer Period value which is required for data handling within the INIT.

If the message is received by the TARG, the TARG interprets the values requested by the INIT and returns a Synchronous Data Transfer Request message or a Message Reject message. The Synchronous Data Transfer Request message can be returned with REQ/ACK Offset and Transfer Period values which can be handled by the TARG itself and are not exceed the value requested by the INIT.

Table 4.3 indicates how IDC responds to the message from an INIT and which transfer mode is to be determined when IDC operates as a TARG.

If the TARG recognizes that the negotiation for synchronous transfer, it sends a Synchronous Data Transfer Request message to the INIT. The TARG can specify the REQ/ACK Offset value which does not cause its buffer overflow and the Transfer Period value which meets the data handling requirements of the TARG.

The INIT shall interpret the values requested by the TARG and shall return a Synchronous Data Transfer Request message or a Message Reject message. The Synchronous Data Transfer Request message can be returned with REQ/ACK Offset and Transfer Period values which can be handled by the INIT itself and are not exceed the value requested by the TARG.

Table 4.4 summarizes the message exchange ways initiated by the IDC and transfer mode to be determined when the IDC operates as a TARG. If the INIT does not respond the message listed in Table 4.4, the IDC assumes that the synchronous mode transfer has not been established and transfers data in asynchronous mode.

Data transfer mode established by above-mentioned message exchange must remain in effect on both SCSI devices until one of the followings occurs:

- Transfer mode between identical SCSI devices is modified.
- A Bus Device Reset message is received.
- 'Hard' Reset condition

The default data transfer mode is asynchronous. After power on, a Bus Device Reset message or a 'Hard' Reset condition, the transfer mode remains in asynchroous mode unless message exchange resulting from Synchronous Data Transfer Request message is performed.

If the IDC preserved the default a synchronous transfer mode for any INIT, the IDC tries to establish the synchronous transfer mode by using the message exchange way shown in Table 4.4 when the IDC is selected first from each INIT.

Table 4.3 Message exchange for synchronous transfer initiated by INIT (IDC = TARG)

Value requested by INIT	Response from IDC (TARG)	Transfer mode to be defined
REQ/ACK Offset ≧ 9	REQ/ACK Offset = 8	Synchronous mode (Offset = 8)
1 ≦ REQ/ACK Offset ≦ 8	REQ/ACK Offset = (Value requested by INIT)	Synchronous mode (Offset = value requested by INIT)
REQ/ACK Offset = 0	REQ/ACK Offset = 0	Asynchronous mode
Transfer Period ≦ X'3E' (248 ns)	Transfer Period = X'3E' (248 ns)	Synchronous mode with 4 MB/s max. (REQ cycle ≧ 250 ns, ACK cycle ≧ 248 ns)
X'3F' ≦ Transfer Period ≦ X'5D' (252 ns) (372 ns)	Transfer Period = (Value requested by INIT)	Synchronous mode with 2.67 MB/s max. (REQ cycle ≧ 375 ns, ACK cycle ≧ 252 ns)
X'5E' ≦ Transfer Period ≦ X'7D' (376 ns) (500 ns)	Transfer Period = (Value requested by INIT)	Synchronous mode with 2 MB/s max. (REQ cycle ≧ 500 ns, ACK cycle ≧ 376 ns)
X'7E' ≦ Transfer Period ≦ X'9C' (504 ns) (624 ns)	Transfer Period = (Value requested by INIT)	Synchronous mode with 1.6 MB/s max. (REQ cycle ≧ 625 ns, ACK cycle ≧ 504 ns)
Transfer Period ≧ X'9D' (628 ns)	REQ/ACK Offset = 0	Asynchronous mode

Table 4.4 Message exchange for synchronous transfer initiated by IDC (IDC = TARG)

Value requested by IDC (TARG)	Response from INIT	Transfer mode to be defined
REQ/ACK Offset = 8 Transfer Period = X'3E' (248 ns)	Message Reject message (*)	Asynchronous mode
	REQ/ACK Offset = 0 (*)	Asynchronous mode
	1 ≦ REQ/ACK Offset ≦ 8	Synchronous mode (Offset = INIT response value)
	Transfer Period = X'3E' (248 ns)	Synchronous mode with 4 MB/s max. (REQ cycle ≧ 250 ns, ACK cycle ≧ 248 ns)
	X'3F' ≦ Transfer Period ≦ X'5D' (252 ns) (372 ns)	Synchronous mode with 2.67 MB/s max. (REQ cycle ≧ 375 ns, ACK cycle ≧ 252 ns)
	X'5E' ≦ Transfer Period ≦ X'7D' (376 ns) (500 ns)	Synchronous mode with 2 MB/s max. (REQ cycle ≧ 500 ns, ACK cycle ≧ 376 ns)
	X'7E' ≦ Transfer Period ≦ X'9C' (504 ns) (624 ns)	Synchronous mode with 1.6 MB/s max. (REQ cycle ≧ 625 ns, ACK cycle ≧ 504 ns)

(*): The REQ signal cycle sent by IDC is 250 ns, 375 ns, 500 ns or 625 ns.
Send Message Reject message or Synchronous Data Transfer Request message with REQ/ACK Offset = 0 as response if INIT requires X'9D' (628 ns) or more for the Transfer Period.

CHAPTER 5 DATA FORMAT AND ADDRESSING

5.1 Data Format

The basic data units processed between IDC and the drive are fixed-length data blocks. The following describes the physical configuration of the data block.

5.1.1 Track format

Each track in the drive is divided into fixed-length sectors, and each sector consists of an ID field, a fixed-length data field, and gaps. Figure 5.1 shows the track and a sector formats. In this drawing, the lengths of gaps G1, G2, G3, and data field depend on device types and data formats. See Table 5.1 for details on the formats for the respective drives.

Note: Unless otherwise notified in this manual, the terms Sector and Block have the following meaning:

Sector: Refers to the physical layout of a data block in the drive. A sector number (address) is a serial number starting from zero with an index as a starting point for each track.

Block: Refers to the logical layout of a data block in the drive. A block number is a serial number starting from zero according to the logical layout for each track. If sectors are not interleaved, the block number is equal to the sector number.

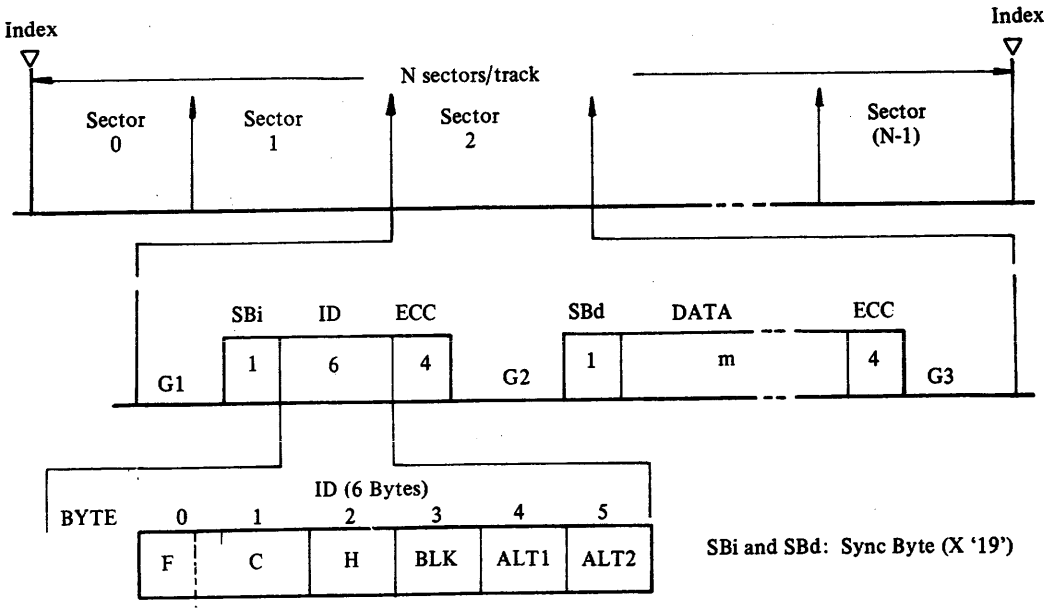


Figure 5.1 Track format

Table 5.1 Track format

		M2333KS/M2331KS		
		S1 (256 bytes)	S2 (512 bytes)	S3 (1,024 bytes)
Bytes/track		40,960		
Sectors/track		121	69	37
Bytes/sector		338	590	1,102
Secter formats (Bytes)	G1	21	21	21
	SBi	1	1	1
	ID	6	6	6
	ECCi	4	4	4
	G2	22	22	22
	SBd	1	1	1
	DATA	256	512	1,024
	ECCd	4	4	4
	G3	23	19	19

5.1.2 Sector format

Figure 5.1 and Table 5.1 show the normal sector format. In addition to the normal sector format, two ID displaced formats are provided as shown in Figure 5.2 to avoid defective field on which the ID field is to be located. The ID displaced formats have an ID field only on that sector. These displaced ID formats improve the availability of the alternate block processing.

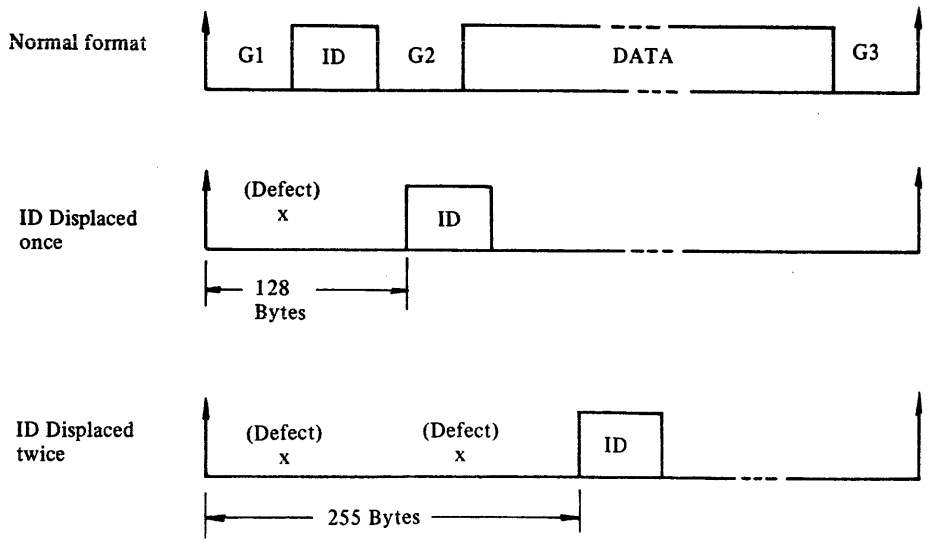


Figure 5.2 Sector formats

5.1.3 ID field format

An ID field is 6 bytes long and consists of a block address, control flag bits, and pointer for defective/alternate block processing. The meaning of each byte of an ID field depends on combinations of flag bits.

Figure 5.3 shows the ID field structure and Figure 5.4 shows combinations of flag bits and contents of the ID field.

	Byte	Bit	Definition	
ID		7	DEF: This block is a defective block	FLAG
		6	ALT: This block is an alternate block	
		5	ASG: This block is an assigned alternate block	
		4	SCY: An alternate block has been assigned on the same cylinder	
		3	ONE: The ID field has been displaced once	
		2	TWO: The ID field has been displaced twice	
		1	Cylinder address	CYL
		0		
	1	7		
		|		
		0		
	2	7	Head address	HD
		|		
		0		
	3	7	Block number on the track	BLK
		|		
		0		
	4	7	Alternate sector offset (*)	ALT
		|		
		0		
		1	Alternate cylinder address	
		0		
	5	7		
		|		
		0		

*: The sector offset indicates a location of the alternate block in an alternate block area provided for each cylinder:

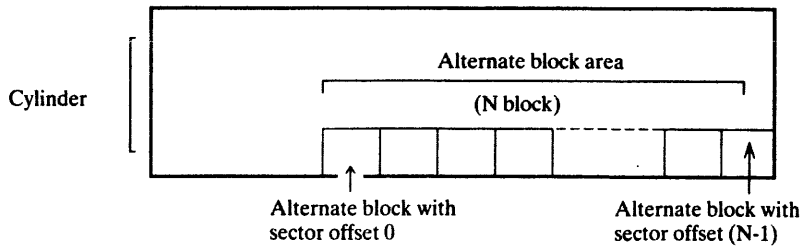


Figure 5.3 ID field structure

	ID					
	Byte 0	1	2	3	4	5
	76543210	76543210	76543210	76543210	76543210	76543210
Primary area normal	000000C Y Flag L H	Low-order cylinder address	Head address	Block Number	00000000	00000000
	Primary area (normal) block address					
Primary area defective (alternate block is on the same cylinder)	1001FFC Y Flag L H	Low-order cylinder address	Head address	Block Number	mmmmmmcc	Low-order alternate cylinder address
	Primary area (defective) block address				Alternate block address	
Primary area defective (alternate block is on different cylinder)	1000FFC Y Flag L H	Low-order cylinder address	Head address	Block Number	mmmmmmcc	Low-order alternate address
	Primary area (defective) block address				Alternate block address	
Alternate normal (unassigned)	010000C Y Flag L H	Low-order cylinder address	Head address	Block Number	00000000	00000000
	Alternate block address					
Alternate normal (assigned)	011000C Y Flag L H	Low-order cylinder address	Head address	Block Number	mmmmmmcc	Low-order alternate cylinder address
	Primary area (defective) block address				Alternate block address	
Alternate defective	1100FFC Y Flag L H	Low-order cylinder address	Head address	Block Number	00000000	00000000
	Alternate block address					

CYLH : High-order cylinder address
FF = 00 : The ID field is in its normal position.
01 : The ID field has been displaced twice.
10 : The ID field has been displaced once.
mmmmmm : Alternate block sector offset
cc : High-order alternate block cylinder address

Figure 5.4 Combinations of flag bits and ID field

5.2 Data Space Definition

Data space (a set of data blocks) in the drive is divided into three types; each space consists of a primary data block area (primary area) and an area reserved for alternate blocks (alternate area):

- User space: User data storage area
- CE space: Area reserved for the diagnostic purposes
- System space:Area for exclusive use of the controller

The system space may not be accessed explicitly by any user. Other spaces may be accessed using the block addressing techniques described in Section 5.3.

An alternate area is provided on the last track of each cylinder to avoid cylinder switching when processing defective blocks. Normally the alternate blocks are assigned in the same cylinder. They are only assigned in an adjacent cylinder when all of the alternate blocks on the same cylinder have been exhaused.

Figure 5.5 and Table 5.2 show the data space configuration.

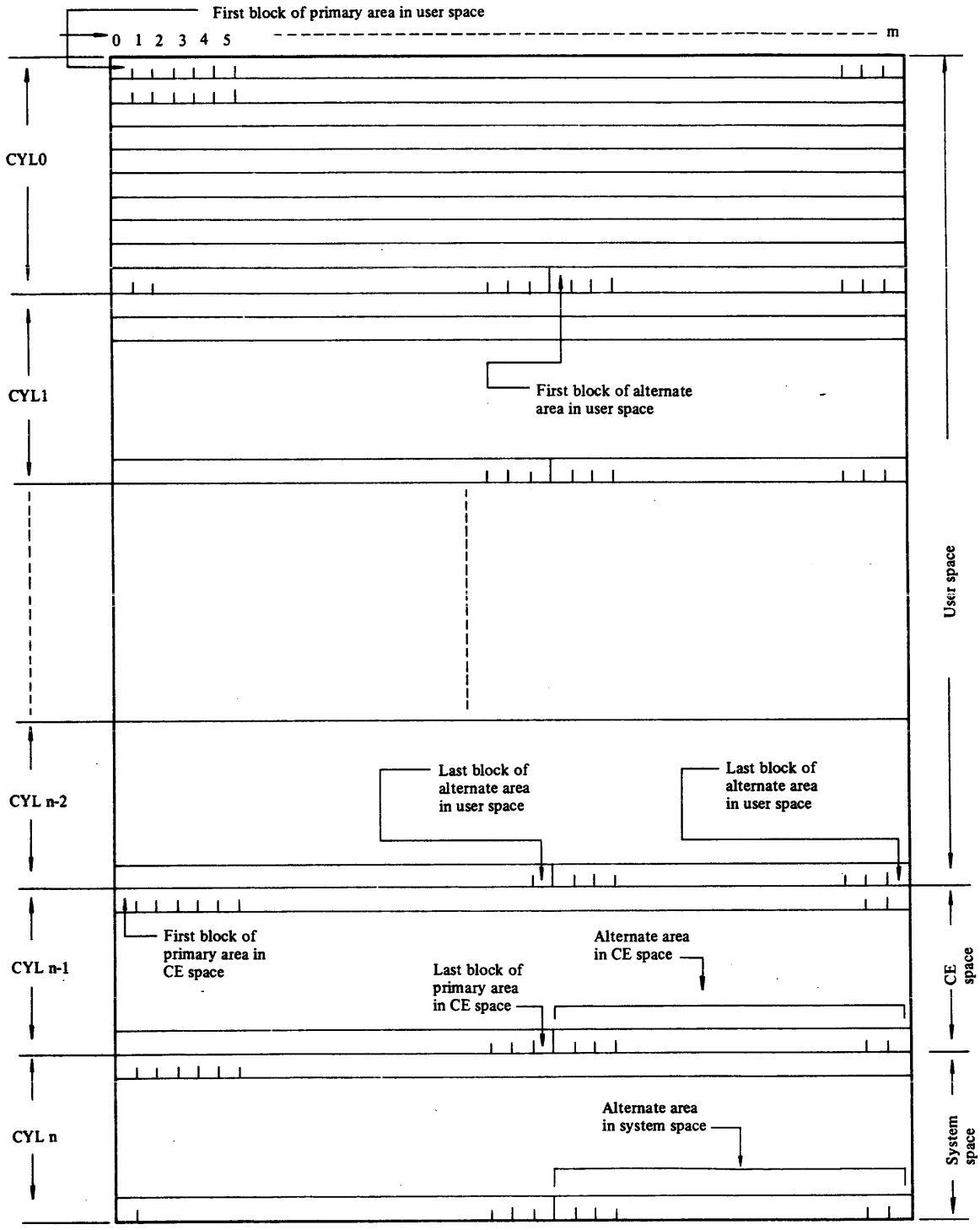


Figure 5.5 Data space configuration

Table 5.2 Data space configuration (1/2)

		M2333KS		
		S1 (256 bytes)	S2 (512 bytes)	S3 (1,024 bytes)
Cylinders/drive		823		
Tracks/cylinder		10		
Capacity	Unformatted/ drive (Bytes)	337,100,800		
	Formatted/ drive (Bytes)	254,432,480	290,749,440	311,818,240
User space	Cylinders	821 (0–820)		
	Primary blocks/ cylinder	1,170	660	350
	Total number of primary blocks	960,570	541,860	287,350
	Total primary area capacity (Bytes)	245,905,920	277,432,320	294,246,440
	Alternate blocks/ cylinder	40	30	20
	Total number of alternate blocks	32,840	24,630	16,420
CE space	Cylinder	1 (821)		
	Primary blocks/ cylinder	1,170	660	350
	Total primary area capacity (Bytes)	299,520	337,920	358,400
	Alternate blocks/ cylinder	40	30	20
System space	Cylinder	1 (822)		
	Primary blocks/ cylinder	1,170	660	350
	Total primary area capacity (Bytes)	299,520	337,920	358,400
	Alternate blocks/ cylinder	40	30	20

Table 5.2 Data space configuration (2/2)

		M2331KS		
		S1 (256 bytes)	S2 (512 bytes)	S3 (1,024 bytes)
Cylinders/drive		823		
Tracaks/cylinder		5		
Capacity	Unformatted/ drive (Bytes)	168,550,400		
	Formatted/ drive (Bytes)	127,466,240	145,374,720	155,909,120
User space	Cylinders	821 (0–820)		
	Primary blocks/ cylinder	565	320	170
	Total number of primary blocks	463,865	262,720	139,570
	Total primary area capacity (Bytes)	118,749,440	134,512,640	142,919,680
	Alternate blocks/ cylinder	40	25	15
	Total number of alternate blocks	32,840	20,525	12,315
CE space	Cylinder	1 (821)		
	Primary blocks/ cylinder	565	320	170
	Total primary area capacity (Bytes)	144,640	163,840	174,080
	Alternate blocks/ cylinder	40	25	15
System space	Cylinder	1 (822)		
	Primary blocks/ cylinder	565	320	170
	Total primary area capacity (Bytes)	144,640	163,840	174,080
	Alternate blocks/ cylinder	40	25	15

5.3 Block Addressing

The logical block addressing independent of the physical structures of drives is used to access data in a drive. IDC also allows access to the data using the cylinder/head/block number through diagnostic commands (Group 6).

5.3.1 Logical block addressing

The logical block addressing permits data blocks to be addressed in ascending number sequence for the respective drives. The logical block addresses are independent of each user accessible space, user space and CE space, and also independent of primary area and alternate area in each space. The logical block address of the first block in each space and each area is '0'. For a primary area in the user space, for example, serial block addresses are assigned to the respective blocks ranging from the leading block (logical block address = '0' at cylinder 0, head 0, block 0) to the last block of the primary area in the user space.

The alternate block area in each space is excluded from the logical block address space for the primary area. Alternate blocks have own serial logical block addresses, with the address of the first alternate block on the first cylinder for each space set to '0' and the address of the last alternate block on the last cylinder set to 'n'. However, because access to an alternate block is automatically performed within the controller, users need not be concerned with the logical block address for the alternate area except that an alternate block address must be specified explicitly in a specific command.

5.3.2 Cylinder/head/block number specification

This addressing method can only be used for group-6 commands.

Specify a block address at bytes 2 to 5 of a CDB by a cylinder/head/block number when PA = '1', where bit 0 of CDB byte 1 is defined as the physical address (PA) bit.

This addressing method requires the user to be concerned with the physical structure of the disk drive. Note that the block number does not agree with the sector number if sector interleaving is used and the block numbers for an alternate block are consecutive number from the last block of a primary area on the track where an alternate area resides.

5.3.3 Data space declaration

To access the data block on each data space other than primary area of the user space, the data space shall be declared by a set File Mask command, and the CDB which specified the data block address shall be issued as a linked command after the Set File Mask command. This is required for both addressing mode, logical block addressing and cylinder/head/block number specification.

The ALT and CE bits in the CDB of Set File Mask command declares the data space to be accessed as shown below:

(ALT)	(CE)	
0	0	Primary area of user space (Default)
1	0	Alternate area of user space
0	1	Primary area of CE space
1	1	Alternate area of CE space

5.3.4 Block address calculation

The address conversion method between the logical block address and cylinder/head/block number each other is as follows:

Symbols

BT:	Number of blocks/track (average)	These values can be read by using the Read Device Characteristics command.
BC:	Number of blocks/cylinder	
BU:	Number of blocks/user space	
AU:	Number of alternate blocks/user space	
HD:	Number of heads	HD = BC/BT
CU:	Number of cylinders in user space	CU = BU/BC
AC:	Number of alternate blocks/cylinder	AC = AU/CU
ST:	Number of sectors/track	ST = BT + AC/HD

(1) Logical block address (L) → Cylinder (C)/head (H)/block (B)

- Primary area of user space:
  C = (L − (L mod BC))/BC
  H = {(L mod BC) − ((L mod BC) mod ST)}/ST
  B = (L mod BC) mod ST

- Primary area of CE space:
  C = CU
  H = (L − (L modd ST))ST
  B = L mod ST

- Alternate area of user space:
  C = (L − (L mode AC))/AC
  H = HD
  B = (L mod AC) + ST − AC

- Alternate area of CE space:
  C = CU
  H = HD
  B = L + ST − AC

(2) Cylinder (C)/head (H)/block (B) → Logical block address (L)

- Primary area of user space: $L = C \times BC + H \times ST + B$
- Primary area of CE space: $L = H \times ST + B$
- Alternate area of user space: $L = C \times AC + B - ST + AC$
- Alternate area of CE space: $L = B - ST + AC$

CHAPTER 6 COMMANDS

6.1 Outline

6.1.1 CBD format

A command descriptor block (CDB) which is transferred from an INIT in the Command phase gives operational commands to a TARG.

The three high-order bits of byte 0 of the CDB constitute a group code field specifying a command group number and the CDB length. IDC uses the following command groups:

- Group 0: 6-byte long CDB (Basic commands)
- Group 1: 10-byte long CDB (Extended commands)
- Group 6: 10-byte long CDB (Diagnostic commands)

The five low-order bits of byte 0 are the command code field.Figures 6.1 to 6.3 show the basic formats of the respective group CDB's.

Byte \ Bit	7	6	5	4	3	2	1	0
00	0	0	0	Command code				
01	LUN			Logical block address (MSB)				
02	Logical block address							
03	Logical block address (LSB)							
04	Transferring block count							
05	Control byte							

Figure 6.1 Group-0 CDB basic format

Byte \ Bit	7	6	5	4	3	2	1	0
00	0	0	1	Command code				
01	LUN			0	0	0	0	Rel.
02	Logical block address (MSB)							
03	Logical block address							
04	Logical block address							
05	Logical block address (LSB)							
06	0	0	0	0	0	0	0	0
07	Transferring block count (MSB)							
08	Transferring block count (LSB)							
09	Control byte							

Figure 6.2 Group-1 CDB basic format

Byte \ Bit	7	6	5	4	3	2	1	0
00	1	1	0	Command code				
01	LUN			0	0	0	0	PA
02	Logical block address (MSB)/Cylinder (MSB)							
03	Logical block address/Cylinder (LSB)							
04	Logical block address/Head							
05	Logical block address (LSB)/Block							
06	Modifier byte							
07	Transferring block count (MSB)							
08	Transferring block count (LSB)							
09	Control byte							

Figure 6.3 Group-6 CDB basic format

(1) Group code field specifies a CDB format and its byte length.

(2) Command code field specifies the commands to be executed.

(3) Logical unit number (LUN) field specifies the address of a device attached to the IDC when the Identify message is not implemented. The INIT can specify the device address (LUN) by way of an Identify message upon completion of the selection phase. In this case, the IDC ignores the contents of the LUN field in the CDB.

(4) Logical block address field indicates the start address of the block to be processed in the device.

(5) Relative address bit: The logical block address field of a CDB indicates the two's complement displacement which is added to the block address last accessed by the preceding command in the same command link when the relative address bit (bit 0 of group-1 CDB byte 1) is '1'.

(6) Physical address bit: The block address field of the CDB indicates the block to be processed by the command in Cylinder/Head/Block number when the physical address (PA) bit (bit 0 of group-6 CDB byte 1) is '1'.

(7) Transferring block count field specifies the number of blocks to be transferred between the INIT and IDC. This field in a CDB may specify a transferring byte count or have no meaning, depending on the type of the command specified.

(8) Control byte

Bit 7	6	5	4	3	2	1	0
0	0	0	0	0	0	Flag	Link

- Bit 0: Link

  A command link is specified when this bit is '1'.

- Bit 1: Flag

  This bit is only valid when the link bit is set to '1'. When the command terminates successfully, the Linked Command Complete with Flag message is sent to the INIT if this bit is '1', and the Linked Command Complete message is sent if this bit is '0'.

6.1.2 Outline of command processing

(1) Single command

The following shows an example of processing a single command. This is the most basic SCSI operation. Although some commands may be accompanied by a disconnection/reconnection before the completion of command execution, this function in not described in the following example. See Subsection 6.1.3 for details about the disconnection/reconnection function.

① The INIT sets the command pointer, data pointer, and status pointer to the initial values for the command to be issued.

② The INIT obtains control of the SCSI bus through the Arbitration phase and then selects the TARG in the Selection phase.

③ If an Attention condition occurs, the TARG executes the Message Out phase and normally receives an Identify message which specifies the LUN to be accessed.

④ The TARG receives a CDB from the INIT in the Command phase. The link bit of the control byte in the CDB is '0'.

⑤ The TARG interprets the command and executes the requested operation. If the command requires data transfer at the SCSI, the Data In or Data Out phase is executed.

⑥ The TARG sends the status byte indicating a result of command execution to the INIT in the Status phase upon termination of command execution.

⑦ The TARG sends Command Complete message in the Message In phase and then goes to the Bus Free phase.

(2) Command link

The command link facility enables a TARG to execute two or more commands successively. Issue of the first command by the INIT and the execution of the first command is the same operation as the above single command example, except for the following:

- The link bit of the control byte of the CDB transferred at step ④ is '1'.
- The status byte reported at step ⑥ upon successful completion of the command indicates "Intermediate" status and the link facility is then executed.
- Either the Linked Command Complete or Linked Command Complete with Flag message is sent at step ⑦ depending on the value of the flag bit of the CDB.

The INIT updates the pointers to the initial values of the next command upon receipt of the Linked Command Complete (with Flag) message. The TARG executes the Command phase after the Message In phase to obtain the command to be executed next.

The command link continues until a command is issued with the link bit of the CDB is '0' or a command terminates abnormally with "Check Condition" status. Only a single LUN can be operated by a series of linked commands.

If the relative address bit in a CDB (group-1) issued by the command link facility is set to '1', the logical address field of the CDB is treated as a positive or negative displacement value (two's complement). The address of the data block to be accessed by the command is formed by adding the displacement value to the address of the block accessed most recently by the preceding command.

6.1.3 Disconnection/reconnection

If any processing which requires no SCSI operation is to be performed during command execution in a TARG, the TARG can disconnect the SCSI bus, and then execute the command within the TARG. This facility enables the INIT to perform multiprocessing on the SCSI bus.

To disconnect the SCSI, the TARG sends a Disconnect message to the INIT and then goes to the Bus Free phase. In this case, the TARG may request the pointer operation before issuing the Disconnect message.

The TARG performs the command execution within itself and then reconnects the INIT when SCSI operation again becomes necessary. For the reconnection, the TARG obtains control of the SCSI bus through the Arbitration phase and reselects the INIT by executing the Reselection phase. Then, the TARG notifies an LUN requiring reconnection by issuing the Identify message. The INIT restores the pointers for the specified LUN to restart command execution.

IDC operating as TARG executes the above disconnection/reconnection processing when all the following conditions are satisfied, that is a disconnection is permitted:

(1) The system has an Arbitration phase and use of the Arbitration phase is enabled by the setting switches in IDC.

(2) The SCSI ID of an INIT has been notified in the Selection phase.

(3) The INIT has permitted disconnection in the Identify message issued after the Selection phase.

Normally, IDC becomes ready to accept a new I/O request from SCSI after the disconnection.

6.2 Commands

Tables 6.1 to 6.3 list the commands implemented on the IDC. Symbols in these tables denote the following:

- Type

S:	Standard	Commands defined in SCSI standard
E:	Extended	
O:	Optional	
FJ:	Fujitsu original (vendor unique) command	

- CDB

a:	Address of data block to be processed
b:	Number of bytes to be transferred
c:	Control bits field
d:	Address of data buffer to be processed
f:	Control flags
i:	Interleaving factor
l:	Number of data blocks to be processed
m:	Modifier field
u:	LUN

- Data Transfer

−:	No data is transferred on SCSI during command execution
T→I:	Data is transferred from TARG to INIT
I→T:	Data is transferred from INIT to TARG
( ):	Data transfer may or may not occur depending on the CDB specification

- Disconnection

−:	SCSI disconnection does not occur during command execution if no error is detected. If any error which requires seek or rezero operation to recover the error occurs, SCSI disconnection may be performed.
×:	SCSI disconnection occurs during command execution if the INIT permits the disconnection.

Table 6.1 Group 0 commands

Command	Type	CDB (HEX)						Data Transfer	Discon-nection	Remarks
		00	01	02	03	04	05			
Test Unit Ready	O	00	u0	00	00	00	0f	—	—	
Rezero Unit	O	01	u0	00	00	00	0f	—	×	
Request Sense	S	03	u0	00	00	bb	0f	T→I	—	
Format Unit	S	04	uc	00	00	ii	0f	(I→T)	×	
Reassign Blocks	O	07	uc	00	00	00	0f	I→T	×	
Read	S	08	ua	aa	aa	ll	0f	T→I	×	
Write	S	0A	ua	aa	aa	ll	0f	I→T	×	
Seek	O	0B	ua	aa	aa	00	0f	—	×	
No Operation	FJ	0D	u0	00	00	00	0f	—	—	
Set File Mask	FJ	0F	um	mm	00	00	0f	—	—	
Inquiry	E	12	u0	00	00	bb	0f	T→I	—	
Read Device Characteristics	FJ	13	u0	00	00	bb	0f	T→I	—	
Priority Reserve	FJ	14	u0	00	00	00	0f	—	—	
Mode Select	O	15	uc	00	00	bb	0f	I→T	—	
Reserve Unit	O	16	uc	00	00	00	0f	—	—	
Release Unit	O	17	uc	00	00	00	0f	—	—	
Copy	O	18	uc	bb	bb	bb	0f	I→T	—	
Mode Sense	O	1A	u0	mm	00	bb	0f	T→I	—	
Receive Diagnostic Results	O	1C	u0	00	bb	bb	0f	T→I	—	
Send Diagnostic	O	1D	uc	00	bb	bb	0f	(I→T)	×	

Table 6.2 Group 1 commands

Command	Type	CDB (HEX)										Data Transfer	Discon-nection	Remarks
		00	01	02	03	04	05	06	07	08	09			
Search Block High	FJ	20	uc	aa	aa	aa	aa	00	ll	ll	0f	I→T	×	
Search Block Equal	FJ	21	uc	aa	aa	aa	aa	00	ll	ll	0f	I→T	×	
Search Block Low	FJ	22	uc	aa	aa	aa	aa	00	ll	ll	0f	I→T	×	
Read Capacity	E	25	uc	aa	aa	aa	aa	00	00	0c	0f	T→I	×	
Read Extended	E	28	uc	aa	aa	aa	aa	00	ll	ll	0f	T→I	×	
Write Extended	E	2A	uc	aa	aa	aa	aa	00	ll	ll	0f	I→T	×	
Seek Extended	O	2B	uc	aa	aa	aa	aa	00	00	00	0f	—	×	
Verify	O	2F	uc	aa	aa	aa	aa	00	ll	ll	0f	(I→T)	×	
Set Limits	O	33	uc	aa	aa	aa	aa	00	ll	ll	0f	—	—	
Read Defect Data	O	37	u0	cc	00	00	00	00	bb	bb	0f	T→I	×	
Writer Buffer	O	3B	uc	00	00	dd	dd	00	bb	bb	0f	I→T	—	
Read Buffer	O	3C	uc	00	00	dd	dd	00	bb	bb	0f	T→I	—	

Table 6.3 Group 6 commands

Command	Type	CDB (HEX)										Data Transfer	Discon-nection	Remarks
		00	01	02	03	04	05	06	07	08	09			
Format ID	FJ	C4	uc	aa	aa	aa	aa	mm	00	00	0f	—	×	
Space ID & Read Data	FJ	C6	uc	aa	aa	aa	aa	00	00	00	0f	T→I	×	
Displaced ID	FJ	C8	u0	00	00	00	00	mm	00	00	0f	—	—	
Read ID	FJ	CA	uc	aa	aa	aa	aa	00	ll	ll	0f	T→I	×	

6.2.1 Group-0 commands

(1) Test Unit Ready

This command checks whether a specified device is ready or not. A status byte with a "Good" status is reported when the specified device has been powered on and is ready for use by the INIT.

(2) Rezero Unit

This command selects a specified device and resets the seek error condition, then moves the head to the cylinder 0/track 0 position.

(3) Request Sense

This command transfers sense data to the INIT.

The sense data implemented on IDC is the Extended Sense Format only, 36-byte long. See Chapter 7 for details about sense data.

(4) Format Unit

This command ensures that the medium is formatted so that all of the initiator addressable data blocks can be accessed. By executing this command, all initiator addressable data blocks are filled with X'00' pattern.

During the execution of this command, the IDC performs a medium defect management scheme which can be selected by the INIT through control field of the CDB. The INIT also can format the drive with sector interleaving by specifying Interleaving Factor in the CDB.

(5) Reassign Blocks

This command assigns alternate blocks according to the defect data list transferred from the INIT. The defect data list contains the logical block addresses of defective blocks.

Upon receipt of the Reassign Blocks command, IDC searches for an unused alternate block, then makes a linkage pointer between the alternate block and the defective block.

If a Reassign Blocks command is linked from a Displaced ID command, the ID field of the defective block is written into the position specified by the Displaced ID command.

The address of specified block on the defect data list which is sent from the INIT is preserved in "Grown Defect List" on the disk medium after successful completion of the reassignment.

(6) Read

This command reads the data fields for a specified number of blocks from the medium and transfers them to the INIT.

If two or more blocks are to be transferred by this command, IDC automatically executes head switching or cylinder switching when a track or cylinder boundary is reached.

Unless retry and data correction are inhibited, the data transferred to the INIT is error-free. In other words, when IDC detects a correctable data check, data is automatically corrected on the data buffer in the IDC.

(7) Write

This command writes the data transferred from the INIT into the data fields on the medium for a specified number of blocks.

To transfer two or more blocks, IDC automatically executes head or cylinder switching when a track or cylinder boundary is reached.

(8) Seek

This command requests the specified device to seek to the cylinder where the block specified exists.

(9) No Operation

This command performs a selection of the specified device and checking the status of the device. But, no other operation for the drive is performed.

(10) Set File Mask

This command defines the operational range of commands linked to this command or a subsequent command.

The INIT can define the data space on the device to be accessed and/or the operations which can be executed.

The restrictions when no Set File Mask command is used are as follows (default values):

- Only the primary area of user space is accessible.
- All write operations are permitted.
- Group-6 commands are inhibited.

(11) Inquiry

The inquity data, 36-byte long, transferred by this command represents the characteristics of a controller and its attached device.

This command is normally executed even if the specified device is not connected or the IDC retains pending unit attention condition.

(12) Read Device Characteristics

The characteristic data, 24-byte long, which is transferred to the INIT by this command contains the following information:

- Controller type code and Device type code
- Data block size and Interleaving factor used
- Number of blocks per track, cylinder, user space and CE space
- Number of alternate blocks per user space and CE space

(13) Priority Reserve

This command reserves forcedly the specified device from the INIT that issued this command even though the device is currently reserved or used by another INIT. Also, this command clears forcedly the sense data pending state even if the sense data has been preserved for another INIT with regard to the specified device.

(14) Mode Select

This command provides a means for the INIT to specify or to change the IDC's various parameters regarding the error recovery procedure and/or other specific features.

The IDC preserves the parameters specified by this command for each LUN and for each INIT. The parameters for each LUN and for each INIT could be different.

The supported parameters called "Page" are as follows:

(Page Code)

X'01'	Error Recovery Parameters
X'02'	Disconnect/Reconnect Control Parameters
X'03'	Format Parameters
X'04'	Geometry Parameters
X'21'	Additional Error Recovery Parameters
X'22'	Reconnection Timing Control Parameters
X'3F'	Defined in Mode Sense only

(15) Reserve Unit

This command reserves a specified device for the INIT issuing this command. Further, the third-party reservation feature implemented on this command allows an INIT to reserve a logical unit for another SCSI device. This feature is intended for use in multiple-initiator systems that use the Copy command.

(16) Release Unit

This command releases the reserved state of the device (if any) related to the INIT that issued this command. The third-party release feature implemented on this command allows an INIT to release a logical unit that was previously reserved using the third-party reservation. This feature is intended for use in multiple-initiator systems that use the Copy command.

(17) Copy

This command copies (transfers) data between the devices or between the areas in the same device. The devices or the areas to be copied are specified in the parameter list transferred by this command. The parameter list specifies the source device from which data is to be read, the destination device to which data is to be written, source logical block address, destination logical block address, and source block count.

The copy operation is only enabled between the devices under the same IDC. IDC reads data for the number of blocks specified in the source block count from the source LUN. Then, IDC writes the data to the destination LUN.

When the source device is different in block size (data length) from the destination device, IDC assembles or disassembles the data read from the source device so that the block size can agree with that for the destination device.

(18) Mode Sense

This command provides a means to report the various parameters concerning the medium, logical unit, error recovery or disconnection/reconnection feature to the INIT. It is a complementary command to the Mode Select command.

The INIT shall issue a Mode Sense command prior to issuing a Mode Select command in order to find out which pages are implemented and which fields or bits are changeable for the particular LUN. An INIT may request a particular block of parameters called "Page" to be returned by the IDC by selecting its code in the CDB.

The IDC supports the following Page Codes for this command:

(Page Code)

X'01'	Error Recovery Parameters
X'02'	Disconnect/Reconnect Control Parameters
X'03'	Format Parameters
X'04'	Geometry Parameters
X'21'	Additional Error Recovery Parameters
X'22'	Reconnection Timing Control Parameters
X'3F'	Return all pages

(19) Receive Diagnostic Results

This command sends data which indicates the results of testing by the diagnostic routine executed by a Send Diagnostic command to the INIT. See Chapter 9 for details.

(20) Send Diagnostic

This command activates a diagnostic routine which tests IDC itself or IDC and a specified device for a certain function.

The INIT specifies the type of the test to be performed by the self test bit and the unit offline bit in the CDB or by parameters transferred by this command. See Chapter 9 for details.

6.2.2 Group-1 commands

(1) Search Block High

This command compares data read from the device with data transferred from the INIT, and searches the block which satisfies the following condition:

(Data in device) > (Data transferred from INIT)

For the data comparison, the leading byte positions of data transferred from the INIT and data read from the device are treated as the MSB. The other functions of this command conform to those of the Search Block Equal command.

(2) Search Block Equal

This command compares data read from the device with data transferred from the INIT within a specified searching block count, and searches an all-byte position matched block.

Data transferred from the INIT by this command must be one-block long. Data comparison is always done in block units. To limit the range of data comparison in a single block, assign data pattern X'FF' to data transferred from the INIT to exclude the corresponding byte position from the comparison range. Data is compared on a byte-by-byte basis from the first byte of each block, excluding the X'FF'-specified byte positions.

If the invert bit in the CDB is set to '1', the search condition is satisfied when comparison is unsuccessful. In other words, the search condition of the Search Block Equal command is changed to "not equal", the search condition of the Search Block High command is changed to "less than or equal", and the search condition of the Search Block Low command is changed to "greater than or equal".

(3) Search Block Low

This command compares data read from the device with data transferred from the INIT, and searches the block which satisfies the following condition:

(Data in device) < (Data transferred from INIT)

For the data comparison, the leading byte positions of data transferred from the INIT and data read from the device are treated as the MSB. The other functions of this command conform to those of the Search Block Equal command.

(4) Read Capacity

This command returns the information regarding the capacity of a specified device to the INIT.

- If the PMI (Partial Medium Indicator) bit of the CDB is set to zero, the IDC reports the logical block address of the last initiator addressable data block on the specified device and the block length (in bytes).

- If the PMI bit is set to one, the IDC reports the last logical block address after which a substantial delay in data transfer will be encountered and the block length (in bytes). The IDC reports the logical block address of the block which is located on the first cylinder boundary or the last block which is not assigned as a defective block, whichever is encountered first.

(5) Read Extended

This command has the same functions as group-0 Read command except that the logical block address and the transferring block count fields of the CDB are expanded.

(6) Write Extended

This command has the same functions as group-0 Write command except that the logical block address and the transferring block count fields of the CDB are expanded.

(7) Seek Extended

The operation of this command is the same as group-0 Seek command except that the logical block address field of the CDB is four-byte long.

(8) Verify

This command verifies data recored on the medium. When the byte check bit (bit 1 of CDB byte 1) is '0', IDC reads the data in the specified blocks and performs an ECC check on the data for verification. No data is then transferred between INIT and IDC. If the byte check bit of the CDB is '1', IDC compares the data read from the device with the data transferred from the INIT for verification.

(9) Set Limits

This command defines a range can be accessed and operations can be performed by any command linked to this command or a subsequent command.

A command linked to this command or a subsequent command can only access to the blocks falling within the range specified by this command. If the read inhibit or write inhibit bit of the CDB is set to '1', any subsequent linked commands cannot perform read or write operations, respectively.

(10) Read Defect Data

This command transfers the medium defect data of the specified device to the INIT.

The IDC supports the Physical Sector Format for the returned defect data, which indicates cylinder, head and defective sector number.

(11) Write Buffer

This command is used in conjunction with the Read Buffer command as a diagnostic function for testing the IDC's data buffer memory and the SCSI bus integrity.

The IDC stores the data transferred from the INIT into its data buffer from the specified buffer address. The size of data buffer implemented in the IDC and available address range are as follows.

Buffer size	Address range
16 KB	X'0000' to X'3FFF'

(12) Read Buffer

This command is used in conjunction with the Write Buffer command as a diagnostic function for testing the IDC's data buffer memory and the SCSI bus integrity.

The IDC transfers data from its data buffer to the INIT from the specified buffer address. The returned buffer data is to be used by the INIT for comparison with data pattern sent during the Write Buffer command.

6.2.3 Group-6 commands

(1) Format ID

This command writes the ID field of the specified block according to the modifier byte (CDB byte 6) which specifies a method of writing an ID field as listed below.

- Formats a block of primary area as normal block.
- Formats a block of alternate area as an unused normal block.
- Formats a block of alternate area as defective block; the ID field is written in normal position, displaced once position, or displaced twice position according to specification of the CDB.

(2) Space ID & Read Data

This command reads the data field of a specified block with no verification check on the ID field and transfers the data to the INIT. This command is useful in reading the data field of a block which cannot be read normally because of an unrecoverable error of the ID field etc.

(3) Displaced ID

This command specifies a method of processing for the succeeding Reassign Blocks command. The modifier byte of the CDB specifies the position to which the ID field of the defective block is to be written by the Reassign Blocks command linked to this command. This command is effective when data check occurs intermittently in the ID field of a defective block.

(4) Read ID

This command reads the ID fields from the medium and transfers them to the INIT. The data transferred to the INIT by this command is the same format as the ID field written on the medium.

If the ID field of a specified block is not in the normal position, the ID field in the displaced once or displaced twice position is read.

6.3 Data Buffer Management

6.3.1 Buffer configuration

The 16 KB data buffer consists of dual 8 KB buffers to assist two types of buffer operations, full buffering mode and dual sector buffer mode. The former aims at improvement of the total system throughput while the latter provides quick response time.

In both buffering mode, the whole buffer storage is commonly used by all LUNs attached to the IDC.

The INIT can specify which type of buffer operation is to be used through a Mode Select command as described below. The default mode of buffer operation after Power on or SCSI Reset condition is a full buffering mode.

Note that it is not always necessary to use the sector interleaving when using the full buffering mode even if the data transfer rate on SCSI bus is slower than the data transfer rate of the attached device.

6.3.2 Read operation

(1) Full buffering mode

If a Buffer Full Ratio parameter of the Mode Select parameters Page 2 is set to no-zero value, the full buffering mode is specified.

The IDC requests the reconnection to the INIT after the specified number of data blocks have been stored into the data buffer. If the specified data blocks are greater than the maximum size of the data buffer (16 KB), the IDC executes reconnection and disconnection at each time that the 16 KB bytes of data have been transferred.

(2) Dual sector buffer mode

If a Buffer Full Ratio parameter of the Mode Select parameters Page 2 is set to zero, the dual sector buffer mode is specified.

The data read from a disk drive is stored temporarily into the each data buffer with every data block, and then sent to SCSI. Figure 6.4 is an outline of read operation. Note that the read/write head position on the disk medium precedes the data block transferred at SCSI by one block.

As shown in Figure 6.4, read operations are performed on block N + 1 in the drive while SCSI is transferring block N. If transferring block N has not yet been completed in SCSI when reading block N + 2 is started, a data overrun occurs. If the data overrun occurs, the IDC continues data transfer of block N and N + 1 on SCSI, then it repositions to the block N + 2 after waiting one revolution of the disk and continues the read processing from the block N + 2.

To avoid the data overrun when reading the data fields of contiguous blocks with dual sector buffer mode, the data transfer rate required in SCSI can be estimated by the following expression:

(SCSI average data transfer rate) $\geqq$

$$\text{(Disk drive data transfer rate)} \times \frac{\text{(Data field length)}}{\text{(Physical sector length)}}$$

If this condition is not satisfied, decrease the data transfer speed through sector interleaving. See Subsection 6.3.4 for details about interleaving.

When the dual sector buffer mode is used, the IDC requests a reconnection to the INIT in P sectors advance of the specified leading data block after the completion of positioning to the track on which the data block exists.

The INIT can specify the value of P through Mode Select Parameters Page 22, Reconnection Timing Control Parameters.

The default value of P depends on the type and data format of the drive as shown in Table 6.4. In Table 6.4, Trps shows the time from beginning of the Reselection phase for reconnection to the leading data block. If the value of P is specified by the INIT, use the following formulas to obtain Trps.

- Trps (MIN) $\fallingdotseq$ (P−1) × Tsct − 160 (μ s)
- Trps (TYP) $\fallingdotseq$ (P−0.5) × Tsct − 150 (μ s)

Where, Tsct is 138 for 256-byte format, 240 for 512-byte format and 450 for 1,024-byte format. If the specified P is smaller than the default value, the specified value is ignored then the default value is used.

Table 6.4 Read reconnection timing default value in dual sector buffer mode

Drive type		M2333KS/M2331KS		
Data format		256 B/sector	512 B/sector	1,024 B/sector
P (sectors)		6	4	3
Trps (μs)	MIN	530	560	740
	TYP	609	690	975

Before the leading data block is encountered, it is required to complete the reconnection. A sector overrun occurs when the leading data block has been passed because of delayed response from the INIT in the reconnection sequence. If the sector overrun occurs, the processing for the data block starts after waiting one revolution of the disk. For details about the timing requirements, see Appendix B, Subsection B.2.1.

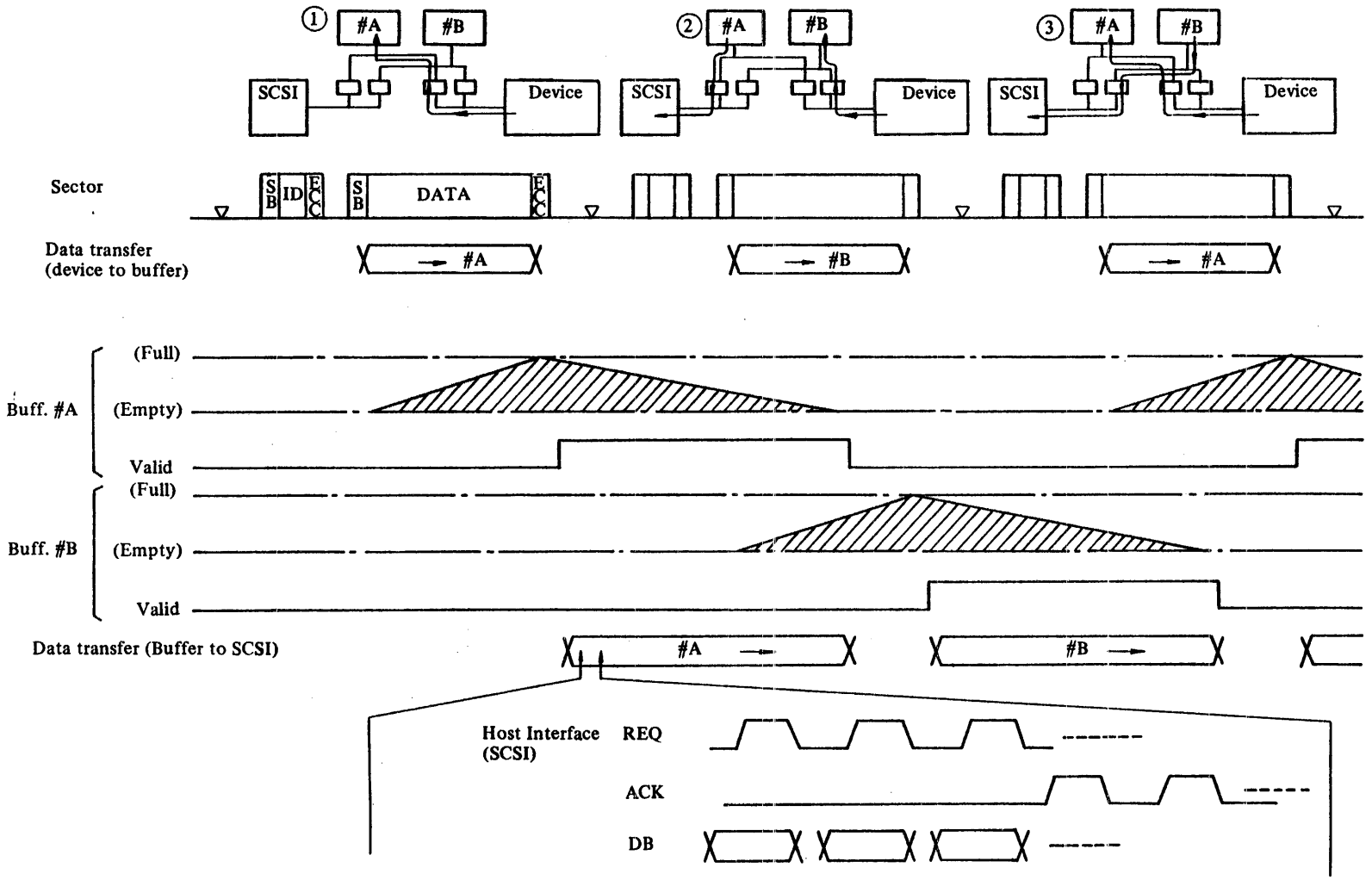


Figure 6.4 Dual sector buffer mode for read operation

6.3.3 Write operation

(1) Full buffering mode

If a Buffer Empty Ratio parameter of the Mode Select parameters Page 2 is set to non-zero value, the full buffering mode is specified.

The IDC requests the reconnection to the INIT after the positioning to the specified track has been completed. Then requests the data transfer (Data Out phase) to prefetch the data to be written onto the specified block. After the data of the specified number of blocks have been prefetched into the data buffer, the IDC disconnects the SCSI bus and performs the write operation. If the specified data blocks are greater than the maximum size of the data buffer (16 KB), the IDC executes disconnection and reconnection at each time that the 16 KB of data have been transferred.

(2) Dual sector buffer mode

If a Buffer Empty Ratio parameter of the Mode Select parameters Page 2 is set to zero, the dual sector buffer mode is specified.

Data received from SCSI is temporarily stored in the each buffer in block units. After data for one block has been prefetched, the data is written onto a disk medium. Figure 6.5 shows an outline of write operation. Note that the data block transferred from SCSI precedes the read/write head position on the disk medium by about one block.

As shown in Figure 6.5, when writing data to contiguous blocks, data to be written to block N + 1 is transferred from SCSI while a write operation for block N is being performed on a drive. If this data prefetch has not been completed before the start of a write operation for block N + 1 on the drive, a data overrun occurs.
In this case, all bytes of the block N + 1 are filled with X'00'. However, the data prefetching for the block N + 1 is executed continuously and the data is written onto the block N + 1 after one revolution.

To avoid data overrun when writing data to the data fields of contiguous blocks with dual sector buffer mode, the data transfer rate required in SCSI is estimated by the following expression:

(SCSI average data transfer rate) $\geqq$

$$\text{(Disk drive data transfer rate)} \times \frac{\text{(Data field length)}}{\text{(Physical sector length)}}$$

If this condition is not satisfied, decrease the data transfer speed using sector interleaving. See Subsection 6.3.4 for details about interleaving.

When the dual sector buffer mode is used, the IDC requests a reconnection to the INIT in Q sectors advance of the specified leading data block after the completion of positioning to the track on which the data is to be written.

The INIT can specify the value of Q through Mode Select Parameters Page 22, Reconnection Timing Control Parameters.

The default value of Q depends on the type and data format of the drive as shown in Table 6.5. In Table 6.5, Trps shows the time from beginning of the Reselection phase for reconnection to the leading data block. If the value of Q is specified by the INIT, use the following formulas to obtain Trps:

- Trps (MIN) $\doteqdot$ (Q − 1) × Tsct − 145 (μs)
- Trps (TYP) $\doteqdot$ (Q − 0.5) × Tsct − 135 (μs)

Where Tsct is 138 for 256-byte format, 240 for 512-byte format and 450 for 1,024-byte format. If the specified Q is smaller than the default value, the specified value is ignored then the default value is used.

Table 6.5 Write reconnection timing default value in dual sector buffer mode

Drive type		M2333KS/M2331KS		
Data format		256 B/sector	512 B/sector	1,024 B/sector
Q (sectors)		6+m	4+m	3+m
Trps (μs)	MIN	683 if m=1	815 if m=1	1,205 if m=1
	TYP	762 if m=1	945 if m=1	1,440 if m=1

Note: m denotes an interleaving factor (m = 1 with no sector interleaving).

Before the leading data block is encountered, it is required to complete the reconnection, and at least one block of data must be prefetched. A sector overrun occurs when the leading data block has been passed because of delayed response from the INIT in the reconnection sequence. If the data prefetch is not in time, a data overrun occurs. In both cases, the processing for the data block starts after waiting one revolution of the disk. For details about the timing requirements, see Appendix B, Subsection B.2.2.

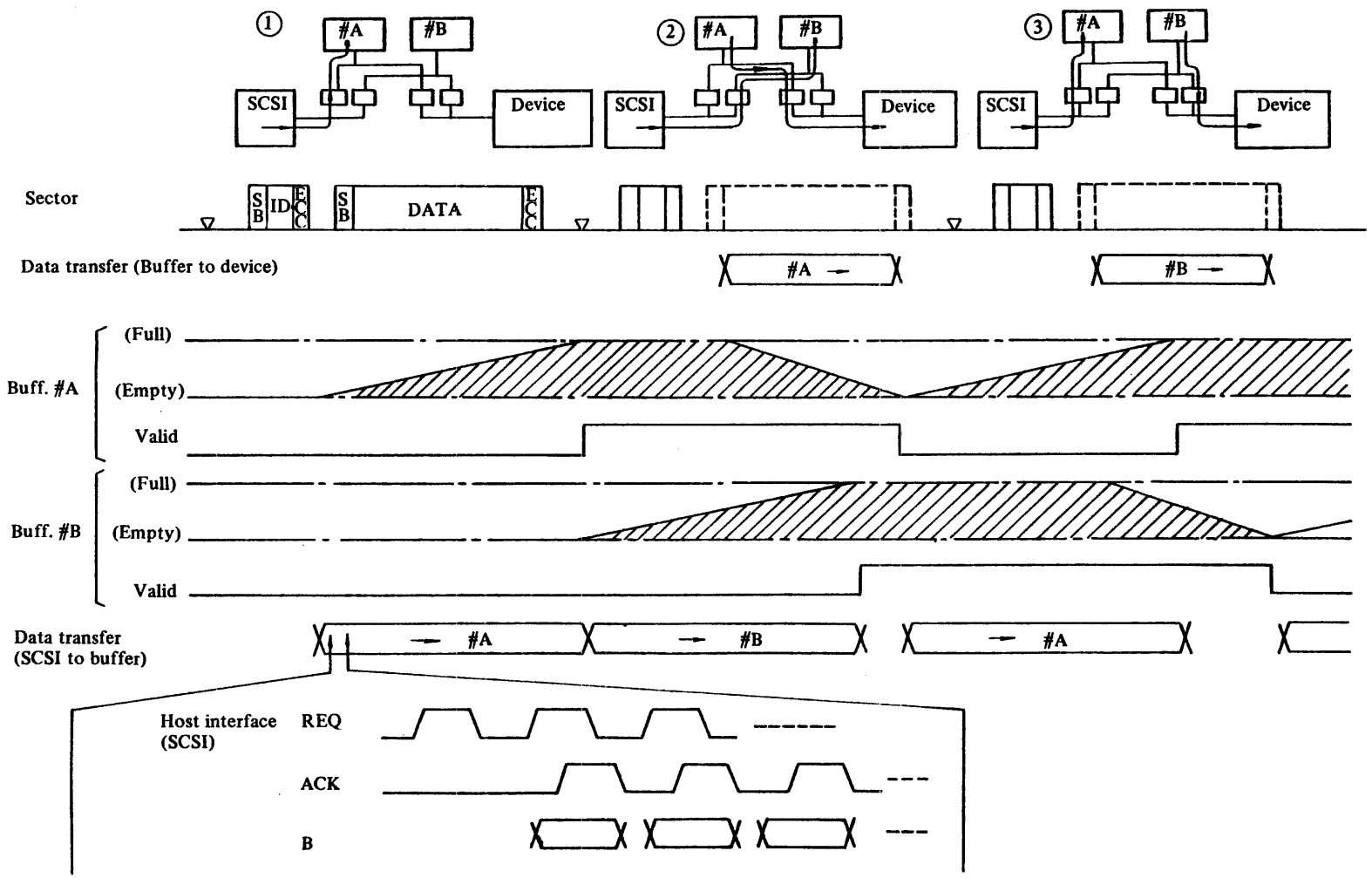


Figure 6.5 Dual sector buffer mode for write operation

6.3.4 Sector interleaving

Sector interleaving enables the data transfer rate required on SCSI during read or write operation of contiguous blocks with dual sector buffer mode to be decreased.

Note that it is not necessary to use the sector interleaving when the full buffering mode is selected.

To use sector interleaving, the user must reformat the disk drive by a Format Unit command. The Format Unit command permits a sector interval between blocks to be specified as an interleaving factor. The user need not be concerned with correspondences of blocks with their physical sector locations, because any data access after the completion of formatting is performed in accordance with the block arrangement.

In sector interleaving mode, the data blocks in a drive are accessed at intervals of m sectors, where m is determined by the interleaving factor. In read/write operations on contiguous blocks in the sector interleaving mode, the data buffer helps decrease data transfer rate required in SCSI. The data transfer rate in SCSI required to maintain contiguous block processing when the interleaving factor is m can be determined by the following expression:

(SCSI average data transfer rate) $\geqq$

$$\text{(Disk drive data transfer rate)} \times \frac{\text{(Sector data field length)}}{\text{(Physical sector length)} \times m}$$

(1) Interleaving factor specification

The interleaving factor is an integer representing the sector interval of the data blocks. When the interleaving factor is m, a single data block is allocated in every m sectors. When, however, m = 0, it is equivalent to specification m = 1(no interleaving).

The range of specifiable interleaving factors depends on the number of sectors per track, as follows:

$0 \leqq$ (m: interleaving factor) $\leqq$ ((Number of sectors per track) $-$ 1).

Where neither divisors (d) of the number of sectors per track nor multiples of d may be specified.

(2) Examples of sector interleaving

Figure 6.6 shows arrangements of data blocks corresponding to example of interleaving factors for a data format of 69 sectors per track.

Interleaving factor	Physical sector number/track																			
	0	1	2	3	4	5	6	7	8	9	10	11	12	61	62	63	64	65	66	67	68
0 or 1	0	1	2	3	4	5	6	7	8	9	10	11	12	61	62	63	64	65	66	67	68
2	0	35	1	36	2	37	3	38	4	39	5	40	6	65	31	66	32	67	33	68	34
3	Inhibited to specify																				
4	0	52	35	18	1	53	36	19	2	54	37	20	3	67	50	33	16	68	51	34	17
5	0	14	28	42	56	1	15	29	43	57	2	16	30	26	40	54	68	13	27	41	55
6	Inhibited to specify																				
7	0	10	20	30	40	50	60	1	11	21	31	41	51	58	68	9	19	29	39	49	59
68	0	68	67	66	65	64	63	62	61	60	59	58	57	8	7	6	5	4	3	2	1

Figure 6.6 Example of sector interleaving format

Figure 6.7 shows an example of reading and writing data where the interleaving factor = 2. Note that the data transfer in SCSI is done at a speed of one block/elapsing time of two sectors, even though the processing time required to process the same amount of data blocks becomes 2 times greater than no sector interleaving mode.

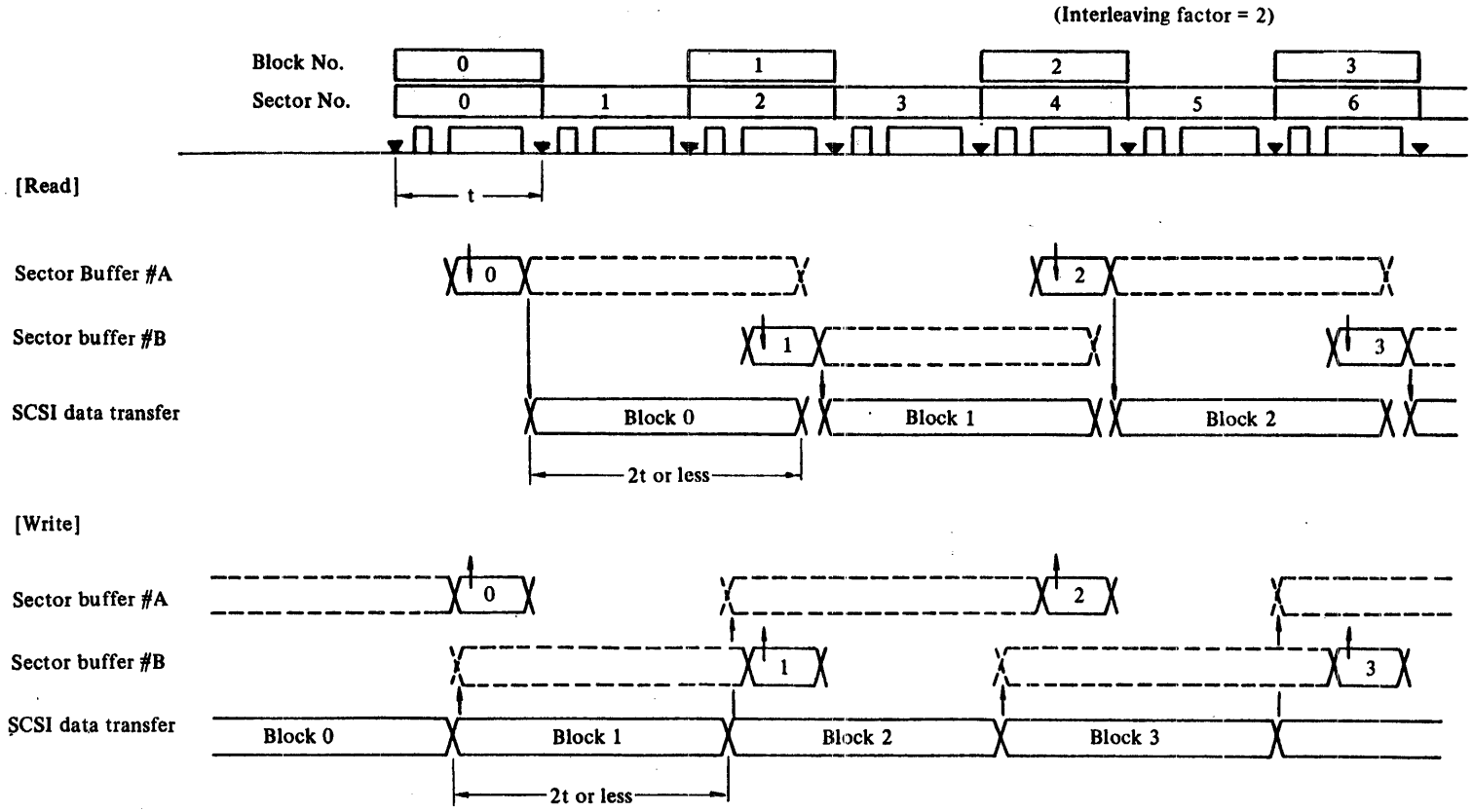


Figure 6.7 Example of read/write operation with sector interleaving

6.4 Command Queuing Feature

6.4.1 Command stacker

The IDC has multiple command stackers that can be used by each INIT to queue the commands.

The IDC can accept one command from all INITs (up to seven INITs) for each attached logical unit (LUN).

6.4.2 Queue management

If the command stackers for an LUN and for the INIT are not full, and a Send Diagnostic command for any LUN has not been received from any INIT, the IDC accepts any command other than a Priority Reserve command and queues it into the stackers as a secondary command even though the LUN has an active command. In this case, the IDC goes to the Bus Free phase immediately after receiving the secondary command by sending a Disconnect message.

If the Disconnect message is rejected by the INIT, the IDC goes to the Status phase and sends a "Busy" status, in this time, the secondary command is removed from the queue. If the INIT which issues the secondary command does not allow the disconnection, the IDC returns a "Busy" status and does not enter the command into the queue.

When the command stackers are full or a Send diagnostic command has been received, the IDC returns a "Busy" status except that the Priority Reserve command is issued.

When the IDC receives the Priority Reserve command from any INIT, all commands previously received for the LUN including the queued and active commands are cleared, then the Priority Reserve command is executed.

The SCSI Reset condition or the Bus Device Reset message clears the command stackers.

The IDC retrieves the queued command other than a Send Diagnostic command from the command stackers sequentially by increasing the LUN number for each LUN and by decreasing the initiator's ID for all INITs after the currently active command and the commands linked from it, if any, have been completed.

However, if the IDC creates a sense data pending state concerning the currently active command due to the "Check Condition" or "Condition Met" status, any queued command from the INIT to which the status is returned and any queued command for the LUN which creates the sense data pending state are not executed until the sense data pending state is released by the INIT.

If the IDC has received the Send Diagnostic command, the IDC executes it after any commands that are in progress or that are queued have been completed the execution.

6.5 Unit Attention Condition

When the following condition occurs, the IDC preserves the unit attention condition.

- Not Ready to Ready

  When the device connected to the IDC becomes into Ready state from Not Ready state, or when the IDC is reset by the Reset condition or Bus Device Reset message, this unit attention condition occurs. The unit attention condition occurs on the individual device (LUN) in the former case, and on all devices in the Ready state in the latter case. This Unit Attention condition persists for each INIT until the condition which clears it, described later, is satisfied.

The IDC returns the "Check Condition" status upon reception of any I/O request except Inquiry, Request Sense, or Priority Reserve when the IDC preserves the unit attention condition for that INIT. The unit attention condition against that INIT is cleared by reporting the "Check Condition" status. At this time, the sense key of the sense data indicates a "Unit Attention".

When the IDC receives a Inquiry command during the unit attention condition, the Inquiry command is executed normally but the unit attention condition is not cleared.

When the IDC receives the Request Sense command during the unit attention condition, the IDC sends the sense data which indicates the unit attention condition. At this time, the unit attention condition against that INIT is cleared.

When the IDC receives the Priority Reserve command during the unit attention condition, IDC executes the command normally. At this time, the unit attention condition for the INIT which issues the command is cleared.

CHAPTER 7 STATUS BYTE AND SENSE DATA

7.1 Status Byte

A status byte notified from IDC to an INIT upon completion of each command indicates a result of the command execution.

Figure 7.1 shows the format of the status byte:

Bit 7	6	5	4	3	2	1	0
0	0	0	Status Byte Code				0

Bit 4321	
0000	Good status
0001	Check Condition status
0010	Condition Met/Good status
0100	Busy status
1000	Intermediate/Good status
1010	Intermediate/Condition Met/Good status
1100	Reservation Conflict status

Figure 7.1 Status byte

(1) Good status

This status indicates that a command has been completed successfully.

(2) Check Condition status

This status is reported either as a result of executing a command or when an I/O request issued from an INIT can not be executed. In either case, the device (LUN) that has reported this status enters a sense data pending state.

(a) When reported as a result of executing a command, this status indicates that the command has terminated abnormally except the case of (b) described below. The sense data then contains the details of the error.

(b) When the sense data indicates a "Recovered Error" sense key, the last command which resulted in "Check Condition" status has been completed successfully with some recovery action performed by the IDC.

(c) This status is reported upon reception of an I/O request in the following cases:

a. When the invalid LUN is specified. In this case, the sense key indicates an "Illegal Request".

b. When the INIT for which the IDC is preserving the unit attention condition issues an I/O request, other than Request Sense, Inquiry, or Priority Reserve. See Section 6.5 for details.

c. If a hardware error is detected while an I/O request is being accepted. The sense key then indicates a "Hardware Error".

(3) Condition Met status

This status is reported when the specified search condition has been satisfied by a Search Block command.

(4) Busy status

This status indicates that IDC or a specified device (LUN) is in Busy state and can not accept any new I/O request. This status is reported in any of the following cases:

(a) The command stacker to queue a command for the specified LUN and for the INIT that issues the I/O request is full, or the IDC has received a Send Diagnostic command. See Section 6.4 for details.

(b) IDC is preserving the sense data for a specified device for another INIT.

(c) IDC is preserving the sense data for any device other than the specified one for the INIT that issues the I/O request.

(d) IDC has completed the execution of a command which had accepted previously, and it has a status to be reported to an INIT.

(5) Intermediate status

This status indicates that a command which specifies command link has been completed successfully.

(6) Reservation Conflict status

This status indicates that a specified device is reserved by another INIT and is unusable until the reservation is released.

7.2 Sense Data

The sense data is created when the IDC reports a "Check Condition" status or a "Condition Met" status, or when the IDC forcedly creates the Bus Free phase due to a certain catastrophic SCSI bus related error.

The sense data implemented in IDC is an Extended Sense Format only. The INIT can retrieve the sense data by a Request Sense command.

7.2.1 Sense data pending state

The IDC goes to sense data pending state after any of the following conditions occur and continues until the reset requirements are satisfied:

- When IDC responds a "Check Condition" status to an INIT.
- When a "Condition Met" status is reported as a result of Search Block command. by a Search Block command.
- When the IDC forcedly creates the Bus Free phase due to a certain catastrophic SCSI bus related error.

The sense data pending state and the sense data are preserved for the INIT to which above-mentioned action has been taken, with respect to the device that has been specified at that time (*1).

The following provide the response to I/O request issued to the IDC which is in sense data pending state and sense data pending state reset requirements:

(1) I/O request from an INIT other than the INIT for which the sense data is preserved can be accepted. However, if an LUN in a sense data pending state is specified, a "Busy" status is returned except that a Priority Reserve command is issued. If other LUN is specified or a Priority Reserve command is issued, the I/O operation requested is executed normally.

(2) I/O request from the INIT for which the sense data is preserved is normally accepted only when the LUN in a sense data pending state is specified. If a command other than No Operation command is issued to the LUN, the sense data pending state is reset. If a Request Sense command is issued, the retained sense data is sent to the INIT. Execution of a command other than the No Operation command causes the retained sense data to be cleared. Similarly, when the INIT issues an Abort message, the sense data pending state is reset, and the sense data is lost.

If an I/O operation is requested from the INIT for which the sense data is preserved to an LUN other than the LUN which is in sense data pending state, a "Busy" status is returned.

If a "Check Condition" has been reported as a result of an invalid LUN being specified, the incorrectly-specified LUN is set to sense data pending state. Therefore, in this case, the INIT is required to reset the sense data pending state by specifying the same LUN that caused the "Check Condition".

A "Check Condition" status is reported if an error is detected during above-mentioned processings. IDC then generates new sense data and goes to another sense data pending state with respect to the LUN specified at that time.

(3) Other sense data pending state reset conditions

The sense data is lost and the sense data pending state is reset in the following cases, in addition to the cases described above.

- If a Reset condition is detected in SCSI
- If a Bus Device Reset message is received from any INIT

*1: If the SCSI ID of the INIT has not been identified, no SCSI ID of the INIT has been notified in the Selection phase, IDC goes to a special sense data pending state with no identified INIT. In this state, IDC regards a new I/O request with no notified SCSI ID of an INIT as an I/O request from the INIT for which the sense data is preserved.

7.2.2 Extended sense data

Figure 7.2 shows the format of extended sense data (Error class = '7', Error code = '0') implemented in the IDC. The extended sense data reports detailed information on an error, or the block address on successful execution of a Search Block command.

	Bit 7	6	5	4	3	2	1	0
BYTE 0	Valid	Error Class = 7			Error Code = 0			
1	Segment Number on Copy (= X'00')							
2	0	0	0	0	Sense Key (Ref. Table 7.1)			
3	ALT	CE	0	Logical Block Address (MSB)				
4	Logical Block Address							
5	Logical Block Address							
6	Logical Block Address (LSB)							
7	Additional Sense Length (= X'1C')							
8	X'00'							
9	X'00'							
10	X'00'							
11	X'00'							
12	Additional Sense Code (Ref. Table 7.2)							
13	X'00'							
14	X'00'							
15	X'00'							
16	X'00'							
17	X'00'							
18	0	0	IDC SCSI ID			LUN		
19	0	Sub-Error Class			Sub-Error Code (Ref. Tables 7.3 to 7.7)			
20	Cylinder Address (MSB)							
21	Cylinder Address (LSB)							
22	Head Address							
23	Block Address							
24	Detailed Information Byte- 0 (Ref. Table 7.8)							
25	Detailed Information Byte- 1 (Ref. Table 7.9)							
26	Detailed Information Byte- 2 (Ref. Fig. 7.3)							
27	Detailed Information Byte- 3 (Ref. Fig. 7.3)							
28	Detailed Information Byte- 4 (Ref. Fig. 7.3)							
29	Detailed Information Byte- 5 (Ref. Fig. 7.3)							
30	Detailed Information Byte- 6 (Ref. Fig. 7.3)							
31	Detailed Information Byte- 7 (Ref. Fig. 7.3)							
32	Detailed Information Byte- 8 (Ref. Fig. 7.3)							
33	Detailed Information Byte- 9 (Ref. Fig. 7.3)							
34	Detailed Information Byte-10 (Ref. Fig. 7.3)							
35	X'00' (Reserved)							

Figure 7.2 Extended sense data

(1) Valid: Byte 0, bit 7

This bit indicates that the bytes 3 to 6 and bytes 20 to 23 contain valid information.

(2) Sense Key: Byte 2, bits 3 to 0

Sense key is 4-bit code indicating the cause which creates the sense data. Further particulars are indicated at the additional sense code field of byte 12 and the sub-error class/sub-error code field of byte 19. Table 7.1 lists the sense keys and their meanings.

(3) ALT, CE, Logical Block Address: Bytes 3 to 6

These are only valid when the valid bit (Byte 0, bit 7) is set to '1', and indicate the following information:

(a) These bytes indicate the identification flag of data space (user space/CE space, primary area/alternate area) and the logical block address of the block (*1) which is associated with the status indicated by the sense key except for item (b).

(b) When a Copy command has terminated with "Check Condition" status, these bytes indicate the difference between the source block count specified in the segment descriptor and the normally copied block count.

(4) Additional Sense Length: Byte 7

This byte indicates the length of sense data from byte 8 onward. This length in IDC is always X'1C' (28 bytes).

(5) Additional Sense Code: Byte 12

This byte indicates more detailed reason concerning the created sense key. Table 7.2 lists the difinition of the additional sense code.

(6) IDC SCSI ID: Byte 18, bits 5 to 3

These bits indicate the SCSI ID of the IDC.

(7) LUN: Byte 18, bits 2 to 0

These bits indicate a Logical unit number of the drive fot which the sense data is created.

(8) Sub-Error Class: Byte 19, bits 6 to 4

These bits classify errors into the following types:

- Sub-Error class 0: Disk drive error or no error condition
- Sub-Error class 1: Error during command processing
- Sub-Error class 2: System error

- Sub-Error class 3: SCSI error/miscellaneous error
- Sub-Error class 7: IDC hardware error

(9) Sub-Error code: Byte 19, bits 3 to 0

These bits indicate the type of a detected error. Table 7.3 to 7.7 list sub-error codes for the respective sub-error classes.

(10) Cylinder, Head, Block Address: Byte 20 to 23

These bytes indicate the address of a data block which is associated with the status indicated by the sense key in cylinder/head/block address (*1). This data is only valid when the valid bit (Byte 0, bit 7) is set to '1'.

When sub-error class = '7', these bytes indicate a part of the detailed information, as shown in Figure 7.3.

(11) Detailed Information: Bytes 24 to 34

As shown in Figure 7.3, these bytes indicate detailed information for errors corresponding to sub-error classes and sub-error codes.

*1: Indications of the data block address on bytes 3 to 6 and bytes 20 to 23 are as follows:

(a) When the ALT bit is '0', these indicate the address of the block which locates on the primary area, and both fields indicate the address of the same data block.

(b) When a processing of the alternate area has been specified through a Set File Mask command, both fields indicate the address of the same alternate block. In this case, the ALT bit indicates '1'.

(c) When a Copy command has terminated abnormally, bytes 20 to 23 indicate the address of the data block on which the error has occurred actually.

(d) Except the above cases, when the erroneous condition has been detected on the alternate block if the defect/alternate block processing was executed during processing of the primary area, the indications of the data block address are as listed below:

ALT	CE	Bytes 3 to 6	Bytes 20 to 23
1	0/1	The logical block address of the primary block (defective block)	The cylinder, head, and block address of the alternate block

Table 7.1 Sense key (1/2)

Sense Key	Name	Description
0	No Sense	No particular sense key exists for a specified LUN.
1	Recovered Error	This sense key indicates that the last command completed successfully with some recovery action performed by the IDC. This sense key is reported only when the PER (Post Error) bit of the Mode Select parameters has been set to one.
2	Not Ready	A specified device (LUN) cannot be accessed.
3	Medium Error	An unrecoverable error has been detected because of a medium defect or an error in the recorded data.
4	Hardware Error	A unrecoverable hardware error was detected while the TARG executed a command or self-diagnosis.
5	Illegal Request	An illegal value was detected in a parameter transferred according to the indication of a command or in a CDB, or the specified LUN is invalid. If the IDC detects an invalid parameter in the CDB, then it terminates the command without any altering the disk medium. However, if an invalid parameter is detected in the additional parameters supplied by Data Out phase, then the IDC may or may not have already altered the medium.
6	Unit Attention	One of the following conditions has been detected. • IDC has been reset by a Reset condition or a Bus Device Reset message. • A not ready device has become ready. For details, see Section 6.5.

Table 7.1 Sense key (2/2)

Sense Key	Name	Description
7	Data Protect	An illegal operation (read or write) has been attempted for an read-inhibited or write-inhibited area. The command is not executed.
8	Blank Check	Unused.
9	(Reserved)	
A	Copy Aborted	Unused.
B	Aborted Command	The TARG has terminated a command abnormally. The INIT can reissue the command for recovery.
C	Equal	A Search command has succeeded in search under the "equal" condition. Bytes 3 to 6 of the sense data then indicate the address of the successfully searched block.
D	Volume Overflow	Unused
E	Miscompare	Data sent from an INIT by a Verify command in the data compare mode (byte check) has not matched the data read from the medium. Or, the data buffer has been corrupted before execution of a Read Buffer command after a Write Buffer command.
F	(Reserved)	

Table 7.2 Additional sense code (1/2)

Additional Sense Code	Definition	Related Sense Key
00	No Additional Sense Code.	All Keys
01	(Reserved)	
02	No Seek Complete	Hardware error
03	Drive Fault	Hardware Error
04	Drive Not Ready	Not Ready
05	Drive Not Selected	Not Ready
06	(Reserved)	
07	Multiple Drives Selected	Hardware Error
08 to 0F	(Reserved)	
10	Unrecovered Read Error of ID Field	Medium Error
11	Unrecovered Read Error of Data Field	Medium Error
12	No Sync Byte Found in ID Field	Medium Error
13	No Sync Byte Found in Data Field	Medium Error
14	No Record Found or Bad Block Found	Medium Error
15	Seek Error	Hardware Error Medium Error Recovered Error
16	(Reserved)	
17	Recovered Read Data with Re-read Retries (not with ECC Correction)	Recovered Error
18	Recovered Read Data with ECC Correction (not with Re-read)	Recovered Error
19	Defect List Error	Medium Error Recovered Error
1A	(Reserved)	
1B	Synchronous Transfer Error	Hardware Error
1C	Primary Defect List not Found	Medium Error
1D	Compare Error	Miscompare
1E	Recovered ID with ECC Correction	Recovered Error
1F	(Reserved)	

Table 7.2 Additional sense code (2/2)

Additional Sense Code	Definition	Related Sense Key
20	Invalid Command Operation Code	Illegal Request
21	Illegal Logical Block Address	Illegal Request
22 and 23	(Reserved)	
24	Illegal Field in CDB	Illegal Request
25	Invalid LUN	Illegal Request
26	Invalid Field in Parameter List	Illegal Request
27	Write Protected	Illegal Request
28	(Reserved)	
29	Power On, Reset condition or Bus Device Reset Occurred	Unit Attention
2A to 2F	(Reserved)	
30	(Reserved)	
31	Format Failed	Medium Error Hardware Error
32	No Defect Spare Location Available	Medium Error
33 to 3F	(Reserved)	
40	RAM Failure	Hardware Error
41	Data Path Diagnostic Failure	Hardware Error
42	Power On Diagnostic Failure	Hardware Error
43	Message Reject Error	Aborted Command
44	Internal Controller Error	Hardware Error
45	Select/Reselect Failed	Aborted Command Recovered Error
46	(Reserved)	
47	SCSI Parity Error	Aborted Command Recovered Error
48	Initiator Detected Error	Aborted Command Recovered Error
49	Inappropriate/Illegal Message	Illegal Request Aborted Command
4A to 4F	(Reserved)	
50 to 5F	(Reserved)	
60 to 6F	(Reserved)	
70 to 7F	(Reserved)	
80 to FF	(Reserved)	

Table 7.3 Sub-error codes (device errors/no error condition)

Sub E-Class	Sub E-Code	Name	Description	Sense Key
0	0	No Sense	A Request Sense command was issued while no sense data was preserved or the sense data includes no error information.	0, 6, C
	1			
	2	No Seek Complete	No Seek Complete signal was reported from the drive.	4
	3	Fault	A Fault signal was reported from the drive.	4
	4	Device Not Ready	The specified device was not ready.	2
	5	Device Not Selected	The specified device could not be selected.	2
	6	Seek Error	A Seek Error signal was reported from the drive.	4
	7	Multiple Drives Selected	Drives were selected doubly.	4
	8			
	9			
	A			
	B	Invalid Device Type	An undefined device type code was detected.	4
	C			
	D	Copy Device Busy	The device specified in parameter list of a Copy command was in "Busy" state.	B
	E			
	F			

Table 7.4 Sub-error codes (errors during command processing)

Sub E-Class	Sub E-Code	Name	Description	Sense Key
1	0	ID Field Uncorrectable	An uncorrectable data check occurred in the ID field.	1, 3
	1	Data Field Uncorrectable	An uncorrectable data check occurred in the data field.	1, 3
	2	ID Field No SYNC Found	No sync byte could be detected in the ID field.	1, 3
	3	Data Field No SYNC Found	No sync byte could be detected in the data field.	1, 3
	4			
	5	Seek Error	The cylinder or head number in the ID field differed from the expected number.	1, 3, 4
	6	ID Field Correctable	A correctable data check occurred in the ID field.	1, 3
	7	Write Protected	A file protect status was detected on the drive during a write operation.	7
	8	Data Field Correctable	A correctable data check occurred in the data field.	1, 3
	9	No Record Found or Bad Block Found	The value of the flag in the ID field was illegal.	3
	A			
	B	Device Information Set-up Failed	The device Information recorded in system space could not be read.	4
	C	Defect List Error	The defect information in P or G list was invalid.	3
	D	Sector Overrun	A sector overrun occurred during reconnection with an INIT.	1, B
	E	Data Overrun	A data overrun occurred during transferring data.	1, B
	F	Hardware Error	A hardware error was detected in IDC.	4

Table 7.5 Sub-error codes (system errors) (1/2)

Sub E-Class	Sub E-Code	Name	Description	Sense Key
2	0	Invalid Command	The operation code in the CDB was illegal.	5
	1	Invalid Block Address	The block address in the CDB was illegal.	5
	2	Invalid Parameter	A parameter in the CDB was invalid.	5
	3			
	4	Invalid Sequence	The command link requirement was violated.	5, 7
	5	End of Volume	A request to process was issued beyond the last block of the space allowed to access.	5
	6	Invalid Protect Flag	The write inhibit flag in the Set File Mask command is inconsistent with the write inhibit flag in the Set Limits command.	5
	7	Data Protected	Access was attempted beyond the area specified in the Set Limits command. An operation inhibited by the Set File Mask or Set Limits command was detected.	7
	8	Verify Not Equal	Unmatched data was detected during Verify (Byte check) command.	E
	9	Invalid LUN	An invalid LUN (4 to 7) was specified.	5
	A	Invalid Parameter List	A value in the parameter list received from an INIT (Data Out phase) was invalid.	5
	B	Disabled Group-6 Command	No group-6 command was permitted through a Set File Mask command.	5

Table 7.5 Sub-error codes (system errors) (2/2)

Sub E-Class	Sub E-Code	Name	Description	Sense Key
2	C	No Defect Spare Available	No unused alternate block was found when assigning an alternate blocks.	3
	D	No G List Space Available	No entry in G list was available to add the defect information.	3
	E	Invalid Access Area	An unaccessible area of data space was specified in the Format ID command.	5
	F	INIT's ID Undefined	A Reserve/Release/Priority Reserve command was issued even though the SCSI ID of an INIT has not been notified in the Selection phase.	5

Table 7.6 Sub-error codes (SCSI errors/miscellaneous errors)

Sub E-Class	Sub E-Code	Name	Description	Sense Key
3	0	SCSI Bus Parity Error	A parity error occurred on the SCSI data bus.	1, B
	1			
	2	Message Parity Error	The IDC received a Message Parity Error message from the INIT (Retry Out)	
	3	Rejected Message	The IDC received a Message Reject message from the INIT.	B
	4			
	5	Select/Reselect Timeout	A timeout was detected during the Reselection phase (Retry Out).	1, B
	6			
	7			
	8	INIT Detected Error	The IDC received an Initiator Detected Error message from the INIT (Retry Out).	1, B
	9	Invalid Message	An inappropriate or illegal message was received.	5, B
	A			
	B			
	C	Data Buffer Corrupted	The data buffer has been corrupted before Read Buffer command	E
	D			
	E	SCSI Information Transfer Timeout	A timeout was detected with respect to Information Transfer phase on SCSI.	B
	F	Microprogram Detected Error	The IDC microprogram detected any miscellaneous error.	4

Table 7.7 Sub-error codes (IDC hardware errors)

Sub E-Class	Sub E-Code	Name	Description	Sense Key
7	0			
	1			
	2			
	3			
	4			
	5			
	6			
	7			
	8 (*1)	Diagnostic Failure	An error was detected as a result of executing a self-diagnostic program.	4, B
	9			
	A			
	B			
	C			
	D			
	E			
	F (*2)	IDC Hardware Control Error	A parity error was detected on the IDC internal bus.	4, B

*1: If this error condition was detected and the Additional Sense Code indicates X'40' (RAM Failure), X'41' (Data Path Diagnostic Failure), or X'42' (Power On Diagnostic Failure), the SCSI Reset condition is reguired to clear the error condition.

*2: When this error was detected, all of the 4-bit LED indicators on the IDC PCA light until the sense data is read out by an INIT.

7.2.3 Sense data detailed information

Byte 24 through byte 34 of the extended sense data indicate the detailed information and hardware status for the detected error. Figure 7.3 shows the structure of detailed information corresponding to each sub-error class and sub-error code.

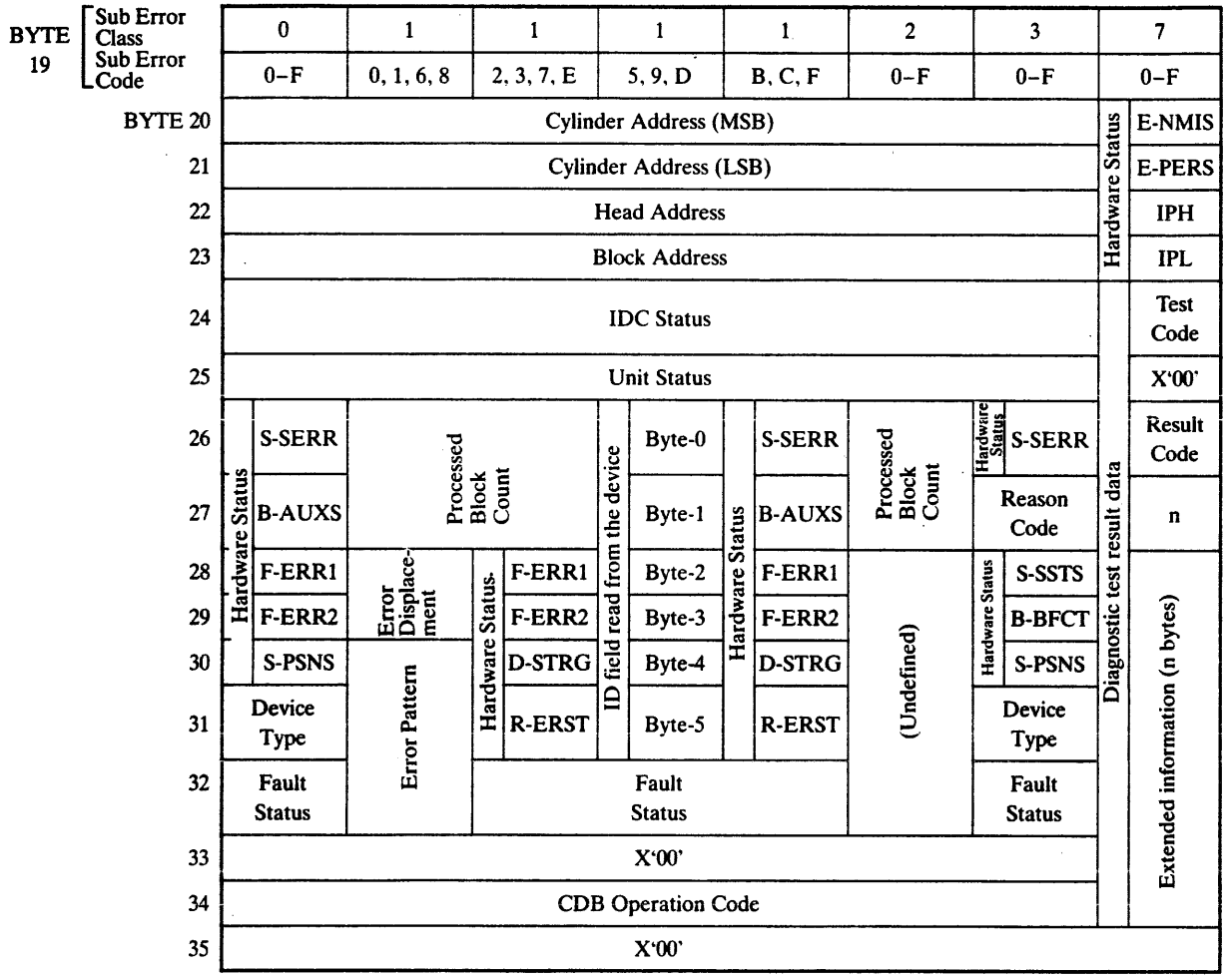


Figure 7.3 Sense data detailed information structure

(1) IDC Status

This byte indicates the status of controller itself as shown in Table 7.8 when it detects the error.

Table 7.8 IDC Status in sense data

Bit 7	6	5	4	3	2	1	0
Device Selected	0	Offset Active	0	11: — 10: Verify Op 01: Write Op 00: Another Op		INIT	Another Error In Retry

- Device Selected: Bit 7 shows that the IDC has actually selected the device on SMD interface.
- Offset Active: Bit 5 indicates that the IDC has been executing read operation with instructing the head offset to the device.
- Operation Type: Bits 3 and 2 indicate the type of operation which has been executed in the IDC.
- INIT: Bit 1 indicates that the IDC has operated as an INIT on SCSI. This bit is always '0'.
- Another Error In Retry: Bit 0 indicates that a different type of error was detected while the IDC attempted a retry procedure for the original error condition.

(2) Unit Status

This byte indicates the unit status byte which was obtained from the SMD interface as shown in Table 7.9. This information is valid only when the IDC Status bit 7 (Device Selected) is '1'. See Appendix A which provides a brief explanation. For details, see the Manual for the attached device.

Table 7.9 Unit Status in sense data

Bit 7	6	5	4	3	2	1	0
Sector	Index	0	File Protect	Fault	Seek Error	On Cylinder	Unit Ready

(3) Device Type

This byte indicates the device type code as shown in Table 7.10, and is valid only when the IDC Status bit 7 (Device Selected) is '1'.

Table 7.10 Device Type code in sense data

Device	Bit 7	6	5	4	3	2	1	0	Code (HEX)
M2333KS	0	0	1	0	1	1	1	0	2E
M2331KS	0	0	1	0	1	1	0	0	2C

(4) Fault Status

This byte indicates the fault status byte which was obtained from the SMD interface as shown in Table 7.11. This information is valid only when both the IDC Status bit 7 (Device Selected) and the Unit status bit 2 (Seek Error) or bit 3 (Fault) are '1'. See Appendix A which provides a brief explanation. For details, see the Manual for the attached device.

Table 7.11 Fault Status in sense data

Bit 7	6	5	4	3	2	1	0
DC Motor Fault	VCM Heat	Seek Error 4	Seek Error 2	Seek Error 1	Fault 4	Fault 2	Fault 1

(5) Processed Block Count

This information indicates the number of actually processed data blocks on the specified device. For read operation, this value is equal to the number of blocks that have already been transferred to the INIT. For write operation, this value is equal to the number of blocks that have already been written onto the disk medium. This value is not ensured for a Copy command, and is valid for the following types of error:

Sub-Error Class	Sub-Error Code	
1	0, 1, 6, 8	Data Check on ID or Data Field
1	2,3	No Sync Byte Found on ID or Data Field
1	E	Data Overrun
2	8	Verify Not Egual
2	C	No Defect Spare Available
2	D	No G List Space Available

(6) CDB Operation Code

This byte indicates byte-0 of the CDB, Operation Code, which was executed when the sense data was created.

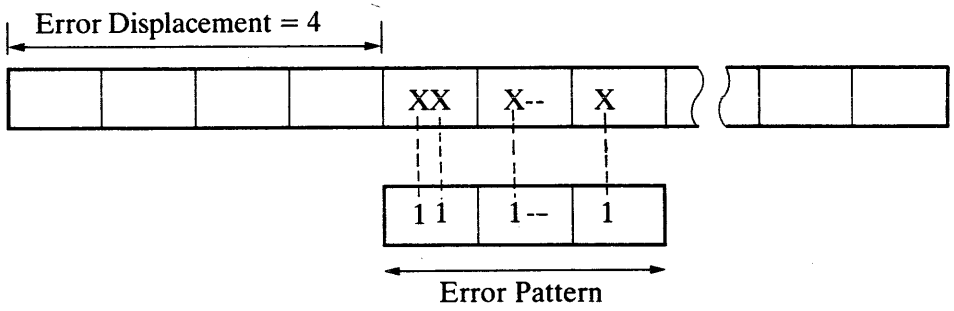
(7) Error Displacement and Error Pattern

These information are valid only for the following types of error:

Sub-Error Class	Sub-Error Code	
1	6	Correctable Data Check on ID Field
1	8	Correctable Data Check on Data Field

The error displacement indicates the byte location containing the correctable error bits in byte distance from the leading byte of the erroneous data block. To point to the leading byte, the error displacement is '0'. The error pattern can be used to find the erroneous bit(s) for three contiguous bytes from and including the byte location indicated by the error displacement. The erroneous bit position is indicated as '1' in the error pattern. See the following example.

Example: Where an error occurs at byte 5



(8) ID Field read from the device

This information indicates the contents of the ID field which has been actually read from the device when the following types of error were detected:

Sub-Error Class	Sub-Error Code	
1	5	Seek Error detected by checking the ID field
1	9	No Record Found or Bad Block Found
1	D	Sector Overrun

(9) Hardware Status

Hardware Status bytes dedicated for some types of error indicate the detailed status or error flags. See Subsection 7.2.4 for details.

(10) Reason Code

This byte indicates the detailed reason for the following errors:

Sub-Error Class	Sub-Error Code	
3	E	SCSI Information Transfer Timeout
3	F	Microprogram Detected Error

See Subsection 7.2.5 for details.

(11) Diagnostic test result data

These bytes are only valid for the following error and indicate a diagnostic routine test code which detects the error and its test result data. The test result data takes the same format as the result data which might be sent by a Receive Diagnostic Results command. For details, see Chapter 9.

Sub-Error Class	Sub-Error Code	
7	8	Diagnostic Failure

7.2.4 Hardware status bytes

The hardware status bytes in the sense data (see Figure 7.3) indicate the detailed error status or error flags. This Subsection describes the meaning of each bit or field of the hardware status bytes and FRU (Field Replaceable Unit) can be considered as a failure which causes the error.

(1) S-SERR

This byte indicates the error flags which are related to the SCSI hardware as shown in Table 7.12.

Table 7.12 S-SERR hardware status

Bit	Meaning	FRU
7, 6	Bit 7 6 0 1: A parity error was detected in the data to be sent to the SCSI bus.	IDC
	1 1: A parity error was detected in the data received from the SCSI bus.	INIT or IDC
5, 4	always '0'	—
3	TC Parity Error: A parity error occurred in the transfer byte counter (TC) within the IDC	IDC
2	Phase Error: Don't care. (This bit is always '0' when the IDC operates as TARG.)	—
1	Short Period: A cycle time of successive ACK signals received from the SCSI was shorter than the limitation of the IDC hardware.	INIT
0	Offset Error: The number of ACK signals received exceeded the REQ signals which had been sent, or the IDC sent REQ signals which exceed the value of REQ/ACK offset.	INIT or IDC

(2) B-AUXS

The error conditions and hardware status indicated in this byte is related to the SERDES and ECC circuits within the IDC as shown in Table 7.15.

Table 7.13 B-AUXS hardware status

Bit	Meaning	FRU
7	Condition Met: Don't care (This bit indicates the completion status of Search operation.)	—
6, 5	always '0'	—
4	Invalid Path: An invalid data path within the IDC was detected. Note that '1' of this bit is not an error status if 'SB Not Found (F-ERR1, bit 6)' was set to '1'.	IDC
3	ADR-A Parity Error: A parity error was detected in the address counter for the buffer #A.	IDC
2	ADR-B Parity Error: A parity error was detected in the address counter for the buffer #B.	IDC
1, 0	always '0'	—

(3) F-ERR1 and F-ERR2

These bytes indicate the hardware and error status with regard to sector format control as shown in Table 7.14.

Table 7.14 F-ERR1/F-ERR2 hardware status

Byte	Bit	Meaning	FRU
F-ERR1	7	ECC≠0: Correctable or uncorrectable read error was detected.	—
	6	SB Not Found: The Sync Byte pattern was not detected in ID or Data field during read operation.	—
	5	ID Mismatch: Unexpected ID field was encountered.	—
	4	ECC Uncorrectable: Uncorrectable data check was detected as a result of ECC analysis.	—
	3	Data Area: '0' indicates that the IDC was processing the ID field, or not processing any sector. '1' indicates that the IDC began the process of the Data field.	—
	2	Halt: The sector format control has been terminated due to data buffer condition. See B-AUXS byte.	—
	1	Sector Error: Unexpected sector pulse was detected.	Drive or IDC
	0	always '0'	—
F-ERR2	7	CMD Parity Error : A parity error was detected in the IDC internal register.	IDC
	6	HDR Parity Error :	
	5	BYCH Parity Error :	
	4	BYCL Parity Error :	
	3	SEQCNT Parity Error:	
	2	SDC Error: The sector format control has been terminated due to error conditions detected in the SERDES & ECC circuits. See D-STRG byte.	—
	1	R/W Error: A Fault signal from the drive was detected during read/write operation, or error was detected on a Write Gate signal.	Drive or IDC
	0	always '0'	—

(4) D-STRG

The error conditions and hardware status indicated in this byte is related to the SERDES and ECC circuits within the IDC as shown in Table 7.15.

Table 7.15 D-STRG hardware status

Bit	Meaning	FRU
7	Data Overrun: A data overrun was detected during read/write operation.	—
6	DDB Parity Error: A parity error was detected in the IDC internal data bus.	IDC
5	SERDES Parity Error: A parity error was detected in the SERDES (Serialize/Deserialize) circuits.	IDC or Drive
4	BITCT Parity Error: A parity error was detected in the bit clock counter in the IDC.	IDC or Drive
3	ECC Parity Error: A parity error was detected in the ECC register.	IDC
2	DTEQ : Don't care (These bits are not error status.)	—
1	HIGH :	
0	Compare skip :	

(5) R-ERST

This byte indicates the error status which is related to RPS (Rotational Position Sensing) circuits in the IDC as shown in Table 7.16.

Table 7.16 R-ERST hardware status

Bit	Meaning	FRU
7	Sector Counter #3 Parity Error :	IDC or Drive
6	Sector Counter #2 Parity Error :	
5	Sector Counter #1 Parity Error :	
4	Sector Counter #0 Parity Error :	
	A parity error was detected in the sector counter which is corresponding to the drive #3 through #0 attached to the IDC.	
3	Device Error #3 :	IDC or Drive
2	Device Error #2 :	
1	Device Error #1 :	
0	Device Error #0 :	
	An index pulse was detected before the sector counter reaches to the maximum value, or an index pulse was not detected after the maximum value. Each bit position corresponds to the drive #3 through #0 attached to the IDC.	

Note: The value of bit position corresponding to a drive number which is not actually attached or powered-off is unpredictable.

(6) S-PSNS

This byte indicates the status of SCSI control signals when the sense data was created as shown on Table 7.17.

Table 7.17 S-PSNS hardware status

Bit	Meaning	
7	REQ :	Each bit corresponds to the SCSI interface signal and indicates the state of the signal: '1': True '0': False
6	ACK :	
5	ATN :	
4	SEL :	
3	BSY :	
2	MSG :	
1	C/D :	
0	I/O :	

(7) S-SSTS

This byte indicates the status of IDC hardware which is related to the SCSI control as shown in Table 7.18.

Table 7.18 S-SSTS hardware status

Bit	Meaning
7	INIT: The IDC was operating on the SCSI as an INIT.
6	TARG: The IDC was operating on the SCSI as a TARG.
5	SPC Busy: The IDC was executing an Information Transfer phase, Selection phase, or Reselection phase.
4	Transfer in Progress: The IDC was executing an Information Transfer phase.
3	SCSI RST: '1' indicates that the RST signal on the SCSI is True state, '0' indicates that the RST signal is False state.
2	TC=0: Transfer Byte Counter which controls transfer length for Data In/ Data Out phase is zero.
1	DREG Full: The data register (8-byte FIFO) for the SCSI is full.
0	DREG Empty: The data register (8-byte FIFO) for the SCSI is empty.

(8) B-BFCT

This byte indicates the status of IDC hardware which is related to a data buffer as shown in Table 7.19.

Table 7.19 B−BFCT hardware status

Bit	Meaning
7	Data Valid #A : The Data buffer #A(bit 7) or #B (bit 6) has the valid data.
6	Data Valid #B :
5	Buffer Empty #A: The data buffer #A (bit 5) or #B (bit 4) has no valid data.
4	Buffer Empty #B:
3	H-Port DREQ: Transfer request to the data buffer from SCSI port is active.
2	D-Port DRDY: Data tranfer between the data buffer and SERDES for drive interface is available.
1	always '0'
0	Scan Window: Don't care

(9) E-NMIS and E-PERS

These bytes indicate the Non-maskable Interruption status to the MPU whithin the IDC. The Non-maskable Interruption occurs when a parity error was detected on the IDC internal MPU bus or when a timeout due to the hardware timer occurred.

Table 7.20 E-NMIS/E-PERS hardware status

Byte	Bit	Meaning	FRU
E-NMIS	7	Test Mode: Don't care	—
	6, 5	always '0'	—
	4	Timer Enable: The hardware timer was enabled.	—
	3	Timeout 0: Interruption from the hardware timer #0	—
	2	Timeout 1: Interruption from the hardware timer #1	—
	1	D-Bus High Parity Error: A parity error was detected in high-order byte of the MPU bus.	IDC
	0	D-Bus Low Parity Error: A parity error was detected in low-order byte of the MPU bus.	IDC
E-PERS	7	$\overline{\text{TM/EX}}$: 1 0 0 0 0 0 0 0 0	—
	6	$\overline{\text{ROM}}$: 1 1 1 1 1 1 1 1 0	
	5	$\overline{\text{RAM}}$: 1 1 1 1 1 1 1 0 1	
	4	$\overline{\text{DBM}}$: 1 0 1 1 1 1 0 1 1	
	3	$\overline{\text{SPC}}$: 1 0 1 1 1 0 1 1 1	
	2	$\overline{\text{FMT}}$: 1 1 1 1 0 1 1 1 1	
	1	$\overline{\text{SDC}}$: 1 1 1 0 1 1 1 1 1	
	0	$\overline{\text{RPS}}$: 1 1 0 1 1 1 1 1 1	
		↳EPROM ↳RAM ↳DBM ↳SPC ↳FMT ↳SDC ↳RPS ↳Data Buffer #A or #B ↳Other external registers } See Figure 2.3	
		This byte indicates which part of the IDC hardware was accessed by MPU when the Non-maskable Interruption occurred. This information is useful when the parity error was detected on the MPU bus.	

(10) IPH and IPL

This information is valid only when the sub-error class/code is 7/F, and indicates the address of microinstruction on which the Non-maskable Interruption occurred.

7.2.5 Reason code

The reason code field in the sense data (see Figure 7.3) is valid only when the sub-error class/code is 3/E or 3/F, and indicates the detailed reason for the error.

(1) Sub-error class/code = 3/E : SCSI Information Transfer Timeout

Figure 7.4 shows structure of the reason code that indicates which SCSI bus phase has been executed when the timeout occurred.

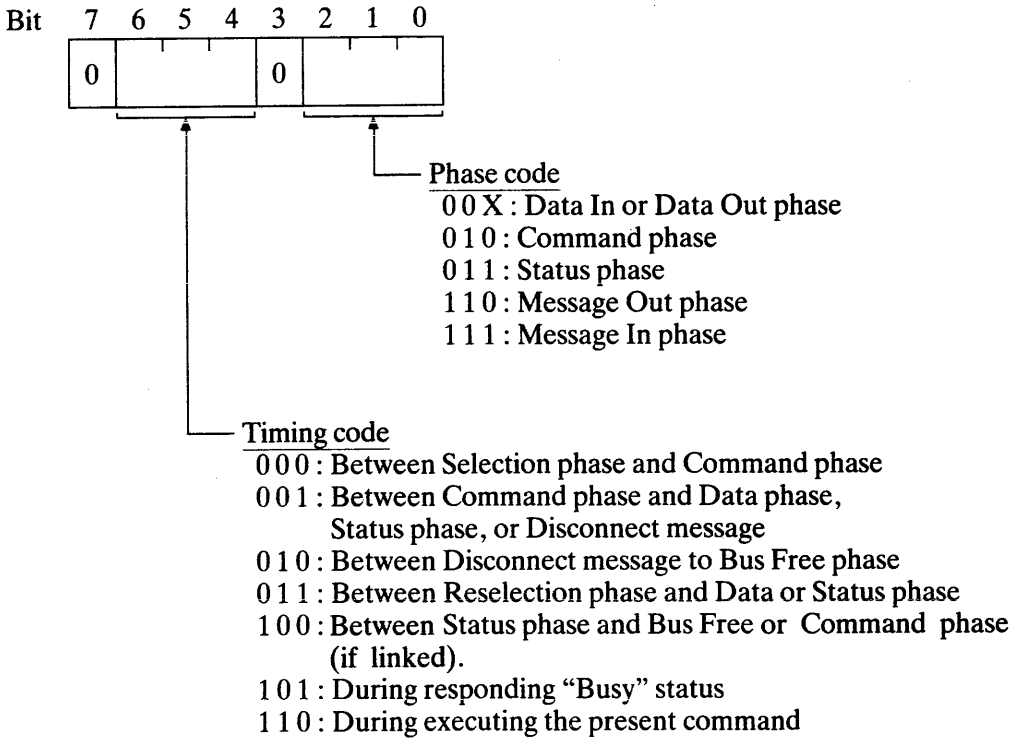


Figure 7.4 Reason code for SCSI Timout error

(2) Sub-error class/code = 3/F : Microprogram Detected Error

The sub-error class/code = 3/F in the sense data indicates that the IDC microprogram detected an unreasonable condition even though the hardware did not create an error condition explicity. Table 7.21 indicates the reason code for this type of error. Generally, the cause of this type error is considered as malfunction of the IDC or the drive although the setting switch on the device should the reconfirmed.

Table 7.21 Reason code for Microprogram Detected error

Reason code	Description
0 X	An unreasonable hardware status or microprogram processing condition was detected.
1 X | 9 X	(Reserved)
A X | F X	The microprogram detected a timeout at the operation check of the hardware: □ □ 8 : FMT–command end or data area 9 : FMT–index or sector latch A : RPS–sector counter B : RPS–attention for seek complete or sector position sensing C : RPS–sector location detection D : SPC–SCSI transfer E : DBM–data buffer empty A : Device Interruption B : Device Selection C : Sense Generation D : Diagnosis E : Command Processing

CHAPTER 8 ERROR RECOVERY

8.1 SCSI Error Conditions and Retry

This section describes the various SCSI bus related errors which may occur during command execution and the actions taken by the IDC in response to the errors.

Under some severe error conditions, the IDC may change the SCSI bus phase to Bus Free without Disconnect or Command Complete message sent to the INIT. The IDC then clears all information regarding the currently executing command and does not attempt to reconnect to the INIT for the command. The INIT shall consider this as a catastrophic error. In this case, the IDC may or may not create the sense data concerning the error. The INIT shall issues a Request sense command attempting to recover further information concerning the catastrophic error.

8.1.1 Error conditions and retry procedure

(1) Message Out phase parity error

When the IDC detects a parity error during the Message Out phase, it retries the Message Out phase using the following sequence:

- Continue the REQ/ACK handshakes until the INIT negates ATN signal.
- Notify the INIT to resend all previous Message Out message bytes within the current phase, by not changing the phase and by sending REQ signal.

Up to two retries are performed. The INIT shall resend all previous message bytes.

When the error recovery is not succesful, the IDC terminates the present command with a "Check Condition" status and with the Sense Key/Additional Sense Code of "Aborted Command/SCSI Parity Error" if the LUN has already been identified. In this case, the IDC may ignore any Attention condition until it goes to the Bus Free phase. This error will not prevent the INIT from retrying the command.

When the error recovery is not successful and the LUN has not been identified through an Identify message or the LUN field in the CDB, the IDC immediately goes to the Bus Free phase with no sense information.

(2) Command phase parity error

When the IDC detects a parity error during the Command phase, it retries the Command phase using the following sequence:

- Change the bus phase to Message In when the parity error is detected or after all bytes of the CDB are transferred, then send a Restore Pointers message.
- Attempt to receive all bytes of the CDB over again.

Up to two retries are performed. The INIT shall resend all bytes of the CDB.

When the error recovery is not successful, The IDC terminates the present command with a "Check Condition" status and with the Sense Key/Additional Sense Code of "Aborted Command/SCSI Parity Error" if the LUN has already been identified from an Identify message. In this case, the IDC may ignore any Attention condition until it goes to the Bus Free phase. This error will not prevent the INIT from retrying the command.

When the error recovery is not successful and the LUN has not been identified, the IDC immediately goes to the Bus Free phase with no sense information.

(3) Data Out phase parity error

When the IDC detects a parity error during the Data Out phase, it retries the Data Out phase using the following sequence:

- Change the bus phase to Message In, then send a Restore Pointers message.
- Change the bus phase to Data Out, then attempt to receive the data over again.

Up to two retries are performed.

When the data is not received successfully, the IDC terminates the executing command with a "Check Condition" status and with the Sense Key/Additional Sense Code of "Aborted Command/SCSI Parity Error". In this case, the IDC may ignore any Attention condition until it goes to the Bus Free phase. This error does not prevent the INIT from retrying the command.

(4) Initiator Detected Error message

If the IDC receives an Initiator Detected Error message, it retries the bus phase just prior to the receipt of the message using the following sequence:

- Change the phase to Message In, then send a Restore Pointers message.
- Return to the phase just prior to the receipt of the Initiator Detected Error message and retry the operation.

If the retry is impossible or the IDC receives the Initiator Detected Error message during this retry operation, the IDC terminates the executing command with a "Check Condition" status and with the Sense Key/Additional Sense Code of "Aborted Command/Initiator Detected Error". In this case, the IDC may ignore any Attention condition until it goes to the Bus Free phase. This error does not prevent the INIT from retrying the command.

However, if the retry is attempted for the Status phase and the operation cannot be completed successfully, the IDC immediately goes to the Bus Free phase with no sense information.

(5) Rejected messages

When the IDC receives a Message Reject message from the INIT, it takes the following action based on which message was rejected.

(a) Command Complete

The IDC goes to Bus Free phase immediately, and does not consider this as an error.

(b) Disconnect

The IDC does not disconnect the SCSI bus and continues the currently executing command. However, the IDC may attempt to disconnect at later time if the INIT has indicated previously in the Identify message that it supports the disconnect/ reconnect option.

(c) Identify

When this message sent for reconnection is rejected, the IDC immediately goes to the Bus Free phase and aborts the command which has requested the reconnection. No further reconnection for the command is attempted, and the IDC does not create the Status or Message In phase with Command Complete message for the aborted command. Then, the IDC creates the sense information with Sense Key/Additional Sense Code of "Aborted Command/Message Reject Error" (*1).

(d) Linked Command Complete (with Flag)

The IDC immediately goes to the Bus Free phase without requesting the next linked command. The command link is broken. Then, the IDC creates the sense information for the INIT with Sense Key/Additional Sense Code of "Aborted Command/Message Reject Error" (*1).

(e) Message Reject

The IDC immediately terminates the currently executing command with "Check Condition" status and with the Sense Key/Additional Sense Code of "Aborted Command/Message Reject Error" (*1).

(f) Restore Pointers

The Restore Pointers message is used during the error recovery procedures. So, the IDC aborts the recovery attempt if this message was rejected, then terminates the command with "Check Condition" status based on the original error condition (*1).

(g) Save Data Pointer

The IDC may send the Save Data Pointer message prior to send the Disconnect message. The IDC continues the currently executing command without disconnection if this message was rejected.

(h) Synchronous Data Transfer Request

The IDC assumes that the INIT does not support the Synchronous Transfer mode, and continues the command execution using the Asynchronous Transfer mode.

*1: When the IDC terminates the present operation due to the rejected message, it may ignore any Attention condition until it creates the Bus Free phase.

(6) Message Parity Error message

When the IDC receives a Message Parity Error message from the INIT, it resends the original message. If the Message Parity Error message is replied again during the resending, the IDC immediately goes to the Bus Free phase and aborts the present command. No status or Command Complete message is returned for the command. The IDC creates the sense information with Sense Key/Additional Sense Code of "Aborted Command/SCSI Parity Error" for the aborted command.

(7) Reselection timeout

The reselection is considered timed out if the INIT does not respond within 250ms, Selection Timeout Delay, from the time the IDC asserts the SEL and I/O signals during the execution of the Reselection phase. When the IDC detects the reselection timeout, it aborts the Reselection phase.

After aborting the Rselection phase, the IDC attempts retries for the reselection up to two times.

If the reselection is not successful, the IDC terminates the command which has requested the reconnection. No further reconnection is attempted and no status or Command Complete message is created for the aborted command. Then, the IDC creates the sense information with Sense Key/Additional Sense Code of "Aborted Command/Select-Reselect Failed".

(8) Internal controller error

If an error occurs within the IDC which is related to the SCSI hardware or firmware, the IDC terminates the present command with a "Check Condition" status and set the Sense Key/Additional Sense Code to "Hardware Error/Internal Controller Error" if the LUN has already been identified. This error does not prevent the INIT from retrying the command.

When the LUN has not been identified, the IDC immediately goes to the Bus Free phase with no sense information.

(9) Information Transfer timeout

If the IDC detects the timeout for REQ/ACK handshake during Information Transfer phase, the IDC immediately goes to the Bus Free phase and aborts the present command. The IDC creates the sense information with Sense Key/ Additional Sense Code of "Aborted Command/Internal Controller Error".

8.1.2 Recovery control

The retry procedures in IDC for the SCSI related error conditions described above are always invoked when the recoverable error condition occurred.

If the PER (Post Error) bit of the Error Recovery Parameters of Mode Select Parameters is set to '0', any recovered error, if any, is not reported to the INIT. The currently executing command terminates with "Good" status if no unrecoverable error occurs.

If the PER bit is set to '1', the recovered error condition, if any, is reported to the INIT if no unrecoverable error occurs. The IDC creates a "Check Condition" status with "Recovered Error" sense key and reports one of the following Additional Sense Code according to the detected error after completion of the command execution.

The default value of the PER bit in the IDC is '1'.

Recovered Error Condition	Additional Sense Code
Message Out phase parity error	47
Command phase parity error	47
Data Out phase parity error	47
Message Parity Error message	47
Initiator Detected Error message	48
Reselection timeout	45

Table 8.1 summalizes the retry procedures for SCSI related error conditions.

Table 8.1 Retry procedure for SCSI error conditions

Error Conditions		LUN	PER	Number of Retries	Termination procedure			
					Retry Success		Retry Out	
					Status	Sense data	Status	Sense data
Message Out phase Parity Error		I	0	2	Good	No sense data	Check	Aborted Command
			1		Check	Recovered Error		
		N	X		Good	No sense data	→Bus Free	No sense data
Command phase Parity Error		I	0	2	Good	No sense data	Check	Aborted Command
			1		Check	Recovered Error		
		N	X		Good	No sense data	→Bus Free	No sense data
Data Out phase Parity Error		X	0	2	Good	No sense data	Check	Aborted Command
			1		Check	Recovered Error		
Initiator Detected Error Message		X	0	1	Good	No sense data	Check	Aborted Command
			1		Check	Recovered Error		
Rejected Message	Command Complete	X	X	No retry	—		→Bus Free	No sense data
	Disconnect	X	X	No retry	Continues the command without disconnection			
	Identify	X	X	No retry	—		→Bus Free	Aborted Command
	Linked Command Complete	X	X	No retry	—		→Bus Free	Aborted Command
	Message Reject	X	X	No retry	—		Check	Aborted Command
	Restore Pointers	X	X	No retry	—		Check	Based on original error
	Save Data Pointer	X	X	No retry	Continues the command without disconnection			
	Sync. Transfer Request	X	X	No retry	Continues the command with asynchronous mode			
Message Parity Error Message		X	0	1	Good	No sense data	→Bus Free	Aborted Command
			1		Check	Recovered Error		
Reselection Timeout		X	0	2	Good	No sense data	→Bus Free	Aborted Command
			1		Check	Recovered Error		
Internal Controller Error		I	X	No retry	—		Check	Hardware Error
		N					→Bus Free	No sense data
Information Transfer Timeout		X	X	No retry	—		Check	Aborted Command

LUN I; : The LUN is already identified
N : The LUN is not identified
X : Don't care

PER 0 : PER (Post Error) bit is set to '0'
1 : PER (Post Error) bit is set to '1'
X : Don't care

→ Bus Free: The IDC goes to Bus Free phase without Disconnect or Command Complete message

8.2 Device Error Conditions and Retry

This section describes how to recover from the various errors detected between the IDC and the disk drive. The retry procedures taken by the IDC can be controlled by the INIT through Mode Select Parameters.

8.2.1 Error conditions and retry procedure

(1) Seek error

A seek error causes repositioning to be performed up to specified times with rezero operation for each repositioning if the recovery action is allowed.

If IDC is connected with SCSI when a seek error is detected, the IDC disconnects SCSI for error recovery as long as disconnection is permitted.

(2) Uncorrectable ID field data check (including "No Synch Byte Found")

This data check causes the ID field to be re-read up to specified times after one revolution if the recovery action is allowed. If the error is not recovered in spite of the fourth retry, repositioning is performed after a rezero operation, then IDC performs a fifth and subsequent retires.

If this error is detected for any operation other than writing to a disk medium, the head offset operation is performed during the retires.

(3) Correctable ID field data check

If correction disable mode is specified, or if this error is detected when the ID field is verified to confirm the position for write operation, the retry procedure (2) is performed.

If the correction enable mode is specified in all commands performing read operations on a disk medium, then the errors are automatically corrected within IDC, and processing restarts after one revolution.

(4) Uncorrectable data field data check (including "No Sync Byte Found")

IDC re-reads the data up to specified times after one revolution if the recovery action is allowed. If the error is not recovered in spite of the fourth retry, IDC repositions to the data block after a rezero operation, then performs a fifth and subsequent retries. These error retries are performed together with head offset motions.

(5) Correctable data field data check

IDC re-reads the data up to five times by the same procedure as (4). If the correctable data check persists, the following procedure is performed.

If correction disable mode is specified, the automatic correction facility in IDC is inhibited, then the recovery procedure (4) is performed.

If the correction enable mode is specified, the errors are automatically corrected within IDC, then the command processing is continued according to other recovery control flags. In this case, the data sent to the INIT, if any, has already been corrected.

(6) Sector overrun

A sector overrun occurs if the target block has been passed because of delayed response from the INIT in the reconnection sequence when the dual sector buffer mode is specified for data buffer management scheme. See Section 6.3 for details.

When a sector overrun occurs, the processing for the target data block starts after waiting one revolution if the recovery action is allowed. Meanwhile, the connection with the INIT is maintained.

(7) Data overrun

This error may occur only when the dual sector buffer mode is specified for data buffer management scheme due to delayed response from the INIT in the Data In or Data Out phase.

If the recovery action is allowed, the IDC repositions to the data block after waiting one revolution, and it continues processing from the block where the overrun has occurred. If a data overrun occurs while data fields are written, the corresponding data field is temporarily filled with data X'00', and is then rewritten during retry after waiting one revolution. While waiting a revolution, IDC keeps the connection with SCSI.

(8) Internal controller error or drive fault conditions

If an error occurs within the IDC which is related to the drive interface hardware or firmware, or if a drive fault condition is reported to the IDC from the drive, the IDC terminates the present command with a "Check Condition" status and a "Hardware Error" sense key. This error does not prevent the INIT from retrying the command.

8.2.2 Recovery control

The following Mode Select parameters called Pages are provided to control the retry procedures taken by the IDC for device error conditions described above. The INIT can select the recovery control flags or retry count by issuing a Mode Select command.

(1) Error Recovery Parameters: Page code 1

	Bit 7	6	5	4	3	2	1	0	
BYTE 0	0	0	0	0	0	0	0	1	
1	X'06' (Page Length)								
2	0	0	TB	0	0	PER	DTE	DCR	
3	X'00'–'FF'		(Retry Count for Read recovery)						
4	X'nn'		(Correction Span)						(*1)
5	X'nn'		(Head Offset Count)						(*1)
6	X'nn'		(Data Strobe Offset Count)						(*1)
7	X'nn'		(Recovery Time Limit)						(*1)

*1: The Correction Span, Head Offset Count, Data Strobe Offset Count and Recovery Time Limit are not changeable. The IDC ignores these field values.

- TB = (Transfer block)

  '1' indicates that the failing data block (recovered or unrecoverable) shall be transferred to the INIT. '0' indicates that the failing data block (recovered or unrecoverable) shall not be transferred to the INIT.

  The default value of TB bit in the IDC is '1'.

- PER = (Post Error)

  '1' requests the IDC to enable the reporting of the "Check Condition" status for recovered errors, with the appropriate sense key. The "Check Condition" occurs during the data transfer phases depending either on the DTE bit value or if an unrecoverable error occurred. If multiple errors occur, the sense data indicates the block address of either the last block on which the recovered error occurred if no unrecoverable error occurred, or the first block on which the unrecoverable error occurred.

  '0' indicates that the IDC does not create a "Check Condition" status for errors recovered within the limits established by the other Error Recovery Flags. Any unrecoverable error is reported by the IDC. The transfer of data may terminate prior to exhausting the Transfer Length depending on the error and the state of the DTE bit.

  The default value of PER bit in the IDC is '1'.

  When the PER bit is set to '1', the following error conditions, if any, are reported with "Recovered Error" sense key if no unrecoverable error occurred.

Recovered Error Condition	Additional Sense Code
Seek error	15
Read data error with re-read retries	17
Read data error with ECC correction	18
Recovered ID with re-read retries	00
Recovered ID with ECC correction	1E
Data overrun/Sector overrun	00
Read error of defect list	19

- DTE = (Disable Transfer on Error)

  If the PER bit is set to '1', this bit of '1' requests the IDC to create a "Check Condition" status and terminate the data transfer immediately upon detection of any recovered or unrecoverable error. The Transfer Length is then not exhausted. The data block on which the error occurred may or may not be transferred to the INIT depending on value of the TB bit. This DTE bit can only be set to 1 by the INIT if the PER bit is set to 1.

  This bit of '0' enables data transfer for any data which can be recovered. If the PER bit is set to '1', the last recovered error is posted after the Transfer Length is exhausted.

  The default value of DTE bit in the IDC is '0'.

- DCR = (Disable correction)

  '1' indicates that the IDC does not correct the correctable data even if possible, then retries within the limits of the error recovery flags. '0' indicates that the data shall be corrected if possible. The default value of DCR bit in the IDC is '0'.

- Retry Count for Read recovery (*2)

  This byte specifies the number of times of the read recovery algorithm. This is applied to the re-reading for the uncorrectable read error. The default value of this field in the IDC is eight (8).

(2) Additional Error Recovery Parameters : Page code 21

	Bit 7	6	5	4	3	2	1	0
BYTE 0	0	0	1	0	0	0	0	1
1	X'02' (Page Length)							
2	X'00'-'FF' (Retry Count on Seek Error)							
3	X'00'-'FF' (Retry Count on Overrun)							

- Retry Count on Seek Error (*2)

  This byte specifies the maximum number of times that the IDC attempts its Seek recovery algorithm. The default value of this byte in the IDC is eight (8).

- Retry Count on Overrun (*2)

  This byte specifies the maximum number of times that the IDC attempts its recovery action for Data Overrun and/or Sector Overrun. The default value of this byte in the IDC is one (1).

*2: If the value of zero is set for the retry count, the corresponding retry action is inhibited.

Table 8.2 summalizes the retry procedure for the device error conditions. The symbols in table 8.2 are as follows:

R:	Retry is attempted if the corresponding Retry Count is other than Zero (*3).
RR:	Re-read retry is attempted if the Retry Count for read recovery is other is other than zero (*3).
ECC:	Correction is applied by using the ECC.
ECC(RD):	Correction is applied by using the ECC except that RR is applied when this error is detected during verifying the ID for write operation.
Ⓡ :	The retry is completed successfully (Recovered error).
Ⓤ :	The retry terminated unsuccessfully (Unrecoverable error) (*3).
TD:	The data of the recovered or unrecoverable block is transfered to the INIT for the following commands; • Read, • Read Extended, • Read ID
NT:	The data of the recovered or unrecovarable block is not transferred to the INIT.
GD:	A "Good Condition" status is reported at the end of the command execution if no unrecoverable error occurred.
CK:	The execution of the present command stops, then a "Check Condition" status with the appropriate sense key is reported.
RE:	The execution of the present command proceeds. A "Check Condition" status with "Recovered Error" sense key and the last block on which the recovered error occurred are reported at the end of the command execution if no unrecoverable error occurred.
RE(STP):	The execution of the present command stops, then a "Check Condition" status with "Recovered Error" sense key and the first block on which the recovered error occurred are reported.

*3: If the Retry Counter corresponding to the error occurred is specified as zero, no retry for the error is attempted. In this case, the action taken by the IDC is the same as the unrecoverable error.

Table 8.2 Retry procedure for device error conditions

Flags				Seek error	Data check on ID field		Data check on Data field		Sector overrun	Data Overrun
PER	DTE	DCR	TB		Uncorrectable or No sync byte	Correctable	Uncorrectable or No sync byte	Correctable		
0	0	0	0	R Ⓡ; GD Ⓤ; CK	RR Ⓡ; TD, GD Ⓤ; NT, CK	ECC (RD), TD, GD	RR Ⓡ; TD, GD Ⓤ; NT, CK	ECC, TD, GD	R Ⓡ; GD Ⓤ; CK	R Ⓡ; TD, GD Ⓤ; TD, CK
0	0	0	1		RR Ⓡ; TD, GD Ⓤ; TD, CK		RR Ⓡ; TD, GD Ⓤ; TD, CK			
0	0	1	0		RR Ⓡ; TD, GD Ⓤ; NT, CK		RR Ⓡ; TD, GD Ⓤ; NT, CK			
0	0	1	1		RR Ⓡ; TD, GD Ⓤ; TD, CK		RR Ⓡ; TD, GD Ⓤ; TD, CK			
1	0	0	0	R Ⓡ; RE Ⓤ; CK	RR Ⓡ; TD, RE Ⓤ; NT, CK	ECC (RD), TD, RE	RR Ⓡ; TD, RE Ⓤ; NT, CK	ECC, TD, GD	R Ⓡ; RE Ⓤ; CK	R Ⓡ; TD, RE Ⓤ; TD, CK
1	0	0	1		RR Ⓡ; TD, RE Ⓤ; TD, CK		RR Ⓡ; TD, RE Ⓤ; TD, CK			
1	0	1	0		RR Ⓡ; TD, RE Ⓤ; NT, CK		RR Ⓡ; TD, RE Ⓤ; NT, CK			
1	0	1	1		RR Ⓡ; TD, RE Ⓤ; TD, CK		RR Ⓡ; TD, RE Ⓤ; TD, CK			
1	1	0	1	R Ⓡ; RE (STP) Ⓤ; CK	RR Ⓡ; TD, RE (STP) Ⓤ; TD, CK	ECC (RD), TD, RE (STP)	RR Ⓡ; TD, RE (STP) Ⓤ; TD, CK	ECC, TD, RE (STP)	R Ⓡ; RE Ⓤ; CK	R Ⓡ; TD, RE Ⓤ; TD, CK
1	1	1	0		RR Ⓡ; NT, RE (STP) Ⓤ; NT, CK		RR Ⓡ; NT, RE (STP) Ⓤ; NT, CK			
1	1	1	1		RR Ⓡ; TD, RE (STP) Ⓤ; TD, CK		RR Ⓡ; TD, RE (STP) Ⓤ; TD, CK			

Note: The default values of the recovery control flags in the IDC are PER='1', DTE='0', DCR='0', and TB='1'.

8.3 Initiator Recovery Procedure (Recommended)

8.3.1 Command retry

This subsection describes the recommended error recovery procedures which shall be performed by the INIT when the SCSI command terminated abnormally.

The INIT shall issue a Request Sense command to obtain the detailed information with regard to the error detected by the TARG when the INIT received a "Check Condition" status, or after the TARG goes to Bus Free phase forcedly. Then the INIT can determine which recovery action shall be taken depending on the sense key as described below:

(1) Recovered Error : Sense Key = 1

The error has already been recovered by some recovery action performed by the IDC. If the DTE bit of the error recovery flags in Mode Select parameter is set to '0', no recovery action by the INIT is required.

Note that the command has terminated without or with exhausting the transfer length if te DTE bit is set to '1', and the recovery procedure which shall be taken by the INIT depends on the intention of the INIT which sets the DTE bit to '1'. See Subsections 8.1.2 and 8.2.2 for details.

(2) Not Ready : Sense Key = 2

Reissue the original command at least once although operator intervention may be required to correct this condition.

(3) Medium Error : Sense Key = 3

Reissue the original command at least once after issuing a Rezero Unit command.

If a "No Defect Spare Location Available (Additional Sense Code = X'32')" or "Defect List Error (Additional Sense Code = X'19')" persists, re-initializing of the medium is required.

(4) Hardware Error : Sense Key = 4

Reissue the original command at least once.

If a "Seek Error (Additional Sense Code = X '15')" was reported, issue a Regero Unit command before retrying the command.

If one of Diagnostic Failure (Additional Sense Code = X'40', X'41' or X'42') was reported, issue SCSI Reset condition, then re-test the hardware function by using a Send Diagnostic command or Diagnostic switch.

(5) Illegal Request : Sense key = 5

Check the CDB, LUN, or parameter list which has been sent to the IDC. For detailed reason, refer to Table 7.5 and 7.6. If the reason is an "Invalid Message", check the SCSI message protocol managed by the INIT.

(6) Unit Attention : Sense key = 6

Reissue the original command. If the synchronous data transfer is required and re-negotiationn for the synchronous transfer has not been completed, the INIT shall create an Attention condition then send a Synchronous Data Transfer Request message when it reissues the command. Normally, the IDC attempts to re-negotiate for the synchronous transfer before it reports a "Check Condition" status with "Unit Attention" sense key.

(7) Data Protect : Sense key = 7

Abort the processing in the INIT. If the rejected command has been linked from a Set Limits or a Set File Mask command, check the parameters specified on those commands and the CDB of the rejected command.

(8) Aborted Command : Sense key = B

Reissue the original command at least once. In case of a Copy command, check that the destination and the source LUN are in Ready state, then reissue the command.

(9) Miscompare : Sense Key = E

If a Verify command terminated with this sense key, reissue the command at least once. If the error persists, it is recommended to check the erroneous data pattern by reading the data block and comparing it with the data which has been sent from the INIT during the Verify command.

If a Read Buffer command terminated with this sense key, re-execute the buffer diagnostic test from the original Write Buffer command.

8.3.2 Medium defect management

This Subsection describes the defect management scheme for the disk medium after completion of the initialization of disk drive. See Section 2.7 for the initialization of disk drive at the installation time.

(1) Primary Defect List

Any data block which contains the defects detected by the original manufacturer of the drive can not be used as a normal data block. These defects shall be considered as permanent defects. The location of these defects has been recorded in the Primary Defect List (P List) on the drive. The INIT can read the defect list by using a Read Defect Data command.

During the execution of a Format Unit command, the IDC performs a medium defect manegement scheme which can be selected by the INIT. The INIT shall not inhibit the usage of the P list of defects by the IDC during the Format Unit command except a special purpose testing of the medium.

Further, the INIT shall not reclaim the defective block which is included in the P list as a normal data block.

(2) Data block certification

The following describes the recommended data block certification procedure which may be performed by the INIT after completion of the initialization of disk drive. or after persisting data check was detected on a data block.

The INIT can perform the certification of the data block(s) by executing Read after Write checking called PASS, where a PASS is defined as that two times write and read operations are performed for the same data block(s) on the primary area.

For the Read after Write checking executed during the PASS, the INIT shall issue a Write or Write Extended command with the recommended data pattern of repeated X 'CCCCCCF6DB4CCCCC'. Then the INIT shall issue a Read, Read Extended, or Verify command after completion of the write operation. The INIT shall set both DTE and PER bits of the error recovery parameters to '1' during executing the PASS(s).

It can be considered as sufficient checking to perform one PASS for the certification of the data block although the number of PASSs to be executed shall be determined based upon system requirements.

If a medium error is detected during the PASS, the INIT shall re-execute the PASS for the data block on which the medium error was detected at least eight (8) times. If the error is detected again during the re-execution, the INIT shall treat the data block as a defective block.

The INIT shall not perform the data block certification for the medium which has been initialized without using the P list of defects.

(3) Alternate block assignments

The INIT shall assign the alternate block for the data block which has determined as a defective block by the certification by issuing a Reassign Blocks command. Note that the logical block address of the primary area shall be always specified for the Reassign Blocks command.

After completion of the Reassign Blocks command, it is required to certify the data block for which the alternate data block has been assigned.

It is recommended to link a Reassign Blocks command from a Displaced ID command according to the type of error detected during the certification. Figure 8.1 shows the recommended procedure for alternate block assignments.

The location of the data block(s) which is specified through the Reassign Blocks command is recorded in the Grown Defect List (G List) on the drive. The INIT can read the defect list by using a Read Defect Data command.

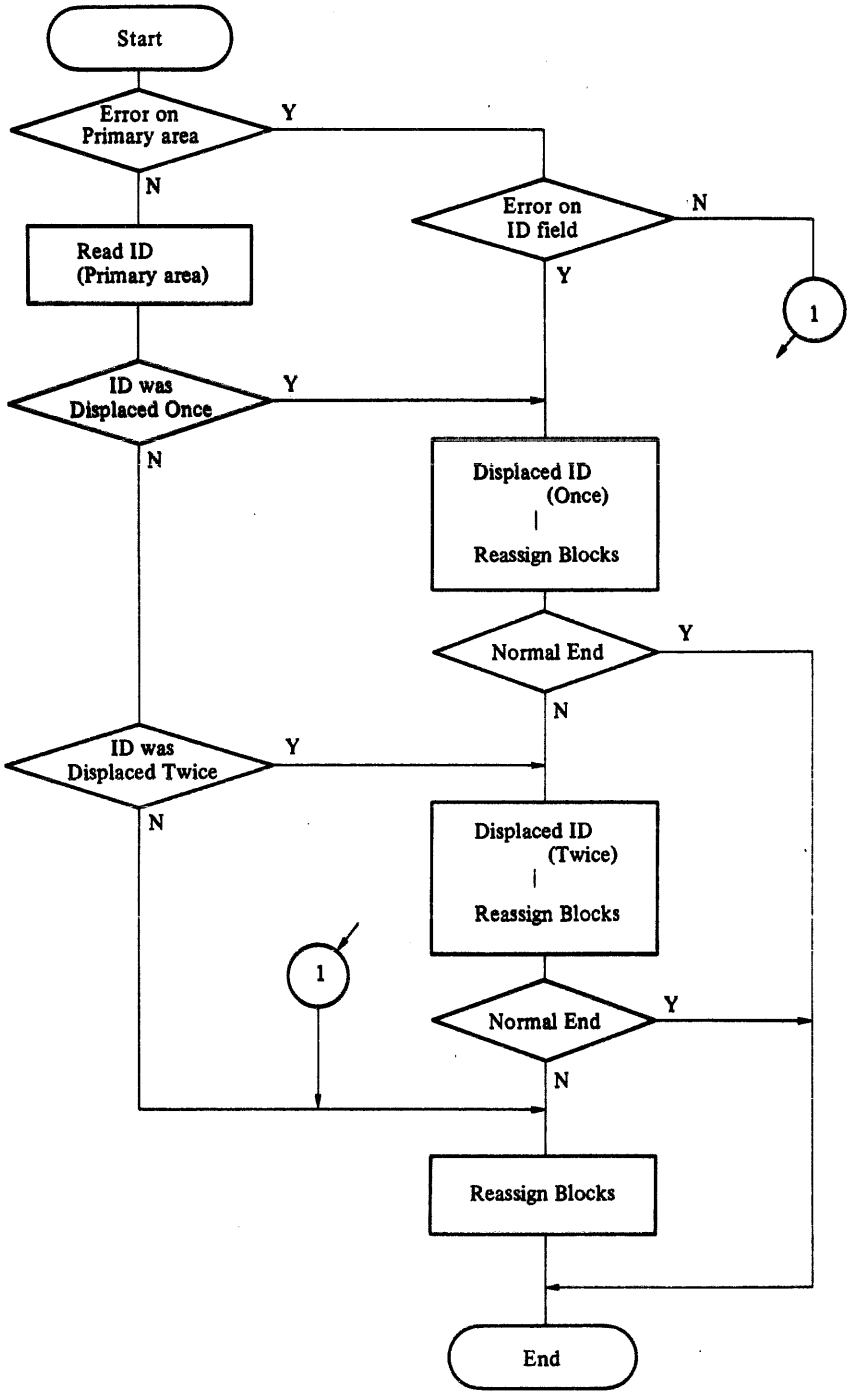


Figure 8.1 Alternate Block assignments (recommended)

(4) Re-initializing

The INIT can re-initialize the disk medium by issuing a Format Unit command. Note that the data block size of the medium can not be changed and that all data blocks are filled with X'00' by the re-initializing.

Figure 8.2 shows CDB of a Format Unit command and format of the Data Defect List which may be sent from the INIT during a Format Unit command.

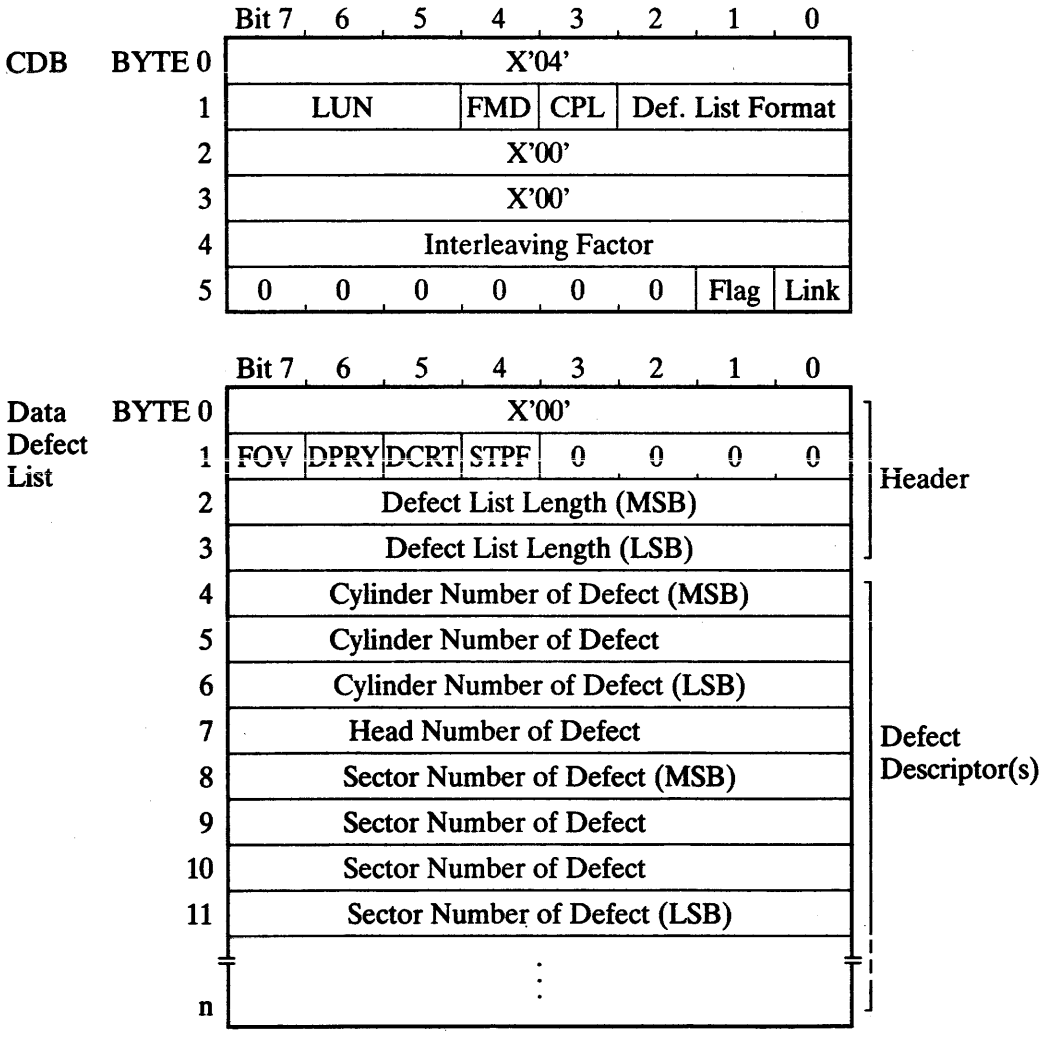


Figure 8.2 Format Unit command and Data Defect List

For the re-initializing, one of the following variations of formating and defect management is recommended. After completion of the re-initializing, the INIT shall perform the data block certification described above. Then, an erroneous data block, if any, shall be reassigned an alternate block.

(a) Using P list only (Permanent factory defect list):

CDB byte-1	Header byte-1	Defect List	Defect
Bit 4 3 2 1 0	FOV DPRY DCPT STPF	Length	Descriptro(s)
0 0 0 0 0	---------- (No Data Out phase)		----------

The IDC formats the entire medium by using the P list of defects and erases the existing G list of defects, so that the disk drive is re-initialized to the same condition as at original shipment.

(b) Using P and G lists (Permanent and grown defect lists):

CDB byte-1	Header byte-1				Defect List	Defect
Bit 4 3 2 1 0	FOV	DPRY	DCPT	STPE	Length	Descriptor(s)
1 0 0 0 0	0	0	0	0	0	(None)

The IDC formats the entire medium by using the P and the existing G lists of defects.

(c) Supplying defect list

CDB byte-1	Header byte-1				Defect List	Defect
Bit 4 3 2 1 0	FOV	DPRY	DCPT	STPE	Length	Descriptor(s)
1 1 1 0 1	0	0	0	0	8×m	m Descriptors

The IDC formats the entire medium by using the P list and the Data Defect List (D List) which is sent from the INIT, and the existing G list is replaced by the D list of defects.

Before issuing this combination of a Format Unit command, the INIT shall perform the following procedures to create the D list of defects:

- Issue a Read Defect Data command which requests the P and G lists to get the existing lists of defects.
- Delete the duplicated defect data (if any) from the retrieved G list of defects, then use it as the Data Defect List.

(5) Space ID & Read Data command

The INIT can read-out the data field of a block on which an unrecoverable error of the ID field persists by using a Space ID & Read Data command. The INIT shall set the TB bit of the error recovery parameters to '1' before issuing this command.

Note that the INIT has to specify the data area (Primary or Alternate) to be accessed by this command explicitly because no verification check of the ID field and no defect/alternate switching are performed by the IDC.

To read-out the data block on Primary area, issue this command with block address of the primary area by linking from a Set File Mask command which allows group-6 commands.

To read-out the data block on Alternate area, issue this command with block address of the alternate area by linking from a Set File Mask command which allows group-6 commands and specifies the alternate area.

8.3.3 Error logging

It is preferred that the INIT performs error logging of errors reported by the IDC to gather the information which is useful for the preventive maintenance.

The recommended scheme of error logging is preserving all bytes of sense data returned by the IDC with a time-stamp.

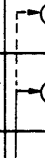
By specifying the PER bit of the error recovery parameters to '1', the INIT can be informed of a recovered error (if any), so that the INIT can log it as well as unrecoverable error.

CHAPTER 9 DIAGNOSIS AND MAINTENANCE

9.1 Diagnosis

Table 9.1 lists the IDC test functions. These test facilities can not only be executed at initial diagnosis or by the diagnostic switch, but also be activated from an INIT by a Send Diagnostic command.

Table 9.1 Test functions

Test Code (HEX)	Test name	Initial diag-nosis	diag-nostic switch	Send Diagnostic Command		
				Self Test=1 Unit Offline=0	Self Test=1 Unit Offline=1	Self Test=0
40	IDC hard-core test	○		○	○	○
80	Seek test				○	○
81	Write/read test (CE space)				○	○

Note: The circles refer to the test which is performed, while the directed lines show an execution sequence of tests.

9.1.1 Initial diagnosis

Initial diagnosis is performed upon powering on IDC or after detecting an SCSI Reset condition, and tests the IDC hardware function (test code = 40). Upon successful completion of the tests, IDC becomes ready for operation on SCSI.

If an error is detected in the test, the LEDs on the IDC PCA indicate the error status. The IDC then reports a "Check Condition" status against an I/O request. The sense data which can be obtained by a Request Sense command issued after the "Check Condition" status (sub-error class = 7, sub-error code = 8 or F) details error information. This status can be cleared by an a SCSI Reset condition.

9.1.2 Diagnostic switch

This diagnosis is initiated by the diagnostic switch (SW3) on the IDC PCA. It tests the IDC hardware function (test code = 40) and the devices (test code = 8X). The device tests are performed sequentially for all devices that are ready state.

When the diagnostic switch is returned to 'NORMAL' position, the IDC becomes ready for operation on SCSI after all the tests have terminated .

When any error has been detected in a series of the test, the IDC status after the releasing of the diagnostic switch is the same as that for errors detected during initial diagnosis. The LEDs and sense data then indicate an error detected last. For errors detected during the device test (test code = 8x), the error status is cleared as soon as the sense data is read by an INIT, then the IDC goes to the ready state.

9.1.3 Send Diagnostic command

Figure 9.1 shows the CDB format of a Send Diagnostic command. If the self test bit is set to '1', the IDC executes IDC hardware function test (test code = 40) and device tests (test code = 8X) on a specified LUN, as listed in Table D.1.

If the unit offline bit in the CDB is set to '0' when the self test bit is '1', the IDC performs IDC hardware function test only. If the unit offline bit is set to '1' when the self test bit is '1', the device tests are executed after completion of the IDC hardware test. The test terminates when an error is detected during the test. IDC then reports a "Check Condition" status. Sense data (sub error class = 7, sub error code = 8 or F) represents detailed error information. Error data takes the same format as the test result data described later. Upon successful completion of all the tests, IDC reports a "Good" status.

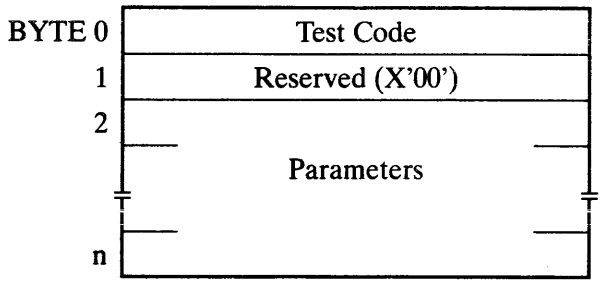
If the self test bit is set to '0', only the test specified in the parameter list transferred by this command is executed. A single Send Diagnostic command allows only one test to be specified.The INIT shall send an Activation parameter for each test described later during Data Out phase. Figure 9.2 shows the basic format of the parameter list (activation parameter).

Test results are retained as test result data in IDC and are transferred to the INIT when a Receive Diagnostic Results command is issued. Figure 9.3 indicates the CDB format of a Receive Diagnostic Results command, and Figure 9.4 shows the basic format of the test result data which is transfered to the INIT by a Receive Diagnostic Results command.

The IDC executes the diagnostic test specified by a Send Diagnodtic command after completion of executing any commands that are in progress or that are queued.

		BIT							
		7	6	5	4	3	2	1	0
BYTE	00	0	0	0	1	1	1	0	1
	01	LUN			0	0	Self Test	0	Unit Offline
	02	0	0	0	0	0	0	0	0
	03	Parameter list length (MSB)							
	04	Parameter list length (LSB)							
	05	0	0	0	0	0	0	Flag	Link

Figure 9.1 CDB for Send Diagnostic command

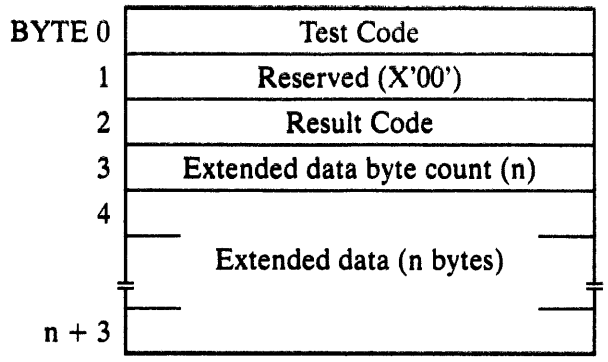


Test Code: Specifies a code indicating the test to be executed.
Parameters: Specify the details of the test. The specification depends on the test code.

Figure 9.2 Send Diagnostic command parameter list

		BIT							
		7	6	5	4	3	2	1	0
BYTE	00	0	0	0	1	1	1	0	0
	01	LUN			0	0	0	0	0
	02	0	0	0	0	0	0	0	0
	03	Transferring byte count (MSB)							
	04	Transferring byte count (LSB)							
	05	0	0	0	0	0	0	Flag	Link

Figure 9.3 CDB for Receive Diagnostic Results command



Test Code: Indicates the code of the test executed.
Result Code: Indicates the test result.
Extended data byte count: Indicates the length of extended data.
Extended data: Indicates the detailed test result.

Figure 9.4 Test results data basic format

The following shows the activation parameter (for a Send Diagnostic command) and the test result data for each test:

(1) IDC hand-core test

(a) Activation parameter

		BIT							
		7	6	5	4	3	2	1	0
BYTE	00	Test Code = X'40'							
	01	Reserved (X'00')							

(b) Test result data

		BIT							
		7	6	5	4	3	2	1	0
BYTE	00	Test Code = X'40'							
	01	Reserved (X'00')							
	02	Result Code (X'00': Normal termination)							
		Error	0	0	0	Buffer	REG	RAM	ROM
	03	Extended data byte count = X'01'							
	04	Extended data							

Extended data

Result Code	Extended data
X'81' or X'82'	X'01': Odd address defective X'02': Even address defective
X'84'	Defective register address
X'88'	X'01': Buffer #A defective X'02': Buffer #B defective

(2) Seek test

(a) Activation parameter

		BIT							
		7	6	5	4	3	2	1	0
BYTE	00	Test Code = X'80'							
	01	Reserved (X'00')							
	02	Cylinder address (1) (MSB)							
	03	Cylinder address (1) (LSB)							
	04	Cylinder address (2) (MSB)							
	05	Cylinder address (2) (LSB)							
	06	Number of seeks to be executed							

Cylinder addresses (1) and (2) specify a range of seek operations. If a value exceeding the maximum cylinder address of the device tested is specified, it is assumed that the maximum cylinder address is specified. The number of seeks (byte 6) specifies the number of round-trip seek operations between the above two addresses. X'00' indicates 256 cycles.

When this test is initiated by the diagnostic switch or the Self Test bit of the Send Diagnostic command, 64 times of the seek operation between cylinder-0 and the maximum cylinder are performed.

(b) Test result data

		BIT							
		7	6	5	4	3	2	1	0
BYTE	00	Test Code = X'80'							
	01	Reserved (X'00')							
	02	Result Code (X'00': Normal termination)							
		Error	0	0	0	Fault	Seek Error	0	No Seek End
	03	Extended data byte count = X'02'							
	04	Unit Status							
	05	Fault Status							

(3) Write/read test (CE space)

(a) Activation parameter

		BIT							
		7	6	5	4	3	2	1	0
BYTE	00	Test Code = X'81'							
	01	Reserved (X'00')							

(b) Test result data

		BIT							
		7	6	5	4	3	2	1	0
BYTE	00	Test Code = X'81'							
	01	Reserved (X'00')							
	02	Result Code (X'00': Normal termination)							
		Error	Sub-Error Class			Sub-Error Code			
	03	Extended data byte count = X'04'							
	04	Cylinder address (MSB)							
	05	Cylinder address (LSB)							
	06	Head address							
	07	Block address							

The sub-error class and sub-error code of the result code byte are the same as the definition in the extended sense data. Bit 7 always takes '1' when an error occurs. X'80' indicates a mismatch was detected during data comparion.

9.2 Maintenance

9.2.1 Spare parts

Table 9.2 lists the spare parts for the IDC.

Table 9.2 Spare parts list

No.	Name	Specification	Quantity	RM	Remarks
1	M1053BD PCA	B05B-2180-B101A	1	R	
2	SMD A-cable for M1053A11	B660-1065-T124A#L60R00	1	–	
3	SMD B-cable for M1053A11	B660-1065-T122A#L100R0	1	–	

Note: RM; Repairable Mark (R; Repairable)

9.2.2 Reliability and service goals

(1) MTBF

The MTBFs of the IDC during its life time are 150,000 hours estimated value.

Note: The MTBF is defined as follows:

$$\text{MTBF} = \frac{\text{Total operating time (hours)}}{\text{The number of equipment failures from all field sites}}$$

The operating time is the total time duration during which the power is on. Failure of the equipment means failure that required either repair or replacement. Mishandling, failures due to bad environmental conditions, power trouble, cable failures, or other failures not caused by the equipment are not included.

(2) MTTR

MTTR is the average time a well-trained service personnel should take to diagnose and repair the trouble. The IDC is designed for an MTTR of 30 minutes or less.

APPENDIX A DRIVE INTERFACE (FOR REFERENCE)

This chapter provides a brief description of the drive interface. Refer to the OEM Manual for the each drive for details.

A.1 Signal Lines

Figure A.1 to Figure A.4 show the signal lines and connector pin assignements.

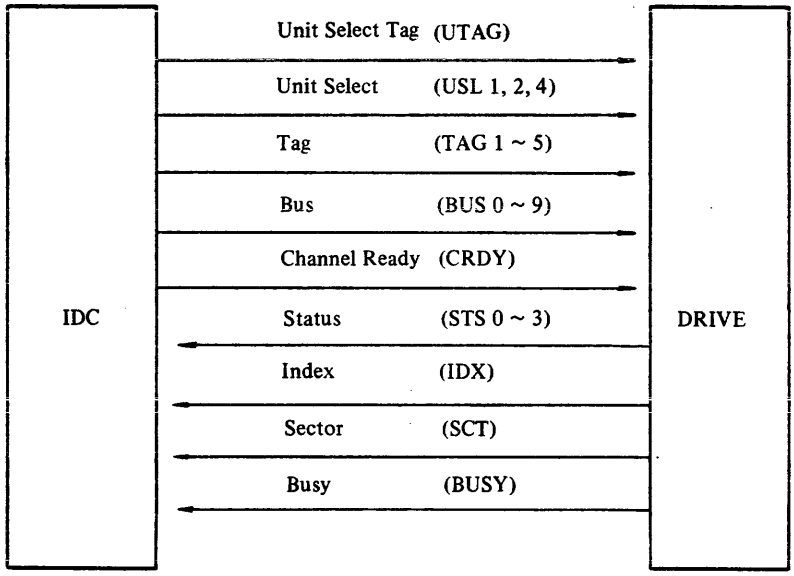


Figure A.1 Cable A signal lines

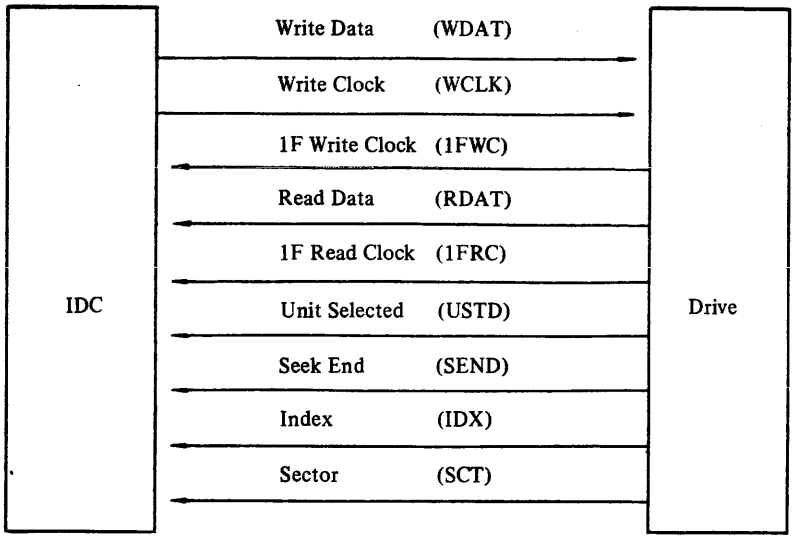


Figure A.2 Cable B signal lines

1	TAG 1	L	2	TAG 1	H
3	TAG 2	L	4	TAG 2	H
5	TAG 3	L	6	TAG 3	H
7	BUS 0	L	8	BUS 0	H
9	BUS 1	L	10	BUS 1	H
11	BUS 2	L	12	BUS 2	H
13	BUS 3	L	14	BUS 3	H
15	BUS 4	L	16	BUS 4	H
17	BUS 5	L	18	BUS 5	H
19	BUS 6	L	20	BUS 6	H
21	BUS 7	L	22	BUS 7	H
23	BUS 8	L	24	BUS 8	H
25	BUS 9	L	26	BUS 9	H
27	Channel Ready	L	28	Channel Ready	H
29	Status 3	L	30	Status 3	H
31	Status 2	L	32	Status 2	H
33	Status 1	L	34	Status 1	H
35	Index	L	36	Index	H
37	Status 0	L	38	Status 0	H
39	Status 5	L	40	Status 5	H
41	Busy	L	42	Busy	H
43	Unit Select Tag	L	44	Unit Select Tag	H
45	Unit Select 1	L	46	Unit Select 1	H
47	Unit Select 2	L	48	Unit Select 2	H
49	Sector	L	50	Sector	H
51	Unit Select 4	L	52	Unit Select 4	H
53	TAG 5	L	54	TAG 5	H
55	Status 4	L	56	Status 4	H
57	Not Used		58	Not Used	
59	TAG 4	L	60	TAG 4	H

Figure A.3 Cable A connector signal assignments

1	E		2	1F Write Clock	H
3	1F Write Clock	L	4	E	
5	Read Data	L	6	Read Data	H
7	E		8	1F Read Clock	H
9	1F Read Clock	L	10	E	
11	Write Clock	L	12	Write Clock	H
13	E		14	Write Data	H
15	Write Data	L	16	E	
17	Unit Selected	H	18	Unit Selected	L
19	Seek End	L	20	Seek End	H
21	E		22	Index	H
23	Index	L	24	E	
25	Sector	L	26	Sector	H

E : Ground

Figure A.4 Cable B connector signal assignments

A.2 Bus and Status Definition

(1) Tag 1 to 3 and Bus 0 to 9 signals

10-bit Bus contents are defined through the Tag 1, 2, and 3 signals as listed in Table A.1.

Table A.1 Tag/Bus definition

Bus \ Tag	Tag 1	Tag 2	Tag 3
	Cylinder Address	Head Address	Control Select
Bit 0	1	1	Write Gate
1	2	2	Read Gate
2	4	4	Servo Offset Plus
3	8	8	Servo Offset Minus
4	16	Undefined	Fault Clear
5	32	Undefined	AM Enable
6	64	Undefined	RTZ
7	128	Undefined	Undefined
8	256	Undefined	Undefined
9	512	Undefined	Release

(2) Tag 4 and 5, Status 0 to 5, Index, and Sector

The contents of 6-bit Status, Index, and Sector signals are defined through combinations of Tag 4 and 5 as listed in Table A.2.

Table A.2 Status definition

Tag 4, 5 / Status Bit	Tag 4 : 0 Tag 5 : 0	Tag 4 : 1 Tag 5 : 0	Tag 4 : 0 Tag 5 : 1	Tag 4 : 1 Tag 5 : 1
Status 0	Unit Ready	Sector Address 1	Fault 1	Device Type 1
Status 1	On Cylinder	Sector Address 2	Fault 2	Device Type 2
Status 2	Seek Error	sector Address 4	Fault 4	Device Type 4
status 3	Fault	Sector Address 8	Seek Error 1	Device Type 8
Status 4	File Protected	Sector Address 16	Seek Error 2	Device Type 16
Status 5	—	Sector Address 32	Seek Error 4	Device Type 32
Index	Index Pulse	Sector Address 64	VCM Heat	—
Sector	Sector Pulse	Sector Address 128	DC Motor Fault	—
Status Definition	Unit Status	Sector Count Status	Fault Status	Device Type

(a) Unit Status

- Unit Ready (Status 0)

  Indicates that the drive is in ready state.

- On Cylinder (Status 1)

  Indicates that the head is located on the track exactly. However, this status is not ensured if a Seek Error occurs.

- Seek Error (Status 2)

  Indicates that a seek or RTZ operation has terminated abnormally.

- Fault (Status 3)

  Indicates that an abnormal condition occurred in the drive. Write operation stops immediately after this bit is turned on.

- File Protected (Status 4)

  Indicates that the drive is set to write inhibit status by turning the switch on the drive PCA or on the drive operator panel.

(b) Fault Status

Indicates the detailed information about the seek error or fault status detected by the drive. Table A.3 lists the contents of status bits.

Table A.3 Fault Status

Sector	Index	Status Bits						Status	
		5	4	3	2	1	0	Status name	Explanation
×	×	×	×	×	0	0	1	Control Check 1	A read/write command was received during a head movement.
×	×	×	×	×	0	1	0	Control Check 2	A write command was received while in the state where write operations cannot be performed.
×	×	×	×	×	0	1	1	Write Offtrack Check	An offtrack occurred during write operation.
×	×	×	×	×	1	0	0	Write Unsafe Check	An error occurred during a write operation.
×	×	×	×	×	1	0	1	Write Protect Check	A write command was received during file protected condition.
×	×	×	×	×	1	1	0	R/W Multi Check	Multiple head are selected during write or read operations.
×	×	×	×	×	1	1	1	Emergency Check	The power-up sequence is unsuccessful or emergency fault occurs on VCM or DC motor.
×	×	0	0	1	×	×	×	RTZ Timeout	RTZ operation did not complete during the specified period.
×	×	0	1	0	×	×	×	Seek Timeout	Seek operation did not complete during the specified period.
×	×	0	1	1	×	×	×	Over-Shoot Check	The head moved out upon or after the head reaches to the target cylinder.
×	×	1	0	0	×	×	×	Seek Guard Band	The guard band was detected during seek operation.
×	×	1	0	1	×	×	×	Linear Mode Guard Band	The guard band was detected while the head was following the track in linear mode.
×	×	1	1	0	×	×	×	RTZ Outer Guard Band	The guard band was detected during RTZ mode.
×	×	1	1	1	×	×	×	Illegal Cylinder	A seek command was issued to illegal cylinder.
×	1	×	×	×	×	×	×	VCM Heat	Over-Load current flowed on VCM.
1	×	×	×	×	×	×	×	DC Motor Fault	Over-Load current flowed on DC motor.

APPENDIX B COMMAND PROCESSING TIME (FOR REFERENCE)

B.1 Command Execution Sequence

This section provides the timing information in a series of command execution sequences.

The values provided here are mere references proved under standard and normal operating conditions. So, use these values to estimate processing time in SCSI, by including the INIT response times.

(1) Activation sequence

Figure B.1 shows the activation sequence where the SCSI is disconnected after the transfer of the CDB. Figure B.2 illustrates the CDB transfer operations in detail.

(2) Reconnection sequence

Figure B.3 shows the reconnection sequence to be followed upon completion of the positioning onto a target data block when the dual sector buffer mode is selected, or to be performed to start the data transfer when the full buffering mode is specified.

In Figure B.3, the interval (Trps) between the start of the Reselection phase for reconnection and the beginning of a target data block is defined for dual sector buffer mode only. For details, see Subsections 6.3.2 and 6.3.3.

(3) Data transfer

(a) Full buffering mode

If the full buffering mode is specified, the data transfer time is determined by average data transfer rate on the SCSI. The approximation for the data transfer time (Txfr) can be obtained by following formula:

$$\text{Txfe} = \frac{\text{Number of bytes to be transferred}}{\text{SCSI average transfer rate (MB/S)}} \quad (\mu s)$$

(b) Dual sector buffer mode

The data transfer time depends on factors such as the type of command issued, the direction of data transfer, the data transfer speed in SCSI. Figure B.4 shows the definition of the data transfer time (Txfr). The approximation for Txfr can be obtained by following formulas:

- For Read operation

$$\text{Txfr}=(N \times m + 1) \times T_{SCT} + T_{CYL} \times p + T_{TRK} \times q$$

- For Write operation

  The time required to prefetch data for the first block is included in Trps.

  Thus,

$$Txfr = ((N-1) \times m + 1) \times T_{SCT} + T_{CYL} \times p + T_{TRK} \times q$$

Where

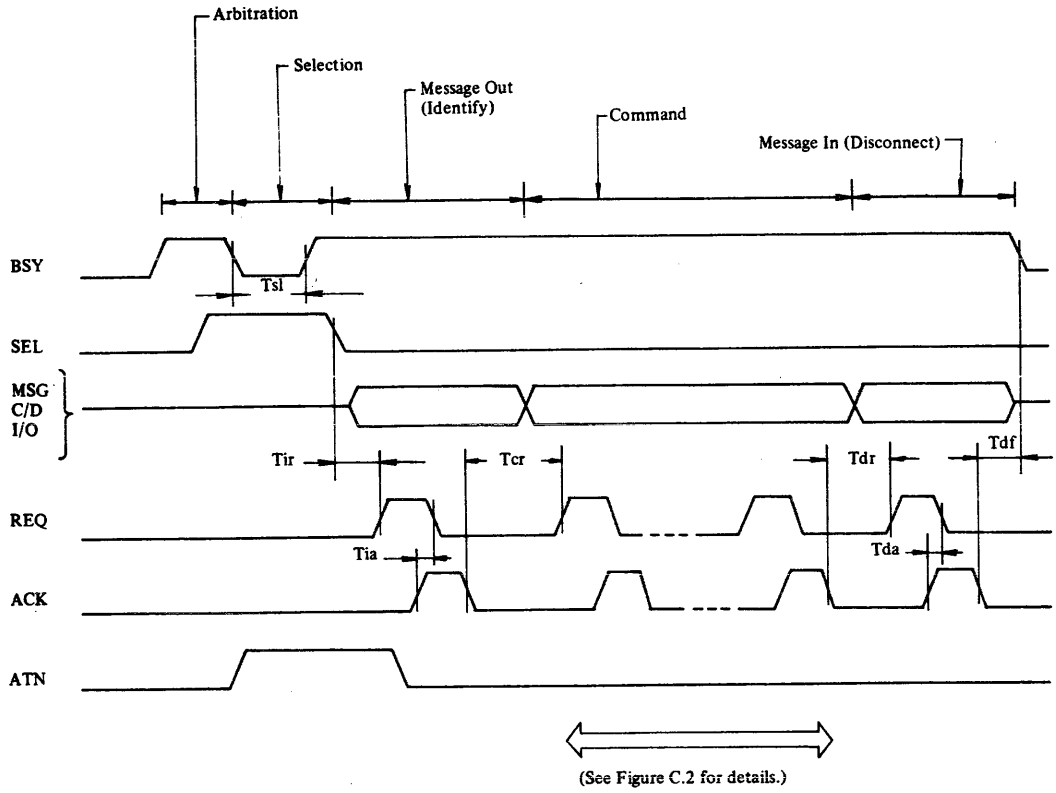
N: Procrssing block count
m: Interleaving factor (m = 1 if no interleaving is used.)
T_{SCT}: Processing time per sector
T_{CYL}: Add the value in the following table per one cylinder boundary only when the processed block extends over the boundary.
(p: Number of extending the cylinder boundary)
T_{TRK}: Add the value in the following table per one track boundary only when the processed block extends over the boundary.
(q: Number of extending the track boundary)

	T_{SCT}	T_{CYL}		T_{TRK}
	M2333/31KS	M2333KS	M2331KS	M2333/31KS
256-byte format	137.5	5525.6	5525.6	25.2
512-byte format	240.0	7302.7	6102.5	101.7
1,024-byte format	448.3	9042.3	6800.7	75.6

Unit: μs

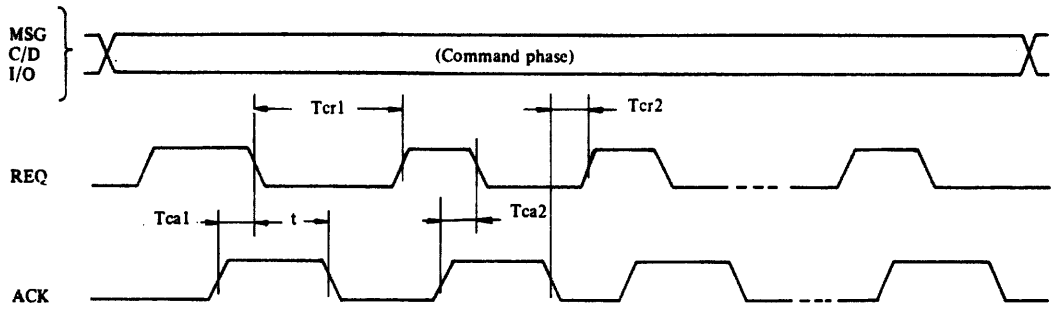
(4) Termination sequence

Figure B.5 is an example of transition to the Bus Free phase as a termination sequence from the completion of a read/wire operation on a data field. Figure B.6 is an example of a transition to fetching the next command (CDB) in a command link.



Tsl: 1 (μs)
Tir: (μs)
Tia: (μs)
Tcr: (μs)
Tdr: (μs)
Tda: (μs)
Tdf: (μs)

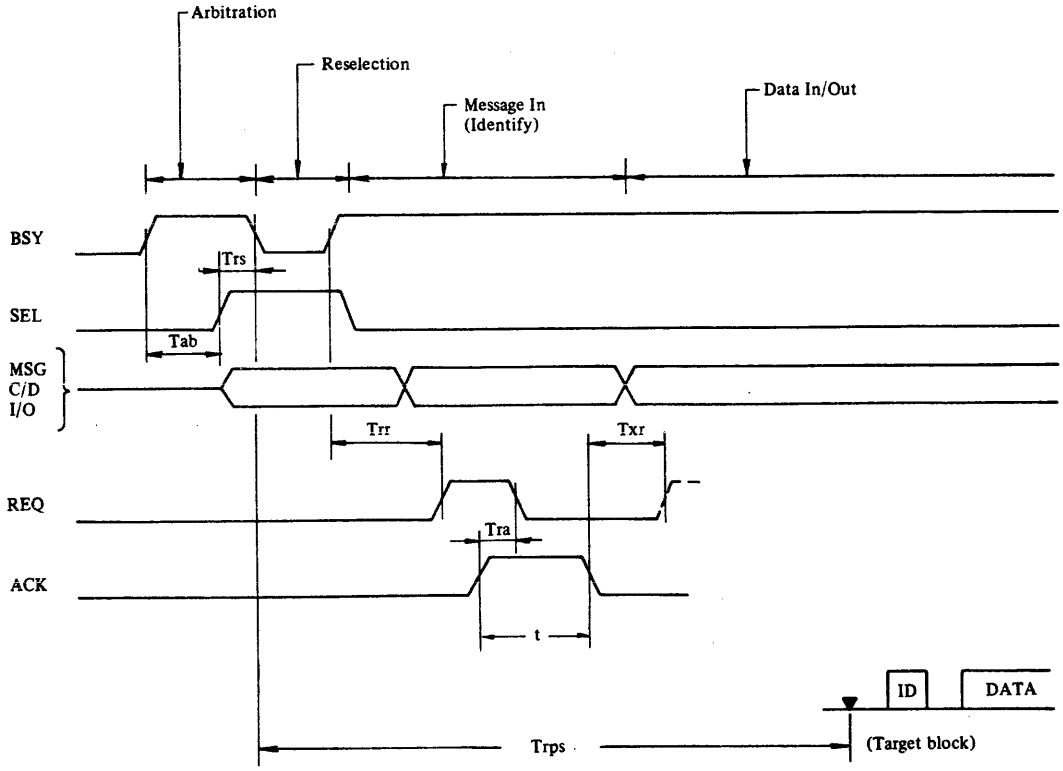
Figure B.1 Activation sequence processing time



Tca1: (μs)
Tcr1: + Max (, t) (μs) where, t is INIT's response time to release ACK.

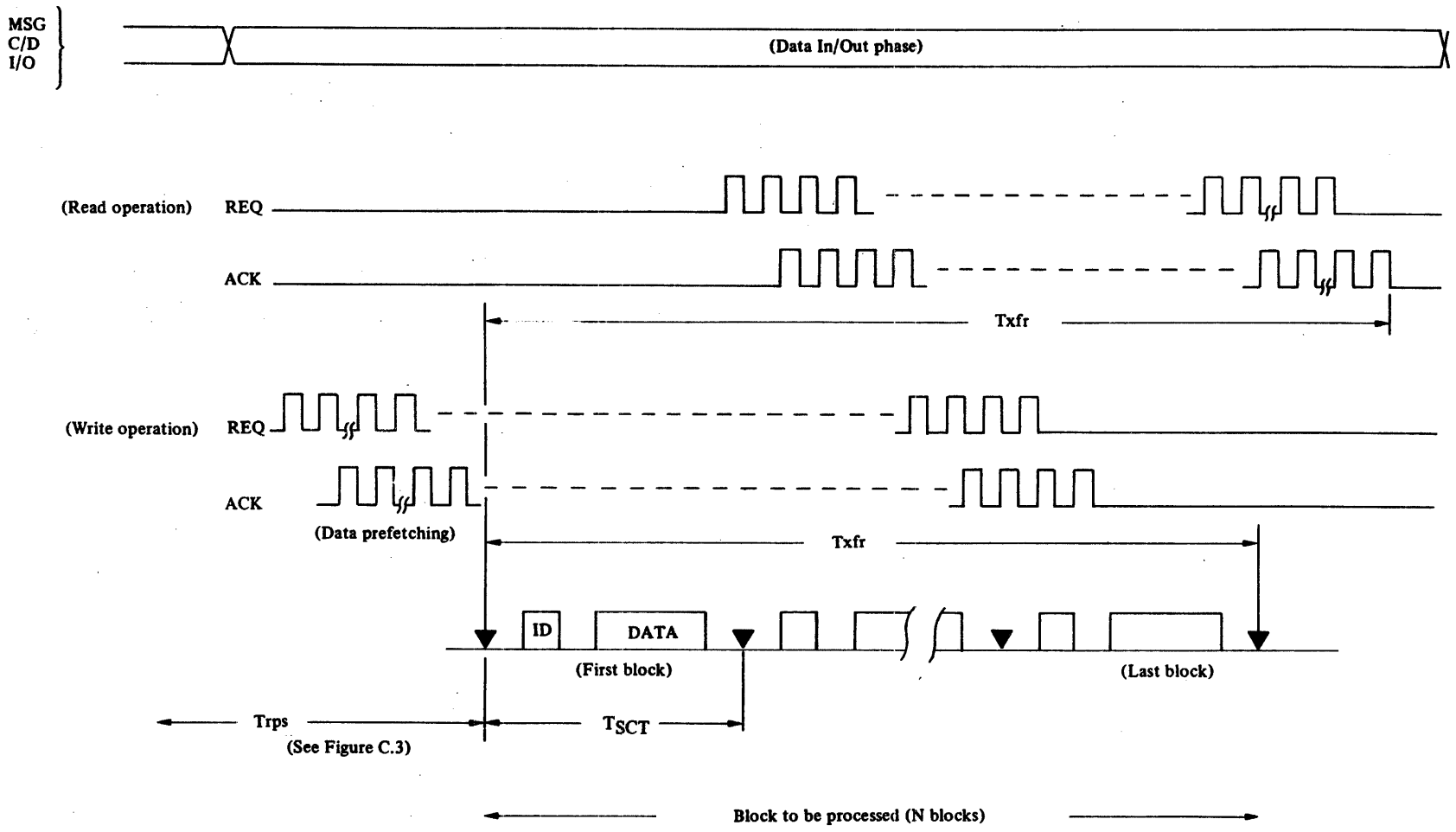
Tca2: (μs) } The same processing time is applied on and after the byte 2 to the
Tcr2: (μs) } last byte of the CDB.

Figure B.2 Command phase processing time



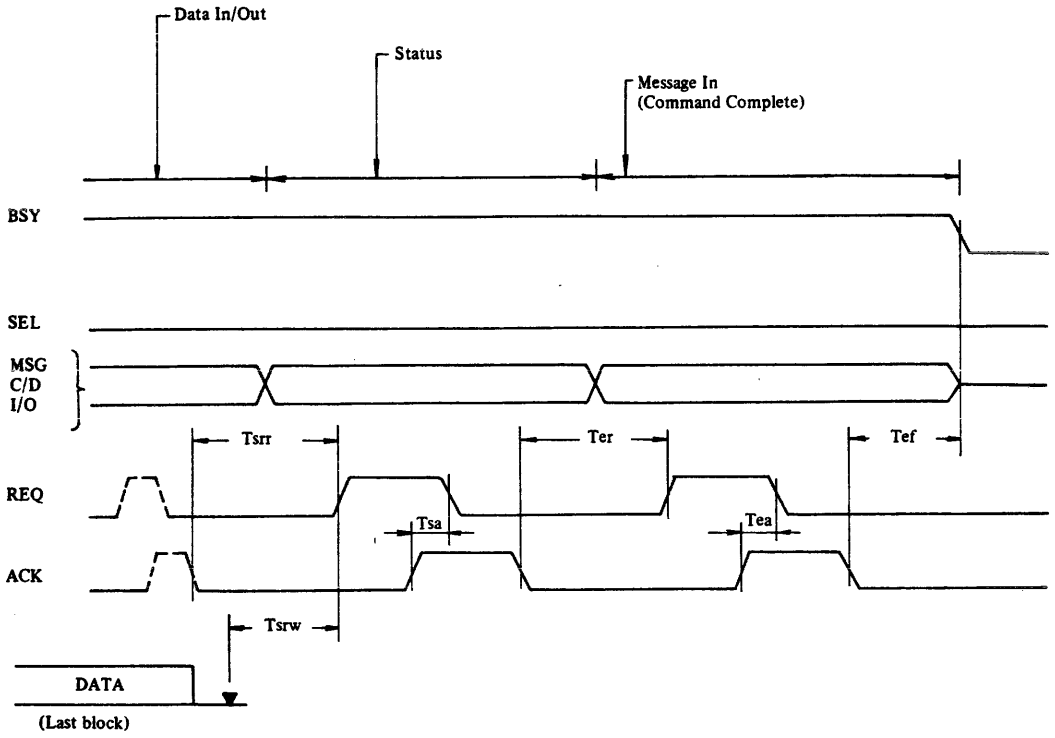
Trps: See Subsections 6.3.2 and 6.3.3, defined for dual sector buffer mode only.
Tab: 6.5(μs)
Trs: 2.9(μs)
Trr: (μs)
Tra: (μs)
Txr: (μs) (When prefeteching data in a write operation)
(μs) (When transferring data in a read operation by using full buffering mode)

Figure B.3 Reconnection sequence processing time



Txfr, T_{SCT}: See Item (3) above.

Fibure B.4 Data transfer processing time (dual sector buffer mode)



Tsrr: (μs) (for read operation in dual sector buffer mode, or for read/write operation in full buffering mode)

Tsrw: (μs) (for write operation in dual sector buffer mode)

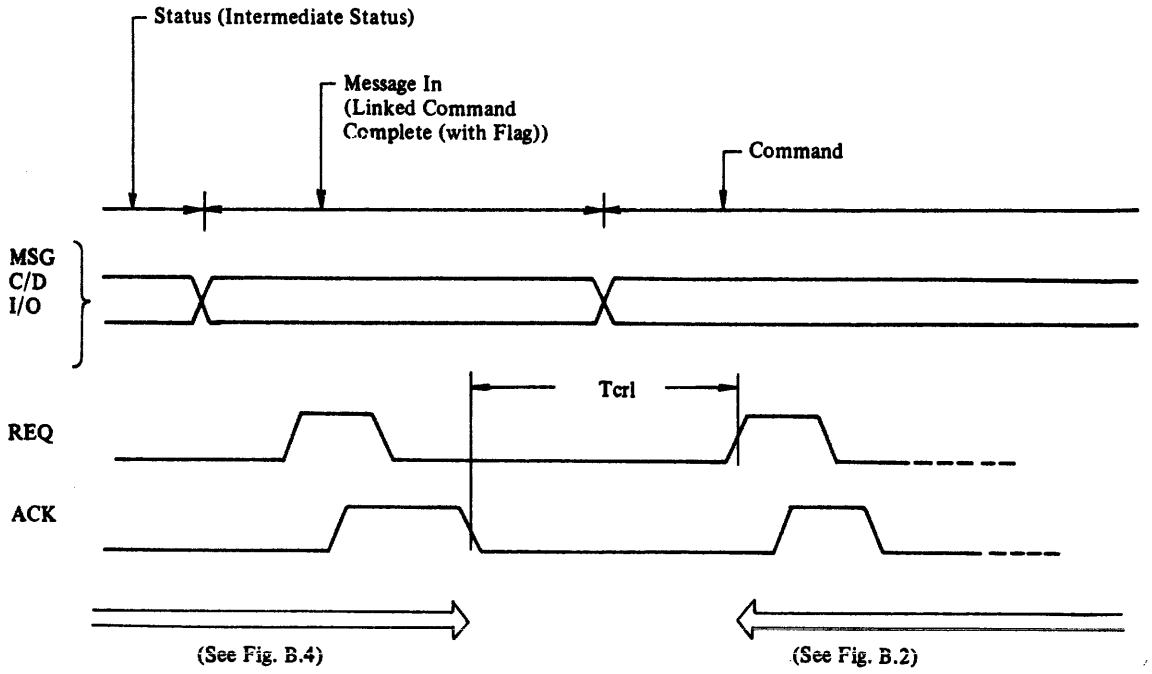
Tsa: (μs)

Ter: (μs)

Tea: (μs)

Tef: (μs)

Figure B.5 Termination sequence processing time



Tcrl: (μs)

Figure B.6 Command link processing time

B.2 Reconnection Timing (Dual sector buffer mode only)

If the dual sector buffer mode is specified, when IDC issues a reconnection request to an INIT upon completion of the positioning to a target block during read/write command, one of the following sources may cause an overrun:

(1) Delayed response by the INIT to the Reselection phase

(2) Processing speed of the INIT in reply to the Identify message issued by IDC

(3) Speed of the INIT in response to a request to fetch data with write commands

This section explains the timing requirements for the above processing to avoid the overrun. Table B.1 lists the commands subject to reconnection upon completion of the positioning.

Table B.1 Commands subject to reconnection on completion of positioning

Group	Commands	Remarks
Read	Read Read Extended Space ID & Read Data Read ID	
Write	Write Write Extended Verify (Data compare mode)	

B.2.1 Read operation in dual sector buffer mode

Figure B.7 is the reconnection timing chart for the read commands.

(1) Description of operation

IDC starts the Reselection phase by Trps before arrival at the target block.

In the Reselection phase, IDC awaits a response from the INIT for a selection timeout delay (Trsw). If the INIT responds to the Reselection phase with Tslr, IDC sends a REQ signal after Trr and notifies the INIT of the LUN to be reconnected. Then, the INIT reconnects the notified LUN within an interval of Tmsg.

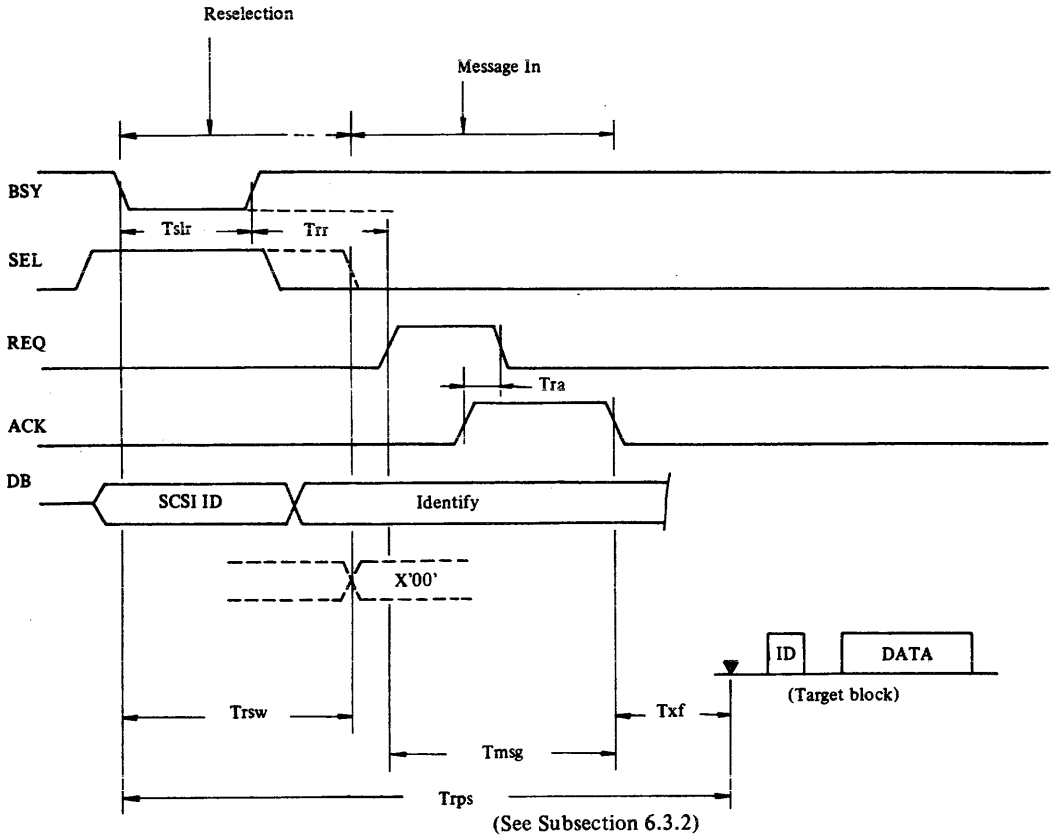
The IDC is informed of successful reconnection by the ACK signal in the Message In phase being negated and starts to process the target block. An interval of Txf is required to process the target block.

(2) Condition for preventing overrun

To prevent overrun, the above processing must be completed before arrival at the target block. The following formula must be satisfied:

$$Trps(MIN) \geqq Tslr(MAX) + Trr(MAX) + Tmsg(MAX) + Txf\ (MAX) + T_{SCT},$$

Where Tslr and Tmsg depend on the processing speed of an INIT.



Note: The broken lines show an withdrawal of reselection.

		T_{SCT}	T_{rsw}	T_{rr}		T_{ra}		T_{xf}	
			TYP	TYP	MAX	TYP	MAX	TYP	MAX
M2333KS M2331KS	256 bytes	138	250,000						
	512 bytes	240							
	1,024 bytes	450							

Unit: μs

Figure B.7 Read commands reconnection (dual sector buffer mode)

B.2.2 Write operation in dual sector buffer mode

Figure B.8 is the reconnection timing chart for the write commands.

(1) Description of operation

The procedures for issuing a request to reconnect from IDC basically conform to those for read commands described above, except that at least one block of data must be prefetched before a target block is encountered.

The IDC requests transfer the data to be writen to a target block after Txr upon completion of the Message In phase (Identify).

Figure B.8 concerns write operations on a data field. In this chart, the time required to transfer data on SCSI for one block is denoted as Tprf.

(2) Conditions for preventing overruns

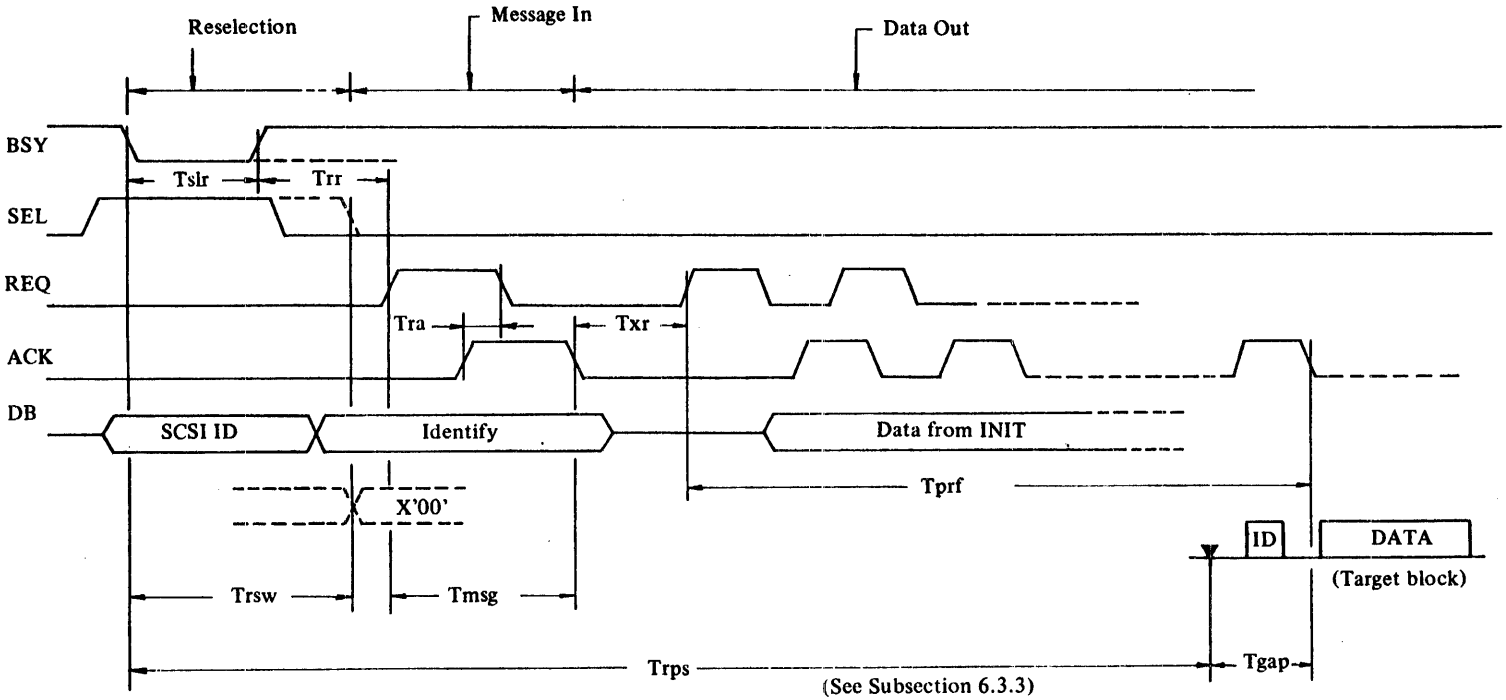
To prevent overrun, reconnection and at least one block of data transfer must be completed before a target block is encountered. The following formulas must be satisfied:

$$Trps\ (MIN) \geqq Tslr\ (MAX) + Trr\ (MAX) + Tmsg\ (MAX) + Txr(MAX) + T_{SCT},$$

and

$$Trps\ (MIN) + Tgap\ (MIN) \geqq Tslr\ (MAX) + Trr\ (MAX) + Tmsg\ (MAX) + Txr\ (MAX) + Tprf\ (MAX),$$

Where Tslr and Tmsg depend on the processing speed of the INIT and Tprf is determined by the data transfer speed in SCSI.



Note: Broken lines indicate withdrawal of reselection.

		T_{SCT}	T_{rsw}	T_{gap}	T_{rr}		T_{ra}		T_{xr}	
			TYP	MIN	TYP	MAX	TYP	MAX	TYP	MAX
M2333KS M2331KS	256 bytes	138	250,000							
	512 bytes	240								
	1,024 bytes	450								

m: Interleaving factor (m=1 if no interleaving is used.) Unit: μs

Figure B.8 Write commands reconnection (dual sector buffer mode)

B.3 Data Transfer without Disconnection

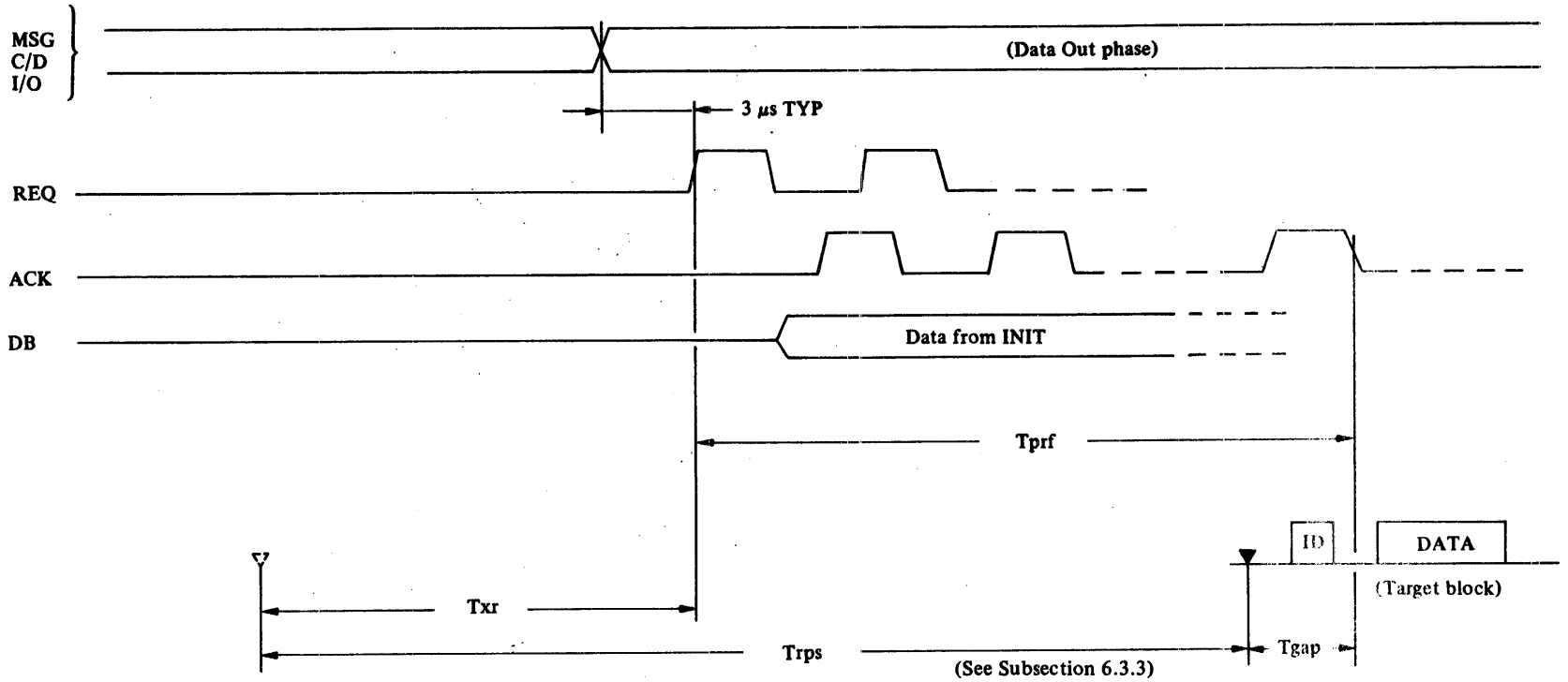
When the disconnection function of the SCSI is not used, the IDC executes commands with connecting the SCSI between completion of Selection phase and repording the Command Complete message. Especially in case of the read/write operation for the disk drive, the IDC is connected to the SCSI during the positioning operation. After completion of the positioning to the target data block, the IDC executes the data transfer (Data In/Out phase) on the SCSI.

In case of read operation, the IDC stores the data into the data buffer then sends that data to the SCSI.

In case of write operation by using the dual sector buffer mode, it is necessary to complete the data prefetching of at least one block length of data before the target block is encountered; this case is similar to the reconnection processing described above. Figure B.9 shows the start timing of the data prefetching in the write operation. To prevent an overrun at the target data block, the following formula must be satisfied.

$$\text{Trps (MIN)} + \text{Tgap (MIN)} \geqq \text{Txr (MAX)} + \text{Tprf (MAX)},$$

Where Tprf is the necessary time for the data transfer of one block length of data on the SCSI, and Trps is the same value as that for the reconnection processing. See Subsection 6.3.3 for value of Trps.



		T_{gap}	T_{xr}	
		MIN	TYP	MAX
M2333KS M2331KS	256 bytes			
	512 bytes			
	1,024 bytes			

m: Interleave factor (m = 1: without interleave) Unit: μs

Figure B.9 Data prefetch without Disconnection (write operation in dual sector buffer mode)

APPENDIX C OPTIONS

C.1 Options for M2331KS/M2333KS

Table C.1 shows the optional parts provided to connect M1053BD to M2331KS or M2333KS Micro-Disk Drive.

Table C.1 Options for M1053BD-M2331KS/M2333KS

	Name	Part Number	Remarks
1-1	Mounting frame	M1053A11	
2-1	Fan unit	B03B-4760-E007A	+24 VDC
2-2	Fan unit	B03B-4760-E008A	+24 VDC
3-1	Power supply unit	B14L-5105-0178A#A2	100/115/120/220/240 VAC
4-1	Power cable	B660-1995-T041A	for drive and fan unit
4-2	Power cable	B660-1995-T060A	for M1053BD
5-1	B cable	B660-1065-T123A	26-pin flat cable
6-1	A cable	B660-1065-T006A	for 1-drive connection
6-2	A cable	B660-1065-T020A	for 2-drive connection
6-3	A cable	B660-1065-T030A	for 3-drive connection
6-4	A cable	B660-1065-T040A	for 4-drive connection

C.1.1 Mounting frame

- M1053A11

  This is special frame to mount the M1053BD on the M2331KS or M2333KS. M1053A11 contains the mounting frame and interface cables (A and B cables each) to connect the M1053BD and the drive on which the M1053BD is mounted. Refer to Subsection 2.2.2 for details.

C.1.2 Fan unit

This is for cooling the M1053BD and the drive when the M1053BD is mounted on the drive using the M1053A11. For the details, Refer to the following manual.

M2331KS/M2333KS MICRO-DISK DRIVES OEM MANUAL

- B03B-4760-E007A

  When this fan unit is mounted, the height of the unit is 162 mm (See Figure 2.10), and industrial standard connector, 26-conductor connector consisting of two rows of 13 female contacts with adjacent contacts 100 mils apart, is available as for B cable.

- B03B-4760-E008A

When this fan unit is mounted, the height of the unit is 154 mm (See Figure 2.10). But, use the optional B cable (B660-1065-T123A) or recommended connector (FCN-747J026-AU/O, see Table 2.2) for the B cable on the IDC side.

C.1.3 Power supply unit

- B14L-5105-0178A#A2

This power supply unit can supply the power to one M2331KS or M2333KS, one M1053BD and the fan unit. Figure C.1 shows the connection between the power supply unit and these devices. For detailed specification of the power supply unit, refer to the following manual.

M2331KS/M2333KS MICRO-DISK DRIVES OEM MANUAL

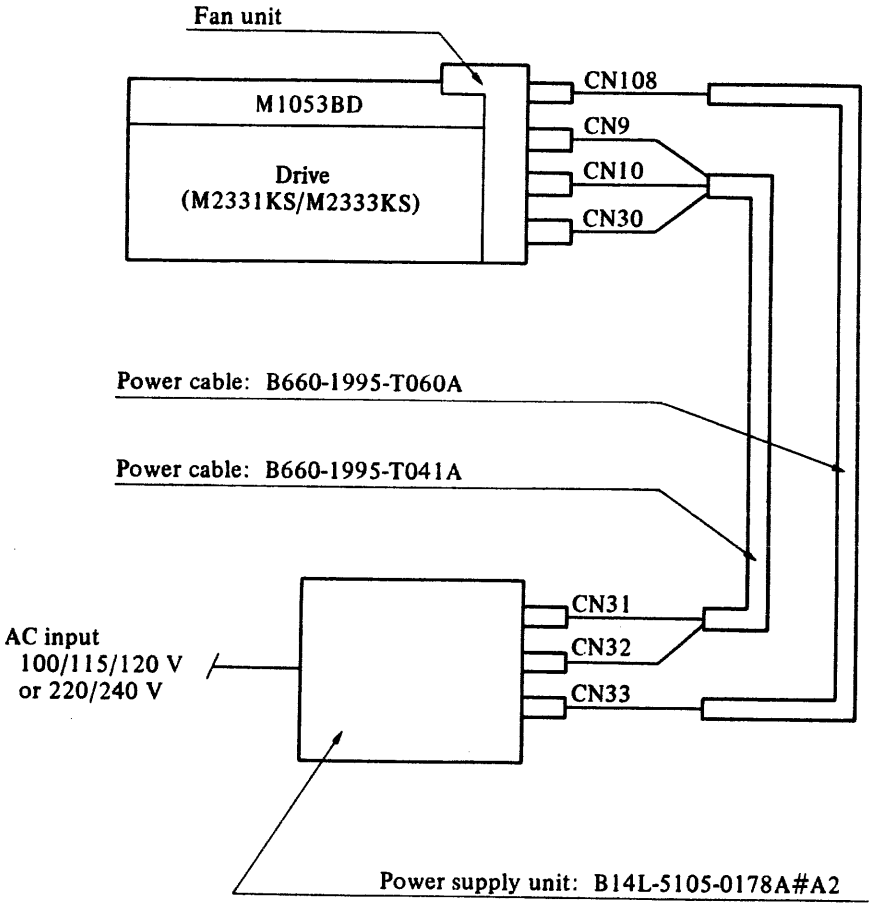


Figure C.1 Power supply unit connection

C.1.4 Cables

(1) Power cable for drive and fan unit

Figure C.2 shows the power cable for the drive (M2331KS or M2333KS) and the fan unit. Its length is 1.5 m or 15 cm.

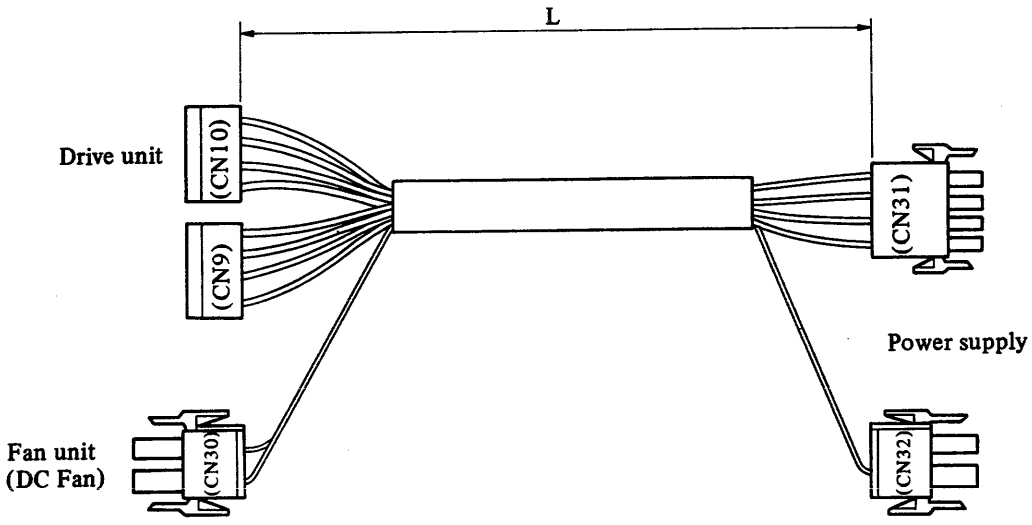


Figure C.2 Power cable B660-1995-T041A (for drive and fan unit)

(2) Power cable for M1053BD

Figure C.3 shows the power cable for M1053BD. Its length is 1.5 m or 15 cm.

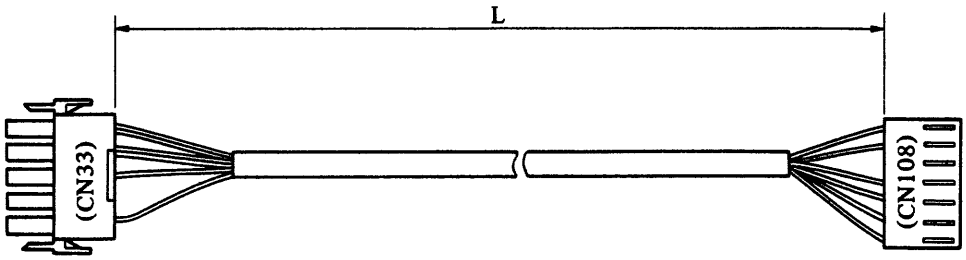


Figure C.3 Power cable B660-1995-T060A (for M1053BD)

(3) B cable (drive interface cable)

Maximum length of B cable is 15 m.

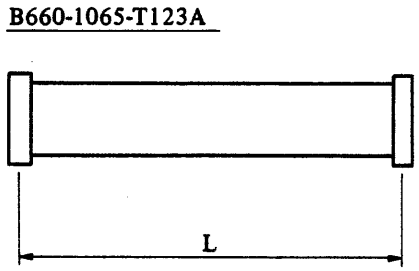
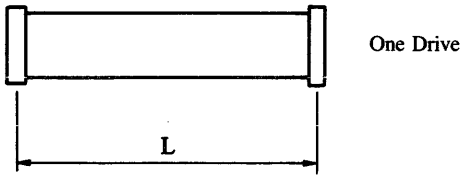


Figure C.4 B cable (drive interface cable)

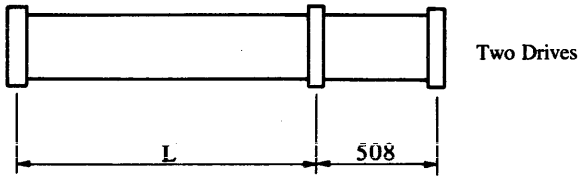
(4) A cable (drive interface cable)

Maximum length of A cable is 15 m.

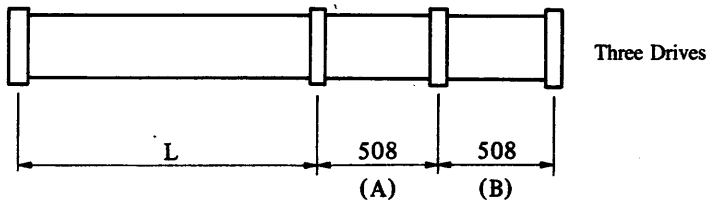
B660-1065-T006A



B660-1865-T020A



B660-1865-T030A



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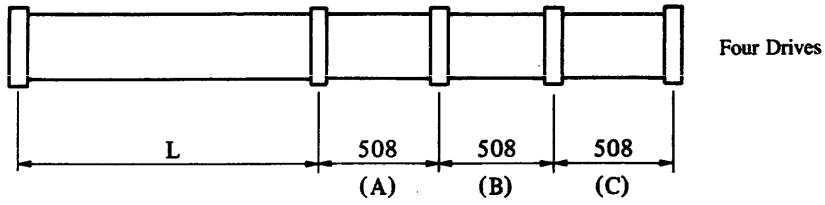

Figure C.5 A cables (drive interface cable)