SYS68K / WFC-1

USER'S MANUAL

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N O T E

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Table of Contents

Table of Contents contd.

Table of Contents contd.

List of Figures

List of Tables

1.Ø General Information

The SYS68K/WFC-1 is a high performance VMEbus interface controller board to control 5 1/4" Floppy and Winchester drives.

The SYS68K/WFC-1 board has been developed to serve as a controller board for high speed data transfers to and from 5 1/4" Floppy and Winchester drives via a 1 KByte FIFO buffer. The board can communicate with a DMA controller to provide maximum bus transfer speed and is able to generate interrupts for complete operation, error operation and data request.

The VMEbus allows easy system design with extended I/O, RAM, CPU, ROM, and DMA cards.

This manual provides a general operating description of the SYS68K/WFC-1 hardware. Follow manufacturer's installation instructions for use and trouble shooting.

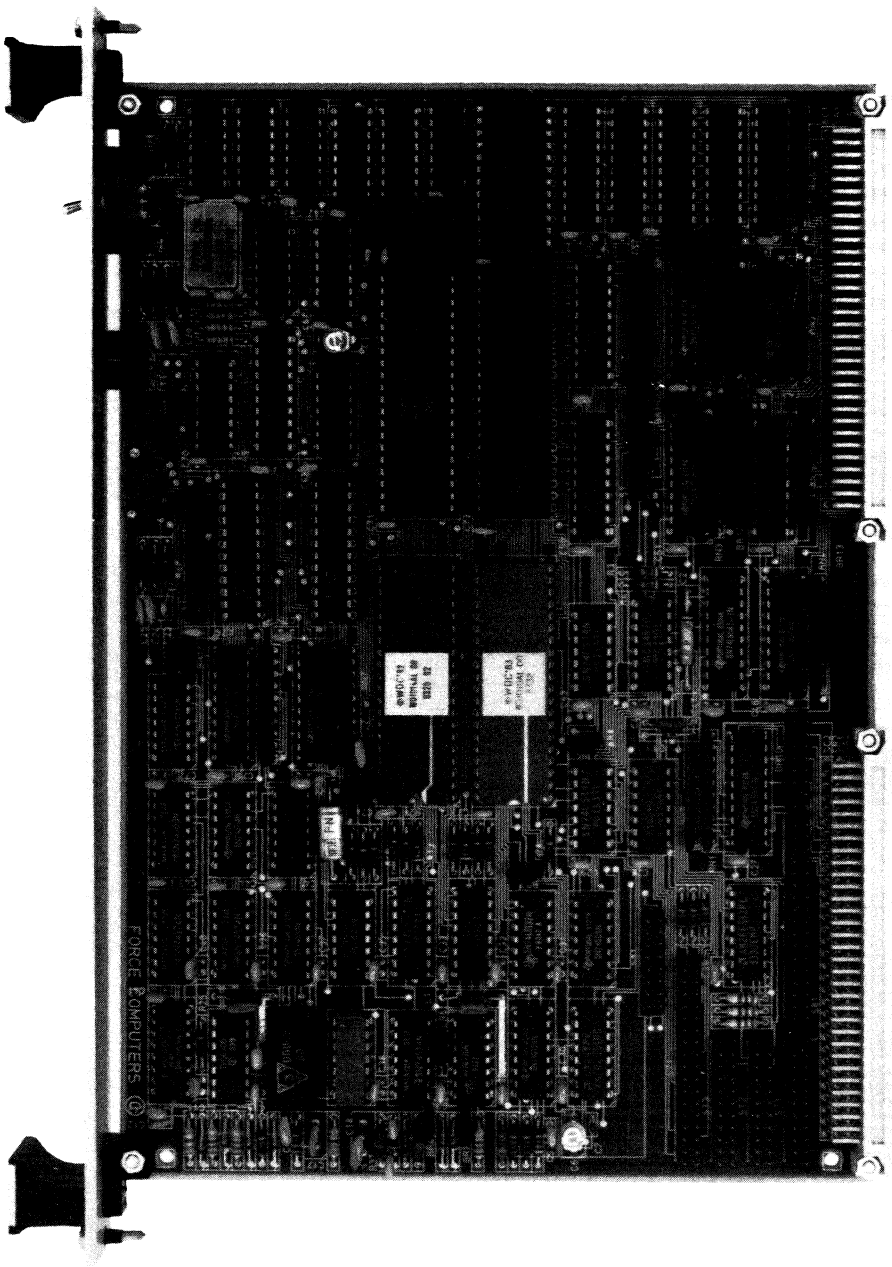


FIG. 1 PHOTO OF BOARD

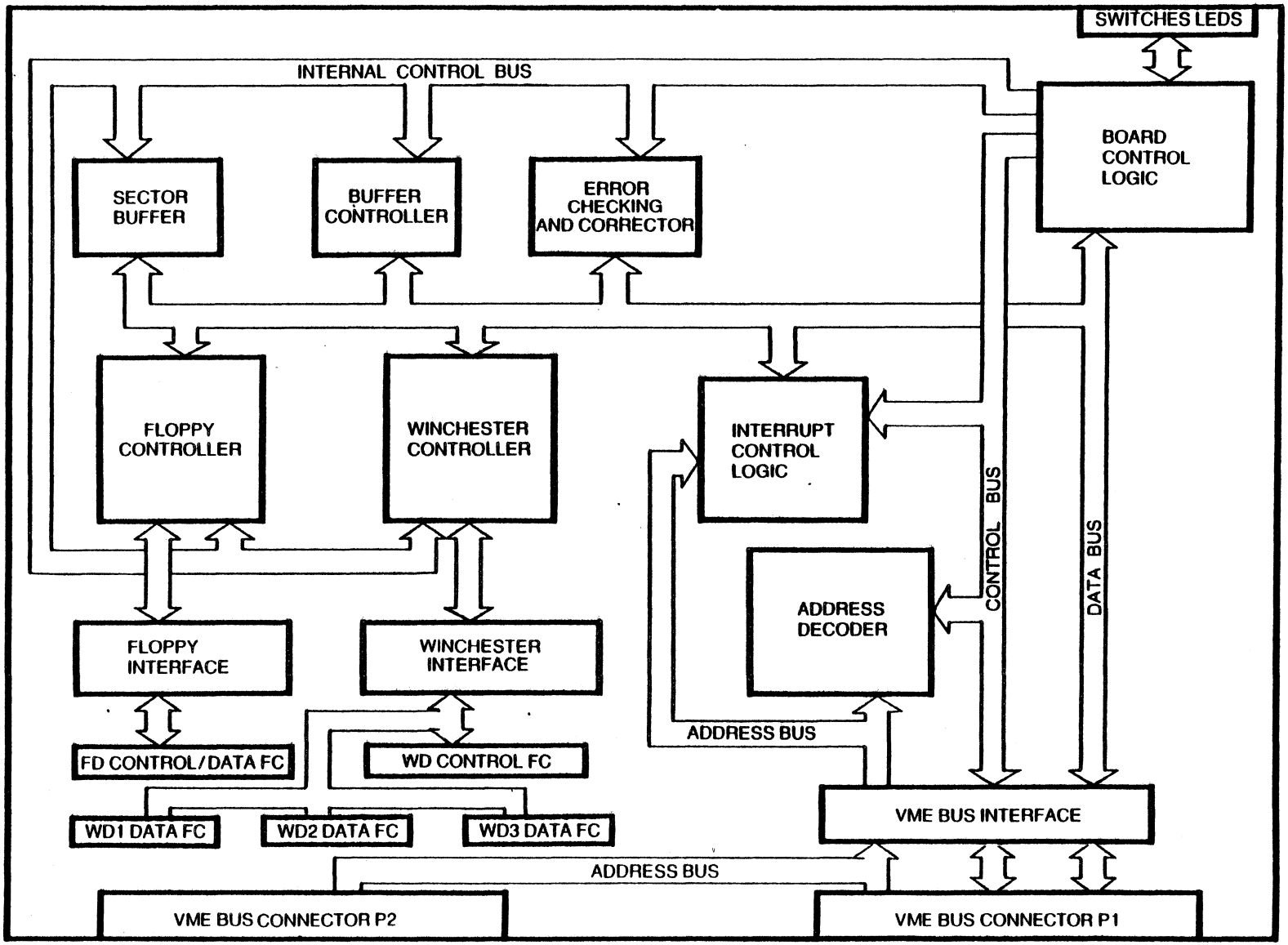


FIG. 2 BOARD BLOCK DIAGRAM SYS68K/WFC-1

2.0 General Operation

The SYS68K/WFC-1 consists of a set of devices specifically designed for control of Winchester and Floppy disk drives. The heart of the control logic is the Control Processor Buffer Manager (WD1015) that manages the on-board static RAM sector buffer (2048-word by 8-bit). All bytes of data written to and read from disk are first stored on this sector buffer. When the buffer is full, the data is transferred, on command, to its intended destination.

The WD1015, besides controlling the data flow between host, sector buffer, and disk controllers, also translates the host Winchester command format to Floppy disk format when addressing the Floppy Disk Controller (WD2797). This permits the host to maintain a single command format (Winchester) while in effect controlling two different disk command formats (Winchester vs. Floppy). This is possible, since the SDH register is used to select either type of drive.

The WD1015 maintains the current copies of necessary host command data in the task files; a set of register physically located in the Winchester Disk Control device (WD1010) and the Error Detection and Support logic device (WD1014).

The WD1010 is the link between the host processor (via sector buffer) and the Winchester disk drives. During transfer of data from the host to the WD1010, the WD1014 computes a 4-byte ECC which is appended to the end of the data being transferred to the WD1010 and recorded on the disk. During data transfers from WD1010 to the host (via the sector buffer), the WD1015 uses the ECC syndrome to validate the data. Retries and corrections are attempted automatically in case of corrupted data.

The WD1015 performs error correction in conjunction with the WD1014 on data transferred to the disk. While the WD1015 controls the operation of the on-board error-correction logic, the WD1014 generates and checks the Error Correction Code (ECC) if SDH bit 7 = 0. Thus the WD1014 also provides the WD1015 with its real-time control capability.

If CRC format Winchester disks are used, CRC is selected by the WD1010 by setting SDH7 = 0. CRC for the floppy disk is performed by the WD2729, a device that furnishes all control functions for floppy disk drives, including necessary data seperation and write precompensation. SDH7 must be set to zero for floppy disk operation.

2.1 Features of the SYS68K/WFC-1

- Fully VMEbus compatible
- Jumper selectable base address with address modifier
- Generation at two different interrupts
- Jumper selectable interrupt level
- Software programmable interrupt vectors
- Three VMEbus options (A31:D16), (A23:D16), (A15:D16) jumper selectable
- User selectable 5.25" Winchester or Floppy operation
- Controls up to 3 Winchester ST506 Interface and up to 4 Floppy drives SA450 compatible
- On-board data seperation circuitry
- On-board write precompensation for floppy and hard disks
- On-board sector buffer supports up to 1 KByte sectors
- Programmable sector sizes - 128, 256, 512, or 1024 bytes
- Automatic track formatting on hard and floppy disks
- Multiple sector operations on all disks
- Data rates up to 5 Mbits/sec on hard disk
- Single burst error correction up to 5 bits on hard disk data
- CRC generation/verification for data and all I.D. fields
- Automatic retries on all errors with simulated completion
- ECC diagnostic commands included (READLONG & WRITELONG)
- Internal diagnostics
- 16 different stepping rates for both hard and floppy drives

3.Ø Hardware Overview

3.1 Global Base Address Selection

The SYS68K/WFC-1 controller board contains a set of jumper fields for the global base address selection.

This board contains also two jumper fields, BR8 and BR9, for the VMEbus options (A15-D16), (A23-D16) and (A31-D16), (see Fig. 3).

The following table shows the connection of BR8 and BR9 for these options :

BR8 CONNECTIONS	BR9 CONNECTIONS	OPTIONS
1 to 2	1 to 2	A15:D16
1 to 2	2 to 3	A23:D16
2 to 3	2 to 3	A32:D16

No other combination is allowed, as it may cause errors in the system.

The address signals A31-A4 are used for the global base address selection. Fig.3 shows the jumper location and the default setting during manufacturing ($BØ1ØØØ) for the A23:D16 option. For all of these jumper fields, jumper in means Ø for the corresponding signal and jumper out means 1 for the corresponding signal. Fig. 4 shows the physical location of these jumpers on the SYS68K/WFC-1 board.

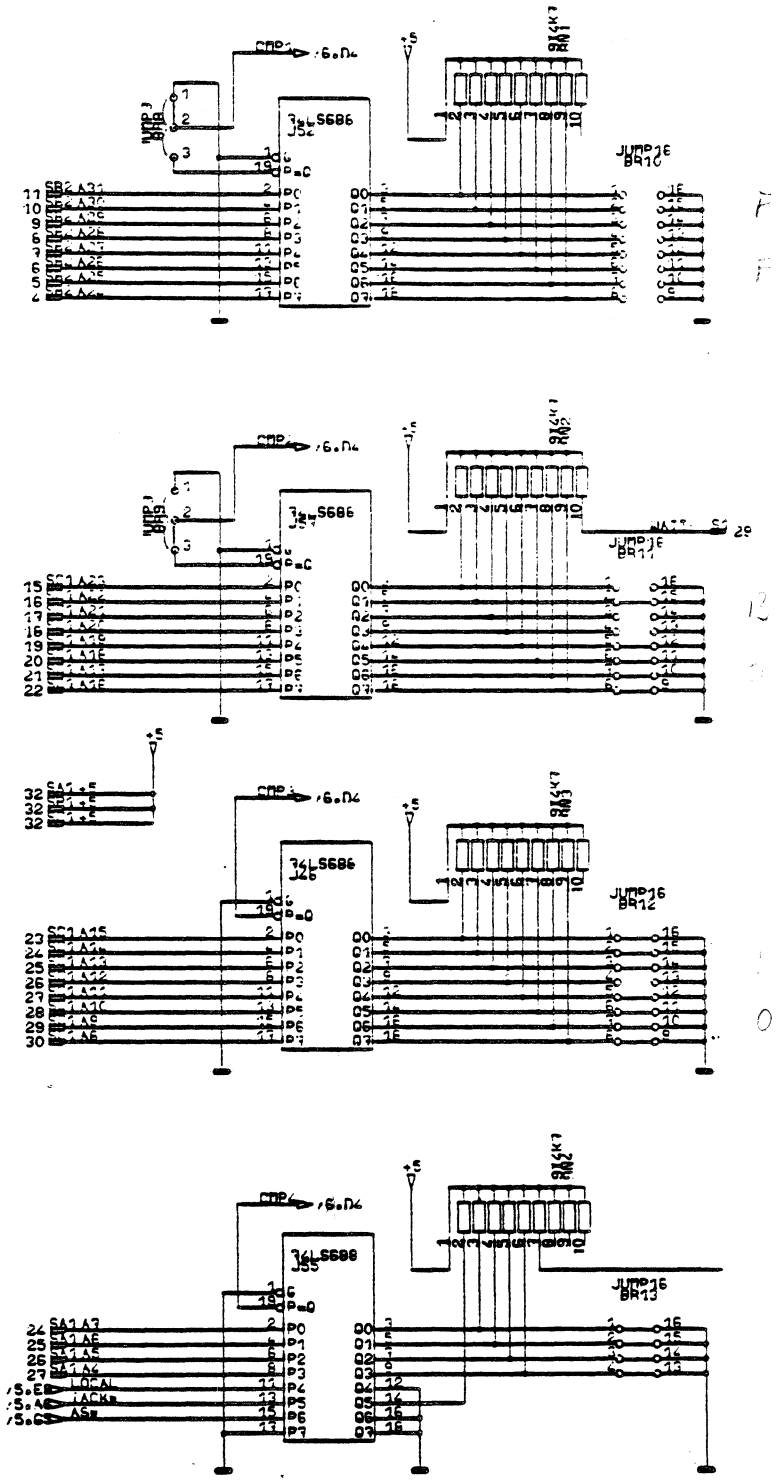


FIG. 3 BASE ADDRESS JUMPER FIELDS

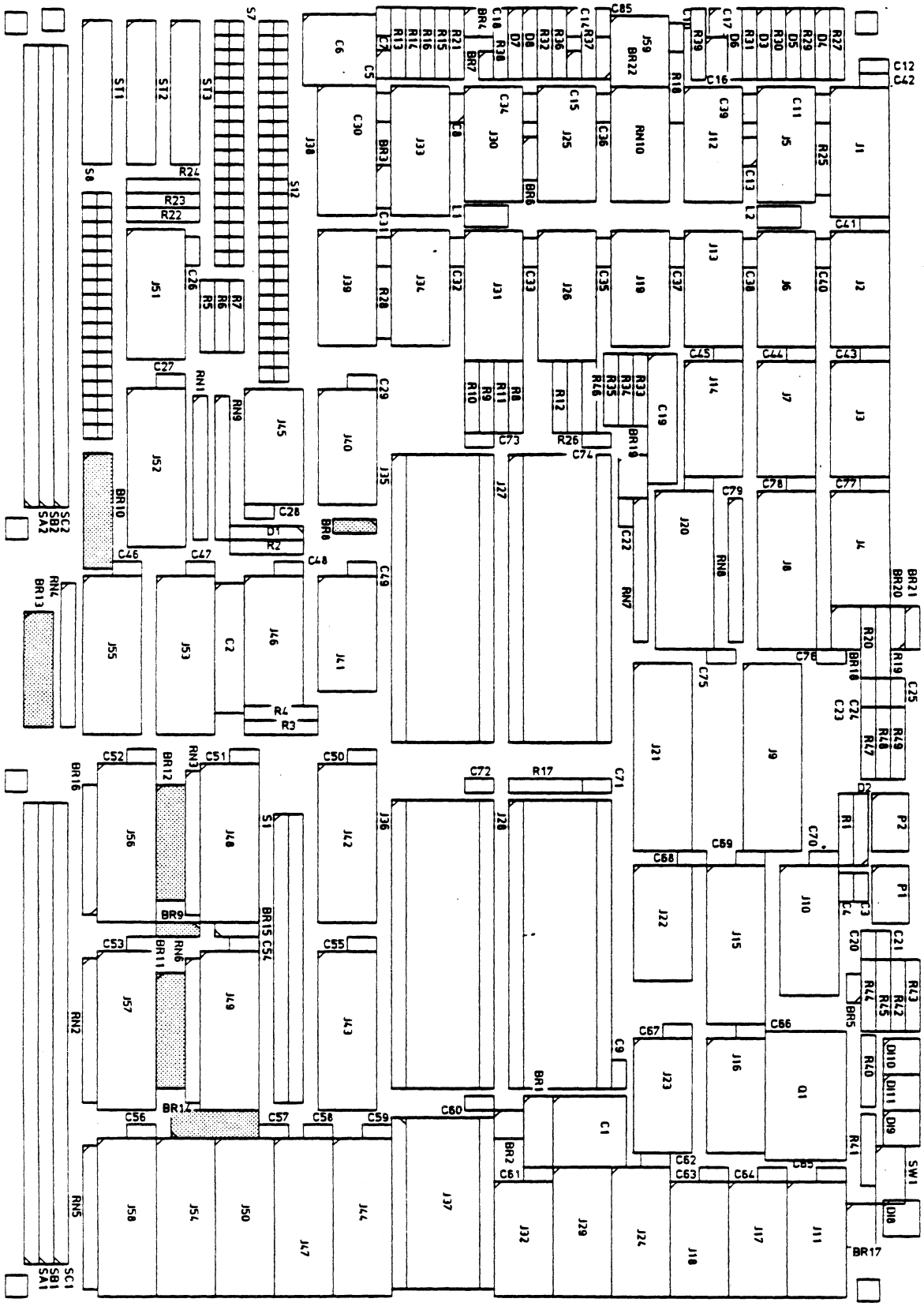


FIG. 4 LOCATION OF THE BASE ADDRESS JUMPER FIELDS

3.2 Address Modifier Decoding

The address modifier (AM) signals of the VMEbus may be used for additional decoding in parallel to the address signals.

Table 1 lists the combination of the AM signals and the relevant functions.

The BR15 may be jumpered so that these signals are not decoded (don't care). If BR15 pin 1 is connected to pin 2, then the AM decoding is enabled. If BR15 pin 2 is connected to pin 3, then the AM decoding is disabled.

The BR14 jumper field includes the AM code and Fig. 5 shows an example for supervisor data decoding. Fig. 4 shows the physical location of the BR14, BR15 jumper field on the SYS68K/WFC-1 board.

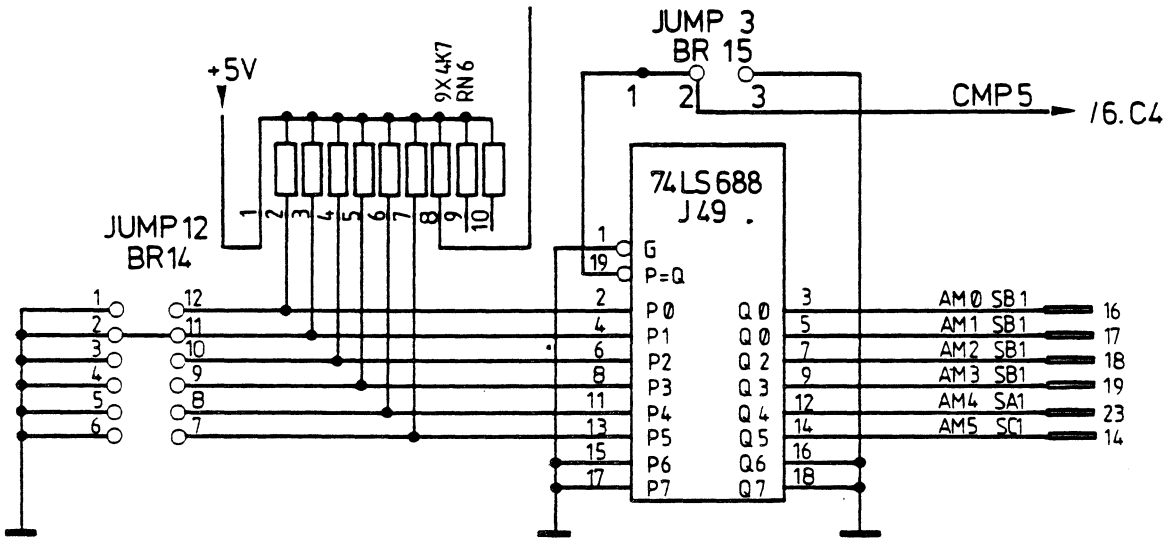


FIG. 5 AM JUMPER FIELDS
EXAMPLE FOR STANDARD SUPERVISORY DATA ACCESS

3.3 Interrupt Jumpering

The SYS68K/WFC-1 controller board can generate two different interrupts. The first interrupt, IR1, is for operation complete and error operation.

The second interrupt, IR2, is for data request by read, write and format operations, if the controller board needs data or has to send data.

Both interrupts can be enabled and disabled seperately and can be jumpered on each interrupt level on the VMEbus.

IR1 can be enabled via BR20 through connection pin 1 to 2 and IR2 via BR21 through connection pin 2 to 3.

If BR20 pin 2 is connected to pin 3, then the operation complete interrupt is disabled. If BR21 pin 1 is connected to pin 2, then the data request interrupt is disabled.

The interrupt request level can be selected via jumper field BR16.

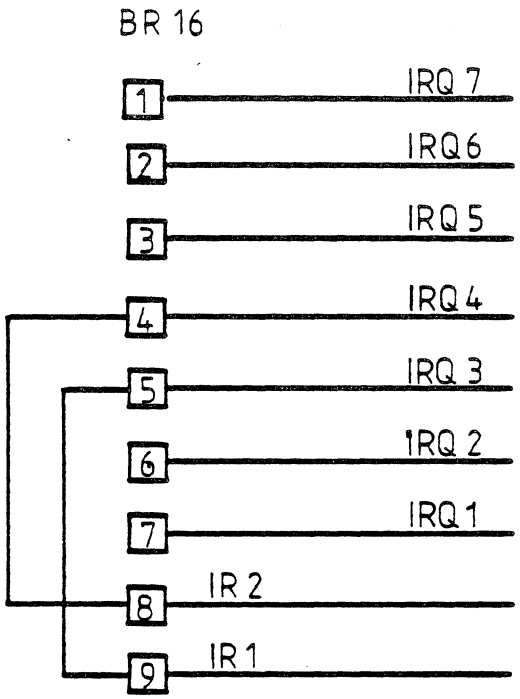
Fig. 6 shows the jumper fields and an example for enabled interrupts for a connection to the interrupt level 3 for IR1 and to the interrupt request level 4 for IR2. BR18 and BR19 must be selected to the corresponding level (see Fig. 6). Fig. 7 shows the physical location of these jumpers on the controller board.

The interrupt default setting by manufacturing is disabled and only programmed I/O is allowed.

ILEXADECIMAL CODE	ADDRESS MODIFIER 5	4	3	2	1	0	FUNCTION	DEFINED BY
3F	H	H	H	H	H	H	Standard Supervisory Ascending Access	VMEbus Spec.
3E	H	H	H	H	H	L	Standard Supervisory Program Access	VMEbus Spec.
3D	H	H	H	H	L	H	Standard Supervisory Data Access	VMEbus Spec.
3C	H	H	H	H	L	L	Undefined	Reserved
3B	H	H	H	L	H	H	Standard Non-Privileged Ascending Access	VMEbus Spec.
3A	H	H	H	L	H	L	Standard Non-Privileged Program Access	VMEbus Spec.
39	H	H	H	L	L	H	Standard Non-Privileged Data Access	VMEbus Spec.
38	H	H	H	L	L	L	Undefined	Reserved
30 – 37	H	H	L	X	X	X	Undefined	Reserved
2F	H	L	H	H	H	H	Undefined	Reserved
2E	H	L	H	H	H	L	Undefined	Reserved
2D	H	L	H	H	L	H	Short Supervisory I/O Access	VMEbus Spec.
2C	H	L	H	H	L	L	Undefined	Reserved
2B	H	L	H	L	H	H	Undefined	Reserved
2A	H	L	H	L	H	L	Undefined	Reserved
29	H	L	H	L	L	H	Short Non-Privileged I/O Access	VMEbus Spec.
28	H	L	H	L	L	L	Undefined	Reserved
20 – 27	H	L	L	X	X	X	Undefined	Reserved
10 – 1F	L	H	X	X	X	X	Undefined	User
OF	L	L	H	H	H	H	Extended Supervisory Ascending Access	VMEbus Spec.
OE	L	L	H	H	H	L	Extended Supervisory Program Access	VMEbus Spec.
OD	L	L	H	H	L	H	Extended Supervisory Data Access	VMEbus Spec.
OC	L	L	H	H	L	L	Undefined	Reserved
OB	L	L	H	L	H	H	Extended Non-Privileged Ascending Access	VMEbus Spec.
OA	L	L	H	L	H	L	Extended Non-Privileged Program Access	VMEbus Spec.
09	L	L	H	L	L	H	Extended Non-Privileged Data Access	VMEbus Spec.
08	L	L	H	L	L	L	Undefined	Reserved
00 – 07	L	L	L	X	x	X	Undefined	Reserved

Table 1 Address Modifier Codes

The AM codes are valid if BR15 is connected from Pin 1 to Pin 2.



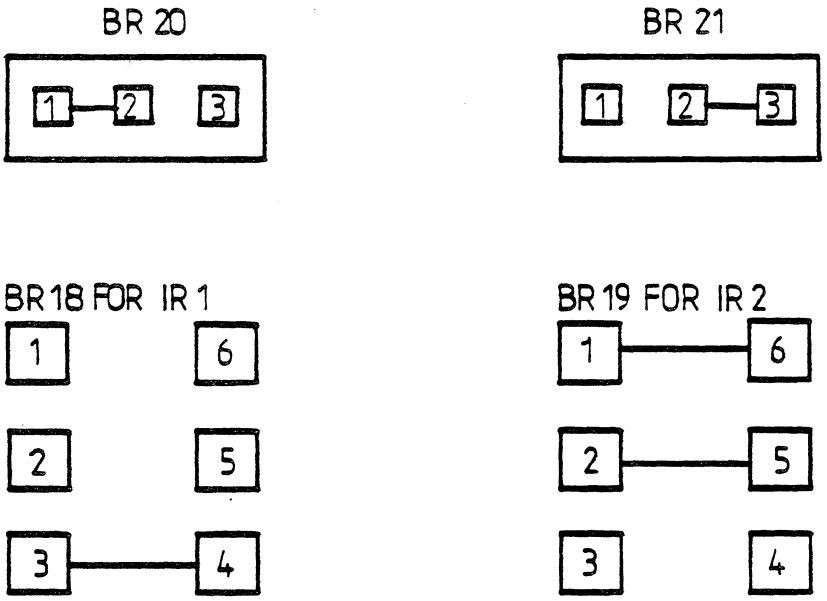


FIG. 6 INTERRUPT JUMPER FIELDS

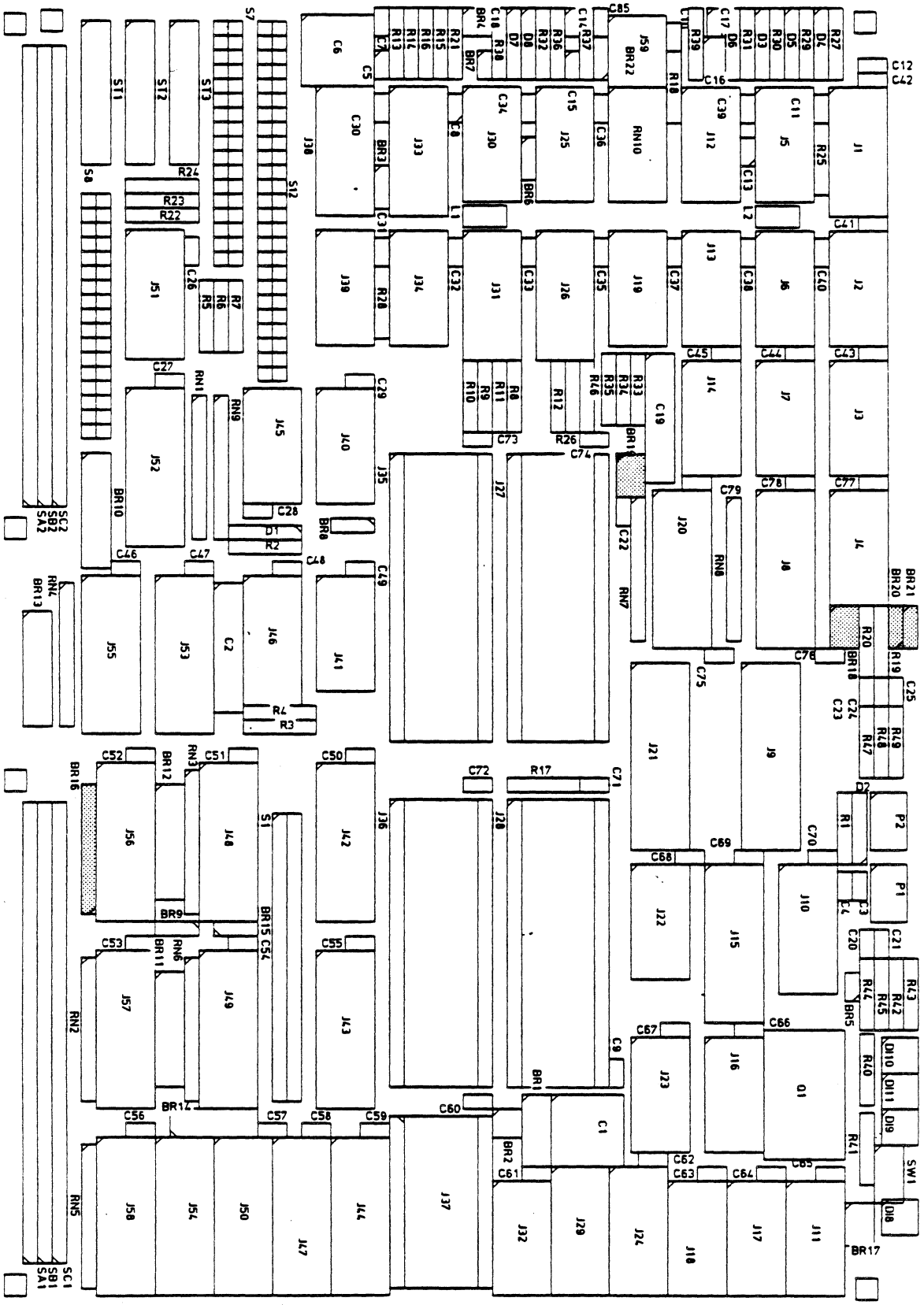


FIG. 7 LOCATION OF THE INTERRUPT JUMPER FIELDS

3.4 Connectors Organisation

The SYS68K/WFC-1 has seven connectors for user applications :

- Two VMEbus connectors SX1 and SX2

- S7 Winchester drive control connector

- S8 Floppy drive control connector

- ST1, ST2, ST3 Winchester high speed data connectors

  ST1 = LUN Ø

  ST2 = LUN 1

  ST3 = LUN 2

The drive control cables are daisy-chained to each of the three Winchester drives. The three drive data connectors carry differential signals and are radially connected.

The following diagram shows the physical location of the connectors on the SYS68K/WFC-1 board.

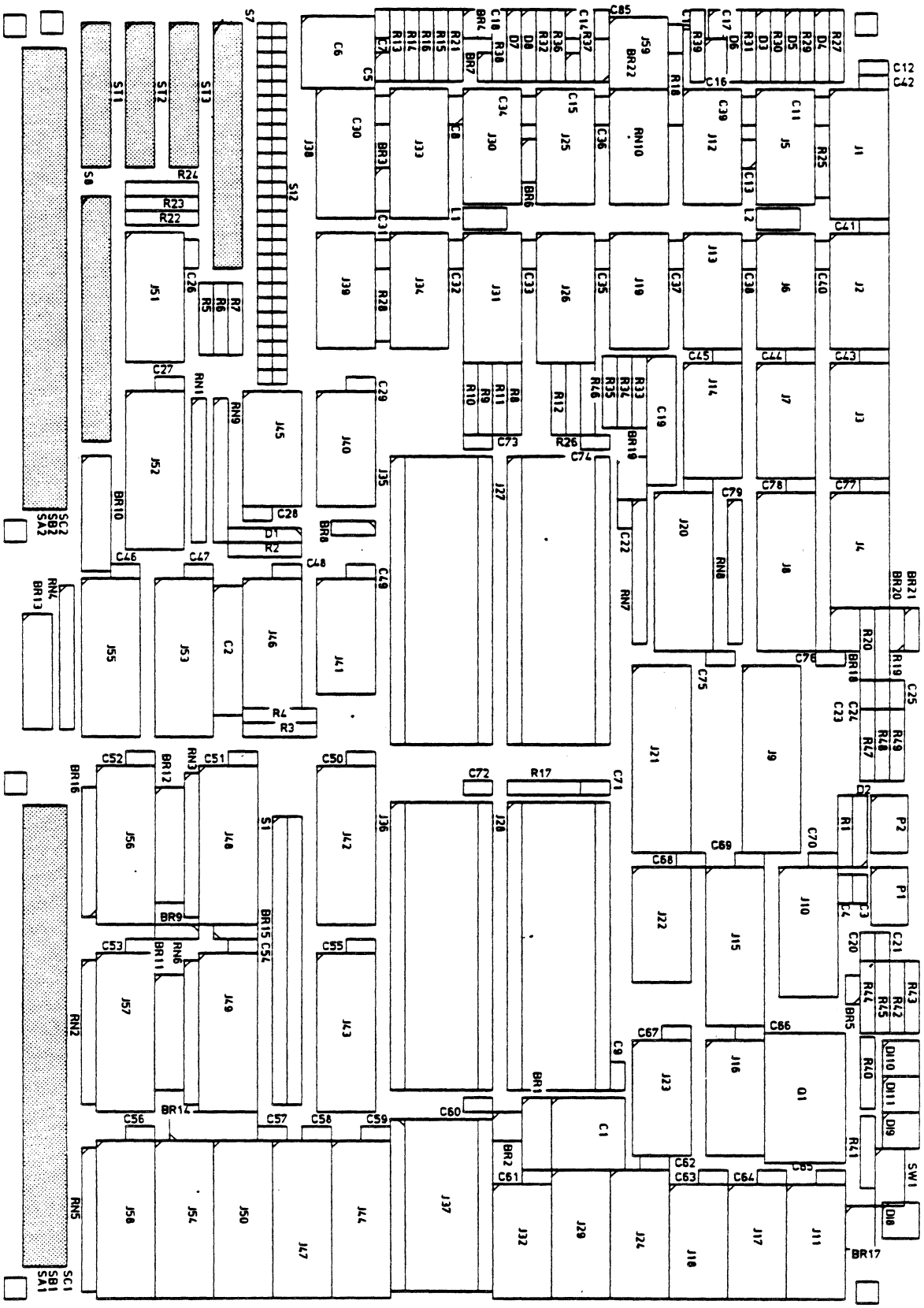


FIG. 8 CONNECTORS LOCATION DIAGRAM

3.5 Winchester Drive Control Signals

The Winchester Drive Control connector S7 is a relatively low-speed bus, daisy chained to each of the Winchester drives in the system. To properly terminate the open collector outputs from the SYS68K/WFC-1, the last drive in the daisy chain should have a 220/330OHm line termination resistor pack installed. All other drives shoud have no termination. Drive control signals are as follows :

RWC* When the Reduce Write Current (RWC*) line is activated with write gate, a lower write current is used to compensate for greater bit-packing density on the inner cylinders. The RWC* line is activated when the cylinder number is greater than or equal to four times the contents of the write precomp register. This output is valid only during write and format commands.

WG* The Write Gate* signal enables the disk write data circuitry.

SC* Seek Complete* line informs the SYS68K/WFC-1 that the head of the selected drive has reached the desired cylinder and has stabilized. Since Seek Complete* is not checked after a seek command, overlapped seeks are allowed.

TRØØØ* Track ØØØ* indicates that the R/W heads are positioned on the outermost cylinder. This line is sampled before each step pulse is issued.

WF* Write Fault* informs the SYS68K/WFC-1 that some fault has occurred on the selected drive. The SYS68K/WFC-1 will not execute commands when this signal is true.

HS2-HSØ* Head Select lines (HS2-HSØ)* are used by the SYS68K/WFC-1 to select a specific R/W head on the selected Winchester drive.

IND* Index* is used to indicate the index point for synchronization during formatting and as a time-out mechanism for retries. This signal ahould pulse once every rotation of the disk.

RDY* Ready* informs the SYS68K/WFC-1 that the desired drive is selected and that its motor is up to speed. The SYS68K/WFC-1 will not execute commands unless this line is true.

STEP* Step* is pulsed once for every cylinder to be stepped. The direction of the step will be determined by the direction line. The Step* pulse period is determined by the internal Winchester stepping rate register during implied seek operations, or explicitly during seek commands. During auto-restore, the step pulse period is determined by the seek complete time from the drive.

DS1-DS3* These three Drive Select* lines (DS1-DS3) are used to select one of three possible drives.

DIRIN* Direction-In* determines the direction of motion of the R/W head when the step line is pulsed. A high on this line defines the direction as OUT, and a low defines the direction as IN.

3.6 5.25" Winchester 34-Pin Drive Control Connector

This drive control connector S7 is a 34-pin vertical header on Ø.1Ø-inch centers. Cabling should be flat ribbon or twisted-pair cable less than 1Ø feet long. The cable pinouts are given in Table 2.

Table 2. Winchester Drive Control Connector Pin Description

Signal Ground	Signal Pin	I/O	Signal Name
1	2	O	RWC*
3	4	O	Head Select 2*
5	6	O	Write Gate*
7	8	I	Seek Complete*
9	1Ø	I	TRØØØ*
11	12	I	Write Fault*
13	14	O	Head Select Ø*
15	16		NC
17	18	O	Head Select 1*
19	2Ø	I	Index*
21	22	I	Ready*
23	24	O	Step*
25	26	O	Drive Select 1*
27	28	O	Drive Select 2*
29	3Ø	O	Drive Select 3*
31	32		NC
33	34	O	Direction-In*

3.7 Winchester Drive Data Connector

Three data connectors (ST1-ST3) allow data to pass between the SYS68K/WFC-1 and each Winchester disk drive. All lines associated with the transfer of data between a drive and the SYS68K/WFC-1 are differential in nature and may not be multiplexed. The three Winchester drive data connectors are 20-pin vertical headers on 0.10" centers. Cabling should be either flat ribbon or twisted-pair cables, less that 10 feet long. Cable pinouts are given in Table 3.

Table 3. Winchester Drive Data Connector Pin Description

Signal Ground	Signal Pin	I/O	Signal Name
2	1		NC
4	3		NC
6	5		NC
8	7		NC
	9		NC
	10		NC
11			GND
12			GND
	13	O	MFM Write Data
	14	O	MFM Write Data*
15			GND
16			GND
	17	I	MFM Read Data
	18	I	MFM Read Data*
19			GND
20			GND

3.8 Floppy Drive Signals

The Floppy Drive Control Connector S8 is a relatively low-speed bus, daisy chained to each of the floppy drives in the system. To properly terminate each TTL-level output signal from the SYS68K/WFC-1, the last drive in the daisy chain should have line terminations as specified by the drive manufacturer. The other drives should not have any terminations. Drive control signals for the floppy disks are functionally similar to those for the hard disks, except that all data is transferred via one connector instead of the seperate connectors used for the Winchester drives. Floppy drive signals are as follows :

IND* The index* line contains a reference index pulse once every disk rotation to indicate the beginning of a track.

DS3-DSØ* These four Drive Select* lines (DS3-DSØ) are used to select one of four possible drives.

MO* The Motor-On* line is used to directly control the dc spindle motor of the floppy drive. If Motor-On Mode (MOM) = Ø (user selectable jumper option), then a 4Ø nsec delay occurs, otherwise a one-second delay occurs after Motor-On and before any reading or writing is attempted. If the floppy drive is not accessed for ~3 seconds, the motor is turned off by the WD1Ø15. Also, the drives supported must be configured so that the R/W heads are loaded when the motor is turned on. This is usually available as an option on most drives.

DIRIN* The Direction-In* line determines the direction of motion of the R/W head when the step line is pulsed. A high on this line defines the direction as OUT, and a low defines the direction as IN.

STEP* The Step* line is pulsed once for each cylinder to be stepped. The direction of the step will be determined by the direction line. The step pulse period is determined by the internal floppy stepping rate register during implied seek operations, auto restore, or explicitly during seek and restore commands. During any restore operation, the stepping rate period is limited to 8ms minimum.

WD* The Write Data* interface line provides data to be written on the disk. This line is enabled by write gate being active.

WG* The Write Gate* output signals enable disk write data circuitry.

TRØØØ* TRØØØ* indicates that the R/W heads are positioned on the outermost cylinder. This line is sampled before each step is issued.

WP* The Write Protect* interface signal provided by the drive indicates to the SYS68K/WFC-1 that a write-protected disk is installed. When write protect is active, no data can be written to the disk by the SYS68K/WFC-1.

RD* The Read Data* line provides the "raw data" (clock and data together) as detected by the drive logic.

SS* Selects Side* of floppy disk to be written or read.

3.9 5.25" Floppy 34-pin Drive Control Connector

This floppy drive control connector S8 is a 34-pin vertical header on Ø.1Ø-inch centers. Cabling should be flat ribbon or twisted-pair cable, less than 2Ø feet long. The cable pinouts are given in Table 4.

Table 4 - Floppy Drive Control Connector Pin Description

Signal Ground	Signal Pin	I/O	Signal Name
1	2	-	NC
3	4	-	NC
5	6	O	Drive Select Ø *
7	8	I	Index *
9	1Ø	O	Drive Select 1 *
11	12	O	Drive Select 2 *
13	14	O	Drive Select 3 *
15	16	O	Motor On *
17	18	O	Direction In *
19	2Ø	O	Step *
21	22	O	Write Data *
23	24	O	Write Gate *
25	26	I	Track ØØØ *
27	28	I	Write Protect *
29	3Ø	I	Read Data *
31	32	O	Side Select *
33	34	-	NC

3.10 The Run/Local Switch

The switch on the front panel (see Fig.9) is used to set the board into RUN or LOCAL mode. In the RUN mode normal access to the on-board registers can be performed and the green RUN LED is turned on.

No access to the on-board registers can be forced in LOCAL mode, since the board is isolated from the bus. This is indicated by the red LOCAL LED on the front panel (see Fig. 9).

3.11 The LED Indicators

The front panel of the SYS68K/WFC-1 contains two additional LEDs, BUSY LED and ERROR LED.

The BUSY LED is turned on if the board is busy and a command is being executed.

The ERROR LED indicates that an error has occurred in the execution of a command. The ERROR LED is turned off only when a new command is being executed.

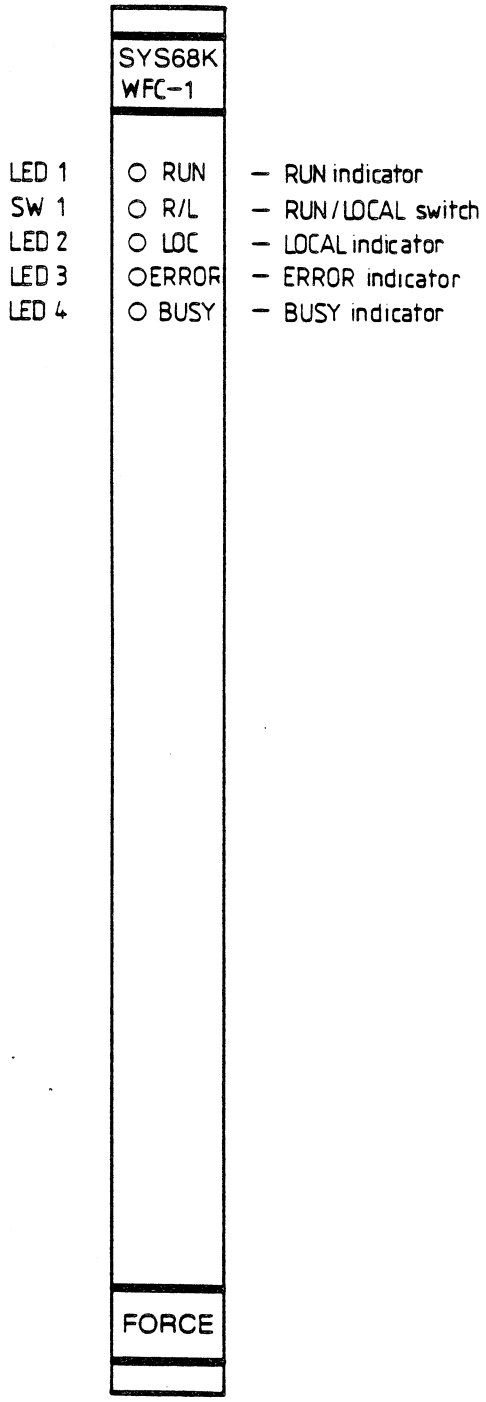


FIG. 9 THE FRONT PANEL OF THE SYS68K/WFC-1

3.12 Access Times

A Read/Write access to the SYS68K/WFC-1 can be performed under the following conditions :

The SYS68K/WFC-1 contains a jumper BR17 which can specify the speed of read and write operation to the board. The Read/Write access time is default 450ns and can be slowed by setting the jumper in the second or third position. The following table shows the three different access times :

BR17 Connections	Access Time
1 to 6	450ns .... default
2 to 5	650ns
3 to 4	850ns

Fig. 10 shows the detailed Read Timing Diagram and Table 5 lists the time values.

Fig. 11 shows the detailed Write Timing Diagram and Table 6 lists the time values.

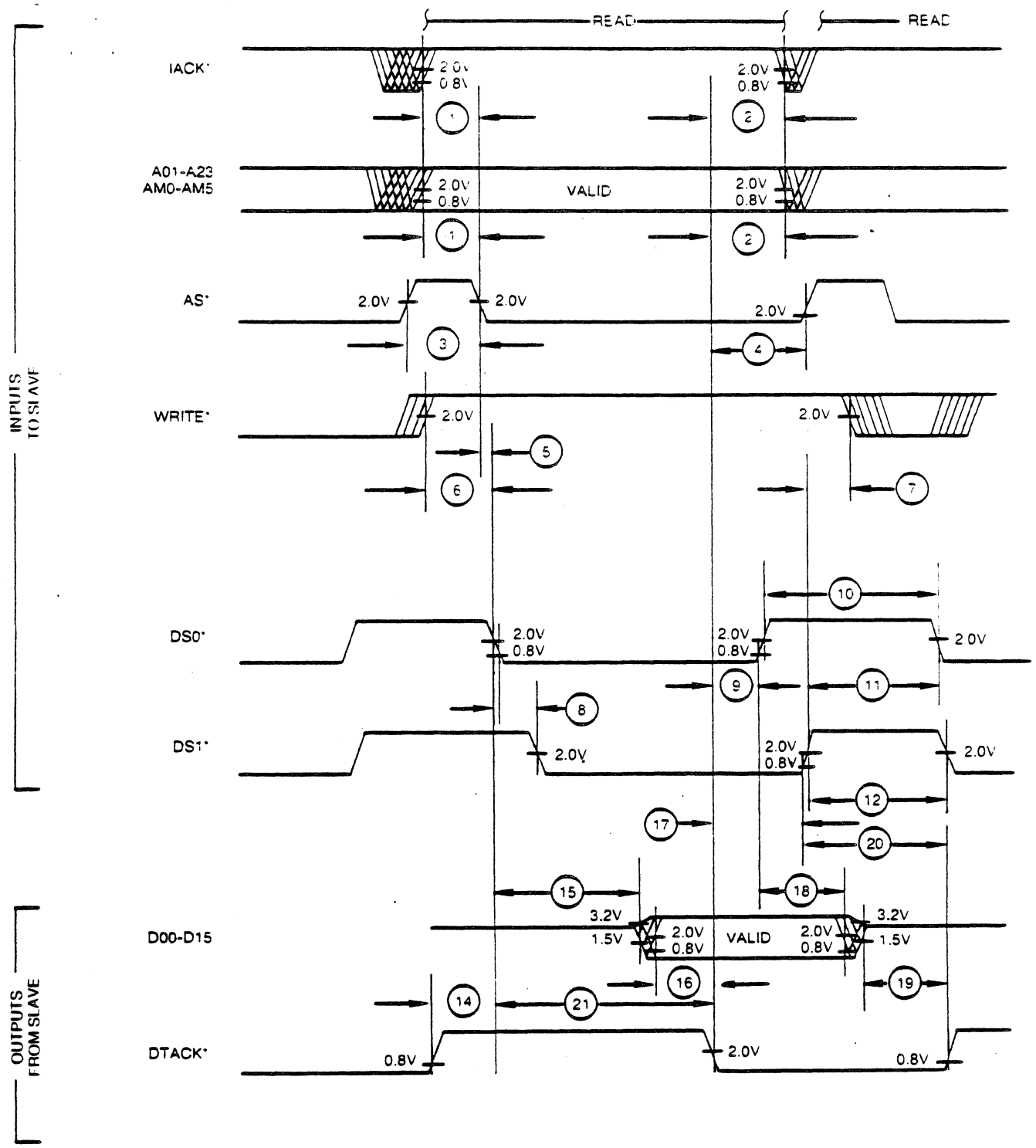


FIG. 10 DATA TANSFER BUS READ CYCLE
(SLAVE TIMING)

Table 5. - Data Transfer Bus Read Time Values

Number	Parameter	(Note A) Min.	Max.	Notes
1	Axx and AMx valid and IACK* high to AS* low	1Ø		E
2	DTACK* low to invalid address IACK* low	Ø		D
3	AS* High	3Ø		E
4	DTACK* low to AS* high	Ø		D
5	AS* to DS"A"* skew	-1Ø		E
6	WRITE* valid to DS"A"* low	1Ø		E
7	DS"B"* high to invalid WRITE*	Ø		E
8	DS"A"* to DS"A"* skew		2Ø	E
9	DTACK* low to DS"A"* high	Ø		D
1Ø	DA"A"* high	3Ø		E
11	DS"B"* high to DS"A"* low	3Ø		E
12	DS"B"* high	3Ø		E
13				
14	DTACK*/BERR* high to DS"A"* low	Ø		D
15	DS"A"* low to Active data bus	Ø		C
16	Data valid to DTACK* low	Ø		B
17	DTACK* low to DS"B"* high	Ø		D
18	DS"A"* high to invalid data	Ø		C
19	Data bus released to DTACK*/BERR* high	Ø		B
2Ø	DS"B"* high to DTACK*/BERR* high	Ø		C
21	DS"B"* low to DTACK* low	23Ø	25Ø	B

Notes:

A. All times given are in nanoseconds.

B. The SYS68K/WFC-1 guarantees this timing between two of its outgoing signal transitions.

C. The SYS68K/WFC-1 waits for the incoming signal edge from the MASTER before changing the level of its outgoing signal.

D. This is a guarantee that the MASTER will not change the incoming signal until the SYS68K/WFC-1 changes its outgoing signal.

E. The SYS68K/WFC-1 is guaranteed this timing between two of its incoming signal transitions.

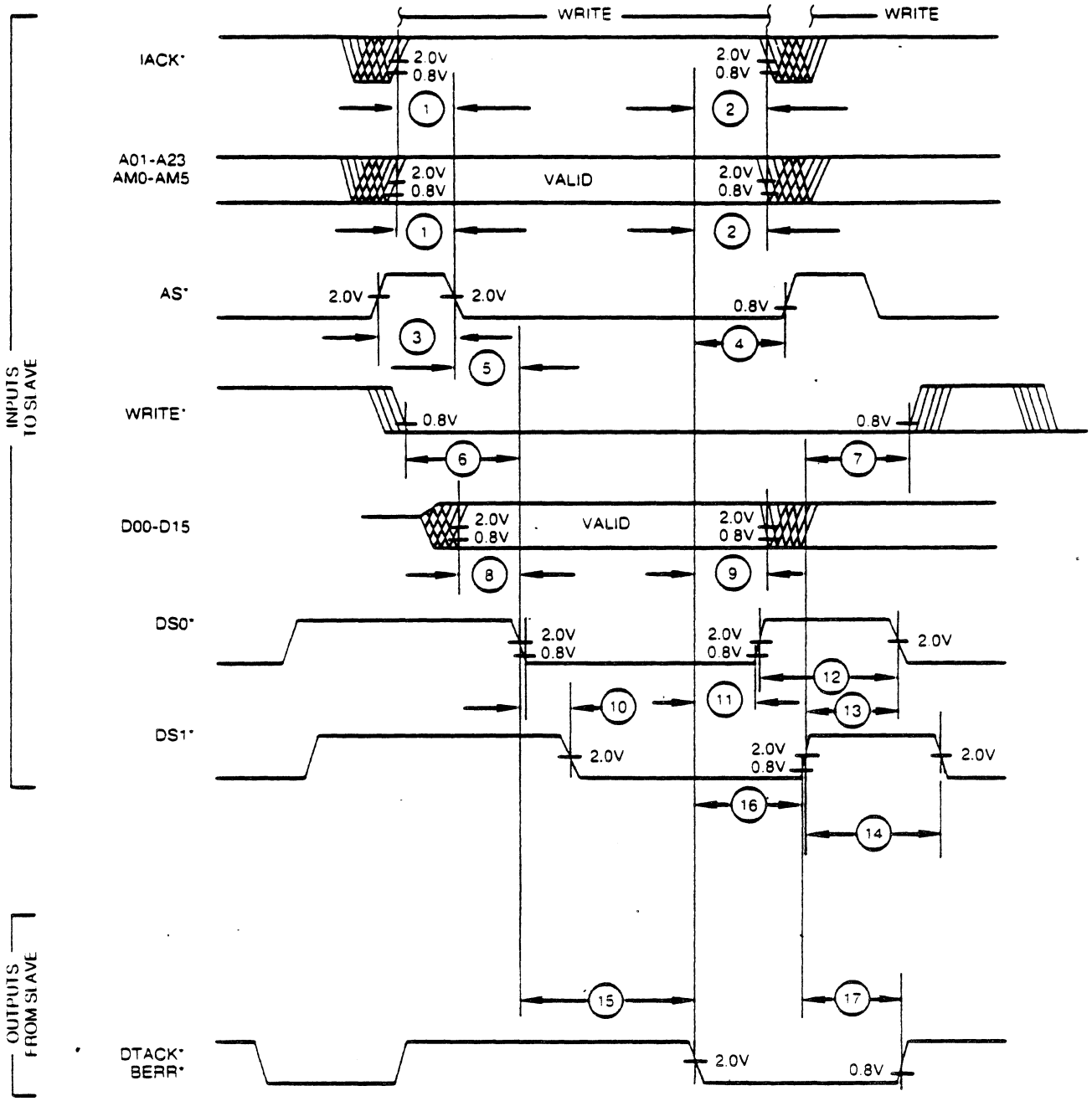


FIG. 11 DATA TRANSFER BUS WRITE CYCLE
(SLAVE TIMING)

Table 6. - Data Transfer Bus Write Time Values

Number	Parameter	(Note A) Min.	Max.	Notes
1	Axx And AMx valid and IACK* high to AS* low	1Ø		D
2	DTACK* low to invalid address or IACK* low	Ø		C
3	AS* high	3Ø		D
4	DTACK* low to AS* high	Ø		C
5	AS* to DS"A" skew	-1Ø		D
6	WRITE* valid to DS"A"* low	1Ø		D
7	DS"B"* high to invalid WRITE*	Ø		D
8	Data valid to DS"A"*low	1Ø		D
9	DTACK* low to invalid data	Ø		C
1Ø	DS"A"* to DS"B"* skew		2Ø	D
11	DTACK*/BERR* low to DS"A"* high	Ø		C
12	DS"A"* high	3Ø		D
13	DS"B"* high to DS"A"* low	3Ø		D
14	DS"B"* high	3Ø		D
15	DS"A"* low to DTACK* low	23Ø	25Ø	B
16	DTACK*/BERR* low to DS"B"* high	Ø		C
17	DS"B"* high to DTACK*/BERR* high	Ø		B
18	DS"A" to BERR* low on Parity Error	3Ø	48Ø	

Notes:

A. All times given are in nanoseconds.

B. The SYS68K/WFC-1 must wait for the incoming signal edge from the MASTER before changing the level of its outgoing signal.

C. This is a guarantee that the Bus MASTER will not change the incoming signal until the SYS68K/WFC-1 changes its outgoing signal.

D. The SYS68K/WFC-1 is guaranteed this timing between two of its incoming signal transitions.

E. The SYS68K/WFC-1 guarantees this timing between two of its outgoing signal transitions.

4.Ø SYS68K/WFC-1 Register Set

4.1 Register Set Basics

The SYS68K/WFC-1 performs all disk functions through a set of registers. The registers are loaded with parameters such as sector number, cylinder number, etc., prior to issuing a command. Individual registers are selected via A1-A3 for both types of drives. There are only Read-Only/Write-Only Registers and a FIFO Buffer for data.

4.2 SYS68K/WFC-1 Address Map

Table 7. shows the available registers and the default SYS68K/WFC-1 Address Map.

Address Default	Read Register	Write Register
BØ1ØØØ		Complete Interrupt Vector Register
BØ1ØØ1	Data Register	Data Register
BØ1ØØ2		Data Req Interrupt Vector Register
BØ1ØØ3	Error Register	Write Precomp*
BØ1ØØ5	Sector Count	Sector Count
BØ1ØØ7	Sector Number	Sector Number
BØ1ØØ9	Cylinder Low	Cylinder Low
BØ1ØØB	Cylinder High**	Cylinder High**
BØ1ØØD	Size/Drive/Head	Size/Drive/Head
BØ1ØØF	Status Register	Command Register

* not used on floppies

** LSB of cylinder high, if set to 1 permits a 48 tpi floppy disk to be read on a 96 tpi floppy disk system.

4.3 Data Register

This register is the user's window to the on-board full sector buffer. It contains the next byte of data to be written to or read from the internal sector buffer. When the DRQ (Data Request) bit is asserted, the second buffer contains data to be read during a Type II command, or is awaiting data to be written during a Type III command. If the SYS68K/WFC-1 is interfaced using programmed I/O, data transfers to this register can be implemented using programmed block moves. This register may not be read from or written to except in the context of a valid command.

4.4 Error Register

This register contains specific fault information pertaining to the last command executed. This register is only valid if the error bit in the status register is set. The error register is read only. Table 8 shoes the error register bits.

Table 8 - Error Register Bits

Bit	Error Register
7	Bad Block Detect
6	Uncorrectable Error
5	--
4	ID not found
3	--
2	Aborted Command
1	TRØØØ Error
Ø	DAM not found

Error Register Bits Description

DAM NOT FOUND	Will be set during a read sector command, if, after successfully identifying the ID field, the data address mafk has not been detected within 16 bytes of ID field.
TRØØØ ERROR	Will be set during a restore command if the track ØØØ line has not been asserted by the drive, after all stepping pulses have been issued. The Winchesters are issued a maximum of 1Ø23 stepping pulses and the floppies a maximum of 256 stepping pulses.
ABORTED COMMAND	Indicates that a valid command has been received that cannot be executed based on status information from the drive, i.e. drive not ready, seek complete not asserted, or write fault. Interrogation of the status register by the host may be performed to determine the cause of this failure.
ID NOT FOUND	When set, this bit indicates that an ID field containing a specified cylinder, head, sector number or sector size has not been found after all the retries have been executed.
UNCORRECTABLE ERROR	Indicates that an ECC or CRC error has been encountered in a data field during a read sector command and the error was uncorrectable.
BAD BLOCK DETECT	Indicates that a bad block mark has been detected in the specified ID field. If the command issued was a write sector command, write gate may be pulsed but the sector will not be written If generated from a read sector command, the data field will not be read. Note that bad block may not be detected if there is a flaw in the ID field.

4.4.1 Diagnostic Errors

On power-up, or when specifically commanded to, the SYS68K/WFC-1 will run a series of internal diagnostic tests. When an error is encountered, the diagnostic routine is terminated. A binary error code is set in the error register without the error bit of the status register being set. The diagnostic routines are exercised in the following order :

Error Code	Major Functional Failure
5	WD1Ø15 error
4	WD1Ø14 or bus error
3	Sector buffer error
2	WD1Ø1Ø error
1	WD2797 error
Ø	Pass-board is functional

4.5 Write Precompensation Register

The write precompensation register holds the cylinder number where the RWC line will be asserted and write compensation logic is to be turned on. This write-only register is loaded with the cylinder number divided by 4 to achieve a range of 1Ø24 cylinders. For example, if write precompensation is desired for cylinder 128 (8Ø Hex) and higher, this register must be loaded with 32 (2Ø Hex). The writer precompensation delay is fixed at 12 nanoseconds from nominal.

This register is not used for floppy disk drives. Floppy disk write precompemsation is contained in WD2797.

4.6 Sector Count

The sector count register is used in read sector, write sector, and format commands to implement multiple sector handling with one command. The value of zero implies a transfer of 256 sectors (any size). For read and write multiple sector commands, the sector count is decremented, and the sector number is incremented after each sector transfer to or from the buffer. During a format command, this register is loaded with the number of sectors to be formatted and decremented as each sector is formatted until it reaches zero. During format, sector numbers are specified using interleave tables loaded in the sector buffer. The sector count is a Read/Write Register.

4.7 Sector Number

This register is loaded with the desired sector number prior to a read or write command. The sector number register may be read or written to by the host.

4.8 Cylinder Number

These two registers form the cylinder number where the head is to be positioned on a seek, read, or write command. The two least significant bits of the cylider high register form the most significant bits if the cylider number as illustrated below:

	Cylinder High								Cylinder Low							
Register bits :	7	6	5	4	3	2	1	Ø	7	6	5	4	3	2	1	Ø
Cylinder bits :							9	8	7	6	5	4	3	2	1	Ø

When bit Ø of the cylinder high register (bit 8 of cylinder register) is set to a 1 during floppy operation, 48 tpi disks can be used in 96 tpi disk drives for all commands. When this bit is set to Ø, only 96 tpi disks can be used.

4.9 SDH Register

This register contains the ECC/CRC sector size, drive select, and head select bits. The SDH register is a Read/Write Register organized as shown in Table 9.

The SDH register is used to select either the Winchester or the floppy disk drives as implied by bits 3 and 4 shown in Table 9. If either bit is set to zero, then one of the hard disks is selected, and bits Ø, 1, and 2 are used to select one of eight heads.

When bits 3 and 4 are both set to 1, then a floppy disk will be selected. Bits Ø, 1, and 2 are used to select one of four drives with side select Ø or 1 as shown.

Whenever different drives are to be accessed, the SDH register must be updated by the host prior to a command being issued.

The ECC/CRC bit is only supported for the Winchester Disk Controller, therefore the host must be set to SDH bit 7 = Ø for all floppy commands. If SDH bit 7 is set to 1 by a Winchester operation, then the Error Correction Mode is supported. If this bit is cleared (=Ø), then a CRC generation and verification for data and all I.D. fields is supported.

Table 9. - Size Drive Head Register

Bit	7	6 5	4 3	2 1 Ø
Function	CRC/ ECC	Sec Size	Drive Select	Head/ Drive Select

SDH Bits 6 & 5

Bit 6	Bit 5	Sector Size
Ø	Ø	256 Bytes
Ø	1	512 Bytes
1	Ø	1Ø24 Bytes
1	1	128 Bytes

SDH Bits 2, 1 & Ø Hard Disk

Bit 2	Bit 1	Bit Ø	Head Selected Hard Disk
Ø	Ø	Ø	Head Ø
Ø	Ø	1	Head 1
Ø	1	Ø	Head 2
Ø	1	1	Head 3
1	Ø	Ø	Head 4
1	Ø	1	Head 5
1	1	Ø	Head 6
1	1	1	Head 7

Table 9. Size Drive Head Register

SDH Bits 4 & 3

Bit 4	Bit 3	Drive Selected (decoded & latched)
Ø	Ø	Drive Sel 1
Ø	1	Drive Sel 2
1	Ø	Drive Sel 3
1	1	Floppy Dr Sel

SDH Bits 2, 1 & Ø Floppy Disk

Bit 2	Bit 1	Bit Ø	Floppy Drive & Head Select
Ø	Ø	Ø	FD1 - HSØ
Ø	Ø	1	FD1 - HS1
Ø	1	Ø	FD2 - HSØ
Ø	1	1	FD2 - HS1
1	Ø	Ø	FD3 - HSØ
1	Ø	1	FD3 - HS1
1	1	Ø	FD4 - HSØ
1	1	1	FD4 - HS1

4.10 Status Register

After execution of a command, the status register is loaded with status information pertaining to the command executed. The host must read this register to ascertain successful execution of the command. The status register is a read-only register; it cannot be written to by the host. If the BUSY bit is set, no other bits in this register are valid.

Status register bits are shown as follows :

Bit	Status Register
7	Busy
6	Drive Ready
5	Write Fault
4	Seek Complete
3	Data Request
2	Corrected Data
1	Not used
0	Error

ERROR — When set, indicates that one or more bits are set in the error register. It provides an efficient means of checking for an error condition by the host. This bit is reset on receipt of a new command.

CORRECTED DATA — This bit indicates that an error correction has been successfully completed on the data field just read from the Winchester disk. For multiple mode operations, this bit indicates one or more data fields have been successfully corrected. If an uncorrectable error occurs, the command is terminated with the appropriate bit being set in the error register.

DATA REQUEST — When set, it indicates that the sector buffer is ready to accept data or contains data to be read by the host. The data request bit is reset when the sector buffer has been fully read or written. Normally, the host need not consult this bit to determine if a byte should be transferred.

SEEK COMPLETE — Indicates the condition of the seek complete line on the selected Winchester drive. For floppy drives, this line is asserted when the SDH register is reloaded.

WRITE FAULT/ WRITE PROTECT — Indicates the condition of the write fault line on a selected Winchester drive. The SYS68K/WFC-1 will not execute any command if this bit is set. If a write-protected disk is sensed in a selected floppy drive during a write operation, the write fault bit will be set. The command will then be aborted and no writing will take place.

READY — Indicates condition of ready line on drive. SYS68K/WFC-1 will not execute any commands unless the ready bit is set. Normally, this line is asserted for floppy drives when the SDH register selects any floppy drive. A user available jumper BR3 option can be implemented if the READY line is available from the floppy drive.

BUSY — After issuing a command, or initialising SYS68K/WFC-1 internal diagnostics, this bit will be set, indicating that the SYS68K/WFC-1 is busy executing a command. No other bits or registers are valid when this bit is set.

4.11 Command Register

All commands are loaded into this register after all other registers have been set.

The command register is a Write Only Register.

4.12 Interrupt Vector Registers

The SYS68K/WFC-1 controller board contains two write only interrupt vector registers. The first interrupt vector register is for the complete interrupr and the second one for the data request interrupt. The registers are free programmable and the address is described in the address map.

5.Ø Commands

5.1 General

The SYS68K/WFC-1 executes six, easy-to-use, macro.commands. Most commands feature automatic "implied" seek, which means the host system need not tell the SYS68K/WFC-1 where the R/W heads of each drive are nor when to move them. The controller automatically performs all retries on error encounters, including data ECC Errors. If the R/W head mis-positions, the SYS68K/WFC-1 will automatically perform a restore and a re-seek. If the error is completely unrecoverable, the SYS68K/WFC-1 will simulate a normal completion to simplify the host's software.

The commands executed by the SYS68K/WFC-1 are mapped to the commands supported by the two disk controllers. The format of the SYS68K/WFC-1 commands is the same as that of the WD1Ø1Ø commands. The on-board WD1Ø15 buffer manager translates this format for the WD2797, transparent to the user. Error correction is only supported for the Winchester disk controller, therefore, the host must set SDH bit 7 = Ø for all the commands when a floppy disk is selected.

Commands are executed by loading the command byte into the command register while the controller is not busy. The host must observe the following simple protocol:

- The registers must be loaded prior to issuing a command. Only parameters that change from the previous command need be entered.

- For any write/format operations, the sector buffer must be filled with the appropriate data before the command can be executed by the SYS68K/WFC-1.

No command will execute if the seek complete or ready lines are false, or the write fault line is true. Normally it is not necessary to poll these signals before issuing a command. If a command is received, that is not defined in Table 1Ø. , undefined results will occur.

5.2 SYS68K/WFC-1 Command Summary

Commands have been divided into three types as summarized in Table 1Ø.

Table 10 - Command Types

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Test	1	0	0	1	0	0	0	0
I	Restore	0	0	0	1	r3	r2	r1	r0
I	Seek	0	1	1	1	r3	r2	r1	r0
II	Read Sector	0	0	1	0	D	M	0	0
III	Write Sector	0	0	1	1	0	M	0	0
III	Format Track	0	1	0	1	0	0	0	0

M = Multiple Sector
D = Read Interrupt

M = 0 : Single Sector
D = 0 : Programmed I/O Mode

M = 1 : Multiple Sector
D = 1 : DMA Mode

Table 11. r3-r0 Stepping Rate

r3-r0	Winchester Disk Drives	Floppy Disk Drives
0000	approx. 35 us	approx. 15 us
0001	0.5 ms	1.0 ms
0010	1.0 ms	2.0 ms
0011	1.5 ms	3.0 ms
0100	2.0 ms	4.0 ms
0101	2.5 ms	5.0 ms
0110	3.0 ms	6.0 ms
0111	3.5 ms	8.0 ms
1000	4.0 ms	10 ms
1001	4.5 ms	12 ms
1010	5.0 ms	14 ms
1011	5.5 ms	16 ms
1100	6.0 ms	18 ms
1101	6.5 ms	20 ms
1110	7.0 ms	25 ms
1111	7.5 ms	40 ms

5.3 Type I Commands

Type I commands do not effect transfer of data between the host and the SYS68K/WFC-1, but merely position the R/W heads of the selected drive or run diagnostics. The restore and seek commands have explicit stepping rate fields. The lower four bits of these commands form the stepping rate for the drives.

5.3.1 Test Command

Bit code: 1 Ø Ø 1 Ø Ø Ø Ø

The test command is used to run internal diagnostics for checking SYS68K/WFC-1 board function. It is mainly employed to isolate faults in the board logic. This command is always executed on a RESET. Any faults are reported as error codes.

5.3.2 Restore

Bit code: Ø Ø Ø 1 R3 R2 R1 RØ

The restore command is used to calibrate the position of the R/W head on each drive by stepping the head outward until the TRØØØ line goes true. Upon receipt of the restore command, the BUSY bit in the status register is set. Cylinder High and cylinder Low Registers are cleared. For Winchester operation, the actual stepping rate is determined by the Seek Complete period. For floppy operation, a minimum stepping pulse of 8 msec. is used. However, the stepping rate field specified by the host is saved internally for use in all future implied seeks. The state of seek complete, ready and write fault are sampled, and if an error condition exists, the aborted command bit in the error register is set, the error bit in the status register is set, an interrupt is generated, and the BUSY bit is cleared.

Regardless of errors encountered, the internal head position register for the selected drive is cleared. The TRØØØ line is sampled. If TRØØØ is true, an interrupt is generated and the BUSY bit is reset. If TRØØØ is not true, stepping pulses at a rate determined by the stepping rate field are issued until the TRØØØ line is activated. When TRØØØ is activated, the busy bit is reset and interrupt is issued. If the TRØØØ line is not activated within 1Ø24 stepping pulses, the TRØØØ error bit in the error register and the error bit in the status register are set, the BUSY bit is reset and an interrupt is issued.

5.3.3 Seek

Bit code: Ø 1 1 1 R3 R2 R1 RØ

The seek command positions the R/W head at a certain cylinder. It is primarily used to start two or more concurrent seeks on drives that support buffered stepping. Note that the seek complete line is not sampled after the seek command so that multiple seek operations may be started using drives with buffered seek capability.

5.4 Type II Commands

Type II commands characteristically transfer blocks of data from the SYS68K/WFC-1 buffer to the host. This type of command has an implicit stepping rate as set by the last restore or seek command.

5.4.1 Read Sector

Bit code: Ø Ø 1 Ø D M Ø Ø

The read sector command is used to enable the host computer to read a sector of data from the disk. If ECC is enabled, ECC bytes are recomputed by the SYS68K/WFC-1. After the buffer is full, the recorded ECC bytes are compared to the recomputed check bytes to generate the syndrome bytes. If the syndrome is non-zero, errors have occurred. Error correction is invoked by the WD1Ø15 if two consecutive syndromes match, otherwise a maximum of 8 retries is attempted by the WD1Ø15. If the data is correctable, the WD1Ø15 makes the correction and passes the data in the buffer to the host. If, after eight retries, the syndromes do not match, the SYS68K/WFC-1 sends an error status to the host along with the status from the WD1Ø1Ø. Multiple sector read commands are modified to single sector commands and are issued a multiple number of times. The status and error registers are updated for every block of data transferred.

During a floppy read sector operation only CRC is used with the data fields. If a CRC error occurs in the data field, the WD1Ø15 buffer manager attempts a maximum of 8 retries and reports the error only if it persists. Regardless of the drive accessed (Winchester or Floppy), CRC is used on all ID fields.

5.4.1.1 DMA Read

D = DMA Read Mode

Ø = Programmed I/O Mode
1 = DMA Mode

The DMA bit is used to position INTRQ in relation to DRQs during the read sector command. If the DMA bit is reset (D=Ø), the interrupt will occur along with the DRQ. This allows the programmed I/O host to intervene and transfer the data from the sector buffer. For programmed I/O, multiple transfer is not permitted (M=Ø). If the DMA bit is set (D=1), then the interrupt will occur only after the system DMA controller has transferred the entire buffer of data. This mode is always used with multiple sector transfers.

5.4.1.2. Normal Completion

A normal completion occurs when the SYS68K/WFC-1 encounters no errors. The BUSY bit is reset. The status of the DMA bit in the command byte is examined. If this bit is reset (D=Ø; programmed I/O mode), an interrupt is issued at this time. DRQ is set until all bytes of data have been read from the buffer. (Note: It is recommended that programmed I/O transfers should take place as a block move without consulting the DRQ bit in the Status Register). After all the data have been moved from the buffer, the DMA bit in the command byte is consulted again. If this bit is set (D=1; DMA mode) then an interrupt will be issued.

5.5 Type III Commands

This type of command is characterized by a transfer of a block of data from the host to the SYS68K/WFC-1 buffer. These commands have implicit stepping rates as set by the last restore or seek command.

The command will not be executed by the SYS68K/WFC-1 controller unless the buffer has been completely filled by the host.

5.5.1 Write Sector

Bit code: Ø Ø 1 1 Ø M Ø Ø

The Write Sector command is used to write a sector of data from the host computer to the disk. Upon receipt of the write command, the controller sets DRQ until the entire sector length of data has been written into the buffer. (Note: It is recommended that programmed I/O transfers should take place as a block move without consulting the DRQ bit in the Status Register.)

5.5.2 Format Track

The format command is used for initializing the ID and data fields on a particular disk. Upon receipt of the format command, the controller sets the DRQ for the interleave table to be written to the buffer. In all cases, the number of bytes transferred to the buffer must correspond to the current sector size.

When the buffer has been completely filled, the specified number of sectors are written and the DRQ is reset. The data field is written with ØØ for the hard disks and E5 (hex) for the floppies. ECC or CRC bytes are automatically computed and written.

Once the index is found, a number of ID and data fields are written to the disk. As each sector is written, the sector count register is decremented and consequently must be updated before each format operation.

6.Ø Programming

6.1 General

Users will find programming the SYS68K/WFC-1 relatively simple as a substantial amount of intelligence formerly required by host computers has been incorporated into the SYS68K/WFC-1 board.

The SYS68K/WFC-1 performs all needed retries, even on head positioning errors. If there is an error in the data field, the SYS68K/WFC-1 will attempt to correct it.

Most commands feature automatic "implied" seek, which means that seek commands need not be issued to perform basic read/write functions. The SYS68K/WFC-1 keeps track of the head position up to eight read/write head assemblies, eliminating the need for the host system to maintain track tables.

All transfers to and from disk are through an on-board sector buffer. This means that data transfers are fully interruptable and can take place at any speed that is convenient to the system designer. In the event of an unrecoverable error, the SYS68K/WFC-1 simulates a normal completion so that special error recovery software is not needed.

6.2 Setting Register Set

Before any of the six macro commands may be executed, a set of parameter registers must be set up. For most commands, this informs the controller board of the exact location on the disk where the data involved in the transfer is located or will be placed. For a normal read or write sector operation, the sector number, the size/drive/head, the cylinder number, and the command registers (usually in that order) will be written.

Note that although most of these registers are readable as well as writeable, they normally are not read from. Read capability for them is provided, however, so that error-reporting routines can determine physically where an error occurred without recalculating the sector, head, and cylinder parameters.

Since all parameters can be recalled by the SYS68K/WFC-1, it is recommended that task file parameters be stored in the SYS68K/WFC-1 as they are calculated. This will save the programmer a few instructions and microseconds by not maintaining two copies of the same information.

6.2.1 Cylinders and Tracks

Since most hard-disk drives contain more than one head per positioner, it is more efficient to step the R/W head assemblies of most disk drives by cylinders, not tracks. In other words, the disk drive software should be designed to read or write all data that are directly accessible by all the heads on a position before stepping to a new cylinder.

The following table shows an example :

Physical Cylinder	Logical Head Number	Physical Head Side	Physical Platter
25	3	Top	B
26	Ø	Bottom	A
26	1	Top	A
26	2	Bottom	B
26	3	Top	B
27	Ø	Bottom	A

6.3 Type I Command Programming

Test, Restore and seek are Type I commands that position the R/W heads of the selected drive and set the implied stepping-rate register. No data is transferred to or from the data register. To execute a Type I command, the system software must perform the following functions in the order shown:

1. Set up register set and issue command with stepping rate.

2. Wait for interrupt or for BUSY bit in status register to be reset.

3. Check error bit in status register for proper completion.

6.3.1 Use of BUSY Bit

Smaller, single-user systems can sense the completion of a command by polling the BUSY bit of the status register. This bit (bit 7) is set whenever the controller starts a disk operation or internal diagnostics, and is reset whenever the controller is ready to communicate with the host computer.

The BUSY bit is located in the same place as the sign bit of many computers to simplify the polling process.

One way to poll this bit using 68000 code is as follows:

```
WAIT:   MOVE. B     STATUS,  DO ;   Input Status Register
        BTST        #7, DO   ;      Is Bit 7 Zero
        BNE         WAIT ;          Wait for BUSY Bit
```

6.3.2 Use of Interrupts

Another, more efficient way of notifying the CPU that the SYS68K/WFC-1 has completed a command is through interrupts. The IR1 line on the board makes a high-to-low transition whenever the disk controller requires CPU intervention. This allows the host CPU to run other tasks while the SYS68K/WFC-1 is reading or writing data to the disk. Only if this mode is used, the control logic is able to force interrupts to the VME bus.

6.3.3 Use of the Error Bit

As the SYS68K/WFC-1 simulates normal completions when errors have been encountered, the only way to determine error status is to check the error bit in the status register. The error bit is so located that it can be easily tested. The contents of the error register are not valid unless the error bit is set.

One way to check the Error bit using 68000 code is as follows:

```
MOVE.B      STATUS, DO      ; Get Status
BTST        # 1, DO         ; Is Error Bit Set
BNE         ERROR           ; Jump if Error Found
```

6.4 Type II Command Programming

The only Type II command is the read sector command. This command is characterized by the transfer of a block of data from the SYS68K/WFC-1 buffer to the host. The command features implied seek with an implicit stepping rate. To execute a Type II single-sector command in programme I/O mode, the system software must perform the following functions in the order shown:

1. Set up register set and issue command with DMA bit reset.

2. Wait for interrupt or for BUSY bit in status register to be reset.

3. Perform a block move from SYS68K/WFC-1 buffer to system memory.

4. Check error bit in status register for proper completion.

Note: Steps 3 and 4 above can be reversed.

To execute a Type II single or multiple sector command in DMA mode with interrupts, the system software does the following:

1. Set up register set and issue command with DMA bit set.

2. Set up DMA controller and wait for data request (DMA controller will move data from SYS68K/WFC-1 to memory).

3. Wait for interrupt from SYS68K/WFC-1.

4. Check error bit in status register for proper completion.

Note: The above sequence is preferred, but steps 1 and 2 above can be reversed.

6.4.1 DMA Mode

The DMA mode bit (D) in the foregoing read sector examples is a special bit in the command byte used to optimize the SYS68K/WFC-1 interrupts during programmed I/O and DMA operations. If the DMA bit is reset (D=Ø), the interrupt will come before the buffer is transferred. This allows a programmed I/O host to intervene and transfer the buffer of data. If the DMA bit is set (D=1), then the interrupt will occur only after the data has been transferred. This allows the host to go uninterrupted until the entire buffer has been transferred.

6.5 Type III Command Programming

Write sector and format are Type III commands. These commands are characterized by the transfer of a block of data from the host to the SYS68K/WFC-1 buffer. Like the Type II commands, these commands feature implied seek with an implicit stepping rate. To execute a single sector Type III command in programmed I/O mode, the system software must go through the following functions in the order indicated:

1. Set up register set and issue command.

2. Perform block move from system memory to SYS68K/WFC-1 buffer (SYS68K/WFC-1 will attempt to write a sector or format).

3. Wait for interrupt or for BUSY bit in status register to be reset.

4. Check error bit in status register for proper completion.

To execute a single or multiple sector Type III command in DMA mode with interrupts, the system software goes through the following steps:

1. Set up register set and issue command.

2. Set up DMA controller and wait for DRQ interrupt (DMA controller will move data from memory to SYS68K/WFC-1). SYS68K/WFC-1 will attempt to write sector or format.

3. Wait for interrupt from SYS68K/WFC-1.

4. Check error bit in status register for proper completion.

Note: Steps 1 and 2 above can be reversed.

6.5.1 Formatting

The format command is very similar to the write sector command, except that the sector buffer is filled with interleave and bad block information instead of with user data. Two bytes will be written to the buffer for each sector to be formatted.

The first (lower) byte will be either a ØØ or an 8Ø in Hex. If the lower byte is a ØØ, the sector is marked as good. If the lower byte is an 8Ø, and there is any attempt to read it or write to it, the sector will set the bad block bit in the status register.

The second (upper) byte is the logical sector number of the next sector to be formatted. This number will be recorded on the disk. The sector number register is not used during format.

6.5.1 Formatting

On a 32-sector-per-track disk, 32 pairs of bytes containing formatting information must be supplied to the drive during each format operation. To start the format operation, the buffer must be completely filled, even if the sector table is not as long as the buffer. This means that on a 32-sector-per-track disk, with 64 bytes of formatting information supplied, if the sector size is 256 bytes, then 192 bytes of garbage must be passed to the controller to start the format operation.

As the contents of the sector buffer do not imply how many sectors are to be formatted, a dedicated register is provided. This Sector Count register must be loaded with the number of sectors to be formatted before every format operation.

6.5.2 Interleaving

If sequential sectors on the disk are to be read, the next sector will pass by the read/write head before a read or write can be set up. The disk will then have to make a complete rotation to pick up this next sector. If an attempt is made to read all 32 sectors on a particular track, it requires 32 rotations or about a half a second per 8K bytes. This performance can be significantly improved by interleaving, a technique that allows the system to read or write more than one sector per rotation.

Suppose the system takes less than three sector times (3 times 32 rotational periods with 256 byte sectors) to digest the data that it has read and to set up the next read operation. This means that if the second logical sector can be physically placed four sectors away from the first one, the controller will be able to read it without much delay. This four-to-one interleave factor will allow a potential reading of the entire track in only four rotations. In the example given, the throughput will be increased by a factor of eight.

The simplest way to determine the optimum interleave for any particular system is through experimentation. If the system maintains its directories or virtual memory-swapping areas in a certain place on the disk, it sometimes makes sense to have more than one interleave.

To simplify driver software, the SYS68K/WFC-1 will automatically map logical sectors to physical sectors to achieve interleave. This logical-to-physical map is recorded during the format operation on each track of the disk in the ID fields of the sectors. Table 12. is an example of an interleave table for a 32-sector track with 4:1 interleave and no bad blocks.

6.5.2 Interleaving

The first byte in each byte-pair in Table 12 is set to ØØ. This marks each block as a "good" block. The second byte of each byte-pair is the logical sector number. The first byte pair in Table 12. represents the first logical sector of the track. The underlined byte pair represents the second logical sector.

Table 12. Interleave Table with 32 Sectors and 4:1 Interleave

ØØ	ØØ	ØØ	Ø8	ØØ	1Ø	ØØ	18
ØØ	Ø1	ØØ	Ø9	ØØ	11	ØØ	19
ØØ	Ø2	ØØ	ØA	ØØ	12	ØØ	1A
ØØ	Ø3	ØØ	ØB	ØØ	13	ØØ	1B
ØØ	Ø4	ØØ	ØC	ØØ	14	ØØ	1C
ØØ	Ø5	ØØ	ØD	ØØ	15	ØØ	1D
ØØ	Ø6	ØØ	ØE	ØØ	16	ØØ	1E
ØØ	Ø7	ØØ	ØF	ØØ	17	ØØ	1F

Note: The balance of the buffer must be filled with something to start the format operation.

6.6.1 Read Sector Examples

An example to read a sector from a Winchester with the LUN Ø, track 8 and sector 1. The read data is placed at memory location $5ØØØ.

```
        MOVE.L    #$5ØØØ, A1          ;Destination Address =A1
        MOVE.L    #256,D1             ;D1 Byte Counter
        MOVE.B    #1,$BØ1ØØ5          ;Sector Number
        MOVE.B    #1,$BØ1ØØ7          ;Sector Counter
        MOVE.B    #8,$BØ1ØØ9          ;Load Cylinder Low
        MOVE.B    #Ø,$BØ1ØØB          ;Load Cylinder High
        MOVE.B    #128,$BØ1ØØD        ;Load Size/Drive/Head
        MOVE.B    #32,$BØ1ØØF         ;Load Read Command
WAIT:   MOVE.B    $BØ1ØØF,DØ          ;Read Status
        BTST      #7,DØ               ;Is WFC BUSY
        BNE       WAIT                ;Wait for BUSY Bit Reset
LOOP1:  MOVE.B    $BØ1ØØ1,(A1)+       ;Read Data from Buffer
        SUBQ.L    #1,D1               ;Decrement Byte Counter
        BNE       LOOP1
        MOVE.B    $BØ1ØØF, DØ         ;Read Status Register
        BTST      #Ø,DØ               ;Is Error occur
        BNE       ERROR               ;If Error occur go Error rout.
        TRAP       #Ø                 ;End with TRAP Ø. Read
                                       data are place into
                                       memory location $5ØØØ.
```

6.6.2 Write Sector Example

An example to write a sector to a Winchester with the LUN Ø, Track 8 and sector 1. The write data are placed on memory location $5ØØØ.

```
          MOVE.L    #$5ØØØ,A1          ;Destination Address = A1
          MOVE.L    #256,D1            ;D1 Byte Counter
          MOVE.B    #1,$BØ1ØØ5         ;Sector Number
          MOVE.B    #1,$BØ1ØØ7         ;Sector Counter
          MOVE.B    #8,$BØ1ØØ9         ;Load Cylinder Low
          MOVE.B    #Ø,$BØ1ØØB         ;Load Cylinder High
          MOVE.B    #128,$BØ1ØØD       ;Load Size/Drive/Head
          MOVE.B    #48,$BØ1ØØF        ;Load Write Command

LOOP1     MOVE.B    (A1)+,$BØ1ØØ1      ;Write Data to Buffer
          SUBQ.L    #1,D1              ;Decrement Byte Counter
          BNE       LOOP1

WAIT      MOVE.B    $BØ1ØØF,DØ
          BTST      #7,DØ              ;Is WFC BUSY
          BNE       WAIT               ;If WFC BUSY wait
          BTST      #Ø,DØ              ;Is Error occur
          BNE       ERROR              ;If Yes goto Error routine
          TRAP      #Ø                 ;End with TRAPØ. Write
                                       ;data are placed on Winch.
```

APPENDIX "A"

SPECIFICATION OF THE SYS68K/WFC-1

Interfaces	4 SA450 compatible Floppy Drives 3 ST506 compatible Winchester Drives
Devices	WD2797 Floppy Disk Controller WD1010 Winchester Disk Controller WD1014 Error Detection & Support Device WD1015 Buffer Manager ECC
Control	RUN/LOCAL Switch for BUS isolation 4 Status indication LED's BUSY, ERROR RUN and LOCAL
Memory	1K-byte FIFO Buffer for Data Transfer Serial I/O
Specials	Error Correction and Detection by Disk Operation. Programmable interrupt vector registers. Two different interrupts generation.
Bus	VME bus interface including address modifier.
Power Requirements	+ 5V / 1600 mA (typ), 1800 mA (max) + 12V / 200 mA (typ), 300 mA (max) - 12V / 200 mA (typ), 300 mA (max)
Operating Temperature	0 to 50 degrees Celsius
Relative Humidity	0 - 90 % (non-condensing)
Board Dimensions	233.7 * 160.0 * 5.0 mm 9.2 * 6.3 * 0.19 inch

APPENDIX "B"

MEMORY MAP FOR THE SYS68K/WFC-1

B01000	Complete Interrupt Vector Register
B01001	Data Register
B01002	Data Request Interrupt Vector Register
B01003	Error Register / Write Precomp Register
B01005	Sector Count
B01007	Sector Number
B01009	Cylinder Low
B0100B	Cylinder High
B0100D	Size-Drive-Head
B0100F	Status / Command Register

APPENDIX "C"

SYS68K/WFC-1 COMPONENT PART LIST

Location	Type	Manufacturer	Function
J1	96S02	Fairchild	IC Dual Retrig One Shot
J2,J6,J18 J25	74S74	TI, NSC, MOT	D Flip Flop
J3,J16	74S00	TI,NSC, MOT	q Input NAND-Gates(OC)
J4,J22	74S74	TI, NSC, MOT	D-Flip Flop
J5	TPQ 6700	Telefunken	2NPN/2NPN transistor
J7,J13	74S64	TI	4-2-3-2 Input and-or invert gates
J8,J20,J48 J57,J49, J52,J55	74LS688	TI	8 Bit comparator
J9,J21	PAL	FORCE	
J10	74LS367	TI	Hex Buffer Drivers
J11,J23	74LS04	TI	Hex Inverters
J12	DDU4-6-60	DATA DELAY	60 Ns delay line
J14	74S04	TI	Hex Inverters
J15	74LS244	TI	Octal Buffers/Line Drivers
J17,J19	74LS02	TI	Quadruple 2 Input positive NOR gates
J24	74LS175	TI	Quad D-Type Flip Flops
J26	74LS174	TI	Hex D-Type Flip Flops
J27	WD1014	WD	Error Detection & Support Device
J28	WD2797	WD	Floppy Disk Controller

APPENDIX "C"
(cont'd)

SYS68K/WFC-1 COMPONENT PART LIST

Location	Type	Manufacturer	Function
J29	74LS193	TI	Synchronous UP/DOWN Dual Clock Counters
J30	74196	TI	Press Table Counter Latches
J31	74LS145	TI	BCD to Decim.Decoder
J32	74LS393	TI	Dual 4-Bit Binary Counters
J33	74S124	TI	Dual voltage controlled oscillator
J34	74LS132	TI	Quadruple 2-Input NAND Schmitt Triggersr
J35	WD1010	WD	Winchester Disk Controller
J36	WD1015	WD	Buffer Mgr ECC
J37	6116	HI	2Kx8 Byte Memory
J38	AM26LS31	AM	Quad Differential Line Driver
J39	74S05	TI	Hex Inverters (OC)
J40,J41	74LS14	TI	Hex Inverters
J42,J56, J58,J54	74LS645-	TI,MMI	8 Bit Bus Transceiver
J44,J43, J50,J47	74LS373	TI,NSC,MOT	Octal D-Type FF's
J45	7406	TI	Hex Inverter Buffer
J46	MC3487		
J51	AM26LS32	AM	Quad Differential Line Receiver
J53	74LS641-1	TI	OC Bus Transceiver

SYS68K/WFC-1 COMPONENT PART LIST

Location	Type	Manufacturer	Function
R38	330R	Various	Resistor
R21,R29,R30	220R	"	"
R22,R23,R24	100R	"	"
R25	1K	"	"
R26,28,31 33,34,35 1,5,6,7,8,9, 10	1K	"	"
R27	3,3K	"	"
R36	200R 1%	"	"
R37,32	2K37 1%	"	"
R39	680R	"	"
RN1,2,3, 4,5,6,7,8	9x4,7KO	"	Resistor Network
RN9	8x150R (5x150OR)	"	" "
RN10	220-330	"	" "
R2	10K	"	Resistor
R3,4,11, 12	470R	"	"
R13	4K7	"	"
R14,R16	22K	"	"
R15	5K6	"	"
R44,45,46, 47,48,49, 40,41,42,43	150R	"	"
P1,P2	P10K	"	Potentiometer

SYS68K/WFC-1 COMPONENT PART LIST

Location	Type	Manufacturer	Function
C1,C6	5-60p	Various	Variable Capacitor
C2	2uF	"	Capacitor
C3,4,5, 13,14,15 C26...C79	0,100uF 50V	"	"
C7	22pF	"	"
C12	68pF	"	"
C17	150pF	"	"
C16	6,8 nF	"	"
C18	330 pF	"	"
C19	22 kF	"	"
C11	100 p	"	"
C20,21,22,	560 pF	"	"
C23	820 pF	"	"
BR8	JMP3		Jumper
BR9	JMP3		"
BR10	JMP16		"
BR11	JMP16		"
BR12	JMP16		"
BR13	JMP12		"
BR15	JUMP3		"
BR16	JUMP9		"
BR20,21,22	JUMP6		"
BR17	JUMP6		"

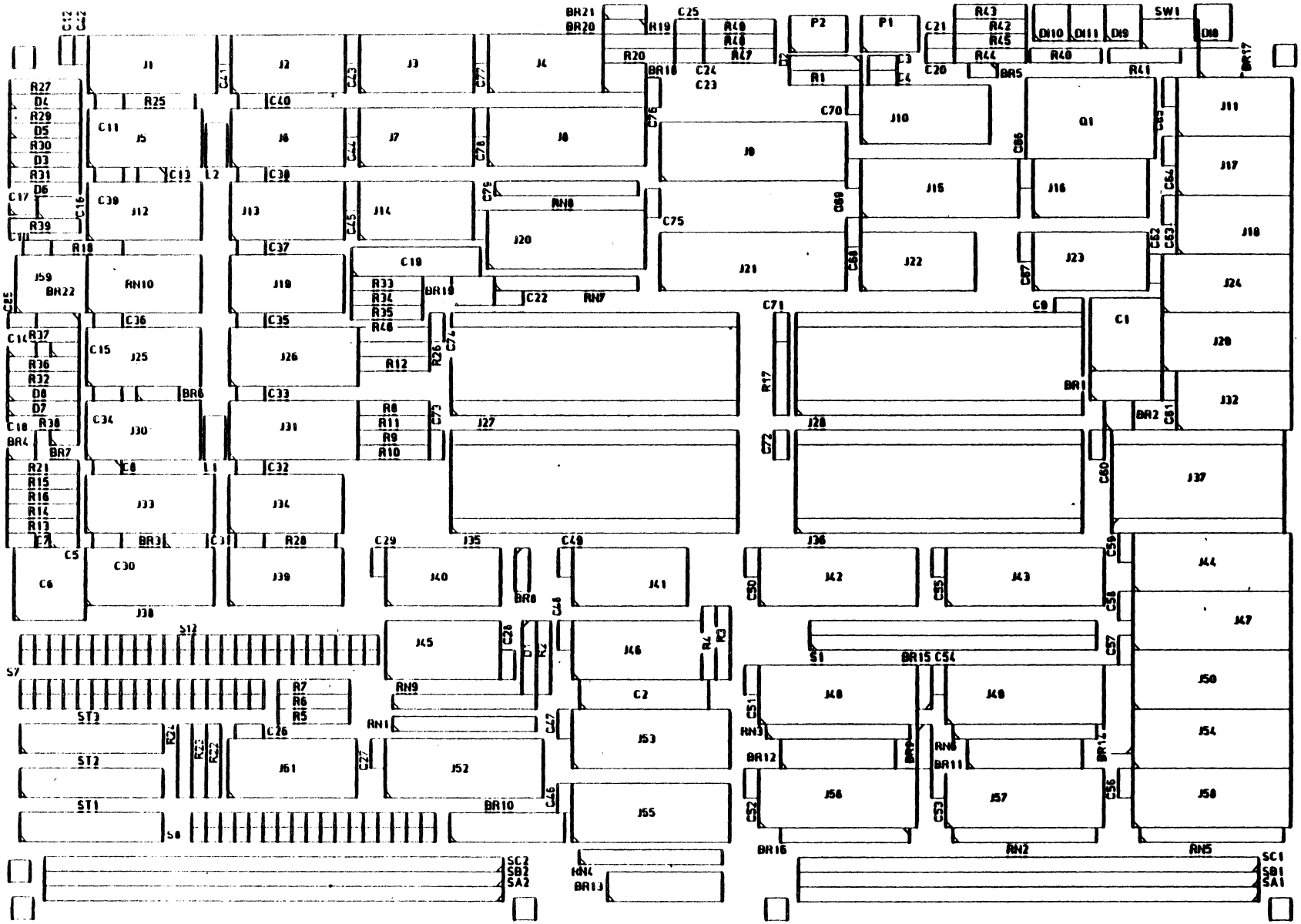
SYS68K/WFC-1 COMPONENT PART LIST

Location	Type	Manufacturer	Function
BR18,BR19	JUMP6		Jumper
ST1	JUMP2Ø		Connector
ST2	JUMP2Ø		"
ST3	JUMP2Ø		"
S7	JMP34		"
S8	JMP34		"
Q1	2Ø MHZ		Quarz
L1	4.7 uH		
L2	4.7 uH		
DØ1	1N4148		Diode
DØ2	"		"
DØ3	"		"
DØ4	"		"
DØ5	"		"
DØ6	"		"
DØ7	"		"
DØ8	"		"
DI8	LED		LED
DI9	LED		LED
DI1Ø	LED		LED
DI11	LED		LED

SYS68K/WFC-1 COMPONENT PART LIST

Location	Type	Manufacturer	Function
BR1	JUMP8		Jumper
BR2	JUMP4		Jumper
BR3	JUMP3		Jumper
BR4	JUMP2		Jumper
BR5	JUMP2		Jumper
BR6	JUMP3		Jumper
BR7	JUMP2		Jumper

APPENDIX "D"


J1
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J4
J5
J6
J7
J8
J9
J10
Q1
J11
J12
J13
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J15
J16
J17
J18
J19
J20
J21
J22
J23
J24
J25
J26
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J59
J60
J61
RN1
RN2
RN3
RN4
RN5
RN6
RN7
RN8
RN9
RN10
P1
P2
SW1
DN8
DN9
DN10
DN11
S1
S2
S3
S4
S5
S6
S7
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R41
R42
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D1
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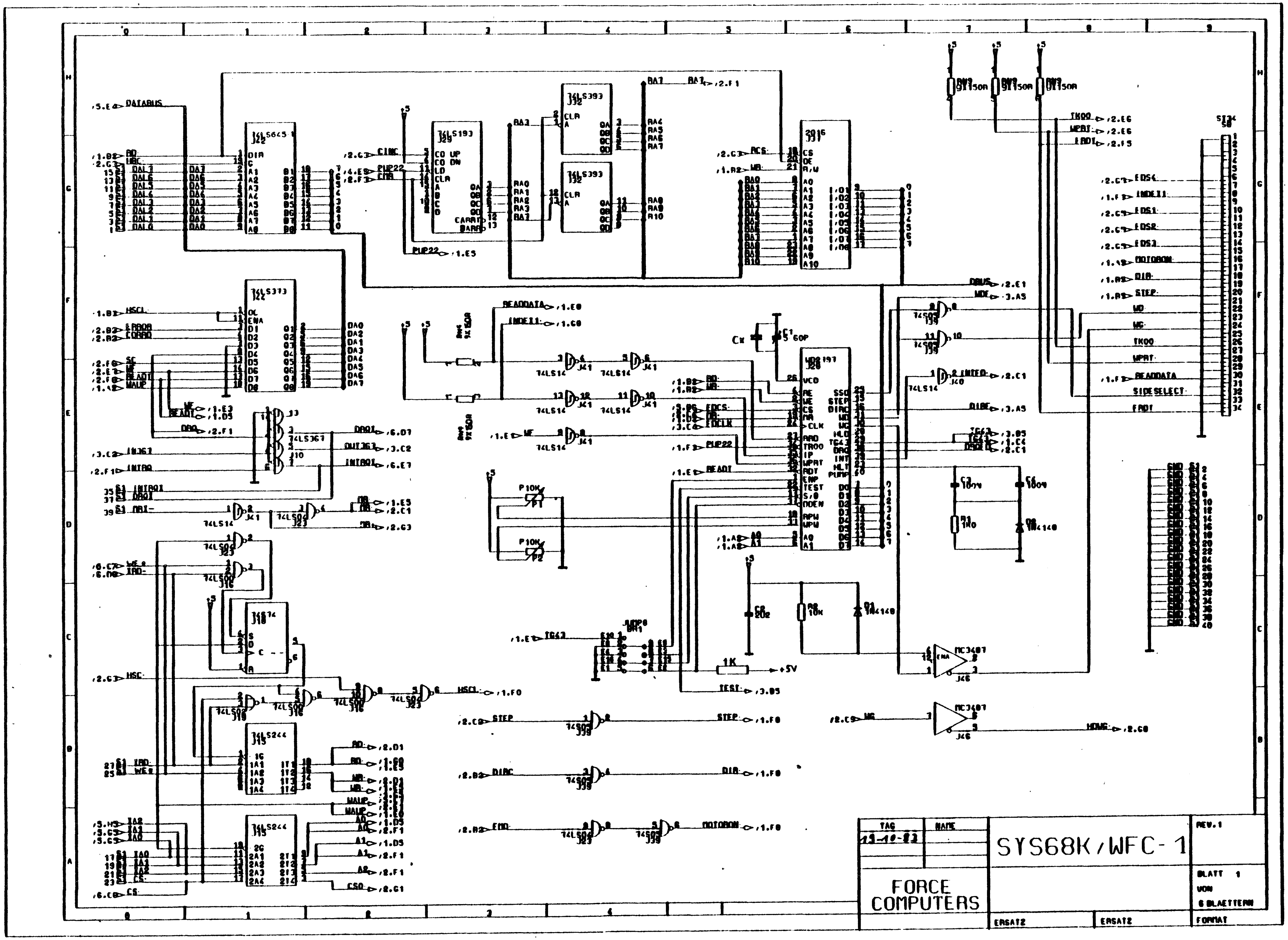
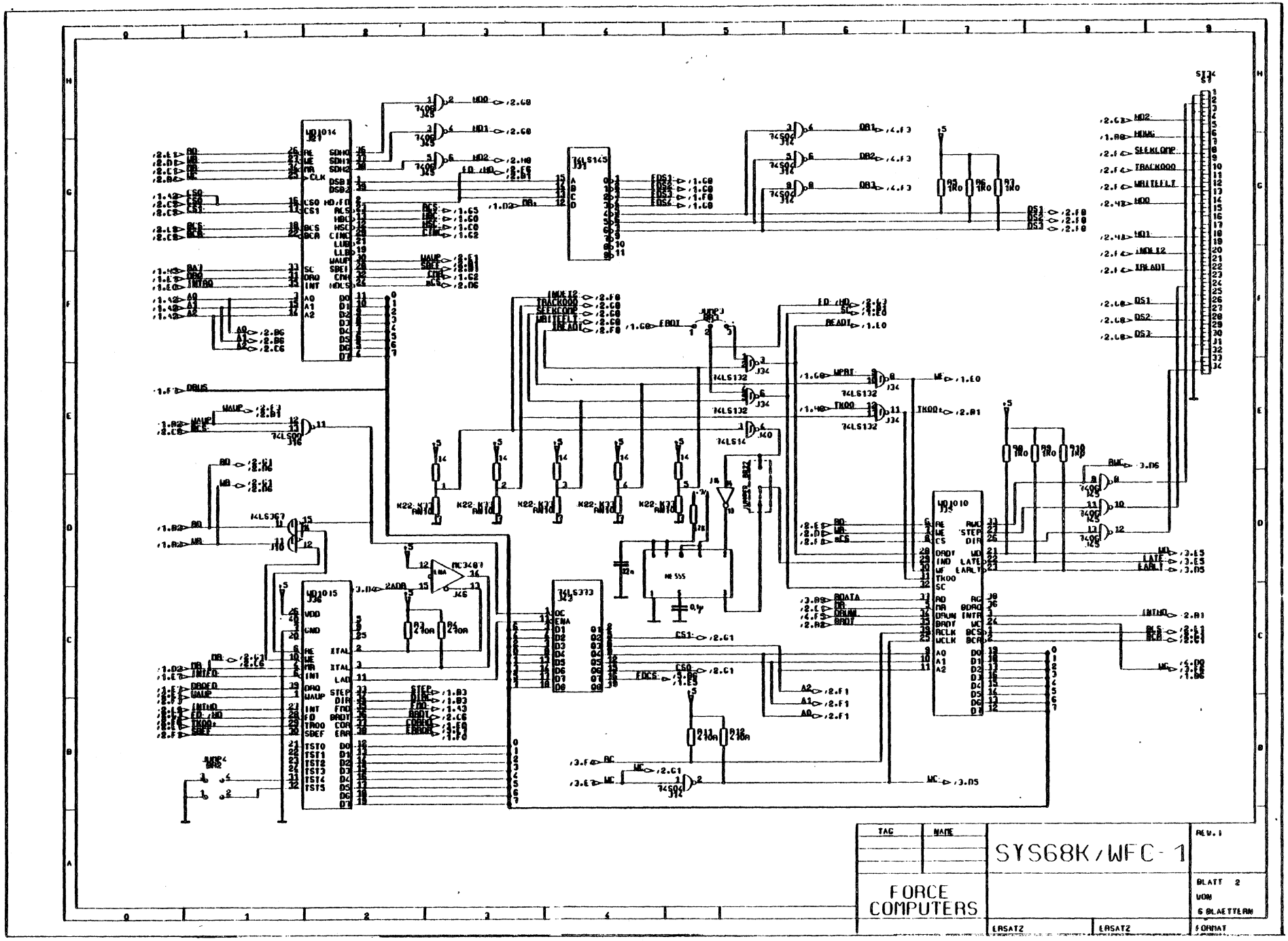
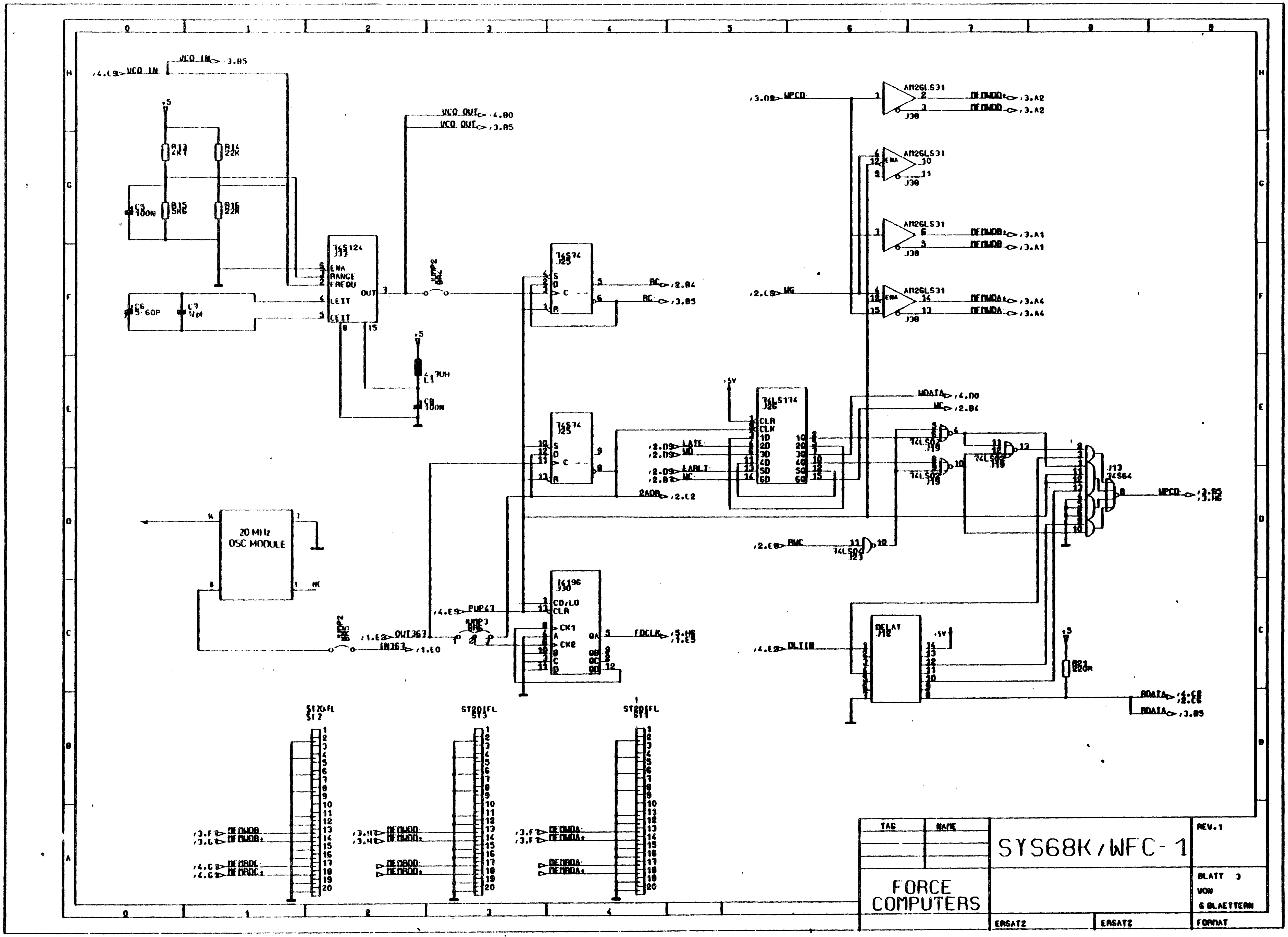
D8
ST1
ST2
ST3


SYS68K/WFC-1
FORCE COMPUTERS
TAG
NAME
REV. 1
BLATT 1
VON
ERSATZ
FORMAT


SYS68K/WFC-1
FORCE COMPUTERS
TAG
NAME
REV. 1
BLATT 2
VON
6 BLAETTERN
ERSATZ
ERSATZ
FORMAT



VCO IN
VCO OUT
74S124
J33
ENA
RANGE
FREQU
CEXT
OUT
R13 2K7
R14 22K
R15 5K6
R16 22K
C5 100N
C6 5-60P
C7 12pF
L1 4.7UH
C8 100N
74S74
J25
BC
WPCD
WG
AM26LS31
J38
MEMWDB
MEMWDA
74LS174
J26
CLR
CLK
LATE
WD
EARLY
WC
2ADR
WDATA
74LS02
J19
74S64
J13
74LS04
J23
RWC
20 MHz
OSC MODULE
74196
J30
CO/LO
CLR
CK1
CK2
PUP43
OUT367
IN363
FDCLK
DLT10
DELAY
J12
R21 220R
RDATA
ST20FL
ST2
ST3
ST1
MEMRDC
MEMRDB
MEMRDA
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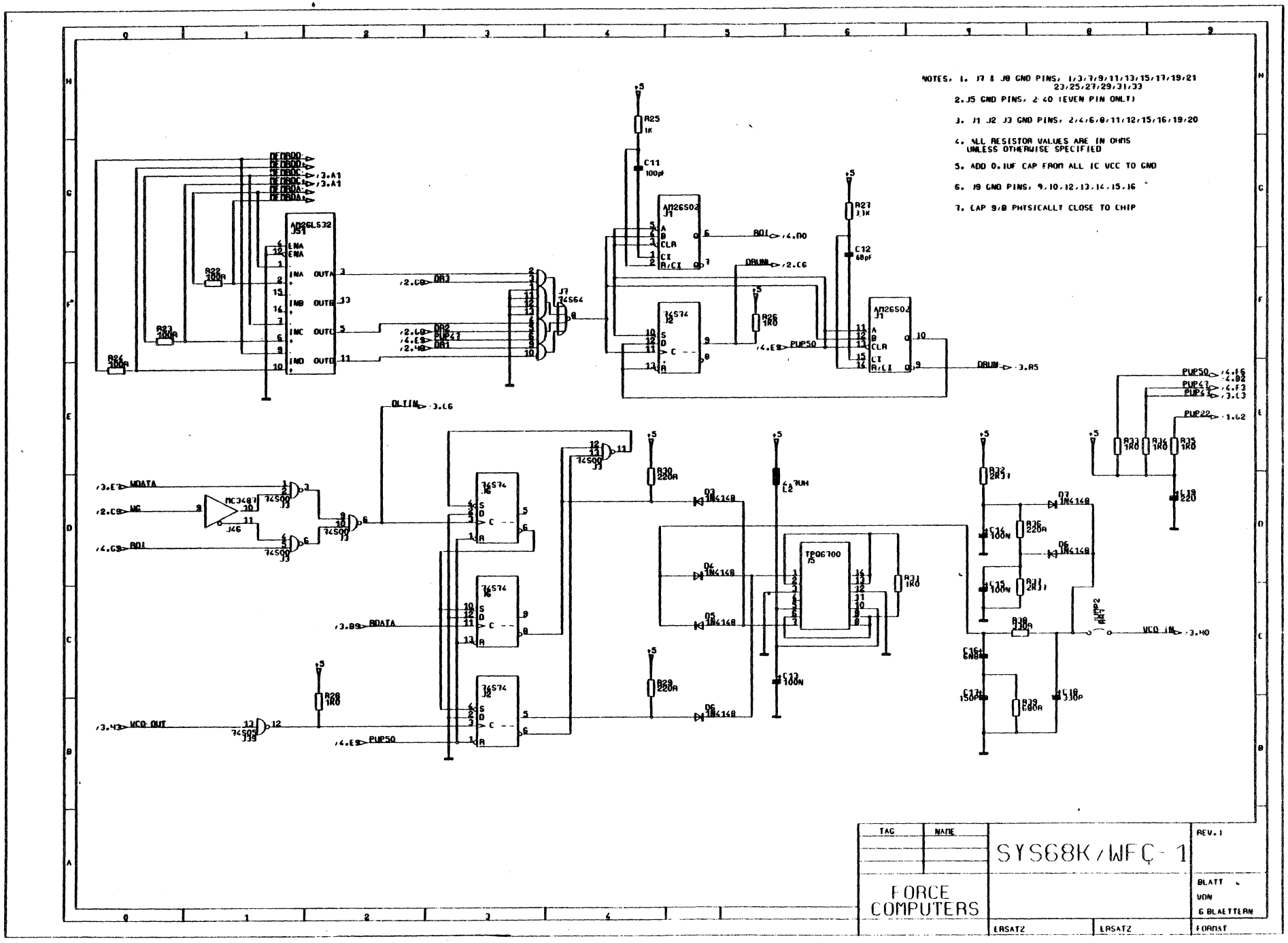
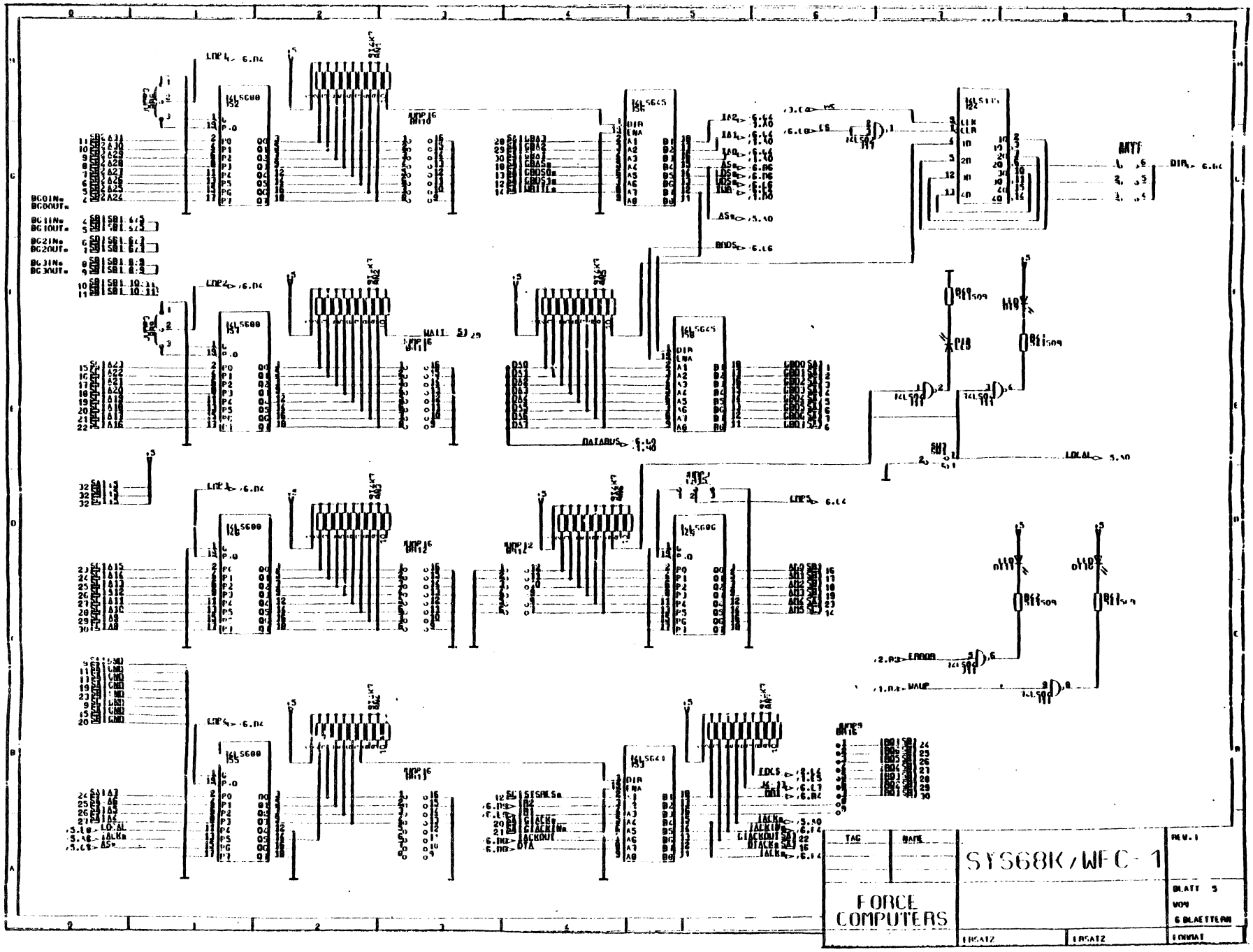
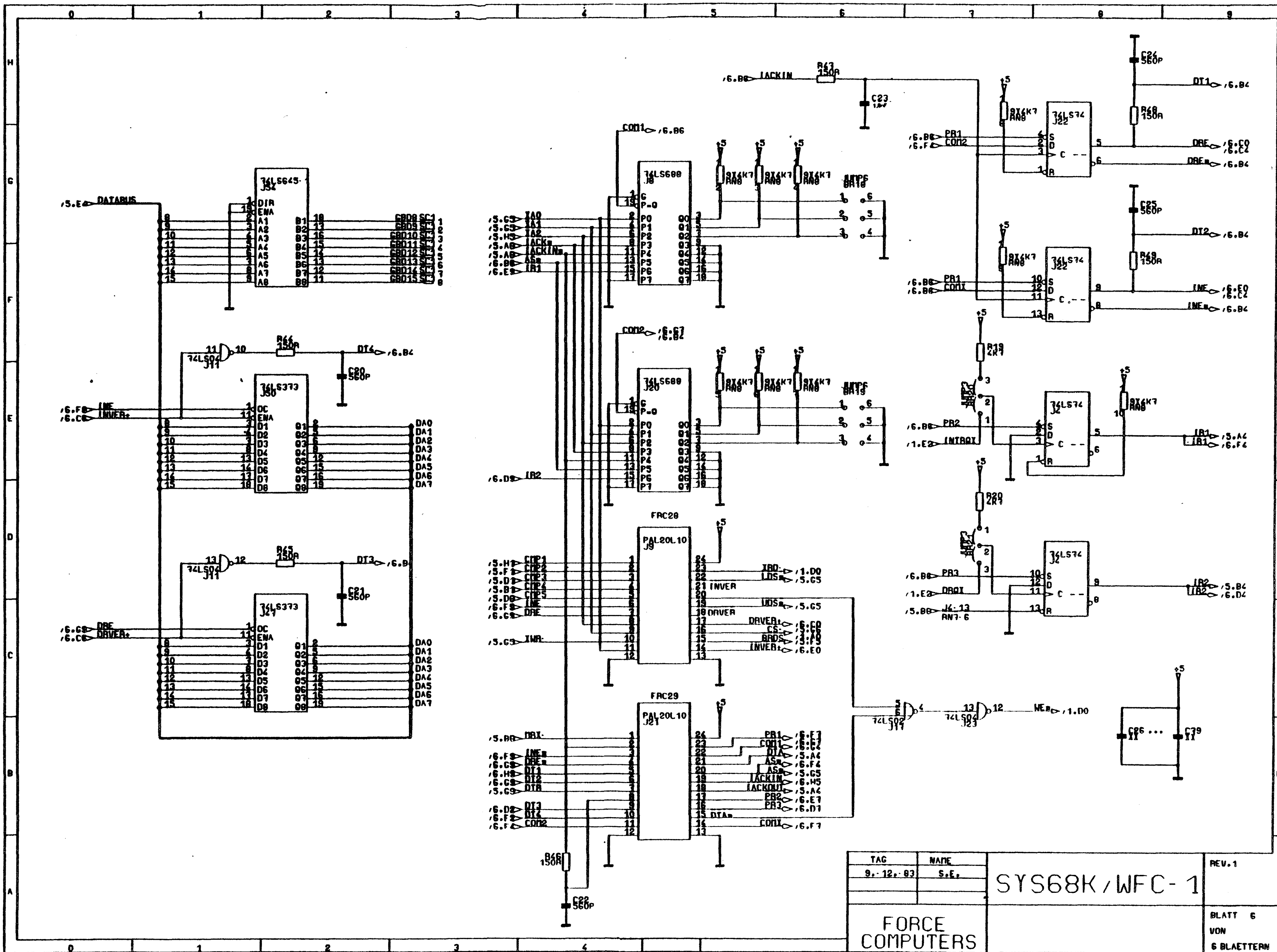
REV.1
FORCE
COMPUTERS
BLATT 3
VON
6 BLAETTERN
ERSATZ
FORMAT


NOTES. 1. J7 & J8 GND PINS, 1/3/7/9/11/13/15/17/19/21
23/25/27/29/31/33
2. J5 GND PINS, 2-40 (EVEN PIN ONLY)
3. J1 J2 J3 GND PINS, 2/4/6/8/11/12/15/16/19/20
4. ALL RESISTOR VALUES ARE IN OHMS
UNLESS OTHERWISE SPECIFIED
5. ADD 0.1UF CAP FROM ALL IC VCC TO GND
6. J9 GND PINS, 9,10,12,13,14,15,16
7. CAP 9/8 PHYSICALLY CLOSE TO CHIP
AM26LS32
AM26S02
74S74
74S64
74S00
MC3487
TPQ6700
1N4148
JUMP2
VCO_IN
VCO_OUT
MDATA
MCLK
RDI
BDATA
DRUN
PUP50
PUP43
PUP41
PUP22
TAG
NAME
SYS68K/WFC-1
REV.1
FORCE COMPUTERS
BLATT
VON
ERSATZ
ERSATZ
FORMAT


SYS68K/WFC-1
FORCE COMPUTERS



TAG	NAME
9. 12. 83	S.E.

SYS68K/WFC-1

REV.1

FORCE COMPUTERS

BLATT 6
VON
6 BLAETTERN

ERSATZ | ERSATZ | FORMAT

APPENDIX "E"

DATA SHEETS

ADVANCE INFORMATION

WESTERN DIGITAL
CORPORATION

WD1010 Winchester Disk Controller

FEATURES

- Compatible with most 8- and 16-bit processors
- Data rate up to 5 Mbits per second
- Multiple sector read/write commands
- Unlimited interleave capability
- Automatic formatting
- Software selectable sector size (128, 256, 512, or 1024 bytes per sector)
- CRC generation/verification
- Automatic retries on all errors
- Automatic restore on seek errors
- Single +5V supply
- Provision for external ECC capability

APPLICATIONS

- Seagate ST506, ST512
- Shugart SA1000, SA1100, SA600
- Tandon 600 Series
- Texas Instruments 506
- RMS 500 Series
- Quantum Q2000 Series
- Miniscribe

. . . and others

DESCRIPTION

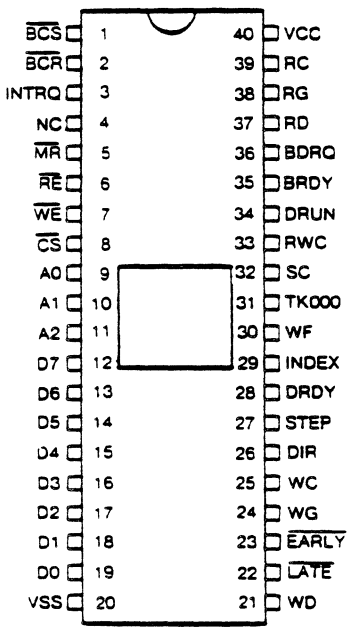
The WD1010 is a MOS/LSI device designed for use with the drives listed above as well as other drives compatible with the SA1000 or ST506 interface. The controller requires only a single +5 volts supply. It is designed to operate with an external sector buffer memory and to interface directly with TTL logic.

The WD1010 is fabricated in NMOS silicon-gate technology and is available in a 40-pin, Dual-in-line ceramic or plastic package.

FUNCTIONAL DESCRIPTION

The WD1010 is software compatible with the WD1000 controller board. Programming is very similar to that of the Western Digital FD179X floppy disk controller.

Data bytes are transferred to or from the buffer every 1.6μsec., with a 5Mbit/sec drive. The buffer may be either the Western Digital WD1510 128x9 FIFO memory (Fig. 1) or a combination of a 256x8 static RAM and a 9 bit resettable counter (Fig. 2). The WD1010 generates control signals to minimize external gating. Buffer to processor transfers are made via programmed I/O or DMA. The controller also generates handshake signals to control DMA operations for multiple sector transfers. The WD1010 interfaces to the Western Digital DM1883 and other DMA controllers.



PIN CONNECTIONS

TABLE 1. INTERFACE SIGNALS

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
12-19	D7-D0	Data 7 - Data 0	Eight bit bidirectional bus used for transfer of commands, status, and data.
6	$\overline{RE}$	READ ENABLE	Tristate bidirectional line, used as an input for reading the task register and an output when WD1010 is reading the buffer.
7	$\overline{WE}$	WRITE ENABLE	Tristate bidirectional line used as an input for writing into the task register and as an output when the WD1010 is writing to the buffer.
9-11	A0-A2	ADDRESS 0 - ADDRESS 2	These three inputs select the register to receive/transmit data on D0-D7.
8	$\overline{CS}$	CHIP SELECT	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals.
3	INTRQ	INTERRUPT REQUEST	Active high output which is set to a logic high in the completion of any command.
5	$\overline{MR}$	MASTER RESET	A logic low in this input will initialize all internal logic.
1	$\overline{BCS}$	BUFFER CHIP SELECT	Active low output used to enable reading or writing of the external sector buffer.
35	BRDY	BUFFER READY	This input is used to inform the controller that the sector buffer is full or empty.
2	$\overline{BCR}$	BUFFER COUNTER RESET	Active low output that is strobed by the WD1010 prior to read/write operations.
36	BDRQ	BUFFER DATA REQUEST	This output is set to initiate data transfers to/from the sector buffer.
40	V_{CC}	+ 5 volt	+ 5V ∓ 5% Power supply input.
20	V_{SS}	GROUND	Ground.
4	NC	NO CONNECTION	This pin must be left open by the user.
21	WD	WRITE DATA	This output contains the MFM clock and data pulses to be written on the disk.
25	WC	WRITE CLOCK	4.34 or 5.0 MHz clock input used to derive all internal write timing.
24	WG	WRITE GATE	This output is set to a logic high before writing is to be performed on the disk.
23, 22	$\overline{EARLY}$, $\overline{LATE}$	EARLY, LATE	Precompensation outputs used to delay the WD pulses externally.
37	RD	READ DATA	Data input from the Drive. Both MFM clocks and data pulses are entered on this pin.
39	RC	READ CLOCK	A normal square wave clock input derived from the external data recovery circuits.
38	RG	READ GATE	This output is set to a logic high when data is being inspected from the disk.
39	DRUN	DATA RUN	This input informs the WD1010 when a field of one's or zeroes have been detected.
27	STEP	STEP PULSE	This output generates a pulse for the stepping motor.
26	DIR	DIRECTION	This output determines the direction of the stepping motor.
28	DRDY	DRIVE READY	This input must be at a logic high in order for commands to execute.
30	WF	WRITE FAULT	An error input to the WD1010 which indicates a fault condition at the drive.
31	TK000	TRACK 000	An input to the WD1010 which indicates that the R/W heads are positioned over the outermost cylinder.

TABLE 1. INTERFACE SIGNALS

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
29	INDEX	INDEX PULSE	A logic high on this input informs the WD1010 when the index hole has been encountered.
33	RWC	REDUCED WRITE CURRENT	This output can be programmed to reduce write current on a selected starting cylinder.
32	SC	SEEK COMPLETE	This input informs the WD1010 when head settling time has expired.

PROCESSOR INTERFACE DESCRIPTION

The WD1010 controller interfaces to a host or I/O processor via an 8 bit bidirectional data bus. The buffer memory is also connected to the data bus. The WD1010 is designed for use with buffer memory and external bus transceivers. One anticipated system configuration is shown in Figure 1. In this system, the processor starts a disk operation by writing task information into the register file in the controller. The task information includes the disk cylinder, head, sector numbers, drive number, track number for start of write precompensation, sector size, and number of sectors to be transferred. After the task information has been written, the processor writes the command into the command register. In the case of a write sector command, the processor can then read the controller status register to inspect the buffer data request flag, and write data into the buffer memory. When the buffer becomes full, it activates the BRDY input of the controller. The controller then deactivates the buffer data request (BDRQ) line and activates the $\overline{BCS}$ line. The buffer chip select ($\overline{BCS}$) line is used both for buffer memory control and for disabling the data bus. $\overline{RE}$ and $\overline{WE}$ buffers. The controller thus has a direct bus to the buffer memory which is isolated from the processor data bus. When the buffered data is transferred to disk and the buffer memory is empty, the controller enables the tristate buffers, thus reconnecting the two busses. The processor can then write more data into the buffer memory.

The WD1010 disk controller generates control signals for RAM-counter control, data bus control, ECC processor and DMA control.

TABLE 2. TASK REGISTER FILE

A2	A1	A0	READ	WRITE
0	0	0	Data	Data
0	0	1	Error Flags	Write Precomp Cyl.
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder No. Low	Cylinder No. Low
1	0	1	Cylinder No. High	Cylinder No. High
1	1	0	SDH	SDH
1	1	1	Status	Command

TABLE 3. SDH REGISTER

SECTOR EXTENSION	SECTOR SIZE		DRIVE* NUMBER		HEAD* NUMBER		
BIT 7	6	5	4	3	2	1	0
1 = ECC 0 = CRC	1	1	128 byte data field				
	0	0	256 byte data field				
	0	1	512 byte data field				
	1	0	1024 byte data field				

*Drive Number and Head Number must be externally decoded and latched.

DRIVE INTERFACE DESCRIPTION

The WD1010 disk controller is designed to interface to SA1000 Winchester disk drives. Winchester drives with similar interfaces, such as the Seagate Technology ST506, can also be controlled.

The WD1010 contains MFM encoder/decoder, address mark detector, and high speed shift register circuitry. Signals are provided to control write precompensation and write splice avoidance. External circuitry must provide a phase locked MFM read clock and high frequency detection. Figure 1 shows a typical controller-drive interface for a system with two Winchester disk drives.

WD1010 inputs are TTL compatible unless otherwise noted. WD1010 outputs will drive one TTL unit load.

STATUS BIT DESCRIPTION

Busy — Active when controller is accessing the disk. Activated by start of command (writing into command register). Deactivated at end of all except read sector. For read sector, Busy is deactivated when a sector of data has been transferred to buffer.

Drive Ready — Normally reflects the state of DRDY pin. After an error interrupt, the state of DRDY is frozen until the status register is read. The DRDY bit then reflects the state of the DRDY pin. An interrupt is generated when reset.

Write Fault — Reflects the state of the WF pin. An interrupt is generated when set.

Seek Complete — Reflects the state of the SC pin.

Data Request — Reflects the state of the BDRQ pin. When active, indicates that a buffer data transfer is desired. The data request flag is used for programmed I/O while the BDRQ pin is used for DMA controlled I/O.

Command in Progress — Indicates that a command is in progress.

Error — Indicates that a bit in the error register has been set.

ERROR BIT DESCRIPTION

Bad Block — A bad block address mark has been detected when trying to read or write that sector.

Data Field CRC Error — An error in the data field has been detected. The sector can be re-read to attempt recovery from a soft error. The data contained in the buffer can be read but contains errors.

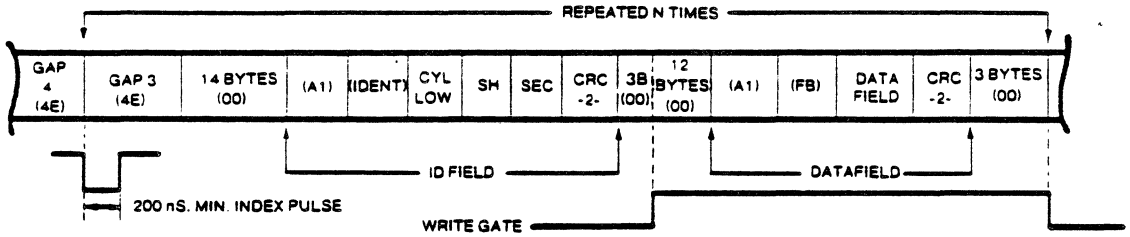
ID Not Found — Occurs when cylinder, head, sector, or size parameters cannot be found after 16 index pulses have been encountered.

TK000 Error — Occurs when track 0 not found in a Restore command after 1024 stepping pulses.

Aborted Command — Set if command was started and one of the following conditions occurred:

1. Drive not ready
2. Write fault
3. Seek complete not active within 16 index pulses
4. Illegal command code

Data AM Not Found — During a read command, the ID field for the desired sector has been found, but the data field address mark was not found. The data AM should be found within 15 bytes after the ID field. Refer to Figure 3 for track format.



NOTE:

1) When MSB of head byte = 1, bad block is detected.
2) Write Gate turn-on is 3 bytes after the ID field's CRC bytes.
3) Write Gate turn-off is 3 bytes after the Data Field's CRC bytes.
4) 12 bytes of zeroes are re-written on a Data Field update.
5) The 2 LSB's of the IDENT byte are used for Cylinder high. These values are:
   FF = 0 to 255 cylinders
   FF = 256 to 511 cylinders
   FC = 512 to 767 cylinders
   FD 768 to 1023 cylinders
6) GAP 3 length is programmable and may range from 3 bytes to 255 bytes.

FIGURE 3
TRACK FORMAT

TABLE 4. STATUS/ERROR REGISTERS

BIT	STATUS REGISTER	ERROR REGISTER
MSB 7	BUSY	Bad Block
6	DRIVE READY	Data Field CRC
5	WRITE FAULT	Reserved (= 0)
4	SEEK COMPLETE	ID Not Found
3	DATA REQUEST	Reserved (= 0)
2	RESERVED (= 0)	Aborted Command
1	COMMAND IN PROGRESS	TK000 Error
LSB 0	ERROR	Data AM Not Found

TABLE 5. COMMAND REGISTER

COMMAND	MSB 7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	R3	R2	R1	R0
SEEK	0	1	1	1	R3	R2	R1	R0
READ SECTOR	0	0	1	0	D	M	0	0
WRITE SECTOR	0	0	1	1	0	M	0	0
SCAN ID	0	1	0	0	0	0	0	0
WRITE FORMAT	0	1	0	1	0	0	0	0

D = 1 for DMA; 0 for Programmed I/O
M = 1 for multiple sector read or write

R3 R2 R1 R0 =
- 0000 : Step time = 20 us
- 0001 : Step time = .5 ms
- 0010 : Step time = 1.0 ms
- 0011 : Step time = 1.5 ms
- 1111 : Step time = 7.5 ms

for 5 MHz write clock

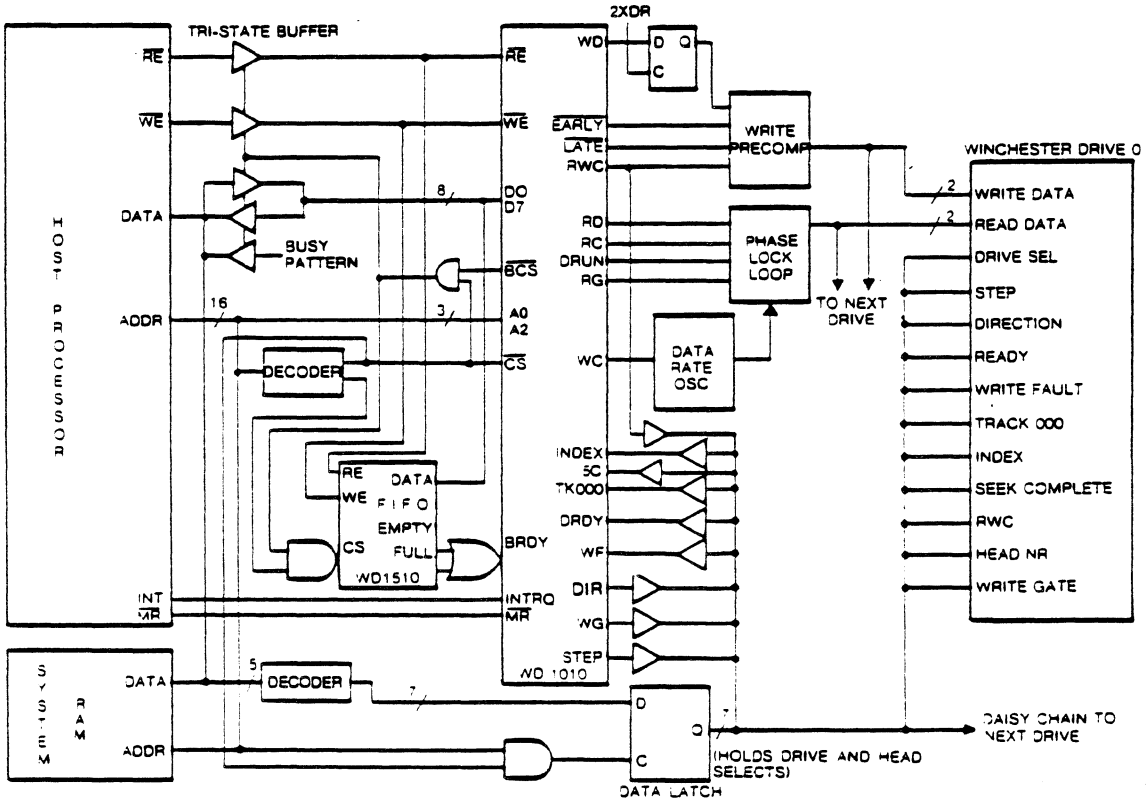


FIGURE 1.

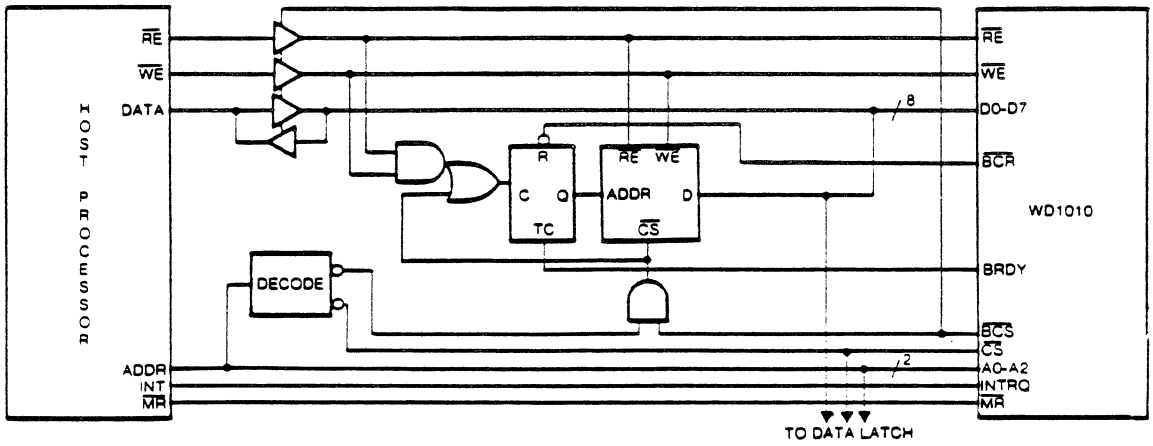


FIGURE 2.

See page 725 for ordering information.

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WESTERN DIGITAL
CORPORATION

ADVANCE INFORMATION

WD1014 Buffer Manager/Error Correction Device

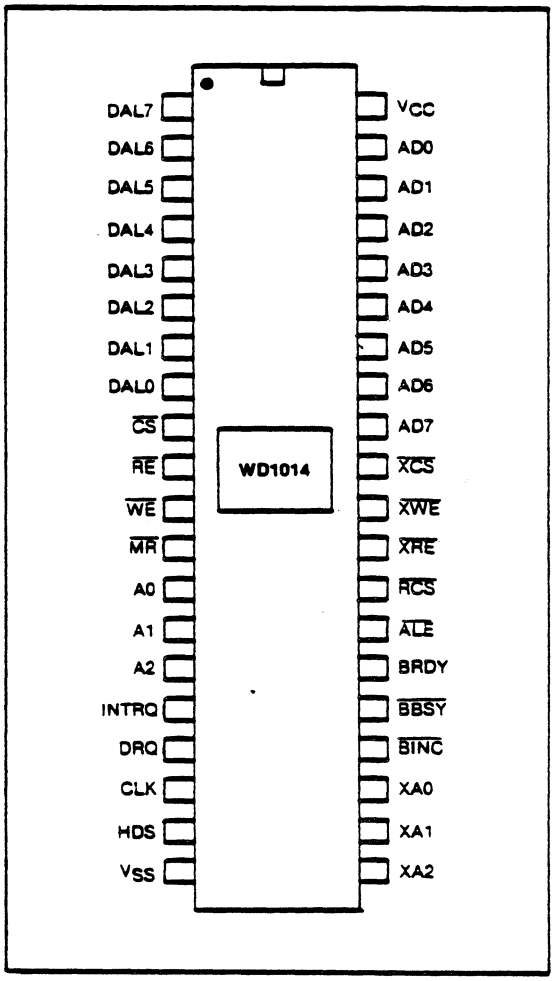
FEATURES

- DIRECT INTERFACE TO THE WD1010
- 32 AND 56 BIT ECC POLYNOMIALS
- 128, 256, 512, OR 1024 BYTE SECTORS
- BUFFER SIZE UP TO 32K BYTES
- CONTROL FOR 4 DRIVES/8 HEADS EACH
- AUTOMATIC RETRY ON ECC ERRORS
- TRANSPARENT ECC CORRECTION
- MULTI-SECTOR READ/WRITE CAPABILITY
- DMA OR PROGRAMMED I/O OPERATION
- 8-BIT TRI-STATE DATA BUS
- EXECUTES 11 MACRO-COMMANDS
- SINGLE +5V SUPPLY

GENERAL DESCRIPTION

The WD1014 is a single chip Buffer Manager/ECC device designed for use with the Western Digital Corp. WD1010 Hard Disk Controller. The device implements all of the logic required for a variable length sector buffer, ECC correction and Host interface circuitry. Use of the BMEC greatly reduces the complexity of the interface design, device count, board size requirements and increases system reliability.

The WD1014 operates from a single +5V supply and is available in a 40 pin plastic or ceramic Dual-in-Line package.



PIN DESIGNATIONS

PIN NUMBER	SYMBOL	DESCRIPTION
1-8	DAL7-0	Data Access Lines. Commands, status, and data to and from buffer are transferred over this tristate bidirectional data bus controlled by the host. DAL7 is MSB.
9	$\overline{CS}$	Chip Select must be active for all communications with the BMEC.
10	$\overline{RE}$	Read Enable. For reading data and status information from the BMEC.
11	$\overline{WE}$	Write Enable. For writing commands and data to the BMEC.
12	$\overline{MR}$	Master Reset. Initializes the BMEC and clears the status flags when activated.
13-15	A0-2	Address inputs. Used to select task file registers and data buffer. A2, A1, A0 = 000 selects buffer. A2 is MSB.
16	INTRQ	INTerrupt ReQuest. Activated whenever a command has been completed. It is reset when the status register is read, or when a new command is loaded via DAL7-0.
17	DRQ	Data ReQuest. Set whenever the buffer contains data to be read by the host or is awaiting data to be written by the host.
18	CLK	Clock signal input used for all internal timing.
19	HDS	Head & Drive Select for setting HS0-3 and DS1-4.
20	V_{SS}	GROUND
21-23	XA2-0	These address lines are used to address the disk controller when $\overline{XCS}$ = 0.
24	$\overline{BCINC}$	Buffer Counter INCrement. Increments the external buffer counter. Each negative transition is a one byte count.
25	$\overline{BBSY}$	Buffer BuSY. Signals the BMEC that the buffer is being accessed by the disk controller. It is also used to control AD0-7 bus switching and tristate $\overline{XWE}$, and $\overline{XRE}$ when it is active.
26	BRDY	Buffer ReaDY output. Signals the disk controller when the buffer memory is ready for controller data transfers. It is active when the buffer memory is full or empty.
27	$\overline{ALE}$	Address Latch Enable. Used to set the external buffer address whenever the buffer is not being accessed by the WD1010 processor.
28	$\overline{RCS}$	Ram Chip Select. Asserted when the BMEC or host accesses the external buffer.
29	$\overline{XRE}$	Tristate line activated only when $\overline{BBSY}$ = high. When $\overline{XCS}$ is low, information is read from the selected WD1010 task files registers. When $\overline{RCS}$ is low, data is read from the buffer.
30	$\overline{XWE}$	Tristate line activated only when BBSY = high. When $\overline{XCS}$ is low, command or task file information is written into the disk controller. When $\overline{RCS}$ is low data is written into the buffer.
31	$\overline{XCS}$	This Chip Select is used to access the disk controller.
32-39	AD7-0	Address or Data bus shared by the buffer, BMEC and the WD1010. While ALE is active a new buffer address is latched in an external counter, where AD7 = A14 and AD0 = A7. This allows buffer sizes from 128 bytes to 32K bytes.
40	V_{CC}	+5 ± 5% volt power supply.

FUNCTIONAL DESCRIPTION

The BMEC is designed to interface directly with industry standard static RAM chips and common TTL/LS latches and counters. The sector buffer, an integral part of the WD1010 system architecture, is addressed by a multiplexed data/address bus (AD0-7), which is also shared by the WD1010 and drive/head control latches. The WD1014 manages the external sector buffer so that it can support all WD1010 sector sizes in single and multiple sector operations. All buffer control signals required by the WD1010 are produced by the BMEC so that no external logic is required to interface the WD1010 to the BMEC.

During sector reads and writes, the BMEC produces an Error Correction Code (ECC) as data is transferred to and from the buffer. The user may select either a 32 or 56 bit polynomial depending upon his needs. Errors are detected and corrected without intervention by the host. The BMEC controls all retries on data ECC errors for the host as well. Corrected errors are reported as a status to the host. Uncorrectable errors are reported by setting the error bit in the status register with the appropriate descriptor bit set in the error register.

TASK FILE

The task file is a set of registers which contain commands, status, track, sector and other task information. Nine registers are accessed via A2 to A0 during read and write modes. Depending on the command from the host and the status of the system, the proper information is stored to or read from the task file.

A2	A1	A0	READ	WRITE
1	1	1	Status	Command
0	0	1	Error flags	Write Precomp Cylinder
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder Number (low)	Cylinder Number (low)
1	0	1	Cylinder Number (high)	Cylinder Number (high)
1	1	0	S D H*	S D H*

*S D H bytes specifies sector size, drive number and head number.

The SDH register is coded as follows:

Bit 7 (MSB) is set for a 7 byte sector extension (used for ECC bytes).

Bits 6 and 5 contain the sector size.

The possible sector sizes and their selection codes are:

BIT 6	BIT 5	SECTOR SIZE
1	1	128 byte data field
0	0	256 byte data field
0	1	512 byte data field
1	0	1024 byte data field

Bits 4 and 3 specify Drive Number. These bits are decoded internally and latched externally to perform the select function.

Bits 2, 1 and 0 specify Head Number.

COMMAND REGISTER

The command register is accessed by writing into register 7. All other task information should be loaded into the task file before loading the command register. Command execution starts immediately after the command register is loaded and subsequent register loads are ignored until the command is done. The commands are as follows:

COMMAND	MSB	7	6	5	4	3	2	1	0
		BIT CODE							
Restore		0	0	0	1	R3	R2	R1	R_0
Seek		0	1	1	1	R3	R2	R1	R_0
Read Sector		0	0	1	0	D	M	0	E
Write Sector		0	0	1	1	0	M	0	E
Scan ID		0	1	0	0	0	0	0	0
Write Format		0	1	0	1	0	0	0	0
Read Copy		1	0	1	0	0	M	0	E
Write Copy		1	0	1	1	0	M	0	E
Read Long		0	1	1	0	D	0	1	E
Write Long		0	1	1	1	D	0	1	E
Set Parameters		1	1	0	1	0	0	0	0

D = 1: Interrupt for DMA mode
D = 0: Interrupt for programmed I/O mode
M = 1: Multiple Sector Read or Write
E = 1: Select 56 bit ECC polynomial
E = 0: Select 32 bit ECC polynomial

R3 R2 R1 R0 =
0000 : Step time = 20μs
0001 : Step time = .5ms
0010 : Step time = 1.0ms
0011 : Step time = 1.5ms
:
:
1111 : Step time = 7.5ms for 5 MHz write clock

THE STATUS AND ERROR REGISTERS

The Status Register indicates to the host the status of the system. If the Error bit in the Status Register is set, one or more bits in the Error Register will be set. The meaning of the these bits is shown below:

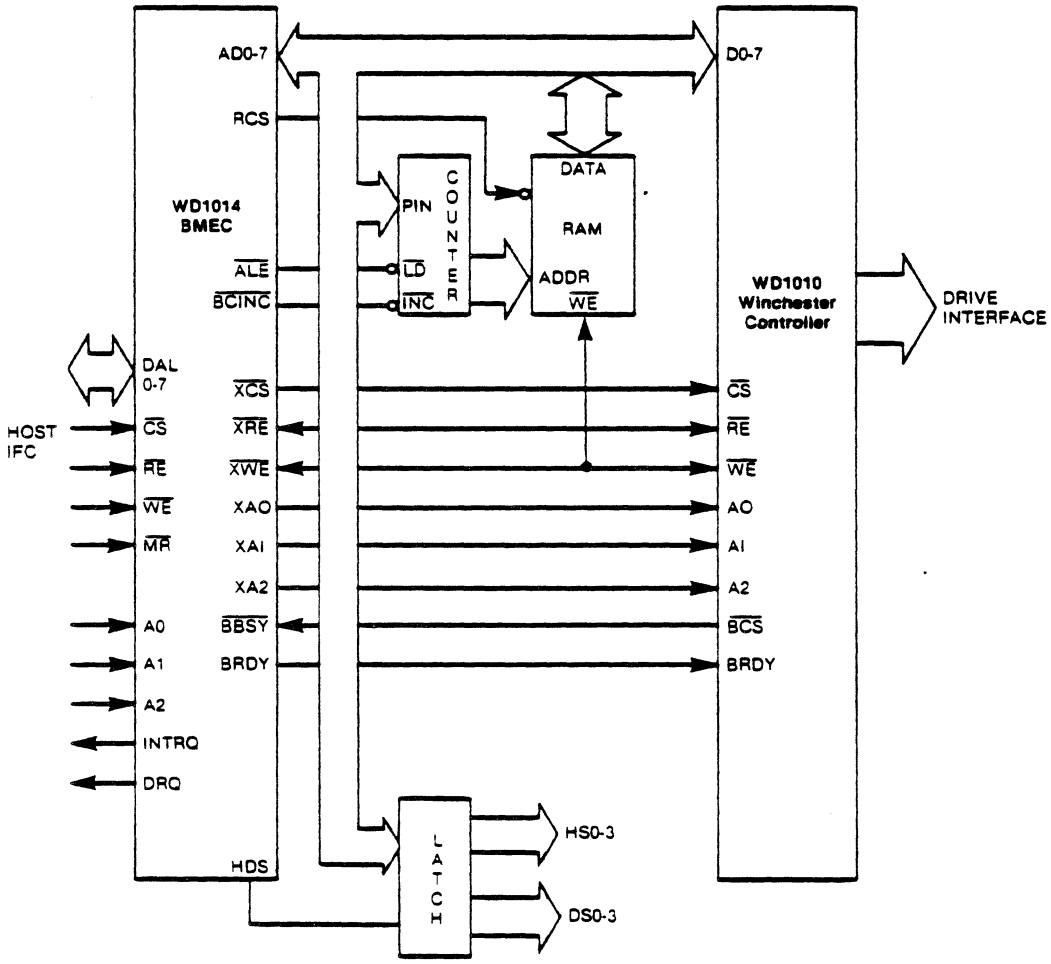
BIT	STATUS REGISTER	ERROR REGISTER
MSB 7	Busy	Bad Block Detect
6	Drive ready	Uncorrectable
5	Write fault	CRC Error — ID Field
4	Seek complete	ID Not Found
3	Data request	—
2	Data Error Corrected	Aborted Command
1	Command in progress	TR000 Error
LSB 0	Error	DAM Not Found

COMMAND DESCRIPTIONS

The BMEC passes on all information between the host and the WD1010. Some commands are modified by the BMEC and some are simply echoed. The following is a list of the commands and their formats and descriptions.

COMMAND	FORMAT	DESCRIPTION
RESTORE	0 0 0 0 R3 R2 R1 R0	Pass on task information and command and initiates a read status after the command is completed. The command is echoed. Stepping rate (R0-R3) is set.
SEEK	0 1 1 0 R3 R2 R1 R0	Pass on task information and command and initiates a read status after the command is completed. The command is echoed. Stepping rate (R0-R3) is set.
SCAN ID	0 1 0 0 0 0 0 0	Passes command to WD1010 which scans ID headers on current track. Updates cylinder number in task file and command and initiates a read status after the command is completed. The command is echoed.
READ SECTOR	0 0 1 0 D M 0 E	Write the buffer with data from WD1010. If ECC is enabled, ECC bytes are recomputed by the BMEC. After the buffer is full, the recorded ECC bytes are compared to the generated bytes to generate the syndrome bytes. If the syndrome is non-zero, errors have occurred and error correction is invoked by the BMEC. If the error is not correctable the BMEC retries the sector read. If the data is correctable the BMEC corrects the data and passes the data in the buffer to the host. Read status is requested by the BMEC and is sent from the WD1010 to the host. If, after a specified number of retries, the error is still uncorrectable, the BMEC sends an error status to the host along wtih the status from the WD1010.
WRITE SECTOR	0 0 1 1 0 M 0 E	Write the buffer with data bytes from the host. Pass the task information and command to the WD1010. The WD1010 seeks track if necessary, then writes the sector from the buffer to disk. Generate the ECC polynomial, selected by E, as the buffer is written to disc. Write the total number of sectors specified by the sector count if M = 1 in format. If M = 0 then the sector count is ignored and only one sector is written. After the sector data is written to the disc, the BMEC sends the WD1010 the ECC bytes. The BMEC requests status from the WD1010 and passes on this information to the host at the host's request.
READ LONG	0 1 1 0 D 0 1 E	Similar to Read Sector except the ECC operation producing a syndrome is inhibited in the BMEC. Instead, the BMEC copies the recorded ECC bytes from disc and passes them unaltered to the host.
WRITE LONG	0 1 1 1 D 0 1 E	The Write Long command functions similarly to the Write Sector command except the ECC operation of computing the ECC word is inhibited in the BMEC. Instead, the BMEC accepts a 32, or 56 bit appendage from the host and passes it unaltered to the WD1010 to be written on the disc after the data.
WRITE COPY	1 0 1 1 0 M 0 E	The Write Copy command is similar to the Write Sector command, except the BMEC does not send a data request (DRQ) to the host at the beginning of the command. The BMEC assumes it has a full buffer to write to the disc. The buffer could have been filled by another device other than the host, such as a back-up tape or data from another disc. This commands allows the copying of data from one disc to another with minimal host intervention.

COMMAND	FORMAT	DESCRIPTION
READ COPY	1 0 1 0 0 M 0 E	The Read Copy command is similar to the Read Sector command, except the BMEC does not send a data request (DRQ) to the host at the end of the command. This command, when used with the Write Copy command, allows the copying of data from one disk to another with minimal host intervention.
SET PARAMETERS	1 1 0 1 0 0 0 0	The buffer size parameter is specified by the value held in the sector size task register. The buffer size corresponds to the sector size task register value multiplied by 128. (E.G. if the sector size task register value = 1, then it specifies a buffer size of 128 bytes. A 32768 (32K) byte length buffer is specified by a sector size register value = 0.)



WD1010/WD1014 WINCHESTER CONTROLLER

See page 725 for ordering information.

Printed in U.S.A.

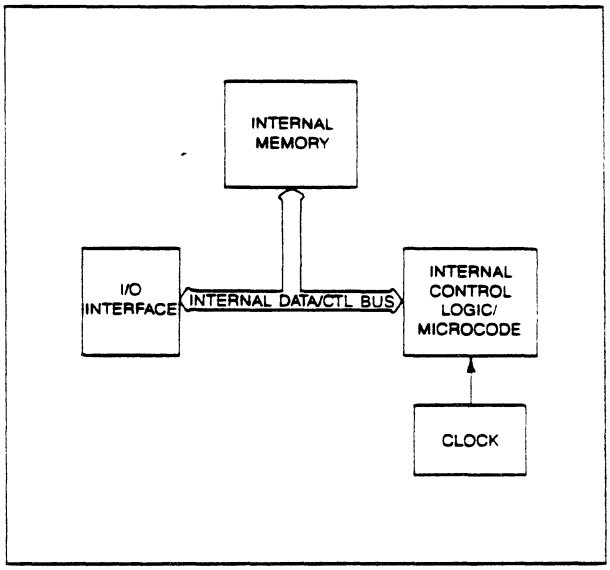
WESTERN DIGITAL
CORPORATION

NEW PRODUCT BULLETIN

Buffer Manager Control Processor WD1015

FEATURES

- SINGLE +5V POWER SUPPLY
- COMPLETE BUFFER MANAGER
- PROGRAMMABLE SECTOR SIZES — 128, 256, 512, OR 1024 BYTES
- ECC BURST ERROR CORRECTION UP TO 5 BITS ON HARD DISK DATA
- 8 BIT MULTIPLEXED ADDRESS/DATA I/O BUS
- FLOPPY DISK COMMAND TRANSLATION
- SUPPORTS MOTOR ON OR HEAD LOAD DRIVES
- SUPPORTS 250 OR 500 KBS FLOPPIES
- BUFFERED SEEKS WITH FLOPPIES AND WINCHESTERS
- 16 POPULAR STEPPING RATES AVAILABLE
- AUTOMATIC RETRIES ON ALL ERRORS WITH SIMULATED COMPLETION
- POWER-ON DIAGNOSTICS INCLUDED
- 10 MHZ CLOCK RATE
- 40 PIN DIP PACKAGE



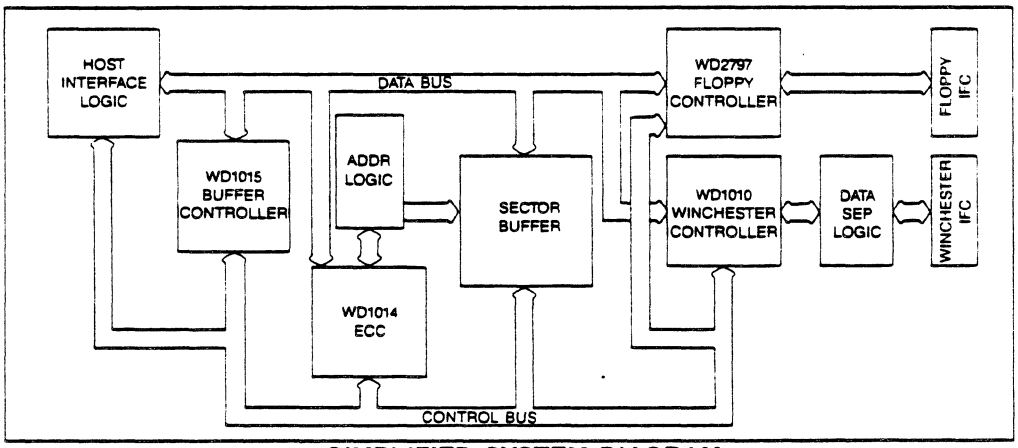
WD1015 BLOCK DIAGRAM

DESCRIPTION

The WD1015 is a complete Control Processor (CP) that is used to handle all aspects of buffer management, in conjuction with the EDS (WD1014) device, for the Winchester/Floppy Controller (WFC) board (WD1002-05). It executes all of the commands used by the WD1002-05 and does all of the control required except for real time processing, which is done by the WD1014. The WD1015 is programmed to control the transfer of information within the WFC and maintain the necessary copies of the task files for both drives.

PROPOSED APPLICATIONS

The WD1015 can be used as part of a proprietary chip set consisting of WD1010, WD1014, and WD2797 as in the WD1002-05 Winchester/Floppy Disk Controller board illustrated below;



SIMPLIFIED SYSTEM DIAGRAM

July, 1983

2445 McCabe Way
Irvine, California 92714
(714) 557-3550, TWX 910-595-1139

WD279X-02 Floppy Disk Formatter/Controller Family

FEATURES

- ON-CHIP PLL DATA SEPARATOR
- ON-CHIP WRITE PRECOMPENSATION LOGIC
- SINGLE +5V SUPPLY
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 (FM)
  - IBM 34 (MFM)
- AUTOMATIC SEEK WITH VERIFY
- MULTIPLE SECTOR READ/WRITE
- TTL COMPATIBLE
- PROGRAMMABLE CONTROL
  - SELECTABLE TRACK-TO-TRACK ACCESS
  - HEAD LOAD TIMING
- SOFTWARE COMPATIBLE WITH THE FD179X SERIES
- SOFT SECTOR FORMAT COMPATIBILITY

APPLICATIONS

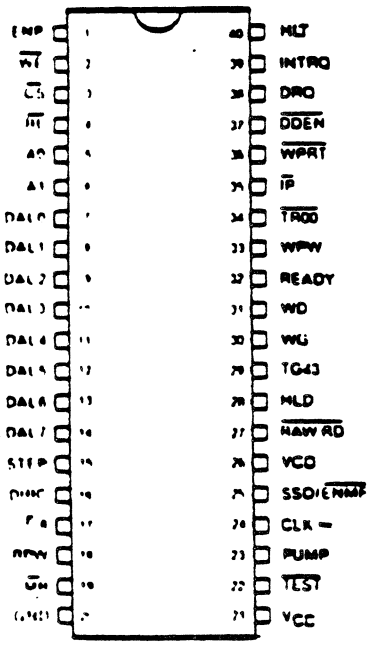
8" FLOPPY AND 5¼" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY
CONTROLLER/FORMATTER

The WD279X Family are MOS/LSI devices which perform the functions of a Floppy Disk Controller/Formatter. Software compatible with its predecessor, the FD179X, the device also contains a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic.

When operating in Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. An on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

The WD279X is fabricated in NMOS silicon gate technology and available in a 40 pin dual-in-line ceramic or plastic package.

FEATURES	2791	2793	2795	2797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Side Select Out			X	X
Internal CLK Divide	X	X		



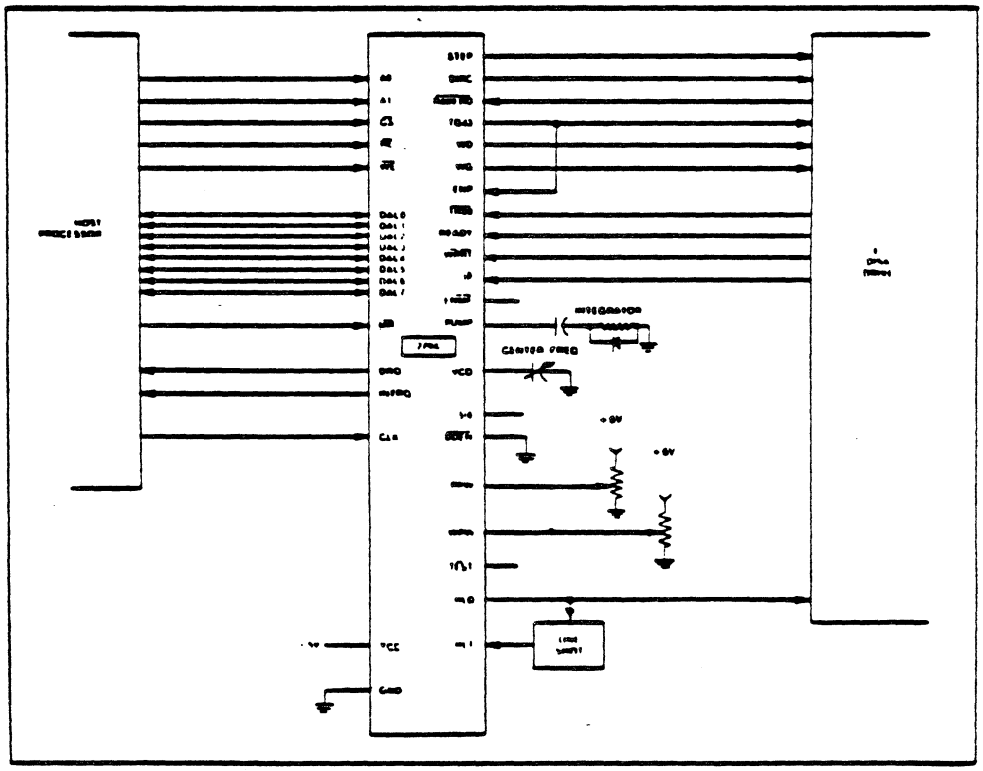


Figure 1.

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	ENABLE PRECOMP	ENP	A Logic high on this input enables write precompensation to be performed on the Write Data output.
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5, 6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: $\overline{CS}$ A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit bi-directional bus used for transfer of commands, status, and data. These lines are inverted (active low) on WD2791 and WD2795.
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz ± 1% for 8" drives, 1 MHz ± 1% for mini-floppies.
38	DATA REQUEST	DRQ	This output indicates that the Data Register contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR.
39	INTERRUPT REQUEST	INTRQ	This output is set at the completion of any command and is reset when the Status register is read or the Command register is written to.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	5¼," 8" SELECT	$\overline{5/8}$	This input selects the internal VCO frequency for use with 5¼" drives or 8" drives.
18	READ PULSE WIDTH	RPW	An external potentiometer tied to this input controls the phase comparator within the data separator.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	A logic low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins.
23	PUMP	PUMP	High-impedance output signal which is forced high or low to increase/decrease the VCO frequency.
25	ENABLE MINI-FLOPPY (2791, 2793)	$\overline{\text{ENMF}}$	A logic low on this input enables an internal ÷2 of the Master Clock when $\overline{5/8}$ is also at a logic 0. This allows both 5¼" and 8" drive operation with a single 2 MHz clock. For a 1 MHz clock on Pin 24, this line must be left open or tied to a Logic 1.
25	SIDE SELECT OUTPUT (2795, 2797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	VOLTAGE-CONTROLLED OSCILLATOR	VCO	An external capacitor tied to this pin adjusts the VCO center frequency.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	A 250ns (MFM) or 500 ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	WRITE PRECOMP WIDTH	WPW	An external potentiometer tied to this input controls the amount of delay in Write precompensation mode.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the WD279X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the WD279X when the index hole is encountered on the diskette.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
36	WRITE PROTECT	WPRT	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	DDEN	This input pin selects either single or double density operation. When DDEN = 0, double density is selected. When DDEN = 1, single density is selected.
40	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.

GENERAL DESCRIPTION

The WD279X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The WD279X, which can be considered the end result of both the FD1771 and FD179X designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The WD279X contains all the features of its predecessor the FD179X plus a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic. In Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the FD1771, FD179X and WD279X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The WD279X is set up to operate on a multiplexed bus with other bus-oriented devices.

The WD279X is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads. The 2793 is identical to the 2791 except the DAL lines are TRUE for systems that utilize true data busses.

The 2795/7 has a side select output for controlling double sided drives.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations in Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

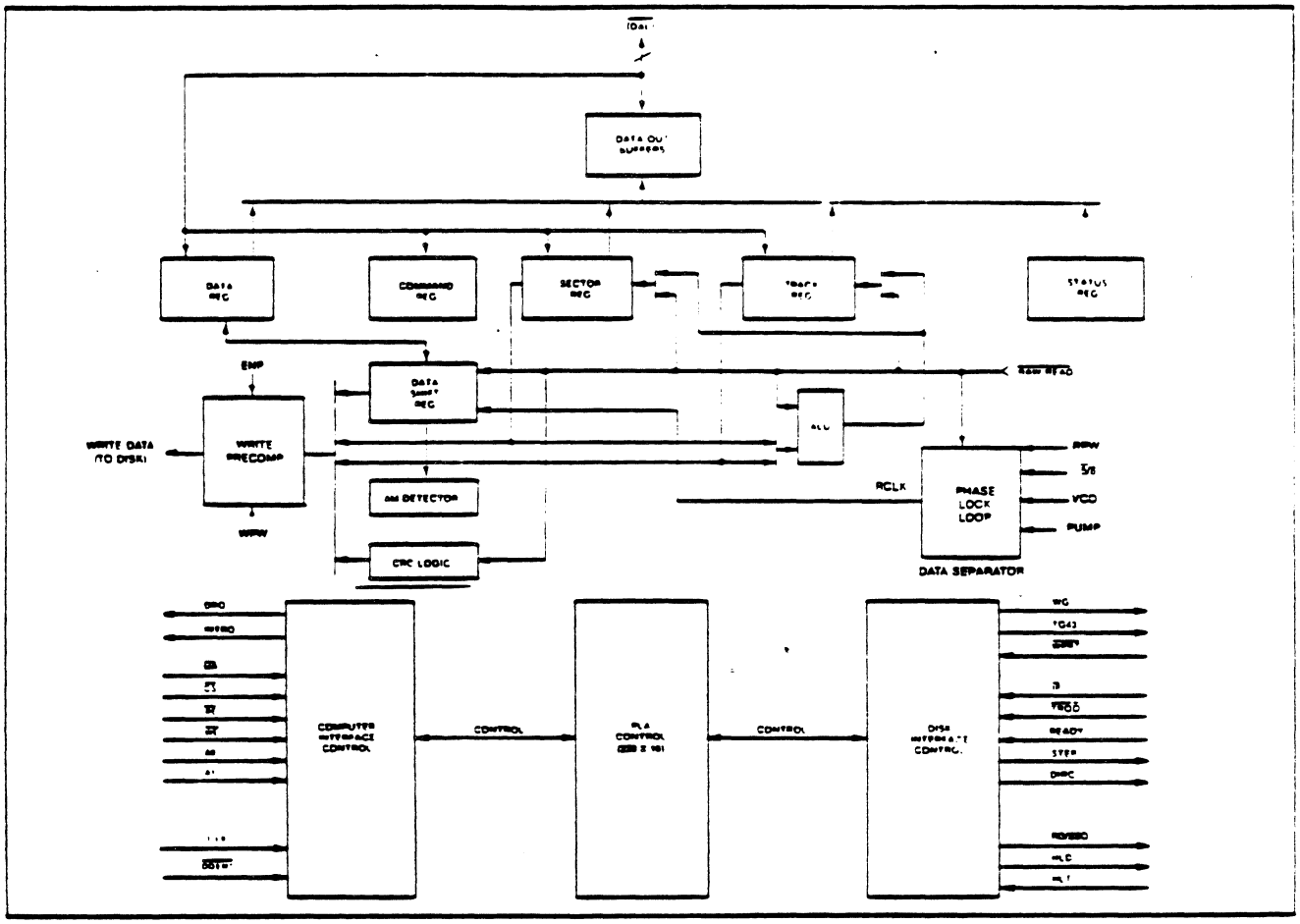
The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

Write Precompensation — enables write precompensation to be performed on the Write Data output.



WD279X BLOCK DIAGRAM

Data Separator — a high performance Phase-Lock-Loop Data Separator with on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the WD279X. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD279X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 279X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, Single Density (FM) is selected. When $\overline{DDEN}$ = 0, Double Density (MFM) is selected. In either case, the CLK input (Pin 24) is set at 2 MHz for 8" drives or 1 MHz for 5¼" drives.

On the 2791/2793, the $\overline{ENMF}$ input (Pin 25) can be used for controlling both 5¼" and 8" drives with a single 2 MHz clock. When $\overline{ENMF}$ = 0, an internal ÷ 2 of the CLK is performed. When $\overline{ENMF}$ = 1, no divide takes place. This allows the use of a 2 MHz clock for both 5¼" and 8" configurations.

The internal VCO frequency must also be set to the proper value. The $\overline{5/8}$ input (Pin 17) is used to select data separator operation by internally dividing the Read Clock. When $\overline{5/8}$ = 0, 5¼" data separation is selected; when 5/8 = 1, 8" drive data separation is selected.

CLOCK (24)	$\overline{ENMF}$ (25)	$\overline{5/8}$ (17)	DRIVE
2 MHz	1	1	8"
2 MHz	0	0	5¼"
1 MHz	1	0	5¼"

Note: All other conditions invalid.

FUNCTIONAL DESCRIPTION

The WD279X-02 is software compatible with the FD179X-02 series of Floppy Disk Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the 179X can be transferred to a 279X system without modification.

In addition to the 179X, the 279X contains an internal Data Separator and Write precompensation circuit. The $\overline{TEST}$ (Pin 22) line is used to adjust both data separator and precompensation. When $\overline{TEST}$ = 0, the WD (Pin 31) line is internally connected to the output of the write precomp one-shot. Adjustment of the WPW (Pin 33) line can then be accomplished. A second one-shot tracks the precomp setting at approximately 3:1 to insure adequate Write Data pulse widths to meet drive specifications.

Similarly, Data separation is also adjusted with $\overline{TEST}$ = 0. The TG43 (Pin 29) line is internally connected to the output of the read data one-shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the Read Clock output (.5 MHz for 8" drives). The VCO Trimming capacitor (Pin 26) is adjusted for center frequency.

Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in-circuit. The $\overline{TEST}$ line also contains a pull-up resistor, so adjustments can be performed simply by grounding the $\overline{TEST}$ pin, overriding the pull-up. The $\overline{TEST}$ pin cannot be used to disable stepping rates during operation as its function is quite different from the 179X.

Other pins on the device also include pull-up resistors and may be left open to satisfy a Logic 1 condition. These are: ENP, $\overline{5/8}$, $\overline{ENMF}$, $\overline{WPRT}$, and $\overline{DDEN}$.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

* 2795/97 may vary — see command summary.

The number of sectors per track as far as the 279X is concerned can be from 1 to 255 sectors. The number of tracks as far as the 279X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the 279X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

For write operations, the 279X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

READY

Whenever a Read or Write command (Type II or III) is received the 297X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

COMMAND DESCRIPTION

The WD279X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

TABLE 1. COMMAND SUMMARY

A. Commands for Models: 2791, 2793

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-In	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

B. Commands for Models: 2795, 2797

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-In	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

TABLE 2. FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag	h = 0, Unload head at beginning h = 1, Load head at beginning
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II & III	0	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 15 MS Delay	E = 0, No. 15 MS delay E = 1, 15 MS delay (30 MS for 1 MHz)
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag	LSB's Sector Length in ID Field 00: L = 0: 256; L = 1: 128 01: L = 0: 512; L = 1: 256 10: L = 0: 1024; L = 1: 512 11: L = 0: 128; L = 1: 1024
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset* I_3-I_0 = 0 Terminate With No Interrupt (INTRQ)	

*NOTE: See Type IV Command Description for further information.

Write Precompensation

When operating in Double Density mode ($\overline{DDEN}$ = 0), the 279X has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10K) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.

Setting the Write precomp value is accomplished by forcing the $\overline{TEST}$ line (Pin 22) to a Logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed in-circuit since Write Gate (Pin 30) is inactive while $\overline{TEST}$ = 0.

Data Separation

The 279X can operate with either an external data separator or its own internal recovery circuits. The condition of the $\overline{TEST}$ line (Pin 22) in conjunction with $\overline{MR}$ (Pin 19) will select internal or external mode.

To program the 279X for external VCO, a $\overline{MR}$ pulse must be applied while $\overline{TEST}$ = 0. A clock equivalent to eight times the data rate (e.g., 4.0 MHz for 8" Double Density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the Pump output (Pin 23) for external integration to control the VCO. $\overline{TEST}$ is returned to a Logic 1 for normal operation. Note: To maintain this mode, $\overline{TEST}$ must be held low whenever $\overline{MR}$ is applied.

For internal VCO operation, the $\overline{TEST}$ line must be high during the $\overline{MR}$ pulse, then set to a Logic 0 for the adjustment procedure.

A 50K Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG43), adjust the RPW pulse for 1/8 of the data rate (250 ns for 8" Double Density). An external variable capacitor of 5-60 pf is tied to the VCO input (Pin 26) for adjusting center frequency. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate Data Rate (500 KHz for 8" Double Density). The $\overline{DDEN}$ line must be low while the 5/8 line is held high or the adjustment times above will be doubled.

After adjustments have been made, the $\overline{TEST}$ pin is returned to a Logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.

The PUMP output (Pin 23) consists of positive and negative pulses, which their duration is equivalent to the phase difference of incoming Data vs. VCO frequency. This signal is internally connected to the VCO input, but a Filter is needed to connect these pulses to a slow moving DC voltage.

The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore, it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.

A first order lag-lead filter can be used at the PUMP output (Pin 23). This filter controls the instantaneous response of the VCO to bit-shifted data (jitter) as well as the response to normal frequency shift, i.e., the lock-up time. A balance must be accomplished between the two conditions to inhibit over-responsiveness to jitter and to prevent an extremely wide lock-up response, leading to PUMP run-away. The filter affects these two reactions in mutually opposite directions.

The Source Impedance for a PUMP UP/DOWN condition is 600/120 ohms, respectively, therefore the change in bias voltage for each pump can be approximated:

$$dV = \frac{dt \, \Delta V}{RC}$$

dt = 250 ns. (set by RPW)
C = 0.1μf
$R = R_S + R$
ΔV = 2.6V for PUMP UP
0.9V for PUMP DOWN

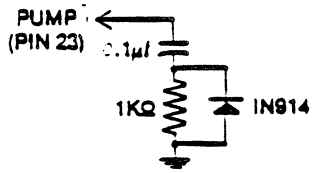
Look up response (T_L) is the transient time for the Loop to lock from center frequency (F_O) to maximum lock range:

$$T_L = 10\% \, F_L \times K_O \times \Delta P$$

Where:
K_O = VCO Conversion Gain = 3.7KHz/mV
F_L = Lock Range = 4.00 MHz
ΔP = Change in Bias for each Pump = 4 mV/PUMP

400 KHz x 3.7 KHz x 4 mV = 27 pumps
27 pumps = 54 μsec = 3.4 Byte times (8" Double Density)

The following Filter Circuit is recommended for 8" FM/MFM:



Since 5¼" Drives operate at exactly one-half the data rate (250 Kb/sec) the above capacitor should be doubled to .2 or .22μf.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0 r_1), which determines the stepping motor rate as defined in Table 3.

A 2μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK R1	CLK R0	2 MHz $\overline{TEST}$ = 1	1 MHz $\overline{TEST}$ = 1
0	0	3 ms	6 ms
0	1	6 ms	12 ms
1	0	10 ms	20 ms
1	1	15 ms	30 ms

After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for

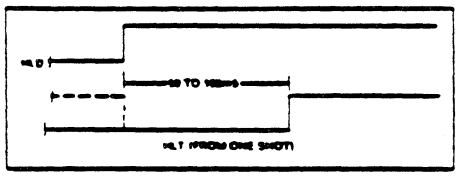
a 1 MHz clock. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The WD279X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the 279X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the 279X which is used for the head engage time. When HLT = 1, the 279X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the 279X.



HEAD LOAD TIMING

When both HLD and HLT are true, the 279X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: If h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the 279X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the 279X then waits for HLT to occur.

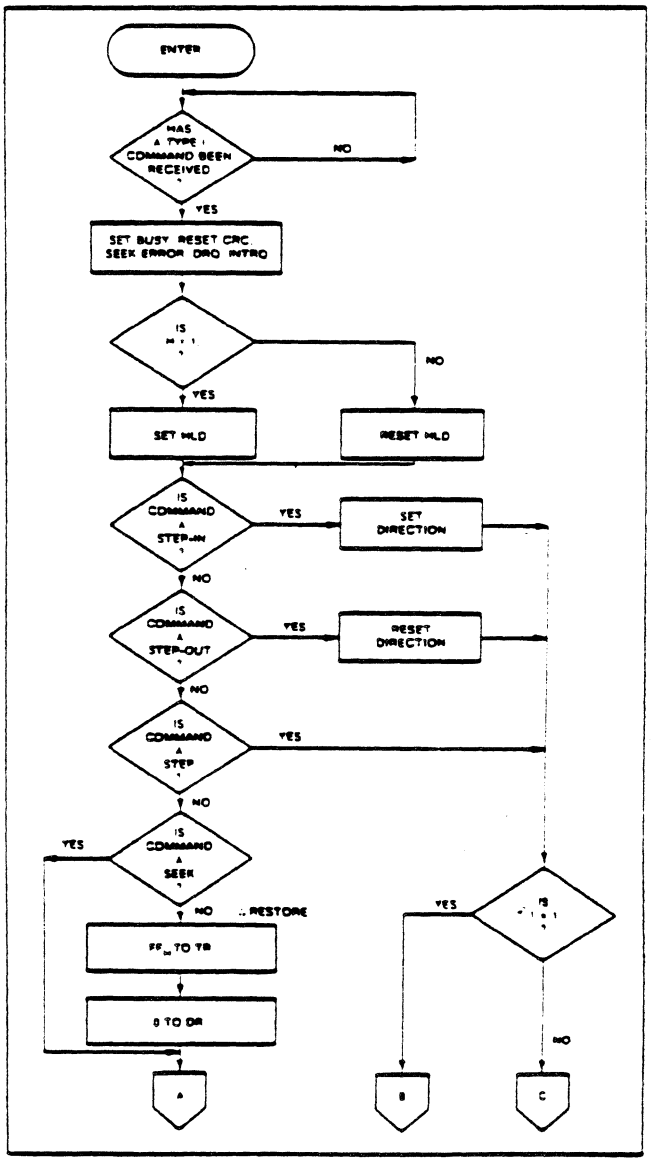
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0)

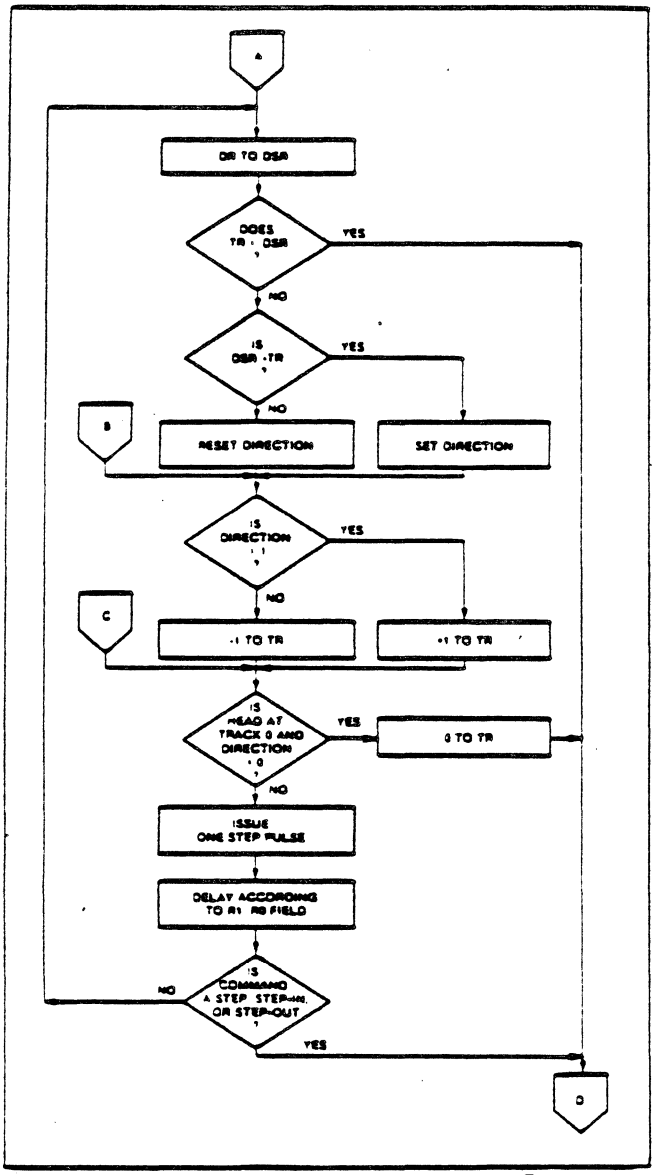
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r1r0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the 279X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state.

SEEK

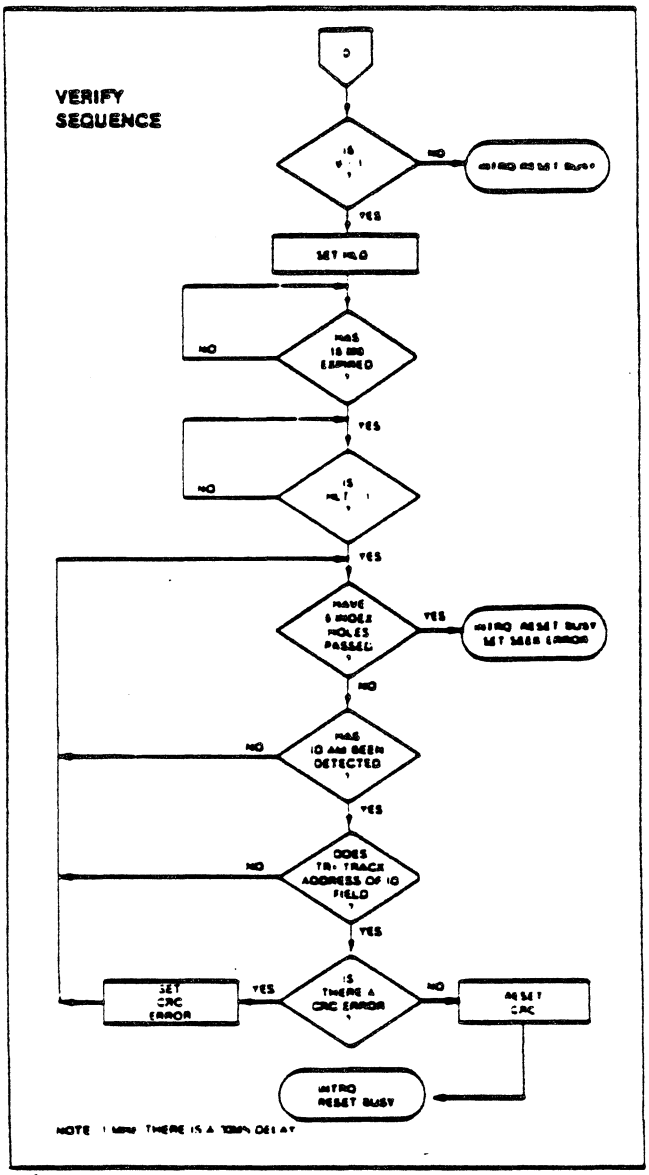
This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The WD279X will update the Track register and issue stepping pulses in the appropriate direction until the



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the 279X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the 279X issues one stepping pulse in the direction towards track 76. If the T flag is on, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the 279X issues one stepping pulse in the direction towards track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

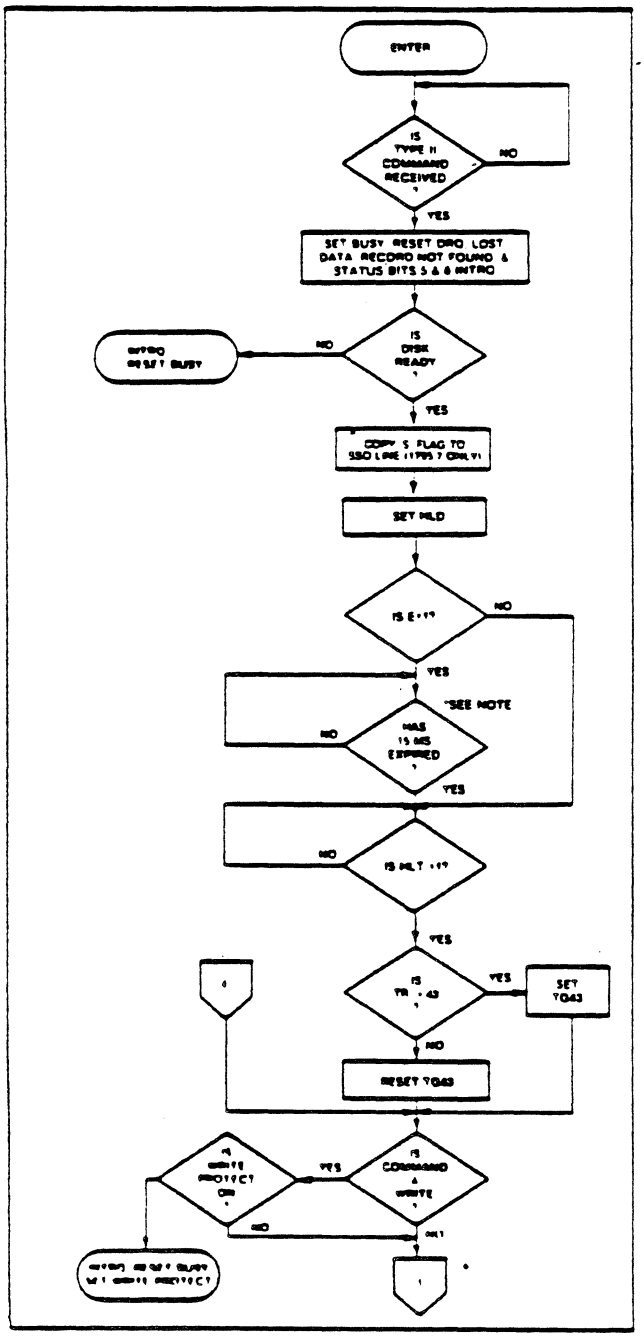
On the 2795/7 devices, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

TYPE II COMMANDS

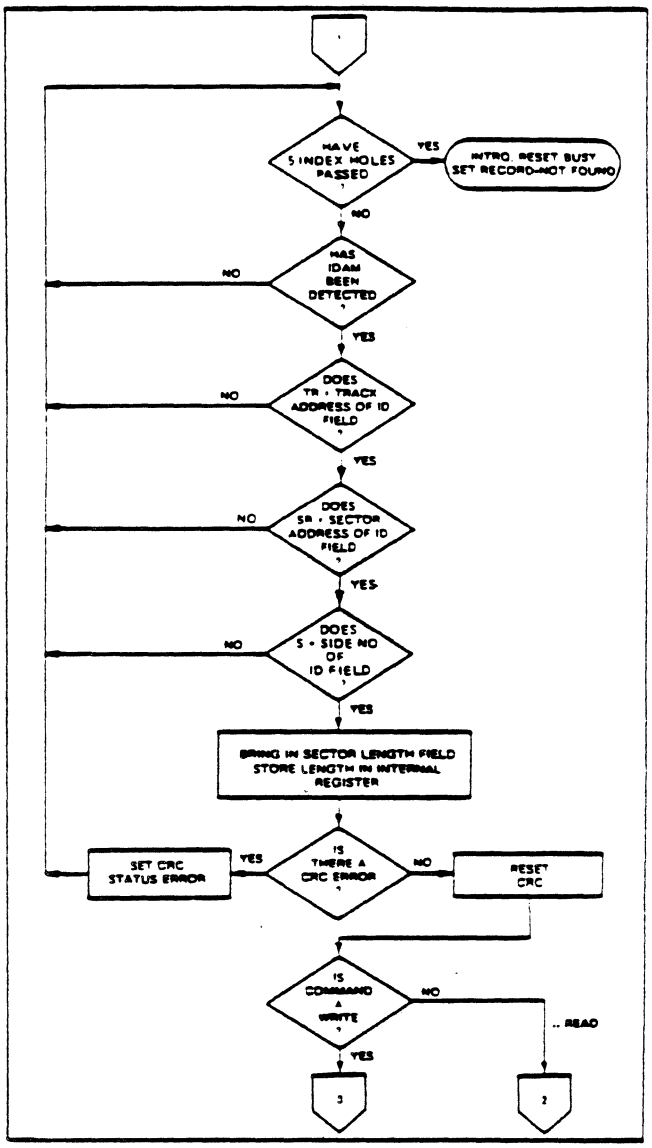
The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the

Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay.

When an ID field is located on the disk, the 279X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from



TYPE II COMMAND

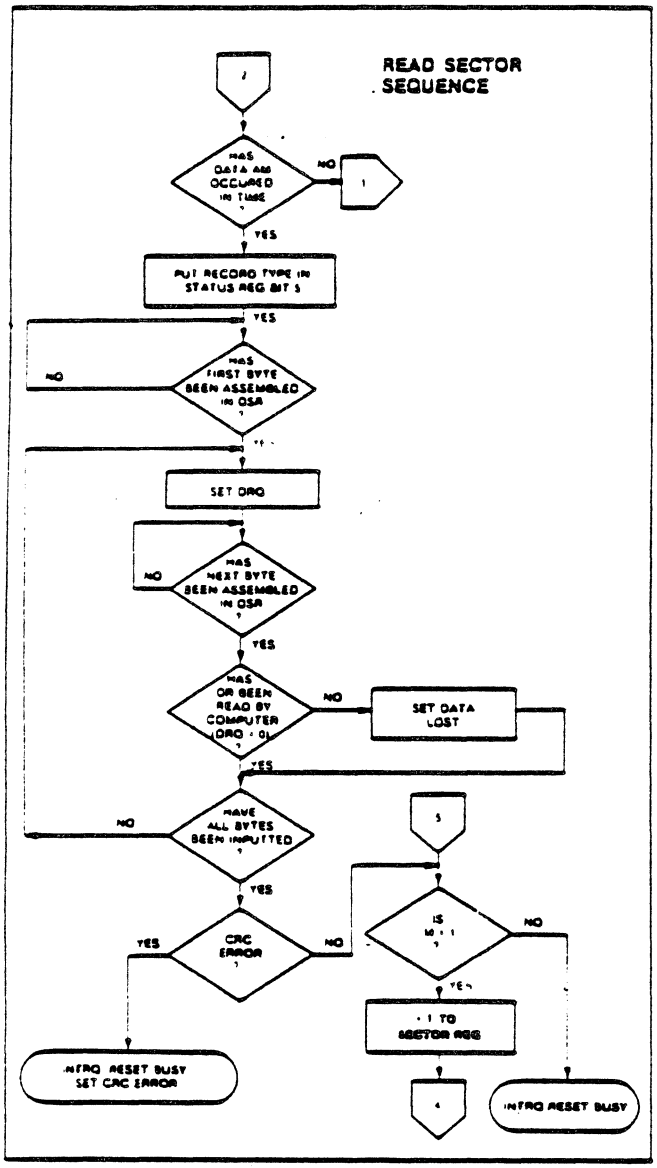


TYPE II COMMAND

depending upon the command. The 279X must find an ID field with a Track number, Sector number, side number, and CRC within 5 revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 4) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The 279X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the 279X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds



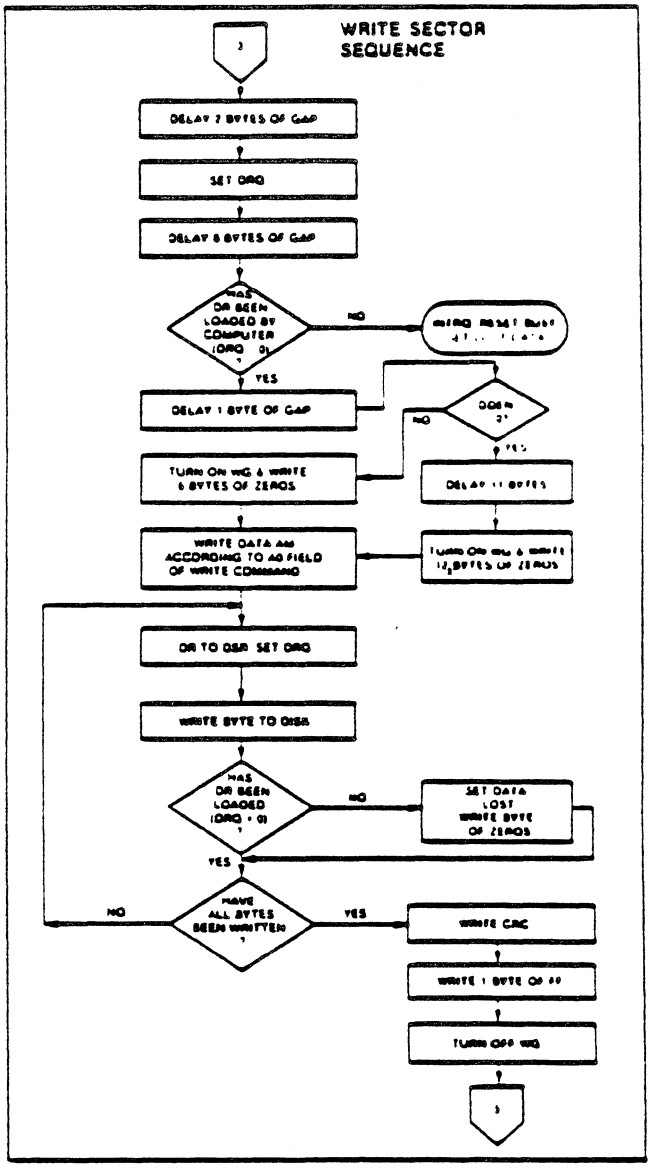
TYPE II COMMAND

the number available. The 279X will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

The Type II commands for 2791-93 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the 279X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III commands for the 2795-97 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

The 2795/7 READ SECTOR and WRITE SECTOR com-



TYPE II COMMAND

mands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the 'L' flag should be set to a one.

READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, search the ID field is repeated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred

that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple sector command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The 279X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a0 field of the command as shown below:

a0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The 279X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one bye of FE in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12 μsec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

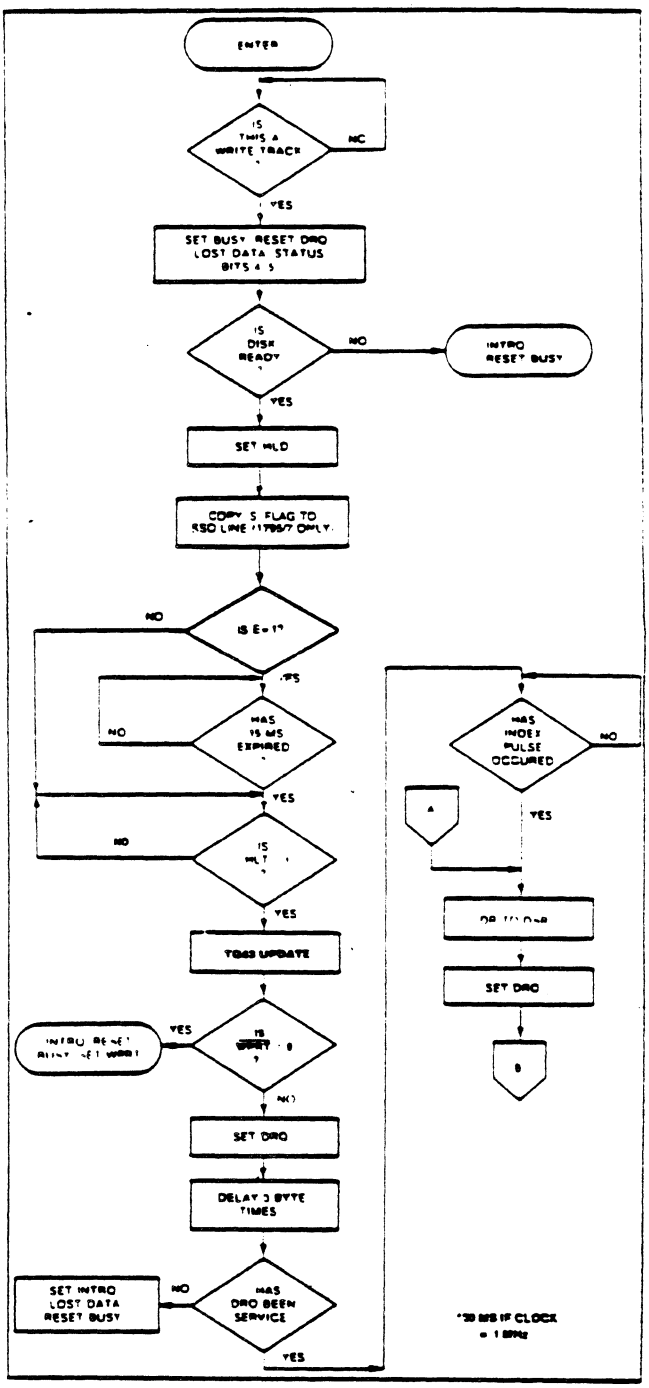
TYPES III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

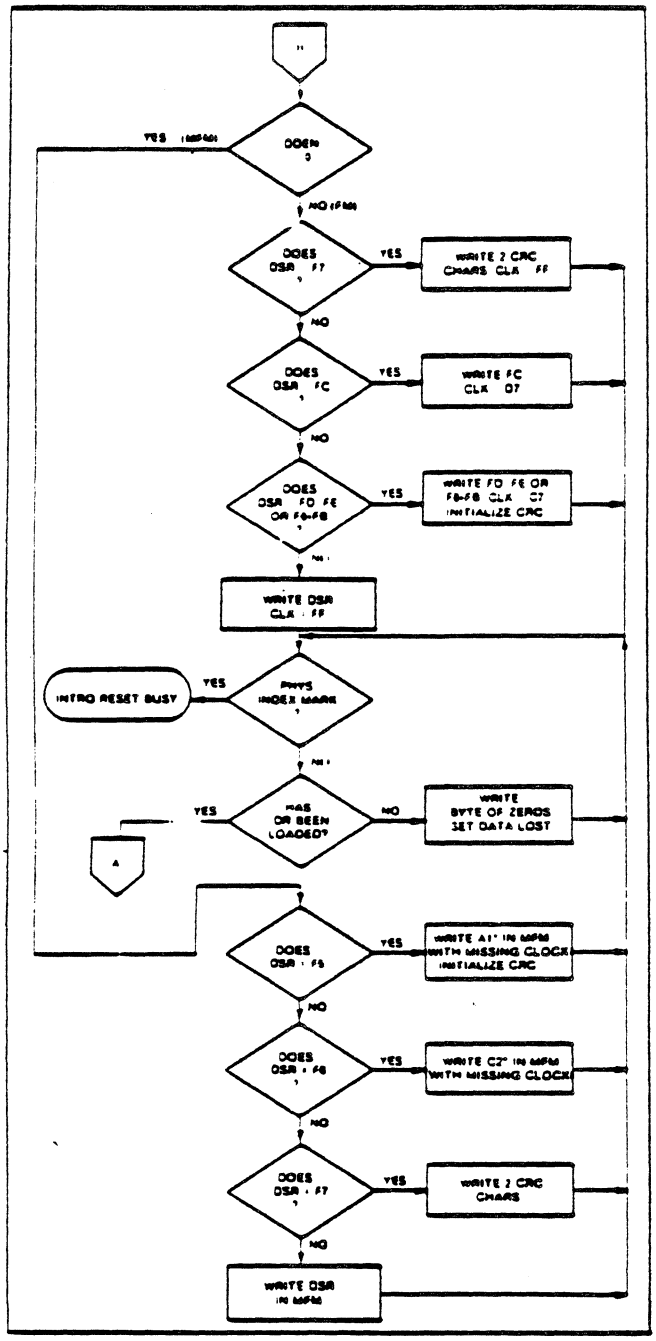
Although the CRC characters are transferred to the computer, the 279X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the host. At the end of the operation an interrupt is generated and the Busy Status is reset.



TYPE III COMMAND WRITE TRACK

READ TRACK

Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The ac-



TYPE III COMMAND WRITE TRACK

cumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule with the Lost Data status flag being set.

The ID A.M., ID field, ID CRC bytes, DAM, Data and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the 279X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	WD279X INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	WD279X INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

* Missing clock transition between bits 4 and 5

** Missing clock transition between bits 3 and 4

or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

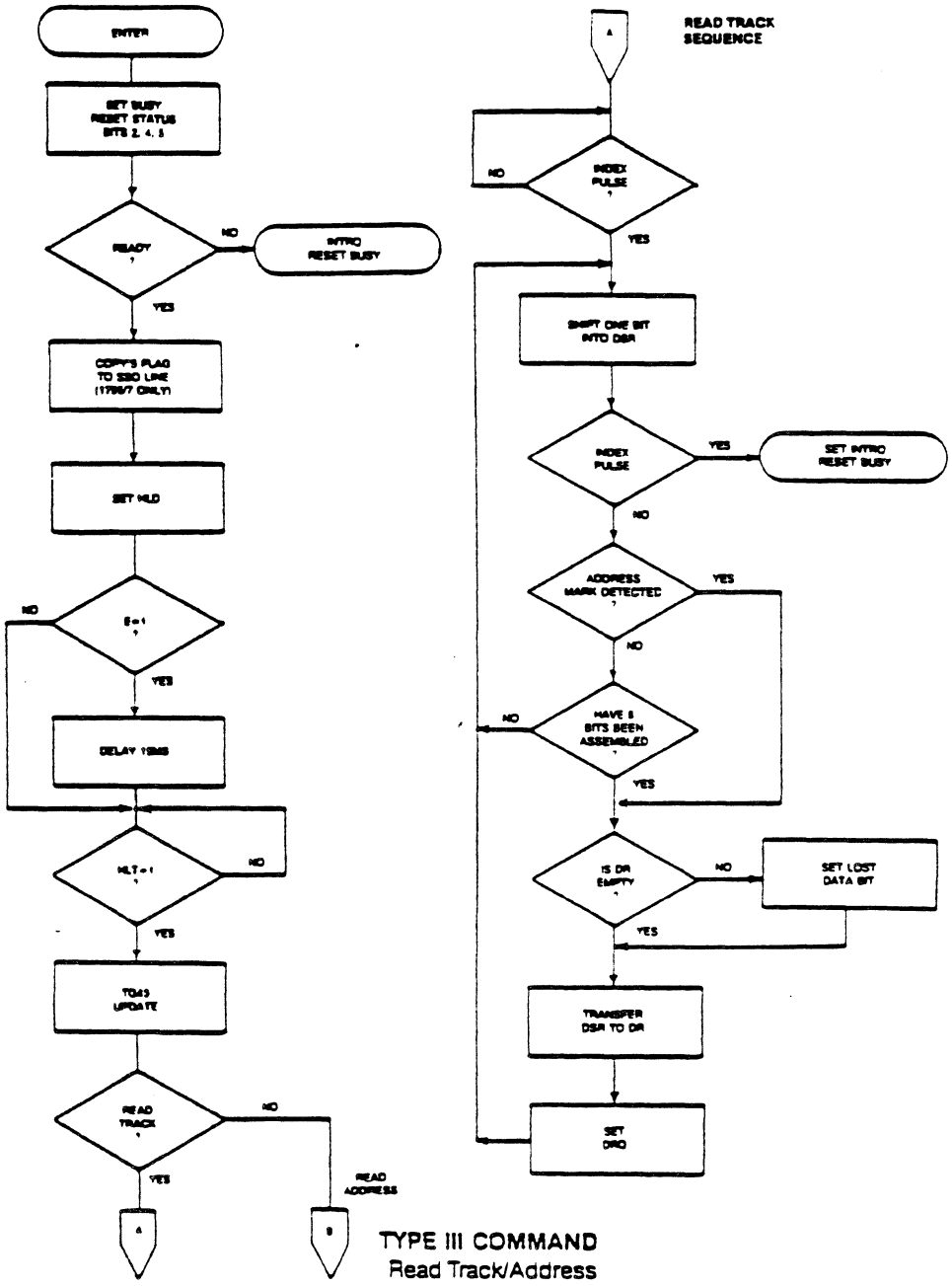
TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

I_0 = Not-Ready to Ready Transition
I_1 = Ready to Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3 - I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3 - I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate



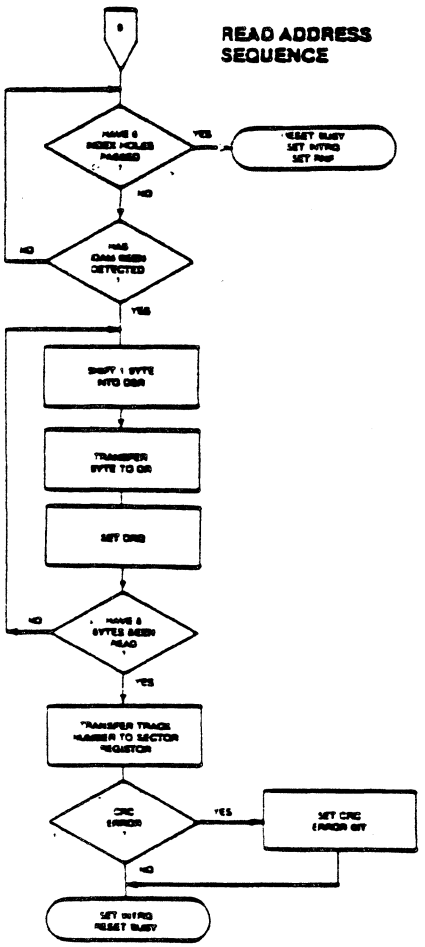
TYPE III COMMAND
Read Track/Address

interrupt condition (I3 = 1), an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 8 micro sec (double density) or 16 micro sec (single density) before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.)

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I1 = 1) and the Every Index Pulse (I2 = 1) are both set, the resultant command would be HEX "DA." The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.



TYPE III COMMAND
Read Track/Address

STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12μs	6μs
Write to Command Reg.	Read Status Bits 1-7	28μs	14μs
Write Any Register	Read From Diff. Register	0	0

IBM 3740 FORMAT — 128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)[3]
6	00
1	FC (Index Mark)
1 26	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)
247[2]	FF (or 00)

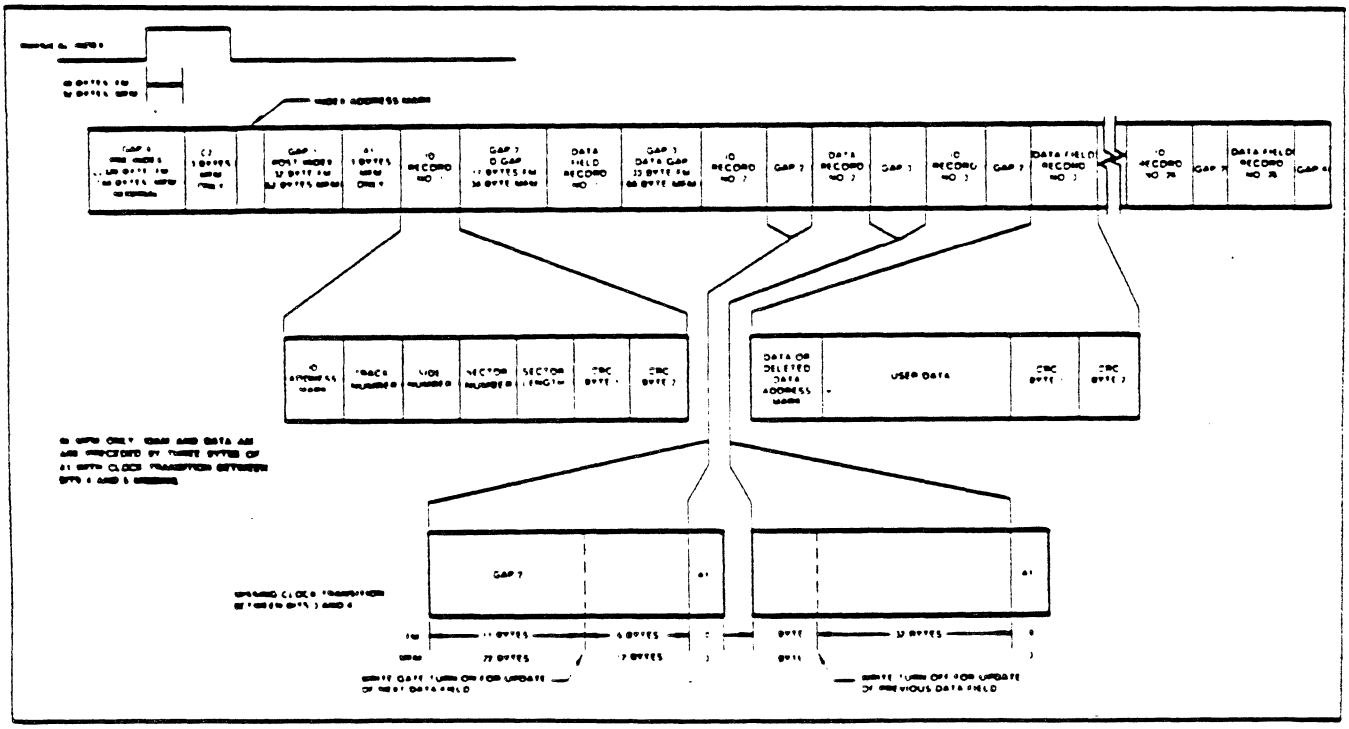
1. Write bracketed field 26 times
2. Continue writing until 279X interrupts out. Approx. 247 bytes.
3. A '00' option is allowed on 2795/7 only.

IBM SYSTEM 34 FORMAT-
256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order for format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
* 50	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

* Write bracketed field 26 times
** Continue writing until 279X interrupts out. Approx. 598 bytes.



IBM TRACK FORMAT

1. NON-IBM FORMATS

Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 of 1024 bytes.

2) Gap 2 cannot be varied from the IBM format.

3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the 279X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for 279X operation, however PLL lock up time, motor speed variation, write splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

* Byte counts must be exact.

** Byte counts are minimum, except exactly 3 bytes of A1 must be written.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Voltage to any input with respect to V_{SS} = +15 to −0.3V

C_{IN} & C_{OUT} = 15 pF max with all pins grounded except one under test.

Operating temperature = 0°C to 70°C

Storage temperature = −55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5M ± .25V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage			10	µA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage			10	µA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.4			V	I_O = −100µA
V_{OL}	Output Low Voltage			0.45	V	I_O = 1.6 mA
V_{OHP}	Output High PUMP	2.2			V	I_{OP} = −1.0 mA
V_{OLP}	Output Low PUMP			0.2	V	I_{OP} = +1.0 mA
P_D	Power Dissipation			.75	W	All Outputs Open
R_{PU}	Internal Pull-up*	100		1700	µA	V_{IN} = 0V
I_{CC}	Supply Current		70	150	mA	All Outputs Open

* Internal Pull-up resistors on PINS 1, 17, 22, 25, 37, and 40.

TIMING CHARACTERISTICS

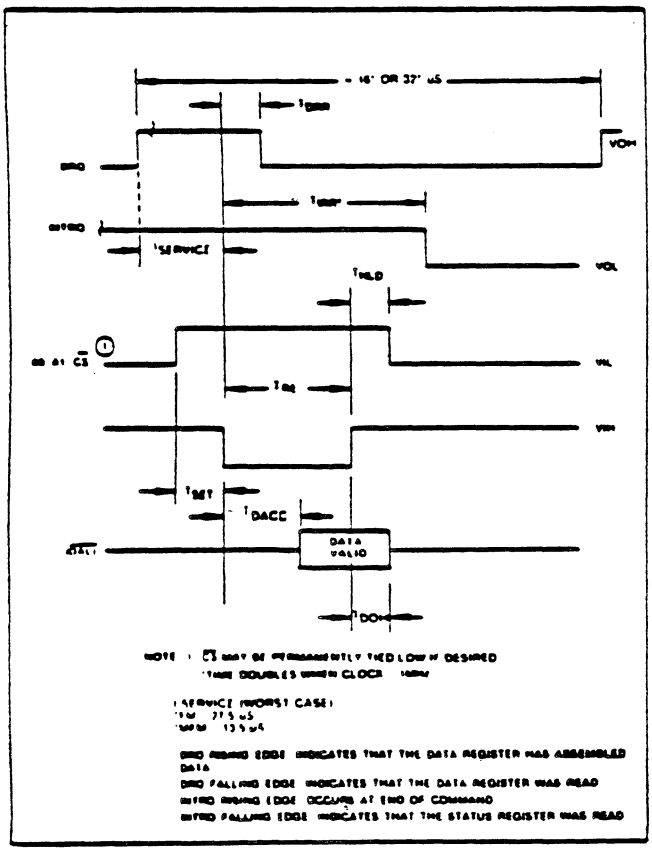
T_A = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V

READ ENABLE TIMING

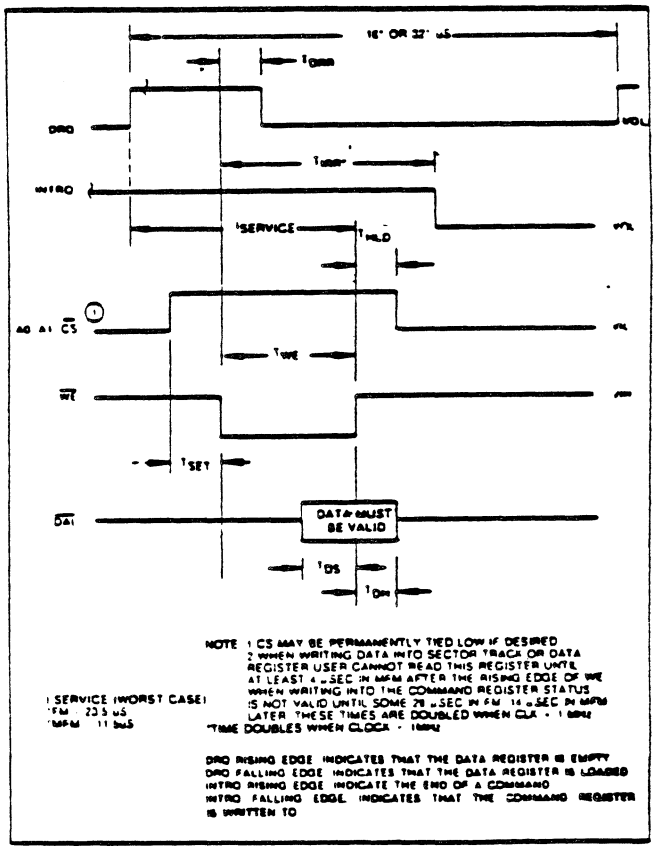
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{SET}	Setup ADDR & CS to $\overline{RE}$	50			nsec	
T_{HLD}	Hold ADDR & CS from $\overline{RE}$	10			nsec	
T_{RE}	$\overline{RE}$ Pulse Width	200			nsec	C_L = 50 pf
T_{DRR}	DRQ Reset from $\overline{RE}$		100	200	nsec	
T_{IRR}	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note
T_{DACC}	Data Valid from $\overline{RE}$		100	200	nsec	C_L = 50 pf
T_{DOH}	Data Hold From $\overline{RE}$	20		150	nsec	C_L = 50 pf

WRITE ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{SET}	Setup ADDR & CS to $\overline{WE}$	50			nsec	
T_{HLD}	Hold ADDR & CS from $\overline{WE}$	10			nsec	
T_{WE}	$\overline{WE}$ Pulse Width	200			nsec	
T_{DRR}	DRQ Reset from $\overline{WE}$		100	200	nsec	
T_{IRR}	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note
T_{DS}	Data Setup to $\overline{WE}$	150			nsec	
T_{DH}	Data Hold from $\overline{WE}$	50			nsec	



READ ENABLE TIMING



WRITE ENABLE TIMING

INPUT DATA TIMING

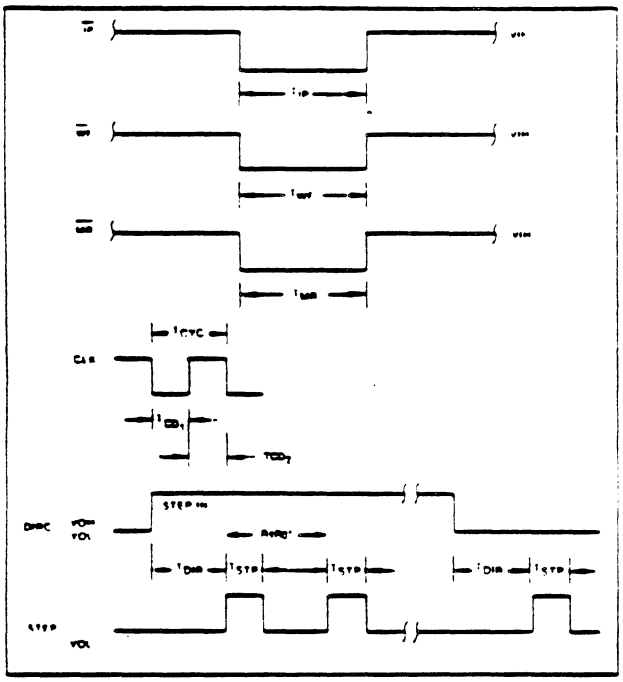
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{PW}	$\overline{\text{Raw Read}}$ Pulse Width	100	200		nsec	
T_{BC}	$\overline{\text{Raw Read}}$ Cycle Time	1500	2000		nsec	

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{WP}	Write Data Pulse Width	400	500	600	nsec	FM
		240		1000	nsec	MFM
T_{WG}	Write Gate to Write Data		2		µsec	FM
			1		µsec	MFM
T_{WF}	Write Gate off from WD		2		µsec	FM
			1		µsec	MFM

MISCELLANEOUS TIMING:

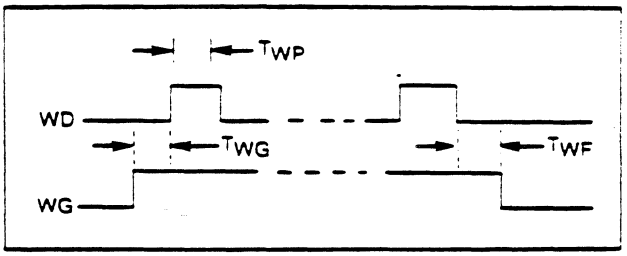
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{CD_1}	Clock Duty (low)	230	250	20000	nsec	
T_{CD_2}	Clock Duty (high)	230	250	20000	nsec	
T_{STP}	Step Pulse Output	2 or 4			µsec	See Note
T_{DIR}	Dir Setup to Step		12		µsec	± CLK ERROR
T_{MR}	Master Reset Pulse Width	50			µsec	
T_{IP}	Index Pulse Width	10			µsec	See Note
RPW	Read Window Pulse Width					Input 0-5V
		120		700	nsec	MFM
		240		1400	nsec	FM ± 15%
WPW	Write Data Pulse Width					Input 0-5V
		300		1000	nsec	MFM
			500		nsec	FM
	Precomp Adjust.	100		250	nsec	MFM
RPW	Read Window Pulse Width					Input 0-5V
		120		700	nsec	MFM
		240		1400	nsec	FM ± 15%
WPW	Write Data Pulse Width					Input 0-5V
		300		1000	nsec	MFM
			500		nsec	FM
	Precomp Adjust.	100		250	nsec	MFM
VCO	Free Run Voltage Controlled	6.0			MHz	Ext. C = 0
	Oscillator. Adjustable by ext. capacitor on Pin 26		4.0		MHz	Ext. C = 35 pf
	Pump Up + 25%	5.0			MHz	PU = 2.2V Cext = 35 pf
VCO	Pump Down − 25%			3.0	MHz	$\overline{PD}$ = 0.2V Cext = 35 pf
	5% Change V_{CC}	3.8		4.2	MHz	Cext = 35 pf
VCO	T_A = 75°C	3.5			MHz	Cext = 35 pf
Cext	Necessary external capacitor	10	35	80	pf	VCO = 4.0MHz nom
RCLK	Derived read clock = VCO ÷ 8, 16, 32					VCO = 4.0MHz
			500		KHz	$\overline{DDEN}$ = 0 $\overline{5/8}$ = 1
			250		KHz	$\overline{DDEN}$ = 0 $\overline{5/8}$ = 0
			250		KHz	$\overline{DDEN}$ = 1 $\overline{5/8}$ = 1
			125		KHz	$\overline{DDEN}$ = 1 $\overline{5/8}$ = 0
PU/DON	PU/$\overline{PD}$ time on (pulse width)			250	ns	MFM
				500	ns	FM



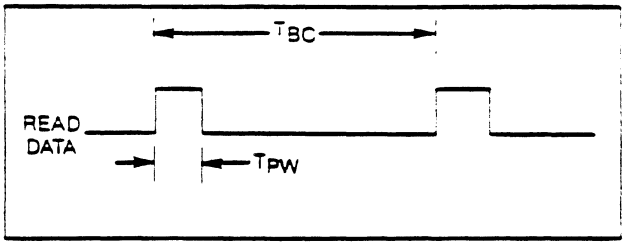
MISCELLANEOUS TIMING

NOTES:

1. Times double when clock = 1 MHz.
2. Output timing readings are at V_{OL} = 0.8v and V_{OH} = 2.0v.



WRITE DATA TIMING



READ DATA TIMING

*FROM STEP RATE TABLE

Table 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	0	0
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TR00}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: Forced to a Zero.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

SUMMARY OF ADJUSTMENT PROCEDURE

WRITE PRECOMPENSATION

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe $\overline{\text{MR}}$ (Pin 19).
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4) Observe pulse width on WD (Pin 31).
5) Adjust WPW (Pin 33) for desired pulse width (Precomp Value).
6) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

DATA SEPARATOR

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe $\overline{\text{MR}}$ (Pin 19). Insure that $\overline{5}/8$, $\overline{\text{ENMF}}$, and $\overline{\text{DDEN}}$ are set properly.
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4) Observe Pulse Width on TG43 (Pin 29).
5) Adjust RPW (Pin 18) for 1/8 of the read clock
   (250ns for 8"DD, 500ns for 5¼"DD, etc.)
6) Observe Frequency on DIRC (Pin 16).
7) Adjust variable capacitor on VCO pin for Data Rate
   (500KHz for 8"DD, 250KHz for 5¼"DD, etc.)
8) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

NOTE: To maintain internal VCO operation, insure that $\overline{\text{TEST}}$ = 1 whenever a master reset pulse is applied.

APPENDIX "F"

The SYS68K/WFC-1 Controller Board is tested with the following Winchester and Floppy Drives during Debbuging and Design Phase.

5 14" Winchester Drives:

- SHUGART SA 600
- QUANTUM Q 520
- MICROPOLIS 1302
- NEC D5244
- BASF 6185
- CDC 9415

5 1/4" Floppy Drives:

- SHUGART SA460/SA465
- BASF 6116
- MICROPOLIS 1115-6
- CDC 9409T
- MITSUBISHI M4853

Dear Customer,

While FORCE Computers has achieved a very high standard of quality in our products and documentation, we continually seek suggestions for new improvements. We would appreciate any feedback you care to offer.

Please use the attached "PRODUCT ERROR REPORT" form for your comments and return it to one of our FORCE Computers offices.

Sincerely,
FORCE Computers.

P R O D U C T E R R O R R E P O R T

HARDWARE/SOFTWARE/SYSTEMS

PRODUCT : _____

SERIAL NO. : _____

DATE OF PURCHASE : _____

ORIGINATOR : _____

COMPANY : _____

ADDRESS : _____

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DATE : _____

TELEPHONE : ( ) _____ EXT _____

CONTACT : _____

This box to be completed by FORCE
DATE : _____
PR# : _____
ACTION BY :
Engineering ( )
Marketing ( )
Production ( )

AFFECTED PRODUCT: ( ) SOFTWARE ( ) HARDWARE ( ) SYSTEM

AFFECTED DOCUMENTATION: ( ) SOFTWARE ( ) HARDWARE ( ) SYSTEM

ERROR DESCRIPTION : _____

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ORIGINATOR : _____

COMPANY : _____

ADDRESS : _____

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