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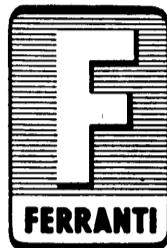
PEGASUS COMPUTER

(F.P.C.I)

VOLUME 2a

LOGICAL DESIGN

(Diagrams)



FERRANTI PEGASUS COMPUTER

VOLUME 2a

LOGICAL DESIGN

(Diagrams)

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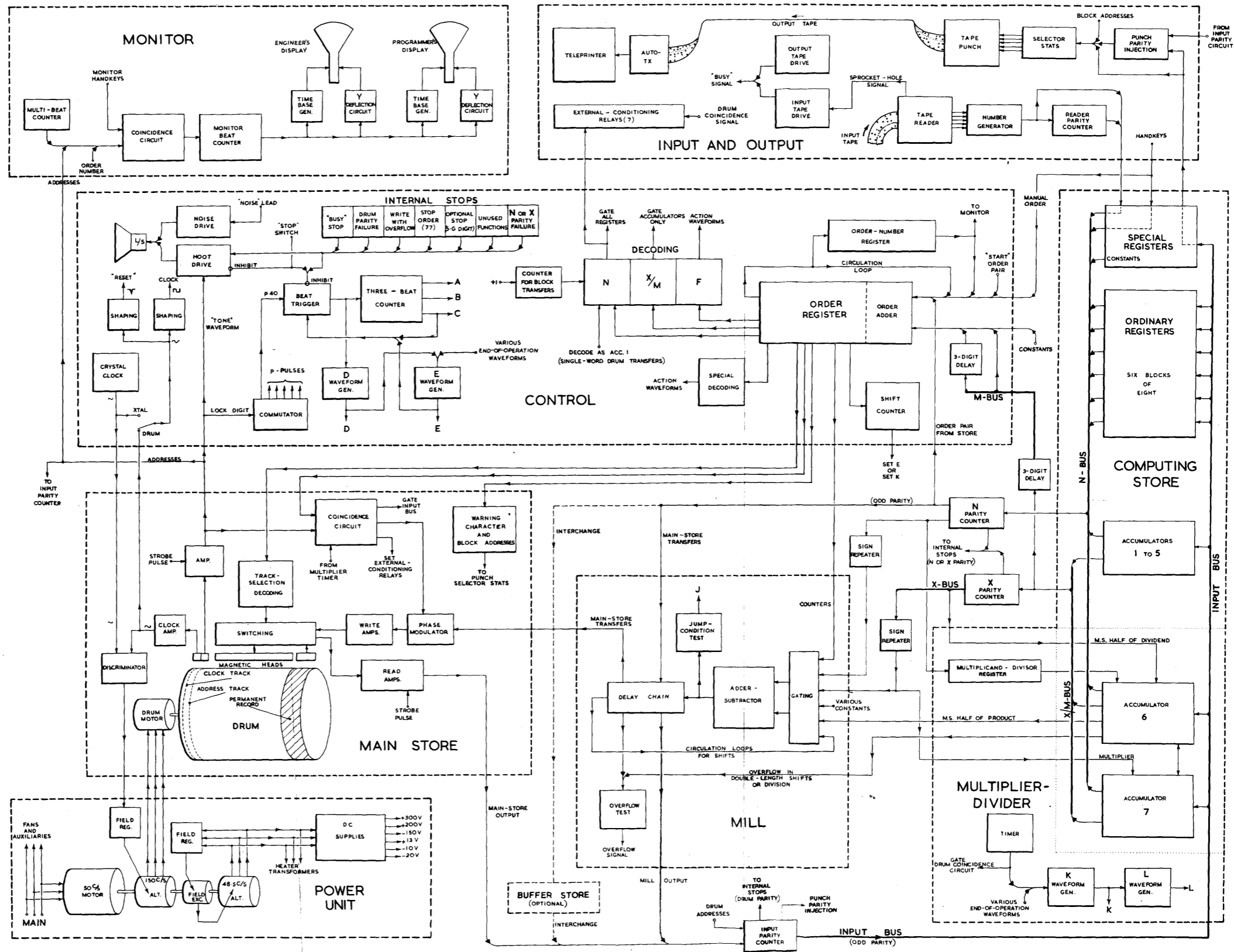
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C O N T E N T S

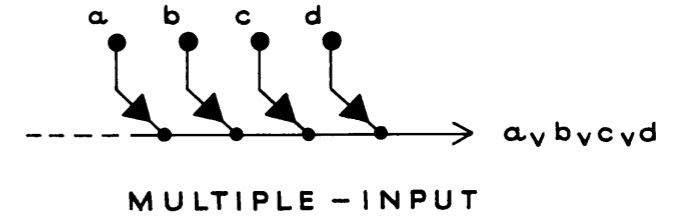
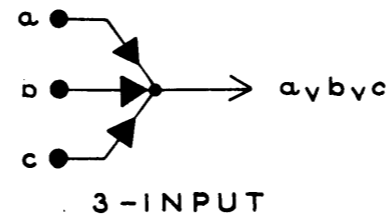
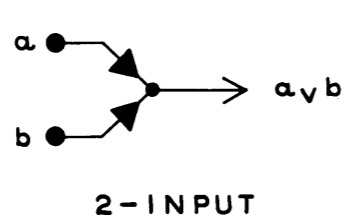
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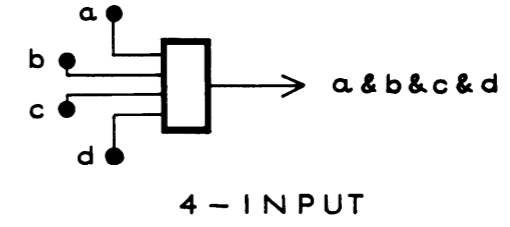
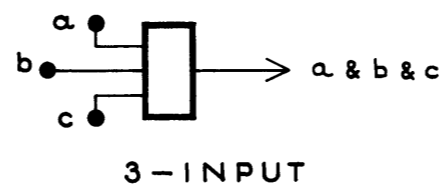
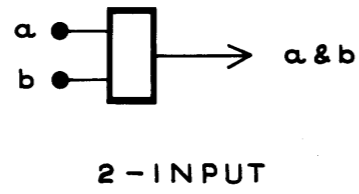


SCHMATIC DIAGRAM OF FERRANTI PEGASUS COMPUTER

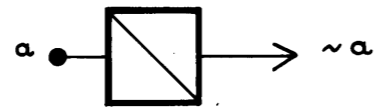
OR GATES



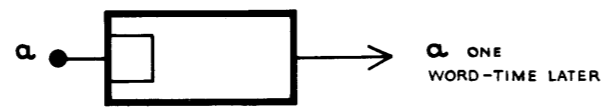
AND GATES



INVERTER



WORD DELAY



DIGIT DELAY

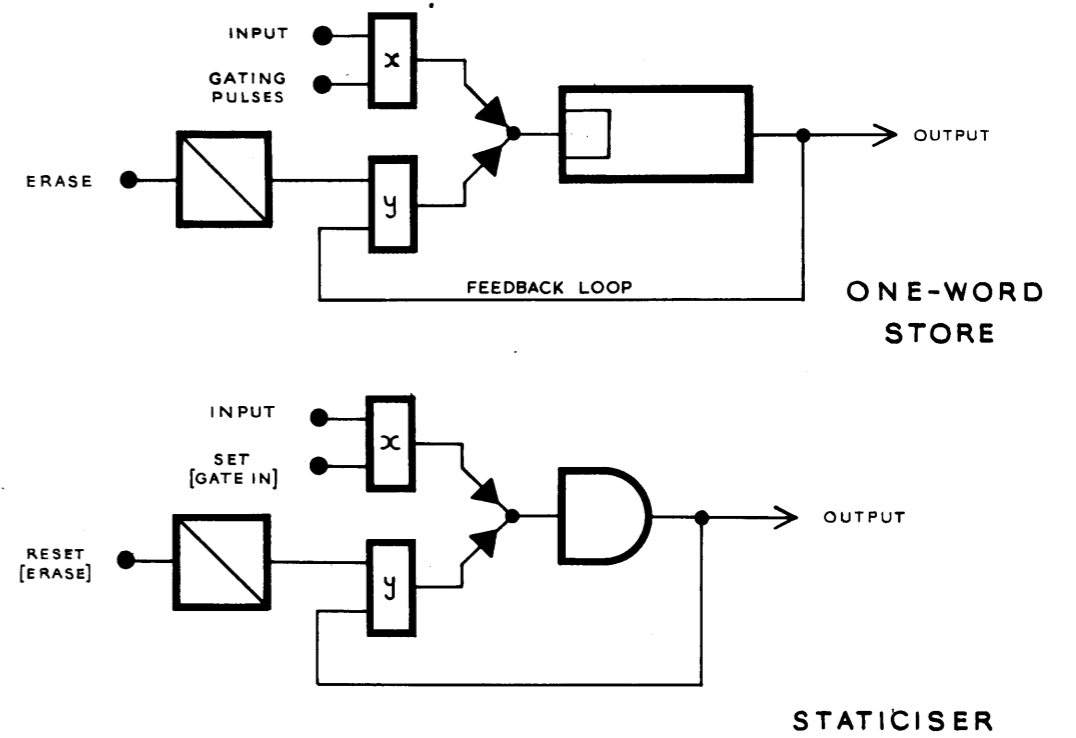
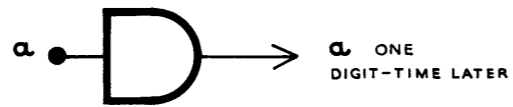
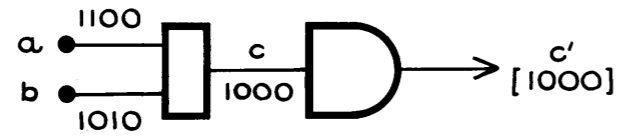
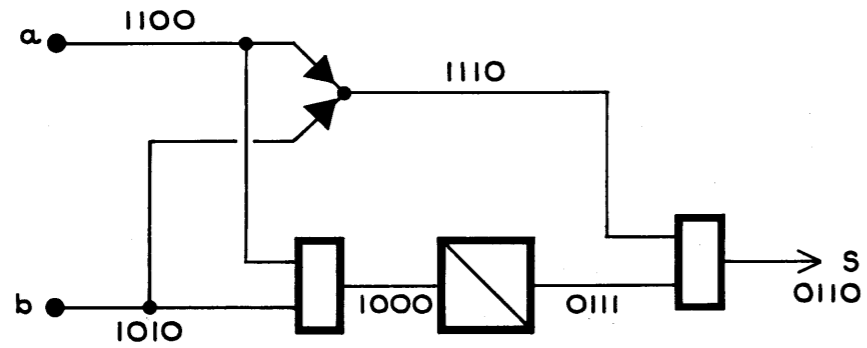
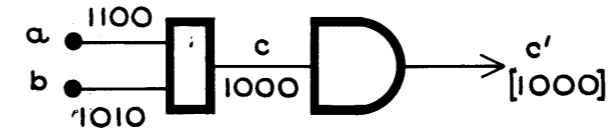


FIG. 3.1 LOGICAL ELEMENTS

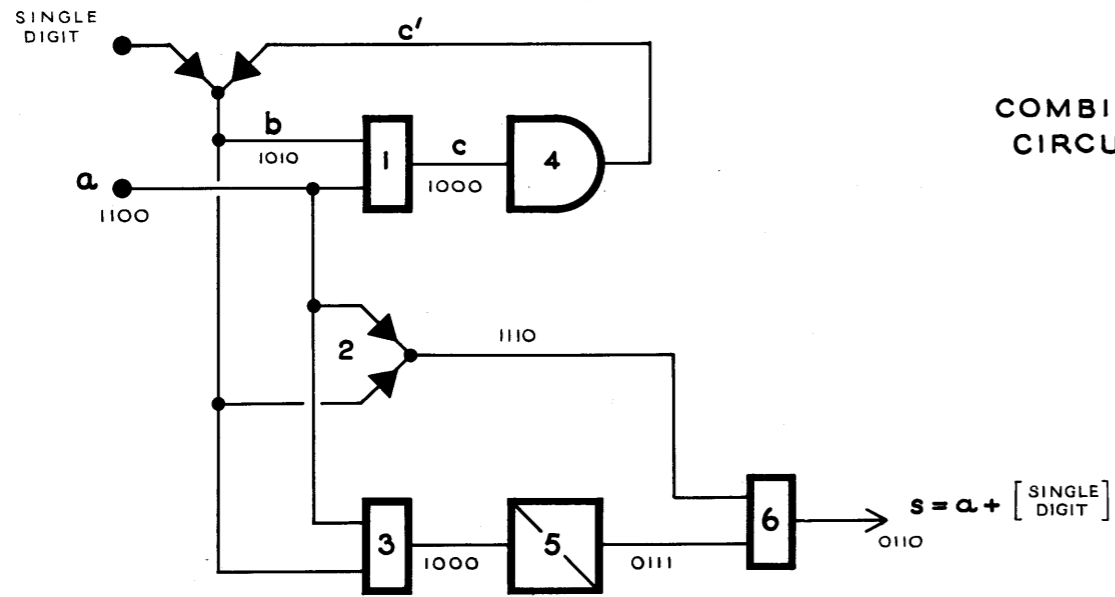
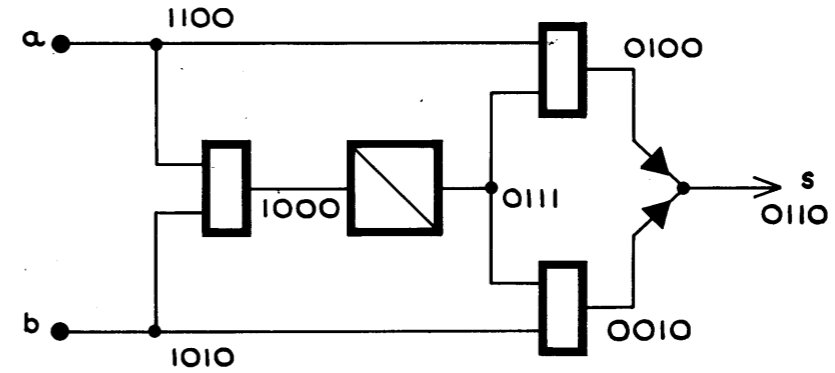
BINARY ANNOTATIONS ARE TO BE TAKEN DIGIT BY DIGIT AS TRUTH-TABLE REPRESENTATIONS, NOT SEQUENTIALLY AS BINARY NUMBERS



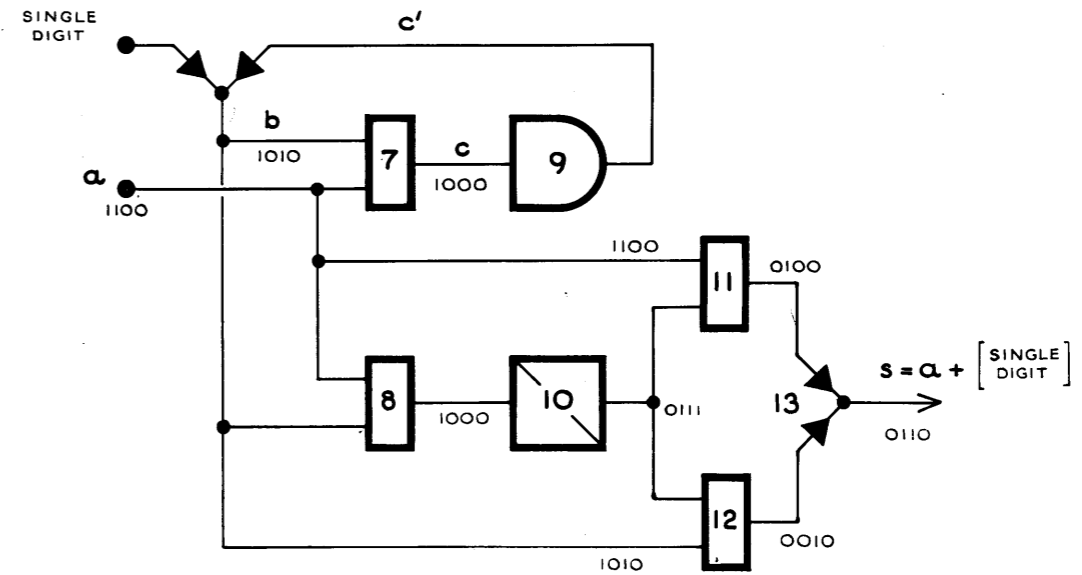
GENERATION OF "CARRY" DIGIT



GENERATION OF "SUM" DIGIT



COMBINED CIRCUITS



$$s = [a \vee b] \& \sim [a \& b]$$

$$s = [a \& \sim [a \& b]] \vee [b \& \sim [a \& b]]$$

FIG. 3.2 HALF ADDERS

BINARY ANNOTATIONS ARE TO BE TAKEN DIGIT BY DIGIT AS TRUTH-TABLE REPRESENTATIONS NOT SEQUENTIALLY AS BINARY NUMBERS

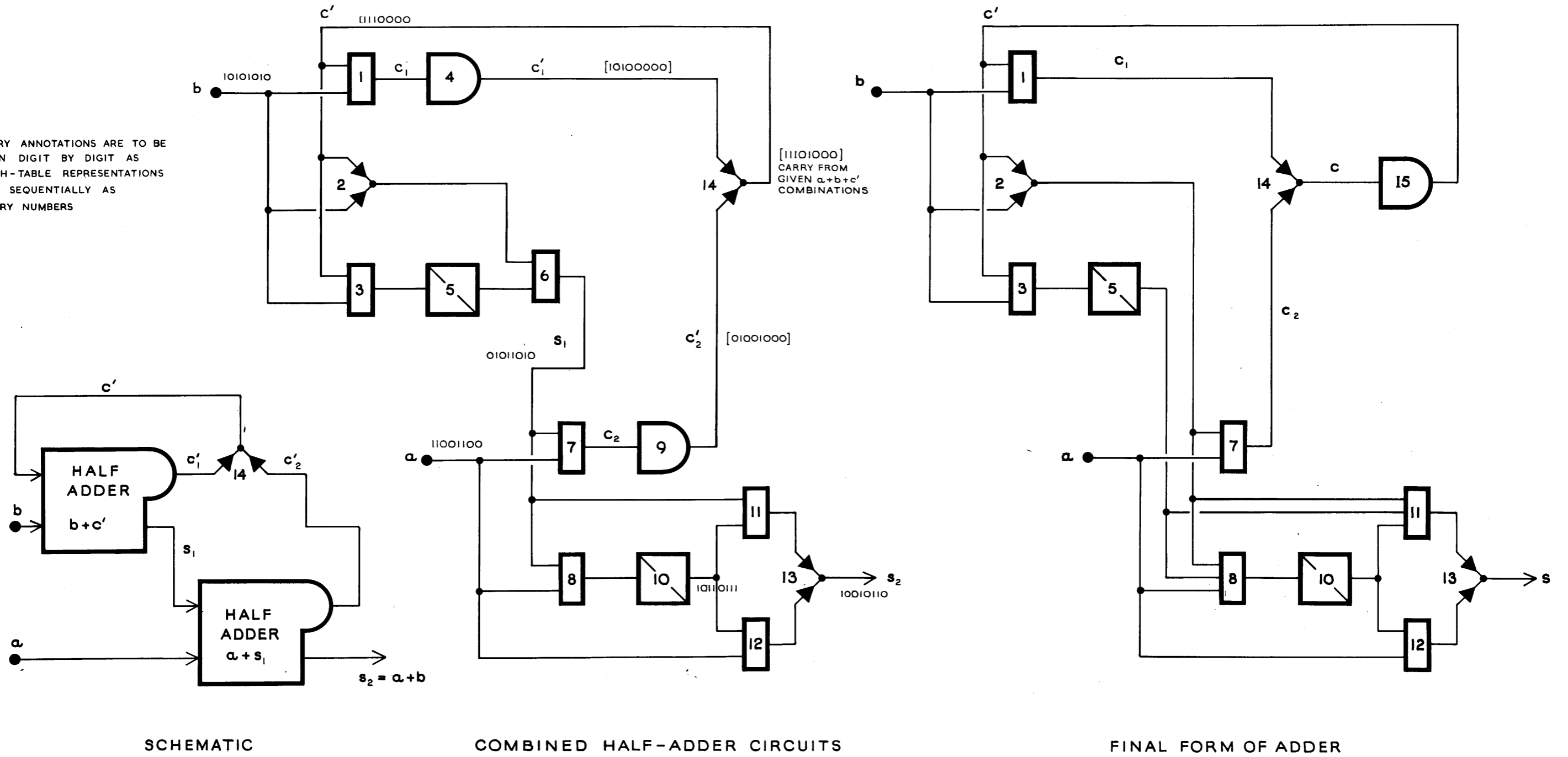
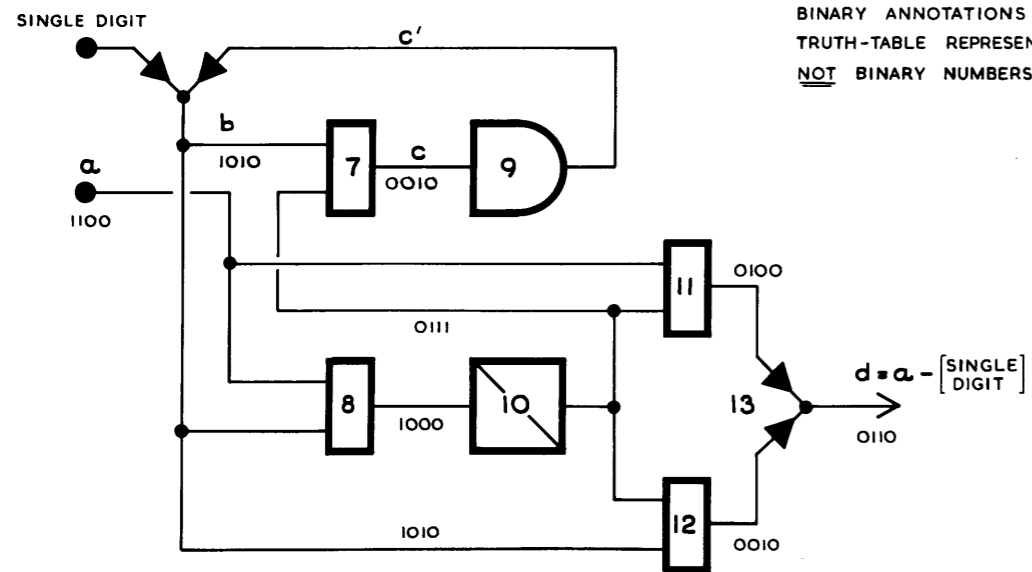
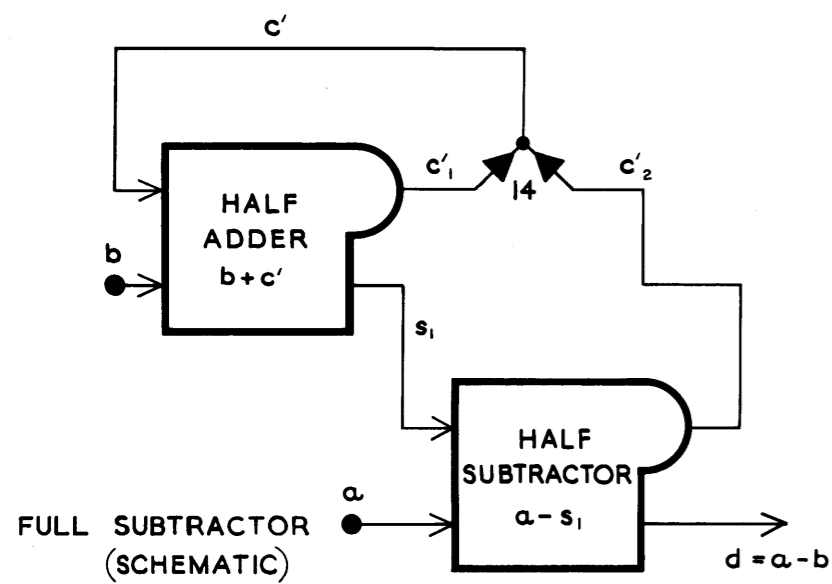
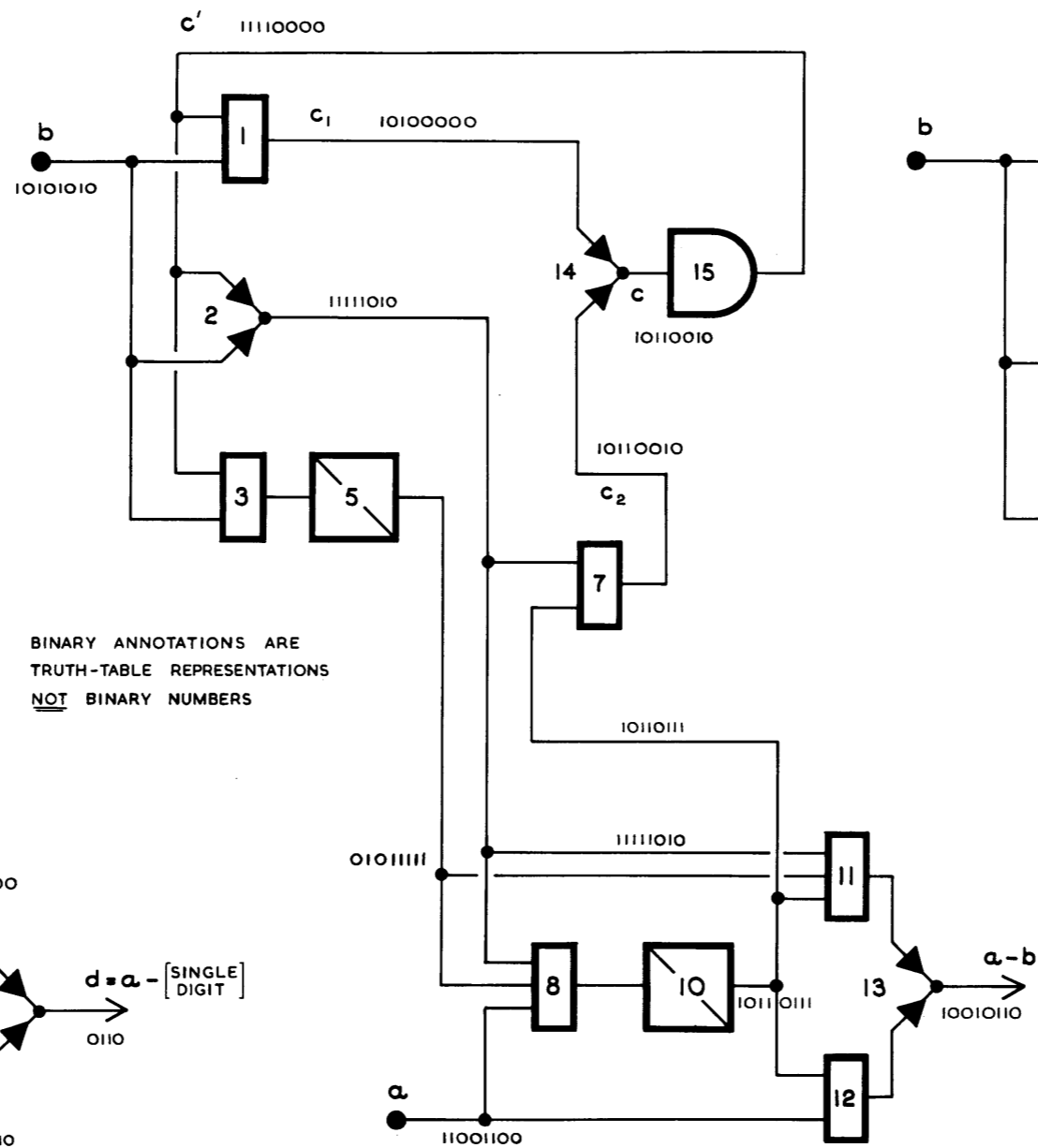


FIG.3.3. FULL ADDER

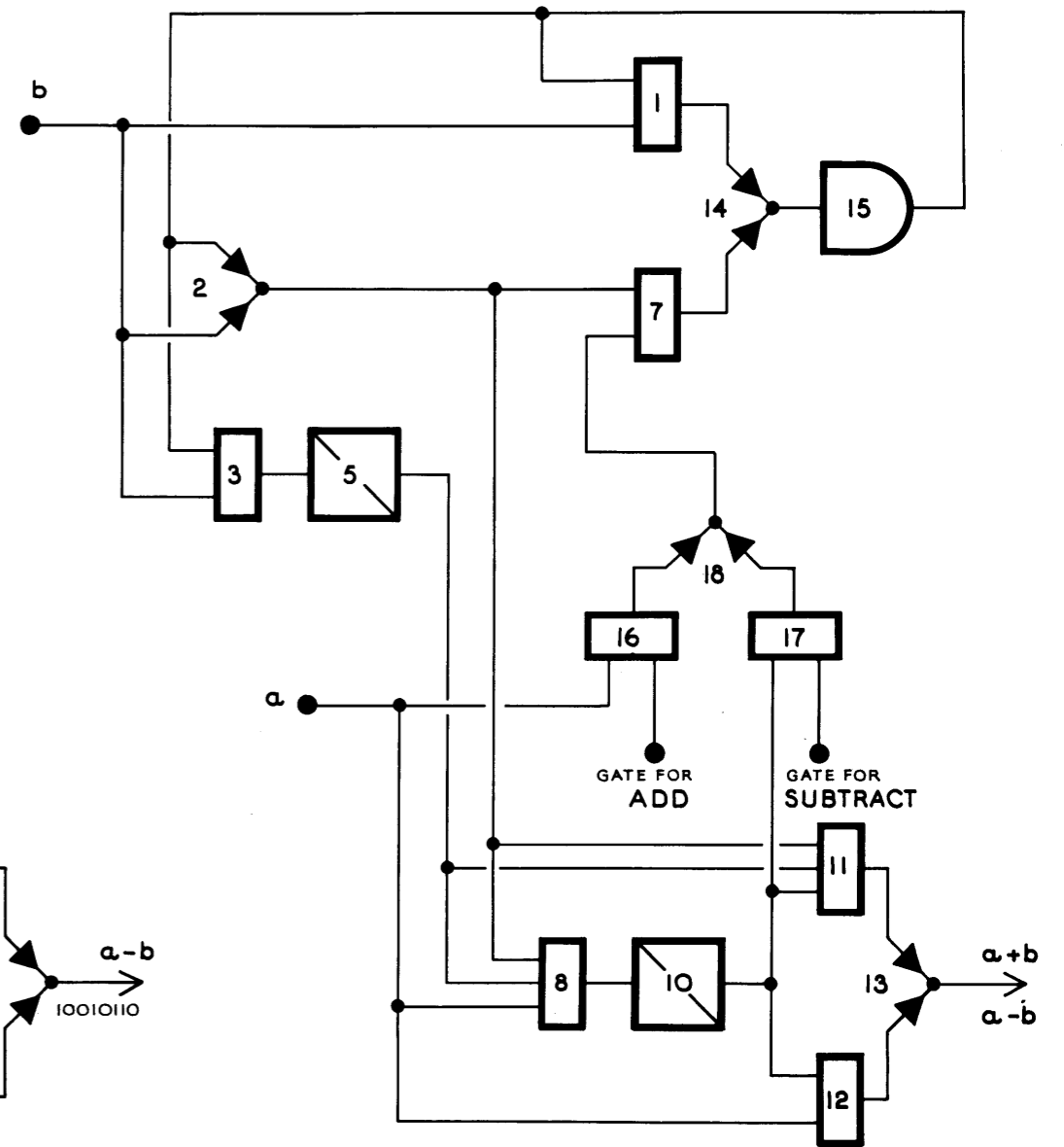


HALF SUBTRACTOR

FIG. 3.4



FULL SUBTRACTOR



ADDER-SUBTRACTOR

| PACKAGE TYPE | ELEMENT | SYMBOL | POSITIONS ON PACKAGE |
|--------------|--------------|---|----------------------|
| 1 | TWIN DELAY | | 1, 2 |
| 2 | SINGLE DELAY | | 1, 2, 3 |
| 3 | INVERTER | | 1, 2, 3 |
| 4 | AND GATE | <p>2-INPUT </p> <p>3-INPUT </p> <p>4-INPUT </p> | 1 2, 3 4 |

| PACKAGE TYPE | ELEMENT | SYMBOL | POSITIONS ON PACKAGE |
|--------------|------------------|--------|----------------------|
| 6 | SPECIAL INVERTER | | |
| 6 | NICKEL LINE | | |
| 7 | NUMBER GENERATOR | | 2, 5 |
| | CATHODE-FOLLOWER | | 1, 3, 4, 6 |

| PACKAGE TYPE | ELEMENT | SYMBOL | POSITIONS ON PACKAGE |
|--------------|--------------------|--------|--|
| 8 | CATHODE - FOLLOWER | | 1, 2, 3 |
| 8 | OR GATE | | 4, 5 |
| 8 | OR GATE | | 6 |
| 9 | OUTPUT ONE | | TWO OFF USED IN CONJUNCTION WITH ELEMENTS 1 AND 2 OR 3 AND 4 IN PARALLEL 1, 2, 3, 4, 5, 6 |
| 10 | OUTPUT TWO | | 1, 2, 3 |

FIG. 3.5

PACKAGED LOGICAL ELEMENTS

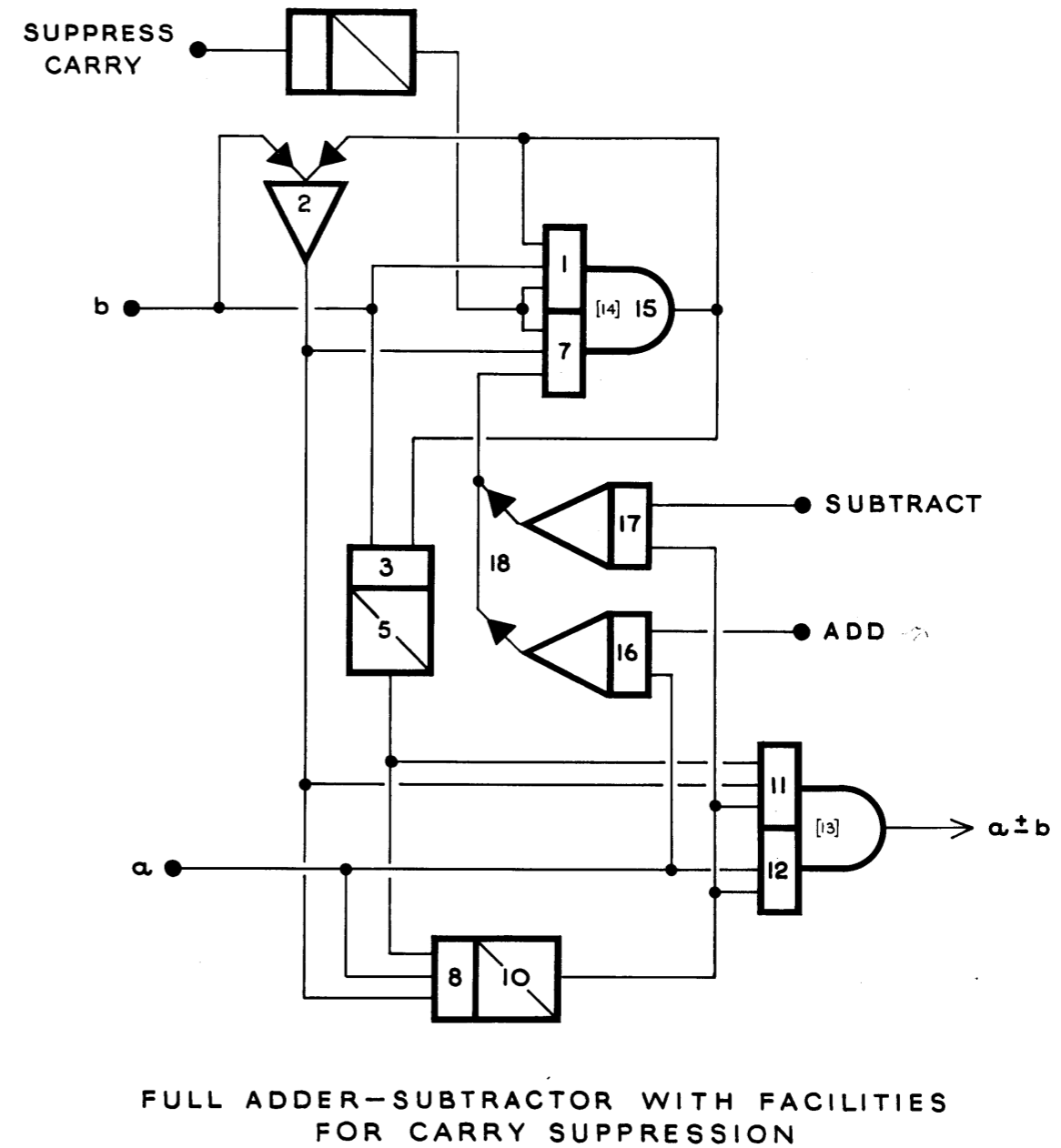
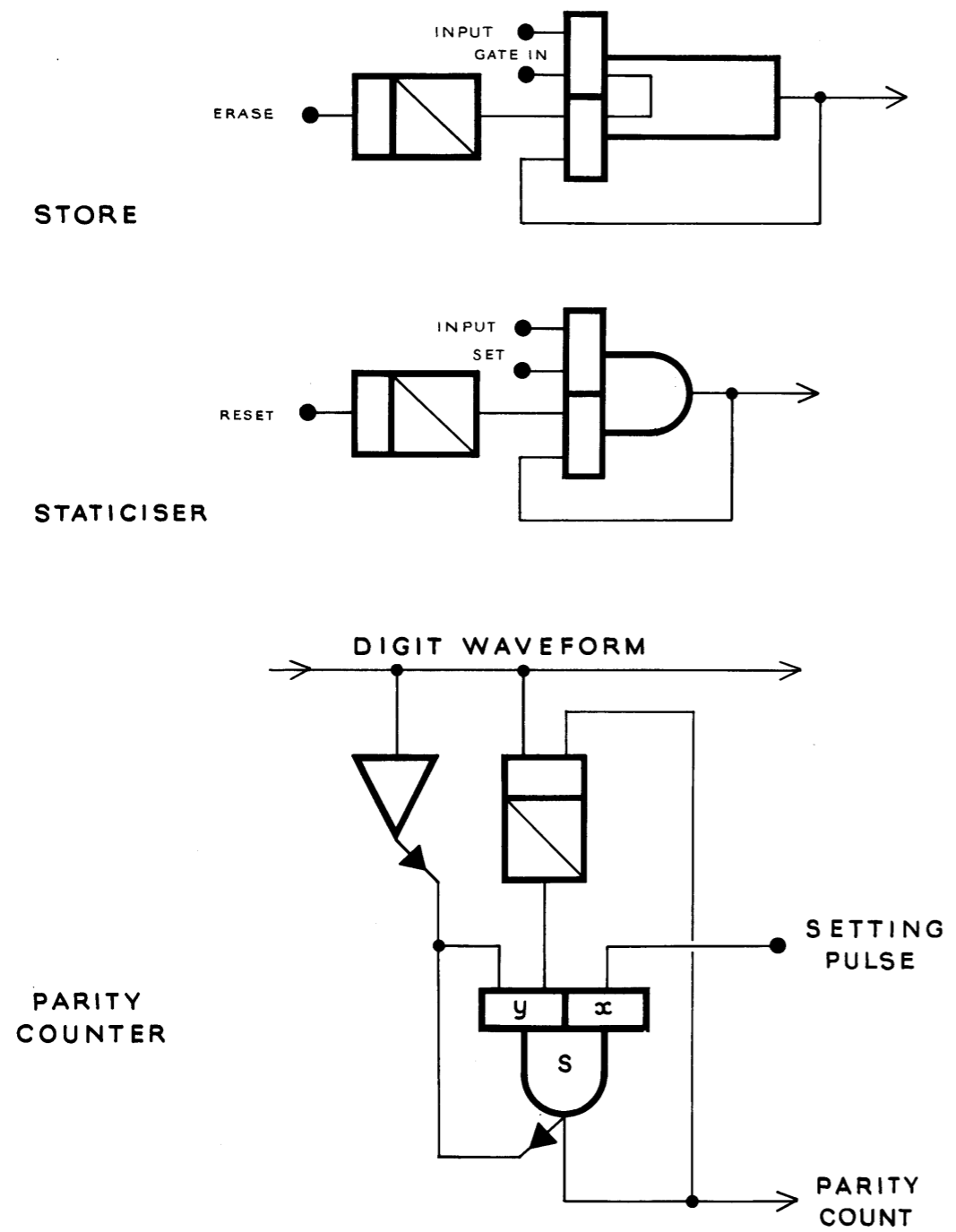


FIG.3.6 EXAMPLES WITH CONTRACTED SYMBOLS

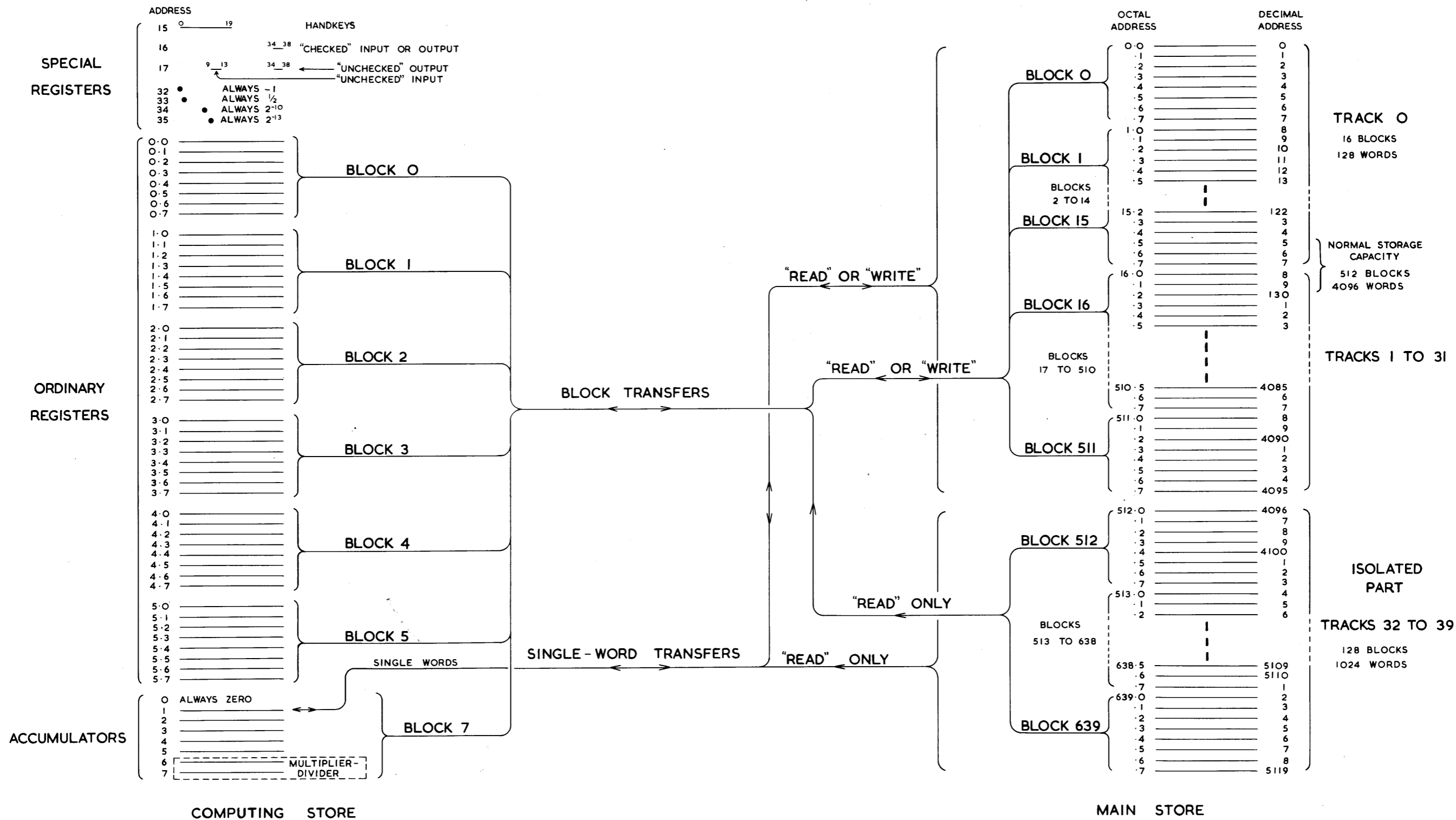


FIG. 4. I THE PEGASUS STORE

| Function | OPERATION | MODIFICATION | |
|----------|--|------------------------|---|
| 00 | $x' = n$ | Last three digits to N | |
| 01 | $x' = x + n$ | | |
| 02 | $x' = -n$ | | |
| 03 | $x' = x - n$ | | |
| 04 | $x' = n - x$ | | |
| 05 | $x' = x \& n$ | | |
| 06 | $x' = x \neq n$ | | |
| 07 | | | |
| 10 | $n' = x$ | Last three digits to N | |
| 11 | $n' = n + x$ | | |
| 12 | $n' = -x$ | | |
| 13 | $n' = n - x$ | | |
| 14 | $n' = x - n$ | | |
| 15 | $n' = n \& x$ | | |
| 16 | $n' = n \neq x$ | | |
| 17 | | | |
| 20 | $p' + 2^{-38}q' = nx$ | Last three digits to N | |
| 21 | $p' + 2^{-38}q' = nx + 2^{-39}$ | | |
| 22 | $p' + 2^{-38}q' = nx + p + 2^{-38}q$ | | |
| 23 | $[q]' = \frac{p}{n} + 2^{-38}q$ (justify) — <i>n can be p but not always</i> | | |
| 24 | $nq' + 2^{-38}p' = x + 2^{-38}q$ | | { unrounded $0 \leq p'/n < 1$ rounded $-1/2 \leq p'/n < 1/2$ |
| 25 | | | |
| 26 | $nq' + 2^{-38}p' = x$ | | unrounded $0 \leq p'/n < 1$ |
| 27 | | | |
| 30 | | | |
| 31 | | | |
| 32 | | | |
| 33 | | | |
| 34 | | | |
| 35 | | | |
| 36 | | | |
| 37 | | | |

| Function | OPERATION | MODIFICATION |
|----------|--|--|
| 40 | $x' = c$ | Last ten digits to N |
| 41 | $x' = x + c$ | |
| 42 | $x' = -c$ | |
| 43 | $x' = x - c$ | |
| 44 | $x' = c - x$ | |
| 45 | $x' = x \& c$ | |
| 46 | $x' = x \neq c$ | |
| 47 | | |
| 50 | $x' = 2^N x$ | Last ten digits to N |
| 51 | $x' = 2^{-N} x$ (rounded) | |
| 52 | shift x up N places | |
| 53 | shift x down N places | |
| 54 | $p' + 2^{-38}q' = 2^N(p + 2^{-38}q)$ | |
| 55 | $p' + 2^{-38}q' = 2^{-N}(p + 2^{-38}q)$ (unrounded) | |
| 56 | $p' + 2^{-38}q' = 2^\mu(p + 2^{-38}q)$ $x' = x - 2^{-38}\mu \uparrow$ | |
| 57 | | |
| 60 | Jump to N if $x = 0$ | Last ten digits to N |
| 61 | Jump to N if $x \neq 0$ | |
| 62 | Jump to N if $x \geq 0$ | |
| 63 | Jump to N if $x < 0$ | |
| 64 | Jump to N if overflow stat. clear (or clear overflow stat.) | |
| 65 | Jump to N if overflow stat. set (and clear overflow stat.) | |
| 66 | $x_m' = x_m + 1$ Jump to N if $x_m' \neq 0 \pmod{8}$ | |
| 67 | $x_c' = x_c - 1$ Jump to N if $x_c' \neq 0$ | |
| 70 | $1' = s$ | } Whole modifier } to N and X } First ten } digits to N } As for 70 } and 71 } As for 72 } and 73 |
| 71 | $s' = 1$ | |
| 72 | $u' = b$ | |
| 73 | $b' = u$ | |
| 74 | Energise external-conditioning relays associated with non-zero N-digits. | |
| 75 | (Interchange if buffer store fitted) | |
| 76 | STOP | |
| 77 | | |

\uparrow $\left. \begin{array}{l} 1/4 \leq p' < 1/2 \\ \text{or } -1/2 \leq p' < -1/4 \end{array} \right\}$ if $\mu < N-1$ otherwise $-1/4 \leq p' < 1/4$ and $\mu = N-1$

FIG. 4.2 THE ORDER CODE

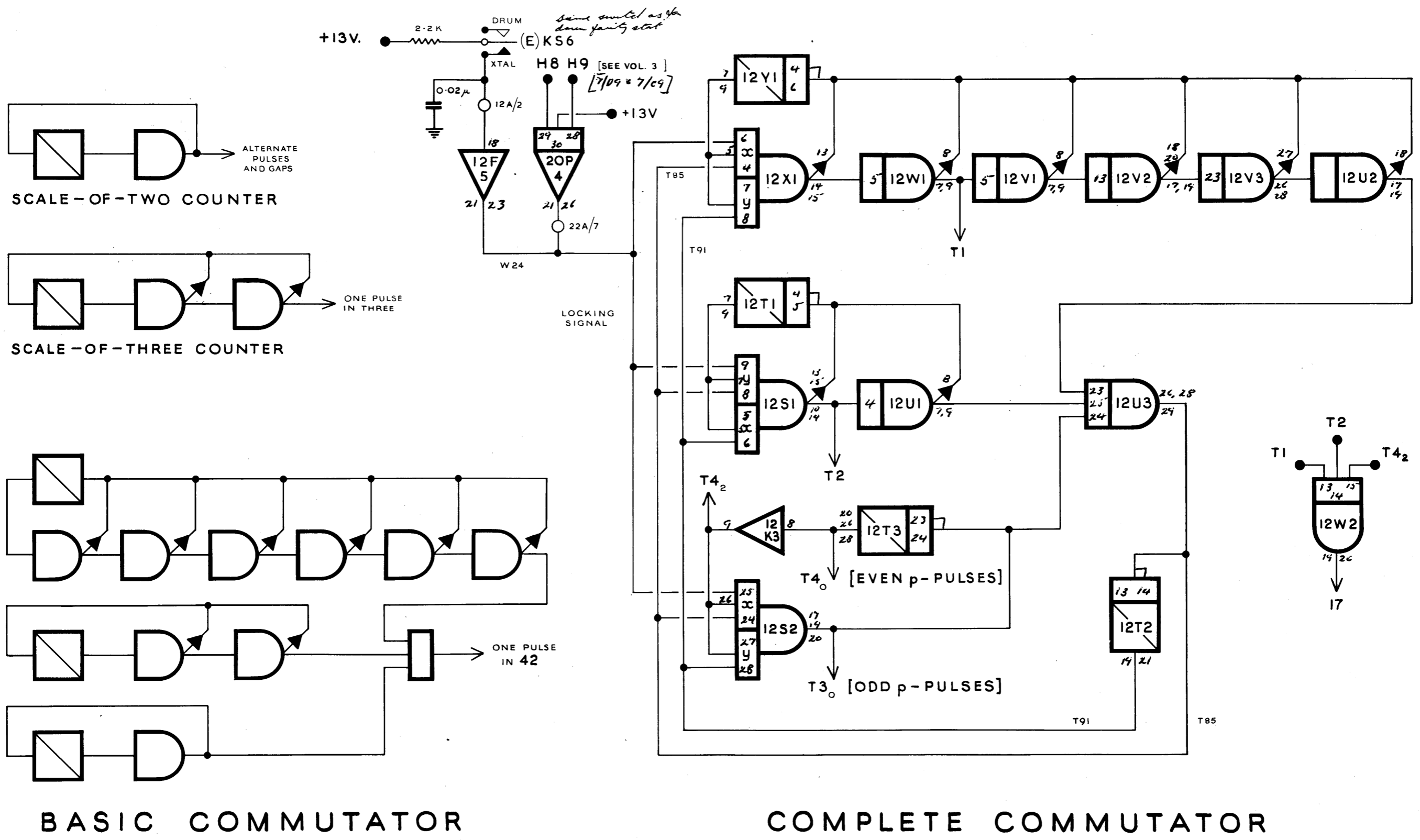


FIG. 5.1

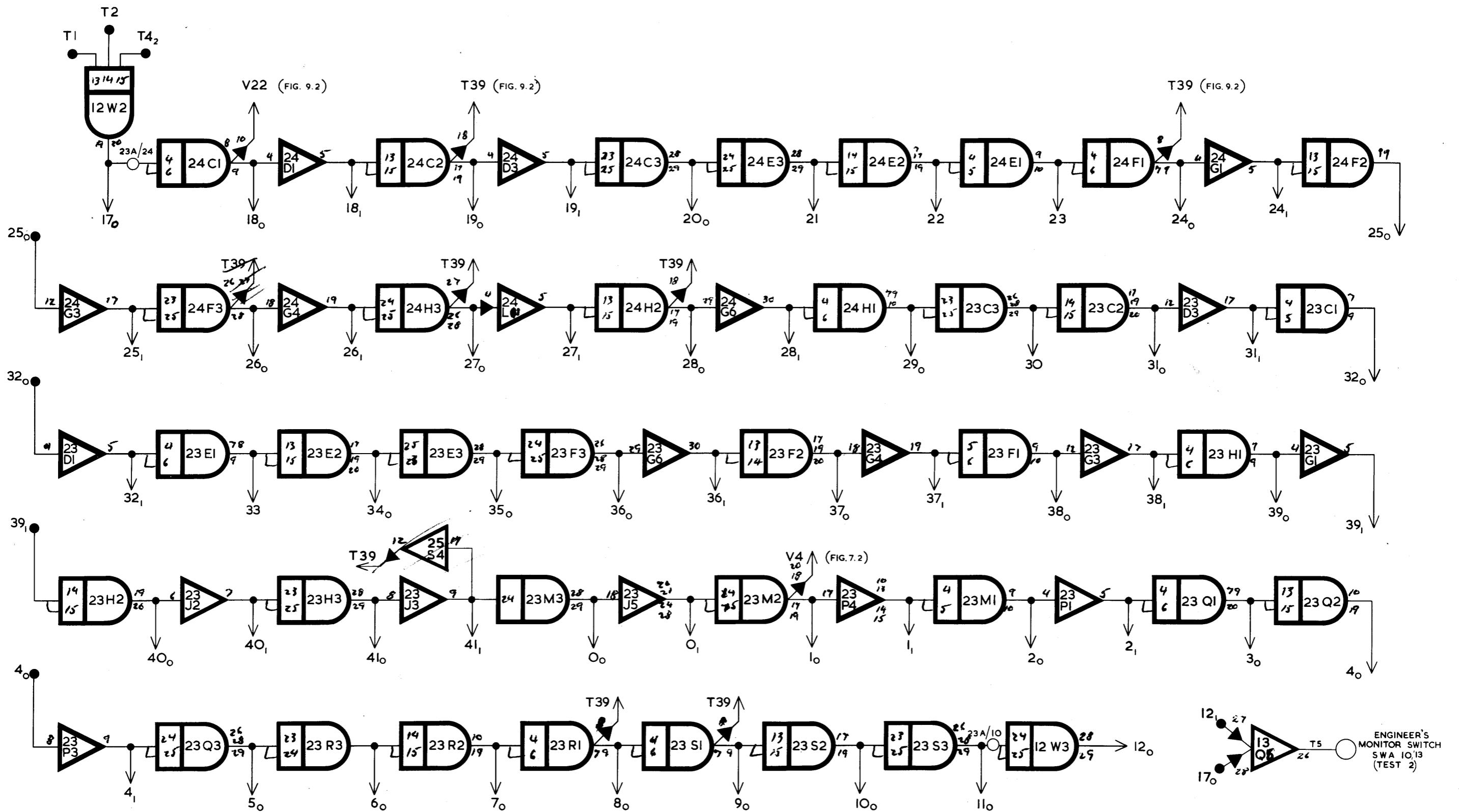


FIG. 5.2 p-PULSE GENERATOR.

SEE FIG. 5.3 FOR p-PULSE INVERTERS AND REPEATERS.

| Output | ELEMENT | Input |
|---------|----------------|---------|
| $p0_1$ | 23J5 | $p0_0$ |
| $p0_2$ | 25R3 | " |
| $p0_3$ | 12K1 | " |
| $p0_4$ | 12K2 | " |
| $p1_1$ | 23P4 | $p1_0$ |
| $p1_2$ | 32C5 | " |
| $p1_3$ | 12F6 (OR gate) | " |
| $p1_4$ | 13Q2 | " |
| $p2_1$ | 23P1 | $p2_0$ |
| $p2_2$ | 12F1 | " |
| $p3_1$ | 23P2 | $p3_0$ |
| $p3_2$ | 11V1 | " |
| $p4_1$ | 23P3 | $p4_0$ |
| $p5_1$ | 12F2 | $p5_0$ |
| $p6_1$ | 13S3 | $p6_0$ |
| $p7_1$ | 13S4 | $p7_0$ |
| $p8_1$ | 23D4 | $p8_0$ |
| $p9_1$ | 13S6 | $p9_0$ |
| $p10_1$ | 13U4 | $p10_0$ |
| $p11_1$ | 13R1 | $p11_0$ |
| $p12_1$ | 13R3 | $p12_0$ |
| $p18_1$ | 24D1 | $p18_0$ |
| $p18_2$ | 24D6 | " |
| $p19_1$ | 24D3 | $p19_0$ |
| $p20_1$ | 24D4 | $p20_0$ |
| $p24_1$ | 24G1 | $p24_0$ |
| $p25_1$ | 24G3 | $p25_0$ |
| $p26_1$ | 24G4 | $p26_0$ |
| $p26_2$ | 13Q3 | " |

| Output | ELEMENT | Input |
|---------|---------------------|---------|
| $p27_1$ | 24L6 (OR gate) | $p27_0$ |
| $p28_1$ | 24G6 | $p28_0$ |
| $p28_2$ | 25S2 | " |
| $p29_1$ | 32D3 | $p29_0$ |
| $p29_2$ | 13R6 | " |
| $p31_1$ | 23D3 | $p31_0$ |
| $p32_1$ | 23D1 | $p32_0$ |
| $p34_2$ | 13T1 | $p34_0$ |
| $p35_1$ | 13T3 | $p35_0$ |
| $p36_1$ | 23G6 | $p36_0$ |
| $p36_2$ | 13Q4 | " |
| $p37_1$ | 23G4 | $p37_0$ |
| $p37_2$ | 23J4 | " |
| $p37_3$ | 13T4 | " |
| $p38_1$ | 23G3 | $p38_0$ |
| $p38_2$ | 31G4 | " |
| $p38_3$ | 13T6 | " |
| $p39_1$ | 23G1 | $p39_0$ |
| $p39_2$ | 13V1 | " |
| $p39_3$ | 20Q5 | " |
| $p39_4$ | 23J1 | " |
| $p39_5$ | 32C6 (OR gate) | " |
| $p39_6$ | 13U3 | " |
| $p40_1$ | 23J2 | $p40_0$ |
| $p40_2$ | 34P3 | " |
| $p40_3$ | 34M3 | " |
| $p40_4$ | 34M2 | " |
| $p40_5$ | 22P5 | " |
| $p40_6$ | 31E1 (single delay) | $p39_5$ |
| $p40_7$ | 11V6 | $p40_0$ |
| $p40_8$ | 13V2 | " |
| $p41_1$ | 23J3 | $p41_0$ |
| $p41_2$ | 35D1 | " |
| $p41_4$ | 13V4 | " |

| Output | ELEMENT | Input |
|--------------|--|--------------|
| $\sim p0_0$ | 23L3 (inverter) | $p0_0$ |
| $\sim p0_1$ | 30G5 | $\sim p0_0$ |
| $\sim p0_2$ | 25R1 | " |
| $\sim p0_3$ | 25R2 | " |
| $\sim p1_0$ | 23L1 (inverter) | $p1_0$ |
| $\sim p1_1$ | 31G5 | $\sim p1_0$ |
| $\sim p2$ | 22D3 (inverter) | $p2_0$ |
| $\sim p3_0$ | 23U2 (inverter) | $p3_0$ |
| $\sim p3_1$ | 11V4 | $\sim p3_0$ |
| $\sim p11_0$ | 23U1 (inverter) | $p11_0$ |
| $\sim p11_1$ | 22Q6 (OR gate) | $\sim p11_0$ |
| $\sim p12_0$ | 12Y3 (inverter, also generating V7) | $p12_0$ |
| $\sim p12_1$ | 11R1 (AND gate) | $\sim p12_0$ |
| $\sim p27$ | 22D2 (inverter) | $p27_0$ |
| $\sim p29$ | 23K3 (inverter) | $p29_0$ |
| $\sim p36$ | 26P1 (inverter) | $p36_0$ |
| $\sim p37$ | 33C3 (inverter) | $p37_0$ |
| $\sim p39_0$ | 23K1 (inverter) | $p39_0$ |
| $\sim p39_1$ | 31R1 | $\sim p39_0$ |
| $\sim p39_2$ | 34X2 | " |
| $\sim p40_0$ | 23K2 (inverter) | $p40_0$ |
| $\sim p40_1$ | 30R2 | $\sim p40_0$ |
| $\sim p40_2$ | 24U2 | " |
| $\sim p40_3$ | 34E2 | " |
| $\sim p40_4$ | 34M1 | " |
| $\sim p40_5$ | 34P2 | " |
| $\sim p40_6$ | 13V2 | " |
| $\sim p41$ | 23L2 | $p41_0$ |
| $\sim p41_1$ | 30R3 | $\sim p41_0$ |
| $\sim p41_2$ | 25S1 | " |

FIG. 5.3 p-PULSE REPEATERS AND INVERTERS

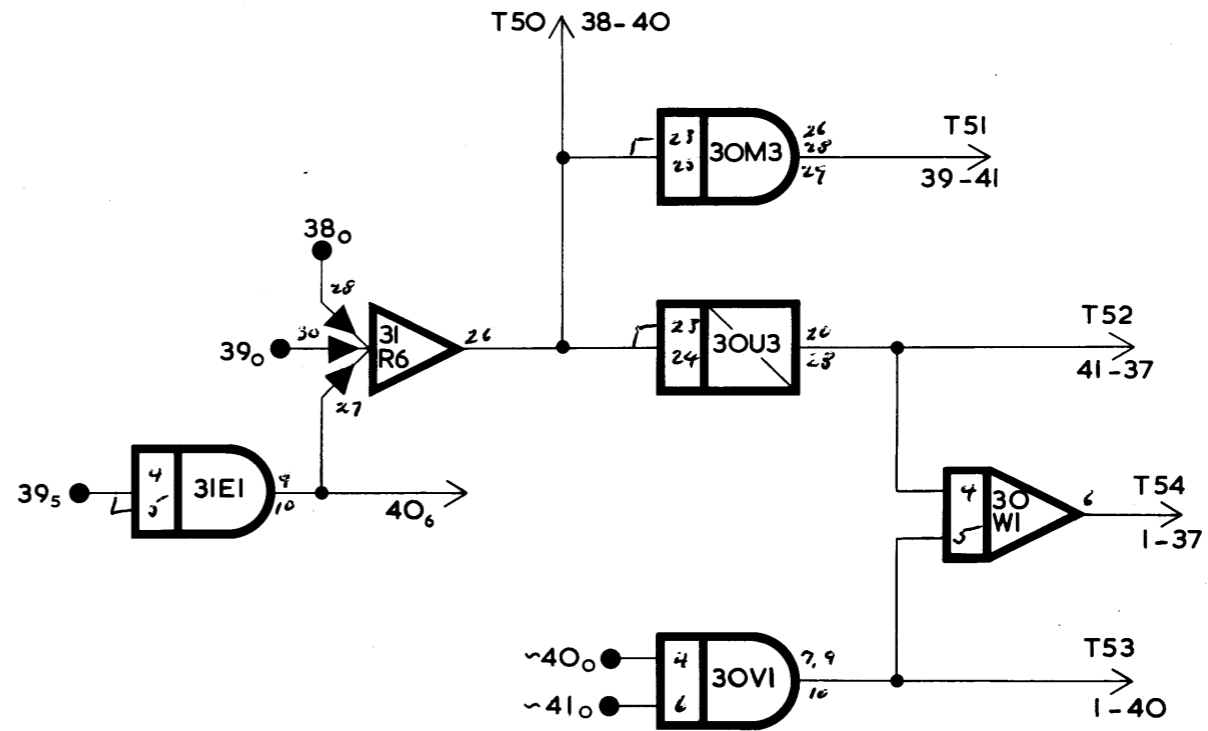
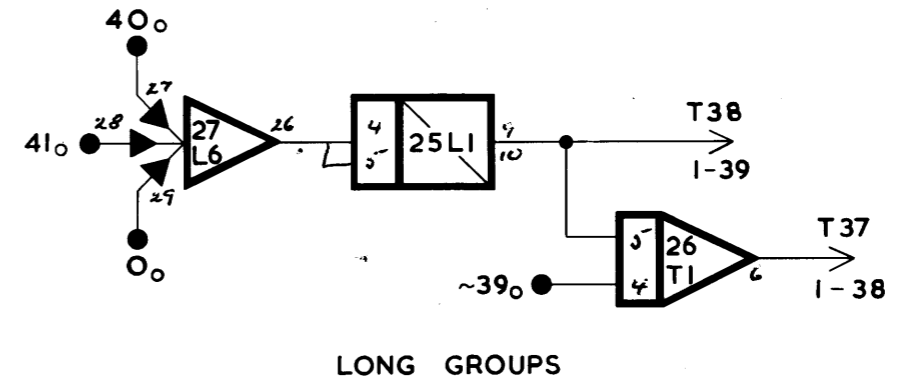
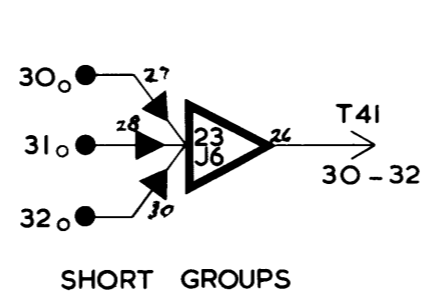
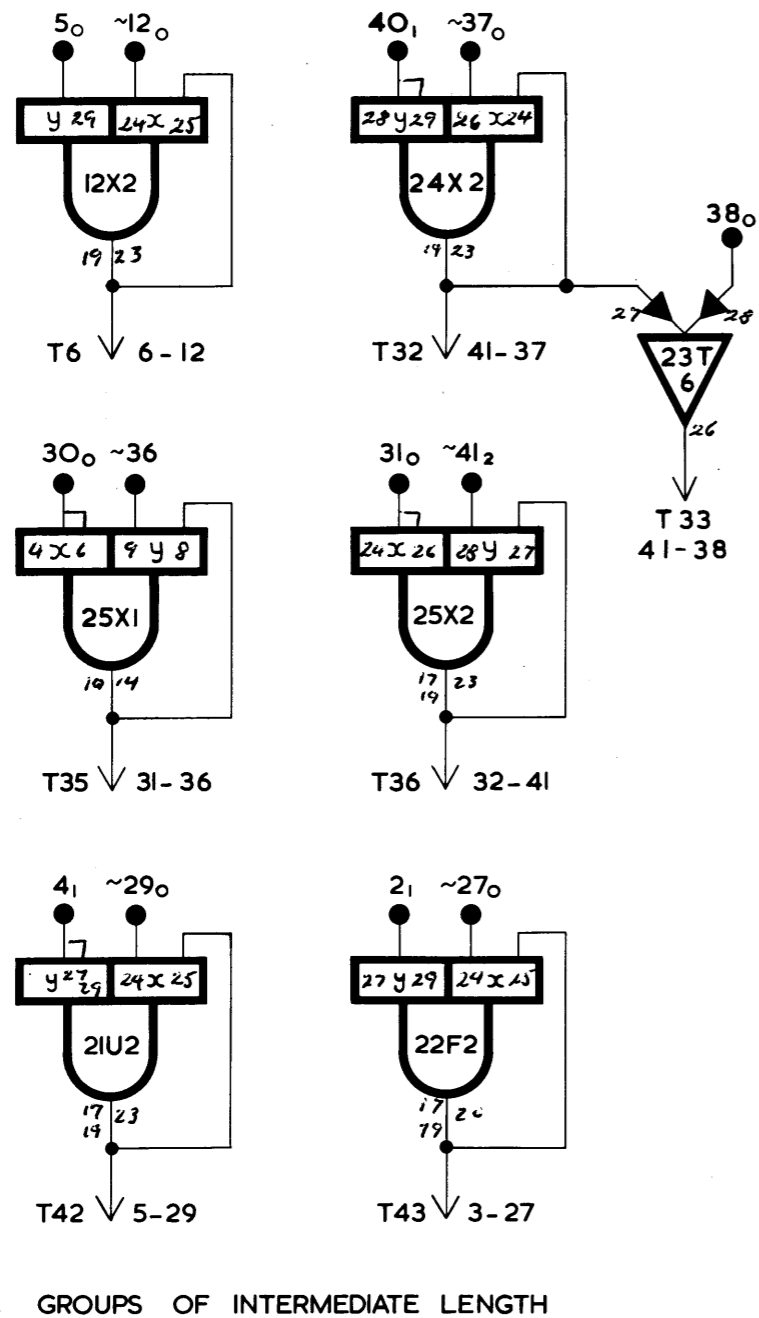


FIG. 5.4 THE GENERATION OF p -PULSE GROUPS.

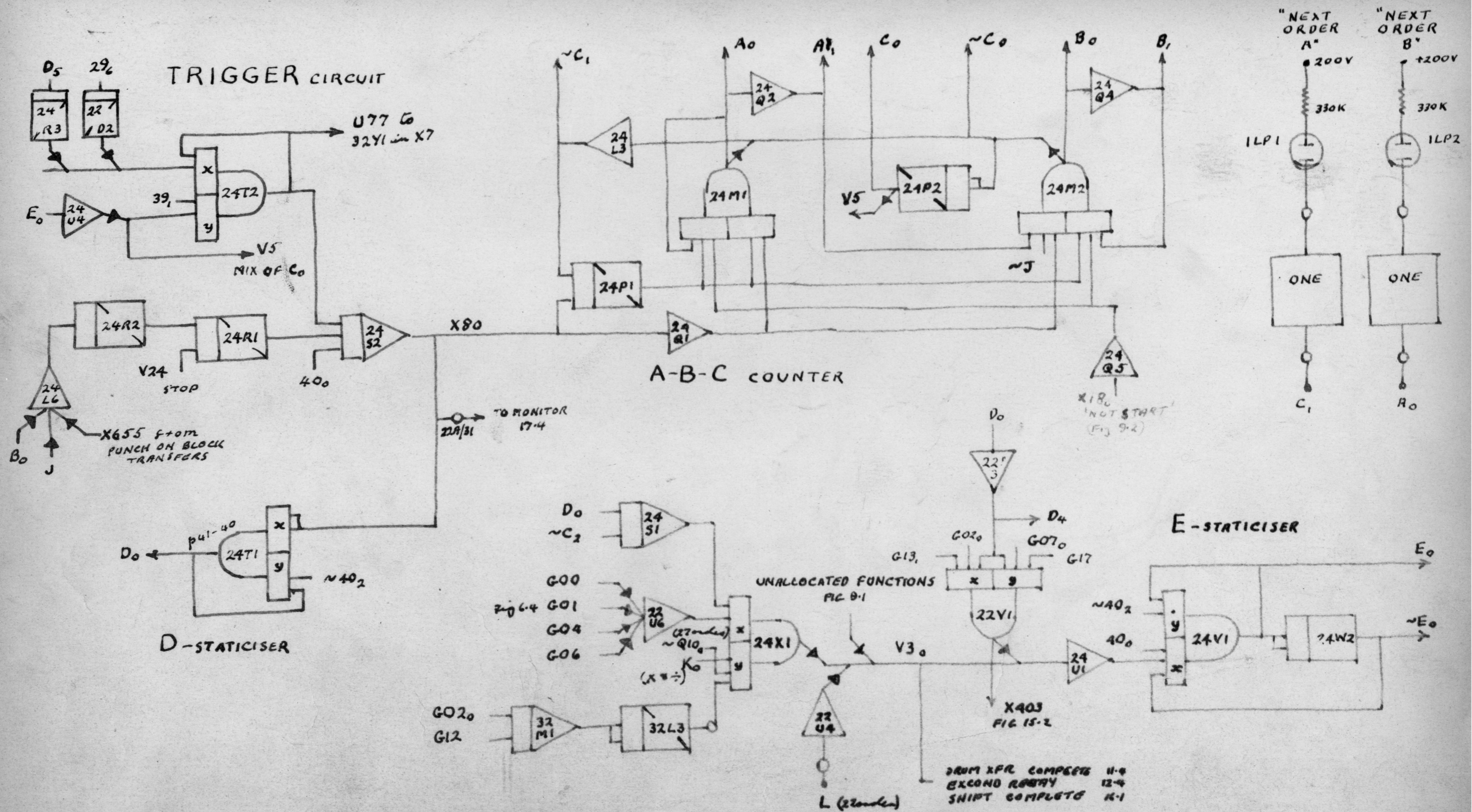
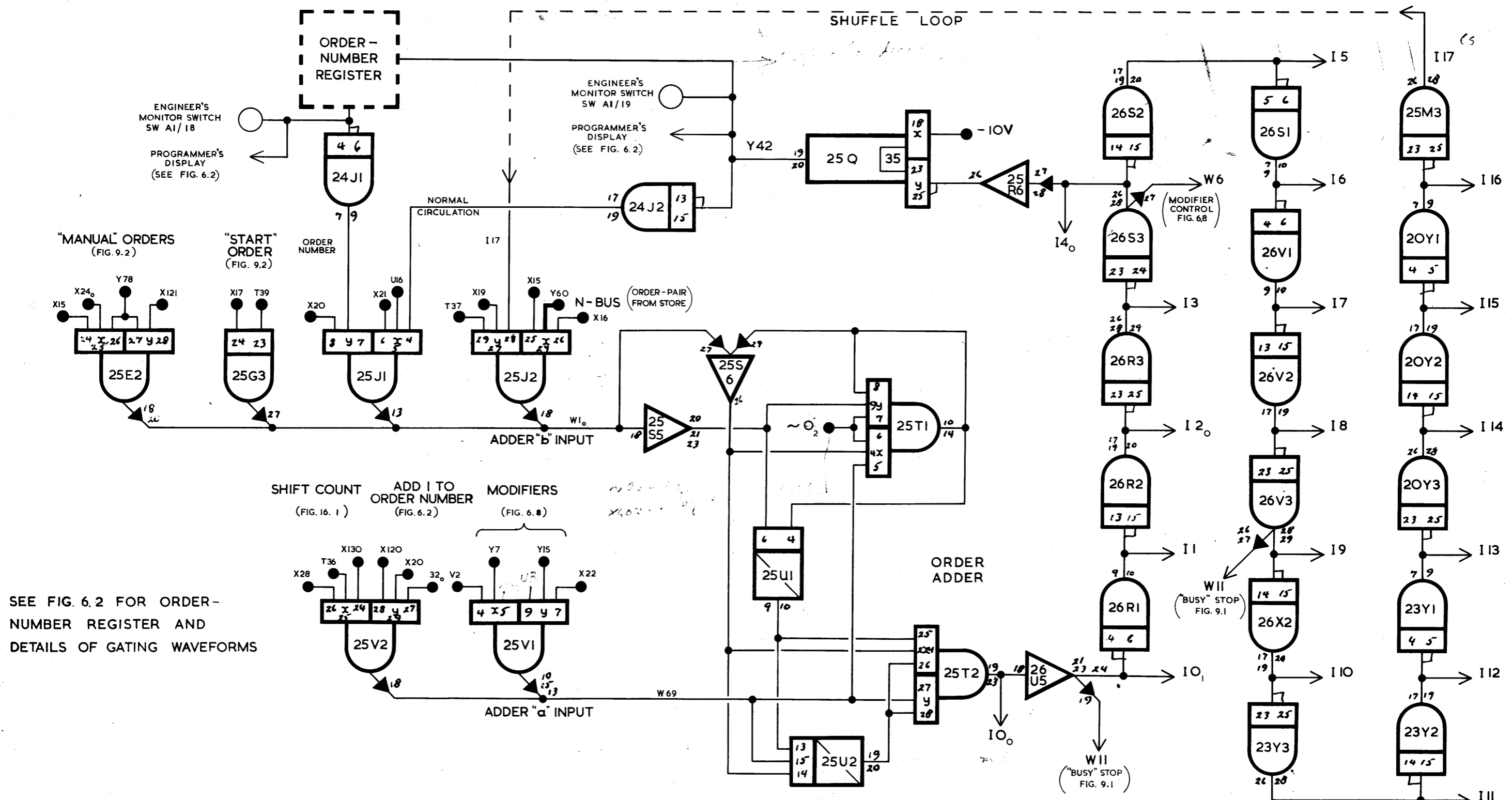


FIG 5.5 BEAT CONTROL



SEE FIG. 6.2 FOR ORDER-NUMBER REGISTER AND DETAILS OF GATING WAVEFORMS

FIG. 6.1 THE ORDER REGISTER.

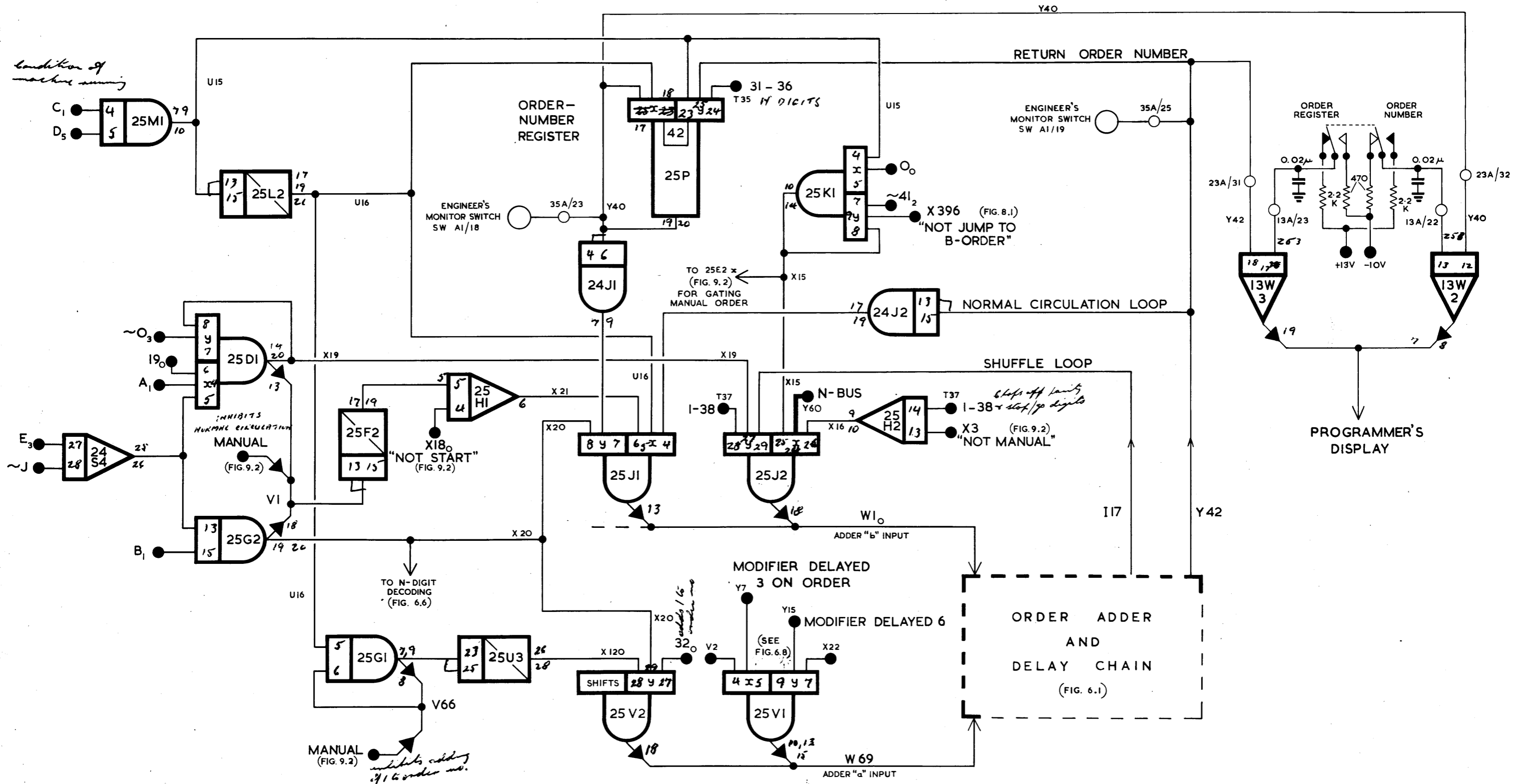
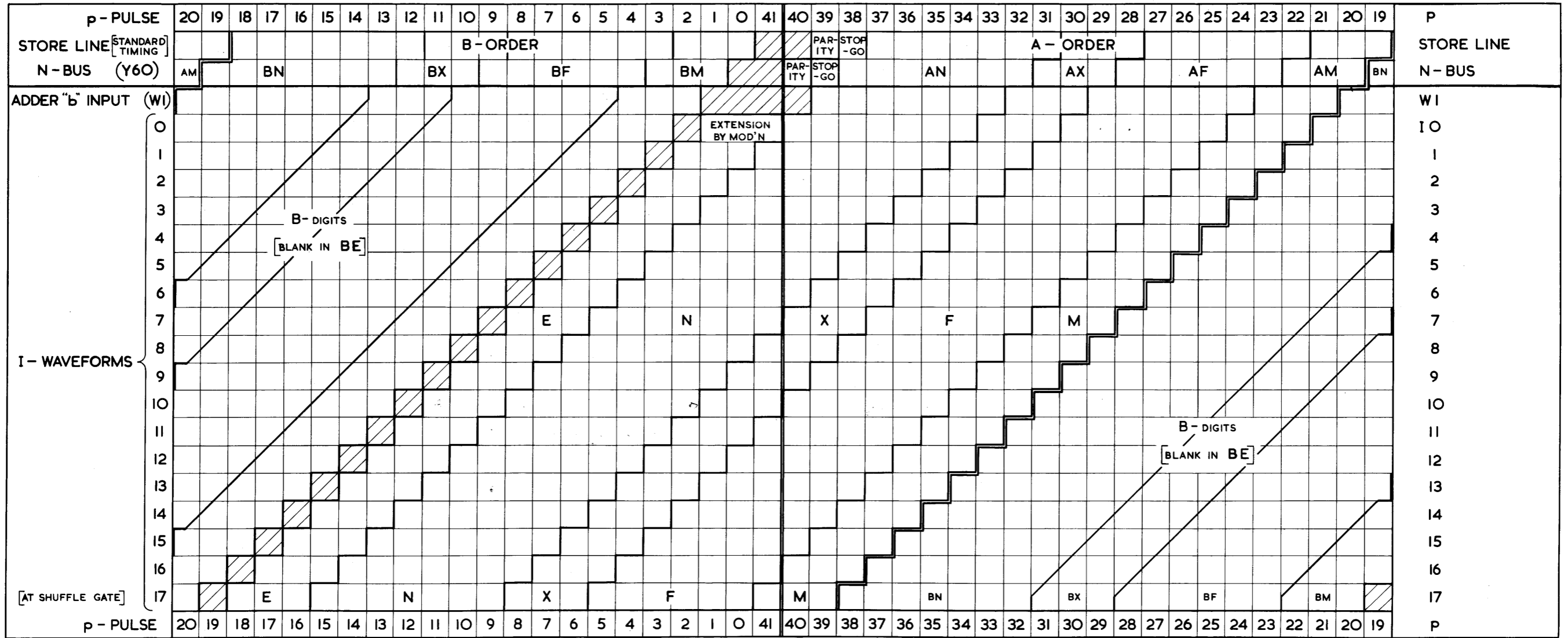


FIG. 6.2 NORMAL ENTRIES TO THE ORDER REGISTER.



MORE SIGNIFICANT

← TIME →

LESS SIGNIFICANT

GAP DIGIT
[ALWAYS ZERO]



THIS DIAGRAM SHOWS HOW THE DIGITS OF AN ORDER ARE PARALLELED ON THE ORDER REGISTER DELAY CHAIN.

THE CURRENT ORDER (A BEFORE SHUFFLE ; B AFTER SHUFFLE) LIES BETWEEN THE ROW OF BLANKS AND THE DOUBLE STEPPED LINE.

DIGITS IN THE LESS SIGNIFICANT HALF-WORD ARE NOT SENSED ; THE B-ORDER GROUPS IN THIS POSITION ARE ONLY SUGGESTED.

IN BE THE ORDER NUMBER APPEARS IN PLACE OF THE LEAST SIGNIFICANT 6 N-DIGITS, ALL OTHER DIGITS BEING ZERO.

NOTE THAT THE ORDER-PAIR APPEARS ON THE N-BUS IN CD ONLY, BUT IS SHOWN CONTINUOUSLY TO PRESERVE THE SEQUENCE.

FIG. 6.3 THE ORDER REGISTER (INTERNAL)

SEE ALSO TIMING CHART 5

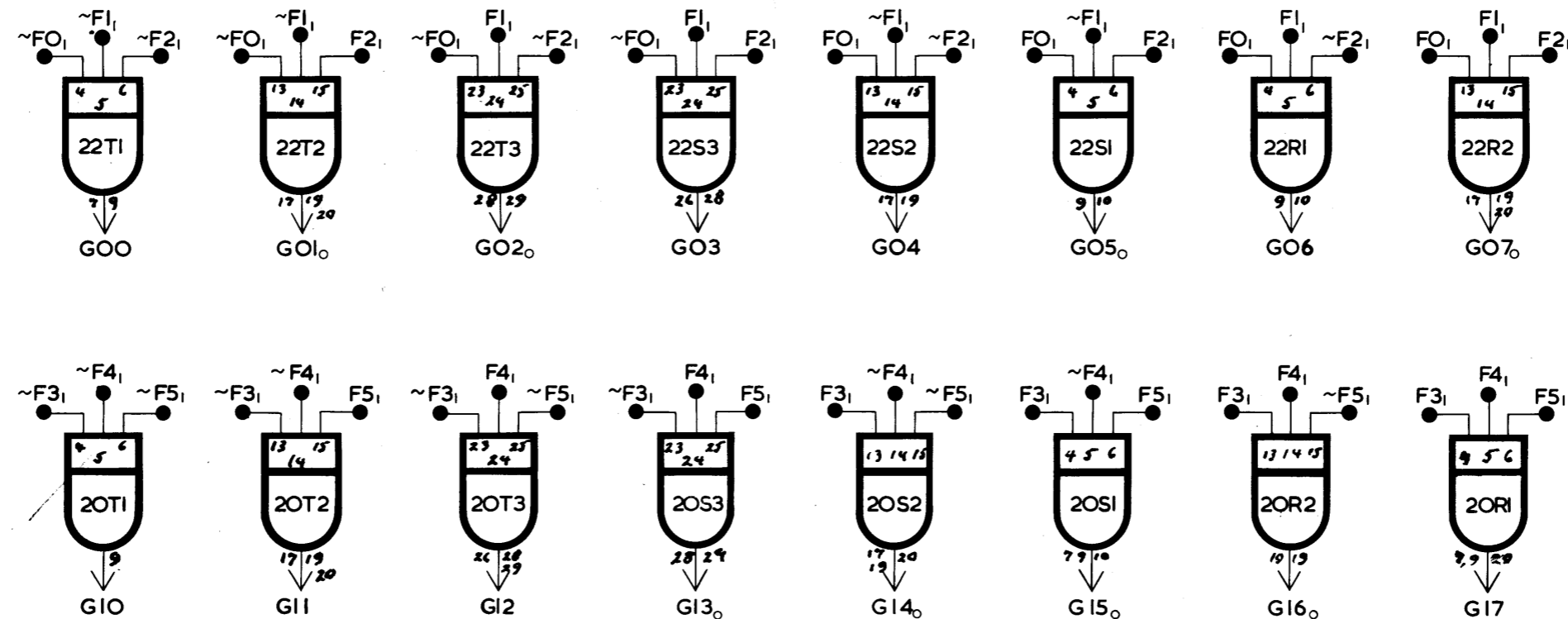
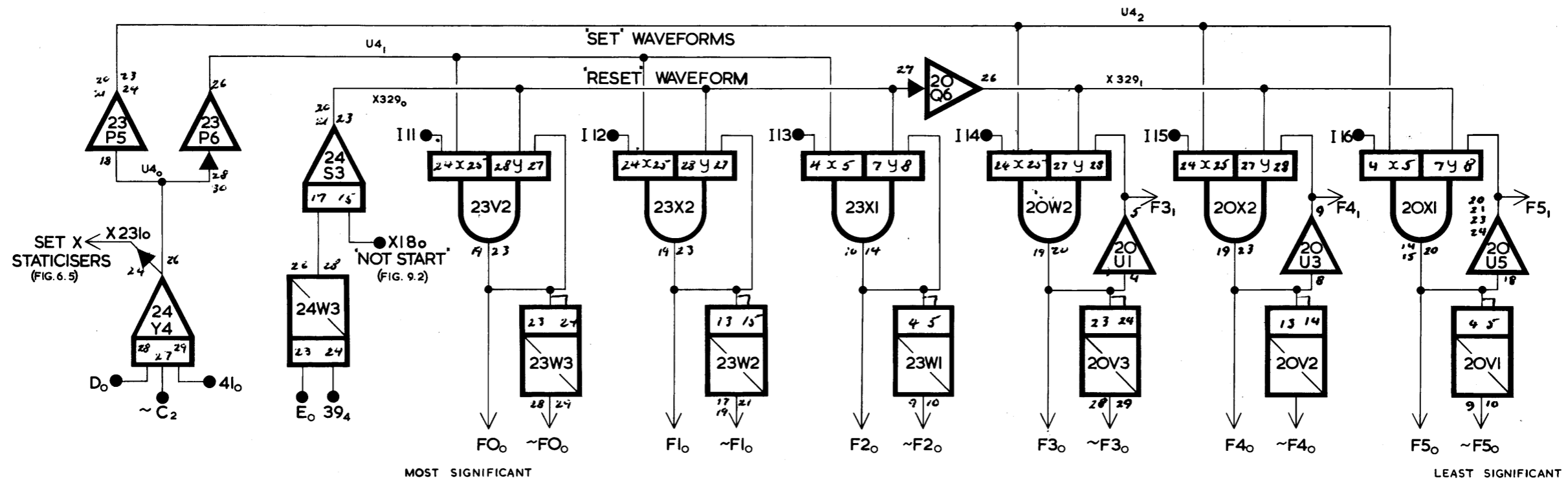


FIG. 6.4 FUNCTION DECODING

SEE FIG. 6.9 FOR REPEATERS ETC.

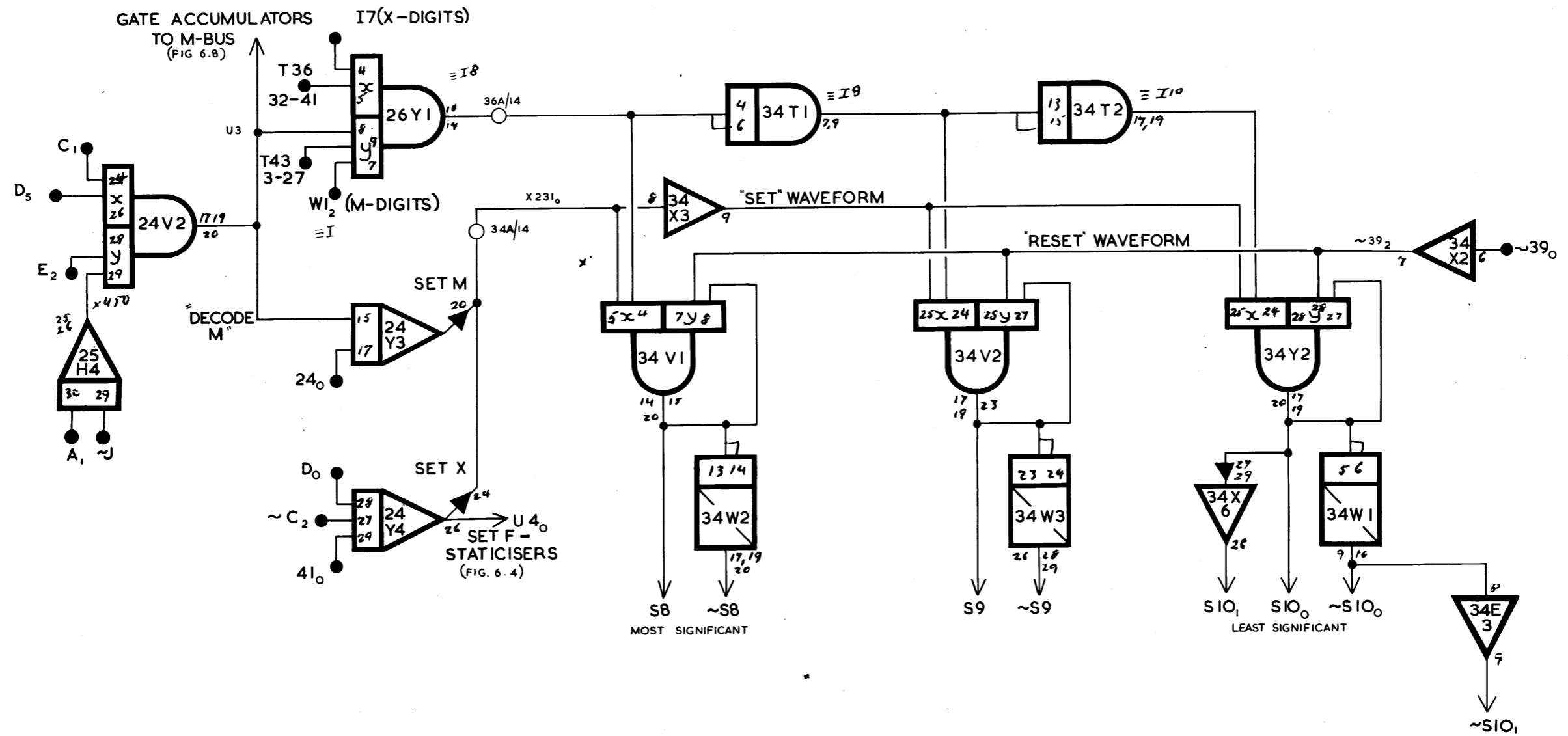


FIG. 6.5 X-DIGIT AND M-DIGIT DECODING

SEE FIG. II.7 FOR CIRCUIT
 DETAILS IN MAIN-STORE TRANSFERS

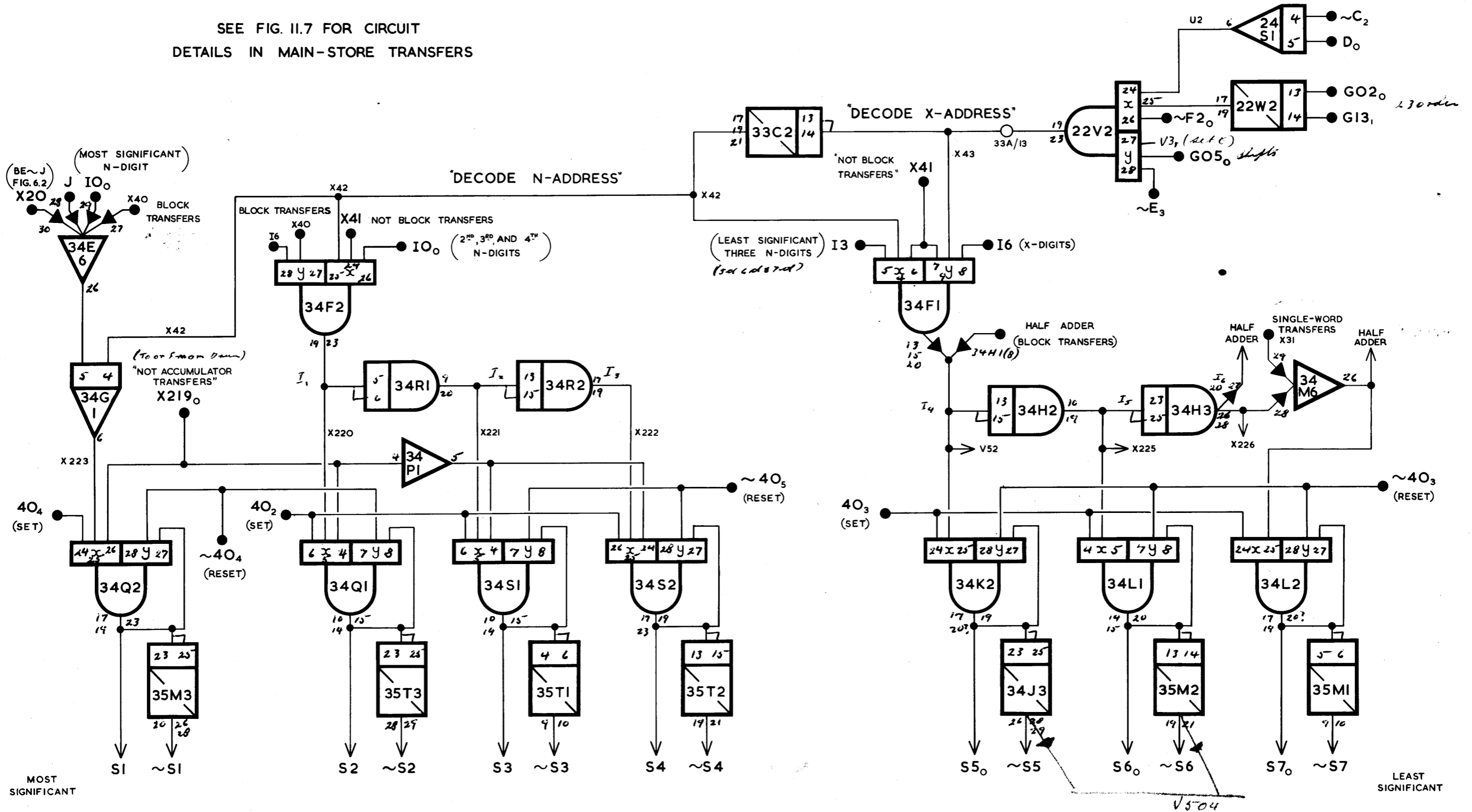
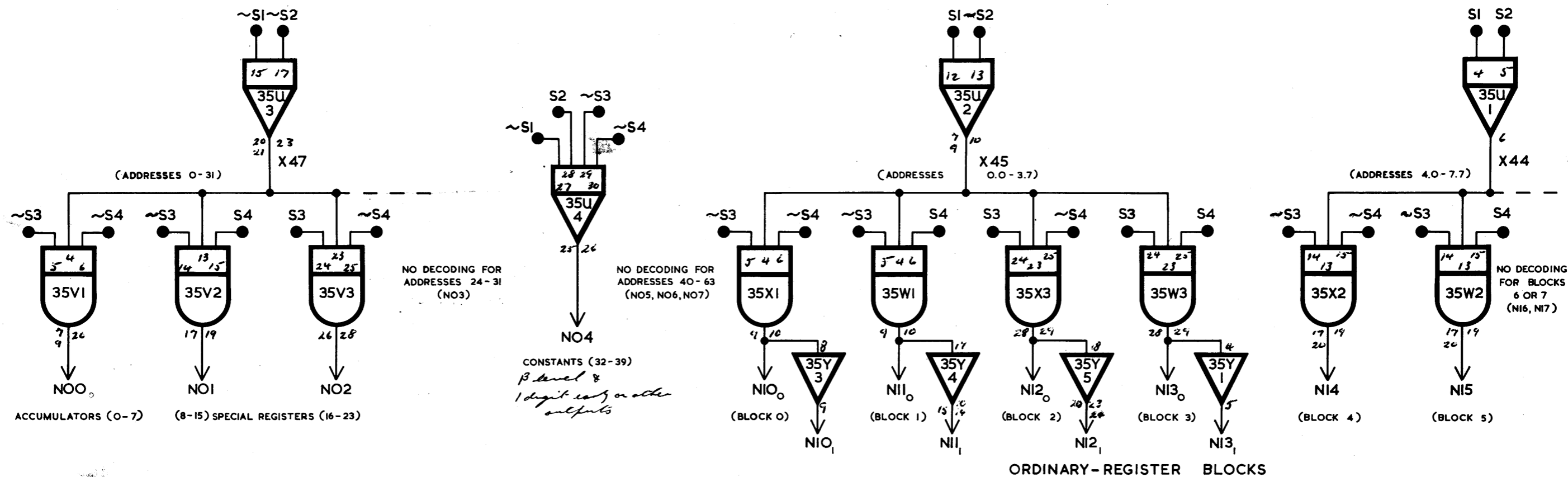


FIG. 6.6 N-DECODING (FIRST STAGE)



DECODING WITHIN BLOCKS (BELOW)

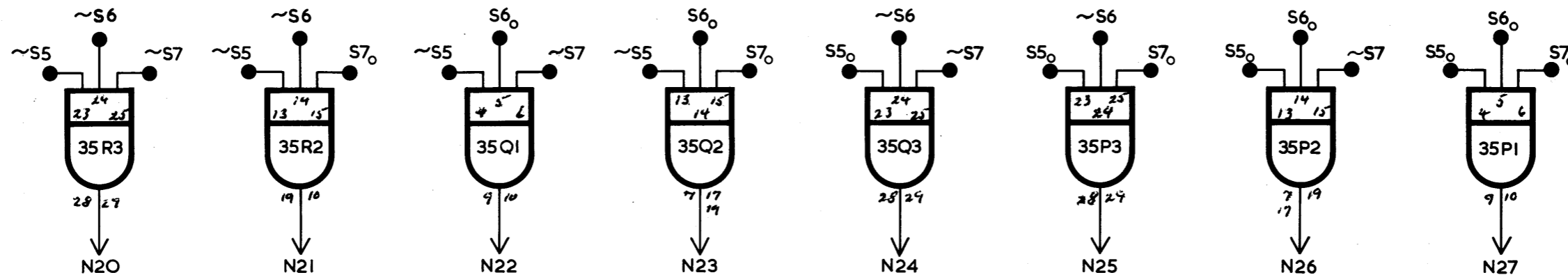


FIG. 6.7 N - DECODING (SECOND STAGE)

| Output | ELEMENT | Input |
|-----------------|----------------------------|-----------------|
| A ₁ | 24Q2 (monitor SW A11/4) | A ₀ |
| B ₁ | 24Q4 (monitor SW A11/5) | B ₀ |
| C ₀ | 24P2 (inverter) | ~C ₀ |
| C ₁ | 24Q3 (monitor SW A11/6) | C ₀ |
| D ₁ | 31G2 | D ₀ |
| D ₂ | 32D1 (monitor SW A11/7) | " |
| D ₃ | 22P4 | " |
| D ₄ | 22P3 | " |
| D ₅ | 24L2 | " |
| D ₇ | 32D2 | " |
| E ₁ | 31R5 (monitor SW A11/8) | E ₀ |
| E ₂ | 24U4 | " |
| E ₃ | 24U5 | " |
| E ₄ | 24L5 | " |
| ~B | 24R2 (inverter) | B ₀ |
| ~C ₁ | 24L3 | ~C ₀ |
| ~C ₂ | 24P3 (inverter) | C ₀ |
| ~C ₃ | 12C2 (inverter) | C ₂ |
| ~D ₀ | 31J1 (inverter) | D ₀ |
| ~D ₁ | 31G1 | ~D ₀ |
| ~D ₂ | 24R3 (inverter) | D ₅ |
| ~D ₃ | 35Y2 | ~D ₀ |
| ~E ₀ | 24W2 (inverter) | E ₀ |
| ~E ₁ | 31G6 (OR gate) | ~E ₀ |
| ~E ₂ | 31G3 | " |
| ~E ₃ | 24U5 | " |
| ~E ₄ | 26U3 | " |
| ~E ₅ | 20D4 | " |
| ~E ₆ | 13U1 | " |

| Output | ELEMENT | Input |
|-----------------------------|----------------|-----------------------------|
| F _{0₁} | 22Q5 | F _{0₀} |
| F _{1₁} | 22U2 | F _{1₀} |
| F _{2₁} | 23T2 | F _{2₀} |
| F _{3₁} | 20U1 | F _{3₀} |
| F _{3₂} | 21K4 | " |
| F _{4₁} | 20U3 | F _{4₀} |
| F _{4₂} | 21K3 | " |
| F _{5₁} | 20U5 | F _{5₀} |
| F _{5₂} | 20Q1 | " |
| F _{5₃} | 32D4 | " |
| ~F _{0₁} | 22U1 | ~F _{0₀} |
| ~F _{1₁} | 22U3 | ~F _{1₀} |
| ~F _{2₁} | 22U5 | ~F _{2₀} |
| ~F _{3₁} | 20U2 | ~F _{3₀} |
| ~F _{3₂} | 21K2 | " |
| ~F _{4₁} | 20U4 | ~F _{4₀} |
| ~F _{5₁} | 20U6 (OR gate) | ~F _{5₀} |
| ~F _{5₂} | 20Q2 | " |

| Output | ELEMENT | Input |
|---|-----------------|---|
| G _{0₁} | 22Q1 | G _{0₀} |
| G _{0₂} | 22Q2 | G _{0₂} |
| G _{0₅} ₁ | 22Q3 | G _{0₅} ₀ |
| G _{0₅} ₂ | 32C4 | " |
| G _{0₇} | 20Q3 | G _{0₇} |
| G _{1₃} | 22P2 | G _{1₃} |
| G _{1₄} | 32C3 | G _{1₄} |
| G _{1₅} | 32C2 | G _{1₅} |
| G _{1₆} ₁ | 21K1 | G _{1₆} ₀ |
| G _{1₆} ₂ | 32C1 | " |
| ~G _{0₅} | 21V3 (inverter) | G _{0₅} ₁ |
| ~G _{0₇} | 22W3 (inverter) | G _{0₇} ₀ |
| ~G _{1₆} | 21Q3 (inverter) | G _{1₆} ₀ |

FIG. 6. 9 REPEATERS AND INVERTERS FOR RHYTHMIC WAVEFORMS AND F - AND G - WAVEFORMS

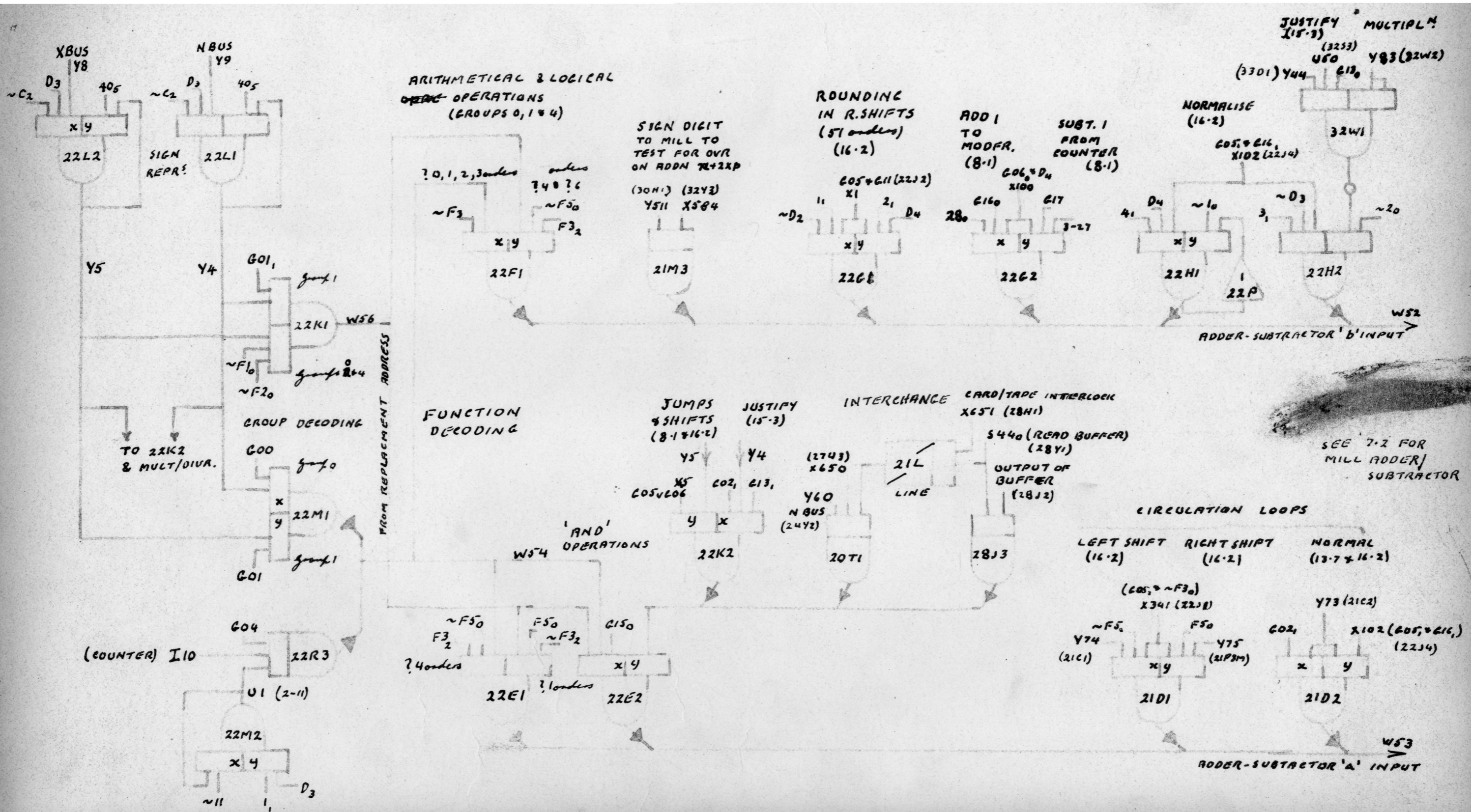


FIG. 7.1 ENTRIES TO THE MILL

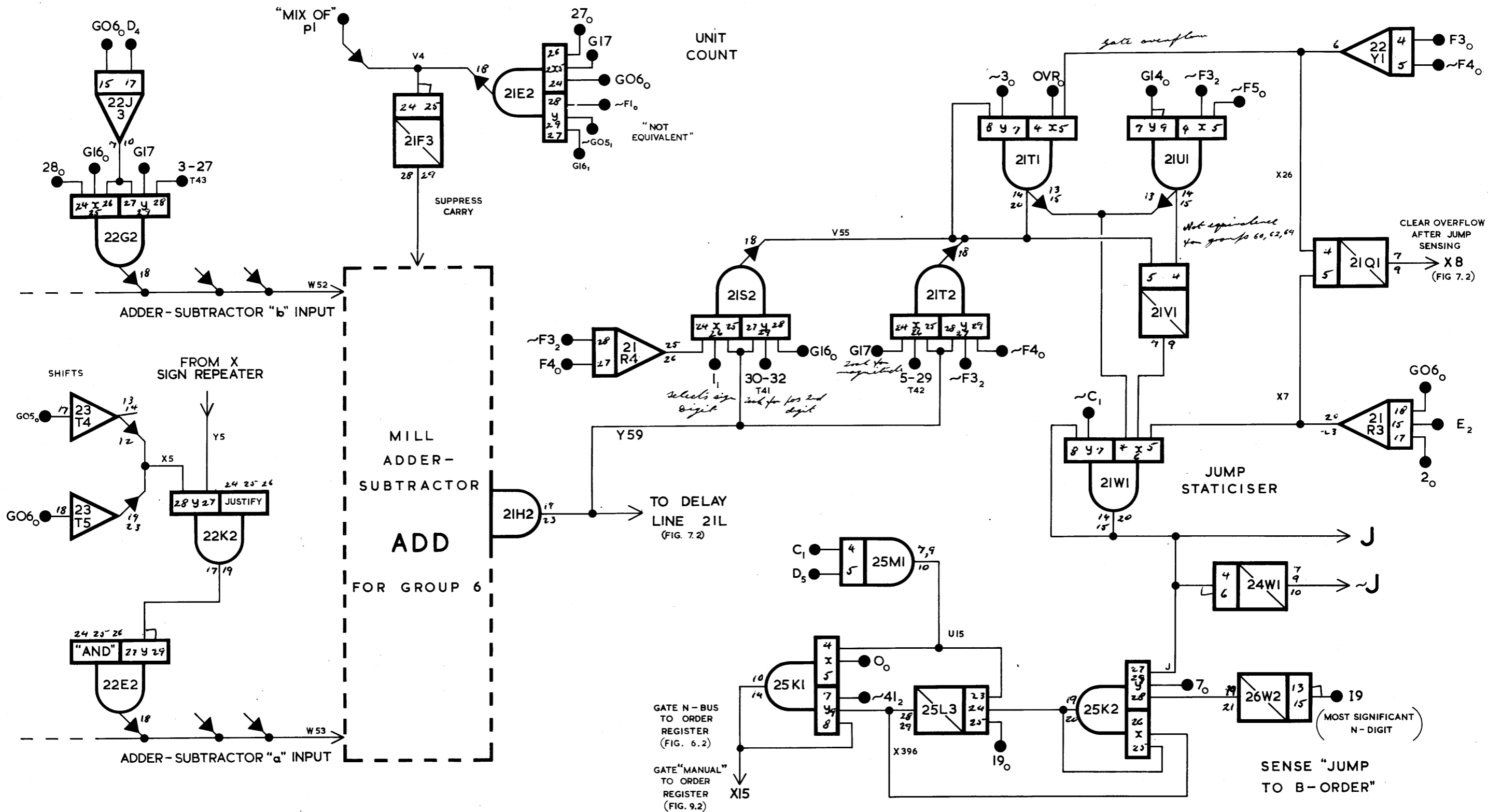


FIG. 8.1 JUMP - CONDITION TESTING

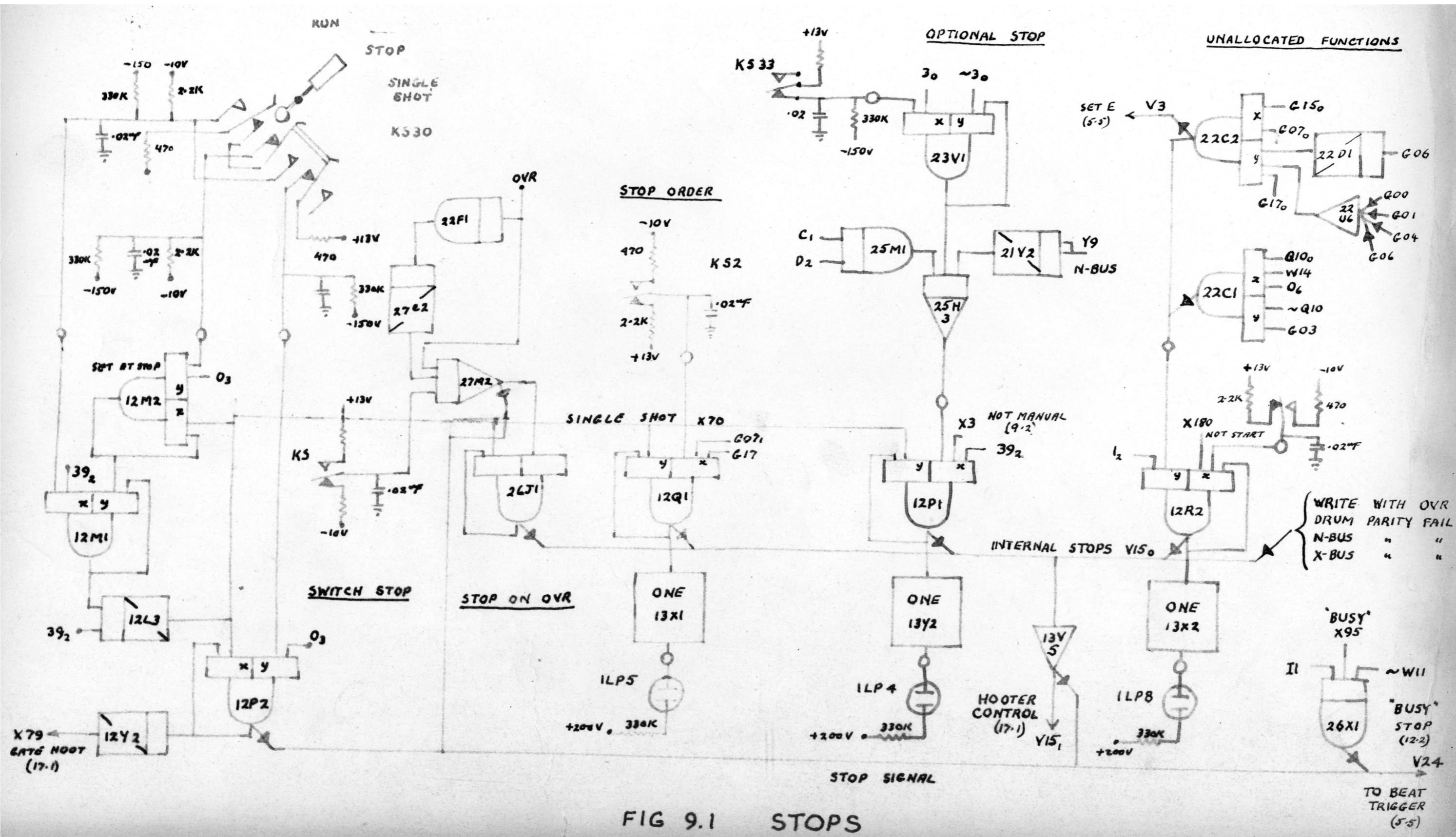


FIG 9.1 STOPS

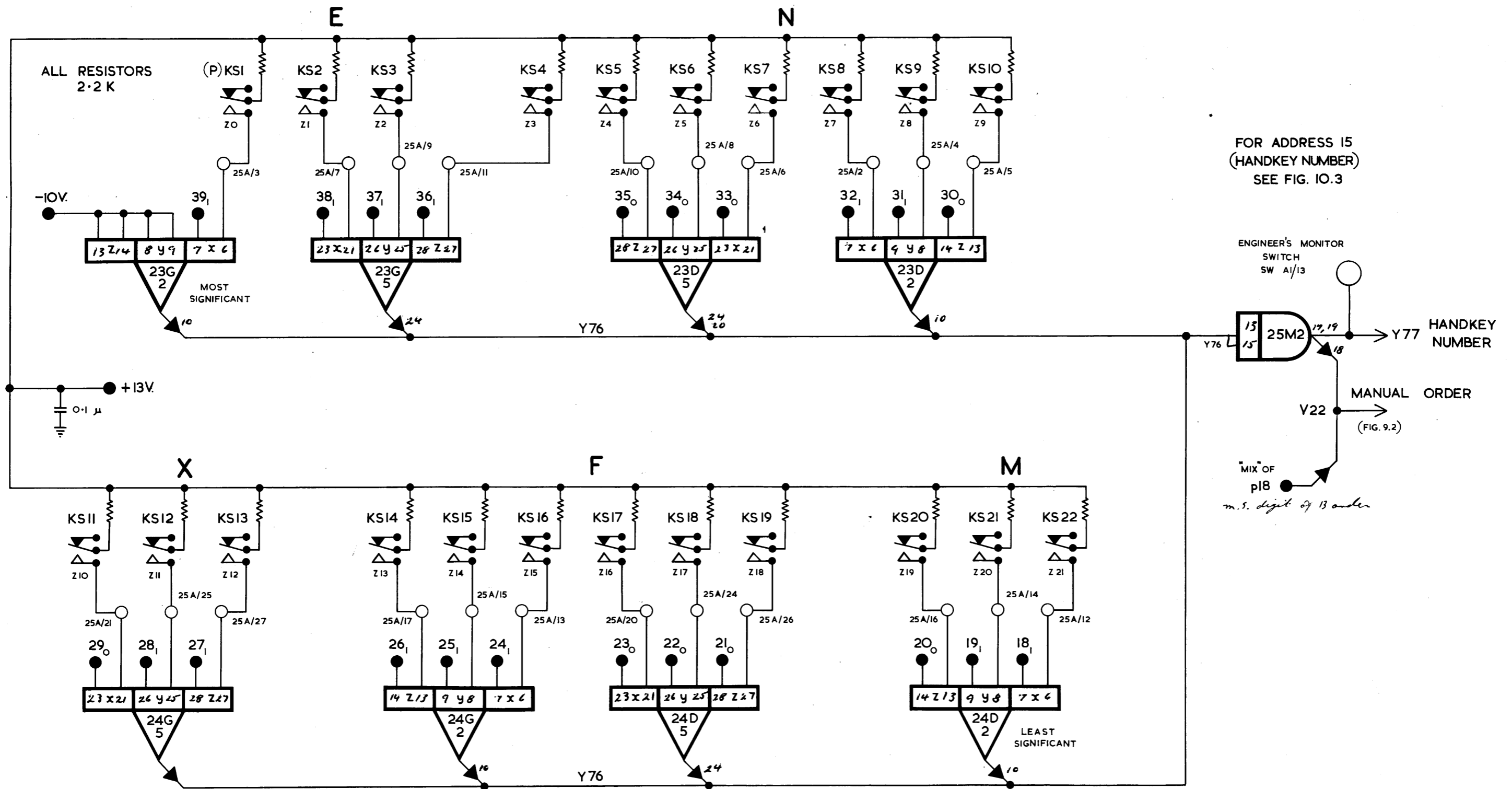


FIG. 9.3 HANDKEY CIRCUIT

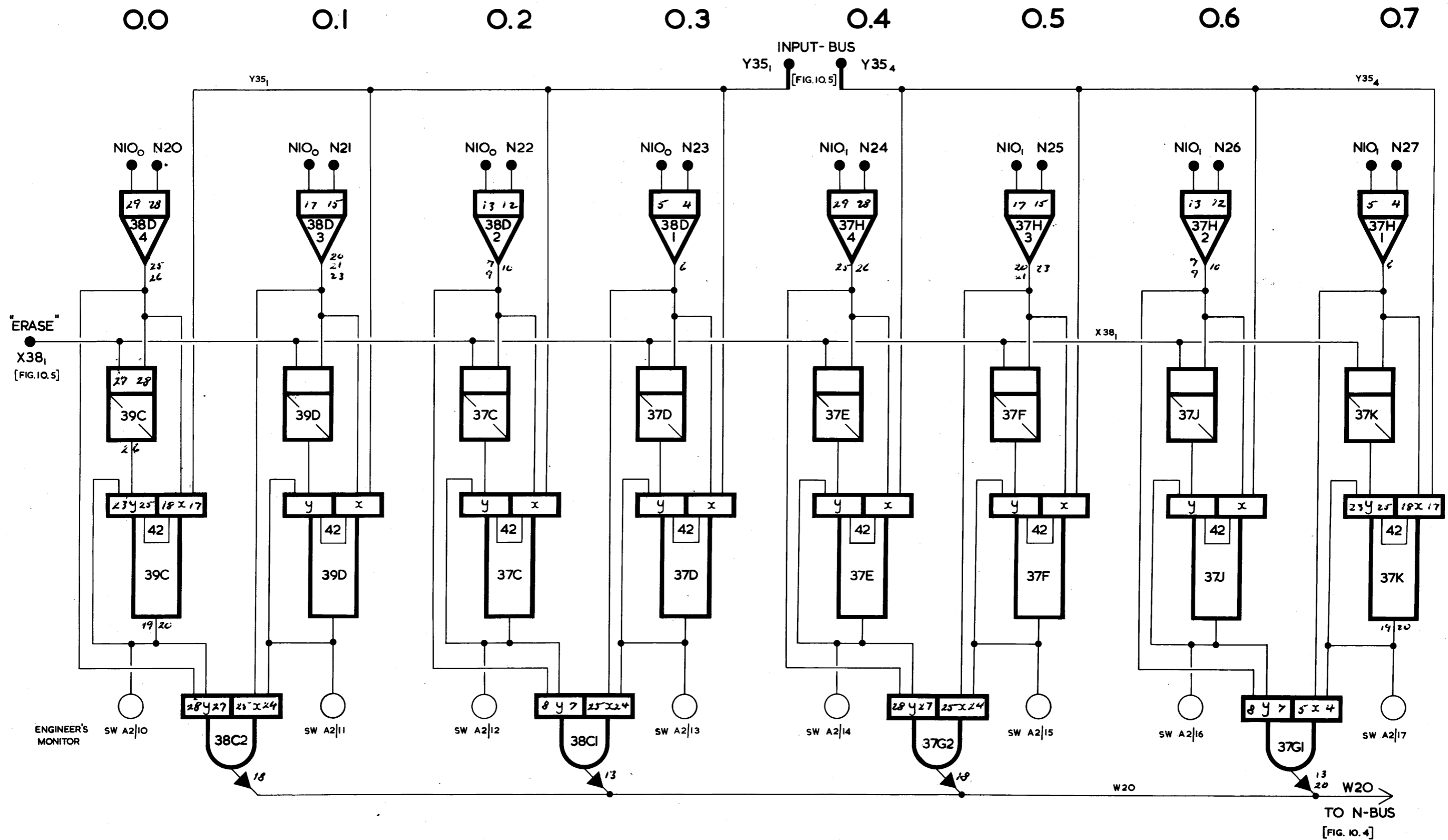


FIG. 10.1 ORDINARY REGISTERS [BLOCK O]

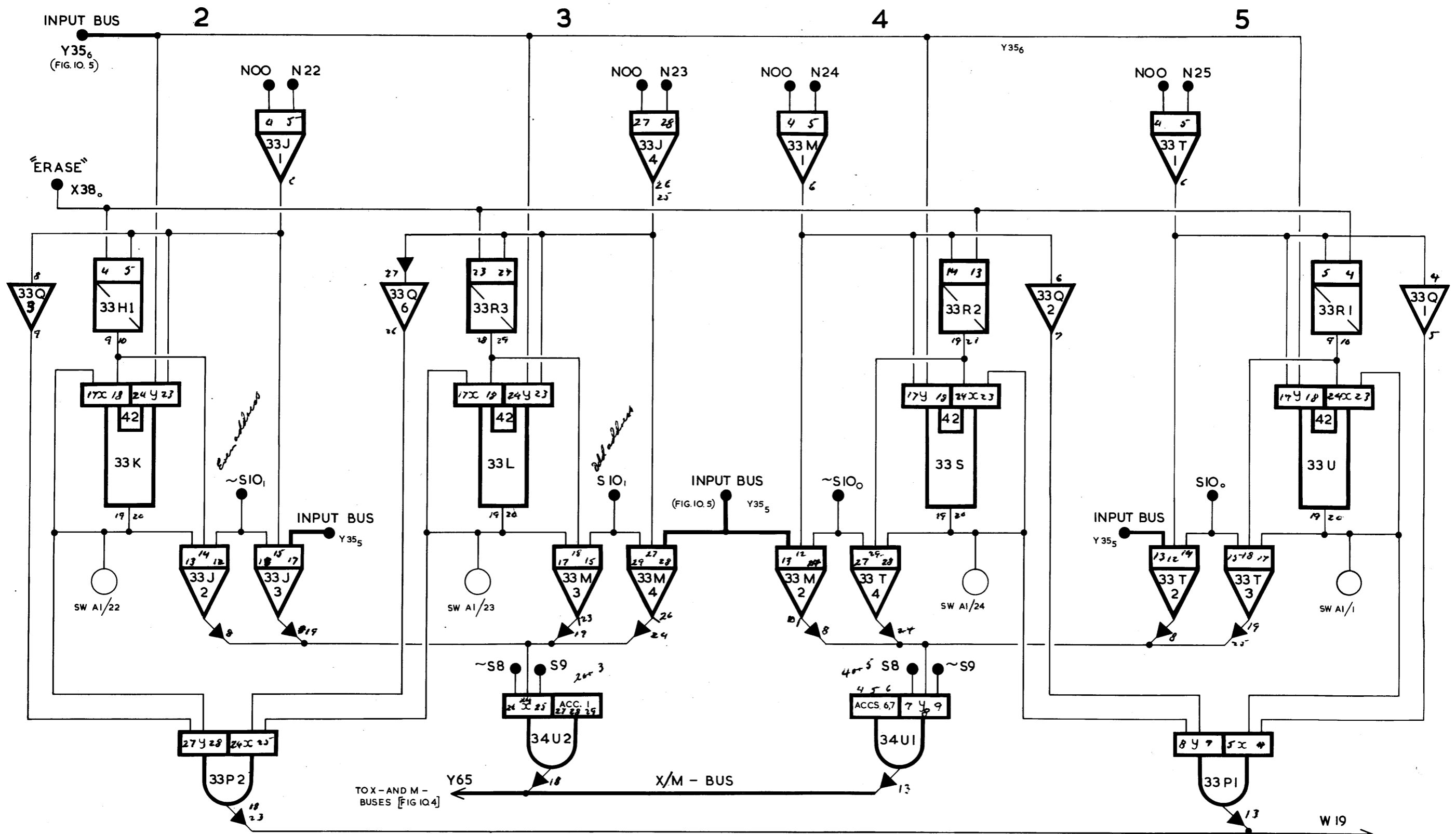


FIG. 10.2 ACCUMULATORS 2 TO 5

TO N-BUS [FIG 10.4]

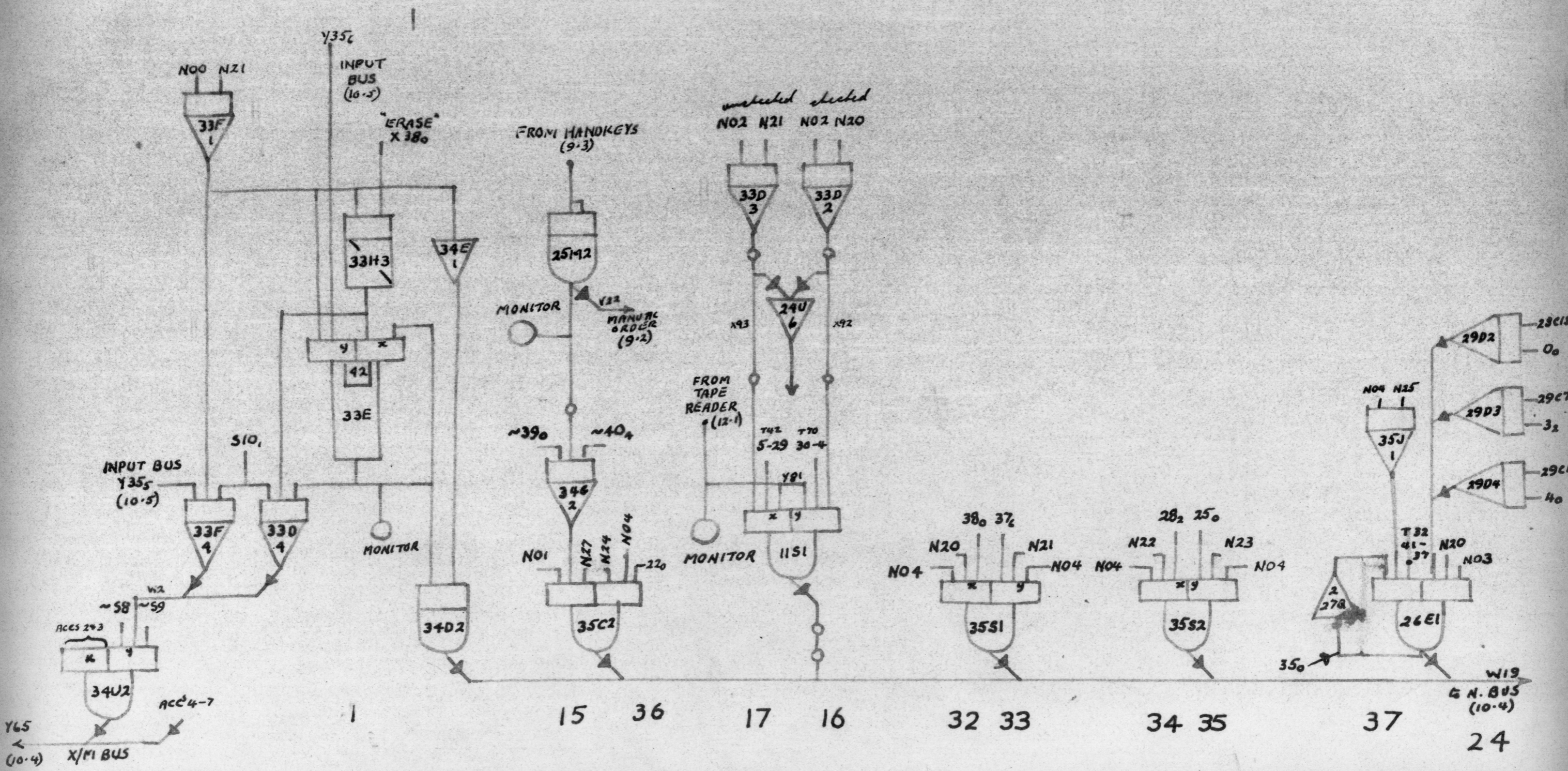


FIG 10.3 ACCUMULATOR 1 AND SPECIAL REGISTERS

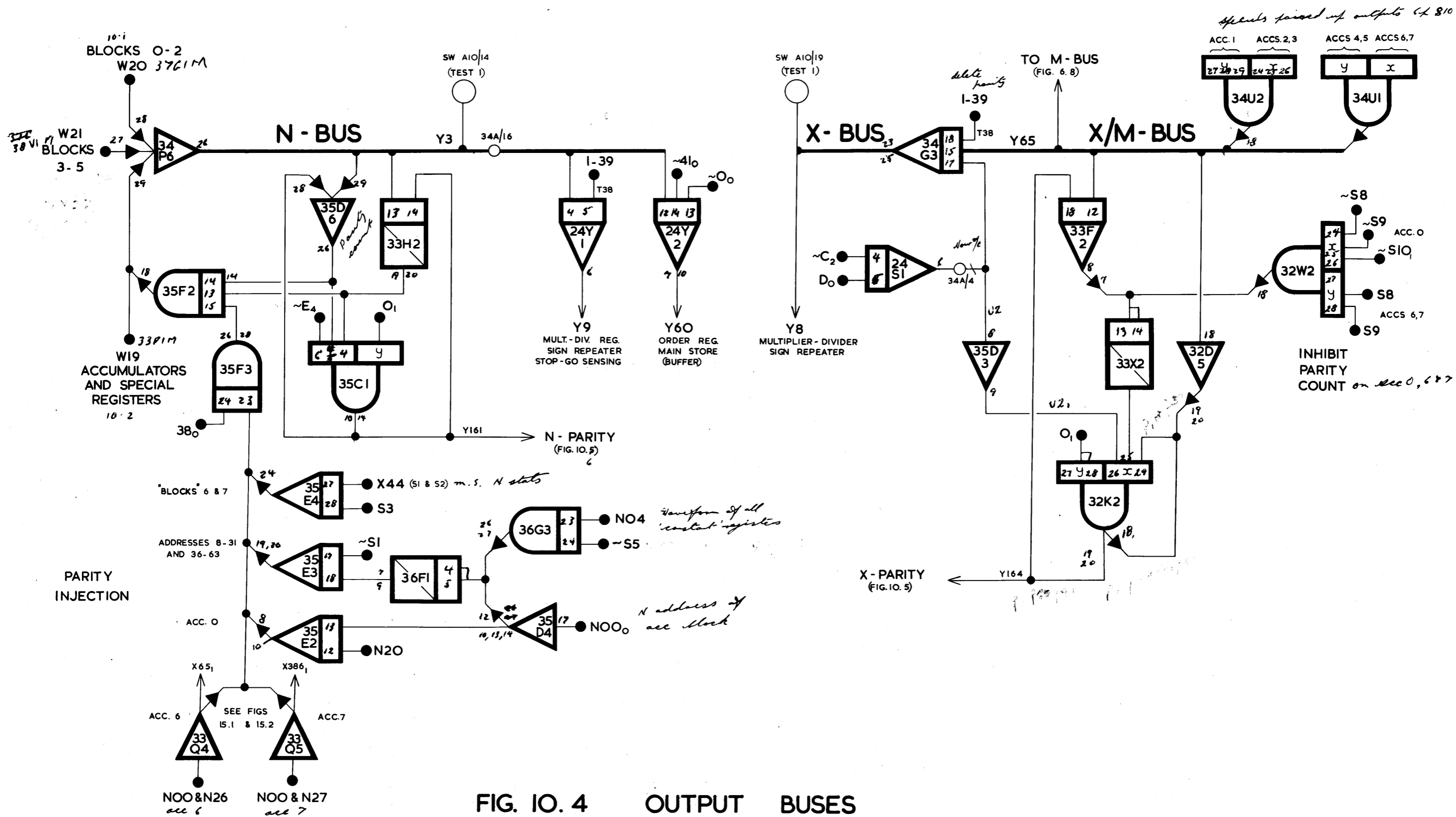


FIG. 10.4 OUTPUT BUSES

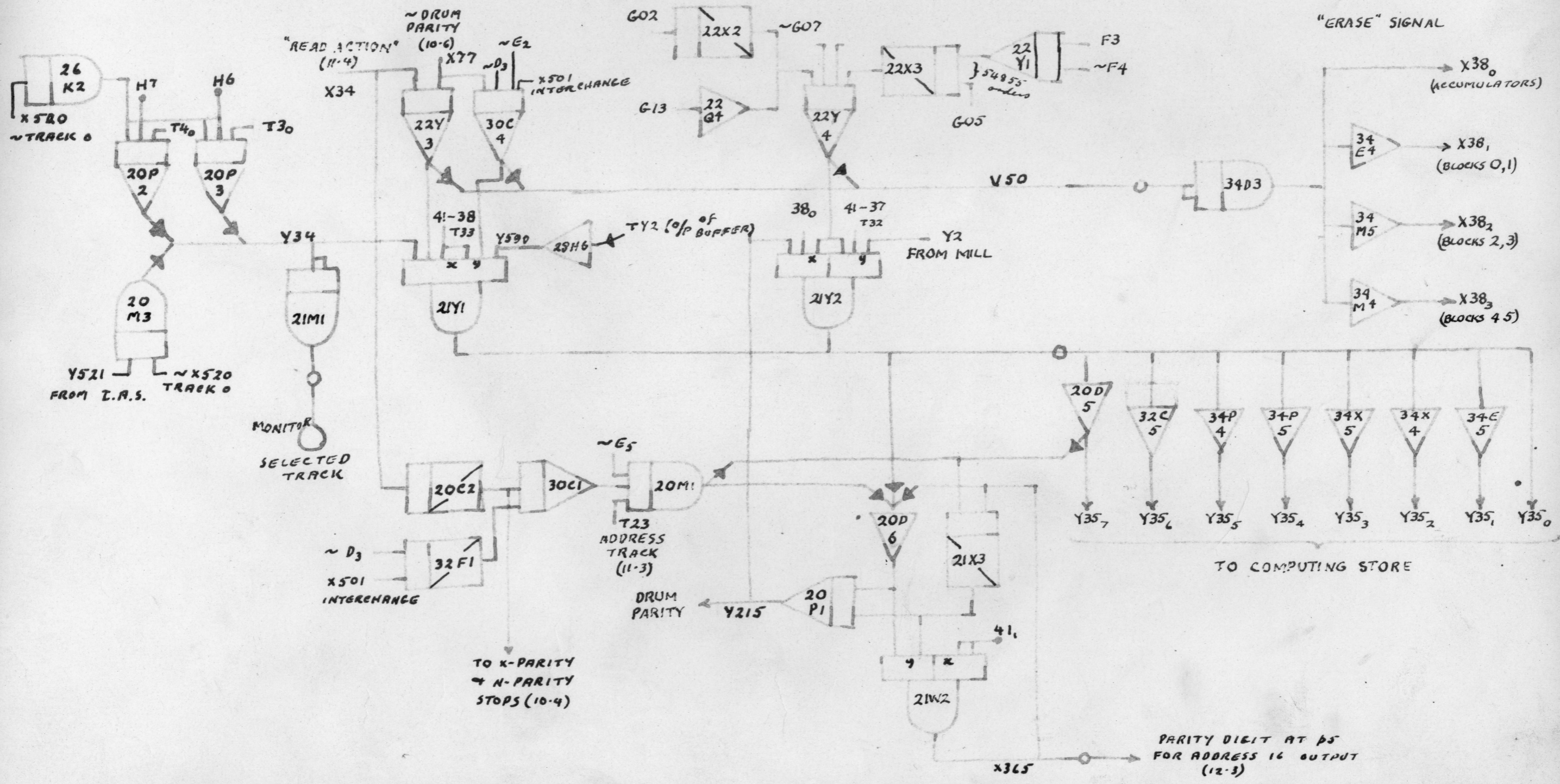


FIG 10.5 INPUT BUS

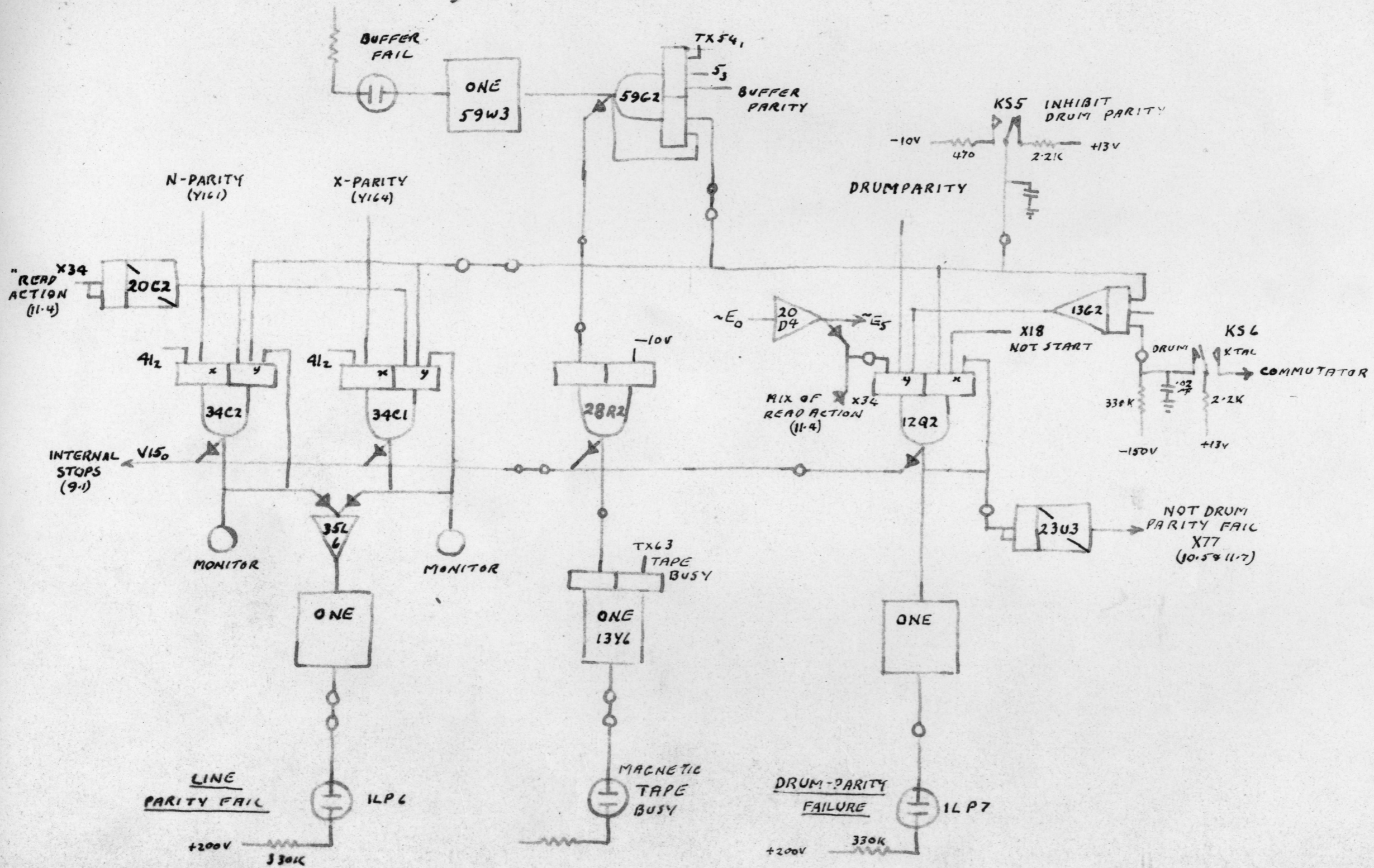


FIG. 10.6 PARITY STOPS

| Address | Gating Waveforms | Package References | | |
|---------|-----------------------|--------------------|-----------------|--------------|
| | | AND Gate | Line & Inverter | Output Delay |
| 0.0. | N10 ₀ ,N20 | 38D4 | 39C | 38C2 |
| 0.1. | N10 ₀ ,N21 | 38D3 | 39D | " |
| 0.2. | N10 ₀ ,N22 | 38D2 | 37C | 38C1 |
| 0.3. | N10 ₀ ,N23 | 38D1 | 37D | " |
| 0.4. | N10 ₁ ,N24 | 37H4 | 37E | 37G2 |
| 0.5. | N10 ₁ ,N25 | 37H3 | 37F | " |
| 0.6. | N10 ₁ ,N26 | 37H2 | 37J | 37G1 |
| 0.7. | N10 ₁ ,N27 | 37H1 | 37K | " |
| 1.0. | N11 ₀ ,N20 | 38H4 | 38E | 38G2 |
| 1.1. | N11 ₀ ,N21 | 38H3 | 38F | " |
| 1.2. | N11 ₀ ,N22 | 38H2 | 38J | 38G1 |
| 1.3. | N11 ₀ ,N23 | 38H1 | 38K | " |
| 1.4. | N11 ₁ ,N24 | 39H4 | 39E | 39G2 |
| 1.5. | N11 ₁ ,N25 | 39H3 | 39F | " |
| 1.6. | N11 ₁ ,N26 | 39H2 | 39J | 39G1 |
| 1.7. | N11 ₁ ,N27 | 39H1 | 39K | " |
| 2.0. | N12 ₀ ,N20 | 39Q4 | 39L | 39P2 |
| 2.1. | N12 ₀ ,N21 | 39Q3 | 39M | " |
| 2.2. | N12 ₀ ,N22 | 39Q2 | 39R | 39P1 |
| 2.3. | N12 ₀ ,N23 | 39Q1 | 39S | " |
| 2.4. | N12 ₁ ,N24 | 39W4 | 39T | 39V2 |
| 2.5. | N12 ₁ ,N25 | 39W3 | 39U | " |
| 2.6. | N12 ₁ ,N26 | 39W2 | 39X | 39V1 |
| 2.7. | N12 ₁ ,N27 | 39W1 | 39Y | " |
| 3.0. | N13 ₀ ,N20 | 38Q4 | 38L | 38P2 |
| 3.1. | N13 ₀ ,N21 | 38Q3 | 38M | " |
| 3.2. | N13 ₀ ,N22 | 38Q2 | 38R | 38P1 |
| 3.3. | N13 ₀ ,N23 | 38Q1 | 38S | " |
| 3.4. | N13 ₁ ,N24 | 38W4 | 38T | 38V2 |
| 3.5. | N13 ₁ ,N25 | 38W3 | 38U | " |
| 3.6. | N13 ₁ ,N26 | 38W2 | 38X | 38V1 |
| 3.7. | N13 ₁ ,N27 | 38W1 | 38Y | " |

ORDINARY REGISTERS

| ADDRESS CODING FOR COMPUTING STORE | | | | |
|------------------------------------|--|----------------|---------|--------------------------------|
| N0x | Accumulators and Special Register Blocks | | | |
| N1y | Ordinary Register Blocks | | | |
| N2z | Position Within Block | | | |
| Examples: | | | | |
| Decoding | Octal Number | Decimal Number | Address | Type |
| N13 N25 | 135 | 93 | 3.5 | Ordinary Register |
| N00 N21 | 01 | 1 | 1 | Accumulator |
| N01 N27 | 17 | 15 | 15 | Special Reg. Handkeys |
| N02 N21 | 21 | 17 | 17 | Unchecked Input or Output |
| N04 N22 | 42 | 34 | 34 | Constant (= 2 ⁻¹⁰) |

| Address | Gating Waveforms | Package References | | |
|---------|------------------|--------------------|-----------------|--------------|
| | | AND Gate | Line & Inverter | Output Delay |
| 4.0. | N14,N20 | 37Q4 | 37L | 37P2 |
| 4.1. | N14,N21 | 37Q3 | 37M | " |
| 4.2. | N14,N22 | 37Q2 | 37R | 37P1 |
| 4.3. | N14,N23 | 37Q1 | 37S | " |
| 4.4. | N14,N24 | 37W4 | 37T | 37V2 |
| 4.5. | N14,N25 | 37W3 | 37U | " |
| 4.6. | N14,N26 | 37W2 | 37X | 37V1 |
| 4.7. | N14,N27 | 37W1 | 37Y | " |
| 5.0. | N15,N20 | 36Q4 | 36L | 36P2 |
| 5.1. | N15,N21 | 36Q3 | 36M | " |
| 5.2. | N15,N22 | 36Q2 | 36R | 36P1 |
| 5.3. | N15,N23 | 36Q1 | 36S | " |
| 5.4. | N15,N24 | 36W4 | 36T | 36V2 |
| 5.5. | N15,N25 | 36W3 | 36U | " |
| 5.6. | N15,N26 | 36W2 | 36X | 36V1 |
| 5.7. | N15,N27 | 36W1 | 36Y | " |

| ADDRESS DECODING | | |
|------------------|-------------------|-------------------|
| Repeater | Input | Output |
| 35Y3 | N10 ₀ | N10 ₁ |
| 35Y4 | N11 ₀ | N11 ₁ |
| 35Y5 | N12 ₀ | N12 ₁ |
| 35Y1 | N13 ₀ | N13 ₁ |
| 34X6 | S10 ₀ | S10 ₁ |
| 34E3 | ~S10 ₀ | ~S10 ₁ |

| INPUT BUS | | |
|--------------------|------------------|---|
| Repeater | Output | Destinations |
| - | Y35 ₀ | Parity circuit and all repeaters |
| 34E5 | Y35 ₁ | Block 1 and first half of block 0 |
| 34X4 | Y35 ₂ | Block 2 and second half of block 3 |
| 34X5 | Y35 ₃ | Block 5 and second half of block 4 |
| 34P5 | Y35 ₄ | First half of blocks 3 and 4. Second half of block 0 |
| 34P4 | Y35 ₅ | All accumulators (modifier by-pass) |
| 33F3 (AND gate) | Y35 ₆ | All accumulators (normal input) |
| 20D5 | Y35 ₇ | Output (punch) circuit ('Mlx' output to parity circuit) |

REPEATERS

FIG. IO. 7 TABULATED DETAILS

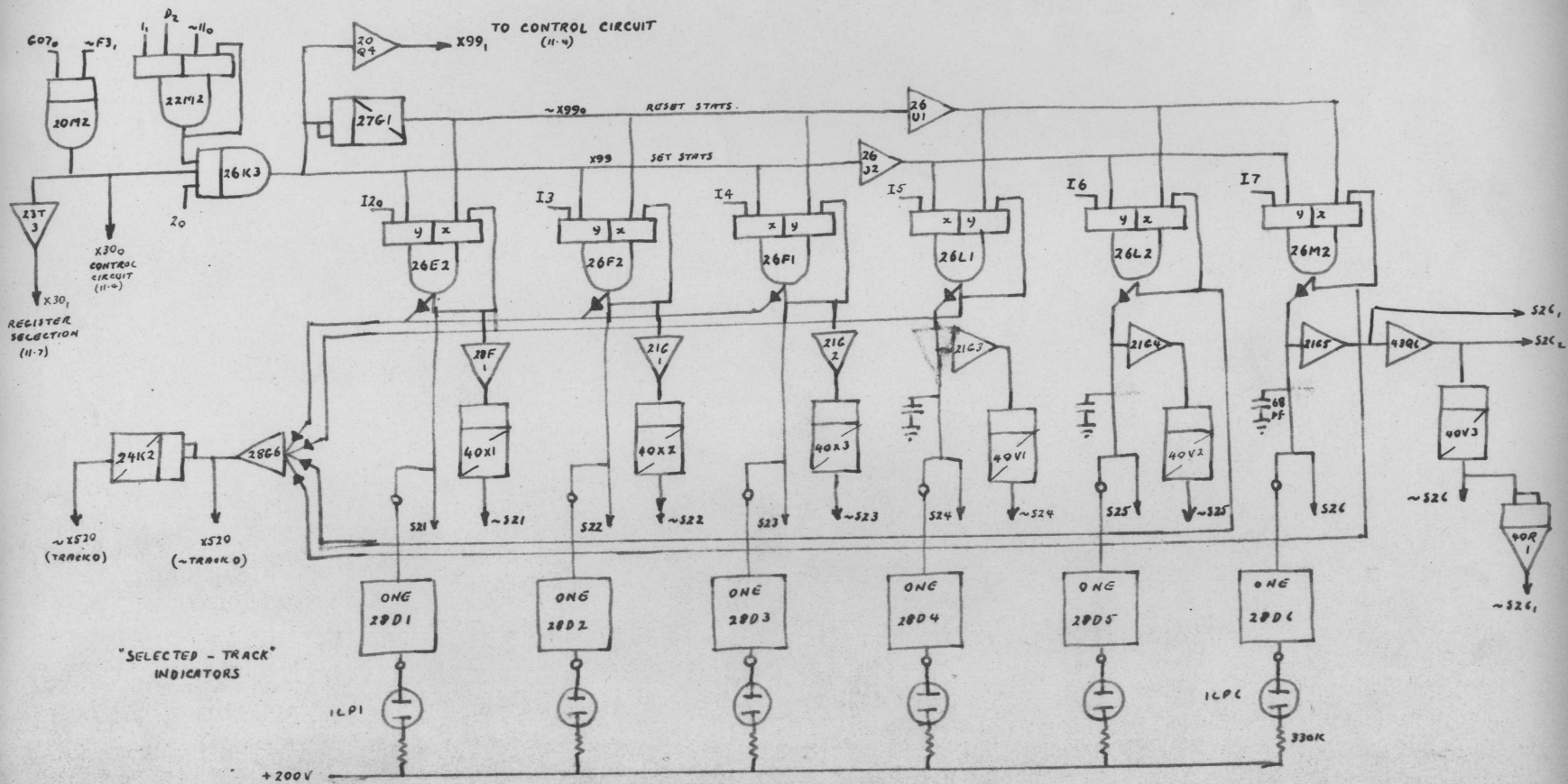
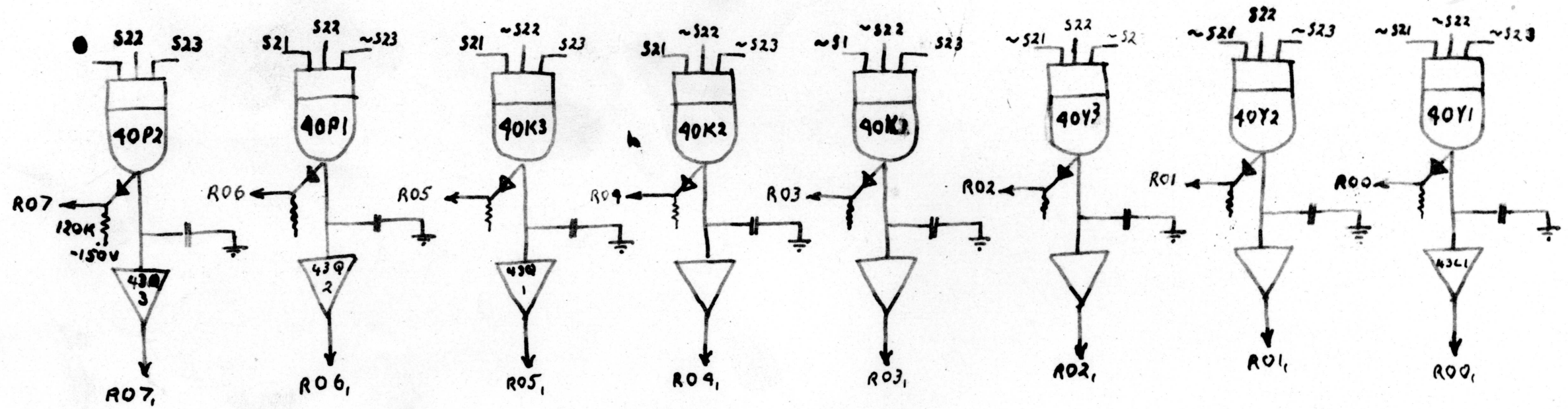


FIG. 11. I TRACK - SELECTION DECODING

COLUMN-SELECTION WAVEFORMS



ROW-SELECTION WAVEFORMS

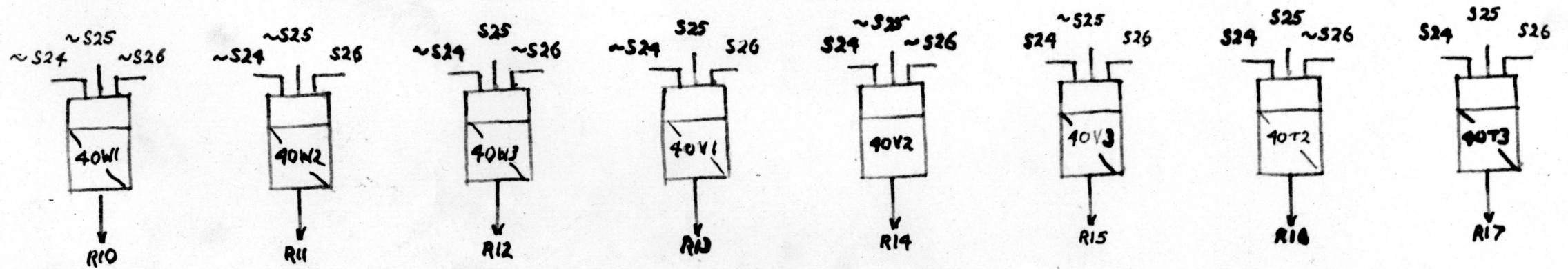


FIG. II.2

TRACK-SELECTION CONTROLS

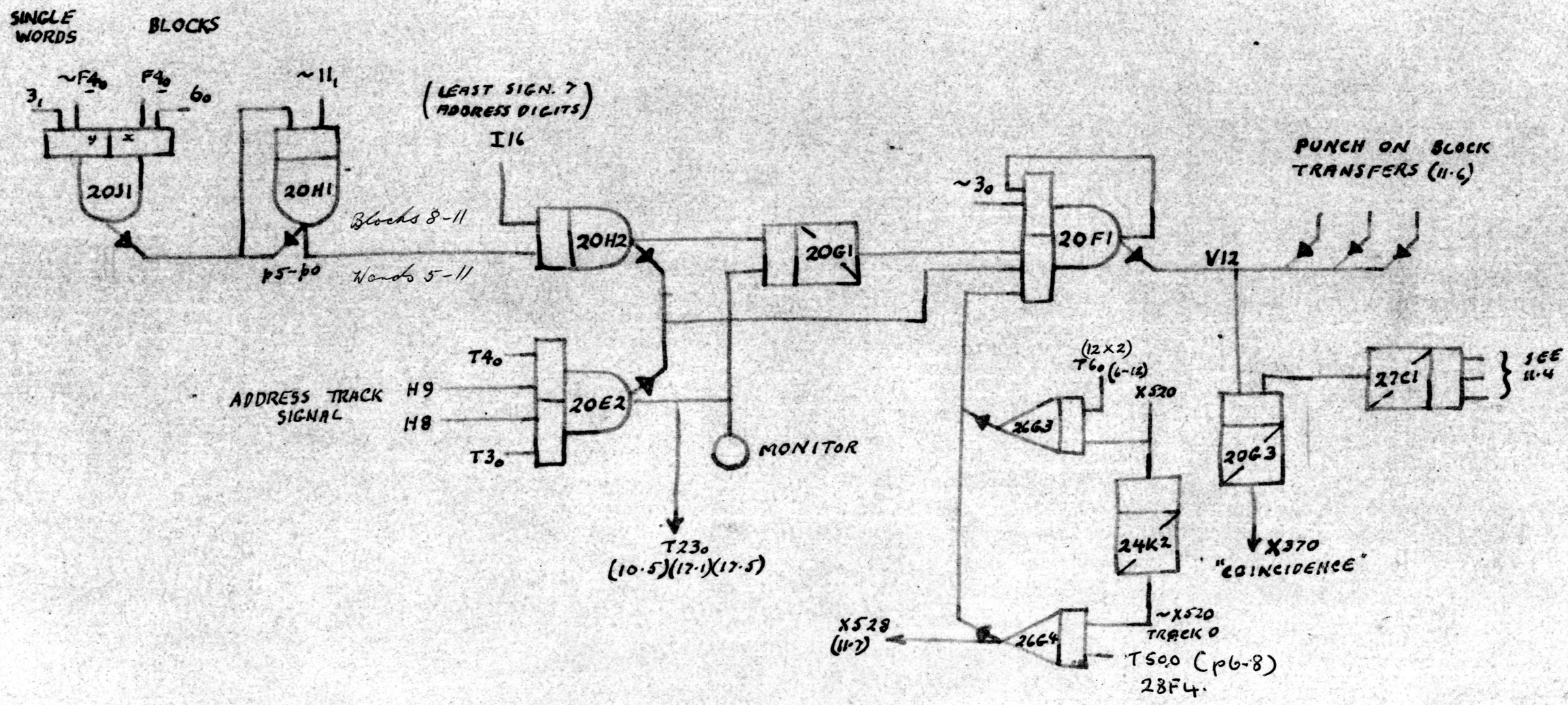


FIG. 11.3 COINCIDENCE CIRCUIT

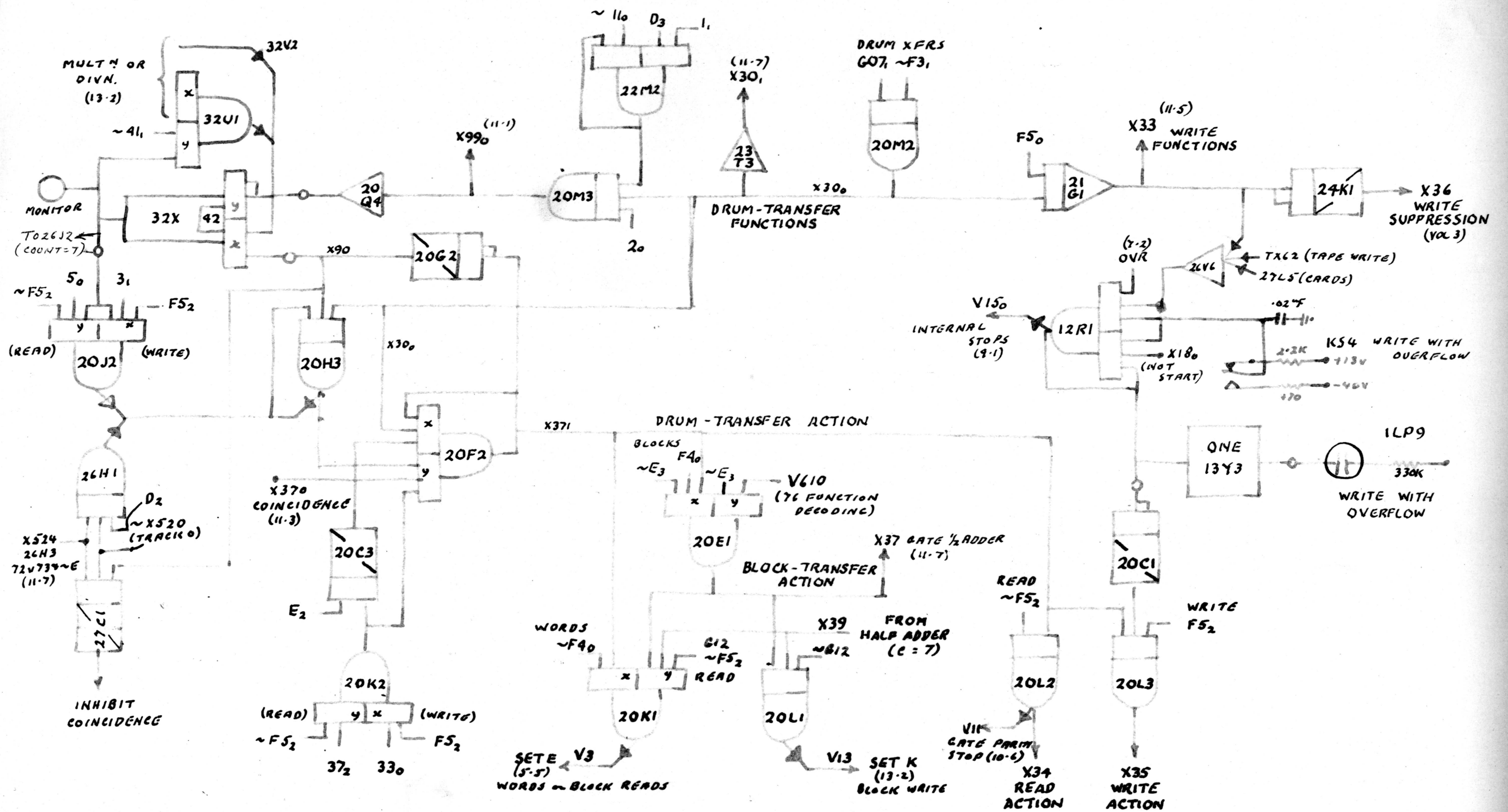


FIG 11.4 CONTROL CIRCUIT FOR DRUM TRANSFERS

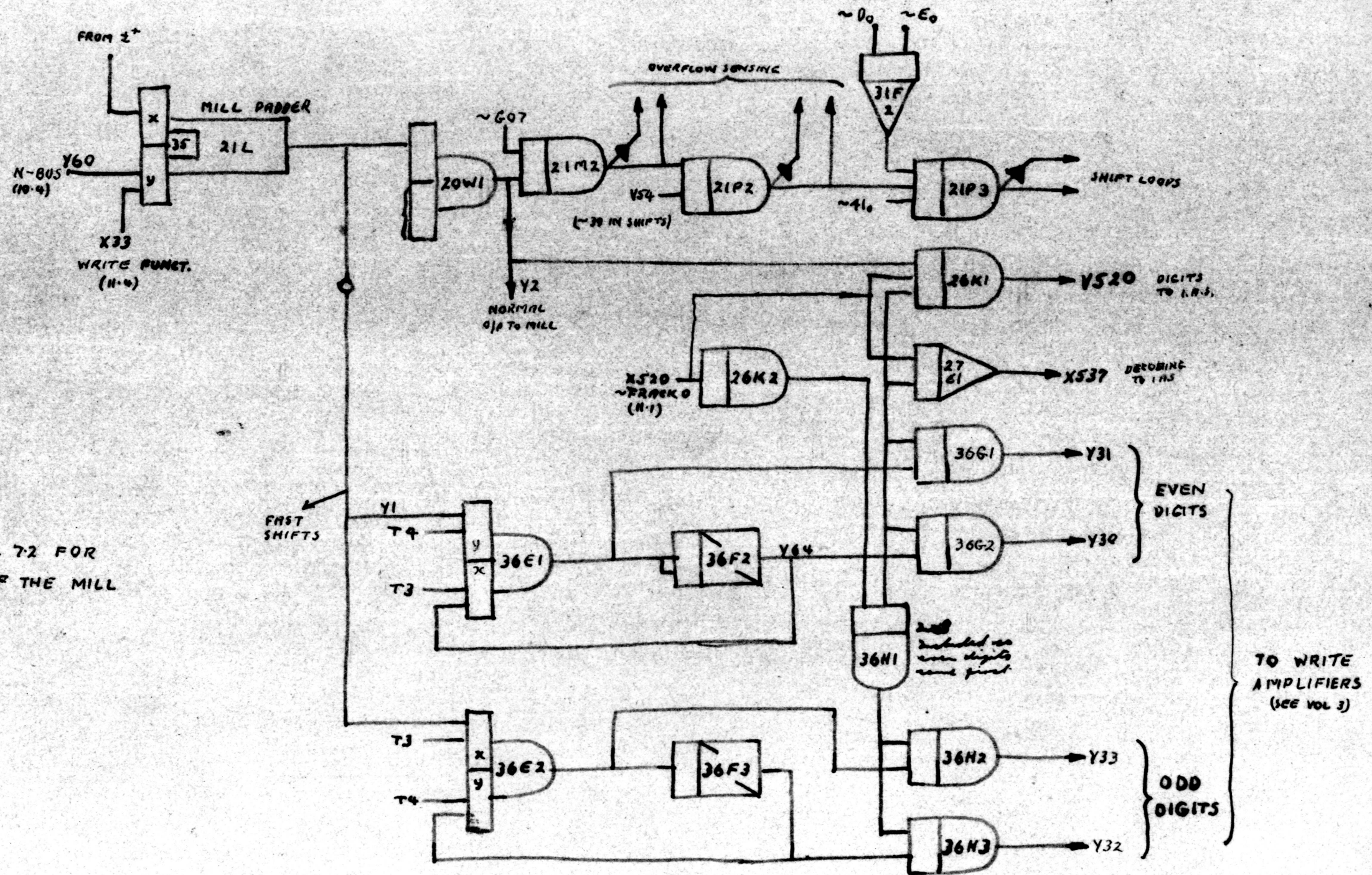


FIG. 11.5

ROUTING IN DRUM-WRITE ORDERS

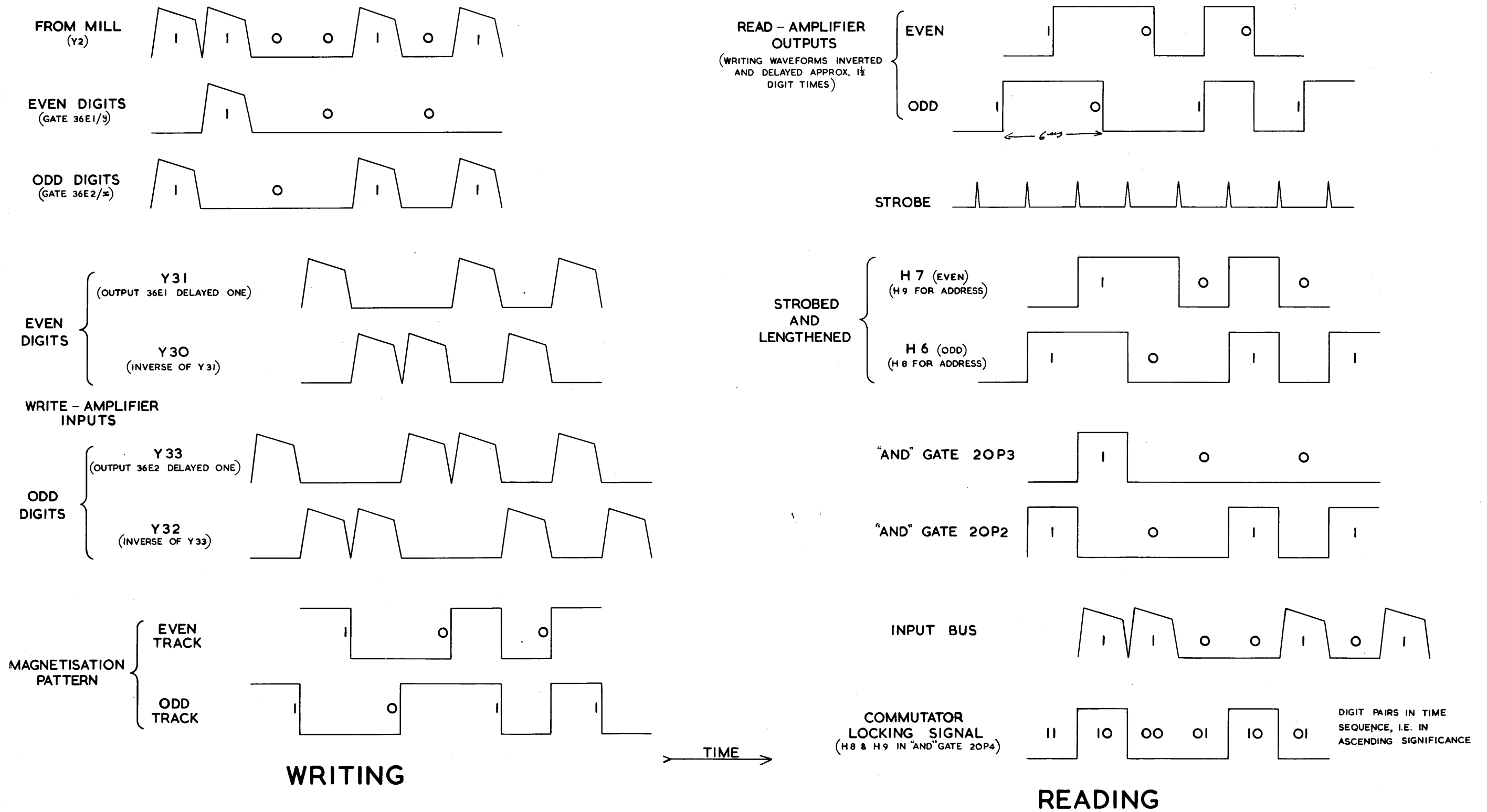


FIG. II. 6 IDEALISED WAVEFORMS

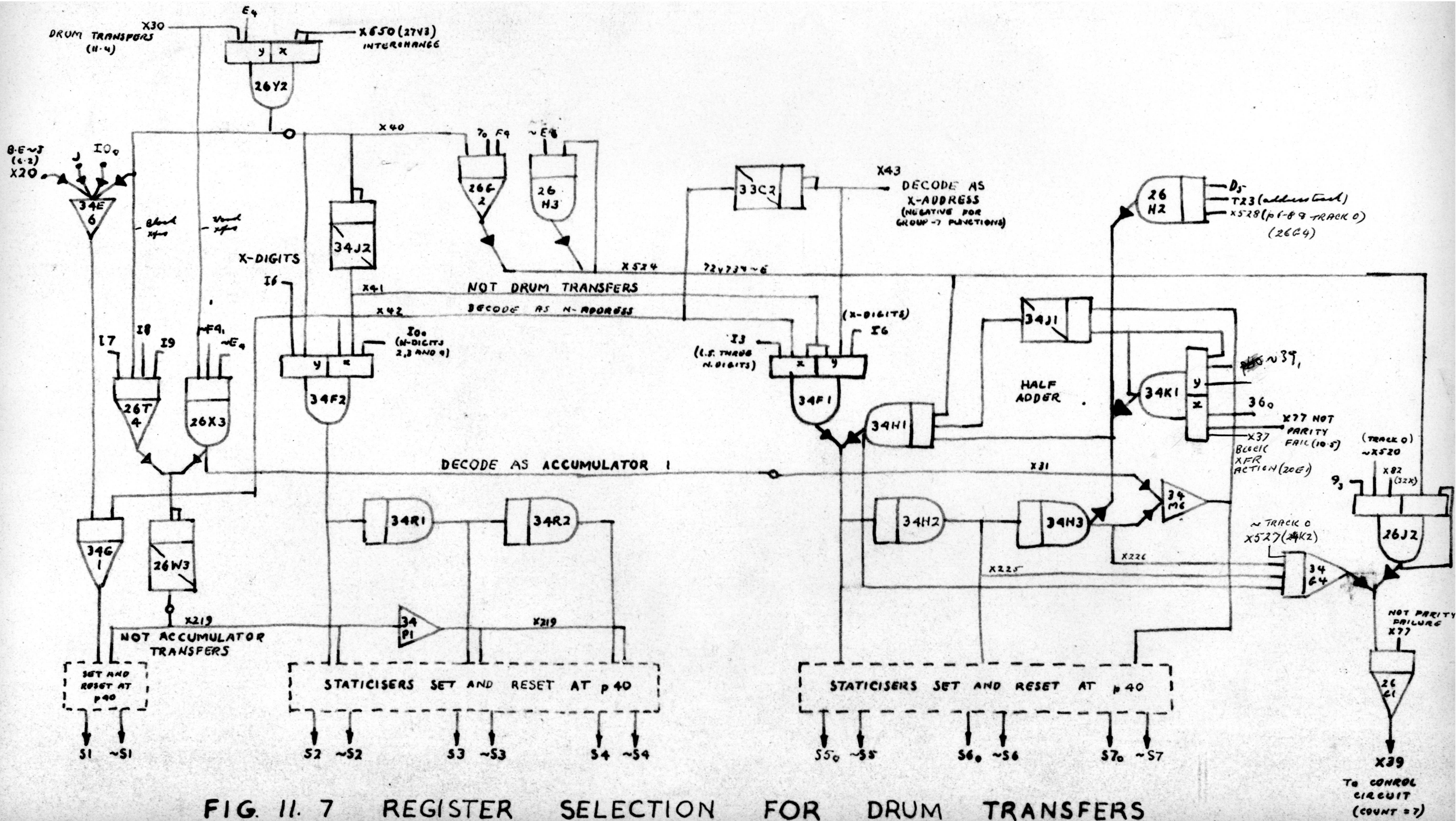


FIG. 11. 7 REGISTER SELECTION FOR DRUM TRANSFERS

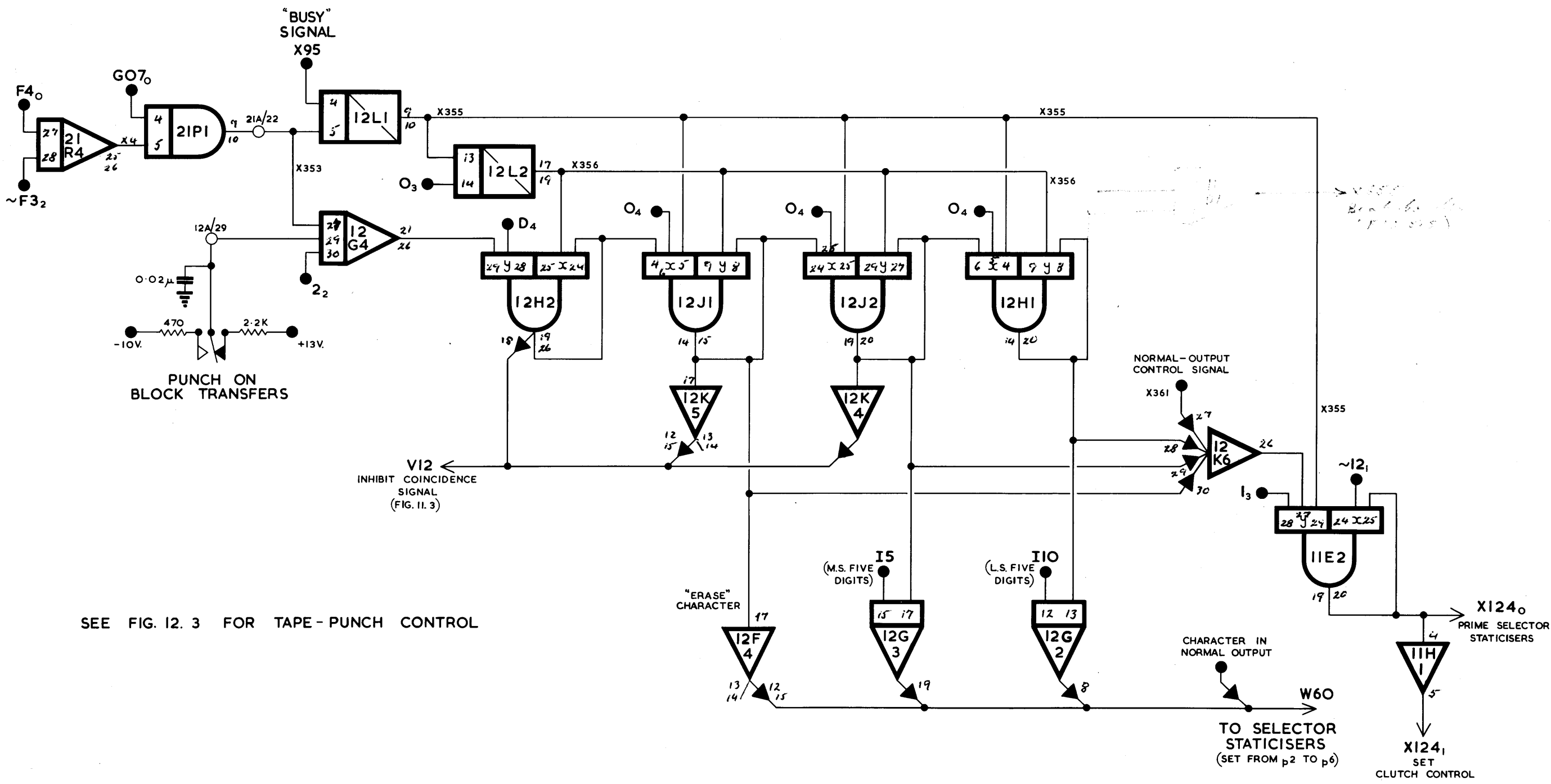


FIG. 11.8 CONTROL FOR BLOCK-ADDRESS PUNCHING

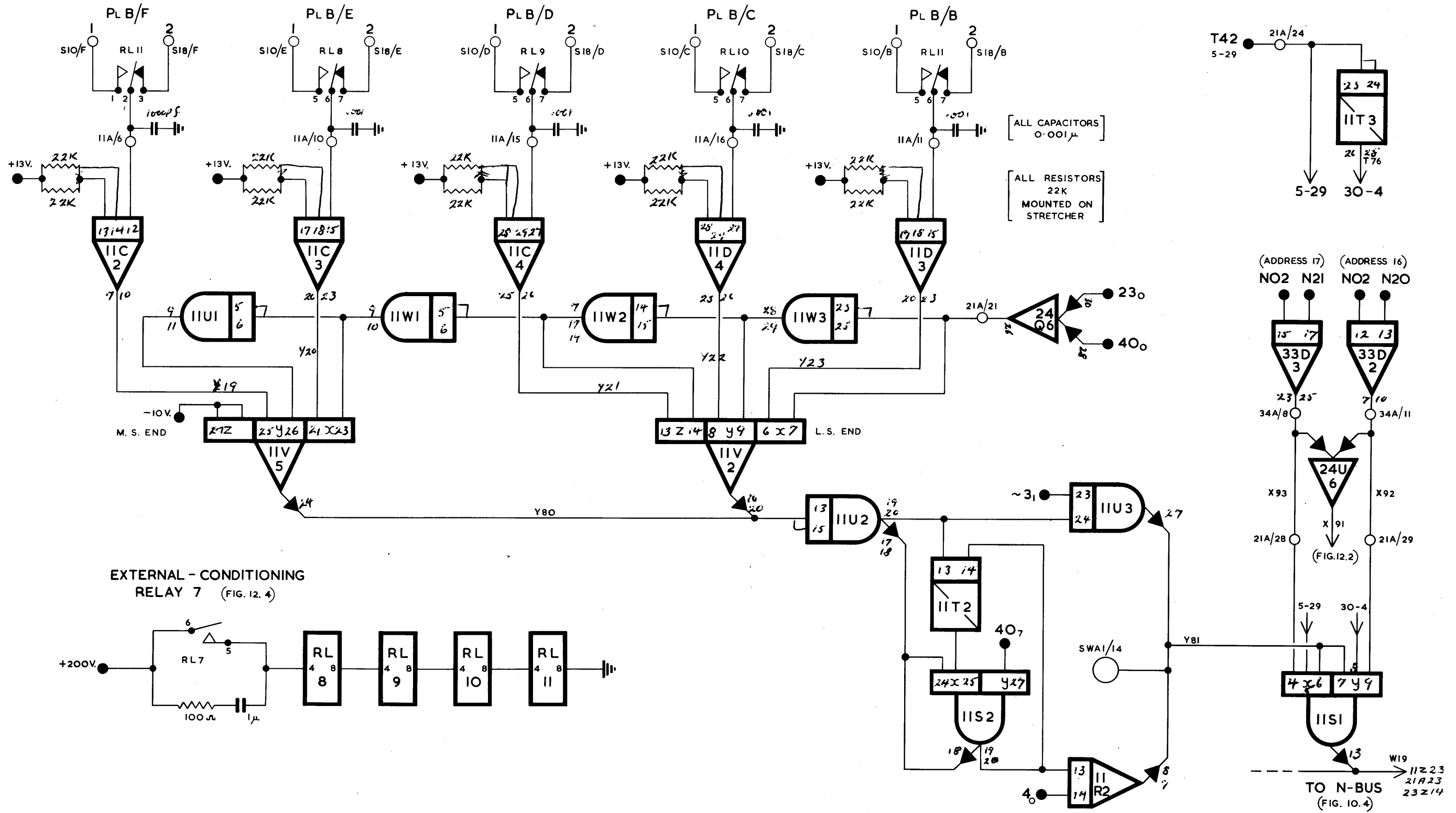
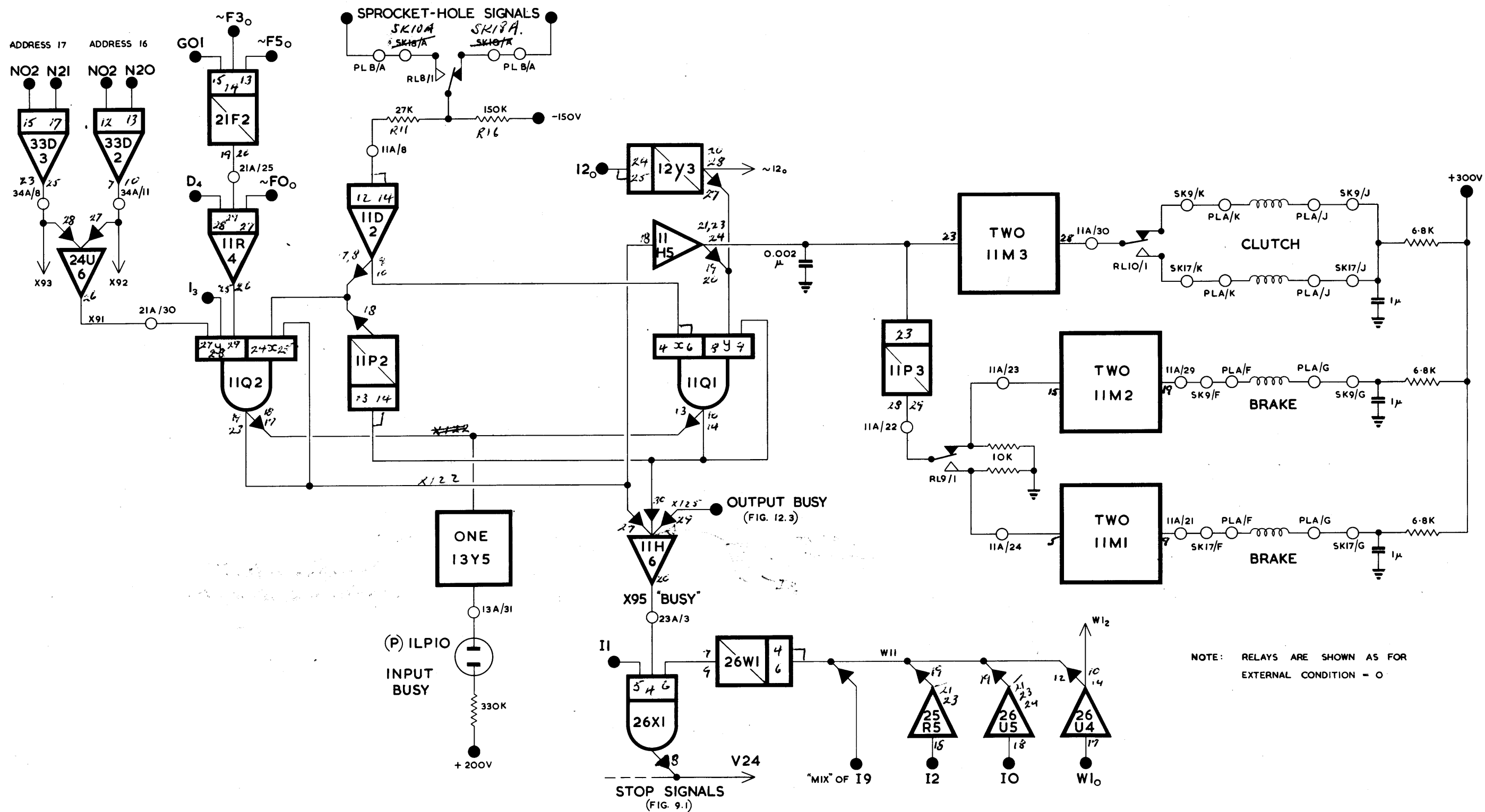


FIG. 12.1 INPUT FROM TAPE READERS



NOTE: RELAYS ARE SHOWN AS FOR EXTERNAL CONDITION - O

FIG. 12. 2 INPUT TAPE - DRIVE CONTROL

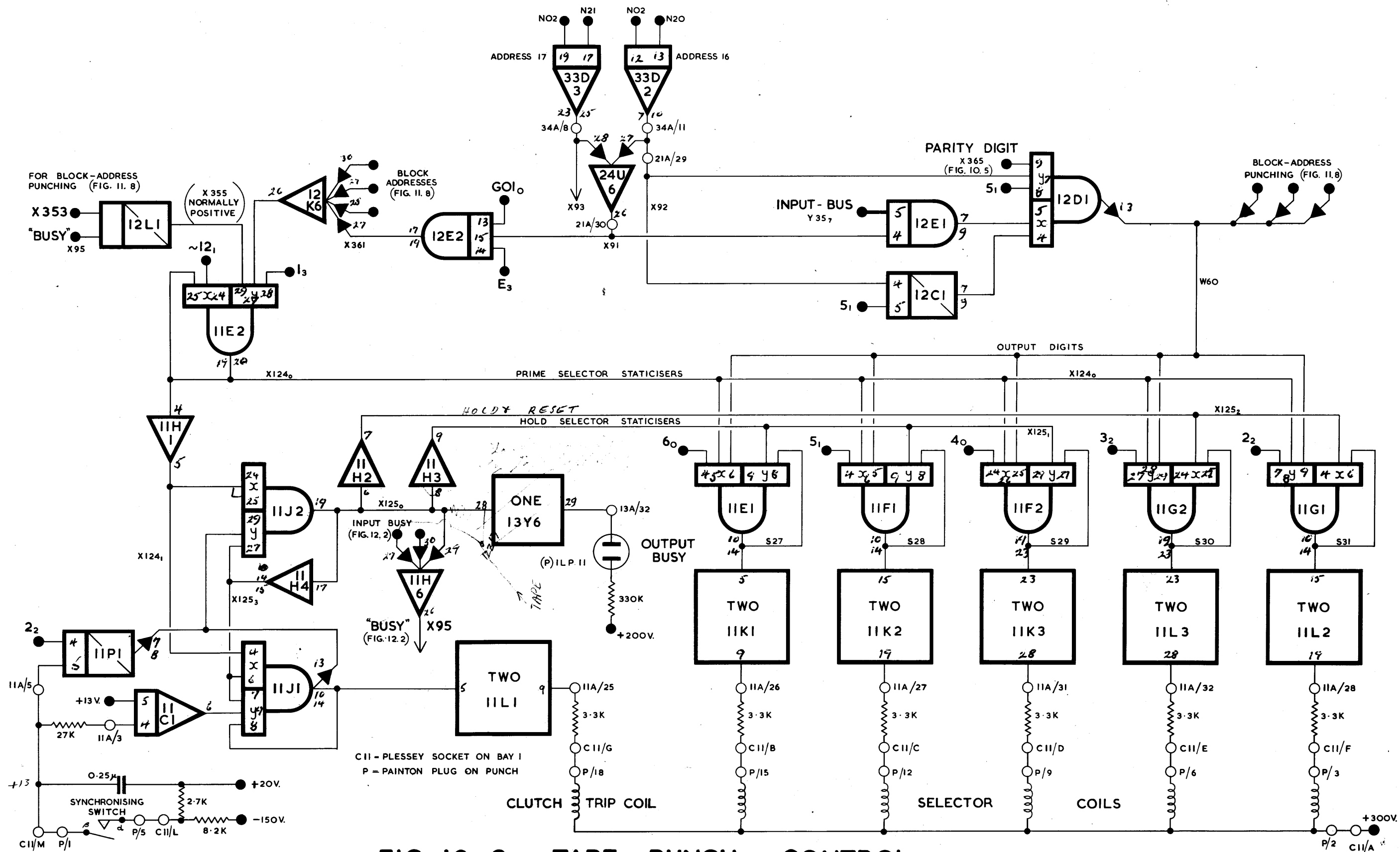


FIG. 12. 3 TAPE - PUNCH CONTROL

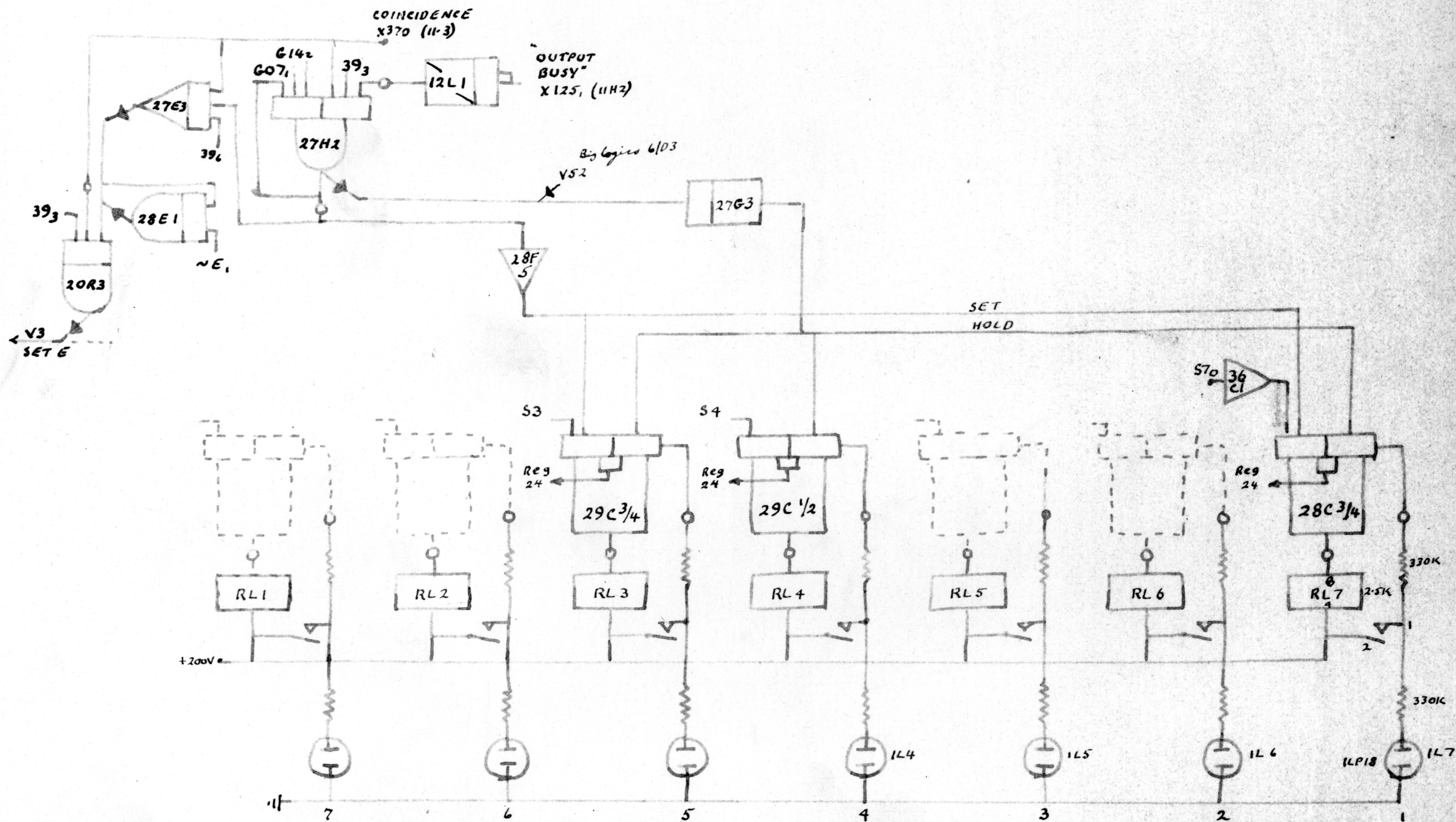
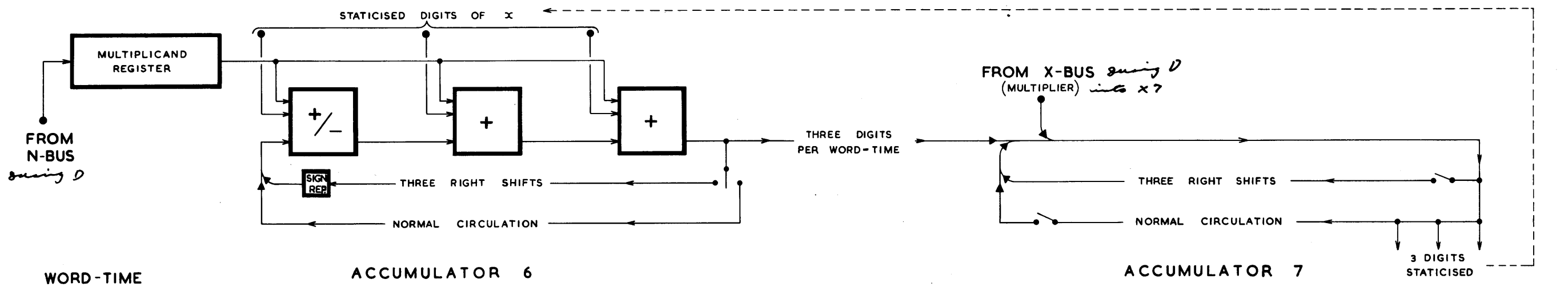


FIG 12. 4 EXTERNAL - CONDITIONING CIRCUITS



WORD-TIME

ACCUMULATOR 6

ACCUMULATOR 7

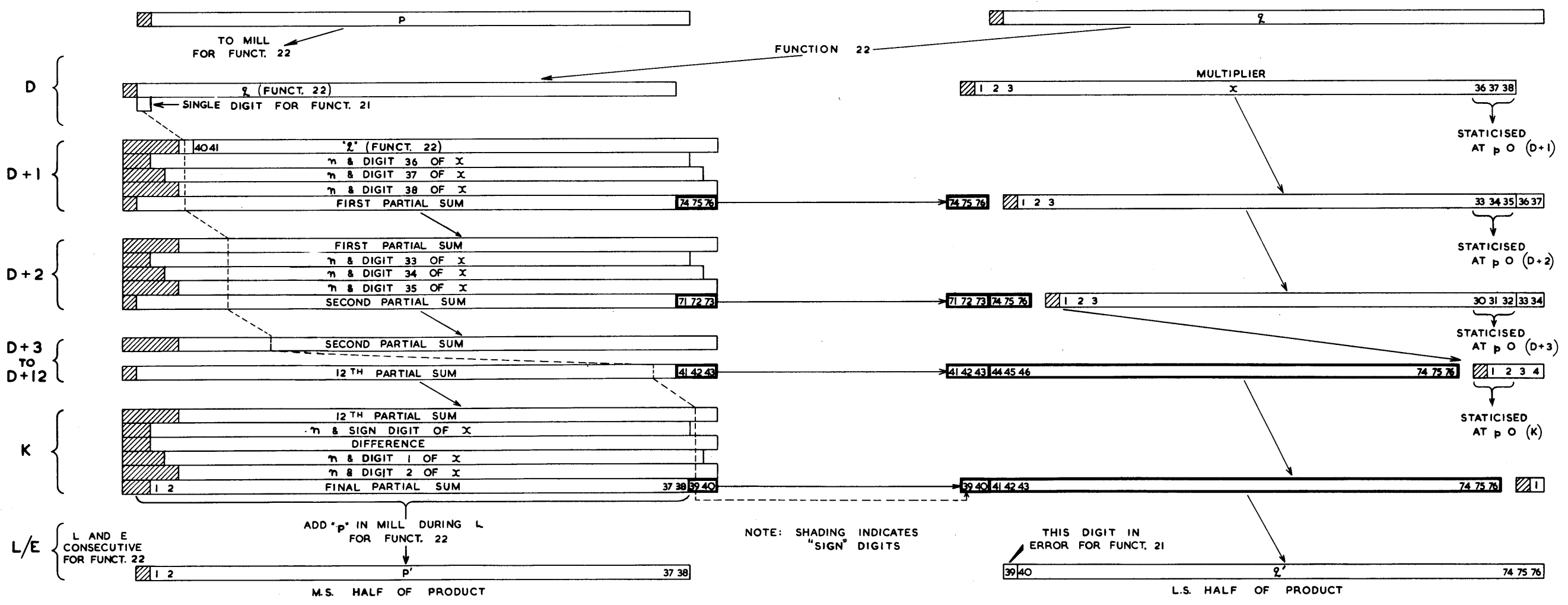


FIG. 13. I. MULTIPLICATION (SCHEMATIC)

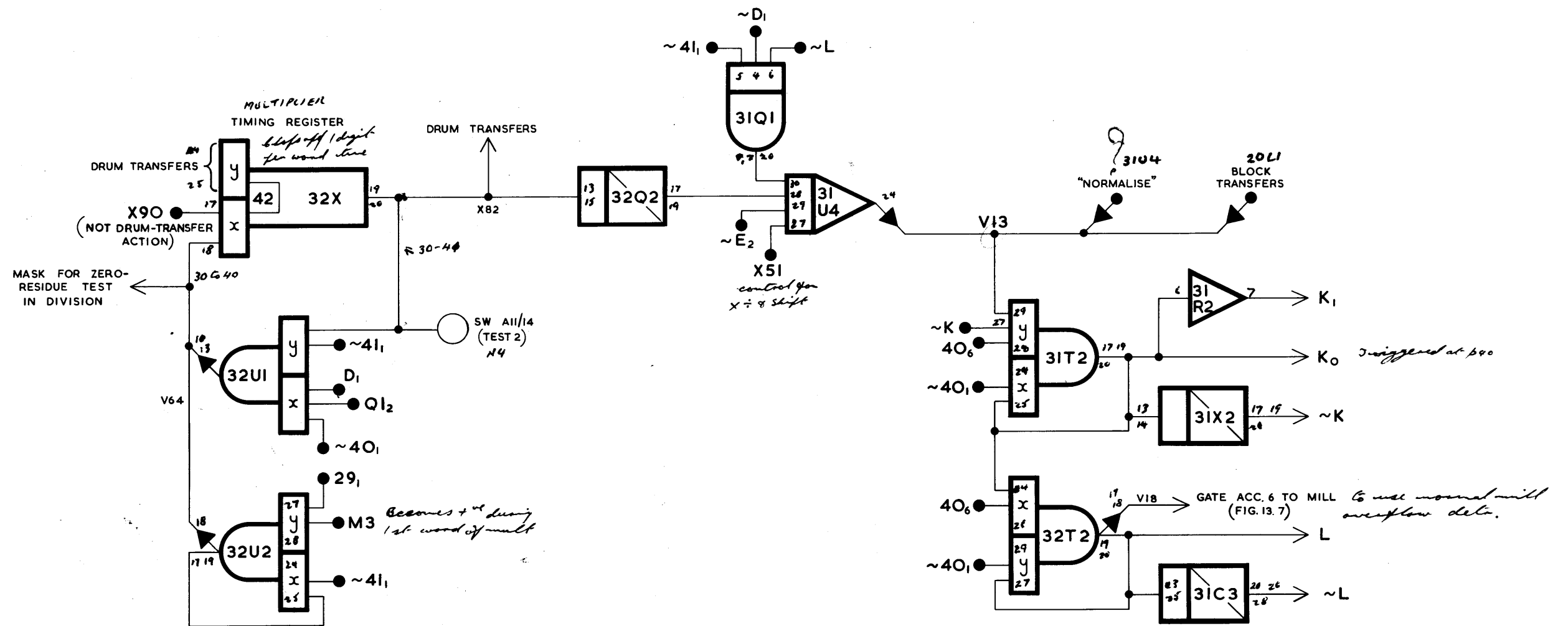


FIG. 13. 2 TIMING CONTROL FOR MULTIPLIER - DIVIDER

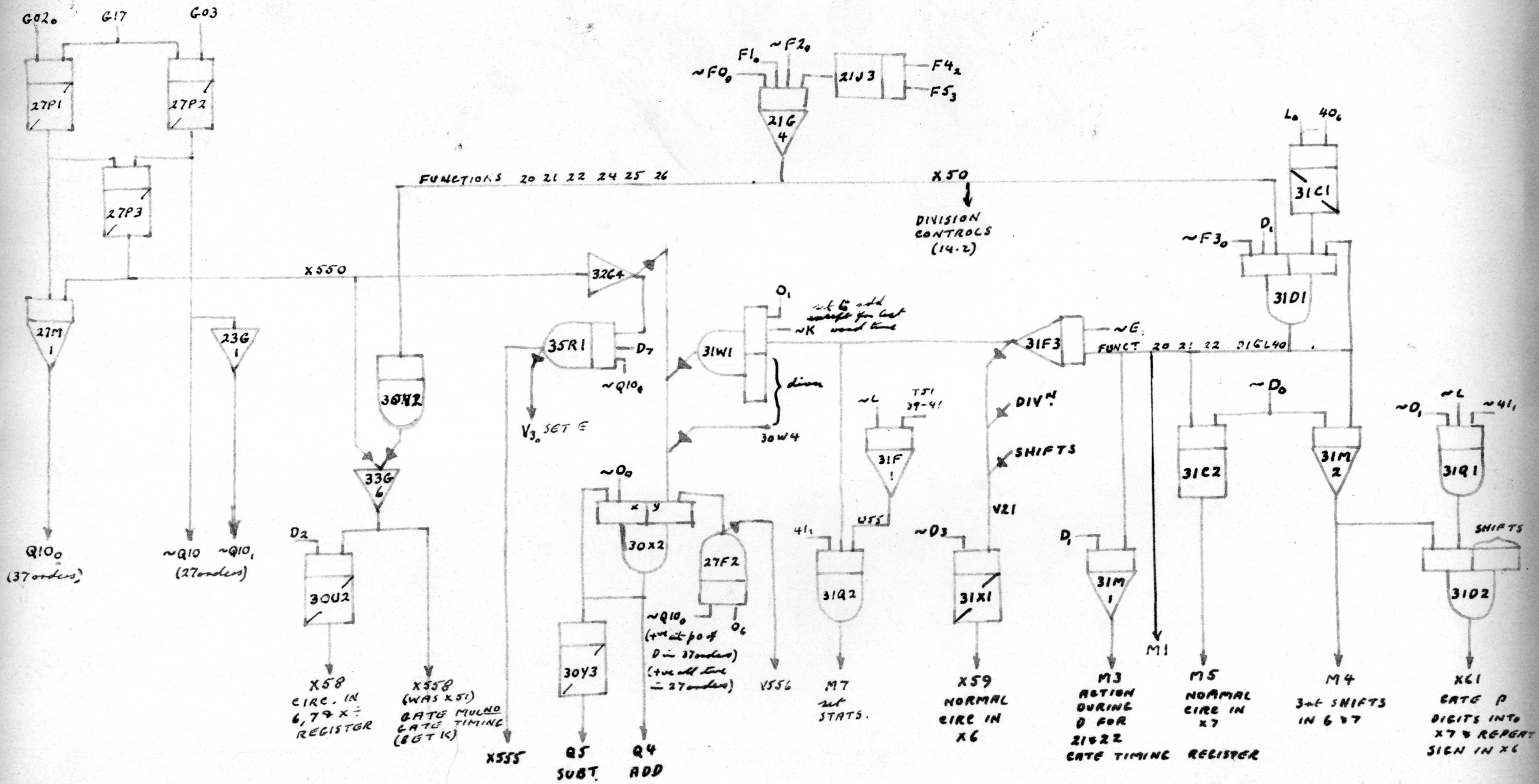


FIG 13.3 CONTROLS FOR MULTIPLICATION

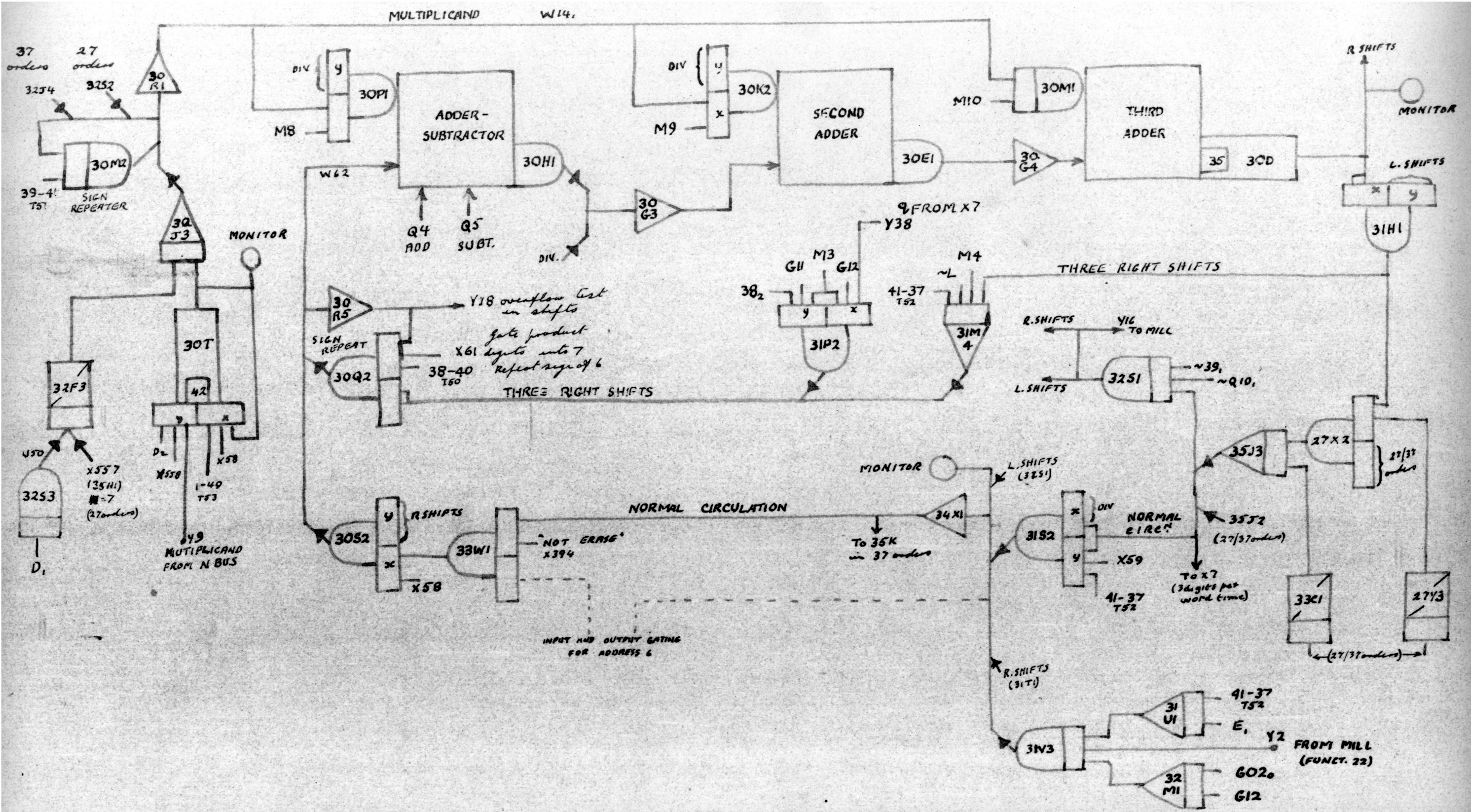


FIG. 13.4

ACCUMULATOR 6 IN MULTIPLICATION.

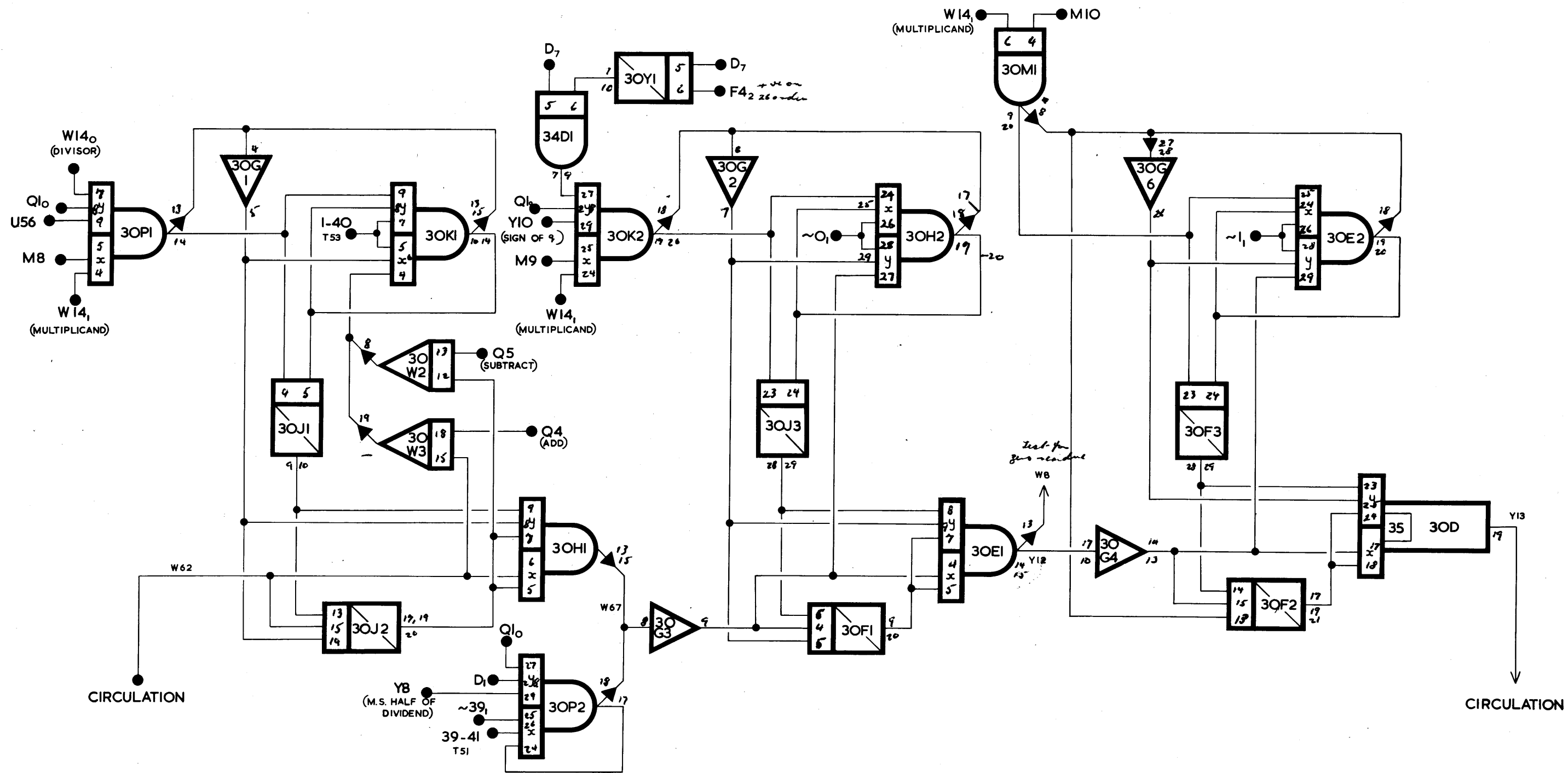


FIG. 13 .5 ADDER - SUBTRACTOR AND ADDERS IN ACCUMULATOR 6.

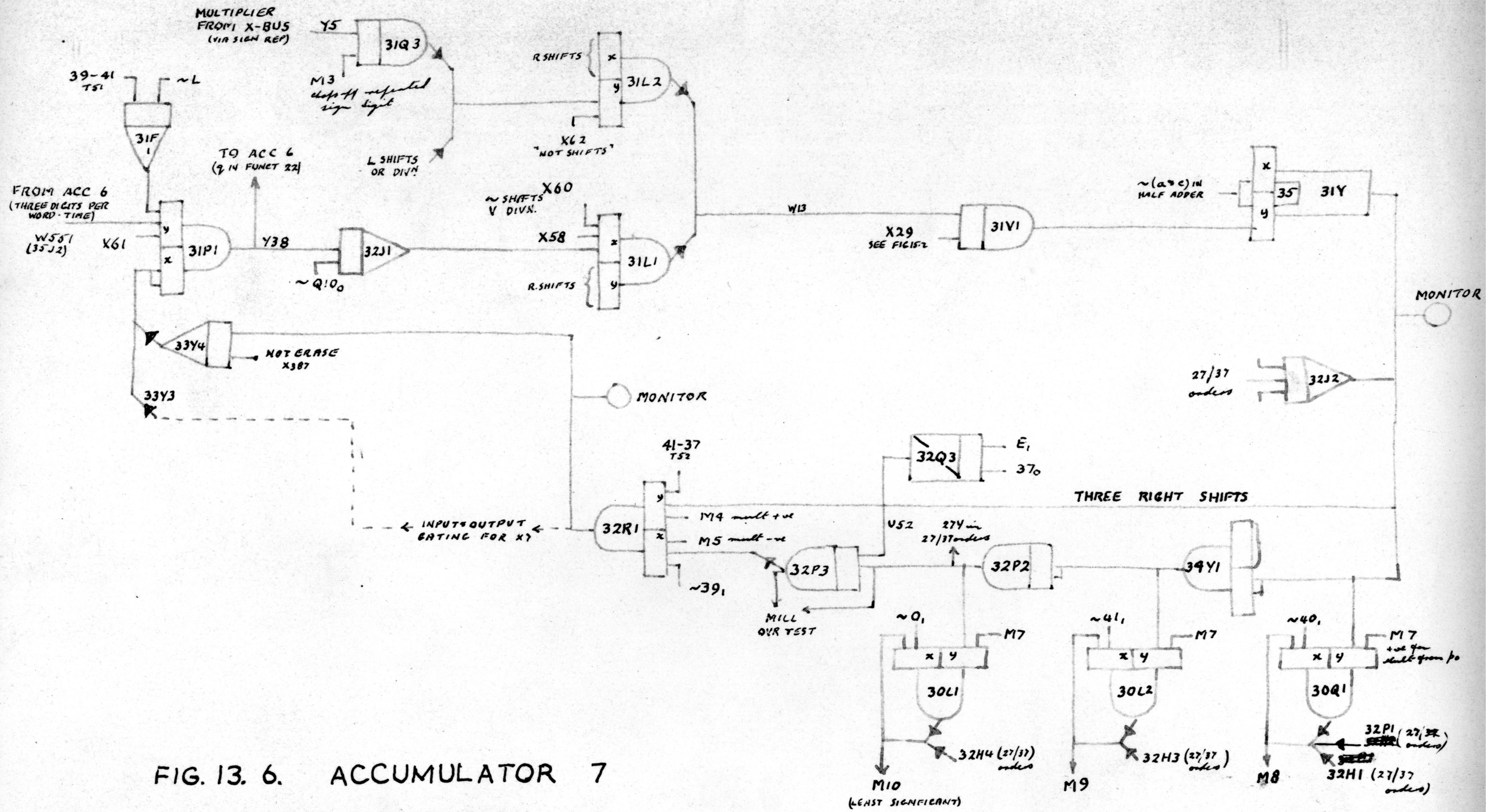


FIG. 13. 6. ACCUMULATOR 7
IN MULTIPLICATION

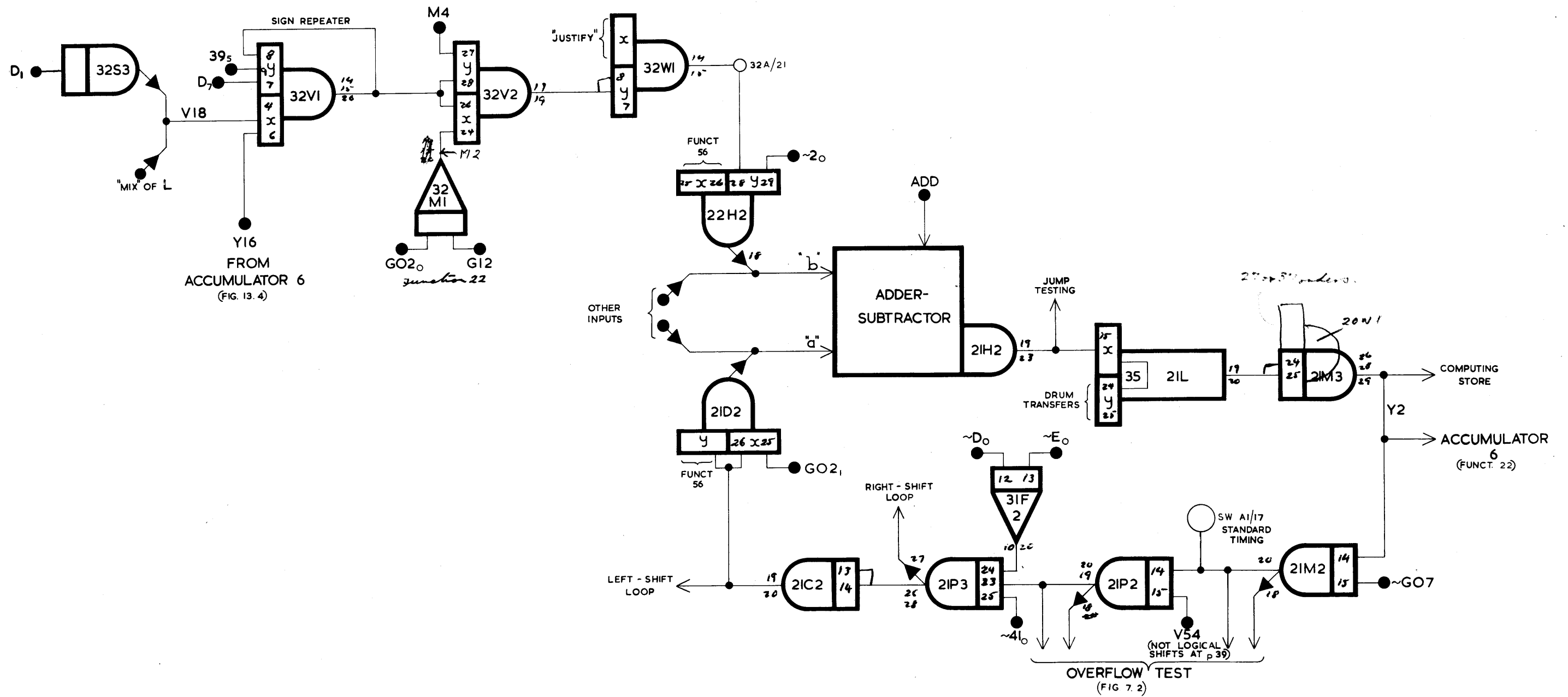
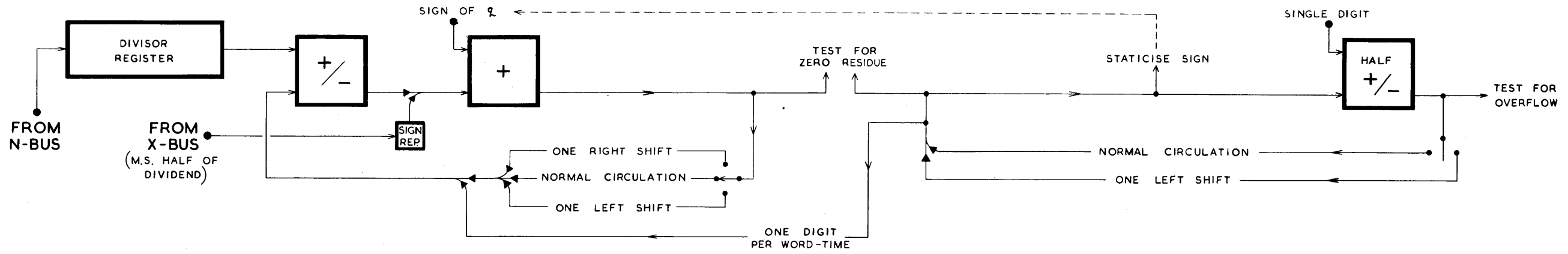


FIG. 13.7 MILL CONNECTIONS FOR MULTIPLICATION



WORD - TIME

ACCUMULATOR 6

ACCUMULATOR 7

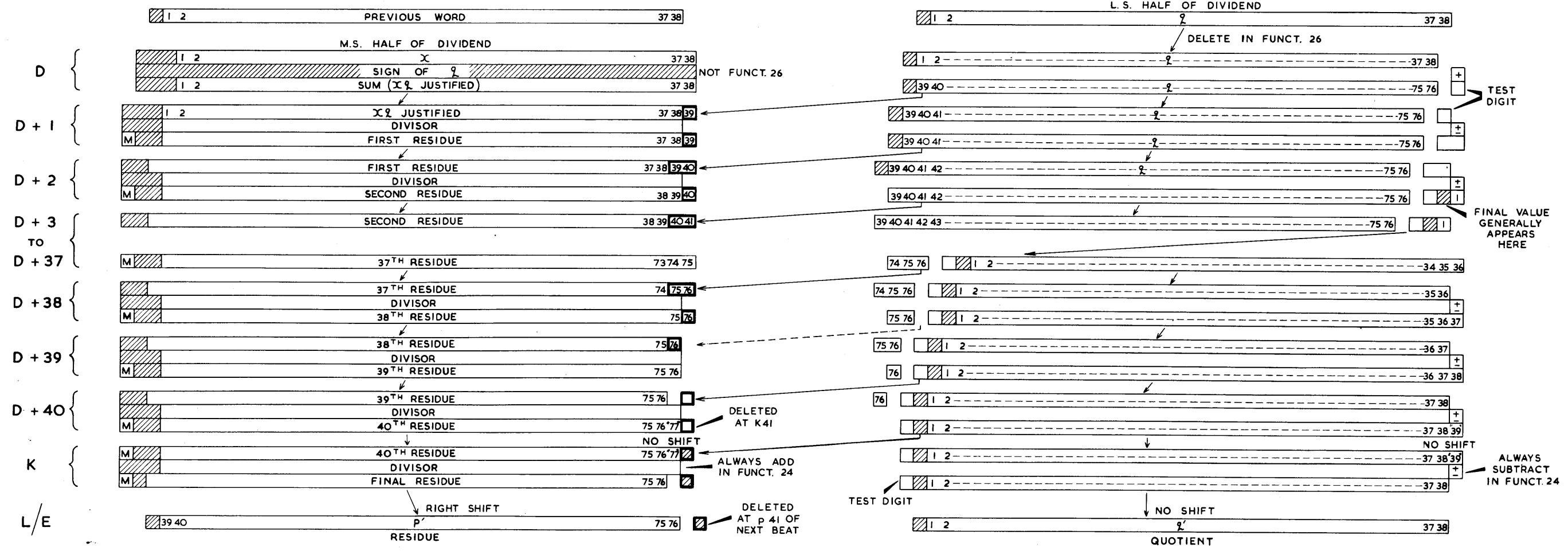


FIG. 14.1 DIVISION (SCHEMATIC)

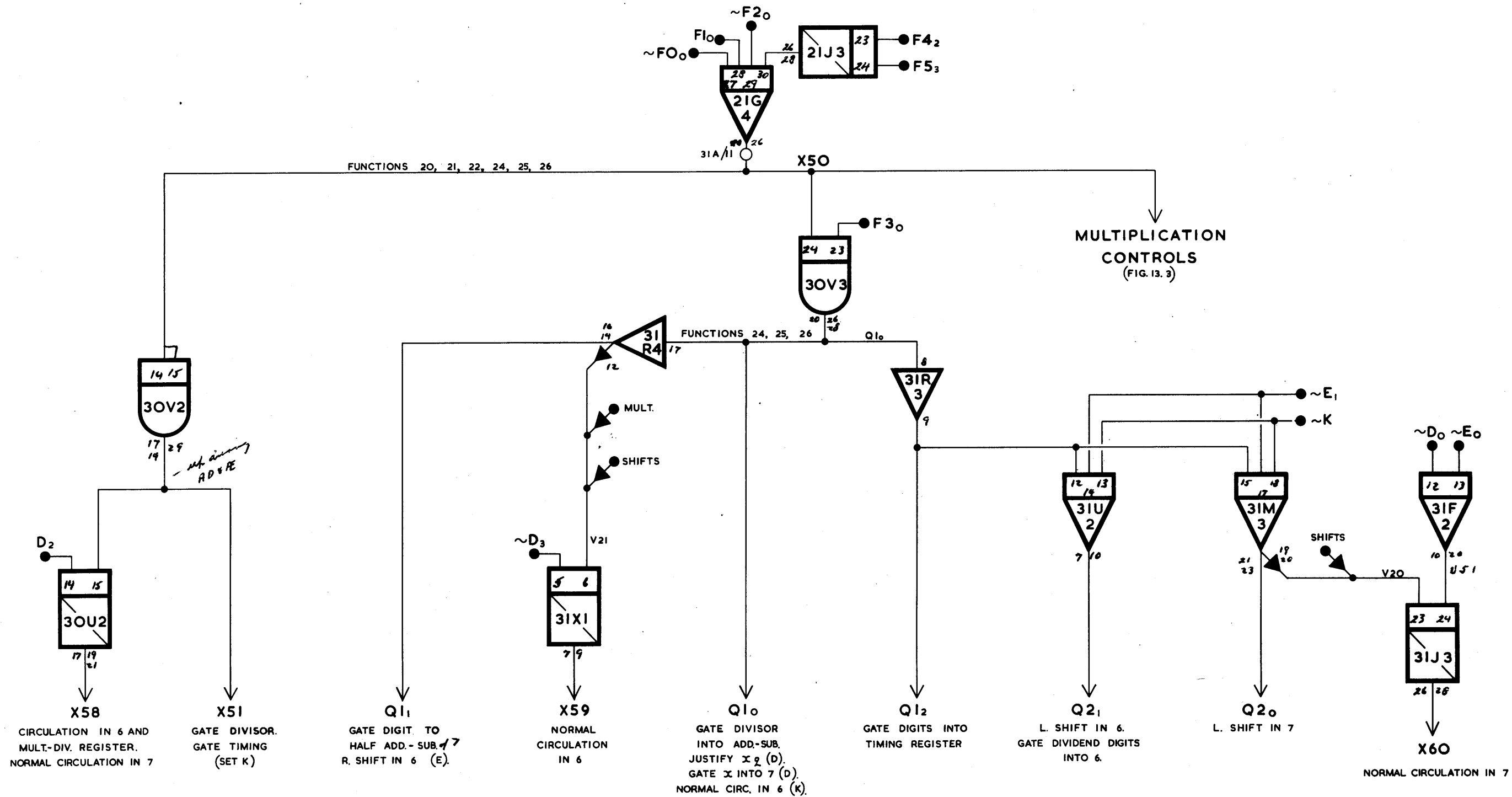


FIG. 14. 2 CONTROLS FOR DIVISION

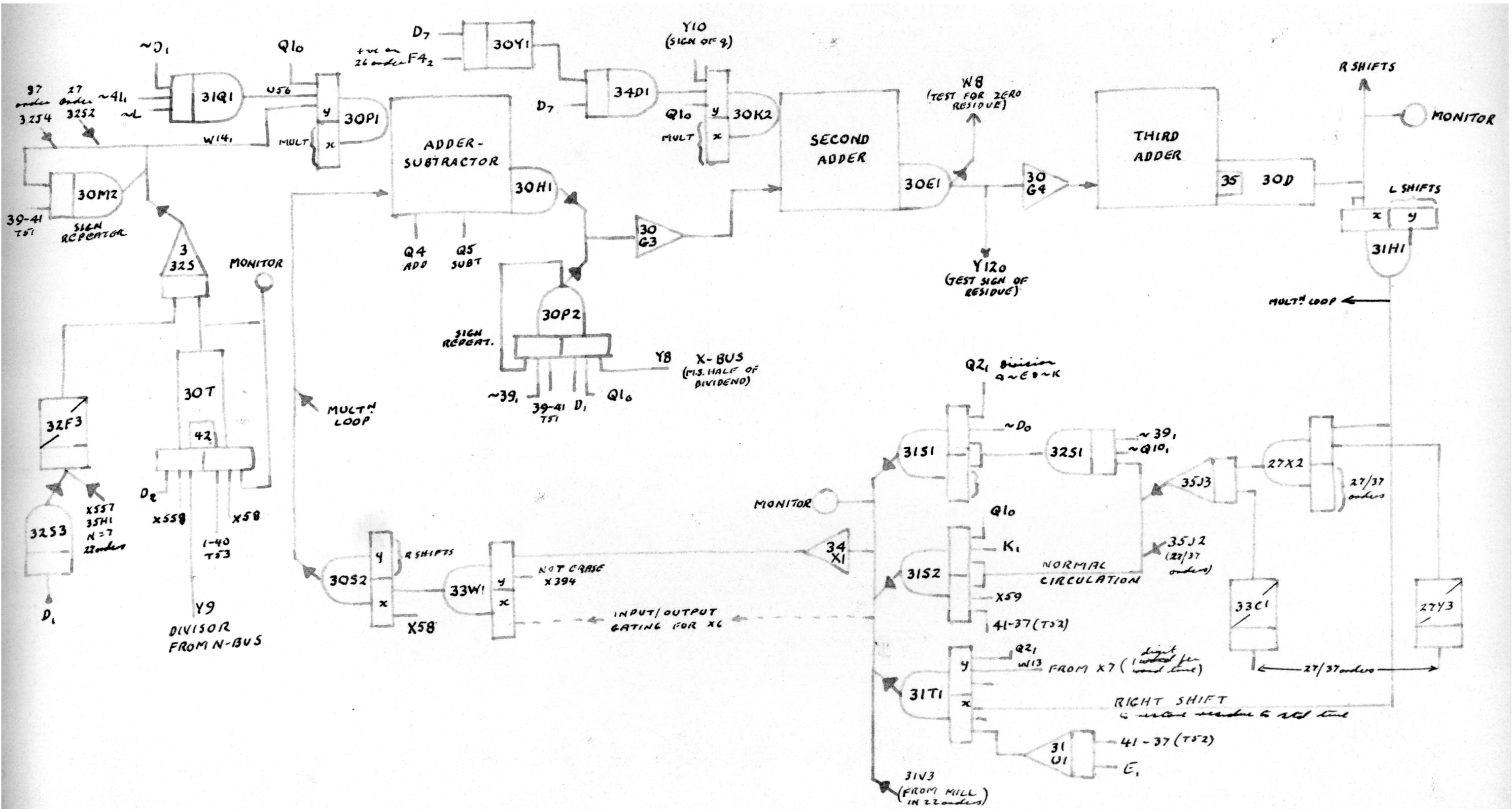


FIG 14.3 ACCUMULATOR 6 IN DIVISION

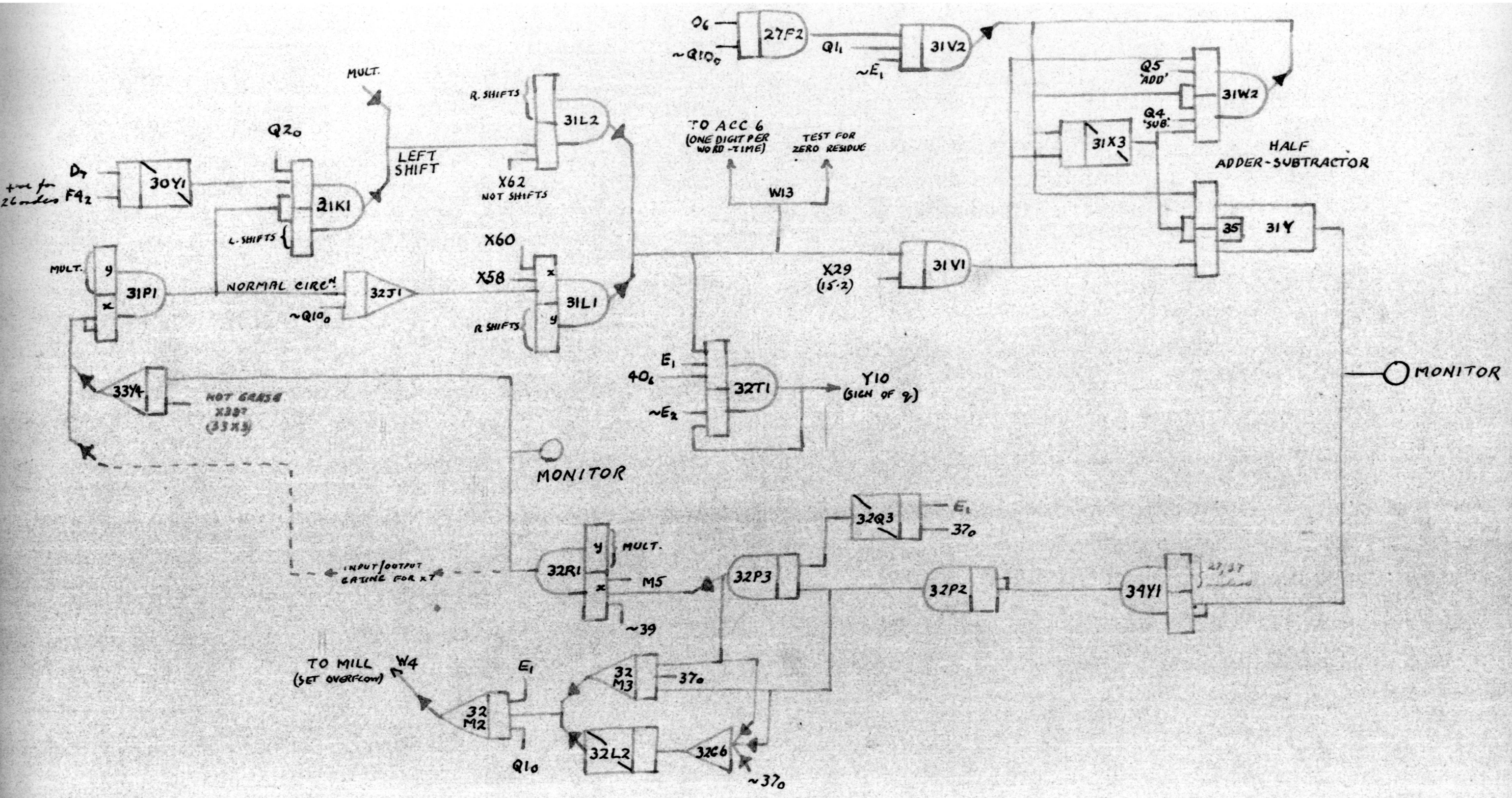


FIG. 14.4 ACCUMULATOR 7 IN DIVISION

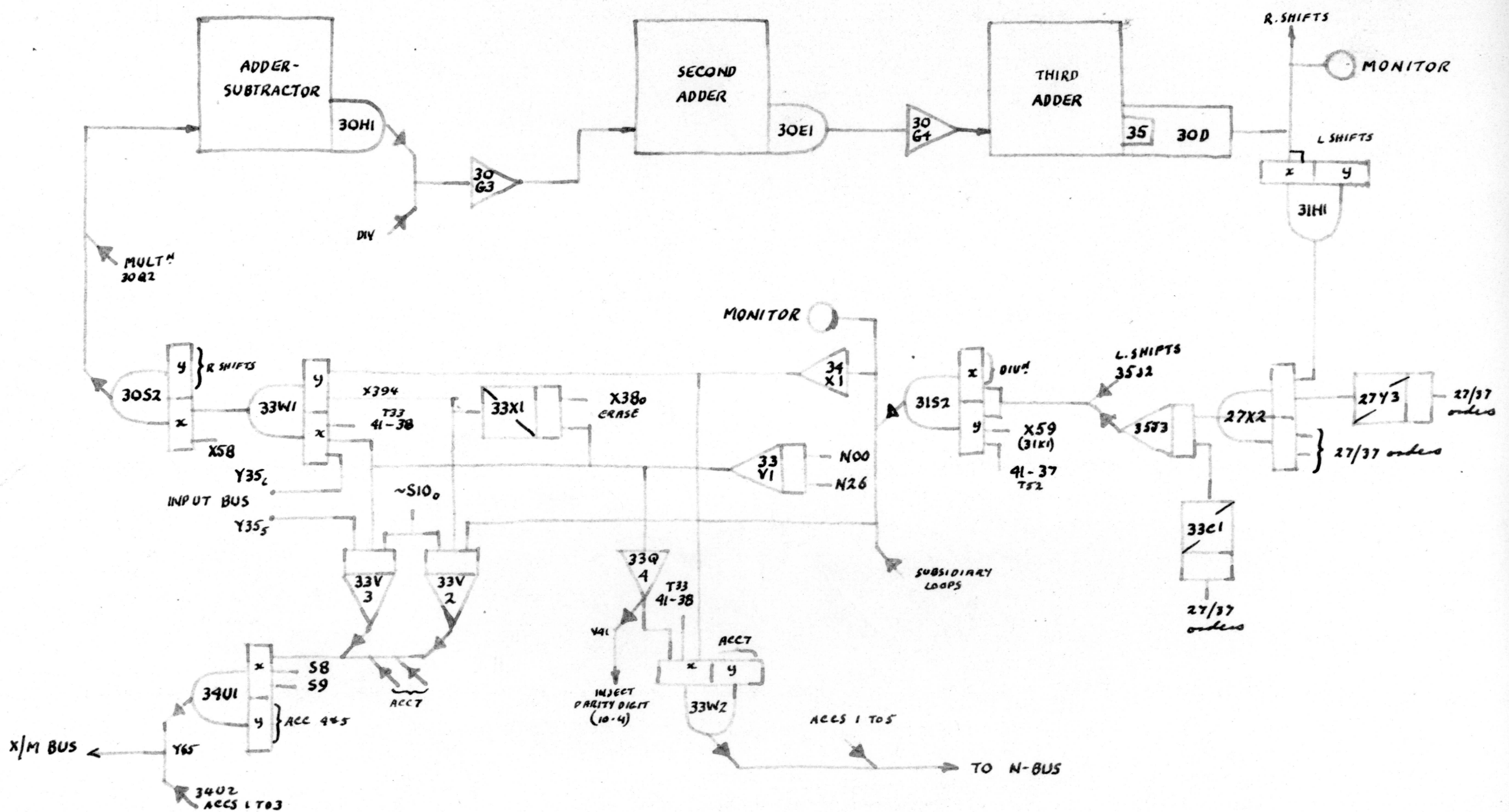


FIG. 15.1 STORAGE IN ADDRESS 6

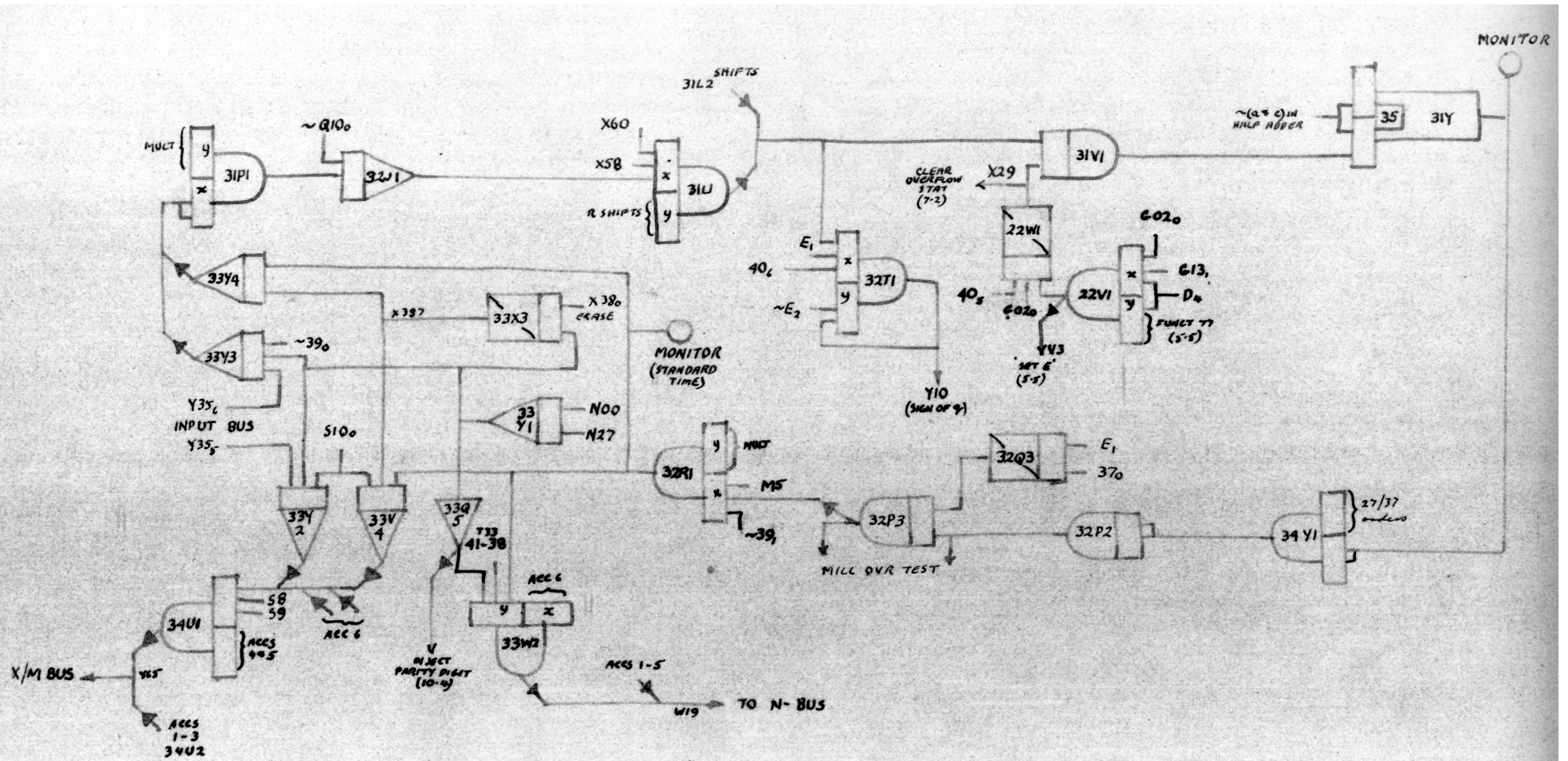


FIG. 15.2 STORAGE IN ADDRESS 7

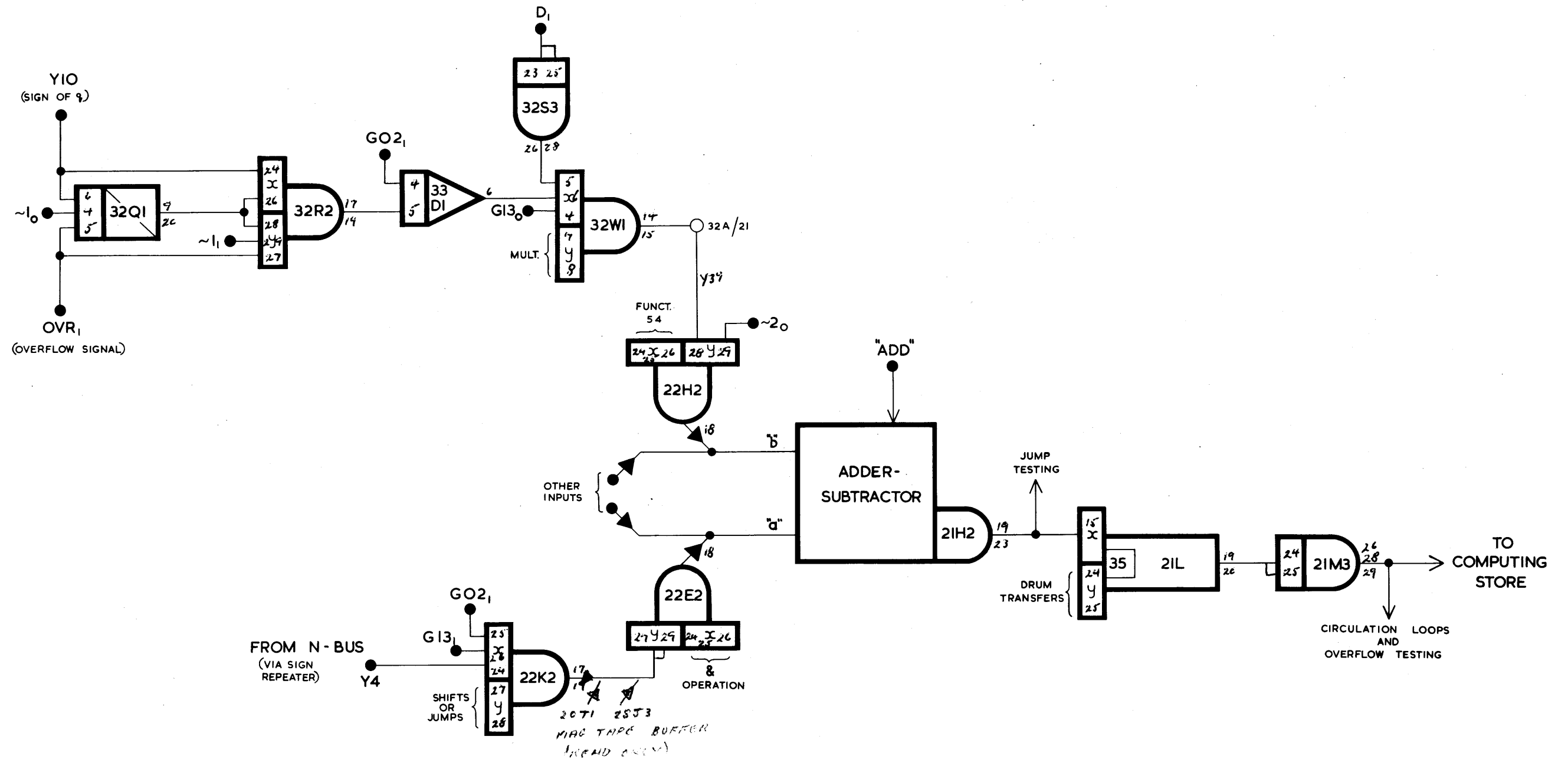


FIG. 15.3 MILL CONNECTIONS FOR JUSTIFICATION.

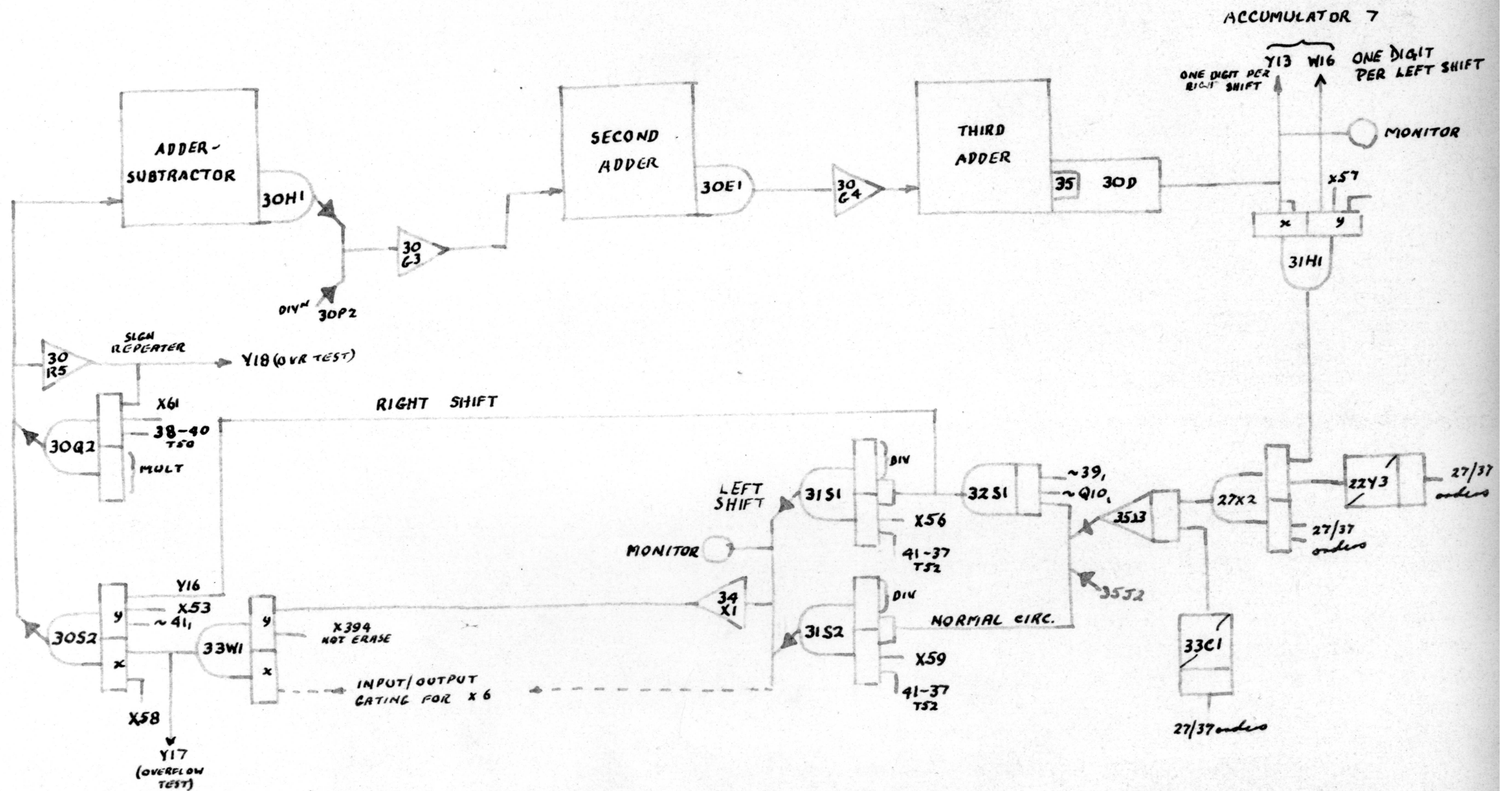


FIG. 16. 4 ACCUMULATOR 6 IN SHIFTS

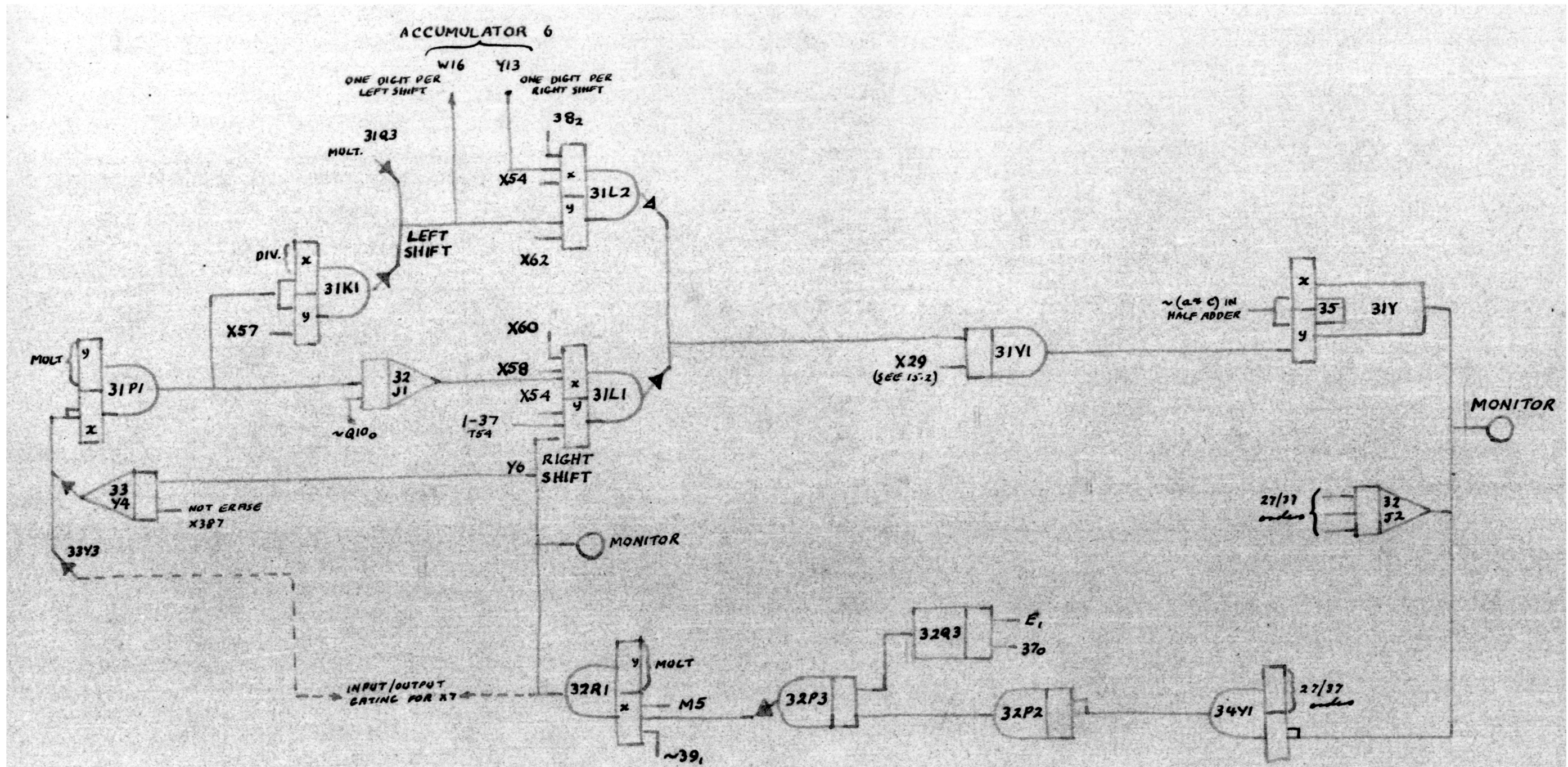
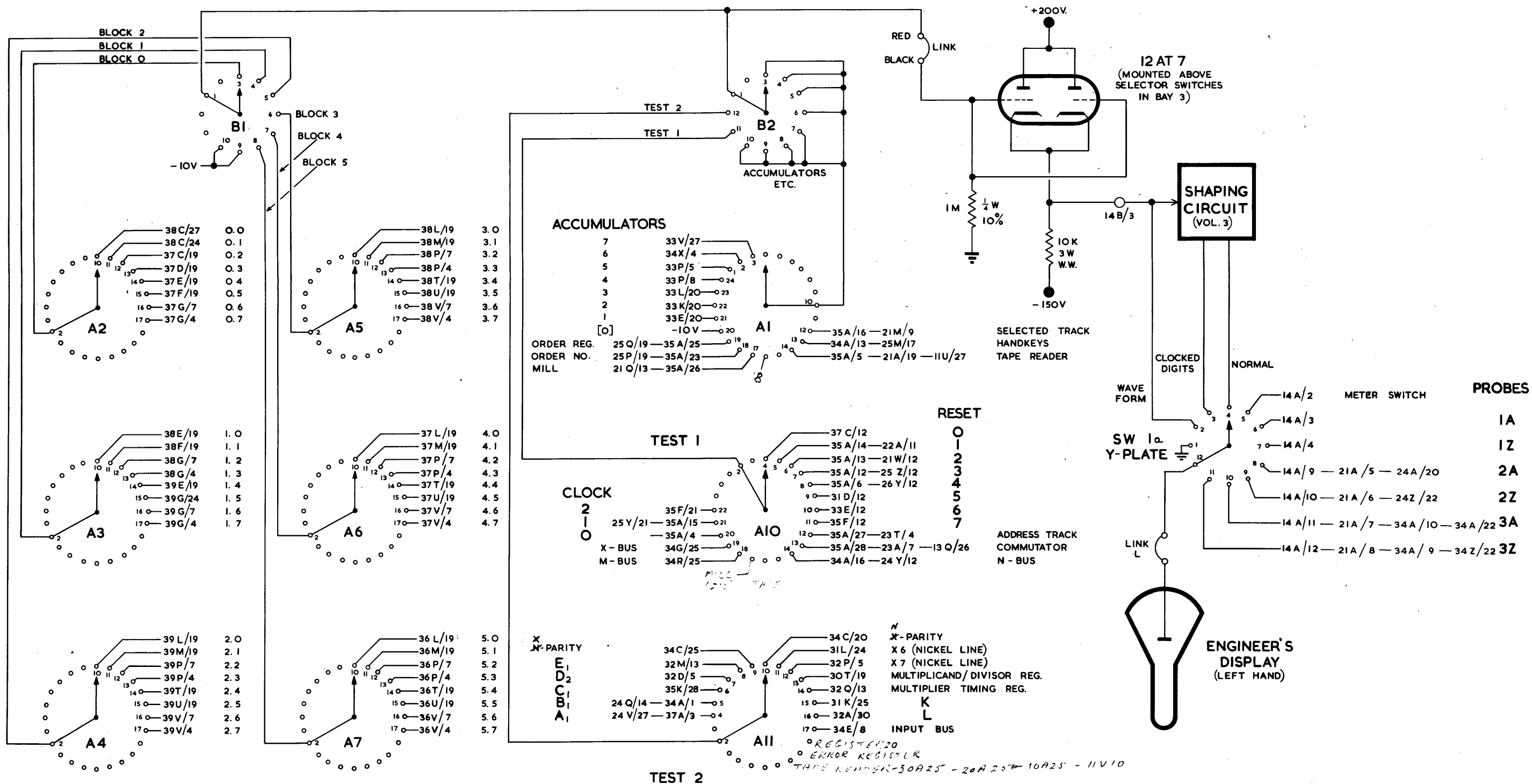


FIG. 16.5 ACCUMULATOR 7 IN SHIFTS



NOTE: WAFERS ARE DRAWN WITH ORIENTATIONS CORRESPONDING TO PANEL ENGRAVING

FIG. 17. 2 SELECTOR SWITCHES FOR ENGINEER'S DISPLAY

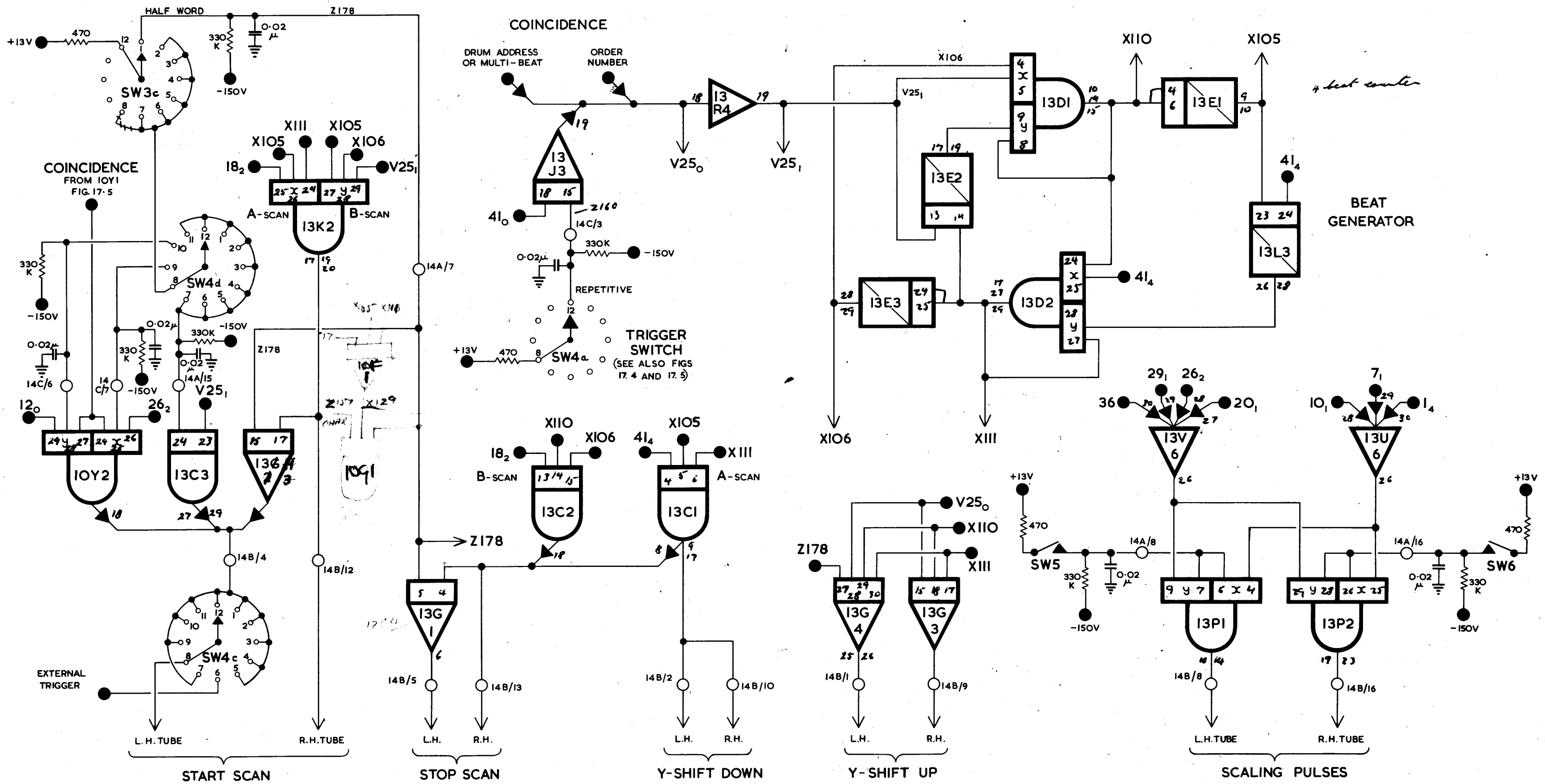


FIG. 17.3

MONITOR CONTROL CIRCUIT.

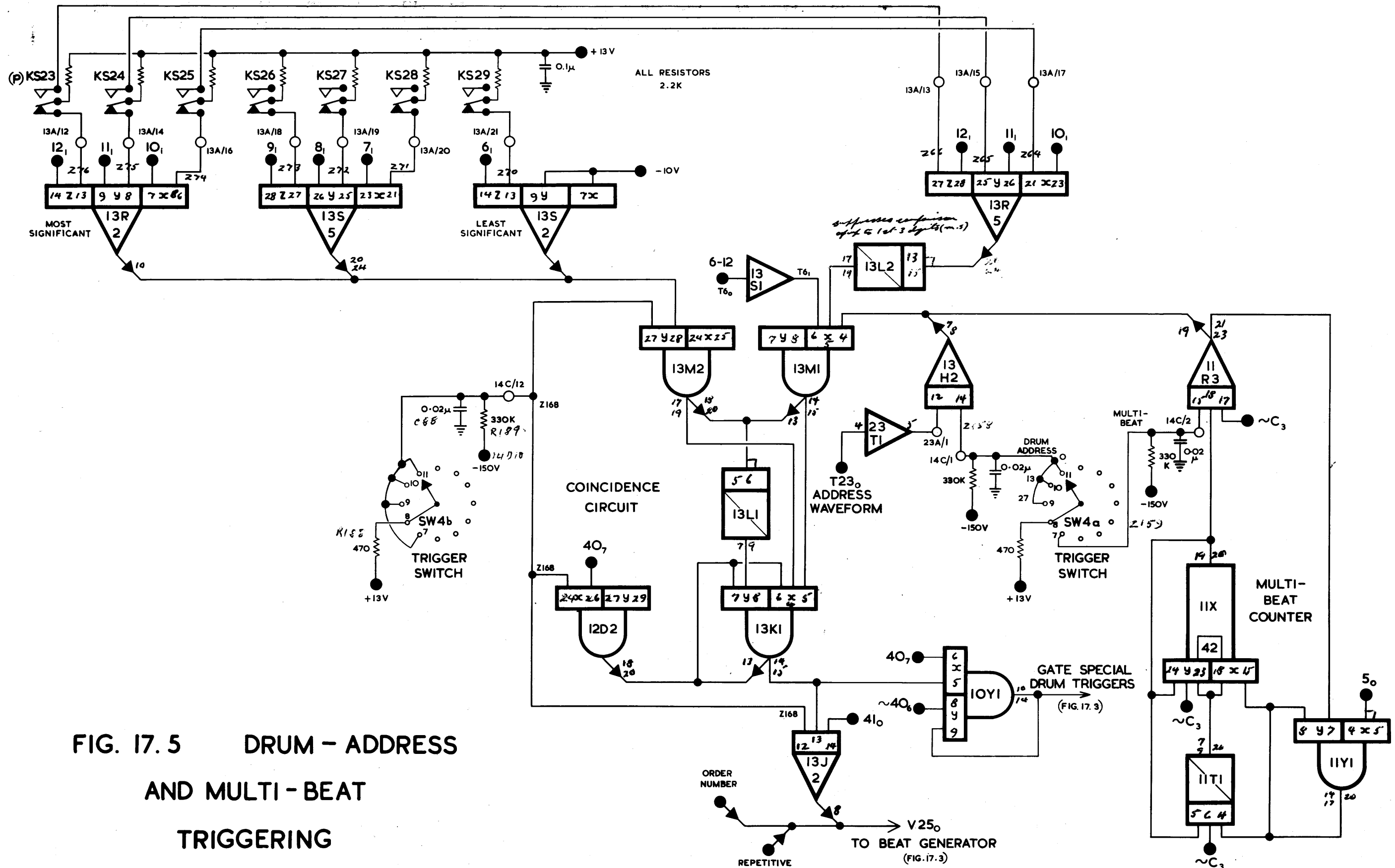
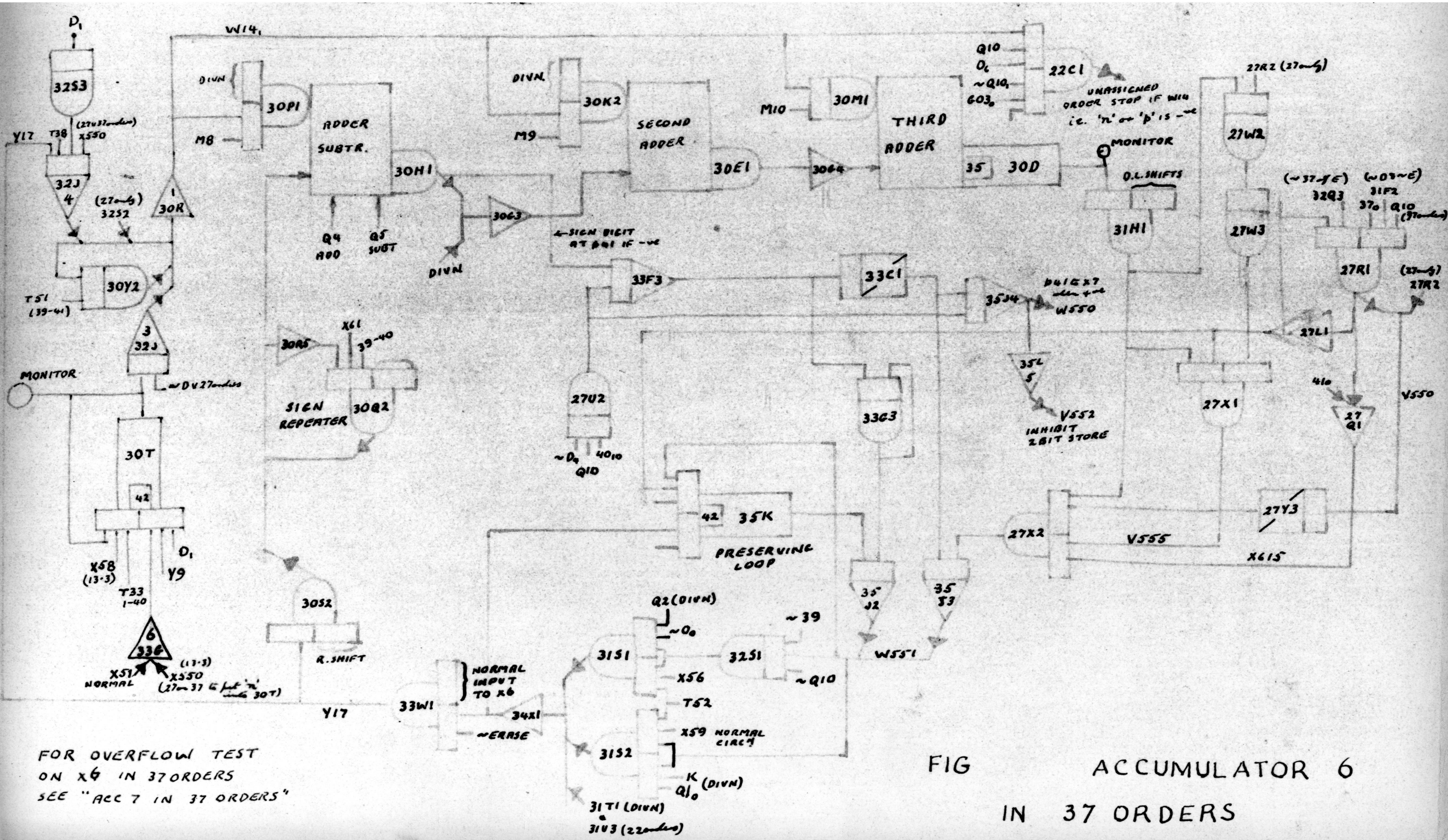


FIG. 17.5 DRUM - ADDRESS AND MULTI - BEAT TRIGGERING



FOR OVERFLOW TEST
ON X6 IN 37 ORDERS
SEE "ACC 7 IN 37 ORDERS"

FIG ACCUMULATOR 6
IN 37 ORDERS

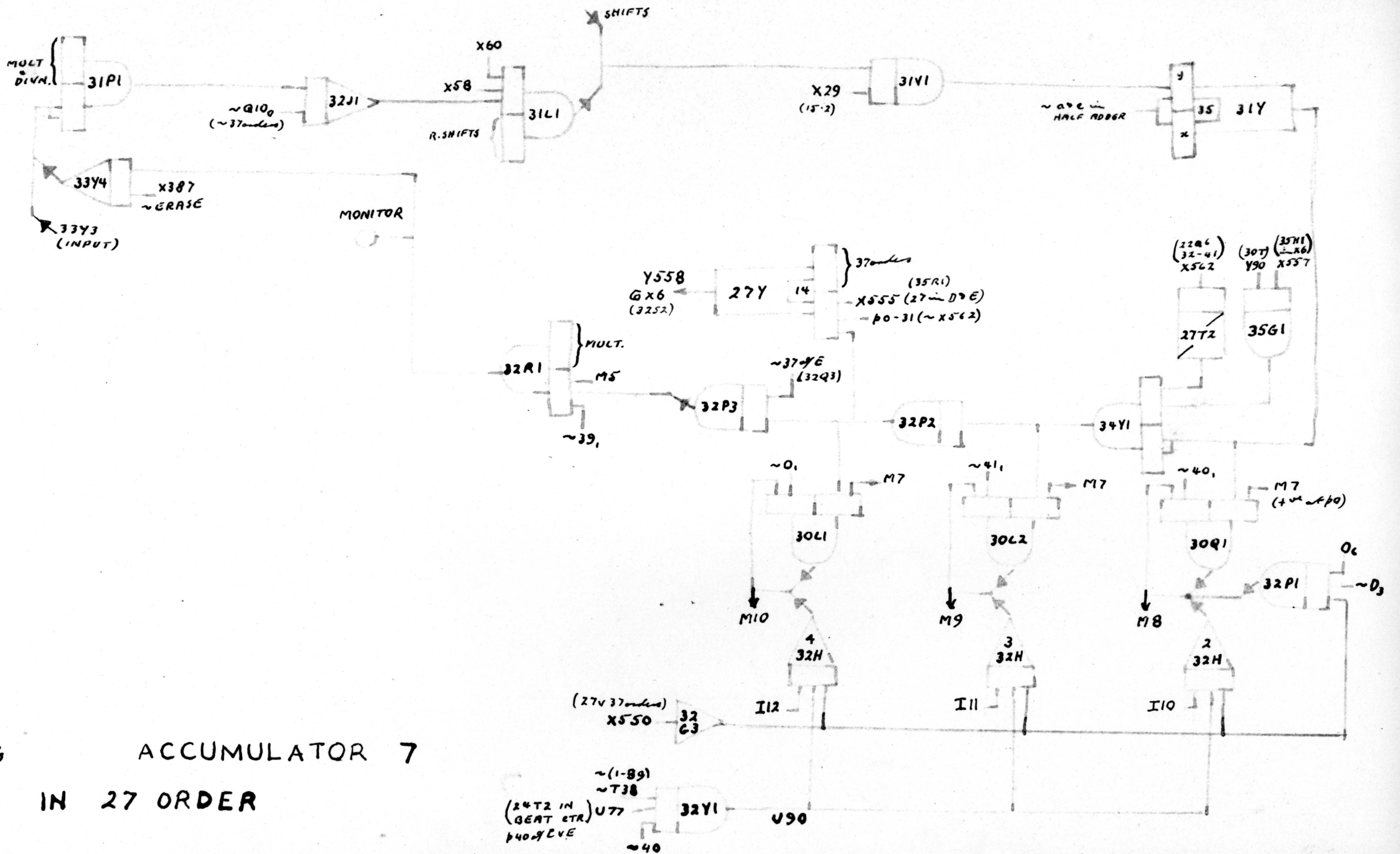


FIG ACCUMULATOR 7
IN 27 ORDER

