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USER'S GUIDE

FOR

DQ202

DISC CONTROLLER

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USER'S GUIDE

FOR

DQ202

DISC CONTROLLER

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SECTION I

GENERAL DESCRIPTION

1.0 INTRODUCTION

This description defines the functional characteristics of a disc drive controller that interfaces LSI-11 based computer systems to SMD interface compatible removable media or winchester disc drives. The complete controller is contained on one quad module that occupies two device locations in the backplane. Data transfers are via the DMA facility of the LSI-11. Full sector buffering in the controller matches the transfer rate of the disc drive and the CPU.

A microprocessor is the sequence and timing center of the controller. The control information is stored as firmware instructions in read-only-memory (ROM) on the controller board. One section of the ROM contains a diagnostic program that tests the functional operation of the controller. This self-test is done automatically each time power is applied or under operator control by pressing the RESET switch. A green DIAGnostic indicator on the controller board lights if self-test passes.

One 60 and two 26-pin connectors, located near the top center of the controller board, are the connection points between the controller and the disc drives. The cable connected to the 60-pin connector conducts the daisy-chained control signals among the disc drives. Data signals between the controller and disc drives are conducted over the 26-pin cables.

1.1 GENERAL DESCRIPTION

The disc controller links the LSI-11 computer to one or more disc storage units. Commands from the computer are received and interpreted by the controller and translated into a form compatible with the disc units. Buffering and signal timing for data transfers between the computer and the discs are performed by the controller.

Data transfers are directly to and from the computer memory using the DMA facility of the LSI-11 I/O bus. In addition, the controller monitors the status of the disc units and the data being transferred and presents this information to the computer upon request. The controller is capable of controlling up to two disc drives in various configurations up to a total on-line capacity of 160 megabytes. **Figure 1-1 illustrates a simplified system.**

*DEC, LSI-11, RT-11 are registered trademarks of Digital Equipment Corporation.

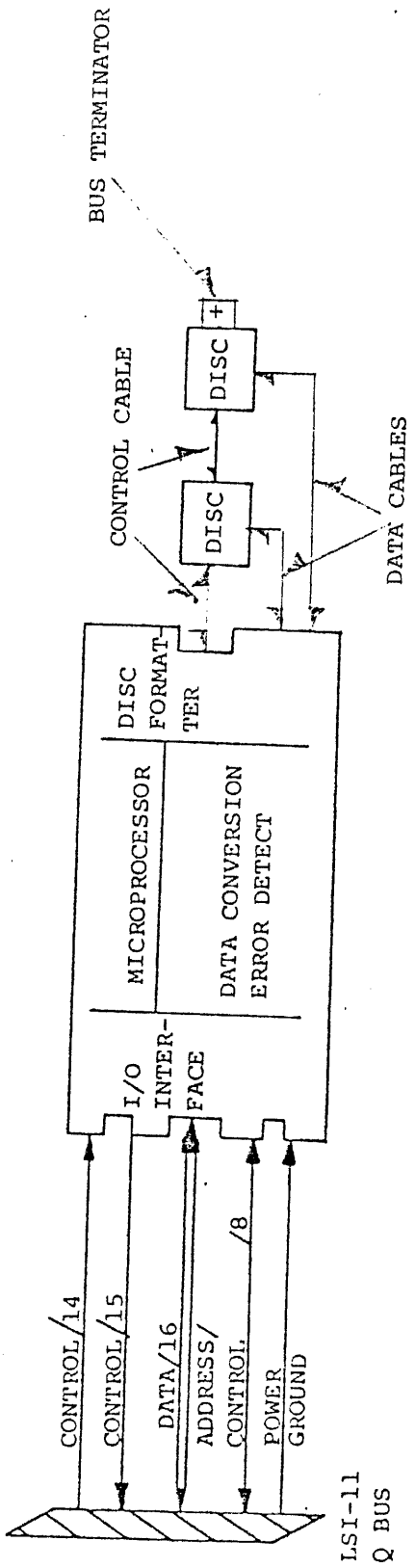


FIGURE 1-1: DISC CONTROLLER SYSTEM SIMPLIFIED DIAGRAM

1.1.1 LSI-11 Q Bus Interface

Commands, data and status transfers between the controller and the computer are executed via the parallel I/O bus (Q bus) of the computer. Data transfers are direct to memory via the DMA facility of the Q bus; commands and status are under programmed I/O and interrupt control. Controller/Q bus interface lines are listed in Table 1-1.

1.1.2 Interrupt

The interrupt vector address is factory set to address 254. The vector address is programmed in a prom on the controller, allowing user selection.

The controller generates interrupt requests to the computer if bits 05 or 13 in controller register RPCS is set (bit 06 is IDE, Interrupt Done Enabler) under the following six conditions:

1. A hard error occurs (RPCS 13 equal hard error).
2. A soft error occurs. Soft errors are either write check errors (WCE) or checksum errors (CSE).
3. The designated number of words have been transferred.
4. A selected disc drive has accepted a seek or drive reset command by acknowledging it's address.
5. Hardware Pool complete indicating a disc drive has completed a seek or drive reset function.

1.1.3 Disc Interface

The controller interfaces with the disc drive, or first of a series of disc drives, through the 60 pin and two 26 pin connectors at the center of the controller board. The maximum cable length from the controller to the last disc drives in a system is 100 feet. Ribbon cables connect the controller to the disc. The 60 pin "A" cable is connected serially among the disc drives. The 26-pin "B" cables are each connected to one disc drive. Figure 1-2 lists the controller to disc interface lines.

TABLE 1-1: Controller/QBus Interface Lines

BUS PIN	MNEMONIC	TO/FROM Q BUS	DESCRIPTION
AJ1,AM1,RT1	GND		Signal Ground and DC return.
AN1	BDMR L	To	Direct Memory Access (DMA) request from controller: active low.
AP1	BHALT L	To	Stops program execution. Refresh and DMA is enabled. Console operation is enabled.
AR1	BREFL	From	Memory Refresh
BA1	BDCOK H	From	DC power ok. All DC voltages are normal.
BB1	BPOK H	From	Primary power ok. When low activates power fail trap sequence.
BJ1,BM1,BT1,BC2	GND		Signal Ground and DC return.
BN1	BSACK L	To	Select Acknowledge. Interlocked with BDMGO indicating controller is bus master in a DMA sequence.
BR1	BEVNT L	To	External Event Interrupt Request.
BV1,AA2,BA2	+5	From	+5 volt system power
AD2,BD2	+12	From	+12 volt system power
AE2	BDOUT L	From/To	Data Out. Valid data from bus master is on the bus. Interlocked with BRPLY.
AF2	BRPLY L	From/To	Reply from slave to BDOUT or BDIN and during IAK.
AH2	BDIN L	From/To	Data Input. Input transfer to master (states master is ready for data). Interlocked with BRPLY.
AJ2	BSYNCL	From/To	Synchronize: becomes active when master places address on bus; stays active during transfer.
AK2	BWTBT L	From/To	Write Byte: indicates output sequence to follow (DATO or DATOB) or marks byte address time during a DATOB.
AL2	B1RQ L	To	Interrupt Request
AM2 AN2	B1AK1 L B1AK0 L	From/To	Serial Interrupt Acknowledge input and output lines routed from QBus, through devices, and back to processor to establish an interrupt priority chain.
AP2	BBS7 L	From/To	Bank 7 Select. Asserted by bus master when addresses in upper 4K bank (28-32K words) is placed on the bus.
AR2 AS2	BDMG1 L BDMG0 L	From/To	DMA Grant Input and Output. Serial DMA priority line from computer, through devices, and back to computer.

(more)

TABLE 1-1: Controller/QBus Interface Lines, continued

BUS PIN	MNEMONIC	TO/FROM Q BUS	DESCRIPTION
AT2	BINIT L	From	Initialize. Clears devices on I/O bus
AU2,AV2	BDAL0/DAL1	From/To	Data/address lines 0 & 1, (2 of 16)
BE2,BF2,BH2	BDAL2	From/To	Data/address lines, 2-15, (14 of 16)
BJ2,BK2,BL2	through		
BM2,BN2,BP2	BDAL 15		
BR2,BS2,BT2			
BU2,BV2			
AC1	BAD16	To	Extended Address Bit
AD1	BAD17	To	

SIGNAL NAME	PIN POLARITY (ACTIVE)		SOURCE
	–	+	
DEVICE SELECT 0	23	53	Control Unit
DEVICE SELECT 1	24	54	Control Unit
DEVICE SELECT 2	26	56	Control Unit
DEVICE SELECT 3	27	57	Control Unit
SELECT ENABLE	22	52	Control Unit
SET CYLINDER TAG	1	31	Control Unit
SET HEAD TAG	2	32	Control Unit
CONTROL SELECT	3	33	Control Unit
BUS OUT 0	4	34	Control Unit
BUS OUT 1	5	35	Control Unit
BUS OUT 2	6	36	Control Unit
BUS OUT 3	7	37	Control Unit
BUS OUT 4	8	38	Control Unit
BUS OUT 5	9	39	Control Unit
BUS OUT 6	10	40	Control Unit
BUS OUT 7	11	41	Control Unit
BUS OUT 8	12	42	Control Unit
BUS OUT 9	13	43	Control Unit
BUS OUT 10	30	60	Control Unit
DEVICE ENABLE	14	44	Control Unit
INDEX	18	48	Drive
SECTOR MARK	25	55	Drive
FAULT	15	45	Drive
SEEK ERROR	16	46	Drive
ON CYLINDER	17	47	Drive
UNIT READY	19	49	Drive
WRITE PROTECTED	28	58	Drive
ADDRESS MARK	20	50	Drive
BUSY (DUAL-PORT ONLY)	21	51	Drive
SEQUENCE IN	29		Control Unit
HOLD	59		Control Unit

FIGURE 1-2a: Controller/Disc I/O Interface "A" CABLE

SIGNAL	PIN POLARITY (ACTIVE)			SOURCE
	–	+	GROUND	
Ground			1	
Servo Clock	2	14		Drive
Ground			15	
Read Data	3	16		Drive
Ground			4	
Read Clock	5	17		Drive
Ground			18	
Write Clock	6	19		CU
Ground			7	
Write Data	8	20		CU
Ground			21	
Unit Selected	22			Drive
Seek End	10	23		Drive
Ground			11	
Reserved for Index	12	24		
Ground			25	
Reserved for Sector	13	26		

FIGURE 1-2b: Controller/Disc I/O Interface "B" CABLE

1.1.4 Disc Data Format

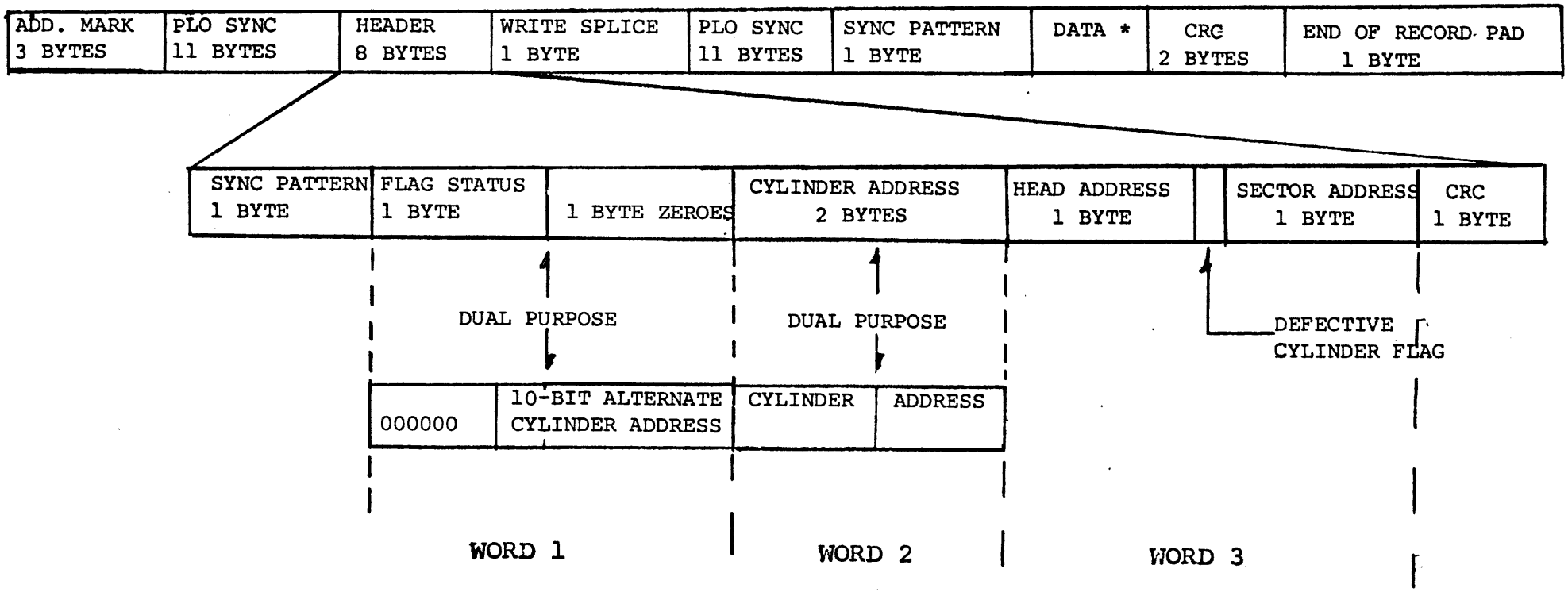
The DQ202 controller functions with disc assemblies that are capable of being either soft or hard sectored. Disc storage units must be initialized by a format routine that writes header records on the disc surfaces. These header records contain address information for position verification and sector size information for use by the controller electronics.

Any read or write function causes the header of the addressed sector to be read into the controller. The controller acts upon the sector size portion of the header to configure itself to either read or write the proper number of bytes in the data record portion of the sector.

Figure 1-3 illustrates the disc sector format. During the format function words 1, 2, and 3 of the header record are accessed from computer memory and written in each sector of the disc. During either read or write functions, the data record is read from disc or written to disc respectively. All other information in the sector (PLO sync, sync pattern, CRC, etc.) is generated by the controller. Paragraph 4.3 describes the sector format in detail.

1.2 SPECIFICATIONS

- Data Format:
  - -512 data bytes per sector
  - -up to 10 sectors per cylinder
  - -up to 404 cylinders per disc drive.
  - -up to 20 heads per cylinder.
  - -maximum of 2 discs per controller.
- Register Addresses:
  - -Drive status (RPDS) 776 710
  - -Error (PRER) 776-712
  - -Control Status (RPCS) 776 714
  - -Word Count (RPWC) 776 716
  - -Bus Address (RPBA) 776 720
  - -Cylinder Address (RPCA) 776 722
  - -Disc Address (RPDA) 776 724
  - -Data Buffer (RPDB) 776 726



* Data Block Size 512 Bytes

FIGURE 1-3: DQ202 SECTOR FORMAT

. Computer I/O Interface:	-Interrupt vector address 254.
. Disc Interface:	-Control Data SMD Compatible -Controller is compatible with discs manufactured by Control Data, Ampex, Futjitsu, Century Data, PRIAM, Kennedy, etc. The connectors at the controller end are a 3M 60-pin and two 26-pin ribbon cable connectors.
. Bootstrap Loader:	-on board bootstrap loader.
. Packaging:	-The controller is completely contained on one quad module 10.44 inches wide by 8.88 inches deep. Optionally supplied with the controller are two 10-foot cables to the first disc drive. Adapter connectors may be required at the disc end depending on the disc manufacturer.
. Documentation:	-One instruction manual and one set of circuit diagrams are supplied with each controller.
. Power:	+5, ±.25 VDC at 3.5 AMPS +12, ±5 VDC at 0.3 AMPS
. Environment:	-Operating temperature 50° to 140°F. -Operating humidity 0 to 90% non-condensing.
. Shipping Weight:	5 pounds, including documentation
. Options:	On-site installation, factory integration of disc. Complete disc systems.

SECTION 2

INSTALLATION

2.1 INSTALLATION

The padded shipping carton that contains the controller board also contains an instruction manual and cables to the first disc drive (if this option is exercised). The controller is completely contained on the quad-size printed circuit board. The disc (or discs), if supplied is contained in a separate shipping carton.

CAUTION

IF DAMAGE TO ANY OF THE COMPONENTS
IS NOTED, DO NOT INSTALL. IMMEDIATELY
INFORM THE CARRIER AND DILOG.

Installation instructions for the disc are contained in the disc manual. Before installing any components of the disc system, read Sections 1, 2 and 3 of the instruction manual for the controller.

2.2 PRE-INSTALLATION CHECKS

There are various LSI-11 configurations, many of which were installed before DEC made a hard disc available for LSI-11 based systems. Certain configurations require minor modifications before operating the DQ200 disc system. These modifications are as follows:

A. If the system contains a REV11-C module, it must be placed closer to the processor module (higher priority) than the DQ202 controller if the DMA refresh logic on the REV11-C is enabled.

B. If the 4K memory on the DK11-F is not used and the memory in the system does not require external refresh, the DMA refresh logic on the REV11-C should be disabled by removing jumper W2 on the REV11-C module.

C. If the system contains a REV11-A module, the refresh DMA logic must be disabled since the module must be placed at the end of the bus (REV11-A contains bus terminator).

D. If the REV11-C module is installed, cut etch to pin 12 on circuit D30 (top of board) and add jumper between pin 12 and pin 13 of D30.

E. If system requires more than a 4 x 4 backplane, place the REV-11 terminator in the last available location in the last backplane.

2.3 INSTALLING

To install the controller module, proceed as follows:

CAUTION

A. REMOVE DC POWER FROM MOUNTING ASSEMBLY BEFORE INSERTING OR REMOVING CONTROLLER MODULE.

B. DAMAGE TO THE BACKPLANE ASSEMBLY MAY OCCUR IF THE CONTROLLER MODULE IS PLUGGED IN BACKWARDS.

1. Select the backplane location into which the controller is to be inserted. Be sure that the disc controller is the lowest priority DMA device in the computer except if the DMA refresh/ bootstrap ROM option module is installed in the system. The lowest priority device is the device farthest from the processor module. Note that the DQ202 contains a bootstrap ROM.

   There are several backplane assemblies depending on the type system: H9270 backplane, DDV11-B backplane, BA11 expansion box. Fig. 2-2 shows typical backplane configurations. Note that the processor module is always installed in the first location of the backplane or the first location in the first backplane of multiple backplane systems.

   It is important that all option slots between the processor and the disc controller be filled to ensure that the daisy-chained interrupt (BIAK) and DMA (BDMG) signal be complete to the controller slots. If empty slots are between the controller and any option board, the following backplane jumpers must be installed:

FROM			TO			SIGNAL
C0	X	N2	C0	X	M2	BIAK1/L0
C0	X	S2	C0	X	R2	BDMG1/L0

Last Full Option Slot

Controller Slot

2. Insert the controller into the selected backplane position. Be sure the controller is installed with the components facing Row One (1).

   The controller module is equipped with handles on the side opposite the slot connectors. Gently position the module slot connectors into the backplane then press until the module connectors are firmly seated into the backplane. Both handles must be pressed simultaneously. When removing the module, apply equal pulling pressure to both handles.

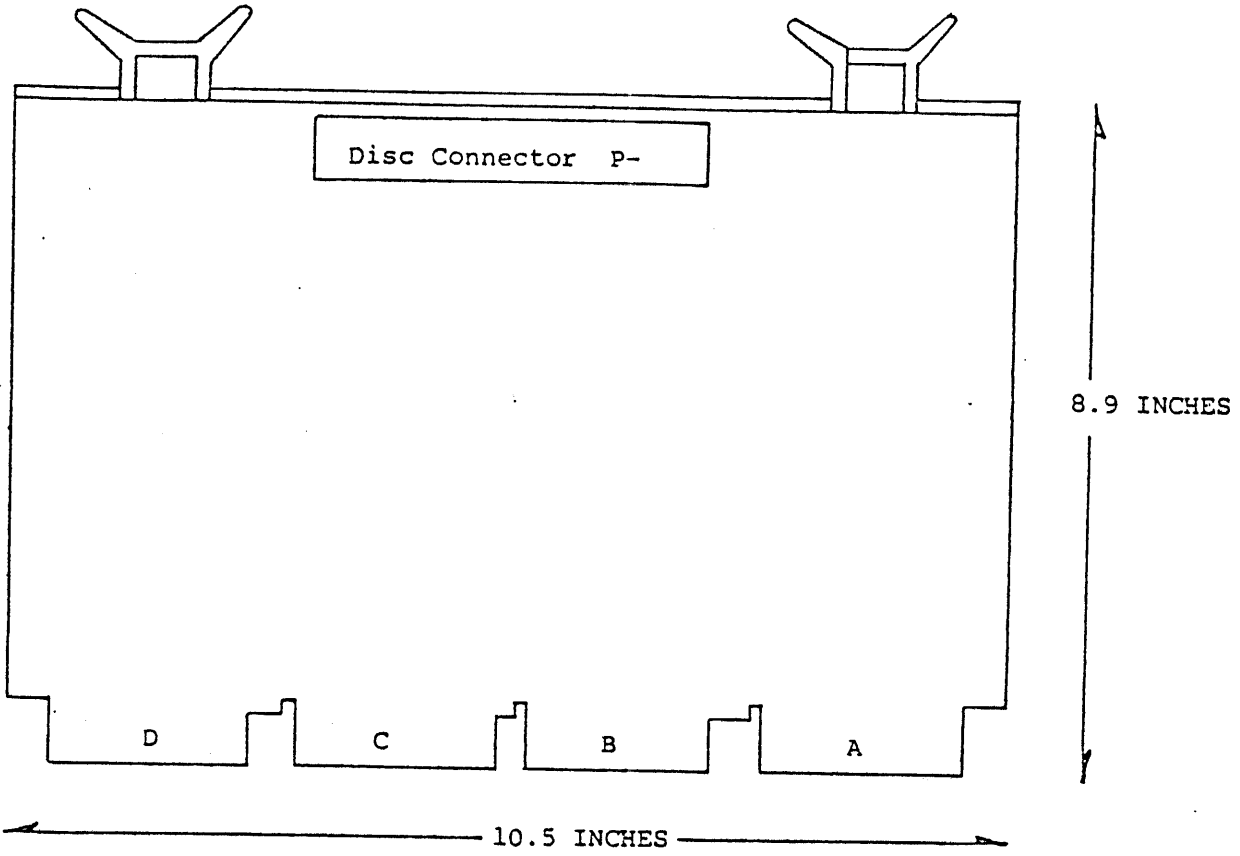
3. Feed the module connector end of the disc I/O cables into the computer module connectors. Install the cable connectors into the module connectors. Verify that the connectors are firmly seated.

4. Connect the disc-end of the I/O cables to the disc I/O connectors. Be sure that the bus terminator is installed at the last disc in the system.

5. Refer to the disc manual for operating instructions and apply power to the disc and computer.

6. Observe that the green DIAGnostic LED on the controller board is lit.

7. The system is now ready to operate. Refer to Section 3 for operating instructions. Run diagnostic to verify correct operation of disc system.



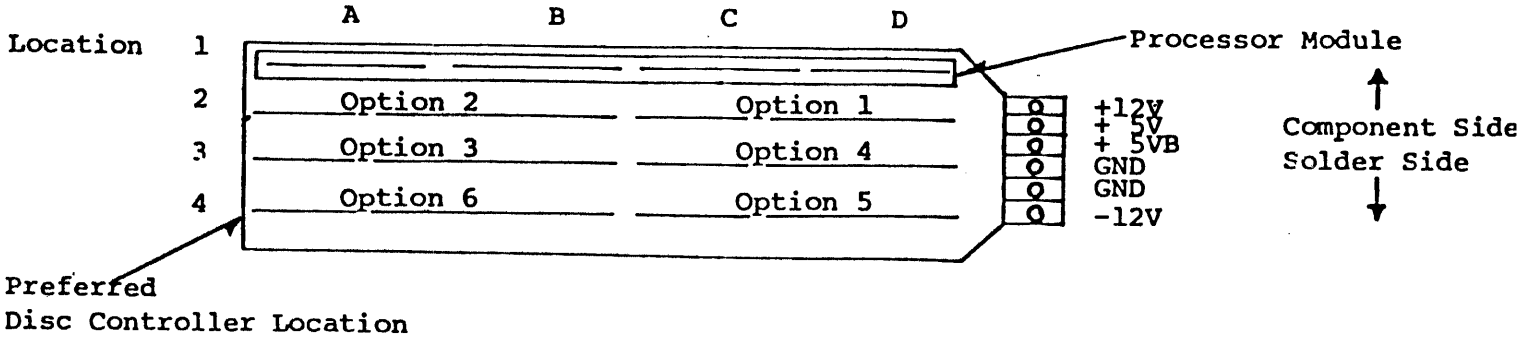
COMPONENT SIDE

SWITCH	POSITION	DEFINITION
S1	ON	Disable bootstrap
	OFF	Enable bootstrap
S2	ON	Retry Error one time
	OFF	Retry Error three times
S3	ON	Inhibit write format
	OFF	Enable write format
S4	ON	CMD Enable
	OFF	All other drives
S5	**ON**	**Two physical drives per controller***
	OFF	**One physical driver per controller.**

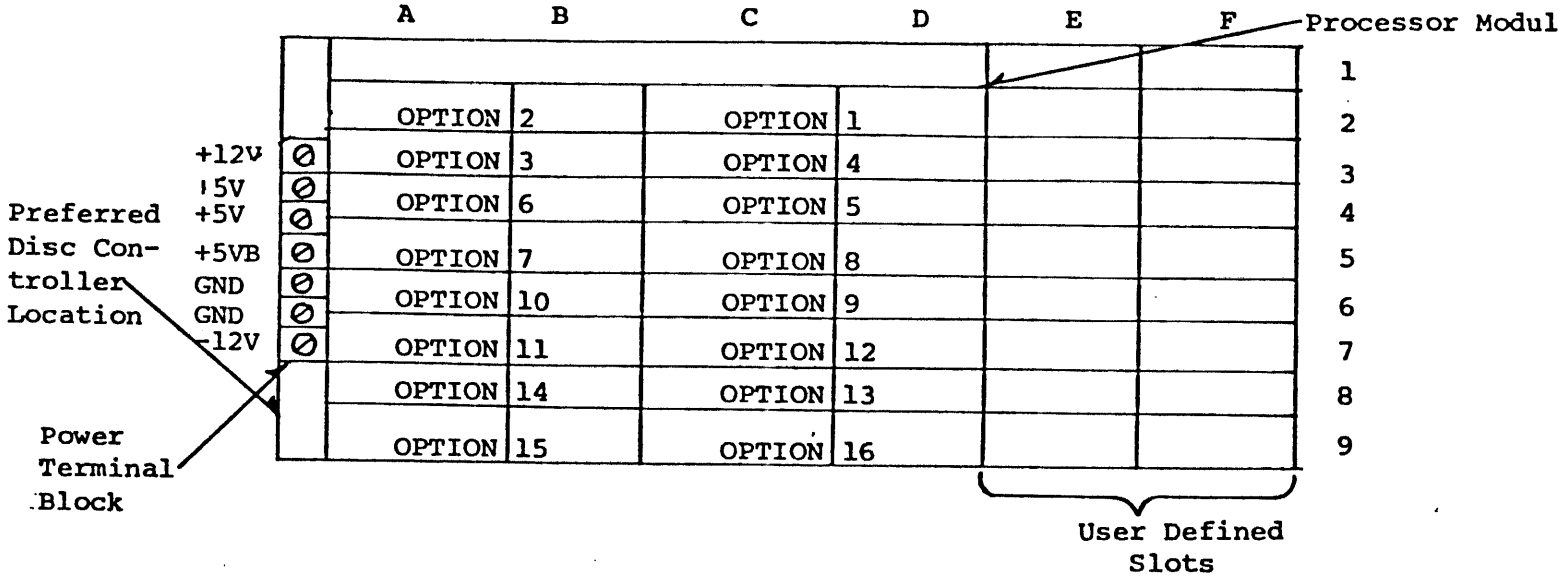
*The second drive is always addressed beginning with logical unit 4, regardless of the number of logical units (must be less than four) in the first drive.

NOTE: Off is the normal position of the switches.

FIGURE 2-1: Controller Configuration



H9270 MODULE INSERTION SIDE



DDV11-B Backplane Module Insertion Side

NOTE: Memory can be installed in any slot; it is not priority dependent and does not need to be adjacent to the processor.

Controllers are also compatible with H9273A Modules.

FIGURE 2-2: Typical Backplane Configurations

SECTION 3

OPERATION

3.0 INTRODUCTION

This section contains procedures for operating the computer system with the DQ202 controller and an SMD disc, or discs. An understanding of Section 2 "OPERATION" of the Digital "MICROCOMPUTER HANDBOOK" is assumed. The material is provided for "first time users" of disc subsystems and describes procedures such as:

Bootstrapping

Operations are conducted from the console device. To reduce confusion the format of operating procedures and the system response will conform to the syntax established in the **Digital (DEC) handbook.** For example, not underlined characters are those typed (displayed) by the system; characters underlined are those typed by the operator.

3.1 PRECAUTIONS AND PREOPERATION CHECKS

The following precautions should be observed while operating the system. Failure to observe these precautions could cause damage to the controller, the disc cartridge, the computer, or could erase a portion or all of the stored software.

1. Do not remove or replace the controller board with power applied to the computer.

2. If system does not operate properly, check operating procedures and verify items in paragraph 2.2, "preinstallation checks" have been performed.

Before operation the following checks should be made:

1. Verify DQ202 board is firmly seated in backplane connector.

2. Verify cable between DQ202 board connector J1 and disc drive is installed.

3. Be sure disc drive cartridge is installed (if it is to be used.)

4. Apply power to computer and console device.

5. If a hardware bootstrap is resident in the system, set S1 ON.

6. See Paragraph 3.2.2 for proper position of switch S5.

5. Verify that green DIAG light on front edge of DQ202 board lights.

6. Be sure power is applied to disc drive and READY light is on.

3.2 BOOTSTRAPPING

This discussion is intended to clarify the locations and purposes of various starting (bootstrap) routines in the computer system. Bootstrapping is discussed because a question often asked is: "Is the REV.11-A or -C option required with the DQ200 disc system so that it is not necessary to enter the bootstrap program manually? The answer is no, REV.11 is not required. This is because the DQ202 has a hardware bootstrap. Bootstrapping is defined as:

> "A technique or routine whose first instructions are sufficient to load (into computer memory) the remainder of itself then load and start a complex system of programs."

One of the complex programs the bootstrap program loads is another loader, either an absolute loader (AL) or a relocatable loader (RL). The combination of the bootstrap loader and either an AL or an RL loads an operational program, such as a monitor.

There are two types of bootstrap loaders: hardware and software. The DEC REV.11-A or REV.11-C options contain hardware loaders contained in ROM. Software loaders can be contained in memory (obviously), on flexible diskettes, cartridge discs, pack discs, magnetic tape, or DEC PACKS.

The confusion occurs because most users are familiar with RXV11 floppy disc-based system operation, which requires either the REV.11 option or manual entry of a program to bootstrap the system monitor from diskette into computer memory. Other than the 10-to-one, or greater, difference in storage capacity between the diskette system and the cartridge disc system, the principle difference between the two is the data transfer method. The diskette controller transfers data via the programmed I/O bus; the DQ200 controller transfers data via the DMA bus. Once the DQ200 controller registers are initialized, it becomes bus master and loads both the bootstrap program and absolute loader program from the disc into computer memory. These two loaders then load the operating system from disc into computer memory.

3.2.1 Bootstrap Program

The device name of the DQ202 is DP. The controller contains an on-board bootstrap ROM. This ROM can be either enabled or disabled by switch S1 on the controller board (see Figure 2-1). Setting switch S1 OFF enables the controller bootstrap; setting switch S1 ON disables the controller bootstrap. If the DEC supplied bootstrap ROM is installed in the system, switch S1 must be ON to disable the controller bootstrap ROM. In any case the following bootstrap procedure assumes that either the DEC bootstrap ROM is in the system or that switch S1 is OFF. If neither bootstrap is installed/enabled and an attempt is made to boot the system, the following error message will be displayed:

@ 173002

BOOTSTRAP PROCEDURE:

The following assumes the system is in ODT mode. Note that the bootstrap can be used under processor Power Up Mode 2 conditions. Refer to the appropriate section of the DEC processor manual for a discussion of the Power Up Modes. Further note that the disc drive does not need to be READY to enter the bootstrap.

Reset the system by pressing RESET or enter the following (characters underlined are output by the system; characters not underlined are input by the operator):

@ 173000G

DP? 0 <CR> Operator please note that booting can be executed from logical units other than "0" shown in the example by entering the desired logical unit number, i.e., 1,2,3,..... or 7.

3.2.2 Bootstrap Switch

Switch S1 controls the operation of the bootstrap ROM. Switch S1 enables or disables the ROM.

3.3 TEST AND FORMAT PROGRAM

This DILOG supplied program tests the DILOG controller and the disc drive(s) and also formats the disc(s). During formatting, the program also verifies the disc. If there are media errors on the disc, the cylinder, head (logical unit) and sectors in which the errors occur are displayed on the CRT terminal. In several sections of the program the operator has the option of assigning alternate cylinders.

The test/format program contains the following sections:

1. TEST CONTROLLER
   A. Test controller registers.
   B. Test controller data buffer.

2. TEST DISC DRIVE
   A. Test if disc ready.
   B. Test of disc will restore (seek to cylinder zero).

3. FORMAT THE DISC
   This section allows the selection of logical units to be formatted. While formatting the following sequence occurs:
   A. Write headers (all data will be erased).
   B. Read headers.
   C. Write data test pattern.
   D. Read data test pattern; alternate cylinders may be assigned at this time if media errors are detected.

4. SEQUENTIAL READ TEST
   This section reads data from all logical units starting at logical unit zero. If a read error is detected, an alternate cylinder may be assigned at this time.

5. SELECTED READ TEST
   This section allows the selection of a specific logical unit to be tested (read data only). If a read error is detected, an alternate cylinder may be assigned at this time.

6. RANDOM SEEK/READ TEST
   This test selects a random cylinder, logical unit, and a sector address within the cylinder. The test then reads data and tests for errors. All logical units are used in this test. Alternate cylinders cannot be assigned during this test. The terminal keyboard space (SP) character is used to exit this test.

7. RANDOM SEEK, WRITE, READ, AND COMPARE TEST
   This test selects a random cylinder address and random sector address and writes five sectors (2560 bytes) of random data. The data written is then read into CPU memory and compared for read errors. This test allows

the section of logical units to be tested. The CRT terminal keyboard space (SP) character is used to exit from this test section.

3.3.1 Test and Format Program Details

The program format for different capacity disc drives is identical. The message content varies, particularly in the program header, depending upon the specific disc drive used in the system.

During execution of the first two section of the program a program header is displayed to the operator. The purpose of the header is to define the characteristics of the disc drive used with the system and to verify the setting of Mode switch 4 (S4) located on the controller board.

The header parameters, such as number of logical units, bytes per logical unit, drive model, etc., will be for the specific disc drive for which the software supplied is configured. For example, the program header for a CDC Model 9448-96 CMD is as follows:

```
DQ202 TEST AND FORMAT CMD MODEL 9448-96 DRIVE
THE DRIVE WILL BE FORMATTED AS 6 LOGICAL UNITS (FIXED =
DP0 TO DP4  (REMOVABLE = DP5)
WITH 15.07 MB PER UNIT (29448 RECORD)
SET CONTROLLER MODE SWITCH 4 ON
FORMAT RK0 (Y OR N)?
```

When the last line of the header is displayed sections 1 and 2 of the program will have been executed and section 3 (FORMAT THE DISC) is ready for execution.

3.3.1.1 FORMAT THE DISC PROGRAM SECTION

This program section allows the operator to either sequentially select logical units or to select one or more specific logical units to be formatted. Program messages are presented for formatting in logical unit number sequence, i.e.,:

```
FORMAT DP0 (Y OR N)?
FORMAT DP1 (Y OR N)?
FORMAT DP2 (Y OR N)?
        .
        .
        .
        .
FORMAT DP7 (Y OR N)?
```

To skip over formatting logical units, respond N (no) followed by a carriage return. To format logical units respond Y (yes) followed by a carriage return. Before the yes response causes a logical unit to be formatted, the following message is displayed:

ARE YOU SURE?

This second-level query, which also requires a Y (yes) response to cause program execution, prevents accidentally formatting a previously-formatted logical unit (possibly destroying good data) unless specifically desired.

If for some reason the disc is not in a condition to be formatted (not ready), the system will display the following message:

PROGRAM ADDRESS XXXXXX

Where the "X"'s reference an address in the program listing that contains status bits identifying the problem.

As a trouble shooting aid, following the PROGRAM ADDRESS XXXXXX message are listed **seven controller register mnemonics, the** register addresses, and the contents of the registers. Following the seven-line controller register message, a two-line message is displayed as a visual aid in isolating the specific problem. With this message as a "key" the operator can examine the contents of the registers previously displayed to isolate the exact nature of the failure to format.

The next message will be:

USE PROCEED (P) TO REPEAT TEST
XXXXXX

Where the "X's" are an address in the program after the program address at which the format problem occured.

As a visual indication of the execution of the format routine, the green LED indicator on the controller board will flicker.

When a selected logical unit has been successfully formatted and verified (a four-step process), the following message will be displayed:

DPx FORMAT AND VERIFICATION COMPLETE

Where the "X" is the specific logical unit number that has been formatted and verified.

After the last logical unit requested to be formatted has been formatted and verified, the following message will be displayed:

SEQUENTIAL READ (ALL CYLINDERS AND LOGICAL UNITS)?

This indicates that section 3 of the program has been completed and section 4 can now be executed. Note that during section 3 alternate cylinders may be assigned (see paragraph 3.3.2).

3.3.1.2 SEQUENTIAL READ TEST PROGRAM SECTION

This section tests all cylinders and logical units of the disc(s) in the system and can be performed at any time. If the response to the section 4 message:

SEQUENTIAL READ (ALL CYLINDERS AND LOGICAL UNITS)?

is Y (yes) section 4 will be executed and the contents of the system disc will be read. If the operator response is N (no), section 4 will not be performed and a message indicating that section 5 can be executed will be displayed. Alternate cylinders may be assigned during this section of the test (see paragraph 3.3.2).

3.3.1.3 SELECTED READ TEST PROGRAM SECTION

This section of the test allows selected logical units that have been formatted to be read. The message indicating entry to this section is:

READ DPØ (Y OR N)?

The message format presenting successive logical units to be read is similar to the format in section 3. A response of either N (no) or CR (carriage return) skips over the testing of logical units. Alternate cylinders may be assigned during this test (see paragraph 3.3.2).

The following message indicates the exit from this test section and the entry into section 6:

RANDOM SEEK, READ OF DRIVE (ALL CYLINDERS AND LOGICAL UNITS)?

3.3.1.4 RANDOM SEEK/READ TEST PROGRAM SECTION

This test section selects a random cylinder, random logical unit, and sector and reads 32 consecutive sectors regardless of the first sector selected by the program. If an error occurs during this test, the following message will be displayed:

PROGRAM ADDRESS = XXXXXX

Where the "X's" are the program address at which the program halted. As in test section 3 register mnemonics, register addresses, and register contents are displayed followed by a summary error message.

The summary error message will have the following form:

READ DATA COMMAND
"the error message"
USE PROCEED (P) TO REPEAT TEST (repeats section 6 only)

The keyboard space (SP) character is used to exit this test and proceed to test section 7.

3.3.1.5 RANDOM SEEK, WRITE, READ, AND COMPARE TEST PROGRAM SECTION

This test performs a write, read, and compare of data in a random cylinder and sector of a selected logical unit. The message format presents successive logical units for operator selection as in test section 3. A N (no) response skips to a successive logical unit. A Y (yes) response is followed by the message:

ARE YOU SURE?

This secondary response request attempts to prevent accidentally destroying good data. A Y (yes) response to this message initiates the test. Physical indications of test performance are the blinking of the green LED on the controller board and vibration of the disc unit (indicating random head seeking).

This test can be exited at any time by pressing the space (SP) bar on the terminal after which the message:

USE PROCEED (P) TO REPEAT TEST

If P (proceed) is pressed, the entire 7-section test sequence will be repeated.

NOTE

After executing the test and format program, the operator must re-boot the system

3.3.2 Alternate Cylinder Assignment

During test steps in which alternate cylinders may be assigned, the message:

ASSIGN ALTERNATE CYLINDER?

will appear. The operator response to this message is either Y (yes) or N (no). This allows the operator the option of either logging defective cylinders or selecting alternate cylinders. Seven spare cylinders are always allocated. Disc manufacturers recommend that if more than seven cylinders are defective, the disc should be serviced by factory-trained personnel.

If the operator response to the ASSIGN ALTERNATE CYLINDERS? message is Y (yes), the following sequence automatically occurs:

1. The alternate inner cylinders are accessed.
2. The first alternate cylinder not already assigned is formatted and verified for media quality. If the verification is satisfactory, the alternate cylinder is flagged as an alternate.
3. The known bad cylinder being re-assigned to an alternate cylinder is accessed and in the header of every sector the alternate cylinder address is written.

A successful alternate cylinder assignment causes the following system message to be displayed:

ALTERNATE CYLINDER ASSIGNED

After this message is displayed the next successive test in the test and format program will be displayed. Within a test step, if cylinder allocation is invoked, the test continues with the next successive cylinder after the bad cylinder until all cylinders have been tested and formatted.

During the test program successive innermost cylinders (the allocated spares) are examined for unassigned cylinders. If all spare cylinders have been assigned, the system will display:

NO ALTERNATE CYLINDERS AVAILABLE

After requesting an alternate cylinder assignment, the operator should perform the test over to verify that assignment of the bad cylinder(s) took place.

NOTE

Before assigning bad cylinders to alternates, the operator should make one or more passes through the test and format program to log all bad cylinders. This is a positive test for media flaws and an indication that the disc may need to be serviced. Successive passes through the program should isolate all defects in the disc subsystem.

SECTION 4

PROGRAMMING

4.1 PROGRAMMING DEFINITIONS

Function - The expected activity of the disc system (write, seek, read, etc.).

Command - To initiate a function (halt, clear, go, etc.)

Instruction - One or more orders executed in a prescribed sequence that causes a function to be performed.

Address - The binary code placed in the BDALO-15 lines by the bus master to select a register in a slave device. Note memory other than computer internal memory, i.e., peripheral device registers, the upper 4K (28-32K) address space is used.

Register - An associated group of memory elements that react to a single address and store information (status, control, data) for use by other assemblies of the total computer system. Classically, registers have been made up of groups of flip-flops. More and more often registers are the contents of addressed locations in solid-state or core memory.

4.2 DISC CONTROLLER FUNCTIONS

The disc controller performs 11 functions. A function is initiated by a GO command after the processor has issued a series of instructions that store function-control information into controller registers. To accept a command and perform a function, the controller must be properly addressed and the disc drive(s) must be powered up, be at operational speed, and be ready.

The 11 functions performed by the controller are established by bits 01, 02, and 03 of the control status register (RPCS). The function and bit codings are given in Table 4-1. Descriptions of the functions are given in the following paragraphs.

TABLE 4-1: CONTROLLER FUNCTIONS

The controller functions are specified by bits 01, 02, 03, and 11 of the Control Status (RPCS) register. The bit configurations and functions specified are as follows:

BITS				FUNCTIONS
11	03	02	01	
0	0	0	0	Controller reset
0	0	0	1	Write data
1	0	0	1	Write headers
0	0	1	0	Read Data
1	0	1	0	Read headers
0	0	1	1	Write check
0	1	0	0	Seek
0	1	0	1	Write
1	1	0	1	Write headers only
0	1	1	0	Seek home (restore)
0	1	1	1	Read

4.2.1 Controller Reset

Clears controller logic to initial conditions and terminates data transfers at the end of the sector currently being transferred. This function is entered when the controller is initially cleared or when the function register contents equal 0. If GO is set while the contents of the function register equals zero, CONTROL RESET is generated. The RESET command can be executed even if the controller is in the NOT READY state.

4.2.2 Write Data

The Write Data function includes a Seek to the desired starting disc address (cylinder and track). The function is executed by loading octal code (1) into the Function register and setting GO. Causes the controller to write one or more data records on the addressed disc. Writing starts at the drive, cylinder, head, and sector address specified by the RPCS, RPCA, and RPDA registers. The amount of data written is specified by the RPWC register. Write data transfer start from memory address specified by the RPBA register. Each data word transferred increments the Bus Address and Word Count registers. When the RPWC overflows, data transfers cease on the Bus and the remainder of the present sector is filled with zeroes. As data is written a CRCC is calculated and written as the last word of each sector. Prior to writing, the Header record is read to verify proper head positioning. If the last word specified requests data be written past the last head, cylinder, and sector, the Overflow Error flag (bit 02 or RPER) will be set and the Function will terminate. If the AIE bit is set, this will in turn cause an interrupt.

4.2.3 Write Headers

If the Write Data and the Header bits are set, the Write Headers function is initiated when GO is set. This function causes the controller to write a three-word header, which is used by the controller when either writing or reading data to determine:

a. Cylinder address
b. Head address
c. Sector address
d. Flags

Controller board switch S3 must be OFF to perform this function.

4.2.4 Read Data

Causes the controller to read one or more data records from the disc drive. The Read function includes a Seek to the starting disc address (cylinder, head, sector) and is initiated by loading octal code (2) into the Function register and setting GO. Data transfers from the disc are stored in memory starting with the memory address specified by the RPBA register. Each data word transferred increments the Bus Address and Word Count registers. The contents of the RPWC at the beginning of the transfer specify the number of words to be transferred. When the RPWC overflows, data transfers stop. The remainder of the present sector is read and parity checked before the DONE flag is set.

Attempts to read beyond the last sector and head of the last cylinder of a disc will generate the OVERFLOW ERROR (bit 02 of RPER) flag and terminate the operation.

While data is being read, the controller calculates a CRC. At the end of the sector, the calculated CRC is compared with the CRC read from the sector. If they disagree, the CheckSum Error (CSME of RPER) bit sets.

Note that if controller Switch 2 is OFF, the controller will perform three read retries before the CSME error flag is set.

Prior to reading the data record the header record is read to verify proper head position.

4.2.5 Read Headers

If the read data and the header bits are set, the Read Headers function is initiated when GO is set. This function causes the controller to read all headers starting at the Index mark. Each 3-word header is read in the order in which it appears on the disc. If a CRC error is detected in the header, bit 7 in the flag byte of the header record is set as well as the CSME bit of RPER.

4.2.6 Write Check

The Write Check function includes a Seek to the starting disc address (cylinder, head, sector). This function is a combination of the Write and Read functions. Data words are transferred from memory to the controller and simultaneously read from the disc drive and transferred to the controller. The two words read are compared in the controller. Discrepancies set the WCE bit in RPER to cause an appropriate interrupt. Data remains unchanged in both the memory and the disc.

If the data transfer is sufficiently large as to exceed the disc head, cylinder, and sector boundaries, the Overflow Error flag bit will be set and the function will terminate. If the AIE bit is set, this will in turn cause an interrupt.

4.2.7 Seek

The Seek function is responded to by the controller if octal code (4) is loaded in the Function register and GO is set; all the proper responses are made to the RP02 handler by the controller to indicate the proper completion of this function, seek complete interrupt, etc.. However, the controller does not actually issue a seek command to the disc drive. This function was originally implemented when each physical disc drive was one logical unit. Now that multiple logical units are in one physical drive, the function is no longer practical. Furthermore, all Read and Write functions include automatic seeks.

4.2.8 Write

This Write function is identical to the other Write Data function (octal code(1)). An automatic seek is performed to the address specified in the RPCA and RPDA registers.

If the data transfer is sufficiently large to exceed the disc head, cylinder, and sector boundaries, the Overflow Error flag bit will be set then the function will terminate. If the AIE bit is set, this will in turn cause an interrupt.

4.2.9 Write Headers Only

Loading the Function register with the bit configuration for the Write Headers Only function and setting GO permits the headers to be re-written without disturbing the data records. This is a method of setting invidivual flag bits on a sector basis.

4.2.10 Seek Home

The Seek Home function is executed by loading its function into the Function register and setting GO. This function restores the head carriage assembly to cylinder 000_8 and the Unit Attention is set with Selected Unit Ready.

This function is used to recover from a Selected Unit Seek Incomplete.

4.2.11 Read

This function is identical to the other Read Data function (octal code(2)). An automatic seek is performed to the address specified in the RPCA and RPDA registers.

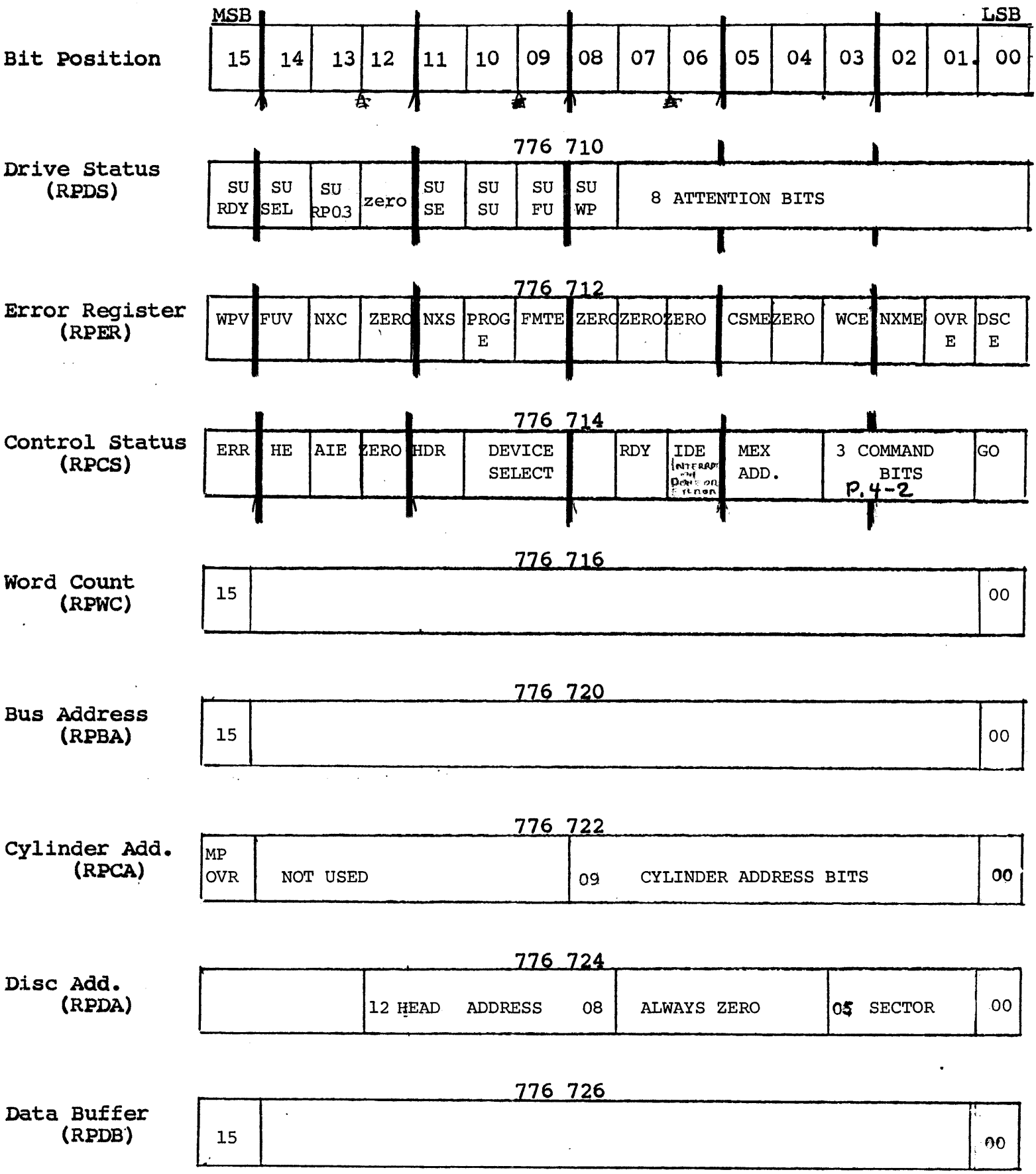


Figure 4-1: Controller Register Configurations

If the data transfer is sufficiently large to exceed the disc head, cylinder, and sector boundaries, the Overflow Error flag bit will be set and the function will terminate. If the AIE bit is set, this will in turn cause an interrupt.

4.3 CONTROLLER REGISTERS

All software interaction between the disc controller, the processor, and the processor memory is accomplished by eight registers in the disc controller. These registers are assigned memory addresses and can be read or written into (except as noted) by instructions that reference respective register addresses. The eight controller registers, their addresses, their mnemonics, and their bit assignments are shown in Figure 4-1.

4.3.1 Drive Status Register (RPDS)

The address of RPDS Is 776 710. RPDS is a read only register except that the eight attention bits can be selectively cleared by moving a 1 to the desired bit location(s). In most cases, the controller will be connected to only one disc drive, which will contain one or more logical units (emulating the RP02 physical units).

The significance of the bits of RPDS is as follows:

BIT(s)	DEFINITIONS
00-07	ATTENTION BITS -- Always zero.
08	SELECTED UNIT WRITE PROTECTED -- Sets when the selected disc is write protected.
09	DRIVE FAULT (UNSAFE) -- Sets if an error condition is detected within the drive and is prohibiting all operations. This bit is reset manually by clearing the fault condition within the drive.
10	SELECTED UNIT SEEK UNDERWAY -- Sets after a seek has been initiated and is reset after completion of the seek.
11	SELECTED UNIT SEEK ERROR -- Sets if a seek is not completed within 100 milliseconds after it was initiated.
12	ALWAYS SET TO A ZERO.
13	Selected unit RP03. Reset when unit is RP02.
14	SELECTED UNIT SELECTED -- Sets when the drive has been selected and is on line.
15	SELECTED UNIT READY -- Sets after a successful seek operation. It is reset during any seek operation and set again after seek is completed.

4.3.2 Error Register (RPER)

The address of RPER is 776 712. This register contains all error conditions generated within the controller. RPER is a read only register. This register is cleared when the GO bit is set in RPCS.

The significance of the bits of RPER is as follows:

BIT(s)	DEFINITIONS
00	DISC ERROR -- The OR condition of header has not been found and the selected unit seek is incomplete. Reset by INIT or RESET functions.
01	OVERFLOW ERROR -- Sets if a data transfer (read or write) is attempted across the end of the last sector of the drive. Reset by INIT or RESET functions.
02	NON-EXISTENT MEMORY -- More than 10 microseconds were required to complete a Q-Bus transaction. Reset by INIT or RESET functions.
03	WRITE CHECK ERROR -- Data read from the drive does not compare with the data read from memory during the Write Check function. Reset by INIT or RESET functions.
04	ALWAYS ZERO.
05	CHECKSUM ERROR -- Calculated checksum does not compare with that read from the drive. Reset by INIT or RESET functions.
06,07,08	ALWAYS ZERO
09	FORMAT ERROR -- Sets if a parity error was detected in a sector's header record. Reset by INIT or RESET functions.
10	PROGRAM ERROR -- Data transfer operation was attempted with the contents of the RPWC equal to zero, or an operation was attempted on an off-line drive, or while another instruction was still in progress. Reset by INIT or RESET functions.

BIT(s)	DEFINITIONS
11	NON-EXISTENT SECTOR -- Operation was attempted when the contents of the Sector Address register was not within the 0--- range. Reset by INIT or RESET functions.
12	ALWAYS ZERO.
13	NON-EXISTENT CYLINDER -- Operation was attempted when the contents of the Cylinder Address register was not within the 0-404 range. Reset by INIT or RESET functions.
14	FILE UNSAFE VIOLATION -- Operation was attempted while the SUFU (bit 09 of RPDS) was set. Reset by INIT or RESET functions.
15.	WRITE PROTECT VIOLATION -- Operation was attempted when the SUWP (bit 08 of RPDS) was set. Reset by INIT or RESET functions.

4.3.3 Control Status Register (RPCS)

The address of PRCS is 776 714. The bit configuration loaded into this register initiates and controls a disc function. All bits of this register are read/write unless otherwise indicated.

The significance of the bits of RPCS is as follows:

BIT(s)	DEFINITIONS
00	GO -- When set causes the controller to initiate the operation encoded in bits 01-03 of RPCS. This is a write only bit always read as a zero.
01-03	COMMAND BITS -- These bits are also referred to as function bits and specify the operation to be performed. These bits are described in Table 4-1. These are read/write bits, cleared by INIT or RESET functions. P.4-2
04-05	MEMORY EXTENDED ADDRESS -- Extended bus address bits for systems with memory larger than 32K 16-bit words. Used in conjunction with the RPBA register. These bits increment each time RPBA overflows. These are read/write bits cleared by INIT or RESET functions.
06	INTERRUPT ON DONE (ERROR) ENABLE -- Causes the controller to raise an interrupt request when either a disc operation is complete or if an error occurs. This read/write bit is cleared by INIT or RESET functions.
07	READY -- Indicates the controller is in a condition to accept and execute a new operation. This is a read only bit.
08-10	DEVICE SELECT -- Specifies one of eight logical units which are to be the subject of any controller action. These read/write bits are cleared by INIT or RESET functions.

BIT(s)	DEFINITIONS
11	HEADER -- Used in conjunction with the function bits specifying read or write operations. It is primarily used to format a new disc or re-format a disc erased due to a controller or drive failure. This read/write bit is cleared by INIT or RESET functions. The write format function causes a header record to be written in each sector. The header record contains three words obtained from a table in computer memory. These three words are read from the disc by the controller to determine sector number (address verification) and sector size (soft sector format). A write header function starts at the Index and continues to write to the next Index. The headers are recorded in the order in which they are stored in the write table in memory. The controller properly spaces the sectors around the tracks of the disc. The read header function reads all header records on one disc surface starting at the Index. The headers are read and stored in memory in the order in which they appear on the disc. Bit 07 of the Flag byte will be set only in computer memory if a CRC error is detected when the header record is read. If a CRC error is detected in the header record, the FMTE bit in RPER is set. The Write Header Only function does not erase the data fields but writes header fields only. Thus, this function is used to set the write protect bit and to mark a sector bad.
12	ALWAYS ZERO.
13	ATTENTION INTERRUPT ENABLE -- Causes the controller to raise an interrupt request whenever any disc raises its Attention line. Cleared at the completion of the interrupt, by INIT or RESET functions. This is a read/write bit.

BIT(s)	DEFINITIONS
14	HARD ERROR -- The OR of all errors except data error. This is a read only bit.
15	ERROR -- The OR of all errors. This is a read only bit.

NOTE
The controller device handler software must include routines that test the ERR and the HE flags to validate the current operation before proceeding.

4.3.4 Word Count Register (RPWC)

The address of RPWC is 776 716. This is a read/write register. The bits of this register contain the 2's complement of the total number of words to be transferred during a read, write, or write check operation. The register is incremented by one after each transfer. When the register overflows (all WC bits go to zero), the transfer is complete and controller action is terminated at the end of the present disc sector. Only the number of words specified in the RPWC are transferred. Cleared by INIT or RESET functions.

4.3.5 Bus Address Register (RPBA)

The address of RPBA is 776 720. The bits of this register contain the bus address of data transferred during read, write, or write check operations. The register is incremented by two at the end of each transfer. If the system has extended memory, the RPBA will overflow to the EX MEM bits (04,05) of the RPCS to reflect the extended bus address. This is a read/write register cleared by INIT or RESET functions.

4.3.6 Cylinder Address Register (RPCA)

The address of RPCA is 776 722. Bits 00-08 contain the binary representation of the disc cylinder to be used for any disc operation. Bits 00-08 are read/write bits cleared by INIT or RESET functions.

Bit 15 is a MAP OVERRIDE bit. This bit can be set by the programmer to override the controller mapping algorithm. When set, the head, cylinder, and sector addresses supplied to the controller specify absolute addresses to the disc. Could be typically used to permit the RP02 device handler to be modified to take advantage of the head per track options available in some disc drives. This bit is always set during the initialize portion of the format routine. Cleared by INIT or RESET functions. Bits 09-14 are not used.

4.3.7 Disc Address Register (RPDA)

The address of RPDA is 776 724. The bits or this register are read/write bits cleared by INIT or RESET functions.

The significance of the bits of this register is as follows:

BIT(s)	DEFINITIONS
00-03	SECTOR ADDRESS -- Specifies the disc sector to be used for any operation other than Seek Home (Restore). Cleared by INIT or RESET functions.
04-07	ALWAYS ZERO.
08-12	HEAD ADDRESS -- Specifies the head (surface) of the disc to be used for the next operation. Cleared by INIT or RESET functions.
13-15	NOT USED.

4.3.8 Data Buffer Register (RPDB)

The address of RPDB is 776 726. This is a read/write register cleared by INIT or RESET functions. This register functions as a general purpose data handler.

4.4 INITIALIZING, FORMATTING A DISC

When a disc drive is first added to a system or a new disc pack is to be used, the unit must be initialized by a format routine. The format routine is initiated to the controller by RPCS function bits 01, 02, and 03 set to 1, 0, 0 respectively with RPCS bit 11 set to a 1.

The controller then performs a two-pass format operation. During pass one all zeroes are written to the disc to "wipe the disc clean". During the second pass, headers only are written on the disc (data fields left blank) from index point to index point. With reference to Figure 1-3, the only information required from the computer is the following three words for each header:

a. Word 1: Flag byte and Sector-size byte
b. Word 2: Cylinder address
c. Word 3: Head address byte and Sector addresd

These three words for each header must be stored in a write headers table in computer memory. Based upon the sector-size byte, the controller properly spaces the sectors around the peripheral of the disc track. The bits of the three words in the write headers table are defined in the following paragraphs.

4.4.1 Flag Byte

The high byte of header word one is called the Flag byte and has the following configuration

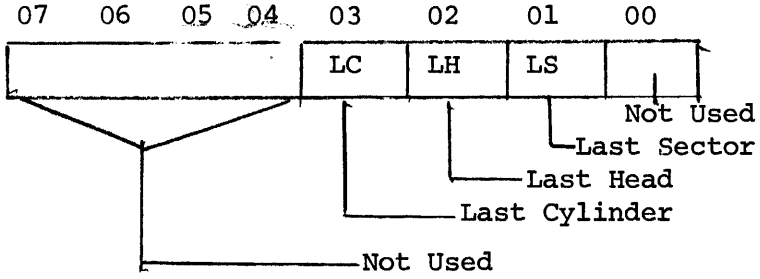


Figure 4-2: Flag Byte Bit Assignment

4.4.1.1 Last Sector - Specifies that this is the last numerical sector of a track and that a new track (surface) must be selected by the controller in a sequential read or write across track/cylinder boundaries situation.

4.4.1.2 Last Head - Specifies that this is the last head in a cylinder and that if this is also the last sector, a seek command must be instituted by the controller during a read or write across surface/cylinder boundaries.

4.4.1.3 Last Cylinder - Specifies that this is the last cylinder in a disc drive. If this is also the last sector of the last head of the last cylinder, the controller recognizes this and prevents accesses beyond this point to protect the disc head carriage from possible damage.

4.4.2 Cylinder Address Word

Ten bits (00-09) are allowed for the cylinder address. This permits 1024 cylinders to be specified.

4.4.3 Head Address Byte

Five bits of the head address byte identify the surface being accessed. This permits a maximum of 16 heads to be accessed and a distinction made between the fixed and removable heads in a CMD-type drive.

The head address from the disc must match the head address specified during a read, write-check, or write function or the function will be aborted.

4.4.4 Sector Address Byte

Six bits are allowed for sector addressing permitting a maximum of 64 sectors to be specified. The two bits over and above the required four bits required for RP02 compatibility are used by the MAP override mode during formatting (mapping) the disc.

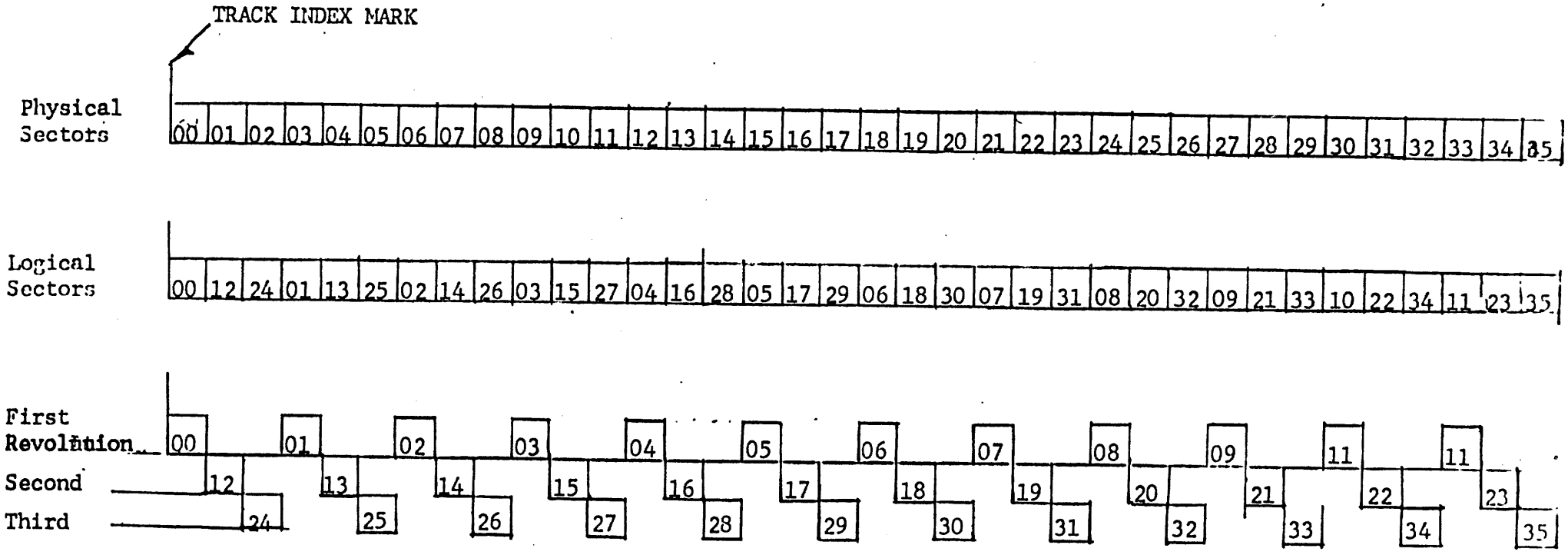
4.4.5 CRC Byte

This byte is the algerbraic sum of all seven bytes in the header. It is the means by which the correctness of the header is verified during reading. An incorrect CRC byte comparison in the header record causes both the bad sector bit and the check sum error bit to be set in RPER. Also, during a read format function, an incorrect CRC causes the bad sector bit in word 1 of the header record to be set.

4.5 INTERLACING

Interlacing is the technique used to match the transfer rate of the discs to the transfer rate of the computer. The data transfer rate of the disc is typically 1.2 megabytes per second (600 kilowords per second). The transfer rate via the DMA facility of the LSI-11 is approximately 500,000 16-bit words per second.

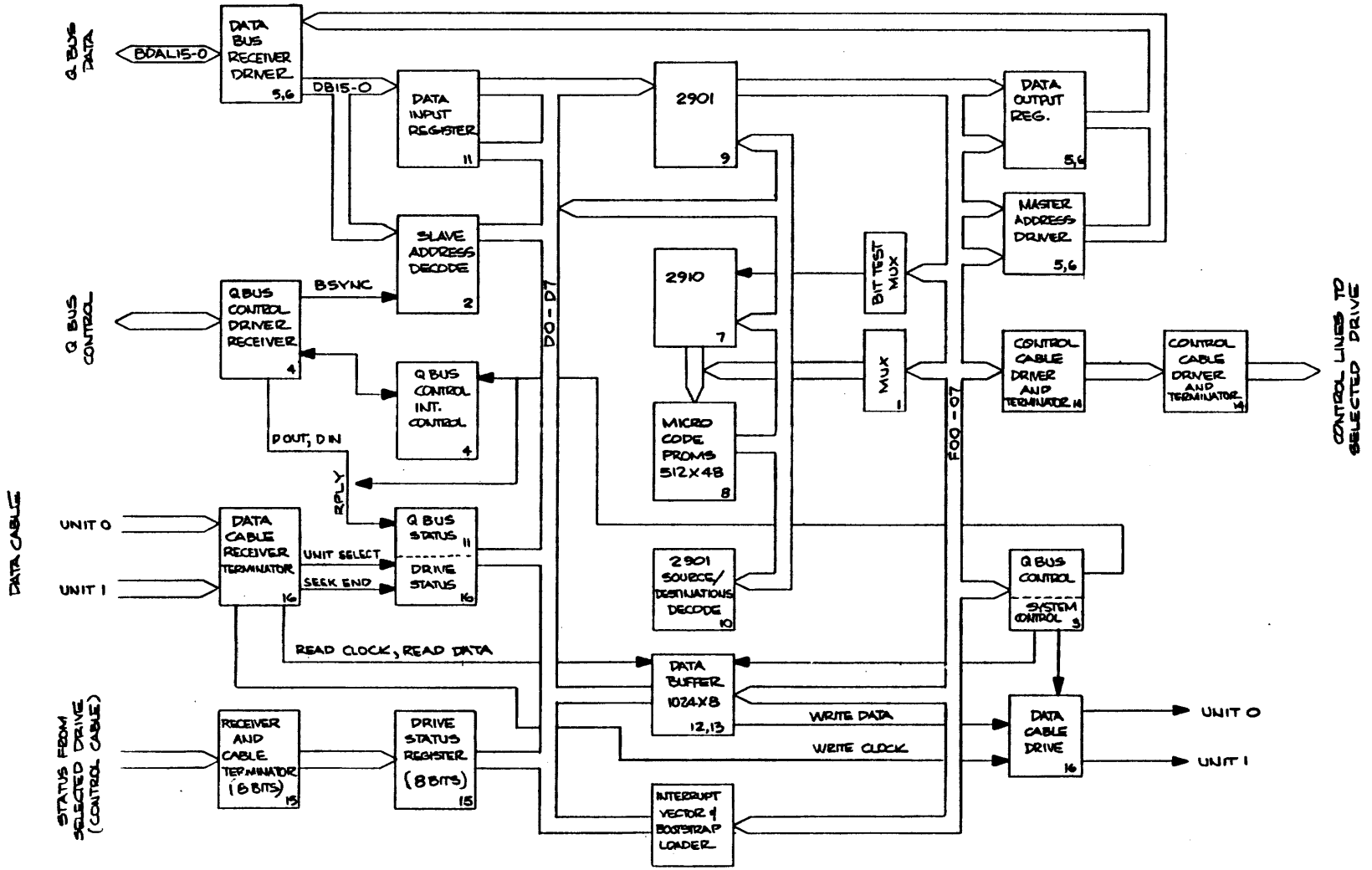
To match this difference in transfer rates, first full sector buffers are contained in the controller, second data records are interlaced on the tracks of the disc. Figure 4-3 illustrates a 3:1 interface for a typical SMD-type disc with 36 sectors per track and rotating at 3600 RPM.



1. Disc speed=3600 RPM
2. Sector size=512 bytes per sector
3. Each disc revolution reads or writes 12 consecutive logical sectors.
   In the above example, one revolution would be lost going from logical sector 35 to logical sector 00.

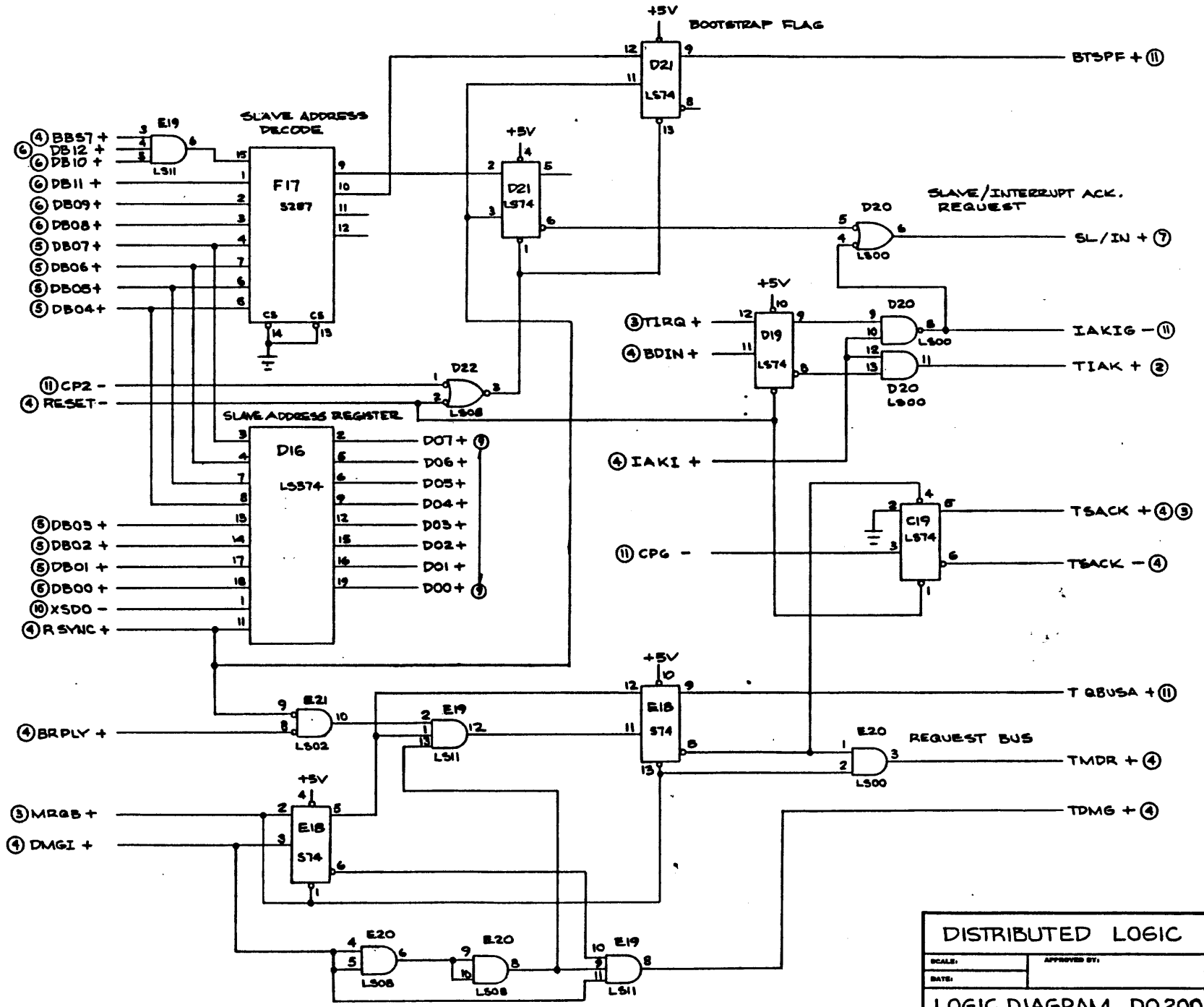
Figure 4-3 : Sector Relationships for a 3:1 Interlace

DRAWINGS AND SCHEMATICS

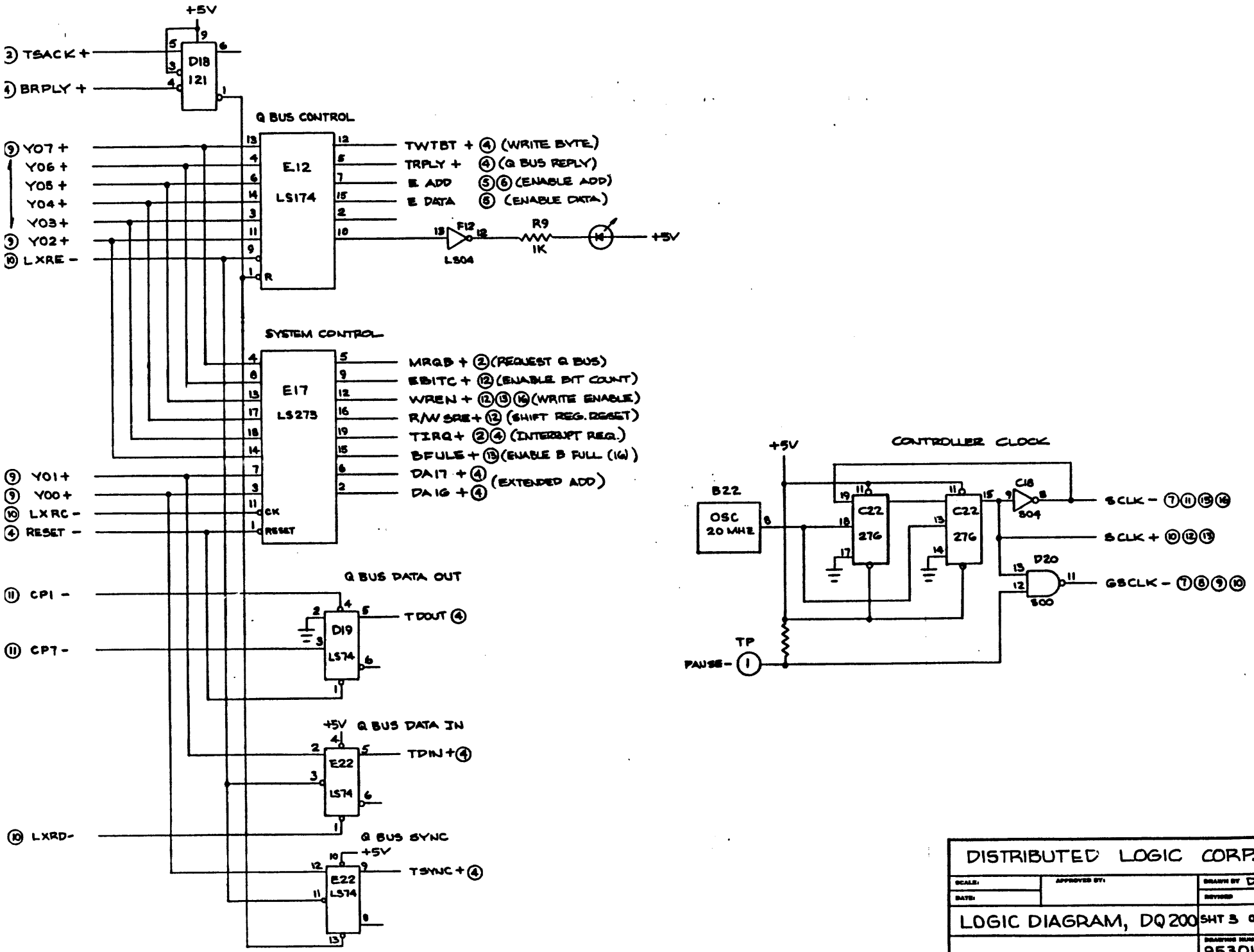


DISTRIBUTED LOGIC CORP.

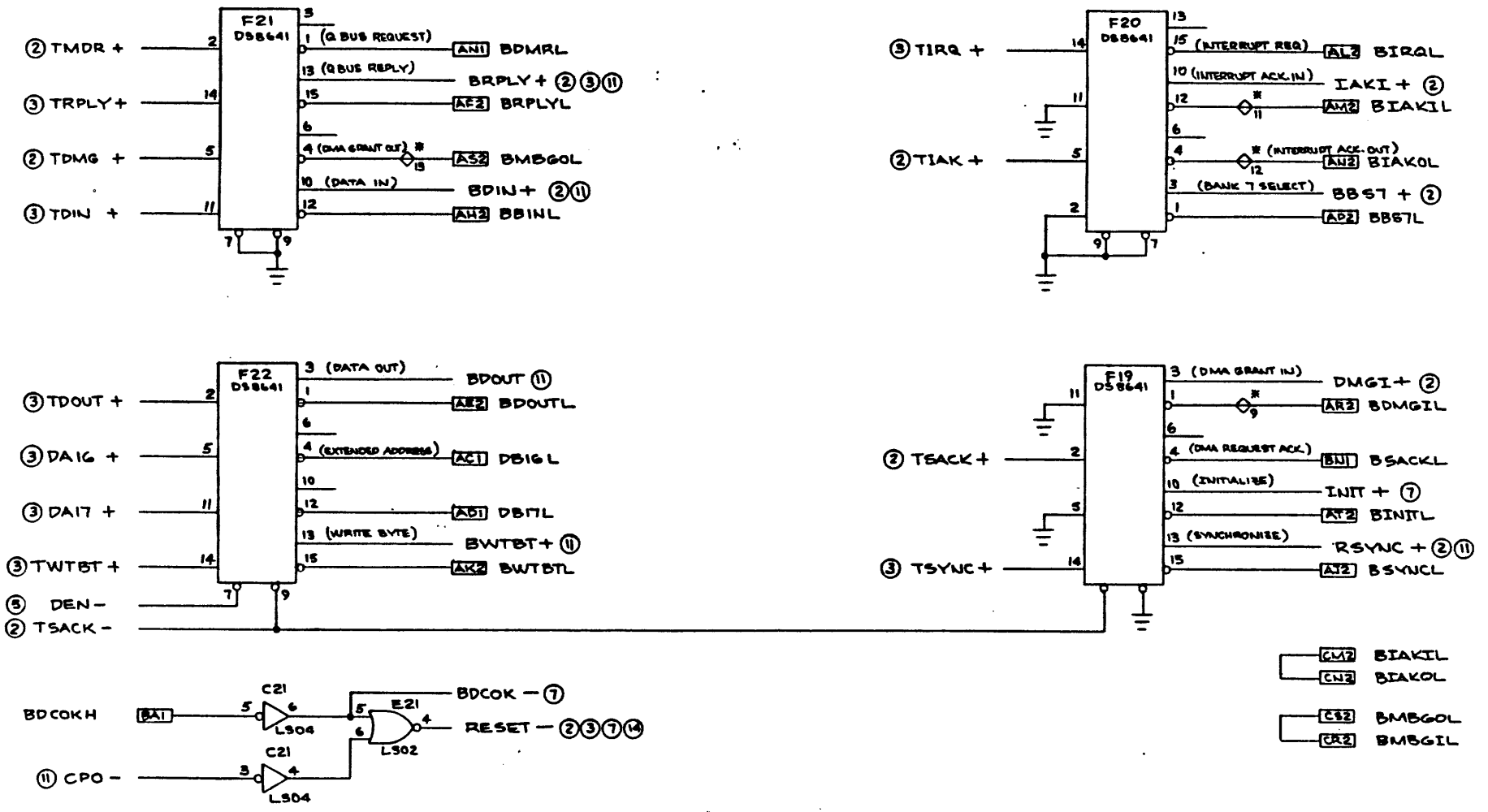
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ200		SHT 1 OF 16
		DRAWING NUMBER 953015



DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ200		SHT 2 OF 16
		DRAWING NUMBER 953015

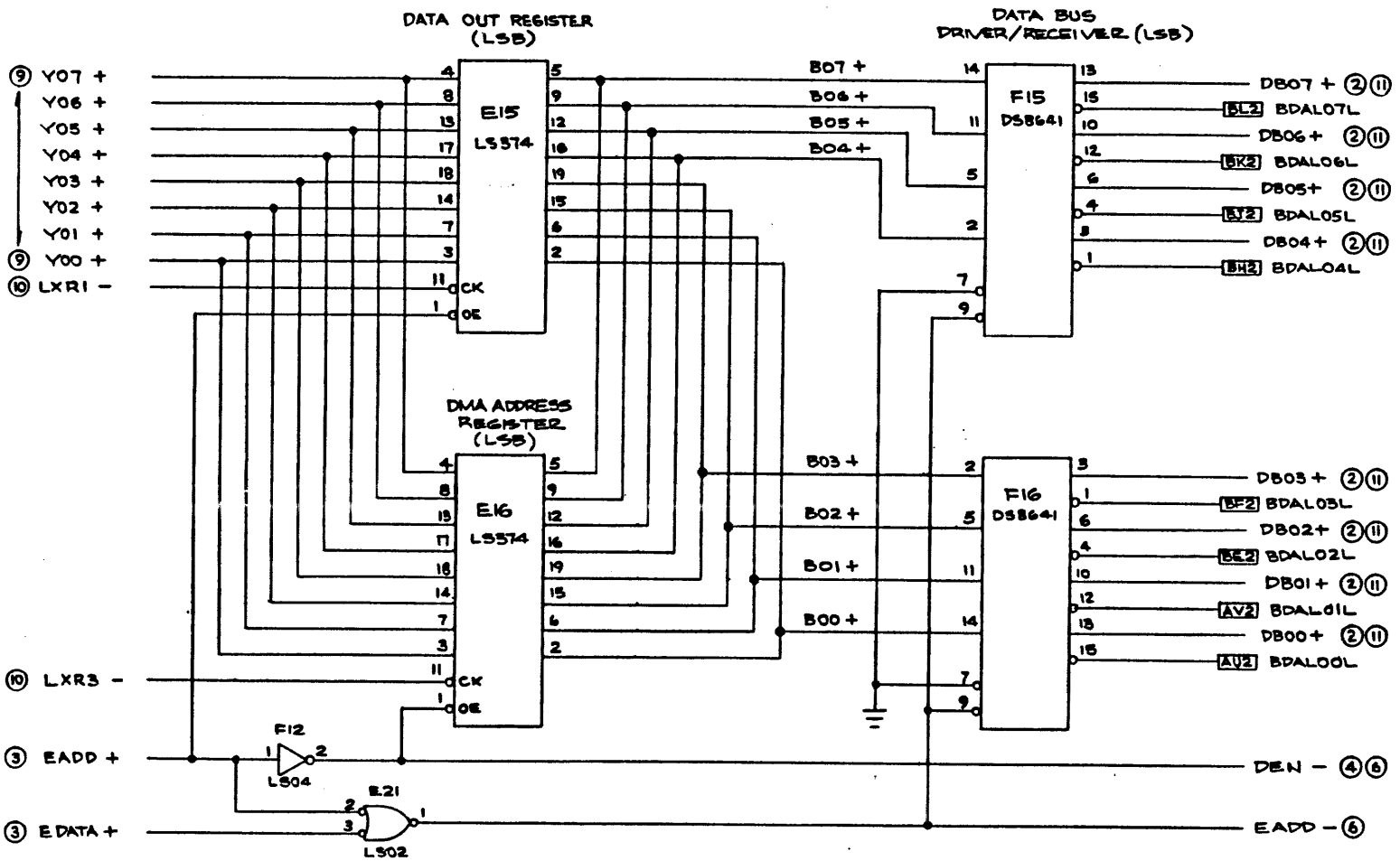


DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ200		SHT 3 OF 16
		DRAWING NUMBER 953015

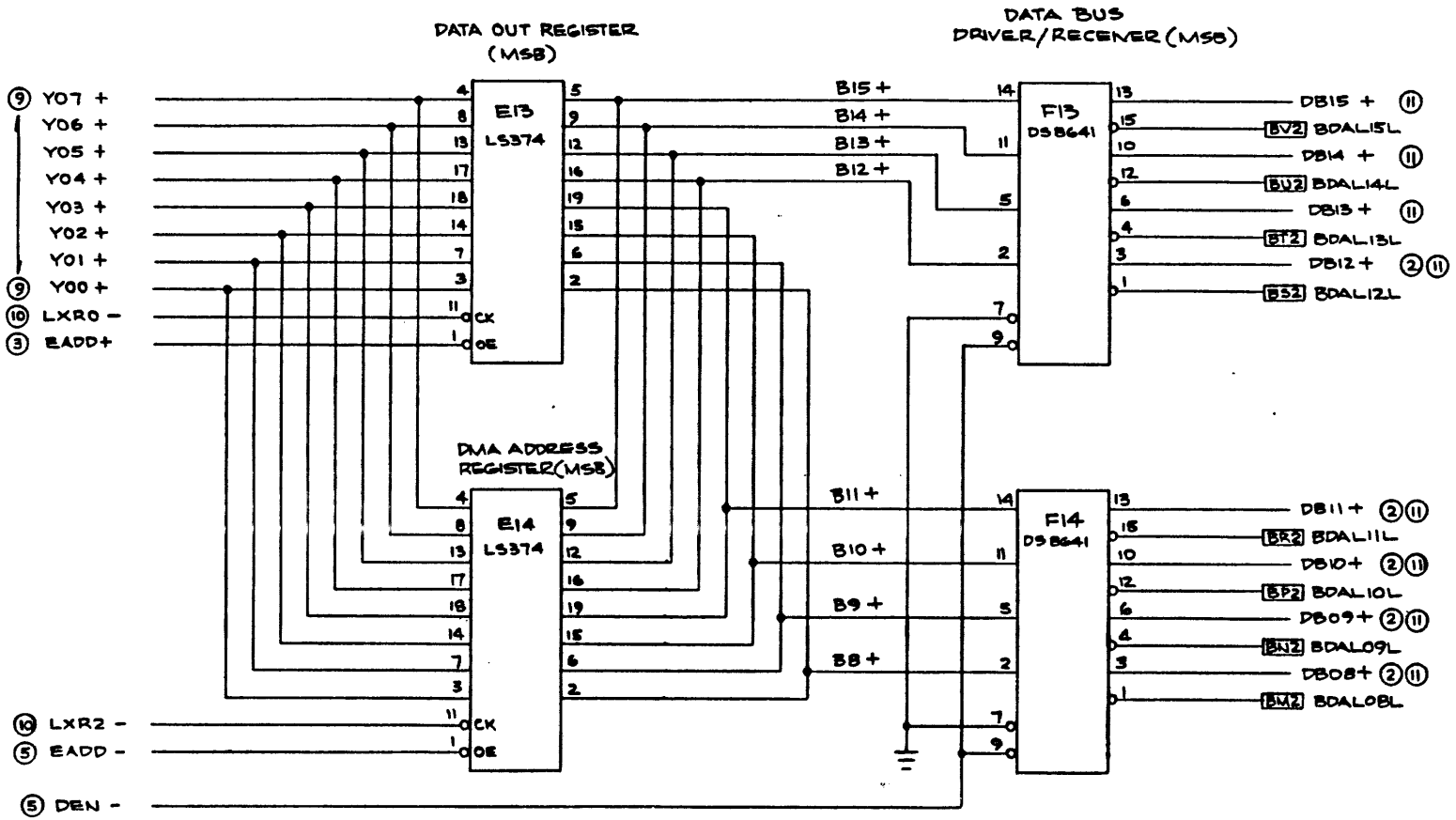


NOTE: * ◇—12 SYMBOL INDICATES PULL-UP(180Ω)/PULL-DOWN(390Ω) RESISTORS. NUMBER SHOWN IS PIN NUMBER USED IN PACK, LOCATION F18.

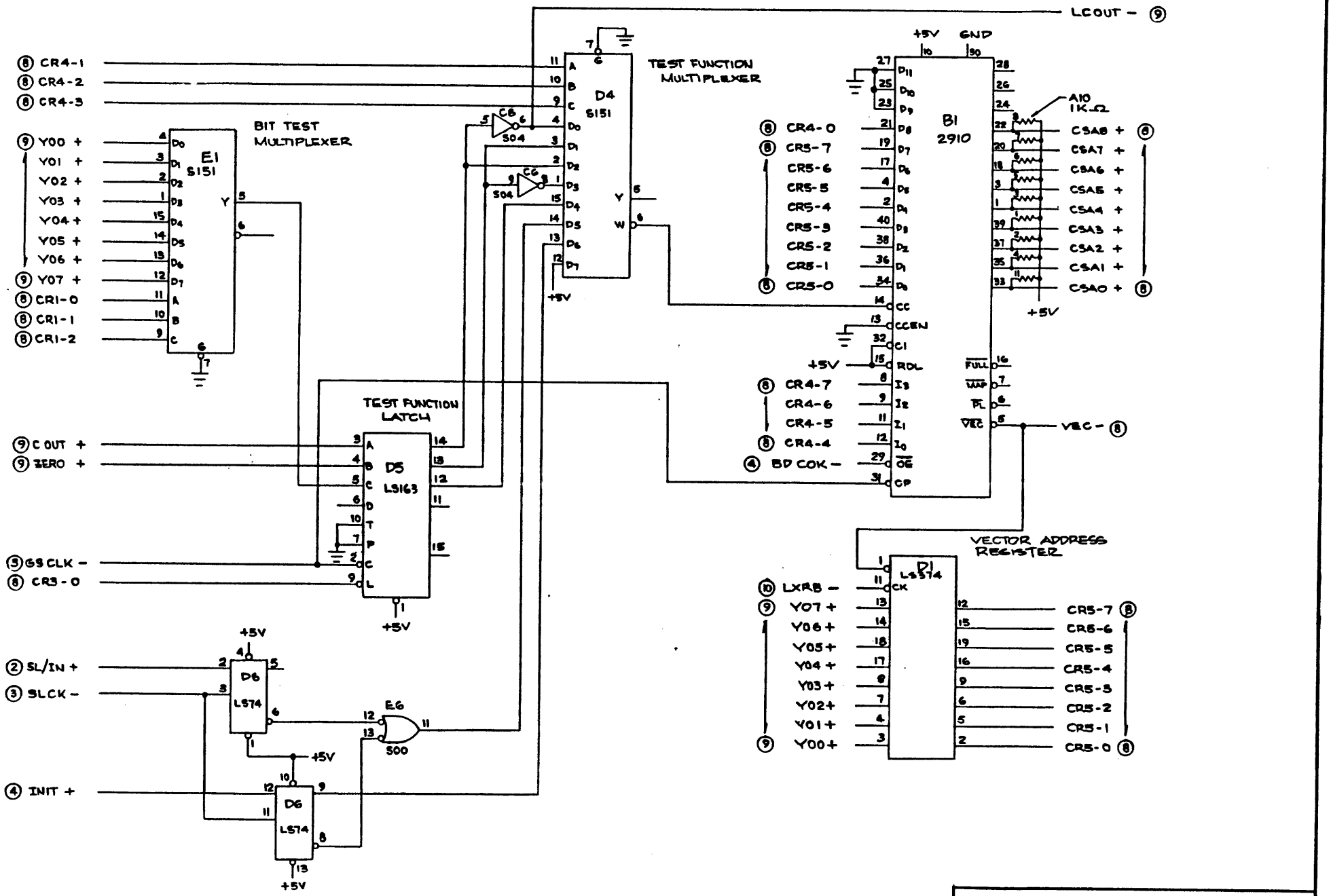
DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ200		SHT 4 OF 16
		DRAWING NUMBER 953015



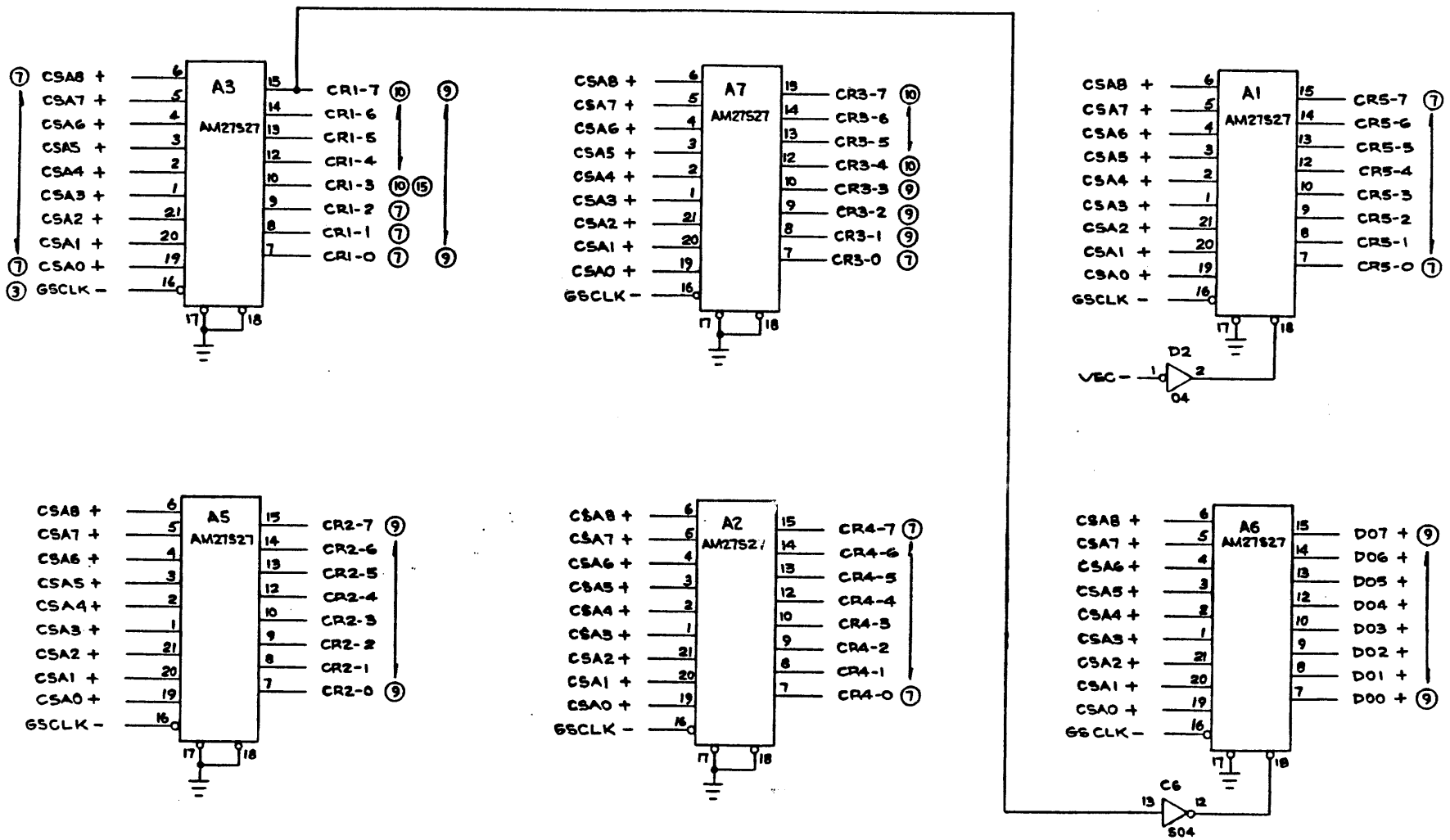
DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ200		SHT 5 OF 16
		DRAWING NUMBER 953015



DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ200		SHT 6 OF 16
		DRAWING NUMBER 953015

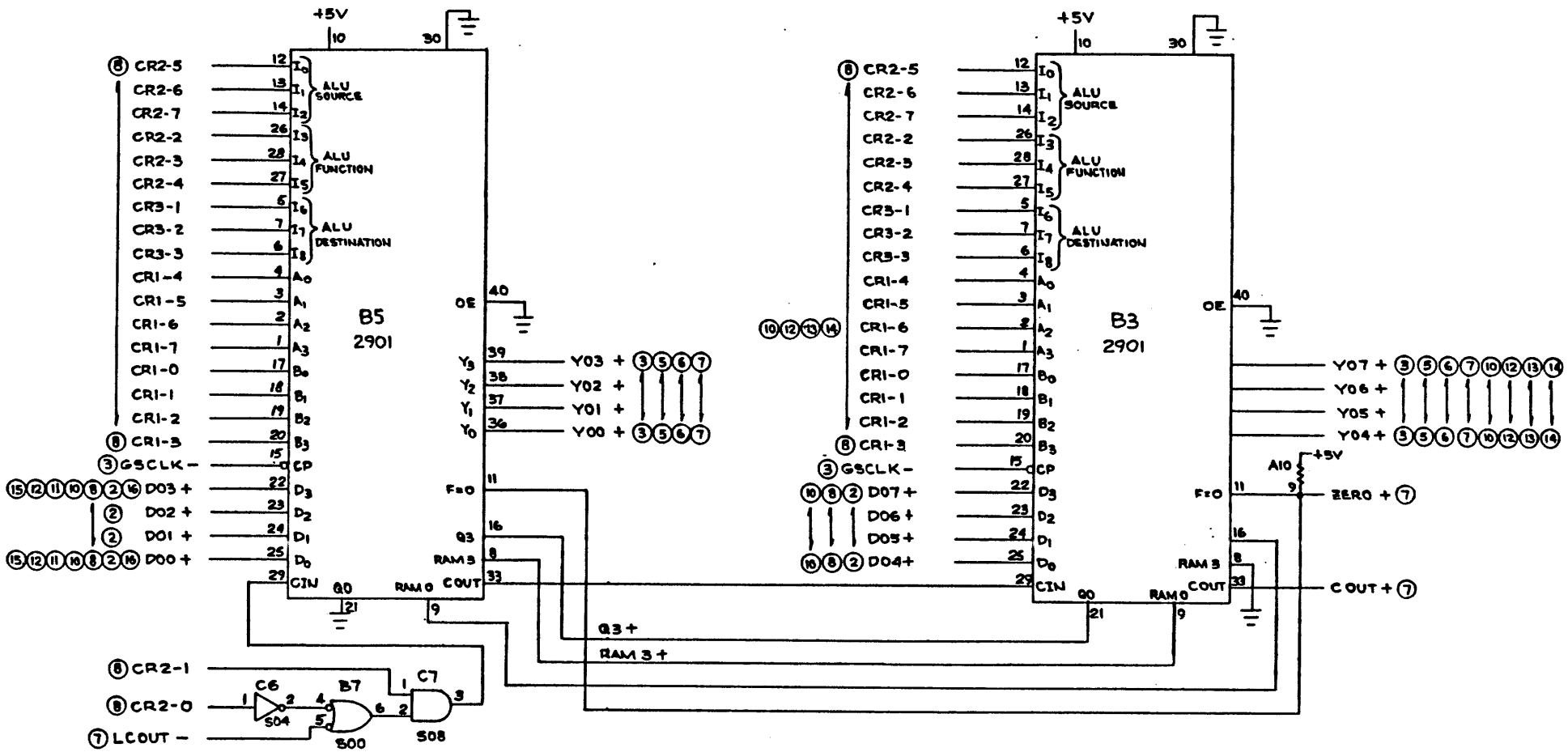


DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ200		SHT 7 OF 16
		DRAWING NUMBER 953015



DISTRIBUTED LOGIC CORP.

SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ200		SHT 8 OF 16
		DRAWING NUMBER 953015



DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
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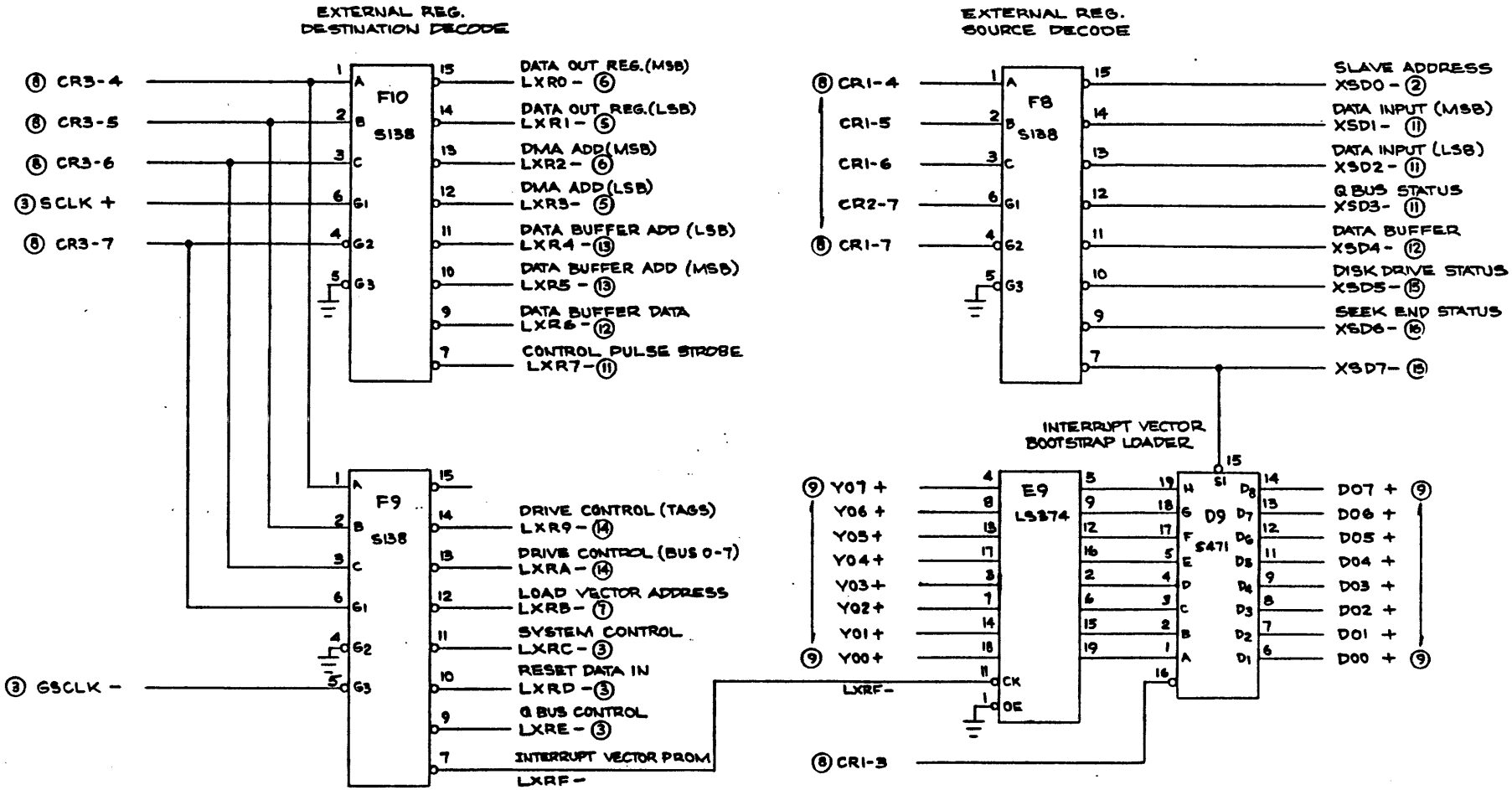
LOGIC DIAGRAM, DQ 200		SHT 9 OF 16
		DRAWING NUMBER 953015



DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
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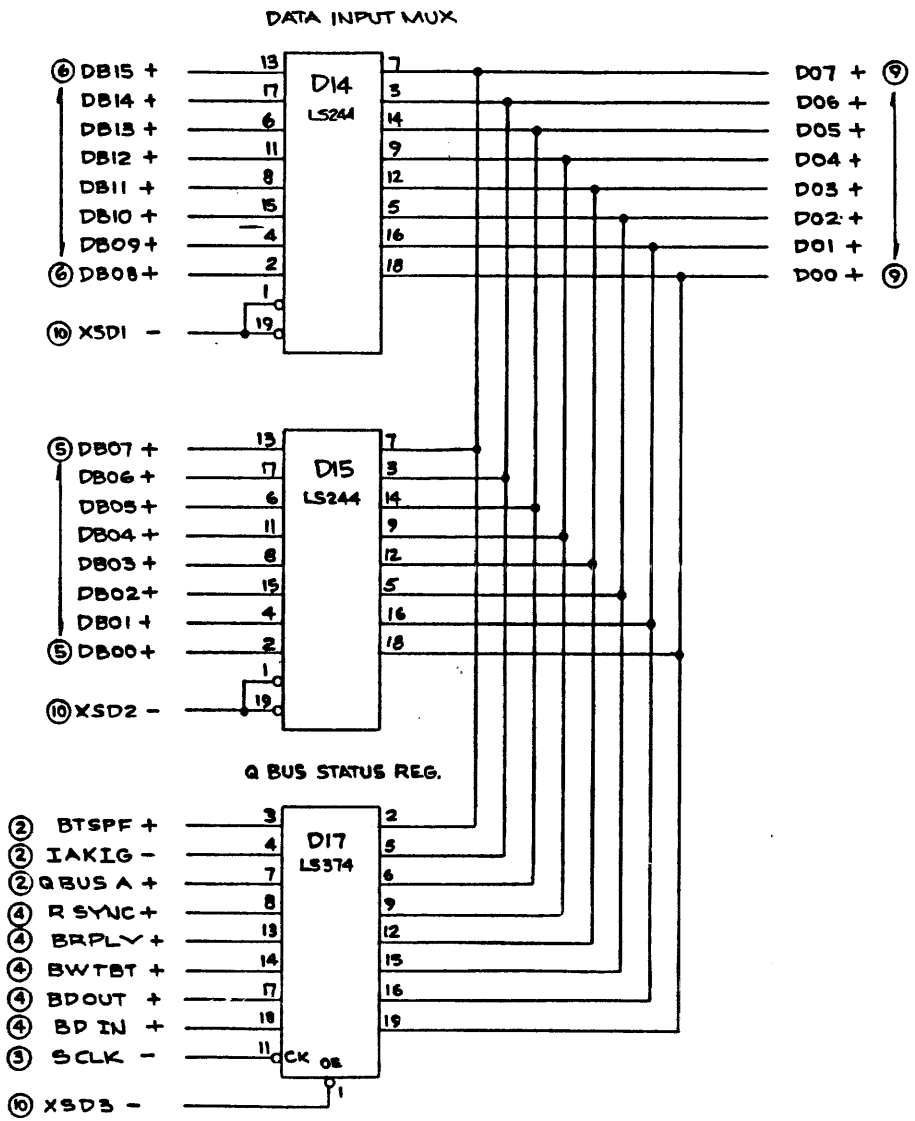
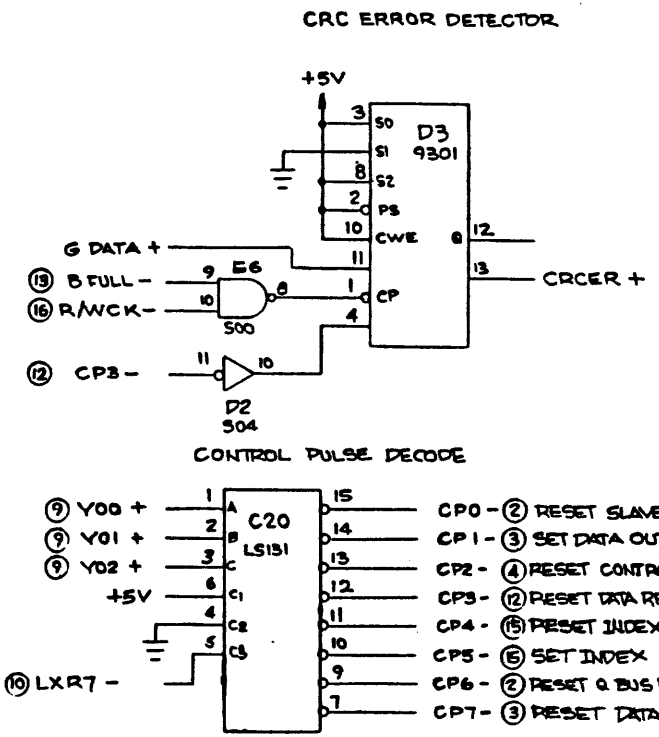
LOGIC DIAGRAM, DQ200		SHT 10 OF 16
		DRAWING NUMBER 953015





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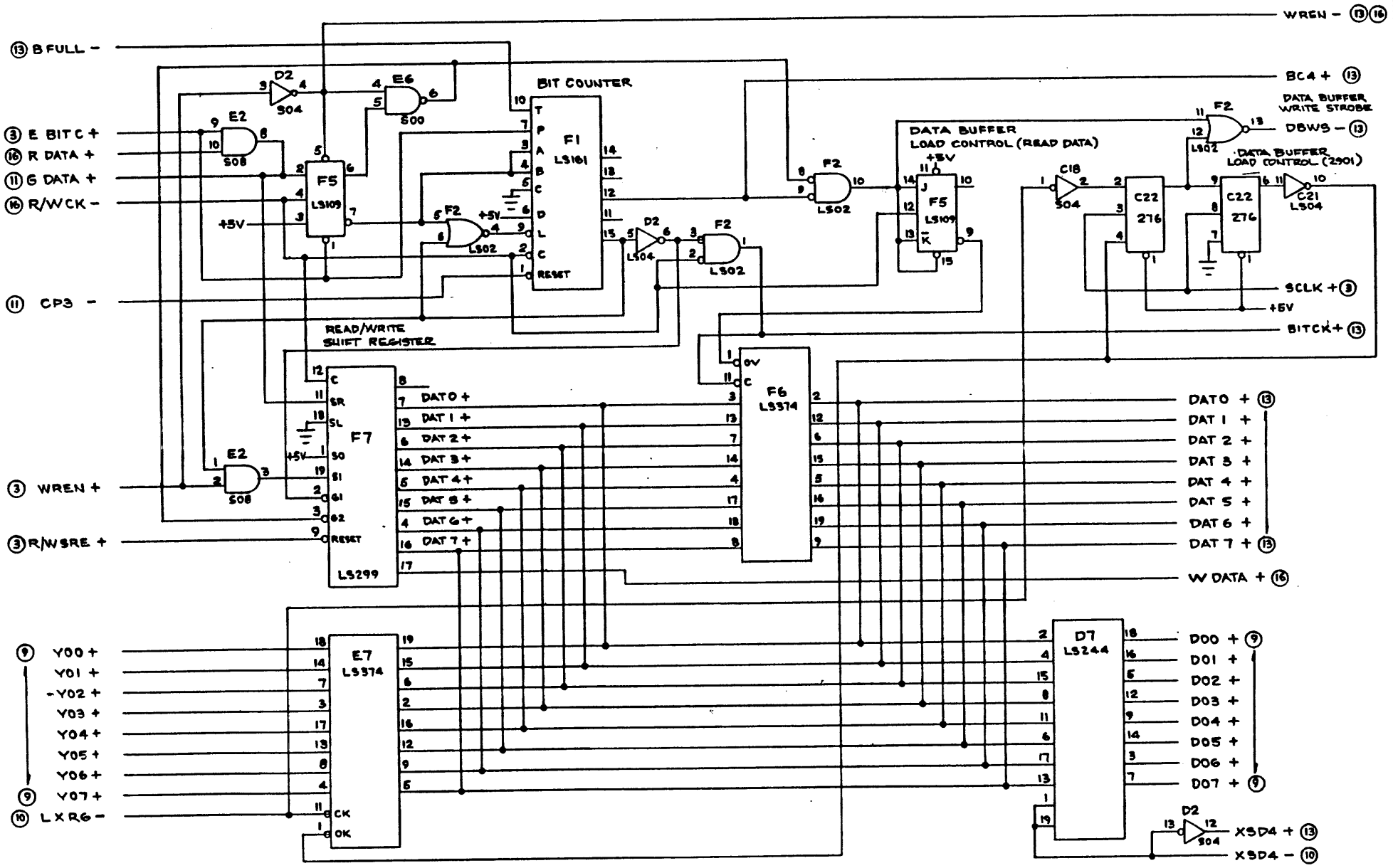
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ200		SHT 11 OF 16
		DRAWING NUMBER 953015



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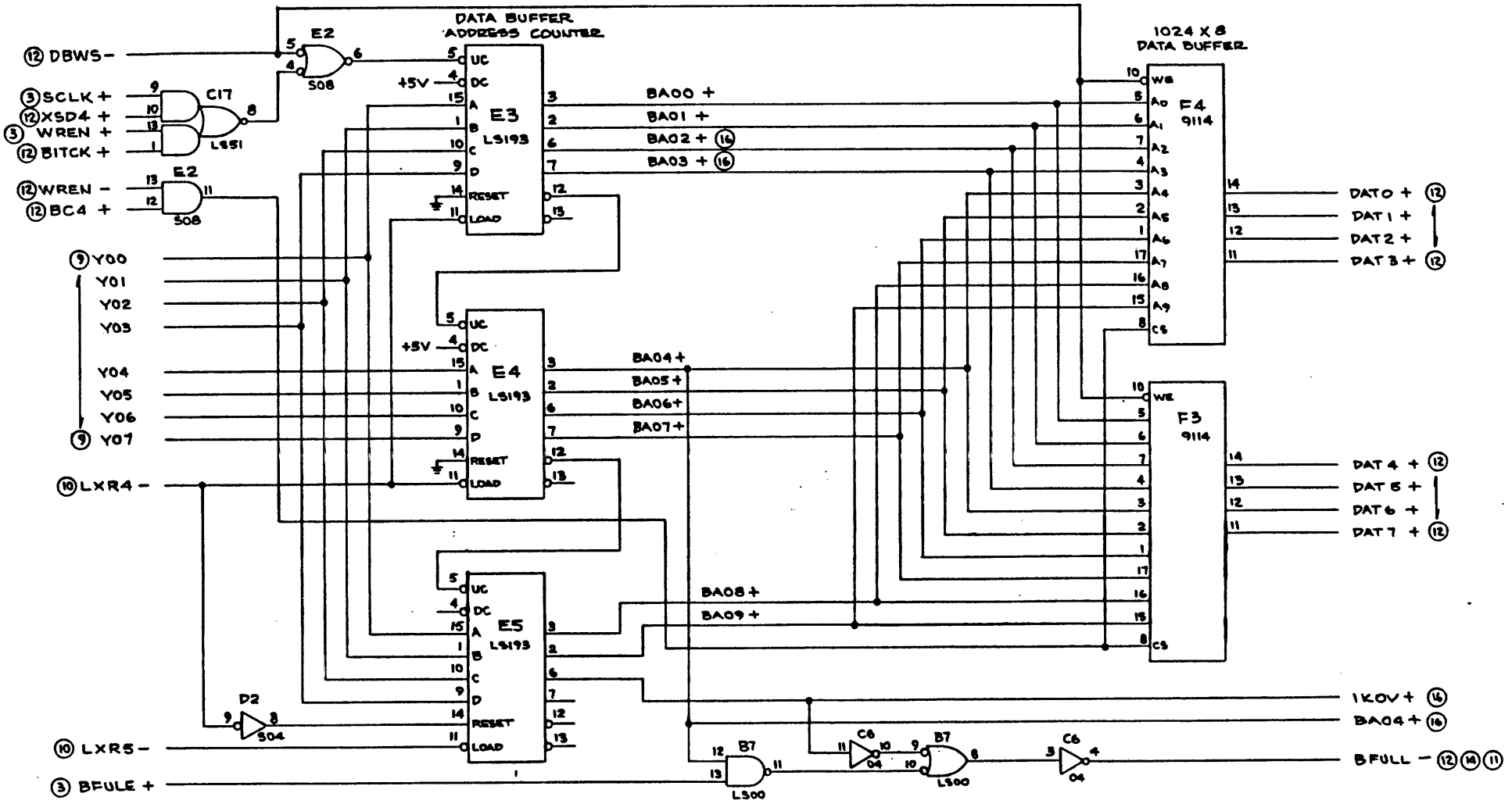
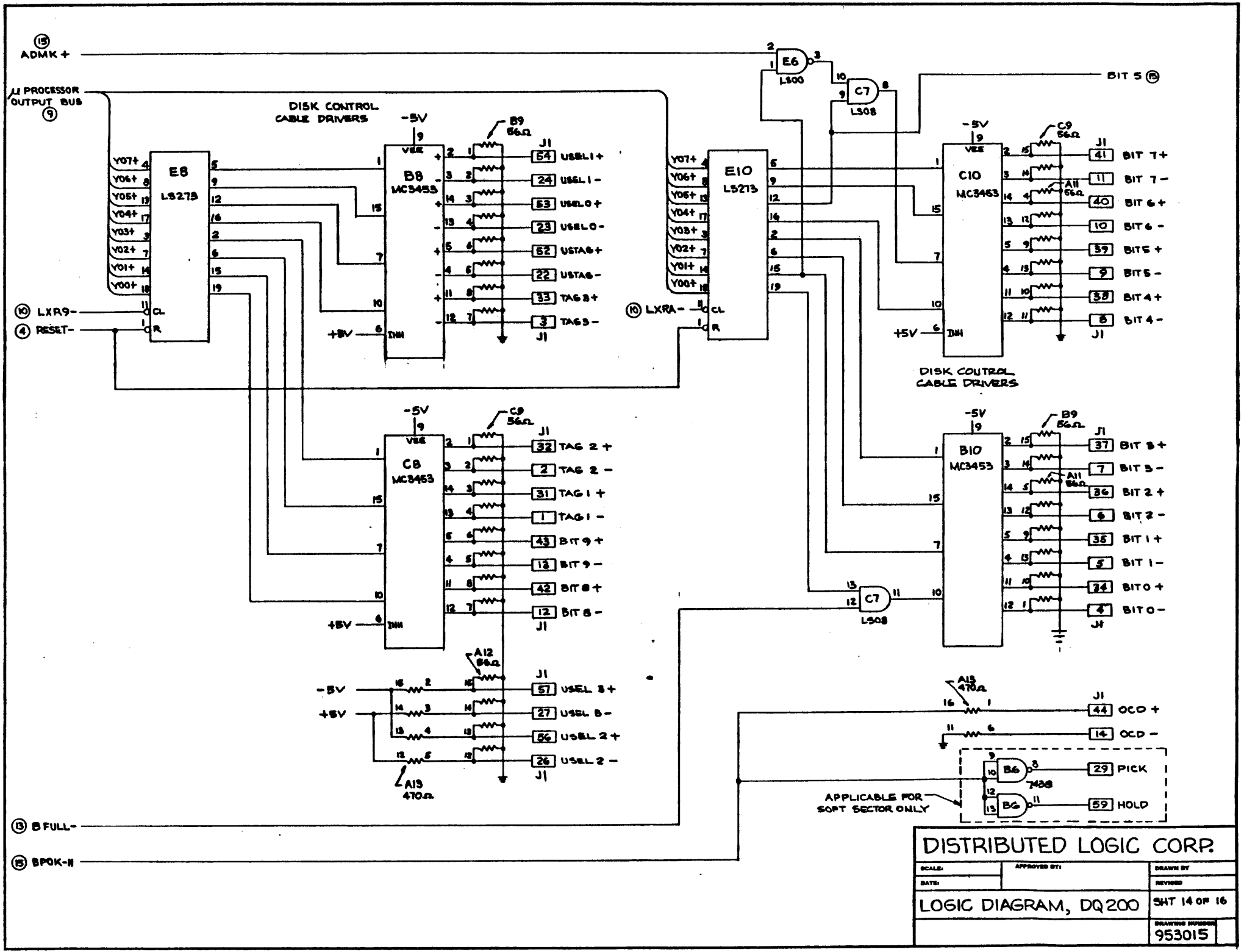
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ 200		SHT 12 OF 16
		DRAWING NUMBER 953015



DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ200		SHT 13 OF 16
		DRAWING NUMBER 953015



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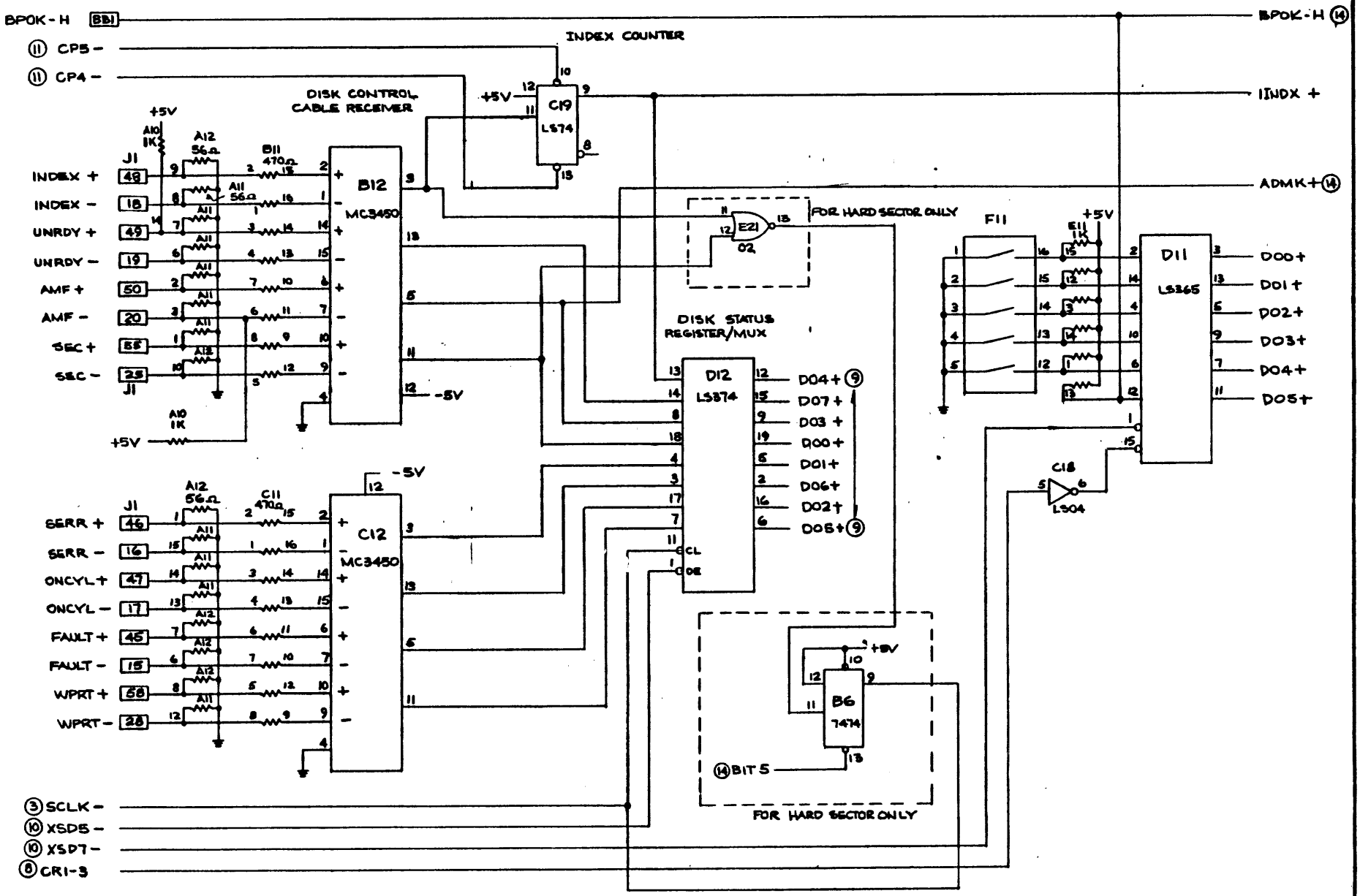
SCALE:	APPROVED BY:	DRAWN BY
DATE:		REVISED
LOGIC DIAGRAM, DQ200		SHT 14 OF 16
		DRAWING NUMBER 953015



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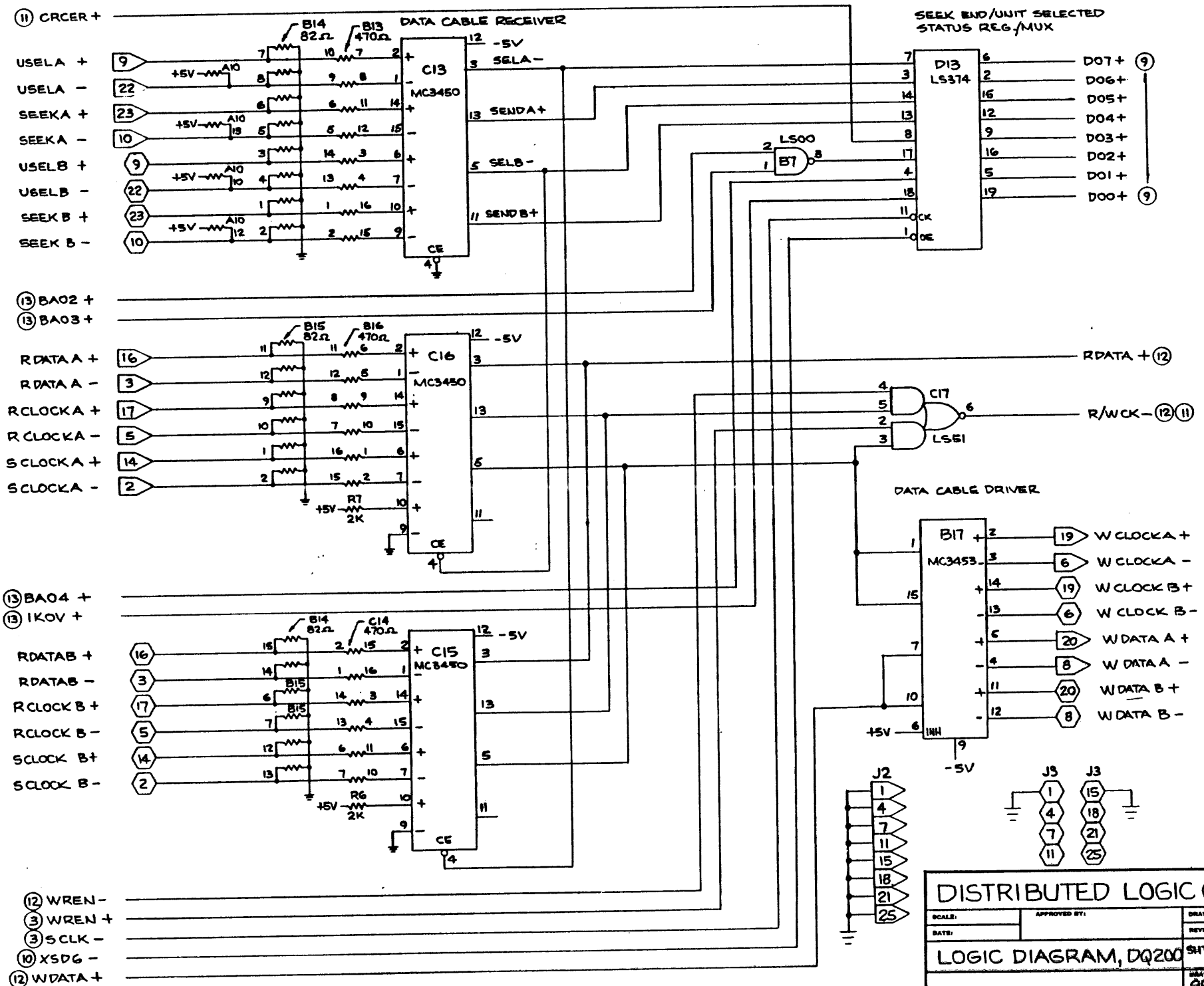
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ200		SHT 15 OF 16
		DRAWING NUMBER 953015


(11) CRCER +
USELA +
USELA −
SEEKA +
SEEKA −
USELB +
USELB −
SEEK B +
SEEK B −
B14 82Ω
B13 470Ω
DATA CABLE RECEIVER
C13
MC3450
+5V
A10
-5V
SELA−
SENDA+
SELB−
SEND B+
CE
SEEK END/UNIT SELECTED
STATUS REG./MUX
D13
LS374
LS00
B7
DO7 + (9)
DO6+
DO5+
DO4+
DO3+
DO2+
DO1 +
DO0+ (9)
CK
OE
(13) BA02 +
(13) BA03 +
RDATA A +
RDATA A −
RCLOCKA +
RCLOCKA −
SCLOCKA +
SCLOCKA −
B15 82Ω
B16 470Ω
C16
MC3450
R7 2K
RDATA + (12)
C17
LS51
R/WCK− (12) (11)
DATA CABLE DRIVER
B17
MC3453
W CLOCKA +
W CLOCKA −
W CLOCK B+
W CLOCK B−
W DATA A +
W DATA A −
W DATA B +
W DATA B −
INH
(13) BA04 +
(13) IKOV +
RDATAB +
RDATAB −
RCLOCK B +
RCLOCK B −
SCLOCK B+
SCLOCK B−
C14 470Ω
C15
MC3450
R6 2K
J2
J3
J5
(12) WREN−
(3) WREN +
(3) SCLK −
(10) XSDG −
(12) WDATA +
DISTRIBUTED LOGIC CORP.
SCALE:
APPROVED BY:
DRAWN BY D.L.
DATE:
REVISED
LOGIC DIAGRAM, DQ200
SHT 16 OF 16
DRAWING NUMBER
953015