344 CASSETTE MAGNETIC TAPE SYSTEM

MAINTENANCE MANUAL

dicom
DICOM INDUSTRIES

344

CASSETTE

MAGNETIC

TAPE SYSTEM

MAINTENANCE

MANUAL

DICOM INDUSTRIES
715 NORTH PASTORIA AVENUE
SUNNYVALE, CALIFORNIA 94086

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SECTION 5

PREVENTIVE MAINTENANCE

SECTION 5

PREVENTIVE MAINTENANCE

5-1 INTRODUCTION

Properly performed at the intervals specified in Table 5-7, preventive maintenance can extend the wear life of the mechanical components past the design life and will significantly reduce failures of components and of data transmission.

5-2 TAPE PATH CLEANING

1. Lower the Loader Assembly
2. Wet a cotton swab with Isopropyl alcohol or Freon thoroughly.
3. Insert the cotton swab into the loader opening and using the EOT/BOT lamp as illumination, wipe off the Read/Write head which is to the rear and right of the lamp.
4. Wipe off the Buffer Spring Assembly which is the shiny metal object to the right and just inside the loader.
5. Wipe off the residue lying about in the Loader Assembly.

5-3 PINCH ROLLER CLEANING

1. Remove the six screws securing the top cover.(Refer to Figure 8-9.A).
2. Remove top cover, and wet a cotton swab with Isopropyl alcohol or Freon.
3. Place the desired Deck in OFF-LINE READ while holding the switch in the center of the Tape Transport Module clear plastic lid depressed. (refer to Figure 8-6).
4. Place the wetted cotton swab behind the rotating pinch roller.
5. Release the cassette in place switch and wipe off the capstan.

CAUTION: DO NOT ALLOW THE COTTON SWAB TO BE PULLED INTO THE CAPSTAN.

5-4 VERIFICATION OF MECHANICAL INTEGRITY

Verification of the mechanical integrity of the Tape Transport Module will be found in Section 8.

5-5 CLEANING AND LUBRICATION OF FRICTION PATHS

5-5.1 Head Arm Actuator and Guillotine Latch

5-5.1.A Using a cotton swab saturated with Freon or or alcohol wipe the visible lubricant from the Head Arm Actuator and the Guillotine Latch (refer to Figure 8-9.A)

5-5.1.B Using a dry cotton swab apply Lubriplate grease along the Head Arm Actuator and press the Lubriplate into the Guillotine Latch (refer to Figure 8-6).

5-5.1.C Lower the Loader mechanism and depress and release the Cassette In Place Switch (refer to Figure 8-6) a few times.

5-5.1.D Wipe off excess Lubriplate.

5-5.2 Rewind Actuator Arm.

5-5.2.A Using a cotton swab saturated with Freon or alcohol wipe the Rewind Actuator Arm on the top and the bottom. (Refer to Figure 8-9.A).

5-5.2.B Press the Rewind Solenoid Plunger into the solenoid and again wipe the Rewind Actuator Arm on the top and the bottom.

5-5.2.C Using a dry cotton swab apply Lubriplate to the Rewind Actuator Arm on the top and the bottom.

5-5.2.D Press the Rewind Solenoid Plunger into the Rewind Solenoid and apply Lubriplate to the top and bottom of the Rewind Actuator Arm.

5-5.2.E Press and Release the Rewind Solenoid Plunger into and out of the solenoid a few times.

5-5.2.F Wipe off excess Lubriplate.

TABLE 5-1

RECOMMENDED DICOM 344 PREVENTIVE MAINTENANCE SCHEDULE

Daily	Monthly	2 Months	6 Months	18 Months
Clean the Read/ Write Head and Buffer Spring Assembly surfaces on each tape transport	Clean the pinch roller of each tape transport. Clean the air filter at the rear of the unit.	Verify clutch performance by testing the start/ stop acceleration profile. Observe all solenoids for proper operation. Observe drive belts and Buffer Spring for wear.	Lubricate transport friction paths. Clean tachometer commutator and check wiper contacts for wear on each tape transport.	If the tape transport has received average to heavy usage, an overhaul should be performed to eliminate possible failures. Overhauls can be performed by either Dicom or the user and should consist of the replacement of the following components: 1. Clutch/Capstan Assy. 2. All drive belts 3. Tachometer wiper contacts 4. Buffer spring 5. Pinch roller The following componenets should be observed for wear and replaced if wear is noted: 1. Rewind pulley assy. 2. Take-up drive idler. 3. Forward take-up reel 4. Read/Write head

Effective January 1, 1971

PRICE SCHEDULE

SPARE PARTS

PART NAME	PART NUMBER	UNIT PRICE
Tape Transport Module	344-70036	$1,250.00
Capstan Assembly	344-70019	290.00
Motor Assembly	186A229-1	82.50
Pinch Roller Assembly	344-80105	35.00
Buffer Spring Assembly	344-70009	37.00
Rewind Drive Belt	2-033 (P665)	.90
Jackshaft Drive Belt	2-230 (P665)	.90
BOT/EOT Lamp Assembly	344-60016	16.75
Forward Drive Idler	528-70186	5.50
Pulley Assy Rewind	528-80305	12.50
Tachometer Wiper contacts	278-90229	22.00
Forward Take-up	528-10185	28.00
Fuse	361003	.15
Lamp Switch Panel	#330	.20
Lamp "Ready"	#373	.20
Fuse	313003	.15
*MOS Buffer Decode	344-50024	125.00
*MOS Buffer	344-50020	375.00
TTY Control	344-50021	125.00
On-Line Sync Control	344-50022	130.00
Mode and State Decode	344-50023	100.00
Tape Data Control	344-50026	160.00
Shift Register 1 & 2	344-50027	125.00
Read/Write Electronics	344-50028	150.00
Deck Control	344-50030	150.00
Off-Line Control	344-50031	110.00
Motion Control	344-50032	135.00
Reproduce	344-50033	145.00
Computer Control	344-50037	130.00
Power Supply	344-70028	350.00
** Power Supply Regulator	344-50035	115.00
*** Serial I/O Control	344-50050	150.00
Extender Module	344-50039	28.80

* Option 2 Requirement
** Included in Power Supply
*** Option 06

TERMS: FOB Sunnyvale, California; freight charges collect; 1% discount 10 days, Net 30 days. 1.5% interest per month (18% per year) charged on accounts over 30 days.

Prices subject to change without notice

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
M	CN 549-1	ALTMAN	4-70	J. Tedesco	5/28/70

HIP/HOP LATCH
LOADER LATCH
REWIND LATCH
READY LATCH
DECK (N) WRITE LATCH
HIP
DECK SEL
J1 → J18-15(S), J2 → J19-15(S), J3 → J20-15(S) HIPS(N) +5V R1 2.2K
J1 → J18-14(S), J2 → J19-14(S), J3 → J20-14(S) E HOPS(N) +5V R2 2.2K
J1 → J18-12(S), J2 → J19-12(S), J3 → J20-12(S) 15 EJECT P-(N) +5V R3 2.2K
J1 → J18-11, J18-13(S), J2 → J19-11, J19-13(S), J3 → J20-11, J20-13(S) CLIP(N) R8 2.2K +5V
+5V R9 2.2K
J1 → J18-10(S), J2 → J19-10(S), J3 → J20-10(S) 17 LOP(N)
J4-16(S), J6-11(S) D RWND P*
J5-Y(S), J6-19 N HALTP
J1 → J18-16 BOT LP (N) 16 R28 100Ω +12V
J2 → J19-16
J3 → J20-16
C1 .01 UF 80V
R31 5.1K +5V
TP2
J1 → J18-F(S), J2 → J19-F(S), J3 → J20-F(S) AA BOT PHOTO CELL IN (N)
Q5 2N3906
R29 47K
J1 → J18-17(S), J2 → J19-17(S), J3 → J20-17(S) T BOT LP RET (N)
R30 100K
R32 68Ω
-12V
R40 1.2K +5V
J1 → J15-AA, J18-9, J2 → J15-5, J19-9, J3 → J15-3, J20-9 13 D(N)W
J4-5(S) P INIT*
J6-X(S) 21 WFMP+ WRITP
J10-27, J4-2(S), J5-E, J6-H(S) 20 READ P*
J1 → J4-CC J5-B(S), J2 → J4-19, J5-J(S), J3 → J4-18 J5-K(S) 18 D(n)*
R41 2.7Ω E2 E3
R22 2.2K +5V NLOSW(n) 11 → J1 → J18-8, J2 → J19-8, J3 → J20-8
R33 4.7K +5V LOX(n)-1 2 → J1 → J25-7, J2 → J24-20, J3 → J24-
DLOS* H → J6-27
DREADS* J → J6-24
DRDY* F → J6-20
DWRITS* L → J6-23
DWLOS* M → J6-EE, J5-4
READ SEL(N)* 19 → J1 → J5-N(S), J15-21, J16-21, J2 → J5-P(S), J15-H, J16-H, J3 → J5-R(S), J15-H, J16-H
IMOT C → J5-Z(S), J6-12
TYP CKT LOCATED IN TTM
+5 AA T 16
J1 → J18-8, J2 → J19-8, J3 → J20-8
J1 → J18-A, J2 → J19-A, J3 → J20-A RAISE HEADS SOL(N) Z
J1 → J18-V, J2 → J19-V, J3 → J20-V LOWER(N) HEADS SOL X
J1 → J18-W, J2 → J19-W, J3 → J20-W RAISE LOADER SOL(N) W
J1 → J18-X, J2 → J19-X, J3 → J20-X REWIND SOL(N) Y
SOL GND 24 J22-B BB
R4 120Ω 1/2W R5 16K CR1 R6 510Ω Q1 2N4923 R7 2.7Ω TP3
R10 120Ω 1/2W R11 16K CR2 R12 510Ω Q2 2N4923 R13 2.7Ω TP5
R14 120Ω 1/2W R15 16K CR3 R16 510Ω Q3 2N4923 R17 2.7Ω TP7
R18 120Ω 1/2W R19 16K CR4 R20 510Ω Q4 2N4923 R21 1Ω 1/2W TP4
DREW* 22 J4-W, J5-25
READY LITE 3 J1 → J18-T, J2 → J19-T, J3 → J20-T
TACH A(N) U J1 → J18-H, J2 → J19-H, J3 → J20-H TP6
R23 1.5K
R24 100K R25 1.8K R38 10K CR8 R26 2.2K CR5 C3 2.2UF Q7 D13T1 C4 2.2UF
HALT P TACH 23 J10-DD
TACH B(N) V J1 → J18-J, J2 → J19-J, J3 → J20-J
R27 100Ω
R34 150Ω 1/2W R35 16K CR7 R36 510Ω Q6 2N4923 R37 2.7Ω TP13
BRAKE B J1 → J18-Y, J2 → J19-Y, J3 → J20-Y
SOL GND 24 J22-B BB
TP1
C8 .1UF 10V, C7 .1UF 10V, C6 .1UF 10V, C5 200F 15V, C9 10UF 25V
1 A +5V, 28 FF GND, 26 +12V, 27 -12V
+25 SOL FIELD
TYP CKT LOCATED IN TTM

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W 5%.
2. ALL DIODES ARE IN914

J1,2,3

FAB REV	ASSY REV
J	M

OUTSTANDING CHANGES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. XX ± XXX ± ANGLES ±
MATERIAL SPECIFICATION
FINISH SPECIFICATION
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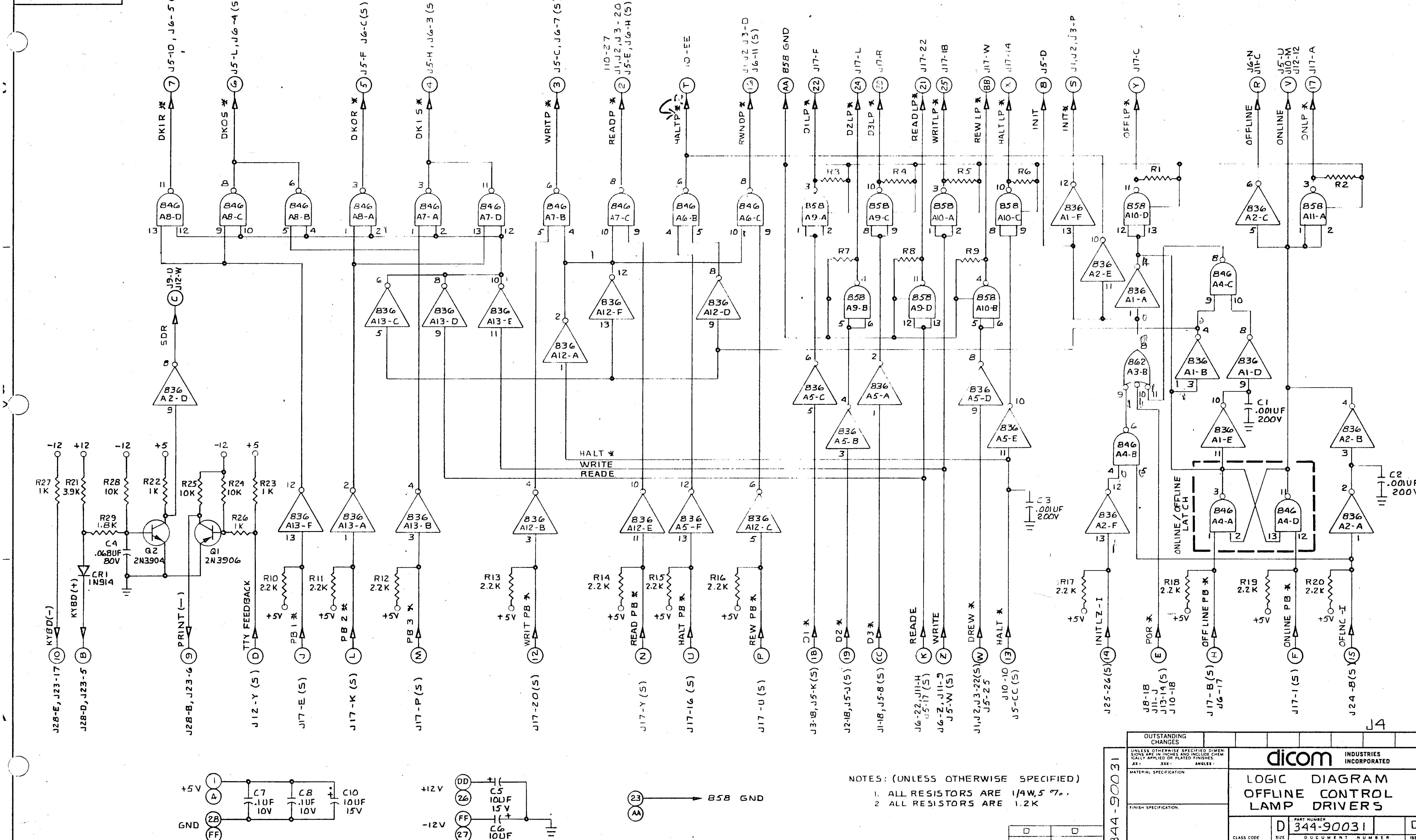
LOGIC DIAGRAM
DECK CONTROL

CLASS CODE S/Z | D | PART NUMBER 344-90030 | M | DOCUMENT NUMBER | ISS
SCALE NONE | SHEET

ISSUE	DESCRIPTION	DRAFTING	DATE	DESIGN	DATE
D	CN 549-1	ALTMAN	3/70	L. T...	5/20/70



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS ARE 1/4W, 5 %.
2. ALL RESISTORS ARE 1.2K

FAB REV	ASSY REV
D	D

344-90031

OUTSTANDING CHANGES

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MATERIAL SPECIFICATION

FINISH SPECIFICATION

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LOGIC DIAGRAM OFFLINE CONTROL LAMP DRIVERS

CLASS CODE | SIZE D | PART NUMBER 344-90031 | ISSUE D

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ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
F	CN 549-1	ALTMAN	4/70	T. Tomasetti	5/20/70

DECK SELECT A LATCH
DECK SELECT B LATCH
READ SELECT A LATCH
READ SELECT B LATCH
BOT INH LATCH
PUT 2

J4-6 (S) J6-4 (S) (L) DKOS *
J4-5 (S) J6-C (S) (F) DKOR *
A4-8 READ E
J4-4 (S) J6-3 (S) (H) DKIS *
J4-7 (S) J6-5 (S) (10) DKIR *
J4-8 (S) (D) INIT
A18-3 READ P
J1,J2,J3-20 J4-2(S),J6-H(S) J10-27 (E) READ P *
J1,J2,J3-H (S) J6-27 (B) DL/OXS *
J1,J2,J3-M (S) J6-EE (4) DWLOS *
J4-3 (S) J6-7 (S) (C) WRITP *

DSA, DSA *, DSB, DSB *, RSA, RSA *, RSB, RSB *

READ SEL 1 * (R) J3-19 J15-H J16-H
READ SEL 2 * (1) J2-19 J15-11 J16-11
READ SEL 3 * (M) J1-19 J15-21 J16-21
DI * (K) J3-18 J4-18
D3 * (B) J1-18 J4-CC
DO * (9) J6-BB J10-21 J11-7
D2 * (J) J2-18 J4-19

+5V (1) (A)
GND (28) (FF)
C12 .1UF 10V
C15 .1UF 10V
C17 .1UF 10V
C19 10UF 15V
TP1 GND

+5V R5 1K
CR3 IN914
R6 68K
CR5 IN914
TP7
R7 82K
R8 1.8K
C20 10UF
Q2 D13T1
R9 2.2K

INIT *, WRIT, WRITE P, HALTP *, BOT INH *, READP *, WRITP *, DO *

NOTES:
1. ALL RESISTORS ARE 1/4W 5%.
2. R10 & C13 ARE TO BE SELECTED AT TEST.

J5

OUTSTANDING CHANGES

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XX- .XXX- ANGLES-
MATERIAL SPECIFICATION:
FINISH SPECIFICATION:

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LOGIC DIAGRAM
MOTION CONTROL

CLASS CODE D | SIZE | PART NUMBER 344-90032 | ISSUE F

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E FAB REV | F ASSY REV

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5-6-3

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
F	CN 549-1	ALTMAN	9/70	Tibbitt	9/30/70

READRST J14-16 (18) · READE A22-1 · READE J4-K J11-H J6-22 (17) · WRIT A7-13 · WRITE J4-Z J6-Z J11-9 (N) · I MOT J1,J2,J3-C J6-12 (Z) · HALT * J4-L3 J10-10 (CC) · UP TO SPD J13-N J6-W (20) · 20 * A13-3

TP3 · TP5 · TP6 · TP4 · TP2

B30 A2-A · B46 A4-C · B62 A3-B · B30 A2-B · CR6 IN914 · B62 A11-A · B30 A12-B · CR1 IN914 · B36 A1-D

BOT INH * A5-8

READ LATCH: B46 A4-B · B62 A11-B

WRIT LATCH: B46 A4-A · B62 A11-C

A6-12 READP * · A6-13 WRITP * · A5-10 INT *

B46 A4-D · B36 A19-F · B36 A19-B · B36 A19-D · C1 120PF 500V

B36 A20-E · B36 A20-D · C8 .001UF 200V · B36 A20-C · B62 A5-A · B36 A19-A · B36 A19-C

B30 A12-A · B36 A1-B · B36 A1-C · B62 A3-C

CR4 IN914 · B36 A17-F · B36 A17-A · C13 · R10 · C10 3.3 UF 15V · +5V

UP TO SPEED DLY LATCH: B46 A9-A · B46 A9-B

PUT 3: Q1 D13T1 · R4 1.8K +5V · R3 2.2K

WRIT · WRITE

B36 A17-C · B36 A1-E · C9 .001 UF 200V · B36 A1-A · B36 A1-F · B46 A9-D · WRIT · WRITR

B46 A9-C

FLGR * (19) J6-21

B36 A17-D · B36 A17-F · B36 A18-F · C11 .0022 UF 80V · B36 A18-D · B36 A18-A · B36 A18-E · B36 A18-B · B36 A18-C

T1 TIME * (T) J13-V (S) · GAPT 2P (G) J6-F · GAPT 2 (S) J6-L J13-Y (S) · SRCH * (11) J11-12 J6-13 (S) · WRITR * (BB) J12-H (S) · A5-10 · HALTP 1 * (2) J6-G (S) J8-20, J12-B · HALTP 1 (Y) J1,J2,J3-N J6-19 · WFM * (V) J6-2 (S) · DREW * (25) J1,J2,J3-22 (S) J4-W · ONLINE (U) J10-M J4-V (S) J12-12 · Ø CR 2 (12) J11-Z (S) J8-X · WRITEP A24-6 · NDATT (24) J10-24 (S) J10-2 · READ P A7-9 · ODATT (21) J10-22 (S) J12-6

J5

OUTSTANDING CHANGES			
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MATERIAL SPECIFICATION	LOGIC DIAGRAM MOTION CONTROL		
FINISH SPECIFICATION	CLASS CODE D · SIZE · PART NUMBER 344-90032 · F		
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344-90032

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5564

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
J	CN 549-1	ALTMAN	4-70	[illegible]	

CMDT (B) J10-B
DKOS * (4) J4-G(S) J5-L
DKOR * (C) J4-5(S), J5-F
DKIS * (3) J4-4(S), J5-H
DKIR * (5) J4-7(S), J5-10
WRITP * (7) J4-3(S), J5-C
WFMP + WRITP (X) J1, J2, J3-21
READP * (H) J1, J2, J3-20, J4-2(S) J5-E, J10-27
HALTP I * (G) J5-2, J10-CC J8-20, J12-B
RWNDP * (11) J1, J2, J3-D J4-16(S)
WFM * (2) J5-V
OFLNS-I (D) J25-S
SHCH * (13) J5-11 J11-12

WFM * → A2-12
A2-8
A1-9
FILE GAP DETECT LATCH → A1-11
GAPT? → A5-9
IMOT? → B5-5
DRDYS → B2-B
IMOT → B3-9
OFFLINE → A3-13

TP5 TP6 TP10 TP1 GND

C5 10UF 15V; C6 .1UF 10V; C7 .1UF 10V; C8 .1UF 10V; +5V (1, A); GND (28, FF)
C11 15UF 15V; R25 16K; R1; C13 120PF 500V; C4 470 PF 500V
R3, R4, R5, R6, R7, R8, R9, R10, R11 +5V

DKSOC-I (D) J25-25(S)
DKSIC-I (E) J25-18(S)
WRITC-I (R) J25-12(S)
READC-I (S) J25-5(S)
HALTC-I (16) J25-24(S)
RWNDC-I (T) J25-17(S)
FLMKC-I (14) J25-11(S)
OFFLINE PB * (17) J9-H J17-B(S)
SRCHC-I (10) J25-4(S)
CMDT-I (M) J25-6(S)
OFFLINE (N) J11-C J4-R(S)
IMOT (12) J1, J2, J3-C J5-Z(S)
HALTP I (19) J1, J2, J3-N J5-Y(S)

836 A7-C; 846 A7-D; 846 D3-C; 846 D7-C; 846 D7-D; 846 D7-B; 846 D7-A; 846 D5-B; 846 D5-C; 846 B7-C; 846 D5-D; 846 D5-A; 846 D3-D; 846 B7-A; 836 B1-A; 9601 D2; 846 B4-B; 846 B4-C; 846 B4-D; 836 A5-F; 836 A7-D; 846 A4-D; 846 A4-C; 836 A3-C; 836 A3-D; 846 B7-D; 846 B4-A; 846 B7-B; 836 D4-F; 836 D4-D; 836 D4-C; 836 D4-A; 836 D4-F; 836 D4-B; 836 B5-F; 836 B5-D; 836 B5-E; 836 B5-A; 836 A7-B; 836 A5-B

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W 5%.
2. ALL RESISTORS ARE 5.1 K
3. * R23, C9 & C10 TO BE SELECTED & INSTALLED AT TEST.

J6

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. XX ± ANGLES ±
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FINISH SPECIFICATION
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LOGIC DIAGRAM
COMPUTER CONTROL

344-90037

CLASS CODE D SIZE PART NUMBER 344-90037 DOCUMENT NUMBER J ISSUE
SCALE NONE SHEET 1 OF 2

FAB REV J ASSY REV J

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5606

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
J	CN 549-1	ALTMAN	9-70	J. Takeuchi	5/24/70

B1-2 WFM*WE

B4-13

A3-8

B7-4

B7-5

B5-2 IMOTM

A5-4 DRDY 5

A5-3 IMOT

B5-11 OFFLINE

TP3 FILE GAP DETECT LATCH

TP8 REG

836 A7-A

836 A1-D

836 A1-C

836 A2-F

836 A2-D

836 A2-E

836 A2-C

836 A2-B

836 A2-A

C2 470PF 500V

R23 * +5V

C9 *

C3 30UF 15V

TP4

R13 27Ω

836 A3-A

836 A3-E

E1

R24 2.7Ω

E2

TP2 ERROS

TP7 FLAGS

TP9 DRDYS

E4

ERROS LATCH

FLAG LATCH

846 A1-A

846 A1-B

862 B3-C

862 B3-A

JUMPER

E6

JUMPER

862 B3-B

836 A5-E

836 A5-C

836 A5-A

836 A5-D

846 A4-B

846 A4-A

BOT INH FILE DETECT LATCH

836 A3-F

836 A3-B

846 B2-C

R12 +5V

J25-2 FLMKS-I R14 +5V

J25-14 ERROS-I R15 +5V

J25-3 FLAGS-I R16 +5V

J25-10 DRDYS-I R17 +5V

J25-22 WRITS-I R18 +5V

J25-9 L/OXS-I R19 +5V

J25-21 WLOKS-I R20 +5V

J25-15 READS-I R21 +5V

858 B6-C

858 B6-B

858 B6-A

858 B6-D

858 D1-C

858 D1-B

858 D1-A

858 D1-D

836 B5-C

836 B5-B

836 B1-F

836 B1-B

836 B1-C

836 B1-D

846 B2-A

846 B2-B

836 B1-E

J5-6(S) GAPT2P (F)

J13-Y(S) J5-5 GAPT 2 (L)

J5-AA(S) (15) BOT INH *

J25-16(S) (V) STATT-I

J13-J(S) (U) ERROR FLAG

J5-19(S) (21) FLAGR *

J10-8(S) (Y) SET RDY FLAG *

J1,J2,J3 R(S) (20) DRDY *

J10-21 J5-5(S) J11-7 DO * (BB)

J1,J2,J3-L(S) (23) DWRITS *

J4-Z J5-W(S) J11-9 WRITE (Z)

J1,J2,J3-H(S) J5-B (27) DL/OXS *

J1,J2,J3-M(S) J5-4 (EE) DWLOS *

J4-K J5-17(S) J11-H READE (22)

J1 J2 J3-J(S) (24) D READS *

J6

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
.XX - ANGLES -

MATERIAL SPECIFICATION

FINISH SPECIFICATION

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LOGIC DIAGRAM COMPUTER CONTROL

344-90037

CLASS CODE D SIZE | PART NUMBER 344-90037 DOCUMENT NUMBER | J ISSUE

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SHEET 2 OF 2

PRINTED ON DIEPO NO. 1000H-S CLEARPRINT
PAGE OUT 1-70

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
F	CN 549-1	ALTMAN	3/10	L Tashjian	3/20/70

LOAD MOS BIT *1 TP2 · NEW DATA TP5 · ANY SOB * TP3 · MB6 * · NEW DATA · REC

J9-BB (W) MB1 · J8-P(S) (23) REC · J9-P(S) (3) DB1 · J9-23 (Y) MB2 · J9-12(S) (R) DB2 · J9-24 (AA) MB3 · J9-N(S) (22) DB3 · J9-CC (Z) MB4 · J9-8(S) (U) DB4 · J9-T (4) MB5 · J9-F(S) (CC) DB5

846 A3-B · 846 A3-A · 846 A3-C · 846 A3-D · 846 A2-B · 846 A2-A · 846 A2-C · 846 A2-D · 846 A6-B · 846 A6-A

R1 2.2K · R2 6.8K · R5 2.2K · R6 6.8K · R9 2.2K · R10 6.8K · R13 2.2K · R14 6.8K · R18 2.2K · R19 6.8K

MOS A17-A · MOS A17-B · MOS A18-B · MOS A18-A · MOS A19-B

836 A7-F · 836 A7-E · 836 A7-D · 836 A7-A · 836 A7-B · 836 A7-C · 836 A8-A · 836 A10-E

+5V · -12VF

MB2 * · MB4 · MB3 · MB1 · MB6 · MB7 · MB5

TP8 · 830 A5-A · DELETE * (B) J8-Y · 833 A16-A · TP9 · 830 A5-B · C/R * (2) J11-20 · 833 A16-B · 500KHZ A * J8-K (C) J13-15(S)

J9-7(S) (BB) DB6 · J9-D(S) (21) DB7 · 9Th REC BIT J11-M (S) (16) · 10 Th REC BIT J11-P(S) (5)

846 A6-C · 846 A6-D · 846 A13-B · 846 A13-A · 846 A13-C · 846 A13-D · 846 A14-B · 846 A14-A · 846 A14-C · 846 A14-D

R3 2.2K · R7 2.2K · R11 2.2K · R15 1K · R16 2.2K · R20 2.2K

MOS A19-A · MOS A20-B · MOS A20-A · MOS A21-B · MOS A21-A

836 A8-B · 836 A8-C · 836 A8-F · 836 A8-E · 836 A8-D · 836 A9-C · 836 A9-B · 836 A9-E · 836 A9-A

R4 6.8K · R8 6.8K · R12 6.8K · R17 6.8K · R21 6.8K

MB6 (T) J9-2 · MB7 (Y) J9-3 · MB8 (X) J9-H · SOB 2 * (J) J8-4 · SOB 1 * (P) J8-D · MB9 (M) J11-K · FIRST CHAR (K) J8-11 · LAST CHAR * (N) J8-J · MB10 * (L) J11-15

TP7 · TP4 · TP6

862 A4-B · 862 A4-A · 846 A15-B · 846 A15-B · 836 A9-D · 836 A10-D · 836 A10-A · 836 A10-C · 836 A10-B

J8-9 J13-E(S) (D) 500KHZ A

ANY SOB * · NEW DATA · LOAD ON A * · SHIFT ON B *

SHIFT ON B CH 1032 A12 · LOAD ON A CH 1032 A1 · R22 470Ω · R23 470Ω

CLK Ø B (24) J13-F (S) · CLK Ø A (25) J13-D (S) · -12VF · +5V

836 A10-F · 846 A15-D · 846 A11-B · SOB IN * (10) J11-25 (S) · SCB 2 IN * (E) J11-23 (S) · DBB * (F) J9-4 (S)

J8-5(S) (H) NEW DATA · (9) ANY SOB * J11-13(S) J8-7

J7

-12V (27) EE · GRD FF (28) · +5V (A) · (J)

C14 22UF 15V · C3 22UF 15V · CR1 IN4005 · C4 .1UF 10V · C15 .1UF 10V · C5 22UF 15V · C6 20UF 15V · C7 .1UF 10V · C8 20UF 15V · C12 10UF 15V · C10 22UF 15V · C13 10UF 15V

TP1

NOTES:
1. ALL RESISTORS ARE 1/4 W, 5%.

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. XX- ±.01 XXX- ±.005 ANGLES- ±1°

MATERIAL SPECIFICATION: NONE

FINISH SPECIFICATION: NONE

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LOGIC DIAGRAM
MOS BUFFER
J7

344-90020

D	G
FAB REV	ASSY REV

CLASS CODE	SIZE	PART NUMBER / DOCUMENT NUMBER	ISSUE
	D	344-90020	F

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ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
E	CN 549-1	ALTMAN	3/70		5/20/70

Ø+3 LOAD BUFFER LATCH
1+2 LOAD BUFFER LATCH
ANY SOB LATCH
UNLOAD SOB 1 LATCH
UNLOAD SOB 2 LATCH
END OF BLOCK LATCH
STOP REC LATCH

J7-P (S) D SOB1 *
J11-24 (S) 3 Ø OR 3
J10-17 (S) E TAKE DATA
J7-J (S) 4 SOB 2 *
J11-22 (S) H 1 OR 2
J7-N (S) J LAST CHAR *
J7-9 J11-13 (S) 7 ANY SOB *
J13-C (S) F 500KHZB
J11-V (S) N LOAD SOB
J11-W (S) R LOAD SOB *
J11-J, J13-14 (S) J10-18, J4-E 18 POR *
J11-21 (S) 13 INH STATE ADV *
J12-5 (S) W
J13-21 19 TAPE CLK GATE *
J12-L (S)
J11-X (S) 12
J10-W (S) 10 SEND DATA
J7-K (S) 11 FIRST CHAR

LOAD SOB1
500KHZA *
500KHZA
DELETE *
Ø OR 2
TP7
TP6
TP4
TP5
TP2
TP1
TP3
POR *
STOP / LOAD *
STOP REC *
SOB1 + SOB2
SOB 2 *
SOB 1 *
500 KHZB *
DELETE SS *
END OF BLOCK
SET STOP REC *

NEW DATA ENABLE FF 853 A12 A
NEW DATA FF 853 A10 A
MOD CHAR FF 853 A16 B
ENAB STATE ADV FF 853 A19 A
WRITE TAPE ADV FF 853 A19 B
CHANGE CHAR FF 853 A16 A
DF 851 A1

CR1 IN914
CR2 IN914
CR3 IN914
C1 390PF 500V
C4 .1UF 10V
C7 .1UF 10V
C9 .1UF 10V
C10 10UF 15V
R1 4.8K 1/4W, 5% .06UF 80V

STOP LOAD A * 2 J10-H, J11-U
NEW DATA 5 J7-H
REC P J7-23
STOP LOAD B J10-3
BURST + OFFLINE S J11-T(S)
9TH & 10TH INH * C J11-S
DEL 55 * T J11-18
HALTP 1 * 20 J12-B, J5-2, J6-6(S) J10-CC (S)
MOD CHAR * L J11-16
STATE ADV * 14 J11-AA
STOP REC * Z NC
MOS DATA STROBE * 6 J10-Y
MOS DATA STROBE V J9-25
CHANGE CHAR * M J11-14
+5V A 1
GRD FF 28

J8

OUTSTANDING CHANGES	
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MATERIAL SPECIFICATION	
FINISH SPECIFICATION	
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LOGIC DIAGRAM
MOS BUFFER CONTROL

CLASS CODE	SIZE	PART NUMBER / DOCUMENT NUMBER	ISSUE
	D	344-90024	E

SCALE NONE SHEET 5 OF 12

E FAB REV	F ASSY REV	344-90024

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ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
D	CN 549-1	ALTMAN	3/70	T. Takeuchi	4/24/70

J10-V (S) (5) INPUT DATA STROBE
J7-3 (P) DB 1
REG 1 RESET * TP5

J24-7 (S) (13) NDAT 0 -I — R9 +5V — 836 A19-E
J7-R (12) DB 2
J24-26 (S) (R) NDAT 1 -I — R8 +5V — 836 A19-F
J7-22 (N) DB 3
J24-19 (S) (M) NDAT 2 -I — R7 +5V — 836 A20-B
J7-U (8) DB 4
J24-13 (S) (9) NDAT 3 -I — R6 +5V — 836 A20-C
J7-CC (F) DB 5
J24-6 (S) (K) NDAT 4 -I — R5 +5V — 836 A20-D
J7-BB (7) DB 6
J24-25 (S) (11) NDAT 5 -I — R4 — 836 A20-A
J7-21 (D) DB 7
J24-18 (S) (L) NDAT 6 -I — R3 — 836 A20-E
J7-F (4) DB 8 *
J24-12 (S) (10) NDAT 7 -I — R2 — 836 A20-F

J12-W, J4-C (S) (U) SDR
J12-J, J11-2 (S) (E) TYPE MODE
J14-21 (S) (J) READ TAPE DATA 0 *
846 A21-D — 836 A19-D — TP4 REG 1 SHIFT

846 A21-C — 846 A22-B — CNTR 1 RST * — J12-22, J13-B (S) (6)
J12-AA (S) (S) CNTR 1 NINE * — 836 A19-A
846 A21-B — 836 A19-C — C1 .001 UF 200 V

846 A12-B — FF 852 A11-B
846 A12-A — FF 852 A6-A
846 A12-D — FF 852 A6-B
846 A12-C — FF 852 A7-A
846 A13-B — FF 852 A7-B
846 A13-A — FF 852 A8-A
846 A13-C — FF 852 A8-B
846 A13-D — FF 845 A14

846 A10-C — 846 A10-10 — 846 A10-A — 846 A10-B — 846 A9-D — 846 A9-C — 846 A9-A — 846 A9-B

846 A16-C — FF 852 A4-B
846 A16-D — FF 852 A4-A
846 A16-A — FF 852 A3-B
846 A16-B — FF 852 A3-A
846 A15-D — FF 852 A2-B
846 A15-C — FF 852 A2-A
846 A15-A — FF 852 A1-B
846 A15-B — FF 852 A1-A

REG 1 RESET * (B) — J10-N (S)
REG 1 SHIFT (C) — J12-17 (S)
DATA TRANS STROBE (21) — J10-BB (S)

MB 1 (BB) — J7-W (S)
MB 2 (23) — J7-V (S)
MB 3 (24) — J7-AA (S)
MB 4 (CC) — J7-Z (S)
MB 5 (T) — J7-4 (S)
MB 6 (2) — J7-T (S)
MB 7 (3) — J7-Y (S)
MB 8 (H) — J7-X (S)
MOS DATA STROBE (25) — J8-V (S)

E4 — R18 — E5 — OPTION 02 REMOVE JUMPER

TP3 REG 2 SHIFT
REG 2 RESET * (16) — J10-15 (S)
REG 2 SHIFT (15) — J12-20 (S)

ØDAT 0 — (W) J13-X
REG 2 SB * — (17) J12-18
REG 2 RESET * TP2
REG 2 BIT 1 * — (18) J13-BB

858 A18-D — ØDAT 0-I — (Y) J24-17 — R17 +5V
858 A18-C — ØDAT 1-I — (X) J24-11 — R16 +5V
858 A18-A — ØDAT 2-I — (Z) J24-4 — R15 +5V
858 A18-B — ØDAT 3-I — (14) J24-23 — R14 +5V
858 A17-D — ØDAT 4-I — (19) J24-16 — R13 +5V
858 A17-C — ØDAT 5-I — (20) J24-10 — R12 +5V
858 A17-A — ØDAT 6-I — (AA) J24-3 — R11 +5V
858 A17-B — Ø DAT 7-I — (22) J24-22 — R10 +5V
OUTPUT STROBE — (V) J12-14 (S), J10-J

DYNAMIC E3 / E2 STROBED / E1 — R1 5.1K 1/4W 5% — +5V

+ C2 20UF 15V — C3 .1UF 10V — C5 .1UF 10V — C7 .1UF 10V — (1) (A) +5V — (2B) (FF) GND
TP1 GND

NOTES:
1. R2 THROUGH R18 ARE OPTIONAL.

J9

OUTSTANDING CHANGES

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LOGIC DIAGRAM SHIFT REG # 1 & # 2

CLASS CODE	SIZE	DOCUMENT NUMBER	ISSUE
	D	344-90027	D

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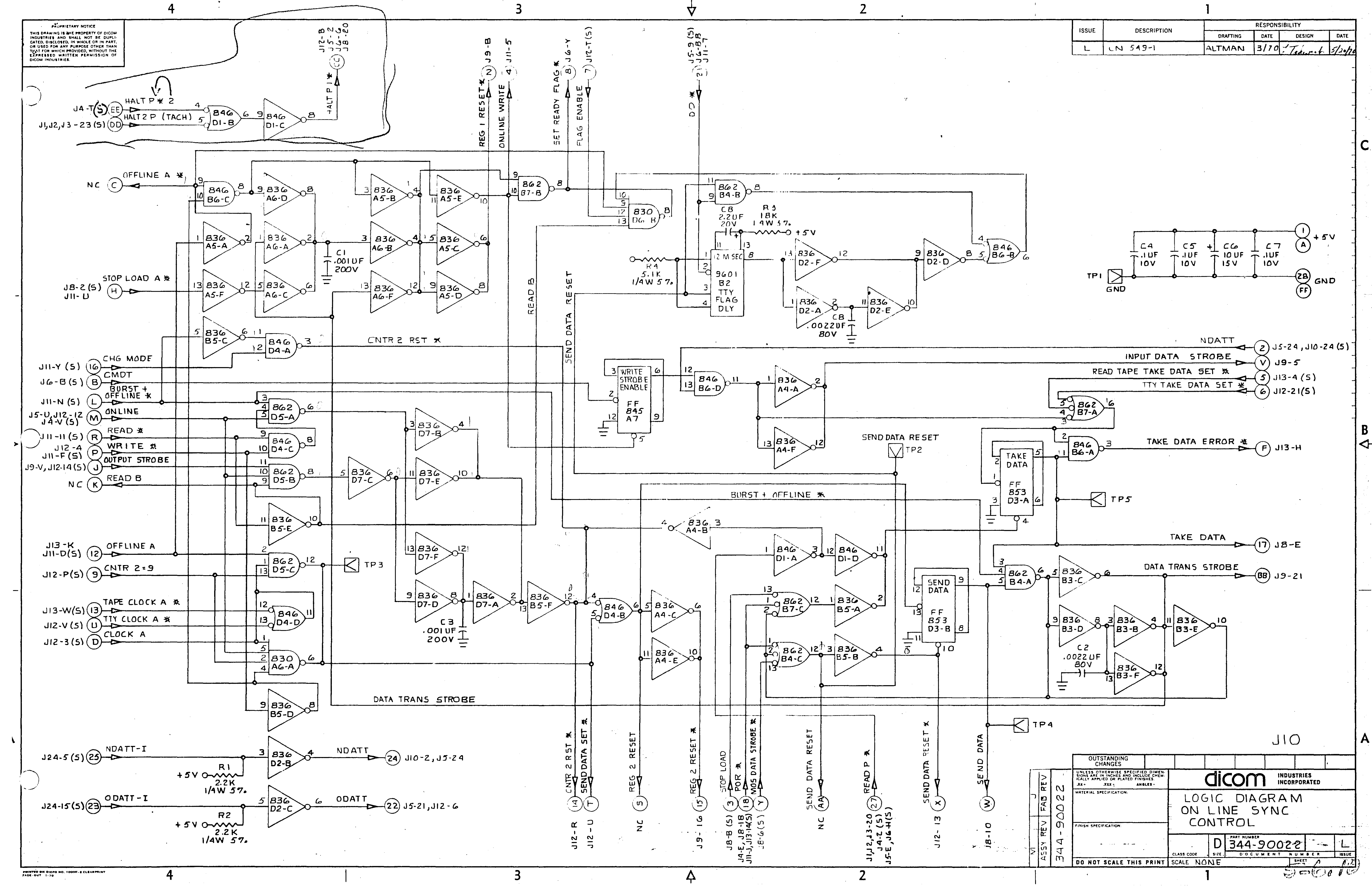
344-90027

C	D
FAB REV	ASSY REV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ISSUE
DESCRIPTION
RESPONSIBILITY
DRAFTING
DATE
DESIGN
DATE
L
CN 549-1
ALTMAN
3/70
HALT P * 2
HALT 2 P (TACH)
HALT P I *
OFFLINE A *
STOP LOAD A *
CHG MODE
CMDT
BURST + OFFLINE *
ONLINE
READ *
WRITE *
OUTPUT STROBE
READ B
OFFLINE A
CNTR 2 = 9
TAPE CLOCK A *
TTY CLOCK A *
CLOCK A
NDATT-I
NDATT
ODATT-I
ODATT
CNTR 2 RST *
DATA TRANS STROBE
REG 1 RESET *
ONLINE WRITE
SET READY FLAG *
FLAG ENABLE
SEND DATA RESET
WRITE STROBE ENABLE
12 M SEC
9601 B2 TTY FLAG DLY
NDATT
INPUT DATA STROBE
READ TAPE TAKE DATA SET *
TTY TAKE DATA SET *
TAKE DATA ERROR *
TAKE DATA
SEND DATA
TP1
TP2
TP3
TP4
TP5
GND
+5V
SEND DATA SET *
REG 2 RESET
STOP LOAD
POR *
MOS DATA STROBE *
READ P *
SEND DATA
J10
OUTSTANDING CHANGES
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FINISH SPECIFICATION
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LOGIC DIAGRAM
ON LINE SYNC
CONTROL
D
344-90022
L
SCALE NONE
344-90022

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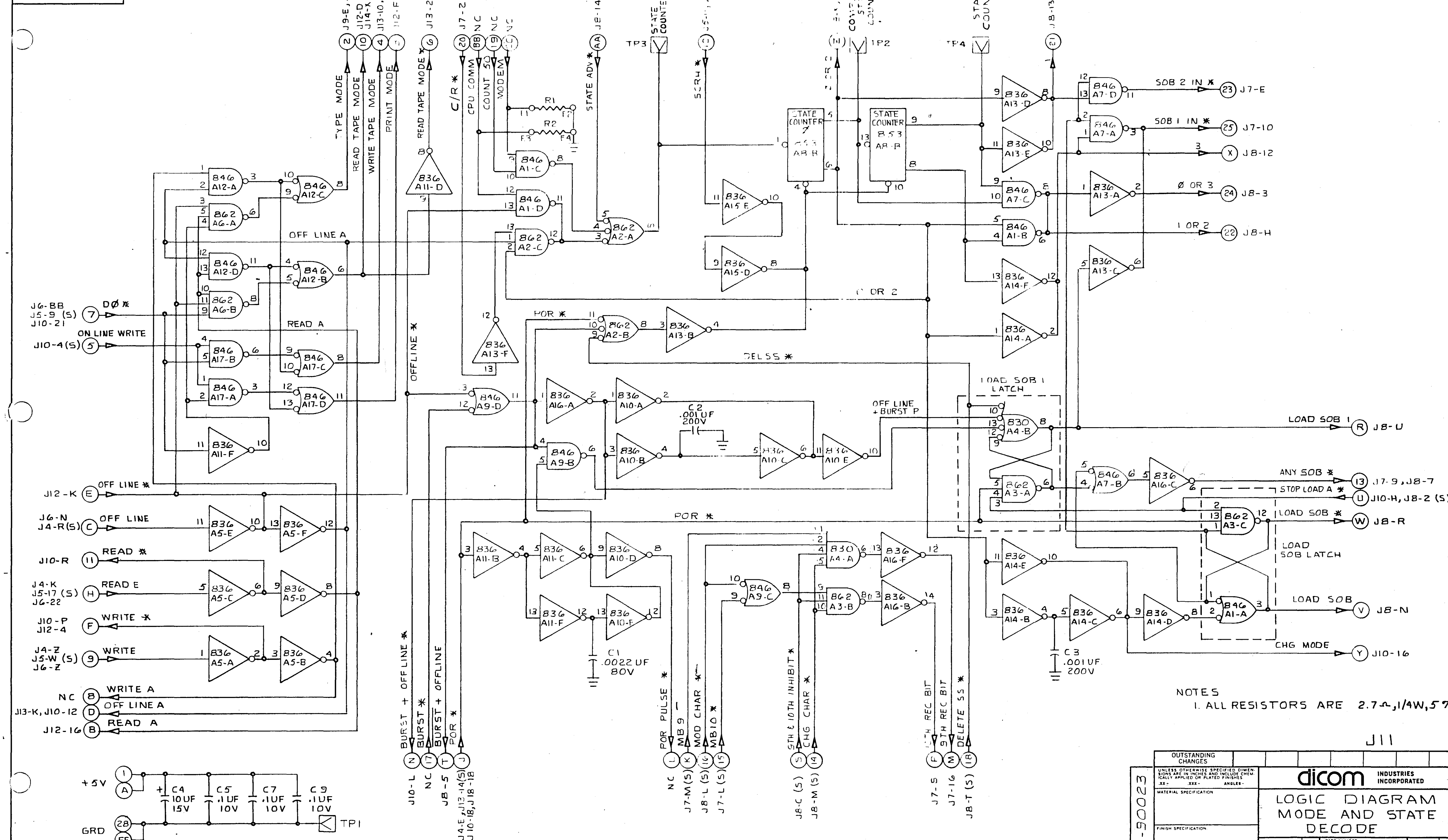
ISSUE	DESCRIPTION	DRAFTING	DATE	DESIGN	DATE
F	CN 549-1	ALTMAN	3/70		5/20/70



NOTES
1. ALL RESISTORS ARE 2.7Ω, 1/4W, 5%

J11

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

MATERIAL SPECIFICATION

FINISH SPECIFICATION

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LOGIC DIAGRAM MODE AND STATE DECODE

SIZE D PART NUMBER 344-90023 ISSUE F

E	F
FAB REV	ASSY REV

344-90023

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ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
D	CN 549-1	ALTMAN	3-70		

SEND DATA RESET LATCH
SEND DATA RESET *
J10-X (S) 13
HALT P1 *
J10-CC (S) B
J5-2, J6-6, J8-20
CNTR1 RST *
J9-6(S), J13-B (S) 22
TTY/TAPE CLOCK ENABLE
TP8
FLAG ENABLE *
TP5
FLAG ENABLE LATCH
J10-T (S) U SEND DATA SET *
J10-D(S) 3 CLOCK A
J11-E(S) K OFF LINE *
J5-BB H WRITR *
J13-9 15 TAPE CLOCK GATE
J13-21, J8-19 L TAPE CLOCK GATE *
J13-8 (S) 2 WRITE COMMAND
J11-3 (S) F PRINT MODE
J9-S AA CNTR 1 NINE *
J9-E, J11-2 (S) J TYPE MODE
NC E TTY CLOCK GATE *
J9-V, J10-J 14 OUTPUT STROBE
J10-7 T FLAG ENABLE
J5-U, J10-M, J4-V(S) 12 ON LINE
J11-B(S) 16 READ A
J5-21, J10-22(S) G ØDATT
J10-14 (S) R CNTR 2 RST *
+5V A
GND FF
C4 .1UF 10V
C6 .1UF 10V
C8 10UF 15V
C9 .1UF 10V
TP1
GND
J13-22 24 CNTR 2=8
NC 23 CNTR 2=9 *
NC X CNTR 2=10 *
J10-P, J11-F (S) 4 WRITE *
COUNTER 1
1 FF 853 A3-A
2 FF 853 A3-B
4 FF 853 A4-A
8 FF 853 A4-B
CNTR1=>4
CNTR1=8
TP3
C3 .001UF 200V
COUNT 1=9 TYPE MODE LATCH
C13 .006BUF 80V
TTY TAKE DATA SET * 21 J10-6
WRITE TAPE MODE CC J11-4(5),J13-10
TAPE CLOCK B BB J13-R (S)
COUNTER 1=9 *
PRINT MODE
REG 2 SHIFT 20 J9-15
READ TAPE SHIFT C J13-5 (S)
READ TAPE MODE D J11-10(S) J13-CC J14-X
TTY CLOCK A * V J10-U
REG 1 SHIFT 17 J9-C
TTY FEEDBACK
TP4
SDR W J4-C(S), J9-U
CNTR 2=(9+10) * 19 J13-P
TTY FEEDBACK Y J4-D
TTY CLOCK GATE 5 NC
CNTR 2=Ø * 25 NC
REG 2 SB * 18 J9-17 (S)
CNTR 2=9 P J10-9
J12
TP7
TAPE CLOCK GATE
C1 2.2UF 20V
R1 4.7K 1/4W, 5%
R2 5K
+5V
JUMPER
4.54 MILLI SECONDS 9601 A17
C2 .0022 UF 80V
TTY CLOCK GATE
C12 470PF 500V
TYPE MODE
COUNTER 2=8
TP2
C11 470PF 500V
COUNTER 2
1 FF 853 A1-A
2 FF 853 A1-B
4 FF 853 A2-A
8 FF 853 A2-B
TP6
TTY CLOCK GATE
INH STATE ADV * 5 J8-W
PRINT MODE

OUTSTANDING CHANGES
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MATERIAL SPECIFICATION: —
FINISH SPECIFICATION: —
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LOGIC DIAGRAM
TTY CONTROL
J12

F	E
FAB REV	ASSY REV

344-90021

CLASS CODE	SIZE	DOCUMENT NUMBER	ISSUE
	D	344-90021	D

SCALE NONE
SHEET 1

PRINTED ON DIPCO NO. 1000H-S CLEARPRINT FADE-OUT 1-70

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
F	CN 549-1	ALTMAN	3/70	L. Tabrah	5/20/70

C4 .033UF 8V
R8 5K
R7 6.8K
9601 A12
TAPE CLOCK GATE
J12-15 (S) 9
READ TAPE MODE * J11-6 (S) 23
836 A7-F
836 A7-E
836 A7-B
836 A7-C
C8 .001UF 200V
TAKE DATA ERROR * J10-F (S) H
846 A10-D
846 A10-C
ERROR FLAG J6-D
TAPE CLOCK J6-N C
836 A5-D
CNTR 1 RST * J9-G J12-22 B
TAPE CLOCK GATE * J8-19 J12-L (S) 21
TAPE CLOCK A * J10-13 W
TAPE CLOCK B * J12-8B R
REG 2 BIT 1 * J5-13 (S) 35
COUNTER 2=8 J12-24 (S) 22
COUNTER 2=(9+10) * J12-P (S) P
COUNTER 2-8 * NC S
Ø DAT 0 J9-W (S) X
836 A19-F
836 A19-F
C5 .0022UF 80V
REG 1 RST SYNC 853 A9-A
READ DATA CLOCK * J14-U (S) J14-W (S) 24
836 A7-A
846 A10-A
÷ 2 TAPE CLOCK 853 A16-A
836 A19-A
C15 500PF 500V
836 A19-B
TP7
846 A15-D
836 A13-D
846 A15-B
836 A13-E
846 A15-A
836 A13-F
846 A6-D
862 A1-A
830 A8-B
TP2
FF 845 A14
WRITE 1 25 J15-2
WRITE 0 19 J15-4
TAPE CLOCK GATE
836 A7-D
846 A10-B
TI TIME * J5-T V
CNTR 1-8 * J12-Z (S) 7
READ TAPE MODE J11-10 (S) CC J2-D, J14-X
TP3
830 A8-A
UP TO SPEED J5-20 (S) N J6-W
GAP T1 NC 6
READ TAPE TAKE DATA SET * J10-5 4
836 A5-F
836 A5-A
836 A5-B
C19 .001UF 200V
846 A17-A
COUNTER 1=8 NC L
+5V
C1 .056UF 80V
R2 5K
R1 5.1K
C2 .1UF 80V
R4 5K
R3 10K
C3 3.3UF 80V
R5 10K
TAPE READ SHIFT 9601 A3 135 USEC
GAP T1 9601 A4 450 USEC
GAP T2 9601 A2 1.1 MSEC
R9 5.1 K
READ TAPE SHIFT TP5
TP6 CHARACTOR GAP
FF 853 A16-B
846 A15-C
TP4 RECORD GAP
UP TO SPEED
846 A6-B
836 A13-C
CR1 CR2 CR3 CR4
+5VO
R6 470 Ω
836 A18-D
836 A18-B
836 A18-C
WRITE TAPE MODE
WRIT CMD J12-2
READ TAPE SHIFT
ECHO PULSE J12-C
REG 2 RESET
ECHO ERROR *
GAP T2 J6-L, J5-S
J4-E, J8-18 J10-18, J11-J POR * 14
J12-CC, J11-4 (S) 10
OFFLINE A K J4-R(S), J6-N, J11-C
846 A17-B
836 A11-C
836 A11-D
C6 500PF 500V
C7 500PF 500V
MOS CLOCK FF 853 A9-B
846 A17-D
836 A11-A
CLK Ø B F J7-24
836 A11-F
500 KHZ B C J8-F
846 A17-C
836 A11-B
500 KHZ A E J8-9, J7-D
TP8
836 A11-E
CLK Ø A D J7-25
500 KHZ A * 15 J8-K, J7-C
+5V 1 A
GND 2B FF
C9 10 UF 15V
C10 .1UF 10V
C12 .1UF 10V
C14 .1UF 10V
TP1 GND

NOTES:
1. ALL RESISTORS ARE 1/4 W, 5%.
2. ALL DIODES ARE IN914

J13

E	F
FAB REV	ASSY REV

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
.XX ± .XXX ± ANGLES ±

MATERIAL SPECIFICATION:

FINISH SPECIFICATION:

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344-90026

dicom INDUSTRIES INCORPORATED

LOGIC DIAGRAM
TAPE DATA CONTROL

CLASS CODE D SIZE 344-90026 DOCUMENT NUMBER F ISSUE

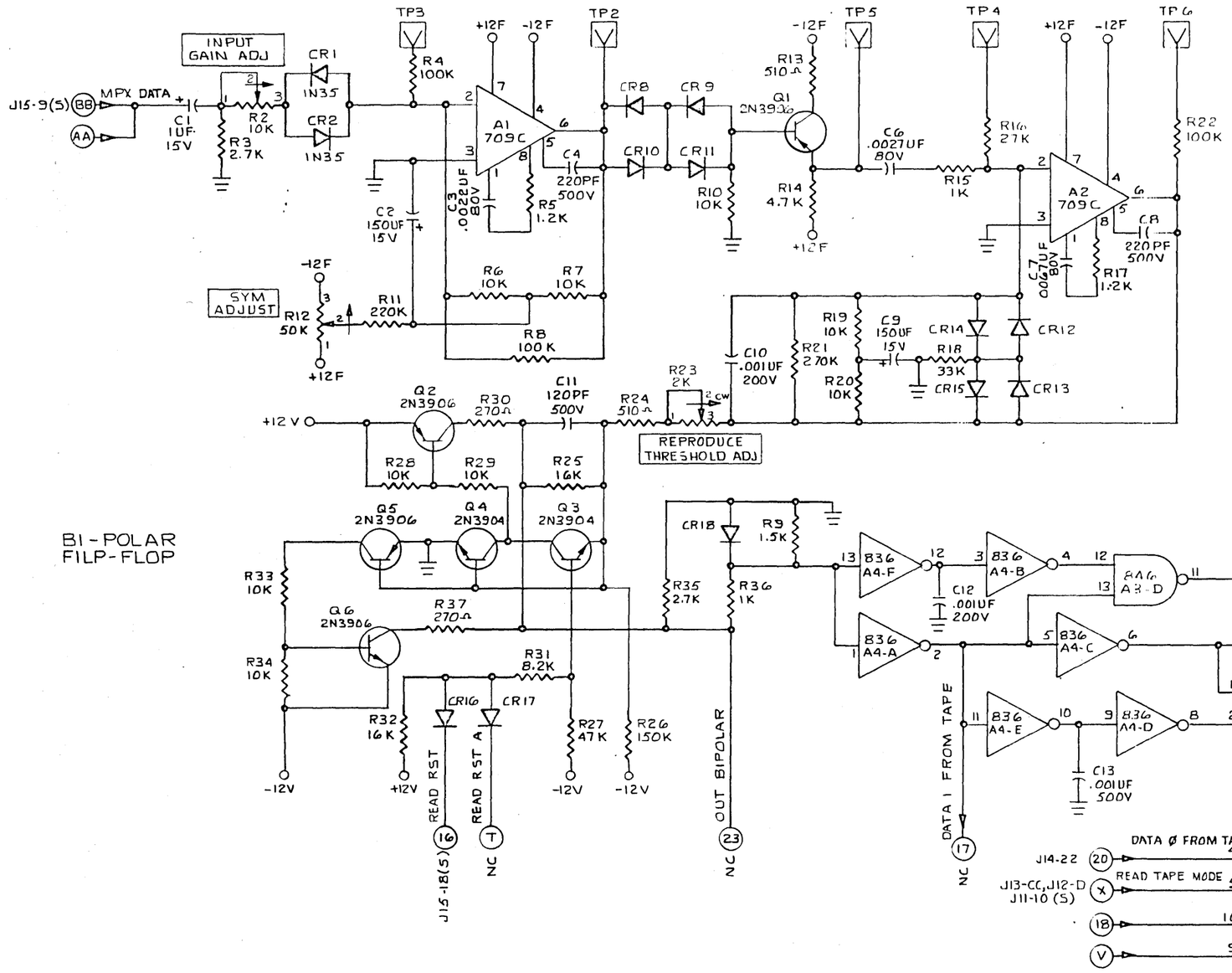
SCALE NONE SHEET 8 OF 12

PRINTED ON DIEPO NO. 1000H-2 CLEARPRINT
FADE-OUT 1-70

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
G	CN 549-1	ALTMAN	3/70		5/20/70

REPRODUCE AMPLIFIER

PEAK DETECTOR



NOTES:
1. ALL RESISTORS ARE 1/4 W, 5%.
2. ALL DIODES ARE IN914.

J14

OUTSTANDING CHANGES				
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. .XX± .XXX± ANGLES±	dicom INDUSTRIES INCORPORATED			
MATERIAL SPECIFICATION: NONE	LOGIC DIAGRAM REPRODUCE			
FINISH SPECIFICATION: NONE	CLASS CODE D SIZE	PART NUMBER 344-90033 DOCUMENT NUMBER	G ISSUE	
DO NOT SCALE THIS PRINT	SCALE NONE	SHEET 1 OF 1		

344-90033

C FAB REV | F ASSY REV

PRINTED ON BRAND NO. 1000H-8 CLEARPRINT

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
G	CN 549-1	ALTMAN	3/70	X Tedrow	5/29/70

WRITE AMPLIFIERS

READ PRE AMPLIFIERS

WRITE I HEAD 3 — TP2

LOW AMP READ DATA 3

WRITE AMPLIFIERS

D3W — J18-9, J1-13 (S) AA
WRITE 1 — J13-25(S) 2
WRITE Ø — J13-19(S) 4

858 A1-C: R1 2.2K, R2 470Ω, CR1, R3 470Ω, R4 2.2K, Q1, Q2
858 A1-D
+12V
R5 3.9K, R6 3.9K, R8 330Ω, R24 1K
TP4 CT REF, TP3 DI PHASE

HEAD A31 — JUMPER — HEAD B31
HEAD A30 — JUMPER — HEAD B30

R10 4.3K, R12 4.3K, R13 3.6K, R14 1K CM REJ
CR2, CR3, CR4, CR5
R23 4.3K
JUMPER — MPX D (3)

709C A4: C1 47PF, C2 240PF, R15 1.5K, R17 470K, R29 100K GAIN, R20 100Ω, TP5
Q3 2N1303
R7 10K — -12F

READ SEL 3 ✱ — J1-19, J5-M (S), J16-21 — 21
858 A1-A: R28 2.2K, R27 470Ω, Q4, +12F
R26 62Ω

D2W — J19-9, J2-13 (S) S
858 A2-C: R30 2.2K, R31 470Ω, CR8, R32 470Ω, Q5, Q6
858 A2-D: R33 2.2K
+12V
R34 3.9K, R35 3.9K, R37 330Ω, R53 1K
TP6

HEAD A21 — JUMPER — HEAD B21
HEAD A20 — JUMPER — HEAD B20

R39 4.3K, R41 4.3K, R42 3.6K, R43 1K CM REJ
CR9, CR10, CR11, CR12
R52 4.3K
JUMPER — MPX D (2)

709C A5: C5 47PF, C6 240PF, R44 1.5K, R46 470K, R58 100K GAIN, R49 100Ω, TP7
Q7 2N1303
R36 10K — -12F

READ SEL 2 ✱ — J2-19, J5-7 (S), J16-11 — 11
858 A2-A: R57 2.2K, R56 470Ω, Q8, +12F
R55 62Ω

DIW — J20-9, J3-13 (S) 3
858 A3-C: R59 2.2K, R60 470Ω, CR15, R61 470Ω, Q9, Q10
858 A3-D: R62 2.2K
+12V
R63 3.9K, R64 3.9K, R66 330Ω, R82 1K
TP8, TP11

TP12
HEAD A11 — JUMPER — HEAD B11
HEAD A10 — JUMPER — HEAD B10

R68 4.3K, R70 4.3K, R71 3.6K, R72 1K CM REJ
CR16, CR17, CR18, CR19
R81 4.3K
JUMPER — MPX D (1)

709C A6: C9 47PF, C10 240PF, R73 1.5K, R75 470K, R87 100K GAIN, R78 100Ω, TP9
Q11 2N1303
R65 10K — -12F

TP10
MPX DATA — 9 J14-BB, 23
R25 2.2K

READ SEL 1 ✱ — J3-19, J5-R(S), J16-H — H
858 A3-A: R86 2.2K, R85 470Ω, Q12, +12FO
R84 62Ω

NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS ARE 1/4 W, 5%.
2. ALL TRANSISTORS ARE 2N3906.
3. ALL DIODES ARE IN914.

POWER SUPPLY DECOUPLING

+12V — 26 DD — R88 27Ω — +12F
C13 20UF 15V, C15 .1UF 30V
GND — 28 FF
C14 20UF 15V, C16 .1UF 30V
-12V — 27 EE — R89 27Ω — -12F

+5V — 1 A — C17 20UF 15V, C18 .1UF 10V — TP1 GND

J15

F	G
FAB REV	ASSY REV

344-90028

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. .XX± .XXX± ANGLES±

MATERIAL SPECIFICATION

FINISH SPECIFICATION

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SCHEMATIC
R/W ELETCTRONICS

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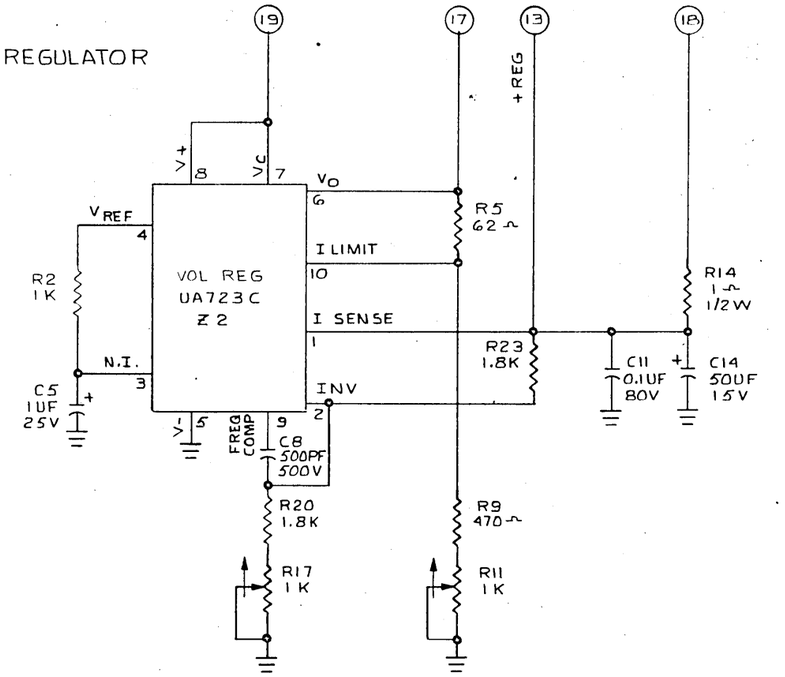
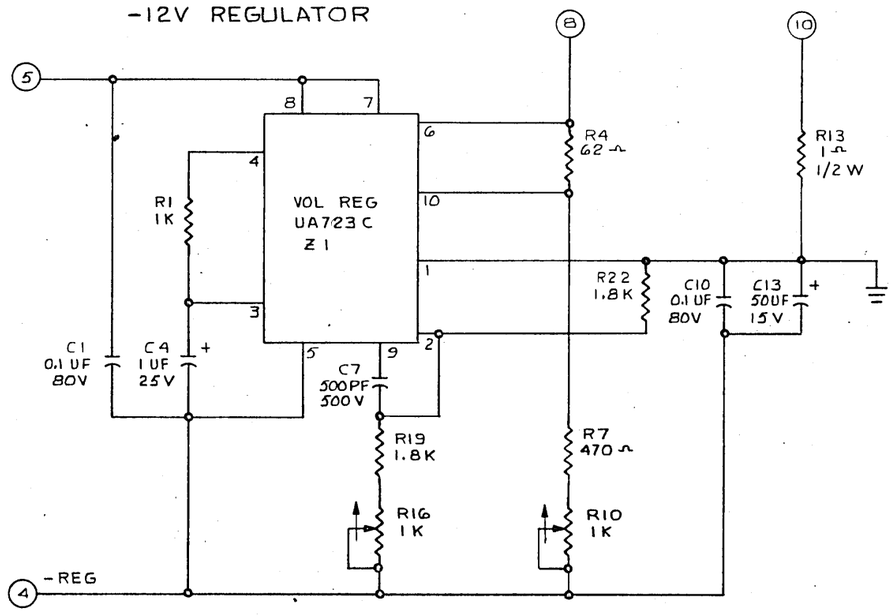
ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
E	CN 549-1	AIMAN	4/70	J. Talmet	5/04/70

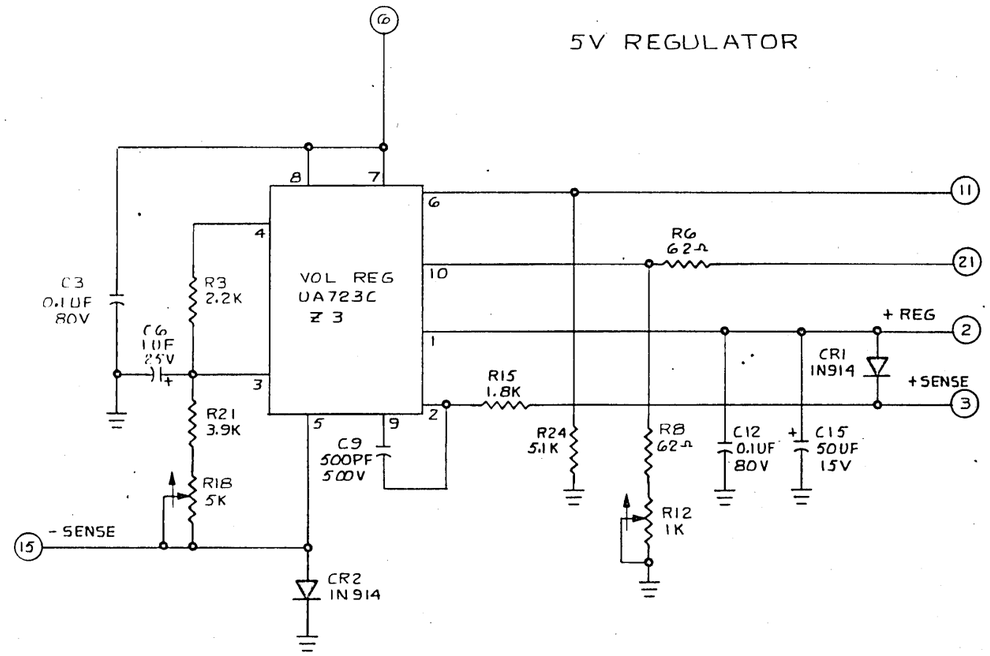
+12V REGULATOR

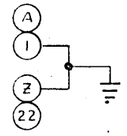


-12V REGULATOR



5V REGULATOR





NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS ARE 1/4W 5%.

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
.XX± .XXX± ANGLES±

MATERIAL SPECIFICATION:

FINISH SPECIFICATION:

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dicom INDUSTRIES INCORPORATED

SCHEMATIC REGULATOR CARD

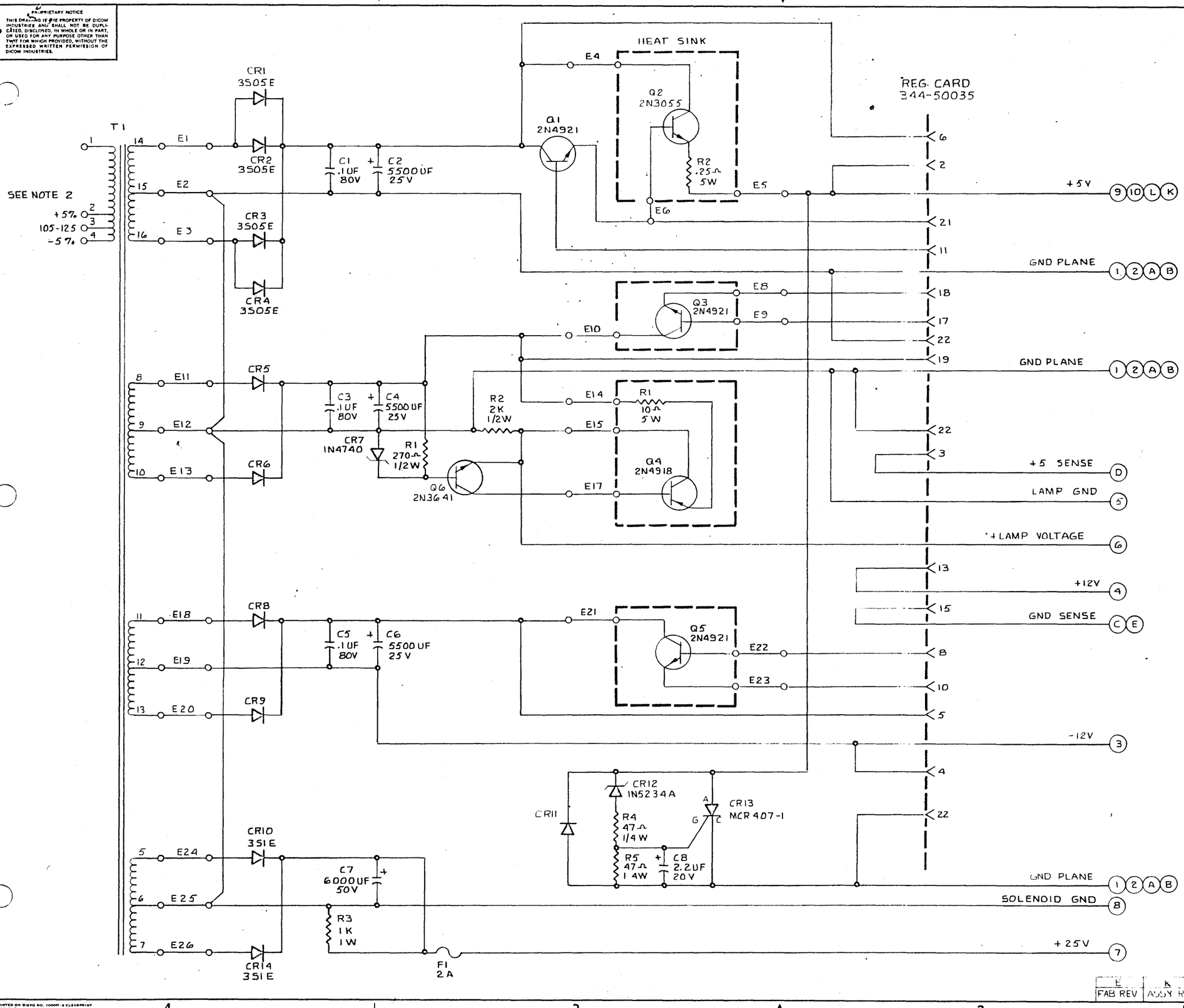
344-90035

C	E
FAB REV	ASSY REV

CLASS CODE D | SIZE | PART NUMBER 344-90035 DOCUMENT NUMBER | ISSUE E | SHEET

SCALE NONE

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
J	CN 549-1	ALTMAN	4-70	E. Tulin	5/20/70



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIODES ARE IN4005
2. ±5% TAPS REFERED TO OUTPUT VOLTAGE

OUTSTANDING CHANGES			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. .XX ±.01 .XXX ±.005 ANGLES ±1°	dicom INDUSTRIES INCORPORATED		
MATERIAL SPECIFICATION	SCHEMATIC POWER SUPPLY		
FINISH SPECIFICATION			
DO NOT SCALE THIS PRINT	CLASS CODE D	SIZE	PART NUMBER 344-90036 J
	SCALE NONE		SHEET 1 of 1

344-90036

E FAB REV	K ASSY REV

PRINTED ON DIEPO NO. 1000H - 6 CLEARPRINT FADE-OUT 1-70

SECTION 6

SYSTEM CHECKOUT PROCEDURE

SECTION 6

SYSTEM CHECKOUT PROCEDURE

6-1 MATERIAL REQUIRED

1. Volt-Ohm-Meter Simpson 360 or equivalent.
2. Oscilloscope, Tektronix type 453 or equivalent.
3. Three each cassette tapes (scratch).
4. One each cassette tape (File Protected).
5. Frequency Counter H/P.
6. Device interfaced ONLINE to the Dicom 344.
7. 5Kc Standard Alignment Cassette Dicom PN 00501.

6-2 SYSTEM GROUND

1. Measure the resistance between the center prong of the AC connector (Power Supply) and the other two prongs using a V.O.M. Verify that an open circuit exists.

2. Measure the resistance between the center prong of the AC connector (Power Supply)and Test Point 1 of any logic module. Verify that an open circuit exists.

6-3 +5 VOLTS

1. Using the oscilloscope, measure the voltage present at J16 Pin 1 (refer to Figure 6-1). Verify the voltage is +5 volts ± 0.25 volts. To adjust this voltage, remove the cover from the Power Supply and rotate R12 (refer to Figure 6-2).

2. Using the oscilloscope, measure the ripple present at J16 Pin 1 (refer to Figure 6-1). Verify that the ripple is less than 20 millivolts. If the ripple is greater than 20 millivolts, the +5 volts may be on the verge of current limiting. To correct, remove the Power Supply cover and rotate R18 (refer to Figure 6-2) until the voltage folds back (drops toward zero) then rotate the potentiometer two full turns in the opposite direction.

6-4 +12 VOLTS

1. Using the oscilloscope, measure the voltage present at J16 Pin 26 (refer to Figure 6-1). Verify that the voltage is +12 volts ±0.6 volts. To adjust this voltage remove Power Supply cover and rotate R11 (refer to Figure 6-2).

2. Using the oscilloscope, measure the ripple present at J16 Pin 26. Verify that the ripple is less than 20 millivolts. If the ripple is greater than 20 millivolts, the +12 volts may be on the verge of current limiting. To correct, remove the Power Supply cover and rotate R17 until the voltage folds back (drops toward zero) then rotate the potentiometer one full turn in the opposite direction.

6-5 -12 VOLTS

1. Using the oscilloscope, measure the voltage present at J16 Pin 27 (refer to Figure 6-1). Verify that the voltage is -12 volts ±0.6 volts. To adjust this voltage remove the Power Supply cover and rotate R10 (refer to Figure 6-2).

2. Using the oscilloscope, measure the ripple present at J15 Pin 27. Verify that the ripple is less than 20 millivolts. If the ripple is greater than 20 millivolts, the Power Supply may be on the verge of current limiting. To correct rotate R16 until the voltage folds back (drop toward zero) then rotate one full turn in the opposite direction.

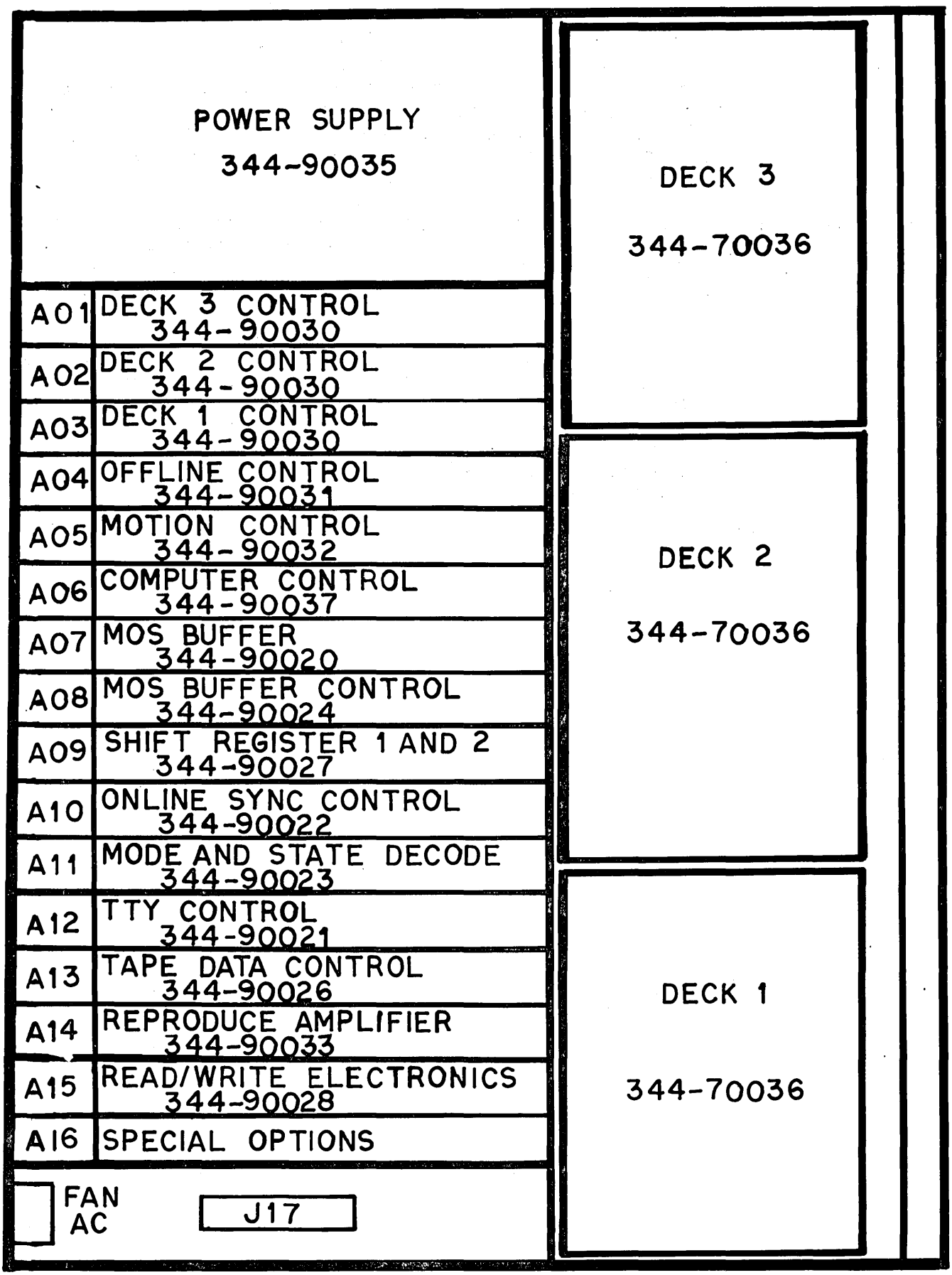

POWER SUPPLY
344-90035
A01 DECK 3 CONTROL 344-90030
A02 DECK 2 CONTROL 344-90030
A03 DECK 1 CONTROL 344-90030
A04 OFFLINE CONTROL 344-90031
A05 MOTION CONTROL 344-90032
A06 COMPUTER CONTROL 344-90037
A07 MOS BUFFER 344-90020
A08 MOS BUFFER CONTROL 344-90024
A09 SHIFT REGISTER 1 AND 2 344-90027
A10 ONLINE SYNC CONTROL 344-90022
A11 MODE AND STATE DECODE 344-90023
A12 TTY CONTROL 344-90021
A13 TAPE DATA CONTROL 344-90026
A14 REPRODUCE AMPLIFIER 344-90033
A15 READ/WRITE ELECTRONICS 344-90028
A16 SPECIAL OPTIONS
FAN AC
J17
DECK 3
344-70036
DECK 2
344-70036
DECK 1
344-70036

FIGURE 6-1

6-6 +31 VOLTS	(Refer to Section 8-1.B for Fuse Replacement.) Check at J1 TP3 with scope (refer to Figure 6-1); should be +29 to +34 V DC.
6-7 +10 VOLTS (LAMP SUPPLY)	Check at J22 Pin 6 (Power Supply connector) with scope; should be +8 to +11 V DC.
6-8 BAUD RATE CLOCKS	Place Unit in OFF-LINE WRITE mode and type on TTY. Sync (+) and monitor at J9 TP4 (Reg 1 Shift). Time should be 99 to 102 milliseconds. If required, adjust J12 R2 for a pulse period of 9.09 milliseconds. To set any other rate use above procedure calculating period as 1/Baud Rate (refer to Figure 6-1).
6-9 MOS BUFFER CLOCKS	(Option 01-02 required). Monitor 500 Kh clocks at J13 TP8 (refer to Figure 6-1). Pulse width should be 400-600 nano sec. Repetition rate should be 1.8 to 2.2 μsec.
6-10 BOT INHIBIT (WRITE)	With the cassette at clear leader and the unit placed in Write, the selected deck should pull 8 to 12 inches of tape past clear leader. Sync (-) (Deck 1) J3 TP2, (Deck 2) J2 TP2 or (Deck 3) J1 TP2 and monitor with scope at J5 TP7 (BOT Inhibit). Time should be 800 to 1200 milliseconds(refer to Figure 6-1).
6-11 BOT INHIBIT (READ)	With the cassette at clear leader and the unit placed in read, the selected deck should pull .4 to .6 inches of tape past clear leader. Sync (-) (Deck 1) J3 TP2, (Deck 2) J2 TP2, or (Deck 3) J1 TP2, and monitor with scope at J5 TP7 (BOT Inhibit). Time from the beginning of the trace to positive change should be 400 to 600 milliseconds (refer to Figure 6-1).
6-12 TAPE WRITE CLOCK	Monitor at J13 TP7 (Tape Clocks) while writing all ones onto tape. The period measured, should be 90 μseconds from negative to positive edges. To adjust the period, rotate R8 on J13 (refer to Figure 6-1).

6-13 WRITE FILE MARK

Using Deck 1, sync (+) and monitor J3 TP13 (Brake) while writing file gaps off-line. Time should be 75 to 90 milliseconds (refer to Figure 6-1).

NOTE: Voltage level at this test point is approximately +30 volts.

6-14 FILE MARK DETECT

Using a test tape which has single file gaps and marks, place the unit in search. Sync(-) J13 TP4 (Gap T2) and monitor J6 TP3 (File Mark Detect). Time difference should be 50 to 60 milliseconds (refer to Figure 6-1).

6-15 TACHOMETER OPERATION VERIFICATION

(Rewind and forward motion failsafe)

6-15.1 Install scratch cassette tape at the end-of-tape in the transport to be tested.

6-15.2 Connect the oscilloscope to TP13 (Brake) of the Deck Control Logic module of the tape transport to be tested. (Refer to Figure 6-1)

6-15.3 Sync the oscilloscope positive on this signal and set vertical amplifier to handle 30 volts DC.

6-15.4 Select OFFLINE and READ for the transport to be tested and observe that the waveform is between 100 and 200 milliseconds.

6-15.5 Select REWIND for the transport to be tested, and using a cotton swab, stall the forward take-up reel. The Rewind sequence should end, i.e., the Rewind Solenoid should de-energize and the Read/Write head should be pulled into place. Perform this test 20 times on each tape transport.

6-15.6 If a failure is noted above, refer to Section 8-9 Tachometer Wiper Contacts Adjustment, Removal/Installation.

6-16 UP TO SPEED (WRITE)

Using ONLINE WRITE on any Deck, sync (+) and monitor J5 TP2 (up to speed delay) while writing onto tape. The time measure should be 24-27 milliseconds (refer to Figure 6-1).

6-17 UP TO SPEED (READ)

Using ONLINE READ on any Deck, sync (+) and monitor J5 TP2 (up to speed delay) while reading from tape. Time should be 3 to 10 milliseconds (refer to Figure 6-1).

6-18 PAPER TAPE TO CASSETTE

(Option 01-02 required). Using OFFLINE WRITE to any tape transport, generate a cassette of long ASCII paper tape (80 lines or more). Rewind and playback onto the TTY using OFFLINE READ. Playback should be identical to input.

6-19 DELETE FUNCTION

Delete Function of the Off-Line Buffer requires Option 01-02. Type a full line of TTY characters, but before the carriage return type a rubout character. Rewind and playback the tape. Verify that the rubbed out record does not appear on the printout.

6-20 OFFLINE MOTION COMMANDS

For OFFLINE WRITE, READ and SEARCH of each deck, place the unit in Write on a deck with a cassette. Using the TTY, generate a series of records followed by a file gap and file mark. Generate 4 files each containing different data. Rewind and check the ability to read and search any one or all of the files. Verify data to input. Repeat on the other two decks.

6-21 WRITE LOCKOUT

Load a deck with a write protected cassette. In the Off-Line mode the selected deck should not be capable of going into write. Repeat on the other two decks.

6-22 DECK 1 LEADER/OXIDE STATUS

(Refer to Appendix C) . Monitor with scope at J27 Pin C. The voltage level should be ground when the cassette in Deck 1 is at clear leader.

6-23 DECK 2 LEADER/OXIDE STATUS

(Refer to Appendix C). Monitor with scope at J27 Pin d. The voltage level should be ground when the cassette in Deck 2 is at clear leader.

6-24 DECK 3 LEADER/OXIDE STATUS

(Refer to Appendix C) Monitor with scope at J27 Pin e. The voltage level should be ground when the cassette in deck 3 is at clear leader.

6-25 OFFLINE STATUS

(Refer to Appendix C) Monitor with scope at J27 Pin h. The voltage level should go to ground as the unit is switched to OFFLINE.

6-26 OFFLINE COMMAND

(Refer to Appendix C) When the unit is in the ONLINE, ground J27 Pin b, the front panel indicator should switch to OFFLINE.

6-27 OFFLINE INITIALIZE

(Refer to Appendix C) with the 344 OFFLINE, ground J27 Pin f. The 344 control panel should indicate ONLINE Halt and DECK Ø selected.

6-28 LONG TERM SPEED VARIATION

Select OFFLINE READ on Deck 1, using the 5KC Standard Tape and monitor with a frequency counter at J14 TP2. Frequency read should be between 5.146 and 5.354KC. Repeat at end of tape. Repeat for all decks.

6-29 INTER FLAG TIME (WRITE)

Using ONLINE WRITE, sync (+) and monitor J6 TP7 while allowing the program to write on any deck. Inter-Flag time should be 2 milliseconds ± 10 microseconds.

6-30 INTER-FLAG TIME (READ)

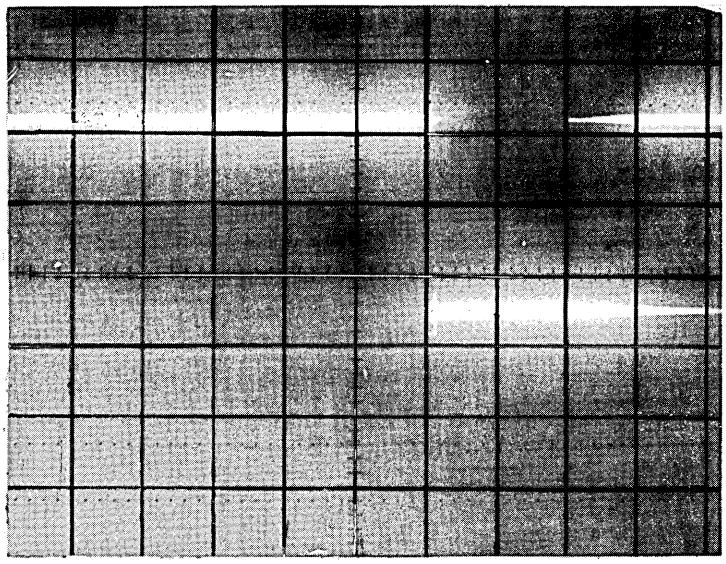
Using ONLINE READ, sync (+) and monitor J6 TP7 while allowing the program to read from any deck. Inter-Flag time should be 2 milliseconds ± 10%.

6-31 DYNAMIC SPEED VARIATIONS

6-31.1 Using an ONLINE copy mode, if available, or a short delay between records (30 to 40 milliseconds) written, Write a tape on each deck to be tested.

6-31.2 Using ONLINE READ mode, sync the scope (-) and observe J13 TP5. With the scope set at 20µsec/cm, the positive edge observed should not vary more than ±14 µsec (refer to Figure 6-31).

DYNAMIC SPEED VARIATIONS



SCOPE: Sync = (+)

Time Base = 20 μsec/cm

Sensitivity = 2v/cm

NOTE: The dynamic speed variations of this tape transport exceed 20 μseconds.

FIG. 6-31

SECTION 7

THEORY OF SYSTEM OPERATION

SECTION 7

THEORY OF SYSTEM OPERATION

7-1 INTRODUCTION

The following paragraphs are explanations of the Dicom 344 Flow Diagrams located in Appendix A. (Table 1 of Appendix A contains definitions of Flow Diagram Symbols).

7-2 POWER ON RESET

(Refer to Appendix A, Page 1) POR (Power on Reset) is used to initialize the Dicom 344 when power is first applied; i.e., the ONLINE mode, Deck Zero and Halt modes are selected, similar to the INITLZ-I command. The POR pulse is generated on J13 and is routed to J10, J4, J7, J11 and J8. The POR generates the SEND DATA RESET signal which resets the SEND DATA Flip-Flop. POR also causes REC to go low, which causes the data in the buffer to be lost. The STATE COUNTER is cleared on J11, as are both LOAD SOB Latch and LOAD SOB1 Latch. On J8 the STOP REC Latch and ANY SOB Latch are cleared. POR OR's with ONLINEPB* and INITLZ-I on J4 which sets to one, the ONLINE Latch on J4 and resets to zero, the D(n) Write Latch on J1, 2 or 3 and Deck SEL A, DECK SEL B, BOTINH, READE and WRIT Latches on J5. The trailing edge of POR* causes PORP on J11, which is ANDed with BURST + OFFLINE, OR'd with DELSS* and OFFLINE + BURST (refer to Section 7-5).

7-3 ONLINE INITIALIZE, INITIALIZE COMMAND

(Refer to Appendix A, Page 1) The Online Initialize and Initialize Command are used to place the Dicom 344 in a quiescent condition after power has been applied. (POR is used to establish a quiescent condition upon application of power.) This quiescent condition can be accomplished by pressing the Front Panel ONLINE Push Button when in the OFFLINE mode or by sending the INITLZ-I command from the computer when in the ONLINE mode.

ONLINE PB*, INITLZ-I and POR are OR'd on J4. This OR'd signal sets the ONLINE Latch on J4 which in turn inhibits the MOS clock (which is enabled in the OFFLINE mode only) on J13. The ONLINE PB*, INITLZ-I and POR OR'd signal also generates the INIT and INIT* signals on J4 which resets the D(n) WRITE latch on J1, 2 and 3, and the DECK SEL A, DECK SEL B, BOTINH, READE, WRIT latches on J5.

7-4 HALT COMMAND

(Refer to Appendix A, Page 1) The HALT Command is used to generate the signal HALTP* which causes the tape transport to stop motion, and resets mode latches. HALTP* is generated by three different logic sources. One logic source is from J4 (during POR*, or entering the Initialize mode, or pressing the ONLINE push button) (refer to Section 7-3). The second logic source is sensing lack of tape motion by the tachometer on the tape transport and generated on J1, J2, or J3 (refer to ballon 2F Appendix A, Page 2). The third logic source is generated on J6 by being in the ONLINE mode (OFFLINE) and the Halt Command, (HALTC-I and CMDT-I) being issued by the Online device.

7-4.1 The HALTP* is inverted on J5 to become HALTP which resets the READE and WRIT Latches on J5, the REWIND and DECK (n) WRITE Latches on J1, J2, and J3 and the FLMK, ERROS and FLAGS latches on J6.

7-4.2 The uninverted HALTP* signal resets the SEND DATA RST Latch on J12. It also generates DELETE SS* (a single shot of 300 microseconds) which generates (REC)that blocks the MOS Buffer from recirculating.

7-4.3 DELETE SS* is OR'd with the output of an AND function of PORP* (Power on Reset Section 7-2) and BURST + OFFLINE and OFFLINE + BURSTP (Offline Initialize Section 7-5) on J11.

7-4.4 The output of this OR function sets the LOAD SOB1 Latch. The LOAD SOB1 allows the code for the Start of Block 1 to be loaded into the MOS Buffer. (This code is Bit 8 (Ø), Bit 9 (1), Bit 10 (Ø)). The LOAD' SOB1 Latch output generates ANY SOB* and LOAD SOB1 on J11. The LOAD SOB1 signal generates SOB1 IN* which is ANDed with NEW DATA on J7 which in turn loads a Zero into MOS bit 8. LOAD SOB1 is ANDed with LAST CHAR* and 500 KHZ* to set the NEW DATA ENABLE Flip-Flop on J8. The output of the NEW DATA ENABLE F/F is ANDed with ANY SOB* false. In the loading of the Start Of Block, ANY SOB* is true which enables the 9th REC BIT and 10th REC BIT.

7-4.5 The loading of the SOB1 code into the MOS buffer is performed by NEW DATA causing BIT 9 to be loaded with a "ONE". NEW DATA ANDed with ANY SOB*

causing BIT 10 to be a "ZERO". SOB1 IN* ANDed with NEW DATA causing BIT 8 to be loaded with a "ZERO".

7-4.6 The significance of the MOS Buffer Bits 8, 9, and 10 are:

8 = Ø	9 = Ø	10 = Ø	No Significance
8 = 1	9 = Ø	10 = Ø	No Significance
8 = Ø	9 = 1	10 = Ø	Start of Block 1
8 = 1	9 = 1	10 = Ø	Start of Block 2
8 = X	9 = Ø	10 = 1	First Character
8 = X	9 = 1	10 = 1	Last Character

7-5 OFFLINE INITIALIZE

(Refer to Appendix A, Page 1) OFFLINE INITIALIZE is generated by pressing the OFFLINE push button or issuing the OFLNC-I from the On-line device. OFFLINE PB* and OFLNC-I are OR'd on J4 to set the OFFLINE Latch. The output of the OFFLINE Latch (OFFLINE*) is OR'd on J11 with the BURST to produce the signal OFFLINE + BURST (exit ballon H). This signal is OR'd (on J11) with BURST+OFFLINE and DELETE SS* to set to "One", the LOAD SOB1 latch. (Refer to Section 7-4.4.)

7-6 TYPE MODE

The signal TYPE MODE is generated by ANDing WRITE and OFFLINEA, OR by ANDing DO*, READA and $\overline{\text{OFFLINE*}}$ on J11.

7-6.1 At J12 TYPE MODE is ANDed with $\overline{\text{CNTR1=9*}}$ and creates TTY CLOCK GATE* which allows the TTY CLOCK oscillator to run. Every other TTY CLOCK causes CNTR1 to advance and also generates SHIFT REG 1 which loads serially the TTY Keyboard Data input.

7-6.2 If, prior to entering TYPE MODE, tape data had been assembled, the state of CNTR1 would equal eight so that two TTY CLOCKS will occur to bring the state of CNTR1=9*. This advance in CNTR1 is disallowed as a data transfer by the CNTR1=9 Latch. This latch sets the first time CNTR1=9* occurs and remains set throughout TYPE MODE.

7-6.3 SDR* (Serial Data Received) from J14 and TYPE MODE are ANDed at J9. If CNTR1=9* is true, this is the start bit from the TTY keyboard which causes CNTR1 RST* to occur and is sent to J12. This clears CNTR1 to "Zero" causing $\overline{\text{CNTR1=9*}}$ and starts the TTY CLOCK. SDR* and TYPE MODE also act as the data input gate to REG 1.

7-6.4 As noted before, every other TTY CLOCK creates a SHIFT REG 1 on J9 to load the serial data bit at the input and shift all prior bits up. Every other TTY CLOCK also causes an increment in CNTR1 on J12. When

CNTR1 reaches nine CNTR1=9* , TTY CLOCKs are stopped as all significant bits from the keyboard are stored in REG 1 and CNTR1=9* is ANDed with TYPE MODE and CNTR1=9 latch to generate TTY TAKE DATA SET pulse. This pulse goes to J10 and sets the TAKE DATA flip-flop generating TAKE DATA. TAKE DATA indicates that the serial data has been assembled and is now ready for parallel transfer which exits ballon D, Page 2.

7-7 PRINT MODE

(Refer to Appendix A, Page 2) PRINT MODE will be entered in either OFFLINE AND READ or ONLINE AND WRITE. Both of the above configurations require data be output to the Offline device.

7-7.1 (Refer to Appendix A, Page 4, ballon H) OFFLINEA ANDed with READA, OR (Refer to Appendix A, Page 3, ballon E) ONLINE WRITE ANDed with DØ* will create PRINT MODE at J11.

7-7.2 On J12 PRINT MODE is ANDed with the state of the SEND DATA RESET Latch to generate TTY CLOCK GATE* when the Latch is set=1.

7-7.3 TTY CLOCK GATE* allows the TTY Clock oscillator to create TTY CLOCKs. These clocks are ANDed with PRINT MODE to create TTY clock A* and TTY CLOCK B*.

7-7.4 TTY CLOCKA* is compared with the state of CNTR2=1Ø. If CNTR2=1Ø is true and the FLAG ENABLE Latch is set (Refer to Appendix A, Page 3, ballon J) the SEND DATA RESET Latch will be reset which disallows TTY CLOCK GATE*. At CNTR2=11, CNTR2 will be reset to all zeros.

7-7.5 TTY CLOCK B* causes CNTR2 to be incremented at each occurrence. It is also compared to the state of CNTR2=N&T* (counter 2 = Nine or Ten) to shift Reg 2 on J9 up which places a new REG 2 SB* to be sent to J12. REG2 SB* is ANDed with PRINT and TTY CLOCK GATE to generate TTY FEEDBACK.

7-7.6 TTY FEEDBACK is sent to J4 to either create a current loop PRINT (-), or RS232B PRINT (-).

7-8 ONLINE/ OFFLINE WRITE

(Refer to Appendix A, Page 3) The following signal flow generates the Write sequence in either the ONLINE or OFFLINE Modes.

7-8.1 When the WRITE push button is pressed in the OFFLINE mode, the signal WRITEPB* is generated on J4. This output is ANDed with HALT* and OFFLINE to generate WRITP* on J5. When the WRITC-I is issued by the Online device to J6, it is ANDed with CMDT-I (also issued by

the Online device) thus generating WRITP*. WRITP* will create the pulse WRITP+WFMP which is generated on J6 and sent to J1, J2, or J3 (refer to Section 7-9 WRITE FILE GAP MODE for further explanation).

7-8.2 WRITP* is ANDed with the Write Lock Switch, $\overline{\text{DWLOS*}}$ on J5 which sets the WRIT Latch. The output of the latch (WRIT) generates IMOT (ballon 2B), UP TO SPEED DELAY (ballon B) and is ANDed with DL/OXS* to generate BOT INH (ballon C).

7-8.3 The output of the WRIT Latch also generates WRITE which inhibits the FLMK Detect circuitry on J6, and is ANDed with OFFLINE on J4 to inhibit the front panel switches. WRITE also causes WRITE* on J11.

7-8.4 WRITE* generates WRITEA which is ANDed with OFFLINEA to cause TYPE MODE to occur (ballon D).

7-8.5 WRITE* is also ANDed with TTY CLOCK GATE on J12 which causes INH STATE ADV* to be generated (ballon H).

7-8.6 WRITE* is ANDed with ONLINE and $\overline{\text{BURST + OFFLINE*}}$ on J10 to generate the pulse CNTR2RST*. This pulse is OR tied with the SEND DATA SET* pulse on J9 which resets REGISTER 2. The OR'd output of the CNTR2RST* or SEND DATA SET* pulse will reset Counter 2 and set the SEND DATA Flip-Flop on J10. The setting of SEND DATA Flip-Flop signifies that the Input (Reg 1) Register is ready to receive a new character.

7-8.7 WRITE* is also ANDed with ONLINE, CNTR2=9 and the CLOCKA pulse (which is generated by an OR of the TTY CLOCK and TAPE CLOCK) thus causing the SEND DATA SET* pulse to occur. Whenever the Output (Reg 2) Register has completed the serial data transfer, this pulse resets the FLAG ENABLE latch and OR's with the CNTR2 RST* pulse (Section 7-8.6).

7-8.8 WRITE is ANDed with $\overline{\text{OFFLINEA*}}$ (signifying the device is in the WRITE ONLINE MODE) to generate the signal ONLINE WRITE on J11.

7-8.9 ONLINE WRITE is ANDed with the CMDT (that set the present mode) to set WRITE STROBE ENABLE flip-flop on J10. Also on J10 the leading edge of ONLINE WRITE causes the pulse SET RDY FLAG*, which goes to J6 to set the FLAGS Latch. The true side of this latch is ANDed with $\overline{\text{OFFLINE*}}$ and STATT-1 to create FLAGS-1. The Online device will answer FLAGS-1 with an NDATT-1 strobe and the 8 bit data character to be written.

NDATT-1 goes to J10 and is inverted and sent to J5 to create FLAGR* which is sent to J6 to reset FLAGS Latch. NDATT-1 is also ANDed with WRITE STROBE ENABLE to generate INPUT STROBE which is sent to J9 to gate the 8 bit data character into REG 1. It also sets the TAKE DATA flip-flop to indicate that REG 1 has been loaded with new data. TAKE DATA is ANDed with SEND DATA (refer to Section 7-8.6) to cause DATA TRANSFER STROBE pulse. Data Transfer Strobe pulse is ANDed with ONLINE WRITE at J10 to cause REG 1 to be transferred to REG 2 on J9 and REG 1 is reset. SET RDY FLAG is also generated which exits ballon F . The TAKE DATA and SEND DATA flip-flops are reset, the SEND DATA RESET pulse goes to J12 to set both the SEND DATA RESET Latch, and the FLAG ENABLE Latch.

7-8.10 ONLINE WRITE on J11 is ANDed with DO* which generates PRINT MODE that exits to the TTY PRINT flow on Page 2 ballon K . It is also ANDed with $\overline{DO*}$ which generates the level WRITE TAPE MODE.

7-8.11 WRITE TAPE MODE goes to J13 and is ANDed with UP TO SPEED (refer to Appendix A, Page 2) to create WRIT CMD. WRIT CMD is ANDed with SEND DATA RESET (L) on J12 generating TAPE CLOCK GATE. TAPE CLOCK GATE at J13 allows the TAPE CLOCK oscillator to run. The output of this oscillator is divided by 2 with one-half of the clocks called TAPE CLOCKA, the other half TAPE CLOCK B.

7-8.12 TAPE CLOCK A, the first clock to occur after TAPE CLOCK GATE, is ANDed with $\overline{CNTR2=8*}$ OR WRITEØ AND $\overline{CNTR2=N+T*}$ which allows the WRITE Flip-Flop on J13 to be complemented every time TAPE CLOCKA occurs until CNTR2= exceeds the count of eight. This always causes a flux reversal to be written on tape. TAPE CLOCK A* also goes to J10 and is OR'd with TTY Clock A* to create CLOCK A*. CLOCK A* goes to J10 and is ANDed with CNTR2=10 and FLAG ENABLE Latch reset, (which means a new character was not placed in REG 1). This causes the WRITE flip-flop to be reset and is ANDed with $\overline{OFFLINEA*}$ to generate WRITR* (WRITE RESET) which goes to J5 to reset the WRIT (L) causing 1MOT to go false. WRITR* also generates the pulse FLAGR* to reset FLAGS Latch on J6.

7-8.13 TAPE CLOCK B increments CNTR1 on J12 and is ANDed with $\overline{CNTR2=8*}$ AND $\overline{CNTR2=N+T*}$ to load the data bit to be written on to tape into the WRITE flip-flop. This is accomplished by two AND conditions; if ODATØ is true, the WRITE flip-flop is set, if REG 2 BIT1* is positive, the WRITE flip-flop is reset. If the data setting or resetting the WRITE flip-flop caused it to change state, then a flux change is written on tape.

TAPE CLOCK B is ANDed with $\overline{\text{CNTR2=N+T}}$ which generates REG2SHIFT that causes REG 2 on J9 to shift up and the bit presently being written to be lost from the Register. Finally TAPE CLOCK B is ANDed with CNTR2=11 and will create CNTR2 RESET which means a full character is now written on tape with the three bit cell time character gap.

7-9 ONLINE/ OFFLINE FILE GAP WRITE

(Refer to Appendix A, Page 3) The File Gap circuitry can be enabled in the ONLINE Mode by either issuing the FLMKC-1 only, or by issuing FLMKC-1 and WRITC-1 simultaneously, accompanied by CMDT-1. (Refer to Section 3-8.2 WRITE FILE GAP MODE) In the OFFLINE mode the File Gap circuitry can be enabled by pressing and holding the OFFLINE switch and momentarily pushing the WRITE switch on the switch panel (refer to Section 3-7.6).

7-9.1 When in the OFFLINE mode, the signal WRITEPB* is ANDed with HALT* and OFFLINEPB* to generate the pulse, WFMP*. The WFMP* pulse sets the WRITE FILE MARK latch which triggers WFM DLY for 75 milliseconds before resetting the WRITE FILE MARK latch. The output of the latch generates WFM* which in turn causes 1MOT on J5. The Setting of the WRITE FILE MARK (for 75 msec) generates WFM* which causes $\overline{\text{Up To Speed}}$ and 1MOT (ballon 2A) (refer to Appendix A, Page 2) to occur. WFMP is also OR'd with WRITP to create WRITP + WFMP (see further explanation below).

7-9.2 In the ONLINE mode if FLMKC-1 only is issued by the Online device, it will be ANDed with CMDT-1 (also issued by the Online device) to generate the WFMP* pulse which is OR'd with WRITP to create WRITP + WFMP. This pulse is sent to J1, J2, and J3 to set the selected DECK(n) WRITE (L) (allowing Write Head current to flow). On J1, J2, or J3, TP9 indicates the state of the DECK (n) WRITE Latch (Positive=Set).

7-9.3 The latch being set creates the level D(n)W which enables the Write Head Driver on J15. The Write Drivers allow current at the Read/Write head to flow: the "1" direction WRITE=1 (WRITE is the write data flip-flop) or flow in the "Ø" direction WRITE=Ø.

7-9.4 The Output of the DECK (n) WRITE Latch is also ANDed with D(n)* to generate WRITS* which is OR'd with DO* AND WRITE, then ANDed with OFFLINE* and STATT-1. The output of this AND function causes the signal WRITS-1 to be issued to the Online device.

NOTE: If the simultaneous commands of WRITC-I and FLMKC-I had been received, the logic would have entered the WRITE FLOW as soon as the level UP TO SPEED had come true IMOT would have remained true because the WRIT (L) was set.

7-10 OFFLINE/ ONLINE READ

(Refer to Appendix A, Page 4)

7-10.1 The Read circuitry can be enabled in the OFFLINE mode by pressing the READ switch which generates READPB* on J4. READPB* is ANDed with HALT* and OFFLINE to cause the READP* pulse to occur.

7-10.2 In the ONLINE mode the Online device issues READC-I which is ANDed with CMDT (also issued by the Online device) causing the READP* pulse to be generated. READP* can also be generated by the Search mode (refer to Section 7-11).

7-10.3 READP* resets the DECK (n) WRITE latch on J1, J2, or J3 and the TAKE DATA flip-flop on J10, and also generates the READP pulse on J5 (exiting ballon I).

7-10.4 READP* also clears the FLAGS latch by generating FLAGR* at J5 (exiting ballon E) and sets the Latch which generates the level READE.

7-10.5 READE generates IMOT (ballon 2A), Up To Speed Delay (exit ballon B to Page 2) and when ANDed with DL/OXS* causes BOT INH to occur (ballon C Page 2).

7-10.6 READE can also be generated by SRCH* (refer to Section 7-11). READE is responsible for holding the READ MODE within the logic. READE generates the signal READLP* on J4 which illuminates the READ indicator on the Front Panel.

7-10.7 READE generates READ* on J11 which in turn causes READB to occur on J10. READB is ANDed with the OUTPUT STROBE pulse (exiting ballon L) generated by ODATT-I, and ONLINE to cause the pulse CNTR2 RST* to occur. The CNTR2 RST* pulse will also be generated by the leading edge of READ* being ANDed with WRITE* AND BURST + OFFLINE* AND ONLINE when the READ or WRITE mode is first entered on J10. The CNTR2 RST* pulse resets the CNTR2 flip-flop, and resets the Reg 2 (output register) flip-flops.

7-10.8 READE generates READA on J11 which is ANDed with OFFLINE to enable PRINT MODE (ballon H Appendix A, Page 2), ANDed with DØ* and OFFLINE to enable TYPE MODE (ballon F Appendix A, Page 2) and READA is ANDed with OFFLINE + DO* to enable READ TAPE MODE (exit ballon D).

7-10.9 The change of state of READ TAPE MODE generates the CNTR1 RST* pulse on J13 which is sent to J9 and resets the REG 1 flip-flops (input register).

7-10.10 READE (at the time the CMDT-1 pulse occurs) with DECK(n) SEL and READP (enter ballon 1) loads READ SELA and/or READ SELB. The outputs of these latches generate READ SEL (n)* which is ANDed with D(n)* (Deck Select) (refer to Appendix A, Page 2) on J1, J2, or J3, thus generating DREADS which is sent to J6. DREADS also is enabled by ANDing READE and DØ*. DREADS when ANDed with OFFLINE* and STATT-1 enables READS-1 status to be placed on the Online Cable.

7-10.11 If READ SEL(n)* designates deck 1, the gain adjustment of R87 controls the READ DATA for deck 1 (refer to Section 8-4.3).

7-10.12 If READ SEL(n)* designates deck 2, the gain adjustment of R58 controls the READ DATA for deck 2 (refer to Section 8-4.3).

7-10.13 If READ SEL(n)* designates deck 3, the gain adjustment of R29 controls the READ DATA for deck 3 (refer to Section 8-4.3).

7-10.14 The READ DATA outputs are multiplexed and become MPX DATA (observed at TP10 and should be approximately 1.2 to 1.6 V AC peak/peak). This analog signal is sent to the REPRODUCE AMPLIFIER J14 (observed at TP2 and should be approximately 16 V AC peak/peak and is adjusted by R2. Refer to Section 8-4.5). The output is then fed through a Peak Detector which generates positive (zeros) and negative (ones) pulses. These pulses cause the Bipolar flip-flop to change to the proper logic state. The Bipolar Flip-Flop is held in the zero state by the level READ RST an OR of BOT INH* + UP TO SPEED + T1 TIME*READE (refer to Appendix A, Page 2). When READ RST is low, the Bipolar flip-flop is allowed to toggle, creating TAPE DATAØ* and the READ TAPE CLOCK pulse sent to J13.

READ DATA CLOCK* starts and clocks the READ sequence. The first one to occur sets the REG1 RST SYNC flip-flop which causes CNTR1 RST* clearing CNTR1 to all zeros. This allows resyncing the counter at each new character.

7-10.15 READ DATA CLOCK* is ANDed with CNTR1=8. READ TAPE MODE • UP TO SPEED. The output of this AND (J13 TP3) sets the READ TAPE SHIFT Delay (this delay is adjustable and should be set as per Section 8-4.5). At the end of 125 µseconds the READ TAPE SHIFT Delay times out, causing READ TAPE SHIFT*.

7-10.16 READ TAPE SHIFT* is ANDed with READ TAPE MODE on J12 (entering ballon D) to create REG 1 SHIFT*.

7-10.17 REG 1 SHIFT* causes CNTR1 to increment by one and is sent to J9 for two functions. First, it shifts all prior data bits stored in REG 1 up on place. Second, (exiting ballon T) it is ANDed with READ TAPE DATA Ø*. To load the lowest Flip-Flop of REG 1 with a "one", READ TAPE DATAØ* would load this Flip-Flop with a "zero".

7-10.18 Going back to READ TAPE SHIFT* (exiting ballon M), we find it is being timed by two integrating single shots. GAP T1 is timing out for 450 μseconds and if READ TAPE SHIFT* should be absent for this length of time or greater, the timer times out causing T1 TIME* pulse and READ TAPE TAKE DATA SET*.

7-10.19 T1 TIME* goes to J5 to create READ RST and (entering ballon R) is ANDed with the state of CNTR1 to determine whether the count was eight CNTR1=8*. If the counter was not at eight, an error occurred and ERROR FLAG* occurs,which is sent to J6 to set ERRØS Latch (J6 TP2). The output of this Latch is gated by OFFLINE•STATT-1 to create ERROS-1 on the Online Cable.

7-10.20 ERROR FLAG* could be set by an AND of READ DATA CLOCK•REG 1 RST SYNC*•CNTR1=8*•READ TAPE DATAØ which indicates the number of flux reversals was not an even number.

7-10.21 READ TAPE TAKE DATA SET* (refer to paragraph 7-10.18) will set the TAKE DATA Flip-Flop and is ANDed with the output of the TAKE DATA Flip-Flop to determine whether the last character assembled was taken by the Online device. If TAKE DATA was set when READ TAPE TAKE DATA SET* occurs, then TAKE DATA ERROR* is sent to J13 to create ERROR FLAG* which is explained in 7-10.19.

7-10.22 TAKE DATA Flip-Flop set, is ANDed with BURST + OFFLINE* AND SEND DATA (entering ballon Q) to generate DATA TRANSFER STROBE.

7-10.23 DATA TRANSFER STROBE transfers the contents of REG 1 (the 8 bit character just assembled) to REG 2 and creates the following pulses; REG 1 RST*, which is sent to J9 to clear REG 1, and SEND DATA RST*.

7-10.24 SEND DATA RST* is sent to J12 to set the SEND DATA RESET Latch (J12 TP8) and to set the FLAG ENABLE Latch (J12 TP5). SEND DATA RST*, on J10, clears both SEND DATA and TAKE DATA Flip-Flops.

7-10.25 SEND DATA RST* is gated against the state of DØ* (Deck Ø Selected). If any deck other than Deck Ø is selected (DØ*), then SEND DATA RESET GATED occurs immediately. However, if DØ* is low, TTY FLAG DLY is started; at the end of 12 mseconds when the Delay times out, SEND DATA RST GATED will occur.

7-10.26 SEND DATA RST GATED is ANDed with FLAG ENABLE (entering ballon K) AND ONLINEA AND READB (entering ballon T) to generate SET RDY FLAG* on J10.

7-10.27 SET RDY FLAG* is sent to J6 and sets the FLAGS Latch (J6 TP7).

7-10.28 FLAGS Latch being set, is ANDed with $\overline{\text{OFFLINE}}$• STATT-I to create FLAGS-I on the Online Cable. FLAGS-I exits ballon Y to the top of the page.

7-10.29 The Online device sensing FLAGS-I will issue ODATT-I indicating that the character stored in REG 2 is being ingested by the Online device.

7-10.30 ODATT-I is ANDed with ONLINE FLAG ENABLE to generate OUTPUT STROBE. ODATT-I is inverted on J10 and is sent as ODATT to J5 to create FLAGR*.

7-10.31 FLAGR* is sent to J5 to reset the FLAGS Latch. FLAGR* was also generated by READP* entering ballon E .

7-10.32 OUTPUT STROBE (refer to INTERFACE SIGNAL MODIFICATION Section 4-2.4.C) can be used optionally to strobe the eight bit character stored in REG 2 onto the Online Cable as ODAT(n)-I.

7-10.33 OUTPUT STROBE also exits ballon L and is ANDed with READB AND ONLINE to create CNTR2 RST* which clears Counter 2 on J12, sets SEND DATA flip-flop and generates REG 2 RST* pluse which clears to "zero" the REG 2 flip-flops on J9.

7-10.34 If READ TAPE SHIFT (entering ballon M) is absent greater than the GAP T2 timer (1.1 msec.) GAP T2 and GAPT2P is generated.

7-10.35 GAP T2P sets the FLMK ENAB Latch on J6 (exit ballon X) and is ANDed with $\overline{\text{SRCH}}$* and ONLINE* to reset the READE Latch.

7-10.36 GAP T2 is ANDed with IMOT, $\overline{\text{WRITE}}$ and FLMK ENAB to allow the FLMK DETECT circuit to time for 50 milliseconds in order to detect the File Gap. The Circuit, when allowed to time out sets the FLMK Latch (ballon W) indicating a File Gap was detected on tape.

7-11 SEARCH FLOW

(Refer to Appendix A, Page 4) SEARCH mode can be entered by pressing and holding the OFFLINE push button and momentarily pushing the READ push button. This causes READPB* OFFLINE* AND HALT* to be true on J4 to generate READP*. READP* is then sent to J6 where it is ANDed with OFFLINEPB* to set SRCH Latch.

7-11.1 In the ONLINE mode, SRCHC-I is issued by the Online device along with CMDT-I to generate READP*.

NOTE: The SEARCH and READ mode operation is basically the same except that only a File Gap and another Record Gap will terminate the SEARCH MODE.

7-11.2 Upon detection of SRCH-I and CMDT-I in the ONLINE mode, SRCH Latch is set and the signal SRCH* is created (ballon A). SRCH* forces READE true and holds the STATE CNTR to "Zero" on J11. (Refer to Appendix A, Page 5.) This prohibits all data being output from the MOS buffer during OFFLINE SEARCH mode.

7-11.3 The READP* is also generated by the detection of a File Gap (ballon J). When the FLMK Latch sets,the RFG* Pulse is generated which causes READP*. This allows reading the record following the File Gap. FLMK (enterin (entering ballon W) and GAPT2 on J6 will cause HALTP* (exiting ballon Z) (refer to Appendix A, Page 1).

7-12 MOS BUFFER

(Refer to Appendix A, Page 5)

7-12.1 Loading data into the buffer beings by placing the Dicom 344 OFFLINE and selecting the mode. (Refer to Table 3-1, Page 3-11).

7-12.2 When the Dicom 344 is placed OFFLINE or Power On Reset occurs or DELETE* is detected, SOB1 is loaded into the buffer (SOB indicates Start Of Block). SOB1 is loaded so that the dynamic, recirculating shift register has a beginning point. SOB1 utilizes the 8th, 9th, and 10th bits in the MOS Buffer. As the buffer can only store an 8 bit character, bits 9 and 10 are used for data location identification in the buffer. The codes and loading sequence of SOB1 are covered by the test in Section 7-4.4.

7-12.3 The significance of the various codes loaded into the buffer (bits 8, 9, and 10) are shown on Appendix A, Page 5.

7-12.3.A SOB1 indicates the Start Of Block 1 and recirculates until one of the OR conditions in 7-12.2 occurs, or Block 2 terminates.

7-12.3.B SOB2 indicates the Start of Block 2. It is

loaded at the end of Block 1 whenever it terminates. SOB2 recirculates until Block 1 has been loaded and again terminates.

7-12.3.C LAST CHARACTER indicates that the present character being loaded in the block is the Last Character. As each new character is input to the buffer, the Last Character code is removed from the character presently in the buffer and inserted on the character being loaded.

7-12.3.D When the ASCII Carriage Return code (015 octal) is located at the output of the buffer, the STATE COUNTER is advanced by STATE ADV* which causes the presend loading block to terminate.

7-12.3.E FIRST CHARACTER indicates that it is the next character to be unloaded. When the unloading SOB is detected, the First Character code is simulated and the next character following the unload SOB code is unloaded. The character following the unloaded character has the First Character code written in bits 9 and 10.

7-12.3.F When the unloaded character has been output to the OFFLINE device, the recirculating buffer will move the First Character code to the output of the buffer where it is detected and that character is unloaded. The next sequential character then is loaded with the First Character code.

7-12.4 (Refer to Appendix A, Page 5) LOADING of data into the buffer starts with the TAKE DATA flip-flop being set. TAKE DATA could have been set by TTY TAKE DATA SET* (OFFLINE WRITE) or by READ TAPE TAKE DATA SET*, (OFFLINE READ).

7-12.5 The count presently loaded into the State Counter will control which SOB is to load and which SOB is to unload. The STATE COUNTER states have the following meanings:

Ø = LOAD SOB 1
1 = LOAD SOB 2; UNLOAD SOB 1
2 = LOAD SOB 2
3 = LOAD SOB 1; UNLOAD SOB 2

NOTE: Refer to STATE COUNTER TRUTH TABLE, Appendix A, Page 5.

7-12.6 TAKE DATA is ANDed with State Counter values 1 or 2 AND SOB 2* OR Ø OR 3 AND SOB 1. When either of these two AND conditions are met, 1 + 2 Load Buffer Latch or Ø + 3 Load Buffer Latch on J8 is set.

7-12.7 The Load Buffer Latches are OR'd together (J8 TP7) and are ENDed with LAST CHAR* (Last Character code) OR ANY SOB* AND 500 KHZA*. The output of

this AND sets NEW DATA ENABLEflip-flop.

7-12.8 NEW DATA ENABLE AND ANY SOB* causes 9th and 10th INH* to occur which is sent to J11. On J11, 9th and 10th INH* causes 9th REC BIT and 10th REC BIT to occur, which stops the recirculation of the LAST CHAR code on this character.

7-12.9 The character with the LAST CHARacter code, resides at the output of the MOS Buffer. With NEW DATA ENABLE set, the LAST CHARacter code is blocked so that at 500KHZB the character is loaded back into the MOS Buffer without the LAST CHARacter code.

7-12.10 At the fall of the next 500KHZ time the NEW DATA Flip-Flip is set, creating NEW DATA.

7-12.11 NEW DATA is also ANDed with ANY SOB* AND 500KHZA which places the contents of REG 1 into the MOS Buffer and loads the LAST CHAR code with the character. NEW DATA is ANDed with 500KHZA to generate STOP/LOADA*. STOP/LOADA* is sent to J10 to create REG 1 RST* which is sent to J9 to "Zero" the REG 1 flip-flop (clear the character just loaded into the buffer). STOP/LOADA* also resets both the LOAD SOB Latch and the STOP SOB1 Latch. The same 500KHZA going false resets NEW DATA.

NOTE: Refer to Appendix A, Page 6 for the timing relationship to load sequence.

7-12.12 NEW DATA is ANDed with 500KHZB which generates STOP/LOAD*. STOP LOAD* resets ANY SOB (L) and NEW DATA ENABLE on J8 and is sent to J10 to reset TAKE DATA.

7-12.13 UNLOADING of data from the buffer starts with SEND DATA flip-flop being set. SEND DATA would have been set by either CHANGE MODE* (which indicates we have just entered the unload cycle) OR by CNTR2=9 AND OFFLINEA AND CLOCKA (which indicates the character unloaded was output to the Offline device).

7-12.14 SEND DATA is ANDed withthe STATE COUNTER values 1 and SOB1* OR 3 AND SOB2*. Satisfying either AND condition will set UNLOAD SOB1 Latch OR UNLOAD SOB2 Latch . The outputs of the two latches are OR'd together and ANDed with FIRST CHAR* (FIRST CHARacter code). The first FIRST CHARacter is written after the SOB was loaded by CHANGE MODE* (exiting ballon L) AND 500KHZA. The output of this AND either UNLOAD Latch or FIRST CHAR* will set the CHANGE CHAR flip-flop.

7-12.15 CHANGE CHAR* is created,which clears the FIRST CHAR code from the present character at the output of the buffer by causing 9th REC BIT and 10th REC BIT on J11. These two signals are sent to J7 and inhibit the recirculation of bits 9 & 10.

7-12.16 At 500KHZB* time CHANGE CHAR flip-flop is reset and MOD CHAR (J8 TP6) flip-flop is set. At this time, the data at the output of the buffer is strobed into REG 2 by MOS DATA STROBE on J9. MOS DATA STROBE* is sent to J10. There it becomes SEND DATA RST* which clears the SEND DATA flip-flop and sets the SEND DATA RESET Latch on J12.

7-12.17 MOD CHAR* creates 9th REC BIT and 10th REC BIT which inserts the FIRST CHAR code on the next character in the buffer.

7-12.18 At 500KHZB time if [LOAD SOB*] OR [SOB1 OR SOB2] are false, the MOD CHAT flip-flop is reset.

7-12.19 If SOB1 or SOB 2 is true AND LOAD SOB* is false, END OF BLOCK Latch is set, END of BLOCK resets MOD CHAR flip-flop prior to the FIRST CHAR code being written.

7-12.20 END OF BLOCK indicates that all of the data stored in the unloading block has been output because the MOD CHAR cycle tried to modify an SOB code. The trailing edge of all SOB codes are ANDed with IHN STATE ADV* (which indicates that the last character unloaded is still being output to the TTY from REG 2). When INH STATE ADV* is false, it allows the ENABLE STATE ADV flip-flop to be set.

7-12.21 END OF BLOCK is also ANDed with TAPE CLK GATE* (which indicates the last character unloaded is still being written onto tape). When TAPE CLK GATE* is false, it allows the WRITE TAPE ENABLE flip-flop to be set.

7-12.22 The outputs of the two flip-flops, ENABLE STATE ADV AND WRITE TAPE ENABLE, are ANDed with END OF BLOCK AND (SOB 1 AND 1) OR (SOB 2 AND 3) to set the STOP RECirculate Latch.

7-12.23 STOP REC* resets the END OF BLOCK Latch and causes REC on J7. This clears the data just unloaded from the buffer.

7-12.24 STOP REC* is ANDed with SOB 1 AND 3 OR SOB 2 AND 1 which indicates that all data output has been cleared and the buffer has reached the loading SOB. At this points, the signal STATE ADV* is generated.

7-12.25 STATE ADV* resets the STOP REC Latch and increments the STATE COUNTER by one.

7-12.26 The STATE COUNTER can be advanced by (STATE ADV*) OR (MODEM AND COUNT 50 Option) OR (OFFLINE* AND CPU COMM) OR(Ø + 2 AND OFFLINE AND C/R*) (ASCII carriage return).

7-12.27 When the STATE COUNTER changes from Ø + 2 to 1 + 3, CHANGE MODE* is generated (refer to text 7-12.13).

7-12.28 The STATE COUNTER is cleared to zero by(SRCH*) or (POR*) + (DELSS*) or (BURST + OFFLINE).

NOTE: Refer to Appendix A, Page 6 for the timing relationship of the unload sequence.

SECTION 8

ELECTRO/MECHANICAL ADJUSTMENTS, REMOVAL, AND INSTALLATION PROCEDURES

SECTION 8

ELECTRO/MECHANICAL ADJUSTMENTS, REMOVAL AND INSTALLATION PROCEDURES

8-1 REPLACEMENT OF FUSES AND LAMPS

8-1.1 Fuse Replacement

NOTE: Three fuses are contained in the Dicom 344

A. Two 3AG 3AMP SB AC line fuses are on the back panel of the Dicom 344.

B. One 8AG 3AMP 28V DC fuse exists on the bottom of the Power Supply mother board.

8-1.2 Power Supply Removal

A. To gain access to the fuse, two captive screws on the Power Supply must be backed out. The Power Supply can then be slid out of the Dicom 344.

B. Turning the Power Supply over exposes the fuse as it is located in the middle of the Power Supply mother board.

8-1.3 Switch Lamp Replacement

A. Grasp the plastic indicator with fingers and pull outward

B. Use GE 330 lamp or equivalent for replacement.

8-1.4 Ready Lamp Replacement Procedure

A. Remove top cover

B. Assure that the loader assembly is in the UP position.

C. Using a screwdriver, press the side of the metal shroud on the side where the wires enter, then raise up that side of the housing.

D. Unscrew the defective lamp and replace with a GE 373.

8-1.5 EOT/BOT Lamp Replacement procedure for TTM SN 450 and below.

A. Remove the affected Deck from the Dicom 344 following the Deck removal instructions in Section 8-2 8-2.

B. Remove the capstan assembly from the Deck following the capstan assembly removal instructions. in Section 8-3.

C. Remove the four Phillips flat head screws that secure the loader assembly.

D. Remove cable clamp that is secured to the Deck baseplate by a Phillips head screw.

E. Turn Deck so that it is resting on its base connector.

F. Remove "C" ring from head in/out actuator and slip the spring off the Head In actuator.

G. Release the two Phillips screws securing the lamp assembly and slit the thermal tubing insulation.

H. Cut the lamp connecting wires below the second layer thermal insulation tubing.

I. Strip and tin the wires going to the lamp. Cut to length, strip and tin the wires going to the new lamp assembly (Dicom part number 344-60016).

J. Slip the thermal tubing insulation supplied over the new lamp wires.

K. Lock the two stripped and tinned wires together and solder.

L. Slide the thermal insulation over the splice joint and shrink into fit.

M. Resecure the lamp, using the two Phillips screws.

N. Slip head arm actuator spring over the Head In actuator and install "C" ring.

8-1.6 EOT/BOT Lamp Replacement procedure for TTM SN 451 and above.

A. Remove the affected Deck from the Dicom 344 following the Deck Removal instructions in Section 8-2.

B. Remove the two mounting screws for the EOT/BOT Lamp Assembly through the circular hole in the tape transport base.

C. Remove the screw securing the three plugs and unplug the EOT/BOT Lamp.

D. Remove the Capstan/Clutch Assembly following the Capstan/Clutch removal instructions in Section 8-3.

E. While the Clutch/Capstan Assembly is raised insert the wires of the new EOT/BOT lamp.

F. Secure the four Allen screws in the Clutch/Capstan Assembly.

G. Secure the screws in the EOT/BOT lamp mount removed in step 2.

H. Insert the EOT/BOT lamp plug into the socket.

I. Secure the screw removed from the three plugs in Step 3.

8-2 TRANSPORT REMOVAL/ INSTALLATION

For tape transport removal/installation, the following steps should be performed.

1. Turn off power to the Dicom 344.

2. Remove the 6 Phillips head screws in the top cover and remove cover.

3. Unplug the Elco plug in the rear housing of the Tape Transport Module to be removed.

4. Two Phillips head screws in the bottom of the motor housing (at the rear of the Tape Transport Module) must be removed.

5. Two Phillips head screws at the lower front of the Tape Transport Module should be released by ten turns.

6. Two Phillips head screws in the black plastic shroud on the outside front of the Tape Transport Module must be removed.

7. The shroud should be removed and the cassette loader mechanism pressed down.

8. Remove the Tape Transport Module by lifting the rear of the transport, and guarding the front so that the switch mechanism in the front does not catch on the front panel.

9. To install a Tape Transport Module, press the loader mechanism down.

10. Angle the transport module so that the front screw slots are touching the front panel.

11. Slide the Tape Transport Module forward and down while guiding the front loader mechanism so that it does not become crushed by the front panel.

12. Install the screws in the lower, rear motor housing leaving them slightly loose.

13. Turn on the Dicom 344 power and verify normal up/down clearance of the loader mechanism of the Tape Transport Module.

14. Turn power off.

15. Tighten the 2 rear Phillips head screws.

16. Tighten the 2 front Phillips head screws.

17. Install the black plastic shroud with the two screws removed.

8-3 CAPSTAN/CLUTCH REMOVAL/INSTALLATION

For Capstan/Clutch removal/installation the following procedure should be performed.

1. Remove deck from the Dicom 344 following the deck removal instructions.

2. Turn the deck over so that the plastic loader lid is down.

3. Release large drive belt between the motor and capstan assembly at the motor pulley.

4. Using a 7/64 Allen key, remove the four Allen screws securing the clutch assembly.

5. Unscrew the Phillips screw securing the 28 V DC power input plug to the clutch assembly.

6. Slowly raise the capstan assembly up and catch the rewind pulley drive belt with a crochet hook or a bent paper clip and slide the belt off the capstan pulley.

7. To reinstall the clutch assembly, capture the rewind pulley drive belt using a crochet hook or bent paper clip and slip the belt over the top shiv in the capstan pulley.

8. Insert and tighten the four Allen head screws.

9. Insert the connector for 28 VDC to the clutch assembly and install the Phillips head screw.

10. Verify that the Rewind Drive Belt is over the Rewind Drive pulley by rotating the flywheel by hand and observing the pulley rotate.

8-4 ANALOG TO DIGITAL ADJUSTMENT PROCEDURE

8-4.1 Material Required

A. Signal Generator*

B. Oscilloscope, Techtronix type 453 or equivalent.

C. An Online device interfaced to the Dicom 344.

D. Three scratch tapes.

8-4.2 Read/Write Electronics common mode rejection adjustment; the following should be performed.

A. Place the Dicom 344 in the OFFLINE READ mode.

B. Using a signal generator, introduce a 5KHZ sinewave to J15 TP4.

NOTE: Reduce signal source to zero volts prior to making any new connection.

C. Connect an oscilloscope to J15 TP5. Set vertical input to AC coupled with .05 v/cm sensitivity.

D. Increase the amplitude of the signal source until the 5KHZ signal appears at J15 TP5.

E. Adjust J15 R14 until the minimum signal is observed (common mode null).

F. Connect the signal source to J15 TP6, scope J15 TP7 and repeat the above procedure while adjusting J15 R43.

G. Connect the signal source to J15 TP8, scope J15 TP9 and repeat the above procedure whil adjusting J15 R72.

8-4.3 Read/Write Electronics Gain Adjustment

Write a tape and read the same tape on all three decks. As the selected deck is playing back, adjust the deck gain control for 1.2 to 1.6 volts p-p and as near equal as possible. Monitor J15 TP10 and adjust:

R87 Deck 1
R58 Deck 2
R29 Deck 3

8-4.4 Reproduce Electronic Symmetry and Bipolar Adjustment.

The following steps should be taken in the Dicom unit serial number 144 or above, or if the 90033 Reproduce Amplifier is Rev. "E" or greater.

A. With a signal generator, introduce 5 Khz sinewave to J15 TP3. Reduce the signal source to zero prior to making connection.

B. Connect an oscilloscope to J14 TP6. Set vertical input to DC coupled with .5v/cm sensitivity.

C. Adjust signal source to a level just exceeding threshold as observed on the scope.

D. Adjust J14 R12 (Symmetry control) for equal amplitude positive and negative peaks.

E. Increase signal source amplitude until signal at J14 TP6 is 1.2 V p-p.

F. Move oscilloscope probe to IC A4-A Pin 1. Re-adjust vertical sensitivity to 2 v/cm.

G. Adjust J14 R23 (Threshold adjustment) until a square wave is present, then re-adjust J14 R23 until the square wave just disappears (bipolar stops switching).

8-4.5 The following steps should be followed in Dicom 344 with serial number of 143 or less, or with Rev "C" 90033 (J14) Reproduce Amplifier.

A. With a signal generator, introduce a 5 kHz sinewave to J15 ~~TP5~~. Reduce the signal source to zero prior to making connection. TP 10

B. Connect an oscilloscope to J14 TP4. Set vertical input to DC coupled with .5 v/cm sensitivity.

C. Adjust signal source to level just exceeding threshold as observed on the scope.

D. Adjust J14 R12 (Symmetry control) for equal amplitude positive and negative peaks.

E. Increase signal source amplitude until signal at J14 TP4 is 1.2 V p-p.

F. Move oscilloscope probe to IC A3-A Pin 1. Set vertical sensitivity to 2 v/cm. GROUND J14 pin T. ← IMPORTANT !

G. Adjust J14 R23 (threshold adjustment) until a square wave is present, then re-adjust J14 R23 until the wquare wave just disappears (bipolar stops switching).

8-4.6 Reproduce Electronics Gain Adjustment

A. Using the tape generated in Step 8-4.3, place the Dicom 344 in the OFFLINE READ mode.

B. Connect the scope to J14 TP2 and adjust R2 for 14 VAC ± 2 VAC.

8-4.7 Gap T1 Adjustment

Using the On-line device, generate a series of 1 character records on a tape deck. Place the unit in OFFLINE READ, and sync (+) at J12 TP3 (Cntr. 1-8) and monitor J13 TP6. TP6 should remain positive for 325 μ seconds minimum. Adjust J13 R4 accordingly.

8-4.8 Gap T2 Verification

Using the same scope sync and tape as in Section 8-4.6, monitor J13 TP4 (Gap (T2). J13 TP4 should remain high for 1 millisecond.

8-5 READ/WRITE HEAD VERIFICATION (ADJUSTMENT)

(Not recommended to be adjusted in the field.)

8-5.1 Material Required

A. 5KHZ Standard Alignment Tape Dicom part number 00501.
B. Diphase test tape Dicom part number 00506.
C. Read/Write Electronics Module Dicom part number 344-90028
D. Oscilloscope, Techtronix type 453 or equivalent.
E. Allen wrench 5/64".

8-5.2 Skew Verification

A. Install Read/Write Electronics Module (344-90028) into J16.

B. Install Standard Alignment tape cassette into the tape transport to be verified.

C. Select: OFFLINE, the tape transport to be verified, and READ.

D. Connect oscilloscope to J15 TP10 and J16 TP10 sync on auto with sensitivity at 2V/cm and sweep speed at 20 milliseconds/cm.

NOTE: In oscilloscope sensitivity settings, a 1X probe is assumed.

E. Observe that the waveform on the scope rises from center to peak equals between .6 and .8 volts and the waveform has a definite peak. Observe waveforms shown in Figure 8-5.B.

8-5.3 Skew adjustment is performed by rotating the Allen screw in the tri-head mount that is closest to the front panel. The waveform observed at J15 and J16 TP10 should be peaked in amplitude and within 20 μseconds displacement as shown in Figure 8-1.B.

8-5.4 Head elevation verification (should be verified any time skew is adjusted). The following steps should be performed.

A. Install the Diphase Test Tape Cassette.
B. Install the Read/Write Electronics Module into open card slot J16.
C. Connect both traces to J15 TP10 and J16 TP10, set sensitivity to .05 v/cm, sync to auto, sweep speed to .2 milliseconds/cm.
D. Observe the waveforms of Figure 8-5.A and verify that both traces are less than 125 millivolts.

8-5.5 Head elevation adjustment would be performed if greater than 125 millivolts of signal is observed. The head elevation adjustment is made by rotating slightly the other two Allen screws (middle and rear screws of the tri-mount) until less than 125 millivolts of signal is observed. Refer to Figure 8-5.A.

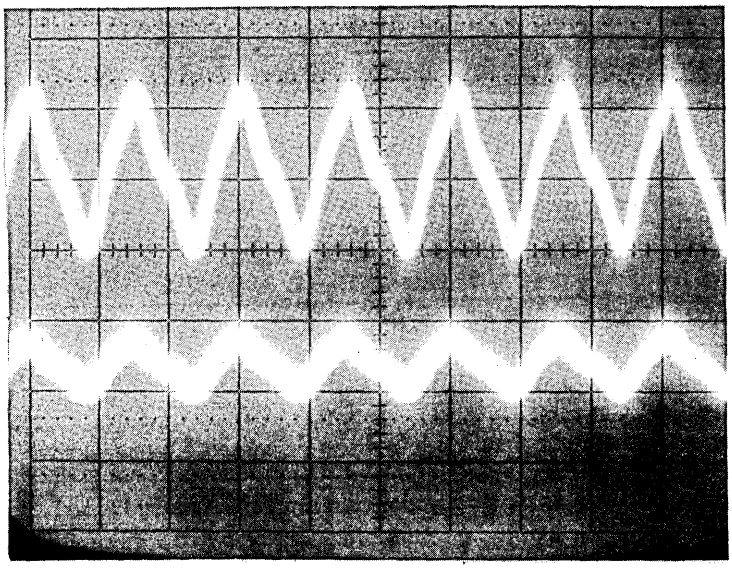
NOTE: The Head Elevation and Skew Adjustments are interactive whenever one is adjusted both must be checked.

CAUTION: Any adjustment performed on the head mount could affect adversely the transport to transport compatibility.

8-5.6 Any Allen screws loosened must be secured by epoxy to assure that they do not change their position.

CROSSTALK: MAX 125mv

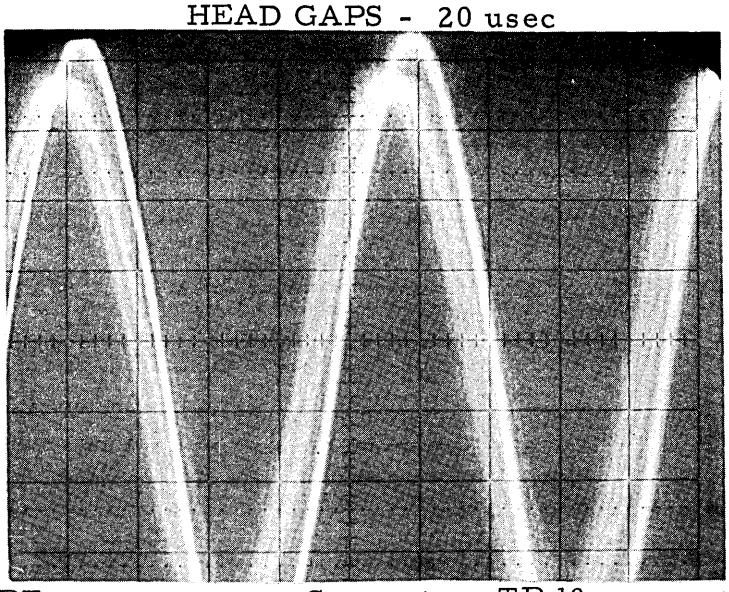
FIG. 8-5.A



SCOPE Sync: Auto TP10 J15 & J16
Vertical Sensitivity: 50 mv/cm
Time Base: .2 m sec/cm

SKEW: MAX SEPARATION BETWEEN TWO HEAD GAPS - 20 usec

FIG. 8-5B



SCOPE Sync: Auto TP 10 J15 & 16
Vertical Sensitivity: .05 mv/cm
Time Base: 20 usec/cm
10 Kc standard

8-6 TAPE TRANSPORT MODULE SWITCH

Operation, verification and adjustment of the Tape Transport Module switches are contained in this section.

8-6.1 Material Required

A. 5/64" Allen key 90° modified so that the short side is less than 1/4" long.

B. 90° Phillips screwdriver.

C. Volt/Ohm meter.

D. 4 shims .0001 inches thick or a short blade feeler gauge.

8-6.2 Test of Head Out of Place Switch adjustment (HOPS

NOTE: Two designs of the Head Out Switch are presently in the field. Refer to Figure 8-6 to determine if the Tape Transport has the GOPS Switch.

Without GOP Switch

A. Connect an Ohm meter between the two wired terminals of the heads out switch.

B. Move the Head Arm Assembly toward the tape chamber by pushing the Pinch Roller Hub until the Head Out of Place Switch opens.

C. Observe that when the switch opened, the Pinch Roller is 1/16 to 1/8 inch away from the Capstan.

D. If the switch energized too soon, release the mounting screws and rotate the switch counter-clockwise as far as possible.

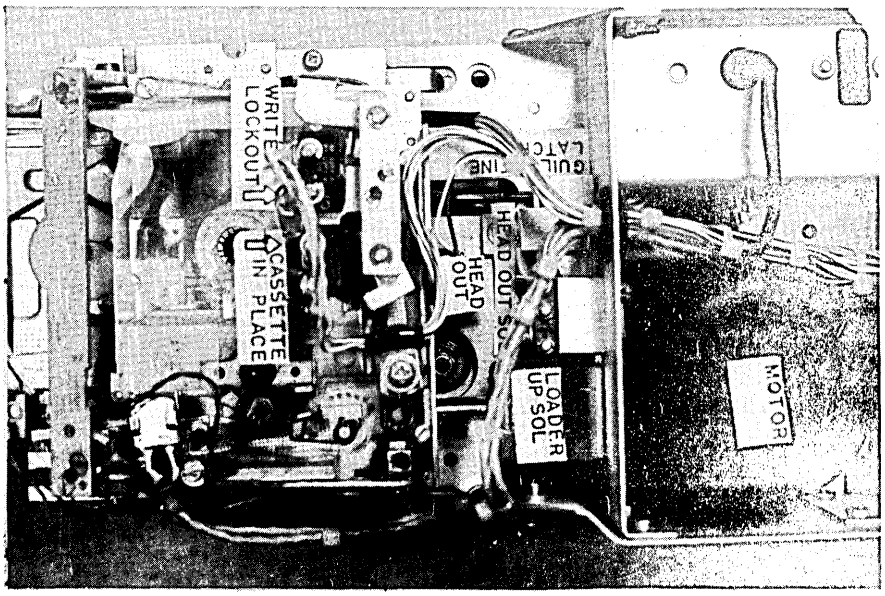
E. If the switch energized too late, release the mounting screws and rotate the switch clockwise slightly.

F. Retest the Heads Out of Place Switch as per Step 8-6.2.B and 8-6.2.C.

With GOP Switch

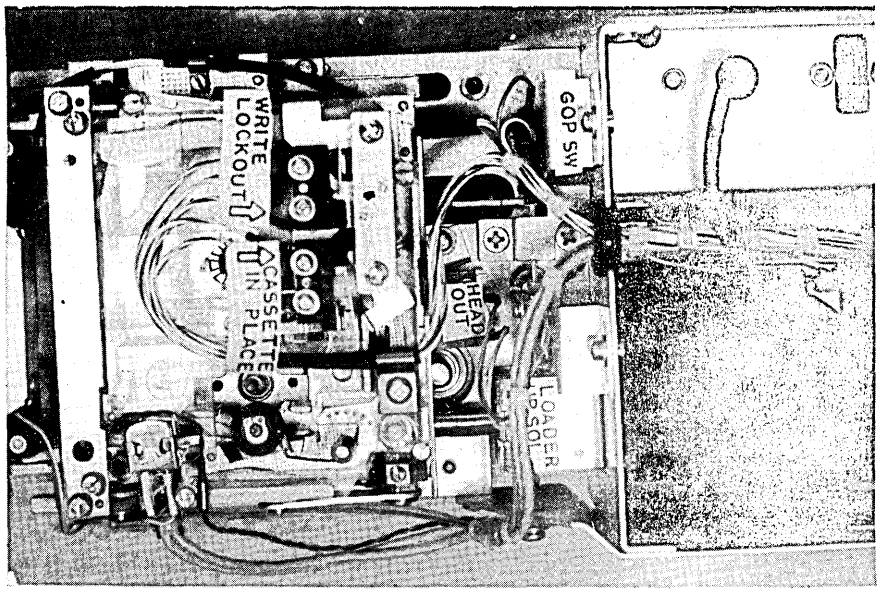
A. Apply power to the Dicom 344.

B. Lower the loader machanism and close the Cassette In Place switch (refer to Figure 8-6). Observe that the Read/Write head pulls into place.



Without the Guillotine Out-of-Place Switch

A



With the Guillotine Out-of-Place Switch.

B

FIG. 8-6

C. Insert a 20 thousandths feeler gauge or shims between the Head Out of Place Switch leaf and the Switch wiper. Observe that the Read/Write head retracts.

D. If the Read/Write head did not retract in Step C, release the round head Phillips screw securing the Head Out of Place Switch mounting bracket and position the switch until the head does retract.

E. Tighten the round head Phillips screw released in Step D and repeat Step C.

8-6.3 Heads in Place Switch Adjustment (HIPS)

NOTE: Two designs of the Head in Place Switch are presently in the field. Refer to Figure 8-6 to determine if the Tape Transport has the GOP Switch.

Without GOP Switch

A. Apply power to the Dicom 344.

B. Lower the Loader Mechanism. Observe that the Read/Write head is retracted.

C. Insert a 20 thousandths feeler gauge or shim between the Guillotine Latch Lever and the end of the Head in Place Switch actuator leaf. Observe that the Head is pulled into place.

D. Press down lightly on the end Head Switch leaf with a soldering aid or small screwdriver. Observe that the head retracts. If the head does not retract, the Head in Place Switch is set too low.

E. Insert a 40 thousandths feeler gauge or shim between the Guillotine Latch Lever and the Head in Place Switch actuator leaf.

F. Press lightly down on the Head in Place actuator leaf as in Step D and observe that the head does not retract. If the head does retract, the switch is set too high.

G. To adjust the position of the Head in Place Switch, release the 5/64" Allen head screw on the motor side of the motor barrier, with the modified Allen wrench.

H. Release the two Phillips head screws mounting the Head in Place Switch to the mounting block. Position the switch so that Step C and D can be accomplished.

I. Tighten the two Phillips head mounting screws and the 5/64" Allen screw.

With GOP Switch

A. Apply power to the Dicom 344.

B. Lower Loader mechanism.

C. Insert a 10 thousandths shim between the end of the Head in Place Switch and the Head out solenoid.

D. Press lightly on the Head in Place Switch actuator leaf with a soldering aid or small screwdriver. Observe that the Head Out solenoid oscillates.

E. If the Head Out solenoid does not oscillate, release the single Phillips head screw on the top of the Head In place mounting bracket and position the switch counter-clockwise until the Head In solenoid does oscillate.

F. Tighten the Phillips head screw released in Step E.

8-6.4 Guillotine Out of Place Switch GOPS

NOTE: Tape Transport of serial numbers 601 and above have the Guillotine Out of Place Switch.

A. Turn the power off on the Dicom 344.

B. Press the Head Out solenoid down until the GOP Switch makes (clicks).

C. The Head Out solenoid plunger should be pressed fully down when the GOP Switch makes.

D. If the GOP Switch made too early, or did not make at all, release the round head Phillips screw securing the the GOP Switch mounting bracket and adjust the position of the switch, while pressing down on the Head In solenoid plunger, until the switch justs makes (clicks).

E. Tighten the round head Phillips screw securing the GOP Switch mounting bracket.

8-6.5 Write/Lock/Cassette In Place Switches Verification

A. Material required

1. Phillips Screwdriver #2
2. Volt Ohm meter

B. The following steps should be performed:

1. Insert a cassette into the tape transport to be verified.

2. Measure between C and NC contacts of the Cassette in Place Switch on top center of the plastic loader cover.

3. An open should be observed.

4. To adjust for an open, release the cassette and bend the actuator arm behind and inside of the loader. A slot exists in back of the loader for this purpose.

5. Re-insert the cassette and measure again for the open.

6. To verify the Write Lock Switch, which is to the left of the Cassette In Place Switch, install a cassette with the the write protect tab in it into the loader.

7. Press lightly on the leaf actuator and measure continuity between C and NO of the Switch. A short should exist.

8. If a short does not exist, the tab end of the linkage should be bent slightly forward.

9. Verify the cassette can be ejected by pressing the eject switch. If the cassette cannot be ejected, too much bend was placed on the actuator tab.

8-7 CAPSTAN/ CLUTCH PERFORMANCE MEASUREMENT

The purpose of this measurement is to determine whether the performance of a Capstan/Clutch assembly could affect the compatability of a tape written by the tape transport module.

8-7.1 Material Required

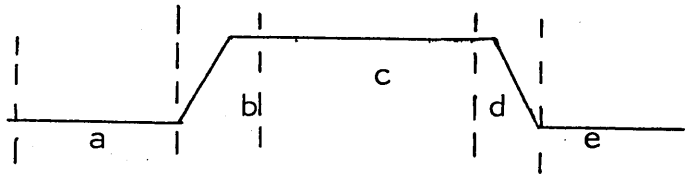
A. 300 ft. cassette tape recorded with data without record gaps.

B. Oscilloscope

C. Torque Wrench Cleco Pnuematic CAL 30A with Allen key APEX-3 185

D. Dicom Template, Cluch adjusting

E. Computer program or Dicom Test Fixture to Start (Read for 30 msec) and Stop (Halt for 15 msec).



	Min.	Max.
a =	4 msec.	7 msec.
b =	3	8
d =	5	7
e =	Ø msec.	3 msec.

FIGURE 8-7

NOTE: If any of the times measured are outside of the Min/Max of Figure 8-7, the times must be inserted into the following equation: 25-a-b/2+d+e/2= X. X should not be greater than 28 or less than 19. If X is greater or less, the Clutch Gap either requires adjustment or the clutch should be replaced.

8-7.2 Verification Procedure

A. Insert the cassette test tape of 8-7.1.A in the tape transport to be evaluated.

B. Connect the oscilloscope sync input to J1, J2 or J3 TP13 and sync positive.

C. Connect the oscilloscope signal input to J15 TP9 (Deck #1), J15 TP7 (Deck #2)or J15 TP5 (Deck #3), and set amplitude for .2 volts/cm.

D. Start either the program or test fixture in the

Start/Stop mode, and measure with the oscilloscope the Capstan/Clutch acceleration profile (refer to Figure 8-7).

8-8 CLUTCH GAP ADJUSTMENT PROCEDURE

1. The Dicom 344 should be turned over so that the bottom cover is facing up. The bottom cover should be removed.

2. Back off the three Allen screws on the clutch assembly (refer to Figure 8-15).

3. Back off the three 10-32 slot head screws.

4. Adjust the 10-32 slot head screws clockwise until they encouter slight resistance, making an effort to keep the resistance equal on each screw.

5. Using the torque Allen wrench, set at 10 inch ounces rotate each Allen screw until snug.

6. Turn the torque Allen wrench until it releases.

7. Using the Dicom Template laid over the Allen screws and slot screws, turn the slot screws counter-clockwise 15° (one mark on the template).

8. Again, turn the Allen screws until snug.

9. Turn the torque Allen wrench until it releases.

10. Repeat the verification of the Start/Stop times (Section 8-7.2).

8-9 TACHOMETER WIPER CONTACTS ADJUSTMENT

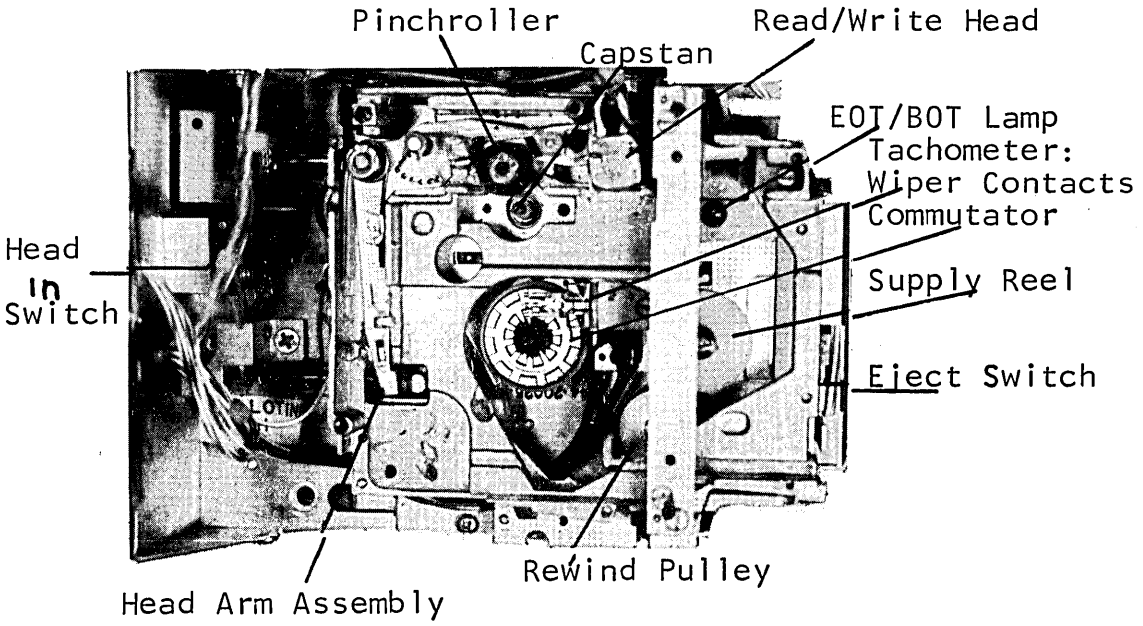
This section will cover Tachometer wiper contacts adjustment, removal and installation (refer to Figure 8-9).

NOTE: A test of the tracking of the Tachometer Wiper Contacts should be performed prior to any adjustment of the Tachometer Wiper Contacts.

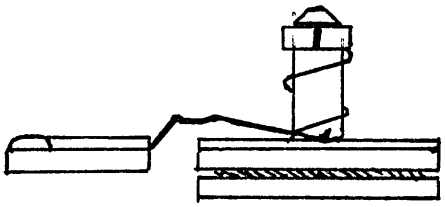
8-9.1 Test for proper tracking of wiper contacts.

A. Connect an oscilloscope to TP6 of the Deck Control Logic Module for the Tape Transport under test (refer to Figure 6-1).

B. Sync automatic on the signal and adjust vertical amplifier for 1 volt DC.

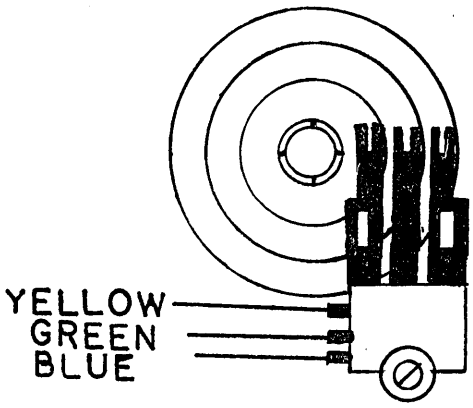


A.



Tachometer
Side View

B.



Tachometer
Top View

C.

FIGURE 8-9

C. Rotate the Take-up Reel slowly using a cotton swab and observe the positive to negative transitions cannot be sustained at ground.

D. If ground can be sustained, note the position of the wiper contacts on the Tachometer Commutator. The normal position is for either the inside contact or the outside contact to be connected to the center contact. At the point where ground can be sustained, both are contacting the center strip of the commutator.

E. If mistracking of Tachometer Wiper Contacts is not indicated in Step D above, refer to Section 6-15, Tachometer Operation Verification.

8-9.2 Centering the Tachometer Wiper Contacts

A. Release clear plastic cover on the cassette loader by removing the four slot head screws (refer to Figure 8-9A).

B. Loosen the slot head screw securing the Tachometer Wiper Contacts and center the wipers on the commutator (refer to Figure 8-9C).

C. Observe that the inner wiper and outer wiper are not contacting the same center commutator segment, by performing the test specified in 8-9.1.C.

8-9.3 Forming the Tachometer Wiper Contacts (refer to Figure 8-9C)

A. Remove the Tape Transport Module from the Dicom 344 as per instructions in Section 8-2.

B. Raise the loader on the Tape Transport by pushing the Loader Up Solenoid Plunger into the solenoid.

C. Access to the inner and outer Tachometer Wiper Contacts can now be gained between the Loader Mechanism and the Main Plate.

D. Using tweezers or hemostats, the Tachometer Wiper Contact that extends out further than the others can be formed so that its point of contact on the Tachometer Commutator is the same as the other two wiper contacts. (Refer to Figure 8-9B.)

E. Reinstall the Tape Transport Module as per instructions in Section 8-2.

F. Retest the Tachometer Wiper Contacts as per instructions in 8-9.1.C.

8-9.4 Removal/Installation of Tachometer Wiper Contacts.

A. Remove the four slot head screws securing the clear plastic lid and raise the clear plastic lid (refer to Figure 8-9.A).

B. Unsolder the wires connected to the Tachometer Wiper Assembly.

C. Remove the slot head screw securing the Tachometer Wiper Assembly and remove the Tachometer Wipers from the Tape Transport.

D. Install the new Tachometer Wiper Contact Assembly carefully so that the individual wipers are not bent and install the holding slot head screw.

NOTE: If this screw was not secured with a lock washer, a drop of Locktite should be placed on the threads.

E. Solder the wires on the Tachometer Wiper Assembly as per Figure 8-9C.

F. Center the Tachometer Wipers as per instructions in 8-9.2.

G. Test the Tachometer Wiper Contacts as per instructions in 8-9.1.

H. Form the Tachometer Wiper Contacts as per instruction in 8-9.3.

I. Verify that the Tachometer operation is normal by performing the verification specified in Section 6- 15.

8-10 AUTOMATIC REWIND SWITCH VERIFICATION

1. To verify proper operation, insert and lower cassette, not at BOT or EOT leader.

2. If the automatic rewind does not occur, the Loader-In-Place switch must be adjusted. This switch is easiest found by removing the clear plastic loader cover and by holding the Eject switch on. The loader should raise and lower. The switch is located to the left below the supply hub (hub closest to the front panel) and will be making and breaking as the loader is raised and lowered.

3. To adjust the switch, bend the left most contact slightyly left.

NOTE: Take care not to bend too far, or Loader will not raise.

4. Reinstall cover and insert the cassette and observe that the auto rewind function occurs.

8-11 EJECT SWITCH VERIFICATION AND ADJUSTMENT

1. Eject switch veritification and adjustment is performed after every removal of a tape transport module or whenever a cassette cannot be ejected by raising the eject bar of the loader shroud or when the cassette cannot be kept in place.

2. Remove the loader shroud by removing the two Phillips head screws in the front of the shroud. The eject switch is at the bottom, inside the metal front edge.

3. If the Loader Mechanism could not be raised, press the eject switch contacts together. If the loader rises, the eject switch contacts are too high; bend them down slightly so that the Shroud Eject Bar can close the switch.

4. If the cassette would not stay in place, separate the contacts and verify that the Loader will now stay down.

8-12 BUFFER SPRING ASSEMBLY VERIFICATION

The combination of the Buffer Spring and pressure pad, allow isolation of the tape path from perturbations taking place at the supply reel. If for some reason the buffer spring should become deformed or worn, the problem would be noted in a large amount of dynamic speed variation.

NOTE: To create a worst case condition, a delay should occur between written records; i.e., copying from one tape to another.

1. Connect an oscilloscope to J13 TP5, Sync (-), set Time Base for 20 μsec/cm.

2. While reading a tape written on this Tape Transport, the observed positive edge @181 μsec. nominal, should not display variations in time greater than ± 18 μsec.

3. If variations are greater than specified, or if the chrome plating on the spring is worn through, the Buffer Spring Assembly must be replaced. Also verify pinch roller as per step 8-23.1.

8-13 REPLACEMENT OF BUFFER SPRING ASSEMBLY

1. Remove the two black slot metric screws securing the Ready Light Assembly to the Tape Transport.

2. The Buffer Spring and Friction Pad are secured to a Buffer Spring Mounting Block on the Head Arm Assembly by a single .080 screw.

3. Remove this screw and the Buffer Spring Assembly.

4. When reinstalling the screw, a drop of Locktite should be placed on the threads of the .080 screw.

5. Carefully install the new Buffer Spring Assembly on the Buffer Spring Mounting Block with tweezers or hemostats with the .080 screw inserted.

6. Reinstall the READY Light Assembly using the two black slot head metric screws removed in Step 8-13.1.

8-14 SOLENOID PERFORMANCE CRITERIA

The function of the following tests to be performed will determine whether the solenoids and associated solenoid drivers are functioning properly. The Heads-In/Heads-Out Switches also have a bearing on the function of the solenoids and a noted malfunction may be related to these switches or due to lack of preventive maintenance lubrication.

8-14.1 Rewind Solenoid Verification

A. Raise the loader mechanism of the Tape Transport.

B. Depress the Cassette in Place switch (center of the loader, refer to Figure 8-6).

C. Place the Tape Transport in OFFLINE Rewind and hold.

D. Observe that the Supply Reel rotates.

E. Release Rewind and observe that at least 10 thousandths of an inch separate the driver idler from the Supply Reel.

F. If this clearance is not present or if the Supply Reel rotates when not in Rewind, adjust the position of the Rewind Drive Idler by bending the Rewind Drive Idler actuator post.

G. Remove the "E" Ring of the Rewind Solenoid Plunger.

H. Depress plunger manually and verify that the physical bottom of the Solenoid is deeper than the groove for the "C" Ring. Also verify that the plunger moves freely in the solenoid.

1. If the plunger failed either test, replace the Rewind Solenoid and Plunger.

8-14.2 Replacement of Rewind Solenoid

NOTE: Three styles of Rewind Solenoid designs are in the field (refer to Figure 8-14). A failure in the Rewind Solenoid of the configuration of Figure 8-14A will require that the Tape Transport be returned to Dicom for the installation of the longer Rewind Return Spring. All failed Rewind Solenoids will be converted to Figure 8-14C at the time of replacement.

8-14.2.A Removal of Rewind Solenoid shown in Figure 8-14B.

1. The Rewind Solenoid and Plunger (matched) ordered from Dicom will contain the Winchester Plug and Socket for ease of mounting.

2. Remove the two round head 8 X 32 Phillips screws securing the mounting plate for the 1000 μf capacitor and the 40Ω Dale Resistor.

3. If the wires from the resistor/capacitor network go to a Winchester Plug, remove 256 X 5/8 flat head Phillips screw securing the plug.

4. If the wires from the resistor/capacitor do not go to a plug, unsolder them from the resistor terminals.

5. Cut the two wires going to the Rewind Solenoid at the splice.

6. Release the Rewind Solenoid Spring from the Rewind Solenoid Plunger.

7. Unscrew the large nut securing the Rewind Solenoid to the Rewind Solenoid Mounting Bracket.

8. Remove the "E" Ring from the Rewind Solenoid Plunger.

9. Slide the Rewind Solenoid and Plunger out of the bracket.

10. If the input wiring of the Rewind Solenoid and resistor/capacitor were <u>not</u> on a Winchester Socket, this should be accomplished by cutting the grey/green wire and the white/blue wire to the length of the clutch field Winchester socket and soldering the two wires to the Winchester socket supplied with the replacement solenoid.

11. To mount the Rewind Solenoid Winchester socket (input), mount the Rewind Solenoid Winchester socket on top and secure both with the same flat head Phillips screw.

12. To mount the Rewind Solenoid Winchester Plug, remove the 256 X 5/8 flat head Phillips screw from the Clutch Field plug and mount the Rewind Plug on top of the clutch field plug and secure both with the same flat head Phillips screw.

8-14.2.B Removal of Rewind Solenoid shown in Figure 8-14.C.

1. Remove the 256 X 5/8 flat head Phillips screw securing the Rewind Solenoid Plug.

2. Unscrew the large nut securing Rewind Solenoid to the mounting bracket.

3. Release the Rewind Spring from the Rewind Solenoid Plunger.

4. Remove the "E" Ring from the Rewind Solenoid Plunger.

5. Slide Rewind Solenoid and Plunger out of the mounting bracket.

6. Plug the new Rewind Solenoid Plug into the socket and secure the plug with the 256 X 5/8 flat head Phillips screw.

8-14.3 Installing Rewind Solenoid.

A. Slide the new Rewind Solenoid Plunger part way into the mounting bracket then slide on the large mounting nut.

B. Slide the Rewind Solenoid the remainder of the way into the mounting bracket and secure with the large mounting nut.

C. Install the "E" Ring on the Rewind Solenoid Plunger.

D. Hook the Rewind Spring to the plunger.

E. Verify that the Rewind Spring is slightly slack. Adjust the position of the mounting bracket by releasing the two round head Phillips mounting screws and positioning the bracket until the spring is nearly under tension but is still slack.

8-14.4 Head In Solenoid Verification

NOTE: Two types of solenoids are presently in the field. The GOP Switch shown in Figure 8-6 identifies the intermittent duty solenoid.

A. Apply power to the Dicom 344 and place the loader mechanism down.

B. Alternately press and release the Cassette in Place switch (center of loader) and observe that the Head In Actuator Arm over travels the Guillotine Latch momentarily then falls back onto the Latch.

C. If the solenoid does not over travel, release the mounting screws of the solenoid and press backward (away from the plunger) and resecure the mounting screws.

D. Retest the solenoid. If a failure to over travel is still apparent, release the Head Load Spring on the Head Arm Actuator by removing the "E" Ring on the underside of the Tape Transport Module.

E. Move the plunger in and out of the solenoid and observe that it is free of drag. If drag is noted, reposition the solenoid by releasing the mounting screws and moving the solenoid to a drag free position.

F. If all attempts to gain overtravel of the solenoid fail, replace solenoid.

8-14.5 Replacement of the Head In Solenoid

NOTE: When ordering this solenoid from Dicom, please state whether the GOP switch is present on the Tape Transport.

A. Remove the motor housing screws (four Phillips head screws, two on each side and at the rear of the Tape Transport Module).

B. Raise the motor housing by rotating the Printed Circuit Connector upward.

C. Unsolder the two wires at the solenoid.

D. Remove the two Phillips head mounting screws at the bottom of the Tape Transport Module securing the Head In Solenoid.

E. Remove Solenoid and install the new solenoid.

F. Secure mounting screws pressing solenoid forward.

G. Solder on the connecting pair of wires.

H. Rotate the motor housing downward and secure the four Phillips head screws.

I. Verify the operation of the Head In Solenoid by performing the instructions in 8-14.5.

8-14.6 Loader Up Solenoid Verification

NOTE: Two types of solenoids are presently in the field; the GOP Switch shown in Figure 8-6 identifies the intermittent duty solenoid.

A. Holding the Loader Mechanism down, alternately press and release the Eject Switch.

B. Observe that the Loader Latch mechanism (slightly right and under the Supply Reel) moves sufficiently to uncover the stationary loader block.

C. If clearance is not present, release the two screws securing the solenoid (underside of the Tape Transport Module) and reposition the solenoid towards the rear of the Tape Transport.

D. Verify that drag does not exist between the solenoid and plunger by pushing the plunger rearward into the solenoid.

E. If drag exists reposition the solenoid by releasing the mounting screws and rotating the solenoid right or left holding the solenoid position.

F. If the solenoid still does not allow proper clearance of the stationary block, replace the solenoid.

8-14.7 Replacement of the Loader Up Solenoid.

NOTE: When ordering this solenoid from Dicom please state whether the GOP switch is present on the Tape Transport.

A. Remove motor housing as in Step 8-14.6.A and 8-14.6.B.

B. Remove the four screws securing the motor and remove the Drive belt.

C. Move the motor out of the way.

D. Cut the spliced wires going to the solenoid.

E. Remove solenoid mounting screws and remove the solenoid.

F. Install the new solenoid using the mounting screws removed in Step 8-14.6.E.

G. Resolder the wires connecting to the solenoid.

H. Reinstall the motor and secure the four mounting screws

I. Reinstall the Drive Pulley on the motor shaft and secure the Allen screw.

J. Install the Drive Belt on the pulley making sure that there is no obvious belt misalignment between the Motor Drive Pulley and the Jackshaft.

K. Reinstall the motor housing as per Step 8-14.6

L. Verify the operation of the Loader Up Solenoid by performing the instructions in 8-14.6.

8-14.8 Heads Out Solenoid Verification

NOTE: Two types of solenoids are presently in the field; the GOP switch shown in Figure 8-6 indentifies the intermittent duty solenoid. The solenoid is just below the Heads In Switch and actuates the Guillotine Latch (refer to Figure 8-6).

A. To test the solenoid with power on, place the Loader Mechanism down.

Activate and deactivate the Cassette In Place Switch (refer to Figure 8-6.). Observe that solenoid raises up the Guillotine Latch over the Head Actuator Arm and that it bottoms into the slot cut in the Head Actuator Arm.

B. Power Off Test

1. Press down on the spring loaded plunger and verify that no drag exists either in the Guillotine Latch or in the solenoid Plunger.

2. If drag is noted, slightly reposition the Guillotine latch and verify that the latch has some play with the plunger in any position but fully up. The Guillotine is repositioned by releasing the two Phillips head mounting screws and rotating the entire assembly right or left. If the Guillotine latch appears badly worn or a great deal of side to side play in the latch is noted, it should be replaced (refer to 8-14.9 for replacement instructions).

3. If the drag is still noted in the plunger travel, release the Phillips head screws securing the solenoid (underside of tape transport) and position the solenoid for minimum drag.

C. If solenoid cannot meet the criteria set in Step 8-14.8.A, replace the solenoid.

8-14.9 Replacement of Head Out Solenoid

NOTE: When ordering this solenoid from Dicom, Please state whether the GOP Switch is present on the Tape Transport.

A. Turn the Tape Transport so that the Loader Mechanism is down.

B. The solenoid is behind the Capstan/Clutch and under the Drive Belt (refer to Figure 8-14).

C. Cut the two wires going to the solenoid at the splice.

D. Remove the two round head Phillips screws mounting the solenoid to the right angle mounting bracket.

E. Turn the Tape Transport on its side, so that the Capstan/Clutch is down and remove the solenoid body without dislocating the plunger from the Guillotine Latch.

F. Slide the new solenoid over the plunger leaving .0002inches gap between the top of the solenoid and the mainplate. Install the two round head Phillips mounting screws into the right angle mounting bracket.

G. Solder the wires from the solenoid to the wires cut free in Step C.

H. Verify that the solenoid is properly positioned by performing the steps in 8-14.8.

8-15 GUILLOTINE LATCH ASSEMBLY REPLACEMENT

NOTE: The Guillotine Latch is actuated by the Head Out Solenoid to release the spring loaded Head Actuator Arm which causes the Head to retract (refer to Figure 8-6).

1. Remove the two flat head Phillips screws which secure the Guillotine Latch to the Main Plate.

2. Press the Head Out Solenoid Plunger spring down to release the Guillotine lever connection to the plunger and remove the latch.

3. Prior to installing the new Guillotine Latch assembly place Lubriplate onto the latch lever and work up and down. Wipe off excess Lubriplate.

4. To install the new Guillotine Latch Assembly into the Tape Transport, press down on the Head Out Solenoid Plunger spring.

5. Insert the Guillotine lever into the Head Out Solenoid Plunger.

6. Install the two flat head mounting screws through the Guillotine Latch Assembly into the Main Plate.

NOTE: If the transport has the GOP switch, the switch must be removed prior to removal of the Guillotine Latch.

8-16 PINCH ROLLER VERIFICATION

1. If the pinch roller should have hard or soft spots in it caused by improper cleaning chemicals or if it becomes pitted or worn, dynamic and long term speed variations will become apparent.

2. The test for dynamic speed variations is contained in Section 8-12.

8-17 PINCH ROLLER REPLACEMENT

1. Requires a Waldes Truarc Grip Ring Pliers M52.

2. Insert the double nose of the pliers into the grip ring securing the pinch roller.

3. Carefully remove the pinch roller as there is a clear plastic washer at the top and botton of the roller.

4. Install new roller with the clear washers at the top and bottom.

5. Using the grip ring pliers, install the grip ring so that no vertical end play of the pinch roller is noted.

6. Using the grip ring pliers, move the grip ring side to side until 2 to 5 ten-thousandths of an inch of end play is noted.

7. Verify that the roller turns freely.

8. Test the dynamic speed stability again as in Step 8-12.1 and 8-12.2.

8-18 MOTOR VERIFICATION

1. The motor generally indicates potential for failure by running very hot at the top of the case (in excess of 70°C) or by excessive noise eminating from the motor-bearings.

2. The motor is the primary cause of blown AC line fuses.

3. To isolate motor blowing fuses, unplug all motors (the motor AC plug is the ELCO to the left and rear of the motor).

4. Plug each motor in one at a time, slowly, to find which motor is the cause of the problem.

5. Replace the motor blowing fuses.

8-19 MOTOR REPLACEMENT

1. Remove the four Phillips screws securing the rear motor housing. These screws are located two on each side and toward the back of the Tape Transport Module.

2. Release the Motor Drive Belt from the Motor Drive Pulley.

3. Rotate the printed circuit connector back and upwards to expose the motor, motor capacitor, AC connector and wiring.

4. Unsolder the motor wiring from the AC connector and standoff.

5. Remove the Drive Pulley and Drive Belt on the underside of the Tape Transport Module.

6. Remove the four Phillips head screws securing the motor.

7. Remove the motor.

8. Install the new motor and secure the four Phillips head mounting screws.

9. Install the Drive Pulley and Drive Belt making sure no mechanical misalignment exists between the Drive Pulley and Jackshaft.

10. Wire the motor:

    Blue wire to standoff
    Red wire to capacitor side of AC connector
    Black and White wire to the other side of the VAC connector

11. Verify the motor operation by plugging in the AC power.

8-20 DRIVE BELT REPLACEMENT

8-20.1 Rewind Idler Drive Belt Replacement

A. Remove Capstan/Clutch Assembly as per instruction in Section 8-3.

B. Remove the four flat head Phillips screws that secure the loader to the Main Plate.

C. Separate the Loader body from the Main Plate.

D. Place new Rewind Idler Drive Belt on the Rewind Idler by slipping the belt over the Actuator attachment and around the Idler Drive Pulley.

E. Reinstall the loader body and secure with the four flat head screws.

NOTE: The Rewind Drive Idler should be connected to the the actuator linkage before the loader body is secured.

F. Reinstall Capstan/Clutch as per instruction in Section 8-3.

8-20.2 Rewind Drive Belt Replacement

A. Remove the Capstan/Clutch Assembly as per instruction in Section 8-3.

B. Replace the Rewind Drive Belt at the top of the Capstan between the Forward/Rewind Pulley and Jackshaft.

C. Reinstall Capstan/Clutch Assembly as per instruction in Section 8-3.

8-20.3 Jackshaft Drive Belt Replacement: (Not recommended to be performed in the field).

A. Remove the Capstan/Clutch Assembly as per instructions in Section 8-3.

B. Remove Rewind Drive Belt.

C. Remove "C" clip from the Forward/Rewind Pulley and remove pulley.

D. Remove the four Phillips screws securing Top Bearing Mount Plate.

E. Raise plate and replace Jackshaft Drive Belt.

F. Replace Top Bearing Mount Plate; install the four Phillips head screws.

G. Reinstall Forward/Rewind Pulley and install "C" clip.

H. Reinstall Rewind Drive Belt.

I. Reinstall Capstan/Clutch Assembly as per instructions in Section 8-3.

8-20.4 Motor Drive Belt (not recommended in the field)

A. Remove the four Phillips head screws securing the bottom bearing mounting plate.

B. Slide bearing mounting plate off the Jackshaft and Capstan shaft carefully with the Bottom Bearing Mounting Plate up, so that none of the preload washers are lost.

C. Replace Motor Drive Belt.

D. Reinstall Bottom Bearing Mount Plate with the preload washers exactly as they were when the plate was removed.

E. Secure Bottom Bearing Mounting Plate with the four Phillips screws.

F. Test the clutch Start/Stop performance as specified in Section 8-7.

8-21 REWIND DRIVE IDLER REPLACEMENT

1. Remove Capstan/Clutch Assembly as per instructions in Section 8-3.

2. Remove the four Phillips flat head screws on the underside of the main plate. By removing these screws the Loading Mechanism is released from the Main Plate. Remove the "E" Ring securing the Head Arm Actuator Return spring and lift the return spring off the post.

3. Pry the clear pastic snap washer from the Rewind Idler mounting post using a small screwdriver under both washers.

4. The Rewind Idler can now be lifted from the post and replaced making sure that the Rewind Drive Belt is around the Rewind Drive Idler Pulley.

5. Place the red plastic washer over the Rewind Idler post.

6. Press the clear plastic retainer down on the spindle until it seats in the groove cut into the post.

7. Replace the Loader Mechanism on the Main Plate making sure that the Head Out of Place switch leaf is not being bent; the Rewind Drive Idler is fit into the Rewind Actuator linkage.

8. Install the four flat head Phillips screws to secure the Loader Mechanism.

9. Reinstall the Capstan/Clutch Assembly as per instructions in Section 8-3.

8-22 FORWARD DRIVE IDLER REPLACEMENT

1. Remove Capstan/Clutch Assembly as per instructions in Section 8-3.

2. Remove the "E" Ring holding the Head Arm Actuator Return spring from the Head Arm post.

3. Release the Loader Mechanism as per instuctions in Section 8-21.2.

4. Remove the Forward Drive Idler Load Spring from the Forward Drive Idler.

5. Remove the "C" ring from the Head Arm Pivot Block

6. Remove Head Arm Pivot Block, remove and replace the Forward Drive Idler.

7. Reinstall the Head Arm Pivot Block and secure with "C" ring.

8. Reinstall Loader Mechanism as per instructions in Section 8-21.7.

9. Reinstall Head Arm Actuator Return spring and secure with "E" ring.

10. Reinstall Capstan/Clutch Assembly as per instructions in Section 8-3.

8-23 FORWARD TAPE-UP REEL ASSEMBLY REPLACEMENT

1. Remove Loader Mechanism clear plastic cover by removing the four metric slot screws.

2. Pry off the black plastic cap on the top of the Forward Take-Up Spindle using two screwdrivers.

3. Remove the screw securing the Tachometer wiper contacts and remove the Tachometer Wiper Contacts from the Forward Take-Up Commutator.

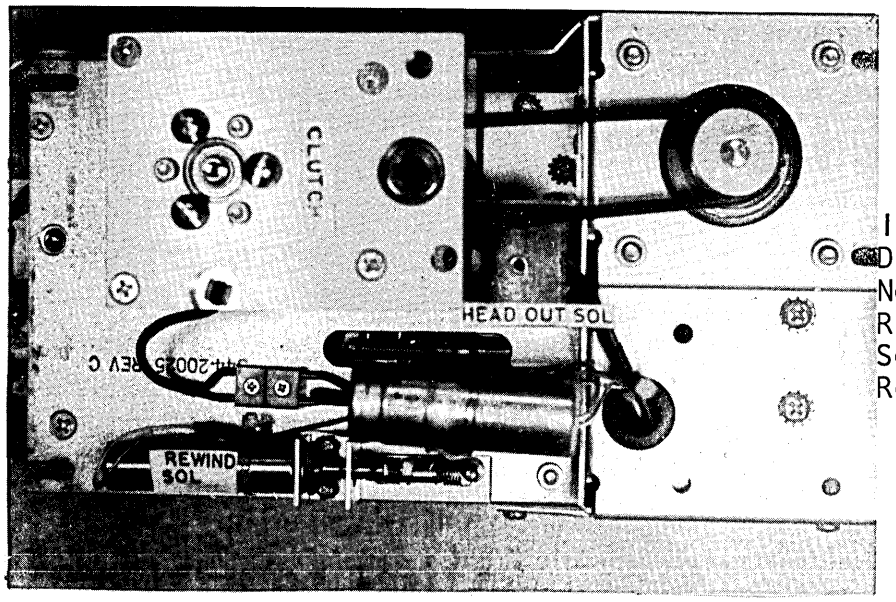
4. Slide the Forward Take-Up Assembly up the Forward Take-Up Spindle and replace with a new Forward Take-Up Assembly.

5. Install a <u>new</u> black plastic cap on the Forward Take-Up Spindle (do not use the old one, as it will not hold).

6. Reinstall the Tachometer Wiper Contacts and secure with the mounting screw.

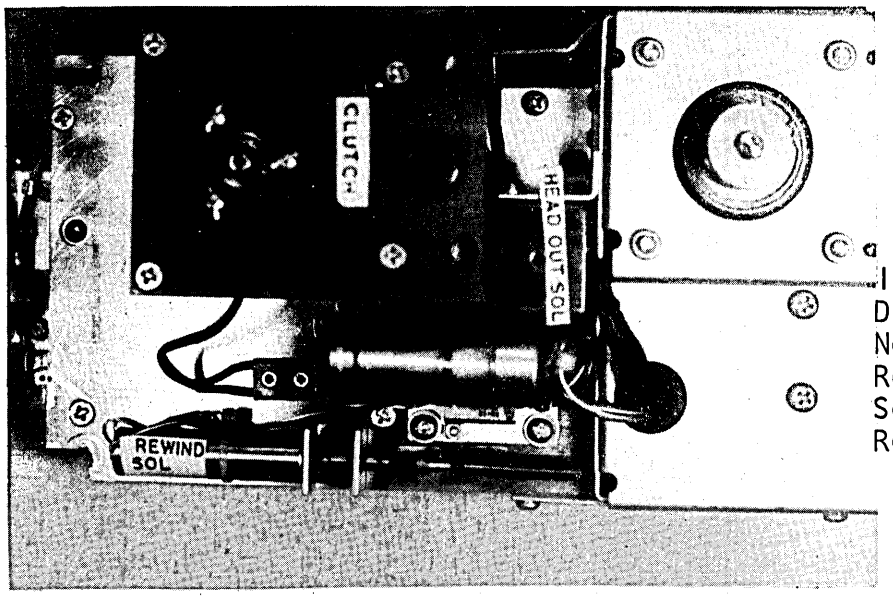
7. Test Tachometer Wiper Contact placement using the instructions in Section 8-9.

FIG. 8-14



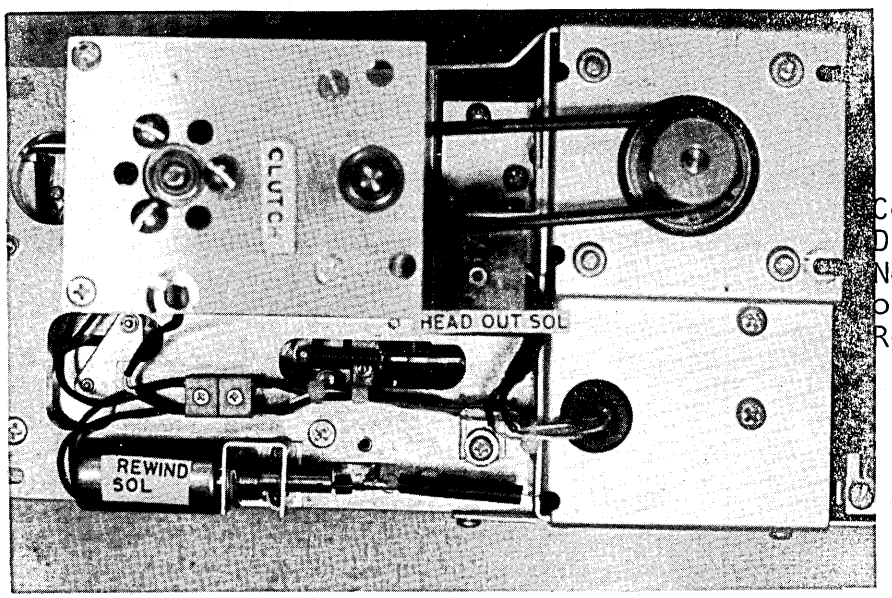
Intermittent Duty Solenoid Note: Short Rewind Solenoid Return Spring

A



Intermittent Duty Solenoid Note: Long Rewind Solenoid Return Spring

B



Continuous Duty Solenoid Note: Removal of Capacitor/ Resitor

C

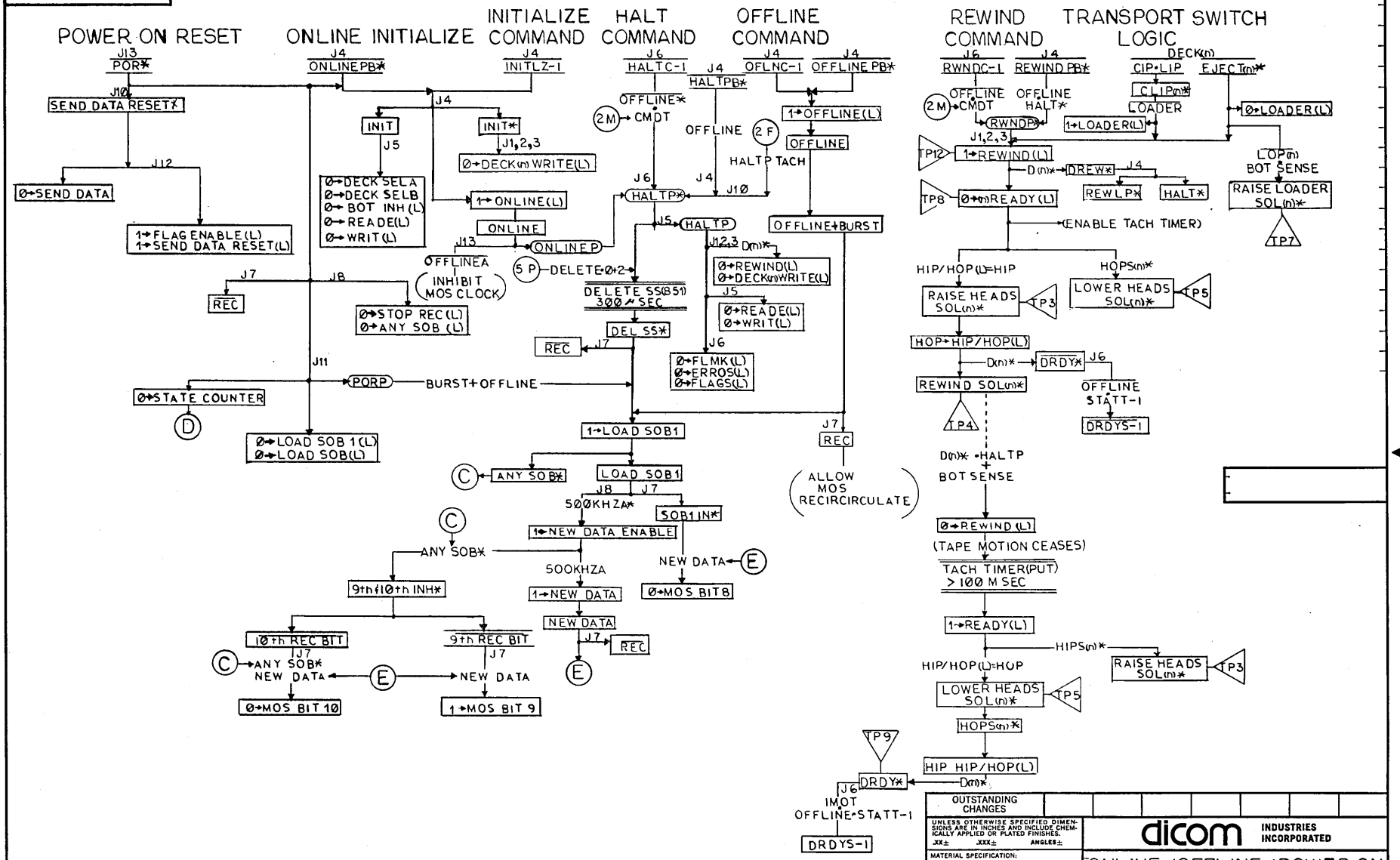
APPENDIX A LOGIC FLOW DIAGRAMS

DEFINITIONS OF FLOW DIAGRAM SYMBOLS

NAME	INDICATES A LEVEL ASSERTED, OR ACTION, IN THE LOGIC SEQUENCE.
(NAME)	INDICATES A PULSE THAT IS GENERATED BY OR OCCURS IN THE LOGIC SEQUENCE.
NAME*	INDICATES THE VOLTAGE OF THE LEVEL OR PULSE IS GROUND WHEN ASSERTED.
NAME	INDICATES THE VOLTAGE OF THE LEVEL OR PULSE IS POSITIVE WHEN ASSERTED.
NAME	A BRAKE IN THE FLOW INDICATES AN "AND" CONDITION. ALSO INDICATED BY A •
$\overline{\text{NAME}}$*	INDICATES THAT THE FLOW WILL CONTINUE IF POSITIVE.
$\overline{\text{NAME}}$	INDICATES THAT THE FLOW WILL CONTINUE IF NEGATIVE.
Ø OR 1→NAME (L)	INDICATES THAT THE LOGIC STATE IS STORED IN A LATCH.
Ø OR 1→NAME	INDICATES THAT THE LOGIC STATE IS STORED IN A FLIP FLOP.
NAME	INDICATES A KNOWN, FIXED DELAY.
NAME	INDICATES AN UNKNOWN DELAY.
NAME	INDICATES AN "OR" CONDITION. ALSO INDICATED BY A +
2A	INDICATES FLOW SEQUENCE ORIGINATES ON PAGE 2 BALLOON A.
( )	PARENTHESIS ARE USED TO DELINEATE AN ACTION.

APPENDIX A

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE



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XX± XXX± ANGLES±

MATERIAL SPECIFICATION:

FINISH SPECIFICATION:

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dicom INDUSTRIES INCORPORATED

ONLINE/OFFLINE/POWER ON TAPE TRANSPORT FLOW DIAGRAMS

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	C	APPENDIX A	

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SHEET PAGE 1

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ISSUE	DESCRIPTION	RESPONSIBILITY			
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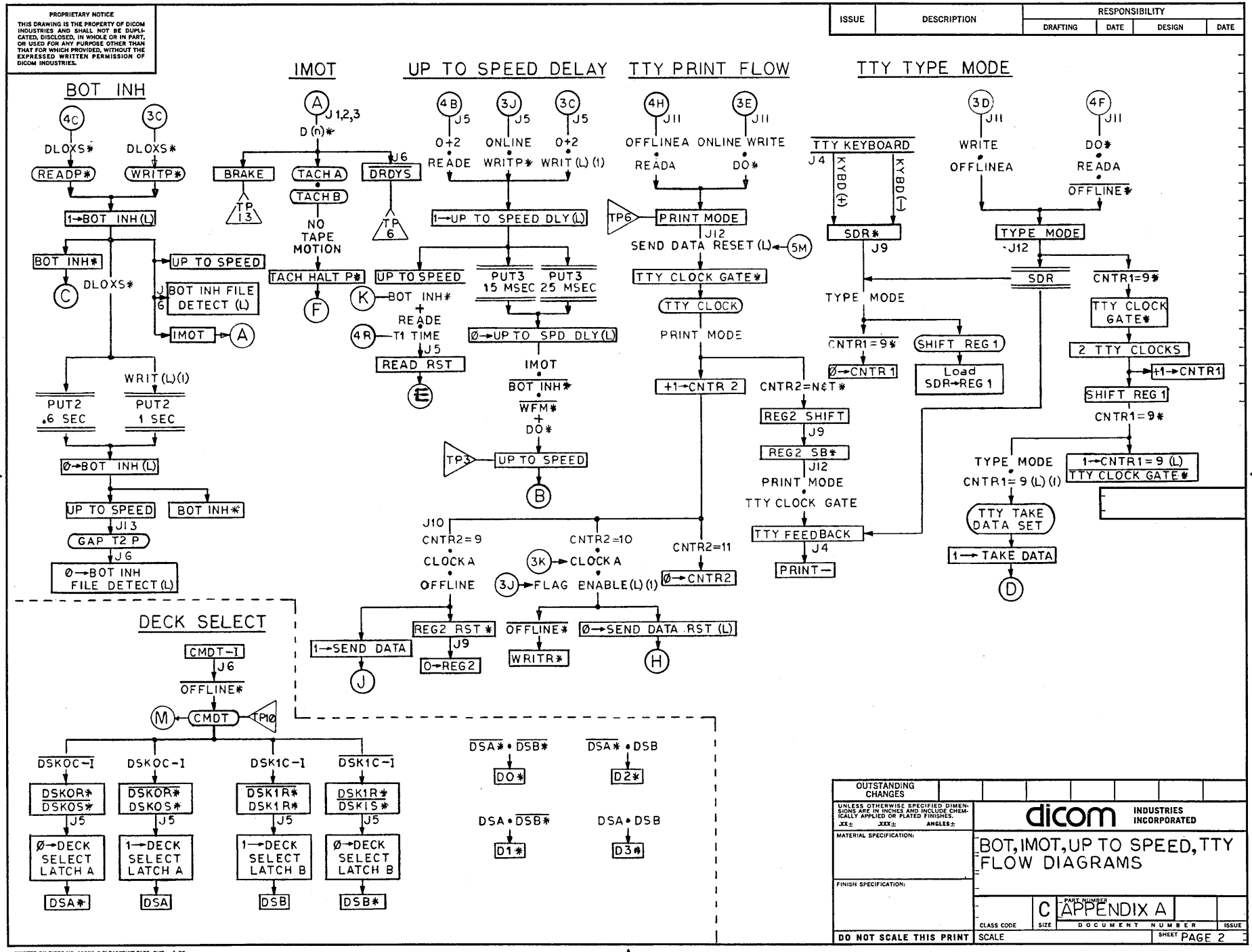

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MATERIAL SPECIFICATION:	BOT, IMOT, UP TO SPEED, TTY FLOW DIAGRAMS							
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ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE

ONLINE/OFFLINE WRITE

WRITE PB*
J4 HALT*
OFFLINE

WRITC-1
J6
CMDT

CMDT-1
J6
IMOT
OFFLINE*
CMDT
TP6

WRITP*
J5
DWLOS*
TP6
1→WRIT (L)

WRIT

WRITE

I
DO*
J6
Inhibit FLMK detect

J4
OFFLINE
Inhibit Panel Switches

2A IMOT
2B UP TO SPEED DELAY
DLOXS*
C
BOT INH

J11
WRITE*

WRITE A
OFFLINEA
TYPE MODE
D

J12
TTY CLOCK GATE
INH STATE ADV*
H

J10
ONLINE
BURST+OFFLINE*
K
CLOCK A

ONLINE
CNTR=9
TTY CLOCK + TAPE CLOCK

CNTR2 RST*
REG2 RESET*
J9
Ø→REG2
J12
Ø→CNTR 2
1→SEND DATA
2J
TP8
1→SEND DATA RESET(L)
1→FLAG ENABLE(L)
J
TP5

SEND DATA SET*
J12
Ø→FLAG ENABLE(L)

OFFLINE A*
ONLINE WRITE
J11

SET RDY FLAG
1→FLAGS(L)
OFFLINE*
STATT-I
FLAGS-I

CMDT
1→WRITE STROBE ENABLE
NDATT-I → FLAGR*
J10
WRITE STROBE ENAB(I)

INPUT STROBE
LOAD REG 1

1→TAKE DATA
SEND DATA (1)
BURST+OFFLINE
DATA TRANSFER STROBE

SEND DATA RST*
Ø→SEND DATA
REG1→REG2
0 TAKE DATA F/F

ONLINE WRITE
SET READY FLAG
F
REG1 RST
J9
Ø→REG1

DO*
PRINT MODE
E

DO*→WRITE TAPE MODE
J12
TAPE CLOCK B
J13
2B→UP TO SPEED
WRIT CMD
J SEND DATA RESET
TAPE CLOCK GATE
J13
TP7
TAPE CLOCK
TAPE CLOCK A
TAPE CLOCK B
CNTR2=8
CNTR2=N+T*
CNTR2=8*
CNTR2=N+T*
COMPLIMENT WRITE I/O
LOAD ODATØ + REG2 BIT1* →WRITE I/O

+1→CNTR1
CNTR2=N+T
REG2 SHIFT
NEXT ODATØ
CNTR2=9+10*
TAPE CLOCK B ODATØ-1
WRITE 1
TAPE CLOCK A
WRITE Ø

CNTR2=10
CNTR2=11
0→CNTR 2

FLAG ENABLE(L)(O)
Ø SEND DATA RESET
TAPE CLOCK GATE
WRITE Ø
OFFLINE*
CLOCK A
WRITR
J5
G
FLAGR*
J6
0→FLAGS(L)
0→WRIT (L)
IMOT

FILE GAP WRITE FLOW

FLMKC-1
CMDT
WRITE PB*
HALT*
OFFINE PB*
WFMP*
WRITP+WFMP
J 1,2,3
D(n)*
1→WRITE FILE MRK (L)

I
DO*
WRITE
TP9
1→DECK(n)WRITE(L)
D(n)*
WRITS*
OFFLINE*
STATT-I
WRITS-I
D(n)W
J15
WRITE 1
WRITE Ø
HEAD I = 1
HEAD I = Ø
TP 12
TP 11

WFM DLY 75 ms
WFM*
IMOT
UP TO SPEED
Ø→WRITE FILE MARK(L)
WFM*
IMOT
UP TO SPEED
2B
WFM*
IMOT
2A

OUTSTANDING CHANGES										

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
XX± XXX± ANGLES±

MATERIAL SPECIFICATION:

FINISH SPECIFICATION:

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ONLINE/OFFLINE WRITE AND WRITE FILE GAP FLOW DIAGRAM

CLASS CODE	SIZE	PART NUMBER / DOCUMENT NUMBER	ISSUE
	C	APPENDIX A	

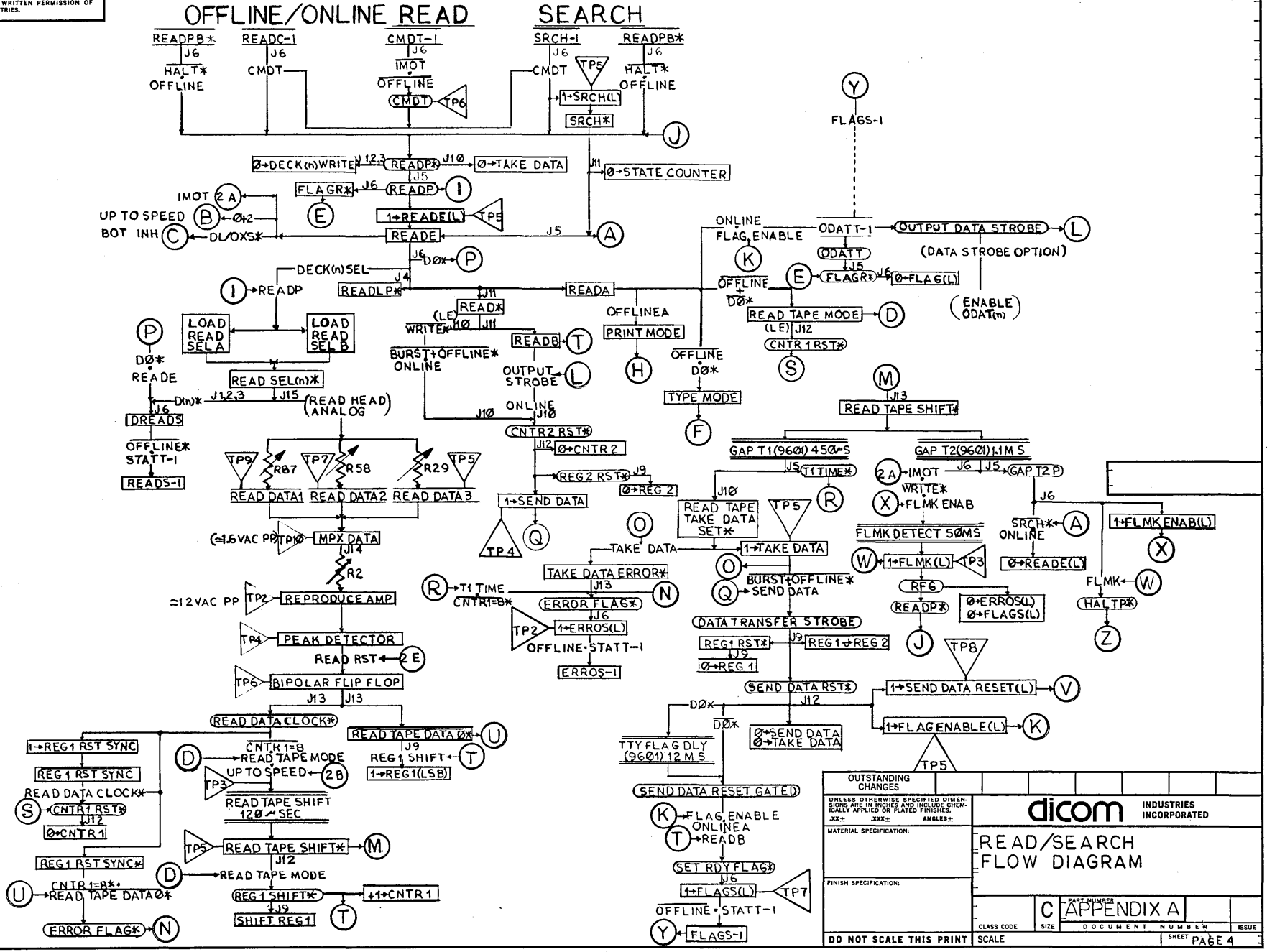
SCALE

SHEET PAGE 3

PRINTED ON DIEPO NO. 1000H-8 CLEARPRINT FADE-OUT 1-70

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE

OFFLINE/ONLINE READ SEARCH



OUTSTANDING CHANGES					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. XX± .XXX± ANGLES±	dicom INDUSTRIES INCORPORATED				
MATERIAL SPECIFICATION:	READ/SEARCH FLOW DIAGRAM				
FINISH SPECIFICATION:					
DO NOT SCALE THIS PRINT	CLASS CODE C	SIZE	PART NUMBER APPENDIX A	DOCUMENT NUMBER	ISSUE
	SCALE		SHEET PAGE 4		

PRINTED ON DIEPO NO. 1000H-8 CLEARPRINT FADE-OUT 1-70

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE

UNLOAD DATA

LOAD DATA

2D J10 TAKE DATA J8 — 1+2 SOB 2* → 1→1+2 LOAD BUFFER (L)
4O J10 TAKE DATA J8 — Ø+3 SOB 1* → 1→Ø+3 LOAD BUFFER (L)

TP7
LAST CHAR* + ANY SOB* + 500KHZA* (J) (D)
1→NEW DATA ENABLE
9th & 10th INH* → J11 9th REC BIT 10 REC BIT
500KHZA → 1→NEW DATA
500KHZB → STOP LOAD* → 0→ANY SOB(L) 0→NEW DATA ENABLE → 0→TAKE DATA
500KHZA → STOP LOADA* → J11 0→LOAD SOB(L) 0→LOAD SOB1(L)
J10 REG1RST* J9 0→REG 1

NEW DATA J7 → REC J7
ANY SOB* 500KHZA → REG1→MOS 1→MOS BIT 9 1→MOS BIT 10
SOB1IN* (I) 500KHZA → 0→MOS BIT 8 → 1→MOS BIT 9 1→MOS BIT 10
SOB2IN* (K) → 1→MOS BIT 8

LOAD SOB

1D POR* 1A DEL SS* 1H BURST+OFFLINE J11 → 1→LOAD SOB 1 (L)
→ SOB1IN* → ANY SOB* (J)
(I) SOB1IN*

(H) J11 CHANGE MODE* J10 OFFLINE → 1→LOAD SOB
(G) 3 (E) 1 → SOB2IN* (K)
LOAD SOB
SOB1+SOB2 500KHZB → 1→MOD CHAR (L)

2J CNTR2=9 OFFLINEA CLOCKA → 1→SEND DATA TP4
SOB 1* (A) (E)*1 → 1→UNLOAD SOB 1(L)
SOB 2* (B) (H)*3 → 1→UNLOAD SOB2(L)
(C) → FIRST CHAR* 500KHZA → 1→CHANGE CHAR
CHANGE CHAR* 500KHZB* → J11 9th REC B 10 REC BIT → J7 0→MOS BIT 9 1→MOS BIT 10
TP6 MOD CHAR* J11 9th REC BIT 10th REC BIT → J7 0→MOS BIT 9 1→MOS BIT 10
1→MOD CHAR → 0→CHANGE CHAR
MOS DATA STROBE* MOS DATA STROBE
J10 SEND DATA RST* J9 MOS→REG 2
J12 0→SEND DATA
1→SEND DATA RESET(L) (M)
500KHZB• LOAD SOB*↑ SOB1+SOB2 → 0→MOD CHAR

SOB1+SOB2 (TE) ------ SOB1+SOB2 LOAD SOB*
INH STATE ADV* TAPE CLK GATE* → 1→ENABLE STATE ADV (S) → 1→WRITE TAPE ENAB (T)
1→END OF BLOCK(L) END OF BLOCK
ENAB STATE ADV* (S) WRITE TAPE ENAB (T) SOB 1•1 — SOB 2•3
1→STOP REC(L) → 0→END OF BLOCK(L)
SOB1•3 — SOB2•1
0→STOP REC(L) → STATE ADV* (U)

STATE COUNTER

(B) J11 STATE ADV* — OPT MODEM COUNT 50 — OPT OFFLINE* CPU COMM — (U) Ø+2• OFFLINE OR* (Q)
J11 → TP 3 → +1→STATE COUNTER
(Ø+2 Δ 1+3) → CHANGE MODE (H)
(STATE COUNTER EQUALS)
(C) Ø+2 (D) Ø+3 (E) 1 (F) 1+2 (G) 3
4A SRCH* 1D POR* 1F DEL SS* 1E BURST+OFFLINE
→ 0→STATE COUNTER

BUFFER DATA DECODE

NOTE: SIGNALS ARE TRUE FROM THE FALL OF 500KHZA

MOS BIT	8	9	10	SIGNAL	
	Ø	1	Ø	SOB1*	(A)
	1	1	Ø	SOB 2*	(B)
	X	Ø	1	FIRST CHAR*	(N)
	X	1	1	LAST CHAR*	(P)
OCTAL		015		C/R*	(Q)
OCTAL		377		DELETE*	(R)

STATE COUNTER TRUTH TABLE

FF0	FF2	STATE
Ø	Ø	Ø
1	Ø	1
Ø	1	2
1	1	3

OUTSTANDING CHANGES

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MATERIAL SPECIFICATION:

FINISH SPECIFICATION:

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dicom INDUSTRIES INCORPORATED

MOS BUFFER FLOW DIAGRAM

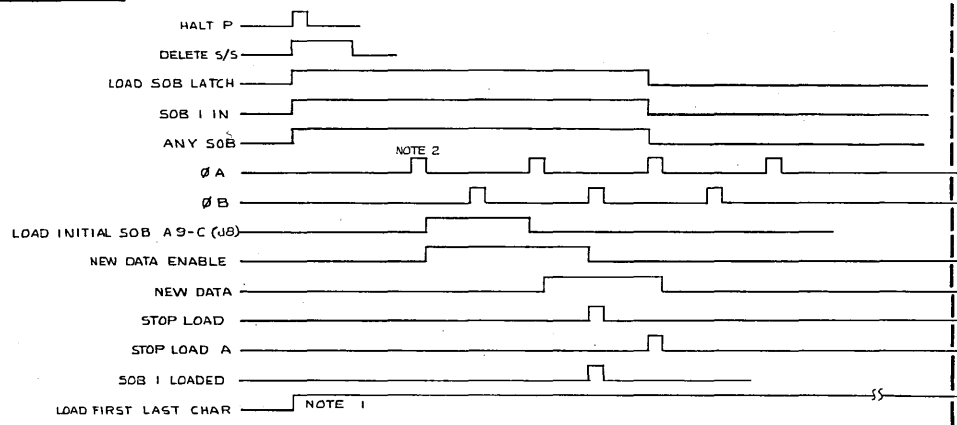
CLASS CODE C | SIZE | PART NUMBER APPENDIX A | DOCUMENT NUMBER | ISSUE

SCALE | SHEET PAGE 5

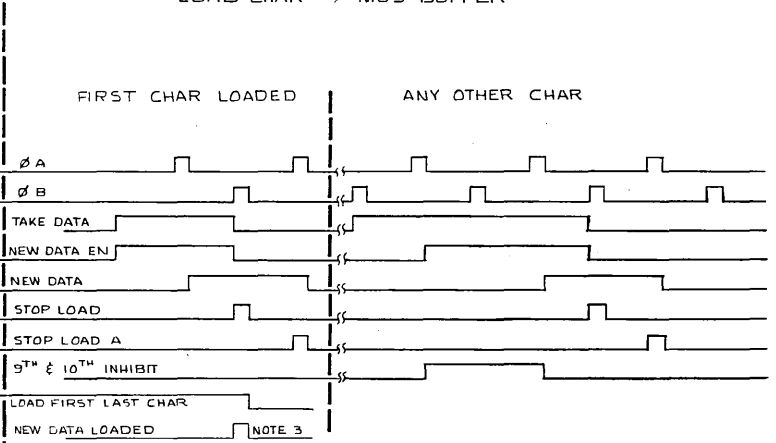
PRINTED ON DIEPO NO. 1000H-8 CLEARPRINT FADE-OUT 1-70

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE

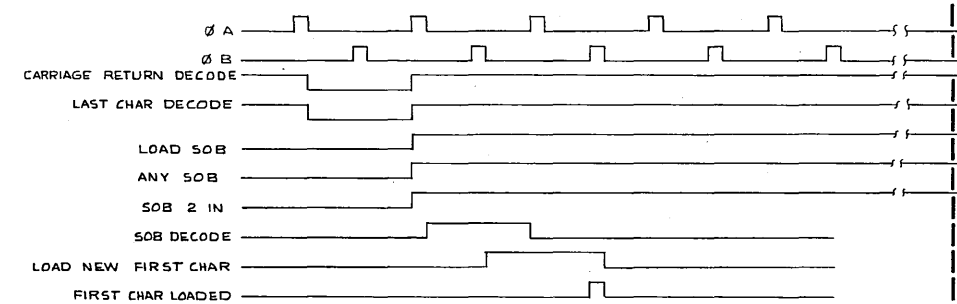
LOAD INITIAL SOB



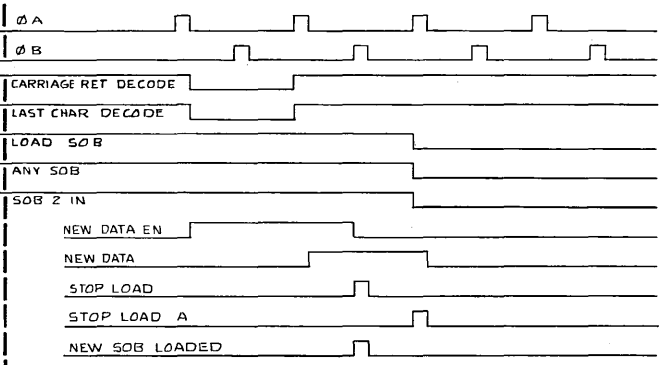
LOAD CHAR ⇒ MOS BUFFER



CHANGE STATES LOAD ⇒ UNLOAD (LOAD FIRST CHAR)



CHANGE STATES LOAD ⇒ UNLOAD (LOAD NEXT SOB)



NOTES:
1. LOAD FIRST LAST CHAR LATCH REMAINS SET UNTIL THE FIRST DATA CHAR IS LOADED. WHEN THE FIRST CHAR IS LOADED NEW DATA AND IMCB RESETS THE LATCH.
2. THIS IS THE FIRST ØA THAT OCCURS AFTER THE DELETE ONE-SHOT TIMES OUT.
3. THE LAST CHAR DECODE IS AUTOMATICALLY LOADED WHEN NEW DATA IS LOADED INTO THE MOS.
4. THE STATE COUNTER IS ADVANCED ON THE TRAILING EDGE OF CARRIAGE RETURN. THIS IS NECESSARY TO ALLOW TIME FOR THE FIRST CHAR DECODE TO BE LOADED BEFORE THE SOB IS LOADED.

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
.XX± .XXX± ANGLES±

MATERIAL SPECIFICATION:

FINISH SPECIFICATION:

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BUFFER LOAD/UNLOAD TIMING DIAGRAM

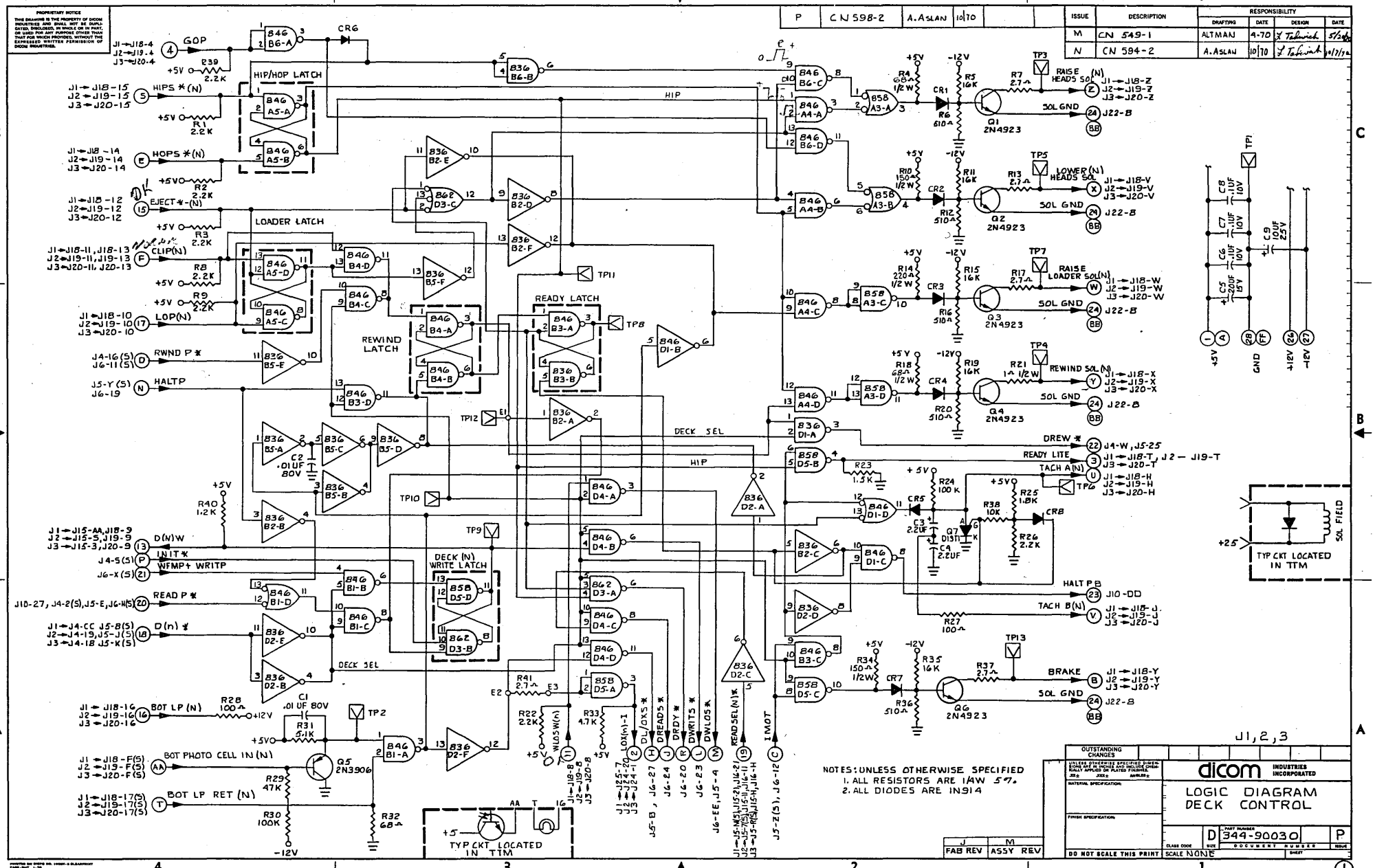
PART NUMBER APPENDIX A

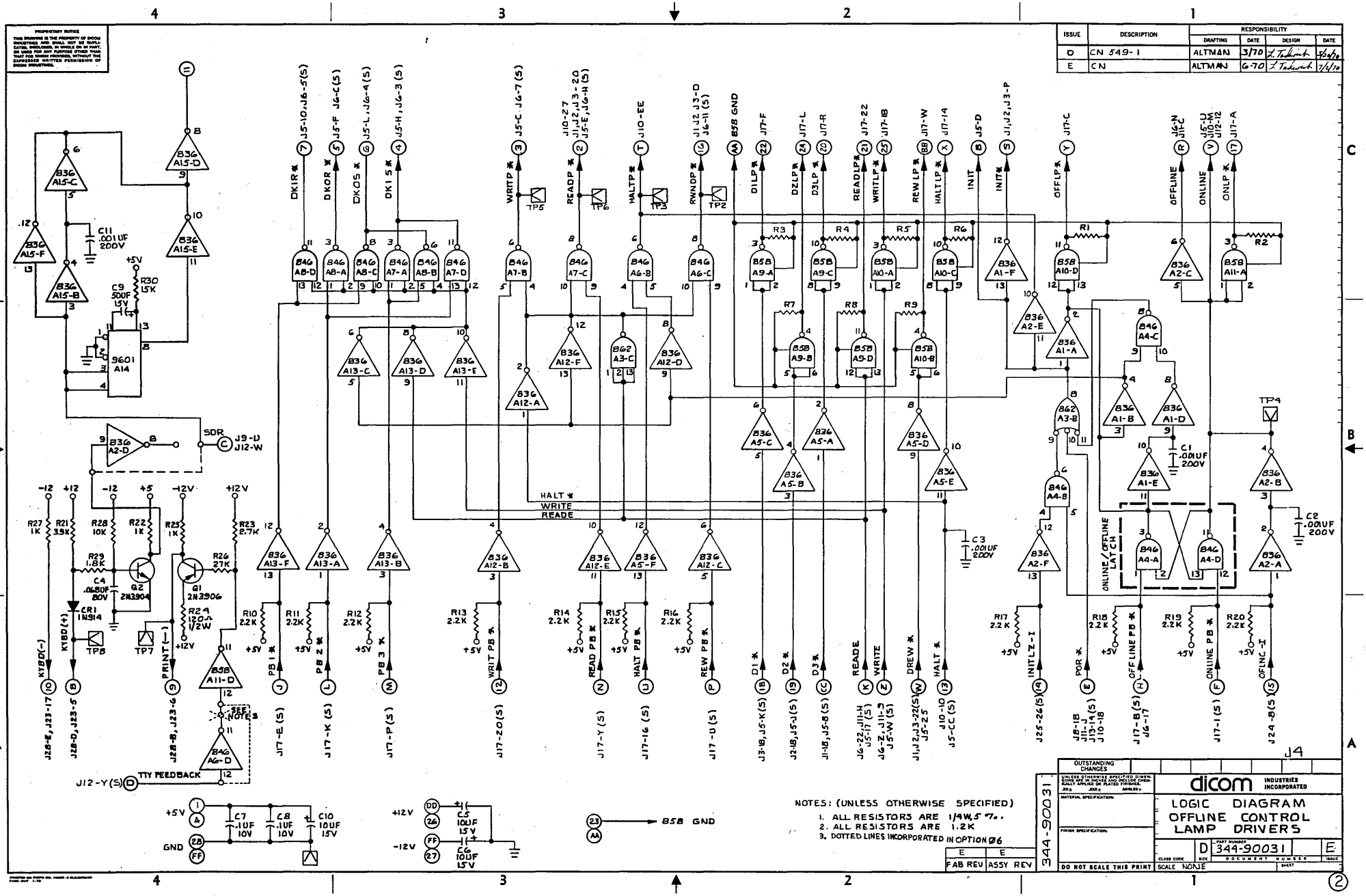
CLASS CODE | SIZE D | DOCUMENT NUMBER | ISSUE

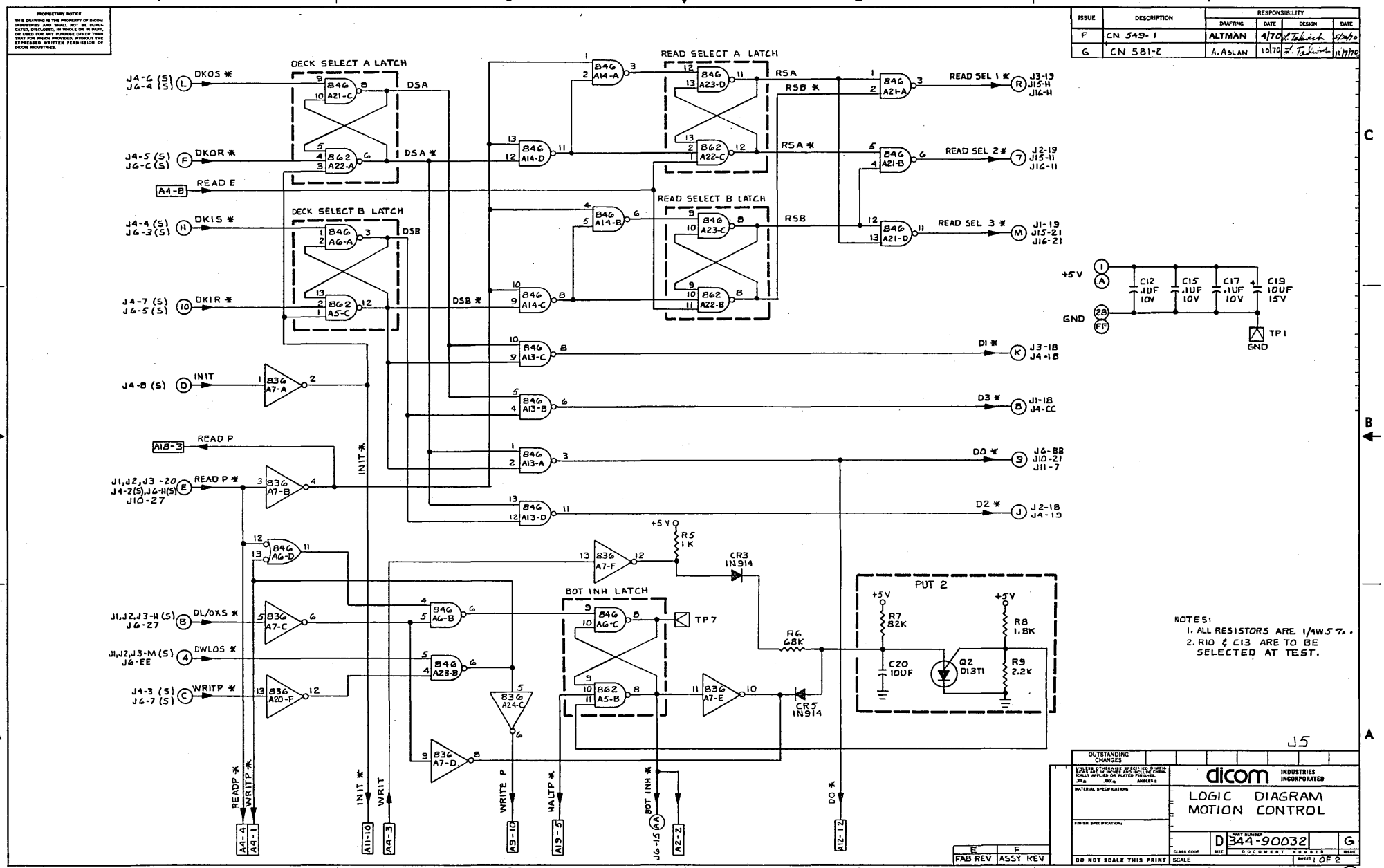
SCALE | SHEET PAGE 6

APPENDIX B

LOGIC DIAGRAMS


HIP/HOP LATCH
LOADER LATCH
REWIND LATCH
READY LATCH
DECK (N) WRITE LATCH
HIP
DECK SEL
GOP
HIPS *(N)
HOPS *(N)
EJECT *-(N)
CLIP(N)
LOP(N)
RWND P *
HALTP
D(N)W
INIT *
WFMP+ WRITP
READ P *
D(n) *
BOT LP (N)
BOT PHOTO CELL IN (N)
BOT LP RET (N)
CR6
RAISE HEADS SOL (N)
LOWER(N) HEADS SOL
RAISE LOADER SOL(N)
REWIND SOL (N)
SOL GND
DREW *
READY LITE
TACH A(N)
TACH B(N)
HALT P B
BRAKE
SOL FIELD
TYP CKT LOCATED IN TTM
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W 5%.
2. ALL DIODES ARE IN914
LOGIC DIAGRAM
DECK CONTROL
dicom INDUSTRIES INCORPORATED
D 344-90030 P
SCALE NONE
DO NOT SCALE THIS PRINT


DKIR *
DKOR *
DKOS *
DK1S *
WRITP *
READP *
HALTP *
RWNDP *
DILP *
D2LP *
D3LP *
READLP *
WRITLP *
REWLP *
HALTLP *
INIT
INT *
OFFLP *
OFFLINE
ONLINE
ONLP *
HALT *
WRITE
READE
SDR
TTY FEEDBACK
PB 1 *
PB 2 *
PB 3 *
WRIT PB *
READ PB *
HALT PB *
REW PB *
D1 *
D2 *
D3 *
DREW *
POR *
INITLZ-I
OFFLINE PB *
ONLINE PB *
OFLNC-I
ONLINE/OFFLINE LATCH
KYBD(-)
KYBD(+)
PRINT(-)
+12V
-12V
+5V
GND
858 GND
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
Q1 2N3906
Q2 2N3904
CR1 1N914
NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS ARE 1/4W, 5 %.
2. ALL RESISTORS ARE 1.2K
3. DOTTED LINES INCORPORATED IN OPTION Ø6
ISSUE
DESCRIPTION
RESPONSIBILITY
DRAFTING
DATE
DESIGN
DATE
D CN 549-1 ALTMAN 3/70
E CN ALTMAN 6-70
dicom INDUSTRIES INCORPORATED
LOGIC DIAGRAM
OFFLINE CONTROL
LAMP DRIVERS
344-90031
D
E
FAB REV
ASSY REV
DO NOT SCALE THIS PRINT
SCALE NONE



ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
F	CN 549-1	ALTMAN	9/70		
G	CN 581-2	A. ASLAN	10/70		

NOTES:
1. ALL RESISTORS ARE 1/4W 5%.
2. R10 & C13 ARE TO BE SELECTED AT TEST.

J5

dicom INDUSTRIES INCORPORATED

LOGIC DIAGRAM
MOTION CONTROL

D 344-90032 G

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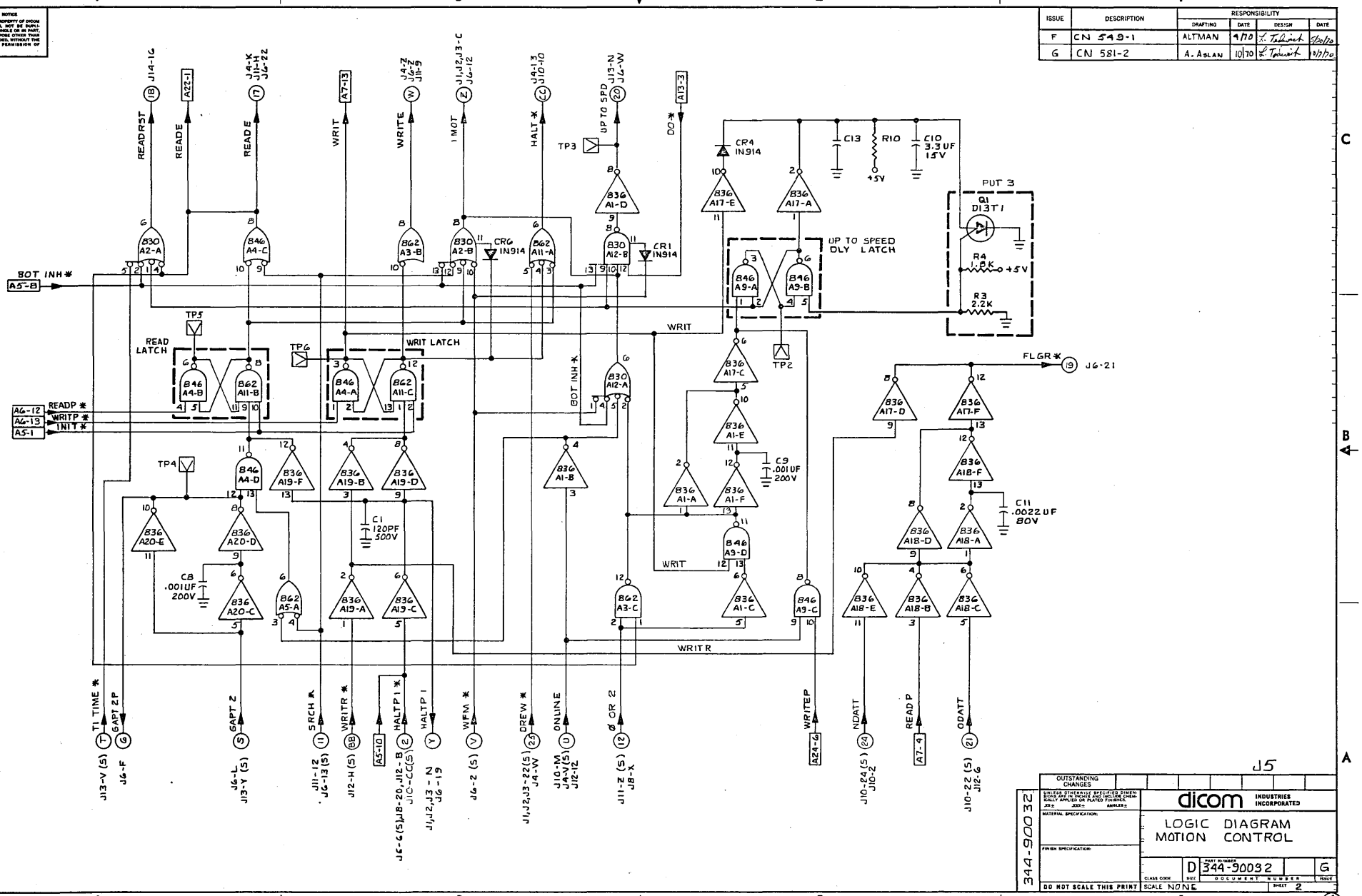
SHEET 1 OF 2

FAB REV | ASSY REV



ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
F	CN 549-1	ALTMAN	9/70	L. Tolbert	9/30/70
G	CN 581-2	A. ASLAN	10/70	L. Tolbert	10/1/70

J5

OUTSTANDING CHANGES

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MATERIAL SPECIFICATION:

FINISH SPECIFICATION:

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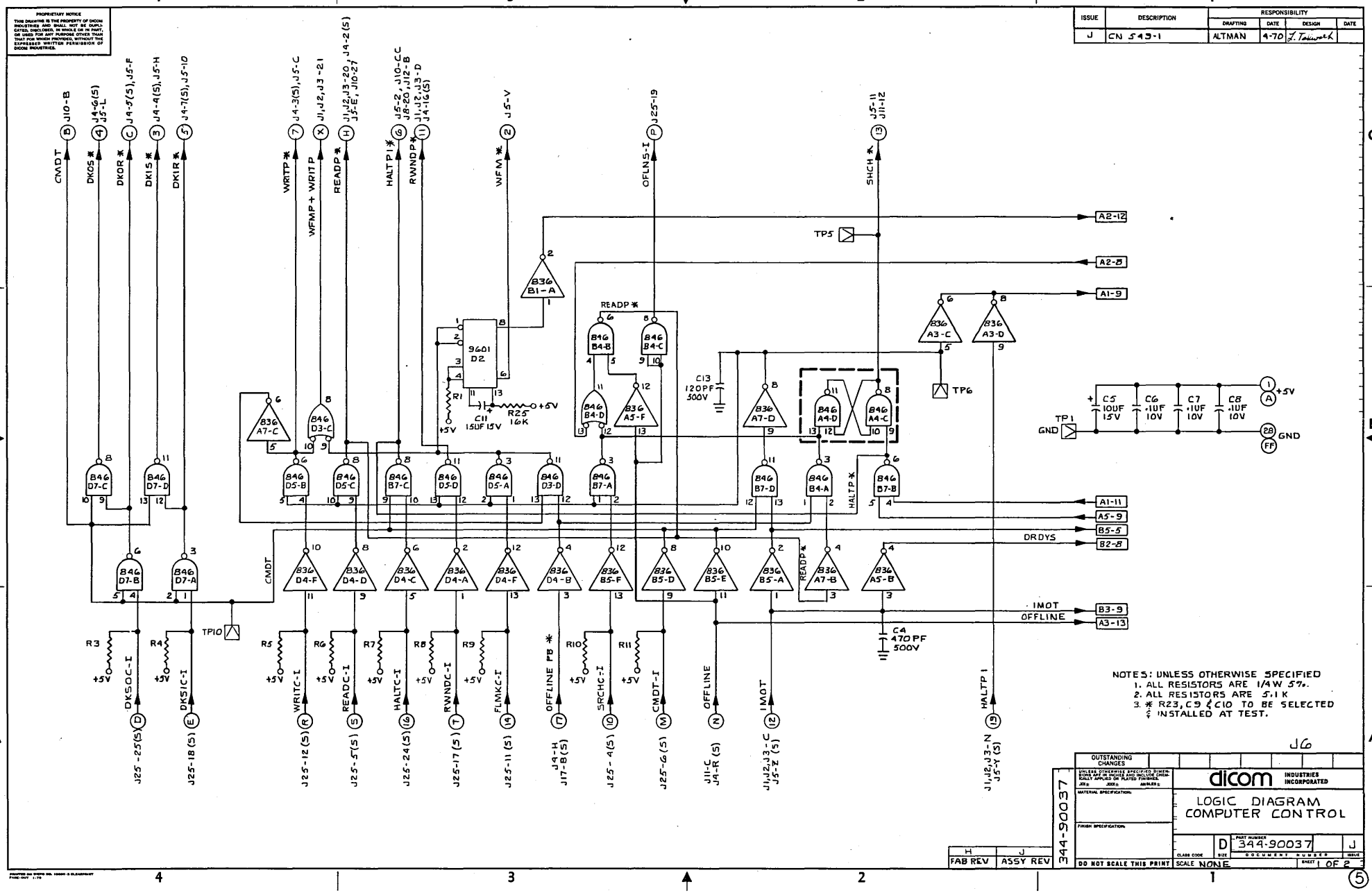
LOGIC DIAGRAM MOTION CONTROL

344-90032

CLASS CODE D SIZE PART NUMBER 344-90032 DOCUMENT NUMBER G ISSUE

SCALE NONE SHEET 2

4



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W 5%.
2. ALL RESISTORS ARE 5.1K
3. * R23, C9 & C10 TO BE SELECTED ‡ INSTALLED AT TEST.

J6

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
J	CN 549-1	ALTMAN	4-70	J. Tallmadge	

FAB REV	ASSY REV
H	J

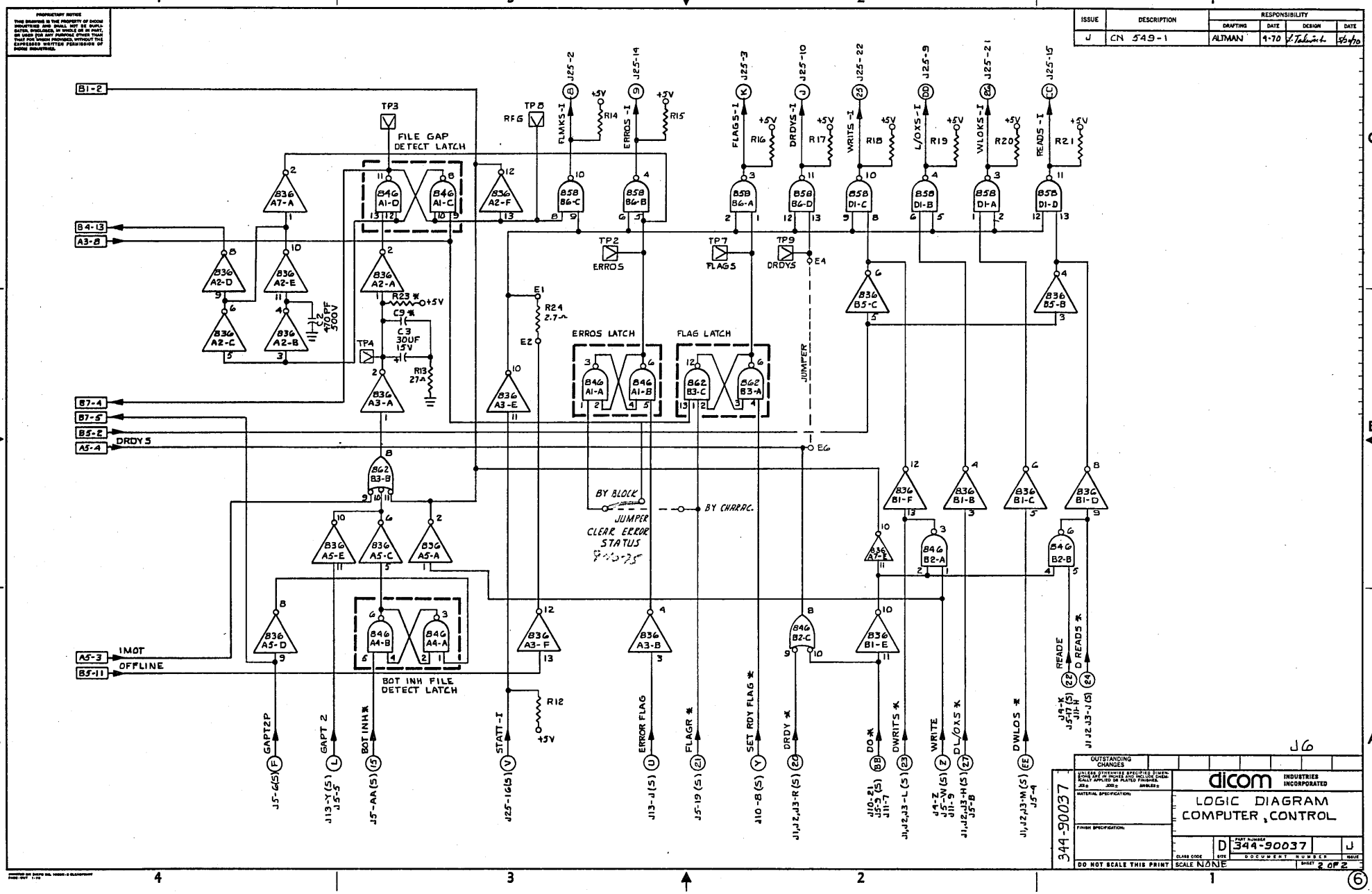
344-90037

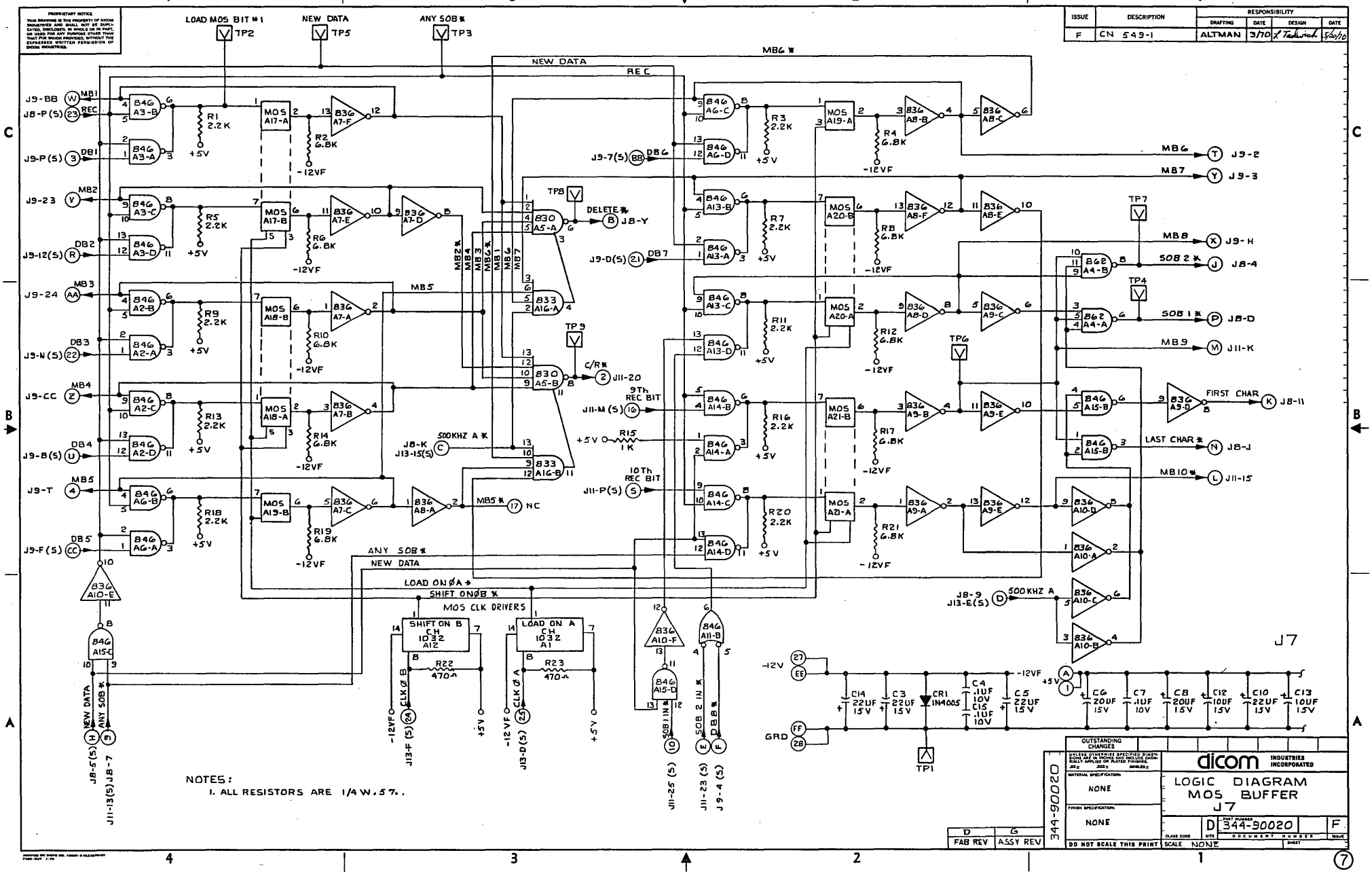
dicom INDUSTRIES INCORPORATED

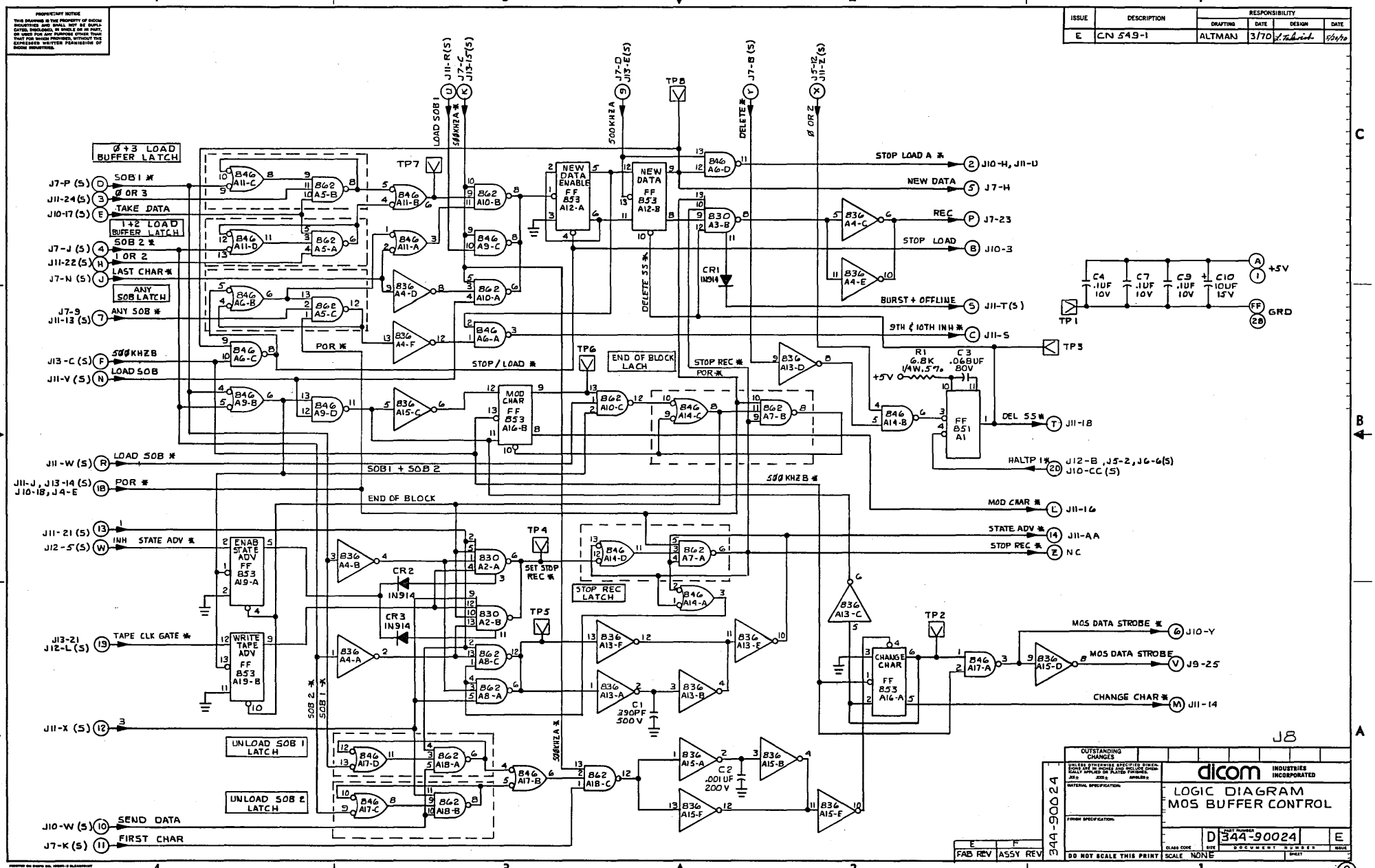
LOGIC DIAGRAM
COMPUTER CONTROL

PART NUMBER 344-90037 D J

DO NOT SCALE THIS PRINT | SCALE NONE | SHEET 1 OF 2


FILE GAP DETECT LATCH
BOT INH FILE DETECT LATCH
ERROS LATCH
FLAG LATCH
JUMPER
BY BLOCK
BY CHARAC.
JUMPER CLEAR ERROR STATUS
B1-2
B4-13
A3-8
B7-4
B7-5
B5-E
DRDYS
A5-4
A5-3
IMOT
B5-11
OFFLINE
GAPT2P
GAPT 2
BOT INH*
STATT-I
ERROR FLAG
FLAGR *
SET RDY FLAG *
DRDY *
DO *
DWRITS *
WRITE
DL/OXS *
DWLOS *
READE
D READS *
ERROS
FLAGS
DRDYS
R23 *
C9 *
C2 470PF 500V
C3 30UF 15V
R13 27A
R24 2.7A
R12
R14
R15
R16
R17
R18
R19
R20
R21
TP2
TP3
TP4
TP7
TP8
TP9
RFG
FLMKS-1
ERROS-1
FLAGS-1
DRDYS-1
WRITS-1
L/OXS-1
WLOKS-1
READS-1
J25-2
J25-14
J25-3
J25-10
J25-22
J25-9
J25-21
J25-15
J5-G(S)
J13-Y(S) J5-5
J5-AA(S)
J25-16(S)
J13-J(S)
J5-19(S)
J10-B(S)
J1,J2,J3-R(S)
J10-P(S) J5-25 J11-7
J1,J2,J3-L(S)
J4-Z J5-W(S) J11-9
J1,J2,J3-H(S) J5-B
J1,J2,J3-N(S) J5-4
J4-K J5-17(S) J11-H
J1,J2,J3-J(S)
J6
344-90037
dicom INDUSTRIES INCORPORATED
LOGIC DIAGRAM COMPUTER, CONTROL
D 344-90037 J
SCALE NONE
SHEET 2 OF 2
DO NOT SCALE THIS PRINT
ISSUE J
DESCRIPTION CN 549-1
RESPONSIBILITY DRAFTING ALTMAN 9-70
DESIGN J. Talbert 9/24/70
OUTSTANDING CHANGES


LOAD MOS BIT #1
TP2
NEW DATA
TP5
ANY SOB *
TP3
MB6 *
NEW DATA REC
J9-BB W MB1
J8-P(S) 23 REC
J9-P(S) 3 DB1
J9-23 V MB2
J9-12(S) R DB2
J9-24 AA MB3
J9-N(S) 22 DB3
J9-CC Z MB4
J9-B(S) U DB4
J9-T 4 MB5
J9-F(S) CC DB5
R1 2.2K
R2 6.8K
R5 2.2K
R6 6.8K
R9 2.2K
R10 6.8K
R13 2.2K
R14 6.8K
R18 2.2K
R19 6.8K
+5V
-12VF
MB2 *
MB4
MB3
MB5 *
MB1
MB6
MB7
MB5
TP8
DELETE *
B J8-Y
TP9
C/R *
2 J11-20
J8-K J13-15(S) C 500KHZ A *
J9-7(5) BB DB6
J9-D(5) 21 DB7
J11-M(S) 16 9Th REC BIT
J11-P(S) 5 10Th REC BIT
R3 2.2K
R4 6.8K
R7 2.2K
R8 6.8K
R11 2.2K
R12 6.8K
R15 1K
R16 2.2K
R17 6.8K
R20 2.2K
R21 6.8K
MB6 T J9-2
MB7 Y J9-3
TP7
MB8 X J9-H
SOB 2 * J J8-4
TP4
SOB 1 * P J8-D
MB9 M J11-K
TP6
FIRST CHAR K J8-11
LAST CHAR * N J8-J
MB10 * L J11-15
17 NC MB5 *
ANY SOB *
NEW DATA
LOAD ON ØA *
SHIFT ON ØB *
MOS CLK DRIVERS
SHIFT ON B CH 1032 A12
LOAD ON A CH 1032 A1
R22 470Ω
R23 470Ω
-12VF CLK Ø B 24 J13-F (S)
-12VF CLK Ø A 25 J13-D (S)
+5V
J8-9 J13-E(S) D 500KHZ A
J7
-12V 27 EE
GRD FF 28
C14 22UF 15V
C3 22UF 15V
CR1 IN4005
C4 .1UF 10V
C15 .1UF 10V
C5 22UF 15V
C6 20UF 15V
C7 .1UF 10V
C8 20UF 15V
C12 10UF 15V
C10 22UF 15V
C13 10UF 15V
TP1
J8-5(S) H NEW DATA
J11-13(S) J8-7 3 ANY SOB *
J11-25 (5) 10 SOB 1 IN *
J11-23 (5) E SOB 2 IN *
J9-4 (5) K DB8 *
NOTES:
1. ALL RESISTORS ARE 1/4 W. 5%.
ISSUE F
DESCRIPTION CN 549-1
RESPONSIBILITY DRAFTING ALTMAN 3/70 DESIGN
OUTSTANDING CHANGES
MATERIAL SPECIFICATION: NONE
FINISH SPECIFICATION: NONE
dicom INDUSTRIES INCORPORATED
LOGIC DIAGRAM MOS BUFFER J7
PART NUMBER D 344-90020 F
CLASS CODE SIZE DOCUMENT NUMBER ISSUE
SCALE NONE SHEET
DO NOT SCALE THIS PRINT
344-90020
D FAB REV G ASSY REV
7



ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
E	CN 549-1	ALTMAN	3/70		5/6/70

OUTSTANDING CHANGES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES EQUALLY APPLIED OR PLATED FINISHES .XX ± .010 .XXX ± .005
MATERIAL SPECIFICATION:
FINISH SPECIFICATION:
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dicom INDUSTRIES INCORPORATED

LOGIC DIAGRAM
MOS BUFFER CONTROL

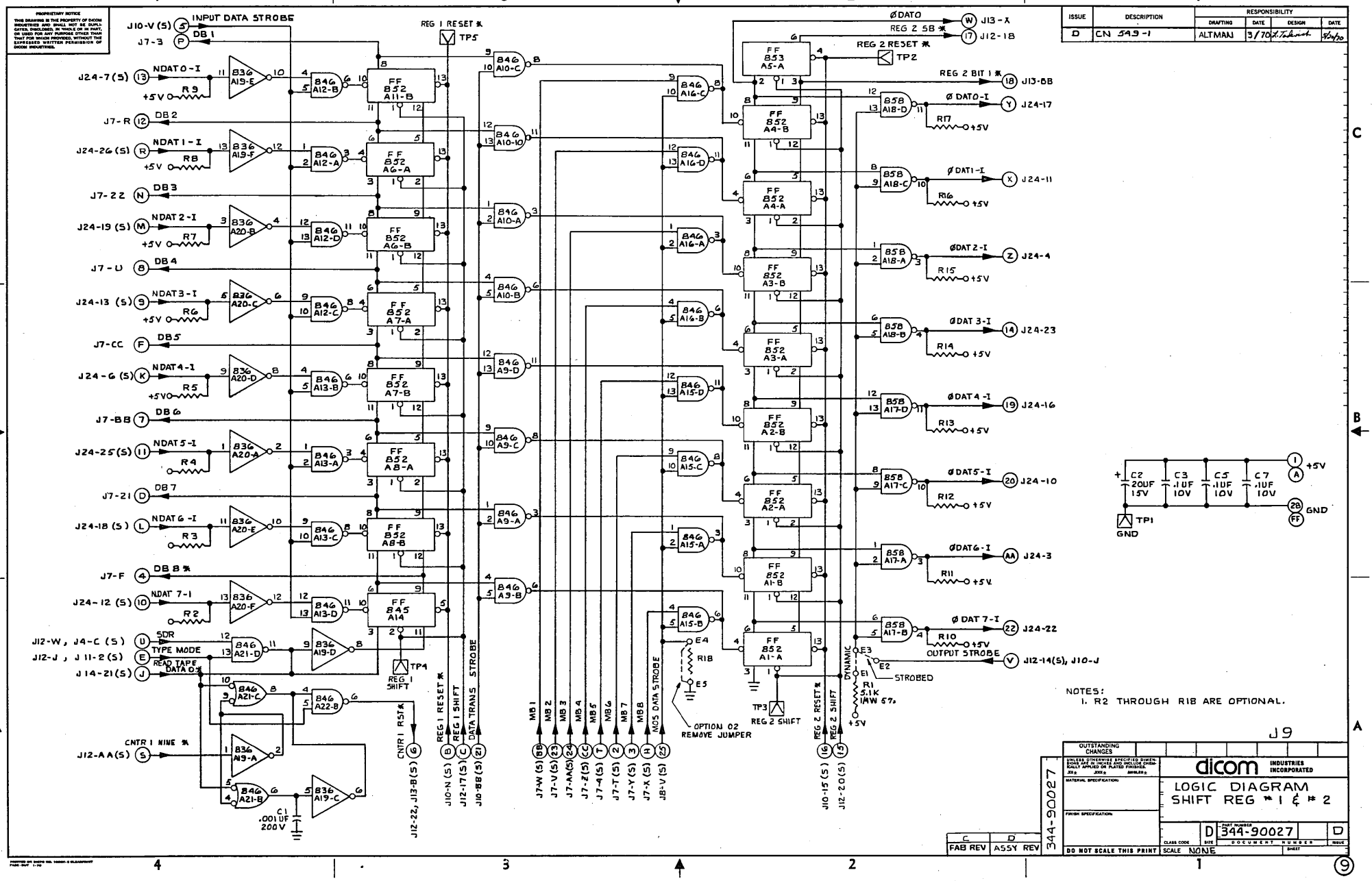
FAB REV	ASSY REV
E	F

344-90024

CLASS CODE	SIZE	PART NUMBER / DOCUMENT NUMBER	ISSUE
	D	344-90024	E

SCALE NONE

SHEET 8



ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
D	CN 549-1	ALTMAN	3/70		

J9

dicom INDUSTRIES INCORPORATED

LOGIC DIAGRAM
SHIFT REG # 1 & # 2

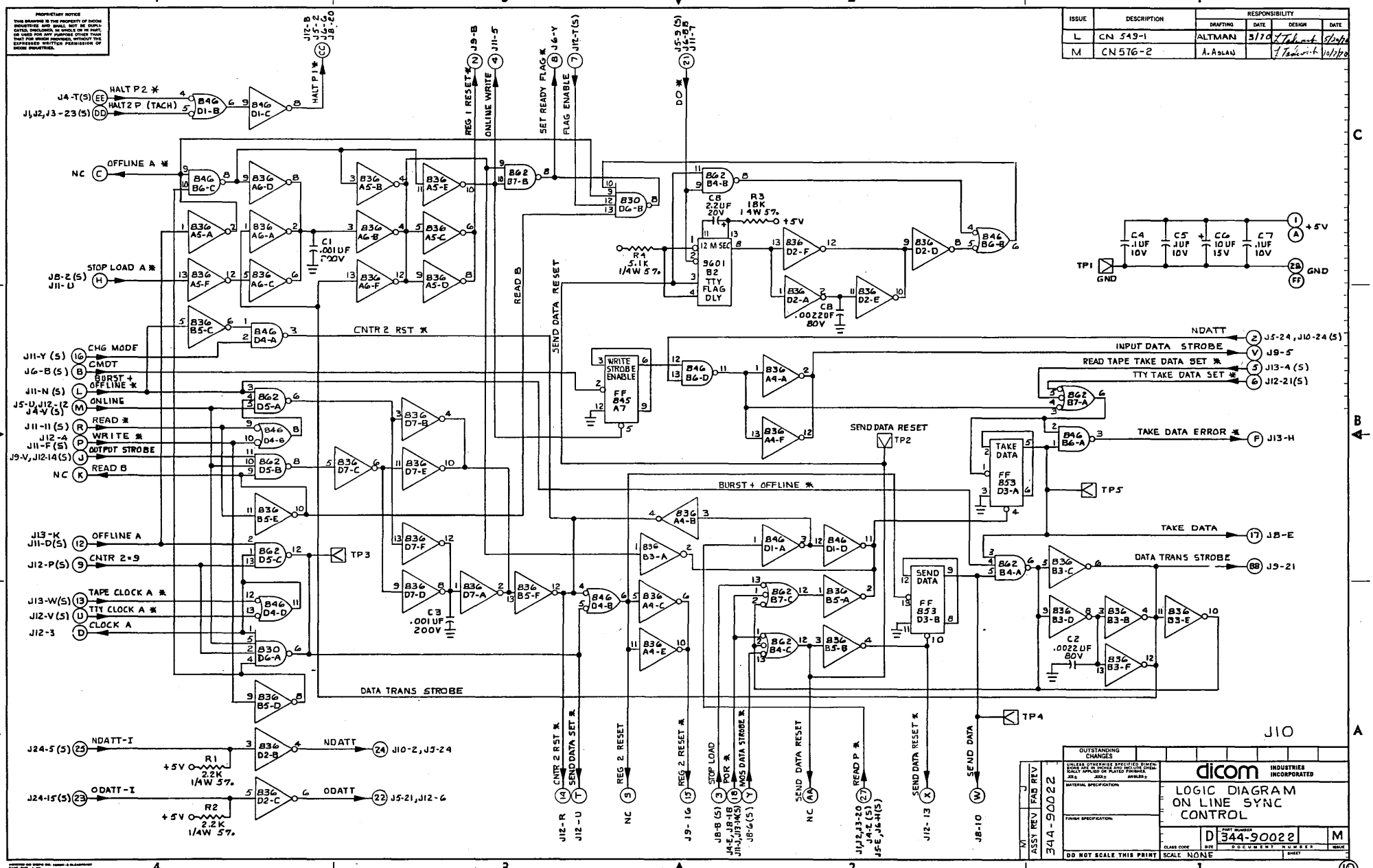
C FAB REV	D ASSY REV

344-90027

D 344-90027 D

SCALE NONE

DO NOT SCALE THIS PRINT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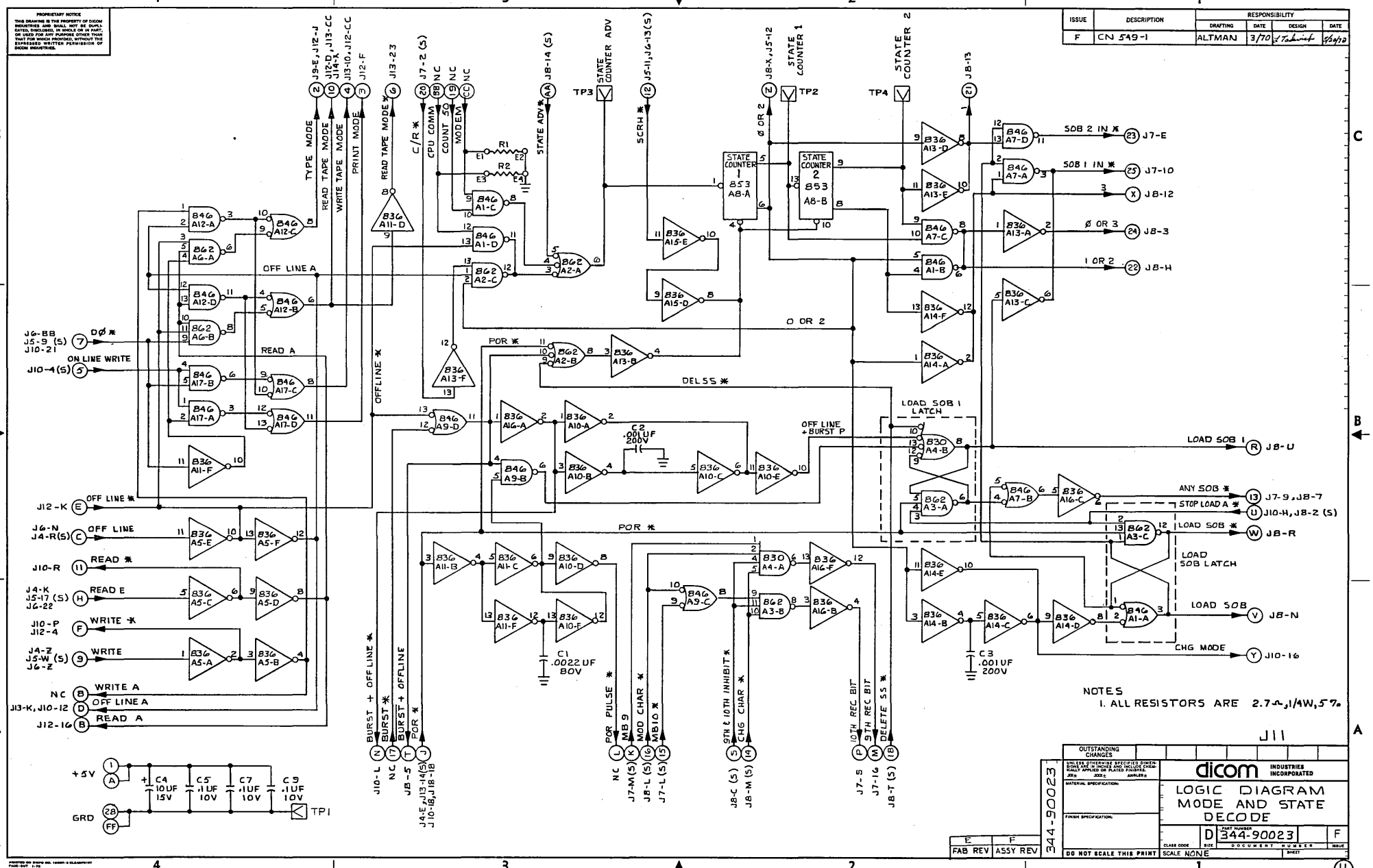
ISSUE | DESCRIPTION | RESPONSIBILITY | DRAFTING | DATE | DESIGN | DATE
L | CN 549-1 | ALTMAN | 3/70 | J Tedesco | 5/20/70
M | CN 576-2 | A. ASLAN | | J Tedesco | 10/12/70
HALT P2 *
HALT2 P (TACH)
HALT P1 *
REG 1 RESET *
ONLINE WRITE
SET READY FLAG *
FLAG ENABLE
DO *
OFFLINE A *
STOP LOAD A *
CHG MODE
BURST + OFFLINE *
ONLINE
READ *
WRITE *
OUTPUT STROBE
READ B
CNTR 2 RST *
SEND DATA RESET
WRITE STROBE ENABLE
FF 845 A7
12 M SEC
9601 B2 TTY FLAG DLY
R1 2.2K 1/4W 5%
R2 2.2K 1/4W 5%
R3 18K 1 4W 5%
R4 5.1K 1/4W 5%
C1 .001UF 200V
C2 .0022UF 80V
C3 .001UF 200V
C4 .1UF 10V
C5 .1UF 10V
C6 10UF 15V
C7 .1UF 10V
C8 2.2UF 20V
C8 .0022UF 80V
+5V
GND
TP1
TP2
TP3
TP4
TP5
NDATT
INPUT DATA STROBE
READ TAPE TAKE DATA SET *
TTY TAKE DATA SET *
TAKE DATA ERROR *
TAKE DATA
DATA TRANS STROBE
SEND DATA
TAKE DATA
FF 853 D3-A
SEND DATA
FF 853 D3-B
NDATT-I
ODATT-I
NDATT
ODATT
J10
dicom INDUSTRIES INCORPORATED
LOGIC DIAGRAM
ON LINE SYNC
CONTROL
PART NUMBER D 344-90022 M
DO NOT SCALE THIS PRINT
SCALE NONE
ASSY REV FAB REV
344-90022
OUTSTANDING CHANGES
for overall board
D⇒C 4⇒3
3⇒2 5⇒4
2⇒1 6⇒5
7⇒6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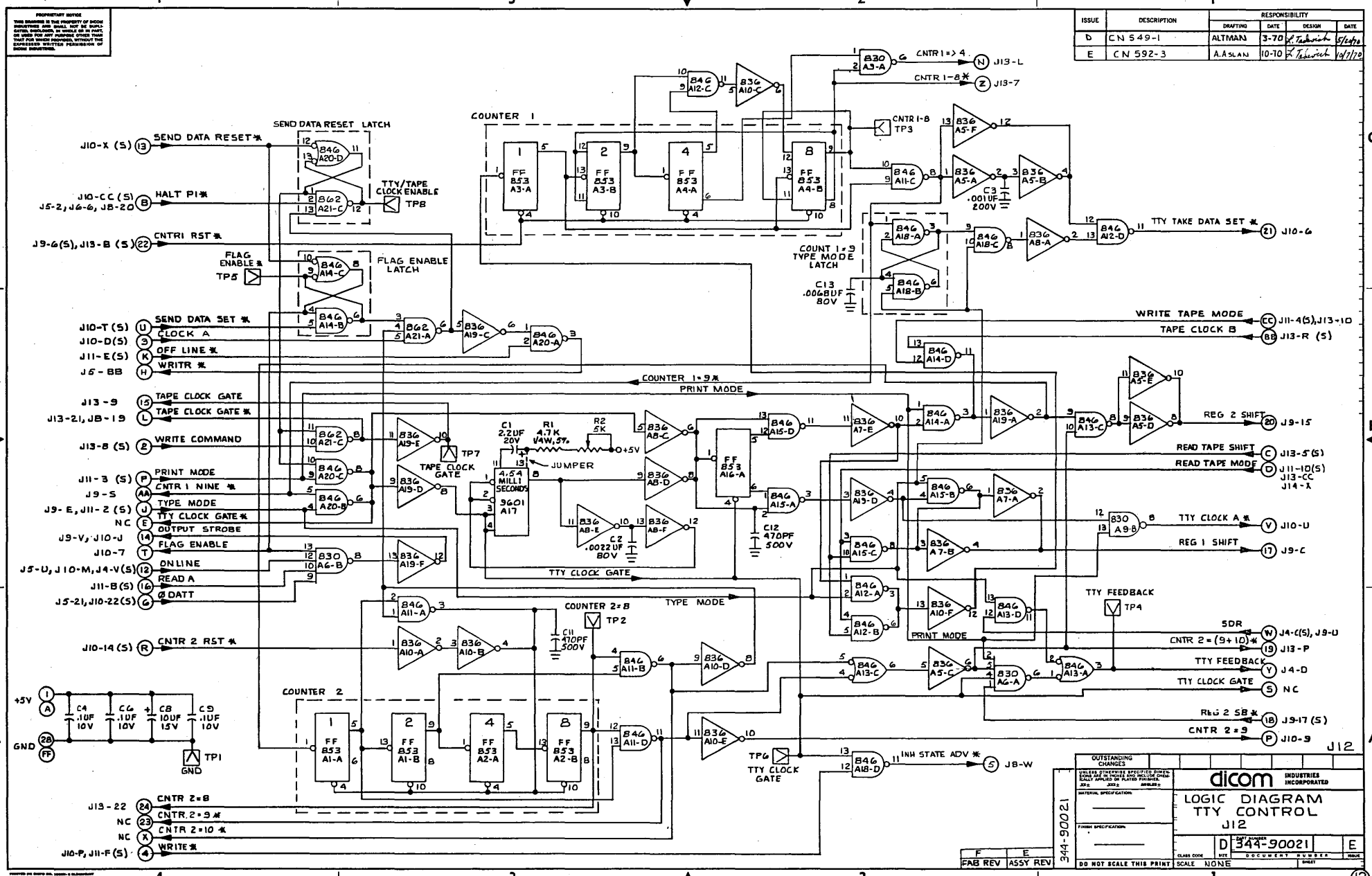
ISSUE
DESCRIPTION
RESPONSIBILITY
DRAFTING
DATE
DESIGN
DATE
F
CN 549-1
ALTMAN
3/70
TYPE MODE
READ TAPE MODE
WRITE TAPE MODE
PRINT MODE
READ TAPE MODE *
C/R *
CPU COMM
COUNT
MODEM
STATE ADV *
SCRH *
STATE COUNTER ADV
STATE COUNTER 1
STATE COUNTER 2
TP1
TP2
TP3
TP4
R1
R2
OFF LINE A
READ A
ON LINE WRITE
OFFLINE *
POR *
DELSS *
Ø OR 2
1 OR 2
LOAD SOB 1 LATCH
OFF LINE + BURST P
LOAD SOB 1
ANY SOB *
STOP LOAD A *
LOAD SOB *
LOAD SOB LATCH
LOAD SOB
CHG MODE
SOB 2 IN *
SOB 1 IN *
Ø OR 3
1 OR 2
C1 .0022 UF 80V
C2 .001UF 200V
C3 .001 UF 200V
C4 10UF 15V
C5 .1UF 10V
C7 .1UF 10V
C9 .1UF 10V
+5V
GRD
BURST + OFF LINE *
BURST *
BURST + OFFLINE
POR PULSE *
MB 9
MOD CHAR *
MB10 *
9TH & 10TH INHIBIT *
9TH CHG CHAR *
10TH REC BIT
9TH REC BIT
DELETE SS *
NOTES
1. ALL RESISTORS ARE 2.7 K, 1/4W, 5%
J11
OUTSTANDING CHANGES
dicom INDUSTRIES INCORPORATED
LOGIC DIAGRAM MODE AND STATE DECODE
D 344-90023 F
SCALE NONE
DO NOT SCALE THIS PRINT
E FAB REV
F ASSY REV
344-90023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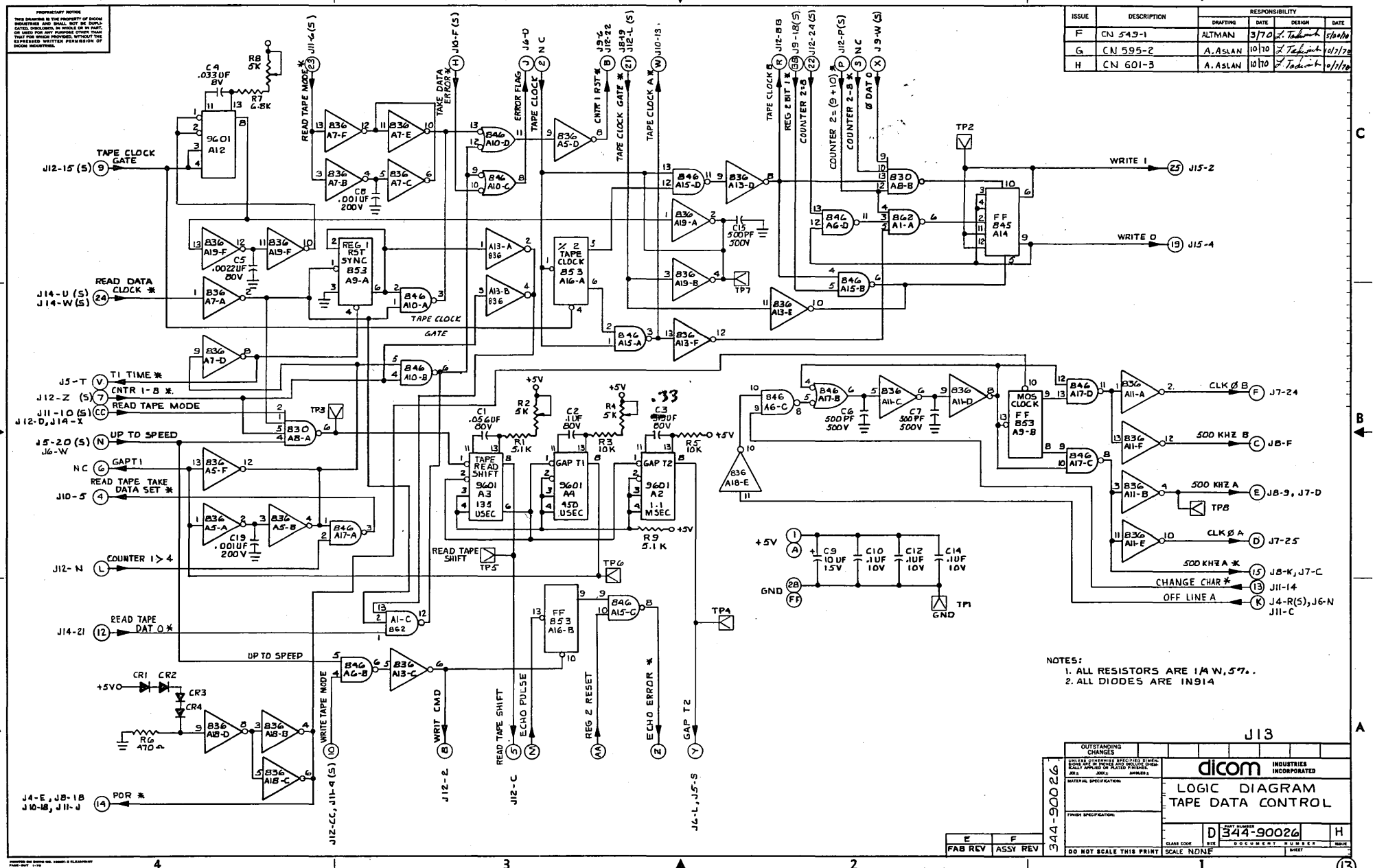
ISSUE | DESCRIPTION | RESPONSIBILITY | DRAFTING | DATE | DESIGN | DATE
D | CN 549-1 | ALTMAN | 3-70 | L. Tabrisch | 5/24/70
E | CN 592-3 | A.ASLAN | 10-70 | L. Tabrisch | 10/7/70
COUNTER 1
COUNTER 2
SEND DATA RESET LATCH
FLAG ENABLE LATCH
COUNT 1=9 TYPE MODE LATCH
TTY/TAPE CLOCK ENABLE
TP8
FLAG ENABLE
TP5
TAPE CLOCK GATE
TP7
TYPE MODE
TP2
TTY FEEDBACK
TP4
TTY CLOCK GATE
TP6
TP1
CNTR 1=8
TP3
JUMPER
J10-X (S) SEND DATA RESET *
J10-CC (S) HALT PI *
J5-2, J6-6, J8-20
J9-6(S), J13-8 (S) CNTR1 RST *
J10-T (S) SEND DATA SET *
J10-D(S) CLOCK A
J11-E(S) OFF LINE *
J5-BB WRITR *
J13-9 TAPE CLOCK GATE
J13-21, J8-19 TAPE CLOCK GATE *
J13-8 (S) WRITE COMMAND
J11-3 (S) PRINT MODE
J9-5 CNTR 1 NINE *
J9-E, J11-2 (S) TYPE MODE
NC TTY CLOCK GATE *
NC OUTPUT STROBE
J9-V, J10-J FLAG ENABLE
J10-7 ON LINE
J5-U, J10-M, J4-V(S) READ A
J11-B(S) ØDATT
J5-21, J10-22(S)
J10-14 (S) CNTR 2 RST *
J13-22 CNTR 2=8
NC CNTR 2=9 *
NC CNTR 2=10 *
J10-P, J11-F (S) WRITE *
+5V
GND
C4 .1UF 10V
C6 .1UF 10V
C8 10UF 15V
C9 .1UF 10V
C1 2.2UF 20V
R1 4.7K 1/4W, 5%
R2 5K
+5V
C2 .0022 UF 80V
C3 .001UF 200V
C11 470PF 500V
C12 470PF 500V
C13 .006BUF 80V
4.54 MILLI SECONDS
9601 A17
CNTR 1=>4
CNTR 1=8 *
J13-L
J13-7
TTY TAKE DATA SET *
J10-6
WRITE TAPE MODE
TAPE CLOCK B
J11-4(S), J13-10
J13-R (S)
COUNTER 1=9 *
PRINT MODE
REG 2 SHIFT
J9-15
READ TAPE SHIFT
READ TAPE MODE
J13-5(S)
J11-10(S)
J13-CC
J14-X
TTY CLOCK A *
J10-U
REG 1 SHIFT
J9-C
COUNTER 2=8
TYPE MODE
PRINT MODE
SDR
J4-C(S), J9-U
CNTR 2=(9+10) *
J13-P
TTY FEEDBACK
J4-D
TTY CLOCK GATE
NC
REG 2 SB *
J9-17 (S)
CNTR 2=9
J10-9
INH STATE ADV *
J8-W
J12
OUTSTANDING CHANGES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICAL APPLICATION PLATED FINISHES.
MATERIAL SPECIFICATION
FINISH SPECIFICATION
DO NOT SCALE THIS PRINT
dicom INDUSTRIES INCORPORATED
LOGIC DIAGRAM
TTY CONTROL
J12
344-90021
D
E
FAB REV
ASSY REV
SCALE NONE
SHEET
12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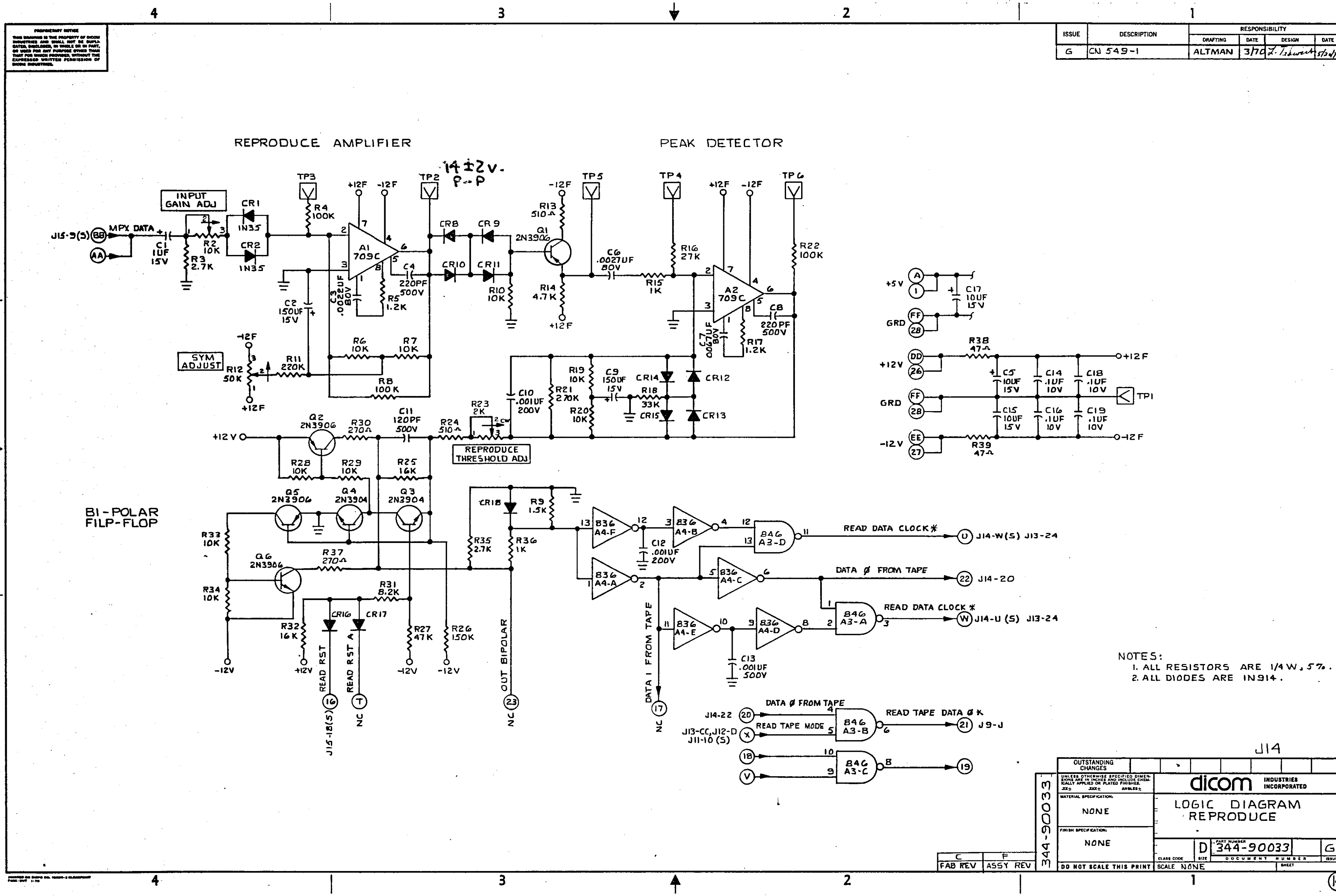
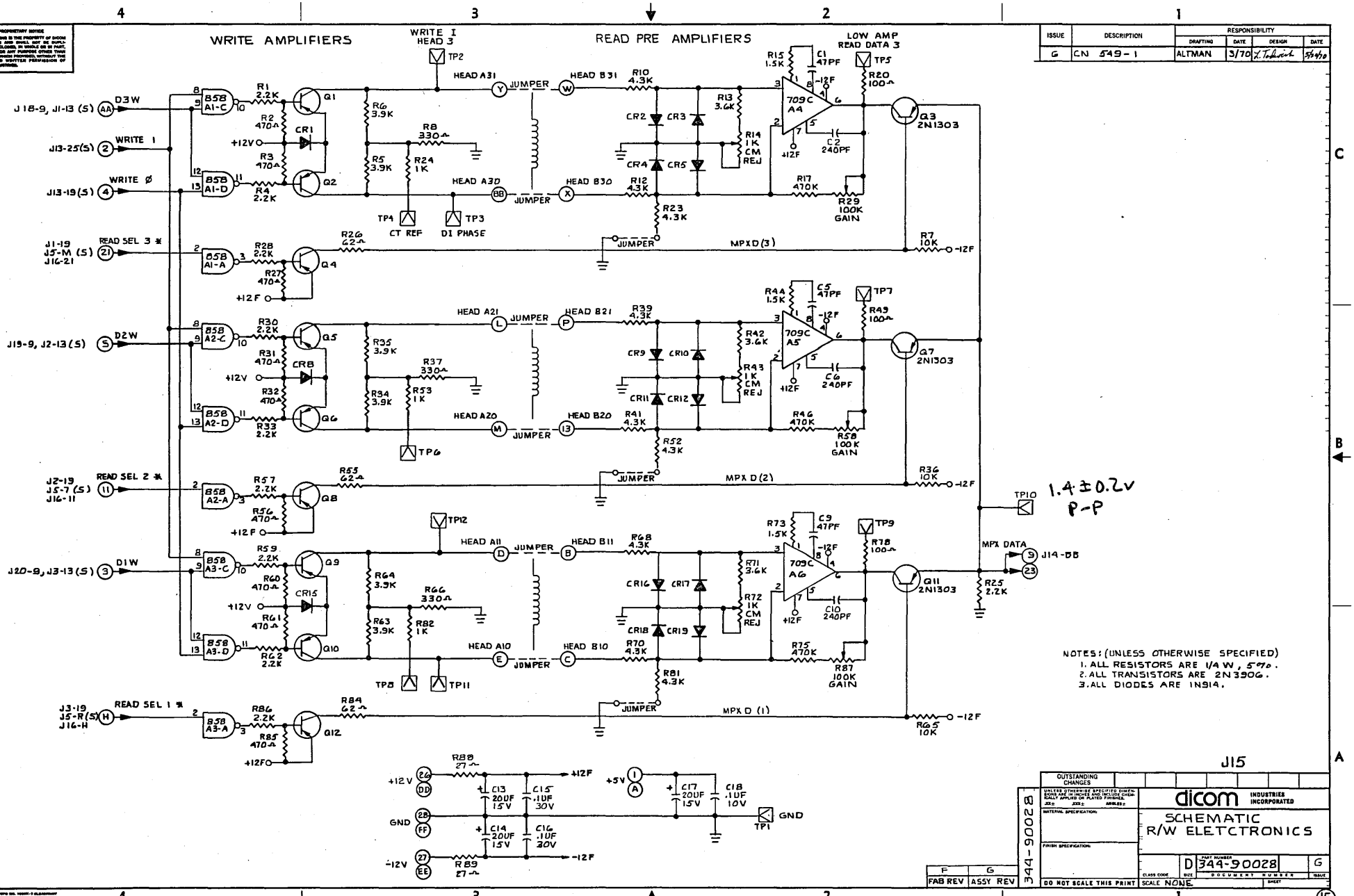
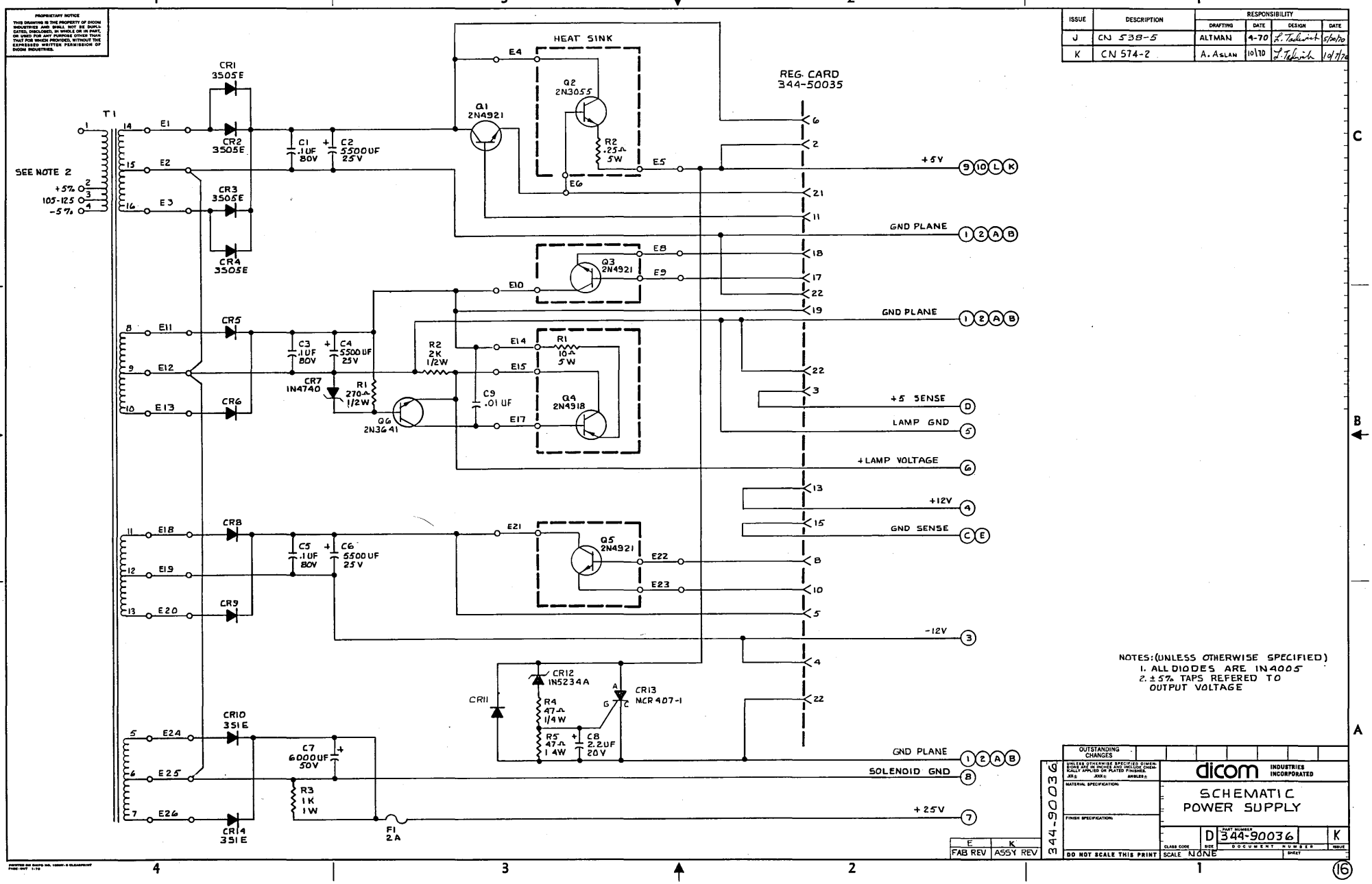
ISSUE | DESCRIPTION | RESPONSIBILITY | DRAFTING | DATE | DESIGN | DATE
F | CN 549-1 | ALTMAN | 3/70 | L. Tedesco | 5/20/70
G | CN 595-2 | A. ASLAN | 10/70 | L. Tedesco | 10/7/70
H | CN 601-3 | A. ASLAN | 10/70 | L. Tedesco | 9/1/70
TAPE CLOCK GATE
READ DATA CLOCK *
T1 TIME *
CNTR 1-8 *
READ TAPE MODE
UP TO SPEED
GAP T1
READ TAPE TAKE DATA SET *
COUNTER 1>4
READ TAPE DAT 0 *
POR *
WRITE 1
WRITE 0
CLK Ø B
500 KHZ B
500 KHZ A
CLK Ø A
500 KHZ A *
CHANGE CHAR *
OFF LINE A
TAPE CLOCK GATE
GAP T2
WRIT CMD
ECHO PULSE
REG 2 RESET
ECHO ERROR *
WRITE TAPE MODE
NOTES:
1. ALL RESISTORS ARE 1/4 W, 5%.
2. ALL DIODES ARE IN914
J13
OUTSTANDING CHANGES
DO NOT SCALE THIS PRINT
MATERIAL SPECIFICATION:
FINISH SPECIFICATION:
dicom INDUSTRIES INCORPORATED
LOGIC DIAGRAM
TAPE DATA CONTROL
344-90026
D
H
SCALE NONE
E FAB REV
F ASSY REV

3.3



REPRODUCE AMPLIFIER
PEAK DETECTOR
14±2V. P-P
INPUT GAIN ADJ
SYM ADJUST
REPRODUCE THRESHOLD ADJ
BI-POLAR FILP-FLOP
J15-9(S) MPX DATA
READ DATA CLOCK*
J14-W(S) J13-24
DATA Ø FROM TAPE
J14-20
READ DATA CLOCK*
J14-U (S) J13-24
DATA I FROM TAPE
READ RST
READ RST A
OUT BIPOLAR
J15-18(S)
J14-22
READ TAPE MODE
J13-CC, J12-D J11-10 (S)
READ TAPE DATA Ø K
J9-J
+5V
GRD
+12V
-12V
+12F
-12F
NOTES:
1. ALL RESISTORS ARE 1/4W, 5%.
2. ALL DIODES ARE IN914.
J14
ISSUE G
DESCRIPTION CN 549-1
DRAFTING ALTMAN
DATE 3/70
dicom INDUSTRIES INCORPORATED
LOGIC DIAGRAM REPRODUCE
MATERIAL SPECIFICATION: NONE
FINISH SPECIFICATION: NONE
D 344-90033 G
SCALE NONE
DO NOT SCALE THIS PRINT
FAB REV C
ASSY REV F
344-90033


WRITE AMPLIFIERS
READ PRE AMPLIFIERS
WRITE I HEAD 3
LOW AMP READ DATA 3
J18-9, J1-13 (S)
D3W
J13-25(S)
WRITE 1
J13-19(S)
WRITE Ø
J1-19 J5-M (S) J16-21
READ SEL 3 *
J19-9, J2-13(S)
D2W
J2-19 J5-7 (S) J16-11
READ SEL 2 *
J20-9, J3-13 (S)
D1W
J3-19 J5-R(S) J16-H
READ SEL 1 *
HEAD A31
HEAD B31
HEAD A30
HEAD B30
HEAD A21
HEAD B21
HEAD A20
HEAD B20
HEAD A11
HEAD B11
HEAD A10
HEAD B10
JUMPER
MPXD(3)
MPX D(2)
MPX D (1)
CT REF
D1 PHASE
709C A4
709C A5
709C A6
2N1303
MPX DATA
J14-B8
1.4±0.2V P-P
J15
GND
+12V
-12V
+5V
-12F
+12F
NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS ARE 1/4 W, 5%.
2. ALL TRANSISTORS ARE 2N3906.
3. ALL DIODES ARE 1N914.
dicom INDUSTRIES INCORPORATED
SCHEMATIC
R/W ELETCTRONICS
344-90028
ALTMAN
3/70
DO NOT SCALE THIS PRINT
SCALE NONE



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIODES ARE IN4005
2. ±5% TAPS REFERED TO OUTPUT VOLTAGE

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
J	CN 538-5	ALTMAN	4-70	L. Tabisch	5/20/70
K	CN 574-2	A. ASLAN	10/70	L. Tabisch	10/7/70

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OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES AS FOLLOWS: DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL SPECIFICATION:

FINISH SPECIFICATION:

DO NOT SCALE THIS PRINT

dicom INDUSTRIES INCORPORATED

SCHEMATIC
POWER SUPPLY

344-90036

FAB REV	ASSY REV
E	K

CLASS CODE D | PART NUMBER 344-90036 | ISSUE K

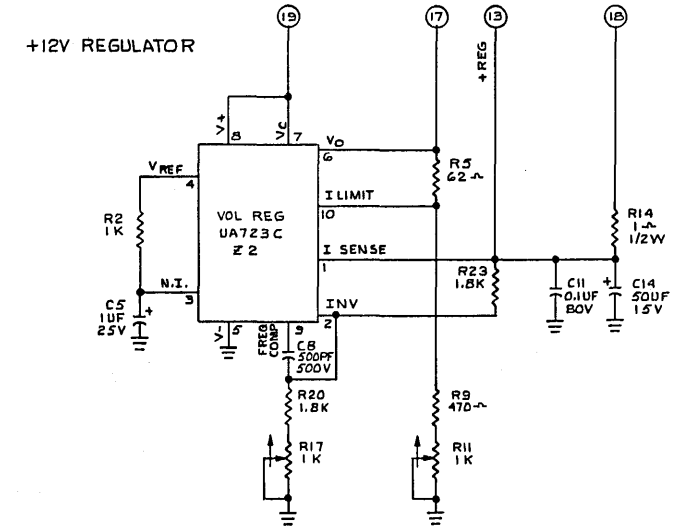
SIZE | DOCUMENT NUMBER | SHEET

SCALE NONE

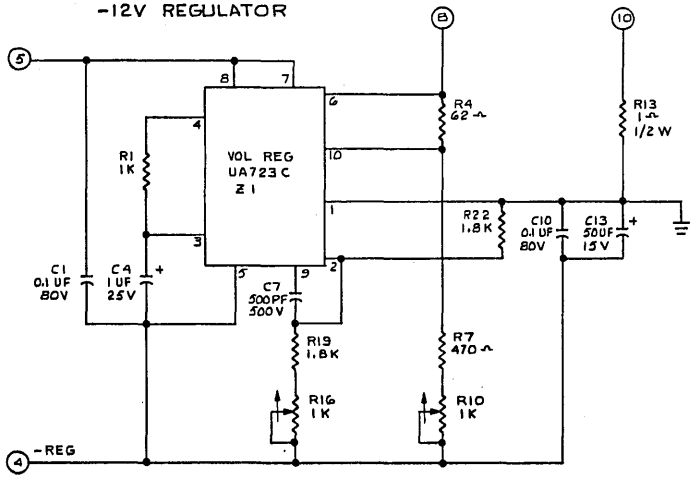
16

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
E	CN 549-1	AJMAN	4/70	J. Tabrisky	5/4/70

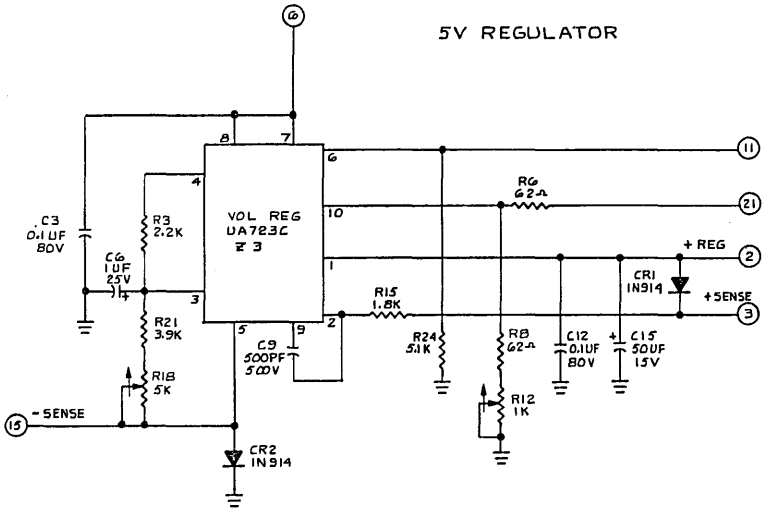
+12V REGULATOR

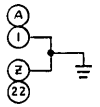


-12V REGULATOR



5V REGULATOR





NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS ARE 1/4W 5%.

C	E
FAB REV	ASSY REV

344-90035

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE APPLIED ON RATED FINISHES.
.XX ± .XXX ±
MATERIAL SPECIFICATION:
FINISH SPECIFICATION:

DO NOT SCALE THIS PRINT

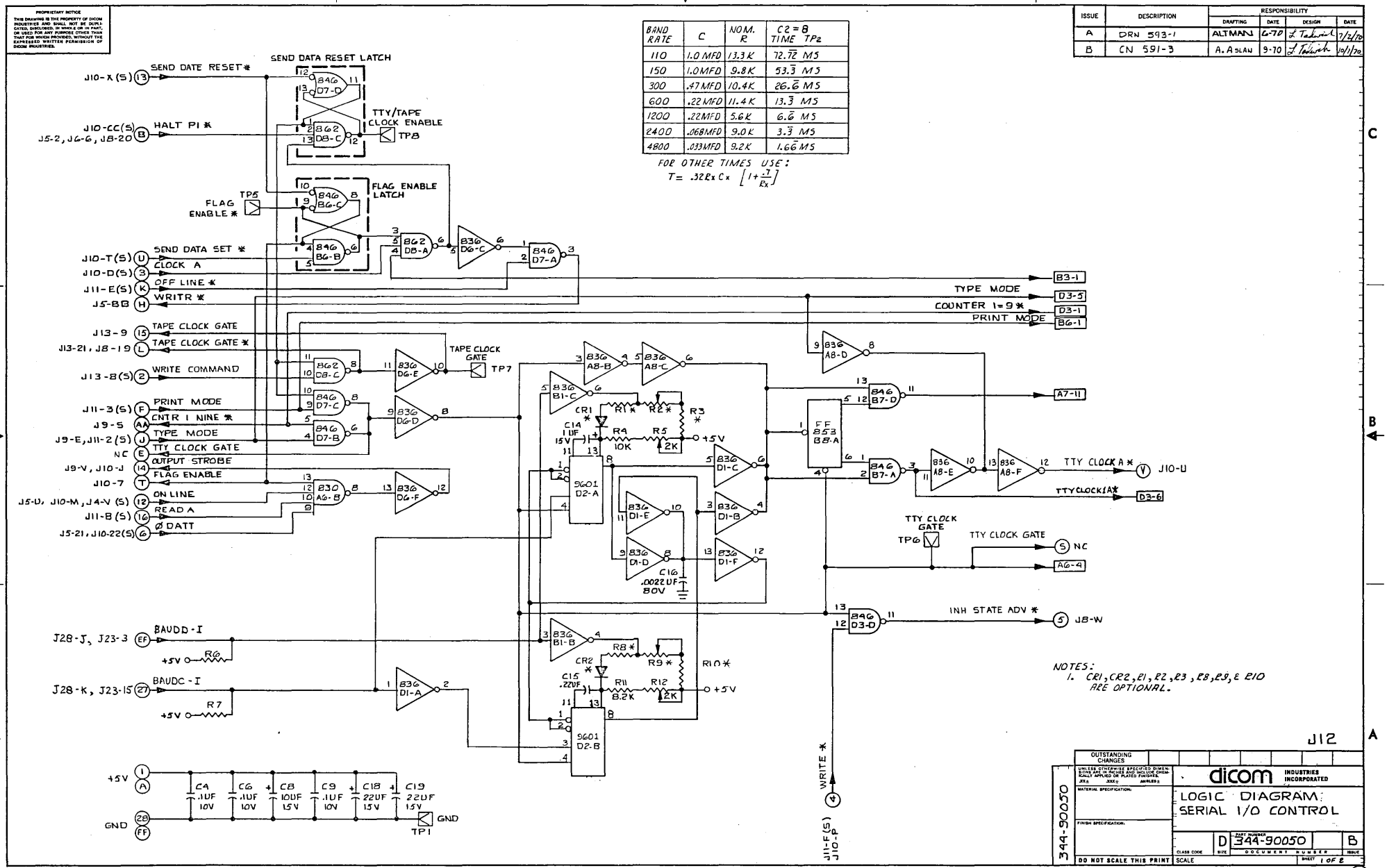
dicom INDUSTRIES INCORPORATED

SCHEMATIC
REGULATOR CARD

CLASS CODE D | SIZE | PART NUMBER 344-90035 | DOCUMENT NUMBER | ISSUE E | SHEET

SCALE NONE

17



BAND RATE	C	NOM. R	C2=8 TIME TP2
110	1.0 MFD	13.3 K	72.72 MS
150	1.0 MFD	9.8 K	53.3 MS
300	.47 MFD	10.4 K	26.6 MS
600	.22 MFD	11.4 K	13.3 MS
1200	.22 MFD	5.6 K	6.6 MS
2400	.068 MFD	9.0 K	3.3 MS
4800	.033 MFD	9.2 K	1.66 MS

FOR OTHER TIMES USE:
$T = .32R_X C_X \left[1 + \frac{7}{R_X}\right]$

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
A	DRN 593-1	ALTMAN	6-70	L Talbert	7/2/70
B	CN 591-3	A. ASLAN	9-70	L Talbert	10/1/70

NOTES:
1. CR1, CR2, R1, R2, R3, R8, R9, & R10 ARE OPTIONAL.

OUTSTANDING CHANGES

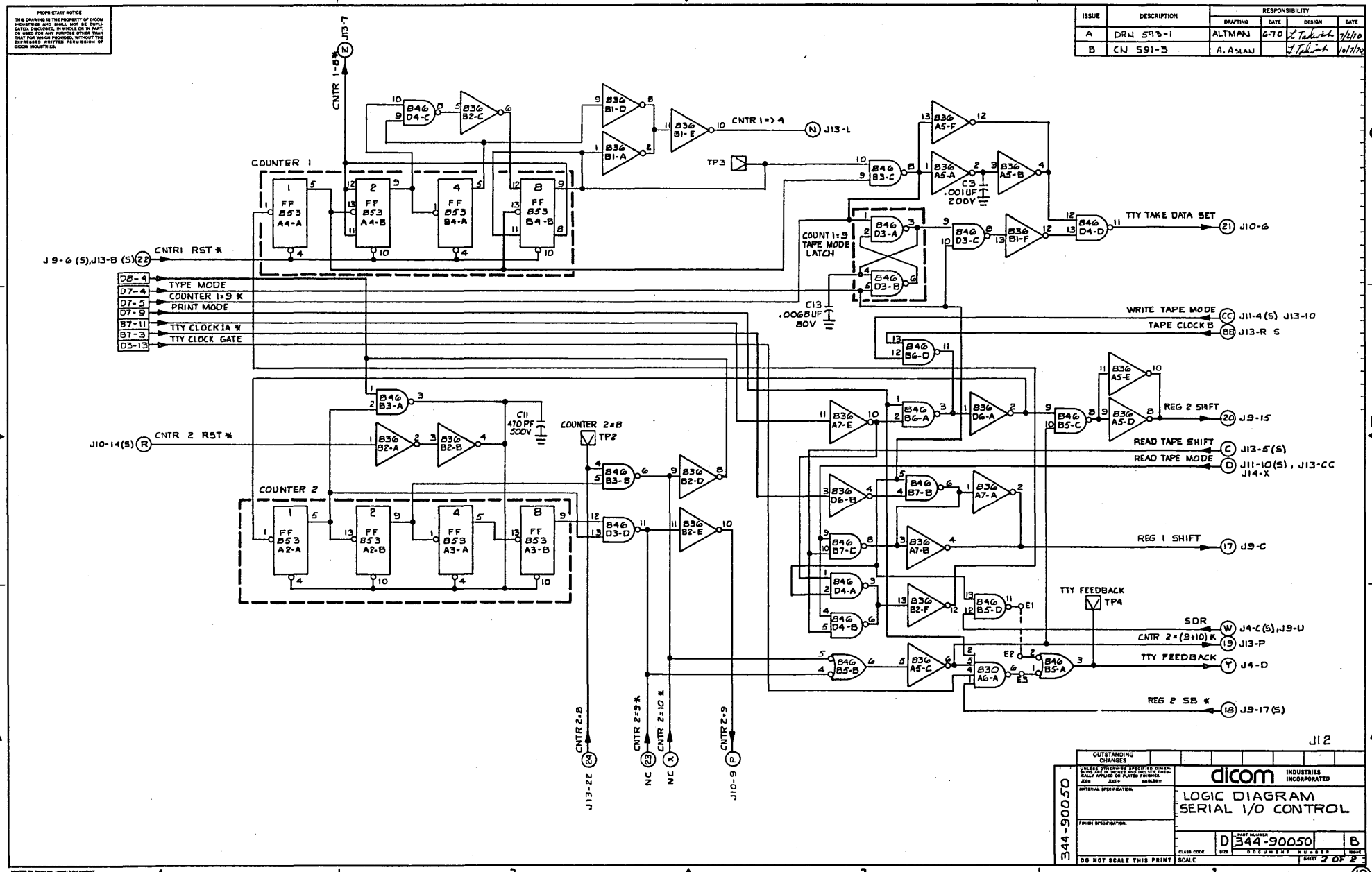
dicom INDUSTRIES INCORPORATED

LOGIC DIAGRAM: SERIAL I/O CONTROL

344-90050

D | 344-90050 | B

DO NOT SCALE THIS PRINT | SCALE | SHEET 1 OF 2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ISSUE | DESCRIPTION | RESPONSIBILITY | DRAFTING | DATE | DESIGN | DATE
A | DRN 593-1 | ALTMAN | 6-70 | J. Tedwick | 7/2/70
B | CN 591-3 | A. ASLAN | | J. Tedwick | 10/7/70
COUNTER 1
COUNTER 2
CNTR 1-8
CNTR 1=>4
CNTR 2=8
CNTR 2=9 *
CNTR 2=10 *
CNTR 2=9
TP3
TP2
TP4
COUNT 1=9 TAPE MODE LATCH
C3 .001UF 200V
C11 470 PF 500V
C13 .0068UF 80V
CNTR1 RST *
CNTR 2 RST *
TYPE MODE
COUNTER 1=9 *
PRINT MODE
TTY CLOCK1A *
TTY CLOCK GATE
TTY TAKE DATA SET
WRITE TAPE MODE
TAPE CLOCK B
REG 2 SHIFT
READ TAPE SHIFT
READ TAPE MODE
REG 1 SHIFT
TTY FEEDBACK
SDR
CNTR 2=(9+10) *
REG 2 SB *
J12
OUTSTANDING CHANGES
MATERIAL SPECIFICATION:
FINISH SPECIFICATION:
DO NOT SCALE THIS PRINT
dicom INDUSTRIES INCORPORATED
LOGIC DIAGRAM
SERIAL I/O CONTROL
344-90050
D
344-90050
B
SCALE
SHEET 2 OF 2
19

APPENDIX C MOTHERBOARD TO CONNECTOR TERMINATION TABLES (ONLINE/OFFLINE CONNECTORS)

ON-LINE INTERFACE TERMINAL POINTS

FROM	TO	WIRE COLOR	REMARKS
J27-A	J24-7	YEL	NDATØ-I
B	26	BRN	NDAT1-I
C	19	GRN	2-I
D	13	RED	3-I
E	6	BLU	4-I
F	25	ORN	5-I
H	18	VIO	6-I
J	12	YEL	NDAT7-I
K	5	GRY	NDATT-I
L	24	GRN	5v RTN
M	17	WHT	ODATØ-I
N	11	BLU	1-I
P	4	BLK	2-I
R	23	VIO	3-I
S	16	BRN	4-I
T	10	GRY	5-I
U	3	RED	6-I
V	22	WHT	ODAT7-I
W	15	ORN	ODATT-I
X	9	BLK	5v RTN
Y	2	YEL	5v RTN
Z	21	BRN	5v RTN
a	14	GRN	5v RTN
b	8	RED	OFLNC-I
c	1	BLU	L/OX1-I
d	J24-20	ORN	L/OX2-I
e	J25-7	YEL	L/OX3-I
f	26	BRN	INITLZ-I
h	19	GRN	OFLNS-I
j	13	RED	5v RTN
k	6	BLU	CMDT-I
m	25	ORN	DKSØC-I
n	18	VIO	DKS1C-I
p	12	YEL	WRITC-I
r	5	GRY	READC-I
s	24	GRN	HALTC-I
t	17	WHT	RWNDC-I
u	11	BLU	FLMKC-I
v	4	BLK	SRCH-I
w	23	VIO	5v RTN
x	16	BRN	STATT-I
y	10	GRY	RDYS-I
z	3	RED	FLAGS-I
AA	22	WHT	WIRTS-I
BB	15	ORN	READS-I
CC	9	BLK	L/OXS-I
DD	2	YEL	FLMKS-I
EE	21	BRN	WLKOS-I
FF	14	GRY	ERROS-I
J27-HH	8	RED	5v RTN
E2	1	BLU	SPARE
E2	J25-20	ORN	SPARE

TELEPRINTER TERMINAL POINTS
(Part of Option 01 or 06)

FROM	TO	WIRE COLOR	EIA (06)	TTY (01)
J28-A	J23-19	BRN	SIG. GND	PRINTER (+)
J28-B	J23-6	RED	RECV DATA	PRINTER (-)
J28-C	J23-18	ORN	GND CHASSIS	GND CHASSIS
J28-D	J23-5	YEL	TRANS DATA	KEYBOARD (+)
J28-E	J23-17	GRN		KEYBOARD (-)
J28-F	J23-4	BLU		GND CHASSIS
J28-H	J23-16	VIO		GND
J28-J	J23-13	GRY		GND
J28-K	J23-15	WHT	BAUDC-1	GND
E1	J23-2	BLK		BOMBTAIL SPLICE
E1	J23-14	BRN		BOMBTAIL SPLICE
E1	J23-1	RED		BOMBTAIL SPLICE

APPENDIX D WIRE TERMINATION TABLES AND MNEMONIC DEFINITIONS

This Appendix contains wire termination points for the Dicom 344, Rev. L. Definitions for each Mnemonic callout are also included.

DICOM 344 WIRE TERMINATION TABLE AND MNEMONIC DEFINITIONS

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
1	S J11	Z	J8	X	J5	12	Ø or 2	Load SOB1 or SOB2 into buffer
2	S J11	24	J8	3			Ø or 3	Load SOB1 or unload SOB2
3	S J11	21	J8	13			1	Unload SOB1 and load SOB2
4	S J11	22	J8	H			1 or 2	Unload SOB1 and load SOB2 or load SOB2
5	S J13	E	J8	9	J17	D	500KHZ A	Buffer shift clock
6	S J13	C	J8	F			500KHZ B	Buffer load clock
7	S J13	15	J8	K	J7	C	500KHZ A*	Trailing edge buffer shift clock
8	S J13	D	J7	25			CLK A	Buffer shift time
9	S J13	F	J7	24			CLK B	Buffer load time
10	S J11	X	J8	12			3	Unload SOB2 and load SOB1
11	S J11	M	J 7	16			9 RECBIT	Buffer bit 9 recirculate
12	S J8	C	J11	S			9 and 10 INH*	Buffer bits 9 and 10 recirculate
13	S J11	P	J7	S			10 RECBIT	Buffer bit 10 recirculate
14	S J11	13	J8	7	J7	9	ANYSOB*	SOB1 or SOB2 detected
15	S J3	16	J20	16			BOTLP 1	Voltage to BOT lamp deck 1
16	S J2	16	J19	16			BOTLP 2	Voltage to BOT lamp deck 2
17	S J1	16	J18	16			BOTLP 3	Voltage to BOT lamp deck 3
18	S J20	17	J3	T			BOTLP RET 1	Return from BOT lamp deck 1
19	S J19	17	J2	T			BOTLP RET 2	Return from BOT lamp deck 2

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
20	S J18	17	J1	T			BOTLP RET 3	Return from BOT lamp deck 3
21	S J20	F	J3	AA			BOTPHOTO CELL In 1	BOT detect from deck 1
22	S J19	F	J2	AA			BOTPHOTO CELL In 2	BOT detect from deck 2
23	S J18	F	J1	AA			BOTPHOTO CELL In 3	BOT detect from deck 3
24	S J5	AA	J6	15			BOT INH*	Delay at BOT
25	S J3	B	J20	Y			BRAKE 1	Deck 1 Brake
26	S J2	B	J19	Y			BRAKE 2	Deck 2 Brake
27	S J1	B	J18	Y			BRAKE 3	Deck 3 Brake
28	S J8	M	J11	14	J13	13	CHG CHAR*	Change first character to last character during buffer unload
29	S J11	Y	J10	16			CHG MODE	Change buffer state counter to load
30	S J20	11	J20	13	J3	F	CLIP 1	Cassette and loader in place deck 1
31	S J19	11	J19	13	J2	F	CLIP 2	Cassette and loader in place deck 2
32	S J18	11	J18	13	J1	F	CLIP 3	Cassette and loader in place deck 3
33	S J10	D	J12	3			CLOCK A	TTY clock or tape clock
34	S J12	N	J13	L			CNTR 1=8*	Counter 1 equals 8 clocks
35	S J12	AA	J9	S			CNTR 1= 4	Counter 1 is greater than 4
36	J9	6	J12	22	S J13	B	CNTR 1 RST*	Counter 1 reset
37	S J12	25					CNTR 2=ZERO*	Counter 2 = zero
38	S J12	24	J13	22			CNTR 2=8	Counter 2 equals 8 clocks
39	S J12	P	J10	9			CNTR 2=9	Counter 2 equals 9 clocks
40	S J12	23					CNTR 2=9*	Counter 2 = nine

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
41	S J12	19	J13	P			CNTR 2=(9+10)*	Counter 2 equals 9 or 10 clocks
42	S J12	X					CNTR 2=10*	Counter 2 equals 10 clock
43	S J10	14	J12	R			CNTR 2 RST*	Counter 2 reset
44	S J6	B	J10	B			CMDT	Command strobe gated
45	S J25	6	J6	M			CMDT-I	Command strobe
46	S		J11	19			COUNT 50	Allow change mode from off-line
47	S		J11	BB			CPUCOMM	Allow change mode on-line
48	S J7	2	J11	20			C/R*	ASCII carriage return dump the buffer
49	S J5	9	J11 J6	7 BB	J10	21	D0*	Deck Ø
50	S J5	K	J4	18	J3	18	D1*	Deck 1
51	S J5	J	J4	19	J2	18	D2*	Deck 2
52	S J5	8	J4	CC	J1	18	D3*	Deck 3
53	S J3	13	J20	9	J15	3	D1W	Deck 1 Write
54	S J2	13	J19	9	J15	S	D2W	Deck 2 Write
55	S J1	13	J18	9	J15	AA	D3W	Deck 3 Write
56	S J4	22	J17	F			D1LP*	Deck 1 lamp
57	S J4	24	J17	L			D2LP*	Deck 2 lamp
58	S J4	20	J17	R			D3LP*	Deck 3 lamp
59	S J14	17					DATA 1 FROM TAPE	Pulsed when a "one" is read from the tape
60	S J10	BB	J9	21			DATA TRANS STRB	Transfer register 1 to register 2
61	S J14	22	J14	20			DATA 0 FROM TAPE	Pulsed when a "zero" is read from tape
62	S J9	P	J7	3			DB 1	Data bit 1 to buffer
63	S J9	12	J7	R			DB 2	Data bit 2 to buffer
64	S J9	N	J7	22			DB 3	Data bit 3 to buffer
65	S J9	8	J7	U			DB 4	Data bit 4 to buffer
66	S J9	F	J7	CC			DB 5	Data bit 5 to buffer

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
67	S J9	7	J7	BB			DB6	Data bit 6 to buffer
68	S J9	D	J7	21			DB7	Data bit 7 to buffer
69	S J9	4	J7	F			DB8*	Data bit 8 to buffer
70	S J4 S J6	5 C	J5	F			DKOR*	Deck Select latch Ø=Ø
71	S J4 S J6	7 5	J5	10			DK1R*	Deck select latch 1=Ø
72	S J4 S J6	6 4	J5	L			DKOS*	Deck select latch Ø=1
73	S J4 S J6	4 3	J5	H			DK1S*	Deck select latch 1=1
74	S J25	25	J6	D			DKSOC-1	Deck select command bit Ø
75	S J25	18	J6	E			DKS1C-1	Deck select command bit 1
76	S J7	B	J8	Y			DELETE*	Delete all data in buffer
77	S J8	T	J11	18			DEL SS*	Delete single shot
78	S J1 S J3	J J	S J2	J	J6	24	DREADS*	Selected deck read status
79	S J1 S J3	R R	S J2	R	J6	20	DRDY*	Selected deck ready status
80	S J1 S J3	H H	S J2	H	J6 J5	27 B	DL/OXS*	Selected deck leader/ oxide status
81	S J1 S J3	M M	S J2	M	J6 J5	EE 4	DWLOS*	Selected deck write/ lock status
82	S J1 S J3	L L	S J2	L	J6	23	DWRITS*	Selected deck write status
83	S J1 S J3	22 22	S J2	22	J4 J5	W 25	DREW*	Selected deck in rewind
84	S J6	J	J25	10			DRDYS-1	Output ready status
85	S J20	12	J3	15			EJECT1*	Eject cassette deck 1
86	S J19	12	J2	15			EJECT2*	Eject cassette deck 2
87	S J18	12	J1	15			EJECT3*	Eject cassette deck 3

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
88	(Ref Grd)		J20	N			EJECT 2=1	Eject switch return
89	(Ref Grd)		J19	N			EJECT 2=2	Eject switch return
90	(Ref Grd)		J18	N			EJECT 2=3	Eject switch return
91	S J7	9	J25	14			ERROS-I	Output error status
92	S J13	J	J6	U			ERROR FLAG	Set error latch
93	S J7	K	J8	11			FIRST CHAR	Unload this character from buffer on the next cycle
94	S J5	19	J6	21			FLAGR*	Reset FLAG latch
95	S J12	T	J10	7			FLAG ENABLE	Enable data transfer flag
96	S J6	K	J25	3			FLAGS-I	Output data transfer FLAG status
97	S J25	11	J6	14			FLMKC-I	Input file gap write command
98	S J6	8	J25	2			FLMKS-I	Output read file gap detect status
99	S J13	Y	J6	L	J5	S	GAPT2	Record gap detect
100	S J5	6	J6	F			GAPT2P	Record gap detect pulse
101	S J5	CC	J4	13	J10	10	HALT*	Halt cycle
102	S J25	24	J6	16			HALTC-I	Input halt command
103	S J4	X	J17	14			HALTLP*	Halt lamp
104	S J5	Y	J1 J6	N 19	J2 J3	N N	HALTP	Halt Pulse
105	S J10	CC	J5 J12	2 B	J6 J8	6 20	HALTP1*	Halt pulse
106	S J10	EE	J4	T			HALTP*2	Off-line halt
107	S J1 S J3	23 23	S J2	23	J10	DD	HALTP* TACH	Halt pulse from tach-ometer
108	S J17	16	J4	U			HALTPB*	Halt push button

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
109	S J20	15	J3	S			HIPS-1*	Heads in place deck 1
110	S J19	15	J2	S			HIPS-2*	Heads in place deck 2
111	S J18	15	J1	S			HIPS-3*	Heads in place deck 3
112	S J20	14	J3	E			HOPS-1*	Heads out of place deck 1
113	S J19	14	J2	E			HOPS-2*	Heads out of place deck 2
114	S J18	14	J1	E			HOPS-3*	Heads out of place deck 3
115	S J5	Z	J6 J1	12 C	J2 J3	C C	1MOT	A deck is moving tape forward
116	S J4	8	J5	D			INIT	Initialize
117	S J4	S	J1 J2	P P	J3	P	INIT*	Initialize
118	S J25	26	J4	14			INITLZ-1	Initialize command
119	S J10	V	J9	5			INPUT DATA STRB	Strobe data into register 1
120	S J23	5	J4	B			KYBD(+)	Data from keyboard
121	S J4	10	J23	17			KYBD(-)	Return from keyboard
122	S J7	N	J8	J			LASTCHAR*	Last character loaded into buffer
123	S J11	V	J8	N			LOADSOB	A start of block is being loaded
124	S J11	W	J8	R			LOADSOB*	A start of block is being being loaded
125	S J11	R	J8	U			LOADSOB1	Load start of block 1
126	S J20	10	J3	17			LOP1*	Loader out of place deck 1
127	S J19	10	J2	17			LOP2*	Loader out of place deck 2
128	S J18	10	J1	17			LOP2*	Loader out of place deck 3

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
129	S J3	X	J20	V			LOWER HD SOL 1	Lower heads deck 1
130	S J2	X	J19	V			LOWER HD SOL 2	Lower heads deck 2
131	S J1	X	J18	V			LOWER HD SOL 3	Lower heads deck 3
132	S J3	2	J24	1			L/OX1-I	Leader*/ oxide deck 1 output status
133	S J2	2	J24	20			L/OX2-I	Leader* / oxide deck 2 output status
134	S J1	2	J25	7			L/OX3-I	Leader* / oxide deck 3 output status
135	S J6	DD	J25	9			L/OXS-I	Selected deck leader*/ oxide output
136	S J7	W	J9	BB			MB1	Buffer data bit 1 to register 2
137	S J7	V	J9	23			MB2	Buffer data bit 2 to register 2
138	S J7	AA	J9	24			MB3	Buffer data bit 3 to register 2
139	S J7	Z	J9	CC			MB4	Buffer data bit 4 to register 2.
140	S J7	4	J9	T			MB5	Buffer data bit 5 to register 2
141	S J7	17					MB5*	Not used
142	S J7	T	J9	2			MB6	Buffer data bit 6 to register 2
143	S J7	Y	J9	3			MB7	Buffer data bit 7 to register 2
144	S J7	X	J9	H			MB8	Buffer data bit 8 to register 2
145	S J7	M	J11	K			MB9	Buffer data bit 9 to mod character
146	S J7	L	J11	15			MB 10*	Buffer data bit 10 to change character

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
147	S J15	9	J14	BB			MPX 1	Read data preamplified
148	S J8	L	J11	16			MODCHAR*	Change first character code in buffer
149	S		J11	CC			MODEM	Modem count 50 equal state advance
150	S J8	V	J9	25			MOS DATA STROBE	Strobe MOS data into register 2
151	S J8	6	J10	Y			MOS DATA STROBE*	Clear send data so new data can be recognized
152	S J24	7	J9	13			NDAT0-I	Input data bit Ø
153	S J24	26	J9	R			NDAT1-I	Input data bit 1
154	S J24	19	J9	M			NDAT2-I	Input data bit 2
155	S J24	13	J9	9			NDAT3-I	Input data bit 3
156	S J24	6	J9	K			NDAT4-I	Input data bit 4
157	S J24	25	J9	11			NDAT5-I	Input data bit 5
158	S J24	18	J9	L			NDAT6-I	Input data bit 6
159	S J24	12	J9	10			NDAT7-I	Input data bit 7
160	S J10	24	J10 J5	2 24	J5	24	NDATT	Input data strobe load register 1
161	S J24	5	J10	25			NDATT-I	Input data strobe
162	S J8	5	J7	H			NEW DATA	New data is ready for buffer storage
163	S J9	W	J13	X			ODATØ	Output data bit Ø
164	S J9	Y	J24	17			ODATØ-I	Output data bit Ø
165	S J9	X	J24	11			ODAT1-I	Output data bit 1
166	S J9	Z	J24	4			ODAT2-I	Output data bit 2
167	S J9	14	J24	23			ODAT3-I	Output data bit 3

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
168	S J9	19	J24	16			ODAT4-I	Output data bit 4
169	S J9	20	J24	10			ODAT5-I	Output data bit 5
170	S J9	AA	J24	3			ODAT6-I	Output data bit 6
171	S J9	22	J24	22			ODAT7-I	Output data bit 7
172	S J24	15	J10	23			ODATT-I	Output data strobe
173	S J10	22	J5	21	J12	6	ODATT	Strobe data out
174	S J4	R	J6	N	J11	C	OFF-LINE	Unit in off-line mode
175	S J11	D	J10	12	J13	K	OFFLINE A	Unit in off-line mode
176	S J11	E	J12	K			OFFLINE*	Unit in off-line mode
177	S J10	C					OFFLINEA*	Unit in off-line mode
178	S J4	Y	J17	C			OFFLP*	Off-line lamp
179	S J17	B	J4	H	J6	17	OFFLINE PB*	Off-line push button
180	S J24	8	J4	15			OFLNC-I	Input off-line command
181	S J6	P	J25	19			OFLNS-I	Output off-line status
182	S J4	V	J5 J12	U 12	J10	M	ONLINE	Unit in on-line mode
183	S J4	17	J17	A			ONLP*	On-Line lamp
184	S J17	1	J4	F			ONLINE PB*	On-Line push button
185	S J10	4	J11	5			ONLINE WRITE	Unit in On-line write mode
186	S J12	14	J10	J	J9	V	OUTPUT STROBE	Informs unit output data was accepted (ODATT-I)
187	S J14	23					OUT BIPOLAR	Bipolar data output
188	S J17	E	J4	J			PB1*	Deck 1 push button
189	S J17	K	J4	L			PB2*	Deck 2 push button
190	S J17	P	J4	M			PB3*	Deck 3 push button

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
191	S J13	14	J10 J8	18 18	J11 J4	J E	POR*	Power on reset
192	S J11	L					POR PULSE	Power on reset pulse
193	(Ref Grd)		J23	19			PRINT(+)	Reference to printer
194	S J4	9	J23	6			PRINT(-)	Data output to printer
195	S J11	3	J12	F			PRINT MODE	Off-line device in print mode
196	S J14 S J14	U W	J13	24			READ DATA CLK*	Self clock from data
197	S J3	Z	J20	Z			RAISE HD SOL 1*	Raise heads deck 1
198	S J2	Z	J19	Z			RAISE HD SOL 2*	Raise heads deck 2
199	S J1	Z	J18	Z			RAISE HD SOL 3*	Raise heads deck 3
200	S J3	W	J20	W			RAISE LDR SOL 1*	Raise loader deck 1
201	S J2	W	J19	W			RAISE LDR SOL 2*	Raise loader deck 2
202	S J1	W	J18	W			RAISE LDR SOL 3*	Raise loader deck 3
203	S J11	B	J12	16			READ A	Read select latch A
204	S J11	11	J10	R			READ*	Unit in read mode
205	S J10	K					READ B	Read select latch B
206	S J5	17	J4 J6	K 22	J11	H	READ E	Read mode latch set
207	S J25	5	J6	S			READC-I	Input read command
208	S J6	CC	J25	15			READS-I	Output read status
209	S J17	Y	J4	N			READPB*	Read push button
210	S J4 S J6	2 H	J5 J2 J10	E 20 27	J3 J1	20 20	READP*	Initiate read pulse
211	S J4	21	J17	22			READLP*	Read lamp
212	S J5	18	J14	16			READRST	Read reset (reset bi-polar)
213	S		J14	T			READRSTA	Not used
214	S J5	R	J3 J16	19 H	J15	H	READSEL1*	Read select deck 1

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
215	S J5	7	J2 J16	19 11	J15	11	READSEL2*	Read select deck 2
216	S J5	M	J1 J16	19 21	J15	21	READSEL3*	Read select deck 3
217	S J14	21	J9	J	J13	12	READ TAPE DATA 0*	Tape read data Ø=* 1=
218	S J11	10	J12 J14	D X	J13	CC	READ TAPE MODE	Unit in read tape mode
219	S J11	6	J13	23			READ TAPE MODE*	Unit in read tape mode
220	S J13	4	J10	5			READ TAPE TAKE DATA SET*	A character has been read and assembled
221	S J13	5	J12	C			READ TAPE SHIFT	Generate register 1 shift in read mode
222	S J3	3	J20	T			READY LITE DRIVER 1	Ready lamp deck 1
223	S J2	3	J19	T			READY LITE DRIVER 2	Ready lamp deck 2
224	S J1	3	J18	T			READY LITE DRIVER 3	Ready lamp deck 3
225	S J22	6	J18 J17	U 11	J19 J20	U U	READY LITE 10V	Power to ready lamps
226	S J10	N	J9	B			REG1RST*	Reset register 1
227	S J12	17	J9	C			REG1SHIFT	Load serial data into register 1
228	S J9	18	J13	BB			REG2BIT1*	Serial data Ø to write F/F
229	S J9	17	J12	18			REG2-SB*	Serial data to TTY
230	S J12	20	J9	15			REG2SHIFT	Shift register 2
231	S J10	S					REG2RST	Not used
232	S J10	15	J9	16			REG2RST*	Reset register 2
233	S J8	P	J7	23			REC	Recirculate data in buffer
234	S J4 S J6	16 11	J2 J1	D D	J3	D	RWNDP*	Initiate rewind cycle

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
235	S J3	Y	J20	X			REWINDSOL1 *	RewindDeck deck 1
236	S J2	Y	J19	X			REWINDSOL2 *	Rewind deck 2
237	S J1	Y	J18	X			REWINDSOL3 *	Rewind deck 3
238	S J25	17	J6	T			RWNDC-1	Input rewind command
239	S J4	BB	J17	W			REWLP*	Rewind lamp
240	S J17	U	J4	P			REWPB*	Rewind push button
241	S J4	C	J9	U	J12	W	SDR*	Serial data received from off-line device
242	S J10	T	J12	U			SEND DATA SET*	Set send data F/F
243	S J10	AA					SEND DATA RST	Not Used
244	S J10	X	J12	13			SEND DATA RST*	Reset send data
245	S J10	W	J8	10			SEND DATA	Unit ready for more data
246	S J10	8	J6	Y			SET RDY FLAG*	Set data request FLAG (FLAGS)
247	S J7	P	J8	D			SOB1*	Start of block 1 decoded in buffer
248	S J7	J	J8	4			SOB2*	Start of block 2 decoded in buffer
249	S J11	25	J7	10			SOB1 IN*	Change mode load SOB1 in buffer
250	S J11	23	J7	E			SOB2 IN*	Change mode load SOB2 in buffer
251	S J6	13	J5	11	J11	12	SRCH*	Unit in search mode
252	S J25	4	J6	10			SRCHC-1	Input search command
253	S J8	B	J10	3			STOP/ LOAD*	Stop recirculate buffer and load new data
254	S J8	2	J10	H	J11	U	STOP/ LOAD* A*	Stop recirculate buffer and load new data

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
255	S J8	Z					STOP/REC*	Stop re-circulating buffer data
256	S J8	14	J11	AA			STATE ADV*	Advance buffer state counter to Ø or 2
257	S J25	16	J6	V			STATT-I	Input status strobe
258	S J11	N	J10	L			(BURST + OFFLINE)*	Burst (on-line buffer) or off-line
259	S J11	T	J8	S			BURST + OFFLINE	Burst or off-line
260	S		J11	17			BURST*	On-line buffer mode
261	S J13	V	J5	T			T I TIME*	Character gap detected
262	S J3	U	J20	H			TACH-A1	Normally closed tach-ometer wiper: deck 1
263	S J2	U	J19	H			TACH-A2	Normally closed tach-ometer wiper: deck 2
264	S J1	U	J18	H			TACH-A3	Normally closed tach-ometer wiper: deck 3
265	S J3	V	J20	J			TACH-B1	Normally open tach-ometer wiper: deck 1
266	S J2	V	J19	J			TACH-B2	Normally open tach-ometer wiper: deck 2
267	S J1	V	J18	J			TACH-B3	Normally open tach-ometer wiper: deck 3
268	Ref Grd		J20	K			TACH-C1	Center tap tachometer wiper:deck 1
269	Ref Grd		J19	K			TACH-C2	Center tap tachometer wiper:deck 2
270	Ref Grd		J18	K			TACH-C3	Center tap tachometer wiper:deck 3

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
271	S J10	17	J8	E			TAKE DATA	Synchronize transfer of register 1 data to register 2
272	S J10	F	J13	H			TAKE DATA ERROR*	Data not taken from register 2 prior to new data ready for transfer
273	S J13	2					TAPE CLK	Not used
274	S J13	W	J10	13			TAPE CLK A*	Complement write flip/flop
275	S J13	R	J12	BB			TAPE CLK B	Write data bit on tape
276	S J12	15	J13	9			TAPE CLK GATE	Allow tape clocks in tape write mode
277	S J12	L	J13	21	J8	19	TAPE CLK GATE*	Allow tape clocks in tape write mode
278	S J12	S					TTY CLK GATE	Allow TTY Clocks in TTY read or write mode
279	S J12	5	J8	W			INH STATE ADV*	Block state advance until present state completed
280	S J12	V	J10	U			TTY CLOCK A*	TTY clock buffered
281	S J12	Y	J4	D			TTY FD BK	Data to TTY printer
282	S J12	21	J10	6			TTY TAKE DATA SET*	TTY data assembled
283	S J11	2	J12	J	J9	E	TYPE MODE	Enable TTY keyboard
284	S J5	20	J13	N	J6	W	UP TO SPD	Transport data valid
285	S J6	2	J5	V			WFM*	Unit in write file gap mode
286	S J20	8	J3	11			WLOSW (NO) 1	Write lock/out switch normally open: deck 1

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
287	S J19	8	J2	11			WLOSW (NO) 2	Write lock/ out switch normally open: deck2
288	S J18	8	J1	11			WLOSW (NO) 3	Write lock/ out switch normally open: deck 3
289	S J6	26	J25	21			WLOKS-I	Output write lock/ out status
290	S J5	W	J4 J6	Z Z	J11	9	WRITE	Unit in write mode
291	S J11	8					WRITE A	Unit in write mode
292	S J11	F	J10	P	J12	4	WRITE *	Unit in write mode
293	S J13	19	J15	4			WRITE 0	Write a "zero" bit
294	S J13	25	J15	2			WRITE 1	Write a "one" bit
295	S J4	25	J17	18			WRITLP*	Write lamp
296	S J13	8	J12	2			WRIT CMD	Write command
297	S J25	12	J6	R			WRITC-I	Input write command
298	S J6	25	J25	22			WRITS-I	Output write status
299	S J4	3	J5	C	J6	7	WRITP*	Initiate write pulse
300	S J17	20	J4	12			WRITPB*	Offline write push button
301	S J12	H	J5	BB			WRITR*	Reset the write mode
302	S J11	4	J12	CC	J13	10	WRITE TAPE MODE	Unit in write on tape mode
303	J17	2			(Ref Grd)			
304	S J6	X	J1 J3	21 21	J2	21	WFMP+ WRIT P	Initiate write or write file gap pulse

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
305	S J22	7	J18	18	J18	19	POWER FOR	
			J18	21	J18	22	DECK	
			J19	19	J19	20	SOLENOIDS	
			J19	22	J20	18		
			J20	20	J20	21	+28V	
			J18	20	J19	18		
			J19	21	J20	19		
			J20	22				
306	S J18	A	to Feedthrough E3				HD A30 RED1	Deck 1
307	S J18	1	to Feedthrough E2				HD A31 BLK1	read/write
308	S J18	B	J18	2	to Feedthrough		SHIELD HD1	head cable
309	S J19	A	to Feedthrough E4				HD A20 RED1	Deck 2
310	S J19	1	to Feedthrough E5				HD A21 BLK1	read/write
311	S J19	B	J19	2	to Feedthrough E6		SHIELD HD1	head cable
312	S J20	A			to Feedthrough E7		HD A10 RED1	Deck 1 read/write
313	S J20	1			to Feedthrough E8		HD A11 BLK1	head cable
314	S J20	B	J20	2	to Feedthrough E9		SHIELD HD1	
315	S J15	BB	J15	X	to Feedthrough E18		HD A30 RED1	Read data in deck 3
316	S J15	Y	J15	W	to Feedthrough E16		HD A31 BLK1	
317	Grd Plane		E17				SHIELD HD1	
318	J15	M	J15	13	to Feedthrough E13		HD A20 RED1	Read data in deck 2
319	S J15	L	J15	P	to Feedthrough E15		HD A21 BLK1	
320	Grd Plane				to Feedthrough E14		SHIELD HD1	
321	S J15	E	J15	C	to Feedthrough E12		HD A10 RED1	Read data in deck 1
322	S J15	D	J15	B	to Feedthrough E10		HD A11 BLK1	
323	Grd Plane				to Feedthrough E11		SHIELD HD1	
324	S J18	3	J16	Y	J16	W	DIPHASE HD 31	Skew Verification test slot deck 3
325	S J18	C	J16	BB	J16	X	DIPHASE HD 30	
326	S J22	8	J1	BB	J1	24	SOL GND	
			J2	24	J3	24		
			J2	BB	J3	BB		
327	S J22	5	J4	AA	J4	23	LAMP GND	
			J1	25	J2	CC		
			J3	CC	J3	25		
			J1	CC	J2	25		

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
	J18	D	J19	D	J20	D		
328	J24	21	J20	M	J22	A	5V GRD	
	J24	9	J17	2	J24	2		
	J24	14	J25	8	J20	L		
	J20	P	J20	R	J20	S		
	J22	B	J22	1	J22	2		
	J19	M	J19	P	J19	R		
	J18	L	J18	M	J18	P		
	J18	S	J18	N	J19	N		
	J20	N	J16	4	J17	D		
		E11		E14		E17		
	J22	C	J22	E	J16	2		
	J18	E	J25	23	J19	E		
	J20	E	J24	24	J25	13		
	J19	L	J19	S	J18	R		
	Pins 28 and FF of Cards J1 to J6							
329	J19	3	J16	L	J16	P	DIPHASE HD 21	Skew verification deck 2
330	J19	C	J16	M	J16	13	DIPHASE HD 20	
331	J20	3	J16	D	J16	B	DIPHASE HD 11	Skew verification deck 1
332	J20	C	J16	E	J16	C	DIPHASE HD 10	
333	J18	4	to Feedthrough E21				ERASE 3	Not used
334	S J19	4	to Feedthrough E20				ERASE 2	Not used
335	S J20	4	to Feedthrough E19				ERASE 1	Not used
336	All card J1 to J16 Pins 1 and A							
	S J22	9	S J22	10	J18	7		+5V
	S J22	L	J19	7	J20	7		
	S J22	K	J22	D				
337	S J22	4	J1	26	J1	DD		
	J2	DD	J3	26	J3	DD		+12V
	J4	DD	J7	26	J7	DD		
	J14	DD	J15	26	J15	DD		
	J16	DD	J2	26	J4	26		
			J14	26	J16	26		
338	S J22	3	J1	27	J1	EE		
	J2	EE	J3	27	J3	EE		-12V
	J4	EE	J7	27	J7	EE		
	J14	EE	J15	27	J15	EE		
	J16	EE	J2	27	J4	27		
			J14	27	J16	27		
339	S J18	4	J1	4			GOP3	Guillotine latch out of place deck 3
340	S J19	4	J2	4			GOP2	Guillotine latch out of place deck 2
341	S 20	4	J3	4			GOP1	Guillotine latch out of place deck 3

SEQUENCE	SOURCE POS	SOURCE PIN	TO POS	TO PIN	TO POS	TO PIN	MNEMONIC	MNEMONIC DEFINITION
342	S J23	15	J12	27			BAUDC-I	Select one of two serial clocks
343	S J23	3	J12	EE			BAUDD-I	Select one of four serial clocks
344	S J23	4	J23	18			GND	

APPENDIX E PARTS LIST

This Appendix contains descriptions, part numbers and quantities for the Dicom 344 unit with one Tape Transport Module

DICOM 344 PARTS LIST APPENDIX E

ITEM	DESCRIPTION	PART NUMBER	QTY
1	MOS Buffer Assy Bd	344-90020	1
2	TTY Board	344-90021	1
3	On-Line Sync Control Bd	344-90022	1
4	Mode & State Decode	344-90023	1
5	MOS Buffer Control Board	344-90024	1
6	Welded Wiring Board (Mother)	344-90025	1
7	Tape Data Control Board	344-90026	1
8	Shift Register 1 & 2 Board	344-90027	1
9	R/W Electronics Board	344-90028	1
10	Deck Control Board	344-90030	3
11	Off-Line Cntrl Lmp Drvr Bd	344-90031	1
12	Motion Control Board	344-90032	1
13	Reproduce Board	344-90033	1
14	Regulator Board	344-90035	1
15	Main Mounting Board	344-90036	1
16	Computer Control Board	344-90037	1
17	Extender Card (Power Supply)	344-40042	1
18	Capacitor 47pf 500v	DM15-470J	3
19	Capacitor 470pf 500v	DM15-471J	4
20	Capacitor 120pf 500v	DM15-121J	4
21	Capacitor 220pf 500v	DM15-221J	2
22	Capacitor 240pf 500v	DM15-241J	3
23	Capacitor 390pf 500v	DM15-391J	1
24	Capacitor 500pf 500v	DM15-501J	6
25	Capacitor	TE1148	1
26	Capacitor 10µf 15v	TE1155	19
27	Capacitor	TE1156	1
28	Capacitor 20µf	TE1157	9
29	Capacitor	TE1158	1
30	Capacitor	TE1160	4
31	Capacitor	TE1163	2
32	Capacitor	TE1200	3
33	Capacitor 2.2µf 20v	150D225X9020A2	9
34	Capacitor	150D226X0015B2	4
35	Capacitor	150D227X9010S2	AR

36	Capacitor .001µf 200v	192P10292	18
37	Capacitor	192P1039R8	7
38	Capacitor .1µf 80v	192P2229R8	9
39	Capacitor .0022µf 80v	192P2229R8	7
40	Capacitor	192P2729R8	1
41	Capacitor .056 uf 80V	192P5639R8	1
42	Capacitor .33µf 80v	192P3349R8	1
43	Capacitor .0068 µf 80v	192P6829R8	2
44	Capacitor .068µf 80v	192P6839R8	2
45	Capacitor	36D552 G025AB2A	3
46	Capacitor	36D602 G050BB2A	1
47	Capacitor .033µf 80v	192P3339R8	1
48	Capacitor .1µf 10v	UK10-104	41
49	Capacitor	150D335X9015AZ	1
50	Capacitor .1µf 30v	DA-104	4
51	Connector (Deck Lite) (Amphenol)	225-22221-103	5
52	Connector PC Card (Amphenol)	225-22821-103	16
53	Connector Pin P/S (Amphenol)	225-21021-103	2
54	Diode	SC3S05E	4
55	Diode (Rectifier)	1N4005	6
56	Diode	1N914	62
57	Diode	1N34	2
58	Diode	1N4740	1
59	Diode	1N5234A	1
60	Diode	MCR407-1	1
61	Fuse 2A	361002	1
62	Fuse Clips, Earless	121002	2
63	Diode	3S1E	2
64	Integrated Circuit	CH1032	2
65	Integrated Circuit	MC833P	1
66	Integrated Circuit	MC836P	64
67	Integrated Circuit	MC845P	3
68	Integrated Circuit	MC846P	83
69	Integrated Circuit	MC851P	1
70	Integrated Circuit	MC852P	8
71	Integrated Circuit	MC853P	13
72	Integrated Circuit	MC858P	16

73	Integrated Circuit	MC862	23
74	Integrated Circuit	MM506	5
75	Integrated Circuit	9601	8
76	Integrated Circuit	USB770939X(709C)	5
77	Integrated Circuit	USR7723393(723C)	3
78	Integrated Circuit	MC830P	10
79	Mounting Pad	RC-T05-140-8A	5
80	Post Mod II	86090-2	78
81	Resistor 100Ω	RC07GF101J	9
82	Resistor 1K	RC07GF102J	11
83	Resistor 10K	RC07GF103J	18
84	Resistor	RC07GF104J	9
85	Resistor	RC07GF152J	14
86	Resistor	RC07GF154J	7
87	Resistor	RC07GF163J	1
88	Resistor	RC07GF182J	19
89	Resistor 2.7Ω	RC07GF2R7J	11
90	Resistor 2.2K	RC07GF222J	18
91	Resistor	RC07GF224J	57
92	Resistor	RC07GF271J	1
93	Resistor	RC07GF272J	2
94	Resistor	RC07GF273J	3
95	Resistor	RC07GF274J	2
96	Resistor	RC07GF333J	1
97	Resistor	RC07GF362J	1
98	Resistor	RC07GF392J	3
99	Resistor	RC07GF432J	8
100	Resistor	RC07GF470J	9
101	Resistor 470Ω	RC07GF471J	4
102	Resistor 4.7K	RC07GF472J	5
103	Resistor	RC07GF473J	4
104	Resistor	RC07GF511J	17
105	Resistor 5.1K	RC07GF512J	28
106	Resistor	RC07GF620J	7
107	Resistor 6.8K	RC07GF682J	12
108	Resistor	RC07GF1R0J	5
109	Resistor	RC32GF102J	1

110	Resistor Var 100k	3009Y-1-104	3
111	Resistor Var 1K	3009Y-1-102	8
112	Resistor Var 2K	3009Y-1-202	1
113	Resistor Var 5k	3009Y-1-502	5
114	Resistor Var 50K	3009Y-1-503	1
115	Resistor Var 10K	3009Y-103	1
116	Resistor	RC20GF202J	1
117	Resistor	RC07GF270J	3
118	Resistor	RC07GF331J	3
119	Resistor	RC07GF183J	1
120	Resistor	RC07GF474J	3
121	Resistor	RC07GF503J	AR
122	Resistor	RC07GF680J	3
123	Resistor	RC07GF683J	1
124	Resistor	RC07GF823J	1
125	Resistor	RC07GF151J	3
126	Resistor	RC20GF680J	3
127	Resistor 120Ω	RC20GF121J	10
128	Resistor	RC20GF271J	1
129	SCR FLHD Phillips	4-40 X 1/4"	4
130	Spacer, Hex	4-40 X .625(8805)	4
131	Transistor	2N4923	15
132	Transistor	2N1303	3
133	Transistor	D13T1	5
134	Transistor	2N3904	4
135	Transistor	2N3906	16
136	Transistor	2N3641	1
137	Transistor	2N4921	1
138	Front Panel	344-10011	1
139	Subpanel	344-10012	1
140	Subpanel	344-10013	1
141	Name plate strip	344-10014	1
142	Rear Panel	344-10019	1
143	Dust Cover Side	344-10034	2
144	Dust Cover Top/Bottom	344-10035	2
145	Filler Plate	344-10037	2
146	Flange	344-10039	1

147	Brkt. Left Side Mounting	344-10040	1
148	Brkt. Right Side Mounting	344-10041	1
149	Read Deck Mtg.	344-10042	1
150	Guide Support Power Supply	344-10043	1
151	Guide Rail	344-10044	1
152	M/F NC-403K Heat Sink	344-10048	1
153	Power Supply Chassis	344-10049	1
154	Power Supply Cover	344-10051	1
155	Front Plate	344-10052	1
156	Cover Support, Lower	344-10054	1
157	Housing Fan	344-10056	1
158	Cover Support, Upper	344-10063	2
159	Plug Mtg. Brkt.	344-10066	1
160	Power Supply Rail	344-10067	1
161	Rail Gard Guide	344-10069	1
162	Rail Card Guide	344-10070	1
163	Rail Card Guide	344-10071	1
164	Rail Card Guide	344-10072	1
165	Support	344-10074	1
166	Trim Strip Front	344-20039	1
167	Trim Strip Top/Bottom	344-20043	2
168	Spacer	344-20044	4
169	Align Pin	344-20075	2
170	Foam Top Cover	344-20076	1
171	Adapter Plate	344-60052	1
172	Buffer Spring Assy	344-70009	1
173	Capstan/Clutch Assy	344-70019	1
174	Power Supply Module	344-70028	1
175	Tape Transport Module	344-70036	3
176	Transformer, AC Step Down	344-00507	1
177	ID Plate #1	344-80016	1
178	ID Plate #2	344-80017	1
179	ID Plate #3	344-80018	1
180	Side Frame W/Handles	344-80049	2
181	Filter, Fan	344-80061	1
182	M/F 2534 Smith Bushing Nylon	344-80076	1
183	Transformer, Power Supply	344-80088	1

184	M/F XMRE-50-1000 Winchester Rcp Mtg.	344-80096	1
185	Card Guide	344-80098	32
186	Label, Dicom	344-800100	2
187	M/F 03-06-2043 Molex P/S Plug	344-800112	1
188	Spacer	344-800117	2
189	Washer	344-800118	2
190	P/S Insulator	344-800146	1
191	M/F 2500 Pamotor Fan	344-800157	1
192	Bushing	2534	1
193	Flat Cable-12 Cond.	SF-1226-64C-10STD	1'
194	Flat Cable-26 Cond.	SF-2626-64C-10STD	3'
195	Cable Clamp	BU-1/4-6B	1
196	Capacitor .01mf 80v	192P1039R8	1
197	Capacitor 2.2µf 20v	150D225X9020A2	1
198	Conn. Recpt., Molex	03-06-1043	6
199	Conn. Recpt., Molex	03-06-2043	10
200	Conn. recpt. 9 Pin, Winchester	XAC9SF	1
201	Conn. Recpt. 50 Pin, Winchester	XAC50SF	1
202	Conn. 26 Pin, 3M	3399-1	3
203	Conn. Splice, Amp	36964	2
204	Conn. Recpt., Elco	01-3102-120-001	3
205	Conn. Recpt. AC, Switchcraft	AC3G	1
206	Conn. 22 Pin, Amphenol	225-22221-101	1
207	Contact Pin Recpt., Molex	02-06-1101-TL	18
208	Contact Pin Plug, Molex	02-06-2101-TL	24
209	Contact Socket, Winchester (I/O)	100-2024S	58
210	Contact Pin, Winchester (I/O)	100-2024P	AR
211	Fuse 3AG3A Slo-Blow	313003	2
212	Fuse Holder, 3AG	342004	2
213	Neoprene foam w/Mactac 9546 Adhsve	.18 thk X5Wx4Lg	1
214	Grommet	2172	1
215	Insulator, Mica	495320	1
216	Lug	1416-4	3
217	Shroud, Cassette Loader	N1	3
218	Screw, Shroud	N6	6
219	Speed Nut	C11351-632-24D	12
220	Hex Nut	#4	4

221	Hex Nut	#6	4
222	Resistor 1/4Ω	RH-5-.250 r	1
223	Resistor 10Ω	RH-5-10Ω	1
224	Relay, Time Delay (120 sec.)	CUA-42-70120	1
225	Switch, Online	690910-11D1	1
226	Switch, Offline	690910-11D2	1
227	Switch, Rewind	690910-11D3	1
228	Switch, Read	690910-11D4	1
229	Switch, Write	690910-11D5	1
230	Switch, Halt	690910-11D6	1
231	Switch, #1	690910-11D7	1
232	Switch #2	690910-11D8	1
233	Switch #3	690910-11D9	1
234	Switch, Power	690910-11D10	1
235	Spacer 4-40	SR5064	2
236	Standoff 8-324.250	3923-19	2
237	Standoff 4-40 X 9/16	8832	3
238	Standoff 4-40 X 3/8	8835	1
239	Screw Oval Head, Nickel Plate	4-40X1/4 Phillips	8
240	Screw Oval Hd., Nickel Plate	6-32X1/4 Phillips	18
241	Screw Oval Hd., Nickel Plate	6-32X1/2 Phillips	12
242	Screw Captive, Power Supply	2375A	2
243	Screw Longlock, TTM Mounting	LP22D62P12	6
244	Screw Fillister Hd	4-40 X 3/4 Ph.	4
245	SCR P/H Phillips	2-56 X 1/4	4
246	SCR P/H Phillips	4-40 X 1/4	14
247	SCR P/H Phillips	4-40 X 3/8	3
248	SCR P/H Phillips	4-40 X 1/2	4
249	SCR P/H Phillips	4-40 X 5/8	3
250	Screw P/H Phillips	4-40 X 3/4	4
251	Screw P/H Phillips	6-32 X 5/16	6
252	Screw P/H Phillips	6-32 X 3/8	34
253	Screw P/H Phillips	6-32 X 1/2	4
254	Screw P/H Phillips	6-32 X 5/8	4
255	Scr P/H Phillips	4-40 X 3/16	4
256	Scr P/H Phillips	4-40 X 1/4	22
257	Scr P/H Phillips	4-40 X 3/8	4

258	Scr P/H Phillips	6-32 X 5/16	16
259	Scr P/H Phillips	6-32 X 1/2	1
260	Flat Washer	1/4X5/32X1/32	6
261	Washer, Flat #2	#2	AR
262	Washer, Flat #4	#4	26
263	Washer, Flat #6	#6	19
264	Washer Split Lock	#2	4
265	Washer Split Lock	#4	41
266	Washer Split Lock	#6	51
267	Transistor	2N4918	1
268	Transistor	2N4921	2
269	Transistor	2N3055	1
270	Link Retainer (Rewind)	344-10003	1
271	Link (Head Actuator)	344-10006	1
272	Structure		
273	Motor Housing		
274	Link (Rewind)	344-10064	1
275	Bracket (Rewind Solenoid)		
276	GOP Switch Mounting Bracket	344-10084	
277	Head-in-Place Switch Mtg. Bracket	344-10083	
278	Head-Out-of-Place Switch Mtg. Brkt.	344-10082	
279	Pulley (Main Drive)	344-20012	
280	Mainplate		
281	Washer (Latch Spring Head-In)	344-20027	
282	Pin Pivot (Head Actuator)		
283	Block (Connector Brd Mtg.)	344-20054	2
284	Spacer (AC Connector)	344-20065	1
285	Post (Photosensor)		
286	Block (Switch Mtg	344-20087	1
	Used only on S/N 600 and below)		
287	PC Board Assembly (Photosensor)	344-50044	1
288	Switch, Cherry (WLO,CIP,GOP,HOP,HIP)	344-60004-01	5
		(E61-10-H)	
289	BOT/EOT Lamp Assembly	344-60016	1
290	Motor Housing Assembly		
291	Connector Board Assembly, TTM	344-60031	1
292	Arm Assembly (Head Mounting)		

293	Forward Tape Guide Assembly		
294	Yoke Assembly (Pinch Roller)		
295	Recording Head Assembly	344-60054	1
296	Pulley Assembly (Forward/Rewind)	344-60056	1
297	Head Arm Actuator Assy	344-60058	1
298	Spring (Head Latch)	344-80002	1
299	Head Latch Assy (Guillotine)	344-60060	1
299A	Block (Head Latch)		
299B	Latch (Head Actuator)		
300	Loader Latch Assy	344-60061	1
300A	Latch (Loader)		
300B	Rod (Latch)		
301	Lampholder Shroud Assy (Ready)	344-60062	1
302	Solenoid Plunger Assy (Head-Out)	344-60063	1
303	Solenoid Plunger Assy (Head-In)	344-60064	1
304	Pivot Mount Assy (Loader Linkage)	344-60065	1
305	Vibration Damper Assy	344-60066	1
306	Connector Board Assy	344-60067	1
307	Actuator Assy (CIP Switch)	344-60068	1
308	Actuator Assy (WLO Switch)	344-60069	1
309	Lens (Ready Light)	344-80014	1
310	Spring Tortion Head Arm	344-80051	1
311	Spring (Rewind)	344-80091	1
312	Spring (Rewind Return)	344-80092	1
313	Pinch Roller Assy	344-80105	
314	Lever, Cassette Eject (Modified)	344-80129	1
315	Washer, Locking (Clear)	344-80140	2
316	Washer, Spacing (Red)	344-80142	2
317	Washer, Spacing (White)	344-80143	2
318	Spacer(Rewind Wheel)	344-80144	1
319	Washer Thrust (Pinch Roller)	344-80140	2
320	Pad (Pressure)	344-80150	1
321	Spacer (Arm Retainer)	344-80151	1
322	Spring (Head Actuator)	344-80153	1
323	Supply Reel	528-10166	1
324	Spring (Forward Take-Up)	344-80155	1
325	Block, Head Arm Holddown	344-80158	

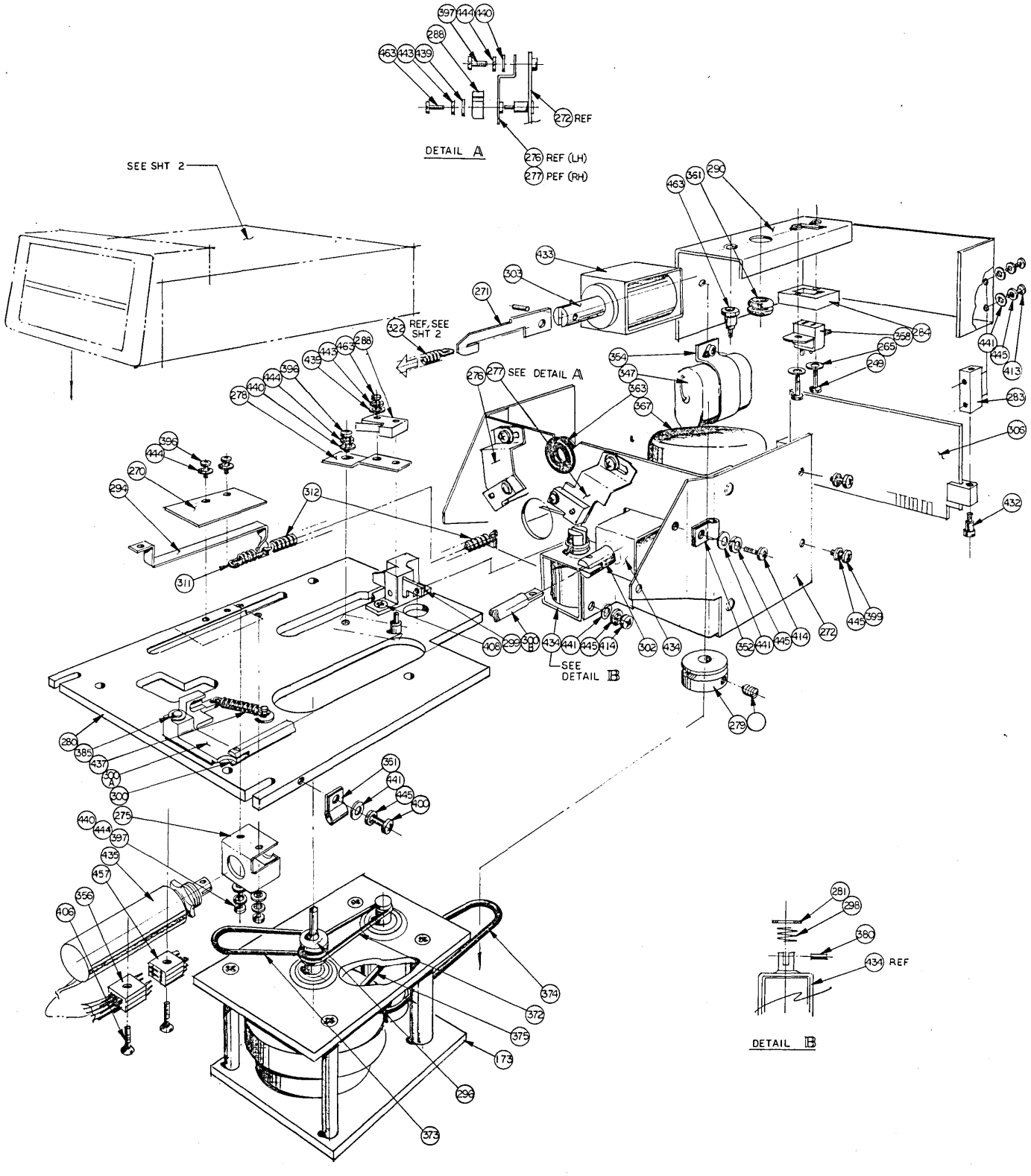
326	Cover (Loader)	344-N3	1
327	Spring (Loader Tension)	344-N10	1
328	Wheel (Forward Take-Up)	344-N11	1
329	Link (Forward Take-Up)	344-N12	1
330	Tachometer Contact Assy	344-N15	1
331	Switch (Loader Position)	344-N24	1
332	Switch (Loader Eject)	344-N29	1
333	Wheel (Rewind Drive)	344-N51	1
334	Tab (Cassette Locating)	344-N62	1
335	Linkage, Main (Loader)	344-N63 Requires	1
		N8	
336	Linkage, Idler (Loader)	344-N64 Requires	
		N8	
337	Lever (Cassette Positioning)	344-N66	1
338	Spring (Lever Tension)	344-N67	1
339	Crossbar (Loader Tension)		
340	Retainer Cap, Turnable	462-70485	
341	Spring, Turnable	492-50698	
342	Spring, Roller Pressure	492-40268	
343	Reel Catch, Cassette Hub (Rewind)	528-20129	
344	Forward Take-Up Reel	528-10185	
345	Drive Idler, Forward	528-70186	
346	Pulley Assy, Rewind	528-80305	
347	Capacitor, Mylar 2.0 MFD 10% 400VDC	2MFW4155K	1
348	Clamp	5300-2	1
349	Clamp	5300-15	2
350	Clamp	5300-18	1
351	Clamp	BU-1/8-6B	1
352	Clamp	BU-3/16-6B	1
353	Clamp	BU-1/2-6B	1
354	Clamp, Motor Capacitor	344-10030	1
355	Clamp, Cable EOT/BOT	5300-13	1
356	Connector (Clutch, EOT/BOT, RWD, SOL)	JF2P	3
357	Connector (Clutch, EOT/BOT, RWD, SOL)	JF2S	3
358	Connector, Motor (AC Power)	01-1102-111-004-000	1
359	Diode	1N4005	5
360	Diode	1N5363A	1

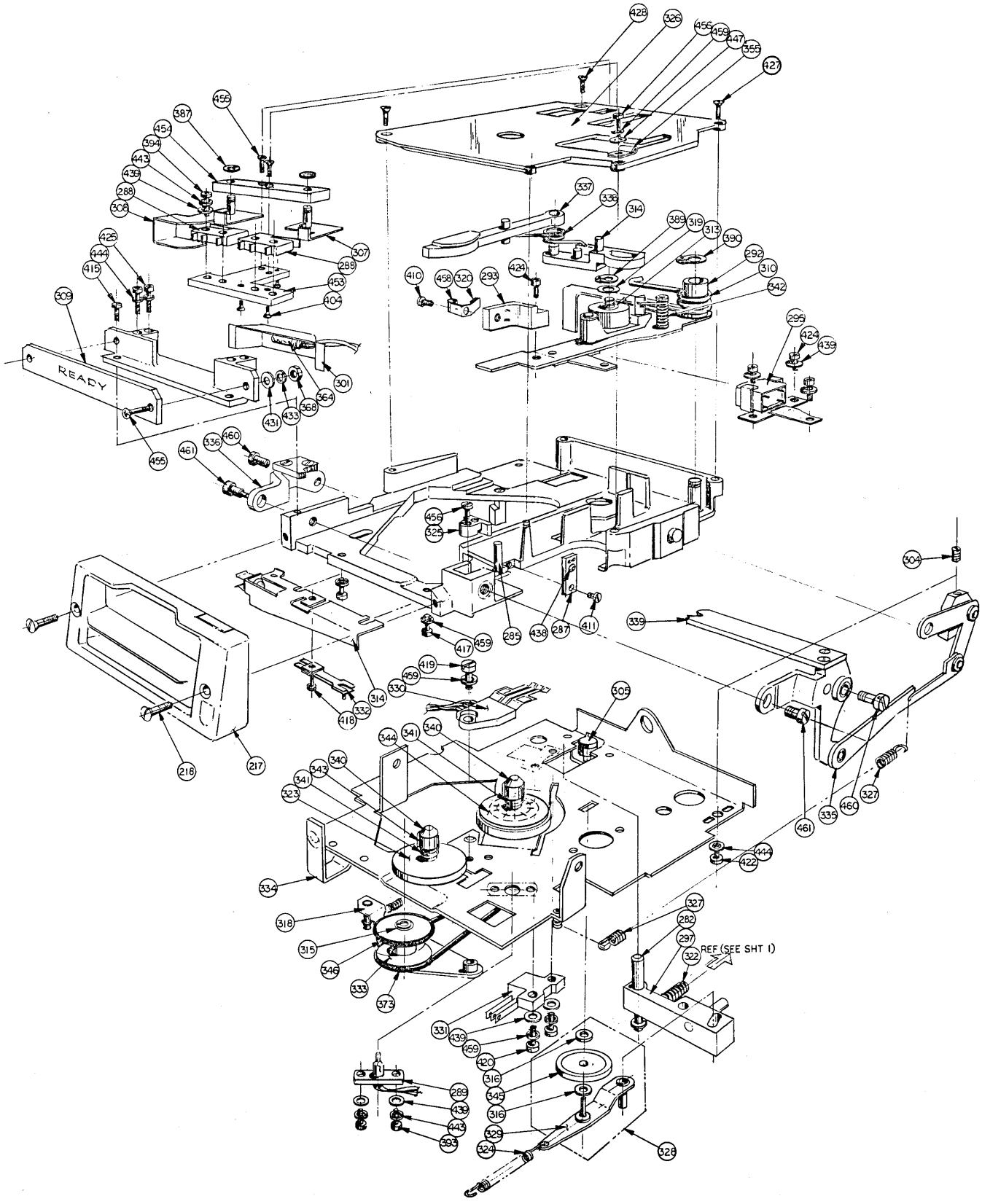
361	Grommet	GOB-215	1
362	Grommet	2101	1
363	Grommet	2177	2
364	Lamp	373	1
365	Lubricant, Lubriplate	23-02	AR
366	Lug, Solder	1488-4	1
367	Motor (Drive)	186A229	1
368	Nut, Hex 2-56		2
369	Nut, Hex 6-32		2
370	Nut, Hex 15/32-32		1
371	Nut, Hex (Metric) M3,0		
372	O-Ring, Rewind Turnaround	2-028	1
373	O-Ring, Rewind Pulley Drive	2-033	1
374	O-Ring, Motor Drive	2-226	1
375	O-Ring, Jackshaft Drive	2-230	1
376	Pin, Dowel 1/8 X 1/2		1
377	Pin, Spring 1/16 X 3/16		1
378	Pin, Spring 5/64 X 5/16		1
379	Pin, Spring 3/32 X 1/4		1
380	Pin, Spring 3/32 X 1/2		1
381	Pin, Spring 1/8 X 3/8		2
382	Pin, Spring 1/8 X 1/2		1
383	Retaining Ring	5100-25	1
384	Retaining Ring	5103-18	1
385	Retaining Ring	X-5131-18	1
386	Retaining Ring	5133-9	3
387	Retaining Ring	5133-12	3
388	Retaining Ring	5133-25-C	1
389	Retaining Ring	5555-12	1
390	Retaining Ring	5555-15	1
391	Retaining Ring	5555-23	1
392	Retaining Ring	5555-62	1
393	Screw, Phillips Pan Head 2-56X1/4		3
394	Screw, Phillips Pan Head 2-56X3/8		4
395	Screw, Phillips Pan Head 2-56X1/2		4
396	Screw, Phillips Pan Head 4-40X1/4		2
397	Screw, Phillips Pan Head 4-40X3/8		2

398	Screw, Phillips Pan Head 4-40X5/8		2
399	Screw, phillips Pan Head 6-32X1/4		8
400	Screw, Phillips Pan Head 6-32X3/8		7
401	Screw, Phillips Pan Head 6-32X1/2		1
402	Screw, Phillips Pan Head 8-32X1/4		2
403	Screw, Phillips Pan Head 8-32X3/8		4
404	Screw, Phillips Flat Head 2-56X1/4		3
405	Screw, Phillips Flat Head 2-56X1/2		4
406	Screw, Phillips Flat Head 2-56X5/8		2
407	Screw, Phillips Flat Head 4-40X3/8		2
408	Screw, Phillips Flat Head 6-32X3/8		6
409	Screw, Phillips Flat Head 6-32X1/2		8
410	Screw, Slotted Pan Head 0-80X3/32		1
411	Screw, Slotted Flat Head 0-80X5/32		1
412	Screw, Slotted Round Head 10-32X1/2		3
413	Screw, Hex Head 6-32X3/8		4
414	Screw, Socket Set 6-32X1/4		1
415	Screw(Metric) Slotted Pan Head	M2.0X5MM Blk Oxde	2
416	Slotted Pan Head M2.0X10MM		1
417	Slotted Pan Head M2.5X4MM		3
418	Slotted Pan Head M2.5X5MM		3
419	Slotted Pan Head M2.5X6MM		5
420	Slotted Pan Head M2.5X8MM		5
421	Slotted Pan Head M2.5X12MM		1
422	Slotted Pan Head M3.0X8MM		1
423	Screw, Socket Head 2-56X3/16		2
424	Screw, Socket Head 2-56X3/8		3
425	Screw Socket Head 4-40X3/8		4
426	Screw, Socket Head 6-32X1/2		
427	Screw, Metric-Slotted Flat Head	M2.0X6MM	1
428	Slotted Flat Head M2.5X6MM		2
429	Slotted Flat Head M2.5X8MM		
430	Slotted Oval Head M3.0X10MM		2
431	Screw Metric-Slotted Headless Set	M4.0X10MM	1
432	Screw, Shoulder	4314	2
433	Head-In Solenoid, (Int. Duty)	3HD	1
434	Head-Out Solenoid, Int. Duty)	#28	2

435	Rewind Solenoid, (Cont Duty)(w/plunger)		1
436	Solvent (Isoprophyl Alcohol)		AR
437	Spring, Loader Latch	LE-016A-00MW	1
438	Transistor, EOT/BOT Photosensitive	LS600	1
439	Washer, Flat (Plain) #2		20
440	Washer, Flat (Plain) #4		3
441	Washer, Flat (Plain) #6		10
442	Washer, Flat (Plain) #8		
443	Washer, Splitlock #2		27
444	Washer, Splitlock #4		11
445	Washer, Splitlock #6°		24
446	Washer, Splitlock #8		6
447	Washer, Flat ("D")	5734-4	7
448	Washer, Flat (Laminated)	5722-3-2A	2
449	Washer, Flat (Shim) .005	G78-2	AR
450	Washer, Flat (Shim) .010	G78-4	AR
451	Washer, Flat (Shim) .020	G78-5	AR
452	Washer, Spring	3539-14-02	2
453	Plate (Switch Mounting)	20040	1
454	Block (Pivot)	20042	1
455	Screw, Phillips Flat Head	2-56X3/8	4
456	Screw, Pan Head Slotted	M2.5X10MM	1
457	Buffer Spring Assy	344-70009	1
458	Washer, Splitlock #3		13
459	Screw	N8	2
460	Screw	N7	
461	Screw, Phillips Pan Head	2-56X7/16	3
462	Extender Card (Logic Module)	344-50039	AR
463	STANDOFF(Motor)	1580-105	1

APPENDIX F EXPLOSION DIAGRAMS


DETAIL A
SEE SHT 2
272 REF
276 REF (LH)
277 PEF (RH)
SEE DETAIL A
REF, SEE SHT 2
SEE DETAIL B
DETAIL B
434 REF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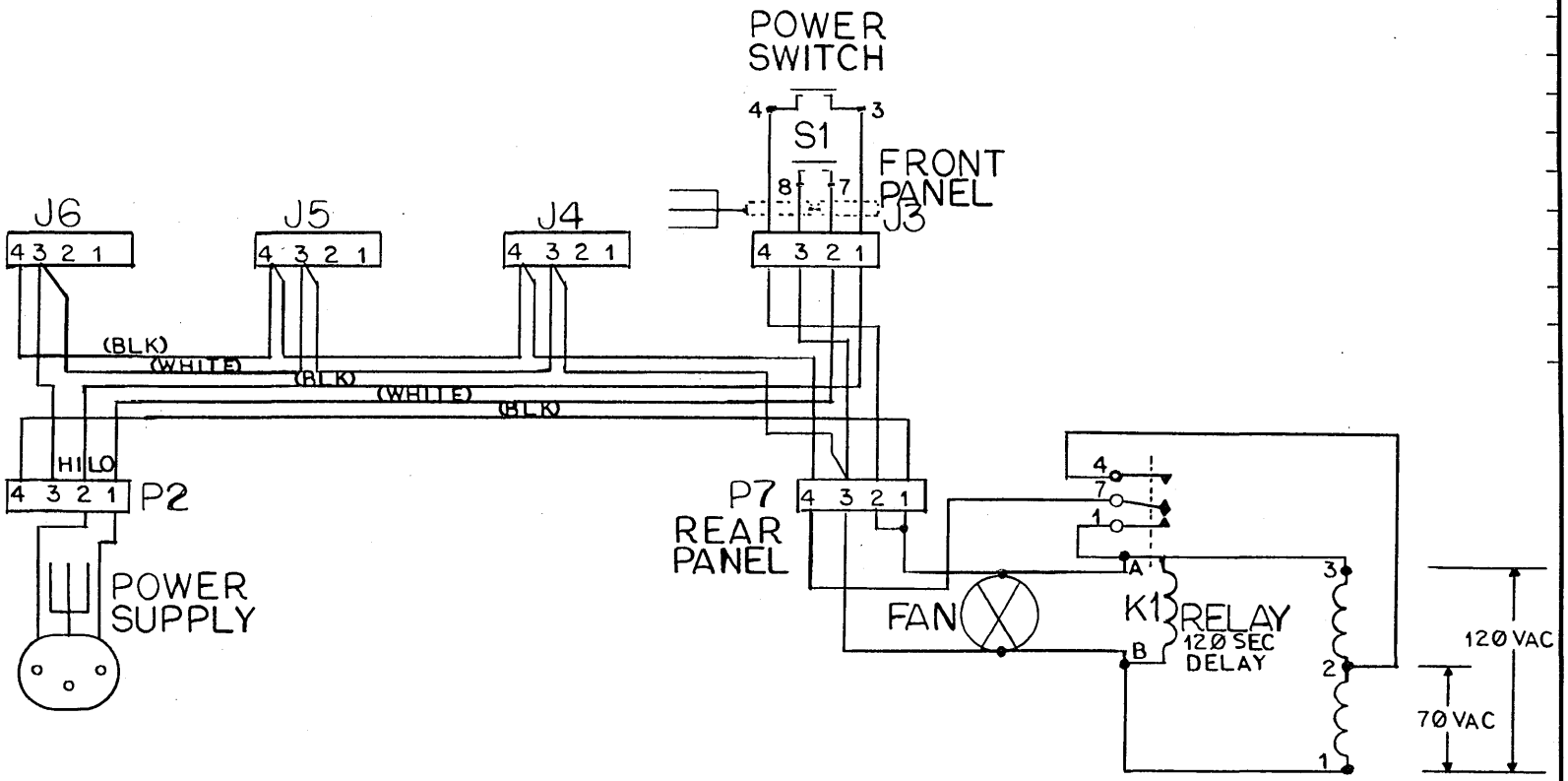
		DRAFTING	DATE	DESIGN	DATE



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	B	APPENDIX G	

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