BM873
restart/loader

digital equipment corporation · maynard, massachusetts

First Edition, January 1974
2nd Printing (Rev), April 1974

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CHAPTER 1
DESCRIPTION

1.1 INTRODUCTION

This manual describes the operation and theory of the BM873 Restart/Loader. This option is intended for use with the PDP-11 family of processors. The BM873

- serves as general purpose loader for processors of the 11 family,
- contains bootstrap loaders for all common devices,
- provides the capability of loading with a "hidden console",
- permits starting from several sources e.g., pushbutton, Watchdog Timer, MODEM control, power fail, etc.,
- gives PDP-11 systems an initial program load capability,
- contains at least four starting addresses, and
- permits the calling of a special user ROM program.

It is assumed that the reader is thoroughly familiar with the operation of the PDP-11 processor with which this option is used.

1.2 GENERAL DESCRIPTION

The BM873 option is mounted on a single quad-sized module which plugs into a small peripheral controller (SPC) slot. In its basic version, it contains several bootstrap loader programs within a 128-word Read-Only Memory (ROM). These programs may be loaded either from the console (Load Address and Start), by a JMP instruction in the program, or by an external contact closure or voltage level. The external interface is made via an 8-pin Mate-N-Lok connector. Specifications are listed in Table 1-1.

Table 1-1
BM873 Specifications

Capacity	128 words, read-only (256 words optional)
Word length	16 bits
ROM cycle time	500 ns
Voltage requirements	+5 V ±5% -15 V ±5%
Current requirements	1.0 A max @ +5 V 2.0 mA max @ -15 V
Operating temperature	10° to 50° C
Humidity	20% to 95%

1.3 FUNCTIONAL DESCRIPTION

The BM873 consists of two basic sections: the Restart Sequencer and the ROM.

Figure 1-1 shows the remote start timing. The Restart Sequencer takes contact closures or voltage levels and, after filtering and delaying, sets one of four Start Address Select flip-flops. The setting of one of the flip-flops causes the Begin Load Sequence flip-flop to set; this, in turn, initiates two one-shots to create a BUS AC LO/BUS DC LO sequence. The processor responds to the sequence by performing its normal power-down and power-up trap routines. Prior to the power-up sequence, however, the BM873 option asserts 773000 on the Unibus Address Lines. As a result, when the Program Counter (PC) and Processor Status Word (PSW) are restored, the data is taken from locations 773024/26 (nonvolatile memory systems) or from locations 773224/26 (volatile memory systems). Both of these addresses are locations within the BM873 option. The data from 773*24 is 173000; the data from 773*26 is 340, establishing a priority level of 7.

The data read from 773*24 (173000) will have an offset address ORed onto Offset Address bits 8 through 1, giving a range of 173000 to 173776. The offset address bits are enabled by one of the four Start Address Select flip-flops via a diode matrix (Paragraph 2.1.1). Each bootstrap loader program has its own starting address, and it is this address that is selected via the offset address bits.

The following sequence of operations would be typical:

- Close external switch and wait for switch filter delay.
- Assert AC LO; wait 6 ms.
- Assert DC LO for 6 ms; then wait 8 ms.
- Drop AC LO and assert address 773000.
- Wait for INIT to finish.
- The processor enters power-up routine.

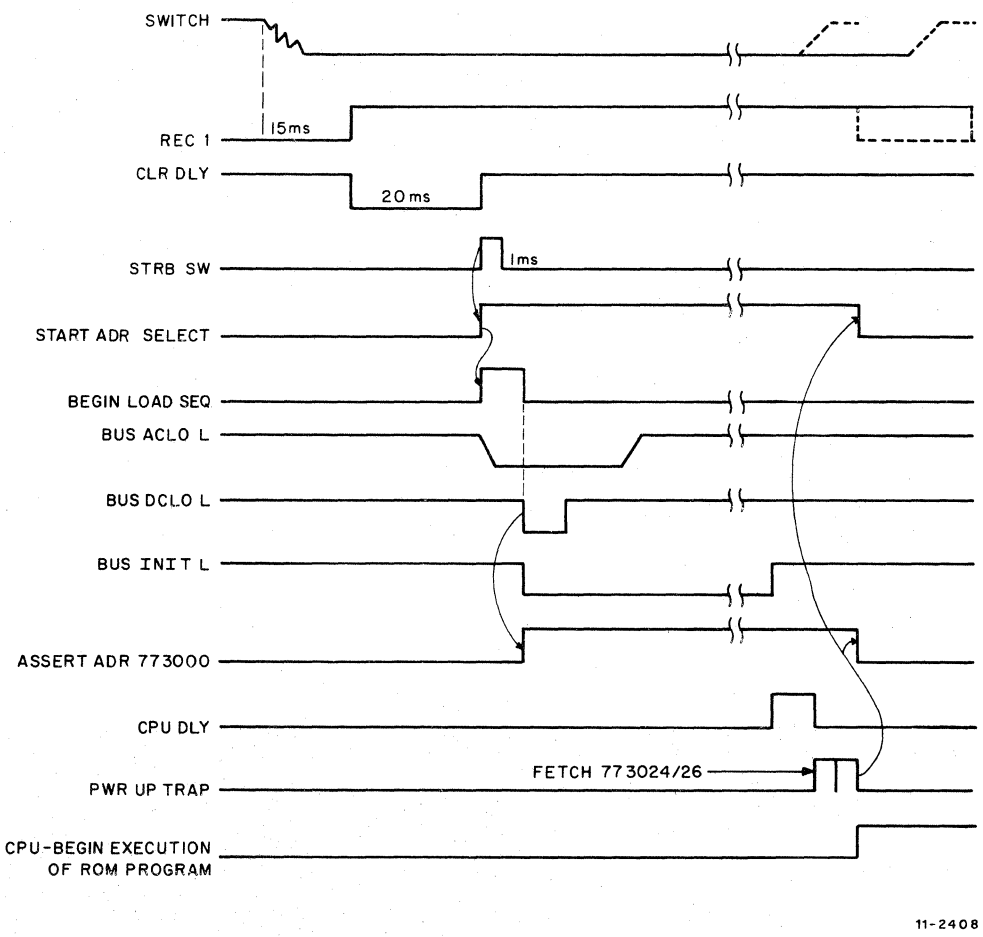

Figure 1-1 Remote Start Timing

- The BM873 option recognizes the fetch of address 773024 or 773224 and asserts 173XXX plus the 8-bit offset address to the data lines.
- The processor reads location 773026 or 773226 which is always 000340 (priority level 7).
- The processor fetches the next instruction from the ROM in address range 773000–773776. From this point, the bootstrap loader program contained in the ROM has control. (In the PDP-11/35 and PDP-11/40 systems, the PSW is fetched before the PC.)

If an actual power fail occurs in a nonvolatile memory system, the BM873 option does nothing, and the power-down and power-up traps work in the normal manner. If an actual power fail occurs in a volatile memory system, the power-up jumpers in the processor are set for 173224. During power-up the processor will fetch from 173224; the combination of address 773224 and no external lines asserted will cause the BM873 option to assert line 1 as a default case. Thus, in this case, the offset address selected for line 1 becomes the bootstrap loader call for power fail.

Data is read from the ROM in two bytes. Address bits 7 through 1 are present at all times via the bus receivers. Address bit 0 is generated on the module. A0 is always clear prior to a read cycle. The setting of A0 clocks the first byte into a holding register and simultaneously changes the address to gate the second byte to the output drivers. After a delay of about 200 ns, the output gates are enabled and the ROM data is placed on the Unibus. SSYN is asserted about 150 ns later, completing the read cycle. Figure 1-2 illustrates memory read timing.

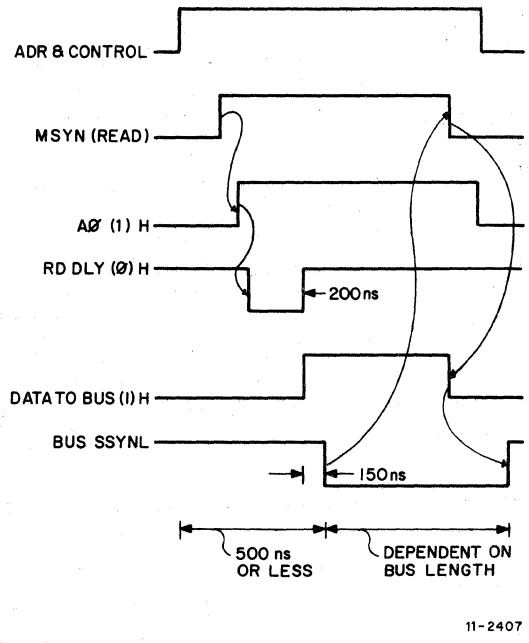

Figure 1-2 Memory Read Timing

CHAPTER 2
INSTALLATION AND CHECKOUT

2.1 INSTALLATION

Normally the BM873 Restart/Loader is installed at the factory and no further installation is required. However, if this option is added to an existing system, it may be necessary to add wiring to make the AC LO and DC LO signals available. These signals are provided on the PDP-11/05 and PDP-11/45 processors, and on the DD11-B. On the PDP-11/15, PDP-11/20, PDP-11/35, PDP-11/40, and the DD11-A it is necessary to ensure that the SPC slot containing the BM873 has BUS AC LO and BUS DC LO wiring available as follows:

Pin CV1 to B01F1 or B04F1 (BUS AC LO)

Pin CN1 to B01F2 or B04F2 (BUS DC LO)

If the wiring is not present, it must be added by hand-wiring, using a wire color different from that of the existing backplane wiring.

NOTE
The BM873 option must be on the CPU side of any bus buffer.

2.1.1 Start Address Selection

Each of the four external interface circuits has an associated address which must be specified for that circuit to be addressed. Each address consists of a fixed high-order portion (773XXX) and a low-order portion (bits 8 through 1) that is selected by adding or cutting diodes (Figure 2-1). When adding diodes, a low-wattage iron should be used and care should be taken with the plated mounting holes, so that the plating is not lifted from the laminate by the heat. The diodes (DEC type 664 or 1N3606) should be positioned so that their cathodes point toward the gold fingers of the module.

Table 2-1 lists starting addresses for various devices used with the BM873-YA Restart/Loader. The three rightmost digits of the address represent the low-order portion to be selected via diodes.

The diagnostic program for this option contains a listing of the loader program in the comments portion of the Data Compare section. That diagnostic will be updated to contain the starting addresses and listing of future variations (-YB, etc.).

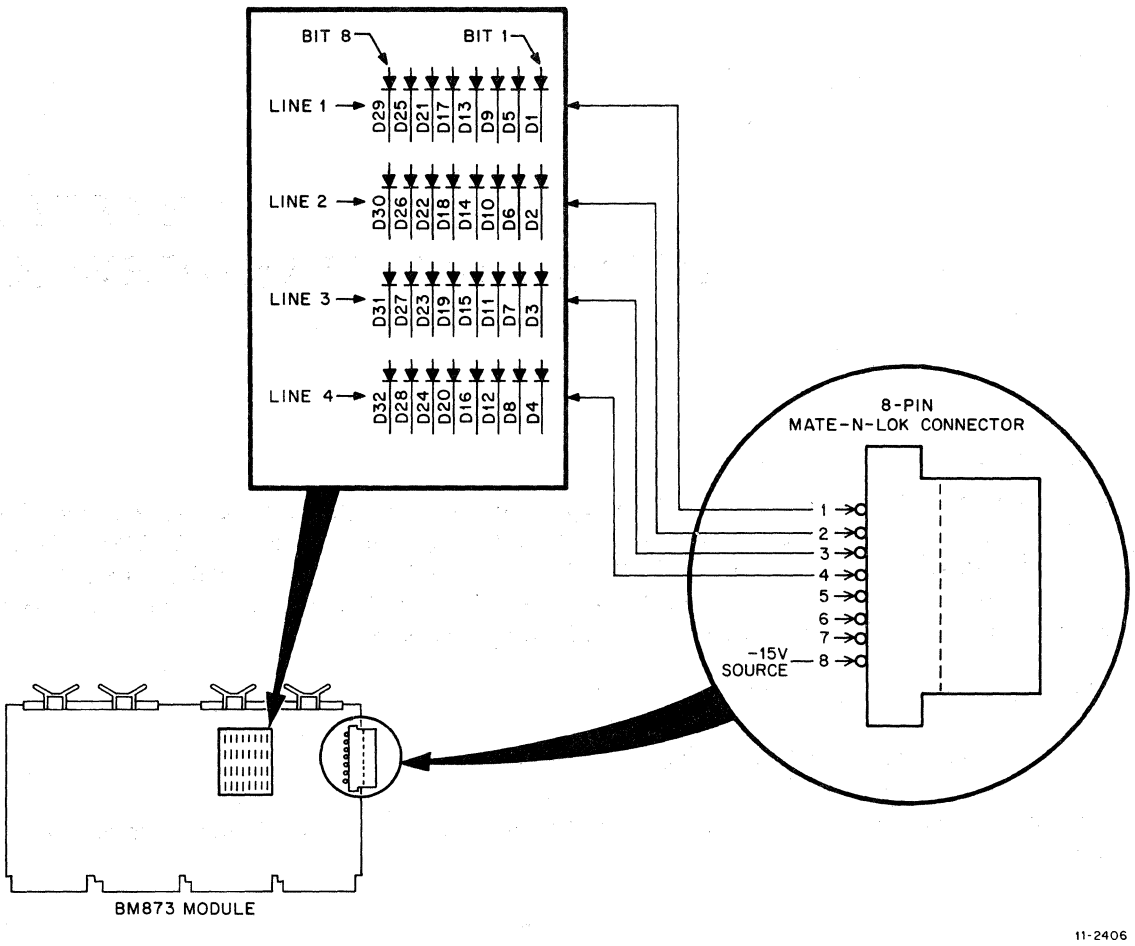

Figure 2-1 External Interface Circuit Diode Matrix

Table 2-1
BM873-YA Option Starting Addresses

Address	Device Type
773 000	RF11
773 010	RK11
773 020	Transfer to Address contained in Switch Register
773 030	TC11
773 050	TM11
773 100	RP11
773 144	RC11
773 210	KL11/DL11 – Console TTY Reader
773 230	TA11
773 312	PC11--Paper Tape Reader

2.1.2 Jumper Selection

The BM873 module contains three jumpers that are marked with the numerals 1, 2, and 3. Jumpers 1 and 2 are used to compensate for differences between the PDP-11/40 and 11/35 and all other PDP-11 family processors. Jumper 1 should be installed when the option is used with either the PDP-11/40 or the PDP-11/35. Jumper 2 should be installed for use with any other processor in the PDP-11 family.

Jumper 3 controls access to an extra 128 words of ROM. When this jumper is cut, additional addresses from 773400 to 773776 become available.

2.1.3 CPU Addressing with Volatile Memory

When this option is used in computers with volatile memory, the power fail trap address must be jumpered to 773224 if automatic reloading is desired.

For a PDP-11/45 CPU, install jumpers W6, W3, and W1 on the M8100 board. This will provide an address of 773224.

For a PDP-11/40 CPU, connect jumper W7 on the M7235 board for a binary 1. This jumper will provide an address of 7732XX. The last two digits are provided by jumpers 4 and 2.

2.2 CHECKOUT

The diagnostic program for the BM873 option is MAINDEC-11-DZBMX-A. This program starts with a dialogue and is self-explanatory. As new ROM programs are implemented, this diagnostic may be modified. However, the basic version may be used on all option variations as long as the user visually checks the ROM data following the first pass.

The diagnostic contains the instructions for its own operation. The opening dialogue establishes which option variation (-YA, -YB, etc.) is being tested.

CHAPTER 3
PROGRAMMING

This device is a Read-Only Memory and requires no programming. However, certain factors must be considered in system programming as the following paragraphs explain.

3.1 POWER FAIL PROGRAMMING

With the BM873 option installed, the power-down/power-up routines may require modification, depending on the bootstrap used. Use of the external interface causes the power-fail sequence in the CPU when AC LO is detected going low; the power-up trap program is not used, and, therefore, not restored.

This is not a problem when a bootstrap loads into core and overwrites location 24, because the new program will set up the power-fail routine. However, if the new program does not reload location 24, the next power-fail sequence (may be real) will find the power-up restore program instead of the power-down routine.

This condition can be resolved by the power-fail routine testing this option with any DATI instruction. The combination of this option and a real power-fail will cause the DATI to perform in a normal manner. The combination of this option and the external interface active (causing the AC LO and trap) will cause a nonexistent device trap (no SSYN) to location 4.

```
        MOV             #1S,@#4         ; TRAP CATCHER
        CLR             @#6
        TST             @#173000        ; DEV BLIND?
        NOP
2S:     MOV             #PWRUP,@#24     ; REAL PWR FAIL
        (SAVE ROUTINE)
1S:     HALT
```

Example 1

The above program works because this option goes "blind" (will not return SSYN) when it has been activated by an external interface signal. This condition continues from the assertion of AC LO until the release of DC LO.

3.2 REGISTER DESCRIPTION

There are no registers in this device. There are four flip-flops that can be loaded for diagnostic purposes but they cannot be read.

CHAPTER 4
OPTIONS

4.1 USER CUSTOM PROGRAM

Two etched circuit positions on the board provide an extra 128 words of ROM. To add this extra memory capacity, Jumper 3 must be cut, permitting address recognition of all 256 words.

Figure 4-1 is a sample ROM program data sheet that can be helpful in programming the ROMs. Columns 1 and 2 contain the PDP-11 program listing. From the address data in column 1, the ROM starting address can be determined and the offset diodes cut (diode = 1; no diode = 0). The data in column 2 must be expressed in binary form as in columns 3 and 4. (Note that byte 1 is moved to the line below that of the original entry.) The eight binary digits for each byte are then shifted into columns 5 and 6 under the ROM B and ROM A headings, respectively. Columns 7 and 8 contain the resulting ROM address in binary and decimal form, respectively. Column 8 consists of four columns of decimal addresses, distinguished by the configuration of the 2 MSB of the binary address. Each program data sheet contains 64 ROM locations (32 words), hence four sheets are required to encode all 128 words. Therefore, only one of the four subcolumns of decimal addresses actually applies for each sheet, and the other three should be crossed out to avoid confusion. The 2-column checklist between columns 7 and 8 can be used for checkoff purposes, e.g., checking off ROMs as they are blasted.

A blank program data sheet is included in Chapter 6 to assist the user in programming the read-only memory of the BM873.

Customers who wish to create their own programs can purchase PROMs from integrated circuit vendors or distributors. Some distributors have programming capabilities so that programmed ROMs can be purchased. The following PROMs have been found acceptable:

Intersil type 5603A
Monolithic Memories Inc. type 6300

The following PROMs have not been tested but according to the manufacturer's data should be acceptable. Any PROM that is specified to be "pin compatible with the 74187" should work in this application.

National Semiconductor type DM8573
Signetics type 82S26

Sheet of 4

Choose one of four sheets. Cross out the other three address lists.

ROM Program Data Sheet – 32_{10} Word Block

Program Listing Addr.	Program Listing Data	Octal List Byte "1"	Octal List Byte "0"	ROM "B" 3 2 1 0	ROM "A" 3 2 1 0	ROM Addr. 5 4 3 2 1	0	A	B	Address Bits 7 & 6 = 00	= 01	= 10	= 11
173000	010702		11 000 010	1100	0010	00000	0	✓	✓	0	64	128	192
		0 001 000 1		0001	0001		1	✓	✓	1	65	129	193
173002	000455		00 101 101	0010	1101	00001	0	✓	✓	2	66	130	194
		0 000 000 1		0000	0001		1	✓	✓	3	67	131	195
173004	177462		00 110 010	0011	0010	00010	0	✓		4	68	132	196
		1 111 111 1		1111	1111		1	✓		5	69	133	197
173006	000005		00 000 101	0000	0101	00011	0	✓		6	70	134	198
		0 000 000 0		0000	0000		1	✓		7	71	135	199
173010	010702		11 000 010	1100	0010	00100	0	✓		8	72	136	200
		0 001 000 1		0001	0001		1	✓		9	73	137	201
173012	000451		00 101 001	0010	1001	00101	0	✓		10	74	138	202
		0 000 000 1		0000	0001		1	✓		11	75	139	203
173014	177406		00 000 110	0000	0110	00110	0	✓		12	76	140	204
		1 111 111 1		1111	1111		1	✓		13	77	141	205
			00		0000	00				14	78		206
173066	000423		00 010 011	0001		11011	0	✓			118	182	246
		0 000 000 1		0000	0001		1	✓		55	119	183	247
173070	176716		11 001 110	1100	1110	11100	0	✓		56	120	184	248
		1 111 110 1		1111	1101		1	✓		57	121	185	249
173072	000005		00 000 101	0000	0101	11101	0	✓		58	122	186	250
		0 000 000 0		0000	0000		1	✓		59	123	187	251
173074	010702		11 000 010	1100	0010	11110	0	✓		60	124	188	252
		0 001 000 1		0001	0001		1	✓		61	125	189	253
173076	000417		00 001 111	0000	1111	11111	0	✓		62	126	190	254
		0 000 000 1		0000	0001		1	✓		63	127	191	255

Figure 4-1 Sample ROM Program Data Sheet

CHAPTER 5
INTERFACE

The external interface consists of four separate high-impedance receivers with 4.7-kilohm resistors in series with each one. A -15 V source is provided through 10 kilohms to facilitate the use of contact closures. The external interface also accepts single-ended voltage inputs. A signal of 0.5 mA at -4 V or greater will cause a Restart sequence. The maximum permissible input is ±25 V.

These inputs are filtered with RC networks and Schmitt triggers and have a time delay of approximately 10 to 15 ms. The signal must remain for at least 45 ms. Only one external line may be active at a time; two or more active at the time of the sample will cause a race condition until one wins, but the result will be indeterminate.

The interface connector is an 8-pin male Mate-N-Lok (DEC Part Number 12-09340-01). Five pins (DEC Part Number 12-09378) are required for connection--placed as shown in Figure 2-1.

CHAPTER 6
ENGINEERING DRAWINGS

This chapter contains the 3-sheet engineering drawing of the BM873 (D-CS-M873-0-1) and a blank program data sheet for use in programming the read-only memory of this option. Use of these sheets is described in Chapter 4 of this manual.

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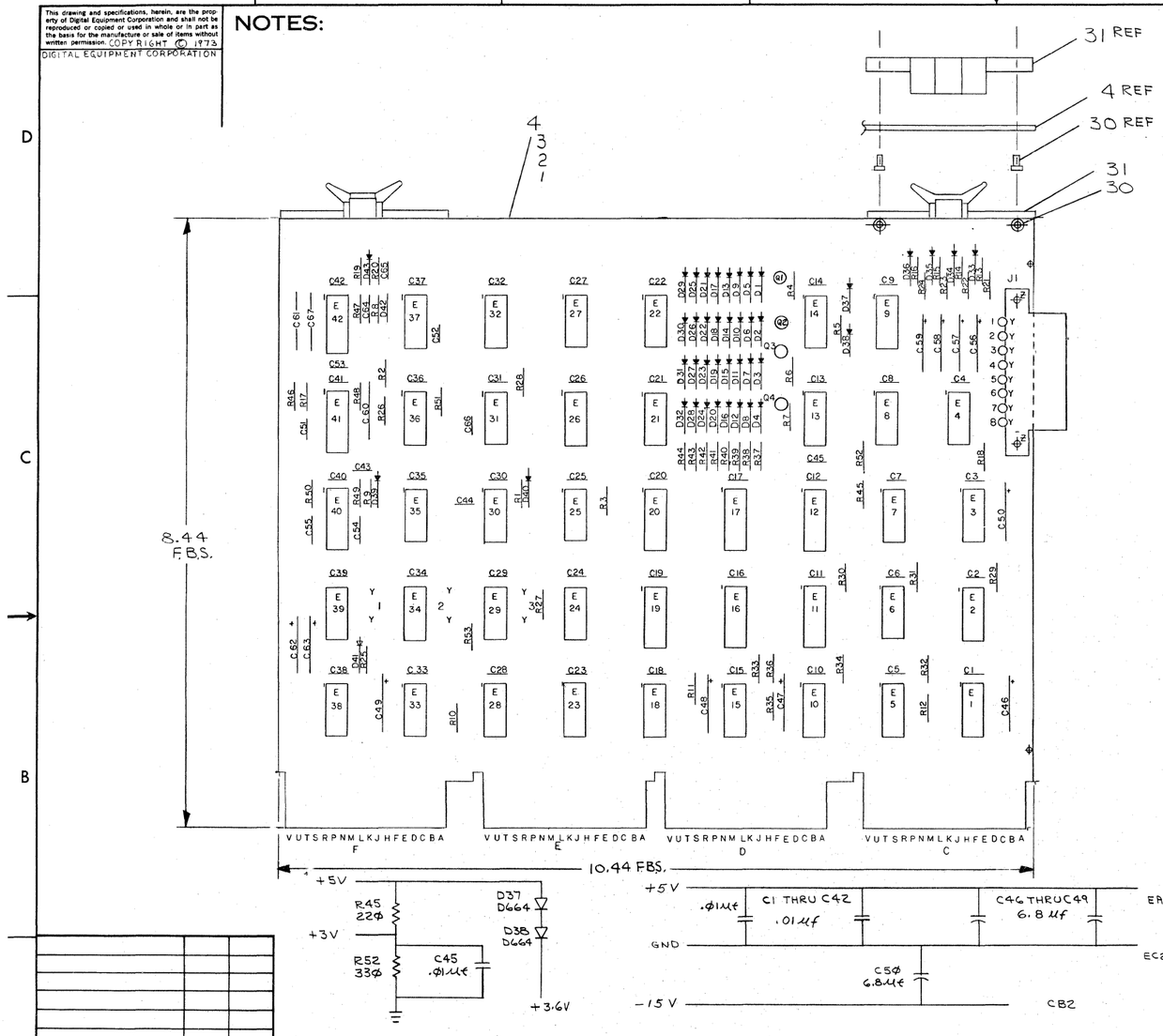
NOTES:



M873-YA	M873-0				
REF	REF		X-Y COORDINATE HOLE LOCATION	K-CO-M873-0-4	1
REF	REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M873-0-5	2
REF	REF		MODULE ECO HISTORY	B-MH-M873-0-6	3
1	1		ETCHED CKT BRD	5010703	4
1	1	C51	CAP 33 PF 100V DM	1000009	5
1	1	C52	CAP 100 PF 100V DM	1000016	6
2	2	C65,C66	CAP 470 PF 100V DM	1000024	7
46	46	C1-C45,C53	CAP .01 UF 50V 20% DISC	1001610	8
1	1	C64	CAP .15 UF 35V 20% TANT	1002180	9
2	2	C54,55	CAP 1 UF 35V 10% TANT	1001776	10
4	4	C56-C59	CAP 2.2 UF 35V 10% TANT	1002431	11
2	2	C60,C61	CAP 3.3 UF 20V 10% TANT	1005334	12
5	5	C46-C50	CAP 6.8 UF 35V 10% TANT	1005306	13
3	3	C62,C63,C67	CAP 39 UF 10V 10% TANT	1000076	14
43	43	D1-D43	DIODE D664	1100114	15
1	1	J1	CONNECTOR	1209340	16
5	5		PINS CONTACT	1209456	17
1	1	R51	RES 100 1/4W 5%	1300229	18
9	9	R37-R45	RES 220 1/4W 5%	1300271	19
1	1	R52	RES 330 1/4W 5%	1300295	20
8	8	R29-R36	RES 470 1/4W 5%	1300316	21
13	13	R1-R12,R20	RES 1K 1/4W 5%	1300365	22
8	8	R21-R28	RES 4.7K 1/4W 5%	1300447	23
8	8	R13-R19,R53	RES 10K 1/4W 5%	1300479	24
5	5	R46-R50	RES 18K 1/4W 5%	1302465	25
4	4	Q1-Q4	TRANS MXAA55	1510706	26
2	2		SCREW NYLON	9006401-4	27
2	2		NUT HEX NYLON	9007992	28
6	6		SPLIT LUG	9006735	29
8	8		EYELET	9006732	30
4	4		HANDLE FLIP/CHIP MAGENTA	9008337-06	31
6	6	E6,7,8,9,13,25	I.C. 7400	1905575	32
1	1	E34	I.C. 7404	1909686	33
1	1	E31	I.C. 7410	1905576	34
1	1	E29	I.C. 7430	1905578	35
4	4	E14,21,30,37	I.C. 7474	1905547	36
3	3	E40,41,42	I.C. 74123	1910436	37
2	2	E11,12	I.C. 74175	1910651	38
8	8	E1,2,3,5,15,24,28,36	I.C. 8881	1909705	39
5	5	E22,26,27,32,35	I.C. 8815	1909713	40
7	7	E4,10,18,23,33,38,39	I.C. 11380	1911113	41
1	—	E16	I.C. 74187	23044-A2	42
1	—	E17	I.C. 74187	23045-A2	43
REF			ROM LISTING FOR 23045A2	K-RL-M873-0-8	44
REF			ROM LISTING FOR 23044A2	K-RL-M873-0-7	45
REF			WORD LISTING OF ROM CONTENTS	B-AP-M873-0-9	46
QTY	QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

7-175	8	16
11380	1	8
74123	8	16
74187	8	16
IC TYPE	GND	+ 5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

BRUNING 40-522 16699

DEC FORM NO. DRD-135A

FIRST USED ON OPTION MODEL: PDP 11

PARTS LIST

ETCH BOARD REV C

SEMICONDUCTOR CONVERSION CHART

DEC NO.	EIA NO.	DEC NO.	EIA NO.

REV	CHANGE NO.	CHK
A	ORIGINATED	R. DIETER 3-18-47
B	M873-00001	Edam 4-16-74

DRN. K. Davis DATE 11-10-73
CHK'D. Tom Hall DATE 11-10-73
ENG. DATE
PROJ. ENG. DATE
MGR. DATE 11-13-73

NEXT HIGHER ASSY: R-DD-BM873-0
SCALE NONE
SHEET 1 OF 3

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: RESTART LOADER

SIZE D | CODE CS | NUMBER M873-0-1 | REV. B

DIST.

SIZE D | CODE CS | NUMBER M873-0-1 | REV B

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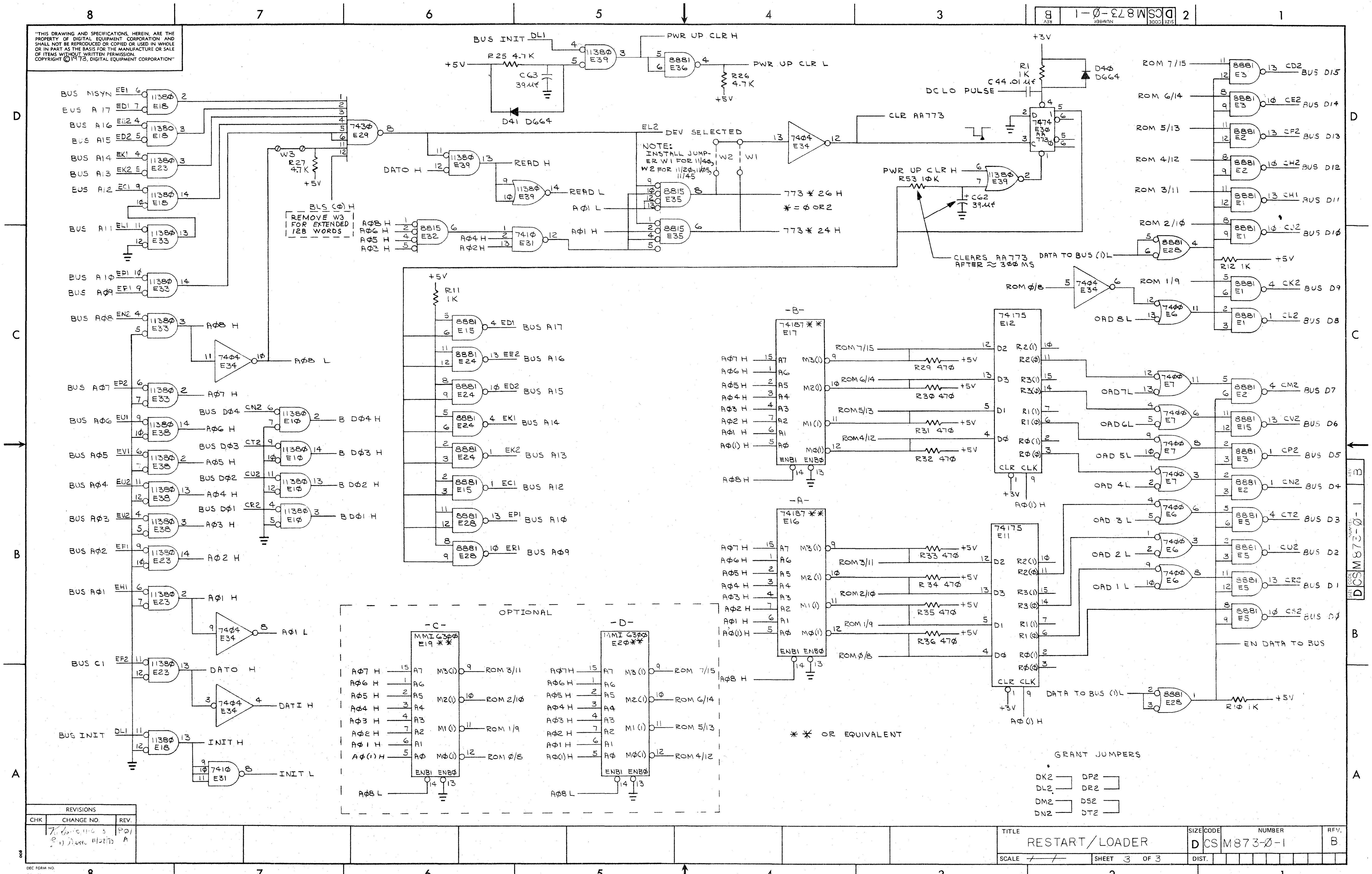
REMOVE R3 TO DELETE DEFAULT ADDRESS FEATURE

DATO *24L
773 *24 H
DATO H
BEGIN CLK H
INIT L
BLS(1) H
BLS(Φ) H
PWR UP CLR L
2ΦMS
4 CN1
BUS DCLO
6MS
DCLO PULSE
1Φ CV1
BUS ACLO
REC 1
REC 2
REC 3
REC 4
STRB SW H
CLR SA FLOPS
READ H
RD DLY (Φ) H
DATA TO BUS (1) L
DATO *24 L
R2 1K
BUS SSYN L
1Φ EJ1
READ L
A Φ (1) H
A Φ (Φ) H
RD DLY (Φ) H
2ΦΦ NS
SAS 1 (Φ) L
SAS 2 (Φ) L
SAS 3 (Φ) L
SAS 4 (Φ) L
EN OFF ADR H
BDΦ1 H
BDΦ2 H
BDΦ3 H
BDΦ4 H
SAS 1 (1) H
SAS 2 (1) H
SAS 3 (1) H
SAS 4 (1) H
CLR SA FLOPS H
+3.6V
MX A A55
Q1
Q2
Q3
Q4
R3 1K
R4 1K
R5 1K
R6 1K
R7 1K
TO D7
BEGIN CLK H
DATI H
773 *24 H
EN OFF ADR H
OAD 8
OAD 7
OAD 6
OAD 5
OAD 4
OAD 3
OAD 2
OAD 1

REVISIONS		
CHK	CHANGE NO.	REV.
T. Wood 11/5/73	D01	
K. Davis 11/6/73	D02	
		A

TITLE	SIZE	CODE	NUMBER	REV.
RESTART LOADER	D	CS	M873-Ø-1	B
SCALE —	SHEET 2 OF 3	DIST.		

DEC FORM NO. DRD 138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BUS INIT
PWR UP CLR H
PWR UP CLR L
DEV SELECTED
NOTE: INSTALL JUMPER W1 FOR 11/40, W2 FOR 11/20, 11/05, 11/45
CLR AA773
DC LO PULSE
READ H
READ L
DATO H
REMOVE W3 FOR EXTENDED 128 WORDS
CLEARS AA773 AFTER ≈ 300 MS
DATA TO BUS (1) L
OPTIONAL
-A-
-B-
-C-
-D-
** OR EQUIVALENT
EN DATA TO BUS
GRANT JUMPERS
DK2 DL2 DM2 DN2 DP2 DR2 DS2 DT2
BUS MSYN
BUS A17
BUS A16
BUS A15
BUS A14
BUS A13
BUS A12
BUS A11
BUS A10
BUS A09
BUS A08
BUS A07
BUS A06
BUS A05
BUS A04
BUS A03
BUS A02
BUS A01
BUS C1
DATO H
DATI H
INIT H
INIT L
BUS D15 BUS D14 BUS D13 BUS D12 BUS D11 BUS D10 BUS D9 BUS D8 BUS D7 BUS D6 BUS D5 BUS D4 BUS D3 BUS D2 BUS D1 BUS D0
REVISIONS
CHK
CHANGE NO.
REV.
TITLE
RESTART/LOADER
SIZE D
CODE CS
NUMBER M873-0-1
REV. B
SCALE
SHEET 3 OF 3
DIST.
DEC FORM NO. DRD 138

ROM Program Data Sheet – 32_{10} Word Block

Sheet of 4

Choose one of four sheets. Cross out the other three address lists.

Program Listing Addr.	Program Listing Data	Octal List Byte "1"	Octal List Byte "0"	ROM "B" 3 2 1 0	ROM "A" 3 2 1 0	ROM Addr. 5 4 3 2 1	0	A	B	Address Bits 7 & 6: 7 6 = 00	7 6 = 01	7 6 = 10	7 6 = 11
						0 0 0 0 0	0			0	64	128	192
							1			1	65	129	193
						0 0 0 0 1	0			2	66	130	194
							1			3	67	131	195
						0 0 0 1 0	0			4	68	132	196
							1			5	69	133	197
						0 0 0 1 1	0			6	70	134	198
							1			7	71	135	199
						0 0 1 0 0	0			8	72	136	200
							1			9	73	137	201
						0 0 1 0 1	0			10	74	138	202
							1			11	75	139	203
						0 0 1 1 0	0			12	76	140	204
							1			13	77	141	205
						0 0 1 1 1	0			14	78	142	206
							1			15	79	143	207
						0 1 0 0 0	0			16	80	144	208
							1			17	81	145	209
						0 1 0 0 1	0			18	82	146	210
							1			19	83	147	211
						0 1 0 1 0	0			20	84	148	212
							1			21	85	149	213
						0 1 0 1 1	0			22	86	150	214
							1			23	87	151	215
						0 1 1 0 0	0			24	88	152	216
							1			25	89	153	217
						0 1 1 0 1	0			26	90	154	218
							1			27	91	155	219
						0 1 1 1 0	0			28	92	156	220
							1			29	93	157	221
						0 1 1 1 1	0			30	94	158	222
							1			31	95	159	223
						1 0 0 0 0	0			32	96	160	224
							1			33	97	161	225
						1 0 0 0 1	0			34	98	162	226
							1			35	99	163	227
						1 0 0 1 0	0			36	100	164	228
							1			37	101	165	229
						1 0 0 1 1	0			38	102	166	230
							1			39	103	167	231
						1 0 1 0 0	0			40	104	168	232
							1			41	105	169	233
						1 0 1 0 1	0			42	106	170	234
							1			43	107	171	235
						1 0 1 1 0	0			44	108	172	236
							1			45	109	173	237
						1 0 1 1 1	0			46	110	174	238
							1			47	111	175	239
						1 1 0 0 0	0			48	112	176	240
							1			49	113	177	241
						1 1 0 0 1	0			50	114	178	242
							1			51	115	179	243
						1 1 0 1 0	0			52	116	180	244
							1			53	117	181	245
						1 1 0 1 1	0			54	118	182	246
							1			55	119	183	247
						1 1 1 0 0	0			56	120	184	248
							1			57	121	185	249
						1 1 1 0 1	0			58	122	186	250
							1			59	123	187	251
						1 1 1 1 0	0			60	124	188	252
							1			61	125	189	253
						1 1 1 1 1	0			62	126	190	254
							1			63	127	191	255

BM 873 RESTART/LOADER
DEC-11-H873A-B-D

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Does it satisfy *your* needs? _____ Why? _____

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Would you please indicate any factual errors you have found. _____

_____

_____

_____

Please describe your position. _____

Name _____ Organization _____

Street _____ Department _____

City _____ State _____ Zip or Country _____

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