DEC-08-16AA-D

OSCILLOSCOPE DISPLAY CONTROL
34D
INSTRUCTION MANUAL

NOVEMBER 1967

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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1 INTRODUCTION

Digital Equipment Corporation of Maynard, Massachusetts, offers as part of its product line an oscilloscope display, designated Type 34D, which may be supplied as an option to a PDP-8 or PDP-8/S system. The display unit allows information from a digital computer to be displayed on the oscilloscope as a point of light whose location is specified by two 10-bit digital words.

The basic 34D Oscilloscope Display Unit consists of a Tektronix RM-503 Oscilloscope or equivalent and its associated logic controls.

A photomultiplier light pen, optional with the 34D, can be employed to exercise control over, or to communicate with, a running computer program.

2 SCOPE

This manual provides complete maintenance data on the logic circuitry, as it relates to the 34D Oscilloscope Display and both the PDP-8 and PDP-8/S. This manual also includes detailed information on logic operation, interface characteristics and connections, and installation and mounting.

3 OPERATION

The 34D Oscilloscope Display accepts both vertical and horizontal 10-bit coordinate address words from bits 2 through 11 of the PDP-8 accumulator. Pulses that are generated internally by the 34D Oscilloscope Display control logic transfer the 10-bit words into an X-axis buffer and a Y-axis buffer. The outputs of these buffers, converted from digital to analog levels, provide dc-level deflection inputs to the display oscilloscope. Logic circuits implement these function by interpreting commands (IOP pulses) generated in the computer.

A 6-bit address code, in the computer memory buffer, provides the basic activating signal to the logic control of the display. The sensing of the address code by the logic circuits enables the receipt of processor-generated IOP pulses. In the display control logic, IOT pulses control operation of the display unit. Upon receipt of IOP pulses, the functions of the IOT pulses that are generated in the display control logic are as follows.

IOT 051 (061) clears the 10-bit X (Y) buffer registers.

IOT 052 (062) loads the 10-bit X (Y) buffer registers with data from the processor accumulator.

IOT 054 (064) intensifies the point of light at the location determined by the X- and Y-address words.

IOT 071 allows the program to skip if the light pen flag is a ONE.

IOT 072 clears the light pen flag.

IOT 074 clears the brightness registers.

IOT 075 sets brightness register to 1.

IOT 076 sets brightness register to 2.

IOT 077 sets brightness register to 3.

3.1 Program Instructions

Table 3-1 lists the instructions from the processor that provide all necessary control over the operation of the Type 34D Oscilloscope Display.

Table 3-1
Control Instructions

Mnemonic	Octal Code	Operation
DCX (DCY)	6051 (6061)	Generates an IOP pulse at event time 1 to clear the X (Y) buffer in preparation for receiving new display data.
DXL (DYL)	6053 (6063)	Generates an IOP pulse at event time 1 (IOP1) and an IOP pulse at event time 2 (IOP2) to clear the X (Y) buffers and then load in new data from bits 2 through 11 of the accumulator.
DIX (DIY)	6054 (6064)	Generates an IOP pulse at event time 3 (IOP4) to intensify the point defined by the content of the X- and Y-coordinate buffers. This command can be combined with the DXL (DYL) command.
DXS	6057	Generates IOP pulses IOP1, IOP2, and IOP4 at event times 1, 2, and 3, respectively, to execute the combined functions performed by the DXL and DIX commands. The X-coordinate buffer is cleared and loaded with new data; then the point defined by the X- and Y-buffers is intensified.
DYS	6067	Generates IOP pulses IOP1, IOP2, and IOP4 at event times 1, 2, and 3, respectively, to execute the combined functions performed by the DYL and DIY commands. The Y-coordinate buffer is cleared and loaded with new data; then the point defined by the content of the X- and Y-buffers is intensified.
DSB	607X	Generates an IOP pulse at event time 3 (IOP4) to load the content of bits 10 and 11 of the instruction into the brightness register. When the instruction is 6075, the minimum brightness (0.4 μs) is set, when 6076, the medium brightness is (0.8 μs) is set, and when 6077, the maximum brightness (3 μs) is set.

3.2 Logic Operation

The following paragraphs describe the operation of the logic control of the Type 34D Oscilloscope Display as it relates to the PDP-8 and PDP-8/S computers. Logic controls for the oscilloscope display appear on DEC engineering drawing BS-D-34D-0-2, sheets 1 and 2 located in section 8 of this manual. When referring to particular logic controls in the text, the sheet number and coordinate location will be given. The coordinate location is a letter/number designation used on DEC drawings to facilitate the location of individual logic controls.

3.2.1 Processor Turn-On - During the processor turn-on period, or whenever the START key is depressed, POWER CLEAR pulses (–3V, 100-ns pulses at a 10 KHz rate) clear the light pen flag flip-flop (sheet 1, D5) and set brightness registers 0 and 1 (sheet 1, B5) to the ONE state. With both brightness registers in the ONE state, the point of light on the oscilloscope is at maximum brightness.

3.2.2 Coordinate Channels - Because the horizontal (X) and vertical (Y) coordinate channels operate identically, only the horizontal channel will be discussed in detail.

3.2.2.1 Initiate - Computer-generated command pulses initiate operation of the 34D Oscilloscope Display. The computer sends the address code of the peripheral device over the I/O bus lines. This display control logic senses the address code, through connectors BOD3 and BOD4 (sheet 2, D1), in the W103 Device Selector at BOA10, BOB10 (sheet 2, C2, D2). (The address code is stored in computer memory buffer bits 3 through 8.) Sensing, by the display control logic, of its own discrete address code allows acceptance of the IOP pulses, generated by the computer, and provided at terminals K, M, and P of connector BOD2 (sheet 2, C1). The decoded address enables the input gates to the three pulse amplifiers (PA) on the W103 Device Selector at BOA10, BOB10 (sheet 2, C2). When enabled, these gates permit incoming IOP pulses to activate their respective PA to produce the IOT pulses actually used within the display control circuits.

3.2.2.2 Clearing and Loading the Buffer - Initially, the computer generates a DCX instruction, setting up the I/O address, and transmitting an IOP1 pulse to the display control through terminal K of connector BOD2 (sheet 2, C1). The 100-ns pulse (IOT 051), which is generated by the ADAE PA in the W103 Device Selector, clears all ten R203 Data Buffer Registers at connectors BOA16 through BOA18, BOA24 (sheet 2, B2 through B8). The DCX instruction is normally generated at the start of the program run to ensure that the data buffer registers are all in the ZERO state. For the remainder of the program, the clear instruction is combined with the load instruction (delayed by 1 μs) to increase the speed of operation.

Typically, an IOP1 pulse (at event time 1) and an IOP2 pulse (at event time 2) are generated by the processor in the same computer cycle. The IOT 051 (event time 1) pulse, generated within this control logic, clears the ten R203 Data Buffer Registers (BOA16 through BOA18, BOA24) (sheet 2, B2 through B8) to prepare them for acceptance of new data. The IOT 052 pulse (positive-going transition at event time 2), occurring either 1 μs or 4.75 μs later, is applied to the ten DCD gates (sheet 2, B2 through B8) in the buffer. The instructions DXL and DCX (1 μs and 4.75 us, respectively) determine when the IOT 052 pulse appears at the input to the DCD gates in the buffer.

The horizontal address word is loaded into the data buffer registers through connectors BOA1 and BOA2 (sheet 2, B2 through B8). This, together, with the positive-going IOT 052 pulse enables the DCD gate. When enabled, the DCD gate activates the data flip-flop register and sets it to the ONE level (−3V). With any bit a logic ZERO (−3V) at connectors BOA1 and BOA2, the corresponding DCD gate is inhibited preventing the data flip-flop from being set to the ONE state. Thus the output of the flip-flop is now set to the same number held by the accumulator.

3.2.2.3 Digital-to-Analog Conversion - The 10-bit horizontal address word at the output of the data flip-flops is converted into an analog voltage between ground and −10V. This is accomplished by four 3-input A601 Digital-to-Analog Converters at connectors BOA20 through BOA23 (sheet 2, B2 through B8). (The D/A converter, at connector BOA23, utilizes only the most significant input, pin U.) The analog voltage varies between its upper and lower limits in 1024 discrete intervals, and is directly proportional to the numerical value of the coordinate address.

A −3V input signal at all inputs to the D/A converter produces a ground level output. Conversely, a 0V at all inputs produces a −10V analog output (see Table 3-2). This output connects to the oscilloscope through pin D of connector BOA32 (sheet 2, A2). Ten data flip-flop registers provide accessibility to 1024 possible locations (2^{10}) on the oscilloscope.

Table 3-2
Coordinate-Channel Logic Conversion Table

Digital Address and Flip-Flop States	Buffer Output and D/A Converter Input	D/A Converter Output
1 1 1 1 1 1 1 1 1 1	x x x x x x x x x x	most positive (ground)
1 1 1 1 1 1 1 1 1 0	x x x x x x x x x 0	
.	.	.
.	.	.
.	.	.
.	.	.
1 0 0 0 0 0 0 0 0 1	x 0 0 0 0 0 0 0 0 x	

Table 3-2
Coordinate-Channel Logic Conversion Table (continued)

Digital Address and Flip-Flop States	Buffer Output and D/A Converter Input	D/A Converter Output
1 0 0 0 0 0 0 0 0 0	x 0 0 0 0 0 0 0 0 0	•
0 1 1 1 1 1 1 1 1 1	0 x x x x x x x x x	•
0 1 1 1 1 1 1 1 1 0	0 x x x x x x x x 0	•
•	•	•
•	•	•
•	•	•
•	•	•
0 0 0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0 0 x	most negative (-10volts)
0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	
0 = logic zero = ZERO state 1 = logic one = ONE state	0 = ground x = −3V	

3.2.3 Intensity Circuits - At event time 3, the computer generates a DIX instruction and transmits an IOP4 pulse which is received by the 34D Oscilloscope Display at pin P of connector BOD2 (sheet 2, C1). The W103 Device Selector Pulse Amplifier (AR AS) generates a 100-ns pulse (IOT 054) which, in its positive-going transition, enables the EF DCD gate in the R302 at connector BOA29 (sheet 2, C2). This triggers the input to the delay and causes its output to change from a ground level (0V) to −3V for 1 μs. When the output returns to ground, it is applied to and half-enables the three DCD gates controlling the high-, medium-, and low-intensity delay circuits. The level of brightness intensity is dependent upon the output of the two R202 Brightness Register Flip-Flops at connector BOA26 (sheet 1, B5). By way of example, the low brightness delay (sheet 2, C5) will operate only when the outputs from BR0 and BR1 are 0 and 1, respectively. When this occurs, the requirements for the DEJH diode gate (sheet 2, D4) are satisfied and the −3V level at inputs D and E is inverted by the JH gate to produce a ground level. This ground level is applied to the EF DCD gate (sheet 2, C4) and, when combined with the IOT 054 positive-going pulse, enables that gate. The DCD gate in turn triggers the JKM delay whose output is applied to the W681 Intensity Amplifier (INT AMP, sheet 2, C6) for 0.4 μs. An output of 25V, produced by the intensity amplifier, is connected to the oscilloscope through pin F of connector BOA32 (sheet 2, C7). The medium and high brightness outputs are produced in the same manner as the low brightness output.

The brightness register is loaded from the contents of memory buffer bits 10 and 11 through connector BOA4 (sheet 1, C5) as a DSB instruction is generated by the PDP-8. If the instruction code is 6075, memory buffer bits 10 and 11 contain a 0 (–3V) and a 1 (GRD) which appear at pins T and V, respectively, of connector BOA4. The 0 level (–3V) at pin T is first inverted by the JK diode gate (sheet 1, C5) which provides a ground level to the DE DCD gate (sheet 1, B5). When coupled with an IOT 074 negative-going pulse, the DE DCD gate will be enabled placing brightness register BR0 in the CLEAR state. The 0 level (–3V) at pin T is also present at the level input to the KL DCD gate, but it only serves to inhibit the gate.

The 1 level (GRD) at pin V is inverted by the LM gate (sheet 1, C5) producing a –3V level output which inhibits the NP DCD gate (sheet 1, C5). The 1 level (GRD) at pin V half enables the UV DCD gate. An IOT 074 pulse fulfills the DCD gate, setting brightness register BR1 to the 1 state. (The two diode gates in R107 at connector BOA25 (sheet 1, B5) permit collector-triggering of the brightness register flip-flops by a power clear pulse.)

3.2.4 Light Pen Operation - A photomultiplier light pen may be used with the 34D to communicate with a computer program. Basically, the light pen detects a point of light on the CRT and supplies it as a negative voltage level to the display control circuits through pin V of connector BOA32 (sheet 1, D8). Because this signal is not a standard DEC level, it is buffered by an emitter follower in module W681 at connector BOA31 (sheet 1, D7). This buffering provides impedance and amplitude characteristics required for DEC logic operation. Pin R of the diode gate in module R111 at connector BOA27 (sheet 1, D6) receives the buffered signal and, together with the –3V light pen strobe at pin S is inverted by the transistor at pin U. This inverted signal collector triggers the light pen flag flip-flop (sheet 1, C5) setting it to the ONE state. The light pen strobe is generated by the W681 Intensity Amplifier at connector BOA31 (sheet 2, C6). The outputs of the 0.4, 0.8, and 3 μs delays are OR-combined so that the activation of any one produces a strobe pulse of the same duration as the intensify signal that is transmitted to the oscilloscope.

The –3V output of the light pen flag flip-flop is inverted by the R111 at connector BOA27 (sheet 1, C6) and activated the interrupt line (pin M of BOA6, sheet 1, C7).

A ONE on the light pen flag flip-flop also half-enables the skip command input gate (sheet 1, pin E, C6). The requirements for a skip are completed when bit 9 of the memory buffer register contains a ZERO (pin D) and when an IOT 071 signal is generated (pin F). The diode gate connected to the three conditions acts as a NAND gate driving an inverter. Thus when all three inputs are ONES, the output at pin H is at a GND level. This GND level is brought out to pin K of connector BOA6 (sheet 1, C6) to initiate the skip instruction.

The light pen flag flip-flop can be cleared by a power-clear pulse or by the combination of an IOT 072 pulse and bit 9 of the memory buffer in the ZERO state. The IOT 072 pulse is generated by the AK AL power amplifier in the W103 Device Selector at connector BOA12/BOB12 (sheet 1, B3). It is applied as a ground level to the UV DCD gate in module R203 at connector BOA24 (sheet 1, D5). Bit 9 of the memory buffer at pin S of connector BOA4 is a −3V level which is inverted and applied to the UV DCD gate. With pins U and V qualified, the DCD gate is enabled and clears the light pen flag flip-flop.

4 INTERFACE

This section illustrates the interface connections and signals between the PDP-8 and the PDP-8/S and the 34D Oscilloscope Display Unit. Figures 4-1 and 4-2 show the interface between the PDP-8 and the 34D. Figures 4-3 through 4-5 illustrate the interface connections between the PDP-8/S and 34D logic control. Figure 4-6 indicates the connections between the 34D logic and the oscilloscope.

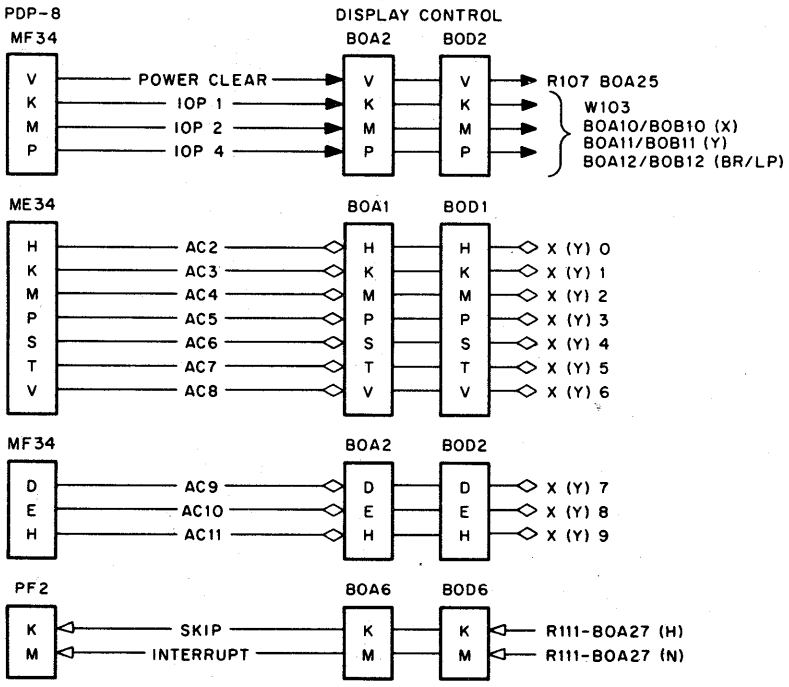


Figure 4-1 PDP-8 to 34D Control Interface, X/Y Address Data and Function Control Signals

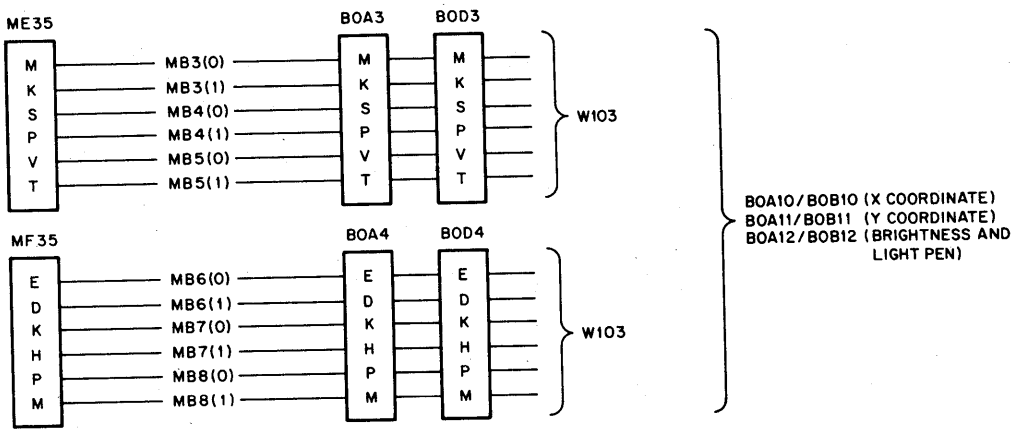


Figure 4-2 PDP-8 to 34D Control Interface, X and Y Coordinate Address and Brightness and Light Pen Address

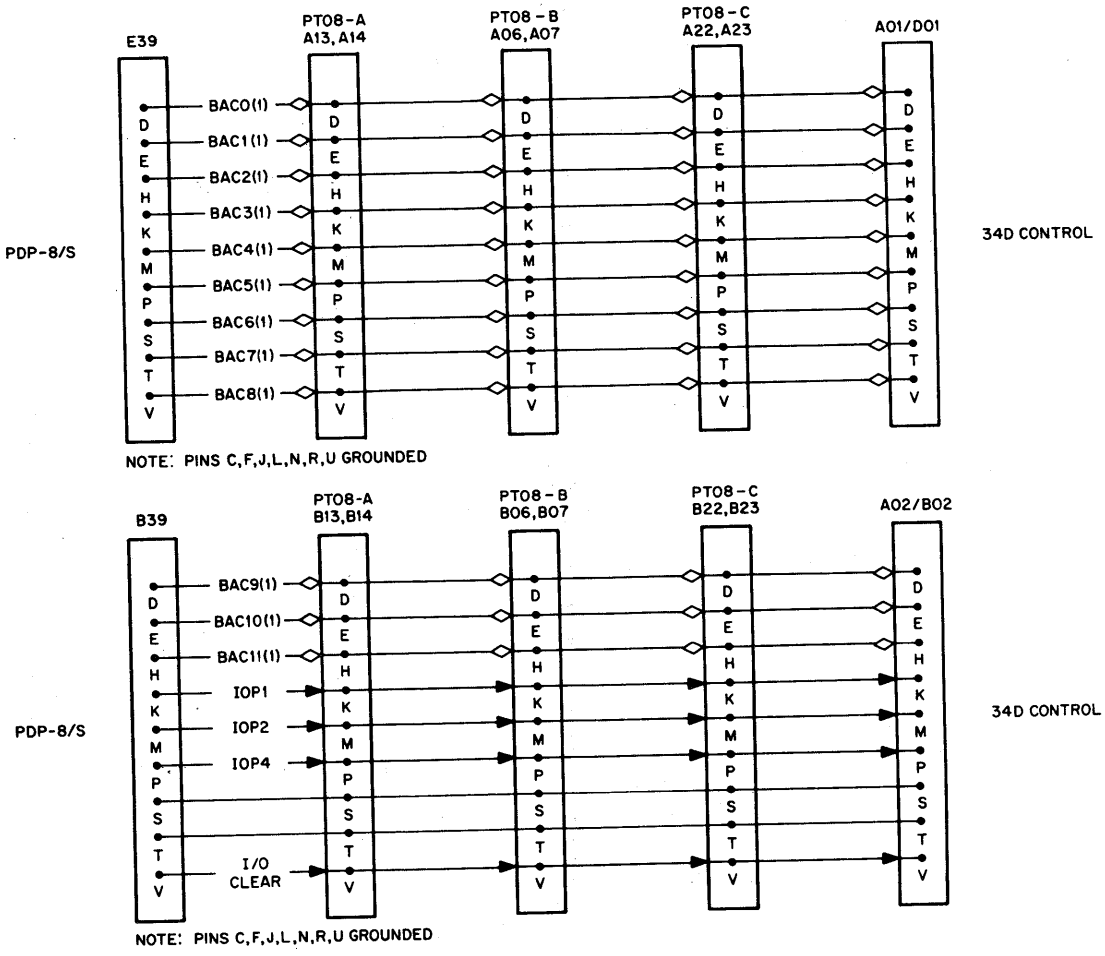


Figure 4-3 PDP-8/S to 34D Control Logic Interface

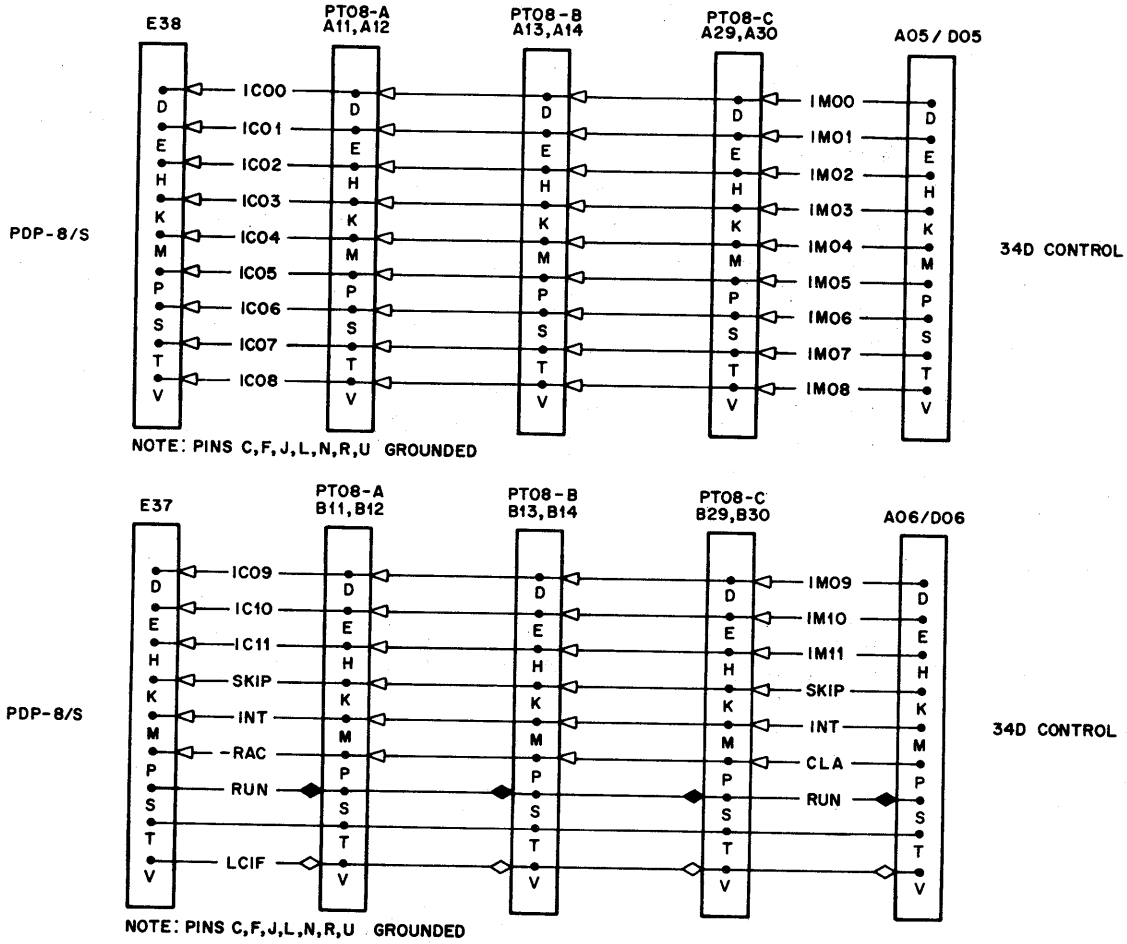


Figure 4-4 PDP-8/S to 34D Control Logic Interface

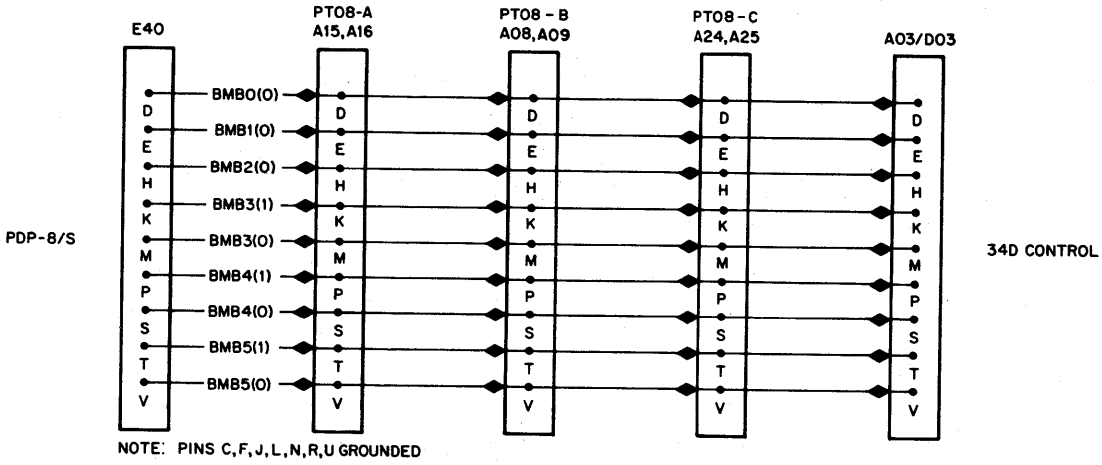


Figure 4-5 PDP-8/S Control Interface, Brightness, Light Pen, and X and Y Coordinate Control Address

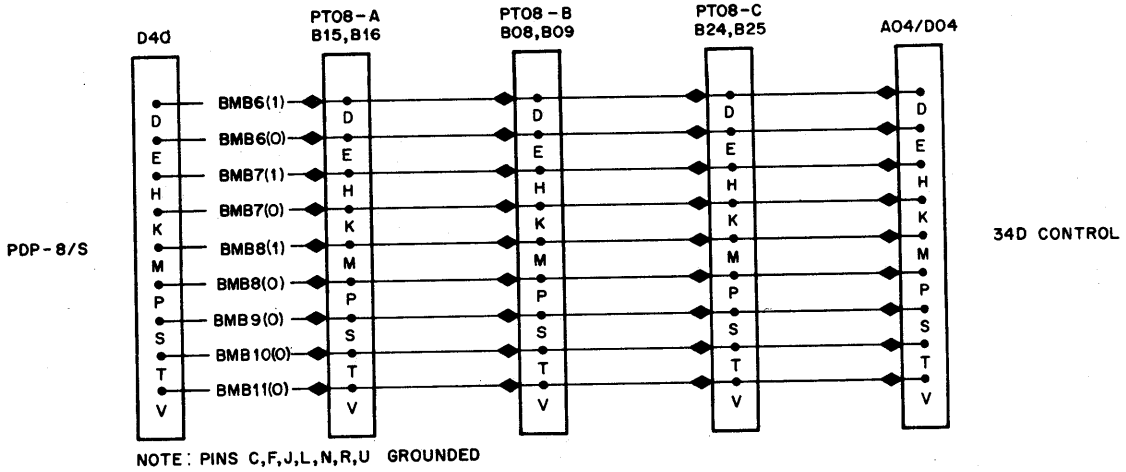


Figure 4-5 PDP-8/S Control Interface, Brightness, Light Pen, and X and Y Coordinate Control Address (continued)

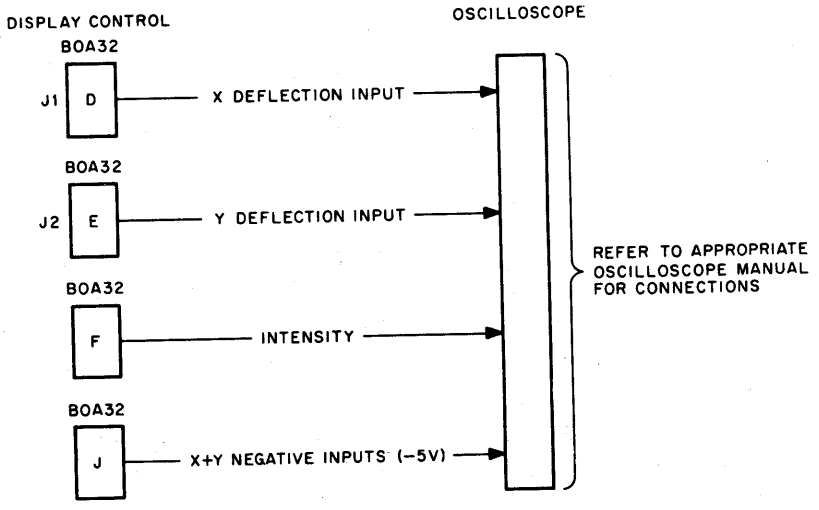


Figure 4-6 34D Control to Oscilloscope Interface

5. POWER SUPPLY

A DEC Type 779 Power Supply that is provided with the display control logic generates the three voltage levels (+10, −15, and −30 Vdc) required for operation of the display and its logic.

Section 8 of this document contains the schematic of the power supply DEC Drawing Number R5-B-779). Detailed information on the operational characteristics of this power supply is provided in the DEC Systems Modules Catalog (C-100).

6. MAINTENANCE

6.1 Preventive Maintenance

The general preventive maintenance procedures in the PDP-8 Maintenance Manual (DEC Doc. F-87) also apply to the display control logic.

6.1.1 Power Supply Checks - Table 6-1 lists the output voltage checks required for the DEC Type 779 Power Supply used in this equipment. To perform the power supply output checks described in Table 6-1, use a multimeter to make the output voltage measurements with the normal load connected, and an oscilloscope to measure the peak-to-peak ripple content on all dc outputs of the supply. The +10V and −15V supplies are not adjustable; therefore, if any voltage or ripple content is not within specifications, consider the power supply defective and initiate troubleshooting procedures.

Table 6-1 Type 779 Power Supply Output Checks

Measurement Terminals at Power Supply Output	Nominal Output (Vdc)	Acceptable Output Range (V)	Maximum Output Current (amp)	Maximum Peak-to-Peak Output Ripple (V)
Orange (+) to Yellow (-)	+10	+9.6 to 11.0	7.5	1.0
Yellow (+) to Blue (-)	-15	-14.5 to 16.0	8.0	0.4
Red (+) to Yellow (-)	+15	+14.5 to 16.0	7.5	1.1
Yellow (+) to Green (-)	+15	+14.5 to 16.0	7.5	1.1

6.2 Oscilloscope Maintenance

For information on maintenance and troubleshooting procedures, refer to the documentation provided by the manufacturer of the oscilloscope. The basic 34D Oscilloscope Display Unit utilizes a Tektronix RM - 503 Oscilloscope; however, other models may be used.

7 INSTALLATION

7.1 Cabinet and Desk Top Configuration

When the oscilloscope is supplied as either part of a cabinet-mounted or desk top PDP-8 system configuration, it normally mounts in a standard 19-in. radio rack adjacent to the central processor.

The logic controls and power supply for the Type 34D Oscilloscope Display Unit are mounted in the same cabinet as the oscilloscope when supplied as part of a desk-top configuration. Otherwise the logic controls and power supply are normally mounted in the PDP-8 cabinet itself.

7.2 Environmental and Power Requirements

The environmental and power requirements for the 34D logic controls are as specified in the PDP-8 Maintenance Manual (DEC Doc. F-87). For the oscilloscope specifications, refer to the appropriate oscilloscope manufacturer's documentation supplied with the Type 34D Oscilloscope Display Unit.

8. ENGINEERING DRAWINGS

This section contains the following logic diagrams, wiring diagrams, and module schematics which are pertinent to the Type 34D Oscilloscope Display Unit:

BS-D34D-0-2	Logic Diagrams
UML-D-34D-0-3	Utilization Module List
WD-D-34D-0-4	PDP-8 Options BOA-BOD
A601 A704 R107 R111 R202 R203 R302 W103 W681	Module Schematics

CODE BS | DRWG. NO. D-34D-0-2 | REV. LTR.

BOA32 J2

-10V REF
+10V REF

A6Ø1 BOB2Ø
A6Ø1 BOB21
A6Ø1 BOB22
A6Ø1 BOB23

R2Ø3-BOB16 (Y0, Y1, Y2)
R2Ø3-BOB17 (Y3, Y4, Y5)
R2Ø3-BOB18 (Y6, Y7, Y8)
R2Ø3-BOA24 (Y9)

BOD1
BOA1

AC2(I) AC3(I) AC4(I) AC5(I) AC6(I) AC7(I) AC8(I) AC9(I) AC1Ø(I) AC11(I)

BOD2
BOA2

BOA 2 BOD 2

IOP1 IOP2 IOP4

PA AD AE IOT Ø61
PA AK AL IOT Ø62
PA AR AS IOT Ø64

BOA 3 BOD 3

MB3(Ø) MB3(1) MB4(Ø) MB4(1) MB5(Ø) MB5(1) MB6(Ø) MB6(1) MB7(Ø) MB7(1) MB8(Ø) MB8(1)

BE BF BH BJ BK BL BM BN BP BR BS BT BU BV

BOA 4 BOD 4

W103 BOA11 BOB11

BOA 2 BOD 2

IOP1 IOP2 IOP4

PA AD AE AF IOT Ø71
PA AK AL IOT Ø72 CLR FLAG
PA AR AS IOT Ø74

BOA 3 BOD 3

MB3(Ø) MB3(1) MB4(Ø) MB4(1) MB5(Ø) MB5(1) MB6(Ø) MB6(1) MB7(Ø) MB7(1) MB8(Ø) MB8(1)

BE BF BH BJ BK BL BM BN BP BR BS BT BU BV

BOA 4 BOD 4

W103 BOA12 BOB12

RIØ7 BOA25
R2Ø2 BOA26 (BRØ, BR1)
RIØ7 BOA25

BOA4
BOD4

MBIØ(I)

RIØ7 BOA25
R2Ø3 BOA24

BOD BOA 2 2 PWR CLR

BOD BOA 4 4 MB9(Ø)

MB11(I) MB9(Ø)

SKIP INTERRUPT
BOD6 - WØ21
BOA6 - WØ21

RIII BOA27

IOT 071

LIGHT PEN STROBE

W681 BOA31

BOA32 LIGHT PEN OUTPUT

NOTE
1 CONNECTORS BOA1 THRU BOA4 & BOD1 THRU BOD4 ARE WØ21

REVISIONS	REV. LTR.	ECO. NO.	DATE	ENG

DRAWN R WATSON	DATE 4-12-65	
CHECKED	DATE 4/27/65	
ENG	DATE	
PROJ ENG	DATE	
PROD	DATE	

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

ASSY NO

SHEET 1 OF 2

TITLE DISPLAY

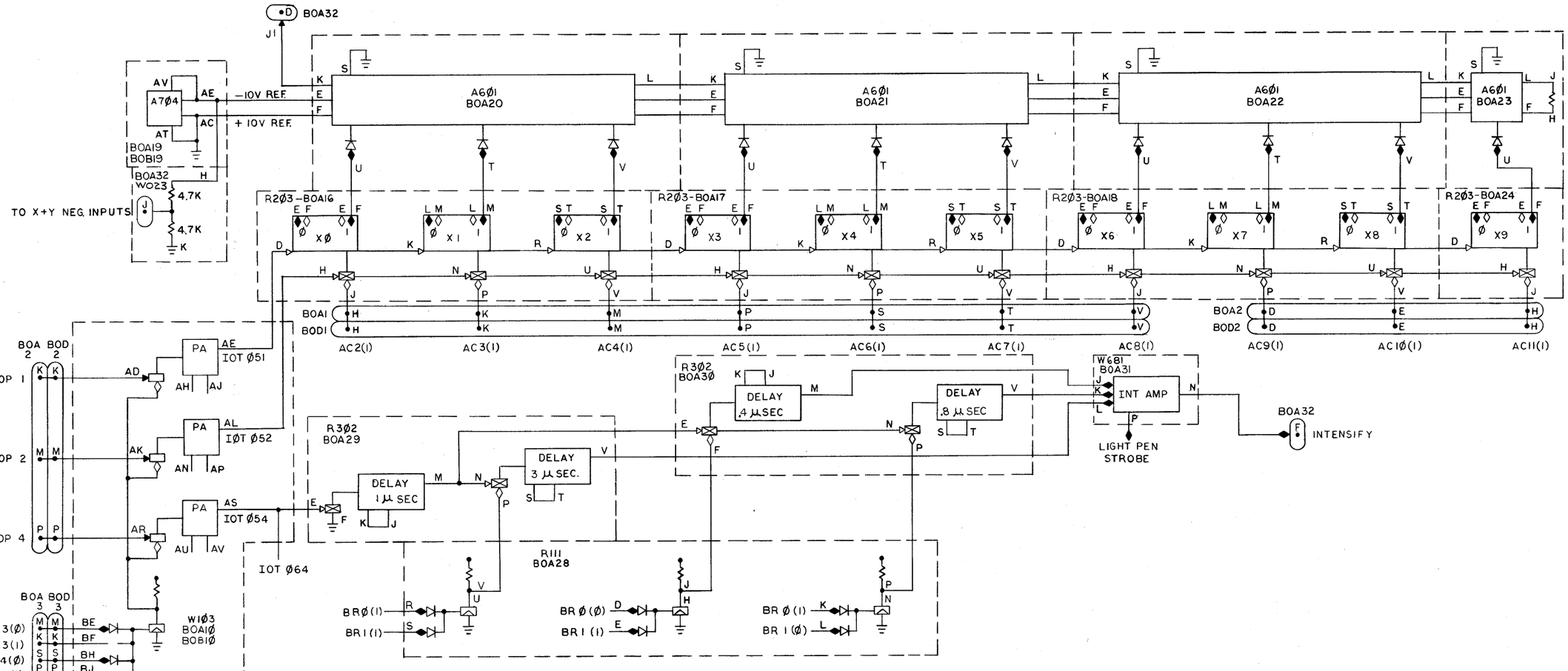
FOR

CODE BS | DRWG. NO. D-34D-0-2 | REV. LTR.

DIST.

BKE-2

CODE BS | DRWG. NO. D-34D-0-2 | REV. LTR.



NOTE
1 CONNECTORS BOA1 THRU BOA4 & BOD1 THRU BOD4 ARE WØ21

REVISIONS	REV. LTR.	ECO. NO.	DATE	ENG

DRAWN R WATSON	DATE 4-9-65	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHECKED	DATE 9/7/65	
ENG	DATE	
PROJ ENG	DATE	
PROD	DATE	

TITLE DISPLAY
FOR
ASSY NO
CODE BS | DRWG. NO. D-34D-0-2 | REV. LTR.
SHEET 2 OF 2 | DIST.

BKE-2

CODE UML | DRWG. NO. D-34D-0-3 | REV. LTR. J

Slot	BOA	BOB	BOC	BOD
1	W021 IN-OUT CONNECTOR AC 0(1) TO AC 8(1)	* PLOTTER CONNECTOR	R201 * PLTR FLAG	W021 IN-OUT CONNECTOR AC 0(1) TO AC 8(1)
2	W021 IN-OUT CONNECTOR AC 9(1) TO AC 11(1) IOP 1 TO IOP 4 T1 & T2 PWR. CLR.	W600 * PEN RIGHT / PEN LEFT / DRUM UP	W600 * DRUM DOWN / PEN UP / PEN DOWN	W021 IN-OUT CONNECTOR AC 9(1) TO AC 11(1) IOP 1 TO IOP 4 T1 & T2 PWR CLR
3	W021 IN-OUT CONNECTOR MB 0(1) TO MB 5(1)	R203 * PEN RIGHT / PEN LEFT / DRUM UP	R203 * DRUM DOWN / PEN UP / PEN DOWN	W021 IN-OUT CONNECTOR MB 0(1) TO MB 5(1)
4	W021 IN-OUT CONNECTOR MB 6(1) TO MB 11(1)	R111 * PEN UP / IOT 504 or IOT 514 / INHIBIT DEVICE SELECTOR	R603 * CLEAR PR & PL & DU & DD / CLEAR PU & PD	W021 IN-OUT CONNECTOR MB 6(1) TO MB 11(1)
5	W021 IN-OUT CONNECTOR IM 0 TO IM 8	R302 * SET PLTR FLAG / SET PLTR	R302 * CLEAR PLTR FLAG / CLEAR PLTR FLAG	W021 IN-OUT CONNECTOR IM 0 TO IM 8
6	W021 IN-OUT CONNECTOR IM 9 TO IM 11 SKIP INTERRUPT AC CLEAR RUN(1)	R107 * X=0 / PWR CLR / PWR CLR / IOT 5X1 / IOT 5X2	R111 * SKIP / SKIP / INTERRUPT	W021 IN-OUT CONNECTOR IM 9 TO IM 11 SKIP INTERRUPT AC CLEAR RUN(1)
7	W103 * DEVICE SELECTOR IOT 5X (PLOTTER)	W103 * DEVICE SELECTOR IOT 5X (PLOTTER)	W023 ◇ CARD READER CONN	W023 ◇ CARD READER CONN
8	W103 △ DEVICE SELECTOR IOT 01 (READER)	W103 △ DEVICE SELECTOR IOT 01 (READER)	W701 ◇ SPR / SMR / SRR	W701 ◇ CLM 12 / CLM 11 / CLM 10 / CLM 1 / CLM 2 / CLM 3
9	W103 □ DEVICE SELECTOR IOT 02 (PUNCH)	W103 □ DEVICE SELECTOR IOT 02 (PUNCH)	W501 ◇ COLUMN CLOCK	W701 ◇ CLM 4 / CLM 5 / CLM 6 / CLM 7 / CLM 8 / CLM 9
10	W103 ☆ DEVICE SELECTOR IOT 05 (DISPLAY)	W103 ☆ DEVICE SELECTOR IOT 05 (DISPLAY)	R107 ◇ SRR / PWR CLR / 0 → CARD DONE / 0 → DATA READY / CLMB 12 / CLMB 11 / CLMB 10	R123 ◇ IM 0 / IM 1 / IM 2 / IM 3 / IM 4 / IM 5
11	W103 ☆ DEVICE SELECTOR IOT 06 (DISPLAY)	W103 ☆ DEVICE SELECTOR IOT 06 (DISPLAY)	R113 ◇ ESCAPE MAGNET / ESCAPE MAGNET / 1 → DATA READY / ALPHA BIT 6 / ALPHA BIT 7	R123 ◇ IM 6 / IM 7 / IM 8 / IM 9 / IM 10 / IM 11
12	W103 ☆ DEVICE SELECTOR IOT 07 (DISPLAY)	W103 ☆ DEVICE SELECTOR IOT 07 (DISPLAY)	R202 ◇ CR RUN / REGISTER	R123 ◇ IM 6 / IM 7 / IM 8 / IM 9 / IM 10 / IM 11
13	W103 ◇ DEVICE SELECTOR IOT 63 (CARD READER)	W103 ◇ DEVICE SELECTOR IOT 63 (CARD READER)	R202 ◇ CARD DONE / DATA READY	R123 ◇ CARD DONE SKIP / CARD DONE INTERRUPT / DATA READY SKIP / DATA READY INTERRUPT / READER READY SKIP / 1 → CR RUN
14	W103 ◇ DEVICE SELECTOR IOT 67 (CARD READER)	W103 ◇ DEVICE SELECTOR IOT 67 (CARD READER)	R111 □ FEED SWITCH / FEED SWITCH	W501 ◇ B SPR
15	W103 SPARE DEVICE SELECTOR	W103 SPARE DEVICE SELECTOR	R203 □ PB_0 / PB_1 / PB_2	
16	R203 ☆ X_0 / X_1 / X_2	R203 ☆ Y_0 / Y_1 / Y_2	R203 □ PB_3 / PB_4 / PB_5	
17	R203 ☆ X_3 / X_4 / X_5	R203 ☆ Y_3 / Y_4 / Y_5	R203 □ PB_6 / PB_7	
18	R203 ☆ X_6 / X_7 / X_8	R203 ☆ Y_6 / Y_7 / Y_8	R111 △□ SKIP / INTERRUPT / PUNCH ACTIVE	
19	A704 ☆ REF SUPPLY	A704 ☆ REF SUPPLY	R302 □ PUNCH DONE	
20	A601 ☆ D-A CONV. 3 BITS X_0 X_2	A601 ☆ D-A CONV. 3 BITS Y_0 Y_2	W520 □ START PUNCH	
21	A601 ☆ D-A CONV. 3 BITS X_3 X_5	A601 ☆ D-A CONV. 3 BITS Y_3 Y_5	R202 □ PUNCH ACTIVE / PUNCH FLAG	
22	A601 ☆ D-A CONV. 3 BITS X_6 X_8	A601 ☆ D-A CONV. 3 BITS Y_6 Y_8	R107 □ PWR CLR / DLY / PUNCH DONE / HOLE 2 & 3 ENABLE / HOLE 4 & 5 ENABLE / FEED & HOLE 6 ENB / HOLE 7 & 8 ENABLE	
23	A601 ☆ D-A CONV. 3 BITS X_9	A601 ☆ D-A CONV. 3 BITS Y_9	W040 □ HOLE 8 / HOLE 7	R111 α STROBE / STROBE / FEED CHECK
24	R203 ☆ X_9 / Y_9 / L.P. FLAG	R123 △ PWR CLR / PWR CLR / SKIP / INTERRUPT / IM_4 / IM_5	W040 □ HOLE 8 / HOLE 7	R603 α STROBE / FEED CHECK / INDEX
25	R107 ☆ PWR CLR / PWR CLR / MB 10(1) / MB 11(1) / PWR CLR / MB 9(0)	R123 △ IM_6 / IM_7 / IM_8 / IM_9 / IM_{10} / IM_{11}	W040 □ HOLE 6 / HOLE 5	R202 α ENABLE / POWER
26	R202 ☆ BR 0 / BR 1	R202 △ RDR RUN / RDR FLAG	W040 □ HOLE 6 / HOLE 5	R302 α STOP DELAY / CLOCK DELAY
27	R111 ☆ SKIP / INTERRUPT / I LP FLAG	R302 △ STROBE DELAY / STOP DELAY	W040 □ HOLE 4 / HOLE 3	G903 α ACCELERATOR
28	R111 ☆ BRIGHT 1 / BRIGHT 2 / BRIGHT 3	W501 △ START READER	W040 □ FEED HOLE / FEED HOLE	R401 α CLOCK
29	R302 ☆ SET UP DELAY / BRIGHT 3	R203 △ RD_0 / RD_1 / RD_2	W040 □ HOLE 4 / HOLE 3	R202 α A / B
30	R302 ☆ BRIGHT 1 / BRIGHT 2	R203 △ RD_3 / RD_4 / RD_5	W040 □ HOLE 2 / HOLE 1	R107 α A(0) / A(1) / B(0) / B(1) / POWER(1) / PWR CLR / $\overline{D2}$
31	W681 ☆ SCOPE INT / LIGHT PEN EMITTER FOLLOWER	R203 △ RD_6 / RD_7 / FEED STARTED	W040 □ HOLE 2 / HOLE 1	R111 α D1 / PC / RUN
32	☆ DISPLAY CONN.	△ READER CONN.	PUNCH CONN.	α PCO1 CONN

* INCREMENTAL PLOTTER TYPE 350B
☆ OSCILLOSCOPE DISPLAY TYPE 34D
△ HIGH SPEED READER TYPE 750C
□ HIGH SPEED PUNCH TYPE 75E
◇ CARD READER CR01C
α PC01 + △ (FROM △ REMOVE BO B27, BO B28)
+ □ (FROM □ REMOVE BO C24 26 29 31)

REV. LTR.	ECO NO.	DATE	ENG
J	183	10/11/67	[illegible]
H	176	[illegible]	[illegible]
F	108	[illegible]	[illegible]
E	94	[illegible]	[illegible]
D	83	[illegible]	[illegible]
C	61	5-18-66	[illegible]
B	53	3-11-66	[illegible]
A	33	12-14-65	[illegible]

REVISIONS

DRAWN RHWATSON DATE 4-23-65
CHECKED [illegible] DATE [illegible]
ENG [illegible] DATE [illegible]
PROJ ENG [illegible] DATE [illegible]
PROD [illegible] DATE

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

ASSY NO

TITLE UTILIZATION MODULE LIST

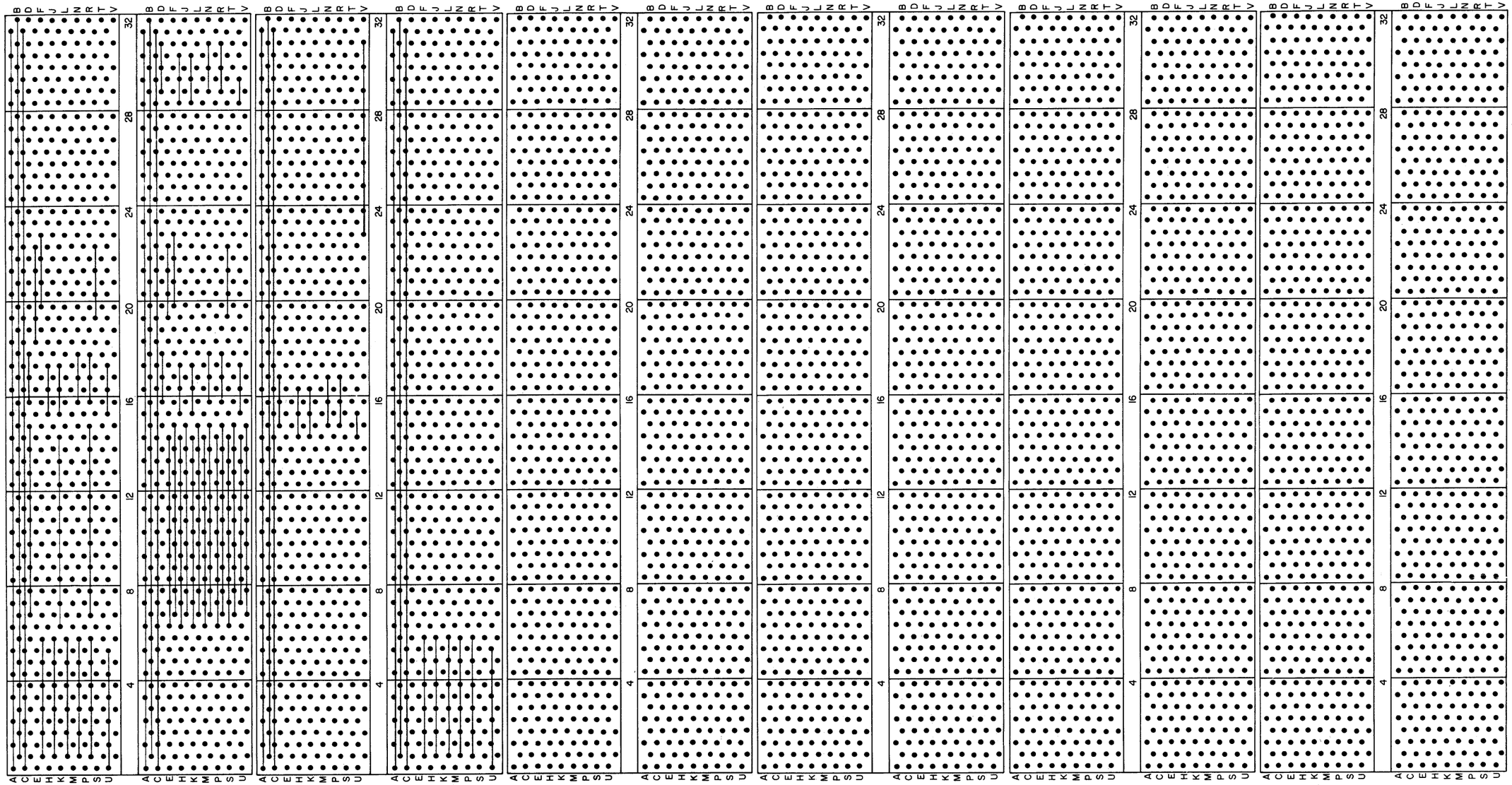
FOR

CODE UML | DRWG. NO. D-34D-0-3 | REV. LTR. J

SHEET 1 OF

DIST.

CODE	DRWG. NO.	REV. LTR.
WD	D-34D-0-4	



REV. LTR.	ECO. NO.	DATE	ENG

REVISIONS

DRAWN	RWATSON	DATE	4-22-65
CHECKED		DATE	4/27/65
ENG		DATE	
PROJ ENG		DATE	
PROD		DATE	

digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ASSY NO

SHEET 1 OF 1

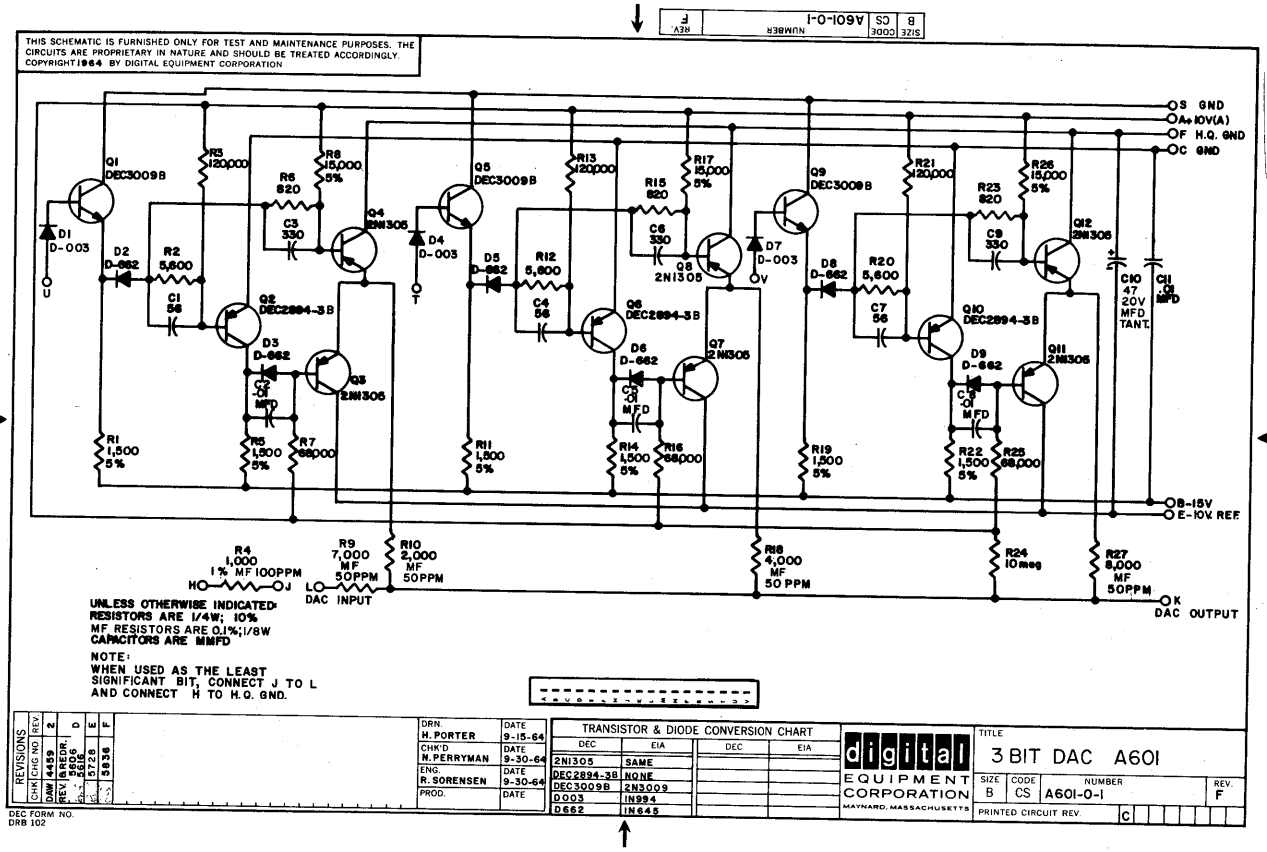
TITLE
PDP-8 OPTIONS
BOA – BOD

FOR

CODE	DRWG. NO.	REV. LTR.
WD	D-34D-0-4	

DIST.

BKE-2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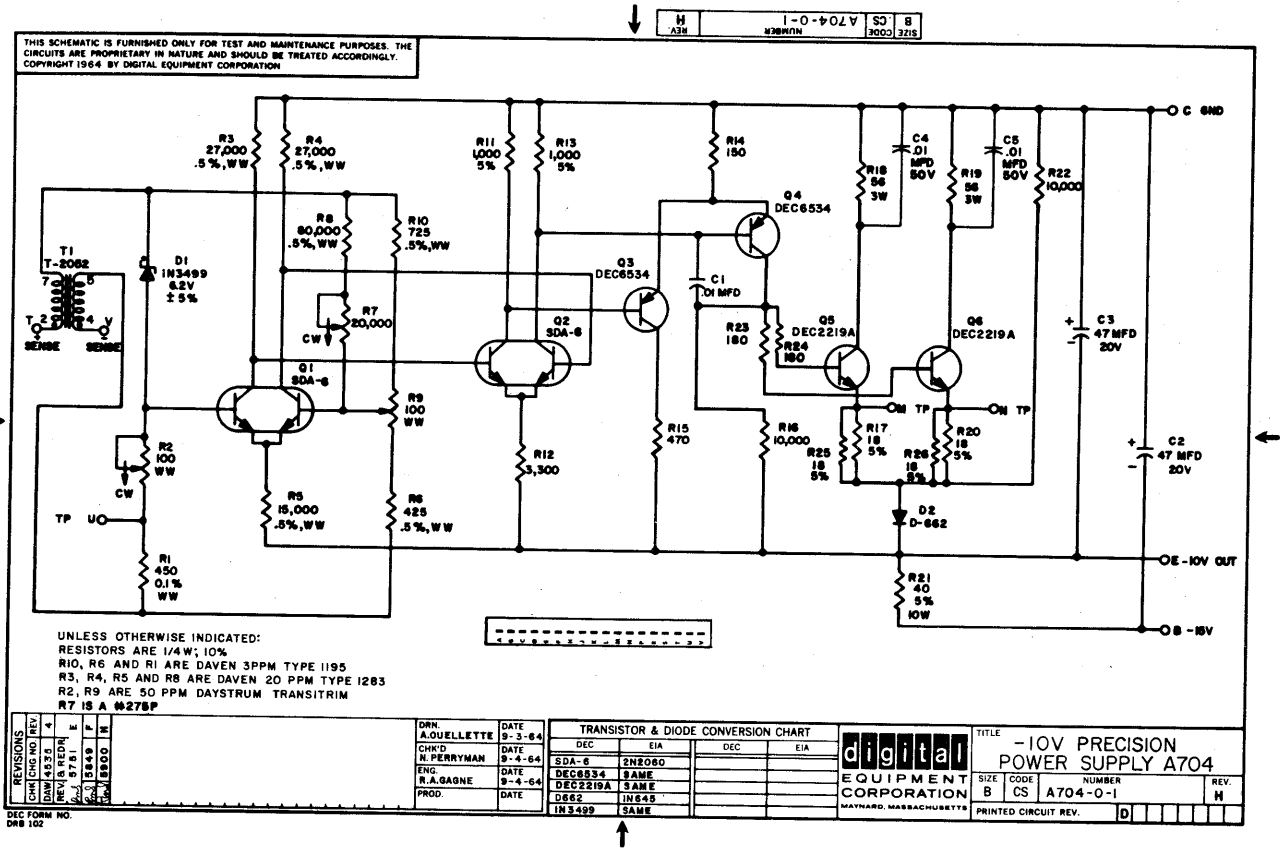
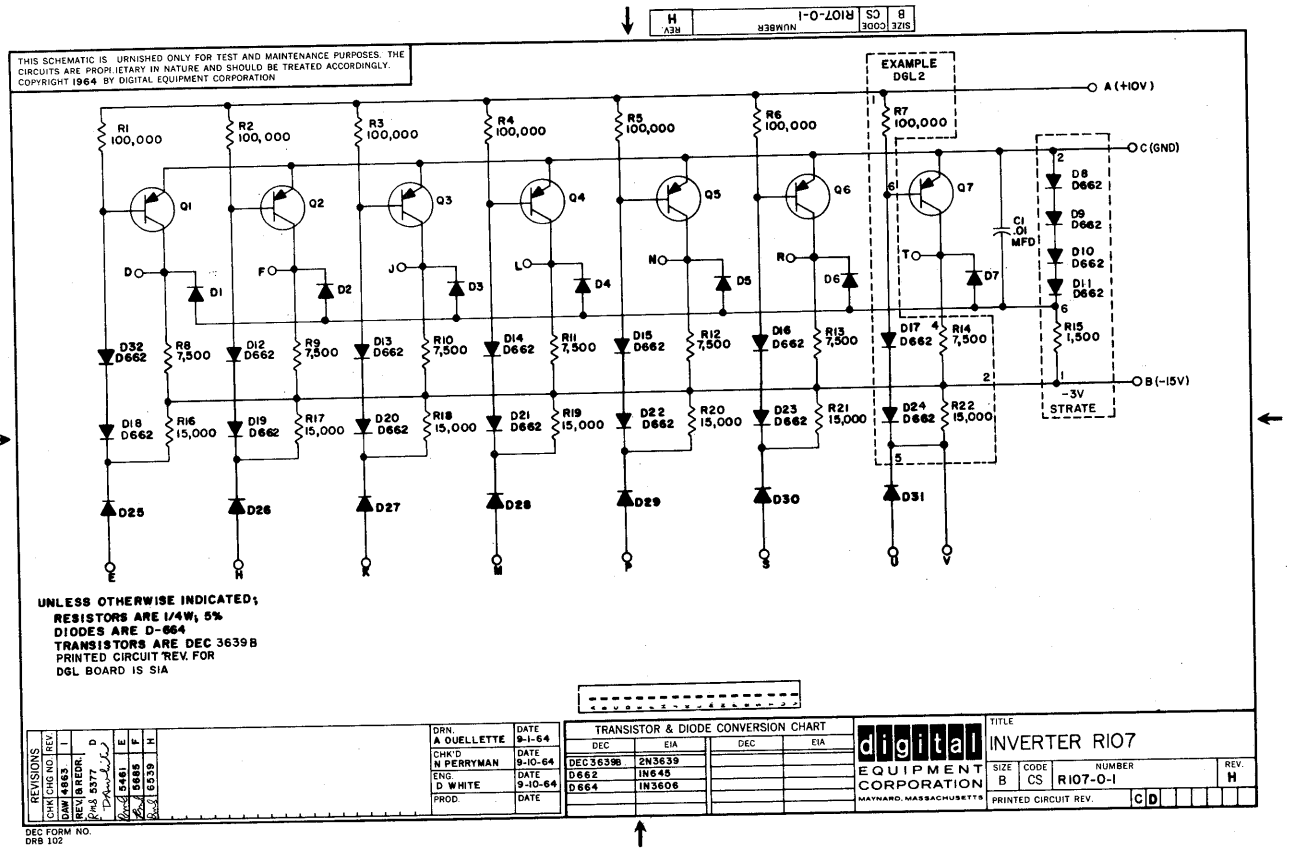
S GND
A+ 10V(A)
F H.Q. GND
C GND
B -15V
E -10V REF
K DAC OUTPUT
DAC INPUT
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
MF RESISTORS ARE 0.1%;1/8W
CAPACITORS ARE MMFD
NOTE:
WHEN USED AS THE LEAST SIGNIFICANT BIT, CONNECT J TO L AND CONNECT H TO H.Q. GND.
TRANSISTOR & DIODE CONVERSION CHART
2N1305 SAME
DEC2894-3B NONE
DEC3009B 2N3009
D003 IN914
D662 IN645
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
3 BIT DAC A601
A601-0-1
DEC FORM NO. DRB 102


THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY. COPYRIGHT 1964 BY DIGITAL EQUIPMENT CORPORATION
C GND
E -10V OUT
B -15V
SENSE
SENSE
TP
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
R10, R6 AND R1 ARE DAVEN 3PPM TYPE 1195
R3, R4, R5 AND R8 ARE DAVEN 20 PPM TYPE 1283
R2, R9 ARE 50 PPM DAYSTRUM TRANSITRIM
R7 IS A #275P
TRANSISTOR & DIODE CONVERSION CHART
SDA-6 2N2060
DEC6534 SAME
DEC2219A SAME
D662 IN645
IN3499 SAME
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
-10V PRECISION POWER SUPPLY A704
A704-0-1
DEC FORM NO. DRB 102



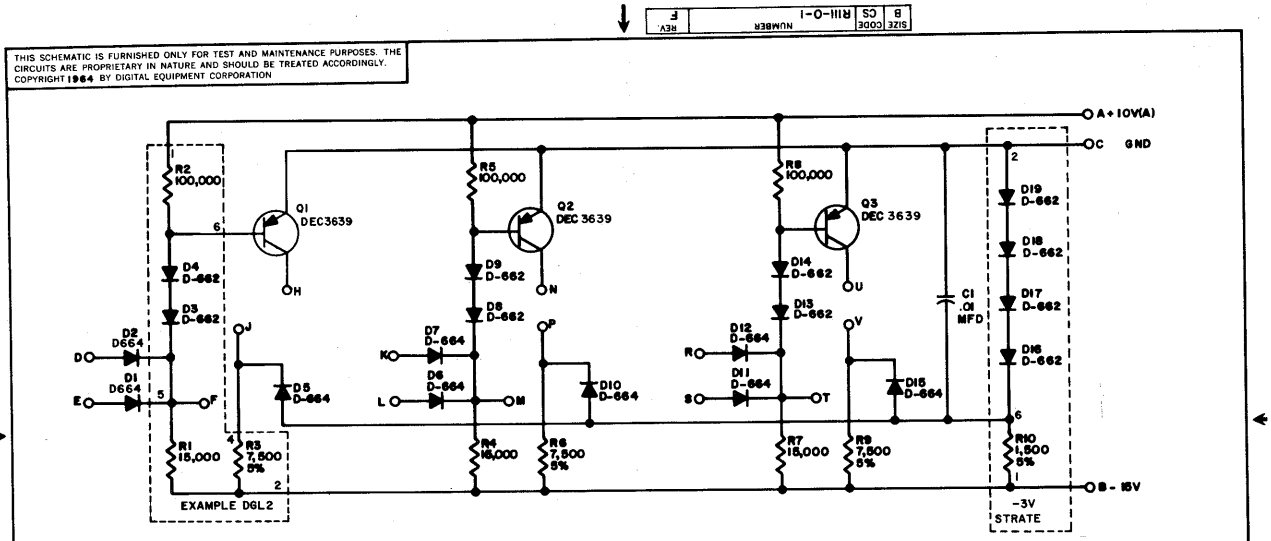
UNLESS OTHERWISE INDICATED;
RESISTORS ARE 1/4W, 5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639B
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIA

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC3639B	2N3639		
D662	IN645		
D664	IN3606		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: INVERTER RIO7
SIZE B | CODE CS | NUMBER RIO7-0-1 | REV. H
PRINTED CIRCUIT REV. C D

DEC FORM NO. DRB 102



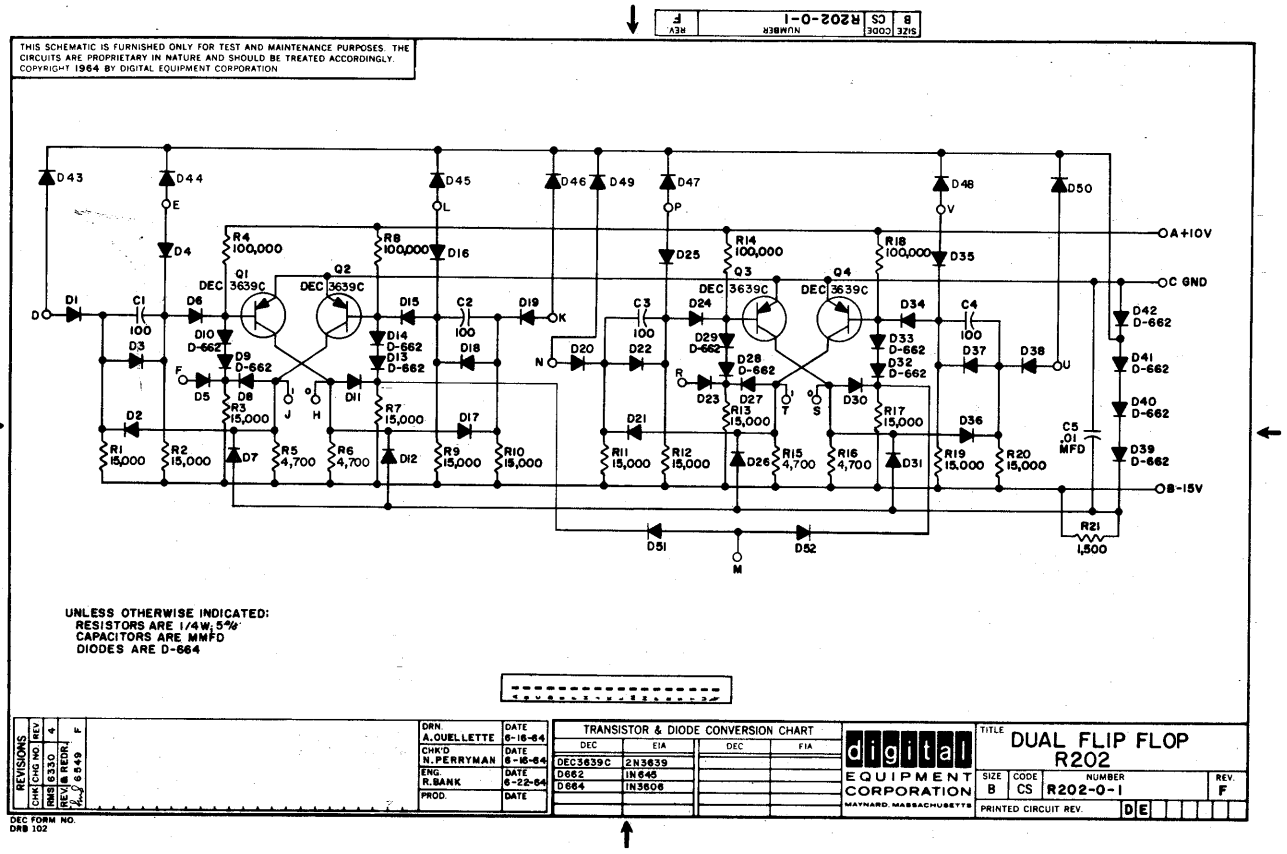
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIB

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC3639	2N3639		
D662	IN645		
D664	IN3606		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DIODE GATE RIII
SIZE B | CODE CS | NUMBER RIII-0-1 | REV. F
PRINTED CIRCUIT REV. D E F

DEC FORM NO. DRB 102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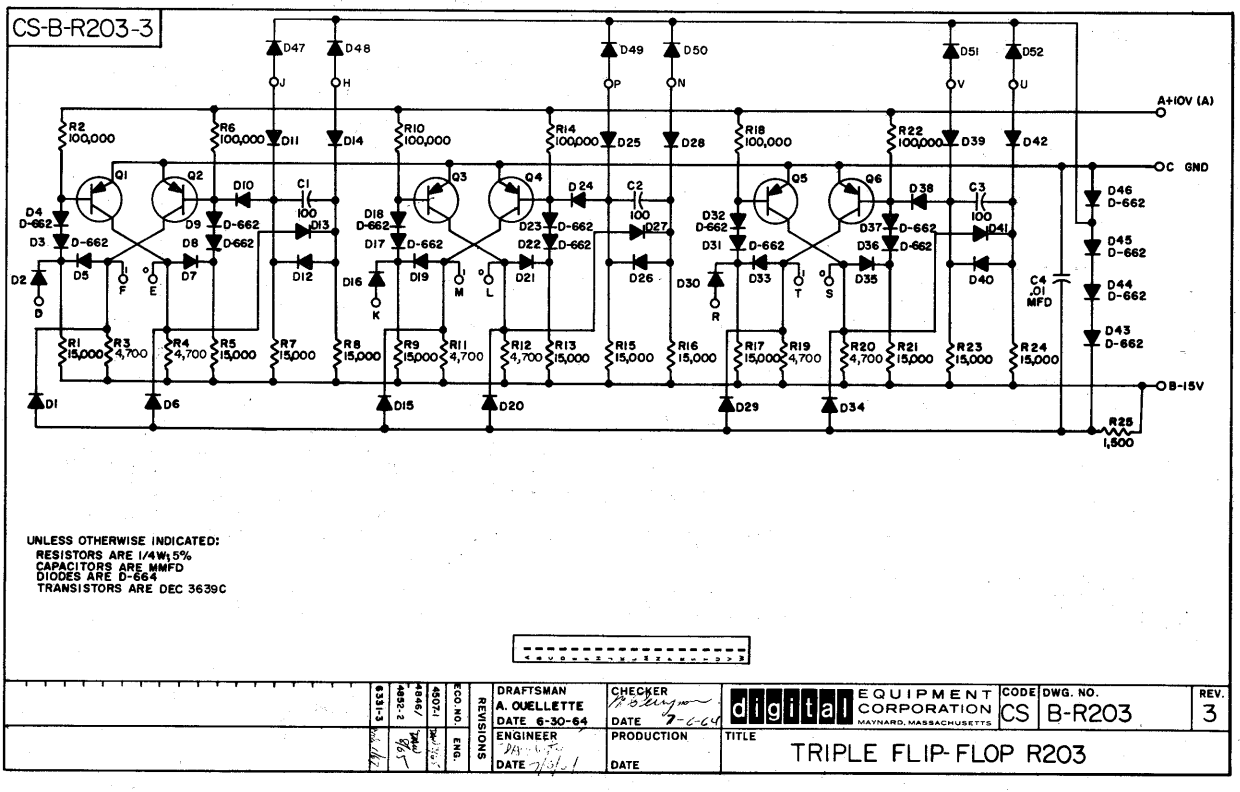
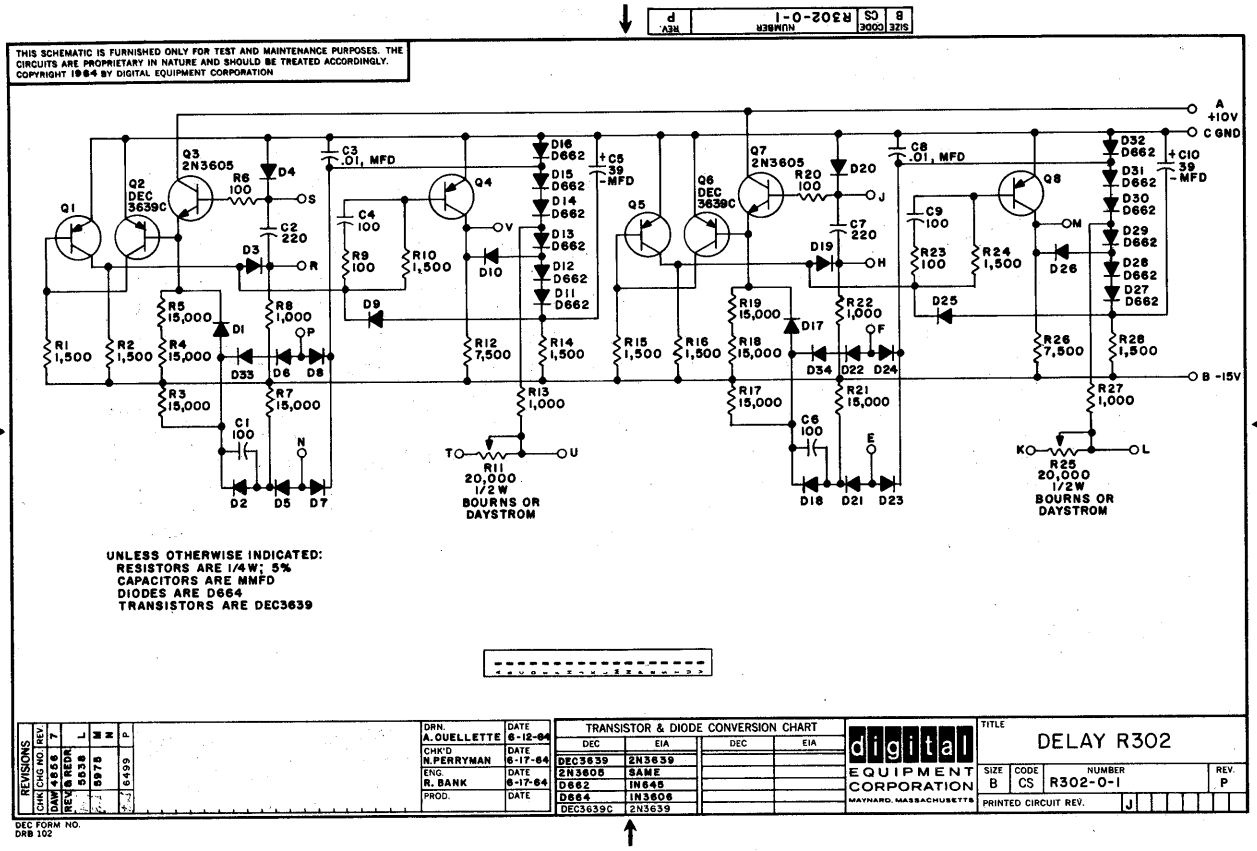
COPYRIGHT 1964 BY DIGITAL EQUIPMENT CORPORATION
SIZE B CODE CS NUMBER R202-0-1 REV F
A+10V
C GND
B-15V
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA
DEC3639C 2N3639
D662 IN645
D664 IN3606
DRN A.OUELLETTE 6-16-64
CHK'D N.PERRYMAN 6-16-64
ENG. R.BANK 6-22-64
PROD.
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE DUAL FLIP FLOP R202
SIZE B CODE CS NUMBER R202-0-1 REV. F
PRINTED CIRCUIT REV. DE
DEC FORM NO. DRB 102


CS-B-R203-3
A+10V (A)
C GND
B-15V
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639C
DRAFTSMAN A. OUELLETTE DATE 6-30-64
CHECKER DATE 7-6-64
ENGINEER DATE
PRODUCTION DATE
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CODE CS DWG. NO. B-R203 REV. 3
TITLE TRIPLE FLIP-FLOP R203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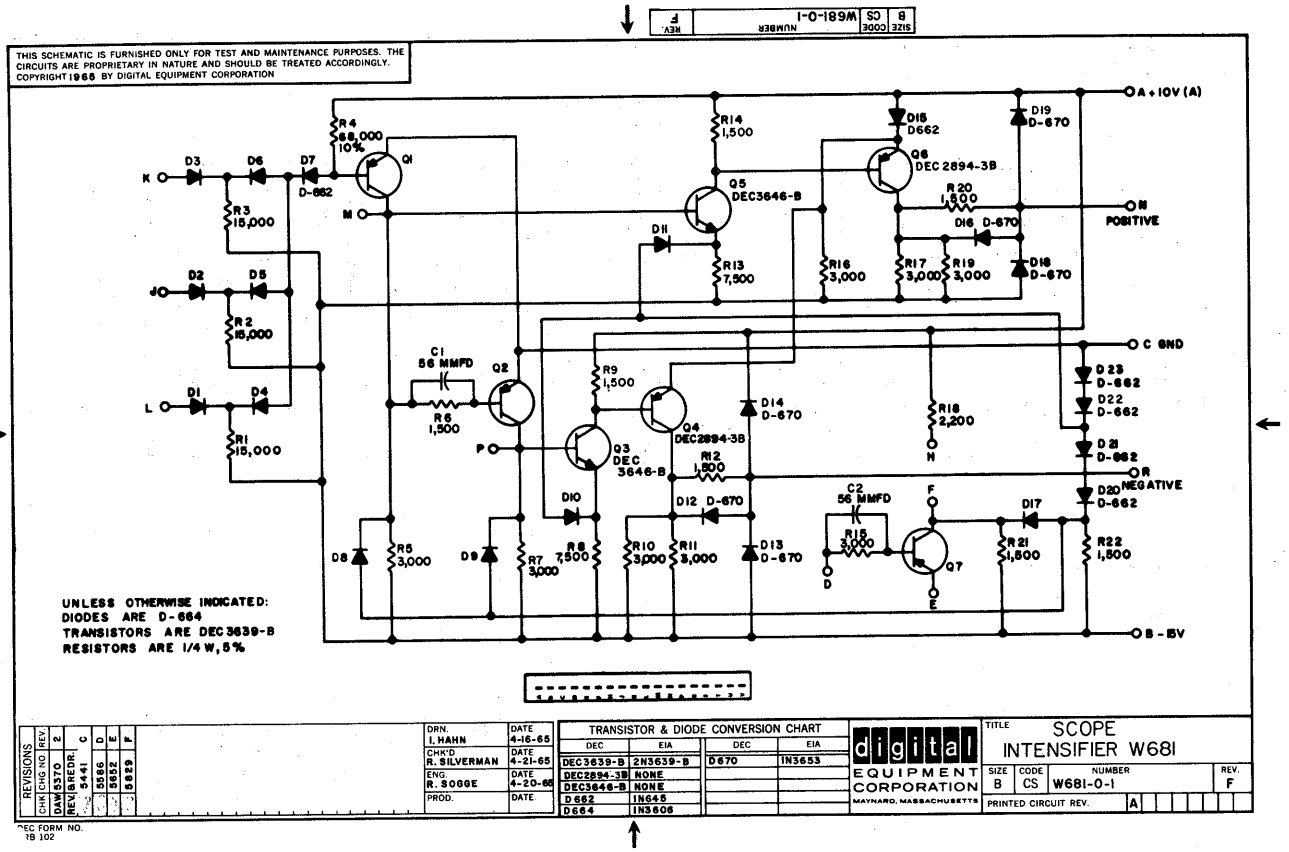
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D664
TRANSISTORS ARE DEC3639
R11 20,000 1/2W BOURNS OR DAYSTROM
R25 20,000 1/2W BOURNS OR DAYSTROM
A +10V
C GND
B -15V
TRANSISTOR & DIODE CONVERSION CHART
DEC3639 2N3639
2N3605 SAME
D662 IN645
D664 IN3606
DEC3639C 2N3639
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE DELAY R302
SIZE B CODE CS NUMBER R302-0-1 REV. P
PRINTED CIRCUIT REV. J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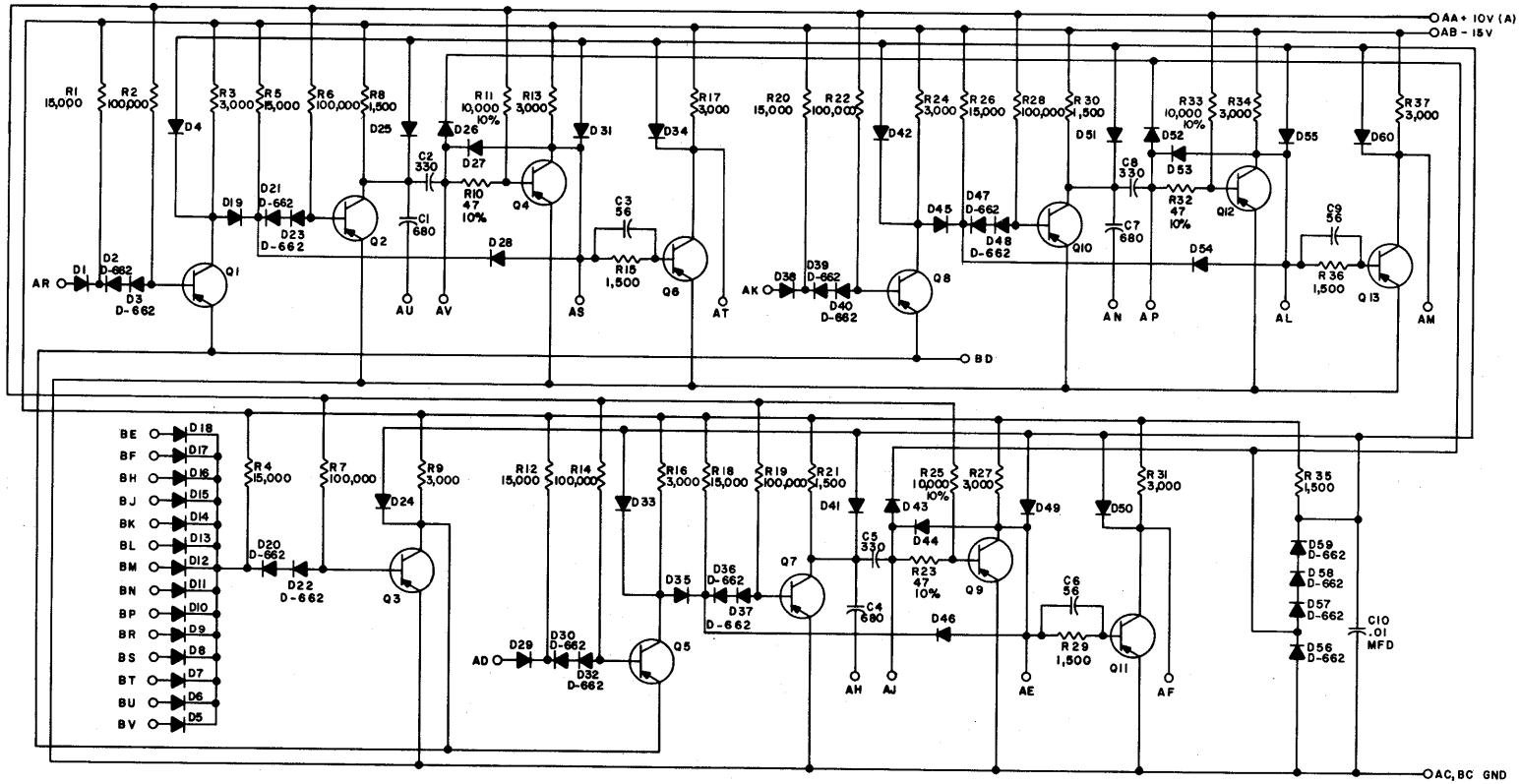
UNLESS OTHERWISE INDICATED:
DIODES ARE D-664
TRANSISTORS ARE DEC3639-B
RESISTORS ARE 1/4 W, 5%
A +10V (A)
C GND
B -15V
POSITIVE
NEGATIVE
TRANSISTOR & DIODE CONVERSION CHART
DEC3639-B 2N3639-B
DEC2894-3B NONE
DEC3646-B NONE
D662 IN645
D664 IN3606
D670 IN3653
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE SCOPE INTENSIFIER W681
SIZE B CODE CS NUMBER W681-0-1 REV. F
PRINTED CIRCUIT REV. A



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4 W, 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

REVISIONS			
CHK	CHG NO.	REV.	
DAW	4792	2	D
REV. & REDR.	6178		

DRN. I. HAHN	DATE 4-21-65	
CHK'D R. SILVERMAN	DATE 4-22-65	
ENG. R. SOGGE	DATE 4-22-65	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3639	2N3639		
D662	IN645		
D664	IN3606		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DEVICE SELECTOR W103

SIZE	CODE	NUMBER	REV.
C	CS	W103-0-1	D

PRINTED CIRCUIT REV. C

SIZE	CODE	NUMBER	REV.
C	CS	W103-0-1	D

DEC FORM NO. DRC 102