Digital Equipment Corporation
Maynard, Massachusetts

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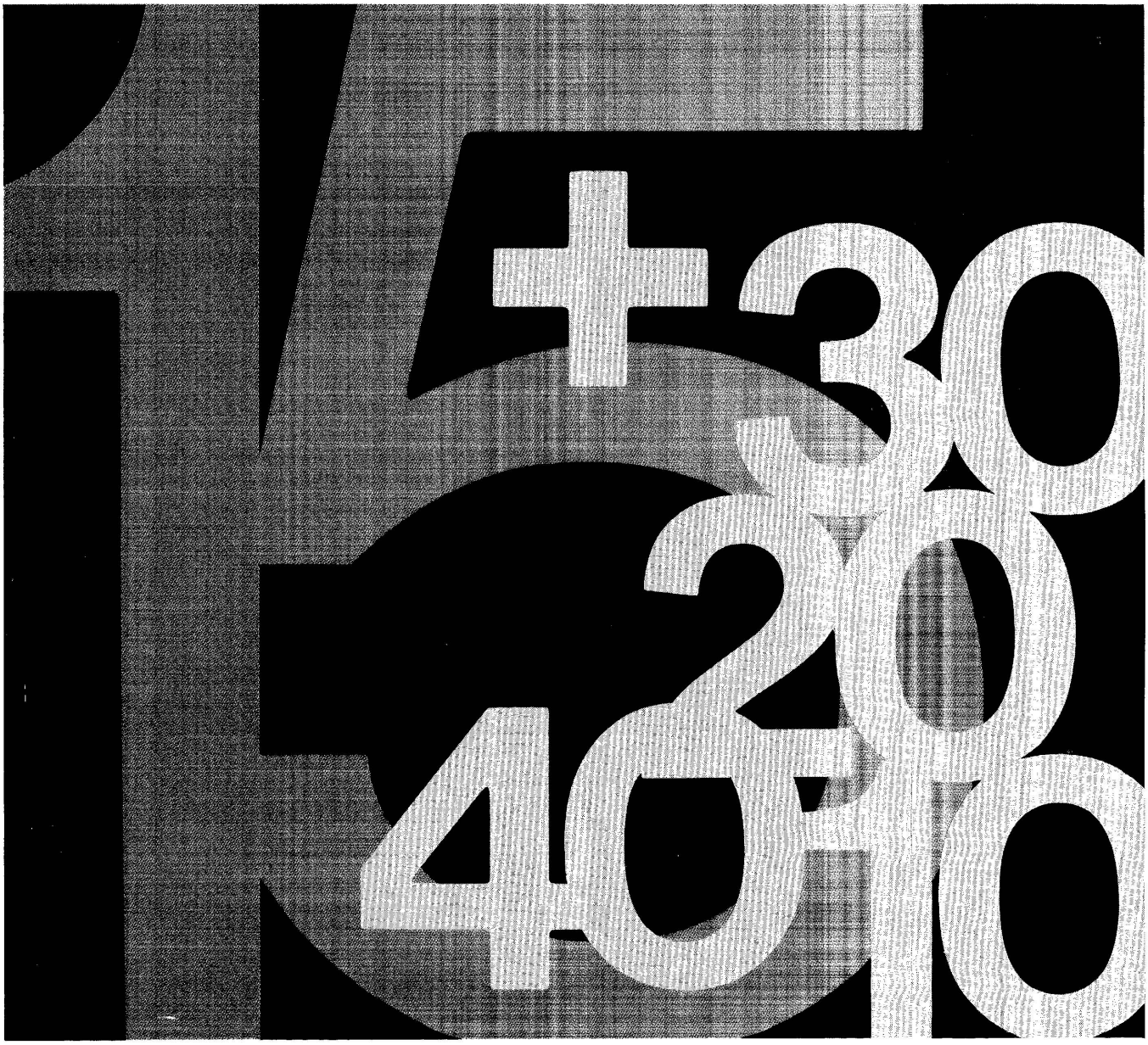
PDP-15 Systems
Maintenance Manual

Volume 1

MX15
Memory Bus Multiplexer



DEC-15-H2XB-D

PDP-15 SYSTEMS
MX15
MEMORY BUS MULTIPLEXER
MAINTENANCE MANUAL
VOLUME 1

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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CHAPTER 1
BASIC DESCRIPTION

1.1 DESCRIPTION AND PURPOSE

The MX15 Memory Bus Multiplexer option is designed for use with the PDP-15 computer system. The option adds three important capabilities to the PDP-15:

a. extended memory

b. direct memory access (DMA)

c. multiprocessor systems application

The option may include up to four MX15-A Memory Bus Multiplexers, with appropriate MM15XD memory banks, power supplies and equipment bays.

The MX15-A is a high-speed hybrid switch with three input ports and one output port that can establish one of three communication paths (see Figure 1-1) on a priority basis. Up to three memory data lines, each from a separate processor or DMA device, can be connected to 32K of core memory via the multiplexer. Logic within the MX15-A governs the granting of priorities for processor access to the multiplexer, thereby gaining access to the core memory. Port 1 has the highest priority, and port 3 has the lowest priority. Memory data line loading enables the PDP-15 processor to drive as many as four MX15-As. In turn, each MX15-A is capable of driving 32K of core memory. Thus, by using four MX15-As, core memory can be extended to 128K. Figures 1-2 through 1-4 illustrate three typical configurations emphasizing extended memory, direct memory access, and multiprocessor applications.

Figure 1-2 illustrates the configuration for an extended memory system; it also emphasizes direct memory access and simultaneous memory access features afforded by the MX15-A. The DMA device has direct access to any memory block, because the DMA device is connected to the highest priority port of each multiplexer. While the DMA device is accessing a specific memory block, the IPU or CPU of a KP15A equipped with the KT15 Memory Protect and Relocate option can access a different memory block via the two lower priority ports. The direct memory access capability of the MX15-A is illustrated in Figure 1-3. Any device with the proper control circuitry can gain access to an MM15 memory through one of the input ports of an MX15-A. Chapter 5 describes how to design a DMA interface. The KT15 memory relocation is required to jump blocks of memory, because user programs are restricted to 32K. Figure 1-4 illustrates a multiprocessor system, emphasizing the bank rotate feature of the MX15-A. The bank rotate feature alters bank address bits 03 and 04 to preserve contiguous addressing

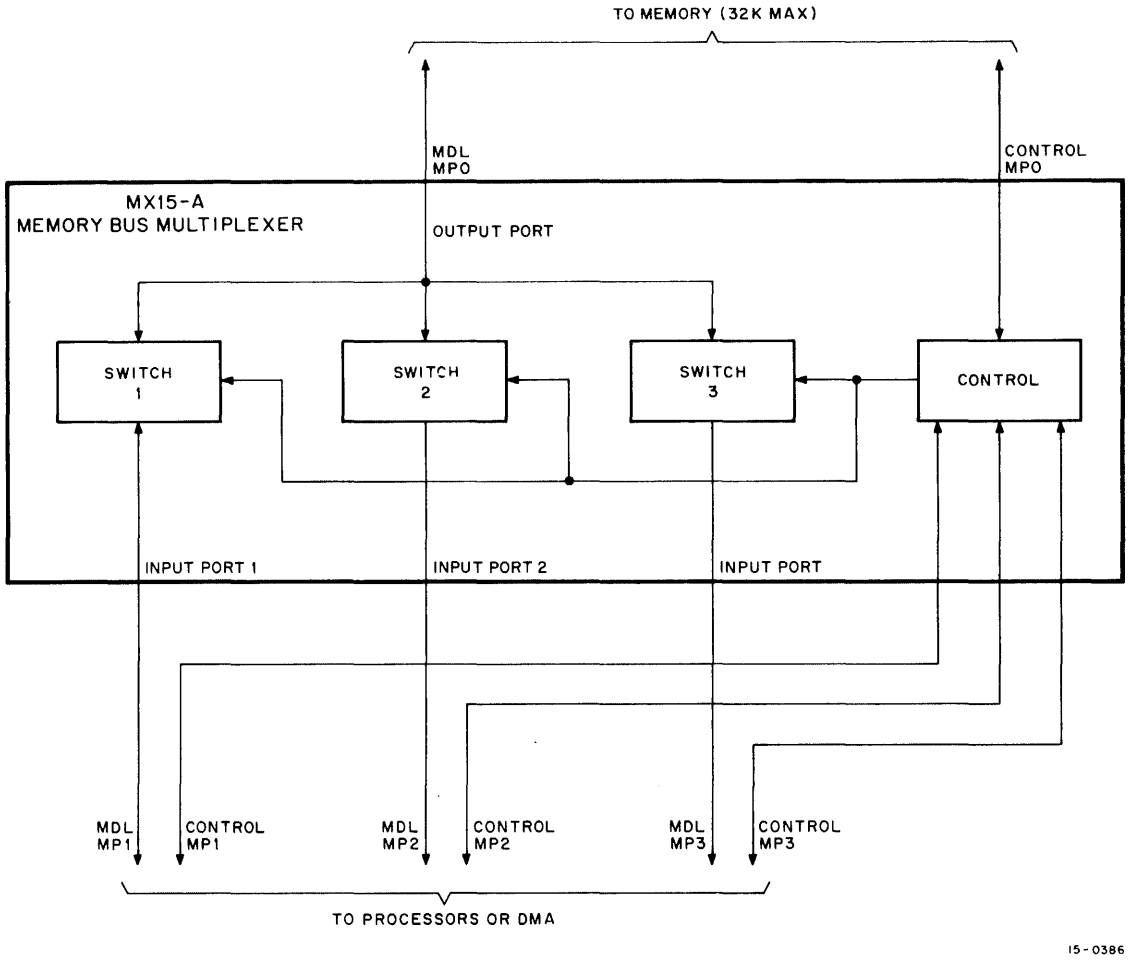


Figure 1-1 MX15-A Simplified Block Diagram

and to enable all memory banks to be accessed by both KP15 processors. Addresses that do not correspond to an existing memory bank are inhibited by the MX15-A. Without the bank rotate feature, a multiprocessor system cannot be assembled using one block of core memory. Other multiprocessor systems can be configured using more than one multiplexer, if each is connected to a block of memory. In these configurations, the bank rotate feature is not needed. In the configuration illustrated by Figure 1-4, the processor connected to the high priority port could be used for high-speed I/O transfers; simultaneously, the other processor can execute complex calculations on the data stored in the directly-connected memory bank.

1.2 SYSTEM DESCRIPTION

1.2.1 Single and Multiprocessor System Description

1.2.1.1 Location of Equipment Bays - The MX15 equipment bays are located immediately to the left of the processor bay. Other options, such as disks that normally are located to the left of the processor, must be located to the immediate left of the MX15 equipment bays.

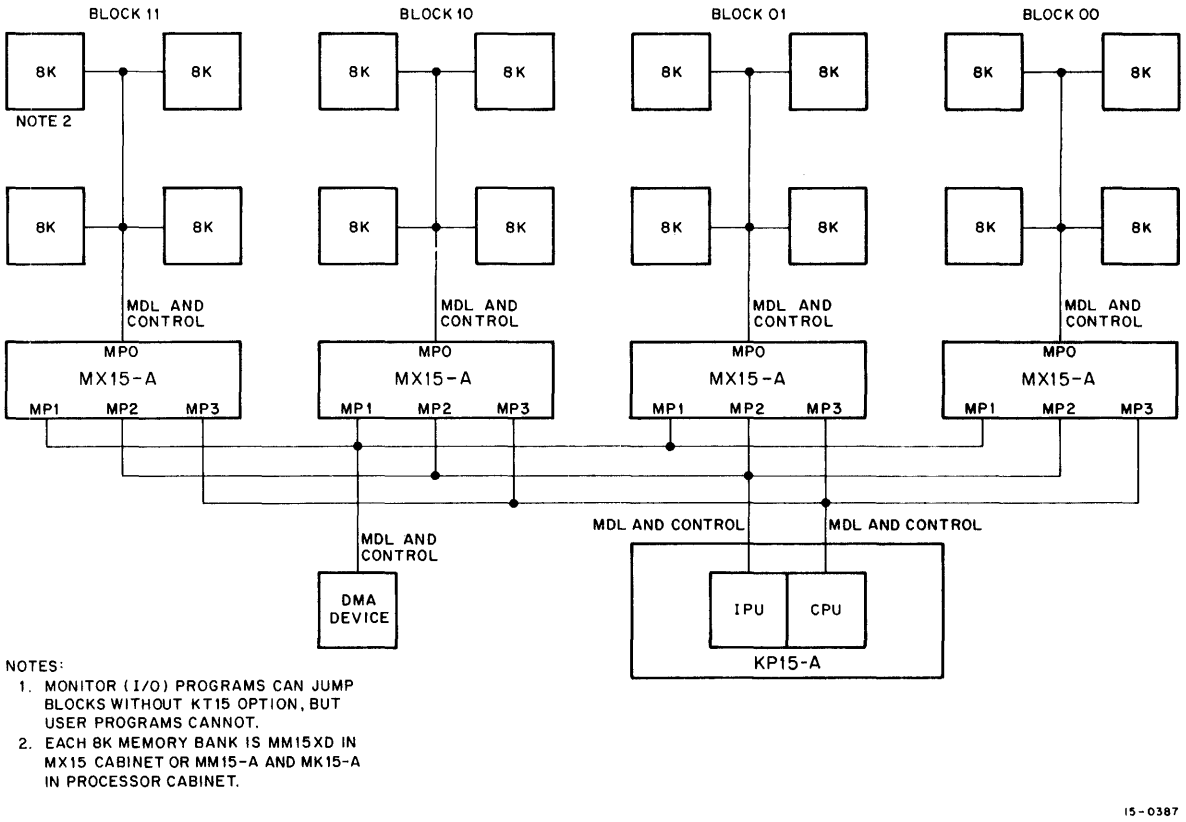


Figure 1-2 Extended Memory Block Diagram

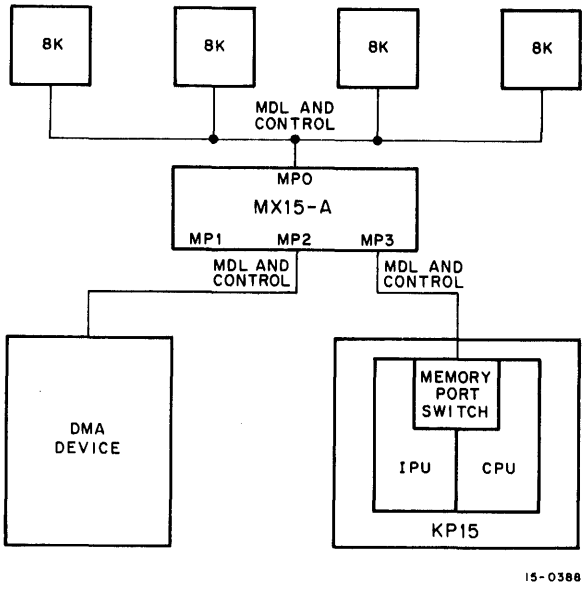
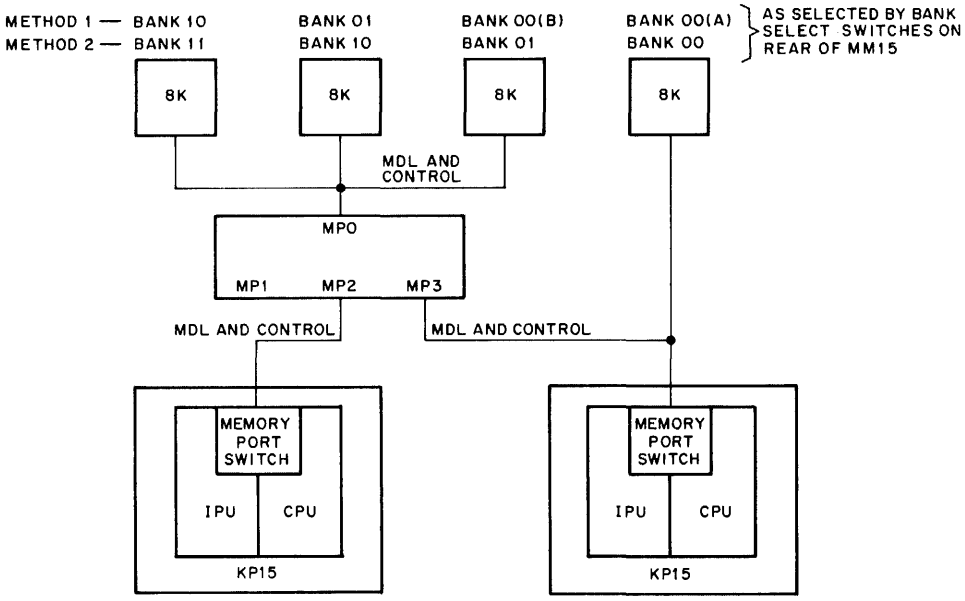


Figure 1-3 Direct Memory Access Block Diagram



METHOD 1: MP3 ROTATED 24K

BANK SELECT BITS			PHYSICAL BANK SELECTED
MP2	MP3	MP0	
—	00	NONE	00(A)
00	01	00	00(B)
01	10	01	01
10	11	10	10
11	—	NONE	

METHOD 2: MP2 ROTATED 8K

BANK SELECT BITS			PHYSICAL BANK SELECTED
MP2	MP3	MP0	
—	00	NONE	00
00	01	01	01
01	10	10	10
10	11	11	11
11	—	NONE	

15-0389

Figure 1-4 Multiprocessor System Block Diagram

In multiple processor systems, MX15 equipment bays are located between the processors (if there are two) with no other bays between processors. In 3-processor systems, care must be taken to keep the longest memory bus length below the maximum length allowed.

1.2.1.2 Memory Bus Loading - A PDP-15 memory bus can accept as many as four loads. An MX15-A is considered one load, as is an MM15. Thus, electrically, a PDP-15 memory bus may be connected to any combination of four MM15s and MX15-As.

1.2.1.3 Addresses of MM15 Attached Directly to Processor Bus - Banks of core memory (MM15s) attached directly to a processor bus can only have addresses in the lowest block of core (block 00).

1.2.1.4 MX15-A Output Bus Loading - The MX15-A can drive as many as four PDP-15 memory bus loads. Because each MM15 is one load, the MX15-A can drive 32K of core.

1.2.1.5 Block Number of a Bank Attached to an MX15-A - The block number of a bank (MM15) attached to the output bus of an MX15-A is determined by the MX15-A. Block numbers are specified by MDL bits 01 and 02. Each MM15 attached to an output bus can be addressed as any block number (0 through 3) independent of the block number the other banks of memory attached to that MX15-A respond to. Each input port having access to that bank can, in addition, address the bank with its own block number. In summary, each input port can address a fixed bank of core attached to an MX15-A with a block number that is independent of the block numbers other ports addressed it and the block numbers of the other banks attached to the MX15-A.

The method of selecting block number is described in Paragraph 2.4, Selecting Block Numbers (M628 Jumpers). The physical process consists of cutting jumpers on the M628 modules in the MX15-A.

1.2.1.6 Bank Numbers of MM15s Attached to MX15-As - Each bank attached to the output bus of an MX15-A must have its bank select switches set to a unique number: one bank 00, one bank 01, one bank 10, and one bank 11 attached to a given MX15-A.

1.2.1.7 Bank Disable (SELECT) - An input port can be prevented from using any combination of MM15s attached to an MX15-A. The bank select switches associated with each port on the MX15-A prevent illegal use. Each input port has four bank select switches, one for each bank (00, 01, 10, 11). By setting a bank select switch to its zero position, the port associated with that switch will be

prevented from using the MM15 whose bank switches are set to the same number. For example, if the bank 10 switch associated with memory port 3 is set to zero, then memory port 3 is prevented from reading or writing in the bank whose switches are set to 10.

1.2.1.8 Bank Rotation - In multiprocessor systems using the MX15-A, each processor must have its own unique bank 00. Consequently, the MX15-A has the capability to rotate the bank addresses it receives before transferring them to individual memories. Each memory port has two bank rotate switches that can add 8K, 16K, or 24K to the address it receives. All addresses received by that port are rotated the amount set on the bank rotate switches. The rotation is always within a given block. The rotation logic does not propagate carries from memory address bit 03 to memory address bit 02.

1.2.1.9 Address Restriction - When configuring multiprocessor systems, only one bank must respond to each address sent from a processor. Also, the user must make certain that the address space of each processor is contiguous.

1.2.1.10 Order of Filling MM15 Slots in MX15 - The MM15 slots in the MX15 must be filled from bottom to top. No blank slots may be left between MM15s because the MM15XD designation numbers include cables that assume the MM15 slot, just below the one to be filled, is already filled.

1.2.1.11 Cable Length Limitation - The PDP-15 memory bus cable is designed to operate satisfactorily at a length of 21 ft. This length must not be exceeded. Figure 1-5 shows five different buses that constitute a 128K PDP-15 System that includes the BB15 option.

1.2.1.12 Indicator Bus Restriction - The MMA (memory address) and MMB (memory data) register positions on the indicator bus have several limitations on MX15-A Systems that are not present on normal PDP-15 Systems. In single-processor systems, these positions contain the inclusive OR of the contents of the MMA and MMB of all the memories. This will be the OR of the last memory operation to each MX15-A, because the MMB and MMA retain their contents until the memory is addressed again. Hence, the MM15s change their MMA and MMB by "MX15-A blocks", and one set of ADDRESS and DATA will be present for each MX15-A on the bus. In multiprocessor systems, the MMA and MMB positions reflect the operations of the other processor, if it is running. It is not possible to examine the MMA and MMB unless both processors are halted. These limitations can be partly overcome by carefully configuring the indicator buses in multiprocessor systems and by making deposits of 0 to location 0 of each MX15-A block of core not of interest.

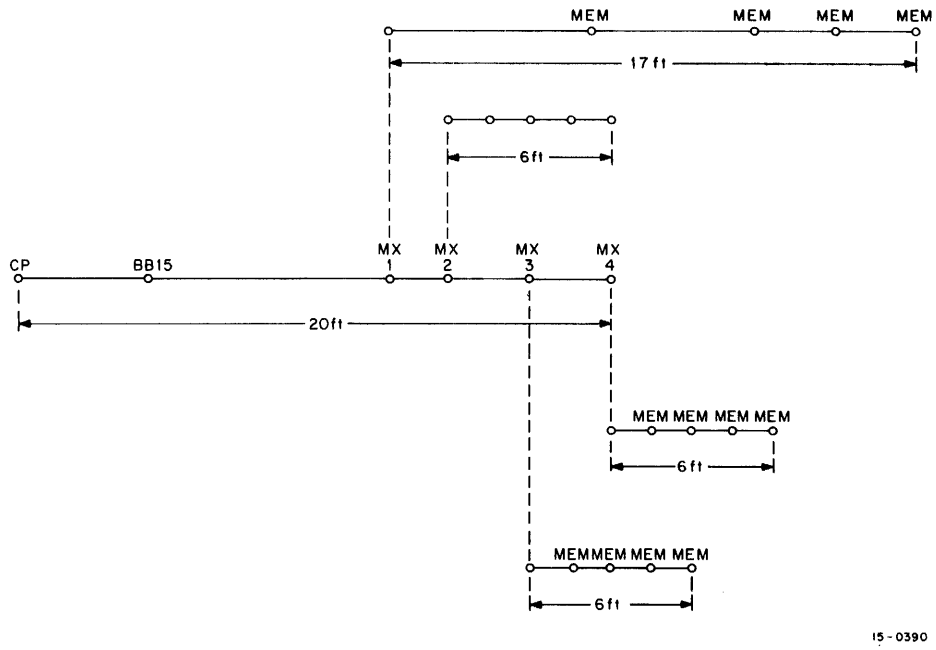


Figure 1-5 128K CP/Memory Cable Lengths

When a processor is turned off, all memory lines go to their true level of ground, including PWR CLR (power clear to the memory). Therefore, the MMA, MMB, and MST indicator positions return to a cleared state at the end of each memory cycle.

1.2.2 Multiprocessor System Rules

The PDP-15 IPU logic system is designed to operate with the increased delays caused by the MX15-A. Certain configurations of large multiprocessor systems with many peripherals can congest the I/O bus. Note that a second processor using memory and using the same MX15-A as the IPU must be considered as an I/O device when calculating latency and I/O bus utilization.

1.2.2.1 MX15-A Priority Types - The MX15-A honors requests in the order in which they occur, except if two or more requests occur simultaneously or are waiting at the end of the current cycle, a hardware priority feature gives memory port 1 service before memory port 2, and memory port 2 before memory port 3.

1.2.2.2 Processor Bus Priority - A processor connected to several MX15-As may have its bus connected into a different priority port in each MX15-A. Thus, a given processor can have higher priority access to some memory and lower priority access to other memory.

1.2.2.3 Proper Port Connection for PDP-15s - A PDP-15 that can process DCH or back-to-back single-cycle I/O breaks, must be connected to port 2 or port 3. Each of these ports has special logic that detects a special memory bus signal, which gives the I/O sequence absolute priority when it is initiated. Consequently, when a three- or four-cycle break is initiated in port 3 for example, neither port 1 or port 2 can interrupt it until the entire break is completed. This is a requirement for the PDP-15 I/O processor. A PDP-15 must not be connected into port 1 unless no I/O activity other than "single" single-cycle breaks is expected.

1.2.2.4 Direct Memory Access (DMA) Port - Port 1 is designed for use with custom equipment, e.g., the DMA channel. With careful programming, the DMA facility can be used concurrently with the processor with no cycle stealing. Other ports can also be used for DMA channels. For a further explanation see the detailed discussion of Direct Memory Access in Chapter 5.

1.2.2.5 Power Fail Protection Configurations - The logic associated with memory power failure is designed to notify all processors, connected to the particular MX15-A whose memory is issuing the memory power failure signal, that a power failure has occurred. Consequently, in systems where the user must be able to turn off power on any processor without affecting the rest of the system, only PRIVATE memory can be located in a processor cabinet where it is powered by the processor power supply. All shared memory must be located in independently-powered MX15 cabinets. A power failure in any memory attached to a given MX15-A is sent to all processors connected to the MX15 multiprocessor system. Thus, in a PDP-15, a power fail signal in a shared memory will power down all processors connected to it.

1.3 MX15-A SPECIFICATIONS

1.3.1 Physical

MX15-A

Dimensions:

Width	19-1/8 in.
Height	5-2/8 in.
Depth	7-2/8 in.

Mounting Space: 5-2/8 in. of rack space

Finish = Aluminum conversion (Chromicoat)

MX15 Bay

Weight - 500 lb

1.3.2 Environmental

Recommended Ambient:

Temperature - 70° to 85°F
Humidity - 30% to 80%

Factory Tested Ambient:

Temperature - 50° to 122°F
Humidity - 20% to 90%

1.3.3 Electrical

1.3.3.1 Power

MX15-A 4.4A @ +5V

MX15 Bay implemented with 32K of memory

10A @ 117V 60 Hz
5A @ 240V 50 Hz

1.3.3.2 Delay and Cycle Times

Circuit delay in MX15-A

Typical	240 ns
Worst Case	300 ns

Cycle Times of PDP-15 Systems with MX15-As are as follows:

Cycle	No Option	KM15	KM15 and KT15
READ	1080 ns	1120/1120 ns	1150/1160 ns
WRITE	1105 ns	1120/1230 ns	1150/1260 ns

1.3.3.3 Latency - Memory access time in the MX15-A varies from 730 ns to 5.06 μs. See Paragraph 5.1.2 for a detailed explanation of the latency specifications of the MX15-A and the latency for different system states.

1.4 EQUIPMENT SUPPLIED

The MX15-A is mounted in a standard H963 19-in. equipment bay with as many as four MM15XD core memory banks and all necessary power supply and power control circuitry. Two MX15-As can be installed in one equipment bay. Any configuration within the limitations specified above can be created and designated an MX15 equipment bay. Typically, three MX15s are required to assemble a maximum configuration. The power supplies and control units included in an MX15 equipment bay are powered for maximum utilization, and all the modules comprising an MX15-A are listed in Table 1-1. The

MM15XD modules are not listed in this table; they are described in the PDP-15 Maintenance Manual. The MM15XD core memory banks located in the MX15 equipment bays differ from the banks (MM15-A and MK15-A) located in the KP15 equipment bay in that the MM15XD banks use a G829 +5V power connector module instead of a G821 +5V regulator module. This difference exists because regulation of the +5V power in the MX15 equipment bay is controlled by the power supplies.

Table 1-1
Equipment Supplied

Type/Part No.	Name	Quantity
MX15	Multiplexer Equipment Bay	3 (max)
MM15XD	Core Memory	4 (max per bay)
MX15-A	Memory Multiplexer	2 (max per bay)
G827	Power Sequence Detector and Delays	1
G829	Power Connector	1
M111	Inverters	3
M133	NAND Gates	2
M135	NAND Gates	1
M139	NAND Gates	6
M311	Tapped Delay Lines	1
M312	Delay Lines	1
M602	Pulse Amplifiers	1
M622	I/O Bus Drivers	18
M627	NAND Power Amplifiers	3
M628	Block-Bank Address Card	3
M902	Terminator Card	6 (max)
M904	Coaxial Cable Connector	14 (max)
M911	Memory Bus CP Terminator Card	6 (max)
W714	Switches	6
841-B	Power Control	1
H721	Power Supply	2
798-A	Power Supply	1
856	Power Control	1
7006862-0-0	Flat Coaxial Cable (13.25 in.)	12 (max)
BC08B-1	Flat Coaxial Cable (1 ft)	6 (max)

Table 1-1 (Cont)
Equipment Supplied

Type/Part No.	Name	Quantity
BC08B-2	Flat Coaxial Cable (2 ft)	22 (max)
BC08B-3	Flat Coaxial Cable (3 ft)	12 (max)
BC08B-7	Flat Coaxial Cable (7 ft)	2 (max)
7006414-1	Cable (8 in.)	6 (max)
7006414-2	Cable (6 ft)	1
7006437-2	Dual Mylar Cable (2 ft)	3 (max)
7006437-6	Dual Mylar Cable (6 ft)	1
7006437-10	Dual Mylar Cable (10 ft)	1
BC08A-*	MX-A Input Port Cables	4

1.5 REFERENCE DOCUMENTS

The complete set of PDP-15 manuals are identified and described in the family tree and accompanied listing in the front of this manual. In addition, the following diagnostic programs are essential to establish the performance of the MX15 equipment bays. Only the last program is supplied with an MX15-A System and then only if the system exceeds 32K.

Memory Address	MAINDEC-15-D0CA-D(D)
Extended Memory Address Test	MAINDEC-15-DIFA-D(D)
Memory Checkerboard Test	MAINDEC-15-D1A0-D(D)
External Memory Checkerboard Test	MAINDEC-15-D1BB-D(D)
Extended Memory Key Instructions,	
PI, API, and Auto Index Test	MAINDEC-15-D1CB-D(D)
MX15 Memory Multiplexer Test	MAINDEC-15-D1MA-D(D)

CHAPTER 2
INSTALLATION

Basic PDP-15 installation information such as unpacking, special handling, inspection, and mounting procedures is contained in the PDP-15 Installation Manual. Information related to the MX15-A is included in this chapter.

2.1 SHIPPING CHECK LIST

The following list of items should be included with your MX15. Any shortages should be immediately reported on the DEC Customer Acceptance form (DEC-12-1015).

A. DOCUMENTATION

MX15 Maintenance Manual (Engineering Specification Part B)

D-UA-7006863-0-0	MX15 Maximum Configuration
D-UA-H963-N	H963-N Cabinet Assembly
A-ML-MX15-A	MX15-A Logic Assembly
D-UA-841B	841-B Power Control
D-CS-H721-0-1	H721 Power Supply
B-CS-798-0-1	798 Power Supply (798-A in 50 cycle systems)
B-CS-856-0-1	856 Power Control (see Figure 7-1)

B. CABLES

1 7006437-10 flexprint cable (indicator bus)

2 BC08B-* flat coax cables (min). The appropriate length can be determined by bay location in the system configuration.

C. FUSES, SPARE

5 AGC 3
5 AGC 5
5 MDA 12
5 GBB 25

D. MODULES, LOOSE

The M902 and M911 modules, not used in the MX15-A configuration, are shipped with the equipment as a maintenance aid.

E. FILTER

1 H950S Filter

F. DIAGNSOTICS

(Systems with greater than 32K only)
DEC-15-D1MA-D(D) MX15 Memory Multiplexer

2.1.1 Customer Acceptance Procedure

The following acceptance procedure is designed to demonstrate that the MX15-A is operating correctly. Several specific tests are described that relate directly to the MX15-A. However, no diagnostic will confirm that the MX15-A is operating correctly, because the MX15-A is "transparent" to the processor. Thus, the correct functioning of the total system demonstrates the correct functioning of the MX15-A. The procedure duplicates steps previously performed at the factory.

CAUTION

Make certain that all modules and memory core stacks are firmly seated before turning on power.

POWER UP/DOWN	Turn the power OFF and then ON in the MX15-A option. Simultaneously, depress STOP and RESET on the PDP-15 console. It must be possible to deposit and examine the core attached to each MX15-A.
BANK SELECT	One at a time, set the bank select switches to 0; with the switch in the 0 position, the processor associated with the corresponding input port must not be able to either write into or read from that bank.
BANK ROTATE	Set a unique number into any location of each bank. Read from this location with the bank rotate switches set for 8K, 16K, and 24K.

NOTE

For systems equipped with greater than 32K of core memory, the system must pass the MX15 Memory Multiplexer Test.

2.1.2 Multiple Processors

With multiple processors, the priority arrangement of the MX15-A can be confirmed by keying a JMP. instruction into the memory, from the console. Both processors should simultaneously execute the JMP.

2.2 MX15 CONFIGURATIONS

The design of the MX15 enables a variety of configurations to be created, each custom built for a customer's specific need. A maximum system configuration is illustrated in Figure 2-1. Figure 2-2

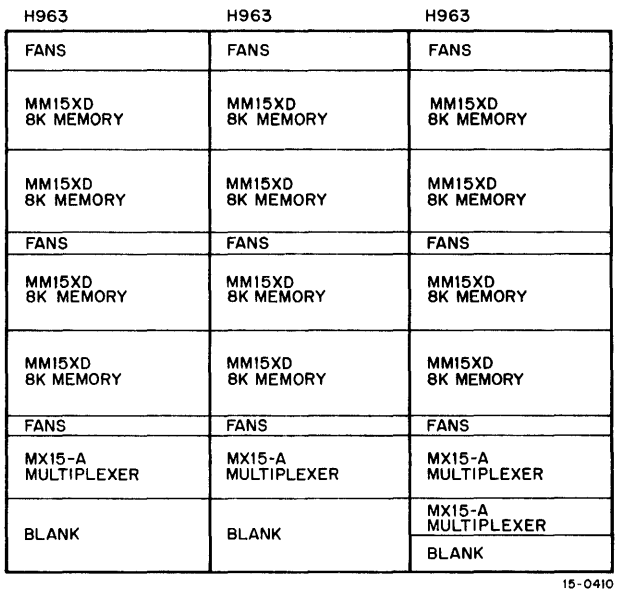


Figure 2-1 Maximum System Configuration Diagram

locates the modules within the MX15-A (viewed from the module side). Each MX15 equipment bay can contain as many as four MM15XD core memory banks and one MX15-A multiplexer. Equipment bay 1 is equipped to handle one additional multiplexer. In addition, each equipment bay contains all the power supply and power control equipment required to power the MM15XD memory banks and MX15-A multiplexer. Power supplies are installed only to the extent needed for the amount of memory ordered.

2.3 CABLING

All interconnecting cables required for a customer's installation are supplied with the equipment. Cables for connecting a customer-supplied DMA device must be ordered separately. There are two additional BC08B-* cables (per MX15-A) required for connecting this device. The cable complement for a maximum MX15 configuration is listed in Table 1-1 of Chapter 1. For specific cabling information, refer to drawing D-UA-7006863-0-0 in Chapter 6.

NOTE

The end of a memory bus must be terminated with M902 modules. Unused input ports must be terminated with M911 modules.

CABLES BC08A-* FROM KP15
OR
TERMINATE WITH M911

CABLE BC08B-X FROM MM15

	MP1		MP2		MP3															MPO													
	CONT	MDL	CONT	MDL	CONT	MDL														CONT	MDL												
	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	M311	M111	M602	M627	M111	M904	M904	M904 OR M911	M904 OR M911	M904 OR M911	M904 OR M911	M622	M622	M622	M622	M622	M622	M622	M622	M622	M904	M904	M628	W714	W714	M628	W714	W714	M628	W714	W714	G829
B	G827	M135	M133	M312	M111	M904 OR M902	M904 OR M902	M904 OR M902	M904 OR M902	M904 OR M902	M904 OR M902	M622	M622	M622	M622	M622	M622	M622	M622	M622	M911	M911	M627	M627	M133	M139	M139	M139	M139	M139	M139	M139	G829

TERMINATE WITH M902 OR CHAIN TO NEXT MX15A WITH M904 (CABLE BC08A-*) IF CABLE IS IN SLOT ABOVE, OTHERWISE LEAVE SLOT BLANK.

TERMINATE WITH M911

15-0391

Figure 2-2 MX15-A Configuration Diagram

2.4 BLOCK AND BANK ASSIGNMENTS

After a system is installed and before power is turned on for the first time, block and bank numbers must be assigned to the memory. These numbers can be assigned by physically cutting jumpers in the M628 modules of the MX15-A, setting switches on the W714 and M628 modules of the MX15-A, and setting switches on the W714 modules of the MM15XD.

NOTE

In factory-assembled systems, these operations have been performed to customer specifications.

Three M628 modules and six W714 modules are contained in each MX15-A. One M628 module and two W714 modules provide the block and bank address identity for each input port. Cutting specific combinations of jumpers (see Figure 2-3) in the M628 module causes the corresponding input port of the multiplexer to respond to one or more block address.

Normally, the jumpers are cut so that a given input port of the multiplexer responds to only one block address. However, in some configurations it may be necessary to have the MX15-A respond to more than one block address. If a bank does not exist on a particular MX15-A, cut all four jumpers.

The BANK ADDR ROTATION switches on the M628 module (see Figure 2-4) should be set to 0, unless the memory bank address bits are to be altered for the corresponding input port. If all memory banks are to respond to a specifically addressed port, the BANK SELECTION switches should be set to 1. Those switches that correspond to a nonexistent bank or to a private bank for another processor must be set to 0. The memory BANK SELECTION switches in the MM15XD must also be set so that each bank will respond to a different address, starting with 00 to ensure contiguous addressing. This procedure is described in the PDP-15 Operator's Guide.

2.5 CONNECTION OF JUMPER WIRES IN WIREWRAP FIELD

Jumper wires are used in the wirewrap field to disable unused input memory ports. To prevent the MX15-A from "locking up" when powering up, all memory ports that are not used in a particular installation must be disabled. A memory port is disabled by preventing the REQ ACTIVE flip-flop from being set (true). To disable a memory port that is not in use, connect a jumper as listed below:

Memory port 1: pin B06P2 to pin B06T1
Memory port 2: pin B04P2 to pin B04T1
Memory port 3: pin B02P2 to pin B02T1

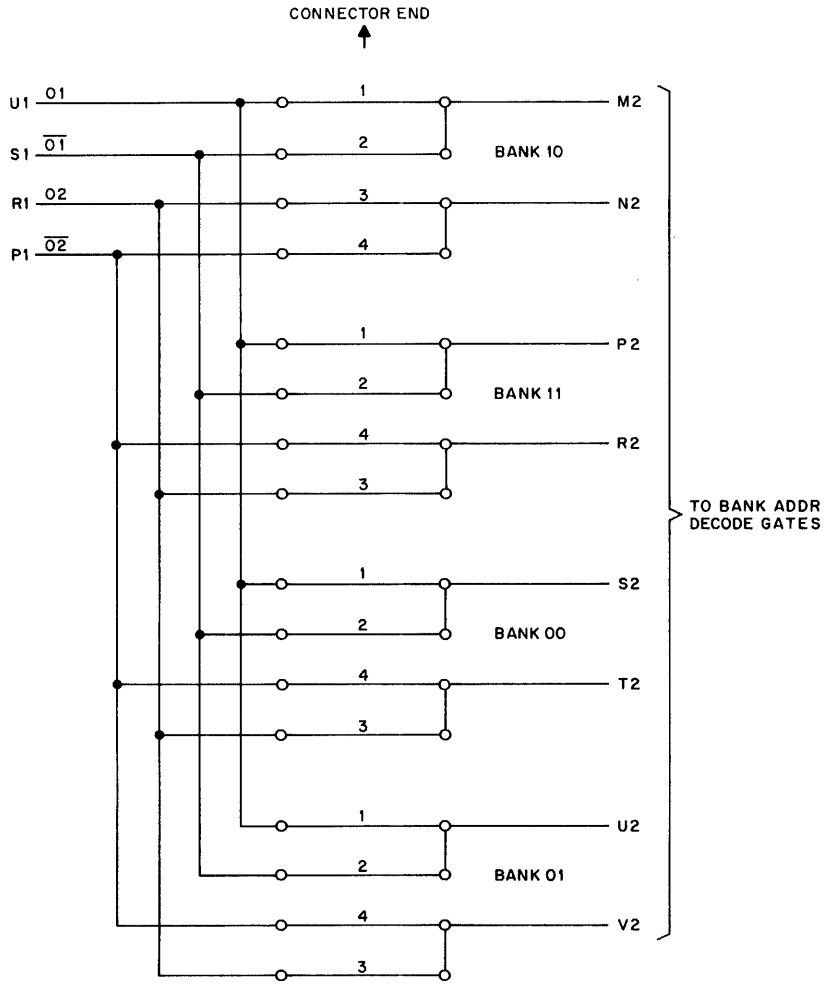


Figure 2-3 M628 Module, Block Select Jumpers

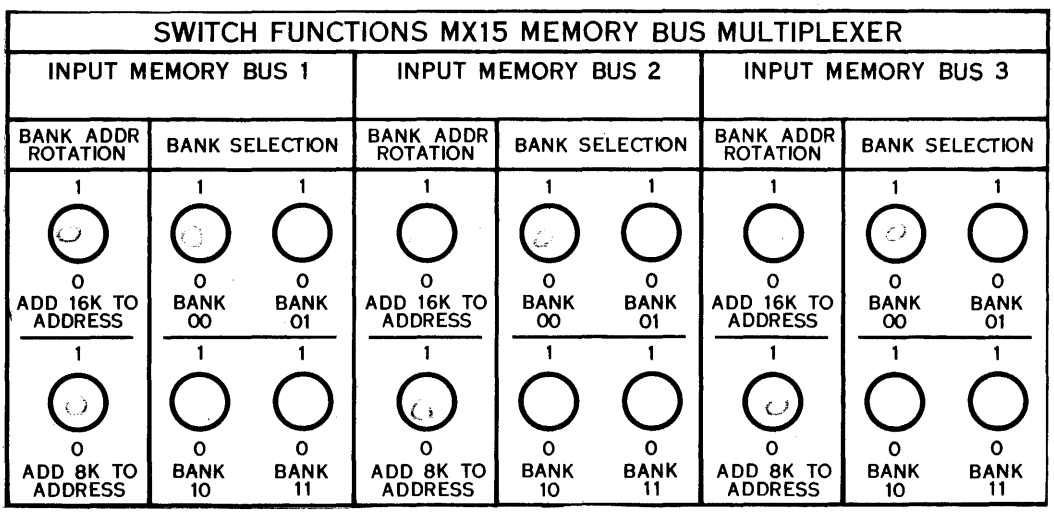


Figure 2-4 M628 and W714 Modules, Switch Functions

2.6 ADJUSTMENT OF PRIORITY MARGIN IN MULTIPROCESSOR AND DMA SYSTEMS

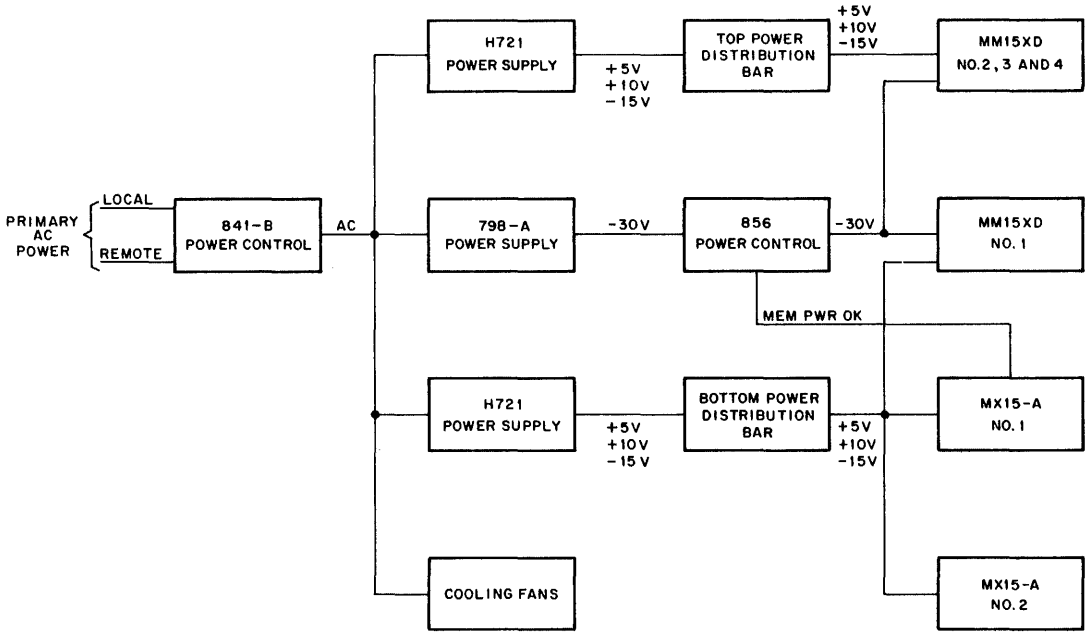
The alternating sequence of memory accesses is maintained by properly setting the TS01 in each processor. The length of the TS01 is measured at pin E30K2 of the KP15 processor. The TS01 is adjusted by turning the potentiometer on the rear of the M775 module in slot E30 in the processor.

The margin available in the system can be checked by following the procedures outlined below.

Step	Procedure
1	Set both processors to a JMP.-1 in the bank at the end of the memory bus that services the processor bay.
2	Attach channel 1 of the oscilloscope to PRIORITY RESET (Pin A30F2) in the MX15-A serving the processor cabinet.
3	Put the channel 2 probe on signal M REQ DLY of the port being checked.
4	Sync the oscilloscope to channel 1 in the processor. The difference in time from the trailing edge of PRIORITY RESET to the leading edge of M REQ DLY plus 10 ns is the low side margin available in the specific processor. The high side margin is determined by factors in the processor. TS01 should be adjusted so that the margin seen on the oscilloscope is no less than 15 ns. However, TS01 should never be reduced below the nominal setting (260 ns) recommended in the PDP-15 engineering specifications.

2.7 POWER

Two primary power sources are available at each equipment bay: local and remote. Local power enables the user to power-up each MX15 equipment bay, independently. Remote power is chained from one cabinet to another and is controlled at the PDP-15 console. Each equipment bay contains all the control circuits and power supplies to convert the local or remote primary ac power to the dc voltages required by the MM15XD banks and MX15-As. Power is automatically turned on by a three-step sequence that stabilizes all power at the correct level. Interlock protection for overtemperature, overvoltage, undervoltage, and overcurrent is also included in the power supplies. A simplified block diagram illustrating the distribution of power within an equipment bay is shown in Figure 2-5. For detailed information concerning distribution and control of ac and dc power, refer to the engineering drawings provided in Chapter 6.



NOTE:
THIS ILLUSTRATION SHOWS A MAXIMUM POWER SOURCE CONFIGURATION IN AN MX15 EQUIPMENT BAY. FOR A SPECIFIC CUSTOMER CONFIGURATION, ONLY THOSE POWER SUPPLIES REQUIRED FOR THAT INSTALLATION ARE INCLUDED IN THE MX15 EQUIPMENT BAY.

15-0394

Figure 2-5 MX15 Power Distribution Block Diagram

2.7.1 Adjustments

Adjust the -15V power level of the H721 power supply to -13V as measured at the output connector. This adjustment is accomplished by removing the top of the H721 power supply and adjusting R204, which is the fourth potentiometer from the left. The +5V power level in the H721 is adjusted to +5V measured on pin A2 of the logic. A screwdriver adjustment through the hole in the top of the H721 power supply performs this adjustment.

2.8 FIELD ADD-ONS

2.8.1 Processor Status

A PDP-15 processor that has an MX15-A added to it must have its wirewrap field updated to at least revision AJ. It must also include the following ECO (engineering change order). Without this ECO, DCH and Real-Time Clock breaks may not function properly. The ECO consists of the following wiring changes:

Signal	Pins	Action
KD06 STB MRLS DLY L	M18V1 - M12T2	delete
KP32 I/O MRLS ACK L	M18S2 - M12T2	add
KD06 M18L1	M18L1 - L18A1	delete
KD06 M18N1	M18N1 - L18A1	add

2.8.2 Memory Status

A memory bank originally located in the processor cabinet can be relocated in an MX15 cabinet if the following steps are taken:

Step	Procedure
1	Remove the G821 module in slot A01 and B01, and replace it with a G829 module.
2	Be sure the G822 modules in slots C01 and D01 are revision F, or later.
3	Before initial power-up of the relocated memory, adjust potentiometer R3 (the center potentiometer) on the G822 module approximately five turns counterclockwise. Failure to make this adjustment will cause the -15V fuse to blow because of the crowbar overvoltage protection in the G822 module. After power is applied, adjust R3 to obtain -6 Vdc output, as described in engineering drawing D-BS-MM15-0-20 in the PDP-15 Maintenance Manual Engineering Drawings.

CHAPTER 3
OPERATION

There are no front panel controls or indicators on the MX15-A; consequently, there are no conventional operating procedures. There are, however, switch modules in the MX15-A whose switches must be properly set, and jumper wires in the wirewrap field that must be connected properly when installing a system (refer to Paragraphs 2.5 and 2.6). These switches and jumper wires can also be changed periodically to change the priority mode, to change distribution of the MM15 memory between two KP15 processors, or to create private banks in a multiprocessor system.

3.1 MEMORY DISTRIBUTION

Figure 3-1 illustrates three ways of distributing four banks of core memory between two processors. The bank address rotation and the bank selection switches enable the user to create or change the distribution. The switch settings required for the illustrated distribution, and the address of each bank (as seen by the processor) is also shown in Figure 3-1. A private bank is created for the other processor by not selecting the high-order bank associated with a specific processor.

These examples do not depict the only method four MM15s may be configured with two processors. It is, however, a successful method for creating a physically separate bank 00 for each processor, which is a necessary prerequisite for multiprocessor systems. A physically separate bank 00 is necessary because the first bank (bank 00) contains the PI, API, Data Channel, and Real-Time Clock locations that must not be shared.

3.2 PRIORITY

The term "priority" is meaningful only in a multiprocessor or direct memory access (DMA) configuration. The equal priority mode enables two processors to equally share common core memory on a cycle-stealing basis; this mode also enables a DMA channel to steal single memory cycles from the two processors. Because of the unique design of the PDP-15 IPU and the special logic included in memory ports 2 and 3, back-to-back single-cycle I/O transfers from the processors connected to memory port 2 or 3 will occur back-to-back, without processors connected to the other memory ports stealing cycles during the block transfer.

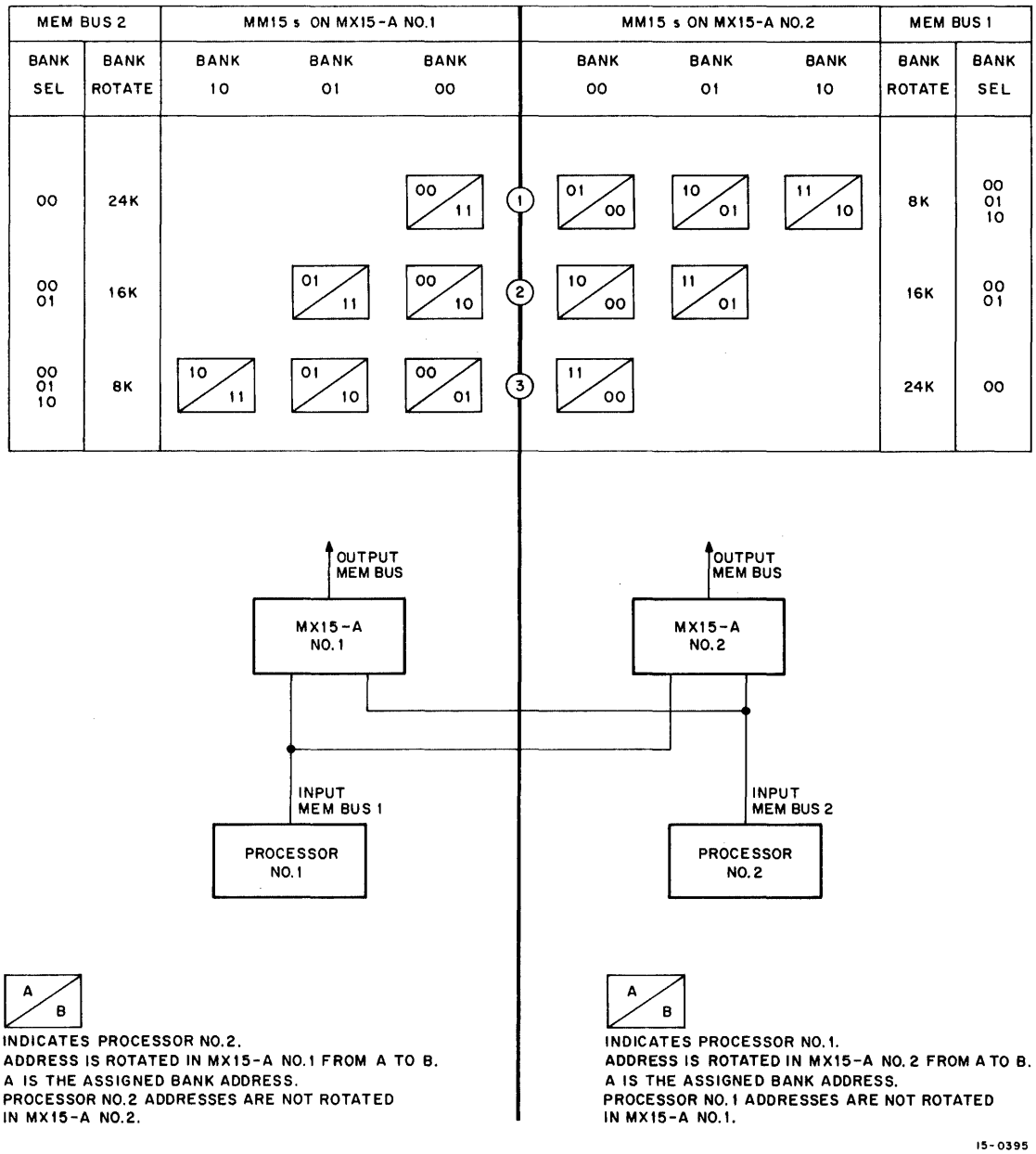


Figure 3-1 Memory Distribution in Multiprocessor Systems

Similarly, DCH transfers will be completed without the processors connected to other memory ports stealing cycles during the 3-cycle transfer. In other words, in the equal priority mode, back-to-back single-cycle transfers and DCH transfers are communicated to memory in the absolute priority mode. All other transfers have equal priority.

CHAPTER 4
PRINCIPLES OF OPERATION

Chapter 4 describes the internal operations of the MX15-A multiplexer. Block diagrams and simplified diagrams are included in this chapter; detailed block schematics are included in Volume 2 (see drawings D-BS-MX15-A-0-12 through 23). For information pertaining to the PDP-15 computer system, such as a description of the address and data formats, memory cycles, or the KT15 option, refer to the PDP-15 Maintenance Manual.

4.1 BLOCK DIAGRAM ANALYSIS

A block diagram of the MX15-A multiplexer is shown in Figure 4-1. Each sheet illustrates a set of bidirectional switches, address decode logic, and control circuits for one input port of the MX15-A. Sheet 1 includes the control circuits common to all input ports.

Communication between processor and memory involves two types of data transfers: memory-to-processor and processor-to-memory. In both cases, an address (in the form of a memory reference instruction) to identify the desired core memory location must precede the transfer of data.

For the MX15-A to properly direct communication traffic between the processor and memory, it must recognize whether the transfer is the address or the data and the type (direction) of data transfer. The MX15-A must know the direction of the transfer because the data to be transferred can appear either in the MO register of the processor or in the MB register of the memory. The MX15-A must also know whether the transfer is an address or actual data so that the multiplexer will not alter the address bits in the case of data transfers. Timing of the read, the write, and the read-pause-write memory cycles is shown in Figure 4-2.

The MX15-A remains idle until a memory request and an address is received and recognized by one of the three input ports. The address is placed onto the memory data lines (MDL) by the processor. This address is received by the bidirectional switches in the MX15-A, and if the address is not recognized, the MX15-A continues to remain idle. The block select jumpers, bank rotate switches, and bank select switches are set when the system is installed to recognize a number of specified block and

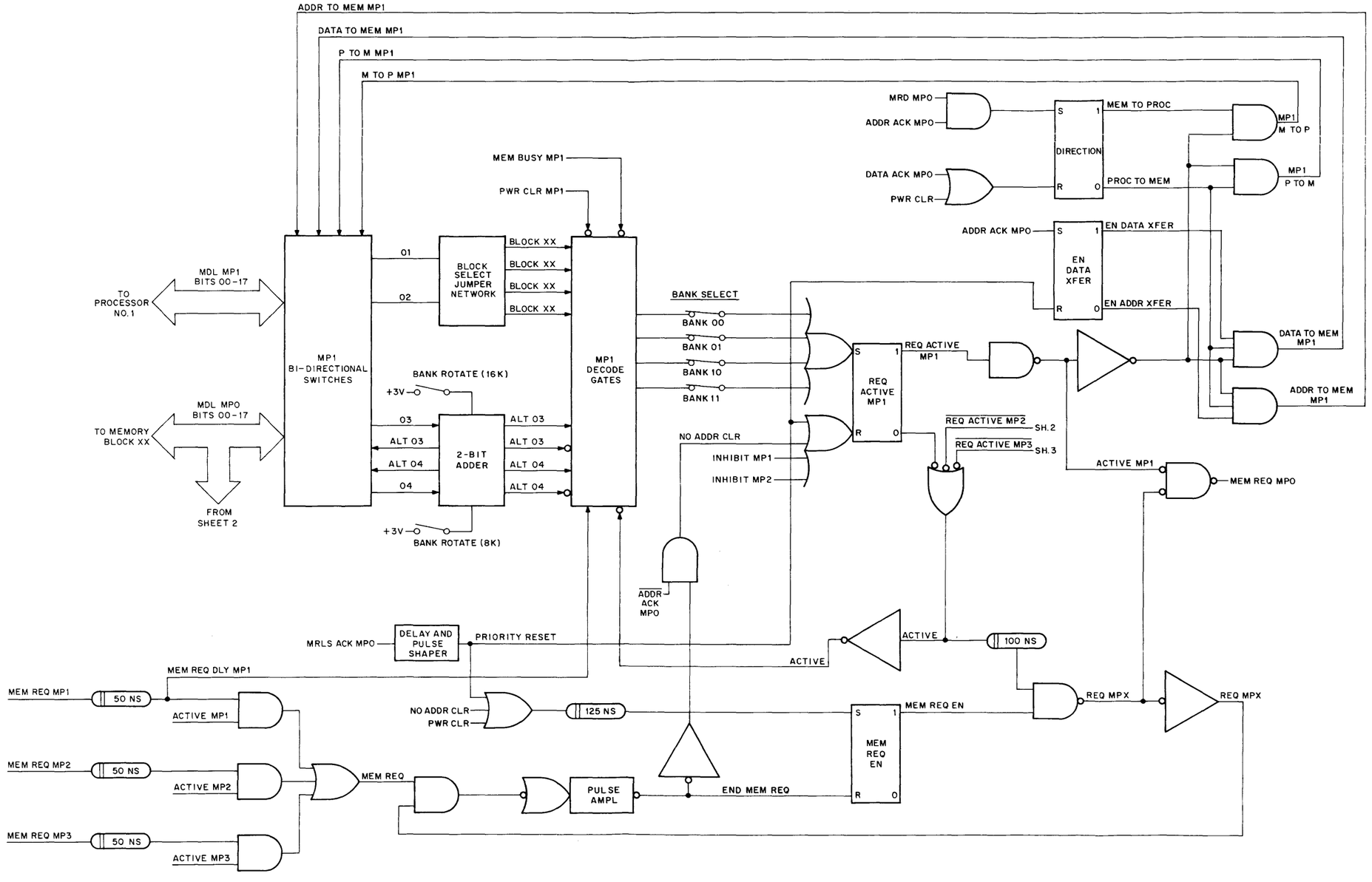


Figure 4-1 MX15-A Block Diagram (Sheet 1)

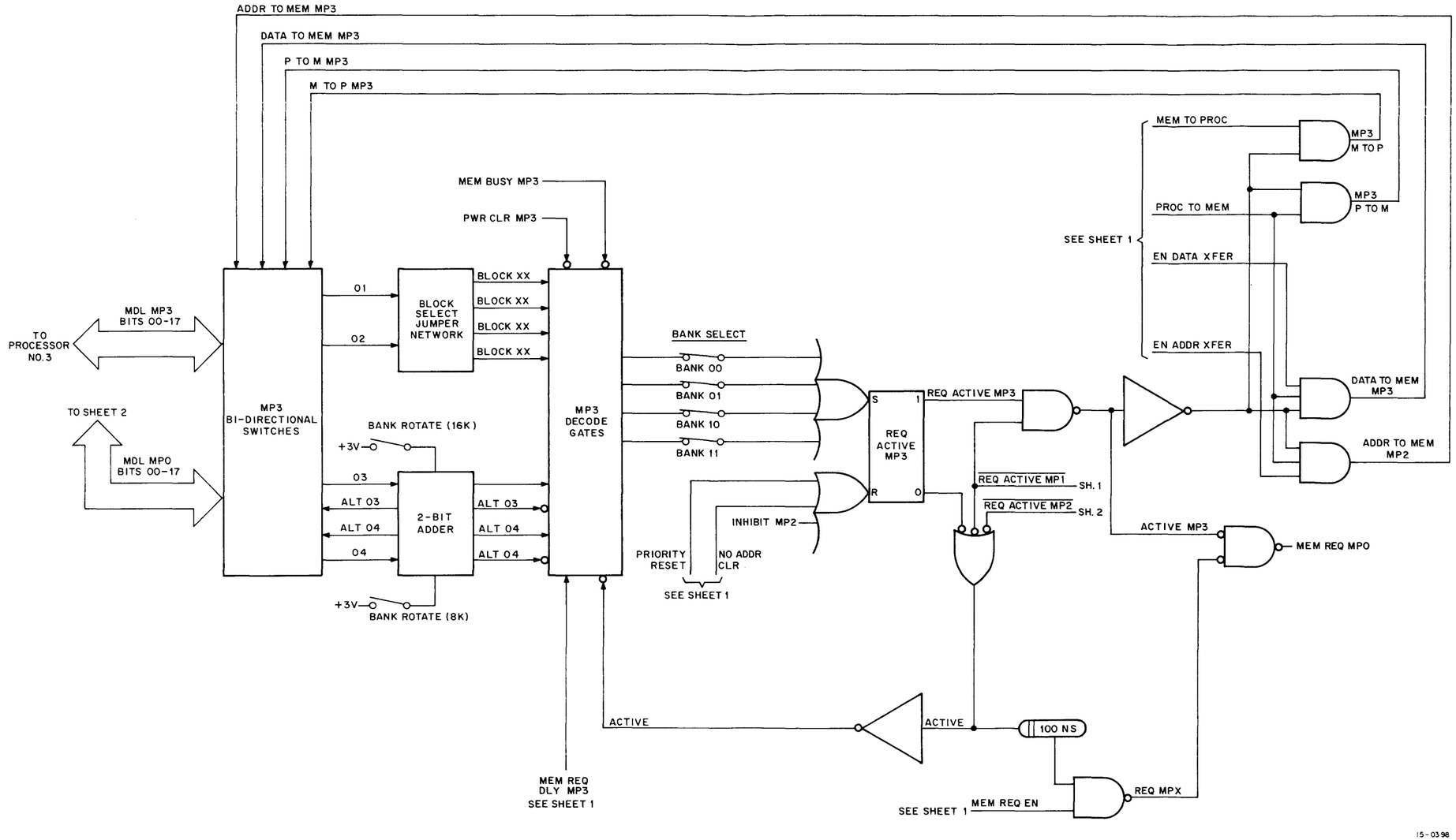


Figure 4-1 MX15-A Block Diagram (Sheet 2)

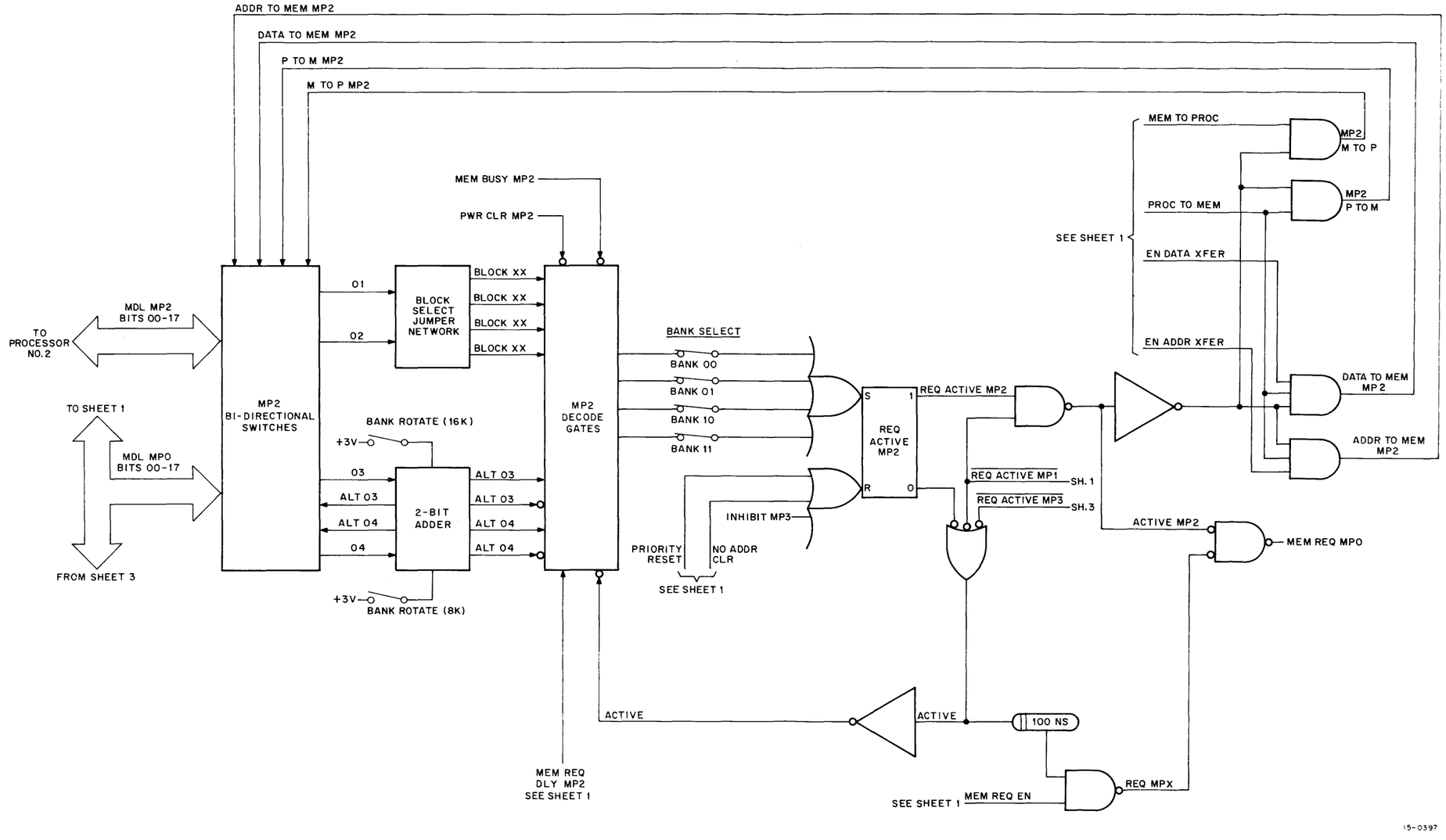


Figure 4-1 MX15-A Block Diagram (Sheet 3)

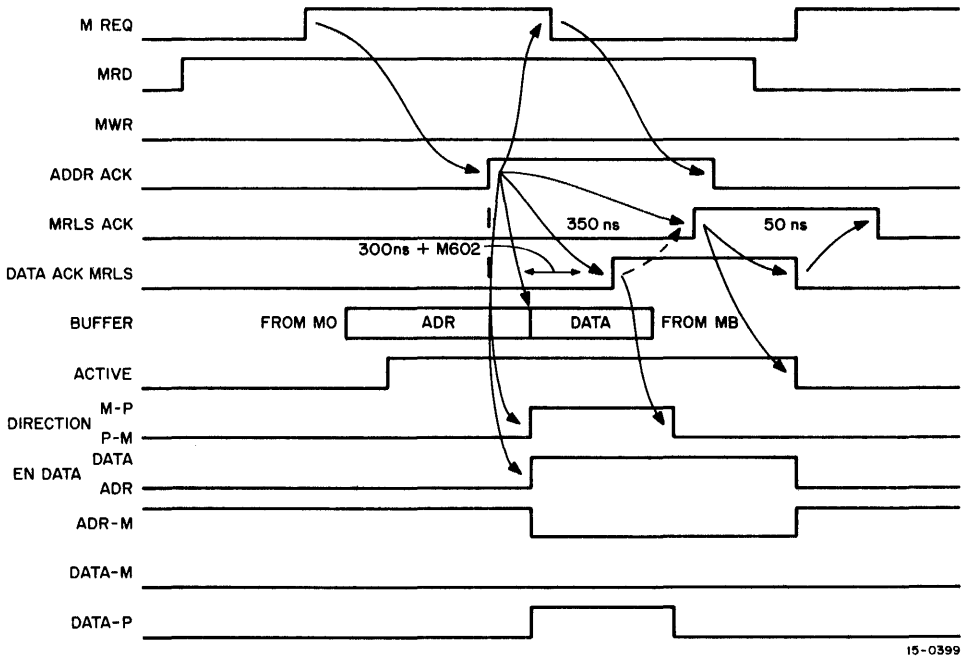


Figure 4-2a MX15-A Timing Diagram

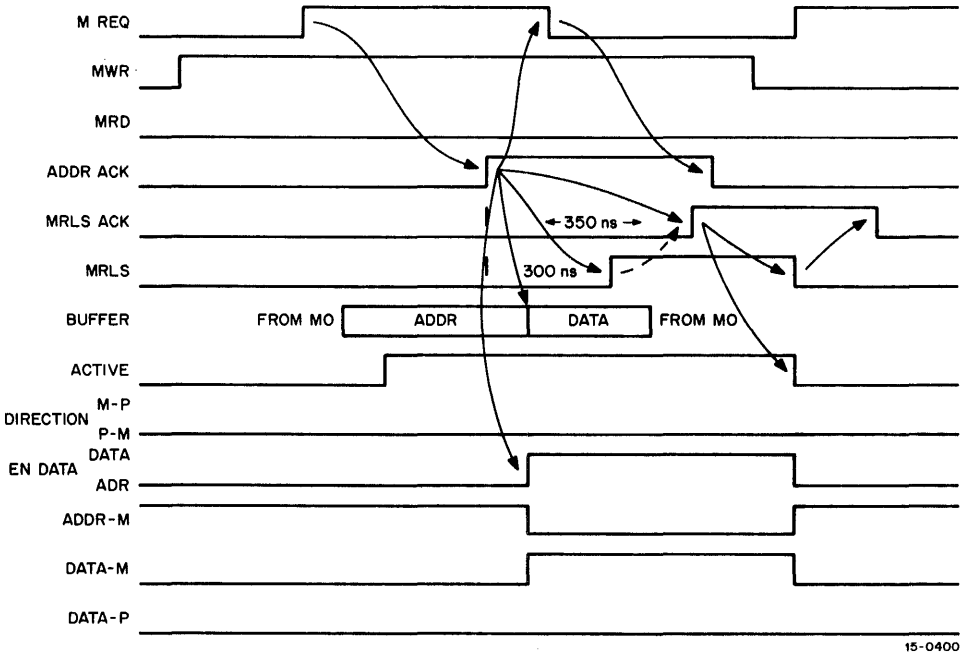


Figure 4-2b MX15-A Timing Diagram

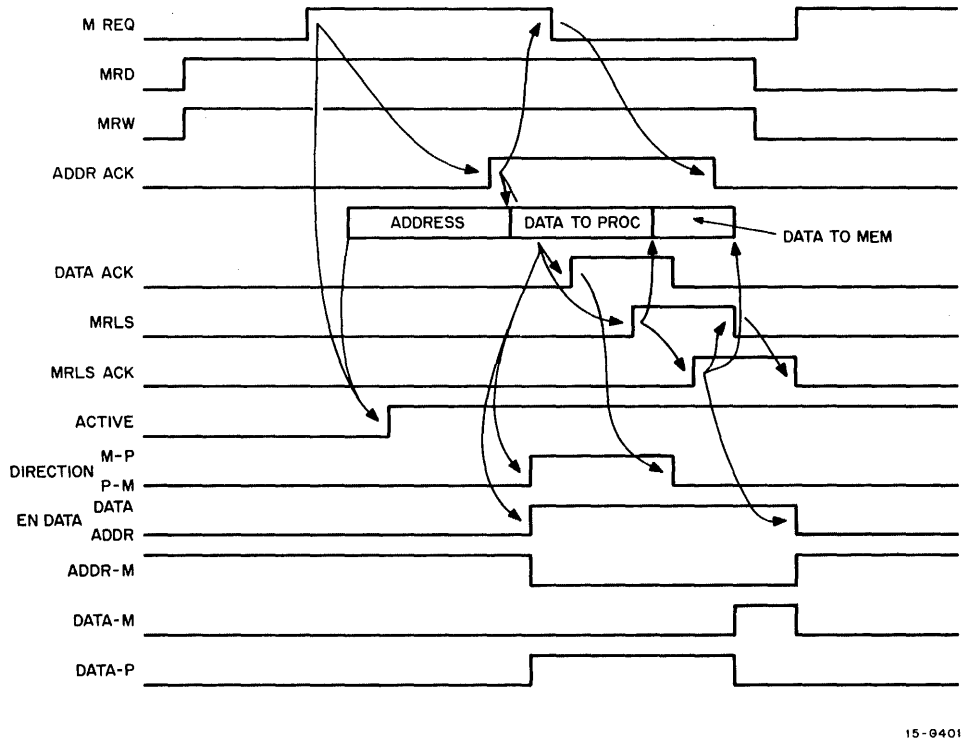


Figure 4-2c MX15-A Timing Diagram

bank addresses. When any one of these addresses is received by the MX15-A, the REQ ACTIVE flip-flop is set. Setting the REQ ACTIVE flip-flop initiates a timing sequence for generating a secondary memory request signal for the core memory and enables the control circuits; consequently, the address and the data can be orderly transferred through the multiplexer.

The secondary memory request signal is derived from the MEM REQ EN (memory request enable) and the REQ ACTIVE signals. The MEM REQ EN flip-flop is set at the end of the previous memory cycle by the MRLS ACK (memory release acknowledge) signal. Therefore, when the processor currently accessing memory issues the next M REQ (memory request) signal, the MEM REQ EN flip-flop has already been set. Setting an REQ ACTIVE flip-flop starts the sequence for generating the secondary memory request signal and also inhibits the address decode logic for all three input ports for the duration of the memory cycle. If more than one input memory port receives a memory request at the time the MX15-A is reset by the MRLS ACK signal, the corresponding REQ ACTIVE flip-flop will be set, and the priority logic will pass only the higher priority request. After the secondary memory request signal is issued by the MX15-A, the M REQ signal from the processor is terminated in response to the ADR ACK (address acknowledge) signal from the memory. The termination of the M REQ signal causes the MEM REQ EN flip-flop to be reset, thereby terminating the secondary memory request signal.

Two flip-flops are included in the control circuits: DIRECTION and EN DATA XFER (enable data transfer). Both of these flip-flops are in the reset state at the start of the memory request cycle. When these flip-flops are reset and when the REQ ACTIVE flip-flop is set, the address-to-memory control signal is applied to the bidirectional switches. This signal causes the address on the input memory bus MDL to be transferred to the output bus MDL and distributed to the core memory. The address is gated through the multiplexer in this manner whether the subsequent data transfer is from memory-to-processor or from processor-to-memory. If the memory responds with an ADR ACK signal, either one or both of the control flip-flops (direction and enable data transfer) are set. The memory replies with an ADR ACK signal only if the bank address is valid. One flip-flop, EN DATA XFER, will always be set in response to an ADR ACK signal. Setting this flip-flop indicates the address transfer is complete and a subsequent data transfer is beginning. The EN DATA XFER state is required because address bits can be rotated; however, data bits must not be rotated. The direction of the data transfer is determined by the state of the direction flip-flop. This flip-flop is set in response to the ADR ACK signal only when a MRD (memory read) signal from the processor is present. The MRD and ADR ACK signals are ANDed at the input of the direction flip-flop. If the MRD signal is present, the flip-flop is set, and a memory-to-processor control signal is generated to gate the data from the memory through the bidirectional switches to the processor. If, however, the MRD signal is not present, the flip-flop remains in the reset state and generates a processor-to-memory signal, which in turn, produces the data-to-memory signal that gates data from the processor through the bidirectional switches to the memory. To reset the multiplexer in preparation for the next memory request cycle, the control and REQ ACTIVE flip-flops are reset, and the MEM REQ EN flip-flop is set by the DATA ACK and the MRLS ACK signals. These signals are produced in indirect response to the ADR ACK signal and are delayed until the data transfer is completed. The DATA ACK signal occurs before the MRLS ACK signal and resets the DIRECTION flip-flop. The MRLS ACK signal is shaped, delayed, and inverted in the multiplexer to provide an early and a late priority reset signal to reset the EN DATA XFER and REQ ACTIVE flip-flops, and to set the MEM REQ EN flip-flop. The early or late priority reset signal can be manually selected by specific jumper wire connections in the wirewrap field; these jumper connections enable an equal or an absolute priority mode, respectively. The equal priority mode affords interleaving access to memory by any two input ports.

An invalid memory address is indicated to the multiplexer when the memory does not respond with an ADR ACK signal, which should occur in direct response to the M REQ signal. If no ADR ACK signal is received by the multiplexer before the M REQ signal times out, a NO ADDR CLR (no address clear) signal is generated to reset the REQ ACTIVE flip-flop and to set the MEM REQ EN flip-flop. The M REQ signal is not removed unless the processor requesting memory is equipped with the memory protect option that is included in the KT15 Memory Protect/Relocate option. Failure to remove the M REQ signal causes the entire PDP-15 multiprocessor system, including the multiplexer, to lock up.

The RESET switch on the console of the processor requesting memory must be pressed to produce a PWR CLR (power clear) signal for resetting the system. If the processor is equipped with the KM Memory Protect option, the MEM REQ signal will be removed approximgtely 500 μs after it is passed by the MX15-A to the memory. The time is determined by setting a delay in the KM15 Memory Protect option.

4.2 DETAILED CIRCUIT ANALYSIS

4.2.1 Bidirectional Switches

All address and data transfers between processor and memory are accomplished via the bidirectional switches in the multiplexer. The basic switch configuration for one bit is illustrated in Figure 4-3. This switch configuration is used for transferring bits 05 through 17 of the address and the data. Two other variations of this switch configuration are employed for transferring bits 00 through 04; these bits are also used in the multiplexer to recognize and modify the address. The bidirectional switches

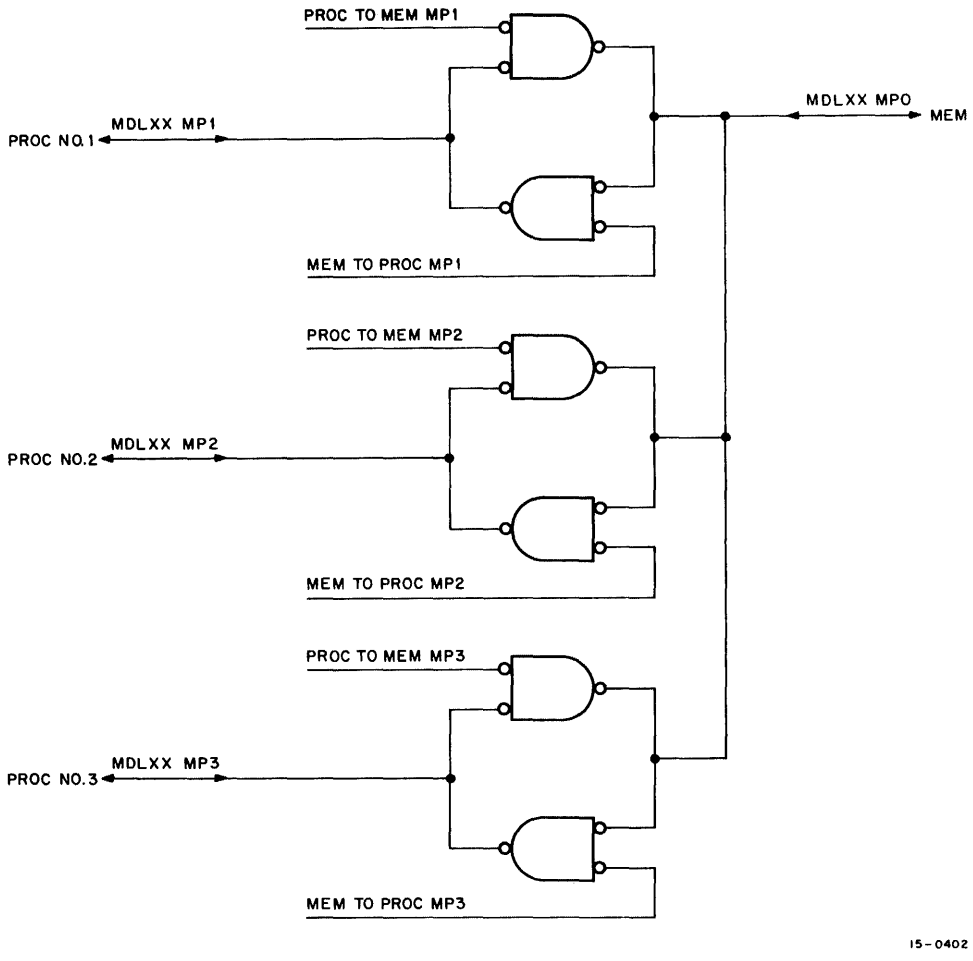


Figure 4-3 Bidirectional Switch

for bits 00 through 02 respond to data transfers in both directions but do not transfer the address bits to memory, and the switches for bits 03 and 04 incorporate a two-bit adder to rotate the bank address prior to transfer. A detailed description of the two-bit adder and associated bidirectional switches is presented in Paragraph 4.2.3. The bidirectional switches transfer the address and data in response to multiplexer control signals and also provide sufficient drive for the processor and memory MDLs.

4.2.2 Address Decode Gates

The block and bank address are recognized in the multiplexer by combinational logic. The combinational logic includes four NAND gates for each input port. Each NAND gate responds to one bank address (bits 03 and 04) and to the block address the bank is assigned (see Figure 4-4). Banks are assigned to a block on installation or in the factory by cutting two jumpers in a set of four. There is a set of four jumpers for each of the four NAND gates; consequently, each bank connected to the multiplexer output port can be assigned to a different block. The address decode circuits for each input port can be set up differently. The bank address can be rotated so that different input ports can access the same memory bank using a different bank address. Rotation of the bank address is accomplished by a two-bit adder that supplies the altered bank address bits to the address decode logic. By presetting the two-bit adder using the bank rotation switches, the bank address bits on the MDL can be rotated 8K, 16K, and 24K.

4.2.3 Two-Bit Adder

The two-bit adder presents the altered bank address bits to the address decode logic of the multiplexer and also to the memory output bus (MPO) via the associated bidirectional switches. A simplified logic diagram of the two-bit adder and the associated bidirectional switches is shown in Figure 4-5. The gates comprising the bidirectional switches are: A and B for bit 04, and C and D for bit 03. The binary adders are connected in series with the cross-coupled bidirectional switches; therefore, the altered bank address bits can be strobed onto the output memory bus (MPO) when an address is transferred to memory. Carries resulting from the two-bit adder are not propagated to address bit 02; therefore, the operation is termed "rotation" rather than translation or shifting. When data is strobed onto the MPO the binary adders are bypassed to transfer bits 03 and 04 unaltered.

4.2.4 Priority Control Circuits

The level of priority each input port assumes is determined by the output logic for the REQ ACTIVE flip-flops. Figure 4-6 illustrates the output logic for these flip-flops. The levels of priority are established by the request active output logic because the REQ ACTIVE MP1 flip-flop inhibits the

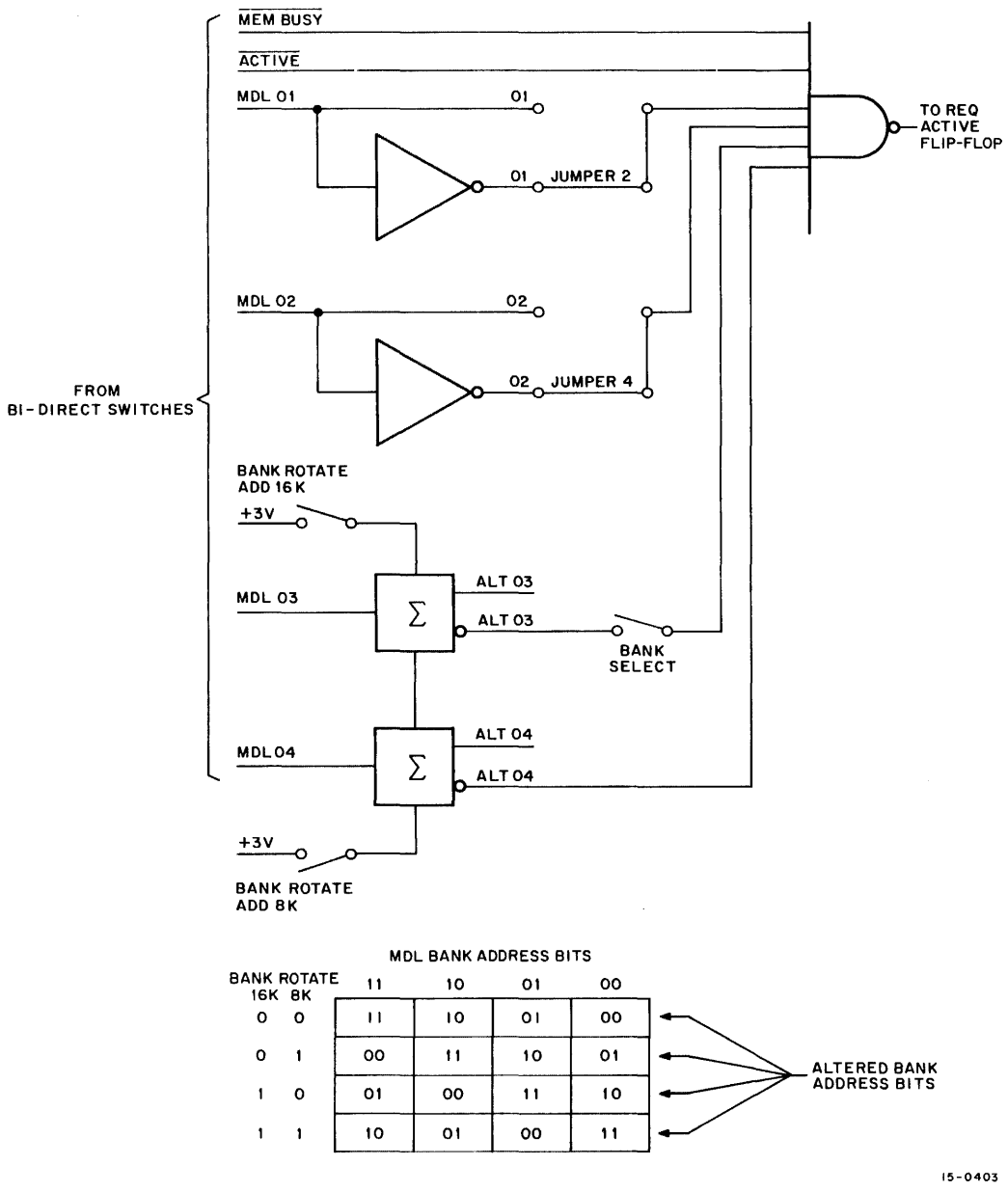


Figure 4-4 Address Decode Gate

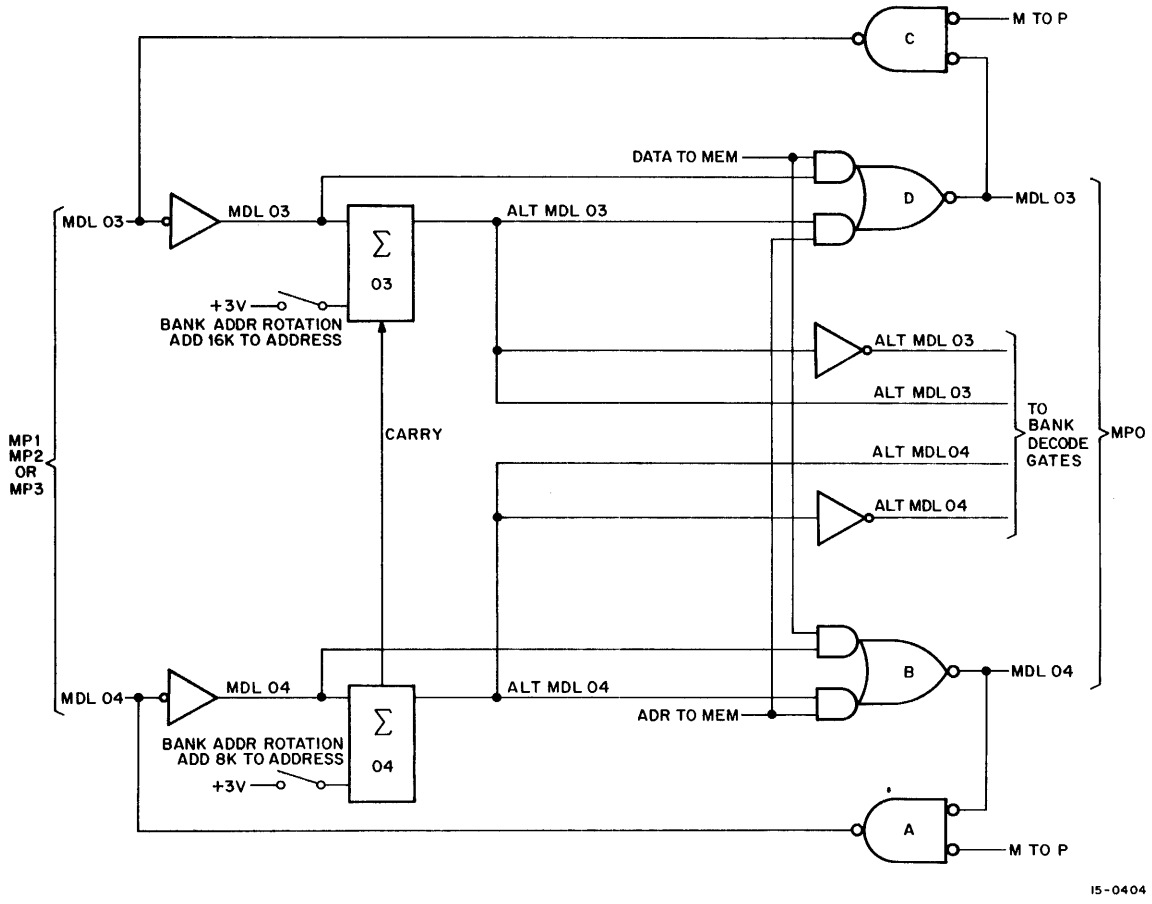


Figure 4-5 Two-Bit Adder

outputs of the REQ ACTIVE MP2 and MP3 flip-flops, and the REQ ACTIVE MP2 flip-flop inhibits the output of the REQ ACTIVE MP3 flip-flop. When an REQ ACTIVE flip-flop is set, the address decode gates for all input ports are disabled for the duration of the memory cycle; thus, no other REQ ACTIVE flip-flops can be set. In equal priority mode, the multiplexer is cleared before the next M REQ is received from the processor currently accessing memory, allowing a lower priority port to gain access to memory. This sequence allows two processors to alternately access memory (cycle stealing) on an equal priority basis for all data transfers except the back-to-back single-cycle I/O transfers and DCH transfers over the data channel. For back-to-back single-cycle I/O transfers and DCH transfers, special logic in memory ports 2 and 3 detects signal DCH SYNC, which locks out other processors. This logic is described in detail in Paragraph 4.2.5.

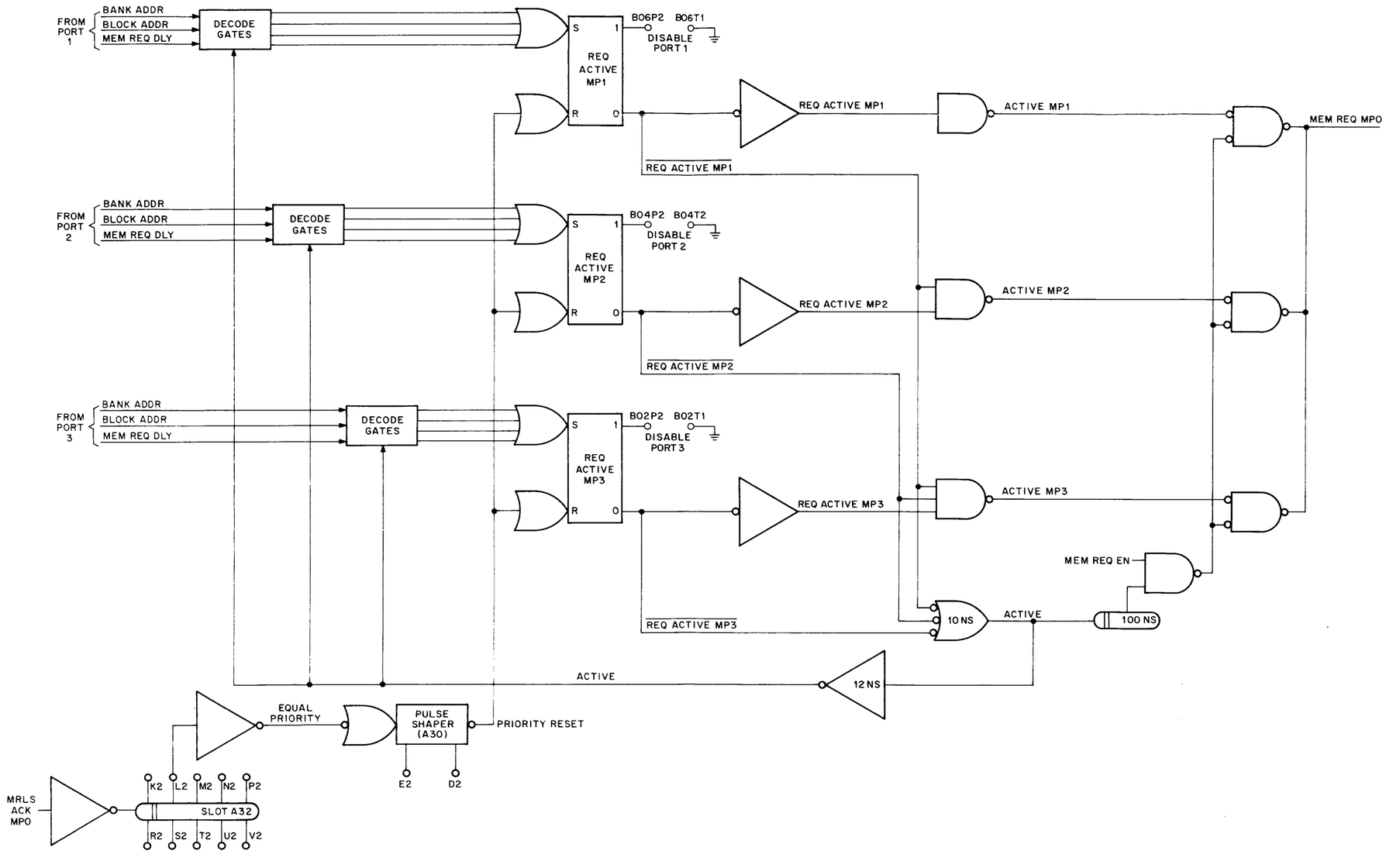


Figure 4-6 Priority Control Circuits

4.2.5 Inhibit Logic

The PDP-15 I/O processor must have continuous access to memory during its word count and current address cycles. Continuous access is enabled by the inhibit logic shown in Figure 4-7. The INHIBIT flip-flop is set in the following manner:

a. DCH SYNC becomes true prior to the beginning of a memory cycle;

b. When the MX15-A recognizes the correct address, MP* ACTIVE becomes true; and

c. REQ MPX becomes true producing the AND condition that sets the INHIBIT flip-flop.

NOTE

The INHIBIT flip-flop is set only after the MX15-A has processed the first of the sequential cycles. The INHIBIT flip-flop is reset with ADR ACK. During every cycle, ADR ACK tests the condition of SET INHIBIT to determine if it is true; if it is false, the INHIBIT flip-flop is reset.

SET INHIBIT is not true during two conditions:

a. The sequential transfer may have been completed, in which case, DCH SYNC is not true, and

b. The MP* ACTIVE flip-flop is not true because the data cycle is from the processor to a memory attached to a different MX15-A. In both cases, the INHIBIT flip-flop is reset.

The INHIBIT flip-flop is also direct reset by DCH SYNC becoming false. PWR CLR also resets the flip-flop. The logic in Figure 4-7 is duplicated in the MX15-A for memory ports 2 and 3.

NOTE

Normally the ADR ACK of the memory cycle following the completion of the transfer clears out the inhibit logic. When the inhibit logic is cleared following a transfer the processor that has just completed an I/O transfer continues to hold memory for one additional cycle.

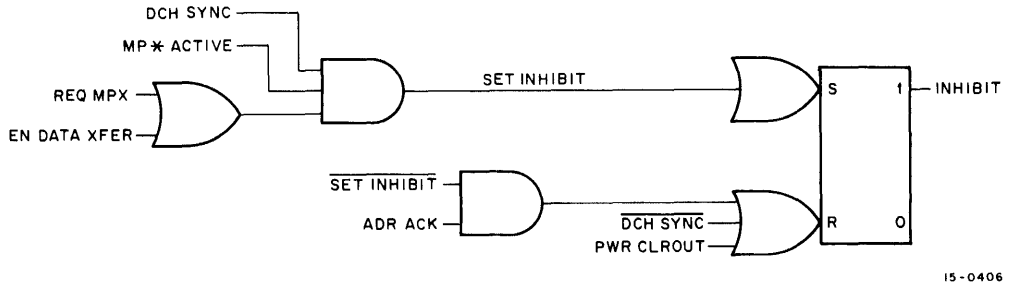


Figure 4-7 Inhibit Logic

4.2.6 M REQ Logic Timing

The M REQ signal and the proper address bits at an input memory port trigger the MX15-A to its active state. After a delay to ensure proper operation of the priority network, the M REQ signal is sent to the memory. When ADR ACK is received by the processor, the processor sets its M REQ signal false. The MX15-A detects this change in condition and sets the M REQ signal to memory false.

A timing and control flow diagram of the M REQ signals is shown in Figure 4-8. The M REQ signal from a processor causes an REQ ACTIVE flip-flop to be set in the MX15-A. An ACTIVE signal is generated, which is delayed 100 ns and ANDed with M REQ EN to become the MP0 M REQ to memory. When the M REQ signal at the processor becomes false, this condition is detected in the MX15-A causing a 50 ns pulse in the MX15-A called END M REQ L. END M REQ L resets M REQ EN, which sets MP0 M REQ to memory false.

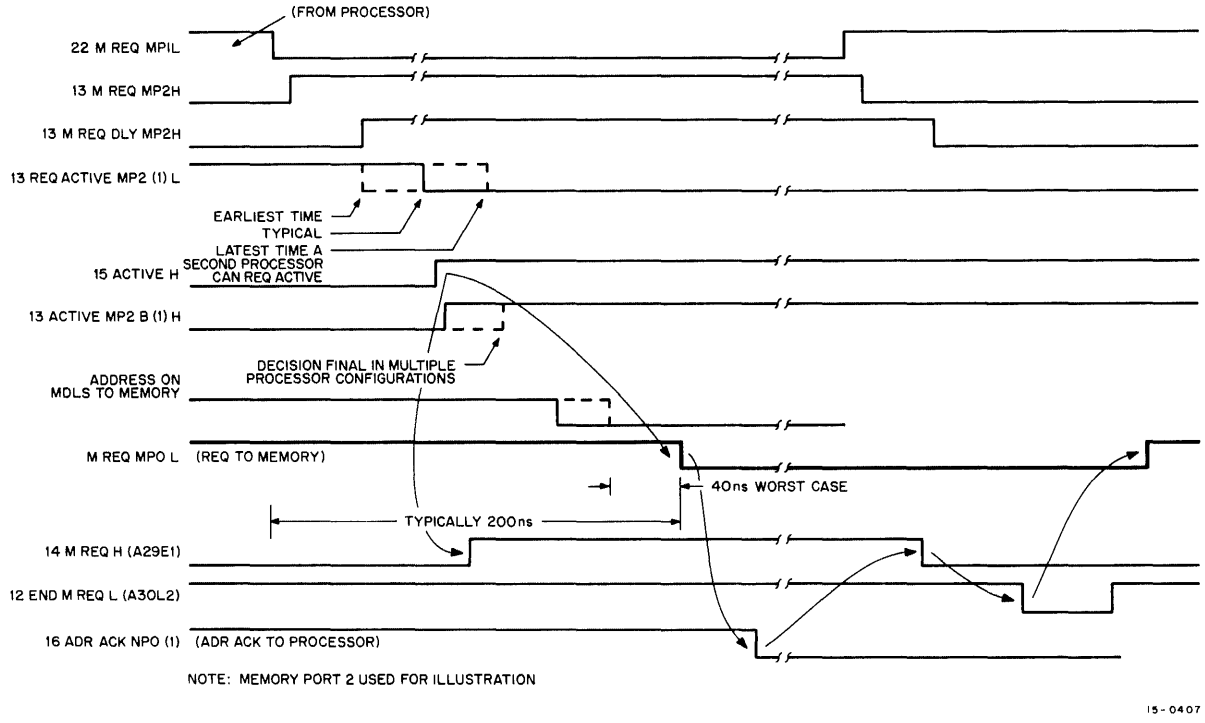


Figure 4-8 Priority and M REQ Timing

CHAPTER 5
DMA INTERFACE DESIGN

Chapter 2 of the PDP-15 Maintenance Manual describes the PDP-15 memory system. The chapter contains a definition of the control signals on the memory bus, a description of the control logic flow, and a description of the storage elements in the memory control logic. The user must understand these sections before proceeding.

Chapter 5 provides information for users who wish to connect their own devices directly to memory, using one of the MX15-A ports as a DMA channel.

5.1 MX15-A ADVANTAGES

5.1.1 Transfer Rate

Transfer rates of 925 kHz are possible; transfers at this rate may be any combination of read and write cycles. The read/pause/write transfer rate depends on the time spent in the pause (or modify) state. Rates exceeding 700 kHz are possible with conventional interfaces.

5.1.2 Latency

The waiting time required to gain access to memory is based on the following assumptions:

a. The processor is a KP15 equipped with KM15 and KT15 options.

b. The DMA device is assumed to have 12 ft of cable to the most remote MX15-A, and additional 12 ft to last memory (24 ft total device to memory length).

c. Times are specified as will appear on DMA to MX15-A cable at the DMA interface and do not include any buffer delay within the DMA device.

d. Read and Read-Modify-Write Cycles - leading edge of M REQ to leading edge of RD RST measured at DMA interface. This is time to access a memory location.

e. Write Cycles - leading edge of M REQ to leading edges of MRLS ACK. This is the time required to deposit a word in memory.

5.1.2.1 No Processor Activity to MX15-A of Interest

Read
M REQ - RD RST = 730 ns

Write
M REQ - MRLS ACK = 790 ns

5.1.2.2 Processor Activity Only (JMP. in user mode)

Read
M REQ - RD RST = 1.8 μs

Write
M REQ - MRLS ACK = 1.86 μs

5.1.2.3 Processor with DCH OUT transfer, DMA, WC, and CA all located in memory attached to same MX15-A.

Read
M REQ - RD RST = 4.13 μs

Write
M REQ - MRLS ACK = 4.2 μs

5.1.2.4 Processor with DCH OUT transfer, DMA, WC, CA, and DATA all located in memory attached to same MX15-A.

Read
M REQ - RD RST = 5.0 μs

Write
M REQ - MRLS ACK = 5.06 μs

5.2 SIGNAL TIMING CONSIDERATIONS

To start a memory operation, a 17-bit address must be placed on the MDLs, and MRD, MWR, or both must be set true. A minimum of 50 ns after these signals are set true, M REQ can be set true. All these signals must remain asserted until ADR ACK is received by the DMA device. The M REQ, address and MWR/MRD signals should be removed from the bus on the leading edge of ADR ACK. ADR ACK is received approximately 340 ns after the MX15-A has accepted M REQ. From this point on, each type of memory transfer requires a slightly different communications sequence. If the cycle is a read or read/pause/write cycle, the memory automatically sends RD RST to the DMA device, approximately 245 ns after sending ADR ACK. The leading edge of the RD RST should be used as a strobe to bring data into the device. RD RST will be de-skewed from the data by a minimum delay of 50 ns. When

the DMA device has strobed in the data, the DMA device sends DATA ACK. If it is a read cycle, MRLS can be sent simultaneously with DATA ACK. If it is a read/pause/write cycle, the DMA device places the new data on the bus after it has manipulated the data (no time limitation). A minimum of 100 ns later, the DMA device sends MRLS to the memory; the memory responds with MRLS ACK, at which time, data can be removed from the bus, the MRLS can be directly reset, and the next address can be placed on the bus.

If it is to be a write cycle, the data to be written into the memory can be placed on the MDLs after ADR ACK and the address are removed from the MDLs. A minimum of 100 ns later, the MRLS can be sent to memory, and the memory responds with MRLS ACK, at which time the data can be removed and MRLS reset.

5.3 MISCELLANEOUS SIGNALS

The paragraphs below list a variety of miscellaneous signals used in the DMA bus.

M BUSY B	This signal is an intermemory communications signal and has no function in a DMA interface.
M PAR	Parity is not offered with the MX15 option; therefore, this signal cannot be used with a DMA interface.
M PWR-OK	A ground on this signal indicates that the G829 module (in either one of the memories attached to an MX15-A) has detected a power malfunction and has shut down memory power. This signal can be used to shut down the DMA device.
PWR CLR	This signal goes to ground when power is removed from the DMA device. The PWR CLR signal should also be at ground until the DMA device is stabilized when powering up. The MX15-A is designed to reject any control signals that originate from a DMA device, when PWR CLR has been grounded. The MX15-A resets itself and the memory attached to it to the idle state from PWR CLR, if the REQ ACTIVE flip-flop from that port is set. If another REQ ACTIVE flip-flop is set, the PWR CLR is inhibited.

5.4 BACK-TO-BACK DMA BREAKS

5.4.1 Single Processor System

The PDP-15 processor is connected to memory port 3 on the MX15-A, and the DMA device is connected to memory port 2. Use the inhibit signal DMA SYNC (pin M2 on the control cable of the memory bus) and referred to as DCH SYNC on the MX15-A prints. The DMA SYNC signal, unlike the rest of the memory bus, has a high true value. To ensure back-to-back breaks, the DMA SYNC should go high with the first address of the block sent to memory; however, if DMA SYNC does not go high on the first address, it must go high no later than simulataneously with the MRLS of the first

cycle. DMA SYNC must remain high until the last cycle of the back-to-back set of breaks. DMA SYNC is lowered with the leading edge of ADR ACK of the last cycle. See Paragraph 4.2.5 for a description of inhibit logic in the MX15-A.

NOTE

If a system contains several MX15-As, the back-to-back guarantee only applies as long as the block addresses stay in the memory attached to a single MX15-A. If an MX15-A address boundary is crossed, the normal latency for the first access to that MX15-A occurs. Subsequent cycles will be back-to-back.

5.4.2 Dual Processor Systems

Memory port 1 must not be used for any DMA device that requires back-to-back facilities. Also, PDP-15 processors that have either DCH or back-to-back I/O transfers must be connected to memory ports 2 and 3.

5.5 WIRING GUIDELINES

The user must give careful attention to creating a solid ground mesh as described in Paragraph 5.3 of the PDP-15 Systems Interface Manual. Each MDL or control line should be buffered, and an M510 Positive Receiver module should be used to obtain maximum noise margins. An M611 or M111 module can be used with somewhat degraded noise margins but with less delay. The receivers should be located as close as possible to the DMA/memory bus cable slot locations. Maximum cable length from the DMA device to the furthest MX15-A is 21 ft. Custom interfaces to the MX15-A can be easily designed from standard modules, connectors, cables, and power supplies available from DEC.

The PDP-15 Systems Interface Manual, PDP-15 Systems Module Manual, and the DEC Logic Handbook provide extensive information on specific parts available.

5.6 MODULES FOR DESIGNING DMA INTERFACE

Table 5-1 lists a summary of modules useful in the design of a DMA interface. These modules are described in detail in the PDP-15 Module Manual.

Table 5-1
Modules for DMA Interface Design

Module Type	Description
M311 Tapped Delay Lines	Contains two tapped delay lines. Each has a 250-ns maximum delay, with taps every 25 ns.
M312 Delay Lines	Contains six delay lines, including four 50-ns delays, one 30-ns delay, and one 0-40 ns delay. These are useful for setting timing within DMA interfaces and providing skew between data and strobes.
M621 Data Bus Driver	An inverting driver that has two inputs. Ideal for switching between address and data source registers.
M622 I/O Bus Driver	A noninverting driver, useful for control signal driving.
M902 Terminator	Must be used to terminate both the MDL and control cable at the MX15-A.
M911 Memory Bus CP Terminator	Provides a source of current to both the M621 and M622 open-collector drivers.
G829 Power Connector	Provides power control and protection.
G827 Power Sequence and Delays	Used to create a DMA PWR-OK signal.

CHAPTER 6
MAINTENANCE

The maintenance procedures presented in this chapter are limited to those procedures required for maintaining and testing the MX15 multiplexer equipment bays. Procedures for maintaining the PDP-15 computer system are contained in the PDP-15 Maintenance Manual. The maintenance philosophy to be followed for the MX15 should be preventive in nature, that is, an optimum amount of preventive procedures performed on a routine schedule will eliminate many costly equipment breakdowns and forecast impending failures before they occur. If a failure does occur, the modular design of the MX15-A minimizes repair and down-time.

6.1 PREVENTIVE MAINTENANCE

The MX15-A option contains no special mechanical devices and is housed in a standard PDP-15 equipment bay; only standard computer system maintenance procedures are required to ensure reliable operation of the equipment. Troubles encountered in the MX15-A should be recorded in the established PDP-15 maintenance log for future reference. Regular entries in the maintenance log of maintenance performed, troubles encountered, and corrective measures taken can serve as a powerful tool in maintaining system reliability.

6.1.1 Voltage Checks

Diagnostic programs referenced in Paragraph 1.4 and power supply voltage checks should be performed at regular intervals to verify proper operation of the MX15-A and associated core memory banks. Power supply output voltages and tolerances are listed in Table 6-1. Because each equipment bay has its own power supplies, the voltage checks must be performed on each bay. Perform the voltage checks on the core memory banks in accordance with the PDP-15 Maintenance Manual.

Table 6-1
Voltage Tolerances

Voltage	Tolerances
+5V	±100 mV (output of G829)
+10.5V	±10%
-13V	±0.2V
-30V	±2.0V
-6V	±200 mV
-25V (Memory +V and -V)	±1.0V

6.1.2 Margin Checks for Multiprocessor and DMA Systems

Periodically check the equal priority margins to confirm that margins exist as described in Paragraph 2.6.

6.2 CORRECTIVE MAINTENANCE

The simplicity of the MX15-A multiplexer and the logic description provided in this manual, in addition to the results of the diagnostic tests, normally permit the use of standard troubleshooting techniques for isolating a malfunction quickly and efficiently. If the priority circuits of the MX15-A multiplexer are suspected to be the malfunction, perform the multiple port jumping test described in Paragraph 6.3.3.1 to verify the operation of these circuits. For economical maintenance under most conditions, replace the inoperative module with a spare module, and return the defective module to DEC for repair or replacement. DEC offers an optional spare modules kit containing one spare of each infrequently-used module and two of each frequently-used module. Recommended spare modules are listed in Table 6-3. All modules except the DEC type M628 are included in the basic PDP-15 computer spare modules kit; therefore, the M628 module should be considered as an additional spare requirement for an MX15 installation.

6.2.1 Test Equipment Required

Maintenance activities for the MX15 require standard hand tools, test cables, and probes and the standard test equipment and special materials listed in Table 6-2.

Table 6-2
Test Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 453 or equivalent
Probe (2)	Tektronix	P6010
X10 Probe (2)	Tektronix	P6008
Module Extender	DEC	Type W982

6.2.2 Specific Troubleshooting Techniques

If a malfunction occurs in the MX15 system, the following paragraphs can be used as guidelines for tracing and isolating the malfunction.

6.2.2.1 Checking Priority Multiple Port Jumping Test

Step	Procedure
1	Connect PDP-15 computer system as shown in Figure 6-1.
2	Connect the oscilloscope to monitor the output of the REQ ACTIVE MP1 gate.
3	Set the address and data switches on one console to access memory and to start a jumpself loop or a short program (JMP .-1). ACTIVE MP1 should become high.
4	Connect the oscilloscope to monitor the REQ ACTIVE MP2 gate.
5	Set the MP1 Bank Select switches on the MX15-A to 0. ACTIVE MP2 should become high.
6	Connect the oscilloscope to monitor the REQ ACTIVE MP3 flip-flop.
7	Set the MP2 Bank Select switches on the MX15-A to 0. ACTIVE MP3 should become high.

6.2.2.2 Indications of Cable Problems - The most common cable fault is an open connection. Generally, a single wire will open. If an MDL cable opens the indications of a malfunction are:

a. a given bit position (both address and data) will always be read into the MMA and MMB as a 1 (as seen on the indicator bus),
b. when the location is read, the MB on the console will show a 0 in that bit position.

A grounded cable connected to the processor is indicated by a 1 that cannot be cleared from the MDL lines (as examined on the indicator bus). Opens and shorts on the control line cable are more difficult to detect.

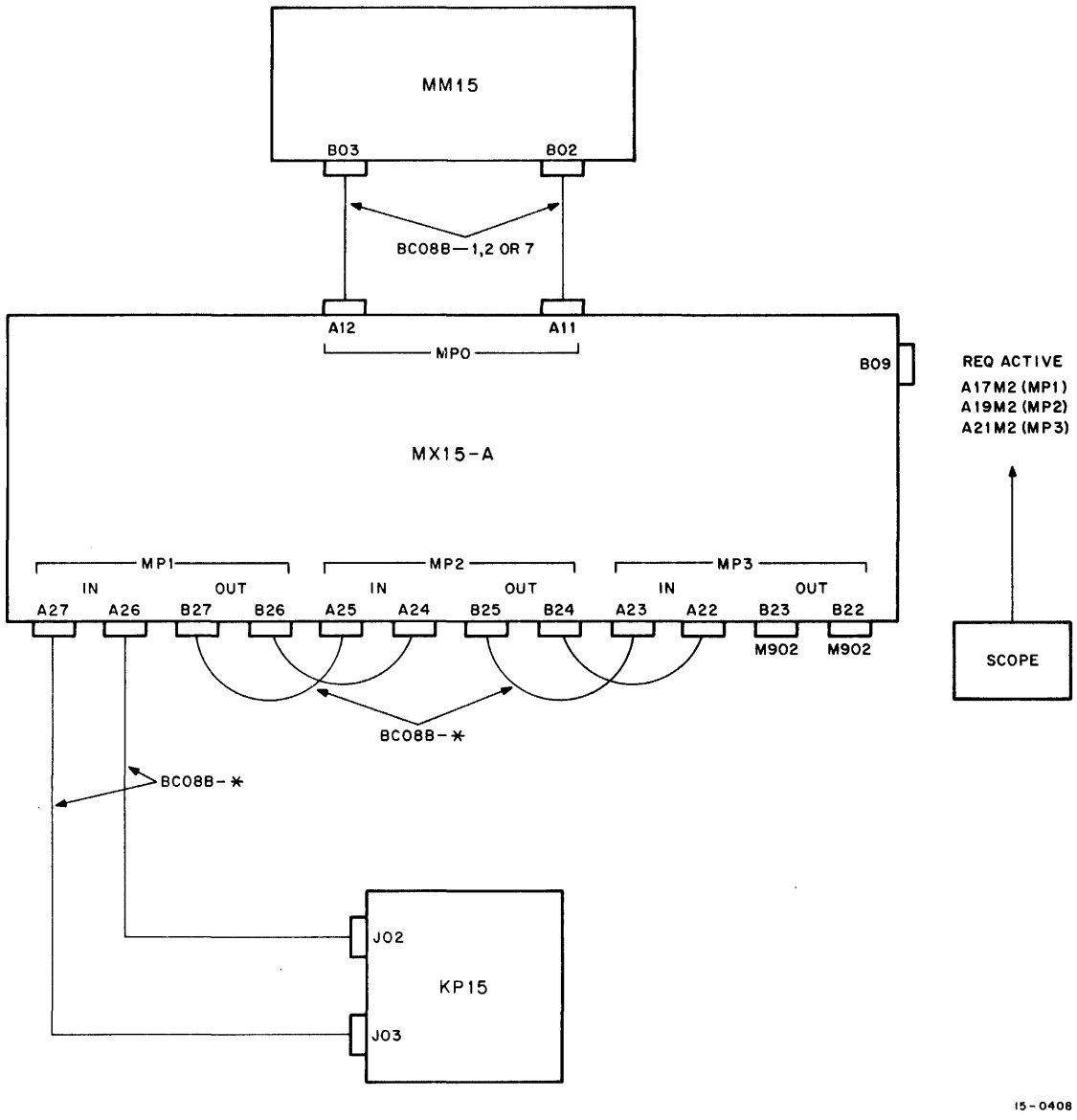


Figure 6-1 Multiple Port Jumping Test Interconnections

6.2.2.3 Indications of Driver/Receiver Malfunction - A malfunction in the drivers is usually an open, i.e., the driver can no longer pull the bus to ground. When a driver in the processor-to-memory direction is defective, it is indicated by:

a. the MMB and MMA in the bit position is always a 0, regardless of what is attempted to be deposited,

b. the contents of the MB will also be a 0 when the location is examined.

A driver in the memory-to-processor direction that is open has the following characteristics:

a. MMA and MMB always obtain the correct data and address, however, when the location is examined, the MB receives a 0 at the bit position.

Failures in the control signal drivers are more difficult to trace.

6.2.2.4 Add-to-Memory and Read Modify Write RMW Malfunctions - Because the real-time clock uses the RMW cycles and the add-to-memory feature, the real-time clock is a convenient test feature for examining any problems that may occur with add-to-memory, word count, and current address cycles of DCH breaks.

6.2.2.5 Processor-Memory Lockup - The MST, MDL, MMA, and MMB positions on the processor indicator bus can be used to determine the state of the memory and processor. Monitoring these four positions can provide extensive troubleshooting information.

NOTE

Ensure that these four positions do not contain the OR of several memory blocks (refer to Paragraph 1.2.1.12).

To troubleshoot the MX15-A, the procedures below should be followed:

Step	Procedure
1	Examine the ACTIVE MP* signal for the memory port in question.
2	Check the M REQ signal from the processor at the input and output to the MX15-A.
3	Check ADR ACK (on the MST position).
4	Check the MRLS and MRLS ACK.

A complete understanding of the control logic in this manual will aid in tracing problems.

6.3. SPARE MODULE REQUIREMENTS

Table 6-3 lists recommended spare modules for the MX15-A. The logic layout of the MX15-A is sectionalized so that certain modules are used only with a single memory input port. If the port is

not used in a particular system, then the set of modules exclusively associated with that port can be temporarily removed and used as spares, as needed for the other two ports in the MX15-A. The table indicates the modules that can be used as spares if memory port 1 is not used.

Table 6-3
Spare Module Recommendations

Recommended Spare Modules for MX15-A		Spares Available if Memory Port 1 is Not Used	
Type	Quantity	Quantity	Location
G827	1		
G829	1		
M111	1		
M133	1		
M135	1		
M139	1	2	B06, B07
M311	1		
M312	1		
M602	1		
M622	3	3	A15,A20,A21
M627	1		
M628	1	1	A10
M902	1		
M911	1	1	A26 or B26
W714	1	2	A08, A09

6.4 ENGINEERING DRAWINGS

A complete set of MX15 Memory Bus Multiplexer enginerring drawings is provided in Volume 2 of this maintenance manual. These drawings are under DEC revision control and are updated as required by ECOs (Engineering Change Orders). The Drawing Index List, Table 6-4, lists all the drawings that are included in Volume 2 in the order that they appear.

Table 6-4
Drawing Index List

Size	Type	Number	Title
D	AD	7006863-0-0	MX15 Maximum Configuration
D	UA	MX15-0-0	MX15 Assembly
D	BS	MX15-A-12	Priority Logic Input Port 1
D	BS	MX15-A-13	Priority Logic Input Port 2
D	BS	MX15-A-14	Priority Logic Input Port 3
D	BS	MX15-A-15	MDL 03, 04 Drivers, M REQ Logic

(continued on next page)

Table 6-4 (Cont)
Drawing Index List

Size	Type	Number	Title
D	BS	MX15-A-16	Control Lines
D	BS	MX15-A-17	MDL 0-8
D	BS	MX15-A-18	MDL 9-17, Parity
D	BS	MX15-A-19	Inhibit Logic
D	IC	MX15-A-20	Memory Port Out
D	IC	MX15-A-21	Memory Port 1
D	IC	MX15-A-22	Memory Port 2
D	IC	MX15-A-23	Memory Port 3
D	AD	7006862-0-0	Wired Assembly (MX15-A)
D	UA	841-B-0	Power Control 841-B, 841-C
D	CS	H721-0-1	H721 Power Supply Circuit Schematic
B	CS	798-0-1	798 Dual 15-Volt Power Supply Schematic
		15-0409	856 Power Control

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