Priority Control

# student workbook introduction to the pdp11

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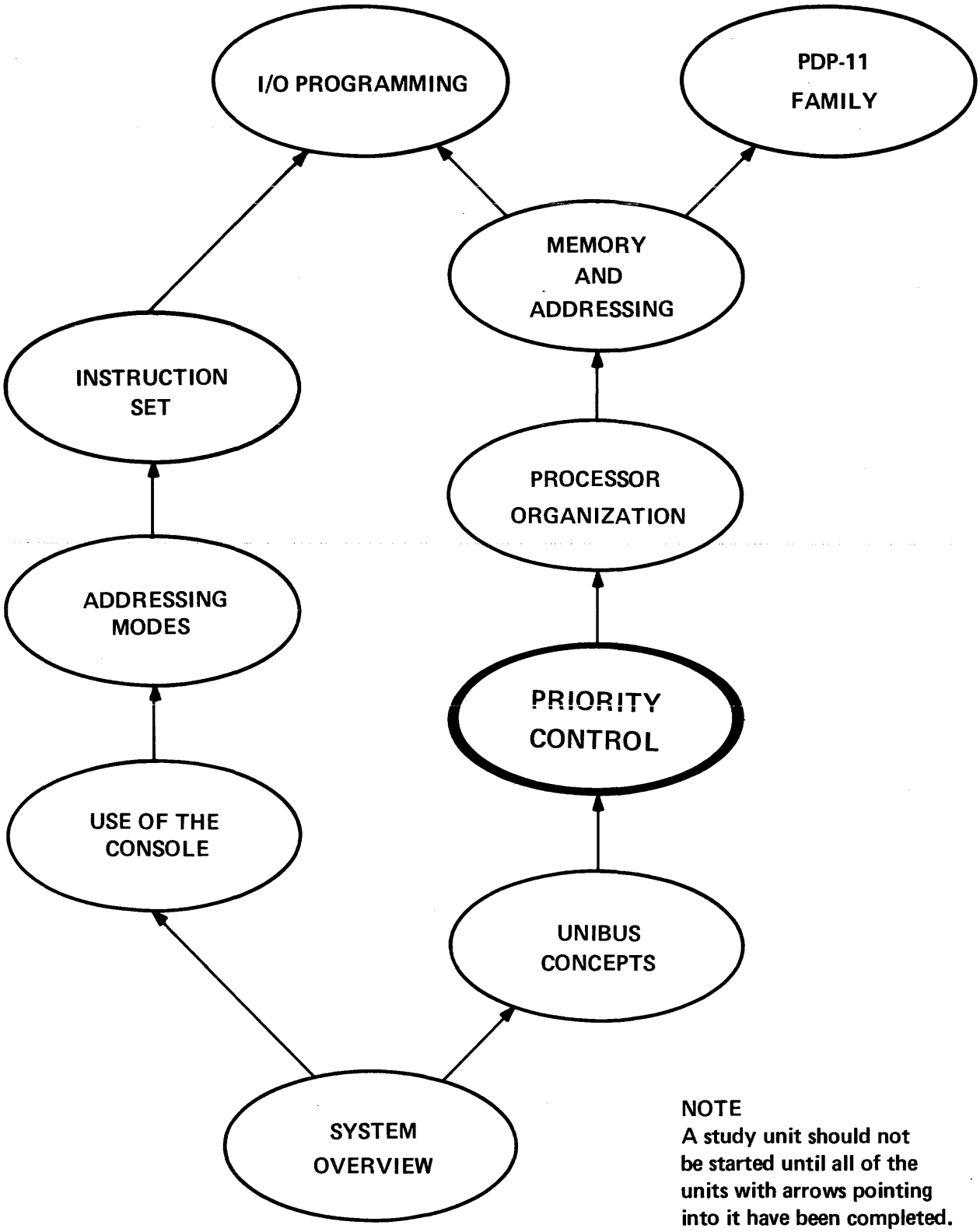
# course map




NOTE
A study unit should not be started until all of the units with arrows pointing into it have been completed.

read on

READ
LEARNING
OBJECTIVES
(page 1)

NOW RUN FILM
CARTRIDGE

REVIEW
MATERIAL
(pages 3 – 9)

TAKE TEST &
CHECK RESULTS
(pages 11 – 14)

ANY
INCORRECT
ANSWERS

YES

PLEASE REVIEW THE
MATERIAL YOU'RE
HAVING DIFFICULTY WITH.
(ADDITIONAL RESOURCES ARE
LISTED ON PAGE 2.)

NO

GOOD WORK!
NOW GO ON TO THE
NEXT STUDY UNIT.


read on

# objectives

After completing this study unit you should be able to . . . .

★ Explain why the PDP-11 uses a priority system for gaining control of the bus.

★ Describe how the PDP-11 priority system is organized into vertical priority levels with a horizontal priority at each level.

★ Explain the difference between "vertical" and "horizontal" priority.

★ Explain how the PDP-11 handles simultaneous bus requests from two or more devices. This includes:

- Priority arbitration for vertical priority.
- Chaining or "bus latency" for horizontal priority.
- Granting of the bus to a device based on its position in the overall priority structure.

★ Identify the Unibus control lines that are used for priority arbitration functions.

★ Explain the factors that must be considered when assigning device priorities. These factors include:

- Operating speed
- Data recovery
- Service requirements

★ Explain the significance of the term "direct memory access" (DMA) and be able to identify typical DMA devices, indicating why they are assigned both a BR and NPR level.

★ Describe the programmable priority used for the CPU and show how the CPU's priority is used for "masking" device interrupts.

★ Be able to assign suitable priority levels, both vertical and horizontal, to typical PDP-11 devices.

# additional resources

| | |
|---|---|
| • **PDP-11/04/05/10/35/40/45 Processor Handbook** | Read Chapter 2, Paragraph 2.4 (Automatic Priority Interrupts). |
| • **PDP-11 Peripherals Handbook** | Read Chapter 5, Paragraphs 5.3.2, 5.3.3, and 5.3.4; Paragraph 5.6 (Priority Arbitration Transactions); and Paragraph 5.8.3 (Priority Chaining). |

The following material is covered in this study unit:

| *Topic* | *Key Points* | *Visual Ref.* |
|---|---|---|
| **basic concepts** | ★ The PDP-11 priority system determines which device obtains the bus.<br>• Each PDP-11 device is assigned a specific location in the priority structure.<br>• Priority arbitration logic determines which device obtains the bus according to its position in the priority structure. | — |
| **priority structure** | ★ The priority structure is 2-dimensional; i.e., there are vertical priority levels and horizontal priority at each level. | — |
| **vertical priority** | ★ There are five vertical priority levels decreasing in priority from the top. A requesting device on one level is serviced before any lower level is handled.<br>• The highest level is the NPR level.<br>• The next highest level is BR7, followed by BR6, BR5, and BR4. | 9 |
| **NPR level** | ★ Highest vertical priority level.<br>★ Devices at NPR level are honored between bus cycles.<br>★ Used for obtaining bus for DMA transfers that do not involve the CPU. | 10–13 |
| **honoring NPRs** | ★ There are two lines associated with the NPR priority level.<br>• The device makes its request on the non-processor *request*, or NPR line.<br>• The priority control responds by issuing a grant on the non-processor *grant*, or NPG line. | 14 |

read on

| *Topic* | *Key Points* | *Visual Ref.* |
|---|---|---|
| **honoring BRs** | ★ There are two lines associated with *each* BR level.<br>• The bus request is made on a BR line (BR7, BR6, BR5, or BR4).<br>• The bus grant is made on the corresponding grant line (BG7, BG6, BG5, or BG4).<br>★ BR levels BR3 through BR0 are *only* used by the CPU; devices are *not* assigned to these BR levels.<br>★ Unlike NPRs, a BR can only be handled between instruction cycles.<br>★ The BR levels are used for interrupts so that the device can obtain help from the CPU.<br>★ Any request made at a BR level requires processor intervention. | 15–19 |
| **CPU priority** | ★ In addition to device priority levels, the CPU has a programmable priority.<br>• The CPU can be set to any one of eight priority levels.<br>• The priority is not fixed; it can be raised or lowered by the program that is running.<br>★ For example, the CPU priority can be elevated from level 4 to level 6 when the CPU stops servicing a BR4 device and starts servicing a BR6 device.<br>★ This programmable priority feature permits *masking* of bus requests.<br>• The CPU can hold off servicing lower priority devices until more critical tasks are completed.<br>• For example, when CPU priority is set to level 6, all bus requests on the *same* and *lower* levels are ignored (in this case, all requests appearing on BR4, BR5, and BR6). | 21–23 |

read on ➧

| *Topic* | *Key Points* | *Visual Ref.* |
|---|---|---|
| **horizontal priority** | ★ Because there are only five vertical priority levels, it is often necessary to connect more than one device to a single level. When a number of devices are connected to the same level, it is referred to as horizontal priority. | 24, 25 |
| **multiple requests** | ★ If more than one device makes a request at the same level, then the device electrically closest to the CPU has the highest priority. | 26 |
| **NPR chaining** | ★ The grant line for the NPR level is connected to all devices on that level in a "daisy chain" arrangement.<br>• When an NPG is issued, it first goes to the device closest to the CPU. If that device did not make the request, it permits the NPG to travel to the next device.<br>• Whenever the NPG reaches a device that has made a request, that device captures the grant, and prevents it from passing to any subsequent device in the chain. | 27–29 |
| **BR chaining** | ★ BR chaining is identical to NPR chaining in function. However, each BR level has its own BG chain. Thus, the grant chain for BR7 is the BG7 line which is chained through all devices at the BR7 level. | 30 |
| **total priority structure** | ★ Any PDP-11 device fits into a 2-dimensional priority structure.<br>• It is assigned to one of the five vertical levels (NPR, BR7–BR4).<br>• Its distance from the CPU on the assigned level determines its horizontal priority. | 31 |
| **bus latency** | ★ Bus latency refers to the device's distance from the CPU on a horizontal line. In other words, the device closest to the CPU has the highest priority. | 31 |

read on

| *Topic* | *Key Points* | *Visual Ref.* |
|---|---|---|
| **direct memory access (DMA)** | ★ Direct memory access (DMA) refers to a device that does not require help from the CPU. A DMA device can obtain the bus and perform a data transfer without CPU intervention. | 32 |
| **devices using both NPR and BR levels** | ★ Direct memory access (DMA) devices operate at both the NPR and BR levels.<br>• The NPR level is used to perform data transactions without CPU help.<br>• A BR level is used when the device interrupts the CPU to let it know the transaction is complete or that an error condition exists. | 32 |
| **priority assignments** | ★ When assigning priorities to a device, three factors must be considered: operating speed, ease of data recovery, and service requirements. | 33–36 |
| **operating speed** | ★ Data from a fast device is available for only a short time period. Therefore, highest priorities are usually assigned to fast devices to prevent loss of data and to prevent the bus from being tied up by slower devices. | 37 |
| **data recovery** | ★ If data from a device is lost, recovery may be automatic, may require manual intervention, or may be impossible to recover. Therefore, highest priorities are assigned to devices whose data cannot be recovered while lowest priorities are reserved for devices with automatic data recovery features. | 38 |
| **service requirements** | ★ Some devices cannot function without help from the CPU; DMA devices can operate independently and require only minimal CPU intervention. Thus, devices requiring continual help from the CPU for servicing are assigned the lowest priorities to prevent tying up the CPU. | 39, 40 |

read on ➧

| *Topic* | *Key Points* | *Visual Ref.* |
|---|---|---|
| **typical priority assignments** | ★ Table A shows typical priority assignments for different types of PDP-11 devices. Note that DMA devices use two levels: the NPR level for data transfers; the BR level for functions requiring CPU intervention. | 41–49 |

**TABLE A**
**TYPICAL PRIORITY ASSIGNMENTS**

| Device | Priority | NPR Level |
|---|---|---|
| A/D Converter | *BR7 | – |
| DECtape | BR6 | Yes |
| Line Clock | BR6 | – |
| Real Time Clock | BR6 | – |
| Disk Pack | BR5 | Yes |
| Disk Cartridge | BR5 | Yes |
| Magnetic Tape | BR5 | Yes |
| DECwriter | BR4 | – |
| Line Printer | BR4 | – |
| Teletype | BR4 | – |
| Paper Tape Reader/Punch | BR4 | – |

*For sampling at high rates. Can be assigned to a lower BR level for slow input applications.

read on

| *Topic* | *Key Points* | *Visual Ref.* |
|---|---|---|
| **priority arbitration** | ★ When more than one device requests the bus, the priority arbitration logic decides who gets the bus, based on the priority structure. | 57, 58 |
| **location** | ★ Priority arbitration logic resides in the CPU but is electrically divorced from it.<br>• The CPU is treated as a bus device.<br>• When no other device wants the bus, control automatically reverts to the CPU. | 59 |
| **arbitrating bus requests** | ★ When two devices, say a BR7 and a BR6 device, both make a simultaneous request, the two requests enter the priority arbitration (PA) logic which acts as an umpire.<br>★ The priority arbitration logic issues a grant to the device with the highest priority, in this case, a BG7.<br>★ The BR7 device then issues SACK while waiting for the bus; the BR6 device keeps its request up.<br>★ When the BR7 device drops SACK and asserts BBSY to take over the bus, the PA is again free to act as an umpire and will honor the BR6 request next.<br>★ Note that the PA arbitrates between bus levels; i.e., it determines which device has the highest vertical priority level. Horizontal priority is not arbitrated by the PA; it's dependent on bus grant line chaining. | 60, 61 |
| **overlapping** | ★ Priority arbitration can be performed at the same time a data transaction or interrupt is being performed.<br>• While one device is using the bus, the PA is free to monitor other requests and issue an appropriate grant. | 66 |

read on ➧

- As soon as the first device is finished with the bus, the next device can immediately take over. There is no time lag when passing bus control from one device to another.

**NOTE**

**Visuals 62 through 76 and the accompanying narration summarize the material covered in this study unit.**

**When you have completed the study unit, please take this self-scoring test. Then compare your answers against the "answer sheet" which can be obtained from your supervisor. Based on your test results, either review the appropriate material in this study unit or proceed to the next unit in the series.**

1. Explain the purpose of the PDP-11 priority control system.

2. Indicate which of the following statements are true regarding vertical priority.

   (a) T – F BR levels are different from NPRs because they are programmable.

   (b) T – F A DMA device can only operate at the NPR level.

   (c) T – F Any request made at the BR level requires CPU intervention.

   (d) T – F All requesting devices on one level are serviced before devices on a lower level.

   (e) T – F Requests at the NPR level are handled between instruction cycles only.

   (f) T – F A device that cannot perform DMA transfers may be assigned the NPR level when a high priority is required.

3. Match each of these vertical priority levels with its corresponding function.

   (a) NPR (b) Priority Level 3 (c) BR7 (d) BR4

   ( ) Highest level for device interrupts.

   ( ) For DMA transfers only.

   ( ) Lowest level for device interrupts.

   ( ) Not used for devices; used only by CPU.

read on

4. The CPU is operating at the BR5 level when a disk, also operating at the BR5 level, issues a bus request in order to interrupt the CPU. What happens?

   (a) The disk receives a BG5 grant and interrupts the CPU.

   (b) The disk receives an NPR grant and interrupts the CPU.

   (c) The disk's bus request is not honored at this time.

5. Indicate why horizontal priority is also needed in the PDP-11.

6. Which of the following statements are true?

   (a) T – F When two or more devices at *different* priority levels request the bus simultaneously, the one closest to the CPU has priority.

   (b) T – F When two or more devices at the *same* level request the bus simultaneously, the one closest to the CPU has priority.

   (c) T – F The priority arbitration logic cannot distinguish among requests made at the same priority level.

   (d) T – F Only one device can be connected to any vertical priority level.

   (e) T – F When two or more devices at the same level request the bus simultaneously, the priority control must arbitrate the requests to determine which device has the higher priority.

read on

7. There are two lines associated with each of the five device priority levels. Name these five pairs of lines and describe what is meant by "priority chaining."

8. Indicate which of the following statements are true for DMA devices.

   (a) T – F DMA means that the device can communicate with other devices without help from the processor.

   (b) T – F DMA devices can perform data transfers at either NPR or BR levels.

   (c) T – F DMA devices can perform data transfers at the NPR level but can also use the BR level for other purposes.

9. Specify the 3 factors to be considered when assigning device priorities.

   (1)

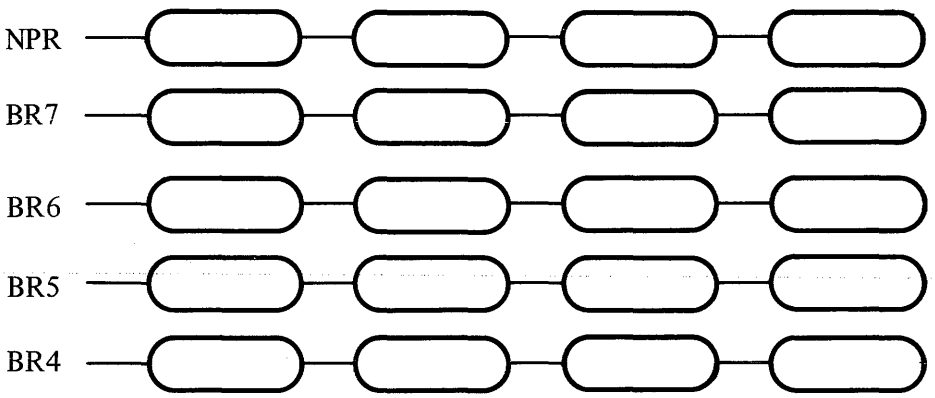
   (2)

   (3)

read on

10. Assign the following devices to the appropriate location in the priority structure shown below.

| | |
|---|---|
| ADC | analog-to-digital converter (high-speed) |
| DISK | disk (DMA device) |
| LP | line printer |
| DEC-T | DECtape (DMA device) |
| LC | line clock |
| RDR/P | reader/punch |
| MAG-T | magnetic tape (DMA device) |
| TTY | teleprinter or DECwriter |




11. The following steps indicate operations performed by both the priority control and the bus device when a device requests bus control. Place these steps in their proper sequence.

**NOTE**

**Assume that a BR7 and BR6 device are both requesting the bus.**

( ) The BR6 device issues SACK and waits for the bus.

( ) The BR7 device drops SACK and asserts BBSY.

( ) The PA logic issues a BG7.

( ) The PA honors the BR6 request.

( ) The BR7 device issues SACK and waits for the bus.

( ) Both the BR6 and BR7 requests enter the PA logic.

notes

notes