FIELD MAINTENANCE PRINT SET

TABLE OF CONTENTS

UNIT VARIATIONS COVERED BY THIS PRINT SET
KDF11-BA
KDF11-BB
KDF11-BC
KDF11-BD

KDF11-B

Field Maintenance Print Set

Digital Equipment Corporation

Print Set Part Number MP- Ø1236

REVISION HISTORY		
REV.	ECO NUMBER	DATE
A	INITALIZE	6/17/81
B	KDF11-B-ML0001	12-APR-82

DRN. P. BROSNIHAN	DATE 4/4/81	TITLE digital
CHK'D. G. MARINI	DATE 4/4/81	FIELD MAINTENANCE PRINT SET KDF11-B
DES. ENG. Jay Nichols	DATE 22-JUN-81	
RESP. ENG. C. D. Valentine	DATE 22-JUN-81	
FIELD SERVICE G. Marden	DATE 23-JUN-81	
NEXT HIGHER DOC. 11/23-B		

DOCUMENT NUMBER

SIZE	CODE	NUMBER	REV
B	TC	KDF11-B-1	B

SHEET 1 OF 1

SIZE	CODE	NUMBER	REV
B	TC	KDF11-B-1	A

DRB 124A

ML 3

TABLE 1. BOOT/DIAG. SELECTION GUIDE FOR SWITCH PACK E1Ø2

SWITCH	ON	OFF
S1	EXECUTE CPU TEST	SKIP CPU TEST
S2	EXECUTE MEMORY TEST	SKIP MEMORY TEST
S3	EXECUTE DECNET BOOT PROGRAM SELECTED BY S4-S7 PER TABLE 2.	EXECUTE STANDARD BOOT PROGRAM PER SWITCH S4
S4	EXECUTE DIALOGUE BOOT PROGRAM. OPERATOR RESPONDS WITH MNEMONIC PER TABLE 3.	EXECUTE AUTOMATIC (TURNKEY) BOOT PROGRAM SELECTED BY S5-S8 PER TABLE 3.

TABLE 2 DECNET BOOT DEVICE SELECTION (S3 ON)

S4	S5	S6	S7	DEVICE
ON	X	X	X	DUV11
OFF	ON	X	OFF	DLV11-E
OFF	ON	X	ON	DLV11-F

NOTE: X = DON'T CARE

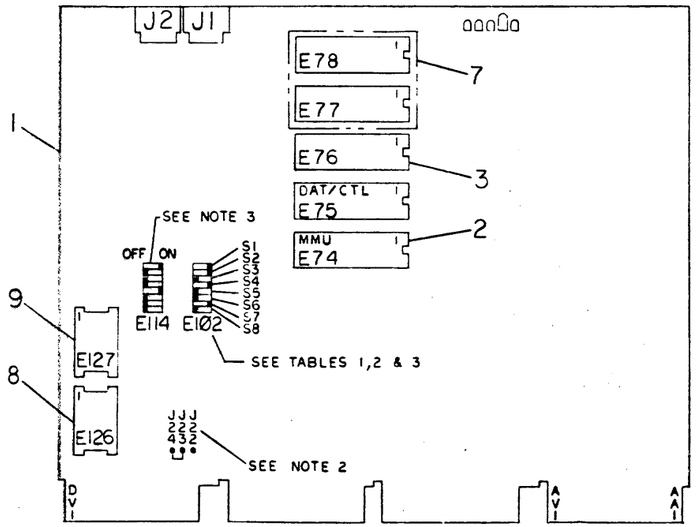
TABLE 3 STANDARD BOOT DEVICE SELECTION (S3 OFF)

MNEMONIC	S5	S6	S7	S8	DEVICE
DKn; n<8	OFF	OFF	OFF	ON	RK05
DLn; n<4	OFF	OFF	ON	OFF	RL01/RL02
DDn; n<2	OFF	OFF	ON	ON	TU58
DXn; n<2	OFF	ON	OFF	OFF	RX01
DYn; n<2	OFF	ON	ON	OFF	RX02

LEGEND	
NUMBER	DESCRIPTION
KDF11-BA	M8189-ØØ PLUS KTF11-AA & BOOT/DIAG. ROMS
KDF11-BB	M8189-ØØ PLUS KTF11-AA, KEF11-AA & BOOT/DIAG. ROMS
KDF11-BC	M8189-ØØ PLUS BOOT/DIAG. ROMS
KDF11-BD	M8189-ØØ PLUS KTF11-AA, KEF11-BB & BOOT/DIAG. ROMS

NOTES:

1. WHEN INSTALLING ITEMS 2,3,8&9 MAKE SURE THAT PIN 1 IS LOCATED AS SHOWN.
2. WHEN ITEMS 8 & 9 ARE MASKED ROMS CONNECT J23 TO J24 WITH J22 NOT CONNECTED. WHEN ITEMS 8 & 9 ARE EPROMS CONNECT J22 TO J23 WITH J24 NOT CONNECTED.
3. BAUD RATE SELECTION. SEE D-CS-M8189-Ø-K11. SETTINGS SHOWN PRODUCE 9600 BAUD EACH LINE.
4. KEF11-BB=CIS MICROCODE HYBRID. CONTAINS CIS MICROCODE TO IMPLEMENT THE COMMERCIAL INSTRUCTION SET.



CAUTION: OFF SHEET PARTS LIST EXISTS, SEE
K-PL-KDF11-B-DBP

REVISIONS		
CHK	CHANGE NO.	REV.
	INITIAL	A
	KDF11-B-ML001	B

A. Valentine 12-APR-82
C. VALENTINE

QUANTITY & VARIATION	DESCRIPTION	DWG PART NO	ITEM NO.
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		

ANGLES ±0° 30'	CLASS OF ACCURACY (CHECK ONE)	NOMINAL DIMENSION RANGE-INCHES					
		OVER 0 TO 0.7	OVER 0.7 TO 1.7	OVER 1.2 TO 4.0	OVER 4.0 TO 12.0	OVER 12.0 TO 40.0	OVER 40.0 TO 80.0
SURFACE QUALITY IN MICROINCHES	MEDIUM	±.004	±.008	±.012	±.016	±.024	±.04
	PREFERRED	±.012	±.016	±.025	±.04	±.063	±0.1

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL

FINISH

DRN H. Cullinane
CHK'D
ENG.
PROJ ENG.
PROD.

NEXT HIGHER ASSY. B SD KDF11-B

SCALE NONE

SHEET 1 OF 1

FIRST USED ON 11/23-B

digital

TITLE KDF11-B CPU UNIT ASSEMBLY

SIZE D | CODE UA | NUMBER KDF11-B-X | REV B | DIST.

B | DWG KDF11-B-Ø | REV B | DWG UA KDF11-B-Ø | REV B

AUTOMATED BY FRTLST.3P(44)

P A R T S L I S T

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QUANTITY PER VARIATION BA	BB	BC
1	1		M8189-00	KDF11-B QUAD HT CPU,Q AND Q-22 B	1	1	1
2	2		2115542-01	DC 304 F11 MMU,FLOAT PT REG	1	1	-
3	3		5700001-00	HYBRID ASSY FLOATING POINT	-	1	-
4	4		23244E2-00	E2-04	1	1	1
5	5		23245E2-00	E2-04	1	1	1
6	6		H3270-00	TEST CONNECTOR	1	1	1

7 NOTE: ITEM #6, THE WRAP-AROUND-TEST JUMPER FOR CONNECTOR J2, IS NOT SHOWN ON UA DWG.
8 NOTE: FOR BULK INTERPLANT SHIPMENT OF MODULES REFER TO PACKAGING INSTRUCTION A-SP-3700053-0-0
9 NOTE: FOR SHIPMENT OF INDIVIDUAL MODULES REFER TO PACKAGING INSTRUCTION A-SP-3700069-0-0

REVISION HISTORY			BASIC PART NO: KDF11									
ENG	ECO NUMBER	REV	SECTION A OF A	DRN: P. BROSNIHAN	DATE: 21-JAN-81		D	I	G	I	T	A	L
---	INITIAL	A	SECTION. VARIATION INDEX [A] BA,BB,BC	CHK'D: G. MARINI	DATE: 27-MAY-81	TITLE	PARTS LIST						
			[B]	DES.ENG.: C. VALENTINE	DATE: 21-JAN-81	KDF11-B CPU UNIT ASSEMBLY							
			[C]			DOCUMENT NUMBER							
			[D]	RESP.ENG.: C. VALENTINE	DATE: 21-JAN-81	SIZE	CODE	NUMBER				REV	
			[E]	MFG.ENG.: T. OLMO	DATE: 27-APR-81	K	PL	KDF11-B-DGP				A	
			[F]	ASSEMBLY NUMBER: C-UA-KDF11-B-0	TOP DOCUMENT NUMBER: #B-DD-KDF11-B			FILE NAME: Z2423A.PLS				EDIT # 4	

SIZE	CODE	NUMBER	REV.
B	DD	M8189-Ø	A

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS
		M8189-ØØ	KDF11-B CPU MODULE	
D-UA-M8189-Ø-Ø	2		KDF11-B CPU MODULE	A
K-PL-M8189-Ø-DBP	3		KDF11-B CPU MODULE	A
K-PC-M8189-Ø-DB1			P.C. DESIGN DATA BASE	C
		5Ø14313-ØØ	P.C. BOARD	C
D-MD-5Ø14313-Ø-Ø	6		DRILL & ETCH DRAWING	A
D-EC-5Ø14313-Ø-Ø	2		ETCH CUT DRAWING	A
K-CS-M8189-0-DBS			CIRCUIT DATA BASE	A
D-CS-M8189-Ø-K1	1		TIMING LOGIC & MIB DECODE	A
D-CS-M8189-Ø-K2	1		BUS CONTROL LOGIC	A
D-CS-M8189-Ø-K3	1		SERVICE, RESET & ODT LOGIC	A
D-CS-M8189-Ø-K4	1		F11 CHIPS & FIXED DATA	A
D-CS-M8189-Ø-K5	1		CDAL/BDAL INTERFACE	A
D-CS-M8189-Ø-K6	1		CDAL/IDAL INTERFACE	A
D-CS-M8189-Ø-K7	1		IDAL ADRS DECODE	A
D-CS-M8189-Ø-K8	1		BOOT & CLOCK LOGIC	A
D-CS-M8189-Ø-K9	1		CONSOLE & SECOND SLU	A
D-CS-M8189-Ø-K10	1		BAUD RATE & -12V	A
D-CS-M8189-Ø-K11	1		CONFIGURATION GUIDE	A

NOTES:

REVISIONS	REV.	CHG NO.	DATE

digital

USED ON OPTION/MODEL	
KDF11-B	

DRN.	R. BARILONE	2DEC80
CHK'D	D. DROZD	22JAN81
ENG.	J. NICHOLS	13APR81
PROD.	T. OLMO	13APR81

TITLE: KDF11-B CPU MODULE

SIZE	CODE	NUMBER	REV.
B	DD	M8189-Ø	A

SHEET 1 OF 1

DRB 126

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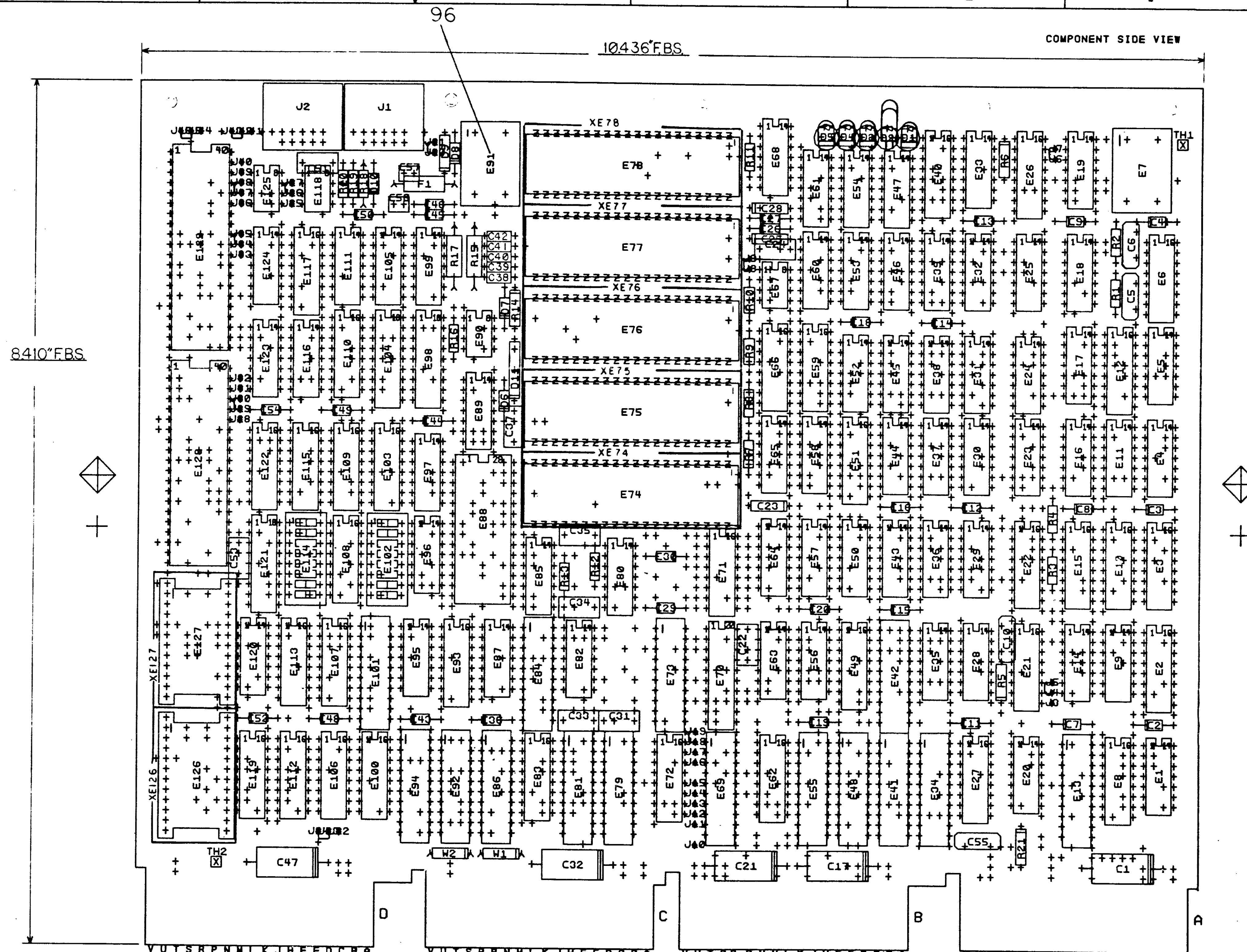


NOTES:

STEP &	↑ Y AXIS ___ STEP ___ TIMES
REPEAT	→ X AXIS ___ STEP ___ TIMES

CHK | CHANGE NO | REV

ETCH REV. C

SIGNATURES	DATE
DRN.	10-15-80
CHK'D.	
MECH. ENG.	4-7-81
PROJ. ENG.	4-13-81
PROD.	4-13-81
SCALE 2-1	
SHT. 1 OF 2	
NEXT HIGHER ASSY. 8-DD-M8189-0	

digital

TITLE KDF11-B CPU MODULE

SIZE	CODE	NUMBER	REV
D	UA	M8189-0-0	A

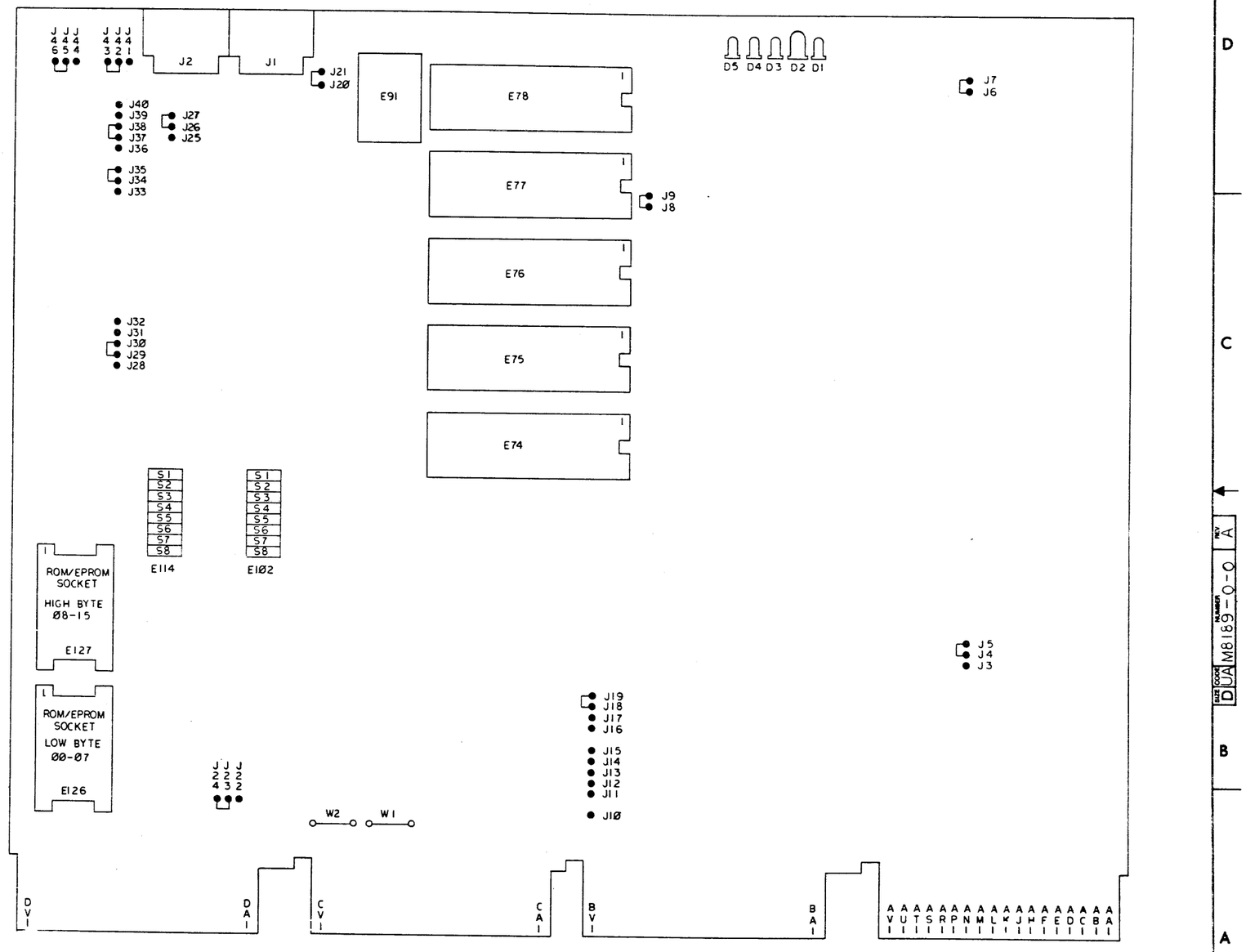
1 WO#275022C

SIZE D CODE DUA NUMBER M8189-0-0 REV A

JUMPER TABLE				
ITEM NO	DESCRIPTION	FROM	TO	
97	MINI JUMPER	J4	J5	SEE NOTE 1
		J6	J7	
		J8	J9	
		J18	J19	
		J20	J21	
		J23	J24	
		J26	J27	
		J29	J30	
		J34	J35	
		J37	J38	
		J42	J43	
		J45	J46	

NOTES: 1. WHEN MASKED ROM'S ARE USED, CONNECT J24 TO J23, J22 IS NOT CONNECTED.

WHEN EPROM'S ARE USED, CONNECT J22 TO J23, J24 IS NOT CONNECTED.



REVISION HISTORY		
DATE	ECO NUMBER	REV.

DRD 138A

TITLE: KDF11-B CPU MODULE

DOCUMENT NUMBER			
SIZE	CODE	NUMBER	REV.
D	DUA	M8189-0-0	A
SCALE		SHEET 2 OF 2	

AUTOMATED BY PRTLST.3P(44)

P A R T S L I S T

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	REFERENCE DESIGNATOR
1	1	D-MD-5014313-0-0	5014313-00	DRILL AND ETCH BD.	1	
2	2		1000022-00	270.0 MMF 100V 5%200PPM MICA	1	C10
3	3		1000024-00	470.0 MMF 100V 5%200PPM MICA	3	C5,C6,C55
4	4		1001610-00	.01 MFD 50V +80-20% 25U CER	3	C26,C27,C30
5	5		1012784-00	.047 MFD 50V +80-20% CER	29	C2-C4,C7-C9,C11-C18,C18-C20,C23,
						CONT C25,C28,C29,C36,C43-C46,C48-C50,
						CONT C52,C54
6	6		1016681-00	.47 MFD 50V +80-20% CER	14	C22,C24,C31,C33-C35,C37-C42,C51,
						CONT C53
7	7		1017472-00	10 MFD 35V +50-10% AL EL	5	C1,C17,C21,C32,C47
8	8		1011740-02	1800.0 MMF 50V 10% CER	2	C56,C57
9	9		1109977-00	1N 749A VZ= 4.3 5%	1	D9
10	10		1112689-00	LED .8MCD@16MA VF=5V	4	D1,D3-D5
11	11		1114384-00	LED 105MW 35MA GREEN	1	D2
12	12		1100114-00	D 664 GS\75PCB PIV= 25V SP	3	D6-D8
13	13		1110967-00	1N 4005 PIV=600 I= 1A D041 SI	1	D10
14	14		1105508-00	1N 823 VZ= 6.2 5% .40W Y	1	D11
15	15		1213506-04	HEADER 10POS RT ANGLE W/3 SI	2	J1,J2
16	16		1215006-06	SOCKET 24PIN IC LOW PROFILE	2	XE126,XE127
17	17		1216116-00	SOCKET 40PIN	5	XE74-XE78
18	18		1210929-02	FUSE, SUB-MINI 1.000A, 125V, A	1	F1
19	19		1211164-04	SW,DIP 1P 1A 8POS	2	E102,E114
20	20		1213113-01	HANDLE,MODULE,	1	
21	21		1300229-00	100.0 .25 W 5.0 % CC	1	R7
22	22		1300316-00	470.0 .25 W 5.0 % CC	3	R6,R12,R16
23	23		1300365-00	1.0 K .25 W 5.0 % CC	4	R3,R4,R8,R11
24	24		1300488-00	12.0 K .25 W 5.0 % CC	2	R19,R20
25	25		1301322-00	180.0 .25 W 5.0 % CC	1	R13
26	26		1301808-00	22.0 K .25 W 5.0 % CC	1	R18
27	27		1302177-00	47.0 K .25 W 5.0 % CC	2	R1,R2

REVISION HISTORY			BASIC PART NO: M8189											
ENG	ECO NUMBER	REV	SECTION A OF A	DRN: R. BUREAU	DATE: 11-JUL-80		D	I	G	I	T	A	L
	INITIAL	A	SECTION.VARIATION INDEX	CHK'D: BOB BARILONE	DATE: 11-JUL-80	TITLE	PARTS LIST						
			[A] 00			KDF11-B CPU MODULE							
			[B]										
			[C]	DES.ENG: C.A. VALENTINE	DATE: 14-APR-81								
			[D]										
			[E]			DOCUMENT NUMBER							
			[F]	RESP.ENG.: JAY NICHOLS	DATE: 14-APR-81								
			[H]			SIZE	CODE	NUMBER				REV	
			[J]										
			[K]	MFG.ENG.: TOMAS OLMO	DATE: 14-APR-81	K	PL	M8189-0-DBP				A	
			[L]										
			[M]	ASSEMBLY NUMBER:	TOP DOCUMENT NUMBER:	FILE NAME:						EDIT #	
			[N]	D-UA-M8189-0-0	B-DD-M8189-0-0	Z1037A.PLS						17	

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	REFERENCE DESIGNATOR
28	28		1302602-00	56.0 .25 W 5.0 % CC	1	R5
29	29		1309422-00	5.10 .25 W 5.0 % CC	2	R9,R10
30	30		1311003-01	R NETWORK 14-180 14-390 16PIN	3	E8,E27,E62
31	31		1301320-00	1.20 K .25 W 5.0 % CC	1	R21
32	32		1300005-03	R NETWORK 13-10K 5.0 % 14PIN	1	E123
33	33		1300005-07	R NETWORK 15-4.7K 5.0 % 16PIN	3	E72,E108,E122
34	34		1300228-00	100.0 .50 W 5.0 % CC	2	R15,R17
35	35		1303178-00	620.0 .25 W 5.0 % CC	1	R14
36	36		1811660-02	OSCILLATOR, XTAL 5.0688 MHZ	1	E91
37	37		1811660-20	OSCILLATOR, XTAL 26.666 MHZ	1	E7
38	38		1910544-00	74S74 FF-D DUAL,EDGE TRIGG	8	E17,E19,E29,E30,E36,E38,E43,E50
39	39		1910548-00	74S157 MUX 1 OF 2 (QUAD)	1	E15
40	40		1910550-00	74S174 FF-D HEX	5	E3,E10,E21,E26,E51
41	41		1910957-00	74S175 FF-D QUAD COMMON CLO	4	E12,E22,E40,E59
42	42		1911117-00	DEC 8838 TRANSCEIVER,BUS,QUA	1	E2
43	43		1911469-00	DEC 8640 RECEIVER,BUS,QUAD,U	3	E1,E20,E63
44	44		1909705-00	DEC 8881 NAND GATE-QUAD 2IN O	1	E9
45	45		1911675-00	74S138 DECODER/DEMUX 3-8 LIN	1	E66
46	46		1911712-00	74S51 AND-OR GATE-INVERT D	1	E45
47	47		1912098-00	0026 DRIVER,MOS CLOCK,2	1	E90
48	48		1912388-00	74S02 NOR GATE-QUAD 2IN,PO	3	E37,E52,E56
49	49		1912389-00	74S08 AND GATE-QUAD 2IN,PO	4	E11,E28,E39,E96
50	50		1912647-00	LS257 MUX 1 OF 2 (QUAD)	6	E83,E100,E106,E110,E113,E119
51	51		1912649-00	LS75 LATCH 4BIT,BISTABLE	1	E49
52	52		1912697-00	LS174 FF-D HEX W/CLEAR	3	E93,E107,E112
53	53		1912730-00	DC 003 INTERRUPT,2 CIRCUIT	2	E98,E104
54	54		1912746-00	DEC 74S37 NAND GATE-QUAD 2IN	1	E61
55	55		1912801-00	LS02 NOR-GATE-QUAD 2IN	1	E85
56	56		1912803-00	74LS04 INVERTER GATE,HEX	1	E89
57	57		1912804-00	LS05 INVERTER GATE-HEX 1I	2	E82,E87
58	58		1912805-00	LS08 AND GATE-QUAD 2IN,PO	1	E65
59	59		1912807-00	LS10 NAND GATE-TRIPLE 3IN	2	E25,E95
60	60		1912808-00	LS11 AND GATE-TRIPLE 3IN	1	E14
61	61		1912810-00	LS20 NAND GATE-DUAL 4IN	2	E53,E60
62	62		1912816-00	LS32 OR GATE-QUAD 2IN,POS	2	E120,E124
63	63		1912824-00	LS74 FF-D DUAL,EDGE TRIGG	4	E5,E80,E111,E64
64	64		1912846-00	LS155 DECODER,2 OF 4(DUAL)	3	E103,E109,E115
65	65		1912853-00	LS175 FF-D QUAD	1	E117
66	66		1912857-00	LS197 COUNTER,BINARY,PRESET	1	E105
67	67		1912858-00	LS221 ONE SHOT-DUAL,SCHMIT	1	E6
68	68		1912863-00	LS273 FF-D OCTAL W/CLEAR	1	E86
69	69		1912868-00	LS299 SHIFT REG. 8-BIT UNI	2	E92,E101
70	70		1913340-00	74S32 OR GATE-QUAD 2IN	4	E4,E44,E97,E116
71	71		1913462-00	74S240 OCTAL BUFFER,INVERTI	3	E42,E73,E79
72	72		1913671-00	74S374 FF-D OCTAL TRISTATE	1	E70
73	73		1913777-00	LS240 DRIVER,LINE,OCTAL,T	1	E94
74	74		1914085-00	74S260 NOR GATE-DUAL,POS	1	E23
75	75		1915218-00	LS245 TRANSCEIVER,BUS,OCT	2	E81,E84

D	I	G	I	T	A	L	TITLE	SECTION A OF A
							KDF11-B CPU MODULE	

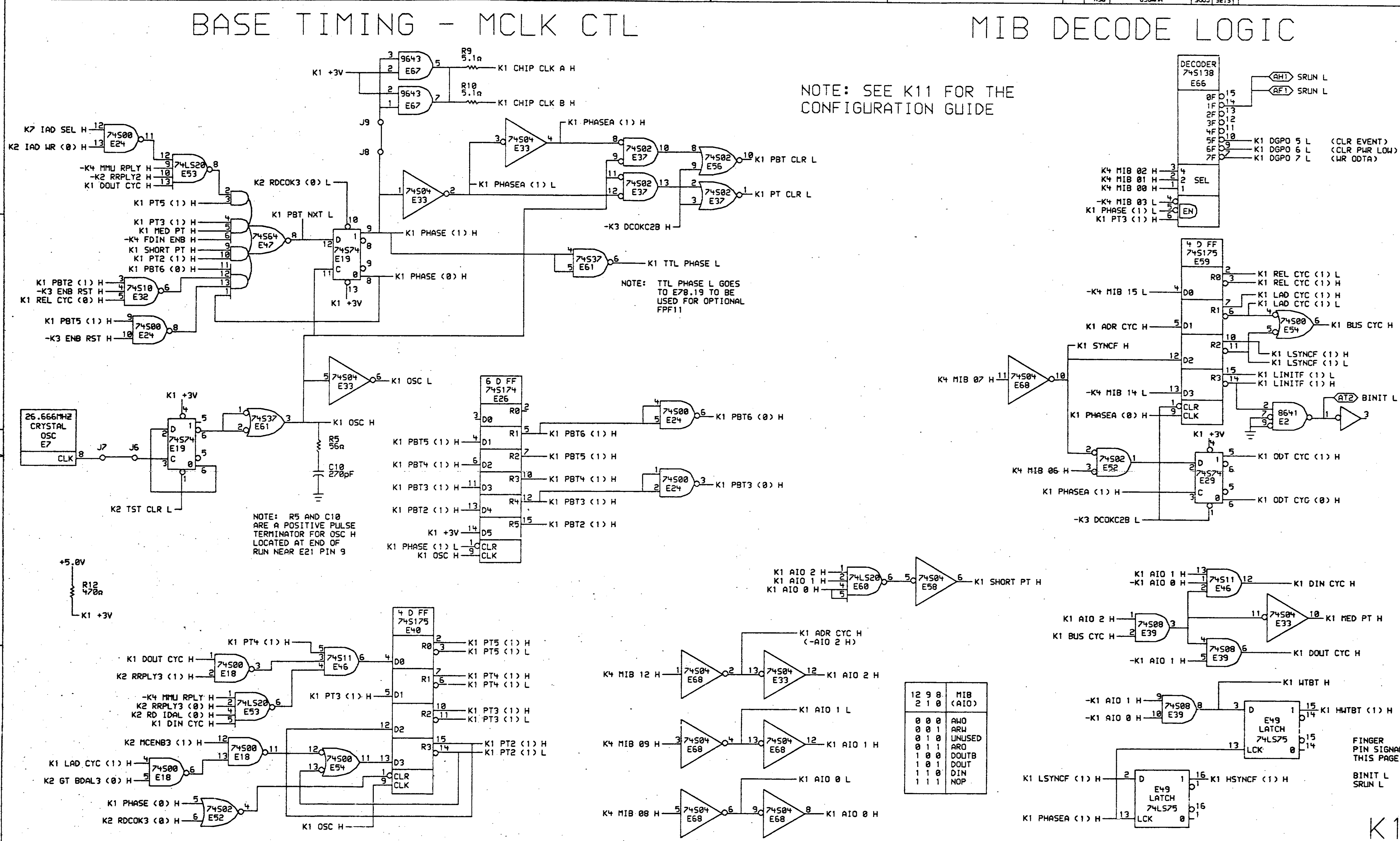
SIZE	CODE	DOCUMENT NUMBER	REV
K	PL	M8189-0-DBP	A

AUTOMATED BY PRTLST.3P(44)

P A R T S L I S T

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	REFERENCE DESIGNATOR
76	76		1915305-00	AM 2908 TRANSCEIVER,BUS,LATCH	6	E13,E34,E41,E48,E55,E69
77	77		1915415-00	9636 DRIVER,DUAL,EIA RS-	1	E118
78	78		1915416-00	9637 RECEIVER,DUAL,RS-42	1	E125
79	79		1916028-01	9643 DRIVER,TTL TO MOS,D	1	E67
80	80		1910532-00	74S00 NAND GATE-QUAD 2IN	6	E16,E18,E24,E31,E35,E54
81	81		1910534-00	74S04 INVERTER GATE-HEX 1I	4	E33,E58,E68,E99
82	82		1910535-00	74S05 INVERTER GATE-HEX 1	1	E57
83	83		1910536-00	74S10 NAND GATE-TRIPLE 3IN	1	E32
84	84		1910537-00	74S11 AND GATE-TRIPLE 3INP	1	E46
85	85		1910542-00	74S64 A-O-I GATE 4-2-3-2	1	E47
86	87		2112623-00	DUAL BAUD RATE GEN/PROG DIVIDER,	1	E121
87	88		2113937-01	6402-1 UART,UNIV.,ASYNCHRO	2	E128,E129
88	91		23061C6-00	C6-01	1	E88
89	92		5700000-01	DAT/CTL HYBRID ASSY W/FP,DCF11-A	1	E75
90	93		9009149-00	PIN, STAKING, P.C. BOARD, .025 X	44	J3-J46
91	94		9009185-00	JUMPER, WIRE, INSULATED, BLACK B	2	W1,W2
92	95		9000024-01	EYELET,ROLL FLANGE .1210DX .192	6	
93	96		9010213-01	SPACER,14 PIN BLK/NYL .060THK.	1	
94	97		1218783-00	CONN .100 2POS JUMPER	12	

D	I	G	I	T	A	L	TITLE	SECTION A OF A	SIZE	CODE	DOCUMENT NUMBER	REV
							KDF11-B CPU MODULE		K	PL	M8189-0-DBP	A



DRAWING 1 OF 11

REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. DATE 05-MAR-81
CHK. DATE 4-13-81

4-13-81

BOARD LOCATION:
SHEET 1 OF 1

[365,3132]M81891.DRW |04-MAR-81 16:55| NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: KDF11-B | B-DD-M8189-0

TITLE: TIMING LOGIC & MIB DECODE

SIZE	CODE	NUMBER	REV.
D	CS	M8189-0-K1	A

BUS CONTROL LOGIC

QBUS SYNCHRONIZER

[NO SACK DELAY]

BSACK L (BN1) → 8640 E63 → K2 RSACK H

+5.0V — R2 4.7KΩ — C6 470pF — 10µS OS → 74LS221 E6

K2 ENB DMR (1) L → 74LS74 E5 → K1 +3V

K2 DMG (1) H, -K2 RRPLY L, -K2 RSACK L → 74S08 E11, 8640 E63

K2 RDMR H, BDMR L (AN1) → 8640 E1

K2 RDCOK1 (0) H, K2 RDCOK L, BDCOK H (BA1) → 8640 E20

K1 +3V → CLR

6 D FF 74S174 E3

K2 RRPLY H	D0	R0 → K2 RRPLYB (1) H
K2 RSYNC H	D1	R1 → K2 RSYNCB (1) H
K2 RSACK H	D2	R2 → K2 RSACKB (1) H
K2 RDMR H	D3	R3 → K2 RDMRB (1) H
K2 RDCOK1 (0) H	D4	R4 → K2 RDCOK3 (0) H
K2 RDCOK L	D5	R5 → K2 RDCOK1 (0) H
K1 +3V	CLR	
	CLK	

K2 RDCOK3 (0) H → 74S00 E54 → K2 RDCOK3 (1) H

4X2 MUX 74S157 E15

K2 RRPLYB (1) H	0-DA	YA → K2 RRPLY2 H
K2 RSYNCB (1) H	1-DA	
K2 RSACKB (1) H	0-DB	YB → K2 RSYNC2 H
K2 RDMRB (1) H	1-DB	
K2 SELA (1) H	0-DC	YC → K2 RSACK2 H
K3 DCOKC3 (1) L	1-DC	
	0-DD	YD → K2 RDMR2 H
	1-DD	
	1 SEL	
	EN	

K2 RRPLY2 H → 74S04 E33 → K2 RRPLY2 L

6 D FF 74S174 E10

K2 RRPLY H	D0	R0 → K2 RRPLYA (1) H
K2 RSYNC H	D1	R1 → K2 RSYNCA (1) H
K2 RSACK H	D2	R2 → K2 RSACKA (1) H
K2 RDMR H	D3	R3 → K2 RDMRA (1) H
K2 MCENB1 (1) H	D4	R4 → K2 MCENB3 (1) H
K2 MCENB H (AM2)	D5	R5 → K2 MCENB1 (1) H
K2 RDCOK3 (0) L	CLR	
	CLK	

BRPLY L (AF2) → 8641 E2 → K2 RRPLY H

K3 TIMEOUT (1) H

BSYNC L (AJ2) → 8641 E2 → K2 RSYNC H

K2 TSYNC (1) H

+5.0V — R3 1KΩ

K1 +3V → K2 SELA (1) H

K1 OSC H → 74S74 E29 → K2 SELA (0) H

R4 1KΩ — +5.0V — K2 TST CLR L

-K3 IRQ 5 L, -K3 IRQ 6 L → 74S32 E4, 74S32 E44

K9 DL IRQ L

K1 +3V → K2 EN DLIAK (1) H

K1 PHASEA (1) H, -K3 DCOKC2B L → 74S74 E30

K2 EN DLIAK (0) H

K4 MIB 13 H (IAK), K1 DIN CYC H, K7 IAD SEL H → 74S51 E45

K1 PT4 (1) L → 74S32 E44

K1 +3V → K2 RD IDAL (1) H, K2 RD IDAL (1) L

K1 OSC H, -K3 DCOKC2B L → 74S74 E50

K1 +3V → K2 TSYNC (1) H

K3 DCOKC2 (1) H, K2 GT BDAL3 (1) L, K1 PHASEA (1) L, K1 LSYNCF (1) H → 74S02 E52, 74S51 E45, 74S08 E28

-K1 OSC H → 74S74 E17 → K2 TSYNC (0) H

K3 RESET (1) H, K1 PHASEA (0) H → 8640 E20, 74S02 E56

K2 LCHIP RST (1) L

-K2 RRPLY L, K2 HLD BUS (0) L → 74S32 E4

K1 +3V → K2 DIN (1) H

K2 DIN ENB H, -K1 OSC H → 74S74 E17

-K3 DCOKC2B L → 8881 E9 → BDIN L (AH2)

4 D FF 74S175 E22

K1 PBT3 (1) H, K1 PT3 (1) H	D0	R0 → K2 LD BBS7 (1) H
K1 PT2 (1) H, K1 PT5 (0) H, K1 DOUT CYC H	D1	R1 → K2 IAD WR (1) L
K2 RSACK2 H	D2	R2 → K2 RSACK3 (1) L
K3 LPOK1 (1) H, -K3 DCOKC2B L, K1 OSC H	D3	R3 → K2 LPOK2 (1) H, K2 LPOK2 (1) L
	CLR	
	CLK	

K1 PT4 (1) H, K1 DIN CYC H, -K4 MMU RPLY H → 74LS20 E60

K1 +3V → K2 RD BDAL (1) H, K2 RD BDAL (1) L

K1 OSC H → 74S74 E50

K1 PBT CLR L

K1 +3V → K2 HLD BUS (1) H

-K1 BUS CYC L → 74S00 E16 → K2 HLD BUS (0) H

K1 PT5 (1) H, K1 DOUT CYC H → 74S08 E39 → K2 DOUT1 (1) H

6 D FF 74S174 E21

K2 DOUT1 (1) H	D0	R0 → K2 DOUT2 (1) H
K1 PBT3 (1) H, K1 LAD CYC (1) H, K1 ODT CYC (0) H	D1	R1 → K2 DOUT1 (1) H
K1 PBT4 (1) H, K1 LAD CYC (1) H, K1 ODT CYC (0) H	D2	R2 → K2 LD BDAL (1) H
K1 ADR CYC H, K1 PT3 (1) H	D3	R3 → K2 LD IADR (1) H
K2 RDMR2 H, K2 GT BDAL1 (0) H, K2 HLD BUS (0) H	D4	R4 → K2 RSACK3 (0) H
K2 GT BDAL3 (0) H, K2 EN DLIAK (0) H, K4 MIB 13 H (IAK)	D5	R5 → K2 TIAK (1) H
-K3 DCOKC2B L, K1 OSC H	CLR	
	CLK	

K1 PT3 (1) L → 74S00 E18

K1 PBT3 (1) H, K1 LAD CYC (1) H, K1 ODT CYC (0) H → 74LS10 E25

K1 PBT4 (1) H, K1 LAD CYC (1) H, K1 ODT CYC (0) H → 74LS10 E25

K2 GAD CYC L → 74S00 E31

K1 ADR CYC H, K1 PT3 (1) H → 74S00 E31

K2 DMG ENB H → 74LS11 E14

K2 GT BDAL3 (0) H, K2 EN DLIAK (0) H, K4 MIB 13 H (IAK) → 74LS11 E14

K2 TSYNC (1) H → 8881 E9 → BDOUT L (AE2)

K2 DOUT1 (1) H

K2 DMG (1) H → 8881 E9 → BDMGO L (AS2)

K2 TIAK (1) H → 8881 E9 → BIAKO L (AN2)

K2 DIN (1) H

K2 TSYNC (0) H, K2 RSYNC2 H → 74S00 E16

K2 DIN ENB H

K1 PT3 (1) H, K1 DIN CYC H, K1 PHASE (1) H → 74S11 E46

K2 RRPLY2 H, K2 GT BDAL2 (0) H → 74S08 E11

K2 RSACK2 H, K2 DMG (1) H, K2 DMG ENB H → 74S260 E23

K2 GAD CYC L → 74S00 E16

K1 BUS CYC H, K2 DOUT2 (1) H → 74S02 E37

K2 RRPLY2 H → 74S08 E11

K2 GT BDAL1 (1) H

K2 GT BDAL2 (1) H → 74S08 E11

K2 INH GT BDAL L → 74S08 E11

-K3 DCOKC2B L, K1 OSC H

4 D FF 74S175 E12

K2 RRPLY2 H	D0	R0 → K2 RRPLY3 (1) H, K2 RRPLY3 (1) L
K2 GT BDAL2 (1) H	D1	R1 → K2 GT BDAL3 (1) L
K2 GT BDAL1 (1) H	D2	R2 → K2 GT BDAL2 (1) H, K2 GT BDAL2 (1) L
	D3	R3 → K2 GT BDAL1 (1) H, K2 GT BDAL1 (1) L
	CLR	
	CLK	

BDMR L
BDCOK H
BSACK L
BRPLY L
BSYNC L
MCENB H
BDOUT L
BDMGO L
BIAKO L
BDIN L

K2

DRAWING 2 OF 11

REVISIONS		
CHK	CHANGE NO.	REV

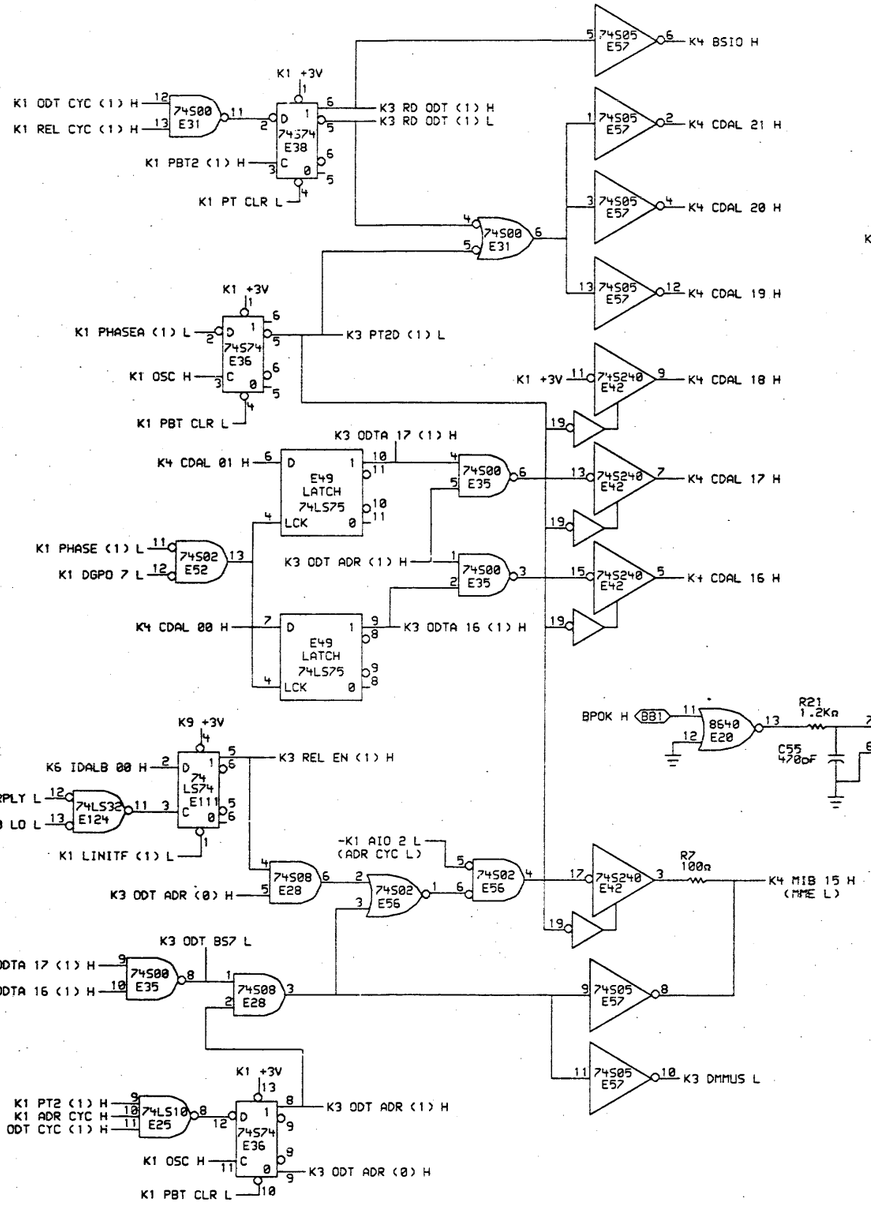
digital

DRN H Cullom	DATE 05-MAR-81	ENG	DATE
CHK D Hallam	DATE 4-13-81	BOARD LOCATION:	
[365,3132]M81892.DRW 04-MAR-81 17:09		SHEET 1 OF 1	NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: KDF11-B		B-DD-M8189-0	

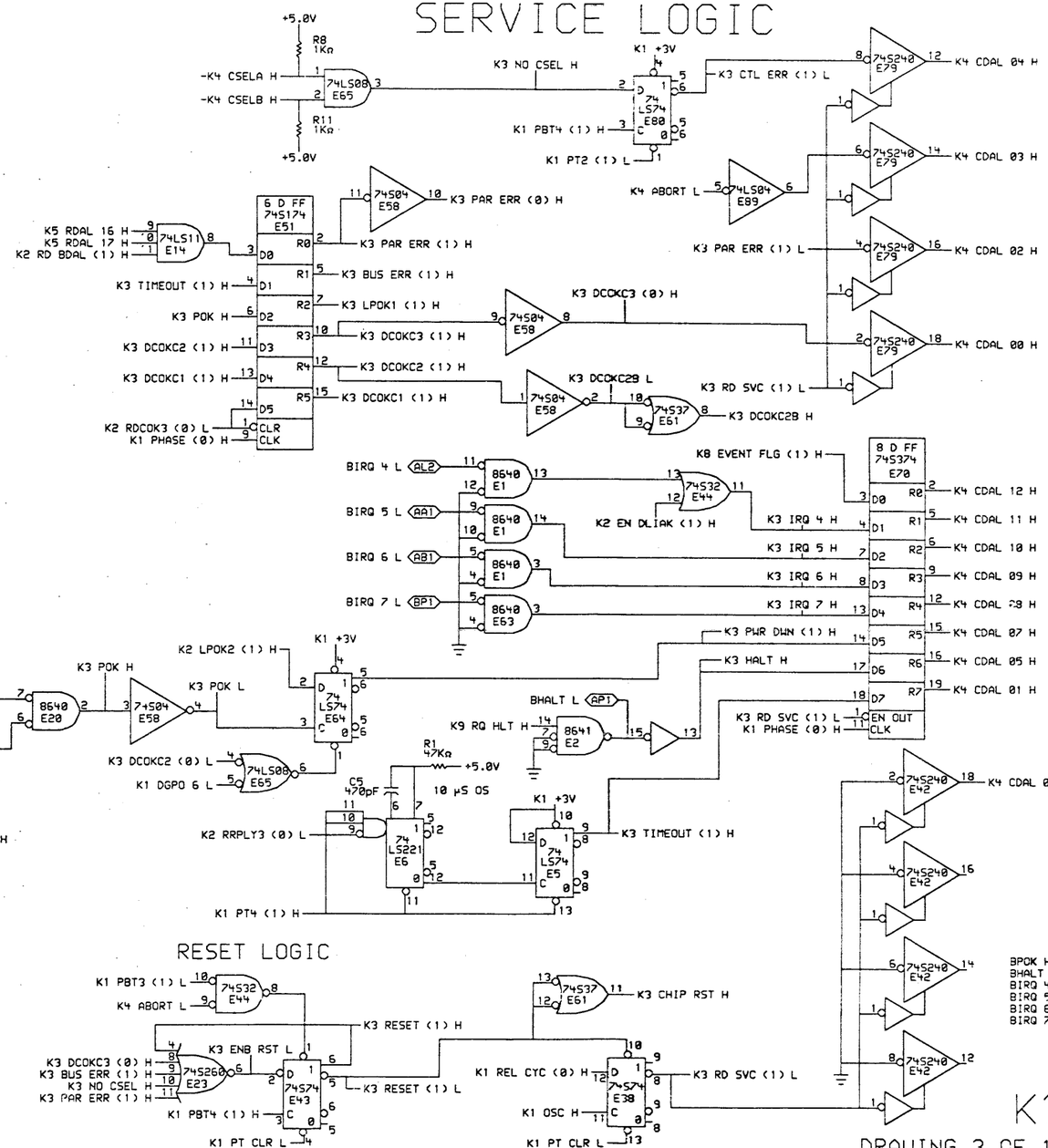
TITLE: BUS CONTROL LOGIC

SIZE	CODE	NUMBER	REV.
D	CS	M8189-0-K2	A

ODT LOGIC



SERVICE LOGIC



RESET LOGIC

K3

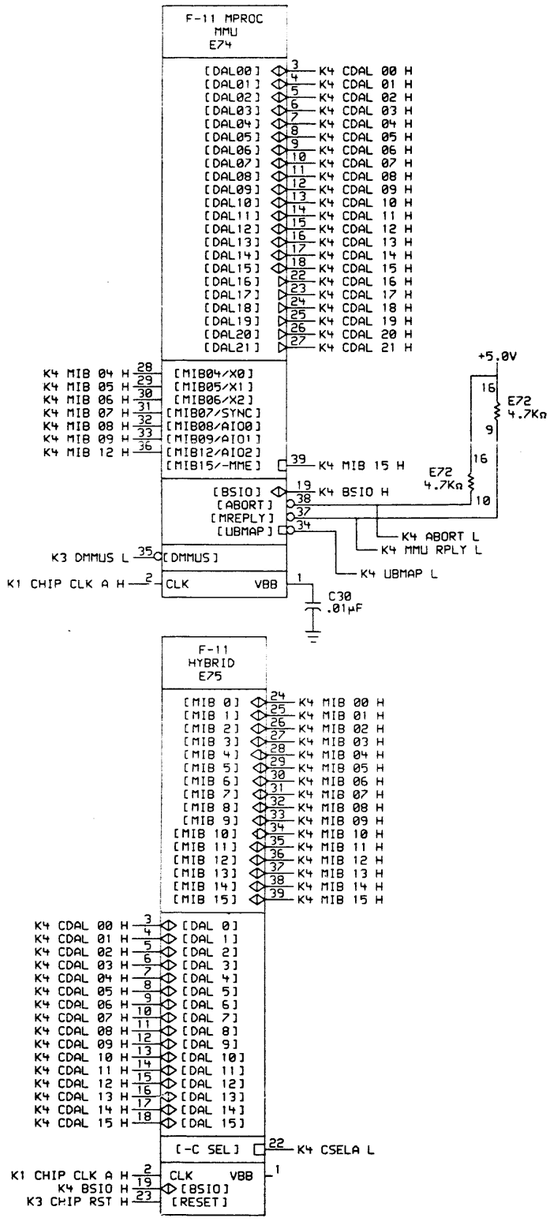
DRAWING 3 OF 11

REVISIONS		
CHK	CHANGE NO.	REV

DRN. HCullum	DATE 03-MAR-81	ENG.	DATE 4-2-81
CHK APCullum	DATE 4-13-81	SCALE LOCATION: SHEET 1 OF 1	
[365,3132]M81893.DRW	04-MAR-81 17:15	NEXT HIGHER ASSEMBLY:	
FIRST USED ON OPTION/MODEL: KDF11-B		8-DD-M8189-0	

TITLE: SERVICE, RESET & ODT LOGIC

SIZE	CODE	NUMBER	REV.
D	CS	M8189-0-K3	A



REVISIONS		
CHK	CHANGE NO.	REV

digital	DRN	05-MAR-81	ENG		
	CHK		DATE	BOARD LOCATION:	
[365,3132]M8189A.DRW	05-MAR-81 08:59	NEXT HIGHER ASSEMBLY:			
FIRST USED ON OPTION/MODEL: KDF11-B		B-DD-M8189-0			

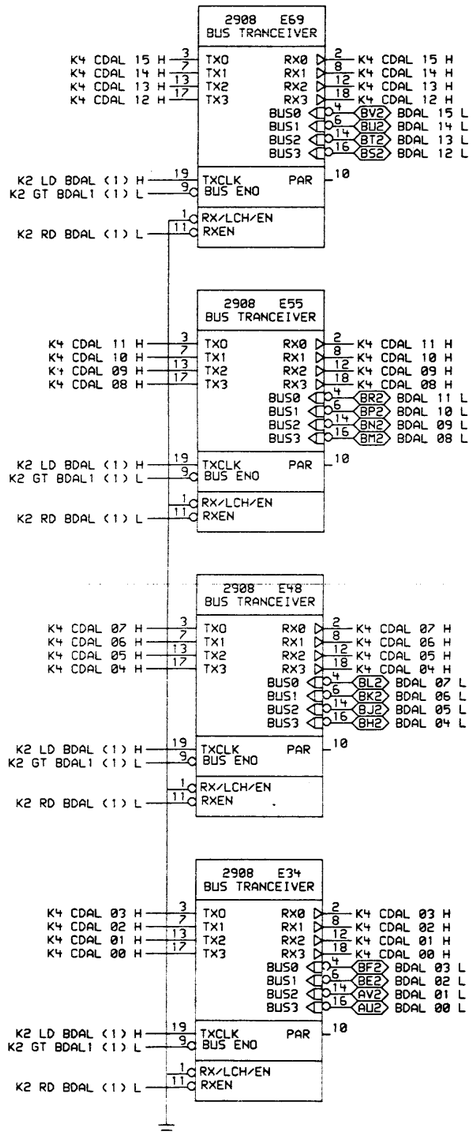
TITLE: F11 CHIPS & FIXED DATA

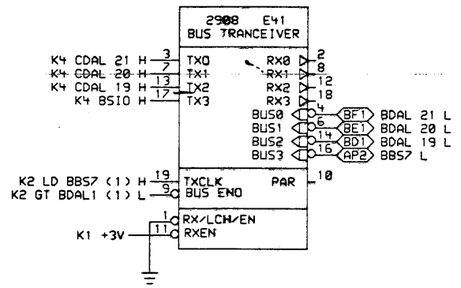
SIZE	CODE	NUMBER	REV.
D	CS	M8189-0-K4	A

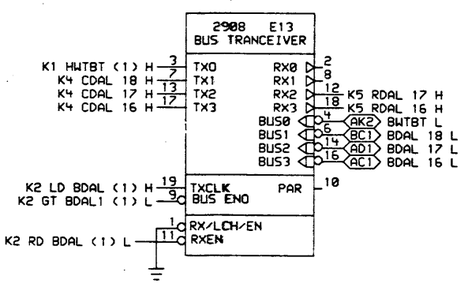
K4

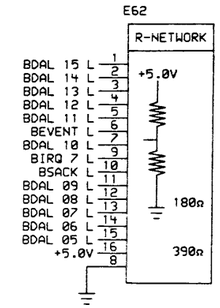
DRAWING 4 OF 11

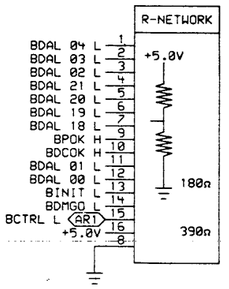
QBUS TERMINATORS

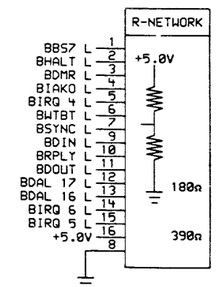












BDAL 00 L
TO
BDAL 21 L
BCTRL L
BBS7 L
BWTBT L

K5

DRAWING 5 OF 11

REVISIONS		
CHK	CHANGE NO.	REV

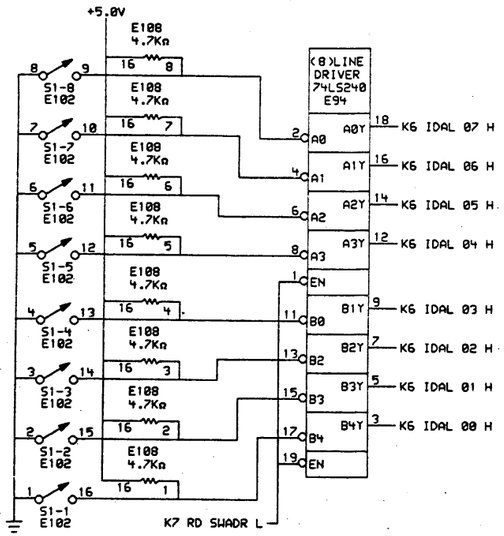
digital

DRN. H. Gillis — DATE 05-MAR-81
CHK'D. H. Gillis — DATE 4-17-81
ENG. Richard Valente — DATE 4-7-81
BOARD LOCATION:
SHEET 1 OF 1
[365,3132]M81895.DRW 05-MAR-81 09:26
FIRST USED ON OPTION/MODEL: KDF11-B
NEXT HIGHER ASSEMBLY: 8-DD-M8189-0

TITLE: CDAL/BDAL INTERFACE

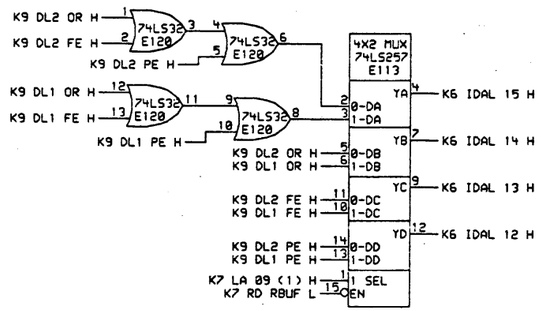
SIZE	CODE	NUMBER	REV.
D	CS	M8189-0-K5	A

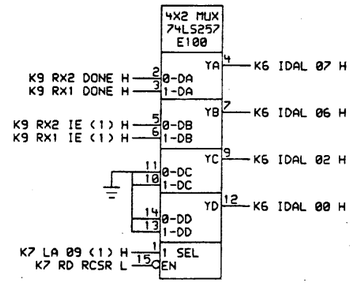
BOOT SWITCHES

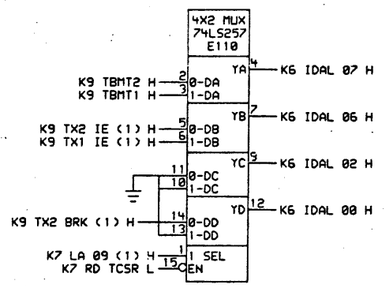


SWITCH PACK 1

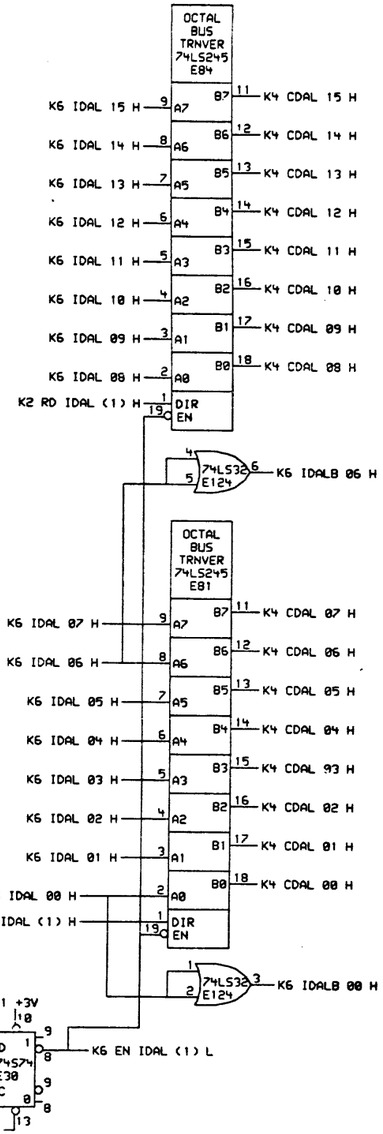
SLU's READ STATUS







CDAL/IDAL TRANSCEIVERS



K6

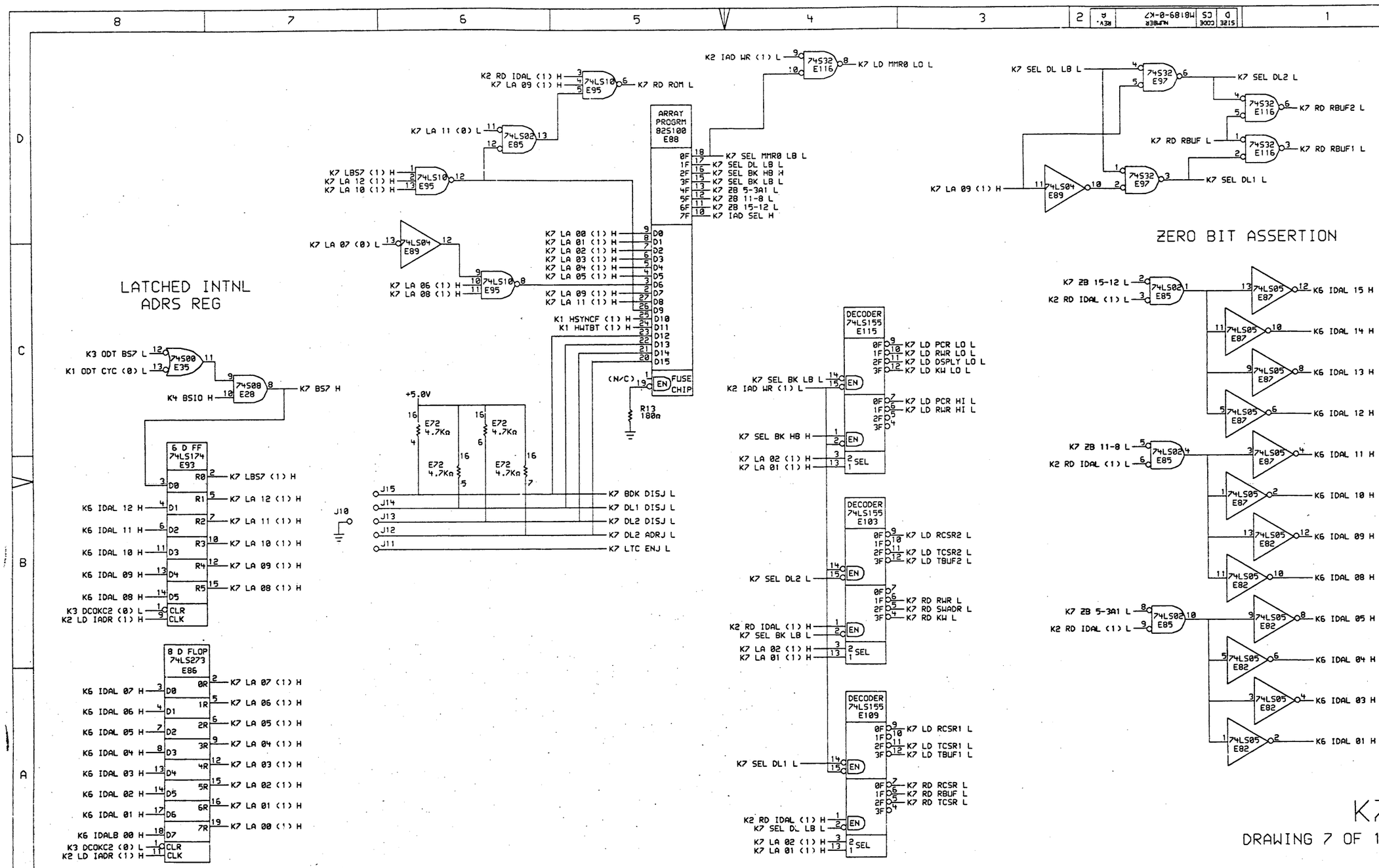
DRAWING 6 OF 11

REVISIONS		
CHK	CHANGE NO.	REV

digital	DRN. HCallain	DATE 05-MAR-81	ENG. Carlo Valenti	DATE 4-7-81
	CHK'D HCallain	DATE 4-13-81	BOARD LOCATION:	SHEET 1 OF 1
[365,3132]M8189G.DRW	05-MAR-81 09:08	NEXT HIGHER ASSEMBLY:		
FIRST USED ON OPTION/MODEL: KDF11-B		B-DD-M8189-0		

TITLE: CDAL/IDAL INTERFACE

SIZE	CODE	NUMBER	REV.
D	CS	M8189-0-K6	A



REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. H Cullivan — DATE 05-MAR-81 — ENG — DATE 4-2-81

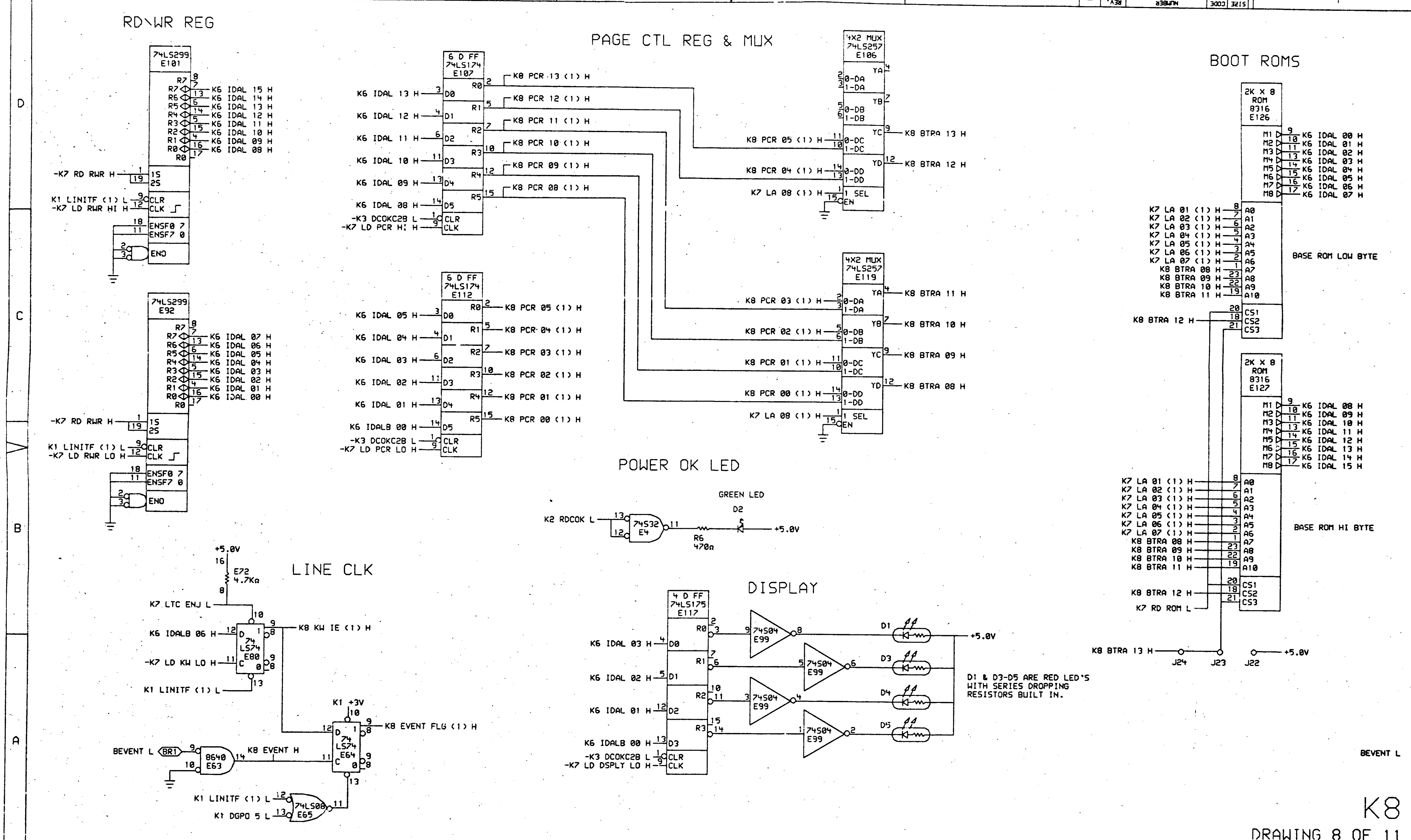
CHK D. Cullivan — DATE 4-13-81 — BOARD LOCATION: — SHEET 1 OF 1

[365,3132]M81897.DRW — 05-MAR-81 09:10 — NEXT HIGHER ASSEMBLY: B-DD-M8189-0

FIRST USED ON OPTION/MODEL: KDF11-B

TITLE: IDAL ADRS DECODE

SIZE	CODE	NUMBER	REV.
D	CS	M8189-0-K7	A



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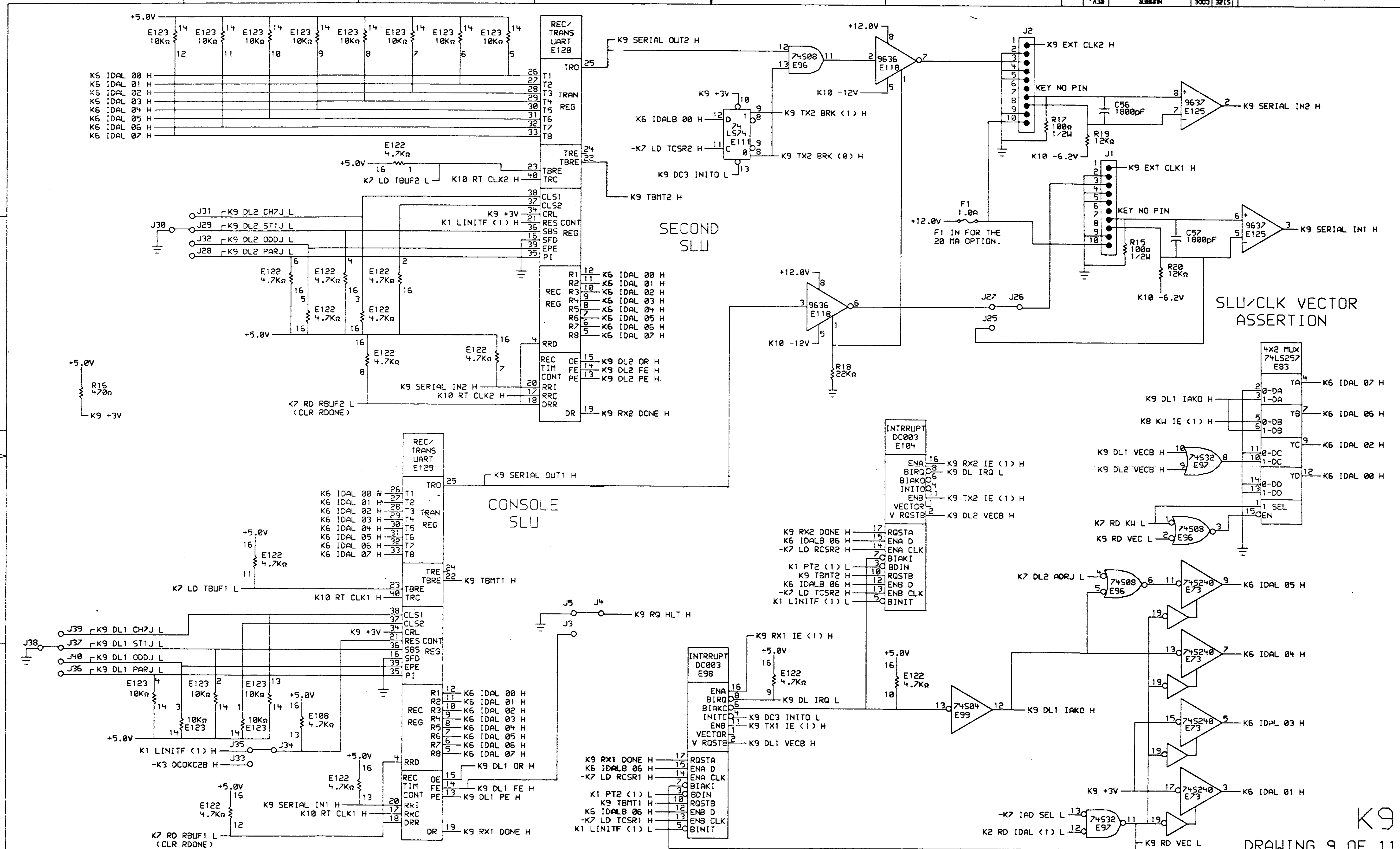
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. H Cullison — DATE 03-APR-81
CHK'D H Cullison — DATE 4-17-81
ENG. — DATE 4-10-81
BOARD LOCATION:
SHEET 1 OF 1
[365,3132]M81898.DRW 02-APR-81 07:52
NEXT HIGHER ASSEMBLY: B-DD-M8189-0
FIRST USED ON OPTION/MODEL: KDF11-B

TITLE: BOOT & CLOCK LOGIC

SIZE	CODE	NUMBER	REV.
D	CS	M8189-0-K8	A



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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. H Cullen — DATE 05-MAR-81 — ENG. Charles Lail — DATE 4-7-81

CHK D. H Cunningham — DATE 4-13-81 — BOARD LOCATION:

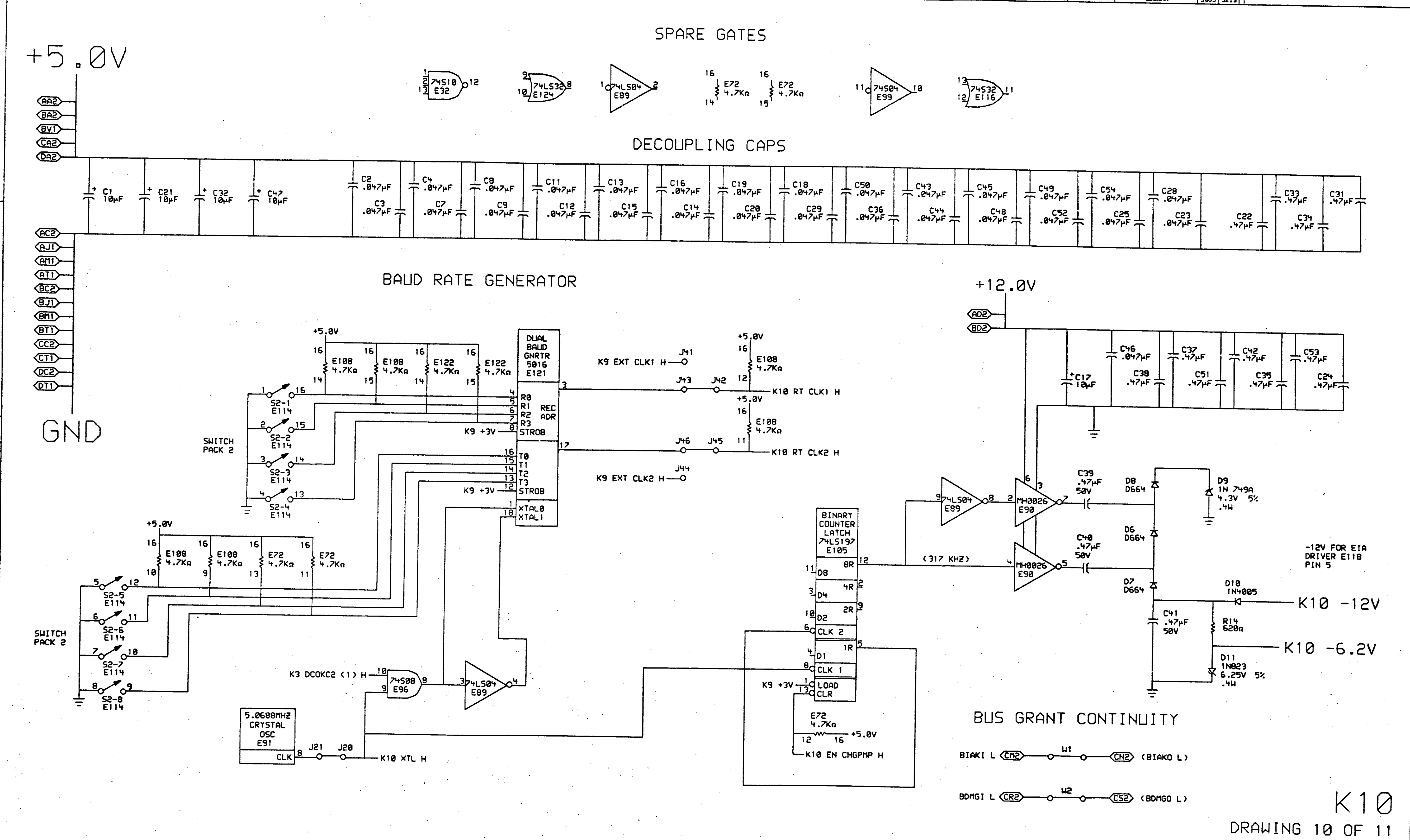
SHEET 1 OF 1

[365,3132]M81899.DRW 05-MAR-81 08:04 — NEXT HIGHER ASSEMBLY: B-DD-M8189-0

FIRST USED ON OPTION/MODEL: KDF11-B

TITLE: CONSOLE & SECOND SLU

SIZE	CODE	NUMBER	REV.
D	CS	M8189-0-K9	A



K10

DRAWING 10 OF 11

REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. H. Calhoun — DATE 05-MAR-81
CHK. H. Calhoun — DATE 4-13-81
ENG. Charlie Valente — DATE 4-7-81
BOARD LOCATION:
SHEET 1 OF 1
[365,3132]M81890.DRW 05-MAR-81 08:08
NEXT HIGHER ASSEMBLY: B-DD-M8189-0
FIRST USED ON OPTION/MODEL: KDF11-B

TITLE: BAUD RATE & -12V

SIZE	CODE	NUMBER	REV.
D	CS	M8189-0-K10	A

CONNECT

J46 TO J45 2ND SLU BAUD RATE SELECTED BY SW. PACK 2 S5-S8 (E114)
J44 TO J45 2ND SLU BAUD RATE DETERMINED BY EXTERNAL SOURCE ON J2 PIN 1

J43 TO J42 CONSOLE BAUD RATE SELECTED BY SW. PACK 2 S1-S4 (E114)
J41 TO J42 CONSOLE BAUD RATE DETERMINED BY EXTERNAL SOURCE ON J1 PIN 1

NOTE: BRG = BAUD RATE GENERATOR

EXT. CLK SOURCE FOR CONSOLE UART
CLOCK INPUT TO CONSOLE UART
CONSOLE BRG OUTPUT

EXT. CLK SOURCE FOR 2ND SLU UART
CLOCK INPUT TO 2ND SLU UART
2ND SLU BRG OUTPUT

J1 J2

J1					J2				
9	7	5	3	1	9	7	5	3	1
10	8	6	4	2	10	8	6	4	2

PINNING FOR J1 & J2
VIEW LOOKING AT MODULE
FROM THE HANDLE END

SIDE 1 (COMPONENT SIDE)
SIDE 2

NOTE: PIN 6 ON J1 & J2 IS A KEYING PIN (NO PIN)

J4 J4 J4 J4 J4 J4
6 5 4 3 2 1

2ND SLU J2
1ST SLU CONSOLE J1

BAUD RATE GEN. CRYSTAL OSC. OUTPUT 5.0688 MHZ
INPUT TO BAUD RATE GENERATOR

J21
J20

GREEN DC POWER OK LED
C4 = DC OK = BDCOK H (BA1) = H
OFF = DC NOT OK

D D D D D
5 4 3 2 1
LSD MSD
BITS 0 1 2 3

J7 BASE TIMING CRYSTAL OSC. OUTPUT 26.666 MHZ
J6 INPUT TO BASE TIMING CIRCUIT

BAUD RATE SELECT

BAUD RATE				
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200
SW#	S4	S3	S2	S1	CONSOLE (J1)
SW#	S8	S7	S6	S5	2ND SLU (J2)

0 = ON
1 = OFF

BAUD RATE SELECTION TABLE.
SET SWITCHES ON E114
ACCORDING TO TABLE ABOVE.

CONSOLE UART CONFIGURATION J36-J40

GROUND TO SELECT ODD PARITY, OTHERWISE EVEN PARITY. ● J40
GROUND TO SELECT 7 BIT CHARACTERS, OTHERWISE 8 BIT. ● J39
GROUND SOURCE ● J38
GROUND FOR 1 STOP BIT, OTHERWISE 2. ● J37
GROUND TO ENABLE PARITY, OTHERWISE DISABLE. ● J36

● J27 OUTPUT OF CONSOLE SLU DRIVER
● J26 CONSOLE CONNECTOR SLU OUTPUT LINE
● J25 CONSOLE SLU INPUT LINE

SIGNAL OUTPUT K1 LINITF (1) H ● J35
INPUT TO CONSOLE UART RESET E129.21 ● J34
SIGNAL OUTPUT -K3 DCOKC2B H ● J33

J34 CONNECTED TO J35 FOR NORMAL OPERATION, J33 NOT CONNECTED.
J34 CONNECTED TO J33 FOR MANUFACTURING APT TEST ONLY.
J35 NOT CONNECTED.

CONNECT J26 TO J27 FOR NORMAL OPERATION
J25 NOT CONNECTED

CONNECT J26 TO J25 FOR FIELD SERVICE WRAP AROUND TESTING
J27 NOT CONNECTED.
THIS ALLOWS A TERMINAL AND ITS CABLE TO BE CHECKED OUT IN LINE MODE WITHOUT THE CPU RUNNING.

2ND SLU UART CONFIGURATION J28-J32

GROUND TO SELECT ODD PARITY, OTHERWISE EVEN PARITY. ● J32
GROUND TO SELECT 7 BIT CHARACTERS, OTHERWISE 8 BIT. ● J31
GROUND SOURCE ● J30
GROUND FOR 1 STOP BIT, OTHERWISE 2. ● J29
GROUND TO ENABLE PARITY, OTHERWISE DISABLE. ● J28

OPTIONAL SOCKET E78 — NOTE: FPF11 MUST PLUG INTO THIS SOCKET IF USED.
OPTIONAL SOCKET E77
OPTIONAL SOCKET E76
DAT/CTL HYBRID E75
MMU E74

J9 INPUT TO MOS CLOCK DRIVER
J8 OUTPUT K1 PHASE (1) H

D1,D3,D4 & D5 ARE THE DISPLAY REGISTER INDICATORS
DISPLAY REGISTER ADDRESS = 777524 WRITE ONLY
WRITE A 1 TO TURN OFF A LED
WRITE A 0 TO TURN ON A LED
POWER FAIL OR RESTART (BDCOK H=L) CLEARS THE REGISTER WHICH TURNS ON ALL 4 LEDS
BITS 15-03 ARE IGNORED

NOTE: E75 AND E78 DO NOT HAVE A .01 UFD CAP CONNECTED TO PIN 1 FOR VBB LIKE E74,E76 AND E77. THEREFORE YOU CAN NOT INSTALL DEVICES WHICH REQUIRE THIS CAP. ONLY HYBRID ASSEMBLIES WITH INTEGRAL VBB CAPS MAY BE INSTALLED IN E75 AND E78.

INTERNAL DEVICE ADDRESSES

	ADDRESS	VECTOR		
CONSOLE				
RCSR (RECEIVE CSR)	777560	60		
RBUF (RECEIVE BUFFER)	777562			
XCSR (TRANSMIT CSR)	777564	64		
XBUF (TRANSMIT BUFFER)	777566			
2ND SLU STANDARD ADDRESS J12 NO CONNECTION (H)				
RCSR (RECEIVE CSR)	776500	300		
RBUF (RECEIVE BUFFER)	776502			
XCSR (TRANSMIT CSR)	776504	304		
XBUF (TRANSMIT BUFFER)	776506			
2ND SLU ALTERNATE ADDRESS J12 GROUNDED (L)				
RCSR (RECEIVE CSR)	776540	340		
RBUF (RECEIVE BUFFER)	776542			
XCSR (TRANSMIT CSR)	776544	344		
XBUF (TRANSMIT BUFFER)	776546			
BOOT/DIAGNOSTIC REGISTERS				
PAGE CONTROL REGISTER	777520		WO	12 BITS 0-5 & 8-13
READ-WRITE MAINTENANCE REG.	777522		R/W	16 BITS
CONFIGURATION REGISTER	777524		RO	8 BITS 0-7
DISPLAY REGISTER	777524		WO	4 BITS 0-3
BEVENT CSR	777546	100	R/W	1 BIT 6
ROM MEMORY ADDRESSES	773000-773777			
LOW BYTE PCR CONTROLS	773000-773377			
HIGH BYTE PCR CONTROLS	773400-773777			

NOTE: THE INTERNAL DEVICES ARE ADDRESSABLE ONLY BY THE CPU ON THE INTERNAL BUS. THIS INCLUDES ALL MEMORY MANAGEMENT AND FLOATING POINT REGISTERS. I.E. YOU CANNOT DO A DMA TRANSFER FROM ANY EXTERNAL OPTION TO ANY OF THE INTERNAL DEVICES.

SWITCH PACK 2 (E114) SELECTS BAUD RATE

SWITCH PACK 2 — E114: S1 S2 S3 S4 S5 S6 S7 S8
SWITCH PACK 1 — E102: S1 S2 S3 S4 S5 S6 S7 S8

CONFIGURATION REGISTER SWITCH PACK 1 (E102)
8 BITS READ ONLY ADDRESS 777524
BITS 15-08 ALWAYS READ AS 0

SWITCH # S8 S7 S6 S5 S4 S3 S2 S1
DATA BIT 07 06 05 04 03 02 01 00

SWITCH ON = 1
SWITCH OFF = 0

ROM/EPROM SOCKET HIGH BYTE 08-15 E127
ROM/EPROM SOCKET LOW BYTE 08-07 E126

WHEN MASKED ROM'S ARE USED CONNECT J24 TO J23, J22 NOT CONNECTED

WHEN EPROM'S ARE USED CONNECT J22 TO J23, J24 NOT CONNECTED

OUTPUT K8 BTRA 13 H
INPUT PIN 21 TO E126 & E127
+5.0V

J J J
2 2 2
4 3 2

BUS GRANT CONTINUITY JUMPERS
W2 W1
W1 BIAKO/I
W2 BDMGO/I
W1 & W2 MUST BE INSTALLED WHEN USING A 0/0 BACKPLANE

POWER UP MODE SELECTION

MODE	NAME	J19	J17
0	PC @24,PS @26	N/C	N/C
1	CONSOLE ODT	N/C	GND
2	BOOTSTRAP 773000	GND	N/C
3	EXTENDED MICROCODE JUMP TO CONTROL CHIP #37	GND	GND

CONNECT J5 TO J4 FOR NORMAL OPERATION. J3 NOT CONNECTED. FRAMING ERROR (BREAK) FROM CONSOLE IGNORED.

CONNECT J3 TO J4 TO HALT CPU IF BREAK RECEIVED FROM CONSOLE. J5 NOT CONNECTED

● J5 GROUND
● J4 INPUT K9 RQ HLT H
● J3 OUTPUT K9 DL1 FE H

● J19 SEE POWER UP MODE TABLE ABOVE. PUP CD1J L
● J18 GROUND SOURCE
● J17 SEE POWER UP MODE TABLE ABOVE. PUP CD0J L
● J16 GROUND TO TRAP TO LOC. 10 IF HALT EXECUTED IN KERNEL MODE. OTHERWISE HALT AND ENTER CONSOLE ODT.
● J15 GROUND TO DISABLE BOOT/DIAG. ROM & CLOCK LOGIC
● J14 GROUND TO DISABLE SLU #1 (CONSOLE)
● J13 GROUND TO DISABLE SLU #2
● J12 GROUND TO SET SLU #2 REGISTER ADD'S TO 776540/340 OTHERWISE 776500/300
● J11 GROUND TO SET THE LINE CLK INTERRUPT ENABLE F/F (BEVENT ALWAYS ENABLED), OTHERWISE BIT 6 OF CSR (777546) CONTROLS F/F.
● J10 GROUND SOURCE

NOTE: IF BDV11 IS USED WITH KDF11-B AND BDV11 CONTROLS BEVENT, THEN J15 AND J11 MUST BE GROUNDED.

IF BDV11 IS USED WITH KDF11-B AND BEVENT IS TO BE IGNORED THEN J15 MUST BE GROUNDED BUT NOT J11.

BIT 6 = 1 BEVENT ENABLED IF PSW PRIORITY < 6
BIT 6 = 0 BEVENT DISABLED

BEVENT VECTOR = 100

A A A A A A A A A A A A A A A A
V U T S R P N M L K J H F E D C B A
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

DV1 DP1 CV1 CA1 BIV1 BA1

REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. M Cullejin DATE 05-MAR-81
CHK'D M Cullejin DATE 4-13-81
ENG. Charlie Valente DATE 4-7-81
BOARD LOCATION:
SHEET 1 OF 1

[365,3132]M8189A.DRW 05-MAR-81 08:42
FIRST USED ON OPTION/MODEL: KDF11-B
NEXT HIGHER ASSEMBLY: B-DD-M8189-0

TITLE: CONFIGURATION GUIDE

SIZE	CODE	NUMBER	REV.
D	CS	M8189-0-K11	A

K11
DRAWING
11 OF 11

DRAWING DIRECTORY

NOTE:

FOR FIELD MAINTENANCE PRINT SET REFER TO B-TC-KEF11-BB-1

UNIT VARIATIONS

VAR	TITLE
KEF11-BB	HYBRID C.I.S. MICROCODE CHIP.

REVISIONS

REV.	CHANGE NO.	CHK
A	INITIAL	

USED ON OPTION/MODEL

KEF11-BB

SHEET 1 OF 2

DRN. A. AMICO	DATE 21JAN81	
CHK'D. ROBICHAUD	DATE 08APR81	
PROJ. ENG. K. AMUNDSEN	DATE 8 May 81	
PROD. Greg Nyleth	DATE 9-Jun-81	

TITLE: DRAWING DIRECTORY KEF11-BB

digital

SIZE	CODE	NUMBER	REV
B	DD	KEF11-BB	A

DIST.

DRB 106A

MC-3

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE
1	MPØ1223-ØØ	KEF11-BB PRINT SET ORDER NO. (MP)	-
	B-TC-KEF11-BB-1	FIELD MAINTENANCE PRINT SET (TC)	-
	K-PL-KEF11-BB-DBP	COMMERCIAL INSTRUCTION SET (KEF11-BB)	E/M
	B-PL-KEF11-BB	SHIPPING LIST KEF11-BB	E/M
2	B-DD-5700006-0	CIS MODULE	E/M
3	A-PS-9905812-0-0	BOX, PAPER SET-UP WITH FOAM	M

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE

TYPE: E ELECTRICAL
M MECHANICAL
E/M ELECTRO/MECHANICAL

digital

TITLE	SHEET	SIZE	CODE	NUMBER	REV
DRAWING DIRECTORY KEF11-BB	2 OF 2	B	DD	KEF11-BB	A

DRB 108A

ML-3