Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-10
TD10 Dectape Control
Maintenance Manual

PDP-10
TD10 DECTAPE CONTROL MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION ▫ MAYNARD, MASSACHUSETTS

1st Printing June 1968
2nd Printing June 1969

Instruction times, operating speeds and the like are included in this manual for reference only; they are not to be taken as specifications.

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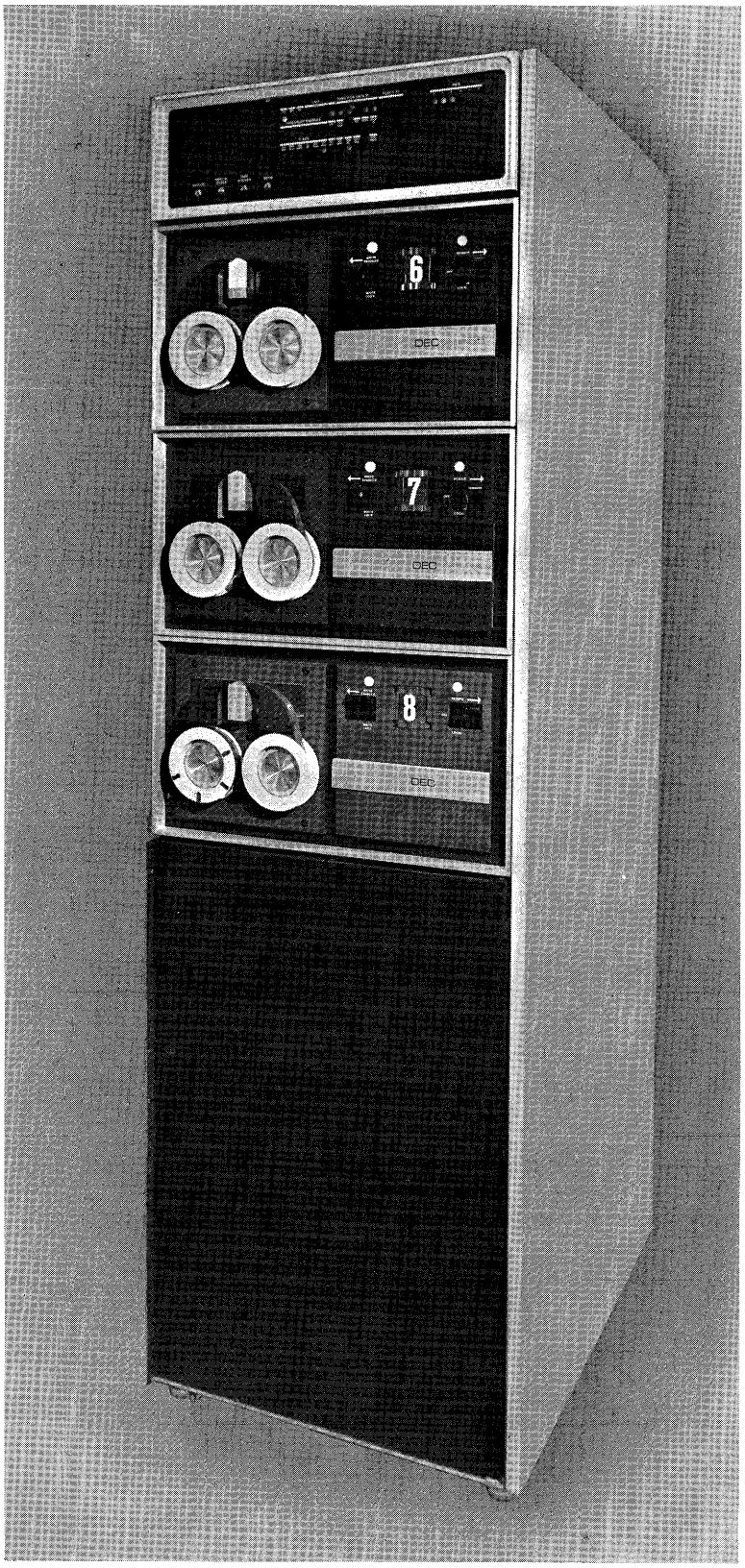


TD10A DECtape Control Unit

CHAPTER 1
INTRODUCTION

This manual and the referenced documents provides operating and maintenance information for the TD10 DECtape Control manufactured by Digital Equipment Corporation, Maynard, Mass., for use with the PDP-10 Digital Data Processor. The TD10 DECtape control is a peripheral device used to buffer and control the transfer of information between the PDP-10 Processor and TU55 DECtape Transport. The level of discussion in this manual assumes that the reader is familiar with DEC logic, PDP-10 operation, and operation of the TU55 Transports.

1.1 GENERAL DESCRIPTION

The TD10 DECtape Control interfaces the PDP-10 Central Processor and up to eight TU55 DECtape Transports as shown on Figure 1-1. Two-way communication is provided between the PDP-10 I/O bus and the TU55 Transport tape.

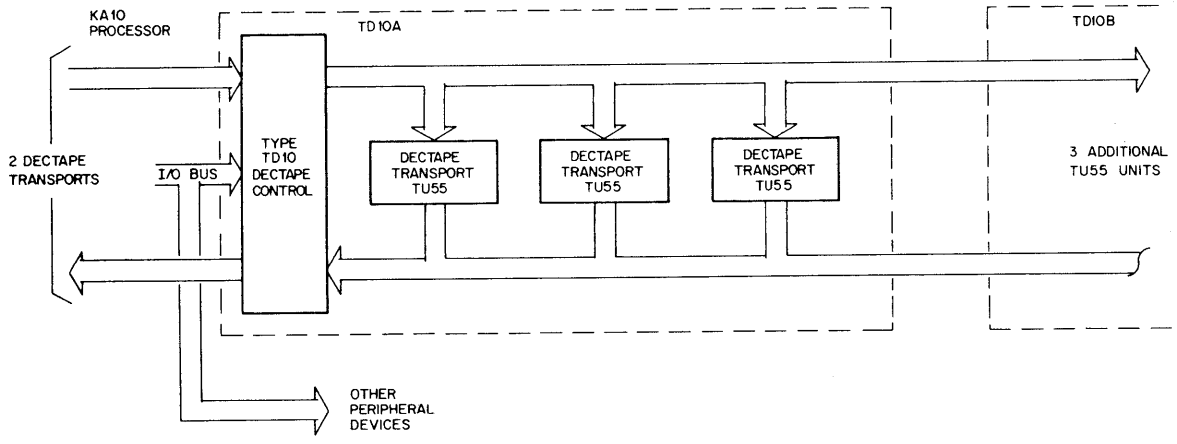


Figure 1-1 System Configuration (TD10A or TD10B)

The TD10A interfaces a maximum of five TU55 units with the standard PDP-10/20, 10/30, 10/40 and 10/50 systems. If six or more TU55 units are provided, the TD10B is required with the TD10A.

During both input and output operations the TD10 receives control information from the PDP-10 and generates the appropriate signals to the selected transport to execute the programmed commands.

All required control timing is derived from the timing and mark tracks information prerecorded on DECtape. Sensing is provided for inhibiting data flow until tape motion is up to speed, and for

monitoring the end zones on tape to prevent tape from unwinding from the reels when the end of tape is reached. All data is read into and out of the TD10 via the I/O bus. Control signals are also sent on separate lines of the I/O bus which are decoded by the TD10 to generate command signals. Since all I/O devices are connected to the I/O bus in parallel, 14 lines are provided for an address selection code. The TD10 monitors these lines and becomes active when its own address is decoded. Control pulses to the TD10 trigger a pair of pulses which clear the control register of the TD10 and strobe the commands into the register. When it is requested by program, TD10 status information is sent back to the computer.

1.2 REFERENCED PUBLICATIONS

The publications listed in Table 1-1 are available to supplement the information contained in this manual. These documents can be obtained from the nearest DEC office or by a request to:

Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

Table 1-1
Referenced Documents

Title	Doc. No.	Description
TU55 DECtape Transport Instruction Manual	H-TU55	Operation and maintenance information on the TU55 DECtape Transport.
PDP-10 Maintenance Manuals Volume I (KA10 Processor)	DEC-10-HMAA-D	Operation and maintenance information on the internal operation of the KA10 processor, memory, basic I/O and options.
Volume II (Engineering Drawings)	DEC-10-HMBA-D	Block schematics and wiring information of the KA10 Processor.
Volume III (Special Modules)	DEC-10-HMCA-D	Description, specifications and schematic of the special modules used in the PDP-10 system.
Digital Logic Handbook	C-105	Description, specifications and application information on FLIP CHIP modules, DEC power supplies, cabinet and hardware.

Table 1-1 (Cont)
Referenced Documents

Title	Doc. No.	Description
Peripheral Device Engineering Drawing Set, Volume II	DEC-10-I6BA-D	Block schematics and wiring information for the DC10 and TD10 Units.
PDP-10 Installation Manual		Preliminary installation information on the KA10 processor and associated options.
PDP-10 System Users Guide	DEC-10-NGCA-D	Operators reference guide containing the basics of Teletype usage and operating procedures for Common User Service Program.
PDP-10 System Reference Manual	DEC-10-HGAA-D	Description of the PDP-10 central processor and programmers information on basic instruction repertoire.

1.3 PHYSICAL DESCRIPTION

Both the TD10A control and TD10B include a standard 19-inch DEC cabinet Type CAB9-B. The cabinet is constructed of a welded steel frame, enclosed by sheet steel panels as required. A half height single door mounted on the lower front of the cabinet provides access to the wiring side of the logic panels. A hinged full width plenum door, mounted on the rear provides mounting space for power supplies and power control panels. The plenum door is covered by a single, full height door. A single fan mounted at the bottom of the cabinet draws filtered air. Three blower fans mounted in an assembly below the logic modules circulate the filtered air throughout the dabinet. The cabinet is supported on four casters which allow the unit to be easily positioned.

The general specifications for the TD10A/TD10B are listed as follows:

	TD10A	TD10B
Cabinet Dimensions (in)	27 x 21-1/4 x 69	27 x 21-1/4 x 69
Weight (lbs)		
Cabinet (1)	160	160
TU55 Transport (3)	195	195
728 Power Supply (2)	40	---
844 Power Control Panel (1)	18	---
Modules and Mounting Panels (4)	30	---
Totals	433	355

	TD10A	TD10B
Cabinet Color	Black	Black
Environmental	Min. - Max.	
Operating temperature (F)	60° - 90°	
Storage Temperature (F)	40° - 110°	
Humidity (Rel)	20% - 80%	
Wet Bulb (max. F)	78°	
Power Requirements		
Voltage (ac)*	Single Phase 115V ± 10% 60 Hz ± 2 Hz 230V ± 10% 50 Hz ± 2 Hz	
Current (a) @ 115V (nominal)		
Without Transport	2.5A	----
TU55 Transport (1)	1.0A	1.0A
Power Dissipation (w)		
Without Transport	200	----
TU55 Transport (1)	150	150
Heat Dissipation (BTU/hr)		
Without Transport	628	----
TU55 Transport (1)	510	510

*Other line voltages can be accommodated.

1.3.1 TD10A Assembly

The TD10A assembly consists of four DEC mounting panels, Type 1943 which contain the FLIP CHIP modules, a control panel, two Type 728 and 728A (50 Hz) Power Supplies, a Type 844 Power Control assembly and sufficient cabinet space to mount a maximum of three TU55 DECtape Transports. Provisions are made within the KA10 console of the PDP-10 processor to mount two TU55 Transports. The TD10A cabinet can be bolted directly to the right side of the KA10 processor in which case all interconnecting cables are run internally. Figure 1-2 shows the TD10A cabinet configuration.

1.3.2 TD10B Assembly

The TD10B assembly is used in addition to the TD10A unit when more than five TU55 units are required for the system. Essentially this cabinet provides only mounting space for a maximum of three TU55 units together with the blower assembly. The power and signals are provided by cable from the TD10A unit.

The cabinet configuration is similar to the TD10B except that blank filler panels enclose the areas within the cabinet which normally provide mounting space for logic panels and power supplies. Figure 1-3 provides the assembly location information for the TD10B unit.

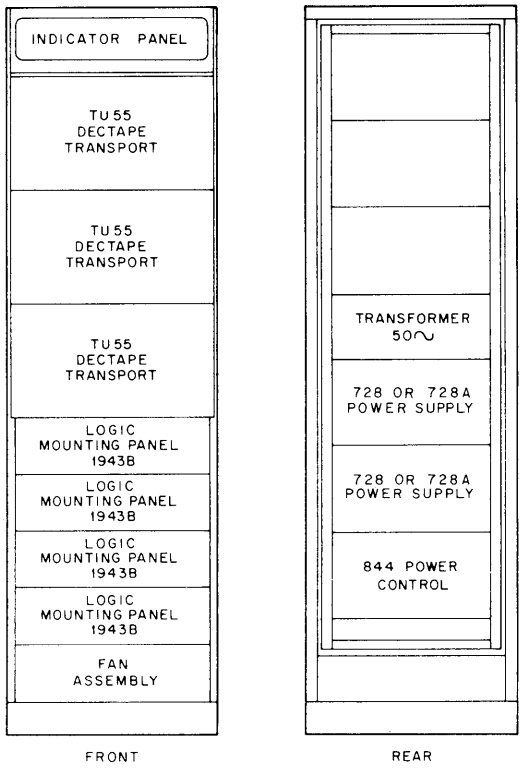


Figure 1-2 TD10A Unit, Assembly Location

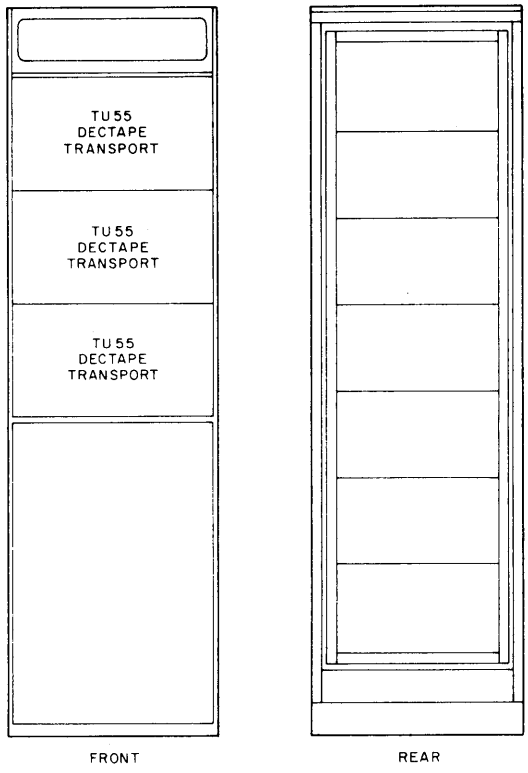


Figure 1-3 TD10B Unit, Assembly Location

CHAPTER 2
OPERATION AND PROGRAMMING

This section contains the information required for operation and programming of the TD10 DECtape Control. This information includes a description of the recording format and recording method used with DECtape and general information on the program instructions and codes. In addition, the operating controls and indicators are listed, together with a functional description of each. The pertinent operating information for the TU55 DECtape Transport is located in the TU55 DECtape Transport Instruction Manual.

2.1 RECORDING METHOD

Data is recorded by the Manchester method in which a prerecorded timing track synchronizes the reading and writing of data on tape. When writing on tape, maximum current is supplied to the read/write heads in one direction or the other depending on whether a zero or one is specified and a pulse is written by reversing the current. The timing track is prerecorded with alternate positive and negative transitions at fixed time intervals. These transitions are used to load information into the buffers, for both reading and writing of information on tape and for reversing the current. The timing track strobe is a relatively narrow pulse noise which is present between the strobe times, and does not affect the operation of the control.

2.2 DECTAPE FORMAT

The tape format used with the DECtape consists of 10 tracks of which three pairs of tracks are available for data and two pairs of tracks each for the timing and mark track information. Figure 2-1 shows the track allocations. A 10-track recording head reads and writes the five duplexed channels on tape. Duplication of each track by nonadjacent read/write heads, wired in series, tends to eliminate bit dropouts due to noise and dust, and the location of the redundant tracks minimizes crosstalk between tracks. The location of the information tracks in the middle portion of the tape minimizes the effects of skew. The location of the timing tracks along the edge of tape allows strobing on the analog sum of the timing track signals and reading of the data tracks at the most favorable position. Each mark track code consists of two octal digits of six serial bits on tape. The mark track bits are positioned in line with the three bits of data or control information as shown on Figure 2-2. A control word that consists of 6 lines or 18 bits normally occupies the area within one mark track code and a data word that consists of 12 lines or 36 bits occupies the area within 2 mark track codes. Information is recorded on tape in block form as shown on Figure 2-3. A maximum of 578 blocks can be written on a complete reel of tape (260 ft) which provides approximately 6 ft of tape at each end for the end zones. A uniform block

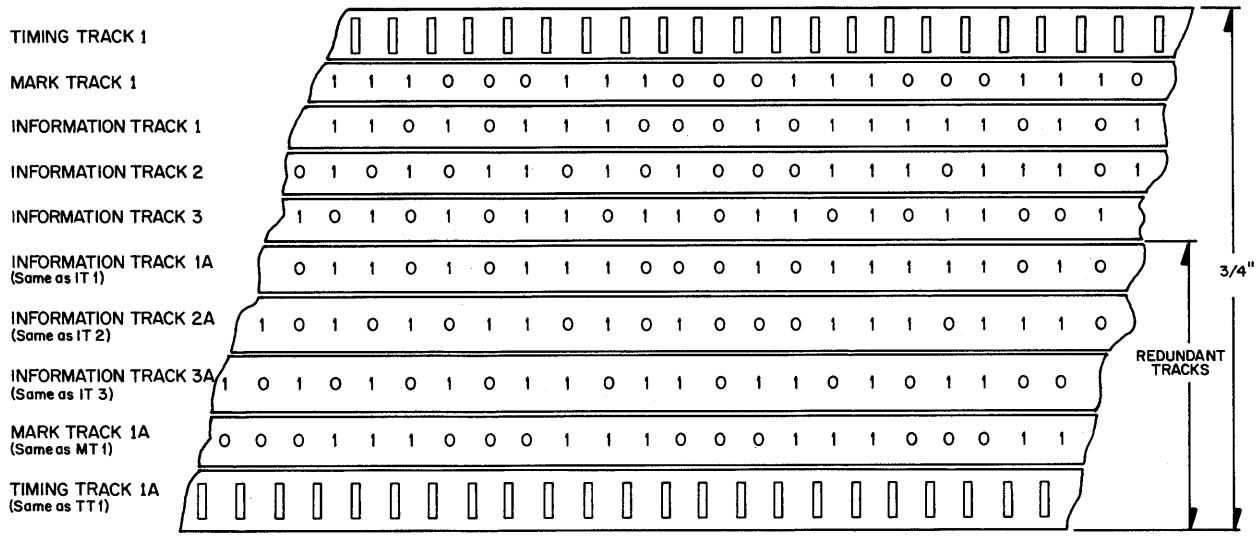


Figure 2-1 DECtape Track Allocations

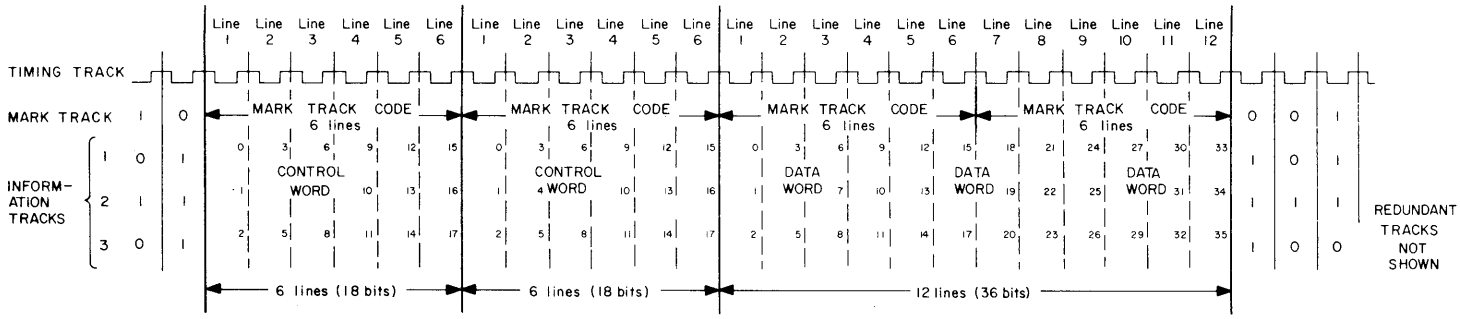


Figure 2-2 DECtape Word Assignments

length is usually established over the entire length of tape by a program which writes the timing and mark track information at specified locations; however, variable length blocks can be written.

Each block consists of data and control information which is assembled by the TD10 control. A uniform block normally consists of 133 36-bit words of which 128 are data words and 5 words are allocated for control information. Because 3 bits are written on tape at one time, 12 bit-times are required to write a full 36-bit word.

Control information is positioned at both ends of the data information on tape to facilitate reading and writing with a forward or reverse tape motion. The control words record address and parity checking information.

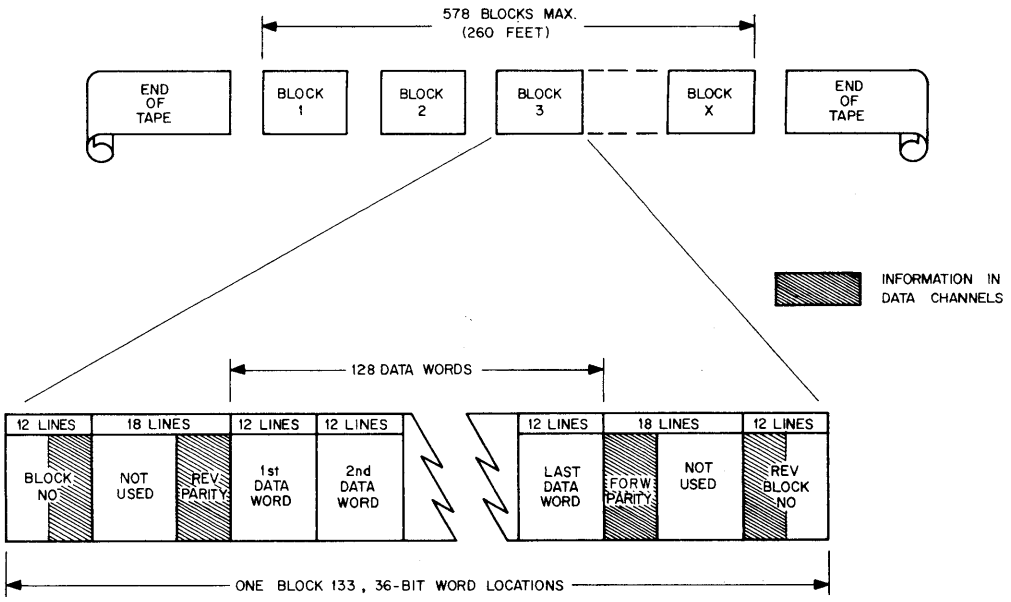


Figure 2-3 DECtape Block Format

Block numbers normally occur in sequence from 0 to 1101 octal. Codes are written on the mark track opposite word locations to identify the type of information stored at that location on tape. Block addresses are written for both forward and reverse directions and identified by two types of mark codes. A checksum is written at each end of the block. The hardware computed checksum is the 6-bit logical equivalence (i.e., the complement of the exclusive OR) of each six bits written on tape plus the reverse checksum previously recorded. By including the reverse checksum in the computation, the block may be read in either direction at a later time without an error. The control uses the final marks to establish synchronism and raise block-end flags. Data marks locate data words. The actual number of blocks written on tape is a function of the number of data words per block.

2.2.1 Mark Track

The mark track contains 6-bit serially stored codes which initiate controls to raise flags in the program, request data breaks, detect block numbers and block ends, and protect control portions of the tape. The mark and information for a complete tape is shown on Figure 2-4. The DECtape control automatically identifies these codes. The mark track also provides for automatic bidirectional compatibility, variable block formatting, and end-of-tape sensing.

In all tape processing functions, except the recording of the timing and mark tracks, a single mark track bit is read from each line of tape regardless of whether the information is being read or written

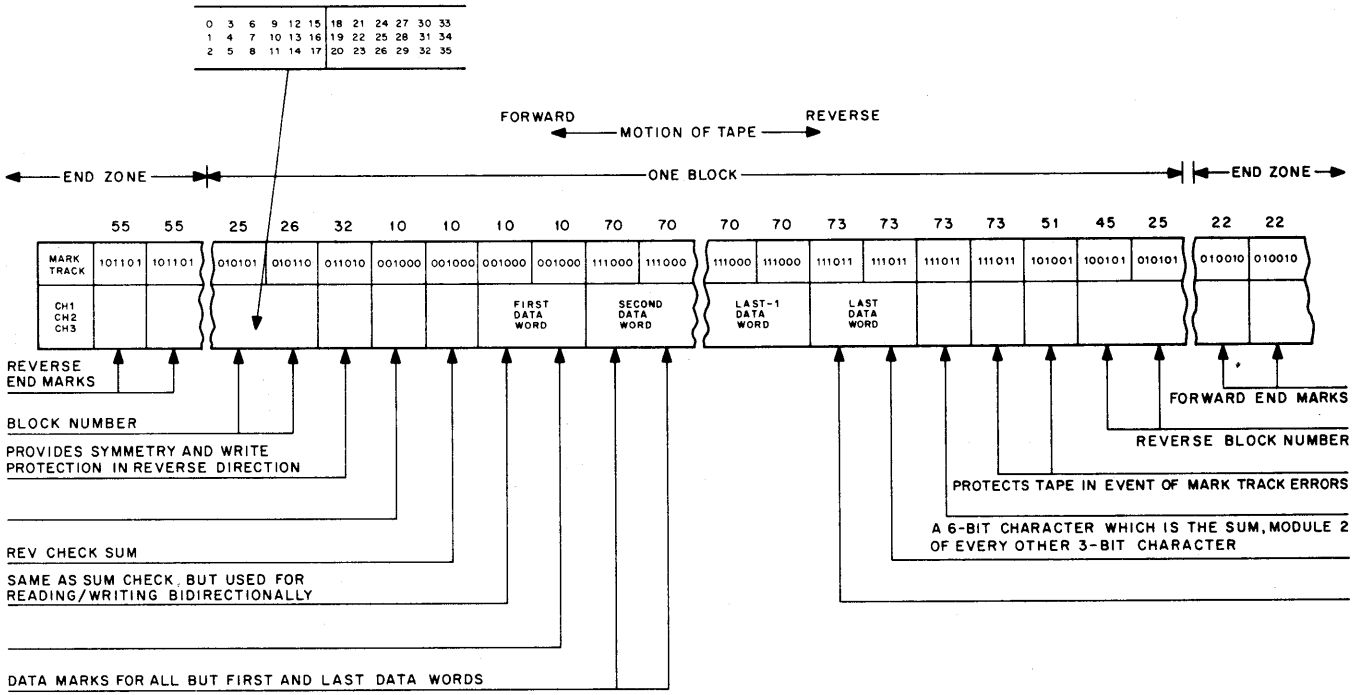


Figure 2-4 DECtape Mark and Information Tracks

into the data tracks. Each tape line in both the information and mark tracks is positioned at the center of the right polarization in the timing track.

A given change of polarization on tape read in one direction produces a pulse opposite in polarity to that produced by the same change read in the opposite direction. Consequently, a mark code read in reverse has the order of bits reversed and the bits complemented.

A mark-track code read forward as 100101 is read as 010110 in reverse, or the complement obverse or the complement image. Every 6-bit code has only one complement obverse which is constructed by complementing all bits and reversing their order. The complement obverse of the complement obverse is, therefore, the original code itself. In octal notation, the complement obverse of any pair of digits is constructed by reversing the order of digits, then performing the following transformation on each:

0 → 7	1 → 3	2 → 5	3 → 1
4 → 6	5 → 2	6 → 4	7 → 0

The eight octal codes which are their own complement obverses are 07, 13, 25, 31, 46, 52, 64, and 70. All other possible combinations of two octal digits are different from their complement obverses. As shown in Table 2-1, the complement obverse of any mark is designated by a minus sign.

Since the DECtape system allows reading and writing in both directions of tape motion, the mark track is coded to present the same information when entering a block from either direction. The marks at the end of a block are the complement obverses of the marks at the beginning, in reverse order. If the control reads the marks 25, 26, and 32 as the first three marks beginning a block in forward motion, then it will read -32, -26, and -25, as the last three marks of the same block. In reverse motion, however, the control recognizes the complement obverse of the contents of the mark track; thus the first information, when reading the block in reverse, is -(-25), -(-26), and -(-32), which is identical to 25, 26, and 32.

The marks used in the standard DECtape format are listed in Table 2-1. Only ten valid codes exist even though a given code may have different designations. Some of these marks are not decoded for the operation of Type TD-10 DECtape Control.

A block begins and ends with a number of words used for timing and control functions. The first of these is the block number which is a 36-bit number used as a label in programming to locate a desired block of information. A tape prerecorded in the standard manner has block numbers from 0 to 1101_8. Two mark codes appear in the mark track opposite the block numbers. These are block number spaces (25_8 and 26_8). The block-number space (25_8) is its own complement obverse and, therefore, appears again opposite the reverse block number (45_8) at the end of the block, immediately adjacent to the block-number space which is part of the following block. This mark consisting of alternate ones and zeros in its binary representation and end zone (22_8) are the only marks which legitimately occur more often than once in six bit positions. The data sync mark code (32_8) signifies that data follows and is used to synchronize data transmission operations so that transmission begins following the next checksum. If data transmission is in progress while this mark is read and a mark track error is detected, transmission is stopped and an error flag is raised. The 18 bits of data opposite this mark are normally unused. The reverse data end mark (10_8) is present for timing purposes to provide additional time in which the arithmetic processor can command the DECtape control to switch from reading block marks to reading or writing data.

Eighteen bits of data comprise the reverse checksum. For symmetry, there is a checksum at each end of a data block. The checksum is a parity check of all 6-bit bytes transmitted between the data control and the DECtape control. The six bits of the checksum are written out once and the remaining 12 bits of the checksum slot are filled with ones. If a data block is written in the forward direction, the reverse checksum is preset to 777777_8.

Table 2-1
Mark Track Coding

Mark	Octal Code	Function
Lock	10	Indicates the first of four octal 10 marks.
Reverse Check	10	Signifies that the 6-bit reverse longitudinal parity check group is contained in the control unit read/write buffer and that the beginning of the data portion of a block is in the forward direction.
Reverse Prefinal	10	In the reverse tape direction, signifies the next to last mark in the data portion of a block.
Reverse Final	10	Signifies that the last word read from the block, in the reverse direction, is in the read/write buffer and data buffer.
End (Forward)	22	A series of end marks which indicates the end zone of tape in forward direction and positioned approximately 10 ft from actual tape end.

Table 2-1 (Cont)
Mark Track Coding

Mark	Octal Code	Function
Extension	25	The first and last mark of every block (no-op mark).
Forward Block	26	Signifies the start of a block and indicates that the block number is contained in the TD10 control.
Reverse Guard	32	Data Sync to indicate the start of a data block.
Reverse Block	45	Not used.
Block Number Sync	51	Performs same function as reverse lock.
-End (Reverse)	55	A series of end marks which indicate the end zone of tape in reverse direction and positioned approximately 10 ft from end of tape.
Data	70	In both forward and reverse tape motion, the data mark occupies all mark frames in the data portion of the block except for the final and prefinal marks. The number of data marks is limited only by the length of tape.
Forward Check	73	Signifies the end of a mark frame whose first two lines were the forward parity check group.
Final	73	Signifies that the last word read from the data portion of the block is in the read/write buffer and data buffer. Signals that the next frame begins with the 6-bit forward longitudinal parity check group.
Reverse Lock	73	Protects subsequent records in the event of mark-track errors.
Prefinal	73	In the forward tape direction, the prefinal mark is the next to last mark in the data portion of a block. It is the first of four marks using octal code 73.

If the data block is written in the reverse direction, the reverse checksum contains the computed checksum. In this case the forward checksum is preset so that the final result, if correct, is all ones. During reading, the checksum of all words, including both the reverse and forward checksums, is recomputed automatically; and if the result is not all ones, the parity error flag is raised.

The remaining reverse data end marks (10_8) indicate that the first data word and mark-track code (70_8) define all 36-bit data words from the second to the next-to-last word in a block. Every two data marks delimit one 36-bit word. A 2-word block requires no data marks because the reverse and forward data end marks are sufficient to delimit two data words. A 0- or 1-word block is improper and cannot be read. Longer blocks have as many data marks as required to delimit all data words. The data mark is its own complement obverse so that the same mark delimits data words in both directions of tape motion.

The first two mark track codes (73_8) define the last data word to be written and are followed by checksum (73_8) which was previously defined in the reverse checksum.

The reverse block number completes the symmetry of a standard block. The two mark-track codes that delimit the reverse block number are 45_8 the complement obverse of block number end which is ignored and 25_8 block number space which is its own complement obverse and is discussed above. The forward block number of the next block immediately follows the reverse block number. Approximately the first and last 10 ft of each reel of DECtape are devoted to consecutive end-mark codes. The forward end marks (22_8) appear at the end of the tape and, when read in the forward direction, cause the DECtape control to stop tape motion. The reverse end mark (55_8, the complement obverse of the forward end mark) is ignored. A tape which has moved into the end zone can be moved back into the center of the tape under program control.

2.3 PROGRAMMED OPERATIONS

Before the Type TD10 DECtape Control is used for data storage, the prerecording of a reel of DECtape is accomplished in two passes. In the first pass, the timing and mark tracks are placed on the tape. During the second pass and the forward and reverse block, numbers are written. These functions can be performed by the program. Prerecording utilizes the WRTM control function and the manual switch on the control panel of the Type TD10A Tape Control to write on the timing and mark tracks, to activate a clock which produces the timing track recording pattern, and to enable flags for program control. Unless the WRTM control function and switch are used simultaneously, the writing on the mark or timing channels is inhibited. The mark track can be written only when the switch is in the WRTM position. Only one prerecording operation is required for each reel of DECtape.

The TD10 DECtape Control decodes two device numbers from the PDP-10 input/output instruction to initiate the transfer of data, status, and control information. Device number 320 selects control register functions (DTC) to allow control and data information to be transferred. Device number 324 selects a status register function (DTS) which permits the transfer of status, interrupt enables, and error conditions. Device numbers 330 and 334 may be assigned to a second TD10A control if required.

A command to the DECtape consists of either a Conditions Out (CONO) or Conditions In (CONI) to the DTC. Conditions In, however, transmits the current command back to the processor. The 18-bit control register configuration is shown in Figure 2-5 and the bit assignments are listed in Table 2-2.

A CONO to the DTS device number transfers status register information to the control from the processor to select interrupt enable bits and Function Stop to stop transmission of data and to terminate a read or write operation and stop transport motion. The bit configuration for the CONO (DTS) is shown in Figure 2-6 and listed on Table 2-3.

A CONI from the selected DTS device number transfers all status levels from the control status register to the PDP-10 processor.

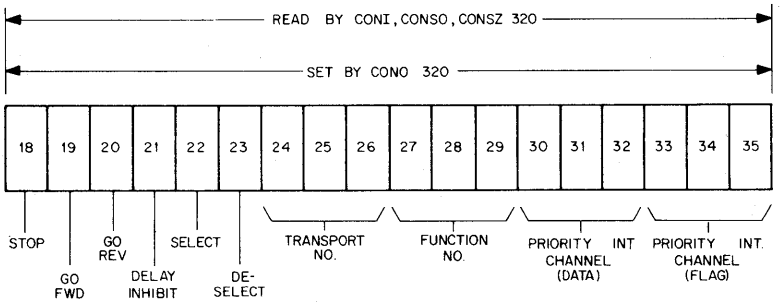


Figure 2-5 CONO DTC Control Register Bit Assignments

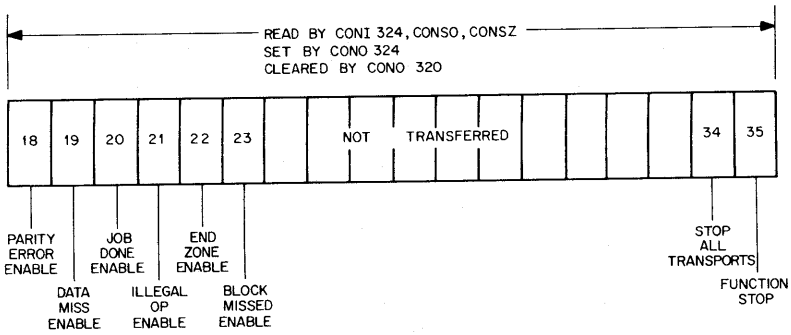


Figure 2-6 CONO DTS Status Register Bit Assignments

Table 2-2
CONO DTC Bit Function

Bits	Function
18-20	Selects transport motion Bit 18 = Stop (1) Bit 19 = Go forward (1) Bit 20 = Go reverse (1) Bits 19 and 20 given together cause a turnaround. If bit 18 is a one, bits 19 and 20 should be zero. All zeros in bits 18-20 cause no change in transport motion.
21	Delay Inhibit. - Inhibit the 120-ms delay used to allow the transport to come up to speed. This delay is suppressed when reselecting a transport that is already up to speed by sending the delay inhibit bit. This bit is ignored if all deselected tapes are stopped.
22	Select. - Enables the selection of a particular transport. This bit should be a one whenever a new transport is selected.

Table 2-2 (Cont)
CONO DTC Bit Function

Bits	Function
23	Deselect. - Deselects all transports and clears the transport number register. This bit is sent whenever the control must disconnect from the current transport or whenever the select bit is sent.
24-26	Transport Number. - Selects one of eight DECtape transports by the following configuration. Ones in bits 24-26 OR into the transport number register. Bits 24 25 26 = Transport Number 0 0 0 = 8 0 0 1 = 1 0 1 0 = 2 0 1 1 = 3 1 0 0 = 4 1 0 1 = 5 1 1 0 = 6 1 1 1 = 7
27-29	Function Number. - Selects the read/write function of the transport as follows. 0 = Do nothing 1 = Read all 2 = Read block number 3 = Read data 4 = Write mark and timing tracks 5 = Write all 6 = Write block number 7 = Write data
30-32	Selects the PI channel for data interrupts.
33-35	Selects the PI channel for flag interrupts.

Table 2-3
CONO DTS Bit Assignments

Bits	Function
18	Parity Error Enable. - Allows the parity error bit to cause an interrupt on the flags channel.
19	Data Missed Enable. - Allows the data missed error bit to cause an interrupt on the flags channel.
20	Job Done Enable. - Allows the job done bit to cause an interrupt on the flags channel.
21	Illegal Operation Enable. - Allows the illegal operation error bit to cause an interrupt on the flags channel.

Table 2-3 (Cont)
CONO DTS Bit Assignments

Bits	Function
22	End Zone Enable. - Allows the end zone bit to cause an interrupt on the flags channel.
23	Block Missed Enable. - Allows the block missed bit to cause an interrupt on the flags channel.
34	Stop all Transports. - This bit causes all transports except the selected transport to stop. The selected transport continues in motion if forward or reverse motion is currently selected.
35	Function Stop. - This bit signals the end of a read or write data operation. If sent while the tape is between blocks, the current operation terminates and the job done flag is set. If the bit is sent at any other time, the control continues if reading, to read to the end of the current block and check the checksum; if writing, to write the last word sent repeatedly until the end of the current block and to write a correct checksum. At the end of the current block, the job-done flag comes on. The data missed flag cannot be set after this bit is sent but may be set prior to the function stop.

The cause of an interrupt can be determined by these status levels which are useful in programming DECtape operations. The CONI instruction from the DTS transfers the 36 bits of status information as listed on Table 2-4. Bits 0-17 are tested by TLNE and TLNN instruction in the processor. The CONSZ and CONSO instructions transfer only bits 18-35 of the status information. The bits which are set by the CONO DTS instruction (18-35) are read back by the CONI DTS instruction as bits 0-17. The CONO to DTC instruction clears all 36 bits of the status register.

Table 2-4
CONI DTS Bit Indications

Bit	Function
0	Parity Error Enable
1	Data Missed Enable
2	Job Done Enable
3	Illegal Operation Enable
4	End Zone Enable
5	Block Missed Enable
6	Delay in Progress. - This bit is a one when the control is waiting for a transport to connect or to turnaround.
7	Active - The control is busy transferring data.
8	Up to Speed. - This bit is a one when the tape is actually moving fast enough for successful reading or writing.

Table 2-4 (Cont)
CONI DTS Bit Indications

Bits	Function
9	Block Number. - This bit is a one when the DECtape control is in the process of reading a block number.
10	Reverse Check. - This bit is a one when the DECtape control is processing a reverse checksum.
11	Data. - This bit is a one when the DECtape control is processing data.
12	Final. - This bit is a one when the DECtape control is processing the last word in a block. The data bit will be off when this bit is on.
13	Checksum. - This bit is a one when the DECtape control is processing the final checksum.
14	Idle. - This bit is a one when the tape is between blocks.
15	Block Number Read. - This bit is set to one when the control reads a block number from the tape. The bit is cleared when the reverse-check bit comes on. A CONO to read or write data, given when the block-number-read bit is off, causes the block missed flag to come on.
16	N.U.
17	Function Stop
18	Parity Error. - This bit is a one if any of the blocks read since the last CONO DTC had a checksum failure or if the mark-track-error bit is on.
19	Data Missed. - This bit is a one if a data request is not answered within 266 μs.
20	Job Done. - This bit is set when a block number is read or written if the command is read or write block numbers; when the checksum is read or written when the command is read or write data, and function stop or data missed is on; when data transmission finally ceases during all mode.
21	Illegal Operation. - This bit is set whenever any of the following manual switch settings conflict with the command sent by the program; write lock when trying to write; write timing and mark track switch off while trying to write timing and mark track or on while not trying to write timing and mark tracks; no units dialed to the selected transport number or more than one unit dialed to the same number.
22	End Zone. - This bit is set when the tape moves into the end zone, and the end zone mark from the tape is sensed. The DECtape control automatically stops the tape when the end zone bit comes on.
23	Block Missed. - This bit is set if a read block number operation is followed by a read or write data operation too late to catch the current block.
24	Write Lock. - This bit is a one when the selected transport has its switch set on the write lock position.
25	Write Mark and Timing Switch. - This bit is a one when the write mark and timing track switch in the control is set.

Table 2-4 (Cont)
CONI DTS Bit Indications

Bits	Function
26	Incomplete Block. - This bit is set when function stop is given or data missed occurs during the reading or writing of a block. This bit is not set if reading or writing stops between blocks.
27	N.U.
28	Mark Track Error. - This bit is set when a valid mark track code fails to appear every sixth bit time or if reading or writing is not terminated when a sync mark appears.
29	Select Error. - This bit is set to one if no unit or more than one unit is dialed to the selected transport number.
30-33	N.U.
34	Flag Request. - This bit is on whenever any of bits 18-23 is a one and its corresponding enable bit is also a one. The flag request bit means that an interrupt is being requested on the flags channel.
35	Data Request. - This bit is on during reading to request that the program read in a data word from the DECtape control. It is on during writing to request the program to transmit the next word to be written. This bit requests an interrupt on the data channel. Satisfying the request or sending a function stop clears the data request bit.

2.4 CONTROLS AND INDICATORS

The control and indicator panel located on the top of the TD10A provides manual selection of specific functions of tape operations and presents a visual indication of the status of the control. The control panel is shown on Figure 2-7 and the function of the controls and indicators are listed on Table 2-5.

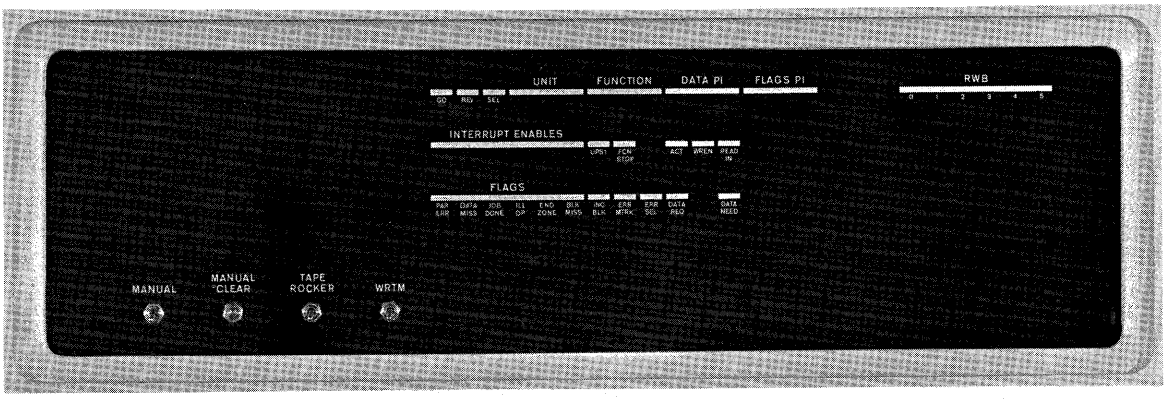


Figure 2-7 Control Panel, Switches and Indicators

Table 2-5
TD10A Controls and Indicators

Control/Indicator	Function
	INDICATORS
GO (1)	Lights to indicate transport motion.
REV (1)	Lights to indicate that selected transport motion is in reverse direction.
SEL (1)	Lights to indicate that a tape transport is selected.
UNIT (3)	Displays the number of the selected transport in binary.
FUNCTION (3)	Displays the command register function of the selected transport in binary as follows. 000 - No operation 001 - Read All 010 - Read Block Numbers 011 - Read Data 100 - Write Mark and Timing Tracks 101 - Write All 110 - Write Block Number 111 - Write Data
DATA PI (3)	Displays channel number for Data Priority Interrupts in binary.
FLAG PI (3)	Displays channel number for Flag Priority Interrupts in binary.
INTERRUPT ENABLES (6)	Lights to indicate that the corresponding flag is enabled to cause an interrupt on the flag channel.
UPS1 (1)	Lights to indicate that the selected transport has reached operating speed in either the forward or reverse direction.
FCN STOP (1)	Lights to indicate the end of a read data, read all, write data, write all function.
ACT (1)	Lights to indicate that the control is transferring data.
WREN (1)	Lights to indicate that a write enable level is present to allow writing on tape.
READ IN (1)	Lights to indicate that the KA10 processor has initiated a read in operation from DECtape. Also lights when the TAPE ROCKER switch is "on."
	FLAGS
PAR ERR (1)	Lights to indicate that a parity error has occurred during a read function.
DATA MISS (1)	Lights to indicate that the processor took longer than 266 μs to answer a data request.
JOB DONE (1)	Lights to indicate that the specified function has been completed.
ILL OP (1)	Lights to indicate that an illegal operation has been specified by a command instruction. (Refer to Table 2-2 for command requirements.)
END ZONE (1)	Lights to indicate that the tape has entered either the forward or reverse end zones.

Table 2-5 (Cont)
TD10A Controls and Indicators

Control/Indicator	Function
	INDICATORS (Cont)
BLK MISS (1)	Lights to indicate that a block of data has been missed during a read or write operation.
INC BLK (1)	Lights to indicate that Function Stop is set or data is missed prior to the end of reading or writing a block.
ERR MTRK (1)	Lights to indicate that an error has been detected in the mark-track decoder.
DATA REQ (1)	During read function, lights to indicate that the control has a data word ready for the processor. During write function lights to indicate control requests data word from processor.
DATA NEED (1)	Lights to indicate that control is ready to use next data word.
RWB 0-5 (6)	Displays content of Read/Write Buffer.
	SWITCHES
MANUAL	Two-position toggle switch - UP position selects manual mode of operation for TU55 DECtape Transport. DOWN position selects program control.
MANUAL CLEAR	Momentary pushbutton switch - when depressed, it clears the command register and control flip-flops in TD10. Must be enabled by the MANUAL switch.
TAPE ROCKER	Two-position toggle switch - UP position forces the transport to alternately go forward and reverse between end zones. Must be enabled by the MANUAL switch.
WRTM	Two-position toggle switch - UP position used to preformat the timing and mark-track information on tape. DOWN position allows all other control functions.

2.5 PROGRAMMING SEQUENCES

Normal DECtape operation consists of reading block numbers until the target block is found, followed by reading or writing as many data words as required, followed by a waiting period for the job done flag to come on indicating that the parity word has been written out or read and checked. An interrupt program first issues a "CONO DTS, 0" to clear all interrupt enables. The next command that is issued is "CONO DTC,...", with the desired direction bit on, the select and deselect bits on, the unit number, function number 2 to read block numbers, and the two PI channel numbers. An interrupt

program now gives "CONO DTS, 660000" to enable all interrupts except job done and block missed. A non-interrupt program must continually check the four corresponding flag bits but an interrupt program just waits for an interrupt. When the transport comes up to speed and a block number is read, the data request flag is raised. The program must give a "DATAI DTC" to obtain the block number and compare it with the block number of the target block. If the numbers match, the program has 800 μs to give a "CONO DTC,..." to select a read or write data operation. If the block number read in is high, the program must give a "CONO DTC, 300200" which turns the tape around and reads the next block number going in the other direction. If the number is low, the program must again wait for the data request flag to read the next block number going in the same direction. After the first step, the tape may be moving in either direction. The example below shows a non-interrupt program to find a given block and to approach it with the tape moving forward.

If an error bit comes on, the program must stop the tape (CONO DTC, 400000) and take some corrective action. If the end zone bit comes on, the program merely gives a "CONO DTC, 300200" to turn the tape around.

Example: This routine finds a given block and assures the tape will be moving forward.

```
        CONO DTC,231200     ;GO FOW, UNIT 1, READ BLOCK NUM.
A:      CONSZ DTS,640000    ;ANY MISC. ERROR ON?
        JRST ERRS           ;YES, DO SOMETHING
        CONSZ DTS,20000     ;END ZONE?
B:      CONO DTC,300200     ;TURNAROUND
        CONSO DTS, 1        ;DATA AVAILABLE?
        JRST A              ;NO, RETEST ALL
        DATAI DTC, 2        ;READ IN BLOCK NUM.
        SUB 2, NUMBER       ;COMPUTE THIS # - DESIRED #
        CONSZ DTC,100000    ;GOING REV?
        TLCA 2,400000       ;YES, COMPLEMENT TURNAROUND
                            ;CONDITION AND SKIP THE = TEST
        JUMPE 2,FOUND       ;AT THE DESIRED BLOCK?
        JUMPGE 2, B         ;NO, TURNAROUND REQUIRED?
        JRST A              ;NO, GO SAME DIRECTION, READ B. NUM
```

After the program finds the target block, it issues a new "CONO DTC,..." to enter read or write data mode within 800 μs of the time when the block number appeared. An interrupt program also provides a new set of interrupt enables via the "CONO DTS,..." to enable all functions. Each time

the data request flag comes on, the program must give a "DATAI DTC," (or DATAO or BLKI or BLKO) instruction which clears the data request. The control continues to read or write across block boundaries until a "CONO DTS, 1" is given to cause a function stop. The control will continue through the current block when programmed to stop, turn on the job done flag and enter the idle state at the end of the block. When the control reaches the end of any block, it reads and checks (or writes out) the parity check word, possibly setting parity error flag. When the job done flag is raised, the function is complete and a new "CONO DTC" must be issued before any further data will pass. The transport, however, continues to move until a "CONO DTC, 400000" (stop) command is given.

Data request flags occur at 400-μs intervals (nominal), but the request must be serviced within 266 μs or else the data missed flag is set.

The four modes of write block number, read all, write all, and write mark and timing track are used mainly for the generation and maintenance of the prewritten block format. Write block number mode is used to write a single block number on the tape. The program must search for the block number preceding the block number to be rewritten. Only the block number for the direction in which the tape is moving is written. For example, when the tape is moving in reverse, the write block number command write a reverse block number.

The write mark and timing track command is enabled by manually setting the WRTM switch on the control panel. When this command is used the entire contents of the tape are lost. This mode is used to prepare an uncertified tape or to repair a tape. The transport used to generate the mark and timing tracks in this case must have a read/write head certified for zero skew. The timing track is automatically written on the output of a clock in the control. Mark-track data is taken from bits 0, 3, 6, 9,...,33. For each data word transferred, two mark track codes are written. Refer to Paragraph 2.2.1 for details of the mark track format. The mark and timing tracks for the entire tape are generated in a single pass, beginning after approximately 10 ft of reverse end zone codes and ending with as many forward end zone codes as can be recorded.

This function is used initially to preformat a tape by write timing and mark track information. Any data or previously written mark track information is destroyed. This function is also used to rewrite mark and/or timing track information which may have been destroyed.

The all mode permits writing or reading in all slots on the tape except the parity word slots which are written automatically. Reading or writing in the all mode begins with the first reverse-block-number slot encountered and continues until a Function Stop command is given. If the tape is reading or writing in a data block when the Function Stop is given, the action that is taken is the same as for read or write data modes; otherwise, the function will stop at the end of the current word. A CONO DTC, to enter write all mode followed by a DATAO DTC, followed by CONO DTS will write one reverse block number.

2.6 AVAILABLE SOFTWARE

The software programs available for use with the TD10 control are listed in the following paragraphs.

2.6.1 TD10A Control Unit Tests 1, 2 and 3 (MAINDEC-10-D3A0, D3BA, D3CA, D3DA)

These programs use the maintenance features incorporated in the TD10A to test the control logic without moving a TU55 DECtape Unit.

2.6.2 PDP-10/20 - PDP-10/50 Monitors

The monitor programs are included in the software documentation. Refer to manuals listed in Section 1 of this manual.

CHAPTER 3
THEORY OF OPERATION

This section contains detailed information on the logical operation of the TD10 DECtape Control and references the engineering drawings contained in Volume II, Peripheral Device Engineering Drawings. To facilitate the source locations of signals on the drawing, the mnemonic term applied to the signals, contain prefix codes which relate to a drawing. (See Table 3-1.)

Table 3-1
Signal/Drawing Identification

Signal Prefix	Title	Drawing
IOB	I/O Bus Interface Manual Mode #1, #2	TD10A-0-IOB1, IOB2
T	Timing 1, 2	TD10A-0-T1 (sheets 1 and 2), T2
ST	Status	TD10A-0-ST
DC	Data Control	TD10A-0-DC
ENB	Enable Flip-Flops	TD10A-0-ENB
RW	Read/Write Buffers	TD10A-0-RW
LP ERR	LP/ERR	TD10A-0-ERR
MK	Mark Track Decoder	TD10A-0-MK
COM	Command DECtape Control #1, #2	TD10A-0-COM 1, COM 2
RWA	Read/Write Amplifiers	TD10A-0-RWA
BA BB	Buffer Register	TD10A-0-B
SH	Shift Register	TD10A-0-SH
MAINT	Maintenance	TD10A-0-MNT

3.1 SYSTEM DESCRIPTION

The overall block diagram of the TD10 and PDP-10 system is shown on Figure 3-1. Data, control and status information are transferred between the processor and the buffer register of the control through the 36-bit I/O bus interface.

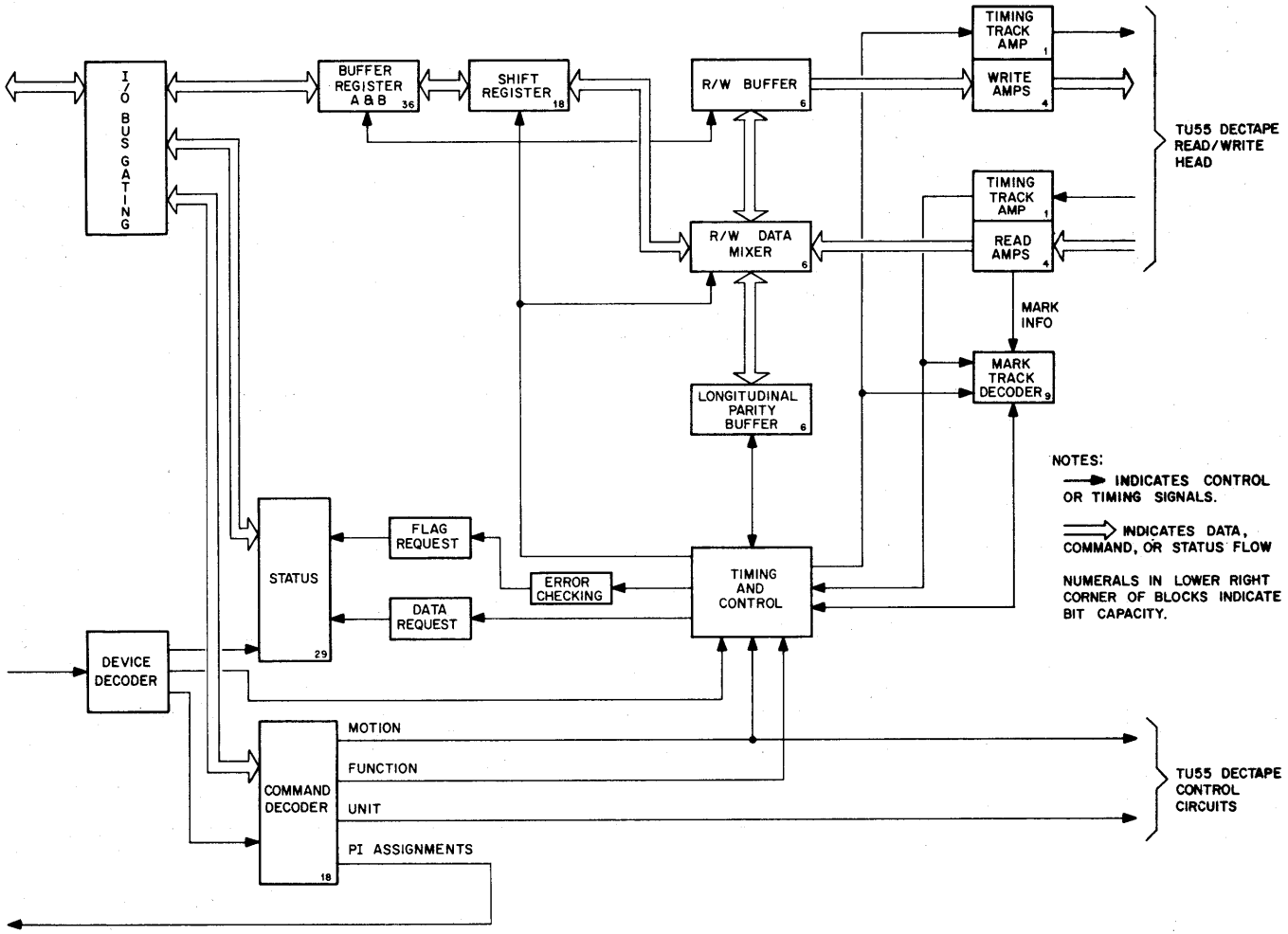


Figure 3-1 TD10A Control, System Block Diagram

All operations of the control are initiated by a CONO command from the processor accumulator which loads the command register with a micro programmed instruction to select a transport, specify a particular transport read/write operation, determine the transport motion and direction and, if required, selects both data and flag priority interrupt channels.

During write operations, a DATAO command from the processor sends a 36-bit data word through the I/O bus interface to the buffer register of the control. Under control of the timing register, the 36-bit word is transferred in 18-bit bytes to the shift register where the information is assembled in the proper order for transfer to the 6-bit read/write data mixer. The RW data mixer loads the RW buffer. The read/write buffer shifts 3 bits at a time to the read write amplifiers where one word of information is recorded on tape as 12 3-bit lines. At the end of each block of data, the longitudinal parity buffer writes the checksum bit.

During read operations, the data flow process is reversed. Information is read in 3-bit bytes from the data tracks on tape, loaded into the R/W buffer and transmitted as 6-bit bytes into the shift register under control of the decoded mark track information read from the mark track on tape. The shift register assembles the data and transfers it to the buffer register in two 18-bit load operations. A programmed DATAI instruction from the processor gates the 36-bit information from the buffer register into the processor memory through the I/O bus interface.

During all operations, the processor is capable of sending and receiving status information to and from the control to monitor or affect operations. In addition, information from the processor can simulate the mark and timing information normally read from tape to check the control operations.

The device selector logic decodes the device address information from the processor to specify a control or status function.

Brief descriptions of the registers in the TD10A are contained in the following paragraphs.

3.1.1 Command Decoder

The command decoder receives control information, data priority interrupt request assignments, and flag priority interrupt request assignments under program control (CONO DTC) from the processor. The bit assignments are described as follows.

a. Motion - A 2-bit register whose decoded output select motion (GO, STOP) and direction (FORWARD, REVERSE) for the TU55 DECtape Transport and control circuits.

b. Unit Select - A 4-bit register, 3 bits of which specify one of eight TU55 transports, 1-bit to indicate that a new transport has been selected.

c. Function - A 3-bit register whose decoded output selects one of seven control functions.

d. PI Assignments - A 6-bit register, 3 bits of which select one of seven lines for the data program interrupts, and 3 bits which select one of seven lines for the flag program interrupts.

3.1.2 Status Register

The status register is a 7-bit register which receives enable levels from the processor to allow error conditions to be affected within the control. In addition it allows the processor to monitor 28 different status and control conditions within the TD10A unit.

3.1.3 I/O Bus Interface

The I/O bus interface is a 36-bit gating network which receives and transmits status, data and control information between the processor and TD10A unit and also includes the device selector logic.

3.1.4 Buffer Register

The buffer register is a 36-bit register consisting of two 18-bit buffers (BA and BB) which stores a data word before transmission to or from the control. It transmits 18 bits at a time to the shift register and 36 bits at one time to the I/O bus interface.

3.1.5 Shift Register

The shift register is an 18-bit register which receives 18 bits at one time from BA of the buffer register, assembles the information into the required order, and transmits 6-bit bytes to the R/W data mixer during write operations. During read operations, the shift register operations is the reverse to that of the write.

3.1.6 R/W Data Mixer

The data mixer consists of six NOR gates, each of which is enabled by seven 2-input AND gates. The data mixer receives inputs from the shift register, read-write buffer, longitudinal parity buffer, and R/W amplifiers; and transmits the information to either the R/W buffer or shift register under enable signals produced by the TD10A control.

3.1.7 Read-Write Buffer (RWB)

The RWB is a 6-bit register which receives information from the R/W data mixer. The high-order 3-bit outputs feed the write amplifiers during write operations and, during read operations, the three read amplifier outputs feed into the low-order three bits of the read-write buffer through the R/W data mixer.

3.1.8 Longitudinal Parity Buffer (LP)

The longitudinal parity buffer is a 6-bit register in which the checksum is computed. During both reading and writing, the complement of each 6-bit byte that enters the read-write buffer is

exclusive ORed into the longitudinal parity buffer through the data mixer. At the end of a block during writing, the contents of the LP buffer are loaded into the read-write buffer through the data mixer and written on tape in the checksum area as two 3-bit lines. The checksum information read from tape is exclusive ORed into the computed checksum through the data mixer and the results are compared with (1), during read operations.

3.1.9 Mark Track Decoder

The mark track decoder is a 9-bit shift register into which the bits read from the mark track are serially shifted and decoded to generate levels to control the operation of the TD10. The mark track register is three bits longer than that required to decode a legal mark (6 bits) to insure that one legal mark follows another in the proper order.

3.1.10 Timing and Control

The timing and control logic produces timing pulses and control levels to synchronize the internal operation of the control and coordinate operations between the control and processor.

3.2 INPUT/OUTPUT BUS INTERFACE

The I/O bus interface with the TD10A control is shown on Dwg TD10A-0-IOB1 and TD10A-0-IOB2. The interface receives the device number or command signals and transfers data, status, and control signals to and from the processor and device. Figure 3-2 shows the information transferred and the direction of flow.

During a CONO command, two control pulses are issued from the processor. The first pulse (IOB CONO CLR) prepares the device to receive the control information and the second pulse (IOB CONO SET) commands the device to read the control information from the data lines into the device. Two command pulses are also used with the DATAO command. The first pulse (IOB DATAO CLR) prepares the device to receive data, and the second pulse (IOB DATAO SET) commands the device to read the information from the data lines. The IOB timing sequence is shown on Figure 3-3. During both the DATAI and CONOI commands, a single level is used (IOB DATAI or IOB CONI) to specify the time and length of time the device will transmit the requested infomation on the data lines.

The READ IN pulses are used in conjunction with the read-in mode available with the KA-10, processor. This read-in instruction is initiated from the control panel of the central processor and generates an IOB RDI PULSE to the device selected which initiates a specific read action in the TD10 control. When the control is ready to transmit data to the processor, an IOB RDI DATA level is sent to the processor to execute the instruction in the processor instruction register. The data read in from the control must be in a specified format outlined in the PDP-10 Systems Reference Manual listed in Table 1-1 of this manual.

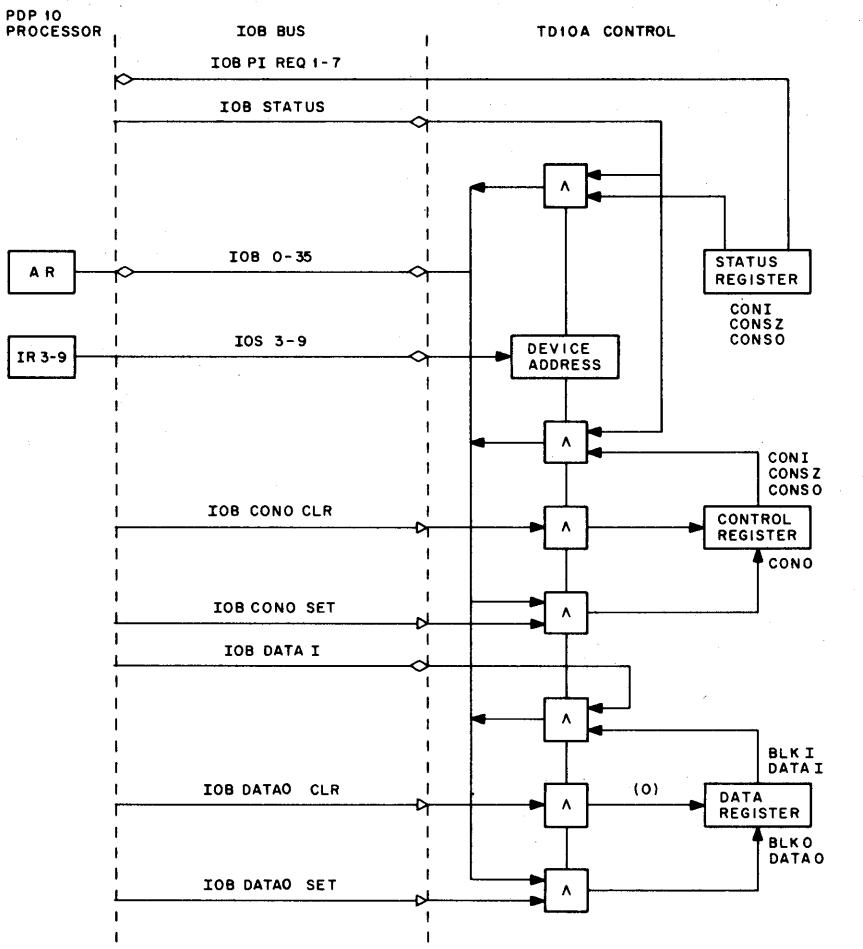


Figure 3-2 I/O Bus Information Flow Simplified Diagram

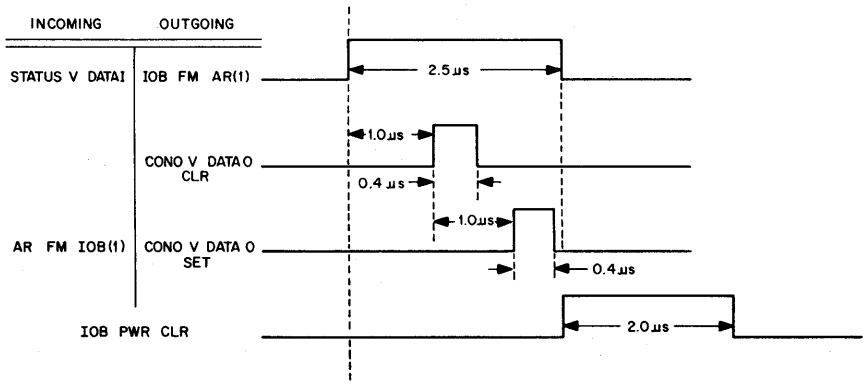


Figure 3-3 IOB Timing Sequence

The IOB RESET pulse, when issued from the processor, will stop motion and clear all devices. No priority interrupts can be issued from the control until a CONO command specifies a new PI channel.

3.2.1 Device Selector Logic (Dwg TD10A-0-IOB2)

The device selector logic is shown on I/O Bus Interface drawing IOB2. The device number, received from the PDP-10 instruction register, appears at connector H15 or J15 on seven pairs of complementary lines (IOS3-IOS9). When only one DECtape control is used in the data processing system, the device selector number assigned is 320. An alternate DECtape control is assigned number 330. Each control receives two separate numbers on the select lines. The control levels (320 or 330), are decoded by the first AND gate to generate the IOB SEL DTC level which provides synchronization for strobing control and data information between the processor and DECtape. Device numbers 324 or 334 are decoded by the remaining AND gate circuit to generate the IOB SEL DTS level which is used to synchronize the transfer of both status and control information between the processor and DECtape control. Both AND gate circuits are disabled when the MANUAL switch on the control panel is activated.

3.2.2 Command Control Signals DTC (Dwg TD10-0-IOB2)

The IOB SEL DTC level produced from the device selector is gated with various processor outputs to produce the DTC command signals as shown on Dwg TD10A-0-IOB2 and simplified diagram of Figure 3-4. When the IOB CONI level is received during a CONI instruction, the resulting IOB DTC STATUS A and B levels gate the motion, function unit, select and priority interrupt information to the IO BUS, as shown on Figure 3-5. The IOB DATAI level, produced during a data transfer, generates the IOB DTC DATAI levels A, B, and C which gate the data information from the buffer register A and B onto the I/O bus. Figure 3-6 shows the data information gated by the output levels. The ~ CROBAR level, shown on Dwg TD10A-0-IOB2 as an input to both of the previous gates referenced, is at ground when ac power to the TD10A is not present. When power is applied, the CROBAR contact remains closed for 4.0s and opens for the remaining time that ac power is applied producing a -3.0V. When ac power is removed by the switch on the Type 844 Power Control Panel or by the turn-on signal from the processor, the contact will close immediately. Power, however, will remain for 4.0s.

The IOB DATA CLR pulse gated with IOB SEL DTC produces the data clear pulse which clears the data buffer after the transfer of information to the processor or before data is transferred from the processor. The IOB CONO CLR pulse, received prior to loading command information into the control during a CONO instruction, produces the IOB DTC CONO CLR pulse which clears the command register and control flip-flops and prepares the unit to receive new command information by the IOB DTC CONO SET pulse. The IOB DTC CONO CLR pulse also clears the IOB RD IN flip-flop which may have been set by a previous read-instruction. The IOB PWR CLR pulse will also produce the IOB DTC CONO CLR pulse.

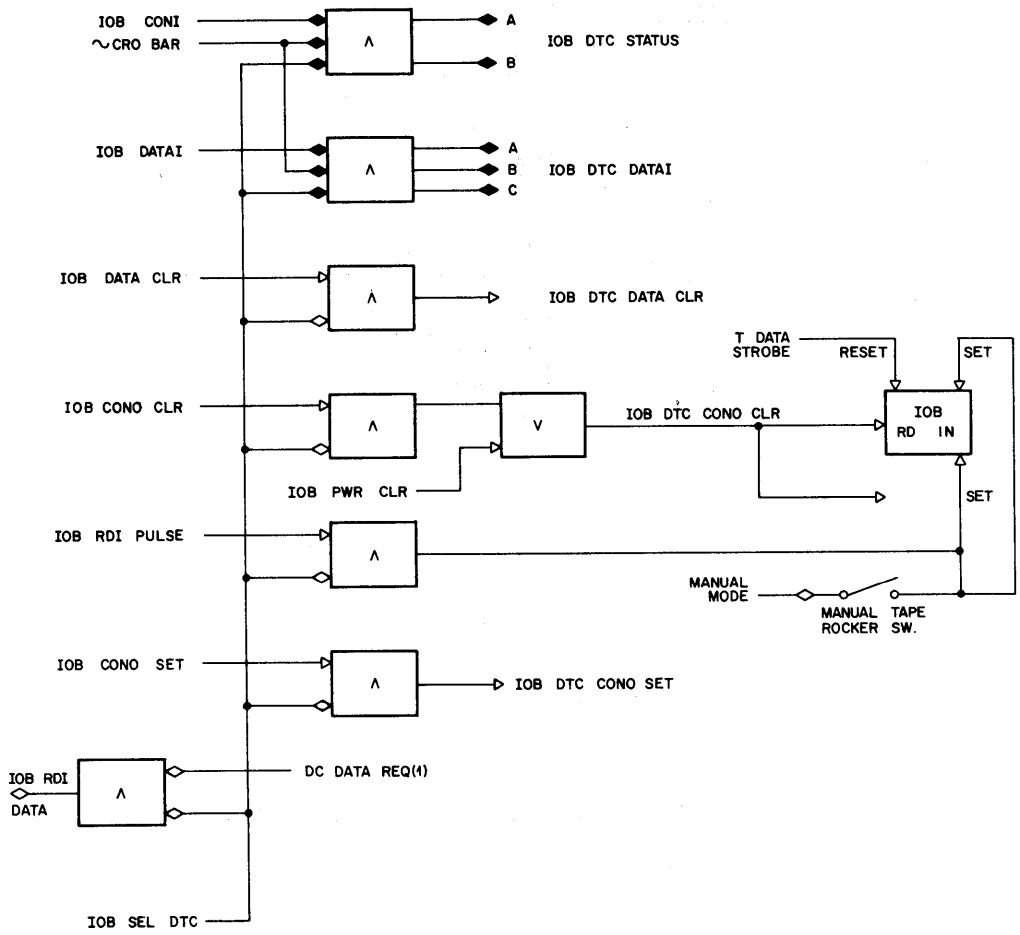


Figure 3-4 IOB DTC Signal Generation, Simplified Diagram

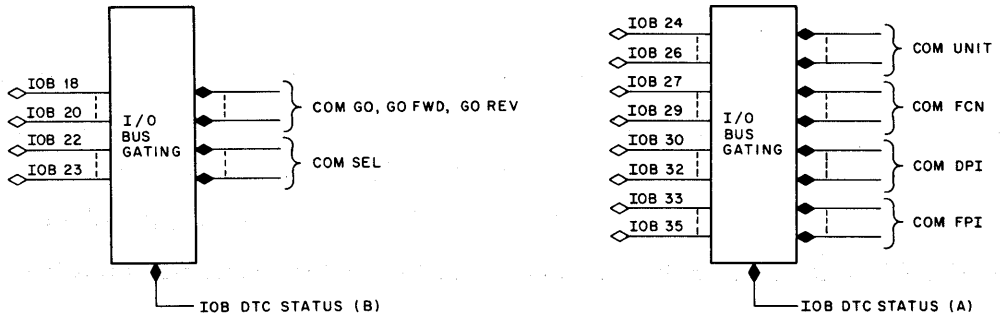


Figure 3-5 IOB DTC Status Gating, Simplified Diagram

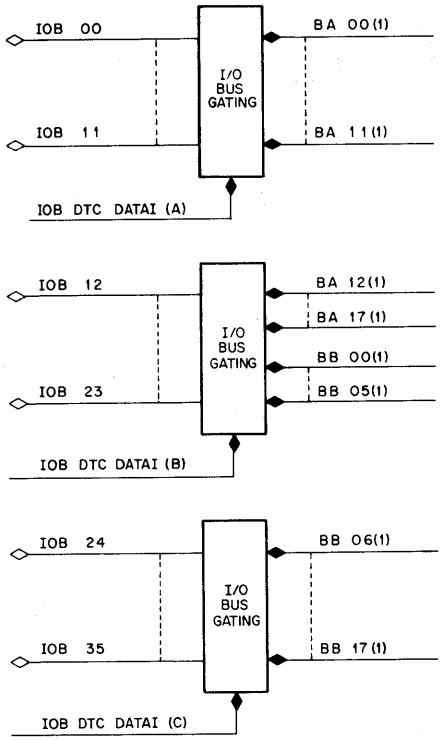


Figure 3-6 IOB DTC Data Gating, Simplified Diagram

The IOB SEL DTC level is also gated with the IOB RDI pulse during a read-in operation. The output sets the IOB RD IN flip-flop to initiate the read-in operation. When data is present in buffer register, an IOB RDI DATA level is sent to the processor to initiate data transfer operation.

3.2.3 Command Status Signals DTS (TD10A-0-IOB2)

The decoded IOB SELECT DTS level is gated with IOB CONI level from the processor to produce IOB DTS STATUS A, B, and C levels, shown on Figure 3-7. These output levels are used to gate 26 status and error condition bits from the control onto the I/O Bus for evaluation by the processor. During a CONO command the IOB DTS CONO CLR pulse clears the enable flip-flops in the control and allows the IOB DTS CONO SET pulse, which follows, to load the enable status bits into the control.

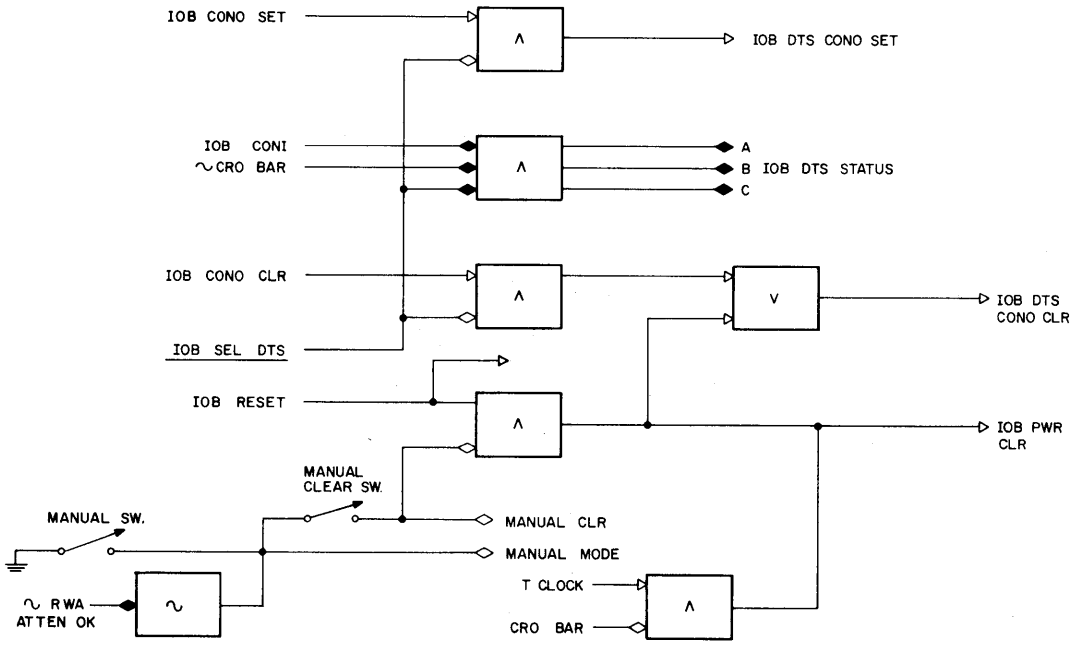


Figure 3-7 IOB DTS Signal Generation and Power Clear Simplified Diagram

3.2.4 Power Clear Pulse (Dwg TD10A-0-IOB2)

The IOB PWR CLR pulse, shown on Figure 3-7, is produced by the following conditions.

a. By depressing the MANUAL CLEAR pushbutton on the TD10A control panel when either the manual mode has been selected by the MANUAL switch or the jumper plug or attenuator plug to the read/write amplifiers (RWA) has been removed.

b. By an IOB RESET pulse being generated where power is initially applied to the processor, the RESET or READ-IN pushbutton on the processor is pressed or a CONO instruction is issued to the processor. The IOB RESET pulse clears the control registers, stops motion and clears any condition which may cause an interrupt.

c. When the CROBAR contact is closed, indicating that the 115 Vac turn-on voltage from the processor has been removed, and the timing clock of the control continues to run.

3.3 COMMAND DECODING

The DECtape command is encoded in 18 bits of information and received during the DTC CONO instruction from the processor. The control operations initiated by this information are shown on Dwg TD10A-0-COM1 and TD10A-0-COM2.

3.3.1 Motion Control (Dwg COM1)

The motion control flip-flops, COM GO and COM REV decoded IOB 18 (B) - 20 (B) to select motion and tape direction. The IOB DTC CONO SET pulse gates the 3 bit configuration into the motion flip-flops, such that IOB 19 (B) on a 1 sets the COM GO flip-flop and clears the COM REV flip-flop, and IOB 20 (B) on a 1 will set both the COM GO and the COM REV flip-flops. If both IOB 19 (B) and IOB 20 (B) are 1, the transport will remain in motion but reverse tape direction. With IOB 18 (B) on a 1, the COM GO flip-flop will be reset and stop transport motion. The COM GO flip-flop is also reset by ST END ZONE (1) when a read-in instruction is not being performed. The IOB BEG RD IN pulse, is generated when the IOB RD IN flip-flop (Dwg TD10A-0-IOB2) is set. When tape motion is in the forward direction, COM REV (0), and the end zone on tape is reached ST END ZONE (1) during the tape rocker operation, the IOB BEG RD IN pulse shown on Dwg TD10A-0-IOB2 will also be enabled. This pulse sets the COM GO flip-flop and the COM REV flip-flop, causing the tapes to move in the reverse direction after the end zone is reached. The IOB FIN RD IN pulse also produced on Dwg TD10A-0-IOB2 will reset the COM REV flip-flop when the reverse end zone is reached, again changing tape direction. The IOB PWR CLR pulse resets both motion flip-flops causing tape motion to stop. The decoded outputs from the COM GO flip-flop produce the STOP, GO levels which control the TU55 tape transport operations and the outputs of the COM REV flip-flops are used to condition the set and clear inputs of the COM REV DLYD flip-flop. The COM READY level gated with the TURNARND DLY (0) level will set or clear the flip-flop, and the outputs are gated with COM GO (1) to produce FWD or REV levels for the TU55 Transport and the COM GO FWD and COM GO REV levels for use by the control. The TURNARND DLY level is a 200 ms delay generated on drawing TD10A-0-T1 (sheet 2) whenever a change in tape motion is indicated. This delay insures that the block number being searched for after turnaround will not be passed before the tape has reached "up to speed." The COM GO FWD and COM GO REV levels together with the COM GO (0) level are transferred to the processor for monitoring during a CONI command. The select bit IOB 22 (B), used to indicate that a new unit has been selected, is gated in on the IOB DTC CONO SET pulse shown at the center of Dwg TD10A-0-COM 1. When IOB 22 (B) is a 1, COM SEL SET pulse is produced which sets the COM SEL flip-flop on the trailing edge, permitting the number in the unit number register to select the desired transport. The IOB BEG RD IN pulse will also set the COM SEL flip-flop during a read-in instruction and IOB PWR CLR pulse will reset it. With IOB 23 (B) on a 1, indicating that the control must disconnect from the transport that it previously controlled or that the select bit is set, the COM SEL flip-flop is reset by IOB CONO CLR. During a CONI command, the status of the COM SEL flip-flop is sent to the processor by the IOB DTC STATUS (B) level.

The IOB DTC CONO SET pulse also initiates a 1-μs delay pulse, COM READY, which prevents action, within the control, until the new command has been received.

3.3.2 Function Select (Dwg COM 1 and COM 2)

The function bits IOB27 (B) - 29 (B) are loaded into the function flip-flops COM FCN 0-2 (Dwg TD10A-0-COM 2) by the IOB DTC CONO SET pulse. The state of the flip-flops are monitored by the IOB DTC STATUS (A) level, during a CONI command, and decoded by the gating network at the bottom of Dwg TD10A-0-COM 1. Table 3-2 lists the function outputs resulting from the various states of the function flip-flops.

Table 3-2
Decoded Functions

	COM FCN 0	1	2	
NONE	0	0	0	COM RD
READ ALL	0	0	1	COM RD + COM ALL
READ BLOCK NO	0	1	0	COM RD + COM BN
READ DATA	0	1	1	COM RD + COM DATA
WRITE TIMING & MK	1	0	0	COM WR + COM WR MT
WRITE ALL	1	0	1	COM WR + COM ALL
WRITE BLOCK NO	1	1	0	COM WR + COM BN
WRITE DATA	1	1	1	COM WR + COM DATA

All read operations and no operation require a COM FCN 0 (0) and all write operations require a COM FCN 0 (1). Initially, during a CONO command the function flip-flops are cleared by the IOB DTC CONO CLR pulse to allow the IOB DTC CONO SET pulse to load in the function information. During the read-in operation when the tape has moved into the end zone in the reverse direction, both the COM FCN 1 and COM FCN 2 flip-flops are collector set to select a read data operation and automatically start reading data in the forward direction.

3.3.3 Unit Select (Dwg TD10A-0-COM 2)

The unit select flip-flops COM UNIT 0-2 are loaded by the IOB DTC CONO SET pulse and the set outputs are monitored by an IOB DTC STATUS level. On the trailing edge of the IOB DTC CONO CLR pulse, if IOB 23 (B) is on a 1, the COM UNIT flip-flops are reset indicating a new unit will be selected. IOB 23 (B) clears the COM SEL flip-flop immediately. Clearing COM UNIT 0-2 is delayed to prevent selecting unit 8 momentarily. The IOB PWR CLR pulse clears the flip-flops automatically and selects unit 8. The unit select decoding is shown on the upper left of the drawing and the

octal configuration of the unit is the decimal number of the unit selected except for unit 8 which is 0_8. For a unit select line to be enabled, the COM SEL input, set by IOB 22 (B), must be a 1.

3.3.4 Data and Flag Priority Interrupts (Dwg TD10A-0-COM 2)

The priority of the data and flag program interrupt requests are assigned by the information loaded into the COM DPI 0-2 and COM FPI 0-2 respectively, during the CONO command. The output information for data interrupts is decoded at the top center of the drawing. When the control is ready to send data or receive data from the processor the DC DATA REQ (1) level generates a ground COM DATA PI REQ level provided that ENB FCN STOP flip-flop contains 0. The ENB FCN STOP will be a 1 when IOB 35 (B) is programmed as a 1 during a CONO DTS instruction. The COM PI REQ ENB flip-flop, when set by the COM DATA PI REQ level, allows a ground level on one of the IOB PI REQ buses to the processor. The IOB DTC DATAI (A) or ENB FCN STOP (1) will hold the IOB PI REQ ENB flip-flop in the reset state, preventing a PI level from being generated. In addition, IOB DTC CONO CLR and IOB DTC DATA CLR will reset PI enable flip-flop and terminate the priority interrupt.

The flag priority interrupts are assigned by the program information on lines IOB 33 (B) - 35 (B) to the COM FPI 0-2 flip-flops. The status of the flip-flops are read onto the I/O Bus by the IOB DTC STATUS level. The outputs of COM FPI flip-flops are decoded at the top right of the drawing. The COM FLAG REQ level to the decoder is provided by a group of enable and error levels, drawing COM 1. When any two associated AND inputs are present, the flag interrupt assignment will be transferred to the processor on a CONI DTC command. The output lines from the COM FPI decoder (1-7) are wired to the W851 connector in common with the outputs of the COM DPI decoder.

3.4 CONTROL TIMING

The sequence of control operations are determined from the timing and mark track information read from tape during all functions except write timing and mark track (WRTM). The basic timing includes certain delays which allow the tape motion to reach an operating speed before a read or write function can be initiated and then provides pulses and levels which synchronize the specified function.

3.4.1 Initial Time Delays (Dwg TD10A-0-T1)

When a CONO command is received by the control which initially selects a unit, function, and motion, changes a tape motion or indicates both a new unit and motion, the required delays are produced, as shown on Dwg TD10A-0-T1. The unit and motion information are inputs to the T-SPEED delay (center right of sheet 2). A COM GO FWD or COM GO REV level is gated with ~ IOB 21 (B) CP ON level. The ~ IOB 21 (B) CP ON level, shown on the lower-center of Dwg TD10A-0-IOB2, is inhibited by either activating the MANUAL MODE switch on the control panel or by specifying a (1)

in bit 21 of the CONO DTC command which disables the delay. The T-SPEED delay generates a 120 ms delay T-WAIT pulse, which inhibits both reading and writing for the duration of the delay. If a new unit is specified but the T-SPEED delay is inhibited by a -3.0V IOB 21 (B) CP ON level, the T RELAY provides a ~ T-WAIT level for 1.0 ms. This delay allows adequate time for the relay in the TU55 DECtape Transport, which connects the read/write heads to the control, to make positive contact. The IOB PWR CLR pulse also initiates both a 120 ms and 1.0 ms delay so that the MANUAL CLEAR pushbutton activates the delays during adjustments. The same positive-going output which produces the T-SPEED delay generates the T-MCL (Master Clear) pulse. The T-MCL pulse is also produced by TP0 timing pulse when the tape end zone is reached (MK END ZONE) and is used to clear various registers and flip-flops when a new operation is specified.

The turn around delay, activated by the COM REV outputs and COM GO (1) level generate a 200 ms T WAIT delay so that reading of the mark track is inhibited when the tape is starting up or slowing down.

The ground T-WAIT output level clears the TUPSI flip-flop conditioning it to receive the RWA TP pulses produced as the timing track information is read from tape. Figure 3-8 shows the relationship of the RWA TP pulses as produced by the timing track read head.

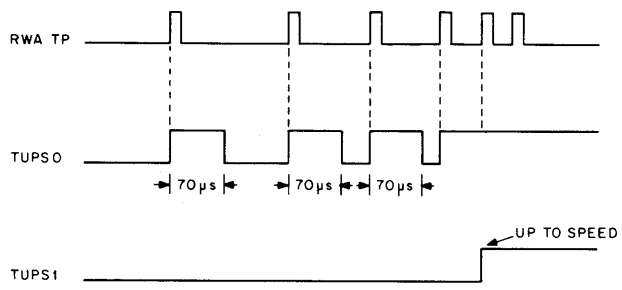


Figure 3-8 RWA TP Pulse Generation

The AC voltage from the timing track is present at pins AF and AH of WO32 (Dwg TD10A-0-RWA). When the transport is moving at normal speed, the read/write head output is sinusoidal and of constant amplitude. When the transport stops or starts or changes direction, the sine wave amplitude and frequency vary as a function of speed. The head outputs are fed to module G853 which couples the voltage to the W532 difference amplifier. The amplified signal is then applied to the W533 Slicer. The slicer determines the voltage level at which the RWA TP pulses will trigger. Initially, as tape motion starts, the amplitude of the output is not sufficient to generate a RWA TP output. As the tape speed increases the positive transition from zero will overcome the slicer level and result in the RWA TP

pulses. The RWA TP pulses trigger the TUPS0 delay (Dwg TD10A-0-T1) which is set for 66 ms. The TUPS0 delay conditions TUPS1 flip-flop for 66 ms. When an RWA TP pulse is generated at a time interval less than the delay, it sets the TUPS1 flip-flop, indicating that the tape motion is up to speed. RWA TP signals occurring at greater than 66 mA intervals will allow the TUPS0 delay to time out removing the conditioning level from the input gate of TUPS1.

3.4.2 Time Pulse Generation

The basic timing pulses which synchronize all operations of the control are generated by the timing track output, read from tape. The timing track contains alternately polarized bits which are preformatted on tape prior to the recording of information. The timing track read-write head output is received at AF and AH of connector W032 (Dwg TD10A-0-RWA) and fed to pins E and D of the G882 module as an alternating voltage. The resulting output (RWA TM) of the amplifier is a complementing square wave which is -3.0V or ground. This output is applied to the timing pulse generation circuit shown at the center of Dwg TD10A-0-T1 (sheet 1).

The RWA TM (0) input is gated with the conditioning level produced when the tape motion is up to speed TUPS1 (1) and the write turning mark switch on the control panel is not activated (~ ST WRTM). On the positive transition of the RWA TM (0) level a ground TP0 and TP0 (B) pulses are produced and on the positive transition of the RWA TM (1) level, the TP1 and TP1 (B) pulses are produced. At normal tape speed, the interval between the TP1 and TP0 pulses is 16.6 μs. The TP1 pulse is used as the read strobe pulse and as the write complement pulse. The TP0 pulse is used to load the read/write buffer during writing. The same levels which produce the TP1 pulse also produce the TP1 (SP) output which is used in the Mark Track Decoder. The TP1 and TP0 pulse outputs trigger an 8 μs TP DLY delay, shown at the center of Dwg TD10A-0-T1. This delay disables the conditioning level from the gate which receives the RWA TM (0) and RWA TM (1) levels to prevent extraneous signals read from the timing track, due to the cross talk from the write current in the data channels, from generating superfluous TP1 or TP0 pulses.

During the Write Timing and Mark Track function, the TP0 and TP1 but not TP1 (SP) pulses are generated by the inputs received from the 120 kc clock and TCK counter, shown at the top of sheet 2.

During maintenance, the DATAO DTS instructions also generate TP0 and TP1 pulses but not TP1 (SP) pulses.

3.4.3 Mark Track Decoding (Dwg TD10A-0-MK)

The mark track code defines the areas on tape where control and data words will be positioned. The mark track information consists of six serial bits per code read by amplifier A05,

Dwg TD10A-0-RWA during both reading and writing data functions. The complementary amplifier output signals RWA MK TK (0) and RWA MK TK (1) are applied as level inputs to the MK8 flip-flop in the mark track register (MK0-MK8), Dwg TD10A-0-MK. When the tape transport is "up to speed" the positive transition of the TP1 (SP) pulse gates the mark track information into MK8. The mark track information is serially shifted through register by the TP1 pulse. The MK0 flip-flop, once set by a 1-bit in the mark track, will remain set until cleared by the TMCL pulse which clears the register when a change on tape motion is specified or when the tape end zone is reached. The mark track register outputs are monitored by eight gating networks which decode specific register configurations to generate specific level outputs for 33.3 μs.

As the tape moves through the reverse end zone in the forward direction, the octal 55 bit configuration is shifted through the register, but not decoded. The first legal code appears in the area assigned to the reverse block number and forward block number and is decoded eight times at every other TP1 pulse, as shown on Figure 3-9. Two space marks (25_8) are required before the forward block number. Two bit positions after the last MK BN SPACE level occurs, the MK BN END level is produced, as shown on Figure 3-9. This level indicates the end of the forward block number area on tape.

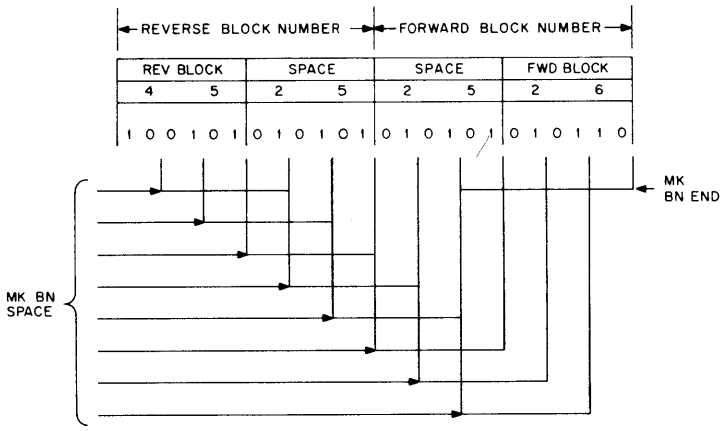


Figure 3-9 Block Number Decoding (Between Blocks)

The block number space levels are used to synchronize the reading and writing of the block number information on tape. This is accomplished by setting the TBN counter, shown on Dwg TD10A-0-T1. The first block number encountered, after leaving the end zone in the forward direction, is not accessible since a decoded 51_8 (MK BN SYNC) level is initially required to start the TBN counter.

The next level produced (MK DATA SYNC) is a result of the decoded reverse mark 32_8, as shown on Figure 3-10.

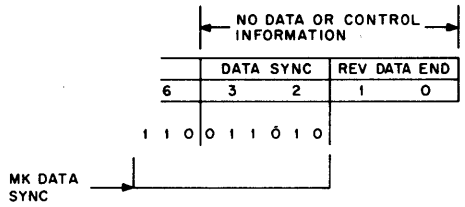


Figure 3-10 Data Sync Mark Decoding

Following the data sync mark (32_8), four MK REV DATA END levels are enabled by the decoding of the 10_8, shown on Figure 3-11. This level indicates the start of the data information, beginning with the reverse checksum information, and locates the first data word area on tape.

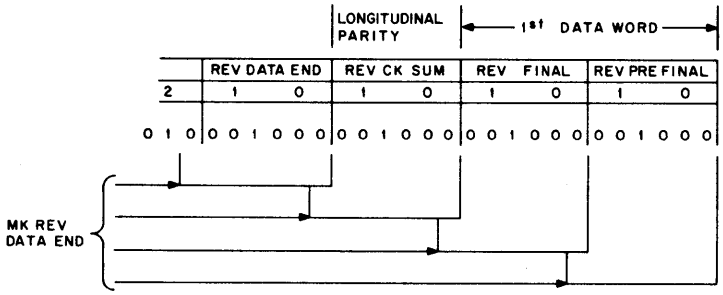


Figure 3-11 Data End Mark Decoding

All data word areas are coded by the data mark (70_8) except for the first and last word. The data mark is decoded to produce the MK DATA level every 6 mark track bits, as shown on Figure 3-12.

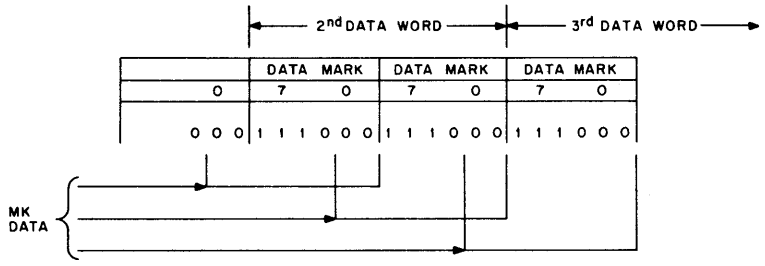


Figure 3-12 Data Mark Decoding

The last data word is identified by the prefinal mark (73_8) which results in the first of four MK FWD DATA END levels, as shown on Figure 3-13. The decoding network receives a comparison input consisting of MK1 $\not\vee$ MK2 produced by the gating circuits shown on the bottom of Dwg TD10A-0-

MK. These bits are compared to insure that MK FWD DATA END levels will not be enabled unless the MK1 and MK2 bits are alike, both must be either (0) or (1). This occurs when (73_8) follows either a (70_8) or another (73_8).

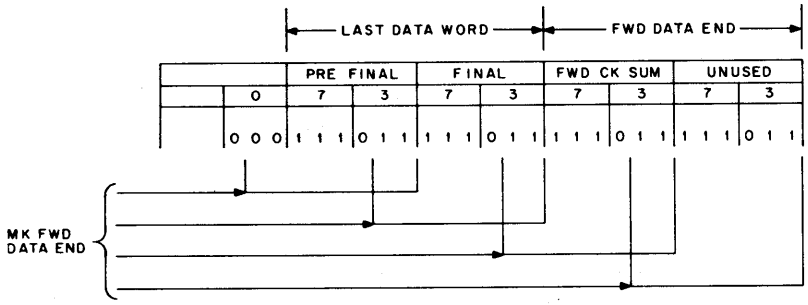


Figure 3-13 Forward Data End Decoding

The last mark to be decoded in a standard block is the block number sync (51_8) (Figure 3-14), which enables the MK BN SYNC level. This level conditions the control to receive a legal block number to identify the block of data which follows.

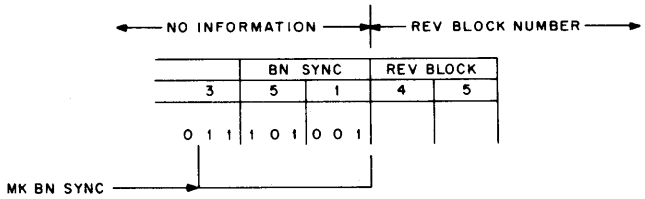


Figure 3-14 Block Number Sync Decoding

The gating circuit at the center left of the drawing produces a MK PRES level output when any of the input levels are present. The MK PRES pulse, therefore, occurs for 33.3 μs at every 6-bit mark track decoding, starting at the end of the forward block number and continuing until the start of the reverse block number of the next block. The MK8 flip-flop has two additional inputs from ~IOB 35 (B) and IOB 35 (B). These inputs are used during a maintenance program to simulate reading mark track information without tape. The MK DATA END level, shown on the bottom of the drawing, is produced eight times during a block, once for each (10_8) and once for each (73_8).

3.5 BASIC READ-WRITE LOGIC

The basic read-write logic used during all functions of the TD10 DECtape is shown on Figure 3-15. Each of the three data channels on tape has an associated read amplifier which provides

an RWA output to the data mixer and the write amplifier which is driven by the complementary input from RWB 0-2. Read amplifier inputs are paralleled with write amplifier outputs across the head, allowing the read amplifier to respond to both the head and write amplifier signals. When input E is more positive than D, the output U is -3.0V and V is at ground. When the inputs reverse, the V output is -3.0V and U is ground. If zero input voltage occurs, the read amplifier oscillates until a voltage is detected.

The write amplifier, enabled by the T WREN level, supplies write current to the head. Only one head is shown on Figure 3-15. Two heads, however, wired in series, produce the two tracks corresponding to each channel on tape. When the RWB flip-flop is set, pin J is negative and pin K floats, allowing current to flow from the head ground termination, through the left coil to induce a polarization on tape from left to right. When the RWB flip-flop is reset, output pin K becomes more negative inducing a right to left polarization on tape. Figure 3-16 shows the relationship of the signals generated during both the read and write sequence.

Two pulses are required to write each bit on tape. One pulse loads the information into the RWB and another pulse complements the flip-flop. Each time the RWB flip-flop changes state, the write amplifier produces a change in flux in the head; however, only changes which occur at TP1 time are recognized as valid data when reading. During a write forward or write reverse operation, the 6-bit information from the shift register is gated into the R/W data mixer by T WR FWD or T WR REV level. The output levels of the R/W data mixer are strobed into the RWB by the TP0 (load) pulse. The next TP1 pulse, which occurs, complements RWB 0-2 but does not affect RWB 3-5. It writes the first 3-bit line on tape. The three bits RWB 3-5 are then gated into the R/W data mixer by the T RWB SHLT level and shifted into RWB 0-2 at the next TP0 pulse. The T RWB COMP level is again produced and complements RWB 0-2 at time TP1, which writes the second 3-bit line on tape. The T WR FWD or T WR REV is again generated to cause six shift register bits to be loaded into the RWB. The operation continues until all the information is written. The R/W DATA (0) output is used to complement the 6-bit longitudinal parity buffer (LP). When the last data line of a block is recorded on tape, the LP 0-5 levels are gated into the R/W data mixer by the T WR LP level. At time TP1, the information in RWB 0-2 is complemented and writes the first 3-bit checksum on tape. The T RWB SH LT level loads RWB 0-2 with the RWB 3-5 at time TP0 and the T RWB COMP level at TP1 time complements RWB 0-3 to write the second three bits of the parity information on tape. The remaining four lines in the checksum area are recorded as all ones.

During a read operation, The T WREN input to the write amplifier is disabled. The first three bits of valid data read from tape RWA 0-3 are gated into the R/W data mixer, by the T RWB SH LT level at time TP0 which precedes the first data bit. The nonvalid information contained in RWA 3-5 is also gated by the same shift left pulse into RWB 0-2. At time TP1 which occurs at the peak of the change in polarization on tape, the R/W data output levels are strobed into the RWB. The T RWB SH LT level remains on the input to the R/W data mixer until the next three bits are detected by the read amplifier and the second TP1 pulse occurs. This pulse fills the RWB and the next TP0 pulse loads the contents of the R/W data mixer, R/W DATA 0-5 enabled by the T RD FWD level, into the shift register SH 12-17.

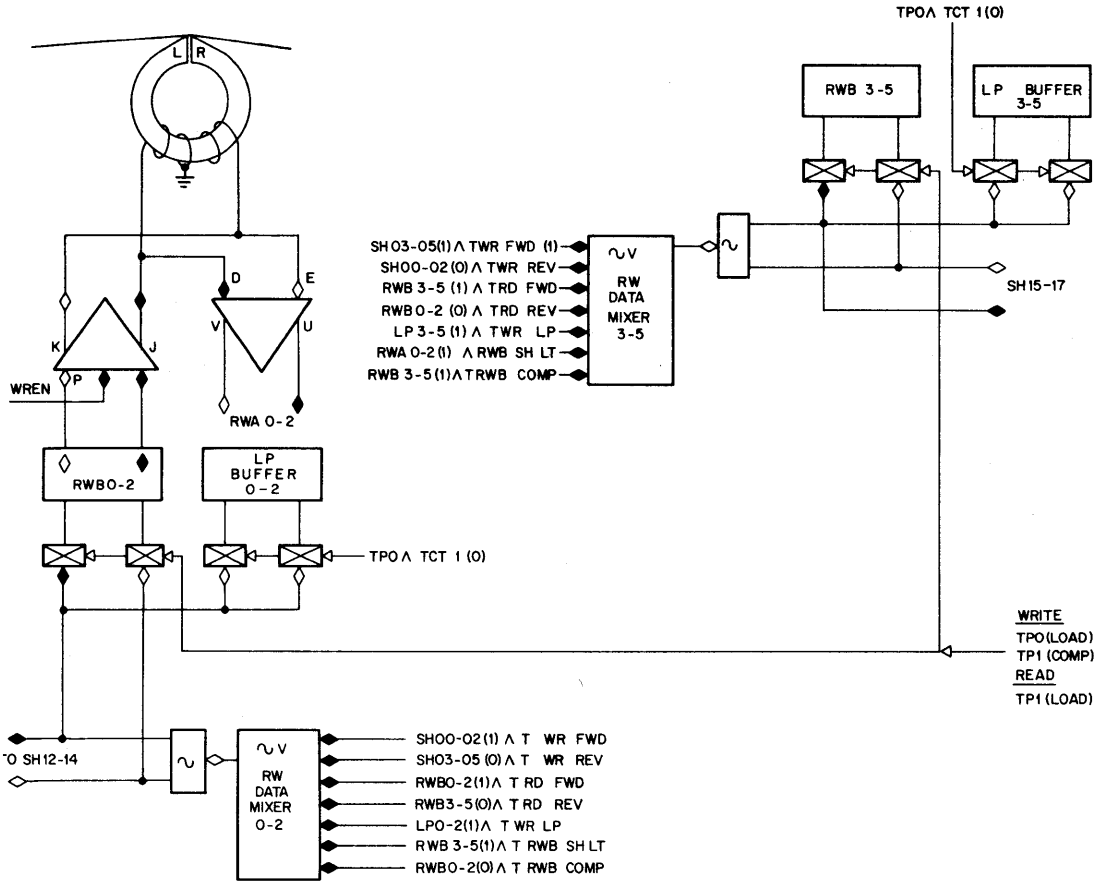


Figure 3-15 Read-Write Head Logic, Simplified Diagram

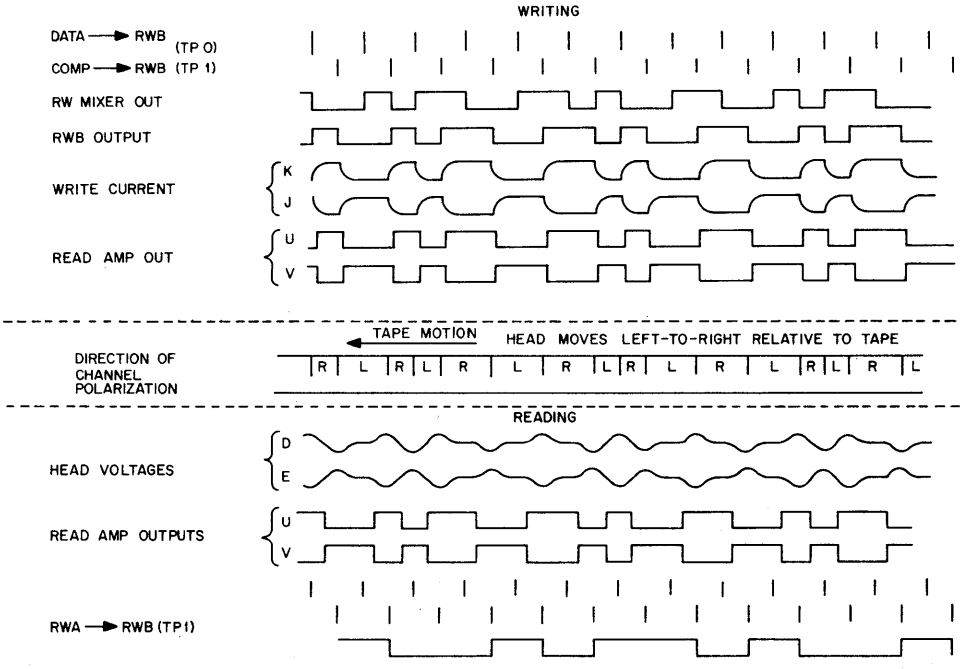


Figure 3-16 Read-Write Timing

During a read reverse operation, the two TP1s generated during the T RWB SH LT interval, load the complement adverse of RWB in the same configuration as read forward. The T RD REV level, however, gates the RW DATA 0-2 into SH 15-17 and RW DATA 3-5 into SH 12-14.

3.6 DATA TRANSMISSION CONTROL

The data control circuits provide delays and sequencing signals which are used to transfer the information to be read or written into the shift register and buffers in the control. Before information can be read or written on tape during a function, the T ACT flip-flop (Dwg TD10A-0-T2) must be enabled by one of four gates. These gates provide a T ACT conditioning level at the proper time during the reading and writing of block numbers, data, all, timing mark and mark track. The output of the T ACT flip-flop sets the T WREN flip-flop, during a write instruction to enable the write amplifiers. The IOB DTC CONO CLR pulse resets both flip-flops prior to the transfer of control information and the CROBAR level disables the T WREN flip-flop with the loss of ac power.

Both the T ACT and T WREN flip-flops are reset by the T INACT level at TP0 time, produced by a combination of level inputs occurring at specified times during a function.

The write enable, T WREN flip-flop, will be inhibited by the ERR SW level input if the WRTM switch on the control panel is not in the proper position, if the write lock function in the TU55 Transport is enabled or if a select error has occurred.

With the T ACT flip-flop enabled during a read or write data function and with the TCT1 level at (0), the TP0 pulse will produce a T DATA STROBE pulse, as shown at the center of Dwg TD10A-0-T1.

During a write all, write block number, or write timing and mark track operation a T DATA STROBE pulse is produced initially when T ACT makes a transition to (1). This is required to load the RWB with the first six bits of data mark in order that it may be written on tape. This does not occur during write data because the reverse checksum is written first from the computation of the LP buffer before the first six bits of data is written.

3.6.1 Timing Counter (Dwg TD10A-0-T1, Sheet 2) and Error Counter (Dwg TD10A-0-LP/ERR)

The TP0 (B), TP1 (B) pulses trigger the timing counter flip-flops TCT0 and TCT 1 as shown on Figure 3-17. The TCT 0 flip-flop is set by the positive-going pulse every 33.33 μs. The TCT 0 count occurs when ever the TP0, TP1 pulses are present. The TCT 1 flip-flop is complemented by the TP1 pulse, enabled by the T ACT level. The TCT 1 output levels are produced when a word is being read from or written on tape.

The error counter (ERR CT2 and ERR CT3) is used to control the operations within the data control during reading and writing of each word. The states of the ERR CT flip-flops, therefore, determine the action of the data control. The error counter flip-flops are cleared by the T CNTRS CL pulse when a change of transport motion is specified by a CONO instruction and by the MK DATA

SYNC and MK BN SYNC levels. With both ERR CT2 and ERR CT3 reset, the first TCT 1 (0) transition will set ERR CT2 and the second TCT 1 (0) transition will set ERR CT3, as indicated on Figure 3-17. The third TCT 1 (0) transition resets both ERR CT2 and ERR CT3 and the action is repeated again for the next three TCT 1 (0) transitions to produce the levels for one complete data word. If the T ACT flip-flop remains set, the Error counter will continue the sequence until T ACT is reset. Two complete cycles of the error counter occur during the reading or writing of each 36-bit word.

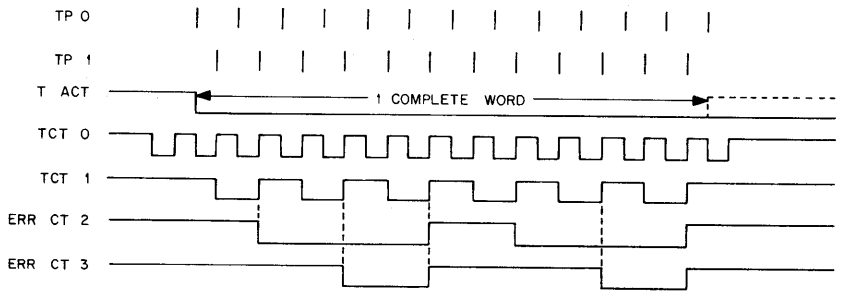


Figure 3-17 Timing and Error Counter, Timing Diagram

3.6.2 T DATA Counter

The Data Timing Counter (T DATA 0-2), shown on Dwg TD10A-0-T1 (sheet 2), is a 3-bit binary counter register which receives input from the mark track decoder to generate levels for reading and writing in the assigned areas on tape. Figure 3-18 shows the relationship of the levels generated to the information in the mark track.

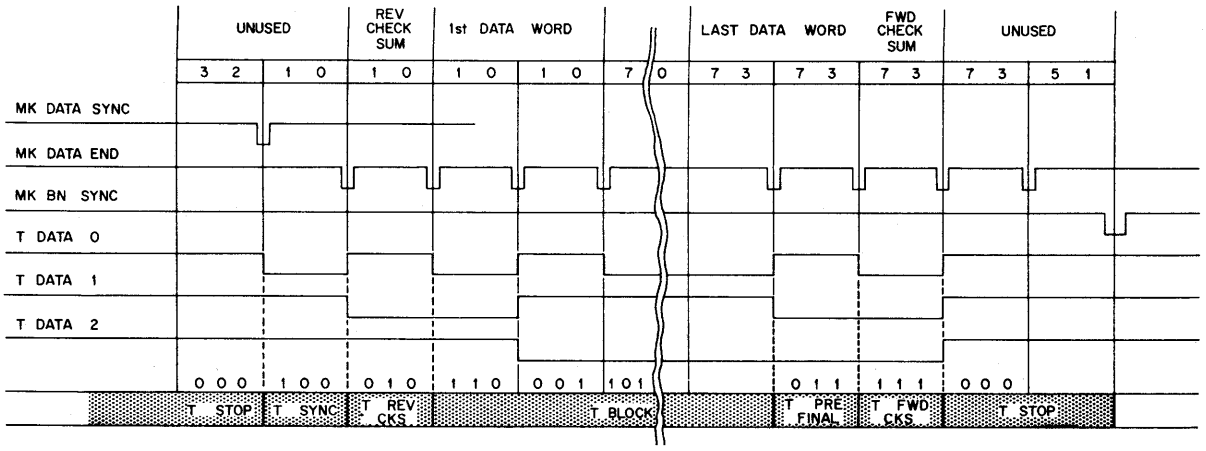


Figure 3-18 T DATA Counter Sequence

When a CONO instruction is initially received that indicates a change in tape motion, the TMCL pulse clears the T DATA 0 flip-flop and also generates the CNTRS CL pulse to clear the T DATA 1 and T DATA 2 flip-flops. The first MK DATA SYNC pulse (decoded 32) which appears, sets the T DATA 0 flip-flop at time TP0. Each succeeding MK DATA END pulse will complement the T DATA 0 flip-flop. The T DATA 1 flip-flop is set on the positive transition of the T DATA 0 output, and the T DATA 2 is set on the positive transition of the T DATA 1 flip-flop. The outputs of the counter are decoded by a DCDR module to produce the levels as shown on Figure 3-18. The last MK DATA END level (73_8) to be decoded will not complement the T DATA 0 flip-flop because of the ground ~ T STOP level to the conditioning gate of T DATA 0. The MK BN SYNC level (51_8) is the complement obverse of MK DATA SYNC so the T DATA counter will be started in either the forward or reverse direction.

3.6.3 Block Number Counter (Dwg TD10A-0-T1 (Sheet 1))

The block number counter, TBN0 through TBN2, is used to control the reading and writing of block numbers in the assigned areas on tape. The TBN counter is initially sequenced, as shown on Figure 3-19, by a decoded MK BN SYNC (51_8) level from the mark track decoder which allows the TP0 pulse to set the TBN0 flip-flop. The TBN0 flip-flop remains set until the first MK BN SPACE (25_8) level is decoded. The positive transition of TBN0 complements the TBN1 flip-flop to the set state. With TBN1 set, the next MK BN SPACE level which occurs will generate the TBN CT level and allow the TP0 pulse to again set TBN0. The TBN CT level will remain only while the MK BN SPACE level is asserted. The third MK BN SPACE level resets the TBN1 flip-flop whose output resets the TBN1 flip-flop. The positive transition of the TBN1 flip-flop sets the TBN2 flip-flop at the start of the forward block number area on tape, and it remains set until the TP0 pulse produced when the MK BN END (26_8) level is decoded, indicating the end of the forward block number area. The TBN1 (0) level inhibits the generation of the TBN CT level, preventing the TBN0 flip-flop from being set at TP0 time when the fourth MK BN SPACE level is decoded.

3.6.4 T INACT COND Level Generation (Dwg TD10A-0-T2)

Figure 3-20 shows the timing sequence that results in the generation of the T INACT COND levels. The T INACT COND levels are produced only when enabled by the COM FCN(1) input specified by a read/write data or block number function or by an ENB FCN STOP(1) level, indicating that bit 35 of a COND DTS instruction is set or that a data miss error has occurred. The T INACT COND level allows the TP0 pulse to reset the T ACT flip-flop to prevent information from being read or written. During write timing and mark track, the T INACT COND level allows the T ACT flip-flop to be continually reset by the TP0 pulse as soon as ENB FCN STOP is set to a 1. During the other functions, the T INACT COND is asserted only at the appropriate locations on tape such as the end of a data block or at the end of a block number.

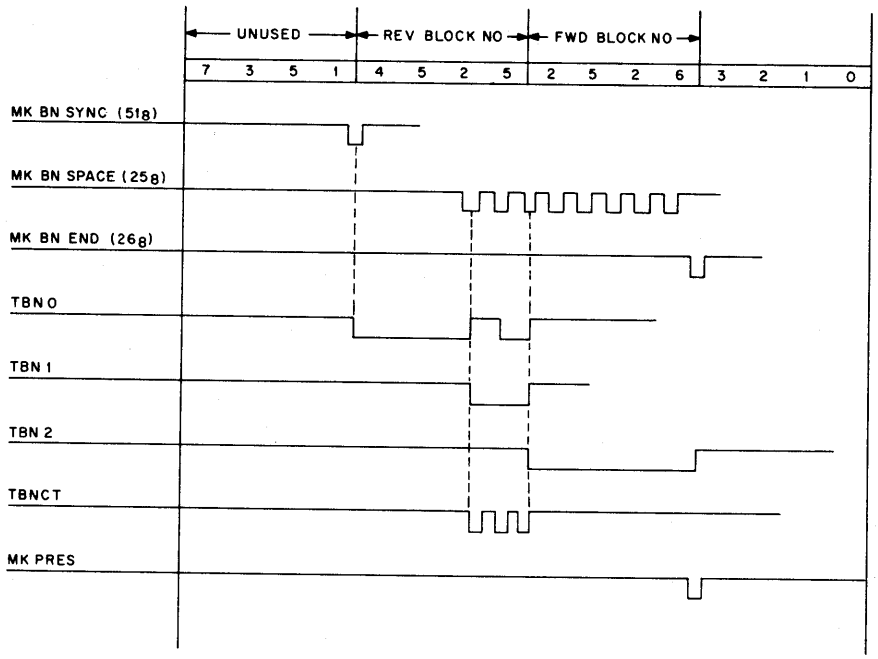


Figure 3-19 T BN Counter, Timing Sequence

3.6.5 T PAUSE Level Generation

The T PAUSE level, produced by the gating circuit shown on Dwg TD10A-0-T1 (Sheet 1), is used to inhibit the generation of T DATA STROBE pulses and T WR FWD levels at the reverse and forward checksum areas on tape. This prevents data from being written in the reverse checksum area during forward tape motion and allows the parity to be written in the forward checksum area. During reverse tape motion the T PAUSE level prevents the writing of data in forward checksum area and allows the parity to be written in the reverse checksum area. In addition, the T INACT COND level (Dwg TD10A-0-T2) will also produce a T PAUSE level to inhibit any additional writing of data when the function is about to terminate.

Figure 3-21 shows the signals and sequence of T PAUSE level generation. Inputs are provided from the T DATA counter, and from the mark track decoder.

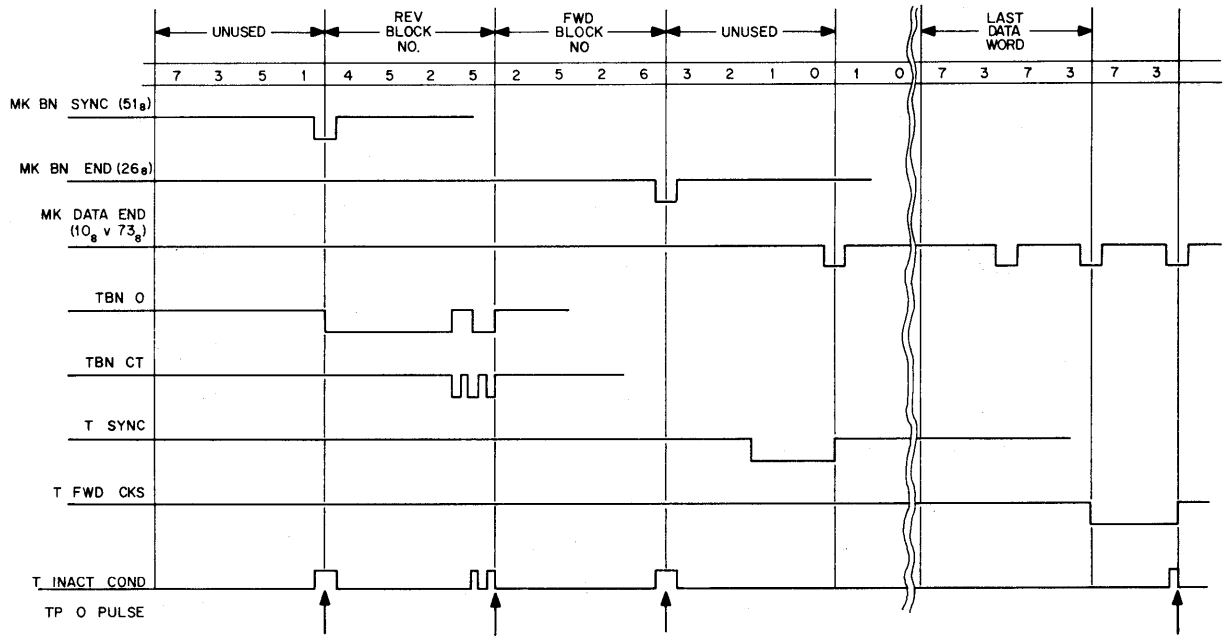


Figure 3-20 T INACT COND Level, Sequence Diagram

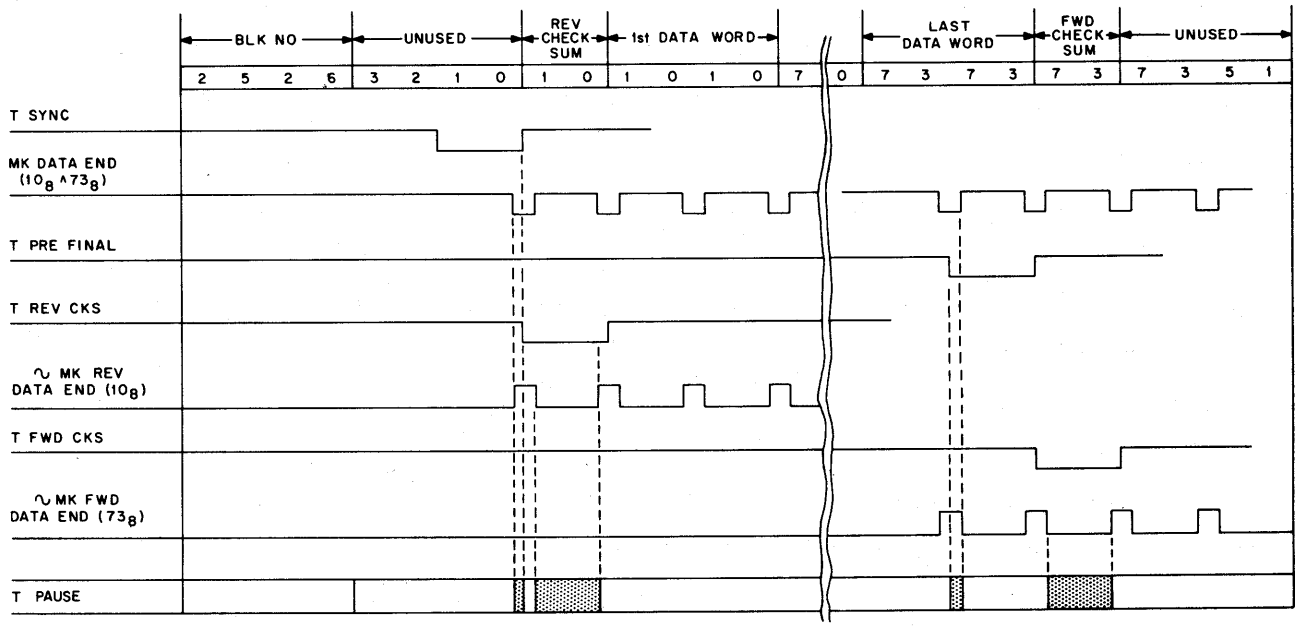


Figure 3-21 T PAUSE Level, Timing Sequence

3.6.6 Data Request

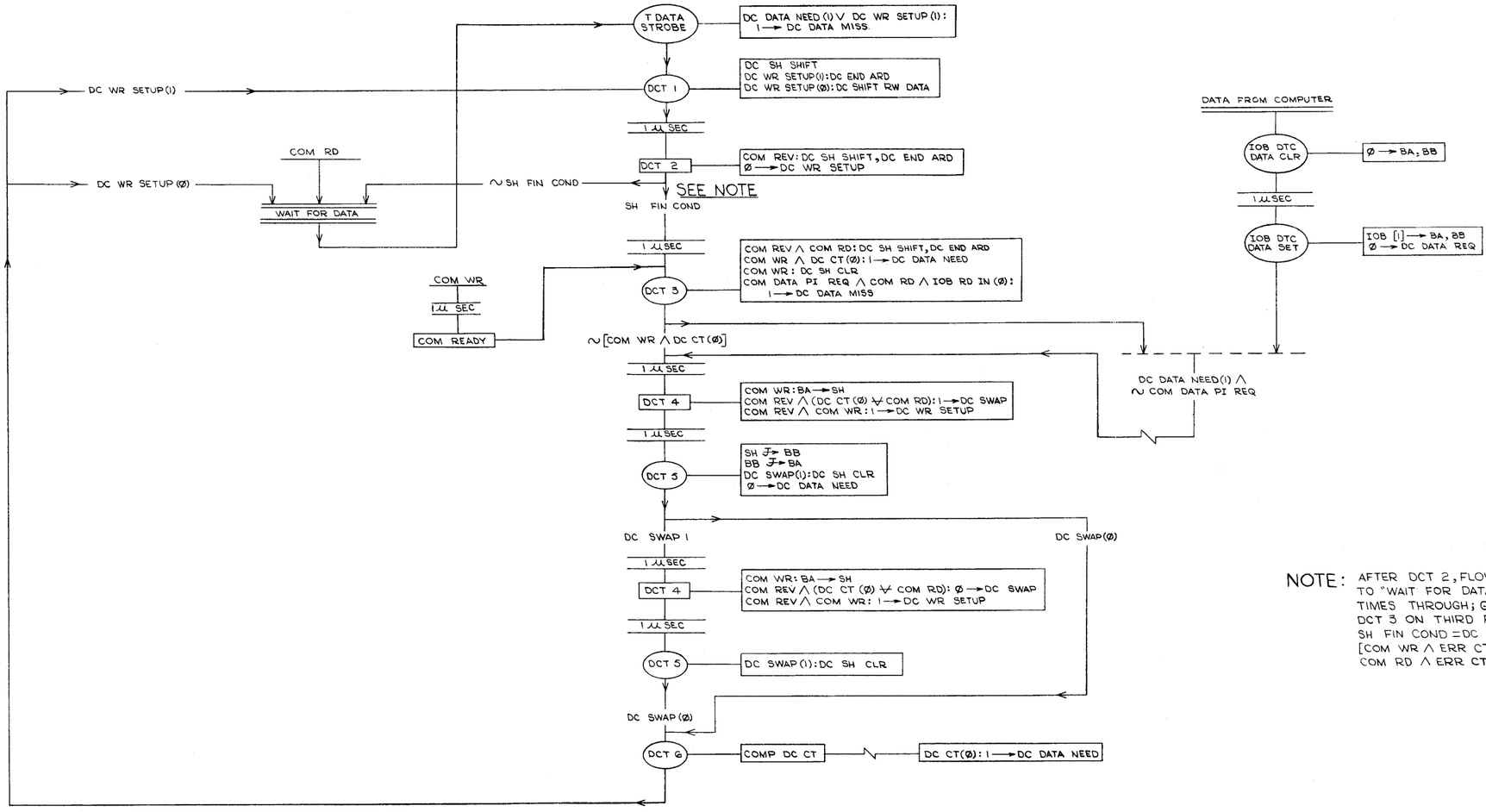
During a write command the DC DATA RQ flip-flop, bottom center of Dwg TD10A-0-DC, is initially set by the IOB DTC CONO SET pulse. The DC DATA RQ (1) output is used to allow the selected priority interrupt to be sent to the processor and it informs the processor under an IOB DTS STATUS level (Dwg TD10A-0-ST) that the control is requesting data. The DC DATA RQ flip-flop is reset during a write operation by IOB DTC DATA SET pulse which loads the data buffer. During a read command, the data request is not produced until the data buffer is loaded and ready to transfer to the processor. This occurs at time DCT 6, when the DC CT flip-flop is cleared. The IOB DTC DATAI (A) level, upon transferring the data from the buffer to the I/O bus, will clear the DC DATA RQ. The IOB DTC CONO CLR transition will also clear both DC CT and DC DATA RQ.

3.6.7 Data Control Operations (Dwg TD10A-0-DC)

The data control flow diagram is shown on Figure 3-22. All write operations of the data control are initiated by a CONO instruction from the processor which produces the first data control sequence. During read operations the data control sequence is initiated by the T DATA STROBE pulse.

The DC Sequence tables associated with each of the read write functions that follow, list the events and operations within the data control and indicate the location and content of the data within registers at the completion of each event. The register content is represented by a number which is the octal equivalent of the three bits of data read or written on tape. The low-order bits of the data word are indicated by the highest numbers, such that number 0 is equivalent to the first three high-order bits of the data word.

a. Read Forward. - Table 3-3 shows the read forward information sequence. The T DATA STROBE, top left of Dwg TD10A-0-DC produces the DCT 1 pulse which is amplified to generate the DC SH SHIFT pulse and gated with DC WR SET UP (0) level resulting in the DC SHIFT RW DATA signal at the top right of the drawing. The DC SH SHIFT pulse transfers the irrelevant information in SH12-17 to SH06-11, and SH06-11 into SH00-05, as shown on Dwg TD10A-0-SH. At the same time, the DC SHIFT RW DATA pulse loads the first six bits of the data information, gated from the R/W data mixer 0-5, into SH12-17. The DCT1 pulse triggers a 1.0 μs delay which generates the DCT2 pulse. The DCT2 pulse, initiated by the first and second T DATA STROBE, has no function and will not produce the DCT3 pulse because of the absence of a conditioning level to the second 1.0 μs delay. The second T DATA STROBE pulse produces the DCT1 pulse resulting in DC SH SHIFT which transfers the first six bits of data from SH12-17 to SH06-11 and the DC SHIFT RW DATA pulse to load the second six bits from R/W data mixer into SH12-17. The third T DATA STROBE pulse loads the shift register with the first half of the data word and allows the DCT3 pulse, enabled by ERR CT 2(0) and COM RD, to be generated, after the delay interval. The DCT3 pulse is gated with ~ DC WRITE ∧ CT (0), at the left center of the drawing, to generate the DCT4 pulse after a 1.0 μs delay interval. The ~ DC WRITE ∧ CT (0) level is produced by the gate at the right center of the drawing. The DCT4 pulse triggers a 1.0 μs delay resulting in pulses DCT5, 5A and 5B which shifts the irrelevant data internally within the buffer register and loads the shift register SH00-17 outputs into BB00-BB17. This completes the assembly of the first half of the data word into the buffer register. The DCT5 pulse, gated with DC SWAP (0), at the top right of the drawing, produces the DCT6 pulse which sets the DC CT flip-flop at the lower center of the drawing. This flip-flop remains set until the completion of the assembly of the second half of the data word.



NOTE: AFTER DCT 2, FLOW FOLLOWS TO "WAIT FOR DATA" FIRST TWO TIMES THROUGH; GOES TO DCT 3 ON THIRD PASS.
SH FIN COND = DC WR SETUP (Ø) ∧ [COM WR ∧ ERR CT 3 (1) ∨ COM RD ∧ ERR CT 2 (Ø)]

Figure 3-22 Data Control Flow Diagram

The second half, or the remaining 18 bits of the data word are assembled in the same sequence as the first; however, the DCT5 pulse will shift BB00-17 into BA00-17 and load the BB00-17 with the shift register input. The DC CT flip-flop transition to (0) will set the DC DATA REQ flip-flop indicating that the buffer register is full and requests a DATAI instruction for transfer to the processor. Before the DATAI, the control can again load the shift register if the data request is not answered.

b. Read Reverse. - Table 3-4 shows the shift register content during a read reverse operation. The first T DATA STROBE pulse which produces the DCT1 pulse will load the RWB3-5 information from the R/W data mixer into SH12-14 and RWB0-2 into SH15-17. This assembles each 6-bit byte of the data word into the proper sequence in SH12-17. The DCT2 pulse is gated with ~ COM FWD to generate a DC SH SHIFT and DC END ARD pulse. This action shifts the first six low-order bits read from tape into SH06-11.

The DCT3 pulse is inhibited for the first two T DATA STROBE pulses by the same levels used during a read forward operation. The second T DATA STROBE allows the DCT1 pulse to again shift the low order bits in SH06-11 into SH00-05 and loads the second 6-bit byte into SH12-17. The DCT2 pulse produces another DC SH SHIFT and DC END ARD pulse which shifts the second six bits read into SH06-11, and the high-order six bits from SH00-05 to SH12-17. The third DCT1 pulse produced by T DATA STROBE shifts the low-order bits into SH06-11 and the second six bits read into SH00-05 and loads the last 6-bit byte, or high-order bits, from R/W data mixer into the SH12-17. After the delay, the DCT2 pulse performs a shift and an end around to transfer the second six bits read from SH00-05 to SH12-17, shift the high-order bits into SH06-11, and the low-order bits into SH00-05. The ERR CT2(0) and COM RD signals condition the gate to allow the DCT2 pulse to trigger the next 1.0 μs delay resulting in the DCT3 pulse. The DCT3 pulse, enabled by COM REV and COM RD inputs, produce the last DC SH SHIFT and DC END ARD pulse which transfers the information in the shift register into the proper order with the low-order bits in SH12-17 and the high-order six bits in SH00-05. The operation continues in the same sequence as read forward with the DCT5 pulses loading the first half of the data word into the buffer register and the DCT6 pulse setting the DCCT flip-flop. After the assembly of the second half of the data word in the shift register, the DCT4 pulse sets the DC SWAP flip-flop enabled by COM REV, DC CT (1) and COM RD. With this flip-flop set, the DCT5 pulse will initiate another DCT4 pulse which resets the DC SWAP flip-flop and generates a DC LOAD SH pulse. The DC LOAD SH pulse will transfer the 18 low-order bits from the BA register into the shift register and allow the DCT5 pulses to shift the low-order 18 bits in the BB register to the BA register, and load the low-order bits in the shift register into the BB register. This assembles the 36-bit data word in the proper order within the buffer register for transfer to the computer.

c. Write Forward. - Table 3-5 lists the data control sequence and the register content for the write forward operation. The DC sequence is initiated by the COM READY and ~ COM RD levels which generate the DCT3 pulse. At the completion of the DCT6 pulse, the data information has been transferred from the processor to the data buffer and the first half of the data word is positioned in the shift register. This sequence occurs as soon as the data request has been answered by a DATAO instruction from the processor. When the first word is ready to be written the T WR FWD level gates the 6 bits of the shift register into the R/W data mixer where it will be written on tape as two 3-bit bytes.

The first and second T DATA STROBE pulses result in only a DCT1 and DCT2 pulse which shifts the data within the shift register to allow the T WR FWD level to gate the data to the RWB. By the time the third T DATA STROBE pulse occurs the shift register has supplied 18 bits, or the first half of the data word, to the RWB. This T DATA STROBE pulse causes a DCT1 through DCT6 sequence which loads the second 18 bits of the data word into the shift register and produces the data request for the second data word. The next two T DATA STROBE pulses again enable only the DCT1 and DCT2 pulses to complete the writing of the data word. The last T DATA STROBE pulse results in DCT1 through DCT6 sequence which loads the second word from the processor into the buffer register and from the BA to the shift register. If the data request has not been answered by a DATAO instruction prior to the DCT3 pulse, the DC DATA MISS flip-flop will be set and the operation of the control will stop.

Table 3-3
Read Forward DC Sequence

Event	Action	Signal	Result
(1) T DATA STROBE / DCT 1 DCT 1 DC WR SET UP (0)	Shift each six bits of SH register to left Load R/W DATA 0-5 into SH 12-17	DC SH SHIFT DC SHIFT R/W DATA	SH [x x | x x | 0 1] 18 bits First six bits from R/W data mixer
DCT 1	Enable delay		
	1.0 μs delay		
DCT 2	No functional operation		
(2) T DATA STROBE / DCT 1 DCT 1 DC WR SET UP (0)	Shift each six bits of SH register to left Load R/W DATA 0-5 into SH 12-17	DC SH SHIFT DC SHIFT R/W DATA	SH [x x | 0 1 | 2 2] 18 bits Second six bits from R/W data mixer
DCT 1	Enable delay		
	1.0 μs delay		
DCT2	No functional operation		
(3) T DATA STROBE / DCT 1 DCT 1 DC WR SET UP(0)	Shift each six bits of SH register to left Load R/W DATA 0-5 into SH 12-17	DC SH SHIFT DC SHIFT R/W DATA	SH [0 1 | 2 2 | 3 3] 18 bits First half of data word
DCT 1	Enable delay		

Table 3-3 (Cont)
Read Forward DC Sequence

Event	Action	Signal	Result
	1.0 μs delay		
DCT 2 ∧ ERR CT 2(0) ∧ COM RD	Enable delay		
	1.0 μs delay		
DCT 3 ∧ ~ DC WRITE ∧ CT(0)	Enable delay		
	1.0 μs delay		
DCT 4	Enable delay		
	1.0 μs delay		
DCT 5 DCT 5(A) DCT 5(B)	Shift the contents of the BB register to the BA register Load SH 00-17 into the BA register		BA [x x | x x | x x] 18 bits BB [0 1 | 2 2 | 3 3] 18 bits
DCT 5 ∧ DC SWAP(0)	Generate DCT 6		
DCT 6	Complement DC counter	DC CT → (1)	
④ T DATA STROBE / DCT 1	Same as DCT 1 for ① T DATA STROBE		SH [x x | x x | 4 5] 18 bits

Table 3-3 (Cont)
Read Forward DC Sequence

Event	Action	Signal	Result
	1.0 μs delay		
DCT 2	Same as DCT 2 for ① T DATA STROBE		
⑤ T DATA STROBE / DCT 1	Same as DCT 1 for ② T DATA STROBE		SH [x x | 4 5 | 6 6] 18 bits
	1.0 μs delay		
DCT 2	Same as DCT 2 for ② T DATA STROBE		
⑥ T DATA STROBE / DCT 1	Same as DCT 1 for ③ T DATA STROBE		SH [4 5 | 6 6 | 7 7] 18 bits
	1.0 μs delay		
DCT 2 ^ ERR ^ CT 2(0) ^ COM RD	Enable delay		
	1.0 μs delay		
DCT 3 ^ ~ DC WRITE CT(0)	Enable delay		
	1.0 μs delay		
DCT 4	Enable delay		
DCT 5 DCT 5(A) DCT 5(B)	Shift the contents of the BB register to the BA register Load SH 00-17 into the BA register		BA [0 1 | 2 2 | 3 3] BB [4 5 | 6 6 | 7 7]

Table 3-3 (Cont)
Read Forward Sequence

Event	Action	Signal	Result
DCT 5 ^ DC SWAP(0)	Generate DCT 6		
DCT 6	Complement DC counter Request data transfer to processor	DC CT → (0) DC DATA RQ → (1)	
IOB DTC DATAI(A)	Transfer contents of buffer register to computer Read next word from tape in same sequence	DC DATA RQ → (0)	

Table 3-4
Read Reverse DC Sequence

Event	Action	Signal	Result
① T DATA STROBE / DCT 1 DCT 1 ^ DC WRITE SET UP(0)	Shift each six bits of SH register to left Load R/W DATA 3-5 into SH 12-14 and R/W DATA 0-2 into SH 15-17	DC SH SHIFT DC SHIFT R/W DATA	SH [x x | x x | 6 7] First six bits of data from R/W data mixer
DCT 1	Enable delay		
	1.0 μs delay		
DCT 2 ^ ~ COM FWD	Shift each six bits of SH register to left Shift SH 00-05 into SH 12-17	DC SH SHIFT DC END ARD	SH [x x | 6 7 | x x] 18 bits
② T DATA STROBE / DCT 1 DCT 1 ^ DCT WRITE SET UP (0)	Shift each six bits of SH register to left Load R/W DATA 3-5 into SH 12-14 and R/W DATA 0-2 into SH 15-17	DC SH SHIFT DC SHIFT R/W DATA	SH [6 7 | x x | 5 5] 18 bits Second six bits of data from R/W data mixer
DCT 1	Enable delay		
DCT 2 ^ ~ COM FWD	Shift each six bits of SH register to left Shift SH 00-05 into SH 12-17	DC SH SHIFT DC END ARD	SH [x x | 5 5 | 6 7] 18 bits

Table 3-4 (Cont)
Read Reverse DC Sequence

Event	Action	Signal	Result
(3) T DATA STROBE / DCT 1 DCT 1 ^ DC WRITE SET UP(0)	Shift each six bits of SH register to left Load R/W DATA 3-5 into SH 12-14 and R/W DATA 0-2 into SH 15-17	DC SH SHIFT DC SHIFT R/W DATA	SH 5 5 6 7 4 4 — 18 bits
DCT 1	Enable delay		
DCT 2 ~ COM FWD	Shift each six bits of SH register to left Shift SH 00-05 into SH 12-17	DC SH SHIFT DC END ARD	SH 6 7 4 4 5 5 — 18 bits
DCT 2 ERR ^ CT 2(0) COM RD	Enable delay		
	1.0 μs delay		
DCT 3 COM ^ REV COM ^ RD	Shift each six bits of SH register to left Shift SH 00-05 into SH 12-17	DC SH SHIFT DC END ARD	SH 4 4 5 5 6 7 — 18 bits Required order for transfer
DC 3 ~ DC WRITE CT(0)	Enable delay		
	1.0 μs delay		
DCT 4	Enable delay		
	1.0 μs delay		

Table 3-4 (Cont)
Read Reverse DC Sequence

Event	Action	Signal	Result
DCT 5 DCT 5(A) DCT 5(B)	Shift contents of BB register to BA register Load contents of SH register into BB register		BA: x x | x x | x x — 18 bits BB: 4 4 | 5 5 | 6 7 — 18 bits
DCT 5 DC SWAP(0)	Generate DCT 6		
DCT 6	Complement DC counter	DC CT → (1)	
(4) T DATA STROBE / DCT 1	Same as DCT 1 for (1) T DATA STROBE		SH: x x | x x | 2 3 — 18 bits Fourth six bits of data from R/W data mixer
	1.0 μs delay		
DCT 2	Same as DCT 2 for (1) T DATA STROBE		SH: x x | 2 3 | x x
(5) T DATA STROBE / DCT 1	Same as DCT 1 for (2) T DATA STROBE		SH: 2 3 | x x | 1 1 Fifth six bits of data from R/W data mixer
	1.0 μs delay		
DCT 2	Same as DCT 2 for (2) T DATA STROBE		SH: x x | 1 1 | 2 3

Table 3-4 (Cont)
Read Reverse DC Sequence

Event	Action	Signal	Result
⑥ T DATA STROBE / DCT 1	Same as DCT 1 for ③ T DATA STROBE		SH [1 1 2 3 0 0] 18 bits
	1.0 μs delay		
DCT 2	Same as DCT 2 for ③ T DATA STROBE		SH [2 3 0 0 1 1] 18 bits
	1.0 μs delay		
DCT 3	Same as DCT 3 for ③ T DATA STROBE		SH [0 0 1 1 2 3] Required order for transfer
	1.0 μs delay		
DCT 4 ^ COM REV ^ COM RD ^ DC CT(1)	Allow infomation swap	DC SWAP → (1)	
DCT 4	Enable delay		
	1.0 μs delay		
DCT 5 DCT 5(A) DCT 5(B)	Shift contents of BB register to BA register Load contents of SH register into BB register Clear SH register	DC SH CLR	BA [4 4 5 5 6 7] BB [0 0 1 1 2 3] SH [0 0 0 0 0 0]
DCT 5 ^ DC SWAP(1)	Enable delay		

Table 3-4 (Cont)
Read Reverse DC Sequence

Event	Action	Signal	Result
	1.0 μs delay		
DC 4 DC SWAP(1)	Transfer contents of BA register to SH register	DC LOAD SH	SH 4 4 5 5 6 7
DC 4 COM REV DC CT(1) COM RD	Disable DC Swap	DC SWAP → (0)	
DCT 4	Enable delay		
	1.0 μs delay		
DCT 5 DCT 5(A) DCT 5(B)	Shift contents of BB register to BA register Load contents of SH register into BB register		BA 0 0 1 1 2 3 18 bits BB 4 4 5 5 6 7 18 bits Required order for transfer
DCT 5 DC SWAP(0)	Generate DCT 6		
DCT 6	Complement DC counter Wait for DATAI instruction to transfer buffer register data to processor	DC CT → (0)	

Table 3-5
Write Forward DC Sequence

Event	Action	Signal	Result
IOB DTC CONO SET IOB ∧ DTC CONO SET IOB 27(B)	Load control data Request data	DC DATA REQ → (1)	
	1.0 μs delay		
COM ∧ READY ~ COM RD	Generate DCT 3		
DCT 3 ∧ ~ COM RD	Clear shift register	DC SH CLR	SH 0 0 | 0 0 | 0 0 — 18 bits
COM WR DC CT(0)	Set DC DATA NEED	DC DATA NEED → (1)	
	Indefinite delay		
IOB DTC DATAO SET	Load data buffer Clear DC DATA RQ	DC DATA RQ → (0)	BA 0 1 | 2 2 | 3 3 — 18 bits BB 4 5 | 6 6 | 7 7 — 18 bits
~ COM DATA PI REQ DC DATA NEED(1)	Enable 1.0 μs delay		
	1.0 μs delay		
DCT 4 ∧ ~ COM RD	Load shift register with contents of BA		SH 0 1 | 2 2 | 3 3 — 18 bits
	1.0 μs delay		

Table 3-5 (Cont)
Write Forward DC Sequence

Event	Action	Signal	Result
DCT 5 DCT 5A DCT 5B	Shift contents of BB to BA register Transfer contents of SH register to BB register		BA 4 5 | 6 6 | 7 7 — 18 bits BB 0 1 | 2 2 | 3 3 — 18 bits Nonusable Data
DCT 5 ^ DC SWAP(0)	Reset data need Generate DCT 6	DC DATA NEED → (0)	
DCT 6	Complement DC counter	DCCT → (1)	
	Gate first six bits in SH 00-05 into R/W data mixer 0-5	T WR FWD	R/W Data Mixer 0 1 — 6 bits
① T DATA STROBE / DCT 1 DCT 1 ^ DC WR SET UP(0)	Shift six bit bytes of SH register left Load R/W DATA 0-5 into SH 12-17	DC SH SHIFT DC SHIFT RW DATA	SH 2 2 | 3 3 | x x — 18 bits Non Valid Data from RWB
	1.0 μs delay		
DCT 2	No operation		
	Gate second six bits in SH 00-05 into R/W data mixer 0-5	T WR FWD	R/W Data Mixer 2 2 — 6 bits
② T DATA STROBE / DCT 1 DCT 1 ^ DC WR SET UP(0)	Shift six bit bytes of SH register left Load R/W DATA 0-5 into SH 12-17	DC SH SHIFT DC SHIFT R/W DATA	SH 3 3 | x x | x x — 18 bits

Table 3-5 (Cont)
Write Forward DC Sequence

Event	Action	Signal	Result
	1.0 μs delay		
DCT 2	No operation		
	Gate third 6 bits of data from SH 00-05 into R/W data mixer 0-5	T WR FWD	R/W Data Mixer [3 3] 6 bits
③ T DATA STROBE / DCT 1 DCT ∧ 1 DC WR SET UP(0)	Shift 6-bit bytes of SH register to left Load R/W DATA 0-5 into SH 12-17	DC SH SHIFT DC SHIFT RW DATA	SH [x x x x x x] 18 bits
	1.0 μs delay		
DCT ∧ 2 ERR ∧ CT 2(0) COM ∧ WR DC WR SET UP 0	Enable 1.0 μs delay		
	1.0 μs delay		
DCT ∧ 3 ~ COM RD DCT ∧ 3 ~ DC WRITE ∧ CT(0)	Clear shift register Enable 1.0 μs delay	DC SH CLR	SH [0 0 0 0 0 0] 18 bits
	1.0 us delay		
DCT ∧ 4 ~ COM RD	Load contents of BA into SH register	DC LOAD SH	SH [4 5 6 6 7 7] 18 bits
DCT 4	Enable 1.0 μs delay		

Table 3-5 (Cont)
Write Forward DC Sequence

Event	Action	Signal	Result
DCT 5 DCT 5(A) DCT 5(B)	1.0 μs delay Shift contents of BB to BA register Transfer contents of SH register to BB register		BA [0 1 | 2 2 | 3 3] 18 bits BB [4 5 | 6 6 | 7 7] 18 bits Non Valid Data
DCT 5 DC SWAP(0)	Generate DCT 6		
DCT 6	Complement DC counter SET DC data request	DC CT → (0) DC DATA RQ → (1)	
	Gate fourth 6 bits of data from SH 00-05 into R/W data mixer 0-5	T WR FWD	R/W Data Mixer [4 5] 6 bits
(4) T DATA STROBE / DCT 1	Same as (1) T DATA STROBE		SH [6 6 | 7 7 | x x] 18 bits
	1.0 μs delay		
DCT 2	No operation		
	Gate fifth 6 bits of data from SH 00-05 into R/W data mixer 0-5	T WR FWD	R/W Data Mixer [6 6] 6 bits
(5) T DATA STROBE / DCT 1	Same as (2) T DATA STROBE		SH [7 7 | x x | x x] 18 bits

Table 3-5 (Cont)
Write Forward DC Sequence

Event	Action	Signal	Result
	1.0 μs delay		
DCT 2	No operation		
	Gate last 6 bits of data from SH 00-05 into R/W data mixer 0-5	T WR FWD(1)	R/W Data [7 7] 6 bits
(6) T DATA STROBE / DCT 1	Same as (3) T DATA STROBE		SH [x x x x x x] 18 bits
	1.0 μs delay		
DCT 2 ∧ ERR CT 3(1) ∧ COM W ∧ DC WR SET UP(0)	Enable 1.0 μs delay		
	1.0 μs delay		
DCT 3 ∧ ~ COM WR	Clear shift register	DC SH CLR	SH [0 0 0 0 0 0] 18 bits
DCT 3 ∧ DC WRITE ∧ CT(0)	Set data need	DC DATA NEED(1)	
IOB DTC DATAO	Clear and load data buffer with new word: Sequence the same as first word.	NOTE: This may occur anytime after the DCT 6 pulse of the (3) T DATA STROBE until after the 7 T DATA STROBE.	

d. Write Reverse. - Table 3-6 lists the DC control sequence and register content for the write-reverse operation. This operation necessitates the reorganization of the data word to allow the low-order three bits to be written first. To accomplish this, the information is shifted between the shift register and buffer register and internally in the shift register in the following sequence.

The IOB DTC CONO SET pulse initiates the data control operations and enables the generation of DCT 3 through DCT 5 pulses. The sequence rearranges the data within the buffer register, via the shift register, to allow the low-order 18 bits of the data word to be written first. The 18 low-order bits are shifted into the shift register during the next DCT 4 - DCT 6 sequence and a DCT 1 and DCT 2 pulse shifts the information within the shift register to allow the low-order 6 bits to be transferred to the RWB by means of the R/W data mixer. The first T DATA STROBE pulse again produces a DCT 1 and DCT 2 pulse to arrange the shift register information, such that the second lowest order six bits will be transferred to the RWB by the R/W data mixer and the second T DATA STROBE pulse performs the same events for the last six bits to allow the complete first half of the data word to be written. The third T DATA STROBE pulse initiates a complete DCT 1 - DCT 6 pulse sequence which clears the shift register, loads the high-order 18 bits into it and generates a request to the processor for a new data word. At the completion of the DCT 6 sequence, a DCT 1 and DCT 2 pulse positions the low-order 6 bits in the shift register for transfer to the RWB and the next two T DATA STROBE pulses complete the DC write sequence for the high-order bits. The last T DATA STROBE pulse conditions the registers to receive the next data word and when received, repositions the buffer register data and loads the high-order bits of the second data word into the shift register. The data control operation then continues in the same sequence as for the first word written. The DC DATA MISS flip-flop will be set for the same conditions as described in the write forward operation and will halt the data transferred.

Table 3-6
Write Reverse DC Sequence

Event	Action	Signal	Result
IOB DTC CONO SET	Load control information		
IOB DTC CONO SET ∧ IOB 27(B)	Generate data request	DC DATA RQ → (1)	
	1.0 μs delay		
COM READY ∧ ~ COM RD	Generate DCT 3		
DCT 3 ∧ ~ COM RD	Clear shift register	DC SH CLR	SH 0 0 0 0 0 0 18 bits
DCT 3 ∧ DC WRITE ∧ CT(0)	Set data need	DATA NEED → (1)	
IOB DTC DATA SET	Load first data word into buffer register		BA 0 0 1 1 2 3 18 bits
	Clear data request	DC DATA RQ → (0)	BB 4 4 5 5 6 7 18 bits
DC DATA NEED(1) ∧ ~ COM DATA PI REQ	Enable 1.0 μs delay		
	1.0 μs delay		
DCT 4 ∧ ~ COM RD	Load shift register from BA register	DC LOAD SH	SH 0 0 1 1 2 3 18 bits
DCT 4 ∧ ~ COM WR ∧ COM REV ∧ DCCT(0)	Allow information swap	DC SWAP → (1)	

Table 3-6 (Cont)
Write Reverse DC Sequence

Event	Action	Signal	Result
DCT 4 COM REV COM WR	Allow write set up	DC WR SET UP → (1)	
DCT	Enable delay		
	1.0 μs delay		
DCT 5 DCT 5(A) DCT 5(B)	Shift contents of BB to BA register Load the BB register with contents of shift register		BA 4 4 5 5 6 7 18 bits BB 0 0 1 1 2 3 18 bits
DCT 5 DCT 5 DC SWAP(1)	Clear data need Clear shift register Enable delay	DC DATA NEED → (0) DC SH CLR	SH 0 0 0 0 0 0 18 bits
	1.0 μs delay		
DCT 4 ~ COM RD	Load shift register from BA register	DC SH LOAD	SH 4 4 5 5 6 7 18 bits
DCT 4 COM REV DC CT(0) COM WR	Disable information swap	DC SWAP → (0)	
DCT 4	Enable delay		

Table 3-6 (Cont)
Write Reverse DC Sequence

Event	Action	Signal	Result
	1.0 μs delay		
DCT 5 DCT 5(A) DCT 5(B)	Shift contents of BB register to BA Load BB register with contents of SH register		BA 0 0 | 1 1 | 2 3 4 4 | 5 5 | 6 7 Non Valid Data
DCT 5 DC SWAP(0)	Generate DCT 6		
DCT 6	Complement DC counter	DC CT → (1)	
DCT 6 DC WRITE SET UP(1)	Generate DCT 1		
DCT 1 DCT 1 DC WR SET UP(1)	Shift 6-bit bytes of shift register to left Load SH 00-05 into SH 12-17	DC SH SHIFT DC END ARD	SH 5 5 | 6 7 | 4 4 18 bits
DCT 1	Enable delay		
	1.0 μs delay		
DCT 2 ~ COM FWD	Shift each 6 bits of SH register left Load SH 00-05 into SH 12-17	DC SH SHIFT DC END ARD	SH 6 7 | 4 4 | 5 5 18 bits
DCT 2	Disable write set up	DC SET UP → (0)	

Table 3-6 (Cont)
Write Reverse DC Sequence

Event	Action	Signal	Result
	Gate SH 00-02 into R/W data mixer 3-5 and SH 03-05 into R/W data mixer 0-2	T WR REV	R/W Data Mixer [$\overline{7}$ $\overline{6}$] 6 bits
(1) T DATA STROBE / DCT 1 DCT 1 DC WRITE SET UP(0)	Shift each 6 bits of SH register to left Load R/W DATA 0-5 into SH 12-17	DC SH SHIFT DC SHIFT R/W DATA	SH [4 4 | 5 5 | x x] 18 bits
DCT 1	Enable delay		
	1.0 μs delay		
DCT 2 ~ COM FWD	Shift each 6 bits of SH register to left Load contents of SH 00-05 into SH 12-17	DC SH SHIFT DC END ARD	SH [5 5 | x x | 4 4] 18 bits
	Gate contents of SH 00-02 into R/W data mixer 3-5 and SH 03-05 into R/W data mixer 0-2	T WR REV	R/W Data Mixer [$\overline{5}$ $\overline{5}$] 6 bits
(2) T DATA STROBE / DCT 1	Shift each 6 bits of SH register to left Load R/W DATA 0-5 into SH 12-17	DC SH SHIFT DC SH SHIFT R/W DATA	SH [x x | 4 4 | x x] 18 bits
DCT 1	Enable delay		

Table 3-6 (Cont)
Write Reverse DC Sequence

Event	Action	Signal	Result
DCT 2 ~ COM FWD	1.0 μs delay Shift each 6 bits of SH register to left Shift contents of SH 00-05 into SH 12-17	DC SH SHIFT DC END ARD	SH [4 4 | x x | x x] 18 bits
	Gate contents of SH 00-02 into R/W data mixer 3-5 and SH 03-05 into R/W data mixer 0-2	T WR REV	R/W Data Mixer [$\overline{4}$ $\overline{4}$] 6 bits
(3) T DATA STROBE DCT 1 DCT 1	Data transfer Non functional Enable delay		
	1.0 μs delay		
DCT 2 ~ COM FWD	Data transfer non functional		
DCT 2 ERR CT 3(1) COM WR DC WR SET UP(0)	Enable delay		
	1.0 μs delay		
DCT 3 ~ COM RD	Clear shift register	DC SH CLR	SH [0 0 | 0 0 | 0 0] 18 bits
DCT 3 ~ DC WRITE CT(0)	Enable delay		
	1.0 μs delay		

Table 3-6 (Cont)
Write Reverse DC Sequence

Event	Action	Signal	Result
DCT 4 ~ COM RD	Load shift register from BA register	DC LOAD SH	SH [0 0 | 1 1 | 2 3] 18 bits
DCT 4 COM REV COM WR	Allow write set up	DC WR SET UP → (1)	
DCT 4	Enable delay		
	1.0 μs delay		
DCT 5 DCT 5(A) DCT 5(B)	Data transfer operations non functional		
DCT 5 DC SWAP(0)	Generate DCT 6		
DCT 6	Complement DC counter	DC CT → (0)	
DC CT → (0)	Request data from processor	DC DATA RQ → (1)	
DCT 6 DC WR SET UP(1)	Generate DCT 1		
DCT 1 DCT 1 DC WR SET UP(1)	Shift each 6 bits of SH register to left Shift contents of SH 00-05 into SH 12-17	DC SH SHIFT DC END ARD	SH [1 1 | 2 3 | 0 0] 18 bits

Table 3-6 (Cont)
Write Reverse DC Sequence

Event	Action	Signal	Result
DCT 1	Enable delay		
	1.0 μs delay		
DCT 2 ~ COM FWD	Shift each 6 bits of SH 00-05 into SH 12-17 Shift contents of SH 00-05 into SH 12-17	DC SH SHIFT DC END ARD	SH [2 3 | 0 0 | 1 1] 18 bits
DCT 2	Clear write set up	DC WR SET UP (0)	
	Gate SH 00-02 into R/W data mixer 3-5 and SH 03-05 into R/W data mixer	T WR REV	R/W Data Mixer [$\overline{3}$ $\overline{2}$] 6 bits
(4) T DATA STROBE DCT 1	Same as (1) T DATA STROBE		SH [0 0 | 1 1 | x x] 18 bits
	1.0 μs delay		
DCT 2	Same as DCT 2 pulse for (1) T DATA STROBE		SH [1 1 | x x | 0 0] 18 bits
	Gate SH 00-02 into R/W data mixer 3-5 and SH 03-05 into R/W data mixer 0-2	T WR REV	R/W Data Mixer [$\overline{1}$ $\overline{1}$] 6 bits
(5) T DATA STROBE	Same as (2) T DATA STROBE		SH [x x | 0 0 | x x] 18 bits
	1.0 μs delay		

Table 3-6 (Cont)
Write Reverse DC Sequence

Event	Action	Signal	Result
DCT 2	Same as DCT 2 for (2) T DATA STROBE		SH | 0 0 | x x | x x |
	Gate SH 00-02 into R/W data mixer 3-5 and SH 03-05 into R/W data mixer 0-2	T WR REV	R/W Data Mixer | $\overline{0}$ $\overline{0}$ | 6 bits
(6) T DATA STROBE DCT 1	Same as DCT 1 for 3 T DATA STROBE		
	1.0 μs delay		
DCT 2	Same as DCT 2 for (3) T DATA STROBE		
	1.0 μs delay		
DCT 3	Set data need and wait for DATAO instruction to load next word into buffer register Continue in sequence from IOB DTC DATA SET		

The writing of mark track information on tape requires writing end zone characters as soon as the tape motion starts. To accomplish this, the ~ T WAIT level is gated with the COM WR MT level to produce the T ACT COND level (Dwg TD10A-0-T2) which allows the TP0 pulse to set the T ACT flip-flop. The T ACT(1) transition will set the T WREN flip-flop, enabled by the ~ ERR SW and COM WR input to the conditioning gate. The T WREN output allows the read/write amplifiers to write in the 3 data tracks.

The CONO DTC instruction which initiated the WRTM function also set the DC DATA REQ flip-flop to request the first data word containing the mark track information. The mark track write amplifier inputs are from the WRB0 flip-flop which normally feeds the amplifier used to write the data information in data track 1; therefore, the same bits of data written in the mark track will also be written in data track 1. To accomplish the writing of mark track information, bits 0, 3, 6, 9, 12, 15, 18, 21, 24, 27, and 30 of the data word will contain the bit configuration of two complete mark track codes to be written. Figure 3-18 shows the data bit configuration required for writing an end zone code on tape. The information in data track 1, however, is not valid and will have no effect when the data information is written.

Table 3-7
Data Format for WRTM Function

END ZONE CODE	5			5			5			5		
MARK TRACK	1	0	1	1	0	1	1	0	1	1	0	1
DATA TRACK 1	1	0	1	1	0	1	1	0	1	1	0	1
DATA TRACK 2	x	x	x	x	x	x	x	x	x	x	x	x
DATA TRACK 3	x	x	x	x	x	x	x	x	x	x	x	x

With the first mark track code loaded into the buffer register by a DATAO DTC instruction, the T ACT(1) level transition, enabled by the COM WR and ~ COM DATA level to the conditioning gate (Dwg TD10A-0-T1) will result in the first T DATA STROBE pulse. Each succeeding T DATA STROBE pulse will be produced at TP0 time, conditioned by the AND gate whose inputs are T ACT(1), ~ T PAUSE, COM WR and TCT 1(0). The ~ T PAUSE input is a result of the mark track register (Dwg TD10A-0-MK) being disabled by the absence of the TP1(SP) pulse input. The TP1 (SP) inputs, are inhibited by the ~ ST WRTM level (Dwg TD10A-0-T1). The mark track information is assembled and written under program control over the entire tape length of tape ending with the forward end zone codes on the last 10 ft of tape.

3.7 FUNCTIONAL OPERATIONS

Bits 27, 28, and 29 of the CONO DTC instruction determine the functional operation of the selected DECtape transport. These functions and codes are listed in Table 3-2. The following paragraphs describe the operation of the TD10 control for each specified function. Figure 3-23 is a timing diagram for read-write block number, data, and all functions.

During all operations, after the CONO command specifies the function, the transfer of data occurs at the times determined by the T ACT levels. The T ACT flip-flop is set and cleared during the reading and writing of block numbers, data, and all, by the signal shown on Dwg No. TD10A-0-T2. When the write timing and mark track function is specified, the T ACT flip-flop is set immediately after ~ T WAIT level appears to allow the preformatting over the entire area of tape.

At the completion of a transfer sequence the ENB FCN STOP flip-flop Dwg TD10A-0-ENB which is set when a data miss error occurs or when bit 35 of a CONO DTC instruction is a 1, together with the T ACT (0) level will allow the TP1 (B) pulse to set the ST JOB DONE flip-flop, Dwg No. TD10A-0-ST. This flip-flop output prevents the T ACT flip-flop from being set again until a new CONO command is issued. The ST JOB DONE is described in Paragraph 3.10.2. A succeeding CONO command is required to clear the ST JOB DONE flip-flop and initiate a new transfer sequence. The T INACT COND level as described in Paragraph 3.6.4, determines the exact position on the tape where the data transfers occur during a CONO command.

3.7.1 Write Timing and Mark Track

The write timing and mark track (WRTM) function is selected by a 100 binary configuration in the COM FCN register and is used to preformat the timing and mark track codes on tape prior to the recording of data. The WRTM function is enabled by the WRTM switch on the TD10A Control Panel in the up position. The WRTM switch shown on Dwg TD10A-0-ST, when activated, provides the ST WRTM level. The ST WRTM level, gated with COM WR MT input on Dwg TD10A-0-ERR, produces a ERR SW level if the switch is in the wrong position. N ERR SW is gated with COM WR MT, Dwg TD10A-0-T1 (sheet 2) to provide the T/M ENB conditioning level to the TCK 1 and TCK 0 flip-flop. The 120 kc pulse output of the clock drives the TCK flip-flop which is connected as a counter. The TCK 0 is activated through a complete cycle every 33.33 μs. The TCK 0 and TCK 1 outputs are DCD gated to generate the TP0 and TP1 pulses (at center of Dwg TD10A-0-T1) as soon as the CONO information is received in the command register. The TCK 0 flip-flop outputs are inputs to the RWA G882 (Dwg TD10A-0-RWA) and cause the writing of the timing track signals on tape when the T/M ENB level is present.

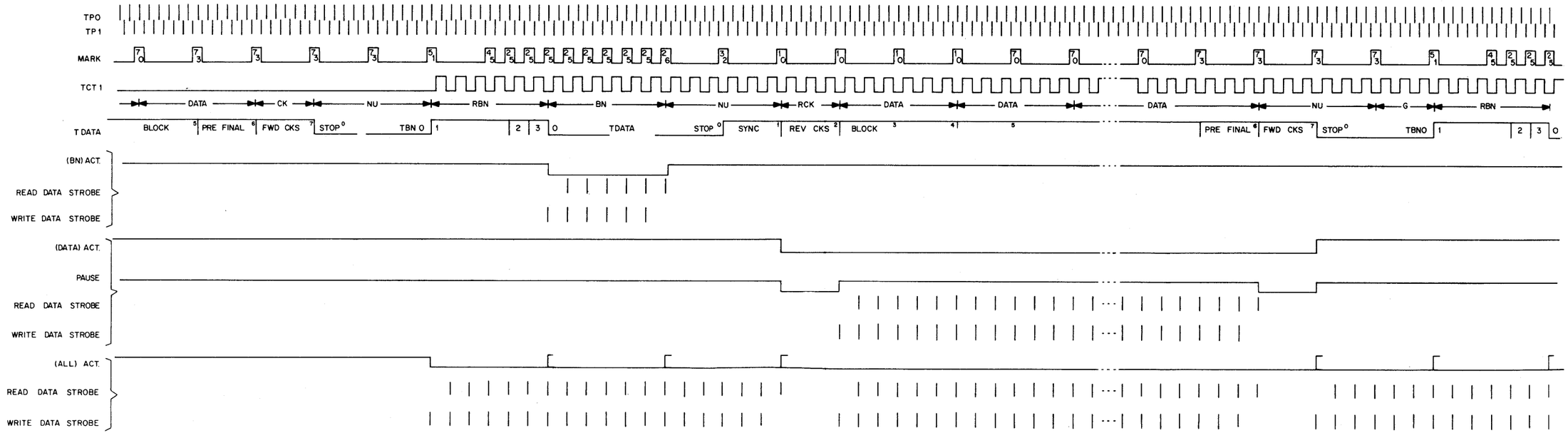


Figure 3-23 TD10A Function Timing Diagram

3.7.2 Write Data

The write data operation, specified by a 111 in the function register, COM FCN 0-2, allows writing data and checksum information in either the forward or reverse direction into areas assigned on tape. This function can be preceded by a read block number function if writing data is requested in a block other than the first block on tape. For this operation, the read block number function performs the initiating action process which enables the tape unit selected to reach operating speed. By comparing the block number read with the desired block number, the processor determines the direction of tape motion required to locate the desired block number. DATAI DTC instructions will continually read in block numbers until the desired block is identified. The next CONO DTC instruction commands control to write into the assigned areas on tape.

Figure 3-19 is the timing diagram for the write data function. The TP0, TP1, and TP1 (SP) pulses (Dwg TD10A-0-T1, Sheet 1), enabled by the T UPS1(1) level, when the tape motion is up to speed, are produced by the RWA TM pulses from the timing track amplifier outputs. The TP1 (SP) pulses, gate the mark track information (RWA MK TRK) from the mark track amplifiers, into MK8, to allow the decoding of the mark track data.

The T ACT flip-flop (Dwg TD10A-0-T2) is set by the TP0 pulse during a data function when the MK DATA END (10_8 V 73_8) and T SYNC levels are present. The T ACT flip-flop sets the T WREN flip-flop, allowing the write operation to begin; however, the T WR FWD or T WR REV pulses which are used to load the data word into the RWB, are inhibited until the T PAUSE level (Dwg TD10A-0-T1, Sheet 2) is removed. This prevents writing data in the checksum areas on tape. The TP0 pulses, enabled by T ACT (1), ~ T PAUSE, COM WR, and the TCT (0) transition, generate the T DATA STROBE pulses (Dwg TD10A-0-T1, Sheet 1) to load the buffers for the dc write sequence. After the computed parity is written at the end of a block, the T INACT COND level will allow the TP0 pulse to reset the T ACT and T WREN flip-flops (Dwg TD10A-0-T2) to disable the write operation. During a write data function the T INACT COND level is produced by inputs T FWD CKS and MK DATA END. The recording of data on tape continues until halted by a CONO DTS which enables the function stop (ENB FCN STOP) until data is missed or until a CONO DTC instruction stops the command in process.

3.7.3 Write Block Number

The block number function, specified by a 110-bit configuration in the function register (FCN0-2) allows numbers to be written in the block number area on tape, prior to the recording of data. If the block number and data are to be written simultaneously, the write all function is used. The block number is the octal configuration assigned to each 3 bit line on tape in the block number area, starting at block number 0 and incrementing to the maximum number of blocks required. No actual block number

is inserted in the first block, (block 0) and data can only be recorded by a write/reverse operation which identifies the reverse block number before writing in the first data area.

After the CONO DTC instruction is received, the tape transport is allowed to reach "up to speed," and the TP1 timing pulses serially load the mark track information into the mark track register for decoding. The decoded MK BN SYNC (51_8) which appears after the first data block area on tape, initiates the TBN counter sequence. The COM BN, TBN0(1), TBN CT, and ST JOB DONE(0) inputs, shown on Dwg TD10A-0-T2, produce the T ACT COND level at the same time the TBN CT and TBN0(1) level produce the T INACT COND level. With both the T ACT COND and T INACT COND levels present, the TP0 pulse complements the T ACT flip-flop from the (0) to (1) states and sets the T WREN flip-flop to enable the write amplifiers. The write sequence is initiated and the 36-bit block number is written on tape enabled by the T WR FWD level and T DATA STROBE pulses. The COM FWD level is asserted regardless of the actual direction of tape motion to provide compatability with the block number formats on tape controls which do not perform an automatic complement obverse function. At the end of the block number, the decoded MK BN END (26_8) pulse produces a T INACT COND level, resulting in another T PAUSE and the T ACT and T WREN flip-flops will be reset. The sequence continues until all the required block numbers are entered on tape. Tape motion will continue until the end zone is reached, a CONO DTC instruction resets the GO flip-flop or CONO DTS indicates a (1) bit in the ENB FCN STOP.

3.7.4 Write All

The write all function is specified by a 101 binary configuration in the function register, COM FCN 0-2, and allows the continuous writing of block numbers and data on tape in one pass and provides access to data areas on tape which are not used in the block number and data modes. The COM GO FWD or COM GO REV level initiates tape motion and activates the 120 μs "up to speed" delay (Dwg TD10A-0-T1, Sheet 2). The UPS1(1) level enables the TP0, TP1, and TP1(SP) pulses to load the mark track register with the mark track codes. The decoded MK BN SYNC (51_8), COM ALL, and ST JOB DONE(0) levels (Dwg TD10A-0-T2) generates the T ACT COND level to allow the TP0 pulse to set the T ACT flip-flop and consequently, the T WREN flip-flop. The T ACT(1) level enables the timing counter TCT1 by the TP1 pulse. The T WR FWD or T WR REV level is immediately present to load the first six bits of the reverse block-number information into the RWB. The reverse block number, forward block number, and data are continuously recorded until the end zone is reached or until a CONO DTS instruction or DATA MISS(1) error enables ENB FCN STOP(1) to produce the T INACT COND level. Any of these will reset the T WREN flip-flop; however, tape motion will continue.

3.7.5 Read Block Number

The read block-number function, initiated by a 110 binary configuration in the function register, permits a specified block number to be located prior to the reading of the data within the block. The tape unit is allowed to reach operating speed and the T ACT level and TBN counter sequence is initiated by the same levels which occur during the write block number sequence. However, the ~ COM WR level prevents the T WREN flip-flop being set. The COM FCN1(1) input (Dwg TD10A-0-T2) enables the T INACT COND to reset the T ACT flip-flop when the block number is read. When the desired block number is located, a CONO DTC instruction must be issued to read the information within the desired block.

3.7.6 Read Data

The read data function, specified by a 010 binary configuration in the function register is normally preceded by a read block number function to locate the desired block of data; however, a read data function may be implemented to continuously read the data in a specified number of blocks starting at block number 0. The T ACT flip-flop is enabled by the same levels used during the write data function and T WREN level is inhibited by the ground COM WR level. The COM FCN(1) level enables the T INACT COND level to be produced at the required times to reset the T ACT flip-flop after a complete block of data has been read. The T PAUSE LEVEL, also enabled by the T INACT level, prevents transferring the checksum information to the processor. Each data block is read and transferred until a CONO DTC instruction is issued to stop the present command or until the end zone on tape is reached. The ENB FCN STOP(1) level which occurs when a data miss error is detected or when bit 35 of the CONO DTS instruction is (1) enables the ST JOB DONE flip-flop to be set to a 1, inhibiting the T ACT COND levels and requesting a flag interrupt.

3.7.7 Read All

The read all function, specified by a 001 binary configuration in the function register, permits reading of both block numbers and data from tape continuously and in sequence from either the reverse block number of block 0 or from a block number located by a read block number function. The operation of the control is similar to the write all function with the T ACT flip-flop being set by the decoded MK BN SYNC (51_8) level. This allows both the reverse and forward block number to be read in one pass. The T WREN flip-flop is disabled by the absence of the COM WR input, and the T INACT COND level is inhibited until ENB FCN STOP(1) level is received, indicating a function stop bit or data miss error. The information on tape, except for parity, will continuously be read and transferred to the processor until a new command is issued, a data miss error is detected, or a CONO DTS instruction sets the ENB FCN STOP flip-flop.

3.8 LONGITUDINAL PARITY (Dwg TD10A-0-LP/ERR)

The longitudinal parity is written in the checksum area on tape after the last data word is recorded in a block. The parity information is written as two 3-bit lines in the 18-line area assigned. During both reading and writing, each 6-bit byte of the information transferred between the control and processor is half added in the LP buffer, such that a 0 bit output of the R/W data mixer will complement the respective LP flip-flop at every other TP0 pulse. The T SYNC level initially sets the LP buffer to all ones and the ~T REV CKS and TCT 1 (0) inputs prevent any R/W data information from entering the LP buffer prior to the last 6 bits of reverse checksum area on tape. At the start of the data area, the ~T REV CKS and TCT (0) levels allows the TP0 pulse to half-add each 6-bit byte into the LP buffer.

During a write operation, an octal 111111 is written by hardware into the reverse checksum area by the T WR LP level at TP1 time, and the parity of the data is then computed. The T WR LP level enables the computed parity to be written into the forward checksum area by the TP1 pulses.

The LP buffer is cleared after the third byte of ones is entered into the reverse checksum slot by the LP CLR pulse. During reading, the LP CLR pulse clears the LP buffer prior to reading the third byte of the reverse checksum slot.

Only the first 6 bits of the forward checksum are checked therefore, the parity check is performed on the last 6 bits of the reverse parity slot, on the data words and on the first 6 bits of the forward checksum.

An example of the parity computation for one word is shown in Figure 3-24.

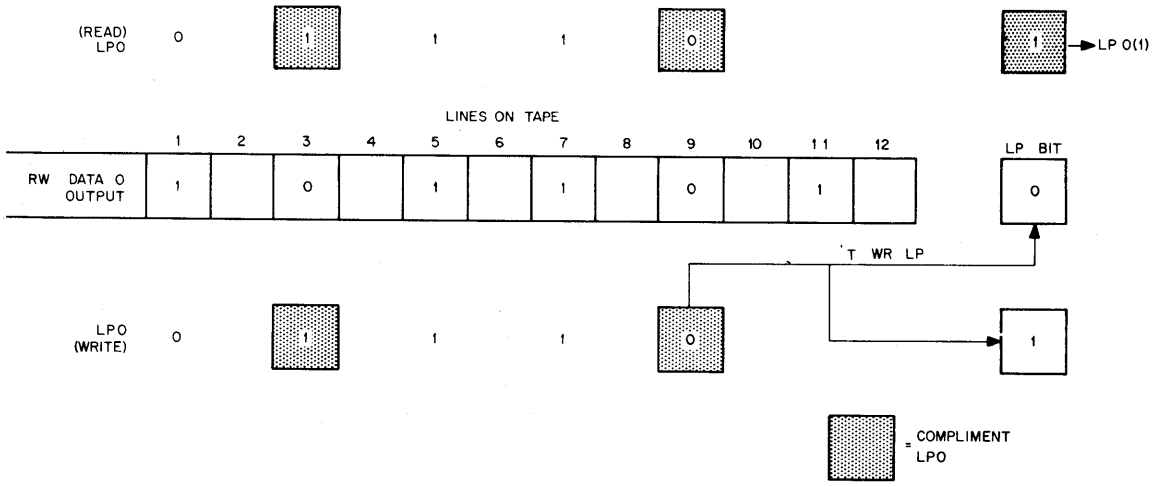


Figure 3-24 Longitudinal Parity Computation

Of the twelve 3-bit lines written for each 36-bit word written on tape, the R/W data 0 output is used for one bit every other line. The state of LP0 after the last word is written is recorded as a checksum bit. While reading, if the LP bit is (0), the LP0 flip-flop will again be complemented resulting in a LP0 (1) level. The output of each LP flip-flop is AND gated to produce the LP 1 output, indicating correct parity.

3.9 ERROR CHECKING

The TD10A control provides error checking circuits to prevent writing when an operational error is detected or to inform the processor of the error condition where requested by a CONI DTS instruction.

3.9.1 Mark Track Error (Dwg TD10A-0-LP/ERR)

In addition to the checking provided by the mark track register which insures that a decoded mark track follows a specific mark track bit configuration, error circuits are included to check for the occurrence of a mark track in every 6-bit position when reading and writing. The ERR CK flip-flop is set by the TP0 pulse enabled by the MK BN END (26_8) level at the end of the forward block mark and remains set until the MK BN SYNC (51_8) level appears at the start of the next block of information. The purpose of ERR CK is to avoid false error conditions from the 45_8 code which is not decoded and from the series of 25_8 codes that occur between blocks. The output of the ERR CK flip-flop is ANDed with a ~ MK PRES, ERR CT2(0), T ACT (1), and TCT 1(0) at the beginning of each data word. If the MK PRES level has not occurred when the remaining conditions are true, the TP1 pulse will set the ERR MK TRK flip-flop indicating an error condition.

The ERR MK TRK flip-flop is also set if a MK PRES level appears at a time other than the specified time. The TCT 1(0) and ERR CT2 (0) levels produce the ERR MK TIME level output. This signal gated with ERR CK (1) and T ACT (1) insures that if a MK PRES level appears in the five slots between legal marks, then an error condition is indicated.

The T DATA counter and T BN counter outputs are gated with the decoded MK DATA SYNC (32_8) and MK BN SYNC (51_8) to insure that the counters contain 0 prior to reading and writing block numbers and data. If any counter flip-flop is set when the sync pulses occur, the TP0 pulse will collector-set the ERR MK TRK flip-flop indicating an error condition.

The ERR MK TRK (1) output is used both to collector-set the ST PAR ERR flip-flop (Dwg TD10A-0-ST) indicating a parity error and as a status bit to IOB28 during a CONI DTS instruction.

3.9.2 Switch and Select Errors (Dwg TD10A-0-LP/ERR)

The ERR SW level is produced by a combination of inputs from the WRTM switch and the functions listed as follows. In addition, the ERR SW level is produced if no TU55 Transport is selected by the transport select switch, or if more than one transport has the same device number.

a. The WRTM switch is in the on position (up) and the command received is not COM WR MT.

b. The command received is COM WR MT and the WRTM switch is in the off position (down).

c. A command to write is specified COM WR and the selected TU55 Transport WRITE LOCK function is enabled.

d. The ERR SEL level is present when the COM SEL (1) level occurs. The ERR SEL level is produced by the single unit comparator logic.

This is effectively accomplished by noting the resistance of the SINGLE UNIT line and generating a ground select error level (SE), if the resistance is not within the specified limits.

With no units connected, the voltage at pins E and K of comparator W520 is -9V. The voltage at pin D and pin L is held constant at -7.5V and -5V, respectively, by the resistance network consisting of 1.5K, 470Ω, and 1K. When this condition exists, pin D being more positive than pin E will cause a ground level SE output at pin H indicating a select error. When one unit is selected, the resistance of the line which is effectively in parallel with the 180Ω resistor, results in a voltage at pin K which is between the constant voltage at pin D of -7.5V and pin E of -5V. This voltage condition prevents the difference amplifiers from conducting, and the output at pin H and N will be -3V indicating a no-error condition. If more than one unit is selected on the line, the resistance in parallel with the 180Ω resistor will be decreased resulting in a voltage at pin K more positive than the -5V at pin L and the difference amplifier will conduct, resulting in a ground SE output at pin N.

3.10 STATUS FUNCTIONS (Dwg TD10A-0-ST)

The error, status, and illegal operations of the TD10A control are monitored by the processor CONI DTS instruction which gates the requested status condition to the I/O bus. The following paragraph lists each condition and the related inputs.

3.10.1 Parity Error

A parity error status is indicated by any of the conditions which caused the ERR MK TRK (1) level and by a longitudinal parity error detection. The ~LP=1 level allows the TP1 pulse, which immediately follows the first 6 bits of the forward checksum area on tape, to set the ST PAR ERR flip-flop. The status of the flip-flop is gated with the ENB PAR ERR (1) level (Dwg TD10A-0-COM1) producing a COM FLAGS REQ level. The COM FLAGS REQ level enables the priority interrupt assignment on the flag channel.

3.10.2 Job Done

The ST JOB DONE flip-flop is used to terminate a current read or write function at a predetermined time when a data miss occurs or when requested by program. During read block number or data function, if the ENB FCN STOP (1) level occurs between blocks, the T ACT (0) level allows the TP1 pulse to immediately set the ST JOB DONE flip-flop and prevent the next block from being read. If the ENB FCN STOP (1) level occurs during a block, the entire block is read and the parity check is performed before the T ACT (0) transition will allow the ST JOB DONE flip-flop to be set.

During a write block number or data function, if the ENB FCN STOP (1) level occurs when the tape is between blocks, the ST JOB DONE flip-flop will not be set until a DC DATA REQ (1) level is generated. This insures that the last word of data received from the processor will be written. If the DC DATA REQ(1) level occurs with ENB FCN STOP(1) during a block, the last data word will be written repeatedly until the end of the block is reached, at which time the correct parity is written and the T ACT (0) transition sets the ST JOB DONE flip-flop to terminate the current operation. The ST JOB DONE (1) output gated with ENB JOB DONE (1) level (Dwg TD10A-0-COM1), when requested, will cause an interrupt on the flag channel.

3.10.3 Illegal Operation

An illegal operation is indicated by any of the conditions that cause an ERR SW level, as described in Paragraph 3.7. The ST ILL OP flip-flop will be collector-set after the T WAIT delay and at the T DATA STROBE pulse time if an ERR SW level occurs due to the operator moving the wrong switch. The ST ILL OP (1) output, gated with the ENB ILL OP (1) level, when requested, will cause an interrupt on the flag channel. Writing cannot begin if the ERR SW level is present at the start of the operation.

3.10.4 End Zone

The ST END ZONE flip-flop is set at TP0 time, enabled by the decoded MK END ZONE level, when the tape reaches the end zone associated with its direction of motion. The ST END ZONE(1) level clears the COM GO flip-flop (Dwg TD10A-0-COM1) and, gated with ENB END ZONE(1) level, causes an interrupt on the flag channel.

3.10.5 Block Missed

The ST BLK MISS flip-flop is set if a CONO DTC instruction to read or write data occurs after the ENB BNR flip-flop is reset. The ENB BNR flip-flop is set during a read block number function and reset by the T REV CKS level; therefore, the command to read or write must occur after the time the block number is read or written, but before the start of the data section of a block or a block-miss error

will be indicated. The ST BLK MISS (1) output is gated with the ENB BLK MISS (1) level (Dwg TD10A-0-COM1), where requested, to cause an interrupt on the flag channel and with IOB DTS STATUS(B) level to provide a status indication to the processor.

3.10.6 Incomplete Block

The ST INC BLOCK flip-flop is set to indicate that a partial block of data has been read or written.

During read operations, if an ENB FCN STOP (1) level occurs during a data block, the DC CT (0) level sets the ST INC BLOCK flip-flop. The ST INC BLOCK flip-flop will also be set if a data request has been initiated but not answered prior to the ENB FCN STOP (1) transition, or if a T DATA STROBE pulse occurs when ENB FCN STOP is a 1.

During writing, the ST INC BLOCK flip-flop is set when a T DATA STROBE pulse occurs when ENB FCN STOP is (1) and no new data is present to be written.

CHAPTER 4
MAINTENANCE

This section includes the general information required to service the TD10A DECtape Control. Specific maintenance programs which utilize the maintenance features incorporated in the control are listed. The control panel and associated indicator functions which can be used effectively during trouble shooting procedures are described in Chapter 2 of this manual. The maintenance procedures required for the TU55 DECtape Transports are contained in the TU55 DECtape instruction Manual (H-TU 55).

4.1 MAINTENANCE EQUIPMENT

Table 4-1 is a list of the equipment recommended for servicing the TD10 control in addition to the standard hand tools normally required.

Table 4-1
Maintenance Equipment

Equipment	Manufacturer	
Multimeter	Triplett or Simpson	630-MA or 260
Oscilloscope	Tektronix	Series 540 or 580, with Type CA differential amplifier
Head Cleaner Kit (8705)	Potter	P/N A 425 484

4.2 DEC MODULES

Table 4-2 lists the module types and the number required for the TD10A DECtape Control. The schematic diagrams for the standard module types are included in this section. The standard DEC modules used in this device are described in the Digital Logic Handbook (C105), and the PDP-10 Special System modules are described in PDP-10 Central Processor Maintenance Manual, Volume III. One spare module of each type is generally recommended to facilitate maintenance of the TD10A control.

The position of the modules within the mounting panels, as viewed from the wiring side, is shown in Dwg MU-TD10A-0-2 (Sheets 1 and 2). In this drawing, each module is represented by a rectangle with the module type designation at the top. Each rectangle in turn is subdivided to show the circuits that are contained on the module. In general, the circuits are identified by the logic signal(s) available at the circuit outputs.

Table 4-2
Module Complement

No. Req'd	Type	Description
2	B152	Binary to Octal Decoder
2	B156	Diode Gate
17	B163	Diode Gate
1	B212	Triple Flip-Flop
2	B685	Diode Gate Driver
2	G705	DECtape Jumper
1	G706	DECtape Attenuator
1	G853	Motion and Selection Crt
5	G882	Manchester Read/Write Amplifier
18	R002	Diode Network
12	R107	Inverter
13	R111	Diode Gate
8	R113	Diode Gate
9	R141	Diode Gate
1	R151	Octal Decoder
9	R201	Flip-Flop
23	R202	Dual Flip-Flop
8	R203	Triple Flip-Flop
26	R205	Dual Flip-Flop
3	R302	Delay (One Shot)
4	R303	Integrating One Shot
1	R401	Clock
9	R602	Pulse Amplifier
11	R602	Pulse Amplifier
1	W005	Clamped Load
4	W012	Indicator Cable Connector
1	W023	Connector Board
2	W032	DECtape Signal Connector
2	W033	Cable Connector
6	W107	I/O Bus Receiver

Table 4-2 (Cont)
Module Complement

No. Req'd	Type	Description
4	W250	Indicator Cable Connector
1	W520	Comparator
1	W532	Difference Amplifier
1	W533	Rectifying Slicer
1	W808	Relay
8	W851	I/O Connector
4	W250	Indicator Cable Connector

Location J of the mounting panel (Dwg TD10A-0-2) has connectors prewired and reserved for modules used with the XY10 Plotter option. Refer to the note on the drawing for information pertaining to the module locations of the XY10 Plotter.

4.2.1 Module Type 882

The Manchester Reader/Writer, G882, is a standard size FLIP-CHIP module for use in reading and writing one channel of the DECtape TU55. Each module contains a write amplifier and a high-gain differential read amplifier. The read amplifier saturates with an input of 1 mV.

The terminals for the module are shown in Figure 4-4. The input and output characteristics are as follows.

Reader Inputs E, D are differential signals centered at ground. The input impedance is approximately 400 ohms to ground. A nominal input signal is a sine wave between 5 kc and 30 kc.

Reader Outputs U,V are standard DEC levels of -3V and ground. The outputs can drive 10 mA of load at ground.

Writer Inputs N, R, and P are standard DEC levels of -3V and ground. The input load of 2 mA is shared by the inputs at ground level.

Writer Outputs J and K are nominal 180-mA current pulses from the ground to -15V.

The power requirements of the module are +10V (A)/18 mA and -15V (B)/235 mA. The marginal check limits in both cases are ± 20%.

Both the reader and writer circuits are returned to a common C, F ground.

4.2.2 Module Replacement Procedure

When it is necessary to remove modules, use the following procedure.

a. Turn off all power to the Type TD10 DECtape Control. (Allow four seconds for the delayed power turn-off to stop the fans.)

b. Gently pull the module from the mounting panel. Use a straight even pull to avoid damage to plug connections and the printed-wiring board.

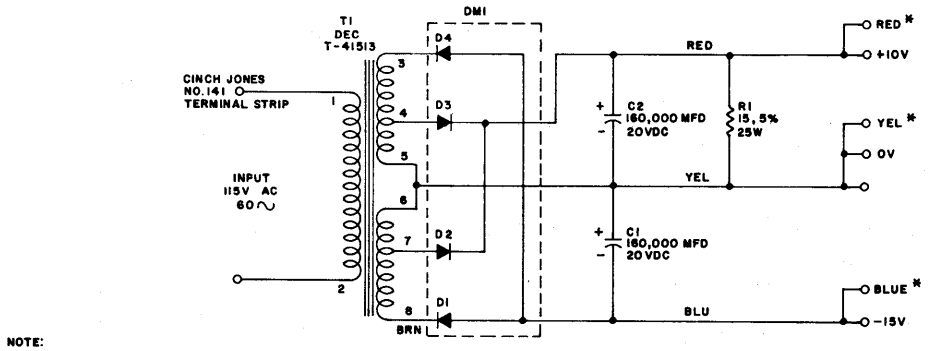
Access to signal tracing points is provided from the wiring side of the mounting panel.

4.3 POWER SUPPLIES AND POWER CONTROL PANEL

Two type 728 or 728A power supplies shown schematically on Figures 4-1 and 4-2 respectively, provide +10.0 Vdc and -15.0 Vdc power to the TD10A logic modules and a maximum number of eight TU55 DECtape Transports. The type 728 supply is used for 60 cycle ac power and the type 728A for 50 cycle ac power. The ac power is supplied to the type 844 Power Control Panel (Figure 4-3) from an extension cord with a 30A, 3-wire Hubbell Twist Lock plug at each end. The KA10 Processor provides an ac remote turn-on signal to the Type 844 Power Control which distributes and controls the ac power to both the TU55 Transports and power supplies. Refer to Dwg TD10A-0-4 for the ac and dc power distribution and wiring.

4.3.1 Power Supply Checks

The use of a multimeter permits output voltage measurements to be made on the power supply without disconnecting the power supply from the TD10A or TD10B. An oscilloscope should be used to measure the peak-to-peak ripple content of each dc output voltage. Because the power supply is not adjustable, a unit that does not meet the following tolerances should be considered defective and steps should be taken to correct the deficiency. Refer to the Digital Logic Handbook (C105) for the general specifications for the type 728 and 728A power supplies.



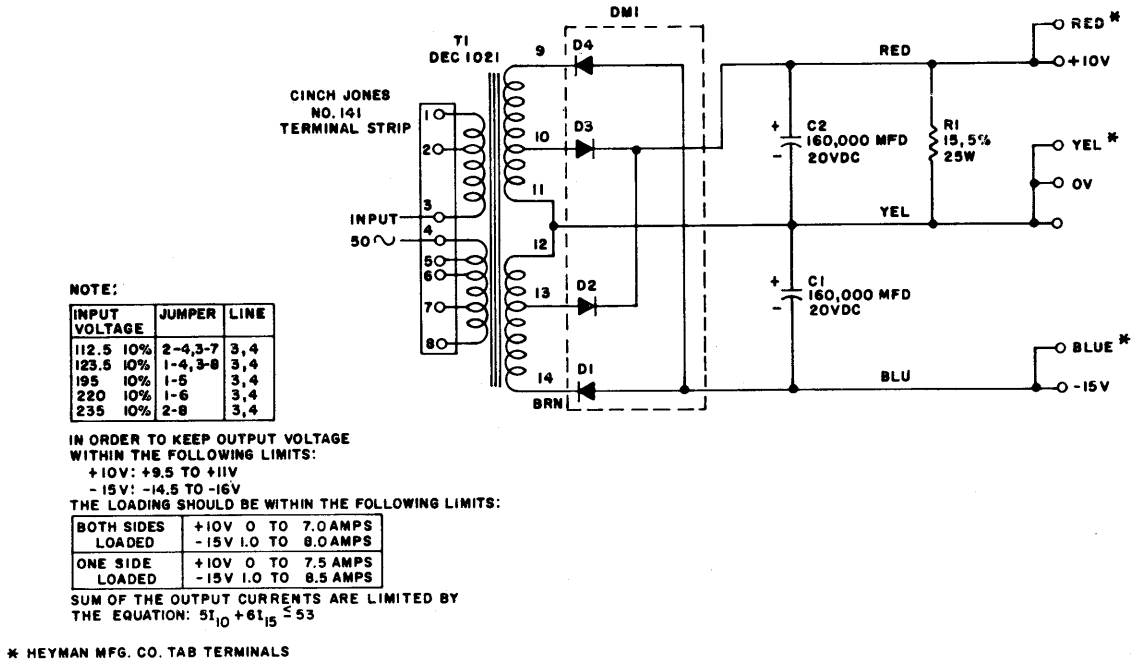
NOTE:
IN ORDER TO KEEP OUTPUT VOLTAGE WITHIN THE FOLLOWING LIMITS:
+10V: +9.5 TO +11V
-15V: -14.5 TO -16V
THE LOADING SHOULD BE WITHIN THE FOLLOWING LIMITS:

BOTH SIDES LOADED	+10V 0 TO 7.0 AMPS -15V 1.0 TO 8.0 AMPS
ONE SIDE LOADED	+10V 0 TO 7.5 AMPS -15V 1.0 TO 8.5 AMPS

SUM OF THE OUTPUT CURRENTS ARE LIMITED BY THE EQUATION: $5I_{10} + 6I_{15} \leq 53$

* HEYMAN MFG. CO. TAB TERMINALS

Figure 4-1 Type 728 Power Supply, Schematic Diagram



NOTE:

INPUT VOLTAGE	JUMPER	LINE
112.5 10%	2-4,3-7	3,4
123.5 10%	1-4,3-8	3,4
195 10%	1-5	3,4
220 10%	1-6	3,4
235 10%	2-8	3,4

IN ORDER TO KEEP OUTPUT VOLTAGE WITHIN THE FOLLOWING LIMITS:
+10V: +9.5 TO +11V
-15V: -14.5 TO -16V
THE LOADING SHOULD BE WITHIN THE FOLLOWING LIMITS:

BOTH SIDES LOADED	+10V 0 TO 7.0 AMPS -15V 1.0 TO 8.0 AMPS
ONE SIDE LOADED	+10V 0 TO 7.5 AMPS -15V 1.0 TO 8.5 AMPS

SUM OF THE OUTPUT CURRENTS ARE LIMITED BY THE EQUATION: $5I_{10} + 6I_{15} \leq 53$

* HEYMAN MFG. CO. TAB TERMINALS

Figure 4-2 Type 728A Power Supply, Schematic Diagram

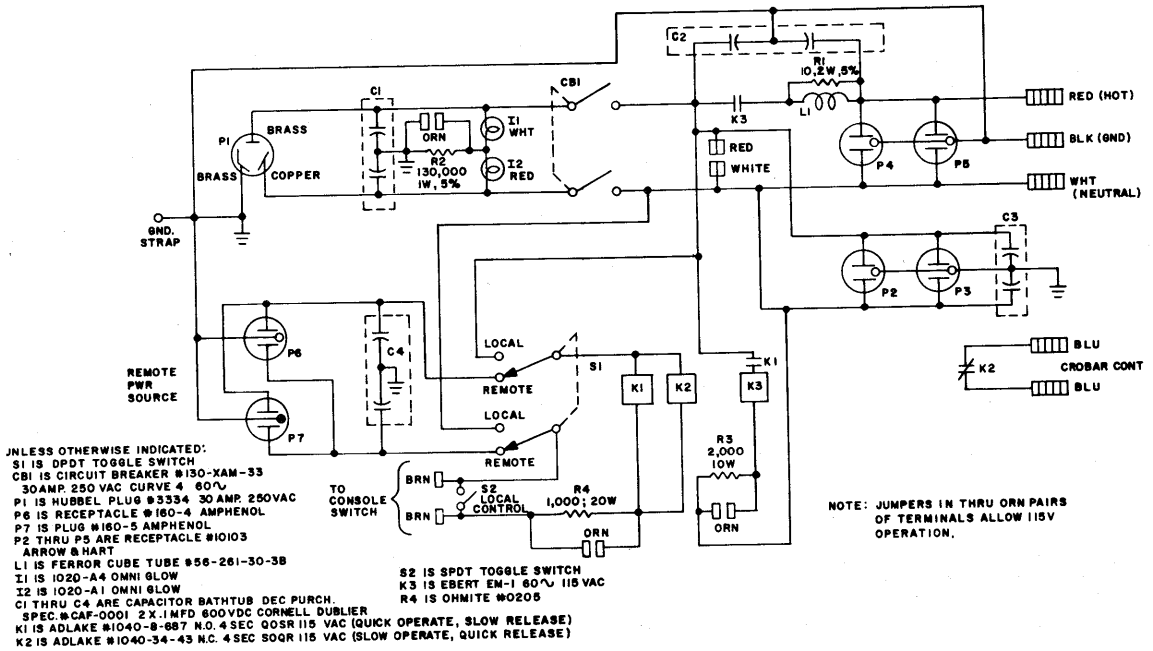


Figure 4-3 Type 844 Power Control, Schematic Diagram

4.4 PREVENTIVE MAINTENANCE

Preventive maintenance consists of procedures that are performed prior to the initial operation of the equipment and periodically during its operating life. These procedures include visual inspections, cleaning, mechanical checks, and circuit element checks. Marginal checks are also conducted when considered necessary to aggravate border-line conditions or intermittent failures so that they can be detected and corrected. A log book should be available for recording specific data which indicates the rate of performance and deterioration and to provide information for determining when components should be replaced.

Except for marginal checks all preventive maintenance procedures should be performed once a month or every 200 operating hours, whichever occurs first.

4.4.1 Mechanical Checks

The following mechanical checks should reveal any substandard conditions in the mechanical operation of the control unit.

a. Clean the exterior and the interior of the control by means of a vacuum cleaner or by using clean cloths moistened in a nonflammable solvent.

b. Clean the air filter at the bottom of each cabinet. Remove the filter by removing the fan and housing which are held in place by two knurled and slotted screws. Wash the filter in soapy water, dry in an oven or by spraying with compressed gas, and spray with Filter-kote (Research Products Corp., 1015 E. Washington Avenue, Wisconsin, 53703).

c. Lubricate door hinges and casters with a light machine oil. Wipe off excess oil.

d. Visually inspect the TD10A and/or TD10B for completeness and general condition.

e. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Repair or replace any defective wiring.

f. Inspect switches, controls, knobs, jacks, connectors, transformers, fans, capacitors, lamp assemblies, etc. Tighten or replace as required.

g. Inspect switches for binding, scraping, misalignment, and positive action. Adjust, align or replace as necessary.

h. Inspect all racks of logic to assure that each module is securely seated in its connector.

i. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors exhibiting these signs of malfunction.

4.4.2 Marginal Voltage Checks

Marginal checks are performed to aggravate borderline circuit conditions within the control logic and thus produce observable faults. By recording the bias voltage levels at which circuits fail, progressive deterioration can be plotted and expected failure rates can be predicted. This procedure provides a means for planned replacement. Marginal checks are also useful as a troubleshooting aid to locate marginal or intermittent components (e.g., deteriorating transistors).

Marginal checks are performed by operating the logic circuits from an adjustable external power supply located in the KA10 Processor Unit. Raising the bias level above +10V increases the transistor cutoff required to be overcome by the preceding transistor, thus causing a below-par transistor to fail. Lowering the bias level below +10V reduces the transistor base bias and noise rejection. This procedure provides detection of high-leakage transistors and simulates high-temperature conditions for checking thermal runaway. Raising and lowering the -15V supply has little effect on the logic circuits because the collector load voltage and most modules is clamped at -3V. It does, however, increase and decrease the output pulse amplitude of the pulse amplifier circuits (e.g., the delay circuit) and then provides a sensitivity check of the circuits which follow.

CAUTION

Increasing the -15V power to a value more negative than -18V will cause damage within the logic circuits.

The switches used for conducting marginal checks of the TD10A DECtape Control are located at the left-hand side of the wired panel assembly. When switched on (up), switches 1A through 1F and 1H and 1J apply power from the marginal check bus; when switched off (down), normal power is applied. The "up" position of the top switch on each panel selects the marginal check voltage of +10V. The "down" position selects the fixed voltage of +10V. The lower switch of each panel performs the same function with the -15V.

A color-coded connector on the right side of each panel connects the normal and marginal operating voltages to the marginal check panel. The normal and marginal power buses are common to all panels. The normal power bus is connected to the Type 728 or 728A Power Supply, and the marginal power bus is connected to the marginal check power supply on the KA10 Processor.

The following margin specs are for regular margin checking for each test.

Tape Rocker Mode

Margin all racks (one at a time) to:

a. +10V ± 7.5V except racks A and B = +10V ± 2.0V

b. -15V ± 3.0V

Diagnostics, Control Tests 1, 2, 3 and 4

Margin all racks (one at a time) to:

a. +10V ± 7.5V except

Rack B = +10V ± 5.0V
Rack H = lower limit +6.0V
upper limit +16.0V

b. -15V ± 3.0V

A marginal check is performed as follows.

a. Set the MARGIN CHECK switch on the KA10 maintenance panel to +10R and adjust the power supply output for 10V.

b. Start DECtape operation in a normal program or in a routine which fully utilizes the circuits in the rack to be tested. If no suitable program is available in the normal system application, select an appropriate maintenance routine. The maintenance programs provide basic exercises of specific functions and scope loops for these functions as well as a routine which redundantly exercises all functions.

c. Set the top normal/marginal check switch on the panel to be tested to its "up" position. This action usually causes an interruption to the normal system operation.

d. Decrease the maringal-check power supply output voltage until normal system operation is interrupted. Record the marginal-check voltage. If desired, locate and replace the marginal transistors at this time.

e. Restart DECtape operation and increase the marginal-check power supply output voltage until normal operation is interrupted. Record the marginal-check voltage. If desired, locate and replace the marginal transistors at this time.

f. Set the top normal/marginal check switch in step c to its "down" position. (See "results" in step c.)

g. Repeat steps a through f for the center normal/marginal switch on the panel being tested.

h. Set the MARGIN CHECK switch on the KA10 Maintenance Panel to -15R, and adjust the power supply output for -15V.

i. Repeat step b.

j. Set the bottom normal/marginal switch on the panel being tested to its "up" position.

k. Repeat steps d and e and then return the bottom normal/marginal switch to its "down" position.

l. Adjust the output of the marginal-check power supply to 0V and set the selector switch to its "off" position.

4.4.3 Delay Adjustment Procedure

The adjustment procedure for the various delays in the TD10A are as follows.

Set the instruction CONO 0, 200000 into the data switches on the KA10 console. Turn the REPEAT switch on. Hit the EXECUTE switch. This procedure causes the KA10 to generate a series of I/O RESET pulses at a repetition rate controlled by the SPEED CONTROL knobs on the KA10. The I/O RESET pulses trigger the following delays which can now be adjusted with the aid of an oscilloscope. Be sure the time between I/O RESET pulses is greater than the length of delay to be achieved.

Delay	Location	
T SPEED	B23	120 ms
T RELAY	B22	1 ms
TURN ARND DLY	C32	200 ms
T UPS0	A22	66 μs

The TP delay D21 (Dwg TD10A-0-T1) is adjusted with the aid of Tape Rocker mode to 10 μs.

NOTE

All 1 μs delays are not adjustable.

4.5 MAINTENANCE LOGIC (Dwg TD10A-0-MNT)

The TD10A Control includes maintenance logic which allows maintenance programs to be run to simulate actual operation of a TU55 transport. The maintenance information is transferred from the processor to the TD10A under program control through the I/O Bus using DATAO DTS commands. The status of the LP buffer, RWB, and mark track decoder are monitored by the processor using a DATAI DTS command. Figure 4-4 shows the bit consignment for the maintenance information.

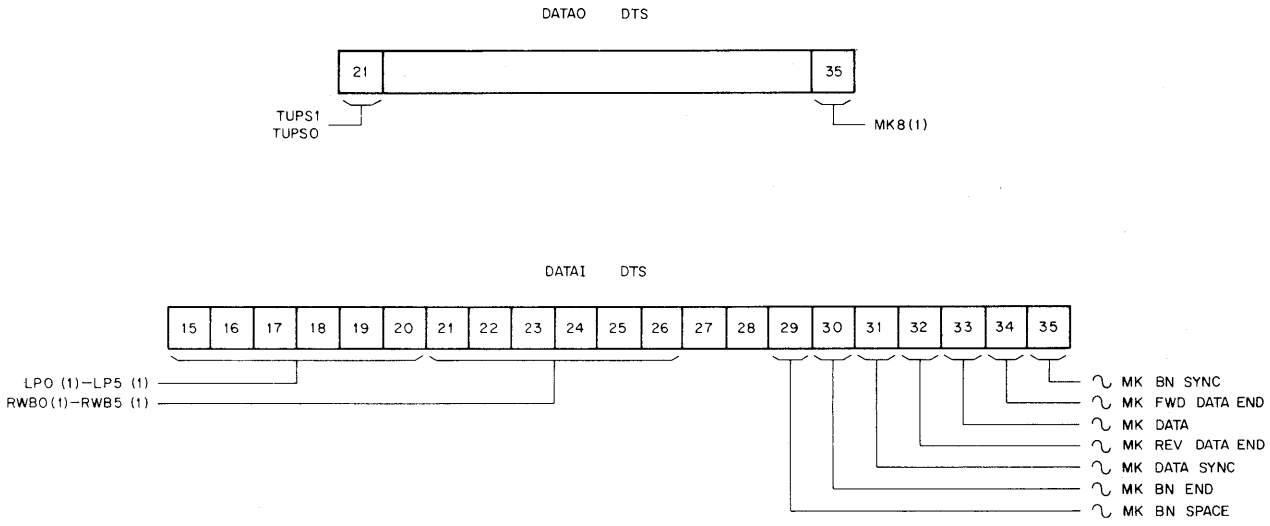


Figure 4-4 Maintenance Information Format

In addition the IOB DATA SET pulse and IOB DATA CLR pulse under a DTS command are used to simulate the TP0 and TP1 pulses on Dwg TD10A-0-MNT. The MAINT DATA CLR and MAINT DATA SET pulses are inputs to PA R602 (Dwg TD10A-0-T1) to produce the TP0 and TP1 pulses. The MAINT DATAO SET pulse also strobes the information in IOB 35 (B) of the data word into MK8 of the mark track register (Dwg TD10A-0-MK).

During a DATAI command, IOB DATAI level is gated with the IOB SEL DTS level to produce the MAINT DATAI(A) and (B) levels which are used to gate the LP buffer, RWB, and decoded mark track information to the I/O Bus.

4.6 DIAGNOSTIC ROUTINE

The diagnostic programs available for checking the operation of the TD10A DECtape Control and TU55 Transports are listed in the following paragraphs together with a brief description of their functional operation. These programs can be run independently or together with the marginal voltage checks previously described.

4.6.1 TD10A Control Unit Test 1 (MAINDEC-10-D3A0-D)

This program tests the major elements of the data control logic without the actual use of tape on the TU55 Transport. In addition the mark track decoders are tested. Error indicators are printed out upon request.

4.6.2 TD10A Control Unit Test 2 (MAINDEC-10-D3BA-D)

This program provides a final check on the control logic by testing data transfer, timing, and counter operation without tape motion. All modes, except for Write Timing and Mark Track are cycled during program operation.

4.6.3 TD10A Control Unit Test 3 (MAINDEC-10-D3CA-D)

This program tests the ability of the control unit to read and write data blocks of varying data patterns without the actual use of tape on the transport.

4.6.4 TD10A Control Unit Test 4 (MAINDEC-10-D3DA-D)

This program is used to certify the tape by prerecording timing and mark track information and verifying the tape operation.

4.7 MODULE SCHEMATICS

The following schematics are of the standard DEC modules listed in the Digital Logic Handbook (C105).

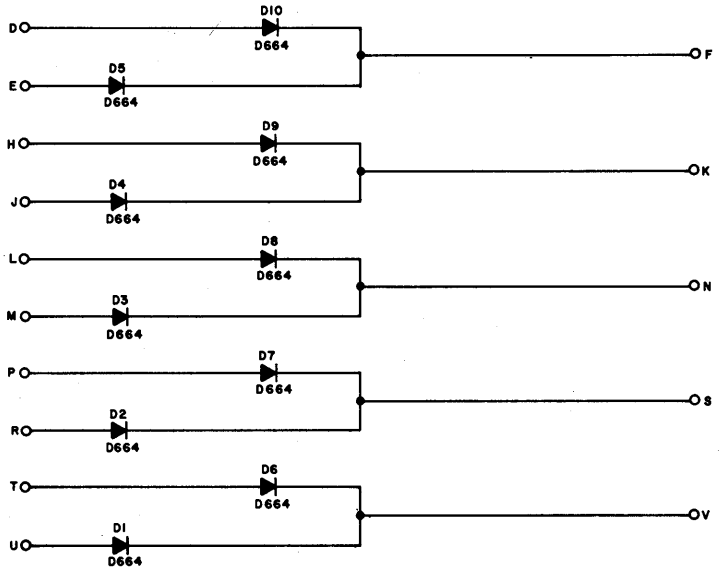
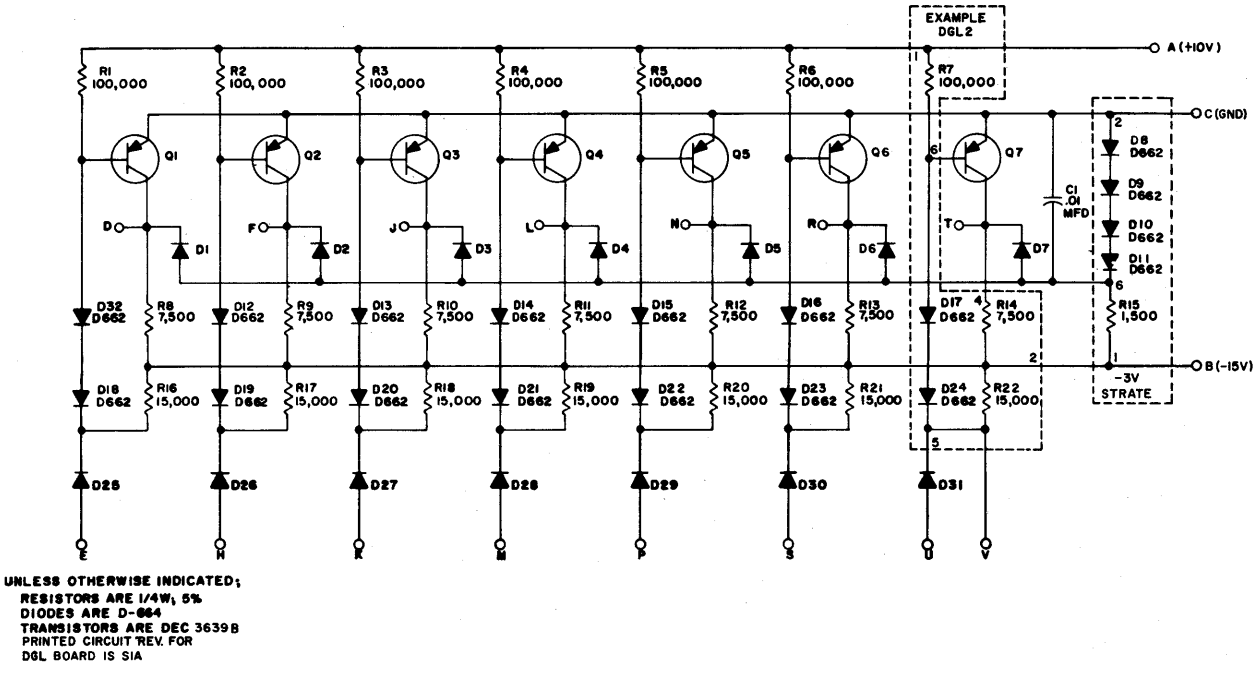
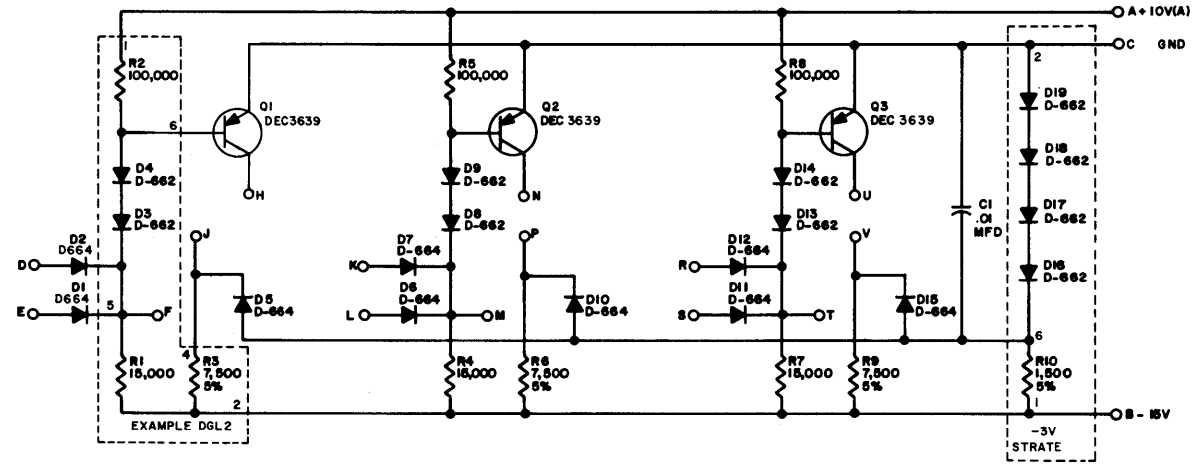


Figure 4-5 Diode Network, Type R002



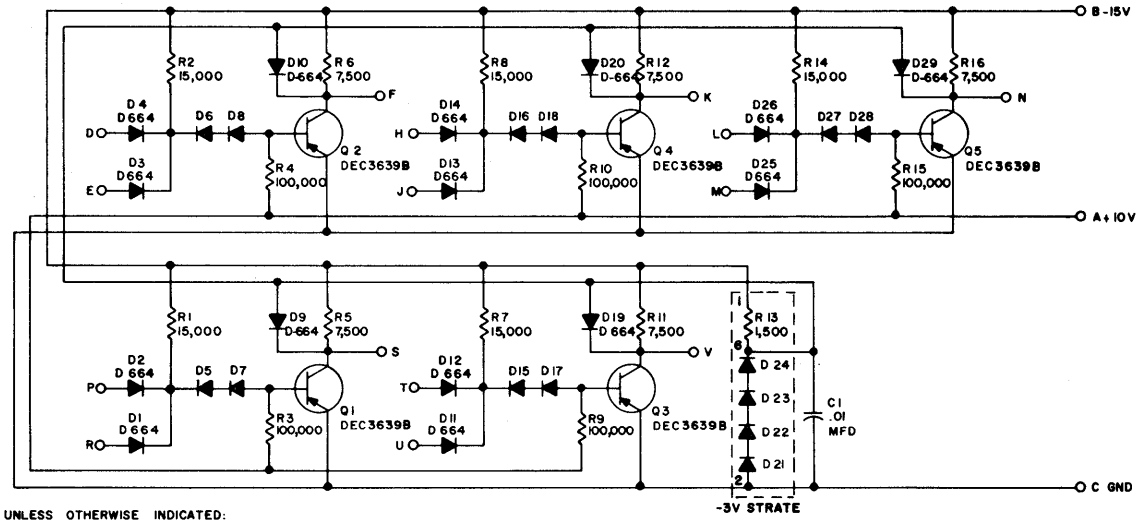
UNLESS OTHERWISE INDICATED;
RESISTORS ARE 1/4W, 5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639B
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIA

Figure 4-6 Inverter, Type R107



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIB

Figure 4-7 Diode Gate, Type R111



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 5%
DIODES ARE D 662

Figure 4-8 Diode Gate, Type R113

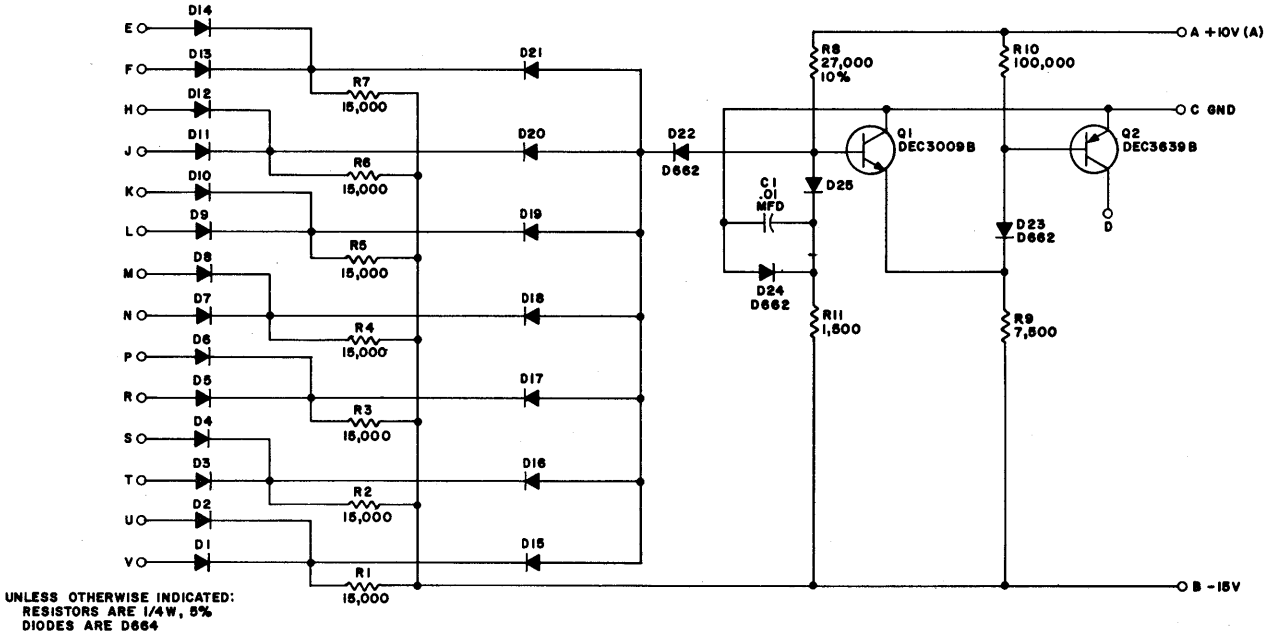


Figure 4-9 Diode Gate, Type R141

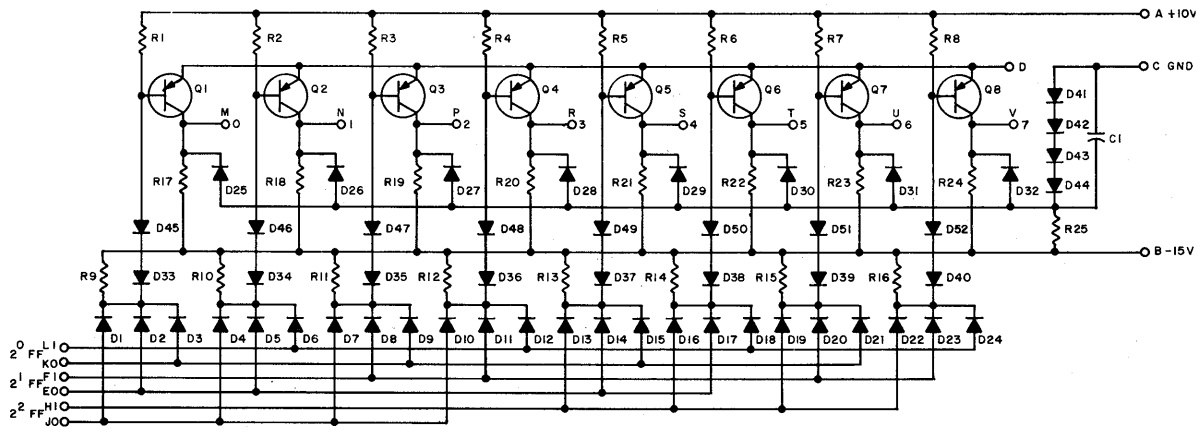
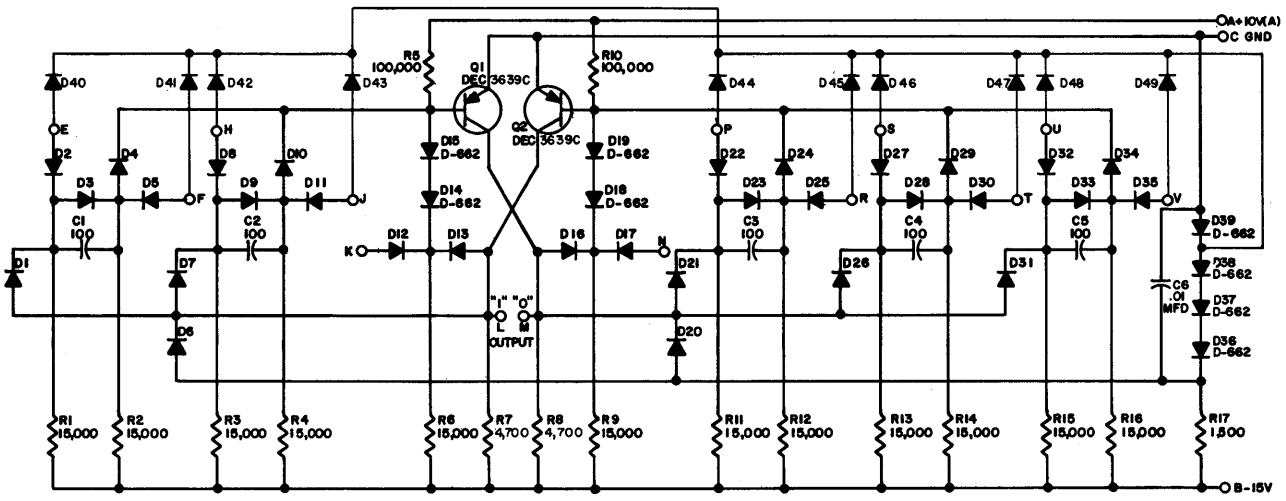
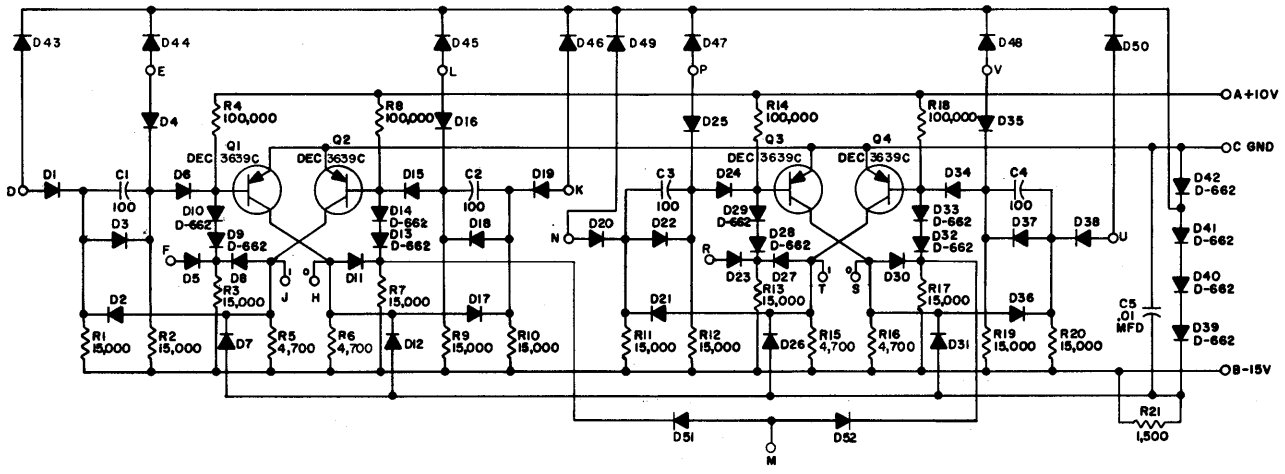


Figure 4-10 Octal Decoder, Type R151



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

Figure 4-11 Flip-Flop, Type R201



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

Figure 4-12 Dual Flip-Flop, Type R202

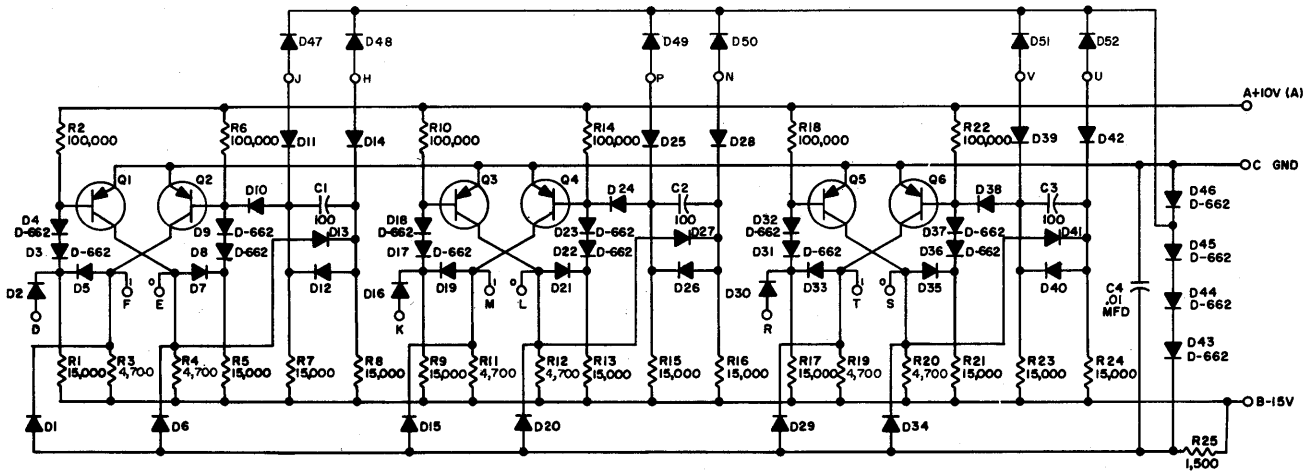


Figure 4-13 Triple Flip-Flop, Type R203

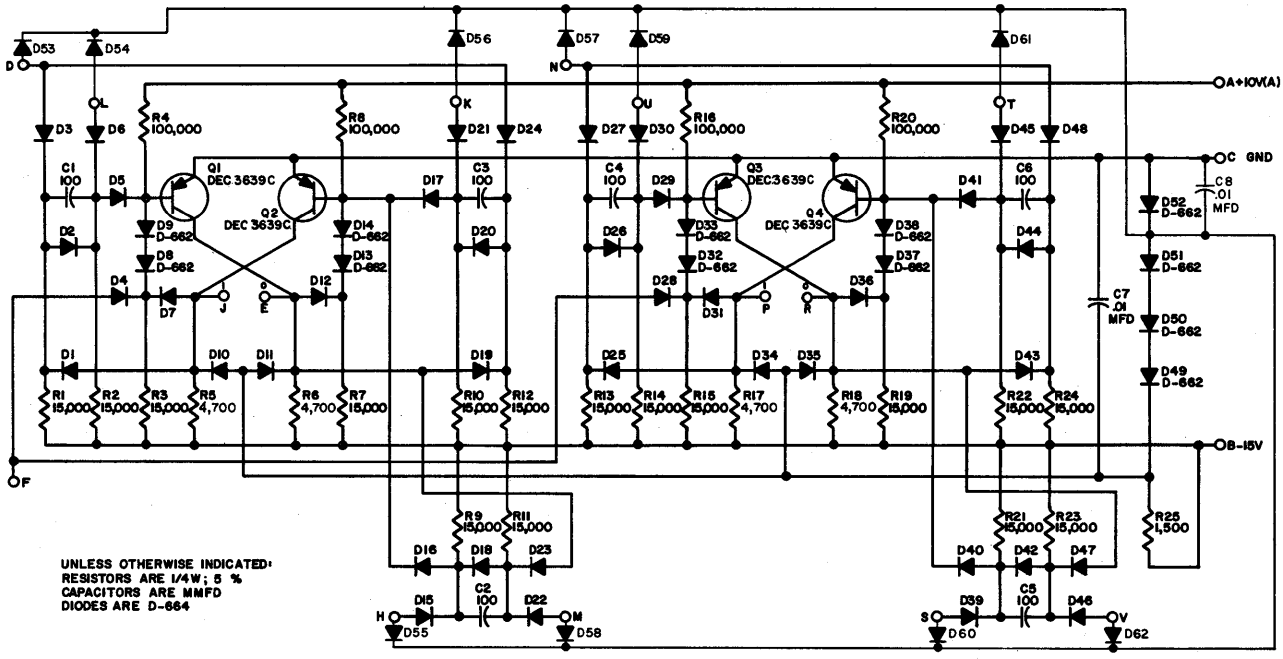
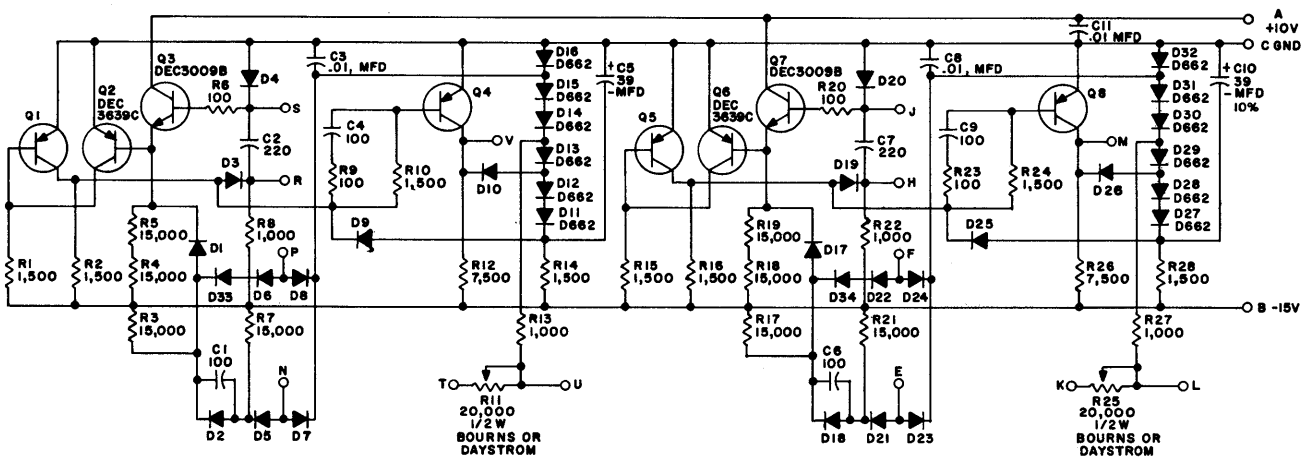


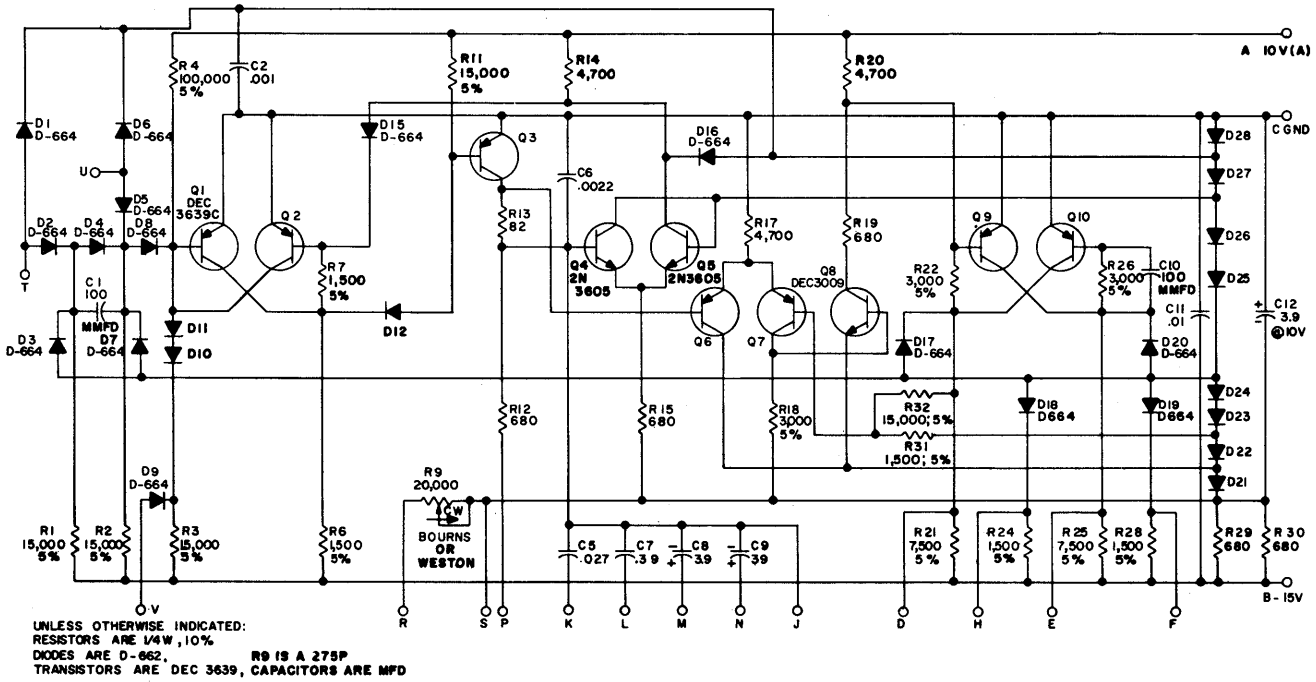
Figure 4-14 Dual Flip-Flop, Type R205



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D664
TRANSISTORS ARE DEC3639

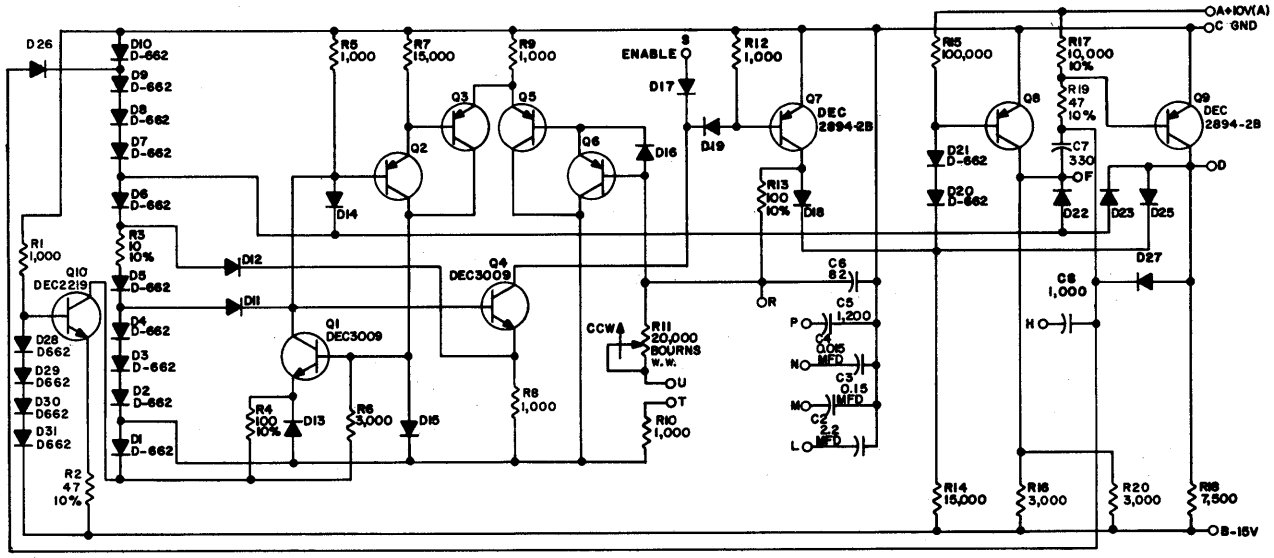
PARTS LIST A-PL-R302-0-0

Figure 4-15 Delay (One Shot), Type R302



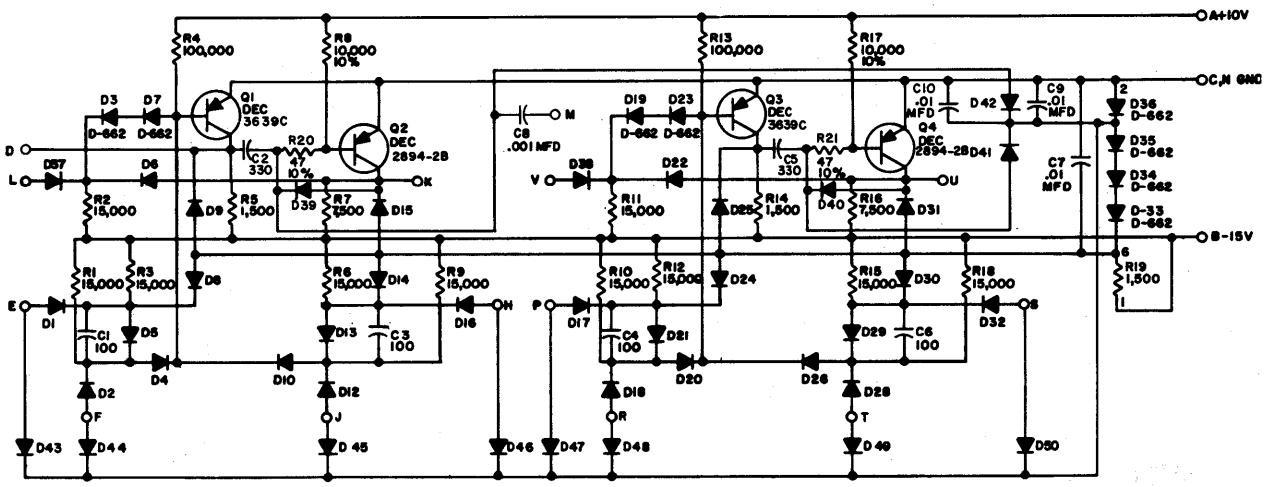
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
DIODES ARE D-662, R9 IS A 275P
TRANSISTORS ARE DEC 3639, CAPACITORS ARE MFD

Figure 4-16 Integrating One Shot, Type R303



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639-0
R11 IS A #275P

Figure 4-17 Clock, Type R401



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

Figure 4-18 Pulse Amplifier, Type R602

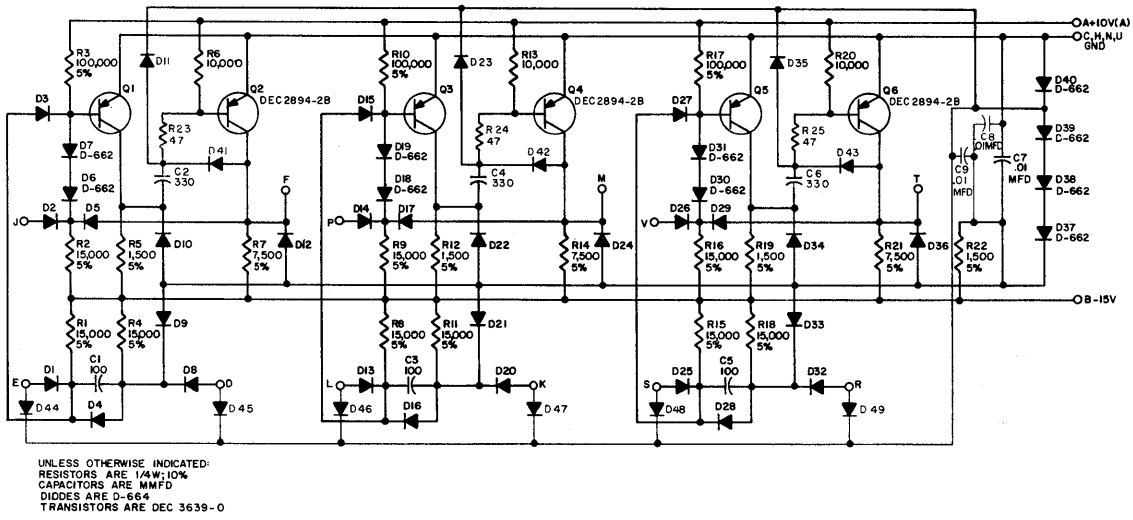


Figure 4-19 Pulse Amplifier, Type R603

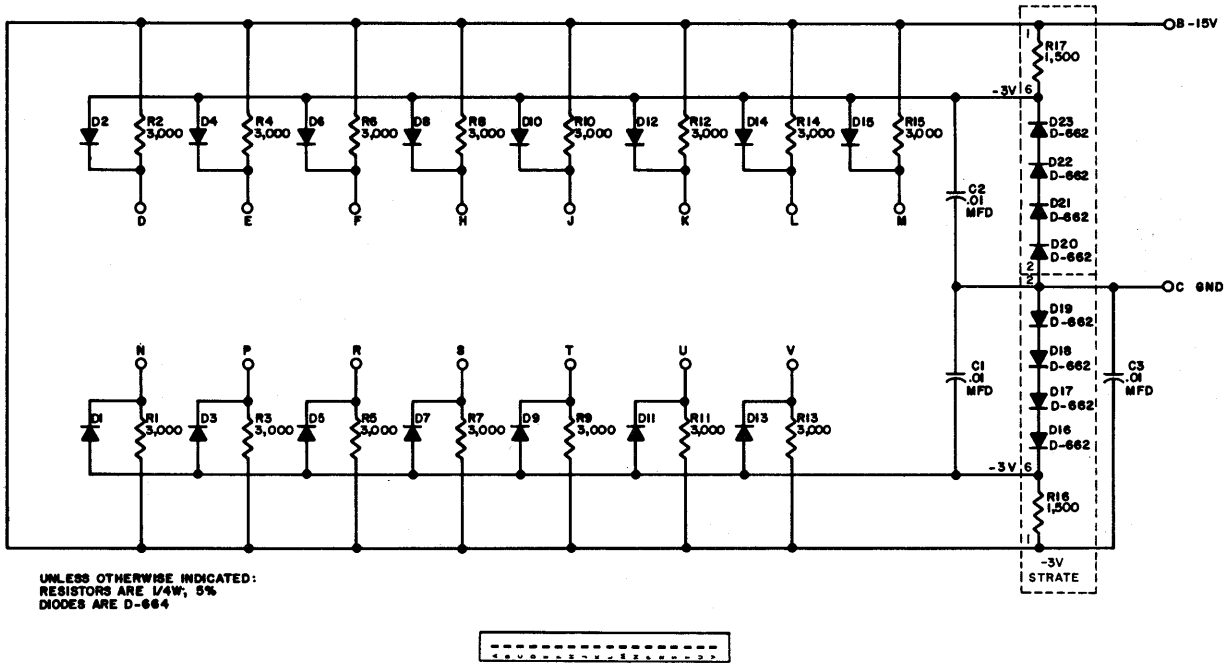


Figure 4-20 Clamped Load, Type W005

To be supplied

Figure 4-21 Connector Board Type W023

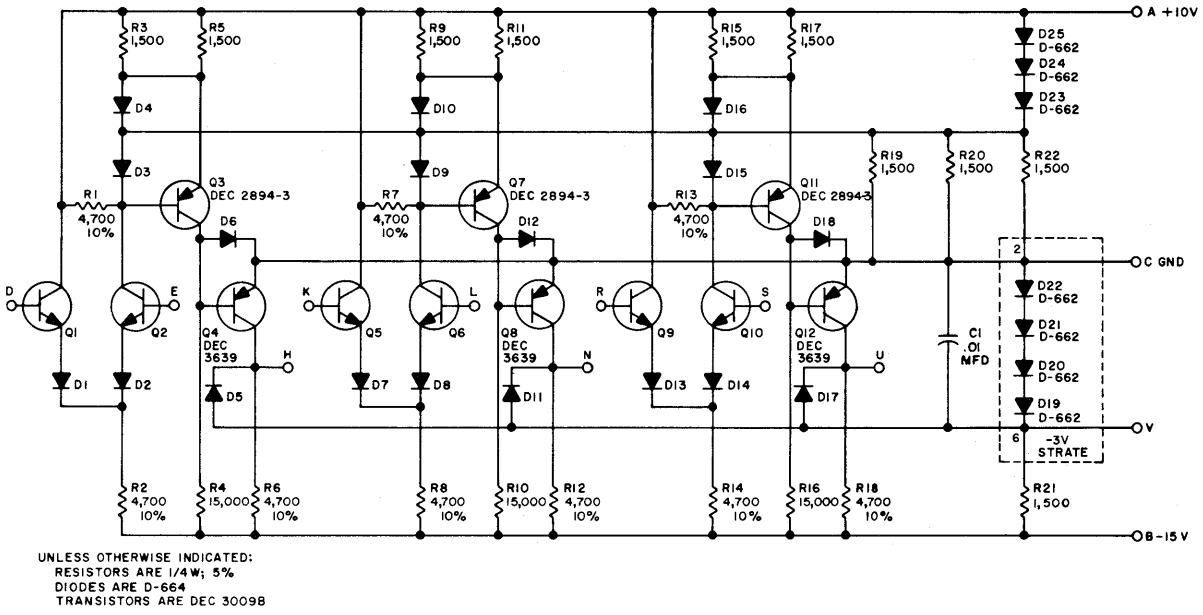
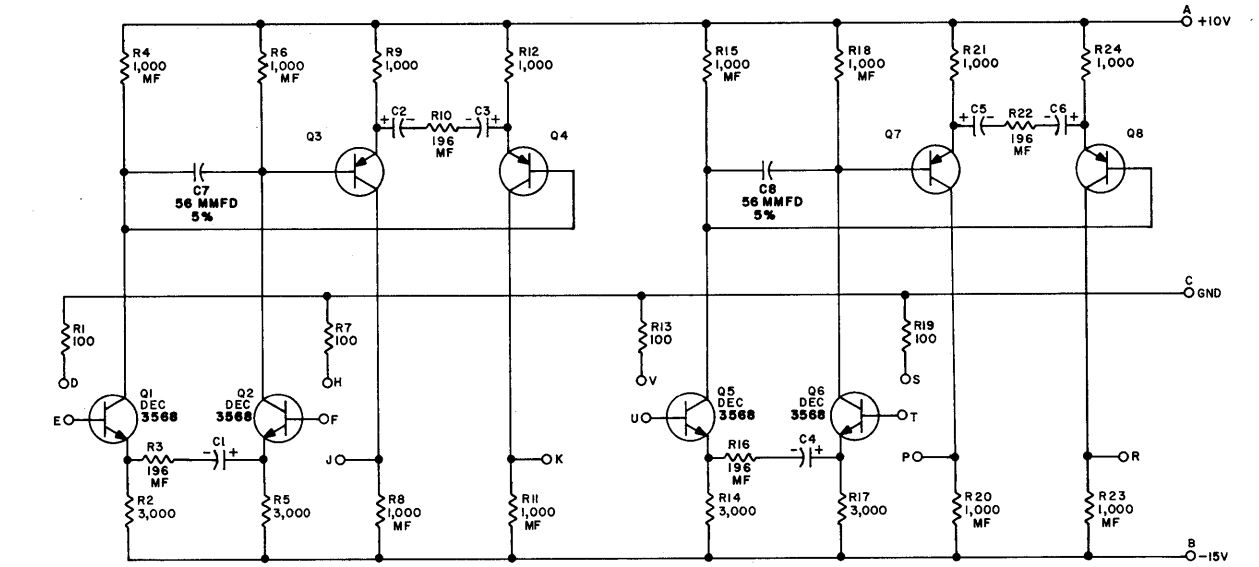
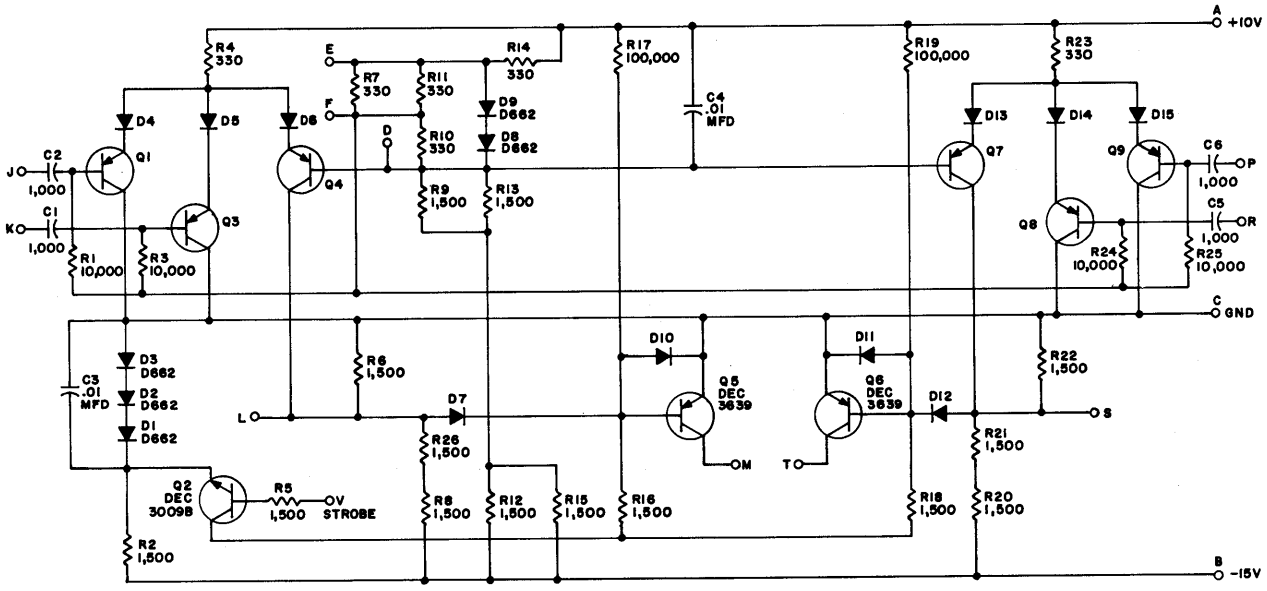


Figure 4-22 Comparator Type W520



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
MF RESISTORS ARE 1/8W; 1% METAL FILM TO
CAPACITORS ARE 3.9 MFD 10% 10V
TRANSISTORS ARE DEC6534C (DEC6534B MAY BE SUBSTITUTED)

Figure 4-23 Difference Amplifier, Type W532



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D664
CAPACITORS ARE MMFD
TRANSISTORS ARE DEC6534D
(DEC6534B MAY BE SUBSTITUTED)

Figure 4-24 Rectifying Slicer, Type W533

CHAPTER 5
INSTALLATION

This section contains the general information on the installation of both the TD10A and TD10B DECtape Control Units. The procedures refer to a single control with a maximum of eight TU55 DECtape Transports. If two control units are required for a PDP-10 System, additional information on installation will be provided.

5.1 SHIPPING

The TD10A and TD10B units are crated and shipped with all the required assemblies mounted and wired. If additional TU55 Transports are requested, each transport is packed, crated and shipped separately, together with hardware and interconnecting cables.

NOTE

Extreme care should be exercised during shipping and receiving to insure against excessive shock or vibration.

5.2 INSTALLATION PROCEDURES

The TD10A and TD10B units can be physically mounted to the right side of KA10 processor or at a remote location limited by the acceptable cable length specified. The following procedures describe both installation configurations.

5.2.1 Site Preparation

No special site preparation is required for the installation of the units. Adequate unit clearance must be provided for proper installation and for servicing. Figure 5-1 shows the installation dimensions required.

When the cabinets are not physically attached to the KA-10 processor, both the power and signal cables enter through holes provided in the base of the cabinet. Adjustable legs mounted on the cabinet base allow the height of the unit to be varied and provide sufficient clearance for the cables. No sub-flooring is normally required.

5.2.2 Environmental Conditions

The environmental conditions for the proper operation of the TD10A and TD10B unit are limited by the magnetic tape used with DECtape transport. The acceptable environmental condition for the magnetic tape are an ambient air temperature between +60°F and +80°F with a relative humidity level between 40% and 60%. The TD10A DECtape Control operating environment is the same as that required by the KA10 processor.

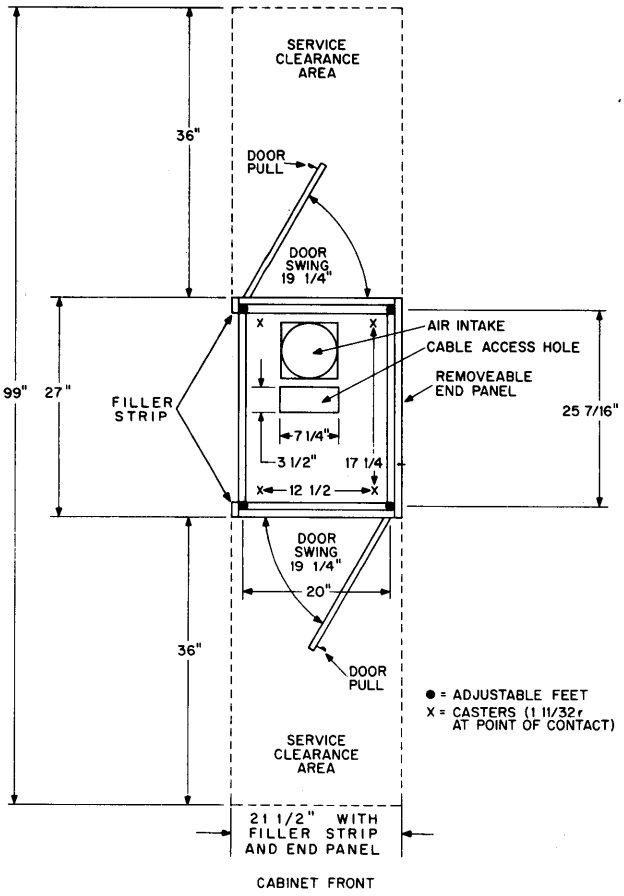


Figure 5-1 TD10A/B Cabinet Clearance Dimensions

5.2.3 Power and Cable Requirements

The TD10A control and associated TU55 Transports operate from single-phase 115V ±10%, 60 Hz ±2 Hz, or from 230V ±10%, 50 Hz ±2 Hz line voltage. The maximum current requirements are dependent on the number of TU55 Transports included in the system. The normal current requirements of the TD10A Control (without transports) is 2.5A and each TU55 requires a normal current of 1.0A. The main ac power is supplied to the TD10 unit by a 3-wire, 30A (single phase) Hubbell Twistlock connector. An earth-ground connection through the power cord is required in addition to the ground bus requirements. Main ac power is supplied from a Hubbell, 3 terminal 220V twistlock flush receptacle, type No. 3330.

The interconnection diagram for the cabling of the TD10 control is shown on Figure 5-2.

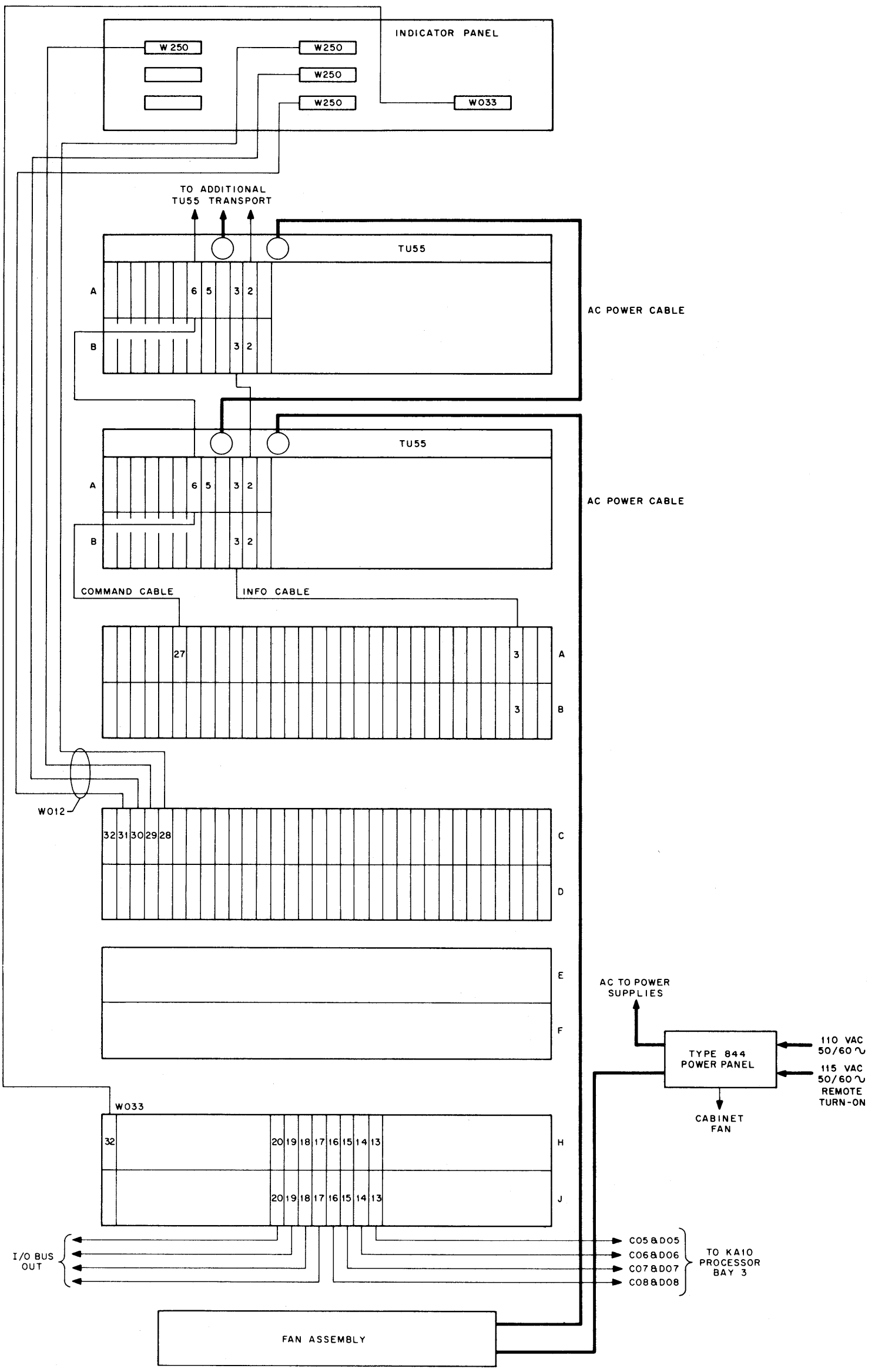


Figure 5-2 TD10A Cable Interconnection Diagram

CHAPTER 6
ENGINEERING DRAWINGS

6.1 INTRODUCTION

This chapter contains a listing of the engineering drawings supplied in the PDP-10 Peripheral Device Engineering Drawings Volume II. These engineering drawings are in addition to the complete set of full-size drawings supplied with each system. Should any discrepancy exist between the drawings in Volume II and those supplied with the equipment, assume the full-size drawings are correct. The full-size drawings should be used by maintenance personnel for work on the equipment because they reflect the variations pertinent to an individual installation. The circuits on these drawings are proprietary in nature and should be treated accordingly.

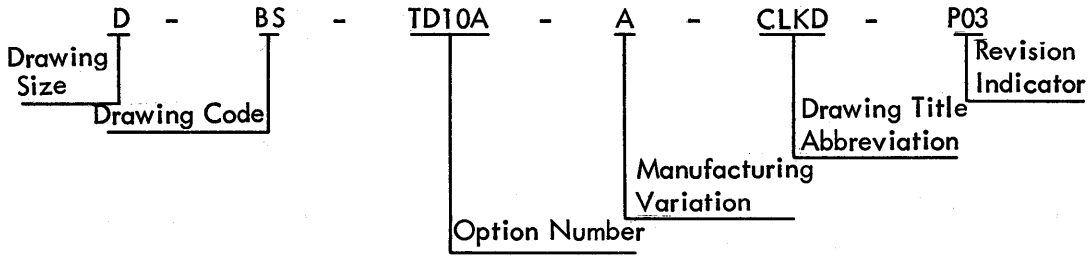
Table 6-1 is a complete list of engineering drawings supplied.

Table 6-1
Drawing List

Drawing No.	Title
TD10A-0-IOB2	I/O Bus Interface Manual Mode No. 2
TD10A-0-ST	Status
TD10A-0-COM1	Command DECtape Control No. 1
TD10A-0-COM2	Command DECtape Control No. 2
TD10A-0-T1	Timing No. 1 (2 sheets)
TD10A-0-T2	Timing No. 2
TD10A-0-RW	Read Write Buffers
TD10A-0-B	Buffer Register
TD10A-0-SH	Shift Register
TD10A-0-MK	Mark Track Decoder
TD10A-0-MNT	Maintenance
TD10A-0-IOB1	I/O Bus Interface Manual Mode No. 1
TD10A-0-ENB	Enable Flip-Flops
TD10A-0-DC	Data Control
TD10A-0-ERR	LP/ERR
TD10A-0-RWA	Read-Write Amplifiers
TD10A-0-2	Module List (2 sheets)

6.2 DRAWING TERMINOLOGY

The engineering drawing numbers contain six fields of information, separated by hyphens. A typical example of a drawing number is shown below.



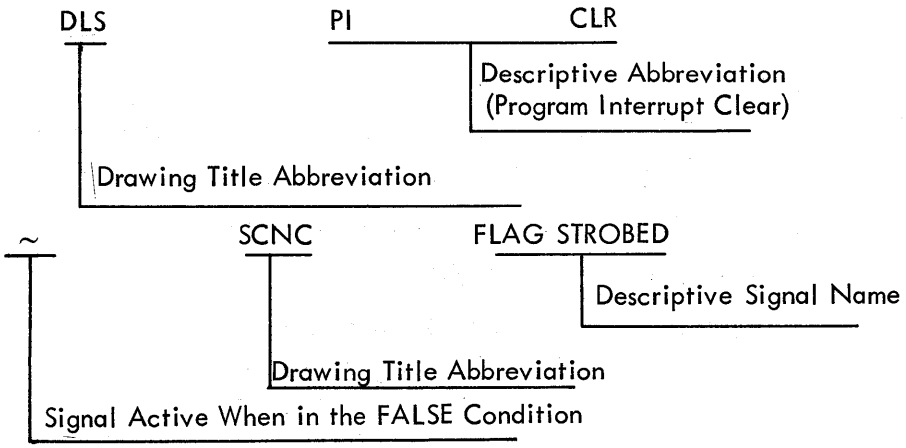
The drawing size, option number, and the drawing title abbreviations are self-explanatory. The manufacturing variation letter identifies the variation that the drawings reflect. For example: 0 reflects a drawing applicable to all variations; A reflects the 60 Hertz equipment; etc. The drawing code identifies the type of drawing. A list of the common drawing codes follows.

BS	Block Schematic or Logic Diagram	MU	Module Utilization
CL	Cable List	RS	Replacement Schematic
CS	Circuit Schematic	SD	System Diagram
FD	Flow Diagram	TD	Timing Diagram
IC	Interconnection Drawing	WD	Wiring Diagram
KS	Key Sheet		

Signal names on the drawings cross reference the signal to the drawing where the signal originates. Two typical examples of signal names are shown below.

Example 1:

Example 2:



6.3 LOGIC SYMBOLS

The DEC standard logic symbols are shown at the input of most circuits to specify enabling condition required to produce a desired output. These symbols represent either standard DEC logic levels or standard DEC pulses. Typical engineering symbols are shown in Figure 6-1.

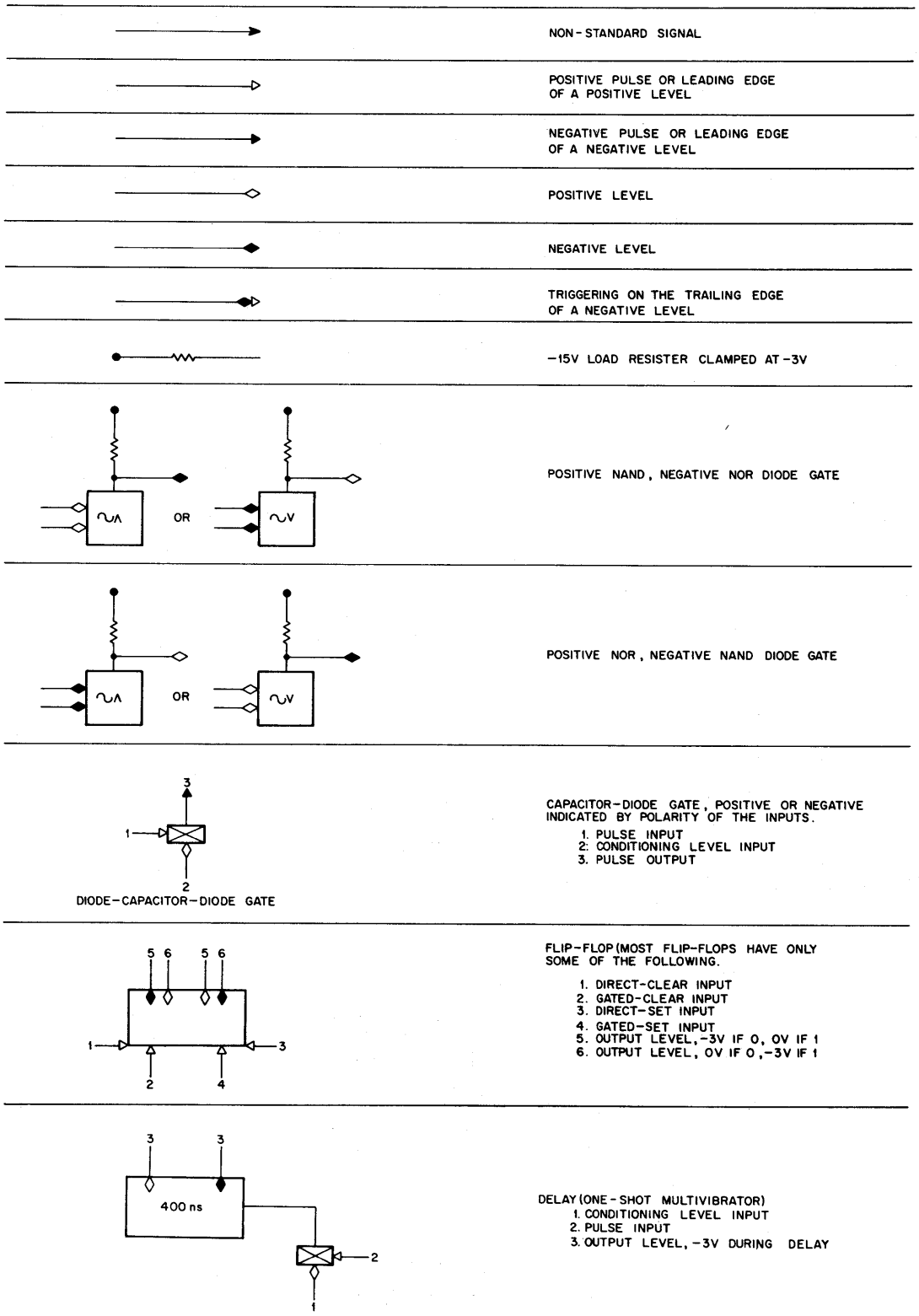


Figure 6-1 DEC Standard Logic Symbols

6.4 LOGIC LEVELS

All logic signals are either standard DEC logic levels or standard DEC pulses. A standard DEC logic level is either a ground (0 to -0.5V) or -3V (-2.5 to -4.0V). Logic signals are generally given mnemonic names which indicate the condition represented by assertion of the signal. An open diamond (—◇) indicates that the signal is a level and that ground represents assertion; a solid diamond (—◆) indicates that the signal is a level and that -3V represents assertion.

All logic levels applied to the conditioning-level inputs of capacitor-diode gates must be present either 100 or 400 ns (depending on the module used) before an input triggering pulse is applied to the gate.

The standard DEC negative pulse is indicated by a solid triangle (—▶) and goes from ground to -2.5 or -3V (-2.5 to -4.0V tolerances). The standard DEC positive pulse, indicated by an open triangle (—▷) goes from -3V to ground. The width of the standard pulses used in this equipment is either 100 or 400 ns, depending on the module and application.

Occasionally, the transition of a level is used at an input where a standard pulse is otherwise expected and a composite symbol (—◆▷) is drawn to indicate this fact. The triangle is drawn open or solid depending, respectively, on whether the positive (-3V to ground) or the negative (ground to -3V) transition triggers circuit action. The shading of the diamond is opposite that of the triangle to indicate triggering on the trailing edge.

Any other signal is nonstandard and is indicated by an arrowhead(—▶)pointing in the direction of signal flow.

6.5 FLIP CHIP PULSES

FLIP CHIP circuit operation in the data line scanner used the DEC R-series pulses. The pulse produced by the R-series modules start at -3V, goes to ground (0.2V) for 100 or 400 ns, then returns to -3V. This pulse is idealized in Figure 6-2.

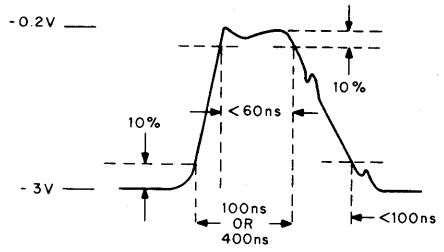


Figure 6-2 R-Series Pulse

Digital Equipment Corporation
Maynard, Massachusetts

digital

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