CORE MEMORY SYSTEM

DR-101

Callier Hearing

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SECTION I

DESCRIPTION

1.0 General

DR-101 is a 650 nanosecond coincident-current, random access, ferrite core memory system. The system has a capacity of 8K words, 20 bits/word on a single printed circuit board assembly. The stack, drive electronics, data register, address register and timing logic are contained on this assembly. No additional control boards are required. The system is expandable to 65K words by adding one additional system board for each 8K of storage. The system may also be operated in a Byte Control mode.

The DR-101 is available in a 19" chassis in two configurations: 32K x 20 in a 5-1/4" high chassis and 16K x 20 in a 3-1/2" high chassis. Both chassis can be supplied with an internal power supply.

SECTION II

SYSTEM SPECIFICATIONS

2.0 System Characteristics

2.01.1 Basic Size: 4K or 8K x 12, 16, 18, 20 bits/word. With byte control the capacity is doubled and the word length is halved. For example, 8K x 20 becomes 16K x 10.

2.01.2 Expandable Size: Additional system boards increase the system size in 8K word increments to a maximum size of 65K words using a total of 8 boards.

2.02 Modes:

Full Cycle: Read/Restore
Clear/Write

Half Cycle: Read/Modify/Write

2.03 Cycle Time:

650 nano sec. minimum

2.04 Access Time:

300 nano sec. maximum

2.05 Voltage Requirements

2.05.1 D.C.
+5.0 V ± 5%
-18.0 V ± 5%

2.05.2 A.C. (When using 19" rack with internal power supply) 115/220 Volts
50 to 60 Hertz

2.06 Current Requirements

2.06.1 D.C. (+5V)

Word Length	Current in Amperes +5V DC
12 Bits	2.2
16 Bits	2.4
18 Bits	2.5
20 Bits	2.6

2.06.2 D.C. (-18V)

The current drain on the -18 volt supply is a function of cycle time and bit length and is shown in the chart in Figure 1.

2.06.3 A.C. (8K x 20) 2 amps.

2.1 Input-Output (Refer to Figure 2 for input-output timing)

2.11 Logic Levels and Characteristics

Refer to Mil-Std. -806B for definition of symbols.

Logic 0	0.45 V @ 1.5 ma.
Logic 1	2.45 V @ 0.1 ma.

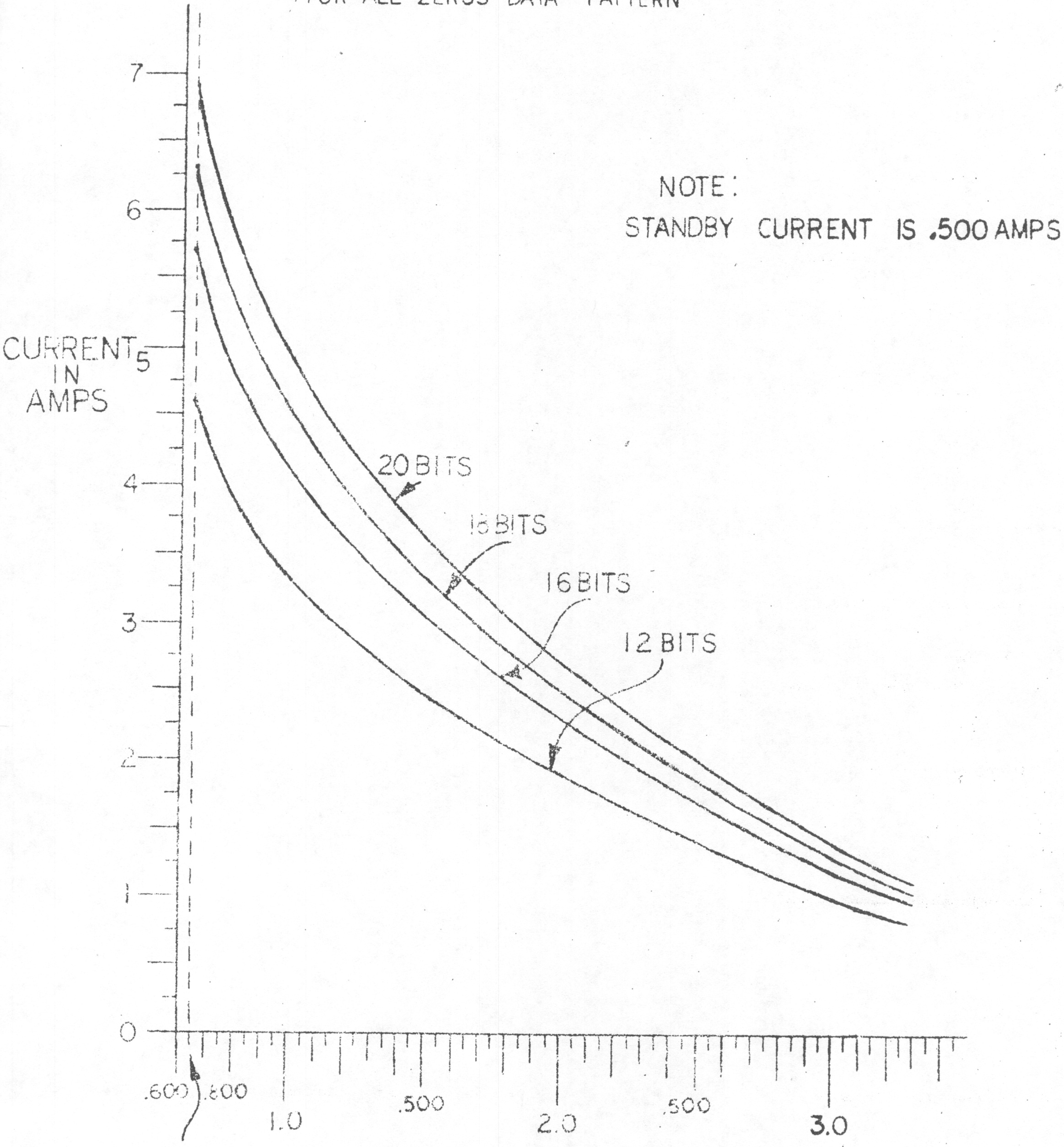
All input commands shall have a risetime (t r) and fall time (t f) of less than 50 nanoseconds. The Overshoot of the leading and trailing edges shall be less than 1.0 volt. All input and output circuits are compatible with standard 830 DTL integrated circuit logic and 7400 TTL logic.

2.12 User - Supplied Inputs (Input lines excluding address may be terminated with 390 ohms to +5 VDC and 470 ohms to ground at customer request)

2.12.1 Address: Thirteen bits single rail are required to select one address of 8192 locations. Additional address bits are required when expanding system. For 65K, three additional bits are required.

-FIG 1-

CURRENT DRAIN VS CYCLE TIME
FOR -18 VOLT POWER SUPPLY
FOR ALL ZEROS DATA PATTERN



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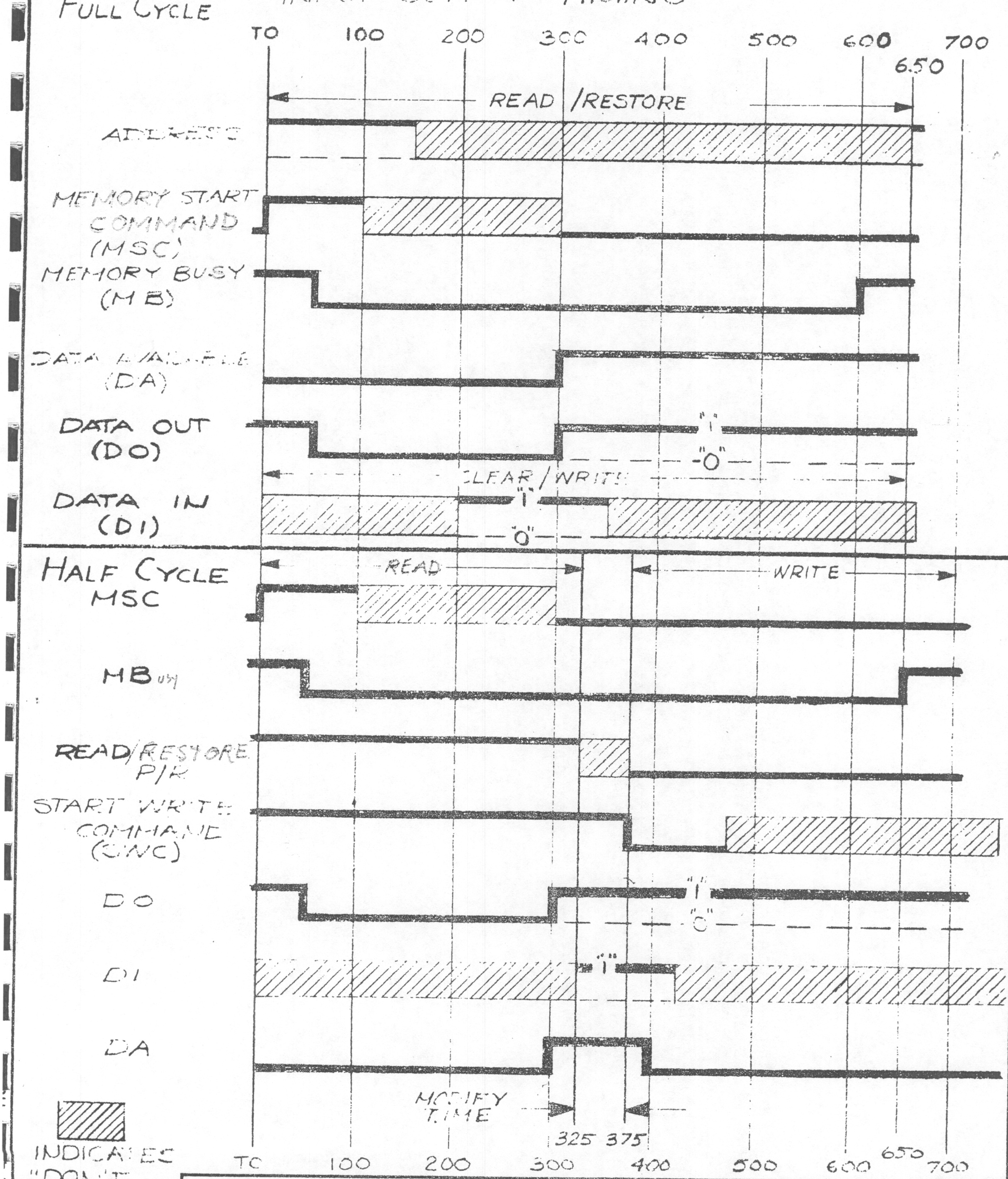
–FIG 2–
INPUT-OUTPUT TIMING



INDICATES "DON'T CARE"

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2.12.2 Full Cycle Mode ($\overline{FCM}$): The FCM command should be in the logic "0" state when the memory is operated in a full-cycle mode, and it should be in the logic "1" state for a half-cycle mode.

* 2.12.3 Memory Start Command (MSC): The MSC initiates the start of a full cycle, or a read half cycle. The command must be a logic one and stay high for a minimum of 100 nanoseconds of t_o.

2.12.4 Start Write Cycle ($\overline{SWC}$): The SWC command is used to start the write half-cycle when the memory is operated in a half-cycle mode. The pulse is a logic 0 valid for 100 nanoseconds minimum. It should return to logic 1 within 200 nanoseconds.

2.12.5 Data In: The Data In can be at either level during a Read/Restore or Read Only operation since the data input lines are internally negated by the R/R command. In a full cycle C/W operation, the data inputs must be valid within 200 nanoseconds of t_o and remain valid for 150 nanoseconds. For a half-cycle Write, data inputs must be valid 50 nanoseconds prior to SWC and remain valid for 150 nanoseconds. A logic 1 will write a "1" into memory.

2.12.6 System Enable 1, System Enable 2, and System Enable 3: These lines are for expanding beyond 8K and are used to allow addressing between system cards. These lines are wired to ground or +5V as follows: This is also shown in Figure 11.

A13	A14	A15	SE1	SE2	SE3	System Size	Bd.No.
0	0	0	GRD	GRD	GRD	8K	1
1	0	0	+5	GRD	GRD	16K	2
0	1	0	GRD	+5	GRD	24K	3
1	1	0	+5	+5	GRD	32K	4
0	0	1	GRD	GRD	+5	40K	5
1	0	1	+5	GRD	+5	48K	6
0	1	1	GRD	+5	+5	56K	7
1	1	1	+5	+5	+5	65K	8

2.12.7 Data Retain: When this line is grounded externally, the cycle in process is completed and future cycles are inhibited. The information within the cores will be protected during power on/off sequences. This line must be held high to operate system.

*When expanding the system beyond 8K words, pulse width of MSC command must be less than the length of time address bits A13-A15 are stable.

2.12.8 Read/Restore 1 (R/R1) and Read/Restore 2 (R/R2): The memory system byte operation modes are controlled by two mode control lines R/R1 and R/R2. The R/R1 line controls Byte 1 (Bits 1-9) operations and the R/R2 line controls Byte 2 (Bits 10-18) operations per the following table:

R/R1	R/R2	Byte 1	Byte 2
Low	Low	Clear/Write	Clear/Write
Low	High	Clear/Write	Read/Restore
High	Low	Read/Restore	Clear/Write
High	High	Read/Restore	Read/Restore

2.13 Memory System Outputs

2.13.1 Data Out: The Data Output will be valid within 300 nanoseconds from t_0 when operating in either a Read/Restore full cycle or a Read half-cycle. It will remain valid until reset by the start of a full or half cycle operation.

The logic level of Data Output with respect to the logic level of Data Input can be inverted or non-inverted as follows:

DR-101-1 Non Inverting ("1" in = "1" out) Data Output lines are from open-collector devices.

DR-101-2 Inverting ("1" in = "0" out) Data Output lines are from Tri-state devices.

DR-101-3 Non Inverting ("1" in = "1" out) Data Output lines are from active-pullup devices.

2.13.2 Memory Busy ($\overline{MB}$): $\overline{MB}$ pulse indicates cycle has been completed and the next cycle can be initiated. The $\overline{MB}$ going to the "1" state indicates that the next cycle can be initiated. It will occur at the end of a full cycle or write half cycle operation.

2.13.3 Data Available (DA): The Data Available pulse is normally low and goes high when data is stable. This line will remain high until data is no longer available from memory.

2.13.4 Lock Up Flag (LUF): Optional signal available when system is supplied in 19 inch chassis with power supply and data retainer circuit. Data retainer circuit senses loss of a.c. power and provides a ground level signal. LUF is normally high when a.c. power is on.

2.2 Mechanical

2.21 Packaging - Figure 3

The system can be in three different mechanical configurations, P.C. card, and two 19" racks. The basic 8K system card consists of a single glass epoxy (G10 material) board approximately 11.5" x 13.7" x .062. The spacing between adjacent boards shall be 1.00" minimum. The two 19" rack chassis are 3.5" high and 17.5" deep for 16K of storage and 5.25" high and 17.5" deep for 32K of storage.

2.22 Connectors

A total of two connectors, Winchester type HW43 are required. The connector pin is designed for wire wrapping. Each connector has 86 pins, 43 per row.

2.3 Cooling

50 cfm of air cooling is required.

2.4 Environmental

2.41 Storage Temperature:

-40° to $+80^{\circ}C$

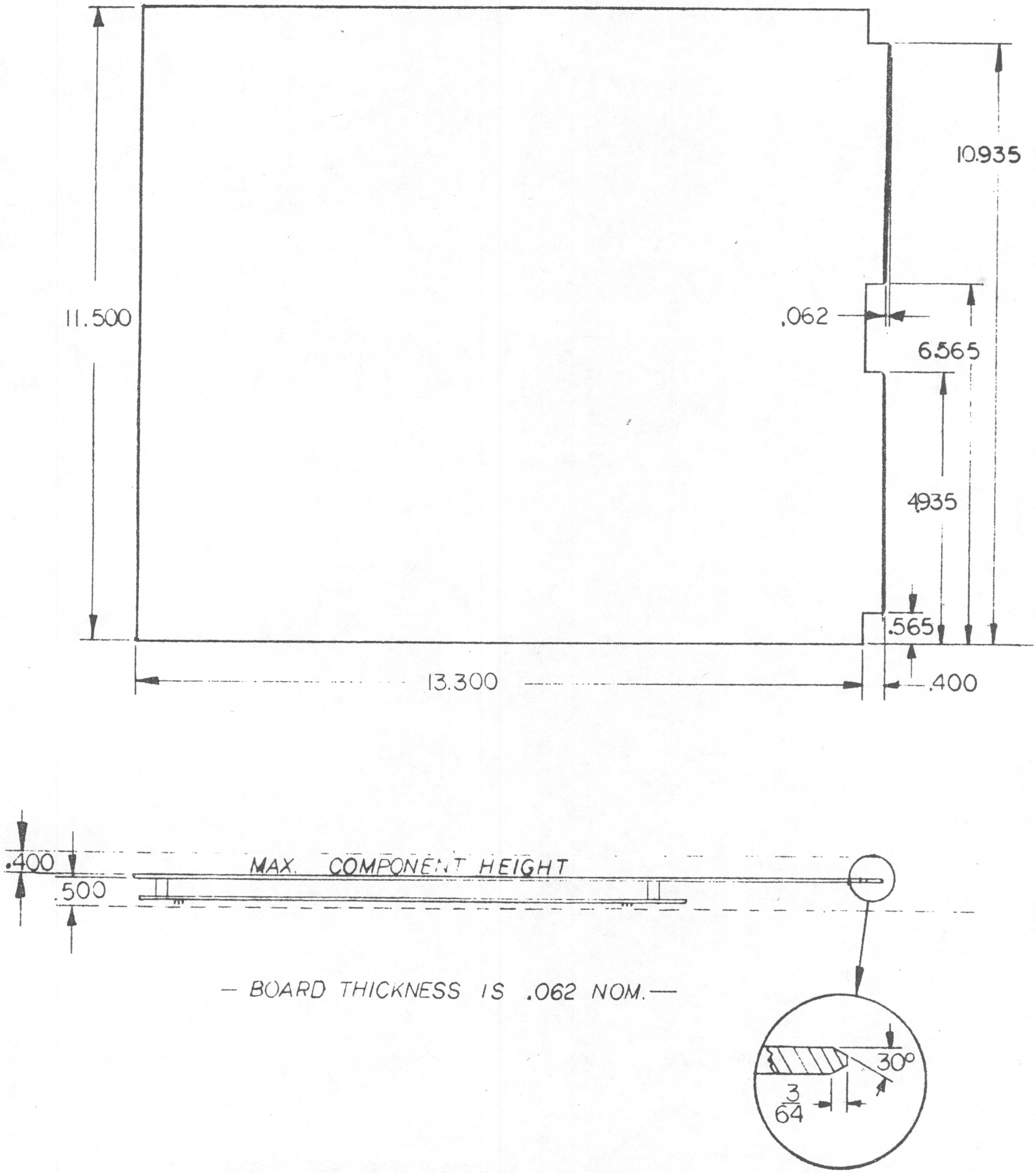
2.42 Operating Temperature:

0° to $+55^{\circ}C$

2.43 Relative Humidity:

Up to 95% without condensation

— FIG 3 —



— BOARD THICKNESS IS .062 NOM. —

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2.5 Interface

2.51 Signal Interface for 19" Rack Mount Chassis

J1 Connector Type: Cannon DC-37S

Pin	Function	Pin	Function
37	Data In - Bit 1	28	Data Out - Bit 5
19	Return	10	Return
36	Data Out - Bit 1	27	Data In - Bit 6
18	Return	9	Return
35	Data In - Bit 2	26	Data Out - Bit 6
17	Return	8	Return
34	Data Out - Bit 2	25	Data In - Bit 7
16	Return	7	Return
33	Data In - Bit 3	24	Data Out - Bit 7
15	Return	6	Return
32	Data Out - Bit 3	23	Data In - Bit 8
14	Return	5	Return
31	Data In - Bit 4	22	Data Out - Bit 8
13	Return	4	Return
30	Data Out - Bit 4	21	Data In - Bit 9
12	Return	3	Return
29	Data In - Bit 5	20	Data Out - Bit 9
11	Return	2	Return
		1	Spare Ground

J2 Connector Type: Cannon DC-37S

37	Data In - Bit 12	28	Data Out - Bit 16
19	Return	10	Return
36	Data Out - Bit 12	27	Data In - Bit 17
18	Return	9	Return
35	Data In - Bit 13	26	Data Out - Bit 17
17	Return	8	Return
34	Data Out - Bit 13	25	Data In - Bit 18
16	Return	7	Return
33	Data In - Bit 14	24	Data Out - Bit 18
15	Return	6	Return
32	Data Out - Bit 14	23	Data In - Bit 19
14	Return	5	Return
31	Data In - Bit 15	22	Data Out - Bit 19
13	Return	4	Return
30	Data Out - Bit 15	21	Data In - Bit 20
12	Return	3	Return
29	Data In - Bit 16	20	Data Out - Bit 20
11	Return	2	Return
		1	Spare Ground

Notes: For an 18 bit system, bits 10 and 11 are eliminated. For a 16 bit system, bits 9-12 are eliminated. For a 12 bit system, bits 7-14 are eliminated.

Four DC-37P connectors are required to mate with J1-J4.

J3 Connector Type: Cannon DC-37S

Pin	Function	Pin	Function
37	Address - Bit 0	29	Address - Bit 8
19	Return	11	Return
36	Address - Bit 1	28	Address - Bit 9
18	Return	10	Return
35	Address - Bit 2	27	Address - Bit 10
17	Return	9	Return
34	Address - Bit 3	26	Address - Bit 11
16	Return	8	Return
33	Address - Bit 4	25	Address - Bit 12
15	Return	7	Return
32	Address - Bit 5	24	Address - Bit 13
14	Return	6	Return
31	Address - Bit 6	23	Address - Bit 14
13	Return	5	Return
30	Address - Bit 7		
12	Return		

J4 Connector Type: Cannon DC-37S

Pin	Function	Pin	Function
35	Memory Start Command (MSC)	28	Data Available
17	Return	10	Return
34	Read/Restore 1 (R/R1)	27	Data Retain
16	Return	9	Return
33	System Enable	26	Read/Restore 2 (R/R2)
15	Return	8	Return
32	Start Write Command ($\overline{\text{SWC}}$)	23	Data In - Bit 10
14	Return	5	Return
31	Full Cycle Mode ($\overline{\text{FCM}}$)	22	Data Out - Bit 10
13	Return	4	Return
29	Memory Busy	21	Data In - Bit 11
11	Return	3	Return
25	Lock Up Flag (LUF)	20	Data Out - Bit 11
7	Return	2	Return

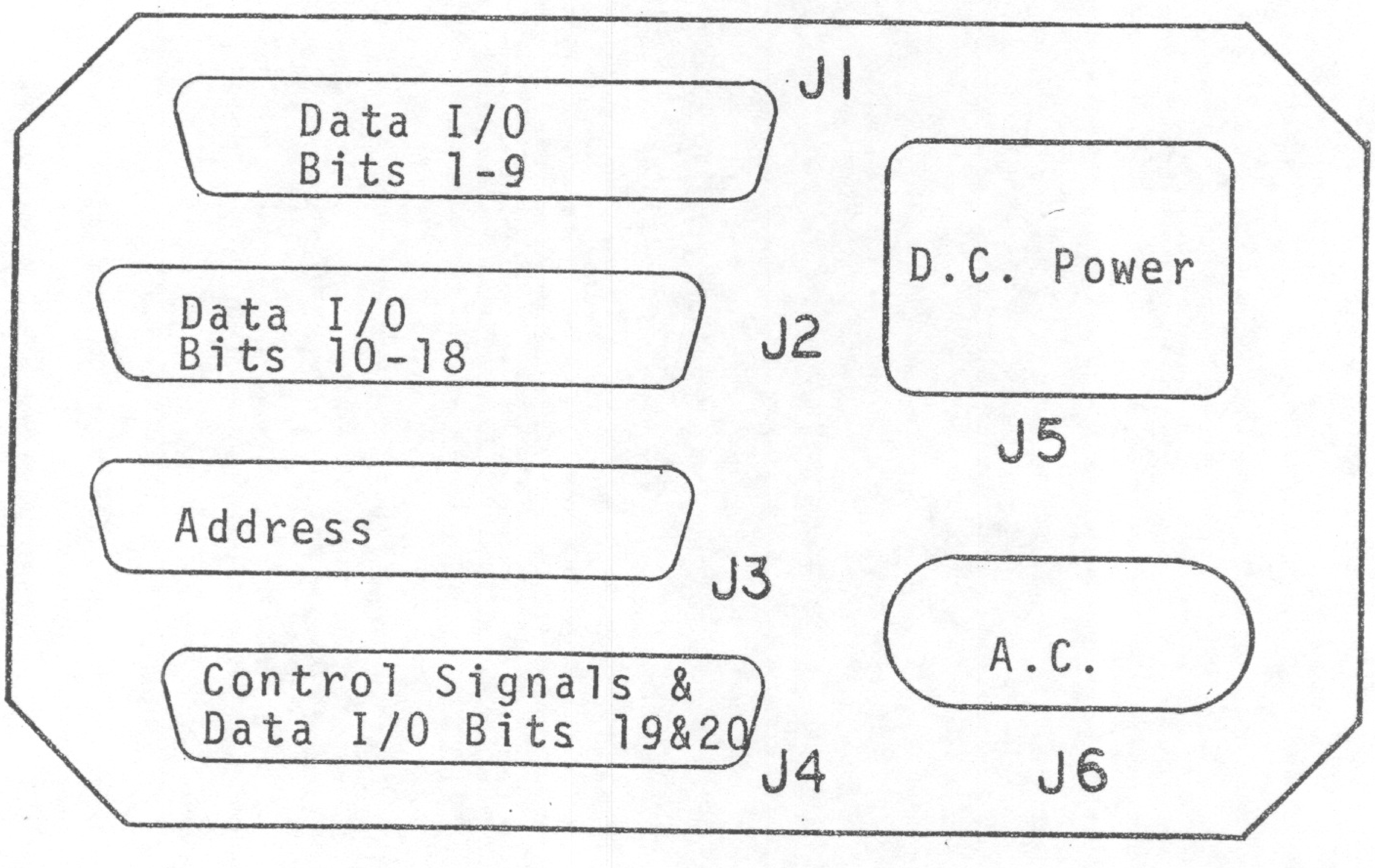
J5 Connector Type: Amphenol 26-4402-8

Pin	Function	Pin	Function
1	+5 Volts DC	5	-18 Volts DC
2	+5 Volts DC	6	-18 Volts DC
3	Ground (+5V)	7	Ground (-18V)
4	Ground (+5V)	8	Ground (-18V)

J6 Connector Type: Switchcraft AC-3G

1	115 V AC
2	115 V AC
3	Ground

2.52 DR-101 P.C. Card Wire List.
The wire list for the DR-101 printed circuit card is located in the documentation section of this manual.



SECTION III

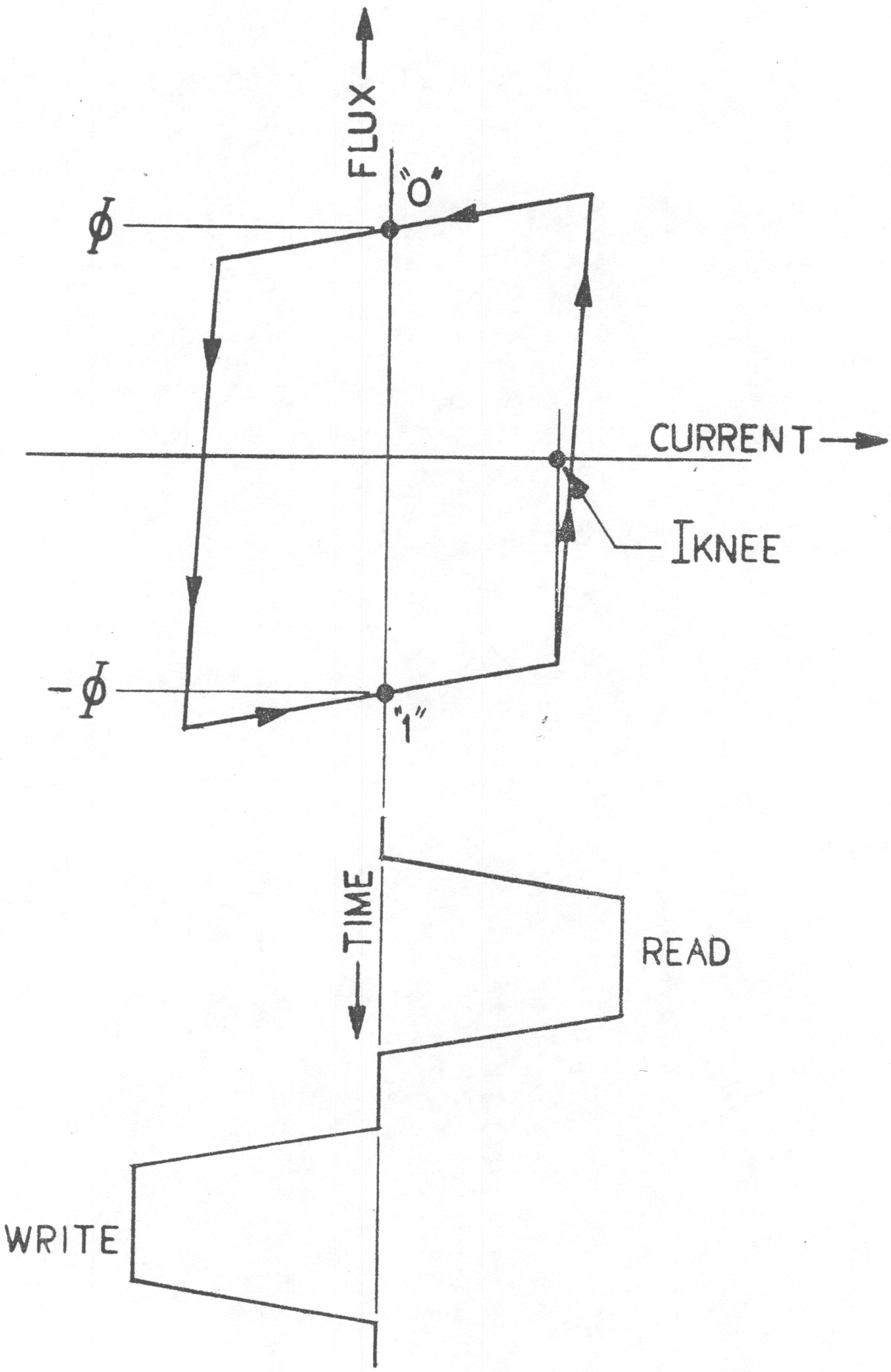
THEORY OF OPERATION

3.0 3D - 3 Wire Operation

A coincident-current core memory, such as the DR-101, has as its basic storage element, a ferrite core, which has a well-defined switching characteristic. Its operation will be explained by referring to Figure 4. This figure defines the switching characteristic of the core and is known as the "hysteresis loop". It shows the relationship of the flux (magnetic field strength) in the core with respect to the total current flowing through the core aperture. Flux above the origin can arbitrarily be defined as flux in the clockwise direction and flux below the origin will be counterclockwise, and the direction of flux will define the storage of a "1" or a "0". Currents on either side of the origin will have opposite directions of current flow through the core. In this explanation, current to the right of the origin will be considered "Read" current and to the left will be "Write" current. A core can be in a "1" or "0" state as shown on the hysteresis loop.

If it is in the "1", a Read current will put it into the "0" state and the flux will change from $-\Phi$ to $+\Phi$ which means the flux will flip from a counterclockwise orientation to clockwise. This change in flux (2Φ) will cause a voltage to be induced on the sense wire which threads the core being interrogated by the Read current and this voltage will be detected as a "1" by the sensing circuitry connected to the sense wire. In the DR-101 system, the "1" output is approximately 30 millivolts. If the core had been in the "0" state, Read current would cause only a relatively (approximately 4 millivolts in DR-101) small change in flux and, therefore, the induced voltage would be seen as a "0" by the sensing circuitry since it is below some minimum detection level.

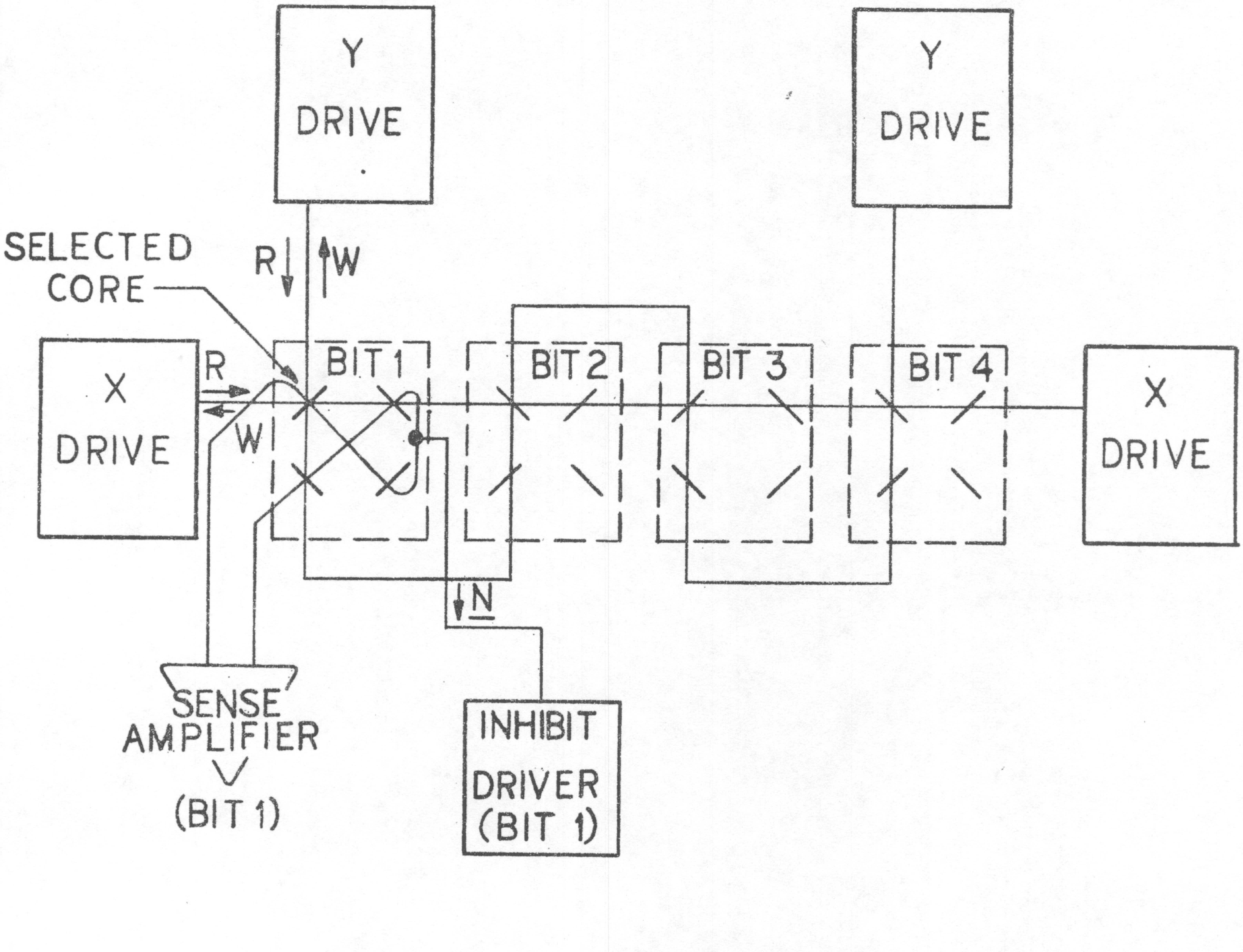
To write, the switching current polarity will be opposite in polarity in relation to the Read current. The Write current will cause the flux to go to a counterclockwise orientation which defines the core as being in the "1" state. When the core does not receive a full Write current during a Write operation, it will stay in the "0" state.



HYSTERESIS LOOP

FIGURE 4

Selection of a particular word in a memory array is shown in Figure 5. The intersection of selected X and Y drive lines in an array will cause the same corresponding core in each bit plane to be pulsed by full Read and full Write currents. In Figure 5, the top left core of each bit plane is selected and the number of bit planes define the number of bits per word. Some unselected cores may experience half-amplitude currents, but the amplitude of these half-amplitude currents will not be sufficient to exceed the knee on the hysteresis loop (see Figure 4) and the core will remain in its previous state.



3D-3 WIRE SCHEME

FIGURE 5

The coincidence of half-Write currents at the selected core location in each bit would cause the selected core to experience full Read and Write currents. This is desired during a Read operation but during a Write operation, it is necessary to control the Write current so that either a "1" or a "0" may be written. This is accomplished by using the sense winding as an inhibit winding during write time and an inhibit driver per bit array. The sense/inhibit winding threads every core in the bit array and the inhibit driver will pulse current through this winding when a "0" is to be written. The inhibit current has the opposite polarity to write current and when it is "on" it cancels one of the two half write currents. The resultant current will be a half-Write, which will be insufficient to switch the core and it will remain in the "0" state.

3.1 System Description

The Block Diagram of the DR-101 memory system is located in the rear of the manual along with the system schematics. The system can be broken into four major functional groups. The stack, timing and control logic, address and drive circuits, and the data loop circuits.

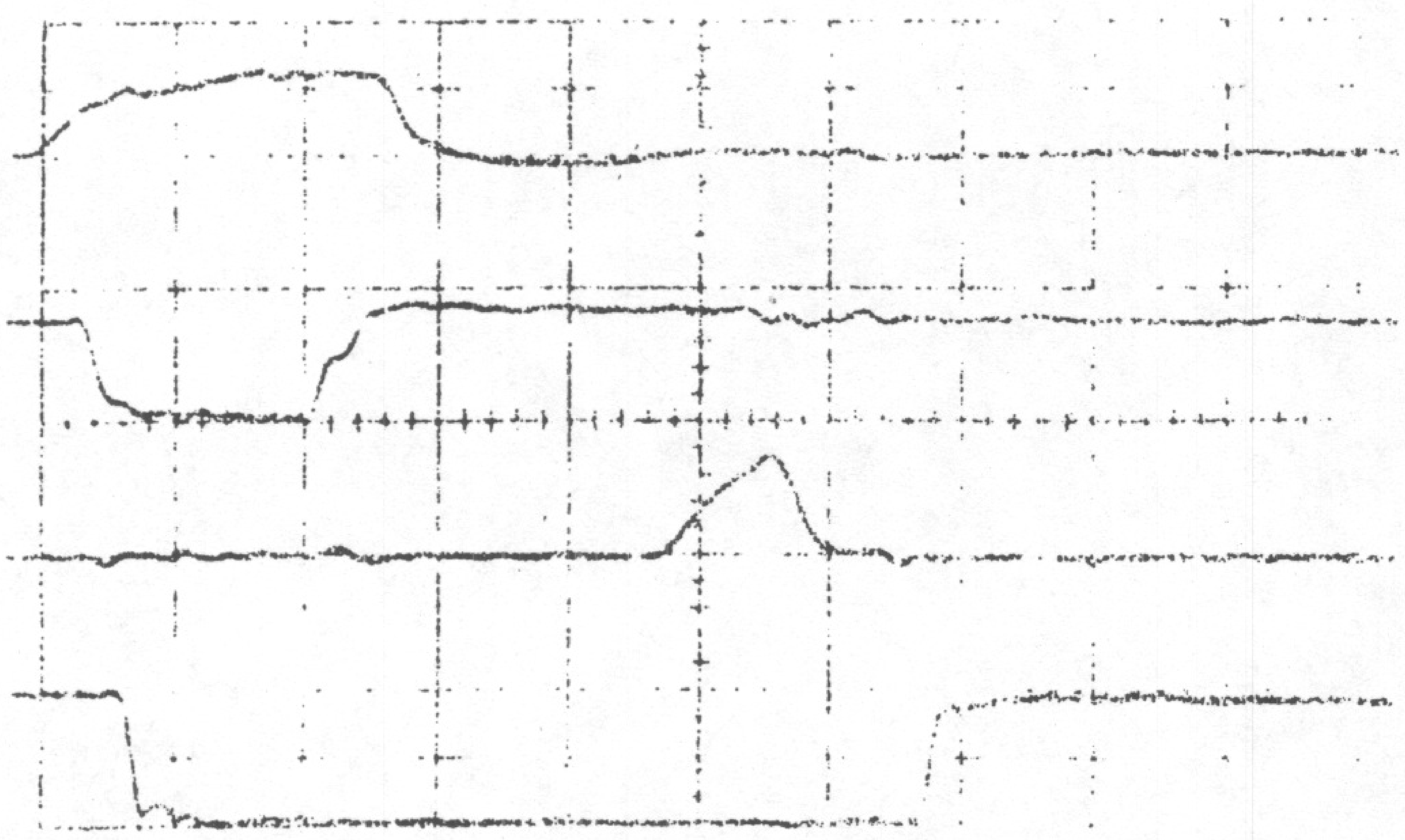
3.11 DR-101 Stack

The DR-101 stack is an 8192 x 20 bit planar core array mounted on an 8 x 10 inch printed circuit board. The lithium ferrite cores (Dataram 1DC101MT) are strung in a 3D-3 Wire array with 64 Y and 128 X drive lines. The selection diodes are also mounted on this board such that there are 8 positive and 8 negative drive connections for each axis along with 8 Y and 16 X sink connections. The drive, sink and sense/inhibit connections interface with the system board via AMP Mod I type pins and receptacles.

3.12 Timing and Control Logic

All timing signals are generated using a lumped constant delay line. The MSC pulse is "latched up" at the input and the latch is reset from a tap 100 nanoseconds down the line. Thus a pulse of 100 nanoseconds propogates down the line. Timing pulses are derived from the 100 nanosecond pulse by logically gating various taps (available every 25 nanoseconds) using T^2L micrologic circuits. During one full cycle operation, the line is "latched up" twice, once for the read half cycle and once for the write half cycle. Significant timing signals are shown in Figures 6 and 7.

DR-101 TIMING WAVEFORMS FIG. 6



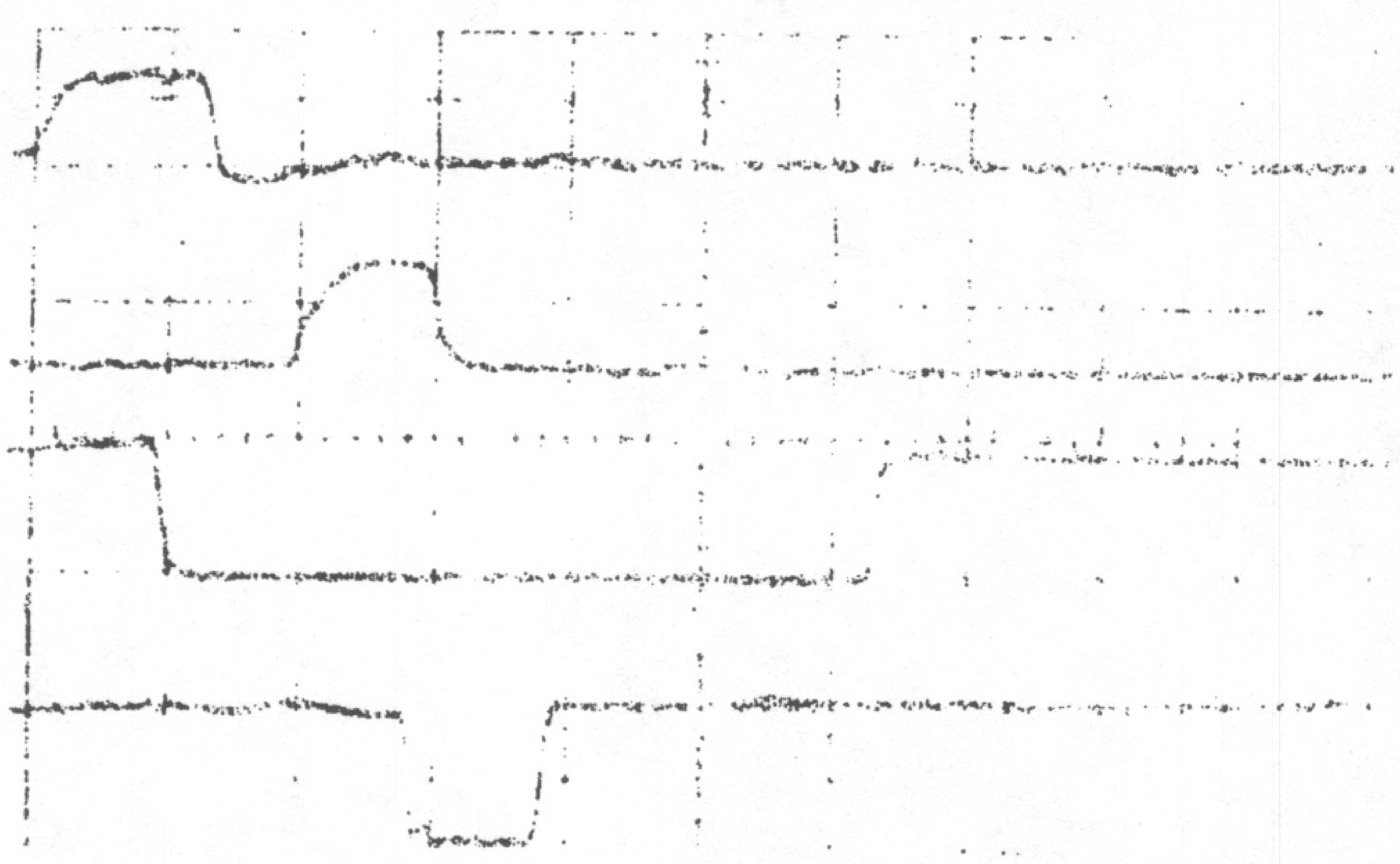
MSC

RESET Z53-2

SSB1 (R/R CYCLE) Z50-1

DATA AVAILABLE Z52-6

VERT.=5V/DIV , HOR.=50 NS/DIV



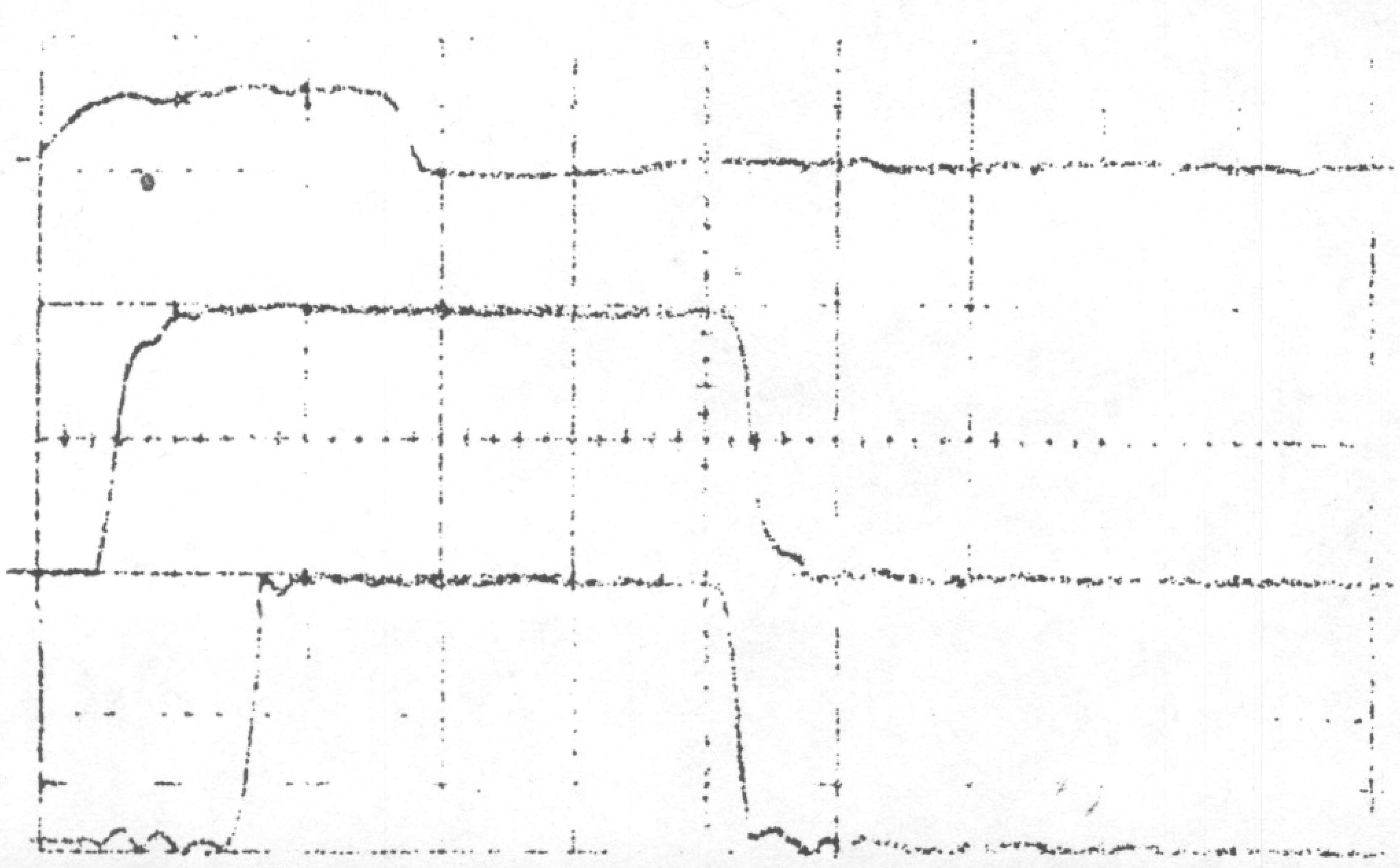
MSC

DATA CLOCK (C/W CYCLE)

MEMORY BUSY

Z58-12

VERT.=5V/DIV , HOR.=100 NS/DIV



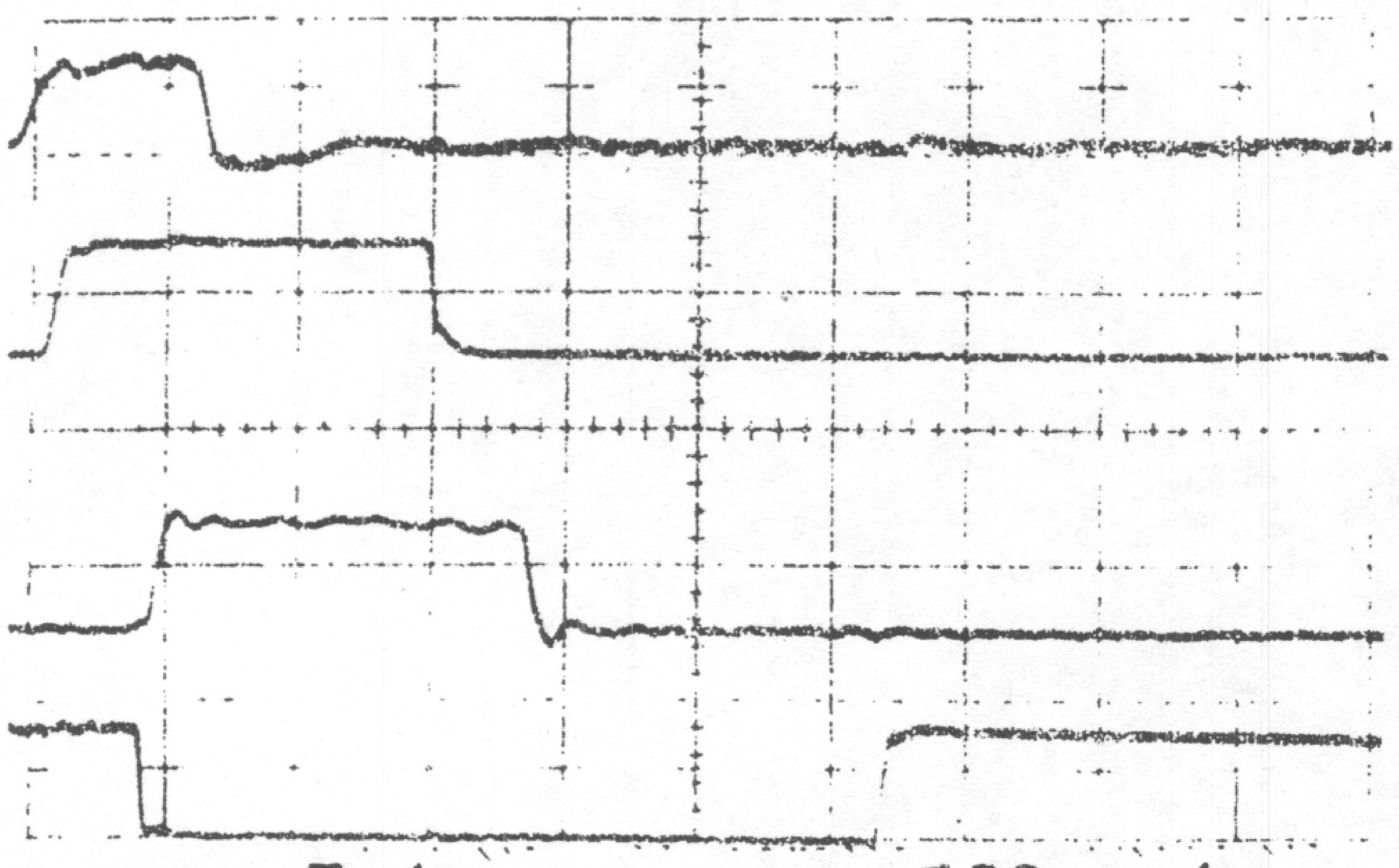
MSC

RY TIMING Z46-8

RX TIMING Z46-6

VERT.=2V/DIV , HOR.=50 NS/DIV

DR - 101 TIMING WAVEFORMS FIG. 7



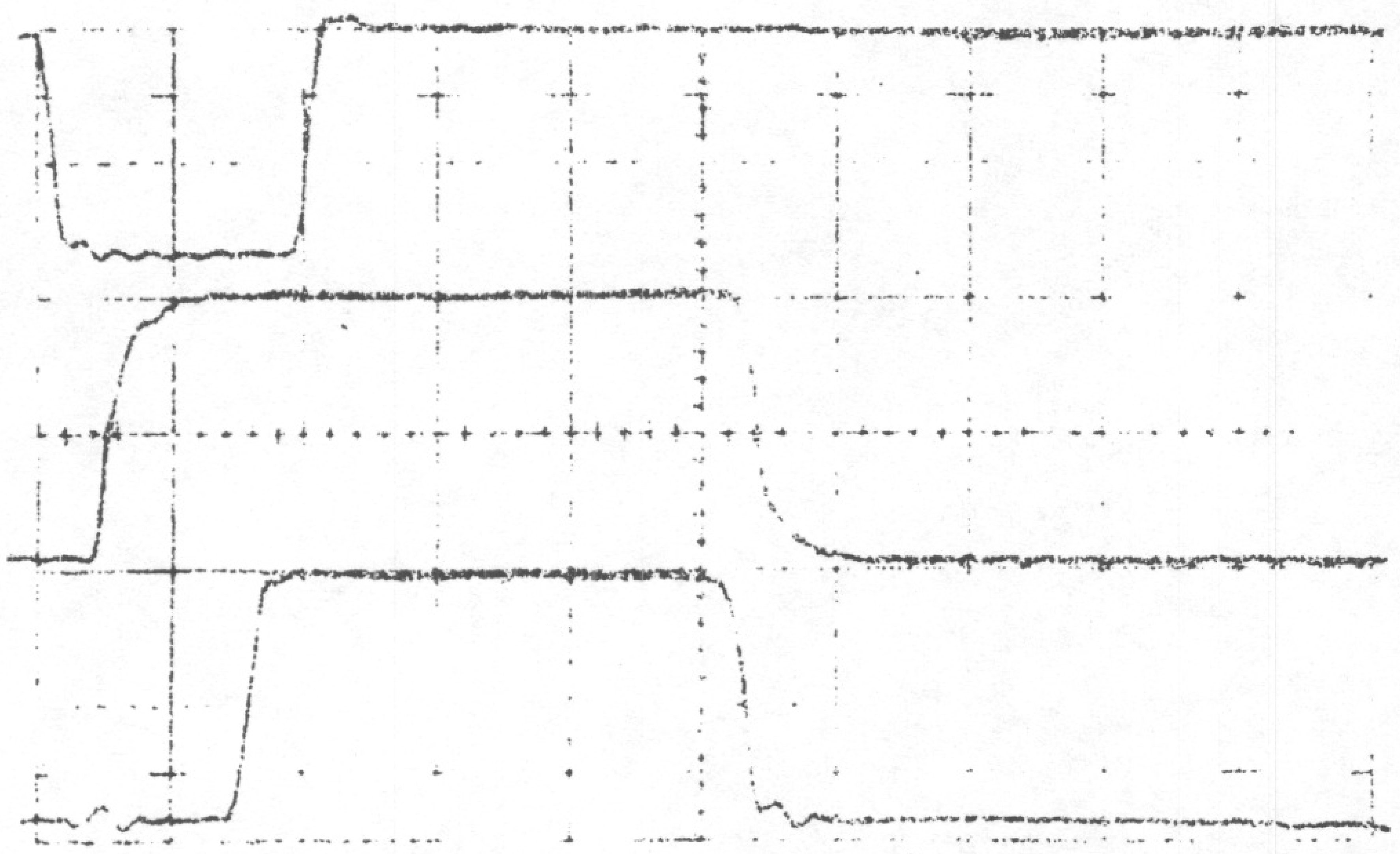
MSC

READ Z56-6

R' Z59-11

ADD. REG. STROBE Z65-8

VERT.=5V/DIV , HOR.=100 NS/DIV



Z58-12 OR Z5-8

IZ TIMING Z47-6

WXY TIMING Z47-8

VERT.=2V/DIV , HOR.=50 NS/DIV

3.13 Address and Drive Circuits

The address register consists of 4 quad "D" type latches. If the clock input is held high, the Q output will follow the D input. The address clock signal for this register is held at a high level prior to the start of a memory cycle and is switched to a low state 50 nanoseconds after the cycle is started. This allows for optimum settling time for the register and the decoder circuits. Address bits A0 - A12 are decoded and connected to the drive circuits. Address bits A13, A14, and A15 are used to enable the system along with signals SE1, SE2 and SE3 via "exclusive-OR" logic.

The basic circuit for the Y drive is shown in figure 8. In this example, four transistors are shown selecting one out of 4 lines. The type of selection circuit used for both the drive and sink ends is known as a bridge switch. A bridge switch consists of one transistor and 4 diodes. At the sink end, the 4 diodes are mounted on the system board. At the drive end, part of the bridge diodes are the stack matrix diodes.

In order to select line 1 for read current, transistor Q_1 and Q_3 are turned on and the current source associated with T_1 is enabled. Thus, a positive current will flow from the dot end of T_1 through Q_1, line 1, Q_3 and back to the opposite end of T_1. No other lines are enabled or disturbed. In order to select line 1 for a write current, transistors Q_2 and Q_4 are turned on and the current source associated with T_2 is enabled. This will allow a current, opposite in direction to the read current, to flow in line 1. The chart below lists the various combinations required to select each line for read and write.

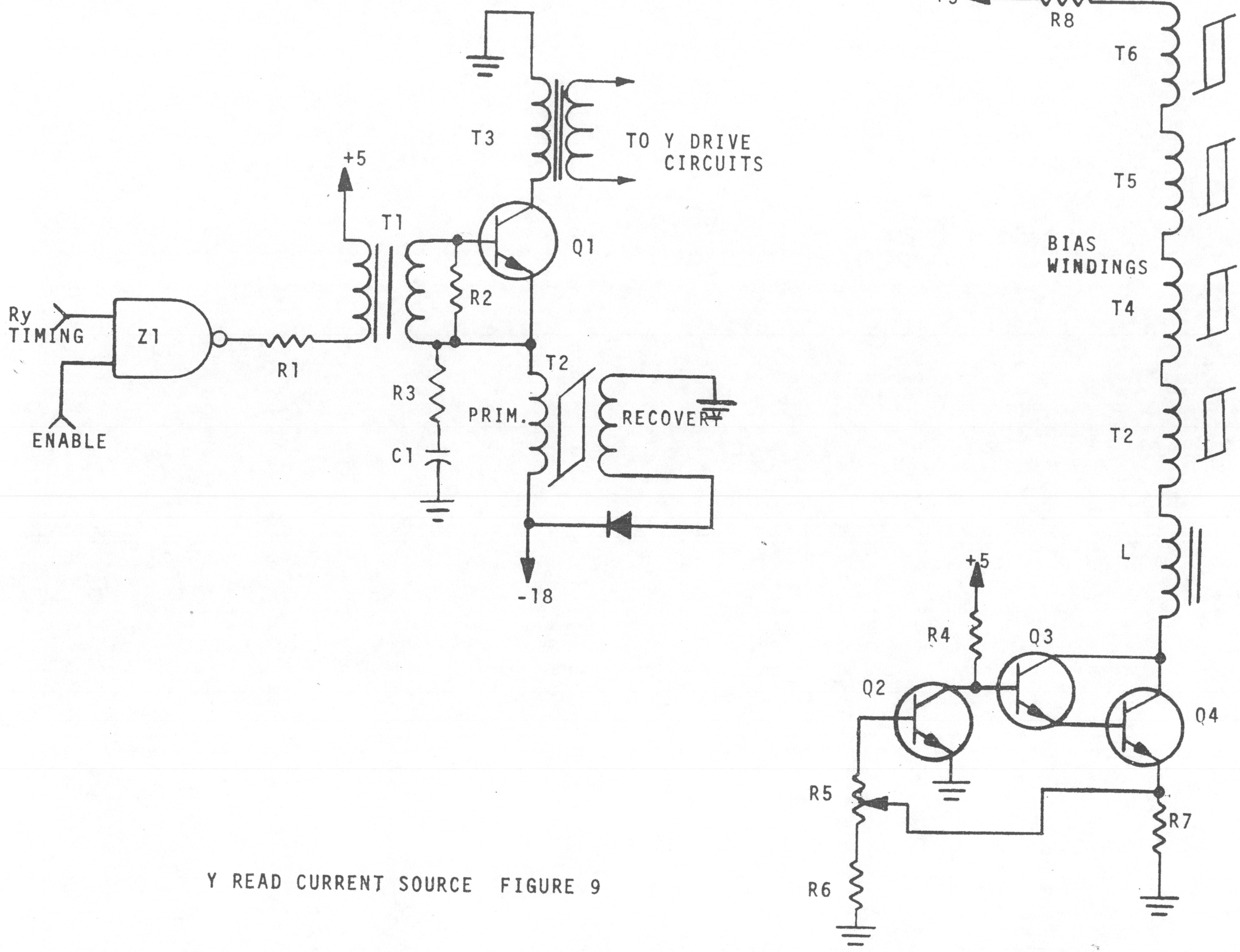
Line	Read Via T_1	Write Via T_2
1	Q_1, Q_3	Q_2, Q_4
2	Q_1, Q_4	Q_2, Q_3
3	Q_2, Q_4	Q_1, Q_3
4	Q_2, Q_3	Q_1, Q_4

BASIC Y DRIVE CIRCUITS FIGURE 8

The bridge switch drive scheme requires half as many transistors as the more conventional bipolar drive scheme. For this example, 8 transistors in a bipolar or teeter-totter arrangement would be required to select one out of 4 lines for both read and write.

Transistors Q_1 - Q_4 are selected via transformers T_3 - T_6 and the 1 out of 8 decoders Z_1 and Z_2. The address register outputs are connected to the inputs of the decoders and one output of each decoder will go low depending upon the state of the address bits. This will enable the transformers and allow one transistor on each side to turn on via the predrive circuits. Exclusive-OR circuits are used to switch the decoders during the write cycle so that the opposite pair of transistors is turned on.

A typical circuit for the Y Read current source is shown in figure 9. This circuit uses a transformer with a square-loop core (T_2) as the current determining element. The transformer has three windings; primary, bias and recovery. The bias winding is connected to a linear current regulator in series with the bias windings of the other current sources. The primary winding is connected in the emitter circuit of transistor Q_1. During read timing, transistor Q_1 saturates via the signal from transformer T_1. The current in the collector circuit will rise until it reaches the value of current that is flowing in the bias winding (about 400 m.a.). At that point, the square loop core switches and the primary winding looks like a high impedance. The current in the collector circuit will remain constant until Q_1 is shut off. The recovery winding is connected to the -18 volt supply via a diode. At turn-off, the voltage across the recovery winding will rise to a value greater than -18 volts to allow current to flow into the supply. This provides a path for the energy stored in the square loop and drive line inductance. The R-C network in the emitter circuit of Q_1 is used to delay the voltage transient during turn-off and thus keeps the dissipation of Q_1 at a low value. The current sources for the Y write and X read and write currents are identical to this circuit.



Y READ CURRENT SOURCE FIGURE 9

The core used in the stack requires the drive currents to be compensated .18%/^{o}C. The overall temperature characteristic of the current regulator approximates this curve. This is primarily due to the variation of Vbe of transistor Q_2 with temperature.

3.14 Data Loop Circuitry

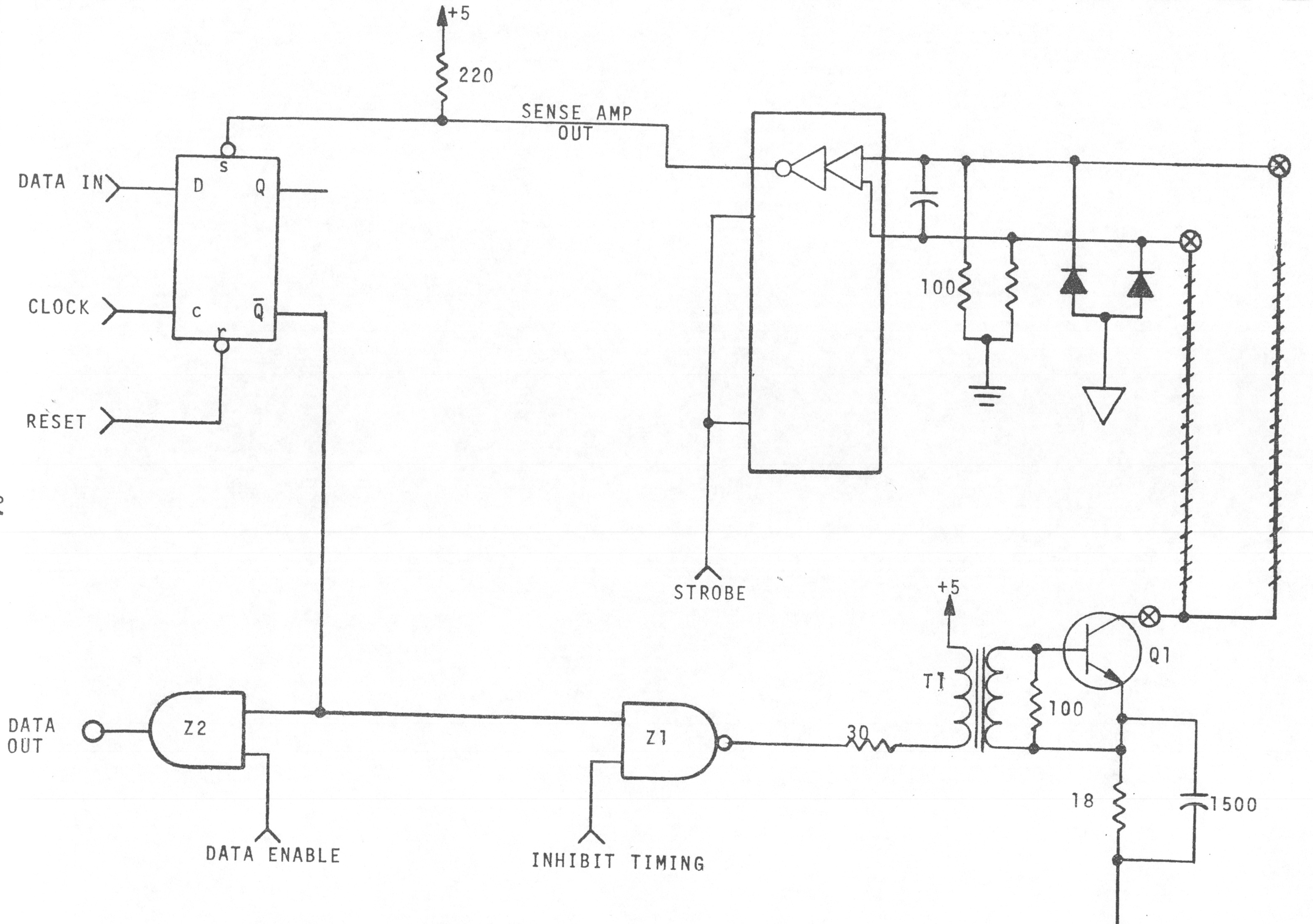
The circuitry shown in figure 10 forms the data loop circuitry whereby information is read from core and recirculated after reading, or data is written into memory from an external source. This circuitry consists of a data register, data output buffer, inhibit driver and sense amplifier per bit.

The data register is a "D" edge triggered binary. The data into memory is connected to the "D" input and is clocked into the register via a pulse at the clock input. The clock is enabled only during a Clear/Write cycle or a Write half cycle.

If a one is to be written into memory, the $\overline{Q}$ output of the binary will be in a low state. During inhibit timing, nand gate Z_1 will be disabled and, therefore, Q_1 will be off and a one will be written into memory.

If a zero is to be written, the $\overline{Q}$ output will go high and nand gate Z_1 will be enabled during inhibit timing. Transistor Q_1 will turn on and inhibit current will flow in the sense/inhibit winding. This flow of current will cause a zero to be written into memory.

It it is desired to read from memory, the data register is first reset at the beginning of the read cycle. The sense amplifier will be enabled by a strobe pulse which goes high at pins 11 and 15 of the sense amplifier. This strobe will be present only in a Read/Restore mode or in a Read half cycle mode. The output of the sense amplifier will be a negative pulse if a "1" core output is present on the differential inputs of the sense amplifier.



DATA LOOP CIRCUIT FIGURE 10

This pulse will set the "D" binary and cause the $\overline{Q}$ output to go low. The $\overline{Q}$ output is connected to the output buffer (Z_2) which will cause the data output to go high. If a zero is present at the sense amplifier terminals, the register will not be set and, therefore, the data output line will remain in a low state.

The other input to Z_1 is an enable line which enables the gate only if the memory is in a Read/Restore or Read half cycle mode and if the memory is enabled. At all other times, the gate will be disabled and the data output will be in a high or inactive state.

For the DR-101-2 option, the gate Z_1 is a tri-state circuit and the data output will be inverted from the levels discussed above. However, when Z_1 is disabled, the output line will still go to an inactive state.

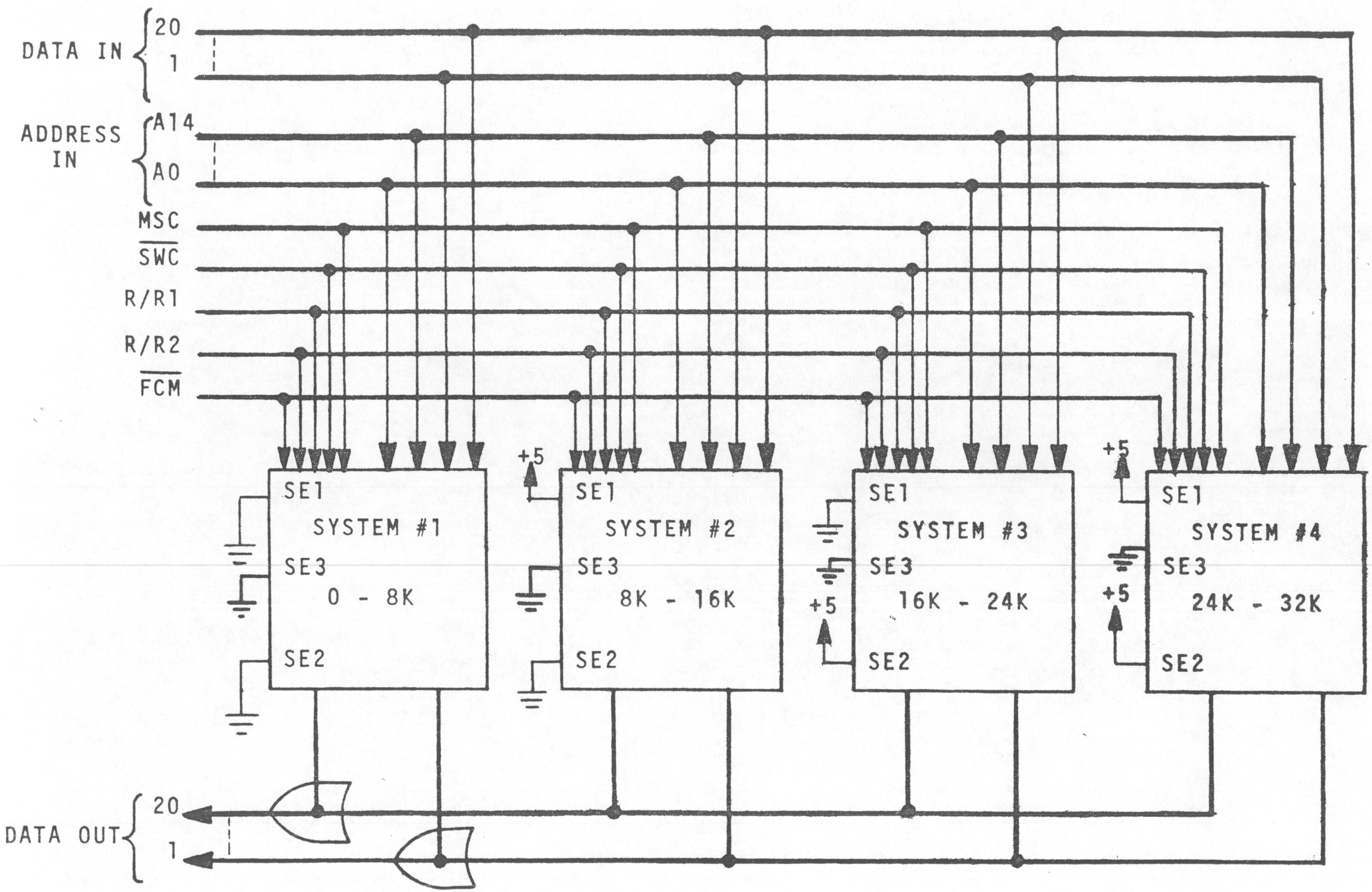
SECTION IV

4.0 System Expansion

The capacity of the DR-101 memory system can be expanded beyond 8K of storage by bussing the input lines and by "dot-oring" the output lines. The block diagram in Figure 11 shows the connections for expansion to 32K. For expansion to 65K, four additional systems are bussed together with the systems shown in Figure 11 except that line SE3 is connected to +5 volts on the additional four boards.

When expanding the DR-101, only options DR-101-1 (open collector) and DR-101-2 (tri-state) may be used. The DR-101-3 system has active pull-up output circuits and may not be used for "dot-or" expansion.

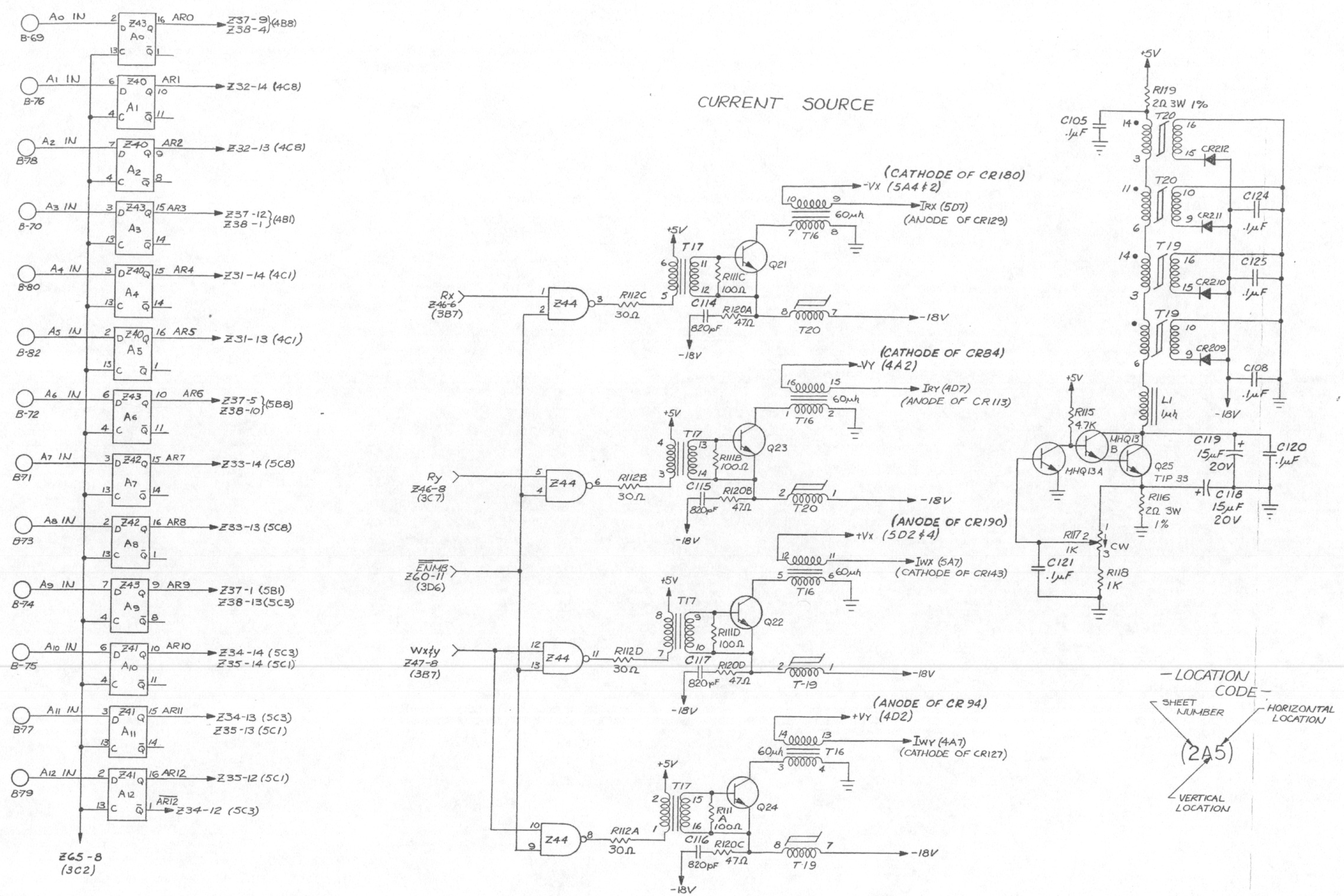
Since address bits A13-A15 are used to enable the memory and the output buss, the timing between these levels and the MSC command must be considered. These address bits must remain valid for a period of time which is 50 nanoseconds longer than the trailing edge of the MSC command. For example: if address bits A13-A15 are valid 50 nanoseconds prior to MSC and remain valid for 250 nanoseconds, then the maximum allowable width for the MSC command is 150 nanoseconds.



SYSTEM EXPANSION DIAGRAM FIGURE 11

SECTION V

DOCUMENTATION



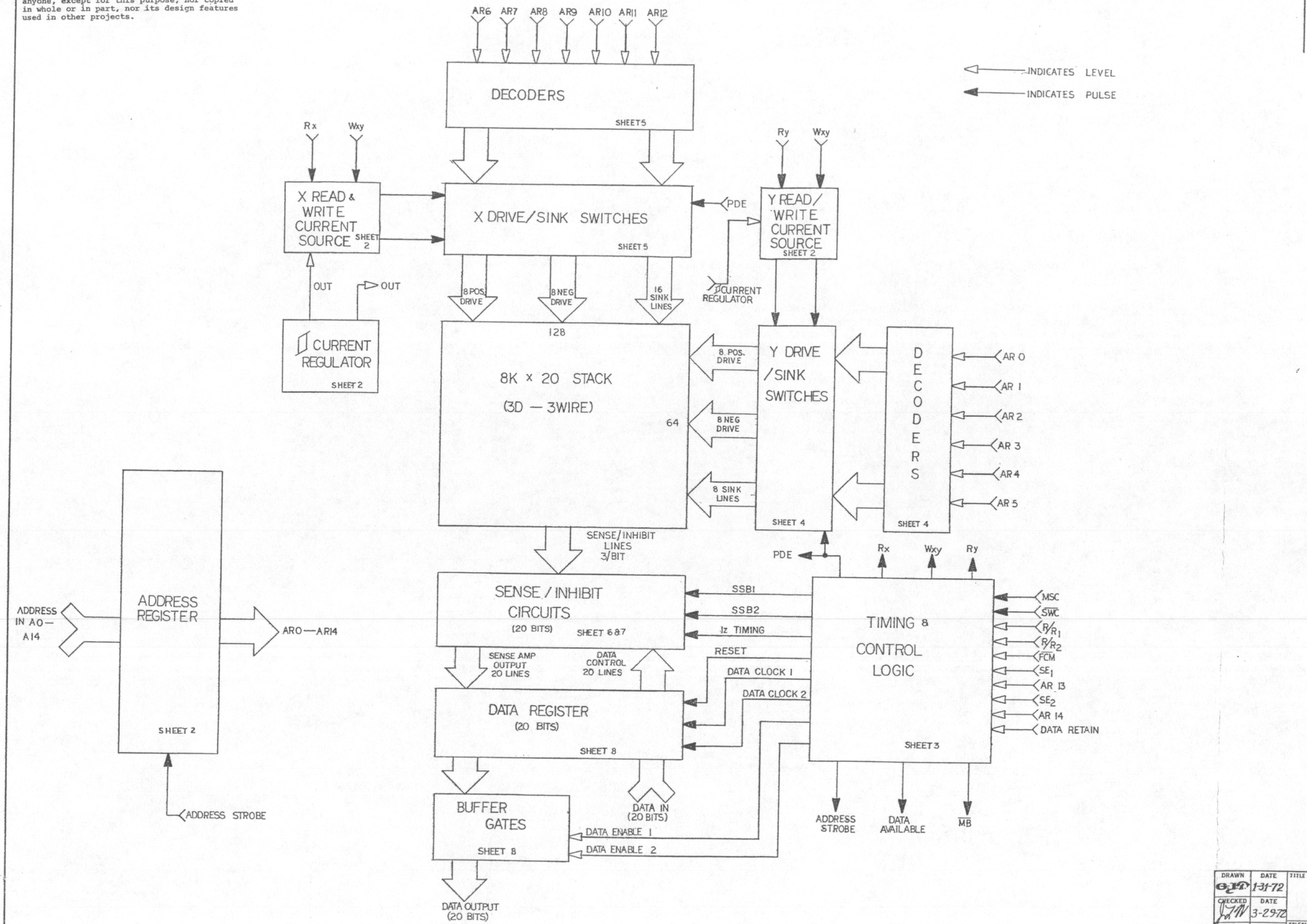
REVISIONS			
SYM.	DESCRIPTION	APPROV.	DATE

— ADDRESS REGISTER & CURRENT SOURCE —

DRAWN	DATE	TITLE SCHEMATIC DIAGRAM DR-101 MEMORY SYSTEM
CHECKED	DATE	
ENGR.	DATE	TOLERANCES, UNLESS OTHERWISE SPECIFIED: DECIMALS ± FRACTIONS ± ANGLES ±
APPROVED	DATE	DATARAM CORPORATION, PRINCETON, NEW JERSEY

DWG. NO. 309D0232 REV. A SHEET 2 OF 8

REVISIONS			
SYM.	DESCRIPTION	APPROV.	DATE
A	RELEASED TO PRODUCTION	B7H	3-29-72



— BLOCK DIAGRAM —

DRAWN	DATE	TITLE
GJP	1-31-72	SCHEMATIC DIAGRAM DR-101 MEMORY SYSTEM
CHECKED JJW	DATE 3-29-72	TOLERANCES, UNLESS OTHERWISE SPECIFIED: DECIMALS ± FRACTIONS ± ANGLES ±
ENGR. B7H	DATE 3-29-72	SCALE —
APPROVED B7H	DATE 3-29-72	DATARAM CORPORATION, PRINCETON, NEW JERSEY — DWG. NO. 309D0232 — SHEET 1 OF 8 — REV. A

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TIMING & CONTROL LOGIC

DRAWN	DATE	TITLE
CHECKED	DATE	SCHEMATIC DIAGRAM DR-101 MEMORY SYSTEM
ENGR.	DATE	TOLERANCES, UNLESS OTHERWISE SPECIFIED DECIMALS ± FRACTIONS ± ANGLES ±
APPROVED	DATE	DATARAM CORPORATION PRINCETON NEW JERSEY — DWG. NO. 309D0232 — REV. A — SHEET 3 OF 8

REVISIONS: SYM. | DESCRIPTION | APPROV. | DATE

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DRAWN	DATE
CHECKED	DATE
ENGR	DATE
APPROVED	DATE

TITLE SCHEMATIC DIAGRAM
DR-101 MEMORY SYSTEM

TOLERANCES, UNLESS OTHERWISE SPECIFIED
DECIMALS ± FRACTIONS ± ANGLES ±

SCALE —

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. 309D0232 REV. A
SHEET 4 OF 8

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—XDRIVE CIRCUITS—

INDICATES POWER GROUND

DRAWN	DATE	TITLE
CHECKED	DATE	SCHEMATIC DIAGRAM DR-101 MEMORY SYSTEM
ENGR	DATE	TOLERANCES, UNLESS OTHERWISE SPECIFIED DECIMALS ± FRACTIONS ± ANGLES ± SCALE
APPROVED	DATE	DATARAM CORPORATION PRINCETON NEW JERSEY DWG. NO. 309D0232 REV. A SHEET 5 OF 8

INDICATES POWER GROUND

INDICATES LOGIC GROUND

⊗ INDICATES A CONNECTION BETWEEN STACKBOARD & SYSTEM BOARD

BYTE 1 — SENSE/INHIBIT CIRCUITS —

DRAWN	DATE	TITLE
CHECKED	DATE	SCHEMATIC DIAGRAM DR-101 MEMORY SYSTEM
ENGR	DATE	TOLERANCES, UNLESS OTHERWISE SPECIFIED DECIMALS ± FRACTIONS ± ANGLES ±
APPROVED	DATE	DATARAM CORPORATION PRINCETON NEW JERSEY

DWG. NO. 309D0232 REV. A SHEET 6 OF 8

BYTE 2 SENSE / INHIBIT CIRCUITS

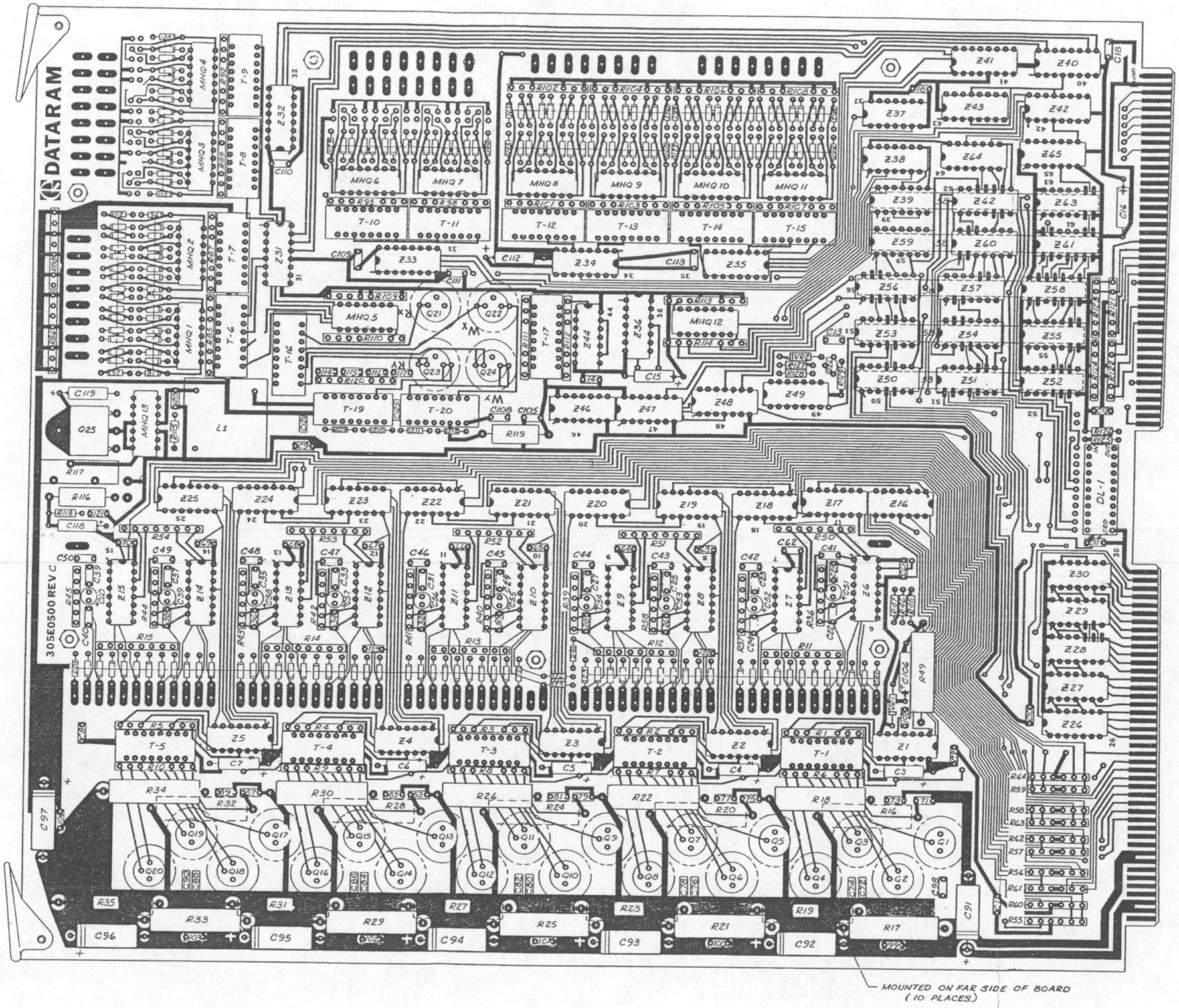
⊗ INDICATES A CONNECTION BETWEEN STACK BOARD & SYSTEM BOARD

▽ INDICATES POWER GROUND

⏚ INDICATES LOGIC GROUND

DRAWN	DATE	TITLE: SCHEMATIC DIAGRAM DR-101 MEMORY SYSTEM
CHECKED	DATE	
ENGR.	DATE	TOLERANCES, UNLESS OTHERWISE SPECIFIED — DECIMALS ± — FRACTIONS ± — ANGLES ± — SCALE
APPROVED	DATE	DATARAM CORPORATION, PRINCETON, NEW JERSEY — DWG. NO. 309D0232 — REV. A — SHEET 7 OF 8


REVISIONS
DESCRIPTION
APPROV.
DATE
DATA IN BIT 1
DØØ
SENSE AMP OUT BIT 1
Z6-14 (6D5)
BIT 1 DATA OUT
DATA CONTROL Z1-12 (6D8)
DATA IN BIT 3
DØ1
SENSE AMP OUT BIT 3
Z6-12 (6C5)
BIT 3 DATA OUT
DATA CONTROL Z1-10 (6C8)
DATA IN BIT 2
DØ2
SENSE AMP OUT BIT 2
Z7-14 (6C5)
BIT 2 DATA OUT
DATA CONTROL Z1-1 (6C8)
DATA IN BIT 6
DØ3
SENSE AMP OUT BIT 6
Z7-12 (6B5)
BIT 6 DATA OUT
DATA CONTROL Z1-5 (6B8)
DATA IN BIT 4
DØ4
SENSE AMP OUT BIT 4
Z8-14 (6B5)
BIT 4 DATA OUT
DATA CONTROL Z2-13 (6B8)
DATA IN BIT 5
DØ5
SENSE AMP OUT BIT 5
Z8-12 (6A5)
BIT 5 DATA OUT
DATA CONTROL Z2-10 (6A8)
DATA IN BIT 7
DØ6
SENSE AMP OUT BIT 7
Z9-14 (6D1)
BIT 7 DATA OUT
DATA CONTROL Z2-1 (6D4)
DATA IN BIT 13
D15
SENSE AMP OUT BIT 13
Z12-14 (7C5)
BIT 13 DATA OUT
DATA CONTROL Z4-13 (7C8)
DATA IN BIT 12
PB
SENSE AMP OUT BIT 12
Z11-12 (7C5)
BIT 12 DATA OUT
DATA CONTROL Z3-5 (7C8)
DATA IN BIT 11
SENSE AMP OUT BIT 11
Z11-14 (7D5)
BIT 11 DATA OUT
DATA CONTROL Z3-1 (7D8)
DATA IN BIT 10
SENSE AMP OUT BIT 10
Z10-12 (6B1)
BIT 10 DATA OUT
DATA CONTROL Z3-10 (6B4)
DATA IN BIT 9
PA
SENSE AMP OUT BIT 9
Z10-14 (6C1)
BIT 9 DATA OUT
DATA CONTROL Z3-13 (6C4)
DATA IN BIT 8
DØ7
SENSE AMP OUT BIT 8
Z9-12 (6C1)
BIT 8 DATA OUT
DATA CONTROL Z2-5 (6C4)
D14
DATA IN BIT 14
SENSE AMP OUT BIT 14
Z12-12 (7B5)
BIT 14 DATA OUT
DATA CONTROL Z4-10 (7B8)
DATA IN BIT 15
D13
SENSE AMP OUT BIT 15
Z13-14 (7B5)
BIT 15 DATA OUT
DATA CONTROL Z4-1 (7B8)
DATA IN BIT 16
D12
SENSE AMP OUT BIT 16
Z13-12 (7A5)
BIT 16 DATA OUT
DATA CONTROL Z4-5 (7A8)
DATA IN BIT 20
D11
SENSE AMP OUT BIT 20
Z14-14 (7D1)
BIT 20 DATA OUT
DATA CONTROL Z5-13 (7D4)
DATA IN BIT 17
D1Ø
SENSE AMP OUT BIT 17
Z14-12 (7C1)
BIT 17 DATA OUT
DATA CONTROL Z5-10 (7C4)
DATA IN BIT 19
DØ9
SENSE AMP OUT BIT 19
Z15-14 (7C1)
BIT 19 DATA OUT
DATA CONTROL Z5-1 (7C4)
DATA IN BIT 18
DØ8
SENSE AMP OUT BIT 18
Z15-12 (7B1)
BIT 18 DATA OUT
DATA CONTROL Z5-5 (7B4)
74H74
Z26 THRU Z30 ON -2 SYSTEM IS DM8094
CLOCK BYTE 1 Z51-13 (3B4)
RESET Z53-4 (3C5)
DATA ENABLE BYTE 1 Z51-10 (3A5)
CLOCK BYTE 2 Z51-1 (3B4)
RESET Z53-2 (3C5)
DATA ENABLE BYTE 2 Z51-4
INSTALLED IN OPTION T SYSTEMS ONLY
— DATA REGISTER —
DRAWN
CHECKED
ENGR
APPROVED
DATE
TITLE
SCHEMATIC DIAGRAM
DR101 MEMORY SYSTEM
TOLERANCES, UNLESS OTHERWISE SPECIFIED
DECIMALS
FRACTIONS
ANGLES
SCALE
DATARAM CORPORATION
PRINCETON
NEW JERSEY
DWG. NO. 309D0232
REV. A
SHEET 8 OF 8



UNLESS OTHERWISE SPECIFIED			SCALE	DRAWN	DATE
FRACTIONS	DECIMALS	ANGLES			1/12/72
MATERIAL SPECIFICATION				CHECKED	DATE 3/29/72
				DSGN/ENGR BJH	DATE 3/29/72
SURFACE TREATMENT	HEAT TREATMENT			APPROVED BJH	DATE 3/29/72

TITLE
COMPONENT LOCATION
DR-101, 8K x 20

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG NO 302E0182 REV
SHEET 1 OF 1

REV. B

DWG. NO. B/M301A0302-0 SHEET 1 OF 6

REVISIONS				
SYM.	SHEET	DESCRIPTION	APPROV.	DATE
A	ALL	REVISED	BJH	3-7-72
B		ADDED ITEMS 70-72	BJH	4-7-72

NOTE:~

ITEMS 56 & 57 USED ON SYSTEMS WITH SUFFIX "T" ONLY.

EX. 301-0302-1-T

ITEM 14: -1 = 7438
-2 = DM8094
-3 = 74H00

DRAWN	DATE	TITLE
JJN	1-3-72	BILL OF MATERIALS
CHECKED	DATE	DR-101-0 8K x 20
D.C.D.	3-7-72	
ENGR.	DATE	
BJH	3-7-72	
APPROVED	DATE	
BJH	3-7-72	

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. B/M301A0302-0 REV. B
SHEET 1 OF 6

TITLE: B/M DR-101 , 8K x 20

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
1	10	7534	SENSE AMP	DR-QPL 01	Z6-15
2	6	7438	QUAD 2 INPUT POS. NAND BUFFER	"	Z1-5, Z44
3	10	74H74	DUAL "D" FLIP FLOP	"	Z16-25
4	4	7475	QUAD "D" FLIP FLOP	"	Z40-43
5	5	74145	BCD TO DECIMAL DECODER	"	Z31-35
6	3	74H51	DUAL 2 WIDE 2 INPUT AND OR INVERTER GATES	"	Z46, 47, 54
7	3	74S40	DUAL 4 INPUT NAND BUFFER	"	Z55, 56, 65
8	2	7486	QUAD 2 INPUT EXCLUSIVE-OR GATE	"	Z37, 38
9	2	74H10	TRIPLE 3 INPUT POS. NAND GATE	"	Z57, 58
10	1	74H08	QUAD 2 INPUT POS. AND GATE	"	Z48
11	2	74H04	HEX INVERTER	"	Z52, 53
12	5	7402	QUAD 2 INPUT NOR GATE	"	Z36, 39, 50, 51, 62
13	4	74H00	QUAD 2 INPUT NAND GATE	"	Z49, 59-61
14	6	*	SEE COVER SHEET	"	Z26-30, 63
32	1	MC3022	QUAD 2 INPUT EXCLUSIVE NOR	MOTOROLA	Z64
15	1	PAC 5119	DELAY LINE	PAC	DL1
16	1	PA2383	INDUCTOR, 1mH, 600mA	NESS	L1
17	2	517A0021	TRANSFORMER, SQUARE LOOP	DATARAM	T19, 20
18	1	517A0024	TRANSFORMER, 60μH	DATARAM	T16
19	16	517A0023	TRANSFORMER, 6μH	DATARAM	T1-15, 17

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. B/M 301A0302-0 REV. B
SHEET 2 OF 6

TITLE: B/M DR-101 , 8K x 20

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
20	1	1N4733	DIODE, ZENER, 5.0V	MOTOROLA	VR1
21	192	A501-0005	DIODE, SIGNAL	DATARAM	
22	13	517A0025	HYBRID TRANSISTOR PACKAGE	DATARAM	MHQ1-13
23	24	2N3725	TRANSISTOR, NPN, TO-39	MOT./ITT/ NATIONAL	Q1-24
24	1	TIP-33	TRANSISTOR, NPN	T.I.	Q25
25	1	2N4401	TRANSISTOR, NPN	MOTOROLA	Q26
26	11	150D156X0020B2	CAPACITOR, 15µF, 20V, TANTALUM ELECTROLYTIC	SPRAGUE	
27	7	150D156X0035B2	CAPACITOR, 15µF, 35V, TANTALUM ELECTROLYTIC	SPRAGUE	C91-97
28	10	43212-11210	CAPACITOR, 10µF, TANTALUM ELECTROLYTIC	TAG	C51-60
29	20	CK05BX680K	CAPACITOR, 68pF, CERAMIC, 10%		C21-40
30	10	CK05BX151K	CAPACITOR, 150pF, CERAMIC, 10%		C41-50
31	41	CK06BX104M	CAPACITOR, .1µF, CERAMIC, 20%		
33	4	CK05BX821M	CAPACITOR, 820pF, CERAMIC, 20%		C114-C117
34	20	CK05BX152M	CAPACITOR, 1500pF, CERAMIC, 20%		C71-90
35	20	RCL-TR-N-7	RESISTOR, 18Ω, 7W, 1%, N.I.	RCL	R16-35

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. B/M301A0302-0 REV. B
SHEET 3 OF 6

TITLE: B/M DR-101, 8K x 20

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
20	1	1N4733	DIODE, ZENER, 5.0V	MOTOROLA	VR1
21	192	A501-0005	DIODE, SIGNAL	DATARAM	
22	13	517A0025	HYBRID TRANSISTOR PACKAGE	DATARAM	MHQ1-13
23	24	2N3725	TRANSISTOR, NPN, TO-39	MOT. / ITT / NATIONAL	Q1-24
24	1	TIP-33	TRANSISTOR, NPN	T. I.	Q25
25	1	2N4401	TRANSISTOR, NPN	MOTOROLA	Q26
26	11	150D156X0020B2	CAPACITOR, 15µF, 20V, TANTALUM ELECTROLYTIC	SPRAGUE	
27	7	150D156X0035B2	CAPACITOR, 15µF, 35V, TANTALUM ELECTROLYTIC	SPRAGUE	C91-97
28	10	43212-11210	CAPACITOR, 10µF, TANTALUM ELECTROLYTIC	TAG	C51-60
29	20	CK05BX680K	CAPACITOR, 68pF, CERAMIC, 10%		C21-40
30	10	CK05BX151K	CAPACITOR, 150pF, CERAMIC, 10%		C41-50
31	41	CK06BX104M	CAPACITOR, .1µF, CERAMIC, 20%		
33	4	CK05BX821M	CAPACITOR, 820pF, CERAMIC, 20%		C114-C117
34	20	CK05BX152M	CAPACITOR, 1500pF, CERAMIC, 20%		C71-90
35	20	RCL-TR-N-7	RESISTOR, 18Ω, 7W, 1%, N.I.	RCL	R16-35

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. B/M301A0302-0 REV. B
SHEET 3 OF 6

TITLE: B/M DR-101 8K x 20

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
36	1	RCL-NT-5/ 165	RESISTOR, 62Ω, 5W, 1%, N.I., W.W., FREON RESISTANT	RCL/ RONEL	R49
37	2	RCL-NT-2A/ 135	RESISTOR, 2Ω, 3W, 1%, N.I., W.W., FREON RESISTANT	RCL/ RONEL	R116, 119
38	2		RESISTOR, 10Ω, 1/10W, 1%, M.F., PRECISION	DALE	R46, 47
39	1		RESISTOR, 2.43K, 1/10W, 1%, M.F. PRECISION	DALE	R48
40	2		RESISTOR, 200Ω, 1/4W, 5%, CARBON	ALLEN BRADLEY	R125, 126
41	1		RESISTOR, 270Ω, 1/4W, 5%, CARBON	ALLEN BRADLEY	R127
42	1		RESISTOR, 470Ω, 1/4W, 5%, CARBON	ALLEN BRADLEY	R128
43					
44					
45	2		RESISTOR, 1K, 1/4W, 5%, CARBON	ALLEN BRADLEY	R118, 129
46	1		RESISTOR, 4.7K, 1/4W, 5%, CARBON	ALLEN BRADLEY	R115
47	1	3067P-1-102	POTENTIOMETER, 1K	BOURNS	R117

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. B/M 301A0302-0 REV. B

TITLE: B/M DR-101 8K x 20

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
48	6	517B0017-08	RESISTOR MODULE, 470Ω, 5%	CTS	
49	16	517B0017-07	RESISTOR MODULE, 100Ω, 5%	CTS	
50	10	517B0018-01	RESISTOR MODULE, 100Ω, 5%	CTS	
51	8	517B0017-01	RESISTOR MODULE, 30Ω, 5%	CTS	
52	6	517B0017-03	RESISTOR MODULE, 47Ω, 5%	CTS	
53	5	517B0016-03	RESISTOR MODULE, 220Ω, 5%	CTS	R50-54
54	2	517B0017-05	RESISTOR MODULE, 270Ω, 5%	CTS	R109, 114
55	1	517B0018-03	RESISTOR MODULE, 390Ω, 5%	CTS	R121
56	6	517B0018-03	RESISTOR MODULE, 390Ω, 5%	CTS	USED ON SYS. W/ SUFFIX "T" ONLY
57	7	517B0018-05	RESISTOR MODULE, 470Ω, 5%	CTS	USED ON SYS. W/ SUFFIX "T" ONLY
58	5	517B0022	MINI BUSS		
59	118	85423-2	RECEPTACLE, MOD I (LOOSE PIECE)	AMP	

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. B/M 301A0302-0 REV. B

TITLE: B/M DR-101 8K x 20

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
60	24-	NF 204	HEAT SINK	WAKEFIELD	ITEM #23
61	24		TRANSISTOR PAD		ITEM #23
62	1	305E0500	P. C. BOARD		
63	2	6100	CARD EJECTOR w/ROLL PIN		
64	1		SCREW, #4-40 PHILIPS PANHEAD 5/16 LG, STEEL, CADMIUM PLATED		ITEM #24
65	1	IN746	DIODE, ZENER, 3.3V	MOTOROLA	VR2
66	7	22NTM	ELASTIC STOP NUT #4-40	ESNA	
72	3		SCREW, #2-56 PHILIPS PANHEAD 3/16 LG, STEEL, CADMIUM PLATED		ITEM #70
67	7		WASHER #4 NYLON		
68	1	201-0337	STACK ASS'Y	DATARAM	
69	2	2024C	TERMINAL, TURRET	H. H. SMITH	
70	1	306B0522	STIFFENER BAR	DATARAM	
71	AR		WIRE, #24 TEFLON INSULATED		

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
PRINCETON NEW JERSEY

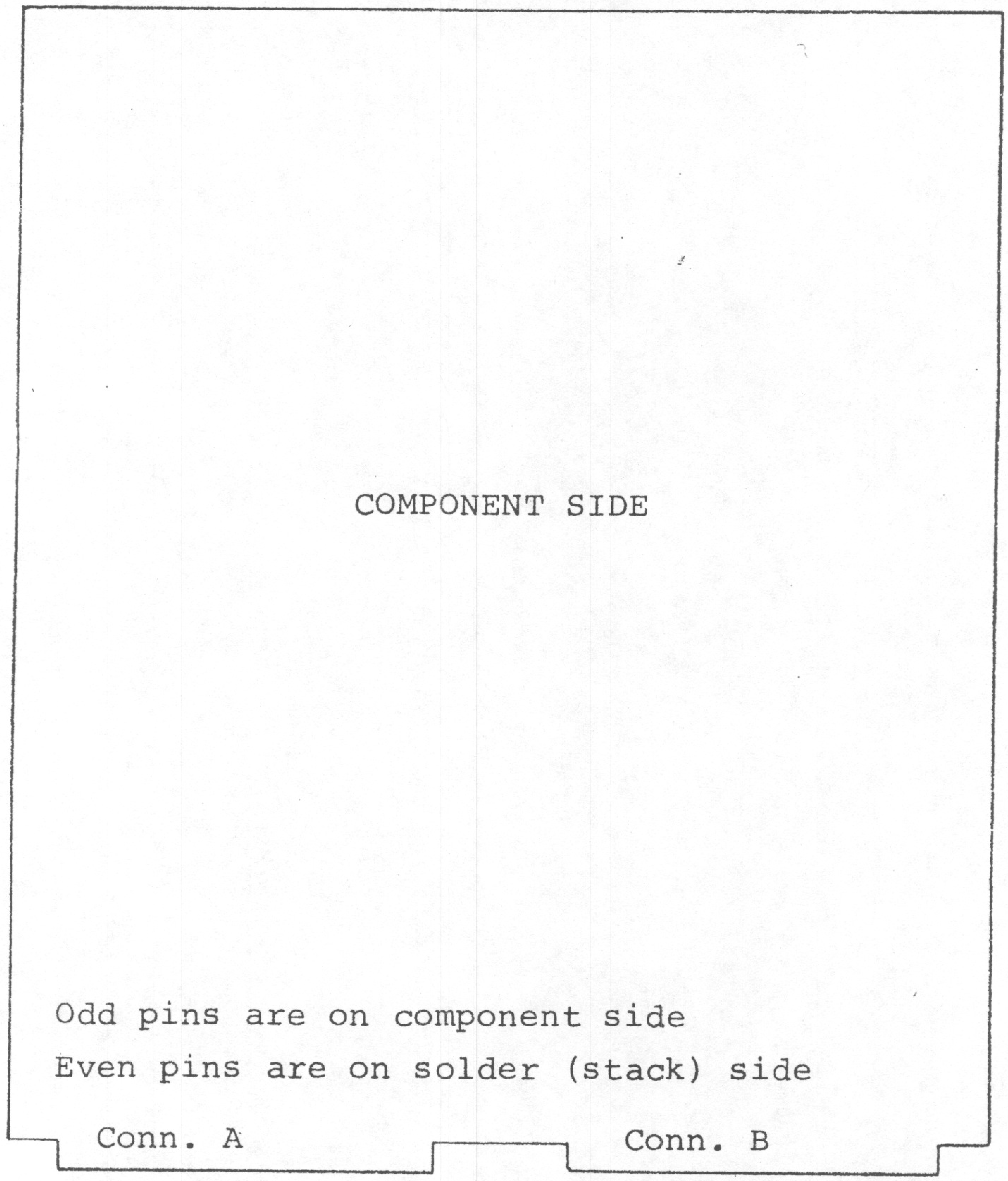
DWG. NO. B/M 301A0302-0 REV. B
SHEET 6 OF 6

REV. B

DWG. NO. 308A0041 SHEET 1 OF 5

REVISIONS

SYM.	SHEET	DESCRIPTION	APPROV.	DATE
A	ALL	ADD 12,16,18 Bit Configurations	BJH	2-24-72
B	3, 4	Added 65K Interface	BJH	3-29-72



DRAWN	DATE	TITLE
PD	1/27/72	Interface Connection List DR-101
CHECKED	DATE	Core Memory System
RDS	1/27/72	4K, 8Kx12,16,18,20
ENGR	DATE	
BJH	1/27/72	
APPROVED	DATE	
BJH	1/27/72	

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. 308A0041 REV. B
SHEET 1 OF 5

-DATA-

Byte Orientation:

Byte	20 BIT	18 BIT	16 BIT	12 BIT
1	1-10	1-9	1-8	1-6
2	11-20	10-18	9-16	7-12

		20 BIT	18 BIT	16 BIT	12 BIT
DATA IN BIT	1	A80	A80	A80	A80
Data in Bit	2	A74	A74	A74	A74
Data in Bit	3	A37	A37	A37	A37
Data in Bit	4	A36	A36	A36	A36
Data in Bit	5	A72	A72	A72	A72
Data in Bit	6	A35	A35	A35	A35
Data in Bit	7	A33	A33	A33	A30
Data in Bit	8	A31	A31	A31	A28
Data in Bit	9	A34	A34	A29	A25
Data in Bit	10	A2	A32	A27	A41
Data in Bit	11	A4	A29	A30	A38
Data in Bit	12	A32	A27	A28	A39
Data in Bit	13	A29	A30	A25	Not used
Data in Bit	14	A27	A28	A41	Not used
Data in Bit	15	A30	A25	A38	Not used
Data in Bit	16	A28	A41	A39	Not used
Data in Bit	17	A25	A38	Not used	Not used
Data in Bit	18	A41	A39	Not used	Not used
Data in Bit	19	A38	Not used	Not used	Not used
Data in Bit	20	A39	Not used	Not used	Not used

Data Out Bit	1	A47	A47	A47	A47
Data out Bit	2	A49	A49	A49	A49
Data out Bit	3	A45	A45	A45	A45
Data out Bit	4	A55	A55	A55	A55
Data out Bit	5	A53	A53	A53	A53
Data out Bit	6	A51	A51	A51	A51
Data out Bit	7	A57	A57	A57	A69
Data out Bit	8	A59	A59	A59	A71
Data out Bit	9	A61	A61	A65	A73
Data out Bit	10	A83	A67	A63	A79
Data out Bit	11	A81	A65	A69	A77
Data out Bit	12	A67	A63	A71	A75
Data out Bit	13	A65	A69	A73	Not used
Data out Bit	14	A63	A71	A79	Not used
Data out Bit	15	A69	A73	A77	Not used
Data out Bit	16	A71	A79	A75	Not used
Data out Bit	17	A73	A77	Not used	Not used
Data out Bit	18	A79	A75	Not used	Not used
Data out Bit	19	A77	Not used	Not used	Not used
Data out Bit	20	A75	Not used	Not used	Not used

-TIMING AND CONTROL SIGNALS-

Memory Start Command	(MSC)	B37
Start Write Command	($S\overline{W}C$)	B45
Full Cycle Mode	($F\overline{C}M$)	B41
Read Restore 1	(R/R1)	B29
Read Restore 2	(R/R2)	B25
Data Retain	(DR)	B39
Memory Busy	($\overline{M}B$)	B35
Data Available	(DA)	B1
System Enable 1	(SE1)	B43
System Enable 2	(SE2)	B44
System Enable 3	(SE3)	B60

-ADDRESS-

Bit	A0	B68	
Bit	A1	B76	
Bit	A2	B78	
Bit	A3	B70	
Bit	A4	B80	
Bit	A5	B82	
Bit	A6	B72	
Bit	A7	B71	
Bit	A8	B73	
Bit	A9	B74	
Bit	A10	B75	
Bit	A11	B77	
Bit	A12	B79	For 8K
Bit	A13	B81	For 16K Expansion
Bit	A14	B67	For 32K Expansion
Bit	A15	B62	

-POWER AND GROUND-

+5 Volts DC	B85, B86
Logic Ground	A85,A86,B83,B84
-18 Volts DC	A15, A17
Power Ground	A1, A3, A5

NOTE: When twisted pair is used for signal lines, pins A85 and A86 should be used for Data input/output ground return terminations and pins B83 and B84 should be used for address, timing and control groúnd return terminations.

DATARAM CORPORATION

MANUFACTURERS OF MEMORY PRODUCTS

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