Honeywell Bull DPS 8 Series

CHARACTERISTICS

UPDATE: *The DPS 8 Series is no longer actively marketed, but upgrades are still available. The DPS 8000 Series, announced in 1987, has since replaced the DPS 8. For your convenience, we are reprinting the DPS 8 Characteristics section and the DPS 8 hardware price list. For information and full pricing on Honeywell Bull peripherals and operating systems software, please refer to the other Honeywell Bull hardware reports appearing in this tab.*

MANUFACTURER: Honeywell Bull Inc., Deer Valley Computer Park, 13430 North Black Canyon Highway, Phoenix, Arizona 85029. Telephone (602) 862-8000. In Canada: 155 Gordon Baker Road, Willowdale, Ontario M2H 3N7. Telephone (416) 499-6111.

MODELS: DPS 8/47, 8/47C, 8/49, 8/49C, 8/52, 8/52C, 8/62, 8/62C, 8/70, 8/70C, 8/70M.

DATA FORMATS

BASIC UNIT: 9-bit bytes organized functionally to process 36-bit (word) groupings of information. Special features are also included for ease in manipulating 4-bit groups; 6-bit, 9-bit, and 18-bit groups; and 72-bit double-precision groups.

FIXED-POINT OPERANDS: Binary fixed-point numbers are represented with 18-bit half-word, 36-bit single-word, and 72-bit double-precision operands.

Decimal numbers used directly in hardware arithmetic commands are expressed as decimal digits in either the four-bit or nine-bit character format. They are expressed as unsigned numbers or as signed numbers using a separate sign character.

Alphanumeric data is represented by 9-bit, 6-bit, or 4-bit characters. A machine word contains either four, six, or eight characters, respectively.

FLOATING-POINT OPERANDS: Binary floating-point numbers are represented with 36-bit single-word and 72-bit double-precision operands. In both operands, 0 represents the sign of the exponent, bits 1 to 7 the exponent, and bit 8 the sign of the fraction. The rest of the operand starting with bit 9 represents the rest of the fraction.

INSTRUCTIONS: All basic instructions use one 36-bit word. The processor performs operations using 6-, 9-, 18-, 36-, and 72-bit operands. All single-word instructions use bits 0 through 17 for the address field, bits 18 through 27 for the op code, bit 28 as the interrupt inhibit bit, bit 29 as the address register bit, and bits 30 through 35 as the instruction address modifier. Multiword instructions use bits 0 through 17 for various functions as required, bits 18 through 27 as the op code, bit 28 as the interrupt inhibit bit, and bits 29 through 36 as the operand descriptor one modification field. Words two, three, and four contain the operand descriptor of indirect pointer for operands, one, two, and three, respectively.

INTERNAL CODE: 9-bit ASCII code is standard.

The DPS 8 Series is Honeywell Bull's family of medium-to-large scale, general-purpose, software-compatible processors, which are no longer actively marketed.

MODELS: DPS 8/47, 8/47C, 8/49, 8/49C, 8/52, 8/52C, 8/62, 8/62C, 8/70, 8/70C, 8/70M.
CONFIGURATION: The DPS 8 systems can have from 8 to 64 megabytes of memory, one to six CPUs, and up to 54 channel slots per I/O processor.
COMPETITION: Amdahl 580; IBM 4300, 308X; NAS AS/8000, AS/9000; NCR V-8600; Sperry 1100 Series.
PRICE: Purchase prices range from $153,000 for a DPS 8/47 central system to $800,000 for a DPS 8/70C central system.

MAIN MEMORY

The DPS 8 Series uses solidstate main memories and cache memories. Main memories feature automatic error detection and correction.

STORAGE TYPE: Metallic oxide semiconductor (MOS).

CAPACITY: See Table 1.

CYCLE TIME: Honeywell Bull does not disclose cycle times.

CHECKING: A 5-bit error-correcting Hamming code is appended to each 36-bit word. Single-bit errors are corrected automatically, and multiple-bit errors are detected and flagged for subsequent error-recovery routines. Odd parity is utilized throughout the processor.

RESERVE STORAGE: DPS 8 systems use a four-level ring protection scheme that is implemented in system firmware with supporting hardware registers. Each user program segment has an associated segment descriptor that is stored in tables in main memory. Within each segment descriptor are two 2-bit fields that specify the security level required by a user program to execute or write to a particular segment. Hardware also checks that data addresses generated during program execution do not exceed specified boundaries. The segment descriptors also contain two bits that can deny execution or write access to a user program.

CENTRAL PROCESSORS

The DPS 8 central processors employ a memory-oriented structure with from one to four system control units (SCUs) managing the communications between system components and servicing all demands on main memory by other system components. An I/O multiplexer (IOM) (at the DPS 8/47 and 8/49 level) and a FIPS-compliant Input/Output Processor (IOP) (at the DPS 8/52, 8/62, and 8/70 level) interface the peripheral processors and front-end communi-

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cations processors with the system control units. The units also control data transfers between I/O devices and main memory concurrently with program execution.

Each processor module in the system has full program execution capability and conducts all actual computational processing (data movement, arithmetic, logic, comparison, and control operations) within the information system. The processor, which communicates only with the system control unit(s) and associated memory, consists of an operations unit, a control unit, a decimal unit, and a virtual unit. The operating unit executes arithmetic and logical operations; the control unit performs instruction fetching, address preparation, memory protection, and data fetching/storing; the decimal unit operates in association with the control unit to execute decimal instructions; and the virtual unit prepares addresses for use in the virtual memory mode. These units operate with relative independence and maximum overlap to provide a high rate of instruction execution.

Virtual memory under GCOS 8 and CP-6 provides an extremely large, directly addressable memory space and a complement of registers and instructions to enable management of virtual address space. The hardware environment for virtual memory is composed of four elements: working spaces, domains, segments, and pages. The working spaces and pages are physical elements, and the segments and domains are logical elements. They are treated as separate components of the virtual memory but must be interpreted in the context of the entire environment, as they are closely related in their interaction with each other.

Virtual memory is divided into approximately equal parts called working spaces. A working space has an associated page table that identifies the real memory location. There are 512 working spaces in memory, each of which contains 1,024 words (4096 bytes). They are used for memory management. Segments are logical elements that reside within a working space and vary in length from one byte to one or more pages. Segments and pages can be compared to a tape file and a tape reel in that a page (tape reel) may contain several segments (files) or a segment (file) may comprise several pages (tape reels). A domain includes more than one noncontiguous segment in one or more working spaces.

All DPS 8 processors use a high-speed cache memory. If an instruction or data to be referenced by the central processor is available in the cache memory, the information can be retrieved from the cache rather than from main memory, which reduces access time and contention. This process increases the effective system throughput.

DPS 8 hardware architecture is memory centered with processors and IOM or IOP using a common memory subsystem and interface through a SCU. This architecture is designed to support simultaneous and asynchronous execution for maximum throughput. To support the distributed systems environment (DSE), one or more front-end network processors (FNPs) are used in the DPS 8 family. The FNP controls all remote terminal interaction with DPS 8 systems. It is connected to the central system via an IOM or IOP and provides the various interfaces required by the elements and protocols of a distributed system as well as a facility for communication with the host system. By performing message management and message handling, the FNP frees the host for other processing functions. The resources of the central system are called upon only when a message is submitted for processing.

Each DPS 8 processor includes a large number of processor-accessible registers, as shown in the following table:

	Length (bits)	Quantity
Accumulator	36	1
Quotient	36	1
Accumulator-Quotient	72	1
Exponent	8	1
Index	18	8
Indicator	18	1
Time	24	1
Instruction Counter	18	1
Address	24	8
Mode	33	1
Cache Mode	28	1
Fault	72	1
Control Unit History	72	16
Operations Unit History	72	16
Decimal Unit History	72	16
Virtual Unit History	72	16
Working Space	9	8
Safe Store	72	1
Linkage Segment	72	1
Argument Stack	72	1
Parameter Stack	72	1
Instruction Segment	72	1
Operand Descriptor	72	8
Segment Identity	12	8
Instruction Segment Identity	12	1
Pointer	—	8
Data Stack Descriptor	72	1
Data Stack Address	17	1
Page Directory Base	15	1
Option	3	1
Pointer and Length	36	8

The DPS 8 uses virtual memory which provides the processor with a directly addressable virtual space of 2^{43} bytes. It also includes the capability of translating the virtual address to a real memory address. Two different addressing modes are provided: absolute and paging. In the absolute addressing mode, a virtual address is generated but is not mapped to a real address. The paging mode maps the virtual memory address to a real memory address.

After a virtual address has been mapped to a real address, the information is stored in the cache (or associative) memory. The amount of this memory varies with the processors. The DPS 8/47, 8/49, 8/52, 8/62, and 8/70 each have 32 kilobytes of cache area. The corresponding DPS 8/C and 8/M models contain the same amount of cache memory. When a new address not contained in the cache has been mapped and the cache memory is full, the new entry replaces the oldest using a first-in/first-out algorithm.

DPS 8 processors have a comprehensive instruction set for performing data movement, binary arithmetic, shifting, logic, and control operations. The instruction set includes arithmetic facilities for performing variable-length fixed- and floating-point decimal arithmetic, and bit and byte string manipulation for processing bytes, BCD characters, packed decimal data, and bit strings.

The basic instruction set has a total of 289 instructions, which include 88 fixed-point binary arithmetic, 20 address register, 29 Boolean, 2 descriptor register, 10 master mode, 17 micro, 29 multiword, 4 pointer register, 18 privileged, 20 transfer of control, and 18 miscellaneous operations.

The central processor operates in three modes: master mode, privileged master mode, and slave mode. Master and privileged master modes are reserved for GCOS 8. They allow unrestricted access to all memory, permit initiation of data transfer operations through the IOMs, and permit the

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TABLE 1. SYSTEM COMPARISON

MODEL	DPS 8/47	DPS 8/49	DPS 8/52	DPS 8/62	DPS 8/70
SYSTEM CHARACTERISTICS					
Date announced	First-Quarter 1983	First-Quarter 1983	October 1979	October 1980	October 1979
Date first delivered	First-Quarter 1983	First-Quarter 1983	Second-Quarter 1980	Third-Quarter 1981	Second-Quarter 1980
Field upgradable to	8/49	See footnote*	8/62	8/70	DPS 88 or DPS 90 Series
Relative performance	0.65	0.95	0.95	1.3	1.7
Number of processors	1-2	1-4	1-2	1-2	1-6
Cycle time, nanoseconds	Not specified	Not specified	Not specified	Not specified	Not specified
Word size, bits	36	36	36	36	36
Operating systems	GCOS, GCOS 8, CP-6	GCOS, GCOS 8, CP-6	GCOS, GCOS 8, CP-6	GCOS, GCOS 8, CP-6	GCOS, GCOS 8, CP-6, Multics
MAIN MEMORY					
Type	64K-bit MOS	64K-bit MOS	64K-bit MOS	64K-bit MOS	64K-bit MOS
Minimum capacity, bytes	8-12M	8-16M	8-16M	8-16M	8-16M
Maximum capacity, bytes	32M	32M	32-64M	32-64M	32-64M
Increment size	2M	2M	2M	2M	2M
Cycle time, nanoseconds	750	750	750	750	750
BUFFER STORAGE					
Minimum capacity	32KB	32KB	32KB	32KB	32KB
Maximum capacity	32KB	32KB	32KB	32KB	32KB
Increment size	—	—	—	—	—
INPUT/OUTPUT CONTROL					
Number of channels:					
Byte multiplexer	—	—	—	—	—
Block multiplexer	—	—	—	—	—
Word	—	—	—	—	—
Other	20	20	36-54	36-54	36-54

Upgrading from a DPS 8/49 to a larger processor involves a processor swap out.

setting of control registers. Slave mode is used by GCOS 8 when appropriate, and for the execution of all user programs. Programs executing in slave mode cannot perform certain control operations. This trimodal operation provides effective operating control and security in a multiprogramming environment.

In DPS 8 systems, every external interrupt or internal fault results in the setting of a specific interrupt cell in the system controller. The interrupt cells are organized in a numbered priority chain. Any active system module connected to a system controller port may request the setting of an interrupt cell. Each system controller contains 32 interrupt cells.

One system control center is required for the DPS 8. The CSU6601 is a desktop arrangement with a 120-character-per-second (cps) printer and a 12-inch, 1,920-character CRT and keyboard. A 23-inch remote display is optional. Also available are the larger CSU6004, with a 30 cps printer and an optional 23-inch remote display unit, and the CSU6005, which has two 12-inch screens with an option for up to two 23-inch remote displays. The keyboard, common to all consoles, is a solidstate unit with an alphanumeric keyboard consisting of 26 alphabetic, 10 numeric, and 28 special character keys. A 120 cps option is available for the CSU6004 and CSU6005 printers.

Additional CSU6601 options include the CSU6602 Auxiliary Console with 120 cps printer and keyboard, CSF6602 Auxiliary Keyboard Display Attachment Feature, CSF6603 Additional Keyboard Display, CSF6604 Large Screen Monitor (the 23-inch monitor), and CSF6606 Extended System Control Center.

SPECIAL FEATURES: In addition to the widely used GCOS operating systems, Honeywell Bull made separate DPS 8 mainframe versions to accommodate CP-6 or Multics operating systems. The five CP-6 models are part of the DPS 8C Series, and the single Multics processor is called the DPS 8/70M.

PHYSICAL SPECIFICATIONS: DPS 8 systems must be located in a room with a raised floor or equivalent. The room ceiling must be 8.5 feet above the raised floor, with at least 8 to 12 inches between the subfloor and raised floor. Power requirements must meet these specifications: a voltage of 208, 240, 440, or 480 V AC ±10 percent for the motor generator set; 60 Hertz nominal with 60.5 maximum and 59.4 minimum frequency; three-phase wire with a maximum phase variation of 5 percent from the nominal; and 120/208 V AC, five-wire cable with ground for peripheral equipment (voltage variation is ±10 percent).

A design temperature between 68 and 78 degrees Fahrenheit with a relative humidity between 40 and 60 percent noncondensing is permissible, although a temperature of 73 degrees with a relative humidity of 50 percent is recommended. Once a temperature and relative humidity are selected, the temperature should not fluctuate more than ±2 degrees Fahrenheit or the relative humidity more than ±5 percent.

CONFIGURATION RULES

DPS 8/47 and 8/49 central systems are packaged within a single cabinet. The DPS 8/47 (CPS8130) and DPS 8/49 (CPS8132) are equipped with eight megabytes of main memory, one CPU, one system control unit (SCU), and one IOM with 20 channel slots. An additional CPU can be configured with the DPS 8/47, and up to three additional CPUs can be configured with the DPS 8/49. One additional SCU and IOM can be configured on the DPS 8/47 and 8/49 to provide a tandem system with all central system units cross-connected. CP-6 models, DPS 8/47C (CPS8119) and 8/49C (CPS8121), have 12 megabytes and 16 megabytes of memory, respectively. Memory on all DPS 8/47 and 8/49 models can be increased to 32 megabytes. All systems are field upgradable.

The central cabinet can include one MSP8000 or MSP8002, and only one MFP8001, MTP8001, or URP8001, since these three units are mutually exclusive. With the addition of a second IOM on the DPS 8/47,

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8/47C, 8/49, and 8/49C, additional integrated peripheral processors can be added in the second cabinet. Additional freestanding peripheral processors can be added as desired.

The DPS 8/52, DPS 8/62, and DPS 8/70 each have a freestanding central system. The DPS 8/52 (CPS8181), DPS 8/62 (CPS8186), and DPS 8/70 (CPS8189) have four megabytes of main memory each, one CPU, one IOM with 36 available slots (an optional unit provides up to 54 slots), and one SCU. Memory on these large systems can be increased in increments of two megabytes (CMM8020) on all processors. Maximum memory capacity for the DPS 8/52, 8/62, and 8/70 operating with GCOS is eight megabytes. When operating with GCOS 8 and Multics, the maximum is 32 megabytes for the DPS 8/52 and 8/62, and 64 megabytes for the DPS 8/70 and 8/70M. The DPS 8/52 and 8/62 can be field upgraded to the DPS 8/70. The DPS 8/52 and 8/62 support up to four FNPs (DCU6661/8010) and four System Consoles (CSU6601, CSU6004, or CSU6005). Up to two CPUs, SCUs, and IOMs are offered for the DPS 8/52 and 8/62.

The DPS 8/70 can support up to eight FNPs and four System Consoles, using the same peripherals as above. The system is expandable to four CPUs, four IOMs, and four SCUs. The DPS 8/70M supports up to six CPUs, two IOMs, and four SCUs. Honeywell Bull recommends multiple SCUs for optimal performance.

For CP-6, the DPS 8/52C, 8/62C, and 8/70C each have a freestanding central system. The DPS 8/52C (CPS8173), DPS 8/62C (CPS8174), and DPS 8/70C (CPS8178) have 16 megabytes of main memory. Each has one CPU, one IOM with 36 available slots (expandable to 54 slots), and one SCU. Memory on each of these large processors can be increased in increments of 2 megabytes (CMM8020) up to a maximum of 64 megabytes. The DPS 8/52C and 8/62C can all be field upgraded to the DPS 8/70C. The DPS 8/52C, 8/62C, and 8/70C can have three additional SCUs and three additional IOMs. The DPS 8/70C can have up to five additional CPUs. The DPS 8/52C, 8/62C, and 8/70C support up to 16 Datanet 8/C FNPs. One FNP is included with each system.

Most peripherals and freestanding peripheral processors available on the Level 66/DPS systems are compatible with the DPS 8/52, 8/52C, 8/62, 8/62C, 8/70, 8/70C, and 8/70M.

INPUT/OUTPUT CONTROL

The Input/Output Multiplexer or Input/Output Processor coordinate all input/output operations between the system control unit, peripheral subsystems, and Datanet 6661, Datanet 8, or Datanet 8/C Series Front-End Network Processors (FNPs) and document processors. The IOM works with 8/47 and 8/49 systems, while the IOP works with the larger 8/52, 8/62, and 8/70 systems. The IOM or IOP also handles data transfers between peripheral devices and memory. IOP is sized to handle the MSU3380 disk products and the MTS8200 magnetic tape products that are attachable to only the 8/52, 8/62, and 8/70 systems. All peripheral device operations are controlled by processor-prepared control word lists stored in reserved IOM positions in memory or in the IOM scratch pad memory, except DPS 6 peripherals that are controlled via the Datanet 8/C in DPS 8/C systems.

The IOM consists of the IOM central and a variable number of channels. The IOM central controls access to storage for each of the channels and can perform one storage access cycle at a time through the appropriate system control unit. The IOM central is time-shared by a number of channels operating concurrently.

The IOM contains scratch pad storage which provides higher speed servicing of data transfers through the data channels and reduces the number of data accesses required for control word retrieval and updating.

Peripheral Subsystem Interface (PSI) channels provide connection between the IOM and various peripheral controllers. Multiple logic channels (up to eight) can be assigned to a single PSI channel for concurrent multiple unit operation. The PSI channel can transfer data at up to 1,600,000 bytes per second.

Total data rate is either 675,000 words (2,700,000 bytes) per second or 1,000,000 words (4,000,000 bytes) per second, depending on the processor model.

All IOM operations are performed asynchronously with program processing. Interference occurs only when two or more IOMs or processors attempt to access the same main storage module.

DPS 8 uses several peripheral processors: mass storage processors, a multifunction processor (which handles tape units, card readers/punches, and printers) available only on the 8/47, 8/49, 8/47C, and 8/49C, and separate magnetic tape and unit record processors. The DPS 8/47 and 8/49 can be configured with either integrated peripheral processors contained within the central system cabinet, freestanding peripheral processors, or a combination of both. The DPS 8/52, 8/62, and 8/70 can be configured only with freestanding peripheral processors. All systems can have an FNP to support a variety of remote devices and communications links.

MASS STORAGE

For information about the latest Honeywell Bull disk storage devices, please refer to the Honeywell Bull DPS 8000 and DPS 90 reports in this tab.

INPUT/OUTPUT UNITS

For information about magnetic tape subsystems and printers, please refer to the Honeywell Bull DPS 8000 and DPS 90 reports in this tab.

TERMINALS

For information about terminals, please refer to the Honeywell Bull DPS 8000 and DPS 90 reports in this tab.

COMMUNICATIONS

For information about the latest Honeywell Bull communications equipment, please refer the DPS 8000 and DPS 90 reports in this tab.

SOFTWARE

OPERATING SYSTEM: The Honeywell *GCOS 8 (General Comprehensive Operating Supervisor 8)* is the primary DPS 8 operating system. For the latest information about GCOS 8, please refer to the DPS 8000 and DPS 90 reports in this tab.

DPS 8/C computer systems use the *Control Program-6 (CP-6)* software and operating system. CP-6 is a Honeywell Bull enhancement of the Xerox-developed CP-5 operating system used on larger Xerox processors. CP-6

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includes facilities for interactive time-sharing, on-line transaction processing, and multiprogrammed local and remote batch processing.

CP-6 provides a memory mapping system for up to 512 program working spaces and for addressing up to 16 megawords. User instruction segments can be up to 224,000 words, while data segments can be up to 384,000 words. CP-6 also provides three-level protection for user context segments and hardware management.

An event-driven scheduler reduces system overhead. The scheduler helps make more CPU cycles available to user-related activities. Communications processing is distributed to local and remote front-end processors based on Honeywell Bull's current minicomputer technology. CP-6 takes advantage of DPS 8 large-memory technology with addressing to 64 million bytes to facilitate rapid response to on-line interactions.

The complete CP-6 system provides a single program interface to all services and an extensive array of productivity features including on-line program development and debugging, high-level, advanced programming languages, data base management systems, friendly terminal user interfaces, an on-line HELP facility, and a query and report language.

CP-6 provides a common command language that is used for initiating and controlling tasks in all processing modes. This design helps simplify program development activities and helps facilitate transportability of programs from one mode to another.

The operating system can support up to 500 current time-sharing users, while the multiprogramming batch processing facility can process up to 500 batch streams concurrently. Batch jobs may be submitted to the system through a central site card reader, from an on-line terminal, or from a remote site via the remote batch facility. The spooling system can help improve throughput by eliminating bottlenecks associated with slow-speed unit record peripherals. All batch jobs form a priority-ordered queue and are processed when program-specified resources become available. Remote batch processing permits flexible communications between CP-6 and a variety of remote terminals. These terminals can range from a simple card reader/card punch/line printer combination to other computer systems with varieties of peripheral devices. CP-6 can communicate as a host system with many terminals and computers at various sites and simultaneously act as a remote terminal to other computers.

The DPS 8/70M system uses Honeywell Bull's *Multics* operating system. Multics is a specially designed virtual memory operating system that offers remote terminal access as the primary means of entering the system, multiprocessing with dynamic reconfiguration capabilities, and a unique hardware-based ring structure that provides security for sharing of programs and data. It also has a tree-structured hierarchy for organization of user and system storage and the availability of multiple programming environments and user interfaces within a single system. It accommodates batch and time-sharing through a common command language and is written primarily in PL/1.

Later Multics releases, MR 11.0 and MR 12.0, were shipped in 1985 and 1986, respectively. These releases contained enhancements for transaction processing, data base software, and the C compiler. Other enhancements involve support for larger capacity 3380 disk drives, purchased on an OEM basis from IBM, and PC support. Another major improvement centers around operating system security features. Because of this work, the operating system has earned a U.S. Department of Defense B2 security rating.

Information in the Multics system's virtual memory is organized in variable-length segments. Each segment can contain either programs or data or can be a directory; i.e., a catalog of related segments represented in tree structure. Segments are directly addressable by a symbolic name. Multics hardware uses a segment descriptor to determine the absolute address of the segment and its access attributes. Any word, character, or bit within a segment can be referenced by its location within the segment. Segments can reside anywhere in main memory and can alter their size independently of other segments.

Multics uses demand paging to determine which portions of a segment are to be present in main memory. Segments are automatically divided into fixed-size pages of 1,024 words, and paging is performed automatically by the Multics hardware, so that only the currently accessed pages of a segment are required in main memory.

Multics performs all input/output operations automatically. The programmer is required to supply the symbolic name of the segment and the address of the desired item within the segment, or the relative address stated in the terminology of a higher level language. A device-independent input/output system is available that permits interchangeable reading and writing on magnetic tapes, communication terminals, cards, printers, and storage system segments through the use of symbolic names. User output can be automatically queued for printer or punched card output. User-written input/output routines can also be accommodated by the system.

Controlled sharing of programs and data is facilitated by the Multics ring structure, a unique security scheme that is implemented as an integral part of the segmentation and paging scheme. The ring structure in conjunction with the segment access control list permits programs to access another owner's data base only through an owner-supplied program that specifies what data can be referenced and what operations can be performed.

CP-6 PROGRAMMING LANGUAGES: ANSI Fortran, Cobol-74, APL, Basic, RPG II, and PL-6.

MULTICS PROGRAMMING LANGUAGES: PL/1, APL, Cobol-74, MRPG, Fortran-77, Basic, C, and Assembly Language for Multics (ALM).

CP-6 DATA BASE MANAGEMENT: CP-6 uses I-D-S/II, a data base management system that can be a combination of singular, tree, hierarchical, and network structures. The system can contain up to 68 billion records. Other CP-6 data base components include *Data Manipulation Language*, a procedural language for jobs accessing the data base, and *Data Definition Language*, a high-level language that is used to describe the areas, sets, records, and data items of the data base.

A Relational System (ARES), also used under CP-6, is a data base management system designed for both programmers and nonprogrammers. Under ARES, data are arrayed in tabular row-and-column formats. ARES commands are submitted through transactions. Data can be stored, accessed, and updated using Data Manipulation Language. Commands can be executed as a onetime inquiry and discarded, or they can be stored as part of the data base description and executed as needed. Data Definition Language lets users define the data base and change its structure.

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CP-6 DATA MANAGEMENT: CP-6 data management functions are included within Integrated Data Store/II (I-D-S/II).

Interactive Data Base Processor is a query and reporting language that lets users retrieve and display data maintained in the I-D-S/II data bases on-line or any file that can be read sequentially. Users who may not be data processing professionals can take advantage of the product using English-like commands.

MULTICS DATA MANAGEMENT: The *Multics Relational Data Store (MRDS)* functions as a subsystem of the Multics operating software and makes use of the DPS 8 virtual memory and file management subsystems. MRDS includes such features as a relational interface, programming language independence, data definition and program independence, query capability via Logical Inquiry and Update System (LINUS), on-line access and updating, concurrent access and update controls, report generation, and data security maintenance.

LINUS is a facility for accessing data bases from a remote terminal. It uses MRDS for data base access. LINUS uses a high-level nonprocedural language called Linus Language (LILA). It also provides a macro facility, line editor for simplifying data expression development, built-in and user-defined functions, a help facility, a report writing capability, and data security.

CP-6 DATA COMMUNICATIONS: CP-6 distributes communications processing functions to local and remote front-end processors that interact with DPS 8 systems through high-speed connections. This configuration enhances throughput and efficiency in the following ways: Front-end systems release additional host processor time for user programs; such systems provide more efficient hardware for specialized tasks and also achieve time-parallel processing. Additionally, more system modularity allows a closer match between customer requirements and installed capacity.

CP-6 transaction processing environment consists of two elements: the forms program that executes in the communication processor and accepts and verifies the transaction, and the application program that executes on the central system and accesses and updates the data base. These two elements are cooperating processes and result in an efficient design because of the distribution of the executing processes to multiple processors.

The CP-6 transaction processing facilities allow users at remote terminals to enter transactions simultaneously using a common data base. These terminals can operate in character or message mode.

CP-6 is designed to support up to 500 concurrent timesharing users. The command language can help reduce user training requirements and enhance program transportability. Comprehensive language and service facilities let timesharing users create, debug, and execute programs and create, modify, and delete files. File and program security are provided for each user.

MULTICS DATA COMMUNICATIONS: *Multics Communications System (Multics CS)*, network processor software for Multics, manages the transfer of data between the central processor and remote equipment through communications channels. Multics CS resides in both the central system and in the network processor. Among its functions, Multics CS supports terminals and hardware of many manufacturers, connects small systems for satellite applications, and provides security on a per-channel basis through access control segments. The facility features built-in diagnostic and dubugging capabilities for increased system availability. Additionally, the facility permits customization of software for specialized user applications and lets administrators monitor and tune system performance.

CP-6 PROGRAM DEVELOPMENT: CP-6 system aids are distributed in a special account called Account X, which contains approximately 175 user tools. Such tools fall under several categories, including programmer aids, system programmer aids, integration aids, installation management aids, documentation aids, development management aids, and microprocessor support aids.

MULTICS PROGRAM DEVELOPMENT: Multics offers several program development and debugging tools that help programmers develop applications in less time. *Probe* allows programmers to set breakpoints in programs, examine or change the values of program variables, and examine the programs' execution history. *Progress* lets programmers check for loops. *Trace* and *Trace-Stack* allow programmers to examine execution history. *Profile* can detect program inefficiencies.

CP-6 UTILITIES: Available CP-6 utilities include *Linker*, *Peripheral Conversion Language (PCL)*, *Sort/Merge*, *Source Editor*, and *Library Maintenance*. Linker performs requested library searches, performs the required linkages, and produces executable run units. PCL is a media conversion service for moving files in various forms from one peripheral device to another. CP-6 Sort/Merge rearranges the records of a file in predetermined order and combines the records of several ordered files into a single ordered file. The CP-6 Source Editor creates a sequenced source file, copies and renumbers records of a source file, and inserts, deletes, or replaces a record or sequence of records in an existing file. It also performs character string substitution and manipulation on groups of records within an existing file. Library Maintenance permits individual modules of widely used routines to be added, deleted, copied, or replaced within CP-6 libraries.

MULTICS UTILITIES: Utility programs include text editors, debugging aids, performance measurement tools, interuser communication facilities to permit messages to be transmitted among users, and on-line documentation of system software and user programs.

OTHER CP-6 SOFTWARE: *TEXT* command language, designed for nonprogrammers, lets users print various types of documents. Available to users in either batch or on-line mode, TEXT permits the merging of separate names and address files with corresponding documents.

Information Resource Management System, available through McCusker-Bearley Associates Ltd. of Azusa, California, is a generalized information system that provides report writing and data base maintenance capabilities.

AZ7, available through AZREX Inc. of Burlington, Massachusetts, is a dictionary-driven, interactive inquiry and report writing system with optional file maintenance capabilities.

VUE, available through National Information Systems Inc. of Cupertino, California, is an interactive, menu-driven project management system. It supports CPM and precedence project networks and provides for resource and cost tracking. Up to 3,000 activities per project can be supported, and a multiproject capability is available.

Computer Assisted Publications (CAP) includes techniques and programs developed to produce technical manuals and HELP files for customers with in-house publication requirements.

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CP-6 Electronic Mail **allows users to send and receive messages through terminals without generating paperwork. The system provides capabilities for message viewing and manipulation, message preparation, and message transmission.**

Error Logging and Analysis (ELAN) **provides logging functions that record hardware and software problems occurring during system operation. The recorded information, formatted for easy interpretation, helps users detect and prevent potential hardware problems.**

OTHER MULTICS SOFTWARE: Multics provides support for a comprehensive word processing system, *Wordpro*, which includes editing, error correction, and formatting tools for the on-line preparation of documents. Multics also provides an interactive graphics system, supporting both static and dynamic terminals, that permits creation and manipulation of complex graphics structures. The Multics Off-Line Page Processing System (PPS) feature creates a system output tape that can be printed later on a Honeywell Bull PPS.

Multics also has an *Electronic Mail Facility*. This facility offers its users direct, on-line, person-to-person distribution of text. It handles mail ranging from brief memos to multivolume documents and delivers that mail immediately to data terminals or on-line mailboxes.

Emacs (Editor Macros) **is a text editing and screen management facility that features screen blocking for operator monitoring of more than one activity.**

PRICING AND SUPPORT

For your convenience, we have listed the latest available pricing for the DPS 8 Series. Please refer to the other Honeywell Bull reports in this tab for peripheral and software pricing and support policies.

EQUIPMENT PRICES

		Purchase Price ($)	Monthly Maint. ($)	1-Year Lease* ($)	4-Year Lease* ($)
PROCESSORS					
CPS8130	DPS 8/47 Central System; integrated I/O Multiplexer, eight megabytes of Main Memory, and System Control Unit	153,000	500	8,800	7,400
CPU8129	Additional CPU for CPS8130; requires MXK8007	125,000	206	5,700	5,000
CPS8132	DPS 8/49 Central System; integrated I/O Multiplexer; eight megabytes of Main Memory, and System Control Unit	235,000	662	12,075	10,000
CPU8131	Additional CPU for CPS8132; requires MXK8007	135,000	335	8,000	7,000
CPS8181	DPS 8/52 Central System; includes Input/Output Processor, eight megabytes of Main Memory, and System Control Unit	450,000	1,425	25,496	21,082
CPU8182	Additional CPU for CPS8181; maximum of one	340,000	747	12,003	9,934
CPS8186	DPS 8/62 Central System; includes Input/Output Processor, eight megabytes of Main Memory, and System Control Unit	550,000	2,000	29,913	25,504
CPU8185	Additional CPU for CPS8186; maximum of one	475,000	9,900	20,476	16,946
CPS8189	DPS 8/70 Central System; includes Input/Output Processor, eight megabytes of Main Memory, and System Control Unit	700,000	3,000	44,715	38,094
CPU8188	Additional CPU for CPS8189; maximum of three	575,000	1,710	31,499	26,068
CPS8119	DPS 8/47C Central System; includes Input/Output Multiplexer, 12 megabytes of Main Memory, System Control Unit, and Datanet 8C Front-End Processor	228,000	967	11,950	10,050
CPU8119	Additional CPU for CPS8119; requires MXK8007	125,000	334	5,700	5,000
CPS8121	DPS 8/49C Central System; includes Input/Output Multiplexer, 16 megabytes of Main Memory, System Control Unit, and Datanet 8C Front-End Processor	350,000	1,365	17,100	14,000
CPU8121	Additional CPU for CPS8121; requires MXK8007	135,000	514	8,000	7,000
CPS8173	DPS 8/52C Central System; includes Input/Output Multiplexer, 16 megabytes of Main Memory, System Control Unit, and Front-End Processor	594,888	2,376	31,181	25,867
CPU8173	Additional CPU for CPS8173; maximum of one	340,000	1,018	12,191	10,122
CPS8174	DPS 8/62C Central System; includes Input/Output Multiplexer, 16 megabytes of Main Memory, System Control Unit, and Front-End Processor	695,000	2,654	35,696	29,601
CPU8174	Additional CPU for CPS8174; maximum of one	475,000	1,307	20,683	17,153
CPS8178	DPS 8/70C Central System; includes Input/Output Multiplexer, 16 megabytes of Main Memory, System Control Unit, and Front-End Processor	800,000	3,867	50,606	41,959
CPU8178	Additional CPU for CPS8178; maximum of five	575,000	2,152	31,751	26,310
CPS8199	DPS 8/70M Central System; includes Input/Output Multiplexer, eight megabytes of Main Memory, and System Control Unit	750,000	3,720	43,775	38,000
CPU8199	Additional CPU for CPS8199; maximum of five	575,000	2,152	34,251	28,310
PROCESSOR OPTIONS					
MXC8001	Additional Freestanding System Control Unit (SCU) for DPS 8/70, DPS 8/70M, and DPS 8C (three max.); includes all the necessary addressing	57,788	110	1,914	1,571
MXC8003	Additional Five-Port SCU for DPS 8/47, 8/49, 47C, and 49C	33,000	64	1,000	936
MXC8002	Additional Five-Port SCU for DPS 8/52, 8/62, 8/70, 8/52C, 8/62C, 8/70C, and 8/70M; includes all necessary addressing	57,788	110	1,914	1,571
MXU6002	Freestanding Input/Output Multiplexer with 35 Channel Function Slots for DPS 8/70, DPS 8/70M, and DPS 8C; includes SCU/IOM port addressing and data rate expansion	175,055	345	4,132	3,719
MXU8003	Additional IOM for DPS 8/47, 8/49, 8/47C, and 8/49C	84,380	205	2,840	2,338
MXF6005	Input/Output Multiplexer Expansion from 35 to 54 Channel Function Slots for DPS 8/70. DPS 8/70M. and DPS 8C	53,855	117	1,297	1,233

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		Purchase Price ($)	Monthly Maint. ($)	1-Year Lease* ($)	4-Year Lease* ($)
MXU8002	Additional IOM for 8/52, 8/62, 8/70, 8/52C, 8/62C, 8/70C, and 8/70M	137,500	131	4,132	3,719
MXF8005	IOM Channel Expansion from 36 to 54 Channel Function Slots; for MXU8002-type IOM only	53,255	108	1,297	1,233
MXF8012	Multics IOM Logical Channel Expansion for DPS 8/M Systems only (24-56 channels)	10,000	20	415	335
MXK8009	SCU Expansion Kit (5-to-8 port); required for 3-4 processor configurations	10,791	21	356	295
CPK8337	System upgrade from DPS 8/47 to 8/49	90,000	162	3,275	2,600
CPK8340	Additional CPU upgrade; DPS 8/47 to 8/49	22,000	129	2,800	2,500
CPK8163	System upgrade from DPS 8/52 to 8/62	135,000	575	4,644	4,423
CPK8185	Additional CPU upgrade; DPS 8/52 to 8/62	100,000	243	8,473	7,012
CPK8171	System upgrade from DPS 8/62 to 8/70	150,000	1,000	14,802	12,590
CPK8188	Additional CPU upgrade; DPS 8/62 to 8/70	100,000	720	11,023	9,122
CPK8362	System upgrade from DPS 8/47C to 8/49C	130,000	398	5,150	3,950
CPK8365	Additional CPU upgrade; DPS 8/47C to 8/49C	22,000	180	2,300	2,000
CPK8164	System upgrade from DPS 8/52C to 8/62C	135,000	278	4,740	4,519
CPK8174	Additional CPU upgrade; DPS 8/52C to 8/62C	100,000	289	8,492	7,031
CPK8172	System upgrade from DPS 8/62C to 8/70C	105,000	1,213	14,909	12,696
CPK8178	Additional CPU upgrade; DPS 8/62C to 8/70C	100,000	845	11,068	9,167
CPK8197	System upgrade from DPS 8/62M to 8/70M	155,000	1,107	14,525	13,000
CPK8198	Additional CPU upgrade; DPS 8/62M to 8/70M	100,000	845	13,751	11,360