29 APRIL 1985



SHINPADS STANDARD DISPLAY AN/UYQ-501(V)

PRODUCT FUNCTION SPECIFICATION

957031-A

SHINPADS STANDARD DISPLAY

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AN/UYQ-501(V)

29 APRIL 1985

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GD COMPUTING DEVICES COMPANY a division of Control Data Canada. Ltd.

957031-A

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PRODUCT FUNCTION SPECIFICATION

FOR THE SHINPADS STANDARD

DISPLAY

AN/UYQ-501 (V)

DOCUMENT ORIGIN AND APPROVAL RECORD

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-A	April 29, 1985	Production Release. IFF, continuous erase, machinery symbols, 1075-line TV added

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1. <u>SCOPE</u>

1.1 <u>Scope</u>. This Specification establishes the performance, test, manufacture and acceptance requirements for the SHINPADS Standard Display (SSD). The SSD shall be available in several configurations ranging from a 'graphics only' capability to a full-up capability (graphics, radar HSSI, and TV).

This Specification considers the full-up option, with the others being subsets.

2. APPLICABLE DOCUMENTS

The following documents of the exact issue shown, form a part of this Specification to the extent specified herein.

2.1 Computing Devices Company

- 650211-A Display Processor Display Controller Interface for SSD
- 650217-1 Display Control Unit Display Driver Assembly Interface
- 650298-A Display Driver Software Interface
- 650349-3 Display Driver Software Requirement Specification
- 955859-2 High Speed Serial Interface Design Specification
- 956001 ComDev Workmanship Standard
- 907611-B High Resolution Colour Monitor Specification
- 959289-A User Manual
- 907943-11 Power Supply

2.2 Military Specifications and Standards

MIL-STD-810	10 Mar 75	Issue C	Environmental Test Methods
MIL-S-901	15 Jan 63	Issue C	Shock Test High Impact Ship- board Machinery, Equipment and Systems
MIL-STD-167	1 May 74	Type l	Mechanical Vibrations of Shipboard Equipment
MIL-E-16400	24 Dec 74	Issue G	Electronic Equipment, Naval Ship and Shore; General Speci- fication for Interior Communi- cation and Navigation Equip- ment
MIL-STD-108	4 Aug 66	Issue E	Definitions of and Basic Re- quirements for Enclosures for Electric and Electronic Equip- ment

MIL-STD-461		Issue B	Electromagnetic Interference Characteristics, Requirements for Equipment
FED-STD-102	29 Jan 63	Issue B	Preservation, Packaging and Packing Levels
FED-STD-123	1 Dec 75	Issue D	Marking for Domestic Shipment
RS-343	Sep 69	Issue A	Electrical Performance Stand- ards for High Resolution Mono- chrome Closed Circuit Tele- vision Camera
STANAG 4146	- -		Interim Standard Specifica- tions for Input/Output Inter- faces in NATO Naval Data Hand- ling Equipments
STANAG 1008			Power Sources Standard
MIL-STD-785			Reliability Program Require- ments
MIL-STD-470			Maintainability Program Re- quirements
MIL-HDBK-472			Maintainability Prediction
MIL-STD-740			Airborne and Structureborne Noise Requirements
RS-170			Electrical Performance Stand- ard – Monochrome Television Studio Facilities.
STANAG 4153 (Edition 1)			Standard Specification For An Asynchronous Serial Data Interface for point-to-point connections and for connection to Data Networks in NATO Naval Systems.
RS-412A			Electrical Performance Stand- ard for Direct View, High Re- solution, Monochrome CCTV Monitor.
RS-422			Electrical Characteristics of Balanced Voltage, Digital In- terface Circuits.
MIL-M-7793			Elapsed Time Meter

3. REQUIREMENTS

Item Definition. The SSD shall consist of 3.1 а high resolution colour TV type display with associated control electronics, pixel memory and operator interface. The display may be easily reconfigured for monochrome applications and will not require changes to the user or driver software for monochrome operation. The major interfaces to the SSD are shown in Figure 3-1. The SSD shall be capable of displaying a wide range of sensor video and synthetic information. It shall interface with three classes of sensors:

> Radars Frame Sensors (TV, FLIR, LLLTV) Line Scan Sensors (Sonar, I/R)

The SSD shall interface with a general-purpose computer (such as an AN/UYK-502) designated the Display Processor which can be programmed by users for individual applications. The SSD will not operate in a stand-alone mode.

3.1.1 <u>Item Diagram</u>. The SSD shall consist of the following functional units which are illustrated in Figure 3-1:

High Resolution TV Monitor Operator Control Unit (CUD)* Display Driver Assembly (DDA)

3.1.1.1 <u>High Resolution TV Monitor</u>. The TV monitor shall be a high resolution colour device using 1225 lines and 30 Hz frame rate (60 Hz field, interlaced 2:1), with aspect ratio of 4:3.

3.1.1.2 <u>Display Driver Assembly (DDA)</u>. The DDA shall provide the SSD with the capability of displaying information from radar, TV and digitized line-scan sensors, as well as complete synthetic graphical displays. For those SSD applications which only require computer-generated synthetic graphics, the total number of cards will be reduced by removing the video processing cards. Partitioning will be such that the graphics and sensor circuits are so far as possible on separate cards. No other change to the DDA besides removal of cards shall be required to delete the sensor capability.

3.1.1.3 Operator Control Unit (CUD). The CUD shall provide the operator interface for 'hard' and 'soft' buttons, cursor positioning, keyboard, and analog controls. The CUD may be tailored for different display function applications by reprogramming. The 'softbutton' shall be implemented using a zero order joystick with response indications on the crt.

CUD = Control Unit Display.

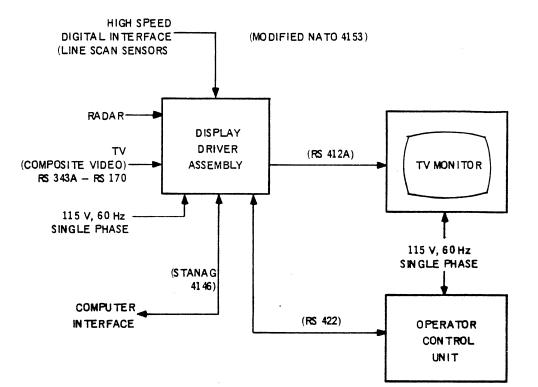


Figure 3-1. SSD Major Units

3.1.1.4 External Computer. The DDA shall interface with an external computer designated the Display Processor (DP). The DDA shall interface with the external computer through the following interface: NATO 4146 Type B - NTDS-Fast 16-bit Parallel Interface in computer/peripheral mode, with the DDA designated as the peripheral. The external computer shall perform Display Processing Applications functions, under user-generated software control.

3.1.2 Interface Definition

3.1.2.1 <u>External SSD Interfaces</u>. The SSD shall have external interfaces to radar, TV, computer and a high-speed digital interface for video.

3.1.2.1.1 <u>Radar Interface</u>. The radar interface shall use signals shown in Table 3-1.

3.1.2.1.2 <u>TV Interface</u>. The SSD shall be capable of accepting TV video for line rates of 525, 625, 875 and 1075. The 525-line rate shall be as defined in the RS-170 Specification and the 625, 875 and 1075-line rates shall be as defined in RS-343A. The characteristics are shown in Tables 3-2 and 3-3. Interlace of 2:1 at 50 and 60 Hz field rates shall be accommodated. In order to provide correct interlace, equalization pulses shall be provided during the vertical blanking interval.

3.1.2.1.3 <u>Computer Interface</u>. The SSD shall interface with the external computer over an NTDS 16-bit parallel STANAG 4146 (Type B) (reference ComDev document 650211).

3.1.2.1.4 <u>High Speed Serial Interface</u>. The SSD shall interface with digital video information over a 10M bit/second input channel, conforming to the electrical and mechanical standards of STANAG 4153. The protocol over this channel shall be such as to allow the transmitting sensor to set up the basic parameters of the scan, such as scan direction (up, down, left, right), line length, and starting position in the video area. Once this has been set up, pixel data may be sent continuously and the SSD formatting electronics shall automatically write the data into the correct locations. The details of this input channel are given in the High Speed Serial Interface Specification, ComDev document 955859.

3.1.2.2 <u>Electrical Power Interface</u>. The SSD shall meet the requirements of NATO STANAG 1008 (Type I power) and shall use:

115V ± 8%, 60 Hz, single phase apportioned as follows: CUD 25W max. DDA 750W max. TV MONITOR 200W max.

<u>Signal</u>	<u>Type</u>	<u>Level</u>	Character- istic	<u>Pulse Width</u>		
Radar Interfaces Trigger 1 (A, R Scan)	Differential	*	O to 6 kHz	150 ns min.		
Trigger 2 (PPI, B Scan)	Differential	*	O to 6 kHz	150 ns min.		
R Scan Range Trigger	Differential	*	O to 6 kHz	150 ns min.		
Azimuth Clock Pulses	Differential	*	4095 pulses per revolu- tion**	150 ns min.		
Azimuth Refer- ence Pulse	Differential	*	0 to 1 Hz	150 ns min.		
Video PPI	Triaxial 75 ohm	0 - 2V		50 ns min.		
Video A/R Scan	Triaxial 75 ohm	0 – 2V		50 ns min.		
Video Offset		<u>+</u> 300mV				
* Differential input of up to <u>+</u> 3 volts. Detailed characteri- zation is as for Line Receiver type 55115 (Texas Instruments).						
** This azimuth resolution is based on 4096 pulse periods per revolution with the 4096th pulse being omitted and the azimuth reference pulse appearing at this time.						
IFF Interface Characteristics The Display shall produce negative-going pulses (synchro- nized with Trigger 1 above), having the following characteris- tics:						
Type:Isolated CoaxialImpedance:75 ohms ± 5%Amplitude:-5.0 volts ± 2VRise and Fall Time:50 ns maximumBaseline:Min. = 0V, Max. = 0.5V, Nominal = 0.2VAzimuth Resolution:0.176°Range Resolution:0.39% of Range Scale						
Note: There will be some delay between the specified position or range of the IFF pulse and the actual position due to circuit delays. This shall be no greater than 50 ns.						

Table 3-1. Radar and IFF Interfaces

Lines/Frame	Active Lines
525	480
625	582
875	804
1075	990

Table 3-2. TV Line Rates

Signal	Impedance	Type	<u>Bandwidth</u>
Composite TV	75 ohm	Triaxial	35 MHz

Table 3-3. TV Video Characteristics

3.1.2.3 <u>Internal Interfaces</u>. The internal interfaces shall connect the following major items:

DDA to TV monitor DDA to CUD (Operator Control Unit)

3.1.2.3.1 <u>DDA to TV Monitor</u>. This interface shall use video signals for the (Red, Green, Blue) RGB outputs as defined in the RS-412 Specification. The composite signal shall be incorporated in the RGB output cell. A capacity to drive up to 100 m of the RGB signals shall be provided. (See Table 3-3.)

3.1.2.3.2 <u>DDA to CUD Interface</u>. The interface shall have electrical characteristics as defined in RS-422. Maximum cable length shall be 100 m.

3.1.2.4 <u>Software Interface</u>. The SSD user is required to generate software for each application of the SSD. This software will execute in the Display Processor. (To simplify the user software, a Display Driver Module which is available for the AN/UYK-20, 502 and 505 computers, performs basic functions for scheduling and interfacing between the user software and the DDA. This is defined in ComDev document 650298, Display Driver Interface Specification.)

3.1.2.4.1 Display Processor to DDA Software Interface. Control of the SSD and selection of its functions shall be performed by the Display Processor using the commands described in ComDev document 650211. These fall into four broad classes, viz:

CUD Functions Video Processing and Display Functions Graphics/Track Management Functions Status/Test Functions

3.1.3 <u>Major Components List</u>. The SSD shall comprise the major components as detailed in the indented list, Table 3-4. This list includes circuit card assemblies (CCA), major subassemblies and modules.

SSD Display Driver Assembly (DDA) Power Supply CCA, Display Controller (DC) CCA, Coordinate Converter (CC) CCA, Radar Processor (RP) CCA, Cell to Word Buffer (CWB) CCA, Ranging Display Formatter (RDF) CCA, High Speed Serial Interface (HSSI) CCA, TV Interface (TVI) CCA, Function Generator (FG) CCA, Memory Controller (MC) CCA, Video Memory (Qty 4) (VM) CCA, Graphics Memory (Qty 2) (GM) CCA, Raster Generator (RG) CCA, TV Driver (TVD) Chassis, Electrical TV Monitor Operator's Control Unit CCA, Processor Joystick Trackball Keyboard Assembly Power Supply Chassis, Electrical

Table 3-4. Indented List of Major Components

3.2 Characteristics

3.2.1 Functional Characteristics

3.2.1.1 <u>TV Monitor</u>. The monitor shall be a high resolution colour device with characteristics as defined in ComDev Specification 907611.

3.2.1.2 Operator's Control Unit (CUD)

3.2.1.2.1 <u>General</u>. The CUD shall be self-contained, communicating with the Display Driver Assembly (DDA) via an RS-422 serial communication link.

The following paragraphs detail the CUD requirements under these broad categories:

functions operator's control panels interface electrical mechanical configuration

3.2.1.2.2 <u>CUD Function</u>. The CUD is intended to be the primary man-machine interface of the SSD. As such, it shall enable the operator to perform his assigned function. To allow the SSD to perform its envisaged role, the CUD shall have the following features:

- (a) A first order trackball cursor controller typical use will be to select and hook targets on the display screen.
- (b) A zero order joystick typical use will be the implementation of 'soft' buttons, e.g., display menu selection.
- (c) Up/down left/right alphanumeric cursor controller.
- (d) Scroll Up/Down buttons.
- (e) 96-character ASCII keyboard.
- (f) Four fixed function quick-action buttons (QABs), three associated with the trackball and one associated with the joystick.
- (g) A repeat function on certain designated keys.
- (h) Indicators and backlit switches with external control of their intensity and blink.

The above functions shall be considered necessary during the normal operation of the SSD in any of its designated roles. Thus, they are primary controls. In addition to the above, the CUD shall have a number of secondary controls and indicators which shall provide the following functions:

- (j) DDA/CUD Power switch and indicator.
- (k) Lamp test indicator-switch.
- (1) Initiation and display of results of built-in tests (BITs).
- (m) DDA Overheat and Power monitoring, with Battleshort override.
- (n) A hooded switch and an enable indicator whose typical use shall be in the weapons fire sequence.
- (p) Four variable function QABs and two continuous controls whose use will be determined by the application.
- (q) Three continuous controls to set the brightness levels of the graphics, video and trackball cursor imagery.
- (r) Two continuous controls to set the intensities of the lamps and an audible alarm in the CUD.
- (s) An indicator-switch to signal and respond to an Alert condition (in conjunction with the audible alarm).

The CUD shall also contain an Elapsed Time Meter.

3.2.1.2.3 <u>Operator's Control Panels</u>. To meet the above functional requirements, the controls and indicators shall be grouped onto two panels, CPD-1 and CPD-2, as shown in Figure 3-2. Unless otherwise specified:

- All indicator-switches shall be momentary-action push buttons with integral illuminated white lenses and black legends.
- All indicators shall have illuminated red "dead-front" lenses with black legends (i.e., the display appears black until illuminated).
- All lamps shall be externally controllable to Off (Low) and On intensities, and to Blink at 2 Hz.

3.2.1.2.3.1 <u>Primary Controls</u>. This group shall be located on the main control panel, CPD-1, and shall comprise the following:

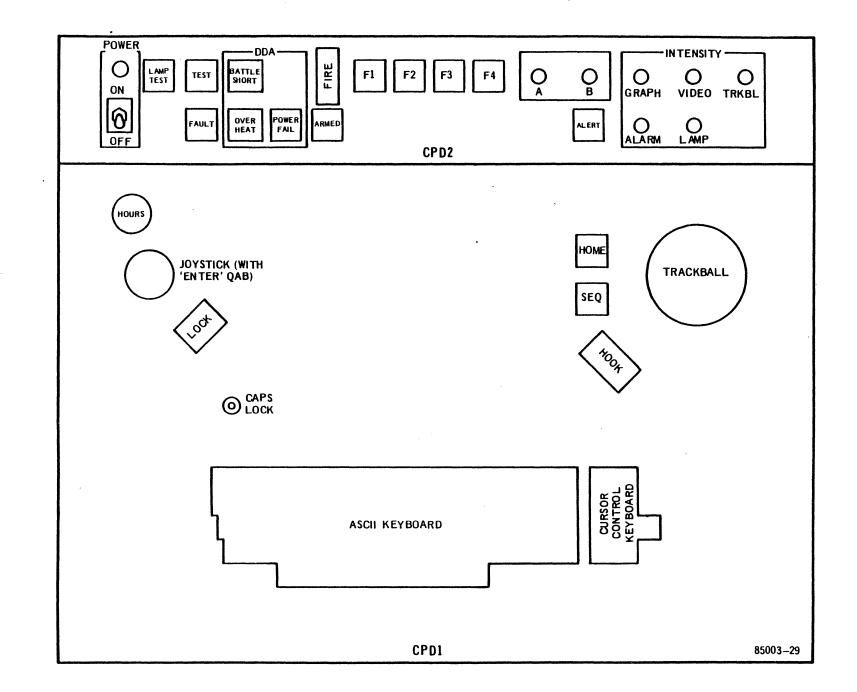


Figure 3-2. CUD Panel Layouts

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- (a) Trackball This shall be a 3-inch diameter trackball providing first-order cursor control, i.e., it shall generate changes in position only. The slew rate response shall be non-linear to provide fine control of the cursor and allow the cursor to be moved across half the screen within 1 second. The trackball is intended to operate in conjunction with the HOME, SEQ and HOOK QABs which shall be adjacent to it.
- (b) Joystick This shall be a zero-order cursor control, i.e., it shall generate absolute position coordinates, with a resolution of 256 x 256 points. The joystick shall incorporate an unlit switch, referred to as the "Enter" QAB, at the top of its handle. The joystick is intended to operate in conjunction with this QAB.
- (c) LOCK This indicator-switch shall be located adjacent to the joystick and is used to enable/disable the transmission of joystick position messages to the DDA. Its lamp shall indicate the joystick operational status and is not externally controllable.
- (d) Keyboard Assembly This keyboard shall have 65 unlit keys to generate the ASCII character repertoire shown in Table 3-5 and shall include the following functions:
 - Full upper and lower case alphabet and control code outputs.
 - Caps Lock mode (indicated by the unlabelled amber LED above the keyboard, whose intensity shall not be adjustable or externally controllable).
 - Alpha-numeric cursor control comprising up, down left, right and home keys, (labelled with directional arrows and "." respectively.
 - Auto-repeat of designated keys at a rate of a 10 Hz when a key is depressed longer than 1/2 second.
- Quick Action Buttons - These QABs shall comprise (e) switches associated with joystick and trackball keys for of operation, and control scrolling. Depression of a QAB shall result in transmission of a message to the DP which shall use it as required by the application, (typical actions are described).
 - ENTER This shall be an unlabelled switch on the joystick handle. Use to action the soft key indicated on the screen by the joystick cursor.
 - HOME Locate the trackball cursor to a predefined location.

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KEY	NORMAL		SHIFT		CTRL			SHIFT AND CTRL				
	OCTAL CODE	DISPLAY CHAR.	REP'D	OCTAL CODE	DISPLAY CHAR.	REP'D	OCTAL CODE	DISPLAY CHAR.	REP ' D	OCTAL CODE	DISPLAY CHAR.	REP'D
ESC	033		N	033		N	033		N	033		 N
1	061	1	Ŷ	041	1	Y	061	1	Y	041		Y
2	062	2	Ŷ	042		Ŷ	062	2	Ŷ	042		Ŷ
3	063	3	Ŷ	043	#	Ŷ	063	3	Ŷ	043	*	Ŷ
4	064	4	Y	044	\$	Ŷ	064	4	Ŷ	044	\$	Ŷ
5	065	5	Y	045	1	Y	065	5	Ŷ	045	3	Ŷ
6	066	6	Y	046	8	Y	066	6	Y	046	8	Y
7	067	7	Y	047	•	Y	067	7	Y	047	•	Y
8	070	8	Y	050	(Y	070	8	Y	050	(Y
9	071	9	Y	051)	Y	071	9	Y	051)	Y
0	060	0	Y	060	0	Y	060	0	Y	060	0	Y
-	055	-	Y	075	-	Y	055	-	Y	075	-	Y
[133	[Y	173	{	Y	133	[Y	173	ł	Y
1	135]	Y	175	}	Y	035		N	035		N
TAB	011		Y	011		Y	011		Y	011		Y
Q	161	Q	Y	121	Q	Y	021		N	021		N
W	167	W	Y	127	W	Y	027		N	027		N
E	145	E	Y	105	E	Y	005		N	005		N
R	162	R	Y	122	R	Y	022		N	022		N
т	164	т	Y	124	т	Y	024		N	024		N
Y	171	Y	Y	131	Y	Y	031		N	031		N
U	165	U	Y	125	U	Y	025		N	025		N
I	151	I	Y	111	. I	Y	011		Y	011		Y
0	157	0	Y	117	0	Y	017		N	017		N
P	160	P	Y	120	P	Y	020		N	020		N
e	100	Ģ	Y	140		Y	000		N	000		N
N	134	\mathbf{N}	Y	174	1	Y	034		N	034		N
-	137	-	Y	137	-	Y	037		N	037		N
DEL	177	Ē	Y	177		Y	177		Y	177	-	Y
A	141	A	Y	101	A	Y	001		N	001		N
S	163	S	Y	123	S	Y	023		N	023		N
D	144	D	Y	104	D	Y	004		N	004		N
F	146	F	Y	106	F	Y	006		N	006		N
G	147	G	Y	107	G	Y	007		N	007		N
н	150	н	Y	110	н	Y	010		Y	010		Y
J	152	J	Y	112	J	Y	012		Y	012		Y
K L	153	ĸ	Y	113	ĸ	Y	013		Y	013		Y
	154 073	L	Y Y	114 053	L	Y Y	014 073		Y Y	014		Y
	072		r Y	053	+	Y Y	073		Y Y	053 052	+	Y
:	136	÷	Ŷ	176		Y Y	072	:	r N	036	•	Y N
CR	015		Y	015	~	Y Y	015		N Y	015		Y
Z	172	Z	Ŷ	132	z	Ŷ	032		N	032		Ň
x	170	x	Ŷ	130	x	Y	030		N	030		N
c	143	ĉ	Ŷ	103	ĉ	Ŷ	003		N	003		N
v	166	v	Ŷ	126	v	Ŷ	026		N	026		N
в	142	В	Ŷ	102	в	Ŷ	002		N	002		N
N	156	N	Ŷ	116	N	Ŷ	016		N	016		N
M	155	M	Ŷ	115	M	Ŷ	015		Ŷ	015		Ŷ
	054		Ŷ	074	<	Ŷ	054		Ŷ	074	<	Ŷ
	056		Ŷ	076	>	Ŷ	056		Ŷ	076	>	Ŷ
1	057	,	Ŷ	077	?	Ŷ	057	,	Ŷ	077	?	Ŷ
LF	012	•	Ŷ	012		Ŷ	012		Ŷ	012		Ŷ
SPACE	040		Ŷ	040		Ŷ	040		Ŷ	040		Ŷ
BS	010		Y	010		Ŷ	010		Ŷ	010		Y
BLNK KEY	206		Ŷ	207		Ŷ	205		Ŷ	211		Ŷ
UP	201		Y	201		Ŷ	201		Ŷ	201		Y
LEFT	204		Y	204		Ŷ	204		Y	204		Y
HOME	210		N	210		N	210		N	210		N
RIGHT	203		Y	203	=	Ŷ	203		Ŷ	203		Y
DOWN	202		Y	202		Y	202		Y	202		Y
			-		-	•		-	•		-	~

Table 3-5. Character Repertoire (Sheet 1 of 2)

KEY	CAPS LOCK			CAPS LOCK AND SHIFT		CAPS LOCK AND CTRL			CAPS LOCK, SHIFT AND CTRL			
	OCTAL CODE	DISPLAY CHAR.	REP'D	OCTAL CODE	DISPLAY CHAR.	REP ' D	OCTAL CODE	DISPLAY CHAR.	REP'D	OCTAL CODE	DISPLAY CHAR.	REP ' D
ESC	033		N	033		- N	033		N	033		N
1	061	1	Y	041	1	Y	061	1	Y	041	1	Y
2	062	2	Y Y	042		Y Y	062	2	Y Y	042	"	Y
3 4	063 064	3	Y Y	043 044	* \$	Y Y	063	3 4	Y Y	043 044		Y Y
5	065	5	Ŷ	045	2	Ŷ	065	5	Ŷ	045	2	Ŷ
6	066	6	Ŷ	046	6	Ŷ	066	6	Ŷ	046	8	Ŷ
7	067	7	Ŷ	047	-	Ŷ	067	7	Ŷ	047	7	Ŷ
8	070	8	Y	050	(Y	070	8	Y	050	(Y
9	071	9	Y	051)	Y	071	9	Y	051)	Y
0	060	0	Y	060	0	Y	060	0	Y	060	0	Y
-	055	-	Y	075	=	Y	055	-	Y	075	-	Y
Ĺ	133	[Y	173	Ĺ	Y	133	(Y	173	{	Y
	135 011]	Y Y	175 011]	Y Y	035 011		N Y	035 011		N Y
TAB Q	121	Q	Y	121	Q	Ŷ	021		N	021		N
Ň	121	Ŵ	Ŷ	127	Ŵ	Ŷ	027		N	021		N
E	105	Ē	Ŷ	105	E	Ŷ	005		N	005		N
R	122	R	Ŷ	122	R	Ŷ	022		N	022		N
т	124	T	Ŷ	124	T	Ŷ	024		N	024		N
Y	131	Y	Y	131	Y	Y	031		N	031		N
U	125	U	Y	125	U	Y	025		N	025		N
I	111	I	Y	111	I	Y	011		Y	011		Y
0	117	0	Y	117	0	Y	017		N	017		N
P	120	P	Y	120	P	Y	020		N	020		N
(e	100	e	Y	140		Y	000		N	000		N
`	134	`	Y	174	ł	Y	034		N	034		N ·
5	137	=	Y	137	Ē	Y	037	_	N	037	_	N
DEL A	177 101	M A	Y Y	177 101	A	Y Y	177 001		Y N	177 001	-	Y N
S	123	S	Y	123	S	Ŷ	023		N	023		N
Ď	104	D	Ŷ	104	D	Ŷ	004		N	004		N
F	106	F	Ŷ	106	F	Ŷ	006		N	006		N
G	107	G	Y	107	G	Y	007		N	007		N
н	110	н	Y	110	н	Y	010		Y	010		Y
J	112	J	Y	112	J	Y	012		Y	012		Y
к	113	к	Y	113	к	Y	013		Y	013		Y
L	114	L	Y	114	L	Y	014		Ŷ	014		Y
;	073	;	Y	053	+	Y	073	;	Y	053	+	Y
÷	072	:	Y	052	*	Y	072	:	Y	052	*	Y
CR	136 015		Y Y	176	~	Y Y	036		N Y	036		N
Z	132	z	Y	015 132	z	Ŷ	015 032		N	015 032		Y N
x	130	x	Ŷ	132	x	Ŷ	032		N	030	•	N
c	103	c	Ŷ	103	ĉ	Ŷ	003		N	003		N
v	126	v	Ŷ	126	v	Ŷ	026		N	026		N
в	102	B	Y	102	B	Ŷ	002		N	002		N
N	116	N	Y	116	N	Y	016		N	016		N
M	115	м	Y	115	M	Y	015		Y	015		Y
•	054		Y	074	<	Y	054		Y	074	<	Y
:	056	÷	Y	076	>	Y	056	÷	· Y	076	>	Y
/	057	/	Y	077	?	Y	057	/	Y	077	?	Y
LF SPACE	012 040		Y Y	012		Y Y	012 040		Y	012		Y
BS	040		Y Y	040 010		Y Y	040		Y Y	040 010		Y Y
BLNK KEY	206		Ŷ	207		Y	205		Y	211		Y
UP	200		Ŷ	201		Y	203		Y	201		Y
LEFT	204	-	Ŷ	204	-	Ŷ	201	-	Ŷ	204	-	Ŷ
HOME	210		Ň	210		Ň	210		Ň	210		Ň
RIGHT	203		Ŷ	203		Ŷ	203		Ŷ	203		Ŷ
DOWN	202		Y			Y						Y

Table 3-5. Character Repertoire (Sheet 2 of 2)

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- SEQ Sequence the trackball cursor and Hook symbol through predetermined positions.
- HOOK Use in conjunction with trackball cursor to identify targets.
- SCRL UP, SCRL DOWN These unlit keys shall be located adjacent to keyboard cursor control keys and shall auto-repeat in the same manner. Use to scroll tabular data up or down.

3.2.1.2.3.2 <u>Secondary Controls</u>. This group shall be located on the auxilary control panel CPD-2 and shall comprise the following:

- (a) POWER This shall be a guarded, two position toggle switch with integral circuit breaker and shall control the application of primary power to the CUD directly and to the DDA indirectly. Power On shall also be indicated by an adjacent 120V ac neon lamp with amber lens.
- (b) LAMP TEST Activation of this indicator-switch shall cause all lamps (except POWER), the audible alarm and their respective drive circuits to be tested. Depression a second time shall cause all indicators to return to their previous status. (This indicator shall not be externally controllable).
- (c) TEST Activation of this indicator-switch shall cause the DDA to initiate off-line SSD self-test with illumination of the lamp indicating test-in-progress, (a message to this effect shall be sent to the DP). This control shall be protected from accidental activation by adjacent raised barriers.
- (d) FAULT This indicator shall be controlled by a "fail-safe" circuit i.e., it shall require periodic action to keep it Off. Illumination of this lamp shall indicate that a fault has been diagnosed by the off-line self-test, or has been detected by the on-line self-test of the SSD. External control of this indicator shall be limited to turn Off.
- (e) OVER HEAT This indicator shall be illuminated when an overtemperature condition is detected in the DDA. The indicator shall blink for approximately 25 seconds, after which the DDA power supply shall shut down and the indicator shall remain On. When the temperature returns to normal the indicator shall be turned Off. This indicator shall not be externally controllable.

- (f) BATTLE SHORT This shall be an alternate-action indicator-switch with a red lens and be located adjacent to the OVER HEAT indicator. Activation of this control while the OVER HEAT lamp is blinking shall override the DDA power supply shutdown. Its lamp shall be illuminated directly by the switch and shall not be externally controllable.
- (g) POWER FAIL This indicator shall be illuminated when the loss of prime power to the DDA power supply is detected. This indicator is not externally controllable.
- (h) FIRE This shall be a momentary-action toggle switch and shall be protected from accidental usage by a red two-position guard. Used to issue a weapons fire command to the DP.
- (j) ARMED This indicator shall be located adjacent to the FIRE switch and is used to indicate that the FIRE switch is enabled.
- (k) F1, F2, F3, F4 These indicator-switches shall be variable function QABs used and controlled by the DP. They shall be located in a row adjacent to the bottom of the screen, (where it is intended that their function will be annotated as determined by the application).
- (1) A. B These shall be variable function continuous rotary controls whose use shall be determined by the application. They shall be located adjacent to the bottom of the screen so that they may be annotated as above. When enabled by the application the "A" control shall set the radar video input threshold.
- (m) ALERT This shall be an indicator-switch with a yellow lens located adjacent to the ALARM intensity control. Used to indicate an Alert condition, (in conjunction with the audible alarm), and to respond.
- (n) INTENSITY This shall be a group of five continuous rotary controls which shall be used internally in the SSD to adjust the following screen and indicator intensities:
 - GRAPH Graphics intensity.
 - VIDEO Video intensity.
 - TRKBL Trackball Cursor intensity.
 - ALARM Audible alarm intensity. The minimum setting shall be audible.
 - LAMP Shall adjust the intensity of all lamps except POWER and Caps Lock.

3.2.1.2.4 <u>Interface</u>. The CUD shall communicate with the DDA directly via a serial data communication link complying to RS-422, operating at a rate of 2400 baud. Data shall be transmitted and received using an ll-bit word (comprising a start bit, 8 bits of data, a parity bit and a stop bit). Odd parity shall be used.

Data transfers shall be accomplished through "messages" of three 8-bit words each consisting of a message code followed by two bytes containing the data related to the message code. See 650217 (DC-CUD IDS) for details.

3.2.1.3 <u>Video Processing and Display Functional Characteristics</u>

3.2.1.3.1 <u>Display Format.</u> The SSD shall have two separate memories. Sensor video information shall use a video memory of 1024 x 1024 picture cells (pixels) with each pixel having 4 bits for intensity. Sensor video colour shall not be dynamically selectable. Characters and graphics shall use a graphics memory covering the full extent of the 1225-line raster (1152 active lines at 1536 pixels/line) with each pixel providing a colour shade (of single intensity) defined by 4-bits, i.e., 1-bit for each of the three primary colours and one bit for BLINK. The video area shall be controlled in size (up to a maximum of 1024 x 1024) and position within the complete raster by the Display Processor. A typical layout for a 19-inch TV is shown in Figure 3-3.

3.2.1.3.1.1 <u>Colour Intensity Characteristic</u>. The 4 bits of video intensity and 1 bit each for the graphics memory colours are combined to form an output intensity characteristic contained in look-up tables. The contents of these tables form the output intensity transfer function and these data are derived from the DP (user defined). In the absence of a DP function, a default linear characteristic is implemented by the DC.

3.2.1.3.2 Radar Processing and Display

3.2.1.3.2.1 <u>Radar Digitization.</u> The radar video shall be digitized to a resolution of 5 bits. The sample rate shall be 41.984 MHz such that radar pulse widths down to a minimum of 50 ns shall be handled without aliasing.

A radar video threshold control shall be supplied on the CUD, that shall control the offset value of the video input to the A/D Converter. The range of offset available is ± 300 mV.

3.2.1.3.2.2 <u>Radar Azimuth Processing.</u> The digitized radar video shall be filtered in range and azimuth. Range filtering shall be by peak detection of groups of adjacent samples. The population of each group is a function of the selected scale.

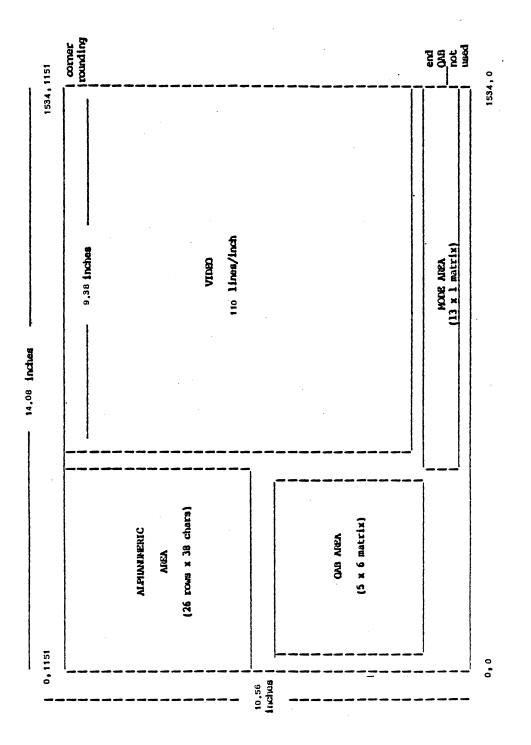


Figure 3-3. Typical Display Format for 19-Inch CRT

Azimuth filtering shall consist of a digital low-pass filter executing the equation:

$$Y_n = Y_{n-1} + \frac{1}{2^K} (X_n - Y_{n-1})$$

where:

Υn	is the new sample to be stored in the filter memory.
Y _{n-1}	is the previous sample from the filter memory.
x _n .	is the new input sample to the filter.
К	is the time constant.

The time constant shall be provided by the Display Processor. A longer time constant increases signal-to-noise ratio but degrades azimuthal resolution.

The effective value of K shall be an integer in the range O to 2. Two additional bits shall be provided in the azimuth filter to supply adequate dynamic range. A level-slice table shall reduce the full 7 bits output to 4 bits for storage in the video memory. The transfer function of this level-slice table shall be set up by the Display Processor, thereby effecting a programmable profile. The table shall be set to a linear transfer function on power-up.

3.2.1.3.2.3 <u>Plan Position Indicator (PPI)</u>. In the PPI mode the radar shall be displayed in the video area. The offset and scale of the radar shall be provided by the Display Processor in external units (data miles), relative to the Display Reference Coordinate (see 3.2.1.4.5.1):

- (a) Range Scales. Range scales in binary increments from 2 data miles to 512 data miles shall be provided. Range scales correspond to 512 pixels (i.e., maximum coverage shall be 1024 data miles).
- (b) Offset. The PPI display shall be capable of being offset anywhere within the 1024-mile square coverage. Offsets of 1.5 times selected range scale shall be permitted without spoking of the video.

3.2.1.3.2.4 <u>B-Scan.</u> In the B-Scan mode the radar shall be displayed in the top half of the video area (i.e., 512 range elements by 1024 azimuth elements). The B-Scan shall have a \pm 1000-yard range scale in the Y direction and \pm 100-milliradian (= \pm 5.73 degrees) bearing scale in the X direction. The bearing

and central range of the B-Scan display shall be defined by the Display Processor. At the same time as the B-Scan, a small PPI from the same radar can be optionally displayed in the bottom-left quarter of the video area, and the bottom-right quarter shall be unused. The B-Scan and small PPI displays shall be updated alternately, and the B-Scan shall be updated once every two radar scans. In the B-Scan mode, the graphics within the video area and the video shall be magnified by a factor of 2. The range scale of the small PPI shall be selectable by the Display Processor. No offset operation for the PPI display is allowed in this mode.

3.2.1.3.2.5 <u>A/R-Scan.</u> In this mode an A- and R-Scan shall be displayed in the top half of the video area. The A-Scan is a range-amplitude display of the radar video and shall cover the range 0 - 40k yards. The radar video shall be quantized at 41.984 MHz using 5 bits of A/D conversion. Each quantization level shall cover 4 pixels of the display. The full amplitude of the A and R Scan shall therefore each cover 64 pixels. The R-Scan shall be an expanded version of the A-Scan and shall display a 2000-yard range gate. The start of the display trace shall be initiated by a trigger pulse. This pulse shall be as defined in Table 3-1.

At the same time as the A, R Scan, a small PPI from a second scanning radar shall be optionally displayed in the bottom-left portion of the video area (767 x 767 pixels). The A/R-Scan and small PPI displays shall be updated alternately, the A/R-Scan being updated once every two revolutions of the scanning radar.

3.2.1.3.2.6 <u>IFF Area Gate Mode</u>. In this mode parameters received from the DP shall be used to generate pulses to an IFF decoder that matches the area gate defined by the DP parameters (see paragraph 3.4.1.2.4 for more details).

3.2.1.3.3 Framing Sensor Processing and Display

3.2.1.3.3.1 <u>Display Format.</u> The SSD shall interface with Framing TV type video, with lines per frame selected as 525, 625, 875 or 1075. The SSD logic shall perform A/D conversion and store the TV video information in the video memory, thus permitting:

annotation, magnification, frame freeze, and external image processing by the Display Processor.

To ensure there is no aspect distortion, imagery that falls outside the 1024×1024 video area shall not be displayed. Where frame size reduction occurs, the displayed portion will be centred within the full frame.

3.2.1.3.3.2 <u>Image Processing.</u> The TV input video shall be digitized to 5 bits. A level-slice table loaded from the Display Processor shall reduce this to 4 bits prior to entry into the video memory. A linear transfer function shall be set into the table as a default condition on power-up.

3.2.1.3.4 <u>Line Scan Sensor Display.</u> The SSD shall provide a High Speed Serial Interface with a maximum input data rate of 10 MHz and a protocol to accept digitized video and load it directly into the video memory. The protocol shall be such that, for line-scan formats, maximum use shall be made of the bandwidth of the digital channel for data transmission. See ComDev Specification 955859 for full details.

Magnification. The SSD shall provide a magnification 3.2.1.3.5 of two or four times. Parameters for defining the start and end addresses shall be applied separately to the video and graphics memories (e.g., it shall be possible to magnify the graphics within the video area, but retain unmagnified graphics outside this area). Graphics and video which normally lie within the video area but, after magnification, would lie outside the video will not Magnification area, be displayed. should be distinguished from range scaling, which is defined in 3.2.1.3.2.3 (a).

3.2.1.3.6 <u>Video Memory Scrolling</u>. The video memory shall be scrolled in Y independently of the graphics memory by specifying the Y address of the memory line desired at the top of the raster. This position shall be specified to a resolution of 2 lines.

3.2.1.3.7 <u>Freeze.</u> The contents of the video memory may be prevented from being updated with new video data on command.

3.2.1.3.8 <u>Scan-to-Scan Integration</u>. On selection, video data from a new scan may be combined with video data from the previous scan. The equation to be used shall be:

$$S_{n+1} = S_n + \frac{1}{2^K} (X_{n+1} - S_n)$$

where:

The filter time constant shall be selectable to be either 1 or 2.

3.2.1.3.9 <u>Target Trails.</u> On selection, target trails shall be implemented by combining video data from a new scan with video data from the previous scan such that (see 3.2.1.3.8 for definitions):

S_{n+1} = X_{n+1} if X_{n+1} ≥S_n
else S_{n+1} = S_n +
$$\frac{1}{2^{K}}$$
 (X_{n+1} - S_n)

3.2.1.3.10 <u>Peak Detect.</u> On selection, a peak detection between video data from a new scan and video data from the previous scan shall be made, such that:

$$S_{n+1} = X_{n+1} \quad \text{if } X_{n+1} \ge S$$
$$S_{n+1} = S_n \quad \text{if } X_{n+1} < S$$

3.2.1.3.11 <u>Continuous Erase</u>. On selection, each pixel in the Video Memory shall be erased after refreshing the TV once. This mode shall effectively bypass the Video Memory and give the same effect as refreshing the crt directly from the Sensor.

3.2.1.4 Graphics and Track File Management Requirements

3.2.1.4.1 <u>Graphics Display Area.</u> The SSD shall be capable of drawing graphics anywhere within the limits of the 1225-line TV raster at full resolution. The graphics memory shall therefore be a minimum of 1152 lines x 1535 pixels/line.

3.2.1.4.2 <u>Brightness Levels.</u> The graphics memory shall be 4 bits deep, giving the capability of off, high brightness and blink, for any of the three colours, and their combinations. The output intensity for a given primary colour can be controlled to 16 shades (selectable through the DP), therefore giving a total palette of 4096 colours for any selected pixel.

3.2.1.4.3 <u>Blink Rate.</u> The blink rate shall be 1 Hz, with on-off ratio 1:1.

3.2.1.4.4 <u>Graphics Repertoire</u>. The SSD shall have the capability of drawing ASCII characters, NTDS characters, machinery control symbols, vectors, arcs and circles in both positive and inverted video format. It shall also allow user-defined line types and character set. Graphics shall be overlayable without loss of information.

Inverted or inverse video is a feature that applies to characters and symbols only. Normally the characters are drawn intensified, against a Black background. Inverse video reverses this, so that the characters are drawn black against an intensified background. An extension of this is available in colour displays, in that the character may be drawn in one colour against a background of a different colour. In this case, inverse video would exchange the uses of those colours, i.e., the character is drawn in what used to be the background colour, against a background of what used to be the character colour.

All graphics are subject to windowing, which is the selective drawing or truncation of graphics, depending on their location relative to the 'window' or defined field-of-view. Separate windows are used for each coordinate system, with the pixel window fixed at the full graphics memory size, and the data-mile window definable. If any point of a character lies outside its defined window, it shall not be drawn. In a line of characters, each character shall be tested separately, thus partial lines may be displayed. Vectors, arcs, and circles shall be windowed, such that only that portion of the graphic appearing inside the window shall be displayed.

3.2.1.4.4.1 <u>ASCII Characters.</u> The full 64-character set of displayable ASCII characters shown in Table 3-6 shall be implemented. Two character sizes shall be provided as shown below.

ASCII	Matrix	Character Size	Character Size in Inches
<u>Type</u>	<u>Pixels</u>	Pixels	(19-inch TV)
Small	13 x 21	9 x l3	0.08 x 0.12
Large	19 x 29	l3 x l7	0.12 x 0.15

3.2.1.4.4.2 <u>Vectors.</u> The SSD shall be capable of drawing vectors and strings of vectors of any length and slope. The vectors shall be defined in two ways: by the endpoints; or by the start point plus length and slope.

3.2.1.4.4.3 <u>Arcs and Circles.</u> The SSD shall be capable of drawing arcs of any radius and angular subtense, up to full circles. A full circle may be drawn by making the angular subtense 360 degrees.

3.2.1.4.4.4 <u>Fixed Line Types.</u> The lines constituting the vectors and circles shall be 1 pixel wide. One of four fixed line types shall be selectable. These types are:

Continuous Dotted Dashed Dot-dash

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OCTAL CODE	CHARACTER	OCTAL CODE	CHARACTER
040 041 042 043 044 045 046 051 051 055 055 055 055 055 055 055 055	(Space) ! (exclamation point) " (quatation mark) # (number or pounde) \$ (dollar sign) % (percent) & (ampersand) * (capostrophe) ((left parentheses) # (asterisk) * (plus) , (comma) - (hyphen or minus) , (period) / (slant) 0 1 2 3 4 5 6 7 8	120 121 122 123 124 125 126 127 130 131 132 133 134 135 136 137 140	P Q R S T U V W X Y Z [(left bracket) \ (reverse slant)] (right bracket) \ (circumflex) (underline) \ (left single quote mark)
071 072 073 074 075 076 077 100 101 102 103 104 105 106 107 110 111 112 113 1:4 115 116 117	9 : (colon) ; (semicolon) < (less than) = (equals) > (greater than) ? (Questian mark) @ (commercial at) A B C D E F G H I J K L M N O	173 174 175 176 177	{ } ~

Table 3-6. Displayable ASCII Character Repertoire

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3.2.1.4.4.5 <u>User Programmable Line Types.</u> It shall be possible for the Display Processor to define four line types in addition to the four fixed types. The mark/space ratio of these lines shall be fully programmable up to a maximum pattern of 32 pixels.

3.2.1.4.4.6 User Programmable Characters. It shall be possible for the Display Processor to define a set of unique characters which may then be called by their defined codes. The number of user characters in the set depends upon the size of the characters. Twenty-four 32 x 32 pixel characters shall be definable, or ninety-six 16 x 16 pixel characters, etc.

3.2.1.4.4.7 <u>NTDS Characters.</u> The NTDS symbol set shown in Table 3-7 shall be implemented. Two symbol sizes for the 68 symbols with codes 33-102 shall be provided as shown below:

NTDS Type	Symbol Matrix <u>Pixels</u>	Symbol Size Pixels	Symbol Size in Inches <u>(19-inch TV)</u>	Subtense at 18 inches <u>(minutes of arc)</u>
Small	19 x 19	17 x 17	0.15 x 0.15	29' x 29'
Large	25 x 25	23 x 23	0.21 x 0.21	40' x 40'

A set of 45 machinery control symbols shall be provided as shown in Table 3-7. Codes 103-131 (small) shall specify 29 symbols. Codes 103-118 (large) shall specify the remaining 16.

3.2.1.4.4.8 <u>Fonts</u>. The small and large NTDS and ASCII fonts for codes 33-102 are shown in Appendix A.

3.2.1.4.5 Graphics Addressing

3.2.1.4.5.1 <u>Coordinate System.</u> Graphics parameters (position, length, etc.) shall be defined in two alternate coordinate systems, pixel coordinates (internal or display units) and data mile coordinates (external units). In the latter case one least-significant bit represents 1/64 dm, and the graphics position shall be relative to a Display Reference Coordinate (DRC). The position of the display raster shall therefore also be defined in data miles, relative to the DRC.

3.2.1.4.5.2 <u>Entities.</u> The smallest piece of graphics that can be identified (line, character, etc.) shall be called an Entity. A graphics Entity may be enabled, moved, suppressed or change intensity, but components of the entity may not be altered independently of other components of that entity (e.g., vector string).

3.2.1.4.5.3 <u>Tags.</u> All displayable graphics data shall be defined in Tag blocks and may be moved, deleted, or altered by reference to the tag block number.

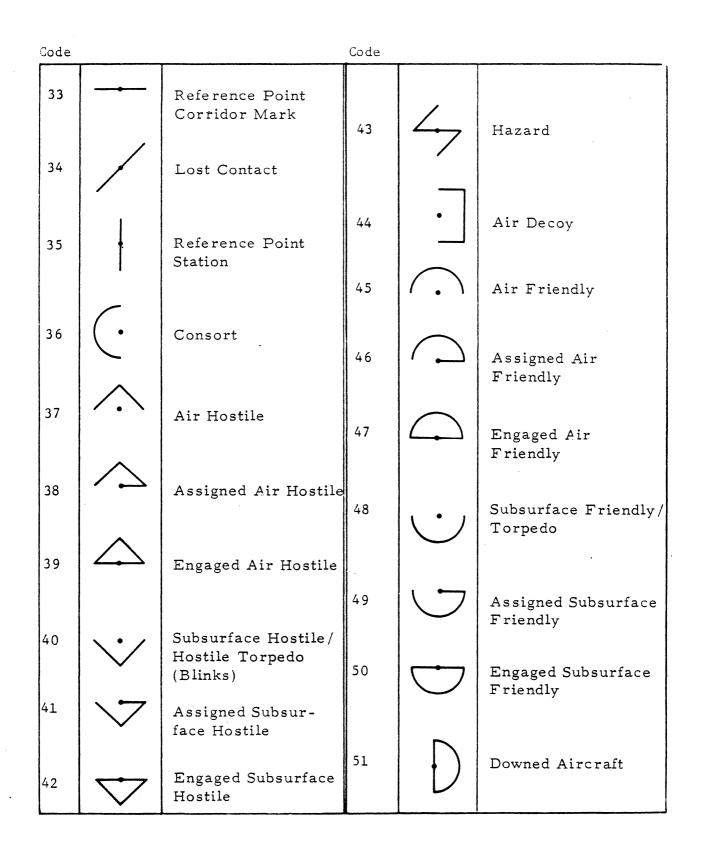


Table 3-7. NTDS Symbols (Sheet 1 of 7)

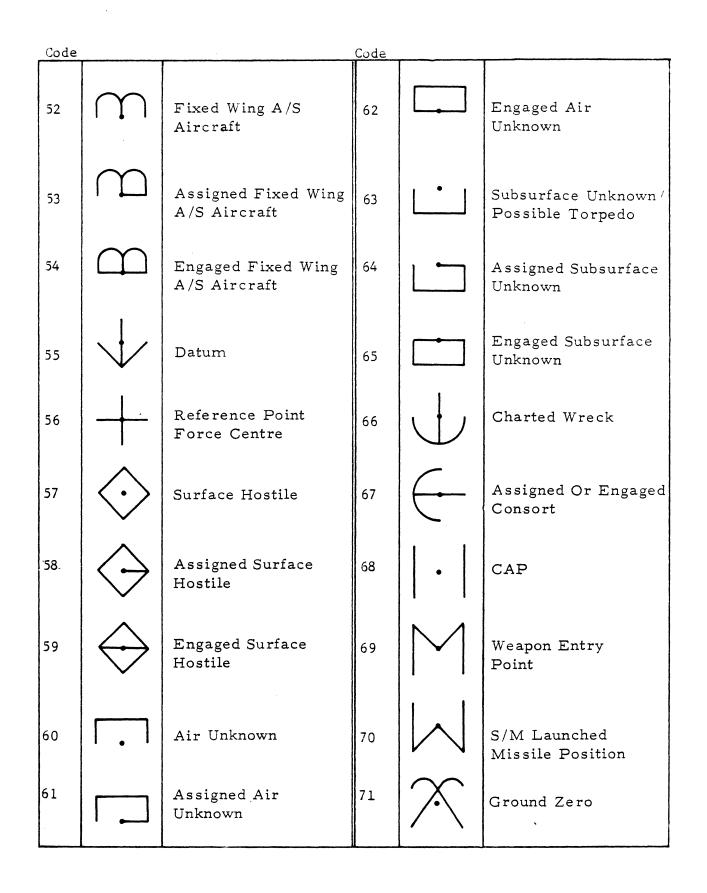


Table 3-7. NTDS Symbols (Sheet 2 of 7)

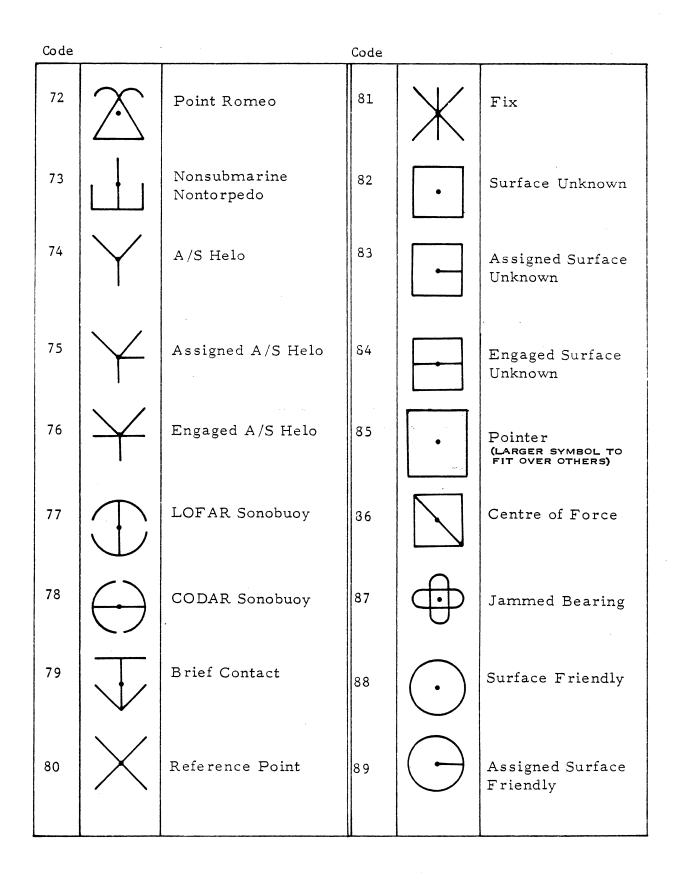


Table 3-7. NTDS Symbols (Sheet 3 of 7)

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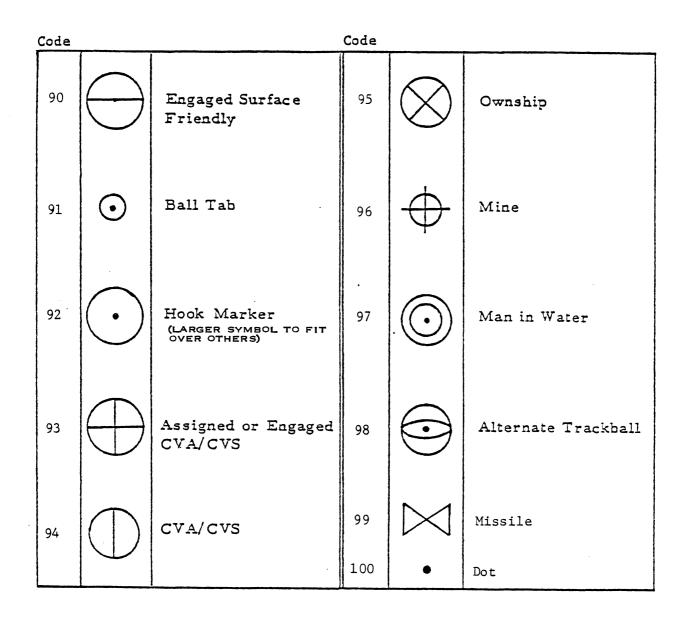


Table 3-7. NTDS Symbols (Sheet 4 of 7)

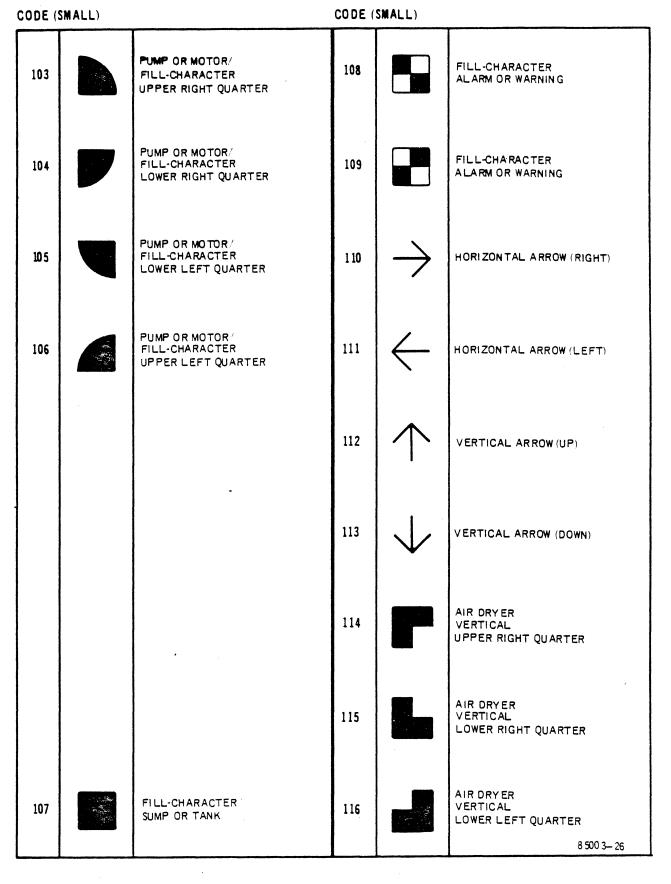


Table 3-7. NTDS Symbols (Sheet 5 of 7)

CODE (SMALL)

CODE (SMALL)

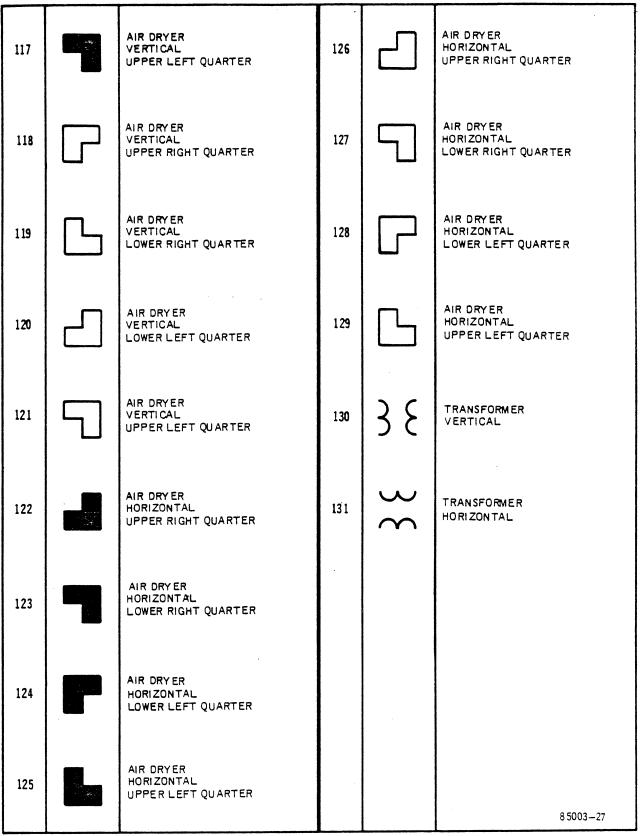


Table 3-7. NTDS Symbols (Sheet 6 of 7)

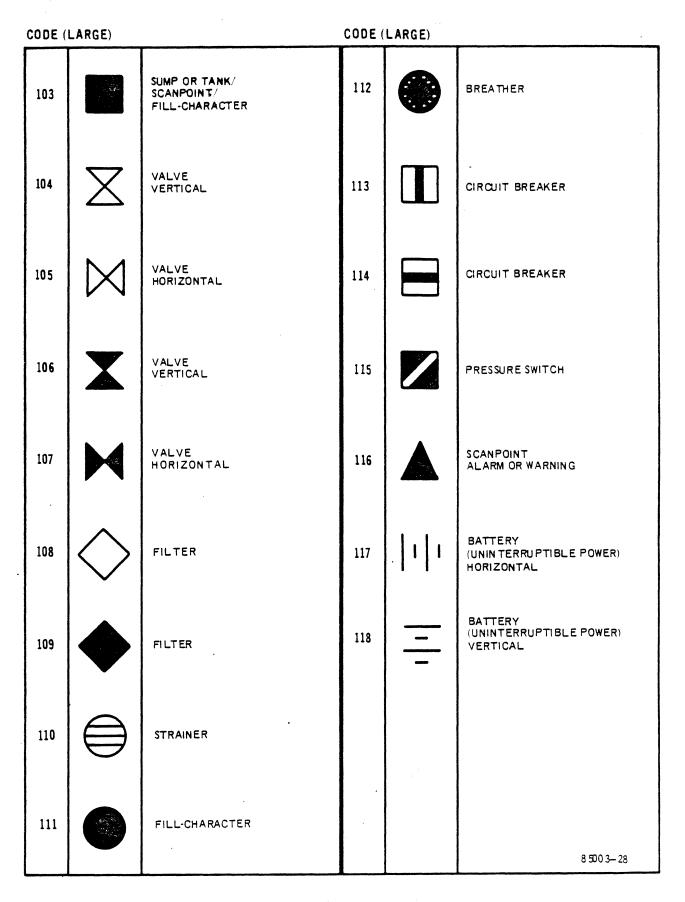


Table 3-7. NTDS Symbols (Sheet 7 of 7)

Quantity	Description
250	Dynamic tracks consisting of an NTDS symbol, 4 alphanumerics and a vector designation course and speed, 60 of these tracks have 6 history points.
120	Static tracks consisting of an NTDS symbol and 4 alphanumerics.
10	Track engagement lines.
4	Closest-point-of-approach and intercept vector and symbol.
40	General-purpose lines (e.g., firing arcs).
10	EW bearing lines.
10	Variable bearing lines.
5	Relative bearing lines.
l	Furthest-on-circle.
1	Torpedo danger area.
2	Utility circles.
10	Screens, formations, lost contact searches, sonobuoy plant patterns, etc.
50	Mapping vectors, average length 128 pixels.
1633	Alphanumeric text characters.

Table 3-8. Graphics Load

3.2.1.4.5.4 <u>Display File.</u> Tags shall be maintained in a Display File. The Display shall be periodically refreshed from this file to eliminate pinholing caused by the movement of intersecting entities. The Display File shall be large enough to accommodate the graphics load in Table 3-8, which requires approximately 13k words. Up to 140 dynamic tracks shall be updated to their new positions every second and static symbols shall be updated to reflect own ship motion in less than 1.5 seconds. These times are cumulative. Detailed definition of entity formats and sizes are given in ComDev Document 650211. 3.2.1.4.5.5 <u>Windowing</u>. The Display Processor shall define a rectangular field of view within the full graphics raster within which entities whose base position is defined in data miles shall be windowed. For most applications, this field-of-view shall be the same as the video overlay area up to the maximum of 1024 x 1024 pixels, although graphics-only applications may define the full raster (1535 x 1152) as the external-unit field-of-view. Entities defined in pixels shall be windowed by the raster. Those portions of all entities that fall within the defined window shall be displayed except for characters and symbols, when the entire symbol matrix must lie within the field-of-view for the symbol to be drawn.

The principle of operation is shown in Figure 3-4. It should be noted that the SSD Function Generator shall only compute addresses within the window. Out of bound addresses shall not be computed in order to minimize the total time taken to draw the entity.

3.2.1.4.6 <u>Graphics Magnification</u>. A graphics magnification of two and four times shall be provided. Only graphics within the video overlay window shall be magnified. See also 3.2.1.3.5.

3.2.1.4.7 <u>Cursor</u>. A trackball cursor symbol and cursor control shall be provided. The trackball cursor shall be constrained to move within the video or graphics field of view under Display Processor control. The cursor shall be positioned either by the Trackball or by the Display Processor. The cursor shall be selectable from a number of types by the Display Processor.

- Ball Tab Cursor. The shape shall be as shown in Figure (a) 3-5, of overall size 32 x 32 pixels. Cursor intensity shall be controlled from the Trackball intensity knob An identical cursor shall be positioned on the CUD. one pixel to the right and one pixel below the Cursor This shall always be set to the black levposition. el. Both components shall be enabled simultaneously. The effective composite cursor shall have a bright portion and a black portion, such that adequate contrast will be provided against either a bright or a dark video background. When defined by the DP to have its movement restricted to the Video Overlay area, the cursor symbol will stop with its center on the particular extremity of the video overlay area regardless of further movement of the trackball. When not so restricted, the cursor symbol will be positionable and 'windowed' within the full graphics (raster) area.
- (b) Horizontal Line Cursor. A Horizontal Line Cursor shall be enabled and programmed in length and X start position by the Display Processor, in multiples of 16 pixels. The line shall be positioned vertically by the Trackball or the Display Processor. Both line cursors shall consist of a bright line and a black line.

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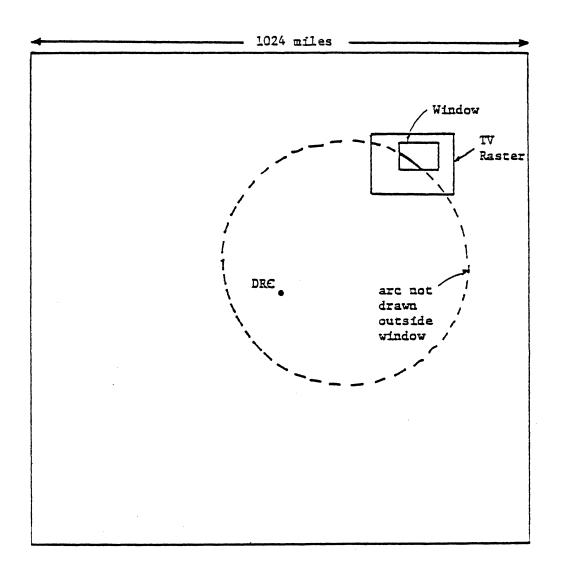


Figure 3-4. Windowing

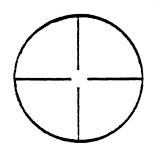


Figure 3-5. Cursor Shape

- (c) Vertical Line Cursor. A Vertical Line Cursor shall be enabled and Programmed in length and Y start position by the Display Processor, in multiples of 16 pixels. The line shall be positioned horizontally by the Trackball or by the Display Processor.
- (d) The Horizontal and Vertical Line cursors may be enabled independently or together.

3.2.1.4.8 <u>Graphics Scrolling.</u> The Graphics memory shall be scrolled in the Y direction independently of the Video Memory, by defining the Y address of the memory line desired at the top of the display. This address shall have a resolution of 2 lines.

3.2.1.5 <u>Elapsed Time Meter.</u> The DDA, CUD and TV Monitor shall contain an elapsed time meter which shall not be capable of being reset. The meter shall record the time that prime power has been applied to the equipment and shall be visible without requiring the removal of panels or covers. The range shall be 0 to 9999 hours. The meter shall be in accordance with MIL-M-7793.

3.2.1.6 <u>Battle Short</u>. A 'battle short' override feature shall be provided to permit system operation regardless of overheating advisory indications and its associated subsequent power supply shutdown.

3.2.2 <u>Physical Characteristics.</u> The SSD shall consist of three physical units:

Display Drive Assembly (DDA) TV Monitor Operator Control Unit (CUD)

The DDA shall be a 19-inch rack mountable module. The TV monitor shall be 24-inch rack mountable. Table 3-9 indicates the approximate sizes and weights of the modules.

Module	<u>Size (HxWxD inches)</u>	<u>Weight (lb)</u>
DDA	14 x 19 x 21	130
TV Monitor	17.5 x 24.0 x 20.0	110
CUD - CPD1 CPD2	5.9 x 24 x 15.72 3 x 24 x 4.00	18 5

Table 3-9. SSD Modules

3.2.2.1 <u>Equipment Cable Lengths.</u> The TV monitor and CUD shall be capable of 100 m separation from the DDA. The NATO STANAG 4153 interfaces shall be capable of operating over 100 m using TRF-58 cable.

3.2.2.2 <u>Exterior Finish.</u> All exterior surfaces shall be painted in light gray which matches the colour specified in MIL-E-15090.

3.2.3 <u>Reliability</u>

3.2.3.1 <u>Quantitative Reliability Requirements</u>. The specified MTBF for the SSD including the TV monitor shall not be less than 1000 hours when operated under the environmental conditions specified.

3.2.4 <u>Maintainability</u>. The mean corrective maintenance time (Mct) to repair the SSD shall not be greater than 45 minutes. The maximum corrective maintenance time (M max ct) shall be less than 2 hours at the 90th percentile. Equipment repair shall be by module replacement with repair of the module as a second or third line maintenance item. Faulty module identification shall be by BITE, fault indicators, and observation of the TV screen.

3.2.4.1 <u>Preventive Maintenance</u>. Preventive maintenance of the SSD shall be limited to the replacement of air filters.

3.2.4.2 <u>Accessibility</u>. Replaceable subassemblies of the DDA shall be accessible from the front of the rack-mounted equipment. Extra fans for cooling shall not be used when equipment is in the service position. Replacement subassemblies for the TV Monitor shall be accessable by removing the relevant panel from the monitor after it has been withdrawn from its console service position. The CUD subassemblies are accessed by first removing the CPD1 from the bullnose and disconnecting the rear cover of the panel. The time taken to remove equipment panels to gain access to test points or replacement modules shall not be greater than three minutes.

3.2.5 Environmental Conditions

3.2.5.1 <u>Temperature</u>. The SSD shall conform to the operating temperature conditions of range 4 of MIL-E-16400. The DDA shall be air cooled via self contained fans. The CUD and TV Monitor require no forced air cooling.

3.2.5.2 <u>Non-Operating Temperature</u>. The SSD shall be capable of extended storage within the non-operating range specified in MIL-E-16400 (-62 to 71°C). When the SSD is removed from storage and restored to the operating temperature range the equipment shall operate correctly with no mechanical or electrical damage.

3.2.5.3 <u>Shock.</u> The SSD Units shall be capable of withstanding the following shock tests.

DDAMIL-S-901 Grade A Class I, Type ATV Monitor, CUDMIL-S-901 Grade A Class II, Type A

When hard-mounted, the TV and CUD shall be capable of withstanding shock levels as tested per MIL-STD-810C Test Method 514.2 Procedure III (30g, 11 ms, 1/2 sine).

3.2.5.4 <u>Vibration</u>. The SSD shall be capable of withstanding the type 1 vibration test of MIL-STD-167.

3.2.5.5 <u>Humidity.</u> The SSD shall be capable of withstanding the humidity requirements as specified in MIL-E-16400.

3.2.5.6 <u>Salt Fog (Spray)</u>. The SSD shall be capable of withstanding the effects of the salt fog environment as specified in MIL-E-16400, para 3.3.5.4.

3.2.5.7 <u>Enclosure (Drip-proof)</u>. The degree of enclosure of the SSD shall be drip-proof (45 degrees) as defined in MIL-E-16400, para 3.7.2.1.

3.2.5.8 <u>Noise</u>. The SSD shall conform to the airborne and structureborne noise requirements for Grade A, Type 3 equipment in accordance with MIL-STD-740.

3.2.5.9 <u>Transportability</u>. The SSD equipment shall be capable of sufficient disassembly to allow shipping by commercial air and ground carriers. After reassembly no servicing or realignment shall be required for correct operation.

3.3 Design and Construction

3.3.1 <u>Material, Process and Parts.</u> Material and processes shall be contractors standards and procedures. Electronic parts (such as integrated circuits, semiconductors, electronic modules, resistors, etc.) shall be of military grade (MIL 883 level B2) to the maximum extent possible consistent with requirements herein.

3.3.2 <u>Electromagnetic Radiation.</u> The SSD shall withstand externally radiated narrow band field intensities and the electromagnetic interference requirements of MIL-STD-461B. These requirements are summarized in Table 3-10.

MIL-STD-461 Applicable Test	Test Description
CEOl	Power Line Conducted Emission (up to 15 kHz)
CE03	Power Line Conducted Emission (15 kHz to 50 MHz)
CE03	Signal Line Conducted Emission (15 kHz to 50 MHz)
CE07	Power Line Exported Switching Transients
REOL	System Radiated Magnetic Field Emission (30 Hz to 50 MHz)
REO2	System Radiated Electric Field Emission (14 kHz to 10 GHz)
CSOl	System Susceptibility to Power Line Conducted Interference (30 Hz to 30 kHz)
CS02	System Susceptibility to Power Line Conducted Interference (30 kHz to 400 MHz)
CS06	System Susceptibility to Power Line Conducted Spikes
RSOL	System Susceptibility to Radiated Magnetic Fields (30 Hz to 30 kHz)
RS02	System Susceptibility to Radiated Spike and Power Frequency Induced Fields
RS03	System Susceptibility to Radiated Electric Fields (14 kHz to 10 GHz)

Table 3-10. EMC Tests

3.4 Major Component Characteristics

The SSD shall consist of three major units:

- Display Driver Assembly (DDA)
- Operator Control Unit (CUD)
- TV Monitor

The following paragraphs specify the performance and physical characteristics of these units and/or their subassemblies.

3.4.1 Display Driver Assembly (DDA)

3.4.1.1. <u>Physical Characteristics of the DDA</u>. The electronics of the DDA shall be contained on circuit card assemblies (CCA). The electronics shall be powered by an integral power supply unit. An electrical chassis shall house these and contain the necessary interconnections. This chassis shall meet all the environmental and EMC requirements stated herein. Figure 3-6 is an outline and installation (O & I) drawing of the DDA and Figure 3-7 of a typical CCA.

The CCA shall have an extraction mechanism to ease insertion and extraction. It shall be appropriately stiffened to meet the vibration and shock requirements. Facility shall be provided on the CCA for keying to avoid seating the CCA in the wrong position. Connector(s) shall be employed to connect to the back plane wiring.

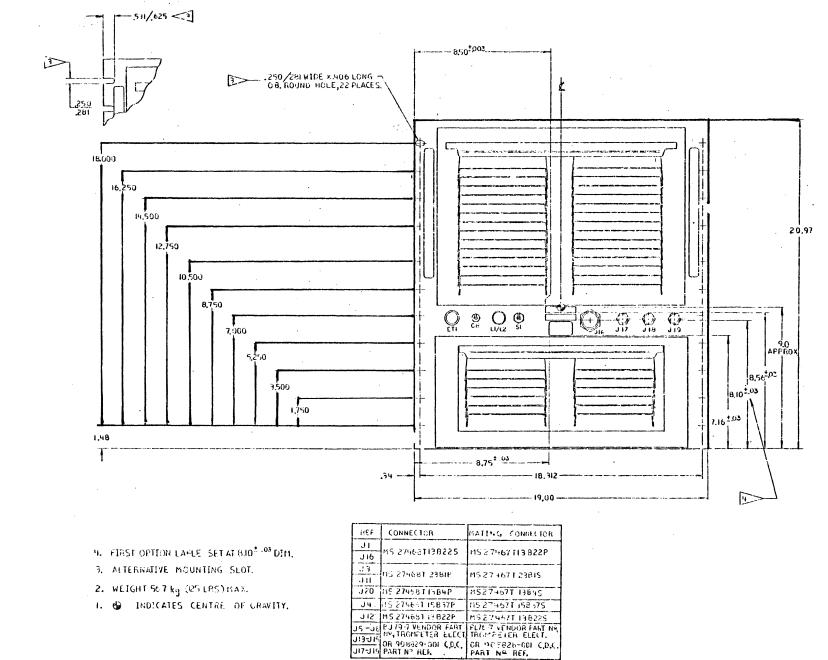
3.4.1.2 <u>Functional Characteristics of the DDA</u>. The DDA shall meet the functional requirements as stated in paragraphs 3.2.1.3 and 3.2.1.4 herein. These functions shall be performed by the CCAs as specified below. The block diagram of the DDA is shown in Figure 3-8.

3.4.1.2.1 <u>CCA</u>, <u>Display Controller (DC)</u>. The DC shall be a self contained microprocessor system. It shall interface with the CUD and display processor, and generally control the operation of the display. This control shall cause various sensor and graphics data to be displayed on the TV monitor.

The microprocessor shall be the Texas Instruments TMS 9900, supported by 16k words of DRAM and 14k words of program memory.

Capability to initiate built-in test routines shall be included. These routines shall be sufficient to isolate faults to a CCA/module.

3.4.1.2.2 <u>CCA, Coordinate Converter (CC)</u>. The CC shall accept normal Radar PPI range and bearing and convert these to the X-Y coordinate form of the display.



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٠ Outline and (Sheet Installati Ч 0 н on D ω Display Driver Assembly

Figure

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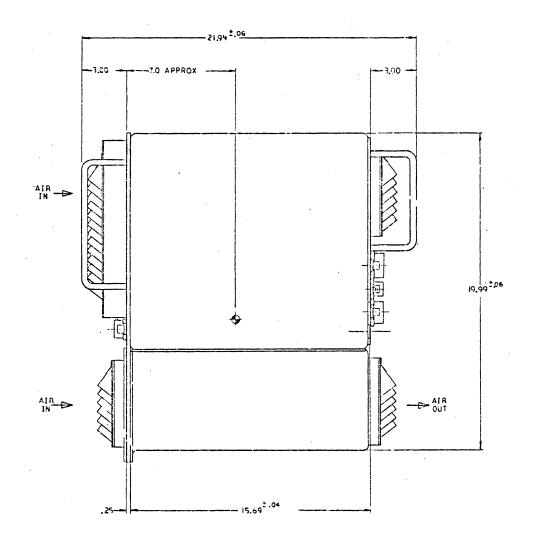


Figure 3-6. Outline and Installation Display Driver Assembly (Sheet 2 of 3)

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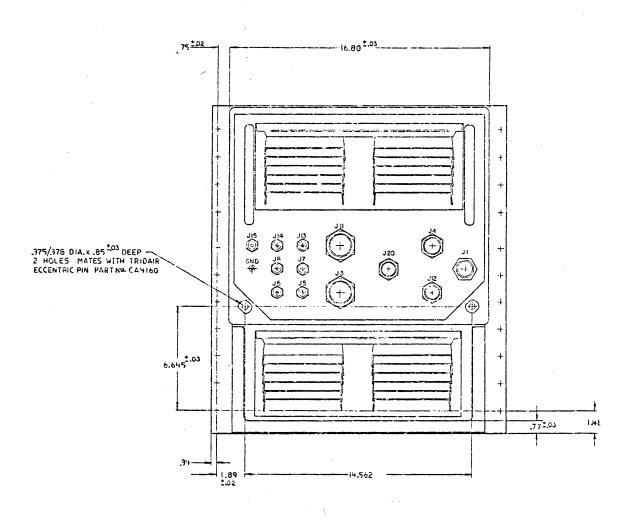


Figure 3-6. Outline and Installation Display Driver Assembly (Sheet 3 of 3)

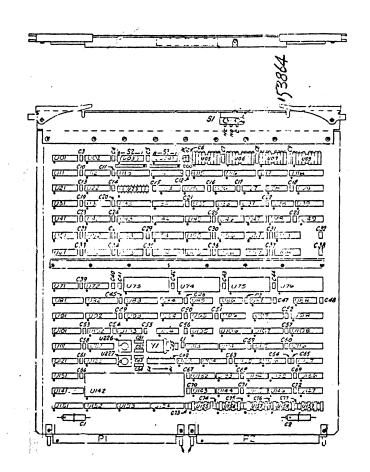
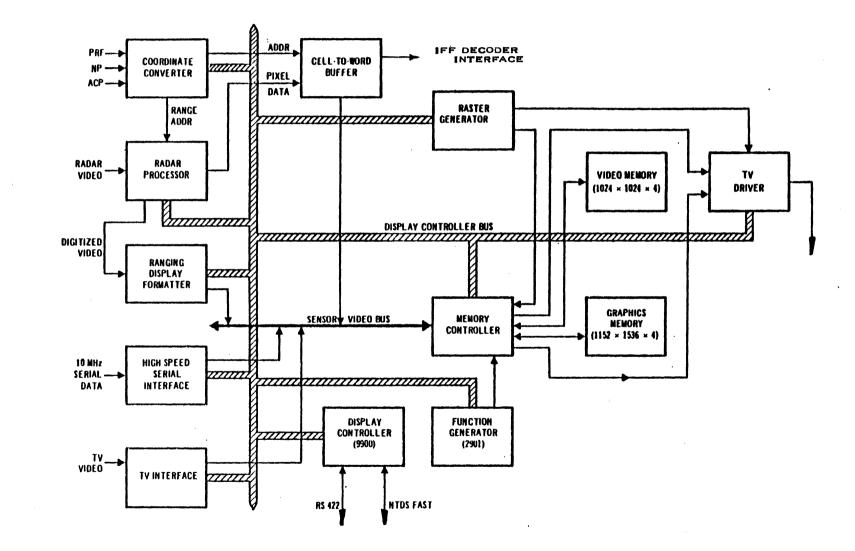


Figure 3-7. Circuit Card Assembly Display Controller



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Figure 3-8. DDA Block Diagram

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In addition, the following features shall be incorporated:

- (a) The ability to display a sector of the PPI in B-Scan (azimuth vs Range) form.
- (b) The ability to offset the centre of the PPI outside of the display Field of View (FOV) in order to effectively magnify any part of the original display.
- (c) The ability to prevent spoking of the display by filling in unmapped pixels based on the data provided for adjacent mapped pixels.

3.4.1.2.3 <u>CCA, Radar Processor (RP)</u>. The RP shall be the interface for all radar data. It shall output data suitable for display with the coordinates selected by the Coordinate Converter.

The radar input shall be selected from one of two sources, either a surveillance radar (normal PPI) or an A/R tracking radar. This signal shall be digitized. At each range increment the peak value of a selectable number of samples (or scale) shall be saved. Each peak value shall be filtered along the azimuth utilizing the following one pole recursive filter

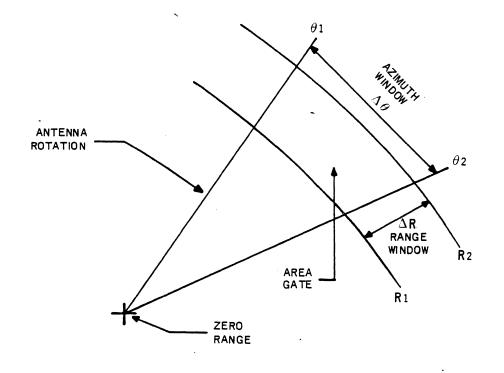
$$X_{new} = X_{old} + (X_{sample} - X_{old}) / 2^{K}$$

where k is the filter constant. The filtered data shall be applied to a level slice table (loaded by the DC) to produce four bits of filtered data for each range increment. These data shall be made available to the Cell to Word Buffer or the Ranging Display Formatter (paras 3.4.1.2.4 and 3.4.1.2.5 respectively) as appropriate.

3.4.1.2.4 <u>CCA, Cell to Word Buffer (CWB)</u>. The CWB shall provide an interface between the Coordinate Converter and the display video memory system. The CWB shall contain two buffer stores, one for the X and the other for Y. The buffers shall be organized to store up to 1024 4-bit data and 1024 10-bit addresses derived from the Coordinate Converter.

At the radar origin, peak detection shall be employed to maximize target detectability where many returns may be mapped to the same cell as a result of coordinate conversion process.

The CWB shall perform IFF area gating. An output shall be supplied that provides a compatible interface to the AN/UPA-59B IFF decoder. Parameters received from the DP shall be used to generate pulses to the AN/UPA-59B decoder that matches the area gate defined by the DP parameters. These parameters are R1, R2, Θ 1, Θ 2 (see Figure 3-9).



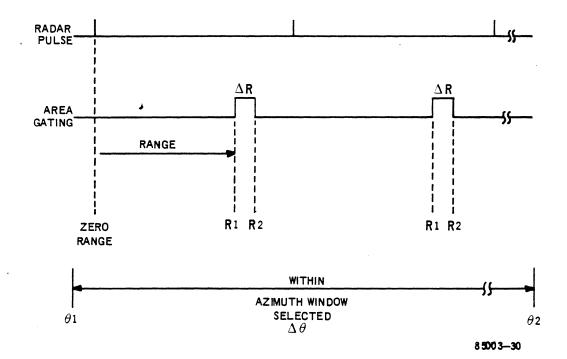


Figure 3-9. Azimuth/Range Gate or Area Gate

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3.4.1.2.5 <u>CCA, Ranging Display Formatter (RDF)</u>. The RDF shall provide a facility for simultaneous display of the A-scan and R-scan together with the reduced PPI display on the crt screen.

Two alternating memories for each scan shall be employed from which the erase and write information is extracted such that the wipe-out of the previous data always precedes the generation of a new pixel on the screen.

The maximum size assigned to each scan shall be 64 pixels in the Y axis and the placement of the scan on the video display area shall be determined by the Display Controller.

3.4.1.2.6 <u>CCA, High Speed Serial Interface (HSSI)</u>. HSSI shall receive digitized video information over a serial transmission line at a nominal rate of 10 megabits per second. To optimize the speed of the data transmission, the HSSI shall be controlled by a set of command words sent to the interface prior to data transmission. The information shall be transmitted using a Manchester II Split-Phase Modulation (also called Bi-Phase Level Modulation).

3.4.1.2.7 <u>CCA, TV Interface (TVI)</u>. The TVI shall enable the SSD to display television images resulting from any one of four standard line formats complying with RS-170 or RS-343 specifications, as appropriate. The line rates compatible with this interface shall be as given below:

Input Sensor Lines/Frame	Displayed Active <u>Lines</u>	Input Active Line Time (us)	Displayed <u>Pixels/Line</u>	Sampling Rate (MH2)	Sampling Line Time (us)
525	480	52.50	640	12.5	51.2
625	582	53.0	752	14.29	52.85
875	804	31.09	1024	33.3	30.72
1075	990	24.01	1024	50.0	20.48

The number of Pixels/Line shall be displayed within the Input Active Line Time to a resolution of 16 pixels.

The TVI shall accept the TV signal strip the sync off and digitize the resulting video to five bits. This data, compressed to 4 bits, is written to the video memory for display on the TV monitor.

The selection of the appropriate line rate to be processed shall be controlled by the Display Controller.

3.4.1.2.8 <u>CCA</u>, Function Generator (FG). The FG shall create graphics data on command from the Display Controller. This data will be written into the graphics memory via the Memory Controller for subsequent display.

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The processing shall be performed by 2900 series bit slice components. Along with this microprogram memory, sufficient scratch pad memory and look-up table ROM shall be provided. The data inputs and outputs shall be pipelined to keep the cycle time to a minimum.

3.4.1.2.9 <u>CCA, Memory Controller (MC)</u>. The MC shall be the interface between the display refresh memory (video and graphics), and the sensor data and Function Generator data. It shall perform the following functions:

- (a) Address and control interface with video data and Raster Generator.
- (b) Combine input addresses into a single video memory address bus.
- (c) Generate control logic for all video and graphics memory operations.
- (d) Address and control interface with the Function Generator.
- (e) Combine FG and TV refresh addresses to generate addresses to the Graphics Memory.
- (f) Interface with the Display Controller and execute its command in the control of the memory system.

3.4.1.2.10 <u>CCA</u>, Video Memory (VM). The VM shall be organized to accept 1024 x 1024 pixels, 4 bits deep, of sensor information. The Display Controller shall be provided with the facility (via the Memory Controller) to access the VM, primarily for test purposes. To reduce bandwidth requirements in the VM, the stored data shall be transferred into a buffer, one TV line at a time. The buffer shall then be read out synchronously with the TV signals for display on the Monitor.

A high speed arithmetic section shall be provided to perform the following:

- (a) Target trailing.
- (b) Scan-to-scan integration using a one-pole recursive filter of the type:

$$S_{n+1} = S_n + (X_{n+1} - S_n) / 2^k$$

- (c) Peak detection.
- (d) Memory erase.

It shall also be possible to pass input data unmodified (raw) for display.

3.4.1.2.11 <u>CCA, Graphics Memory (GM)</u>. The GM shall be organized to accept graphics data in a 1536 x 1152 pixel form. Each pixel shall be 4 bits deep (one for each of the three colours and one for blink) and originating in the Function Generator (via the Memory Controller). The Display Controller shall be provided with the facility of bypassing the Function Generator and accessing the GM directly (via the Memory Controller). To reduce the bandwidth requirements on the GM, the stored data shall be transferred into a buffer, one complete TV line at a time. The buffer shall then be read out synchronously with the TV raster signals for display on the monitor.

3.4.1.2.12 <u>CCA, Raster Generator (RG)</u>. The RG shall generate syncrhonization signals capable of driving a display monitor handling 1225 scanning lines with a field rate of 60 Hz, interlaced 2:1. These signals shall be compliant with RS-343 in order to drive a TV monitor compliant with RS-412. The number of active (viewable) lines shall be 1152 with the remainder of the scanning lines occurring during vertical blanking. The number of pixels displayed during each line scan shall be 1536, yielding an aspect ratio of 4:3.

The raster logic shall transfer data from the video and graphics memory modules to their respective line buffer store memories and then present the data to the TV Driver module.

The FG shall provide the facility of x2 or x4 display magnification under the command of the Display Controller. It shall also be possible via Display Controller command(s) to define a video area and its position on the TV screen.

3.4.1.2.13 <u>CCA, TV Driver (TVD)</u>. TVD shall accept digital video, graphics and cursor display data. It shall provide the necessary data manipulation and cursor symbol generation to drive an RGB display monitor. Output drive characteristics shall be per RS-343 performance standard. The TVD shall drive a 1225-line display monitor at a 60 Hz field rate with a 2:1 interlace. Each active line shall contain 1536 pixels and each frame 1152 active lines. Each pixel of the display information shall be one of the following:

(a) Video data received from the Video Memory via the Raster Generator Module on a pixel by pixel basis (4 bits).

- (b) Graphics display data from the Graphics Memory. Each colour shall be controlled independently.
- (c) Trackball, horizontal line or vertical line cursor.

The TVD shall utilize a priority system such that the video and graphics information is inhibited if any cursor information is present, and video output data shall be suppressed if any graphics information is present.

3.4.1.2.14 <u>Power Supply Unit (PSU)</u>. The following are the functional paragraphs taken from the ComDev Specification Control Drawing 907943.

3.4.1.2.14.1 <u>Primary Input Power</u>. The PSU shall meet performance requirements when supplied with 102-130V ac, 45 to 63 Hz, single phase, Type 1, NATO STANAG 1008.

3.4.1.2.14.2 <u>Output Power</u>. The PSU shall be capable of simultaneously producing all of its regulated dc output voltages $(\pm 1\%)$ over their required load ranges. Each output shall be isolated from the remaining outputs and ground.

3.4.1.2.14.3 <u>Ripple and Noise</u>. The peak to peak ripple and noise spikes, hash, periodic and aperiodic components shall be kept to a minimum over the frequency band dc to 25 MHz.

3.4.1.2.14.4 <u>Efficiency</u>. When operating within the input voltage range indicated in para 3.4.1.2.14.1 and a power load range of 75 to 100%, the PSU shall have an efficiency of at least 60% over the environmental operating conditions specified herein.

3.4.1.2.14.5 <u>Output Inhibit Control</u>. A control line shall be provided for remote on/off control of the DC power rails. The control line shall be suitably buffered to protect the PSU from damage due to induced coupled energy.

3.4.1.2.14.6 <u>Remote Sense</u>. The PSU shall have a remote sensory capability and shall not cause an overdrive condition when opened.

3.4.1.2.14.7 <u>Current Limiting</u>. The power supplies shall contain integral current limiting such that the maximum current drawn on a given power rail shall be limited to 125% of the maximum operating current specified. The PSU shall not be damaged by a permanent short circuit between any of the output power or output return terminals.

3.4.1.2.14.8 Over Voltage Protection. The over voltage protection shall limit each output voltage to 120% of the specified DC rails. Output power shall be removed from all rails if an over voltage condition is sensed on any rail.

3.4.1.2.14.9 <u>Fault Monitor Signal</u>. A signal line shall be provided to indicate the serviceability of any or all of the power rails. The fault monitor line shall be suitably buffered to protect the PSU from damage due to induced coupled energy.

3.4.1.2.14.10 <u>Overtemperature</u>. The power supply shall include a temperature sensing device to signal excessive temperature build-up due to an internal malfunction.

3.4.1.2.14.11 <u>Fault Indicators</u>. Indicators, one for each rail, shall be provided to indicate an overvoltage or undervoltage condition. Input line voltage shall be monitored and an indicator provided which shall illuminate when the line is greater than a specified minimum.

3.4.1.3 <u>Electrical Chassis Characteristics</u>. This chassis shall be the mechanical enclosure that will contain the CCAs and PSU of the DDA. The enclosure shall meet the environmental conditions of shock and vibration, and provide the EMI shielding and drip proofing, as specified herein.

It shall consist of an interconnection back plane to accept the CCA, cooling fans as required, connectors to interface with external equipment, and necesary controls and indicators to operate the DDA (power on/off switch, elapsed time indicator, etc.).

To facilitate handling of the DDA, appropriate handles shall be provided.

3.4.2 <u>TV Monitor Characteristics</u>. The complete operating requirements are covered in ComDev Specification 907611.

3.4.2.1 <u>Physical Characteristics</u>. The monitor shall be capable of being mounted into a standard 24-inch rack. To facilitate field maintenance, it shall be provided with mounting slides and handles.

Its construction shall meet the environmental and EMC conditions specified herein. It shall be modular for ease of maintenance. It shall not be necessary to remove the unit from its mounting to gain access to these modules. All electronic parts except the crt shall be solid state.

Figure 3-10 is an O & I drawing of the TV monitor.

3.4.2.2 <u>Performance Characteristics</u>. The monitor shall be capable of colour display. It shall accept three inputs, one for each Red, Green and Blue (RGB) primaries. Each of the RGB inputs shall be capable of accepting data conforming to RS-412. It shall be capable of displaying a picture with each of the RGB inputs organized as follows:

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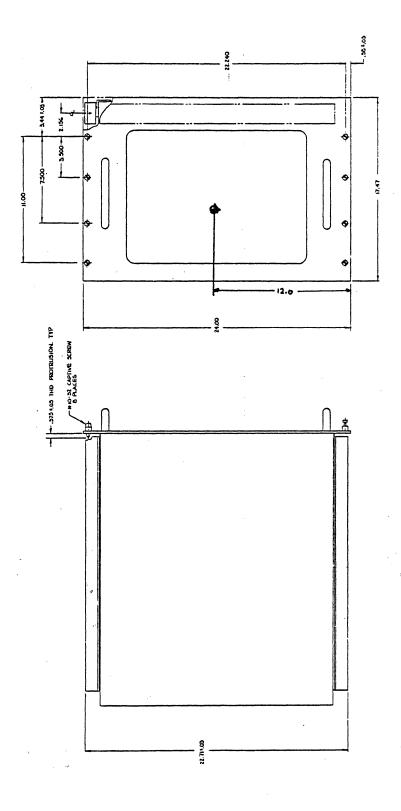
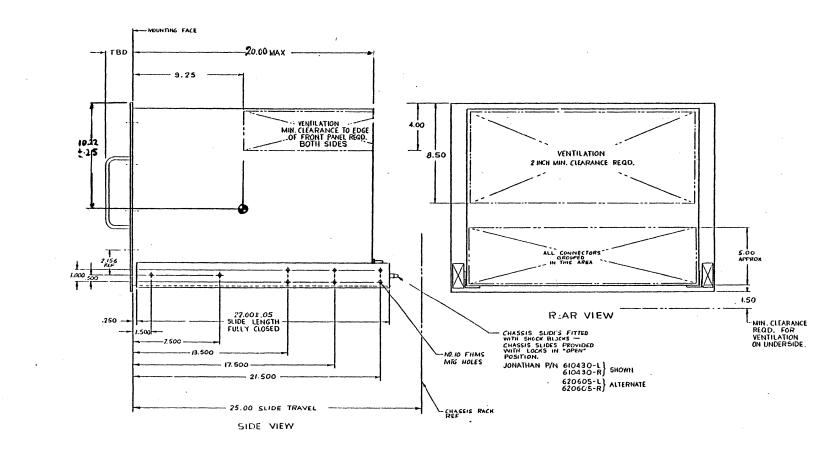


Figure 3-10. O&I Drawing of TV Monitor (Sheet 1 of 2)





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total lines scanned	1225
active lines	1152
active pixels per line	1536
interlaced	2:1
frame rate	30 Hz

The crt shall be 19 inch (diagonal) utilizing a shadow mask technique. The mask shall have a triad pitch of 0.31 mm. The phosphor shall be such as to present no perceiveable flicker.

The bandwidth of the RGB video amplifiers shall be 50 MHz minimum. Spot size shall be less than 0.015 inch within an 11.5 inch diameter centered circle and 0.020 inch in the corners. Convergence error shall be less than 0.015 inch within a 9-inch centred circle and 0.020 inch elsewhere.

It shall be possible to display white and 6 other distinct colours. Once these are selected, it shall be possible to vary the intensity of these by varying the RGB amplitude.

3.4.3 <u>CUD Characteristics</u>. The CUD shall consist of two separate subassemblies (Figure 3-11). Each subassembly shall be designed to meet the environmental and maintainability requirements specified herein irrespective of how they may be integrated into the operator's work station. The two subassemblies shall be partitioned as follows:

- CPD-1 containing keyboard, trackball, etc. (as shown on Figure 3-2)
- CPD-2 containing power switch, variable controls, etc. (as shown on Figure 3-2)

The contents of the two panels are described in paras 3.2.1.2. 3.1 and 3.2.1.2.3.2. The electronics to control the CUD and to interface with the DDA along with the power supply shall be included in the CPD-1 subassembly. This assembly shall also contain an Elapsed Time Meter capable of indicating up to 9999.9 hours of operation. All CUD lamps except the Caps Lock indicator shall be replaceable from the front.

The subassemblies shall be interconnected through suitable cabling having connectors at both ends (Figure 3-12).

The LOCK, HOME, SEQ, and HOOK QABs and the keyboard shall have suitable protection barriers to avoid inadvertent activation by items such as books, etc., which may be laid on the surface during the normal operation.

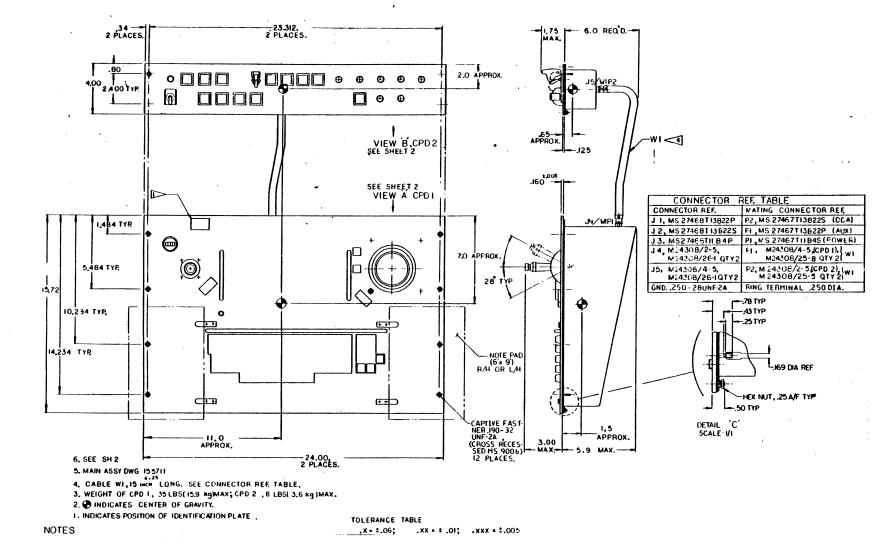
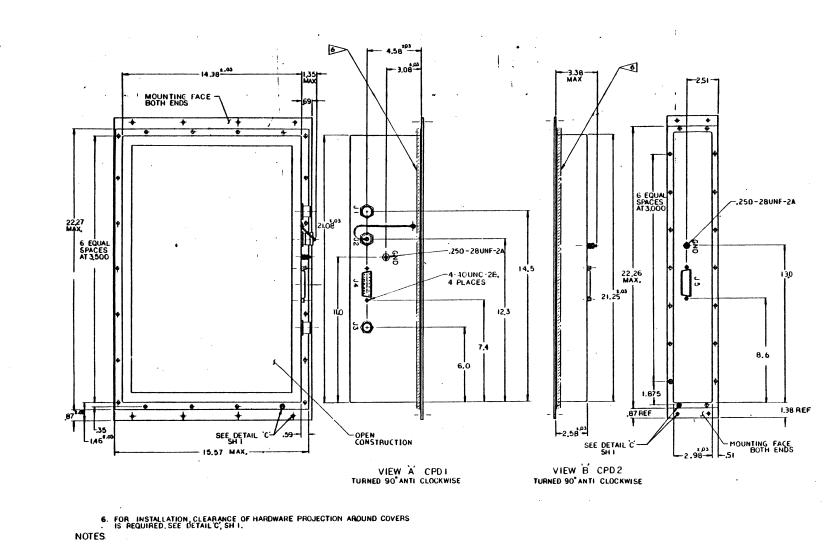


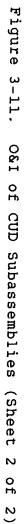
Figure ω Ι 11 ٠ 0& I ο Ť. CUD Subassemblie S (Shee rt 1 0 Ťb. Ν

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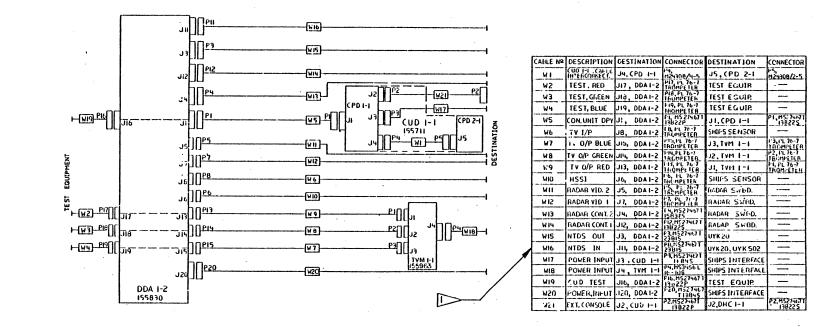
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I. FOR UYK 502 OPERATION WIG CABLE IS ATTACHED TO NOTES JII ONLY.

Figure

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erface Cabling

4. QUALITY ASSURANCE

4.1 General Conditions

4.1.1 <u>Responsibility for Test</u>. The contractor shall be responsible for the performance of all tests. The contractor may use his own or any other facilities suitable for testing purposes.

4.1.2 <u>Test Plan</u>. The contractor shall prepare a test plan which contains the procedures, data forms, a list of test equipment and the sequence of tests for performing factory and qualification testing.

4.1.3 <u>Test Reports</u>. Reports containing the results of a test or sequence of tests shall be submitted no later than 15 days after the completion of the tests.

4.1.4 <u>Qualification Testing</u>. Qualification testing shall be carried out only on items not previously qualified. A configuration of testing shall be selected to provide worst case operating conditions to ensure that specification requirements will be met.

4.1.5 <u>Factory Acceptance Test Procedures (ATP)</u>. The contractor shall submit an ATP for approval. This ATP shall be used to test all production SSDs, in preparation for their delivery.

4.2 Quality Conformance Inspection

4.2.1 <u>Factory Testing</u>. All production SSDs shall undergo thorough factory testing which will include surface examination, debug and checkout, performance testing and burn-in.

Surface examination shall be performed to ensure compliance with appropriate quality and workmanship standards. After this inspection, the SSD shall undergo a debug and checkout process to remove any latent manufacturing errors.

After successful completion of the above process, a thorough performance test in accordance with the approved ATP shall be performed. The equipment shall then undergo a burn-in period of (24) hours with the last (8) hours to be failure free.

4.2.2 <u>Qualification Testing</u>. One production unit shall be designated to undergo a series of qualification tests to determine compliance with this Specification. The following inspections and tests shall be performed:

- (a) Surface examination: MIL-E-16400G, para 4.8.1
- (b) Performance testing: ATP

(c) Vibration: MIL-STD-167-1, Type 1

- (d) Shock: DDA: MIL S-901 Grade A, Class I, Type A TV,CUD: MIL-STD-810C, Test Method 514.2 Procedure III (30g, 11 ms, 1/2 sine)
- (e) Temperature: Method 501 and 502 of MIL-STD-810
- (f) Humidity: Method 507, Procedure IV of MIL-STD-810
- (g) EMC: MIL-STD-461B
- (h) Salt Fog: Method 509 of MIL-STD-810
- (j) Power Transients: STANAG 1008, Type I
- (k) Steady State Power: STANAG 1008, Type I(115V <u>+</u>8%)
- (m) Acoustic Noise: MIL-STD-740 Airborne, Structure-

borne

(n) Drip Test: MIL-STD-108, drip proof (45°)

(p) Inclination MIL-E-16400G, para 3.3.5.15

After these tests, the equipment shall be refurbished and await disposition instructions from the procuring agency. Refurbishment shall ensure that the equipment passes mechanical, workmanship and functional inspection.

4.2.3 <u>Testing Criteria</u>. All test failures shall be classified as minor or major failures by the Design Authority. If minor failures occur the test shall be stopped, repairs made or the failure analyzed and the test continued or repeated as required by the individual test requirement. If major failures occur the test shall be discontinued, the contractor shall submit a failure analysis report, repair the equipment and repeat the entire test. All necessary changes discovered during testing shall be retrofitted on all delivered systems and spares at the contractors own expense. 4.3 <u>Test Matrix</u>. Table 4-1 defines those items to be verified by Qualification, Verification (First Article) and Acceptance Tests. Verification Tests shall be performed whenever a new configuration of firmware is implemented. Tests shall be performed as defined by Analysis (A) or Demonstration (D).

<u>Requirement</u>	Paragraph	Verification	Acceptance	Qualifi
Item Definition	3.1	D	D	
Item Diagram	3.1.1	A ·	A	
High Resolution TV Monitor	3.1.1.1	D	D	
-		(TV ATP)		
Display Driver Assembly	3.1.1.2	D	D	
Operator Control Unit	3.1.1.3	D	D	
External Computer	3.1.1.4	D	D	
Radar Interface	3.1.2.1.1	. D	D	
TV Interface	3.1.2.1.2	D	D	1
Computer Interface	3.1.2.1.3	D	D	
High Speed Serial Interface	3.1.2.1.4	D.	D	
Electrical Power Interface	3.1.2.2	D (First Ar	ticle)	
Internal Interfaces	3.1.2.3	D	D	
DDA to TV	3.1.2.3.1	D		
DDA to CUD Interface	3.1.2.3.2	D		
Software Interface	3.1.2.4	D	D	
Display Processor to DDA Software Interface	3.1.2.4.1	D	D	1
Major Commponents List	3.1.3	A	A	1
CUD Function	3.2.1.2.2	D	D	
Operators Control Panels	3.2.1.2.3	D	D	
Primary Controls	3.2.1.2.3.1	D	D	
Secondary Controls	3.2.1.2.3.2	D	D	
Interface	3.2.1.2.4	A		
Display Format	3.2.1.3.1	D	D	1
Colour Intensity Characteristics	3.2.1.3.1.1	D	D	
Radar Resolution	3.2.1.3.2.1	D,A	D	1
Radar Azimuth Processing	3.2.1.3.2.2	D,A	D	
Plan Position Indicator	3.2.1.3.2.3	D	D	
B-Scan	3.2.1.3.2.4	D	D	1
A/R Scan	3.2.1.3.2.5	D	D	
IFF Area Gate	3.2.1.3.2.6	D	D	1
Display Format	3.2.1.3.3.1	D	D	1
Image Processing	3.2.1.3.3.2	D	D	1
Line Scan Sensor Display	3.2.1.3.4	D	D	
Magnification	3.2.1.3.5	D	D	
Video Memory Scrolling	3.2.1.3.6	D	D	
Freeze	3.2.1.3.7	D	D	1
Scan to Scan Integration	3.2.1.3.8	D	D	
Target Trails	3.2.1.3.9	D	D	

Table 4-1. Verification Test Requirements

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Requirement	Paragraph	Verification	<u>Acceptance</u>	<u>Qualificati</u>
Peak Detect	3.2.1.3.10	D	D	
Continous Erase	3.2.1.3.11	D	D	
Graphics Display Area	3.2.1.4.1	D	D	
Brightness Levels	3.2.1.4.2	D	D	
Blink Rate	3.2.1.4.3	D	D	
Graphics Repetoire	3.2.1.4.4	D	D	
ASC II Characters	3.2.1.4.4.1	D	D	
Vectors	3.2.1.4.4.2	D	D	
Arcs and Circles	3.2.1.4.4.3	D	D	
Fixed Line Types	3.2.1.4.4.4	D	D	
User Programmable Line Types	3.2.1.4.4.5	D	D	
User Programmable Characters	3.2.1.4.4.6		D	
NTDS Characters	3.2.1.4.4.7	D	. D	
Fonts	3.2.1.4.4.8	D	D	1
Coordinate System	3.2.1.4.5.1	D	U	
	3.2.1.4.5.2	D		
Fags	3.2.1.4.5.3	D		
Display File	3.2.1.4.5.4			
Vindowing	3.2.1.4.5.5	D		
Graphics Magnification	3.2.1.4.6	D	D	
Cursor	3.2.1.4.7	D	D	
Graphics Scrolling	3.2.1.4.8	D	D	
Elapsed Time Meter	3.2.1.5	D	D	
Battle Short	3.2.1.6	D	D	
Physical Characteristics	3.2.2	D	L L	
Equipment Cable Lengths	3.2.2.1	D		
Exterior Finish	3.2.2.2	Å		
Quantitation Reliability Requirements	3.2.3.1	Å		
Maintainability	3.2.4	Å		
Preventive Maintenance	3.2.4.1	A		
Accessiblity	3.2.4.2	Å		
Gemperature	3.2.5.1	-		D
Non-Operating Temperature	3.2.5.2			D
Shock	3.2.5.3			D
Vibration	3.2.5.4			D
fumidity	3.2.5.5			D
Salt Fog	3.2.5.6			D
Enclosure (Drip-proof)	3.2.5.7			D
Noise	3.2.5.8			D
Fransportability	3.2.5.9	D	D	
Material, Process and Parts	3.3.1	Å		
Electromagnetic Radiation	3.3.2			р
Physical Characteristics of DDA	3.4.1.1	D (First A	sticle)	ŀ
TV Monitor Characteristics	3.4.2	D (First A)		
CUD Characteristics	3.4.3	D (First A)		

Table 4-1. Verification Test Requirements (Sheet

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5. PREPARATION FOR DELIVERY

5.1 <u>Preservation</u>, <u>Packaging</u> and <u>Packing</u>. Preservation, packaging and packing shall be to level C as defined in Federal Standard 102B (FED-STD-102) of January 2, 1963.

5.2 <u>Marking</u>. Marking shall be in accordance with Federal Standard 123A (FED-STD-123) of June 29, 1970. Each shipping container shall be legibly marked with water resistant paint or ink in accordance with the following:

Item Name

Specification and Serial Number

Contract Number

Manufacturer's Name and Trademark

Handling Precautions as deemed necessary by the contractor

6. NOTES

6.1 <u>SSD Configuration Options</u>. The SSD specified herein fulfills the requirements for a complete multisensor display. However, there are applications that do not need the full capability. In recognition of this, the SSD can be configured into several options. The differences in these configurations lie only in the CCA population of the DDA and choice of TV monitor. All other non-functional requirements of this specification apply.

Table 6-1 contains the CCA complement for the different options available. If monochrome operation is desireable, only one Graphics Memory CCA is required.

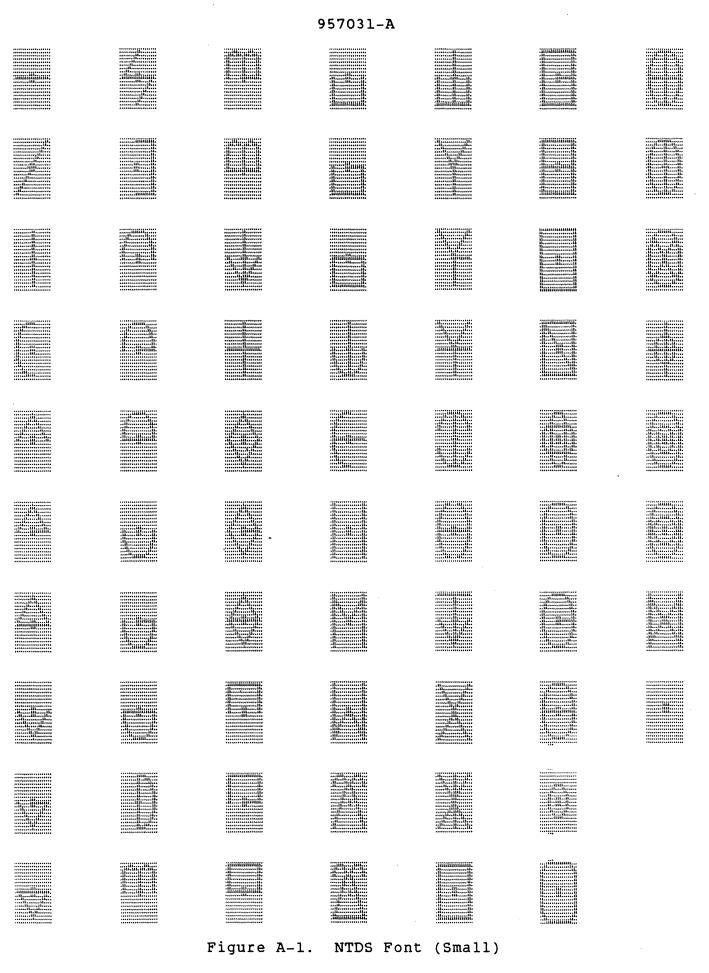
CCA			Us	er Opti	ons			
Descrip-	Graphics	Fullup				Radar	Radar	HSSI
tion	Only	Option	HSSI	Radar	TV	+ HSSI	+ TV	+ TV
Display Controller	X	x	x	x	x	х	X	X
Function Generator	x	х	x	x	x	x	х	x
Memory Controller	x	x	x	X	X	X	X	x
Graphics Memory (Qty 2)	x	x	x	x	X	Х	X	x
Raster Generator	x	X	x	X	X	x	x	x
TV Driver	_ x	x	x	X .	x	x	x	x
Video Memory (Qty 4)		X	x	x	X	X	x	X
Coordinate Converter		x		x		х	x	
Radar Processor		x		X		Х	X	
Cell-to- Word Buffer		x		x		х	x	
Ranging Display Formatter		x		x		Х	x	
High Speed Serial Interface		X	x			X		x
TV Interface		x			x		x	Х
Total CCA Count	7	17	12	15	12	16	16	13

Table 6-1. SSD Configurations

APPENDIX A

NTDS AND ASCII FONTS

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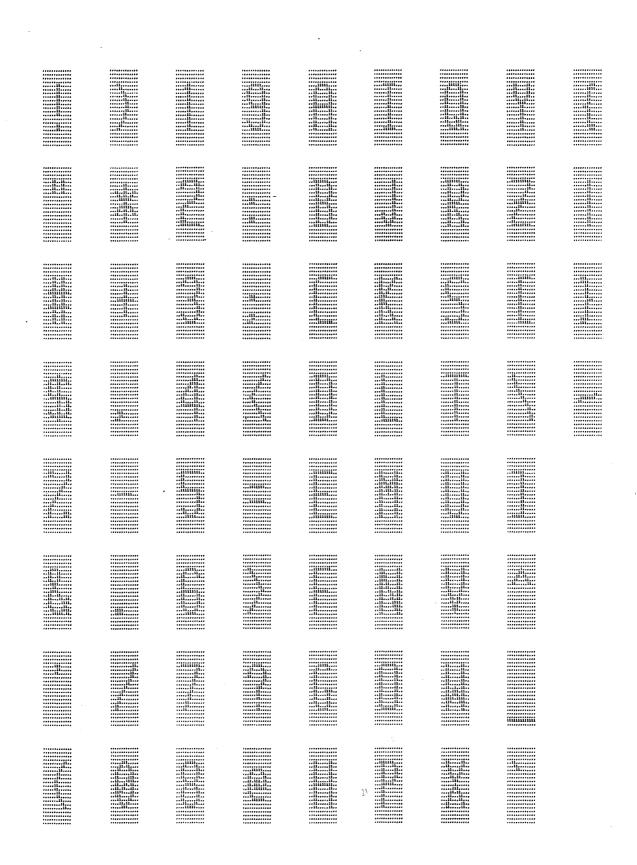


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Figure A-2. NTDS Font (Large)

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Figure A-3. ASCII Font (Small)

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Figure A-4. ASCII Font (Large)

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