

CONTROL DATA® 6638 DISK FILE SYSTEM

**STANDARD OPTION 10037-A
6639-A/B DISK FILE CONTROLLER**

**DIAGRAMS AND
CIRCUIT DESCRIPTION
MAINTENANCE
MAINTENANCE AIDS
PARTS LIST
WIRE LISTS
CHASSIS TABS**

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

SHEET 1 OF 1

| | | EQUIPMENTS | | | | | |
|-----------------------|-------------------|-------------------|--------|--------------------|--|--|--|
| MANUAL REV | FCO OR ECO | 6639-A | 6639-B | St. Opt 10037-A | | | |
| F | FCO29035 | A09 | B08 | A09 | | | |
| G | ECO34071 | A09 | B08 | A09 | | | |
| | ECO34061 | A10 | B09 | A10 | | | |
| H | FCO34710 | A11 | B10 | A11 | | | |

PREFACE

The CONTROL DATA[®] 6638 Disk File System consists of a large capacity disk file with two independent positioning controls, and a controller for interfacing the disk to a CONTROL DATA[®] 6000 Series Computer. CONTROL DATA[®] Standard Option 10037-A supplements the normal time-shared access to the file (one read-write control services two data channels) with a second read-write control, thereby permitting simultaneous access to the file.

Logic diagrams contained in this manual do not attempt to show the entire device. The purpose of the diagrams is to show the logical significance of circuits that may involve parts of many modules. The logic diagrams do not replace the chassis tabs, but they are a valuable tool in understanding the tabs and the overall operation of the controller.

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SECTION 1
GENERAL DESCRIPTION

SECTION 2
OPERATION AND PROGRAMMING

(Refer to 6638 Disk File Subsystem Reference Manual,
Publication No. 60334100 for information on these sections.)

SECTION 3
INSTALLATION AND CHECKOUT

SECTION 4
THEORY OF OPERATION

(These sections are not available.)

SECTION 5

DIAGRAMS

KEY TO LOGIC SYMBOLS

Logic diagrams represent a symbolic approach to electronic schematics. By using symbols to represent building block circuits, the schematic becomes easy to read if the reader understands the function of the symbols. In CONTROL DATA[®] logic, two signals, a "0" and a "1" are the possible input or output conditions of a circuit. For example, "1" is considered "up" and "0" is considered "down" on a timing chart. Detailed descriptions of logic symbols and their associated electronic representations are contained in the Printed Circuit Manual, Cordwood Modules. See Literature Distribution Center Catalog for publication numbers.

STANDARD LOGIC SYMBOLS

Standard logic diagram symbols for Control Data equipment using 6000 Series card types are inverters, test points, flip-flops, twisted pair line drivers, and coaxial cable line drivers.

Inverters

An inverter is a logic element which provides an output that is a negation of its input. When more than one input is provided to an inverter, "0's" take precedence over "1's" and therefore drive the output of the inverter to "1". Because all of the several inputs have to be "1" to drive the output of the inverter to a "0", the inverter may be considered an inverting AND (or NAND) gate when more than one input is present. The basic inverter is shown in the logic diagrams as an arrow into either a circle or a square (Figure 1). Both symbols represent the same electronic circuit and have the same logic interpretation. In a logic sequence of inverters, circle and square symbols are usually alternated as an aid in tracing signals, e.g., a "1" output from a square symbol implies a "1" output from subsequent squares in the logic chain.



Figure 1. Inverter Symbols

Certain card types employ variations of the standard inverter building block. These differences are indicated in the logic diagrams by a dot or a cross in the circle or square (Figure 2). Both the chassis tabs containing the card in question and the Printed Circuit Manual, Cordwood Modules contain electronic schematics of these special variations.

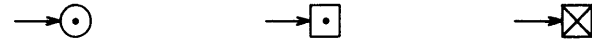


Figure 2. Special Inverters

Acceptable conventions for showing multiple inputs and outputs are given in Figure 3. Note that the output of inverter A is "0" only if inputs X, Y, and Z are all "1". The multiple outputs are identical.



Figure 3. Multiple Inputs/Outputs

Acceptable conventions for showing inverter networks are illustrated in Figure 4. As a general rule, circle inverters alternate with square inverters wherever possible. Because multiple outputs are identical, only one arrow is shown in cases where an inverter (A) serves as the single input to several succeeding inverters. In more complex inverter networks, multiple arrows are used (B to C and D; in this case because B is not the only input to C or D).

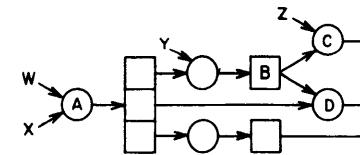


Figure 4. Inverter Networks

Test Points

A test point has no logic function, but is shown in the logic diagrams as a triangle (Figure 5). They are numbered from 1 to 6.

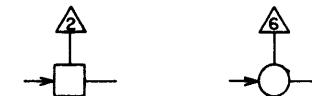


Figure 5. Test Point Symbols

KEY TO LOGIC SYMBOLS (Cont'd.)

Flip-Flops (FF)

The flip-flop (FF) is a storage device with two stable states--designated as Set and Clear--and is composed of two inverters (Figure 6). The flip-flop is said to be set when the set output (B) is a "1", and clear when it is a "0". Note that the input (A) must be "0" to set the flip-flop and (C) must be "0" to clear it.

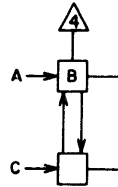


Figure 6. Flip-Flop Symbol

Logic signals are transmitted from one module to another by means of a line driver. Modules on the same chassis are connected with twisted pair lines, and those on separate chassis are connected by coaxial cable.

Twisted Pair Drivers

The twisted pair driver is represented by the standard square or circle. The output of the square or circle, however, is connected to a pin of the module in question and wired from there to a pin on another module (Figure 7). The ground wire of the pair is wired to the connector ground bus of each module. The pins are represented by small circles and are numbered from 1 to 28 (Pins 29 and 30 are ground and +6 volts, respectively, and generally are not shown in logic diagrams). The module location is shown above the card, and the module type is denoted in the upper right corner.

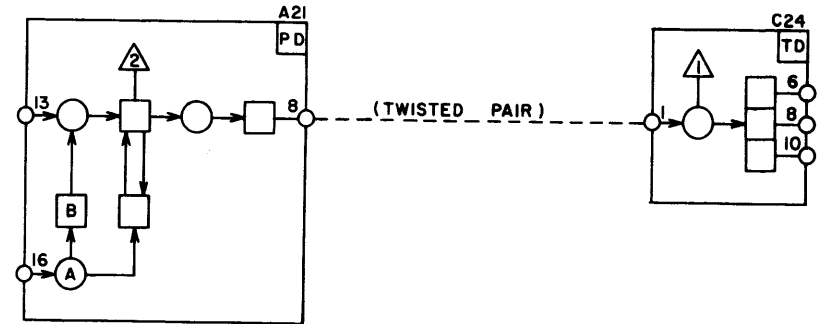


Figure 7. Twisted Pair Line Driver

Coaxial Cable Drivers

The coaxial cable driver is a 25 nsec pulse circuit, and is represented as shown in Figure 8. The pins used are represented by a small double circle.

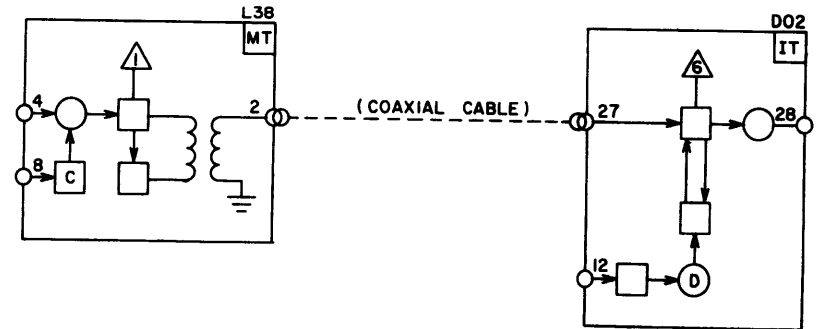


Figure 8. Coaxial Cable Driver

KEY TO LOGIC SYMBOLS (Cont'd)

3000 Series Interface Modules

These modules convert 3000 Series logic voltage levels to cordwood module logic levels. In Figure 9, the crossed wire representation shows that both wires in a twisted pair line are used. The transmitter/receiver modules are used for bidirectional signals. The others are for unidirectional signals. Electrical schematics appear in the chassis tabs.

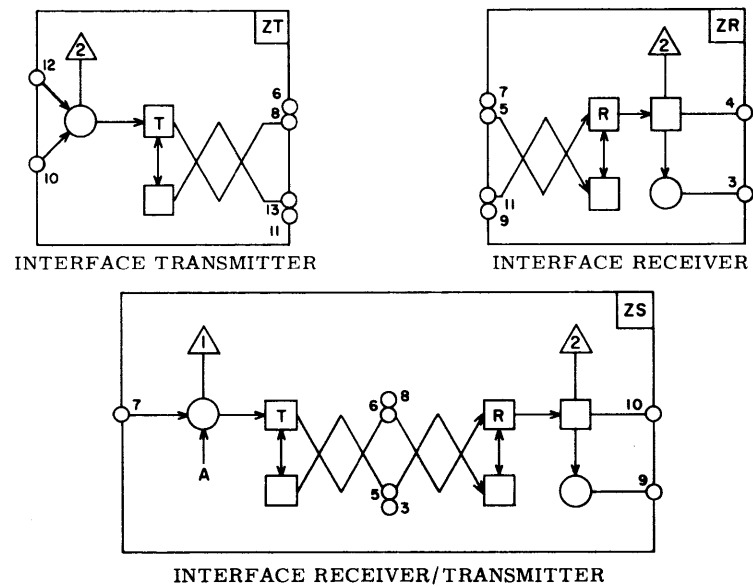


Figure 9. 3000 Series Interface Modules

MODULE LOCATION INDEX

| CHASSIS | PUB. NO. | SECTION |
|---------|-------------|-------------------|
| ROW A | MODULE TYPE | PAGE |
| 01 | PC | 14 |
| 02 | PC | 14 |
| 03 | QK | 14 |
| 04 | QK | 14 |
| 05 | PD | 14 |
| 06 | PD | 14 |
| 07 | TE | 15 |
| 08 | AB | 15 |
| 09 | AB | 9, 14, 15, 18, 19 |
| 10 | AA | 9 |
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| ROW B | MODULE TYPE | PAGE |
| 01 | PC | 14 |
| 02 | PC | 14 |
| 03 | QK | 14 |
| 04 | QK | 14 |
| 05 | PD | 14 |
| 06 | PD | 14 |
| 07 | TH | 9, 14, 15 |
| 08 | HQ | 14 |
| 09 | TH | 15 |
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| 02 | PC | 8 |
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| 04 | QK | 8 |
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| 06 | PJ | 7 |
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| 15 | PC | 18 |
| 16 | PC | 18 |
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| 03 | TB | 7, 14 |
| 04 | TB | 7, 8 |
| 05 | PJ | 7 |
| 06 | JR | 15 |
| 07 | AE | 7, 9 |
| 08 | AA | 7, 16 |
| 09 | XL | 7, 9, 10 |
| 10 | AA | 5, 9, 17 |
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| 12 | TB | 10, 16, 18, 19 |
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| 03 | HQ | 8, 10 |
| 04 | HC | 19 |
| 05 | HC | 19 |
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| 08 | AA | 12, 15 |
| 09 | TL | 6, 10, 15, 17, 18, 19 |
| 10 | TH | 1, 10, 12, 13 |
| 11 | HC | 11, 18 |
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| 13 | HC | 9, 12, 13 |
| 14 | IP | 16 |
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| 16 | PJ | 16 |
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| 03 | PD | 19 |
| 04 | TH | 7, 10 |
| 05 | AA | 10 |
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| 07 | TL | 7, 10, 11, 16, 17, 19 |
| 08 | QH | 12, 13, 17 |
| 09 | TH | 9, 10, 14 |
| 10 | AA | 10, 12, 13 |
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| 14 | TE | 16 |
| 15 | AB | 16 |
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| 06 | PD | 7, 9, 13 |
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| 08 | TB | 10, 11, 12 |
| 09 | TE | 11 |
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| 16 | PC | 16 |
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| 08 | PJ | 11 |
| 09 | PJ | 11 |
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| 11 | PO | 11 |
| 12 | PO | 11 |
| 13 | QH | 11, 12 |
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| 15 | KL | 4 |
| 16 | PJ | 4, 5 |
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| 07 | TE | 6 |
| 08 | TE | 6 |
| 09 | QH | 4, 5, 19 |
| 10 | QH | 4, 5, 17 |
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| 12 | TG | 4 |
| 13 | TG | 4 |
| 14 | TG | 4 |
| 15 | TG | 4 |
| 16 | TG | 4 |
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| 05 | SB | 13 |
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| 07 | TI | 1, 7, 9, 11, 17 |
| 08 | TH | 1, 6, 9 |
| 09 | HC | 6, 18 |
| 10 | TH | 1 |
| 11 | TD | |
| 12 | TD | 18 |
| 13 | HQ | 18 |
| 14 | TD | 18 |
| 15 | TD | 18 |
| 16 | HQ | 18 |
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| ROW K | MODULE TYPE | PAGE |
| 01 | ZR | 8 |
| 02 | ZR | 14 |
| 03 | ZR | 19 |
| 04 | AA | 1 |
| 05 | CX | 1 |
| 06 | AE | 1 |
| 07 | AE | 1 |
| 08 | TD | 1, 5, 6 |
| 09 | TB | 1, 11, 17 |
| 10 | TB | 1, 17 |
| 11 | QJ | 4 |
| 12 | QJ | 4 |
| 13 | QJ | 4 |
| 14 | QJ | 4 |
| 15 | QJ | 4 |
| 16 | QJ | 4 |
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| 03 | ZS | 11, 13 |
| 04 | ZS | 11, 13 |
| 05 | ZT | 7, 9, 10, 12 |
| 06 | ZT | 5 |
| 07 | QI | 1 |
| 08 | QI | 1 |
| 09 | QI | 1 |
| 10 | QI | 1 |
| 11 | QI | 1 |
| 12 | QI | 1 |
| 13 | QI | 1 |
| 14 | QI | 1 |
| 15 | QI | 1 |
| 16 | QI | 1 |
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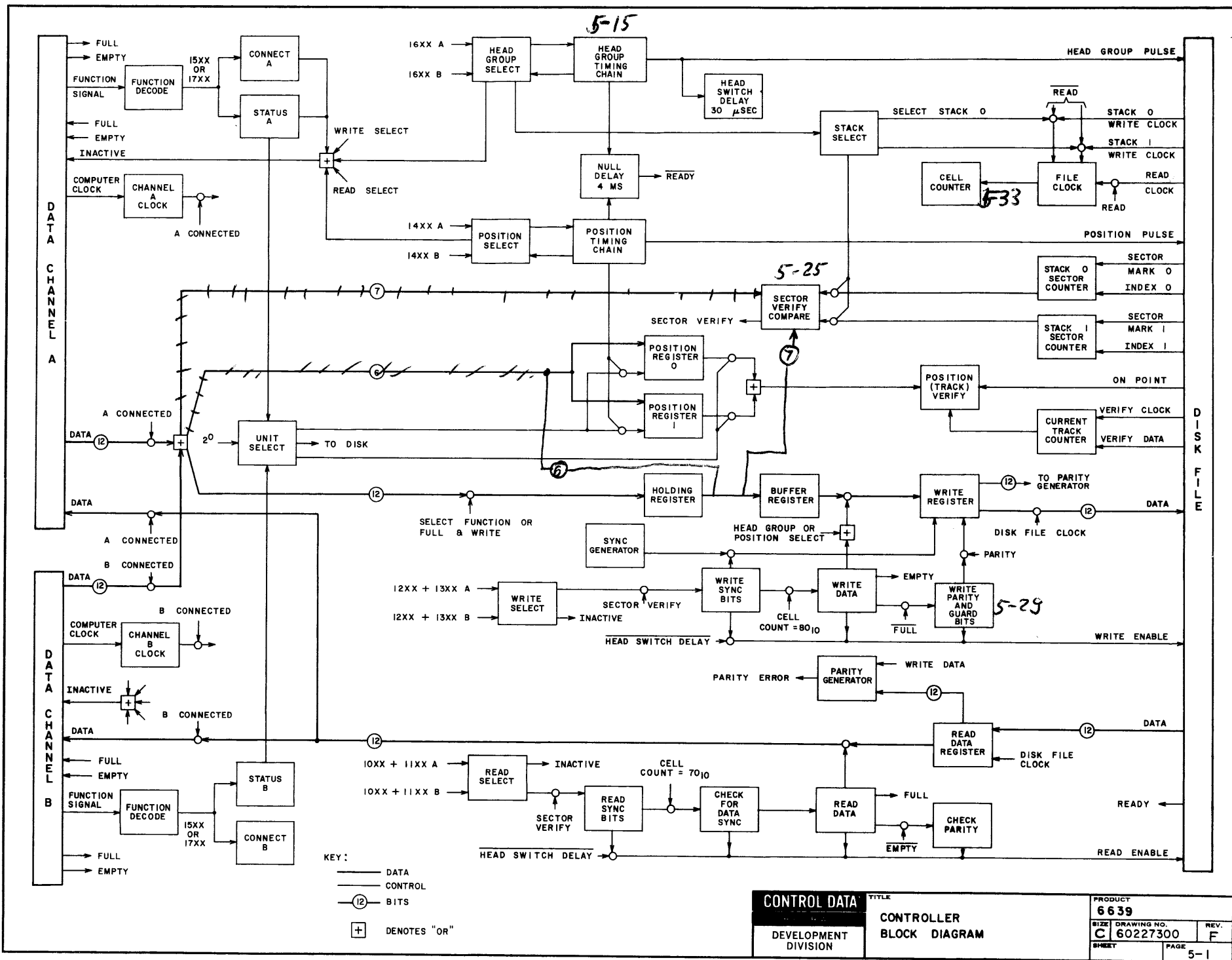
The controller buffers data in a 12-bit parallel format between the computer and disk file via the data channel. A 12-bit function code conditions the controller to connect to the disk file and designates a location on the disk from which data is to be transferred, thus initiating an I/O operation.

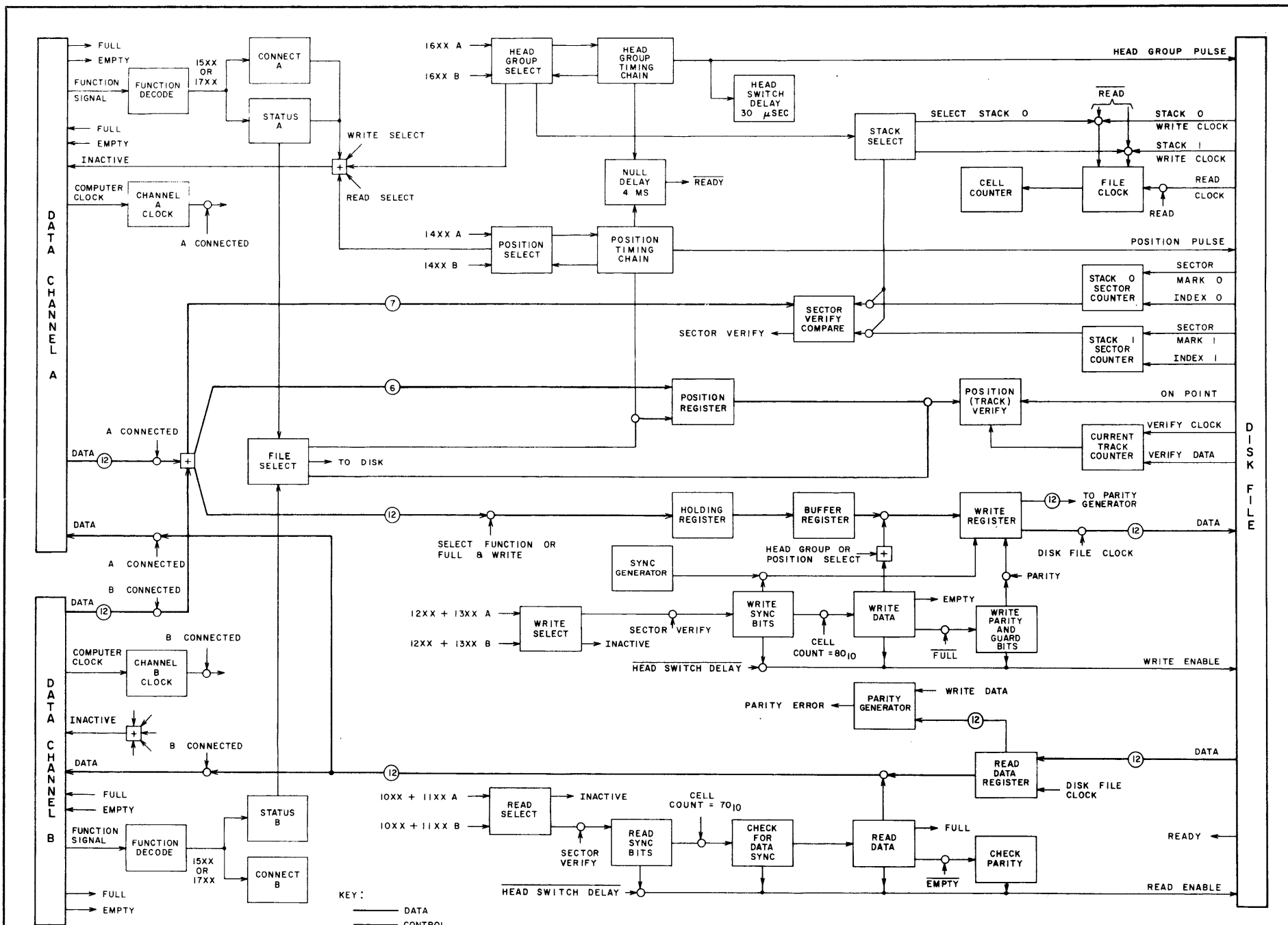
The data channel issues an output word to the controller. If the output word is accompanied by a function signal, the controller defines it as a function code. Otherwise, the controller recognizes it as a data word. When the controller accepts a function word, it returns an inactive signal to the data channel. The eight function codes are: connect and status, position select, head group select, read, write, select offset, clear file, and select file status. The connect code selects the disk file in which an I/O operation will be performed. A status response check can be performed to determine the state of conditions within the controller. The position select function causes the disk file access mechanism (positioner) to move to one of 32 positions. The position select function provides a position address which the

controller compares against a position code from the disk file to verify that the access mechanism is positioned correctly. The head group select function selects one of 32 head groups to correspond with the position selected.

If the function is a read, the active signal (sent with the read code) requests the controller to send data. The controller sends a data word and a full signal. The data channel then returns an empty signal, causing the controller to send the next word. Operations continue in this way until the end of the read buffer.

On a write operation, the full signal (sent with the write code) signals the controller that the data channel is ready to start sending data. The controller acknowledges the data word by returning an empty signal, causing the data channel to send the next data word. Operation continues in this way until the end of the write buffer.



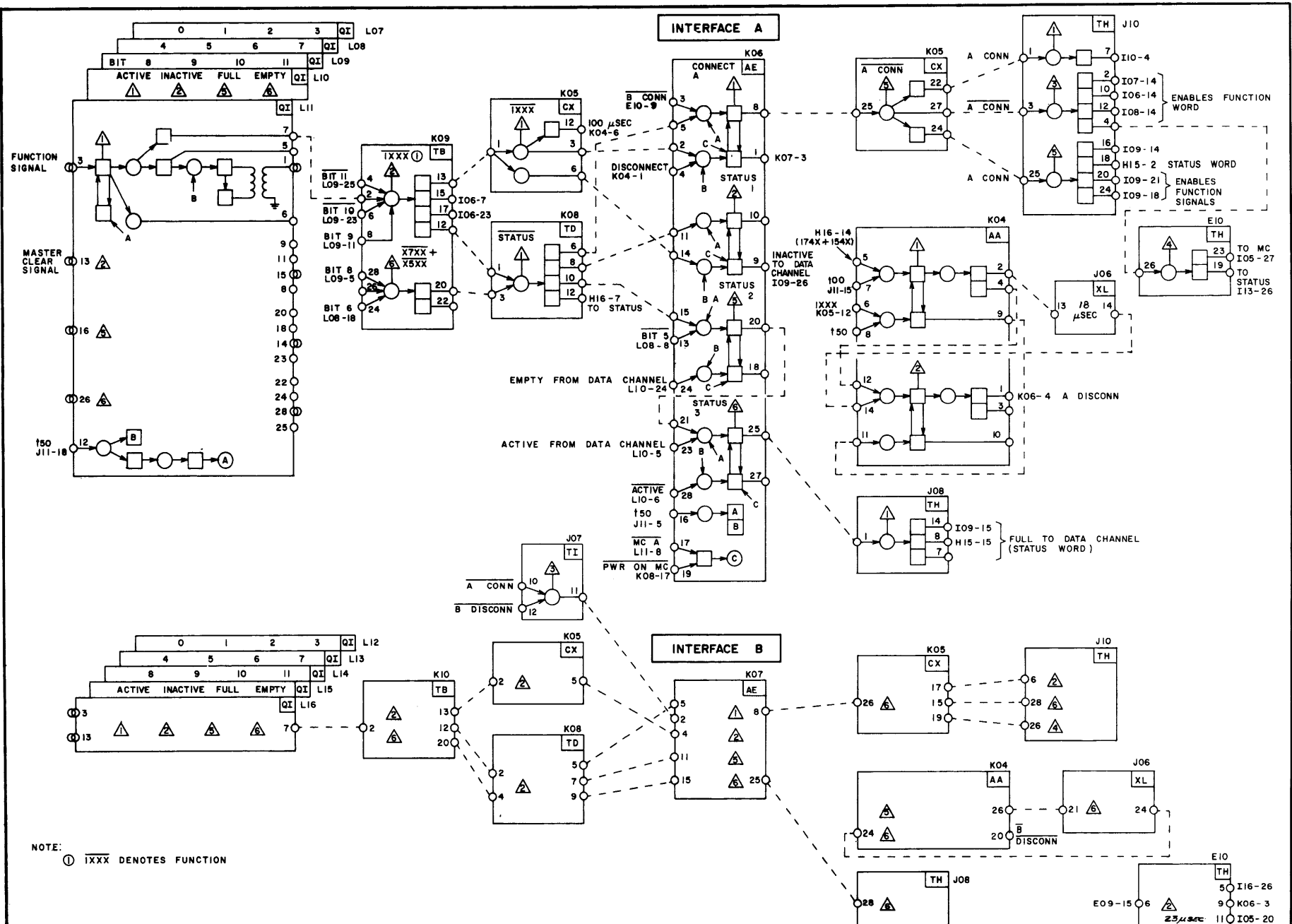


KEY:
 — DATA
 - - - CONTROL
 (12) BITS
 + DENOTES "OR"

This logic provides for receiving signals and data from the data channel for transmission to the disk file. Interfaces A and B connect the controller to data channels A and B, respectively. If the connect and status function word is received through interface A, it sets the connect A flip flop (FF) which provides various enables for transmitting the status word, data, and function signals through the controller during operation. The controller connects to data channel A if channel B is not connected and vice versa. If channels A and B attempt to connect simultaneously, the controller gives priority to channel A.

Receiving the connect and status function word and function signal causes the controller to set the status 1 FF. This causes the controller to return an inactive signal to the data channel, indicating acceptance of the function word. It also sets the status 2 FF which, together with the active signal from the data channel, sets the status 3 FF. Setting the status 3 FF enables the status word (and full signal) to the data channel.

A function code of 1740 or 1540 will disconnect the controller from the data channel approximately 100 microseconds after a function instruction is received.

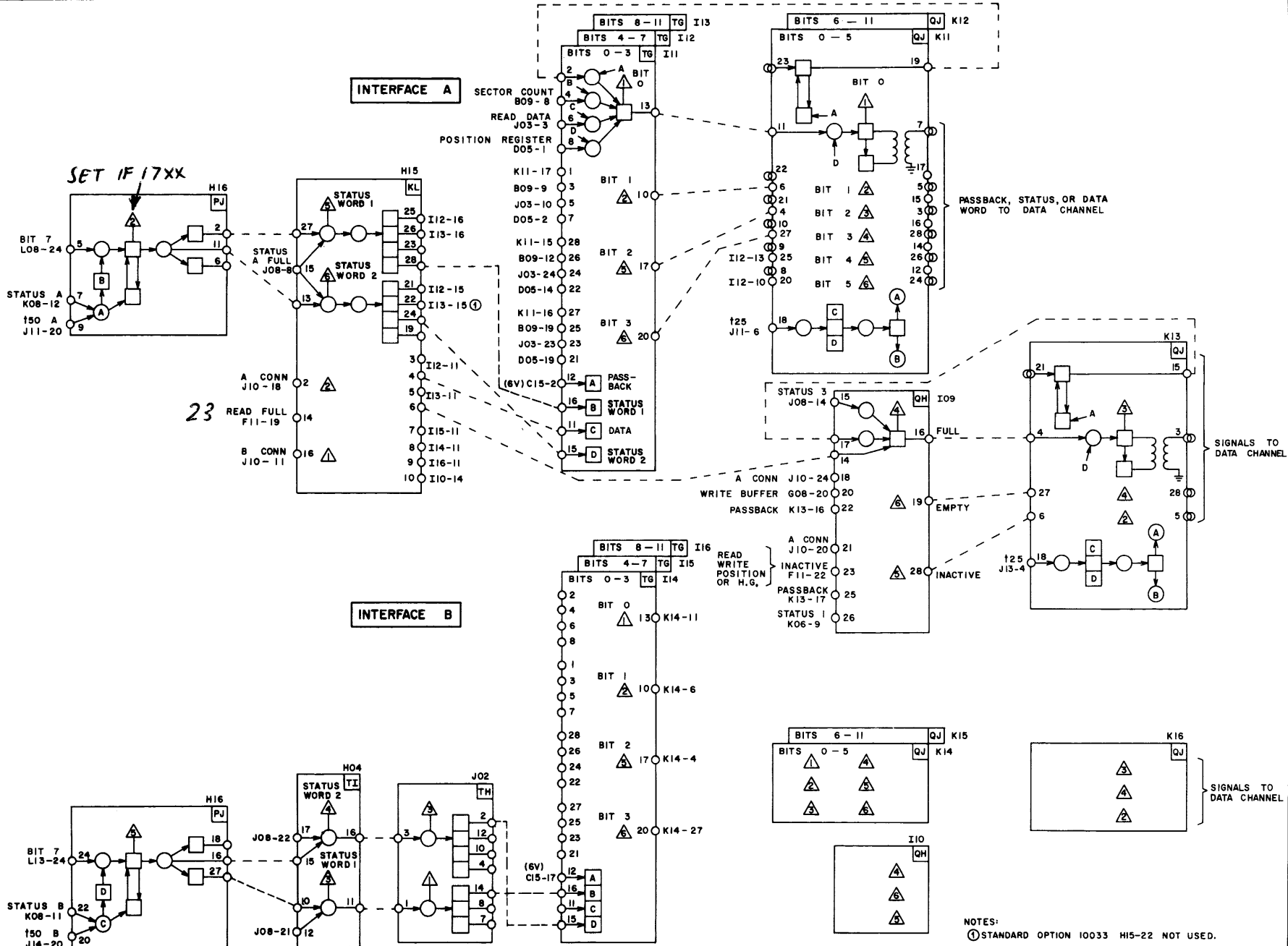


NOTE: ① IXXX DENOTES FUNCTION

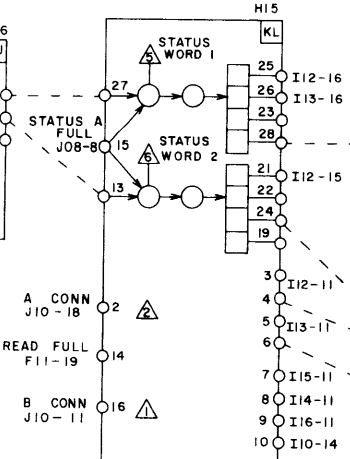
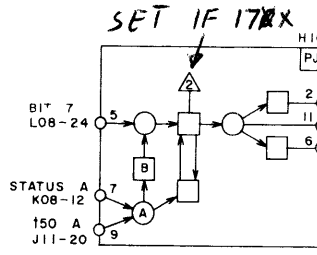
| | | |
|--------------------------------------|----------------------------------|-------------------------------|
| CONTROL DATA DEVELOPMENT DIVISION | TITLE | 6639/ST OPT 10037 |
| | CONTROLLER CONNECT AND STATUS | SIZE DRAWING NO C 60227300 |
| | | REV. G |
| | SHEET | PAGE 5-3 |

NOTE

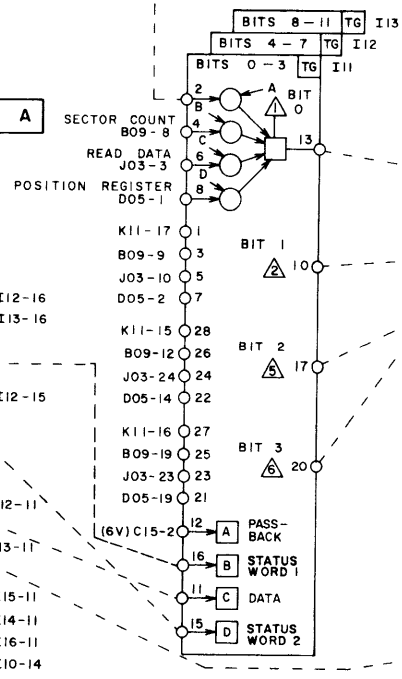
Pages 5-4, 5-5, 5-6, 5-7, and 5-8
are not included intentionally.



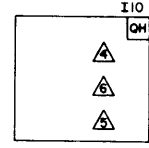
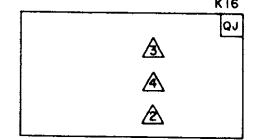
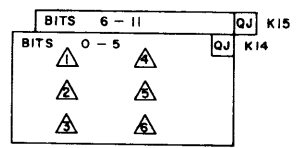
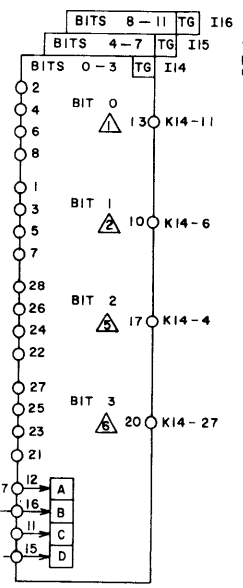
| | | | | | |
|----------------------|-------------|---|-------|-------------------|--|
| CONTROL DATA | | TITLE | | PRODUCT | |
| DEVELOPMENT DIVISION | | CONTROLLER STATUS, GATES OUT TO CHANNEL | | 6639/ST OPT 10033 | |
| SIZE | DRAWING NO. | REV. | | | |
| C | 60227300 | H | | | |
| SHEET | PAGE | | 5 - 9 | | |



INTERFACE A

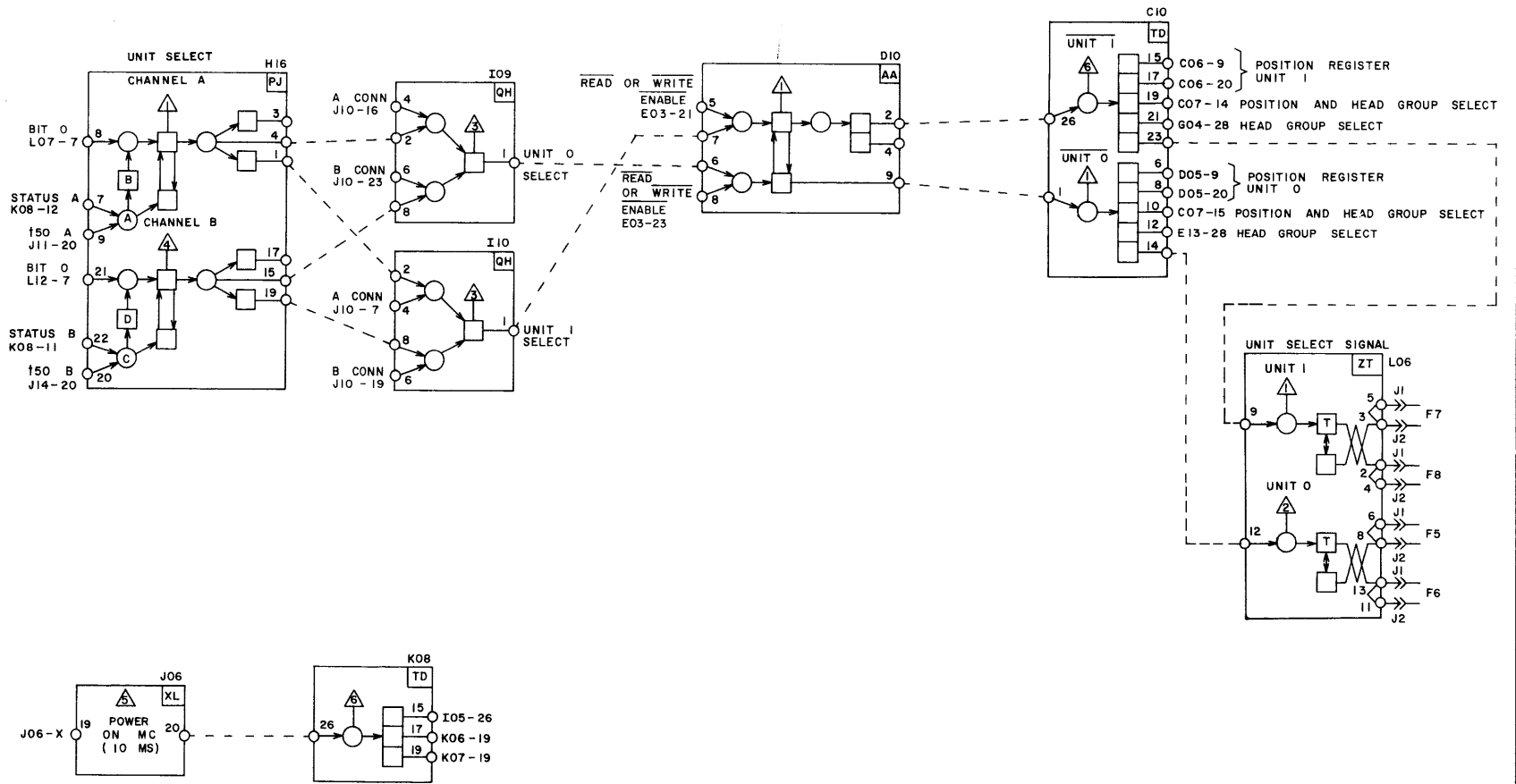


INTERFACE B

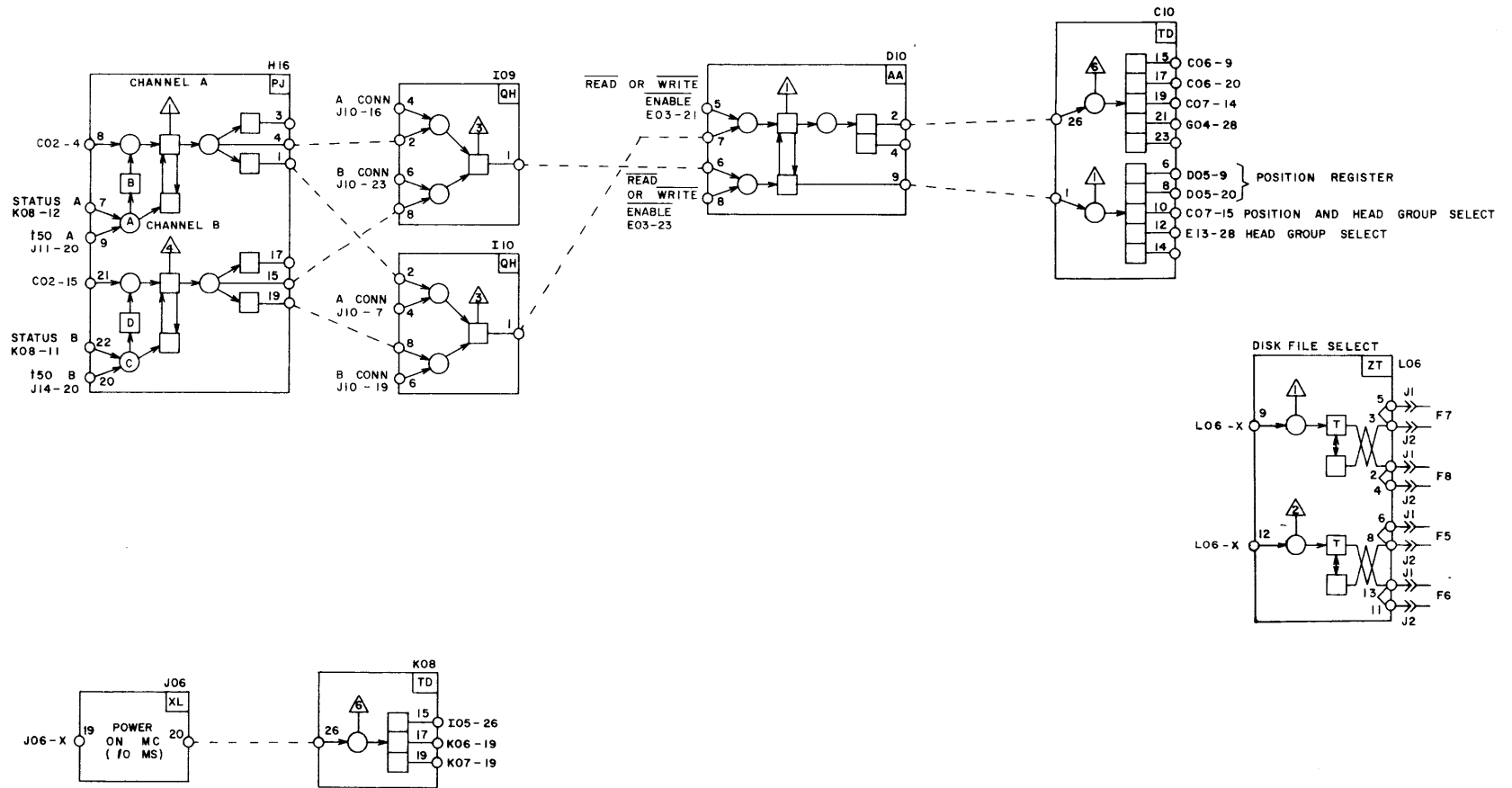


| | | | |
|---------------------|----------------------|---|--------------|
| CONTROL DATA | TITLE | PRODUCT STANDARD | |
| | DEVELOPMENT DIVISION | CONTROLLER STATUS, GATES OUT TO CHANNEL | OPTION 10037 |
| | | SIZE DRAWING NO | |
| | | C 60227300 | REV F |
| | | SHEET 4A | PAGE 5-9A |

"0" = UNIT 0 SELECT
 "1" = UNIT 1 SELECT

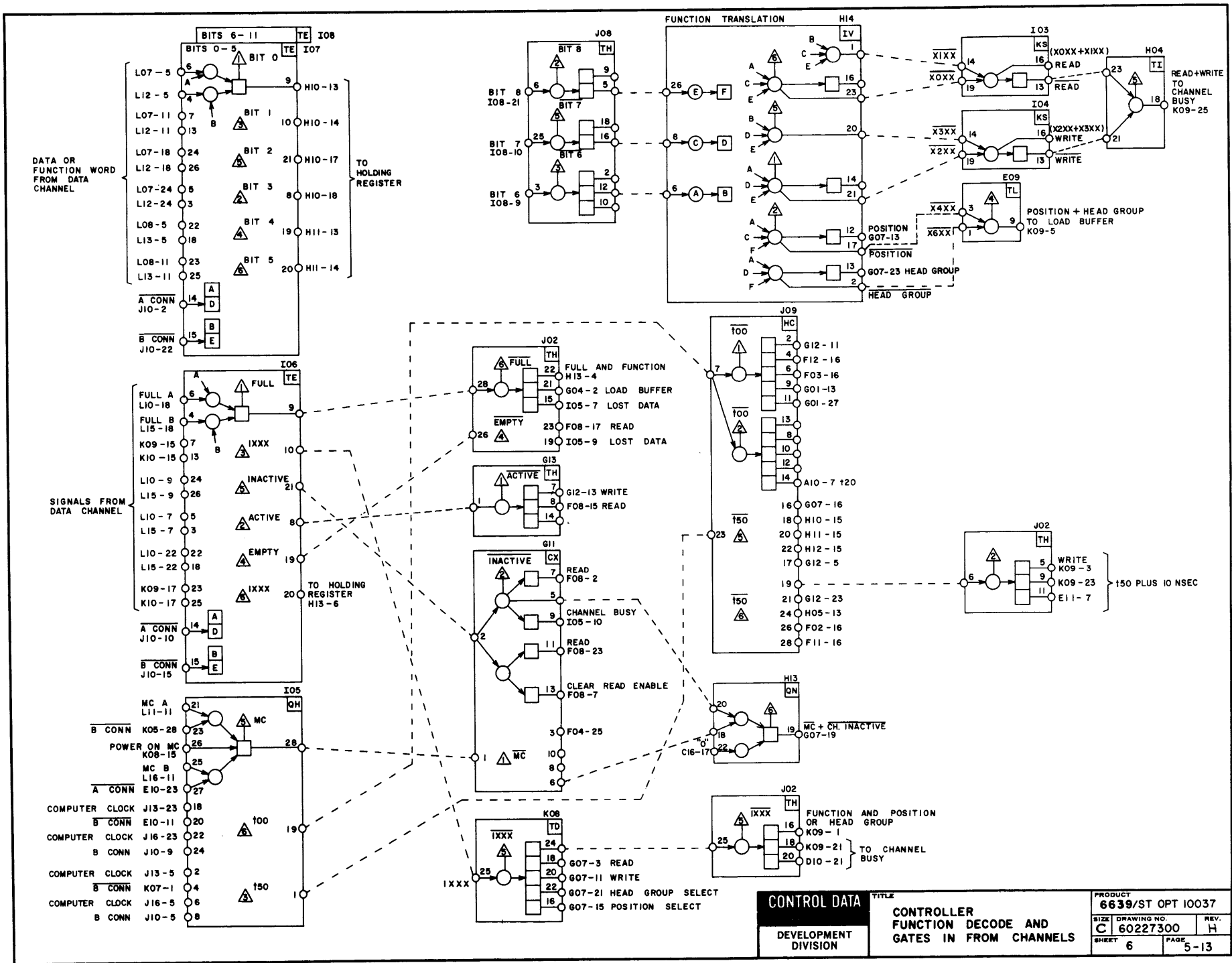


| | | | |
|----------------------|-------------|------------------------|---------|
| CONTROL DATA | | TITLE | PRODUCT |
| DEVELOPMENT DIVISION | | CONTROLLER UNIT SELECT | 6639 |
| SIZE | DRAWING NO. | REV. | |
| C | 60227300 | F | |
| SHEET | PAGE | PAGE | |
| 5 | 5 | 11 | |



| | | | |
|---------------------|----------------------|------------------|------------------|
| CONTROL DATA | DEVELOPMENT DIVISION | TITLE | PRODUCT STANDARD |
| | | CONTROLLER | OPTION 10037 |
| | | DISK FILE SELECT | REV. F |
| SIZE | DRAWING NO. | SHEET | PAGE |
| C | 60227300 | 5A | 5-11A |

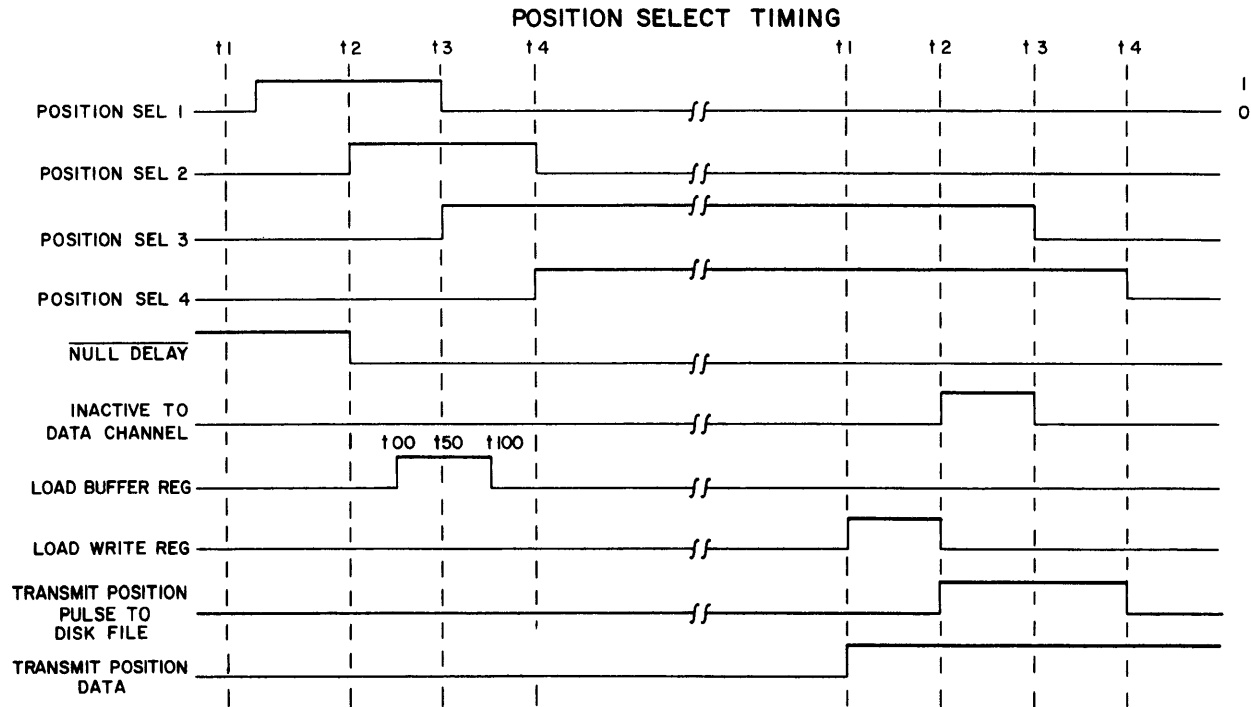
Function words from the data channel are transmitted to the holding register and are also translated to initiate a read, write, position select, or head group select. Either a read or write causes a channel busy condition prior to an I/O operation. A position select or head group select function causes the position address or head group number to be gated to the buffer register for register to the disk file. Inactive, active, full, and empty signals sent by the data channel are distributed here to enable various controller operations. The function signal is fanned out to the position select, head group select, read, and write logic to enable the function being selected.

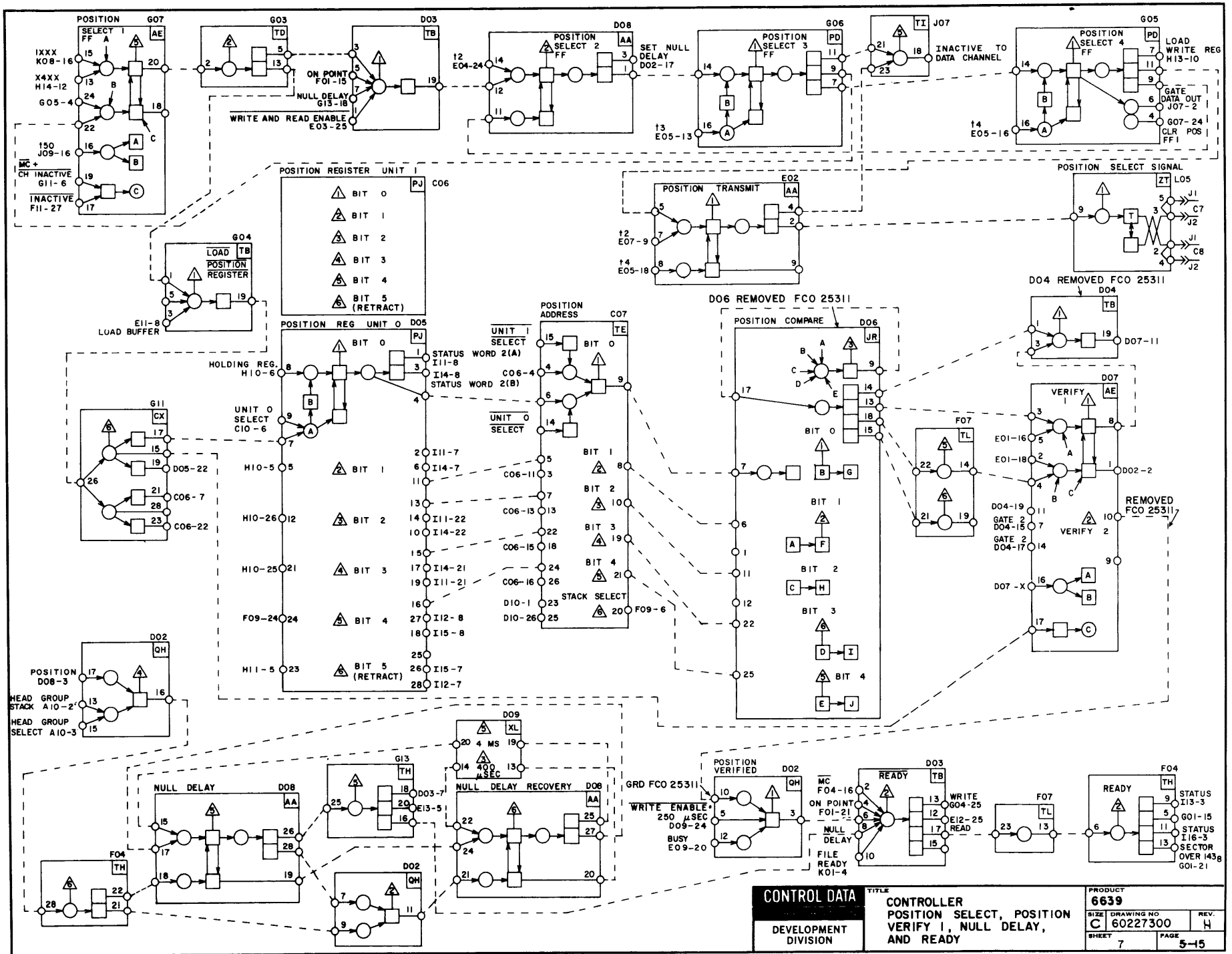


| | | | | | |
|-----------------------------|--|--|--------------------|--------------------------|--|
| CONTROL DATA | | TITLE | | PRODUCT | |
| | | CONTROLLER FUNCTION DECODE AND GATES IN FROM CHANNELS | | 6639/ST OPT 10037 | |
| DEVELOPMENT DIVISION | | SIZE | DRAWING NO. | REV. | |
| | | C | 60227300 | H | |
| | | SHEET | PAGE | | |
| | | 6 | 5-13 | | |

The position select function word activates the position select logic and provides a position address for selecting one of 32 positions in the disk file. An inactive signal is sent to the data channel which indicates acceptance of the position select function word by the controller. The address is fed through the holding register (page 5-23), buffer register, write register and sent to the disk file. The address is also gated to the position register for comparison against a position code from the disk file. Two successive valid comparisons are necessary to set the verify 1 and verify 2 FF's, respectively, and to verify the new position.

Since it takes a comparatively long time (4 milliseconds) for the positioner mechanism to move from the old on point, a null delay circuit is provided to force a not ready condition for at least 4 milliseconds after the position is issued. This provides time for the positioner to become off point with respect to the original position. Otherwise, the controller could possibly output a ready based on the previous on point, causing an I/O operation to begin before the positioning mechanism had begun to move.

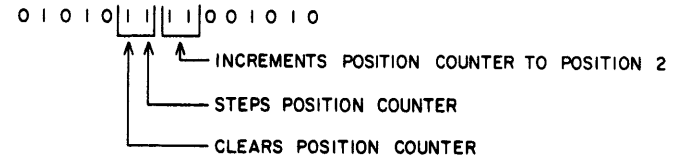




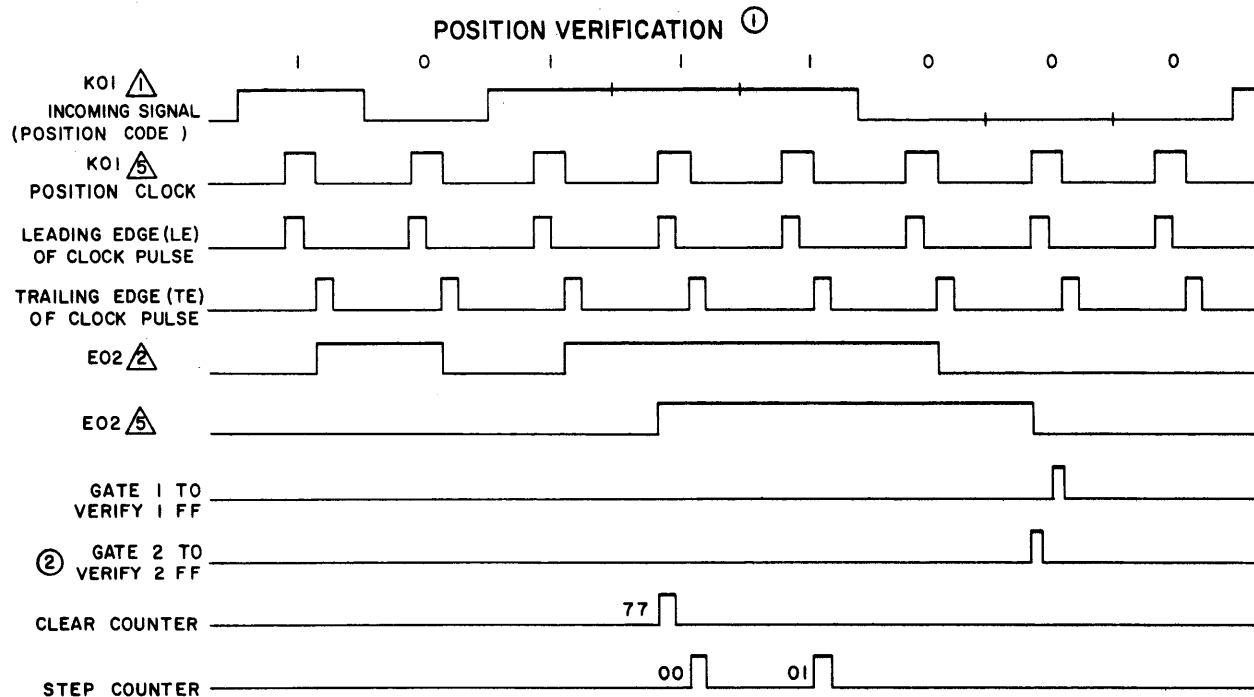
Position codes which have been prerecorded on separate tracks for each of the 32 positions in a disk file unit are translated to determine that the read/write heads are positioned properly on the disks. Each track contains one position code which is repeated every 64 bits around the track. The position codes are received in non-return to zero (NRZ) data. Examples of the first five position codes are as follows:

| Position | Data Pattern |
|----------|---------------------------------|
| 0 | 0 1 0 1 0 1 1 1 0 0 1 0 1 0 1 0 |
| 1 | 0 1 0 1 0 1 1 1 0 0 0 1 0 1 0 |
| 2 | 0 1 0 1 0 1 1 1 1 0 0 1 0 1 0 |
| 3 | 0 1 0 1 0 1 1 1 1 0 0 0 1 0 |
| 4 | 0 1 0 1 0 1 1 1 1 1 1 0 0 1 0 |

Position-clock pulses derived from the position code tracks are used to gate position code data to the position counter. The position-clock pulses provide leading edge (LE) and trailing edge (TE) pulses which gate the position code data through the logic, causing the position counter to be stopped if the proper bit combination of position code data is present. An example of the bit combination for position 2 is as follows.

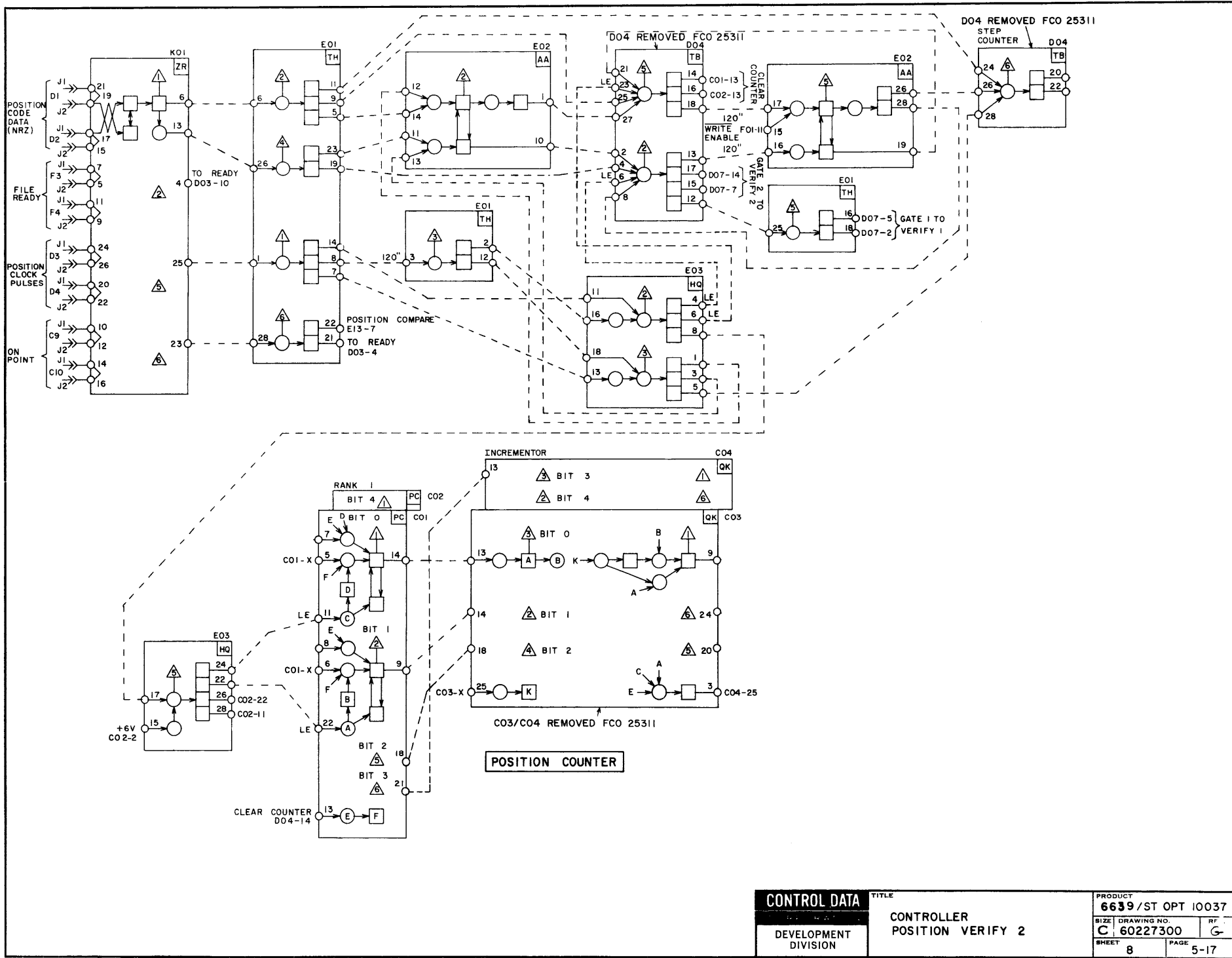


To increment the position counter, two or more 1 bits in succession are required. In addition to the position code data and the position-clock pulses, file ready and on point signals from the disk file are gated in for transfer to other logic circuits.



NOTES:

- ① POSITION VERIFICATION ON TRACK 1 IS SHOWN. THREE '1' BITS IN SUCCESSION SIGNIFY TRACK 1.
- ② AN ON-POINT AND TWO VERIFIES ARE NEEDED TO SET THE VERIFY 2 FF.



| | | | |
|----------------------|-------------|------------------------------|---------------------|
| CONTROL DATA | | TITLE | PRODUCT |
| DEVELOPMENT DIVISION | | CONTROLLER POSITION VERIFY 2 | 6639 / ST OPT 10037 |
| SIZE | DRAWING NO. | RF | |
| C | 60227300 | G | |
| SHEET | PAGE | | |
| 8 | 5-17 | | |

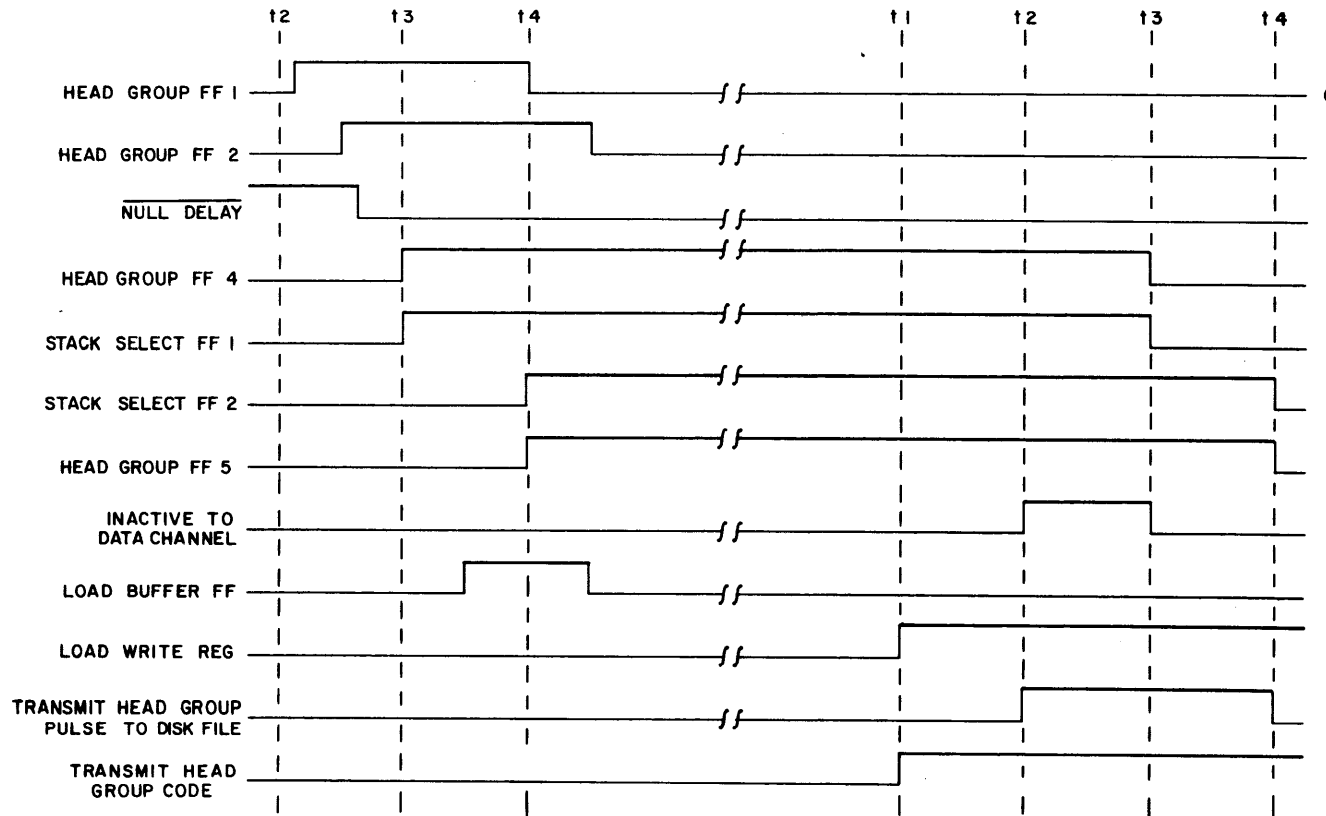
The head group select function word activates the head group select logic and loads the 5-bit head group address in the holding register. Activating the logic provides a head group pulse which provides for transmitting a head group inactive signal to the data channel. This indicates acceptance of the function word, enables a head group select signal to the disk file, and activates the head switch delay circuit to provide time for the read/write heads to complete switching before a read or write operation. At completion of the delay, read or write enables are provided.

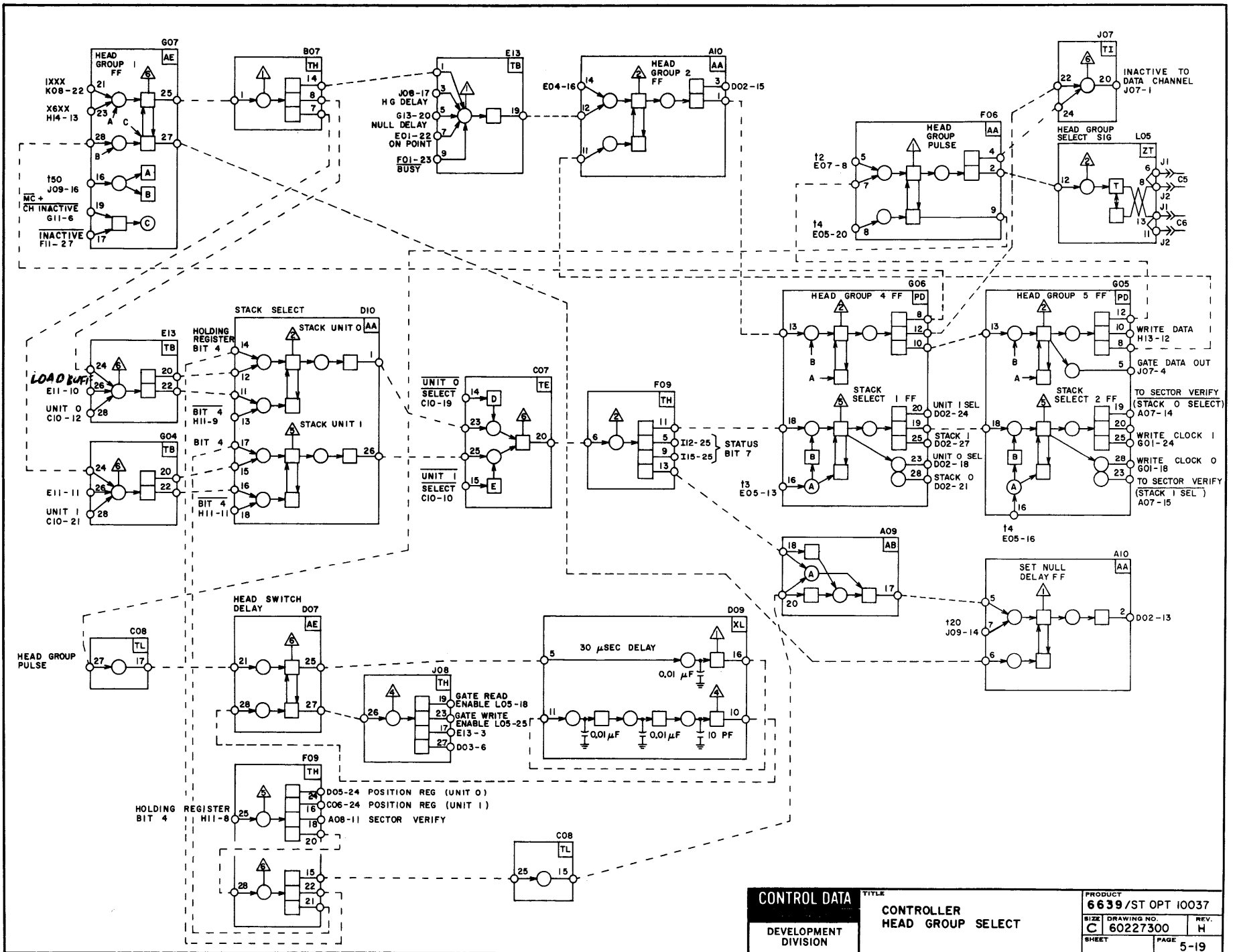
Bit 4 of the holding register determines if a head group is to be selected in stack 0 or 1. If bit 4 is a 0, the head group is selected in stack 0 (bits 0-15). If bit 4 is a 1, the head group is selected in stack 1 (bits 16-31). When the head group selection

is made in the designated stack, this information is available for sampling as the next status word, and enables are provided for the write clock and sector verify logic.

If the head groups are to be selected (switched) during an I/O operation, a head group select function can be issued to switch heads between sectors. However, if the switching involves changing to heads in the other stack, the null delay circuit (page 5-15) provides a 4-millisecond delay to allow the positioner to become off point and start to reposition on the other stack. This delay occurs each time that the heads are switched between stacks.

HEAD GROUP SELECT TIMING

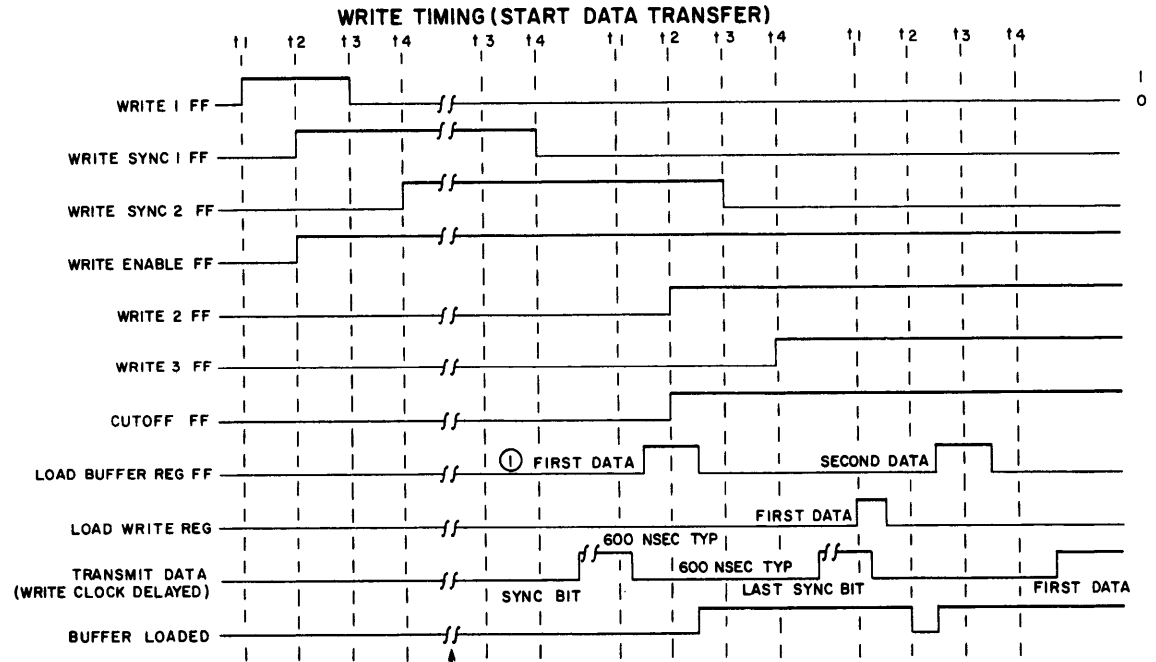




| | | | |
|---------------------|-----------------------------|-------------------------------------|--------------------------|
| CONTROL DATA | TITLE | PRODUCT | |
| | DEVELOPMENT DIVISION | CONTROLLER HEAD GROUP SELECT | 6639/ST OPT 10037 |
| | SIZE | DRAWING NO. | |
| | C | 60227300 | REV. |
| | SHEET | PAGE | 5-19 |

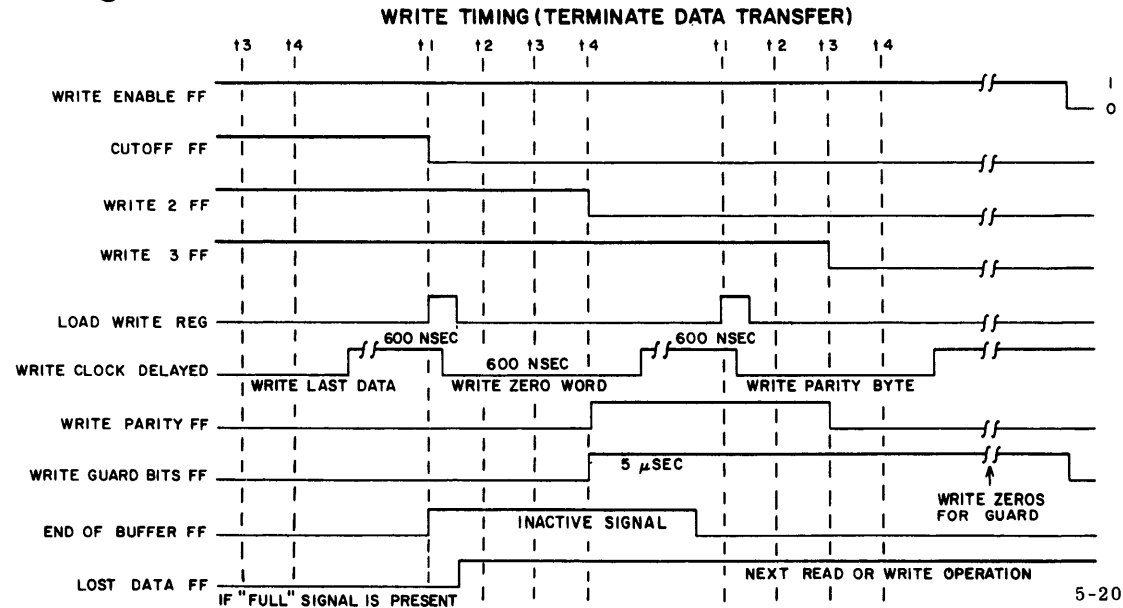
The write function word activates the write logic and loads the 7 bits of the function word containing the sector address to the holding register. Further operations in the write control logic depend upon completion of sector verify and the presence of ready. Sector verify ensures that the write operation will begin at the sector designated by the write function word. A ready indicates that the disk file positioner is on point, that the position at which the write operation is to take place has been verified, and that the disk file is ready for operation.

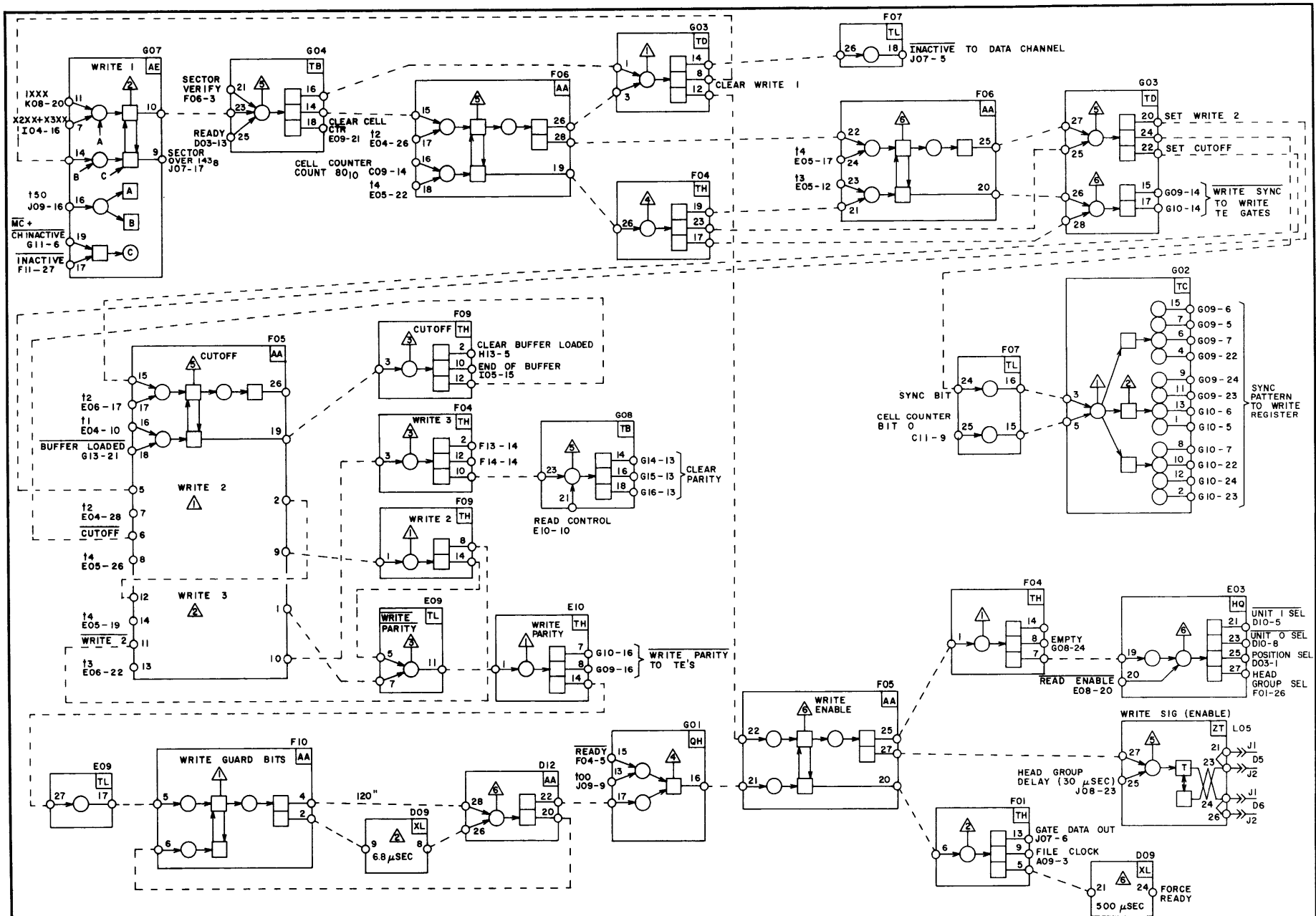
When the sector is verified and the system is ready, the write enable gates the write signal to the disk file. The cell counter begins counting preamble bits, starting at the sector mark determined by sector verify. An inactive signal is returned to the data channel to indicate acceptance of the write function word. The 80 preamble bits are written in an alternating 1's and 0's pattern. Two 1 bits in succession signify the beginning of data. The second 1 bit is the sync bit. The data buffer (record) may cover from 1 to 10 sectors. At the end of data is the postamble, consisting of at least 28 bits, including the parity and guard bits. Only the parity and guard bits (5 bits) are written on the record. At the end of the record, the buffer register is not loaded, clearing the cutoff FF. This causes the Write 2 FF to clear, resulting in the writing of the guard bit 0's. The write 3 FF clears, enabling the parity byte generated from the last record to be written as well as the remainder of the postamble.



WAIT FOR A CELL COUNT OF 80₁₀

NOTES: ① OCCURS WHEN FULL SIGNAL COMES IN ANY TIME DURING SYNC WRITING.





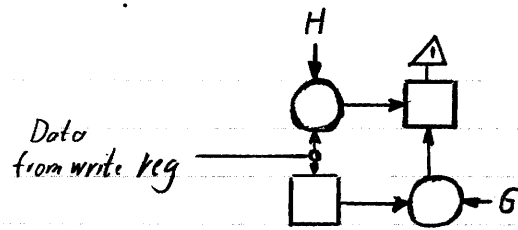
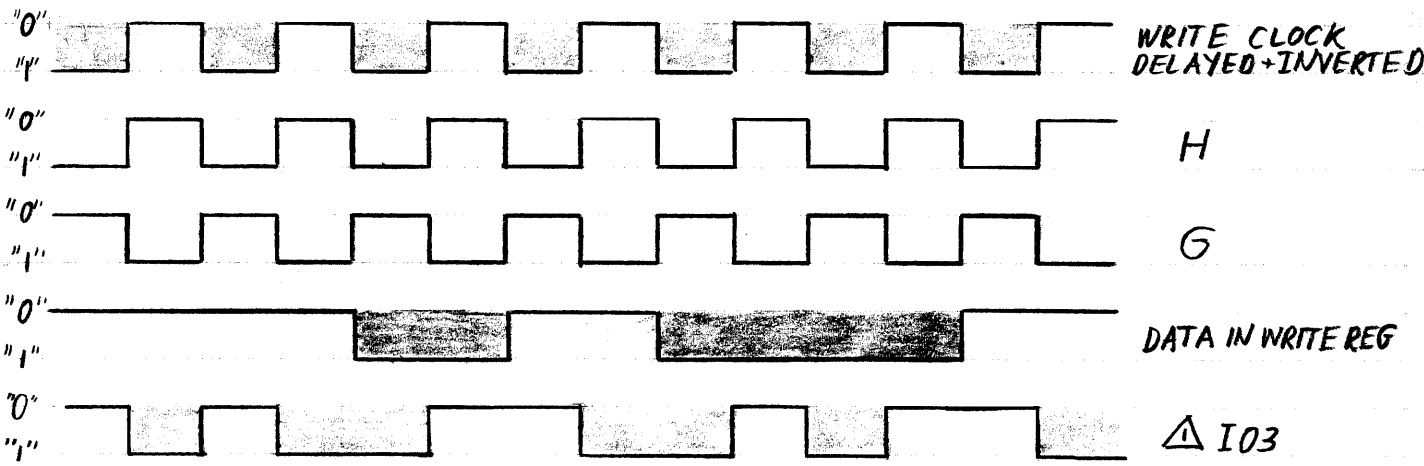
| | | | | |
|-----------------------------|----------------------------------|--------------------------|--------------------|-------------|
| CONTROL DATA | 6639/ST OPT 10037 | PRODUCT | | |
| | | 6639/ST OPT 10037 | | |
| | | SIZE | DRAWING NO. | REV. |
| | | C | 60227300 | H |
| DEVELOPMENT DIVISION | CONTROLLER WRITE CONTROLS | | SHEET | |
| | | | 10 | |
| | | | PAGE | |
| | | | 5-21 | |

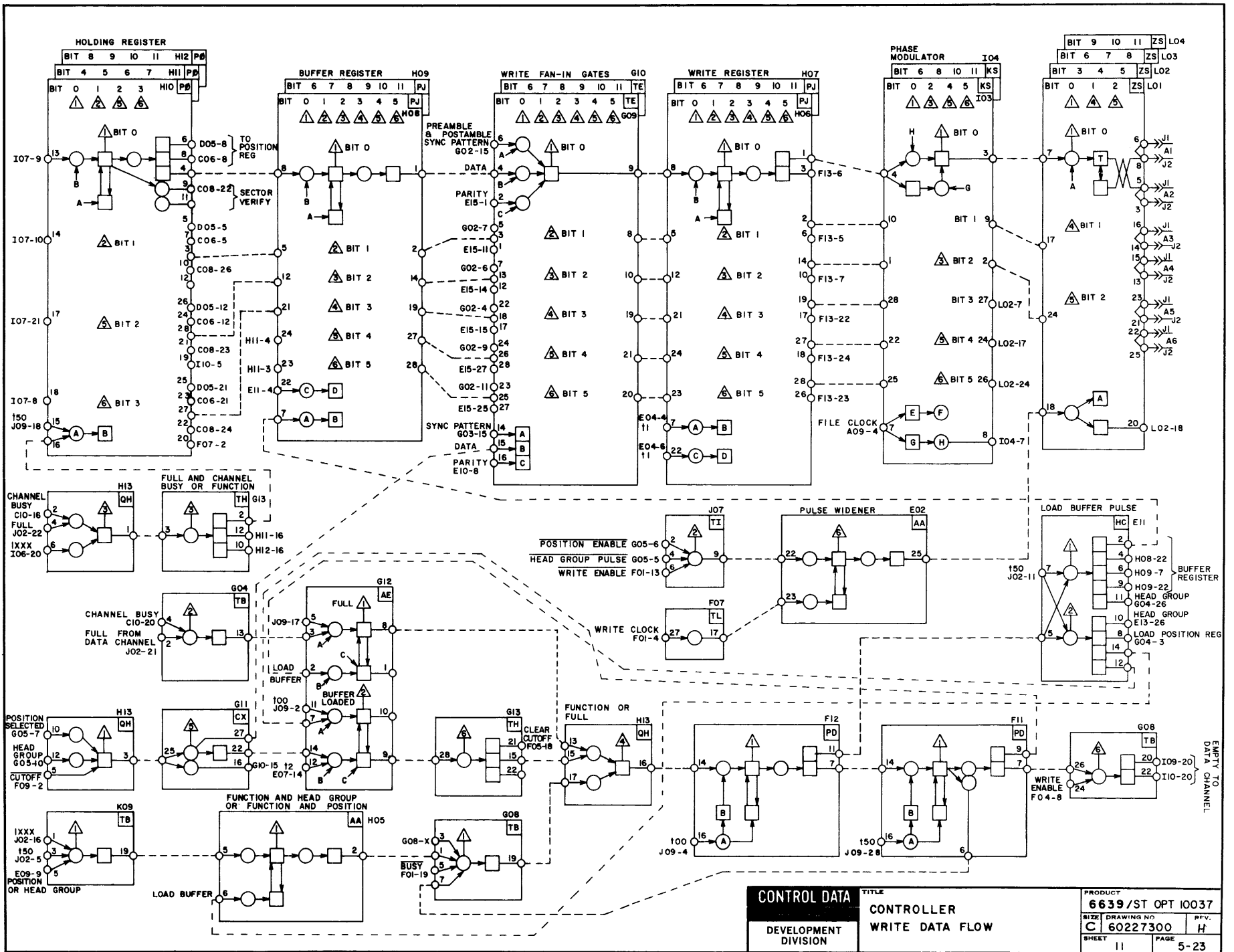
The holding, buffer, and write register, and write fan-in gates provide a path for the transmission of data out to the disk file. All function or data words are transmitted to the holding register. During a write, a full signal is needed from the data channel to enable data to the buffer register.

The write fan-in gates allow gating of the sync pattern (preamble) bits, data, or parity byte out to the disk file.

As data is shifted in parallel to the disk file, an empty signal is generated and sent to the data channel. The data channel returns another data word with a full pulse and the process is repeated. Operation continues in this manner until the end of the buffer (record).

PHASE MODULATOR





CONTROL DATA
DEVELOPMENT DIVISION

TITLE
CONTROLLER
WRITE DATA FLOW

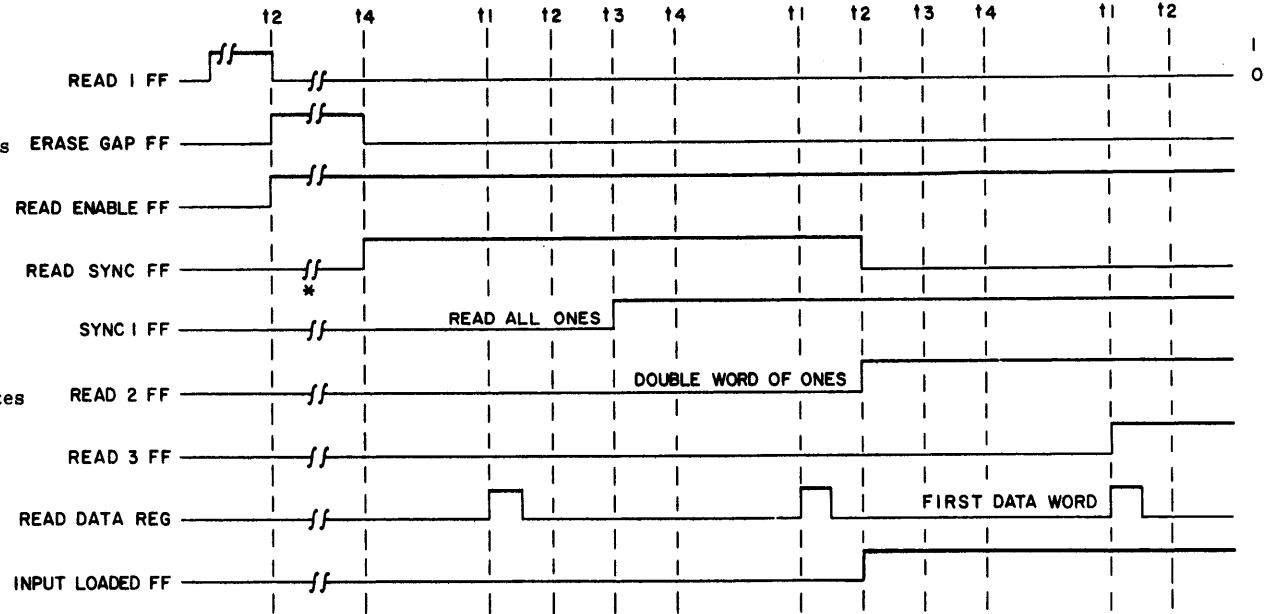
| | |
|-------------------------------------|--------------------------------|
| PRODUCT 6639/ST OPT 10037 | |
| SIZE C | DRAWING NO. 60227300 |
| SHEET 11 | PAGE 5-23 |
| REV. H | |

The function code portion of the read function word activates the read logic. The address portion of the read function word contains the sector address.

Sector verify and ready signals must be present as for a write function. The sector verify pulse indicates that the sector mark has been determined at which reading will begin. An inactive signal is returned to the data channel to denote the acceptance of the function word. When the cell counter reaches a count of 106_8 (70_{10}), the controller begins looking at the preamble. When 2 bytes of sevens are read in succession (page 5-27), the read 2 FF sets. Setting the read 2 and read 3 FF's denotes the beginning of data transfer. It enables the data being read off the disk to be gated through the controller registers to the data channel.

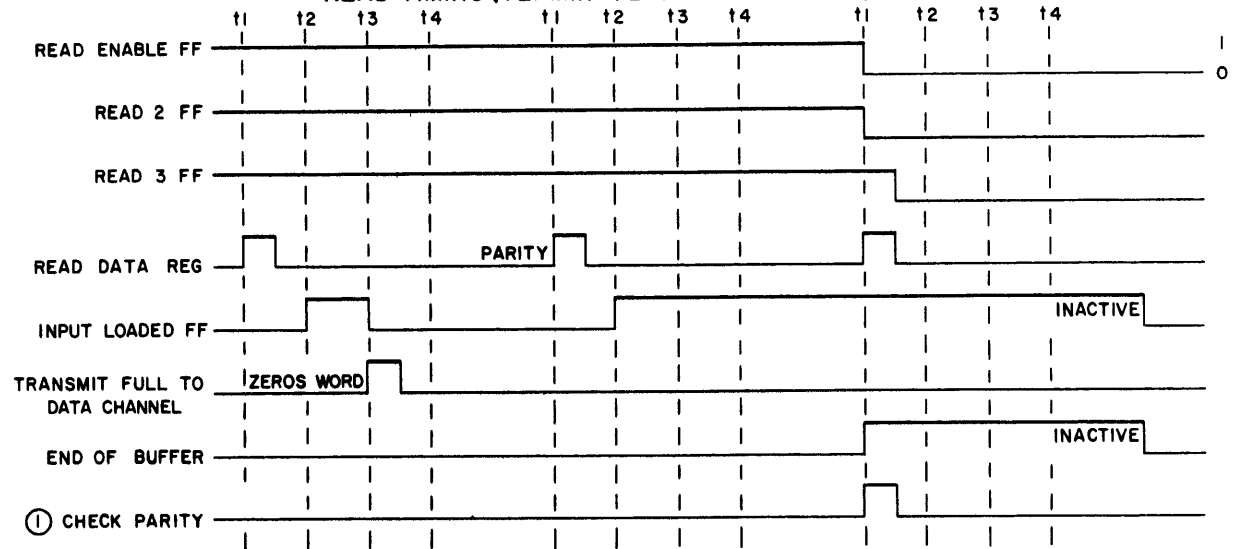
If 2 bytes of all seven are not read in succession by the time the cell counter reaches a count of 160_8 (112_{10}), the read 2 FF is forced to set in order to prevent a hang-up, and the parity error FF is set automatically.

READ TIMING (START DATA TRANSFER)



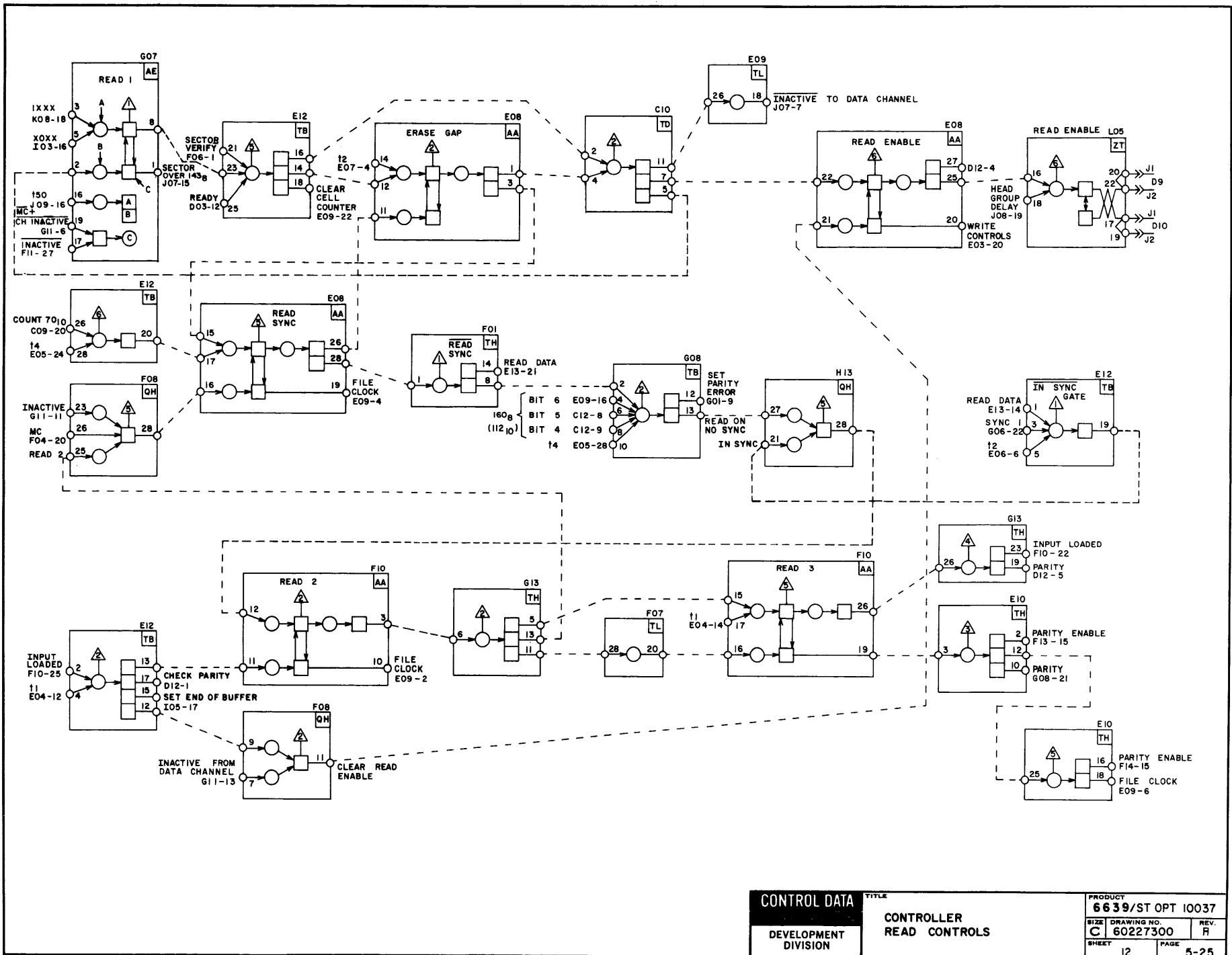
* WAIT FOR A CELL COUNT OF 70_{10}

READ TIMING (TERMINATE DATA TRANSFER)



NOTES:

① SEE PAGE 1-29, GOI-TP2



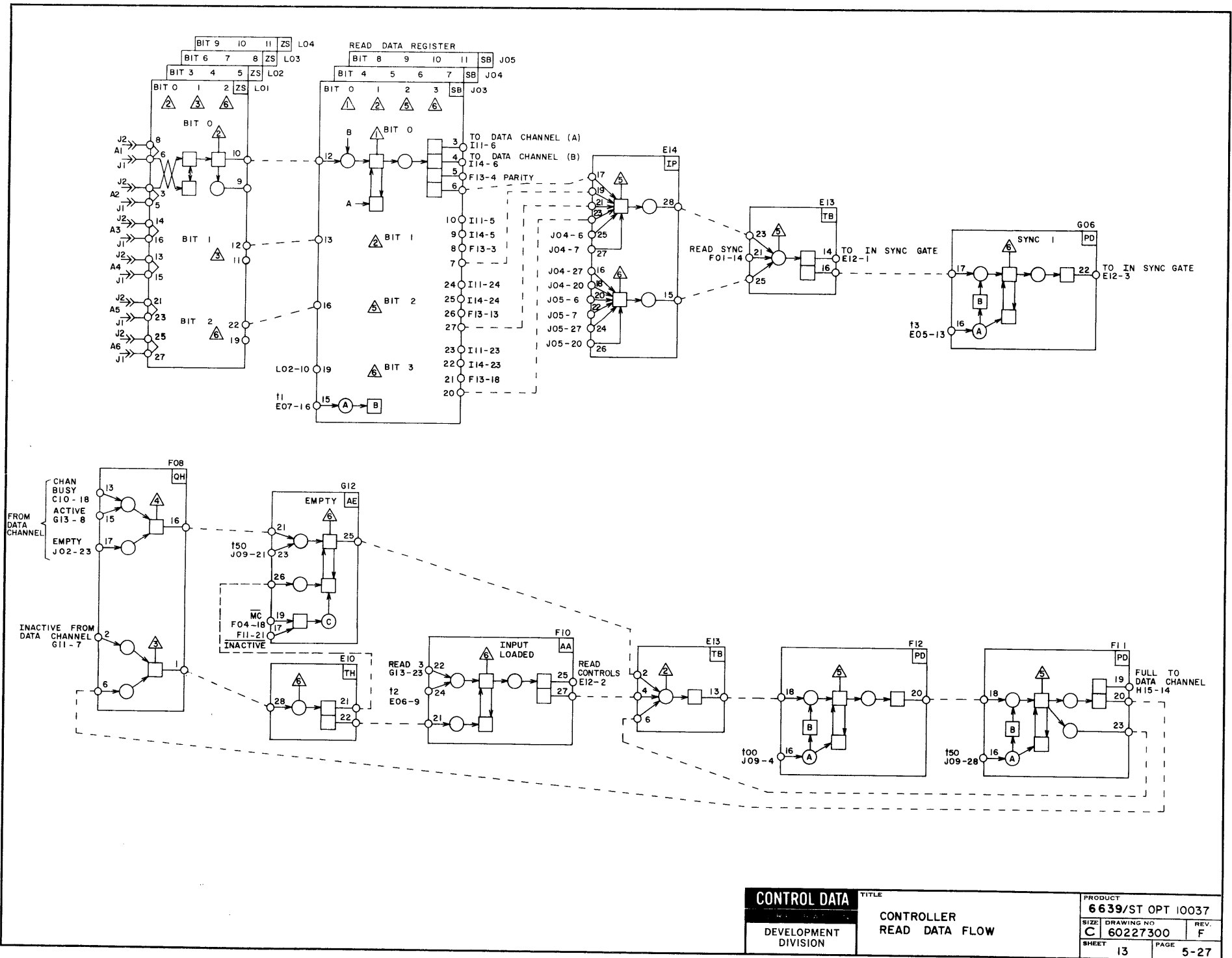
CONTROL DATA
DEVELOPMENT DIVISION

TITLE
CONTROLLER
READ CONTROLS

| | |
|-------------------------------------|--------------------------------|
| PRODUCT 6639/ST OPT 10037 | |
| SIZE C | DRAWING NO. 60227300 |
| SHEET 12 | REV. R |
| PAGE 5-25 | |

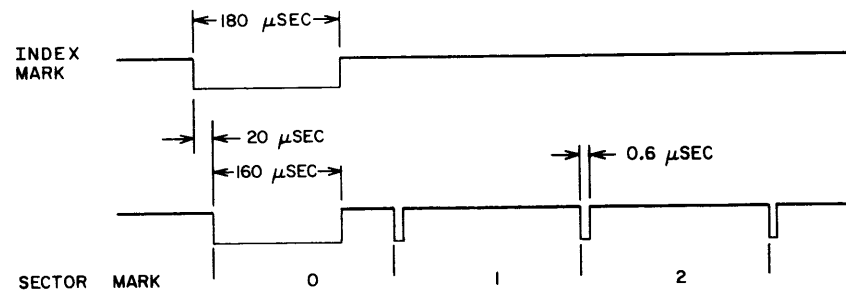
Data being read from the disk file is transmitted through the read data register to the data channel. During reading of the preamble, alternating bytes of 1's (7777_8) and 0's (0000) are read off the disk. Each time T1 comes up, a byte is gated into the read data register. A byte of 1's sets the sync I FF at T3. A byte of 0's clears the sync I FF. Since the preamble contains alternating 1's and 0's bytes, the sync I FF is alternately set and cleared until the beginning of data. Two consecutive bytes of 1's denote the beginning of data. The sync I FF is set, and the read register is all sevens, allowing the in sync gate (page 5-25) to output a 1 at the next T2, thereby setting the read 2 FF (page 5-25).

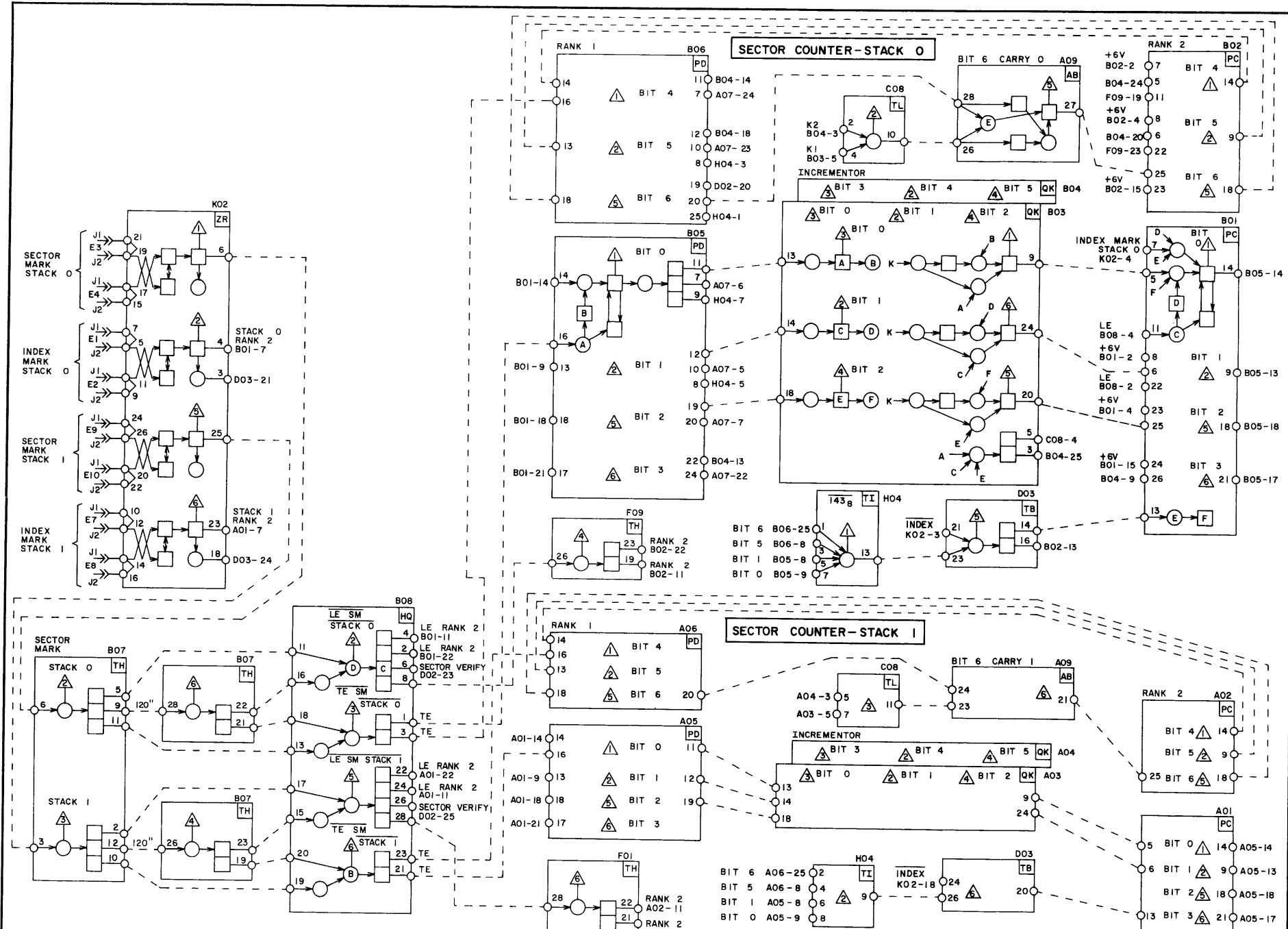
The data channel sends an active signal requesting the controller to send the first data word. In this case, the active serves as the first empty. The controller responds with the data word accompanied by a full signal. Thereafter, the data channel returns an empty signal to request more data. The process is repeated to the end of the buffer (record).



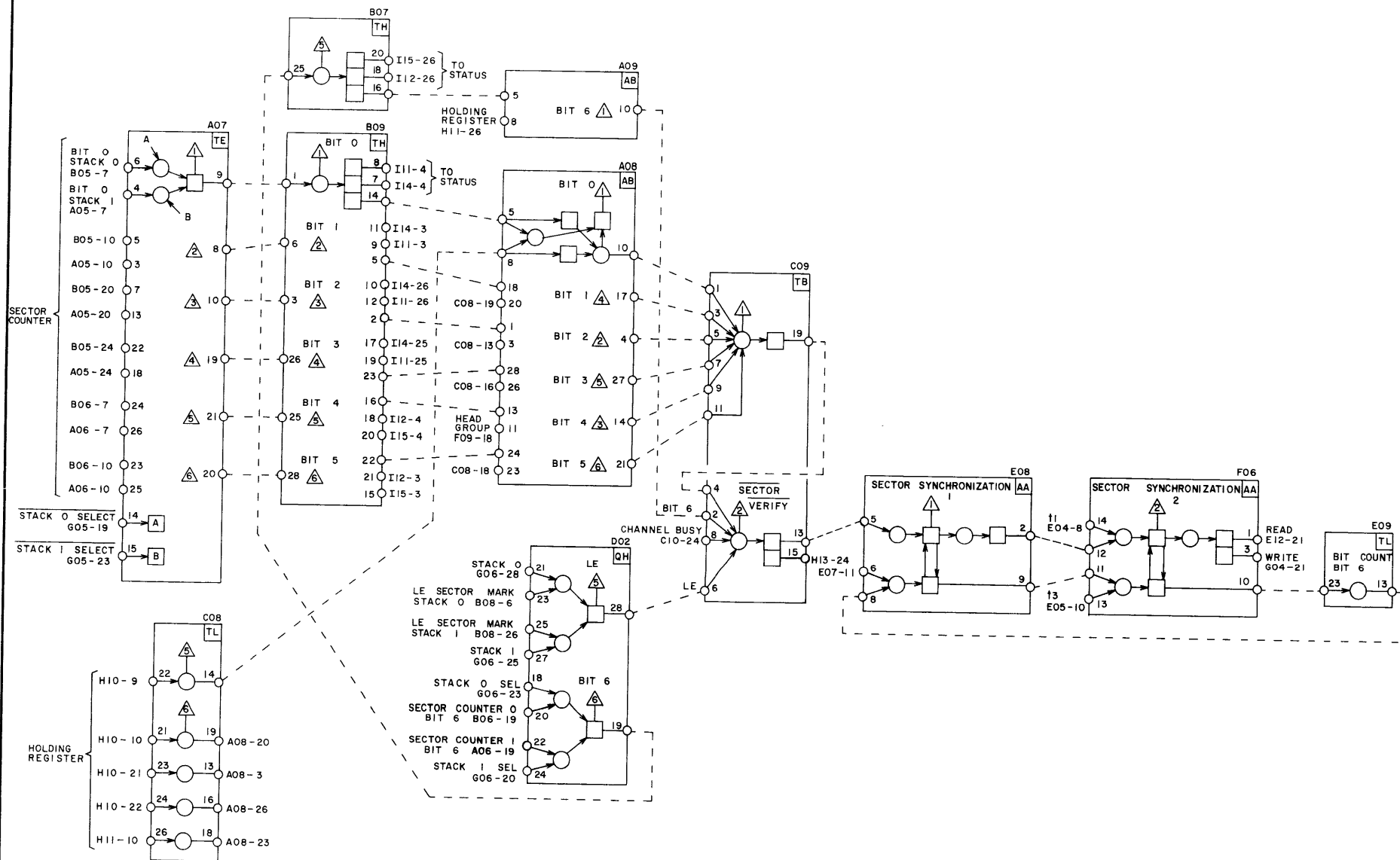
Sector mark pulses received from the disk file are gated to the sector counters for stacks 0 or 1. The leading edge of the sector mark pulse advances the increment count in rank 2, and the trailing edge transfer the count in rank 1. The rank 1 count represents the actual position (plus 1) of the read/write heads.

Since only 100_{10} sectors are used, the counter must be cleared to 0000 when 143_8 (100_{10}) is reached. The sector mark 0 pulse lags the index mark pulse by 20 microseconds, and its duration is wider than the other pulses as shown.





The contents of the sector counter, which reflect the actual position of the read/write heads, are compared against the holding register contents containing the designated sector address. Sector verify occurs when the leading edge pulse of a sector mark for the selected stack is present and the contents of the sector counter and holding register are equal.



CONTROL DATA

TITLE

DEVELOPMENT DIVISION

CONTROLLER
SECTOR VERIFY 2

PRODUCT
6639/ST OPT 10037

SIZE
C 60227300

REV.
F

SHEET
15

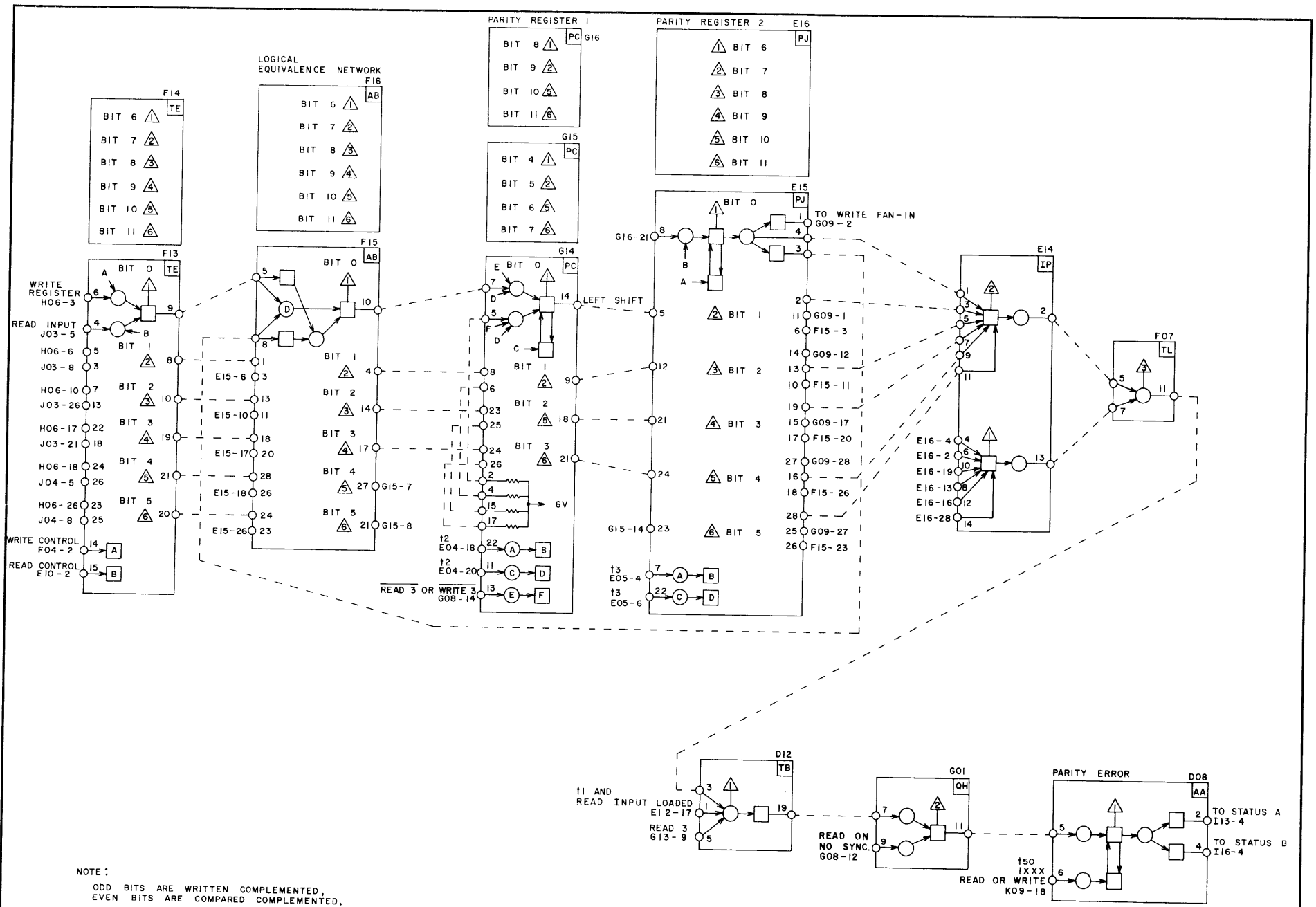
PAGE
5-31

A parity byte is generated for each record that is written on the disk. The parity byte is written on the disk at the end of the record. During a read operation, this previously written parity byte is read back and it should be the same as the parity byte generated from the record being read. If not, a parity error is present.

On a write, the contents of parity register 2 (register 2) should be initially all 0's. The contents of register 2 are merged with the first byte of the write word in the logical equivalence network. This forms the logical equivalent which is gated to parity register 1 (register 1). The contents of register 1 are then left-shifted one place (end-around) to register 2. The odd bits (1, 3, 5, etc.) in register 2 are com-

plemented and transferred to the write fan-in gates on each iteration. On the last iteration (at the end of the record), the complemented odd bits together with the uncomplemented even bits of register 2 are written on the disk as the parity byte.

As the record is transferred back during a read, the process is the same as for the write, except that the even bits in register 2 are complemented. Receiving a parity byte should cause a bit pattern of 2525_8 in register 1. The contents of register 1 are then left-shifted into register 2 for a resulting bit pattern of 5252_8 . The even bits of the parity byte are then complemented and all bits compared. This should cause all 1's to be gated out of register 2 which in turn results in no parity error.



CHANNEL BUSY

During initiation of a read or write operation, the channel busy FF sets to indicate an operation is in progress. It provides enables for gating sector verify, full, and empty signals to the data channel and terminating the operation when the right conditions are present. An inactive signal generated by either the data channel or the controller clears the channel busy FF.

INACTIVE

The inactive FF sets to return an inactive signal to the data channel for normal replies to the functions (read, write, position select, or head group select) or when the following abnormal conditions are present: setting of lost data FF; channel busy, active, and not ready; sector of 144_8 or greater selected and read 1 or write 1 FF set.

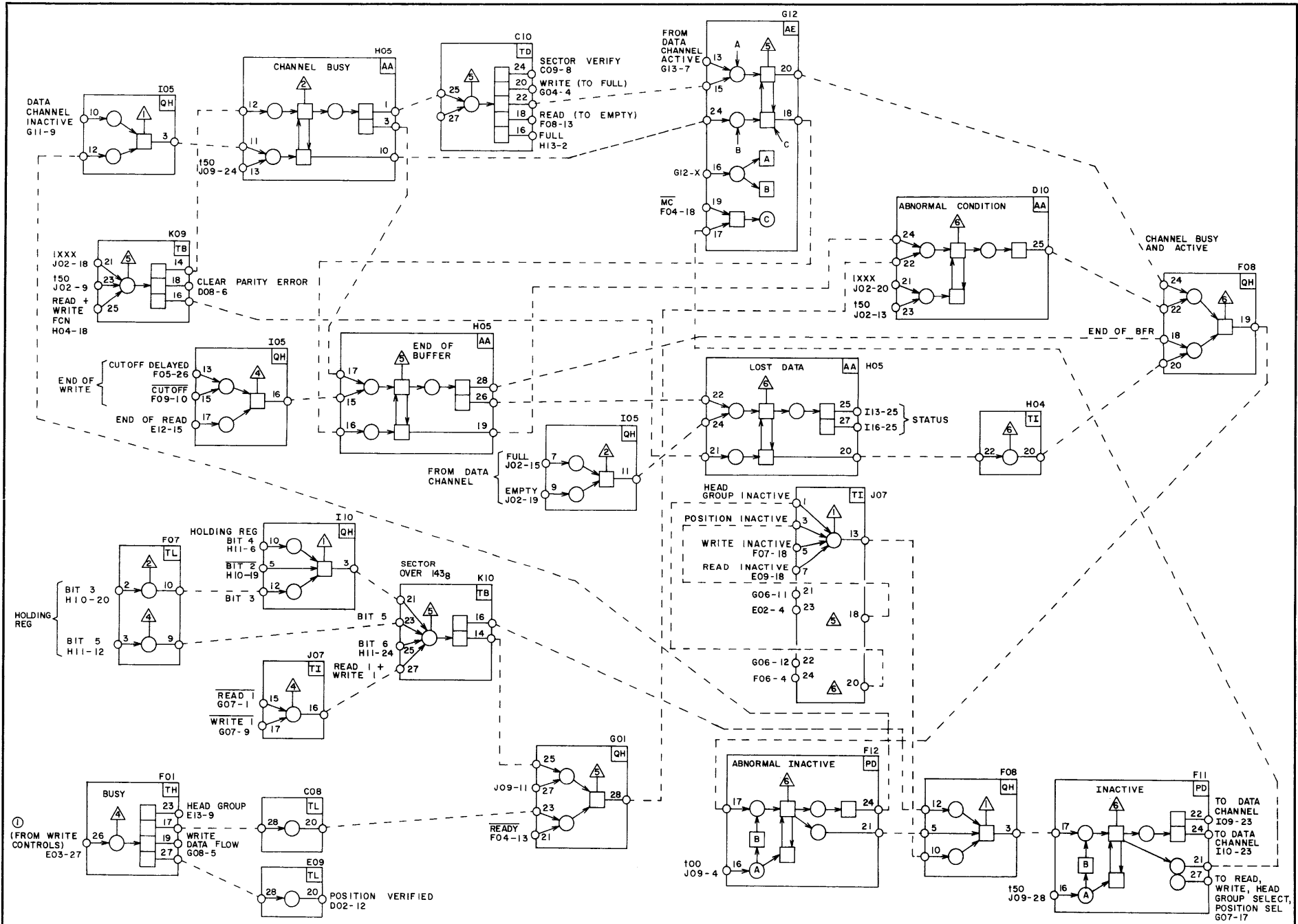
END OF BUFFER

The end of data on a write or the end of a read operation sets the end of buffer FF. The enables the lost data FF to set if a new full or empty signal is seen before an inactive.

LOST DATA

The lost data FF sets for the following conditions.

1. When an input or output buffer follows a read or write function, respectively, by more than 90 microseconds.
2. If program control issues a read or write function which is followed by two consecutive inputs or outputs.
3. If the instantaneous disk file rate exceeds the data channel rate.



NOTES:
 ① READ - WRITE ENABLE

| | | | |
|----------------------|-------------|--|-------------------|
| CONTROL DATA | | TITLE | PRODUCT |
| DEVELOPMENT DIVISION | | CONTROLLER CHANNEL BUSY, INACTIVE, END OF BUFFER, AND LOST DATA CONTROLS | 6639/ST OPT 10037 |
| SIZE | DRAWING NO. | REV. | |
| C | 60227300 | F | |
| SHEET | 17 | PAGE | 5-35 |

CELL COUNTER

The cell counter counts disk file clock pulses. It is used to count preamble bits for determining the beginning of data during a read or write operation. It provides three bit-count translations. These are 80_{10} (write preamble), 70_{10} (read preamble), and 112_{10} (forces setting of read 2 FF, page 5-25, in the event it is not set at the end of the preamble).

COMPUTER CLOCK

The 10-mHz input from the data channel (computer clocks) is used to provide 25-nanosecond timing pulses for sequencing operations between the computer and the controller.

The file clock logic receives clock pulses from a permanently recorded clock track in the disk file. These clock pulses provide for synchronizing the writing of data in the disk file. Times T1, T2, T3, and T4 come up in 100-nanosecond intervals.

Time T1 is a leading edge pulse formed off the file clock. Times T2, T3, and T4 are synchronized with the computer clock. Provisions are made to use the read self-clock when reading.

SECTION 6

MAINTENANCE

MAINTENANCE

INTRODUCTION

Maintenance procedures for the disk file controller follow the same general routines used in other Control Data equipment.

In addition to this manual, the following supporting documents provide information to aid maintenance personnel in servicing the equipment:

CONTROL DATA 6000 Series Input/Output Specifications Manual, (Publication No. 60045100)

CONTROL DATA Peripheral Controller Cabinets Manual (Publication No. 60097300)

CONTROL DATA Cordwood Modules Manual, Volumes 1, 2, and 3 (Publication No. 60042700)

CONTROLLER SPECIFICATIONS

PHYSICAL

| | |
|-----------------------|--|
| Height | 56-7/8 (1.44 m) |
| Width | 42 in. (1.07 m) |
| Depth | 20-1/2 in. (0.52 m) |
| Weight | 659 lb (300 kg) |
| Heat Dissipation | 4100 BTU/hr (1032 kg-cal/hr) |
| Operating Environment | 60° to 78°F (15.5° to 25.5°C) temperature 25% to 75% rh |

ELECTRICAL

208v, 3-phase, 400 Hz, 2.3 amp
120v, single-phase, 60 Hz, 2.8 amp

TRANSMISSION LINE ASSIGNMENTS

Refer to Tables 6-1 and 6-2 for cable wire assignments between the controller and the data channel and to Table 6-3 for controller-to-disk-file pin assignments.

TABLE 6-1. INPUT CABLE LINE ASSIGNMENTS - CONTROLLER TO DATA CHANNEL

| Input to Data Chan A or B From Controller Data Bit or Sig | 38W04 to Data Chan A From Controller Card, Pin | 38W05 Pass- Back to Controller (Interface A) Card, Pin | 38W06 to Data Chan B From Controller Card, Pin | 38W07 Pass- Back to Controller (Interface B) Card, Pin | Color Code of Wires Between Controller and Data Channel |
|--|---|--|---|--|--|
| 0 | K11-7 | K11-23 | K14-7 | K14-23 | 90 |
| 1 | K11-5 | K11-22 | K14-5 | K14-22 | 91 |
| 2 | K11-3 | K11-21 | K14-3 | K14-21 | 92 |
| 3 | K11-28 | K11-10 | K14-28 | K14-10 | 93 |
| 4 | K11-26 | K11-9 | K14-26 | K14-9 | 94 |
| 5 | K11-24 | K11-8 | K14-24 | K14-8 | 95 |
| 6 | K12-7 | K12-23 | K15-7 | K15-23 | 96 |
| 7 | K12-5 | K12-22 | K15-5 | K15-22 | 97 |
| 8 | K12-3 | K12-21 | K15-3 | K15-21 | 98 |
| 9 | K12-28 | K12-10 | K15-28 | K15-10 | 99 |
| 10 | K12-26 | K12-9 | K15-26 | K15-9 | 900 |
| 11 | K12-24 | K12-8 | K15-24 | K15-8 | 901 |
| Active | K13-7 | K13-23 | K16-7 | K16-23 | 902 |
| Inactive | K13-5 | K13-22 | K16-5 | K16-22 | 903 |
| Full | K13-3 | K13-21 | K16-3 | K16-21 | 904 |
| Empty | K13-28 | K13-10 | K16-28 | K16-10 | 905 |
| Clock (10 mc) | J13-12 | K13-26 | J16-12 | K16-26 | 906 |
| Clock (1 mc) | K13-8 | K13-24 | K16-8 | K16-24 | 907 |
| Not Used | | | | | 908 |

TABLE 6-2. OUTPUT CABLE LINE ASSIGNMENTS - DATA CHANNEL TO CONTROLLER

| Output From Data Chan A or B to Controller Data Bit or Signal | 38W00 From Data Chan A to Controller Card, Pin | 38W01 Pass-On From Controller (Interface A) Card, Pin | 38W02 From Data Chan B to Controller Card, Pin | 38W03 Pass-On From Controller (Interface B) Card, Pin | Color Code of Wires Between Controller and Data Channel |
|---|--|---|--|---|---|
| 0 | L07-3 | L07-1 | L12-3 | L12-1 | 90 |
| 1 | L07-13 | L07-15 | L12-13 | L12-15 | 91 |
| 2 | L07-16 | L07-14 | L12-16 | L12-14 | 92 |
| 3 | L07-26 | L07-28 | L12-26 | L12-28 | 93 |
| 4 | L08-3 | L08-1 | L13-3 | L13-1 | 94 |
| 5 | L08-13 | L08-15 | L13-13 | L13-15 | 95 |
| 6 | L08-16 | L08-14 | L13-16 | L13-14 | 96 |
| 7 | L08-26 | L08-28 | L13-26 | L13-28 | 97 |
| 8 | L09-3 | L09-1 | L14-3 | L14-1 | 98 |
| 9 | L09-13 | L09-15 | L14-13 | L14-15 | 99 |
| 10 | L09-16 | L09-14 | L14-16 | L14-14 | 900 |
| 11 | L09-26 | L09-28 | L14-26 | L14-28 | 901 |
| Active | L10-3 | L10-1 | L15-3 | L15-1 | 902 |
| Inactive | L10-13 | L10-15 | L15-13 | L15-15 | 903 |
| Full | L10-16 | L10-14 | L15-16 | L15-14 | 904 |
| Empty | L10-26 | L10-28 | L15-26 | L15-28 | 905 |
| Function | L11-3 | L11-1 | L16-3 | L16-1 | 906 |
| Master Clear | L11-13 | L11-15 | L16-13 | L16-15 | 907 |
| Not Used | | | | | 908 |

TABLE 6-3. CONTROLLER TO DISK FILE CABLE PIN ASSIGNMENTS

| Pin | Signal | Direction |
|-------|---------------------|----------------|
| A1-2 | Data Bit 0 | Bi-Directional |
| A3-4 | Data Bit 1 | Bi-Directional |
| A5-6 | Data Bit 2 | Bi-Directional |
| A7-8 | Data Bit 3 | Bi-Directional |
| A9-10 | Data Bit 4 | Bi-Directional |
| B1-2 | Data Bit 5 | Bi-Directional |
| B3-4 | Data Bit 6 | Bi-Directional |
| B5-6 | Data Bit 7 | Bi-Directional |
| B7-8 | Data Bit 8 | Bi-Directional |
| B9-10 | Data Bit 9 | Bi-Directional |
| C1-2 | Data Bit 10 | Bi-Directional |
| C3-4 | Data Bit 11 | Bi-Directional |
| C5-6 | Head Select | To Disk File |
| C7-8 | Position Select | To Disk File |
| C9-10 | On Point | From Disk File |
| D1-2 | Clear File | To Disk File |
| D3-4 | Select File Station | To Disk File |
| D5-6 | Write Enable | To Disk File |
| D7-8 | Read Clock | From Disk File |
| D9-10 | Read Enable | To Disk File |
| E1-2 | Index Mark Stack 0 | From Disk File |
| E3-4 | Sector Mark Stack 0 | From Disk File |
| E5-6 | Write Clock Stack 0 | From Disk File |
| E7-8 | Index Mark Stack 1 | From Disk File |
| E9-10 | Sector Mark Stack 1 | From Disk File |
| F1-2 | Write Clock Stack 1 | From Disk File |
| F3-4 | Ready | From Disk File |
| F5-6 | Disk File Select | To Disk File |
| F7-8 | Disk File Select | To Disk File |
| F9-10 | Terminator Power | * |

*Terminator power is provided to the disk file and controller through a separate two-wire power cable.

SECTION 7

MAINTENANCE AIDS

6639/STANDARD OPTION 10037 CARD PLACEMENT

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|-----------------------------|----|--------------------|----|-----------------------------|-------|---------------------------|---------|-------------------|----|---------------------------|----|----|----|----|----|----|
| A | PC | PC | QK | QK | PD | PD | TE | AB | AB | AA | | | | | | | A |
| | SECTOR COUNTER STACK I | | | | SECTOR VERIFY | | | | | | | | | | | | |
| B | PC | PC | QK | QK | PD | PD | TH | HQ | TH | AA | | TL | TQ | TI | | | B |
| | SECTOR COUNTER STACK O | | | | CONTROL | | | | | | | | | | | | |
| C | PC | PC | | | PJ | PJ | TE | TL | TB | TD | PD | PD | QK | QK | PC | PC | C |
| | POSITION COUNTER | | | | CONTROLS | | | | | | CELL COUNTER | | | | | | |
| D | | QH | TB | | PJ | | AE | AA | XL | AA | | TB | QH | | | | D |
| | POSITION VERIFY, NULL DELAY | | VERIFY, READY | | DELAY | | UNIT SELECT | | | | CONTROL | | | | | | |
| E | TH | AA | HQ | HC | HC | HC | HC | AA | TL | TH | HC | TB | TB | IP | PJ | PJ | E |
| | POSITION VERIFY | | FILE CLOCK | | | | FUNCTIONS & CONTROL | | | | PARITY | | | | | | |
| F | TH | PD | PD | TH | AA | AA | TL | QH | TH | AA | PD | PD | TE | TE | AB | AB | F |
| | FILE CLOCK | | CONTROL | | FUNCTIONS & CONTROL | | | | PARITY | | | | | | | | |
| G | QH | TC | TD | TB | PD | PD | AE | TB | TE | TE | CX | AE | TH | PC | PC | PC | G |
| | FUNCTIONS & CONTROL | | | | WRITE FAN-IN GATES | | | | CONTROL | | PARITY | | | | | | |
| H | | | | | TI | AA | PJ | PJ | IP | PJ | PO | PO | PO | QH | IV | KL | PJ |
| | | | | | CONTROL | | WRITE & BUFFER REGISTERS | | HOLDING REGISTER | | FUNCTION TRANS. & CONTROL | | | | | | |
| I | | | | | KS | KS | QH | TE | TE | TE | QH | QH | TG | TG | TG | TG | I |
| | PHASE MODULATOR | | CONTROL | | INTERFACE GATES | | UNIT SEL | | GATES TO CHANNELS | | | | | | | | |
| J | | TH | SB | SB | SB | XL | TI | TH | HC | TH | TD | TD | HQ | TD | TD | HQ | J |
| | CONTROL | | READ DATA REGISTER | | | DELAY | | CONTROL | | | COMPUTER CLOCK | | | | | | |
| K | ZR | ZR | ZR | AA | CX | AE | AE | TD | TB | TB | QJ | QJ | QJ | QJ | QJ | QJ | K |
| | SIGNALS FROM DISK FILE | | CONNECT & STATUS | | | | DATA & SIGNALS TO CHANNEL | | | | | | | | | | |
| L | ZS | ZS | ZS | ZS | ZT | ZT | QI | QI | QI | QI | QI | QI | QI | QI | QI | QI | L |
| | DATA TO & FROM DISK FILE | | SIGNALS TO FILE | | DATA & SIGNALS FROM CHANNEL | | | | | | | | | | | | |

P/N 18079700

NOTE

Standard Option 10037-A does not use location CO6.

SECTION 8

PARTS LIST

PARTS LIST

INTRODUCTION

The parts list provides the identification and ordering data necessary for the replacement of electrical and hardware parts for Control Data Standard Option 10037-A and the 6639 Disk File Controller .

Electrical contents: all chassis and cabinet items are included except jumper wires and bulk wires.

The chassis assembly and associated subassemblies are broken down into individual parts and are listed in alphabetical rather than disassembly order.

The following publications contain information on printed circuit card assemblies, peripheral cabinets, power supplies, and vendor parts lists necessary to complete a total breakdown of the equipment. Order manuals from Literature Distribution Services Catalog.

Ault Power Supply Manual

Control Data Power Supply Manual

Peripheral Controller Cabinets Customer Engineering Instruction Manual
(Includes cabinet parts list and Control Data modifications to vendor power supplies.)

ORDERING OF PARTS

When ordering Control Data parts, include the following information: Control Data drawing number, description, quantity needed, equipment used on. When ordering vendor parts use the procedure indicated by that vendor.

| CDC - DRAWING NUMBER | DESCRIPTION | QUANTITY EACH MACHINE |
|-------------------------|---|-----------------------------|
| 17801900 | Bar, Mounting, Card | |
| 18027900 | Bar, Mounting, Receptacle | |
| 18082800 | Bar, Support | |
| 17944100 | Blank Card Cap | |
| 17992900 | Bracket, Mounting, Panel, LH | |
| 17993000 | Bracket, Mounting, Panel, RH | |
| 18028000 | Bus Bar, Horizontal | |
| 17902300 | Cabinet Assembly, Peripheral Type B | |
| 18164200 | Capacitor, Fixed, Electrolytic, 300UF, 10 VDC | |
| 18079700 | Card Placement | |
| 18039400 | Chassis Assembly | |
| 17928300 | Clamp, Bus Bar | |
| 17900200 | Clamp, Bus Bar | |
| 00863707 | Clamp, Cable, 0.52 ID | |
| 18240800 | Connector Assembly, 61 Socket, J01 | |
| 24518103 | Connector, Flexible, 3/4 Conduit | |
| 24562500 | Connector, Receptacle, 30 Socket | |
| 24532300 | Connector, Receptacle, 61 Pin | |
| 30094402 | Connector, Receptacle, Red, 10 Socket | |
| 30094406 | Connector, Receptacle, Blue, 10 Socket | |
| 30094410 | Connector, Receptacle, Black, 10 Socket | |
| 30000901 | Connector, Receptacle, 61 Socket | |
| 46910000 | Disk File | |
| 00865004 | Grommet, Strain Relief | |
| 17912702 | Insulator Strip, Bus Bar | |
| 17913800 | Member, Frame, Chassis, RH | |
| 18038200 | Member, Frame, Chassis, LH | |
| 18076100 | Panel, Mounting, Connector | |
| 17941500 | Panel, Filler | |
| 17884500 | Panel, Filler, Front | |
| 17881400 | Power Supply Assembly | |
| 30001201 | Resistor-Terminator Assembly | |
| 17805300 | Seal, Rubber, Connector | |
| 30000902 | Socket for Connector 30000901 | |

| CDC - DRAWING NUMBER | DESCRIPTION | QUANTITY EACH MACHINE |
|-------------------------|---|-----------------------------|
| 17932700 | Strip, Marker, Horizontal, Light Blue, -6 | |
| 17932701 | Strip, Marker, Horizontal, Light Red, +6 | |
| 18228800 | Wire List, Logic | |

| CDC - DRAWING NUMBER | DESCRIPTION | QUANTITY EACH MACHINE |
|-------------------------|--|-----------------------------|
| 63040000 | Printed Circuit Module Assembly, Type AA | 52543600 |
| 63040100 | Printed Circuit Module Assembly, Type AB | 3500 |
| 63040400 | Printed Circuit Module Assembly, Type AE | 3200 |
| 63042900 | Printed Circuit Module Assembly, Type CX | 2600 |
| 63044800 | Printed Circuit Module Assembly, Type HC | 52567500 |
| 63046200 | Printed Circuit Module Assembly, Type HQ | 2100 |
| 63048700 | Printed Circuit Module Assembly, Type IP | 52544200 |
| 63049300 | Printed Circuit Module Assembly, Type IV | 52544500 |
| 63051500 | Printed Circuit Module Assembly, Type JR | 8200 |
| 63053200 | Printed Circuit Module Assembly, Type KL | |
| 63053800 | Printed Circuit Module Assembly, Type KS | |
| 63057800 | Printed Circuit Module Assembly, Type PC | |
| 63057900 | Printed Circuit Module Assembly, Type PD | |
| 63058400 | Printed Circuit Module Assembly, Type PJ | |
| 63058900 | Printed Circuit Module Assembly, Type PO | |
| 63060700 | Printed Circuit Module Assembly, Type QH | |
| 63060800 | Printed Circuit Module Assembly, Type QI | |
| 63060900 | Printed Circuit Module Assembly, Type QJ | |
| 63061000 | Printed Circuit Module Assembly, Type QK | |
| 63062700 | Printed Circuit Module Assembly, Type SB | |
| 63063400 | Printed Circuit Module Assembly, Type TB | |
| 63063500 | Printed Circuit Module Assembly, Type TC | |
| 63063600 | Printed Circuit Module Assembly, Type TD | |
| 63063700 | Printed Circuit Module Assembly, Type TE | |
| 63063900 | Printed Circuit Module Assembly, Type TG | |
| 63064000 | Printed Circuit Module Assembly, Type TH | |
| 63064100 | Printed Circuit Module Assembly, Type TI | |
| 63064400 | Printed Circuit Module Assembly, Type TL | |
| 63065500 | Printed Circuit Module Assembly, Type XL | |
| 17876300 | Printed Circuit Module Assembly, Type ZR | |
| 17876100 | Printed Circuit Module Assembly, Type ZS | |
| 17876500 | Printed Circuit Module Assembly, Type ZT | |

SECTION 9

WIRE LISTS

SECTION 10

EQUATION SUMMARY

(Not Applicable)

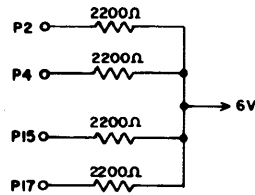
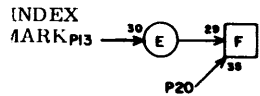
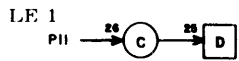
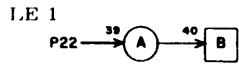
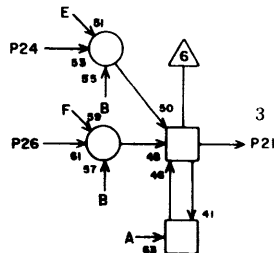
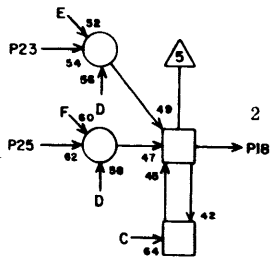
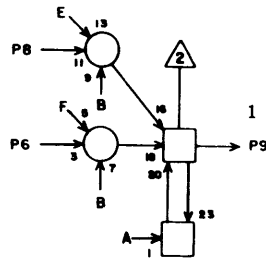
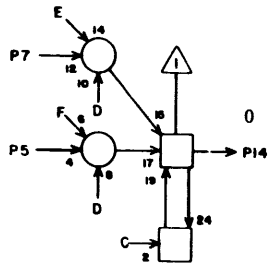
CHASSIS TABS

LS 63057800
ASSY **C**
REV

SECTOR COUNTER - STACK 1
RANK 2, BITS 0-3

PC

RV 1A01



| RV | PC | LG |
|----|--------|----|
| 1 | - | |
| 2 | A01- 8 | 3 |
| 3 | - | |
| 4 | A01-23 | 5 |
| 5 | A03- 9 | 5 |
| 6 | A03-24 | 7 |
| 7 | K02-23 | 37 |
| 8 | A01- 2 | 3 |
| 9 | A05-13 | 7 |
| 10 | - | |
| 11 | B08-24 | 13 |
| 12 | - | |
| 13 | D03-20 | 13 |
| 14 | A05-14 | 7 |
| 15 | A01-24 | 5 |
| 16 | - | |
| 17 | - | |
| 18 | A05-18 | 7 |
| 19 | - | |
| 20 | A01- x | 2 |
| 21 | A05-17 | 7 |
| 22 | B08-22 | 13 |
| 23 | A01- 4 | 5 |
| 24 | A01-15 | 5 |
| 25 | A03-20 | 5 |
| 26 | A04- 9 | 7 |
| 27 | - | |
| 28 | - | |

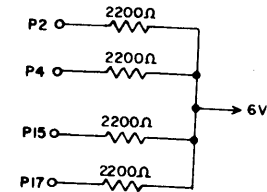
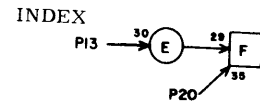
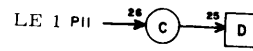
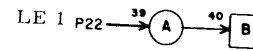
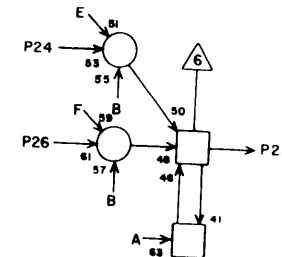
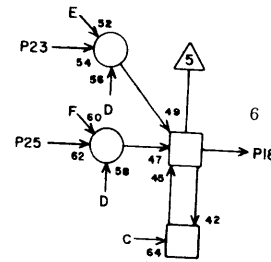
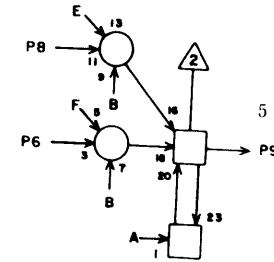
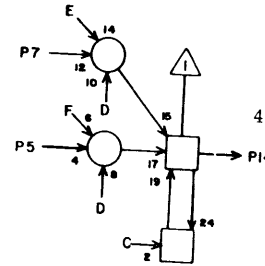
JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63057800
ASSY **C**
REV

SECTOR COUNTER - STACK 1
RANK 2, BITS 4-6

PC

RV G A02



| RV | G | A02 |
|----|--------|-----|
| 1 | - | |
| 2 | A02- 7 | 5 |
| 3 | - | |
| 4 | A02- 8 | 3 |
| 5 | A04-24 | 5 |
| 6 | A04-20 | 7 |
| 7 | A02- 2 | 5 |
| 8 | A02- 4 | 3 |
| 9 | A06-13 | 7 |
| 10 | - | |
| 11 | F01-22 | 21 |
| 12 | - | |
| 13 | D03-22 | 13 |
| 14 | A06-14 | 7 |
| 15 | A02-23 | 5 |
| 16 | - | |
| 17 | - | |
| 18 | A06-18 | 7 |
| 19 | - | |
| 20 | - | |
| 21 | - | |
| 22 | F01-21 | 19 |
| 23 | A02-15 | 5 |
| 24 | - | |
| 25 | A09-21 | 11 |
| 26 | - | |
| 27 | - | |
| 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

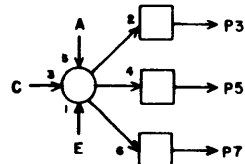
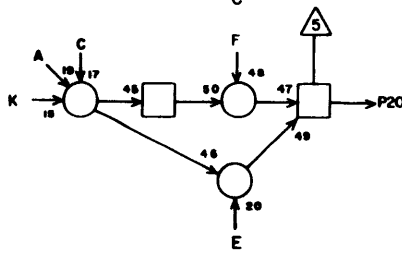
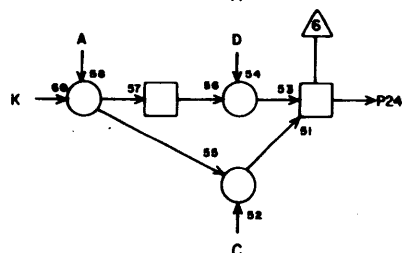
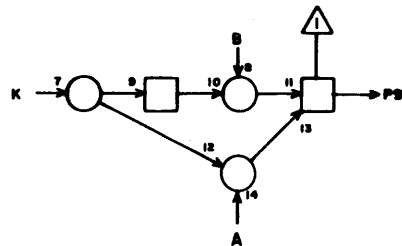
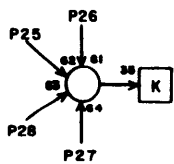
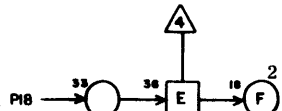
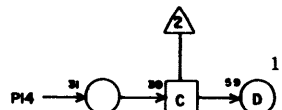
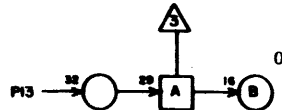
LS 63061000
ASSY

3
REV

SECTOR COUNTER - STACK 1
INCREMENTOR, BITS 0-2

QH

RV G A03



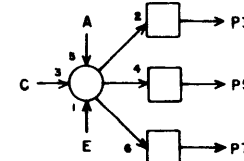
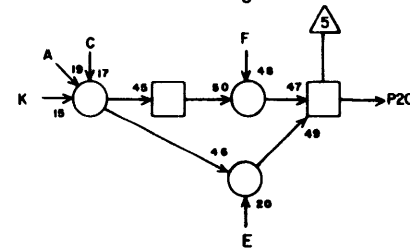
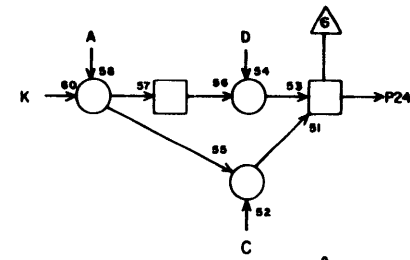
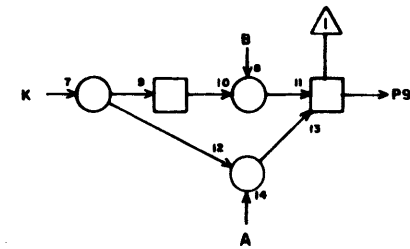
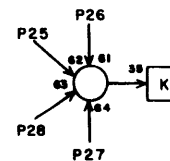
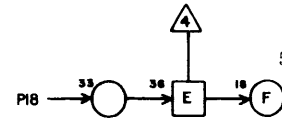
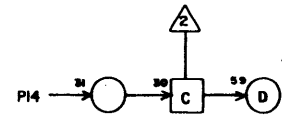
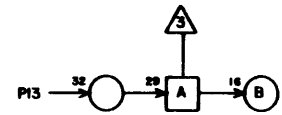
LS 63061000
ASSY

3
REV

SECTOR COUNTER - STACK 1
INCREMENTOR, BITS 3-5

QH

RV G A04



| | | |
|----|--------|----|
| 1 | - | |
| 2 | - | |
| 3 | A04-25 | 5 |
| 4 | - | |
| 5 | C08-7 | 13 |
| 6 | - | |
| 7 | - | |
| 8 | - | |
| 9 | A01-5 | 5 |
| 10 | - | |
| 11 | - | |
| 12 | - | |
| 13 | A05-11 | 5 |
| 14 | A05-12 | 5 |
| 15 | - | |
| 16 | - | |
| 17 | - | |
| 18 | A05-19 | 5 |
| 19 | - | |
| 20 | A01-25 | 5 |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | A01-6 | 7 |
| 25 | A03-X | 2 |
| 26 | A03-X | 2 |
| 27 | A03-X | 2 |
| 28 | A03-X | 2 |

JACK PIN LG
CIRCUIT SPECIFICATION 1027600

60227300 F

| | | |
|----|--------|----|
| 1 | - | |
| 2 | - | |
| 3 | C08-5 | 11 |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | - | |
| 8 | - | |
| 9 | A01-26 | 7 |
| 10 | - | |
| 11 | - | |
| 12 | - | |
| 13 | A05-22 | 5 |
| 14 | A06-11 | 5 |
| 15 | - | |
| 16 | - | |
| 17 | - | |
| 18 | A06-12 | 5 |
| 19 | - | |
| 20 | A02-6 | 7 |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | A02-5 | 5 |
| 25 | A03-3 | 5 |
| 26 | A04-X | 2 |
| 27 | A04-X | 2 |
| 28 | A04-X | 2 |

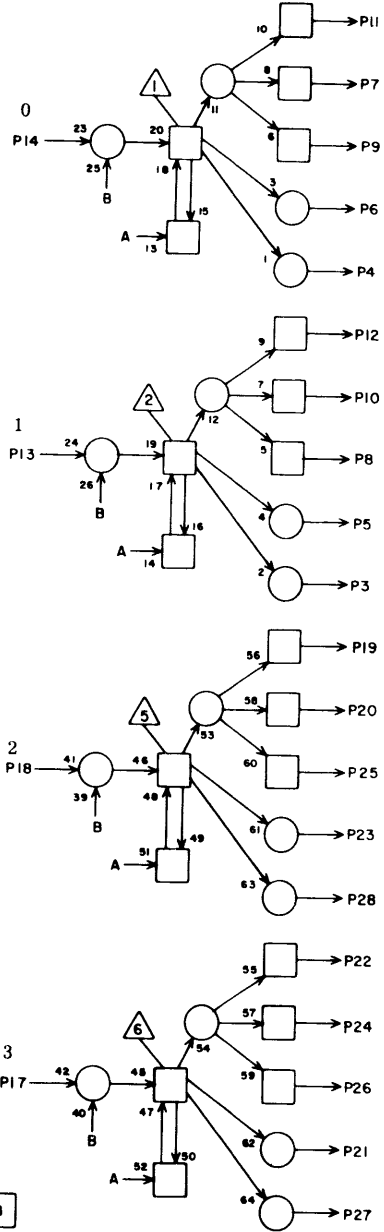
JACK PIN LG
CIRCUIT SPECIFICATION 1027600

60227300 F

LS 63057900
ASSY

B
REV

SECTOR COUNTER - STACK 1
RANK 1, BITS 0-3



PD

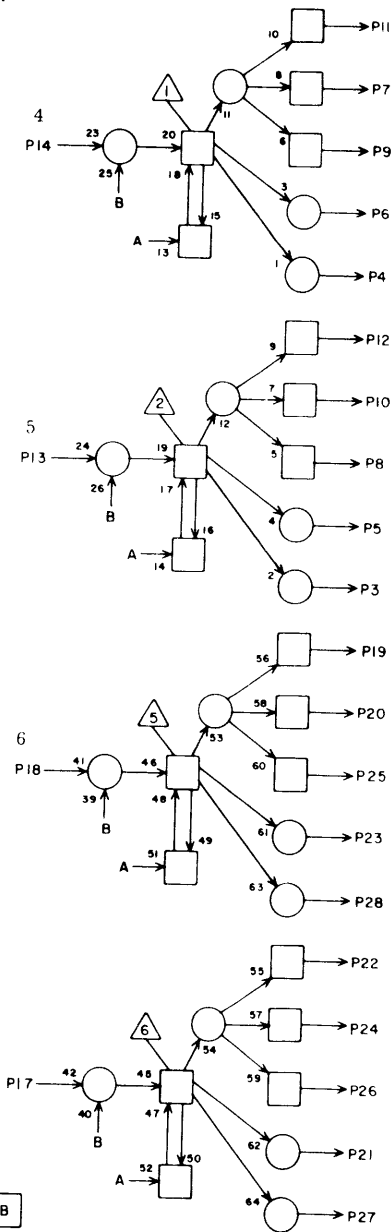
| RV | G | A05 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | A07-4 | 5 |
| 8 | H04-6 | 27 |
| 9 | H04-8 | 27 |
| 10 | A07-3 | 7 |
| 11 | A03-13 | 5 |
| 12 | A03-14 | 5 |
| 13 | A01-9 | 7 |
| 14 | A01-14 | 7 |
| 15 | - | |
| 16 | B08-21 | 9 |
| 17 | A01-21 | 7 |
| 18 | A01-18 | 7 |
| 19 | A03-18 | 5 |
| 20 | A07-13 | 7 |
| 21 | - | |
| 22 | A04-13 | 5 |
| 23 | - | |
| 24 | A07-18 | 5 |
| 25 | - | |
| 26 | - | |
| 27 | - | |
| 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63057900
ASSY

B
REV

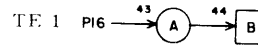
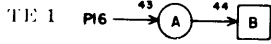
SECTOR COUNTER - STACK 1
RANK 1, BITS 4-6



PD

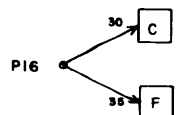
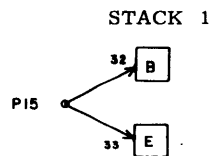
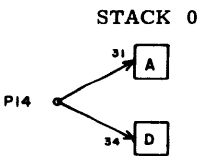
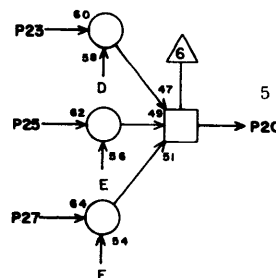
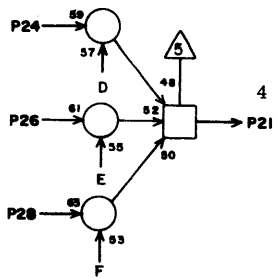
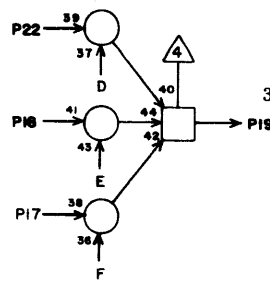
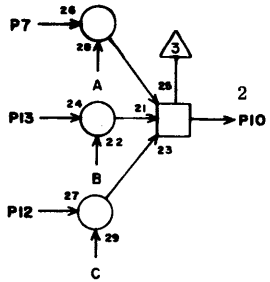
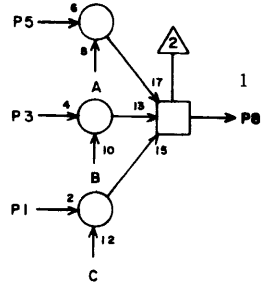
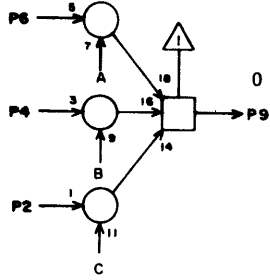
| RV | G | A06 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | A07-26 | 5 |
| 8 | H04-4 | 27 |
| 9 | - | |
| 10 | A07-25 | 5 |
| 11 | A04-14 | 5 |
| 12 | A04-18 | 5 |
| 13 | A02-9 | 7 |
| 14 | A02-14 | 7 |
| 15 | - | |
| 16 | B08-23 | 9 |
| 17 | - | |
| 18 | A02-18 | 7 |
| 19 | D02-22 | 15 |
| 20 | A09-24 | 7 |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | - | |
| 25 | H04-2 | 25 |
| 26 | - | |
| 27 | - | |
| 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F



LS 63063700
ASSY

REV

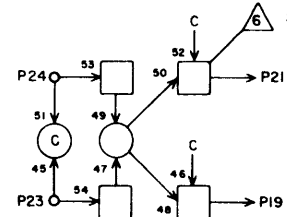
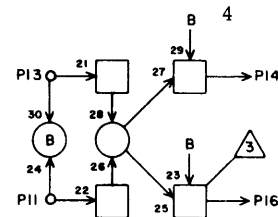
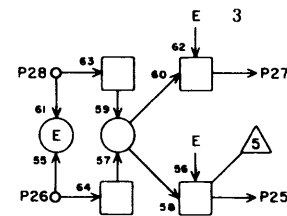
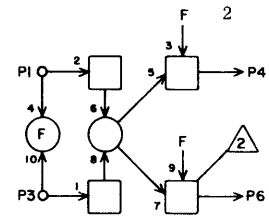
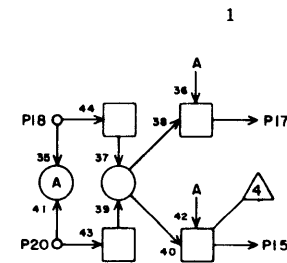
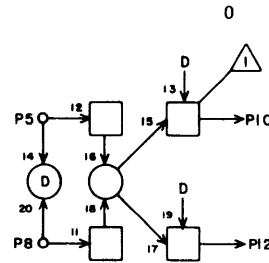


JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

| TE | RV | G | A07 |
|----|----|--------|-----|
| | 1 | - | |
| | 2 | - | |
| | 3 | A05-10 | 7 |
| | 4 | A05-7 | 5 |
| | 5 | B05-10 | 9 |
| | 6 | B05-7 | 7 |
| | 7 | B05-20 | 9 |
| | 8 | B09-6 | 7 |
| | 9 | B09-1 | 7 |
| | 10 | B09-3 | 7 |
| | 11 | - | |
| | 12 | - | |
| | 13 | A05-20 | 7 |
| | 14 | G05-19 | 23 |
| | 15 | G05-23 | 25 |
| | 16 | A07-X | 2 |
| | 17 | - | |
| | 18 | A05-24 | 5 |
| | 19 | B09-26 | 7 |
| | 20 | B09-28 | 9 |
| | 21 | B09-25 | 7 |
| | 22 | B05-24 | 7 |
| | 23 | B06-10 | 7 |
| | 24 | B06-7 | 5 |
| | 25 | A06-10 | 5 |
| | 26 | A06-7 | 5 |
| | 27 | - | |
| | 28 | - | |

LS 63040100
ASSY

REV



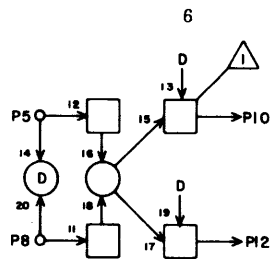
| AB | RV | G | A08 |
|----|----|--------|-----|
| | 1 | B09-2 | 7 |
| | 2 | - | |
| | 3 | C08-13 | 11 |
| | 4 | C09-5 | 11 |
| | 5 | B09-14 | 7 |
| | 6 | - | |
| | 7 | - | |
| | 8 | C08-14 | 11 |
| | 9 | - | |
| | 10 | C09-1 | 9 |
| | 11 | F09-10 | 21 |
| | 12 | - | |
| | 13 | B09-16 | 7 |
| | 14 | C09-9 | 9 |
| | 15 | - | |
| | 16 | - | |
| | 17 | C09-3 | 9 |
| | 18 | B09-5 | 7 |
| | 19 | - | |
| | 20 | C08-19 | 9 |
| | 21 | C09-11 | 9 |
| | 22 | - | |
| | 23 | C08-18 | 9 |
| | 24 | B09-22 | 7 |
| | 25 | - | |
| | 26 | C08-16 | 9 |
| | 27 | C09-7 | 9 |
| | 28 | B09-23 | 7 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600

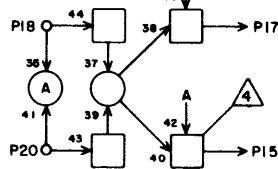
60227300 F

LS 63040100
ASSY

E
REV

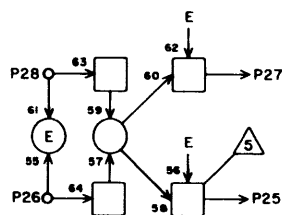
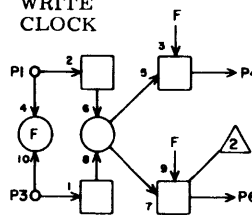


HEAD GROUP
NULL DELAY

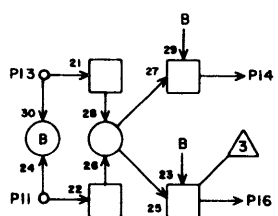


SECTOR COUNTER BIT 6
CARRY 0

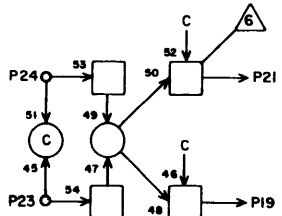
WRITE
CLOCK



BIT COUNTER
CARRY BIT 6



SM BIT 6
CARRY 1



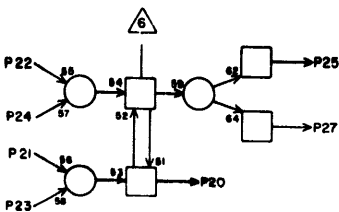
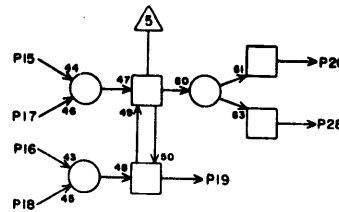
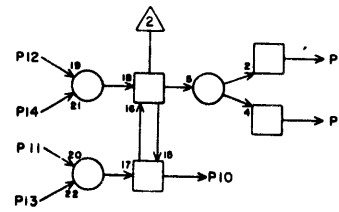
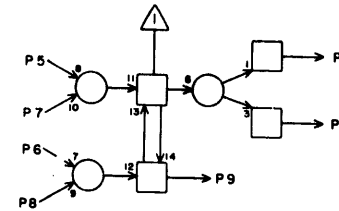
WRITE
ENABLE

| AB | RV | G | A09 |
|----|----|--------|-----|
| | 1 | F01-2 | 23 |
| | 2 | - | |
| | 3 | F01-9 | 25 |
| | 4 | I03-7 | 31 |
| | 5 | B07-16 | 9 |
| | 6 | - | |
| | 7 | - | |
| | 8 | H11-26 | 29 |
| | 9 | - | |
| | 10 | C09-2 | 9 |
| | 11 | C08-9 | 9 |
| | 12 | - | |
| | 13 | C16-18 | 13 |
| | 14 | C12-18 | 11 |
| | 15 | - | |
| | 16 | - | |
| | 17 | A10-5 | 5 |
| | 18 | F09-13 | 19 |
| | 19 | - | |
| | 20 | C08-15 | 9 |
| | 21 | A02-25 | 11 |
| | 22 | - | |
| | 23 | C08-11 | 9 |
| | 24 | A06-20 | 7 |
| | 25 | - | |
| | 26 | C08-10 | 9 |
| | 27 | B02-25 | 11 |
| | 28 | B06-20 | 7 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS625415600
ASSY

B
REV



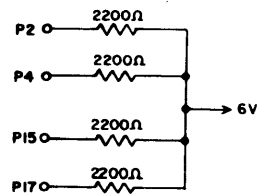
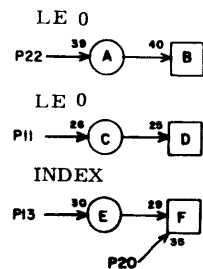
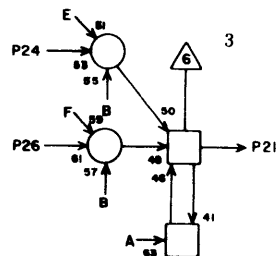
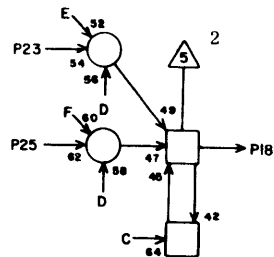
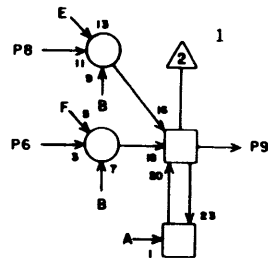
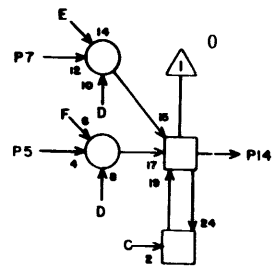
| RV | LA10 |
|----|------------|
| 1 | G06-13 25 |
| 2 | D02-13 17 |
| 3 | D02-15 17 |
| 4 | - |
| 5 | A09-17 5 |
| 6 | G07-27 25 |
| 7 | J09-14 132 |
| 8 | - |
| 9 | - |
| 10 | - |
| 11 | G05-8 25 |
| 12 | E13-19 17 |
| 13 | - |
| 14 | E04-16 19 |
| 15 | |
| 16 | |
| 17 | |
| 18 | |
| 19 | |
| 20 | |
| 21 | |
| 22 | |
| 23 | |
| 24 | |
| 25 | |
| 26 | |
| 27 | |
| 28 | |

CIRCUIT SPECIFICATION 11827600
60227300 G

LS 63057800 **C**
 ASSY REV

SECTOR COUNTER - STACK 0
 RANK 2, BITS 0-3

| PC | RV | G | B01 |
|----|----|--------|-----|
| | 1 | - | |
| | 2 | 801-8 | 3 |
| | 3 | - | |
| | 4 | 801-23 | 5 |
| | 5 | 803-9 | 5 |
| | 6 | 803-24 | 7 |
| | 7 | K02-4 | 31 |
| | 8 | 801-2 | 3 |
| | 9 | 805-13 | 7 |
| | 10 | - | |
| | 11 | 803-4 | 11 |
| | 12 | - | |
| | 13 | 003-14 | 11 |
| | 14 | 805-14 | 7 |
| | 15 | 801-24 | 5 |
| | 16 | - | |
| | 17 | - | |
| | 18 | 805-18 | 7 |
| | 19 | - | |
| | 20 | - | |
| | 21 | 805-17 | 7 |
| | 22 | 808-2 | 11 |
| | 23 | 801-4 | 5 |
| | 24 | 801-15 | 5 |
| | 25 | 803-20 | 5 |
| | 26 | 804-9 | 7 |
| | 27 | - | |
| | 28 | - | |

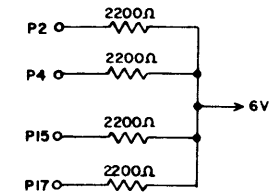
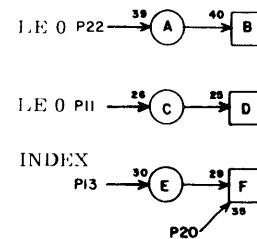
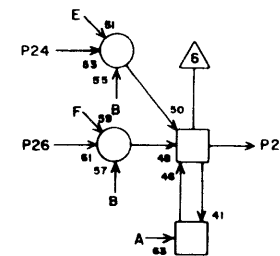
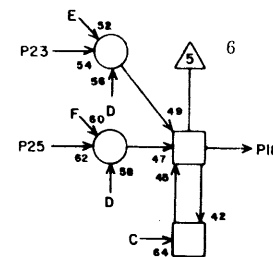
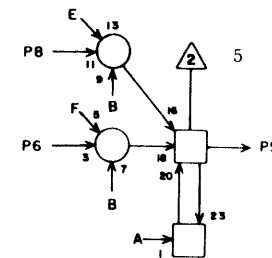
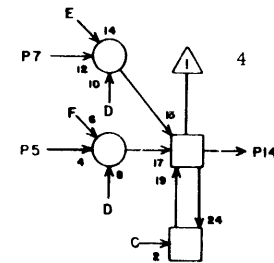


JACK PIN LG
 CIRCUIT SPECIFICATION I1827600
 60227300 F

LS 63057800 **C**
 ASSY REV

SECTOR COUNTER - STACK 0
 RANK 2, BITS 4-6

| PC | RV | G | B02 |
|----|----|--------|-----|
| | 1 | - | |
| | 2 | 802-7 | 5 |
| | 3 | - | |
| | 4 | 802-8 | 3 |
| | 5 | 804-24 | 5 |
| | 6 | 804-20 | 7 |
| | 7 | 802-2 | 5 |
| | 8 | 802-4 | 3 |
| | 9 | 806-13 | 7 |
| | 10 | - | |
| | 11 | F09-19 | 21 |
| | 12 | - | |
| | 13 | 003-16 | 11 |
| | 14 | 806-14 | 7 |
| | 15 | 802-23 | 5 |
| | 16 | - | |
| | 17 | - | |
| | 18 | 806-18 | 7 |
| | 19 | - | |
| | 20 | - | |
| | 21 | - | |
| | 22 | F09-23 | 21 |
| | 23 | 802-15 | 5 |
| | 24 | - | |
| | 25 | A09-27 | 11 |
| | 26 | - | |
| | 27 | - | |
| | 28 | - | |



JACK PIN LG
 CIRCUIT SPECIFICATION I1827600
 60227300 F

LS 63061000
ASSY

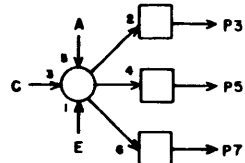
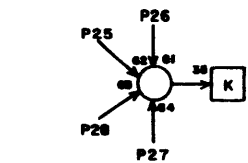
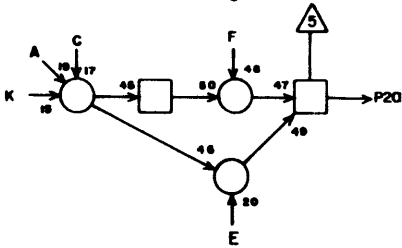
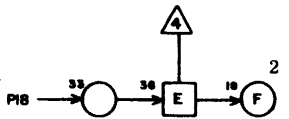
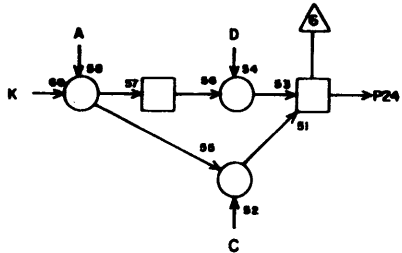
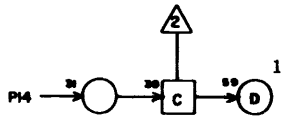
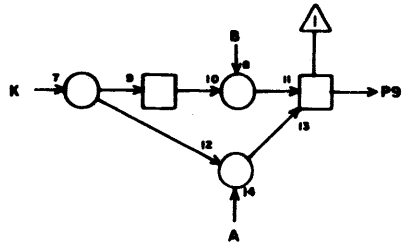
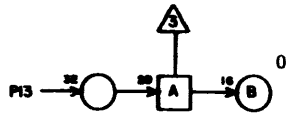
REV

SECTOR COUNTER - STACK 0
INCREMENTOR, BITS 0-2

OK

RV G

B03



| | | |
|----|--------|---|
| 1 | - | |
| 2 | - | |
| 3 | B04-25 | 5 |
| 4 | - | |
| 5 | C08-4 | 9 |
| 6 | - | |
| 7 | - | |
| 8 | - | |
| 9 | B01-5 | 5 |
| 10 | - | |
| 11 | - | |
| 12 | - | |
| 13 | B05-11 | 5 |
| 14 | B05-12 | 5 |
| 15 | - | |
| 16 | - | |
| 17 | - | |
| 18 | B05-19 | 5 |
| 19 | - | |
| 20 | B01-25 | 5 |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | B01-6 | 7 |
| 25 | B03-X | 2 |
| 26 | B03-X | 2 |
| 27 | B03-X | 2 |
| 28 | B03-X | 2 |

JACK PIN LG
CIRCUIT SPECIFICATION 1N27600
60227300 F

LS 63061000
ASSY

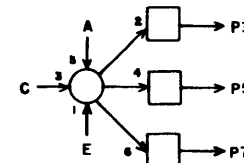
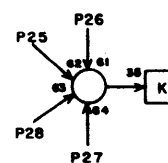
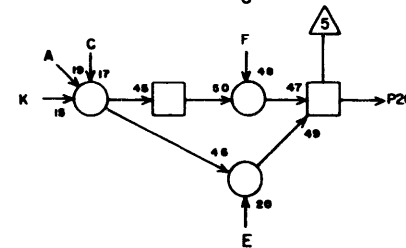
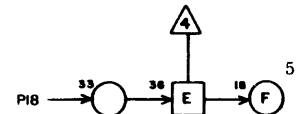
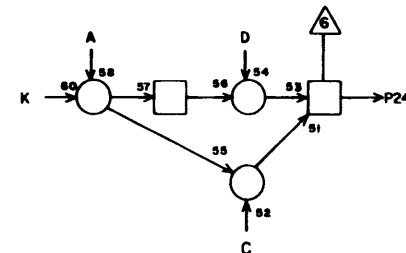
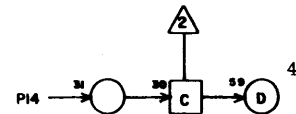
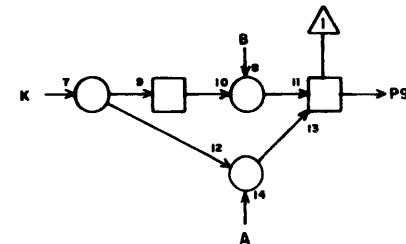
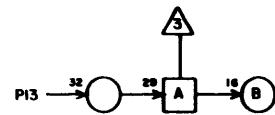
REV

SECTOR COUNTER - STACK 0
INCREMENTOR, BITS 3-5

OK

RV G

B04



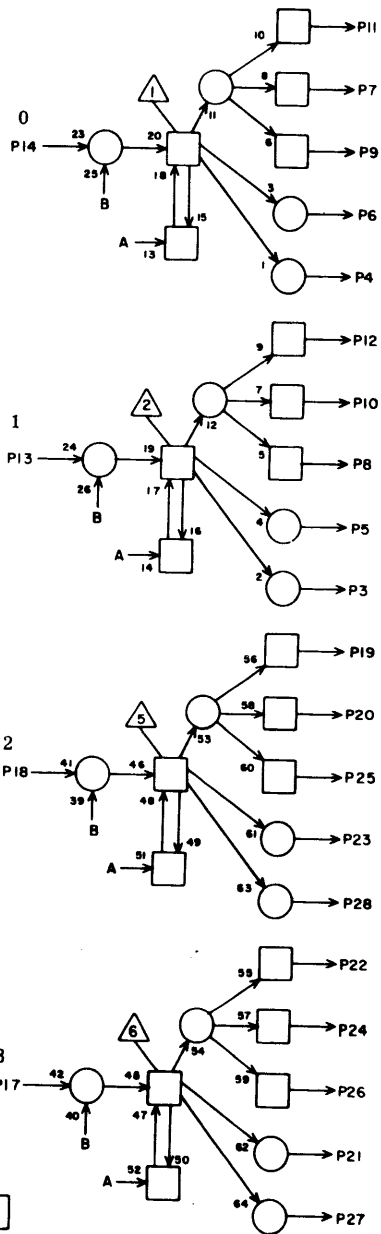
| | | |
|----|--------|---|
| 1 | - | |
| 2 | - | |
| 3 | C08-2 | 9 |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | - | |
| 8 | - | |
| 9 | B01-26 | 7 |
| 10 | - | |
| 11 | - | |
| 12 | - | |
| 13 | B05-22 | 5 |
| 14 | B06-11 | 5 |
| 15 | - | |
| 16 | - | |
| 17 | - | |
| 18 | B03-12 | 5 |
| 19 | - | |
| 20 | B02-6 | 7 |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | B02-5 | 5 |
| 25 | B03-3 | 5 |
| 26 | B04-X | 2 |
| 27 | B04-X | 2 |
| 28 | B04-X | 2 |

JACK PIN LG
CIRCUIT SPECIFICATION 1N27600
60227300 F

LS 63057900
ASSY

B
REV

SECTOR COUNTER - STACK 0
RANK 1, BITS 0-3



PD

RV G

805

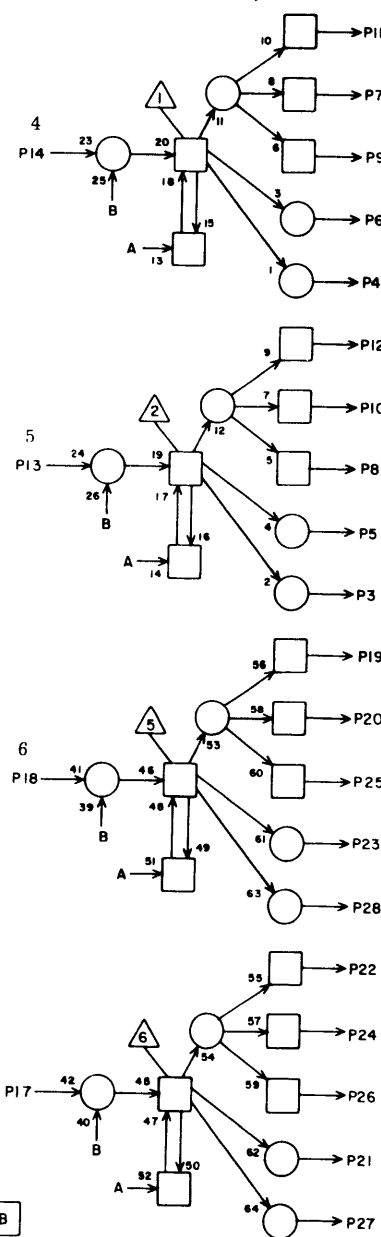
| | | |
|----|--------|----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | A07- 6 | 7 |
| 8 | H04- 5 | 23 |
| 9 | H04- 7 | 23 |
| 10 | A07- 5 | 9 |
| 11 | 803-13 | 5 |
| 12 | 803-14 | 5 |
| 13 | 801- 9 | 7 |
| 14 | 801-14 | 7 |
| 15 | - | |
| 16 | 808- 1 | 7 |
| 17 | 801-21 | 7 |
| 18 | 801-18 | 7 |
| 19 | 803-18 | 5 |
| 20 | A07- 7 | 9 |
| 21 | - | |
| 22 | 804-13 | 5 |
| 23 | - | |
| 24 | A07-22 | 7 |
| 25 | - | |
| 26 | - | |
| 27 | - | |
| 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63057900
ASSY

B
REV

SECTOR COUNTER - STACK 0
RANK 1, BITS 4-6



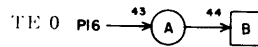
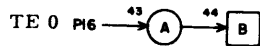
PD

RV G

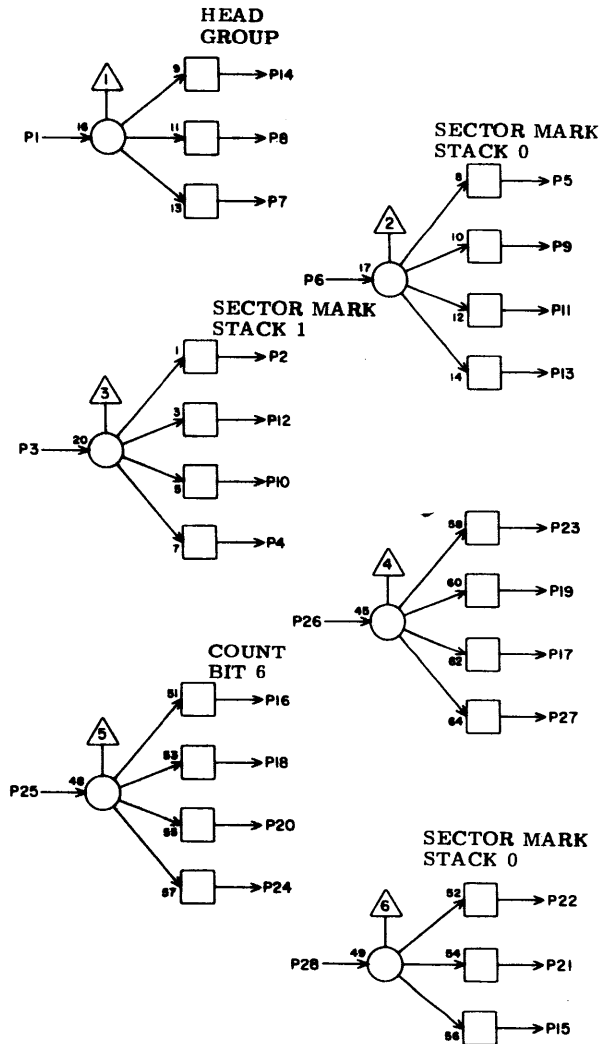
806

| | | |
|----|--------|----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | A07-24 | 5 |
| 8 | H04- 3 | 23 |
| 9 | - | |
| 10 | A07-23 | 7 |
| 11 | 804-14 | 5 |
| 12 | 804-18 | 5 |
| 13 | 802- 9 | 7 |
| 14 | 802-14 | 7 |
| 15 | - | |
| 16 | 808- 3 | 7 |
| 17 | - | |
| 18 | 802-18 | 7 |
| 19 | 802-20 | 11 |
| 20 | A09-28 | 7 |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | - | |
| 25 | H04- 1 | 21 |
| 26 | - | |
| 27 | - | |
| 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F



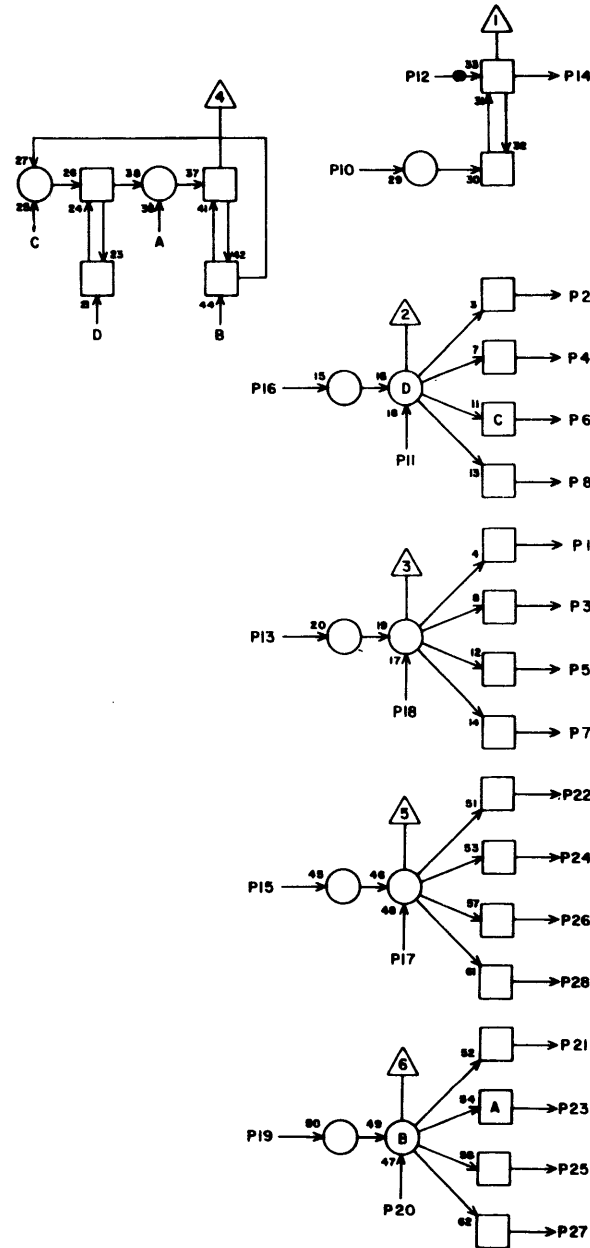
LS 63064000
ASSY REV



| TH | RV | G | B07 |
|----|--------|-----|-----|
| 1 | G07-25 | 21 | |
| 2 | B08-17 | 5 | |
| 3 | K02-25 | 35 | |
| 4 | - | | |
| 5 | B08-11 | 5 | |
| 6 | K02- 6 | 35 | |
| 7 | G04-24 | 23 | |
| 8 | E13-24 | 17 | |
| 9 | B07-28 | 120 | |
| 10 | B08-19 | 5 | |
| 11 | B08-13 | 5 | |
| 12 | B07-26 | 120 | |
| 13 | - | | |
| 14 | E13- 1 | 15 | |
| 15 | - | | |
| 16 | A09- 5 | 9 | |
| 17 | - | | |
| 18 | I12-26 | 29 | |
| 19 | B08-20 | 5 | |
| 20 | I15-26 | 31 | |
| 21 | B08-18 | 5 | |
| 22 | B08-16 | 5 | |
| 23 | B08-15 | 5 | |
| 24 | - | | |
| 25 | D02-19 | 11 | |
| 26 | B07-12 | 120 | |
| 27 | - | | |
| 28 | B07- 9 | 120 | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827000
60227300 F

LS 63046200
ASSY REV



| HQ | RV | G | B08 |
|----|--------|----|-----|
| 1 | B05-16 | 7 | |
| 2 | B01-22 | 11 | |
| 3 | B06-16 | 7 | |
| 4 | B01-11 | 11 | |
| 5 | - | | |
| 6 | D02-23 | 13 | |
| 7 | - | | |
| 8 | F09-26 | 19 | |
| 9 | - | | |
| 10 | - | | |
| 11 | B07- 5 | 5 | |
| 12 | - | | |
| 13 | B07-11 | 5 | |
| 14 | - | | |
| 15 | B07-23 | 5 | |
| 16 | B07-22 | 5 | |
| 17 | B07- 2 | 5 | |
| 18 | B07-21 | 5 | |
| 19 | B07-10 | 5 | |
| 20 | B07-19 | 5 | |
| 21 | A05-16 | 9 | |
| 22 | A01-22 | 13 | |
| 23 | A06-16 | 9 | |
| 24 | A01-11 | 13 | |
| 25 | - | | |
| 26 | D02-25 | 13 | |
| 27 | - | | |
| 28 | F01-28 | 21 | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827000
60227300 F

LS 63064000
ASSY

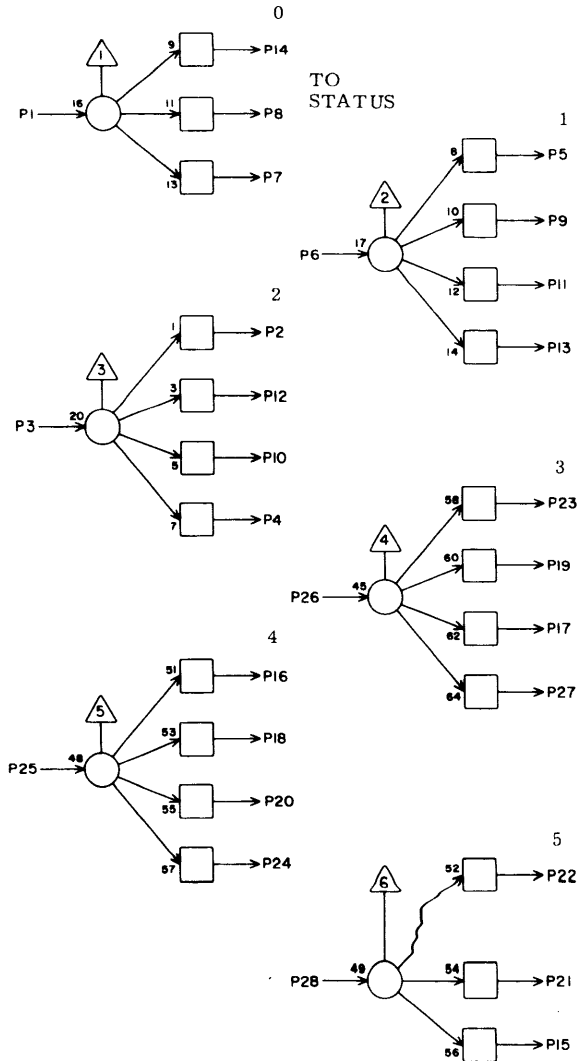


TH

RV G

809

SECTOR
COUNT



| TH | RV | G | 809 |
|----|--------|----|-----|
| 1 | A07-9 | 7 | |
| 2 | A08-1 | 7 | |
| 3 | A07-10 | 7 | |
| 4 | - | | |
| 5 | A08-18 | 7 | |
| 6 | A07-8 | 7 | |
| 7 | I14-4 | 27 | |
| 8 | I11-4 | 27 | |
| 9 | I11-3 | 27 | |
| 10 | I14-26 | 29 | |
| 11 | I14-3 | 27 | |
| 12 | I11-26 | 27 | |
| 13 | - | | |
| 14 | A08-5 | 7 | |
| 15 | I15-3 | 27 | |
| 16 | A08-13 | 7 | |
| 17 | I14-25 | 29 | |
| 18 | I12-4 | 27 | |
| 19 | I11-25 | 27 | |
| 20 | I15-4 | 27 | |
| 21 | I12-3 | 25 | |
| 22 | A08-24 | 7 | |
| 23 | A08-28 | 7 | |
| 24 | - | | |
| 25 | A07-21 | 7 | |
| 26 | A07-19 | 7 | |
| 27 | - | | |
| 28 | A07-20 | 9 | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600

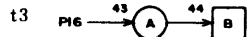
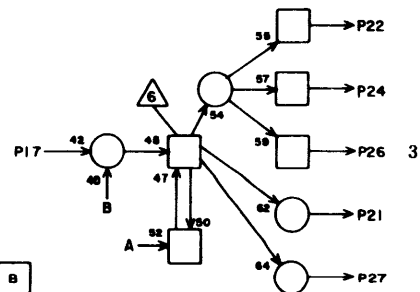
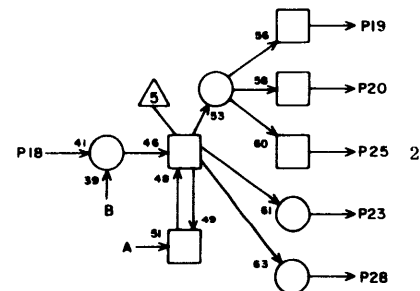
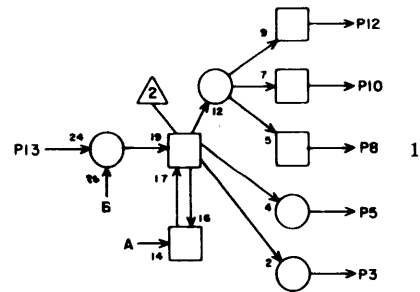
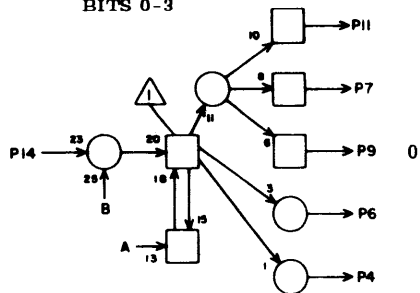
60227300 F

LS 63037900

ASSY



CELL
COUNTER
BITS 0-3



PP

RV 6

C11

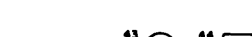
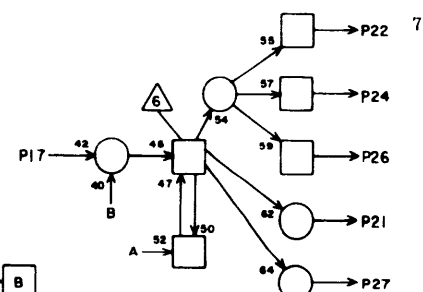
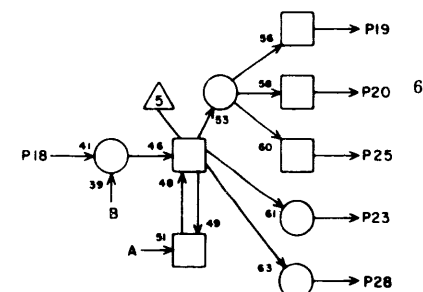
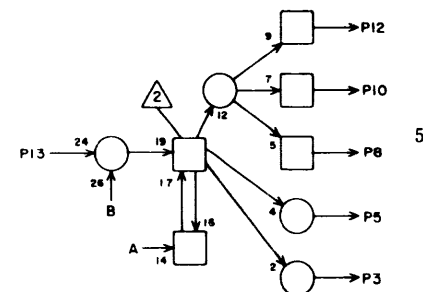
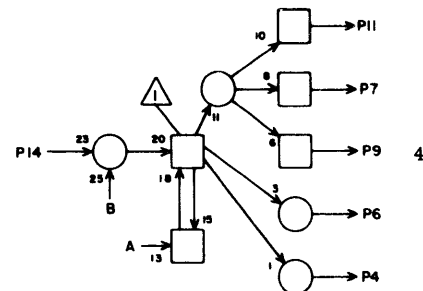
| | | |
|----|--------|----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | - | |
| 8 | - | |
| 9 | F07-25 | 15 |
| 10 | C09-20 | 7 |
| 11 | C15-5 | 7 |
| 12 | C15-6 | 7 |
| 13 | C13-24 | 5 |
| 14 | C13-9 | 7 |
| 15 | - | |
| 16 | E06-16 | 13 |
| 17 | C14-9 | 7 |
| 18 | C13-21 | 5 |
| 19 | C15-25 | 7 |
| 20 | C09-26 | 5 |
| 21 | - | |
| 22 | C15-26 | 7 |
| 23 | - | |
| 24 | - | |
| 25 | - | |
| 26 | - | |
| 27 | - | |
| 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63057900
ASSY



CELL
COUNTER
BITS 4-7



PD

RV 6

C12

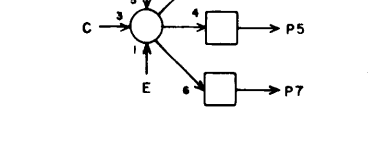
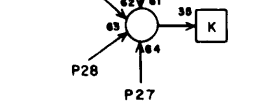
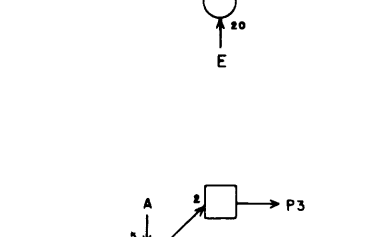
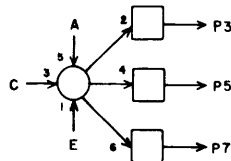
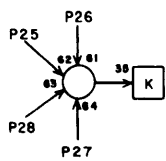
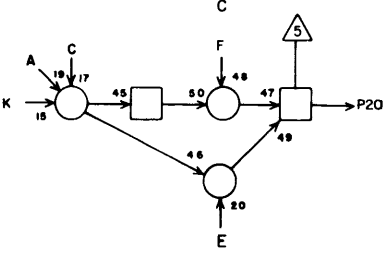
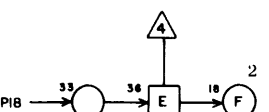
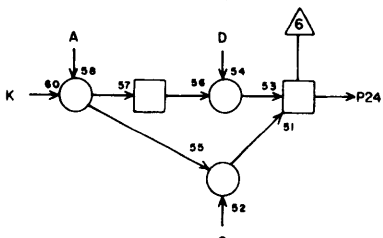
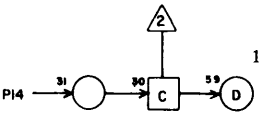
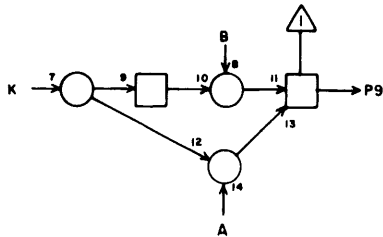
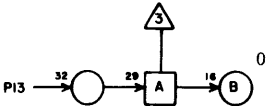
| | | |
|----|--------|----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | C09-21 | 7 |
| 8 | G08-6 | 17 |
| 9 | G08-8 | 19 |
| 10 | - | |
| 11 | C16-5 | 7 |
| 12 | C16-6 | 7 |
| 13 | C14-20 | 5 |
| 14 | C14-24 | 5 |
| 15 | - | |
| 16 | E06-18 | 13 |
| 17 | - | |
| 18 | A09-14 | 11 |
| 19 | C16-25 | 7 |
| 20 | C09-23 | 7 |
| 21 | - | |
| 22 | - | |
| 23 | E09-24 | 11 |
| 24 | - | |
| 25 | C09-24 | 7 |
| 26 | - | |
| 27 | - | |
| 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63061000
ASSY 3
REV

CELL COUNTER
(BIT COUNTER)
BITS 0-2

OK RV G C13



| OK | RV | G | C13 |
|----|--------|---|-----|
| 1 | - | - | |
| 2 | - | - | |
| 3 | C14-25 | 5 | |
| 4 | - | - | |
| 5 | C08- 1 | 9 | |
| 6 | - | - | |
| 7 | - | - | |
| 8 | - | - | |
| 9 | C11-14 | 7 | |
| 10 | - | - | |
| 11 | - | - | |
| 12 | - | - | |
| 13 | C15-14 | 5 | |
| 14 | C15- 9 | 7 | |
| 15 | - | - | |
| 16 | - | - | |
| 17 | - | - | |
| 18 | C15-18 | 5 | |
| 19 | - | - | |
| 20 | C11-18 | 5 | |
| 21 | - | - | |
| 22 | - | - | |
| 23 | - | - | |
| 24 | C11-13 | 5 | |
| 25 | C13- X | 2 | |
| 26 | C13- X | 2 | |
| 27 | C13- X | 2 | |
| 28 | C13- X | 2 | |

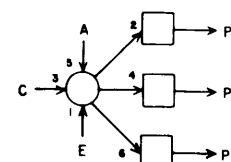
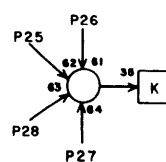
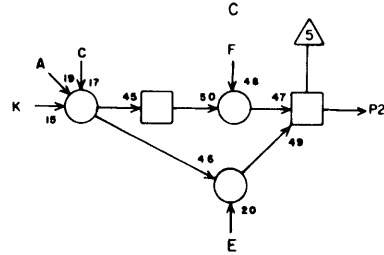
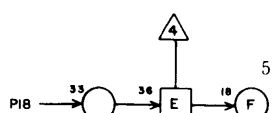
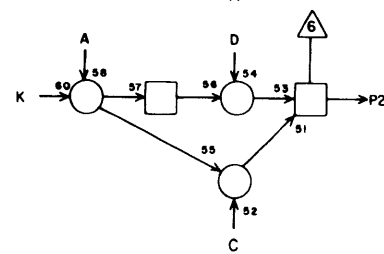
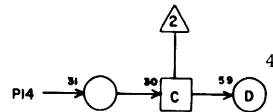
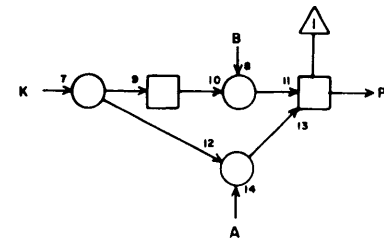
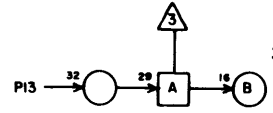
JACK PIN LG
CIRCUIT SPECIFICATION 11827600

60227300 F

LS 63061000
ASSY 3
REV

CELL COUNTER
(BIT COUNTER)
BITS 3-5

OK RV G C14



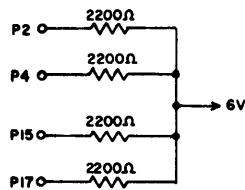
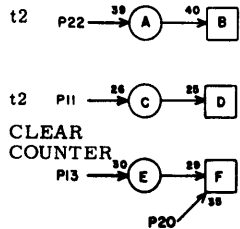
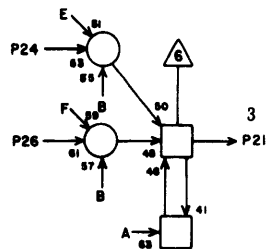
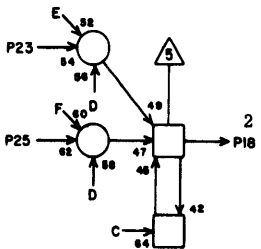
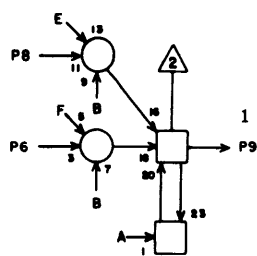
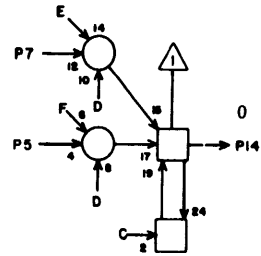
| OK | RV | G | C14 |
|----|--------|---|-----|
| 1 | - | - | |
| 2 | - | - | |
| 3 | C08- 3 | 9 | |
| 4 | - | - | |
| 5 | - | - | |
| 6 | - | - | |
| 7 | - | - | |
| 8 | - | - | |
| 9 | C11-17 | 7 | |
| 10 | - | - | |
| 11 | - | - | |
| 12 | - | - | |
| 13 | C15-21 | 5 | |
| 14 | C16-14 | 5 | |
| 15 | - | - | |
| 16 | - | - | |
| 17 | - | - | |
| 18 | C16- 9 | 7 | |
| 19 | - | - | |
| 20 | C12-13 | 5 | |
| 21 | - | - | |
| 22 | - | - | |
| 23 | - | - | |
| 24 | C12-14 | 5 | |
| 25 | C13- 3 | 5 | |
| 26 | C14- X | 2 | |
| 27 | C14- X | 2 | |
| 28 | C14- X | 2 | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63057600
ASSY **C**
REV

CELL COUNTER
BITS 0-3

| PC | RV | G | C15 |
|----|----|--------|-----|
| | 1 | - | |
| | 2 | I11-12 | 25 |
| | 3 | - | |
| | 4 | I12-12 | 25 |
| | 5 | C11-11 | 7 |
| | 6 | C11-12 | 7 |
| | 7 | C15- X | 2 |
| | 8 | C15- X | 2 |
| | 9 | C13-14 | 7 |
| | 10 | - | |
| | 11 | E06-13 | 15 |
| | 12 | - | |
| | 13 | D12-16 | 9 |
| | 14 | C13-13 | 5 |
| | 15 | I13-12 | 23 |
| | 16 | - | |
| | 17 | I14-12 | 23 |
| | 18 | C13-18 | 5 |
| | 19 | - | |
| | 20 | C15- X | 2 |
| | 21 | C14-13 | 5 |
| | 22 | E06-11 | 15 |
| | 23 | C15- X | 2 |
| | 24 | C15- X | 2 |
| | 25 | C11-19 | 7 |
| | 26 | C11-22 | 7 |
| | 27 | - | |
| | 28 | - | |

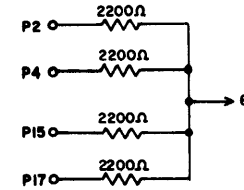
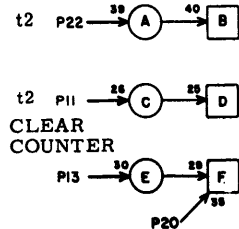
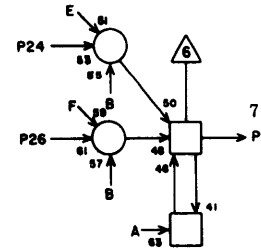
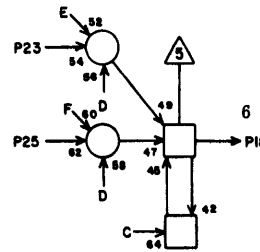
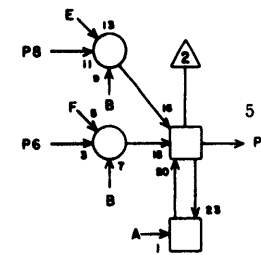
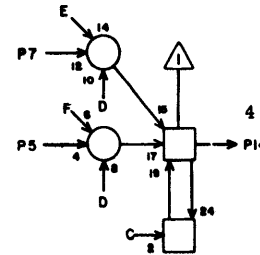


JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63057600
ASSY **C**
REV

CELL COUNTER
BITS 4-7

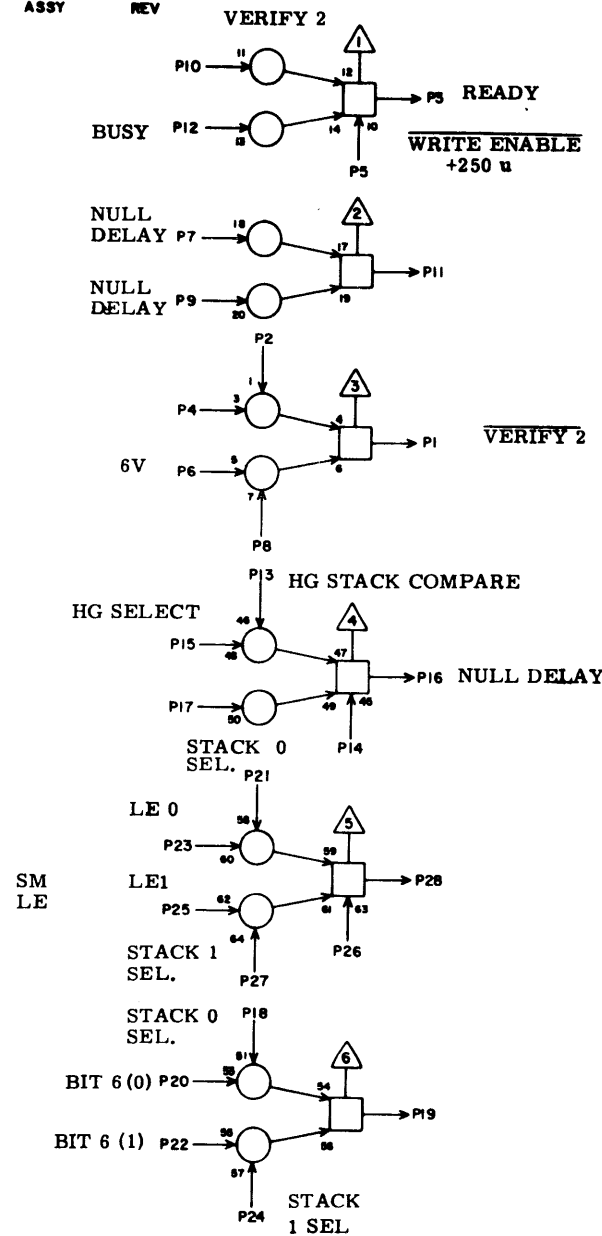
| PC | RV | G | C16 |
|----|----|--------|-----|
| | 1 | - | |
| | 2 | I15-12 | 23 |
| | 3 | - | |
| | 4 | I16-12 | 23 |
| | 5 | C12-11 | 7 |
| | 6 | C12-12 | 7 |
| | 7 | C16- X | 2 |
| | 8 | C16- X | 2 |
| | 9 | C14-18 | 7 |
| | 10 | - | |
| | 11 | E06-10 | 17 |
| | 12 | - | |
| | 13 | D12-14 | 9 |
| | 14 | C14-14 | 5 |
| | 15 | I09- 9 | 25 |
| | 16 | - | |
| | 17 | H13-22 | 19 |
| | 18 | A09-13 | 13 |
| | 19 | - | |
| | 20 | C16- X | 2 |
| | 21 | - | |
| | 22 | E06- 8 | 15 |
| | 23 | C16- X | 2 |
| | 24 | - | |
| | 25 | C12-19 | 7 |
| | 26 | - | |
| | 27 | - | |
| | 28 | - | |



JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 H

LS 63080700
ASSY

REV



QH RV G D02

| | | |
|----|--------|----|
| 1 | D07-12 | 9 |
| 2 | D07-1 | 9 |
| *3 | - | |
| 3 | D03-6 | 3 |
| 4 | F07-19 | 13 |
| 5 | D09-24 | 11 |
| 6 | C02-17 | 5 |
| 7 | D08-28 | 9 |
| 8 | D02-X | 2 |
| 9 | F04-21 | 11 |
| 10 | D02-X | 2 |
| 11 | D08-21 | 9 |
| 12 | E09-28 | 13 |
| 13 | A10-2 | 17 |
| 14 | D02-X | 2 |
| 15 | A10-3 | 17 |
| 16 | F04-28 | 11 |
| 17 | D08-3 | 11 |
| 18 | G06-23 | 15 |
| 19 | B07-25 | 11 |
| 20 | B06-19 | 11 |
| 21 | G06-28 | 15 |
| 22 | A06-19 | 15 |
| 23 | B08-6 | 13 |
| 24 | G06-28 | 15 |
| 25 | B08-26 | 13 |
| 26 | D02-X | 2 |
| 27 | G06-25 | 15 |
| 28 | C09-6 | 13 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827800

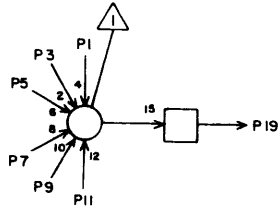
*Standard Option 10037

60227300 G



BUSY

POSITION

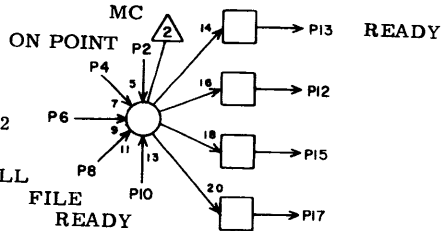


MC ON POINT

SECTOR VERIFY 2

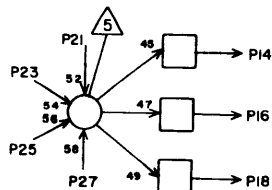
NULL FILE

READY



INDEX

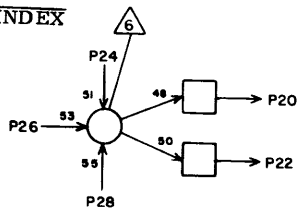
143₈



PRESET SECTOR COUNT 0

INDEX

143₈



PRESET SECTOR COUNT 1

TB

V G 003

| | | |
|----|--------|----|
| 1 | E03-25 | 9 |
| 2 | F04-16 | 11 |
| 3 | G03- 5 | 13 |
| 4 | E01-21 | 9 |
| 5 | E01-15 | 9 |
| *6 | J08-27 | 27 |
| 6 | D02- 3 | 3 |
| 7 | G13-18 | 19 |
| 8 | G13-16 | 19 |
| 9 | D03- X | 2 |
| 10 | K01- 4 | 27 |
| 11 | D03- X | 2 |
| 12 | E12-25 | 15 |
| 13 | G04-25 | 15 |
| 14 | H01-13 | 11 |
| 15 | - | - |
| 16 | H02-13 | 11 |
| 17 | F07-23 | 13 |
| 18 | - | - |
| 19 | D08-12 | 9 |
| 20 | A01-13 | 13 |
| 21 | K02- 3 | 25 |
| 22 | A02-13 | 13 |
| 23 | H04-13 | 15 |
| 24 | K02-18 | 25 |
| 25 | D03- X | 2 |
| 26 | H04- 9 | 15 |
| 27 | D03- X | 2 |
| 28 | D03- X | 2 |

JACK PIN LG

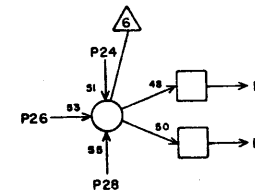
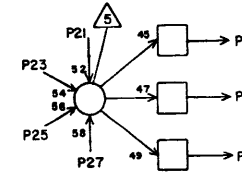
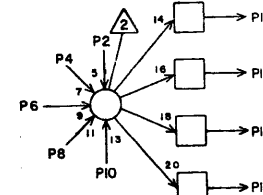
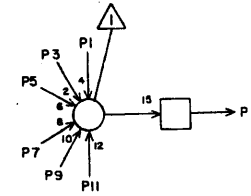
CIRCUIT SPECIFICATION 11827600
60227300 G



TB

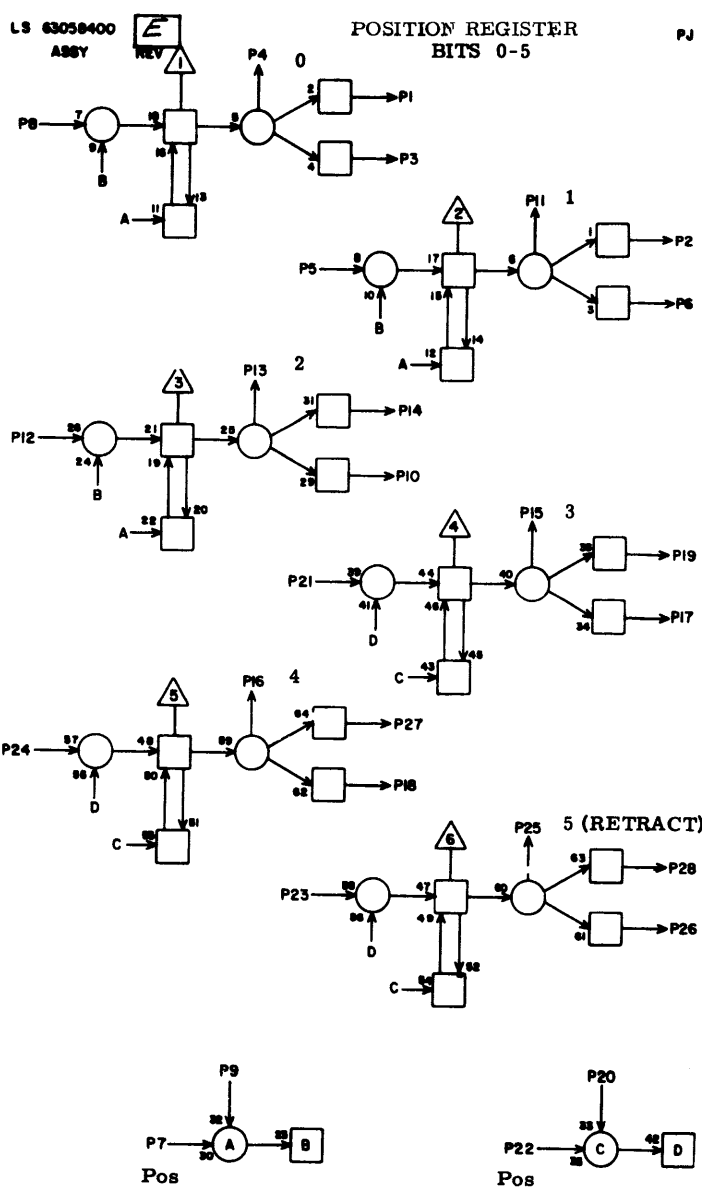
RV

1D04



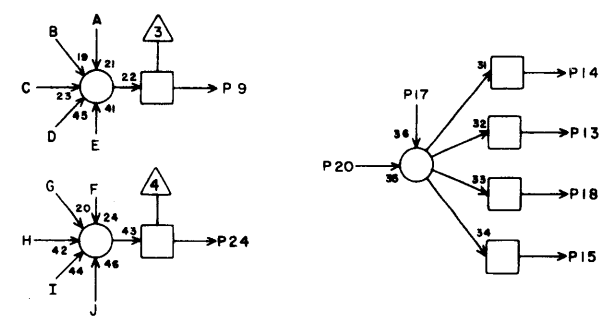
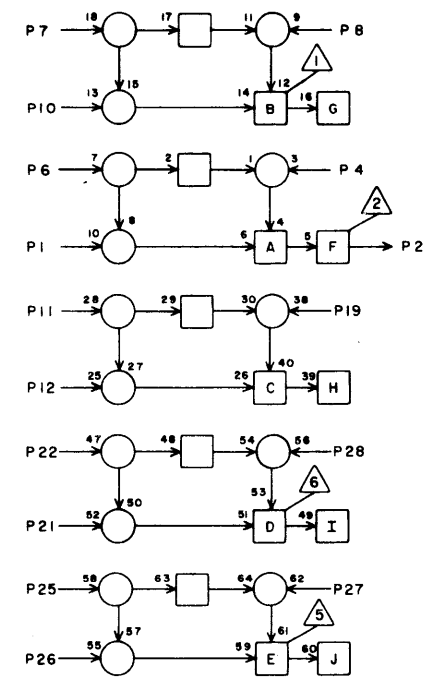
| | | |
|----|--------|-----|
| 1 | D06-14 | 5 |
| 2 | E02-10 | 9 |
| 3 | D07- 8 | 7 |
| 4 | E01-19 | 7 |
| 5 | D04- X | 2 |
| 6 | E03- 4 | 7 |
| 7 | D04- X | 2 |
| 8 | E02-28 | 9 |
| 9 | D04- X | 2 |
| 10 | D04- X | 2 |
| 11 | D04- X | 2 |
| 12 | E01-25 | 121 |
| 13 | E02-16 | 120 |
| 14 | C01-13 | 7 |
| 15 | D07- 7 | 7 |
| 16 | C02-13 | 7 |
| 17 | D07-14 | 7 |
| 18 | E02-17 | 120 |
| 19 | D07-11 | 7 |
| 20 | - | - |
| 21 | E02-19 | 7 |
| 22 | - | - |
| 23 | E03- 6 | 5 |
| 24 | E01-11 | 7 |
| 25 | E01- 9 | 7 |
| 26 | E02-26 | 7 |
| 27 | E02- 1 | 5 |
| 28 | E03- 5 | 5 |

60227300 G



| PJ | RV | G | D05 |
|----|----|--------|-----|
| | 1 | I11- 8 | 23 |
| | 2 | I11- 7 | 23 |
| | 3 | I14- 8 | 25 |
| | 4 | C07- 6 | 7 |
| | 5 | H10- 5 | 19 |
| | 6 | I14- 7 | 25 |
| | 7 | G11-17 | 17 |
| | 8 | H10- 6 | 19 |
| | 9 | C10- 6 | 9 |
| | 10 | I14-22 | 25 |
| | 11 | C07- 5 | 7 |
| | 12 | H10-26 | 21 |
| | 13 | C07- 7 | 7 |
| | 14 | I11-22 | 23 |
| | 15 | C07-22 | 7 |
| | 16 | C07-24 | 7 |
| | 17 | I14-21 | 25 |
| | 18 | I15- 8 | 23 |
| | 19 | I11-21 | 23 |
| | 20 | C10- 8 | 11 |
| | 21 | H10-25 | 19 |
| | 22 | G11-19 | 15 |
| | 23 | H11- 5 | 17 |
| | 24 | F09-24 | 11 |
| | 25 | - | - |
| | 26 | I15- 7 | 23 |
| | 27 | I12- 8 | 21 |
| | 28 | I12- 7 | 21 |

LS 63051500 ASSY D REV

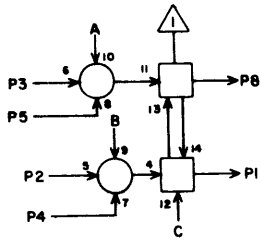


| JR | RV | D06 | 1006 |
|----|----|--------|------|
| | 1 | - | |
| | 2 | - | |
| | 3 | - | |
| | 4 | - | |
| | 5 | - | |
| | 6 | C07- 8 | 7 |
| | 7 | C07- 9 | 7 |
| | 8 | - | |
| | 9 | D06-17 | 5 |
| | 10 | - | |
| | 11 | C07-10 | 7 |
| | 12 | - | |
| | 13 | D07- 3 | 5 |
| | 14 | D04- 1 | 5 |
| | 15 | F07-21 | 11 |
| | 16 | - | |
| | 17 | D06- 9 | 5 |
| | 18 | F07-22 | 11 |
| | 19 | - | |
| | 20 | - | |
| | 21 | - | |
| | 22 | C07-19 | 7 |
| | 23 | - | |
| | 24 | - | |
| | 25 | C07-21 | 7 |
| | 26 | - | |
| | 27 | - | |
| | 28 | - | |

LS 63040400
ASSY

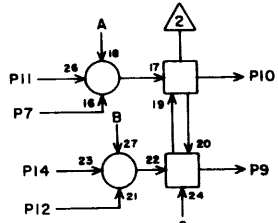
C
REV

GATE 1



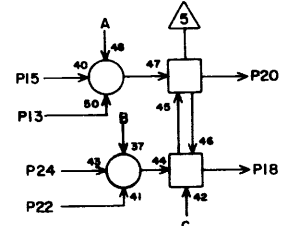
VERIFY 1

GATE 2

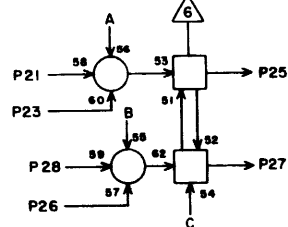


VERIFY 2

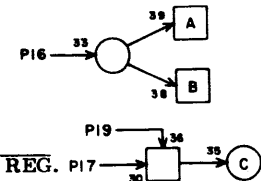
GATE 2



HG PULSE



HG & 30 MS



LOAD POS. REG.

AE

| RV | 1007 | |
|----|--------|-----|
| 1 | D02- 2 | 9 |
| 2 | E01-18 | 121 |
| 3 | D06-13 | 5 |
| 4 | F07-14 | 11 |
| 5 | E01-16 | 121 |
| 6 | - | |
| 7 | D04-15 | 7 |
| 8 | D04- 3 | 7 |
| 9 | - | |
| 10 | - | |
| 11 | D04-19 | 7 |
| 12 | D02- 1 | 9 |
| 13 | - | |
| 14 | D04-17 | 7 |
| 15 | - | |
| 16 | D07- X | 2 |
| 17 | G11-15 | 15 |
| 18 | - | |
| 19 | D07- X | 2 |
| 20 | - | |
| 21 | C08-17 | 7 |
| 22 | - | |
| 23 | D07- X | 2 |
| 24 | - | |
| 25 | D09- 5 | 7 |
| 26 | D07- X | 2 |
| 27 | J08-26 | 23 |
| 28 | D09-10 | 7 |

JACK PIN LG

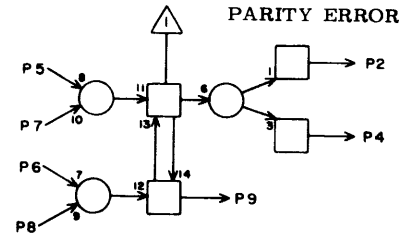
CIRCUIT SPECIFICATION 11827600
60227300 G

LS 63040000
ASSY

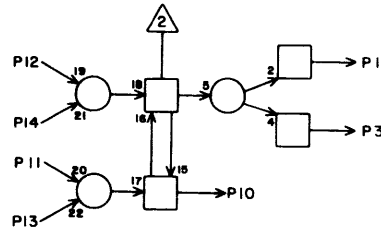
D
REV

AA

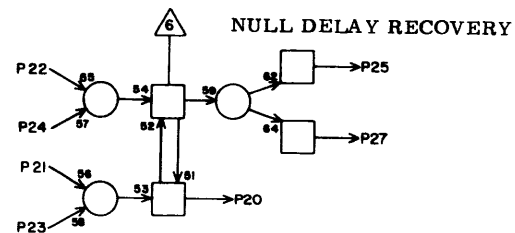
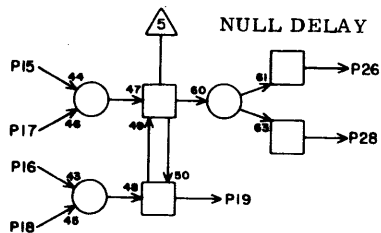
RV G D08



POSITION



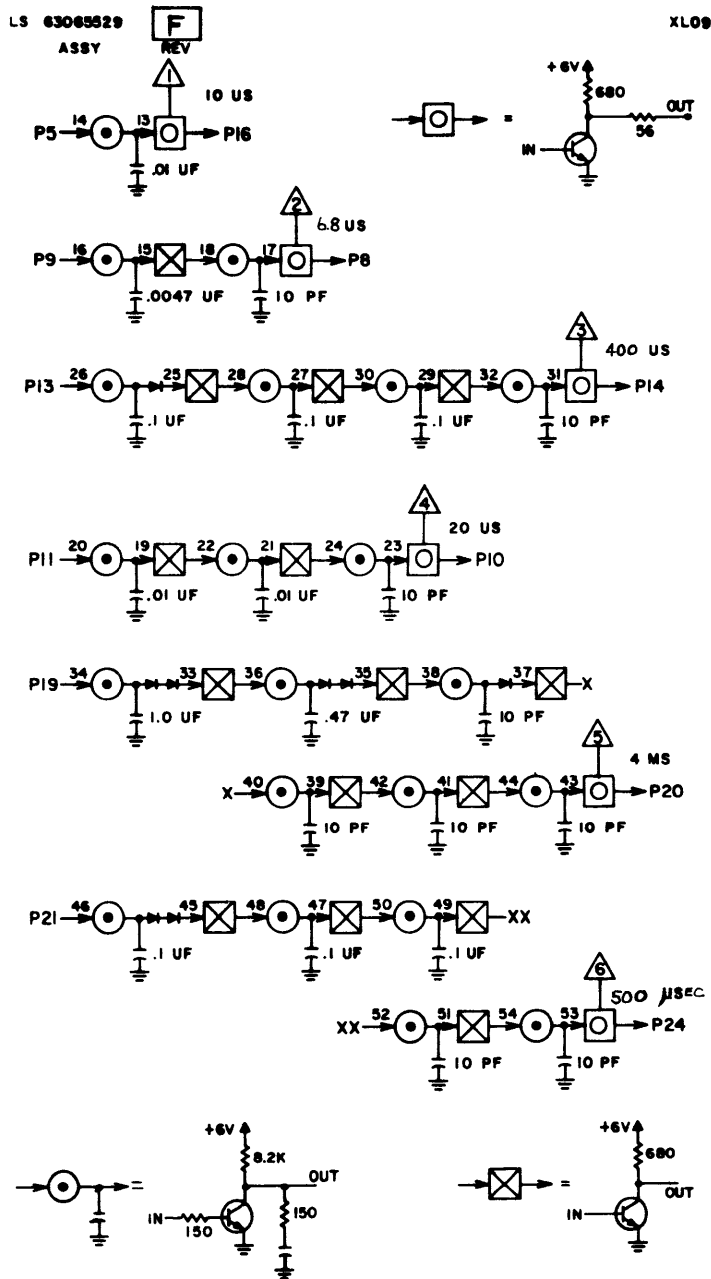
POS. SEL



| | | |
|----|--------|----|
| 1 | G06-14 | 15 |
| 2 | I13- 4 | 23 |
| 3 | D02-17 | 11 |
| 4 | I16- 4 | 23 |
| 5 | G01-11 | 17 |
| 6 | K09-18 | 27 |
| 7 | D08- X | 2 |
| 8 | D08- X | 2 |
| 9 | - | |
| 10 | - | |
| 11 | G05- 9 | 13 |
| 12 | D03-19 | 9 |
| 13 | D08- X | 2 |
| 14 | E04-24 | 9 |
| 15 | D09-20 | 5 |
| 16 | D08- X | 2 |
| 17 | D08-27 | 5 |
| 18 | F04-22 | 11 |
| 19 | D08-24 | 5 |
| 20 | D09-13 | 5 |
| 21 | D02-11 | 9 |
| 22 | D09-14 | 5 |
| 23 | D08- X | 2 |
| 24 | D08-19 | 5 |
| 25 | D09-19 | 5 |
| 26 | G13-25 | 15 |
| 27 | D08-17 | 5 |
| 28 | D02- 7 | 9 |

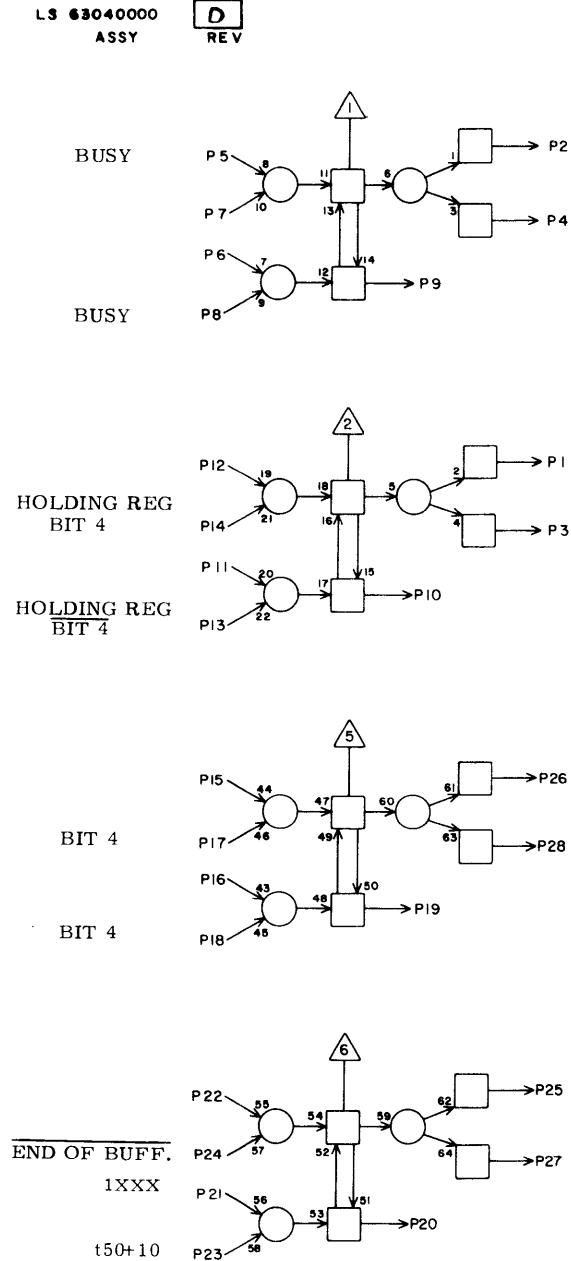
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60227300 F



| RV | G | D09 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | D07-25 | 7 |
| 6 | - | |
| 7 | - | |
| 8 | D12-26 | 7 |
| 9 | F10-2 | 9 |
| 10 | D07-28 | 7 |
| 11 | D09-16 | 5 |
| 12 | - | |
| 13 | D08-20 | 5 |
| 14 | D08-22 | 5 |
| 15 | - | |
| 16 | D09-11 | 5 |
| 17 | - | |
| 18 | - | |
| 19 | D08-25 | 5 |
| 20 | D08-15 | 5 |
| 21 | F01-5 | 13 |
| 22 | - | |
| 23 | - | |
| 24 | D02-5 | 11 |
| 25 | - | |
| 26 | - | |
| 27 | - | |
| 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION
11827600
60227300 F



END OF BUFF.
1XXX
t50+10

| AA | RV | G | D18 |
|----|----|--------|-----|
| | 1 | C07-23 | 7 |
| | 2 | C10-26 | 5 |
| | 3 | - | |
| | 4 | - | |
| | 5 | E03-21 | 13 |
| | 6 | I09-1 | 19 |
| | 7 | I18-1 | 19 |
| | 8 | E03-23 | 13 |
| | 9 | C10-1 | 7 |
| | 10 | - | |
| | 11 | E13-22 | 9 |
| | 12 | E13-20 | 9 |
| | 13 | H11-9 | 15 |
| | 14 | F09-22 | 11 |
| | 15 | G04-20 | 17 |
| | 16 | G04-22 | 17 |
| | 17 | F09-21 | 11 |
| | 18 | H11-11 | 15 |
| | 19 | - | |
| | 20 | - | |
| | 21 | J02-20 | 27 |
| | 22 | G01-28 | 19 |
| | 23 | J02-13 | 25 |
| | 24 | H05-19 | 19 |
| | 25 | F08-22 | 11 |
| | 26 | C07-25 | 7 |
| | 27 | - | |
| | 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

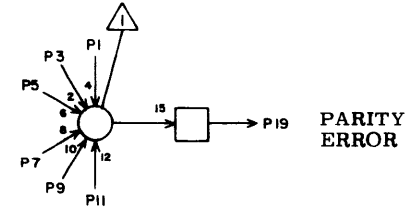
LS 63063400
ASSY



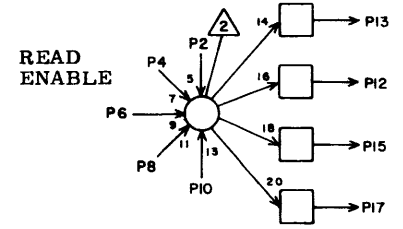
REV

TB

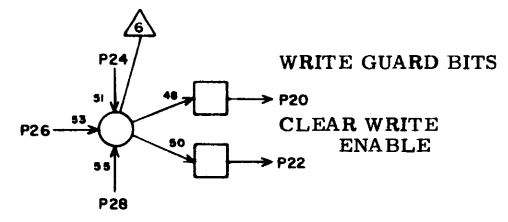
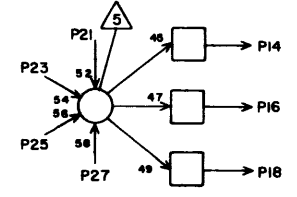
RV 6 012



SELECT READ CLOCK



CLEAR COUNTER



| | | |
|----|--------|-----|
| 1 | E12-17 | 7 |
| 2 | E09-10 | 9 |
| 3 | F07-11 | 13 |
| 4 | E08-27 | 11 |
| 5 | G13-19 | 15 |
| 6 | D12- X | 2 |
| 7 | D12- X | 2 |
| 8 | D12- X | 2 |
| 9 | D12- X | 2 |
| 10 | D12- X | 2 |
| 11 | D12- X | 2 |
| 12 | G01- 2 | 19 |
| 13 | E09- 8 | 9 |
| 14 | C16-13 | 9 |
| 15 | - | |
| 16 | G15-13 | 9 |
| 17 | - | |
| 18 | - | |
| 19 | G01- 7 | 19 |
| 20 | F10- 6 | 9 |
| 21 | E09-14 | 9 |
| 22 | G01-17 | 19 |
| 23 | E09-19 | 7 |
| 24 | D12- X | 2 |
| 25 | D12- X | 2 |
| 26 | D09- 8 | 7 |
| 27 | D12- X | 2 |
| 28 | F10- 4 | 120 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600

60227300 F

S 63064000
ASSY

REV

TH

RV 1E01

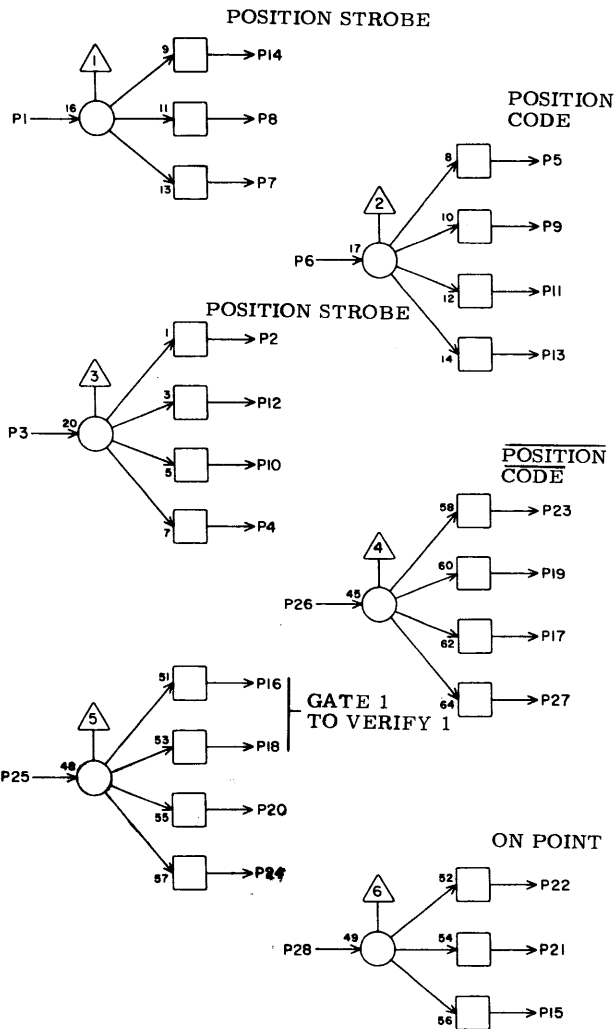
LS 63040000
ASSY

D
REV

AA

RV

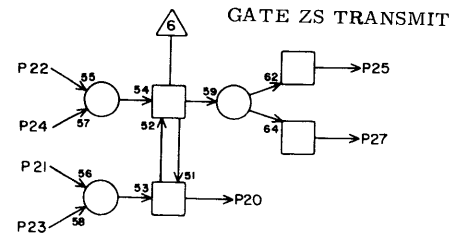
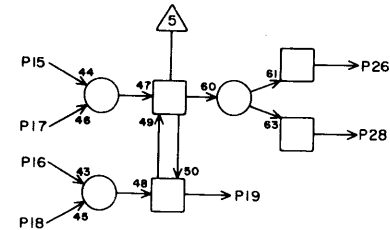
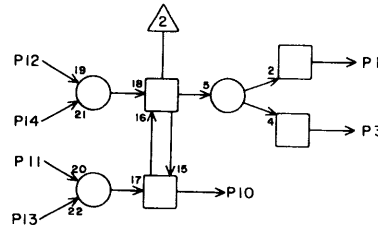
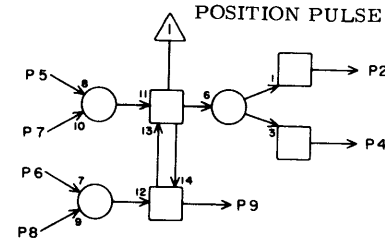
1E02



| | | |
|----|---------|-----|
| 1 | K01-25 | 23 |
| 2 | E03-16 | 7 |
| 3 | E01- 8 | 121 |
| 4 | | |
| 5 | E02-14 | 3 |
| 6 | K01- 6 | 23 |
| 7 | E03-13 | 5 |
| 8 | E01- 3 | 120 |
| 9 | D04-25 | 7 |
| 10 | - | |
| 11 | D04-24 | 7 |
| 12 | E03- 18 | 5 |
| 13 | - | |
| 14 | E03-11 | 5 |
| 15 | D03- 5 | 9 |
| 16 | D07- 5 | 120 |
| 17 | | |
| 18 | D07- 2 | 120 |
| 19 | D04- 4 | 9 |
| 20 | - | |
| 21 | D03- 4 | 9 |
| 22 | E13- 7 | 17 |
| 23 | E02-11 | 5 |
| 24 | - | |
| 25 | D04-12 | 120 |
| 26 | K01-13 | 21 |
| 27 | - | |
| 28 | K01-23 | 23 |

JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60227300 G



| | | |
|----|--------|-----|
| 1 | D04-27 | 7 |
| 2 | L05- 9 | 29 |
| 3 | - | |
| 4 | J07-23 | 23 |
| 5 | G05-11 | 11 |
| 6 | E02- X | 2 |
| 7 | E07- 9 | 9 |
| 8 | E05-18 | 7 |
| 9 | - | |
| 10 | D04- 2 | 9 |
| 11 | E01-23 | 5 |
| 12 | E03- 1 | 5 |
| 13 | E03- 3 | 5 |
| 14 | E01- 5 | 5 |
| 15 | F01-11 | 7 |
| 16 | D04-13 | 120 |
| 17 | D04-18 | 120 |
| 18 | E02- X | 2 |
| 19 | D04-21 | 7 |
| 20 | - | |
| 21 | E02- X | 2 |
| 22 | J07- 9 | 21 |
| 23 | F07-17 | 9 |
| 24 | F02- X | 2 |
| 25 | L01-18 | 25 |
| 26 | D04-26 | 7 |
| 27 | - | |
| 28 | D04- H | 9 |

JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60227300 G

LS 63048200
ASSY

D
REV

HQ

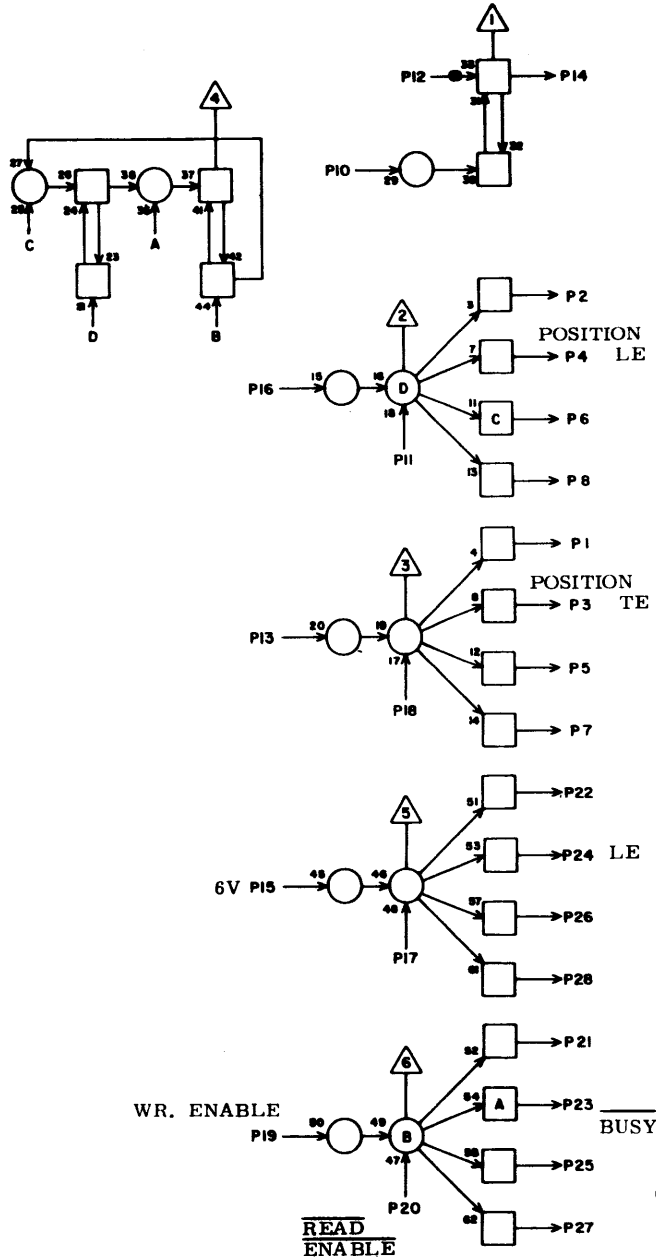
RV G E03

LS 63047000
ASSY

B
REV

HC

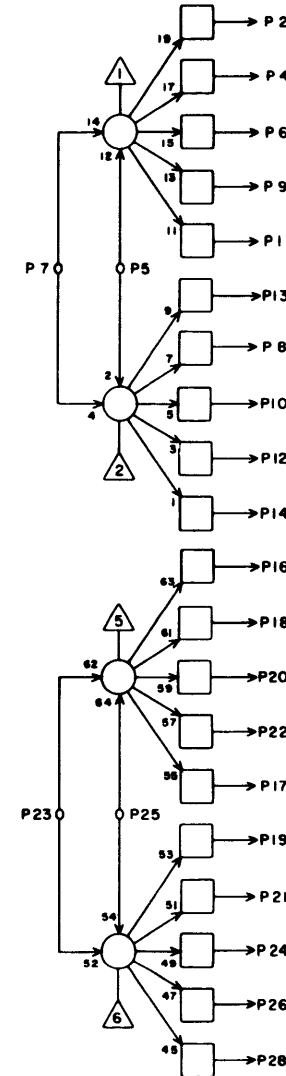
RV G E04



JACK PIN LG
CIRCUIT SPECIFICATION 11027600

60227300 G

| RV | G | E03 |
|----|--------|-----|
| 1 | E02-12 | 5 |
| 2 | - | |
| 3 | E02-13 | 5 |
| 4 | D04-6 | 7 |
| 5 | D04-28 | 5 |
| 6 | D04-23 | 5 |
| 7 | - | |
| 8 | E03-17 | 5 |
| 9 | - | |
| 10 | - | |
| 11 | E01-14 | 5 |
| 12 | - | |
| 13 | E01-7 | 5 |
| 14 | - | |
| 15 | C02-2 | 11 |
| 16 | E01-2 | 7 |
| 17 | E03-8 | 5 |
| 18 | E01-12 | 5 |
| 19 | F04-7 | 7 |
| 20 | E08-20 | 9 |
| 21 | D10-5 | 13 |
| 22 | C01-22 | 11 |
| 23 | D10-8 | 13 |
| 24 | C01-11 | 11 |
| 25 | D03-1 | 9 |
| 26 | C02-22 | 11 |
| 27 | F01-26 | 7 |
| 28 | C02-11 | 11 |

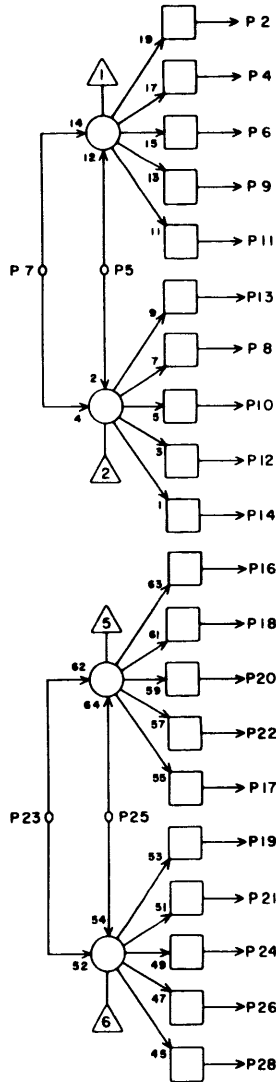


JACK PIN LG
CIRCUIT SPECIFICATION 11027600
60227300 F

| RV | G | E04 |
|----|--------|-----|
| 1 | - | |
| 2 | E07-23 | 7 |
| 3 | - | |
| 4 | H06-7 | 72 |
| 5 | F01-18 | 9 |
| 6 | H06-22 | 72 |
| 7 | F07-12 | 9 |
| 8 | F06-14 | 7 |
| 9 | H07-7 | 72 |
| 10 | F05-16 | 7 |
| 11 | H07-22 | 72 |
| 12 | E12-4 | 11 |
| 13 | - | |
| 14 | F10-17 | 11 |
| 15 | - | |
| 16 | A10-14 | 19 |
| 17 | G15-11 | 17 |
| 18 | G14-22 | 17 |
| 19 | G16-22 | 19 |
| 20 | G14-11 | 17 |
| 21 | G16-11 | 19 |
| 22 | G15-22 | 19 |
| 23 | F02-10 | 7 |
| 24 | D08-14 | 9 |
| 25 | F03-5 | 9 |
| 26 | F06-17 | 7 |
| 27 | - | |
| 28 | F05-7 | 9 |

LS 63044800
ASSY

B
REV



T3

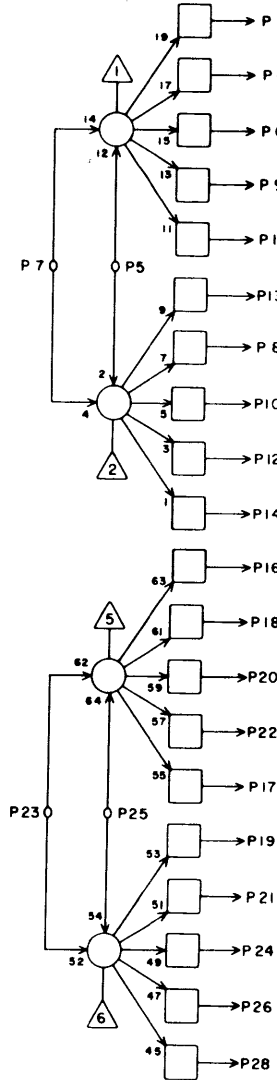
T4

| HC | RV | G | E05 |
|----|--------|----|-----|
| 1 | - | | |
| 2 | | | |
| 3 | - | | |
| 4 | E15-7 | 15 | |
| 5 | F03-23 | 9 | |
| 6 | E15-22 | 15 | |
| 7 | F02-20 | 9 | |
| 8 | E16-7 | 15 | |
| 9 | - | | |
| 10 | F06-13 | 7 | |
| 11 | E16-22 | 15 | |
| 12 | F06-23 | 9 | |
| 13 | G06-16 | 11 | |
| 14 | - | | |
| 15 | - | | |
| 16 | G05-16 | 9 | |
| 17 | F06-24 | 7 | |
| 18 | E02-8 | 7 | |
| 19 | F05-14 | 7 | |
| 20 | F06-8 | 7 | |
| 21 | - | | |
| 22 | F06-10 | 7 | |
| 23 | F02-24 | 9 | |
| 24 | E12-20 | 11 | |
| 25 | F03-21 | 7 | |
| 26 | F05-8 | 5 | |
| 27 | - | | |
| 28 | G08-10 | 9 | |

JACK PIN LG
CIRCUIT SPECIFICATION 11027600
60227300 G

LS 63044800
ASSY

B
REV



T2

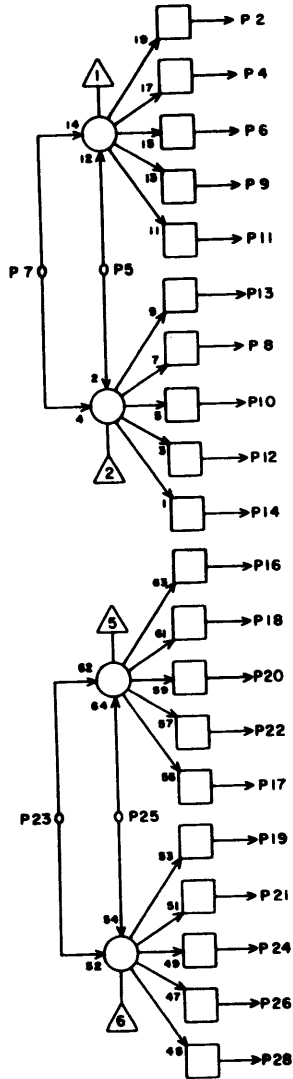
T3

| HC | RV | G | E06 |
|----|--------|----|-----|
| 1 | - | | |
| 2 | | | |
| 3 | - | | |
| 4 | E07-7 | 5 | |
| 5 | F03-3 | 7 | |
| 6 | E12-5 | 9 | |
| 7 | F02-8 | 9 | |
| 8 | C16-22 | 15 | |
| 9 | F10-24 | 9 | |
| 10 | C16-11 | 17 | |
| 11 | C15-22 | 15 | |
| 12 | - | | |
| 13 | C15-11 | 15 | |
| 14 | | | |
| 15 | - | | |
| 16 | C11-16 | 13 | |
| 17 | F05-17 | 7 | |
| 18 | C12-16 | 13 | |
| 19 | - | | |
| 20 | - | | |
| 21 | - | | |
| 22 | F05-13 | 7 | |
| 23 | F02-25 | 9 | |
| 24 | - | | |
| 25 | F03-20 | 9 | |
| 26 | - | | |
| 27 | - | | |
| 28 | - | | |

JACK PIN LG
CIRCUIT SPECIFICATION 11027600
60227300 G

LS 63044800
ASSY

B
REV



T2

T1

JACK PIN LG
CIRCUIT SPECIFICATION 11827000

60227300 F

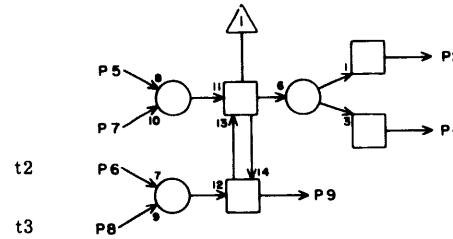
E07

| HC | RV | G | ASSY |
|----|----|--------|------|
| | 1 | - | |
| | 2 | - | |
| | 3 | - | |
| | 4 | E08-14 | 5 |
| | 5 | E07- X | 2 |
| | 6 | - | |
| | 7 | E06- 4 | 5 |
| | 8 | F06- 5 | 7 |
| | 9 | E02- 7 | 9 |
| | 10 | - | |
| | 11 | E08- 6 | 5 |
| | 12 | - | |
| | 13 | - | |
| | 14 | G12-12 | 11 |
| | 15 | - | |
| | 16 | J03-15 | 21 |
| | 17 | - | |
| | 18 | J04-15 | 21 |
| | 19 | - | |
| | 20 | J05-15 | 21 |
| | 21 | - | |
| | 22 | - | |
| | 23 | E04- 2 | 7 |
| | 24 | - | |
| | 25 | E07- X | 2 |
| | 26 | - | |
| | 27 | - | |
| | 28 | - | |

LS 63040000
ASSY

D
REV

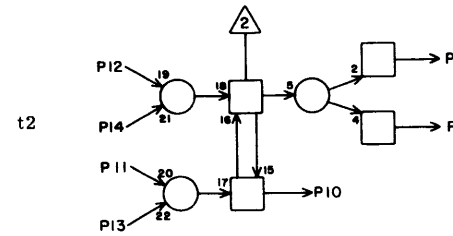
SECTOR SYNC I



t2

t3

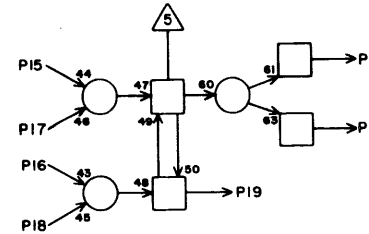
ERASE GAP



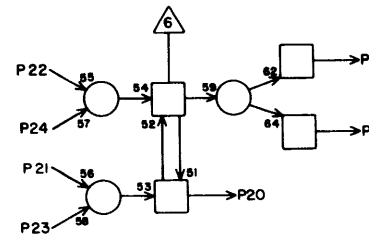
t2

t4

READ SYNC



READ ENABLE



AA

| RV | G | E08 |
|----|--------|-----|
| 1 | C10- 4 | 11 |
| 2 | F06-12 | 9 |
| 3 | E08-15 | 9 |
| 4 | - | |
| 5 | C09-13 | 9 |
| 6 | E07-11 | 5 |
| 7 | E08- X | 2 |
| 8 | E09-13 | 5 |
| 9 | F06-11 | 7 |
| 10 | - | |
| 11 | E08-26 | 5 |
| 12 | E12-14 | 7 |
| 13 | E08- X | 2 |
| 14 | E07- 4 | 5 |
| 15 | E08- 3 | 5 |
| 16 | F08-28 | 7 |
| 17 | E12-28 | 7 |
| 18 | E08- X | 2 |
| 19 | E09- 4 | 5 |
| 20 | E03-28 | 9 |
| 21 | F08-11 | 5 |
| 22 | C10- 7 | 11 |
| 23 | E08- X | 2 |
| 24 | E08- X | 2 |
| 25 | L05-16 | 27 |
| 26 | E08-11 | 9 |
| 27 | D12- 4 | 11 |
| 28 | F01- 1 | 11 |

JACK PIN

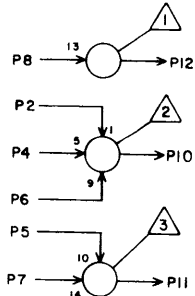
CIRCUIT SPECIFICATION 1182760

60227300 F

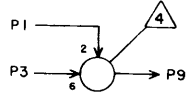
LS 63064400
ASSY



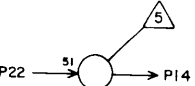
READ 2
READ SYNC
READ 3



WRITE
PARITY

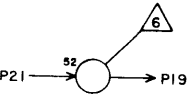


POSITION & HG



READ

CLEAR
COUNTER



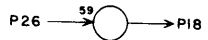
WRITE



BIT COUNT
BIT 6



B CONN



READ
INACTIVE



WRITE TIME OUT



BUSY

TL

| RV | G | E09 |
|----|--------|-----|
| 1 | M14- 2 | 15 |
| 2 | F10-10 | 7 |
| 3 | M14-17 | 17 |
| 4 | E08-19 | 5 |
| 5 | F09-14 | 7 |
| 6 | E10-18 | 5 |
| 7 | F05- 1 | 9 |
| 8 | D12-13 | 9 |
| 9 | K09- 5 | 23 |
| 10 | D12- 2 | 9 |
| 11 | E10- 1 | 5 |
| 12 | G01- 8 | 15 |
| 13 | E08- 8 | 5 |
| 14 | D12-21 | 9 |
| 15 | E10- 6 | 5 |
| 16 | G08- 4 | 9 |
| 17 | F10- 5 | 7 |
| 18 | J07- 7 | 19 |
| 19 | D12-23 | 7 |
| 20 | D02-12 | 13 |
| 21 | G04-18 | 11 |
| 22 | E12-18 | 7 |
| 23 | F06-10 | 7 |
| 24 | G12-23 | 11 |
| 25 | K05-23 | 25 |
| 26 | C10-11 | 11 |
| 27 | E10-14 | 5 |
| 28 | F01-27 | 13 |

JACK PIN LG

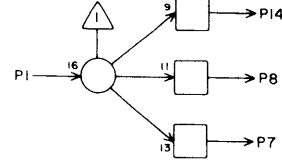
CIRCUIT SPECIFICATION 11827600

60227300 F

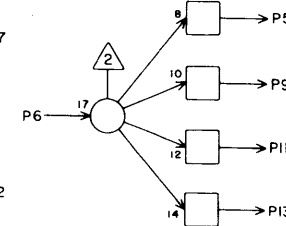
LS 63064000
ASSY



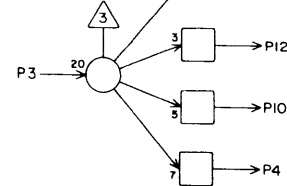
WRITE PARITY



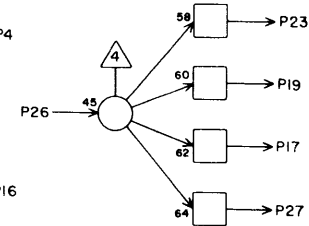
B CONN



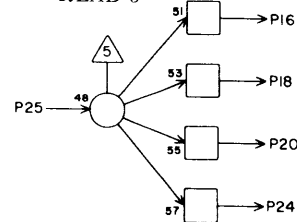
READ 3



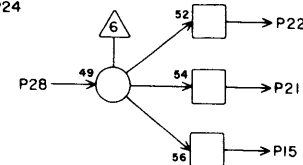
A CONN



READ 3



CLEAR EMPTY &
INPUT LOADED



| TH | RV | G | E10 |
|----|----|--------|-----|
| | 1 | E09-11 | 5 |
| | 2 | F13-15 | 9 |
| | 3 | F10-19 | 7 |
| | 4 | - | |
| | 5 | I16-26 | 21 |
| | 6 | E09-15 | 5 |
| | 7 | G10-16 | 11 |
| | 8 | G09-16 | 11 |
| | 9 | K06- 3 | 120 |
| | 10 | G08-21 | 11 |
| | 11 | I05-20 | 19 |
| | 12 | E10-25 | 5 |
| | 13 | | |
| | 14 | E09-27 | 5 |
| | 15 | - | |
| | 16 | F14-15 | 9 |
| | 17 | - | |
| | 18 | E09- 6 | 5 |
| | 19 | I13-26 | 17 |
| | 20 | - | |
| | 21 | G12-26 | 11 |
| | 22 | F10-21 | 7 |
| | 23 | I05-27 | 19 |
| | 24 | - | |
| | 25 | E10-12 | 5 |
| | 26 | J10- 4 | 17 |
| | 27 | - | |
| | 28 | F08- 1 | 5 |

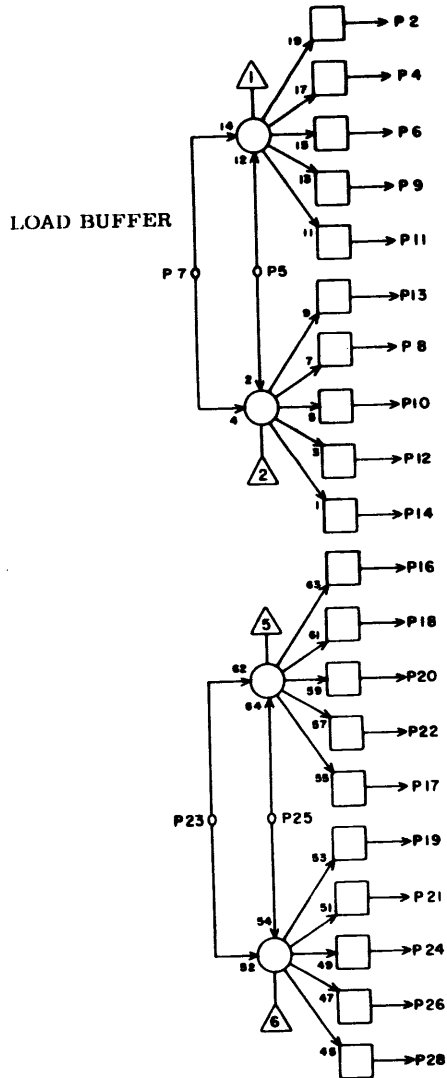
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60227300 G

LS 63044800
ASSY

B
REV



| RV | 1E11 |
|----|-----------|
| 1 | - |
| 2 | H08-7 15 |
| 3 | - |
| 4 | H08-22 15 |
| 5 | F12-11 7 |
| 6 | H09-7 13 |
| 7 | J02-11 25 |
| 8 | G04-3 13 |
| 9 | H09-22 15 |
| 10 | E13-26 7 |
| 11 | G04-26 15 |
| 12 | G12-2 9 |
| 13 | - |
| 14 | H05-6 15 |
| 15 | - |
| 16 | - |
| 17 | - |
| 18 | - |
| 19 | - |
| 20 | - |
| 21 | - |
| 22 | - |
| 23 | - |
| 24 | - |
| 25 | - |
| 26 | - |
| 27 | - |
| 28 | - |

JACK PIN LG
CIRCUIT SPECIFICATION 11027600
60227300 G

LS 63063400
ASSY

C
REV

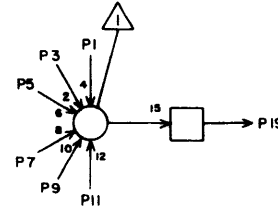
IN SYNC

| RV | 1E12 |
|----|-----------|
| 1 | E13-14 5 |
| 2 | F10-25 9 |
| 3 | G06-22 15 |
| 4 | E04-12 11 |
| 5 | E06-6 9 |
| 6 | E12-X 2 |
| 7 | E12-X 2 |
| 8 | E12-X 2 |
| 9 | E12-X 2 |
| 10 | E12-X 2 |
| 11 | E12-X 2 |
| 12 | F08-9 9 |
| 13 | F10-11 7 |
| 14 | E08-12 7 |
| 15 | I05-17 21 |
| 16 | C10-2 11 |
| 17 | D12-1 7 |
| 18 | E09-22 7 |
| 19 | H13-21 13 |
| 20 | E08-17 7 |
| 21 | F06-1 11 |
| 22 | - |
| 23 | G07-8 11 |
| 24 | E12-X 2 |
| 25 | D03-12 15 |
| 26 | C09-20 11 |
| 27 | E12-X 2 |
| 28 | E05-24 11 |

JACK PIN LG
CIRCUIT SPECIFICATION 11027600
60227300 F

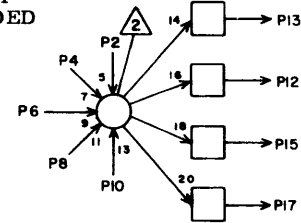
READ DATA

SYNC 1
t2



INPUT LOADED

t1



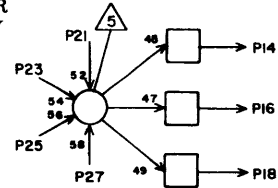
INPUT LOADED
t1

READ SECTOR VERIFY

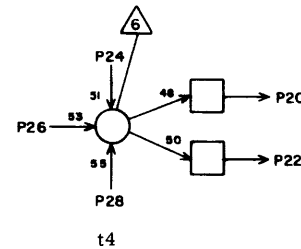
SECTOR VERIFY

READ 1

READY



COUNT
70
10

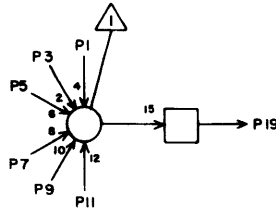


LS 63063400
ASSY



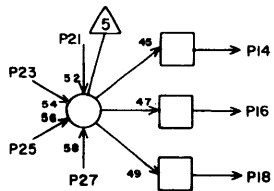
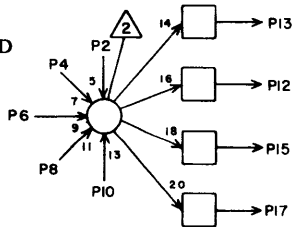
REV

TB



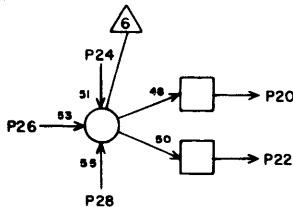
EMPTY

INPUT LOADED



TO IN SYNC
GATE

LOAD
BUFFER

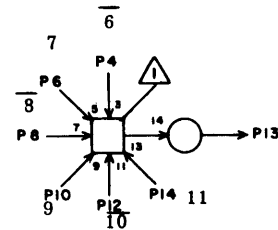


LS 63048700
ASSY

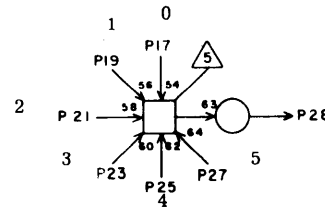
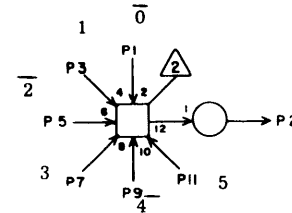


REV

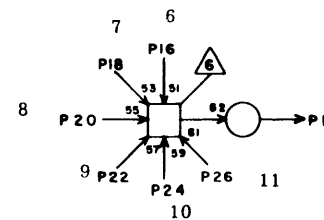
IP



PARITY



TO IN SYNC
GATE



| RV | G | E13 |
|----|--------|-----|
| 1 | B07-14 | 15 |
| 2 | G12-25 | 11 |
| 3 | J08-17 | 23 |
| 4 | F10-27 | 9 |
| 5 | G13-20 | 11 |
| 6 | F11-23 | 9 |
| 7 | E01-22 | 17 |
| 8 | E13- X | 2 |
| 9 | F01-23 | 17 |
| 10 | E13- X | 2 |
| 11 | E13- X | 2 |
| 12 | - | - |
| 13 | F12-18 | 7 |
| 14 | E12- 1 | 5 |
| 15 | - | - |
| 16 | G06-17 | 13 |
| 17 | - | - |
| 18 | - | - |
| 19 | A10-12 | 17 |
| 20 | D10-12 | 9 |
| 21 | F01-14 | 17 |
| 22 | D10-11 | 9 |
| 23 | E14-28 | 5 |
| 24 | B07- 8 | 17 |
| 25 | E14-15 | 5 |
| 26 | E11-10 | 7 |
| 27 | E13- X | 2 |
| 28 | G10-12 | 13 |

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

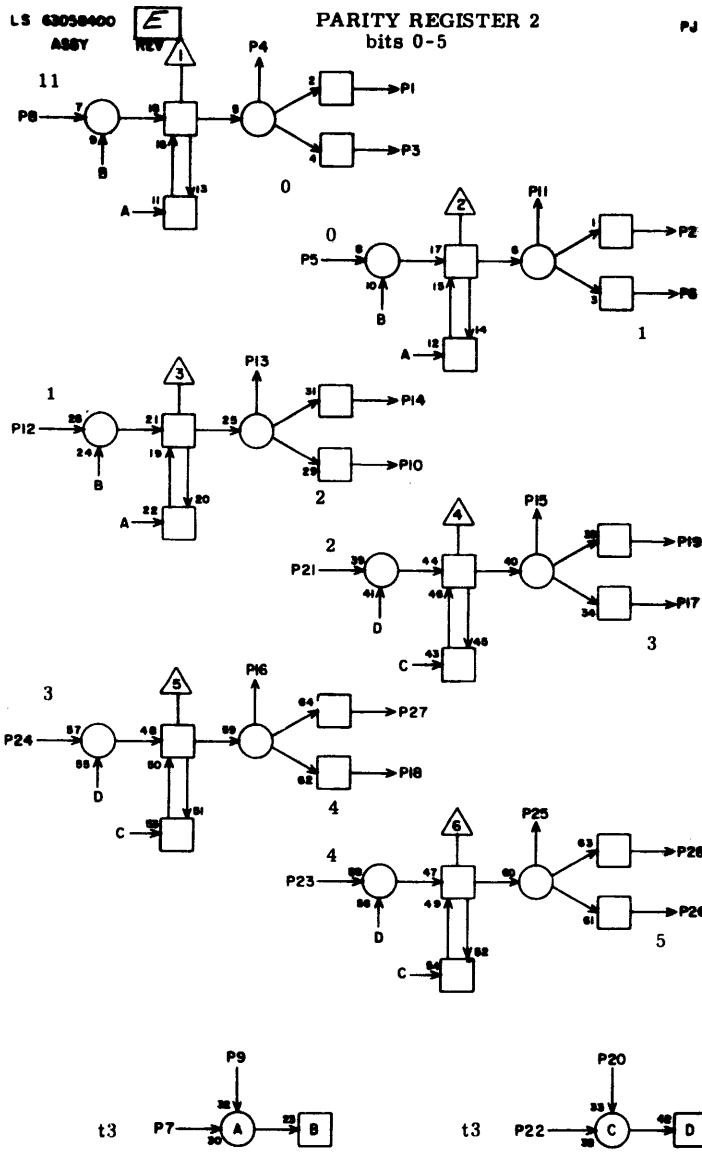
60227300 F

| RV | G | E14 |
|----|--------|-----|
| 1 | E15- 4 | 5 |
| 2 | F07- 5 | 11 |
| 3 | E15- 2 | 5 |
| 4 | E16- 4 | 5 |
| 5 | E15-13 | 5 |
| 6 | E16- 2 | 5 |
| 7 | E15-19 | 5 |
| 8 | E16-13 | 7 |
| 9 | E15-16 | 5 |
| 10 | E16-19 | 7 |
| 11 | E15-28 | 5 |
| 12 | E16-16 | 5 |
| 13 | F07- 7 | 11 |
| 14 | E16-28 | 7 |
| 15 | E13-25 | 5 |
| 16 | J04-27 | 25 |
| 17 | J03- 6 | 25 |
| 18 | J04-20 | 25 |
| 19 | J03- 7 | 25 |
| 20 | J05- 6 | 23 |
| 21 | J03-27 | 25 |
| 22 | J05- 7 | 23 |
| 23 | J03-20 | 25 |
| 24 | J05-27 | 25 |
| 25 | J04- 6 | 23 |
| 26 | J05-20 | 23 |
| 27 | J04- 7 | 23 |
| 28 | E13-23 | 5 |

JACK PIN LG

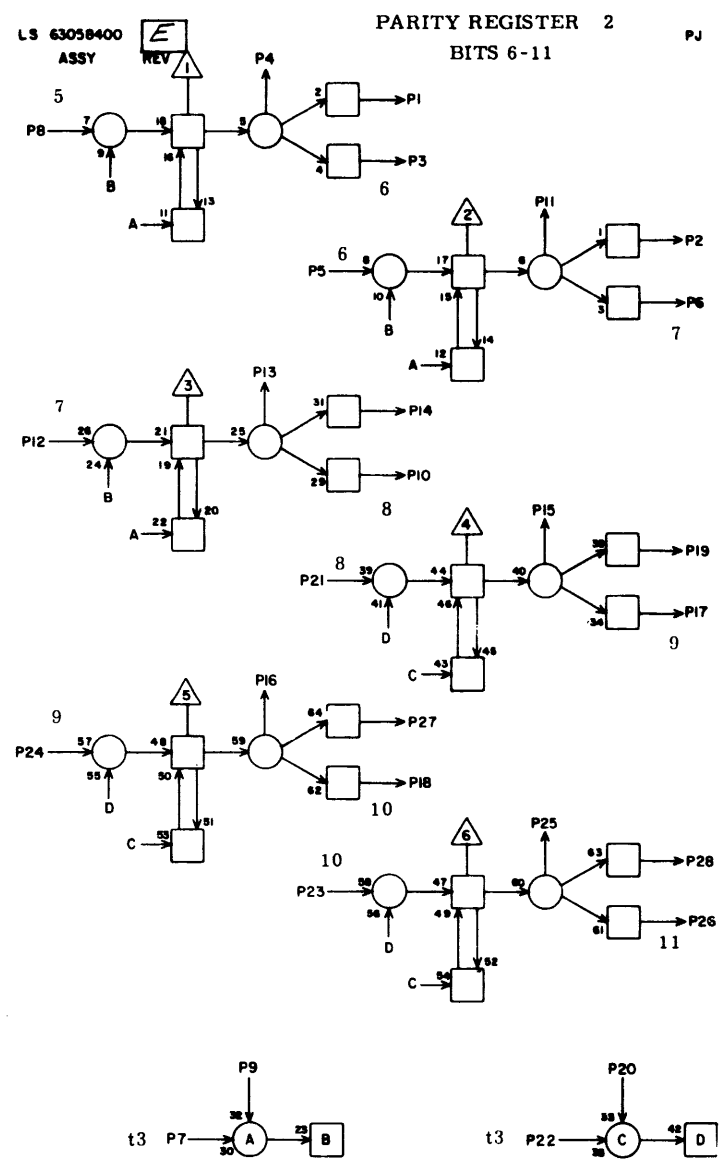
CIRCUIT SPECIFICATION 11827600

60227300 F



| V | G | E15 |
|----|--------|-----|
| 1 | G09- 2 | 13 |
| 2 | E14- 3 | 5 |
| 3 | F15- 8 | 7 |
| 4 | E14- 1 | 5 |
| 5 | G14-14 | 11 |
| 6 | F15- 3 | 7 |
| 7 | E05- 4 | 15 |
| 8 | G16-21 | 11 |
| 9 | E15- X | 2 |
| 10 | F15-11 | 7 |
| 11 | G09- 1 | 13 |
| 12 | G14- 9 | 9 |
| 13 | E14- 5 | 5 |
| 14 | G09-12 | 13 |
| 15 | G09-17 | 13 |
| 16 | E14- 9 | 5 |
| 17 | F15-20 | 7 |
| 18 | F15-26 | 7 |
| 19 | E14- 7 | 5 |
| 20 | E15- X | 2 |
| 21 | G14-18 | 9 |
| 22 | E05- 6 | 15 |
| 23 | G15-14 | 9 |
| 24 | G14-21 | 9 |
| 25 | G09-27 | 13 |
| 26 | F15-23 | 7 |
| 27 | G09-28 | 13 |
| 28 | E14-11 | 5 |

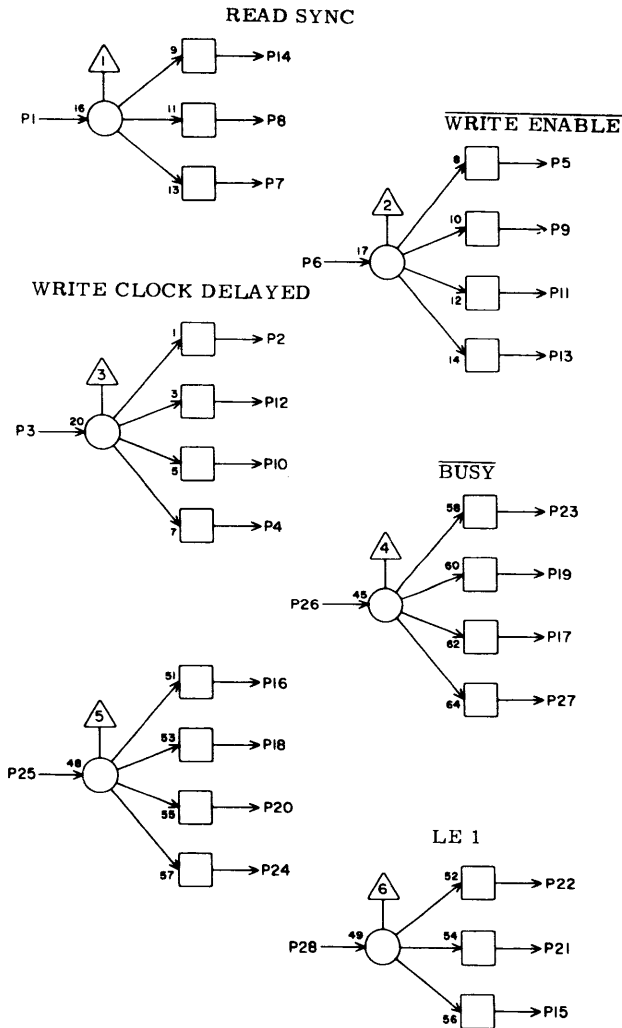
JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F



| RV | G | E16 |
|----|--------|-----|
| 1 | G10- 2 | 13 |
| 2 | E14- 6 | 5 |
| 3 | F16- 8 | 7 |
| 4 | E14- 4 | 5 |
| 5 | G15-18 | 11 |
| 6 | F16- 3 | 7 |
| 7 | E05- 8 | 15 |
| 8 | G15- 9 | 11 |
| 9 | E16- X | 2 |
| 10 | F16-11 | 7 |
| 11 | G10- 1 | 13 |
| 12 | G15-21 | 11 |
| 13 | E14- 8 | 7 |
| 14 | G10-12 | 13 |
| 15 | G10-17 | 13 |
| 16 | E14-12 | 5 |
| 17 | F16-20 | 7 |
| 18 | F16-26 | 7 |
| 19 | E14-10 | 7 |
| 20 | E16- X | 2 |
| 21 | G16-14 | 9 |
| 22 | E05-11 | 15 |
| 23 | G16-18 | 9 |
| 24 | G16- 9 | 9 |
| 25 | G18-27 | 13 |
| 26 | F16-23 | 7 |
| 27 | G18-28 | 13 |
| 28 | E14-14 | 7 |

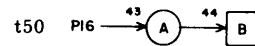
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CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63064000
ASSY REV



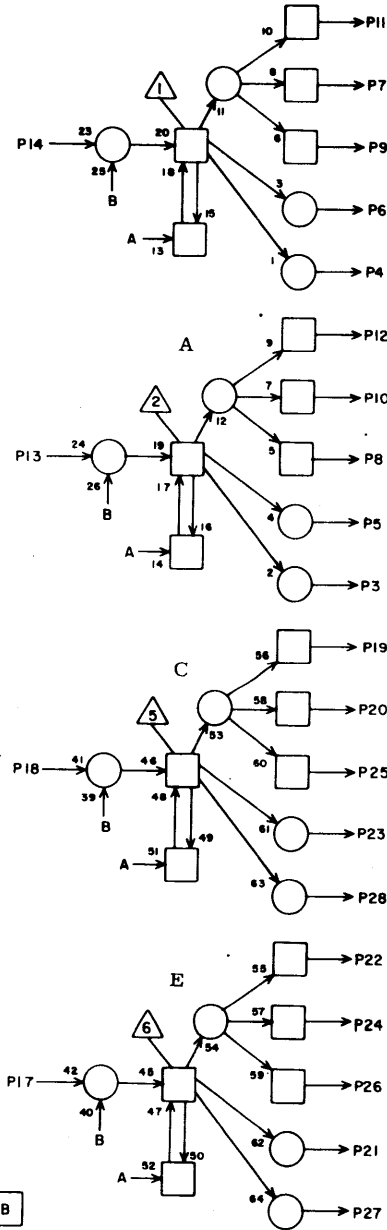
| TH | RV | G | F01 |
|----|----|--------|-----|
| | 1 | E08-28 | 11 |
| | 2 | A09- 1 | 23 |
| | 3 | F01-16 | 120 |
| | 4 | F07-27 | 11 |
| | 5 | D09-21 | 13 |
| | 6 | F05-20 | 9 |
| | 7 | - | |
| | 8 | G08- 2 | 11 |
| | 9 | A09- 3 | 25 |
| | 10 | I09- 7 | 120 |
| | 11 | E02-15 | 7 |
| | 12 | - | |
| | 13 | J07- 6 | 19 |
| | 14 | E13-21 | 17 |
| | 15 | - | |
| | 16 | F01- 3 | 120 |
| | 17 | C08-20 | 15 |
| | 18 | E04- 5 | 9 |
| | 19 | G08- 5 | 11 |
| | 20 | F02-14 | 5 |
| | 21 | A02-22 | 19 |
| | 22 | A02-11 | 21 |
| | 23 | E13- 9 | 17 |
| | 24 | - | |
| | 25 | G01- 1 | 5 |
| | 26 | E03-27 | 7 |
| | 27 | E09-28 | 13 |
| | 28 | B08-28 | 21 |

JACK PIN
CIRCUIT SPECIFICATION 11827800
60227300 F



LS 63057900
ASSY REV

FILE CLOCK
STROBE NETWORK



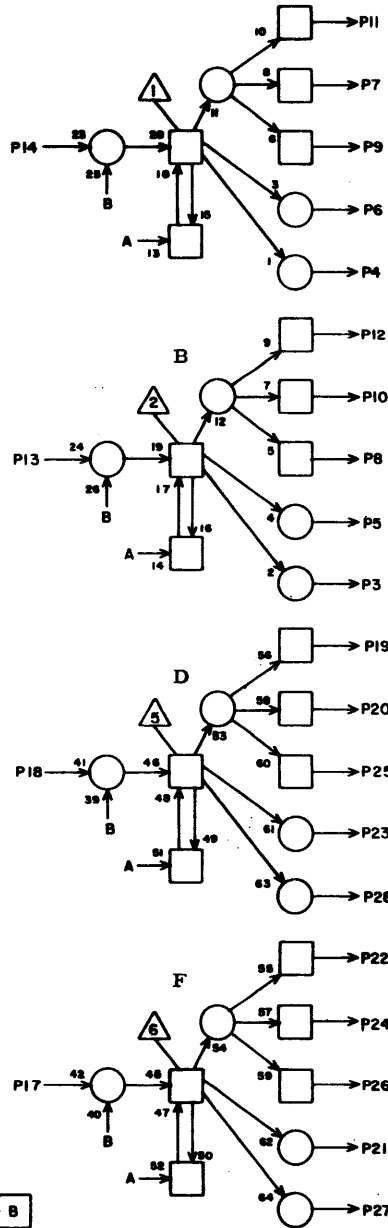
| PD | RV | G | F02 |
|----|----|--------|-----|
| | 1 | - | |
| | 2 | - | |
| | 3 | - | |
| | 4 | - | |
| | 5 | - | |
| | 6 | - | |
| | 7 | - | |
| | 8 | E06- 7 | 9 |
| | 9 | - | |
| | 10 | F04-23 | 7 |
| | 11 | F03-14 | 5 |
| | 12 | F03-13 | 5 |
| | 13 | F03-11 | 5 |
| | 14 | F01-20 | 5 |
| | 15 | - | |
| | 16 | J09-26 | 21 |
| | 17 | F03-19 | 5 |
| | 18 | F03-12 | 5 |
| | 19 | F03-18 | 5 |
| | 20 | E05- 7 | 9 |
| | 21 | - | |
| | 22 | F03-17 | 5 |
| | 23 | - | |
| | 24 | E05-23 | 9 |
| | 25 | E06-23 | 9 |
| | 26 | - | |
| | 27 | - | |
| | 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827800
60227300 G

LS 63067900
ASSY

B
REV

FILE CLOCK
STROBE NETWORK



| PO | RV | G | F03 |
|----|--------|----|-----|
| 1 | - | - | |
| 2 | - | - | |
| 3 | E06- 5 | 7 | |
| 4 | - | - | |
| 5 | E04-25 | 5 | |
| 6 | - | - | |
| 7 | - | - | |
| 8 | - | - | |
| 9 | - | - | |
| 10 | - | - | |
| 11 | F02-13 | 5 | |
| 12 | F02-18 | 5 | |
| 13 | F02-12 | 5 | |
| 14 | F02-11 | 5 | |
| 15 | - | - | |
| 16 | J09- 6 | 19 | |
| 17 | F02-22 | 5 | |
| 18 | F02-19 | 5 | |
| 19 | F02-17 | 5 | |
| 20 | - | - | |
| 21 | E05-25 | 7 | |
| 22 | - | - | |
| 23 | E05- 5 | 9 | |
| 24 | - | - | |
| 25 | - | - | |
| 26 | - | - | |
| 27 | - | - | |
| 28 | E06-25 | 9 | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827900
60227300 G

LS 63064000
ASSY

C
REV

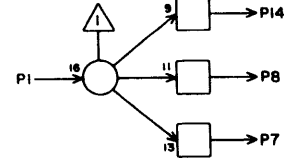
TH

R# G F04

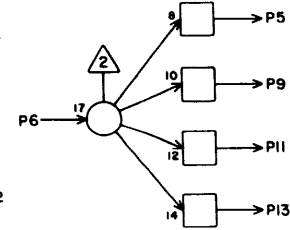
| R# | G | F04 |
|----|--------|-----|
| 1 | F05-25 | 5 |
| 2 | F13-14 | 13 |
| 3 | F05-10 | 5 |
| 4 | - | - |
| 5 | G01-15 | 9 |
| 6 | F07-13 | 7 |
| 7 | E03-19 | 7 |
| 8 | G08-24 | 9 |
| 9 | I13- 3 | 17 |
| 10 | G08-23 | 9 |
| 11 | I16- 3 | 21 |
| 12 | F14-14 | 13 |
| 13 | G01-21 | 9 |
| 14 | - | - |
| 15 | - | - |
| 16 | D03- 2 | 11 |
| 17 | G03-28 | 9 |
| 18 | G12-19 | 13 |
| 19 | F06-21 | 5 |
| 20 | F08-26 | 7 |
| 21 | D02- 9 | 11 |
| 22 | D08-18 | 11 |
| 23 | G03-25 | 7 |
| 24 | I05- 5 | 11 |
| 25 | G11- 3 | 11 |
| 26 | F06-19 | 7 |
| 27 | - | - |
| 28 | D02-16 | 11 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827900
60227300 F

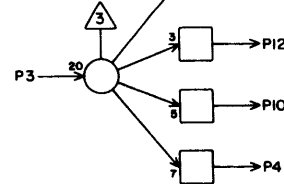
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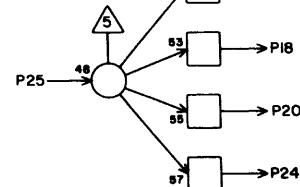
READY



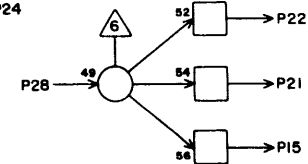
WRITE 3



MC

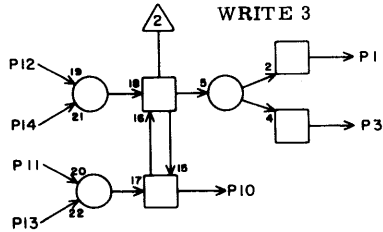
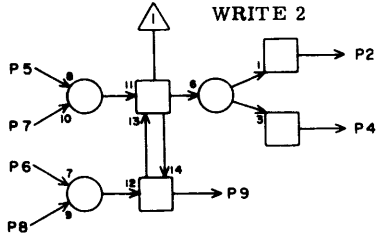


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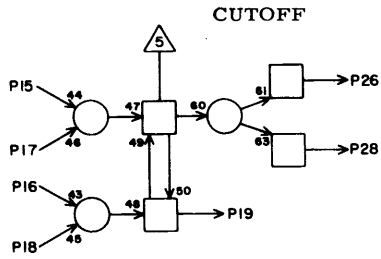


LS 63040000
ASSY

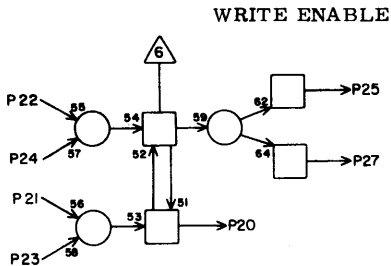
D
REV



WRITE 2



BUFFER
LOADED



AA

RV G F05

| | | |
|----|--------|-----|
| 1 | E09- 7 | 9 |
| 2 | F05-12 | 5 |
| 3 | - | |
| 4 | - | |
| 5 | G03-20 | 9 |
| 6 | F09-12 | 7 |
| 7 | E04-20 | 5 |
| 8 | E05-26 | 5 |
| 9 | F09- 1 | 7 |
| 10 | F04- 3 | 5 |
| 11 | F09- 8 | 7 |
| 12 | F05- 2 | 5 |
| 13 | E06-22 | 7 |
| 14 | E05-19 | 7 |
| 15 | G03-22 | 9 |
| 16 | E04-10 | 7 |
| 17 | E06-17 | 7 |
| 18 | G13-21 | 13 |
| 19 | F09- 3 | 9 |
| 20 | F01- 6 | 9 |
| 21 | G01-16 | 9 |
| 22 | G03-12 | 7 |
| 23 | F05- X | 2 |
| 24 | F05- X | 2 |
| 25 | F04- 1 | 5 |
| 26 | I05-13 | 120 |
| 27 | L05-27 | 23 |
| 28 | - | |

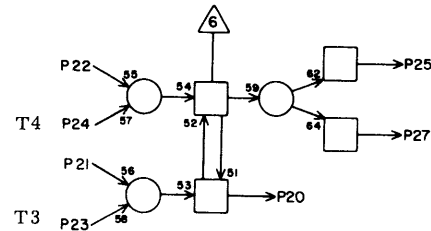
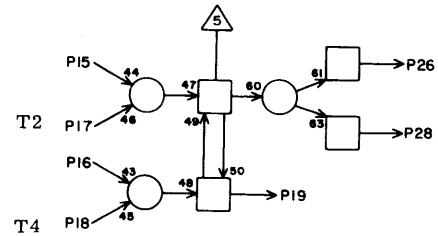
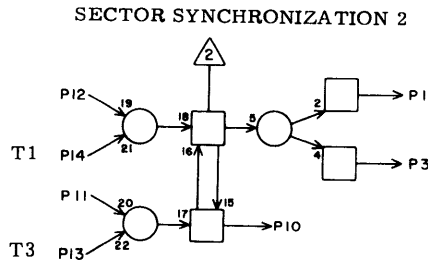
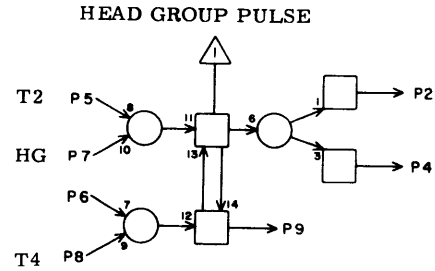
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60227300 F

LS 63040000
ASSY

D
REV



AA

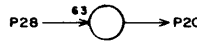
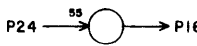
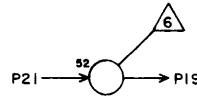
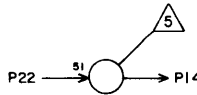
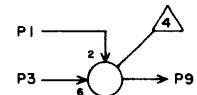
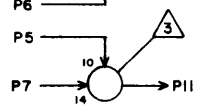
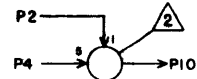
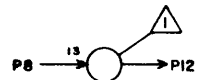
RV G F06

| | | |
|----|--------|----|
| 1 | E12-21 | 11 |
| 2 | L05-12 | 23 |
| 3 | G04-21 | 9 |
| 4 | J07-24 | 19 |
| 5 | E07- 8 | 7 |
| 6 | F06- X | 2 |
| 7 | G05-12 | 7 |
| 8 | E05-20 | 7 |
| 9 | C08-27 | 13 |
| 10 | E09-23 | 7 |
| 11 | E08- 9 | 7 |
| 12 | E08- 2 | 9 |
| 13 | E05-10 | 7 |
| 14 | E04- 8 | 7 |
| 15 | G04-14 | 7 |
| 16 | C09-14 | 15 |
| 17 | E04-26 | 7 |
| 18 | E05-22 | 7 |
| 19 | F04-26 | 7 |
| 20 | G03-26 | 9 |
| 21 | F04-19 | 5 |
| 22 | F06-20 | 3 |
| 23 | E05-12 | 9 |
| 24 | E05-17 | 7 |
| 25 | G03-27 | 9 |
| 26 | G03- 3 | 7 |
| 27 | - | |
| 28 | F06-22 | 3 |

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60227300 F



BIT 3 HOLDING REG

PARITY

BIT 5 HOLDING REG

VERIFY

VERIFY

READY

WRITE INACTIVE

WRITE CLOCK

READ 2

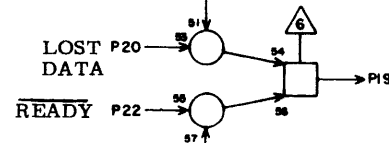
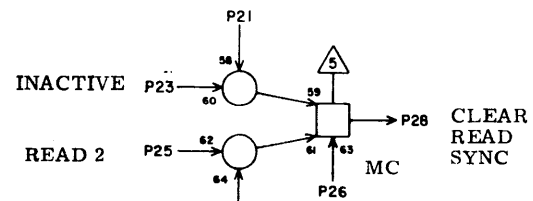
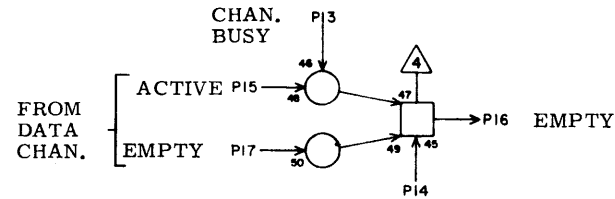
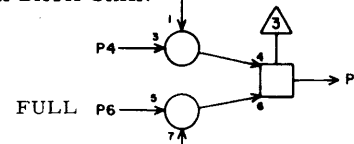
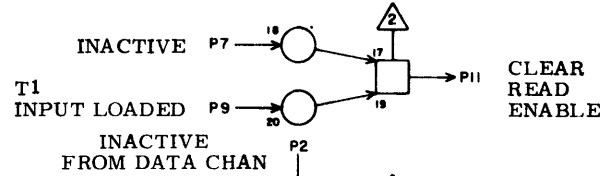
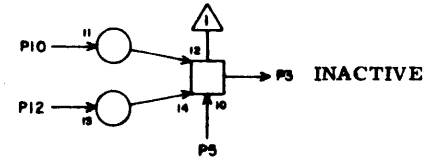
TL

| RV | 1F07 | |
|----|--------|----|
| 1 | F07- X | 2 |
| 2 | H10-20 | 13 |
| 3 | H11-12 | 11 |
| 4 | F07- X | 2 |
| 5 | E14- 2 | 11 |
| 6 | F07- X | 2 |
| 7 | E14-13 | 11 |
| 8 | I09-11 | 15 |
| 9 | K10-23 | 23 |
| 10 | I10-12 | 15 |
| 11 | O12- 3 | 13 |
| 12 | E04- 7 | 9 |
| 13 | F04- 6 | 7 |
| 14 | D07- 4 | 11 |
| 15 | G02- 5 | 9 |
| 16 | G02- 3 | 9 |
| 17 | E02-23 | 9 |
| 18 | J07- 5 | 15 |
| 19 | D02- 4 | 13 |
| 20 | F10-16 | 7 |
| 21 | D06-15 | 11 |
| 22 | D05-18 | 11 |
| 23 | D03-17 | 13 |
| 24 | G03-24 | 9 |
| 25 | C11- 9 | 15 |
| 26 | G03-14 | 9 |
| 27 | F01- 4 | 11 |
| 28 | G13-11 | 11 |

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60227300 G



CHANNEL BUSY & ACTIVE

QM

RV 1F08

| RV | 1F08 | |
|----|--------|----|
| 1 | E10-28 | 5 |
| 2 | G11- 7 | 9 |
| 3 | F11-17 | 7 |
| 4 | F08- X | 2 |
| 5 | F12-21 | 9 |
| 6 | F11-20 | 7 |
| 7 | G11-13 | 9 |
| 8 | F08- X | 2 |
| 9 | E12-12 | 9 |
| 10 | J07-13 | 17 |
| 11 | E08-21 | 5 |
| 12 | K10-16 | 21 |
| 13 | C10-18 | 13 |
| 14 | F08- X | 2 |
| 15 | G13- 8 | 9 |
| 16 | G12-21 | 9 |
| 17 | J02-23 | 21 |
| 18 | H05-28 | 11 |
| 19 | F12-17 | 7 |
| 20 | H04-20 | 11 |
| 21 | F08- X | 2 |
| 22 | H10-25 | 11 |
| 23 | G11-11 | 7 |
| 24 | G12-20 | 9 |
| 25 | G13-13 | 9 |
| 26 | F04-20 | 7 |
| 27 | F08- X | 2 |
| 28 | E08-16 | 7 |

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60227300 F

LS 63064000
ASSY

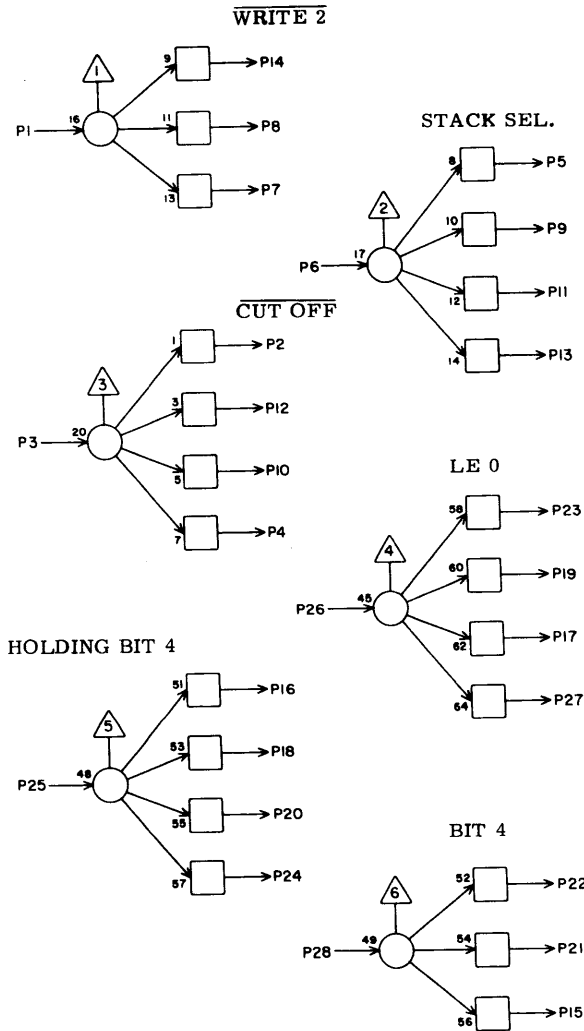


TH

| RV | G | F09 |
|----|--------|-----|
| 1 | F05- 9 | 7 |
| 2 | H13- 5 | 13 |
| 3 | F05-19 | 9 |
| 4 | - | |
| 5 | I12-25 | 15 |
| 6 | C07-20 | 13 |
| 7 | - | |
| 8 | F05-11 | 7 |
| 9 | I15-25 | 17 |
| 10 | I05-15 | 15 |
| 11 | G06-18 | 9 |
| 12 | F05- 6 | 7 |
| 13 | A09-18 | 19 |
| 14 | E09- 5 | 7 |
| 15 | C08-25 | 13 |
| 16 | C06-24 | 13 |
| 17 | - | |
| 18 | A08-11 | 21 |
| 19 | B02-11 | 21 |
| 20 | F09-28 | 5 |
| 21 | D10-17 | 11 |
| 22 | D10-14 | 11 |
| 23 | B02-22 | 21 |
| 24 | D05-24 | 11 |
| 25 | H11- 8 | 9 |
| 26 | B08- 8 | 19 |
| 27 | - | |
| 28 | F09-20 | 5 |

JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60227300 F



LS 63040000
ASSY



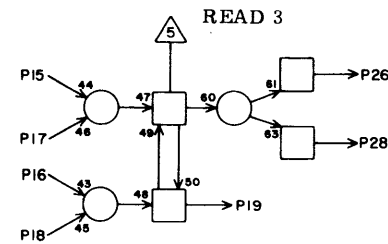
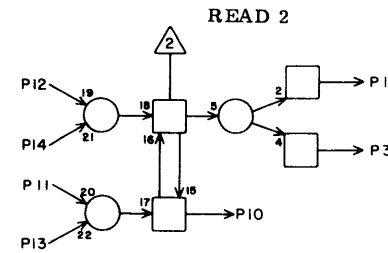
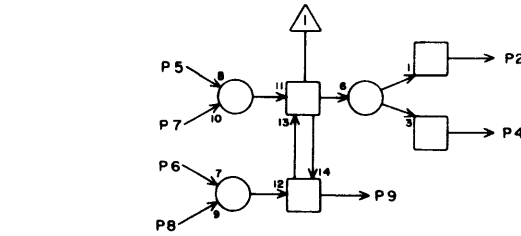
WRITE GUARD BITS TIME OUT

AA

| RV | G | F10 |
|----|--------|-----|
| 1 | - | |
| 2 | 009- 9 | 9 |
| 3 | G13- 6 | 7 |
| 4 | D12-28 | 120 |
| 5 | E09-17 | 7 |
| 6 | D12-20 | 9 |
| 7 | F10- X | 2 |
| 8 | F10- X | 2 |
| 9 | - | |
| 10 | E09- 2 | 7 |
| 11 | E12-13 | 7 |
| 12 | H13-28 | 13 |
| 13 | F10- X | 2 |
| 14 | F10- X | 2 |
| 15 | G13- 5 | 7 |
| 16 | F07-20 | 7 |
| 17 | E04-14 | 11 |
| 18 | F10- X | 2 |
| 19 | E10- 3 | 7 |
| 20 | - | |
| 21 | E10-22 | 7 |
| 22 | G13-23 | 9 |
| 23 | F10- X | 2 |
| 24 | E06- 9 | 9 |
| 25 | E12- 2 | 9 |
| 26 | G13-26 | 9 |
| 27 | E13- 4 | 9 |
| 28 | - | |

JACK PIN LG

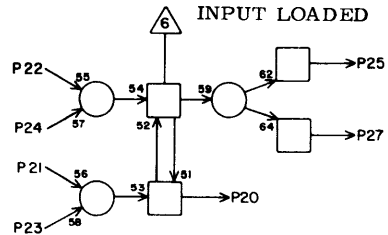
CIRCUIT SPECIFICATION 11827600
60227300 F



READ 2

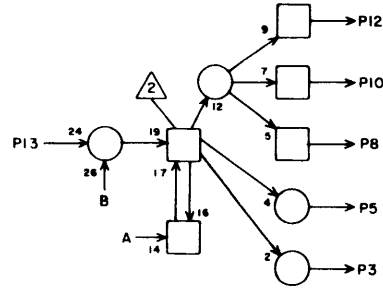
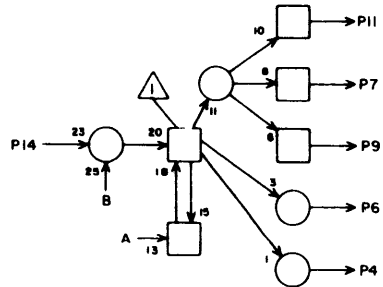
READ 3

t2

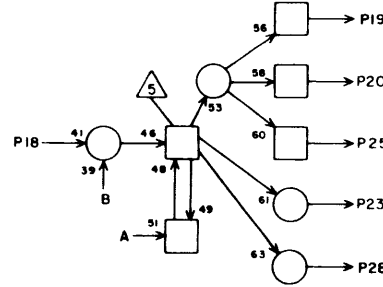


LS 63057900
ASSY

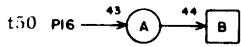
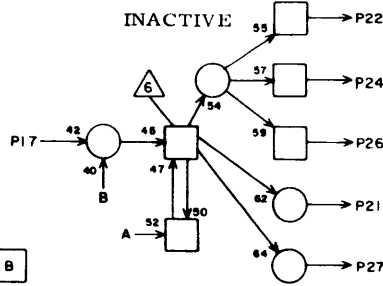
B
REV



EMPTY



INACTIVE



| PD | R# | G | F11 |
|----|--------|----|-----|
| 1 | - | - | |
| 2 | - | - | |
| 3 | - | - | |
| 4 | - | - | |
| 5 | - | - | |
| 6 | G08-7 | 7 | |
| 7 | G08-26 | 9 | |
| 8 | - | - | |
| 9 | G12-7 | 7 | |
| 10 | - | - | |
| 11 | - | - | |
| 12 | - | - | |
| 13 | F12-12 | 5 | |
| 14 | F12-7 | 5 | |
| 15 | - | - | |
| 16 | J09-28 | 19 | |
| 17 | F08-3 | 7 | |
| 18 | F12-20 | 5 | |
| 19 | H15-14 | 11 | |
| 20 | F08-6 | 7 | |
| 21 | G12-17 | 7 | |
| 22 | I09-23 | 13 | |
| 23 | E13-6 | 9 | |
| 24 | I10-23 | 13 | |
| 25 | - | - | |
| 26 | - | - | |
| 27 | G07-17 | 9 | |
| 28 | - | - | |

FULL TO DATA CHANNELS

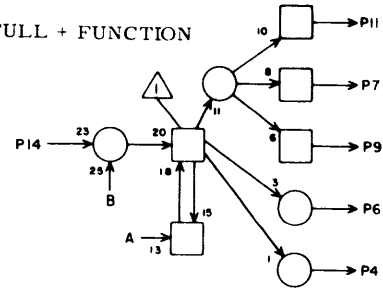
JACK PIN LG
CIRCUIT SPECIFICATION 11827600

60227300 G

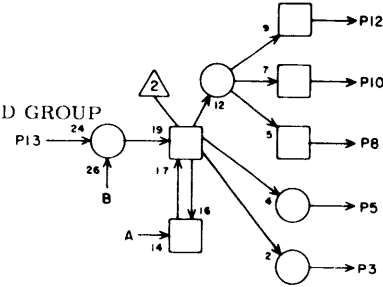
LS 63057900
ASSY

B
REV

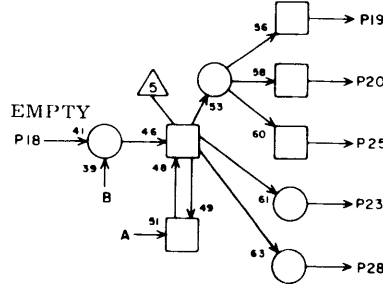
FULL + FUNCTION



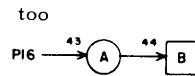
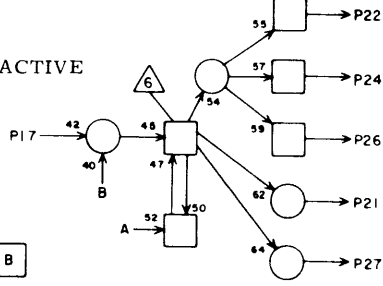
HEAD GROUP



EMPTY




INACTIVE



| PD | R# | G | F12 |
|----|--------|----|-----|
| 1 | - | - | |
| 2 | - | - | |
| 3 | - | - | |
| 4 | - | - | |
| 5 | - | - | |
| 6 | - | - | |
| 7 | F11-14 | 5 | |
| 8 | - | - | |
| 9 | - | - | |
| 10 | - | - | |
| 11 | E11-5 | 7 | |
| 12 | F11-13 | 5 | |
| 13 | - | - | |
| 14 | H13-16 | 11 | |
| 15 | - | - | |
| 16 | J09-4 | 17 | |
| 17 | F08-19 | 7 | |
| 18 | E13-13 | 7 | |
| 19 | - | - | |
| 20 | F11-18 | 5 | |
| 21 | F08-5 | 9 | |
| 22 | - | - | |
| 23 | - | - | |
| 24 | I05-12 | 15 | |
| 25 | - | - | |
| 26 | - | - | |
| 27 | - | - | |
| 28 | - | - | |


JACK PIN LG
CIRCUIT SPECIFICATION 11827600

60227300 F

LS 63063700
ASSY 
REV

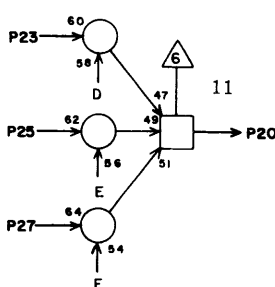
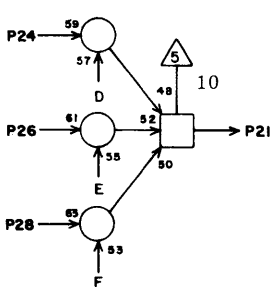
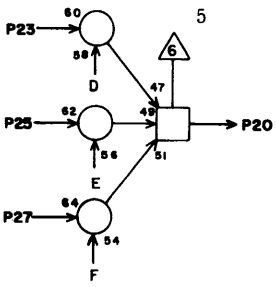
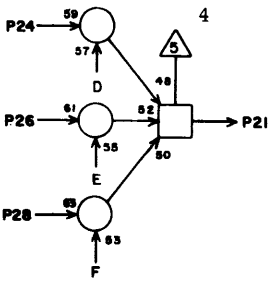
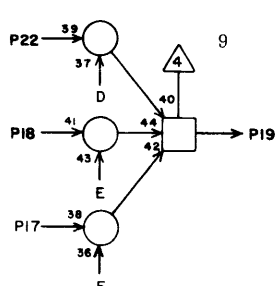
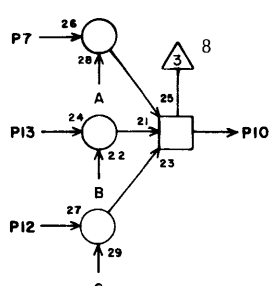
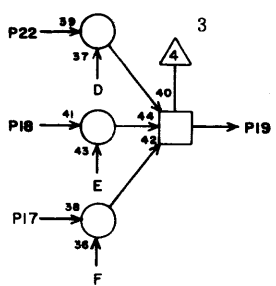
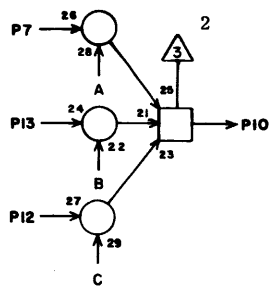
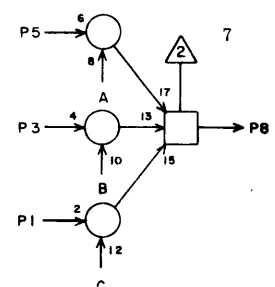
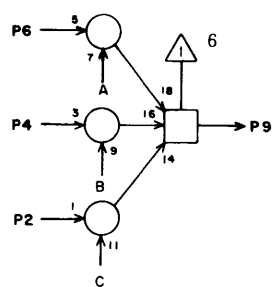
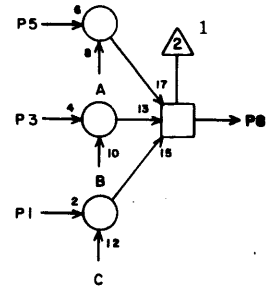
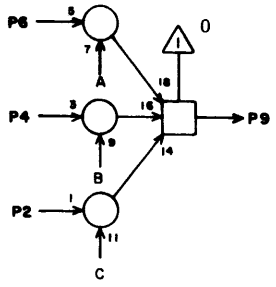
PARITY
BITS 0-5

TE RV G F13

LS 63063700
ASSY 
REV

PARITY
BITS 6-11

TE RV G F14

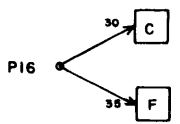
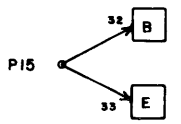
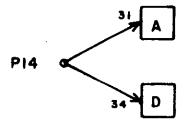


| | | |
|----|--------|----|
| 1 | - | |
| 2 | - | |
| 3 | J03- 8 | 23 |
| 4 | J03- 5 | 21 |
| 5 | H06- 6 | 13 |
| 6 | H06- 3 | 13 |
| 7 | H06-10 | 15 |
| 8 | F15- 1 | 7 |
| 9 | F15- 5 | 5 |
| 10 | F15-13 | 7 |
| 11 | - | |
| 12 | - | |
| 13 | J03-26 | 23 |
| 14 | F04- 2 | 13 |
| 15 | E10- 2 | 9 |
| 16 | F13- X | 2 |
| 17 | - | |
| 18 | J03-21 | 21 |
| 19 | F15-18 | 5 |
| 20 | F15-24 | 5 |
| 21 | F15-28 | 5 |
| 22 | H06-17 | 13 |
| 23 | H06-26 | 15 |
| 24 | H06-18 | 13 |
| 25 | J04- 8 | 19 |
| 26 | J04- 5 | 19 |
| 27 | - | |
| 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

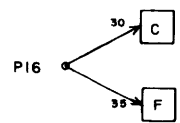
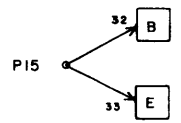
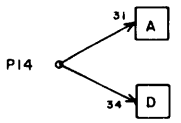
WRITE 3

READ 3



WRITE 3

READ 3

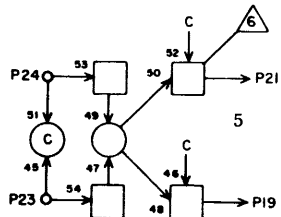
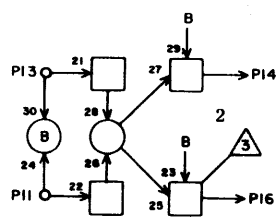
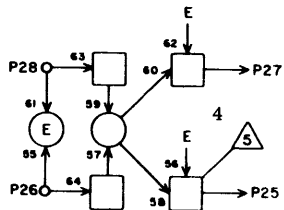
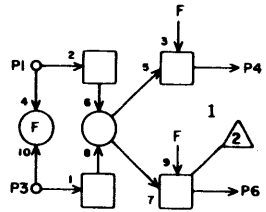
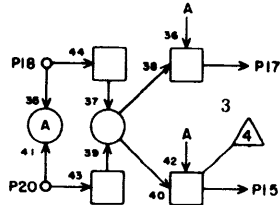
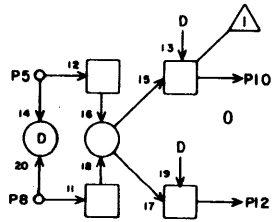


JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63040100
ASSY

E
REV

LOGICAL EQUIVALENCE
NETWORK - PARITY
BITS 0-5



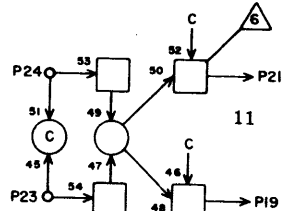
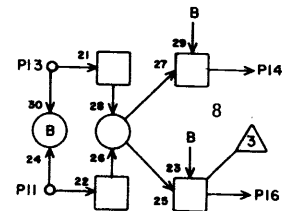
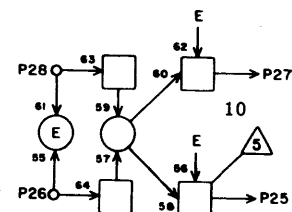
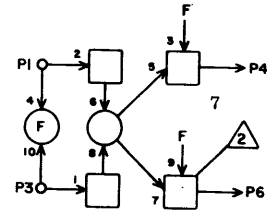
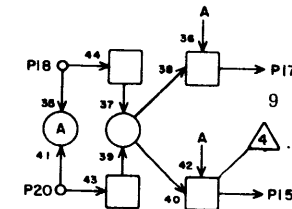
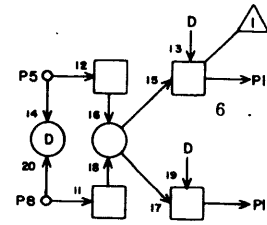
| AB | RV | G | F15 |
|----|----|--------|-----|
| | 1 | F13- 8 | 7 |
| | 2 | - | |
| | 3 | E15- 6 | 7 |
| | 4 | G14- 8 | 7 |
| | 5 | F13- 9 | 5 |
| | 6 | - | |
| | 7 | - | |
| | 8 | E15- 3 | 7 |
| | 9 | - | |
| | 10 | G14- 7 | 7 |
| | 11 | E15-10 | 7 |
| | 12 | - | |
| | 13 | F13-10 | 7 |
| | 14 | G14-23 | 7 |
| | 15 | - | |
| | 16 | - | |
| | 17 | G14-24 | 7 |
| | 18 | F13-19 | 5 |
| | 19 | - | |
| | 20 | E15-17 | 7 |
| | 21 | G15- 8 | 5 |
| | 22 | - | |
| | 23 | E15-26 | 7 |
| | 24 | F13-20 | 5 |
| | 25 | - | |
| | 26 | E15-18 | 7 |
| | 27 | G15- 7 | 5 |
| | 28 | F13-21 | 5 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63040100
ASSY

E
REV

LOGICAL EQUIVALENCE
NETWORK - PARITY
BITS 6-11



| AB | RV | G | F16 |
|----|----|--------|-----|
| | 1 | F14- 8 | 7 |
| | 2 | - | |
| | 3 | E16- 6 | 7 |
| | 4 | G15-24 | 9 |
| | 5 | F14- 9 | 5 |
| | 6 | - | |
| | 7 | - | |
| | 8 | E16- 3 | 7 |
| | 9 | - | |
| | 10 | G15-23 | 7 |
| | 11 | E16-10 | 7 |
| | 12 | - | |
| | 13 | F14-10 | 7 |
| | 14 | G16- 7 | 7 |
| | 15 | - | |
| | 16 | - | |
| | 17 | G16- 8 | 5 |
| | 18 | F14-19 | 5 |
| | 19 | - | |
| | 20 | E16-17 | 7 |
| | 21 | G16-24 | 7 |
| | 22 | - | |
| | 23 | E16-26 | 7 |
| | 24 | F14-20 | 5 |
| | 25 | - | |
| | 26 | E16-18 | 7 |
| | 27 | G16-23 | 7 |
| | 28 | F14-21 | 5 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300
60227300 F

LS 63060700
ASSY



QH

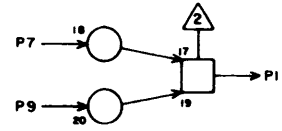
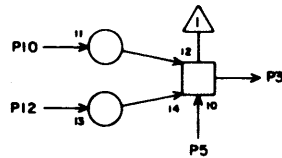
RV G G01

LS 63063500
ASSY



TC

RV G G02

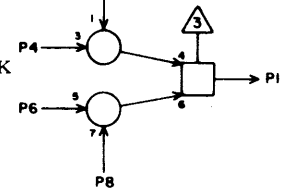


READ ON
NO SYNC.

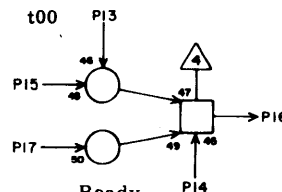
SET PARITY
ERROR FF

READ
CLOCK

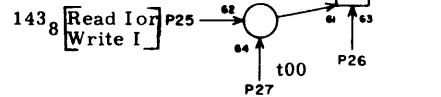
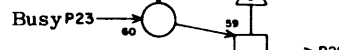
WRITE
CLOCK



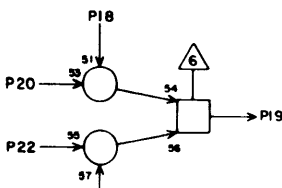
READY



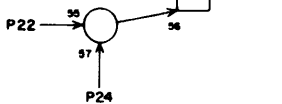
CLEAR WRITE
ENABLE



WRITE 1



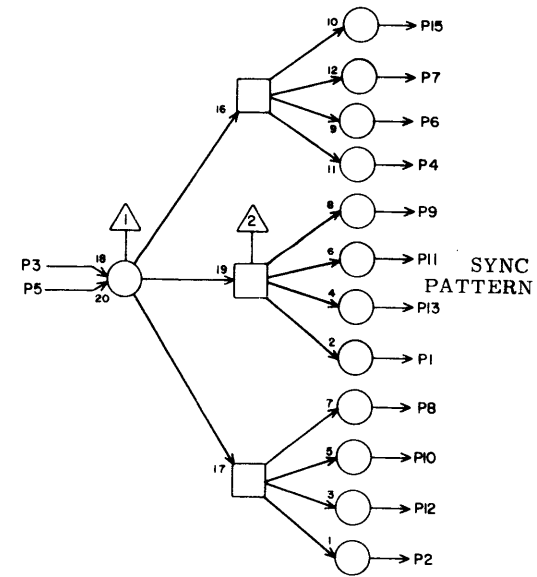
WRITE 2



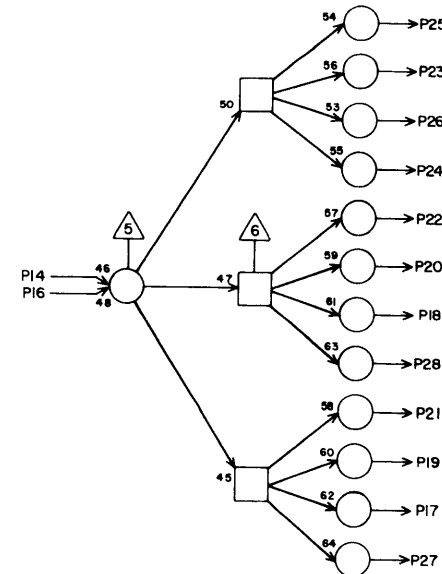
WRITE CLOCK

| | | |
|----|--------|-----|
| 1 | F01-25 | 5 |
| 2 | D12-12 | 19 |
| 3 | - | |
| 4 | K03- 6 | 17 |
| 5 | - | |
| 6 | G01-19 | 5 |
| 7 | D12-19 | 19 |
| 8 | E09-12 | 15 |
| 9 | G00-12 | 11 |
| 10 | - | |
| 11 | D08- 5 | 17 |
| 12 | - | |
| 13 | J09- 9 | 17 |
| 14 | G01- X | 2 |
| 15 | F04- 5 | 9 |
| 16 | F05-21 | 9 |
| 17 | D12-22 | 19 |
| 18 | G05-20 | 7 |
| 19 | G01- 6 | 5 |
| 20 | K03- 4 | 15 |
| 21 | F04-13 | 9 |
| 22 | K03-25 | 17 |
| 23 | C08-20 | 21 |
| 24 | G05-25 | 7 |
| 25 | K10-14 | 19 |
| 26 | G01- X | 2 |
| 27 | J09-11 | 120 |
| 28 | D10-22 | 19 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

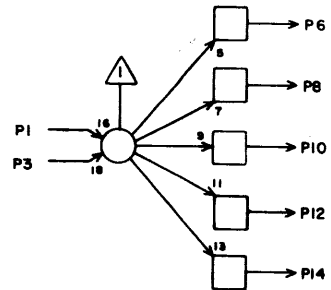


SYNC
PATTERN

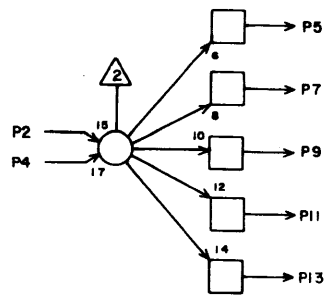


| | | |
|----|--------|----|
| 1 | G10- 5 | 11 |
| 2 | G10-23 | 13 |
| 3 | F07-16 | 9 |
| 4 | G09-22 | 11 |
| 5 | F07-15 | 9 |
| 6 | G09- 7 | 11 |
| 7 | G09- 5 | 11 |
| 8 | G10- 7 | 11 |
| 9 | G09-24 | 11 |
| 10 | G10-22 | 11 |
| 11 | G09-23 | 11 |
| 12 | G10-24 | 11 |
| 13 | G10- 6 | 11 |
| 14 | - | |
| 15 | G09- 6 | 11 |
| 16 | - | |
| 17 | - | |
| 18 | - | |
| 19 | - | |
| 20 | - | |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | - | |
| 25 | - | |
| 26 | - | |
| 27 | - | |
| 28 | - | |

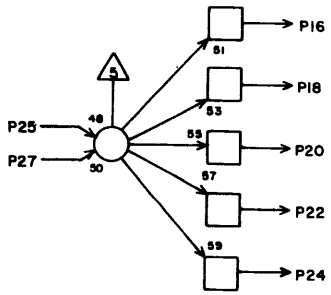
JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F



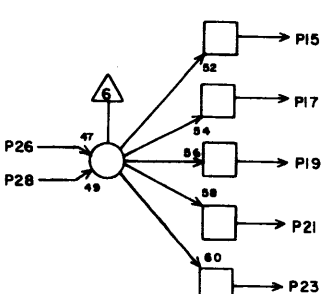
WRITE
INACTIVE



POSITION 1



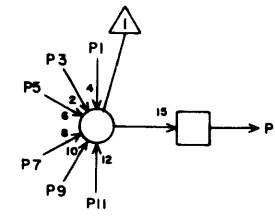
SYNC BIT



WRITE
SYNC

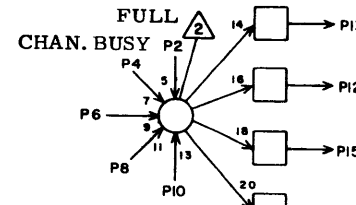
| TD | RV | G | 603 |
|----|----|--------|-----|
| | 1 | G04-16 | 5 |
| | 2 | G07-20 | 9 |
| | 3 | F06-26 | 7 |
| | 4 | G03-X | 2 |
| | 5 | D03-3 | 13 |
| | 6 | - | |
| | 7 | - | |
| | 8 | G07-14 | 7 |
| | 9 | - | |
| | 10 | - | |
| | 11 | - | |
| | 12 | F05-22 | 7 |
| | 13 | G04-1 | 5 |
| | 14 | F07-26 | 9 |
| | 15 | G09-14 | 9 |
| | 16 | - | |
| | 17 | G10-14 | 11 |
| | 18 | - | |
| | 19 | - | |
| | 20 | F05-5 | 9 |
| | 21 | - | |
| | 22 | F05-15 | 9 |
| | 23 | - | |
| | 24 | F07-24 | 9 |
| | 25 | F04-23 | 7 |
| | 26 | F06-20 | 9 |
| | 27 | F06-25 | 9 |
| | 28 | F04-17 | 9 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

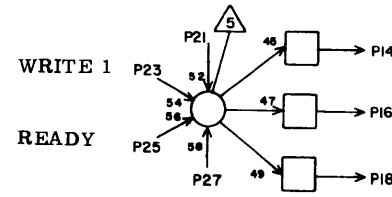


LOAD
POSITION
REGISTER
(UNITS 0 & 1)

FULL & CHAN. BUSY

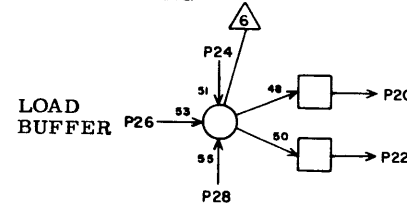


SECTOR VERIFY (WRITE)



WRITE 1
READY

HG



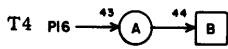
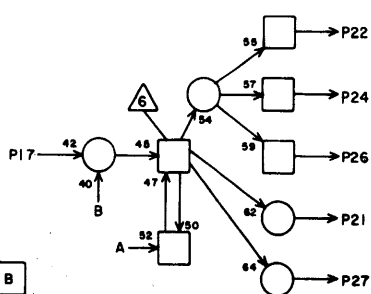
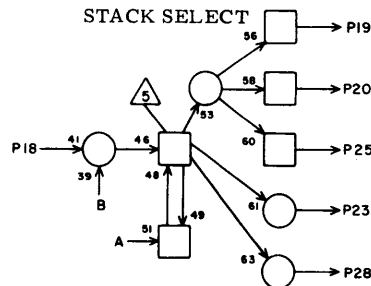
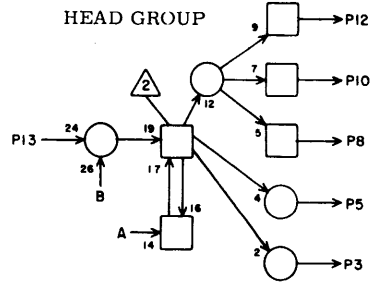
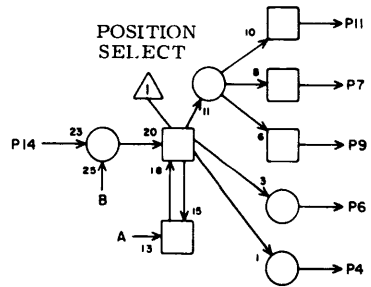
LOAD
BUFFER

| TB | PV | 1604 |
|----|----|-----------|
| | 1 | G03-13 5 |
| | 2 | J02-21 15 |
| | 3 | E11-8 13 |
| | 4 | C10-20 17 |
| | 5 | G04-X 2 |
| | 6 | G04-X 2 |
| | 7 | G04-X 2 |
| | 8 | G04-X 2 |
| | 9 | G04-X 2 |
| | 10 | G04-X 2 |
| | 11 | G04-X 2 |
| | 12 | - |
| | 13 | G12-3 11 |
| | 14 | F06-15 7 |
| | 15 | - |
| | 16 | G03-1 5 |
| | 17 | - |
| | 18 | E09-21 11 |
| | 19 | G11-26 11 |
| | 20 | D10-15 17 |
| | 21 | F06-3 9 |
| | 22 | D10-16 17 |
| | 23 | G07-10 7 |
| | 24 | B07-7 23 |
| | 25 | D03-13 15 |
| | 26 | E11-11 15 |
| | 27 | G04-X 2 |
| | 28 | C10-21 21 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 G

LS 63057900
ASSY

B
REV



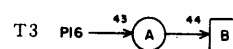
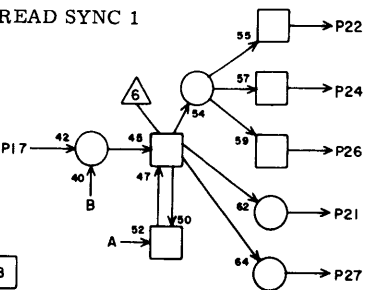
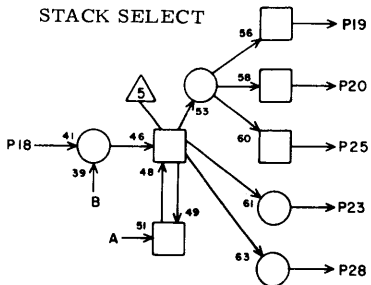
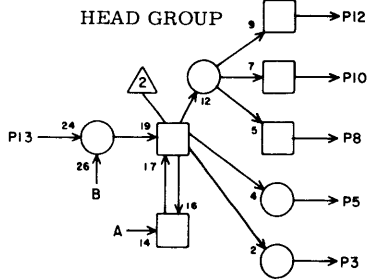
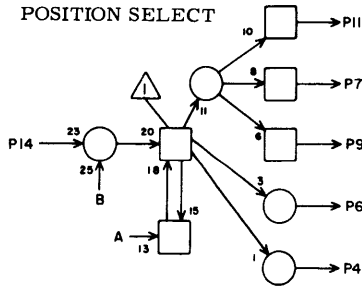
| RV | G | G05 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | G07-24 | 7 |
| 5 | J07- 4 | 13 |
| 6 | J07- 2 | 13 |
| 7 | H13-10 | 13 |
| 8 | A10-11 | 25 |
| 9 | D08-11 | 13 |
| 10 | H13-12 | 13 |
| 11 | E02- 5 | 11 |
| 12 | F06- 7 | 7 |
| 13 | G06-10 | 5 |
| 14 | G06- 7 | 5 |
| 15 | - | |
| 16 | E05-16 | 9 |
| 17 | - | |
| 18 | G06-19 | 5 |
| 19 | A07-14 | 23 |
| 20 | - | |
| 21 | - | |
| 22 | - | |
| 23 | A07-15 | 25 |
| 24 | - | |
| 25 | G01-24 | 7 |
| 26 | - | |
| 27 | - | |
| 28 | G01-18 | 7 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600

60227300 F

LS 63057900
ASSY

B
REV



PD RV G G06

| RV | G | G06 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | G05-14 | 5 |
| 8 | G07-28 | 5 |
| 9 | G07-22 | 5 |
| 10 | G05-13 | 5 |
| 11 | J07-21 | 13 |
| 12 | J07-22 | 13 |
| 13 | A10- 1 | 25 |
| 14 | D08- 1 | 15 |
| 15 | - | |
| 16 | E05-13 | 11 |
| 17 | E13-16 | 13 |
| 18 | F09-11 | 9 |
| 19 | G05-18 | 5 |
| 20 | D02-24 | 15 |
| 21 | - | |
| 22 | E12- 3 | 15 |
| 23 | D02-18 | 15 |
| 24 | - | |
| 25 | D02-27 | 15 |
| 26 | - | |
| 27 | - | |
| 28 | D02-21 | 15 |

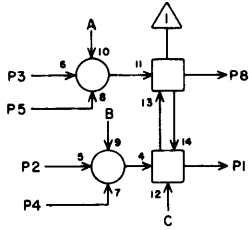
JACK PIN LG
CIRCUIT SPECIFICATION 11827600

60227300 F

LS 63040400
ASSY

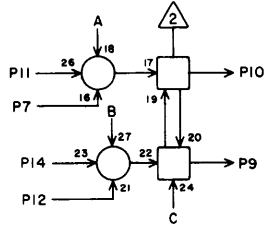


1XXX
X0XX



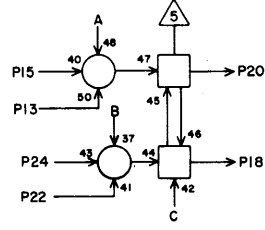
READ 1

1XXX
X1XX



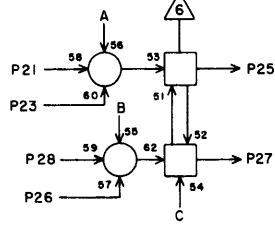
WRITE I

1XXX
X4XX



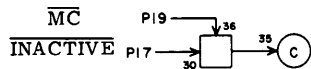
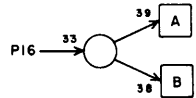
POSITION

1XXX
X6XX



HG

T50



| AE | RV | G | G07 |
|----|----|--------|-----|
| | 1 | J07-15 | 13 |
| | 2 | C10- 5 | 17 |
| | 3 | K08-18 | 17 |
| | 4 | G07- X | 2 |
| | 5 | I03-16 | 13 |
| | 6 | - | |
| | 7 | I04-16 | 11 |
| | 8 | E12-23 | 11 |
| | 9 | J07-17 | 13 |
| | 10 | G04-23 | 7 |
| | 11 | K08-20 | 17 |
| | 12 | G07- X | 2 |
| | 13 | H14-12 | 11 |
| | 14 | G03- 8 | 7 |
| | 15 | K08-16 | 15 |
| | 16 | J09-16 | 13 |
| | 17 | F11-27 | 9 |
| | 18 | | |
| | 19 | H13-19 | 13 |
| | 20 | G03- 2 | 9 |
| | 21 | K08-22 | 15 |
| | 22 | G06- 9 | 5 |
| | 23 | H14-13 | 11 |
| | 24 | G05- 4 | 7 |
| | 25 | 807- 1 | 21 |
| | 26 | G07- X | 2 |
| | 27 | A10- 6 | 25 |
| | 28 | G06- 8 | 5 |

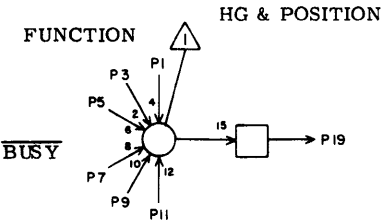
JACK PIN LG
CIRCUIT SPECIFICATION 11827600

60227300 H

LS 63063400
ASSY

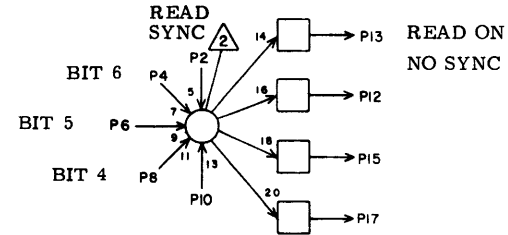


T8
RV G G08



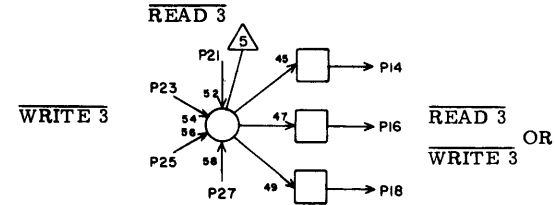
FUNCTION

HG & POSITION



READ SYNC

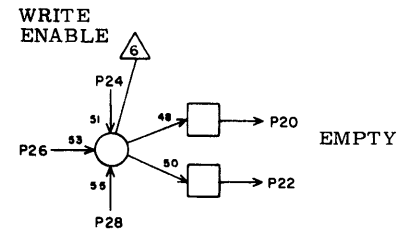
READ ON
NO SYNC



READ 3

WRITE 3

READ 3
OR
WRITE 3



WRITE ENABLE

EMPTY

JACK PIN LG
CIRCUIT SPECIFICATION 11827600

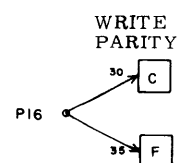
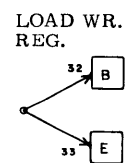
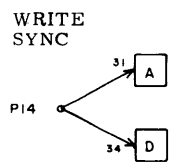
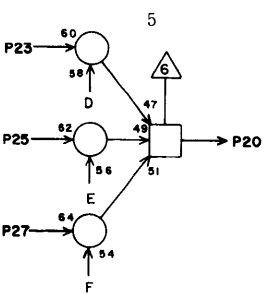
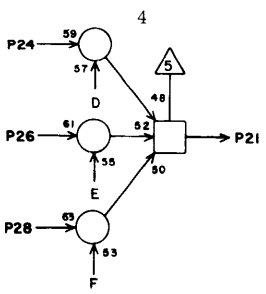
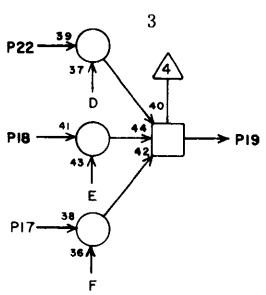
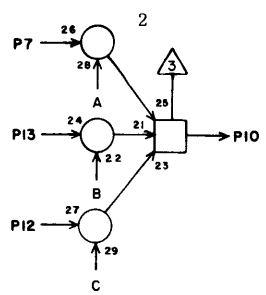
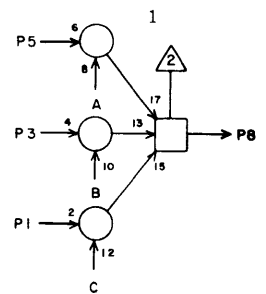
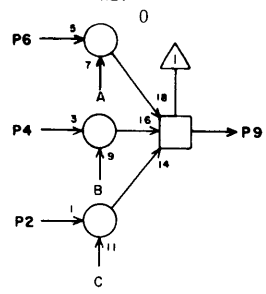
60227300 H

LS 63063700
ASSY REV

WRITE FAN-IN GATES
BITS 0 - 5

TE

RV G G09



JACK PIN LG
CIRCUIT SPECIFICATION 11827600

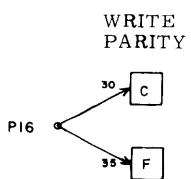
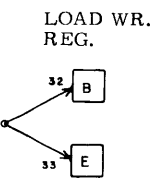
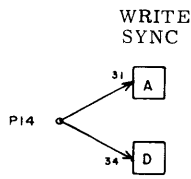
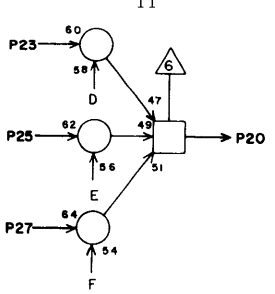
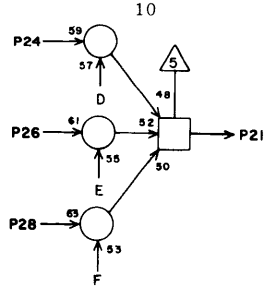
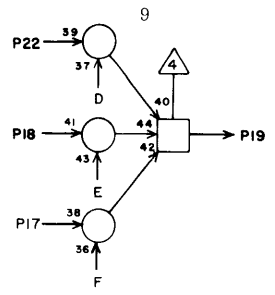
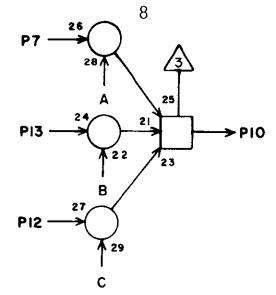
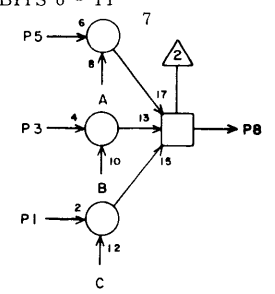
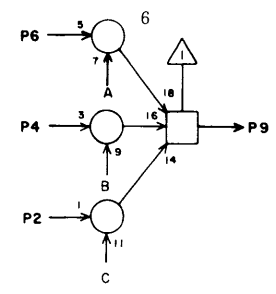
60227300 F

LS 63063700
ASSY REV

WRITE FAN-IN GATES
BITS 6 - 11

TE

RV G G10

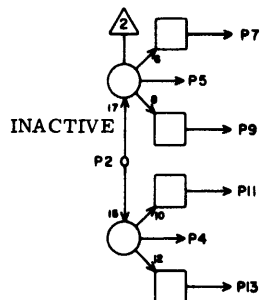
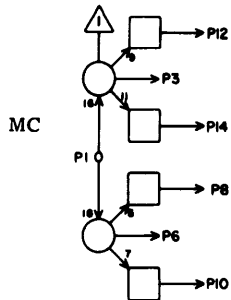


JACK PIN LG
CIRCUIT SPECIFICATION 11827600

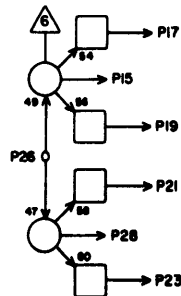
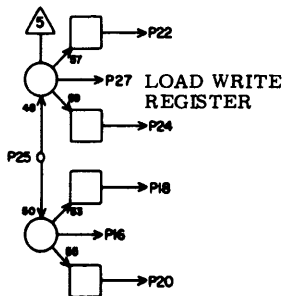
60227300 F

LS 63042900 **B**
 ASSY REV

| CX | RV | 1611 |
|----|--------|------|
| 1 | I05-28 | 15 |
| 2 | I06-21 | 13 |
| 3 | F04-25 | 11 |
| 4 | - | - |
| 5 | H13-20 | 11 |
| 6 | H13-18 | 11 |
| 7 | F08-2 | 9 |
| 8 | - | - |
| 9 | I05-10 | 13 |
| 10 | - | - |
| 11 | F08-23 | 7 |
| 12 | - | - |
| 13 | F08-7 | 9 |
| 14 | - | - |
| 15 | D07-17 | 15 |
| 16 | G10-15 | 5 |
| 17 | D05-7 | 17 |
| 18 | - | - |
| 19 | D05-22 | 15 |
| 20 | - | - |
| 21 | C16-7 | 21 |
| 22 | G12-14 | 5 |
| 23 | C06-22 | 19 |
| 24 | - | - |
| 25 | H13-3 | 7 |
| 26 | G04-19 | 11 |
| 27 | G09-15 | 5 |
| 28 | - | - |



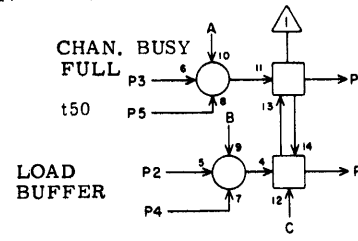
LOAD POSITION REGISTER (UNIT 0 & 1)



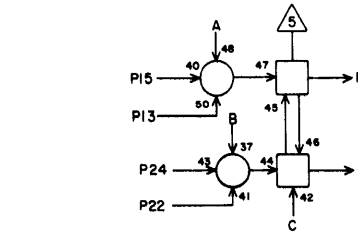
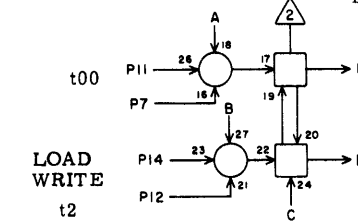
JACK PIN LG
 CIRCUIT SPECIFICATION I1827600
 60227300 H

LS 63040400 **C**
 ASSY REV

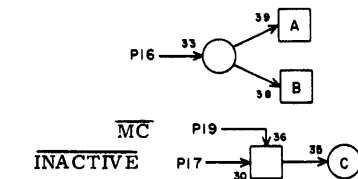
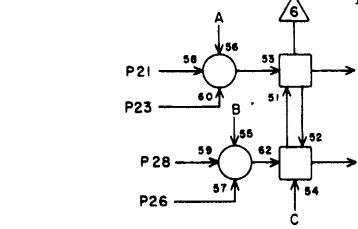
| AE | RV | 1612 |
|----|--------|------|
| 1 | - | - |
| 2 | E11-12 | 9 |
| 3 | G04-13 | 11 |
| 4 | G12-X | 2 |
| 5 | J09-17 | 15 |
| 6 | - | - |
| 7 | F11-9 | 7 |
| 8 | H13-13 | 7 |
| 9 | G13-28 | 5 |
| 10 | - | - |
| 11 | J09-2 | 13 |
| 12 | E07-14 | 11 |
| 13 | G13-7 | 5 |
| 14 | G11-22 | 5 |
| 15 | C10-22 | 17 |
| 16 | G12-X | 2 |
| 17 | F11-21 | 7 |
| 18 | H05-16 | 11 |
| 19 | F04-18 | 13 |
| 20 | F08-24 | 9 |
| 21 | F08-16 | 9 |
| 22 | G12-X | 2 |
| 23 | J09-21 | 13 |
| 24 | H05-10 | 11 |
| 25 | E13-2 | 11 |
| 26 | E10-21 | 11 |
| 27 | - | - |
| 28 | G12-X | 2 |



BUFFER LOADED



EMPTY



JACK PIN LG
 CIRCUIT SPECIFICATION I1827600
 60227300 F

LS 63064000
ASSY REV

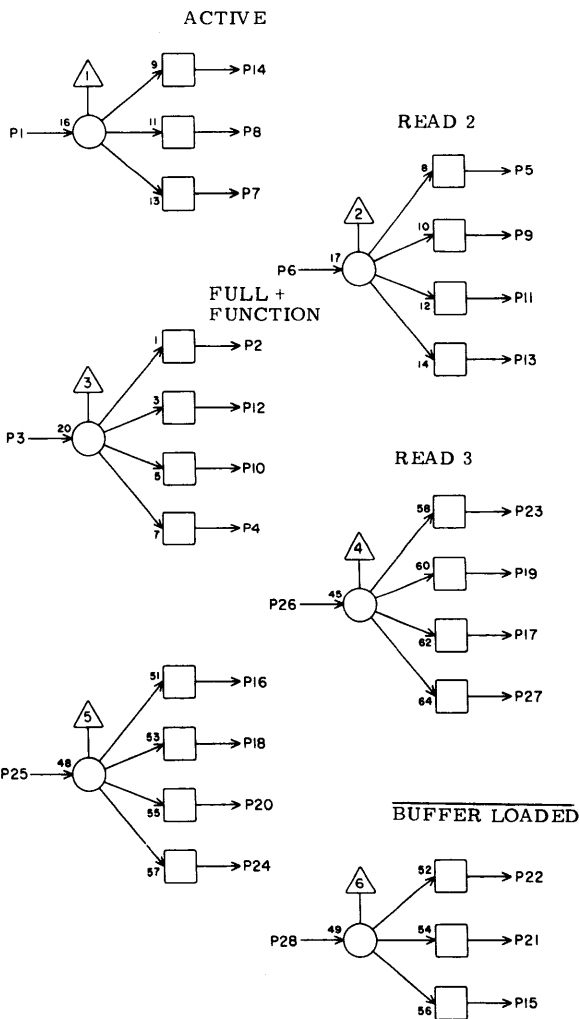
TH

LS 63057800
ASSY REV

PARITY REGISTER 1
BITS 0 - 3

P RV

1G14

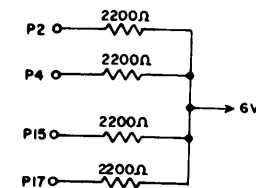
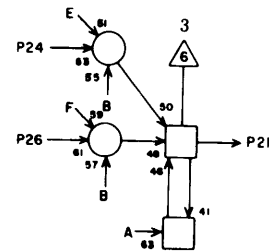
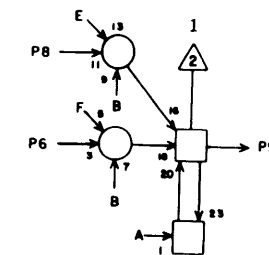
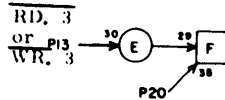
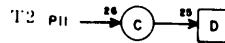
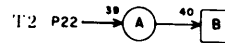
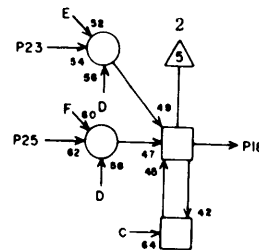
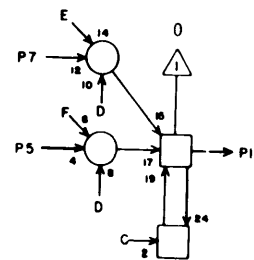


RV 1G13

| | | |
|----|--------|----|
| 1 | I05- 8 | 15 |
| 2 | H10-16 | 9 |
| 3 | H13- 1 | 7 |
| 4 | - | - |
| 5 | F10-15 | 7 |
| 6 | F10- 3 | 7 |
| 7 | G12-13 | 5 |
| 8 | F03-15 | 9 |
| 9 | - | - |
| 10 | H12-16 | 7 |
| 11 | F07-28 | 11 |
| 12 | H11-16 | 7 |
| 13 | F09-25 | 9 |
| 14 | - | - |
| 15 | H13-15 | 7 |
| 16 | D03- 4 | 19 |
| 17 | - | - |
| 18 | D03- 7 | 19 |
| 19 | D12- 5 | 15 |
| 20 | F13- 5 | 11 |
| 21 | F05-18 | 13 |
| 22 | - | - |
| 23 | F10-22 | 9 |
| 24 | - | - |
| 25 | D09-26 | 15 |
| 26 | F10-26 | 9 |
| 27 | - | - |
| 28 | G12- 9 | 5 |

CIRCUIT SPECIFICATION 11827800

60227300 H



| | | |
|----|--------|----|
| 1 | - | - |
| 2 | G14- 5 | 5 |
| 3 | - | - |
| 4 | G14- 6 | 3 |
| 5 | G14- 2 | 5 |
| 6 | G14- 4 | 3 |
| 7 | F15-10 | 7 |
| 8 | F15- 4 | 7 |
| 9 | E15-12 | 9 |
| 10 | - | - |
| 11 | E04-20 | 17 |
| 12 | - | - |
| 13 | G08-14 | 9 |
| 14 | E15- 5 | 11 |
| 15 | G14-25 | 5 |
| 16 | - | - |
| 17 | G14-26 | 5 |
| 18 | E15-21 | 9 |
| 19 | - | - |
| 20 | G14- X | 2 |
| 21 | E15-24 | 9 |
| 22 | E04-18 | 17 |
| 23 | F15-14 | 7 |
| 24 | F15-17 | 7 |
| 25 | G14-15 | 5 |
| 26 | G14-17 | 5 |
| 27 | - | - |
| 28 | - | - |

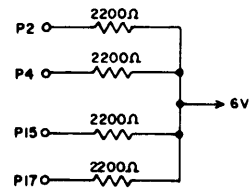
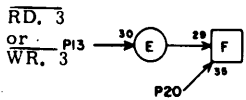
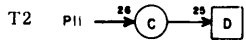
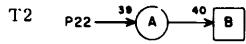
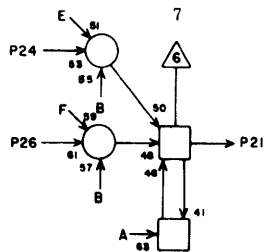
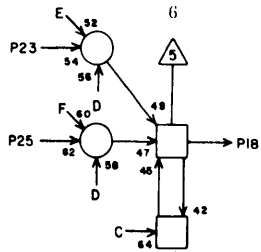
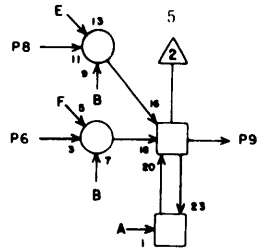
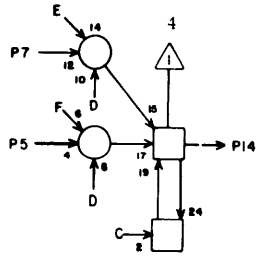
JACK PIN LG
CIRCUIT SPECIFICATION 11827800

60227300 F

LS 63067800 **C**
 ASSY REV

PARITY REGISTER 1
 BITS 4-7

PC RV 1G15



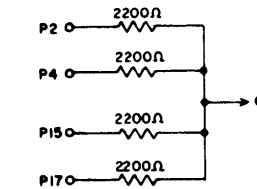
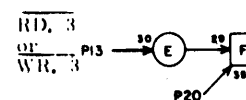
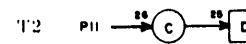
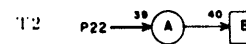
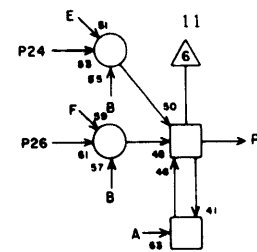
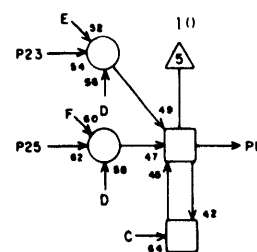
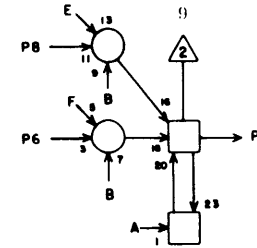
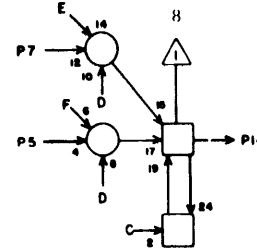
| | | |
|----|--------|----|
| 1 | - | |
| 2 | G15- 5 | 5 |
| 3 | - | |
| 4 | G15- 6 | 3 |
| 5 | G15- 2 | 5 |
| 6 | G15- 4 | 3 |
| 7 | F15-27 | 5 |
| 8 | F15-21 | 5 |
| 9 | E16- 8 | 11 |
| 10 | - | |
| 11 | E04-17 | 17 |
| 12 | - | |
| 13 | G08-16 | 11 |
| 14 | F15-23 | 9 |
| 15 | G15-25 | 5 |
| 16 | - | |
| 17 | G15-26 | 5 |
| 18 | E16- 5 | 11 |
| 19 | - | |
| 20 | G15- X | 2 |
| 21 | E16-12 | 11 |
| 22 | E04-22 | 19 |
| 23 | F16-10 | 7 |
| 24 | F16- 4 | 9 |
| 25 | G15-15 | 5 |
| 26 | G15-17 | 5 |
| 27 | - | |
| 28 | - | |

JACK PIN LG
 CIRCUIT SPECIFICATION 1027600
 60227300 F

LS 63067800 **C**
 ASSY REV

PARITY REGISTER 1
 BITS 8-11

PC RV 1G16



| | | |
|----|--------|----|
| 1 | - | |
| 2 | G16- 5 | 5 |
| 3 | - | |
| 4 | G16- 6 | 3 |
| 5 | G16- 2 | 5 |
| 6 | G16- 4 | 3 |
| 7 | F16-14 | 7 |
| 8 | F16-17 | 5 |
| 9 | E16-24 | 9 |
| 10 | - | |
| 11 | E04-21 | 19 |
| 12 | - | |
| 13 | G08-18 | 13 |
| 14 | E16-21 | 9 |
| 15 | G16-25 | 5 |
| 16 | - | |
| 17 | G16-26 | 5 |
| 18 | E16-23 | 9 |
| 19 | - | |
| 20 | G16- X | 2 |
| 21 | E15- 8 | 11 |
| 22 | E04-19 | 19 |
| 23 | F16-27 | 7 |
| 24 | F16-21 | 7 |
| 25 | G16-15 | 5 |
| 26 | G16-17 | 5 |
| 27 | - | |
| 28 | - | |

JACK PIN LG
 CIRCUIT SPECIFICATION 1027600
 60227300 F

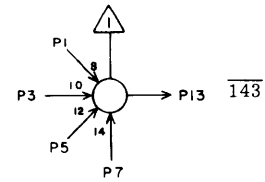
LS 63064100
ASSY

REV

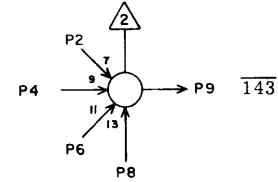
T1

RV G

H04

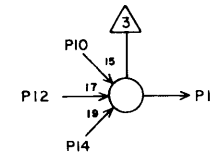


SECTOR
COUNTER 0



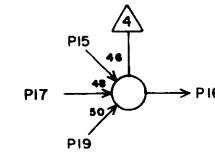
SECTOR
COUNTER 1

BIT 7
STATUS B

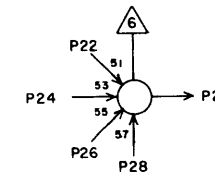
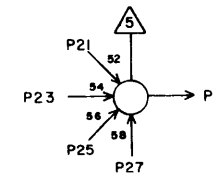


STATUS FULL B

BIT 7
STATUS B



POSITION FULL B



LOST DATA

| RV | G | H04 |
|----|--------|-----|
| 1 | B06-25 | 21 |
| 2 | A06-25 | 25 |
| 3 | B06- 8 | 23 |
| 4 | A06- 8 | 27 |
| 5 | B05- 8 | 23 |
| 6 | A05- 8 | 27 |
| 7 | B05- 9 | 23 |
| 8 | A05- 9 | 27 |
| 9 | D03-26 | 15 |
| 10 | H16-27 | 17 |
| 11 | J02- 1 | 9 |
| 12 | J08-21 | 13 |
| 13 | D03-23 | 15 |
| 14 | H04- X | 2 |
| 15 | H16-16 | 15 |
| 16 | J02- 3 | 9 |
| 17 | J08-22 | 11 |
| 18 | K09-25 | 15 |
| 19 | H04- X | 2 |
| 20 | F08-20 | 11 |
| 21 | I04-13 | 5 |
| 22 | H05-20 | 5 |
| 23 | I03-13 | 7 |
| 24 | H04- X | 2 |
| 25 | H04- X | 2 |
| 26 | H04- X | 2 |
| 27 | H04- X | 2 |
| 28 | H04- X | 2 |

JACK PIN LG

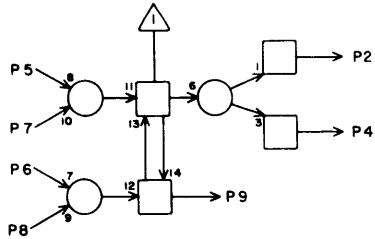
CIRCUIT SPECIFICATION 11827600

60227300 F

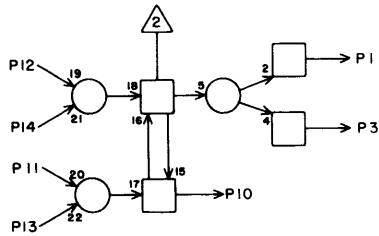
LS 63040000
ASSY

D
REV

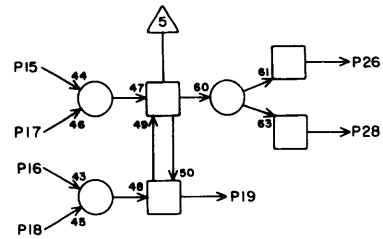
FUNCTION & HG + POSITION



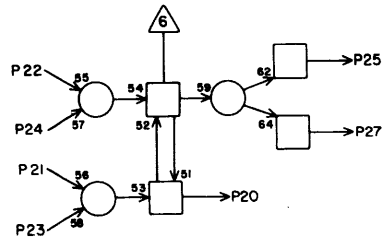
CHANNEL BUSY



END OF BUFFER



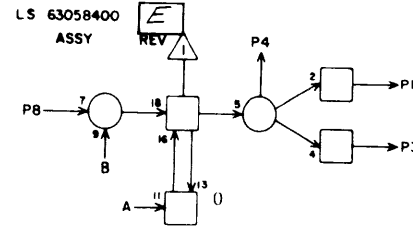
LOST DATA



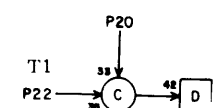
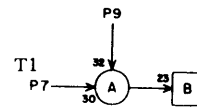
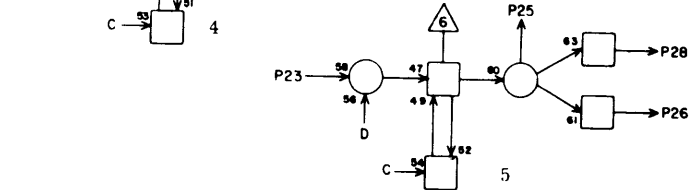
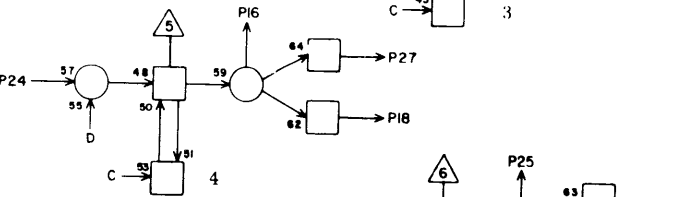
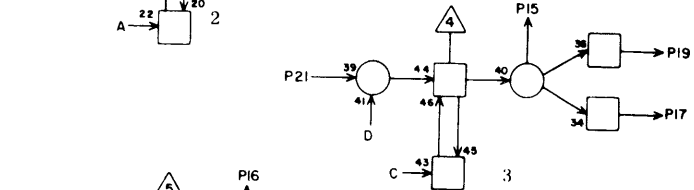
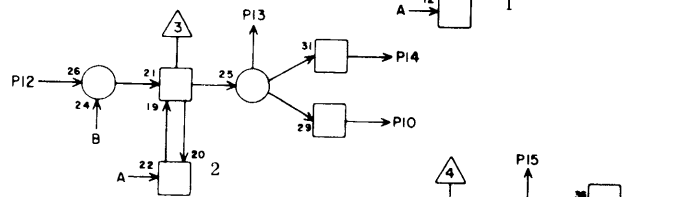
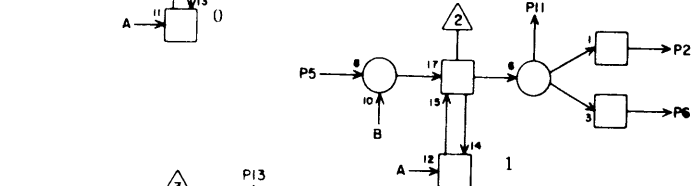
| RV | G | H05 | JACK | PIN | LG |
|----|--------|-----|------|-----|----|
| 1 | C10-25 | 21 | | | |
| 2 | G08- 1 | 9 | | | |
| 3 | H05-17 | 5 | | | |
| 4 | - | | | | |
| 5 | K09-19 | 15 | | | |
| 6 | E11-14 | 15 | | | |
| 7 | H05- X | 2 | | | |
| 8 | H05- X | 2 | | | |
| 9 | - | | | | |
| 10 | G12-24 | 11 | | | |
| 11 | I05- 3 | 5 | | | |
| 12 | K09-14 | 15 | | | |
| 13 | J09-24 | 13 | | | |
| 14 | H05- X | 2 | | | |
| 15 | I05-16 | 7 | | | |
| 16 | G12-18 | 11 | | | |
| 17 | H05- 3 | 5 | | | |
| 18 | H05- X | 2 | | | |
| 19 | O10-24 | 19 | | | |
| 20 | H04-22 | 5 | | | |
| 21 | K09-16 | 13 | | | |
| 22 | H05-26 | 3 | | | |
| 23 | H05- X | 2 | | | |
| 24 | I05-11 | 5 | | | |
| 25 | I13-25 | 13 | | | |
| 26 | H05-22 | 3 | | | |
| 27 | I16-25 | 15 | | | |
| 28 | F08-18 | 11 | | | |

CIRCUIT SPECIFICATION I1827600

60227300 F



WRITE REGISTER
BITS 0 - 5



| RV | G | H06 | JACK | PIN | LG |
|----|--------|-----|------|-----|----|
| 1 | I03- 4 | 9 | | | |
| 2 | I03-10 | 9 | | | |
| 3 | F13- 6 | 13 | | | |
| 4 | - | | | | |
| 5 | G09- 8 | 7 | | | |
| 6 | F13- 5 | 13 | | | |
| 7 | E04- 4 | 72 | | | |
| 8 | G09- 9 | 9 | | | |
| 9 | H06- X | 2 | | | |
| 10 | F13- 7 | 15 | | | |
| 11 | - | | | | |
| 12 | G09-10 | 9 | | | |
| 13 | - | | | | |
| 14 | I03- 1 | 7 | | | |
| 15 | - | | | | |
| 16 | - | | | | |
| 17 | F13-22 | 13 | | | |
| 18 | F13-24 | 13 | | | |
| 19 | I03-28 | 9 | | | |
| 20 | H06- X | 2 | | | |
| 21 | G09-19 | 9 | | | |
| 22 | E04- 6 | 72 | | | |
| 23 | G09-20 | 9 | | | |
| 24 | G09-21 | 9 | | | |
| 25 | - | | | | |
| 26 | F13-23 | 15 | | | |
| 27 | I03-22 | 9 | | | |
| 28 | I03-25 | 7 | | | |

CIRCUIT SPECIFICATION I1827600

60227300 F

LS 63058400
ASSY

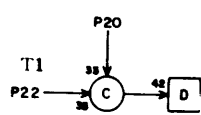
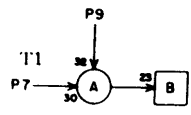
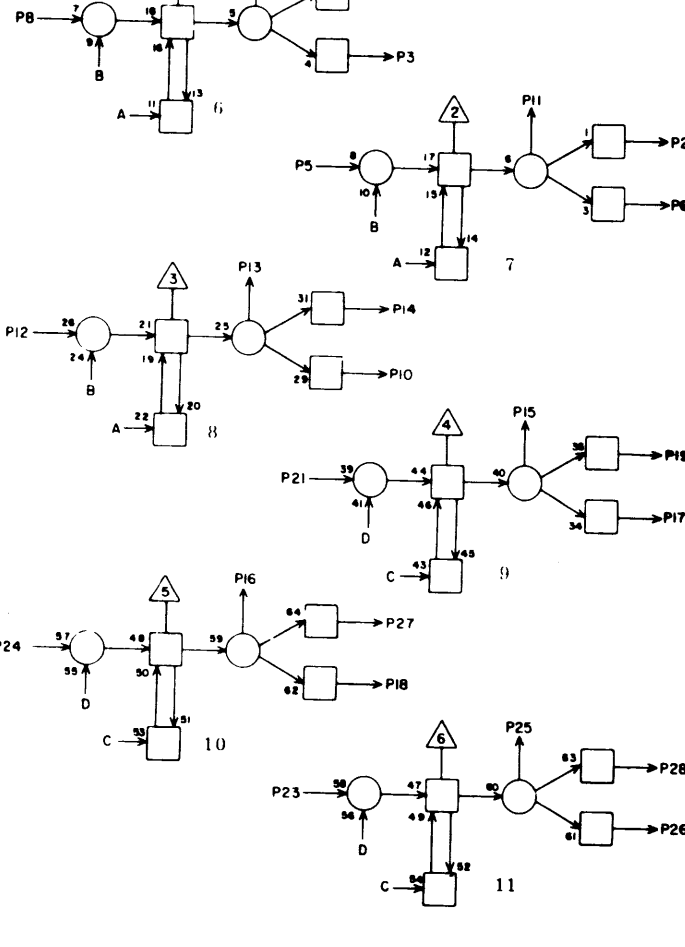
REV E

WRITE REGISTER
BITS 6-11

| PJ | RV | G | H07 |
|----|----|--------|-----|
| | 1 | I04-4 | 9 |
| | 2 | I04-10 | 9 |
| | 3 | F14-6 | 13 |
| | 4 | - | - |
| | 5 | G10-8 | 7 |
| | 6 | F14-5 | 13 |
| | 7 | E04-9 | 72 |
| | 8 | G10-9 | 9 |
| | 9 | H07-X | 2 |
| | 10 | F14-7 | 15 |
| | 11 | - | - |
| | 12 | G10-18 | 9 |
| | 13 | - | - |
| | 14 | I04-1 | 7 |
| | 15 | - | - |
| | 16 | - | - |
| | 17 | F14-22 | 13 |
| | 18 | F14-24 | 13 |
| | 19 | I04-28 | 9 |
| | 20 | H07-X | 2 |
| | 21 | G10-19 | 9 |
| | 22 | E04-11 | 72 |
| | 23 | G10-20 | 9 |
| | 24 | G10-21 | 9 |
| | 25 | - | - |
| | 26 | F14-23 | 15 |
| | 27 | I04-22 | 9 |
| | 28 | I04-25 | 7 |

JACK PIN LG
CIRCUIT SPECIFICATION 11027600

60227300 F



LS 63058400
ASSY

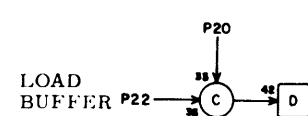
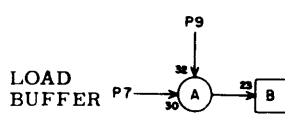
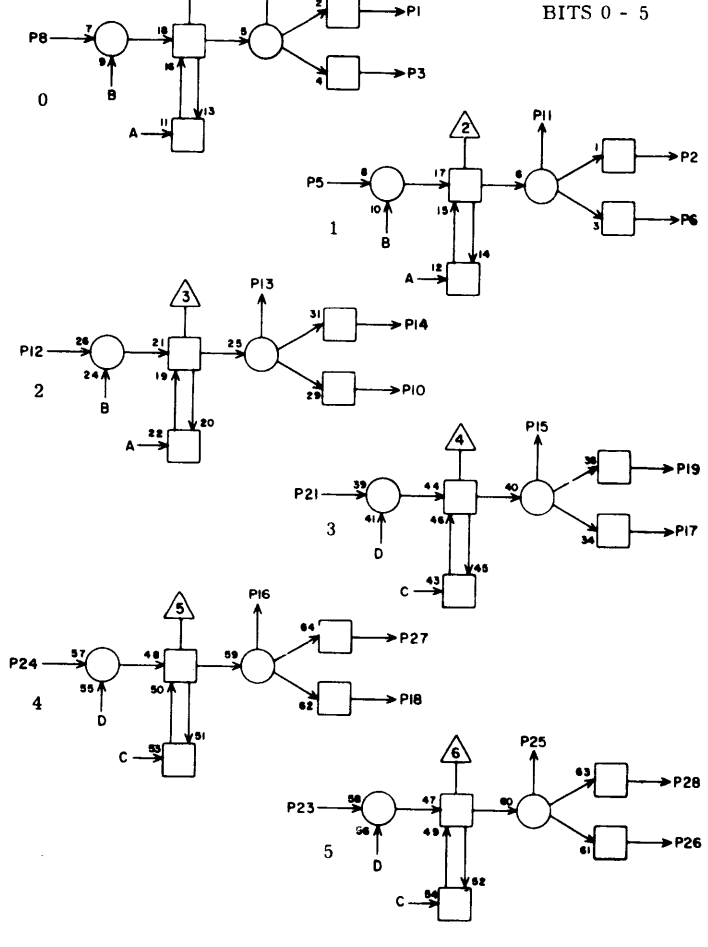
REV E

BUFFER REGISTER
BITS 0 - 5

| PJ | RV | G | H08 |
|----|----|--------|-----|
| | 1 | G09-4 | 7 |
| | 2 | G09-3 | 7 |
| | 3 | - | - |
| | 4 | - | - |
| | 5 | H10-3 | 5 |
| | 6 | - | - |
| | 7 | E11-2 | 15 |
| | 8 | H10-4 | 5 |
| | 9 | H08-X | 2 |
| | 10 | - | - |
| | 11 | - | - |
| | 12 | H10-28 | 7 |
| | 13 | - | - |
| | 14 | G09-13 | 7 |
| | 15 | - | - |
| | 16 | - | - |
| | 17 | - | - |
| | 18 | - | - |
| | 19 | G09-18 | 7 |
| | 20 | H08-X | 2 |
| | 21 | H10-27 | 5 |
| | 22 | E11-4 | 15 |
| | 23 | H11-3 | 7 |
| | 24 | H11-4 | 7 |
| | 25 | - | - |
| | 26 | - | - |
| | 27 | G09-26 | 7 |
| | 28 | G09-25 | 7 |

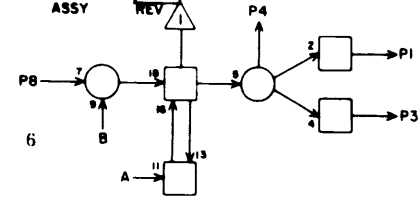
JACK PIN LG
CIRCUIT SPECIFICATION 11027600

60227300 F

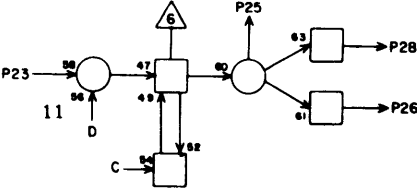
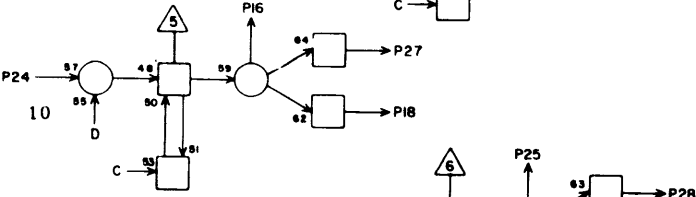
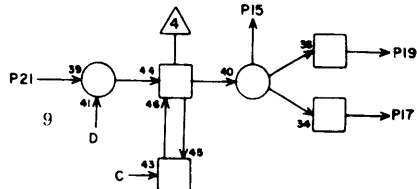
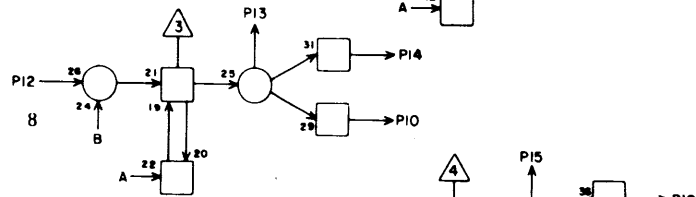
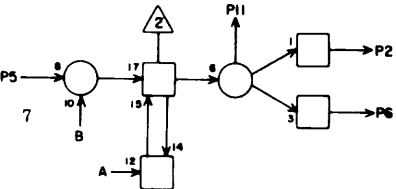


LS 63058400
ASSY

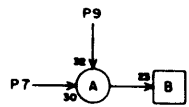
REV **E**



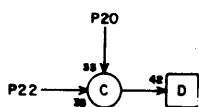
BUFFER REGISTER
BITS 6-11



LOAD
BUFFER



LOAD
BUFFER



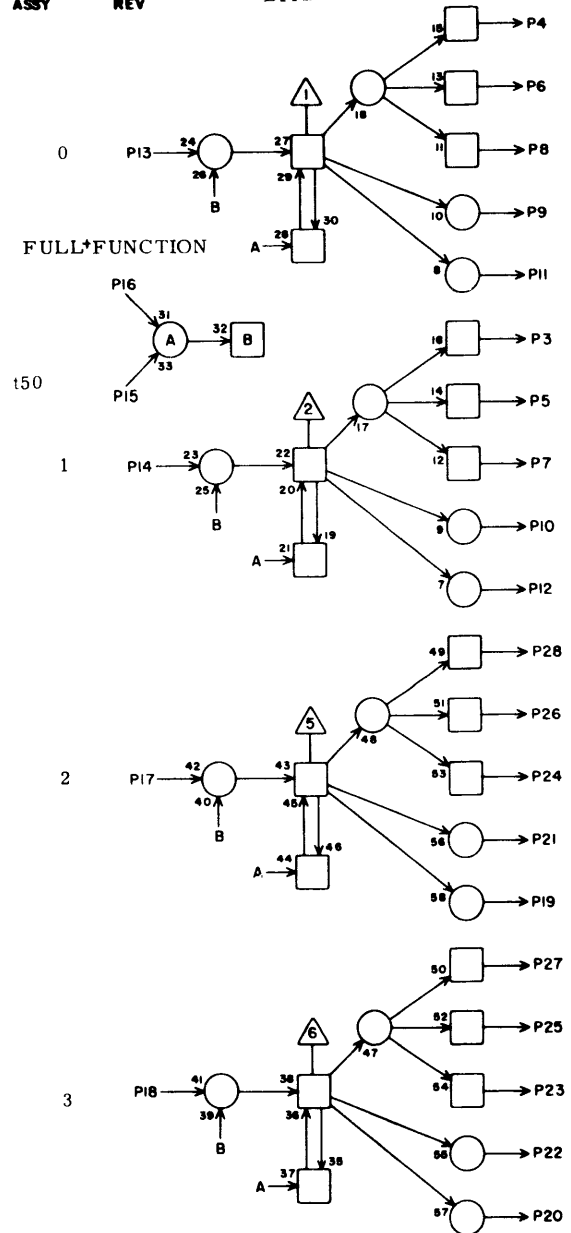
| PJ | RV | G | H89 |
|----|----|--------|-----|
| | 1 | G10-4 | 7 |
| | 2 | G10-3 | 7 |
| | 3 | - | |
| | 4 | - | |
| | 5 | H11-27 | 7 |
| | 6 | - | |
| | 7 | E11-6 | 13 |
| | 8 | H11-28 | 7 |
| | 9 | H09-X | 2 |
| | 10 | - | |
| | 11 | - | |
| | 12 | H12-4 | 7 |
| | 13 | - | |
| | 14 | G10-13 | 7 |
| | 15 | - | |
| | 16 | - | |
| | 17 | - | |
| | 18 | - | |
| | 19 | G10-18 | 7 |
| | 20 | H09-X | 2 |
| | 21 | H12-3 | 7 |
| | 22 | E11-9 | 15 |
| | 23 | H12-27 | 7 |
| | 24 | H12-28 | 7 |
| | 25 | - | |
| | 26 | - | |
| | 27 | G10-26 | 7 |
| | 28 | G10-25 | 7 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63058900
ASSY

REV **B**

HOLDING REGISTER
BITS 0-3

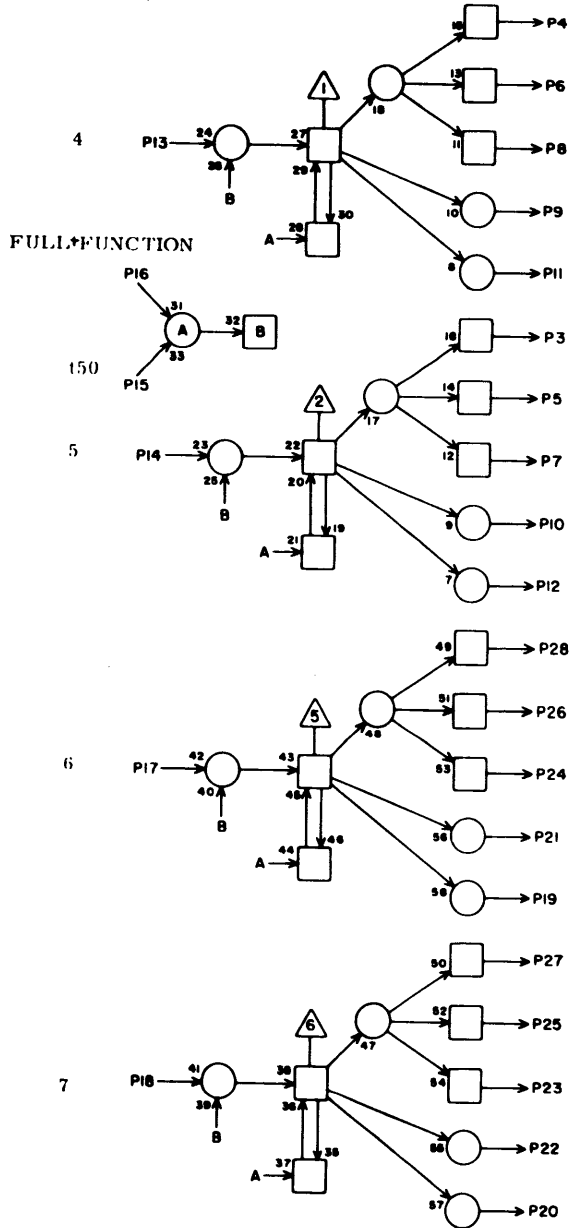


FULL FUNCTION

| PO | RV | G | H18 |
|----|----|--------------------------------|-----|
| | 1 | - | |
| | 2 | - | |
| | 3 | H08-5 | 5 |
| | 4 | H08-8 | 5 |
| | 5 | D05-5 | 19 |
| | 6 | D05-8 | 19 |
| | 7 | C06-5 | 21 |
| | 8 | C06-8 | 21 |
| | 9 | C08-22 | 19 |
| | 10 | C08-21 | 19 |
| | 11 | - | |
| | 12 | - | |
| | 13 | I07-9 | 7 |
| | 14 | I07-10 | 7 |
| | 15 | J09-18 | 11 |
| | 16 | G13-2 | 9 |
| | 17 | I07-21 | 9 |
| | 18 | I07-8 | 7 |
| | 19 | I10-5 | 5 |
| | 20 | F07-2 | 13 |
| | 21 | C08-23 | 21 |
| | 22 | C08-24 | 21 |
| | 23 | C06-21 | 21 |
| | 24 | C06-12 | 23 |
| | 25 | D05-21 | 19 |
| | 26 | D05-12 | 21 |
| | 27 | H08-21 | 5 |
| | 28 | H08-12 | 7 |
| | | JACK PIN LG | |
| | | CIRCUIT SPECIFICATION 11827600 | |
| | | 60227300 F | |

LS 63058900
ASSY **B**
REV

HOLDING REGISTER
BITS 4 - 7

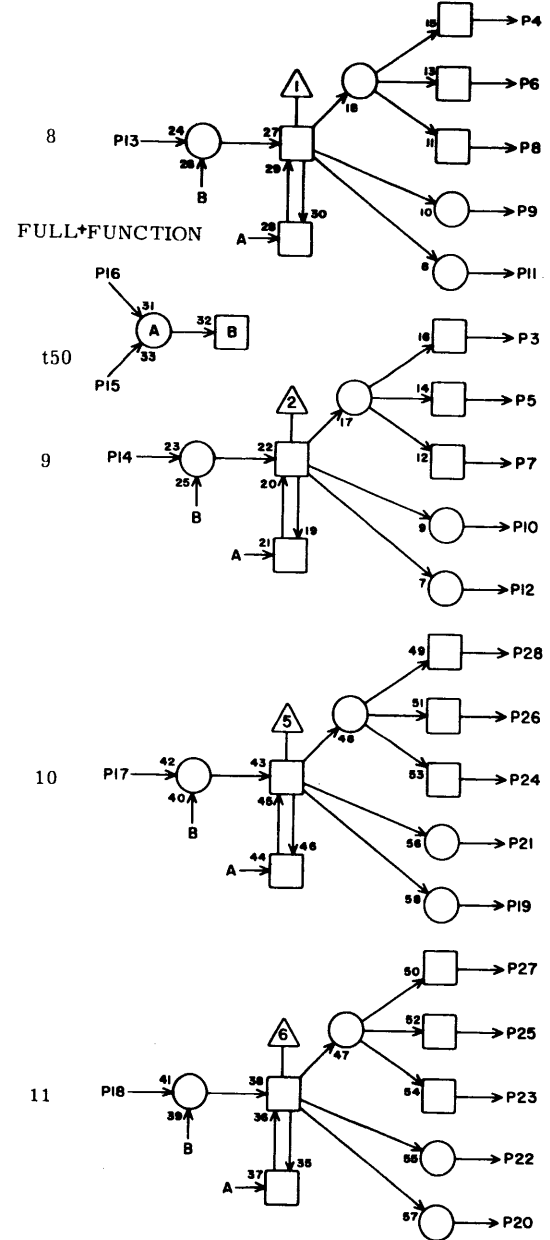


| PO | RV | 1M11 |
|----|--------|------|
| 1 | - | |
| 2 | - | |
| 3 | H08-23 | 7 |
| 4 | H08-24 | 7 |
| 5 | D05-23 | 17 |
| 6 | I10-10 | 7 |
| 7 | C06-23 | 21 |
| 8 | F09-25 | 9 |
| 9 | D10-13 | 15 |
| 10 | C08-26 | 19 |
| 11 | D10-18 | 15 |
| 12 | F07- 3 | 11 |
| 13 | I07-19 | 9 |
| 14 | I07-20 | 9 |
| 15 | J09-20 | 11 |
| 16 | G13-12 | 7 |
| 17 | J08-10 | 11 |
| 18 | J08-18 | 11 |
| 19 | - | |
| 20 | - | |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | K10-25 | 13 |
| 25 | - | |
| 26 | A09- 8 | 29 |
| 27 | H09- 5 | 7 |
| 28 | H09- 8 | 7 |

JACK PIN LG
CIRCUIT SPECIFICATION 1B27600
60227300 G

LS 63058900
ASSY **B**
REV

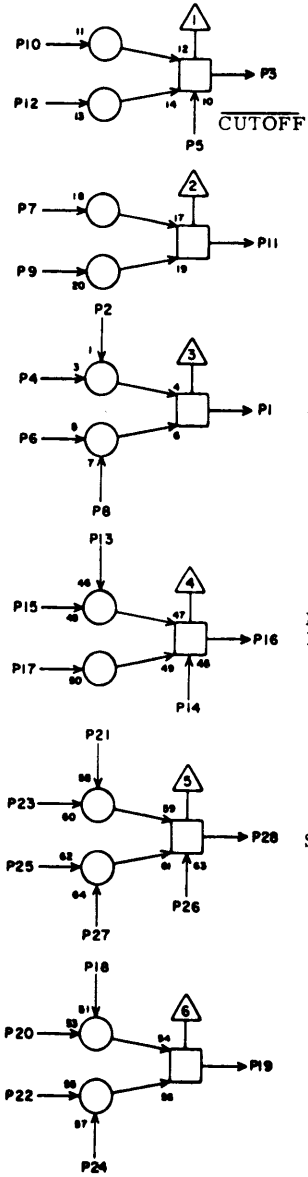
HOLDING REGISTER
BITS 8 - 11



| PO | RV | 1M12 |
|----|--------|------|
| 1 | - | |
| 2 | - | |
| 3 | H09-21 | 7 |
| 4 | H09-12 | 7 |
| 5 | - | |
| 6 | - | |
| 7 | - | |
| 8 | - | |
| 9 | - | |
| 10 | - | |
| 11 | - | |
| 12 | - | |
| 13 | J08- 9 | 11 |
| 14 | I08- 8 | 9 |
| 15 | J09-22 | 11 |
| 16 | G13-10 | 7 |
| 17 | I08-19 | 9 |
| 18 | I08-20 | 9 |
| 19 | - | |
| 20 | - | |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | - | |
| 25 | - | |
| 26 | - | |
| 27 | H09-23 | 7 |
| 28 | H09-24 | 7 |

JACK PIN LG
CIRCUIT SPECIFICATION 1B27600
60227300 F

LS 63060700
ASSY REV



LOAD HOLDING REGISTER

FULL + FUNCTION LOAD BUFFER

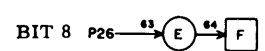
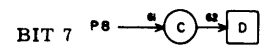
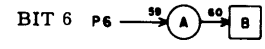
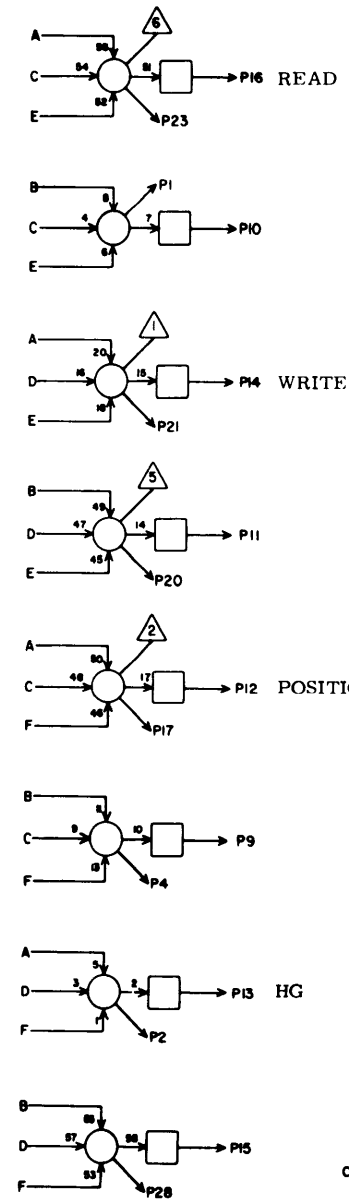
SET READ 2

READ SYNC
160₈-14

| Q# | RV | G | H13 |
|----|--------|---|-----|
| 1 | G13- | 3 | 7 |
| 2 | C10-16 | | 21 |
| 3 | G11-25 | | 7 |
| 4 | J02-22 | | 19 |
| 5 | F09- | 2 | 13 |
| 6 | I06-20 | | 13 |
| 7 | - | | |
| 8 | H13- | X | 2 |
| 9 | - | | |
| 10 | G05- | 7 | 13 |
| 11 | - | | |
| 12 | G05-10 | | 13 |
| 13 | G12- | 8 | 7 |
| 14 | H13- | X | 2 |
| 15 | G13-15 | | 7 |
| 16 | F12-14 | | 11 |
| 17 | G08-19 | | 9 |
| 18 | G11-6 | | 11 |
| 19 | G07-19 | | 13 |
| 20 | G11-5 | | 11 |
| 21 | E12-19 | | 13 |
| 22 | C16-17 | | 19 |
| 23 | H13- | X | 2 |
| 24 | - | | |
| 25 | H13- | X | 2 |
| 26 | H13- | X | 2 |
| 27 | G08-13 | | 11 |
| 28 | F10-12 | | 13 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 H

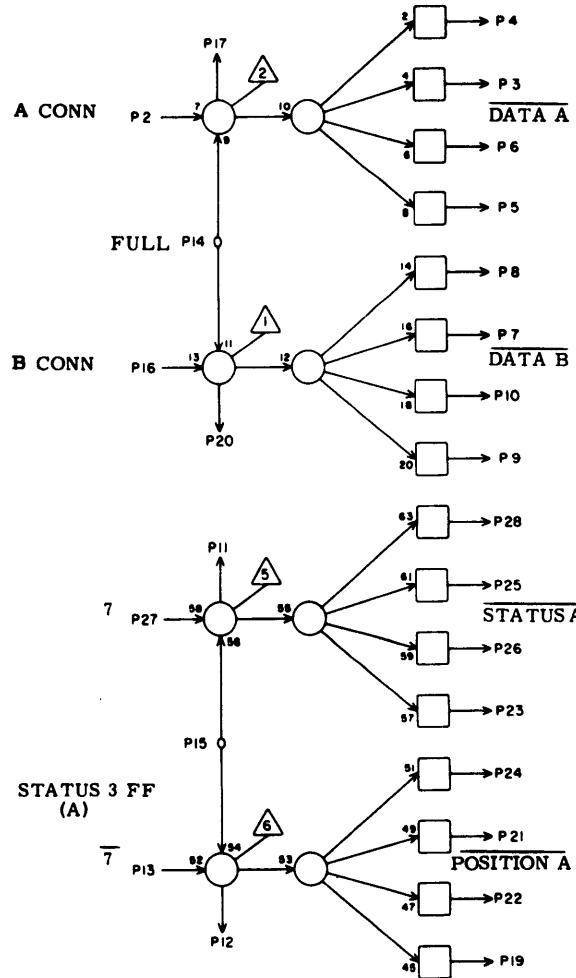
LS 63049300
ASSY REV



| IV | RV | G | H14 |
|----|--------|---|-----|
| 1 | I03-14 | | 17 |
| 2 | E09- | 1 | 15 |
| 3 | - | | |
| 4 | - | | |
| 5 | - | | |
| 6 | J08-12 | | 13 |
| 7 | - | | |
| 8 | J08-16 | | 13 |
| 9 | - | | |
| 10 | - | | |
| 11 | - | | |
| 12 | G07-13 | | 11 |
| 13 | G07-23 | | 11 |
| 14 | - | | |
| 15 | - | | |
| 16 | - | | |
| 17 | E09- | 3 | 17 |
| 18 | - | | |
| 19 | - | | |
| 20 | I04-14 | | 15 |
| 21 | I04-19 | | 15 |
| 22 | - | | |
| 23 | I03-19 | | 15 |
| 24 | - | | |
| 25 | - | | |
| 26 | J08- | 5 | 11 |
| 27 | - | | |
| 28 | - | | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

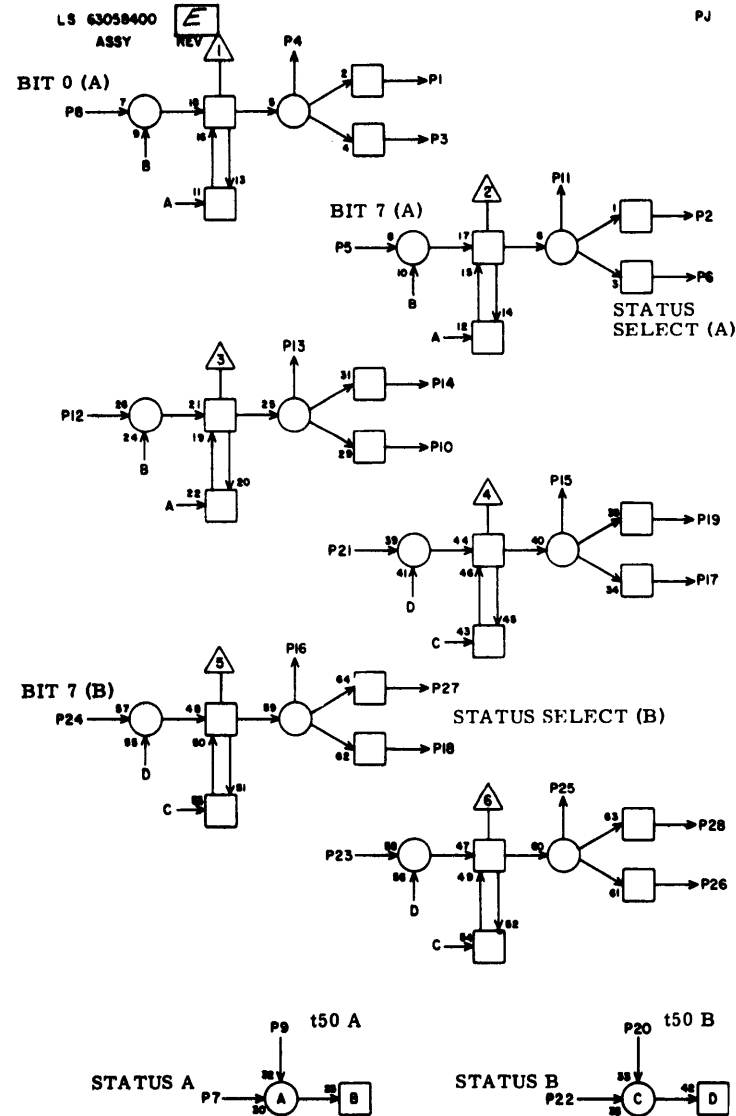
LS 630532 ASSY 6 REV



| KL | RV | G | H15 |
|----|-----|--------|-----|
| | 1 | - | |
| | 2 | J10-18 | 13 |
| | 3 | I12-11 | 9 |
| | 4 | I11-11 | 9 |
| | 5 | I13-11 | 7 |
| | 6 | I09-14 | 11 |
| | 7 | I15-11 | 7 |
| | 8 | I14-11 | 7 |
| | 9 | I16-11 | 7 |
| | 10 | I10-14 | 11 |
| | 11 | - | |
| | 12 | - | |
| | 13 | H16-11 | 5 |
| | 14 | F11-19 | 11 |
| | 15 | J08-8 | 13 |
| | 16 | J10-11 | 11 |
| | 17 | - | |
| | 18 | - | |
| | 19 | - | |
| | 20 | - | |
| | 21 | I12-15 | 7 |
| | *22 | I13-15 | 7 |
| | 23 | - | |
| | 24 | I11-15 | 9 |
| | 25 | I12-16 | 9 |
| | 26 | I13-16 | 7 |
| | 27 | H16-2 | 5 |
| | 28 | I11-16 | 9 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 G

* Standard Option 10037



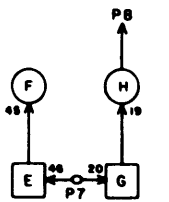
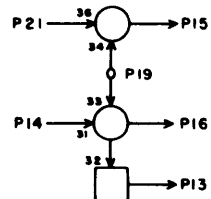
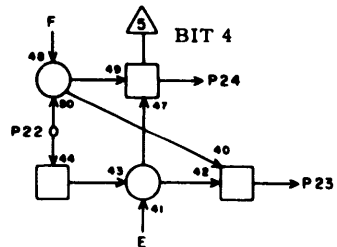
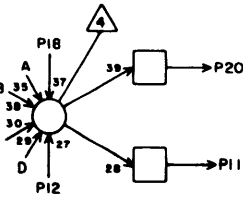
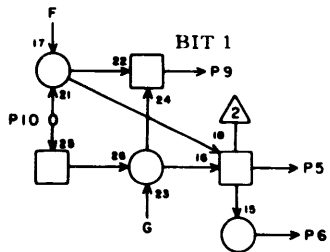
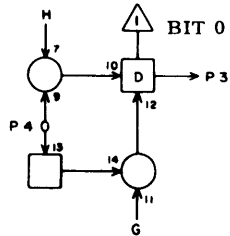
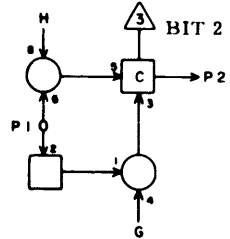
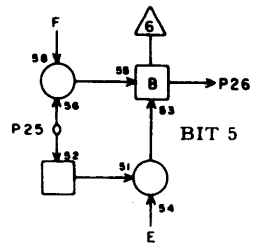
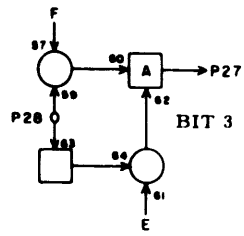
| RV | G | H16 |
|-----|--------|-----|
| 1 | I10-2 | 11 |
| 2 | H15-27 | 5 |
| 3 | - | |
| 4 | I09-2 | 11 |
| 5 | L08-24 | 23 |
| 6 | - | |
| 7 | K08-12 | 17 |
| *8 | C02-4 | 23 |
| 8 | L07-7 | 21 |
| 9 | J11-20 | 13 |
| 10 | - | |
| 11 | H15-13 | 5 |
| 12 | L08-9 | 21 |
| 13 | - | |
| 14 | K04-5 | 21 |
| 15 | I09-8 | 13 |
| 16 | H04-15 | 15 |
| 17 | - | |
| 18 | - | |
| 19 | I10-8 | 11 |
| 20 | J14-20 | 11 |
| *21 | C02-15 | 23 |
| 21 | L12-7 | 17 |
| 22 | K08-11 | 15 |
| 23 | L13-9 | 17 |
| 24 | L13-24 | 17 |
| 25 | - | |
| 26 | - | |
| 27 | H04-10 | 17 |
| 28 | K04-15 | 21 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

* Standard Option 10037

LS 63053800
ASSY

3
REV



WRITE LOCK

KS

RV G

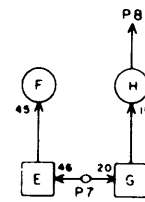
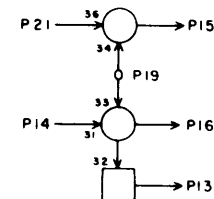
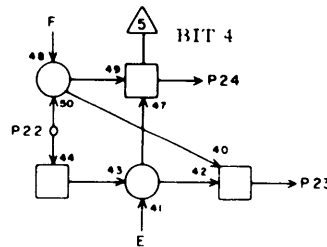
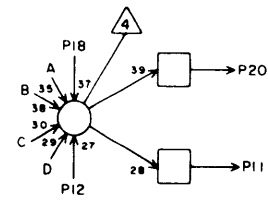
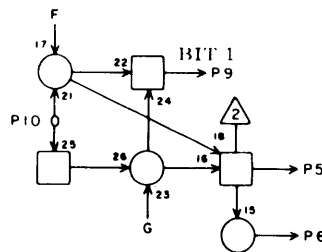
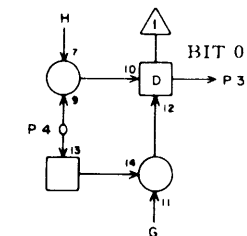
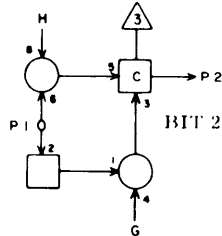
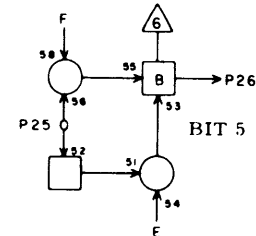
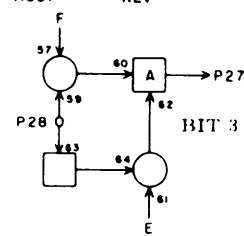
I03

| | | |
|----|--------|----|
| 1 | H06-14 | 7 |
| 2 | L01-24 | 15 |
| 3 | L01-7 | 13 |
| 4 | H06-1 | 9 |
| 5 | - | - |
| 6 | - | - |
| 7 | A09-4 | 31 |
| 8 | I04-7 | 5 |
| 9 | L01-17 | 15 |
| 10 | H06-2 | 9 |
| 11 | - | - |
| 12 | - | - |
| 13 | H04-23 | 7 |
| 14 | H14-1 | 17 |
| 15 | - | - |
| 16 | G07-5 | 13 |
| 17 | - | - |
| 18 | - | - |
| 19 | H14-23 | 15 |
| 20 | - | - |
| 21 | - | - |
| 22 | H06-27 | 9 |
| 23 | - | - |
| 24 | L02-17 | 13 |
| 25 | H06-28 | 7 |
| 26 | L02-24 | 13 |
| 27 | L02-7 | 11 |
| 28 | H06-19 | 9 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63053800
ASSY

3
REV



KS

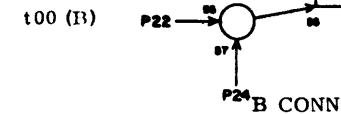
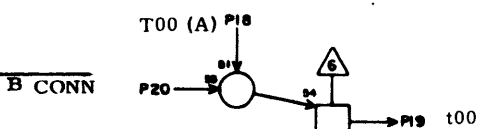
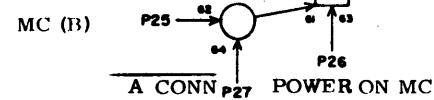
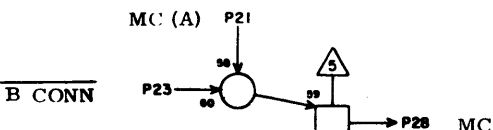
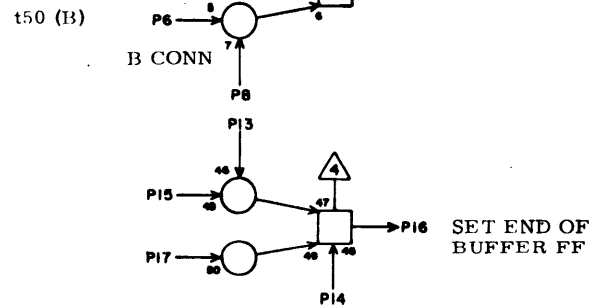
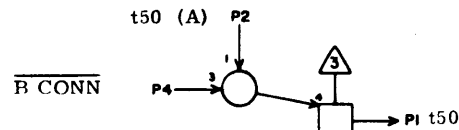
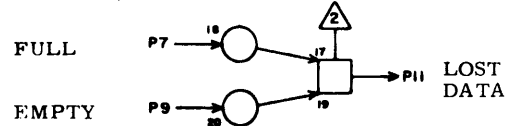
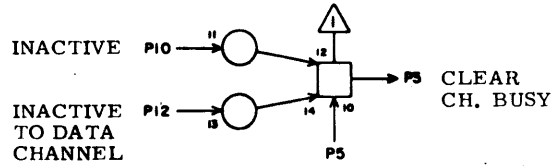
RV G

I04

| | | |
|----|--------|----|
| 1 | H07-14 | 7 |
| 2 | L03-24 | 15 |
| 3 | L03-7 | 13 |
| 4 | H07-1 | 9 |
| 5 | - | - |
| 6 | - | - |
| 7 | I03-8 | 5 |
| 8 | - | - |
| 9 | L03-17 | 13 |
| 10 | H07-2 | 9 |
| 11 | - | - |
| 12 | - | - |
| 13 | H04-21 | 5 |
| 14 | H14-20 | 15 |
| 15 | - | - |
| 16 | G07-7 | 11 |
| 17 | - | - |
| 18 | - | - |
| 19 | H14-21 | 15 |
| 20 | - | - |
| 21 | - | - |
| 22 | H07-27 | 9 |
| 23 | - | - |
| 24 | L04-17 | 13 |
| 25 | H07-28 | 7 |
| 26 | L04-24 | 13 |
| 27 | L04-7 | 11 |
| 28 | H07-19 | 9 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63060700
ASSY REV

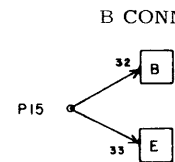
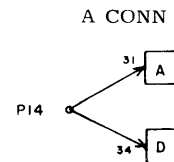
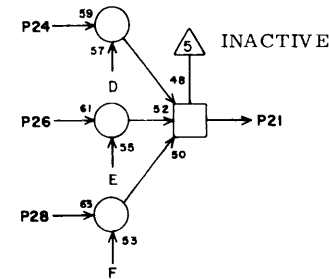
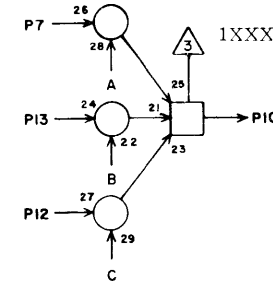
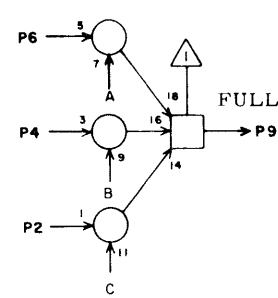


QH

| RV | G | I05 |
|----|--------|-----|
| 1 | J09-23 | 11 |
| 2 | J13- 5 | 13 |
| 3 | H05-11 | 5 |
| 4 | K07- 1 | 11 |
| 5 | F04-24 | 11 |
| 6 | J16- 5 | 17 |
| 7 | J02-15 | 9 |
| 8 | J10- 5 | 11 |
| 9 | J02-19 | 9 |
| 10 | G11- 9 | 13 |
| 11 | H05-24 | 5 |
| 12 | F12-24 | 15 |
| 13 | F05-26 | 120 |
| 14 | I05- X | 2 |
| 15 | F09-10 | 15 |
| 16 | H05-15 | 7 |
| 17 | E12-15 | 21 |
| 18 | J13-23 | 13 |
| 19 | J09- 7 | 9 |
| 20 | E10-11 | 19 |
| 21 | L11-11 | 15 |
| 22 | J16-23 | 17 |
| 23 | K05-28 | 11 |
| 24 | J10- 9 | 9 |
| 25 | L16-11 | 19 |
| 26 | K08-15 | 11 |
| 27 | E18-23 | 19 |
| 28 | G11- 1 | 15 |

JACK PIN LG
CIRCUIT SPECIFICATION I1827600
60227300 F

LS 63063700
ASSY REV

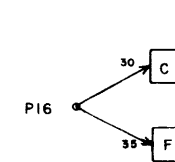
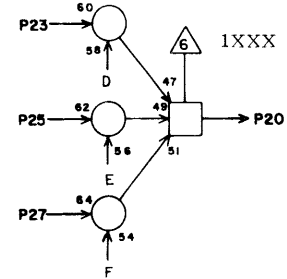
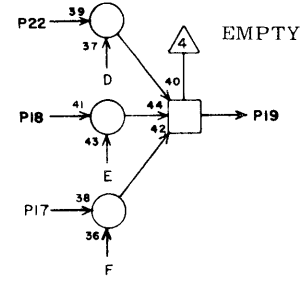
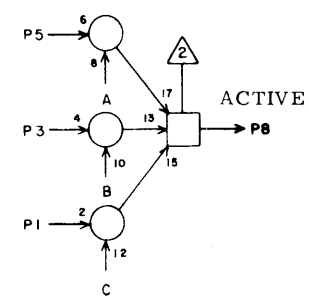


TE

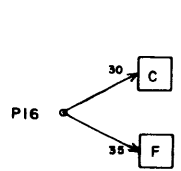
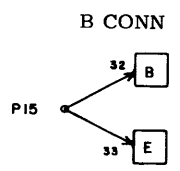
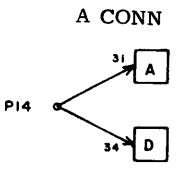
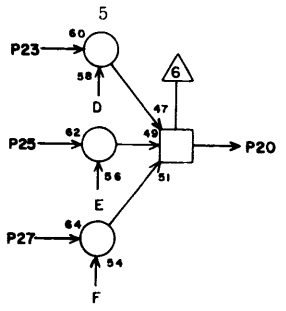
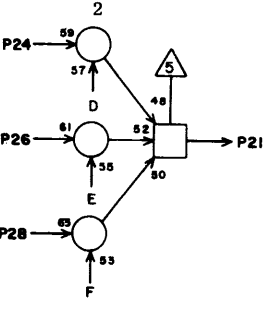
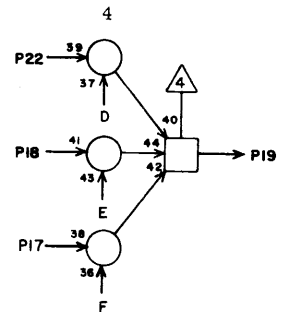
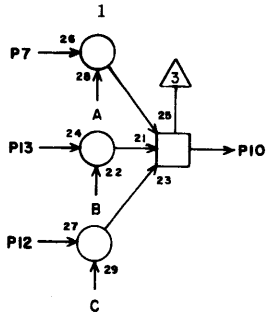
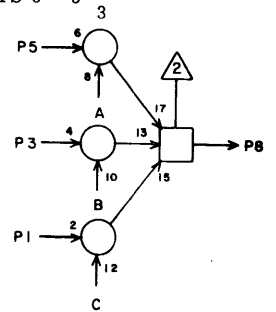
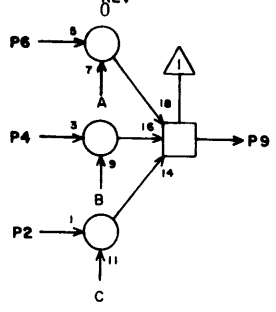
| RV | G | I06 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | L15- 7 | 17 |
| 4 | L15-18 | 19 |
| 5 | L10- 7 | 15 |
| 6 | L10-18 | 15 |
| 7 | K09-15 | 11 |
| 8 | G13- 1 | 15 |
| 9 | J02-28 | 11 |
| 10 | K08-25 | 13 |
| 11 | - | |
| 12 | - | |
| 13 | K10-15 | 11 |
| 14 | J10-10 | 9 |
| 15 | J10-15 | 9 |
| 16 | I06- X | 2 |
| 17 | - | |
| 18 | L15-22 | 17 |
| 19 | J02-26 | 9 |
| 20 | H13- 6 | 13 |
| 21 | G11- 2 | 13 |
| 22 | L10-22 | 15 |
| 23 | K09-17 | 11 |
| 24 | L18- 9 | 13 |
| 25 | K10-17 | 11 |
| 26 | L15- 9 | 17 |
| 27 | - | |
| 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION I1827600

60227300 F



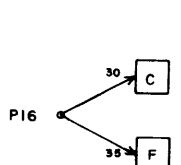
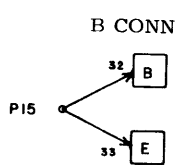
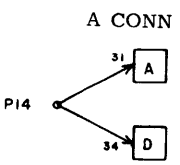
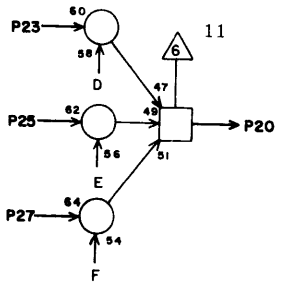
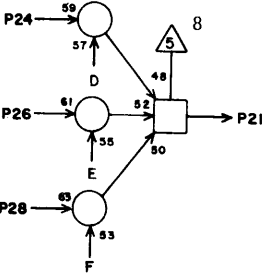
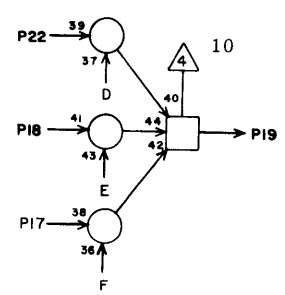
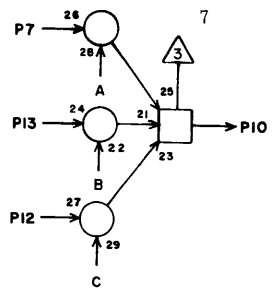
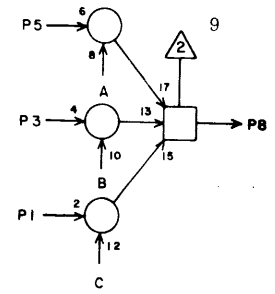
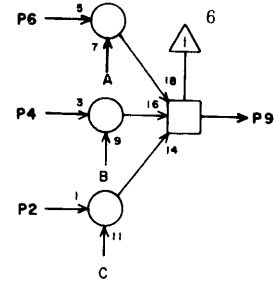
LS 63063700 ASSY REV 0 GATES IN FROM DATA CHANNEL BITS 0 - 5 TE



| RV | G | I87 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | L12-24 | 17 |
| 4 | L12-5 | 15 |
| 5 | L07-24 | 15 |
| 6 | L07-5 | 13 |
| 7 | L07-11 | 13 |
| 8 | H10-18 | 7 |
| 9 | H10-13 | 7 |
| 10 | H10-14 | 7 |
| 11 | - | |
| 12 | - | |
| 13 | L12-11 | 15 |
| 14 | J10-2 | 7 |
| 15 | J10-22 | 9 |
| 16 | I07-X | 2 |
| 17 | - | |
| 18 | L13-5 | 15 |
| 19 | H11-13 | 9 |
| 20 | H11-14 | 9 |
| 21 | H10-17 | 9 |
| 22 | L00-5 | 13 |
| 23 | L00-11 | 13 |
| 24 | L07-18 | 13 |
| 25 | L13-11 | 15 |
| 26 | L12-18 | 15 |
| 27 | - | |
| 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION I1827600
60227300 F

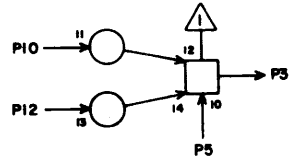
LS 63063700 ASSY REV 0 GATES IN FROM DATA CHANNEL BITS 6 - 11 TE



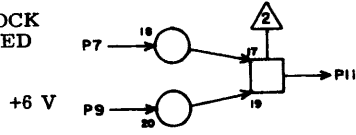
| RV | G | I08 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | L14-9 | 17 |
| 4 | L13-20 | 17 |
| 5 | L09-9 | 13 |
| 6 | L08-20 | 13 |
| 7 | L08-22 | 13 |
| 8 | H12-14 | 9 |
| 9 | J08-3 | 7 |
| 10 | J08-25 | 7 |
| 11 | - | |
| 12 | - | |
| 13 | L13-22 | 15 |
| 14 | J10-12 | 7 |
| 15 | J10-21 | 7 |
| 16 | I08-X | 2 |
| 17 | - | |
| 18 | L14-20 | 15 |
| 19 | H12-17 | 9 |
| 20 | H12-18 | 9 |
| 21 | J08-6 | 5 |
| 22 | L09-20 | 13 |
| 23 | L09-22 | 13 |
| 24 | L09-7 | 13 |
| 25 | L14-22 | 15 |
| 26 | L14-7 | 15 |
| 27 | - | |
| 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION I1827600
60227300 F

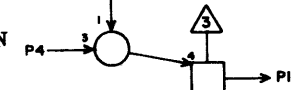
LS 63060700
ASSY **D**
REV



WRITE CLOCK
DELAYED

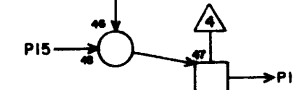


A CONN

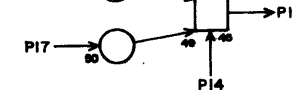


B CONN

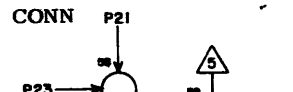
FULL (A)



FULL (A)



A CONN



INACTIVE

INACTIVE (A)

A CONN



EMPTY

EMPTY (A)

QH

RV G

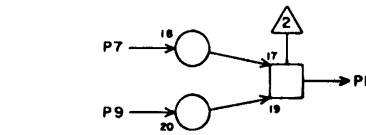
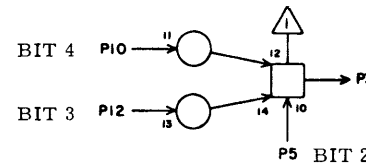
I09

| | | |
|----|--------|-----|
| 1 | D10- 6 | 19 |
| 2 | H16- 4 | 11 |
| 3 | - | |
| 4 | J10-16 | 7 |
| 5 | - | |
| 6 | J10-23 | 9 |
| 7 | F01-10 | 120 |
| 8 | H16-15 | 13 |
| 9 | C16-15 | 25 |
| 10 | - | |
| 11 | F07- 8 | 15 |
| 12 | - | |
| 13 | I09- X | 2 |
| 14 | H15- 6 | 11 |
| 15 | J08-14 | 7 |
| 16 | K13- 4 | 11 |
| 17 | K13-15 | 11 |
| 18 | J10-24 | 7 |
| 19 | K13-27 | 13 |
| 20 | G08-20 | 11 |
| 21 | J10-20 | 7 |
| 22 | K13-16 | 11 |
| 23 | F11-22 | 13 |
| 24 | I09- X | 2 |
| 25 | K13-17 | 11 |
| 26 | K06- 9 | 9 |
| 27 | I09- X | 2 |
| 28 | K13- 6 | 9 |

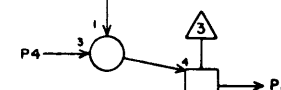
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63060700
ASSY **C**
REV

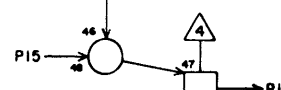


A CONN

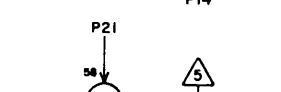


B CONN

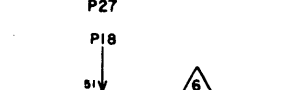
STATUS
3



FULL (B)



INACTIVE (B)



EMPTY (B)

QH

RV G

I10

| | | |
|----|--------|----|
| 1 | D10- 7 | 19 |
| 2 | H16- 1 | 11 |
| 3 | K10-21 | 11 |
| 4 | J10- 7 | 7 |
| 5 | H10-19 | 5 |
| 6 | J10-19 | 7 |
| 7 | - | |
| 8 | H16-19 | 11 |
| 9 | - | |
| 10 | H11- 6 | 7 |
| 11 | - | |
| 12 | F07-10 | 15 |
| 13 | I10- X | 2 |
| 14 | H15-10 | 11 |
| 15 | K16-15 | 13 |
| 16 | K16- 4 | 13 |
| 17 | J08-15 | 7 |
| 18 | J10-27 | 7 |
| 19 | K16-27 | 13 |
| 20 | G08-22 | 11 |
| 21 | J10-17 | 7 |
| 22 | K16-16 | 13 |
| 23 | F11-24 | 13 |
| 24 | I10- X | 2 |
| 25 | K16-17 | 13 |
| 26 | K07- 9 | 9 |
| 27 | I10- X | 2 |
| 28 | K16- 6 | 11 |

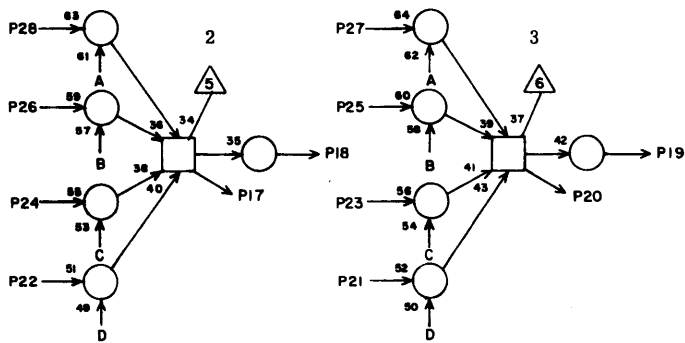
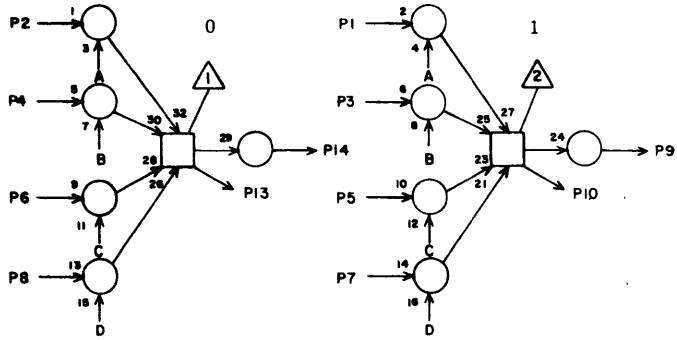
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63063900
ASSY **G**
REV

INTERFACE A
BITS 0-3

TG



+6V

- PI2 → **A** PASSBACK
- PI6 → **B** STATUS A
- PI11 → **C** DATA A
- PI5 → **D** POSITION A

CIRCUIT SPECIFICATION 11827600
60227300 F

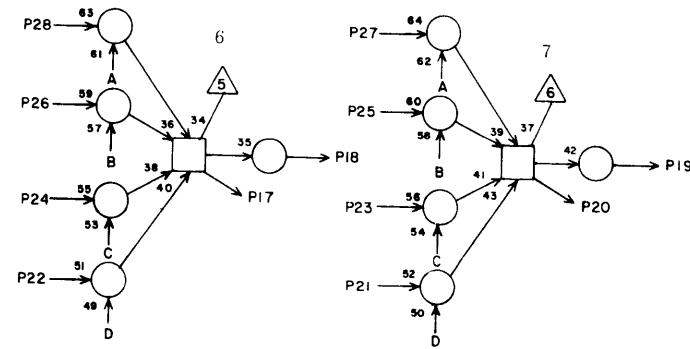
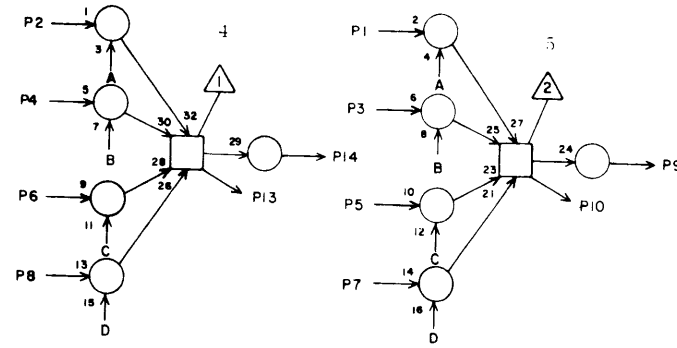
| RV | G | I11 |
|----|--------|-----|
| 1 | K11-17 | 11 |
| 2 | K11-19 | 11 |
| 3 | 809- 9 | 27 |
| 4 | 809- 8 | 27 |
| 5 | J03-10 | 13 |
| 6 | J03- 3 | 13 |
| 7 | D05- 2 | 23 |
| 8 | D05- 1 | 23 |
| 9 | - | - |
| 10 | K11- 6 | 9 |
| 11 | H15- 4 | 9 |
| 12 | C15- 2 | 25 |
| 13 | K11-11 | 9 |
| 14 | - | - |
| 15 | H15-24 | 9 |
| 16 | H15-28 | 9 |
| 17 | K11- 4 | 9 |
| 18 | - | - |
| 19 | - | - |
| 20 | K11-27 | 11 |
| 21 | D05-19 | 23 |
| 22 | D05-14 | 23 |
| 23 | J03-23 | 13 |
| 24 | J03-24 | 13 |
| 25 | 809-19 | 27 |
| 26 | 809-12 | 27 |
| 27 | K11-16 | 9 |
| 28 | K11-15 | 9 |

JACK PIN LG

LS 63063900
ASSY **G**
REV

INTERFACE
BITS 4-7

TG



- + 6V PI2 → **A** PASS BACK
- PI6 → **B** STATUS A
- PI11 → **C** DATA A
- PI5 → **D** POSITION A

* Standard Option 10037

CIRCUIT SPECIFICATION 11827600

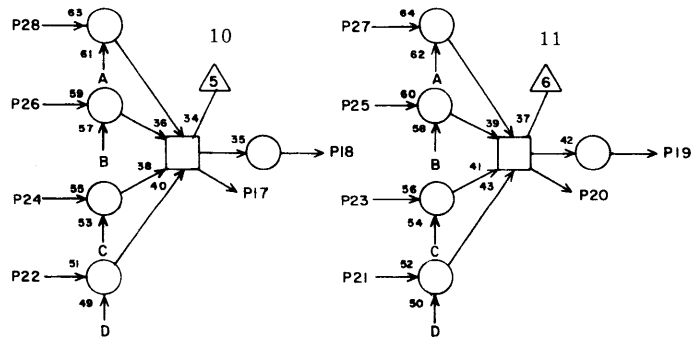
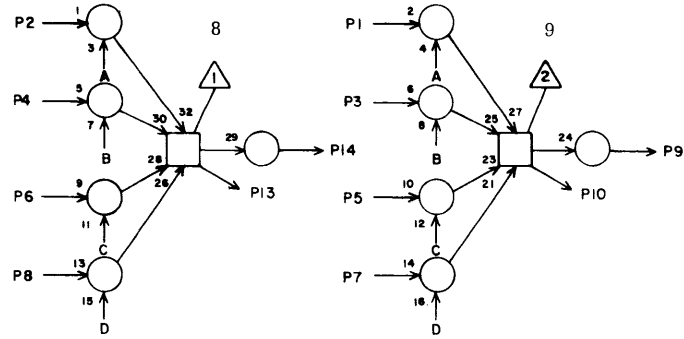
| RV | G | I12 |
|-----|--------|-----|
| 1 | K11-12 | 11 |
| 2 | K11-14 | 11 |
| 3 | 809-21 | 25 |
| 4 | 809-18 | 27 |
| 5 | J04-10 | 13 |
| 6 | J04- 3 | 13 |
| 7 | D05-28 | 21 |
| 8 | D05-27 | 21 |
| 9 | - | - |
| 10 | K11-20 | 11 |
| 11 | H15- 3 | 9 |
| 12 | C15- 4 | 25 |
| 13 | K11-25 | 11 |
| 14 | - | - |
| 15 | H15-21 | 7 |
| 16 | H15-25 | 9 |
| 17 | K12-11 | 9 |
| 18 | - | - |
| 19 | - | - |
| 20 | K12- 6 | 9 |
| *21 | C01- 2 | 25 |
| 21 | C06- 2 | 27 |
| *22 | C01- 4 | 25 |
| 22 | C06- 1 | 27 |
| 23 | J04-23 | 13 |
| 24 | J04-24 | 13 |
| 25 | F09- 5 | 15 |
| 26 | 807-18 | 29 |
| 27 | K12-17 | 9 |
| 28 | K12-19 | 9 |

JACK PIN LG

60227300 F

LS 63063900
ASSY **G**
REV

INTERFACE A
BITS 8-11 T6



+ 6V PI2 → **A** PASS BACK
PI6 → **B** STATUS A
PI11 → **C** DATA A
PI5 → **D** POSITION A

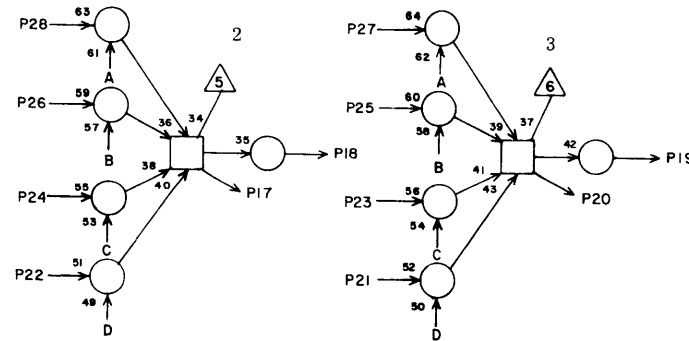
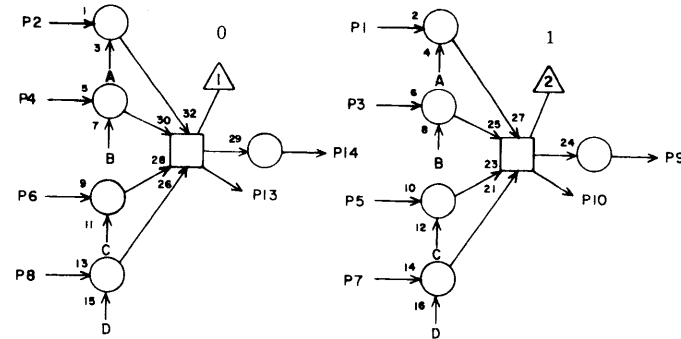
| RV | G | I13 |
|-----|--------|-----|
| 1 | K12-16 | 11 |
| 2 | K12-15 | 11 |
| 3 | F04- 9 | 17 |
| 4 | D08- 2 | 23 |
| 5 | J05-10 | 13 |
| 6 | J05- 3 | 13 |
| 7 | C06-19 | 25 |
| 8 | C06-14 | 25 |
| 9 | - | |
| 10 | K12-27 | 11 |
| 11 | H15- 5 | 7 |
| 12 | C15-15 | 23 |
| 13 | K12- 4 | 9 |
| 14 | - | |
| *15 | PI3-x | 2 |
| 15 | H15-22 | 7 |
| 16 | H15-26 | 7 |
| 17 | K12-25 | 11 |
| 18 | - | |
| 19 | - | |
| 20 | K12-20 | 11 |
| 21 | C06-28 | 25 |
| 22 | C06-27 | 25 |
| 23 | J05-23 | 13 |
| 24 | J05-24 | 13 |
| 25 | H05-25 | 13 |
| 26 | E10-19 | 17 |
| 27 | K12-12 | 9 |
| 28 | K12-14 | 9 |

JACK PIN LG
CIRCUIT SPECIFICATION I1827600
60227300 F

* Standard Option 10037

LS 63063900
ASSY **G**
REV

INTERFACE B
BITS 0-3 T6



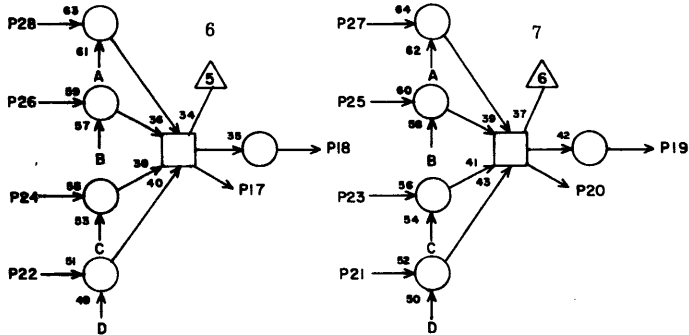
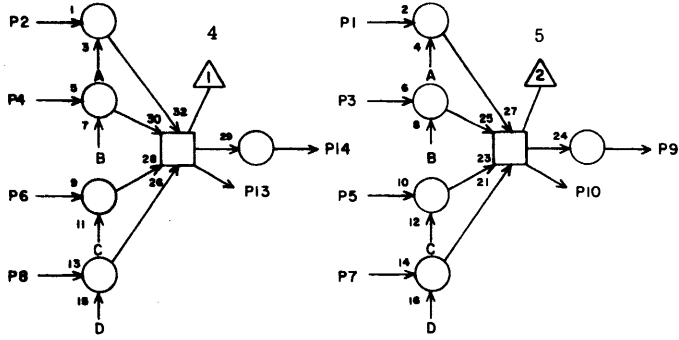
+ 6v PI2 → **A** PASS BACK
PI6 → **B** STATUS B
PI11 → **C** DATA B
PI5 → **D** POSITION B

| RV | G | I14 |
|----|--------|-----|
| 1 | K14-17 | 11 |
| 2 | K14-19 | 11 |
| 3 | B09-11 | 27 |
| 4 | B09- 7 | 27 |
| 5 | J03- 9 | 17 |
| 6 | J03- 4 | 15 |
| 7 | D05- 6 | 25 |
| 8 | D05- 3 | 25 |
| 9 | - | |
| 10 | K14- 6 | 9 |
| 11 | H15- 8 | 7 |
| 12 | C15-17 | 23 |
| 13 | K14-11 | 9 |
| 14 | - | |
| 15 | J02- 2 | 17 |
| 16 | J02-14 | 17 |
| 17 | K14- 4 | 9 |
| 18 | - | |
| 19 | - | |
| 20 | K14-27 | 11 |
| 21 | D05-17 | 25 |
| 22 | D05-10 | 25 |
| 23 | J03-22 | 17 |
| 24 | J03-25 | 15 |
| 25 | B09-17 | 29 |
| 26 | B09-10 | 29 |
| 27 | K14-16 | 9 |
| 28 | K14-15 | 9 |

JACK PIN LG
CIRCUIT SPECIFICATION I1827600
60227300 F

INTERFACE B
BITS 4-7

TG



- + 6v PI2 → **A** PASS BACK
- PI6 → **B** STATUS B
- PI1 → **C** DATA B
- PI5 → **D** POSITION B

| R# | G | I15 |
|-----|--------|-----|
| 1 | K14-12 | 11 |
| 2 | K14-14 | 11 |
| 3 | B09-15 | 27 |
| 4 | B09-20 | 27 |
| 5 | J04- 9 | 17 |
| 6 | J04- 4 | 15 |
| 7 | D05-26 | 23 |
| 8 | D05-18 | 23 |
| 9 | - | - |
| 10 | K14-20 | 11 |
| 11 | H15- 7 | 7 |
| 12 | C16- 2 | 23 |
| 13 | K14-25 | 11 |
| 14 | - | - |
| 15 | J02-12 | 19 |
| 16 | J02- 8 | 19 |
| 17 | K15-11 | 9 |
| 18 | - | - |
| 19 | - | - |
| 20 | K15- 6 | 9 |
| *21 | C01-15 | 27 |
| 21 | C06- 6 | 29 |
| *22 | C01-17 | 27 |
| 22 | C06- 3 | 29 |
| 23 | J04-22 | 17 |
| 24 | J04-25 | 15 |
| 25 | F09- 9 | 17 |
| 26 | B07-20 | 31 |
| 27 | K15-17 | 9 |
| 28 | K15-19 | 9 |

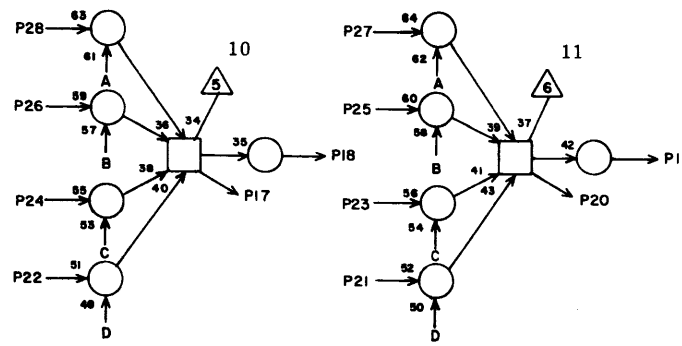
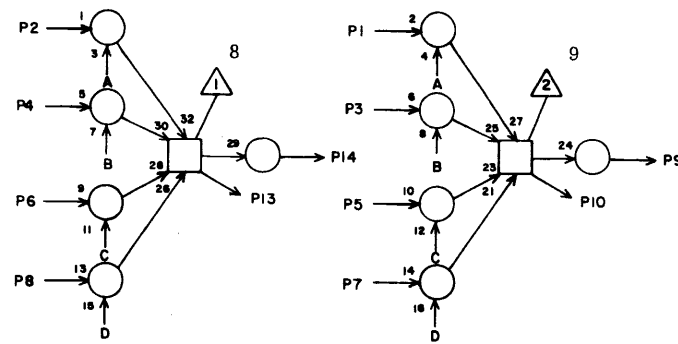
JACK PIN LG
CIRCUIT SPECIFICATION I1827600

60227300 F

* Standard Option 10037

INTERFACE B
BITS 8-11

TG



- +6v PI2 → **A** PASS BACK
- PI6 → **B** STATUS B
- PI1 → **C** DATA B
- PI5 → **D** POSITION B

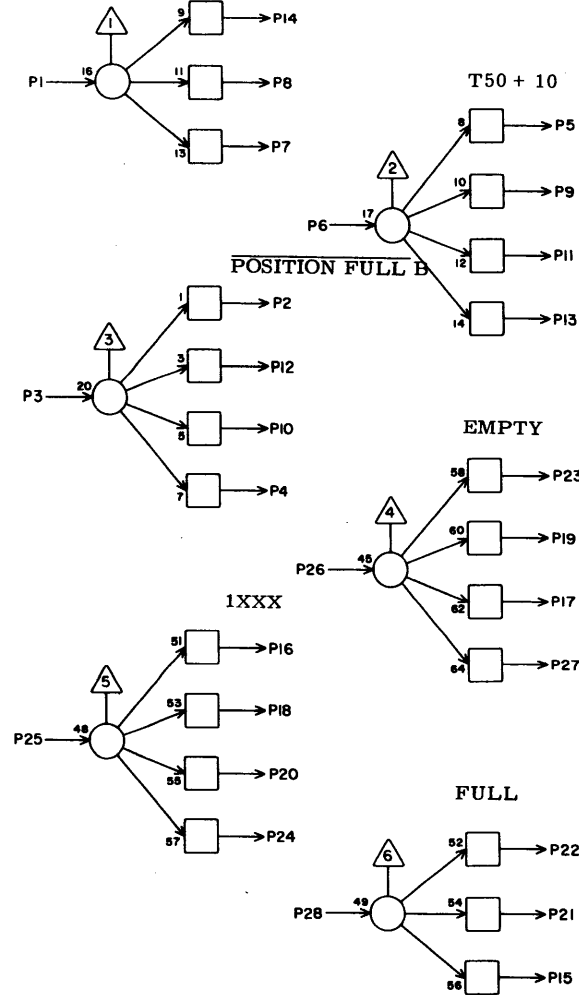
| R# | G | I16 |
|-----|---------|-----|
| 1 | K15-16 | 11 |
| 2 | K15-15 | 11 |
| 3 | F04-11 | 21 |
| 4 | D08- 4 | 23 |
| 5 | J05- 9 | 17 |
| 6 | J05- 4 | 15 |
| 7 | C06-17 | 27 |
| 8 | C06-10 | 27 |
| 9 | - | - |
| 10 | K15-27 | 11 |
| 11 | H15- 9 | 7 |
| 12 | C16- 4 | 23 |
| 13 | K15- 4 | 9 |
| 14 | - | - |
| *15 | I16-x | 21 |
| 15 | J02- 10 | 21 |
| 16 | J02- 7 | 19 |
| 17 | K15-25 | 11 |
| 18 | - | - |
| 19 | - | - |
| 20 | K15-20 | 11 |
| 21 | C06-26 | 27 |
| 22 | C06-18 | 27 |
| 23 | J05-22 | 17 |
| 24 | J05-25 | 15 |
| 25 | H05-27 | 15 |
| 26 | E10- 5 | 21 |
| 27 | K15-12 | 9 |
| 28 | K15-14 | 9 |

JACK PIN LG
CIRCUIT SPECIFICATION I1827600

* Standard Option 10037

60227300 F

STATUS FULL B



| RV | G | J02 |
|-----|--------|-----|
| 1 | H04-11 | 9 |
| 2 | I14-15 | 17 |
| 3 | H04-16 | 9 |
| 4 | - | |
| 5 | K09- 3 | 11 |
| 6 | J09-19 | 11 |
| 7 | I16-16 | 19 |
| 8 | I15-16 | 19 |
| 9 | K09-23 | 13 |
| *10 | I18-15 | 21 |
| 11 | E11- 7 | 25 |
| 12 | I15-15 | 19 |
| 13 | D10-23 | 25 |
| 14 | I14-16 | 17 |
| 15 | I05- 7 | 9 |
| 16 | K09- 1 | 11 |
| 17 | - | |
| 18 | K09-21 | 13 |
| 19 | I05- 9 | 9 |
| 20 | D10-21 | 27 |
| 21 | G04- 2 | 15 |
| 22 | H13- 4 | 19 |
| 23 | F08-17 | 21 |
| 24 | - | |
| 25 | K08-24 | 11 |
| 26 | I06-19 | 9 |
| 27 | - | |
| 28 | I06- 9 | 11 |

JACK PIN LG

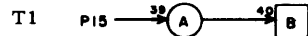
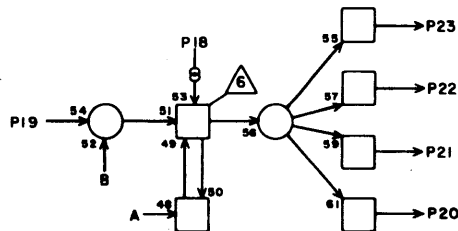
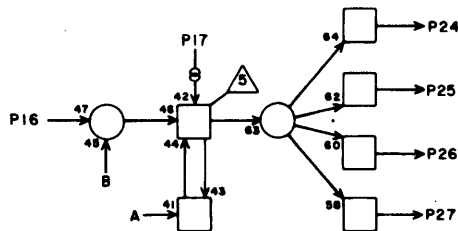
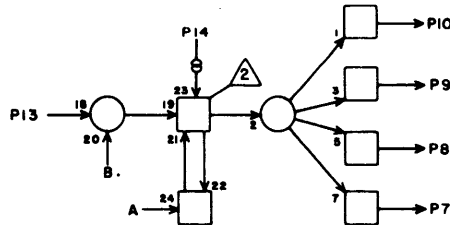
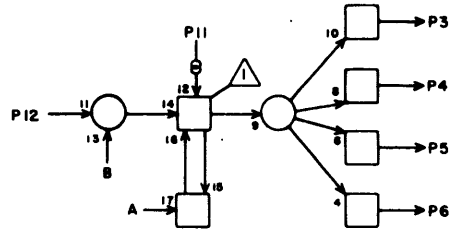
* Standard Option 10037

CIRCUIT SPECIFICATION 11827400

LS 63062700
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D
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READ DATA REGISTER
BITS 0-3



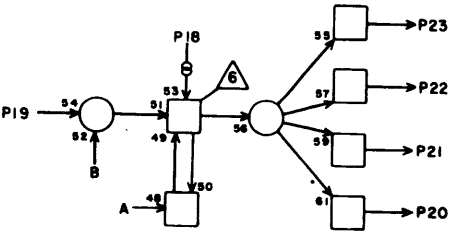
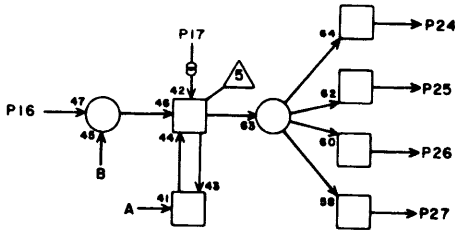
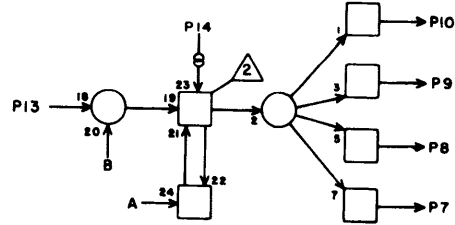
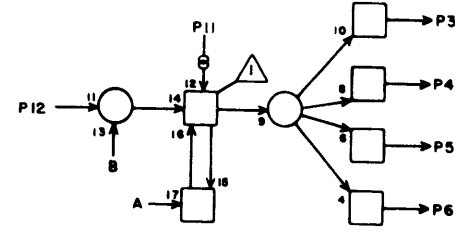
| SB | RV | G | J03 |
|----|--------|---|-----|
| 1 | - | | |
| 2 | - | | |
| 3 | I11- 6 | | 13 |
| 4 | I14- 6 | | 15 |
| 5 | F13- 4 | | 21 |
| 6 | E14-17 | | 25 |
| 7 | E14-19 | | 25 |
| 8 | F13- 3 | | 23 |
| 9 | I14- 5 | | 17 |
| 10 | I11- 5 | | 13 |
| 11 | J03- X | | 2 |
| 12 | L01-10 | | 11 |
| 13 | L01-12 | | 11 |
| 14 | J03- X | | 2 |
| 15 | E07-16 | | 21 |
| 16 | L01-22 | | 11 |
| 17 | J03- X | | 2 |
| 18 | J03- X | | 2 |
| 19 | L02-10 | | 9 |
| 20 | E14-23 | | 25 |
| 21 | F13-18 | | 21 |
| 22 | I14-23 | | 17 |
| 23 | I11-23 | | 13 |
| 24 | I11-24 | | 13 |
| 25 | I14-24 | | 15 |
| 26 | F13-13 | | 23 |
| 27 | E14-21 | | 25 |
| 28 | - | | |

JACK PIN LG
CIRCUIT SPECIFICATION I1827600
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READ DATA REGISTER
BITS 4-7



| SB | RV | G | J04 |
|----|--------|---|-----|
| 1 | - | | |
| 2 | - | | |
| 3 | I12- 6 | | 13 |
| 4 | I15- 6 | | 15 |
| 5 | F13-26 | | 19 |
| 6 | E14-25 | | 23 |
| 7 | E14-27 | | 23 |
| 8 | F13-25 | | 19 |
| 9 | I15- 5 | | 17 |
| 10 | I12- 5 | | 13 |
| 11 | J04- X | | 2 |
| 12 | L02-12 | | 11 |
| 13 | L02-22 | | 11 |
| 14 | J04- X | | 2 |
| 15 | E07-16 | | 21 |
| 16 | L03-10 | | 9 |
| 17 | J04- X | | 2 |
| 18 | J04- X | | 2 |
| 19 | L03-12 | | 9 |
| 20 | E14-18 | | 25 |
| 21 | F14- 3 | | 23 |
| 22 | I15-23 | | 17 |
| 23 | I12-23 | | 13 |
| 24 | I12-24 | | 13 |
| 25 | I15-24 | | 15 |
| 26 | F14- 4 | | 23 |
| 27 | E14-16 | | 25 |
| 28 | - | | |

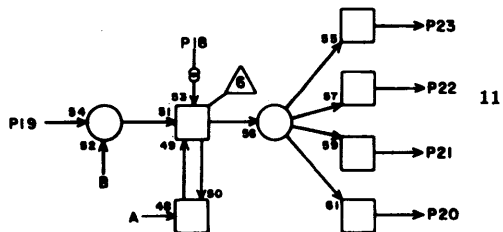
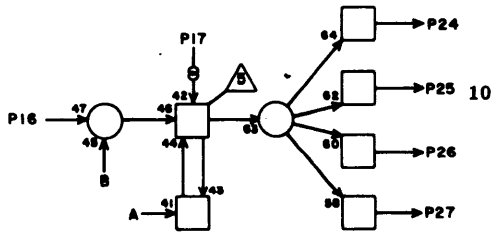
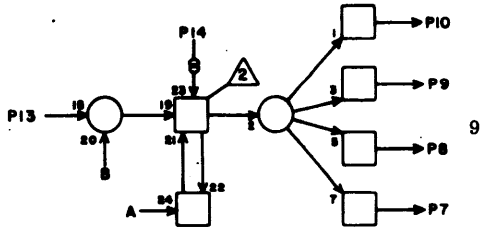
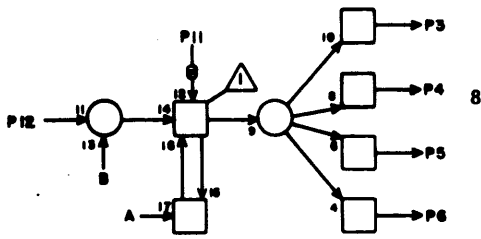
JACK PIN LG
CIRCUIT SPECIFICATION I1827600

60227300 F

READ DATA REGISTER
BITS 8-11

SB

RV G J05



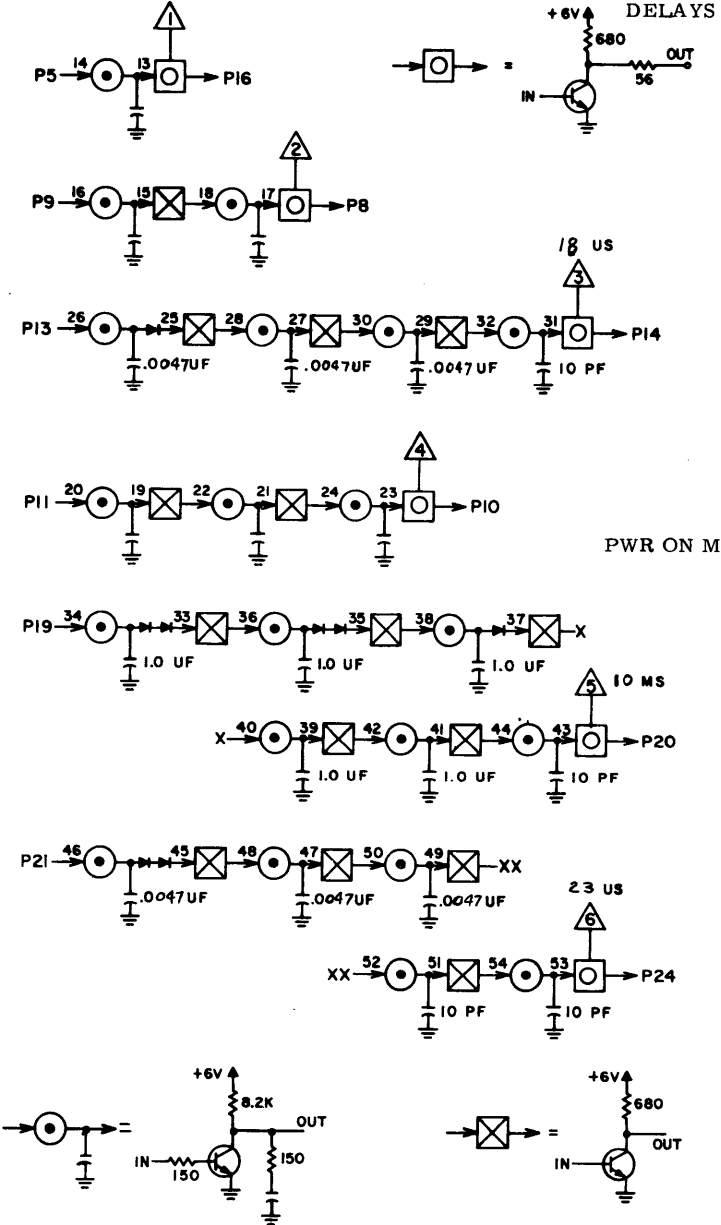
JACK PIN LG
CIRCUIT SPECIFICATION 11827600

60227300 F

J06

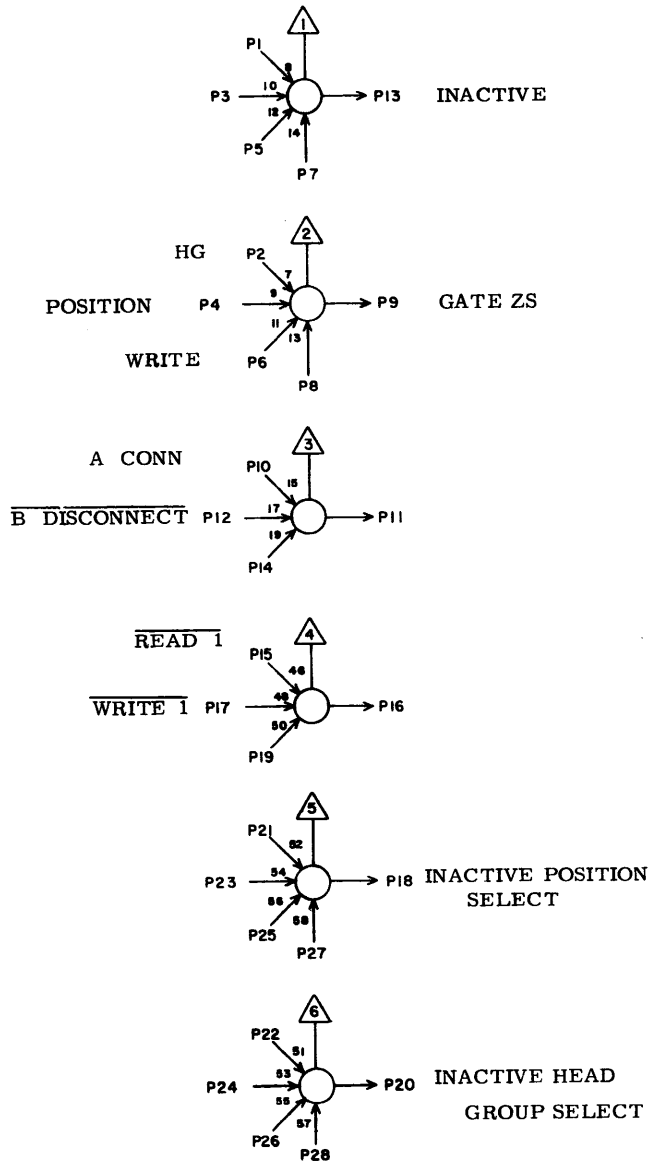
XL10

RV G



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CIRCUIT SPECIFICATION 11827600

60227300 F

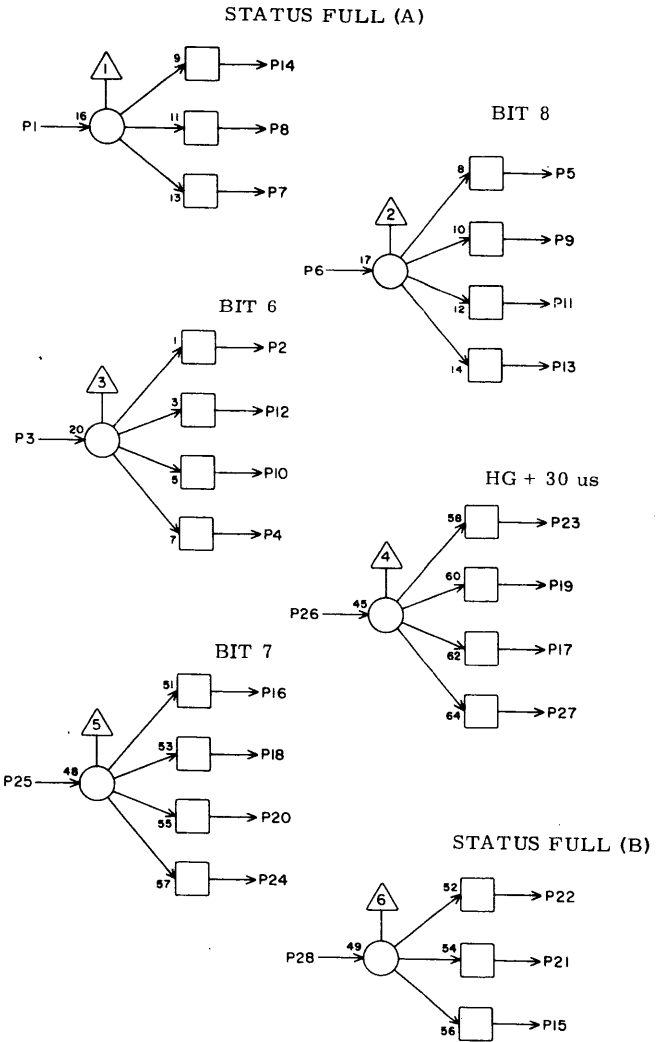


| RV | G | J07 |
|----|--------|-----|
| 1 | J07-20 | 5 |
| 2 | G05-6 | 13 |
| 3 | J07-18 | 5 |
| 4 | G05-5 | 13 |
| 5 | F07-18 | 15 |
| 6 | F01-13 | 19 |
| 7 | E09-18 | 19 |
| 8 | J07-X | 2 |
| 9 | E02-22 | 21 |
| 10 | K05-16 | 7 |
| 11 | K07-2 | 5 |
| 12 | K04-20 | 9 |
| 13 | F08-10 | 17 |
| 14 | J07-X | 2 |
| 15 | G07-1 | 13 |
| 16 | K10-27 | 9 |
| 17 | G07-9 | 13 |
| 18 | J07-3 | 5 |
| 19 | J07-X | 2 |
| 20 | J07-1 | 5 |
| 21 | G06-11 | 13 |
| 22 | G06-12 | 13 |
| 23 | E02-4 | 23 |
| 24 | F06-4 | 19 |
| 25 | J07-X | 2 |
| 26 | J07-X | 2 |
| 27 | J07-X | 2 |
| 28 | J07-X | 2 |

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60227300 G

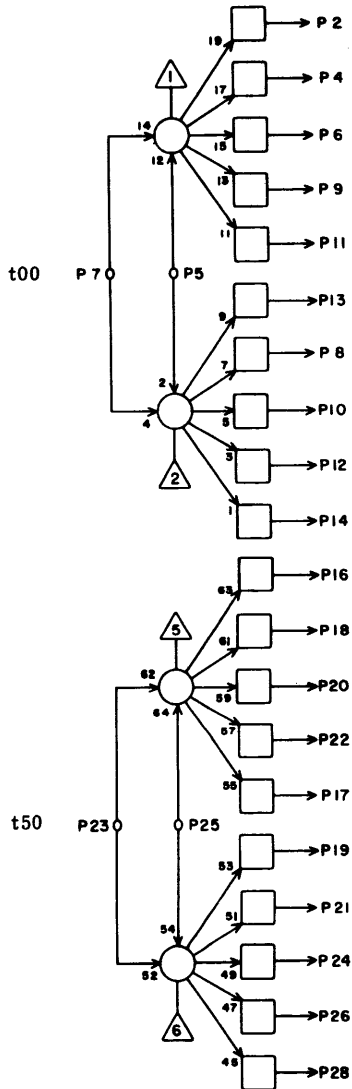


| RV | G | J08 |
|----|--------|-----|
| 1 | K06-25 | 9 |
| 2 | - | |
| 3 | I08-9 | 7 |
| 4 | - | |
| 5 | H14-26 | 11 |
| 6 | I08-21 | 5 |
| 7 | - | |
| 8 | H15-15 | 13 |
| 9 | H12-13 | 11 |
| 10 | H11-17 | 11 |
| 11 | - | |
| 12 | H14-6 | 13 |
| 13 | - | |
| 14 | I09-15 | 7 |
| 15 | I10-17 | 7 |
| 16 | H14-8 | 13 |
| 17 | E13-3 | 23 |
| 18 | H11-18 | 11 |
| 19 | L05-18 | 11 |
| 20 | - | |
| 21 | H04-12 | 13 |
| 22 | H04-17 | 11 |
| 23 | L05-25 | 11 |
| 24 | - | |
| 25 | I08-10 | 7 |
| 26 | O07-27 | 23 |
| 27 | O03-6 | 27 |
| 28 | K07-25 | 7 |

JACK PIN LG

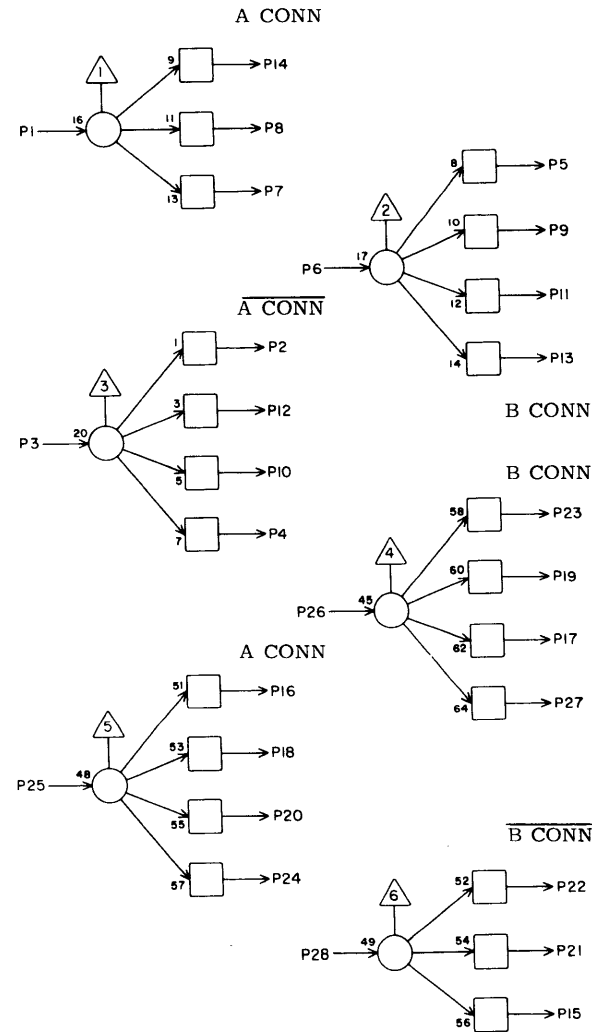
CIRCUIT SPECIFICATION 11827600

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| RV | G | J09 |
|----|--------|-----|
| 1 | - | |
| 2 | G12-11 | 13 |
| 3 | - | |
| 4 | F12-16 | 17 |
| 5 | J09- X | 2 |
| 6 | F03-16 | 19 |
| 7 | I05-19 | 9 |
| 8 | | |
| 9 | G01-13 | 17 |
| 10 | - | |
| 11 | G01-27 | 120 |
| 12 | - | |
| 13 | - | |
| 14 | A10- 7 | 132 |
| 15 | - | |
| 16 | G07-16 | 13 |
| 17 | G12- 5 | 15 |
| 18 | H10-15 | 11 |
| 19 | J02- 6 | 11 |
| 20 | H11-15 | 11 |
| 21 | G12-23 | 13 |
| 22 | H12-15 | 11 |
| 23 | I05- 1 | 11 |
| 24 | H05-13 | 13 |
| 25 | J09- X | 2 |
| 26 | F02-16 | 21 |
| 27 | - | |
| 28 | F11-16 | 19 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 G

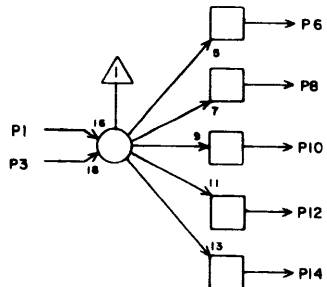


| RV | G | J10 |
|----|--------|-----|
| 1 | K05-22 | 11 |
| 2 | I07-14 | 7 |
| 3 | K05-27 | 11 |
| 4 | E10-26 | 17 |
| 5 | I05- 8 | 11 |
| 6 | K05-17 | 11 |
| 7 | I10- 4 | 7 |
| 8 | | |
| 9 | I05-24 | 9 |
| 10 | I06-14 | 9 |
| 11 | H15-16 | 11 |
| 12 | I08-14 | 7 |
| 13 | | |
| 14 | | |
| 15 | I06-15 | 9 |
| 16 | I09- 4 | 7 |
| 17 | I10-21 | 7 |
| 18 | H15- 2 | 13 |
| 19 | I10- 6 | 7 |
| 20 | I09-21 | 7 |
| 21 | I08-15 | 7 |
| 22 | I07-15 | 9 |
| 23 | I09- 6 | 9 |
| 24 | I09-18 | 7 |
| 25 | K05-24 | 11 |
| 26 | K05-19 | 9 |
| 27 | I10-18 | 7 |
| 28 | K05-15 | 9 |

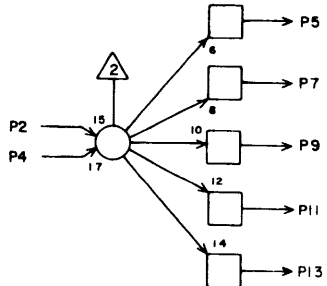
JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 G

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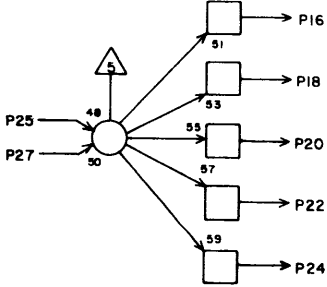
REV



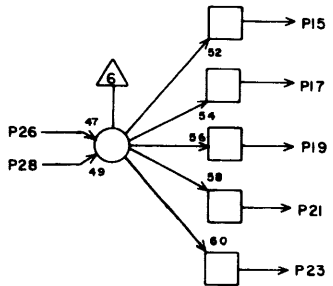
t25(A)



t50(A)



t50(A)



t00(A)

TD

| RV | G | J11 |
|----|--------|-----|
| 1 | J13- 2 | 5 |
| 2 | J13- 1 | 5 |
| 3 | J11- X | 2 |
| 4 | J11- X | 2 |
| 5 | K06-16 | 11 |
| 6 | K11-18 | 41 |
| 7 | K04- 8 | 13 |
| 8 | K12-18 | 41 |
| 9 | L07-12 | 11 |
| 10 | - | |
| 11 | L08-12 | 11 |
| 12 | - | |
| 13 | L09-12 | 11 |
| 14 | - | |
| 15 | K04- 7 | 11 |
| 16 | L10-12 | 9 |
| 17 | - | |
| 18 | L11-12 | 9 |
| 19 | - | |
| 20 | H16- 9 | 13 |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | - | |
| 25 | J13- 3 | 7 |
| 26 | J13-21 | 7 |
| 27 | J11- X | 2 |
| 28 | J11- X | 2 |

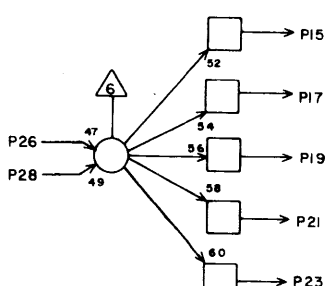
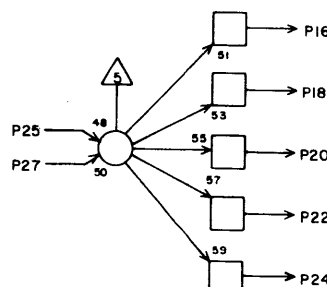
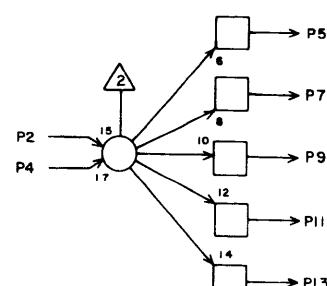
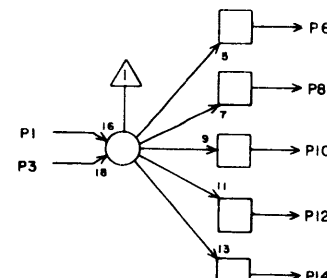
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60227300 F

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ASSY

REV

CHANNEL A CLOCK
STROBE NETWORK



TD

| RV | G | J12 |
|----|--------|-----|
| 1 | J13-14 | 132 |
| 2 | J12-10 | 108 |
| 3 | J12- X | 2 |
| 4 | J12- X | 2 |
| 5 | J13-16 | 17 |
| 6 | J13-11 | 55 |
| 7 | J13-18 | 55 |
| 8 | J13-19 | 17 |
| 9 | J12-25 | 108 |
| 10 | J12- 2 | 108 |
| 11 | - | |
| 12 | J13-10 | 45 |
| 13 | - | |
| 14 | - | |
| 15 | J13-15 | 17 |
| 16 | J13-13 | 17 |
| 17 | J13-20 | 55 |
| 18 | J13-17 | 55 |
| 19 | - | |
| 20 | J12-26 | 108 |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | - | |
| 25 | J12- 9 | 108 |
| 26 | J12-20 | 108 |
| 27 | J12- X | 2 |
| 28 | J12- X | 2 |

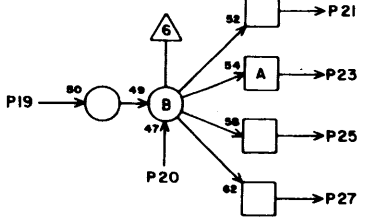
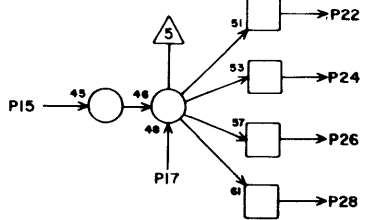
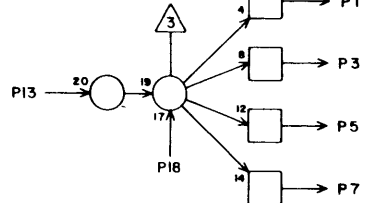
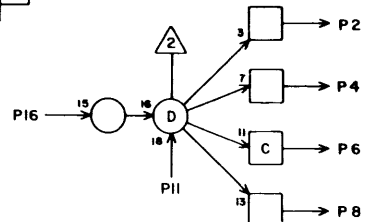
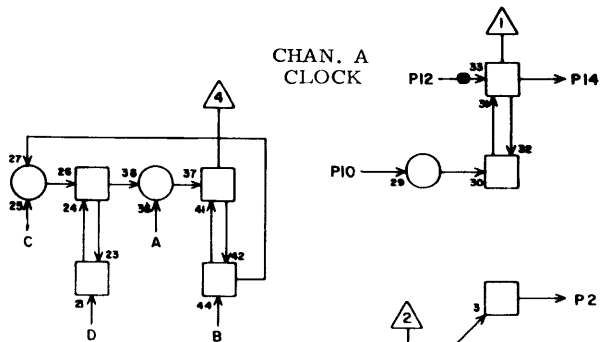
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60227300 F

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ASSY

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REV

CHAN. A
CLOCK

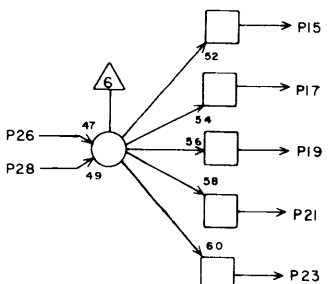
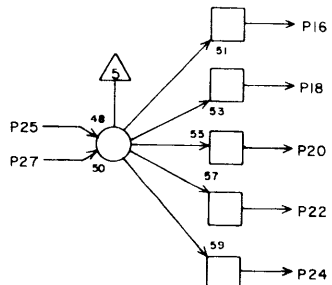
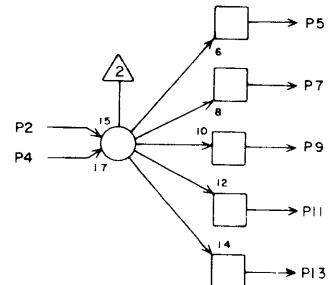
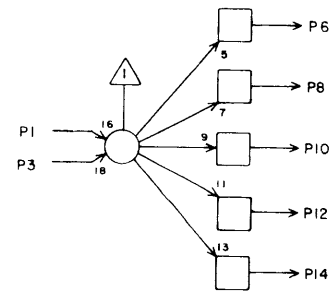


| HQ | RV | G | J13 |
|-----|----|--------|-----|
| | 1 | J11- 2 | 5 |
| | 2 | J11- 1 | 5 |
| | 3 | J11-25 | 7 |
| | 4 | K13-18 | 7 |
| | 5 | I05- 2 | 13 |
| | 6 | - | |
| | 7 | - | |
| | 8 | - | |
| | 9 | - | |
| | 10 | J12-12 | 45 |
| 25 | 11 | J12- 6 | 55 |
| | 12 | - | |
| | 13 | J12-16 | 17 |
| | 14 | J12- 1 | 132 |
| | 15 | J12-15 | 17 |
| 50 | 16 | J12- 5 | 17 |
| | 17 | J12-18 | 55 |
| | 18 | J12- 7 | 55 |
| | 19 | J12- 8 | 17 |
| | 20 | J12-17 | 55 |
| | 21 | J11-26 | 7 |
| 75 | 22 | - | |
| | 23 | I05-18 | 13 |
| | 24 | - | |
| | 25 | - | |
| | 26 | - | |
| | 27 | - | |
| 100 | 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION I1827600
60227300 G

LS 63063600
ASSY

REV



t25 (B)

150 (B)

150 (B)

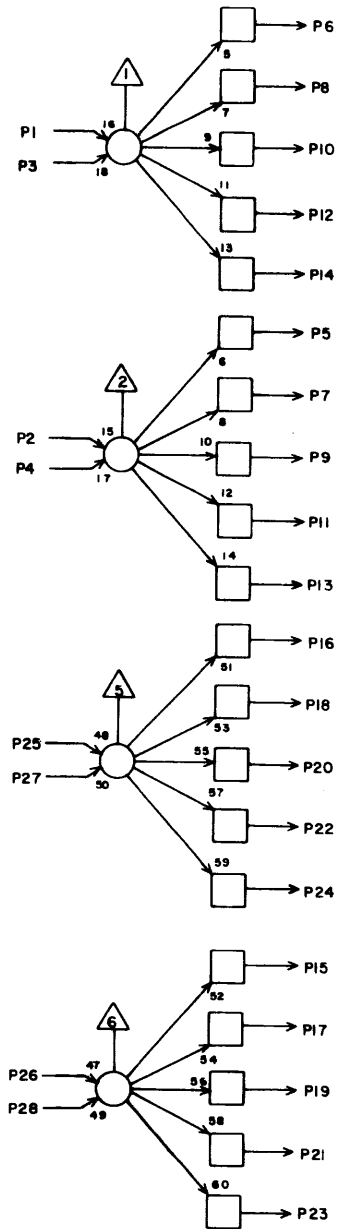
100 (B)

| TD | RV | G | J14 |
|----|----|--------|-----|
| | 1 | J16- 2 | 5 |
| | 2 | J16- 1 | 5 |
| | 3 | J14- X | 2 |
| | 4 | J14- X | 2 |
| | 5 | K07-16 | 13 |
| | 6 | K14-18 | 41 |
| | 7 | K04-18 | 15 |
| | 8 | K15-18 | 41 |
| | 9 | L12-12 | 11 |
| | 10 | - | |
| | 11 | L13-12 | 11 |
| | 12 | - | |
| | 13 | L14-12 | 9 |
| | 14 | - | |
| | 15 | K04-17 | 15 |
| | 16 | L15-12 | 9 |
| | 17 | - | |
| | 18 | L16-12 | 11 |
| | 19 | - | |
| | 20 | H16-20 | 11 |
| | 21 | - | |
| | 22 | - | |
| | 23 | - | |
| | 24 | - | |
| | 25 | J16- 3 | 7 |
| | 26 | J16-21 | 7 |
| | 27 | J14- X | 2 |
| | 28 | J14- X | 2 |

JACK PIN LG
CIRCUIT SPECIFICATION I1827600
60227300 F

LS 63063600
ASSY REV

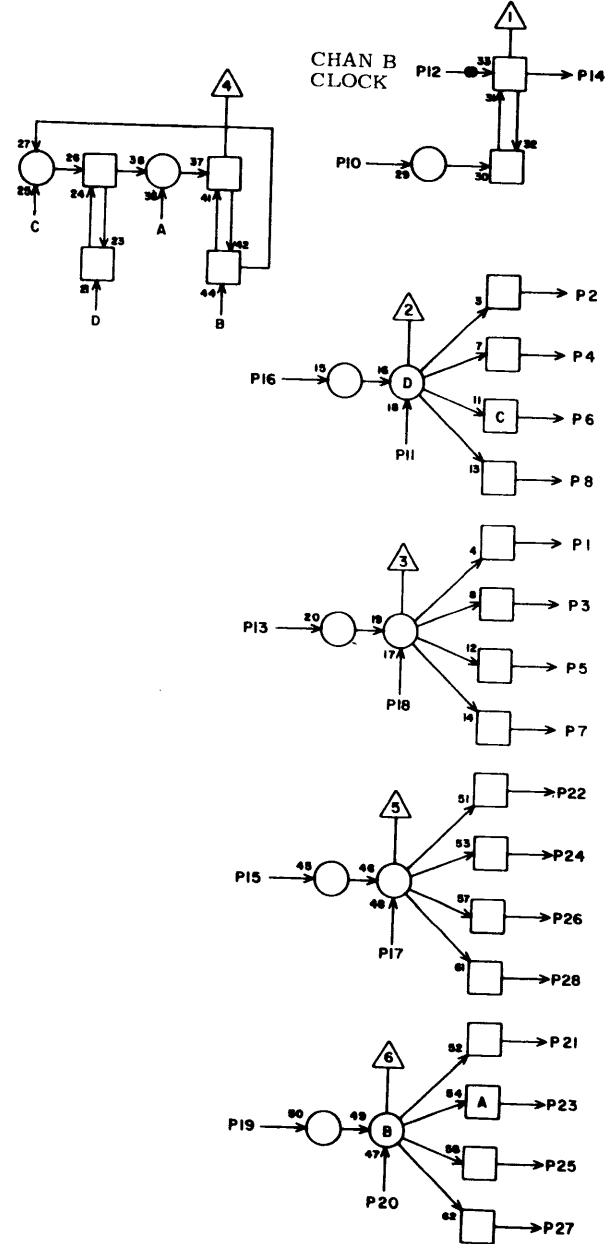
CHANNEL B CLOCK
STROBE NETWORK



| RV | G | J15 |
|----|--------|-----|
| 1 | J16-14 | 132 |
| 2 | J15-10 | 108 |
| 3 | J15- X | 2 |
| 4 | J15- X | 2 |
| 5 | J16-16 | 17 |
| 6 | J16-11 | 55 |
| 7 | J16-18 | 55 |
| 8 | J16-19 | 17 |
| 9 | J15-25 | 108 |
| 10 | J15- 2 | 108 |
| 11 | - | |
| 12 | J16-10 | 45 |
| 13 | - | |
| 14 | - | |
| 15 | J16-15 | 17 |
| 16 | J16-13 | 17 |
| 17 | J16-20 | 55 |
| 18 | J16-17 | 55 |
| 19 | - | |
| 20 | J15-26 | 108 |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | - | |
| 25 | J15- 9 | 108 |
| 26 | J15-20 | 108 |
| 27 | J15- X | 2 |
| 28 | J15- X | 2 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63046200
ASSY REV



| HQ | RV | G | J16 |
|----|----|--------|-----|
| | 1 | J14- 2 | 5 |
| | 2 | J14- 1 | 5 |
| | 3 | J14-25 | 7 |
| | 4 | K16-18 | 7 |
| | 5 | I05- 6 | 17 |
| | 6 | - | |
| | 7 | - | |
| | 8 | - | |
| | 9 | - | |
| | 10 | J15-12 | 45 |
| | 11 | J15- 6 | 55 |
| | 12 | - | |
| | 13 | J15-16 | 17 |
| | 14 | J15- 1 | 132 |
| | 15 | J15-15 | 17 |
| | 16 | J15- 5 | 17 |
| | 17 | J15-18 | 55 |
| | 18 | J15- 7 | 55 |
| | 19 | J15- 8 | 17 |
| | 20 | J15-17 | 55 |
| | 21 | J14-26 | 7 |
| | 22 | - | |
| | 23 | I05-22 | 17 |
| | 24 | - | |
| | 25 | - | |
| | 26 | - | |
| | 27 | - | |
| | 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 G

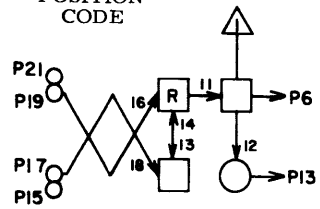
LSI7876300
ASSY



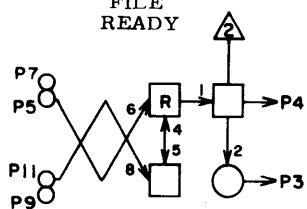
ZR

RV G K01

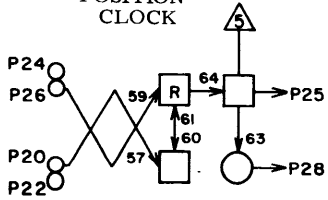
POSITION
CODE



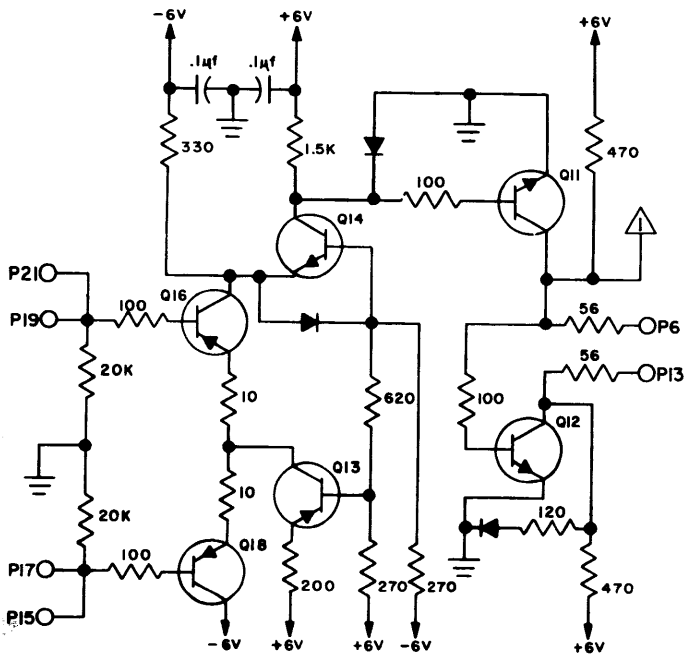
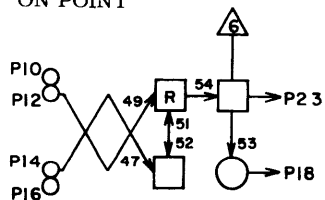
FILE
READY



POSITION
CLOCK



ON POINT



13 E01-26 21

14 -

15 -

16 -

17 -

18 -

19 -

20 -

21 -

22 -

23 E01-28 23

24 -

25 E01- 1 25

26 -

27 -

28 -

JACK PIN LG
60227300 G

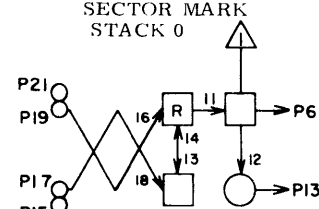
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ASSY



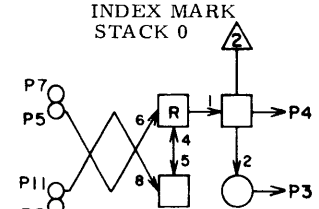
ZR

RV G K02

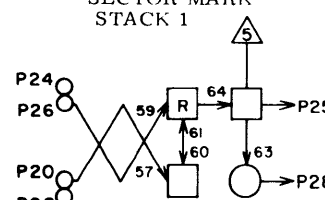
SECTOR MARK
STACK 0



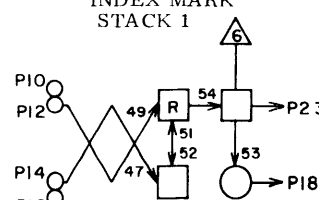
INDEX MARK
STACK 0



SECTOR MARK
STACK 1



INDEX MARK
STACK 1



14 -

15 -

16 -

17 -

18 -

19 -

20 -

21 -

22 -

23 E01-28 23

24 -

25 E01- 1 25

26 -

27 -

28 -

JACK PIN LG
60227300 F

14 -

15 -

16 -

17 -

18 003-24 25

19 -

20 -

21 -

22 -

23 A01- 7 37

24 -

25 807- 3 35

26 -

27 -

28 -

JACK PIN LG
60227300 F

LSI7876300
ASSY



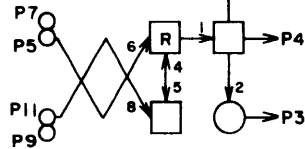
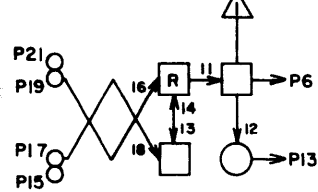
ZR

RV G

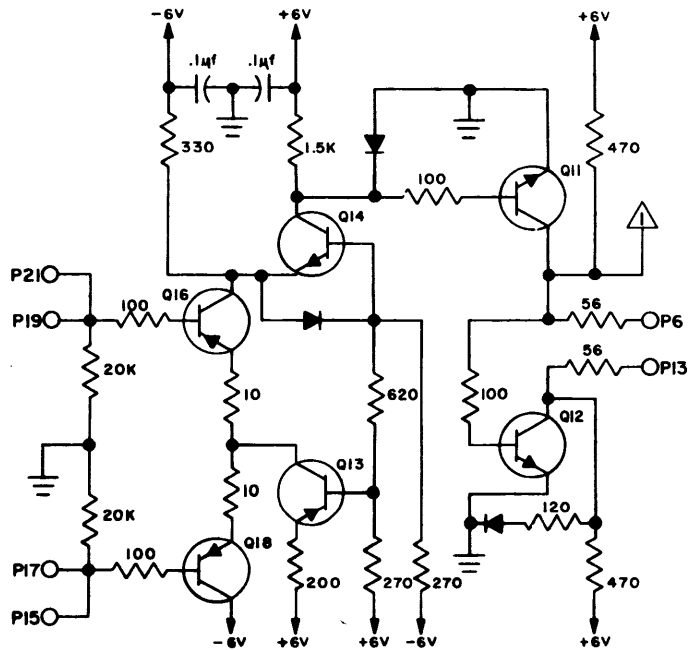
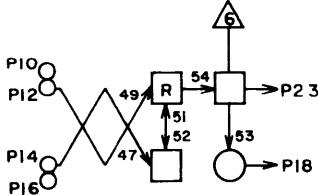
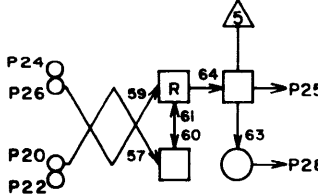
K83

READ CLOCK

WRITE CLOCK 0



WRITE CLOCK I



| JACK | PIN | LG |
|------|--------|----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | G01-20 | 15 |
| 5 | - | |
| 6 | G01-4 | 17 |
| 7 | - | |
| 8 | - | |
| 9 | - | |
| 10 | - | |
| 11 | - | |
| 12 | - | |
| 13 | - | |
| 14 | - | |
| 15 | - | |
| 16 | - | |
| 17 | - | |
| 18 | - | |
| 19 | - | |
| 20 | - | |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | - | |
| 25 | G01-22 | 17 |
| 26 | - | |
| 27 | - | |
| 28 | - | |

60227300 F

LS 63040000
ASSY



AA

RV G

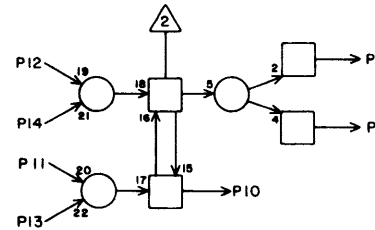
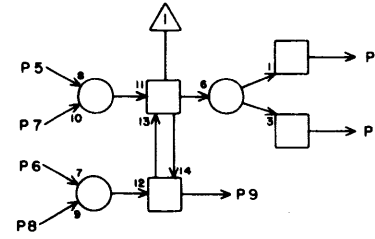
K04

INACTIVE

A CONN

1XXX

+ 50

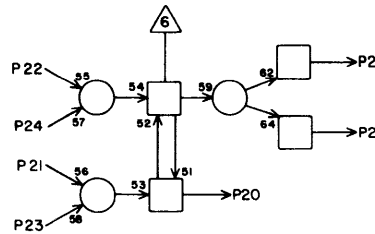
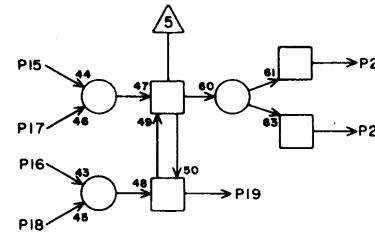


INACTIVE

B CONN

1XXX

+ 50



A DISCONNECT

B DISCONNECT

| JACK | PIN | LG |
|------|--------|----|
| 1 | K06-4 | 5 |
| 2 | J06-13 | 7 |
| 3 | - | |
| 4 | K04-12 | 5 |
| 5 | H16-14 | 21 |
| 6 | K05-12 | 5 |
| 7 | J11-15 | 11 |
| 8 | J11-7 | 13 |
| 9 | K04-11 | 3 |
| 10 | - | |
| 11 | K04-9 | 3 |
| 12 | K04-4 | 5 |
| 13 | K04-X | 2 |
| 14 | J06-14 | 7 |
| 15 | H16-28 | 21 |
| 16 | K05-7 | 5 |
| 17 | J14-15 | 15 |
| 18 | J14-7 | 15 |
| 19 | K04-21 | 3 |
| 20 | J07-12 | 9 |
| 21 | K04-19 | 3 |
| 22 | K04-28 | 3 |
| 23 | K04-X | 2 |
| 24 | J06-24 | 7 |
| 25 | - | |
| 26 | J06-21 | 9 |
| 27 | - | |
| 28 | K04-22 | 3 |

CIRCUIT SPECIFICATION 11827600

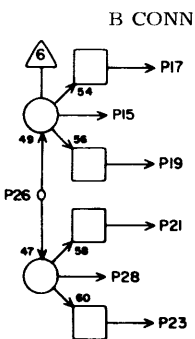
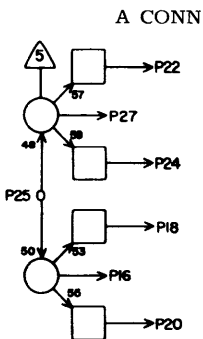
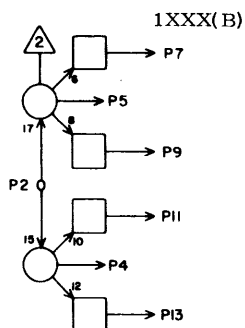
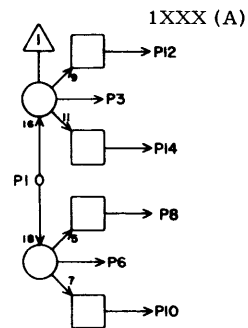
60227300 G

LS 63042900
ASSY

REV B

| CX | RV | G | K05 |
|----|--------|----|-----|
| 1 | K09-13 | 7 | |
| 2 | K10-13 | 9 | |
| 3 | K06- 2 | 5 | |
| 4 | K07-14 | 5 | |
| 5 | K07- 4 | 5 | |
| 6 | K06-14 | 5 | |
| 7 | K04-16 | 5 | |
| 8 | - | - | |
| 9 | - | - | |
| 10 | - | - | |
| 11 | - | - | |
| 12 | K04- 6 | 5 | |
| 13 | - | - | |
| 14 | - | - | |
| 15 | J10-28 | 9 | |
| 16 | J07-10 | 7 | |
| 17 | J10- 6 | 11 | |
| 18 | - | - | |
| 19 | J10-26 | 9 | |
| 20 | - | - | |
| 21 | - | - | |
| 22 | J10- 1 | 11 | |
| 23 | E09-25 | 25 | |
| 24 | J10-25 | 11 | |
| 25 | K06- 8 | 5 | |
| 26 | K07- 8 | 7 | |
| 27 | J10- 3 | 11 | |
| 28 | I05-23 | 11 | |

JACK PIN LG
CIRCUIT SPECIFICATION I1827600
60227300 G



LS 63040400
ASSY

REV C

B CONN
STATUS

1XXX
DISCONNECT

STATUS

X

1XXX

X

STATUS

X

EMPTY

X

STATUS 2

ACTIVE

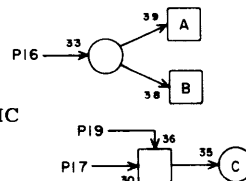
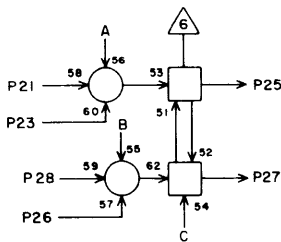
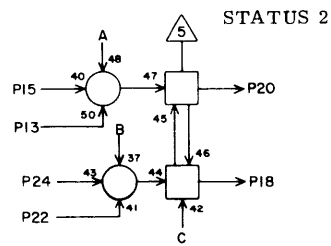
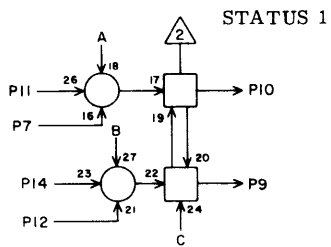
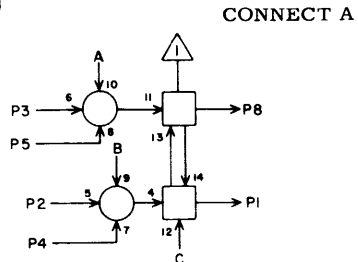
ACTIVE

X

t50 (A)

PWR ON MC

MC



| AE | RV | G | K06 |
|----|----|--------|-----|
| | 1 | K07- 3 | 5 |
| | 2 | K05- 3 | 5 |
| | 3 | E10- 9 | 120 |
| | 4 | K04- 1 | 5 |
| | 5 | K08- 6 | 5 |
| | 6 | - | - |
| | 7 | K06- X | 2 |
| | 8 | K05-25 | 5 |
| | 9 | I09-26 | 9 |
| | 10 | - | - |
| | 11 | K08- 8 | 5 |
| | 12 | K06- X | 2 |
| | 13 | L08- 8 | 7 |
| | 14 | K05- 6 | 5 |
| | 15 | K08-10 | 5 |
| | 16 | J11- 5 | 11 |
| | 17 | L11- 8 | 9 |
| | 18 | - | - |
| | 19 | K08-17 | 5 |
| | 20 | K06-21 | 3 |
| | 21 | K06-20 | 3 |
| | 22 | K06- X | 2 |
| | 23 | L10- 5 | 9 |
| | 24 | L10-24 | 9 |
| | 25 | J08- 1 | 9 |
| | 26 | K06- X | 2 |
| | 27 | - | - |
| | 28 | L10- 6 | 9 |

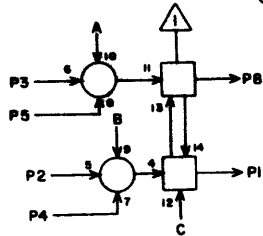
JACK PIN LG
CIRCUIT SPECIFICATION I1827600
60227300 G

3 63040400
ASSY



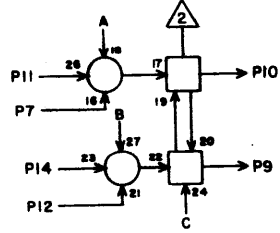
CONNECT B

A CONN
STATUS



1XXX

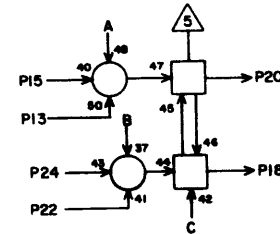
STATUS



STATUS 1

1XXX

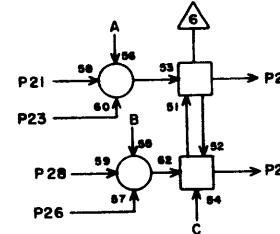
STATUS



STATUS 2

EMPTY

STATUS

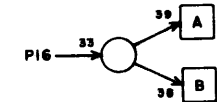


STATUS 3

ACTIVE

ACTIVE

t50



PWR ON MC

MC

| AE | RV | G | K07 |
|----|----|--------|-----|
| | 1 | I05-4 | 11 |
| | 2 | J07-11 | 5 |
| | 3 | K06-1 | 5 |
| | 4 | K05-5 | 5 |
| | 5 | K00-5 | 5 |
| | 6 | - | |
| | 7 | K07-X | 2 |
| | 8 | K05-26 | 7 |
| | 9 | I10-26 | 9 |
| | 10 | - | |
| | 11 | K08-7 | 5 |
| | 12 | K07-X | 2 |
| | 13 | L13-8 | 11 |
| | 14 | K05-4 | 5 |
| | 15 | K08-9 | 5 |
| | 16 | J14-5 | 13 |
| | 17 | L16-8 | 13 |
| | 18 | - | |
| | 19 | K00-19 | 5 |
| | 20 | K07-21 | 3 |
| | 21 | K07-20 | 3 |
| | 22 | K07-X | 2 |
| | 23 | L15-5 | 13 |
| | 24 | L15-24 | 13 |
| | 25 | J08-28 | 7 |
| | 26 | K07-X | 2 |
| | 27 | - | |
| | 28 | L15-6 | 13 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 G

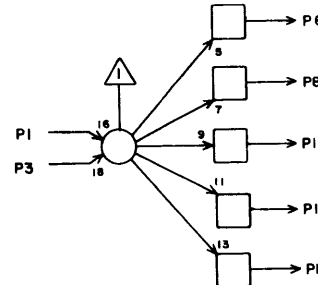
LS 63063600
ASSY



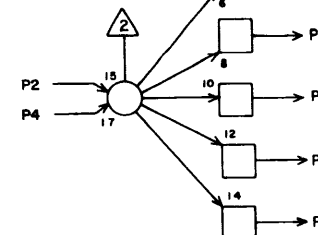
1XXX
X7XX

1XXX
X7XX

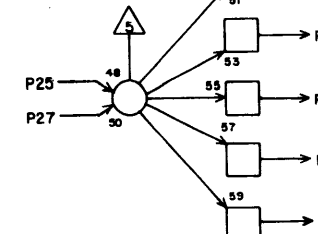
1XXX



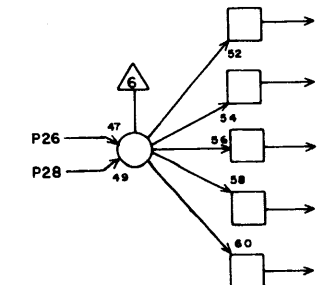
STATUS A



STATUS B



1XXX



POWER ON MC

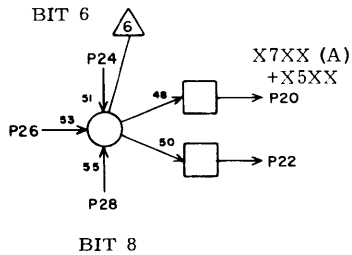
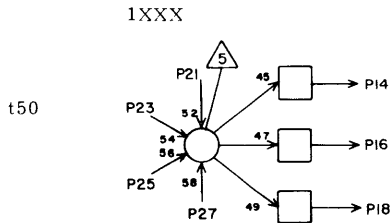
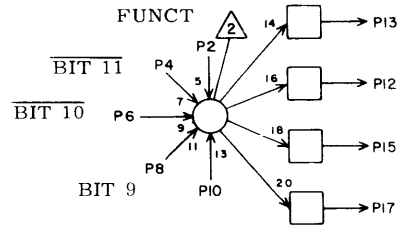
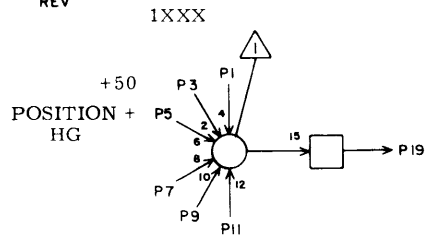
| TD | RV | G | K08 |
|----|----|--------|-----|
| | 1 | K09-12 | 5 |
| | 2 | K10-12 | 5 |
| | 3 | K09-20 | 5 |
| | 4 | K10-20 | 7 |
| | 5 | K07-5 | 5 |
| | 6 | K06-5 | 5 |
| | 7 | K07-11 | 5 |
| | 8 | K06-11 | 5 |
| | 9 | K07-15 | 5 |
| | 10 | K06-15 | 5 |
| | 11 | H16-22 | 15 |
| | 12 | H16-7 | 17 |
| | 13 | - | |
| | 14 | - | |
| | 15 | I05-26 | 11 |
| | 16 | G07-15 | 15 |
| | 17 | K06-19 | 5 |
| | 18 | G07-3 | 17 |
| | 19 | K07-19 | 5 |
| | 20 | G07-11 | 17 |
| | 21 | - | |
| | 22 | G07-21 | 15 |
| | 23 | - | |
| | 24 | J02-25 | 11 |
| | 25 | I06-10 | 13 |
| | 26 | J06-20 | 7 |
| | 27 | K08-X | 2 |
| | 28 | K08-X | 2 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 G

LS 63063400
ASSY



REV



1XXX (A)

1XXX (B)

143₈ (Read 1 + Write 1)

X7XX (B)

+ X5XX

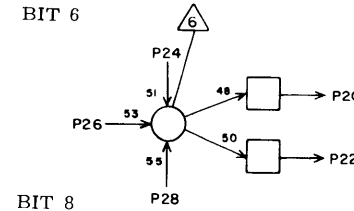
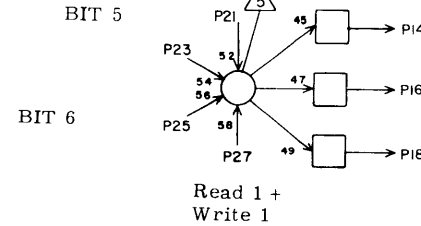
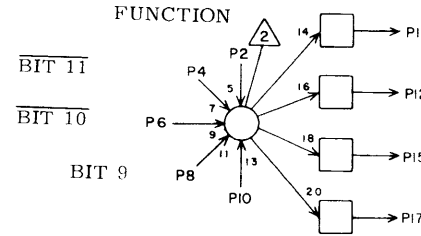
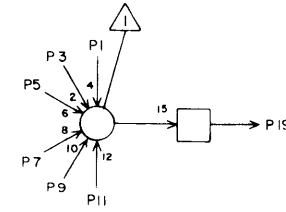
| TB | RV | G | K09 |
|----|----|--------|-----|
| | 1 | J02-16 | 11 |
| | 2 | L11- 7 | 9 |
| | 3 | J02- 5 | 11 |
| | 4 | L09-25 | 9 |
| | 5 | E09- 9 | 23 |
| | 6 | L09-23 | 9 |
| | 7 | K09- X | 2 |
| | 8 | L09-11 | 7 |
| | 9 | K09- X | 2 |
| | 10 | K09- X | 2 |
| | 11 | K09- X | 2 |
| | 12 | K08- 1 | 5 |
| | 13 | K05- 1 | 7 |
| | 14 | H05-12 | 15 |
| | 15 | I06- 7 | 11 |
| | 16 | H05-21 | 13 |
| | 17 | I06-23 | 11 |
| | 18 | D08- 6 | 27 |
| | 19 | H05- 5 | 15 |
| | 20 | K08- 3 | 5 |
| | 21 | J02-18 | 13 |
| | 22 | - | - |
| | 23 | J02- 9 | 13 |
| | 24 | L08-18 | 7 |
| | 25 | H04-18 | 15 |
| | 26 | K09- X | 2 |
| | 27 | K09- X | 2 |
| | 28 | L09- 5 | 5 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63063400
ASSY



REV



| TB | RV | G | K10 |
|----|----|--------|-----|
| | 1 | - | - |
| | 2 | L16- 7 | 11 |
| | 3 | - | - |
| | 4 | L14-25 | 11 |
| | 5 | - | - |
| | 6 | L14-23 | 11 |
| | 7 | - | - |
| | 8 | L14-11 | 9 |
| | 9 | - | - |
| | 10 | K10- X | 2 |
| | 11 | - | - |
| | 12 | K08- 2 | 5 |
| | 13 | K05- 2 | 9 |
| | 14 | G01-25 | 19 |
| | 15 | I06-13 | 11 |
| | 16 | F08-12 | 21 |
| | 17 | I06-25 | 11 |
| | 18 | - | - |
| | 19 | - | - |
| | 20 | K08- 4 | 7 |
| | 21 | I10- 3 | 11 |
| | 22 | - | - |
| | 23 | F07- 9 | 23 |
| | 24 | L13-18 | 7 |
| | 25 | H11-24 | 13 |
| | 26 | K10- X | 2 |
| | 27 | J07-16 | 9 |
| | 28 | L14- 5 | 9 |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63060900
ASSY REV 1

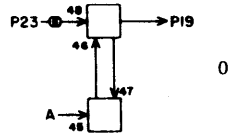
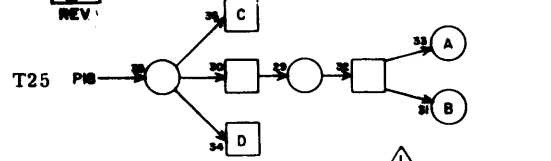
TO DATA CHANNEL A

BITS 0-5

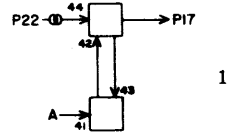
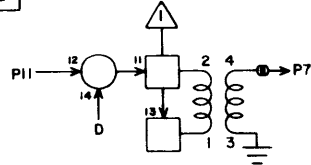
QJ

RV G

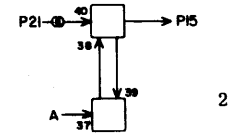
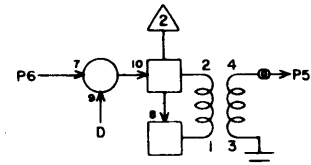
K11



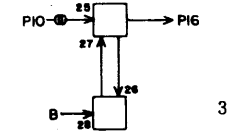
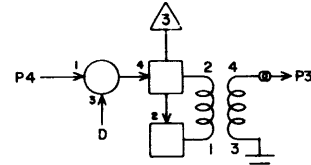
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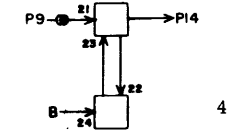
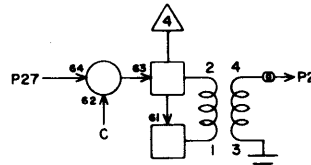
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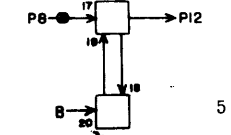
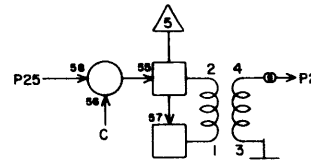
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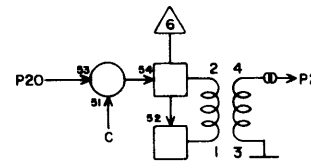
3



4



5



| RV | G | K11 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | I11-17 | 9 |
| 5 | - | |
| 6 | I11-18 | 9 |
| 7 | - | |
| 8 | - | |
| 9 | - | |
| 10 | - | |
| 11 | I11-13 | 9 |
| 12 | I12-1 | 11 |
| 13 | - | |
| 14 | I12-2 | 11 |
| 15 | I11-28 | 9 |
| 16 | I11-27 | 9 |
| 17 | I11-1 | 11 |
| 18 | J11-6 | 41 |
| 19 | I11-2 | 11 |
| 20 | I12-10 | 11 |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | - | |
| 25 | I12-13 | 11 |
| 26 | - | |
| 27 | I11-20 | 11 |
| 28 | - | |

JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60227300 F

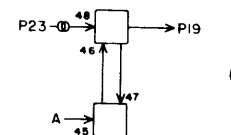
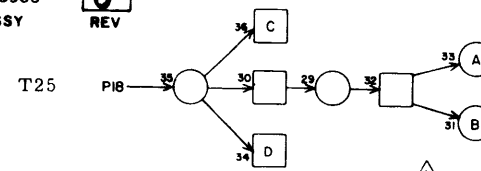
LS 63060900
ASSY REV

TO DATA CHANNEL A
BITS 6-11

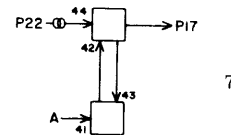
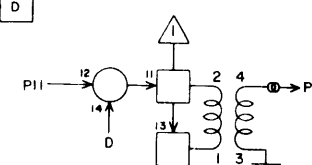
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RV G

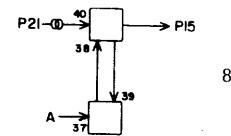
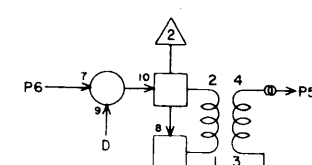
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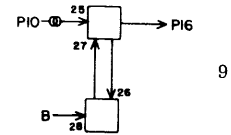
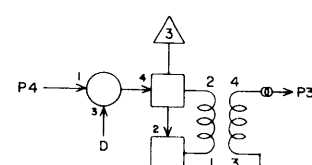
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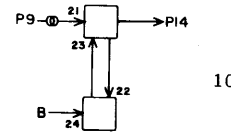
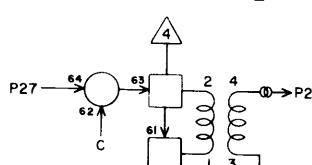
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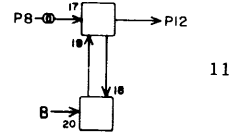
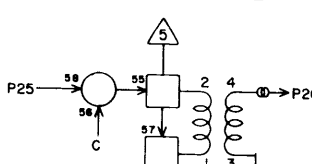
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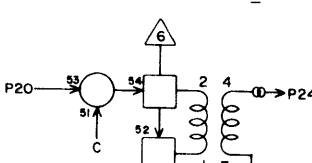
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10



11



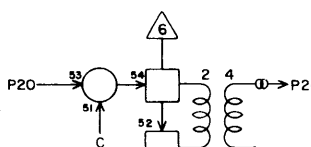
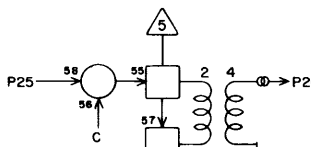
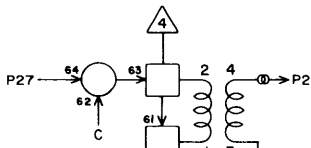
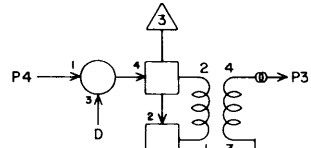
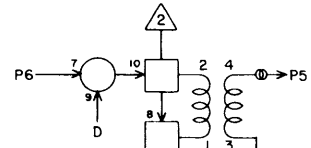
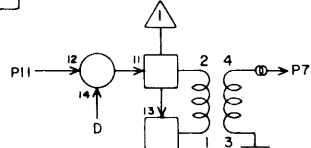
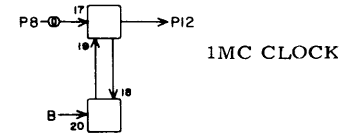
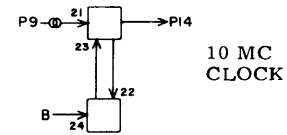
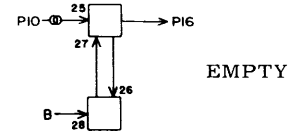
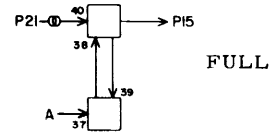
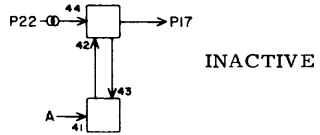
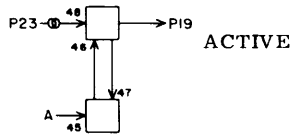
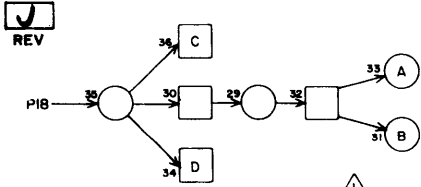
| RV | G | K12 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | I13-13 | 9 |
| 5 | - | |
| 6 | I12-20 | 9 |
| 7 | - | |
| 8 | - | |
| 9 | - | |
| 10 | - | |
| 11 | I12-17 | 9 |
| 12 | I13-27 | 9 |
| 13 | - | |
| 14 | I13-28 | 9 |
| 15 | I13-2 | 11 |
| 16 | I13-1 | 11 |
| 17 | I12-27 | 9 |
| 18 | J11-8 | 41 |
| 19 | I12-28 | 9 |
| 20 | I13-28 | 11 |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | - | |
| 25 | I13-17 | 11 |
| 26 | - | |
| 27 | I13-10 | 11 |
| 28 | - | |

JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60227300 F

TO DATA CHANNEL A SIGNALS

LS 63060900 ASSY REV



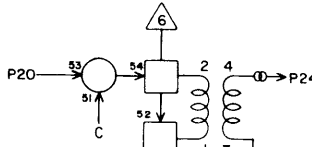
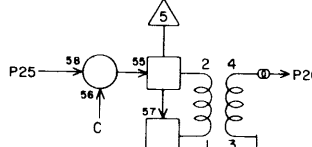
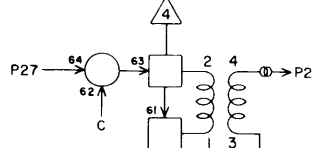
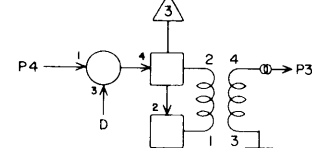
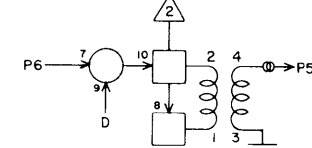
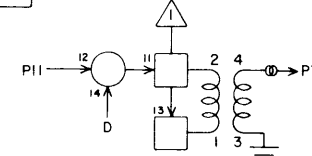
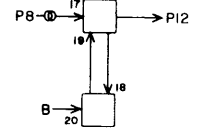
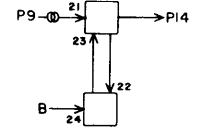
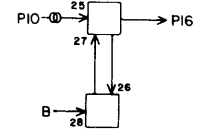
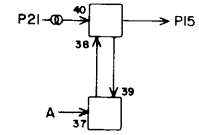
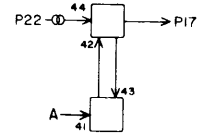
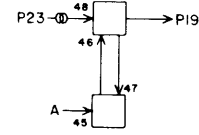
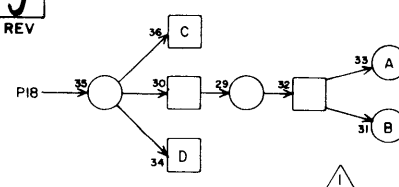
| RV | G | K13 | JACK | PIN | LG |
|----|--------|-----|------|-----|----|
| 1 | - | | | | |
| 2 | - | | | | |
| 3 | - | | | | |
| 4 | I09-16 | 11 | | | |
| 5 | - | | | | |
| 6 | I09-20 | 9 | | | |
| 7 | - | | | | |
| 8 | - | | | | |
| 9 | - | | | | |
| 10 | - | | | | |
| 11 | K13-19 | 5 | | | |
| 12 | K13-20 | 5 | | | |
| 13 | - | | | | |
| 14 | - | | | | |
| 15 | I09-17 | 11 | | | |
| 16 | I09-22 | 11 | | | |
| 17 | I09-25 | 11 | | | |
| 18 | J13- 4 | 7 | | | |
| 19 | K13-11 | 5 | | | |
| 20 | K13-12 | 5 | | | |
| 21 | - | | | | |
| 22 | - | | | | |
| 23 | - | | | | |
| 24 | - | | | | |
| 25 | K13- X | 2 | | | |
| 26 | - | | | | |
| 27 | I09-19 | 13 | | | |
| 28 | - | | | | |

CIRCUIT SPECIFICATION 11827600

60227300 F

TO DATA CHANNEL B BITS 0-5

LS 63060900 ASSY REV



| RV | G | K14 | JACK | PIN | LG |
|----|--------|-----|------|-----|----|
| 1 | - | | | | |
| 2 | - | | | | |
| 3 | - | | | | |
| 4 | I14-17 | 9 | | | |
| 5 | - | | | | |
| 6 | I14-10 | 9 | | | |
| 7 | - | | | | |
| 8 | - | | | | |
| 9 | - | | | | |
| 10 | - | | | | |
| 11 | I14-13 | 9 | | | |
| 12 | I15- 1 | 11 | | | |
| 13 | - | | | | |
| 14 | I15- 2 | 11 | | | |
| 15 | I14-20 | 9 | | | |
| 16 | I14-27 | 9 | | | |
| 17 | I14- 1 | 11 | | | |
| 18 | J14- 6 | 41 | | | |
| 19 | I14- 2 | 11 | | | |
| 20 | I15-10 | 11 | | | |
| 21 | - | | | | |
| 22 | - | | | | |
| 23 | - | | | | |
| 24 | - | | | | |
| 25 | I15-13 | 11 | | | |
| 26 | - | | | | |
| 27 | I14-20 | 11 | | | |
| 28 | - | | | | |

CIRCUIT SPECIFICATION 11827600

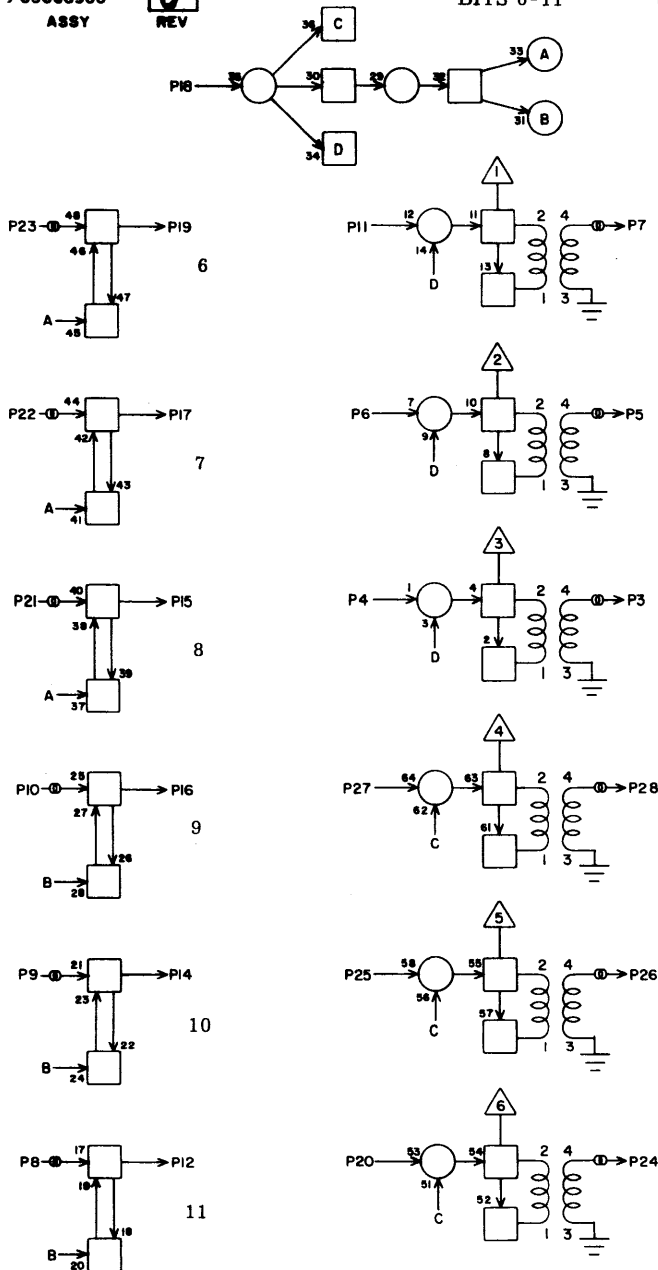
60227300 F

63060900
ASSY



TO DATA CHANNEL B
BITS 6-11

QJ



| RV | G | K15 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | I16-13 | 9 |
| 5 | - | |
| 6 | I15-20 | 9 |
| 7 | - | |
| 8 | - | |
| 9 | - | |
| 10 | - | |
| 11 | I15-17 | 9 |
| 12 | I16-27 | 9 |
| 13 | - | |
| 14 | I16-28 | 9 |
| 15 | I16- 2 | 11 |
| 16 | I16- 1 | 11 |
| 17 | I15-27 | 9 |
| 18 | J14- 8 | 41 |
| 19 | I15-28 | 9 |
| 20 | I16-20 | 11 |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | - | |
| 25 | I16-17 | 11 |
| 26 | - | |
| 27 | I16-10 | 11 |
| 28 | - | |

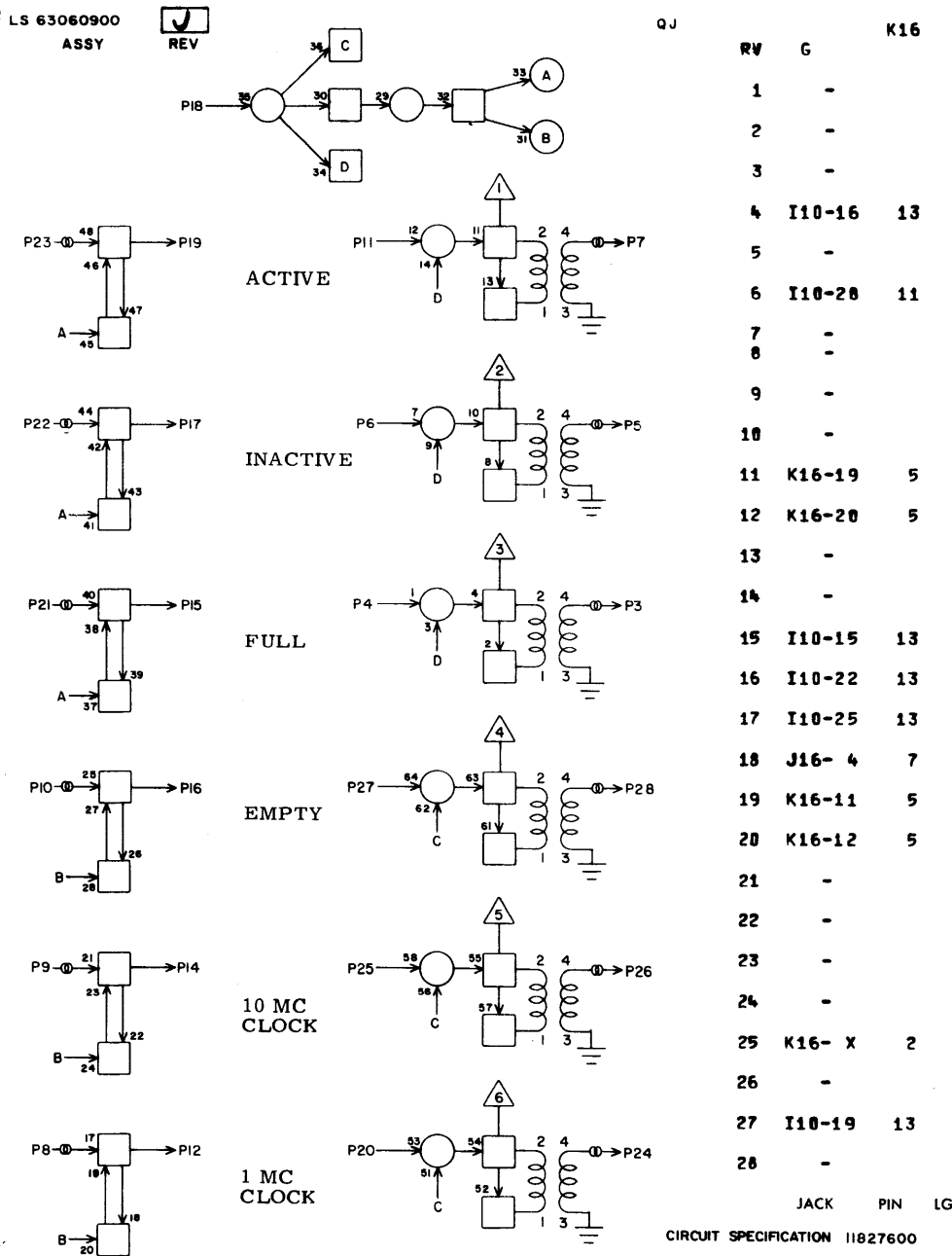
JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63060900
ASSY



TO DATA CHANNEL B
SIGNALS

QJ

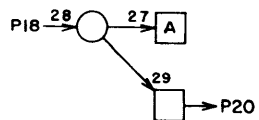
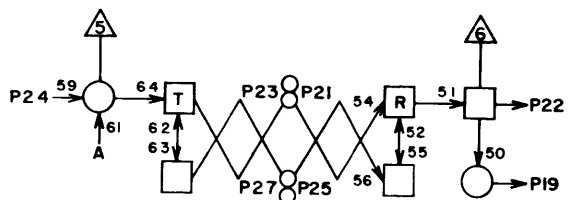
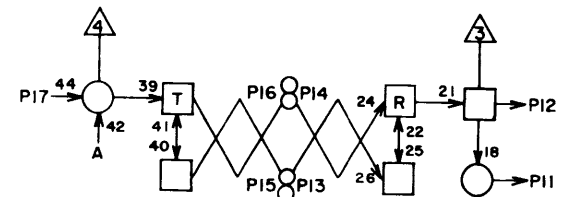
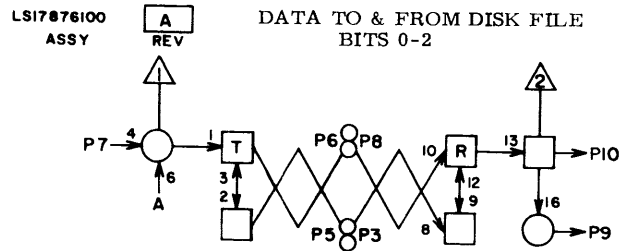


| RV | G | K16 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | I10-16 | 13 |
| 5 | - | |
| 6 | I10-28 | 11 |
| 7 | - | |
| 8 | - | |
| 9 | - | |
| 10 | - | |
| 11 | K16-19 | 5 |
| 12 | K16-20 | 5 |
| 13 | - | |
| 14 | - | |
| 15 | I10-15 | 13 |
| 16 | I10-22 | 13 |
| 17 | I10-25 | 13 |
| 18 | J16- 4 | 7 |
| 19 | K16-11 | 5 |
| 20 | K16-12 | 5 |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | - | |
| 25 | K16- X | 2 |
| 26 | - | |
| 27 | I10-19 | 13 |
| 28 | - | |

JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60227300 F



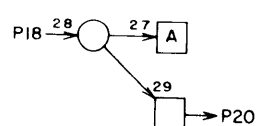
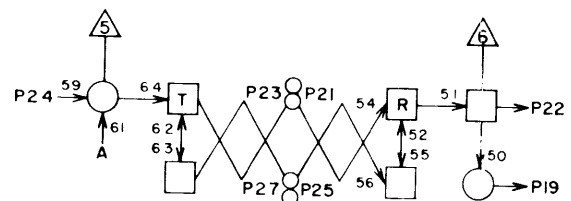
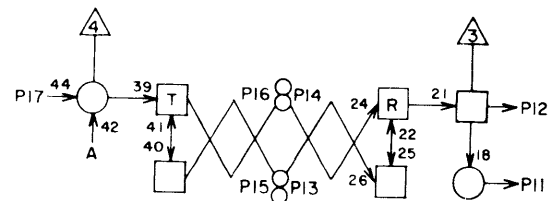
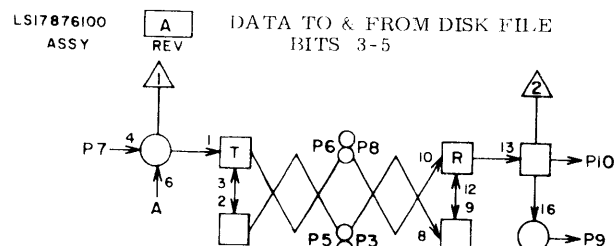
NOTES:

1. REFERENCE DRAWINGS:
17876500 LOGIC SCHEMATIC ZT
17876300 LOGIC SCHEMATIC ZR
2. THIS CIRCUIT IS A COMBINATION OF CIRCUITS ZR & ZT.
3. THE BASE RESISTORS ON TRANSISTOR 6, 42, & 61 ARE 150 OHMS.
4. THERE ARE ONLY TWO FILTER CAPACITORS. ONE BETWEEN +6V AND GROUND AND ONE BETWEEN -6V AND GROUND.

| RV | G | L01 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | I03-3 | 13 |
| 8 | - | |
| 9 | - | |
| 10 | J03-12 | 11 |
| 11 | - | |
| 12 | J03-13 | 11 |
| 13 | - | |
| 14 | - | |
| 15 | - | |
| 16 | - | |
| 17 | I03-9 | 15 |
| 18 | E02-25 | 25 |
| 19 | - | |
| 20 | L02-10 | 5 |
| 21 | - | |
| 22 | J03-16 | 11 |
| 23 | - | |
| 24 | I03-2 | 15 |
| 25 | - | |
| 26 | - | |
| 27 | - | |
| 28 | - | |

JACK PIN LG

60227300 F



NOTES:

1. REFERENCE DRAWINGS:
17876500 LOGIC SCHEMATIC ZT
17876300 LOGIC SCHEMATIC ZR
2. THIS CIRCUIT IS A COMBINATION OF CIRCUITS ZR & ZT.
3. THE BASE RESISTORS ON TRANSISTOR 6, 42, & 61 ARE 150 OHMS.
4. THERE ARE ONLY TWO FILTER CAPACITORS. ONE BETWEEN +6V AND GROUND AND ONE BETWEEN -6V AND GROUND.

| RV | G | L02 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | I03-27 | 11 |
| 8 | - | |
| 9 | - | |
| 10 | J03-19 | 9 |
| 11 | - | |
| 12 | J04-12 | 11 |
| 13 | - | |
| 14 | - | |
| 15 | - | |
| 16 | - | |
| 17 | I03-24 | 13 |
| 18 | L01-20 | 5 |
| 19 | - | |
| 20 | L03-10 | 5 |
| 21 | - | |
| 22 | J04-13 | 11 |
| 23 | - | |
| 24 | I03-26 | 13 |
| 25 | - | |
| 26 | - | |
| 27 | - | |
| 28 | - | |

JACK PIN LG

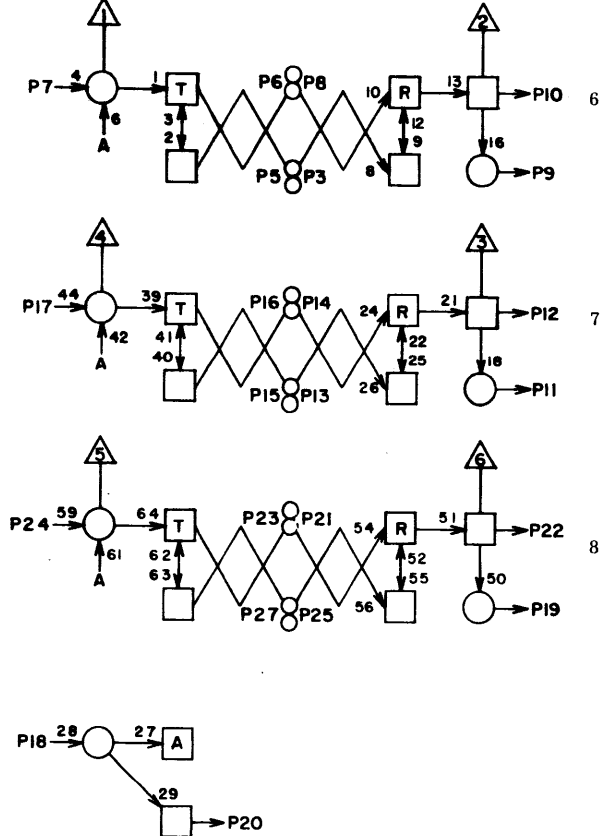
60227300 F

LS17876100
ASSY

A
REV

DATA TO & FROM DISK FILE
BITS 6-8

Z8



NOTES:

1. REFERENCE DRAWINGS:
17876500 LOGIC SCHEMATIC ZT
17876300 LOGIC SCHEMATIC ZR
2. THIS CIRCUIT IS A COMBINATION OF CIRCUITS ZR & ZT.
3. THE BASE RESISTORS ON TRANSISTOR 6, 42, & 61 ARE 150 OHMS
4. THERE ARE ONLY TWO FILTER CAPACITORS. ONE BETWEEN +6V AND GROUND AND ONE BETWEEN -6V AND GROUND.

JACK PIN LG

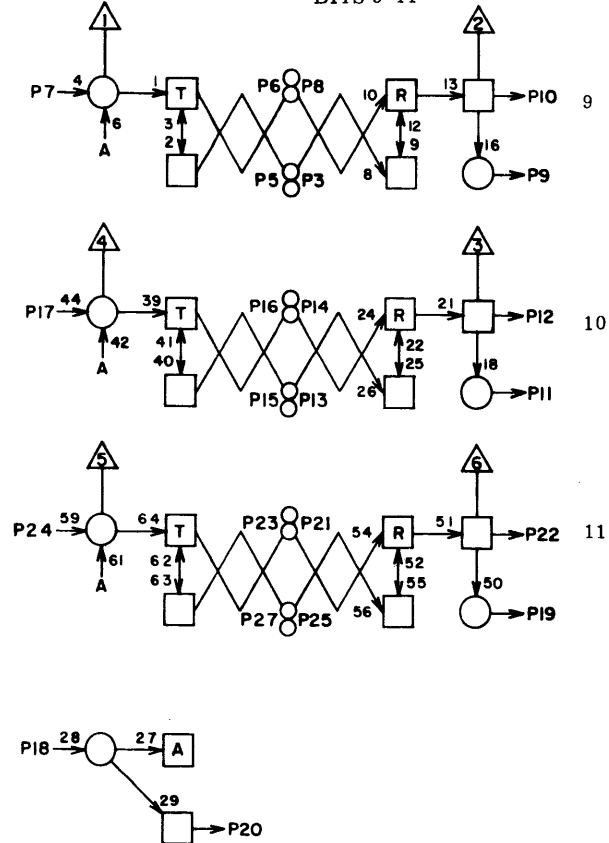
60227300 F

LS17876100
ASSY

A
REV

DATA TO & FROM DISK FILE
BITS 9-11

Z8



NOTES:

1. REFERENCE DRAWINGS:
17876500 LOGIC SCHEMATIC ZT
17876300 LOGIC SCHEMATIC ZR
2. THIS CIRCUIT IS A COMBINATION OF CIRCUITS ZR & ZT.
3. THE BASE RESISTORS ON TRANSISTOR 6, 42, & 61 ARE 150 OHMS.
4. THERE ARE ONLY TWO FILTER CAPACITORS. ONE BETWEEN +6V AND GROUND AND ONE BETWEEN -6V AND GROUND.

JACK PIN LG

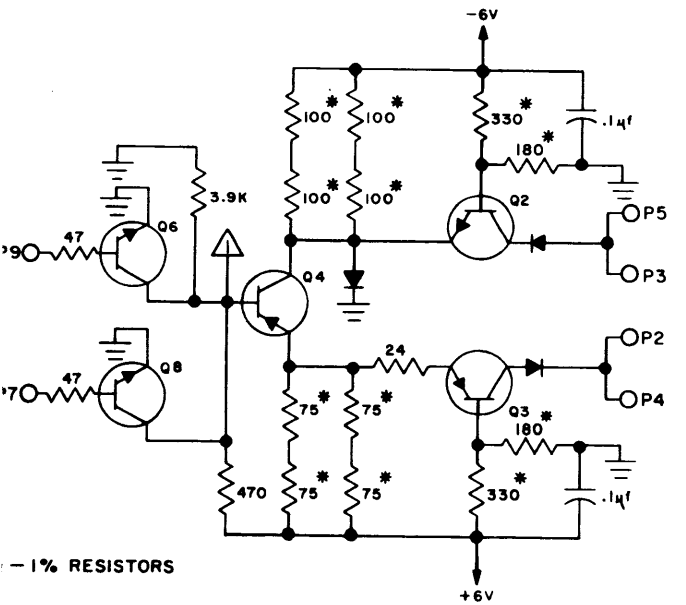
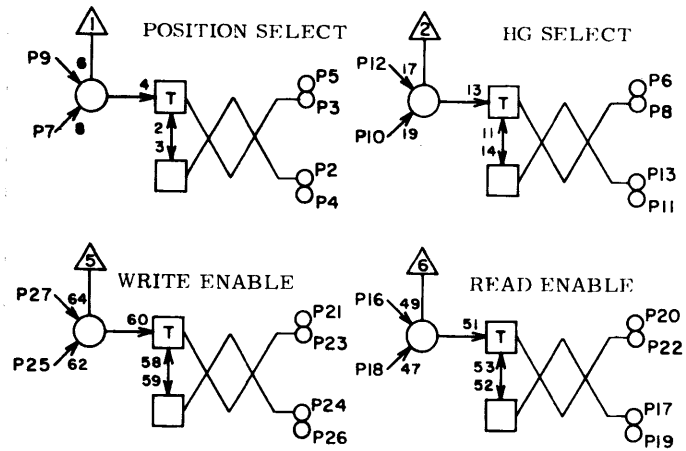
60227300 F

| RV | G | L03 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | I04-3 | 13 |
| 8 | - | |
| 9 | - | |
| 10 | J04-16 | 9 |
| 11 | - | |
| 12 | J04-19 | 9 |
| 13 | - | |
| 14 | - | |
| 15 | - | |
| 16 | - | |
| 17 | I04-9 | 13 |
| 18 | L02-20 | 5 |
| 19 | - | |
| 20 | L04-18 | 5 |
| 21 | - | |
| 22 | J05-12 | 11 |
| 23 | - | |
| 24 | I04-2 | 15 |
| 25 | - | |
| 26 | - | |
| 27 | - | |
| 28 | - | |

| RV | G | L04 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | I04-27 | 11 |
| 8 | - | |
| 9 | - | |
| 10 | J05-13 | 9 |
| 11 | - | |
| 12 | J05-16 | 9 |
| 13 | - | |
| 14 | - | |
| 15 | - | |
| 16 | - | |
| 17 | I04-24 | 13 |
| 18 | L03-20 | 5 |
| 19 | - | |
| 20 | - | |
| 21 | - | |
| 22 | J05-19 | 11 |
| 23 | - | |
| 24 | I04-26 | 13 |
| 25 | - | |
| 26 | - | |
| 27 | - | |
| 28 | - | |

LSI7876500
ASSY REV

ZT



- 1% RESISTORS

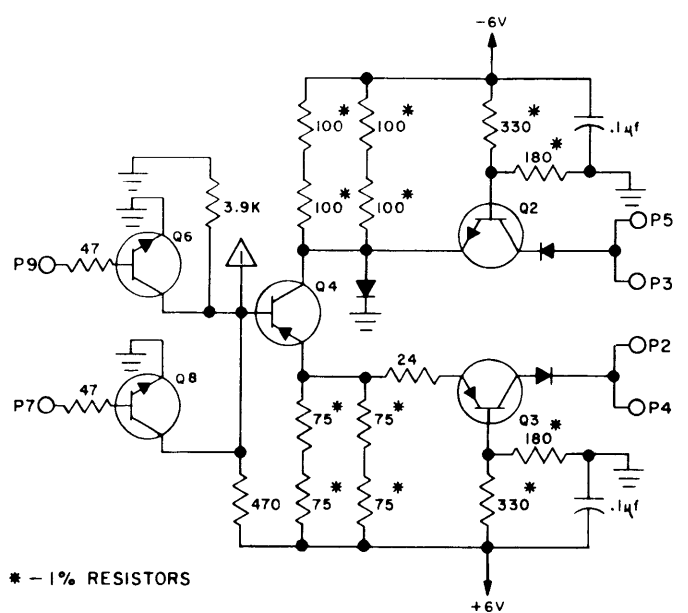
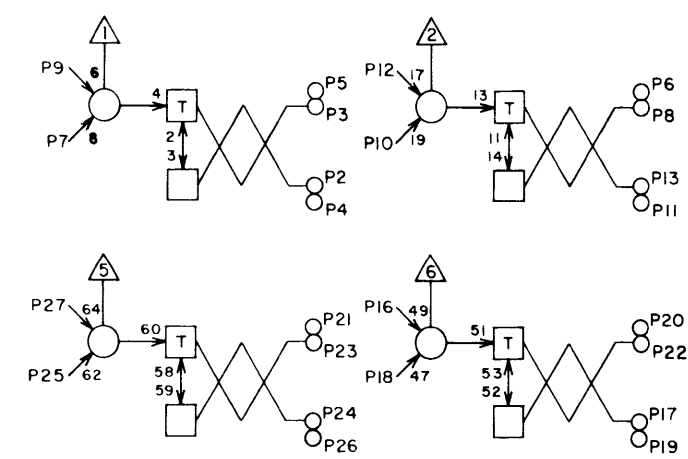
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|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | L05-X | 2 |
| 8 | - | |
| 9 | E02-1 | 27 |
| 10 | L05-X | 2 |
| 11 | - | |
| 12 | F06-2 | 23 |
| 13 | - | |
| 14 | - | |
| 15 | - | |
| 16 | E08-25 | 27 |
| 17 | - | |
| 18 | J08-19 | 11 |
| 19 | - | |
| 20 | - | |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | - | |
| 25 | J08-23 | 11 |
| 26 | - | |
| 27 | F05-27 | 23 |
| 28 | - | |

JACK PIN LG

60227300F

LSI7876500
ASSY REV

ZT



* - 1% RESISTORS

* Standard Option 10037

| RV | G | L06 |
|-----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | L06-X | 2 |
| 8 | - | |
| *9 | L06-x | 23 |
| 9 | C10-23 | 33 |
| 10 | L06-X | 2 |
| 11 | - | |
| *12 | L06-X | 2 |
| 12 | C10-14 | 33 |
| 13 | - | |
| 14 | - | |
| 15 | - | |
| 16 | - | |
| 17 | - | |
| 18 | - | |
| 19 | - | |
| 20 | - | |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | - | |
| 25 | - | |
| 26 | - | |
| 27 | - | |
| 28 | - | |

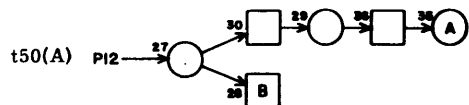
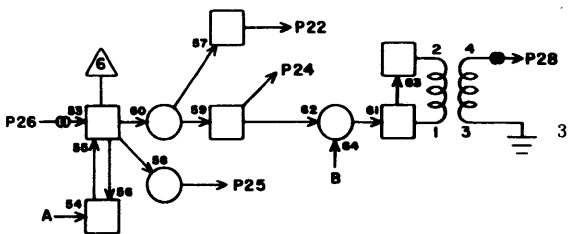
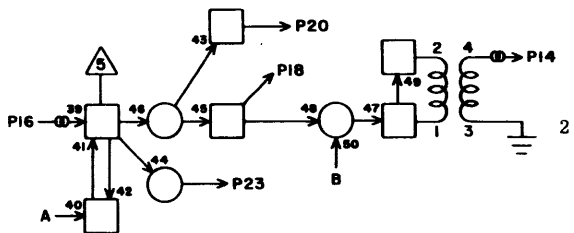
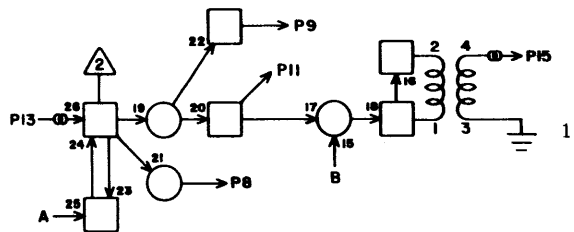
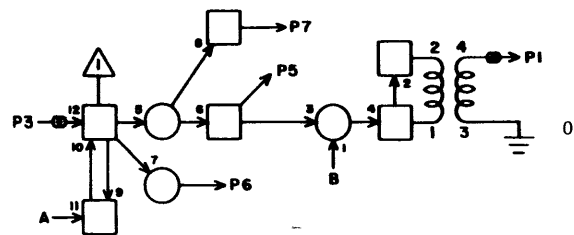
JACK PIN LG

60227300 G

LS 63060800 ASSY [F] REV

DATA FROM CHANNEL A
BITS 0 - 3

| Q1 | RV | G | L07 |
|----|--------|----|-----|
| 1 | - | - | |
| 2 | - | - | |
| 3 | - | - | |
| 4 | - | - | |
| 5 | I07-6 | 13 | |
| 6 | - | - | |
| *7 | - | - | |
| 7 | H16-8 | 21 | |
| 8 | - | - | |
| 9 | - | - | |
| 10 | - | - | |
| 11 | I07-7 | 13 | |
| 12 | J11-9 | 11 | |
| 13 | - | - | |
| 14 | - | - | |
| 15 | - | - | |
| 16 | - | - | |
| 17 | - | - | |
| 18 | I07-24 | 13 | |
| 19 | - | - | |
| 20 | - | - | |
| 21 | - | - | |
| 22 | - | - | |
| 23 | - | - | |
| 24 | I07-5 | 15 | |
| 25 | - | - | |
| 26 | - | - | |
| 27 | - | - | |
| 28 | - | - | |



* Standard Option 10037

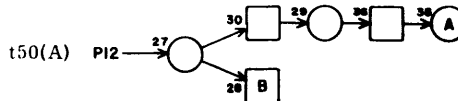
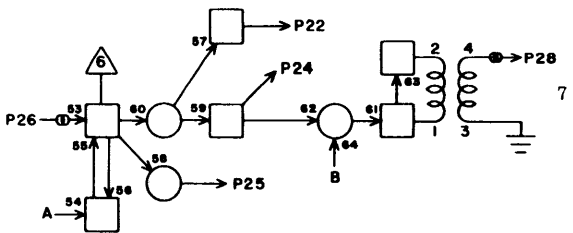
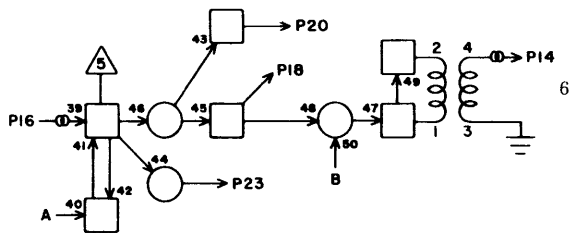
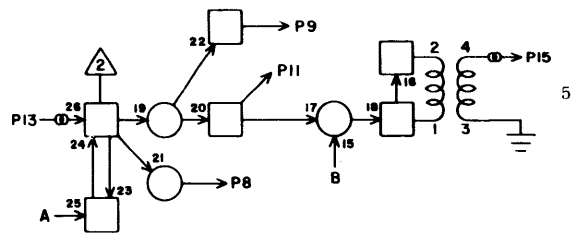
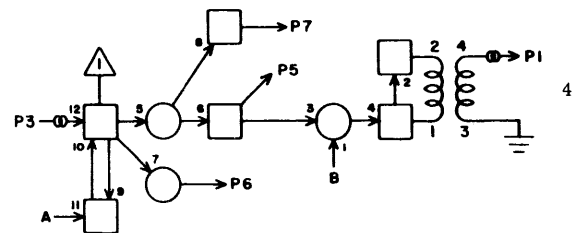
JACK PIN LG
CIRCUIT SPECIFICATION 11827600

60227300 G

LS 63060800 ASSY [F] REV

DATA FROM CHANNEL A

| Q1 | RV | G | L08 |
|----|--------|----|-----|
| 1 | - | - | |
| 2 | - | - | |
| 3 | - | - | |
| 4 | - | - | |
| 5 | I07-22 | 13 | |
| 6 | - | - | |
| 7 | - | - | |
| 8 | K06-13 | 7 | |
| 9 | H16-12 | 21 | |
| 10 | - | - | |
| 11 | I07-23 | 13 | |
| 12 | J11-11 | 11 | |
| 13 | - | - | |
| 14 | - | - | |
| 15 | - | - | |
| 16 | - | - | |
| 17 | - | - | |
| 18 | K09-24 | 7 | |
| 19 | - | - | |
| 20 | I08-6 | 13 | |
| 21 | - | - | |
| 22 | I08-7 | 13 | |
| 23 | - | - | |
| 24 | H16-5 | 23 | |
| 25 | - | - | |
| 26 | - | - | |
| 27 | - | - | |
| 28 | - | - | |



JACK PIN LG
CIRCUIT SPECIFICATION 11827600

60227300 G

LS 63060800
ASSY

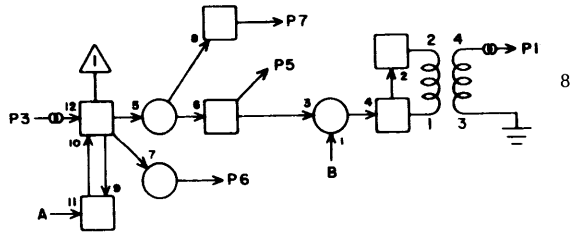
F
REV

DATA FROM CHANNEL A

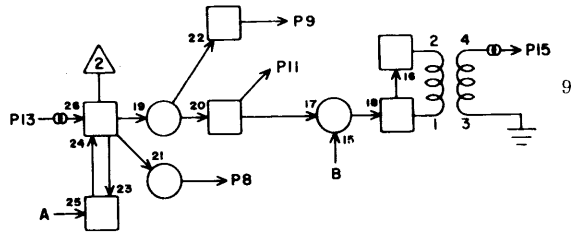
Q1

RV G

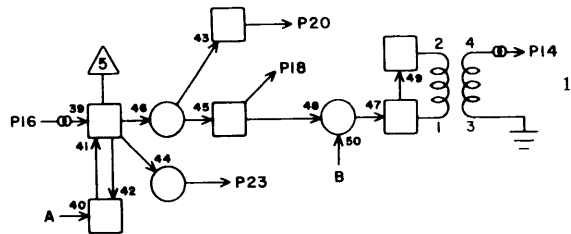
L09



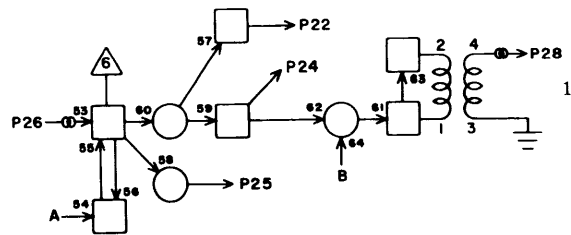
8



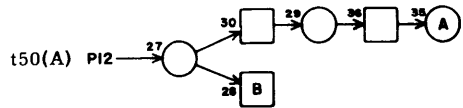
9



10



11



t50(A) PI2

JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63060800
ASSY

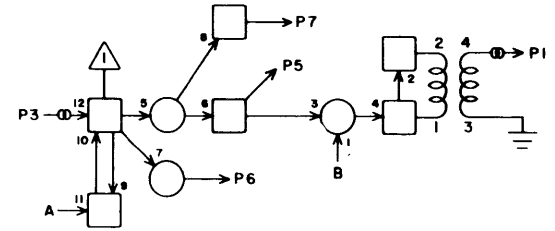
F
REV

SIGNALS FROM CHANNEL A

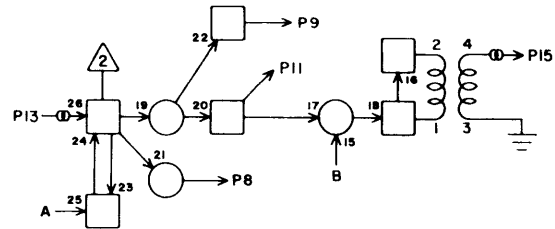
Q1

RV G

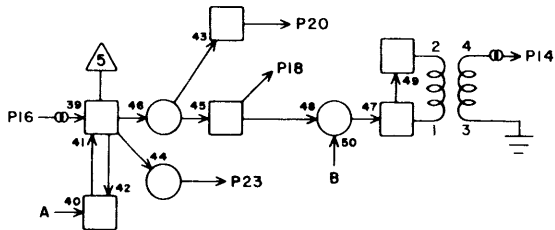
L10



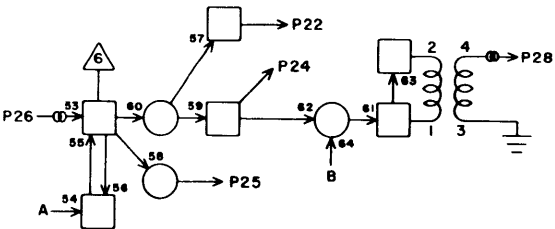
ACTIVE



INACTIVE

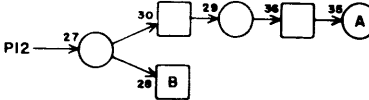


FULL



EMPTY

t50(A)

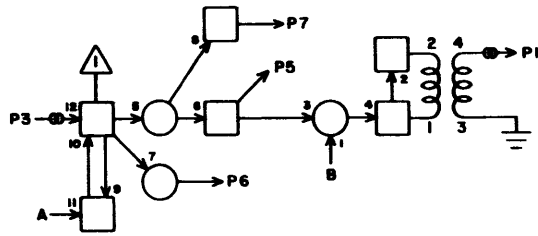


JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

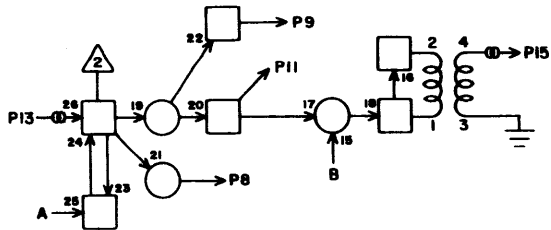
LS 63060800
ASSY REV

SIGNALS FROM CHANNEL A₀₁

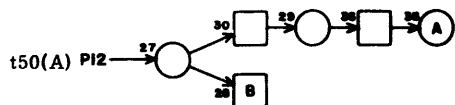
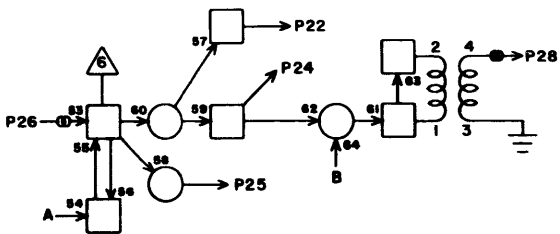
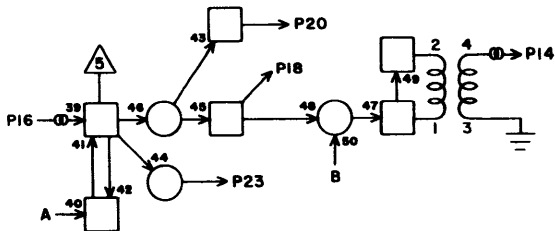
L11



FUNCTION



M. C.

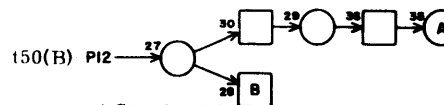
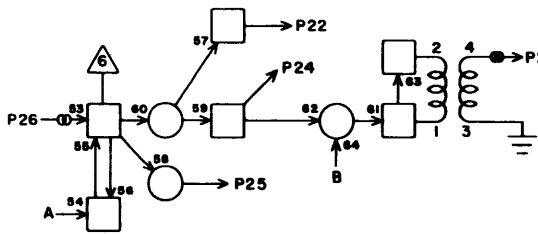
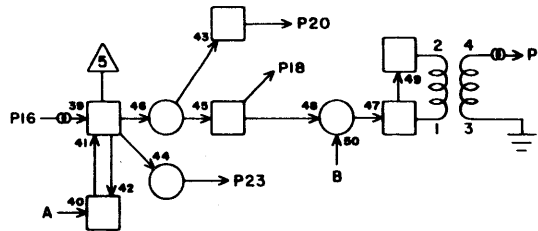
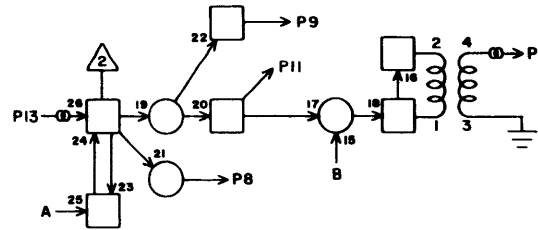
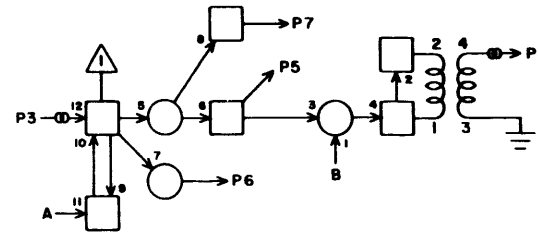


JACK PIN LG
CIRCUIT SPECIFICATION 11827800
60227300 F

LS 63060800
ASSY REV

DATA FROM CHANNEL B
BITS 0 - 3

L12



* Standard Option 10037

JACK PIN LG
CIRCUIT SPECIFICATION 11827800
60227300 G

| RV | G | L11 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | - | |
| 6 | - | |
| 7 | K09-2 | 9 |
| 8 | K06-17 | 9 |
| 9 | - | |
| 10 | - | |
| 11 | I05-21 | 15 |
| 12 | J11-13 | 9 |
| 13 | - | |
| 14 | - | |
| 15 | - | |
| 16 | - | |
| 17 | - | |
| 18 | - | |
| 19 | - | |
| 20 | - | |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | - | |
| 25 | - | |
| 26 | - | |
| 27 | - | |
| 28 | - | |

| RV | G | L12 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | I07-4 | 15 |
| 6 | - | |
| *7 | - | |
| 7 | H16-21 | 17 |
| 8 | - | |
| 9 | - | |
| 10 | - | |
| 11 | I07-13 | 15 |
| 12 | J14-9 | 11 |
| 13 | - | |
| 14 | - | |
| 15 | - | |
| 16 | - | |
| 17 | - | |
| 18 | I07-26 | 15 |
| 19 | - | |
| 20 | - | |
| 21 | - | |
| 22 | - | |
| 23 | - | |
| 24 | I07-3 | 17 |
| 25 | - | |
| 26 | - | |
| 27 | - | |
| 28 | - | |

LS 63060800
ASSY

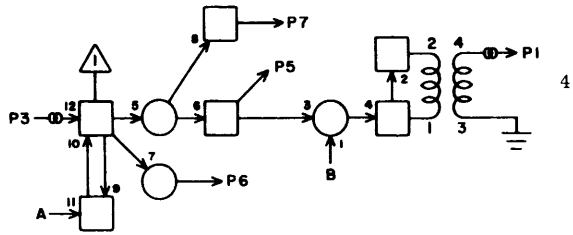
F
REV

DATA FROM CHANNEL B
BITS 4-7

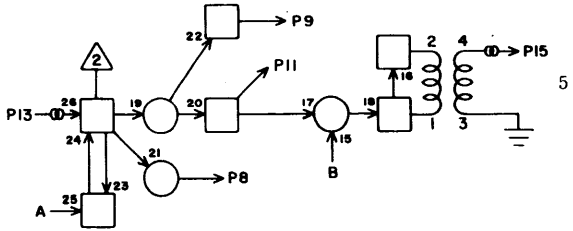
Q1

RV G

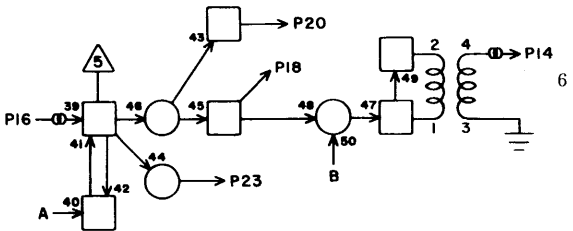
L13



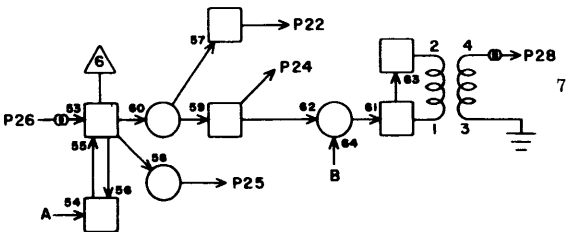
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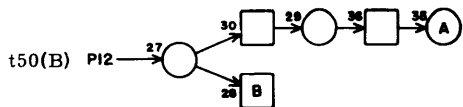
5



6



7



t50(B)

LS 63060800
ASSY

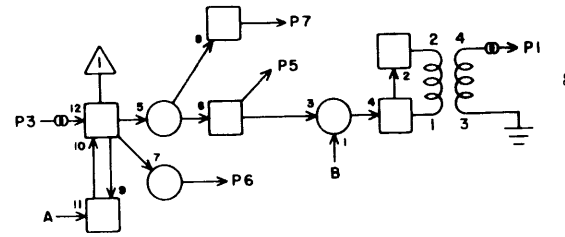
F
REV

DATA FROM CHANNEL B
BITS 8-11

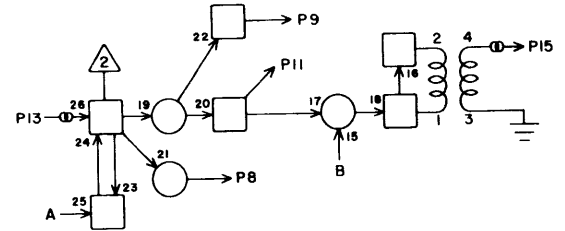
Q1

RV G

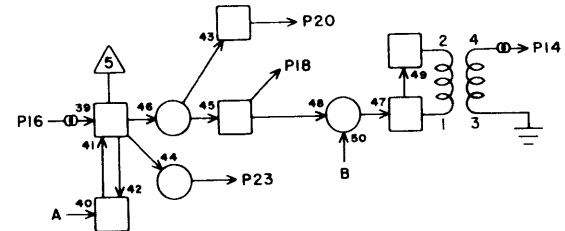
L14



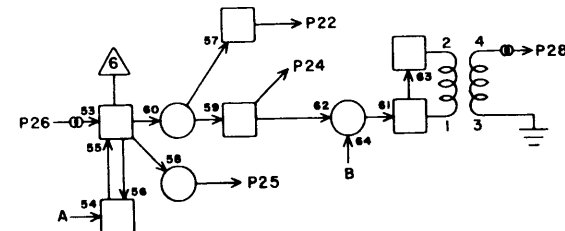
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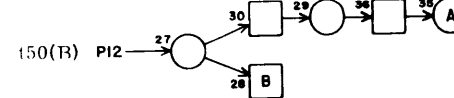
9



10



11



150(B)

| RV | G | L13 |
|----|--------|-----|
| 1 | - | |
| 2 | - | |
| 3 | - | |
| 4 | - | |
| 5 | I07-18 | 15 |
| 6 | | |
| 7 | | |
| 8 | K07-13 | 11 |
| 9 | H16-23 | 17 |
| 10 | - | |
| 11 | I07-25 | 15 |
| 12 | J14-11 | 11 |
| 13 | - | |
| 14 | - | |
| 15 | - | |
| 16 | - | |
| 17 | - | |
| 18 | K10-24 | 7 |
| 19 | - | |
| 20 | I08-4 | 17 |
| 21 | - | |
| 22 | I08-13 | 15 |
| 23 | - | |
| 24 | H16-24 | 17 |
| 25 | - | |
| 26 | - | |
| 27 | - | |
| 28 | - | |

JACK PIN LG
CIRCUIT SPECIFICATION 11827600

60227300 G

JACK PIN LG
CIRCUIT SPECIFICATION 11827600

60227300 F

LS 63060800
ASSY

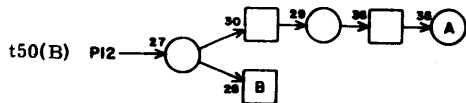
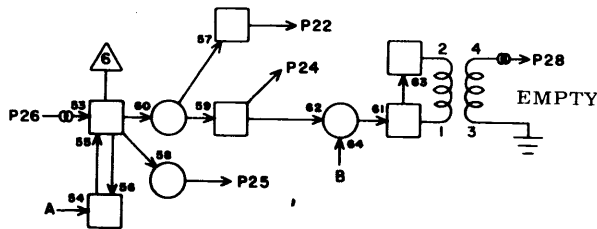
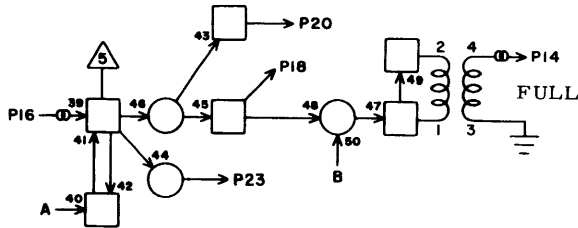
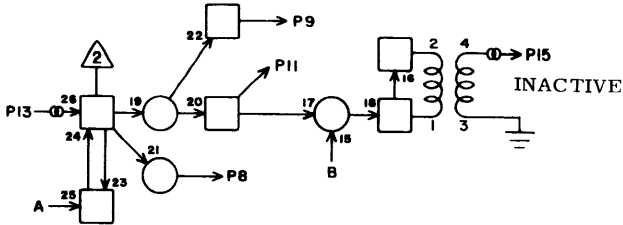
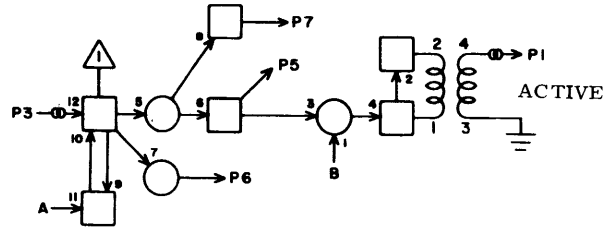
F
REV

SIGNALS FROM CHANNEL B

Q1

RV G

L15



JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

LS 63060800
ASSY

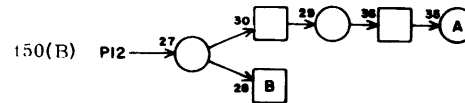
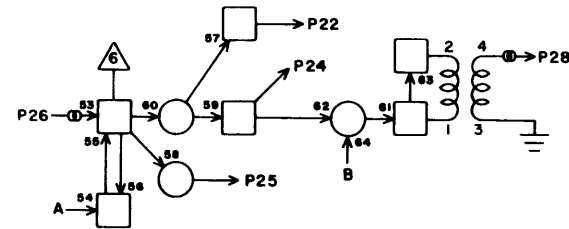
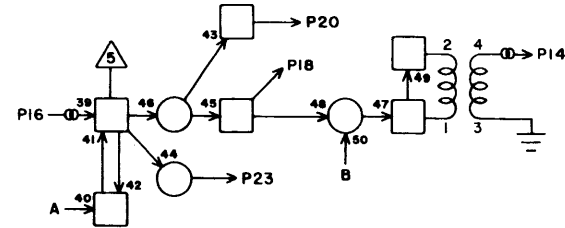
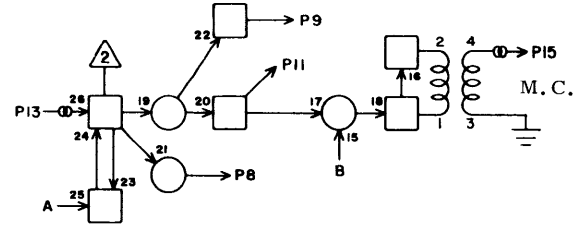
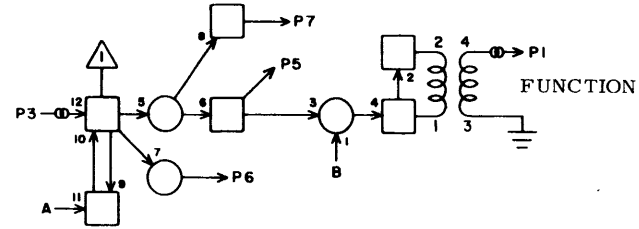
F
REV

SIGNALS FROM CHANNEL B

Q1

RV G

L16



JACK PIN LG
CIRCUIT SPECIFICATION 11827600
60227300 F

COMMENT SHEET

MANUAL TITLE CONTROL DATA® 6638/6639 DISK FILE SYSTEM

Standard Option 10037-A Customer Engineering Manual

PUBLICATION NO. 60227300 REVISION H

FROM: NAME: _____

BUSINESS
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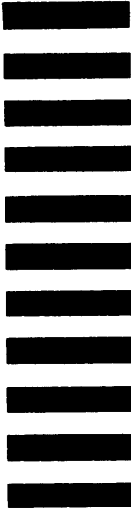
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