CONTROL DATA® CYBER 70™ SERIES MODEL 74 COMPUTING SYSTEM

CONTROL DATA
CORPORATION

The CONTROL DATA CYBER 70 Series/Model 74 is a large-scale, solid-state, general-purpose, digital computing system. Advanced design techniques incorporated into this system provide extremely fast operation in data processing and scientific computing applications. In addition, capability exists for multiprocessing, timesharing, multiprogramming, real-time, and hybrid applications. Its unusual multiple-computer architecture lends itself to high rates of input/output such as in — environments with large data bases or heavy communications.

The high-speed central processing unit (CPU) is composed of functional processors, with 10 separate arithmetic and logical units. These units operate in parallel, effectively achieving simultaneous execution of instructions. Twenty-four operating registers are also associated with the CPU, as well as an 8-word instruction stack, which has a two-word fetch-ahead capability.

A second CPU is available as an option. The CPU has a unified arithmetic section, with 24 operating registers (as in CONTROL DATA CYBER 70 Series/Model 73). Up to 20 peripheral processor units (PPU's), each with its own 4K, 12-bit word, one microsecond cycle memory, handle peripheral and input/output operations. Twelve to twenty-four data channels are serviced by the peripheral processors. Data channels are bi-directional and each data channel has a maximum data rate of two million characters per second. The SCOPE Operating System permits jobs to be assigned to a specific processor, so the user can schedule the CPU most effective to the particular job.

The Model 74 offers a wide selection of central memory (CM) and extended core storage (ECS) configurations. Central memory is common to both central processors and peripheral processors. Central memory is also organized in logically independent banks of 4096, 60-bit words, with available capacities ranging from 32K to 131K words.

ECS is arranged into logically independent multiphased memory banks. The transfer rate between ECS and central memory is up to 10 million words per second. ECS is available in sizes from 125K words to 2 million words and can be shared by separate CONTROL DATA CYBER 70 Systems.

The following peripheral equipment is available for use with the CDC CYBER 70 Series/Model 74:

- Magnetic Tape Transports
- Line Printers
- Console Displays
- Rotating Mass Storage
- Card Readers
- Card Punches
- Graphic Terminals
- Interactive Terminals
- Remote Batch Terminals
- Paper Tape Readers
- Paper Tape Punches

Interfacing equipment used with mass storage devices and communication subsystems has core memory and is programmable, allowing distribution of functions to these subsystems.

CDC's SCOPE Operating System and KRONOS Timesharing System both operate on the Model 74. These operating systems support an extensive product set, which includes COMPASS, FORTRAN RUN, FORTRAN EXTENDED, COBOL, ALGOL, SORT/MERGE, BASIC, APT (numerical control for machine tools), and OPHELIE (mathematical programming). A variety of data management products are available.

SPECIFICATIONS

Multi-Function Central Processor:

- Ten arithmetic and logical units
- Twenty-four operating registers
- Eight-word instruction stack with two-word look-ahead capability
- Integer multiply
- Central exchange jump
- Central memory access priority
- Real time clock
- Instruction issue rate:
  - For one CPU: 3.0 million instructions per second (MIPS)
  - For two CPU's: 3.7 million instructions per second (MIPS)

Serial-Function Central Processor (Optional Second CPU in System):

- Unified arithmetic unit, with 24 operating registers and a buffer register
- Integer multiply
- Central exchange jump

Programmable Peripheral Processors:

- 4K words (12 bit), 1 microsecond read/write memory
- Interlock register

Central Memory Options:

- 32K, 49K, 65K, 98K, and 131K, 60-bit words, 1 microsecond read/write time

Extended Core Storage:

- 10 million word-per-second transfer rate
- Distributive data path (DDP) — up to 4 peripheral processor units per DDP access to ECS.

  480 bit data path connecting the input/output channels to ECS. The DDP is controlled by the peripheral processors.

  One data path is standard in an ECS configuration with expansion to four paths per DDP unit for simultaneous data transfer to one ECS Controller port. Multiple DDP units (with up to four data paths per unit) can be configured in one CYBER 70 System.

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