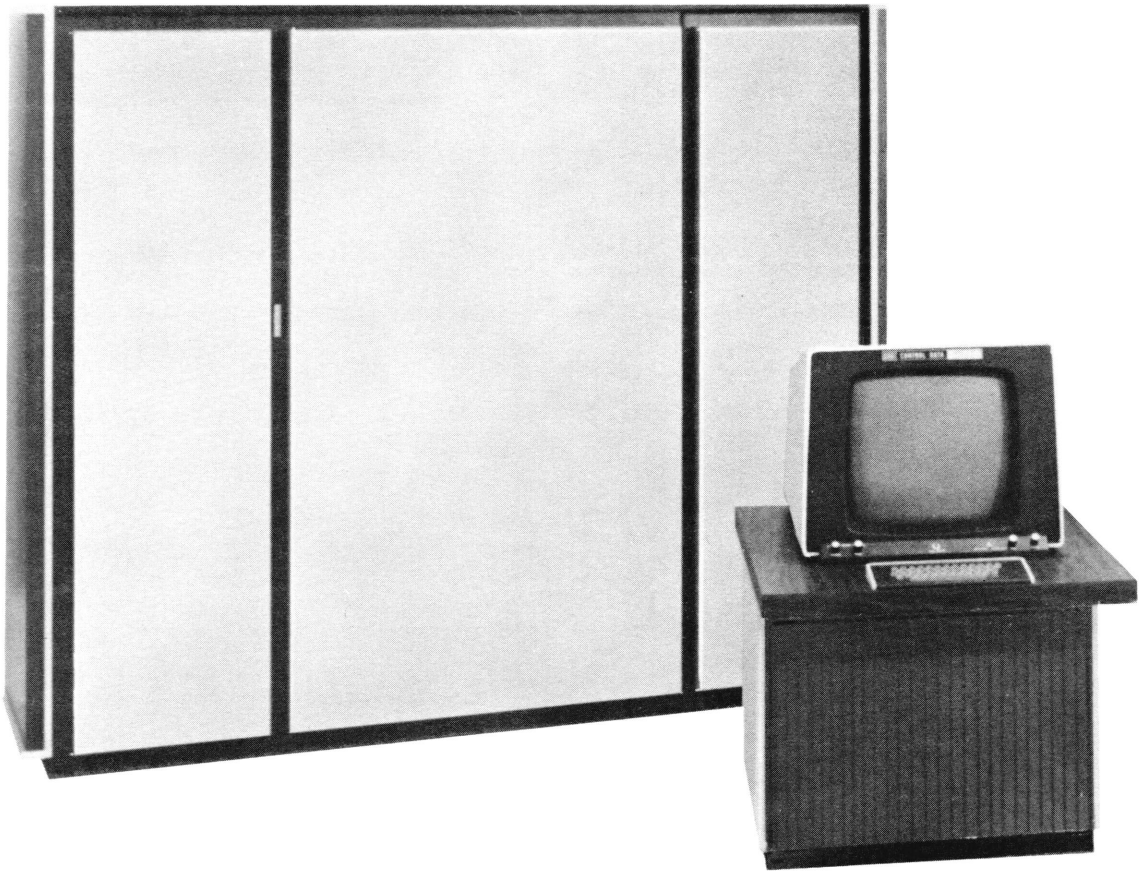
CONTROL DATA® CYBER 170 SERIES MODEL 172 COMPUTER SYSTEM

CONTROL DATA CORPORATION



The Model 172 is the smallest system of the CDC® CYBER 170 family of compatible computers. This system can be used as a central computer for batch operations and/or as the nucleus for networks of interactive terminals. It is suitable for data management applications, scientific computation, commercial data processing and data communications. Due to hardware and software compatibility among all CDC CYBER 170 systems, Model 172 serves as an expandable base for long-range growth plans.

Advanced circuit technology such as large-scale integration (LSI) and emitter-coupled logic (ECL) is used throughout the Model 172. Central memory also uses a metallic-oxide semiconductor (MOS) random access memory chip, which enables considerable size reduction in the overall system.

The basic mainframe includes:

- Central Processor Unit
- Central Memory Control
- Central Memory
- One Peripheral Processor Subsystem (ten peripheral processors)

Central Processor

The Model 172's central processor unit (CPU) consists of a basic arithmetic unit with 24 operating registers. The processor communicates with central memory via the central memory control (CMC). Because the CPU is isolated from the peripheral processor subsystem, computation is handled without obstructing other input/output requirements. Character-handling instructions are included in the instruction repertoire.

Central Memory Control

Central memory control is the system's control center, providing orderly flow of data between central memory and the requesting elements of the system.

Central Memory/Extended Core Storage

A wide selection of central memory (CM) and extended core storage (ECS) options are available to the Model 172 user. Central memory is organized in eight logically independent, phased banks of 60-bit words. This is metal-oxide semiconductor (MOS) memory, with a capacity range of 32K to 131K words. There are also eight single-error correcting, double-error detecting (SECDED) check bits per 60-bit word. This feature allows operation to continue unimpeded if a single bit failure should occur in central memory.

ECS is arranged in logically independent multiphased banks. The transfer rate between ECS and central memory is up to 10 million 60-bit words per second, where at least 500K words of ECS are available. ECS is available in sizes ranging from 125K words to 2 million words, and can be shared by separate CDC CYBER 170 Systems.

Peripheral Processor Subsystem

The peripheral processor subsystem (PPS) consists of 10 functionally independent computers (PPU's) with 4096 12-bit words (plus one parity bit) of MOS memory. The peripheral processors are programmable, and share access to central memory and 12 bi-directional I/O channels. All 10 peripheral processors form a multiplexing system which allows them to share common hardware for arithmetic, logical, and I/O operations without losing speed or independence.

The following peripheral equipment is available for use with the CDC CYBER 170/Model 172:

- Magnetic Tape Transports
- Line Printers
- Console Displays
- Rotating Mass Storage
- Card Readers
- Card Punches
- Graphic Terminals
- Interactive Terminals
- Remote Batch Terminals
- Communication Interfaces

Interfacing equipment used with mass storage devices and communication subsystems have independent memory facilities and are programmable via controlware (vendor supplied software). This allows distribution of control functions to these subsystems.

Software

All members of the CDC CYBER 170 family are supported by the CDC CYBER 170 Network Operating System — a single, powerful, multimode operating system. This system operates with an extensive software product set which includes: COMPASS (assembler language), FORTRAN, COBOL, ALGOL, APL, SORT/MERGE, BASIC, GPSS, SIMSCRIPT, APT (numerical control for machine tools), and a comprehensive set of basic data management software.

SPECIFICATIONS

High-Speed Central Processor —

- Basic arithmetic unit with 24 operating registers
- Compare and move instructions
- Central exchange jump
- Real-time clock
- CDC CYBER 70 compatible
- Address parity
- Data parity, with single-error correction, double-error detection (SECDED)
- I/O channel parity

Programmable Peripheral Processors —

- 4K words (12-bit) memory
- Status and control register

Central Memory (options) —

- 49K, 65K, 98K or 131K 60-bit words

Extended Core Storage —

- Maximum data transfer rate: 10 million words per second
- 125K to 2 million words in ECS
- Distributive Data Path (DDP): 480-bit data path connecting the input/output channel to ECS. The DDP is controlled by the peripheral processors.

  One data path is standard in an ECS configuration with expansion to four paths per DDP unit for simultaneous data transfer. Multiple DDP units (with up to four data paths per unit) can be configured in the CDC CYBER 170 System.

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