CONTROL DATA®
AC104-A CENTRAL PROCESSOR
DC111-A COMMUNICATIONS MODULE

Volume 2

DIAGRAMS
CABLE TABS

CONTROL DATA CORPORATION

CUSTOMER ENGINEERING MANUAL

D. LEIGH.

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AC104-A CENTRAL PROCESSOR
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Volume 2

DIAGRAMS
CABLE TABS

CONTROL DATA CORPORATION CUSTOMER ENGINEERING MANUAL

REVISION RECORD

REVISION	DESCRIPTION
01	Preliminary Edition. Information in this manual current through Product
(9-15-67)	Designation CPU01-A01 and CHB01-A01.
02	Engineering/Publication Change Order 17631. New Product Designation
(1-29-68)	CPU01-A02. Pages revised: 5-31, 5-37, 5-43, 5-49, 6-61, 6-63, 6-67, 6-69,
	6-73, 6-75, 6-79 and 6-81.
03	Publications Change Order 18576 which incorporates Engineering Change
(1-20-68)	Orders 17786, 17830 and 18343. New Product Designations are AC104-A03,
	CR105-A01 and DC111-A01. Pages revised: Cover, Title Page, Contents,
	1-1, 1-5, 1-7, 2-3, 2-5, 2-7, 2-9, 2-11, 2-13, 2-17, 2-19, 2-21, 2-23, 2-27, 2-37,
	2-41, 2-43, 2-45, 2-47, 2-49, 2-51, 2-53, 3-i, 3-19, 3-23, 3-29, 3-41, 4-1, 4-3,
	4-5, 4-7, 4-9, 4-11, 4-13, 4-15, 4-17, 4-19, 4-21, 4-23, 4-25, 4-27, 4-29, 4-31,
	4-33, 4-35, 4-37, 4-41, 4-43, 4-45, 4-47, 4-49, 4-51, 4-53, 4-55, 4-57, 4-59,
	4-67, 4-69, 4-73, 4-77, 4-79, 4-81, 4-83, 4-85, 5-7, 5-33, 5-35, 5-39, 5-41,
	5-45, 5-47, 5-51, 5-53, 5-89, 6-59, 6-65, 6-71, 6-77 and 6-83. Pages added:
	1-9, 1-11, 4-i, 6-197, 6-199, 6-201, 7-0, 7-1, 8-1, 8-3, 8-5, 8-7, 8-9, 8-11, 8-13,
	8-15, 8-17, 9-1, 9-2, 9-3, 9-4, 9-5, 9-7, 9-8, 9-9, 9-11, 9-13, 9-14, 9-15, 9-17,
	9-19, 9-21, 9-23, 9-25, 9-27, 9-29, 9-31, 9-33, 9-35, 9-37, 9-39, and 9-41.
A	Manual released; includes Field Change Order 18461, equipment level
(10-9-68)	AC104-A05 and Engineering Change Order 20696, publications change only.
	This printing obsoletes all previous editions.
B	Manual not affected. Engineering Change Order 20639.
(12-13-68)	
C	Manual revised. Engineering Change Order 20704, publication change
(12-13-68)	only. Page 8-7 revised.
D	Manual not affected. Engineering Change Order 20736.
(12-13-68)	
E	Manual revised. Engineering Change Order 21229, to incorporate
Publication No. 60181000	

REVISION	DESCRIPTION
E (Cont'd)	Engineering Change Orders 19601, 19861 and 19960 into this manual. Pages
(12-13-68)	1-14, 1-15, 2-1, 2-5, 2-8, 2-19, 2-23, 2-29, 2-37, 2-51, 2-52, 2-53, 2-65, 3-1,
	3-3, 3-7, 3-9, 3-11, 3-13, 3-17, 3-19, 3-23, 3-29, 3-35, 3-41, 3-43, 3-45, 3-51,
	3-63, 3-75, 3-77, 3-93, 3-97, 3-101, 3-103, 3-105, 3-111, 3-115, 3-117, 3-119,
	3-121, 3-123, 3-127, 3-135, 4-3, 4-5, 4-7, 4-9, 4-11, 4-13, 4-15, 4-19, 4-22,
	4-33, 4-37, 4-41, 4-43, 4-45, 4-49, 4-51, 4-53, 4-67, 4-79, 4-83, viii, ix, 6-5,
	6-7, 6-11, 6-13, 6-17, 6-51, 6-52, 6-57, 6-109, 6-121, 6-123, 6-131, 6-133,
	6-135, 6-137, 6-139, 6-167, 6-169, 6-171, 6-173, 6-175, 6-197, 8-5 and 8-7
	revised.
F	Manual revised; includes Engineering Change Order 21227, publication
(2-28-69)	change only. Pages 10-17, 10-19 and 10-21 revised.
G	Manual revised; includes Engineering Change Order 21773, publication
(2-28-69)	change only. Pages 1-5, 1-7, 1-15, 2-1, 2-19, 2-37, 3-5, 3-7, 3-9, 3-11, 3-13,
	3-19, 3-35, 3-43, 3-47, 4-1, 4-5, 4-7, 4-11, 4-13, 4-15, 4-19, 4-21, 4-31, 4-33,
	viii, 5-31, 5-33, 5-37, 5-39, 5-43, 5-45, 5-49, 5-51, 6-61, 6-63, 6-67, 6-69, 6-73,
	6-75, 6-79, 6-81, 10-3, 10-4, 10-5 and 10-7 revised.
H	Manual revised; includes Engineering Change Order 21714, equipment
(6-12-69)	level CR105-A02. Pages 10-5 and 10-7 revised.
J	Field Change Order 22076, equipment level AC104-A06. Page 1-4, 1-5, 2-3,
(10-8-70)	2-7, 2-9, 2-15, 2-17, 2-19, 2-21, 2-34, 2-35, 2-36, 2-37, 2-42, 2-43, 2-48, 2-49,
	2-70, 2-71, 3-3, 3-5, 3-7, 3-9, 3-11, 3-12, 3-13, 3-14, 3-15, 3-23, 3-29, 3-40,
	3-41, 3-107, 3-111, 3-113, 3-125, 3-127, 4-1, 4-3, 4-5, 4-8, 4-9, 4-10, 4-11,
	4-14, 4-15, 4-16, 4-17, 4-18, 4-19, 4-20, 4-21, 4-25, 4-26, 4-27, 4-29, 4-30,
	4-31, 4-33, 4-35, 4-37, 4-39, 4-44, 4-45, 4-48, 4-49, 4-51, 4-53, 4-57, 4-59,
	4-61, 4-67, 4-69, 4-79, 4-83 and 9-1 changed. Pages 2-6, 2-14, 2-16, 2-18,
	2-20, 3-22, 3-106, 3-108, 3-110, 3-112, 3-124, 3-126, 4-0, 4-4, 4-24, 4-28,
	4-32, 4-34, 4-38, 4-50, 4-52, 4-56, 4-58, 4-60, 4-66, 4-68, 9-21, 9-22, 9-23 and
	9-24 added.
K	Field Change Order 23184, equipment level AC104-A07. Page 2-11
(10-8-70)	changed.
L	Field Change Order 24499, equipment level AC104-A08. Pages 1-14, 1-15,
(10-8-70)	viii, ix, 5-23, 6-iii, 6-119, 8-1, 8-3, 8-5, and 8-9 changed.
N	Field Change Order 25019, equipment level CR105-A04. Pages 1-9,
(10-8-70)	10-17, 10-19 and 10-21 changed.
P	FC025308 CR105 - A04.

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4201 North Lexington Avenue
Arden Hills, Minnesota 55112

or use Comment Sheet in the back of this manual.

REVISION RECORD (sheet 2)

REVISION	DESCRIPTION
P	FCO 25308, modifies CR105, new equipment level CR105-A04
R	FCO 23835, modifies CR105, new equipment level CR105-A06
S	ECO 25918 Documentation change only
T	FCO 23691 & 25950, modifies AC104-A and DC111-A, new equipment levels AC104-A14, DC111-A02
U	FCO 24235, modifies AC104-A, new equipment level AC104-A11
V	FCO 25892, modifies CR105-A, new equipment level CR105-A08
W	FCO 26069, modifies CR105-A, new equipment level CR105-A07
Y	FCO 21066, modifies AC104-A, new equipment level AC104-A12
Z	FCO 23690, modifies AC104-A, new equipment level AC104-A13
AA	FCO 25840 " " " " " " A15
	FCO 26162 " " " " " A18
	FCO 27293 A19

REVISION	DESCRIPTION

Publication No.
60181000
Vol 2-

Address comments concerning this manual to:

or use Comment Sheet in the back of this manual.

5

REVISION W PUBLICATION NO. 60285300

TITLE: AC106 A, CR106 A, DC111 A, AT124-A C E Diagrams

C. E. TRAINING COPY.

REASON FOR CHANGE:

Field Change Order 23466, equipment level AC106-A01 thru A10 and AT124-A01 and A02. Is (1) improve the reliability and maintainability and to (2) reduce the manufacturing cost of the 3514 Computer System by replacing the present HSSP with one of a new design.

INSTRUCTIONS: Replace the following pages with the attached revised pages:

Rec of Revs

4-31	4-53	5-79
4-33	5-61	5-81
4-35	5-63	5-83
4-37	5-65	
4-39	5-67	10-31
4-41	5-69	10-33
4-43	5-71	
4-45	5-73	
4-47	5-75	
4-49	5-77	
4-51		

ORIGINATED BY _____ APPROVED _____ DATE _____

AA3148

Note: These prints were drawn for the AC-106. To be used on a AC-104 the page numbers will have to be changed. RB

FLIG - P/N 5231 5000
- P/N 1885 2500

New HSSP

FOREWORD

This manual contains customer engineering material for the CONTROL DATA® AC104-A Central Processor, DC111-A Communications Channel and CR105-A Console. It consists primarily of logic and power diagrams. A maintenance section will be added later on.

The manual is intended for use as a maintenance aid by personnel who have attended the CONTROL DATA training course on the above devices. It is not primarily a training manual and thus does not contain a detailed explanation of theory.

The following CONTROL DATA publications will also be useful in maintaining the above devices.

- 3500 Computer System Reference Manual
- 3500 Computer System Site Preparation Manual
- 3300/3500 Computer Systems Instruction Codes
- 3L00 System Maintenance Monitor Reference Manual
- Parts Data for AC104-A, DC111-A and CR105-A
- Maintenance Aids for AC104-A (Command Timing Charts)
- Maintenance Aids for AC104-A, DC111-A and CR105
  (Module Striptabs and Maps)
- INTEBRID® Circuits Manual
- 3000 Series Computer Systems Input/Output Specification IBM Selectric Series 73 Reference Manual
  (Applies to Console Typewriter)

GENERAL CONTENTS

CONTENTS - VOLUME 2

9

Part 7. Maintenance Panel and I/O Switch Panel

Part 8. Central Processor Power Wiring

Part 9. Central Processor Cable Tabs

Part 10. Console

Part 11. Maintenance

MAIN CONTROL

IA0

	0	1	2	3	4	5	6	7	8	9
	184626	184630	184626	184630	184626	184630	184626	184630	184626	184630
	02	01	02	01	03	01	02	01	02	01
	004	004	003	003	002	002	001	001	000	000
	2-63	2-83	2-61	2-81	2-59	2-79	2-57	2-77	2-55	2-75
A	D0, P1, P3, P6 BITS 12-14	B1, B2, B3, B6 BITS 12-14	D0, P1, P3, P6 BITS 09-11	B1, B2, B3, B6 BITS 09-11	D0, P1, P3, P6 BITS 06-08	B1, B2, B3, B6 BITS 06-08	D0, P1, P3, P6 BITS 03-05	B1, B2, B3, B6 BITS 03-05	D0, P1, P3, P6 BITS 00-02	B1, B2, B3, B6 BITS 00-02
	184884	184709	184884	183710	184884	183710	184884	183985	184884	
	01	01	01	01	01	01	01	01	01	
	004	000	003	001	002	000	001	000	000	
	2-73	2-85	2-71	2-89	2-69	2-87	2-67	2-91	2-65	
B	C0, F0, F1, S6 BITS 12-14	B6 CARRY NETWORK	C0, F0, F1, S6 BITS 09-11	S6 GATES	C0, F0, F1, S6 BITS 06-08	C3 GATES	C0, F0, F1, S6 BITS 03-05	P6 CARRY NETWORK	C0, F0, F1, S6 BITS 00-02	

IA1

	0	1	2	3	4	5	6	7	8	9
	184394	184394	184394	184008	184008	184008	184400	184008	184008	184008
	01	01	01	01	01	01	02	01	01	01
	005	004	003	011	010	009	000	008	007	006
	3-89	3-87	3-95	3-63	3-61	3-59	3-77	3-57	3-55	3-53
A	I0, I1, E1, E2 BITS 20-23	I0, I1, E1, E2 BITS 16-19	I0, I1, E1, E2 BITS 12-15	A1, A2, A3 ADDER BITS 20-23	A1, A2, A3 ADDER BITS 16-19	A1, A2, A3 ADDER BITS 12-15	GROUP CARRY INTERCHANGE	A1, A2, A3 ADDER BITS 08-11	A1, A2, A3 ADDER BITS 04-07	A1, A2, A3 ADDER BITS 00-03
	184394	184394	184394	184008	184008	184008	184007	184008	184008	184008
	01	01	01	01	01	01	01	01	01	01
	002	001	000	005	004	003	000	002	001	000
	3-83	3-81	3-79	3-75	3-73	3-71	3-51	3-69	3-67	3-65
B	I0, I1, E1, E2 BITS 08-11	I0, I1, E1, E2 BITS 04-07	I0, I1, E1, E2 BITS 00-03	Q1, Q2, Q3 ADDER BITS 20-23	Q1, Q2, Q3 ADDER BITS 16-19	Q1, Q2, Q3 ADDER BITS 12-15	ADDER CONTROLS	Q1, Q2, Q3 ADDER BITS 08-11	Q1, Q2, Q3 ADDER BITS 04-07	Q1, Q2, Q3 ADDER BITS 00-03

IA2

	0	1	2	3	4	5	6	7	8	9
	186090	186032	185850	186031	184635	184635	202934	186087	186094	
	01	03	01	02	01	01	03	04	01	
	000	000	000	000	000	001	000	000	000	
	4-27	4-11	4-9	4-1	4-3	4-7	4-13	4-5	4-21	
A	MAINTENANCE REGISTER	MEMORY REQUEST	MEMORY REQUEST TRANSLATIONS	START CONTROL	RNI 2 TIMING	RNI 3 TIMING	MAIN TIMING	INTERRUPT STOP	BLOCK RESTART	
	185849	186096	186097	186098	186089	185851	186088	186095	186009	186093
	04	03	01	01	01	02	01	03	03	01
	000	000	000	000	000	000	000	000	000	000
	4-25	4-37	4-35	4-23	4-29	4-33	4-31	4-15	4-17	4-19
B	D5 AND D6 CONTROL	CAC 2 AND 3	CAC 1	W3, 4, 5, AND 6 CONTROL	FUNCTION TRANSLATIONS	FUNCTION TRANSLATIONS	FUNCTION TRANSLATIONS	BCD FAULT	CONDITION REGISTER	OPERATION COMPLETE

MAIN CONTROL

IB0

	0	1	2	3	4	5	6	7	8	9
	184688	184688	184688	184710	185134	184691	184629	185220	184753	
	01	01	01	02	02	01	01	01	02	
	002	001	000	000	000	000	000	000	000	
	2-35	2-33	2-31	2-21	2-1	2-29	2-25	2-15	2-13	
A	C0, D0, F0, F1 BITS 21-23	C0, D0, F0, F1 BITS 18-20	C0, D0, F0, F1 BITS 15-17	S6, P6 CONTROLS	MAIN TIMING CHAIN	FUNCTION TRANSLATION-3	FUNCTION TRANSLATION-1	B8 ADD CYCLE CONTROLS	B5 ADD CHAIN CONTROLS	
		185116	185125	185239	184968	184852	184628	184945	185238	184851
		01	02	01	01	02	02	02	02	01
		000	000	000	000	000	000	000	000	000
		2-9	2-23	2-3	2-7	2-5	2-27	2-19	2-11	2-17
B		MISCELLANEOUS CONTROLS	C3, D2, D0 CONTROLS	MAIN CHAIN CYCLE EXITS	START ARITHMETIC MEMORY REQUEST	MAIN CHAIN CYCLE FFS	FUNCTION TRANSLATION-2	F0, F1, F8, P1, P3 CONTROLS	ADD TIMING CHAIN	B1, B2, B3, B4, B6 CONTROLS

ARITHMETIC

IB1

	0	1	2	3	4	5	6	7	8	9
	184395	184395	184395	184395	184779	183981	184395	184395	184395	184395
	01	01	01	01	01	01	01	01	01	01
	003	002	001	000	000	000	007	006	005	004
	3-105	3-103	3-101	3-99	3-95	3-97	3-113	3-111	3-109	3-107
A	X1, I2, I4 BITS 18-23	X1, I2, I4 BITS 12-17	X1, I2, I4 BITS 06-11	X1, I2, I4 BITS 00-05	I2-I5 ENABLE-A	I2-I5 ENABLE-B	X2, I3, I5 BITS 18-23	X2, I3, I5 BITS 12-17	X2, I3, I5 BITS 06-11	X2, I3, I5 BITS 00-05
	183898	183898	183898	183898	183969	184252	184393	185309	184391	184391
	01	01	01	01	02	01	01	01	01	01
	003	002	001	000	000	000	000	000	001	000
	3-123	3-121	3-119	3-117	3-115	4-39	3-91	3-93	3-127	3-125
B	EXPONENT ADDER AND REGISTER BITS 21-23	EXPONENT ADDER AND REGISTER BITS 18-20	EXPONENT ADDER AND REGISTER BITS 15-17	EXPONENT ADDER AND REGISTER BITS 12-14	EXPONENT CONTROLS	CHARACTER DISASSEMBLY	SHIFT COUNT ADDER	CONSTANT GENERATOR	MAINTENANCE REGISTER BITS 08-15 AND 20-23	MAINTENANCE REGISTER BITS 00-07 AND 16-19

BDP

IB2

	0	1	2	3	4	5	6	7	8	9
	185530	185531	185572	185680	186092	186091	186010	184472	185533	
	01	01	02	01	02	02	03	02	01	
	000	000	000	000	000	000	000	000	000	
	4-59	4-53	4-49	4-51	4-41	4-43	4-45	4-67	4-69	
A	D5 BITS 00-05 AND 12-17	C5 COMPARE NETWORK	J3, J5, AND J7	J4, D7, Z2, AND Z3	W2 A FIELD C FIELD LOOK-AHEAD	W2 C FIELD CURRENT CHARACTER	W2 EDIT CONTROLS	L1	L2	
	185530	185532	185544	185544	185562	186008	185282	185282	185543	185543
	01	01	01	01	01	01	01	01	02	02
	001	000	000	001	000	000	000	001	000	001
	4-61	4-57	4-63	4-65	4-55	4-47	4-71	4-75	4-73	4-77
B	D5 BITS 06-11 AND BITS 18-23	J8 AND J9	D5 BITS 00-31	D6 BITS 32-55	BCD ADDER	W2 CHARACTER GENERATOR	W3 BITS 00-05 W4 BITS 00-05	W5 BITS 00-05 W6 BITS 00-05	W3 BITS 06-11 W4 BITS 06-11	W5 BITS 06-11 W6 BITS 06-11

MAIN CONTROL / BDP / ARITHMETIC

IC0

	0	1	2	3	4	5	6	7	8	9
	184754	185237	185111	184830	186640	187050	187051	184582	184874	184874
	C2	01	01	01	01	00	01	01	02	02
	000	000	000	000	000	000	000	000	002	003
	2-37	2-43	2-53	2-39	2-41	4-79, 81	4-83, 85	3-1	3-9	3-11
A	STORAGE CONTROLS	INTERRUPT CONTROL	DIGIT COUNTER	ISR, OSR, CIR AND CONDITION REGISTER BITS 0, 1, 2	INTERRUPT CONTROLS AND CONDITION REGISTER BITS 3, 4, 5	W0 ASCII TO BCD	W1 BCD TO ASCII	MANUAL CONTROL	TIMING CHAIN T2 AND T3 MASTER	TIMING CHAIN T2 AND T3 SLAVE
	185110	184829	185112	184627				185504	184874	184874
	01	01	C2	01				C3	02	02
	000	000	000	000				000	000	001
	2-45	2-47	2-51	2-49				3-3	3-5	3-7
B	INTERRUPT MODE CYCLE CONTROLS	KEYBOARD CONTROLS	AUTO LOAD	GO, STOP, AND MASTER CLEAR				START, STOP	TIMING CHAIN T0 AND T1 MASTER	TIMING CHAIN T0 AND T1 SLAVE

ARITHMETIC

IC1

	0	1	2	3	4	5	6	7	8	9
	185277	185461	184729	184885	185275	185113	185534	185482	185135	185626
	02	01	03	01	02	01	01	03	02	02
	000	000	000	000	000	000	000	000	000	000
	3-43	3-45	3-47	3-49	3-31	3-33	3-35	3-37	3-39	3-41
A	I0 AND I1 ENABLES	I2 AND I3 ENABLES	I4 AND I5 ENABLES	I6 AND I7 ENABLES	FLOATING POINT ADD/SUBTRACT SEQUENCE	MULTIPLY SEQUENCE	DIVIDE SEQUENCE	COMPLEMENT AND MERGE	34, 35 IAI SEQUENCE	66.0 BDP SEQUENCE
	185542	185481	184583	184585		185505	185276	184643	184584	184586
	C3	00	02	02		01	01	02	03	03
	000	000	000	000		000	000	000	000	000
	3-23	3-25	3-27	3-29		3-21	3-13	3-15	3-17	3-19
B	FUNCTION TRANSLATION-A	FUNCTION TRANSLATION-B	FUNCTION TRANSLATION-C	FUNCTION TRANSLATION-D		CONSTANT DERIVATIONS	TIMING FANOUT	CYCLE COUNT	COUNT TRANSLATIONS	FAULTS AND CONDITIONS FOR BRANCHING

ARITHMETIC

IC2

	0	1	2	3	4	5	6	7	8	9
	184399	184399	184399	184398	184397	184397	184397	184397	184397	184397
	01	01	01	01	01	01	01	01	01	01
	002	001	000	000	005	004	003	002	001	000
	3-133	3-131	3-129	3-149	3-147	3-145	3-143	3-141	3-139	3-137
A	E3, E4 BITS 16-23	E3, E4 BITS 08-15	E3, E4 BITS 00-07	NORMALIZE SENSE TRANSLATIONS	SHIFT NETWORK LOWER 1, 2, 4 BITS 40-47	SHIFT NETWORK LOWER 1, 2, 4 BITS 32-39	SHIFT NETWORK LOWER 1, 2, 4 BIT 24-31	SHIFT NETWORK LOWER 1, 2, 4 BITS 16-23	SHIFT NETWORK LOWER 1, 2, 4 BITS 08-15	SHIFT NETWORK LOWER 1, 2, 4 BITS 00-07
		184006	184396	184396	184396	184396	184396	184396	184396	184396
		01	00	00	00	00	00	00	00	00
		000	007	006	005	004	003	002	001	000
		3-135	3-165	3-163	3-161	3-159	3-157	3-155	3-153	3-151
B		MBT AND MBO REGISTERS	SHIFT NETWORK UPPER 8, 16, 32 BITS 07, 15, 23, 31, 39, 47	SHIFT NETWORK UPPER 8, 16, 32 BITS 06, 14, 22, 30, 38, 46	SHIFT NETWORK UPPER 8, 16, 32 BITS 05, 13, 21, 29, 37, 45	SHIFT NETWORK UPPER 8, 16, 32 BITS 04, 12, 20, 28, 36, 44	SHIFT NETWORK UPPER 8, 16, 32 BITS 03, 11, 19, 27, 35, 43	SHIFT NETWORK UPPER 8, 16, 32 BITS 02, 10, 18, 26, 34, 42	SHIFT NETWORK UPPER 8, 16, 32 BITS 01, 09, 17, 25, 33, 41	SHIFT NETWORK UPPER 8, 16, 32 BITS 00, 08, 16, 24, 32, 40

NOTE:

① BDP MODULE

② THE 50-PAK PART NUMBER IS 8 DIGITS; THE LAST 2 DIGITS REPRESENT THE REVISION LEVEL OF THE 50-PAK. WHEN ORDERING A 50-PAK, USE THE 8-DIGIT PART NUMBER.

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE: CHASSIS MAP, UNIT I
MAIN CONTROL, ARITHMETIC, AND BDP

PRODUCT

SIZE C | DRAWING NO. 60181000 | REV. L

SHEET | PAGE VIII

BLOCK CONTROL

	1	2 ①	① 3	4	5	6 ①	① 7	8	9
184003	184003	185437	185437	183980		185437	185437	184003	184003
01	01	01	01	01		01	01	01	01
003	002	003	002	000		001	000	001	000
6-153	6-149	6-139	6-137	6-157		6-135	6-133	6-145	6-141
A	CHANNEL 3 Ø LOWER	CHANNEL 2 Ø LOWER	CHANNEL 3 C CONTROLS	CHANNEL 2 C CONTROLS	Ø LOWER FAN-IN		CHANNEL 1 C CONTROLS	CHANNEL 0 C CONTROLS	CHANNEL 1 Ø LOWER	CHANNEL 0 Ø LOWER
184003	184003	185415	185415		183980	185415	185415	184003	184003
01	01	01	01		01	01	01	01	01
011	010	003	002		001	001	000	009	008
6-155	6-151	6-131	6-129		6-159	6-127	6-125	6-147	6-143
B	CHANNEL 3 Ø UPPER	CHANNEL 2 Ø UPPER	CHANNEL 3 A CONTROLS	CHANNEL 2 A CONTROLS	Ø UPPER FAN-IN		CHANNEL 1 A CONTROLS	CHANNEL 0 A CONTROLS	CHANNEL 1 Ø UPPER	CHANNEL 0 Ø UPPER
		②	②				②	②		

BLOCK CONTROL

2A1

	0	1	2	3	4	5	6	7	8	9
	185301	185301	185301	185301	184660	183984	183984	183984	184700	
50-PAK PART NO.	00	00	00	00	01	01	01	01	00	
SERIAL NO.	003	002	001	000	000	000	001	002	000	
PAGE NO.	6-79	6-73	6-67	6-61	6-59	6-47	6-49	6-51	6-55	
	6-81	6-75	6-69	6-63						
	6-83	6-77	6-71	6-65						
A	REGISTER FILE LOCATIONS 40-77, UPPER 12	REGISTER FILE LOCATIONS 40-77, LOWER 12	REGISTER FILE LOCATIONS 00-37, UPPER 12 AND 2 CONTROL	REGISTER FILE LOCATIONS 00-37, LOWER 12 AND 2 CONTROL	SO REGISTER AND ADDRESS TRANSLATION	ZO REGISTER BITS 04-07	ZO REGISTER BITS 08-11	ZO REGISTER BITS 12-15	ZO REGISTER BITS 20-23	
					185161	185379	185380	184854	184853	
					01	00	01'	01	01	
					000	000	000	000	000	
					6-57	6-45	6-43	6-41	6-53	
B					ZO TRANSLATION	ZO REGISTER BITS 00-03	ZO CONTROL	TIMING CHAIN T150-T157	ZO REGISTER BITS 16-19	

RELOCATION

2A2

	0	1	2	3	4	5	6	7	8	9
	185301	185301	185301	185301	184699	184992	185210	184875	183374	183374
	00	00	00	00	02	01	05	01	01	01
	007	006	005	004	000	000	000	000	000	001
	5-49	5-43	5-37	5-31	5-7	5-3	5-1	5-5	5-9	5-11
	5-51	5-45	5-39	5-33						
	5-53	5-47	5-41	5-35						
A					PAGE FILE ADDRESS TRANSLATION AND TIMING CHAIN	PAGE FILE MISCELLANEOUS CONTROL	PAGE FILE PRIORITY AND ADDRESS CHANGE DETECTOR	STORAGE INTERFACE CONTROL AND TIMING	ADDRESS BUS AND PARITY BITS 00, 02, 04, 08	ADDRESS BUS AND PARITY BITS 01, 03, 05, 07
					185236	184755	184755	184755	184663	186443
					01	01	01	01	01	01
					000	002	001	000	000	000
					5-21	5-19	5-17	5-15	5-13	5-23
B	PAGE FILE QUADRANT 3	PAGE FILE QUADRANT 2	PAGE FILE QUADRANT 1	PAGE FILE QUADRANT 0	ADDRESS BUS BITS 06 AND 17, AND ILLEGAL WRITE	ADDRESS BUS BITS 15 AND 16	ADDRESS BUS BITS 13 AND 14	ADDRESS BUS BITS 11 AND 12	ADDRESS BUS BITS 09 AND 10	ILLEGAL WRITE SWITCH COMPARE

BLOCK CONTROL

2B0

	③ 0	③ 1	③ 2	③ 3	4	5	6	7	8	9
	184658	184658	184658	184658	183986	183987	183987	184659	185416	185649
	01	01	01	01	01	01	01	01	01	01
	003	002	001	000	000	001	000	000	000	000
	6-91	6-89	6-87	6-85	6-103	6-123	6-121	6-117	6-109	6-101
A	CHANNEL 3 B CONTROLS	CHANNEL 2 B CONTROLS	CHANNEL 1 B CONTROLS	CHANNEL 0 B CONTROLS	CHANNEL 0,1,4,5 COMMON CONTROLS	ODD STATUS FAN-IN	EVEN STATUS FAN-IN	INTERNAL MASK AND INTERRUPT	INTERRUPT PRIORITY 1 AND 4	FO TRANSLATIONS B CONTROLS
	184658	184658	184658	184658	183986	185677	183983	183983	185293	
	01	01	01	01	01	01	01	01	01	
	007	006	005	004	001	000	001	000	000	
	6-99	6-97	6-95	6-93	6-105	6-107	6-115	6-113	6-111	
B	CHANNEL 7 B CONTROLS	CHANNEL 6 B CONTROLS	CHANNEL 5 B CONTROLS	CHANNEL 4 B CONTROLS	CHANNEL 2,3,6,7 COMMON CONTROL	CHANNEL COUPLER CONTROL	ODD INTERRUPT FAN-IN	EVEN INTERRUPT FAN-IN	INTERRUPT PRIORITY 2 AND 3	
	③	③	③	③						

BLOCK CONTROL

2B1

	0	1	2	3	4	5	6	7	8	9
	185304	185438	183988	183988	183988	183982	185458	184854	185414	185460
	01	01	00	00	00	01	01	01	01	01
	000	000	005	004	003	000	000	001	000	000
	6-5	6-25	6-39	6-37	6-35	6-19	6-13	6-1	6-17	6-23
A	BLOCK CONTROL PRIORITY 1 AND 4	REGULAR FILE ADDRESS TRANSLATION AND SEARCH BUFFER	D4 REGISTER BITS 05,11,17,23	D4 REGISTER BITS 04,10,16,22	D4 REGISTER BITS 03,09,15,21	I/O ENABLES CHANNEL 0-3	D4 I/O AND SEARCH/ MOVE CONTROL	TIMING CHAIN T158-T165	MISCELLANEOUS CONTROL	FO TRANSLATION
	185304	185417	183988	183988	183988	183982	185413	185391	185459	185281
	01	03	00	00	00	01	02	01	01	01
	001	000	002	001	000	001	000	000	000	000
	6-7	6-9	6-33	6-31	6-29	6-21	6-15	6-3	6-11	6-27
B	BLOCK CONTROL PRIORITY 2 AND 3	CLEAR SEQUENCE AND CONNECT/ FUNCTION CONTROL	D4 REGISTER BITS 02,08,14,20	D4 REGISTER BITS 01,07,13,19	D4 REGISTER BITS 00,06,12,18	I/O ENABLES CHANNEL 4-7	D4 CONTROL	TIMING CHAIN T166 AND T265-T268	TYPEWRITER, CLOCK, AND PROGRAM CONTROL	TYPEWRITER REGISTER AND SWITCHES

RELOCATION

2B2

	0	1	2	3	4	5	6	7	8	9
		184668	184668	184668	184668	183989	184668	184668	184668	184668
		01	01	01	01	01	01	01	01	01
		007	006	005	004	000	003	002	001	000
		5-71	5-69	5-67	5-65	5-73	5-63	5-61	5-59	5-57
A	DATA BUS BITS 21-23	DATA BUS BITS 18-20	DATA BUS BITS 15-17	DATA BUS BITS 12-14	DATA BUS PARITY BITS 24-27	DATA BUS BITS 09-11	DATA BUS BITS 06-08	DATA BUS BITS 03-05	DATA BUS BITS 00-02	
		185392	185392	185392	185392	185392	185392	185136	185136	
		00	00	00	00	08	00	01	01	
		005	004	003	002	001	000	001	000	
		5-89	5-87	5-85	5-83	5-81	5-79	5-77	5-75	
B		CONSOLE LIGHT DRIVERS: CHANNEL STATUS AND MISCELLANEOUS	CONSOLE LIGHT DRIVERS: CHANNEL STATUS AND MISCELLANEOUS	CONSOLE LIGHT DRIVERS: F UPPER	CONSOLE LIGHT DRIVERS: B8 AND F LOWER	CONSOLE LIGHT DRIVERS: MISCELLANEOUS	CONSOLE LIGHT DRIVERS: A/Q/E REGISTER	PARTIAL WRITE BITS 2-4 AND INTERRUPT CODE BITS 3,5,6	PARTIAL WRITE BITS 0 AND 1 AND INTERRUPT CODE BITS 0,1,2,4	

BLOCK CONTROL

2C0

	0	1	2 ②	② 3	4	5	6 ②	② 7	8	9
	184003	184003	185415	185415		183980	185415	185415	184003	184003
	01	01	01	01		01	01	01	01	01
	015	014	007	006		003	005	004	013	012
	6-191	6-187	6-167	6-165		6-195	6-163	6-161	6-183	6-179
A	CHANNEL 7 Ø UPPER	CHANNEL 6 Ø UPPER	CHANNEL 7 A CONTROLS	CHANNEL 6 A CONTROLS		Ø LOWER FAN-IN	CHANNEL 5 A CONTROLS	CHANNEL 4 A CONTROLS	CHANNEL 5 Ø UPPER	CHANNEL 4 Ø UPPER
	184003	184003	185437	185437	183980		185437	185437	184003	184003
	01	01	01	01	01		01	01	01	01
	007	006	007	006	002		005	004	005	004
	6-189	6-185	6-175	6-173	6-193		6-171	6-169	6-181	6-177
B	CHANNEL 7 Ø LOWER	CHANNEL 6 Ø LOWER	CHANNEL 7 C CONTROLS	CHANNEL 6 C CONTROLS	Ø UPPER FAN-IN		CHANNEL 5 C CONTROLS	CHANNEL 4 C CONTROLS	CHANNEL 5 Ø LOWER	CHANNEL 4 Ø LOWER
			①	①				①	①	

MAINTENANCE PANEL

2C1

SEE PAGE 7-1

2C2

NOTES:

① DUMMY MODULE PART NO. 186944--

② DUMMY MODULE PART NO. 186943--

③ DUMMY MODULE PART NO. 186942--

4. DUMMY MODULES REPLACE A, B, AND C CONTROL MODULES WHEN A PARTICULAR CHANNEL(S) IS NOT PRESENT.

5. JACK LOCATIONS FOR Ø UPPER AND Ø LOWER MODULES ARE EMPTY WHEN A CHANNEL IS NOT PRESENT.

⑥ THE 50-PAK PART NUMBER IS 8 DIGITS; THE LAST 2 DIGITS REPRESENT THE REVISION LEVEL OF THE 50-PAK. WHEN ORDERING A 50-PAK, USE THE 8-DIGIT PART NUMBER. EXAMPLE: 18400301

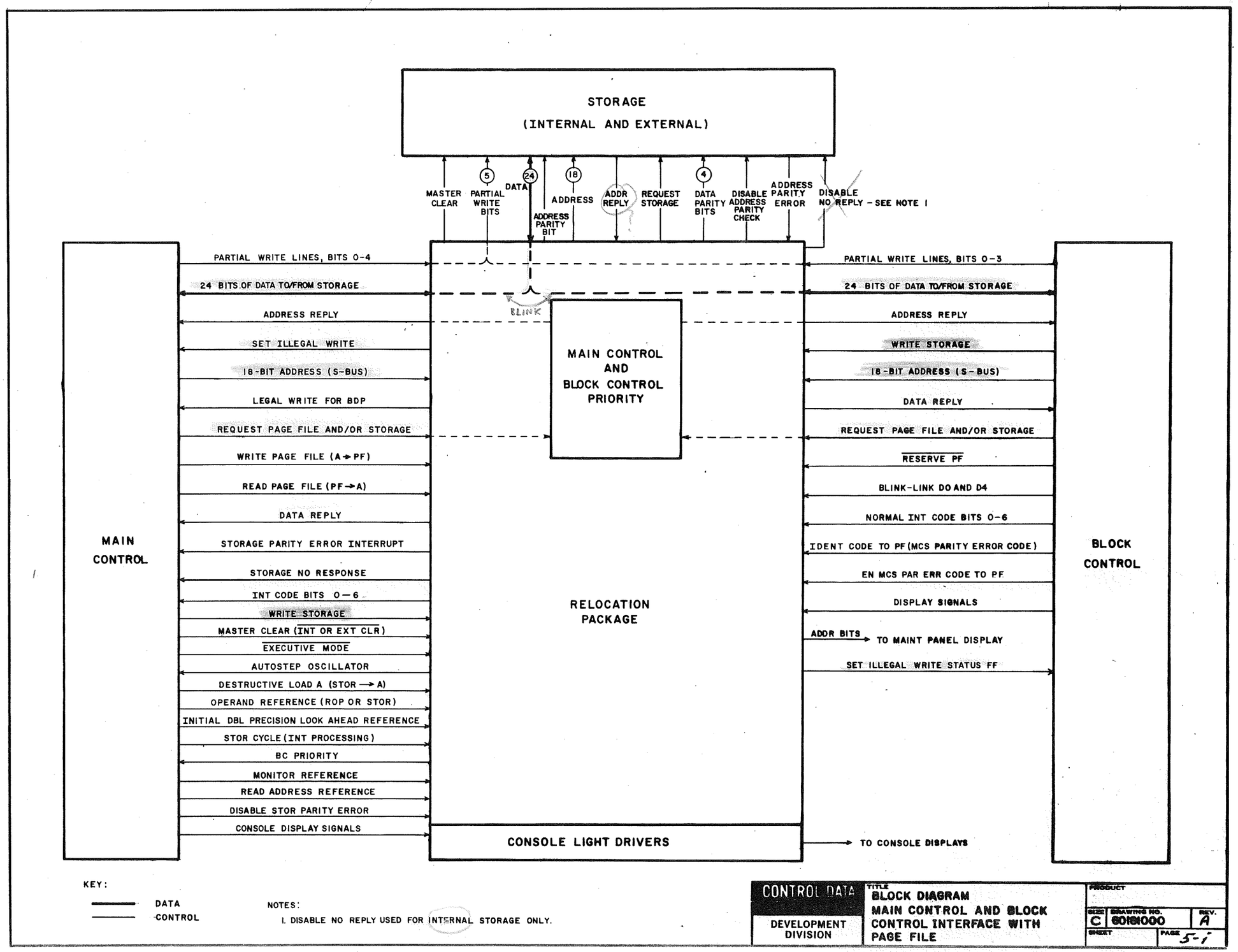
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

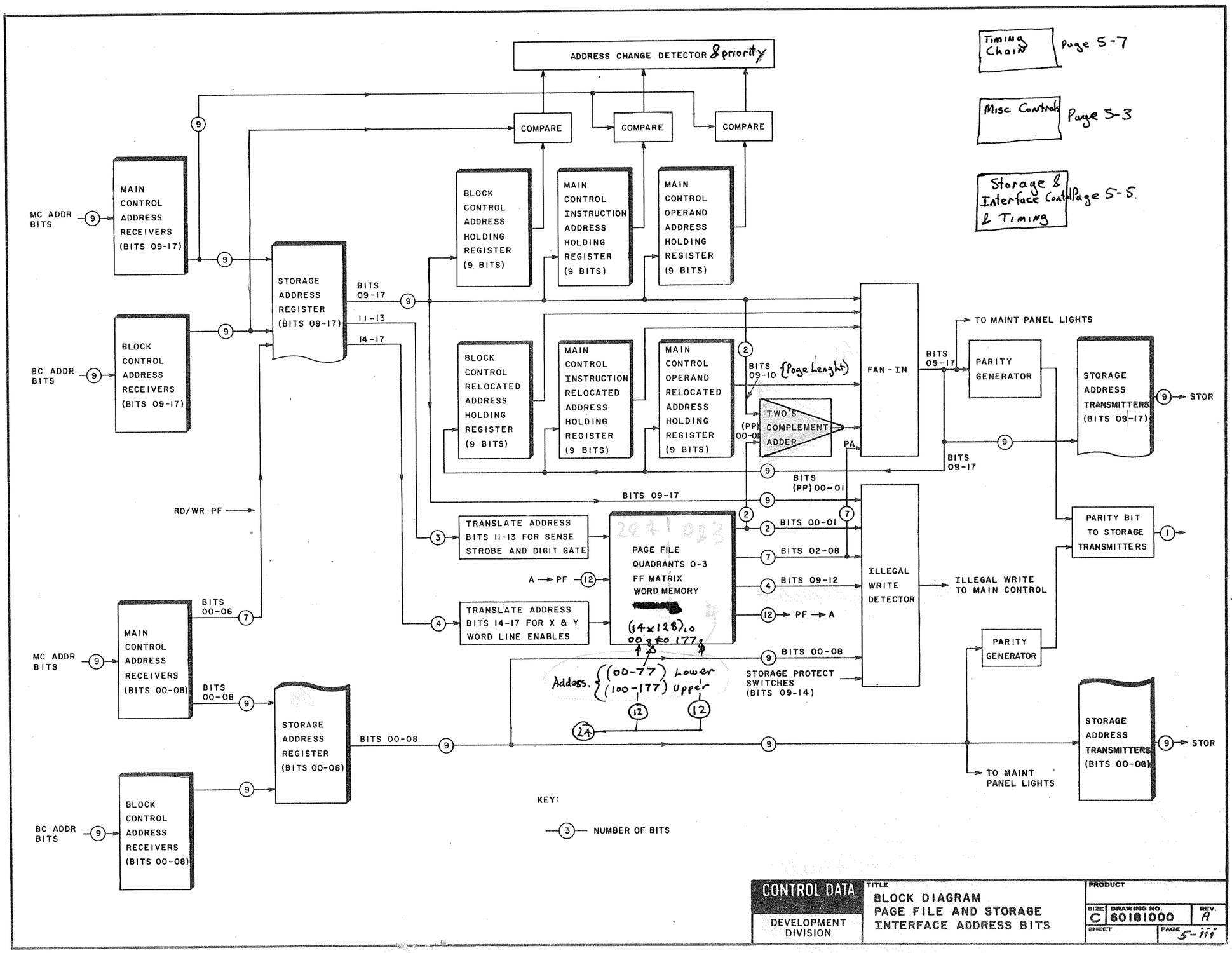
TITLE: CHASSIS MAP, UNIT 2
BLOCK CONTROL AND RELOCATION

PRODUCT

SIZE C | DRAWING NO. 60181000 | REV. Z

SHEET | PAGE 1X


STORAGE
(INTERNAL AND EXTERNAL)
MASTER CLEAR
5
PARTIAL WRITE BITS
24
DATA
ADDRESS PARITY BIT
18
ADDRESS
ADDR REPLY
REQUEST STORAGE
4
DATA PARITY BITS
DISABLE ADDRESS PARITY CHECK
ADDRESS PARITY ERROR
DISABLE NO REPLY – SEE NOTE 1
MAIN CONTROL
PARTIAL WRITE LINES, BITS 0-4
24 BITS OF DATA TO/FROM STORAGE
ADDRESS REPLY
SET ILLEGAL WRITE
18-BIT ADDRESS (S-BUS)
LEGAL WRITE FOR BDP
REQUEST PAGE FILE AND/OR STORAGE
WRITE PAGE FILE (A→PF)
READ PAGE FILE (PF→A)
DATA REPLY
STORAGE PARITY ERROR INTERRUPT
STORAGE NO RESPONSE
INT CODE BITS 0-6
WRITE STORAGE
MASTER CLEAR (INT OR EXT CLR)
EXECUTIVE MODE
AUTOSTEP OSCILLATOR
DESTRUCTIVE LOAD A (STOR → A)
OPERAND REFERENCE (ROP OR STOR)
INITIAL DBL PRECISION LOOK AHEAD REFERENCE
STOR CYCLE (INT PROCESSING)
BC PRIORITY
MONITOR REFERENCE
READ ADDRESS REFERENCE
DISABLE STOR PARITY ERROR
CONSOLE DISPLAY SIGNALS
BLINK
MAIN CONTROL AND BLOCK CONTROL PRIORITY
RELOCATION PACKAGE
CONSOLE LIGHT DRIVERS
PARTIAL WRITE LINES, BITS 0-3
24 BITS OF DATA TO/FROM STORAGE
ADDRESS REPLY
WRITE STORAGE
18-BIT ADDRESS (S-BUS)
DATA REPLY
REQUEST PAGE FILE AND/OR STORAGE
RESERVE PF
BLINK-LINK D0 AND D4
NORMAL INT CODE BITS 0-6
IDENT CODE TO PF (MCS PARITY ERROR CODE)
EN MCS PAR ERR CODE TO PF
DISPLAY SIGNALS
ADDR BITS → TO MAINT PANEL DISPLAY
SET ILLEGAL WRITE STATUS FF
TO CONSOLE DISPLAYS
BLOCK CONTROL
KEY:
DATA
CONTROL
NOTES:
1. DISABLE NO REPLY USED FOR INTERNAL STORAGE ONLY.
CONTROL DATA
DEVELOPMENT DIVISION
TITLE
BLOCK DIAGRAM
MAIN CONTROL AND BLOCK CONTROL INTERFACE WITH PAGE FILE
PRODUCT
SIZE C
DRAWING NO. 60161000
REV. A
SHEET
PAGE 5-1



CONTROL DATA DEVELOPMENT DIVISION	TITLE BLOCK DIAGRAM PAGE FILE AND STORAGE INTERFACE ADDRESS BITS	PRODUCT	
		SIZE C	DRAWING NO. 60181000
		REV. A	
		SHEET	PAGE 5-111

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A3	2A2B4*M1	5* 21		NOT MAIN CONTROL ADDR, COMPARE
B3	2A2B8*J3	5* 13		NOT MAIN CONTROL ADDR, COMPARE
C0	2A1R6*L1	6* 43		
C1	2A1B6*L0	6* 43		PC PAGE FILE REQUEST
C3	2A2R7*Q3	5* 15		NOT MAIN CONTROL ADDR, COMPARE
D0	2B1A8*L1	6* 17		

(Allows bursts of 11uS(approx) of Block control (I/O) Priority)

```
D1      2R1A8*L0   6* 17                NOT RC RESERVE TO PAGE FILE
D2      2A2B6*Q3   5* 17                NOT MAIN CONTROL ADDR. COMPARE
D3      2A2B5*Q3   5* 19                NOT MAIN CONTROL ADDR. COMPARE
E2      2A2B8*I3   5* 13                EXECUTIVE MODE
E3      2A2A5*X2   5*  3   2A2A5-BW     ADDRESS CHANGE DETECTED
F2      2A2B5*H3   5* 19                EXECUTIVE MODE
F3      2A2A5*E1   5*  3   2A2A5-AV     EXECUTIVE MODE
G0      2A2A5*L3   5*  3   2A2A6-AD     NOT STORAGE BUS REQUEST
G2      2A2B7*H3   5* 15                EXECUTIVE MODE
G3      2A2A4*I1   5*  7                EXECUTIVE MODE
H0   2A1A06J06D-07                      MC REQUEST PAGE FILE
     1A4A06P01D-07
        1R0B4*R1   2*  7
H1   2A1A06J06D-08
     1A4A06P01D-08
        1R0B4*R0   2*  7
H2   2A1A06P03F-03                      NOT  (EXECUTIVE MODE)
     1A4A06J20F-03
        1C0B0*F1   2* 45
H3   2A1A06P03F-04
     1A4A06J20F-04
        1C0B0*F0   2* 45
I0   2A1A06P03F-06
     1A4A06J20F-06
        1C0B3*H3   2* 49
I1   2A1A06P03F-05                      NOT (MASTER CLR +INTERNAL CLR)
     1A4A06J20F-05
        1C0B3*H2   2* 49
I2      2A2A7*R0   5*  5                NOT LOAD S FROM BLOCK CONTROL
I3      2A2B6*H3   5* 17                EXECUTIVE MODE
J0      2R2B9*D1   5* 75
J1      2B2B9*D0   5* 75                BLOCK CONTROL PRIORITY
J2      2A2A5*U3   5*  3   2A2A5-BP     LOAD S FROM MAIN CONTROL
J3      2A2A7*V1   5*  5                NOT LOAD S FROM MAIN CONTROL
K0      2A2A5*H3   5*  3   2A2A5-BR     MAIN CONTROL PRIORITY
K1      2A2A7*L3   5*  5                BLOCK CONTROL PRIORITY
        2A2B4*I3   5* 21
K2      2A2B6*P3   5* 17                ROP + STOR COMPARE BIT 14
K3      2A2B6*S0   5* 17   2A2A6-BG     ROP + STOR COMPARE BIT 13
L0      2A2B8*S1   5* 13                BLOCK CONTROL PRIORITY
L1      2A2B5*M0   5* 19                MAIN CONTROL PRIORITY
L2      2A2B5*S0   5* 19                ROP + STOR COMPARE BIT 15
L3      2A2B5*P3   5* 19                ROP + STOR COMPARE BIT 16
M0      2A2B6*M0   5* 17                MAIN CONTROL PRIORITY
M1      2A2A9*T0   5* 11                BLOCK CONTROL PRIORITY
M2      2A2B8*I2   5* 13                NOT BLOCK CONTROL ADDR COMP EN
M3      2A2B7*P2   5* 15                NOT BLOCK CONTROL ADDR COMP EN
N0      2A2B7*H0   5* 15                MAIN CONTROL PRIORITY
N1      2A2A8*T0   5*  9                BLOCK CONTROL PRIORITY
N2      2A2B4*J0   5* 21                NOT BLOCK CONTROL ADDR COMP EN
N3      2A2A7*R1   5*  5   2A2A6-BJ     NOT STORAGE ADDR REPLY TIME
O0      2A2B8*S0   5* 13                LOAD S REGISTER
        2A2B4*K3   5* 21
O1      2A2B5*B0   5* 19                NOT LOAD S REGISTER
O2      2A2B6*G0   5* 13                BLOCK CONTROL COMPARE BIT 10
O3      2A2B8*E0   5* 13   2A2A6-BN     BLOCK CONTROL COMPARE BIT 09
P0      2A2A8*T1   5*  9   2A2A8-AM     LOAD S REGISTER
P1      2A2B7*B0   5* 15                NOT LOAD S REGISTER
P2      2A2B6*P2   5* 17                NOT BLOCK CONTROL ADDR COMP EN
P3      2A2B7*R1   5* 15                BLOCK CONTROL COMPARE BIT 11
Q0      2A2B6*B0   5* 17                NOT LOAD S REGISTER
Q1      2A2A9*T1   5* 11   2A2A9-AM     LOAD S REGISTER
Q2      2A2B7*I2   5* 15                BLOCK CONTROL COMPARE BIT 12
Q3      2A2B5*P2   5* 19                NOT BLOCK CONTROL ADDR COMP EN
R0      2B2B9*X0   5* 75
R1      2B2B9*X1   5* 75                NOT LOAD S REG
R2      2A2B6*I2   5* 17                BLOCK CONTROL COMPARE BIT 14
R3      2A2B5*R1   5* 19                BLOCK CONTROL COMPARE BIT 15
S0      2A2A4*L0   5*  7   2A2A4-BY     PAGE FILE BUSY
S1      2A2A5*G3   5*  3   2A2A6-AU     OPERAND ADDRESS COMPARE ENABLE
S2      2A2A5*E2   5*  3   2A2A6-BP     BLOCK CONTROL ADDR COMPARE EN
S3      2A2B5*I2   5* 19                BLOCK CONTROL COMPARE BIT 16
T0   2A1A06J06D-09                      PF ADDR REPLY TO MN CONTROL
     1A4A06P01D-09
        1B0B7*S1   2* 19
T1   2A1A06J06D-10
     1A4A06P01D-10
        1B0B7*S0   2* 19
T2      2A2B8*I0   5* 13   2A2A6-BU     RNI + RADR COMPARE BIT 09
T3      2A2B6*R1   5* 17   2A2A6-BS     BLOCK CONTROL COMPARE BIT 13
U0      2A2A5*X3   5*  3   2A2A6-AW     NOT PAGE FILE TIME 5
U1      2A2A7*A3   5*  5                MASTER CLEAR PAGE FILE
U2      2A2B8*H0   5* 13                RNI + RADR COMPARE BIT 10
U3      2A2B7*S1   5* 15                RNI + RADR COMPARE BIT 11
V0      2A2B8*D0   5* 13   2A2A6-AY     ROP + STOR COMPARE BIT 09
V1      2A2B8*A0   5* 13                ROP + STOR COMPARE BIT 10
V2      2A2B6*N2   5* 17                RNI + RADR COMPARE BIT 14
V3      2A2B7*N2   5* 15                RNI + RADR COMPARE BIT 12
W0      2A2B7*P3   5* 15                ROP + STOR COMPARE BIT 12
W1      2A2B7*S0   5* 15                ROP + STOR COMPARE BIT 11
W2      2A2B5*S1   5* 19                RNI + RADR COMPARE BIT 15
W3      2A2B5*N2   5* 19                RNI + RADR COMPARE BIT 16
X0      2B1A8*J1   6* 17                PAGE FILE ADDR REPLY TO BC
X1      2R1A8*J0   6* 17
X2      2A2A5*F3   5*  3   2A2A6-BZ     INSTRUCTION  ADDR COMPARE EN
X3      2A2B6*S1   5* 17   2A2A6-BY     RNI + RADR COMPARE BIT 13

        PAGE   5*  1
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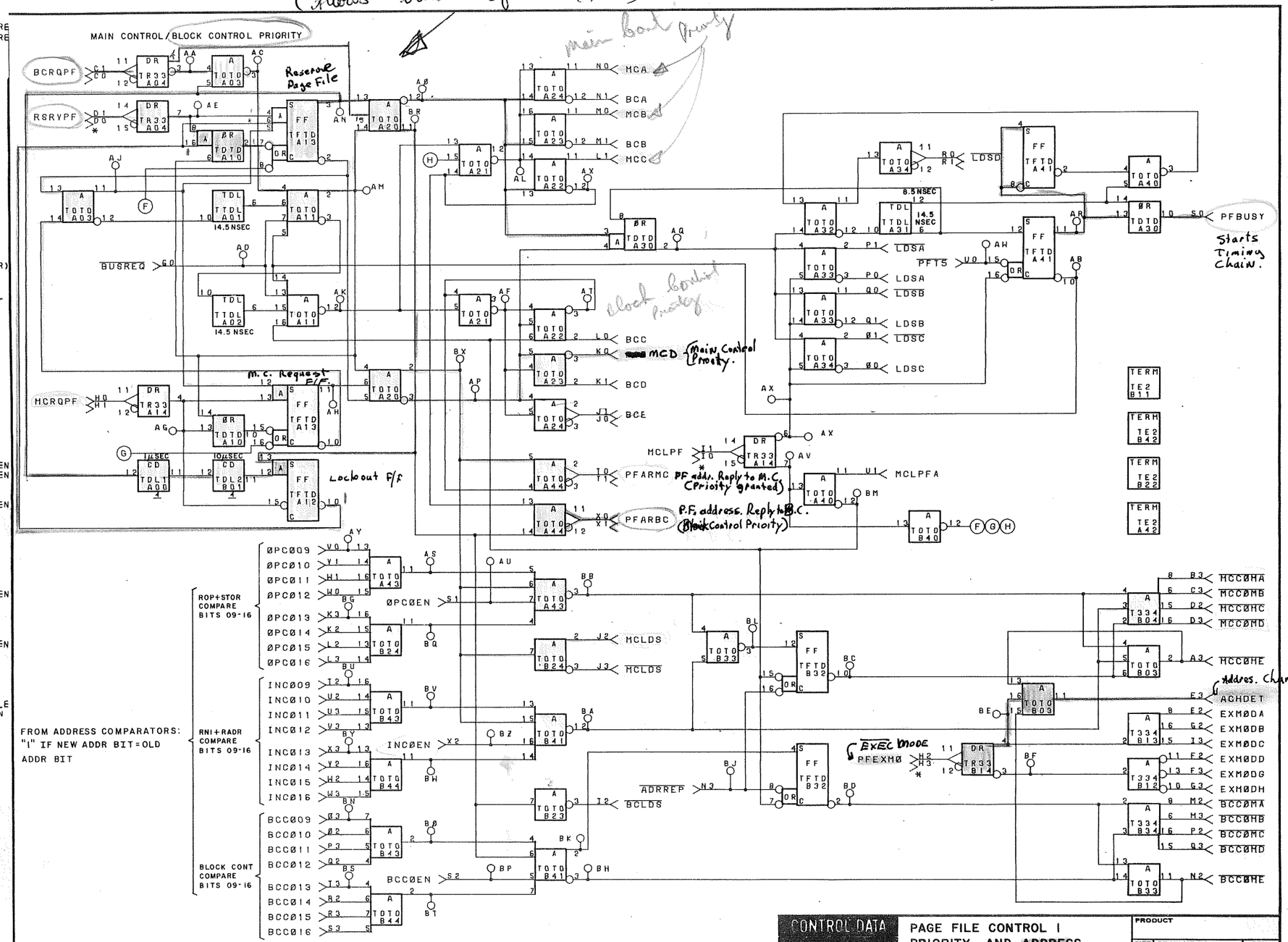
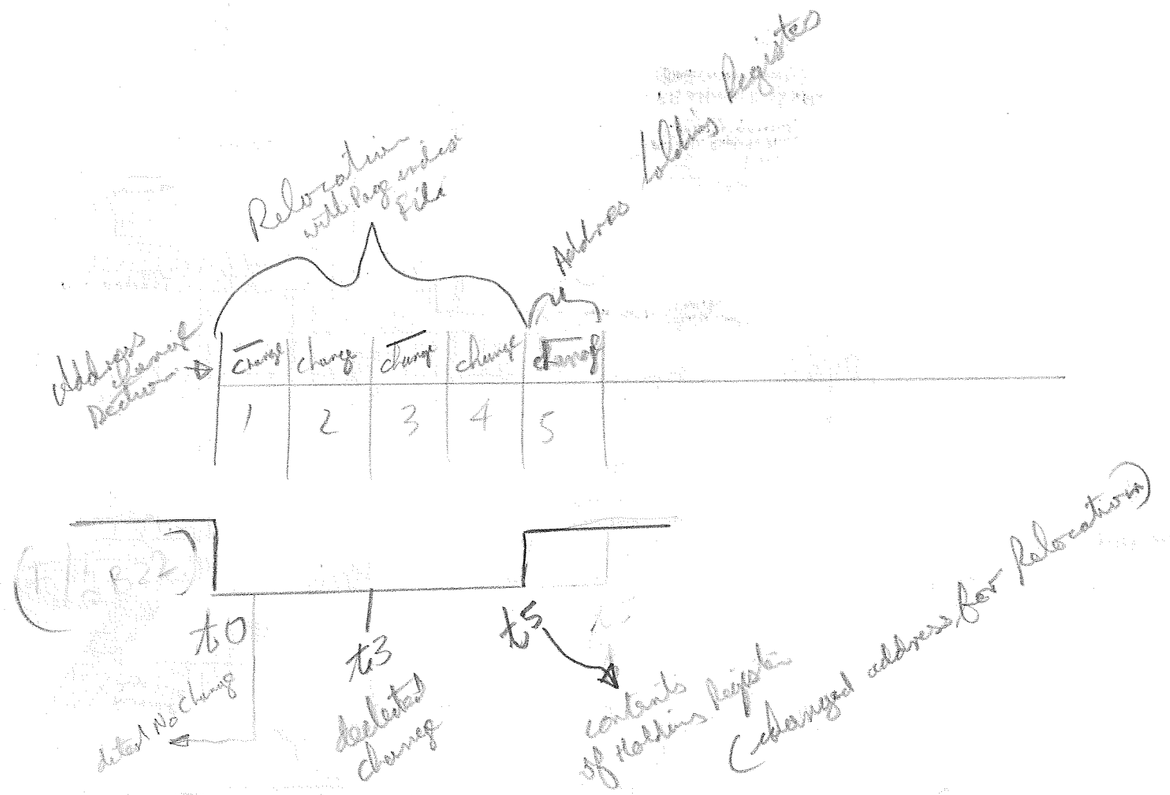


CONTROL DATA DEVELOPMENT DIVISION	PAGE FILE CONTROL I PRIORITY AND ADDRESS CHANGE COMPARE LOC:2A2A6 PART NO.185210 SER.000	PRODUCT	
		SIZE C	DRAWING NO. 60181000 REV. AA
		SHEET	PAGE 5-1

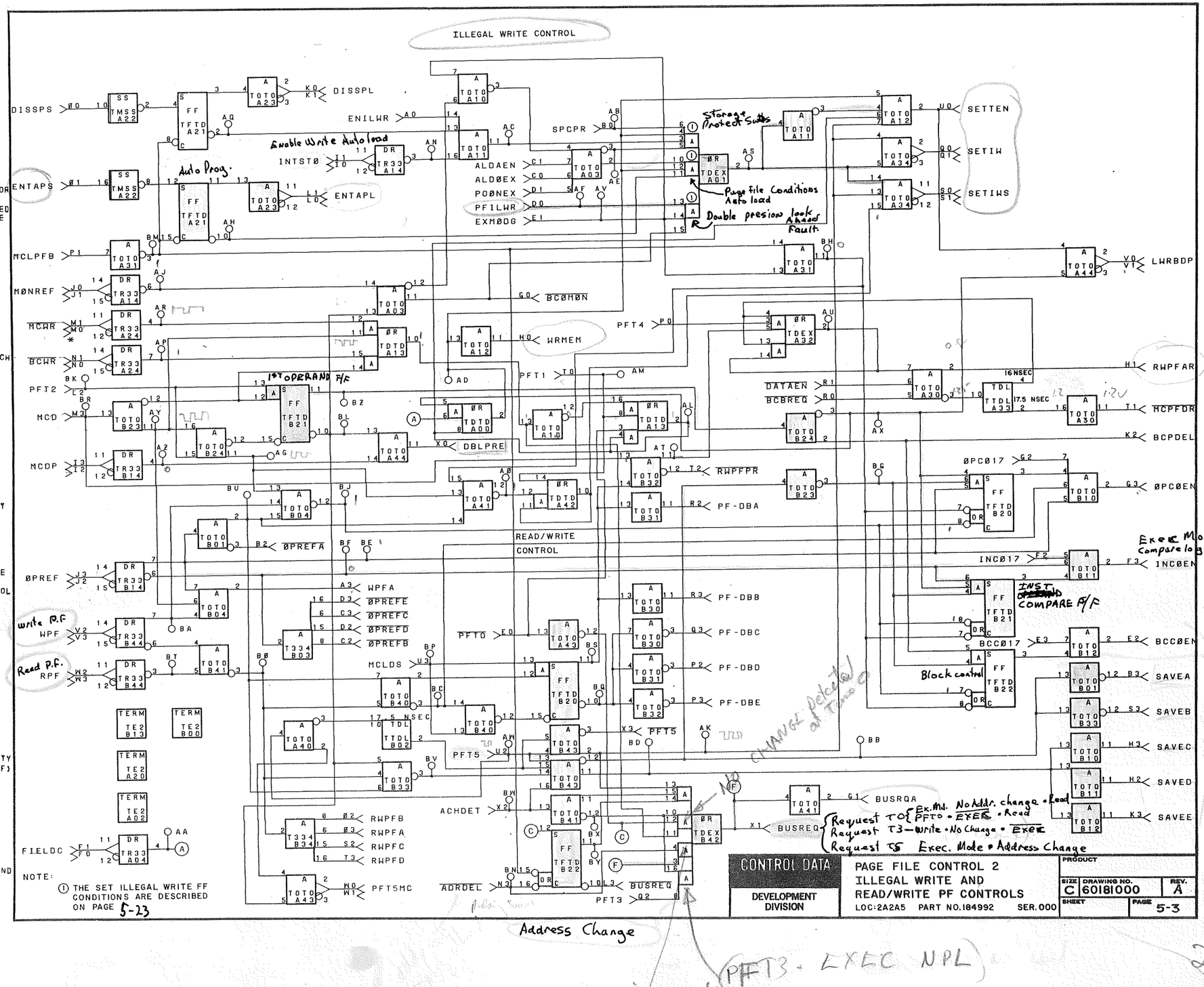
25

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A2B5-U3	5- 19		ENABLE ILLEGAL WRITE SWITCHES
A3	2A2A4-J8	5- 7	2A2A4-AJ	WRITE PAGE FILE
B0	2A2B9-M3	5- 23	2A2A5-AB	STOR PROTECT COMP TO ILL. WR
B2	2A2B7-V1	5- 15		NOT OPERAND REFERENCE
B3	2A2B8-Q8	5- 13		SAVE NEW (S) REG UNTIL CHANGE
C0	2A2B6-T8	5- 17		AUTO LOAD/AUTO DUMP ADDRESS OR EXECUTIVE MODE
C1	2A2B4-M8	5- 21		AUTO LOAD/AUTO DUMP ADDR. EN.
C2	2A2B6-V1	5- 17		NOT OPERAND REFERENCE
C3	2A2B5-V1	5- 19		NOT OPERAND REFERENCE
D0	2A2B4-A8	5- 21	2A2A5-AF	PAGE FILE ILLEGAL WRITE SENSED
D1	2A2B7-U3	5- 15		PAGE 0 OR NOT EXECUTIVE MODE
D2	2A2B4-L3	5- 21		NOT OPERAND REFERENCE
D3	2A2B8-V1	5- 13		NOT OPERAND REFERENCE
E0	2A2A4-M3	5- 7		NOT PAGE FILE TIME 0
E1	2A2A6-F3	5- 1	2A2A5-AV	EXECUTIVE MODE
E2	2A2A6-S2	5- 1	2A2A6-BP	BLOCK CONTROL ADDR COMPARE EN
E3	2A2B4-D2	5- 21		BLOCK CONTROL COMPARE BIT 17
F0	2A1A06J06E-06 1A4A06P01E-06			
	1A2A1-B2	4- 11		
F1	2A1A06J06E-05 1A4A06P01F-05			READ C OPERAND REQUEST(EDIT+67(0&1))
	1A2A1-B3	4- 11		
F2	2A2B4-D3	5- 21		RNI + RADR COMPARE BIT 17
F3	2A2A6-X2	5- 1	2A2A6-BZ	INSTRUCTION ADDR COMPARE EN
G0	2A2B5-T2	5- 19		NOT BLOCK CONTROL OR MON STATE
G1	2A2B9-U8	5- 23		BUS REQUEST
G2	2A2B4-C3	5- 21		ROP + STOR COMPARE BIT 17
G3	2A2A6-S1	5- 1	2A2A6-AU	OPERAND ADDRESS COMPARE ENABLE
H0	2A2B4-P8	5- 21		WRITE INTO STORAGE
H1	2A2B9-V1	5- 23	2A2B9-AV	RD/WR PAGE FILE ADDR REPLY
H2	2A2B5-01	5- 19		SAVE NEW (S) REG UNTIL CHANGE
H3	2A2B6-01	5- 17		SAVE NEW (S) REG UNTIL CHANGE
I0	2A1A06P03B-06 1A4A06J20B-06			
	1C0A0-L1	2- 37		
I1	2A1A06P03B-05 1A4A06J20B-05			STORE CYCLE,INT. PROCESSING



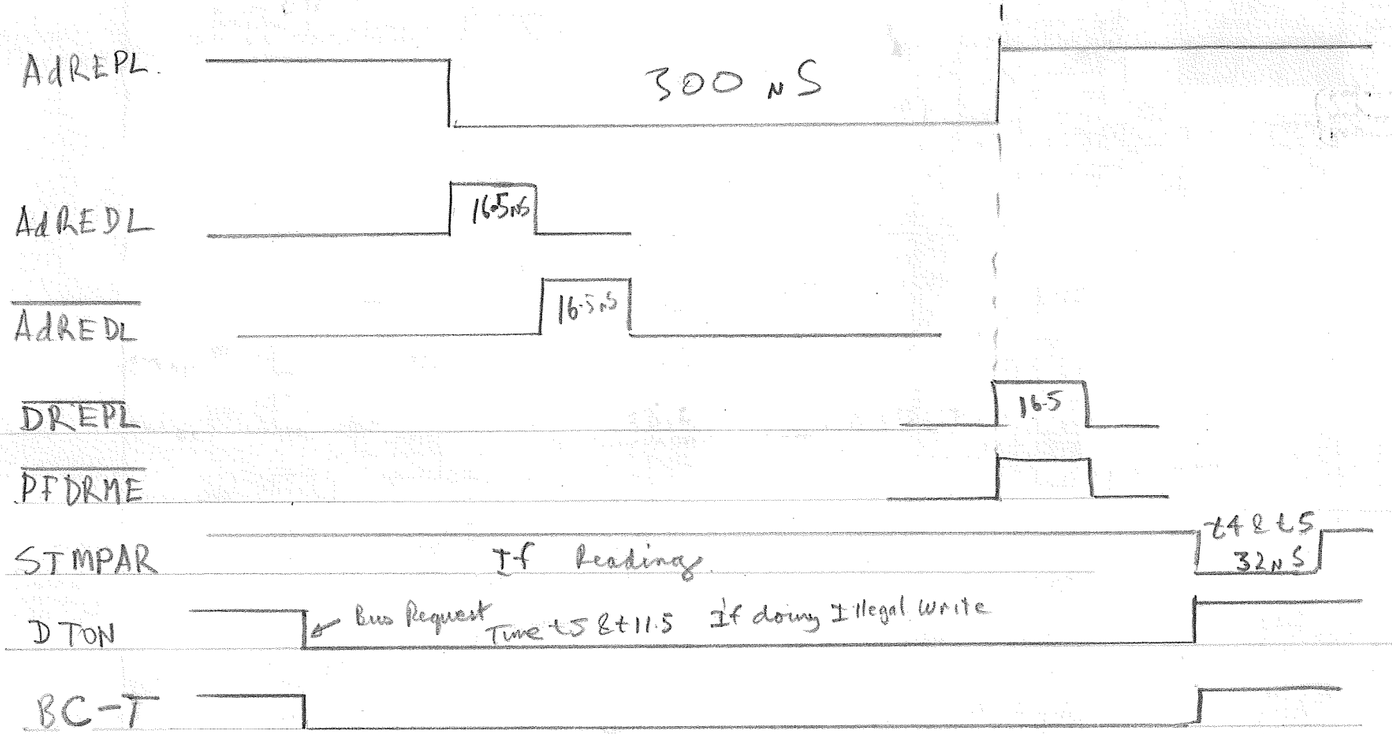
```
        1C0A0=L0   2= 37
I2  2A1A06J06D-06
    1A4A06P01D-06
        1B0A8=T2   2= 13
I3  2A1A06J06D-05                          (FIRST OPERAND)(DP INST.)
    1A4A06P01D-05
        1B0A8=T3   2= 13
J0  2A1A06P03A-07                          MONITOR STATE
    1A4A06J20A-07
        1C0A0=Q0   2= 37
J1  2A1A06P03A-08
    1A4A06J20A-08
        1C0A0=Q1   2= 37
J2  2A1A06P05D-04
    1A4A06J14D-04
        1B0B5=U3   2=  5                   OPERAND REFERENCE
J3  2A1A06P05D-03
    1A4A06J14D-03
        1B0B5=U2   2=  5
K0      2B2B6=W1   5= 81                   DISABLE STOR PROTECT INDICATOR
K1      2B2B6=W0   5= 81
K2      2A2A7=Q0   5=  5                   BLOCK CONTROL PRIORITY DELAYED
K3      2A2B4=J3   5= 21                   SAVE NEW (S) REG UNTIL CHANGE
L0      2B2R6=C2   5= 81
L1      2B2B6=C3   5= 81                   ENTER AUTO PROGRAM INDICATOR
L2      2A2A4=X3   5=  7  2A2A5=RK         PAGE FILE TIME 2
L3      2A2A6=G0   5=  1  2A2A6=AD         NOT STORAGE BUS REQUEST
M0  2A1A06P03A-09                          MAIN CONT WRITE SIGNAL TO PF
    1A4A06J20A-09
        1C0A0=I1   2= 37
M1  2A1A06P03A-10
    1A4A06J20A-10
        1C0A0=I0   2= 37
M3      2A2A6=K0   5=  1  2A2A5=RR         MAIN CONTROL PRIORITY
N0      2B1A7=C3   6=  1                   NOT RC MCS WRITE TO PF
N1      2B1A7=C2   6=  1
N3      2A2A7=T2   5=  5  2A2A5=RN         NOT STOR ADDR REPLY DELAYED
Q0  2A1A06J16D-01                          DISABLE STORAGE PROTECT SWITCH
Q1  2A1A06J16D-03                          ENTER AUTO PROGRAM SWITCH
Q2      2A2B6=A0   5= 17                   READ/WRITE PAGE FILE
Q3      2A2B7=A0   5= 15                   READ/WRITE PAGE FILE
P0      2A2A4=R3   5=  7                   PAGE FILE TIME 4
P1      2A2A7=B3   5=  5                   MASTER CLEAR PAGE FILE
P2      2A2B5=N3   5= 19                   ENABLE PAGE FILE TO DATA BUS
P3      2A2R4=U0   5= 21                   ENABLE PAGE FILE TO DATA BUS
Q0  2A1A06P03A-01                          SET ILLEGAL WRITE
    1A4A06J20A-01
        1C0A1=X3   2= 43
Q1  2A1A06P03A-02
    1A4A06J20A-02
        1C0A1=X2   2= 43
Q2      2A2A4=F1   5=  7                   PAGE FILE TIME 3
Q3      2A2B6=N3   5= 17                   ENABLE PAGE FILE TO DATA BUS
R0      2A2A7=T3   5=  5                   NOT BLOCK CONTROL BUS REQUEST
R1      2A2A7=V0   5=  5                   NOT STORAGE DATA ENABLE ON
R2      2A2B6=L2   5= 13                   ENABLE PAGE FILE TO DATA BUS
R3      2A2B7=N3   5= 15                   ENABLE PAGE FILE TO DATA BUS
S0      2B0R7=03   6=113                   SET ILLEGAL WRITE STATUS FF
S1      2B0B7=02   6=113
S2      2A2B5=A0   5= 19                   READ/WRITE PAGE FILE
S3      2A2R7=01   5= 15                   SAVE NEW (S) REG UNTIL CHANGE
T0      2A2A4=K0   5=  7  2A2A5=AM         PAGE FILE TIME 1
T1      2A2A7=W2   5=  5  2A2A7=RZ         NOT DATA REPLY TO MAIN CONTROL
T2      2A2A7=B1   5=  5                   NOT RD/WR PAGE FILE PRIORITY
T3      2A2B4=P3   5= 21                   READ/WRITE PAGE FILE
U0      2A2A7=H0   5=  5                   SET TRANSMITTER ENABLE
U2      2A2A4=Q3   5=  7                   PAGE FILE TIME 5
U3      2A2A6=J2   5=  1  2A2A5=RP         LOAD S FROM MAIN CONTROL
V0  2A1A06J06E-03                          LEGAL WRITE FOR RDP
    1A4A06P01E-03
        1A2A1=L0   4= 11
V1  2A1A06J06E-04
    1A4A06P01E-04
        1A2A1=L1   4= 11
V2  2A1A06P03R-01                          WRITE PF
    1A4A06J20R-01
        1C0A0=01   2= 37
V3  2A1A06P03R-02
    1A4A06J20R-02
        1C0A0=00   2= 37
W0  2A1A06J06E-09                          (PF TIME 5)(MAIN CONT PRIORITY
    1A4A06P01E-09                                                  IN PF)
        1B0B7=X0   2= 19
W1  2A1A06J06E-10
    1A4A06P01F-10
        1B0B7=X1   2= 19
W2  2A1A06P03R-03                          READ PF
    1A4A06J20R-03
        1C0A0=H1   2= 37
W3  2A1A06P03R-04
    1A4A06J20R-04
        1C0A0=M0   2= 37
X0      2A2R4=K1   5= 21                   DOUBLE PRECISION FIRST OPERAND
X1      2A2A7=B0   5=  5                   STORAGE BUS REQUEST
X2      2A2A6=E3   5=  1  2A2A5=RW         ADDRESS CHANGE DETECTED
X3      2A2A6=U0   5=  1  2A2A6=AW         NOT PAGE FILE TIME 5

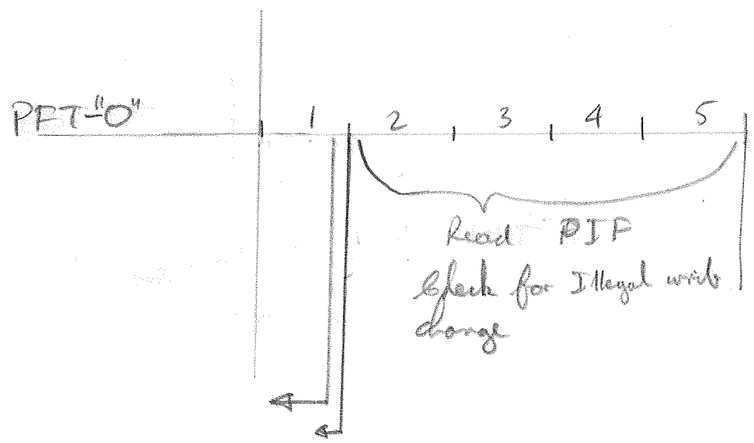
      PAGE   5= 3
```



See Page 5-2 also

→ Data blain 82.5 nS.

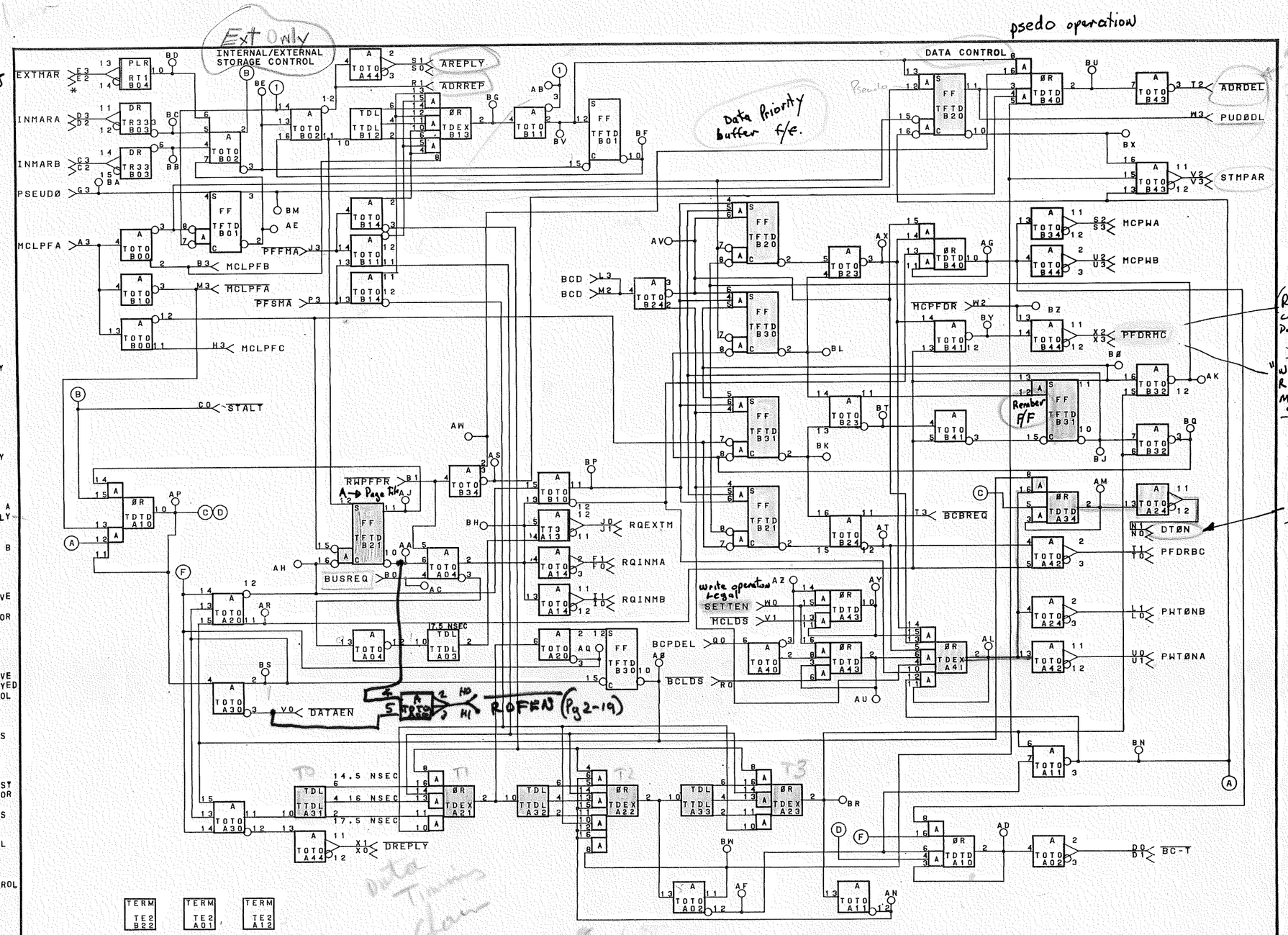




{Start Timing Chain} From Storage

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A3	2A2A6*U1	5* 1		MASTER CLEAR PAGE FILE
B0	2A2A5*X1	5* 3		STORAGE BUS REQUEST
B1	2A2A5*T2	5* 3		NOT RD/WR PAGE FILE PRIORITY
B3	2A2A5*P1	5* 3		MASTER CLEAR PAGE FILE
C0	2A2B9*W3	5* 23		NOT STOR ADDR REPL
C2	2A1A06J05E*10			
C3	2A1A06J05E*09			ADDR REPLY FROM INT STOR B
D0	2B2A5*U3	5* 73		
D1	2B2A5*U2	5* 73		NOT BC DATA XMIT ENABLE
D2	2A1A06J03E*10			
D3	2A1A06J03E*09			ADDR REPLY FROM INT STOR A
E2	2A1A06J07E*09			EXTERNAL STORAGE ADDR. REPLY
	2A1A06J08E*09			
E3	2A1A06J07E*10			
	2A1A06J08E*10			
F0	2A1A06J03E*08			
F1	2A1A06J03E*07			REQUEST TO INTERNAL STORAGE A
G3	2A2B9*V0	5* 23	2A2A7*RA	INITIATE PSEUDO STORAGE REPLY
H3	2A2B9*G1	5* 23		MASTER CLEAR PAGE FILE
I0	2A1A06J05E*08			
I1	2A1A06J05E*07			REQUEST TO INTERNAL STORAGE B
J0	2A1A06J07E*07			REQUEST TO EXTERNAL STORAGE
	2A1A06J08E*07			
J1	2A1A06J07E*08			
	2A1A06J08E*08			
J3	2A2A4*K3	5* 7		NOT PAGE FILE FAST MODE SLAVE
L0	2B2B8*R3	5* 77		
L1	2B2B8*R2	5* 77		EN PARTIAL WRITE BITS TO STOR
L3	2A2A6*K1	5* 1		BLOCK CONTROL PRIORITY
M2	2A2B4*I3	5* 21		BLOCK CONTROL PRIORITY
M3	2A2A4*L1	5* 7		NOT MASTER CLEAR PAGE FILE
N0	2B2A5*R1	5* 73		
N1	2B2A5*R0	5* 73		DATA TRANSMITTERS ON
P3	2A2A4*L3	5* 7		NOT PAGE FILE SLOW MODE SLAVE
Q0	2A2A5*K2	5* 3		BLOCK CONTROL PRIORITY DELAYED
R0	2A2A6*I2	5* 1		NOT LOAD S FROM BLOCK CONTROL
R1	2A2A6*N3	5* 1	2A2A6*BJ	NOT STORAGE ADDR REPLY TIME
S0	2B2B9*G0	5* 75		NOT STOR ADDR REPLY TIME
S1	2B2B9*G1	5* 75		
S2	2B2B9*S3	5* 75		SELECT MAIN CONT PAR WR BITS
S3	2B2B9*S2	5* 75		
T0	2B1B7*F3	6* 3		
T1	2B1B7*F2	6* 3		DATA REPLY TO BLOCK CONTROL
T2	2A2A5*N3	5* 3	2A2A5*BN	NOT STOR ADDR REPLY DELAYED
T3	2A2A5*R0	5* 3		NOT BLOCK CONTROL BUS REQUEST
U0	2B2B9*R2	5* 75		EN PARTIAL WRITE BITS TO STOR
U1	2B2B9*R3	5* 75		
U2	2B2B8*S3	5* 77		SELECT MAIN CONT PAR WR BITS
U3	2B2B8*S2	5* 77		
V0	2A2A5*R1	5* 3		NOT STORAGE DATA ENABLE ON
V1	2A2A6*J3	5* 1		NOT LOAD S FROM MAIN CONTROL
V2	2B2A5*X0	5* 73		STROBE STORAGE PARITY CHECK
V3	2B2A5*X1	5* 73		
W0	2A2A5*U0	5* 3		SET TRANSMITTER ENABLE
W2	2A2A5*T1	5* 3	2A2A7*RZ	NOT DATA REPLY TO MAIN CONTROL
W3	2A2B9*R0	5* 23	2A2B9*AP	PSEUDO REPLY DELAYED
X0	2B2B8*X1	5* 77		NOT STORAGE DATA REPLY TIME
X1	2B2B8*X0	5* 77		
X2	2A1A06J06E*02			
	1A4A06P01E*02			
	1B0B7*W2	2* 19		
X3	2A1A06J06E*01			NOT DATA REPLY TO MAIN CONTROL
	1A4A06P01E*01			
	1R0B7*W3	2* 19		

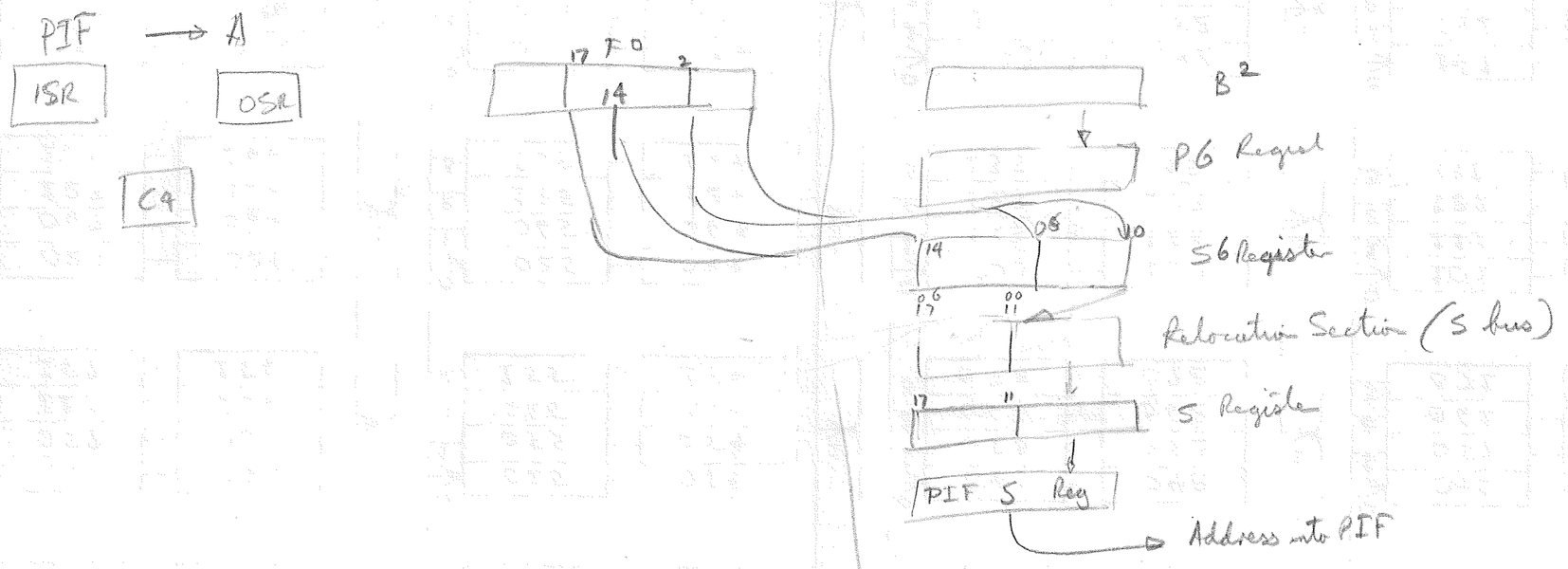
PAGE 5* 5



NOTES:

1. ALL TTDL DELAYS HAVE SAME DELAY TIMES ON RESPECTIVE PINS.

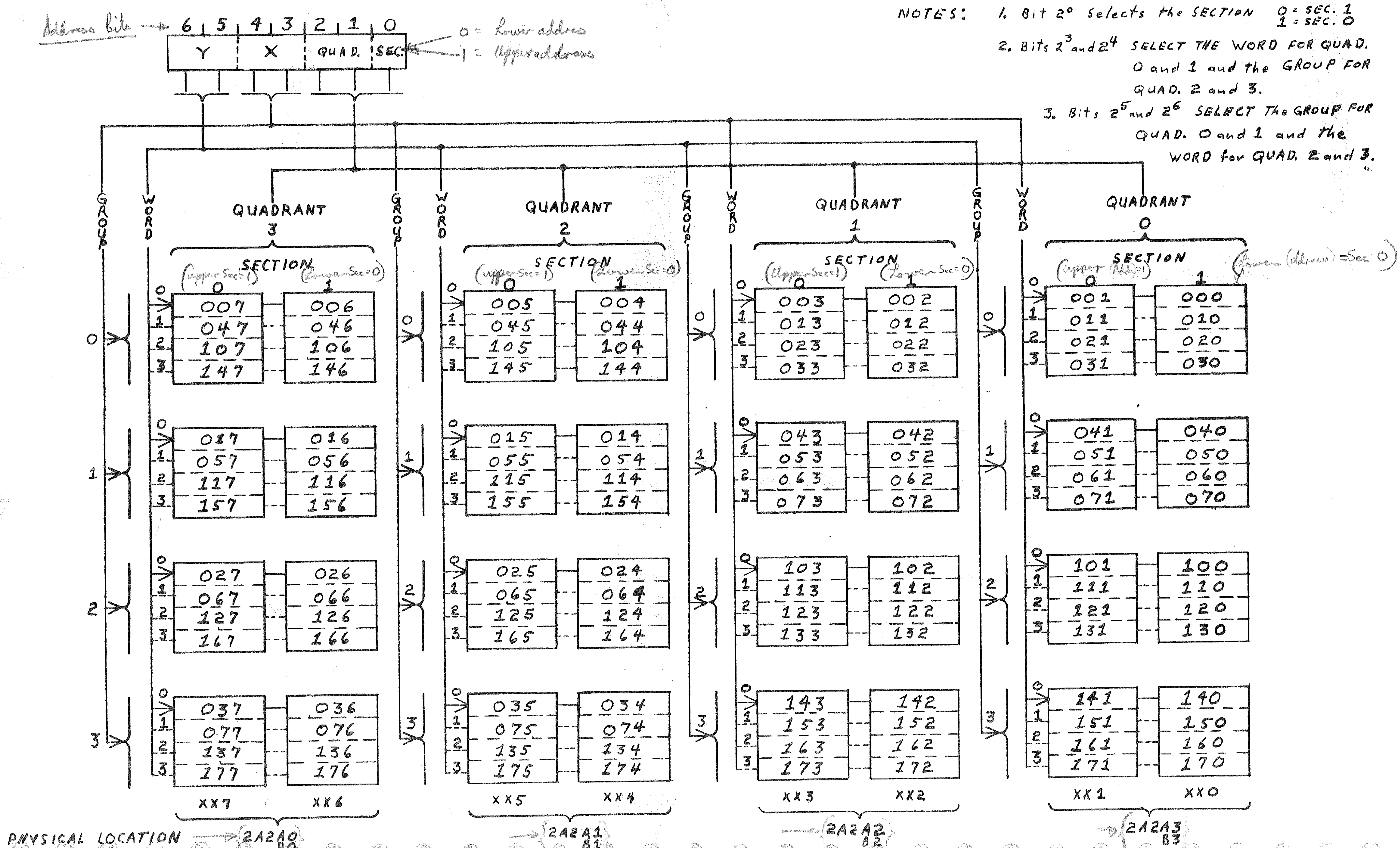
CONTROL DATA DEVELOPMENT DIVISION	PAGE FILE CONTROL 3 STORAGE AND DATA CONTROL DATA TIMING CHAIN. LOC:2A2A7 PART NO.184875 SER.000	PRODUCT	
		SIZE C	DRAWING NO. 60181000 REV. A
		SHEET	PAGE 5-5


PIF → A
ISR
OSR
C9
17 15 0
2
14
B 2
PG Reqst
14
08
00
S6 Registe
06
17
00
11
Relocation Section (S bus)
17
11
S Registe
PIF S Reg
Address into PIF

PAGE INDEX FILE ADDRESSING SCHEME

NOTES:

1. Bit 2^0 selects the SECTION 0 = SEC. 1, 1 = SEC. 0
2. Bits 2^3 and 2^4 SELECT THE WORD FOR QUAD. 0 and 1 and the GROUP FOR QUAD. 2 and 3.
3. Bits 2^5 and 2^6 SELECT The GROUP FOR QUAD. 0 and 1 and the WORD for QUAD. 2 and 3.



(write 063)

6	5	4	3	2	1	0
X	X	Quad			Seeting	
0	1	1	0	0	1	1

3X21Y2
3Y11X1
1S21S3
1D31D0

TRANSLATION MIS LEADING

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A2A0=D1	5= 49		QUADRANT 3 Y=1, QUADRANT 1 X=1
	2A2A2=C1	5= 37		
A3	2A2A2=G0	5= 37		QUADRANT 3 X=3, QUADRANT 1 Y=3
	2A2A0=K1	5= 49		
B0	2A2A1=I1	5= 43		QUADRANT 2 Y=2, QUADRANT 0 X=2
	2A2A3=K0	5= 31		
B3	2A2A2=D1	5= 37		QUADRANT 3 X=1, QUADRANT 1 Y=1
	2A2A0=C1	5= 49		
C0	2A2A0=G1	5= 49		QUADRANT 3 Y=0, QUADRANT 1 X=0
	2A2A2=B1	5= 37		
C3	2A2A3=F1	5= 31		QUADRANT 2 X=0, QUADRANT 0 Y=0
	2A2A1=B1	5= 43		
D0	2A2A1=D1	5= 43		QUADRANT 2 Y=1, QUADRANT 0 X=1
	2A2A3=C1	5= 31		
D3	2A2A2=G1	5= 37		QUADRANT 3 X=0, QUADRANT 1 Y=0
	2A2A0=B1	5= 49		
E0	2A2B4=D1	5= 21		NOT PAGE FILE ADDRESS BIT 06
E3	2A2R6=H2	5= 17		NOT PAGE FILE ADDRESS BIT 03
F0	2A2A1=G1	5= 43		QUADRANT 2 Y=0, QUADRANT 0 X=0
	2A2A3=B1	5= 31		
F1	2A2A5=Q2	5= 3		PAGE FILE TIME 3
F3	2A2A3=D1	5= 31		QUADRANT 2 X=1, QUADRANT 0 Y=1
	2A2A1=C1	5= 43		
G0	2A2B5=H2	5= 19		NOT PAGE FILE ADDRESS BIT 05
G3	2A2B5=E0	5= 19		NOT PAGE FILE ADDRESS BIT 04
H0	2A2A0=I1	5= 49		QUADRANT 3 Y=2, QUADRANT 1 X=2
	2A2A2=K0	5= 37		
H1	2A2A0=G0	5= 49		QUADRANT 3 Y=3, QUADRANT 1 X=3
	2A2A2=K1	5= 37		
H3	2A2A3=G0	5= 31		QUADRANT 2 X=3, QUADRANT 0 Y=3
	2A2A1=K1	5= 43		
I0	2A2A1=G0	5= 43		QUADRANT 2 Y=3, QUADRANT 0 X=3
	2A2A3=K1	5= 31		
I1	2A2A6=G3	5= 1		EXECUTIVE MODE
I3	2A2A2=I1	5= 37		QUADRANT 3 X=2, QUADRANT 1 Y=2
	2A2A0=K0	5= 49		
J0	2A2A5=A3	5= 3	2A2A4-AJ	WRITE PAGE FILE
J1	2A2B6=E0	5= 17		NOT PAGE FILE ADDRESS BIT 02
J3	2A2A3=I1	5= 31		QUADRANT 2 X=2, QUADRANT 0 Y=2
	2A2A1=K0	5= 43		
K0	2A2A5=T0	5= 3	2A2A5-AM	PAGE FILE TIME 1
K1	2A2B2=C1	5= 37		QUADRANT 1 DIGIT GATE 3 AND
	2A2B2=F0	5= 39		QUADRANT 1 DIGIT GATE 0
K3	2A2A7=J3	5= 5		NOT PAGE FILE FAST MODE SLAVE
L0	2A2A6=S0	5= 1	2A2A4-RY	PAGE FILE BUSY
L1	2A2A7=M3	5= 5		NOT MASTER CLEAR PAGE FILE
L3	2A2A7=P3	5= 5		NOT PAGE FILE SLOW MODE SLAVE
M0	2A2B7=E0	5= 15		NOT PAGE FILE ADDRESS BIT 00
M1	2A2B3=D1	5= 33		QUADRANT 0 DIGIT GATE 1 AND
	2A2B0=F1	5= 49		QUADRANT 3 DIGIT GATE 2
M3	2A2A5=E0	5= 3		NOT PAGE FILE TIME 0
N0	2A2B3=C1	5= 31		QUADRANT 0 DIGIT GATE 3 AND
	2A2B3=F0	5= 33		QUADRANT 0 DIGIT GATE 0
N1	2A2R0=C1	5= 49		QUADRANT 3 DIGIT GATE 3 AND
	2A2R0=F0	5= 51		QUADRANT 3 DIGIT GATE 0
N3	2A2A04J03F=03			NOT PAGE FILE SLOW MODE
O0	2A2B7=H2	5= 15		NOT PAGE FILE ADDRESS BIT 01
P0	2A2B2=D0	5= 39		QUADRANT 1 DIGIT GATE 1 AND
	2A2B3=F1	5= 31		QUADRANT 0 DIGIT GATE 2
P3	2A2A04J03E=03			NOT PAGE FILE FAST MODE
Q0	2A2B1=D0	5= 45		QUADRANT 2 DIGIT GATE 1 AND
	2A2B2=F1	5= 37		QUADRANT 1 DIGIT GATE 2
Q3	2A2A5=U2	5= 3		PAGE FILE TIME 5
R0	2A2B1=C1	5= 43		QUADRANT 2 DIGIT GATE 3 AND
	2A2B1=F0	5= 45		QUADRANT 2 DIGIT GATE 0
R3	2A2A5=P0	5= 3		PAGE FILE TIME 4
S0	2A2B0=D0	5= 51		QUADRANT 3 DIGIT GATE 1 AND
	2A2B1=F1	5= 43		QUADRANT 2 DIGIT GATE 2
T0	2A2R2=I1	5= 39		QUADRANT 1 SENSE GATE 0 AND
	2A2R2=J0	5= 37		QUADRANT 1 SENSE GATE 1
U0	2A2B3=G1	5= 33		QUADRANT 0 SENSE GATE 2 AND
	2A2B3=J1	5= 31		QUADRANT 0 SENSE GATE 3
V0	2A2B3=I1	5= 33		QUADRANT 0 SENSE GATE 0 AND
	2A2B3=J0	5= 31		QUADRANT 0 SENSE GATE 1
V1	2A2B2=G1	5= 39		QUADRANT 1 SENSE GATE 2 AND
	2A2B2=J1	5= 37		QUADRANT 1 SENSE GATE 3
W0	2A2R1=G1	5= 45		QUADRANT 2 SENSE GATE 2 AND
	2A2R1=J1	5= 43		QUADRANT 2 SENSE GATE 3
W1	2A2B0=I1	5= 51		QUADRANT 3 SENSE GATE 0 AND
	2A2R0=J0	5= 49		QUADRANT 3 SENSE GATE 1
X0	2A2R0=G1	5= 51		QUADRANT 3 SENSE GATE 2 AND
	2A2R0=J1	5= 49		QUADRANT 3 SENSE GATE 3
X1	2A2R1=I1	5= 45		QUADRANT 2 SENSE GATE 0 AND
	2A2R1=J0	5= 43		QUADRANT 2 SENSE GATE 1
X3	2A2A5=L2	5= 3	2A2A5-BK	PAGE FILE TIME 2

PAGE 5= 7

NOT Bits.

Octal Translations

OUT

PFS00 M0
PFS01 B0
PFS02 J1
HPFA J0
AJ

DIGIT SELECT TRANSLATIONS
SENSE SELECT TRANSLATIONS
X/Y TRANSLATIONS
Y/X TRANSLATIONS
look Ahead bit control.

M1 0D13D2 (xx0)
N0 0D30D0 (xx1)
P0 1D10D2 (xx2)
K1 1D31D0 (xx3)
Q0 2D11D2 (xx4)
R0 2D32D0 (xx5)
S0 3D12D2 (xx6)
N1 3D33D0 (xx7)
V0 0S00S1 (xx0)
U0 0S20S3 (xx1)
T0 1S01S1 (xx2)
V1 1S21S3 (xx3)
X1 2S02S1 (xx4)
W0 2S22S3 (xx5)
W1 3S03S1 (xx6)
X0 3S23S3 (xx7)

PFS05 G0 — 2C3 2X00Y0, 2X01Y0, 2X10Y1, 2X11Y1, 2X20Y2, 3X21Y2, 2X30Y3, 3X31Y3
PFS06 E0 — F3 2X10Y1
PFS03 E3
PFS04 G3

2Y00X0 (FO/56)
3Y01X0 (CO/56)
2Y10X1 (DO/56)
3Y11X1 (AO/56) GRN
2Y20X2 (BO/56)
3Y21X2 (HO/56) GRD
2Y30X3 (IO/56)
3Y31X3 (H1/56)

TERM TE2 B21
TERM TE2 A10

MCLPFA L1
EXMØDH T1
PFBUSY BY L0
PFFM P3 (FAST)
PFSM N3 (SLOW)

WRITE PF FF TFTD A23
TIMING CHAIN
PFT1 K0 — PFT2 X3 — PFT3 F1 — PFT4 R3 — PFT5 Q3
PFTO M3
PFFMA K3
PFSMA L3

CONTROL DATA
DEVELOPMENT DIVISION

PAGE FILE ADDRESS DECODING AND TIMING CHAIN

LOC:2A2A4 PART NO. 184699 SER.000

PRODUCT
SIZE C | DRAWING NO. 60181000 | REV.
SHEET | PAGE 5-7

Time chain 825 NS long

33

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A2A9-H0	5- 11		NOT STOR ADDR BIT 07 TO PAR, GENERATOR AND IND DRIVER
A3	2A2A8-I3	5- 9		NOT STOR ADDR BIT 02 TO PAR, GENERATOR AND IND DRIVER

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B0   2A2A04J01H-01
B1   2A2A04J01H-02
B2   2A2A04J01C-01
B3   2A2A04J01C-02
C0        2A2B4-B3   5- 21

C2   2A2A04J01D-02
C3   2A2A04J01D-01
D0   2A2A04J01J-02
D1   2A2A04J01J-01
D2        2A2A9-G2   5- 11

D3        2A2A8-G2   5-  9

E0   2A2A04J01G-02
E1   2A2A04J01G-01
E2   2A2A04J01R-02
E3   2A2A04J01R-01
F0        2A2A9-X1   5- 11

F1       -2A2A8-H0   5-  9

F3        2A2A9-I3   5- 11

G2        2A2A8-D3   5-  9

H0        2A2A8-F1   5-  9

H1        2A2B5-H0   5- 19
H2   2A2A04J01A-01
H3   2A2A04J01A-02
I3        2A2A8-A3   5-  9

J0   2A2A04J01F-02
J1   2A2A04J01F-01
J2        2A2A8-X1   5-  9

K0   2A1A06J05A-10
K1   2A1A06J05A-09
K2   2A2A04J01E-02
K3   2A2A04J01E-01
L0   2A1A06J05B-08
L1   2A1A06J05B-07
M0   2A1A06J03B-07
M1   2A1A06J03B-08
M2        2A2B9-F0   5- 23
M3        2A2B9-G0   5- 23
N0   2A1A06J07B-08
     2A1A06J08B-08
N1   2A1A06J07B-07
     2A1A06J08B-07
O0   2A1A06J07A-10
     2A1A06J08A-10
O1   2A1A06J07A-09
     2A1A06J08A-09
P0   2A1A06J03A-10
P1   2A1A06J03A-09
P2   2A1A06J05A-01
P3   2A1A06J05A-02
Q0        2A2B4-L0   5- 21
Q2   2A1A06J05A-06
Q3   2A1A06J05A-05
R0        2A2B5-B1   5- 19   2A2A8-AS
R2   2A1A06J03A-05
R3   2A1A06J03A-06
S0        2A2B4-H2   5- 21
S2   2A1A06J07A-06
     2A1A06J08A-06
S3   2A1A06J07A-05
     2A1A06J08A-05
T0        2A2A6-N1   5-  1
T1        2A2A6-P0   5-  1   2A2A8-AM
T2   2A1A06J07A-02
     2A1A06J08A-02
T3   2A1A06J07A-01
     2A1A06J08A-01
U0   2A1A06J06B-07
     1A4A06P01B-07
          1A0B4-S3   2- 69
U1   2A1A06J06B-08
     1A4A06P01B-08
          1A0B4-S2   2- 69
U2   2A1A06J03A-01
U3   2A1A06J03A-02
V0        2A1A6-B3   6- 49
V1        2A1A6-B2   6- 49
V2        2A1B7-U1   6- 41
V3        2A1B7-U0   6- 41
W0        2A1A5-B3   6- 47
W1        2A1A5-B2   6- 47
W2        2A1A5-B0   6- 47
W3        2A1A5-B1   6- 47
X1        2A2A8-J2   5-  9

X2        2A2B7-B1   5- 15   2A2A8-RZ
X3        2A2B6-B1   5- 17   2A2A8-RY

          PAGE   5-  9
```

```
STOR ADDR BIT 07 TO INDICATOR

STOR ADDR BIT 02 TO INDICATOR

NOT STOR ADDR BIT 06 TO PAR,
GENERATOR AND IND DRIVER

STOR ADDR BIT 03 TO INDICATOR

STOR ADDR BIT 08 TO INDICATOR
NOT STOR ADDR BIT 01 TO PAR,
GENERATOR AND IND DRIVER
NOT STOR ADDR BIT 00 TO PAR,
GENERATOR AND IND DRIVER

STOR ADDR BIT 06 TO INDICATOR

STOR ADDR BIT 01 TO INDICATOR
NOT STOR ADDR BIT 05 TO PAR,
GENERATOR AND IND DRIVER
NOT STOR ADDR BIT 08 TO PAR,
GENERATOR AND IND DRIVER
NOT STOR ADDR BIT 03 TO PAR,
GENERATOR AND IND DRIVER
NOT STOR ADDR BIT 00 TO PAR,
GENERATOR AND IND DRIVER
NOT STOR ADDR BIT 08 TO PAR,
GENERATOR AND IND DRIVER
ADDR BIT 15 TO TERMINATE
STOR ADDR BIT 00 TO INDICATOR

NOT STOR ADDR BIT 02 TO PAR,
GENERATOR AND IND DRIVER

STOR ADDR BIT 05 TO INDICATOR
NOT STOR ADDR BIT 04 TO PAR,
GENERATOR AND IND DRIVER

ADDR BIT 04 TO INTERNAL STOR B

STOR ADDR BIT 04 TO INDICATOR

ADDR BIT 08 TO INTERNAL STOR B
ADDR BIT 08 TO INTERNAL STOR A

ADDR PAR, GENERATE
ADDR PAR, GENERATE

ADDR BIT 08 TO EXTERNAL STOR

ADDR BIT 04 TO EXTERNAL STOR

ADDR BIT 04 TO INTERNAL STOR A
ADDR BIT 00 TO INTERNAL STOR B

ADDR BIT 08 TO DETECT ILL, WR,

MAIN CONTROL S BIT 04 SHIFTED
ADDR BIT 02 TO INTERNAL STOR A

ADDR, BITS 00, 02, AND 04 SET

ADDR BIT 02 TO EXTERNAL STOR

BLOCK CONTROL PRIORITY
LOAD S REGISTER

ADDR BIT 00 TO EXTERNAL STOR

S6(S BUS) BIT 08

ADDR BIT 00 TO INTERNAL STOR A

RC S BUS BIT 08 TO PAGE FILE

RC S BUS BIT 00 TO PAGE FILE

RC S BUS BIT 04 TO PAGE FILE

RC S BUS BIT 02 TO PAGE FILE

NOT STOR ADDR BIT 04 TO PAR,
GENERATOR AND IND DRIVER

MAIN CONTROL S BIT 00 SHIFTED
MAIN CONTROL S BIT 02 SHIFTED
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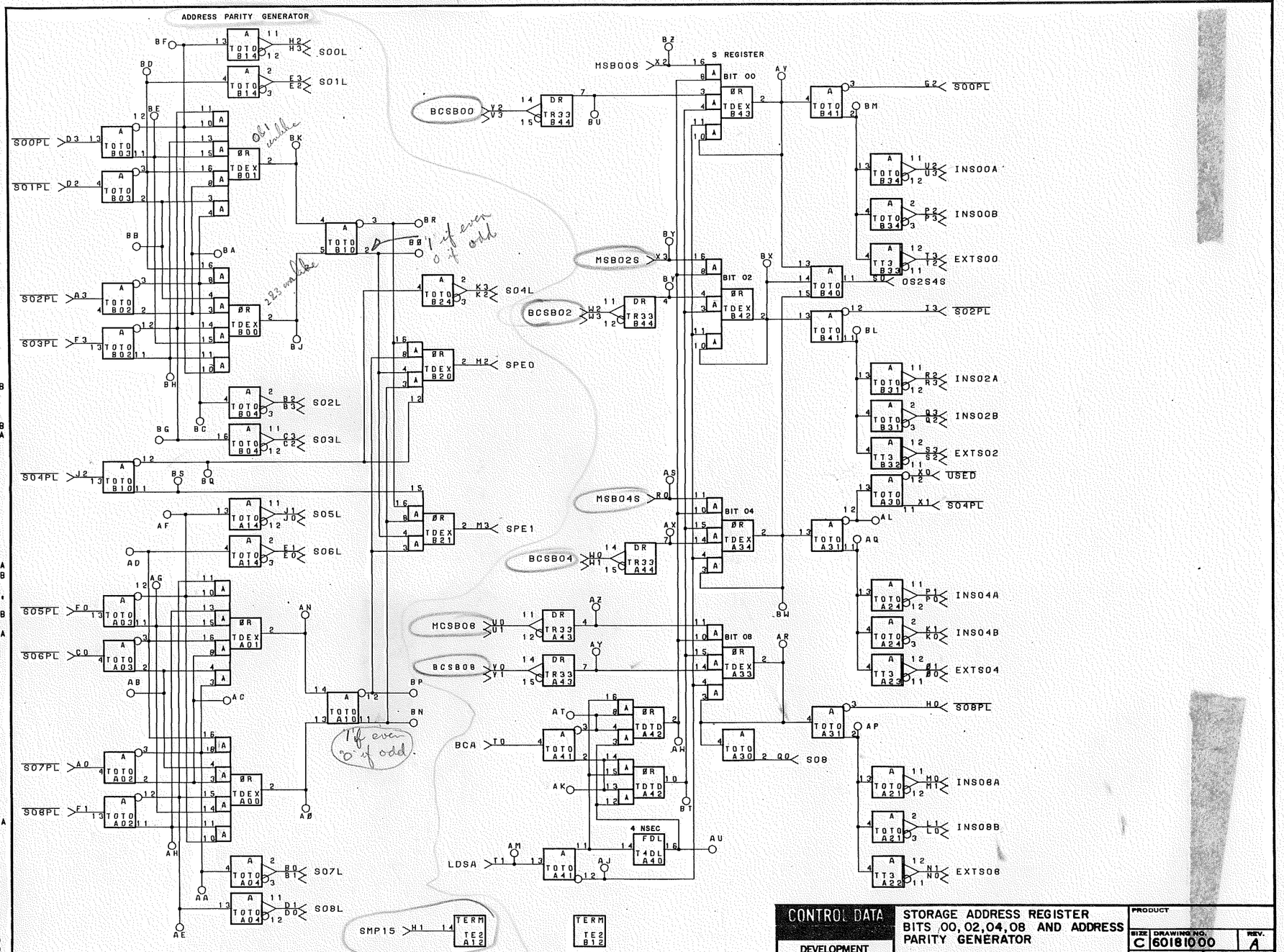


CONTROL DATA	STORAGE ADDRESS REGISTER BITS 00,02,04,08 AND ADDRESS PARITY GENERATOR	PRODUCT	
DEVELOPMENT DIVISION	LOC: 2A2A8 PART NO. 183374 SER.000	SIZE C / DRAWING NO. 60181000	REV. A
		SHEET	PAGE 5-9

35

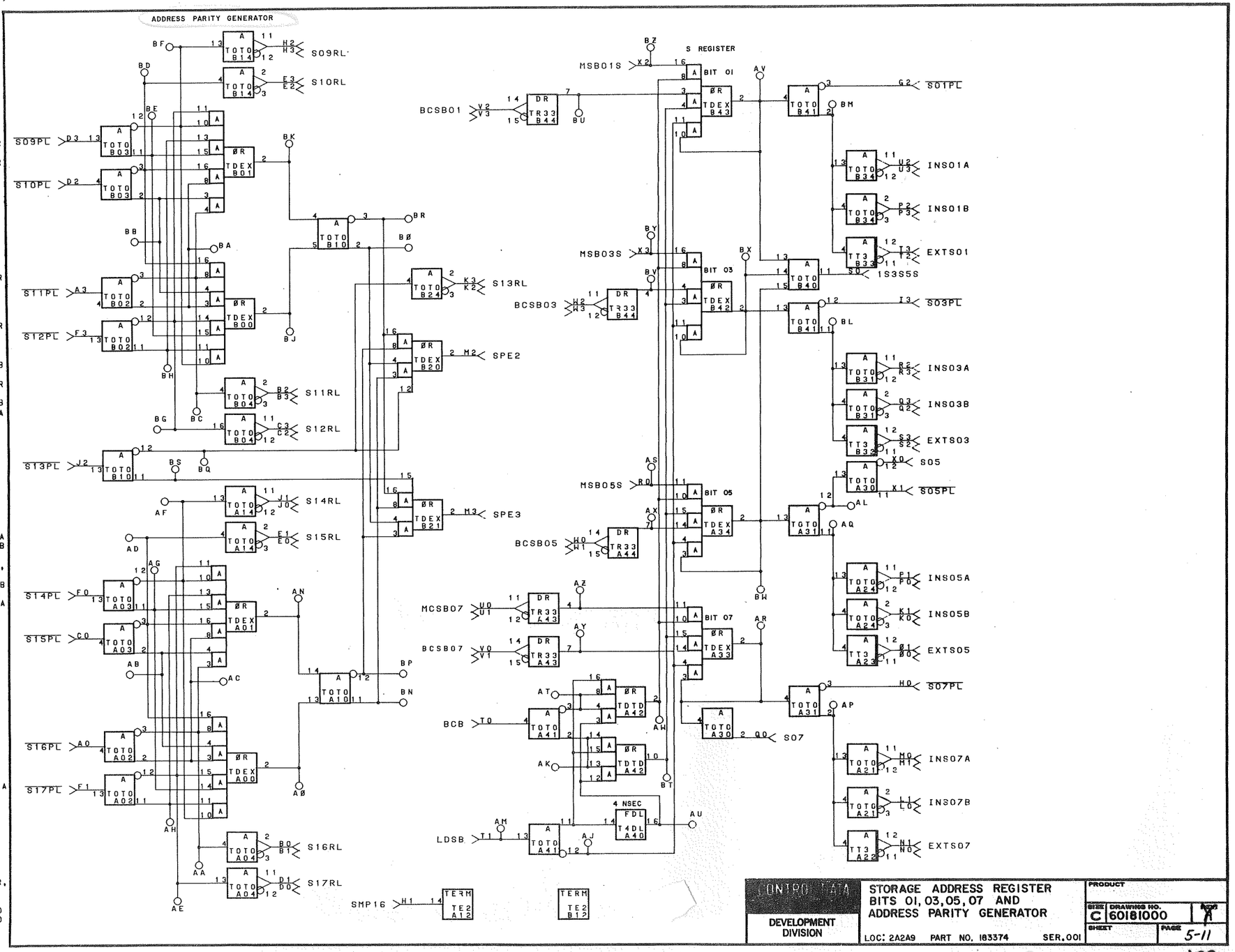
Bd 6 on Page 5-21

Y see above

PIN	ORIGIN/ DEST,	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A2B5-J3	5- 19		NOT STOR ADDR BIT 16 TO PAR, GENERATOR AND IND DRIVER
A3	2A2B7-K0	5- 15		NOT STOR ADDR BIT 11 TO PAR, GENERATOR AND IND DRIVER
B0	2A2A04J017-01			RELOC ADDR BIT 16 TO INDICATOR

B1	2A2A04J01T-02			
B2	2A2A04J01M-01			
B3	2A2A04J01M-02			
C0	2A2B5-K0	5- 19		RELOC ADDR BIT 11 TO INDICATOR
C2	2A2A04J01N-02			
C3	2A2A04J01N-01			NOT STOR ADDR BIT 15 TO PAR, GENERATOR AND IND DRIVER
D0	2A2A04J01U-02			
D1	2A2A04J01U-01			RELOC ADDR BIT 12 TO INDICATOR
D2	2A2B8-T2	5- 13		RELOC ADDR BIT 17 TO INDICATOR
D3	2A2B8-T3	5- 13		NOT STOR ADDR BIT 10 TO PAR, GENERATOR AND IND DRIVER NOT STOR ADDR BIT 09 TO PAR, GENERATOR AND IND DRIVER
E0	2A2A04J01S-02			
E1	2A2A04J01S-01			RELOC ADDR BIT 15 TO INDICATOR
E2	2A2A04J01L-02			
E3	2A2A04J01L-01			RELOC ADDR BIT 10 TO INDICATOR
F0	2A2B6-I3	5- 17		NOT STOR ADDR BIT 14 TO PAR, GENERATOR AND IND DRIVER
F1	2A2B4-I2	5- 21		NOT STOR ADDR BIT 17 TO PAR, GENERATOR AND IND DRIVER
F3	2A2B7-I3	5- 15		NOT STOR ADDR BIT 12 TO PAR, GENERATOR AND IND DRIVER
G2	2A2A8-D2	5- 9		NOT STOR ADDR BIT 01 TO PAR, GENERATOR AND IND DRIVER
H0	2A2A8-A0	5- 9		NOT STOR ADDR BIT 07 TO PAR, GENERATOR AND IND DRIVER
H1	2A2B5-X0	5- 19		ADDR BIT 16 TO TERMINATE
H2	2A2A04J01K-01			RELOC ADDR BIT 09 TO INDICATOR
H3	2A2A04J01K-02			
I3	2A2A8-F3	5- 9		NOT STOR ADDR BIT 03 TO PAR, GENERATOR AND IND DRIVER
J0	2A2A04J01R-02			
J1	2A2A04J01R-01			RELOC ADDR BIT 14 TO INDICATOR
J2	2A2B6-K0	5- 17		NOT STOR ADDR BIT 13 TO PAR, GENERATOR AND IND DRIVER
K0	2A1A06J05R-02			
K1	2A1A06J05R-01			ADDR BIT 05 TO INTERNAL STOR B
K2	2A2A04J01P-02			
K3	2A2A04J01P-01			RELOC ADDR BIT 13 TO INDICATOR
L0	2A1A06J05B-06			
L1	2A1A06J05R-05			ADDR BIT 07 TO INTERNAL STOR B
M0	2A1A06J03B-05			ADDR BIT 07 TO INTERNAL STOR A
M1	2A1A06J03R-06			
M2	2A2B9-E0	5- 23		ADDR PAR, GENERATE
M3	2A2B9-F1	5- 23		ADDR PAR, GENERATE
N0	2A1A06J07B-06			
	2A1A06J08R-06			
N1	2A1A06J07B-05			ADDR BIT 07 TO EXTERNAL STOR
	2A1A06J08R-05			
O0	2A1A06J07R-02			
	2A1A06J08B-02			
O1	2A1A06J07R-01			ADDR BIT 05 TO EXTERNAL STOR
	2A1A06J08B-01			
P0	2A1A06J03B-02			
P1	2A1A06J03B-01			ADDR BIT 05 TO INTERNAL STOR A
P2	2A1A06J05A-03			ADDR BIT 01 TO INTERNAL STOR B
P3	2A1A06J05A-04			
Q0	2A2B4-L1	5- 21		ADDR BIT 07 TO DETECT ILL, WR,
Q2	2A1A06J05A-08			
Q3	2A1A06J05A-07			ADDR BIT 03 TO INTERNAL STOR B
R0	2A2B5-C3	5- 19	2A2A9-AS	MAIN CONTROL S BIT 05 SHIFTED
R2	2A1A06J03A-07			ADDR BIT 03 TO INTERNAL STOR A
R3	2A1A06J03A-08			
S0	2A2B4-H3	5- 21		ADDR, BITS 01, 03, AND 05 SET
S2	2A1A06J07A-08			
	2A1A06J08A-08			
S3	2A1A06J07A-07			ADDR BIT 03 TO EXTERNAL STOR
	2A1A06J08A-07			
T0	2A2A6-M1	5- 1		BLOCK CONTROL PRIORITY
T1	2A2A6-Q1	5- 1	2A2A9-AM	LOAD S REGISTER
T2	2A1A06J07A-04			
	2A1A06J08A-04			
T3	2A1A06J07A-03			ADDR BIT 01 TO EXTERNAL STOR
	2A1A06J08A-03			
U0	2A1A06J06B-05			S6(S BUS) BIT 07
	1A4A06P01B-05			
	1A0B4-P2	2- 69		
U1	2A1A06J06B-06			
	1A4A06P01B-06			
	1A0B4-P3	2- 69		
U2	2A1A06J03A-03			ADDR BIT 01 TO INTERNAL STOR A
U3	2A1A06J03A-04			
V0	2A1A6-G1	6- 49		RC S BUS BIT 07 TO PAGE FILE
V1	2A1A6-G0	6- 49		
V2	2A1B7-X1	6- 41		RC S BUS BIT 01 TO PAGE FILE
V3	2A1B7-X0	6- 41		
W0	2A1A5-F2	6- 47		RC S BUS BIT 05 TO PAGE FILE
W1	2A1A5-F3	6- 47		
W2	2A1A5-G1	6- 47		RC S BUS BIT 03 TO PAGE FILE
W3	2A1A5-G0	6- 47		
X0	2A2B7-V0	5- 15		ADDR BIT 05 TO DETECT ILL, WR,
X1	2A2A8-F0	5- 9		NOT STOR ADDR BIT-05 TO PAR, GENERATOR AND IND DRIVER
X2	2A2B7-C3	5- 15	2A2A9-RZ	MAIN CONTROL S BIT 01 SHIFTED
X3	2A2B6-C3	5- 17	2A2A9-RY	MAIN CONTROL S BIT 03 SHIFTED

PAGE 5- 11

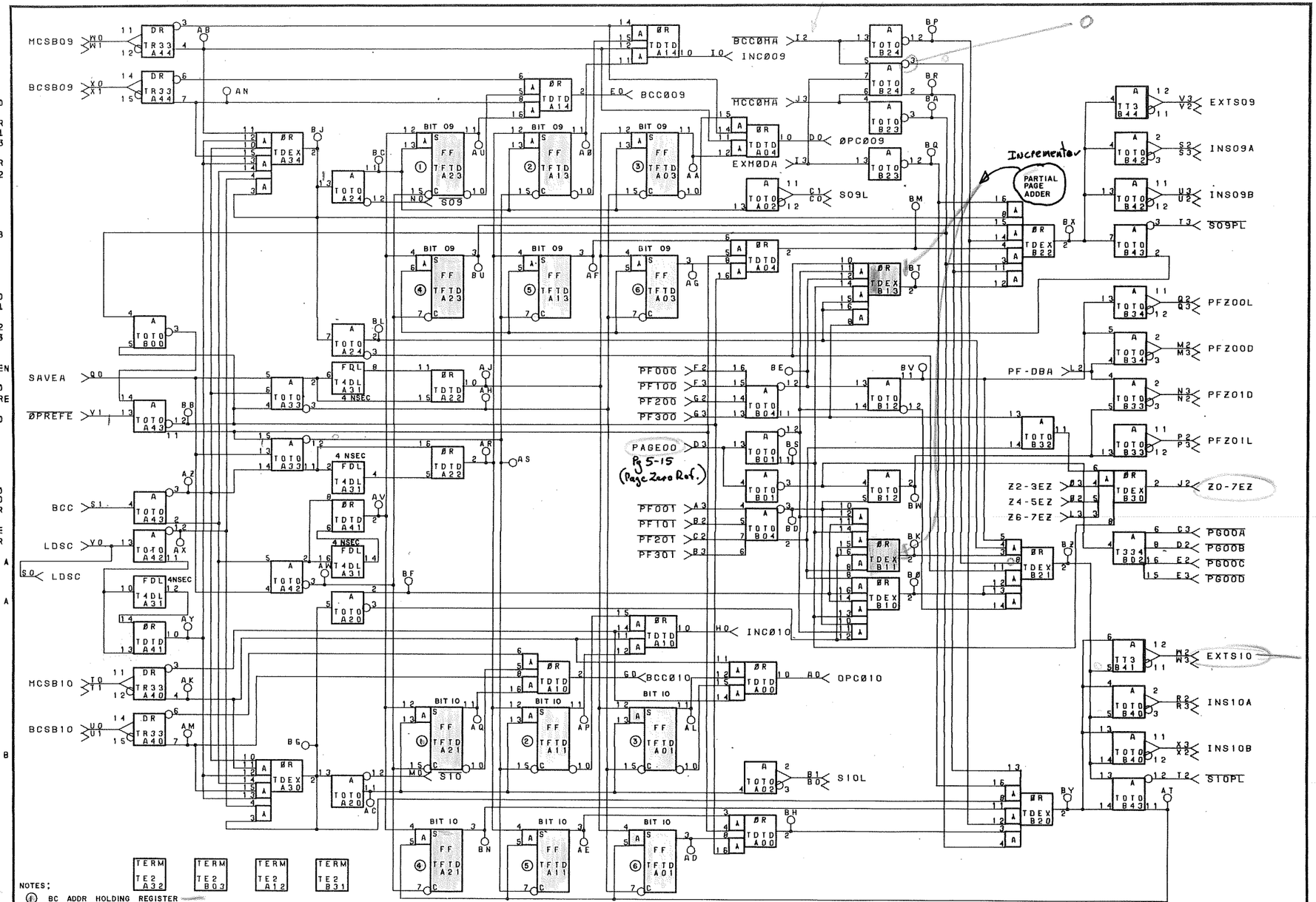


Bit 6 on Page 5-21

see above

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A2A6*V1	5* 1		ROP * STOR COMPARE BIT 10
A3	2A2B3*S0	5* 35		NOT BIT 01 FROM PF QUADRANT 0
B0	2A2A04J02P*02			
B1	2A2A04J02P*01			STOR ADDR BIT 10 TO INDICATOR
B2	2A2B2*S0	5* 41		NOT BIT 01 FROM PF QUADRANT 1
B3	2A2B0*S0	5* 53		NOT BIT 01 FROM PF QUADRANT 3
C0	2A2A04J02N*02			
C1	2A2A04J02N*01			STOR ADDR BIT 09 TO INDICATOR
C2	2A2B1*S0	5* 47		NOT BIT 01 FROM PF QUADRANT 2
C3	2A2B7*Q2	5* 15		NOT PAGE 0 TO ENABLE PAGE FILE QUADRANT BITS 2,3
D0	2A2A6*V0	5* 1	2A2A6-AY	ROP * STOR COMPARE BIT 09
D2	2A2B6*Q2	5* 17		NOT PAGE 0 TO ENABLE PAGE FILE QUADRANT BITS 4,5
D3	2A2B7*U2	5* 15		PAGE 0 TO DISABLE BITS 0 TO 8
E0	2A2A6*03	5* 1	2A2A6-RN	BLOCK CONTROL COMPARE BIT 09
E2	2A2B5*Q2	5* 19		NOT PAGE 0 TO ENABLE PAGE FILE QUADRANT BITS 6,7
E3	2A2B4*Q2	5* 21		NOT PAGE 0 TO ENABLE PAGE FILE QUADRANT BIT 8
F2	2A2B3*T1	5* 35		NOT BIT 00 FROM PF QUADRANT 0
F3	2A2B2*T1	5* 41		NOT BIT 00 FROM PF QUADRANT 1
G0	2A2A6*02	5* 1		BLOCK CONTROL COMPARE BIT 10
G2	2A2B1*T1	5* 47		NOT BIT 00 FROM PF QUADRANT 2
G3	2A2B0*T1	5* 53		NOT BIT 00 FROM PF QUADRANT 3
H0	2A2A6*U2	5* 1		RNI * RADR COMPARE BIT 10
I0	2A2A6*T2	5* 1	2A2A6-BU	RNI * RADR COMPARE BIT 09
I2	2A2A6*M2	5* 1		NOT BLOCK CONTROL ADDR COMP EN
I3	2A2A6*E2	5* 1		EXECUTIVE MODE
J2	2A2B4*P1	5* 21		PAGE FILE OUT BITS 0 TO 7 = 0
J3	2A2A6*B3	5* 1		NOT MAIN CONTROL ADDR, COMPARE
L2	2A2A5*R2	5* 3		ENABLE PAGE FILE TO DATA BUS
L3	2A2B5*T3	5* 19		PAGE FILE OUT BITS 6 TO 7 = 0
M0	2A2B4*H1	5* 21		NOT ADDRESS BIT 10
M2	2B2A9*H3	5* 57		BIT 00 OUT OF PF TO DB XMTR
M3	2B2A9*H2	5* 57		
N0	2A2B4*J1	5* 21		NOT ADDRESS BIT 00
N2	2B2A9*G2	5* 57		
N3	2B2A9*G3	5* 57		BIT 01 OUT OF PF TO DB XMTR
O2	2A2B6*T3	5* 17		PAGE FILE OUT BITS 4 TO 5 = 0
O3	2A2B7*T3	5* 15		PAGE FILE OUT BITS 2 TO 3 = 0
P2	2A2A04J02B*01			BIT 01 OUT OF PF TO INDICATOR
P3	2A2A04J02B*02			
Q0	2A2A5*B3	5* 3		SAVE NEW (S) REG UNTIL CHANGE
Q2	2A2A04J02A*01			BIT 00 OUT OF PF TO INDICATOR
Q3	2A2A04J02A*02			
R2	2A1A06J03C*01			ADDR BIT 10 TO INTERNAL STOR A
R3	2A1A06J03C*02			
S0	2A2A6*00	5* 1		LOAD S REGISTER
S1	2A2A6*L0	5* 1		BLOCK CONTROL PRIORITY
S2	2A1A06J03A*09			ADDR BIT 09 TO INTERNAL STOR A
S3	2A1A06J03B*10			
T0	2A1A06J06C*01			S6(S BUS) BIT 10
	1A4A06P01C*01			
	1A0B2*P2	2* 71		
T1	2A1A06J06C*02			
	1A4A06P01C*02			
	1A0B2*P3	2* 71		
T2	2A2A9*D2	5* 11		NOT STOR ADDR BIT 10 TO PAR, GENERATOR AND IND DRIVER
T3	2A2A9*D3	5* 11		NOT STOR ADDR BIT 09 TO PAR, GENERATOR AND IND DRIVER
U0	2A1A7*B0	6* 51		BC S BUS BIT 10 TO PAGE FILE
U1	2A1A7*B1	6* 51		
U2	2A1A06J05B*10			ADDR BIT 09 TO INTERNAL STOR B
U3	2A1A06J05B*09			
V0	2A2B4*K3	5* 21		LOAD S REGISTER
V1	2A2A5*D3	5* 3		NOT OPERAND REFERENCE
V2	2A1A06J07B*10			
	2A1A06J08B*10			ADDR BIT 09 TO EXTERNAL STOR
V3	2A1A06J07B*09			
	2A1A06J08B*09			
W0	2A1A06J06B*09			S6(S BUS) BIT 09
	1A4A06P01B*09			
	1A0B2*M2	2* 71		
W1	2A1A06J06A*10			
	1A4A06P01B*10			
	1A0B2*M3	2* 71		
W2	2A1A06J07C*01, 2A1A06J08C*01			ADDR BIT 10 TO EXTERNAL STOR
W3	2A1A06J07C*02 2A1A06J08C*02			
X0	2A1A6*F2	6* 49		BC S BUS BIT 09 TO PAGE FILE
X1	2A1A6*F3	6* 49		
X2	2A1A06J05C*02			ADDR BIT 10 TO INTERNAL STOR B
X3	2A1A06J05C*01			

PAGE 5* 13



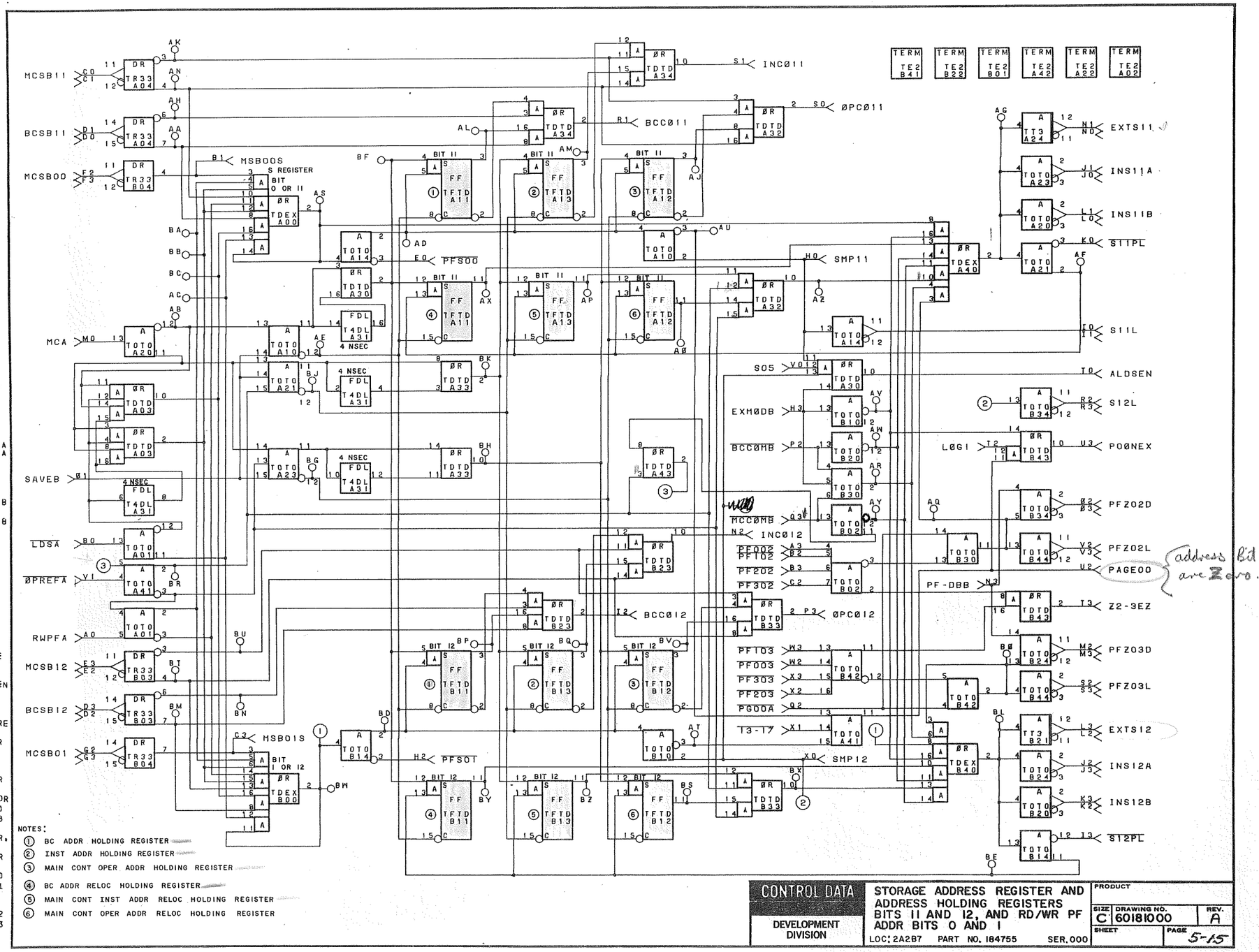
NOTES:
1. BC ADDR HOLDING REGISTER
2. INST ADDR HOLDING REGISTER
3. MAIN CONT OPER ADDR HOLDING REGISTER
4. BC ADDR RELOC HOLDING REGISTER
5. MAIN CONT INST ADDR RELOC HOLDING REG
6. MAIN CONT OPER ADDR RELOC HOLDING REG

CONTROL DATA	STORAGE ADDRESS REGISTER AND ADDRESS HOLDING REGISTERS BITS 09 AND 10, AND PARTIAL PAGE ADDER	PRODUCT	
DEVELOPMENT DIVISION	LOC: 2A2B0 PART NO. 184663 SER. 000	SIZE C / DRAWING NO. 60181000 / REV. A	SHEET / PAGE 5-13

PIN	ORIGIN/ DEST,	PAGE	TEST POINT	SIGNAL DEFINITION,
A0	2A2A5-03	5- 3		READ/WRITE PAGE FILE

A3	2A2R3*S1	5* 35		NOT BIT 02 FROM PF QUADRANT 0
B0	2A2A6*P1	5* 1		NOT LOAD S REGISTER
B1	2A2A8*X2	5* 9	2A2A8-PZ	MAIN CONTROL S BIT 00 SHIFTED
B2	2A2R2*S1	5* 41		NOT BIT 02 FROM PF QUADRANT 1
B3	2A2R1*S1	5* 47		NOT BIT 02 FROM PF QUADRANT 2
C0	2A1A06J06C*03			S6(S BUS) BIT 11
	1A4A06P01C*03			
	1A0R2*S3	2* 71		
C1	2A1A06J06C*04			
	1A4A06P01C*04			
	1A0B2*S2	2* 71		
C2	2A2R0*S1	5* 53		NOT BIT 02 FROM PF QUADRANT 3
C3	2A2A9*X2	5* 11	2A2A9-PZ	MAIN CONTROL S BIT 01 SHIFTED
D0	2A1A7*G0	6* 51		
D1	2A1A7*G1	6* 51		BC S BUS BIT 11 TO PAGE FILE
D2	2A1A7*B2	6* 51		
D3	2A1A7*B3	6* 51		BC S BUS BIT 12 TO PAGE FILE
E0	2A2A4*M0	5* 7		NOT PAGE FILE ADDRESS BIT 00
E2	2A1A06J06C*06			
	1A4A06P01C*06			
	1A0B0*M3	2* 73		
E3	2A1A06J06C*05			S6(S BUS) BIT 12
	1A4A06P01C*05			
	1A0B0*M2	2* 73		
F2	2A1A06J06A*01			S6(S BUS) BIT 00
	1A4A06P01A*01			
	1A0B8*M2	2* 65		
F3	2A1A06J06A*02			
	1A4A06P01A*02			
	1A0B8*M3	2* 65		
G2	2A1A06J06A*03			S6(S BUS) BIT 01
	1A4A06P01A*03			
	1A0B8*P2	2* 65		
G3	2A1A06J06A*04			
	1A4A06P01A*04			
	1A0B8*P3	2* 65		
H0	2A2B9*A3	5* 23		ADDR BIT 11 TO STOR PROTECT
H2	2A2A4*G0	5* 7		NOT PAGE FILE ADDRESS BIT 01
H3	2A2A6*G2	5* 1		EXECUTIVE MODE
I0	2A2A04J02R*01			STOR ADDR BIT 11 TO INDICATOR
I1	2A2A04J02R*02			
I2	2A2A6*Q2	5* 1		BLOCK CONTROL COMPARE BIT 12
I3	2A2A9*F3	5* 11		NOT STOR ADDR BIT 12 TO PAR, GENERATOR AND IND DRIVER
J0	2A1A06J03C*04			
J1	2A1A06J03C*03			ADDR BIT 11 TO INTERNAL STOR A
J2	2A1A06J03C*05			ADDR BIT 12 TO INTERNAL STOR A
J3	2A1A06J03C*06			
K0	2A2A9*A3	5* 11		NOT STOR ADDR BIT 11 TO PAR, GENERATOR AND IND DRIVER
K2	2A1A06J05C*06			
K3	2A1A06J05C*05			ADDR BIT 12 TO INTERNAL STOR B
L0	2A1A06J05C*04			
L1	2A1A06J05C*03			ADDR BIT 11 TO INTERNAL STOR B
L2	2A1A06J07C*06			
	2A1A06J08C*06			
L3	2A1A06J07C*05			ADDR BIT 12 TO EXTERNAL STOR
	2A1A06J08C*05			
M0	2A2A6*N0	5* 1		MAIN CONTROL PRIORITY
M2	2B2A8*H3	5* 59		BIT 03 OUT OF PF TO DB XMTR
M3	2B2A8*H2	5* 59		
N0	2A1A06J07C*04			
	2A1A06J08C*04			ADDR BIT 11 TO EXTERNAL STOR
N1	2A1A06J07C*03			
	2A1A06J08C*03			
N2	2A2A6*V3	5* 1		RNI * RADR COMPARE BIT 12
N3	2A2A5*R3	5* 3		ENABLE PAGE FILE TO DATA BUS
O1	2A2A5*S3	5* 3		SAVE NEW (S) REG UNTIL CHANGE
O2	2B2A9*R1	5* 57		BIT 02 OUT OF PF TO DB XMTR
O3	2B2A9*R0	5* 57		
P2	2A2A6*H3	5* 1		NOT BLOCK CONTROL ADDR COMP EN
P3	2A2A6*H0	5* 1		ROP * STOR COMPARE BIT 12
Q2	2A2B8*C3	5* 13		NOT PAGE 0 TO ENABLE PAGE FILE QUADRANT BITS 2,3
Q3	2A2A6*C3	5* 1		NOT MAIN CONTROL ADDR, COMPARE
R1	2A2A6*P3	5* 1		BLOCK CONTROL COMPARE BIT 11
R2	2A2A04J02S*01			STOR ADDR BIT 12 TO INDICATOR
R3	2A2A04J02S*02			
S0	2A2A6*W1	5* 1		ROP * STOR COMPARE BIT 11
S1	2A2A6*U3	5* 1		RNI * RADR COMPARE BIT 11
S2	2A2A04J02D*01			BIT 03 OUT OF PF TO INDICATOR
S3	2A2A04J02D*02			
T0	2A2B6*V0	5* 17		SENSE AUTO LOAD/AUTO DUMP ADDR
T3	2A2B8*O3	5* 13		PAGE FILE OUT BITS 2 TO 3 = 0
U2	2A2B8*D3	5* 13		PAGE 0 TO DISABLE BITS 0 TO 8
U3	2A2A5*D1	5* 3		PAGE 0 OR NOT EXECUTIVE MODE
V0	2A2A9*X0	5* 11		ADDR BIT 05 TO DETECT ILL, WR, NOT OPERAND REFERENCE
V1	2A2A5*B2	5* 3		BIT 02 OUT OF PF TO INDICATOR
V2	2A2A04J02C*01			
V3	2A2A04J02C*02			
W2	2A2B3*X0	5* 35		NOT BIT 03 FROM PF QUADRANT 0
W3	2A2B2*X0	5* 41		NOT BIT 03 FROM PF QUADRANT 1
X0	2A2B9*B3	5* 23		ADDR BIT 12 TO STOR PROTECT
X1	2A2B6*U2	5* 17		NOT ADDRESS BITS 13 TO 17
X2	2A2B1*X0	5* 47		NOT BIT 03 FROM PF QUADRANT 2
X3	2A2B0*X0	5* 53		NOT BIT 03 FROM PF QUADRANT 3

PAGE 5* 15



NOTES:
1. BC ADDR HOLDING REGISTER
2. INST ADDR HOLDING REGISTER
3. MAIN CONT OPER ADDR HOLDING REGISTER
4. BC ADDR RELOC HOLDING REGISTER
5. MAIN CONT INST ADDR RELOC HOLDING REGISTER
6. MAIN CONT OPER ADDR RELOC HOLDING REGISTER

CONTROL DATA
DEVELOPMENT DIVISION

STORAGE ADDRESS REGISTER AND ADDRESS HOLDING REGISTERS BITS 11 AND 12, AND RD/WR PF ADDR BITS 0 AND 1

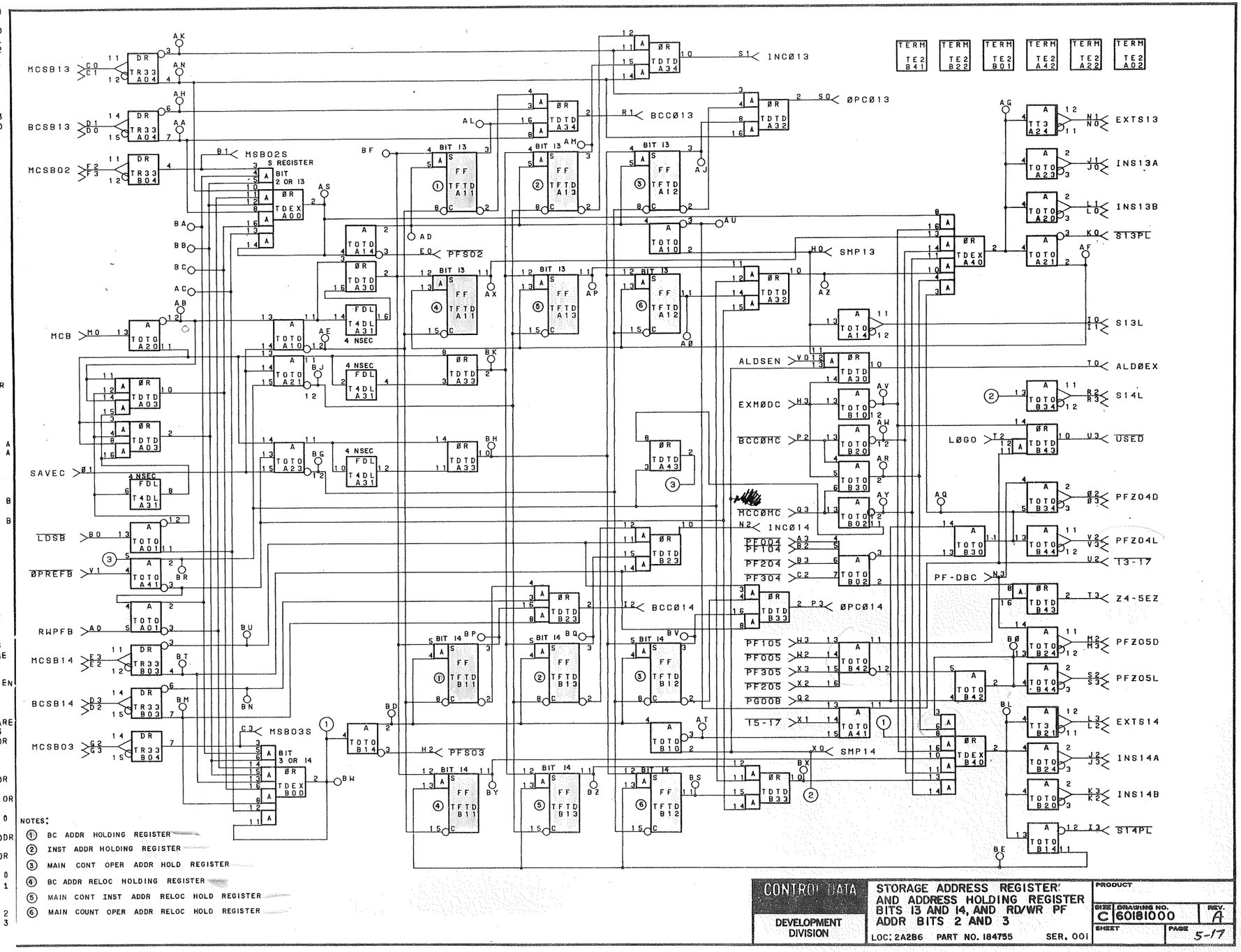
LOC: 2A2B7 PART NO. 184755 SER. 000

PRODUCT
SIZE C | DRAWING NO. 60181000 | REV. A
SHEET | PAGE 5-15

41

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A2A5*02	5* 3		READ/WRITE PAGE FILE

A3	2A2B3-X1	5- 35		NOT BIT 04 FROM PF QUADRANT 0
B0	2A2A6-Q0	5- 1		NOT LOAD S REGISTER
B1	2A2A8-X3	5- 9	2A2A8-RY	MAIN CONTROL S BIT 02 SHIFTED
B2	2A2B2-X1	5- 41		NOT BIT 04 FROM PF QUADRANT 1
B3	2A2B1-X1	5- 47		NOT BIT 04 FROM PF QUADRANT 2
C0	2A1A06J06C-07			S6(S BUS) BIT 13
	1A4A06P01C-07			
	1A0B0-P2	2- 73		
C1	2A1A06J06C-08			
	1A4A06P01C-08			
	1A0B0-P3	2- 73		
C2	2A2B0-X1	5- 53		NOT BIT 04 FROM PF QUADRANT 3
C3	2A2A9-X3	5- 11	2A2A9-RY	MAIN CONTROL S BIT 03 SHIFTED
D0	2A1A7-F3	6- 51		
D1	2A1A7-F2	6- 51		RC S BUS BIT 13 TO PAGE FILE
D2	2A1B8-F0	6- 53		
D3	2A1B8-F1	6- 53		RC S BUS BIT 14 TO PAGE FILE
E0	2A2A4-J1	5- 7		NOT PAGE FILE ADDRESS BIT 02
E2	2A1A06J06C-10			
	1A4A06P01C-10			
	1A0B0-S2	2- 73		
E3	2A1A06J06C-09			S6(S BUS) BIT 14
	1A4A06P01C-09			
	1A0B0-S3	2- 73		
F2	2A1A06J06A-05			S6(S BUS) BIT 02
	1A4A06P01A-05			
	1A0R8-S3	2- 65		
F3	2A1A06J06A-06			
	1A4A06P01A-06			
	1A0B8-S2	2- 65		
G2	2A1A06J06A-07			S6(S BUS) BIT 03
	1A4A06P01A-07			
	1A0B6-M2	2- 67		
G3	2A1A06J06A-08			
	1A4A06P01A-08			
	1A0B6-M3	2- 67		
H0	2A2B9-K3	5- 23		ADDR BIT 13 TO STOR PROTECT
H2	2A2A4-E3	5- 7		NOT PAGE FILE ADDRESS BIT 03
H3	2A2A6-I3	5- 1		EXECUTIVE MODE
I0	2A2A04J02Y-01			STOR ADDR BIT 13 TO INDICATOR
I1	2A2A04J02Y-02			
I2	2A2A6-R2	5- 1		BLOCK CONTROL COMPARE BIT 14
I3	2A2A9-F0	5- 11		NOT STOR ADDR BIT 14 TO PAR, GENERATOR AND IND DRIVER
J0	2A1A06J03C-08			ADDR BIT 13 TO INTERNAL STOR A
J1	2A1A06J03C-07			ADDR BIT 14 TO INTERNAL STOR A
J2	2A1A06J03C-09			
J3	2A1A06J03C-10			
K0	2A2A9-J2	5- 11		NOT STOR ADDR BIT 13 TO PAR, GENERATOR AND IND DRIVER
K2	2A1A06J05C-10			
K3	2A1A06J05C-09			ADDR BIT 14 TO INTERNAL STOR B
L0	2A1A06J05C-08			
L1	2A1A06J05C-07			ADDR BIT 13 TO INTERNAL STOR B
L2	2A1A06J07C-10			
	2A1A06J08C-10			
L3	2A1A06J07C-09			ADDR BIT 14 TO EXTERNAL STOR
	2A1A06J08C-09			
M0	2A2A6-M0	5- 1		MAIN CONTROL PRIORITY
M2	2B2A8-R1	5- 59		BIT 05 OUT OF PF TO DB XMTR
M3	2B2A8-R0	5- 59		
N0	2A1A06J07C-08			
	2A1A06J08C-08			ADDR BIT 13 TO EXTERNAL STOR
N1	2A1A06J07C-07			
	2A1A06J08C-07			
N2	2A2A6-V2	5- 1		RNI = RADR COMPARE BIT 14
N3	2A2A5-Q3	5- 3		ENABLE PAGE FILE TO DATA BUS
O1	2A2A5-H3	5- 3		SAVE NEW (S) REG UNTIL CHANGE
O2	2B2A8-G3	5- 59		BIT 04 OUT OF PF TO DB XMTR
O3	2B2A8-G2	5- 59		
P2	2A2A6-P2	5- 1		NOT BLOCK CONTROL ADDR COMP EN
P3	2A2A6-K2	5- 1		ROP = STOR COMPARE BIT 14
Q2	2A2B8-D2	5- 13		NOT PAGE 0 TO ENABLE PAGE FILE QUADRANT BITS 4,5
Q3	2A2A6-D2	5- 1		NOT MAIN CONTROL ADDR, COMPARE
R1	2A2A6-T3	5- 1	2A2A6-RS	BLOCK CONTROL COMPARE BIT 13
R2	2A2A04J02U-01			STOR ADDR BIT 14 TO INDICATOR
R3	2A2A04J02U-02			
S0	2A2A6-K3	5- 1	2A2A6-RG	ROP = STOR COMPARE BIT 13
S1	2A2A6-X3	5- 1	2A2A6-RY	RNI = RADR COMPARE BIT 13
S2	2A2A04J02F-01			BIT 05 OUT OF PF TO INDICATOR
S3	2A2A04J02F-02			
T0	2A2A5-C0	5- 3		AUTO LOAD/AUTO DUMP ADDRESS OR EXECUTIVE MODE
T3	2A2B8-O2	5- 13		PAGE FILE OUT BITS 4 TO 5 = 0
U2	2A2B7-X1	5- 15		NOT ADDRESS BITS 13 TO 17
V0	2A2B7-T0	5- 15		SENSE AUTO LOAD/AUTO DUMP ADDR
V1	2A2A5-C2	5- 3		NOT OPERAND REFERENCE
V2	2A2A04J02E-01			BIT 04 OUT OF PF TO INDICATOR
V3	2A2A04J02E-02			
W2	2A2B3-W0	5- 35		NOT BIT 05 FROM PF QUADRANT 0
W3	2A2B2-W0	5- 41		NOT BIT 05 FROM PF QUADRANT 1
X0	2A2B9-P3	5- 23		ADDR BIT 14 TO STOR PROTECT
X1	2A2B5-U2	5- 19		NOT ADDRESS BITS 15 TO 17
X2	2A2B1-W0	5- 47		NOT BIT 05 FROM PF QUADRANT 2
X3	2A2B0-W0	5- 53		NOT BIT 05 FROM PF QUADRANT 3



NOTES:
1. BC ADDR HOLDING REGISTER
2. INST ADDR HOLDING REGISTER
3. MAIN CONT OPER ADDR HOLD REGISTER
4. BC ADDR RELOC HOLDING REGISTER
5. MAIN CONT INST ADDR RELOC HOLD REGISTER
6. MAIN COUNT OPER ADDR RELOC HOLD REGISTER

CONTROL DATA
DEVELOPMENT DIVISION

STORAGE ADDRESS REGISTER AND ADDRESS HOLDING REGISTER BITS 13 AND 14, AND RD/WR PF ADDR BITS 2 AND 3

LOC: 2A2B6 PART NO. 184755 SER. 001

PRODUCT
SIZE C | DRAWING NO. 60181000 | REV. A
SHEET | PAGE 5-17

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A2A5-S2	5- 3		READ/WRITE PAGE FILE

F2 2A2B4 H3 5-21 S 1235
I2 2A2B7-F3 S9,13
J3 2A2A963 S10, 11, 12, 14
S0 2A2B4 H2 S9,4+S4,9→14 5-2

S REGISTER

STORAGE ADDRESS REGISTER
BITS 00, 02, 04, 08 AND ADDRESS
PARITY GENERATOR

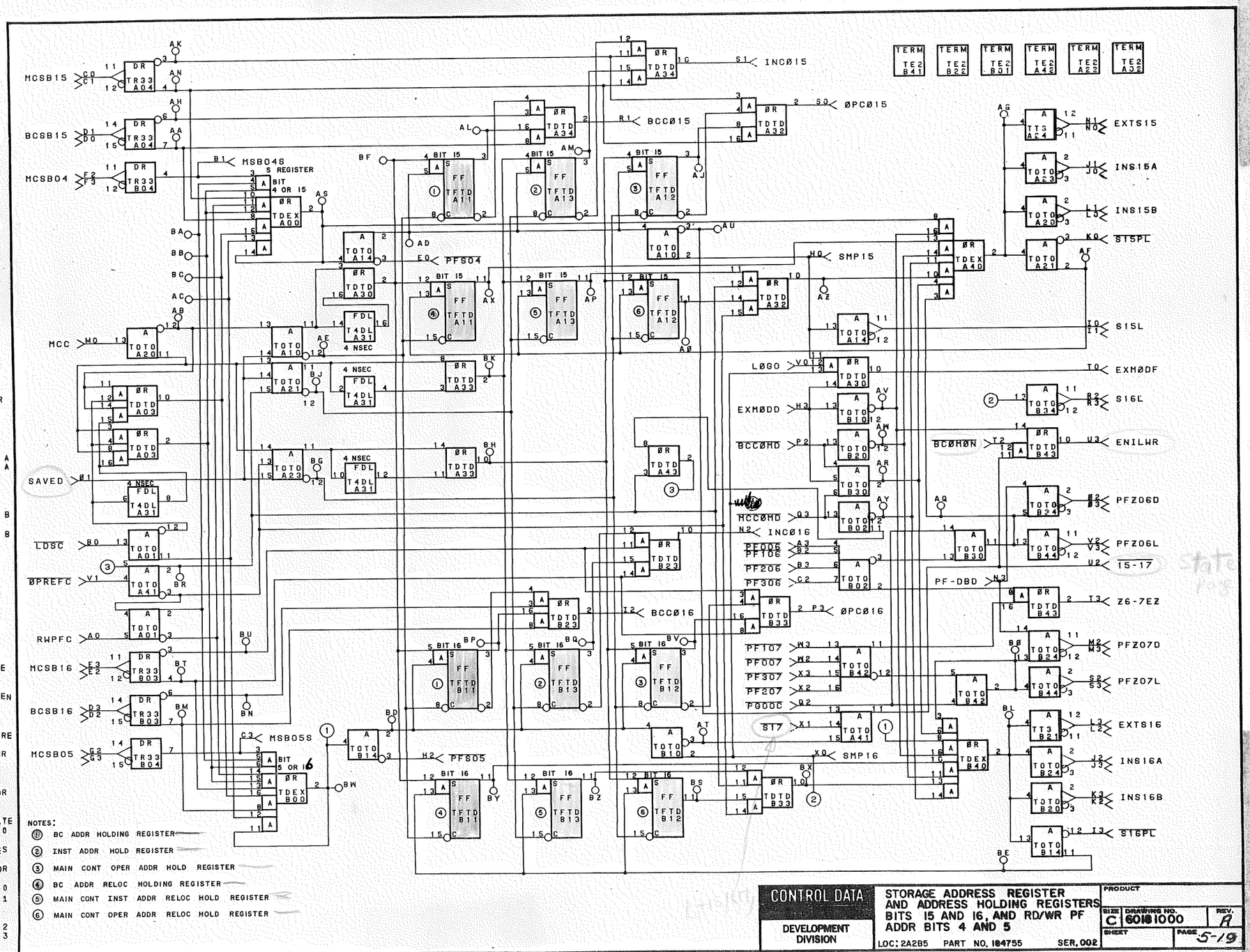
DEVELOPMENT DIVISION

LOC: 2A2A8 PART NO. 183374 SER.000

PRODUCT
SIZE C DRAWING NO. 60181000 Y
SHEET PAGE 5-9

2-43B
2-43A
5-9

A3	2A2B3=N1	5= 33		NOT BIT 06 FROM PF QUADRANT 0
B0	2A2A6=01	5= 1		NOT LOAD S REGISTER
B1	2A2A8=R0	5= 9	2A2A8=AS	MAIN CONTROL S BIT 04 SHIFTED
B2	2A2B2=N1	5= 39		NOT BIT 06 FROM PF QUADRANT 1
B3	2A2B1=N1	5= 45		NOT BIT 06 FROM PF QUADRANT 2
C0	2A1A06P03D=01			C4 FAN IN BIT 0(S BUS BIT 15)
	1A4A06J20D=01			
	1C0A3=H0	2= 39		
C1	2A1A06P03D=02			
	1A4A06J20D=02			
	1C0A3=M1	2= 39		
C2	2A2B0=N1	5= 51		NOT BIT 06 FROM PF QUADRANT 3
C3	2A2A9=R0	5= 11	2A2A9=AS	MAIN CONTROL S BIT 05 SHIFTED
D0	2A1A8=K0	6= 55		
D1	2A1A8=K1	6= 55		BC S BUS BIT 15 TO PAGE FILE
D2	2A1A8=I0	6= 55		
D3	2A1A8=I1	6= 55		BC S BUS BIT 16 TO PAGE FILE
E0	2A2A4=G3	5= 7		NOT PAGE FILE ADDRESS BIT 04
E2	2A1A06P03D=04			
	1A4A06J20D=04			
	1C0A3=T1	2= 39		
E3	2A1A06P03D=03			C4 FAN IN BIT 1(S BUS BIT 16)
	1A4A06J20D=03			
	1C0A3=T0	2= 39		
F2	2A1A06J06A=09			S6(S BUS) BIT 04
	1A4A06P01A=09			
	1A0B6=P2	2= 67		
F3	2A1A06J06A=10			
	1A4A06P01A=10			
	1A0B6=P3	2= 67		S6(S BUS) BIT 05
G2	2A1A06J06B=01			
	1A4A06P01B=01			
	1A0B6=S3	2= 67		
G3	2A1A06J06B=02			
	1A4A06P01B=02			
	1A0B6=S2	2= 67		
H0	2A2A8=H1	5= 9		ADDR BIT 15 TO TERMINATE
H2	2A2A4=G0	5= 7		NOT PAGE FILE ADDRESS BIT 05
H3	2A2A6=F2	5= 1		EXECUTIVE MODE
I0	2A2A04J02V=01			STOR ADDR BIT 15 TO INDICATOR
I1	2A2A04J02V=02			
I2	2A2A6=S3	5= 1		BLOCK CONTROL COMPARE BIT 16
I3	2A2A9=A0	5= 11		NOT STOR ADDR BIT 16 TO PAR, GENERATOR AND IND DRIVER
J0	2A1A06J03D=02			ADDR BIT 15 TO INTERNAL STOR A
J1	2A1A06J03D=01			ADDR BIT 16 TO INTERNAL STOR A
J2	2A1A06J03D=03			
J3	2A1A06J03D=04			NOT STOR ADDR BIT 15 TO PAR, GENERATOR AND IND DRIVER
K0	2A2A9=C0	5= 11		
K2	2A1A06J05D=04			ADDR BIT 16 TO INTERNAL STOR B
K3	2A1A06J05D=03			
L0	2A1A06J05D=02			ADDR BIT 15 TO INTERNAL STOR B
L1	2A1A06J05D=01			
L2	2A1A06J07D=04			
	2A1A06J08D=04			ADDR BIT 16 TO EXTERNAL STOR
L3	2A1A06J07D=03			
	2A1A06J08D=03			
M0	2A2A6=L1	5= 1		MAIN CONTROL PRIORITY
M2	2B2A7=G3	5= 61		BIT 07 OUT OF PF TO DB XMTR
M3	2B2A7=G2	5= 61		
N0	2A1A06J07D=02			ADDR BIT 15 TO EXTERNAL STOR
	2A1A06J08D=02			
N1	2A1A06J07D=01			
	2A1A06J08D=01			
N2	2A2A6=N3	5= 1		RNI = RADR COMPARE BIT 16
N3	2A2A5=P2	5= 3		ENABLE PAGE FILE TO DATA BUS
O1	2A2A5=H2	5= 3		SAVE NEW (S) REG UNTIL CHANGE
O2	2B2A7=H3	5= 61		BIT 06 OUT OF PF TO DB XMTR
O3	2B2A7=H2	5= 61		
P2	2A2A6=Q3	5= 1		NOT BLOCK CONTROL ADDR COMP EN
P3	2A2A6=L3	5= 1		ROP = STOR COMPARE BIT 16
Q2	2A2B8=E2	5= 13		NOT PAGE 0 TO ENABLE PAGE FILE QUADRANT BITS 6,7
Q3	2A2A6=D3	5= 1		NOT MAIN CONTROL ADDR, COMPARE
R1	2A2A6=R3	5= 1		BLOCK CONTROL COMPARE BIT 15
R2	2A2A04J03A=01			STOR ADDR BIT 16 TO INDICATOR
R3	2A2A04J03A=02			
S0	2A2A6=L2	5= 1		ROP = STOR COMPARE BIT 15
S1	2A2A6=W2	5= 1		RNI = RADR COMPARE BIT 15
S2	2A2A04J02H=01			BIT 07 OUT OF PF TO INDICATOR
S3	2A2A04J02H=02			
T0	2A2B4=A3	5= 21		EXECUTIVE MODE
T2	2A2A5=G0	5= 3		NOT BLOCK CONTROL OR MON STATE
T3	2A2B8=L3	5= 13		PAGE FILE OUT BITS 6 TO 7 = 0
U2	2A2B6=X1	5= 17		NOT ADDRESS BITS 15 TO 17
U3	2A2A5=A0	5= 3		ENABLE ILLEGAL WRITE SWITCHES
V1	2A2A5=C3	5= 3		NOT OPERAND REFERENCE
V2	2A2A04J02G=01			BIT 06 OUT OF PF TO INDICATOR
V3	2A2A04J02G=02			
W2	2A2B3=M0	5= 33		NOT BIT 07 FROM PF QUADRANT 0
W3	2A2B2=M0	5= 39		NOT BIT 07 FROM PF QUADRANT 1
X0	2A2A9=H1	5= 11		ADDR BIT 16 TO TERMINATE
X1	2A2B4=J2	5= 21		NOT ADDRESS BIT 17
X2	2A2B1=M0	5= 45		NOT BIT 07 FROM PF QUADRANT 2
X3	2A2B0=M0	5= 51		NOT BIT 07 FROM PF QUADRANT 3



CONTROL DATA	STORAGE ADDRESS REGISTER AND ADDRESS HOLDING REGISTERS BITS 15 AND 16, AND RD/WR PF ADDR BITS 4 AND 5	PRODUCT	
DEVELOPMENT DIVISION	LOC: 2A2B5 PART NO. 184755 SER. 002	SIZE C	DRAWING NO. 60181000 REV. A
		SHEET	PAGE 5-19

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A2A5-D0	5- 3	2A2A5-AF	PAGE FILE ILLEGAL WRITE SENSED
A3	2A2B5-T0	5- 19		EXECUTIVE MODE
B0	2A1A06J03B-04			
B1	2A1A06J03B-03			ADDR BIT 06 TO INTERNAL STOR A
B2	2A2B3-M1	5- 33		NOT BIT 08 FROM PF QUADRANT 0
B3	2A2A8-C0	5- 9		NOT STOR ADDR BIT 06 TO PAR, GENERATOR AND IND DRIVER
C0	2A1A06J05B-04			
C1	2A1A06J05B-03			ADDR BIT 06 TO INTERNAL STOR B
C2	2A2B3-K0	5- 31		NOT BIT 12 FROM PF QUADRANT 0
C3	2A2A5-G2	5- 3		ROP + STOR COMPARE BIT 17

5-21

MC 2A2H6 SD S-1
H3 2H2A & F2

NOTES:
1. BC ADDR HOLDING REGISTER
2. INST ADDR HOLD REGISTER
3. MAIN CONT OPER ADDR HOLDING REGISTER
4. BC ADDR RELOC HOLD REGISTER
5. MAIN CONT INST ADDR RELOC HOLD. REGISTER
6. MAIN CONT OPER ADDR RELOC HOLD. REGISTER

S 1,2,3,5
S4,9→14→S0,14

STORAGE ADDRESS REGISTER BITS 06 AND 17, ADDR HOLDING REG BIT 17, ILL.WR SENSED, AND RD/WR PF ADDR BIT 06

DEVELOPMENT DIVISION

LOC: 2A2B4 PART NO. 185236 SER. 000

PRODUCT

SIZE C | DRAWING NO. 60181000

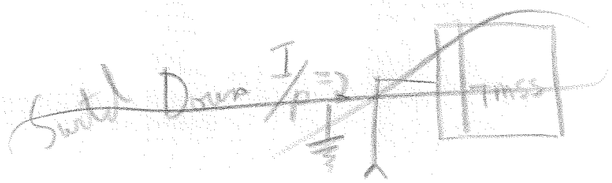
SHEET | PAGE 5-21

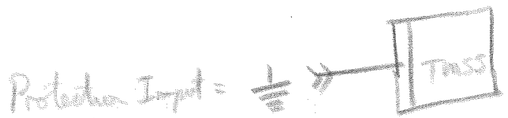
2-47A

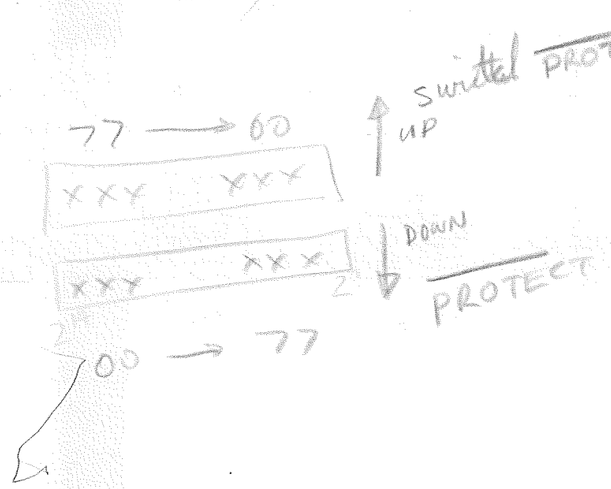
2-47B

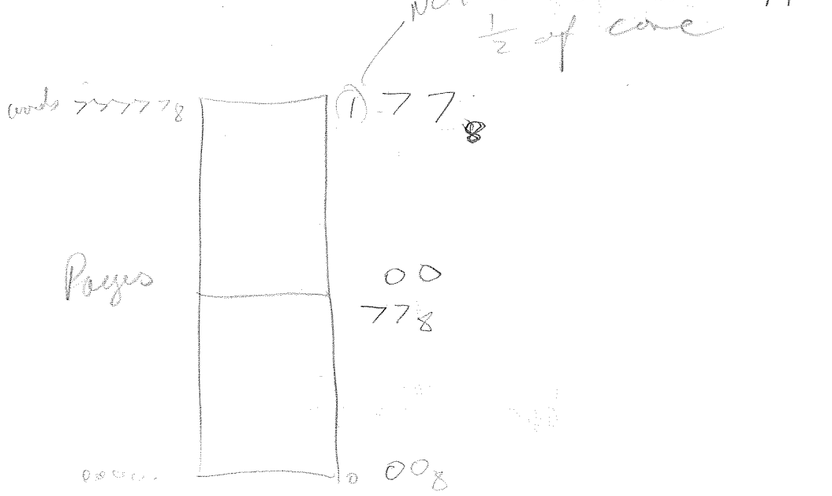
D0	2A2B9-C1	5- 23	2A2B9-AK	NOT ADDR BIT 10 TO STOR PROT
D1	2A2A4-E0	5- 7		NOT PAGE FILE ADDRESS BIT 06
D2	2A2A5-E3	5- 3		BLOCK CONTROL COMPARE BIT 17
D3	2A2A5-F2	5- 3		RNI + RADR COMPARE BIT 17
E0	2A1A06J06R-04			
	1A4A06P01R-04			
	1A0R4-M3	2- 69		
E1	2A1A06J06R-03			S6(S BUS) BIT 06
	1A4A06P01R-03			
	1A0B4-M2	2- 69		
E2	2A2R3-Q0	5- 33		NOT BIT 11 FROM PF QUADRANT 0
E3	2A2R2-Q0	5- 39		NOT BIT 11 FROM PF QUADRANT 1
F0	2A1A6-B0	6- 49		RC S BUS BIT 06 TO PAGE FILE
F1	2A1A6-B1	6- 49		
F2	2A1A8-S1	6- 55		RC S BUS BIT 17 TO PAGE FILE
F3	2A1A8-S0	6- 55		
G1	2A2B9-B0	5- 23		ADDR BIT 10 TO STOR PROTECT
G2	2A1A06P03D-05			C4 FAN IN BIT 2(S BUS BIT 17)
	1A4A06J20D-05			
	1C0A3-S0	2- 39		
G3	2A1A06P03D-06			
	1A4A06J20D-06			
	1C0A3-S1	2- 39		
H1	2A2B8-M0	5- 13		NOT ADDRESS BIT 10
H2	2A2A8-S0	5- 9		ADDR, BITS 00, 02, AND 04 SET
H3	2A2A9-S0	5- 11		ADDR, BITS 01, 03, AND 05 SET
I0	2A2B9-A0	5- 23		ADDR BIT 09 TO STOR PROTECT
I1	2A2B9-B1	5- 23	2A2B9-AE	NOT ADDR BIT 09 TO STOR PROT
I2	2A2A9-F1	5- 11		NOT STOR ADDR BIT 17 TO PAR. GENERATOR AND IND DRIVER
I3	2A2A7-M2	5- 5		BLOCK CONTROL PRIORITY
J0	2A2A6-K1	5- 1		NOT BLOCK CONTROL ADDR COMP EN
J1	2A2A6-N2	5- 1		NOT ADDRESS BIT 09
J2	2A2B8-N0	5- 13		NOT ADDRESS BIT 17
J3	2A2B5-X1	5- 19		SAVE NEW (S) REG UNTIL CHANGE
K0	2A2A5-K3	5- 3		NOT BIT 10 FROM PF QUADRANT 0
K1	2A2B3-R1	5- 33		DOUBLE PRECISION FIRST OPERAND
K2	2A2A5-X0	5- 3		NOT BIT 12 FROM PF QUADRANT 1
K3	2A2B2-K0	5- 37		LOAD S REGISTER
	2A2B8-V0	5- 13		
	2A2A6-00	5- 1		
L0	2A2A8-Q0	5- 9		ADDR BIT 08 TO DETECT ILL. WR,
L1	2A2A9-Q0	5- 11		ADDR BIT 07 TO DETECT ILL. WR,
L2	2A2B2-M1	5- 39		NOT BIT 08 FROM PF QUADRANT 1
L3	2A2A5-D2	5- 3		NOT OPERAND REFERENCE
M0	2A2A5-C1	5- 3		AUTO LOAD/AUTO DUMP ADDR, EN,
M1	2A2A6-A3	5- 1		NOT MAIN CONTROL ADDR, COMPARE
M2	2A2B1-M1	5- 45		NOT BIT 08 FROM PF QUADRANT 2
M3	2A2B0-M1	5- 51		NOT BIT 08 FROM PF QUADRANT 3
N0	2A1A06J07B-03			ADDR BIT 06 TO EXTERNAL STOR
	2A1A06J08B-03			
N1	2A1A06J07B-04			
	2A1A06J08B-04			
N2	2A2B1-K0	5- 43		NOT BIT 12 FROM PF QUADRANT 2
N3	2A2B0-K0	5- 49		NOT BIT 12 FROM PF QUADRANT 3
Q2	2A2A04J03B-01			STOR ADDR BIT 17 TO INDICATOR
Q3	2A2A04J03R-02			
P0	2A2A5-H0	5- 3		WRITE INTO STORAGE
P1	2A2B8-J2	5- 13		PAGE FILE OUT BITS 0 TO 7 = 0
P2	2A2B1-Q0	5- 45		NOT BIT 11 FROM PF QUADRANT 2
P3	2A2A5-T3	5- 3		READ/WRITE PAGE FILE
Q0	2A2A04J02K-01			BIT 09 OUT OF PF TO INDICATOR
Q1	2A2A04J02K-02			
Q2	2A2B8-E3	5- 13		NOT PAGE 0 TO ENABLE PAGE
Q3	2A2B0-Q0	5- 51		FILE QUADRANT BIT 8
R0	2A2B2-R0	5- 39		NOT BIT 11 FROM PF QUADRANT 3
R1	2A2B3-R0	5- 33		NOT BIT 09 FROM PF QUADRANT 1
R2	2A1A06J03D-06			NOT BIT 09 FROM PF QUADRANT 0
R3	2A1A06J03D-05			
S0	2A2B0-R0	5- 51		ADDR BIT 17 TO INTERNAL STOR A
S1	2A2B1-R0	5- 45		NOT BIT 09 FROM PF QUADRANT 3
S2	2B2A7-R1	5- 61		NOT BIT 09 FROM PF QUADRANT 2
S3	2B2A7-R0	5- 61		BIT 08 OUT OF PF TO DB XMTR
T0	2B2A6-H2	5- 63		
T1	2B2A6-H3	5- 63		BIT 09 OUT OF PF TO DB XMTR
T2	2A2A04J02J-02			
T3	2A2A04J02J-01			BIT 08 OUT OF PF TO INDICATOR
U0	2A2A5-P3	5- 3		ENABLE PAGE FILE TO DATA BUS
U1	2A2B2-R1	5- 39		NOT BIT 10 FROM PF QUADRANT 1
U2	2B2A6-R1	5- 63		BIT 11 OUT OF PF TO DB XMTR
U3	2B2A6-R0	5- 63		
V0	2A2B0-R1	5- 51		NOT BIT 10 FROM PF QUADRANT 3
V1	2A2B1-R1	5- 45		NOT BIT 10 FROM PF QUADRANT 2
V2	2A2A04J02M-01			BIT 11 OUT OF PF TO INDICATOR
V3	2A2A04J02M-02			
W0	2B2A6-G3	5- 63		BIT 10 OUT OF PF TO DB XMTR
W1	2B2A6-G2	5- 63		
W2	2A1A06J07D-05			ADDR BIT 17 TO EXTERNAL STOR
	2A1A06J08D-05			
W3	2A1A06J07D-06			
	2A1A06J08D-06			
X0	2A2A04J02L-02			
X1	2A2A04J02L-01			
X2	2A1A06J05D-06			BIT 10 OUT OF PF TO INDICATOR
X3	2A1A06J05D-05			ADDR BIT 17 TO INTERNAL STOR B

see above


Switch Down I/p
THIS


Protection Input =
THIS


77 → 00
Switch PROTECT
UP
DOWN
PROTECT
00 → 77


not used all 1s suppre
1/2 of cone
Pages
00
778
00

F3

G3

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A2B4-I0	5-21		ADDR BIT 09 TO STOR PROTECT
A3	2A2B7-H0	5-15		ADDR BIT 11 TO STOR PROTECT
B0	2A2B4-G1	5-21		ADDR BIT 10 TO STOR PROTECT
B1	2A2B4-I1	5-21	2A2B9-AE	NOT ADDR BIT 09 TO STOR PROT
B3	2A2B7-X0	5-15		ADDR BIT 12 TO STOR PROTECT
C0	2A2A04J02B-03			LWR STOR PROTECT BIT 09 SW = 1
C1	2A2B4-D0	5-21	2A2B9-AK	NOT ADDR BIT 10 TO STOR PROT
C3	2A2A04J02F-03			LWR STOR PROTECT BIT 11 SW = 1
D0	2A2A04J01B-03			UP, STOR PROTECT BIT 09 SW = 1
D1	2A2A04J02D-03			LWR STOR PROTECT BIT 10 SW = 1
D3	2A2A04J01F-03			UP, STOR PROTECT BIT 11 SW = 1
E0	2A2A9-M2	5-11		ADDR PAR, GENERATE
E1	2A2A04J01D-03			UP, STOR PROTECT BIT 10 SW = 1
F0	2A2A8-M2	5-9		ADDR PAR, GENERATE
F1	2A2A9-M3	5-11		ADDR PAR, GENERATE
G0	2A2A8-M3	5-9		ADDR PAR, GENERATE
G1	~~2A2A7-M3~~	~~5-~~	2B2A5	MASTER CLEAR PAGE FILE
H0	2A1A06J05F-05		Page S-73	ADDR LWR PAR BIT TO INT STOR B
H1	2A1A06J05F-06			
H3	2A2A04J01H-03			UP, STOR PROTECT BIT 12 SW = 1
I0	2A2A04J01V-01			ADDR LWR PAR, BIT TO INDICATOR
I1	2A2A04J01V-02			
I3	2A2A04J02H-03			LWR STOR PROTECT BIT 12 SW = 1
J0	2A1A06J03F-03			MASTER CLEAR INTERNAL STOR A
J1	2A1A06J03F-04			
K3	2A2B6-H0	5-17		ADDR BIT 13 TO STOR PROTECT
L0	2A1A06J03F-05			ADDR LWR PAR BIT TO INT STOR A
L1	2A1A06J03F-06			
M0	2R2B9-U2	5-75		
M1	2R2B9-U3	5-75		STORAGE NO RESPONSE
M3	2A2A5-B0	5-3	2A2A5-AB	STOR PROTECT COMP TO ILL, WR
N0	2A1A06J07F-05			ADDR LWR PAR, BIT TO EXT STOR
	2A1A06J08F-05			
N1	2A1A06J07F-06			
	2A1A06J08F-06			
N3	2A2A04J02K-03			LWR STOR PROTECT BIT 13 SW = 1
O0	2A1A06J05F-03			MASTER CLEAR INTERNAL STOR B
O1	2A1A06J05F-04			
O3	2A2A04J01K-03			UP, STOR PROTECT BIT 13 SW = 1
P0	2A1A06J07F-03			MASTER CLEAR EXTERNAL STORAGE
	2A1A06J08F-03			
P1	2A1A06J07F-04			
	2A1A06J08F-04			
P3	2A2B6-X0	5-17		ADDR BIT 14 TO STOR PROTECT
Q0	2A1A06P05F-04			
	1A4A06J14F-04			
	1R0B1-F2	2-9		
Q1	2A1A06P05F-03			STORAGE NO RESPONSE
	1A4A06J14F-03			
	1R0B1-F3	2-9		
R0	2A2A7-W3	5-5	2A2B9-AP	PSEUDO REPLY DELAYED
S3	2A2A04J01M-03			UP, STOR PROTECT BIT 14 SW = 1
T0	2A1A06J07F-08			
	2A1A06J08F-08			
T1	2A1A06J07F-07			EXT STOR NO RESPONSE
	2A1A06J08F-07			
T3	2A2A04J02H-03			LWR STOR PROTECT BIT 14 SW = 1
U0	2A2A5-G1	5-3		BUS REQUEST
V0	2A2A7-G3	5-5	2A2A7-RA	INITIATE PSEUDO STORAGE REPLY
V1	2A2A5-H1	5-3	2A2B9-AV	RD/WR PAGE FILE ADDR REPLY
V2	2B1B1-K0	6-9		SWITCH, POWER ON MASTER CLEAR
	2A1A06J16D-07			
V3	2A2A04J02S-03			SWITCH, TEST MODE
W0	2A1A06J03F-07			INTERNAL STOR A NO RESPONSE
W1	2A1A06J03F-08			
W2	2A1A06P09E-09			SWITCH, TEST MODE
	1A4A06J12E-09			
	1C0B2-Q0	2-51		
W3	2A2A7-C0	5-5		NOT STOR ADDR REPL
X0	2A1A06J05F-07			INTERNAL STOR B NO RESPONSE
X1	2A1A06J05F-08			
X2	2A1A06J15C-08			STOR ADDR REPLY
	2A1A06J16C-08			
X3	2A1A06J15C-07			
	2A1A06J16C-07			

LOWER LIMIT COMPARATOR

UPPER LIMIT COMPARATOR

PARITY GENERATOR

SP14S0 SP14S1 SMP14 SP13S0 SP13S1 SMP13 SP12S0 SP12S1 SMP12 SP11S0 SP11S1 SMP11 SP10S0 SP10S1 SMP10 SP09S0 SP09S1 SMP09 SMP09

SPE0 SPE1 SPE2 SPE3

EXTSLP INSLPA INSLPB SLPL

SPCPR (ILLWrite) TSTMØD PØHCLR MCLPLC Page S-73 G3 F3

CLEXTM CLINMA CLINMB TERM TE2 A12 TERM TE2 B32 TERM TE2 B12

EXTDNR INDNRA INDNRB STALT STA

NØRESP MNØRES PSEUDØ

BUSRQA PUDØDL RWPFAR

385 NSEC ~2.5μSEC 17.5 NSEC

NO RESPONSE

Read/Write Page File only

Read or Write Page File.
Reply IN 2.9μS. (from Memory)

CONTROL DATA
DEVELOPMENT DIVISION

STORAGE PROTECT, NO RESPONSE, AND PARITY GENERATOR

LOC:2A2B9 PART NO.186433 SER,000

PRODUCT

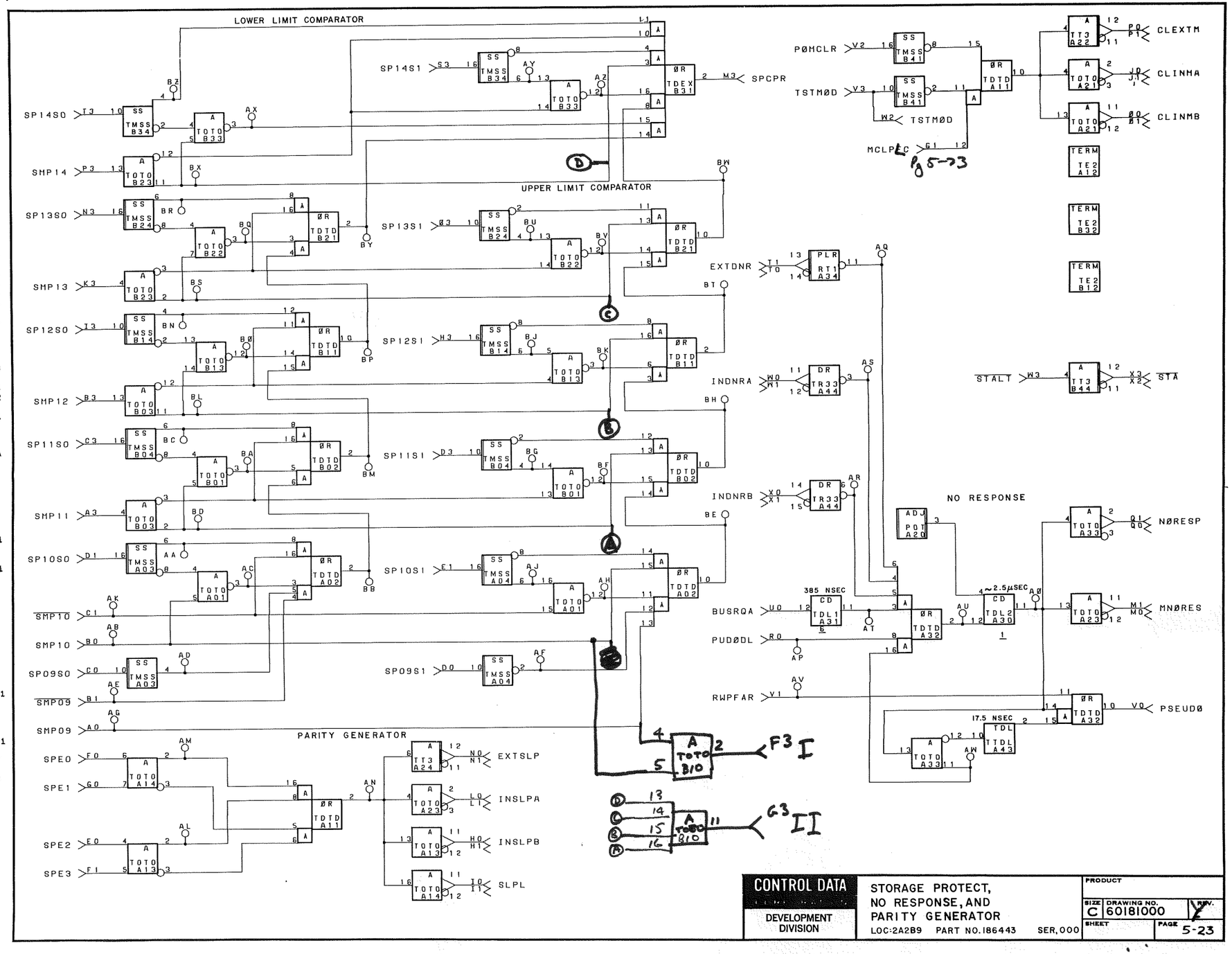
SIZE C DRAWING NO. 60181000

SHEET PAGE 5-23

Next Page is a Rev. Y

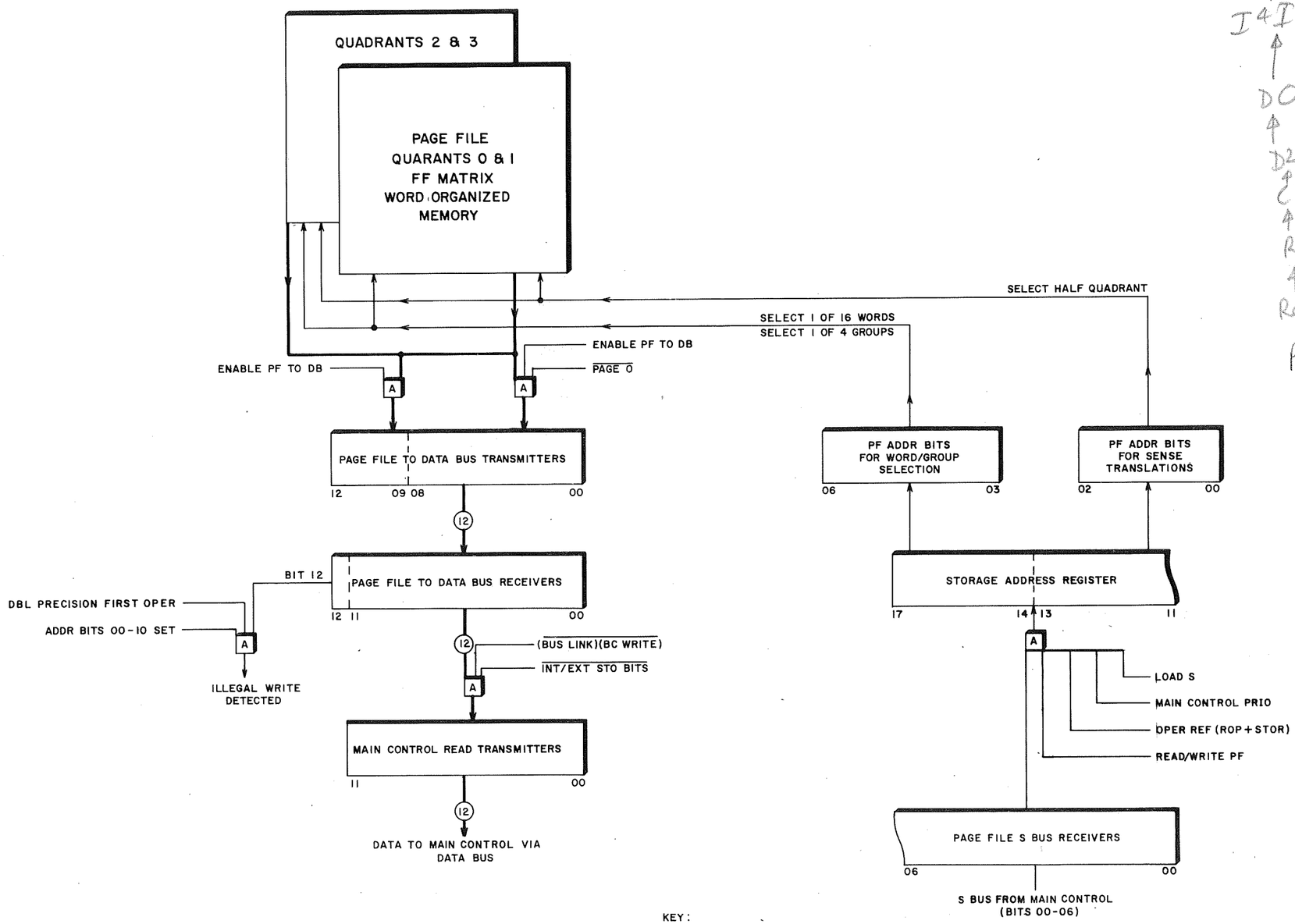
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A2R4-I0	5- 21		ADDR BIT 09 TO STOR PROTECT
A3	2A2R7-H0	5- 15		ADDR BIT 11 TO STOR PROTECT
B0	2A2R4-G1	5- 21		ADDR BIT 10 TO STOR PROTECT
B1	2A2R4-I1	5- 21	2A2B9-AE	NOT ADDR BIT 09 TO STOR PROT
B3	2A2R7-X0	5- 15		ADDR BIT 12 TO STOR PROTECT
C0	2A2A04J02R-03			LWR STOR PROTECT BIT 09 SW = 1
C1	2A2R4-D0	5- 21	2A2B9-AK	NOT ADDR BIT 10 TO STOR PROT
C3	2A2A04J02F-03			LWR STOR PROTECT BIT 11 SW = 1
D0	2A2A04J01R-03			UP, STOR PROTECT BIT 09 SW = 1
D1	2A2A04J02D-03			LWR STOR PROTECT BIT 10 SW = 1
D3	2A2A04J01F-03			UP, STOR PROTECT BIT 11 SW = 1
E0	2A2A9-M2	5- 11		ADDR PAR, GENERATE
E1	2A2A04J01D-03			UP, STOR PROTECT BIT 10 SW = 1
F0	2A2A8-M2	5- 9		ADDR PAR, GENERATE
F1	2A2A9-M3	5- 11		ADDR PAR, GENERATE
G0	2A2A8-M3	5- 9		ADDR PAR, GENERATE
G1	2A2A7-H3	5- 5		MASTER CLEAR PAGE FILE
H0	2A1A06J05F-05			ADDR LWR PAR BIT TO INT STOR B
H1	2A1A06J05F-06			
H3	2A2A04J01H-03			UP, STOR PROTECT BIT 12 SW = 1
I0	2A2A04J01V-01			ADDR LWR PAR, BIT TO INDICATOR
I1	2A2A04J01V-02			
I3	2A2A04J02H-03			LWR STOR PROTECT BIT 12 SW = 1
J0	2A1A06J03F-03			MASTER CLEAR INTERNAL STOR A
J1	2A1A06J03F-04			
K3	2A2R6-H0	5- 17		ADDR BIT 13 TO STOR PROTECT
L0	2A1A06J03F-05			ADDR LWR PAR BIT TO INT STOR A
L1	2A1A06J03F-06			
M0	2R2B9-U2	5- 75		
M1	2R2B9-U3	5- 75		STORAGE NO RESPONSE
M3	2A2A5-B0	5- 3	2A2A5-AR	STOR PROTECT COMP TO ILL. WR
N0	2A1A06J07F-05			ADDR LWR PAR, BIT TO EXT STOR
	2A1A06J08F-05			
N1	2A1A06J07F-06			
	2A1A06J08F-06			
N3	2A2A04J02K-03			LWR STOR PROTECT BIT 13 SW = 1
O0	2A1A06J05F-03			MASTER CLEAR INTERNAL STOR B
O1	2A1A06J05F-04			
O3	2A2A04J01K-03			UP, STOR PROTECT BIT 13 SW = 1
P0	2A1A06J07F-03			MASTER CLEAR EXTERNAL STORAGE
	2A1A06J08F-03			
P1	2A1A06J07F-04			
	2A1A06J08F-04			
P3	2A2R6-X0	5- 17		ADDR BIT 14 TO STOR PROTECT
Q0	2A1A06P05F-04			
	1A4A06J14F-04			
	1R0R1-F2	2- 9		
Q1	2A1A06P05F-03			STORAGE NO RESPONSE
	1A4A06J14F-03			
	1R0R1-F3	2- 9		
R0	2A2A7-W3	5- 5	2A2B9-AP	PSEUDO REPLY DELAYED
S3	2A2A04J01M-03			UP, STOR PROTECT BIT 14 SW = 1
T0	2A1A06J07F-08			
	2A1A06J08F-08			
T1	2A1A06J07F-07			EXT STOR NO RESPONSE
	2A1A06J08F-07			
T3	2A2A04J02M-03			LWR STOR PROTECT BIT 14 SW = 1
U0	2A2A5-G1	5- 3		BUS REQUEST
V0	2A2A7-G3	5- 5	2A2A7-BA	INITIATE PSEUDO STORAGE REPLY
V1	2A2A5-H1	5- 3	2A2B9-AV	RD/WR PAGE FILE ADDR REPLY
V2	2R1B1-K0	6- 9		SWITCH, POWER ON MASTER CLEAR
	2A1A06J16D-07			
V3	2A2A04J02S-03			SWITCH, TEST MODE
W0	2A1A06J03F-07			INTERNAL STOR A NO RESPONSE
W1	2A1A06J03F-08			
W2	2A1A06P09F-09			SWITCH, TEST MODE
	1A4AD6J12E-09			
	1C0B2-00	2-51		
W3	2A2A7-C0	5- 5		NOT STOR ADDR REPL
X0	2A1A06J05F-07			INTERNAL STOR A NO RESPONSE
X1	2A1A06J05F-08			
X2	2A1A06J15C-08			STOR ADDR REPLY
	2A1A06J16C-08			
X3	2A1A06J15C-07			
	2A1A06J16C-07			

F3 2A2A8-I2 5-9
G3 2A2A8-J3 5-9



CONTROL DATA	STORAGE PROTECT, NO RESPONSE, AND PARITY GENERATOR	PRODUCT
DEVELOPMENT DIVISION	LOC-2A2B9 PART NO.186443 SER,000	SIZE C DRAWING NO. 60181000 REV. Y
		SHEET PAGE 5-23

Revious has correction and updated. same as previous 51



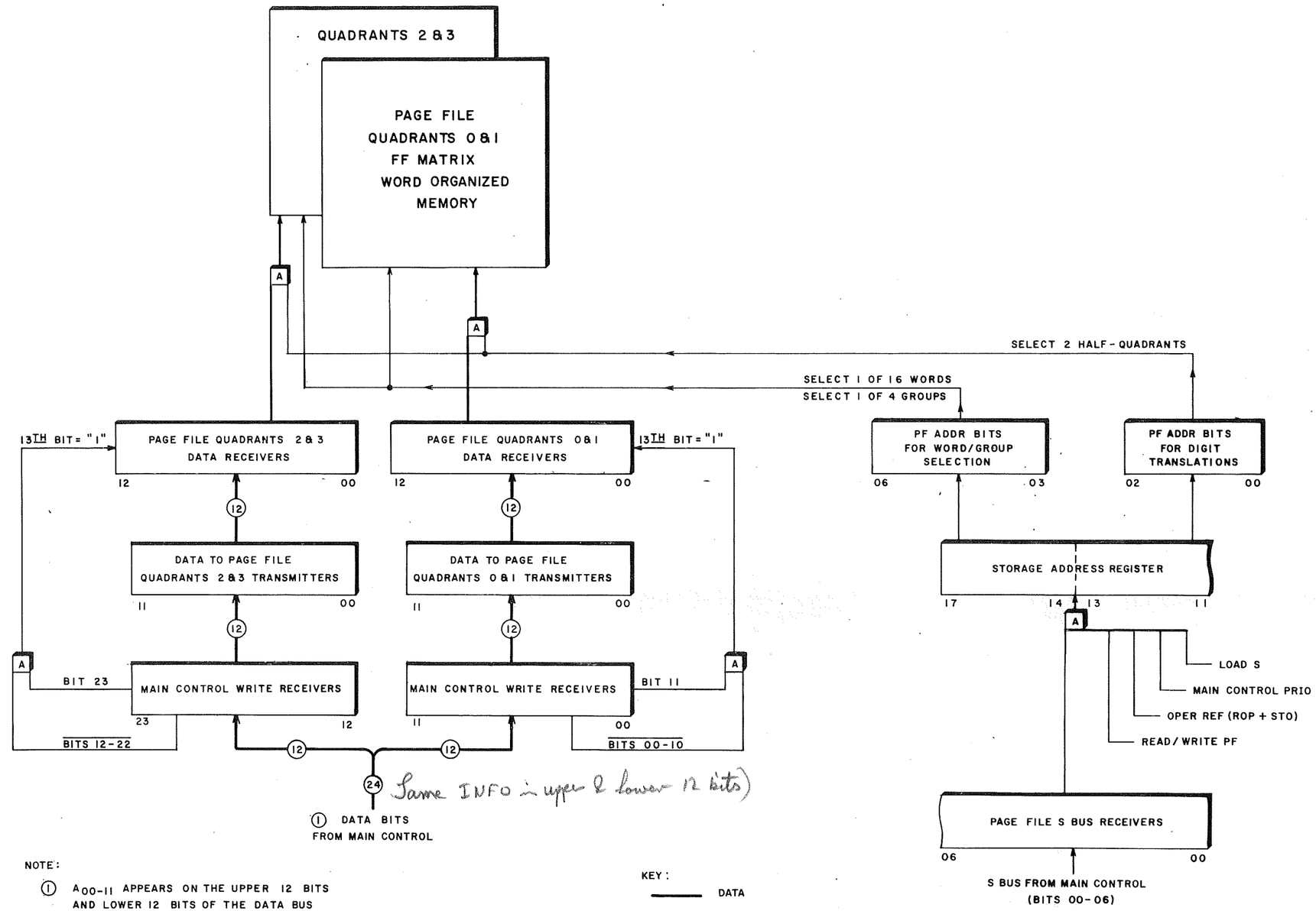
CONTROL DATA
DEVELOPMENT DIVISION

TITLE
BLOCK DIAGRAM
PF → (A 00-11)

PRODUCT

SIZE C | DRAWING NO. 60181000 | REV.

SHEET | PAGE 5-25



NOTE:

(1) A_{00-11} APPEARS ON THE UPPER 12 BITS AND LOWER 12 BITS OF THE DATA BUS DURING $(A_{00-11}) \rightarrow$ PF.

KEY:

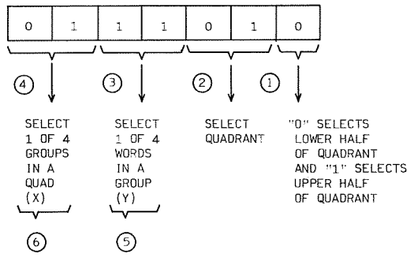
- DATA
- CONTROL
- (12) NUMBER OF BITS

CONTROL DATA DEVELOPMENT DIVISION	TITLE BLOCK DIAGRAM $(A_{00-11}) \rightarrow$ PF	PRODUCT	
		SIZE C	DRAWING NO. 60181000
		REV.	
		SHEET	PAGE 5-27

READ

ON A READ OPERATION, THE DECODED PAGE ADDRESS BITS (0-2) TURN ON THE SENSE LINES WITHIN THE UPPER OR LOWER HALF OF THE SELECTED QUADRANT FOR A 14-BIT READ (12-BIT INDEX, 1-BIT LOOK AHEAD, AND 1-BIT SPARE).

TYPICAL ADDRESS



SENSE SELECT TRANSLATIONS

1. 0= LOWER HALF OF QUADRANT
2. 01 = QUADRANT 1
3. Y = 11 = WORD 3
4. X = 01 = GROUP 1
5. BITS 3 & 4 = (Y FOR QUADRANTS 0 & 1) AND (X FOR QUADRANTS 2 & 3)
6. BITS 5 & 6 = (X FOR QUADRANTS 0 & 1) AND (Y FOR QUADRANTS 2 & 3)

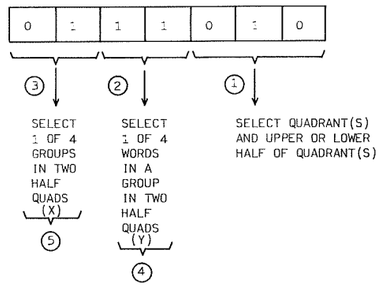
WRITE

ON A WRITE OPERATION, THE DECODED PAGE ADDRESS BITS (0-2) TURN ON THE DIGIT LINES IN ONE OF TWO WAYS: (1) IF THE UPPER HALF OF A QUADRANT IS SELECTED, A 12-BIT WRITE OCCURS IN THAT HALF AND A 2-BIT WRITE OCCURS IN THE LOWER HALF, OR (2) IF THE LOWER HALF OF A QUADRANT IS SELECTED, A 12-BIT WRITE OCCURS IN THAT HALF AND A 2-BIT WRITE OCCURS IN THE UPPER HALF OF THE PRECEDING QUADRANT.

THE PURPOSE OF HAVING 2 DISTINCTIVE WRITE OPERATIONS IS TO ALLOW A LOOK AHEAD BIT TO BE WRITTEN INTO THE 13TH BIT POSITION OF EACH WORD INDEX. IF A "1" IS WRITTEN INTO THE 13TH BIT, THE FOLLOWING WORD INDEX CONTAINS 4000, AND IF "0" IS WRITTEN INTO THE 13TH BIT, THE FOLLOWING WORD INDEX CONTAINS A QUANTITY OTHER THAN 4000. A WORD INDEX OF 4000 DEFINES AN UNADDRESSABLE PAGE WHERE READING AND WRITING ARE PROHIBITED.

IF THE FIRST OPERAND FOR A DOUBLE PRECISION INSTRUCTION IS TO BE READ FROM THE LAST AVAILABLE STORAGE LOCATION SPECIFIED BY PL, OR IF FROM THE LAST STORAGE LOCATION WHEN PL SPECIFIES A FULL PAGE AND THE NEXT INDEX TO BE USED CONTAINS 4000, THE DOUBLE PRECISION INSTRUCTION WILL NOT BE PROCESSED. THE 13TH BIT OF THE WORD INDEX OF THE FIRST OPERAND CONTAINS A "1" LOOK AHEAD INDICATOR FOR TERMINATING THE DOUBLE PRECISION IN ADVANCE, THUS AVOIDING PARTIAL COMPLETION OF THE INSTRUCTION.

TYPICAL ADDRESS



* DIGIT SELECT TRANSLATIONS

1. 010 = QUADRANT 1 LOWER AND QUADRANT 0 UPPER
2. Y = 11 = SELECT WORD 3 - QUAD 1 AND SELECT WORD 3 - QUAD 0
3. X = 01 = SELECT GROUP 1 - QUAD 1 AND SELECT GROUP 1 - QUAD 0
4. BITS 3 & 4 = Y FOR QUADRANTS 0 & 1 AND X FOR QUADRANTS 2 & 3
5. BITS 5 & 6 = X FOR QUADRANTS 0 & 1 AND Y FOR QUADRANTS 2 & 3

* THE PAGE ADDRESS BITS ARE ALWAYS DECODED FOR TWO HALF QUADRANTS ON A WRITE OPERATION

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE
READ/WRITE
PAGE ADDRESS BITS

PRODUCT

SIZE	DRAWING NO.	REV.
C	60181000	A

SHEET

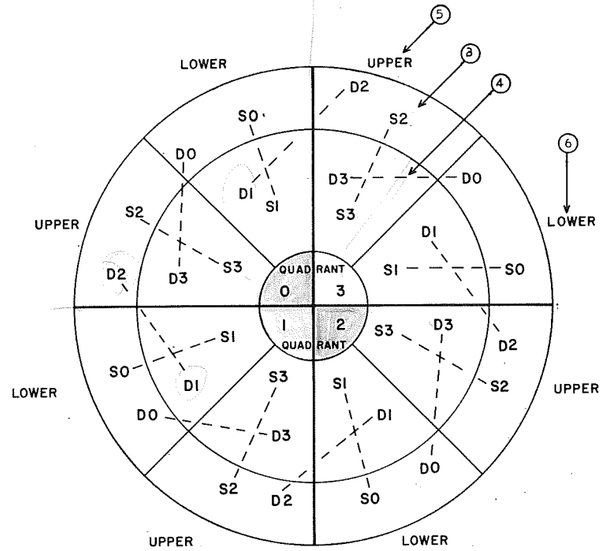
PAGE 5-28

CIRCLE DIAGRAM

1. D0 - D3 = DIGIT LINES (WRITE)
2. S0 - S3 = SENSE LINES (READ)
3. 2 BITS $(2^{13} \geq 2^{12})$ $(2^{12} = LA)$
4. 12 BITS
5. UPPER HALF OF QUADRANT
6. LOWER HALF OF QUADRANT
7. ALL QUADRANTS ARE IDENTICALLY STRUCTURED.
8. IT IS IMPORTANT TO NOTE THAT THE 14-BIT WORD INDEX STORAGE IS DIVIDED INTO A 12-BIT PORTION AND A 2-BIT PORTION, EACH WITH ITS OWN SENSE LINES FOR READING AND DIGIT LINES FOR WRITING.

READ

IF A READ OPERATION OCCURS, WITH QUADRANT 3 UPPER SELECTED, SENSE LINE S3 IS TURNED ON FOR A 12-BIT READ AND SENSE LINE S2 IS TURNED ON FOR A 2-BIT READ. THE CONTROLS FOR THE SENSE LINES ARE SEPARATE YET SIMULTANEOUSLY OPERATING WITHIN THE SAME HALF QUADRANT. THE SENSE LINES READ A FULL 14-BIT WORD INDEX.



WRITE

IF A WRITE OPERATION OCCURS, WITH QUADRANT 3 UPPER AND QUADRANT 3 LOWER SELECTED, DIGIT LINE D3 IS TURNED ON FOR A 12-BIT WRITE AND DIGIT LINE D0 IS TURNED ON FOR A 2-BIT WRITE. THE CONTROLS FOR THE DIGIT LINES ARE SEPARATE YET SIMULTANEOUSLY OPERATING WITHIN TWO HALF QUADRANTS BECAUSE THE DIGIT LINES MUST WRITE A "1" IN THE 13TH BIT POSITION OF THE WORD INDEX PRECEDING A WORD INDEX CONTAINING 4000 AND THEY MUST WRITE A "0" FOR ALL OTHER QUANTITIES. THE 13TH BIT, A LOOK AHEAD BIT, IS USED ON SPECIFIC DOUBLE PRECISION OPERATIONS TO INDICATE A TOTALLY EXCLUDED PAGE IN STORAGE WHERE READING AND WRITING ARE PROHIBITED. SEE THE TYPICAL ADDRESS AND WRITE ON PAGE _____ FOR A MORE DETAILED EXPLANATION OF THE LOOK AHEAD FEATURE.

NOTE THE DISTINCTIVE DIFFERENCES BETWEEN THE READ AND WRITE SENSE/DIGIT LINES.

PAGE ADDRESS BITS (3) FOR_

QUADRANT 0

(4) LOWER Y	(X)	Quad	Sect	(5) UPPER Y	X	Quad	Sect
(1) 0 0 0 0	0 0	0	0	0 0 0 0	0 0	0	1
0 0 0 1	0 0	0	0	0 0 0 1	0 0	0	1
0 0 1 0	0 0	0	0	0 0 1 0	0 0	0	1
0 0 1 1	0 0	0	0	0 0 1 1	0 0	0	1
0 1 0 0	0 0	0	0	0 1 0 0	0 0	0	1
0 1 0 1	0 0	0	0	0 1 0 1	0 0	0	1
0 1 1 0	0 0	0	0	0 1 1 0	0 0	0	1
0 1 1 1	0 0	0	0	0 1 1 1	0 0	0	1
1 0 0 0	0 0	0	0	1 0 0 0	0 0	0	1
1 0 0 1	0 0	0	0	1 0 0 1	0 0	0	1
1 0 1 0	0 0	0	0	1 0 1 0	0 0	0	1
1 0 1 1	0 0	0	0	1 0 1 1	0 0	0	1
1 1 0 0	0 0	0	0	1 1 0 0	0 0	0	1
1 1 0 1	0 0	0	0	1 1 0 1	0 0	0	1
1 1 1 0	0 0	0	0	1 1 1 0	0 0	0	1
1 1 1 1	0 0	0	0	1 1 1 1	0 0	0	1

2A 2A3 B3

QUADRANT 1

LOWER								UPPER							
0	0	0	0	0	1	0		0	0	0	0	0	1	1	
0	0	0	1	0	1	0		0	0	0	1	0	1	1	
0	0	1	0	0	1	0		0	0	1	0	0	1	1	
0	0	1	1	0	1	0		0	0	1	1	0	1	1	
0	1	0	0	0	1	0		0	1	0	0	0	1	1	
0	1	0	1	0	1	0		0	1	0	1	0	1	1	
0	1	1	0	0	1	0		0	1	1	0	0	1	1	
0	1	1	1	0	1	0		0	1	1	1	0	1	1	
1	0	0	0	0	1	0		1	0	0	0	0	1	1	
1	0	0	1	0	1	0		1	0	0	1	0	1	1	
1	0	1	0	0	1	0		1	0	1	0	0	1	1	
1	0	1	1	0	1	0		1	0	1	1	0	1	1	
1	1	0	0	0	1	0		1	1	0	0	0	1	1	
1	1	0	1	0	1	0		1	1	0	1	0	1	1	
1	1	1	0	0	1	0		1	1	1	0	0	1	1	
1	1	1	1	0	1	0		1	1	1	1	0	1	1	

LA

QUADRANT 2

LOWER								UPPER							
0	0	0	0	1	0	0		0	0	0	0	1	0	1	
0	0	0	1	1	0	0		0	0	0	1	1	0	1	
0	0	1	0	1	0	0		0	0	1	0	1	0	1	
0	0	1	1	1	0	0		0	0	1	1	1	0	1	
0	1	0	0	1	0	0		0	1	0	0	1	0	1	
0	1	0	1	1	0	0		0	1	0	1	1	0	1	
0	1	1	0	1	0	0		0	1	1	0	1	0	1	
0	1	1	1	1	0	0		0	1	1	1	1	0	1	
1	0	0	0	1	0	0		1	0	0	0	1	0	1	
1	0	0	1	1	0	0		1	0	0	1	1	0	1	
1	0	1	0	1	0	0		1	0	1	0	1	0	1	
1	0	1	1	1	0	0		1	0	1	1	1	0	1	
1	1	0	0	1	0	0		1	1	0	0	1	0	1	
1	1	0	1	1	0	0		1	1	0	1	1	0	1	
1	1	1	0	1	0	0		1	1	1	0	1	0	1	
1	1	1	1	1	0	0		1	1	1	1	1	0	1	

QUADRANT 3

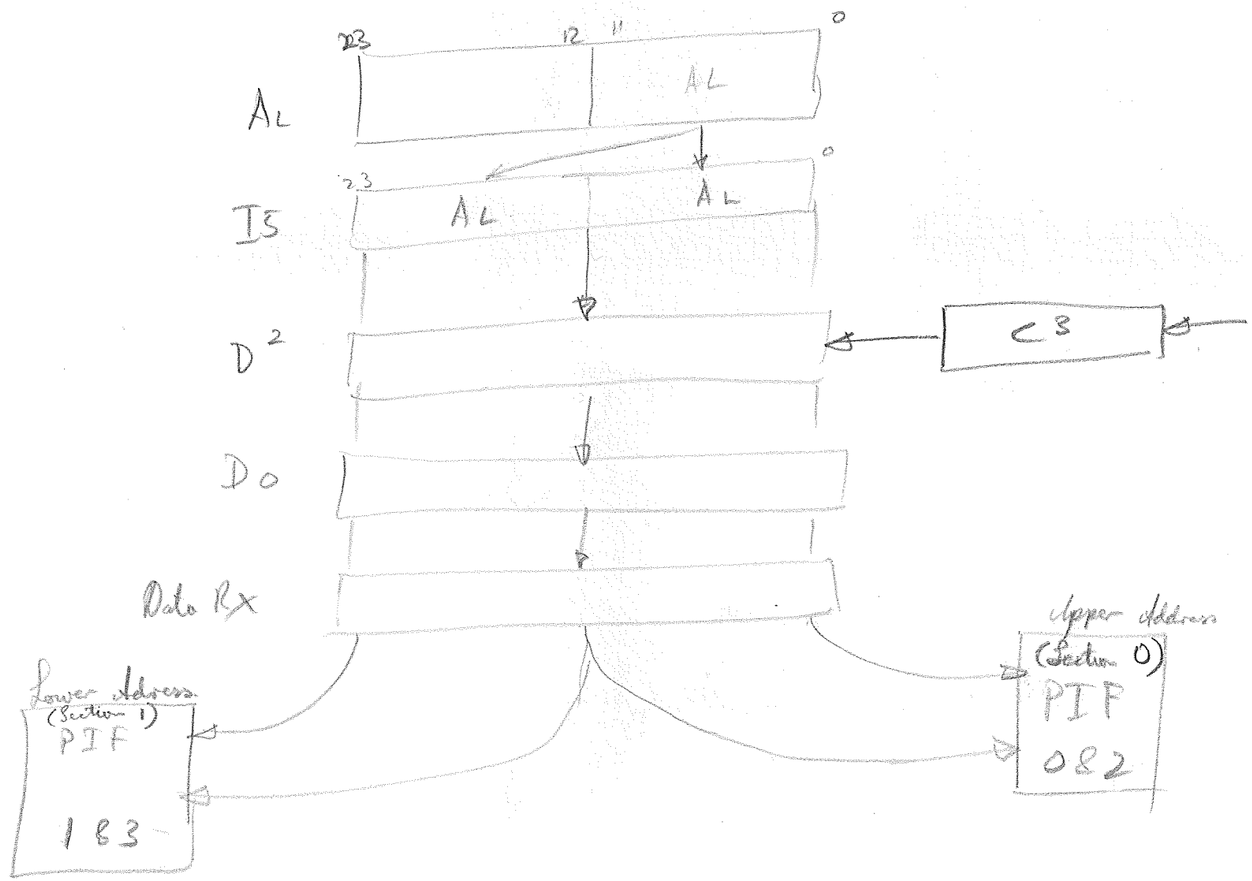
LOWER								UPPER							
0	0	0	0	1	1	0		0	0	0	0	1	1	1	
0	0	0	1	1	1	0		0	0	0	1	1	1	1	
0	0	1	0	1	1	0		0	0	1	0	1	1	1	
0	0	1	1	1	1	0		0	0	1	1	1	1	1	
0	1	0	0	1	1	0		0	1	0	0	1	1	1	
0	1	0	1	1	1	0		0	1	0	1	1	1	1	
0	1	1	0	1	1	0		0	1	1	0	1	1	1	
0	1	1	1	1	1	0		0	1	1	1	1	1	1	
1	0	0	0	1	1	0		1	0	0	0	1	1	1	
1	0	0	1	1	1	0		1	0	0	1	1	1	1	
1	0	1	0	1	1	0		1	0	1	0	1	1	1	
1	0	1	1	1	1	0		1	0	1	1	1	1	1	
1	1	0	0	1	1	0		1	1	0	0	1	1	1	
1	1	0	1	1	1	0		1	1	0	1	1	1	1	
1	1	1	0	1	1	0		1	1	1	0	1	1	1	
1	1	1	1	1	1	0		1	1	1	1	1	1	1	(2)

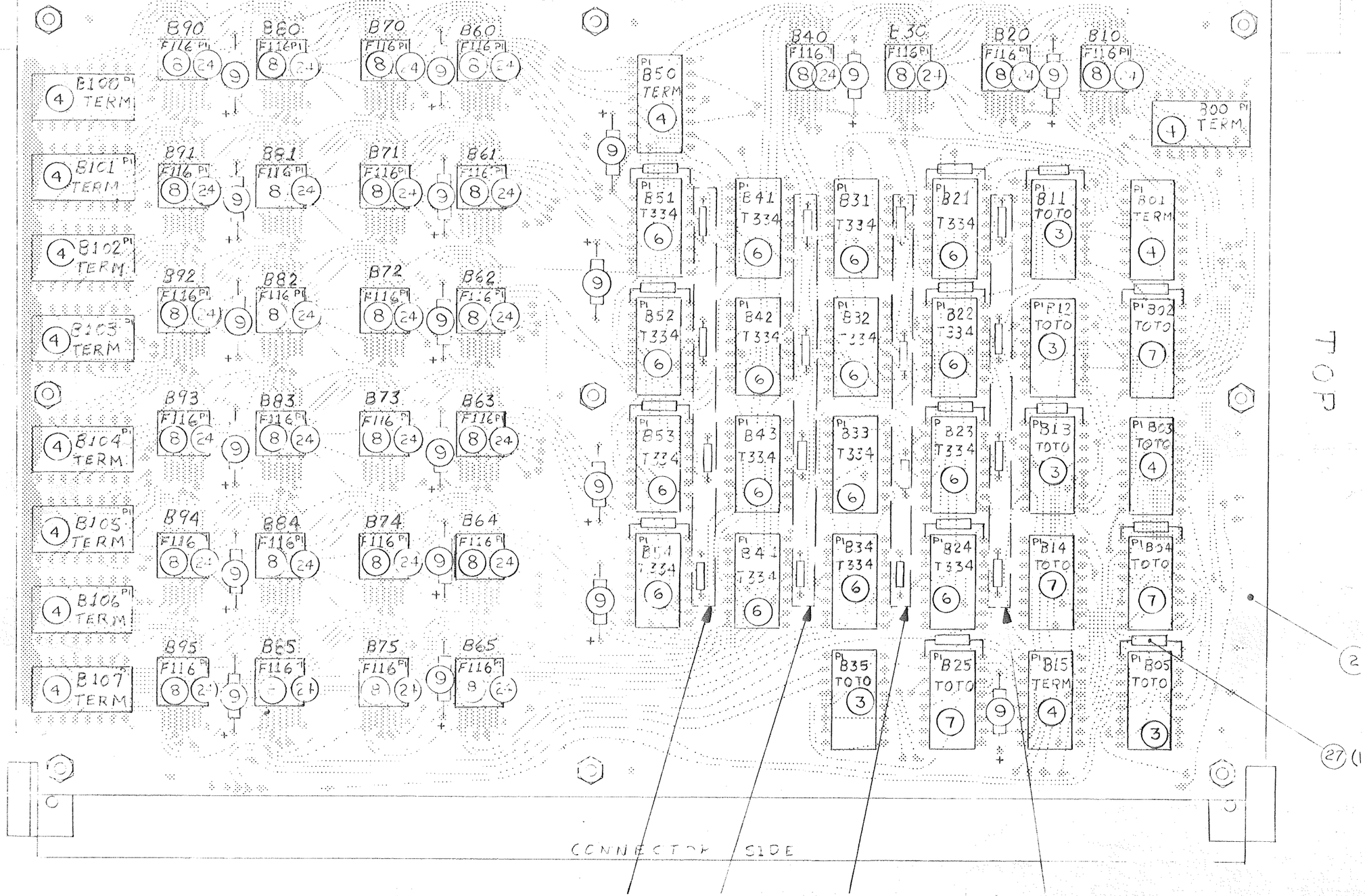
NOTES:

(1) FIRST ADDRESS = PAGE INDEX 0_{10}
(2) LAST ADDRESS = PAGE INDEX 128_{10}
(3) UPPER 7 BITS OF 18-BIT ADDRESS
(4) LOWER = WORDS 1-16
(5) UPPER = WORDS 17-32

CONTROL DATA DEVELOPMENT DIVISION	TITLE PAGE FILE SENSE/DIGIT LINE CONFIGURATION AND ADDRESS STRUCTURE	PRODUCT SIZE C DRAWING NO. 60181000 REV. A SHEET PAGE 5-29	

'A Reg to Page File" Instruction pull (Data)



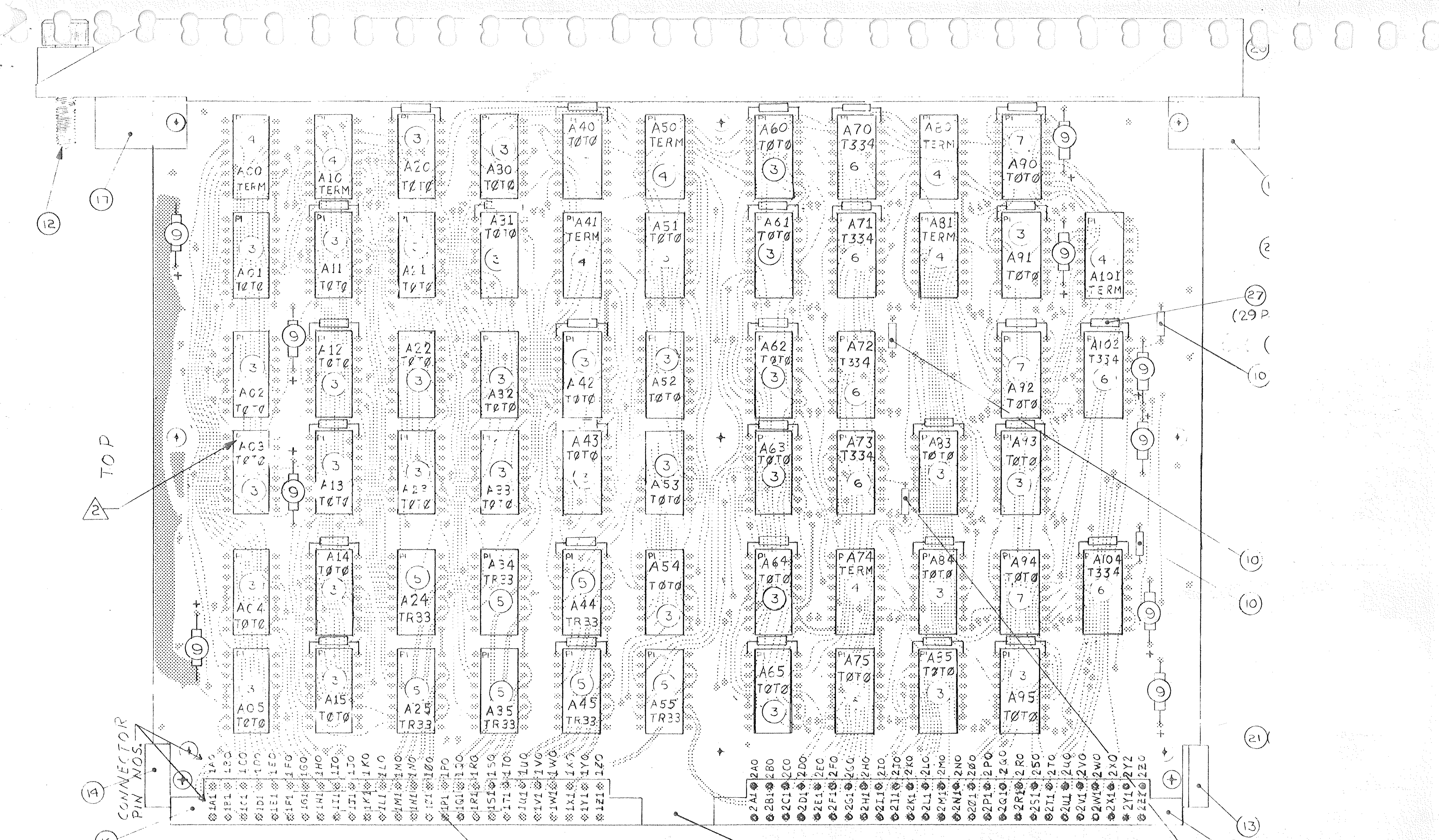


New Scratch Pad Memory Module
Used In Page File & Reg File

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

NEW HSSP
B-BOARD MAP

EQUIPMENT
SIZE C | DRAWING NO. 60289500 | REV W
SHEET | PAGE 18-31



CONTROL DATA

DEVELOPMENT DIVISION

NEW HSSP
A - BOARB MAP

PRODUCT

SIZE C | DRAWING NO. 60289500 | REV. W

SHEET | PAGE

61

1B1	2A2A1-F1	4- 43	QUADRANT 2 Y=0, QUADRANT 0 X=0
	2A2A4-F0	4- 7	
1C1	2A2A1-E1	4- 43	QUADRANT 2 Y=1, QUADRANT 0 X=1
	2A2A4-U0	4- 7	
1D1	2A2A4-F3	4- 7	QUADRANT 2 X=1, QUADRANT 0 Y=1
1E1	2A2A1-C1	4- 43	QUADRANT 2 X=1, QUADRANT 0 Y=1
1F1	2A2A4-C3	4- 7	QUADRANT 2 X=0, QUADRANT 0 Y=0
1G0	2A2A4-H3	4- 7	QUADRANT 2 X=3, QUADRANT 0 Y=3
1G1	2A2A1-H1	4- 43	QUADRANT 2 X=0, QUADRANT 0 Y=0
1H0	2A2A1-K1	4- 43	QUADRANT 2 X=3, QUADRANT 0 Y=3
1I1	2A2A4-J3	4- 7	QUADRANT 2 X=2, QUADRANT 0 Y=2
1J1	2A2A1-K0	4- 43	QUADRANT 2 X=2, QUADRANT 0 Y=2
1K0	2A2A1-J1	4- 43	QUADRANT 2 Y=2, QUADRANT 0 X=2
	2A2A4-B0	4- 7	
1K1	2A2A1-H0	4- 43	QUADRANT 2 Y=3, QUADRANT 0 X=3
	2A2A4-I0	4- 7	
1M0	2A2B9-C2	4- 75	
1M1	2A2B9-C3	4- 75	DATA TO PF QUADRANT 0, BIT 12
2C1	2A2A4-N0	4- 7	QUADRANT 0 DIGIT GATE 3 AND
			QUADRANT 0 DIGIT GATE 0
2F0	2A2B3-C0	4- 39	QUADRANT 0 DIGIT GATE 3 AND
	2A2A4-N0	4- 7	QUADRANT 0 DIGIT GATE 0
2F1	2A2B2-D1	4- 39	QUADRANT 1 DIGIT GATE 1 AND
	2A2A4-P0	4- 7	QUADRANT 0 DIGIT GATE 2
2J0	2A2B3-I0	4- 33	QUADRANT 0 SENSE GATE 0 AND
	2A2A4-V0	4- 7	QUADRANT 0 SENSE GATE 1
2J1	2A2B3-G0	4- 33	QUADRANT 0 SENSE GATE 2 AND
	2A2A4-U0	4- 7	QUADRANT 0 SENSE GATE 3
2K0	2A2B4-C2	4- 21	NOT BIT 12 FROM PF QUADRANT 0

2-62A

SELECT 1 OF 4
GROUPS IN A QUAD

SELECT 1 OF 4
WORDS IN A SECT.

ADDR BITS 586 DECODED

ADDR BITS 384 DECODED

2Y00X0 (00XXXXX) (00-37)
2Y10X1 (01XXXXX) (40-77)
2Y30X3 (11XXXXX) (137-177)
2Y20X2 (10XXXXX) (100-137)
USEDX
2X00Y0
2X00Y0 (XX00XXX)
USEDW
2X10Y1
2X10Y0 (XX01XXX)
USEDZ
2X20Y2
2X20Y2 (XX10XXX)
USEDY
2X30Y3
2X30Y3 (XX11XXX)

NOTES
① ADDR BITS 0-2 DECODED.

BIT USED — SECT. 0 — SECT. 1

DZ13A / DZ13A
DZ13B / DZ13B
USED A
USED B

BIT 12 — SECT. 0 — SECT. 1

DZ12A / DZ12A
DZ12B / DZ12B
PF012

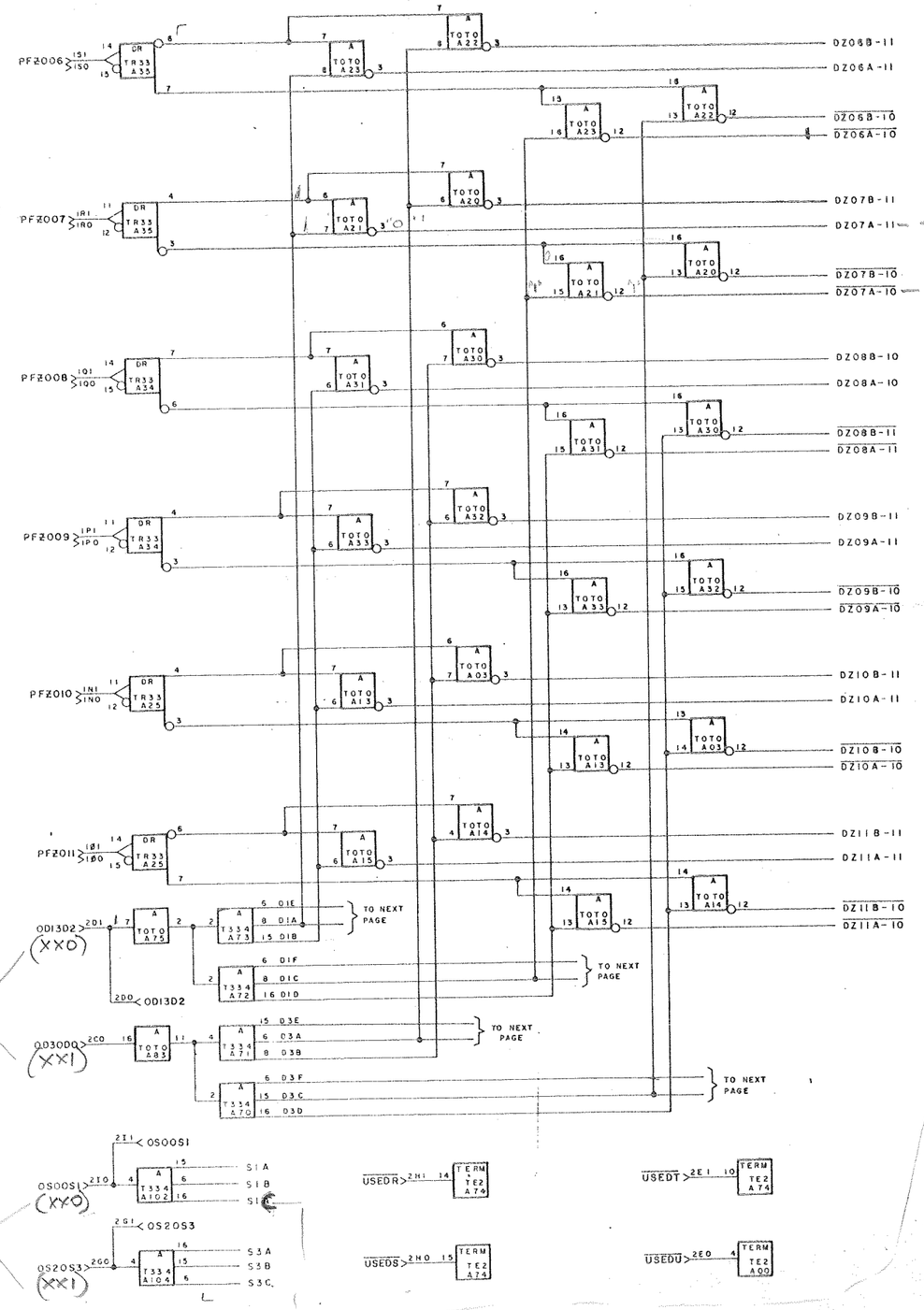
① SECT. 0 2-BIT RD LWR — OS0051 (XX0)
① SECT. 1 2-BIT RD UP — OS2053 (XX1)

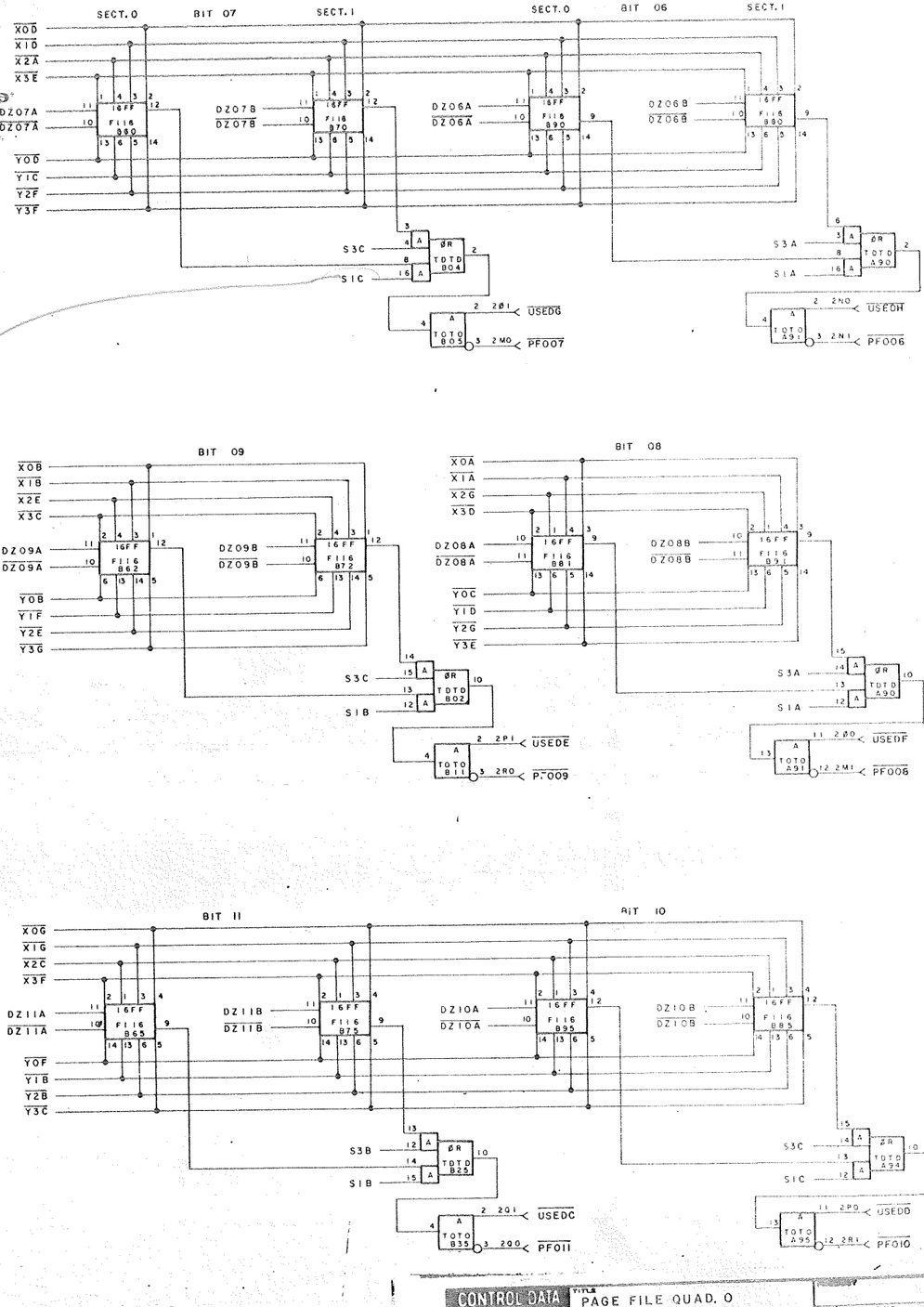
DATA

① SECT. 0 2-BIT WR LWR — OD3000 (XX1)
① SECT. 1 2-BIT WR UP — ID1002 (XX2)

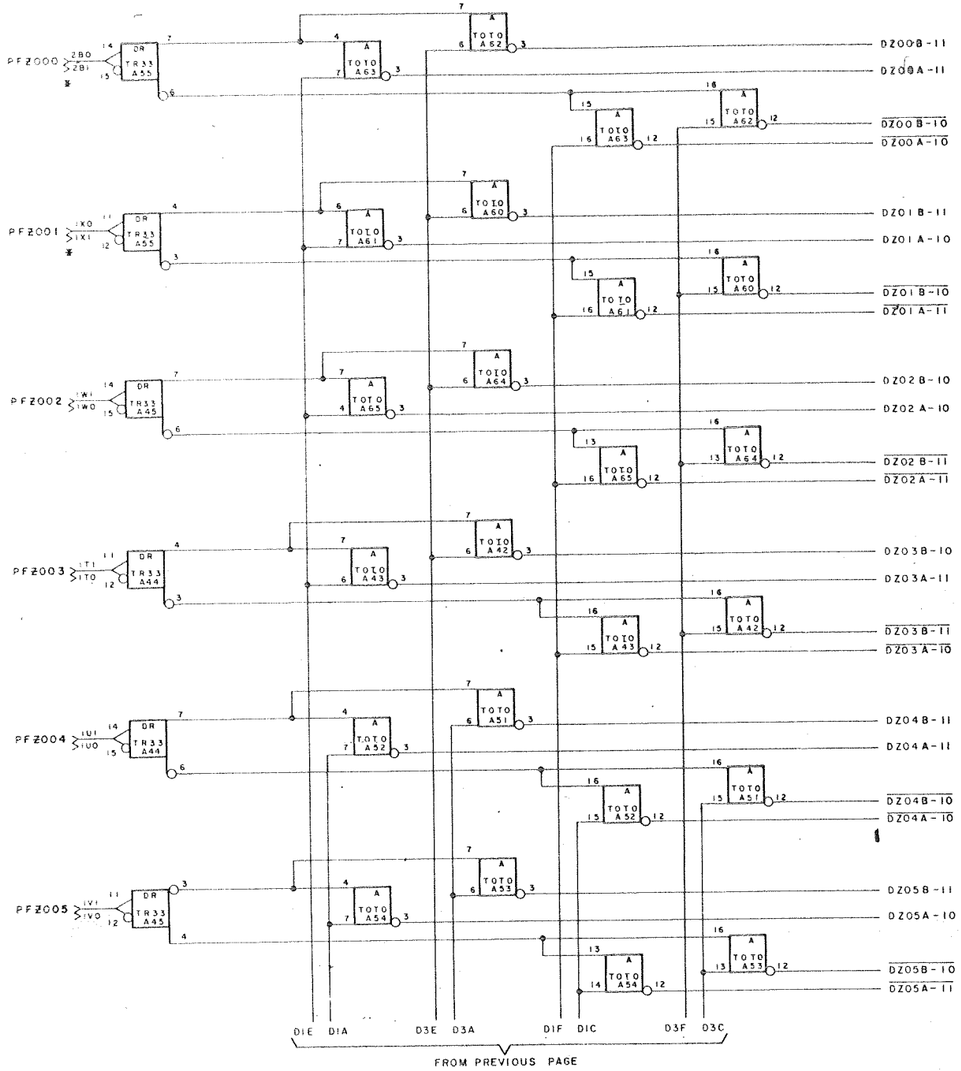
DZ12B-11
DZ12A-11
DZ12B-10
DZ12A-10
DZ13B-11
DZ13A-11
DZ13B-10
DZ13A-10

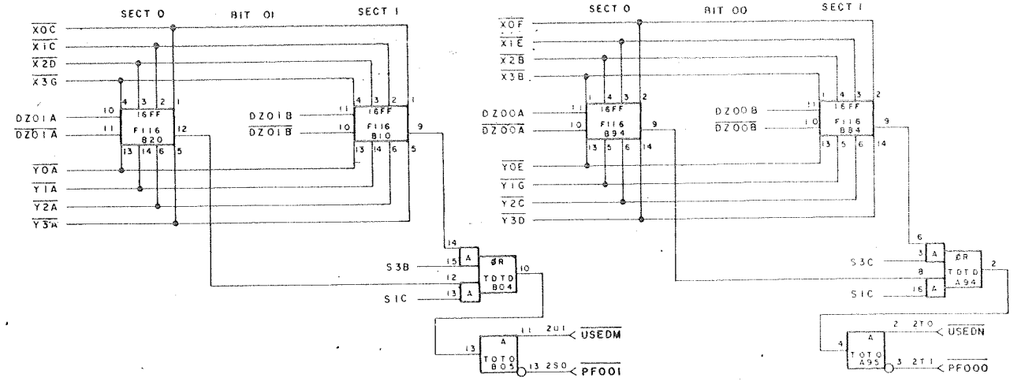
CONTROL DATA CORPORATION — DEVELOPMENT DIVISION	TITLE: PAGE FILE QUAD 0 ADDRESSES XX0, XX1	2A2A3 LOC 2A283 PART NO. 185301 SER 004	PRODUCT; SIZE C; DRAWING NO. 60289500; REV. W; SHEET; PAGE 4-31

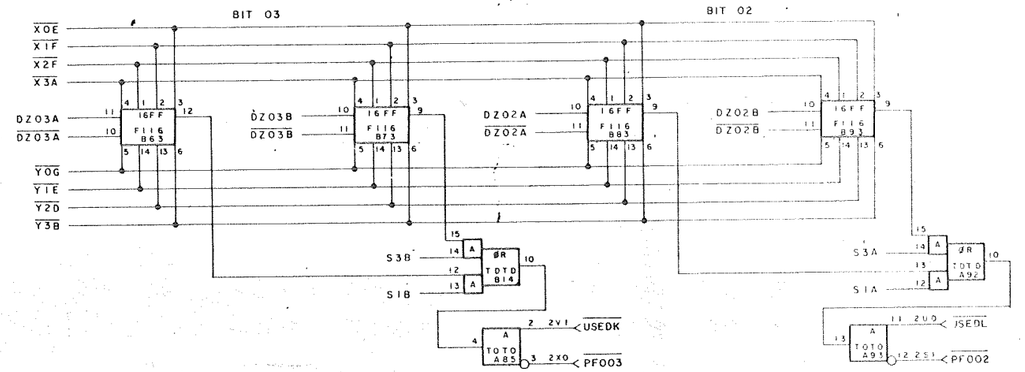


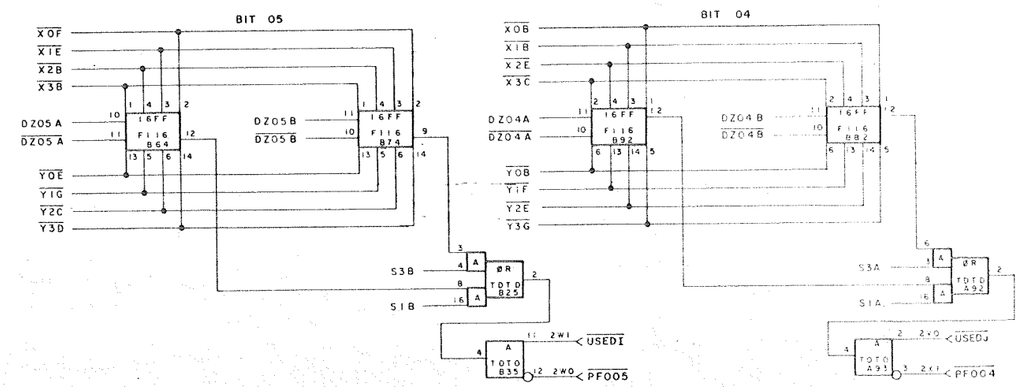


CONTROL DATA	TITLE: PAGE FILE QUAD. 0 ADDRESSES XX0, XX1	SIZE C	DRAWING NO 60289500 REV W
DEVELOPMENT DIVISION	2A2A3 LOC: 2A2B3 PART NO 185301 SER 004	SHEET	PAGE 4-33









CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE
PAGE FILE QUAD 0
ADDRESSES XX0, XX1
2A2A3
LOC: 2A2B3 PART NO. 185301 SER 004

PRODUCT

SIZE C | DRAWING NO 60289500 | REV W

SHEET | PAGE 4-35

```
1B1     2A2A0-F1  4-  49          QUADRANT 3 Y=0, QUADRANT 1 X=0
        2A2A4-C0  4-   7
1C1     2A2A0-E1  4-  49          QUADRANT 3 Y=1, QUADRANT 1 X=1
        2A2A4-A0  4-   7
1D1     2A2A4-H3  4-   7          QUADRANT 3 X=1, QUADRANT 1 Y=1
1E1     2A2A0-C1  4-  49          QUADRANT 3 X=1, QUADRANT 1 Y=1
1F1     2A2A0-H1  4-  49          QUADRANT 3 X=0, QUADRANT 1 Y=0
1G0     2A2A4-A3  4-   7          QUADRANT 3 X=3, QUADRANT 1 Y=3
1G1     2A2A4-D3  4-   7          QUADRANT 3 X=0, QUADRANT 1 Y=0
1H0     2A2A0-K1  4-  49          QUADRANT 3 X=3, QUADRANT 1 Y=3
1I1     2A2A4-I3  4-   7          QUADRANT 3 X=2, QUADRANT 1 Y=2
1J1     2A2A0-K0  4-  49          QUADRANT 3 X=2, QUADRANT 1 Y=2
1K0     2A2A0-J1  4-  49          QUADRANT 3 Y=2, QUADRANT 1 X=2
        2A2A4-H0  4-   7
1K1     2A2A0-H0  4-  49          QUADRANT 3 Y=3, QUADRANT 1 X=3
        2A2A4-H1  4-   7
1M0     2B2B9-P2  4-  75
1M1     2B2B9-P3  4-  75          DATA TO PF QUADRANT 1, BIT 12
2C1     2A2A4-K1  4-   7          QUADRANT 1 DIGIT GATE 3 AND
                                  QUADRANT 1 DIGIT GATE 0
2F0     2A2B2-C0  4-  39          QUADRANT 1 DIGIT GATE 3 AND
        2A2A4-K1  4-   7          QUADRANT 1 DIGIT GATE 0
2F1     2A2B1-D1  4-  45          QUADRANT 2 DIGIT GATE 1 AND
        2A2A4-U0  4-   7          QUADRANT 1 DIGIT GATE 2
2J0     2A2B2-I0  4-  39          QUADRANT 1 SENSE GATE 0 AND
        2A2A4-T0  4-   7          QUADRANT 1 SENSE GATE 1
2J1     2A2B2-G0  4-  39          QUADRANT 1 SENSE GATE 2 AND
        2A2A4-V1  4-   7          QUADRANT 1 SENSE GATE 3
2K0     2A2A4-K2  4-  21          NOT BIT 12 FROM PF QUADRANT 1
```

2-68A

Rev W Page 4-36

SELECT 1 OF 4
GROUPS IN A QUAD.

ADDR
BITS
5&6
DECODED

GROUP 0

3Y0IX0 (00XXXXX) 1B1

GROUP 1

3Y11X1 (01XXXXX) 1C1

GROUP 3

3Y31X3 (11XXXXX) 1K1

GROUP 2

3Y21X2 (10XXXXX) 1K0

USEOX 1F0

USEOW 1D0

USEOZ 1I0

USEOY 1H1

3X0IY0 (XX00XXX) 1F1

3X11Y1 (XX01XXX) 1D1

3X21Y2 (XX10XXX) 1I1

3X31Y3 (XX11XXX) 1G0

SELECT 1 OF 4
WORDS IN A QUAD.

ADDR
BITS
3&4
DECODED

NOTES:
① ADDR BITS 0-2 DECODED.

SECT 0 BIT USED SECT 1

DZ13A DZ13A
DZ13B DZ13B

SECT 0 BIT 12 SECT 1

DZ12A DZ12A
DZ12B DZ12B

USEDA 2LO
USEDB 2LO
USEDP 12 2K1
PF 112 12 2K0

① SECT. 0 2-BIT RD LWR 1S0IS1 2J0
① SECT. 1 2-BIT RD UP 1S2IS3 2J1

DATA

PFZ112 1M1 1M0

USEDV 1L1 1L0

① SECT. 0 2-BIT WR LWR 1D3IDO 2C1
① SECT. 1 2-BIT WR UP 2D1ID2 2F1

DZ12B-11
DZ12A-11
DZ12B-10
DZ12A-10
DZ13B-11
DZ13A-11
DZ13B-10
DZ13A-10

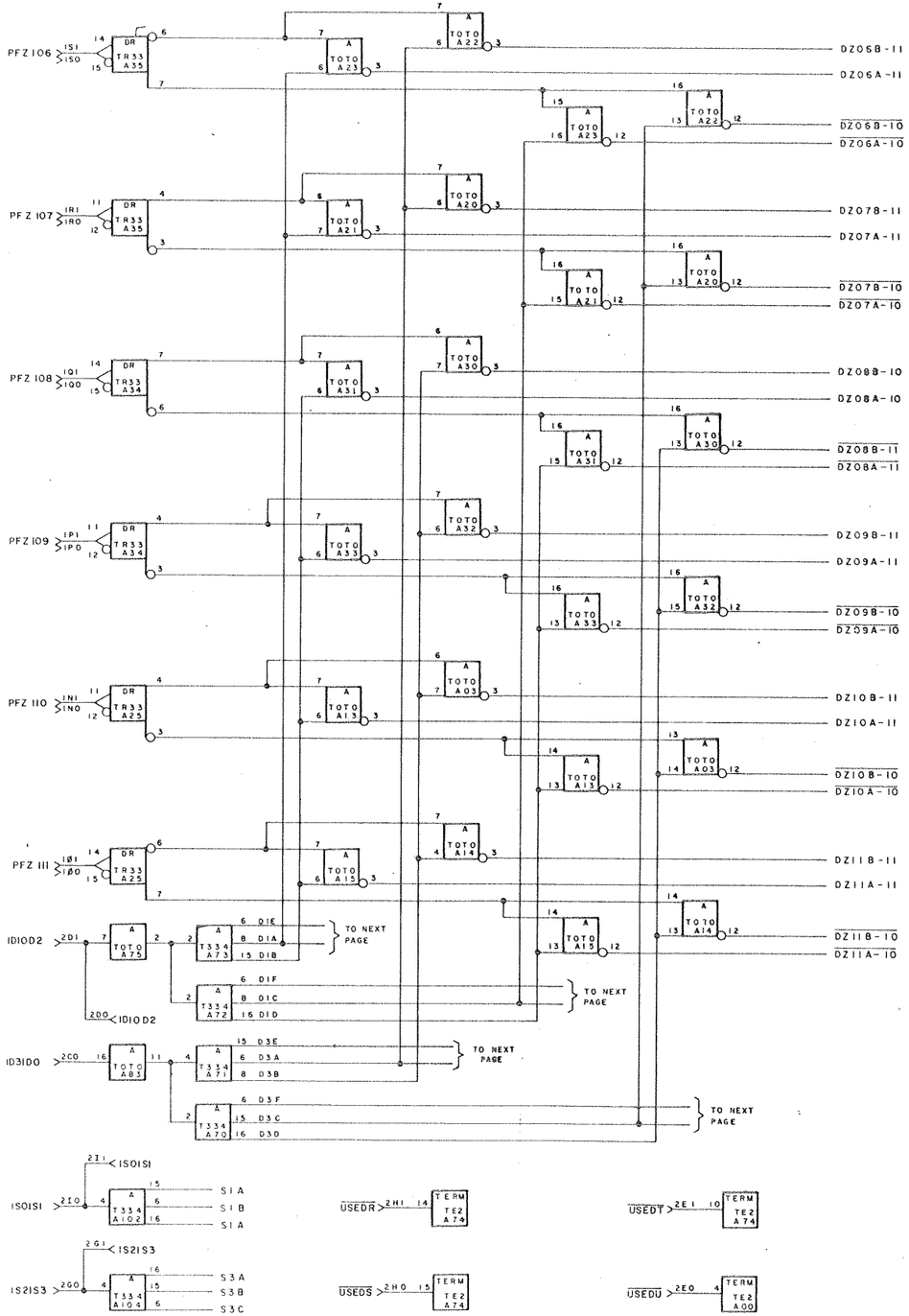
160

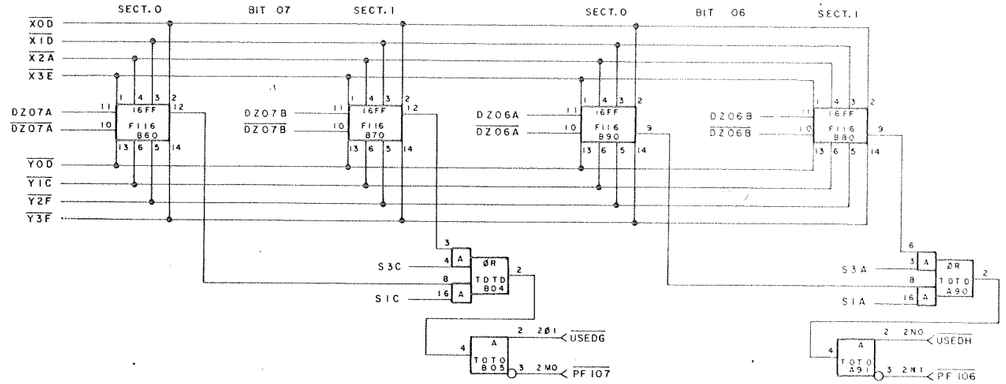
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

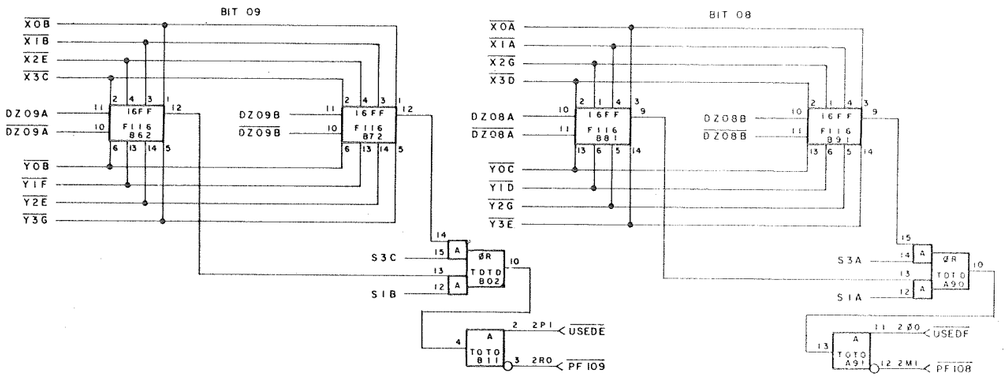
TITLE
PAGE FILE QUAD. 1
ADDRESSES XX2, XX3
2A2A2
LOC: 2A2B2 PART NO. 185301 SER 005

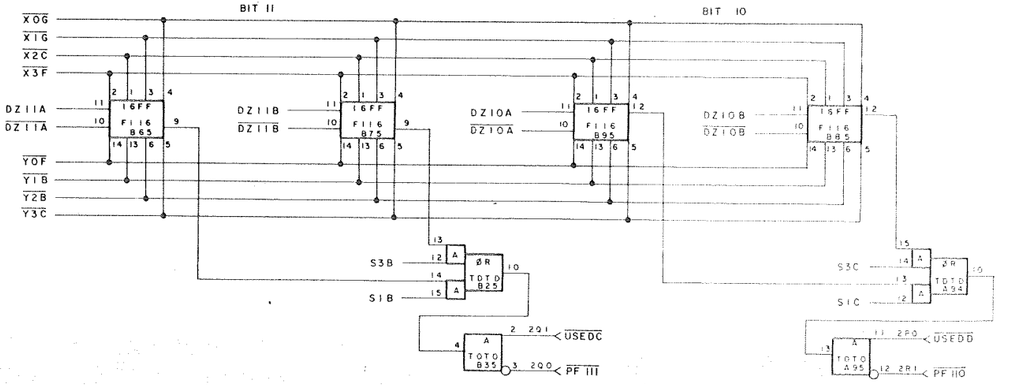
PRODUCT
SIZE C | DRAWING NO. 60289500 | REV V1
SHEET | PAGE 4-37

69

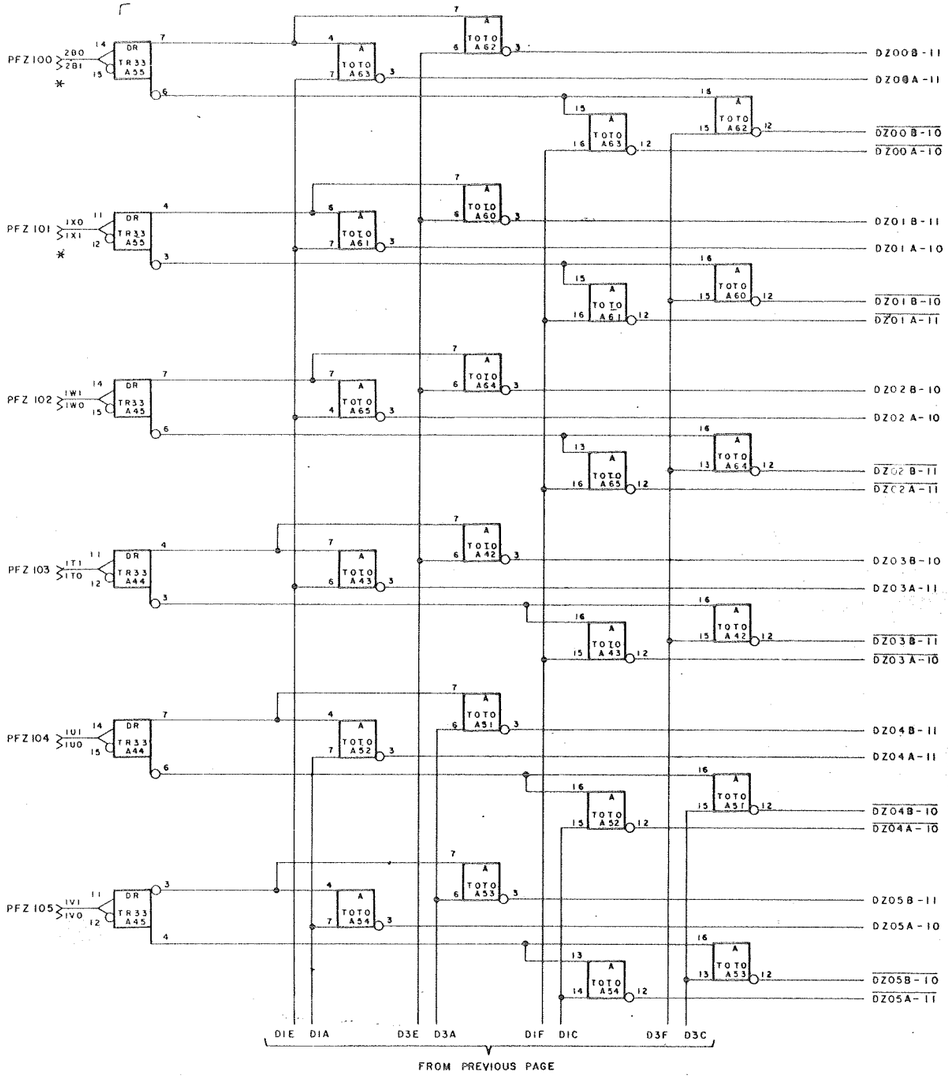


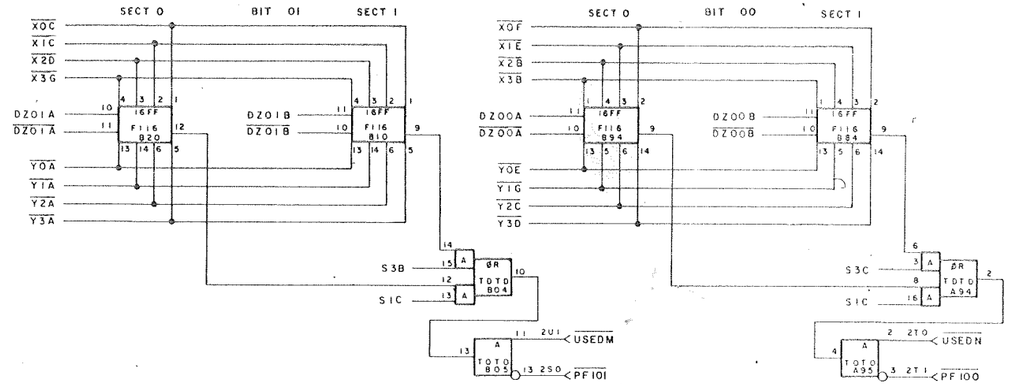






CONTROL DATA	TITLE: PAGE FILE QUAD. I ADDRESSES XX2, XX3 2A2A2 LOC: 2A282 PART NO. 185301 SER 005	SIZE C	DRAWING NO 60289500	REV J
DEVELOPMENT DIVISION		SHEET	PAGE 4-39	


PFZ100
PFZ101
PFZ102
PFZ103
PFZ104
PFZ105
DZ00B-11
DZ00A-11
DZ00B-10
DZ00A-10
DZ01B-11
DZ01A-10
DZ01B-10
DZ01A-11
DZ02B-10
DZ02A-10
DZ02B-11
DZ02A-11
DZ03B-10
DZ03A-11
DZ03B-11
DZ03A-10
DZ04B-11
DZ04A-11
DZ04B-10
DZ04A-10
DZ05B-11
DZ05A-10
DZ05B-10
DZ05A-11
D1E D1A D3E D3A D1F D1C D3F D3C
FROM PREVIOUS PAGE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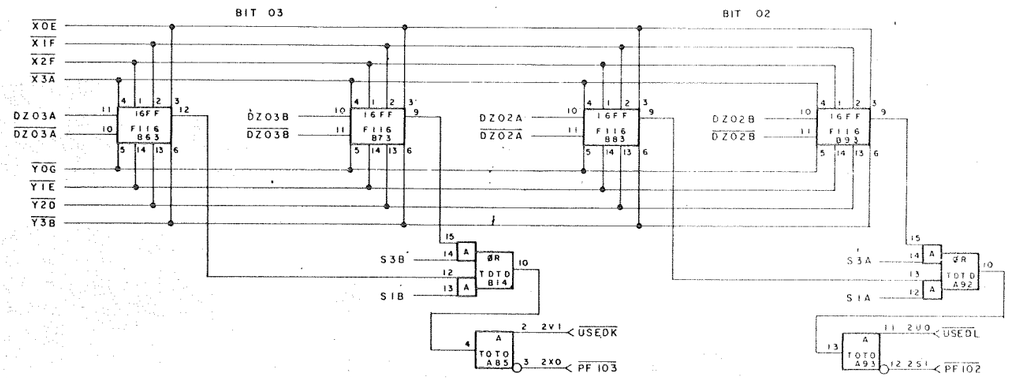
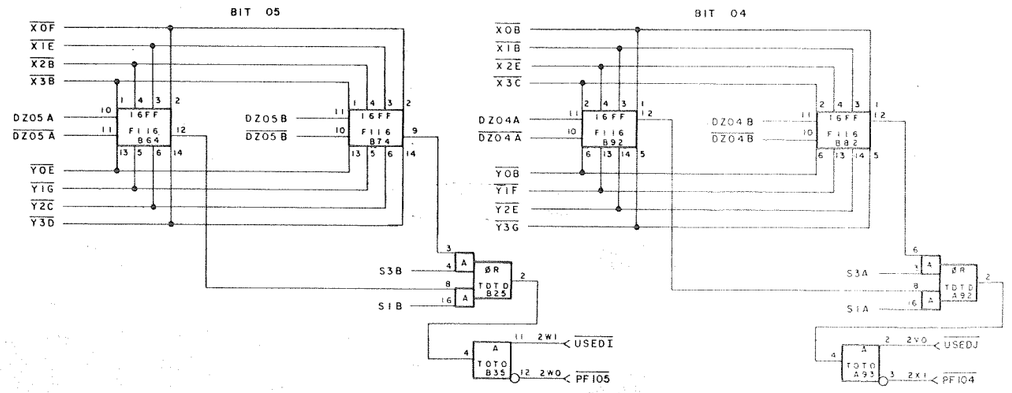
BIT 01
SECT 1
BIT 00
S3B
S1C
S3C
USEDM
USEDN
PF101
PF100


BIT 03
BIT 02
S3B
S1B
S3A
S1A
USEDK
USEDL
PF103
PF102


BIT 05
BIT 04
S3B
S1B
S3A
S1A
USEDI
USEDJ
PF105
PF104

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1B1     2A2A3-G1  4- 31        QUADRANT 2 X=0, QUADRANT 0 Y=0
        2A2A4-C3  4-  7
1C1     2A2A3-E1  4- 31        QUADRANT 2 X=1, QUADRANT 0 Y=1
        2A2A4-F3  4-  7
1D1     2A2A4-D0  4-  7        QUADRANT 2 Y=1, QUADRANT 0 X=1
1E1     2A2A3-C1  4- 31        QUADRANT 2 Y=1, QUADRANT 0 X=1
1F1     2A2A3-B1  4- 31        QUADRANT 2 Y=0, QUADRANT 0 X=0
1G0     2A2A4-I0  4-  7        QUADRANT 2 Y=3, QUADRANT 0 X=3
1G1     2A2A4-F0  4-  7        QUADRANT 2 Y=0, QUADRANT 0 X=0
1H0     2A2A3-K1  4- 31        QUADRANT 2 Y=3, QUADRANT 0 X=3
1I1     2A2A4-B0  4-  7        QUADRANT 2 Y=2, QUADRANT 0 X=2
1J1     2A2A3-K0  4- 31        QUADRANT 2 Y=2, QUADRANT 0 X=2
1K0     2A2A3-J1  4- 31        QUADRANT 2 X=2, QUADRANT 0 Y=2
        2A2A4-J3  4-  7
1K1     2A2A3-H0  4- 31        QUADRANT 2 X=3, QUADRANT 0 Y=3
        2A2A4-H3  4-  7
1M0     2B2B8-02  4- 77
1M1     2B2B8-03  4- 77
2C1     2A2A4-H0  4-  7        DATA TO PF QUADRANT 2, BIT 12
2F0     2A2B1-C0  4- 45        QUADRANT 2 DIGIT GATE 3 AND
        2A2A4-H0  4-  7        QUADRANT 2 DIGIT GATE 0
2F1     2A2B0-D1  4- 51        QUADRANT 2 DIGIT GATE 3 AND
        2A2A4-S0  4-  7        QUADRANT 2 DIGIT GATE 0
2J0     2A2B1-I0  4- 45        QUADRANT 3 DIGIT GATE 1 AND
        2A2A4-A1  4-  7        QUADRANT 2 DIGIT GATE 2
2J1     2A2B1-G0  4- 45        QUADRANT 2 SENSE GATE 0 AND
        2A2A4-H0  4-  7        QUADRANT 2 SENSE GATE 1
2K0     2A2B4-N2  4- 21        QUADRANT 2 SENSE GATE 2 AND
                               QUADRANT 2 SENSE GATE 3
                               NOT BIT 12 FROM PF QUADRANT 2
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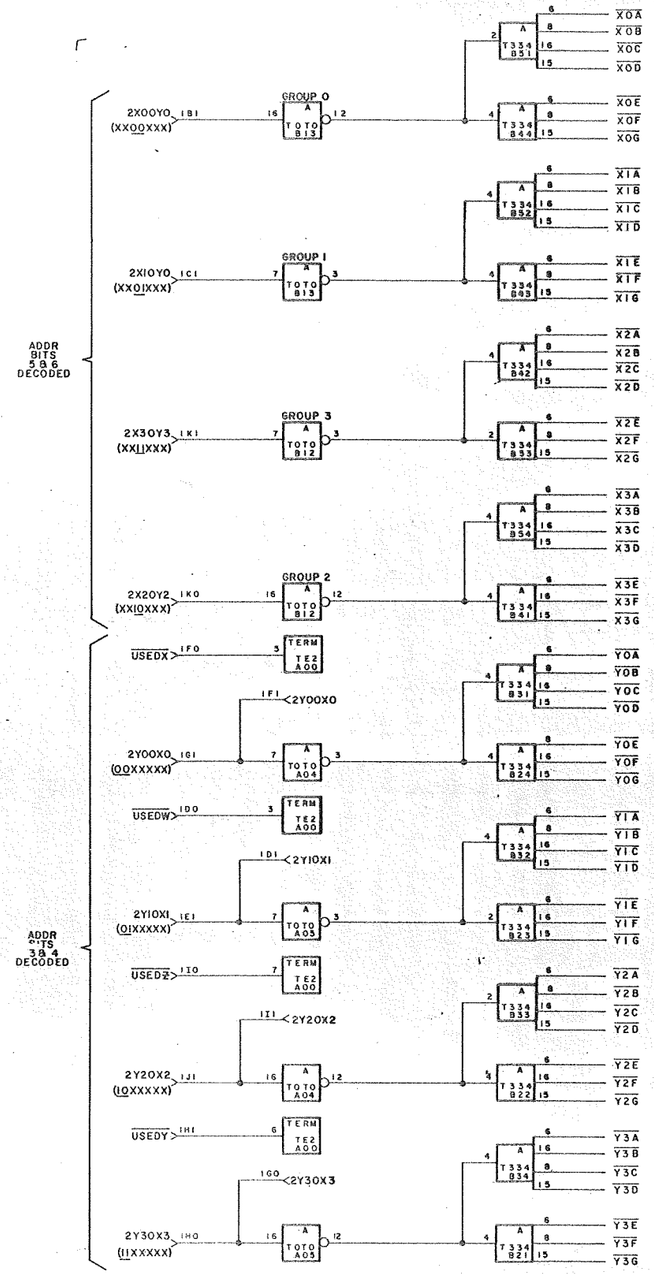
2-74A Rev W Pg 4-42

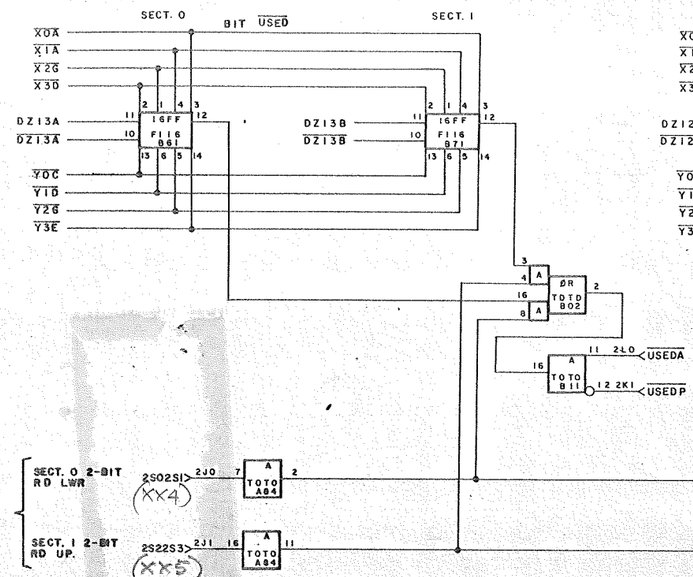
SELECT 1 OF 4
GROUPS IN A QUAD

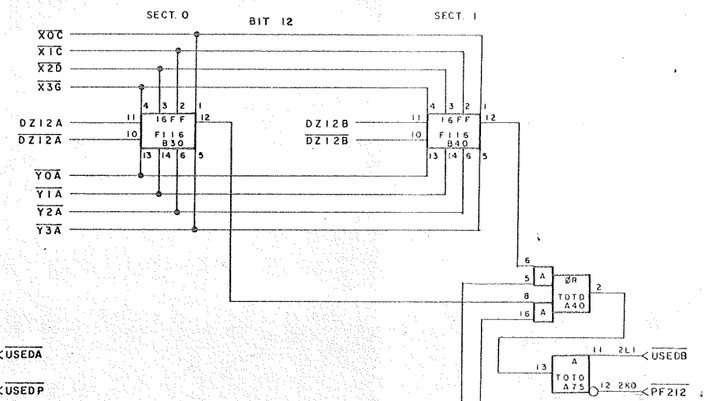


SELECT 1 OF 4
WORDS IN A SECT

ADDR BITS 3 & 4 DECODED

NOTES:
① ADDR BITS 0-2 DECODED.





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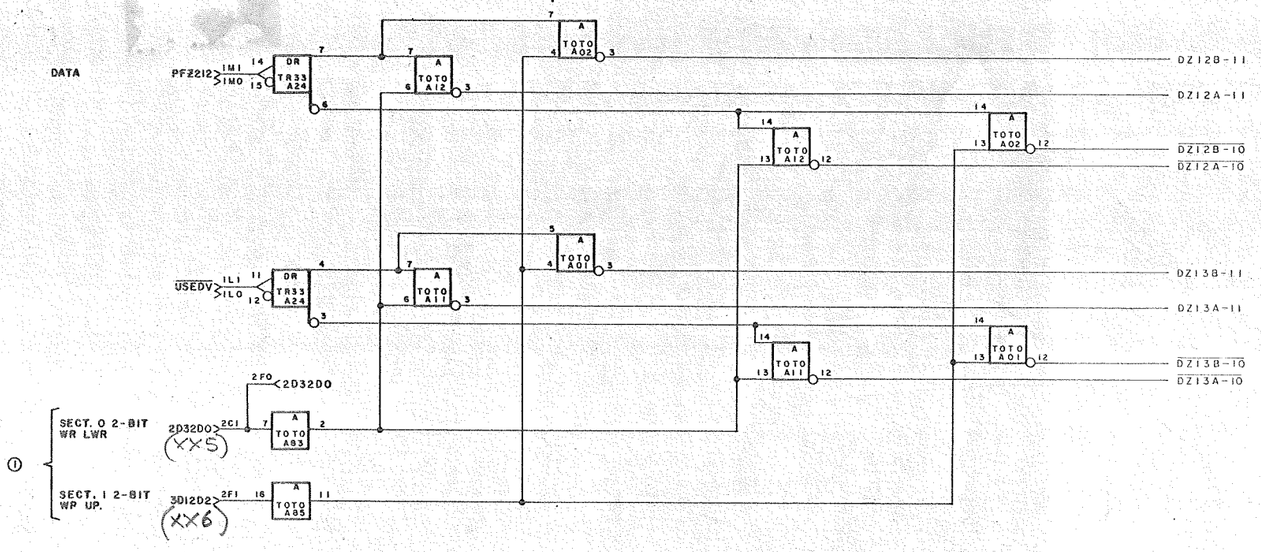
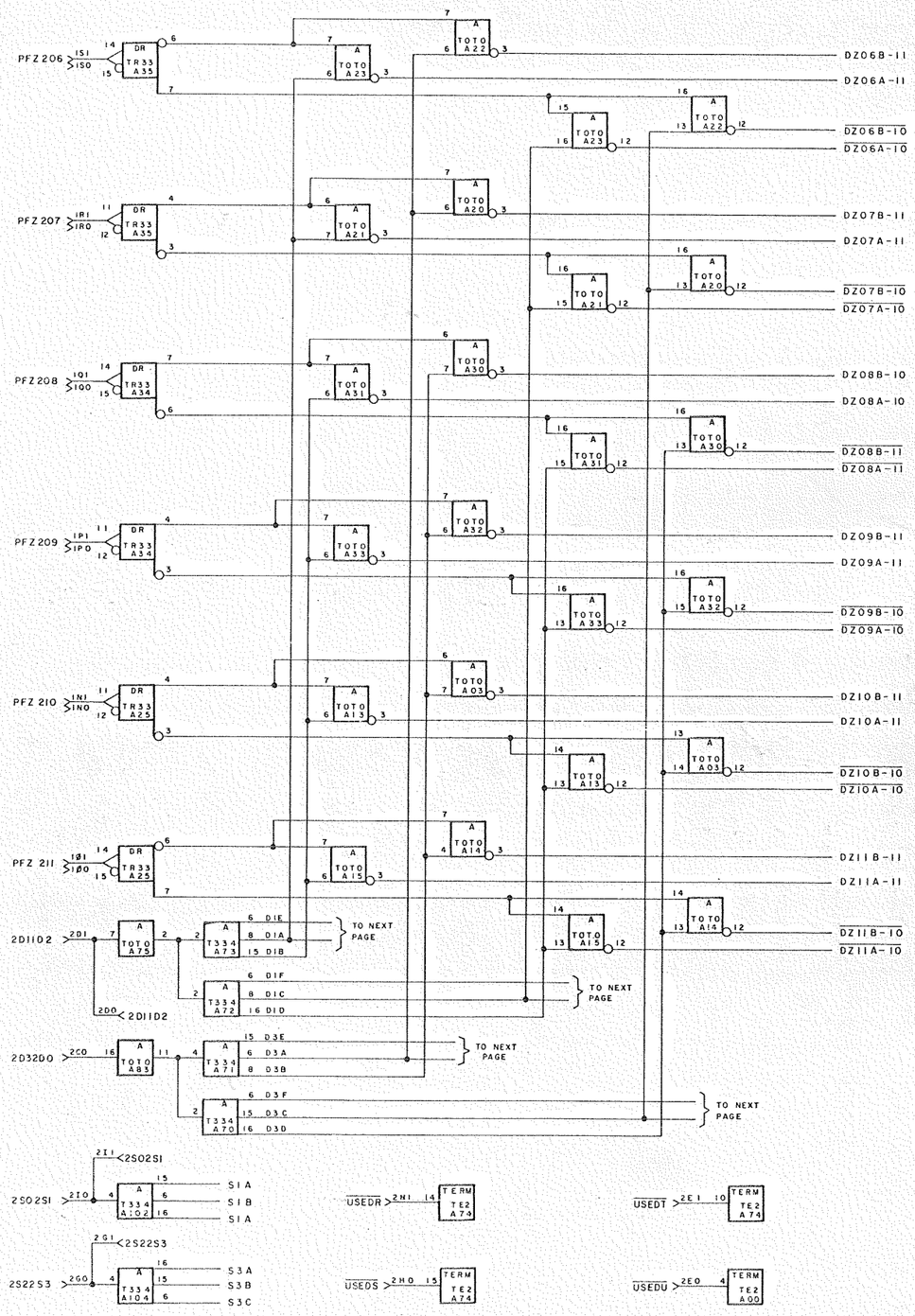
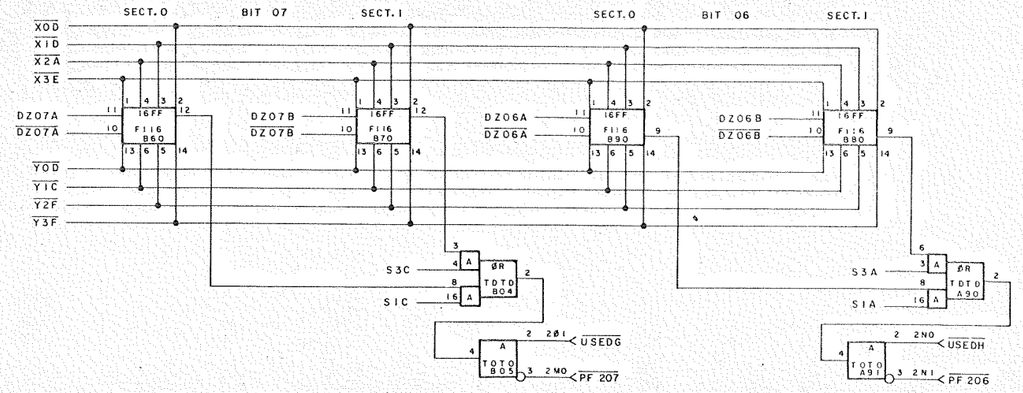
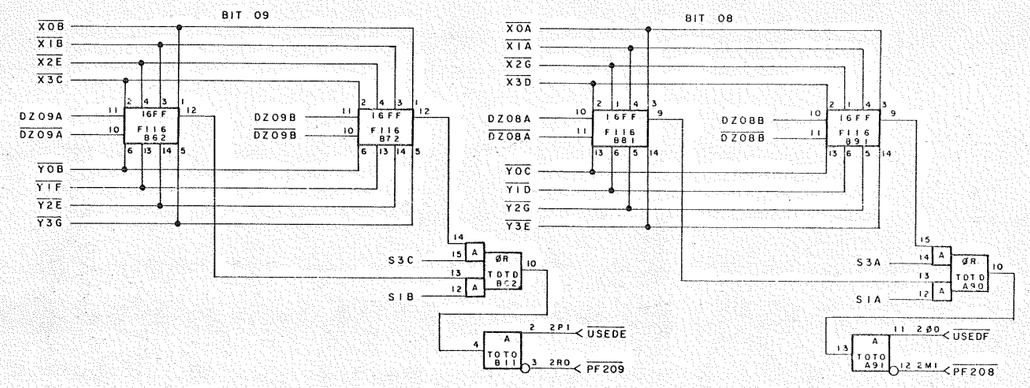
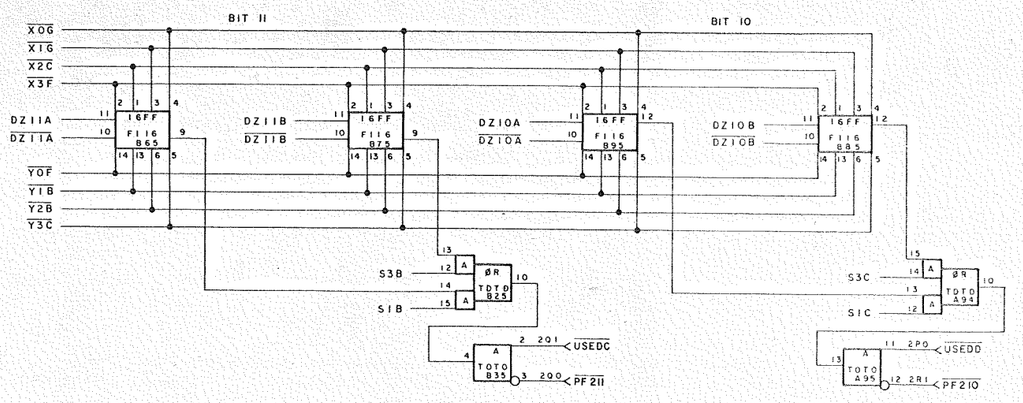


CONTROL DATA	TITLE: PAGE FILE QUAD. 2 ADDRESSES XX4, XX5 2A2A1 LOC: 2A2B1 PART NO. 183301 SER 006	PRODUCT	
DEVELOPMENT DIVISION		SIZE C	DRAWING NO. 60289500 REV. W
		SHEET	PAGE 4-43



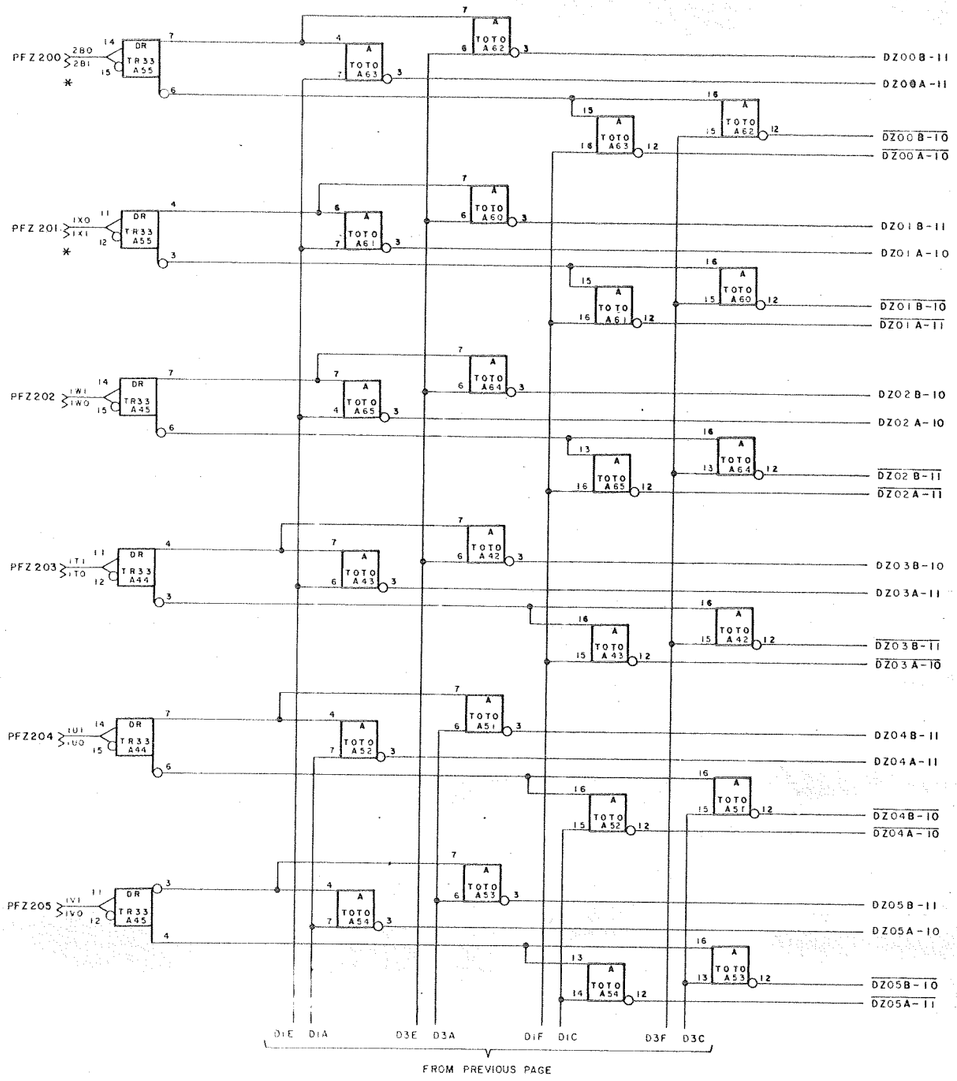


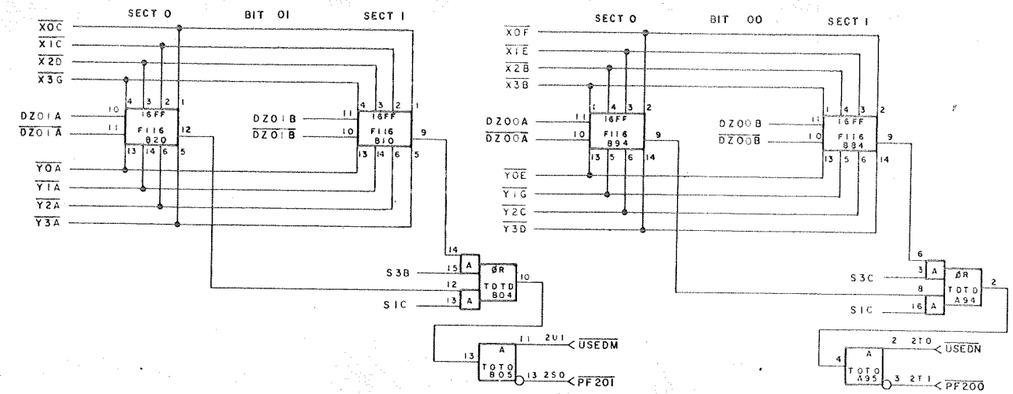


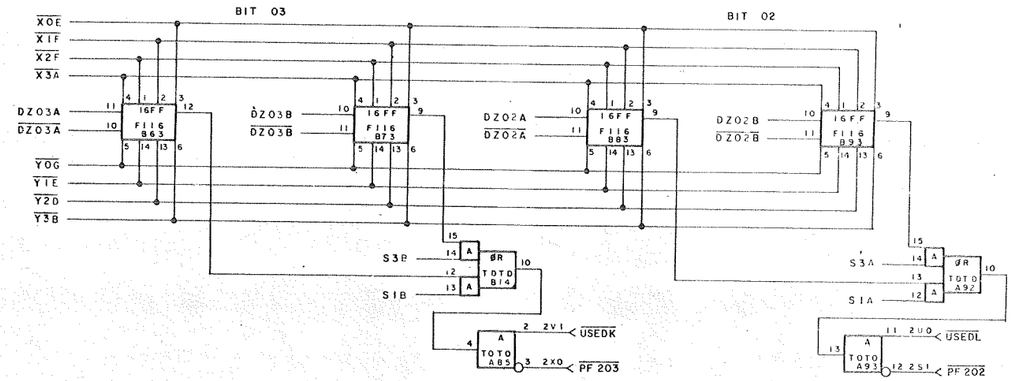


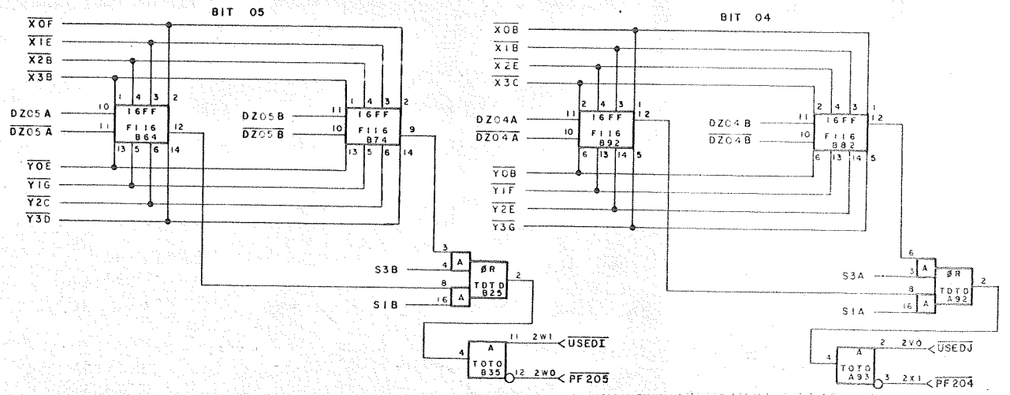
CONTROL DATA	TITLE: PAGE FILE QUAD. 2 ADDRESSES XX4,XX5		REV. 4-45
DEVELOPMENT DIVISION	2A2A1 LOC: 2A2B1	PART NO. 185[illegible]	SER 00
		SIZE C	DRAWING NO. 60289500 REV. W
		SHEET	PAGE 4 - [illegible]

holes punched wrong









CONTROL DATA	TITLE	PRODUCT
DEVELOPMENT DIVISION	PAGE FILE QUAD. 2 ADDRESSES XX4, XX5 2A2A1 LOC: 2A2B1 PART NO. 85301 SER 006	SIZE C · DRAWING NO. 60289500 · REV. W SHEET · PAGE 4-47

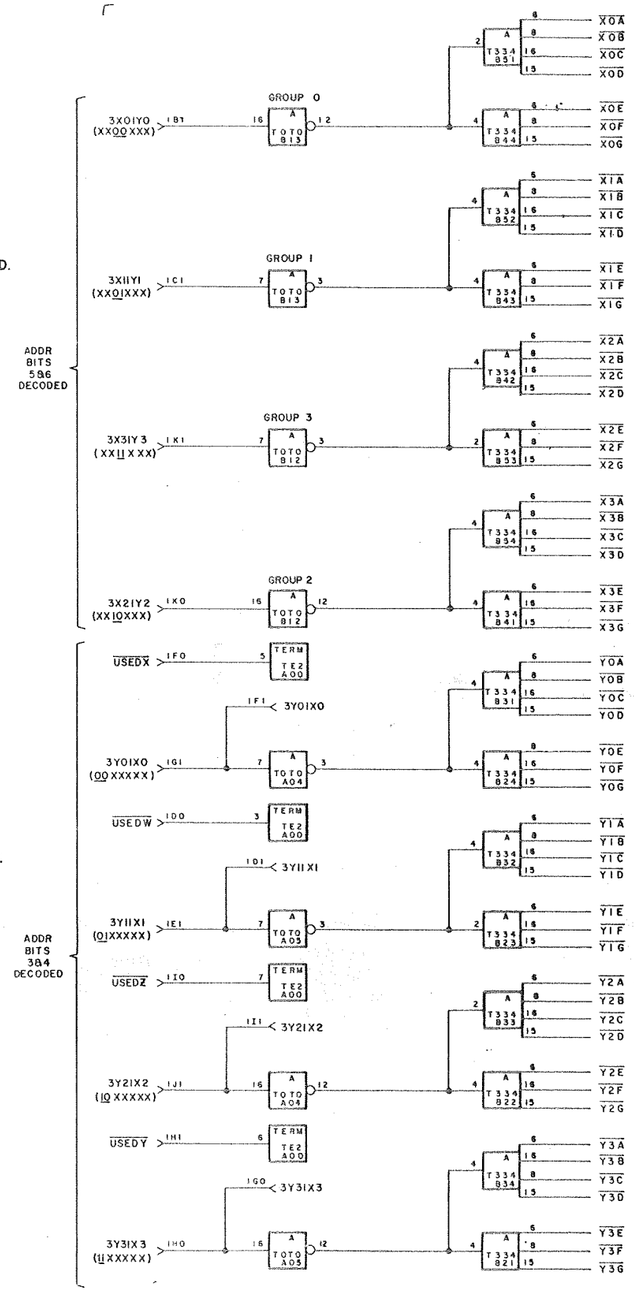
```
1B1     2A2A2-F1  4- 37        QUADRANT 3 X=0, QUADRANT 1 Y=0
        2A2A4-D3  4-  7
1C1     2A2A2-E1  4- 37
        2A2A4-B3  4-  7        QUADRANT 3 X=1, QUADRANT 1 Y=1
1D1     2A2A4-A3  4-  7
1E1     2A2A2-C1  4- 37        QUADRANT 3 Y=1, QUADRANT 1 X=1
1F1     2A2A2-B1  4- 37        QUADRANT 3 Y=1, QUADRANT 1 X=1
1G0     2A2A4-H1  4-  7        QUADRANT 3 Y=0, QUADRANT 1 X=0
1G1     2A2A4-C0  4-  7        QUADRANT 3 Y=3, QUADRANT 1 X=3
1H0     2A2A2-K1  4- 37        QUADRANT 3 Y=0, QUADRANT 1 X=0
1I1     2A2A4-H0  4-  7        QUADRANT 3 Y=3, QUADRANT 1 X=3
1J1     2A2A2-K0  4- 37        QUADRANT 3 Y=2, QUADRANT 1 X=2
1K0     2A2A2-J1  4- 37        QUADRANT 3 Y=2, QUADRANT 1 X=2
        2A2A4-I3  4-  7        QUADRANT 3 X=2, QUADRANT 1 Y=2
1K1     2A2A2-H0  4- 37
        2A2A4-A3  4-  7        QUADRANT 3 X=3, QUADRANT 1 Y=3
1M0     2B2A8-P2  4- 77
1M1     2B2A8-P3  4- 77
2C1     2A2A4-N1  4-  7        DATA TO PF QUADRANT 3, BIT 12
                               QUADRANT 3 DIGIT GATE 3 AND
2F0     2A2B0-C0  4- 51        QUADRANT 3 DIGIT GATE 0
        2A2A4-N1  4-  7        QUADRANT 3 DIGIT GATE 3 AND
2F1     2A2B3-D0  4- 93        QUADRANT 3 DIGIT GATE 0
        2A2A4-M1  4-  7        QUADRANT 0 DIGIT GATE 1 AND
2J0     2A2B0-I0  4- 51        QUADRANT 3 DIGIT GATE 2
        2A2A4-M1  4-  7        QUADRANT 3 SENSE GATE 0 AND
2J1     2A2B0-G0  4- 51        QUADRANT 3 SENSE GATE 1
        2A2A4-X0  4-  7        QUADRANT 3 SENSE GATE 2 AND
2K0     2A2B4-N3  4- 21        QUADRANT 3 SENSE GATE 3
                               NOT BIT 12 FROM PF QUADRANT 3
```

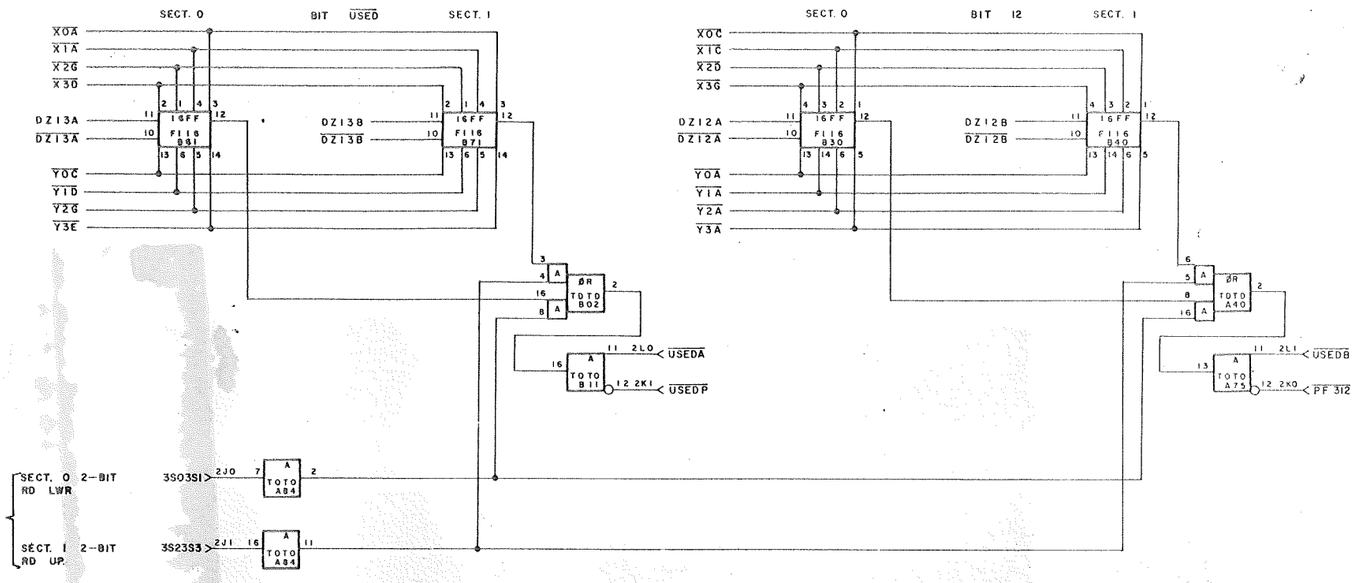
2-80A

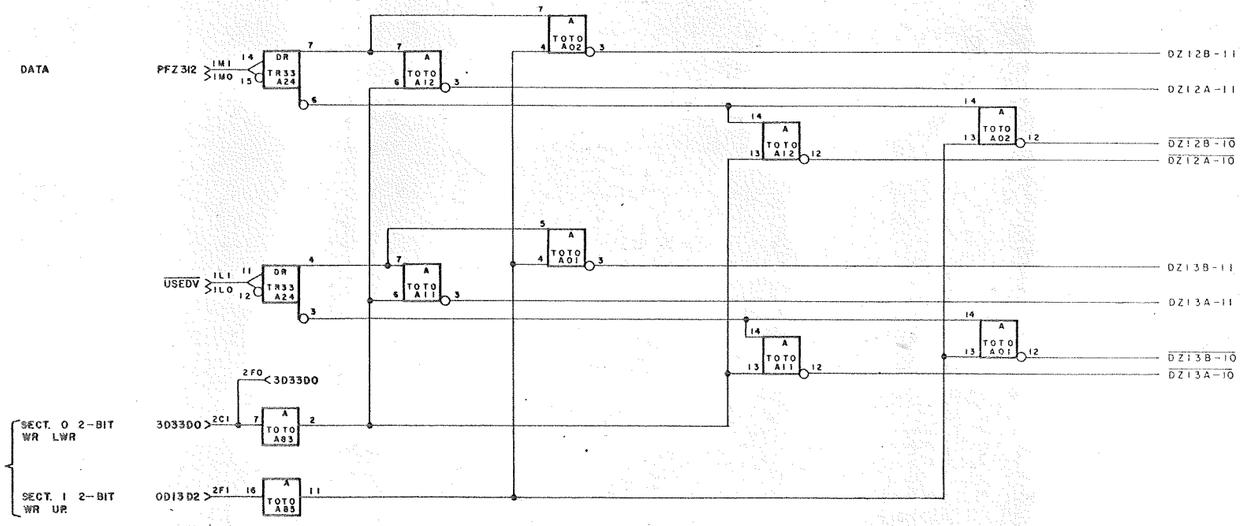
Rev W
4-48

SELECT 1 OF 4
GROUPS IN A QUAD.

SELECT 1 OF 4
WORDS IN A SECT.



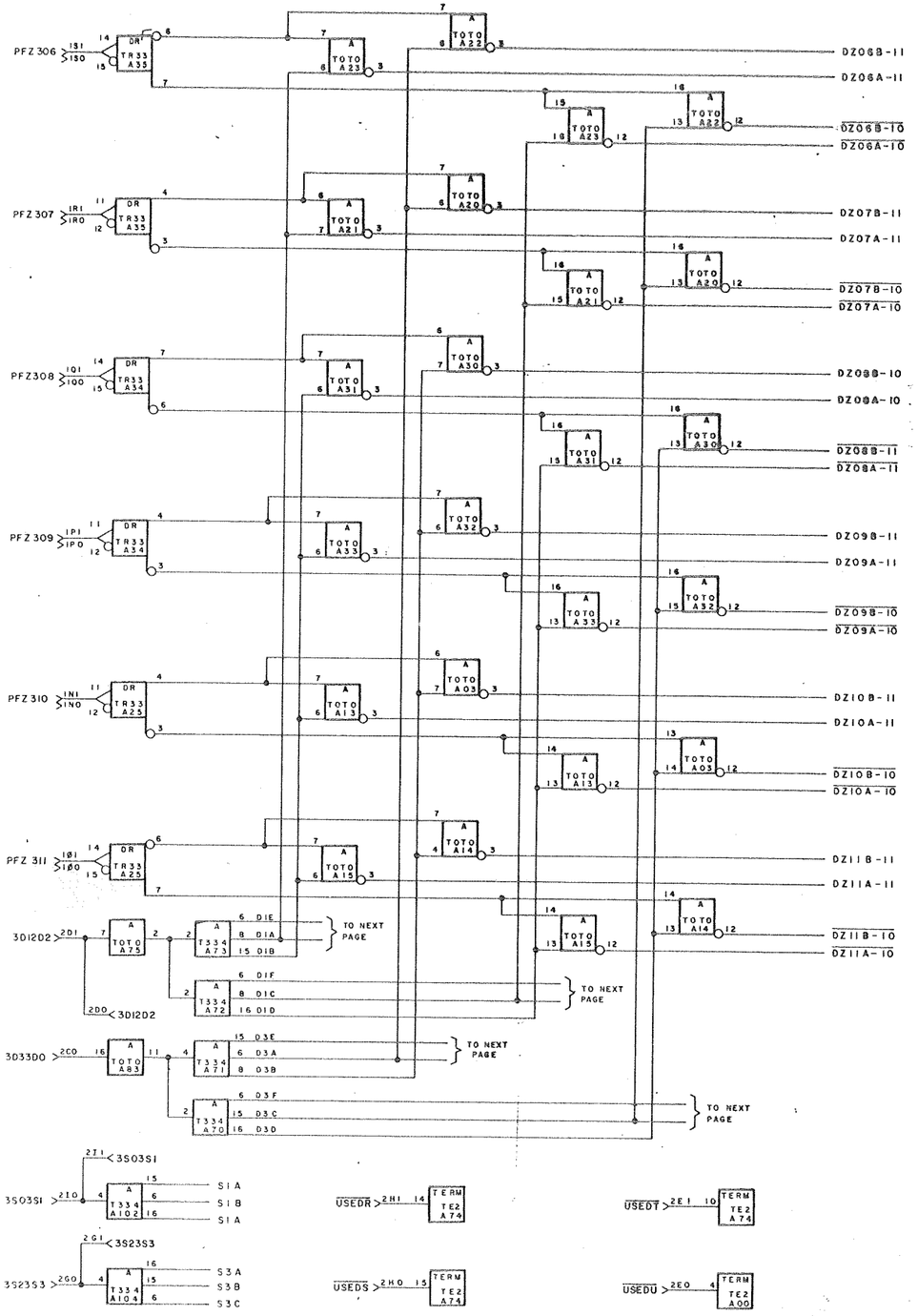


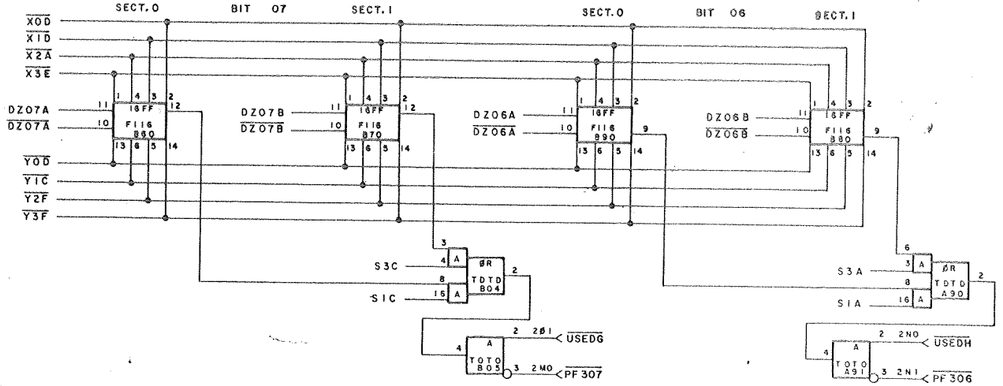


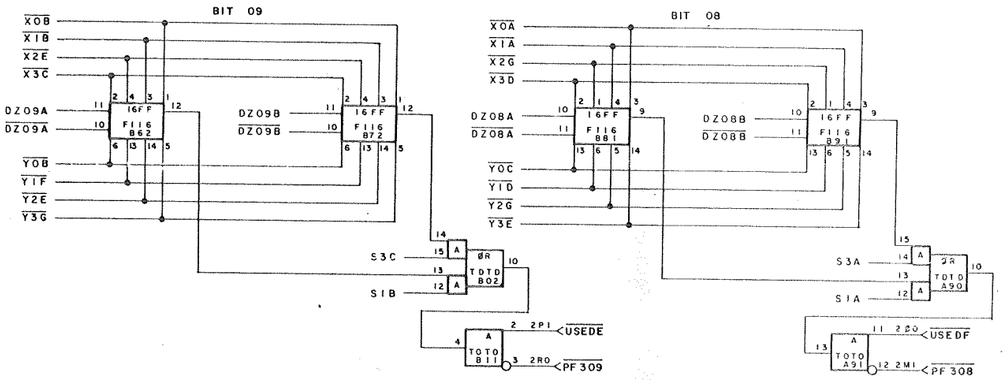
NOTES:
① ADDR BITS 0-2 DECODED.

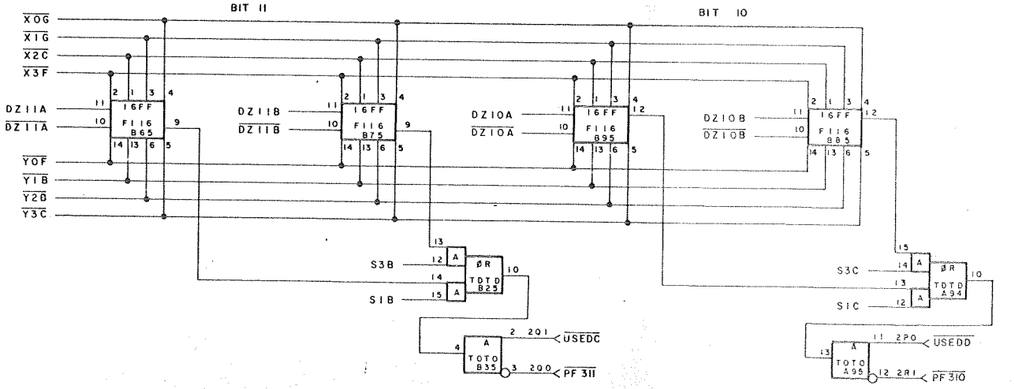
CONTROL DATA CORPORATION — DEVELOPMENT DIVISION	TITLE: PAGE FILE QUAD. 3 ADDRESSES XX6, XX7	PRODUCT	
	2A2A0 LOC. 2A2B0 PART NO. 185301 SER007	SIZE C / DRAWING NO. 60289500 / REV. W	
		SHEET / PAGE 4-49	

81

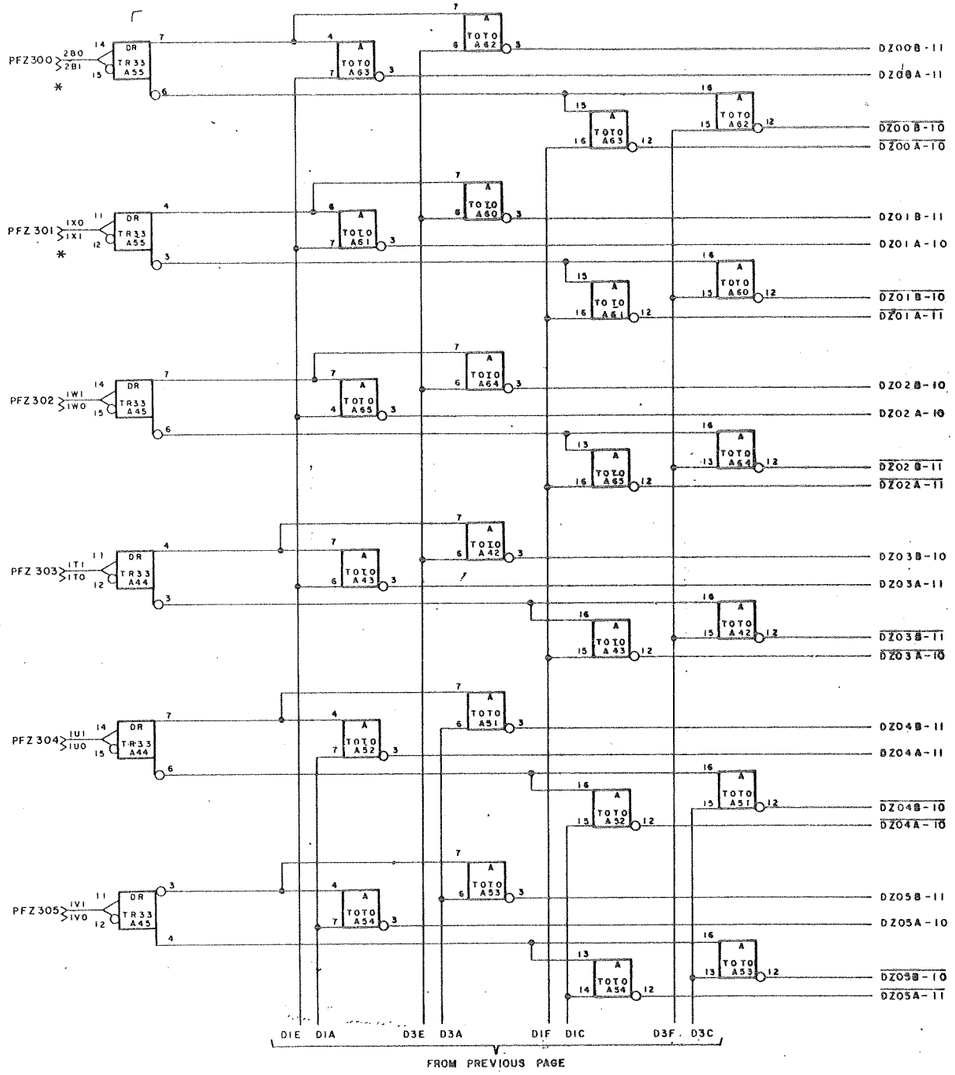


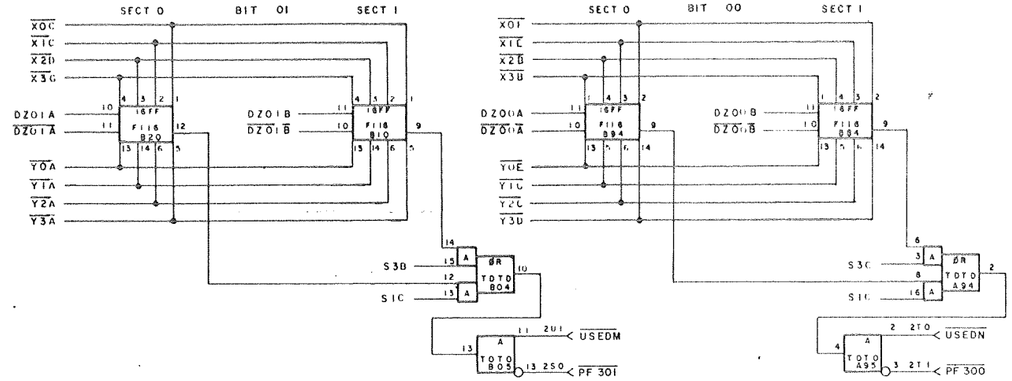


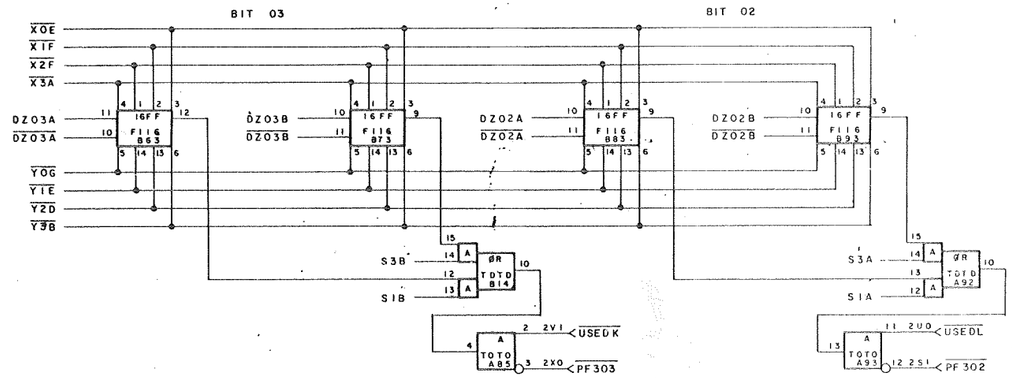


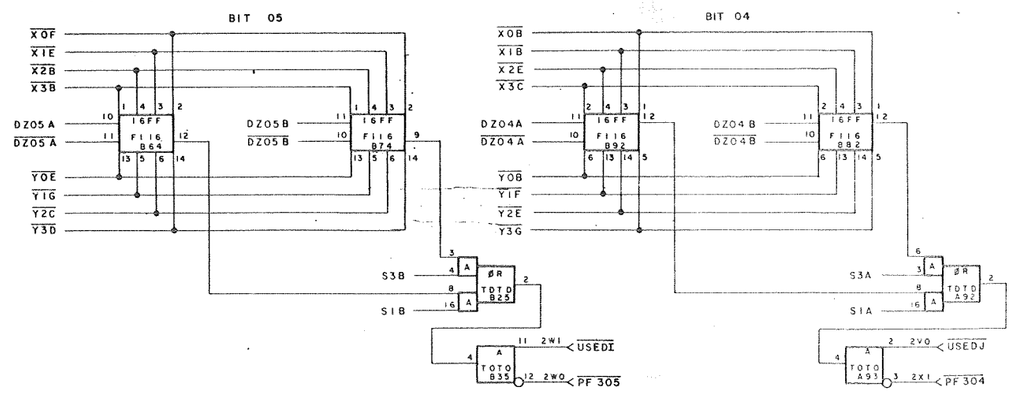


CONTROL DATA DEVELOPMENT DIVISION	TITLE PAGE FILE QUAD. 3 ADDRESSES XX6, XX7 2A2A0 LOC: 2A280 PART NO 185301 SER 007	SIZE C	DRAWING NO 60289500 REV W
		SHEET	PAGE 4-51





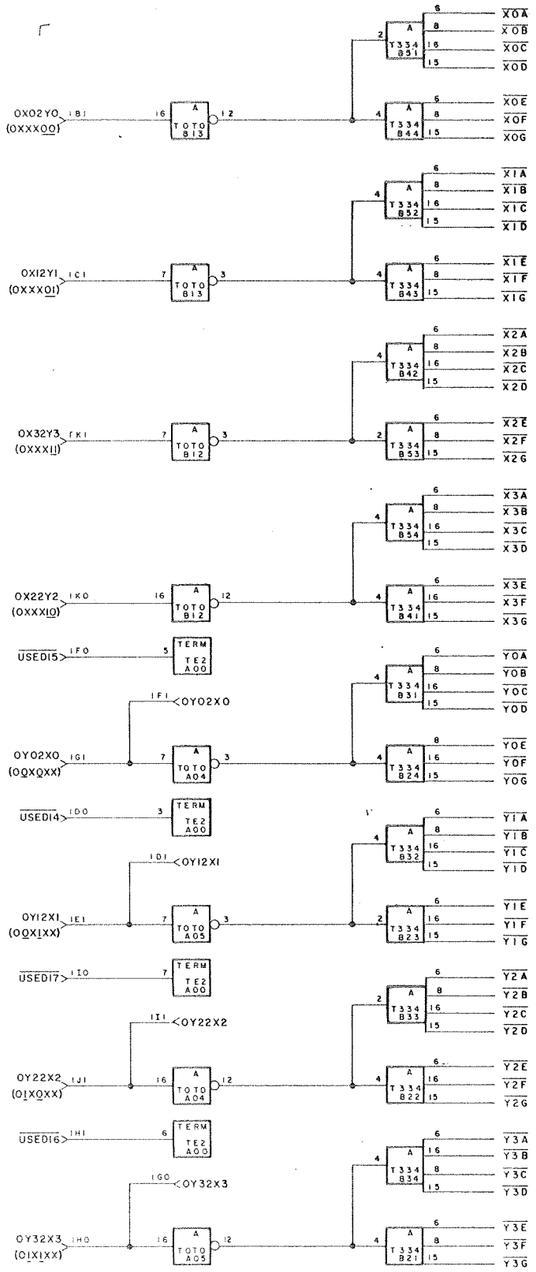


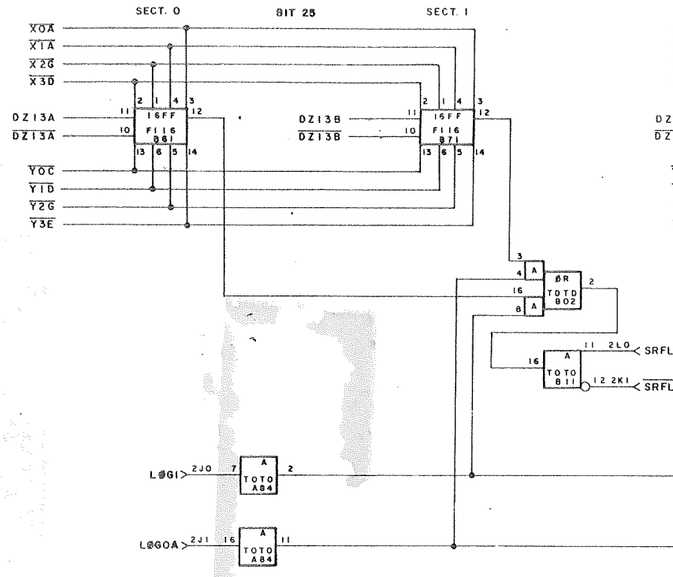


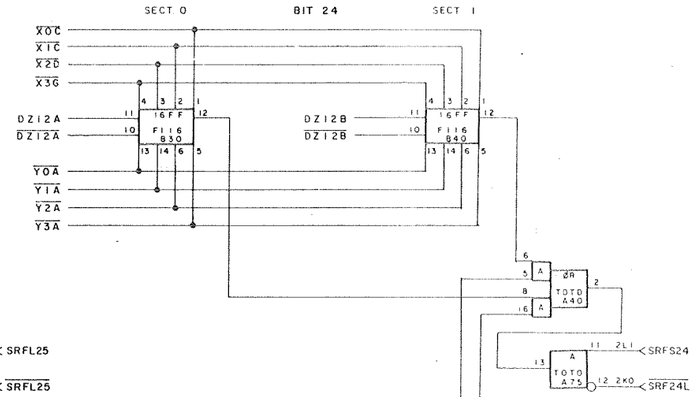
CONTROL DATA	TITLE	PRODUCT
DEVELOPMENT DIVISION	PAGE FILE QUAD. 3 ADDRESSES XX6, XX7 2A2A0 LOC: 2A2B0 PART NO 185301 SER 007	SIZE C DRAWING NO 60289500 REV W SHEET PAGE 4-53

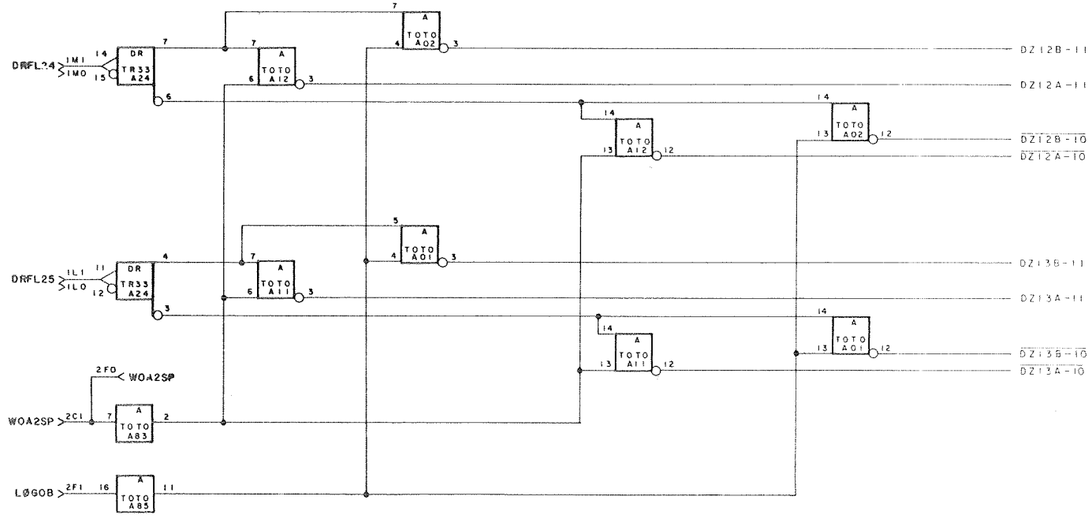
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
1R1	2A1A2-S1	5-67		S BITS 01/00 = 0 TO RF 00-37
	2A1A9-H1	5-59		
1C1	2A1A2-D1	5-67		S BITS 01/00 = 1 TO RF 00-37
	2A1A9-H0	5-59		
1D1	2A1A4-G1	5-59		S BITS 04/02 = 1 TO RF 00-37
1E1	2A1A2-C1	5-67		S BITS 04/02 = 1 TO RF 00-37
1F1	2A1A2-H1	5-67		S BITS 04/02 = 0 TO RF 00-37
1G0	2A1A9-K0	5-59		S BITS 04/02 = 3 TO RF 00-37
1G1	2A1A4-G0	5-59		S BITS 04/02 = 0 TO RF 00-37
1H0	2A1A2-K1	5-67		S BITS 04/02 = 3 TO RF 00-37
1J1	2A1A4-J0	5-59		S BITS 04/02 = 2 TO RF 00-37
1J1	2A1A2-K0	5-67		S BITS 04/02 = 2 TO RF 00-37
1K0	2A1A2-J1	5-67		S BITS 01/00 = 2 TO RF 00-37
	2A1A4-A0	5-59		
1K1	2A1A2-H0	5-67		S BITS 01/00 = 3 TO RF 00-37
	2A1A4-E1	5-59		
1L0	2A1A2-K2	5-23		
1L1	2A1A2-K2	5-23		DIGIT DRIVE 25 TO RF 00-37
1M0	2A1A2-J2	5-23		
1M1	2A1A2-J2	5-23		DIGIT DRIVE 24 TO RF 00-37
2C1	2A1A4-W0	5-59		WRITE RF 0X AND 2X CONT. BITS
2F0	2A1A2-F1	5-67		WRITE RF 1X AND 3X CONT. BITS
2K0	2A1A4-G1	5-57		SENSE RF 00-37 NOT(BIT 24)
2K1	2A1A4-D2	5-57		SENSE RF 00-37 NOT(BIT 25)
2L0	2A1A5-J1	5-55	2A1A4-W	SENSE REG FILE 00-37 BIT 25
2L1	2A1A4-K1	5-57		SENSE REG FILE 00-37 BIT 24

2-86A Rev. W Page 5-60



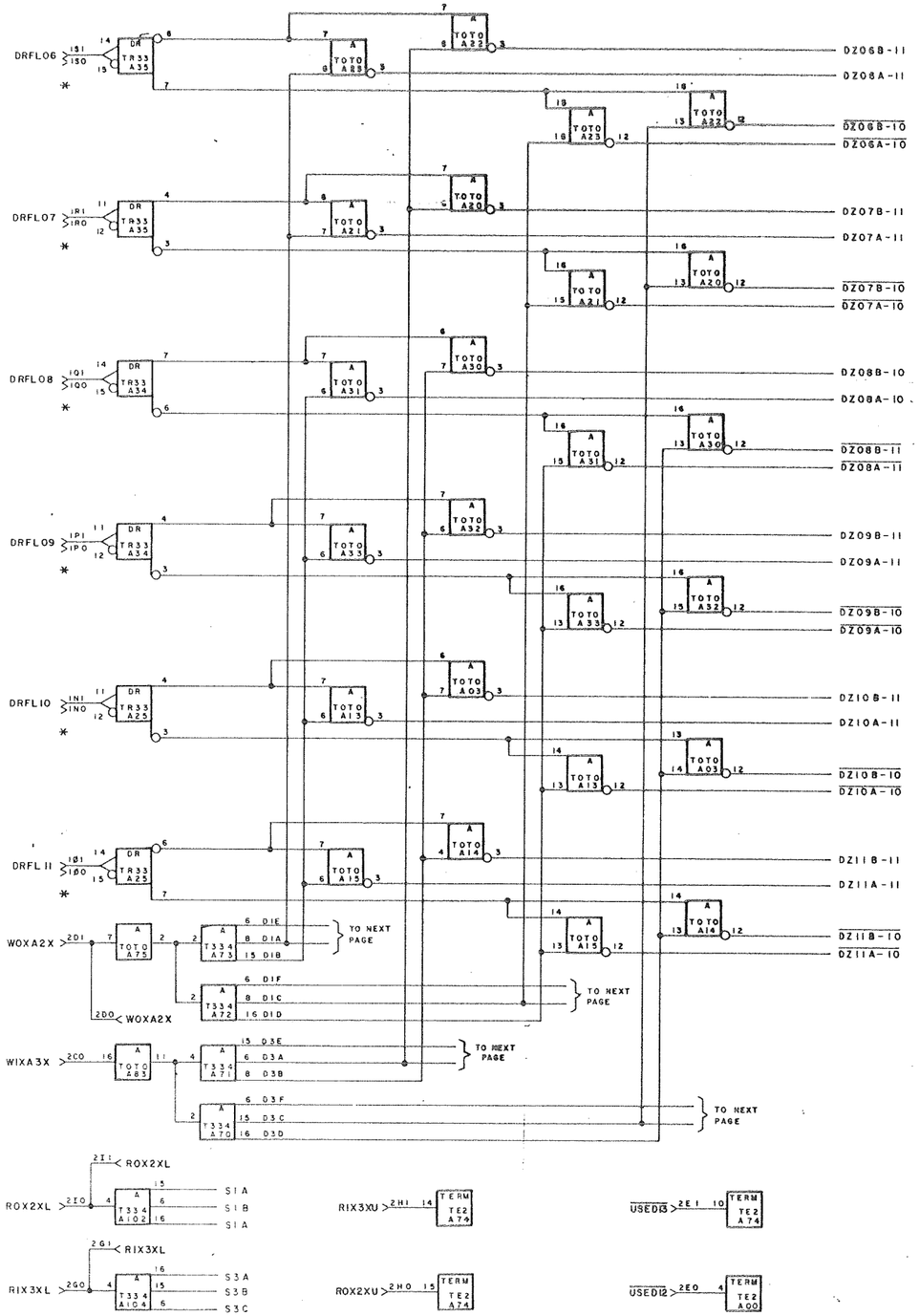


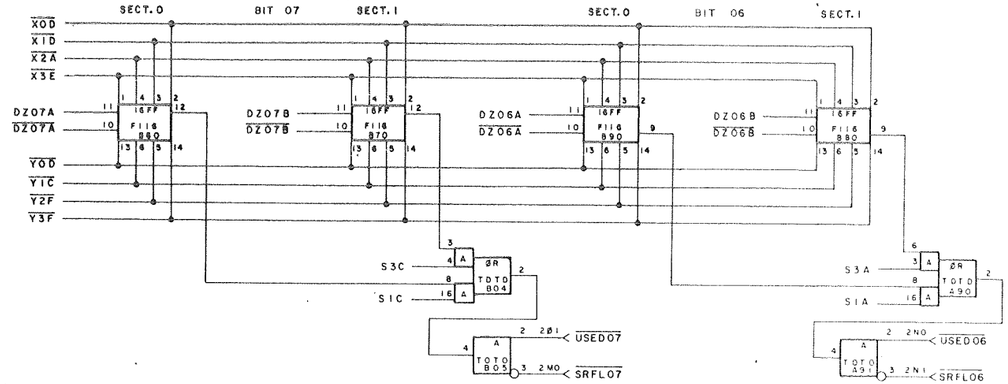


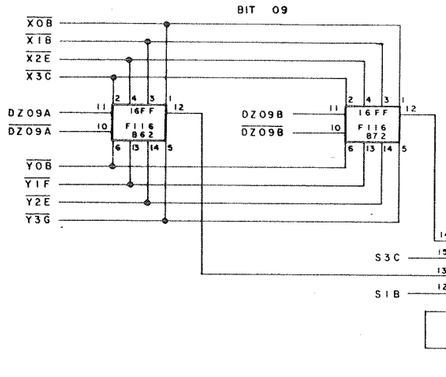


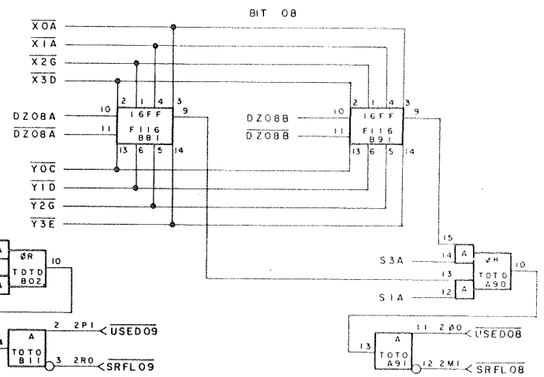
CONTROL DATA	TITLE: REGISTER FILE LOCATIONS 00-37 LWR 12 AND 2 CONT		PRODUCT
DEVELOPMENT DIVISION	LOC: 2A1A3, 2A1B3 PART NO.	SER 000	SIZE C · DRAWING NO. 60289500 · REV W SHEET · PAGE 5-61

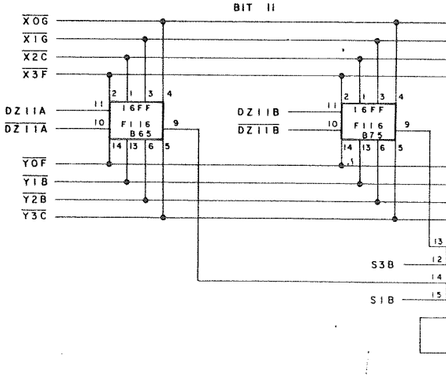
87

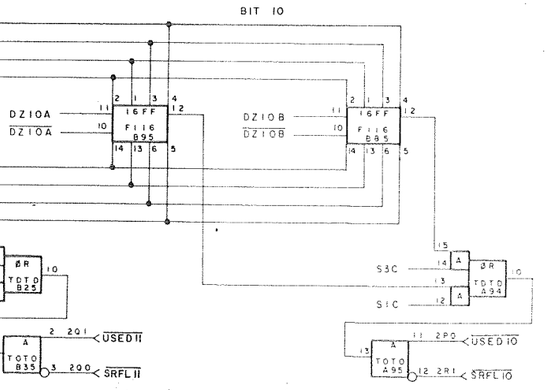




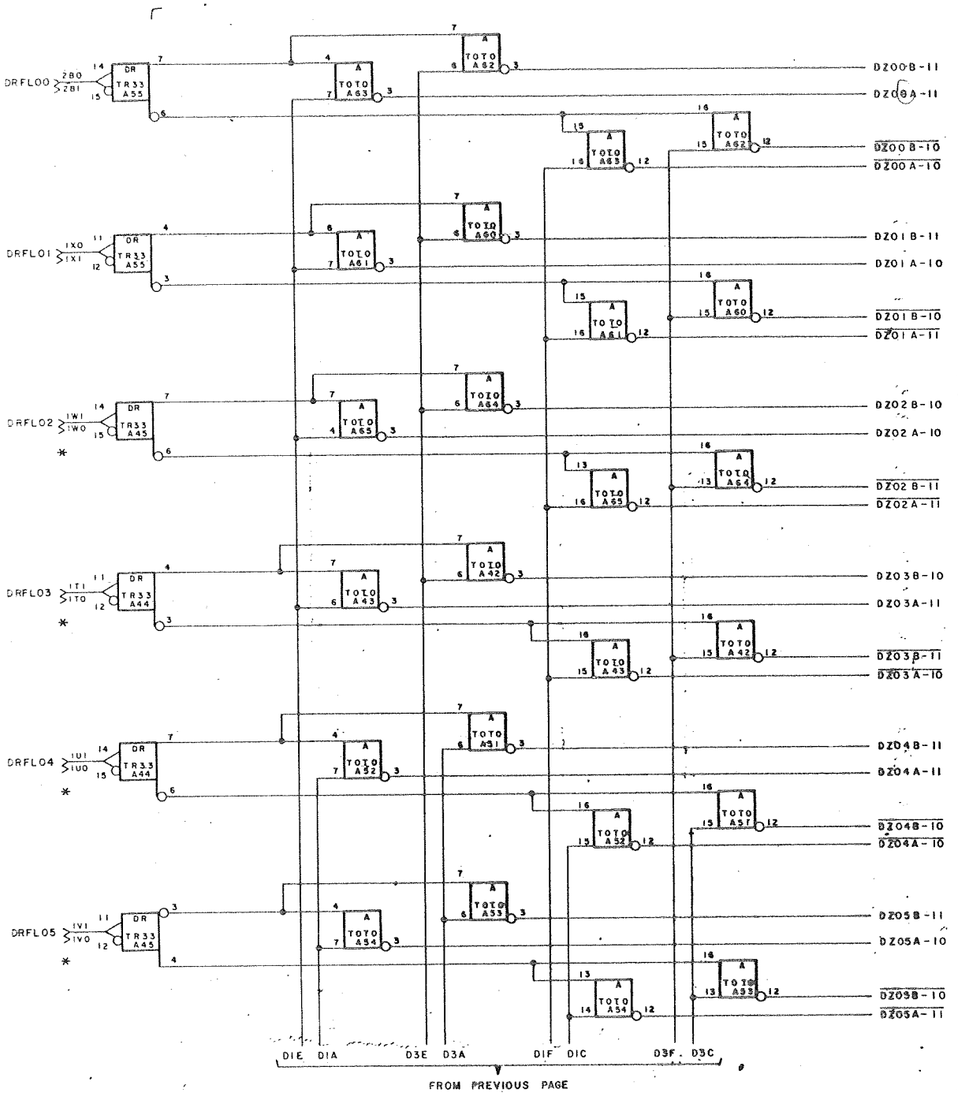


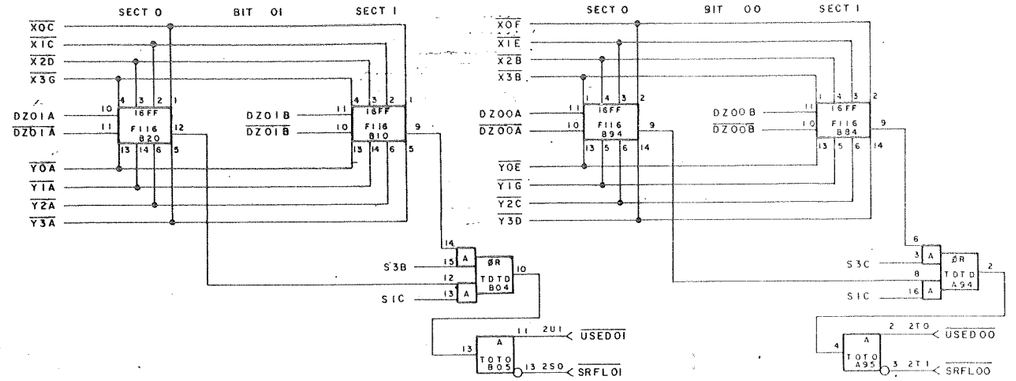


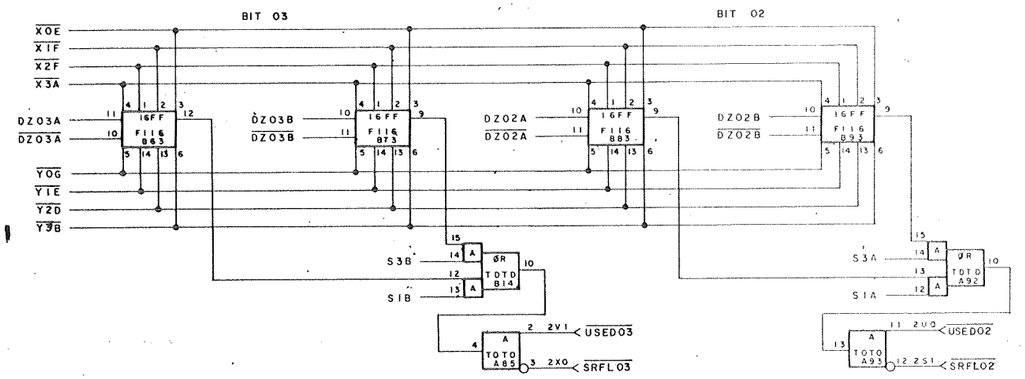


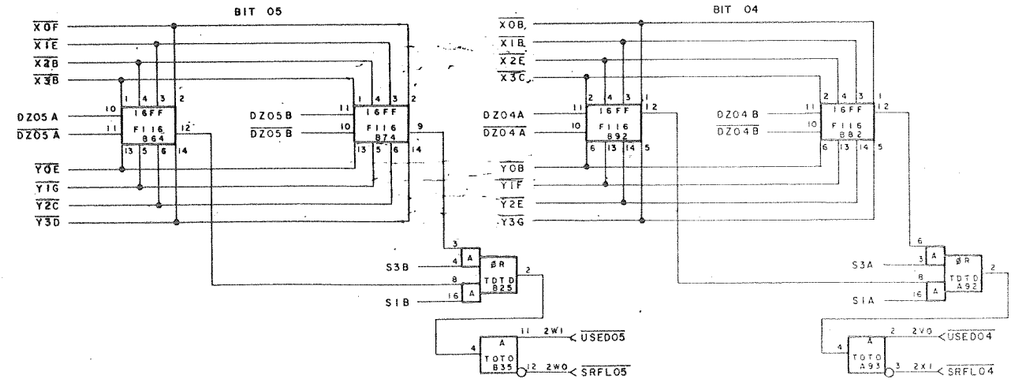


CONTROL DATA	TITLE: REGISTER FILE LOCATIONS 00-37 LOWER 12 AND 2 CONT 2AIA3 LOC: 2AIB3 PART NO.	SIZE: C	DRAWING NO: 60289500	REV: W
DEVELOPMENT DIVISION	SER. 000	SHEET	PAGE 5-63	









CONTROL DATA
DEVELOPMENT DIVISION

TITLE
REGISTER FILE
LOCATIONS 00-37
LOWER 12 AND 2 CONT
2A1A3
LOC: 2A183 PART NO SER 000

PRODUCT
SIZE C DRAWING NO 60289500 REV W
SHEET PAGE 5-65

```
                2A1A3-F1  5- 61          S BITS 04/02 = 0 TO RF 00-37
                2A1A4-G0  5- 59
                2A1A3-E1  5- 61          S BITS 04/02 = 1 TO RF 00-37
                2A1A4-G1  5- 59
                2A1A3-C1  5- 61          S BITS 01/00 = 1 TO RF 00-37
                2A1A4-H0  5- 59          S BITS 01/00 = 1 TO RF 00-37
                2A1A4-H1  5- 59          S BITS 01/00 = 0 TO RF 00-37
                2A1A4-E1  5- 59          S BITS 01/00 = 3 TO RF 00-37
                2A1A3-D1  5- 61          S BITS 01/00 = 0 TO RF 00-37
                2A1A3-K1  5- 61          S BITS 01/00 = 3 TO RF 00-37
                2A1A4-A0  5- 59          S BITS 01/00 = 2 TO RF 00-37
                2A1A3-K0  5- 61          S BITS 01/00 = 2 TO RF 00-37
                2A1A3-G1  5- 61          S BITS 04/02 = 2 TO RF 00-37
                2A1A4-J0  5- 59
                2A1A3-H0  5- 61          S BITS 04/02 = 3 TO RF 00-37
                2A1A4-K0  5- 59
                2S1A7-F2  5-  1
                2B1A7-F3  5-  1          DIGIT DRIVE 27 TO RF 00-37
                2B1A9-T3  5- 23
                2A1A9-T2  5- 23          DIGIT DRIVE 26 TO RF 00-37
                2A1A3-F2  5- 61          WRITE RF 0X AND 2X  CONT. BITS
                2A1A4-H0  5- 59
                2A1A4-K0  5- 57          SENSE RF 00-37 NOT(BIT 26)
                2A1A4-J1  5- 57          SENSE RF 00-37 NOT(BIT 27)
                2A1A4-J0  5- 57          SENSE REG FILE 00-37  BIT 27
                2A1A8-Q1  5- 55  2A1A8-A0  SENSE REG FILE 00-37  BIT 26
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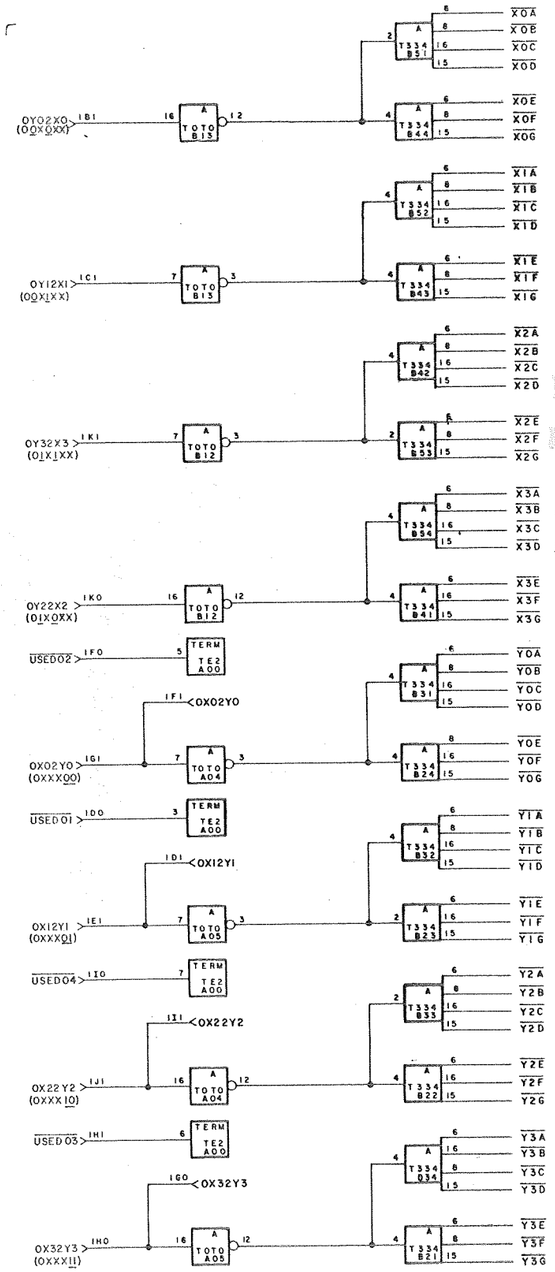
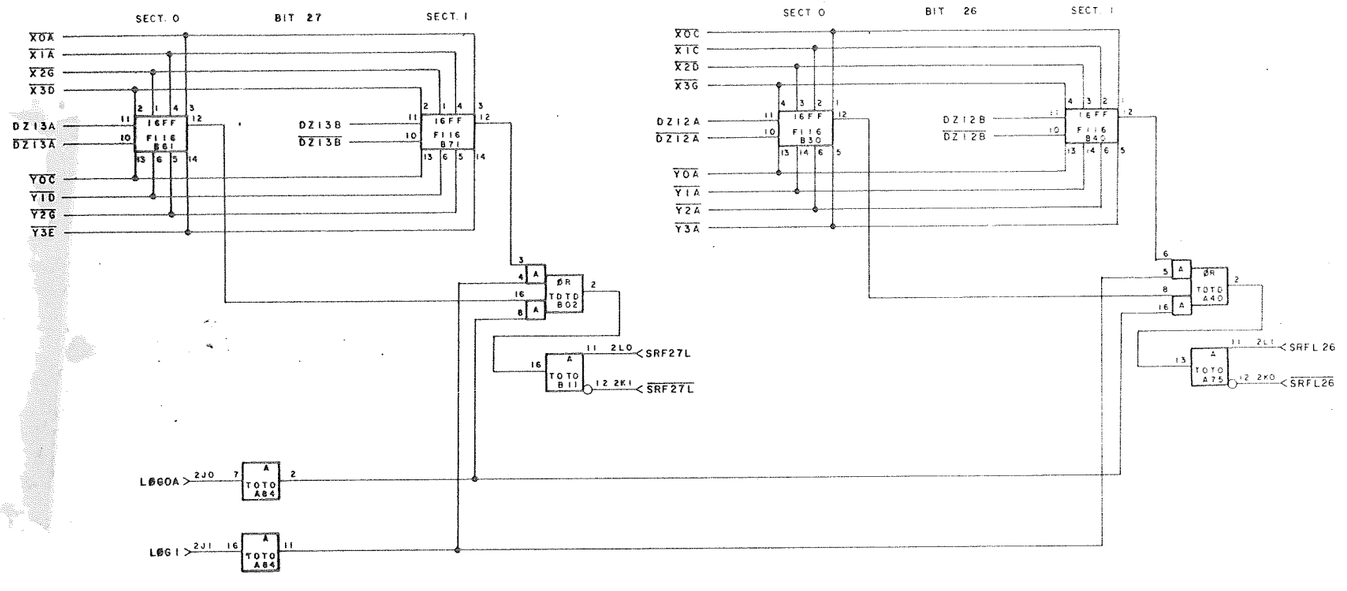
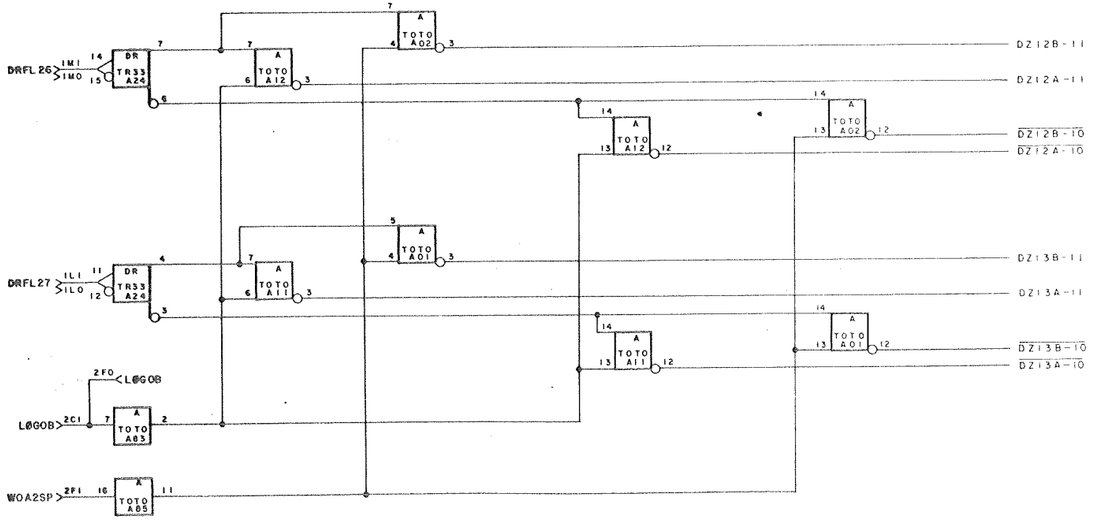
2-92A Rev W 5-66

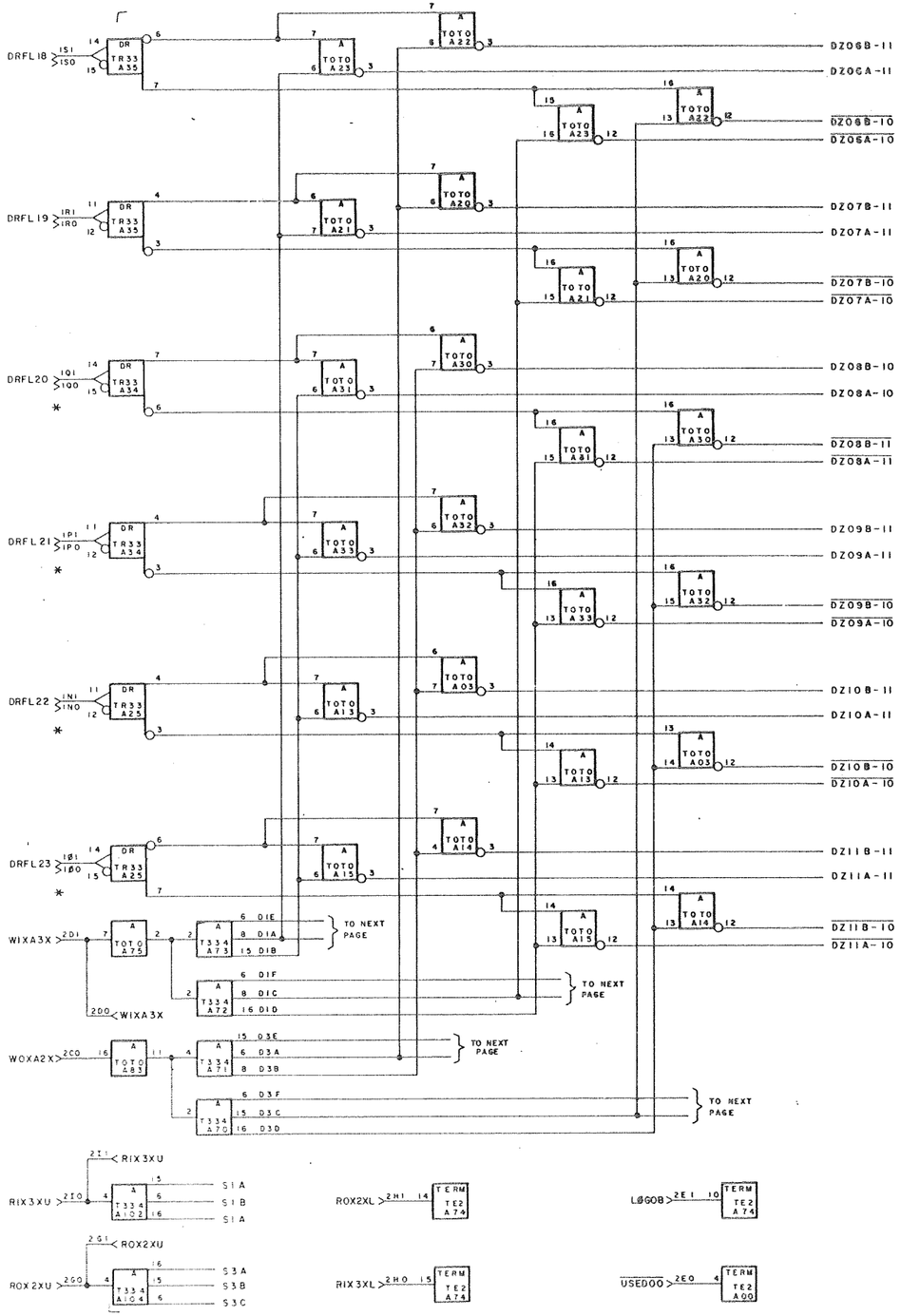


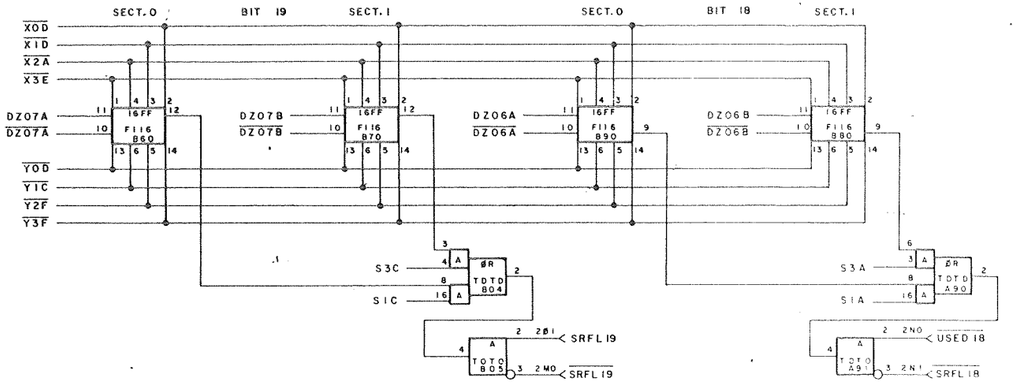


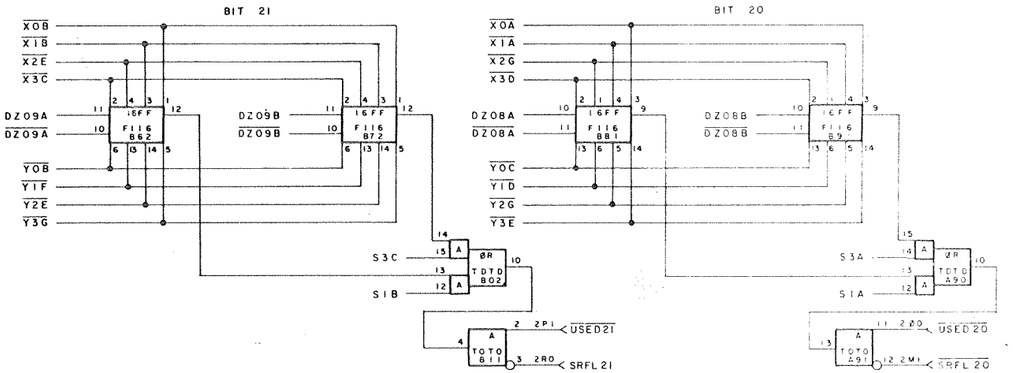


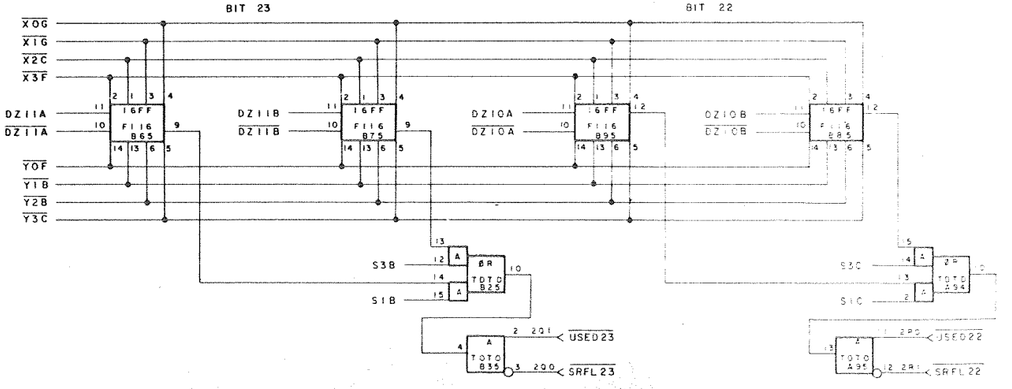
93

CONTROL DATA	TITLE	PRODUCT
DEVELOPMENT DIVISION	REGISTER FILE LOCATIONS 00-37 UPPER 12 AND 2 CONT	SIZE C · DRAWING NO. 60289500 · REV. W
LOC: 2A1A2, 2A1B2 PART NO.	SER 001	SHEET · PAGE 5-67









CONTROL DATA
DEVELOPMENT DIVISION

TITLE
REGISTER FILE
LOCATIONS 00-37
UPPER 12 AND 2 CONT
2AIA2
LOC: 2AIB2 PART NO.

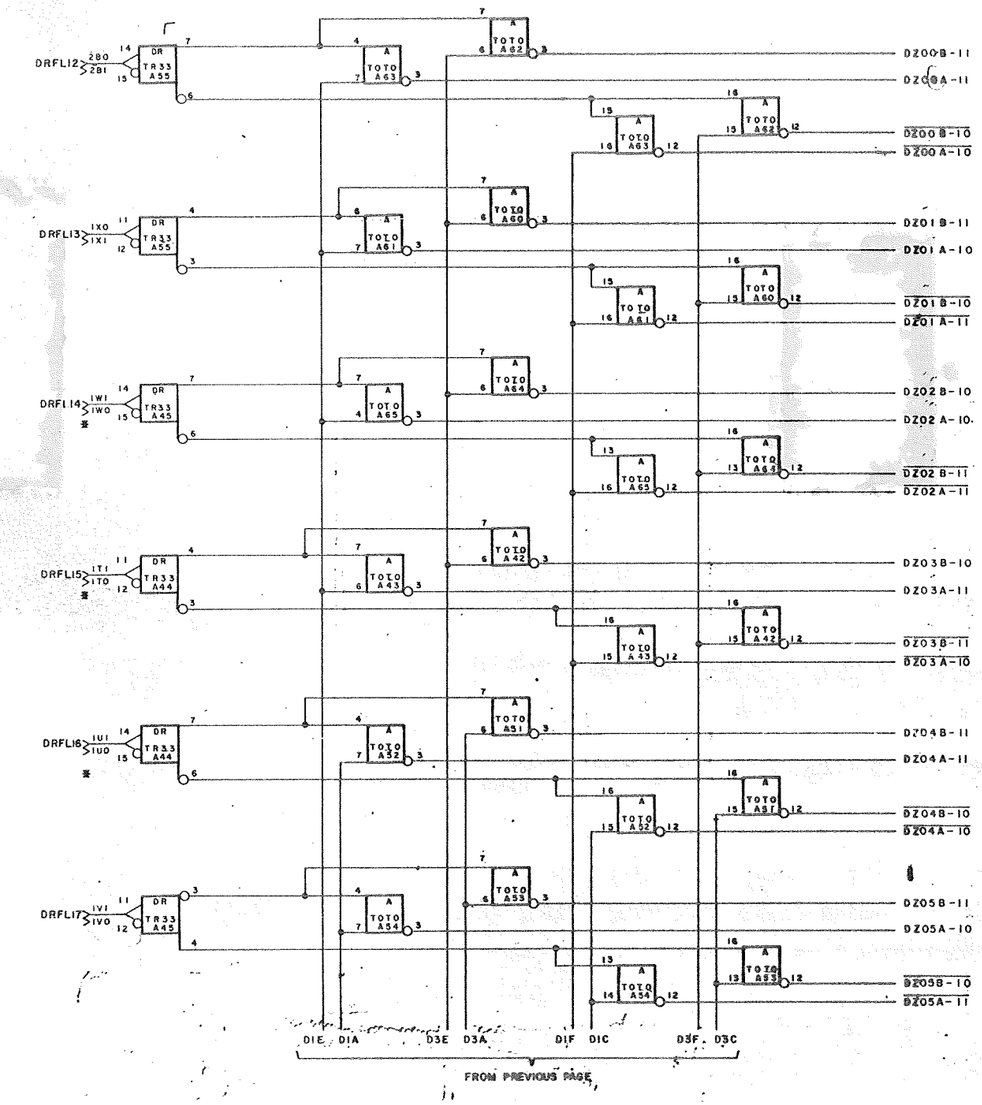
SIZE C | DRAWING NO 60289500 | REV W
SHEET | PAGE 5-69

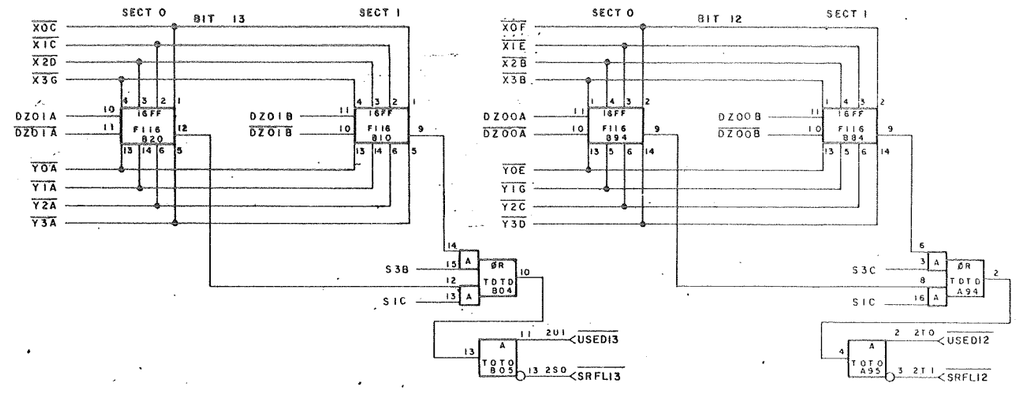
95

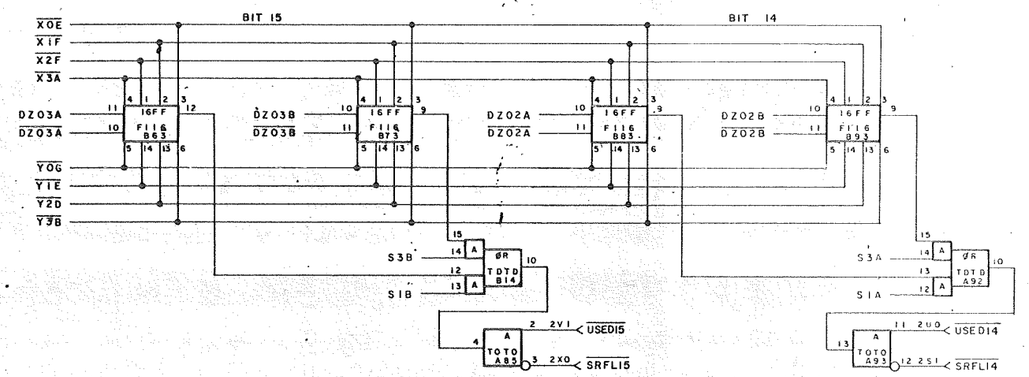
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
	2A1A0-F1	5- 79		S BITS 01/00 = 0 TO RF 40-77
181	2A1A4-E0	5- 59		S BITS 01/00 = 1 TO RF 40-77
	2A1A0-E1	5- 79		
1C1	2A1A4-R0	5- 59		S BITS 04/02 = 1 TO RF 40-77
	2A1A4-L0	5- 59		S BITS 04/02 = 1 TO RF 40-77
1D1	2A1A0-C1	5- 77		S BITS 04/02 = 0 TO RF 40-77
1E1	2A1A0-B1	5- 77		S BITS 04/02 = 3 TO RF 40-77
1F1	2A1A4-N0	5- 59		S BITS 04/02 = 0 TO RF 40-77
1G0	2A1A4-F0	5- 59		S BITS 04/02 = 3 TO RF 40-77
1G1	2A1A0-K1	5- 77		S BITS 04/02 = 2 TO RF 40-77
1H0	2A1A4-K1	5- 59		S BITS 04/02 = 2 TO RF 40-77
1I1	2A1A0-K0	5- 77		S BITS 01/00 = 2 TO RF 40-77
1J1	2A1A0-J1	5- 79		
1K0	2A1A4-F1	5- 59		S BITS 01/00 = 3 TO RF 40-77
	2A1A0-H0	5- 79		
1K1	2A1A4-J1	5- 59		

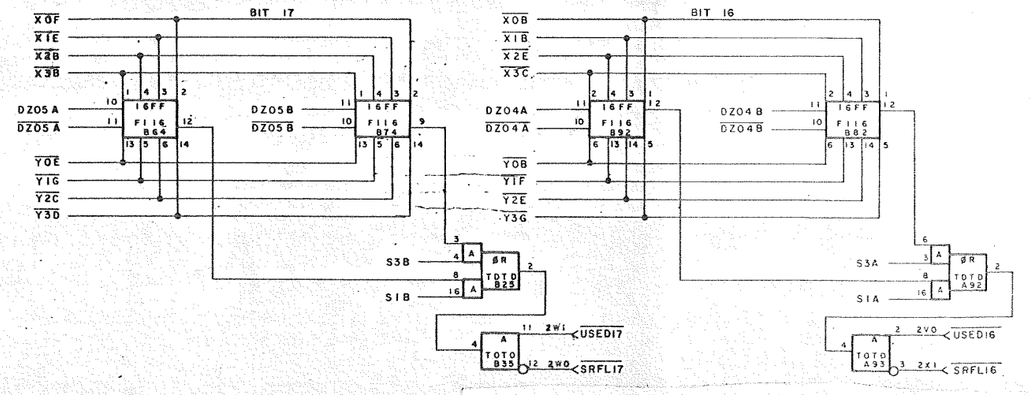
2-96A

Rev W
5-72

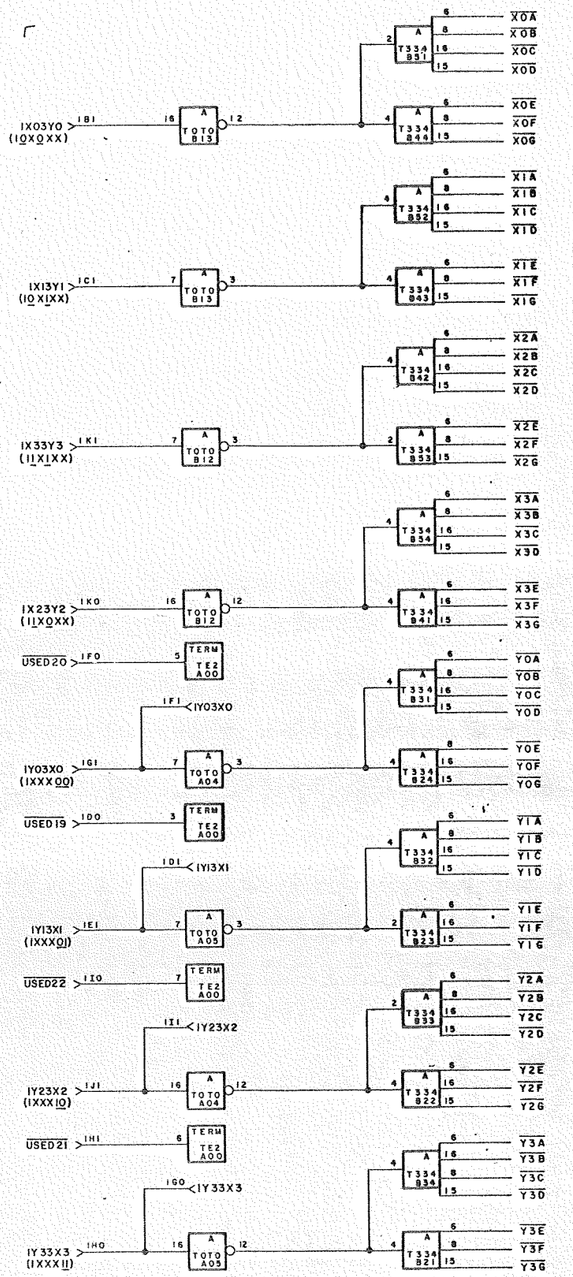


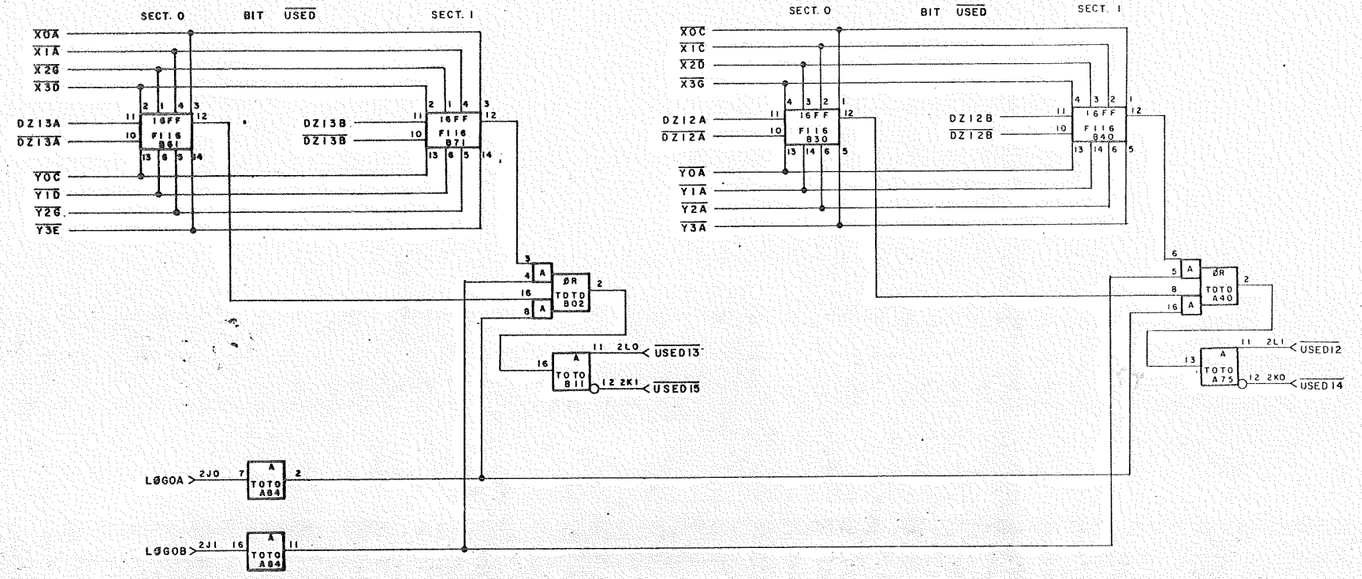


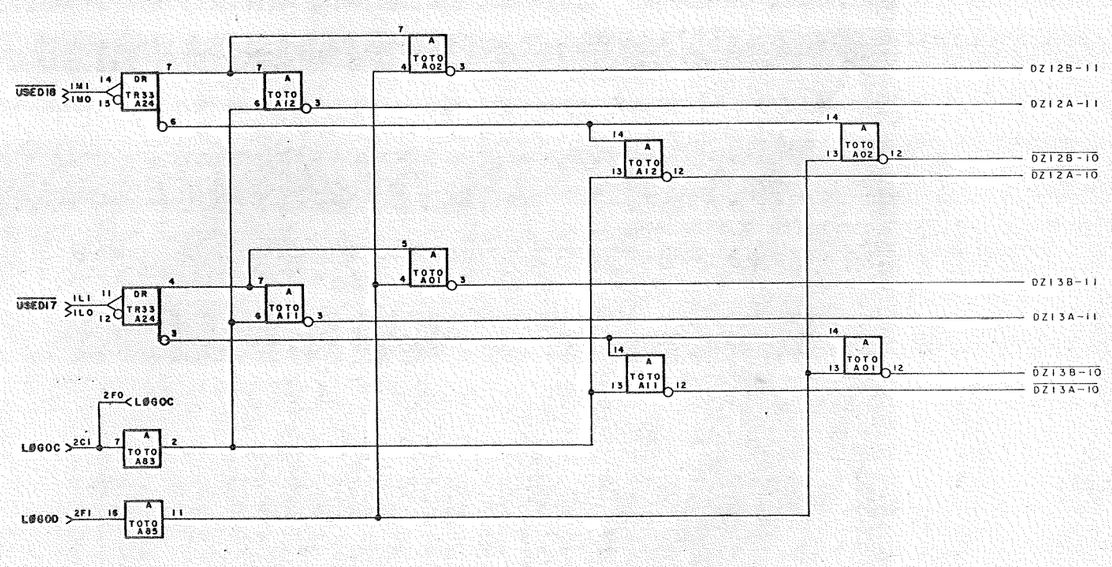




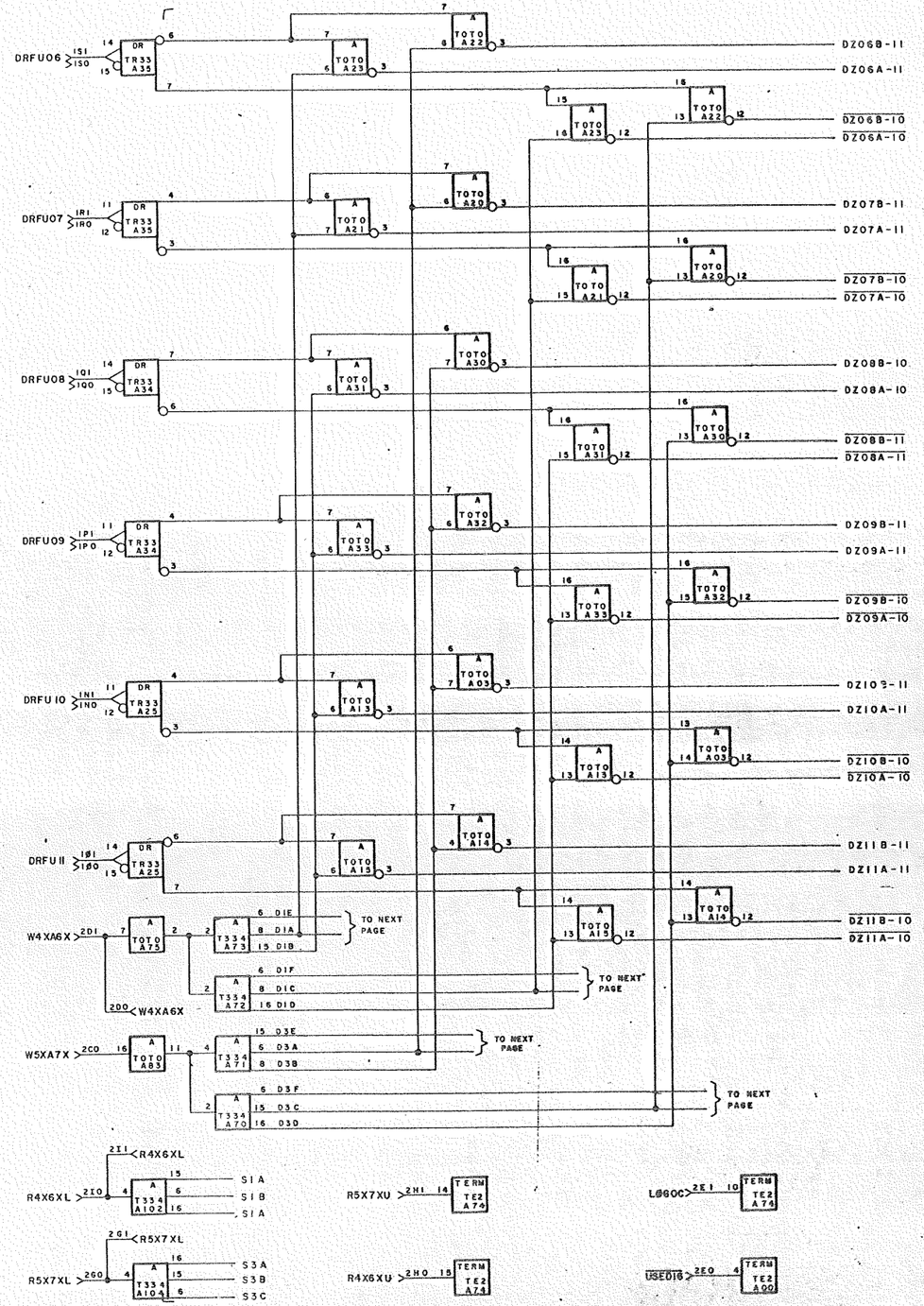
CONTROL DATA DEVELOPMENT DIVISION	TITLE: REGISTER FILE LOCATIONS 00-37 UPPER 12 AND 2 CONT 2A1A2 LOC: 2A1B2 PART NO 185301 SER 001	PRODUCT	
		SIZE C	DRAWING NO 60289500 REV W
		SHEET	PAGE 5-71

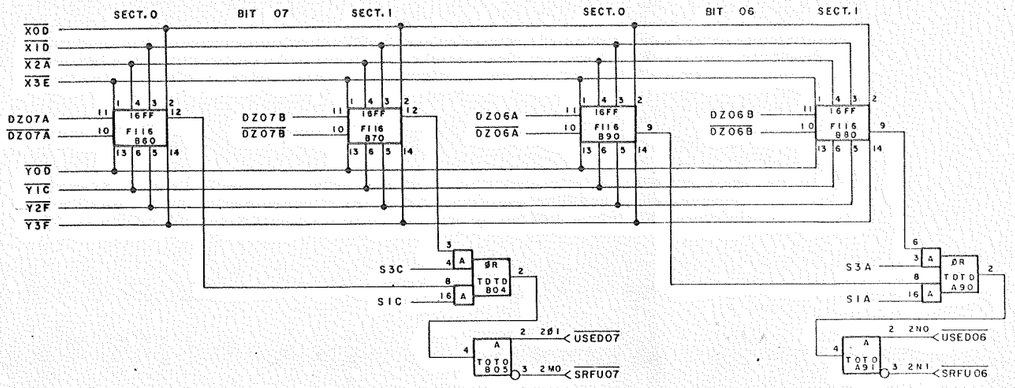


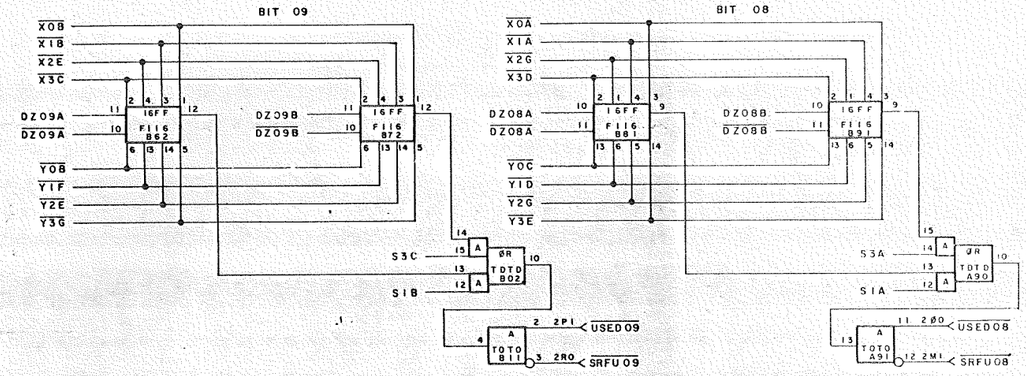


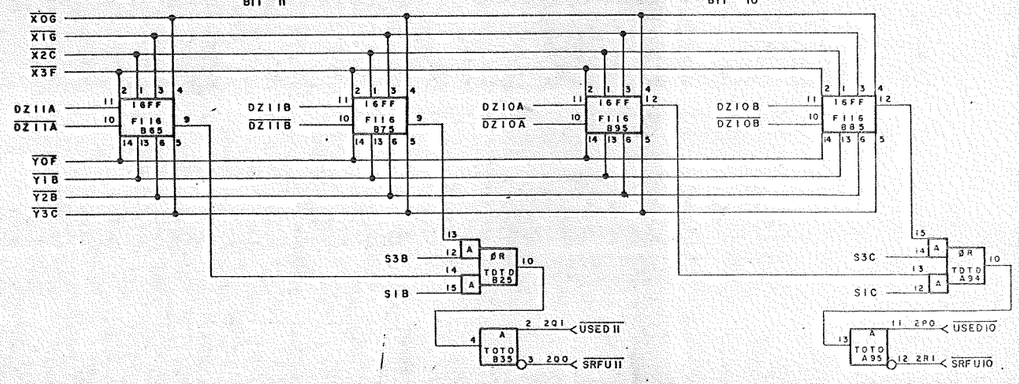


CONTROL DATA DEVELOPMENT DIVISION	TITLE: REGISTER FILE LOCATIONS 40-77 LOWER 12	PRODUCT	
	LOC:2AIA1, 2AIBI PART NO.18530I. SER002	SIZE C / DRAWING NO. 60289500	REV. W
		SHEET	PAGE 5-73



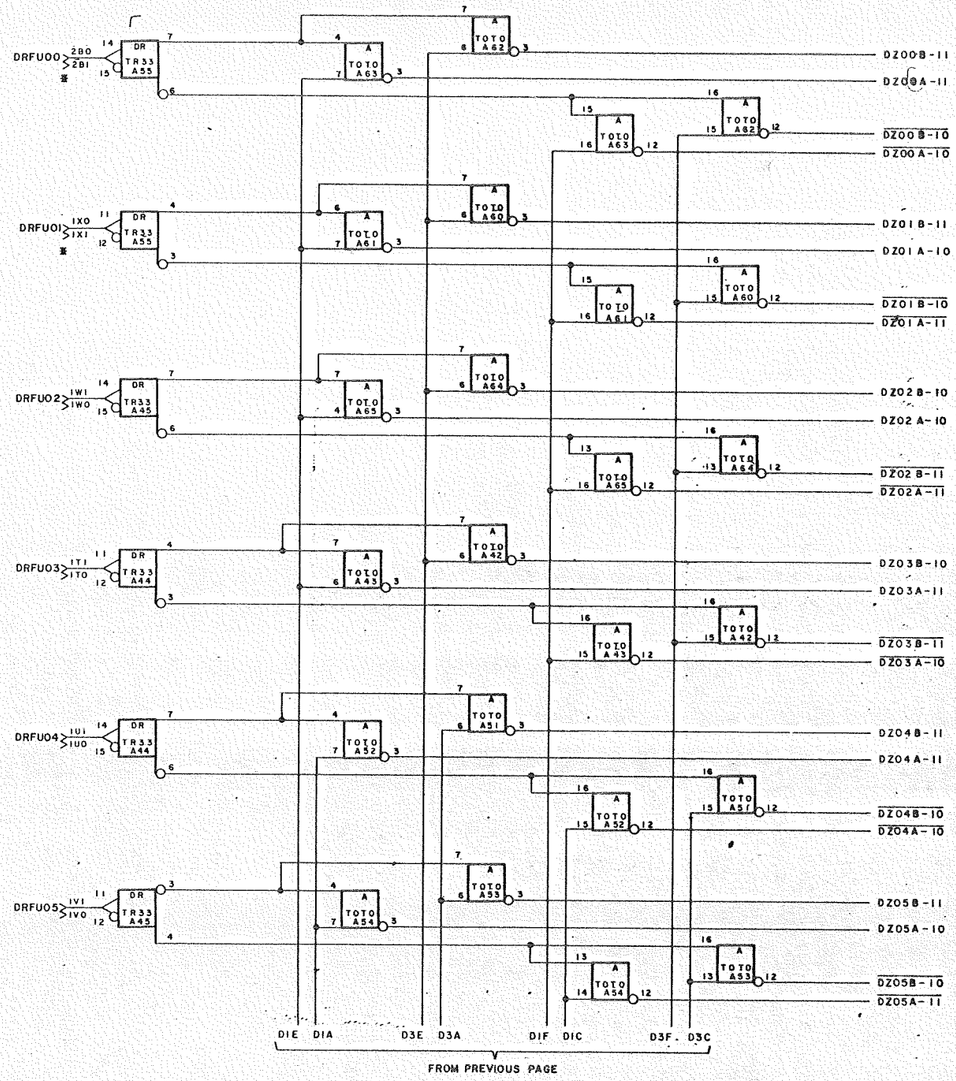


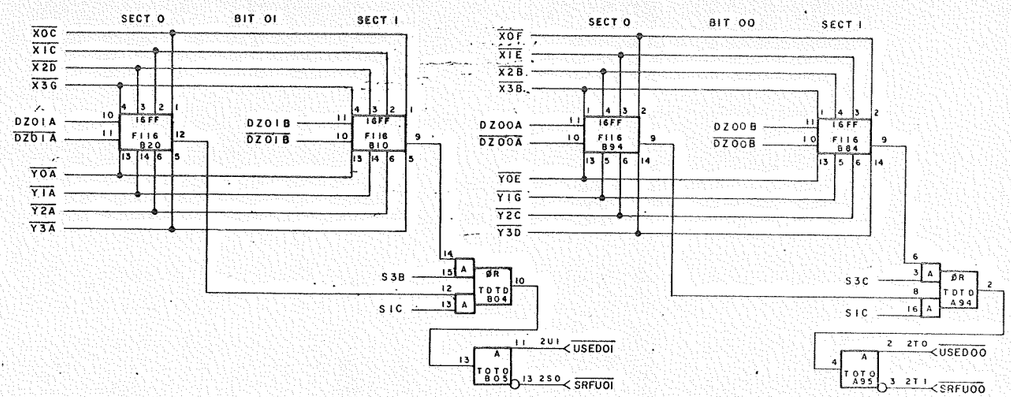


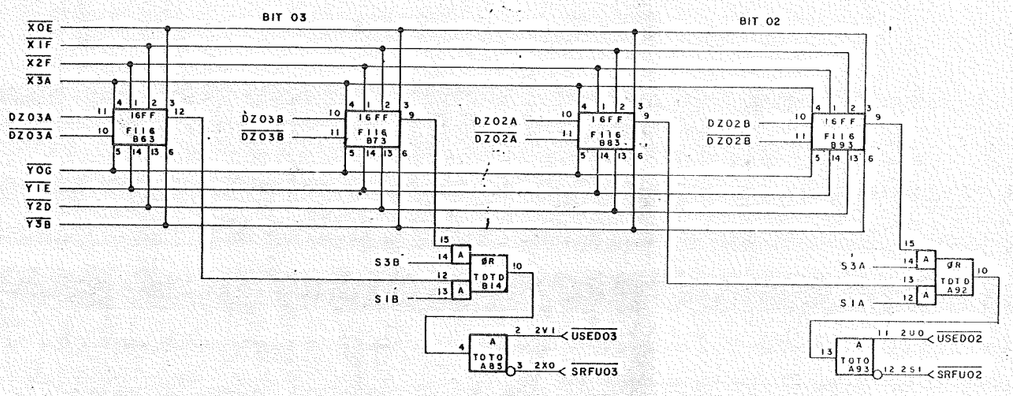


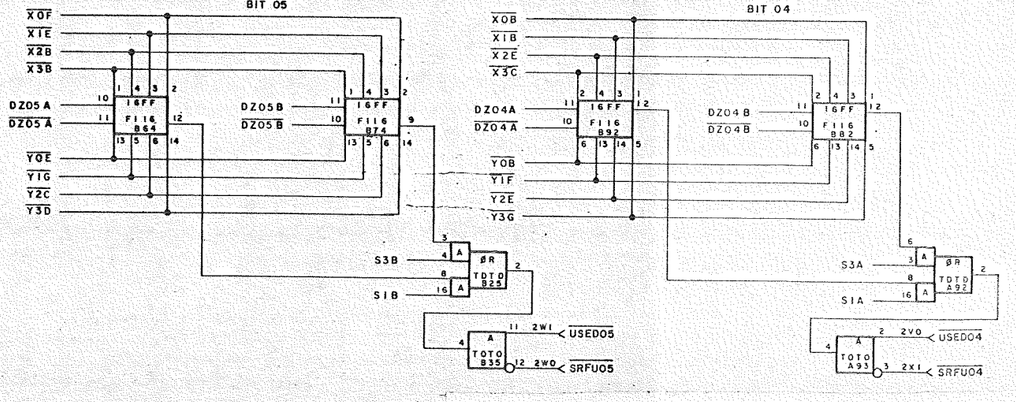
CONTROL DATA	TITLE: REGISTER FILE LOCATIONS 40-77 LOWER 12 2A1A1 LOC: 2A1B1 PART NO: 185301 SER 002	SIZE: C	DRAWING NO: 60289500 REV: W
DEVELOPMENT DIVISION		SHEET	PAGE: 5-75

101









CONTROL DATA	TITLE: REGISTER FILE LOCATIONS 40-77 LOWER I2 2A1A1	PRODUCT	
DEVELOPMENT DIVISION	LOC: 2A1B1 PART NO 185301 SER 002	SIZE C	DRAWING NO 60289500 REV W
		SHEET	PAGE 5-77

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        2A1A4-F0  S- 59
1C1     2A1A1-E1  S- 77     S BITS 04/02 = 1 TO BF 40-77
        2A1A4-C1  S- 59
1D1     2A1A4-D0  S- 59     S BITS 01/00 = 1 TO BF 40-77
1F1     2A1A1-C1  S- 77     S BITS 01/00 = 1 TO BF 40-77
1F1     2A1A1-B1  S- 77     S BITS 01/00 = 0 TO BF 40-77
1G0     2A1A4-J1  S- 59     S BITS 01/00 = 3 TO BF 40-77
1G1     2A1A4-E0  S- 59     S BITS 01/00 = 0 TO BF 40-77
1H0     2A1A1-K1  S- 77     S BITS 01/00 = 3 TO BF 40-77
1J1     2A1A4-F1  S- 59     S BITS 01/00 = 2 TO BF 40-77
1K0     2A1A1-K0  S- 77     S BITS 01/00 = 2 TO BF 40-77
        2A1A1-J1  S- 77     S BITS 04/02 = 2 TO BF 40-77
        2A1A4-K1  S- 59
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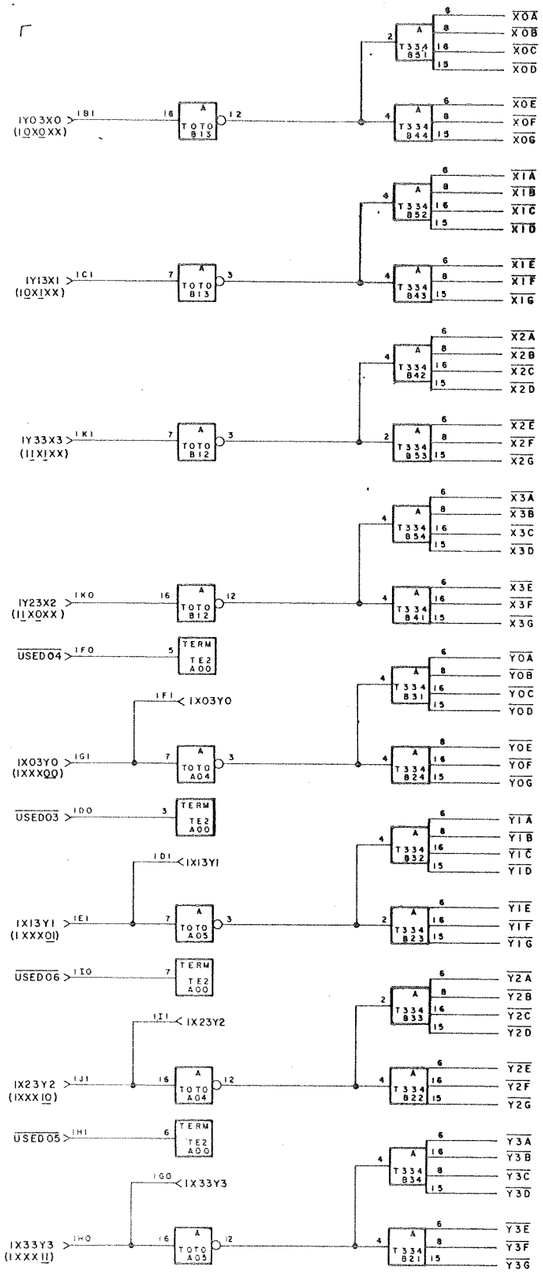
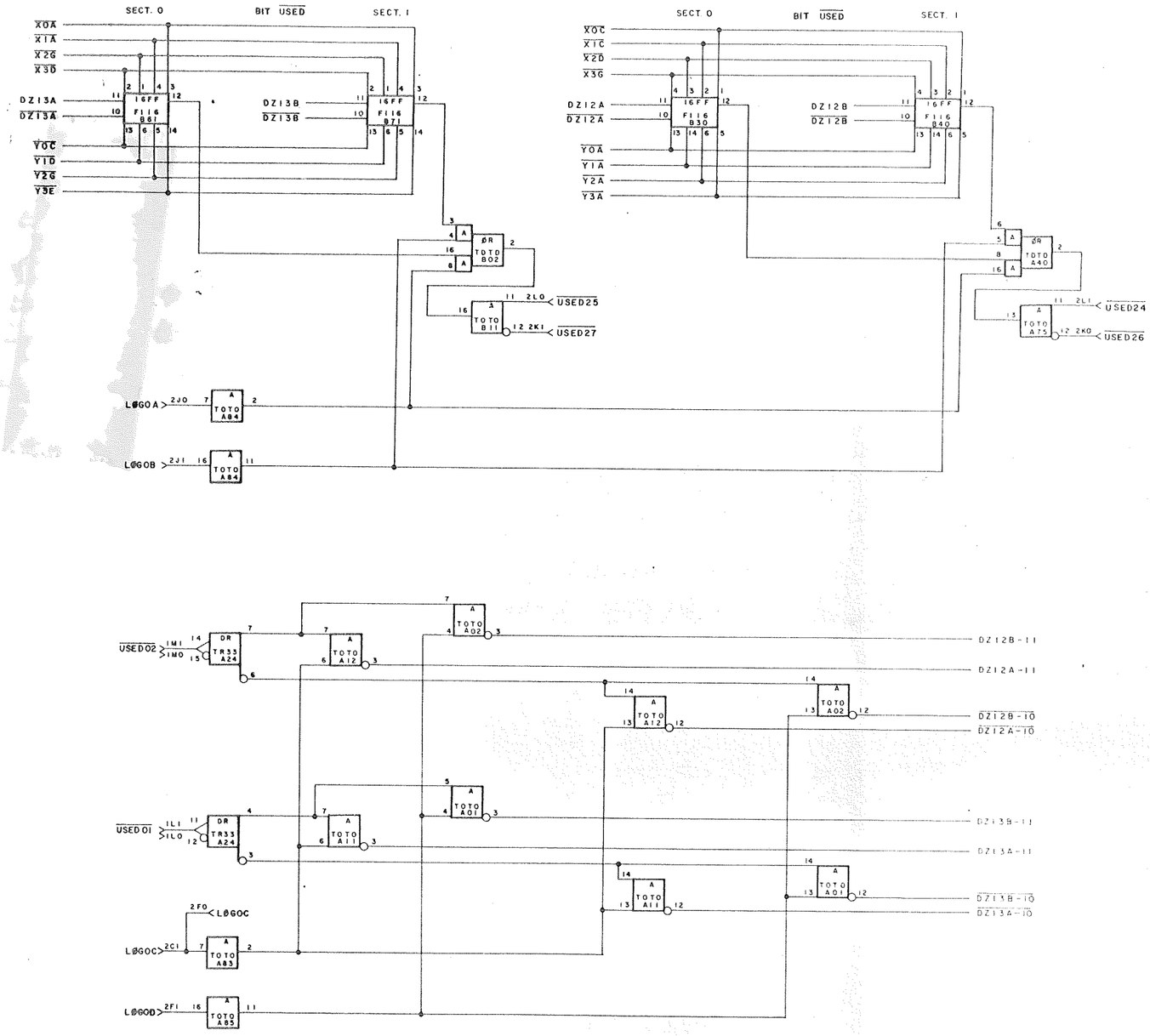
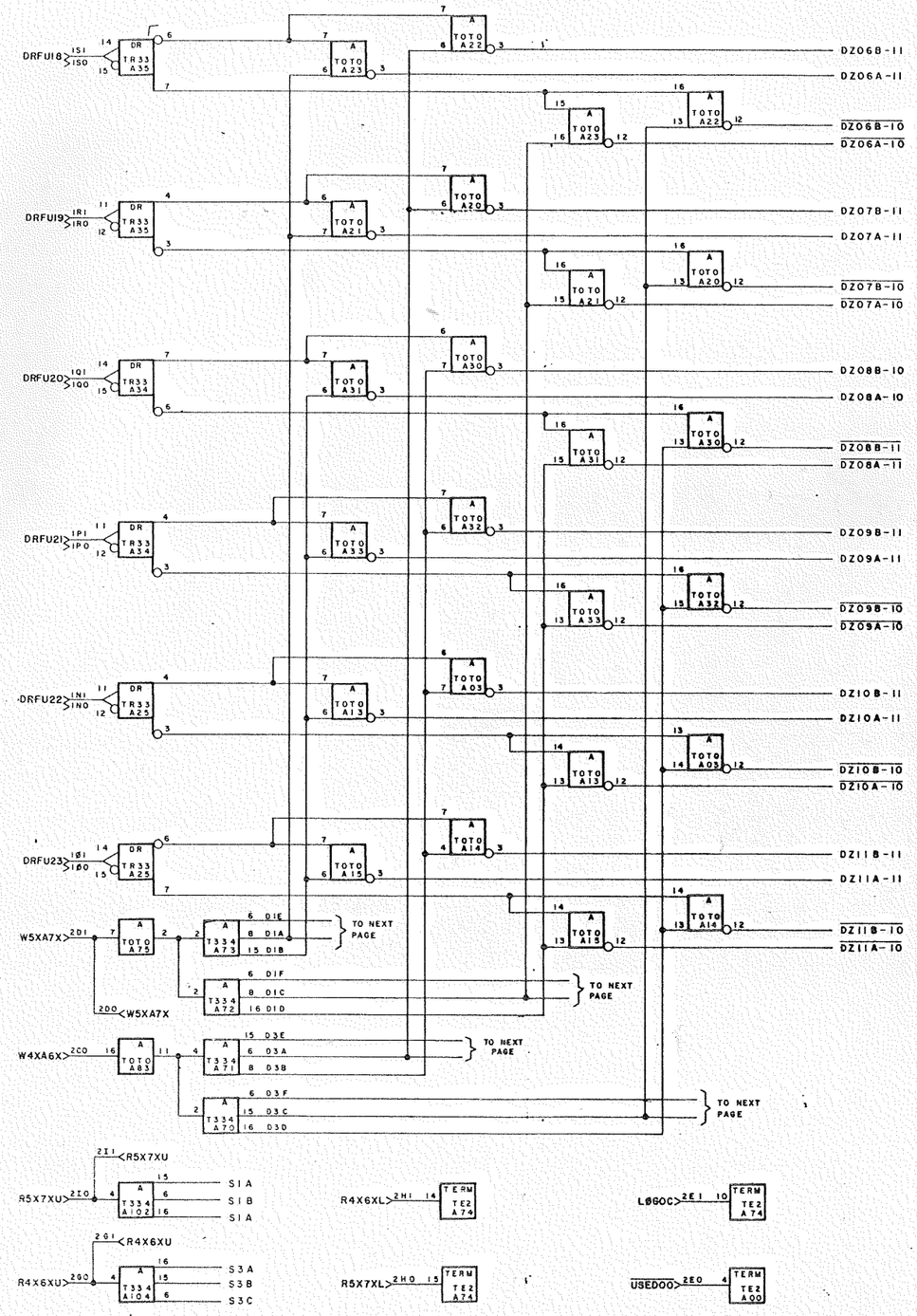
2-104A Rev W 5-78

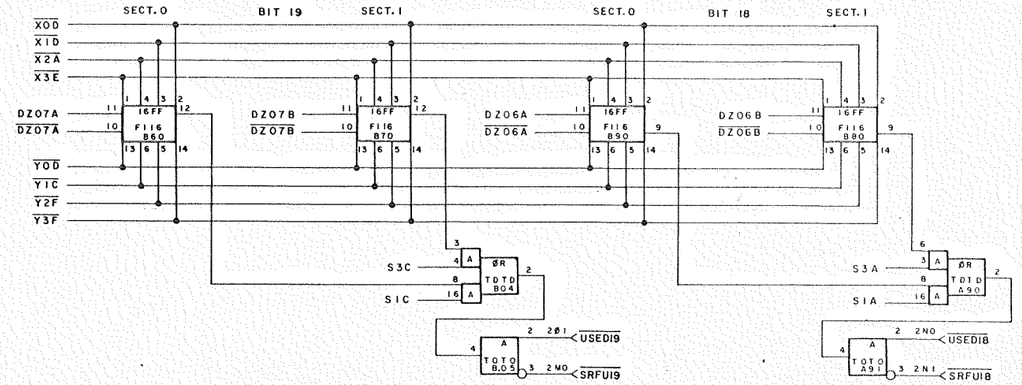


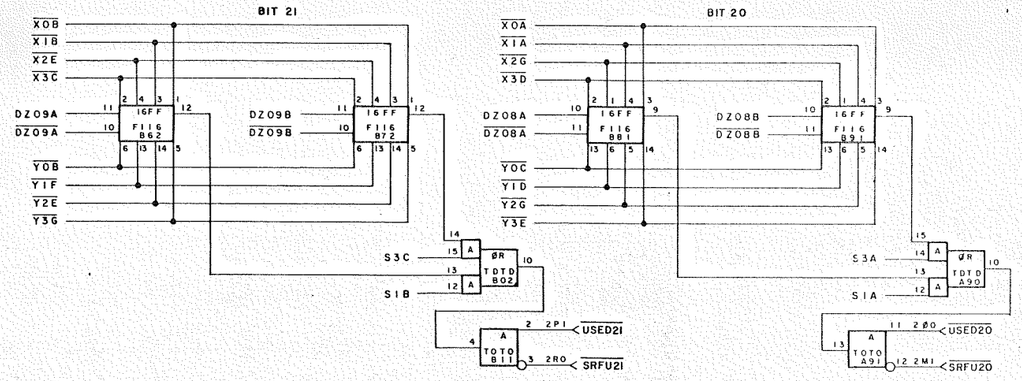


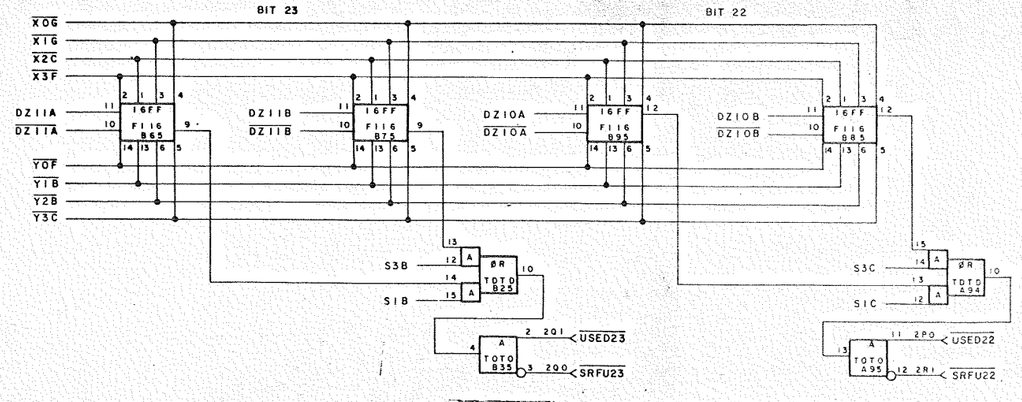
CONTROL DATA DEVELOPMENT DIVISION	TITLE: REGISTER FILE LOCATIONS 40-77 UPPER 12 LOC 2A1A0, 2A1B0 PART NO.	SERDC3	PRODUCT
		SIZE C	DRAWING NO. 60289500 REV. W
		SHEET	PAGE 5-79

05

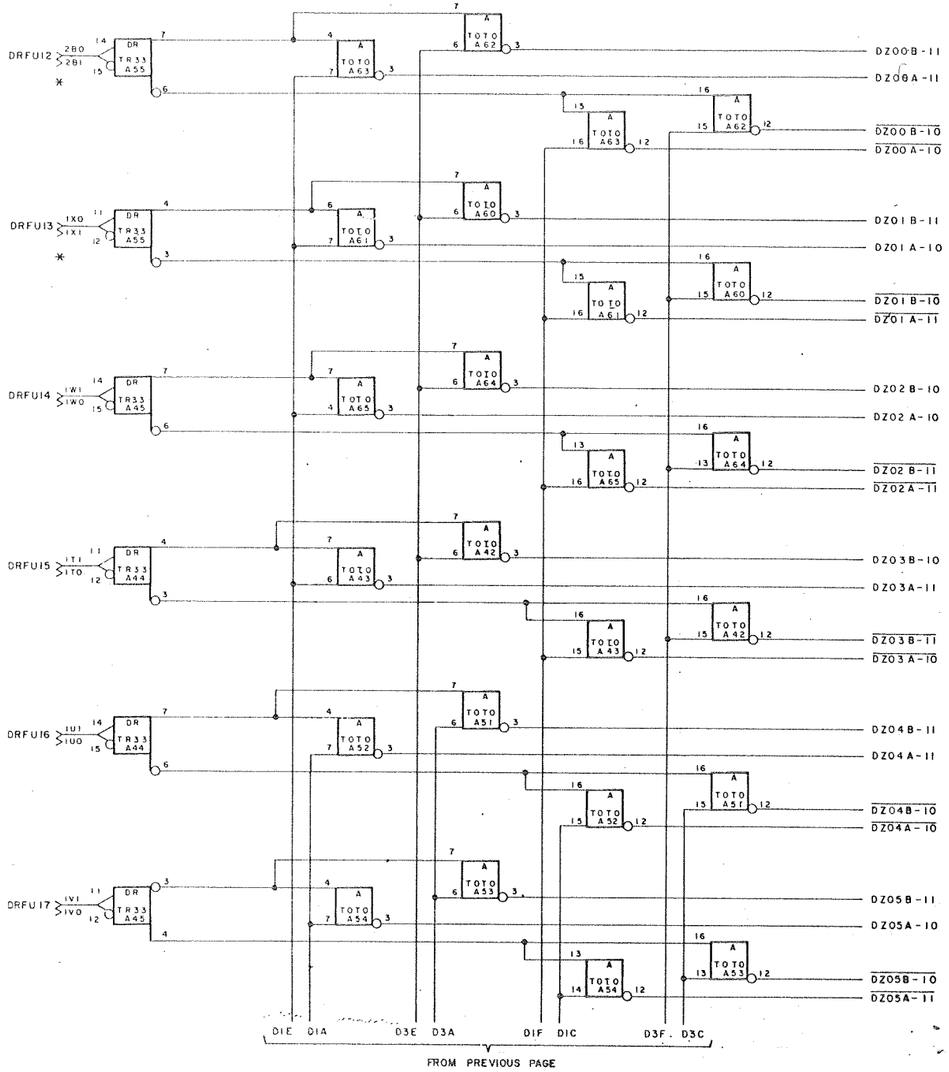


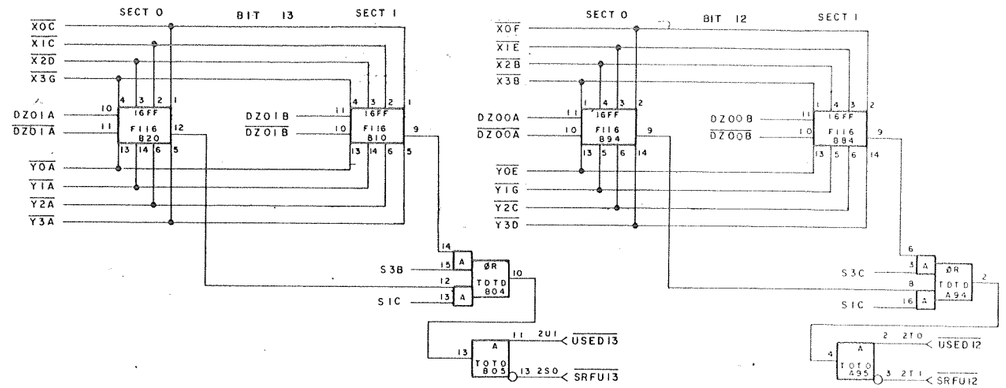


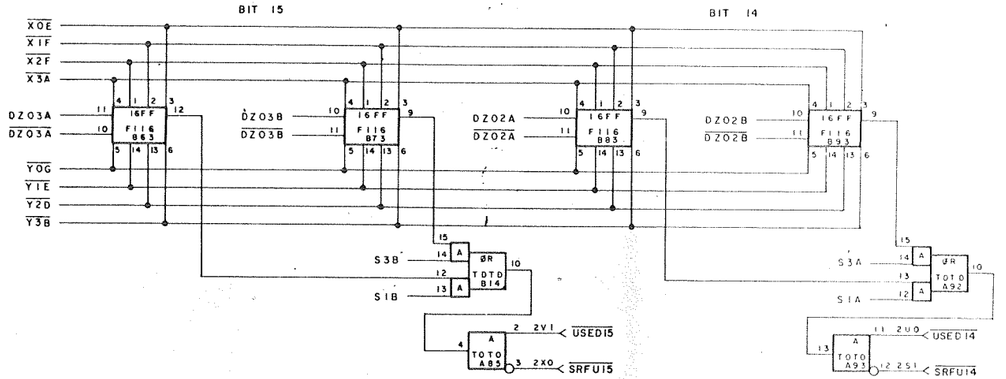


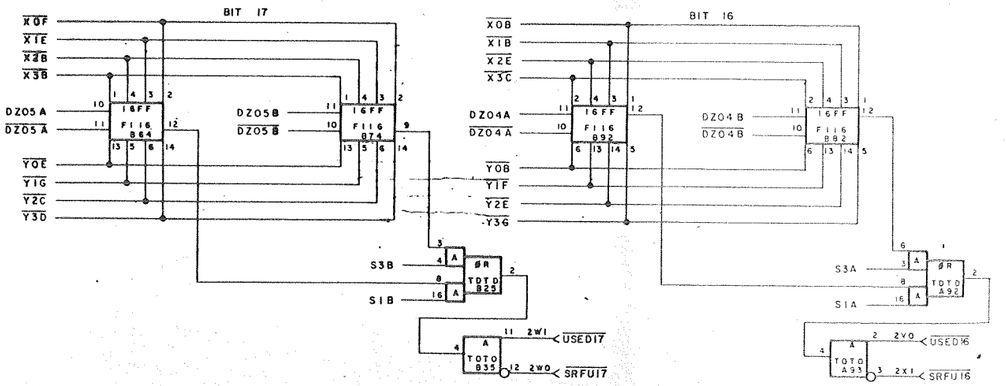


CONTROL DATA	TITLE: REGISTER FILE LOCATIONS 40-77 UPPER 12 2A1A0 LOC:2A1B0	SIZE C	DRAWING NO 60289500 REV W
DEVELOPMENT DIVISION	PART NO. SER.003	SHEET	PAGE 5-81









CONTROL DATA
DEVELOPMENT DIVISION

TITLE
REGISTER FILE
LOCATIONS 40-77
UPPER 12
2A1A0
LOC: 2A1B0 PART NO. SER003

PRODUCT
SIZE C | DRAWING NO 60289500 | SURV N
SHEET | PAGE 5-83

(upper address = "1") (lower address = "0")

SELECT 1 OF 4 GROUPS IN A QUAD

BIT USED

SECT. 0 | SECT. 1 | SECT. 0 | BIT 12 | SECT. 1

GROUP 0 | GROUP 1 | GROUP 2 | GROUP 3

2Y00X0 (00XXXXX) 1B1
2Y10X1 (01XXXXX) 1C1
2Y20X2 (10XXXXX) 1K0
2Y30X3) (11XXXXX) 1K1

ADDR BITS 5 & 6 DECODED

SELECT 1 OF 4 WORDS IN A SECT.

ADDR BITS 3 & 4 DECODED

USEDW 2X00Y0 (XX00XXX)
USEDX 2X10Y1 (XX01XXX)
USEDY 2X20Y2 (XX10XXX)
USEDZ 2X30Y3 (XX11XXX)

SECT. 0 2-BIT WR LWR — OD30D0
SECT. 1 2-BIT WR UP. — ID1OD2
SECT. 0 2-BIT RD LWR — OS00S1
SECT. 1 2-BIT RD UP. — OS20S3 — OD30D0

DATA PFZ012 — USEDV — USEDA — USEDB — USEDP — PF012

TO NEXT PAGE

NOTES:
1. TO INTERNAL TERMINATING RESISTOR.
2. ADDR BITS 0-2 DECODED.
3. ON EARLY UNITS CIRCUIT TYPE LDR WAS USED INSTEAD OF T612.

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1B1	2A2A1-F1	5- 43	QUADRANT 2 Y=0, QUADRANT 0 X=0
	2A2A4-F0	5- 7	
1C1	2A2A1-E1	5- 43	QUADRANT 2 Y=1, QUADRANT 0 X=1
	2A2A4-D0	5- 7	
1D1	2A2A4-F3	5- 7	QUADRANT 2 X=1, QUADRANT 0 Y=1
1E1	2A2A1-C1	5- 43	QUADRANT 2 X=1, QUADRANT 0 Y=1
1F1	2A2A4-C3	5- 7	QUADRANT 2 X=0, QUADRANT 0 Y=0
1G0	2A2A4-H3	5- 7	QUADRANT 2 X=3, QUADRANT 0 Y=3
1G1	2A2A1-H1	5- 43	QUADRANT 2 X=0, QUADRANT 0 Y=0
1H0	2A2A1-K1	5- 43	QUADRANT 2 X=3, QUADRANT 0 Y=3
1J1	2A2A4-J3	5- 7	QUADRANT 2 X=2, QUADRANT 0 Y=2
1J0	2A2A1-J1	5- 43	QUADRANT 2 Y=2, QUADRANT 0 X=2
1K0	2A2A4-H0	5- 7	
1K1	2A2A1-H0	5- 43	QUADRANT 2 Y=3, QUADRANT 0 X=3
	2A2A4-I0	5- 7	
1M0	2B2B9-02	5- 75	
1M1	2B2B9-03	5- 75	DATA TO PF QUADRANT 0, BIT 12
2C1	2A2A4-N0	5- 7	QUADRANT 0 DIGIT GATE 3
			QUADRANT 0 DIGIT GATE 0
2F0	2A2H3-C0	5- 33	QUADRANT 0 DIGIT GATE 3
			QUADRANT 0 DIGIT GATE 0
2F1	2A2B2-D1	5- 39	QUADRANT 1 DIGIT GATE 1
	2A2A4-P0	5- 7	QUADRANT 0 DIGIT GATE 2
2J0	2A2H3-I0	5- 33	QUADRANT 0 SENSE GATE 0
	2A2A4-W0	5- 7	QUADRANT 0 SENSE GATE 1
2J1	2A2H3-G0	5- 33	QUADRANT 0 SENSE GATE 2
	2A2A4-U0	5- 7	QUADRANT 0 SENSE GATE 3
2K0	2A2H4-C2	5- 21	NOT BIT 12 FROM PF QUADRANT 0

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE: PAGE FILE QUAD. 0 ADDRESSES XX0, XX1
2A2A3
LOC: 2A2B3 PART NO. 185301 SER 004

PRODUCT

SIZE	DRAWING NO.	REV.
C	60181000	G

SHEET | PAGE 5-31

001

111

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1N0	2B2A6-M1	5- 63	
1N1	2B2A6-M0	5- 63	DATA TO PF QUADRANT 0, BIT 10
1O0	2B2A6-T0	5- 63	
1O1	2B2A6-T1	5- 63	DATA TO PF QUADRANT 0, BIT 11
1P0	2B2A6-G1	5- 63	
1P1	2B2A6-G0	5- 63	DATA TO PF QUADRANT 0, BIT 09
1Q0	2B2A7-T0	5- 61	
1Q1	2B2A7-T1	5- 61	DATA TO PF QUADRANT 0, BIT 08
1R0	2B2A7-M1	5- 61	
1R1	2B2A7-M0	5- 61	DATA TO PF QUADRANT 0, BIT 07
1S0	2B2A7-G1	5- 61	
1S1	2B2A7-G0	5- 61	DATA TO PF QUADRANT 0, BIT 06
2C0	2A2B3-F0	5- 31	QUADRANT 0 DIGIT GATE 3 ℄
	2A2A4-N0	5- 7	QUADRANT 0 DIGIT GATE 0
2D0	2A2B0-F1	5- 49	QUADRANT 0 DIGIT GATE 1 ℄
			QUADRANT 3 DIGIT GATE 2
2D1	2A2A4-M1	5- 7	QUADRANT 0 DIGIT GATE 1 ℄
			QUADRANT 3 DIGIT GATE 2
2G0	2A2B3-J1	5- 31	QUADRANT 0 SENSE GATE 2 ℄
			QUADRANT 0 SENSE GATE 3
2G1	2A2A4-U0	5- 7	QUADRANT 0 SENSE GATE 2 ℄
			QUADRANT 0 SENSE GATE 3
2I0	2A2B3-J0	5- 31	QUADRANT 0 SENSE GATE 0 ℄
			QUADRANT 0 SENSE GATE 1
2I1	2A2A4-V0	5- 7	QUADRANT 0 SENSE GATE 0 ℄
			QUADRANT 0 SENSE GATE 1
2M0	2A2B5-W2	5- 19	NOT BIT 07 FROM PF QUADRANT 0
2M1	2A2B4-B2	5- 21	NOT BIT 08 FROM PF QUADRANT 0
2N1	2A2B5-A3	5- 19	NOT BIT 06 FROM PF QUADRANT 0
2Q0	2A2B4-E2	5- 21	NOT BIT 11 FROM PF QUADRANT 0
2R0	2A2B4-R1	5- 21	NOT BIT 09 FROM PF QUADRANT 0
2R1	2A2B4-K0	5- 21	NOT BIT 10 FROM PF QUADRANT 0

BIT 11 BIT 10 BIT 09 BIT 08 BIT 07 BIT 06

FROM PREVIOUS PAGE

TO NEXT PAGE

001 000 011 010 021 020 031 030 041 040 051 050 061 060 071 070 101 100 111 110 121 120 131 130 141 140 151 150 161 160 171 170

4FF FF4 A14 · 4FF FF4 A15 · 4FF FF4 A16 · 4FF FF4 A17 · 4FF FF4 A18 · 4FF FF4 A19 · 4FF FF4 A20 · 4FF FF4 A21 · 4FF FF4 A22 · 4FF FF4 A23 · 4FF FF4 A24 · 4FF FF4 A25

4FF FF4 B14 · 4FF FF4 B15 · 4FF FF4 B16 · 4FF FF4 B17 · 4FF FF4 B18 · 4FF FF4 B19 · 4FF FF4 B20 · 4FF FF4 B21 · 4FF FF4 B22 · 4FF FF4 B23 · 4FF FF4 B24 · 4FF FF4 B25

4FF FF4 D14 · 4FF FF4 D15 · 4FF FF4 D16 · 4FF FF4 D17 · 4FF FF4 D18 · 4FF FF4 D19 · 4FF FF4 D20 · 4FF FF4 D21 · 4FF FF4 D22 · 4FF FF4 D23 · 4FF FF4 D24 · 4FF FF4 D25

4FF FF4 C14 · 4FF FF4 C15 · 4FF FF4 C16 · 4FF FF4 C17 · 4FF FF4 C18 · 4FF FF4 C19 · 4FF FF4 C20 · 4FF FF4 C21 · 4FF FF4 C22 · 4FF FF4 C23 · 4FF FF4 C24 · 4FF FF4 C25

1ST

PFZ010 1N1 1N0 — DR TR33 6 — E3A, E11A — DGI E10, E9, E8, F9, F8, E7, F7

USEDU 2E0 — TERM TE2 18

USEDT 2E1

PFZ011 1P1 1P0 — DR TR33 6 — E2A, E10A — DGI E10, E9, E8, F9, F8, E7, F7

PFZ008 — E4B, E12B — DGI E14, F14, E13, F13, E12, F12, E11, F11

PFZ009 1P1 1P0 — DR TR33 7 — E4A, E12A — DGI E14, F14, E13, F13, E12, F12, E11, F11

PFZ006 1S1 1S0 — DR TR33 6 — E2B, E10B — DGI E18, F18, E17, F17, E16, F16, E15, F15

PFZ007 1R1 1R0 — DR TR33 6 — E3B, E11B — DGI E18, F18, E17, F17, E16, F16, E15, F15

SAI G7 · SAI G8 · SAI G5 · SAI G6 · SAI G11 · SAI G12 · SAI G9 · SAI G10 · SAI G15 · SAI G16 · SAI G13 · SAI G14

ØR

CONV SA2 14 — E26A 2 2PO — USEDD

CONV SA2 14 — E23A 7 2RI — PF010

CONV SA2 13 — E25A 2 2QI — USEDC

CONV SA2 13 — E24A 7 2QO — PF011

CONV SA2 16 — E27B 2 2BO — USEDF

CONV SA2 16 — E22B 7 2MI — PF008

CONV SA2 15 — E27A 2 2PI — USEDE

CONV SA2 15 — E22A 7 2RO — PF009

CONV SA2 18 — E25B 2 2NO — USEDH

CONV SA2 18 — E24B 7 2NI — PF006

CONV SA2 17 — E26B 2 2DI — USEDG

CONV SA2 17 — E23B 7 2MO — PF007

2DI OD13D2

OD13D2 2DO — PD T422 19 — E5A, E13A, E5B, E13B

OD30D0 2CO — PD T422 19 — E6A, E14A, E6B, E14B — PD T104 11

PD T104 15

USEDR 2HI 2IO — PD T612 20 — E18B — SE STI H4

OS00S1 2I1 OS00S1

USEDS 2HO 2GO — PD T612 20 — E18A — SE STI H3

SE STI H6 · SE STI H5 · SE STI H8 · SE STI H7

OD13D2 TO T104

OD30D0 TO T104

TO NEXT PAGE

OS00S1 TO F18B

OS20S3 TO F18A

NOTE

(1) TO INTERNAL TERMINATING RESISTOR

(2) ON EARLY UNITS CIRCUIT TYPE LDR WAS USED INSTEAD OF T612.

CONTROL DATA DEVELOPMENT DIVISION

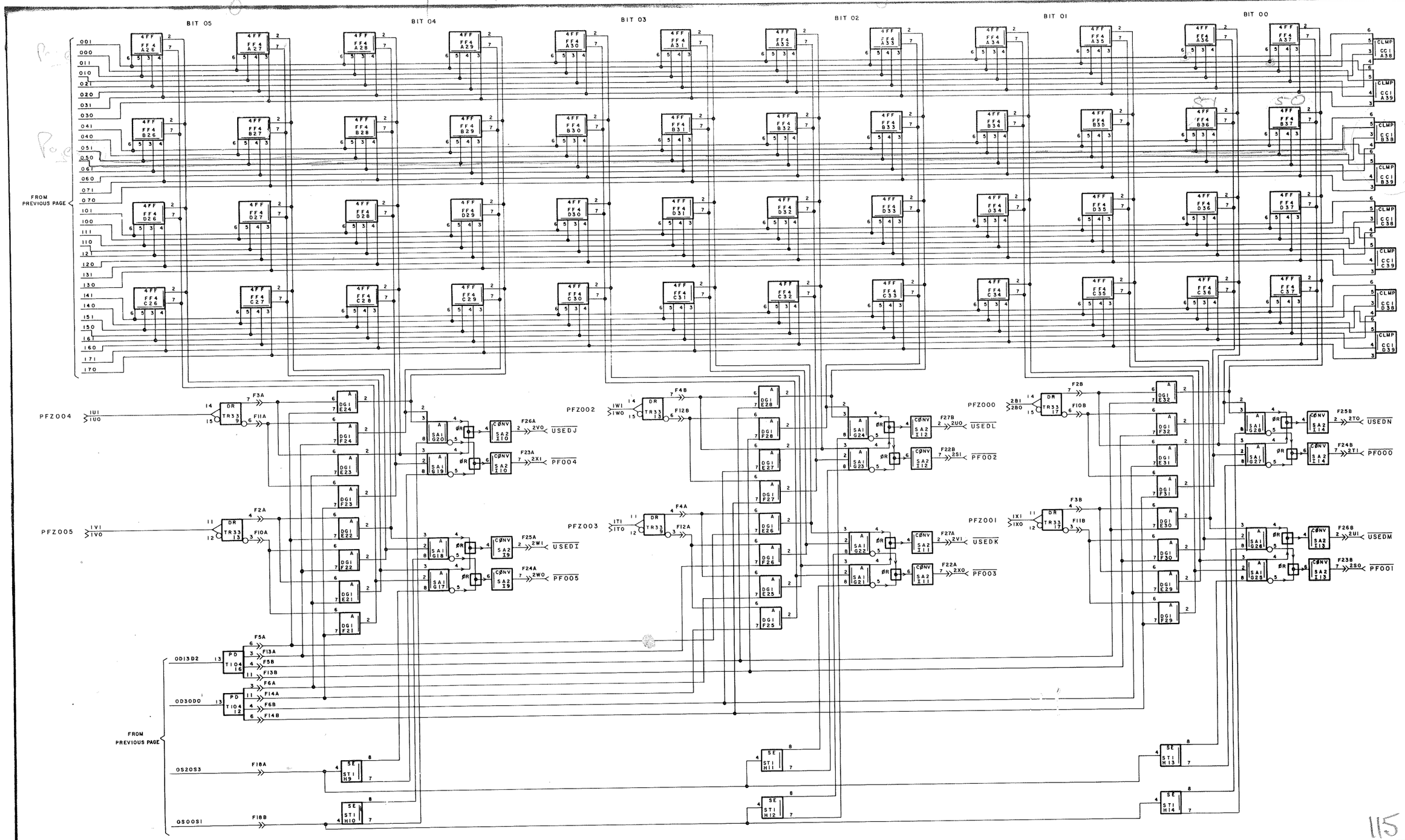
TITLE PAGE FILE QUAD. 0 ADDRESSES XX0, XX1

LOC: 2A2A3 2A2B3 PART NO 185301 SER 004

SIZE C DRAWING NO. 60181000 REV. E

SHEET PAGE 5-33

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1I0	2B2A8-G1	5- 59	
1I1	2B2A8-G0	5- 59	DATA TO PF QUADRANT 0, BIT 03
1U0	2B2A8-M1	5- 59	
1U1	2B2A8-M0	5- 59	DATA TO PF QUADRANT 0, BIT 04
1V0	2B2A8-T0	5- 59	
1V1	2B2A8-T1	5- 59	DATA TO PF QUADRANT 0, BIT 05
1*0	2B2A9-T0	5- 57	
1*1	2B2A9-T1	5- 57	DATA TO PF QUADRANT 0, BIT 02
1A0	2B2A9-M1	5- 57	
1A1	2B2A9-M0	5- 57	DATA TO PF QUADRANT 0, BIT 01
2B0	2B2A9-G1	5- 57	
2B1	2B2A9-G0	5- 57	DATA TO PF QUADRANT 0, BIT 00
2S0	2A2B8-A3	5- 13	NOT BIT 01 FROM PF QUADRANT 0
2S1	2A2B7-A3	5- 15	NOT BIT 02 FROM PF QUADRANT 0
2I1	2A2B8-F2	5- 13	NOT BIT 00 FROM PF QUADRANT 0
2*0	2A2B6-W2	5- 17	NOT BIT 05 FROM PF QUADRANT 0
2A0	2A2B7-W2	5- 15	NOT BIT 03 FROM PF QUADRANT 0
2A1	2A2B6-A3	5- 17	NOT BIT 04 FROM PF QUADRANT 0



115

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE
PAGE FILE QUAD. 0
ADDRESSES XX0, XX1
2A2A3
LOC: 2A2B3 PART NO 185301 SER 004

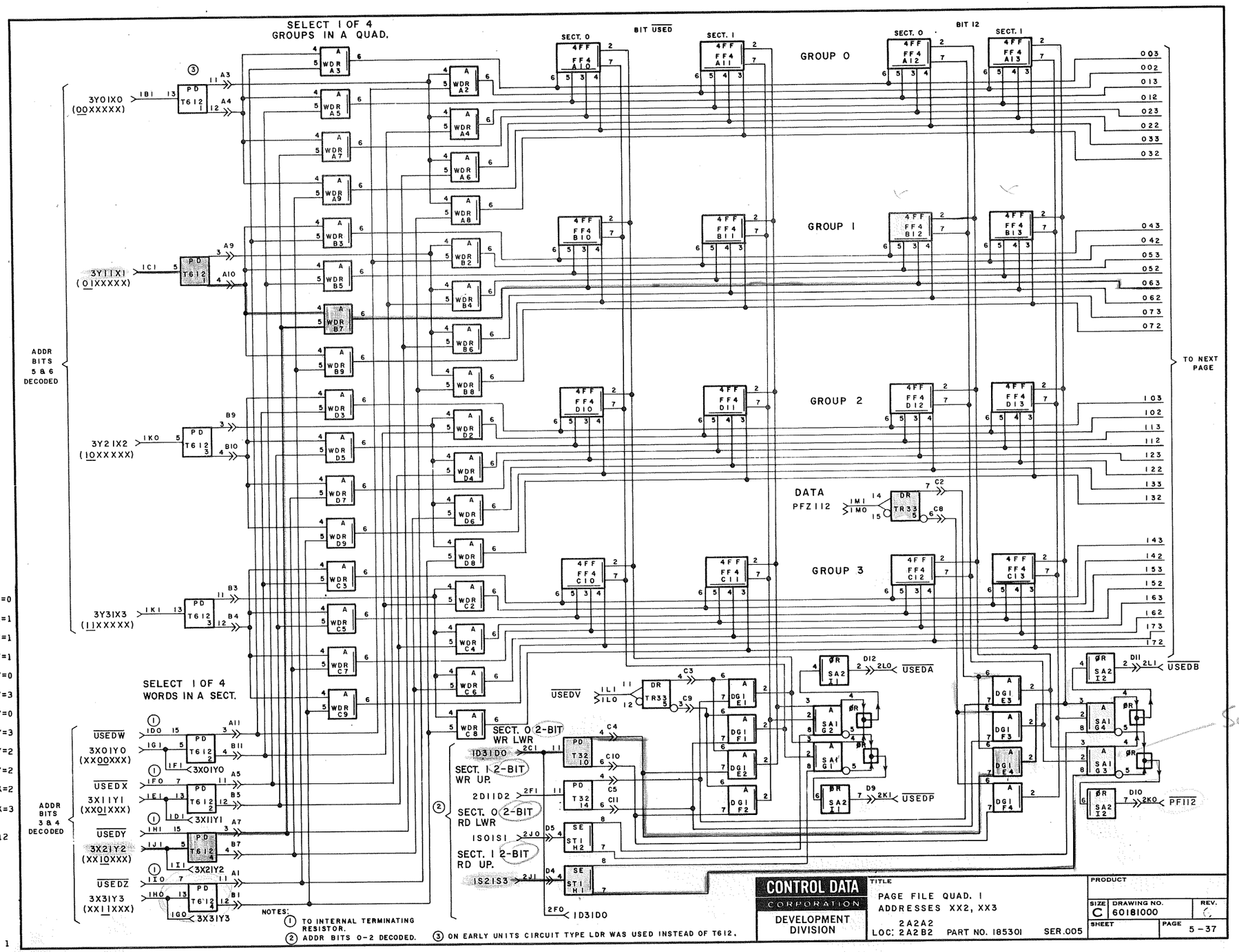
PRODUCT

SIZE	DRAWING NO	REV.
C	60181000	A

SHEET | PAGE 5-35

Read example
Write into Page File #063

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1B1	2A2A0-F1	5- 49	QUADRANT 3 Y=0, QUADRANT 1 X=0
	2A2A4-C0	5- 7	
1C1	2A2A0-E1	5- 49	QUADRANT 3 Y=1, QUADRANT 1 X=1
	2A2A4-A0	5- 7	
1D1	2A2A4-B3	5- 7	QUADRANT 3 X=1, QUADRANT 1 Y=1
1E1	2A2A0-C1	5- 49	QUADRANT 3 X=1, QUADRANT 1 Y=1
1F1	2A2A0-B1	5- 49	QUADRANT 3 X=0, QUADRANT 1 Y=0
1G0	2A2A4-A3	5- 7	QUADRANT 3 X=3, QUADRANT 1 Y=3
1G1	2A2A4-D3	5- 7	QUADRANT 3 X=0, QUADRANT 1 Y=0
1H0	2A2A0-K1	5- 49	QUADRANT 3 X=3, QUADRANT 1 Y=3
1J1	2A2A4-I3	5- 7	QUADRANT 3 X=2, QUADRANT 1 Y=2
1J1	2A2A0-K0	5- 49	QUADRANT 3 X=2, QUADRANT 1 Y=2
1K0	2A2A0-J1	5- 49	QUADRANT 3 Y=2, QUADRANT 1 X=2
	2A2A4-H0	5- 7	
1K1	2A2A0-H0	5- 49	QUADRANT 3 Y=3, QUADRANT 1 X=3
	2A2A4-H1	5- 7	
1M0	2B2B9-P2	5- 75	
1M1	2B2B9-P3	5- 75	DATA TO PF QUADRANT 1, BIT 12
2C1	2A2A4-K1	5- 7	QUADRANT 1 DIGIT GATE 3 ½
			QUADRANT 1 DIGIT GATE 0
2F0	2A2B2-C0	5- 34	QUADRANT 1 DIGIT GATE 3¾
	2A2A4-K1	5- 7	QUADRANT 1 DIGIT GATE 0
2F1	2A2B1-D1	5- 45	QUADRANT 2 DIGIT GATE 1 ½
	2A2A4-G0	5- 7	QUADRANT 1 DIGIT GATE 2
2J0	2A2H2-I0	5- 31	QUADRANT 1 SENSE GATE 0 ½
	2A2A4-I0	5- 7	QUADRANT 1 SENSE GATE 1
2J1	2A2H2-G0	5- 39	QUADRANT 1 SENSE GATE 2 ½
	2A2A4-V1	5- 7	QUADRANT 1 SENSE GATE 3
2K0	2A2B4-K2	5- 21	NOT BIT 12 FROM PF QUADRANT 1



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

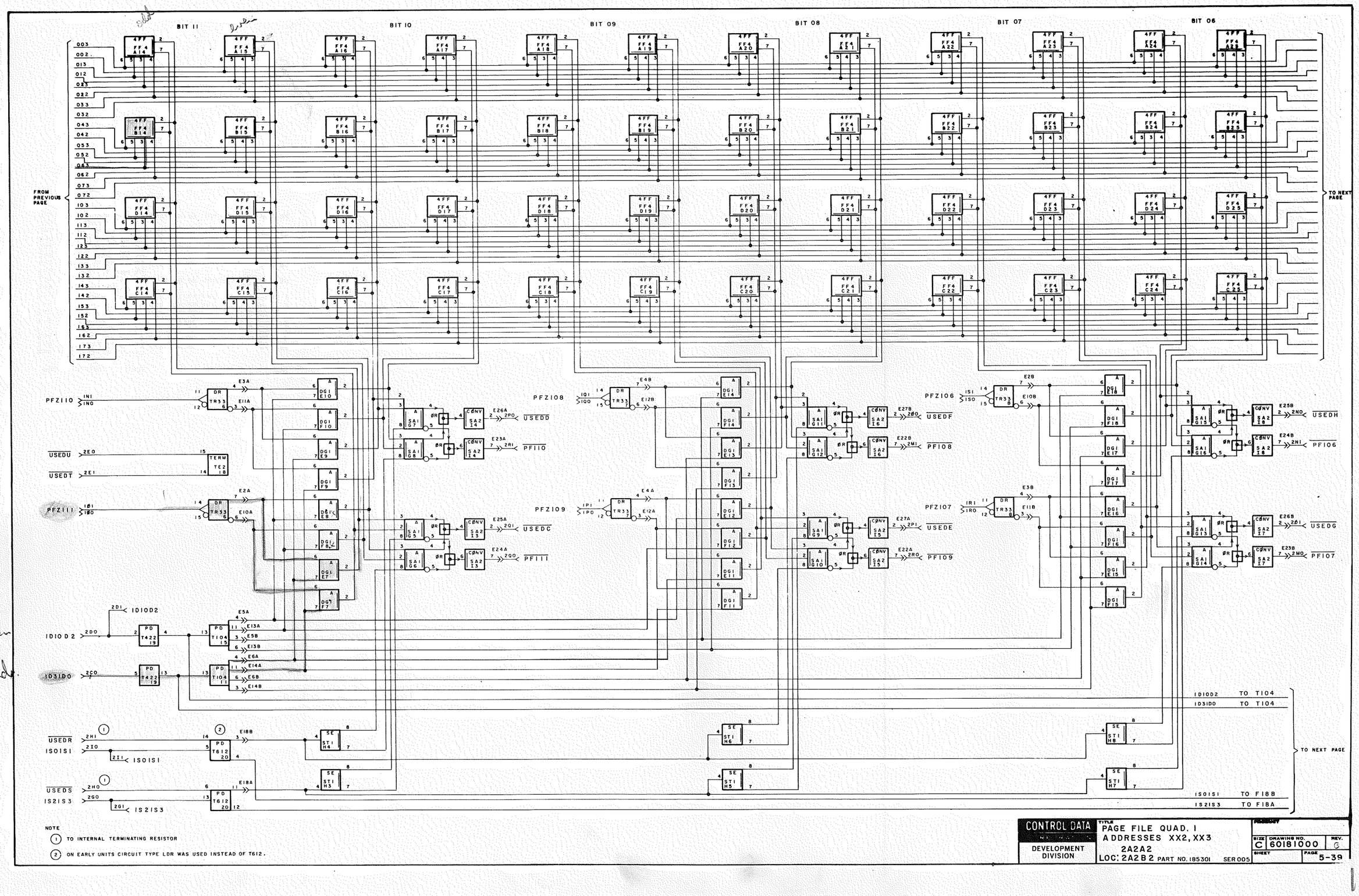
TITLE: PAGE FILE QUAD. 1
ADDRESSES XX2, XX3
2A2A2
LOC: 2A2B2 PART NO. 185301 SER.005

PRODUCT

SIZE	DRAWING NO.	REV.
C	60181000	G

SHEET | PAGE 5-37

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1W0	2B2A6-N0	5- 63	
1N1	2B2A6-N1	5- 63	DATA TO PF QUADRANT 1, BIT 10
1W0	2B2A6-W1	5- 63	
1U1	2B2A6-W0	5- 63	DATA TO PF QUADRANT 1, BIT 11
1P0	2B2A6-I0	5- 63	
1P1	2B2A6-I1	5- 63	DATA TO PF QUADRANT 1, BIT 09
1W0	2B2A7-W1	5- 61	
1W1	2B2A7-W0	5- 61	DATA TO PF QUADRANT 1, BIT 08
1N0	2B2A7-N0	5- 61	
1N1	2B2A7-N1	5- 61	DATA TO PF QUADRANT 1, BIT 07
1S0	2B2A7-I0	5- 61	
1S1	2B2A7-I1	5- 61	DATA TO PF QUADRANT 1, BIT 06
2L0	2A2H2-F0	5- 37	QUADRANT 1 DIGIT GATE 3 ¢
	2A2A4-K1	5- 7	QUADRANT 1 DIGIT GATE 0
2U0	2A2A4-P0	5- 7	QUADRANT 1 DIGIT GATE 1 ¢
			QUADRANT 0 DIGIT GATE 2
2U1	2A2H3-F1	5- 31	QUADRANT 1 DIGIT GATE 1 ¢
			QUADRANT 0 DIGIT GATE 2
2U0	2A2H2-J1	5- 37	QUADRANT 1 SENSE GATE 2 ¢
			QUADRANT 1 SENSE GATE 3
2U1	2A2A4-V1	5- 7	QUADRANT 1 SENSE GATE 2 ¢
			QUADRANT 1 SENSE GATE 3
2L0	2A2H2-J	5- 37	QUADRANT 1 SENSE GATE 0 ¢
			QUADRANT 1 SENSE GATE 1
2L1	2A2A4-T0	5- 7	QUADRANT 1 SENSE GATE 0 ¢
			QUADRANT 1 SENSE GATE 1
2M0	2A2H5-W3	5- 19	NOT BIT 07 FROM PF QUADRANT 1
2M1	2A2H4-L2	5- 21	NOT BIT 08 FROM PF QUADRANT 1
2N1	2A2H5-H2	5- 19	NOT BIT 06 FROM PF QUADRANT 1
2W0	2A2H4-E3	5- 21	NOT BIT 11 FROM PF QUADRANT 1
2K0	2A2H4-H0	5- 21	NOT BIT 09 FROM PF QUADRANT 1
2K1	2A2H4-U1	5- 21	NOT BIT 10 FROM PF QUADRANT 1



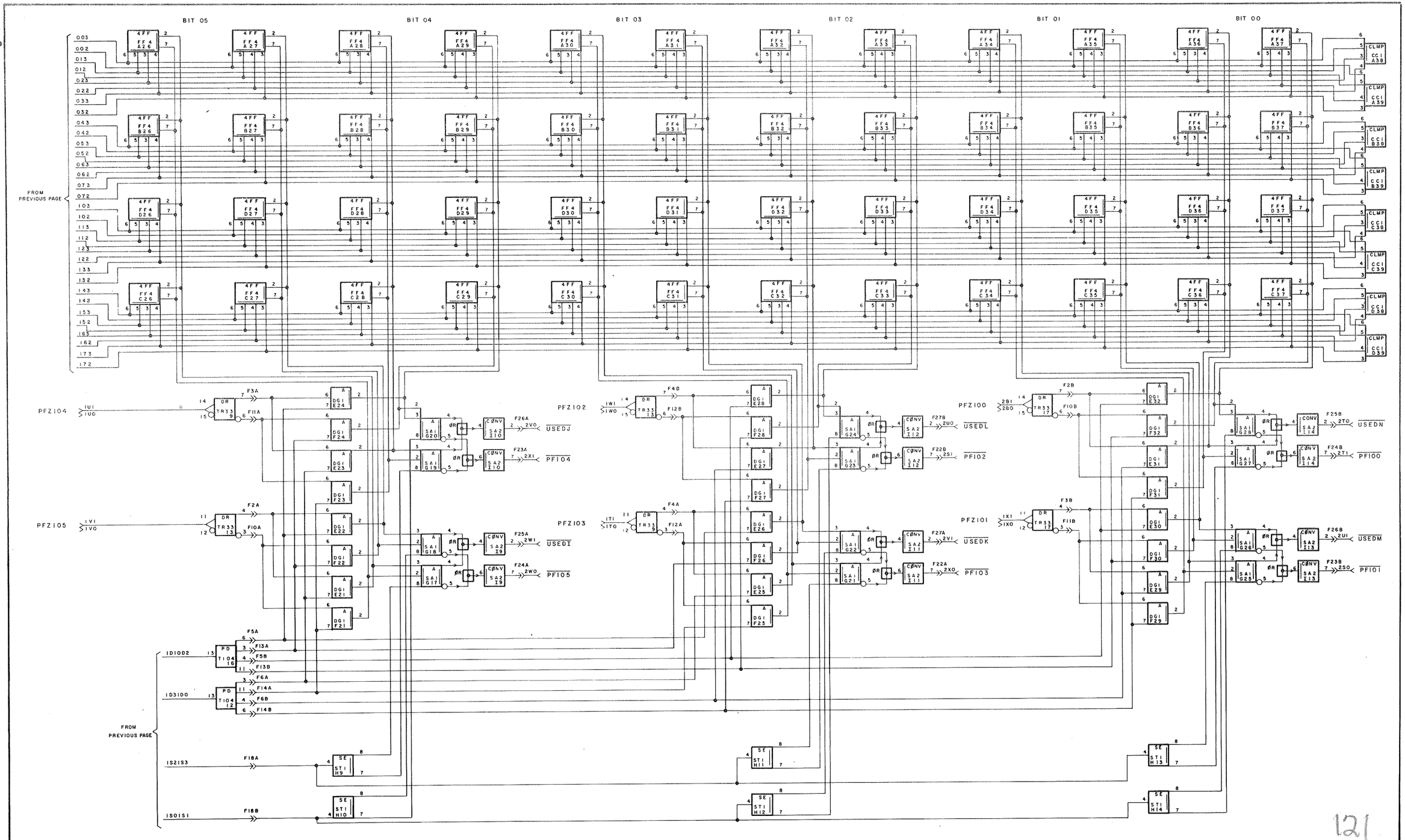
NOTE

(1) TO INTERNAL TERMINATING RESISTOR

(2) ON EARLY UNITS CIRCUIT TYPE LDR WAS USED INSTEAD OF T612.

CONTROL DATA DEVELOPMENT DIVISION	TITLE: PAGE FILE QUAD. I ADDRESSES XX2, XX3 2A2A2 LOC: 2A2B2 PART NO. 185301 SER 005	SIZE C	DRAWING NO. 60181000 REV. G
		SHEET	PAGE 5-39

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
2B0	2B2A9-I0	5- 57	
2B1	2B2A9-I1	5- 57	DATA TO PF QUADRANT 1, BIT 00
2J0	2A2B8-B2	5- 13	NOT BIT 01 FROM PF QUADRANT 1
2J1	2A2B7-B2	5- 15	NOT BIT 02 FROM PF QUADRANT 1
2L1	2A2B8-F3	5- 13	NOT BIT 06 FROM PF QUADRANT 1
2M0	2A2B6-W3	5- 17	NOT BIT 05 FROM PF QUADRANT 1
2N0	2A2B7-W3	5- 15	NOT BIT 03 FROM PF QUADRANT 1
2N1	2A2B6-B2	5- 17	NOT BIT 04 FROM PF QUADRANT 1
1L0	2B2A8-I0	5- 59	
1L1	2B2A8-I1	5- 59	DATA TO PF QUADRANT 1, BIT 03
1V0	2B2A8-N0	5- 59	
1V1	2B2A8-N1	5- 59	DATA TO PF QUADRANT 1, BIT 04
1W0	2B2A8-W1	5- 59	
1W1	2B2A8-W0	5- 59	DATA TO PF QUADRANT 1, BIT 05
1N0	2B2A9-W1	5- 57	
1N1	2B2A9-W0	5- 57	DATA TO PF QUADRANT 1, BIT 02
1K0	2B2A9-N0	5- 57	
1K1	2B2A9-N1	5- 57	DATA TO PF QUADRANT 1, BIT 01


BIT 05
BIT 04
BIT 03
BIT 02
BIT 01
BIT 00
FROM PREVIOUS PAGE
003
002
013
012
023
022
033
032
043
042
053
052
063
062
073
072
103
102
113
112
123
122
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132
143
142
153
152
163
162
173
172
FF4 A26
FF4 A27
FF4 A28
FF4 A29
FF4 A30
FF4 A31
FF4 A32
FF4 A33
FF4 A34
FF4 A35
FF4 A36
FF4 A37
FF4 B26
FF4 B27
FF4 B28
FF4 B29
FF4 B30
FF4 B31
FF4 B32
FF4 B33
FF4 B34
FF4 B35
FF4 B36
FF4 B37
FF4 D26
FF4 D27
FF4 D28
FF4 D29
FF4 D30
FF4 D31
FF4 D32
FF4 D33
FF4 D34
FF4 D35
FF4 D36
FF4 D37
FF4 C26
FF4 C27
FF4 C28
FF4 C29
FF4 C30
FF4 C31
FF4 C32
FF4 C33
FF4 C34
FF4 C35
FF4 C36
FF4 C37
CCI A38
CCI A39
CCI B38
CCI B39
CCI C38
CCI C39
CCI D38
CCI D39
PFZ104
PFZ105
PFZ102
PFZ103
PFZ100
PFZ101
IU1
IU0
IV1
IV0
IW1
IW0
IT1
IT0
2B1
2B0
IX1
IX0
F3A
F11A
F2A
F10A
F4D
F12B
F4A
F12A
F2B
F10B
F3B
F11B
F26A
2V0
USEDJ
F23A
2X1
PFI04
F25A
2W1
USEDI
F24A
2W0
PFI05
F27B
2U0
USEDL
F28
2S1
PFI02
F27A
2V1
USEDK
F22A
2X0
PFI03
F25B
2T0
USEDN
F24B
2T1
PFI00
F26B
2U1
USEDM
F23B
2S0
PFI01
F5A
F13A
F5B
F13B
F6A
F14A
F6B
F14B
ID1OD2
ID3ID0
FROM PREVIOUS PAGE
IS2IS3
IS0IS1
F18A
F18B
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
TITLE
PAGE FILE QUAD. I
ADDRESSES XX2, XX3
2A2A2
LOC: 2A2B2 PART NO 185301 SER 005
PRODUCT
SIZE C
DRAWING NO. 60181000
REV. A
SHEET
PAGE 5-41

121

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1B1	2A2A3-G1	5- 31	QUADRANT 2 X=0, QUADRANT 0 Y=0
	2A2A4-C3	5- 7	
1C1	2A2A3-E1	5- 31	QUADRANT 2 X=1, QUADRANT 0 Y=1
	2A2A4-F3	5- 7	
1D1	2A2A4-D0	5- 7	QUADRANT 2 Y=1, QUADRANT 0 X=1
1E1	2A2A3-C1	5- 31	QUADRANT 2 Y=1, QUADRANT 0 X=1
1F1	2A2A3-B1	5- 31	QUADRANT 2 Y=0, QUADRANT 0 X=0
1G0	2A2A4-I0	5- 7	QUADRANT 2 Y=3, QUADRANT 0 X=3
1G1	2A2A4-F0	5- 7	QUADRANT 2 Y=0, QUADRANT 0 X=0
1H0	2A2A3-K1	5- 31	QUADRANT 2 Y=3, QUADRANT 0 X=3
1J1	2A2A4-H0	5- 7	QUADRANT 2 Y=2, QUADRANT 0 X=2
1J1	2A2A3-K0	5- 31	QUADRANT 2 Y=2, QUADRANT 0 X=2
1K0	2A2A3-J1	5- 31	QUADRANT 2 X=2, QUADRANT 0 Y=2
1K1	2A2A4-J3	5- 7	QUADRANT 2 X=3, QUADRANT 0 Y=3
	2A2A4-H3	5- 7	
1M0	2B2H8-02	5- 77	
1M1	2B2H8-03	5- 77	DATA TO PF QUADRANT 2, BIT 12
2C1	2A2A4-H0	5- 7	QUADRANT 2 DIGIT GATE 3 $\frac{1}{2}$
			QUADRANT 2 DIGIT GATE 0
2F0	2A2H1-C0	5- 45	QUADRANT 2 DIGIT GATE 3 $\frac{1}{2}$
2F1	2A2H0-D1	5- 51	QUADRANT 2 DIGIT GATE 0
	2A2A4-S0	5- 7	QUADRANT 2 DIGIT GATE 2
2J0	2A2H1-I0	5- 45	QUADRANT 2 SENSE GATE 0 $\frac{1}{2}$
	2A2A4-X1	5- 7	QUADRANT 2 SENSE GATE 1
2J1	2A2H1-G0	5- 45	QUADRANT 2 SENSE GATE 2 $\frac{1}{2}$
	2A2A4-W0	5- 7	QUADRANT 2 SENSE GATE 3
2K0	2A2H4-N2	5- 21	NOT BIT 12 FROM PF QUADRANT 2

SELECT 1 OF 4 GROUPS IN A QUAD.

ADDR BITS 5 & 6 DECODED

2X00Y0 (XX00XXX) 1B1

2X10Y1 (XX01XXX) 1C1

2X20Y2 (XX10XXX) 1K0

2X30Y3 (XX11XXX) 1K1

SELECT 1 OF 4 WORDS IN A SECT.

ADDR BITS 3 & 4 DECODED

2Y00X0 (00XXXXX) 1G1

2Y10X1 (01XXXXX) 1E1

2Y20X2 (10XXXXX) 1H1

2Y30X3 (11XXXXX) 1J1

BIT USED

BIT 12

GROUP 0

GROUP 1

GROUP 2

GROUP 3

SECT. 0

SECT. 1

DATA PFZ212

USEDV 1L1

USEDW 1D0

USEDX 1F0

USEDY 1H1

USEDZ 1H0

USEDA 2LO

USEDB 2L1

USEDP 2K1

PF212 2K0

SECT. 0 2-BIT WR LWR 2D32D0

SECT. 1 2-BIT WR UP. 3D12D2

SECT. 0 2-BIT RD LWR 2S02S1

SECT. 1 2-BIT RD UP. 2S22S3

2D32D0

TO NEXT PAGE

NOTES:
1. TO INTERNAL TERMINATING RESISTOR.
2. ADDR BITS 0-2 DECODED.
3. ON EARLY UNITS CIRCUIT TYPE LDR WAS USED INSTEAD OF T612.

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

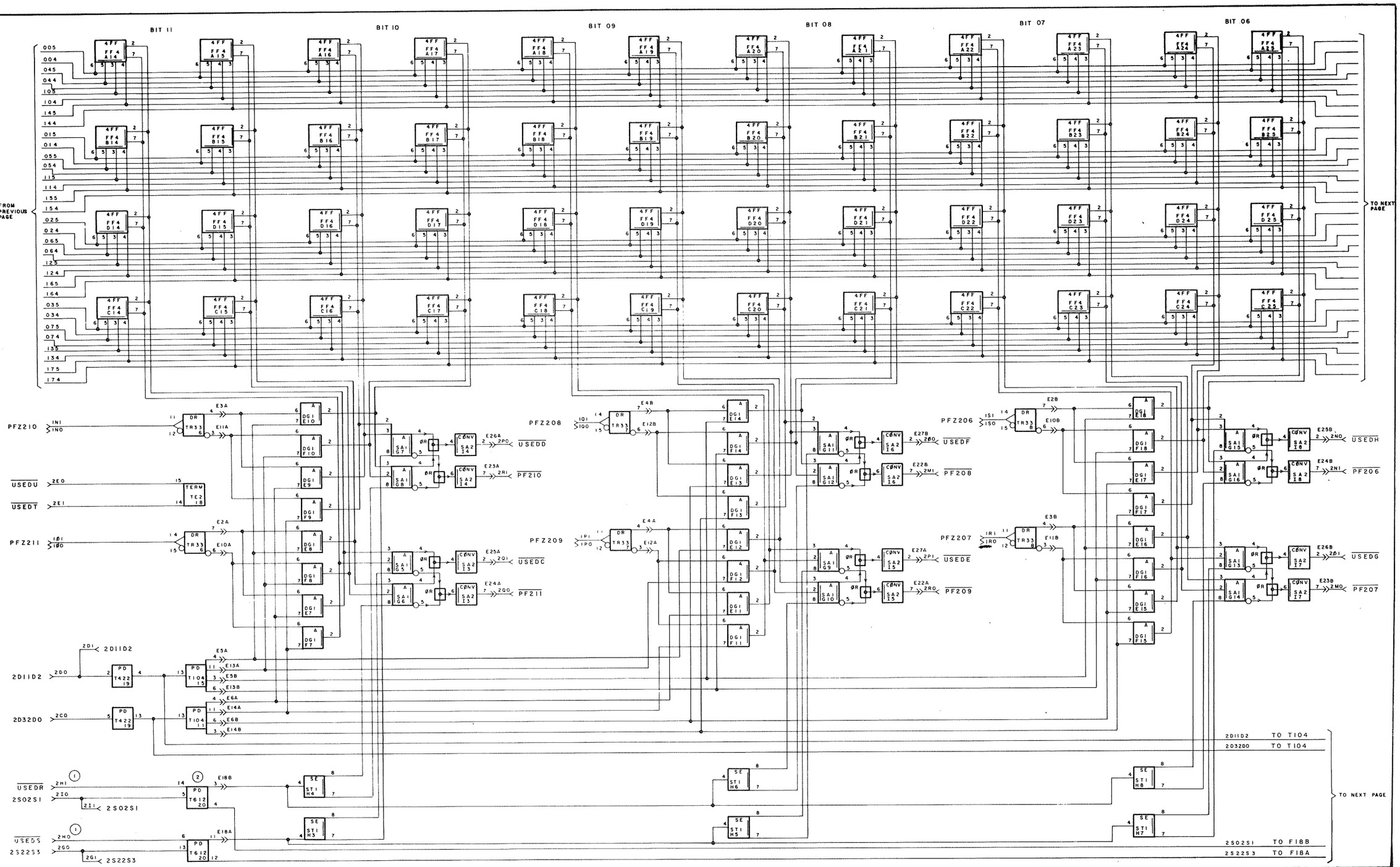
TITLE: PAGE FILE QUAD. 2
ADDRESSES XX4, XX5
2A2A1
LOC: 2A2B1 PART NO. 185301 SER 006

PRODUCT

SIZE C | DRAWING NO. 60181000 | REV. G

SHEET | PAGE 5-43

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1N0	2B2A1-M1	5- 71	
1N1	2B2A1-M0	5- 71	DATA TO PF QUADRANT 2, BIT 10
1U0	2B2A1-T0	5- 71	
1U1	2B2A1-T1	5- 71	DATA TO PF QUADRANT 2, BIT 11
1P0	2B2A1-G1	5- 71	
1P1	2B2A1-G0	5- 71	DATA TO PF QUADRANT 2, BIT 09
1W0	2B2A2-T0	5- 69	
1W1	2B2A2-T1	5- 69	DATA TO PF QUADRANT 2, BIT 08
1K0	2B2A2-M1	5- 69	
1K1	2B2A2-M0	5- 69	DATA TO PF QUADRANT 2, BIT 07
1S0	2B2A2-G1	5- 69	
1S1	2B2A2-G0	5- 69	DATA TO PF QUADRANT 2, BIT 06
2C0	2A2B1-F0	5- 43	QUADRANT 2 DIGIT GATE 3 ¢
	2A2A4-R0	5- 7	QUADRANT 2 DIGIT GATE 0
2U0	2A2A4-Q0	5- 7	QUADRANT 2 DIGIT GATE 1 ¢
			QUADRANT 1 DIGIT GATE 2
2U1	2A2H2-F1	5- 37	QUADRANT 2 DIGIT GATE 1 ¢
			QUADRANT 1 DIGIT GATE 2
2W0	2A2B1-J1	5- 43	QUADRANT 2 SENSE GATE 2 ¢
			QUADRANT 2 SENSE GATE 3
2W1	2A2A4-W0	5- 7	QUADRANT 2 SENSE GATE 2 ¢
			QUADRANT 2 SENSE GATE 3
2L0	2A2B1-J0	5- 43	QUADRANT 2 SENSE GATE 0 ¢
			QUADRANT 2 SENSE GATE 1
2L1	2A2A4-X1	5- 7	QUADRANT 2 SENSE GATE 0 ¢
			QUADRANT 2 SENSE GATE 1
2M0	2A2H5-X2	5- 19	NOT BIT 07 FROM PF QUADRANT 2
2M1	2A2B4-M2	5- 21	NOT BIT 08 FROM PF QUADRANT 2
2N1	2A2B5-N3	5- 19	NOT BIT 06 FROM PF QUADRANT 2
2W0	2A2B4-P2	5- 21	NOT BIT 11 FROM PF QUADRANT 2
2K0	2A2H4-S1	5- 21	NOT BIT 09 FROM PF QUADRANT 2
2K1	2A2H4-V1	5- 21	NOT BIT 10 FROM PF QUADRANT 2



NOTE

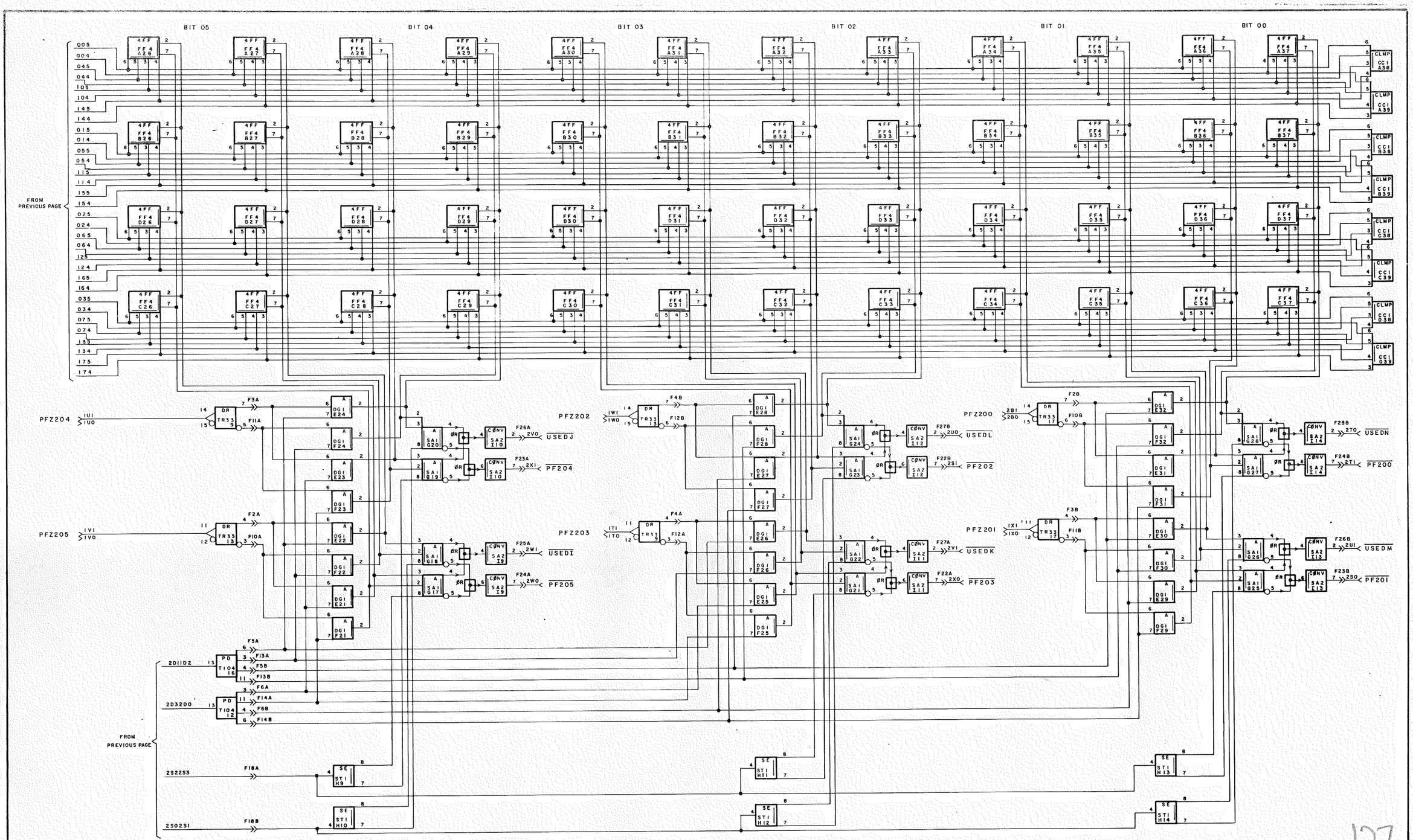
(1) TO INTERNAL TERMINATING RESISTOR

(2) ON EARLY UNITS CIRCUIT TYPE LDR WAS USED INSTEAD OF T612.

CONTROL DATA	TITLE: PAGE FILE QUAD. 2 ADDRESSES XX4, XX5 2A2A1 LOC: 2A2B1 PART NO. 185301 SER 006	SIZE C	DRAWING NO. 60181000 REV. C
DEVELOPMENT DIVISION		SHEET	PAGE 5-45

125

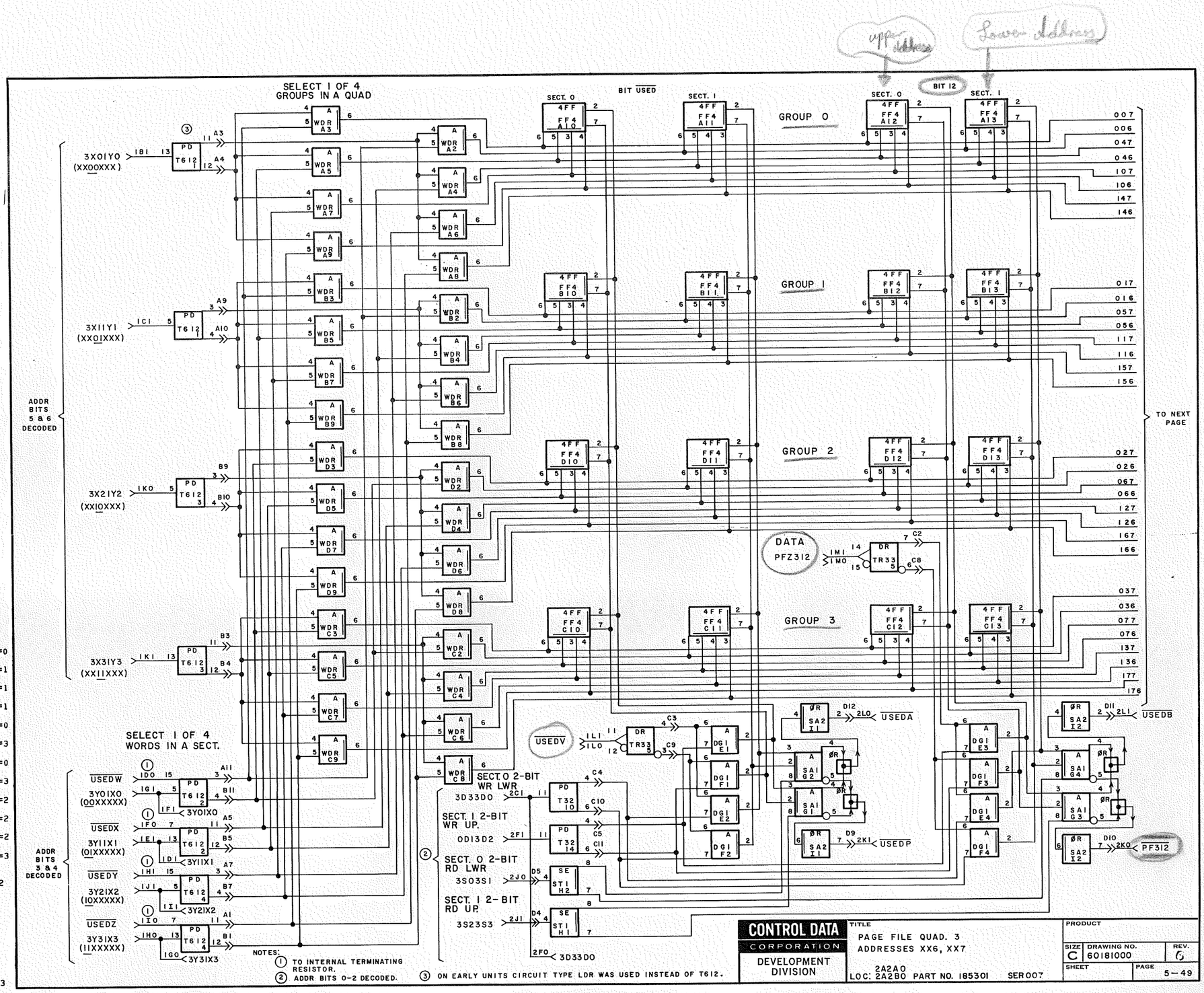
PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1T0	2B2A3-G1	5- 67	
1T1	2B2A3-G0	5- 67	DATA TO PF QUADRANT 2, BIT 03
1U0	2B2A3-M1	5- 67	
1U1	2B2A3-M0	5- 67	DATA TO PF QUADRANT 2, BIT 04
1V0	2B2A3-T0	5- 67	
1V1	2B2A3-T1	5- 67	DATA TO PF QUADRANT 2, BIT 05
1W0	2B2A4-T0	5- 65	
1W1	2B2A4-T1	5- 65	DATA TO PF QUADRANT 2, BIT 02
1X0	2B2A4-M1	5- 65	
1X1	2B2A4-M0	5- 65	DATA TO PF QUADRANT 2, BIT 01
2B0	2B2A4-G1	5- 65	
2B1	2B2A4-G0	5- 65	DATA TO PF QUADRANT 2, BIT 00
2J0	2A2B8-C2	5- 13	NOT BIT 01 FROM PF QUADRANT 2
2J1	2A2B7-H3	5- 15	NOT BIT 02 FROM PF QUADRANT 2
2H1	2A2B8-G2	5- 13	NOT BIT 00 FROM PF QUADRANT 2
2K0	2A2B6-X2	5- 17	NOT BIT 05 FROM PF QUADRANT 2
2X0	2A2B7-X2	5- 15	NOT BIT 03 FROM PF QUADRANT 2
2X1	2A2B6-H3	5- 17	NOT BIT 04 FROM PF QUADRANT 2



127

CONTROL DATA ORION	TITLE: PAGE FILE QUAD. 2 ADDRESSES XX4, XX5 2A2A1 LOC: 2A2B1 PART NO. 85301 SER 006	PRODUCT	
DEVELOPMENT DIVISION		SIZE C	DRAWING NO. 60181000 REV. A
		SHEET	PAGE 5-47

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1B1	2A2A2-F1	5- 37	QUADRANT 3 X=0, QUADRANT 1 Y=0
1C1	2A2A4-D3	5- 7	
1C1	2A2A2-E1	5- 37	QUADRANT 3 X=1, QUADRANT 1 Y=1
1D1	2A2A4-B3	5- 7	
1D1	2A2A4-A0	5- 7	QUADRANT 3 Y=1, QUADRANT 1 X=1
1E1	2A2A2-C1	5- 37	QUADRANT 3 Y=1, QUADRANT 1 X=1
1F1	2A2A2-B1	5- 37	QUADRANT 3 Y=0, QUADRANT 1 X=0
1G0	2A2A4-H1	5- 7	QUADRANT 3 Y=3, QUADRANT 1 X=3
1G1	2A2A4-C0	5- 7	QUADRANT 3 Y=0, QUADRANT 1 X=0
1H0	2A2A2-K1	5- 37	QUADRANT 3 Y=3, QUADRANT 1 X=3
1J1	2A2A4-H0	5- 7	QUADRANT 3 Y=2, QUADRANT 1 X=2
1J1	2A2A2-K0	5- 37	QUADRANT 3 Y=2, QUADRANT 1 X=2
1K0	2A2A2-J1	5- 37	QUADRANT 3 X=2, QUADRANT 1 Y=2
1K1	2A2A4-J3	5- 7	
1K1	2A2A2-H0	5- 37	QUADRANT 3 X=3, QUADRANT 1 Y=3
1M0	2A2A4-A3	5- 7	
1M1	2B2B8-P2	5- 77	
2C1	2B2B8-P3	5- 77	DATA TO PF QUADRANT 3, BIT 12
2C1	2A2A4-N1	5- 7	QUADRANT 3 DIGIT GATE 3
			QUADRANT 3 DIGIT GATE 0
2F0	2A2H0-C0	5- 57	QUADRANT 3 DIGIT GATE 3
			QUADRANT 3 DIGIT GATE 0
2F1	2A2B3-D0	5- 33	QUADRANT 3 DIGIT GATE 1
	2A2A4-M1	5- 7	QUADRANT 3 DIGIT GATE 2
2J0	2A2H0-J0	5- 57	QUADRANT 3 SENSE GATE 0
	2A2A4-W1	5- 7	QUADRANT 3 SENSE GATE 1
2J1	2A2H0-G0	5- 57	QUADRANT 3 SENSE GATE 2
	2A2A4-X0	5- 7	QUADRANT 3 SENSE GATE 3
2K0	2A2H4-N3	5- 21	NOT BIT 12 FROM PF QUADRANT 3



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE
PAGE FILE QUAD. 3
ADDRESSES XX6, XX7
2A2A0
LOC: 2A2B0 PART NO. 185301 SER007

PRODUCT
SIZE C | DRAWING NO. 60181000 | REV. G
SHEET | PAGE 5-49

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1N0	2B2A1-N0	5- 71	
1N1	2B2A1-N1	5- 71	DATA TO PF QUADRANT 3, BIT 10
1U0	2B2A1-W1	5- 71	
1U1	2B2A1-W0	5- 71	DATA TO PF QUADRANT 3, BIT 11
1P0	2B2A1-I0	5- 71	
1P1	2B2A1-I1	5- 71	DATA TO PF QUADRANT 3, BIT 09
1W0	2B2A2-W1	5- 69	
1W1	2B2A2-W0	5- 69	DATA TO PF QUADRANT 3, BIT 08
1K0	2B2A2-N0	5- 69	
1K1	2B2A2-N1	5- 69	DATA TO PF QUADRANT 3, BIT 07
1J0	2B2A2-I0	5- 69	
1J1	2B2A2-I1	5- 69	DATA TO PF QUADRANT 3, BIT 06
2C0	2A2B0-F0	5- 49	QUADRANT 3 DIGIT GATE 3
	2A2A4-N1	5- 7	QUADRANT 3 DIGIT GATE 0
2U0	2A2A4-S0	5- 7	QUADRANT 3 DIGIT GATE 1 & QUADRANT 2 DIGIT GATE 2
2U1	2A2B1-F1	5- 43	QUADRANT 3 DIGIT GATE 1 & QUADRANT 2 DIGIT GATE 2
2W0	2A2B0-J1	5- 49	QUADRANT 3 SENSE GATE 2 & QUADRANT 3 SENSE GATE 3
2W1	2A2A4-X0	5- 7	QUADRANT 3 SENSE GATE 2 & QUADRANT 3 SENSE GATE 3
2J0	2A2B0-J	5- 49	QUADRANT 3 SENSE GATE 0 & QUADRANT 3 SENSE GATE 1
2J1	2A2A4-W1	5- 7	QUADRANT 3 SENSE GATE 0 & QUADRANT 3 SENSE GATE 1
2M0	2A2B5-X3	5- 19	NOT BIT 07 FROM PF QUADRANT 3
2M1	2A2B4-M3	5- 21	NOT BIT 08 FROM PF QUADRANT 3
2N1	2A2B5-C2	5- 19	NOT BIT 06 FROM PF QUADRANT 3
2W0	2A2B4-Q3	5- 21	NOT BIT 11 FROM PF QUADRANT 3
2K0	2A2B4-S0	5- 21	NOT BIT 09 FROM PF QUADRANT 3
2K1	2A2B4-V0	5- 21	NOT BIT 10 FROM PF QUADRANT 3

BIT 11 BIT 10 BIT 09 BIT 08 BIT 07 BIT 06

FROM PREVIOUS PAGE

007 006 047 046 107 106 147 146 017 016 057 056 117 116 157 156 027 026 067 066 127 126 167 166 037 036 077 076 137 136 177 176

4FF FF4 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A24 A25
4FF FF4 B14 B15 B16 B17 B10 B19 B20 B21 B22 B23 B24 B25
4FF FF4 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25
4FF FF4 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25

TO NEXT PAGE

PFZ310 INI INO
USEDU 2E0
USEDT 2E1
PFZ311 1D1 1D0
3D12D2 2D0
3D33D0 2C0
USEDR 2HI 2I0
3S03S1 2I1 3S03S1
USEDS 2H0 2G0
3S23S3 2G1 3S23S3

DR TR33 E3A E11A E2A E10A E5A E13A E5B E13B E6A E14A E6B E14B E18B E18A
DGI E10 E9 F9 E8 F8 E7 F7
PD T422 19 T104 15 11 T612 20
SAI G7 G8 G5 G6
ØR
CONV SA2 I4 I3
E26A 2PO USEDD
E23A 2RI PF310
E25A 2QI USEDC
E24A 2QO PF311

PFZ308 PFZ309

1D1 1D0 E4B E12B E4A E12A
DGI E14 F14 E13 F13 E12 F12 E11 F11
SAI G11 G12 G9 G10
CONV SA2 I6 I5
E27B 2BO USEDF
E22B 2MI PF308
E27A 2PI USEDE
E22A 2RO PF309

PFZ306 PFZ307

1S1 1S0 E2B E10B E3B E11B
DGI E18 F18 E17 F17 E16 F16 E15 F15
SAI G15 G16 G13 G14
E25B 2NO USEDH
E24B 2NI PF306
E26B 2QI USEDG
E23B 2MO PF307

3D12D2 TO T104
3D33D0 TO T104
3S03S1 TO F18B
3S23S3 TO F18A

TO NEXT PAGE

NOTE
(1) TO INTERNAL TERMINATING RESISTOR
(2) ON EARLY UNITS CIRCUIT TYPE LDR WAS USED INSTEAD OF T612.

CONTROL DATA
DEVELOPMENT DIVISION

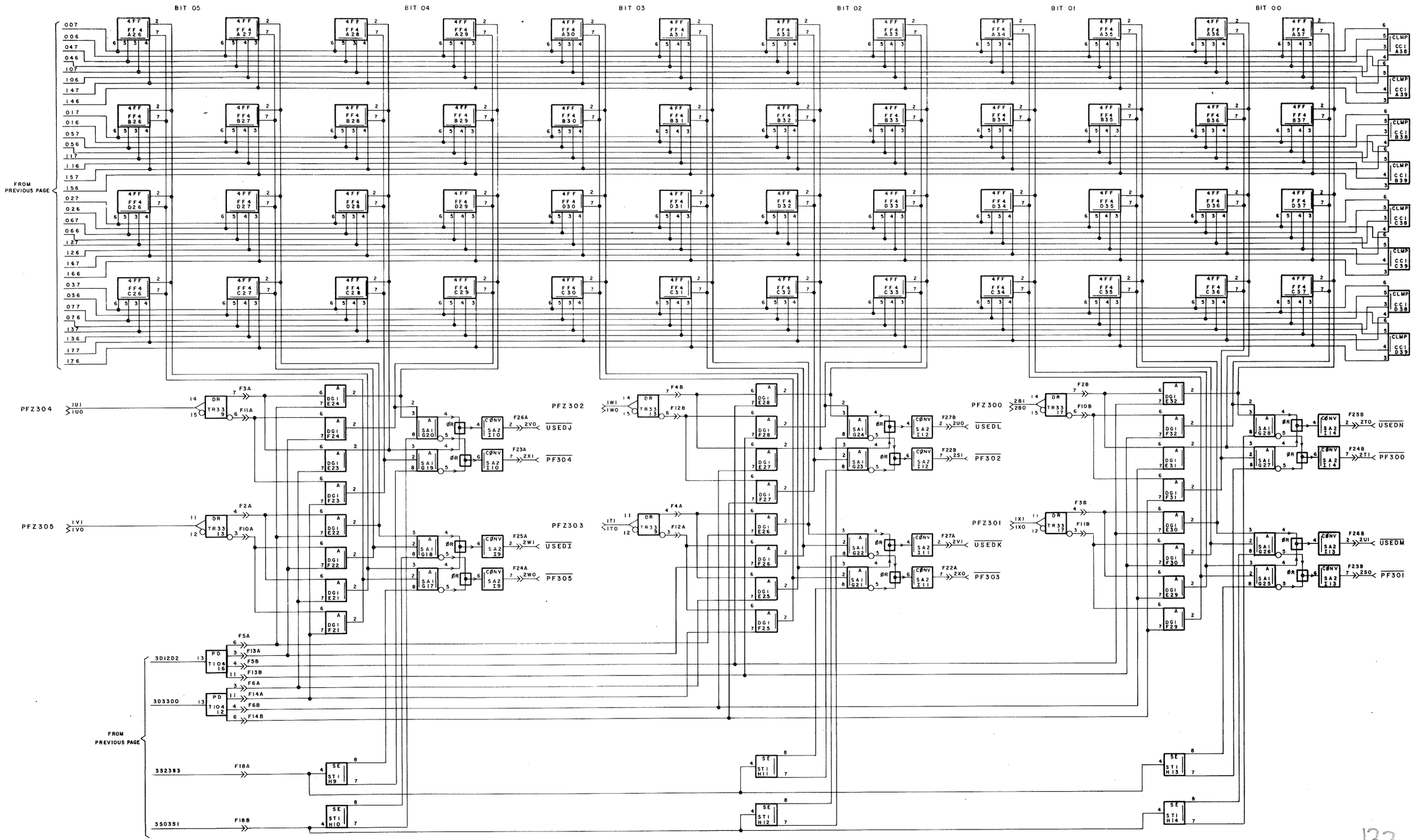
TITLE
PAGE FILE QUAD. 3
ADDRESSES XX6, XX7
2A2A0
LOC: 2A2B0 PART NO. 185301 SER 007

PRELIMINARY

SIZE	DRAWING NO.	REV.
C	60181000	G

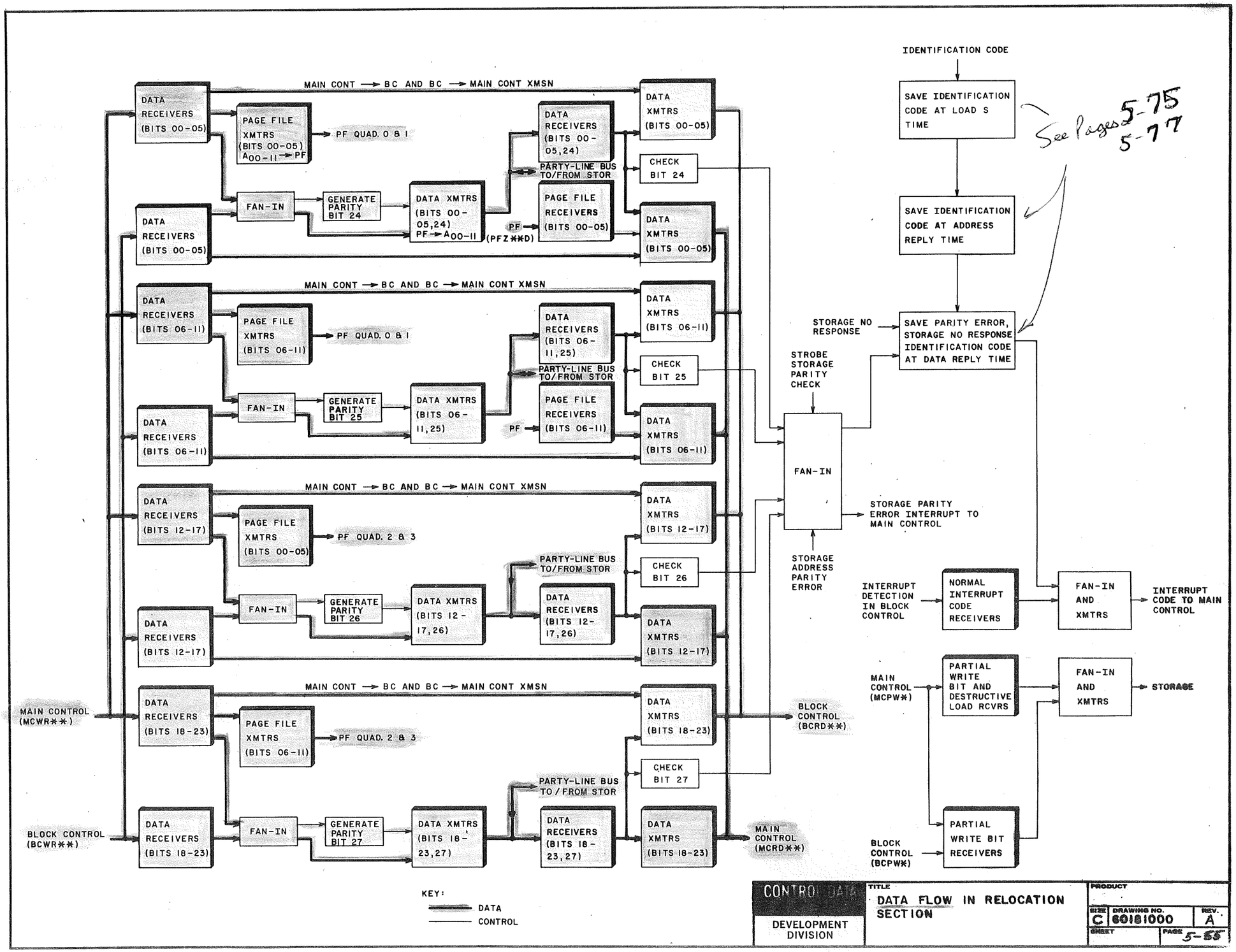
SHEET PAGE 5-51

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1L0	2B2A3-L0	5- 67	
1L1	2B2A3-L1	5- 67	DATA TO PF QUADRANT 3, BIT 03
1U0	2B2A3-N0	5- 67	
1U1	2B2A3-N1	5- 67	DATA TO PF QUADRANT 3, BIT 04
1V0	2B2A3-M1	5- 67	
1V1	2B2A3-M0	5- 67	DATA TO PF QUADRANT 3, BIT 05
1M0	2B2A4-M1	5- 65	
1M1	2B2A4-M0	5- 65	DATA TO PF QUADRANT 3, BIT 02
1N0	2B2A4-N0	5- 65	
1N1	2B2A4-N1	5- 65	DATA TO PF QUADRANT 3, BIT 01
2S0	2B2A4-L0	5- 65	
2S1	2B2A4-L1	5- 65	DATA TO PF QUADRANT 3, BIT 00
2S0	2A2B8-B3	5- 13	NOT BIT 01 FROM PF QUADRANT 3
2S1	2A2B7-C2	5- 15	NOT BIT 02 FROM PF QUADRANT 3
2T1	2A2B8-G3	5- 13	NOT BIT 00 FROM PF QUADRANT 3
2M0	2A2B6-K3	5- 17	NOT BIT 05 FROM PF QUADRANT 3
2N0	2A2B7-K3	5- 15	NOT BIT 03 FROM PF QUADRANT 3
2N1	2A2B6-C2	5- 17	NOT BIT 04 FROM PF QUADRANT 3



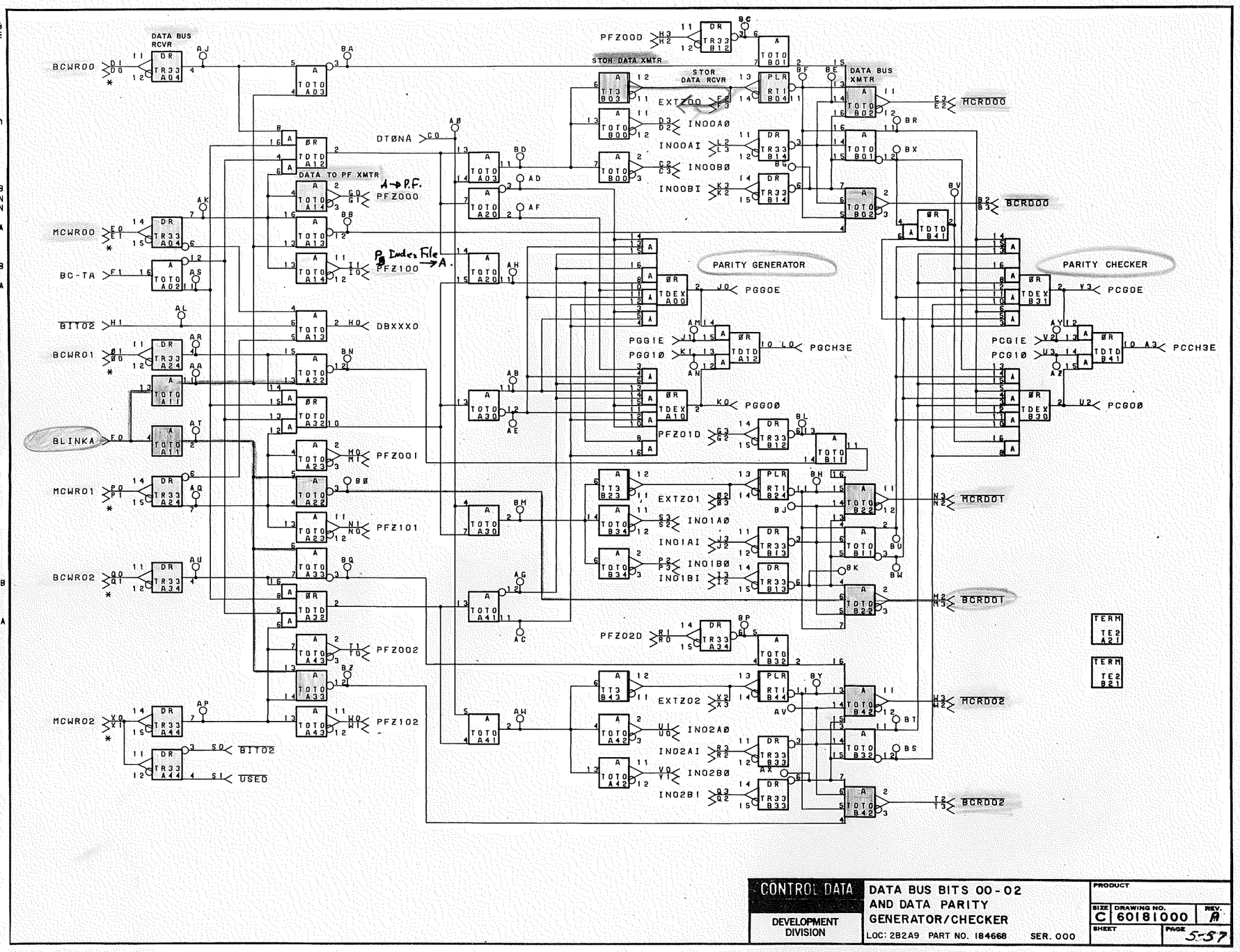
133

CONTROL DATA CORPORATION	TITLE: PAGE FILE QUAD. 3 ADDRESSES XX6, XX7 2A2A0 LOC: 2A2B0 PART NO 185301 SER 007	PRODUCT	
DEVELOPMENT DIVISION		SIZE C	DRAWING NO 60181000 REV. A
		SHEET	PAGE 5-53


MAIN CONT → BC AND BC → MAIN CONT XMSN
DATA RECEIVERS (BITS 00-05)
PAGE FILE XMTRS (BITS 00-05) A00-11 → PF
PF QUAD. 0 & 1
FAN-IN
GENERATE PARITY BIT 24
DATA XMTRS (BITS 00-05,24) PF → A00-11
DATA RECEIVERS (BITS 00-05,24)
PARTY-LINE BUS TO/FROM STOR
PAGE FILE RECEIVERS (BITS 00-05)
PF (PFZ**D)
DATA XMTRS (BITS 00-05)
CHECK BIT 24
DATA RECEIVERS (BITS 00-05)
MAIN CONT → BC AND BC → MAIN CONT XMSN
DATA RECEIVERS (BITS 06-11)
PAGE FILE XMTRS (BITS 06-11)
PF QUAD. 0 & 1
FAN-IN
GENERATE PARITY BIT 25
DATA XMTRS (BITS 06-11,25)
DATA RECEIVERS (BITS 06-11,25)
PARTY-LINE BUS TO/FROM STOR
PAGE FILE RECEIVERS (BITS 06-11)
PF
DATA XMTRS (BITS 06-11)
CHECK BIT 25
DATA RECEIVERS (BITS 06-11)
MAIN CONT → BC AND BC → MAIN CONT XMSN
DATA RECEIVERS (BITS 12-17)
PAGE FILE XMTRS (BITS 00-05)
PF QUAD. 2 & 3
FAN-IN
GENERATE PARITY BIT 26
DATA XMTRS (BITS 12-17,26)
DATA RECEIVERS (BITS 12-17,26)
PARTY-LINE BUS TO/FROM STOR
DATA XMTRS (BITS 12-17)
CHECK BIT 26
DATA RECEIVERS (BITS 12-17)
MAIN CONT → BC AND BC → MAIN CONT XMSN
MAIN CONTROL (MCWR**)
DATA RECEIVERS (BITS 18-23)
PAGE FILE XMTRS (BITS 06-11)
PF QUAD. 2 & 3
FAN-IN
GENERATE PARITY BIT 27
DATA XMTRS (BITS 18-23,27)
DATA RECEIVERS (BITS 18-23,27)
PARTY-LINE BUS TO/FROM STOR
DATA XMTRS (BITS 18-23)
CHECK BIT 27
BLOCK CONTROL (BCWR**)
DATA RECEIVERS (BITS 18-23)
KEY:
DATA
CONTROL
IDENTIFICATION CODE
SAVE IDENTIFICATION CODE AT LOAD S TIME
See Pages 5-75 5-77
SAVE IDENTIFICATION CODE AT ADDRESS REPLY TIME
STORAGE NO RESPONSE
SAVE PARITY ERROR, STORAGE NO RESPONSE IDENTIFICATION CODE AT DATA REPLY TIME
STROBE STORAGE PARITY CHECK
FAN-IN
STORAGE PARITY ERROR INTERRUPT TO MAIN CONTROL
STORAGE ADDRESS PARITY ERROR
INTERRUPT DETECTION IN BLOCK CONTROL
NORMAL INTERRUPT CODE RECEIVERS
FAN-IN AND XMTRS
INTERRUPT CODE TO MAIN CONTROL
MAIN CONTROL (MCPW*)
PARTIAL WRITE BIT AND DESTRUCTIVE LOAD RCVRS
FAN-IN AND XMTRS
STORAGE
BLOCK CONTROL (BCRD**)
MAIN CONTROL (MCRD**)
BLOCK CONTROL (BCPW*)
PARTIAL WRITE BIT RECEIVERS
CONTROL DATA
DEVELOPMENT DIVISION
TITLE
DATA FLOW IN RELOCATION SECTION
PRODUCT
SIZE C
DRAWING NO. 60181000
REV. A
SHEET
PAGE 5-85

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A3	2B2A5-E0	5- 73	2B2A5-AH	PARITY CHECK, CHARACTER 3 EVEN
B2	2B1B4-E0	6- 29		
B3	2B1B4-E1	6- 29		NOT BC READ BIT 00
C0	2B2A5-S8	5- 73	2B2A9-A0	DATA TRANSMITTERS ON
C2	2A1A06J13A-01			BIT 00 TO INTERNAL STORAGE B
C3	2A1A06J13A-02			
D0	2B1B4-E2	6- 29		
D1	2B1B4-E3	6- 29		NOT D4 BIT 00 TO MCS VIA FI
D2	2A1A06J11A-02			
D3	2A1A06J11A-01			BIT 00 TO INTERNAL STORAGE A
E0	2A1A06P01D-01			NOT DO REGISTER BIT 00
	1A4A06J04D-01			
	1A0A8-C1	2- 55		
E1	2A1A06P01D-02			
	1A4A06J04D-02			
	1A0A8-C0	2- 55		
E2	2A1A06P01A-01			NOT MAIN CONTROL READ, BIT 00
	1A4A06J04A-01			
	1A0B8-E1	2- 65		
E3	2A1A06P01A-02			
	1A4A06J04A-02			
	1A0B8-E0	2- 65		

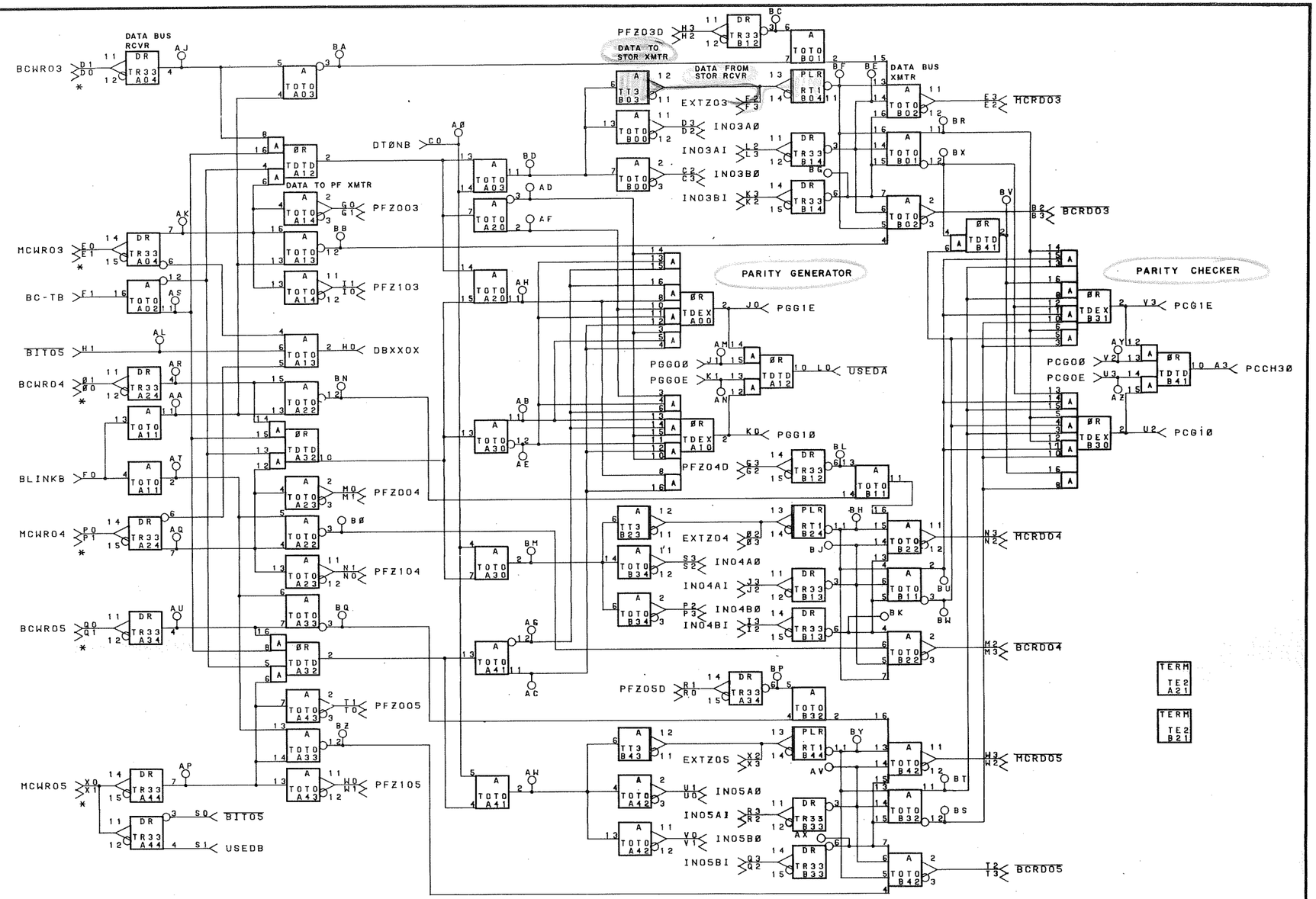
F0	2B2A5-R2	5- 73		LINK MN CONT/BC DB REG THRU DB
F1	2B2A5-P3	5- 73		BLOCK CONTROL DATA XMIT ENABLE
F2	2A1A06J09A-01			BIT 00 TO/FROM EXTERNAL STOR
	2A1A06J10A-01			
F3	2A1A06J09A-02			
	2A1A06J10A-02			
G0	2A2B3-B1	5- 35		DATA TO PF QUADRANT 0, BIT 00
G1	2A2B3-B0	5- 35		
G2	2A2B8-N2	5- 13		
G3	2A2B8-N3	5- 13		BIT 01 OUT OF PF TO DB XMTR
H0	2B2B9-H1	5- 75	2B2B9-RU	MAIN CONTROL DATA BITS 00-02=0
H1	2B2A9-S0	5- 57	2B2A9-AL	NOT MAIN CONTROL DATA BIT 02
H2	2A2B8-M3	5- 13		
H3	2A2B8-M2	5- 13		BIT 00 OUT OF PF TO DB XMTR
I0	2A2B2-B0	5- 41		
I1	2A2B2-B1	5- 41		DATA TO PF QUADRANT 1, BIT 00
I2	2A1A06J14A-04			
I3	2A1A06J14A-03			BIT 01 FROM INTERNAL STORAGE B
J0	2B2A8-K1	5- 59	2B2A8-AN	PARITY GENERATOR, GROUP 0 EVEN
J1	2B2A8-J0	5- 59	2B2A9-AM	PARITY GENERATOR, GROUP 1 EVEN
J2	2A1A06J12A-04			
J3	2A1A06J12A-03			BIT 01 FROM INTERNAL STORAGE A
K0	2B2A8-J1	5- 59	2B2A8-AM	PARITY GENERATOR, GROUP 0 ODD
K1	2B2A8-K0	5- 59	2B2A9-AN	PARITY GENERATOR, GROUP 1 ODD
K2	2A1A06J14A-02			
K3	2A1A06J14A-01			BIT 00 FROM INTERNAL STORAGE B
L0	2B2A5-N0	5- 73	2B2A5-AU	PARITY GEN,, CHARACTER 3 EVEN
L2	2A1A06J12A-01			BIT 00 FROM INTERNAL STORAGE A
L3	2A1A06J12A-02			
M0	2A2A3-X1	5- 35		DATA TO PF QUADRANT 0, BIT 01
M1	2A2A3-X0	5- 35		
M2	2B1B3-E0	6- 31		
M3	2B1B3-E1	6- 31		NOT BC READ BIT 01
N0	2A2A2-X0	5- 41		
N1	2A2A2-X1	5- 41		DATA TO PF QUADRANT 1, BIT 01
N2	2A1A06P01A-03			NOT MAIN CONTROL READ, BIT 01
	1A4A06J04A-03			
	1A0B8-F1	2- 65		
N3	2A1A06P01A-04			
	1A4A06J04A-04			
	1A0B8-F0	2- 65		
O0	2B1B3-E2	6- 31		
O1	2B1B3-E3	6- 31		NOT D4 BIT 01 TO MCS VIA F1
O2	2A1A06J09A-03			BIT 01 TO/FROM EXTERNAL STOR
	2A1A06J10A-03			
O3	2A1A06J09A-04			
	2A1A06J10A-04			
P0	2A1A06P01D-03			NOT D0 REGISTER BIT 01
	1A4A06J04D-03			
	1A0A8-B1	2- 55		
P1	2A1A06P01D-04			
	1A4A06J04D-04			
	1A0A8-B0	2- 55		
P2	2A1A06J13A-03			BIT 01 TO INTERNAL STORAGE B
P3	2A1A06J13A-04			
Q0	2B1B2-E3	6- 33		NOT D4 BIT 02 TO MCS VIA F1
Q1	2B1B2-E2	6- 33		
Q2	2A1A06J14A-06			
Q3	2A1A06J14A-05			BIT 02 FROM INTERNAL STORAGE B
R0	2A2B7-O3	5- 15		BIT 02 OUT OF PF TO DB XMTR
R1	2A2B7-O2	5- 15		
R2	2A1A06J12A-06			
R3	2A1A06J12A-05			BIT 02 FROM INTERNAL STORAGE A
S0	2B2A9-H1	5- 57	2B2A9-AL	NOT MAIN CONTROL DATA BIT 02
S2	2A1A06J11A-04			
S3	2A1A06J11A-03			BIT 01 TO INTERNAL STORAGE A
T0	2A2A3-W0	5- 35		DATA TO PF QUADRANT 0, BIT 02
T1	2A2A3-W1	5- 35		
T2	2B1B2-E0	6- 33		
T3	2B1B2-E1	6- 33		NOT BC READ BIT 02
U0	2A1A06J11A-06			
U1	2A1A06J11A-05			BIT 02 TO INTERNAL STORAGE A
U2	2B2A8-V2	5- 59	2B2A8-AY	PARITY CHECK, GROUP 0 ODD
U3	2B2A8-U2	5- 59	2B2A9-AZ	PARITY CHECK, GROUP 1 ODD
V0	2A1A06J13A-05			BIT 02 TO INTERNAL STORAGE B
V1	2A1A06J13A-06			
V2	2B2A8-V3	5- 59	2B2A9-AY	PARITY CHECK, GROUP 1 EVEN
V3	2B2A8-U3	5- 59	2B2A8-AZ	PARITY CHECK, GROUP 0 EVEN
W0	2A2A2-W1	5- 41		DATA TO PF QUADRANT 1, BIT 02
W1	2A2A2-W0	5- 41		
W2	2A1A06P01A-05			NOT MAIN CONTROL READ, BIT 02
	1A4A06J04A-05			
	1A0B8-W0	2- 65		
W3	2A1A06P01A-06			
	1A4A06J04A-06			
	1A0B8-W1	2- 65		
X0	2A1A06P01D-05			NOT D0 REGISTER BIT 02
	1A4A06J04D-05			
	1A0A8-H1	2- 55		
X1	2A1A06P01D-06			
	1A4A06J04D-06			
	1A0A8-H0	2- 55		
X2	2A1A06J09A-05			BIT 02 TO/FROM EXTERNAL STOR
	2A1A06J10A-05			
X3	2A1A06J09A-06			
	2A1A06J10A-06			



CONTROL DATA	DATA BUS BITS 00-02 AND DATA PARITY GENERATOR/CHECKER	PRODUCT	
DEVELOPMENT DIVISION	LOC: 2B2A9 PART NO. 184668 SER. 000	SIZE C	DRAWING NO. 60181000 REV. A
		SHEET	PAGE 5-57

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A3	2B2A5-E1	5- 73	2B2A5-A0	PARITY CHECK, CHARACTER 3 ODD
B2	2B1A4-E0	6- 35		
B3	2B1A4-E1	6- 35		NOT BC READ BIT 03
C0	2B2A5-C0	5- 73	2B2A8-A0	DATA TRANSMITTERS ON
C2	2A1A06J13A-07			BIT 03 TO INTERNAL STORAGE B
C3	2A1A06J13A-08			
D0	2B1A4-E2	6- 35		
D1	2B1A4-E3	6- 35		NOT D4 BIT 03 TO MCS VIA F1
D2	2A1A06J11A-08			
D3	2A1A06J11A-07			BIT 03 TO INTERNAL STORAGE A
E0	2A1A06P01D-07			NOT DO REGISTER BIT 03
	1A4A06J04D-07			
	1A0A6-C1	2- 57		
E1	2A1A06P01D-08			
	1A4A06J04D-08			
	1A0A6-C0	2- 57		
E2	2A1A06P01A-07			NOT MAIN CONTROL READ, BIT 03
	1A4A06J04A-07			
	1A0B6-E1	2- 67		
E3	2A1A06P01A-08			
	1A4A06J04A-08			

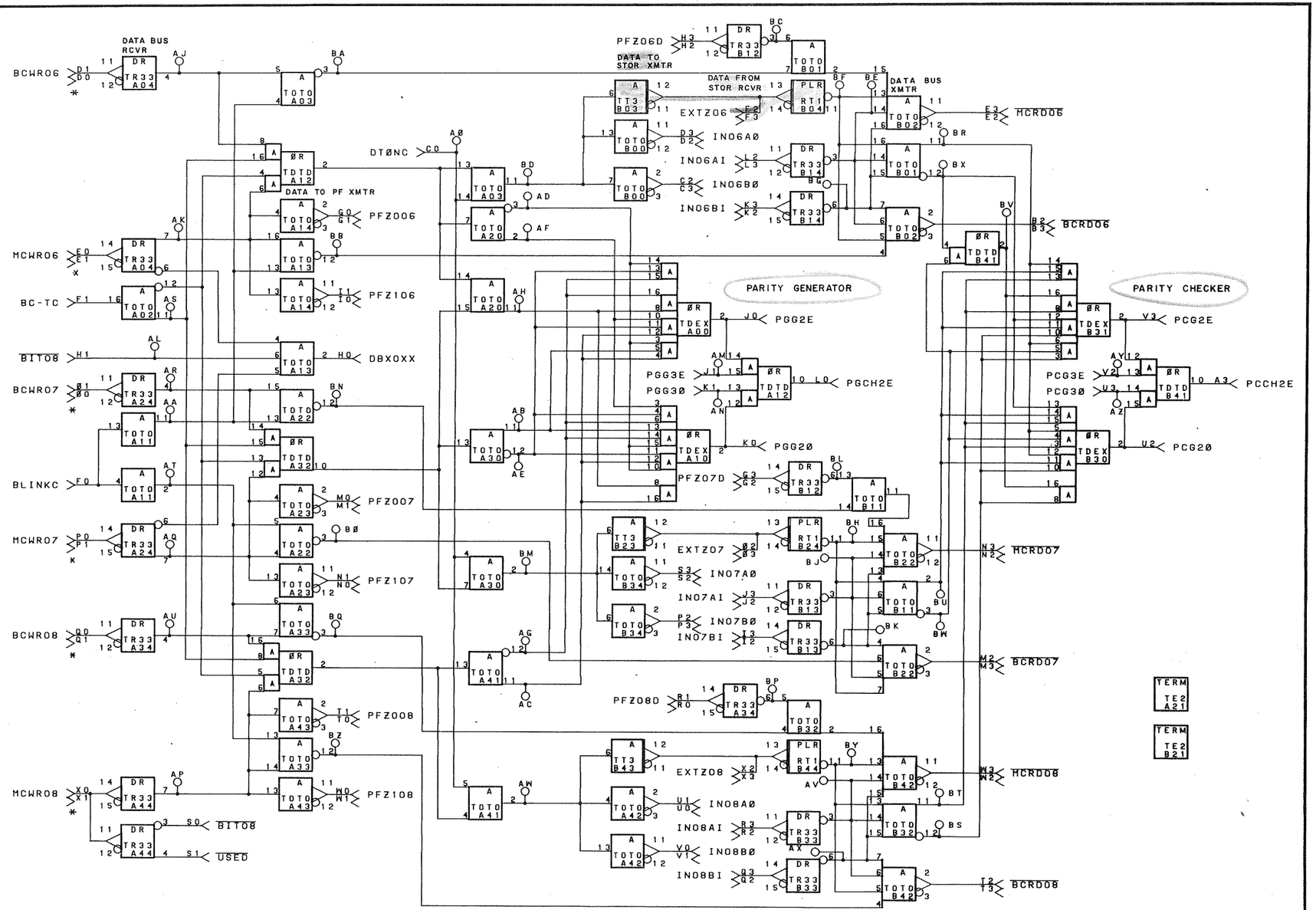
	1A0B6-E0	2- 67			
F0	2B2A5-S3	5- 73			LINK MN CONT/BC DB REG THRU DB
F1	2B2A5-W3	5- 73			BLOCK CONTROL DATA XMIT ENABLE
F2	2A1A06J09A-07				BIT 03 TO/FROM EXTERNAL STOR
	2A1A06J10A-07				
F3	2A1A06J09A-08				
	2A1A06J10A-08				
G0	2A2A3-T1	5- 35			DATA TO PF QUADRANT 0, BIT 03
G1	2A2A3-T0	5- 35			
G2	2A2B6-03	5- 17			
G3	2A2B6-02	5- 17			BIT 04 OUT OF PF TO DB XMTR
H0	2B2B9-K0	5- 75	2B2B9-RS		MAIN CONTROL DATA BITS 03-05=0
H1	2B2A8-S0	5- 59	2B2A8-AL		NOT MAIN CONTROL DATA BIT 05
H2	2A2B7-M3	5- 15			
H3	2A2B7-M2	5- 15			BIT 03 OUT OF PF TO DB XMTR
I0	2A2A2-T0	5- 41			
I1	2A2A2-T1	5- 41			DATA TO PF QUADRANT 1, BIT 03
I2	2A1A06J14A-10				
I3	2A1A06J14A-09				BIT 04 FROM INTERNAL STORAGE B
J0	2B2A9-J1	5- 57	2B2A9-AH		PARITY GENERATOR, GROUP 1 EVEN
J1	2B2A9-K0	5- 57	2B2A8-AM		PARITY GENERATOR, GROUP 0 ODD
J2	2A1A06J12A-10				
J3	2A1A06J12A-09				BIT 04 FROM INTERNAL STORAGE A
K0	2B2A9-K1	5- 57	2B2A9-AN		PARITY GENERATOR, GROUP 1 ODD
K1	2B2A9-J0	5- 57	2B2A8-AN		PARITY GENERATOR, GROUP 0 EVEN
K2	2A1A06J14A-08				
K3	2A1A06J14A-07				BIT 03 FROM INTERNAL STORAGE B
L2	2A1A06J12A-07				BIT 03 FROM INTERNAL STORAGE A
L3	2A1A06J12A-08				
M0	2A2A3-U1	5- 35			DATA TO PF QUADRANT 0, BIT 04
M1	2A2A3-U0	5- 35			
M2	2B1A3-E0	6- 37			
M3	2B1A3-E1	6- 37			NOT BC READ BIT 04
N0	2A2A2-U0	5- 39			
N1	2A2A2-U1	5- 39			DATA TO PF QUADRANT 1, BIT 04
N2	2A1A06P01A-09				NOT MAIN CONTROL READ, BIT 04
	1A4A06J04A-09				
	1A0B6-F1	2- 67			
N3	2A1A06P01A-10				
	1A4A06J04A-10				
	1A0B6-F0	2- 67			
O0	2B1A3-E2	6- 37			
O1	2B1A3-E3	6- 37			NOT D4 BIT 04 TO MCS VIA F1
O2	2A1A06J09A-09				BIT 04 TO/FROM EXTERNAL STOR
	2A1A06J10A-09				
O3	2A1A06J09A-10				
	2A1A06J10A-10				
P0	2A1A06P01D-09				NOT DO REGISTER BIT 04
	1A4A06J04D-09				
	1A0A6-B1	2- 57			
P1	2A1A06P01D-10				
	1A4A06J04D-10				
	1A0A6-B0	2- 57			
P2	2A1A06J13A-09				BIT 04 TO INTERNAL STORAGE B
P3	2A1A06J13A-10				
Q0	2B1A2-E3	6- 39			NOT D4 BIT 05 TO MCS VIA F1
Q1	2B1A2-E2	6- 39			
Q2	2A1A06J14B-02				
Q3	2A1A06J14B-01				BIT 05 FROM INTERNAL STORAGE B
R0	2A2B6-M3	5- 17			
R1	2A2B6-M2	5- 17			BIT 05 OUT OF PF TO DB XMTR
R2	2A1A06J12B-02				
R3	2A1A06J12B-01				BIT 05 FROM INTERNAL STORAGE A
S0	2B2A8-H1	5- 59	2B2A8-AL		NOT MAIN CONTROL DATA BIT 05
S2	2A1A06J11A-10				
S3	2A1A06J11A-09				BIT 04 TO INTERNAL STORAGE A
T0	2A2A3-V0	5- 35			
T1	2A2A3-V1	5- 35			DATA TO PF QUADRANT 0, BIT 05
T2	2B1A2-E0	6- 39			
T3	2B1A2-E1	6- 39			NOT BC READ BIT 05
U0	2A1A06J11B-02				
U1	2A1A06J11B-01				BIT 05 TO INTERNAL STORAGE A
U2	2B2A9-U3	5- 57	2B2A9-AZ		PARITY CHECK, GROUP 1 ODD
U3	2B2A9-V3	5- 57	2B2A8-AZ		PARITY CHECK, GROUP 0 EVEN
V0	2A1A06J13B-01				BIT 05 TO INTERNAL STORAGE B
V1	2A1A06J13B-02				
V2	2B2A9-U2	5- 57	2B2A8-AY		PARITY CHECK, GROUP 0 ODD
V3	2B2A9-V2	5- 57	2B2A9-AY		PARITY CHECK, GROUP 1 EVEN
W0	2A2A2-V1	5- 41			DATA TO PF QUADRANT 1, BIT 05
W1	2A2A2-V0	5- 41			
W2	2A1A06P01B-01				NOT MAIN CONTROL READ, BIT 05
	1A4A06J04B-01				
	1A0B6-W0	2- 67			
W3	2A1A06P01B-02				
	1A4A06J04B-02				
	1A0B6-W1	2- 67			
X0	2A1A06P01E-01				NOT DO REGISTER BIT 05
	1A4A06J04E-01				
	1A0A6-H1	2- 57			
X1	2A1A06P01E-02				
	1A4A06J04E-02				
	1A0A6-H0	2- 57			
X2	2A1A06J09B-01				BIT 05 TO/FROM EXTERNAL STOR
	2A1A06J10B-01				
X3	2A1A06J09B-02				
	2A1A06J10B-02				



CONTROL DATA DEVELOPMENT DIVISION	DATA BUS BITS 03-05 AND DATA PARITY GENERATOR/CHECKER	PRODUCT	
	LOC: 2B2A8 PART NO. 184668 SER. 001	SIZE C	DRAWING NO. 60181000 REV. A
		SHEET	PAGE 5-59

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A3	2B2A5-J1	5- 73	2B2A5-AR	PARITY CHECK, CHARACTER 2 EVEN
B2	2B1B4-X1	6- 29		
B3	2R1B4-X0	6- 29		NOT RC READ BIT 06
C0	2B2A5-U1	5- 73	2B2A7-A0	DATA TRANSMITTERS ON
C2	2A1A06J13B-03			BIT 06 TO INTERNAL STORAGE B
C3	2A1A06J13B-04			
D0	2B1B4-K2	6- 29		
D1	2R1B4-K3	6- 29		NOT D4 BIT 06 TO MCS VIA FI
D2	2A1A06J11B-04			
D3	2A1A06J11B-03			BIT 06 TO INTERNAL STORAGE A
E0	2A1A06P01E-03			NOT MD REGISTER BIT 06
	1A4A06J04E-03			
	1A0A4-C1	2- 59		
E1	2A1A06P01E-04			
	1A4A06J04E-04			
	1A0A4-C0	2- 59		
E2	2A1A06P01B-03			NOT MAIN CONTROL READ, BIT 06
	1A4A06J04B-03			
	1A0B4-E1	2- 69		
E3	2A1A06P01B-04			
	1A4A06J04B-04			
	1A0B4-E0	2- 69		

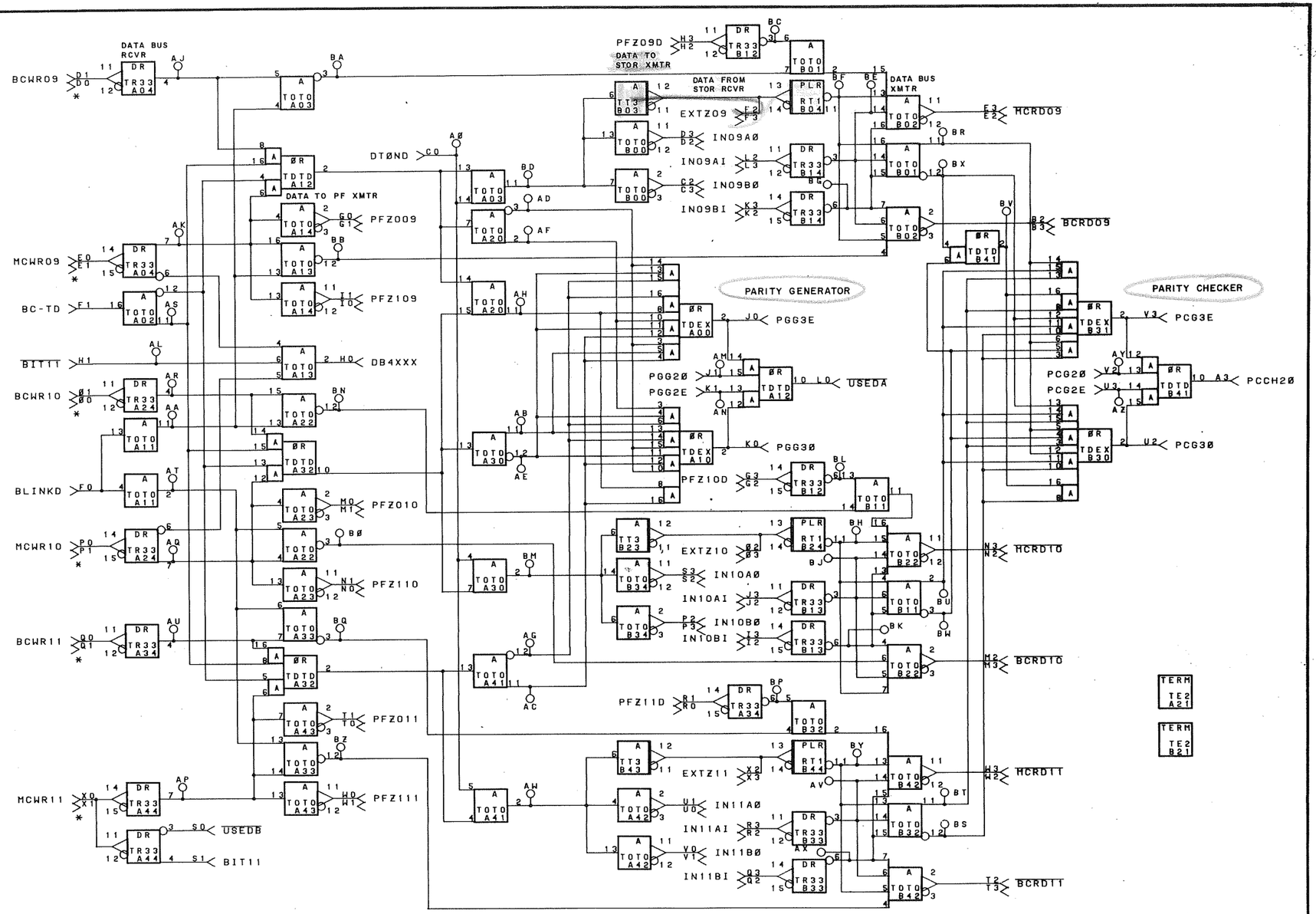
F0	2B2A5-S2	5- 73		LINK MN CONT/BC DB REG THRU DB
F1	2B2A5-N3	5- 73		BLOCK CONTROL DATA XMIT ENABLE
F2	2A1A06J09B-03			BIT 06 TO/FROM EXTERNAL STOR
	2A1A06J10R-03			
F3	2A1A06J09B-04			
	2A1A06J10B-04			
G0	2A2A3-S1	5- 33		DATA TO PF QUADRANT 0, BIT 06
G1	2A2A3-S0	5- 33		
G2	2A2B5-N3	5- 19		
G3	2A2B5-M2	5- 19		BIT 07 OUT OF PF TO DB XMTR
H0	2B2B9-J0	5- 75	2B2B9-RT	MAIN CONTROL DATA BITS 06-08=0
H1	2B2A7-S0	5- 61	2B2A7-AL	NOT MAIN CONTROL DATA BIT 08
H2	2A2B5-03	5- 19		
H3	2A2B5-02	5- 19		BIT 06 OUT OF PF TO DB XMTR
I0	2A2A2-S0	5- 39		
I1	2A2A2-S1	5- 39		DATA TO PF QUADRANT 1, BIT 06
I2	2A1A06J14B-06			
I3	2A1A06J14B-05			BIT 07 FROM INTERNAL STORAGE B
J0	2B2A6-K1	5- 63	2B2A6-AN	PARITY GENERATOR, GROUP 2 EVEN
J1	2B2A6-J0	5- 63	2B2A7-AH	PARITY GENERATOR, GROUP 3 EVEN
J2	2A1A06J12B-06			
J3	2A1A06J12B-05			BIT 07 FROM INTERNAL STORAGE A
K0	2B2A6-J1	5- 63	2B2A6-AM	PARITY GENERATOR, GROUP 2 ODD
K1	2B2A6-K0	5- 63	2B2A7-AN	PARITY GENERATOR, GROUP 3 ODD
K2	2A1A06J14B-04			
K3	2A1A06J14B-03			BIT 06 FROM INTERNAL STORAGE B
L0	2B2A5-A0	5- 73	2B2A5-AB	PARITY GEN,, CHARACTER 2 EVEN
L2	2A1A06J12B-03			BIT 06 FROM INTERNAL STORAGE A
L3	2A1A06J12B-04			
M0	2A2A3-R1	5- 33		DATA TO PF QUADRANT 0, BIT 07
M1	2A2A3-R0	5- 33		
M2	2B1B3-X1	6- 31		
M3	2B1B3-X0	6- 31		NOT BC READ BIT 07
N0	2A2A2-R0	5- 39		
N1	2A2A2-R1	5- 39		DATA TO PF QUADRANT 1, BIT 07
N2	2A1A06P01B-05			NOT MAIN CONTROL READ, BIT 07
	1A4A06J04B-05			
	1A0B4-F1	2- 69		
N3	2A1A06P01B-06			
	1A4A06J04R-06			
	1A0B4-F0	2- 69		
O0	2B1B3-K2	6- 31		
O1	2B1B3-K3	6- 31		NOT D4 BIT 07 TO MCS VIA F1
O2	2A1A06J09B-05			BIT 07 TO/FROM EXTERNAL STOR
	2A1A06J10R-05			
O3	2A1A06J09A-06			
	2A1A06J10B-06			
P0	2A1A06P01E-05			NOT DO REGISTER BIT 07
	1A4A06J04E-05			
	1A0A4-B1	2- 59		
P1	2A1A06P01E-06			
	1A4A06J04E-06			
	1A0A4-B0	2- 59		
P2	2A1A06J13B-05			BIT 07 TO INTERNAL STORAGE B
P3	2A1A06J13R-06			
Q0	2B1B2-K3	6- 33		NOT D4 BIT 08 TO MCS VIA F1
Q1	2B1B2-K2	6- 33		
Q2	2A1A06J14R-08			
Q3	2A1A06J14B-07			BIT 08 FROM INTERNAL STORAGE B
R0	2A2B4-S3	5- 21		
R1	2A2B4-S2	5- 21		BIT 08 OUT OF PF TO DB XMTR
R2	2A1A06J12B-08			
R3	2A1A06J12B-07			BIT 08 FROM INTERNAL STORAGE A
S0	2B2A7-H1	5- 61	2B2A7-AL	NOT MAIN CONTROL DATA BIT 08
S2	2A1A06J11B-06			
S3	2A1A06J11B-05			BIT 07 TO INTERNAL STORAGE A
T0	2A2A3-Q0	5- 33		
T1	2A2A3-Q1	5- 33		DATA TO PF QUADRANT 0, BIT 08
T2	2B1B2-X1	6- 33		
T3	2B1B2-X0	6- 33		NOT BC READ BIT 08
U0	2A1A06J11B-08			
U1	2A1A06J11B-07			BIT 08 TO INTERNAL STORAGE A
U2	2B2A6-V2	5- 63	2B2A6-AY	PARITY CHECK, GROUP 2 ODD
U3	2B2A6-U2	5- 63	2B2A7-AZ	PARITY CHECK, GROUP 3 ODD
V0	2A1A06J13R-07			BIT 08 TO INTERNAL STORAGE B
V1	2A1A06J13B-08			
V2	2B2A6-V3	5- 63	2B2A7-AY	PARITY CHECK, GROUP 3 EVEN
V3	2B2A6-U3	5- 63	2B2A6-AZ	PARITY CHECK, GROUP 2 EVEN
W0	2A2A2-Q1	5- 39		DATA TO PF QUADRANT 1, BIT 08
W1	2A2A2-Q0	5- 39		
W2	2A1A06P01B-07			NOT MAIN CONTROL READ, BIT 08
	1A4A06J04R-07			
	1A0B4-H0	2- 69		
W3	2A1A06P01R-08			
	1A4A06J04R-08			
	1A0B4-H1	2- 69		
X0	2A1A06P01E-07			NOT DO REGISTER BIT 08
	1A4A06J04E-07			
	1A0A4-H1	2- 59		
X1	2A1A06P01E-08			
	1A4A06J04E-08			
	1A0A4-H0	2- 59		
X2	2A1A06J09B-07			BIT 08 TO/FROM EXTERNAL STOR
	2A1A06J10R-07			
X3	2A1A06J09B-08			
	2A1A06J10B-08			



CONTROL DATA DEVELOPMENT DIVISION	DATA BUS BITS 06-08 AND DATA PARITY GENERATOR/CHECKER	PRODUCT	
	LOC: 2B2A7 PART NO. 184668 SER.002	SIZE C	DRAWING NO. 60181000 REV. A
		SHEET	PAGE 5-61

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A3	2B2A5-J0	5- 73	2B2A5-AP	PARITY CHECK, CHARACTER 2 ODD
B2	2B1A4-X1	6- 35		
B3	2B1A4-X0	6- 35		NOT AC READ BIT 09
C0	2B2A5-Q0	5- 73	2B2A6-A0	DATA TRANSMITTERS ON
C2	2A1A06J13B-09			BIT 09 TO INTERNAL STORAGE B
C3	2A1A06J13B-10			
D0	2B1A4-K2	6- 35		
D1	2B1A4-K3	6- 35		NOT D4 BIT 09 TO MCS VIA F1
D2	2A1A06J11B-10			
D3	2A1A06J11B-09			BIT 09 TO INTERNAL STORAGE A
E0	2A1A06P01E-09			NOT DO REGISTER BIT 09
	1A4A06J04E-09			
	1A0A2-C1	2- 61		
E1	2A1A06P01E-10			
	1A4A06J04E-10			
	1A0A2-C0	2- 61		
E2	2A1A06P01B-09			NOT MAIN CONTROL READ, BIT 09
	1A4A06J04B-09			
	1A0B2-E1	2- 71		
E3	2A1A06P01B-10			
	1A4A06J04B-10			

	1A0B2-E0	2- 71		
F0	2B2A5-T3	5- 73		LINK MN CONT/BC DB REG THRU DE
F1	2B2A5-Q2	5- 73		BLOCK CONTROL DATA XMIT ENABLE
F2	2A1A06J09B-09			BIT 09 TO/FROM EXTERNAL STOR
	2A1A06J10B-09			
F3	2A1A06J09B-10			
	2A1A06J10B-10			
G0	2A2A3-P1	5- 33		DATA TO PF QUADRANT 0, BIT 09
G1	2A2A3-P0	5- 33		
G2	2A2B4-W1	5- 21		
G3	2A2B4-W0	5- 21		BIT 10 OUT OF PF TO DB XMTR
H0	2B2B9-B1	5- 75	2B2B9-RR	MAIN CONTROL DATA BITS 09-11=4
H1	2B2A6-S1	5- 63	2B2A6-AL	MAIN CONTROL DATA BIT 11
H2	2A2B4-T0	5- 21		
H3	2A2B4-T1	5- 21		BIT 09 OUT OF PF TO DB XMTR
I0	2A2A2-P0	5- 39		
I1	2A2A2-P1	5- 39		DATA TO PF QUADRANT 1, BIT 09
I2	2A1A06J14C-02			
I3	2A1A06J14C-01			BIT 10 FROM INTERNAL STORAGE B
J0	2B2A7-J1	5- 61	2B2A7-AM	PARITY GENERATOR, GROUP 3 EVEN
J1	2B2A7-K0	5- 61	2B2A6-AM	PARITY GENERATOR, GROUP 2 ODD
J2	2A1A06J12C-02			
J3	2A1A06J12C-01			BIT 10 FROM INTERNAL STORAGE A
K0	2B2A7-K1	5- 61	2B2A7-AN	PARITY GENERATOR, GROUP 3 ODD
K1	2B2A7-J0	5- 61	2B2A6-AN	PARITY GENERATOR, GROUP 2 EVEN
K2	2A1A06J14B-10			
K3	2A1A06J14B-09			BIT 09 FROM INTERNAL STORAGE B
L2	2A1A06J12B-09			BIT 09 FROM INTERNAL STORAGE A
L3	2A1A06J12B-10			
M0	2A2A3-N1	5- 33		DATA TO PF QUADRANT 0, BIT 10
M1	2A2A3-N0	5- 33		
M2	2B1A3-X1	6- 37		
M3	2B1A3-X0	6- 37		NOT BC READ BIT 10
N0	2A2A2-N0	5- 39		
N1	2A2A2-N1	5- 39		DATA TO PF QUADRANT 1, BIT 10
N2	2A1A06P01C-01			NOT MAIN CONTROL READ, BIT 10
	1A4A06J04C-01			
	1A0B2-F1	2- 71		
N3	2A1A06P01C-02			
	1A4A06J04C-02			
	1A0B2-F0	2- 71		
O0	2B1A3-K2	6- 37		
O1	2B1A3-K3	6- 37		NOT D4 BIT 10 TO MCS VIA F1
O2	2A1A06J09C-01			BIT 10 TO/FROM EXTERNAL STOR
	2A1A06J10C-01			
O3	2A1A06J09C-02			
	2A1A06J10C-02			
P0	2A1A06P01F-01			NOT D0 REGISTER BIT 10
	1A4A06J04F-01			
	1A0A2-B1	2- 61		
P1	2A1A06P01F-02			
	1A4A06J04F-02			
	1A0A2-B0	2- 61		
P2	2A1A06J13C-01			BIT 10 TO INTERNAL STORAGE B
P3	2A1A06J13C-02			
Q0	2B1A2-K3	6- 39		NOT D4 BIT 11 TO MCS VIA F1
Q1	2B1A2-K2	6- 39		
Q2	2A1A06J14C-04			
Q3	2A1A06J14C-03			BIT 11 FROM INTERNAL STORAGE B
R0	2A2B4-U3	5- 21		
R1	2A2B4-U2	5- 21		BIT 11 OUT OF PF TO DB XMTR
R2	2A1A06J12C-04			
R3	2A1A06J12C-03			BIT 11 FROM INTERNAL STORAGE A
S1	2B2A6-H1	5- 63	2B2A6-AL	MAIN CONTROL DATA BIT 11
S2	2A1A06J11C-02			
S3	2A1A06J11C-01			BIT 10 TO INTERNAL STORAGE A
T0	2A2A3-O0	5- 33		
T1	2A2A3-O1	5- 33		DATA TO PF QUADRANT 0, BIT 11
T2	2B1A2-X1	6- 39		
T3	2B1A2-X0	6- 39		NOT BC READ BIT 11
U0	2A1A06J11C-04			
U1	2A1A06J11C-03			BIT 11 TO INTERNAL STORAGE A
U2	2B2A7-U3	5- 61	2B2A7-AZ	PARITY CHECK, GROUP 3 ODD
U3	2B2A7-V3	5- 61	2B2A6-AZ	PARITY CHECK, GROUP 2 EVEN
V0	2A1A06J13C-03			BIT 11 TO INTERNAL STORAGE B
V1	2A1A06J13C-04			
V2	2B2A7-U2	5- 61	2B2A6-AY	PARITY CHECK, GROUP 2 ODD
V3	2B2A7-V2	5- 61	2B2A7-AY	PARITY CHECK, GROUP 3 EVEN
W0	2A2A2-O1	5- 39		DATA TO PF QUADRANT 1, BIT 11
W1	2A2A2-O0	5- 39		
W2	2A1A06P01C-03			NOT MAIN CONTROL READ, BIT 11
	1A4A06J04C-03			
	1A0B2-W0	2- 71		
W3	2A1A06P01C-04			
	1A4A06J04C-04			
	1A0B2-W1	2- 71		
X0	2A1A06P01F-03			NOT D0 REGISTER BIT 11
	1A4A06J04F-03			
	1A0A2-H1	2- 61		
X1	2A1A06P01F-04			
	1A4A06J04F-04			
	1A0A2-H0	2- 61		
X2	2A1A06J09C-03			BIT 11 TO/FROM EXTERNAL STOR
	2A1A06J10C-03			
X3	2A1A06J09C-04			
	2A1A06J10C-04			



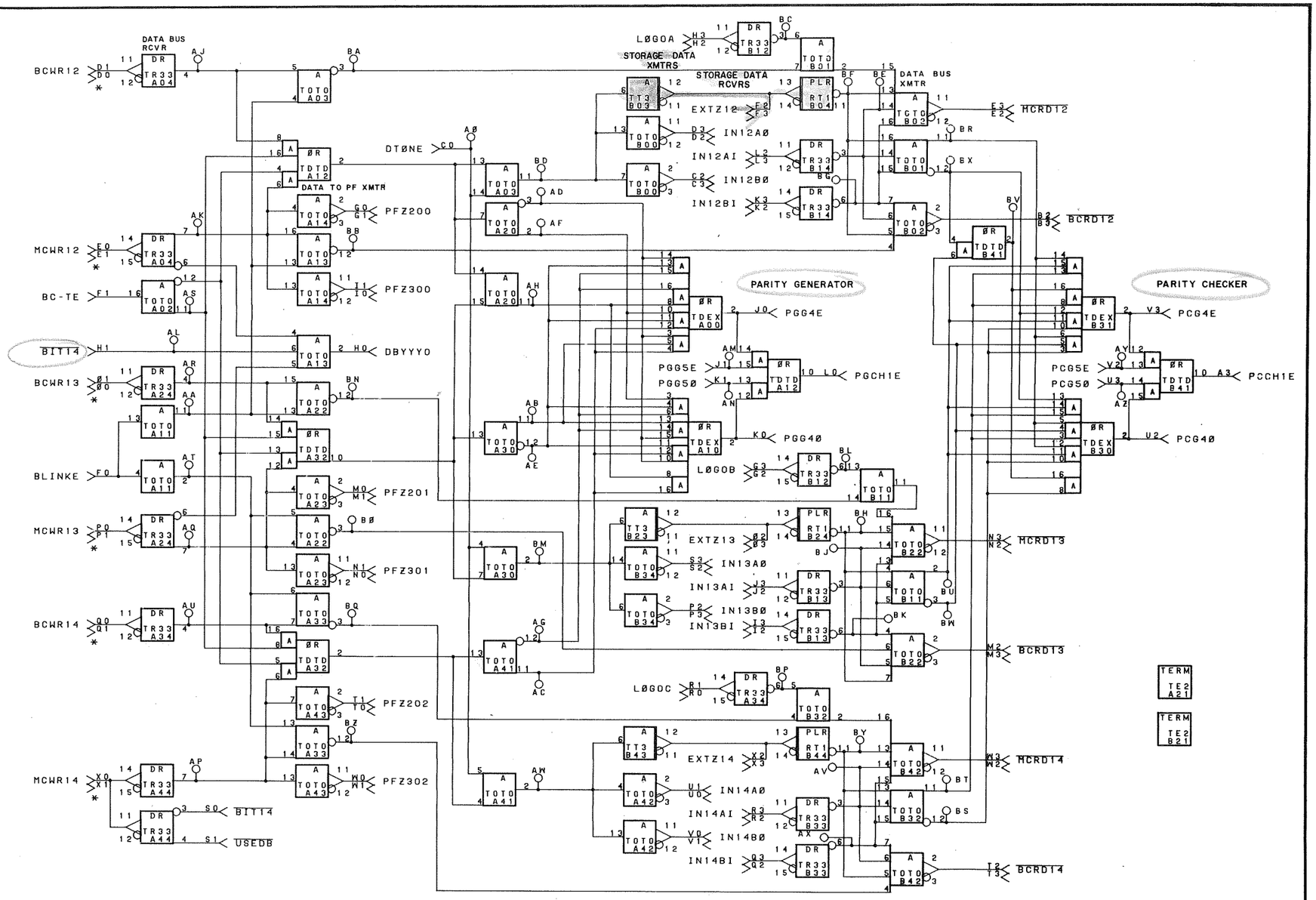
CONTROL DATA
DEVELOPMENT DIVISION

DATA BUS BITS 09-11
AND DATA PARITY
GENERATOR/CHECKER
LOC: 2B2A6 PART NO. 184668 SER. 003

PRODUCT
SIZE C | DRAWING NO. 60181000 | REV. A
SHEET | PAGE 5-63

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A3	2B2A5-V1	5- 73	2B2A5-RH	PARITY CHECK, CHARACTER 1 EVEN
B2	2B1B4-D0	6- 29		
B3	2B1B4-D1	6- 29		NOT BC READ BIT 12
C0	2B2A5-P0	5- 73	2B2A4-A0	DATA TRANSMITTERS ON
C2	2A1A06J13C-05			BIT 12 TO INTERNAL STORAGE B
C3	2A1A06J13C-06			
D0	2B1B4-02	6- 29		
D1	2B1B4-03	6- 29		NOT D4 BIT 12 TO MCS VIA F1
D2	2A1A06J11C-06			
D3	2A1A06J11C-05			BIT 12 TO INTERNAL STORAGE A
E0	2A1A06P01F-05			NOT DO REGISTER BIT 12
	1A4A06J04F-05			
	1A0A0-C1	2- 63		
E1	2A1A06P01F-06			
	1A4A06J04F-06			
	1A0A0-C0	2- 63		

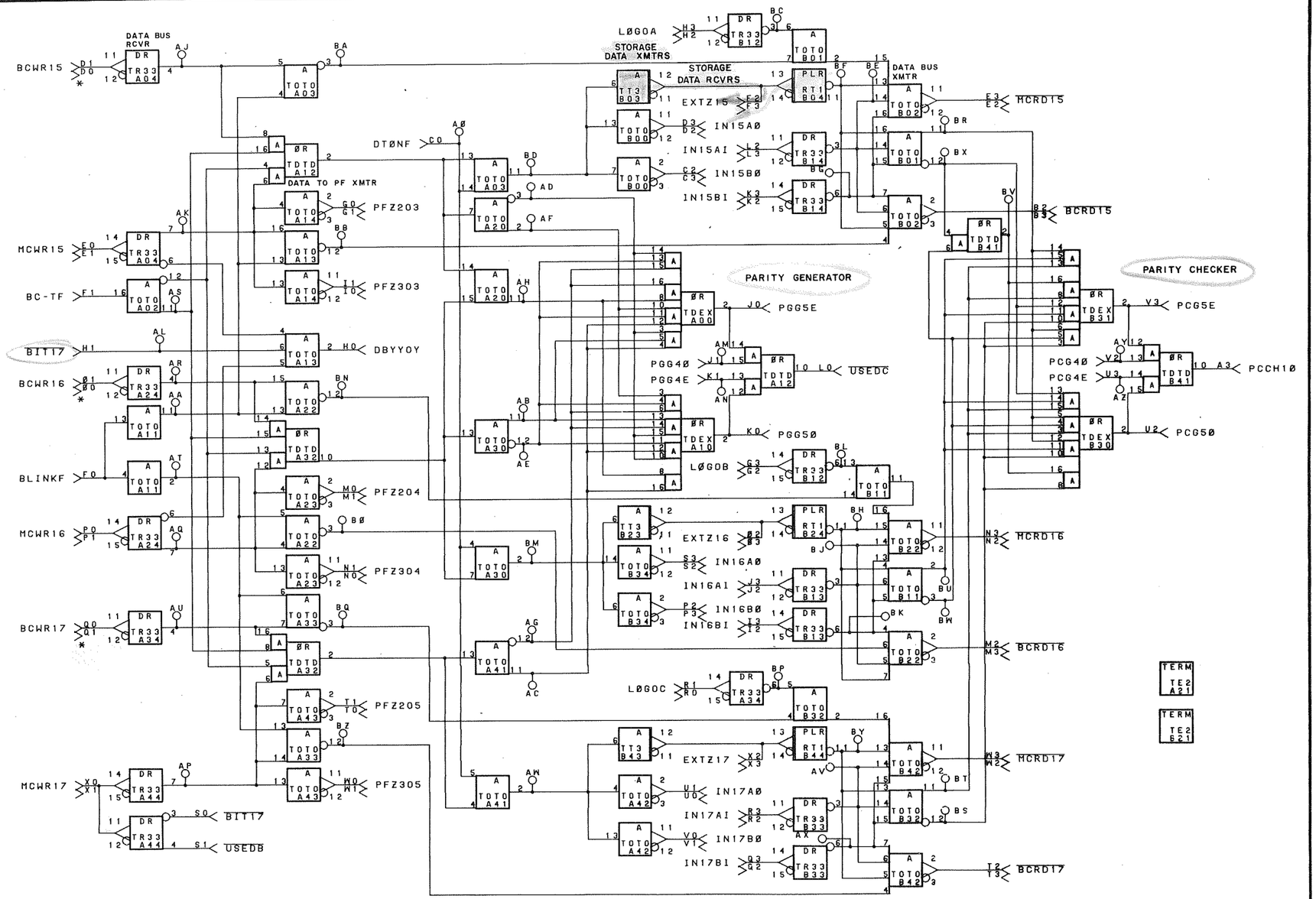
E2	2A1A06P01C-05 1A4A06J04C-05 1A0B0-E1	2- 73		NOT MAIN CONTROL READ, BIT 12
E3	2A1A06P01C-06 1A4A06J04C-06 1A0B0-E0	2- 73		
F0	2B2A5-P2	5- 73		LINK MN CONT/BC DB REG THRU DB
F1	2B2A5-N2	5- 73		BLOCK CONTROL DATA XMIT ENABLE
F2	2A1A06J09C-05 2A1A06J10C-05			BIT 12 TO/FROM EXTERNAL STOR
F3	2A1A06J09C-06 2A1A06J10C-06			
G0	2A2B1-B1	5- 47		DATA TO PF QUADRANT 2, BIT 00
G1	2A2R1-B0	5- 47		
H0	2B2B8-H1	5- 77	2B2B8-RU	MAIN CONTROL DATA BITS 00-02=0
H1	2B2A4-S0	5- 65	2B2A4-AL	NOT MAIN CONTROL DATA BIT 14
I0	2A2B0-B0	5- 53		
I1	2A2B0-B1	5- 53		DATA TO PF QUADRANT 3, BIT 00
I2	2A1A06J14C-08			
I3	2A1A06J14C-07			BIT 13 FROM INTERNAL STORAGE B
J0	2B2A3-K1	5- 67	2B2A3-AN	PARITY GENERATOR, GROUP 4 EVEN
J1	2B2A3-J0	5- 67	2B2A4-AM	PARITY GENERATOR, GROUP 5 EVEN
J2	2A1A06J12C-08			
J3	2A1A06J12C-07			BIT 13 FROM INTERNAL STORAGE A
K0	2B2A3-J1	5- 67	2B2A3-AM	PARITY GENERATOR, GROUP 4 ODD
K1	2B2A3-K0	5- 67	2B2A4-AN	PARITY GENERATOR, GROUP 5 ODD
K2	2A1A06J14C-06			
K3	2A1A06J14C-05			BIT 12 FROM INTERNAL STORAGE B
L0	2B2A5-K2	5- 73	2B2A5-RV	PARITY GEN,, CHARACTER 1 EVEN
L2	2A1A06J12C-05			BIT 12 FROM INTERNAL STORAGE A
L3	2A1A06J12C-06			
M0	2A2A1-X1	5- 47		DATA TO PF QUADRANT 2, BIT 01
M1	2A2A1-X0	5- 47		
M2	2B1B3-D0	6- 31		
M3	2B1B3-D1	6- 31		NOT BC READ BIT 13
N0	2A2A0-X0	5- 53		
N1	2A2A0-X1	5- 53		DATA TO PF QUADRANT 3, BIT 01
N2	2A1A06P01C-07 1A4A06J04C-07 1A0B0-F1	2- 73		NOT MAIN CONTROL READ, BIT 13
N3	2A1A06P01C-08 1A4A06J04C-08 1A0B0-F0	2- 73		
O0	2B1B3-02	6- 31		
O1	2B1B3-03	6- 31		NOT D4 BIT 13 TO MCS V1A F1
O2	2A1A06J09C-07 2A1A06J10C-07			BIT 13 TO/FROM EXTERNAL STOR
O3	2A1A06J09C-08 2A1A06J10C-08			
P0	2A1A06P01F-07 1A4A06J04F-07 1A0A0-B1	2- 63		NOT D0 REGISTER BIT 13
P1	2A1A06P01F-08 1A4A06J04F-08 1A0A0-B0	2- 63		
P2	2A1A06J13C-07			BIT 13 TO INTERNAL STORAGE B
P3	2A1A06J13C-08			
Q0	2B1B2-03	6- 33		NOT D4 BIT 14 TO MCS V1A F1
Q1	2B1B2-02	6- 33		
Q2	2A1A06J14C-10			BIT 14 FROM INTERNAL STORAGE B
Q3	2A1A06J14C-09			
R2	2A1A06J12C-10			BIT 14 FROM INTERNAL STORAGE A
R3	2A1A06J12C-09			
S0	2B2A4-H1	5- 65	2B2A4-AL	NOT MAIN CONTROL DATA BIT 14
S2	2A1A06J11C-08			
S3	2A1A06J11C-07			BIT 13 TO INTERNAL STORAGE A
T0	2A2A1-W0	5- 47		
T1	2A2A1-W1	5- 47		DATA TO PF QUADRANT 2, BIT 02
T2	2B1B2-D0	6- 33		
T3	2B1B2-D1	6- 33		NOT BC READ BIT 14
U0	2A1A06J11C-10			
U1	2A1A06J11C-09			BIT 14 TO INTERNAL STORAGE A
U2	2B2A3-V2	5- 67	2B2A3-AY	PARITY CHECK, GROUP 4 ODD
U3	2B2A3-U2	5- 67	2B2A4-AZ	PARITY CHECK, GROUP 5 ODD
V0	2A1A06J13C-09			BIT 14 TO INTERNAL STORAGE B
V1	2A1A06J13C-10			
V2	2B2A3-V3	5- 67	2B2A4-AY	PARITY CHECK, GROUP 5 EVEN
V3	2B2A3-U3	5- 67	2B2A3-AZ	PARITY CHECK, GROUP 4 EVEN
W0	2A2A0-W1	5- 53		DATA TO PF QUADRANT 3, BIT 02
W1	2A2A0-W0	5- 53		
W2	2A1A06P01C-09 1A4A06J04C-09 1A0B0-W0	2- 73		NOT MAIN CONTROL READ, BIT 14
W3	2A1A06P01C-10 1A4A06J04C-10 1A0B0-W1	2- 73		
X0	2A1A06J06E-07 1A4A06P01E-07 1A0A0-W1	2- 63		NOT D0 REGISTER BIT 14
X1	2A1A06J06E-08 1A4A06P01E-08 1A0A0-W0	2- 63		
X2	2A1A06J09C-09 2A1A06J10C-09			BIT 14 TO/FROM EXTERNAL STOR
X3	2A1A06J09C-10 2A1A06J10C-10			



CONTROL DATA DEVELOPMENT DIVISION	DATA BUS BITS 12-14 AND DATA PARITY GENERATOR/CHECKER LOC: 2B2A4 PART NO. 184668 SER.004	PRODUCT	
		SIZE C	DRAWING NO. 60181000 REV. A
		SHEET	PAGE

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A3	2B2A5-K3	5- 73	2B2A5-RS	PARITY CHECK, CHARACTER 1 ODD
B2	2B1A4-D0	6- 35		
B3	2B1A4-D1	6- 35		NOT BC READ BIT 15
C0	2B2A5-01	5- 73	2B2A3-A0	DATA TRANSMITTERS ON
C2	2A1A06J13D-01			BIT 15 TO INTERNAL STORAGE B
C3	2A1A06J13D-02			
D0	2B1A4-02	6- 35		
D1	2B1A4-03	6- 35		NOT D4 BIT 15 TO MCS VIA FI
D2	2A1A06J11D-02			
D3	2A1A06J11D-01			BIT 15 TO INTERNAL STORAGE A
E0	2A1A06P04E-03			DO REGISTER BIT 15
	1A4A06J10E-03			
	1BDA2-F0	2- 31		
E1	2A1A06P04E-04			
	1A4A06J10B-04			

	1B0A2=F1	2= 31			
E2	2A1A06P04C=05				NOT MAIN CONTROL READ, BIT 15
	1A4A06J10C=05				
	1B0A2=Q0	2= 31			
E3	2A1A06P04C=06				
	1A4A06J10C=06				
	1B0A2=Q1	2= 31			
F0	2B2A5=Q3	5= 73			LINK MN CONT/BC DB REG THRU DB
F1	2B2A5=R3	5= 73			BLOCK CONTROL DATA XMIT ENABLE
F2	2A1A06J09D=01				BIT 15 TO/FROM EXTERNAL STOR
	2A1A06J10D=01				
F3	2A1A06J09D=02				
	2A1A06J10D=02				
G0	2A2A1=T1	5= 47			DATA TO PF QUADRANT 2, BIT 03
G1	2A2A1=T0	5= 47			
H0	2B2B8=H0	5= 77	2B2B8=RS		MAIN CONTROL DATA BITS 03=05=0
H1	2B2A3=S0	5= 67	2B2A3=AL		NOT MAIN CONTROL DATA BIT 17
I0	2A2A0=T0	5= 53			
I1	2A2A0=T1	5= 53			DATA TO PF QUADRANT 3, BIT 03
I2	2A1A06J14D=04				
I3	2A1A06J14D=03				BIT 16 FROM INTERNAL STORAGE B
J0	2B2A4=J1	5= 65	2B2A4=AM		PARITY GENERATOR, GROUP 5 EVEN
J1	2B2A4=K0	5= 65	2B2A3=AM		PARITY GENERATOR, GROUP 4 ODD
J2	2A1A06J12D=04				
J3	2A1A06J12D=03				BIT 16 FROM INTERNAL STORAGE A
K0	2B2A4=K1	5= 65	2B2A4=AN		PARITY GENERATOR, GROUP 5 ODD
K1	2B2A4=J0	5= 65	2B2A3=AN		PARITY GENERATOR, GROUP 4 EVEN
K2	2A1A06J14D=02				
K3	2A1A06J14D=01				BIT 15 FROM INTERNAL STORAGE B
L2	2A1A06J12D=01				BIT 15 FROM INTERNAL STORAGE A
L3	2A1A06J12D=02				
M0	2A2A1=U1	5= 47			DATA TO PF QUADRANT 2, BIT 04
M1	2A2A1=U0	5= 47			
M2	2B1A3=D0	6= 37			
M3	2B1A3=D1	6= 37			NOT BC READ BIT 16
N0	2A2A0=U0	5= 53			
N1	2A2A0=U1	5= 53			DATA TO PF QUADRANT 3, BIT 04
N2	2A1A06P04C=07				NOT MAIN CONTROL READ, BIT 16
	1A4A06J10C=07				
	1B0A2=E3	2= 31			
N3	2A1A06P04C=08				
	1A4A06J10C=08				
	1B0A2=E2	2= 31			
O0	2B1A3=O2	6= 37			
O1	2B1A3=O3	6= 37			NOT D4 BIT 16 TO MCS VIA F1
O2	2A1A06J09D=03				BIT 16 TO/FROM EXTERNAL STOR
	2A1A06J10D=03				
O3	2A1A06J09D=04				
	2A1A06J10D=04				
P0	2A1A06P04E=05				DO REGISTER BIT 16
	1A4A06J10E=05				
	1B0A2=01	2= 31			
P1	2A1A06P04E=06				
	1A4A06J10E=06				
	1B0A2=00	2= 31			
P2	2A1A06J13D=03				BIT 16 TO INTERNAL STORAGE B
P3	2A1A06J13D=04				
Q0	2B1A2=03	6= 39			NOT D4 BIT 17 TO MCS VIA F1
Q1	2B1A2=02	6= 39			
Q2	2A1A06J14D=06				BIT 17 FROM INTERNAL STORAGE B
Q3	2A1A06J14D=05				
R2	2A1A06J12D=06				BIT 17 FROM INTERNAL STORAGE A
R3	2A1A06J12D=05				
S0	2B2A3=H1	5= 67	2B2A3=AL		NOT MAIN CONTROL DATA BIT 17
S2	2A1A06J11D=04				
S3	2A1A06J11D=03				BIT 16 TO INTERNAL STORAGE A
T0	2A2A1=V0	5= 47			DATA TO PF QUADRANT 2, BIT 05
T1	2A2A1=V1	5= 47			
T2	2B1A2=D0	6= 39			NOT BC READ BIT 17
T3	2B1A2=D1	6= 39			
U0	2A1A06J11D=06				BIT 17 TO INTERNAL STORAGE A
U1	2A1A06J11D=05				
U2	2B2A4=U3	5= 65	2B2A4=AZ		PARITY CHECK, GROUP 5 ODD
U3	2B2A4=V3	5= 65	2B2A3=AZ		PARITY CHECK, GROUP 4 EVEN
V0	2A1A06J13D=05				BIT 17 TO INTERNAL STORAGE B
V1	2A1A06J13D=06				
V2	2B2A4=U2	5= 65	2B2A3=AY		PARITY CHECK, GROUP 4 ODD
V3	2B2A4=V2	5= 65	2B2A4=AY		PARITY CHECK, GROUP 5 EVEN
W0	2A2A0=V1	5= 53			DATA TO PF QUADRANT 3, BIT 05
W1	2A2A0=V0	5= 53			
W2	2A1A06P04C=09				NOT MAIN CONTROL READ, BIT 17
	1A4A06J10C=09				
	1B0A2=V2	2= 31			
W3	2A1A06P04C=10				
	1A4A06J10C=10				
	1B0A2=V3	2= 31			
X0	2A1A06P04E=07				DO REGISTER BIT 17
	1A4A06J10E=07				
	1B0A2=X1	2= 31			
X1	2A1A06P04E=08				
	1A4A06J10E=08				
	1B0A2=X0	2= 31			
X2	2A1A06J09D=05				BIT 17 TO/FROM EXTERNAL STOR
	2A1A06J10D=05				
X3	2A1A06J09D=06				
	2A1A06J10D=06				

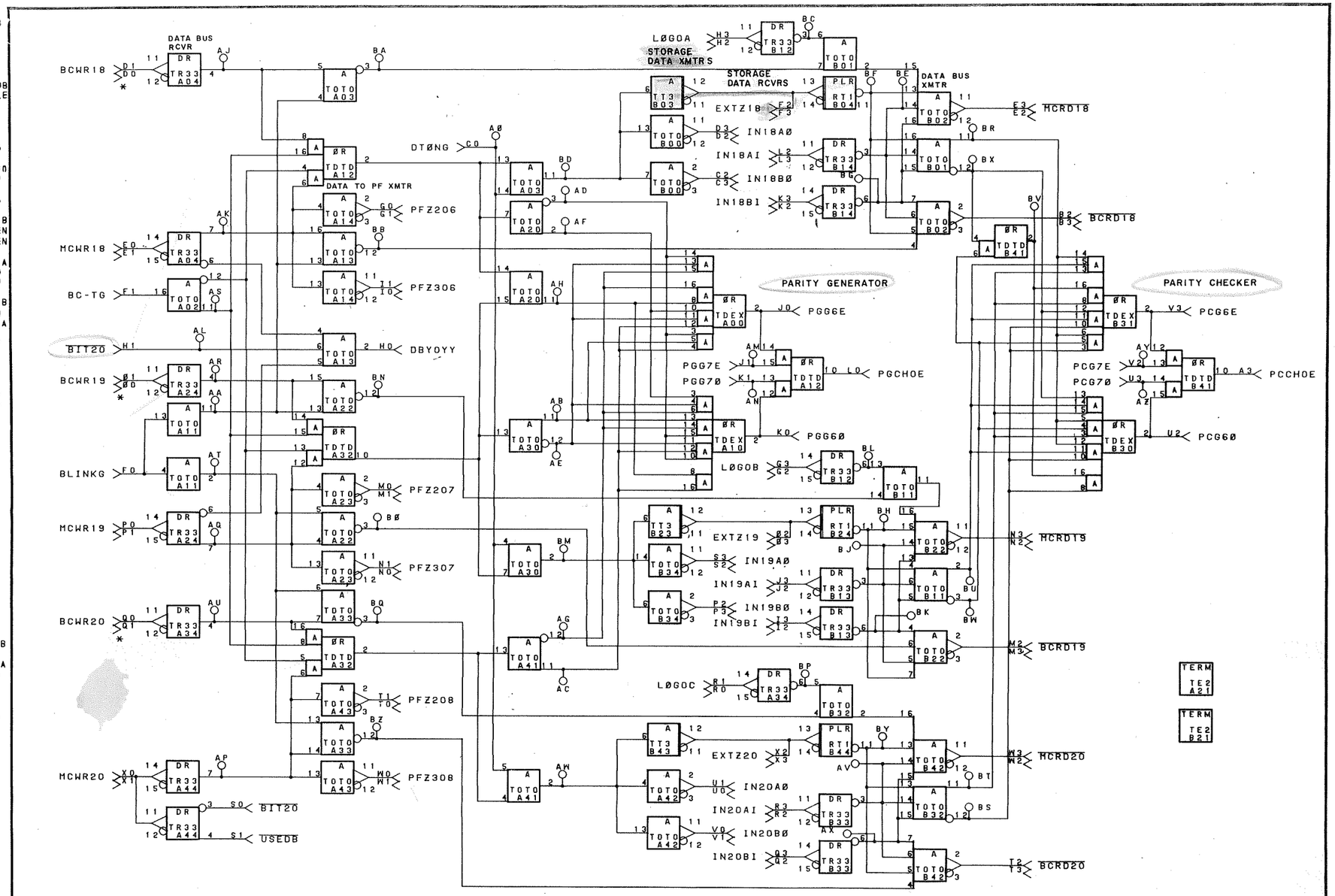


CONTROL DATA	DATA BUS BITS 15-17 AND DATA PARITY GENERATOR/CHECKER	PRODUCT	
DEVELOPMENT DIVISION	LOC: 2B2A3 PART NO. 184668 SER. 005	SIZE C / DRAWING NO. 60181000 / REV. A	SHEET / PAGE 5-67

147

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A3	2B2A5-I3	5- 73	2B2A5-R0	PARITY CHECK, CHARACTER 0 EVEN
B2	2B1B4-J0	6- 29		
B3	2B1B4-J1	6- 29		NOT BC READ BIT 18
C0	2B2A5-P1	5- 73	2B2A2-A0	DATA TRANSMITTERS ON
C2	2A1A06J13D-07			BIT 18 TO INTERNAL STORAGE B
C3	2A1A06J13D-08			
D0	2B1B4-L2	6- 29		
D1	2B1B4-L3	6- 29		NOT D4 BIT 18 TO MCS VIA FI
D2	2A1A06J11D-08			
D3	2A1A06J11D-07			BIT 18 TO INTERNAL STORAGE A
E0	2A1A06P04E-09			DO REGISTER BIT 18
	1A4A06J10E-09			
	1B0A1-F0	2- 33		
E1	2A1A06P04E-10			
	1A4A06J10E-10			
	1B0A1-F1	2- 33		

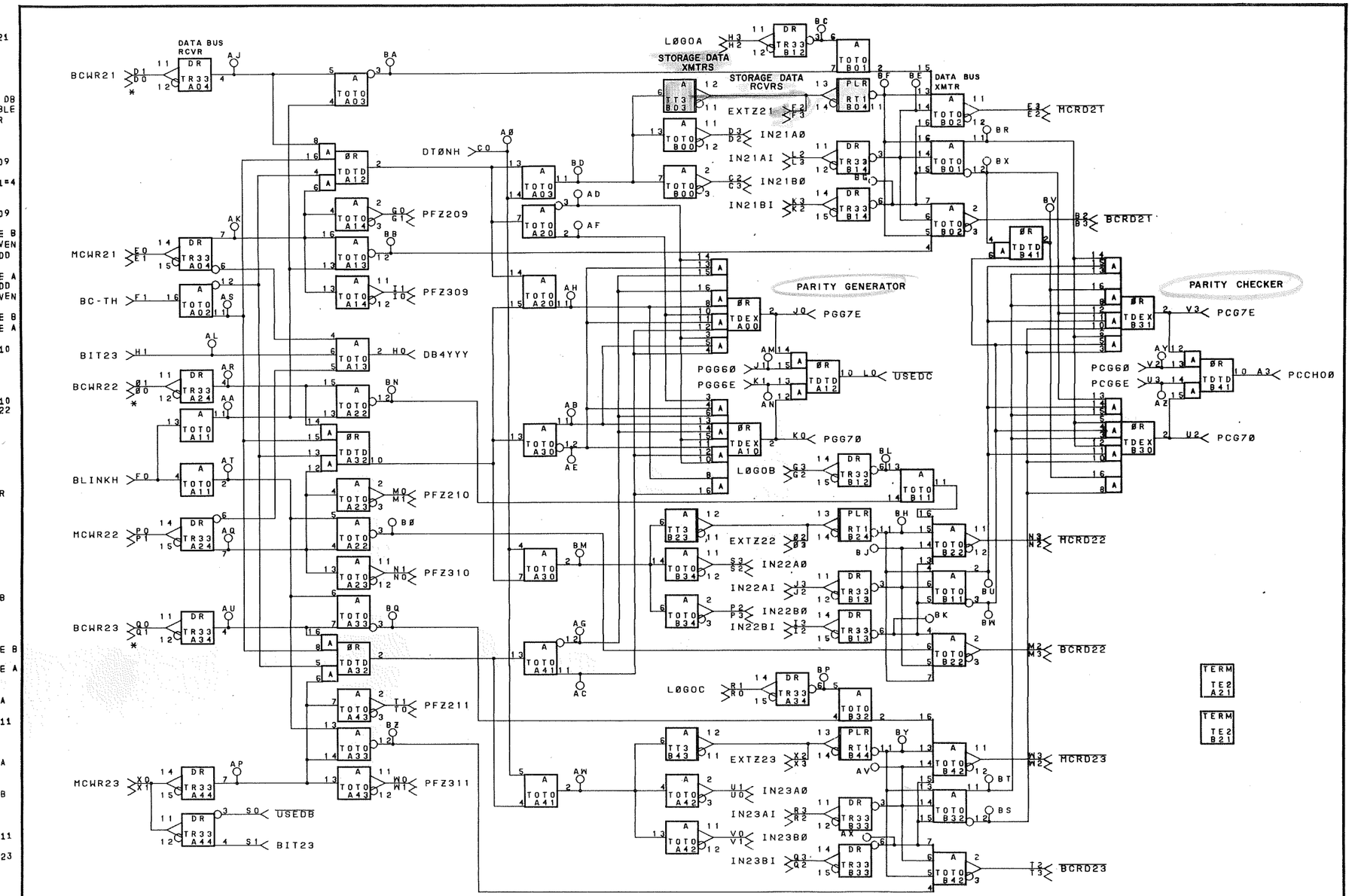
E2	2A1A06P04D-01				NOT MAIN CONTROL READ, BIT 18
	1A4A06J10D-01				
	1R0A1-Q0	2- 33			
E3	2A1A06P04D-02				
	1A4A06J10D-02				
	1R0A1-Q1	2- 33			
F0	2B2A5-X3	5- 73			LINK MN CONT/BC DB REG THRU DB
F1	2B2A5-03	5- 73			BLOCK CONTROL DATA XMIT ENABLE
F2	2A1A06J09D-07				BIT 18 TO/FROM EXTERNAL STOR
	2A1A06J10D-07				
F3	2A1A06J09D-08				
	2A1A06J10D-08				
G0	2A2A1-S1	5- 45			DATA TO PF QUADRANT 2, BIT 06
G1	2A2A1-S0	5- 45			
H0	2B2B8-J0	5- 77	2B2B8-RT		MAIN CONTROL DATA BITS 06-08-0
H1	2B2A2-S0	5- 69	2B2A2-AL		NOT MAIN CONTROL DATA BIT 20
I0	2A2A0-S0	5- 51			
I1	2A2A0-S1	5- 51			DATA TO PF QUADRANT 3, BIT 06
I2	2A1A06J14D-10				
I3	2A1A06J14D-09				BIT 19 FROM INTERNAL STORAGE B
J0	2B2A1-K1	5- 71	2B2A1-AN		PARITY GENERATOR, GROUP 6 EVEN
J1	2B2A1-J0	5- 71	2B2A2-AM		PARITY GENERATOR, GROUP 7 EVEN
J2	2A1A06J12D-10				
J3	2A1A06J12D-09				BIT 19 FROM INTERNAL STORAGE A
K0	2B2A1-J1	5- 71	2B2A1-AM		PARITY GENERATOR, GROUP 6 ODD
K1	2B2A1-K0	5- 71	2B2A2-AN		PARITY GENERATOR, GROUP 7 ODD
K2	2A1A06J14D-08				
K3	2A1A06J14D-07				BIT 18 FROM INTERNAL STORAGE B
L0	2B2A5-A3	5- 73	2B2A5-RB		PARITY GEN,, CHARACTER 0 EVEN
L2	2A1A06J12D-07				BIT 18 FROM INTERNAL STORAGE A
L3	2A1A06J12D-08				
M0	2A2A1-R1	5- 45			DATA TO PF QUADRANT 2, BIT 07
M1	2A2A1-R0	5- 45			
M2	2B1B3-J0	6- 31			
M3	2B1B3-J1	6- 31			NOT BC READ BIT 19
N0	2A2A0-R0	5- 51			
N1	2A2A0-R1	5- 51			DATA TO PF QUADRANT 3, BIT 07
N2	2A1A06P04D-03				NOT MAIN CONTROL READ, BIT 19
	1A4A06J10D-03				
	1R0A1-E3	2- 33			
N3	2A1A06P04D-04				
	1A4A06J10D-04				
	1R0A1-E2	2- 33			
O0	2B1B3-L2	6- 31			
O1	2B1B3-L3	6- 31			NOT D4 BIT 19 TO MCS VIA F1
O2	2A1A06J09D-09				BIT 19 TO/FROM EXTERNAL STOR
	2A1A06J10D-09				
O3	2A1A06J09D-10				
	2A1A06J10D-10				
P0	2A1A06P04F-01				DO REGISTER BIT 19
	1A4A06J10F-01				
	1R0A1-01	2- 33			
P1	2A1A06P04F-02				
	1A4A06J10F-02				
	1R0A1-00	2- 33			
P2	2A1A06J13D-09				BIT 19 TO INTERNAL STORAGE B
P3	2A1A06J13D-10				
Q0	2B1B2-L3	6- 33			NOT D4 BIT 20 TO MCS VIA F1
Q1	2B1B2-L2	6- 33			
Q2	2A1A06J14E-02				
Q3	2A1A06J14E-01				BIT 20 FROM INTERNAL STORAGE B
R2	2A1A06J12E-02				
R3	2A1A06J12E-01				BIT 20 FROM INTERNAL STORAGE A
S0	2B2A2-H1	5- 69	2B2A2-AL		NOT MAIN CONTROL DATA BIT 20
S2	2A1A06J11D-10				
S3	2A1A06J11D-09				BIT 19 TO INTERNAL STORAGE A
T0	2A2A1-Q0	5- 45			
T1	2A2A1-Q1	5- 45			DATA TO PF QUADRANT 2, BIT 08
T2	2B1B2-J0	6- 33			
T3	2B1B2-J1	6- 33			NOT BC READ BIT 20
U0	2A1A06J11E-02				
U1	2A1A06J11E-01				BIT 20 TO INTERNAL STORAGE A
U2	2B2A1-V2	5- 71	2B2A1-AY		PARITY CHECK, GROUP 6 ODD
U3	2B2A1-U2	5- 71	2B2A2-AZ		PARITY CHECK, GROUP 7 ODD
V0	2A1A06J13E-01				BIT 20 TO INTERNAL STORAGE B
V1	2A1A06J13E-02				
V2	2B2A1-V3	5- 71	2B2A2-AY		PARITY CHECK, GROUP 7 EVEN
V3	2B2A1-U3	5- 71	2B2A1-AZ		PARITY CHECK, GROUP 6 EVEN
W0	2A2A0-Q1	5- 51			DATA TO PF QUADRANT 3, BIT 08
W1	2A2A0-Q0	5- 51			
W2	2A1A06P04D-05				NOT MAIN CONTROL READ, BIT 20
	1A4A06J10D-05				
	1R0A1-V2	2- 33			
W3	2A1A06P04D-06				
	1A4A06J10D-06				
	1R0A1-V3	2- 33			
X0	2A1A06P04F-03				DO REGISTER BIT 20
	1A4A06J10F-03				
	1R0A1-X1	2- 33			
X1	2A1A06P04F-04				
	1A4A06J10F-04				
	1R0A1-X0	2- 33			
X2	2A1A06J09E-01				BIT 20 TO/FROM EXTERNAL STOR
	2A1A06J10E-01				
X3	2A1A06J09E-02				
	2A1A06J10E-02				



CONTROL DATA	DATA BUS BITS 18-20 AND DATA PARITY GENERATOR/CHECKER	PRODUCT	
DEVELOPMENT DIVISION	LOC: 2B2A2 PART NO. 184668 SER.006	SIZE C	DRAWING NO. 60181000 REV. A
		SHEET	PAGE 5-69

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A3	2B2A5-I2	5- 73	2B2A5-BR	PARITY CHECK, CHARACTER 0 ODD
B2	2B1A4-J0	6- 35		
B3	2B1A4-J1	6- 35		NOT BC READ BIT 21
C0	2B2A5-01	5- 73	2B2A1-A0	DATA TRANSMITTERS ON
C2	2A1A06J13E-03			BIT 21 TO INTERNAL STORAGE B
C3	2A1A06J13E-04			
D0	2B1A4-L2	6- 35		
D1	2B1A4-L3	6- 35		NOT D4 BIT 21 TO MCS VIA FI
D2	2A1A06J11E-04			
D3	2A1A06J11E-03			BIT 21 TO INTERNAL STORAGE A
E0	2A1A06P04F-05			DO REGISTER BIT 21
	1A4A06J10F-05			
	1B0A0-F0	2- 35		
E1	2A1A06P04F-06			
	1A4A06J10F-06			

		1B0A0=F1	2= 35		
E2	2A1A06P04D=07				NOT MAIN CONTROL READ, BIT 21
	1A4A06J10D=07				
		1B0A0=Q0	2= 35		
E3	2A1A06P04D=08				
	1A4A06J10D=08				
		1B0A0=Q1	2= 35		
F0		2B2A5=X2	5= 73		LINK MN CONT/BC DB REG THRU DB
F1		2B2A5=T2	5= 73		BLOCK CONTROL DATA XMIT ENABLE
F2	2A1A06J09E=03				BIT 21 TO/FROM EXTERNAL STOR
	2A1A06J10E=03				
F3	2A1A06J09E=04				
	2A1A06J10E=04				
G0		2A2A1=P1	5= 45		DATA TO PF QUADRANT 2, BIT 09
G1		2A2A1=P0	5= 45		
H0		2B2B8=B1	5= 77	2B2B8-RR	MAIN CONTROL DATA BITS 09=11=4
H1		2B2A1=S1	5= 71	2B2A1-AL	MAIN CONTROL DATA BIT 23
I0		2A2A0=P0	5= 51		DATA TO PF QUADRANT 3, BIT 09
I1		2A2A0=P1	5= 51		
I2	2A1A06J14E=06				BIT 22 FROM INTERNAL STORAGE B
I3	2A1A06J14E=05				
J0		2B2A2=J1	5= 69	2B2A2-AM	PARITY GENERATOR, GROUP 7 EVEN
J1		2B2A2=K0	5= 69	2B2A1-AM	PARITY GENERATOR, GROUP 6 ODD
J2	2A1A06J12E=06				BIT 22 FROM INTERNAL STORAGE A
J3	2A1A06J12E=05				
K0		2B2A2=K1	5= 69	2B2A2-AN	PARITY GENERATOR, GROUP 7 ODD
K1		2B2A2=J0	5= 69	2B2A1-AN	PARITY GENERATOR, GROUP 6 EVEN
K2	2A1A06J14E=04				
K3	2A1A06J14E=03				BIT 21 FROM INTERNAL STORAGE B
L2	2A1A06J12E=03				BIT 21 FROM INTERNAL STORAGE A
L3	2A1A06J12E=04				
M0		2A2A1=N1	5= 45		DATA TO PF QUADRANT 2, BIT 10
M1		2A2A1=N0	5= 45		
M2		2B1A3=J0	6= 37		
M3		2B1A3=J1	6= 37		NOT BC READ BIT 22
N0		2A2A0=N0	5= 51		
N1		2A2A0=N1	5= 51		DATA TO PF QUADRANT 3, BIT 10
N2	2A1A06P04D=09				NOT MAIN CONTROL READ, BIT 22
	1A4A06J10D=09				
		1B0A0=E3	2= 35		
N3	2A1A06P04D=10				
	1A4A06J10D=10				
		1B0A0=E2	2= 35		
O0		2B1A3=L2	6= 37		
O1		2B1A3=L3	6= 37		NOT D4 BIT 22 TO MCS VIA F1
O2	2A1A06J09E=05				BIT 22 TO/FROM EXTERNAL STOR
	2A1A06J10E=05				
O3	2A1A06J09E=06				
	2A1A06J10E=06				
P0	2A1A06P04F=07				DO REGISTER BIT 22
	1A4A06J10F=07				
		1B0A0=01	2= 35		
P1	2A1A06P04F=08				
	1A4A06J10F=08				
		1B0A0=00	2= 35		
P2	2A1A06J13E=05				BIT 22 TO INTERNAL STORAGE B
P3	2A1A06J13E=06				
Q0		2B1A2=L3	6= 39		NOT D4 BIT 23 TO MCS VIA F1
Q1		2B1A2=L2	6= 39		
Q2	2A1A06J14E=08				BIT 23 FROM INTERNAL STORAGE B
Q3	2A1A06J14E=07				
R2	2A1A06J12E=08				BIT 23 FROM INTERNAL STORAGE A
R3	2A1A06J12E=07				
S1		2B2A1=H1	5= 71	2B2A1-AL	MAIN CONTROL DATA BIT 23
S2	2A1A06J11E=06				
S3	2A1A06J11E=05				BIT 22 TO INTERNAL STORAGE A
T0		2A2A1=O0	5= 45		
T1		2A2A1=O1	5= 45		DATA TO PF QUADRANT 2, BIT 11
T2		2B1A2=J0	6= 39		
T3		2B1A2=J1	6= 39		NOT BC READ BIT 23
U0	2A1A06J11E=08				
U1	2A1A06J11E=07				BIT 23 TO INTERNAL STORAGE A
U2		2B2A2=U3	5= 69	2B2A2-AZ	PARITY CHECK, GROUP 7 ODD
U3		2B2A2=V3	5= 69	2B2A1-AZ	PARITY CHECK, GROUP 6 EVEN
V0	2A1A06J13E=07				BIT 23 TO INTERNAL STORAGE B
V1	2A1A06J13E=08				
V2		2B2A2=U2	5= 69	2B2A1-AY	PARITY CHECK, GROUP 6 ODD
V3		2B2A2=V2	5= 69	2B2A2-AY	PARITY CHECK, GROUP 7 EVEN
W0		2A2A0=O1	5= 51		DATA TO PF QUADRANT 3, BIT 11
W1		2A2A0=O0	5= 51		
W2	2A1A06P04E=01				NOT MAIN CONTROL READ, BIT 23
	1A4A06J10E=01				
		1B0A0=V2	2= 35		
W3	2A1A06P04E=02				
	1A4A06J10E=02				
		1B0A0=V3	2= 35		
X0	2A1A06P05F=05				DO REGISTER BIT 13
	1A4A06J14F=05				
		1B0A0=X1	2= 35		
X1	2A1A06P05F=06				
	1A4A06J14F=06				
		1B0A0=X0	2= 35		
X2	2A1A06J09E=07				BIT 23 TO/FROM EXTERNAL STOR
	2A1A06J10E=07				
X3	2A1A06J09E=08				
	2A1A06J10E=08				

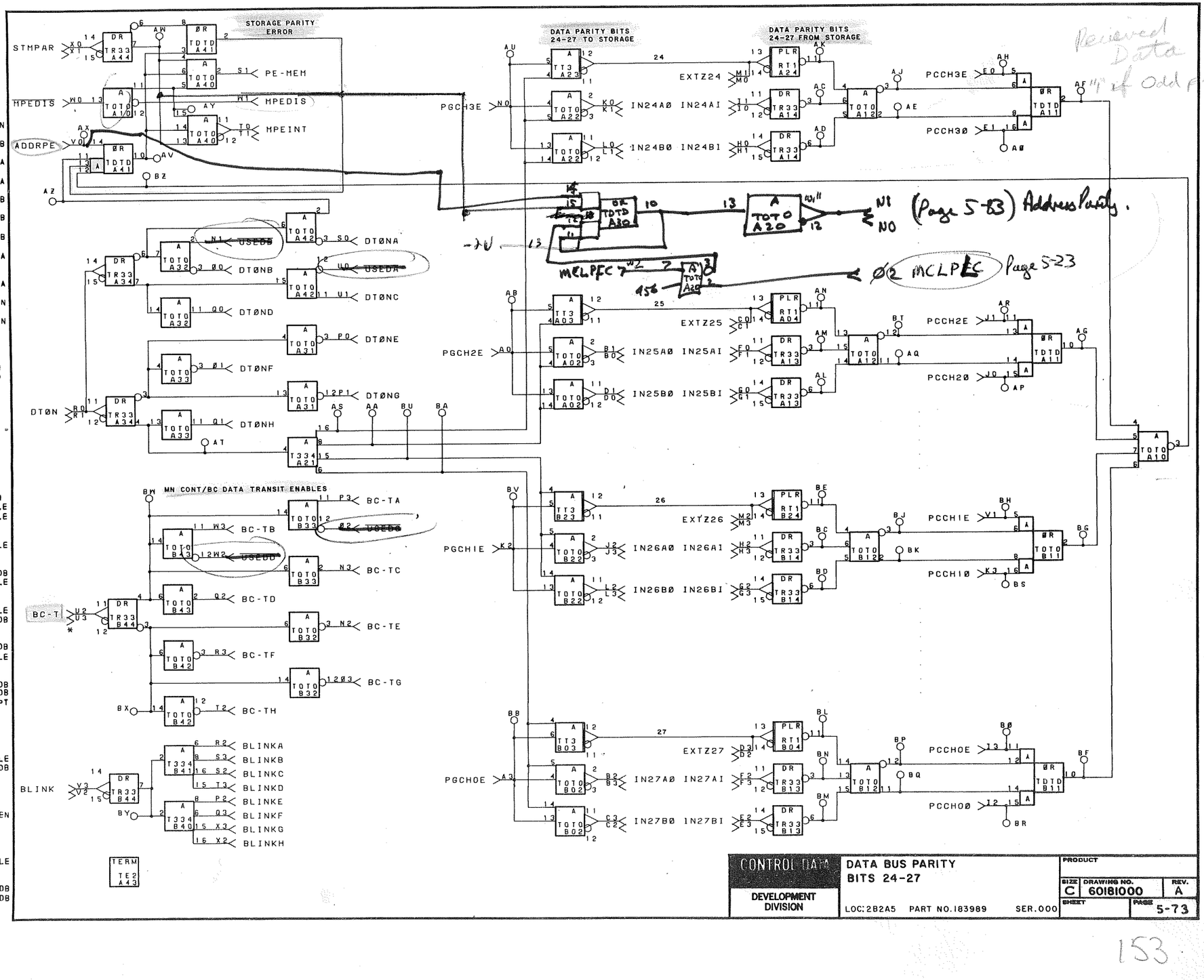


CONTROL DATA DEVELOPMENT DIVISION	DATA BUS BITS 21-23 AND DATA PARITY GENERATOR/CHECKER LOC: 2B2A1 PART NO. 184668 SER. 007	PRODUCT	
		SIZE C	DRAWING NO. 60181000
		REV. A	
		SHEET	PAGE 5-71

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B2A7-L0	5- 61	2B2A5-AB	PARITY GEN., CHARACTER 2 EVEN
A3	2B2A2-L0	5- 69	2B2A5-BB	PARITY GEN., CHARACTER 0 EVEN
B0	2A1A06J11F-02			
B1	2A1A06J11F-01			BIT 25 TO INTERNAL STORAGE A
B2	2A1A06J11F-05			BIT 27 TO INTERNAL STORAGE A
B3	2A1A06J11F-06			

C0	2A1A06J09F-01				BIT 25 TO/FROM EXTERNAL STOR
	2A1A06J10F-01				
C1	2A1A06J09F-02				
	2A1A06J10F-02				
C2	2A1A06J13F-06				BIT 27 TO INTERNAL STORAGE B
C3	2A1A06J13F-05				
D0	2A1A06J13F-02				BIT 25 TO INTERNAL STORAGE B
D1	2A1A06J13F-01				
D2	2A1A06J09F-06				
	2A1A06J10F-06				BIT 27 TO/FROM EXTERNAL STOR
D3	2A1A06J09F-05				
	2A1A06J10F-05				
E0	2B2A9-A3	5-57	2B2A5-AH		PARITY CHECK, CHARACTER 3 EVEN
E1	2B2A8-A3	5-59	2B2A5-AQ		PARITY CHECK, CHARACTER 3 ODD
E2	2A1A06J14F-05				BIT 27 FROM INTERNAL STORAGE B
E3	2A1A06J14F-06				
F0	2A1A06J12F-01				BIT 25 FROM INTERNAL STORAGE A
F1	2A1A06J12F-02				
F2	2A1A06J12F-05				BIT 27 FROM INTERNAL STORAGE A
F3	2A1A06J12F-06				
G0	2A1A06J14F-01				BIT 25 FROM INTERNAL STORAGE B
G1	2A1A06J14F-02				
G2	2A1A06J14F-03				BIT 26 FROM INTERNAL STORAGE B
G3	2A1A06J14F-04				
H0	2A1A06J14E-09				BIT 24 FROM INTERNAL STORAGE B
H1	2A1A06J14E-10				
H2	2A1A06J12F-03				BIT 26 FROM INTERNAL STORAGE A
H3	2A1A06J12F-04				
I0	2A1A06J12E-10				
I1	2A1A06J12E-09				BIT 24 FROM INTERNAL STORAGE A
I2	2B2A1-A3	5-71	2B2A5-RR		PARITY CHECK, CHARACTER 0 ODD
I3	2B2A2-A3	5-69	2B2A5-RQ		PARITY CHECK, CHARACTER 0 EVEN
J0	2B2A6-A3	5-63	2B2A5-AP		PARITY CHECK, CHARACTER 2 ODD
J1	2B2A7-A3	5-61	2B2A5-AR		PARITY CHECK, CHARACTER 2 EVEN
J2	2A1A06J11F-03				BIT 26 TO INTERNAL STORAGE A
J3	2A1A06J11F-04				
K0	2A1A06J11E-09				BIT 24 TO INTERNAL STORAGE A
K1	2A1A06J11E-10				
K2	2B2A4-L0	5-65	2B2A5-RV		PARITY GEN,, CHARACTER 1 EVEN
K3	2B2A3-A3	5-67	2B2A5-RS		PARITY CHECK, CHARACTER 1 ODD
L0	2A1A06J13E-09				BIT 24 TO INTERNAL STORAGE B
L1	2A1A06J13E-10				
L2	2A1A06J13F-03				BIT 26 TO INTERNAL STORAGE B
L3	2A1A06J13F-04				
M0	2A1A06J09E-10				
	2A1A06J10E-10				
M1	2A1A06J09E-09				BIT 24 TO/FROM EXTERNAL STOR
	2A1A06J10E-09				
M2	2A1A06J09F-03				BIT 26 TO/FROM EXTERNAL STOR
	2A1A06J10F-03				
M3	2A1A06J09F-04				
	2A1A06J10F-04				
N0	2B2A9-L0	5-57	2B2A5-AU		PARITY GEN,, CHARACTER 3 EVEN
N2	2B2A4-F1	5-65			BLOCK CONTROL DATA XMIT ENABLE
N3	2B2A7-F1	5-61			BLOCK CONTROL DATA XMIT ENABLE
O0	2B2A8-C0	5-59	2B2A8-AO		DATA TRANSMITTERS ON
O1	2B2A3-C0	5-67	2B2A3-AO		DATA TRANSMITTERS ON
O3	2B2A2-F1	5-69			BLOCK CONTROL DATA XMIT ENABLE
P0	2B2A4-C0	5-65	2B2A4-AO		DATA TRANSMITTERS ON
P1	2B2A2-C0	5-69	2B2A2-AO		DATA TRANSMITTERS ON
P2	2B2A4-F0	5-65			LINK MN CONT/BC DB REG THRU DB
P3	2B2A9-F1	5-57			BLOCK CONTROL DATA XMIT ENABLE
Q0	2B2A6-C0	5-63	2B2A6-AO		DATA TRANSMITTERS ON
Q1	2B2A1-C0	5-71	2B2A1-AO		DATA TRANSMITTERS ON
Q2	2B2A6-F1	5-63			BLOCK CONTROL DATA XMIT ENABLE
Q3	2B2A3-F0	5-67			LINK MN CONT/BC DB REG THRU DB
R0	2A2A7-N1	5-5			DATA TRANSMITTERS ON
R1	2A2A7-N0	5-5			
R2	2B2A9-F0	5-57			LINK MN CONT/BC DB REG THRU DB
R3	2B2A3-F1	5-67			BLOCK CONTROL DATA XMIT ENABLE
S0	2B2A9-C0	5-57	2B2A9-AO		DATA TRANSMITTERS ON
S1	2B2B9-J1	5-75	2B2B9-AJ		PARITY ERROR TO/FROM STORAGE
S2	2B2A7-F0	5-61			LINK MN CONT/BC DB REG THRU DB
S3	2B2A8-F0	5-59			LINK MN CONT/BC DB REG THRU DB
T0	2A1A06P03A-05				STORAGE PARITY ERROR INTERRUPT
	1A4A06J20A-05				
	1C0B3-W0	2-49			
T1	2A1A06P03A-06				
	1A4A06J20A-06				
	1C0B3-W1	2-49			
T2	2B2A1-F1	5-71			BLOCK CONTROL DATA XMIT ENABLE
T3	2B2A6-F0	5-63			LINK MN CONT/BC DB REG THRU DB
U1	2B2A7-C0	5-61	2B2A7-AO		DATA TRANSMITTERS ON
U2	2A2A7-D1	5-5			NOT BC DATA XMIT ENABLE
U3	2A2A7-D0	5-5			
V0	2B2B8-U1	5-77	2B2A5-AX		STORAGE ADDRESS PARITY ERROR
V1	2B2A4-A3	5-65	2B2A5-RH		PARITY CHECK, CHARACTER 1 EVEN
V2	2B1A6-F0	6-13			
V3	2B1A6-F1	6-13			LINK D0 AND D4 TO PAGE FILE
W0	2B2B9-L2	5-75			NOT STOR PAR; ERR, DISABLE
W1	2B2B9-L3	5-75			STOR PARITY ERROR DISABLE
W3	2B2A8-F1	5-59			BLOCK CONTROL DATA XMIT ENABLE
X0	2A2A7-V2	5-5			STRORE STORAGE PARITY CHECK
X1	2A2A7-V3	5-5			
X2	2B2A1-F0	5-71			LINK MN CONT/BC DB REG THRU DB
X3	2B2A2-F0	5-69			LINK MN CONT/BC DB REG THRU DB
	PAGE	5-73			

W2 2A2A7-H3 Page 5-5 MCLPFC



Received Data "1" of odd parity

153

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B2B9-S0	5- 75		STORAGE ADDRESS REPLY TIME
B0	2B2B8-S0	5- 77		STORAGE ADDRESS REPLY TIME
B1	2B2A6-H0	5- 63	2B2B9-RR	MAIN CONTROL DATA BITS 09-11=4
B2	2A1A06J03D-07			PART, WR, BIT 0 TO INT STOR A
B3	2A1A06J03D-08			
C0	2A1A06P05D-06			
	1A4A06J14D-06			
	1B0B5-E1	2- 5		
C1	2A1A06P05D-05			OPERAND REFERENCE
	1A4A06J14D-05			
	1B0B5-E0	2- 5		
C2	2A1A06J05D-07			PART, WR, BIT 0 TO INT STOR B
C3	2A1A06J05D-08			
D0	2A2A6-J1	5- 1		BLOCK CONTROL PRIORITY
D1	2A2A6-J0	5- 1		
D2	2A1A06J05D-10			
D3	2A1A06J05D-09			PART, WR, BIT 1 TO INT STOR B
E0	2A1A4-D0	6- 59		BC IDENT, TO PF - MOS PE CODE
E1	2A1A4-D1	6- 59		
E2	2A1A06J03D-10			
E3	2A1A06J03D-09			PART, WR, BIT 1 TO INT STOR A
F0	2A1A06P03C-10			
	1A4A06J20C-10			
	1C0A1-N3	2- 43		
F1	2A1A06P03C-09			NOT READ ADDRESS CYCLE
	1A4A06J20C-09			
	1C0A1-N2	2- 43		
F2	2A1A06J07D-10			
	2A1A06J08D-10			
F3	2A1A06J07D-09			PART, WR BIT 1 TO EXT STORAGE
	2A1A06J08D-09			
G0	2A2A7-S0	5- 5		NOT STOR ADDR REPLY TIME
G1	2A2A7-S1	5- 5		
G2	2A1A06J07D-08			
	2A1A06J08D-08			
G3	2A1A06J07D-07			PART, WR BIT 0 TO EXT STORAGE
	2A1A06J08D-07			
H0	2B2B8-T1	5- 77		MAIN CONTROL PRIORITY
H1	2B2A9-H0	5- 57	2B2B9-RU	MAIN CONTROL DATA BITS 00-02=0
H2	2A1B4-I2	6- 57		
H3	2A1B4-I3	6- 57		BC PARTIAL WRITE BIT 01 TO PF
I0	2A1A06P08D-03			INTERRUPT CODE BIT 1
	1A4A06J08D-03			
	1A0A2-H3	2- 61		
I1	2A1A06P08D-04			
	1A4A06J08D-04			
	1A0A2-H2	2- 61		

Partial write Bits

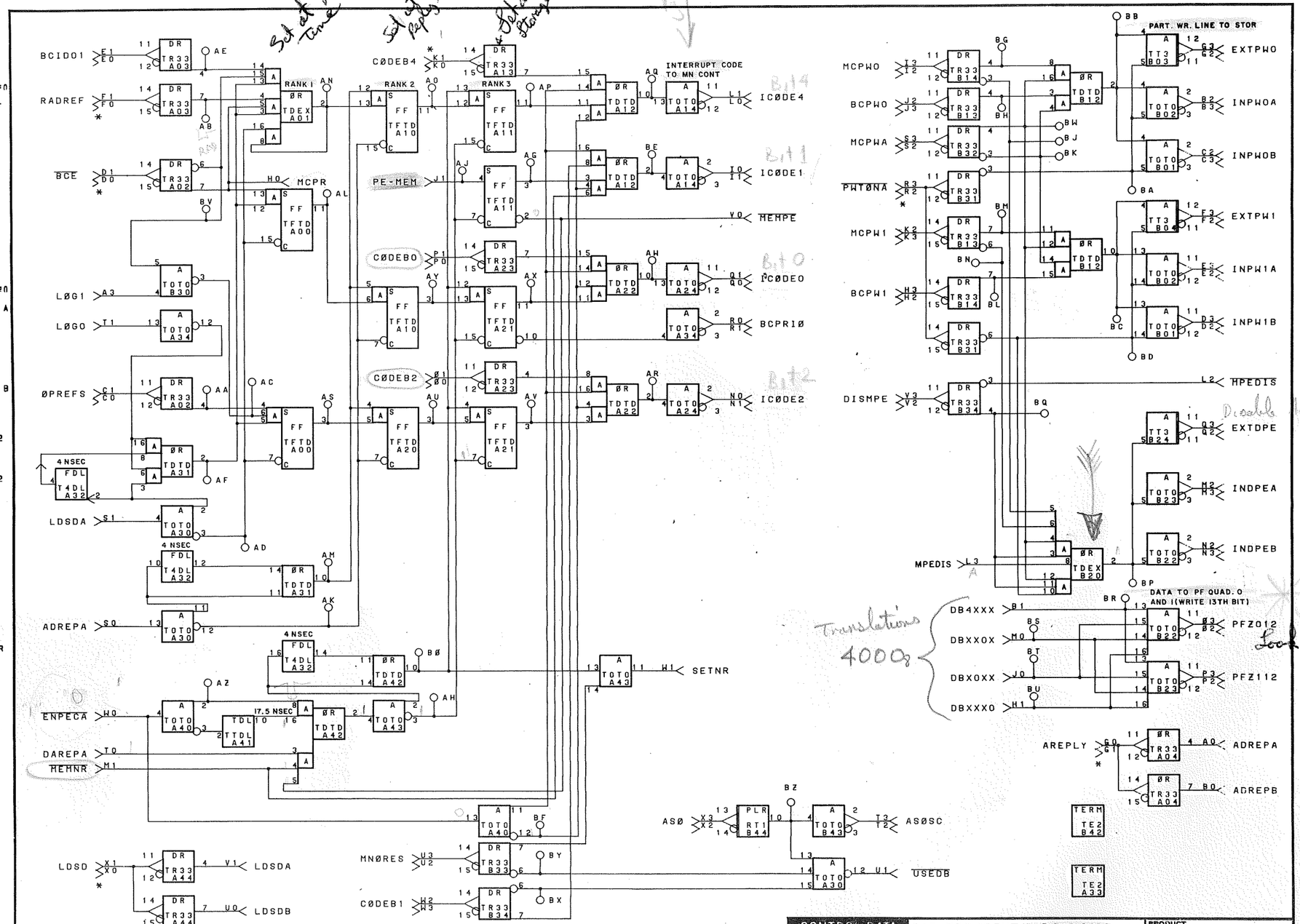
PWB

0	1	2	3	4
X	X	X	X	
	X	X	X	X
		X	X	X
			X	
				X

Full word
17 bits
15 bit
Character
Dest
(Destructive Read "A")

Block control only uses this

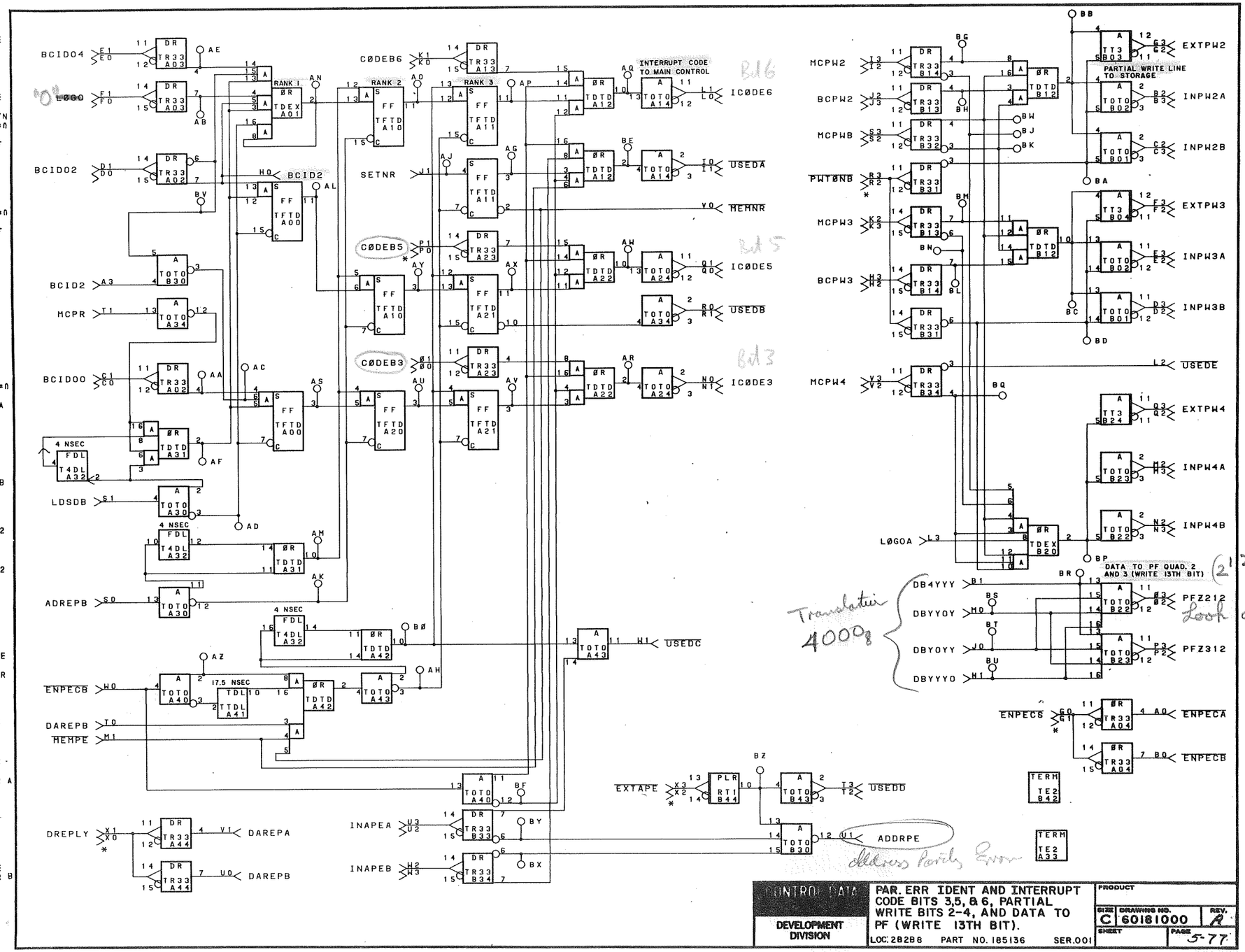
I2	2A1A06P03B-10			
	1A4A06J20B-10			
	1C0A0-U3	2- 37		
I3	2A1A06P03B-09			MC PARTIAL WRITE BIT 0
	1A4A06J20B-09			
	1C0A0-U2	2- 37		
J0	2B2A7-H0	5- 61	2B2B9-RT	MAIN CONTROL DATA BITS 06-08=0
J1	2B2A5-S1	5- 73	2B2B9-AJ	PARITY ERROR TO/FROM STORAGE
J2	2A1B4-H2	6- 57		MC PARTIAL WRITE BIT 00 TO PF
J3	2A1B4-H3	6- 57		
K0	2B0B8-V0	6-111		
K1	2B0B8-V1	6-111		NOT NORMAL INT CODE BIT 04
K2	2A1A06P03C-01			MC PARTIAL WRITE BIT 1
	1A4A06J20C-01			
	1C0A0-R2	2- 37		
K3	2A1A06P03C-02			
	1A4A06J20C-02			
	1C0A0-R3	2- 37		
L0	2A1A06P08D-10			
	1A4A06J08D-10			
	1A0A9-G0	2- 75		
L1	2A1A06P08D-09			INTERRUPT CODE BIT 4
	1A4A06J08D-09			
	1A0A9-G1	2- 75		
L2	2B2A5-W0	5- 73		NOT STOR PAR, ERR, DISABLE
L3	2B2A5-W1	5- 73		STOR PARITY ERROR DISABLE
M0	2B2A8-H0	5- 59	2B2B9-RS	MAIN CONTROL DATA BITS 03-05=0
M1	2B2B8-V0	5- 77		NOT STORAGE NO RESPONSE
M2	2A1A06J12F-07			DISABLE ADR PAR CHK, INT STOR A
M3	2A1A06J12F-08			
N0	2A1A06P08D-05			INTERRUPT CODE BIT 2
	1A4A06J08D-05			
	1A0A0-N3	2- 63		
N1	2A1A06P08D-06			
	1A4A06J08D-06			
	1A0A0-N2	2- 63		
N2	2A1A06J14F-07			DISABLE ADR PAR CHK, INT STOR B
N3	2A1A06J14F-08			
O0	2B0A8-Q0	6-109		NORMAL INTERRUPT CODE BIT 02
O1	2B0A8-Q1	6-109		
O2	2A2A3-H0	5- 31		DATA TO PF QUADRANT 0, BIT 12
O3	2A2A3-H1	5- 31		
P0	2B0A8-X1	6-109		NORMAL INTERRUPT CODE BIT 00
P1	2B0A8-X0	6-109		
P2	2A2A2-H0	5- 37		DATA TO PF QUADRANT 1, BIT 12
P3	2A2A2-H1	5- 37		
Q0	2A1A06P08D-02			
	1A4A06J08D-02			
	1A0A2-N2	2- 61		INTERRUPT CODE BIT 0
Q1	2A1A06P08D-01			
	1A4A06J08D-01			
	1A0A2-N3	2- 61		
Q2	2A1A06J09F-08			
	2A1A06J10F-08			
Q3	2A1A06J09F-07			DISABLE ADR PAR CHK, EXT STOR
	2A1A06J10F-07			
R0	2A1A06P03A-03			BLOCK CONTROL PRIORITY
	1A4A06J20A-03			
	1C0A1-N1	2- 43		
R1	2A1A06P03A-04			
	1A4A06J20A-04			
	1C0A1-N0	2- 43		
R2	2A2A7-U0	5- 5		EN PARTIAL WRITE BITS TO STOR
R3	2A2A7-U1	5- 5		
S0	2B2B9-A0	5- 75		STORAGE ADDRESS REPLY TIME
S1	2B2B9-V1	5- 75		LOAD S REGISTER TIME
S2	2A2A7-S3	5- 5		
S3	2A2A7-S2	5- 5		SELECT MAIN CONT PAR WR BITS
T0	2B2B8-V1	5- 77		STORAGE DATA REPLY TIME
T2	2A1A06P06C-02			
	1A4A06J16C-02			
	1C0B2-R1	2- 51		
T3	2A1A06P06C-01			AUTO-STEP OSCILLATOR
	1A4A06J16C-01			
	1C0B2-R0	2- 51		
U0	2B2B8-S1	5- 77		LOAD S REGISTER TIME
U2	2A2B9-M0	5- 23		STORAGE NO RESPONSE
U3	2A2B9-M1	5- 23		
V0	2B2B8-M1	5- 77		NOT STORAGE PARITY ERROR
V1	2B2B9-S1	5- 75		LOAD S REGISTER TIME
V2	2A1A06P03F-08			
	1A4A06J20F-08			
	1C0B3-S0	2- 49		
V3	2A1A06P03F-07			DISABLE MEMORY PARITY ERROR
	1A4A06J20F-07			
	1C0B3-S1	2- 49		
W0	2B2B8-A0	5- 77		NOT ENABLE PARITY ERROR CODE
W1	2B2B8-J1	5- 77	2B2B8-AJ	SET NO RESPONSE BIT IN CODE
W2	2B0A8-S0	6-109		NORMAL INTERRUPT CODE BIT 01
W3	2B0A8-S1	6-109		
X0	2A2A6-R0	5- 1		
X1	2A2A6-R1	5- 1		NOT LOAD S REG
X2	2A1A06J15C-06			
	2A1A06J16C-06			
X3	2A1A06J15C-05			UTO-STEP OSCILLATOR FROM
	2A1A06J16C-05			ONSOLE



CONTROL DATA	PAR. ERR IDENT AND INT CODE BITS 0, 1, 2, AND 4, PARTIAL WR BITS 0 AND 1, AND DATA TO PE (WRITE 13TH BIT)	PRODUCT	
DEVELOPMENT DIVISION	LOC:2B2B9 PART NO.185136 SER. 000	SIZE C / DRAWING NO. 60181000 / REV. A	SHEET / PAGE 5-75

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B2B9-W0	5- 75		NOT ENABLE PARITY ERROR CODE
A3	2B2B8-W0	5- 77		CODE BIT 2 FROM INT SCAN, XLTN
B0	2B2B8-W0	5- 77		NOT ENABLE PARITY ERROR CODE
B1	2B2A1-W0	5- 71	2B2B6-RR	MAIN CONTROL DATA BITS 09-11-14
B2	2A1A06J03E-01			PART, WR, BIT 2 TO INT STOR A
B3	2A1A06J03E-02			
C0	2A1A4-C0	6- 59		
C1	2A1A4-C1	6- 59		BC IDENT, TO PF + MCS PE CODE
C2	2A1A06J05E-01			PART, WR, BIT 2 TO INT STOR B
C3	2A1A06J05E-02			
D0	2A1A4-I0	6- 59		
D1	2A1A4-I1	6- 59		BC IDENT, TO PF + MCS PE CODE
D2	2A1A06J05E-04			
D3	2A1A06J05E-03			PART, WR, BIT 3 TO INT STOR B
E0	2A1A4-M0	6- 59		
E1	2A1A4-M1	6- 59		BC IDENT, TO PF + MCS PE CODE
E2	2A1A06J03E-04			
E3	2A1A06J03E-03			PART, WR, BIT 3 TO INT STOR A
F2	2A1A06J07E-04			

	2A1A06J08E=04			
F3	2A1A06J07E=03			PART, WR BIT 3 TO EXT STORAGE
	2A1A06J08F=03			
G0	2B1B7=E1	6=	3	ENABLE MCS PE CODE TO PF
G1	2B1B7=E0	6=	3	
G2	2A1A06J07E=02			
	2A1A06J08E=02			PART, WR BIT 2 TO EXT STORAGE
G3	2A1A06J07E=01			
	2A1A06J08E=01			
H0	2B2B8=A3	5=	77	CODE BIT 2 FROM INT SCAN, XLTN
H1	2B2A4=H0	5=	65	28288=BU MAIN CONTROL DATA BITS 00=02=0
H2	2A1B4=J2	6=	57	
H3	2A1B4=J3	6=	57	BC PARTIAL WRITE BIT 03 TO PF
I2	2A1A06P03C=04			
	1A4A06J20C=04			
	1C0A0=T2	2=	37	
I3	2A1A06P03C=03			MC PARTIAL WRITE BIT 2
	1A4A06J20C=03			
	1C0A0=T3	2=	37	
J0	2B2A2=H0	5=	69	28288=BT MAIN CONTROL DATA BITS 06=08=0
J1	2B2B9=W1	5=	75	28288=AJ SET NO RESPONSE BIT IN CODE
J2	2A1B4=G2	6=	57	BC PARTIAL WRITE BIT 02 TO PF
J3	2A1B4=G3	6=	57	
K0	2B0B8=U0	6=111		
K1	2B0B8=V1	6=111		NORMAL INTERRUPT CODE BIT 06
K2	2A1A06P03C=05			MC PARTIAL WRITE BIT 3
	1A4A06J20C=05			
	1C0A0=S2	2=	37	
K3	2A1A06P03C=06			
	1A4A06J20C=06			
	1C0A0=S3	2=	37	
L0	2A1A06P03B=08			
	1A4A06J20B=08			
	1C0A1=W1	2=	43	
L1	2A1A06P03B=07			INTERRUPT CODE BIT 6
	1A4A06J20B=07			
	1C0A1=W0	2=	43	
M0	2B2A3=H0	5=	67	28288=RS MAIN CONTROL DATA BITS 03=05=0
M1	2B2B9=V0	5=	75	NOT STORAGE PARITY ERROR
M2	2A1A06J03E=05			PART, WR, BIT 4 TO INT STOR A
M3	2A1A06J03E=06			
N0	2A1A06P08D=07			INTERRUPT CODE BIT 3
	1A4A06J08D=07			
	1A0A0=M3	2=	63	
N1	2A1A06P08D=08			
	1A4A06J08D=08			
	1A0A0=M2	2=	63	
N2	2A1A06J05E=05			PART, WR, BIT 4 TO INT STOR B
N3	2A1A06J05E=06			
O0	2B0B8=W3	6=111		NORMAL INTERRUPT CODE BIT 03
O1	2B0B8=W2	6=111		
O2	2A2A1=M0	5=		DATA TO PF QUADRANT 2, BIT 12
O3	2A2A1=M1	5=		
P0	2B0B8=P1	6=111		NOT NORMAL INT CODE BIT 05
P1	2B0B8=P0	6=111		
P2	2A2A0=M0	5=	49	DATA TO PF QUADRANT 3, BIT 12
P3	2A2A0=M1	5=	49	
Q0	2A1A06P08E=02			
	1A4A06J08E=02			
	1A0A7=G0	2=	77	INTERRUPT CODE BIT 5
Q1	2A1A06P08E=01			
	1A4A06J08E=01			
	1A0A7=G1	2=	77	
Q2	2A1A06J07E=06			
	2A1A06J08E=06			
Q3	2A1A06J07E=05			PART, WR BIT 4 TO EXT STORAGE
	2A1A06J08E=05			
R2	2A2A7=L1	5=	5	EN PARTIAL WRITE BITS TO STOR
R3	2A2A7=L0	5=	5	
S0	2B2B9=B0	5=	75	STORAGE ADDRESS REPLY TIME
S1	2B2B9=U0	5=	75	LOAD S REGISTER TIME
S2	2A2A7=U3	5=	5	
S3	2A2A7=U2	5=	5	SELECT MAIN CONT PAR WR BITS
T0	2B2B8=U0	5=	77	STORAGE DATA REPLY TIME
T1	2B2B9=H0	5=	75	MAIN CONTROL PRIORITY
U0	2B2B8=T0	5=	77	STORAGE DATA REPLY TIME
U1	2B2A5=V0	5=	73	2B2A5=AX STORAGE ADDRESS PARITY ERROR
U2	2A1A06J03F=02			
U3	2A1A06J03F=01			ADDR PAR, ERR, FROM INT STOR A
V0	2B2B9=M1	5=	75	NOT STORAGE NO RESPONSE
V1	2B2B9=T0	5=	75	STORAGE DATA REPLY TIME
V2	2A1A06P03C=08			
	1A4A06J20C=08			
	1C0A0=H2	2=	37	
V3	2A1A06P03C=07			MC PARTIAL WRITE BIT4 OR
	1A4A06J20C=07			DESTRUCTIVE LOAD
	1C0A0=H3	2=	37	
W0	2B2B8=B0	5=	77	NOT ENABLE PARITY ERROR CODE
W2	2A1A06J05F=01			ADDR PAR, ERR, FROM INT STOR B
W3	2A1A06J05F=02			
X0	2A2A7=X1	5=	5	
X1	2A2A7=X0	5=	5	NOT STORAGE DATA REPLY TIME
X2	2A1A06J07F=01			ADDR PAR, ERR FROM EXT STOR
	2A1A06J08F=01			
X3	2A1A06J07F=02			
	2A1A06J08F=02			



CONTROL DATA DEVELOPMENT DIVISION	PAR. ERR IDENT AND INTERRUPT CODE BITS 3,5, & 6, PARTIAL WRITE BITS 2-4, AND DATA TO PF (WRITE 13TH BIT). LOC: 28288 PART NO. 185136 SER.001	PRODUCT	
		SIZE C	DRAWING NO. 60181000 REV. A
		SHEET	PAGE 5-77

157

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A1A06J18A-01			A/Q/E REG DISPLAY BIT 00
A3	2A1A06J18B-05			A/Q/E REG DISPLAY BIT 14
B0	2A1A06J18A-03			A/Q/E REG DISPLAY BIT 02
B1	2A1A06J18A-02			A/Q/E REG DISPLAY BIT 01
B2	2A1A06J18B-06			A/Q/E REG DISPLAY BIT 15
B3	2A1A06J18B-07			A/Q/E REG DISPLAY BIT 16
C0	2A1A06J17A-06			
	1A4A06P02A-06			
	1A1R2-T3	3, 79		
C1	2A1A06J17A-05			NOT BIT 02 OF A1*Q1*E1*E2
	1A4A06P02A-05			
	1A1R2-T2	3, 79		
C2	2A1A06J17C-10			
	1A4A06P02C-10			
	1A1A2-T3	3, 85		
C3	2A1A06J17C-09			NOT BIT 14 OF A1*Q1*E1*E2
	1A4A06P02C-09			
	1A1A2-T2	3, 85		
D0	2A1A06J17A-04			
	1A4A06P02A-04			
	1A1B2-U1	3, 79		
D1	2A1A06J17A-03			NOT BIT 01 OF A1*Q1*E1*E2
	1A4A06P02A-03			
	1A1B2-U0	3, 79		
D2	2A1A06J17D-02			
	1A4A06P02D-02			
	1A1A2-U3	3, 85		
D3	2A1A06J17D-01			NOT BIT 15 OF A1*Q1*E1*E2
	1A4A06P02D-01			
	1A1A2-U2	3, 85		
E0	2A1A06J17A-01			NOT BIT 00 OF A1*Q1*E1*E2
	1A4A06P02A-01			
	1A1B2-T0	3, 79		
E1	2A1A06J17A-02			
	1A4A06P02A-02			
	1A1B2-T1	3, 79		
E2	2A1A06J17D-03			NOT BIT 16 OF A1*Q1*E1*E2
	1A4A06P02D-03			
	1A1A1-T0	3, 87		
E3	2A1A06J17D-04			
	1A4A06P02D-04			
	1A1A1-T1	3, 87		
F0	2A1A06J18A-05			A/Q/E REG DISPLAY BIT 04
F1	2A1A06J18A-04			A/Q/E REG DISPLAY BIT 03
F2	2A1A06J18B-08			A/Q/E REG DISPLAY BIT 17
F3	2A1A06J18B-09			A/Q/E REG DISPLAY BIT 18
G1	2A1A06J18A-06			A/Q/E REG DISPLAY BIT 05
G3	2A1A06J18B-10			A/Q/E REG DISPLAY BIT 19
H0	2A1A06J17B-02			
	1A4A06P02B-02			
	1A1B1-U1	3, 81		
H1	2A1A06J17B-01			NOT BIT 05 OF A1*Q1*E1*E2
	1A4A06P02B-01			
	1A1B1-U0	3, 81		
H2	2A1A06J17D-06			
	1A4A06P02D-06			
	1A1A1-U1	3, 87		
H3	2A1A06J17D-05			NOT BIT 17 OF A1*Q1*E1*E2
	1A4A06P02D-05			
	1A1A1-U0	3, 87		
I0	2A1A06J17A-10			
	1A4A06P02A-10			
	1A1B1-T1	3, 81		
I1	2A1A06J17A-09			NOT BIT 04 OF A1*Q1*E1*E2
	1A4A06P02A-09			
	1A1B1-T0	3, 81		
I2	2A1A06J17D-08			
	1A4A06P02D-08			
	1A1A1-T3	3, 87		
I3	2A1A06J17D-07			NOT BIT 18 OF A1*Q1*E1*E2
	1A4A06P02D-07			
	1A1A1-T2	3, 87		

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J0  2A1A06J17A-07                    NOT BIT 03 OF A1*Q1*B1*E2
    1A4A06P02A-07
        1A1B2-U2  3- 79
J1  2A1A06J17A-08
    1A4A06P02A-08
        1A1B2-U3  3- 79              NOT BIT 19 OF A1*Q1*B1*E2
J2  2A1A06J17D-09
    1A4A06P02D-09
        1A1A1-U2  3- 87
J3  2A1A06J17D-10
    1A4A06P02D-10
        1A1A1-U3  3- 87
K0  2A1A06J18A-08                    A/Q/E REG DISPLAY BIT 07
K1  2A1A06J18A-09                    A/Q/E REG DISPLAY BIT 08
K2  2A1A06J18C-01                    A/Q/E REG DISPLAY BIT 20
K3  2A1A06J18C-02                    A/Q/F REG DISPLAY BIT 21
L0  2A1A06J18A-07                    A/Q/F REG DISPLAY BIT 06
L3  2A1A06J18C-03                    A/Q/E REG DISPLAY BIT 22
M0  2A1A06J17B-08
    1A4A06P02B-08
        1A1B0-T1  3- 83
M1  2A1A06J17B-07                    NOT BIT 08 OF A1*Q1*B1*E2
    1A4A06P02B-07
        1A1B0-T0  3- 83
M2  2A1A06J17E-02
    1A4A06P02E-02
        1A1A0-T1  3- 89
M3  2A1A06J17E-01                    NOT BIT 20 OF A1*Q1*B1*E2
    1A4A06P02E-01
        1A1A0-T0  3- 89
N0  2A1A06J17B-06
    1A4A06P02B-06
        1A1B1-U3  3- 81
N1  2A1A06J17B-05                    NOT BIT 07 OF A1*Q1*B1*E2
    1A4A06P02B-05
        1A1B1-U2  3- 81
N2  2A1A06J17E-04
    1A4A06P02E-04
        1A1A0-U1  3- 89
N3  2A1A06J17E-03                    NOT BIT 21 OF A1*Q1*B1*E2
    1A4A06P02E-03
        1A1A0-U0  3- 89
O0  2A1A06J17B-03                    NOT BIT 06 OF A1*Q1*B1*E2
    1A4A06P02B-03
        1A1B1-T2  3- 81
O1  2A1A06J17B-04
    1A4A06P02B-04
        1A1B1-T3  3- 81              NOT BIT 22 OF A1*Q1*B1*E2
O2  2A1A06J17E-05
    1A4A06P02E-05
        1A1A0-T2  3- 89
O3  2A1A06J17E-06
    1A4A06P02E-06
        1A1A0-T3  3- 89
P0  2A1A06J18B-01                    A/Q/E REG DISPLAY BIT 10
P1  2A1A06J18B-02                    A/Q/F REG DISPLAY BIT 11
P2  2A1A06J18C-04                    A/Q/E REG DISPLAY BIT 23
Q0  2A1A06J18A-10                    A/Q/F REG DISPLAY BIT 09
R0  2A1A06J17C-04
    1A4A06P02C-04
        1A1B0-U3  3- 83
R1  2A1A06J17C-03                    NOT BIT 11 OF A1*Q1*B1*E2
    1A4A06P02C-03
        1A1B0-U2  3- 83
R2  2A1A06J17E-08
    1A4A06P02E-08
        1A1A0-U3  3- 89
R3  2A1A06J17E-07                    NOT BIT 23 OF A1*Q1*B1*E2
    1A4A06P02E-07
        1A1A0-U2  3- 89
S0  2A1A06J17C-02
    1A4A06P02C-02
        1A1B0-T3  3- 83
S1  2A1A06J17C-01                    NOT BIT 10 OF A1*Q1*B1*E2
    1A4A06P02C-01
        1A1B0-T2  3- 83
T0  2A1A06J17B-10
    1A4A06P02B-10
        1A1B0-U1  3- 83
T1  2A1A06J17B-09                    NOT BIT 09 OF A1*Q1*B1*E2
    1A4A06P02B-09
        1A1B0-U0  3- 83
U0  2A1A06J18B-03                    A/Q/E REG DISPLAY BIT 12
U1  2A1A06J18B-04                    A/Q/F REG DISPLAY BIT 13
W0  2A1A06J17C-08
    1A4A06P02C-08
        1A1A2-U1  3- 85
W1  2A1A06J17C-07                    NOT BIT 13 OF A1*Q1*B1*E2
    1A4A06P02C-07
        1A1A2-U0  3- 85
X0  2A1A06J17C-06
    1A4A06P02C-06
        1A1A2-T1  3- 85
X1  2A1A06J17C-05                    NOT BIT 12 OF A1*Q1*B1*E2
    1A4A06P02C-05
        1A1A2-T0  3- 85

                PAGE  5- 79
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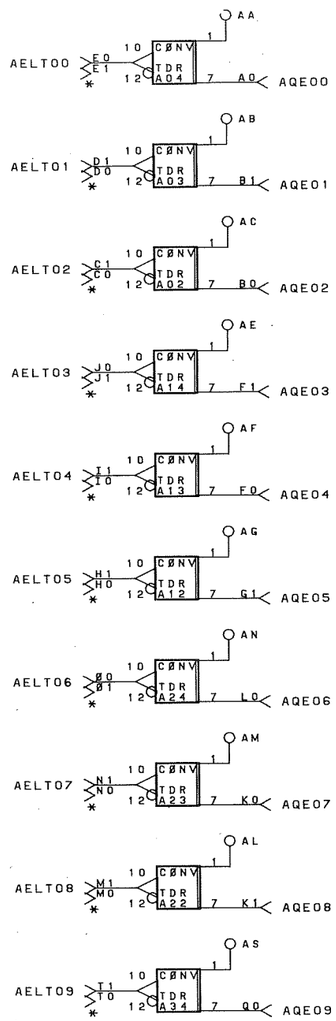

CONTROL DATA	TCS TO DTL CONVERSION FOR CONSOLE DISPLAYS PART I	PRODUCT
DEVELOPMENT DIVISION	LOC:2B2B7 PART NO.185392 SER:000	SIZE C · DRAWING NO. 60181000 · REV. A · SHEET · PAGE 5-79

159

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A1A06J18C-07			GATE FOR A/Q, B REG, DISPLAYS
A3	2A1A06J18E-01			ENTER AUTO PROGRAM DISPLAY
B0	2A1A06J18C-09			F GATE MIDDLE DISPLAY
B1	2A1A06J18C-08			F GATE LOWER DISPLAY
C0	2A1A06P09F-04			
	1A4A06J12F-04			
	1C0A2-J3	2- 53		
C1	2A1A06P09F-03			GATE C + F DIGIT 4
	1A4A06J12F-03			
	1C0A2-J2	2- 53		
C2	2A2A5-L0	5- 3		
C3	2A2A5-L1	5- 3		ENTER AUTO PROGRAM INDICATOR
D0	2A1A06P09F-02			
	1A4A06J12F-02			
	1C0A2-I3	2- 53		
D1	2A1A06P09F-01			GATE C + F DIGITS 0-3
	1A4A06J12F-01			
	1C0A2-I2	2- 53		
E0	2A1A06J21C-03			GATE A,Q,E REGISTER DISPLAY
	1A4A06P04C-03			
	1C0A2-L3	2- 53		
E1	2A1A06J21C-04			
	1A4A06P04C-04			
	1C0A2-L2	2- 53		
F1	2A1A06J18C-10			F GATE UPPER DISPLAY
G1	2A1A06J18D-02			GO INDICATOR - CONSOLE SWITCH
H0	2A1A06J21D-04			
	1A4A06P04D-04			
	1C0B3-J1	2- 49		
H1	2A1A06J21D-03			NOT (GO FF)
	1A4A06P04D-03			
	1C0B3-J0	2- 49		
J0	2A1A06P09F-05			GATE C + F DIGITS 5-7
	1A4A06J12F-05			
	1C0A2-C2	2- 53		
J1	2A1A06P09F-06			
	1A4A06J12F-06			
	1C0A2-C3	2- 53		
K0	2A1A06J18D-04			SWEEP/ENTER CONTINUOUS IND
K1	2A1A06J18D-05			STOP SWITCH INDICATOR
K3	2A1A06J18F-02			BACKGROUND LIGHT IN OSR
L0	2A1A06J18D-03			INDICATOR FOR DISPLAY C

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L3  2A1A06J18F=03                OSR BIT 0 TO CONSOLE DISPLAY

M0  2A1A06J21D=06
    1A4A06P04D=06
        1C0B3=L1   2= 49
M1  2A1A06J21D=05                STOP FF
    1A4A06P04D=05
        1C0B3=L0   2= 49
N0  2A1A06J21D=02
    1A4A06P04D=02
        1C0B1=F0   2= 47
N1  2A1A06J21D=01                SWEEP=ENTER CONTINUOUS FF SET
    1A4A06P04D=01
        1C0B1=F1   2= 47
N2  2A1A06P06C=10
    1A4A06J18C=10
        1C0A0=E0   2= 37
N3  2A1A06P06C=09                OSR BACKGROUND LIGHT
    1A4A06J18C=09
        1C0A0=E1   2= 37
O0  2A1A06J21E=01                CO DISPLAY INDICATOR
    1A4A06P04E=01
        1C0A2=G2   2= 53
O1  2A1A06J21E=02
    1A4A06P04E=02
        1C0A2=G3   2= 53
O2  2A1A06J21A=07                OSR ,BIT 0
    1A4A06P04A=07
        1C0A3=J0   2= 39
O3  2A1A06J21A=08
    1A4A06P04A=08
        1C0A3=J1   2= 39
P0  2A1A06J18D=07                AUTO LOAD SWITCH INDICATOR
P1  2A1A06J18D=08                TYPEWRITER FINISH INDICATOR
P2  2A1A06J18F=04                OSR BIT 1 TO CONSOLE DISPLAY

P3  2A1A06J18F=05                OSR BIT 2 TO CONSOLE DISPLAY

Q0  2A1A06J18D=06                TO AUTO - DUMP - SWITCH LAMP
Q3  2A1A06J18F=06                ISR BIT 0 TO CONSOLE DISPLAY

R0       2B1A0=M0  6=  5
R1       2B1A0=M1  6=  5         NOT TYPEWRITER FINISH LIGHT DR
R2  2A1A06J21A=10
    1A4A06P04A=10
        1C0A3=Q1   2= 39
R3  2A1A06J21A=09                OSR  BIT 1
    1A4A06P04A=09
        1C0A3=Q0   2= 39
S0  2A1A06J21B=10
    1A4A06P04B=10
        1C0B2=N1   2= 51
S1  2A1A06J21B=09                AUTO LOAD LIGHT
    1A4A06P04B=09
        1C0B2=N0   2= 51
S2  2A1A06J21B=02
    1A4A06P04B=02
        1C0A3=L1   2= 39
S3  2A1A06J21B=01                OSR ,BIT 2
    1A4A06P04B=01
        1C0A3=L0   2= 39
T0  2A1A06J21C=02
    1A4A06P04C=02
        1C0B2=L0   2= 51
T1  2A1A06J21C=01                AUTO DUMP LIGHT
    1A4A06P04C=01
        1C0B2=L1   2= 51
T2  2A1A06J21A=02
    1A4A06P04A=02
        1C0A3=O1   2= 39
T3  2A1A06J21A=01                ISR ,BIT 0
    1A4A06P04A=01
        1C0A3=O0   2= 39
U0  2A1A06J18D=09                TYPEWRITER REPEAT INDICATOR
U1  2A1A06J18D=10                DISABLE STOR PROTECT INDICATOR
U2  2A1A06J18F=08                SET SWITCH, ISR, BIT 2
                                 ISR BIT 1 TO CONSOLE DISPLAY
U3  2A1A06J18F=07                SET SWITCH, ISR, BIT 1

W0       2A2A5=K1  5=  3
W1       2A2A5=K0  5=  3         DISABLE STOR PROTECT INDICATOR
W2  2A1A06J21A=04
    1A4A06P04A=04
        1C0A3=N0   2= 39
W3  2A1A06J21A=03                ISR ,BIT 1
    1A4A06P04A=03
        1C0A3=N1   2= 39
X0       2B1A7=C0  6=  1
X1       2B1A7=C1  6=  1         NOT TW REPEAT LIGHT DRIVER
X2  2A1A06J21A=06
    1A4A06P04A=06
        1C0A3=P1   2= 39
X3  2A1A06J21A=05                ISR ,BIT 2
    1A4A06P04A=05
        1C0A3=P0   2= 39

          PAGE   5= 81
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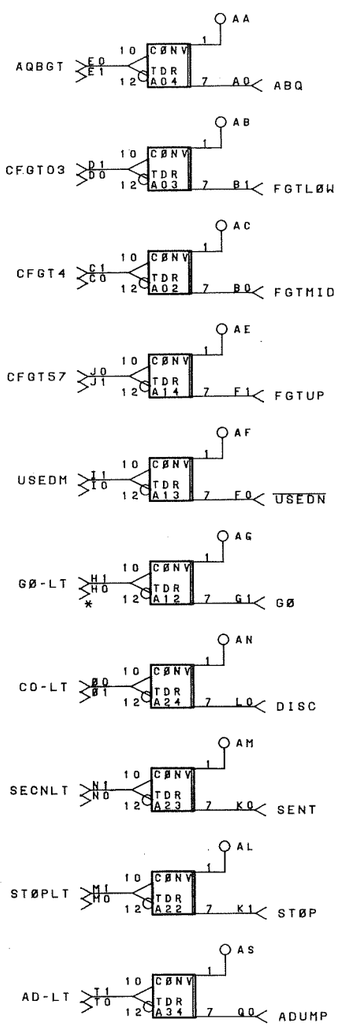

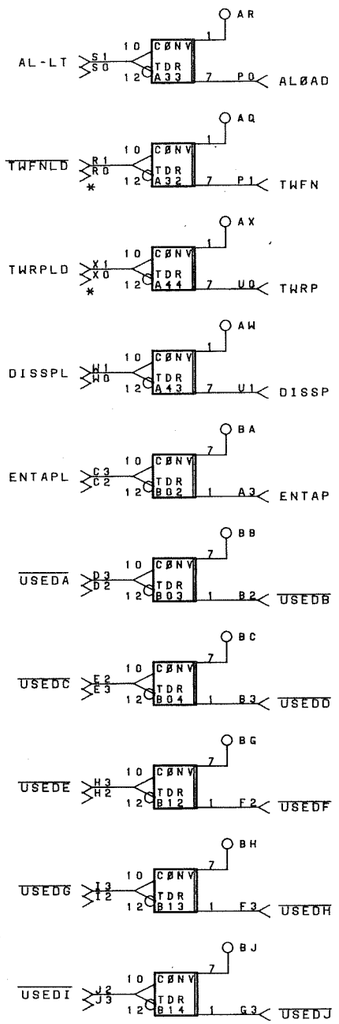

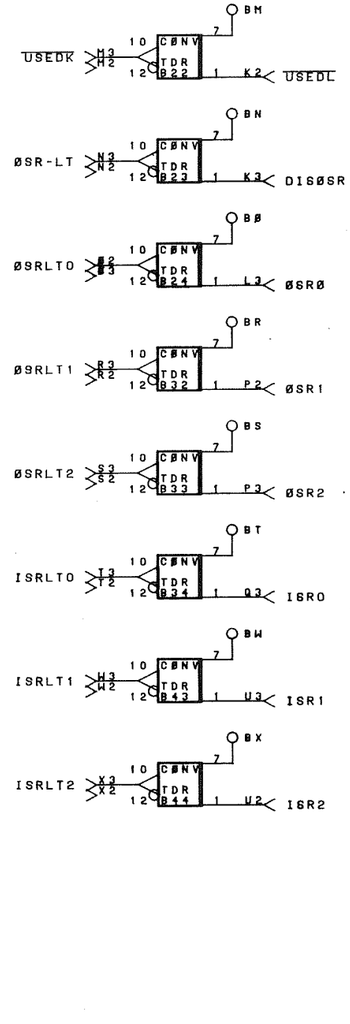

CONTROL DATA DEVELOPMENT DIVISION	TCS TO DTL CONVERSION FOR CONSOLE DISPLAYS PART 2 LOC: 2B2B6 PART NO. 185392 SER: 001	PRODUCT	
		SIZE C	DRAWING NO. 60181000
		REV. A	
		SHEET	PAGE 5-81

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A3	2A1A06J20B-03			P BIT 12 TO CSL DISPLAY
B0	2A1A06J20A-01			P BIT 00 TO CSL DISPLAY
B2	2A1A06J20B-04			P BIT 13 TO CSL DISPLAY
B3	2A1A06J20B-05			P BIT 14 TO CSL DISPLAY
C0	2A1A06J21B-04			
	1A4A06P04B-04			
	1C0A3-V3	2- 39		
C1	2A1A06J21B-03			B DISPLAY, BIT 0
	1A4A06P04B-03			
	1C0A3-V2	2- 39		
C2	2A1A06P07E-10			
	1A4A06J02E-10			
	1A0A1-T1	2- 83		
C3	2A1A06P07E-09			B8 BIT 12
	1A4A06J02E-09			
	1A0A1-T0	2- 83		
D2	2A1A06P07F-02			
	1A4A06J02F-02			
	1A0A1-L2	2- 83		
D3	2A1A06P07F-01			B8 BIT 13
	1A4A06J02F-01			
	1A0A1-L3	2- 83		
E2	2A1A06P07F-03			B8 BIT 14
	1A4A06J02F-03			
	1A0A1-S1	2- 83		
E3	2A1A06P07F-04			
	1A4A06J02F-04			
	1A0A1-S0	2- 83		
F0	2A1A06J20A-03			P BIT 02 TO CSL DISPLAY
F1	2A1A06J20A-02			P BIT 01 TO CSL DISPLAY
F2	2A1A06J20B-07			C/F BIT 00 TO CONSOLE DISPLAY
F3	2A1A06J20B-08			C/F BIT 01 TO CONSOLE DISPLAY
G1	2A1A06J20A-04			P BIT 03 TO CSL DISPLAY
G3	2A1A06J20B-09			C/F BIT 02 TO CONSOLE DISPLAY
H0	2A1A06P07D-02			
	1A4A06J02D-02			
	1A0A7-T1	2- 77		
H1	2A1A06P07D-01			B8 BIT 3
	1A4A06J02D-01			
	1A0A7-T0	2- 77		
H2	2A1A06P08A-02			
	1A4A06J08A-02			
	1A0B8-P0	2- 65		
H3	2A1A06P08A-01			C2 BIT 0
	1A4A06J08A-01			
	1A0B8-P1	2- 65		
I0	2A1A06J21B-08			
	1A4A06P04B-08			
	1C0A3-M2	2- 39		
I1	2A1A06J21B-07			B DISPLAY, BIT 2
	1A4A06P04B-07			
	1C0A3-M3	2- 39		
I2	2A1A06P08A-04			
	1A4A06J08A-04			
	1A0B8-T0	2- 65		
I3	2A1A06P08A-03			C2 BIT 1
	1A4A06J08A-03			
	1A0B8-T1	2- 65		
J0	2A1A06J21B-05			B DISPLAY, BIT 1
	1A4A06P04B-05			
	1C0A3-P3	2- 39		
J1	2A1A06J21B-06			
	1A4A06P04B-06			
	1C0A3-P2	2- 39		
J2	2A1A06P08A-05			C2 BIT 2
	1A4A06J08A-05			
	1A0B8-Q1	2- 65		
J3	2A1A06P08A-06			
	1A4A06J08A-06			
	1A0B8-Q0	2- 65		
K0	2A1A06J20A-06			P BIT 05 TO CSL DISPLAY
K1	2A1A06J20A-07			P BIT 06 TO CSL DISPLAY
K2	2A1A06J20B-10			BACKGROUND DIGIT 0 C DISPLAY
K3	2A1A06J20C-01			C/F BIT 03 TO CONSOLE DISPLAY
L0	2A1A06J20A-05			P BIT 04 TO CSL DISPLAY
L3	2A1A06J20C-02			C/F BIT 04 TO CONSOLE DISPLAY
M0	2A1A06P07D-08			
	1A4A06J02D-08			
	1A0A5-T1	2- 79		
M1	2A1A06P07D-07			B8 BIT 6
	1A4A06J02D-07			
	1A0A5-T0	2- 79		
M2	2A1A06J21E-06			
	1A4A06P04E-06			
	1C0A2-V0	2- 53		
M3	2A1A06J21E-05			BOUNCING BALL, OCTAL DIGIT 0

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      1A4A06P04E-05
          1C0A2-V1   2- 53
N0    2A1A06P07D-06
      1A4A06J02D-06
          1A0A7-S0   2- 77
N1    2A1A06P07D-05
      1A4A06J02D-05
          1A0A7-S1   2- 77
N2    2A1A06P08A-08
      1A4A06J08A-08
          1A0B6-P0   2- 67
N3    2A1A06P08A-07
      1A4A06J08A-07
          1A0B6-P1   2- 67
O0    2A1A06P07D-03
      1A4A06J02D-03
          1A0A7-L3   2- 77
O1    2A1A06P07D-04
      1A4A06J02D-04
          1A0A7-L2   2- 77
O2    2A1A06P08A-09
      1A4A06J08A-09
          1A0B6-T1   2- 67
O3    2A1A06P08A-10
      1A4A06J08A-10
          1A0B6-T0   2- 67
P0    2A1A06J20A-09
P1    2A1A06J20A-10
P2    2A1A06J20C-03
P3    2A1A06J20C-04
Q0    2A1A06J20A-08
Q3    2A1A06J20C-05
R0    2A1A06P07E-04
      1A4A06J02E-04
          1A0A3-T1   2- 81
R1    2A1A06P07E-03
      1A4A06J02E-03
          1A0A3-T0   2- 81
R2    2A1A06P08B-02
      1A4A06J08B-02
          1A0B6-Q0   2- 67
R3    2A1A06P08B-01
      1A4A06J08B-01
          1A0B6-Q1   2- 67
S0    2A1A06P07E-02
      1A4A06J02E-02
          1A0A5-S0   2- 79
S1    2A1A06P07E-01
      1A4A06J02E-01
          1A0A5-S1   2- 79
S2    2A1A06J21E-08
      1A4A06P04E-08
          1C0A2-W1   2- 53
S3    2A1A06J21E-07
      1A4A06P04E-07
          1C0A2-W0   2- 53
T0    2A1A06P07D-10
      1A4A06J02D-10
          1A0A5-L2   2- 79
T1    2A1A06P07D-09
      1A4A06J02D-09
          1A0A5-L3   2- 79
T2    2A1A06P08B-04
      1A4A06J08B-04
          1A0B4-P0   2- 69
T3    2A1A06P08B-03
      1A4A06J08B-03
          1A0B4-P1   2- 69
U0    2A1A06J20B-01
U1    2A1A06J20B-02
U2    2A1A06J20C-07
U3    2A1A06J20C-06
W0    2A1A06P07E-08
      1A4A06J02E-08
          1A0A3-S0   2- 81
W1    2A1A06P07E-07
      1A4A06J02E-07
          1A0A3-S1   2- 81
W2    2A1A06P08B-06
      1A4A06J08B-06
          1A0B4-T0   2- 69
W3    2A1A06P08B-05
      1A4A06J08B-05
          1A0B4-T1   2- 69
X0    2A1A06P07E-06
      1A4A06J02E-06
          1A0A3-L2   2- 81
X1    2A1A06P07E-05
      1A4A06J02E-05
          1A0A3-L3   2- 81
X2    2A1A06P08B-08
      1A4A06J08B-08
          1A0B4-Q0   2- 69
X3    2A1A06P08B-07
      1A4A06J08B-07
          1A0B4-Q1   2- 69

                PAGE   5- 83
```

B8 BIT 5

C2 BIT 3

B8 BIT 4

C2 BIT 4

P BIT 08 TO CSL DISPLAY
P BIT 09 TO CSL DISPLAY
C/F BIT 05 TO CONSOLE DISPLAY
BACKGROUND DIGIT 1 C DISPLAY
P BIT 07 TO CSL DISPLAY
C/F BIT 06 TO CONSOLE DISPLAY

B8 BIT 9

C2 BIT 5

B8 BIT 8

ROUNCING BALL, OCTAL DIGIT 1

B8 BIT 7

C2 BIT 6

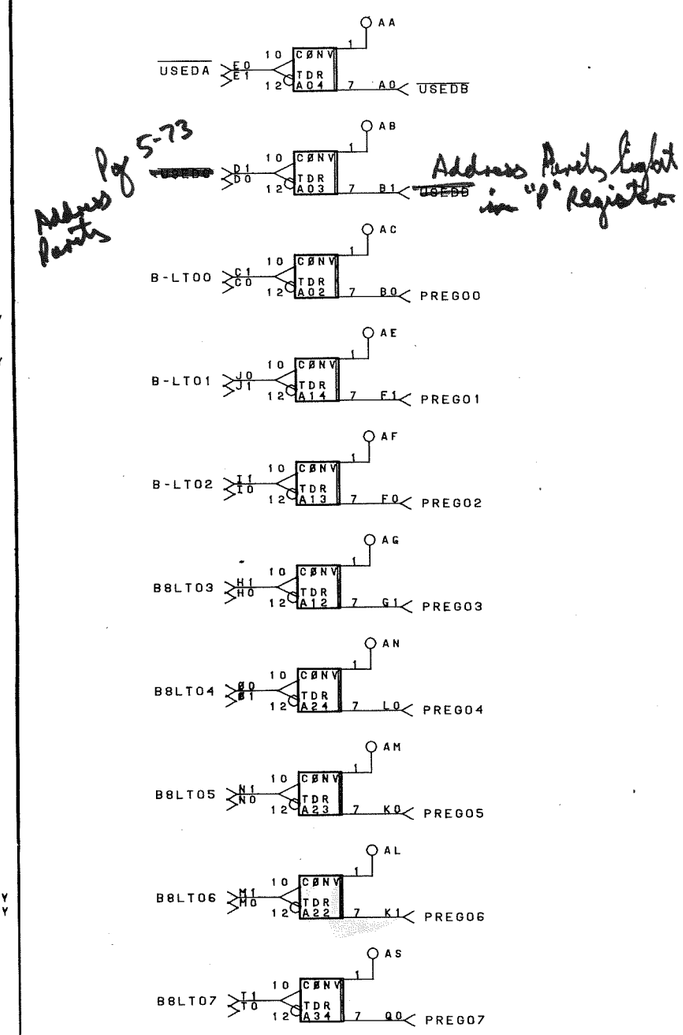
P BIT 10 TO CSL DISPLAY
P BIT 11 TO CSL DISPLAY
C/F BIT 08 TO CONSOLE DISPLAY
C/F BIT 07 TO CONSOLE DISPLAY

B8 BIT 11

C2 BIT 7

B8 BIT 10

C2 BIT 8



CONTROL DATA
DEVELOPMENT DIVISION

TCS TO DTL CONVERSION
FOR CONSOLE DISPLAYS
PART 3

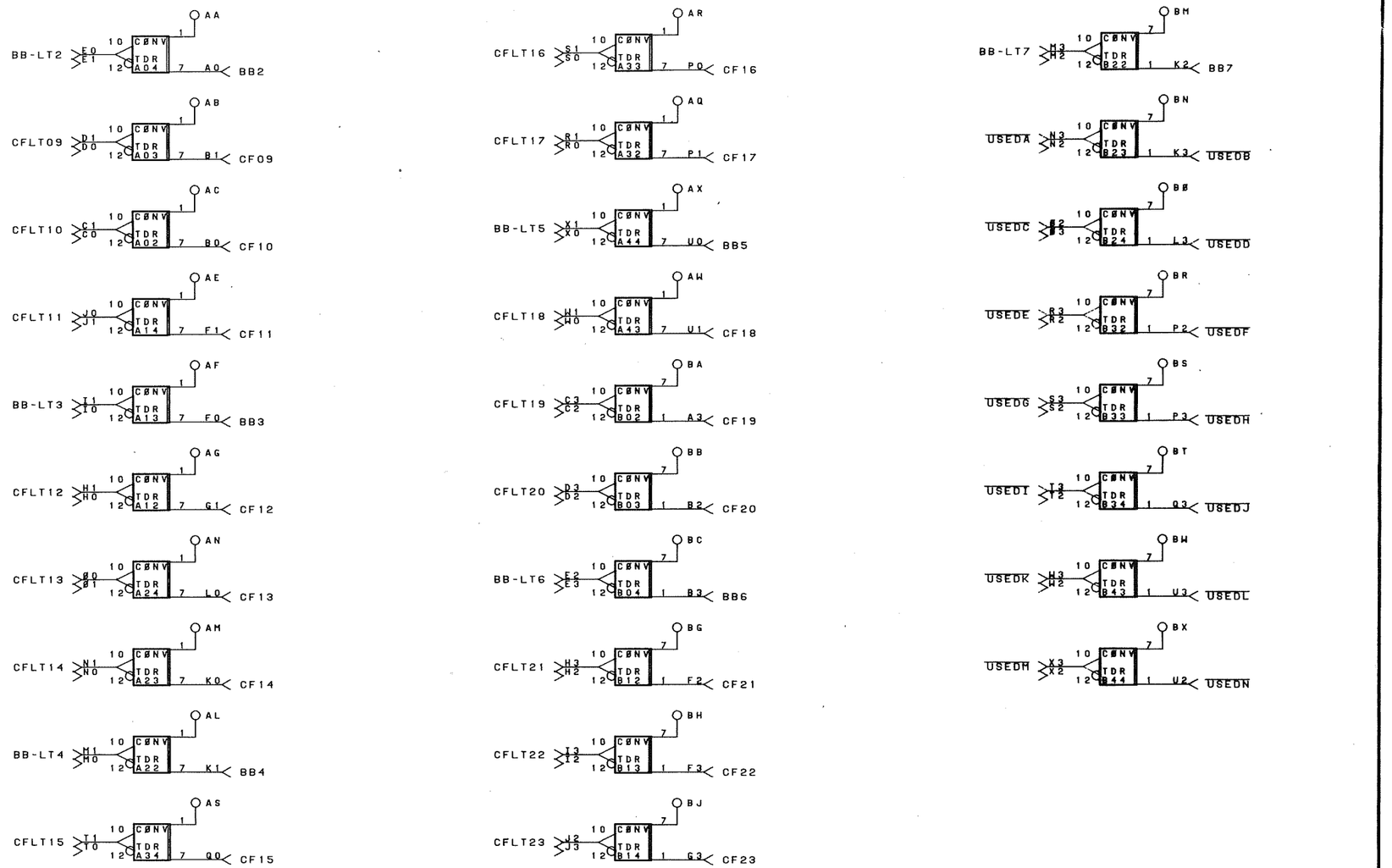
LOC:2B2B5 PART NO.185392 SER:002

PRODUCT
SIZE C | DRAWING NO. 60181000 | REV. A
SHEET | PAGE 5-83

163

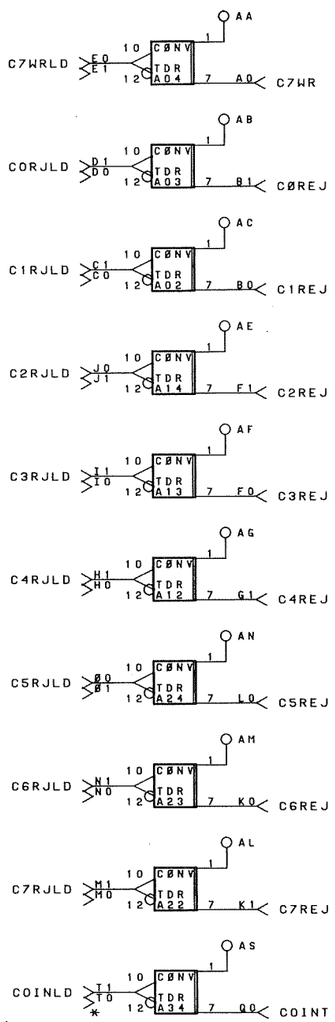
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A1A06J20C-08			BACKGROUND DIGIT 2 C DISPLAY
A3	2A1A06J20E-02			C/F BIT 19 TO CONSOLE DISPLAY
B0	2A1A06J20C-10			C/F BIT 10 TO CONSOLE DISPLAY
B1	2A1A06J20C-09			C/F BIT 09 TO CONSOLE DISPLAY
B2	2A1A06J20E-03			C/F BIT 20 TO CONSOLE DISPLAY
B3	2A1A06J20E-04			BACKGROUND DIGIT 6 C DISPLAY
C0	2A1A06P08C-02			
	1A4A06J08C-02			
	1A0B2-T0	2-71		
C1	2A1A06P08C-01			C2 BIT 10
	1A4A06J08C-01			
	1A0B2-T1	2-71		
C2	2A1A06P09C-02			
	1A4A06J12C-02			
	1R0A1-J1	2-33		
C3	2A1A06P09C-01			C2 BIT 19
	1A4A06J12C-01			
	1R0A1-J0	2-33		
D0	2A1A06P08B-10			
	1A4A06J08B-10			
	1A0B2-P0	2-71		
D1	2A1A06P08B-09			C2 BIT 9
	1A4A06J08B-09			
	1A0B2-P1	2-71		
D2	2A1A06P09C-04			
	1A4A06J12C-04			
	1R0A1-T0	2-33		
D3	2A1A06P09C-03			C2 BIT 20
	1A4A06J12C-03			
	1R0A1-T1	2-33		
E0	2A1A06J21E-09			BOUNCING BALL, OCTAL DIGIT 2
	1A4A06P04E-09			
	1C0A2-02	2-53		
E1	2A1A06J21E-10			
	1A4A06P04E-10			
	1C0A2-03	2-53		
E2	2A1A06J21F-07			BOUNCING BALL, OCTAL DIGIT 6
	1A4A06P04F-07			
	1C0A2-W3	2-53		
E3	2A1A06J21F-08			
	1A4A06P04F-08			
	1C0A2-W2	2-53		
F0	2A1A06J20D-02			BACKGROUND DIGIT 3 C DISPLAY
F1	2A1A06J20D-01			C/F BIT 11 TO CONSOLE DISPLAY
F2	2A1A06J20E-05			C/F BIT 21 TO CONSOLE DISPLAY
F3	2A1A06J20E-06			C/F BIT 22 TO CONSOLE DISPLAY
G1	2A1A06J20D-03			C/F BIT 12 TO CONSOLE DISPLAY
G3	2A1A06J20E-07			C/F BIT 23 TO CONSOLE DISPLAY
H0	2A1A06P08C-06			
	1A4A06J08C-06			
	1A0B0-P0	2-73		

H1	2A1A06P08C-05 1A4A06J08C-05 1A0B0-P1	2- 73	C2 BIT 12
H2	2A1A06P09C-06 1A4A06J12C-06 1B0A0-C1	2- 35	C2 BIT 21
H3	2A1A06P09C-05 1A4A06J12C-05 1B0A0-C0	2- 35	
I0	2A1A06J21F-02 1A4A06P04F-02 1C0A2-P2	2- 53	BOUNCING BALL, OCTAL DIGIT 3
I1	2A1A06J21F-01 1A4A06P04F-01 1C0A2-P3	2- 53	
I2	2A1A06P09C-08 1A4A06J12C-08 1B0A0-J1	2- 35	C2 BIT 22
I3	2A1A06P09C-07 1A4A06J12C-07 1B0A0-J0	2- 35	C2 BIT 11
J0	2A1A06P08C-03 1A4A06J08C-03 1A0B2-Q1	2- 71	
J1	2A1A06P08C-04 1A4A06J08C-04 1A0B2-Q0	2- 71	C2 BIT 23
J2	2A1A06P09C-09 1A4A06J12C-09 1B0A0-T1	2- 35	
J3	2A1A06P09C-10 1A4A06J12C-10 1B0A0-T0	2- 35	C/F BIT 14 TO CONSOLE DISPLAY
K0	2A1A06J20D-05		BACKGROUND DIGIT 4 C DISPLAY
K1	2A1A06J20D-06		BACKGROUND DIGIT 7 C DISPLAY
K2	2A1A06J20E-08		C/F BIT 13 TO CONSOLE DISPLAY
L0	2A1A06J20D-04		
M0	2A1A06J21F-04 1A4A06P04F-04 1C0A2-R3	2- 53	
M1	2A1A06J21F-03 1A4A06P04F-03 1C0A2-R2	2- 53	BOUNCING BALL, OCTAL DIGIT 4
M2	2A1A06J21E-04 1A4A06P04E-04 1C0A2-V3	2- 53	
M3	2A1A06J21E-03 1A4A06P04E-03 1C0A2-V2	2- 53	BOUNCING BALL, OCTAL DIGIT 7
N0	2A1A06P08C-10 1A4A06J08C-10 1A0B0-Q0	2- 73	
N1	2A1A06P08C-09 1A4A06J08C-09 1A0B0-Q1	2- 73	C2 BIT 14
O0	2A1A06P08C-07 1A4A06J08C-07 1A0B0-T1	2- 73	C2 BIT 13
O1	2A1A06P08C-08 1A4A06J08C-08 1A0B0-T0	2- 73	
P0	2A1A06J20D-08		C/F BIT 16 TO CONSOLE DISPLAY
P1	2A1A06J20D-09		C/F BIT 17 TO CONSOLE DISPLAY
Q0	2A1A06J20D-07		C/F BIT 15 TO CONSOLE DISPLAY
R0	2A1A06P09B-08 1A4A06J12B-08 1B0A2-T0	2- 31	
R1	2A1A06P09B-07 1A4A06J12B-07 1B0A2-T1	2- 31	C2 BIT 17
S0	2A1A06P09B-06 1A4A06J12B-06 1B0A2-J1	2- 31	
S1	2A1A06P09B-05 1A4A06J12B-05 1B0A2-J0	2- 31	C2 BIT 16
T0	2A1A06P09B-04 1A4A06J12B-04 1B0A2-C1	2- 31	
T1	2A1A06P09B-03 1A4A06J12B-03 1B0A2-C0	2- 31	C2 BIT 15
U0	2A1A06J20D-10		BACKGROUND DIGIT 5 C DISPLAY
U1	2A1A06J20E-01		C/F BIT 18 TO CONSOLE DISPLAY
W0	2A1A06P09B-10 1A4A06J12B-10 1B0A1-C1	2- 33	
W1	2A1A06P09B-09 1A4A06J12B-09 1B0A1-C0	2- 33	C2 BIT 18
X0	2A1A06J21F-06 1A4A06P04F-06 1C0A2-S3	2- 53	
X1	2A1A06J21F-05 1A4A06P04F-05 1C0A2-S2	2- 53	BOUNCING BALL, OCTAL DIGIT 5



CONTROL DATA DEVELOPMENT DIVISION	TCS TO DTL CONVERSION FOR CONSOLE DISPLAYS PART 4 LOC:2B2B4 PART NO.185392 SER:003	PRODUCT	
		SIZE C	DRAWING NO. 60181000
		REV. A	
		SHEET	PAGE 5-85

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A1A06J22F-06			CHAN 7 WRITE INDICATOR, CONSOLE
A3	2A1A06J22B-02			CHANNEL 5 INTERRUPT INDICATOR
B0	2A1A06J22F-08			CHANNEL 1 REJECT INDICATOR
B1	2A1A06J22F-07			CHANNEL 0 REJECT INDICATOR
B2	2A1A06J22B-03			CHANNEL 6 INTERRUPT INDICATOR
B3	2A1A06J22B-04			CHANNEL 7 INTERRUPT INDICATOR
C0	2B0A2-R1	6- 87		
C1	2B0A2-R0	6- 87		CHL 1 REJECT LIGHT DRIVER
C2	2B0B2-B3	6- 95		
C3	2B0B2-B2	6- 95		CHL 5 INTERRUPT LIGHT DRIVER
D0	2B0A3-R1	6- 85		
D1	2B0A3-R0	6- 85		CHAN 0 REJECT INDICATOR DRIVER
D2	2B0B1-B3	6- 97		
D3	2B0B1-B2	6- 97		NOT CHL 6 INT LIGHT DRIVER
E0	2B0B0-L1	6- 99		CHL 7 WRITE LIGHT DRIVER
E1	2B0B0-L0	6- 99		
E2	2B0B0-B2	6- 99		NOT CHAN 7 INT LIGHT DRIVER
E3	2B0B0-B3	6- 99		
F0	2A1A06J22A-02			CHANNEL 3 REJECT INDICATOR
F1	2A1A06J22A-01			CHANNEL 2 REJECT INDICATOR
F2	2A1A06J22B-05			CHANNEL 0 PAR, ERR, INDICATOR
F3	2A1A06J22B-06			CHANNEL 1 PAR, ERR, INDICATOR
G1	2A1A06J22A-03			CHANNEL 4 REJECT INDICATOR
G3	2A1A06J22B-07			CHANNEL 2 PAR, ERR, INDICATOR
H0	2B0B3-R1	6- 93		
H1	2B0B3-R0	6- 93		CHL 4 REJECT LIGHT DRIVER
H2	2B0A3-B0	6- 85		
H3	2B0A3-B1	6- 85		CHAN 0 PARITY ERROR LIGHT
I0	2B0A0-R1	6- 91		
I1	2B0A0-R0	6- 91		CHL 3 REJECT LIGHT DRIVER
I2	2B0A2-B0	6- 87		
I3	2B0A2-B1	6- 87		CHAN 1 PARITY ERR, LT DRIVER
J0	2B0A1-R0	6- 89		CHL 2 REJECT LIGHT DRIVER
J1	2B0A1-R1	6- 89		
J2	2B0A1-B1	6- 89		CHAN 2 PARITY ERR, LT DRIVER
J3	2B0A1-B0	6- 89		
K0	2A1A06J22A-05			CHANNEL 6 REJECT INDICATOR
K1	2A1A06J22A-06			CHANNEL 7 REJECT INDICATOR
K2	2A1A06J22B-08			CHANNEL 3 PAR, ERR, INDICATOR
K3	2A1A06J22B-09			CHANNEL 4 PAR, ERR, INDICATOR
L0	2A1A06J22A-04			CHANNEL 5 REJECT INDICATOR
L3	2A1A06J22B-10			CHANNEL 5 PAR, ERR, INDICATOR
M0	2B0B0-R1	6- 99		
M1	2B0B0-R0	6- 99		CHL 7 REJECT LIGHT DRIVER
M2	2B0A0-B0	6- 91		
M3	2B0A0-B1	6- 91		CHAN 3 PARITY ERR, LT DRIVER
N0	2B0B1-R1	6- 97		
N1	2B0B1-R0	6- 97		CHL 6 REJECT LIGHT DRIVER
N2	2B0B3-B0	6- 93		
N3	2B0B3-B1	6- 93		CHAN 4 PARITY ERR, LT DRIVER
O0	2B0B2-R0	6- 95		CHL 5 REJECT LIGHT DRIVER
O1	2B0B2-R1	6- 95		
O2	2B0B2-B1	6- 95		CHL 5 PARITY ERROR LIGHT DRIVE
O3	2B0B2-B0	6- 95		
P0	2A1A06J22A-08			CHANNEL 1 INTERRUPT INDICATOR
P1	2A1A06J22A-09			CHANNEL 2 INTERRUPT INDICATOR
P2	2A1A06J22C-01			CHANNEL 6 PAR, ERR, INDICATOR
P3	2A1A06J22C-02			CHANNEL 7 PAR, ERR, INDICATOR
Q0	2A1A06J22A-07			CHANNEL 0 INTERRUPT INDICATOR
R0	2B0A1-B3	6- 89		
R1	2B0A1-B2	6- 89		NOT CHAN 2 INT LIGHT DRIVER
R2	2B0B1-B0	6- 97		
R3	2B0B1-B1	6- 97		CHAN 6 PARITY ERR, LT DRIVER
S0	2B0A2-B3	6- 87		
S1	2B0A2-B2	6- 87		NOT CHAN 1 INT LIGHT DRIVER
S2	2B0B0-B0	6- 99		
S3	2B0B0-B1	6- 99		CHAN 7 PARITY ERR, LT DRIVER
T0	2B0A3-B3	6- 85		
T1	2B0A3-B2	6- 85		NOT CHAN 0 INT LIGHT DRIVER
U0	2A1A06J22A-10			CHANNEL 3 INTERRUPT INDICATOR
U1	2A1A06J22B-01			CHANNEL 4 INTERRUPT INDICATOR
W0	2B0B3-B3	6- 93		
W1	2B0B3-B2	6- 93		NOT CHL 4 INT LIGHT DRIVER
X0	2B0A0-B3	6- 91		
X1	2B0A0-B2	6- 91		CHL 3 INTERRUPT LIGHT DRIVER

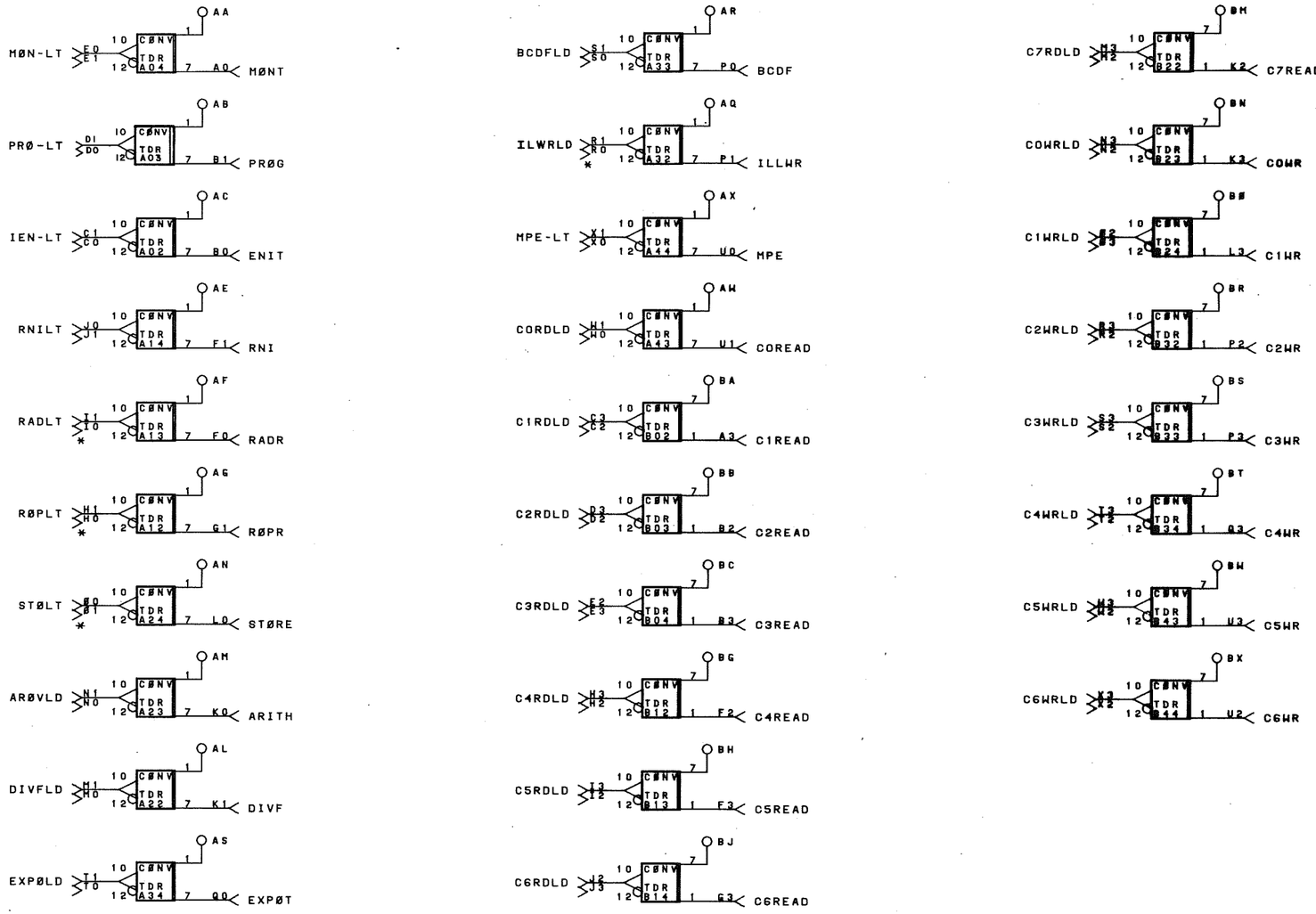


CONTROL DATA	TCS TO DTL CONVERSION FOR CONSOLE DISPLAYS PART 5	PRODUCT
DEVELOPMENT DIVISION	LOC:2B2B3 PART NO.185392 SER:004	SIZE C · DRAWING NO. 60181000 · REV. A · SHEET · PAGE 5-87

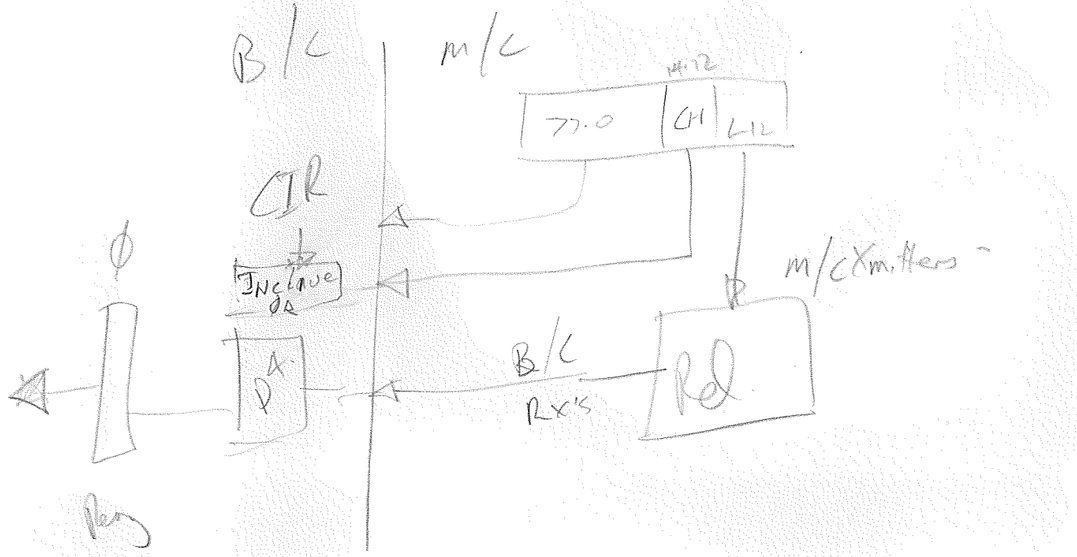
167

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A1A06J22C-08			MONITOR STATE INDICATOR
A3	2A1A06J22E-02			CHAN 1 READ INDICATOR, CONSOLE
B0	2A1A06J22C-10			INTERRUPT ENABLED INDICATOR
B1	2A1A06J22C-09			PROGRAM STATE INDICATOR
B2	2A1A06J22F-03			CHAN 2 READ INDICATOR, CONSOLE
B3	2A1A06J22E-04			CHAN 3 READ INDICATOR, CONSOLE
C0	2A1A06P06C-08			
	1A4A06J18C-08			
	1C0A4-F3	2- 41		
C1	2A1A06P06C-07			INTERRUPT ENABLED FF
	1A4A06J18C-07			
	1C0A4-F2	2- 41		
C2	2B0A2-H0	6- 87		
C3	2B0A2-H1	6- 87		CHL 1 READ LIGHT DRIVER
D0	2A1A06P06D-04			
	1A4A06J18D-04			
	1C0A0-S0	2- 37		
D1	2A1A06P06D-03			PROGRAM STATE
	1A4A06J18D-03			
	1C0A0-S1	2- 37		

D2	2B0A1-H0	6- 89	CHL 2 READ LIGHT DRIVER
D3	2B0A1-H1	6- 89	MONITOR STATE
E0	2A1A06P09D-09		
	1A4A06J12D-09		
	1C0A0-T1	2- 37	
E1	2A1A06P09D-10		
	1A4A06J12D-10		
	1C0A0-T0	2- 37	
E2	2B0A0-H1	6- 91	CHL 3 READ LIGHT DRIVER
E3	2B0A0-H0	6- 91	
F0	2A1A06J22D-02		RADR CYCLE INDICATOR
F1	2A1A06J22D-01		RNI CYCLE INDICATOR
F2	2A1A06J22E-05		CHAN 4 READ INDICATOR, CONSOLE
F3	2A1A06J22E-06		CHAN 5 READ INDICATOR, CONSOLE
G1	2A1A06J22D-03		ROP CYCLE INDICATOR
G3	2A1A06J22E-07		CHAN 6 READ INDICATOR, CONSOLE
H0	2A1A06P09B-02		
	1A4A06J12B-02		
	1B0B5-H1	2- 5	
H1	2A1A06P09B-01		NOT(ROP1 OR ROP2 CYCLE)
	1A4A06J12B-01		
	1B0B5-H0	2- 5	
H2	2B0B3-H0	6- 93	CHL 4 READ LIGHT DRIVER
H3	2B0B3-H1	6- 93	
I0	2A1A06P09A-10		
	1A4A06J12A-10		
	1B0B5-V0	2- 5	
I1	2A1A06P09A-09		NOT (RAD CYCLE FF)
	1A4A06J12A-09		
	1B0B5-V1	2- 5	
I2	2B0B2-H0	6- 95	CHL 5 READ LIGHT DRIVER
I3	2B0B2-H1	6- 95	RNI CYCLE LIGHT
J0	2A1A06P09A-07		
	1A4A06J12A-07		
	1B0B5-N1	2- 5	
J1	2A1A06P09A-08		
	1A4A06J12A-08		
	1B0B5-N0	2- 5	
J2	2B0B1-H1	6- 97	CHL 6 READ LIGHT DRIVER
J3	2B0B1-H0	6- 97	
K0	2A1A06J22D-05		ARITHMETIC OVERFLOW INDICATOR
K1	2A1A06J22D-06		DIVIDE FAULT INDICATOR
K2	2A1A06J22E-08		CHAN 7 READ INDICATOR, CONSOLE
K3	2A1A06J22E-09		CHANNEL 0 WRITE INDICATOR
L0	2A1A06J22D-04		STOR CYCLE INDICATOR
L3	2A1A06J22E-10		CHAN 1 WRITE INDICATOR, CONSOLE
M0	2B0A7-F2	6-117	
M1	2B0A7-F3	6-117	DIVIDE FAULT INDICATOR DRIVER
M2	2B0B0-H0	6- 99	
M3	2B0B0-H1	6- 99	CHL 7 READ LIGHT DRIVER
N0	2B0A7-C2	6-117	
N1	2B0A7-C3	6-117	ARITH OVFL INDICATOR
N2	2B0A3-L0	6- 85	
N3	2B0A3-L1	6- 85	CHAN 0 WRITE INDICATOR DRIVER
O0	2A1A06P06D-01		STOR CYCLE TO INDICATOR
	1A4A06J18D-01		
	1C0A0-G0	2- 37	
O1	2A1A06P06D-02		
	1A4A06J18D-02		
	1C0A0-G1	2- 37	
O2	2B0A2-L1	6- 87	CHL 1 WRITE LIGHT DRIVER
O3	2B0A2-L0	6- 87	
P0	2A1A06J22D-08		BCD FAULT INDICATOR
P1	2A1A06J22D-09		ILLEGAL WRITE INDICATOR
P2	2A1A06J22F-01		CHAN 2 WRITE INDICATOR, CONSOLE
P3	2A1A06J22F-02		CHAN 3 WRITE INDICATOR, CONSOLE
Q0	2A1A06J22D-07		EXPONENT OVERFLOW INDICATOR
Q3	2A1A06J22F-03		CHAN 4 WRITE INDICATOR, CONSOLE
R0	2B0B4-J3	6-105	
R1	2B0B4-J2	6-105	NOT ILLEGAL WRITE TO LIGHT DR
R2	2B0A1-L0	6- 89	
R3	2B0A1-L1	6- 89	CHL 2 WRITE LIGHT DRIVER
S0	2B0A7-C1	6-117	
S1	2B0A7-C0	6-117	BDP FAULT INDICATOR
S2	2B0A0-L0	6- 91	
S3	2B0A0-L1	6- 91	CHL 3 WRITE LIGHT DRIVER
T0	2B0A7-D0	6-117	
T1	2B0A7-D1	6-117	EXPONENT OVERFLOW IND DRIVER
T2	2B0B3-L0	6- 93	
T3	2B0B3-L1	6- 93	CHL 4 WRITE LIGHT DRIVER
U0	2A1A06J22D-10		STORAGE PARITY ERROR INDICATOR
U1	2A1A06J22E-01		CHAN 0 READ INDICATOR, CONSOLE
U2	2A1A06J22F-05		CHAN 6 WRITE INDICATOR, CONSOLE
U3	2A1A06J22F-04		CHAN 5 WRITE INDICATOR, CONSOLE
W0	2B0A3-H0	6- 85	
W1	2B0A3-H1	6- 85	CHAN 0 READ INDICATOR DRIVER
W2	2B0B2-L0	6- 95	
W3	2B0B2-L1	6- 95	CHL 5 WRITE LIGHT DRIVER
X0	2A1A06J21D-08		
	1A4A06P04D-08		
	1C0B3-O0	2- 49	
X1	2A1A06J21D-07		MEMORY ERROR FF
	1A4A06P04D-07		
	1C0B3-O1	2- 49	
X2	2B0B1-L0	6- 97	
X3	2B0B1-L1	6- 97	CHL 6 WRITE LIGHT DRIVER



CDC DEVELOPMENT DIVISION	TCS TO DLT CONVERSION FOR CONSOLE DISPLAYS PART 6	DRAWING C 60181000	REV. A
	LOC:2B282 PART NO. 185392 SER:005	SHEET	PAGE 5-09


B/C
m/c
M-12
77.0
CH
L12
CIR
INCLINE
m/c Xmitters
B/C
RX's
RD

Channel Coupler
Page 6-107

BLOCK CONTROL PRIORITY I AND 4

FANOUT

Ø REGISTER - CHANNEL 0 (24 BITS)
Ø REGISTER - CHANNEL 1 (24 BITS)
Ø REGISTER - CHANNEL 2 (24 BITS)
Ø REGISTER - CHANNEL 3 (24 BITS)
Ø REGISTER - CHANNEL 4 (24 BITS)
Ø REGISTER - CHANNEL 5 (24 BITS)
Ø REGISTER - CHANNEL 6 (24 BITS)
Ø REGISTER - CHANNEL 7 (24 BITS)

FANIN

TYPEWRITER Ø REGISTER (6 BITS)

SEARCH BUFFER REGISTER (6 BITS)

A

DATA FROM D^0 OR MCS

OR

RS2 CHAR
STRAIGHT

OR

STRAIGHT
RSI CHAR

BLOCK CONTROL PRIORITY 2 AND 3

PARITY

TO CHAN 0-7

FANOUT

COMPARE TO SEARCH CONTROL

DATA BUS REGISTER D4 (24 BITS)

LS1 CHAR
LS2 CHAR

OR

STRAIGHT
LS2 CHAR

OR

DATA TO D^0 OR MCS VIA PF

CLEAR SEQUENCE
PROGRAM CONTROL
CLOCK OSCILLATOR
TYPEWRITER CONTROL
SEARCH/MOVE CONTROL
CONN/FCN CONTROL
I/Ø CONTROL

BLOCK CONTROL TIMING AND TRANSLATIONS

F_U FROM MAIN CONTROL

INTERNAL STATUS
EXTERNAL STATUS

STATUS SELECT AND FAN-IN

COPY
TO A_{LI2} VIA D^0

COMPARE A
STATUS = F_{LI2} TO MAIN CONTROL

COPY
TO A_{UI2} VIA D^0

F_{LI2} FROM MAIN CONTROL

INTERRUPT MASK REGISTER (12 BITS)

INTERNAL FAULTS

INTERNAL FAULT FAN-IN

CHANNEL 0,2,4, AND 6 LINE INTERRUPTS

INTERRUPT FAN-IN (EVEN)

CHANNEL 1,3,5, AND 7 LINE INTERRUPTS

INTERRUPT FAN-IN (ODD)

INTERRUPT PRIORITY 1 AND 4

INTERRUPT PRIORITY 2 AND 3

INTERRUPT TO MAIN CONTROL
INTERRUPT IDENTIFICATION CODE TO PF
INTERRUPT IDENTIFICATION CODE TO PF

F^0 (00-05)
R/W REG FILE (BREAKPOINT SW)

S^0 REGISTER (6 BITS)

TRANSLATIONS

READ/WRITE
X
Y

REGISTER FILE (64 X 28)

ADDER

OR

BC ADDR TO PF VIA S-BUS

F^0 (00-14)
D^0 (00-17)
TRANSLATIONS

OR

STRAIGHT
LS2 CHAR

Z^0 REGISTER

COMPARE

OPR COMPLETE RF = (Z^0)

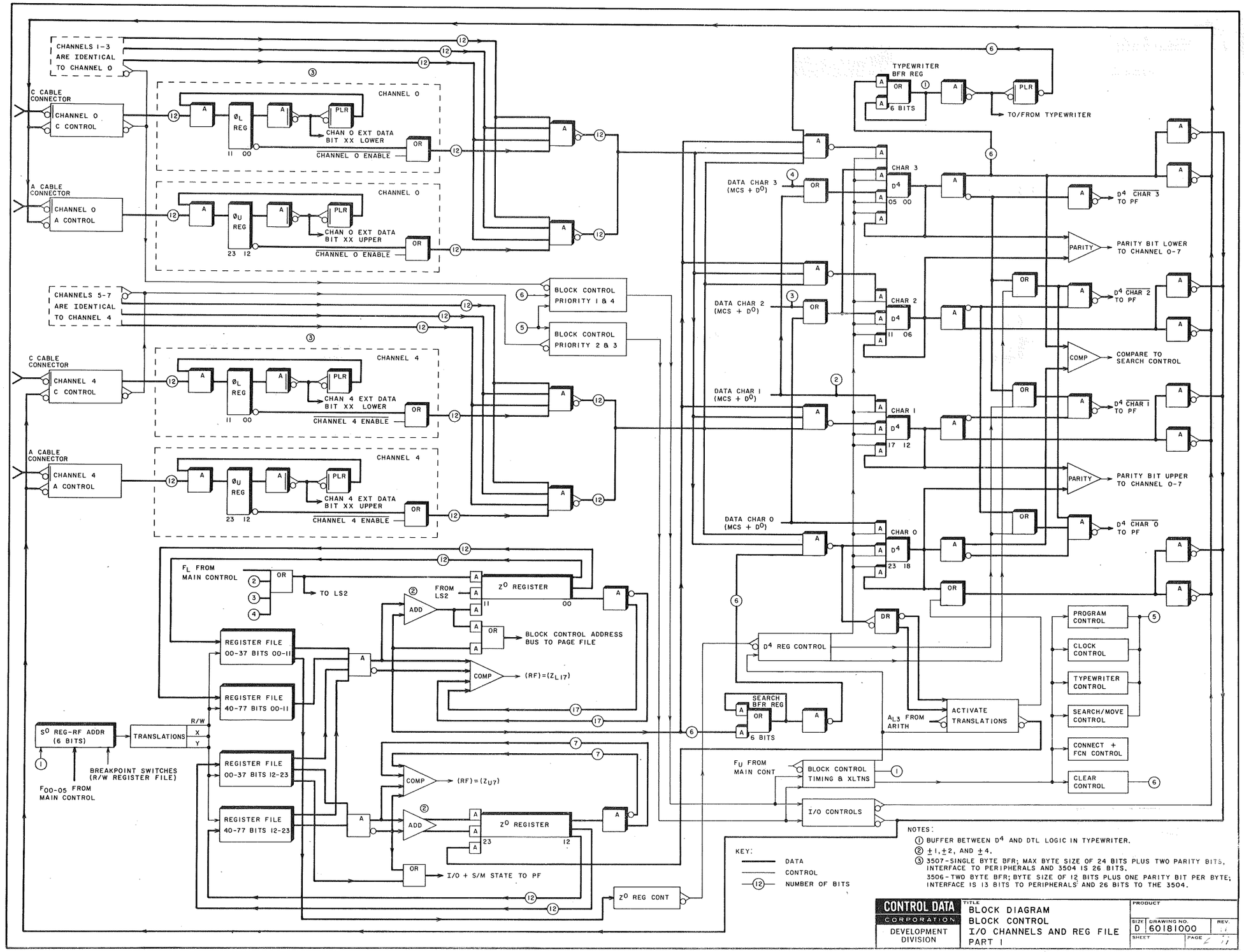
KEY:
DATA
CONTROL
6 NUMBER OF BITS

NOTES:
① BUFFER BETWEEN D^4 AND DTL LOGIC IN TYPEWRITER.
② ±1, ±2, AND ±4.
③ 3507-SINGLE BYTE BFR; MAX BYTE SIZE OF 24 BITS PLUS TWO PARITY BITS; INTERFACE TO PERIPHERALS AND 3504 IS 26 BITS.
3506-TWO BYTE BFR; BYTE SIZE OF 12 BITS PLUS ONE PARITY BIT PER BYTE; INTERFACE IS 13 BITS TO PERIPHERALS AND 26 BITS TO THE 3504.

CONTROL DATA
DEVELOPMENT DIVISION

TITLE
BLOCK DIAGRAM
BLOCK CONTROL.
DATA AND CONTROL

PRODUCT
SIZE C | DRAWING NO. 60181000 | REV. A
SHEET | PAGE 6-1


CHANNELS 1-3 ARE IDENTICAL TO CHANNEL 0
C CABLE CONNECTOR
CHANNEL 0 C CONTROL
A CABLE CONNECTOR
CHANNEL 0 A CONTROL
CHANNEL 0
ØL REG
ØU REG
CHAN 0 EXT DATA BIT XX LOWER
CHAN 0 EXT DATA BIT XX UPPER
CHANNEL 0 ENABLE
CHANNELS 5-7 ARE IDENTICAL TO CHANNEL 4
CHANNEL 4 C CONTROL
CHANNEL 4 A CONTROL
CHANNEL 4
CHAN 4 EXT DATA BIT XX LOWER
CHAN 4 EXT DATA BIT XX UPPER
CHANNEL 4 ENABLE
BLOCK CONTROL PRIORITY 1 & 4
BLOCK CONTROL PRIORITY 2 & 3
FL FROM MAIN CONTROL
TO LS2
FROM LS2
ADD
Z0 REGISTER
BLOCK CONTROL ADDRESS BUS TO PAGE FILE
REGISTER FILE 00-37 BITS 00-11
REGISTER FILE 40-77 BITS 00-11
REGISTER FILE 00-37 BITS 12-23
REGISTER FILE 40-77 BITS 12-23
COMP
(RF)=(ZL17)
(RF)=(ZU7)
S0 REG-RF ADDR (6 BITS)
TRANSLATIONS
R/W
X
Y
BREAKPOINT SWITCHES (R/W REGISTER FILE)
F00-05 FROM MAIN CONTROL
I/O + S/M STATE TO PF
Z0 REG CONT
TYPEWRITER BFR REG
6 BITS
TO/FROM TYPEWRITER
DATA CHAR 3 (MCS + D0)
DATA CHAR 2 (MCS + D0)
DATA CHAR 1 (MCS + D0)
DATA CHAR 0 (MCS + D0)
CHAR 3
CHAR 2
CHAR 1
CHAR 0
D4 CHAR 3 TO PF
D4 CHAR 2 TO PF
D4 CHAR 1 TO PF
D4 CHAR 0 TO PF
PARITY
PARITY BIT LOWER TO CHANNEL 0-7
PARITY BIT UPPER TO CHANNEL 0-7
COMP
COMPARE TO SEARCH CONTROL
D4 REG CONTROL
SEARCH BFR REG
AL3 FROM ARITH
ACTIVATE TRANSLATIONS
FU FROM MAIN CONT
BLOCK CONTROL TIMING & XLTNS
I/O CONTROLS
PROGRAM CONTROL
CLOCK CONTROL
TYPEWRITER CONTROL
SEARCH/MOVE CONTROL
CONNECT + FCN CONTROL
CLEAR CONTROL
KEY:
DATA
CONTROL
NUMBER OF BITS
NOTES:
1 BUFFER BETWEEN D4 AND DTL LOGIC IN TYPEWRITER.
2 ±1, ±2, AND ±4.
3 3507-SINGLE BYTE BFR; MAX BYTE SIZE OF 24 BITS PLUS TWO PARITY BITS, INTERFACE TO PERIPHERALS AND 3504 IS 26 BITS.
3506-TWO BYTE BFR; BYTE SIZE OF 12 BITS PLUS ONE PARITY BIT PER BYTE; INTERFACE IS 13 BITS TO PERIPHERALS AND 26 BITS TO THE 3504.
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
TITLE
BLOCK DIAGRAM
BLOCK CONTROL
I/O CHANNELS AND REG FILE
PART 1
PRODUCT
SIZE D
DRAWING NO. 60181000
REV.
SHEET
PAGE

INT PRIO 2A-2D TO EN FAN-IN

CHAN 0-7 INT PRIO

CHAN X EVEN LINE INT FAN-IN

CHAN X EVEN LINE INT PRIO

CHAN X EVEN LINE FAN-IN

CHAN X EVEN LINE

EVEN LINE X FAN-IN FOR CHAN 0-7

EVEN LINE X FOR CHAN X

CHAN 0-3 INT PRIO

CHAN 0-3 EVEN LINE

TO INT PRIO STAGE 3A

CHAN 4-7 INT PRIO

CHAN 4-7 EVEN LINE

TO INT PRIO STAGE 3B

CHAN X ODD LINE INT FAN-IN

CHAN X ODD LINE INT PRIO

CHAN X ODD LINE FAN-IN

CHAN X ODD LINE

ODD LINE X FAN-IN FOR CHAN 0-7

ODD LINE X FOR CHAN X

CHAN 0-3 ODD LINE

CHAN 4-7 ODD LINE

INT PRIO 2A-2D TO EN FAN-IN

EXT LINE

CHAN X EXT LINE INT X

CHAN X INT LIGHT DRIVER

CHAN ACTIVATE
CHAN ENABLE
CHAN X EN
INTERRUPT ON COMPLETION

SELECT INTERRUPT ON COMPLETION

CHAN TERMINATE

CHAN INTERRUPT FLIP FLOPS

OR

CHAN X MASKED INT

CHAN 0-7

CHAN X READ STATUS FAN-IN

CHAN 0-7

CHAN X WRITE STATUS FAN-IN

CHAN X EXT OVERRIDE

EXTERNAL INTERRUPT LOCKOUT (8 BITS)

F0 BITS 00-07
SET BY INSTRUCTION DURING CHAN BUSY

CHANNEL INTERRUPT ENABLE

CHAN 0-7 MASKED INT

OR

COPY 12-19 TO A REG VIA D0 IN MAIN CONTROL

S/M INT
ARITH OVERFLOW FAULT
DIVIDE FAULT
EXP UNDERFLOW OVERFLOW FAULT
BCD FAULT
REAL-TIME CLOCK INT

M A S K E D

S/M
ARITH
DIVIDE
EXP
BCD
CLOCK

COPY 20-23 TO A REG VIA D0 IN MAIN CONTROL

08-11 00-07 11 10 09 08

INTERRUPT MASK REGISTER (12 BITS)

11 00

F0 FROM MAIN CONT
SEL SET INT MASK

MANUAL INT SET

MANUAL INT

EXT INT FROM ASSOC PROCESSOR

ASSOC PROCESSOR INTERRUPT

MASKED INT/FAULT FAN-IN

81-84
5-8
9-72

CHAN 0-3
CHAN 4-7

STAGE 4 FAN-IN

PRIO 3A+3C

INTERRUPT PRIORITY STAGE 4

NORMAL INT CODE BITS 00-02

Pg 6-109 Upper Right

MASKED FAULT
BCD
DIVIDE
EXPONENT
ARITH

MASKED EXT INTERRUPT
BLOCK LINE INTERRUPTS
MASKED FAULT INTERRUPT
MASKED CHAN INTERRUPT
MASKED MISC INTERRUPT

MASKED S/M
MASKED CLOCK
MANUAL INT
ASSOC PROCESSOR INT

ARITH INT PRIO
MISC INT PRIO

INTERRUPT SYSTEM EN

OR

73-80

INTERRUPT PRIORITY STAGE I

Pg 6-109 Lower Middle

INTERRUPT TO MAIN CONT
81-84
5-8
9-72
81-84
5-8

TO PRIO STAGE 3D

LINE 0-7 FAN-IN FOR CHAN 0-7

LINE INT 0-7 FF FAN-IN

TO PRIO STAGE 3C

INTERRUPT PRIORITY STAGE 2

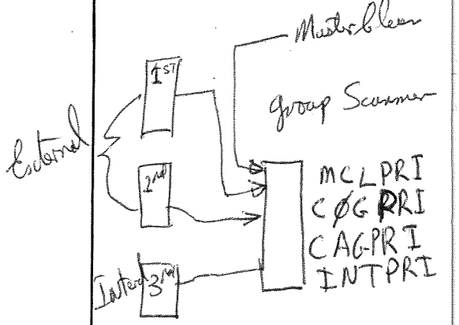
NORMAL INT CODE BITS 04-06

Pg 6-111 Lower Right

INTERRUPT PRIORITY STAGE 3

NORMAL INT CODE BIT 03

Pg 6-111 Upper Left.



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE
BLOCK DIAGRAM
BLOCK CONTROL
INTERRUPT PRIORITY
PART 2

PRODUCT

SIZE D | DRAWING NO. 60181000 | REV. L

SHEET | PAGE 6-111

175

Test BUSY
Gain Prog. Cont. Priority

Set/Clear PRGCON FF (6-25)
Set SBUSY
Set BUS LINK FF

Set. Chan. Enable
Set MCS Read FF. Enables D0 Inputs to D4.

Input (D0) into D4
This is the CON + SEL code.
Set Chan. BUSY Lockout.

Bring Up DCENAB
Set BUS to O FF
Send Clr O to Chan.
Clear MCS Read, Bus LINK FF and Chan. Enable.

(I/O With Storage) PFDRBC

(IOWA) + (CON + SEL) DCENAB

Set CONT EN FF to generate CORFEO after 250ns. *(See Inset) Set BUSOEO and send (D4) to the O Reg. From T266 through 268

A

T150-151-152-153

T154 - 155

T156-157

T158-159-160-161-162-163-164

DR

T265 - 266 - 267 - 268

T165-166

TCENIA
(SBUSY)

TCENIB
[(DBUSY) · (RWRFPR + PROGPR)]
+
[(BFRSTT)] ie Request by:
Chan. 0 through 7, CLK, TWR, or S/M

TCEN 2
(DBUSY) + (CLKCON)

TCEN 3
(PRGCON + CLKCON) +
(IOWA + B/C Clear) +
(PF Addr Reply)

TCEN 4
(D4BUSY) +
(CLKCON)

DELDRP

Another PROG CONT Cycle Will Not Be Able To Start Until After BCRPY1* (See Inset)

SBUSY Could Come Up Again If A BFRSTT Cycle Starts.

SBUSY FF (6-17)

RESCAN FF (6-11)

CONT BUSY FF (6-17)

DATA BUS REQ FF (6-17)

D4 BUSY FF (6-17)

PROG. CONT. FF (6-17) ← T268 of a BFRSTT Cycle.

SADBSY (6-17)

DBUSY (6-17) ← T268 of a BFRSTT Cycle.

Resets the B/C Priority Scanner

Allows the Scanner to Resolve Priority for the Next Cycle.

End of B/C Cycle.

DBUSY Will Allow A PROG. CONT Cycle to Start or A BFRSTT Cycle to Go Beyond T153

D4BUSY Will Prevent the Next Cycle From Going Beyond T157 If It Is A BFRSTT Except CLK, or T153 If It Is A PROG. CONT. Cycle.

SBUSY Will Allow A BFRSTT to Start the Timing Chain.

SBUSY Prevents Another Cycle From Starting Down the T.C. PROG.CONT. FF Could Extend DBUSY if the Previous Cycle Was A BFRST Cycle. SADBSY Will Prevent A Master Clear During This Cycle.

DBUSY Will Prevent Any Other Cycle Except CLK From Going Past T153

*** Inset**

T265-266-267-268

BUSOEO — Transfers the Code From D4 to O.

CONT. EN. FF — These Signals Will Drop Upon Reply or Reject From the FQ or After 100us

COOLTL

CORFEO — 250ns After T265

BCRPY1 — BCRPY1 Will Come Up At the Same Time and Allow M/C to Continue at P + 2 or P + 1.

CORFEO Enables the Equipment to Look at the Code.

MISC. CONT. TIMING
For
CON + SEL INSTRUCTION
(For Training Only)

Test BUSY
Gain PROG. CONT.
Priority.

Put Addr. 1X or 3X in S
Set SBUSY FF
F0→Z0 and Write in 1X
Set BUS LINK
Set/Clear PRGCON FF (6-25)

Clear USES03
Set RESCAN
Set Chan. Enable
Set D0 + MCS to D4 FF

D0→Z0 and Write into 0X.

Clear Rescan.

Clear BUS Link
Set I/O Activate FF
Clear D0 + MCS to D4 FF
Clear SBUSY FF
Set Cont BUSY FF
Est. S/M or Chan. Control Logic

T265 Through 268 Are Not Used In Program Activate Cycles.

PFDRBC → DR
DCENAB → A
A → A

T265-266-267-268

T165-166

A — T150-151-152-153 — A — T154 - 155 — A — T156-157 — A — T158 - 159 - 160 - 161 - 162 - 163 - 164

TCENIA
$\overline{\text{SBUSY}}$

TCENIB
[$\overline{\text{DBUSY}}$) · (RWRFPR + PROGPR)]
+
[BFRSTT] ie Request By:
Chan. 0 through 7, CLK, TWR, or S/M.

TCEN2
$\overline{\text{DBUSY}}$) + (CLKCON)

TCEN3
(PRGCON + CLKCON) +
(IOWA + B/C Clear) +
(PF Addr. Reply)

TCEN4
($\overline{\text{D4BUSY}}$) +
(CLKCON)

BCRPY1 to M/C
So M/C Can Read
the Next Instr.

SBUSY Could Come Up if
A BFRSTT Cycle Starts.

SBUSY FF (6-17)

RESCAN FF (6-11)

CONT BUSY FF (6-17)

DATA BUS REQ FF (6-17)

D4 BUSY FF (6-17)

PROG CONT FF (6-17) ← T268 of a BFRSTT Cycle.

SADBSY (6-17) — If a BFRSTT Cycle Has Started, SADBSY Will Not Drop

DBUSY (6-17) ← T268 of a BFRSTT Cycle.

$\overline{\text{SBUSY}}$ Will Allow a BFRSTT to Start the Timing Chain

$\overline{\text{DBUSY}}$ Signals the End of This Cycle and Allows A PROG. CON Cycle to Start or a BFRSTT Cycle to Continue Beyond T153.

$\overline{\text{SBUSY}}$ Prevents Another Cycle From Starting Down The Timing Chain.
$\overline{\text{PROG CONT FF}}$ Gives SETFRD and Could Extend DBUSY if the Previous Cycle Was A BFRSTT.
$\overline{\text{SADBSY}}$ Will Prevent A Master Clear During This Cycle.

Resets the B/C Priority Scanner

Allows the Scanner to Resolve Priority for the Next Cycle

DBUSY Will Prevent Any Other Cycle Except CLK From Going Beyond T153

MISC. CONTROL TIMING
For
PROGRAM ACTIVATE
(For Training Only)

Set Early PF Reserve Gain BFRSTT Priority (Request Generated in the Channel)

Put Address 0X in S Reg. Read 0X and Put Address on BUS. Set SBUSY and I/O Cont. FF. Incr/Decr (0X) Set PF Reserve FF

Incr/Decr (0X) to Z. Set PF Request FF Set Chan. Enable and Resume, Set Char. Desig. FF's Wait for PFARBC.

Set S03 and Read (1X) Compare (1X) to (Z) Set Strip/Duplicate Write (Z) into (0X) Clear PF Request FF

Input to D4 from Storage or D0 Reg. if IOWA. Test Operation Complete. Send Clear O Reg. to Chan. Set MCS Read FF

(I/O With Storage) PFDRBC

(I/O With A) DCENAB

Set BUSOEO and Transfer Data from D4 to Chan. O Reg from T266 through T268. Clear MCS Read FF

T265-266-267-268

DELDRP

T165-166

T150-151-152-153

T154-155

T156-157

T158-159-160-161-162-163-164

TCENIA
(SBUSY)

TCENIB
[(DBUSY) · (RWRFPR + PROGPR)]
+
[(BFRSTT)] ie Request By:
Chan. 0 through 7, CLK, TWR, or S/M

TCEN2
(DBUSY) + (CLKCON)

TCEN3
(PRGCON + CLKCON) +
(IOWA + B/C Clear) +
(PF Addr Reply)

TCEN4
(D4BUSY) +
(CLKCON)

Set BLINK if IOWA

Send BCRPY2 to M/C if IOWA

If IOWA, T165 and T265 Occur At About the Same Time.

Clear BLINK if IOWA

This Timing Ensures That the Data in D4 Will Not Change Until the O Reg. Gating is Dropped.

Wait for PFARBC if I/O With Storage

SBUSY Could Come Up Again if A BFRSTT Cycle Starts

Must Wait For PF Data Reply if I/O With Storage

If A PROG CONT Cycle Starts

SBUSY FF (6-17)

RESCAN FF (6-11)

CONT BUSY FF (6-17)

DATA BUS REQ FF (6-17)

D4BUSY FF (6-17)

PROG CONT FF (6-17)

SADBSY (6-17)

DBUSY (6-17)

T150 of Next Cycle if it is a PROG. CONT. Cycle

SBUSY Prevents Another Cycle From Starting Down the Timing Chain.

SADBSY Will Prevent A Master Clear During This Cycle.

Resets the B/C Priority Scanner

Allows the Scanner to Resolve Priority for the Next Cycle

DBUSY Will Prevent Any Other Cycle Except CLK From Going Beyond T153

SBUSY Will Allow A BFRSTT to Start the Timing Chain.

D4BUSY Will Prevent the Next Cycle from going Beyond T157 if it is A BFRSTT Cycle, Except For CLK, or T153 if it is A PROG. CONT. Cycle.

DBUSY Will Allow A PROG. CONT. Cycle to Start or A BFRSTT Cycle to Continue Past T153.

If This Cycle is followed by a PROG. CONT. Cycle DBUSY Will Come Up Again to Ensure That the PROG. CONT. Cycle Does Not Get Past T153.

MISC. CONT. TIMING
For
Buffer Output
(For Training Only)

Set Early PF Reserve
Gain BFRSTT Priority
(Request generated in the channel)

Put Addr. 0X in S Reg.
Read 0X and Put Addr. on BUS
Set SBUSY and Control Logic
Incr/Decr. (0X)
Set PF Reserve FF

Incr/Decr (0X) into Z.
Set PF Request FF
Set Chan. Enable and Resume
Set Char. Desig. FF

Set S03 and Read (1X)
Compare (1X) to (Z).
Set Strip/Duplicate
Set MCS Write FF
Write (Z) Int 0X

Input to D4 from Chan. and Gate the Data to D0 or Storage Via Reloc. Section.
Send Clear O Reg. to Chan.
Set PW FFs., Test Op. Compl.

(I/O With Storage) PFDRBC → DR
(I/O With A) DCENAB → A
A → T265-266 - 267 - 268

Clear Data Bus Required FF
Clear MCS Write

TCENIA ($\overline{SBUSY}$)
TCENIB [($\overline{DBUSY}$) · (RWRFPR + PROGPR)] + [(BFRSTT)] ie Request By: Chan. 0 Through 7, CLK, TWR, or S/M
A → T150-151-152-153

TCEN2 ($\overline{DBUSY}$) + (CLKCON)
A → T154-155

TCEN3 (PRGCON + CLKCON) + (IOWA + B/C Clear) + (PF Addr Reply)
A → T156-157
Set BLINK if IOWA

TCEN4 ($\overline{D4BUSY}$) + (CLKCON)
A → T158-159-160 - 161 - 162-163-164

Send BCRPY1 to M/C if IOWA

T165-166

$\overline{DELDRP}$

If IOWA, T265 and T165 Occur At About the Same Time.

Clear BLINK if IOWA

Wait for PFARBC if I/O With Storage

SBUSY Could Come Up Again Here if A BFRSTT Cycle Starts.

Must Wait for Page File Data Reply if I/O With Storage

SBUSY Could Come Up Again Here if A PROG. CONT. Cycle Starts.

SBUSY FF	(6-17)	
RESCAN FF	(6-11)	
CONT BUSY FF	(6-17)	
DATA BUS REQ FF	(6-17)	
D4 BUSY FF	(6-17)	
PROG CONT FF	(6-17)	T150 of Next Cycle if it is A PROG. CONT. Cycle
SADBSY	(6-17)	
DBUSY	(6-17)	

SBUSY Prevents Another Cycle From Starting Down the Timing Chain

SADBSY Will Prevent A Master Clear During This Cycle.

Resets the B/C Priority Scanner

Allows the Scanner to Resolve Priority for the Next Cycle.

DBUSY Will Prevent Any Other Cycle Except CLK from Going Beyond T153

$\overline{SBUSY}$ Will Allow A BFRSTT to Start the Timing Chain.

D4BUSY Will Prevent the Next Cycle from Going Beyond T157 if it is A BFRSTT Cycle, Except For CLK, or T153 if it is A PROG. CONT. Cycle.

If This Cycle is Followed by A PROG. CONT. Cycle, DBUSY Will Come Up Again to Insure the Prog. Cycle Does Not Get Past T153

$\overline{DBUSY}$ Will Allow A PROG. CONT. Cycle to Start or A BFRSTT Cycle to Continue Past T153.

MISC. CONT. TIMING
For
Buffer Input
(For Training Only)

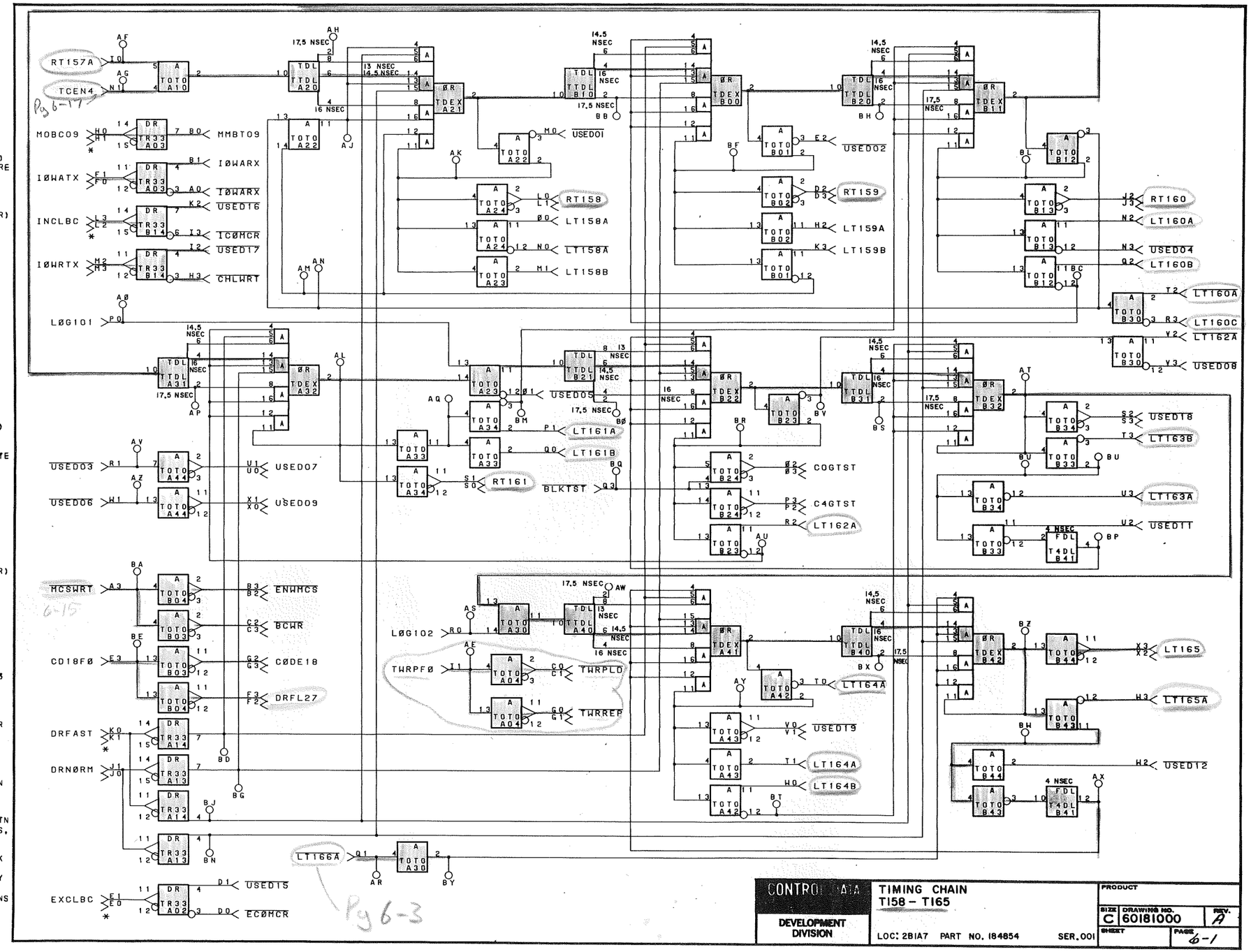
Reg File & Cycle Control Time
Page 6-41

Data Xfer
Page 6-183

Special Data Xfer from
TM from D4
Page 6-3

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1B6-I3	6- 15		NOT (I/O WITH A XLTN)
A3	2B1B6-P3	6- 15	2B1A7-RA	NOT(MCS WRITE) TO FAN OUT
B0	2B1A8-W2	6- 17	2B1A8-RX	MAINT MODE REG BIT 09
B1	2B1A6-W3	6- 13		I/O WITH A XLTN
B2	2A1B4-M2	6- 57		NOT FN SET OF PARTIAL WRITES
B3	2A1B4-M3	6- 57		
C0	2B2B6-X0	5- 81		
C1	2B2B6-X1	5- 81		NOT TW REPEAT LIGHT DRIVER
C2	2A2A5-N1	5- 3		
C3	2A2A5-N0	5- 3		NOT RC MCS WRITE TO PF
D0	2B1B1-M0	6- 9	2B1B1-AP	NOT(EXT CLR + MASTER CLR REQ)
D2	2A1B4-F0	6- 57		T159 TO Z PANEL + TEST COMPARE
D3	2A1B4-F1	6- 57		
E0	2A1A06P06B-02			
	1A4A06J18B-02			
	1C0B3-T2	2- 49		
E1	2A1A06P06B-01			NOT (MASTER CLR +EXTERNAL CLR)
	1A4A06J18B-01			
	1C0B3-T3	2- 49		
E3	2B1A9-G3	6- 23	2B1A7-BE	
F0	2A1B4-W1	6- 57		
F1	2A1B4-W0	6- 57		I/O WITH A XLTN
F2	2A1A2-L0	6- 67		
F3	2A1A2-L1	6- 67		DIGIT DRIVE 27 TO RF 00-37
G0	2B0A6-P1	6-121		
G1	2B0A6-P0	6-121		NOT TW REPEAT TO STATUS F1
G2	2A1B8-V3	6- 53		INPUT TO Z REG BIT 18
G3	2A1B8-V2	6- 53		
H0	2A1A06P06A-05			NOT BIT 09 OF MAINT.REGISTER
	1A4A06J18A-05			
	1C1B7-S0	3- 15		
H1	2A1A06P06A-06			
	1A4A06J18A-06			
	1C1B7-S1	3- 15		
H2	2B1A6-C3	6- 13		T159 TO ACT; AND SEARCH FFS
H3	2B1B6-C3	6- 15		NOT(CHL WRITE XLTN)
I0	2B1A8-Q3	6- 17	2B1A7-AF	T157 + INPUT TO T158 DELAY
I1	2B1B9-R2	6- 27	2B1A7-AE	TWR REPEAT XLTN TO FAN OUT
I3	2B1B1-K1	6- 9	2B1B1-AM	NOT(INT CLR + MASTER CLR REQ)
J0	2B1B7-Q2	6- 3		
J1	2B1B7-Q3	6- 3		NORMAL TIMING SELECT
J2	2A1B6-W2	6- 43		T160 TO Z PANEL + CLR RF WRITE
J3	2A1B6-W3	6- 43		
K0	2B1B7-X3	6- 3		NOT FAST TIMING SELECT
K1	2B1B7-X2	6- 3		
K3	2B1B6-V1	6- 15		T159 TO BC REPLY TO MAIN CONTROL XLTN
L0	2A1B4-N3	6- 57		T158 TO Z PANEL + CLR/SET PARTIAL WRITE
L1	2A1B4-N2	6- 57		
L2	2A1A06P06B-04			
	1A4A06J18B-04			
	1C0B3-S2	2- 49		
L3	2A1A06P06B-03			NOT (MASTER CLR +INTERNAL CLR)
	1A4A06J18B-03			
	1C0B3-S3	2- 49		
M1	2B1B6-L1	6- 15		T158 TO INPUT TO D4 XLTN
M2	2A1B4-V1	6- 57		I/O WRITE XLTN
M3	2A1B4-V0	6- 57		
N0	2B1A8-M1	6- 17	2B1A8-AO	NOT(T158) CLR CHL RESUME
N1	2B1A8-M2	6- 17	2B1A7-AG	TIMING CHAIN ENABLE 4
N2	2B1B8-O1	6- 11		T160 - SET TWR DATA EN
O0	2B1A6-D3	6- 13		T158 CLR/SET D4 CONT + S/M CONTROL
O2	2A0A4-V0	6-157		TEST OPR COMPL/PE TO CHAN 0-3
O3	2A0A4-V1	6-157		
P1	2B1A8-C2	6- 17	2B1A8-RC	T161 TO READ MCS XLTN
P2	2C0B4-V1	6-193		
P3	2C0B4-V0	6-193		TEST OPR COMP/PE TO CHAN 4-7
Q0	2B1B6-P2	6- 15		T161 TEST MAINT MODE RF ERROR
Q1	2B1B7-F1	6- 3	2B1A7-AR	NOT(T166) - CLEAR T165
Q2	2B1A8-I3	6- 17	2B1A8-RN	T160 - SET DATA TIMING BUSY
Q3	2B1A9-C2	6- 23	2B1A7-BQ	NOT(BLOCK CHAN TEST SIGNAL)
R2	2B1B6-V0	6- 15		T162 TO BC REPLY TO MAIN CONTROL XLTN
R3	2B1B1-P3	6- 9		T160 - SET CONN + FCN DATA EN
S0	2A1B6-L3	6- 43		
S1	2A1B6-L2	6- 43		T161 TO Z PANEL + CLR S BUSY
T0	2B1A8-A0	6- 17	2B1A8-AB	NOT(T164) TO CLR Q REG XLTN
T1	2B1B7-A3	6- 3		T164 TO START DATA TIMING XLTN
T2	2B1B6-Q3	6- 15		NOT(T160)- CLR+SET MISC CONTS,
T3	2B1A8-D1	6- 17		NOT(T163) TO CLR Q REG XLTN
U3	2B1B8-Q0	6- 11		NOT(T163) TO CLR TWR LOCKOUT
W2	2B1A6-R3	6- 13		NOT (T162) + CLR D TO Z/BLINK
W0	2B1B6-G0	6- 15		T164 TO CLR PRG REQ XLTN
W3	2B1A8-G2	6- 17	2B1A8-RH	NOT(T165) TO CLR CONTROL BUSY
X2	2B1B7-G3	6- 3		
X3	2B1B7-G2	6- 3		T165 TO T166 DELAY AND XLTNS

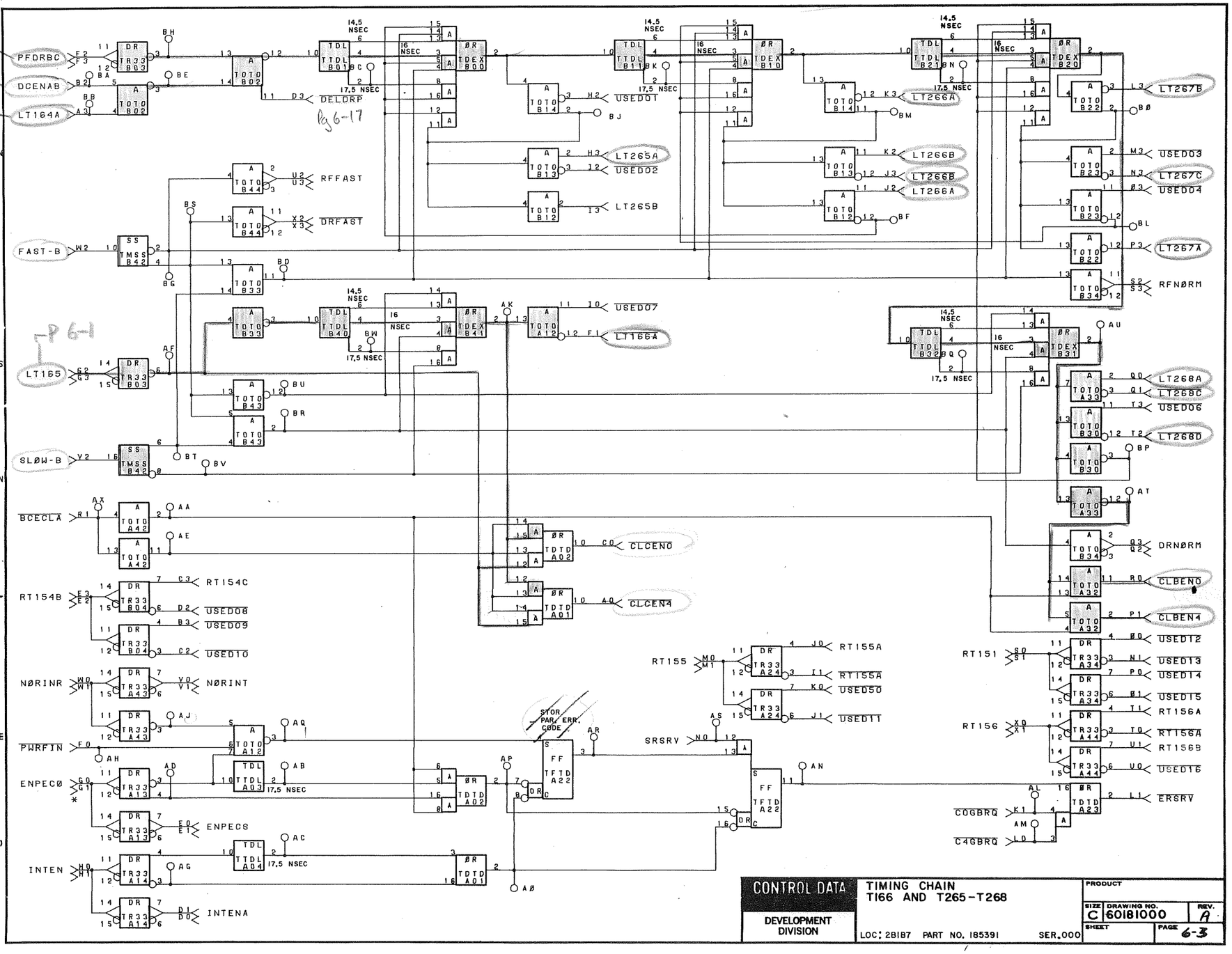
PAGE 6- 1



Pg 6-3

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1B5-P0	6- 21		NOT(CLR CHL ENABLES 4-7)
A3	2B1A7-T1	6- 1		T164 TO START DATA TIMING XLTN
B2	2B1B6-S3	6- 15	2B1B7-RA	DATA TIMING CHAIN ENABLE FOR CONN + FUNC + INA + OTA
C0	2B1A5-P0	6- 19		NOT(CLR CHL ENABLES 0-3)
C3	2B1B6-Q0	6- 15		T154 TO INPUT TO D4 XLTN
D0	2B0B6-P2	6-115		
D1	2B0B6-P3	6-115		INTERRUPTS ENABLED
D3	2B1A8-A3	6- 17	2B1A8-BO	NOT(DELAYED DATA REPLY)
E0	2B2B8-G1	5- 77		ENABLE MCS PE CODE TO PF
E1	2B2B8-G0	5- 77		
E2	2A1B7-P2	6- 41		
E3	2A1B7-P3	6- 41		T154
F0	2B1A8-V1	6- 17	2B1B7-AH	NOT(POWER FAILURE INTERRUPT)
F1	2B1A7-Q1	6- 1	2B1A7-AR	NOT(T166) - CLEAR T165
F2	2A2A7-T1	5- 5		DATA REPLY TO BLOCK CONTROL
F3	2A2A7-T0	5- 5		
G0	2A1A06P03E-01			NOT(FN PAR ERR CODE + M CLR)
	1A4A06J20E-01			
	1C0A1-D3	2- 43		
G1	2A1A06P03E-02			
	1A4A06J20E-02			
	1C0A1-D2	2- 43		
G2	2B1A7-X3	6- 1		T165 TO T166 DELAY AND XLTNS
G3	2B1A7-X2	6- 1		
H0	2A1A06P03E-05			INTERRUPT ENABLED FF
	1A4A06J20E-05			
	1C0A4-C3	2- 41		
H1	2A1A06P03E-06			
	1A4A06J20E-06			
	1C0A4-C2	2- 41		
H3	2B1B8-O0	6- 11		T265 - TO TWR BFR CONTROLS
I1	2B1A6-M3	6- 13		NOT (T155) - TO S/M BFR CONT
I3	2B1B1-Q3	6- 9		T265 - SET CONTROL ENABLE F/F
J0	2B1B8-W0	6- 11		T155 - TO CLOCK/TW/PROG CONT
J2	2B1A6-L3	6- 13		T266 - TEST SEARCH COMPL, XLTN
J3	2B1A8-E1	6- 17	2B1A8-AD	NOT(T266) - TO BUS TO 0 XLTNS
K1	2B1A0-Q1	6- 5	2B1B7-AL	NOT(CHL 0-3 BC REQUEST)
K2	2B1B6-J1	6- 15		T266 - TO CLR BLINK XLTN
K3	2B1B1-P2	6- 9		NOT (T266) - CLR CONN + FCN DATA ENABLE
L0	2B1B0-Q1	6- 7	2B1B7-AM	NOT(CHL 4-7 BC REQUEST)
L1	2B1A8-O1	6- 17	2B1A8-AQ	NOT(EARLY PF RESERVE)
L3	2B1A8-Q1	6- 17	2B1A8-AT	NOT(T267) - TO BUS TO 0 XLTNS
M0	2A1B7-S2	6- 41		T155
M1	2A1B7-S3	6- 41		
N0	2B1A8-G1	6- 17	2B1B7-AS	PAGE FILE RESERVED BY RC
N3	2B1B6-L3	6- 15		NOT(T267) - CLEAR MISC CONTROL
P1	2B1B5-M0	6- 21		NOT(CLR BUS TO 0 REG EN 4-7)
P3	2B1A6-B3	6- 13		NOT(T267) - CLR SEARCH DATA
Q0	2B1A8-Q0	6- 17	2B1A8-AU	T268 - TO BUS TO 0 XLTNS
Q1	2B1A8-I2	6- 17	2B1A8-RH	NOT(T268)- CLR D4 TIMING BUSY
Q2	2B1A7-J0	6- 1		
Q3	2B1A7-J1	6- 1		NORMAL TIMING SELECT
R0	2B1A5-M0	6- 19		NOT(CLR BUS TO 0 REG EN 0-3)
R1	2B1B1-G0	6- 9	2B1B7-AX	NOT (CLEAR CHAN ENABLES)
S0	2A1B7-D2	6- 41		T151
S1	2A1B7-D3	6- 41		
S2	2A1B7-J1	6- 41		NORMAL TIMING SEL, TO Z PANEL
S3	2A1B7-J0	6- 41		
T0	2B1A8-O0	6- 17	2B1A8-AR	NOT(T156)- CLR PF RESERVE F/F
T1	2B1A6-X3	6- 13		T156 - CLR/SET D4 STRIP CONT.
T2	2B1B8-P0	6- 11		NOT(T268)- CLR TWR DATA ENABLE
U1	2B1B6-J0	6- 15		T156 - TO INPUT TO D4 XLTN
U2	2A1B7-K0	6- 41		FAST TIMING SELECT TO Z PANEL
U3	2A1B7-K1	6- 41		
V0	2A1A06P03E-03			NORMAL INT XLTN TO MN CONT
	1A4A06J20E-03			
	1C0A1-S0	2- 43		
V1	2A1A06P03E-04			
	1A4A06J20E-04			
	1C0A1-S1	2- 43		
V2	2A2A04J03H-03			NOT(BC SLOW TIMING SELECTED)
W0	2B0A8-E2	6-109		(NORMAL INTERRUPTS)(NOT ARITH)
W1	2B0A8-E3	6-109		
W2	2A2A04J03G-03			NOT(BC FAST TIMING SELECTED)
X0	2A1B7-V0	6- 41		T156
X1	2A1B7-V1	6- 41		
X2	2B1A7-K1	6- 1		
X3	2B1A7-K0	6- 1		NOT FAST TIMING SELECT

PAGE 6- 3



CONTROL DATA
DEVELOPMENT DIVISION

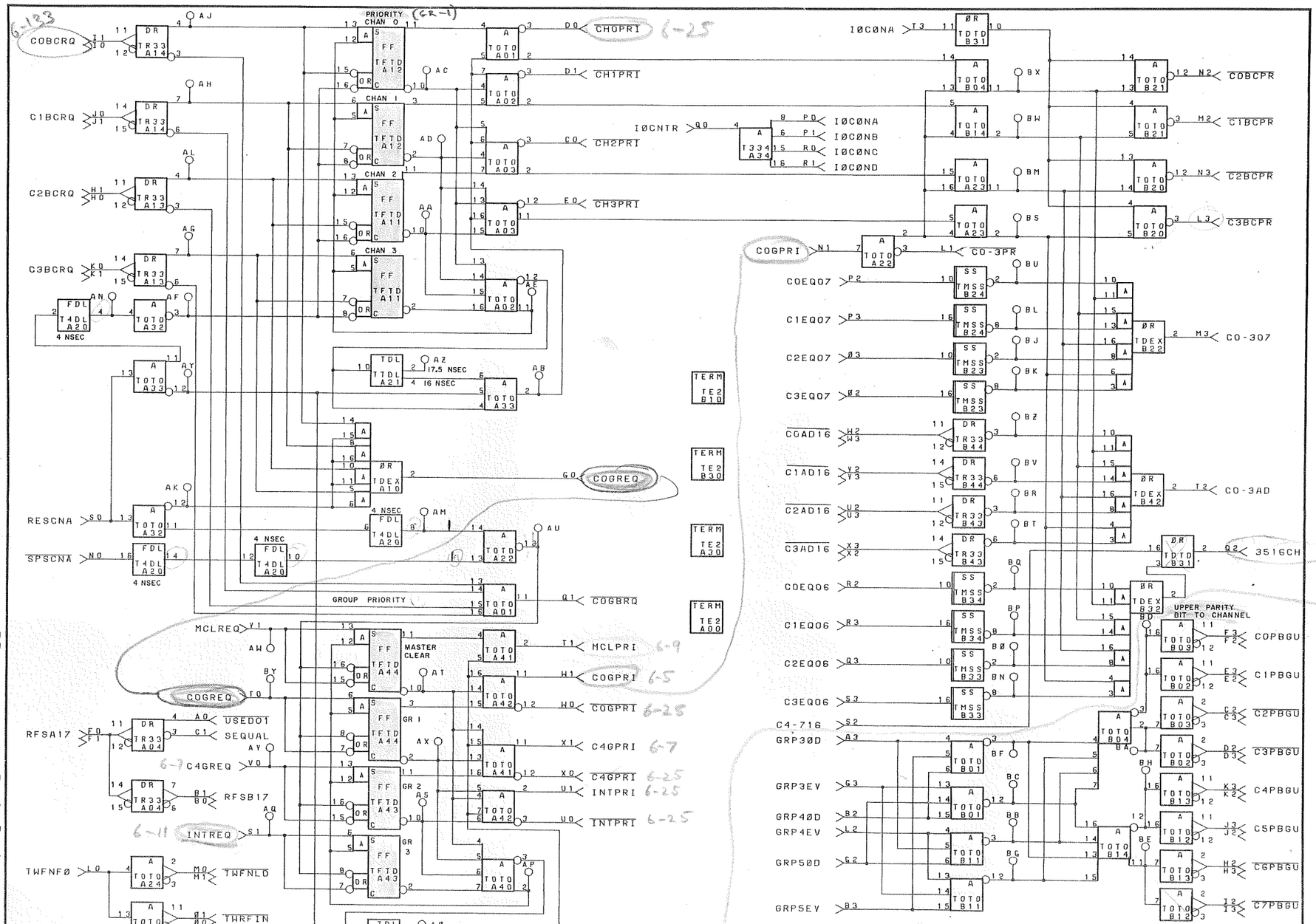
TIMING CHAIN
T166 AND T265-T268

LOC: 2B1B7 PART NO. 185391 SER.000

PRODUCT
SIZE C | DRAWING NO. 60181000 | REV. A
SHEET | PAGE 6-3

187

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A3	2B1B3-W3	6- 31		SUM OF 12/13/18/19= ODD TOTAL
B0	2B1A2-T0	6- 39		
B1	2B1A2-T1	6- 39		REG. FILE TO D4 REG. - BIT 17
B2	2B1A4-W3	6- 35		SUM OF 14/15/20/21= ODD TOTAL
B3	2B1A2-S3	6- 39		SUM OF 16/17/22/23= EVEN TOTAL
C0	2B1A1-C2	6- 25		NOT (CHAN 2 INITIAL BC PRIO)
C1	2B1A1-R0	6- 25		SEARCH EQUALITY
C2	2AAB1-D0	6-151		
C3	2AAB1-D1	6-151		NOT UPPER PARITY BIT TO CHAN 2
D0	2B1A1-A3	6- 25		NOT (CHAN 0 INITIAL BC PRIO)
D1	2B1A1-D2	6- 25		NOT (CHAN 1 INITIAL BC PRIO)
D2	2AAB8-D0	6-155		
D3	2AAB8-D1	6-155		NOT UPPER PARITY BIT TO CHAN 3
E0	2B1A1-C3	6- 25		NOT (CHAN 3 INITIAL BC PRIO)
E2	2AAB8-D0	6-147		
E3	2AAB8-D1	6-147		UPPER PARITY BIT TO CHANNEL 1
F0	2A1B8-K1	6- 53		RF SENSE AMP BIT 17 TO D4 REG
F1	2A1B8-K2	6- 53		
F2	2AAB9-D0	6-143		
F3	2AAB9-D1	6-143		UPPER PARITY BIT TO CHANNEL 0
G0	2B1A0-T0	6- 5	2B1A0-BY	(CHL 0-3 BC REQ) (NOT RESCAN)
G2	2B1A2-W3	6- 39		SUM OF 16/17/22/23= ODD TOTAL
G3	2B1B3-S3	6- 31		SUM OF 12/13/18/19= EVEN TOTAL
H0	2AAA3-Q0	6-137		
H1	2AAA3-Q1	6-137		CHL 2 BLOCK CONTROL REQUEST
H2	2CAA1-D0	6-187		
H3	2CAA1-D1	6-187		NOT UPPER PARITY BIT TO CHL 6
I0	2AAA7-Q0	6-133		
I1	2AAA7-Q1	6-133		CHL 0 BLOCK CONTROL REQUEST
I2	2CAA0-D0	6-191		
I3	2CAA0-D1	6-191		NOT UP. PAR. BIT TO CHAN 7
J0	2AAA6-Q1	6-135		CHL 1 BLOCK CONTROL REQUEST
J1	2AAA6-Q0	6-135		
J2	2CAA8-D0	6-183		
J3	2CAA8-D1	6-183		UPPER PARITY BIT TO CHANNEL 5
K0	2AAA2-Q1	6-139		CHL 3 BLOCK CONTROL REQUEST
K1	2AAA2-Q0	6-139		
K2	2CAA9-D0	6-179		
K3	2CAA9-D1	6-179		UPPER PARITY BIT TO CHANNEL 4
L0	2B1B9-Q2	6- 27		TWR FINISH XLTN TO FAN OUT
L1	2B1A1-U1	6- 25		NOT(CHL 0-3 BC PRIORITY XLTN)
L2	2B1A4-S3	6- 35		SUM OF 14/15/20/21= EVEN TOTAL
L3	2B1A5-X3	6- 19	2B1A5-BZ	NOT(CHL 3 BC PRIORITY XLTN)
M0	2B2B6-R0	5- 81		
M1	2B2B6-R1	5- 81		NOT TYPEWRITER FINISH LIGHT DR
M2	2B1A5-W3	6- 19	2B1A5-BX	NOT(CHL 1 BC PRIORITY XLTN)
M3	2B1B[illegible]-S2	6- 7		CHAN 0-3 24-BIT MODE PRIORITY TRANSLATION
N0	2B1B8-Q3	6- 11		NOT(SPECIAL SCAN BC PRIO 4)
N1	2B1A[illegible]-W1	6- 5		CHL 0-3 FINAL BC PRIORITY
N2	2B1A5-V2	6- 19	2B1A5-BW	NOT(CHL 0 BC PRIORITY XLTN)
N3	2B1A5-V3	6- 19	2B1A5-BY	NOT(CHL 2 BC PRIORITY XLTN)
O0	2B0A5-P0	6-123		NOT TW FINISH STATUS BIT 09
O1	2B0A5-P1	6-123		
O2	2A4A15J01G-02			CHAN 3 24-BIT MODE
O3	2A4A15J01E-02			CHAN 2 24-BIT MODE
P0	2B1A[illegible]-T3	6- 5		I/O CONTROL - EN CHAN 0-3 XLTN
P1	2B1B[illegible]-T3	6- 7		I/O CONTROL - EN CHAN 4-7 XLTN
P2	2A4A15J01A-02			CHAN 0 24-BIT MODE
P3	2A4A15J01C-02			CHAN 1 24-BIT MODE
Q0	2B1A1-R1	6- 25		I/O CONTROL XLTN TO FANOUT
Q1	2B1B7-K1	6- 3	2B1B7-AL	NOT(CHL 0-3 BC REQUEST)
Q2	2B1A1-V1	6- 25	2B1A1-AZ	12-BIT MODE CHAN PRIORITY
Q3	2A4A15J01F-02			CHAN 2 12-BIT MODE
R0	2B1A8-U0	6- 17	2B1A8-AV	I/O CONTROL - EN CHAN RESUME
R1	2B1B6-D3	6- 15		I/O CONTROL - EN I/O R/W XLTN
R2	2A4A15J01B-02			CHAN 0 12-BIT MODE
R3	2A4A15J01D-02			CHAN 1 12-BIT MODE
S0	2B1B8-Q2	6- 11		RESCAN TO BC PRIORITY 1 AND 4
S1	2B1B8-Q3	6- 11	2B1A0-AQ	INTERNAL OPR REQ TO BC PRI. 4
S2	2B1B[illegible]-M3	6- 7		CHAN 4-7 12-BIT MODE PRIO XLTN
S3	2A4A15J01H-02			CHAN 3 12-BIT MODE
T0	2B1A0-G0	6- 5	2B1A0-BY	(CHL 0-3 BC REQ) (NOT RESCAN)
T1	2B1B1-C0	6- 9		MASTER CLEAR FINAL BC PRIORITY
T2	2B1A1-P1	6- 25		CHAN 0-3 A/D PRIORITY XLTN
T3	2B1A[illegible]-P0	6- 5		I/O CONTROL - EN CHAN 0-3 XLTN
U0	2B1A1-J3	6- 25		NOT(INTERNAL OPR FINAL BC PRIORITY)
U1	2B1A1-E2	6- 25		INTERNAL OPR FINAL BC PRIORITY
U2	2AAA3-T1	6-137		
U3	2AAA3-T0	6-137		NOT((CH 2)(12-BIT MODE)(A/D))
V0	2B1B[illegible]-G0	6- 7	2B1A0-AV	(CHL 4-7 BC REQ) (NOT RESCAN)
V1	2B1B1-P1	6- 9	2B1A0-AW	MASTER CLEAR REQ TO BC PRI. 4
V2	2AAA6-T1	6-135		
V3	2AAA6-T0	6-135		NOT((CH 1)(12-BIT MODE)(A/D))
W0	2B1A1-R3	6- 25		NOT(CHL 0-3 FINAL BC PRIORITY)
W1	2B1A[illegible]-N1	6- 5		CHL 0-3 FINAL BC PRIORITY
W2	2AAA7-T1	6-133		
W3	2AAA7-T0	6-133		NOT((CH 5)(12-BIT MODE)(A/D))
X0	2B1A1-H3	6- 25		NOT(CHL 4-7 FINAL BC PRIORITY)
X1	2B1B[illegible]-N1	6- 7		CHL 4-7 FINAL BC PRIORITY
X2	2AAA2-T0	6-139		NOT((CH 3)(12-BIT MODE)(A/D))
X3	2AAA2-T1	6-139		



CONTROL DATA CORPORATION	BLOCK CONTROL PRIORITY 1 AND 4 Parity Bit to Channel	PRODUCT
DEVELOPMENT DIVISION	LOC: 2B1A0 PART NO. 185304 SER. 000	SIZE C | DRAWING NO. 60181000 | REV E
		SHEET | PAGE 6-5

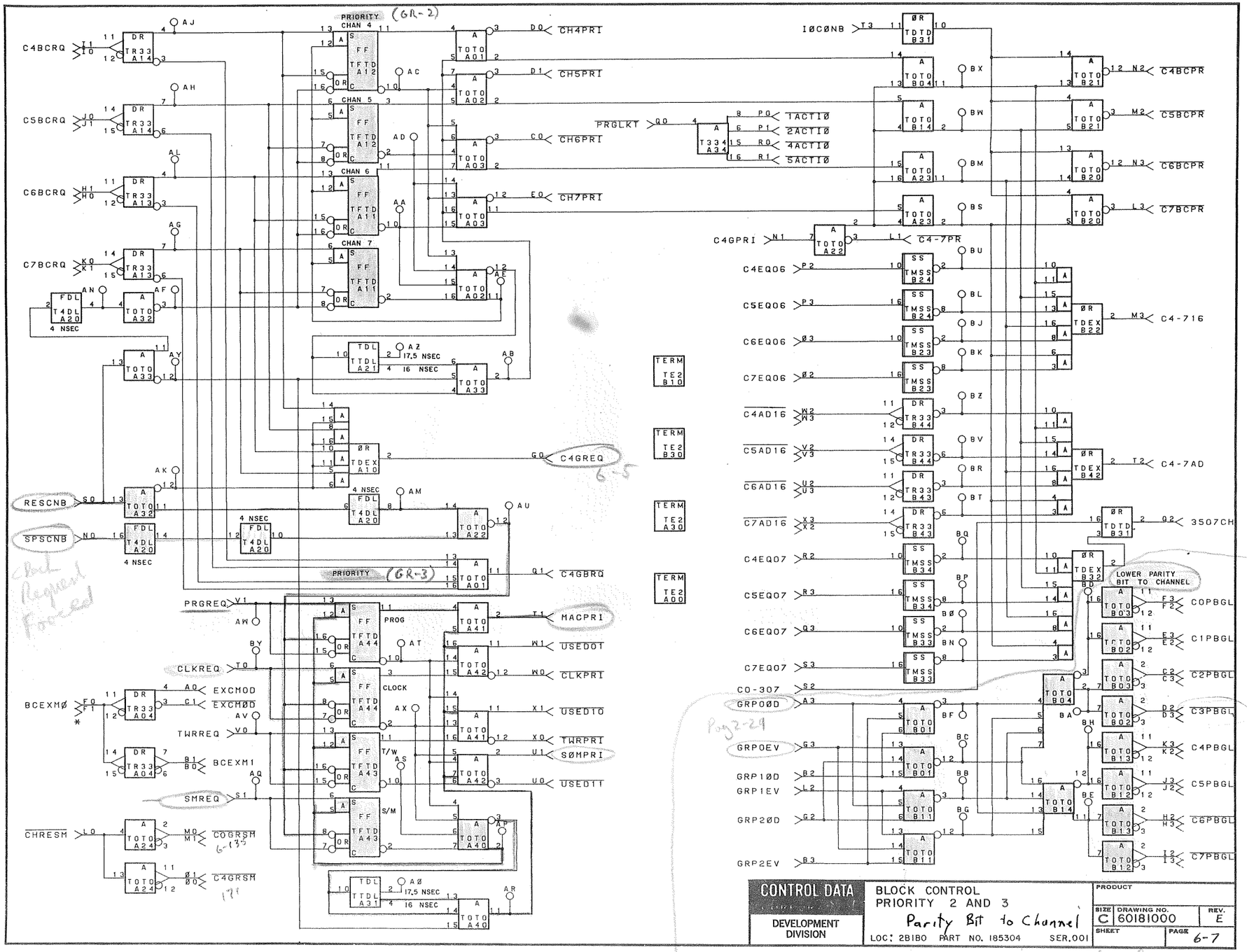
Priority!

Group 1	Group 2	group 3
chan. 0 1 2 3	chan 4 5 6 7	PROGRAM Real Time Typewriter Searchfmouse

Parity Ø Upper 189

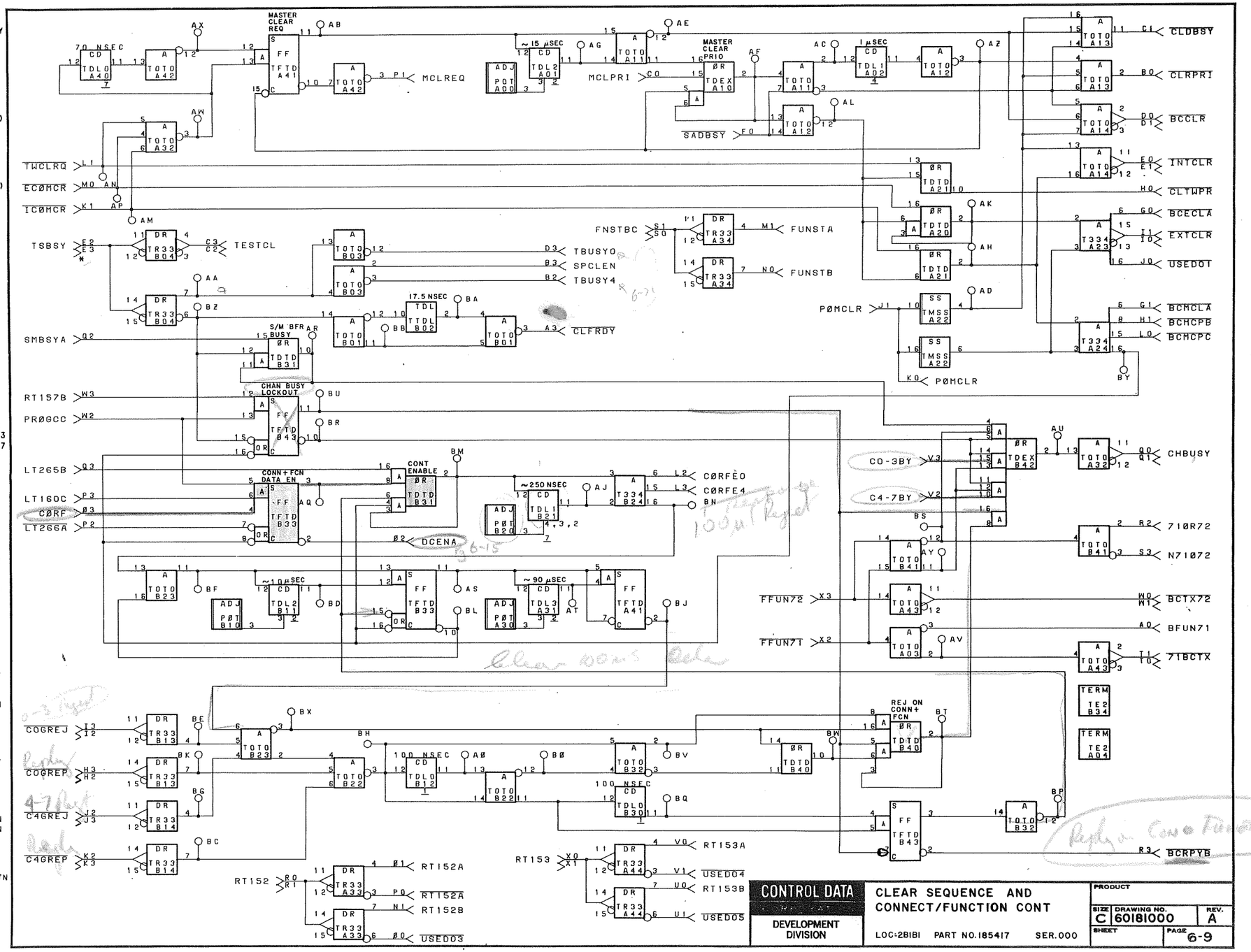
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1A9-R2	6- 23	2B1A9-RR	EXECUTIVE MODE TO CONTROL XLTN
A3	2B1B4-W3	6- 29		SUM OF 00/01/06/07= ODD TOTAL

B0		2A1AB-W0	6- 55		BC EXECUTIVE MODE
B1		2A1AB-W1	6- 55		SUM OF 02/08/03/09= ODD TOTAL
B2		2B1B2-W3	6- 33		SUM OF 04/05/10/11= EVEN TOTAL
B3		2B1A3-S3	6- 37		NOT (CHAN 6 INITIAL BC PRIO)
C0		2B1A1-G3	6- 25		NOT(EXEC MODE) TO CONTROL XLTN
C1		2B1A9-Q3	6- 23		
C2		2A2A1-D0	6-149		NOT LOWER PARITY BIT TO CHAN 2
C3		2A2A1-D1	6-149		NOT (CHAN 4 INITIAL BC PRIO)
D0		2B1A1-H2	6- 25		NOT (CHAN 5 INITIAL BC PRIO)
D1		2B1A1-F3	6- 25		
D2		2A2A1-D0	6-153		NOT LOWER PARITY BIT TO CHAN 3
D3		2A2A1-D1	6-153		NOT (CHAN 7 INITIAL BC PRIO)
E0		2B1A1-G2	6- 25		
E2		2A2A8-D0	6-145		LOWER PARITY BIT TO CHANNEL 1
E3		2A2A8-D1	6-145		NOT (EXEC MODE) SIGNAL TO B.C.
F0	2A1A06P06A-09				
	1A4A06J18A-09				
		1C2B0-C1	2- 45		
F1	2A1A06P06A-10				
	1A4A06J18A-10				
		1C2B0-C0	2- 45		
F2		2A2A9-D0	6-141		LOWER PARITY BIT TO CHANNEL 0
F3		2A2A9-D1	6-141		(CHL 4-7 BC REQ) (NOT RESCAN)
G0		2B1A6-V0	6- 5	2B1A0-AV	SUM OF 04/05/10/11= ODD TOTAL
G2		2B1A3-W3	6- 37		SUM OF 00/01/06/07= EVEN TOTAL
G3		2B1B4-S3	6- 29		
H0		2C2B3-Q0	6-173		CHL 6 BLOCK CONTROL REQUEST
H1		2C2B3-Q1	6-173		
H2		2C2B1-D0	6-185		NOT LOW PARITY BIT TO CHL 6
H3		2C2B1-D1	6-185		
I0		2C2B7-Q0	6-169		CHL 4 BLOCK CONTROL REQUEST
I1		2C2B7-Q1	6-169		
I2		2C2B6-D0	6-189		NOT LOW PARITY BIT TO CHL 7
I3		2C2B6-D1	6-189		CHL 5 BLOCK CONTROL REQUEST
J0		2C2B6-Q0	6-171		
J1		2C2B6-Q1	6-171		
J2		2C2B8-D0	6-181		LOWER PARITY BIT TO CHANNEL 5
J3		2C2B8-D1	6-181		CHL 7 BLOCK CONTROL REQUEST
K0		2C2B2-Q1	6-175		
K1		2C2B2-Q0	6-175		
K2		2C2B9-D0	6-177		
K3		2C2B9-D1	6-177		LOWER PARITY BIT TO CHANNEL 4
L0		2B1A8-K0	6- 17		NOT(CHANNEL RESUME) TO FAN OUT
L1		2B1A1-V0	6- 25		NOT(CHL 4-7 BC PRIORITY XLTN)
L2		2B1B2-S3	6- 33		SUM OF 02/08/03/09= EVEN TOTAL
L3		2B1B5-X3	6- 21	2B1B5-BZ	NOT(CHL 7 BC PRIORITY XLTN)
M0		2A2A6-W3	6-135		
M1		2A2A6-W2	6-135		NOT BC RESUME TO CHAN 0-3
M2		2B1B5-W3	6- 21	2B1B5-BX	NOT (CHL 5 BC PRIORITY XLTN)
M3		2B1A6-S2	6- 5		CHAN 4-7 12-BIT MODE PRIO XLTN
N0		2B1B8-U3	6- 11		NOT(SPECIAL SCAN BC PRIO 3)
N1		2B1A6-X1	6- 5		CHL 4-7 FINAL BC PRIORITY
N2		2B1B5-V2	6- 21	2B1B5-BW	NOT(CHL 4 BC PRIORITY XLTN)
N3		2B1B5-V3	6- 21	2B1B5-BY	NOT(CHL 6 BC PRIORITY XLTN)
O0		2C2B6-W2	6-171		NOT BC RESUME TO CHLS 4-7
O1		2C2B6-W3	6-171		
O2	2A4A15J01S-02				CHAN 7 12-BIT MODE
O3	2A4A15J01P-02				CHAN 6 12-BIT MODE
P0		2B1B4-R3	6- 29	2B1B4-BU	NOT (ACT. I/O - BLOCK D4 BIT 18)
P1		2B1B3-R3	6- 31	2B1B3-BU	NOT (ACT. I/O - BLOCK D4 BIT 19)
P2	2A4A15J01K-02				CHAN 4 12-BIT MODE
P3	2A4A15J01M-02				CHAN 5 12-BIT MODE
Q0		2B1B8-U2	6- 11		NOT(PROGRAM LOCKOUT) TO FANOUT
Q1		2B1B7-L0	6- 3	2B1B7-AM	NOT(CHL 4-7 BC REQUEST)
Q2		2B1A1-U0	6- 25	2B1A1-AW	24-BIT MODE CHAN PRIORITY
Q3	2A4A15J01N-02				CHAN 6 24-BIT MODE
R0		2B1A4-R3	6- 35	2B1A4-BU	NOT (ACT. I/O - BLOCK D4 BIT 21)
R1		2B1A3-R3	6- 37	2B1A3-BU	NOT (ACT. I/O - BLOCK D4 BIT 22)
R2	2A4A15J01J-02				CHAN 4 24-BIT MODE
R3	2A4A15J01L-02				CHAN 5 24-BIT MODE
S0		2B1B8-V2	6- 11		RESCAN TO BC PRIORITY 2 AND 3
S1		2B1A6-N1	6- 13	2B1B0-AQ	S/M REQUEST TO BC PRIORITY 3
S2		2B1A7-M3	6- 5		CHAN 0-3 24-BIT MODE PRIORITY TRANSLATION
S3	2A4A15J01R-02				CHAN 7 24-BIT MODE
T0		2B1B8-A0	6- 11	2B1B9-BY	CLOCK BFR REQ TO BC PRIORITY 3
T1		2B1A1-E3	6- 25		MAIN CONT INITIAL BC PRIORITY
T2		2B1A1-Q0	6- 25		CHAN 4-7 A/D PRIORITY XLTN
T3		2B1A7-P1	6- 5		I/O CONTROL - EN CHAN 4-7 XLTN
U1		2B1A1-K3	6- 25		SRCH + MOVE - INITIAL BC PRIO
U2		2C2B3-T1	6-173		
U3		2C2B3-T0	6-173		NOT((CH 6)(12-BIT MODE)(A/D))
V0		2B1B8-N0	6- 11	2B1B6-AV	TWR BFR REQUEST TO BC PRI. 3
V1		2B1B8-M3	6- 11	2B1B6-AW	PROG REQUEST TO BC PRIORITY
V2		2C2B6-T1	6-171		
V3		2C2B6-T0	6-171		NOT((CH 5)(12-BIT MODE)(A/D))
W0		2B1A1-I2	6- 25		NOT(CLOCK INITIAL BC PRIORITY)
W2		2C2B7-T1	6-169		
W3		2C2B7-T0	6-169		NOT((CH 4)(12-BIT MODE)(A/D))
X0		2B1A1-K2	6- 25		NOT(TWR INITIAL BC PRIORITY)
X2		2C2B2-T0	6-175		NOT((CH 7)(12-BIT MODE)(A/D))
X3		2C2B2-T1	6-175		



PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1A6-J2	6- 13		F=71 - ACTIVATE SEARCH
A3	2B1B8-K2	6- 11		NOT(CLR FUNCTION READY FF)
B0	2B1B8-T3	6- 11		NOT(CLEAR PRIORITY LOGIC)

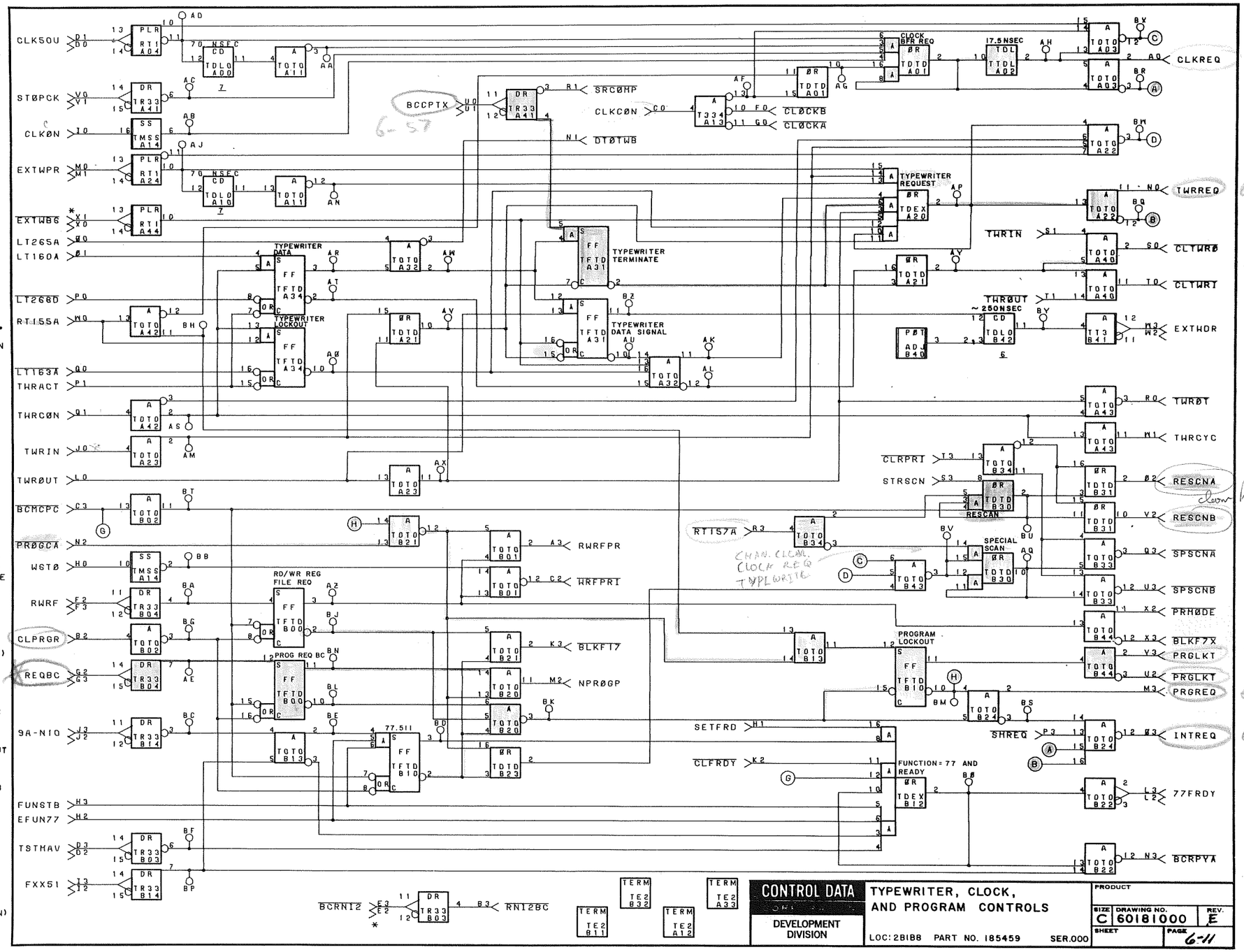
B2		2R1B5=N2	6= 21		TEST CHL 4=7 BUSY
B3		2R1A9=D1	6= 23		SPECIAL CLEAR OF TIMED XLTN
C0		2R1A0=T1	6= 5		MASTER CLEAR FINAL BC PRIORITY
C1		2R1A8=I1	6= 17	2B1A8=AK	NOT(CLEAR D4 BUSY)
C2		2R0A9=X1	6=101		
C3		2R0A9=X0	6=101		TEST CLEAR TO INTERNAL FAULTS
D0		2A1B6=J1	6= 43		
D1		2A1B6=J0	6= 43		NOT RC CLEAR
D3		2R1A5=N2	6= 19		TEST CHL 0=3 BUSY
E0		2R0A8=L2	6=109		
E1		2R0A8=L3	6=109		NOT(INTERNAL CLR *MASTER CLR* POWER ON MASTER CLR)
E2	2A1A06P05R=09				NOT(TEST BUSY) SIG TO R CONT)
	1A4A06J14R=09				
		1R0A4=01	2= 1		
E3	2A1A06P05R=10				
	1A4A06J14R=10				
		1R0A4=00	2= 1		
F0		2B1A8=K3	6= 17		NOT(ADDRESS AND DATA REG BUSY)
G0		2B1B7=R1	6= 3	2B1B7=AX	NOT (CLEAR CHAN ENABLES)
G1		2B1A6=V2	6= 13		NOT (CLEAR SEARCH/MOVE CONT)
H0		2B1B9=T3	6= 27		NOT(CLR TYPEWRITER BFR)
H1		2B1B9=R3	6= 27		NOT (CLEAR TW BFR CONTROLS)
H2		2A0A4=F3	6=157		NOT CHAN 0=3 CONN + FCN REPLY FAN=IN
H3		2A0A4=F2	6=157		
I0		2R0B6=03	6=115		EXT CLEAR I/O THRU CHAN
I1		2R0B6=02	6=115		
I2		2A0B5=F3	6=159		NOT CHAN 0=3 CONN + FCN EXT REJECT FAN=IN
I3		2A0B5=F2	6=159		
J1	2A1A06J16R=07				SWITCH, POWER ON MASTER CLEAR
J2		2C0A5=F2	6=195		
J3		2C0A5=F3	6=195		NOT CHL 4=7 CONN + FCN EXT REJECT FAN=IN
K0		2A2B9=V2	5= 23		SWITCH, POWER ON MASTER CLEAR
K1		2R1A7=I3	6= 1	2B1B1=AH	NOT(INT CLR + MASTER CLR REQ)
K2		2C0B4=F2	6=193		
K3		2C0R4=F3	6=193		NOT CHL 4=7 CONN + FCN REPLY FAN=IN
L0		2R1B8=C3	6= 11		NOT(CLEAR PROG/TW CONTROLS)
L1		2R1B9=Q3	6= 27	2B1B1=AN	NOT(TWR CLEAR REQ) TO CLR BFR
L2		2R1A5=N3	6= 19		CONN + FCN TO CONTROL XLTN 0=3
L3		2R1B5=N3	6= 21		CONN + FCN TO CONTROL XLTN 4=7
M0		2R1A7=D0	6= 1	2B1B1=AP	NOT(EXT CLR + MASTER CLR REQ)
M1		2R1A9=D0	6= 23		FUNCTIONS STABLE
N0		2R1B8=H3	6= 11		FUNCTIONS STABLE
N1		2R1A8=H1	6= 17	2B1A8=RY	T152 = SET PF RESERVE
O1		2R1A6=U2	6= 13		T152 = TEST MOVE COMPLETE
O2		2R1B6=R3	6= 15		NOT(DATA TIMING CHAIN EN ON CONN + FCN)
O3		2R1A9=01	6= 23		CONN + FCN XLTN TO CONN + FCN CONTROL
P0		2R1A8=W3	6= 17	2B1A8=RT	NOT (T152) = RESYNC MAINT H REGISTER = BIT 09
P1		2R1A0=V1	6= 5	2B1A0=AW	MASTER CLEAR REQ TO BC PRI, 4
P2		2R1B7=K3	6= 3		NOT (T266) = CLR CONN + FCN DATA ENABLE
P3		2R1A7=R3	6= 1		T160 = SET CONN + FCN DATA EN
Q0	2A1A06P05E=03				SELECTED CHAN BUSY + REJECT CONN + FCN
	1A4A06J14E=03				
		1R0B2=V2	2= 23		
Q1	2A1A06P05E=04				
	1A4A06J14E=04				
		1R0B2=V3	2= 23		
Q2		2R1A6=L1	6= 13		S/M BFR BUSY TO MN CONT TEST FAN-IN
Q3		2R1B7=I3	6= 3		T265 = SET CONTROL ENABLE F/F
R0		2A1B7=J2	6= 41		T152
R1		2A1B7=J3	6= 41		
R2		2R1A6=H2	6= 13		F=71+72 = ENABLE ACTIVATE S/M
R3		2R1B6=U0	6= 15		NOT(RC REPLY TO MN CONT ON CONN + FCN)
S0	2A1A06P05R=08				
	1A4A06J14R=08				
		1R0A4=S3	2= 1		
S1	2A1A06P05R=07				FUNCTION STABLE TO BLOCK CONT
	1A4A06J14R=07				
		1R0A4=S2	2= 1		
S3		2R1A9=S2	6= 23		NOT(F=71+72) TO Z REG FAN IN
T0		2A1R6=X2	6= 43		NOT(F=71)
T1		2A1B6=X3	6= 43		
U0		2R1B6=X1	6= 15		T153 = TO BC REPLY TO MC XLTN
V0		2R1A6=X2	6= 13		T153 = TEST NC MOVE/D TO Z EN
V2		2R1B5=A3	6= 21		SELECTED CHANNEL (4=7) BUSY
V3		2R1A5=A3	6= 19		SELECTED CHANNEL (0=3) BUSY
W0		2A1B7=F0	6= 41		
W1		2A1B7=F1	6= 41		NOT(F = 72)
W2		2R1A6=01	6= 13		PROG CONT EN = CONN + FCN XLTN
W3		2R1A8=P3	6= 17		T157 = SET CHL BUSY LOCKOUT
X0		2A1B7=S1	6= 41		T153
X1		2A1B7=S0	6= 41		
X2		2R1A9=L0	6= 23		NOT(FCN CODE=71)TO FANOUT
X3		2R1A9=K1	6= 23		NOT(FCN CODE=72)TO FANOUT



193

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1B0-T0	6- 7	2B1B0-RY	CLOCK BFR REQ TO BC PRIORITY 3
A3	2B1B6-C1	6- 15	2B1B6-AD	READ/WRITE REGISTER FILE CONT
B2	2B1B6-I0	6- 15		CLEAR PROGRAM REQUESTS
B3	2B1A9-C0	6- 23		NOT(RNI 2) FROM MN CONT TO BC
C0	2B1A1-X2	6- 25		CLOCK CONT XLTN TO CLOCK BFR
C2	2B1A9-U1	6- 23		WRITE REGISTER FILE CONTROL

C3	2B1B1-L7	6- 9		NOT(CLEAR PROG/TW CONTROLS)
D0	2A1A06J15C-04			
	2A1A06J16C-04			
D1	2A1A06J15C-03			CLOCK PULSE-50 USEC EACH MS
	2A1A06J16C-03			
D2	2B1A8-G3	6-109		
D3	2B1A8-G2	6-109		TEST STORAGE AVAILABILITY
E2	2A1A06P05B-03			INIT. RNI 2 CYCLE FF
	1A4A06J14B-03			
	1B1B5-C2	2- 5		
E3	2A1A06P05B-04			
	1A4A06J14B-04			
	1B1B5-C3	2- 5		
F0	2B1A8-H3	6- 17	2B1A8-BL	NOT(CLOCK CONTROL) TO TIMING CHAIN ENABLE 4 READ OR WRITE REGISTER FILE
F2	2A1A06P06B-06			
	1A4A06J18B-05			
	1C1B5-F3	2- 45		
F3	2A1A06P06B-05			
	1A4A06J18B-06			
	1C1B5-F2	2- 45		
G0	2B1A6-G5	6- 13		NOT(CLOCK CONTROL) TO D4 CONT REQUEST BC PULSE
G2	2A1A06P05B-05			
	1A4A06J14B-05			
	1B1A4-V2	2- 1		
G3	2A1A06P05B-06			
	1A4A06J14B-06			
	1B1A4-V3	2- 1		
H0	2A1A06J16D-09			SWITCH, WRITE STORAGE OR RF WRITE STORAGE SWITCH ON KYBD
H1	2B1A8-M2	6- 17		SET FUNCTION READY FF
H2	2B1A9-Q0	6- 23		EARLY FCN XLTN OF 77
H3	2B1B1-N0	6- 9		FUNCTIONS STABLE
I0	2A2A04J02N-03			CLOCK ON FROM MAINT. PANEL SW.
I2	2B1A8-B2	6-109		
I3	2B1A8-B3	6-109		FCN CODE=XX51 TO CLR CHAN XLTN
J0	2B1B9-B3	6- 27		TYPE IN XLTN TO TWR BFR
J2	2B1B8-B2	6-111		
J3	2B1B8-B3	6-111		(F BIT 09)(NOT F BIT 10)
K2	2B1B1-A3	6- 9		NOT(CLR FUNCTION READY FF)
K3	2B1A9-Q0	6- 23		NOT(BLOCK F XLTN BIT 17)
L0	2B1B9-D2	6- 27		TYPE OUT XLTN TO TWR BFR
L2	2B1A9-Q3	6-101		
L3	2B1A9-Q2	6-101		FCN CODE = 77 AND STABLE
M0	2A1A06J15B-05			EXT TW PRIORITY REQ ON LOAD
	2A1A06J16B-05			
M1	2A1A06J15B-06			
	2A1A06J16B-06			
M2	2B1B6-A0	6- 15	2B1B6-AA	NORMAL PROGRAM CONTROL
M3	2B1B0-V1	6- 7	2B1B0-AW	PROG REQUEST TO BC PRIORITY
N0	2B1B0-V0	6- 7	2B1B0-AV	TWR BFR REQUEST TO BC PRI. 3
N1	2B1B9-Q0	6- 27		NOT(D4 TO TW 0 REG CLR/SET)
N2	2B1A6-P1	6- 13		NOT (PROG CONT) EN PROG XLTN
N3	2B1B6-U1	6- 15		NOT(BC REPLY TO MN CONT ON 77,51)
U0	2B1B7-H3	6- 3		T265 - TO TWR BFR CONTROLS
U1	2B1A7-N2	6- 1		T160 - SET TWR DATA EN
U2	2B1A7-S0	6- 5		RESCAN TO BC PRIORITY 1 AND 4
U3	2B1A0-S1	6- 5	2B1A0-AQ	INTERNAL OPR REQ TO BC PRI. 4
P0	2B1B7-T2	6- 3		NOT(T268)- CLR TWR DATA ENABLE
P1	2B1B9-K3	6- 27		TYPE BUSY TO TWR BFR
P3	2B1A6-N0	6- 13		NOT (S/M REQ) TO INT REQ FAN-IN
Q0	2B1A7-U3	6- 1		NOT(T163) TO CLR TWR LOCKOUT
Q1	2B1A1-T3	6- 25		TWR CONTROL XLTN TO TWR BFR
Q3	2B1A0-N0	6- 5		NOT(SPECIAL SCAN BC PRIO 4)
R0	2B1B6-F3	6- 15	2B1B6-BL	NOT(TYPE OUT BFR CYCLE)
R1	2B1A6-Q3	6- 13		NOT(SEARCH COMPLETE - ADDRESS)
R3	2B1A8-P2	6- 17		NOT(T157) - CLR RESCAN F/F
S0	2B1B9-J2	6- 27		NOT(CLEAR TYPEOUT FF)
S1	2B1B9-C2	6- 27		NOT(TYPE IN) XLTN TO TWR BFR
S3	2B1A8-K1	6- 17		SET RESCAN F/F
T0	2B1B9-F3	6- 27		NOT(CLEAR TYPE-IN FF)
T1	2B1B9-C3	6- 27		NOT(TYPE OUT) XLTN TO TWR BFR
T3	2B1B1-B0	6- 9		NOT(CLEAR PRIORITY LOGIC)
U0	2A1B4-C2	6- 57		ADDR COMPARE TO SEARCH/TYPE
U1	2A1B4-C3	6- 57		
U2	2B1B0-Q0	6- 7		NOT(PROGRAM LOCKOUT) TO FANOUT
U3	2B1B0-N0	6- 7		NOT(SPECIAL SCAN BC PRIO 3)
V0	2B1A9-U3	6-101		STOP CLOCK ON PRIORITY PAUSE
V1	2B1A9-U2	6-101		
V2	2B1B0-S0	6- 7		RESCAN TO BC PRIORITY 2 AND 3
V3	2B1A9-C3	6- 23		PROGRAM LOCKOUT TO I/O ACT. TRANSLATION
W0	2B1B7-J0	6- 3		T155 - TO CLOCK/TW/PROG CONT
W1	2B1B9-F0	6- 27		TYPE. CONTROL TO TYPE. RCVR
W2	2A1A06J15C-02			
	2A1A06J16C-02			TW DATA READY SIGNAL FROM BC
W3	2A1A06J15C-01			
	2A1A06J16C-01			TW CONTROL BUSY
X0	2A1A06J15B-03			
	2A1A06J16B-03			
X1	2A1A06J15B-04			
	2A1A06J16B-04			
X2	2B1A1-L1	6- 25		NOT(PROG MODE TO BC PRIO XLTN)
X3	2B1A9-T0	6- 23		NOT(BLOCK F XLTNS OF 7X)



PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1B5-Q0	6- 21	2B1B5-AX	NOT(LEFT SHIFT D4 CHAR MODE)
A1	2B1B5-R0	6- 21	2B1B5-AY	RIGHT SHIFT D4 1 CHAR POS
B0	2B1B5-S0	6- 21	2B1B5-AZ	NOT(BLOCK XFER TO D4 CHAR 2)
B1	2B1A5-P2	6- 19		LEFT SHIFT D4 CHAR MODE
B2	2B1B4-P0	6- 29		NOT(SEARCH DATA) TO D4 BIT 18
B3	2B1B7-P3	6- 3		NOT(T267) = CLR SEARCH DATA
C0	2B1B5-T0	6- 21		BLOCK XFER TO D4 CHAR 0/1
C1	2B1A5-T0	6- 19		BLOCK XFER TO D4 CHAR 2
C2	2B1A5-Q2	6- 19		NOT(RIGHT SHIFT D4 1 CHAR POS)
C3	2B1A7-H2	6- 1		T155 TO ACT. AND SEARCH FFS
D0	2B1A5-R0	6- 19	2B1A5-AY	RIGHT SHIFT D4 2 CHAR POS
D1	2B1A5-S0	6- 19	2B1A5-AZ	NOT(BLOCK XFER TO D4 CHAR 0/1)
D2	2B1A1-T2	6- 25		S/M CONTROL XLTN TO S/M BFR
D3	2B1A7-Q0	6- 1		T158 CLR/SET D4 CONT - S/M CONTROL
E0	2B1B5-P2	6- 21		LEFT SHIFT D4 CHAR + BYTE
E1	2B1B5-Q2	6- 21		NOT(RIGHT SHIFT D4 2 CHAR POS)
E2	2B1B3-P0	6- 31		NOT(SEARCH DATA) TO D4 BIT 19
E3	2B1B2-P0	6- 33		NOT(SEARCH DATA) TO D4 BIT 20
F0	2B2A5-V2	5- 73		
F1	2B2A5-V3	5- 73		LINK D0 AND D4 TO PAGE FILE
F2	2A1B6-S2	6- 43		
F3	2A1B6-S3	6- 43		Z UPPER 7 = ZERO TO MOVE CONT
G0	2B1B8-G0	6- 11		NOT(CLOCK CONTROL) TO D4 CONT
G1	2B1A5-Q0	6- 19	2B1A5-AX	NOT(LEFT SHIFT D4 CHAR + BYTE)
G2	2B0A9-V0	6-101		CLEAR SEARCH/MOVE CONTROLS
G3	2B0A9-V1	6-101		
H0	2A1B4-S0	6- 57		STRIP/DUPLICATE BYTE
H1	2A1B4-S1	6- 57		
H2	2B1B1-R2	6- 9		F=71•72 - ENABLE ACTIVATE S/M
H3	2B1A9-B1	6- 23		FCN CODE = 73 THRU 76 TO ACT. FF
I0	2A1B4-Q1	6- 57		STRIP/DUPLICATE CHAR.
I1	2A1B4-Q0	6- 57		
I2	2B1B6-H3	6- 15		SEARCH CONTROL ENABLE MCS READ
I3	2B1A9-N1	6- 23		S/M INTERRUPT ON COMPLETE EN
J0	2A1B4-T0	6- 57		RIGHT SHIFT 2 TO D4 XLTN FF
J1	2A1B4-T1	6- 57		
J2	2B1B1-A0	6- 9		F=71 - ACTIVATE SEARCH
J3	2B1A1-D3	6- 25		MOVE MODE TO S/M PRIO XLTN
K0	2A1B4-R1	6- 57		RIGHT SHIFT 1 TO D4 XLTN FF
K1	2A1B4-R0	6- 57		
K2	2A1B6-M3	6- 43		
K3	2A1B6-M2	6- 43		CONSECUTIVE MOVE CYCLE
L0	2B1A9-R3	6- 23		D0 TO Z REG ENABLE TO Z FAN IN
L1	2B1B1-Q2	6- 9		S/M BFR BUSY TO MN CONT TEST FAN-IN
L3	2B1B7-J2	6- 3		T266 - TEST SEARCH COMPL. XLTN
M0	2C0A2-G0	6-167		
M1	2C0A2-G1	6-167		ACT. I/O TO CHAN 4-7 FANOUT
M2	2B1B6-F2	6- 15	2B1B6-BF	NOT(MOVE CONTROL - WRITE MCS)
M3	2B1B7-J1	6- 3		NOT (T155) - TO S/M BFR CONT
N0	2B1B8-P3	6- 11		NOT (S/M REQ) TO INT REQ FAN-IN
N1	2B1B0-S1	6- 7	2B1B0-AQ	S/M REQUEST TO BC PRIORITY 3
N2	2A1B6-E2	6- 43		NON-CONSECUTIVE MOVE CYCLE
N3	2A1B6-E3	6- 43		
O0	2B1A9-I3	6- 23		NOT(PROG CONTROL) EN. CHL XLTN
O1	2B1B1-W2	6- 9		PROG CONT EN - CONN + FCN XLTN
O2	2B0A7-G3	6-117		
O3	2B0A7-G2	6-117		SET S/M INTERRUPT ON COMPL
P0	2B1B6-D0	6- 15		PROG CONTROL ENABLE 7X XLTN
P1	2B1B8-N2	6- 11		NOT (PROG CONT) EN PROG XLTN
P2	2B1B6-E3	6- 15		MOVE CONTROL TO READ MCS XLTN
Q0	2B1A4-P0	6- 35		NOT(SEARCH DATA) TO D4 BIT 21
Q1	2B1A1-P2	6- 25		PROGRAM CONT XLTN TO FAN OUT
Q2	2B1A1-L0	6- 25		NOT(SEARCH FIND)
Q3	2B1B8-R1	6- 11		NOT(SEARCH COMPLETE - ADDRESS)
R0	2A1B7-H0	6- 41		D0 TO Z REG ENABLE TO FAN OUT
R1	2A1B7-H1	6- 41		
R3	2B1A7-V2	6- 1		NOT (T162) - CLR D TO Z/BLINK
S0	2A0B2-G1	6-131		ACT. I/O TO CHAN 0-3 FANOUT
S1	2A0B2-G0	6-131		
T0	2B0A5-Q1	6-123		
T1	2B0A5-Q0	6-123		S/M BFR BUSY TO STATUS FAN-IN
U0	2B1A8-B3	6- 17	2B1A8-BA	F ADDRESS REGISTER BUSY
U1	2B1A5-J0	6- 19		
U2	2B1B1-O1	6- 9		T152 - TEST MOVE COMPLETE
U3	2B1A1-J2	6- 25		MOVE FINAL BC PRIORITY
V0	2B1B4-G0	6- 29		NOT (D0 BIT 18) TO SUPPRESS A/D XLTN
V1	2B1A9-K0	6- 23		F= 73•75 TO SUPPR A/D XLTN
V2	2B1B1-G1	6- 9		NOT (CLEAR SEARCH/MOVE CONT)
V3	2B1B6-F0	6- 15		NOT(CLEAR BLINK FF)
W0	2B1B5-J0	6- 21		ACT. SUPPR A/D - CHAN 4-7
W1	2B1A3-P0	6- 37		NOT(SEARCH DATA) TO D4 BIT 22
W2	2B1A2-P0	6- 39		NOT(SEARCH DATA) TO D4 BIT 23
W3	2B1A7-B1	6- 1		I/O WITH A XLTN
X0	2A1A4-U0	6- 59		
X1	2A1A4-U1	6- 59		S REG BUSY TO D4 XLTN
X2	2B1B1-V0	6- 9		T153 - TEST NC MOVE/D TO Z EN
X3	2B1B7-T1	6- 3		T156 - CLR/SET D4 STRIP CONT.

CONTROL DATA
DEVELOPMENT DIVISION

D4 I/Ø AND SRCH / MOVE CONT

LOC: 2B1A6 PART NO. 185458 SER. 000

PRODUCT

SIZE C | DRAWING NO. 60181000 | REV. E

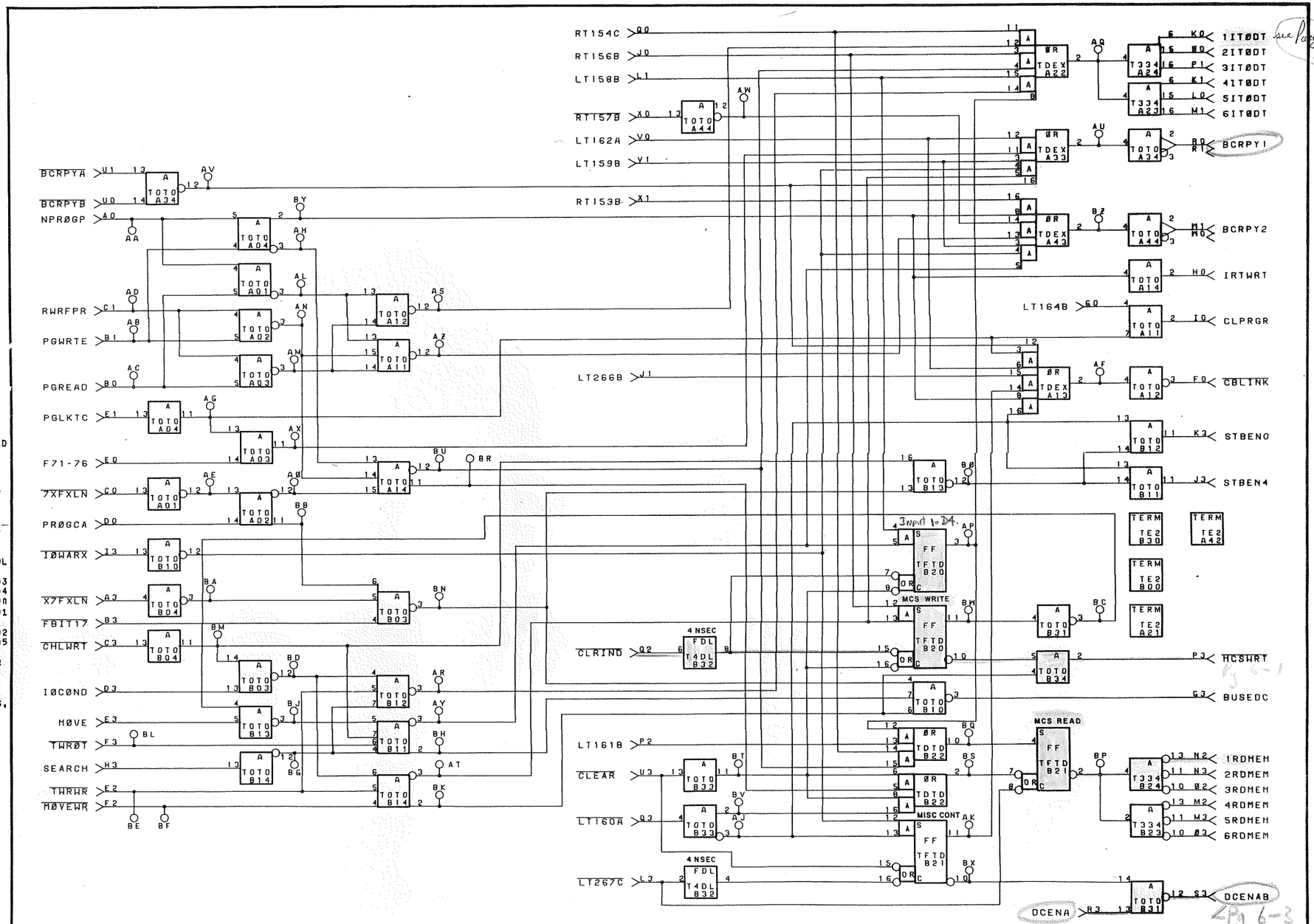
SHEET | PAGE 6-13

197

See page 24 of Block Control

117ϕTDT drug page 6-16.

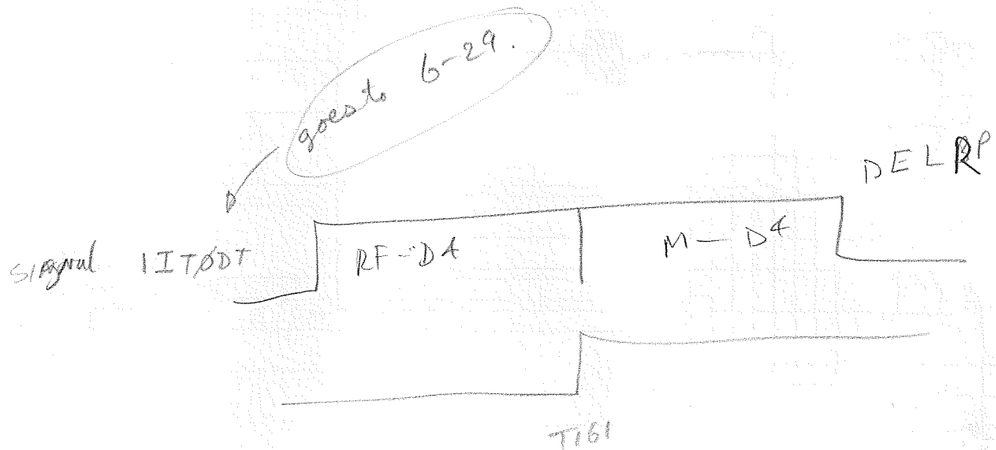
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1B8-M2	6- 11	2B1B6-AA	NORMAL PROGRAM CONTROL
A3	2B1A9-L1	6- 23		NOT(F=X7) TO MISC CONTROL
B0	2B1A9-U0	6- 23	2B1B6-AC	PROGRAM CONTROL RF READ
B1	2B1A9-T1	6- 23	2B1B6-AB	PROGRAM CONTROL RF WRITE
B3	2B1A9-N0	6- 23		NOT(F BIT 17)TO MISC CONT
C0	2B1A9-Q1	6- 23		NOT(FCN CODE=7X) TO MISC CONT
C1	2B1B8-A3	6- 11	2B1B6-AD	READ/WRITE REGISTER FILE CONT
C3	2B1A7-H3	6- 1		NOT(CHL WRITE XLTN)
D0	2B1A6-P0	6- 13		PROG CONTROL ENABLE 7X XLTN
D3	2B1A0-R1	6- 5		I/O CONTROL = EN I/O R/W XLTN
E0	2B1A9-D2	6- 23		F= (71 THRU 76)(NOT INA)
E1	2B1A9-D3	6- 23		PROGRAM LOCKOUT TO MISC CONT
E2	2B1B9-E0	6- 27	2B1B6-BE	NOT(TYPE CONTROL/WRITE MCS)
E3	2B1A6-P2	6- 13		MOVE CONTROL TO READ MCS XLTN
F0	2B1A6-V3	6- 13		NOT(CLEAR BLINK FF)
F2	2B1A6-M2	6- 13	2B1B6-BF	NOT(MOVE CONTROL = WRITE MCS)
F3	2B1B8-R0	6- 11	2B1B6-BL	NOT(TYPE OUT BFR CYCLE)
G0	2B1A7-W0	6- 1		T164 TO CLR PRG REQ XLTN
G3	2B1A8-J3	6- 17	2B1A8-BP	DATA BUS REQUIRED
H0	2B1A8-C3	6- 17	2B1A8-RD	IRT WRITE TO MAINT MODE TEST
H3	2B1A6-I2	6- 13		SEARCH CONTROL ENABLE MCS READ
I0	2B1B8-B2	6- 11		CLEAR PROGRAM REQUESTS
I3	2B1A7-A0	6- 1		NOT (I/O WITH A XLTN)
J0	2B1B7-U1	6- 3		T156 = TO INPUT TO D4 XLTN
J1	2B1B7-K2	6- 3		T266 = TO CLR BLINK XLTN
J3	2B1B5-M1	6- 21		STORE BUS TO 0 ENABLE CHL 4-7
K0	2B1B4-01	6- 29	2B1B4-AQ	INPUT TO D4 TIMING = BIT 00
K1	2B1A4-01	6- 35	2B1A4-AQ	INPUT TO D4 TIMING = BIT 03
K3	2B1A5-M1	6- 19		STORE BUS TO 0 ENABLE CHL 0-3
L0	2B1A3-01	6- 37	2B1A3-AQ	INPUT TO D4 TIMING = BIT 04
L1	2B1A7-M1	6- 1		T158 TO INPUT TO D4 XLTN
L3	2B1B7-N3	6- 3		NOT(T267) = CLEAR MISC CONTROL
M1	2B1A2-01	6- 39	2B1A2-AQ	INPUT TO D4 TIMING = BIT 05
M2	2B1A4-P1	6- 35	2B1A4-AR	ENABLE D0 + MCS TO D4 = BIT 03
M3	2B1A3-P1	6- 37	2B1A3-AR	ENABLE D0 + MCS TO D4 = BIT 04
N2	2B1B4-P1	6- 29	2B1B4-AR	ENABLE D0 + MCS TO D4 = BIT 00
N3	2B1B3-P1	6- 31	2B1B3-AR	ENABLE D0 + MCS TO D4 = BIT 01
O0	2B1B3-01	6- 31	2B1B3-AQ	INPUT TO D4 TIMING = BIT 01
O2	2B1B2-P1	6- 33	2B1B2-AR	ENABLE D0 + MCS TO D4 = BIT 02
O3	2B1A2-P1	6- 39	2B1A2-AR	ENABLE D0 + MCS TO D4 = BIT 05
P1	2B1B2-01	6- 33	2B1B2-AQ	INPUT TO D4 TIMING = BIT 02
P2	2B1A7-Q0	6- 1		T161 TEST MAINT MODE RF ERROR
P3	2B1A7-A3	6- 1	2B1A7-BA	NOT(MCS WRITE) TO FAN OUT
Q0	2B1B7-C3	6- 3		T154 TO INPUT TO D4 XLTN
Q2	2B1A8-B2	6- 17		NOT(CLEAR INPUT TO D4 FF)
Q3	2B1A7-T2	6- 1		NOT(T160)= CLR+SET MISC CONTS,
R0	2A1A06P05E-01			BC REPLY 1 TO MN CONT
	1A4A06J14E-01			
	1B0B1-J2	2- 9		
R1	2A1A06P05E-02			
	1A4A06J14E-02			
	1B0B1-J3	2- 9		
R3	2B1B1-02	6- 9		NOT(DATA TIMING CHAIN EN ON CONN + FCN)
S3	2B1B7-B2	6- 3	2B1B7-BA	DATA TIMING CHAIN ENABLE FOR CONN + FUNC + INA + OTA
U0	2B1B1-R3	6- 9		NOT(BC REPLY TO MN CONT ON CONN + FCN)
U1	2B1B8-N3	6- 11		NOT(BC REPLY TO MN CONT ON 77,51)
U3	2B1A8-I0	6- 17		NOT(CLEAR) TO MISC CONTROLS
V0	2B1A7-R2	6- 1		T162 TO BC REPLY TO MAIN CONTROL XLTN
V1	2B1A7-K3	6- 1		T159 TO BC REPLY TO MAIN CONTROL XLTN
W0	2A1A06P05D-10			
	1A4A06J14D-10			
	1B0B4-P1	2- 7		
W1	2A1A06P05D-09			BC REPLY 2 TO MN CONT
	1A4A06J14D-09			
	1B0B4-P0	2- 7		
X0	2B1A8-Q2	6- 17		NOT T157 TO D4 CONTROL ENABLE
X1	2B1B1-U0	6- 9		T153 = TO BC REPLY TO MC XLTN



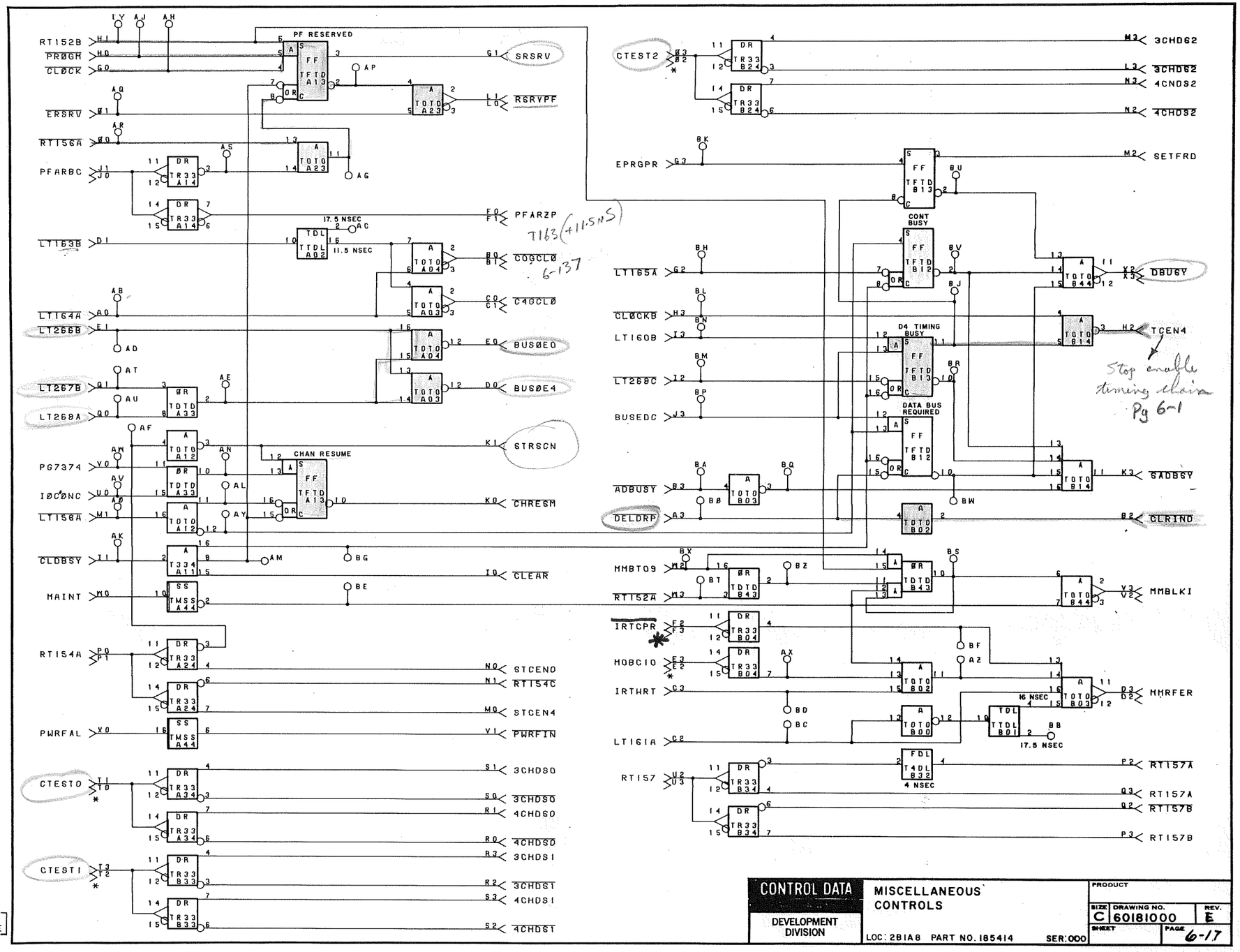
see Page 6-16

Pg 6-3

goes to 6-29.

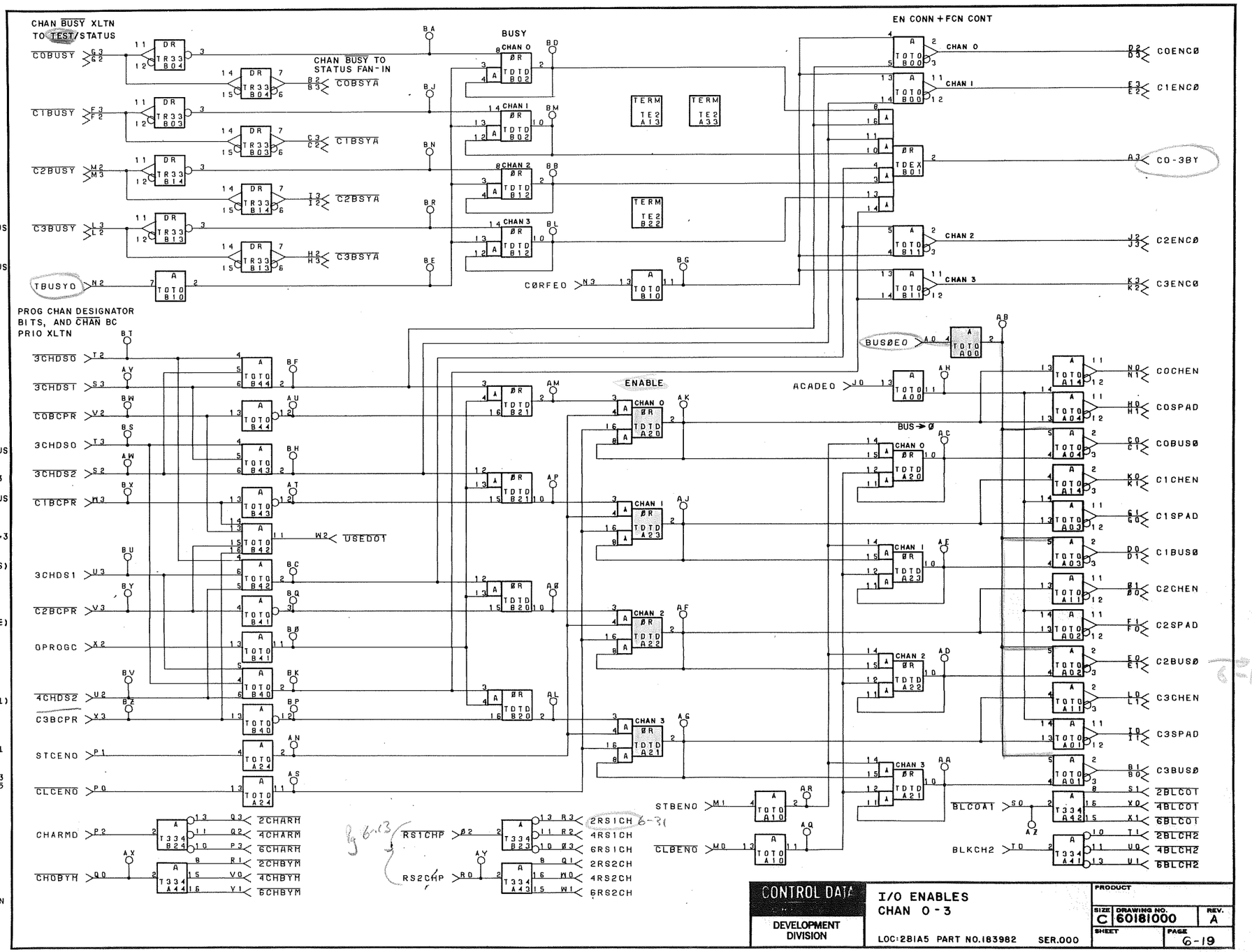


PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1A7-T4	6- 1	2B1A8-AB	NOT(T164) TO CLR 0 REG XLTN
A3	2B1B7-D3	6- 3	2B1A8-B0	NOT(DELAYED DATA REPLY)
B0	2A2A3-W3	6-137		
B1	2A2A3-W2	6-137		NOT CLR 0 REG TO CHAN 0-3
B2	2B1B6-Q2	6- 15		NOT(CLEAR INPUT TO D4 FF)
B3	2B1A6-U4	6- 13	2B1A8-BA	F ADDRESS REGISTER BUSY
C0	2C2B3-W3	6-173		
C1	2C2B3-W2	6-173		NOT CLR 0 REG TO CHL 4-7
C2	2B1A7-P1	6- 1	2B1A8-BC	T161 TO READ MCS XLTN
C3	2B1B6-H4	6- 15	2B1A8-BD	IRT WRITE TO MAINT MODE TEST
D0	2B1B5-A4	6- 21		BUS TO 0 REGISTER TIMING ENABLE - CHAN 4-7
D1	2B1A7-T3	6- 1		NOT(T163) TO CLR 0 REG XLTN
D2	2B1B7-P2	6-113		
D3	2B1B7-P3	6-113		MAINT MODE RF ERROR IRT WRITE
E0	2B1A5-A4	6- 19		BUS TO 0 REGISTER TIMING ENABLE - CHAN 0-3
E1	2B1B7-J3	6- 3	2B1A8-AD	NOT(T266) - TO BUS TO 0 XLTNS
E2	2A1A06P06A-08			
	1A4A06J18A-08			
	1C1B7-R1	3- 15		
E3	2A1A06P06A-07			NOT BIT 1_0 OF MAINT*REGISTER
	1A4A06J18A-07			
	1C1B7-R4	3- 15		
F0	2A1B6-I1	6- 43		PAGE FILE ADDRESS REPLY TO Z
F1	2A1B6-I4	6- 43		
F2	2A1B4-E3	6- 57		RF = Z - 24 BITS TO D4 XLTN
F3	2A1B4-E2	6- 57		
G0	2B1A1-I3	6- 25	2B1A8-AH	NOT(CLOCK FINAL BC PRIORITY)
G1	2B1B7-N4	6- 3	2B1B7-AS	PAGE FILE RESERVED BY BC
G2	2B1A7-W3	6- 1	2B1A8-BH	NOT(T165) TO CLR CONTROL BUSY
G3	2B1A1-P3	6- 25	2B1A8-BK	(PROG CONT)(T150) TO BUSY XLTN
H0	2B1A1-F2	6- 25	2B1A8-AJ	NOT(R/W RF + PROG) BC PRIORITY
H1	2B1B1-N1	6- 9	2B1A8-BY	T152 - SET PF RESERVE
H2	2B1A7-N1	6- 1	2B1A7-AG	TIMING CHAIN ENABLE 4
H3	2B1B8-F4	6- 11	2B1A8-BL	NOT(CLOCK CONTROL) TO TIMING CHAIN ENABLE 4
I0	2B1B6-U3	6- 15		NOT(CLEAR) TO MISC CONTROLS
I1	2B1B1-C1	6- 9	2B1A8-AK	NOT(CLEAR D4 BUSY)
I2	2B1B7-Q1	6- 3	2B1A8-BM	NOT(T268)- CLR D4 TIMING BUSY
I3	2B1A7-Q2	6- 1	2B1A8-BN	T160 - SET DATA TIMING BUSY
J0	2A2A6-X1	5- 1		
J1	2A2A6-X4	5- 1		PAGE FILE ADDR REPLY TO BC
J3	2B1B6-G3	6- 15	2B1A8-BP	DATA BUS REQUIRED
K0	2B1B0-L4	6- 7		NOT(CHANNEL RESUME) TO FAN OUT
K1	2B1B8-S3	6- 11		SET RESCAN F/F
K3	2B1B1-F4	6- 9		NOT(ADDRESS AND DATA REG BUSY)
L0	2A2A6-D1	5- 1		NOT BC RESERVE TO PAGE FILE
L1	2A2A6-D4	5- 1		
L3	2B1A5-S2	6- 19	2B1A5-AW	NOT(PROG CHAN DES - BIT 02)
M0	2B1B5-P1	6- 21		SET SELECTED CHL ENABLE 4-7
M1	2B1A7-N4	6- 1	2B1A8-AO	NOT(T158) CLR CHL RESUME
M2	2B1B8-H1	6- 11		SET FUNCTION READY FF
M3	2B1B5-S2	6- 21		PROG CHL DESIGNATOR BIT 02
N0	2B1A5-P1	6- 19		SET SELECTED CHL ENABLE 0-3
N1	2B1A1-Q1	6- 25		NOT(T154) CLR/SET SEARCH BFR
N2	2B1A5-U2	6- 19	2B1A5-BV	NOT(PROG CHAN DES - BIT 02)
N3	2B1B5-U2	6- 21		PROG CHL DESIGNATOR BIT 02
O0	2B1B7-T4	6- 3	2B1A8-AR	NOT(T156)- CLR PF RESERVE F/F
O1	2B1B7-L1	6- 3	2B1A8-AQ	NOT(EARLY PF RESERVE)
O2	2A1B8-Q3	6- 53		
O3	2A1B8-Q2	6- 53		NOT CHL SEL BIT 2 TEST BUSY 7X
P0	2A1B7-O2	6- 41		T154
P1	2A1B7-O3	6- 41		
P2	2B1B8-R3	6- 11		NOT(T157) - CLR RESCAN F/F
P3	2B1B1-W3	6- 9		T157 - SET CHL BUSY LOCKOUT
Q0	2B1B7-Q4	6- 3	2B1A8-AU	T268 - TO BUS TO 0 XLTNS
Q1	2B1B7-L3	6- 3	2B1A8-AT	NOT(T267) - TO BUS TO 0 XLTNS
Q2	2B1B6-X4	6- 15		NOT T157 TO D4 CONTROL ENABLE
Q3	2B1A7-I4	6- 1	2B1A7-AF	T157 - INPUT TO T158 DELAY
R0	2B1B5-T2	6- 21	2B1B5-BT	NOT(PROG CHAN DES - BIT 00)
R1	2B1B5-T3	6- 21		PROG CHL DESIGNATOR BIT 00
R2	2B1A5-S3	6- 19	2B1A5-AV	NOT(PROG CHAN DES - BIT 01)
R3	2B1A5-U3	6- 19		PROG CHL DESIGNATOR BIT 01
S0	2B1A5-T2	6- 19	2B1A5-BT	NOT(PROG CHAN DES - BIT 00)
S1	2B1A5-T3	6- 19		PROG CHL DESIGNATOR BIT 00
S2	2B1B5-S3	6- 21	2B1B5-AV	NOT(PROG CHAN DES - BIT 01)
S3	2B1B5-U3	6- 21		PROG CHL DESIGNATOR BIT 01
T0	2A1B8-J3	6- 53		
T1	2A1B8-J2	6- 53		NOT CHL SEL BIT 0 TEST BUSY 7X
T2	2A1B8-N2	6- 53		
T3	2A1B8-N3	6- 53		NOT CHL SEL BIT 1 TEST BUSY 7X
U0	2B1A0-R4	6- 5	2B1A8-AV	I/O CONTROL - EN CHAN RESUME
U2	2A1B7-X3	6- 41		T157
U3	2A1B7-X2	6- 41		
V0	2B1A9-G2	6- 23	2B1A8-AW	CHAN RESUME EN=(PROG)(73 + 74)
V1	2B1B7-F4	6- 3	2B1B7-AH	NOT(POWER FAILURE INTERRUPT)
V2	2A1B6-D2	6- 43		
V3	2A1B6-D3	6- 43		MAINT MODE BLOCK RF INCREMENT
W0	2A2A04J02P-03			
W2	2B1A7-B4	6- 1	2B1A8-BX	MAINT MODE REG BIT 09
W3	2B1B1-P4	6- 9	2B1A8-BT	NOT (T152) - RESYNC MAINT M REGISTER - BIT 09
X0	2A1A06P06-10 TWO WIRES IN 2A2A01TB2-4 TAPER PIN			POWER-FAIL INTERRUPT LINE SEE POWER WIRING DIAGRAM ON P. 8-7 FOR EXTENSION OF THIS LINE
X2	2A1B6-C4	6- 43		
X3	2A1B6-C1	6- 43		NOT BC DATA REG BUSY



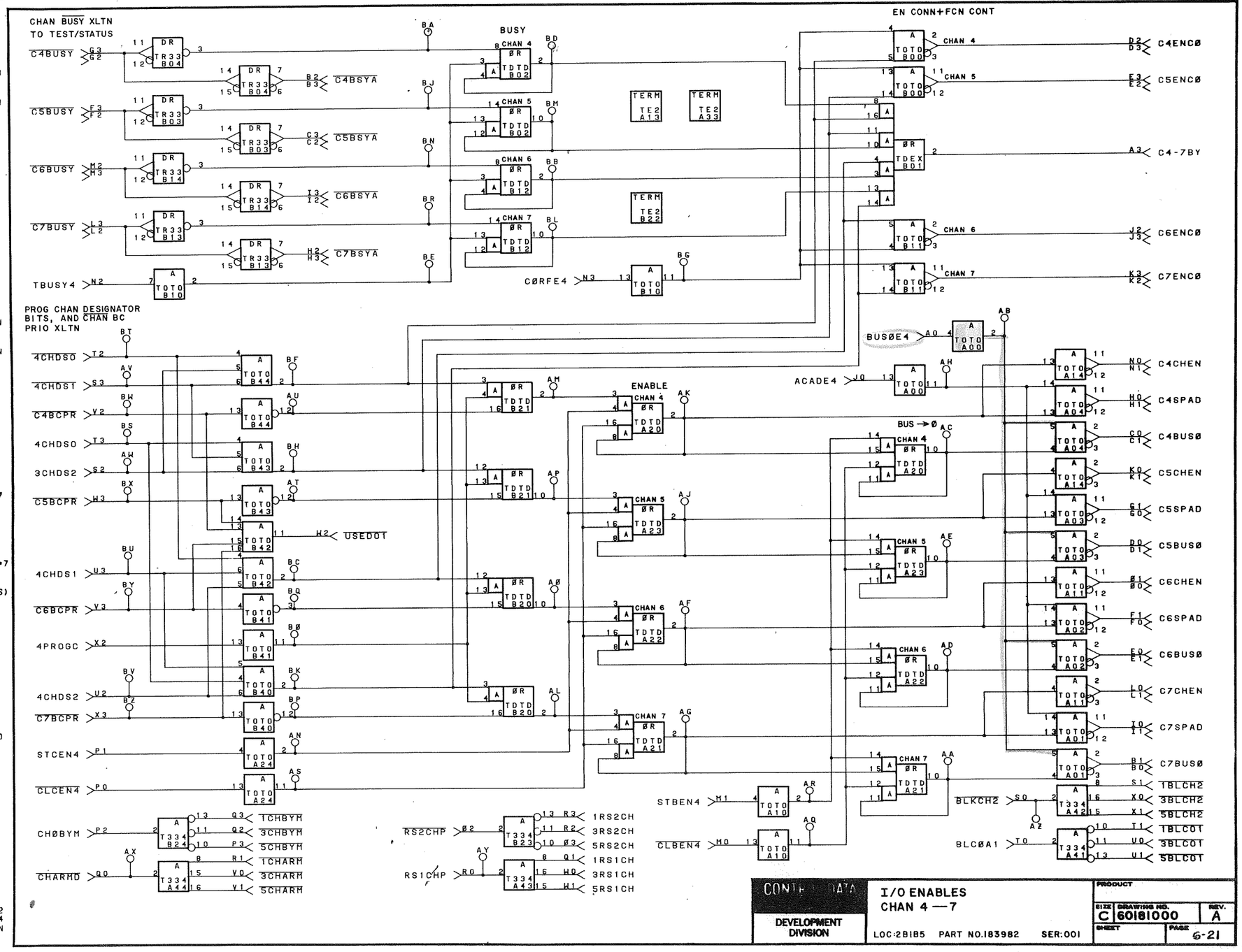
CONTROL DATA	MISCELLANEOUS CONTROLS	PRODUCT
DEVELOPMENT DIVISION	LOC: 2B1A8 PART NO. 185414 SER: 000	SIZE C DRAWING NO. 60181000 REV. E
		SHEET PAGE 6-17

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1A8-E0	6- 17		BUS TO 0 REGISTER TIMING
				ENABLE = CHAN 0-3
A3	2B1B1-V3	6- 9		SELECTED CHANNEL (0-3) BUSY
B0	2A0A2-V3	6-139		
B1	2A0A2-V2	6-139		EN CHAN 3 BUS TO 0 XFER/XMIT
B2	2B0A6-E3	6-121		
B3	2B0A6-E2	6-121		NOT CHAN 0 BUSY TO STATUS FI
C0	2A0A7-V2	6-133		EN CHAN 0 BUS TO 0 XFER/XMIT
C1	2A0A7-V3	6-133		
C2	2B0A5-E2	6-123		NOT CHAN 1 BUSY TO STATUS FI
C3	2B0A5-E3	6-123		
D0	2A0A6-V2	6-135		EN CHAN 1 BUS TO 0 XFER/XMIT
D1	2A0A6-V3	6-135		
D2	2A0B7-H2	6-125		
D3	2A0B7-H3	6-125		
E0	2A0A3-V2	6-137		EN CHAN 2 BUS TO 0 XFER/XMIT
E1	2A0A3-V3	6-137		
E2	2A0B6-H3	6-127		
E3	2A0B6-H2	6-127		
F0	2B0B4-E0	6-105		
F1	2B0B4-E1	6-105		ACT, CHAN 2 SUPPRESS EXT A/D
F2	2A0B6-D2	6-127		NOT CHAN 1 BUSY TO TEST/STATUS
F3	2A0B6-D3	6-127		
G0	2B0A4-Q1	6-103		
G1	2B0A4-Q0	6-103		ACT, CHAN 1 SUPPRESS EXT A/D
G2	2A0B7-D2	6-125		NOT CHAN 0 BUSY TO TEST/STATUS
G3	2A0B7-D3	6-125		
H0	2B0A4-E1	6-103		ACT, CHAN 0 SUPPRESS EXT A/D
H1	2B0A4-E0	6-103		
H2	2B0A5-D2	6-123		
H3	2B0A5-D3	6-123		NOT CHAN 3 BUSY TO STATUS FI
I0	2B0B4-Q0	6-105		ACT, CHAN 3 SUPPRESS EXT A/D
I1	2B0B4-Q1	6-105		
I2	2B0A6-D3	6-121		NOT CHAN 2 BUSY TO STATUS FI
I3	2B0A6-D2	6-121		
J0	2B1A6-U1	6- 13		ACT, SUPPR A/D = CHAN 0-3
J2	2A0B3-H2	6-129		
J3	2A0B3-H3	6-129		
K0	2A0A6-I1	6-135		EN CHAN 1 TO COMMON CONTROL
K1	2A0A6-I0	6-135		
K2	2A0B2-H3	6-131		
K3	2A0B2-H2	6-131		
L0	2A0A2-I1	6-139		EN CHAN 3 TO COMMON CONTROL
L1	2A0A2-I0	6-139		
L2	2A0B2-D2	6-131		NOT CHAN 3 BUSY TO TEST/STATUS
L3	2A0B2-D3	6-131		
M0	2B1B7-R0	6- 3		NOT(CLR BUS TO 0 REG EN 0-3)
M1	2B1B6-K3	6- 15		STORE BUS TO 0 ENABLE CHL 0-3
M2	2A0B3-D3	6-129		
M3	2A0B3-D2	6-129		NOT CHAN 2 BUSY TO TEST/STATUS
N0	2A0A7-I1	6-133		EN CHAN 0 TO COMMON CONTROL
N1	2A0A7-I0	6-133		
N2	2B1B1-D3	6- 9		TEST CHL 0-3 BUSY
N3	2B1B1-L2	6- 9		CONN + FCN TO CONTROL XLTN 0-3
O0	2A0A3-I0	6-137		
O1	2A0A3-I1	6-137		EN CHAN 2 TO COMMON CONTROL
O2	2B1A6-C2	6- 13		NOT(RIGHT SHIFT D4 1 CHAR POS)
O3	2B1A2-O0	6- 39		RS 1 CHAR POS. TO D4 BIT 05
P0	2B1B7-C0	6- 3		NOT(CLR CHL ENABLES 0-3)
P1	2B1A8-N0	6- 17		SET SELECTED CHL ENABLE 0-3
P2	2B1A6-B1	6- 13		LEFT SHIFT D4 CHAR MODE
P3	2B1A2-J3	6- 39	2B1A2-RJ	NOT(CHAR MODE) TO D4 BIT 05
Q0	2B1A6-G1	6- 13	2B1A5-AX	NOT(LEFT SHIFT D4 CHAR + BYTE)
Q1	2B1B3-G1	6- 31		RS 2 CHAR POS. TO D4 BIT 01
Q2	2B1A4-J3	6- 35	2B1A4-BJ	NOT(CHAR MODE) TO D4 BIT 03
Q3	2B1B3-J3	6- 31	2B1B3-BJ	NOT(CHAR MODE) TO D4 BIT 01
R0	2B1A6-D0	6- 13	2B1A5-AY	RIGHT SHIFT D4 2 CHAR POS
R1	2B1B3-Q2	6- 31	2B1B3-BN	NOT(CHAR+BYTE) TO D4 BIT 01
R2	2B1A4-O0	6- 35		RS 1 CHAR POS. TO D4 BIT 03
R3	2B1B3-O0	6- 31		RS 1 CHAR POS. TO D4 BIT 01
S0	2B1A6-D1	6- 13	2B1A5-AZ	NOT(BLOCK XFER TO D4 CHAR 0/1)
S1	2B1B3-I2	6- 31	2B1B3-AO	NOT(BLK 00/01) TO D4 BIT 01
S2	2B1A8-L3	6- 17	2B1A5-AW	NOT(PROG CHAN DES = BIT 02)
S3	2B1A8-R2	6- 17	2B1A5-AV	NOT(PROG CHAN DES = BIT 01)
T0	2B1A6-C1	6- 13		BLOCK XFER TO D4 CHAR 2
T1	2B1B3-A0	6- 31	2B1B3-AL	NOT(BLK CHAR 02) TO D4 BIT 01
T2	2B1A8-S0	6- 17	2B1A5-RT	NOT(PROG CHAN DES = BIT 00)
T3	2B1A8-S1	6- 17		PROG CHL DESIGNATOR BIT 00
U0	2B1A4-A0	6- 35	2B1A4-AL	NOT(BLK CHAR 02) TO D4 BIT 03
U1	2B1A2-A0	6- 39	2B1A2-AL	NOT(BLK CHAR 02) TO D4 BIT 05
U2	2B1A8-N2	6- 17	2B1A5-RV	NOT(PROG CHAN DES = BIT 02)
U3	2B1A8-R3	6- 17		PROG CHL DESIGNATOR BIT 01
V0	2B1A4-Q2	6- 35	2B1A4-RN	NOT(CHAR+BYTE) TO D4 BIT 03
V1	2B1A2-Q2	6- 39	2B1A2-RN	NOT(CHAR+BYTE) TO D4 BIT 05
V2	2B1A0-N2	6- 5	2B1A5-RW	NOT(CHL 0 BC PRIORITY XLTN)
V3	2B1A0-N3	6- 5	2B1A5-RY	NOT(CHL 2 BC PRIORITY XLTN)
W0	2B1A4-G1	6- 35		RS 2 CHAR POS. TO D4 BIT 03
W1	2B1A2-G1	6- 39		RS 2 CHAR POS. TO D4 BIT 05
W3	2B1A0-M2	6- 5	2B1A5-RX	NOT(CHL 1 BC PRIORITY XLTN)
X0	2B1A4-I2	6- 35	2B1A4-AO	NOT(BLK 00/01) TO D4 BIT 03
X1	2B1A2-I2	6- 39	2B1A2-AO	NOT(BLK 00/01) TO D4 BIT 05
X2	2B1A9-P1	6- 23		PROG CONT+ENABLE CHL 0-3 XLTN
X3	2B1A0-L3	6- 5	2B1A5-RZ	NOT(CHL 3 BC PRIORITY XLTN)



203

A0	2B1A8=D0	6= 17		BUS TO 0 REGISTER TIMING
				ENABLE = CHAN 4-7
A3	2B1R1=V2	6= 9		SELECTED CHANNEL (4-7) BUSY
B0	2C0R2=V3	6=175		
B1	2C0R2=V2	6=175		EN CHAN 7 BUS TO 0 XFER/XMIT
B2	2R0A6=V2	6=121		
B3	2R0A6=V3	6=121		NOT CHL 4 BUSY TO STAT FAN=IN
C0	2C0B7=V2	6=169		EN CHAN 4 BUS TO 0 XFER/XMIT
C1	2C0B7=V3	6=169		
C2	2R0A5=V3	6=123		NOT CHL 5 BUSY TO STAT FAN=IN
C3	2R0A5=V2	6=123		
D0	2C0B6=V2	6=171		EN CHAN 5 BUS TO 0 XFER/XMIT
D1	2C0B6=V3	6=171		
D2	2C0A7=H2	6=161		
D3	2C0A7=H3	6=161		
E0	2C0B3=V2	6=173		EN CHAN 6 BUS TO 0 XFER/XMIT
E1	2C0B3=V3	6=173		
E2	2C0A6=H3	6=163		
E3	2C0A6=H2	6=163		
F0	2R0B4=D2	6=105		
F1	2R0B4=D3	6=105		ACT, CHAN 6 SUPPR EXT A/D
F2	2C0A6=D2	6=163		NOT CHAN 5 BUSY XLTN TO TEST/STATUS
F3	2C0A6=D3	6=163		
G0	2B0A4=R3	6=103		
G1	2B0A4=R2	6=103		ACT, CHAN 5 SUPPR EXT A/D
G2	2C0A7=D2	6=161		NOT CHAN 4 BUSY XLTN TO TEST/STATUS
G3	2C0A7=D3	6=161		ACT, CHAN 4 SUPPR EXT A/D
H0	2R0A4=D3	6=103		
H1	2B0A4=D2	6=103		
H2	2R0A5=W1	6=123		NOT CHL 7 BUSY TO STAT FAN=IN
H3	2R0A5=W0	6=123		ACT, CHAN 7 SUPPR EXT A/D
I0	2B0B4=R2	6=105		
I1	2R0B4=R3	6=105		NOT CHL 6 BUSY TO STAT FAN=IN
I2	2B0A6=W0	6=121		
I3	2B0A6=W1	6=121		ACT, SUPPR A/D = CHAN 4-7
J0	2B1A6=W0	6= 13		
J2	2C0A3=H2	6=165		
J3	2C0A3=H3	6=165		EN CHAN 5 TO COMMON CONTROL
K0	2C0B6=I1	6=171		
K1	2C0B6=I0	6=171		
K2	2C0A2=H3	6=167		
K3	2C0A2=H2	6=167		EN CHAN 7 TO COMMON CONTROL
L0	2C0B2=I1	6=175		
L1	2C0B2=I0	6=175		NOT CHL 7 BUSY XLTN TO TEST/STATUS
L2	2C0A2=D2	6=167		
L3	2C0A2=D3	6=167		
M0	2R1B7=P1	6= 3		NOT(CLR BUS TO 0 REG EN 4-7)
M1	2R1R6=J3	6= 15		STORE BUS TO 0 ENABLE CHL 4-7
M2	2C0A3=D3	6=165		
M3	2C0A3=D2	6=165		NOT CHAN 6 BUSY XLTN TO TEST/STATUS
N0	2C0B7=I1	6=169		EN CHAN 4 TO COMMON CONTROL
N1	2C0B7=I0	6=169		
N2	2R1B1=B2	6= 9		TEST CHL 4-7 BUSY
N3	2R1B1=L3	6= 9		CONN + FCN TO CONTROL XLTN 4-7
O0	2C0B3=I0	6=173		
O1	2C0B3=I1	6=173		EN CHAN 6 TO COMMON CONTROL
O2	2B1A6=E1	6= 13		NOT(RIGHT SHIFT D4 2 CHAR POS)
O3	2R1A3=G1	6= 37		RS 2 CHAR POS, TO D4 BIT 04
P0	2R1B7=A0	6= 3		NOT(CLR CHL ENABLES 4-7)
P1	2B1A8=H0	6= 17		SET SELECTED CHL ENABLE 4-7
P2	2B1A6=E0	6= 13		LEFT SHIFT D4 CHAR + BYTE
P3	2R1A3=Q2	6= 37	2B1A3=RN	NOT(CHAR+BYTE TO D4 BIT 04
Q0	2B1A6=A0	6= 13	2B1B5=AX	NOT(LEFT SHIFT D4 CHAR MODE)
Q1	2R1B4=O0	6= 29		RS 1 CHAR POS, TO D4 BIT 00
Q2	2R1B2=Q2	6= 33	2B1B2=RN	NOT(CHAR+BYTE) TO D4 BIT 02
Q3	2R1B4=Q2	6= 29	2B1B4=RN	NOT(CHAR+BYTE) TO D4 BIT 00
R0	2R1A6=A3	6= 13	2B1B5=AY	RIGHT SHIFT D4 1 CHAR POS
R1	2R1B4=J3	6= 29	2B1B4=RJ	NOT(CHAR MODE) TO D4 BIT 00
R2	2R1B2=G1	6= 33		RS 2 CHAR POS, TO D4 BIT 02
R3	2R1B4=G1	6= 29		RS 2 CHAR POS, TO D4 BIT 00
S0	2R1A6=B0	6= 13	2B1B5=AZ	NOT(BLOCK XFER TO D4 CHAR 2)
S1	2R1B4=A0	6= 29	2B1B4=AL	NOT(BLK CHAR 02) TO D4 BIT 00
S2	2R1A8=M3	6= 17		PROG CHL DESIGNATOR BIT 02
S3	2R1A8=S2	6= 17	2B1B5=AV	NOT(PROG CHAN DES = BIT 01)
T0	2R1A6=C0	6= 13		BLOCK XFER TO D4 CHAR 0/1
T1	2R1B4=I2	6= 29	2B1B4=AO	NOT(BLK 00/01) TO D4 BIT 00
T2	2R1A8=R0	6= 17	2B1B5=RT	NOT(PROG CHAN DES = BIT 00)
T3	2R1A8=R1	6= 17		PROG CHL DESIGNATOR BIT 00
U0	2R1B2=I2	6= 33	2B1B2=AO	NOT(BLK 00/01) TO D4 BIT 02
U1	2R1A3=I2	6= 37	2B1A3=AO	NOT(BLK 00/01) TO D4 BIT 04
U2	2R1A8=N3	6= 17		PROG CHL DESIGNATOR BIT 02
U3	2R1A8=S3	6= 17		PROG CHL DESIGNATOR BIT 01
V0	2R1B2=J3	6= 33	2B1B2=RJ	NOT(CHAR MODE) TO D4 BIT 02
V1	2R1A3=J3	6= 37	2B1A3=RJ	NOT(CHAR MODE) TO D4 BIT 04
V2	2R1R0=N2	6= 7	2B1B5=RW	NOT(CHL 4 BC PRIORITY XLTN)
V3	2R1R0=N3	6= 7	2B1B5=RY	NOT(CHL 6 BC PRIORITY XLTN)
W0	2B1B2=O0	6= 33		RS 1 CHAR POS, TO D4 BIT 02
W1	2R1A3=O0	6= 37		RS 1 CHAR POS, TO D4 BIT 04
W3	2R1R0=M2	6= 7	2B1B5=RX	NOT (CHL 5 BC PRIORITY XLTN)
X0	2R1B2=A0	6= 33	2B1B2=AL	NOT(BLK CHAR 02) TO D4 BIT 02
X1	2R1A3=A0	6= 37	2B1A3=AL	NOT(BLK CHAR 02) TO D4 BIT 04
X2	2R1A9=P0	6= 23		PROG CONT=ENABLE CHL 4-7 XLTN
X3	2R1R0=L3	6= 7	2B1B5=RZ	NOT(CHL 7 BC PRIORITY XLTN)



CONTROL DATA
DEVELOPMENT DIVISION

I/O ENABLES
CHAN 4 — 7

LOC:2B1B5 PART NO.183982 SER:001

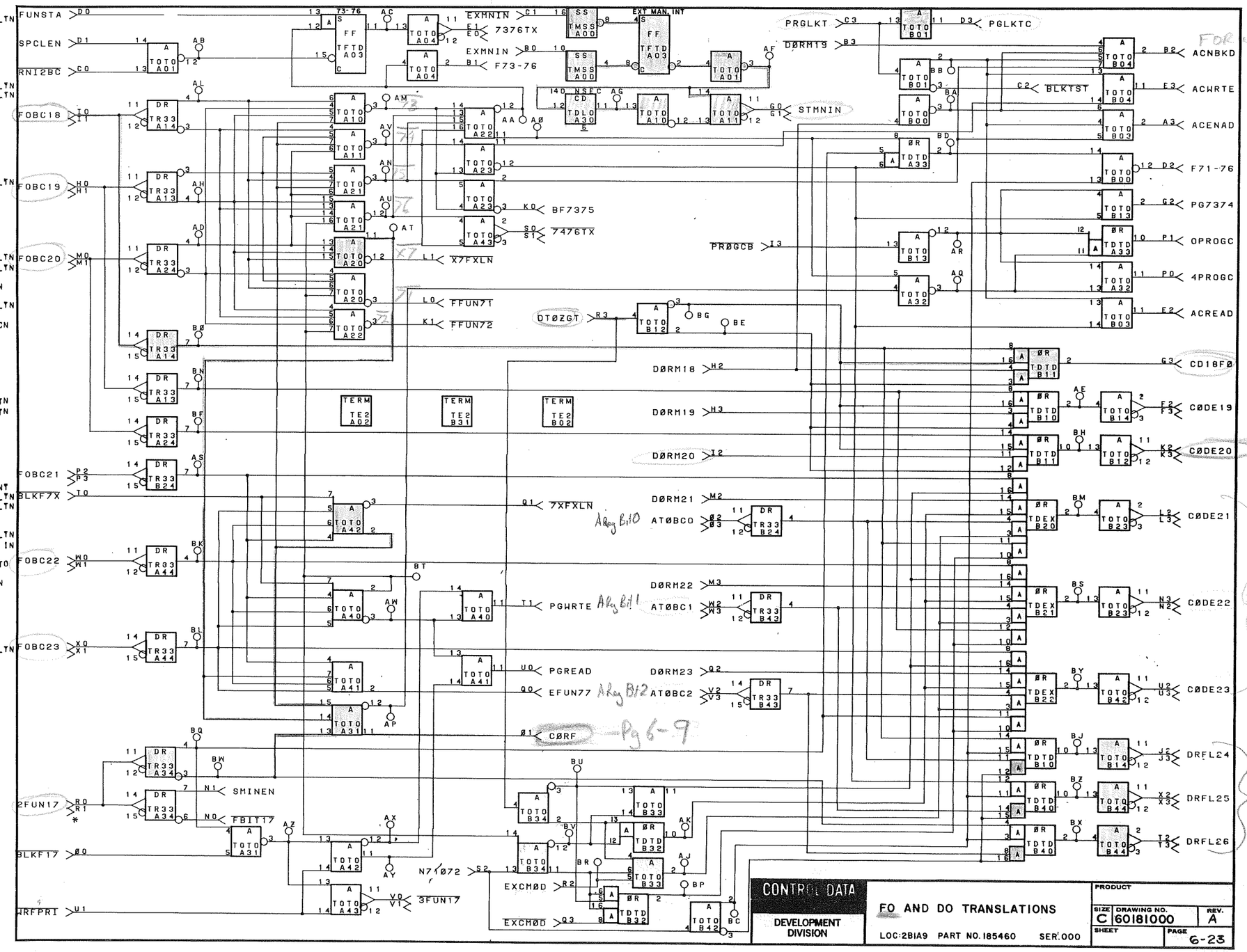
PRODUCT
SIZE C | DRAWING NO. 60181000 | REV. A
SHEET | PAGE 6-21

205

PIN	ORIGIN/ DEST,	PAGE	TEST POINT	SIGNAL DEFINITION.
A3	2B1B4-R2	6- 29	2B1B4-RV	ACT, I/O CHAN ASSY/DISASSY
B0	2A1A06J16E-07			CONSOLE MANUAL INTERRUPT SW
B1	2B1A6-H3	6- 13		FCN CODE = 73 THRU 76 TO ACT, FF
B2	2B1B3-R2	6- 31	2B1B3-RV	ACT, I/O FORWARD ASSY/DISASSY
B3	2B1B3-G0	6- 31		NOT(D0 BIT 19) TO FORWARD XLTN
C0	2B1B8-B3	6- 11		NOT(RNI 2) FROM MN CONT TO BC
C1	2A1A06J16E-08			NOT(CONSOLE MANUAL INT SW)
C2	2B1A7-Q3	6- 1	2B1A7-RQ	NOT(BLOCK CHAN TEST SIGNAL)
C3	2B1B8-V3	6- 11		PROGRAM LOCKOUT TO I/O ACT, TRANSLATION
D0	2B1B1-M1	6- 9		FUNCTIONS STABLE
D1	2B1B1-B3	6- 9		SPECIAL CLEAR OF TIMED XLTN
D2	2B1B6-E0	6- 15		F= (71 THRU 76)(NOT INA)
D3	2B1B6-E1	6- 15		PROGRAM LOCKOUT TO MISC CONT
E0	2A1B6-X1	6- 43		
E1	2A1B6-X0	6- 43		FCN CODE = 73 - 76 TIMED XLTN
E2	2B1A3-R2	6- 37	2B1A3-RV	ACT, I/O INPUT - I/O READ
E3	2B1A4-R2	6- 35	2B1A4-RV	ACT, I/O OUTPUT - I/O WRITE
F2	2A1B8-U3	6- 53		CODE 19 TO Z REG=D0+F0
F3	2A1B8-U2	6- 53		
G0	2B0A8-T1	6-109		SET MANUAL INTERRUPT
G1	2B0A8-T0	6-109		
G2	2B1A8-V0	6- 17	2B1A8-AW	CHAN RESUME EN=(PROG)(73 - 74)
G3	2B1A7-E3	6- 1	2B1A7-RE	
H0	2A1A06P05A-03			F0 REGISTER BIT 19
	1A4A06J14A-03			
	1B0A1-N0	2- 33		
H1	2A1A06P05A-04			
	1A4A06J14A-04			
	1B0A1-N1	2- 33		
H2	2B1B4-F1	6- 29		D0 BIT 18 TO Z REG FAN IN XLTN

EXT Manual Interrupt

H3	2B1B3=F1	6= 31		DO BIT 19 TO Z REG FAN IN XLTN
I0	2A1A06P05A=01			FO REGISTER BIT 18
	1A4A06J14A=01			
	1B0A1=E0	2= 33		
I1	2A1A06P05A=02			
	1A4A06J14A=02			
	1B0A1=E1	2= 33		
I2	2B1B2=F1	6= 33		DO BIT 20 TO Z REG FAN IN XLTN
I3	2B1A6=O0	6= 13		NOT(PROG CONTROL) EN; CHL XLTN
J2	2A1A3=H1	6= 61		DIGIT DRIVE 24 TO RF 00=37
J3	2A1A3=H0	6= 61		
K0	2B1A6=V1	6= 13		F= 73=75 TO SUPPR A/D XLTN
K1	2B1B1=X3	6= 9		NOT(FCN CODE=72)TO FANOUT
K2	2A1A8=G1	6= 55		CODE 20 TO Z REG=D0+F0
K3	2A1A8=G0	6= 55		
L0	2B1B1=X2	6= 9		NOT(FCN CODE=71)TO FANOUT
L1	2B1B6=A3	6= 15		NOT(F=X7) TO MISC CONTROL
L2	2A1A8=H1	6= 55		CODE 21 TO Z REG=D0+F0+A0+XLTN
L3	2A1A8=H0	6= 55		
M0	2A1A06P05A=05			FO REGISTER BIT 20
	1A4A06J14A=05			
	1B0A1=W1	2= 33		
M1	2A1A06P05A=06			
	1A4A06J14A=06			
	1B0A1=W0	2= 33		
M2	2B1A4=F1	6= 35		DO BIT 21 TO Z REG FAN IN XLTN
M3	2B1A3=F1	6= 37		DO BIT 22 TO Z REG FAN IN XLTN
N0	2B1B6=B3	6= 15		NOT(F BIT 17)TO MISC CONT
N1	2B1A6=I3	6= 13		S/M INTERRUPT ON COMPLETE EN
N2	2A1A8=E0	6= 55		
N3	2A1A8=E1	6= 55		CODE 22 TO Z REG=D0+F0+A0+XLTN
O0	2B1B8=K3	6= 11		NOT(BLOCK F XLTN BIT 17)
O1	2B1B1=O3	6= 9		CONN + FCN XLTN TO CONN + FCN CONTROL
				BIT 00 OF A
O2	2A1A06P06D=07			
	1A4A06J18D=07			
	1A1B6=O2	3= 51		
O3	2A1A06P06D=08			
	1A4A06J18D=08			
	1A1B6=O3	3= 51		
P0	2B1B5=X2	6= 21		PROG CONT=ENABLE CHL 4=7 XLTN
P1	2B1A5=X2	6= 19		PROG CONT=ENABLE CHL 0=3 XLTN
P2	2A1A06P05A=07			FO REGISTER BIT 21
	1A4A06J14A=07			
	1B0A0=E0	2= 35		
P3	2A1A06P05A=08			
	1A4A06J14A=08			
	1B0A0=E1	2= 35		
Q0	2B1B8=H2	6= 11		EARLY FCN XLTN OF 77
Q1	2B1B6=C0	6= 15		NOT(FCN CODE=7X) TO MISC CONT
Q2	2B1A2=F1	6= 39		DO BIT 23 TO Z REG FAN IN XLTN
Q3	2B1B0=C1	6= 7		NOT(EXEC MODE) TO CONTROL XLTN
R0	2B0A9=I0	6=101		NOT FO = BIT 17
R1	2B0A9=I1	6=101		
R2	2B1B0=A0	6= 7	2B1A9-BR	EXECUTIVE MODE TO CONTROL XLTN
R3	2R1A6=L0	6= 13		DO TO Z REG ENABLE TO Z FAN IN
S0	2A1B6=W1	6= 43		
S1	2A1B6=W0	6= 43		NOT FCN CODE=74+76=ADDRESS TO Z LS2
S2	2R1B1=S3	6= 9		NOT(F=71+72) TO Z REG FAN IN
T0	2R1B8=X3	6= 11		NOT(BLOCK F XLTNS OF 7X)
T1	2R1B6=B1	6= 15	2B1B6-AB	PROGRAM CONTROL RF WRITE
T2	2A1A2=M1	6= 67		DIGIT DRIVE 26 TO RF 00=37
T3	2A1A2=M0	6= 67		
U0	2B1B6=B0	6= 15	2B1B6-AC	PROGRAM CONTROL RF READ
U1	2R1B8=C2	6= 11		WRITE REGISTER FILE CONTROL
U2	2A1A8=F1	6= 55		CODE 23 TO Z REG=D0+F0+A0+XLTN
U3	2A1A8=F0	6= 55		
V0	2A1B8=V1	6= 53		
V1	2A1B8=V0	6= 53		NOT F BIT 17
V2	2A1A06P06E=01			BIT 02 OF A
	1A4A06J18E=01			
	1A1B6=T3	3= 51		
V3	2A1A06P06E=02			
	1A4A06J18E=02			
	1A1B6=T2	3= 51		
W0	2A1A06P05A=09			FO REGISTER BIT 22
	1A4A06J14A=09			
	1B0A0=N0	2= 35		
W1	2A1A06P05A=10			
	1A4A06J14A=10			
	1B0A0=N1	2= 35		
W2	2A1A06P06D=09			BIT 01 OF A
	1A4A06J18D=09			
	1A1B6=R2	3= 51		
W3	2A1A06P06D=10			
	1A4A06J18D=10			
	1A1B6=R3	3= 51		
X0	2A1A06P05B=01			FO REGISTER BIT 28
	1A4A06J14B=01			
	1R0A0=W1	2= 35		
X1	2A1A06P05B=02			
	1A4A06J14B=02			
	1R0A0=W0	2= 35		
X2	2A1A3=L1	6= 61		DIGIT DRIVE 25 TO RF 00=37
X3	2A1A3=L0	6= 61		



FOR LOAD 6-31

Reg Fl6 ax Bit 55

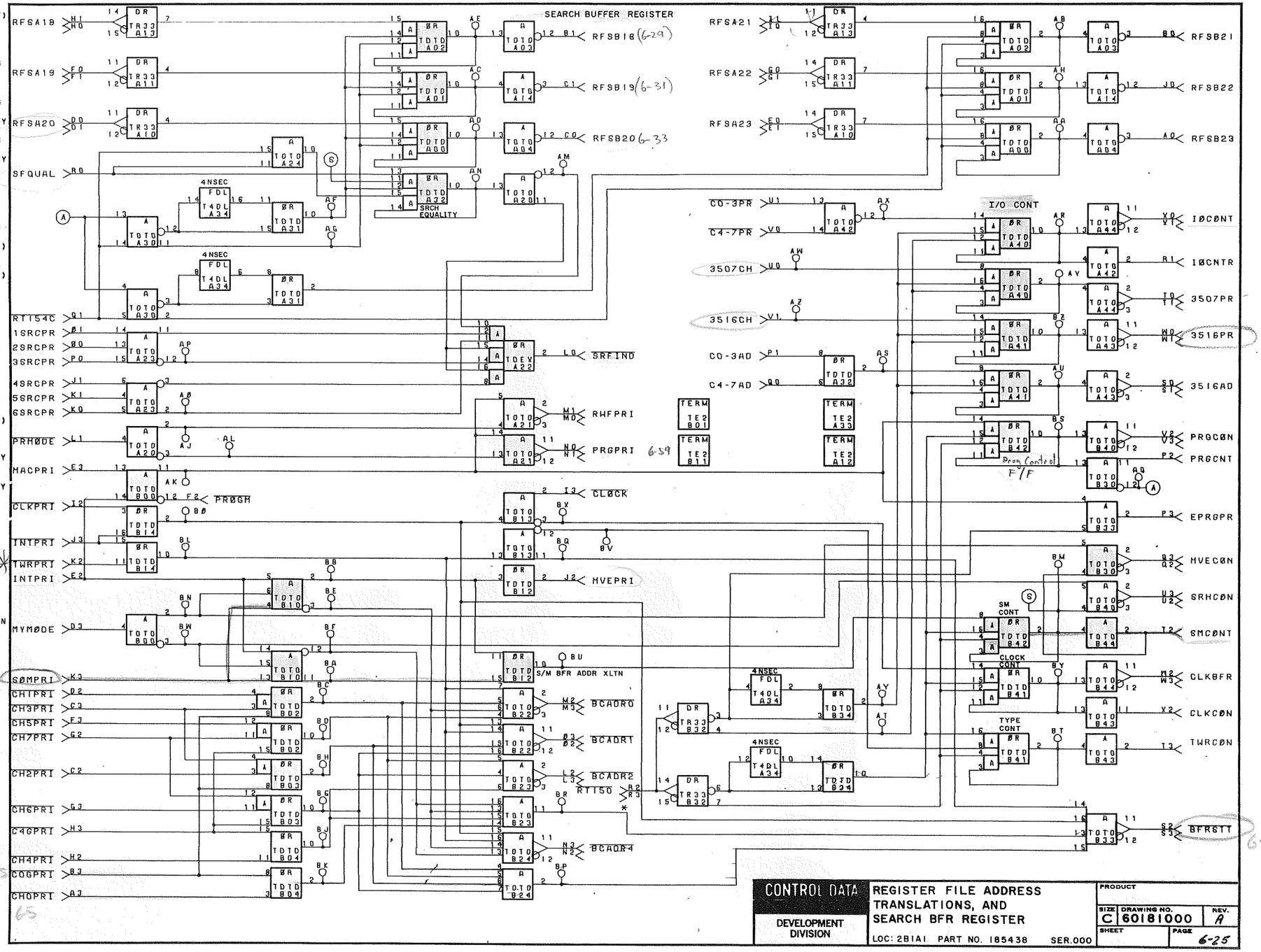
Pg 6-9

s/m

207

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1A2-K1	6- 39		SEARCH BFR NOT(BIT 23) TO D4
A3	2B1A0-D0	6- 5		NOT (CHAN 0 INITIAL RC PRIO)
B0	2B1A4-K1	6- 35		SEARCH BFR NOT(BIT 21) TO D4

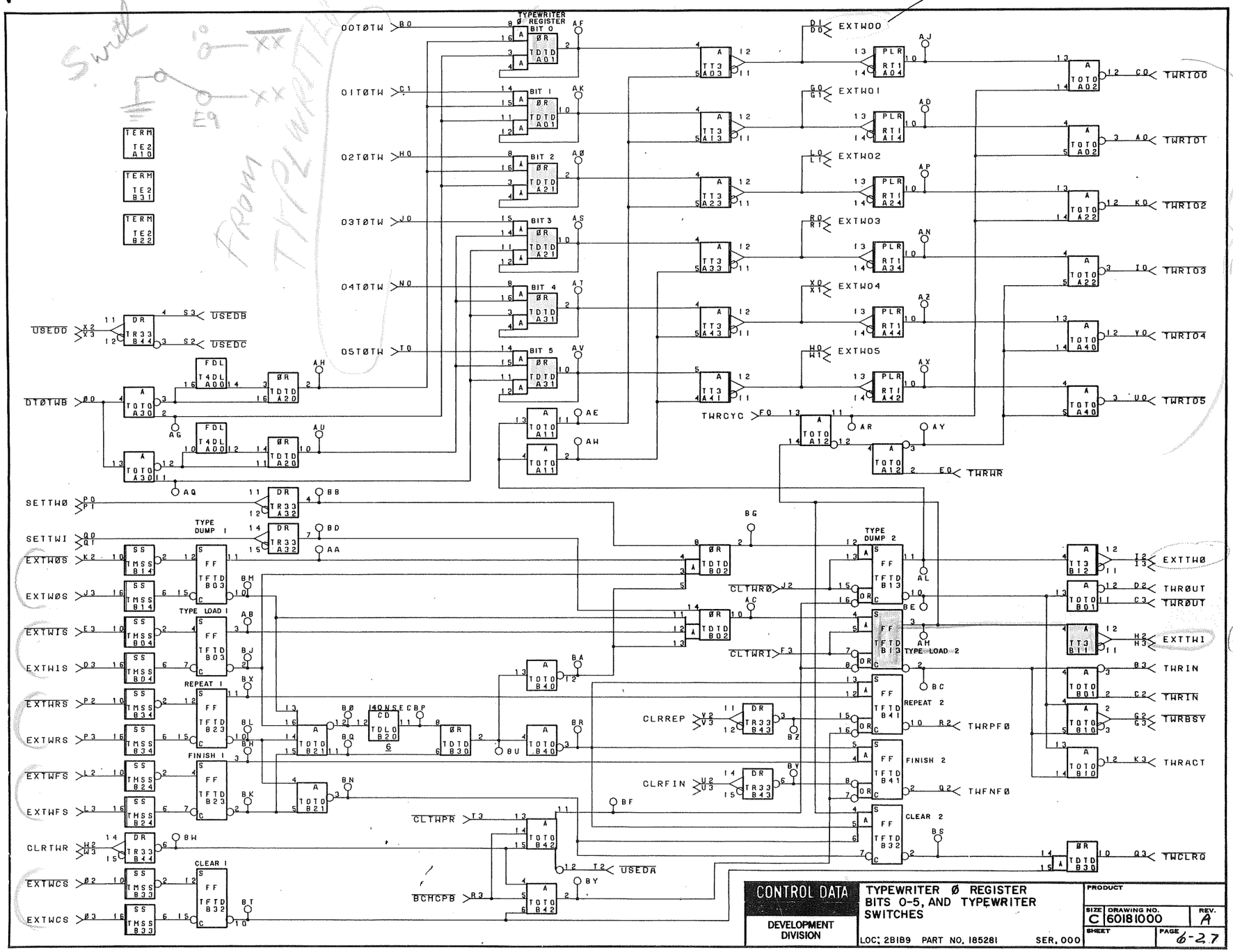
B1	2B1B4-K1	6- 29		SEARCH BFR NOT(BIT 18) TO D4
B3	2B1A0-W0	6- 5		NOT(CHL 0-3 FINAL BC PRIORITY)
C0	2B1B2-K1	6- 33		SEARCH BFR NOT(BIT 20) TO D4
C1	2B1B3-K1	6- 31		SEARCH BFR NOT(BIT 19) TO D4
C2	2B1A0-C0	6- 5		NOT (CHAN 2 INITIAL BC PRIO)
C3	2B1A0-E0	6- 5		NOT (CHAN 3 INITIAL BC PRIO)
D0	2A1A8-C2	6- 55		RF SENSE AMP BIT 20 TO D4 REG
D1	2A1A8-C3	6- 55		
D2	2B1A0-D1	6- 5		NOT (CHAN 1 INITIAL BC PRIO)
D3	2B1A6-J3	6- 13		MOVE MODE TO S/M BRIO XLTN
E0	2A1A8-M2	6- 55		RF SENSE AMP BIT 23 TO D4 REG
E1	2A1A8-M3	6- 55		
E2	2B1A0-U1	6- 5		INTERNAL OPR FINAL BC PRIORITY
E3	2B1B0-T1	6- 7		MAIN CONT INITIAL BC PRIORITY
F0	2A1B8-Q0	6- 53		RF SENSE AMP BIT 19 TO D4 REG
F1	2A1B8-Q1	6- 53		
F2	2B1A8-H0	6- 17	2B1A8-AJ	NOT(R/W RF + PROG) BC PRIORITY
F3	2B1B0-D1	6- 7		NOT (CHAN 5 INITIAL BC PRIO)
G0	2A1A8-N3	6- 55		RF SENSE AMP BIT 22 TO D4 REG
G1	2A1A8-N2	6- 55		
G2	2B1B0-E0	6- 7		NOT (CHAN 7 INITIAL BC PRIO)
G3	2B1B0-C0	6- 7		NOT (CHAN 6 INITIAL BC PRIO)
H0	2A1B8-M1	6- 53		
H1	2A1B8-M0	6- 53		RF SENSE AMP BIT 18 TO D4 REG
H2	2B1B0-D0	6- 7		NOT (CHAN 4 INITIAL BC PRIO)
H3	2B1A0-X0	6- 5		NOT(CHL 4-7 FINAL BC PRIORITY)
I0	2A1A8-H3	6- 55		
I1	2A1A8-H2	6- 55		RF SENSE AMP BIT 21 TO D4 REG
I2	2B1B0-W0	6- 7		NOT(CLOCK INITIAL BC PRIORITY)
I3	2B1A8-G0	6- 17	2B1A8-AH	NOT(CLOCK FINAL BC PRIORITY)
J0	2B1A3-K1	6- 37		SEARCH BFR NOT(BIT 22) TO D4
J1	2B1A4-I3	6- 35		SEARCH COMPARE(D4 BIT 03 = D4 BIT 21)
J2	2B1A6-U3	6- 13		MOVE FINAL BC PRIORITY
J3	2B1A0-U0	6- 5		NOT(INTERNAL OPR FINAL BC PRIORITY)
K0	2B1A2-I3	6- 39		SEARCH COMPARE(D4 BIT 05 = D4 BIT 23)
K1	2B1A3-I3	6- 37		SEARCH COMPARE(D4 BIT 04 = D4 BIT 22)
K2	2B1B0-X0	6- 7		NOT(TWR INITIAL BC PRIORITY)
K3	2B1B0-U1	6- 7		SRCH + MOVE = INITIAL BC PRIO
L0	2B1A6-Q2	6- 13		NOT(SEARCH FIND)
L1	2B1B8-X2	6- 11		NOT(PROG MODE TO BC PRIO XLTN)
L2	2A1A4-U3	6- 59		
L3	2A1A4-U2	6- 59		NOT RF ADDR XLTN BIT 02 TO S
M0	2A1A4-P2	6- 59		
M1	2A1A4-P3	6- 59		R/W REG FILE FINAL BC PRIORITY
M2	2A1A4-D3	6- 59		
M3	2A1A4-D2	6- 59		NOT RF ADDR XLTN BIT 00 TO S
N0	2A1A4-Q3	6- 59		PROG CONTROL FINAL BC PRIORITY
N1	2A1A4-Q2	6- 59		
N2	2A1A4-T2	6- 59		NOT RF ADDR XLTN BIT 04 TO S
N3	2A1A4-T3	6- 59		
O0	2B1B3-I3	6- 31		SEARCH COMPARE(D4 BIT 01 = D4 BIT 19)
O1	2B1B4-I3	6- 29		SEARCH COMPARE(D4 BIT 00 = D4 BIT 18)
O2	2A1A4-C2	6- 59		NOT RF ADDR XLTN BIT 01 TO S
O3	2A1A4-C3	6- 59		
P0	2B1B2-I3	6- 33		SEARCH COMPARE(D4 BIT 02 = D4 BIT 20)
P1	2B1A0-T2	6- 5		CHAN 0-3 A/D PRIORITY XLTN
P2	2B1A6-Q1	6- 13		PROGRAM CONT XLTN TO FAN OUT
P3	2B1A8-G3	6- 17	2B1A8-BK	(PROG CONT)(T150) TO BUSY XLTN
Q0	2B1B0-T2	6- 7		CHAN 4-7 A/D PRIORITY XLTN
Q1	2B1A8-N1	6- 17		NOT(T154) CLR/SET SEARCH BFR
Q2	2A1B6-N0	6- 43		
Q3	2A1B6-N1	6- 43		MOVE CONT XLTN TO Z
R0	2B1A0-C1	6- 5		SEARCH EQUALITY
R1	2B1A0-Q0	6- 5		I/O CONTROL XLTN TO FANOUT
R2	2A1B7-L1	6- 41		
R3	2A1B7-L0	6- 41		T150
S0	2A1B4-E0	6- 57		12-BIT MODE CHAN A/D XLTN
S1	2A1B4-E1	6- 57		
S2	2A1B6-D1	6- 43		
S3	2A1B6-D0	6- 43		NOT READY/BC START EN
T0	2A1B4-O1	6- 57		24-BIT MODE I/O CONT XLTN
T1	2A1B4-O0	6- 57		
T2	2B1A6-D2	6- 13		S/M CONTROL XLTN TO S/M BFR
T3	2B1B8-O1	6- 11		TWR CONTROL XLTN TO TWR BFR
U0	2B1B0-Q2	6- 7	2B1A1-AW	24-BIT MODE CHAN PRIORITY
U1	2B1A0-L1	6- 5		NOT(CHL 0-3 BC PRIORITY XLTN)
U2	2A1B6-M0	6- 43		
U3	2A1B6-M1	6- 43		SEARCH CONTROL XLTN
V0	2B1B0-L1	6- 7		NOT(CHL 4-7 BC PRIORITY XLTN)
V1	2B1A0-Q2	6- 5	2B1A1-AZ	12-BIT MODE CHAN PRIORITY
V2	2A1B6-E0	6- 43		PROGRAM CONTROL XLTN
V3	2A1B6-E1	6- 43		
W0	2A1B4-N1	6- 57		12-BIT MODE I/O CONT XLTN
W1	2A1B4-N0	6- 57		
W2	2A1B7-E1	6- 41		CLOCK CONTROL XLTN
W3	2A1B7-E0	6- 41		
X0	2A1B4-U1	6- 57		I/O CONTROL XLTN
X1	2A1B4-U0	6- 57		
X2	2B1B8-C0	6- 11		CLOCK CONT XLTN TO CLOCK BFR



CONTROL DATA	REGISTER FILE ADDRESS TRANSLATIONS, AND SEARCH BFR REGISTER	PRODUCT	
DEVELOPMENT DIVISION	LOC: 2B1A1 PART NO. 185438 SER.000	SIZE C	DRAWING NO. 60181000 REV. A
		SHEET	PAGE 6-25

209

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1B3=F0	6= 31		NOT(TWR BIT 01) CONSOLE TO D4
B0	2B1B4=D2	6= 29		D4 BIT 00 TO TYPEWRITER 0 REG
B3	2B1B8=J0	6= 11		TYPE IN XLTN TO TWR BFR
C0	2B1B4=F0	6= 29		NOT(TWR BIT 00) CONSOLE TO D4
C1	2B1B3=D2	6= 31		D4 BIT 01 TO TYPEWRITER 0 REG
C2	2B1B8=S1	6= 11		NOT(TYPE IN) XLTN TO TWR BFR
C3	2B1B8=T1	6= 11		NOT(TYPE OUT) XLTN TO TWR BFR
D0	2A1A06J15A=02			
	2A1A06J16A=02			
D1	2A1A06J15A=01			TW 0 REG BIT 00 TO CONSOLE
	2A1A06J16A=01			
D2	2B1B8=L0	6= 11		TYPE OUT XLTN TO TWR BFR
D3	2A1A06J16F=07			CONSOLE TYPE LOAD SW
E0	2B1B6=E2	6= 15	2B1B6=RE	NOT(TYPE CONTROL/WRITE MCS)
E3	2A1A06J16F=08			NOT(CONSOLE TYPE LOAD SW
F0	2B1B8=W1	6= 11		TYPE, CONTROL TO TYPE, RCVR
F3	2B1B8=T0	6= 11		NOT(CLEAR TYPE-IN FF)
G0	2A1A06J15A=03			TW 0 REG BIT 01 TO CONSOLE
	2A1A06J16A=03			
G1	2A1A06J15A=04			
	2A1A06J16A=04			
G2	2B0A6=Q1	6=121		
G3	2B0A6=Q0	6=121		NOT TW BUSY TO STATUS FI
H0	2B1B2=D2	6= 33		D4 BIT 02 TO TYPEWRITER 0 REG
H2	2A1A06J15B=07			TW LOAD XLTN TO CONSOLE
	2A1A06J16B=07			
H3	2A1A06J15B=08			
	2A1A06J16B=08			
I0	2B1A4=F0	6= 35		NOT(TWR BIT 03) CONSOLE TO D4
I2	2A1A06J15B=09			TW DUMP XLTN TO CONSOLE
	2A1A06J16B=09			
I3	2A1A06J15B=10			
	2A1A06J16B=10			
J0	2B1A4=D2	6= 35		D4 BIT 03 TO TYPEWRITER 0 REG
J2	2B1B8=S0	6= 11		NOT(CLEAR TYPEOUT FF)
J3	2A1A06J16F=05			CONSOLE TYPE DUMP SW
K0	2B1B2=F0	6= 33		NOT(TWR BIT 02) CONSOLE TO D4
K2	2A1A06J16F=06			NOT(CONSOLE TYPE DUMP SW)
K3	2B1B8=P1	6= 11		TYPE BUSY TO TWR BFR
L0	2A1A06J15A=05			TW 0 REG BIT 02 TO CONSOLE
	2A1A06J16A=05			
L1	2A1A06J15A=06			
	2A1A06J16A=06			
L2	2A1A06J16F=02			NOT(CONSOLE TYPE FINISH SW)
L3	2A1A06J16F=01			CONSOLE TYPE FINISH SW
N0	2B1A3=D2	6= 37		D4 BIT 04 TO TYPEWRITER 0 REG
O0	2B1B8=N1	6= 11		NOT(D4 TO TW 0 REG CLR/SET)
O2	2A1A06J16E=10			NOT(CONSOLE TYPE CLEAR SW)
O3	2A1A06J16E=09			CONSOLE TYPE CLEAR SW
P0	2B0A9=03	6=101		SET TYPE OUT TO TWR CONTROL
P1	2B0A9=02	6=101		
P2	2A1A06J16F=04			NOT(CONSOLE TYPE REPEAT SW)
P3	2A1A06J16F=03			CONSOLE TYPE REPEAT SW
Q0	2B0A9=N2	6=101		SET TYPE IN TO TWR CONTROL
Q1	2B0A9=N3	6=101		
Q2	2B1A0=L0	6= 5		TWR FINISH XLTN TO FAN OUT
Q3	2B1B1=L1	6= 9	2B1B1=AN	NOT(TWR CLEAR REQ) TO CLR BFR
R0	2A1A06J15A=07			TW 0 REG BIT 03 TO CONSOLE
	2A1A06J16A=07			
R1	2A1A06J15A=08			
	2A1A06J16A=08			
R2	2B1A7=I1	6= 1	2B1A7=AE	TWR REPEAT XLTN TO FAN OUT
R3	2B1B1=H1	6= 9		NOT (CLEAR TW BFR CONTROLS)
T0	2B1A2=D2	6= 39		D4 BIT 05 TO TYPEWRITER 0 REG
T3	2B1B1=H0	6= 9		NOT(CLR TYPEWRITER BFR)
U0	2B1A2=F0	6= 39		NOT(TWR BIT 05) CONSOLE TO D4
U2	2B0A5=B1	6=123		CLEAR TYPEWRITER FINISH FF
U3	2B0A5=B0	6=123		
V0	2B1A3=F0	6= 37		NOT(TWR BIT 04) CONSOLE TO D4
V2	2B0A6=B1	6=121		CLEAR TYPEWRITER REPEAT FF
V3	2B0A6=B0	6=121		
W0	2A1A06J15B=01			TW 0 REG BIT 05 TO CONSOLE
	2A1A06J16B=01			
W1	2A1A06J15B=02			
	2A1A06J16B=02			
W2	2B0A9=00	6=101		CLEAR TYPEWRITER CONTROLS
W3	2B0A9=01	6=101		
X0	2A1A06J15A=09			TW 0 REG BIT 04 TO CONSOLE
	2A1A06J16A=09			
X1	2A1A06J15A=10			
	2A1A06J16A=10			



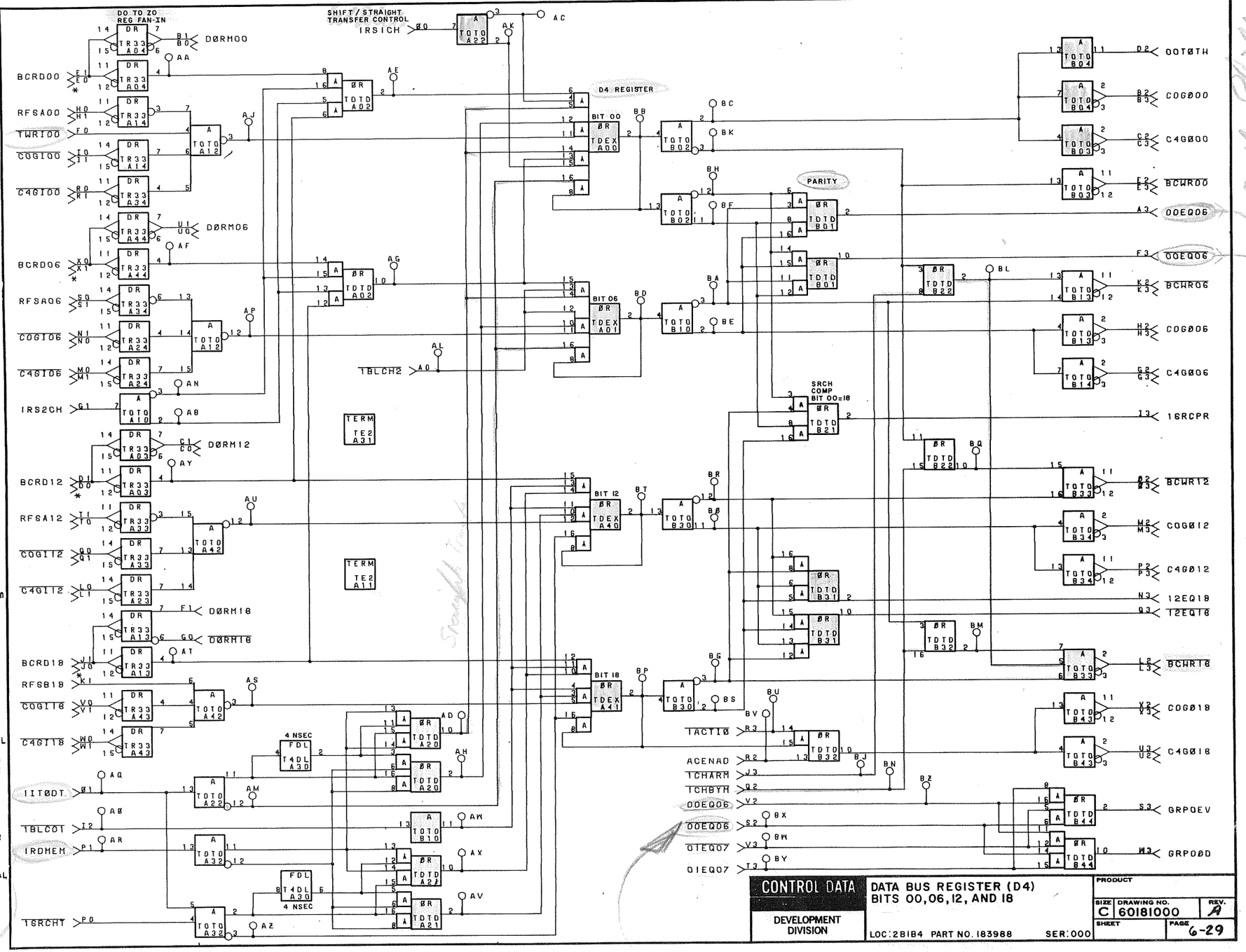
CONTROL DATA DEVELOPMENT DIVISION	TYPEWRITER Ø REGISTER BITS 0-5, AND TYPEWRITER SWITCHES	PRODUCT
	LOC: 2B1B9 PART NO. 185281 SER. 000	SIZE C DRAWING NO. 60181000 REV. A
		SHEET PAGE 6-27

211

FAN-OUT

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1B5-S1	6- 21	2B1B4-AL	NOT(RLK CHAR 02) TO D4 BIT 00
A3	2B1B4-V2	6- 29		BIT 00 = BIT 06 = D4 REGISTER
B0	2A1B7-L2	6- 41		
B1	2A1B7-L3	6- 41		DO BIT 00 TO Z REG FAN IN
B2	2A0A7-C0	6-133		D4 BIT 00 TO CHL 0-3 FAN OUT
B3	2A0A7-C1	6-133		
C0	2A1A7-W1	6- 51		
C1	2A1A7-W0	6- 51		DO BIT 12 TO Z REG FAN IN
C2	2C0B7-C0	6-169		D4 BIT 00 TO CHL 4-7 FAN OUT
C3	2C0B7-C1	6-169		
D0	2B2A4-B2	5- 65		
D1	2B2A4-B3	5- 65		NOT BC READ BIT 12
D2	2B1B9-B0	6- 27		D4 BIT 00 TO TYPEWRITER 0 REG
E0	2B2A9-B2	5- 57		
E1	2B2A9-B3	5- 57		NOT BC READ BIT 00
E2	2B2A9-D0	5- 57		
E3	2B2A9-D1	5- 57		NOT D4 BIT 00 TO MCS VIA F1
F0	2B1B9-C0	6- 27		NOT(TWR BIT 00) CONSOLE TO D4
F1	2B1A9-W2	6- 23		DO BIT 18 TO Z REG FAN IN XLTN
F3	2B1B4-S2	6- 29	2B1B4-BX	NOT(BIT 00 = BIT 06) D4 REG
G0	2B1A6-V0	6- 13		NOT (DO BIT 18) TO SUPPRESS A/D XLTN
G1	2B1B5-R3	6- 21		RS 2 CHAR POS, TO D4 BIT 00
G2	2C0B3-D1	6-173		D4 BIT 06 TO CHL 4-7 FAN OUT
G3	2C0B3-D0	6-173		
H0	2A1B5-R1	6- 45		RF SENSE AMP BIT 00 TO D4 REG
H1	2A1B5-R0	6- 45		
H2	2A0A3-D1	6-137		D4 BIT 06 TO CHAN 0-3 FANOUT
H3	2A0A3-D0	6-137		
I0	2A0A4-I1	6-157		
I1	2A0A4-I0	6-157		NOT CHL 0-3 BIT 00 F1 TO D4
I2	2B1B5-T1	6- 21	2B1B4-AO	NOT(RLK 00/01) TO D4 BIT 00
I3	2B1A1-O1	6- 25		SEARCH COMPARE(D4 BIT 00 = D4 BIT 18)
J0	2B2A2-B2	5- 69		
J1	2B2A2-B3	5- 69		NOT BC READ BIT 18
J3	2B1B5-R1	6- 21	2B1B4-BJ	NOT(CHAR MODE) TO D4 BIT 00
K1	2B1A1-B1	6- 25		SEARCH BFR NOT(BIT 18) TO D4
K2	2B2A7-D0	5- 61		
K3	2B2A7-D1	5- 61		NOT D4 BIT 06 TO MCS VIA F1
L0	2C0A5-I1	6-195		
L1	2C0A5-I0	6-195		NOT CHL 4-7 BIT 12 F1 TO D4
L2	2B2A2-D0	5- 69		
L3	2B2A2-D1	5- 69		NOT D4 BIT 18 TO MCS VIA F1
M0	2C0B4-P3	6-193		
M1	2C0B4-P2	6-193		NOT CHL 4-7 BIT 06 F1 TO D4
M2	2A0A7-W2	6-133		D4 BIT 12 TO CHL 0-3 FAN OUT
M3	2A0A7-W3	6-133		
N0	2A0A4-P2	6-157		NOT CHAN 0-3 BIT 06 F1 TO D4
N1	2A0A4-P3	6-157		
N3	2B1B3-V2	6- 31		(BIT 12 = BIT 18) D4 REG
O0	2B1B5-Q1	6- 21		RS 1 CHAR POS, TO D4 BIT 00
O1	2B1B6-K0	6- 15	2B1B4-AQ	INPUT TO D4 TIMING = BIT 00
O2	2B2A4-D0	5- 65		
O3	2B2A4-D1	5- 65		NOT D4 BIT 12 TO MCS VIA F1
P0	2B1A6-B2	6- 13		NOT(SEARCH DATA) TO D4 BIT 18
P1	2B1B6-N2	6- 15	2B1B4-AR	ENABLE D0 = MCS TO D4 = BIT 00
P2	2C0B7-W2	6-169		D4 BIT 12 TO CHL 4-7 FAN OUT
P3	2C0B7-W3	6-169		
Q0	2A0B5-I1	6-159		
Q1	2A0B5-I0	6-159		NOT CHAN 0-3 BIT 12 F1 TO D4
Q2	2B1B5-Q3	6- 21	2B1B4-RN	NOT(CHAR=BYTE) TO D4 BIT 00
Q3	2B1B3-S2	6- 31	2B1B3-RX	NOT(BIT 12 = BIT 18) D4 REG
R0	2C0B4-I1	6-193		
R1	2C0B4-I0	6-193		NOT CHL 4-7 BIT 00 F1 TO D4
R2	2B1A9-A3	6- 23	2B1B4-RV	ACT, I/O CHAN ASSY/DISASSY
R3	2B1B0-P0	6- 7	2B1B4-RU	NOT (ACT, I/O = BLOCK D4 BIT 18)
S0	2A1A5-I2	6- 47		RF SENSE AMP BIT 06 TO D4 REG
S1	2A1A5-I3	6- 47		
S2	2B1B4-F3	6- 29	2B1B4-RX	NOT(BIT 00 = BIT 06) D4 REG
S3	2B1B0-G3	6- 7		SUM OF 00/01/06/07= EVEN TOTAL
T0	2A1A7-J1	6- 51		
T1	2A1A7-J0	6- 51		RF SENSE AMP BIT 12 TO D4 REG
T3	2B1B3-A3	6- 31		BIT 01 = BIT 07 = D4 REGISTER
U0	2A1A5-U3	6- 47		
U1	2A1A5-U2	6- 47		DO BIT 06 TO Z REG FAN IN
U2	2C0A6-G0	6-163		
U3	2C0A6-G1	6-163		D4 BIT 18 TO CHL 4-7 FAN OUT
V0	2A0B5-P3	6-159		
V1	2A0B5-P2	6-159		NOT CHAN 0-3 BIT 18 F1 TO D4
V2	2B1B4-A3	6- 29		BIT 00 = BIT 06 = D4 REGISTER
V3	2B1B3-F3	6- 31	2B1B4-RW	NOT(BIT 01 = BIT 07) D4 REG
W0	2C0A5-P3	6-195		
W1	2C0A5-P2	6-195		NOT CHL 4-7 BIT 18 F1 TO D4
W3	2B1B0-A3	6- 7		SUM OF 00/01/06/07= ODD TOTAL
X0	2B2A7-B3	5- 61		NOT BC READ BIT 06
X1	2B2A7-B2	5- 61		
X2	2A0B6-G1	6-127		D4 BIT 18 TO CHL 0-3 FAN OUT
X3	2A0B6-G0	6-127		

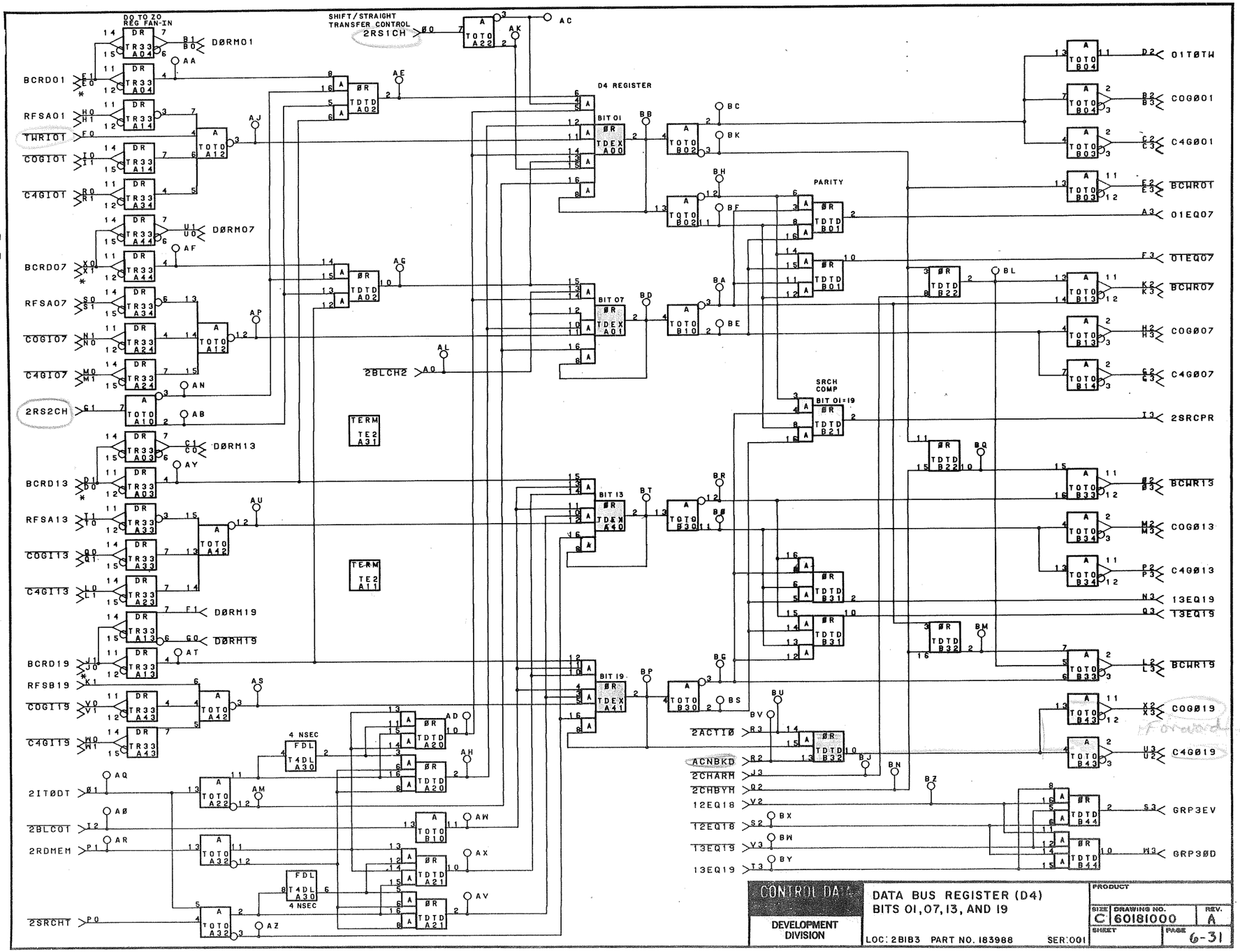
PAGE 6- 29



CONTROL DATA	DATA BUS REGISTER (D4) BITS 00,06,12, AND 18	PRODUCT
DEVELOPMENT DIVISION	LOC:2B1B4 PART NO. 183988 SER:000	SIZE C · DRAWING NO. 60181000 · REV. A · SHEET · PAGE 6-29

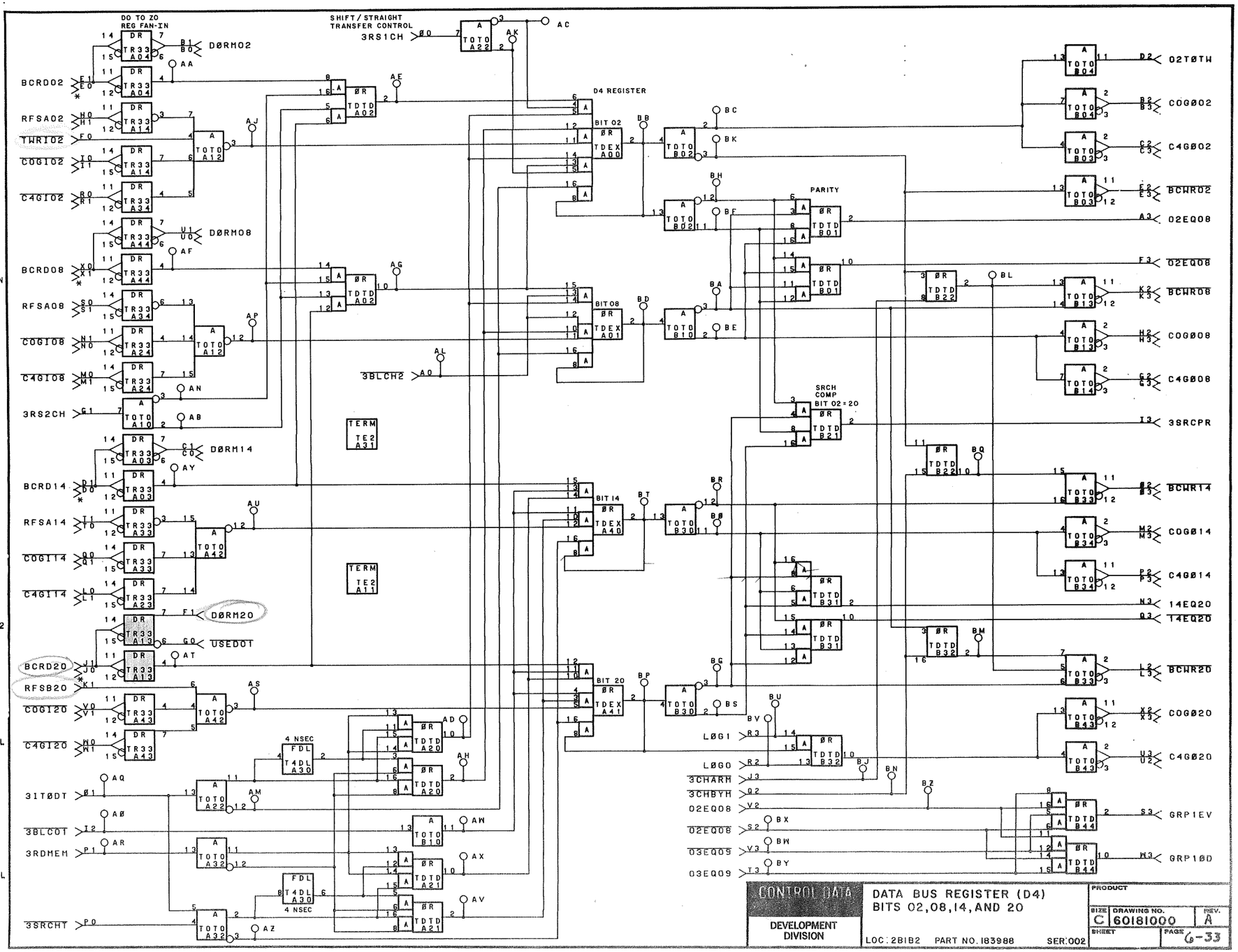
213

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1A5-T1	6- 19	2B1B3-AL	NOT(BLK CHAR 02) TO D4 BIT 01
A3	2B1B4-T3	6- 29		BIT 01 = BIT 07 - D4 REGISTER
B0	2A1B7-M3	6- 41		
B1	2A1B7-M2	6- 41		D0 BIT 01 TO Z REG FAN IN
B2	2A0A6-C0	6-135		D4 BIT 01 TO CHL 0-3 FAN OUT
B3	2A0A6-C1	6-135		
C0	2A1A7-V1	6- 51		
C1	2A1A7-V0	6- 51		D0 BIT 13 TO Z REG FAN IN
C2	2C0B6-C0	6-171		D4 BIT 01 TO CHL 4-7 FAN OUT
C3	2C0B6-C1	6-171		
D0	2B2A4-M2	5- 65		
D1	2B2A4-M3	5- 65		NOT BC READ BIT 13
D2	2B1B9-C1	6- 27		D4 BIT 01 TO TYPEWRITER O REG
E0	2B2A9-M2	5- 57		
E1	2B2A9-M3	5- 57		NOT BC READ BIT 01
E2	2B2A9-00	5- 57		
E3	2B2A9-01	5- 57		NOT D4 BIT 01 TO MCS VIA F1
F0	2B1B9-A0	6- 27		NOT(TWR BIT 01) CONSOLE TO D4
F1	2B1A9-H3	6- 23		D0 BIT 19 TO Z REG FAN IN XLTN
F3	2B1B4-V3	6- 29	2B1B4-RW	NOT(BIT 01 = BIT 07) D4 REG
G0	2B1A9-B3	6- 23		NOT(D0 BIT 19) TO FORWARD XLTN
G1	2B1A5-Q1	6- 19		RS 2 CHAR POS, TO D4 BIT 01
G2	2C0B2-D1	6-175		D4 BIT 07 TO CHL 4-7 FAN OUT
G3	2C0B2-D0	6-175		
H0	2A1B5-U0	6- 45		RF SENSE AMP BIT 01 TO D4 REG
H1	2A1B5-U1	6- 45		
H2	2A0A2-D1	6-139		D4 BIT 07 TO CHL 0-3 FAN OUT
H3	2A0A2-D0	6-139		
I0	2A0A4-J0	6-157		
I1	2A0A4-J1	6-157		NOT CHAN 0-3 BIT 01 FI TO D4
I2	2B1A5-S1	6- 19	2B1B3-AO	NOT(BLK 00/01) TO D4 BIT 01
I3	2B1A1-00	6- 25		SEARCH COMPARE(D4 BIT 01 = D4 BIT 19)
J0	2B2A2-M2	5- 69		
J1	2B2A2-M3	5- 69		NOT BC READ BIT 19
J3	2B1A5-Q3	6- 19	2B1B3-BJ	NOT(CHAR MODE) TO D4 BIT 01
K1	2B1A1-C1	6- 25		SEARCH BFR NOT(BIT 19) TO D4
K2	2B2A7-00	5- 61		
K3	2B2A7-01	5- 61		NOT D4 BIT 07 TO MCS VIA F1
L0	2C0A5-J0	6-195		
L1	2C0A5-J1	6-195		NOT CHL 4-7 BIT 13 FI TO D4
L2	2B2A2-00	5- 69		
L3	2B2A2-01	5- 69		NOT D4 BIT 19 TO MCS VIA FI
M0	2C0B4-03	6-193		
M1	2C0B4-02	6-193		NOT CHL 4-7 BIT 07 FI TO D4
M2	2A0B7-W3	6-125		D4 BIT 13 TO CHL 0-3 FAN OUT
M3	2A0B7-W2	6-125		
N0	2A0A4-02	6-157		NOT CHAN 0-3 BIT 07 FI TO D4
N1	2A0A4-03	6-157		
N3	2B1B3-T3	6- 31		(BIT 13 = BIT 19) D4 REG
O0	2B1A5-R3	6- 19		RS 1 CHAR POS, TO D4 BIT 01
O1	2B1R6-00	6- 15	2B1B3-AQ	INPUT TO D4 TIMING - BIT 01
O2	2B2A4-00	5- 65		
O3	2B2A4-01	5- 65		NOT D4 BIT 13 TO MCS VIA F1
P0	2B1A6-E2	6- 13		NOT(SEARCH DATA) TO D4 BIT 19
P1	2B1R6-N3	6- 15	2B1B3-AR	ENABLE D0 - MCS TO D4 - BIT 01
P2	2C0A7-W3	6-161		D4 BIT 13 TO CHL 4-7 FAN OUT
P3	2C0A7-W2	6-161		
Q0	2A0B5-J0	6-159		
Q1	2A0B5-J1	6-159		NOT CHAN 0-3 BIT 13 FI TO D4
Q2	2B1A5-R1	6- 19	2B1B3-BN	NOT(CHAR-BYTE) TO D4 BIT 01
Q3	2B1B3-V3	6- 31	2B1B3-RW	NOT(BIT 13 = BIT 19) D4 REG
R0	2C0B4-J0	6-193		
R1	2C0B4-J1	6-193		NOT CHL 4-7 BIT 01 FI TO D4
R2	2B1A9-B2	6- 23	2B1B3-RV	ACT, I/O FORWARD ASSY/DISASSY
R3	2B1B0-P1	6- 7	2B1B3-RU	NOT (ACT, I/O = BLOCK D4 BIT 19)
S0	2A1A5-L2	6- 47		RF SENSE AMP BIT 07 TO D4 REG
S1	2A1A5-L3	6- 47		
S2	2B1B4-Q3	6- 29	2B1B3-RX	NOT(BIT 12 = BIT 18) D4 REG
S3	2B1A0-G3	6- 5		SUM OF 12/13/18/19= EVEN TOTAL
T0	2A1A7-L0	6- 51		
T1	2A1A7-L1	6- 51		RF SENSE AMP BIT 13 TO D4 REG
T3	2B1B3-N3	6- 31		(BIT 13 = BIT 19) D4 REG
U0	2A1A5-V3	6- 47		
U1	2A1A5-V2	6- 47		D0 BIT 07 TO Z REG FAN IN
U2	2C0A3-L0	6-165		
U3	2C0A3-L1	6-165		D4 BIT 19 TO CHL 4-7 FAN OUT
V0	2A0B5-03	6-159		
V1	2A0B5-02	6-159		NOT CHAN 0-3 BIT 19 FI TO D4
V2	2B1B4-N3	6- 29		(BIT 12 = BIT 18) D4 REG
V3	2B1B3-Q3	6- 31	2B1B3-RW	NOT(BIT 13 = BIT 19) D4 REG
W0	2C0A5-03	6-195		
W1	2C0A5-02	6-195		NOT CHL 4-7 BIT 19 FI TO D4
W3	2B1A0-A3	6- 5		SUM OF 12/13/18/19= ODD TOTAL
X0	2B2A7-M3	5- 61		NOT BC READ BIT 07
X1	2B2A7-M2	5- 61		
X2	2A0B3-L1	6-129		D4 BIT 19 TO CHL 0-3 FAN OUT
X3	2A0B3-L0	6-129		

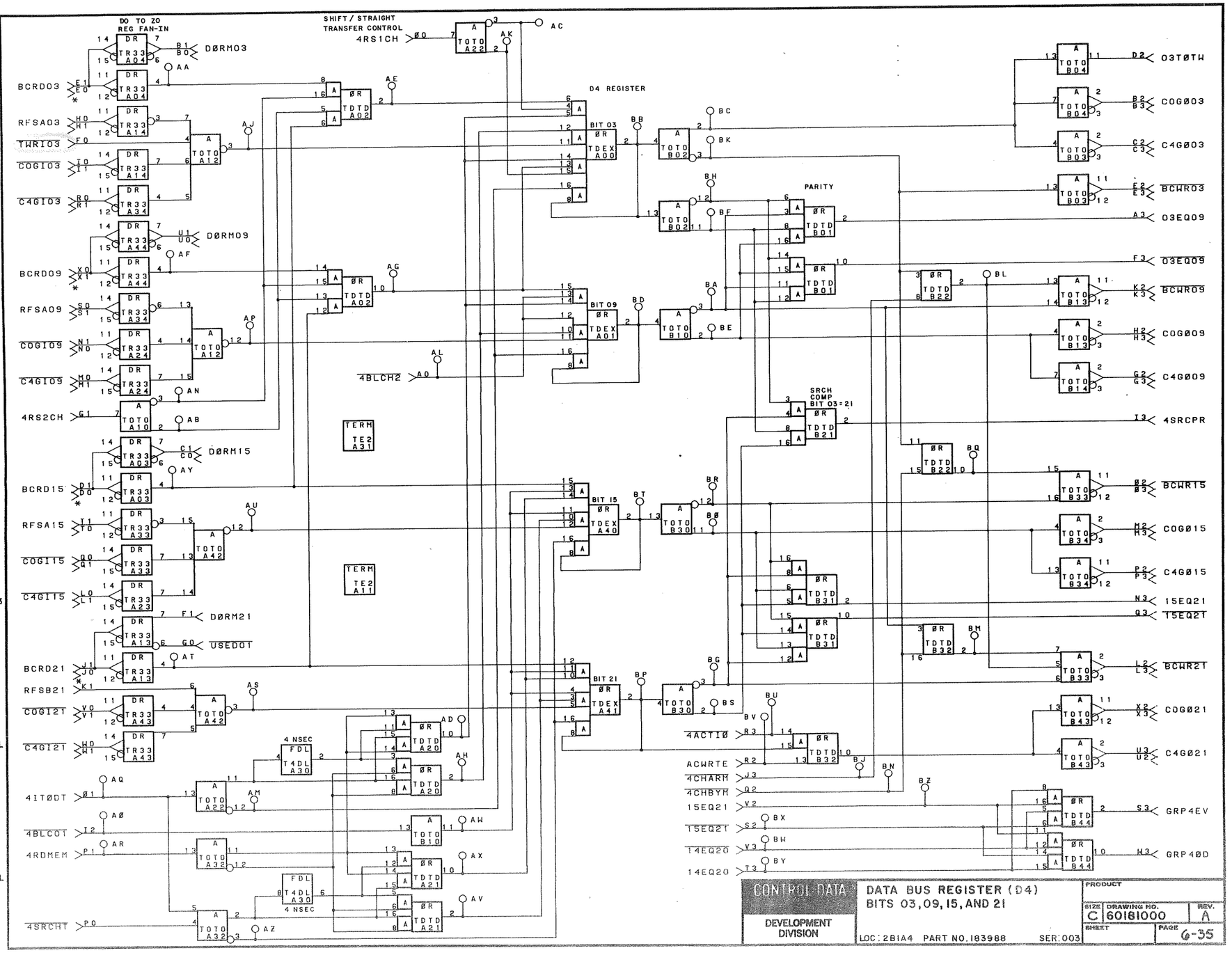


215

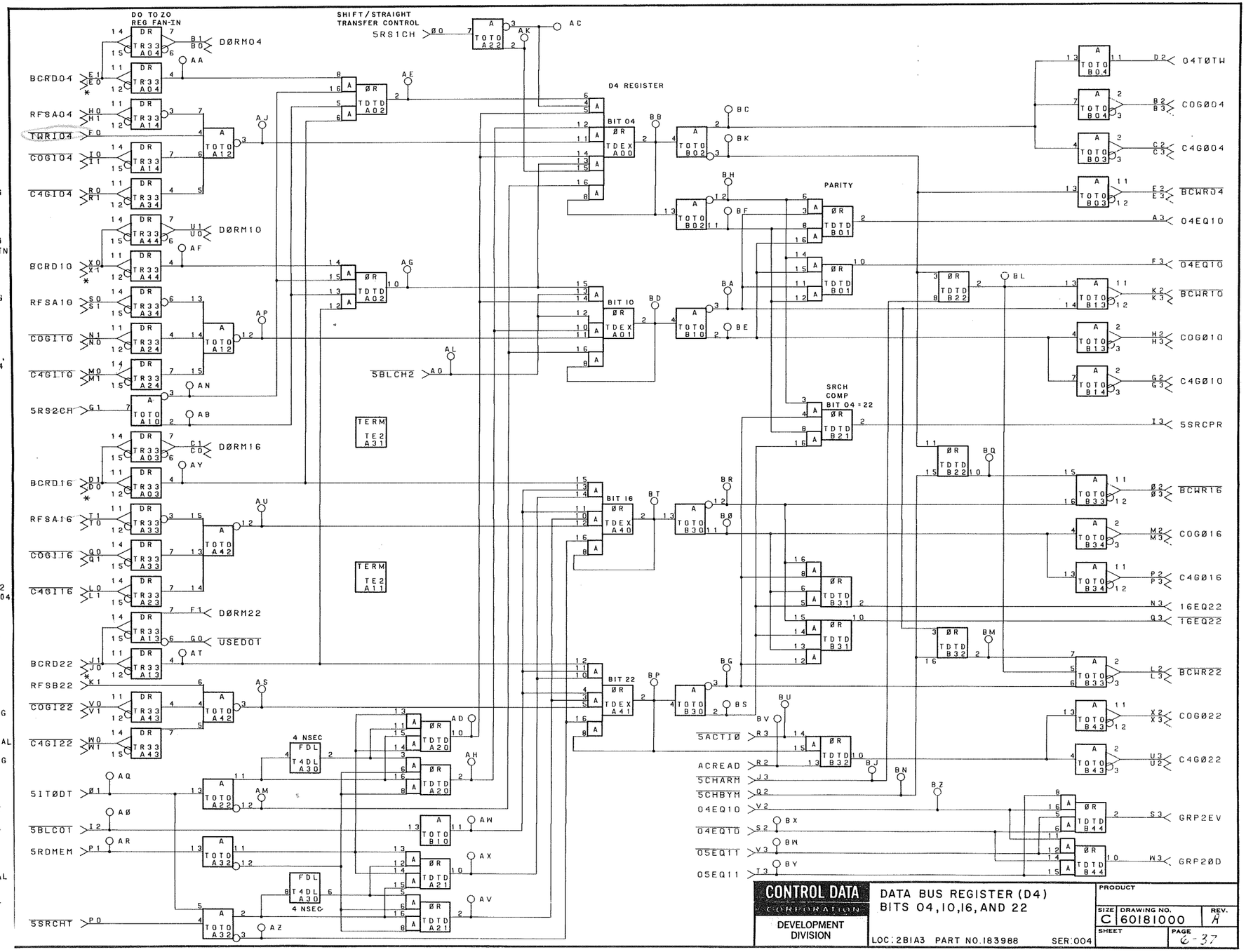
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1B5-X0	6- 21	2B1B2-AL	NOT(BLK CHAR 02) TO D4 BIT 02
A3	2B1B2-V2	6- 33		BIT 02 = BIT 08 = D4 REGISTER
B0	2A1B5-E3	6- 45		
B1	2A1B5-E2	6- 45		DO BIT 02 TO Z REG FAN-IN
B2	2A0A3-C0	6-137		D4 BIT 02 TO CHL 0-3 FAN OUT
B3	2A0A3-C1	6-137		
C0	2A1A7-U3	6- 51		
C1	2A1A7-U2	6- 51		DO BIT 14 TO Z REG FAN IN
C2	2C0B3-C0	6-173		D4 BIT 02 TO CHL 4-7 FAN OUT
C3	2C0B3-C1	6-173		
D0	2B2A4-T2	5- 65		
D1	2B2A4-T3	5- 65		NOT BC READ BIT 14
D2	2B1B9-H0	6- 27		D4 BIT 02 TO TYPEWRITER 0 REG
E0	2B2A9-T2	5- 57		
E1	2B2A9-T3	5- 57		NOT BC READ BIT 02
E2	2B2A9-Q1	5- 57		
E3	2B2A9-Q0	5- 57		NOT D4 BIT 02 TO MCS VIA F1
F0	2B1B9-K0	6- 27		NOT(TWR BIT 02) CONSOLE TO D4
F1	2B1A9-I2	6- 23		DO BIT 20 TO Z REG FAN IN XLTN
F3	2B1B2-S2	6- 33	2B1B2-RX	NOT(BIT 02 = BIT 08) D4 REG
G1	2B1B5-R2	6- 21		RS 2 CHAR POS, TO D4 BIT 02
G2	2C0B7-J0	6-169		D4 BIT 08 TO CHL 4-7 FAN OUT
G3	2C0B7-J1	6-169		
H0	2A1B5-R2	6- 45		RF SENSE AMP BIT 02 TO D4 REG
H1	2A1B5-R3	6- 45		
H2	2A0A7-J0	6-133		D4 BIT 08 TO CHL 0-3 FAN OUT
H3	2A0A7-J1	6-133		
I0	2A0A4-K0	6-157		
I1	2A0A4-K1	6-157		NOT CHAN 0-3 BIT 02 F1 TO D4
I2	2B1B5-U0	6- 21	2B1B2-AO	NOT(BLK 00/01) TO D4 BIT 02
I3	2B1A1-P0	6- 25		SEARCH COMPARE(D4 BIT 02 = D4 BIT 20)
J0	2B2A2-T2	5- 69		
J1	2B2A2-T3	5- 69		NOT BC READ BIT 20
J3	2B1B5-V0	6- 21	2B1B2-RJ	NOT(CHAR MODE) TO D4 BIT 02
K1	2B1A1-C0	6- 25		SEARCH BFR NOT(BIT 20) TO D4
K2	2B2A7-Q1	5- 61		
K3	2B2A7-Q0	5- 61		NOT D4 BIT 08 TO MCS VIA F1
L0	2C0A5-K0	6-195		
L1	2C0A5-K1	6-195		NOT CHL 4-7 BIT 14 F1 TO D4
L2	2B2A2-Q1	5- 69		
L3	2B2A2-Q0	5- 69		NOT D4 BIT 20 TO MCS VIA F1
M0	2C0B4-N2	6-193		
M1	2C0B4-N3	6-193		NOT CHL 4-7 BIT 08 F1 TO D4
M2	2A0B6-W3	6-127		D4 BIT 14 TO CHAN 0-3 FANOUT
M3	2A0B6-W2	6-127		
N0	2A0A4-N3	6-157		NOT CHAN 0-3 BIT 08 F1 TO D4
N1	2A0A4-N2	6-157		
N3	2B1A4-T3	6- 35		(BIT 14 = BIT 20) D4 REG
O0	2B1B5-W0	6- 21		RS 1 CHAR POS, TO D4 BIT 02
O1	2B1B6-P1	6- 15	2B1B2-AQ	INPUT TO D4 TIMING = BIT 02
O2	2B2A4-Q1	5- 65		
O3	2B2A4-Q0	5- 65		NOT D4 BIT 14 TO MCS VIA F1
P0	2B1A6-E3	6- 13		NOT(SEARCH DATA) TO D4 BIT 20
P1	2B1B6-O2	6- 15	2B1B2-AR	ENABLE D0 = MCS TO D4 = BIT 02
P2	2C0A6-W3	6-163		D4 BIT 14 TO CHL 4-7 FAN OUT
P3	2C0A6-W2	6-163		
Q0	2A0B5-K0	6-159		
Q1	2A0B5-K1	6-159		NOT CHAN 0-3 BIT 14 F1 TO D4
Q2	2B1B5-Q2	6- 21	2B1B2-RN	NOT(CHAR=BYTE) TO D4 BIT 02
Q3	2B1A4-V3	6- 35	2B1A4-RW	NOT(BIT 14 = BIT 20) D4 REG
R0	2C0B4-K0	6-193		
R1	2C0B4-K1	6-193		NOT CHL 4-7 BIT 02 F1 TO D4
S0	2A1A6-J0	6- 49		RF SENSE AMP BIT 08 TO D4 REG
S1	2A1A6-J1	6- 49		
S2	2B1B2-F3	6- 33	2B1B2-RX	NOT(BIT 02 = BIT 08) D4 REG
S3	2B1B0-L2	6- 7		SUM OF 02/08/03/09= EVEN TOTAL
T0	2A1A7-I3	6- 51		
T1	2A1A7-I2	6- 51		RF SENSE AMP BIT 14 TO D4 REG
T3	2B1A4-A3	6- 35		BIT 03 = BIT 09 = D4 REGISTER
U0	2A1A6-W1	6- 49		
U1	2A1A6-W0	6- 49		DO BIT 08 TO Z REG FAN IN
U2	2C0A2-L0	6-167		
U3	2C0A2-L1	6-167		D4 BIT 20 TO CHL 4-7 FAN OUT
V0	2A0B5-N2	6-159		
V1	2A0B5-N3	6-159		NOT CHAN 0-3 BIT 20 F1 TO D4
V2	2B1B2-A3	6- 33		BIT 02 = BIT 08 = D4 REGISTER
V3	2B1A4-F3	6- 35	2B1B2-RW	NOT(BIT 03 = BIT 09) D4 REG
W0	2C0A5-N2	6-195		
W1	2C0A5-N3	6-195		NOT CHL 4-7 BIT 20 F1 TO D4
W3	2B1B0-B2	6- 7		SUM OF 02/08/03/09= ODD TOTAL
X0	2B2A7-T3	5- 61		NOT BC READ BIT 08
X1	2B2A7-T2	5- 61		
X2	2A0B2-L1	6-131		D4 BIT 20 TO CHAN 0-3 FANOUT
X3	2A0B2-L0	6-131		



PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1A5-U0	6- 19	2B1A4-AL	NOT(RLK CHAR 02) TO D4 BIT 03
A3	2B1B2-T3	6- 33		BIT 03 = BIT 09 - D4 REGISTER
B0	2A1B5-D2	6- 45		
B1	2A1R5-D3	6- 45		D0 BIT 03 TO Z REG FAN IN
B2	2A0A2-C0	6-139		D4 BIT 03 TO CHAN 0-3 FANOUT
B3	2A0A2-C1	6-139		
C0	2A1A7-V3	6- 51		
C1	2A1A7-V2	6- 51		D0 BIT 15 TO Z REG FAN IN
C2	2C0B2-C0	6-175		D4 BIT 03 TO CHL 4-7 FAN OUT
C3	2C0R2-C1	6-175		
D0	2B2A3-B2	5- 67		
D1	2B2A3-B3	5- 67		NOT RC READ BIT 15
D2	2B1B9-J0	6- 27		D4 BIT 03 TO TYPEWRITER 0 REG
E0	2B2A8-B2	5- 59		
E1	2B2A8-B3	5- 59		NOT RC READ BIT 03
E2	2B2A8-D0	5- 59		
E3	2B2A8-D1	5- 59		NOT D4 BIT 03 TO MCS VIA FI
F0	2B1B9-I0	6- 27		NOT(TWR BIT 03) CONSOLE TO D4
F1	2B1A9-M2	6- 23		D0 BIT 21 TO Z REG FAN IN XLTN
F3	2B1B2-V3	6- 33	2B1B2-RW	NOT(BIT 03 = BIT 09) D4 REG
G1	2B1A5-W0	6- 19		RS 2 CHAR POS. TO D4 BIT 03
G2	2C0B6-J0	6-171		D4 BIT 09 TO CHL 4-7 FAN OUT
G3	2C0B6-J1	6-171		
H0	2A1B5-U2	6- 45		RF SENSE AMP BIT 03 TO D4 REG
H1	2A1B5-U3	6- 45		
H2	2A0A6-J0	6-135		D4 BIT 09 TO CHL 0-3 FAN OUT
H3	2A0A6-J1	6-135		
I0	2A0A4-N0	6-157		
I1	2A0A4-N1	6-157		NOT CHAN 0-3 BIT 03 FI TO D4
I2	2B1A5-X0	6- 19	2B1A4-AO	NOT(RLK 00/01) TO D4 BIT 03
I3	2B1A1-J1	6- 25		SEARCH COMPARE(D4 BIT 03 = D4 BIT 21)
J0	2B2A1-B2	5- 71		
J1	2B2A1-B3	5- 71		NOT RC READ BIT 21
J3	2B1A5-Q2	6- 19	2B1A4-BJ	NOT(CHAR MODE) TO D4 BIT 03
K1	2B1A1-B0	6- 25		SEARCH BFR NOT(BIT 21) TO D4
K2	2B2A6-D0	5- 63		
K3	2B2A6-D1	5- 63		NOT D4 BIT 09 TO MCS VIA FI
L0	2C0A5-N0	6-195		
L1	2C0A5-N1	6-195		NOT CHL 4-7 BIT 15 FI TO D4
L2	2B2A1-D0	5- 71		
L3	2B2A1-D1	5- 71		NOT D4 BIT 21 TO MCS VIA FI
M0	2C0B4-M3	6-193		
M1	2C0R4-M2	6-193		NOT CHL 4-7 BIT 09 FI TO D4
M2	2A0B3-G1	6-129		D4 BIT 15 TO CHAN 0-3 FANOUT
M3	2A0B3-G0	6-129		
N0	2A0A4-M2	6-157		NOT CHAN 0-3 BIT 09 FI TO D4
N1	2A0A4-M3	6-157		
N3	2B1A4-V2	6- 35		(BIT 15 = BIT 21) D4 REG
O0	2B1A5-R2	6- 19		RS 1 CHAR POS. TO D4 BIT 03
O1	2B1B6-K1	6- 15	2B1A4-AQ	INPUT TO D4 TIMING - BIT 03
O2	2B2A3-D0	5- 67		
O3	2B2A3-D1	5- 67		NOT D4 BIT 15 TO MCS VIA FI
P0	2B1A6-Q0	6- 13		NOT(SEARCH DATA) TO D4 BIT 21
P1	2B1B6-M2	6- 15	2B1A4-AR	ENABLE D0 - MCS TO D4 - BIT 03
P2	2C0A3-G1	6-165		D4 BIT 15 TO CHL 4-7 FAN OUT
P3	2C0A3-G0	6-165		
Q0	2A0B5-N0	6-159		
Q1	2A0B5-N1	6-159		NOT CHAN 0-3 BIT 15 FI TO D4
Q2	2R1A5-V0	6- 19	2B1A4-RN	NOT(CHAR-BYTE) TO D4 BIT 03
Q3	2B1A4-S2	6- 35	2B1A4-RX	NOT(BIT 15 = BIT 21) D4 REG
R0	2C0B4-N0	6-193		
R1	2C0R4-N1	6-193		NOT CHL 4-7 BIT 03 FI TO D4
R2	2R1A9-E3	6- 23	2B1A4-RV	ACT, I/O OUTPUT = I/O WRITE
R3	2R1B0-R0	6- 7	2B1A4-RU	NOT (ACT, I/O = BLOCK D4 BIT 21)
S0	2A1A6-L1	6- 49		RF SENSE AMP BIT 09 TO D4 REG
S1	2A1A6-L0	6- 49		
S2	2R1A4-Q3	6- 35	2B1A4-RX	NOT(BIT 15 ≠ BIT 21) D4 REG
S3	2R1A0-L2	6- 5		SUM OF 14/15/20/21= EVEN TOTAL
T0	2A1A7-L3	6- 51		
T1	2A1A7-L2	6- 51		RF SENSE AMP BIT 15 TO D4 REG
T3	2R1B2-N3	6- 33		(BIT 14 = BIT 20) D4 REG
U0	2A1A6-V1	6- 49		
U1	2A1A6-V0	6- 49		D0 BIT 09 TO Z REG FAN IN
U2	2C0A7-L0	6-161		
U3	2C0A7-L1	6-161		D4 BIT 21 TO CHL 4-7 FAN OUT
V0	2A0B5-M3	6-159		
V1	2A0R5-M2	6-159		NOT CHAN 0-3 BIT 21 FI TO D4
V2	2R1A4-N3	6- 35		(BIT 15 = BIT 21) D4 REG
V3	2R1B2-Q3	6- 33	2B1A4-RW	NOT(BIT 14 = BIT 20) D4 REG
W0	2C0A5-M3	6-195		
W1	2C0A5-M2	6-195		NOT CHL 4-7 BIT 21 FI TO D4
W3	2R1A0-B2	6- 5		SUM OF 14/15/20/21= ODD TOTAL
X0	2R2A6-B3	5- 63		NOT RC READ BIT 09
X1	2R2A6-B2	5- 63		
X2	2A0R7-L1	6-125		D4 BIT 21 TO CHL 0-3 FAN OUT
X3	2A0R7-L0	6-125		



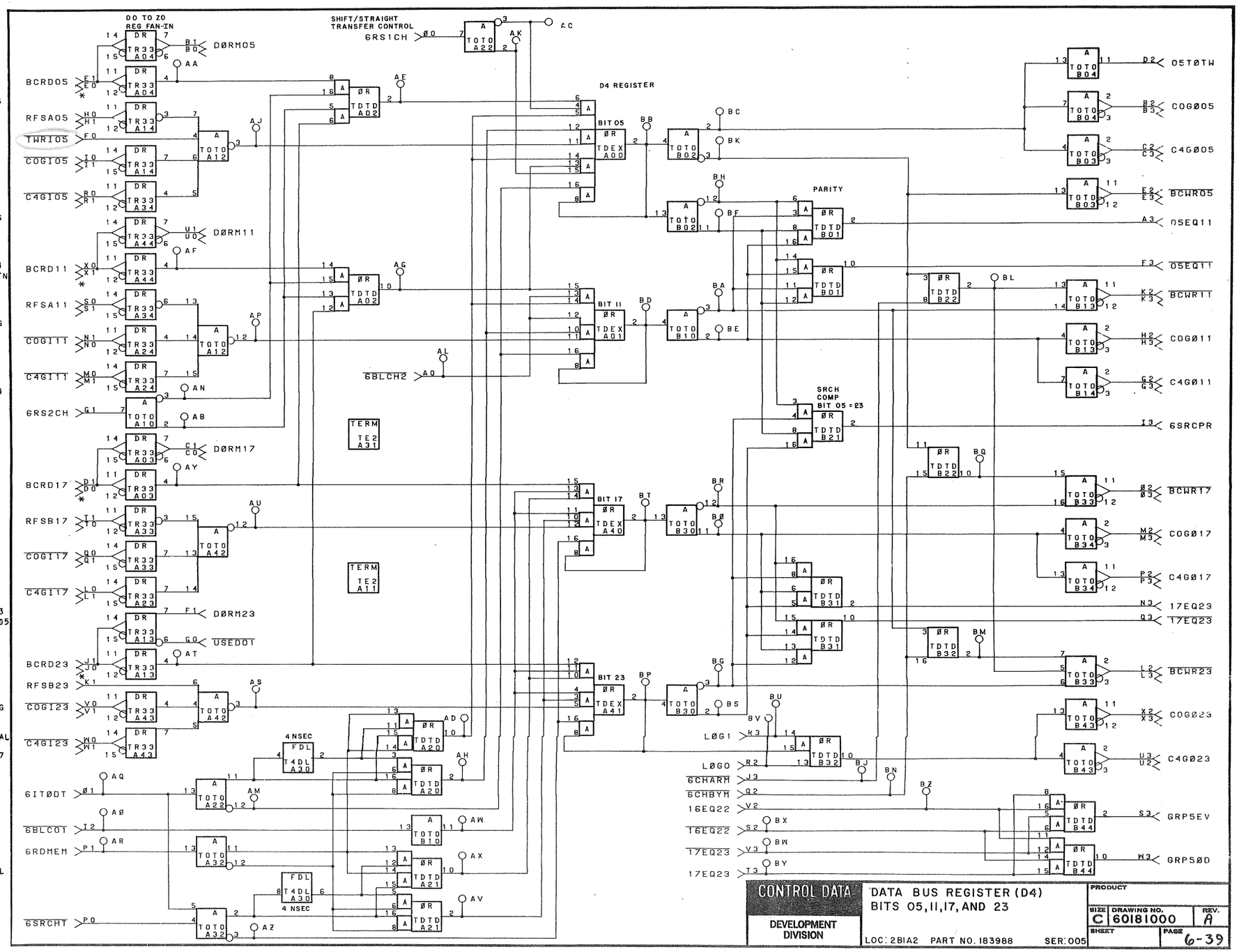
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B1B5-X1	6- 21	2B1A3-AL	NOT(PLK CHAR 02) TO D4 BIT 04
A3	2B1A3-V2	6- 37		BIT 04 = BIT 10 D4 REG
B0	2A1A5-W1	6- 47		
B1	2A1A5-W0	6- 47		D0 BIT 04 TO Z REG FAN IN
B2	2A0A7-D1	6-133		D4 BIT 04 TO CHAN 0-3 FANOUT
B3	2A0A7-D0	6-133		
C0	2A1R8-N1	6- 53		
C1	2A1R8-N0	6- 53		D0 BIT 16 TO Z REG FAN IN
C2	2C0R7-D1	6-169		D4 BIT 04 TO CHL 4-7 FAN OUT
C3	2C0R7-D0	6-169		
D0	2B2A3-M2	5- 67		
D1	2B2A3-M3	5- 67		NOT RC READ BIT 16
D2	2B1B9-N0	6- 27		D4 BIT 04 TO TYPEWRITER 0 REG
E0	2B2A8-M2	5- 59		
E1	2B2A8-M3	5- 59		NOT RC READ BIT 04
E2	2B2A8-D0	5- 59		
E3	2B2A8-D1	5- 59		NOT D4 BIT 04 TO MCS VIA FI
F0	2B1B9-V0	6- 27		NOT(TWR BIT 04) CONSOLE TO D4
F1	2B1A9-M3	6- 23		D0 BIT 22 TO Z REG FAN IN XLTN
F3	2B1A3-S2	6- 37	2B1A3-RX	NOT(BIT 04 = BIT 10) D4 REG
G1	2B1B5-D3	6- 21		RS 2 CHAR POS. TO D4 BIT 04
G2	2C0R3-J0	6-173		D4 BIT 10 TO CHL 4-7 FAN OUT
G3	2C0R3-J1	6-173		
H0	2A1A5-J0	6- 47		RF SENSE AMP BIT 04 TO D4 REG
H1	2A1A5-J1	6- 47		
H2	2A0A3-J0	6-137		D4 BIT 10 TO CHL 0-3 FAN OUT
H3	2A0A3-J1	6-137		
I0	2A0A4-L0	6-157		
I1	2A0A4-L1	6-157		NOT CHAN 0-3 BIT 04 FI TO D4
I2	2B1B5-U1	6- 21	2B1A3-AO	NOT(CLK 00/01) TO D4 BIT 04 ,
I3	2B1A1-K1	6- 25		SEARCH COMPARE(D4 BIT 04 = D4 BIT 22)
J0	2B2A1-M2	5- 71		
J1	2B2A1-M3	5- 71		NOT RC READ BIT 22
J3	2B1B5-V1	6- 21	2B1A3-RJ	NOT(CHAR MODE) TO D4 BIT 04
K1	2B1A1-J0	6- 25		SEARCH BFR NOT(BIT 22) TO D4
K2	2B2A6-00	5- 63		
K3	2B2A6-01	5- 63		NOT D4 BIT 10 TO MCS VIA FI
L0	2C0A5-L0	6-195		
L1	2C0A5-L1	6-195		NOT CHL 4-7 BIT 16 FI TO D4
L2	2B2A1-00	5- 71		
L3	2B2A1-01	5- 71		NOT D4 BIT 22 TO MCS VIA FI
M0	2C0B4-K2	6-193		
M1	2C0R4-K3	6-193		NOT CHL 4-7 BIT 10 FI TO D4
M2	2A0R2-W3	6-131		D4 BIT 16 TO CHL 0-3 FAN OUT
M3	2A0R2-W2	6-131		
N0	2A0A4-K3	6-157		NOT CHAN 0-3 BIT 10 FI TO D4
N1	2A0A4-K2	6-157		
N3	2B1A2-V2	6- 39		(BIT 16 = BIT 22) D4 REG
O0	2B1B5-W1	6- 21		RS 1 CHAR POS. TO D4 BIT 04
O1	2B1R6-L0	6- 15	2B1A3-AQ	INPUT TO D4 TIMING - BIT 04
O2	2B2A3-00	5- 67		
O3	2B2A3-01	5- 67		NOT D4 BIT 16 TO MCS VIA FI
P0	2B1A6-W1	6- 13		NOT(SEARCH DATA) TO D4 BIT 22
P1	2B1R6-M3	6- 15	2B1A3-AR	ENABLE D0 + MCS TO D4 - BIT 04
P2	2C0A2-W3	6-167		D4 BIT 16 TO CHL 4-7 FAN OUT
P3	2C0A2-W2	6-167		
Q0	2A0R5-L0	6-159		
Q1	2A0R5-L1	6-159		NOT CHAN 0-3 BIT 16 FI TO D4
Q2	2B1R5-P3	6- 21	2B1A3-RN	NOT(CHAR+BYTE TO D4 BIT 04
Q3	2B1A2-S2	6- 39	2B1A2-RX	NOT(BIT 16 = BIT 22) D4 REG
R0	2C0R4-L0	6-193		
R1	2C0R4-L1	6-193		NOT CHL 4-7 BIT 04 FI TO D4
R2	2B1A9-E2	6- 23	2B1A3-RV	ACT. I/O INPUT - I/O READ
R3	2B1R0-R1	6- 7	2B1A3-RU	NOT (ACT. I/O - BLOCK D4 BIT 22)
S0	2A1A6-I2	6- 49		RF SENSE AMP BIT 10 TO D4 REG
S1	2A1A6-I3	6- 49		
S2	2B1A3-F3	6- 37	2B1A3-RX	NOT(BIT 04 = BIT 10) D4 REG
S3	2B1R0-B3	6- 7		SUM OF 04/05/10/11= EVEN TOTAL
T0	2A1R8-L0	6- 53		
T1	2A1R8-L1	6- 53		RF SENSE AMP BIT 16 TO D4 REG
T3	2B1A2-A3	6- 39		(BIT 05 = BIT 11) D4 REG
U0	2A1A6-U3	6- 49		
U1	2A1A6-U2	6- 49		D0 BIT 10 TO Z REG FAN IN
U2	2C0A6-L0	6-163		
U3	2C0A6-L1	6-163		D4 BIT 22 TO CHL 4-7 FAN OUT
V0	2A0R5-K2	6-159		
V1	2A0R5-K3	6-159		NOT CHAN 0-3 BIT 22 FI TO D4
V2	2B1A3-A1	6- 37		BIT 04 = BIT 10 D4 REG
V3	2B1A2-F3	6- 39	2B1A3-RW	NOT(BIT 05 = BIT 11) D4 REG
W0	2C0A5-K2	6-195		
W1	2C0A5-K3	6-195		NOT CHL 4-7 BIT 22 FI TO D4
W3	2B1A0-G2	6- 7		SUM OF 04/05/10/11= ODD TOTAL
X0	2B2A6-M2	5- 63		NOT RC READ BIT 10
X1	2B2A6-M3	5- 63		
X2	2A0R6-L1	6-127		D4 BIT 22 TO CHL 0-3 FAN OUT
X3	2A0R6-L0	6-127		



CONTROL DATA CORPORATION	DATA BUS REGISTER (D4) BITS 04,10,16, AND 22	PRODUCT
DEVELOPMENT DIVISION	LOC: 2B1A3 PART NO. 183988 SER: 004	SIZE C | DRAWING NO. 60181000 | REV. H
		SHEET | PAGE 6-37

PIN	ORIGIN/ DEST,	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2R1A5-U1	6- 19	2B1A2-AL	NOT(RLK CHAR 02) TO D4 BIT 05
A3	2R1A3-T3	6- 37		(BIT 05 = BIT 11) D4 REG
B0	2A1A5-V1	6- 47		
B1	2A1A5-V0	6- 47		D0 BIT 05 TO Z REG FAN IN
B2	2A0A6-D1	6-135		D4 BIT 05 TO CHL 0-3 FAN OUT
B3	2A0A6-D0	6-135		
C0	2A1B8-U1	6- 53		
C1	2A1B8-U0	6- 53		D0 BIT 17 TO Z REG FAN IN
C2	2C0B6-D1	6-171		D4 BIT 05 TO CHL 4-7 FAN OUT
C3	2C0B6-D0	6-171		
D0	2B2A3-T2	5- 67		
D1	2B2A3-T3	5- 67		NOT BC READ BIT 17
D2	2B1B9-T0	6- 27		D4 BIT 05 TO TYPEWRITER 0 REG
E0	2B2A8-T2	5- 59		
E1	2B2A8-T3	5- 59		NOT BC READ BIT 05
E2	2B2A8-Q1	5- 59		
E3	2B2A8-Q0	5- 59		NOT D4 BIT 05 TO MCS VIA FI
F0	2B1B9-U0	6- 27		NOT(TWR BIT 05) CONSOLE TO D4
F1	2R1A9-Q2	6- 23		D0 BIT 23 TO Z REG FAN IN XLTN
F3	2B1A3-V3	6- 37	2B1A3-RW	NOT(BIT 05 = BIT 11) D4 REG
G1	2B1A5-W1	6- 19		RS 2 CHAR POS. TO D4 BIT 05
G2	2C0B2-J0	6-175		D4 BIT 11 TO CHL 4-7 FAN OUT
G3	2C0B2-J1	6-175		
H0	2A1A5-L1	6- 47		RF SENSE AMP BIT 05 TO D4 REG
H1	2A1A5-L0	6- 47		
H2	2A0A2-J0	6-139		D4 BIT 11 TO CHL 0-3 FAN OUT
H3	2A0A2-J1	6-139		
I0	2A0A4-M1	6-157		
I1	2A0A4-M0	6-157		NOT CHAN 0-3 BIT 05 FI TO D4
I2	2B1A5-X1	6- 19	2B1A2-AO	NOT(RLK DD/01) TO D4 BIT 05
I3	2B1A1-K0	6- 25		SEARCH COMPARE(D4 BIT 05 = D4 BIT 23)
J0	2B2A1-T2	5- 71		
J1	2B2A1-T3	5- 71		NOT BC READ BIT 23
J3	2B1A5-P3	6- 19	2B1A2-BJ	NOT(CHAR MODE) TO D4 BIT 05
K1	2B1A1-A0	6- 25		SEARCH BFR NOT(BIT 23) TO D4
K2	2B2A6-Q1	5- 63		
K3	2B2A6-Q0	5- 63		NOT D4 BIT 11 TO MCS VIA FI
L0	2C0A5-M1	6-195		
L1	2C0A5-M0	6-195		NOT CHL 4-7 BIT 17 FI TO D4
L2	2B2A1-Q1	5- 71		
L3	2B2A1-Q0	5- 71		NOT D4 BIT 23 TO MCS VIA FI
M0	2C0B4-L2	6-193		
M1	2C0B4-L3	6-193		NOT CHL 4-7 BIT 11 FI TO D4
M2	2A0B7-G1	6-125		D4 BIT 17 TO CHAN 0-3 FANOUT
M3	2A0B7-G0	6-125		
N0	2A0A4-L3	6-157		NOT CHAN 0-3 BIT 11 FI TO D4
N1	2A0A4-L2	6-157		
N3	2B1A2-T3	6- 39		(BIT 17 = BIT 23) D4 REG
O0	2R1A5-O3	6- 19		RS 1 CHAR POS. TO D4 BIT 05
O1	2B1B6-M1	6- 15	2B1A2-AQ	INPUT TO D4 TIMING - BIT 05
O2	2B2A3-Q1	5- 67		
O3	2B2A3-Q0	5- 67		NOT D4 BIT 17 TO MCS VIA FI
P0	2B1A6-W2	6- 13		NOT(SEARCH DATA) TO D4 BIT 23
P1	2B1B6-O3	6- 15	2B1A2-AR	ENABLE D0 - MCS TO D4 - BIT 05
P2	2C0A7-G1	6-161		D4 BIT 17 TO CHL 4-7 FAN OUT
P3	2C0A7-G0	6-161		
Q0	2A0B5-M1	6-159		
Q1	2A0B5-M0	6-159		NOT CHAN 0-3 BIT 17 FI TO D4
Q2	2B1A5-V1	6- 19	2B1A2-RN	NOT(CHAR-BYTE) TO D4 BIT 05
Q3	2B1A2-V3	6- 39	2B1A2-RW	NOT(BIT 17 = BIT 23) D4 REG
R0	2C0B4-M1	6-193		
R1	2C0B4-M0	6-193		NOT CHL 4-7 BIT 05 FI TO D4
S0	2A1A6-L2	6- 49		RF SENSE AMP BIT 11 TO D4 REG
S1	2A1A6-L3	6- 49		
S2	2B1A3-Q3	6- 37	2B1A2-RX	NOT(BIT 16 = BIT 22) D4 REG
S3	2R1A0-B3	6- 5		SUM OF 16/17/22/23= EVEN TOTAL
T0	2B1A0-B0	6- 5		
T1	2B1A0-B1	6- 5		REG, FILE TO D4 REG, = BIT 17
T3	2B1A2-N3	6- 39		(BIT 17 = BIT 23) D4 REG
U0	2A1A6-V3	6- 49		
U1	2A1A6-V2	6- 49		D0 BIT 11 TO Z REG FAN IN
U2	2C0A3-W2	6-165		
U3	2C0A3-W3	6-165		D4 BIT 23 TO CHAN 4-7 FANOUT
V0	2A0B5-L2	6-159		
V1	2A0B5-L3	6-159		NOT CHAN 0-3 BIT 23 FI TO D4
V2	2R1A3-N3	6- 37		(BIT 16 = BIT 22) D4 REG
V3	2R1A2-Q3	6- 39	2B1A2-RW	NOT(BIT 17 = BIT 23) D4 REG
W0	2C0A5-L2	6-195		
W1	2C0A5-L3	6-195		NOT CHL 4-7 BIT 23 FI TO D4
W3	2R1A0-G2	6- 5		SUM OF 16/17/22/23= ODD TOTAL
X0	2R2A6-T3	5- 63		NOT BC READ BIT 11
X1	2R2A6-T2	5- 63		
X2	2A0B3-W3	6-129		D4 BIT 23 TO CHL 0-3 FAN OUT
X3	2A0B3-W2	6-129		

PAGE 6- 39



223

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A1B6-V2	6- 43		NOT (BC FCN CODE = 72)
A3	2A1B8-H0	6- 53	2A1B7-RA	Z REG BIT 17 TO DIGIT FAN OUT
B0	2A1A8-R3	6- 55		NOT(F REG TO Z REG) TO FAN OUT
B1	2A1A4-E3	6- 59		BC FCN CODE = 72
B2	2A1A0-V0	6- 83		
B3	2A1A0-V1	6- 83		DIGIT DRIVE 17 TO RF 40-77
C0	2A1A0-R1	6- 81		DIGIT DRIVE 19 TO RF 40-77
C1	2A1A0-R0	6- 81		
C2	2A1A2-V1	6- 71		DIGIT DRIVE 17 TO RF 00-37
C3	2A1A2-V0	6- 71		
D0	2A1A8-Q0	6- 55		NOT(CLOCK CONTROL) TO FAN OUT
D1	2A1B6-K0	6- 43		CLOCK CONT TO Z REG CONTROL
D2	2B1B7-S0	6- 3		T151
D3	2B1B7-S1	6- 3		
E0	2B1A1-W3	6- 25		
E1	2B1A1-W2	6- 25		CLOCK CONTROL XLTN
E3	2A1B8-X1	6- 53	2A1B7-RE	Z REG BIT 18 TO DIGIT FAN OUT
F0	2B1B1-W0	6- 9		
F1	2B1B1-W1	6- 9		NOT(F = 72)
F2	2A1A2-S0	6- 69		
F3	2A1A2-S1	6- 69		DIGIT DRIVE 18 TO RF 00-37
G0	2A1A2-R1	6- 69		DIGIT DRIVE 19 TO RF 00-37
G1	2A1A2-R0	6- 69		
G2	2A1A0-S1	6- 81		DIGIT DRIVE 18 TO RF 40-77
G3	2A1A0-S0	6- 81		
H0	2B1A6-R0	6- 13		DO TO Z REG ENABLE TO FAN OUT
H1	2B1A6-R1	6- 13		
H2	2A1B6-I3	6- 43		T151 TO RF WRITE F/F
H3	2A1B6-O3	6- 43		NOT(DO BIT 01) TO WORD MOVE TRANSLATION
I0	2A1A4-S1	6- 59	2A1B7-AF	NOT(S REG BUSY) = EN TIMING CHAIN START
I1	2A1B8-W1	6- 53	2A1B7-AE	Z REG BIT 19 TO DIGIT FAN OUT
I2	2A1B5-F1	6- 45		DO BIT 01 TO Z REG BIT 01
I3	2A1B6-N2	6- 43		NOT(DO BIT 0) TO WORD MVE XLTN
J0	2B1B7-S3	6- 3		
J1	2B1B7-S2	6- 3		NORMAL TIMING SEL, TO Z PANEL
J2	2B1B1-R0	6- 9		T152
J3	2B1B1-R1	6- 9		
K0	2B1B7-V2	6- 3		FAST TIMING SELECT TO Z PANEL
K1	2B1B7-U3	6- 3		
K2	2A1B5-B0	6- 45		DO BIT 00 TO Z REG BIT 00
L0	2B1A1-R3	6- 25		T150
L1	2B1A1-R2	6- 25		
L2	2B1B4-B0	6- 29		
L3	2B1B4-B1	6- 29		DO BIT 00 TO Z REG FAN IN
M0	2A1B6-I2	6- 43		NOT(T150) TO USE S03 F/F XLTN
M2	2B1B3-B1	6- 31		DO BIT 01 TO Z REG FAN IN
M3	2B1B3-B0	6- 31		
N1	2A1B6-A3	6- 43	2A1B7-AG	ENABLE TIMING CHAIN START XLTN
O0	2A1B6-J3	6- 43		T150 TO SET S BUSY/INP TO Z XLTN
O2	2B1A8-P0	6- 17		T154
O3	2B1A8-P1	6- 17		
P0	2A1B6-A0	6- 43	2A1B7-AO	EN T153 TO T154 XLTN TO TIMING CHAIN
P2	2B1B7-E2	6- 3		
P3	2B1B7-E3	6- 3		T154
Q1	2A1B4-A0	6- 57	2A1B7-AR	NOT(T158) TO CLEAR T157
R0	2A1B6-G1	6- 43	2A1B7-AS	EN T155 TO T156 XLTN TO TIMING CHAIN
R1	2A1B5-V3	6- 45	2A1B7-AV	WORD ADDR BIT 00 TO PF XMTR
R2	2A1B6-K2	6- 43		T154 TO USE S03 FF = INPUT TO Z XLTN
S0	2B1B1-X1	6- 9		
S1	2B1B1-X0	6- 9		T153
S2	2B1B7-M0	6- 3		T155
S3	2B1B7-M1	6- 3		
T1	2A1B6-R0	6- 43		T156 TO SET S03 AND INPUT TO Z XLTN
U0	2A2A8-V3	5- 9		
U1	2A2A8-V2	5- 9		BC S BUS BIT 00 TO PAGE FILE
U2	2A1B6-F3	6- 43		T155 TO PF REQUEST XLTN
V0	2B1B7-X0	6- 3		T156
V1	2B1B7-X1	6- 3		
V2	2A1B4-R3	6- 57		NOT (T154) TO CHAR, AND WRITE STORAGE FFS
V3	2A1B6-G2	6- 43		T154 TO PF REQUEST XLTN
W1	2A1B5-M3	6- 45	2A1B7-AZ	WORD ADDR BIT 01 TO PF XMTR
W2	2A1B6-K3	6- 43		T157 TO RF WRITE AND S/M FFS
W3	2A1B6-F0	6- 43		NOT(T157) TO BC PAGE FILE F/FS
X0	2A2A9-V3	5- 11		
X1	2A2A9-V2	5- 11		BC S BUS BIT 01 TO PAGE FILE
X2	2B1A8-U3	6- 17		
X3	2B1A8-U2	6- 17		T157

PAGE 6- 41

Pg 6-59
Pg 6-43

TCEN1A
TCEN1B
DTØZEN
BCTX72
DØRMOO
DØRMO1
TCEN2
ADDS00
ADDS01
TØDD17
TØDD18
TØDD19
TCEN3
RFFAST
RFNØRM
CLKBFR
RT158A
1CLK
TCLK
BCSB00
BCSB01
DRFU17
DRFL17
DRFU18
DRFL18
DRFU19
DRFL19
FTØZ
BCFN72
DØHOO
DØMO1
DØMOT
RT150
LT150
USED01
USED02
RT151
LT151
USED03
USED05
RT152
USED06
USED07
USED08
USED09
USED04
RT154
LT154S
USED11
USED13
USED14
RT153
LØG1
RT154A
RT154B
LT154
USED10
RT155
USED16
USED18
LT155
RT157
LT157
RT156
LT156
USED19
USED22
14,5 NSEC
17,5 NSEC
13 NSEC
16 NSEC
4 NSEC

Pg 6-43
Pg 6-57

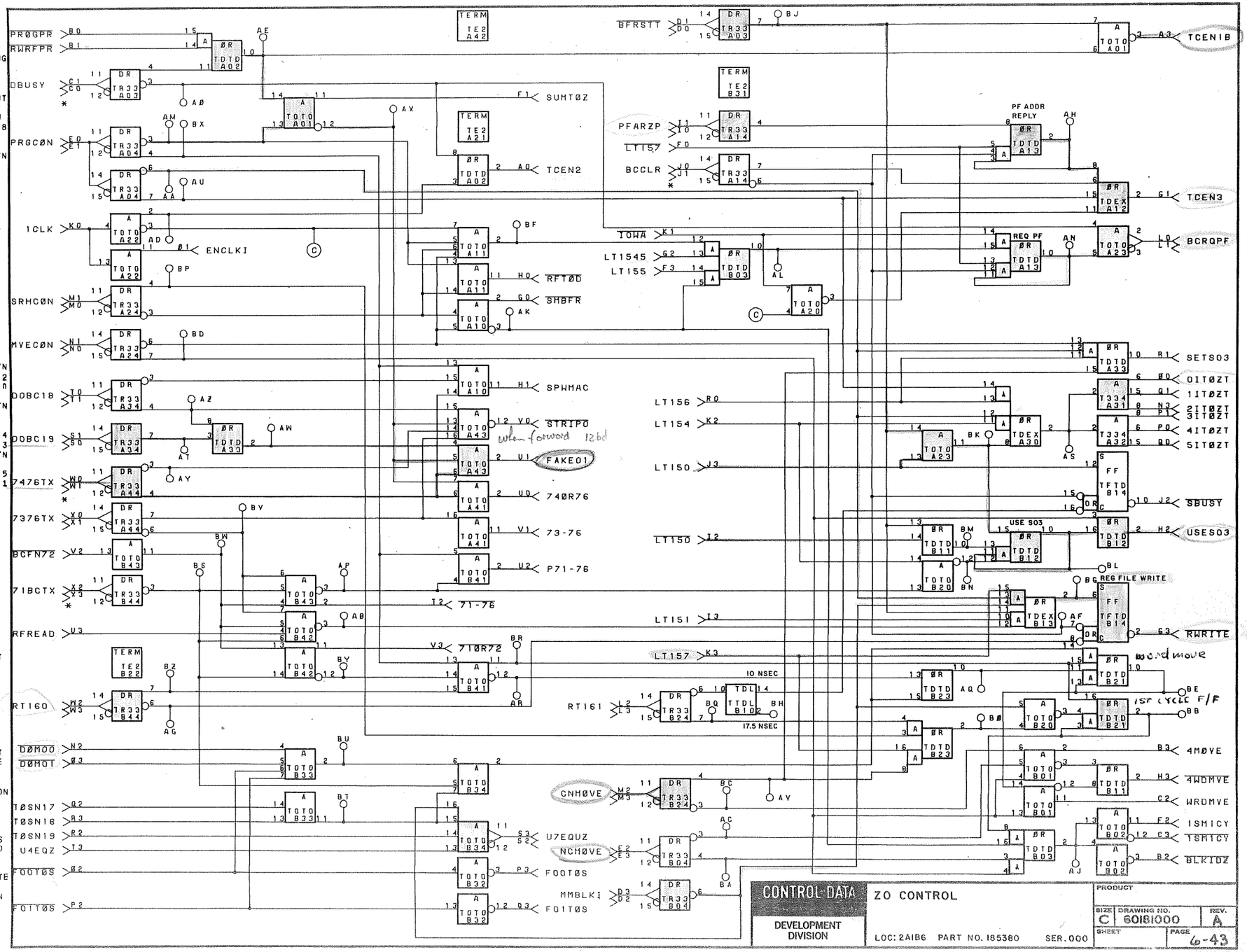
2 Reg Bit 19 fan out

CONTROL DATA	TIMING CHAIN T150-T157	PRODUCT
DEVELOPMENT DIVISION	LOC: 2A1B7 PART NO. 184854 SER,000	SIZE C · DRAWING NO. 60181000 · REV. A · SHEET · PAGE 6-41

225

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A187-P0	6- 41	2A187-A0	EN T153 TO T154 XLTN TO TIMING CHAIN
A3	2A187-N1	6- 41	2A187-AG	ENABLE TIMING CHAIN START XLTN
B0	2A1A4-M3	6- 59		NOT(PROGRAM OPR, XLTN)-Z CONT
B1	2A1A4-D3	6- 59		NOT (READ/WRITE RF XLTN) - Z CONTROL
B2	2A184-A3	6- 57		NOT (S/M FIRST CYCLE) - BLOCK INT CODE 4
B3	2A188-D0	6- 53		MOVE DECR RF U7 XLTN TO GR 4
C0	2R1A8-X2	6- 17		
C1	2R1A8-X3	6- 17		NOT BC DATA REG BUSY
C2	2A184-D1	6- 57		WORD MOVE TO INCR/PART, WRITE XLTN
C3	2A185-D1	6- 45		NOT (S/M FIRST CYCLE) - BLOCK INT CODE 1
D0	2R1A1-S3	6- 25		NOT READY/BC START EN
D1	2R1A1-S2	6- 25		
D2	2R1A8-V2	6- 17		
D3	2R1A8-V3	6- 17		MAINT MODE BLOCK RF INCREMENT
E0	2R1A1-V2	6- 25		PROGRAM CONTROL XLTN
E1	2R1A1-V3	6- 25		
E2	2R1A6-N2	6- 13		NON-CONSECUTIVE MOVE CYCLE
E3	2R1A6-N3	6- 13		
F0	2A187-W3	6- 41		NOT(T157) TO BC PAGE FILE F/FS

F1	2A1A8-D2	6- 55			SUM TO Z XLTN TO FAN OUT
F2	2A1B5-K0	6- 45			S/M FIRST CYCLE-EN RF SENSE AMPL 00
F3	2A1B7-U2	6- 41			T155 TO PF REQUEST XLTN
G0	2A1A6-L0	6- 55			NOT (S/M BFR XLTN) TO FAN OUT
G1	2A1B7-R0	6- 41	2A1B7-AS		EN T155 TO T156 XLTN TO TIMING CHAIN
G2	2A1B7-V3	6- 41			T154 TO PF REQUEST XLTN
G3	2A1A4-V0	6- 59	2A1A4-AU		NOT(WRITE REGISTER FILE F/F)
H0	2A1A6-X3	6- 55			NOT(ENABLE RF TO D4) TO FANOUT
H1	2A1B4-O3	6- 57			SUPPR WORD MARK ON I/O ACT,
H2	2A1A4-N1	6- 59			USE S REG BIT 03 = WRITE XLTN
H3	2A1B8-X2	6- 53	2A1B8-RU		NOT(WORD MOVE) = BLK SUM 17/18
I0	2R1A8-F1	6- 17			
I1	2R1A8-F0	6- 17			PAGE FILE ADDRESS REPLY TO Z
I2	2A1B7-H0	6- 41			NOT(T150) TO USE S03 F/F XLTN
I3	2A1B7-W2	6- 41			T151 TO RF WRITE F/F
J0	2R1B1-D1	6- 9			NOT RC CLEAR
J1	2R1B1-D0	6- 9			
J2	2A1A4-V3	6- 59			NOT(ADDRESS BUSY) TO S REG
J3	2A1B7-O0	6- 41			T150 TO SET S BUSY/INP TO Z XLTN
K0	2A1B7-D1	6- 41			CLOCK CONT TO Z REG CONTROL
K1	2A1B4-P1	6- 57			NOT (I/O WITH A XLTN) TO CONT
K2	2A1B7-R2	6- 41			T154 TO USE S03 FF = INPUT TO Z XLTN
K3	2A1B7-W2	6- 41			T157 TO RF WRITE AND S/M FFS
L0	2A2A6-C1	5- 1			RC PAGE FILE REQUEST
L1	2A2A6-C0	5- 1			
L2	2R1A7-S1	6- 1			T161 TO Z PANEL = CLR S BUSY
L3	2R1A7-S0	6- 1			
M0	2R1A1-U2	6- 25			
M1	2R1A1-U3	6- 25			SEARCH CONTROL XLTN
M2	2R1A6-K3	6- 13			CONSECUTIVE MOVE CYCLE
M3	2R1A6-K2	6- 13			
N0	2R1A1-Q2	6- 25			
N1	2R1A1-Q3	6- 25			MOVE CONT XLTN TO Z
N2	2A1B7-I3	6- 41			NOT(DO BIT 0) TO WORD MVE XLTN
N3	2A1A6-P2	6- 49			INPUT TO Z REG TIMING =GROUP 2
O0	2A1B5-W1	6- 45			INPUT TO Z REG TIMING =GROUP 0
O1	2A1B4-D0	6- 57			EN CLOCK INTERRUPT
O2	2A1B5-E0	6- 45			NOT(F BIT 00) TO WORD MVE XLTN
O3	2A1B7-H3	6- 41			NOT(DO BIT 01) TO WORD MOVE TRANSLATION
P0	2A1B8-X3	6- 53			INPUT TO Z REG TIMING =GROUP 4
P1	2A1A7-P2	6- 51			INPUT TO Z REG TIMING =GROUP 3
P2	2A1B5-K1	6- 45			NOT(F BIT 01) TO WORD MVE XLTN
P3	2A1A4-B3	6- 59			F BIT 00 TO S REG FAN IN
Q0	2A1A8-B3	6- 55			INPUT TO Z REG TIMING =GROUP 5
Q1	2A1A5-P2	6- 47			INPUT TO Z REG TIMING =GROUP 1
Q2	2A1B8-G0	6- 53			NOT (Z REG BIT 17) TO SENSE EQUAL Z
Q3	2A1A4-F2	6- 59			F BIT 01 TO S REG FAN IN
R0	2A1B7-T1	6- 41			T156 TO SET S03 AND INPUT TO Z XLTN
R1	2A1A4-N3	6- 59	2A1A4-BP		SET S REG BIT 03 = BFR XLTN
R2	2A1B8-W0	6- 53			NOT (Z REG BIT 19) TO SENSE EQUAL Z
R3	2A1B8-X0	6- 53			NOT (Z REG BIT 18) TO SENSE EQUAL Z
S0	2A1A06P05C-04 1A4A06J14C-04 1B0B8-01	2- 11			
S1	2A1A06P05C-03 1A4A06J14C-03 1B0B8-00	2- 11			DO TO BLOCK CONT, BIT 19
S2	2R1A6-F2	6- 13			
S3	2R1A6-F3	6- 13			Z UPPER 7 = ZERO TO MOVE CONT
T0	2A1A06P05C-01 1A4A06J14C-01 1B0B8-T1	2- 11			DO TO BLOCK CONT, BIT 18
T1	2A1A06P05C-02 1A4A06J14C-02 1B0B8-T0	2- 11			
T2	2A1A4-F3	6- 59	2A1A4-RX		NOT (F = 71 THROUGH 76) TO S INPUT TRANSLATION
T3	2A1A8-X2	6- 55			Z UPPER 4 EQUAL ZERO
U0	2A1A8-Q0	6- 55			F=74 + 76 TO LS2 XLTN FAN=OUT
U1	2A1B5-O0	6- 45			FORCE BIT 01 TO Z ON ACTIVATE
U2	2A1A4-X0	6- 59	2A1A4-AX		F=71 THRU 76 TO EN RF WRITE CONTROL BITS
U3	2A1B8-J1	6- 53			RF READ XLTN ON PROG OPERATION
V0	2A1B5-M0	6- 45			NOT (BLOCK BIT 00 TO Z ON ACT,)
V1	2A1B6-I3	6- 53			F=73 THRU 76 TO CHL SEL XLTN
V2	2A1B7-A0	6- 41			NOT (BC FCN CODE = 72)
V3	2A1A4-Q1	6- 59	2A1A4-AK		NOT(F=71+72) TO S INPUT XLTNS
W0	2R1A9-S1	6- 23			NOT FCN CODE=74+76=ADDRESS TO Z LS2
W1	2R1A9-S0	6- 23			
W2	2R1A7-J2	6- 1			T160 TO Z PANEL = CLR RF WRITE
W3	2R1A7-J3	6- 1			
X0	2R1A9-E1	6- 23			FCN CODE = 73 = 76 TIMED XLTN
X1	2R1A9-E0	6- 23			
X2	2R1B1-T0	6- 9			NOT(F=71)
X3	2R1B1-T1	6- 9			



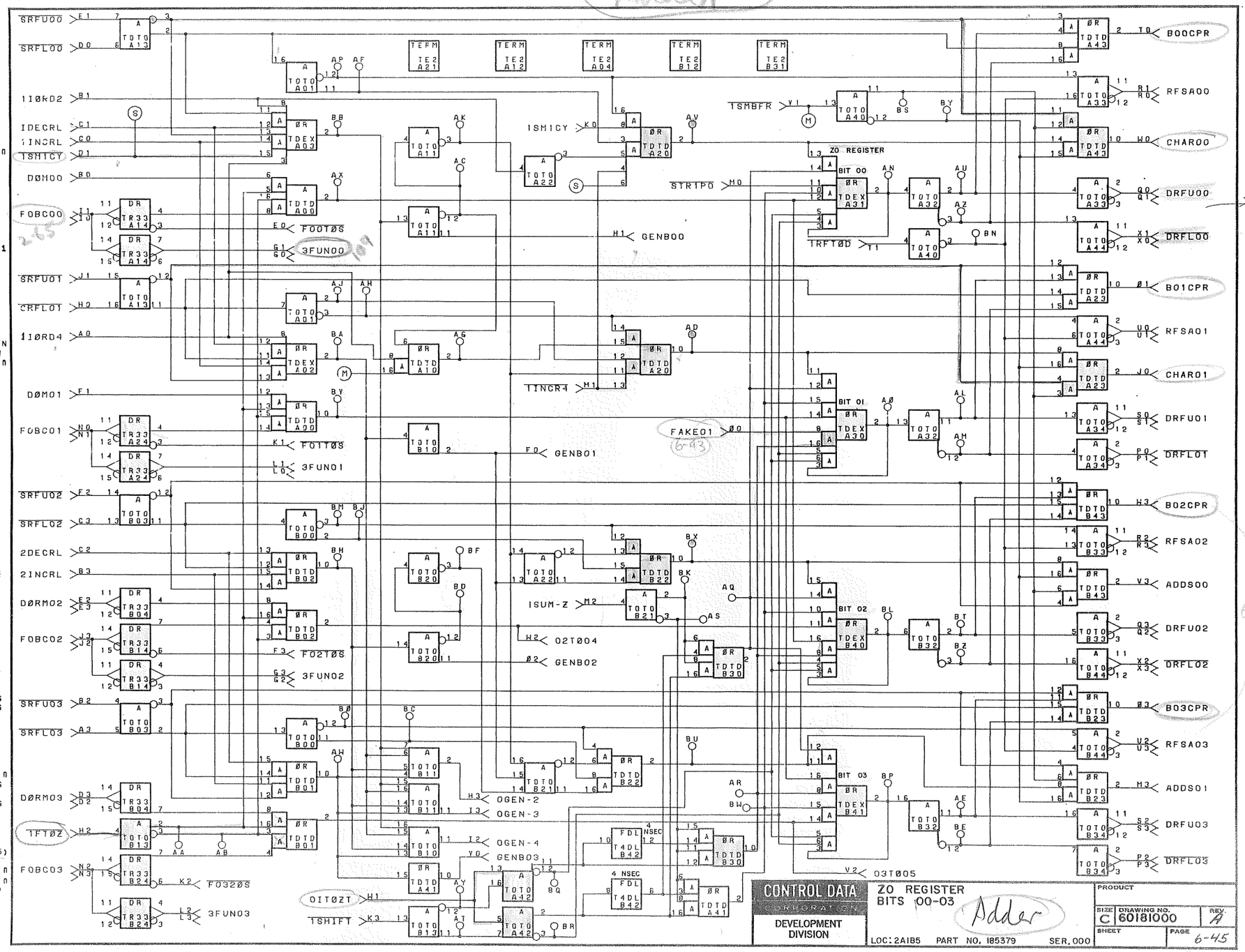
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A1B4=C0	6= 57		INCR + DECR BY 4 TO GRP 0
A3	2A1B3=X0	6= 65		SENSE RF 00=37 NOT(BIT 03)
B0	2A1B7=K2	6= 41		DO BIT 00 TO Z REG BIT 00
B1	2A1R4=H1	6= 57		INCR OR DECR BY 2 TO GROUP 0
B2	2A1B1=X0	6= 77		SENSE RF 40=77 NOT(BIT 03)
B3	2A1R4=S3	6= 57		INCREMENT RF L17 TO BITS 02/03
C0	2A1R4=Q2	6= 57		INCREMENT RF L17 TO BITS 00/01
C1	2A1R4=R2	6= 57		DECREMENT RF L17 TO BITS 00/01
C2	2A1B4=S2	6= 57		DECREMENT RF L17 TO BITS 02/03
C3	2A1B3=S1	6= 65		SENSE RF 00=37 NOT(BIT 02)
D0	2A1B3=T1	6= 65		SENSE RF 00=37 NOT(BIT 00)
D1	2A1B6=C3	6= 43		NOT (S/M FIRST CYCLE) + BLOCK INT CODE 1
D2	2B1A4=B0	6= 35		
D3	2B1A4=B1	6= 35		DO BIT 03 TO Z REG FAN IN
E0	2A1B6=Q2	6= 43		NOT(F BIT 00) TO WORD MVE XLTN

Server A → Increment by +1 into 20-RF

Adder

Increments 1, 2 or 4

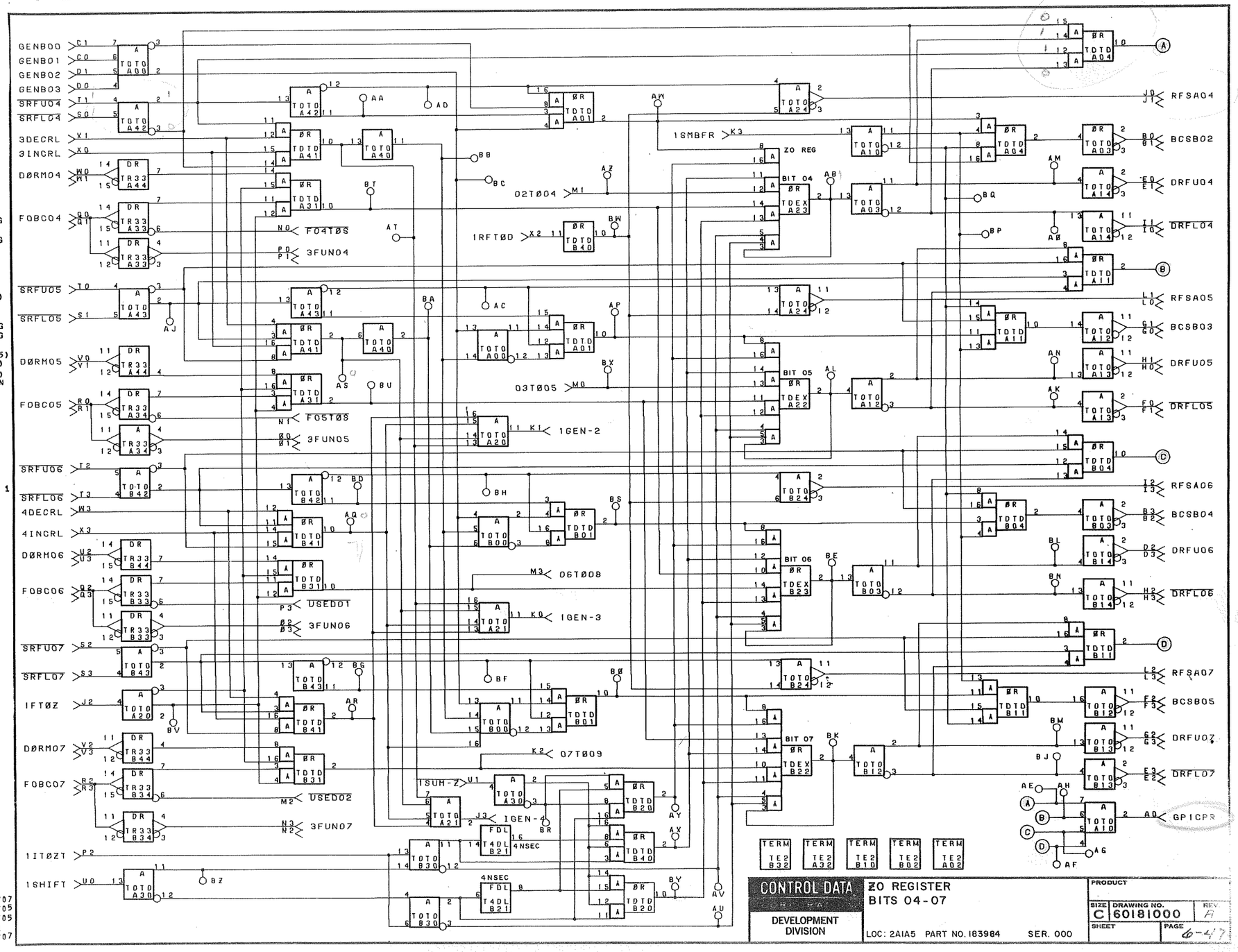
E1	2A1R1=T1	6= 77		SENSE RF 40=77 NOT(BIT 00)
E2	2R1R2=B1	6= 33		NO BIT 02 TO Z REG FAN=IN
E3	2R1R2=B0	6= 33		
F0	2A1A5=C0	6= 47		BIT 01 GENERATE TO GROUP 1
F1	2A1R7=I2	6= 41		NO BIT 01 TO Z REG BIT 01
F2	2A1R1=S1	6= 77		SENSE RF 40=77 NOT(BIT 02)
F3	2A1A4=A3	6= 59		NOT(F BIT 02) TO S REG FAN IN
G0	2R0A8=D0	6=109		
G1	2R0A8=D1	6=109		F BIT 00 TO STATUS COMPARE
G2	2R0A7=R3	6=117		
G3	2R0A7=R2	6=117		F BIT 02 TO STATUS COMPARE
H0	2A1B3=S0	6= 65		SENSE RF 00=37 NOT(BIT 01)
H1	2A1A5=C1	6= 47		BIT 00 GENERATE TO GROUP 1
H2	2A1A8=V3	6= 55		NOT(F0 TO Z FAN IN) TO GROUP 0
H3	2A1A6=C1	6= 49		GROUP 0 GENERATE TO GROUP 2
I0	2A1A06P02D=02 1A4A06J06D=02			
	1A0B8=B1	2= 65		
I1	2A1A06P02D=01 1A4A06J06D=01			F0 REGISTER BIT 0
	1A0B8=B0	2= 65		
I2	2A1B8=A0	6= 53		GROUP 0 GENERATE TO GROUP 4
I3	2A1A7=C1	6= 51		GROUP 0 GENERATE TO GROUP 3
J0	2A1B4=P3	6= 57		CHARACTER ADDRESS DESIGNATOR 1
J1	2A1B1=S0	6= 77		SENSE RF 40=77 NOT(BIT 01)
J2	2A1A06P02D=06 1A4A06J06D=06			
	1A0B8=K0	2= 65		
J3	2A1A06P02D=05 1A4A06J06D=05			F0 REGISTER BIT 2
	1A0B8=K1	2= 65		
K0	2A1B6=F2	6= 43		S/M FIRST CYCLE=EN RF SENSE AMPL 00
K1	2A1B6=P2	6= 43		NOT(F BIT 01) TO WORD MVE XLTN
K2	2A1A4=Q0	6= 59	2A1A4=AM	NOT(F BIT 03) TO S REG FAN IN
K3	2A1A8=U1	6= 55		NOT(F0=00 TO Z LS2) TO GROUP 0
L0	2R0A8=E0	6=109		
L1	2R0A8=E1	6=109		F BIT 01 TO STATUS COMPARE
L2	2R0A7=02	6=117		F BIT 03 TO STATUS COMPARE
L3	2R0A7=03	6=117		
M0	2A1B6=V0	6= 43		NOT (BLOCK BIT 00 TO Z ON ACT$_1$)
M1	2A1B4=C1	6= 57		NOT INCR BY 4 TO Z BITS 0/1
M2	2A1A8=E3	6= 55		(ADDER TO Z) TO GROUP 0
M3	2A1B7=W1	6= 41	2A1B7=AZ	WORD ADDR BIT 01 TO PF XMTR
N0	2A1A06P02D=03 1A4A06J06D=03			F0 REGISTER BIT 1
	1A0B8=D1	2= 65		
N1	2A1A06P02D=04 1A4A06J06D=04			
	1A0B8=D0	2= 65		
N2	2A1A06P02D=07 1A4A06J06D=07			F0 REGISTER BIT 3
	1A0B6=B0	2= 67		
N3	2A1A06P02D=08 1A4A06J06D=08			
	1A0B6=B1	2= 67		
O0	2A1B6=U1	6= 43		FORCE BIT 01 TO Z ON ACTIVATE
O1	2A1B4=M1	6= 57		RF=Z BIT 01
O2	2A1A5=D1	6= 47		BIT 02 GENERATE TO GROUP 1
O3	2A1B4=I1	6= 57		RF=Z BIT 03
P0	2A1A3=X0	6= 65		
P1	2A1A3=X1	6= 65		NOT DIGIT DR 01 TO RF 00=37
P2	2A1A3=T0	6= 65		
P3	2A1A3=T1	6= 65		NOT DIGIT DR 03 TO RF 00=37
Q0	2A1B1=B1	6= 77		DIGIT DRIVE 00 TO RF 40=77
Q1	2A1B1=B0	6= 77		
Q2	2A1A1=W0	6= 77		
Q3	2A1A1=W1	6= 77		DIGIT DRIVE 02 TO RF 40=77
R0	2R1R4=H1	6= 29		
R1	2R1R4=H0	6= 29		RF SENSE AMP BIT 00 TO D4 REG
R2	2R1B2=H0	6= 33		RF SENSE AMP BIT 02 TO D4 REG
R3	2R1B2=H1	6= 33		
S0	2A1A1=X1	6= 77		DIGIT DRIVE 01 TO RF 40=77
S1	2A1A1=X0	6= 77		
S2	2A1A1=T1	6= 77		DIGIT DRIVE 03 TO RF 40=77
S3	2A1A1=T0	6= 77		
T0	2A1B4=I0	6= 57		RF=Z BIT 00
T1	2A1A8=W3	6= 55		NOT(EN REG FILE TO D4) TO GR 0
U0	2R1R3=H0	6= 31		RF SENSE AMP BIT 01 TO D4 REG
U1	2R1R3=H1	6= 31		
U2	2R1A4=H0	6= 35		RF SENSE AMP BIT 03 TO D4 REG
U3	2R1A4=H1	6= 35		
V0	2A1A5=D0	6= 47		BIT 03 GENERATE TO GROUP 1
V1	2A1A8=R0	6= 55		NOT (S/M XLTN TO ADDR SEL GR 0)
V2	2A1A5=M0	6= 47	2A1A5=RX	F0=D0(BIT 03) TO Z REG(BIT 05)
V3	2A1B7=R1	6= 41	2A1B7=AV	WORD ADDR BIT 00 TO PF XMTR
W0	2A1B4=L3	6= 57		CHARACTER ADDRESS DESIGNATOR 0
W1	2A1B6=O0	6= 43		INPUT TO Z REG TIMING =GROUP 0
W2	2A1A5=M1	6= 47	2A1A5=AZ	F0=D0(BIT 02)TO Z REG(BIT 04)
W3	2A1R4=H0	6= 57		RF=Z BIT 02
X0	2A1B3=B1	6= 65		NOT DIGIT DR 00 TO RF 00=37
X1	2A1B3=B0	6= 65		
X2	2A1A3=W0	6= 65		
X3	2A1A3=W1	6= 65		NOT DIGIT DR 02 TO RF 00=37



229

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A184-K0	6- 57		RF=Z BITS(04)(05)(06)(07)
B0	2A2A8-W2	5- 9		RC S BUS BIT 02 TO PAGE FILE
B1	2A2A8-W3	5- 9		
B2	2A2A8-W1	5- 9		
B3	2A2A8-W0	5- 9		RC S BUS BIT 04 TO PAGE FILE
C0	2A185-F0	6- 45		BIT 01 GENERATE TO GROUP 1
C1	2A185-H1	6- 45		BIT 00 GENERATE TO GROUP 1
D0	2A185-V0	6- 45		BIT 03 GENERATE TO GROUP 1
D1	2A185-D2	6- 45		BIT 02 GENERATE TO GROUP 1

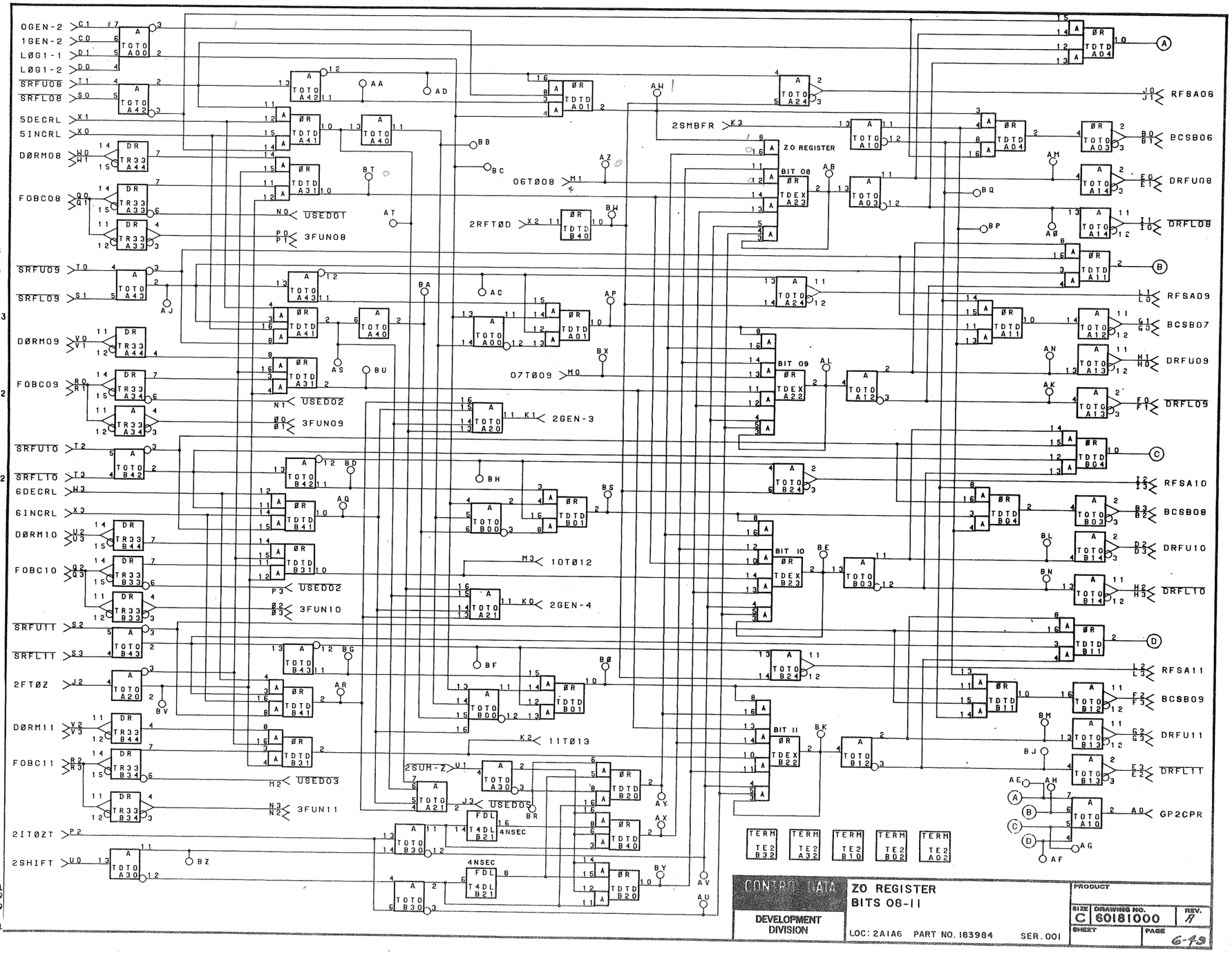
D2	2A1A1*S1	6* 75		DIGIT DRIVE 06 TO RF 40*77
D3	2A1A1*S0	6* 75		DIGIT DRIVE 04 TO RF 40*77
E0	2A1A1*U1	6* 77		
E1	2A1A1*U0	6* 77		
E2	2A1A3*R1	6* 63		NOT DIGIT DR 07 TO RF 00*37
E3	2A1A3*R0	6* 63		
F0	2A1A3*V0	6* 65		
F1	2A1A3*V1	6* 65		NOT DIGIT DR 05 TO RF 00*37
F2	2A2A9*W0	5* 11		BC S BUS BIT 05 TO PAGE FILE
F3	2A2A9*W1	5* 11		
G0	2A2A9*W3	5* 11		
G1	2A2A9*W2	5* 11		BC S BUS BIT 03 TO PAGE FILE
G2	2A1A1*R1	6* 75		DIGIT DRIVE 07 TO RF 40*77
G3	2A1A1*R0	6* 75		
H0	2A1A1*V0	6* 77		
H1	2A1A1*V1	6* 77		DIGIT DRIVE 05 TO RF 40*77
H2	2A1A3*S0	6* 63		
H3	2A1A3*S1	6* 63		NOT DIGIT DR 06 TO RF 00*37
I0	2A1A3*U1	6* 65		NOT DIGIT DR 04 TO RF 00*37
I1	2A1A3*U0	6* 65		
I2	2B1B4*S0	6* 29		RF SENSE AMP BIT 06 TO D4 REG
I3	2B1B4*S1	6* 29		
J0	2B1A3*W0	6* 37		RF SENSE AMP BIT 04 TO D4 REG
J1	2B1A3*W1	6* 37		
J2	2A1A8*U2	6* 55		F0 TO Z FAN*IN TO GROUP 1
J3	2A1B8*B1	6* 53		GROUP 1 GENERATE TO GROUP 4
K0	2A1A7*C0	6* 51		GROUP 1 GENERATE TO GROUP 3
K1	2A1A6*C0	6* 49		GROUP 1 GENERATE TO GROUP 2
K2	2A1A6*M0	6* 49	2A1A6*RX	F0*D0(BIT 07)TO Z REG(BIT 09)
K3	2A1A8*R1	6* 55		S/M XLTN TO ADDR SELECT GR 1
L0	2B1A2*W1	6* 39		
L1	2B1A2*W0	6* 39		RF SENSE AMP BIT 05 TO D4 REG
L2	2B1B3*S0	6* 31		RF SENSE AMP BIT 07 TO D4 REG
L3	2B1B3*S1	6* 31		
M0	2A1B5*V2	6* 45	2A1A5*RX	F0*D0(BIT 03) TO Z REG(BIT 05)
M1	2A1B5*W2	6* 45	2A1A5*AZ	F0*D0(BIT 02)TO Z REG(BIT 04)
M3	2A1A6*W1	6* 49	2A1A6*AZ	F0*D0(BIT 06)TO Z REG(BIT 08)
N0	2A1A4*X3	6* 59		NOT(F BIT 04) TO S REG FAN IN
N1	2A1A4*W3	6* 59		NOT (F BIT 05) TO S REG FAN*IN
N2	2B0A7*P3	6*117		
N3	2B0A7*P2	6*117		F BIT 07 TO STATUS COMPARE
O0	2B0A8*C1	6*109		F BIT 05 TO STATUS COMPARE
O1	2B0A8*C0	6*109		
O2	2B0A7*Q2	6*117		F BIT 06 TO STATUS COMPARE
O3	2B0A7*Q3	6*117		
P0	2B0A8*F0	6*109		F BIT 04 TO STATUS COMPARE
P1	2B0A8*F1	6*109		
P2	[illegible]1	6* 43		INPUT TO Z REG TIMING *GROUP 1
Q0	[illegible]*09			F0 REGISTER BIT 4
	2A4A06J060*09			
	1A0B6*D1	2* 67		
Q1	2A1A06P02D*10			
	1A4A06J06D*10			
	1A0B6*D0	2* 67		
Q2	2A1A06P02E*01			F0 REGISTER BIT 6
	1A4A06J06E*01			
	1A0B4*B0	2* 69		
Q3	2A1A06P02E*02			
	1A4A06J06E*02			
	1A0B4*B1	2* 69		
R0	2A1A06P05D*07			F0 REGISTER BIT 5
	1A4A06J14D*07			
	1B0A5*F3	2* 29		
R1	2A1A06P05D*08			
	1A4A06J14D*08			F0 REGISTER BIT 7
	1B0A5*F2	2* 29		
R2	2A1A06P02E*03			
	1A4A06J06E*03			
	1A0B4*D1	2* 69		
R3	2A1A06P02E*04			
	1A4A06J06E*04			
	1A0B4*D0	2* 69		
S0	2A1B3*X1	6* 65		SENSE RF 00*37 NOT(BIT 04)
S1	2A1B3*W0	6* 65		SENSE RF 00*37 NOT(BIT 05)
S2	2A1B1*M0	6* 75		SENSE RF 40*77 NOT(BIT 07)
S3	2A1B3*M0	6* 63		SENSE RF 00*37 NOT(BIT 07)
T0	2A1B1*W0	6* 77		SENSE RF 40*77 NOT(BIT 05)
T1	2A1B1*X1	6* 77		SENSE RF 40*77 NOT(BIT 04)
T2	2A1B1*N1	6* 75		SENSE RF 40*77 NOT(BIT 06)
T3	2A1B3*N1	6* 63		SENSE RF 00*37 NOT(BIT 06)
U0	2A1A8*U0	6* 55		(F0*D0 TO Z LS2) TO GROUP 1
U1	2A1A8*E2	6* 55		NOT(ADDER TO Z) TO GROUP 1
U2	2B1B4*U1	6* 29		DO BIT 06 TO Z REG FAN IN
U3	2B1B4*U0	6* 29		
V0	2B1A2*B1	6* 39		DO BIT 05 TO Z REG FAN IN
V1	2B1A2*B0	6* 39		
V2	2B1B3*U1	6* 31		DO BIT 07 TO Z REG FAN IN
V3	2B1B3*U0	6* 31		
W0	2B1A3*B1	6* 37		DO BIT 04 TO Z REG FAN IN
W1	2B1A3*B0	6* 37		
W3	2A1B4*P2	6* 57		DECREMENT RF L17 TO BITS 06/07
X0	2A1B4*T3	6* 57		INCREMENT RF L17 TO BITS 04/05
X1	2A1B4*T2	6* 57		DECREMENT RF L17 TO BITS 04/05
X2	2A1A8*V2	6* 55		(ENABLE RF TO D4) TO GROUP 1
X3	2A1B4*Q3	6* 57		INCREMENT RF L17 TO BITS 06/07



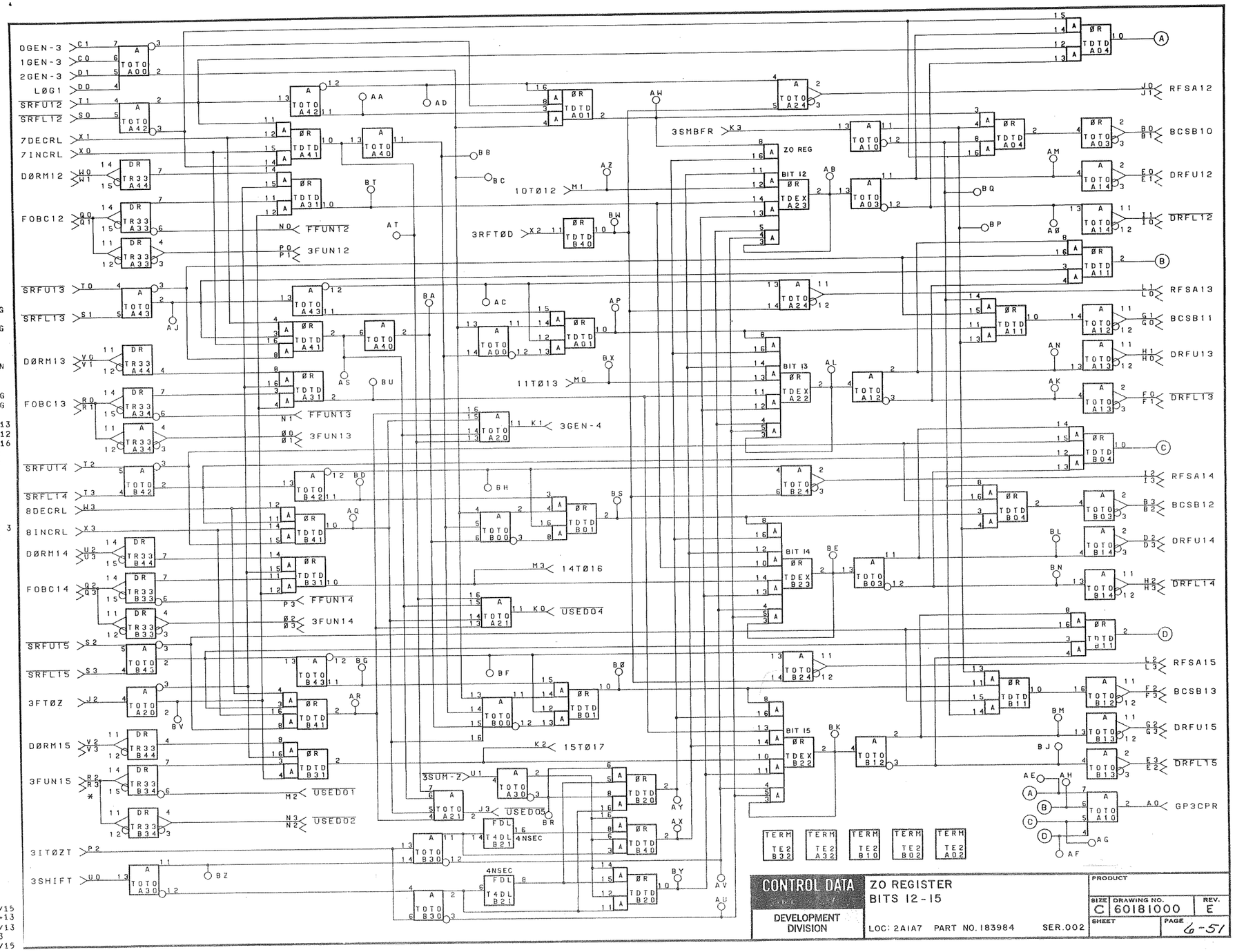
231

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A1B4-L0	6- 57		RF=Z BITS(08)(09)(10)(11)
B0	2A2B4-F0	5- 21		RC S BUS BIT 06 TO PAGE FILE
B1	2A2B4-F1	5- 21		

B2	2A2A8=V1	5= 9		
B3	2A2A8=V0	5= 9		RC S BUS BIT 08 TO PAGE FILE
C0	2A1A5=K1	6= 47		GROUP 1 GENERATE TO GROUP 2
C1	2A1B5=H3	6= 45		GROUP 0 GENERATE TO GROUP 2
D2	2A1A1=N1	6= 75		DIGIT DRIVE 10 TO RF 40=77
D3	2A1A1=N0	6= 75		
E0	2A1A1=Q1	6= 75		DIGIT DRIVE 08 TO RF 40=77
E1	2A1A1=Q0	6= 75		
E2	2A1A3=01	6= 63		NOT DIGIT DR 11 TO RF 00=37
E3	2A1A3=00	6= 63		
F0	2A1A3=P0	6= 63		
F1	2A1A3=P1	6= 63		NOT DIGIT DR 09 TO RF 00=37
F2	2A2B6=X0	5= 13		RC S BUS BIT 09 TO PAGE FILE
F3	2A2B6=X1	5= 13		
G0	2A2A9=V1	5= 11		
G1	2A2A9=V0	5= 11		RC S BUS BIT 07 TO PAGE FILE
G2	2A1A1=01	6= 75		DIGIT DRIVE 11 TO RF 40=77
G3	2A1A1=00	6= 75		
H0	2A1A1=P0	6= 75		
H1	2A1A1=P1	6= 75		DIGIT DRIVE 09 TO RF 40=77
H2	2A1A3=N0	6= 63		
H3	2A1A3=N1	6= 63		NOT DIGIT DR 10 TO RF 00=37
I0	2A1A3=Q1	6= 63		NOT DIGIT DR 08 TO RF 00=37
I1	2A1A3=Q0	6= 63		
I2	2B1A3=S0	6= 37		RF SENSE AMP BIT 10 TO D4 REG
I3	2B1A3=S1	6= 37		
J0	2B1B2=S0	6= 33		RF SENSE AMP BIT 08 TO D4 REG
J1	2B1B2=S1	6= 33		
J2	2A1A8=T2	6= 55		(F0 TO Z FAN IN) TO GROUP 2
K0	2A1B8=B0	6= 53		GROUP 2 GENERATE TO GROUP 4
K1	2A1A7=D1	6= 51		GROUP 2 GENERATE TO GROUP 3
K2	2A1A7=H0	6= 51	2A1A7=RX	(F0+D0) BIT 11 TO Z REG BIT 13
K3	2A1A8=P0	6= 55		S/M XLTN TO ADDR SELECT GR 2
L0	2B1A4=S1	6= 35		
L1	2B1A4=S0	6= 35		RF SENSE AMP BIT 09 TO D4 REG
L2	2B1A2=S0	6= 39		RF SENSE AMP BIT 11 TO D4 REG
L3	2B1A2=S1	6= 39		
M0	2A1A5=K2	6= 47	2A1A6=RX	F0+D0(BIT 07)TO Z REG(BIT 09)
M1	2A1A5=H3	6= 47	2A1A6=AZ	F0+D0(BIT 06)TO Z REG(BIT 08)
M3	2A1A7=H1	6= 51	2A1A7=AZ	(F0+D0) BIT 10 TO Z REG BIT 12
N2	2B0B8=F2	6=111		
N3	2B0B8=F3	6=111		F BIT 11 TO STATUS COMPARE
O0	2B0B8=E3	6=111		F BIT 09 TO STATUS COMPARE
O1	2B0B8=E2	6=111		
O2	2B0B8=D3	6=111		F BIT 10 TO STATUS COMPARE
O3	2B0B8=D2	6=111		
P0	2B0B8=G2	6=111		F BIT 08 TO STATUS COMPARE
P1	2B0B8=G3	6=111		
P2	2A1B6=N3	6= 43		INPUT TO Z REG TIMING =GROUP 2
Q0	2A1A06P02E=05			F0 REGISTER BIT 8
	1A4A06J06E=05			
	1A0B4=K1	2= 69		
Q1	2A1A06P02E=06			
	1A4A06J06E=06			
	1A0B4=K0	2= 69		
Q2	2A1A06P02E=09			F0 REGISTER BIT 10
	1A4A06J06E=09			
	1A0B2=D1	2= 71		
Q3	2A1A06P02E=10			
	1A4A06J06E=10			
	1A0B2=D0	2= 71		
R0	2A1A06P02E=07			F0 REGISTER BIT 9
	1A4A06J06E=07			
	1A0B2=B0	2= 71		
R1	2A1A06P02E=08			
	1A4A06J06E=08			
	1A0B2=B1	2= 71		
R2	2A1A06P02F=01			F0 REGISTER BIT 11
	1A4A06J06F=01			
	1A0B2=K1	2= 71		
R3	2A1A06P02F=02			
	1A4A06J06F=02			
	1A0B2=K0	2= 71		
S0	2A1B3=M1	6= 63		SENSE RF 00=37 NOT(BIT 08)
S1	2A1B3=R0	6= 63		SENSE RF 00=37 NOT(BIT 09)
S2	2A1B1=Q0	6= 75		SENSE RF 40=77 NOT(BIT 11)
S3	2A1B3=Q0	6= 63		SENSE RF 00=37 NOT(BIT 11)
T0	2A1B1=R0	6= 75		SENSE RF 40=77 NOT(BIT 09)
T1	2A1B1=M1	6= 75		SENSE RF 40=77 NOT(BIT 08)
T2	2A1B1=R1	6= 75		SENSE RF 40=77 NOT(BIT 10)
T3	2A1B3=R1	6= 63		SENSE RF 00=37 NOT(BIT 10)
U0	2A1A8=V0	6= 55		(F0+D0 TO Z LS2) TO GROUP 2
U1	2A1A8=F3	6= 55		NOT(ADDER TO Z) TO GROUP 2
U2	2B1A3=U1	6= 37		D0 BIT 10 TO Z REG FAN IN
U3	2B1A3=U0	6= 37		
V0	2B1A4=U1	6= 35		D0 BIT 09 TO Z REG FAN IN
V1	2B1A4=U0	6= 35		
V2	2B1A2=U1	6= 39		D0 BIT 11 TO Z REG FAN IN
V3	2B1A2=U0	6= 39		
W0	2B1B2=U1	6= 33		D0 BIT 08 TO Z REG FAN IN
W1	2B1B2=U0	6= 33		
W3	2A1B4=W3	6= 57		DECREMENT RF L17 TO BITS 10/11
X0	2A1B4=X2	6= 57		INCREMENT RF L17 TO BITS 08/09
X1	2A1B4=X3	6= 57		DECREMENT RF L17 TO BITS 08/09
X2	2A1A8=S3	6= 55		ENABLE RF TO D4 TO GROUP 1
X3	2A1B4=W2	6= 57		INCREMENT RF L17 TO BITS 10/11



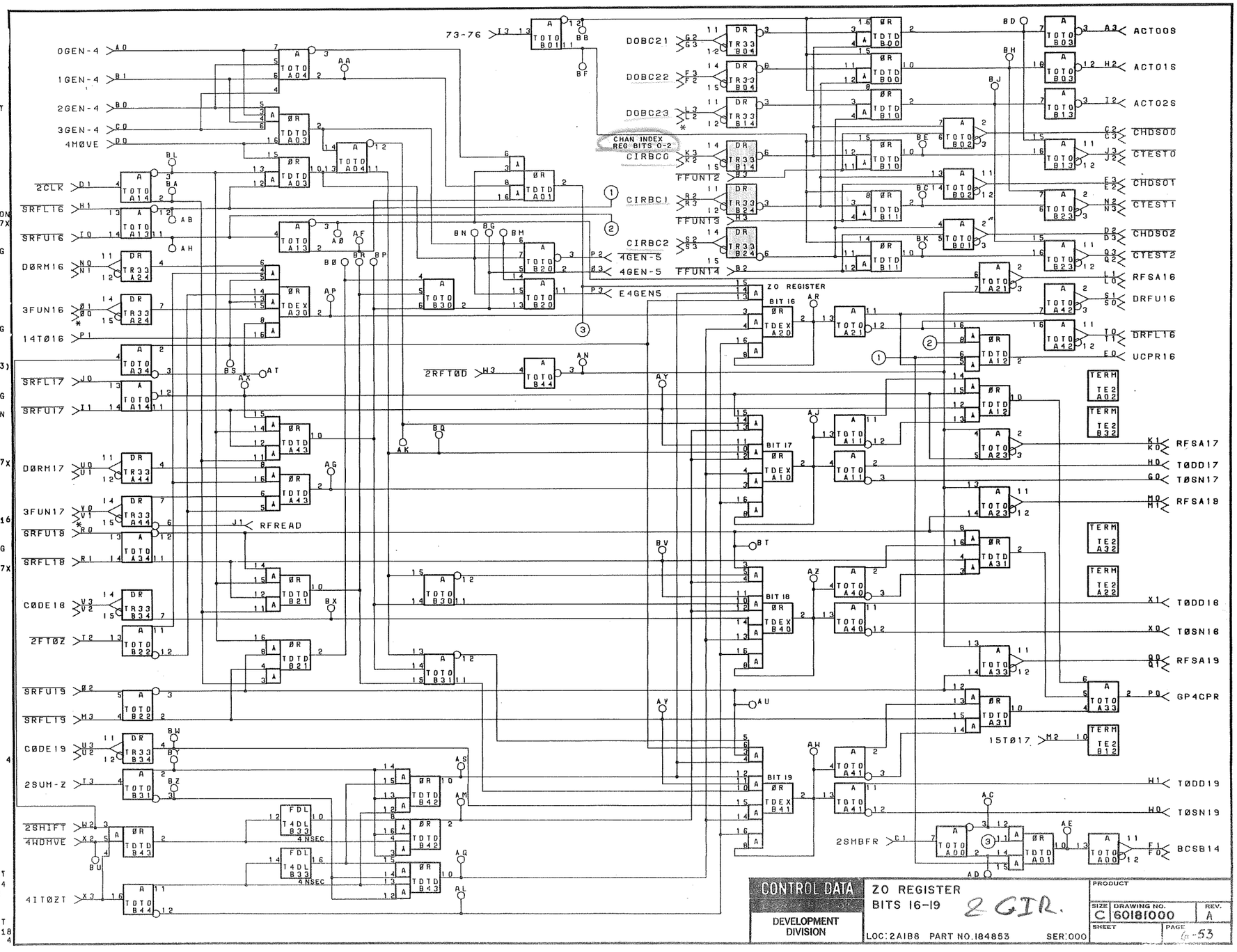
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A1R4-L1	6- 57		RF=Z BITS (12)(13)(14)(15)
B0	2A2R8-U0	5- 13		AC S BUS BIT 10 TO PAGE FILE
B1	2A2R8-U1	5- 13		
B2	2A2R7-D2	5- 15		
B3	2A2R7-D3	5- 15		AC S BUS BIT 12 TO PAGE FILE
C0	2A1A5-K0	6- 47		GROUP 1 GENERATE TO GROUP 3
C1	2A1B5-I3	6- 45		GROUP 0 GENERATE TO GROUP 3
D1	2A1A6-K1	6- 49		GROUP 2 GENERATE TO GROUP 3
D2	2A1A0-W1	6- 83		DIGIT DRIVE 14 TO RF 40-77
D3	2A1A0-W0	6- 83		
E0	2A1B0-B1	6- 83		DIGIT DRIVE 12 TO RE 40-77
E1	2A1B0-B0	6- 83		
E2	2A1A2-T1	6- 71		NOT DIGIT DR 15 TO RF 00-37
E3	2A1A2-T0	6- 71		
F0	2A1A2-X0	6- 71		
F1	2A1A2-X1	6- 71		NOT DIGIT DR 13 TO DR 00-37
F2	2A2R6-D1	5- 17		AC S BUS BIT 13 TO PAGE FILE
F3	2A2R6-D0	5- 17		
G0	2A2R7-D0	5- 15		
G1	2A2R7-D1	5- 15		AC S BUS BIT 11 TO PAGE FILE
G2	2A1A0-T1	6- 83		DIGIT DRIVE 15 TO RF 40-77
G3	2A1A0-T0	6- 83		
H0	2A1A0-X0	6- 83		
H1	2A1A0-X1	6- 83		DIGIT DRIVE 13 TO RF 40-77
H2	2A1A2-W0	6- 71		
H3	2A1A2-W1	6- 71		NOT DIGIT DR 14 TO DR 00-37
I0	2A1B2-B1	6- 71		NOT DIGIT DR 12 TO RF 00-37
I1	2A1B2-B0	6- 71		
I2	2A1R2-T1	6- 33		RF SENSE AMP BIT 14 TO D4 REG
I3	2A1R2-T0	6- 33		
J0	2A1R4-T1	6- 29		RF SENSE AMP BIT 12 TO D4 REG
J1	2A1R4-T0	6- 29		
J2	2A1A8-R2	6- 55		(F0 TO Z FAN IN) TO GROUP 3
K1	2A1B8-C0	6- 53		GROUP 3 GENERATE TO GROUP 4
K2	2A1B8-M2	6- 53		(F0+D0) BIT 15 TO TERMINATION
K3	2A1A8-L1	6- 55		S/M XLTN TO ADDR SELECT GR 3
L0	2A1B3-T0	6- 31		
L1	2A1R3-T1	6- 31		RF SENSE AMP BIT 13 TO D4 REG
L2	2A1A4-T1	6- 35		RF SENSE AMP BIT 15 TO D4 REG
L3	2A1A4-T0	6- 35		
M0	2A1A6-K2	6- 49	2A1A7-RX	(F0+D0) BIT 11 TO Z REG BIT 13
M1	2A1A6-H3	6- 49	2A1A7-AZ	(F0+D0) BIT 10 TO Z REG BIT 12
M3	2A1B8-P1	6- 53		(F0+D0) BIT 14 TO Z REG BIT 16
N0	2A1B8-B3	6- 53		NOT(F BIT 12) TO OR WITH CIR
N1	2A1B8-H3	6- 53		NOT(F BIT 13) TO OR WITH CIR
O0	2R0A9-M2	6-101		F BIT 13 TO STATUS COMPARE
O1	2R0A9-M3	6-101		
O2	2R0A9-P2	6-101		F BIT 14 TO STATUS COMPARE
O3	2R0A9-P3	6-101		
P0	2R0A9-L2	6-101		F BIT 12 TO STATUS COMPARE
P1	2R0A9-L3	6-101		
P2	2A1R6-P1	6- 43		INPUT TO Z REG TIMING *GROUP 3
P3	2A1B8-B2	6- 53		NOT(F BIT 14) TO OR WITH CIR
Q0	2A1A06P02F-03			FO REGISTER BIT 12
	1A4A06J06F-03			
	1A0R0-B0	2- 73		
Q1	2A1A06P02F-04			
	1A4A06J06F-04			
	1A0R0-B1	2- 73		FO REGISTER BIT 14
Q2	2A1A06P02F-07			
	1A4A06J06F-07			
	1A0R0-K1	2- 73		
Q3	2A1A06P02F-08			
	1A4A06J06F-08			
	1A0R0-K0	2- 73		FO REGISTER BIT 13
R0	2A1A06P02F-05			
	1A4A06J06F-05			
	1A0R0-D1	2- 73		
R1	2A1A06P02F-06			
	1A4A06J06F-06			
	1A0R0-D0	2- 73		NOT FO BIT 15 TO Z REG FI
R2	2R0A9-C1	6-101		
R3	2R0A9-C0	6-101		SENSE RF 00-37 NOT(BIT 12)
S0	2A1R2-T1	6- 71		SENSE RF 00-37 NOT(BIT 13)
S1	2A1R2-S0	6- 71		SENSE RF 40-77 NOT(BIT 15)
S2	2A1R0-X0	6- 83		SENSE RF 00-37 NOT(BIT 15)
S3	2A1R2-X0	6- 71		SENSE RF 40-77 NOT(BIT 13)
T0	2A1R0-S0	6- 83		SENSE RF 40-77 NOT(BIT 12)
T1	2A1R0-T1	6- 83		SENSE RF 40-77 NOT(BIT 14)
T2	2A1R0-S1	6- 83		SENSE RF 00-37 NOT(BIT 14)
T3	2A1R2-S1	6- 71		(FO+D0 TO Z LS2) TO GROUP 3
U0	2A1A8-T0	6- 55		NOT(ADDER TO Z) TO GROUP 3
U1	2A1A8-D3	6- 55		NO BIT 14 TO Z REG FAN IN
U2	2R1R2-C1	6- 33		
U3	2R1R2-C0	6- 33		NO BIT 13 TO Z REG FAN IN
V0	2R1R3-C1	6- 31		
V1	2R1R3-C0	6- 31		NO BIT 15 TO Z REG FAN IN
V2	2R1A4-C1	6- 35		
V3	2R1A4-C0	6- 35		NO BIT 12 TO Z REG FAN IN
W0	2R1R4-C1	6- 29		
W1	2R1R4-C0	6- 29		
W3	2A1R4-V2	6- 57		DECREMENT RF L17 TO BITS 14/15
X0	2A1R4-U3	6- 57		INCREMENT RF L17 TO BITS 12-13
X1	2A1R4-U2	6- 57		DECREMENT RF L17 TO BITS 12/13
X2	2A1A8-W2	6- 55		(ENABLE RF TO D4) TO GROUP 3
X3	2A1R4-V3	6- 57		INCREMENT RF L17 TO BITS 14/15



CONTROL DATA	ZO REGISTER BITS 12-15	PRODUCT
DEVELOPMENT DIVISION	LOC: 2A1A7 PART NO. 183984 SER.002	SIZE C · DRAWING NO. 60181000 · REV. E · SHEET · PAGE 6-51

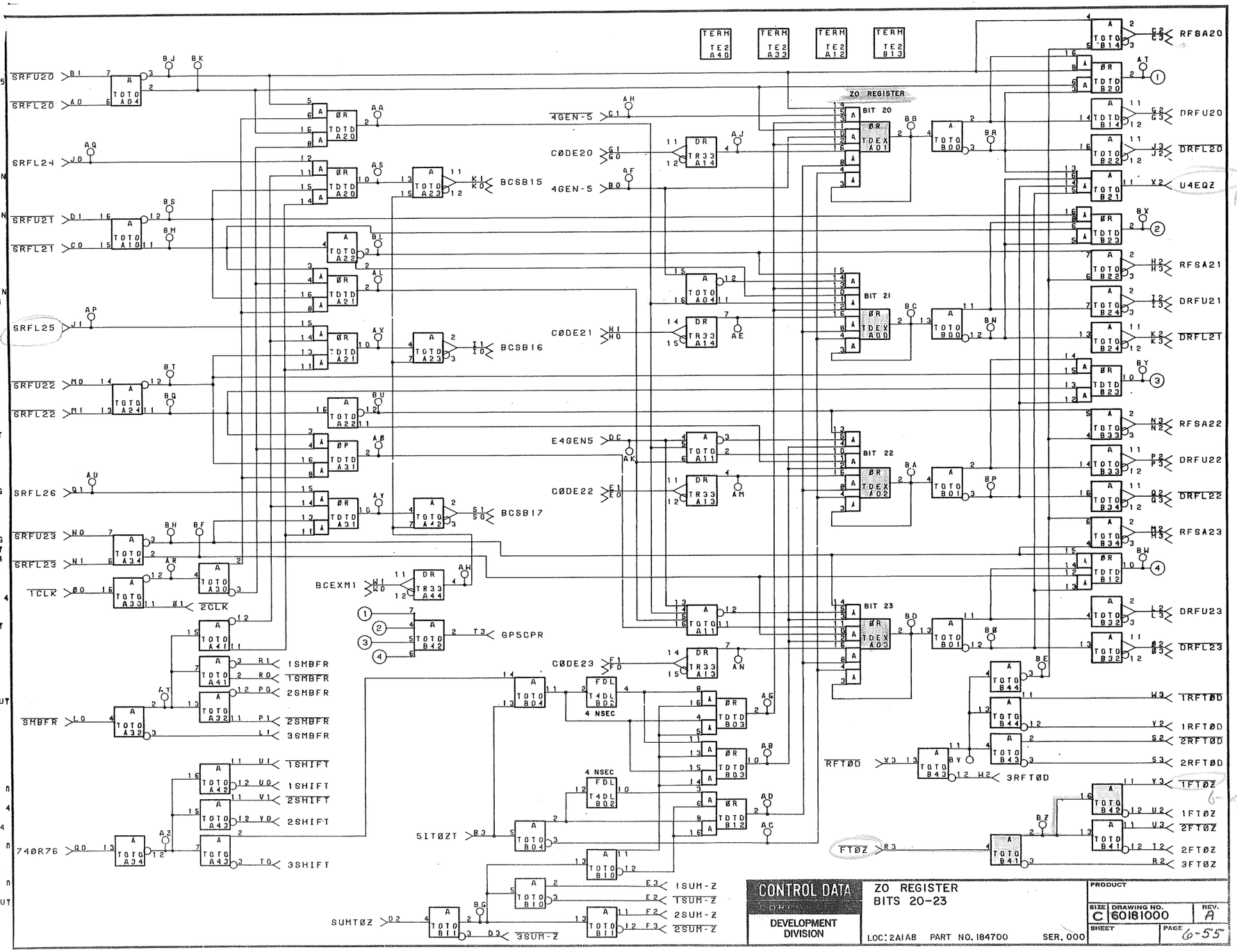
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A1B5-I2	6- 45		GROUP 0 GENERATE TO GROUP 4
A3	2A1A4-B2	6- 59		ACT. I/O ADDR BIT 00 TO S FAN-IN
B0	2A1A6-K0	6- 49		GROUP 2 GENERATE TO GROUP 4
B1	2A1A5-J3	6- 47		GROUP 1 GENERATE TO GROUP 4
B2	2A1A7-P3	6- 51		NOT(F BIT 14) TO OR WITH CIR
B3	2A1A7-N0	6- 51		NOT(F BIT 12) TO OR WITH CIR
C0	2A1A7-K1	6- 51		GROUP 3 GENERATE TO GROUP 4
C1	2A1A8-P1	6- 55		NOT(SM XLTN) TO ADDR SEL GRP 4
C2	2B0A6-X3	6-121		
C3	2B0A6-X2	6-121		NOT CHAN SEL BIT 00 ON 7X
D0	2A1B6-B3	6- 43		MOVE DECR RF U7 XLTN TO GR 4
D1	2A1A8-01	6- 55		NOT(CLOCK) TO Z ADDER GROUP 4
D2	2B0A5-X3	6-123		
D3	2B0A5-X2	6-123		NOT CHAN SEL BIT 02 ON 7X
E0	2A1B4-M0	6- 57		RF=Z BIT 16 ONLY
E2	2B0A6-X1	6-121		NOT CHAN SEL BIT 01 ON 7X
E3	2B0A6-X0	6-121		
F0	2A2B6-D2	5- 17		
F1	2A2B6-D3	5- 17		BC S BUS BIT 14 TO PAGE FILE
F2	2A1A06P05C-08			
	1A4A06J14C-08			
	1B0B1-C2	2- 9		
F3	2A1A06P05C-07			D0 TO BLOCK CONT, BIT 22
	1A4A06J14C-07			
	1B0B1-C3	2- 9		

G0	2A1R6=Q2	6= 43		NOT (Z REG BIT 17) TO SENSE EQUAL Z
G2	2A1A06P05C=05			DO TO BLOCK CONT, BIT 21
	1A4A06J14C=05			
	1R0B1=R3	2= 9		
G3	2A1A06P05C=06			
	1A4A06J14C=06			
	1R0B1=R2	2= 9		
H0	2A1B7=A3	6= 41	2A1B7=BA	Z REG BIT 17 TO DIGIT FAN OUT
H1	2A1B2=X1	6=		SENSE RF 00=37 NOT(BIT 16)
H2	2A1A4=K3	6= 59		ACT, I/O ADDR BIT 01 TO S FAN=IN
H3	2A1A7=N1	6= 51		NOT(F BIT 13) TO OR WITH CIR
I0	2A1B0=X1	6= 83		SENSE RF 40=77 NOT(BIT 16)
I1	2A1R0=W0	6= 83		SENSE RF 40=77 NOT(BIT 17)
I2	2A1A4=L3	6= 59		ACT, I/O ADDR BIT 02 TO S FAN=IN
I3	2A1R6=V1	6= 43		F=73 THRU 76 TO CHL SEL XLTN
J0	2A1B2=W0	6= 71		SENSE RF 00=37 NOT(BIT 17)
J1	2A1R6=U3	6= 43		RF READ XLTN ON PROG OPERATION
J2	2B1A8=T1	6= 17		NOT CHL SEL BIT 0 TEST BUSY 7X
J3	2B1A8=T0	6= 17		
K0	2B1A0=F1	6= 5		
K1	2B1A0=F0	6= 5		RF SENSE AMP BIT 17 TO D4 REG
K2	2A1A06P03E=08			
	1A4A06J20E=08			
	1C0A3=U3	2= 39		
K3	2A1A06P03E=07			CIR,BIT 0
	1A4A06J20E=07			
	1C0A3=U2	2= 39		
L0	2R1A3=T0	6= 37		
L1	2B1A3=T1	6= 37		RF SENSE AMP BIT 16 TO D4 REG
L2	2A1A06P05C=10			
	1A4A06J14C=10			
	1R0B1=E3	2= 9		
L3	2A1A06P05C=09			NOT (DO TO BLOCK CONT, BIT 23)
	1A4A06J14C=09			
	1B0B1=E2	2= 9		
M0	2R1A1=H1	6= 25		RF SENSE AMP BIT 18 TO D4 REG
M1	2R1A1=H0	6= 25		
M2	2A1A7=K2	6= 51		(F0*D0) BIT 15 TO TERMINATION
M3	2A1B2=M0	6= 69		SENSE RF 00=37 NOT(BIT 19)
N0	2B1A3=C1	6= 37		D0 BIT 16 TO Z REG FAN IN
N1	2B1A3=C0	6= 37		
N2	2B1A8=T2	6= 17		
N3	2B1A8=T3	6= 17		NOT CHL SEL BIT 1 TEST BUSY 7X
O0	2B0A9=E1	6=101		
O1	2R0A9=E0	6=101		NOT F0 BIT 16 TO Z REG F1
O2	2A1B0=M0	6= 81		SENSE RF 40=77 NOT(BIT 19)
O3	2A1A8=B0	6= 55		GROUP 4 GENERATE TO GROUP 5
P0	2A1B4=L2	6= 57		RF=Z BITS (17)(18)(19)
P1	2A1A7=M3	6= 51		(F0*D0) BIT 14 TO Z REG BIT 16
P2	2A1A8=C1	6= 55	2A1A8=AH	NOT(GR 4 GENERATE TO GR 5)
P3	2A1A8=D0	6= 55	2A1A8=AK	GROUP 4 GENERATE TO GROUP 5
Q0	2B1A1=F0	6= 25		RF SENSE AMP BIT 19 TO D4 REG
Q1	2B1A1=F1	6= 25		
Q2	2B1A8=D3	6= 17		NOT CHL SEL BIT 2 TEST BUSY 7X
Q3	2B1A8=D2	6= 17		
R0	2A1B0=N1	6= 81		SENSE RF 40=77 NOT(BIT 18)
R1	2A1B2=N1	6= 69		SENSE RF 00=37 NOT(BIT 18)
R2	2A1A06P03E=09			CIR,BIT 1
	1A4A06J20E=09			
	1C0A3=R3	2= 39		
R3	2A1A06P03E=10			
	1A4A06J20F=10			
	1C0A3=R2	2= 39		
S0	2A1A0=U0	6= 83		
S1	2A1A0=U1	6= 83		DIGIT DRIVE 16 TO RF 40=77
S2	2A1A06P03F=01			CIR,BIT 2
	1A4A06J20F=01			
	1C0A3=L3	2= 39		
S3	2A1A06P03F=02			
	1A4A06J20F=02			
	1C0A3=L2	2= 39		
T0	2A1A2=U0	6= 71		
T1	2A1A2=U1	6= 71		NOT DIGIT DR 16 TO RF 00=37
T2	2A1A8=U3	6= 55		NOT(F0 TO Z FAN IN) TO GROUP 4
T3	2A1A8=F2	6= 55		(ADDER TO Z) TO GROUP 4
U0	2B1A2=C1	6= 39		D0 BIT 17 TO Z REG FAN IN
U1	2B1A2=C0	6= 39		
U2	2R1A9=F3	6= 23		
U3	2R1A9=F2	6= 23		CODE 19 TO Z REG=D0*F0
V0	2B1A9=V1	6= 23		NOT F BIT 17
V1	2R1A9=V0	6= 23		
V2	2R1A7=G3	6= 1		
V3	2R1A7=G2	6= 1		INPUT TO Z REG BIT 18
W0	2A1B6=R2	6= 43		NOT (Z REG BIT 19) TO SENSE EQUAL Z
W1	2A1B7=I1	6= 41	2A1B7=AE	Z REG BIT 19 TO DIGIT FAN OUT
W2	2A1A8=V1	6= 55		NOT(F0*D0 TO Z LS2)TO GROUP 4
W3	2A1A8=S2	6= 55		NOT(FNABLE RF TO D4) TO GR 4
X0	2A1B6=R3	6= 43		NOT (Z REG BIT 18) TO SENSE EQUAL Z
X1	2A1B7=E3	6= 41	2A1B7=RE	Z REG BIT 18 TO DIGIT FAN OUT
X2	2A1R6=H3	6= 43	2A1B8=RU	NOT(WORD MOVE) + BLK SUM 17/18
X3	2A1R6=P0	6= 43		INPUT TO Z REG TIMING =GROUP 4



CONTROL DATA	Z0 REGISTER BITS 16-19 2 CIR.	PRODUCT
DEVELOPMENT DIVISION	LOC:2A1B8 PART NO.184853 SER:000	SIZE C DRAWING NO. 60181000 REV. A
		SHEET PAGE 4-53

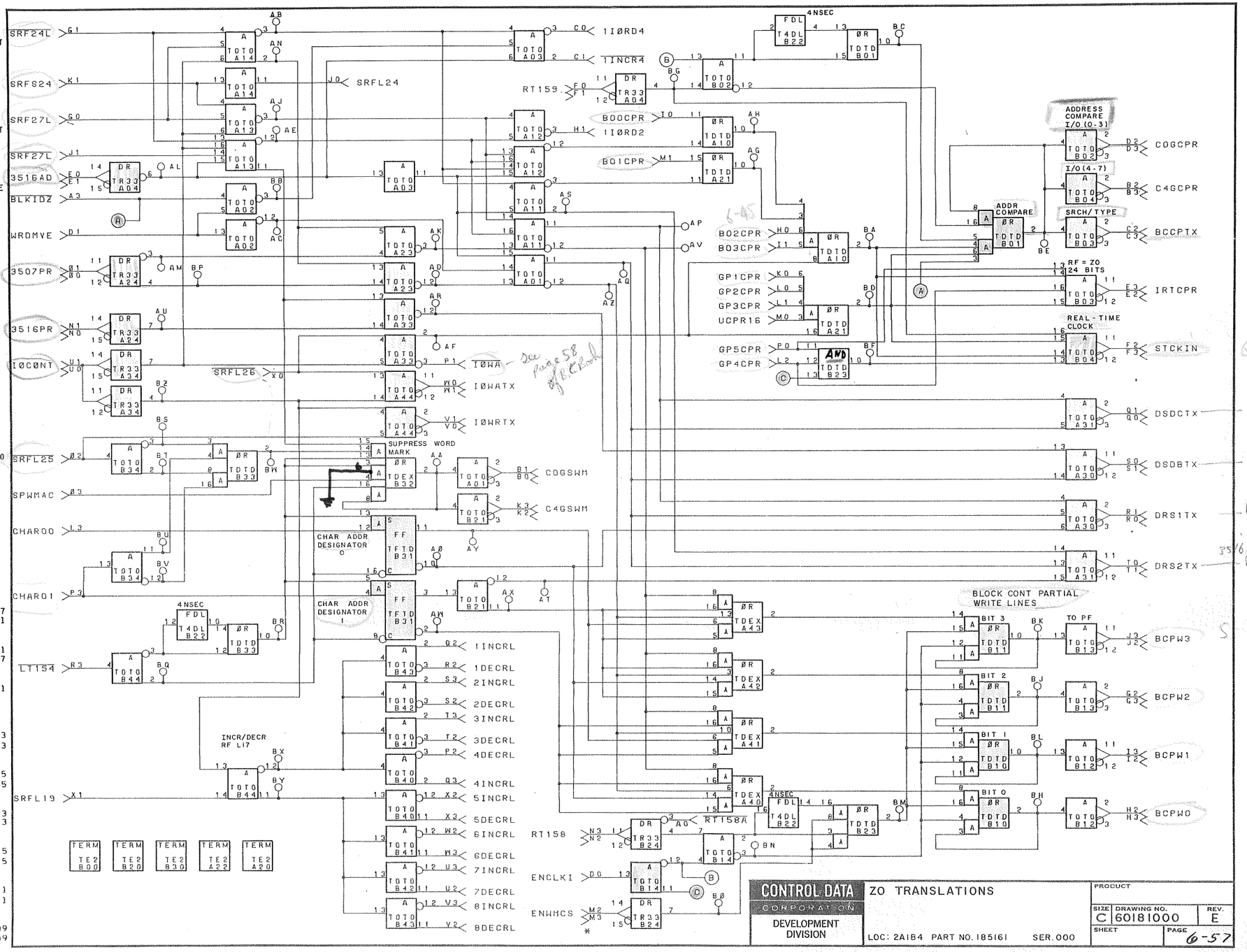
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A1R2*M1	6* 69		SENSE RF 00*37 NOT(BIT 20)
B0	2A1B8*O3	6* 53		GROUP 4 GENERATE TO GROUP 5
B1	2A1B0*M1	6* 81		SENSE RF 40*77 NOT(BIT 20)
B3	2A1B6*Q0	6* 43		INPUT TO Z REG TIMING *GROUP 5
C0	2A1R2*R0	6* 69		SENSE RF 00*37 NOT(BIT 21)
C1	2A1B8*P2	6* 53	2A1A8*AH	NOT(GR 4 GENERATE TO GR 5)
C2	2B1A1*D0	6* 25		RF SENSE AMP BIT 20 TO D4 REG
C3	2R1A1*D1	6* 25		
D0	2A1B8*P3	6* 53	2A1A8*AK	GROUP 4 GENERATE TO GROUP 5
D1	2A1B0*R0	6* 81		SENSE RF 40*77 NOT(BIT 21)
D2	2A1B6*F1	6* 43		SUM TO Z XLTN TO FAN OUT
D3	2A1A7*U1	6* 51		NOT(ADDER TO Z) TO GROUP 3
E0	2B1A9*N2	6* 23		
E1	2B1A9*N3	6* 23		CODE 22 TO Z REG*D0+F0+A0*XLTN
E2	2A1A5*U1	6* 47		NOT(ADDER TO Z) TO GROUP 1
E3	2A1B5*M2	6* 45		(ADDER TO Z) TO GROUP 0
F0	2B1A9*U3	6* 23		
F1	2B1A9*U2	6* 23		CODE 23 TO Z REG*D0+F0+A0*XLTN
F2	2A1B8*T3	6* 53		(ADDER TO Z) TO GROUP 4
F3	2A1A6*U1	6* 49		NOT(ADDER TO Z) TO GROUP 2
G0	2B1A9*K3	6* 23		
G1	2B1A9*K2	6* 23		CODE 20 TO Z REG*D0+F0
G2	2A1A0*Q1	6* 81		DIGIT DRIVE 20 TO RF 40*77
G3	2A1A0*Q0	6* 81		
H0	2B1A9*L3	6* 23		
H1	2B1A9*L2	6* 23		CODE 21 TO Z REG*D0+F0+A0*XLTN
H2	2B1A1*I1	6* 25		RF SENSE AMP BIT 21 TO D4 REG
H3	2B1A1*I0	6* 25		
I0	2A2B5*D2	5* 19		
I1	2A2B5*D3	5* 19		BC S BUS BIT 16 TO PAGE FILE
I2	2A1A0*P1	6* 81		DIGIT DRIVE 21 TO RF 40*77
I3	2A1A0*P0	6* 81		
J0	2A1B4*J0	6* 57	2A1A8*AQ	RF SENSE AMPL BIT 24 TO GR 5
J1	2A1B3*L0	6* 61	2A1A8*AP	SENSE REG FILE 00*37 BIT 25
J2	2A1A2*Q1	6* 69		NOT DIGIT DR 20 TO RF 00*37
J3	2A1A2*Q0	6* 69		
K0	2A2B5*D0	5* 19		
K1	2A2B5*D1	5* 19		BC S BUS BIT 15 TO PAGE FILE
K2	2A1A2*P0	6* 69		
K3	2A1A2*P1	6* 69		NOT DIGIT DR 21 TO RF 00*37
L0	2A1B6*G0	6* 43		NOT (S/M BFR XLTN) TO FAN OUT
L1	2A1A7*K3	6* 51		S/M XLTN TO ADDR SELECT GR 3
L2	2A1A0*O1	6* 81		DIGIT DRIVE 23 TO RF 40*77
L3	2A1A0*O0	6* 81		
M0	2A1B0*R1	6* 81		SENSE RF 40*77 NOT(BIT 22)
M1	2A1B2*R1	6* 69		SENSE RF 00*37 NOT(BIT 22)
M2	2B1A1*E0	6* 25		RF SENSE AMP BIT 23 TO D4 REG
M3	2B1A1*E1	6* 25		
N0	2A1B0*Q0	6* 81		SENSE RF 40*77 NOT(BIT 23)
N1	2A1B2*Q0	6* 69		SENSE RF 00*37 NOT(BIT 23)
N2	2B1A1*G1	6* 25		
N3	2B1A1*G0	6* 25		RF SENSE AMP BIT 22 TO D4 REG
O0	2A1B7*D0	6* 41		NOT(CLOCK CONTROL) TO FAN OUT
O1	2A1B8*D1	6* 53		NOT(CLOCK) TO Z ADDER GROUP 4
O2	2A1A2*O0	6* 69		
O3	2A1A2*O1	6* 69		NOT DIGIT DR 23 TO RF 00*37
P0	2A1A6*K3	6* 49		S/M XLTN TO ADDR SELECT GR 2
P1	2A1B8*C1	6* 53		NOT(SM XLTN) TO ADDR SEL GRP 4
P2	2A1A0*N1	6* 81		DIGIT DRIVE 22 TO RF 40*77
P3	2A1A0*N0	6* 81		
Q0	2A1B6*U0	6* 43		F=74 + 76 TO LS2 XLTN FAN*OUT
Q1	2A1B2*L1	6* 67	2A1A8*AU	SENSE REG FILE 00*37 BIT 26
Q2	2A1A2*N0	6* 69		
Q3	2A1A2*N1	6* 69		NOT DIGIT DR 22 TO RF 00*07
R0	2A1B5*V1	6* 45		NOT (S/M XLTN TO ADDR SEL GR 0)
R1	2A1A5*K3	6* 47		S/M XLTN TO ADDR SELECT GR 1
R2	2A1A7*J2	6* 51		(F0 TO Z FAN IN) TO GROUP 3
R3	2A1B7*B0	6* 41		NOT(F REG TO Z REG) TO FAN OUT
S0	2A2R4*F3	5* 21		
S1	2A2B4*F2	5* 21		BC S BUS BIT 17 TO PAGE FILE
S2	2A1B8*W3	6* 53		NOT(ENABLE RF TO D4) TO GR 4
S3	2A1A6*X2	6* 49		ENABLE RF TO D4 TO GROUP 1
T0	2A1A7*U0	6* 51		(F0*D0 TO Z LS2) TO GROUP 3
T2	2A1A6*J2	6* 49		(F0 TO Z FAN IN) TO GROUP 2
T3	2A1B4*P0	6* 57		RF=Z BITS (20)(21)(22)(23)
U0	2A1A5*U0	6* 47		(F0+D0 TO Z LS2) TO GROUP 1
U1	2A1B5*K3	6* 45		NOT(F0*D0 TO Z LS2) TO GROUP 0
U2	2A1A5*J2	6* 47		F0 TO Z FAN=IN TO GROUP 1
U3	2A1B8*T2	6* 53		NOT(F0 TO Z FAN IN) TO GROUP 4
V0	2A1A6*U0	6* 49		(F0*D0 TO Z LS2) TO GROUP 2
V1	2A1B8*W2	6* 53		NOT(F0*D0 TO Z LS2) TO GROUP 4
V2	2A1A5*X2	6* 47		(ENABLE RF TO D4) TO GROUP 1
V3	2A1B5*H2	6* 45		NOT(F0 TO Z FAN IN) TO GROUP 0
W0	2R1B0*B0	6* 7		
W1	2R1B0*B1	6* 7		HC EXECUTIVE MODE
W2	2A1A7*X2	6* 51		(ENABLE RF TO D4) TO GROUP 3
W3	2A1B5*T1	6* 45		NOT(EN REG FILE TO D4) TO GR 0
X2	2A1B6*T3	6* 43		Z UPPER 4 EQUAL ZERO
X3	2A1B6*H0	6* 43		NOT(ENABLE RF TO D4) TO FANOUT
	PAGE	6* 55		



239

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A1B7-Q1	6- 41	2A1B7-AR	NOT(T158) TO CLEAR T157
A3	2A1B6-B2	6- 43		NOT (S/H FIRST CYCLE) - BLOCK INT CODE 4
B0	2A0A2-W3	6-139		

B1	2A1A2-W2	6-139		SUPPR WORD MARK TO CHAN 0-3 FANOUT
B2	2C?A5-V?	6-195		ADDR COMPARE TO CHL 4-7 FANOUT
B3	2C?A5-V1	6-195		
C0	2A1B5-A?	6- 45		INCR & DECR BY 4 TO GRP 0
C1	2A1B5-M1	6- 45		NOT INCR BY 4 TO Z BITS 0/1
C2	2B1B8-U?	6- 11		ADDR COMPARE TO SEARCH/TYPE
C3	2B1B8-U1	6- 11		
D0	2A1B6-01	6- 43		EN CLOCK INTERRUPT
D1	2A1B6-C?	6- 43		WORD MOVE TO INCR/PART. WRITE XLTN
D2	2A?B5-V?	6-159		ADDR COMPARE TO CHL 0-3 FANOUT
D3	2A?B5-V1	6-159		
E0	2B1A1-S?	6- 25		12-BIT MODE CHAN A/D XLTN
E1	2B1A1-S1	6- 25		
E2	2B1A8-F3	6- 17		RF = Z - 24 BITS TO D4 XLTN
E3	2B1A8-F?	6- 17		T15$_0$ TO Z PANEL - TEST COMPARE
F0	2B1A7-D?	6- 1		
F1	2B1A7-D3	6- 1		SET CLOCK INTERRUPT F/F
F2	2B?A7-I1	6-117		
F3	2B?A7-I?	6-117		
G?	2A1B2-L?	6-		SENSE REG FILE 00-37 BIT 27
G1	2A1B3-K?	6-		SENSE RF 00-37 NOT(BIT 24)
G2	2B2B8-J2	5- 77		BC PARTIAL WRITE BIT 02 TO PF
G3	2B2B8-J3	5- 77		
H0	2A1B5-W3	6- 45		RF=Z BIT 02
H1	2A1B5-B1	6- 45		INCR OR DECR BY 2 TO GROUP 0
H2	2B2B9-J?	5- 75		BC PARTIAL WRITE BIT 00 TO PF
H3	2B2B9-J3	5- 75		
I0	2A1B5-T?	6- 45		RF=Z BIT 00
I1	2A1B5-03	6- 45		RF=Z BIT 03
I2	2B2B9-H?	5- 75		
I3	2B2B9-H3	5- 75		BC PARTIAL WRITE BIT 01 TO PF
J0	2A1A8-J?	6- 55	2A1A8-AQ	RF SENSE AMPL BIT 24 TO GR 5
J1	2A1B2-K1	6-		SENSE RF 00-37 NOT(BIT 27)
J2	2B2B8-H?	5- 77		
J3	2B2B8-H3	5- 77		BC PARTIAL WRITE BIT 03 TO PF
K0	2A1A5-A?	6- 47		RF=Z BITS(04)(05)(06)(07)
K1	2A1B3-L1	6-		SENSE REG FILE 00-37 BIT 24
K2	2C?B2-W3	6-175		
K3	2C?B2-W2	6-175		SUPPR WORD MARK TO CHAN 4-7 FANOUT
L0	2A1A6-A?	6- 49		RF=Z BITS(08)(09)(10)(11)
L1	2A1A7-A?	6- 51		RF=Z BITS (12)(13)(14)(15)
L2	2A1B8-P?	6- 53		RF=Z BITS (17)(18)(19)
L3	2A1B5-W?	6- 45		CHARACTER ADDRESS DESIGNATOR 0
M0	2A1B8-E?	6- 53		RF=Z BIT 16 ONLY
M1	2A1B5-01	6- 45		RF=Z BIT 01
M2	2B1A7-B?	6- 1		NOT EN SET OF PARTIAL WRITES
M3	2B1A7-B3	6- 1		
N0	2B1A1-W1	6- 25		12-BIT MODE I/O CONT XLTN
N1	2B1A1-W?	6- 25		
N2	2B1A7-L1	6- 1		T158 TO Z PANEL - CLR/SET PARTIAL WRITE
N3	2B1A7-L?	6- 1		
O0	2B1A1-T1	6- 25		24-BIT MODE I/O CONT XLTN
O1	2B1A1-T?	6- 25		SENSE RF 00-37 NOT(BIT 25)
O2	2A1B3-K1	6-		SUPPR WORD MARK ON I/O ACT.
O3	2A1B6-H1	6- 43		RF=Z BITS (20)(21)(22)(23)
P0	2A1A8-T3	6- 55		NOT (I/O WITH A XLTN) TO CONT
P1	2A1B6-K1	6- 43		DECREMENT RF L17 TO BITS 06/07
P2	2A1A5-W3	6- 47		CHARACTER ADDRESS DESIGNATOR 1
P3	2A1B5-J?	6- 45		
Q0	2B1A6-I1	6- 13		STRIP/DUPLICATE CHAR.
Q1	2B1A6-I?	6- 13		INCREMENT RF L17 TO BITS 00/01
Q2	2A1B5-C?	6- 45		INCREMENT RF L17 TO BITS 06/07
Q3	2A1A5-X3	6- 47		
R0	2B1A6-K1	6- 13		RIGHT SHIFT 1 TO D4 XLTN FF
R1	2B1A6-K?	6- 13		DECREMENT RF L17 TO BITS 00/01
R2	2A1B5-C1	6- 45		NOT (T154) TO CHAR. AND WRITE
R3	2A1B7-V?	6- 41		STORAGE FFS
				STRIP/DUPLICATE BYTE
S0	2B1A6-H?	6- 13		
S1	2B1A6-H1	6- 13		DECREMENT RF L17 TO BITS 02/03
S2	2A1B5-C?	6- 45		INCREMENT RF L17 TO BITS 02/03
S3	2A1B5-B3	6- 45		RIGHT SHIFT 2 TO D4 XLTN FF
T0	2B1A6-J?	6- 13		
T1	2B1A6-J1	6- 13		DECREMENT RF L17 TO BITS 04/05
T2	2A1A5-X1	6- 47		INCREMENT RF L17 TO BITS 04/05
T3	2A1A5-X?	6- 47		
U0	2B1A1-X1	6- 25		I/O CONTROL XLTN
U1	2B1A1-X?	6- 25		DECREMENT RF L17 TO BITS 12/13
U2	2A1A7-X1	6- 51		INCREMENT RF L17 TO BITS 12-13
U3	2A1A7-X?	6- 51		
V0	2B1A7-W3	6- 1		I/O WRITE XLTN
V1	2B1A7-W?	6- 1		DECREMENT RF L17 TO BITS 14/15
V2	2A1A7-W3	6- 51		INCREMENT RF L17 TO BITS 14/15
V3	2A1A7-X3	6- 51		I/O WITH A XLTN
W0	2B1A7-F1	6- 1		
W1	2B1A7-F?	6- 1		INCREMENT RF L17 TO BITS 10/11
W2	2A1A6-X3	6- 49		DECREMENT RF L17 TO BITS 10/11
W3	2A1A6-W3	6- 49		SENSE RF 00-37 NOT(BIT 26)
X0	2A1B2-K?	6-		SENSE REG FILE 00-37 BIT 19
X1	2B1A7-01	6-		INCREMENT RF L17 TO BITS 08/09
X2	2A1A6-X?	6- 49		DECREMENT RF L17 TO BITS 08/09
X3	2A1A6-X1	6- 49		



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

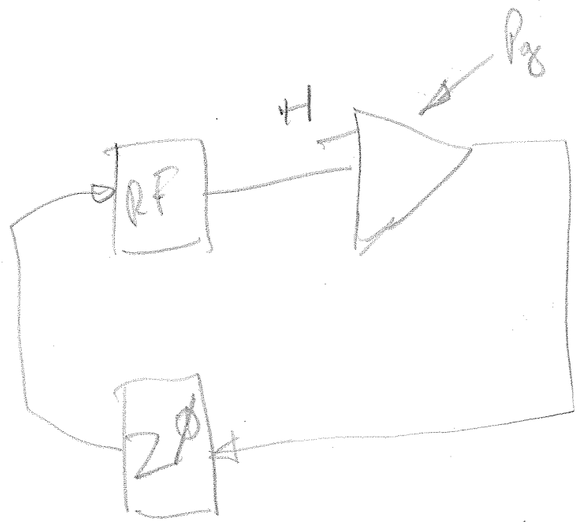
ZO TRANSLATIONS

LOC: 2A1B4 PART NO. 185161 SER. 000

PRODUCT
SIZE C | DRAWING NO. 60181000 | REV. E
SHEET | PAGE 6-57

241

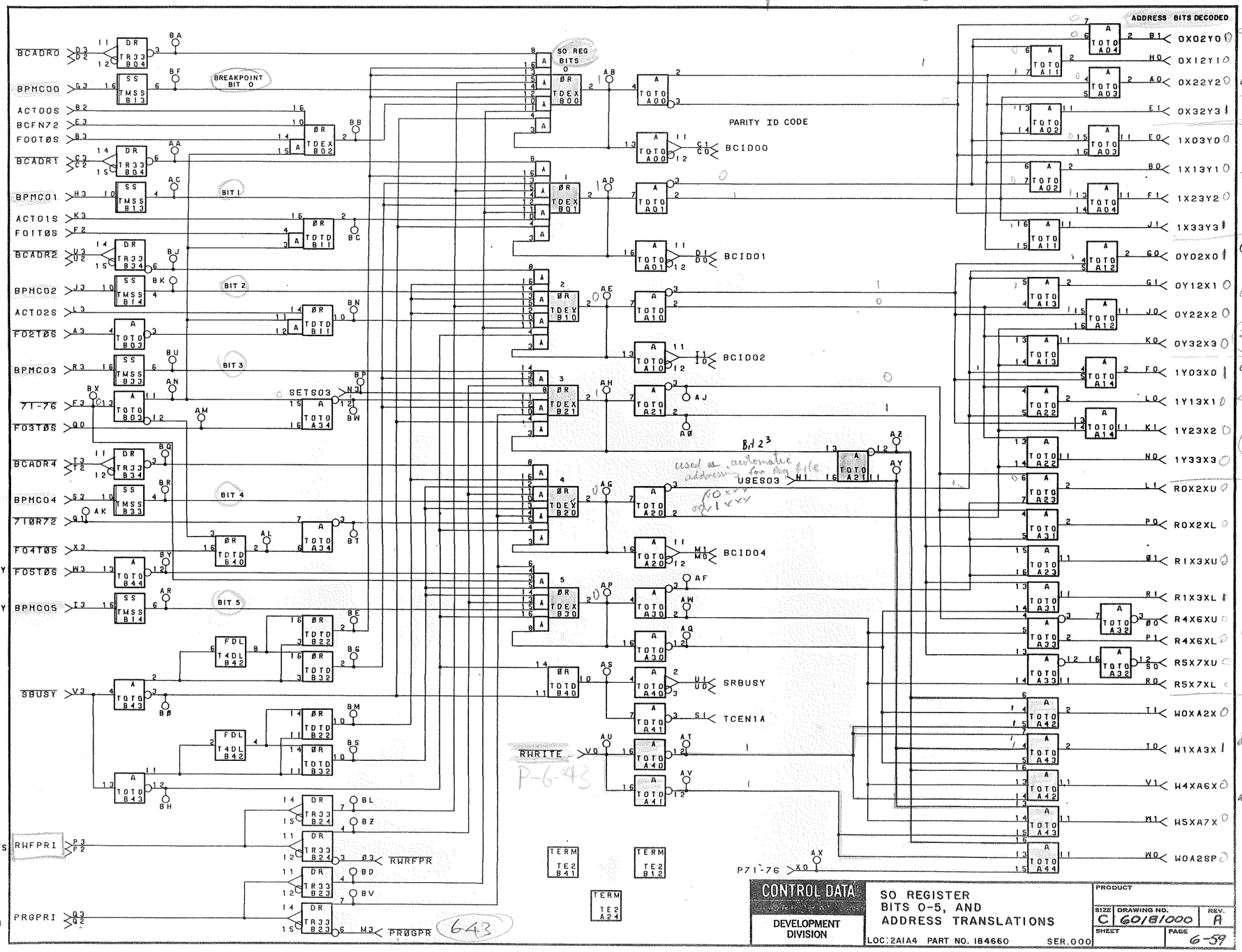
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A1A2-I1	6-		S BITS 01/00 = 2 TO RF 00-37
	2A1A3-K0	6-		
A3	2A1B5-F3	6- 45		NOT(F BIT 02) TO S REG FAN IN
B0	2A1A0-D1	6-		S BITS 01/00 = 1 TO RF 40-77
	2A1A1-C1	6-		
B1	2A1A2-F1	6-		S BITS 01/00 = 0 TO RF 00-37
	2A1A3-B1	6-		
B2	2A1B8-A3	6- 53		ACT. I/O ADDR BIT 00 TO S FAN-IN
B3	2A1B6-P3	6- 43		F BIT 00 TO S REG FAN IN
C0	2B2B8-C0	5- 77		
C1	2B2B8-C1	5- 77		BC IDENT, TO PF + MCS PE CODE
C2	2B1A1-O2	6- 25		NOT RF ADDR XLTN BIT 01 TO S
C3	2B1A1-O3	6- 25		
D0	2B2B9-E0	5- 75		
D1	2B2B9-E1	5- 75		BC IDENT, TO PF + MCS PE CODE
D2	2B1A1-M3	6- 25		NOT RF ADDR XLTN BIT 00 TO S
D3	2B1A1-M2	6- 25		



Example for Reg File 13.

E0	2A1A0-G1	6-			S BITS 01/00 = 0 TO RF 40-77
	2A1A1-B1	6-			
E1	2A1A2-G0	6-			S BITS 01/00 = 3 TO RF 00-37
	2A1A3-K1	6-			
E3	2A1B7-B1	6-	41		BC FCN CODE = 72
F0	2A1A1-G1	6-			S BITS 04/02 = 0 TO RF 40-77
	2A1A0-B1	6-			
F1	2A1A0-I1	6-			S BITS 01/00 = 2 TO RF 40-77
	2A1A1-K0	6-			
F2	2A1B6-Q3	6-	43		F BIT 01 TO S REG FAN IN
F3	2A1B6-T2	6-	43	2A1A4-RX	NOT (F = 71 THROUGH 76) TO S INPUT TRANSLATION
G0	2A1A3-G1	6-			S BITS 04/02 = 0 TO RF 00-37
	2A1A2-B1	6-			
G1	2A1A3-D1	6-			S BITS 04/02 = 1 TO RF 00-37
	2A1A2-C1	6-			
G3	2A1A06J16E-06				BREAK POINT SWITCH BIT 0
H0	2A1A2-E1	6-			S BITS 01/00 = 1 TO RF 00-37
	2A1A3-C1	6-			
H3	2A1A06J16E-05				BREAK POINT SWITCH BIT 1
I0	2B2B8-D0	5-	77		BC IDENT, TO PF = MCS PE CODE
I1	2B2B6-D1	5-	77		
I3	2A1A06J16E-01				BREAK POINT SWITCH BIT 5
J0	2A1A3-I1	6-			S BITS 04/02 = 2 TO RF 00-37
	2A1A2-K0	6-			
J1	2A1A0-G0	6-			S BITS 01/00 = 3 TO RF 40-77
	2A1A1-K1	6-			
J3	2A1A06J16E-04				BREAK POINT SWITCH BIT 2
K0	2A1A3-G0	6-			S BITS 04/02 = 3 TO RF 00-37
	2A1A2-K1	6-			
K1	2A1A1-I1	6-			S BITS 04/02 = 2 TO RF 40-77
	2A1A0-K0	6-			
K3	2A1B8-H2	6-	53		ACT, I/O ADDR BIT 01 TO S FAN-IN
L0	2A1A1-D1	6-			S BITS 04/02 = 1 TO RF 40-77
	2A1A0-C1	6-			
L1	2A1B2-G1	6-			READ RF 0X AND 2X UPPER BITS
	2A1B3-H0	6-			
L3	2A1B8-I2	6-	53		ACT, I/O ADDR BIT 02 TO S FAN-IN
M0	2B2B8-E0	5-	77		
M1	2B2B8-E1	5-	77		BC IDENT, TO PF = MCS PE CODE
M3	2A1B6-B0	6-	43		NOT(PROGRAM OPR, XLTN)=Z CONT
N0	2A1A1-G0	6-			S BITS 04/02 = 3 TO RF 40-77
	2A1A0-K1	6-			
N1	2A1B6-H2	6-	43		USE S REG BIT 03 = WRITE XLTN
N3	2A1B6-R1	6-	43	2A1A4-BP	SET S REG BIT 03 = BPR XLTN
O0	2A1B0-G1	6-			READ RF 4X AND 6X UPPER BITS
	2A1B1-H0	6-			
O1	2A1B2-I1	6-			READ RF 1X AND 3X UPPER BITS
	2A1B3-H1	6-			
O3	2A1B6-B1	6-	43		NOT (READ/WRITE RF XLTN) = Z CONTROL
P0	2A1B3-I1	6-			READ RF 0X AND 2X LOWER BITS
	2A1B2-H1	6-			
P1	2A1B1-I1	6-			READ RF 4X AND 6X LOWER BITS
	2A1B0-H1	6-			
P2	2B1A1-H0	6-	25		
P3	2B1A1-H1	6-	25		R/W REG FILE FINAL BC PRIORITY
Q0	2A1B5-K2	6-	45	2A1A4-AM	NOT(F BIT 03) TO S REG FAN IN
Q1	2A1B6-V3	6-	43	2A1A4-AK	NOT(F=71-72) TO S INPUT XLTNS
Q2	2B1A1-N1	6-	25		
Q3	2B1A1-N0	6-	25		PROG CONTROL FINAL BC PRIORITY
R0	2A1B1-G1	6-			READ RF 5X AND 7X LOWER BITS
	2A1B0-H0	6-			
R1	2A1B3-G1	6-			READ RF 1X AND 3X LOWER BITS
	2A1B2-H0	6-			
R3	2A1A06J16E-03				BREAK POINT SWITCH BIT 3
S0	2A1B0-I1	6-			READ RF 5X AND 7X UPPER BITS
	2A1B1-H1	6-			
S1	2A1B7-I0	6-	41	2A1B7-AF	NOT(S REG BUSY) = EN TIMING CHAIN START
S3	2A1A06J16E-02				BREAK POINT SWITCH BIT 4
T0	2A1B2-D1	6-			WRITE RF 1X AND 3X 24 BITS
	2A1B3-C0	6-			
T1	2A1B3-D1	6-			WRITE RF 0X AND 2X 24 BITS
	2A1B2-C0	6-			
T2	2B1A1-N2	6-	25		NOT RF ADDR XLTN BIT 04 TO S
T3	2B1A1-N3	6-	25		
U0	2B1A6-X0	6-	13		
U1	2B1A6-X1	6-	13		S REG BUSY TO D4 XLTN
U2	2B1A1-L3	6-	25		NOT RF ADDR XLTN BIT 02 TO S
U3	2B1A1-L2	6-	25		
V0	2A1B6-G3	6-	43	2A1A4-AU	NOT(WRITE REGISTER FILE F/F)
V1	2A1B1-D1	6-			WRITE RF 4X AND 6X 24 BITS
	2A1B0-C0	6-			
V3	2A1B6-J2	6-	43		NOT(ADDRESS BUSY) TO S REG
W0	2A1B3-C1	6-			WRITE RF 0X AND 2X CONT. BITS
	2A1B2-F1	6-			
W1	2A1B0-D1	6-			WRITE RF 5X AND 7X 24 BITS
	2A1B1-C0	6-			
W3	2A1A5-N1	6-	47		NOT (F BIT 05) TO S REG FAN-IN
X0	2A1B6-U2	6-	43	2A1A4-AX	F=71 THRU 76 TO EN RF WRITE CONTROL BITS
X3	2A1A5-N0	6-	47		NOT(F BIT 04) TO S REG FAN IN

PAGE 6-59



243

REGISTER FILE
ADDRESSING SCHEME

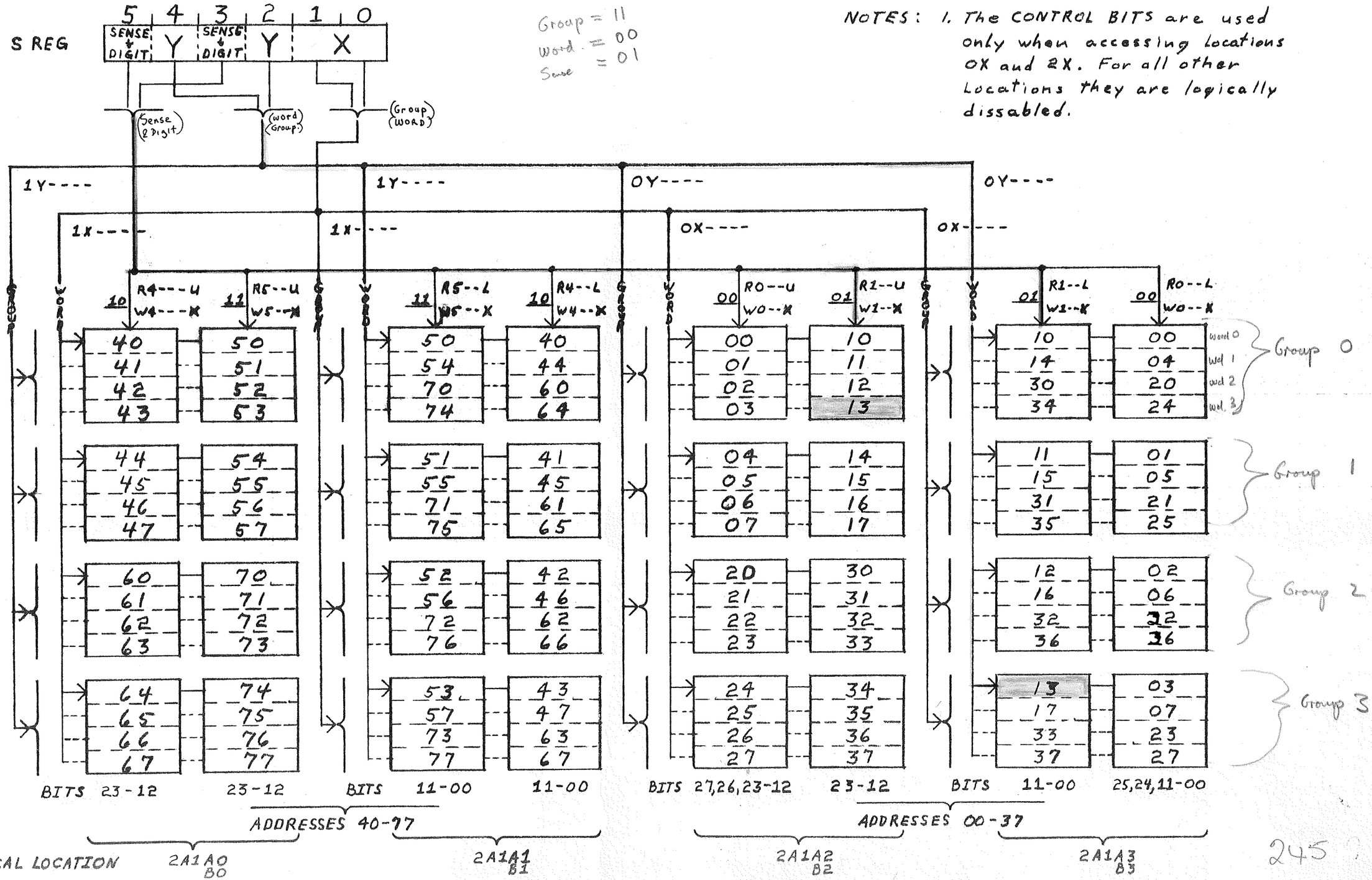
0	0	1	0	1	1

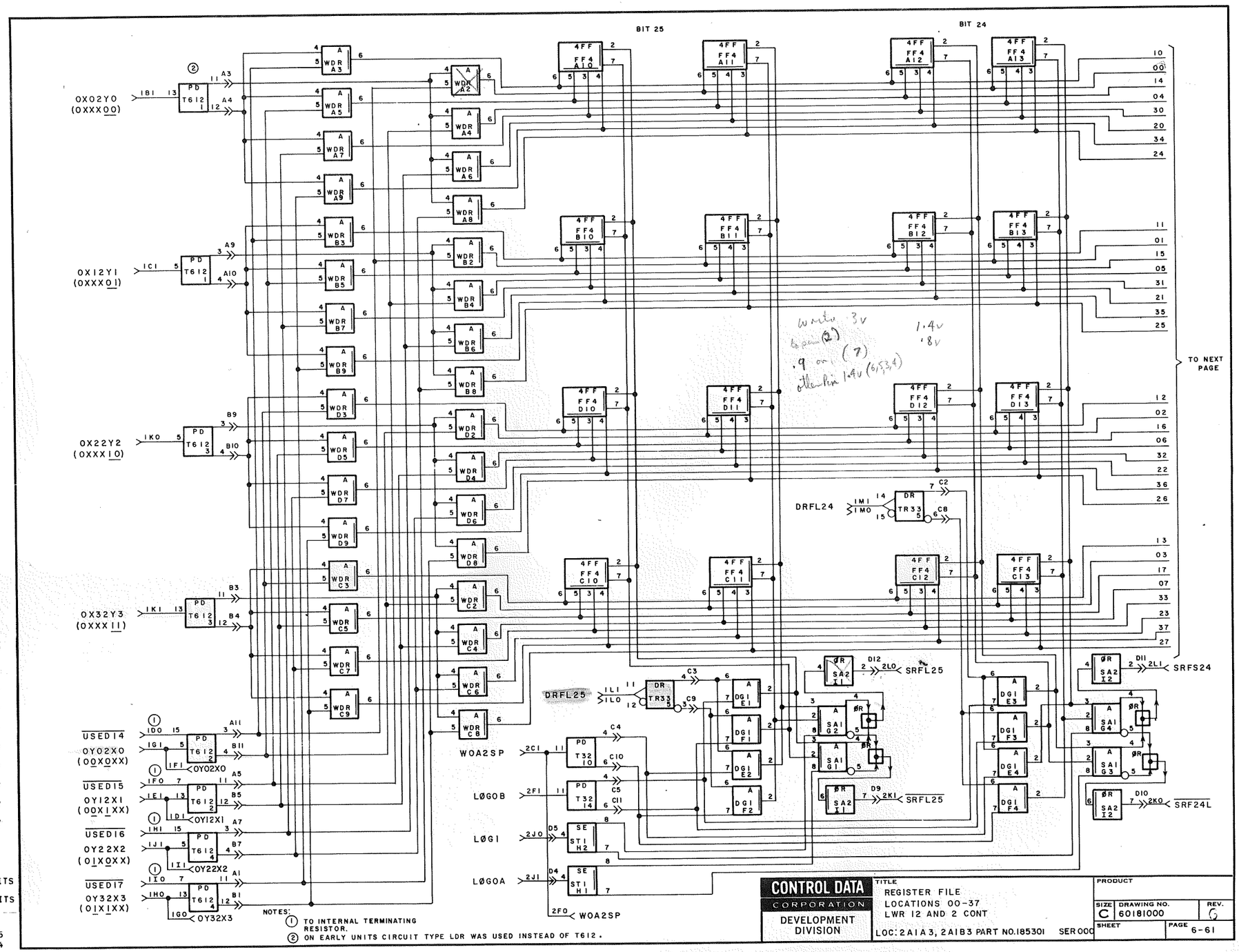
S REG

5	4	3	2	1	0
SENSE DIGIT	Y	SENSE DIGIT	Y	X	

Group = 11
Word = 00
Sense = 01

NOTES: 1. The CONTROL BITS are used only when accessing locations 0X and 2X. For all other Locations they are logically dissabled.





PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1B1	2A1A2-G1	6- 67	S BITS 01/00 = 0 TO RF 00-37
	2A1A4-B1	6- 59	
1C1	2A1A2-D1	6- 67	S BITS 01/00 = 1 TO RF 00-37
	2A1A4-H0	6- 59	
1D1	2A1A4-G1	6- 59	S BITS 04/02 = 1 TO RF 00-37
1E1	2A1A2-C1	6- 67	S BITS 04/02 = 1 TO RF 00-37
1F1	2A1A2-B1	6- 67	S BITS 04/02 = 0 TO RF 00-37
1G0	2A1A4-K0	6- 59	S BITS 04/02 = 3 TO RF 00-37
1G1	2A1A4-G0	6- 59	S BITS 04/02 = 0 TO RF 00-37
1H0	2A1A2-K1	6- 67	S BITS 04/02 = 3 TO RF 00-37
1J1	2A1A4-J0	6- 59	S BITS 04/02 = 2 TO RF 00-37
1J1	2A1A2-K0	6- 67	S BITS 04/02 = 2 TO RF 00-37
1K0	2A1A2-J1	6- 67	S BITS 01/00 = 2 TO RF 00-37
	2A1A4-A0	6- 59	
1K1	2A1A2-H0	6- 67	S BITS 01/00 = 3 TO RF 00-37
	2A1A4-E1	6- 59	
1L0	2B1A9-X3	6- 23	
1L1	2B1A9-X2	6- 23	DIGIT DRIVE 25 TO RF 00-37
1M0	2B1A9-J3	6- 23	
1M1	2B1A9-J2	6- 23	DIGIT DRIVE 24 TO RF 00-37
2C1	2A1A4-W0	6- 59	WRITE RF 0X AND 2X CONT. BITS
2F0	2A1H2-F1	6- 67	WRITE RF 0X AND 2X CONT. BITS
2A0	2A1H4-G1	6- 57	SENSE RF 00-37 NOT(BIT 24)
2A1	2A1H4-G2	6- 57	SENSE RF 00-37 NOT(BIT 25)
2L0	2A1A8-J1	6- 55	SENSE REG FILE 00-37 BIT 25
2L1	2A1H4-K1	6- 57	SENSE REG FILE 00-37 BIT 24

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE: REGISTER FILE LOCATIONS 00-37 LWR 12 AND 2 CONT	PRODUCT	
	LOC: 2A1A3, 2A1B3 PART NO. 185301 SER 000	SIZE C	DRAWING NO. 60181000
		REV. G	
		SHEET	PAGE 6-61

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1N0	2A1A6-H2	6- 49	
1N1	2A1A6-H3	6- 49	NOT DIGIT DR 10 TO RF 00-37
1U0	2A1A6-E3	6- 49	
1U1	2A1A6-E2	6- 49	NOT DIGIT DR 11 TO RF 00-37
1P0	2A1A6-F0	6- 49	
1P1	2A1A6-F1	6- 49	NOT DIGIT DR 09 TO RF 00-37
1W0	2A1A6-I1	6- 49	
1W1	2A1A6-I0	6- 49	NOT DIGIT DR 08 TO RF 00-37
1R0	2A1A5-E3	6- 47	
1R1	2A1A5-E2	6- 47	NOT DIGIT DR 07 TO RF 00-37
1S0	2A1A5-H2	6- 47	
1S1	2A1A5-H3	6- 47	NOT DIGIT DR 06 TO RF 00-37
2C0	2A1H2-D0	6- 69	WRITE RF 1X AND 3X 24 BITS
	2A1A4-T0	6- 59	
2D0	2A1H2-C0	6- 69	WRITE RF 0X AND 2X 24 BITS
2D1	2A1A4-T1	6- 59	WRITE RF 0X AND 2X 24 BITS
2G0	2A1H2-H0	6- 69	READ RF 1X AND 3X LOWER BITS
2G1	2A1A4-R1	6- 59	READ RF 1X AND 3X LOWER BITS
2H0	2A1B2-G0	6- 69	READ RF 0X AND 2X UPPER BITS
	2A1A4-L1	6- 59	
2H1	2A1B2-I0	6- 69	READ RF 1X AND 3X UPPER BITS
	2A1A4-Φ1	6- 59	
2I0	2A1H2-H1	6- 69	READ RF 0X AND 2X LOWER BITS
2I1	2A1A4-P0	6- 59	READ RF 0X AND 2X LOWER BITS
2M0	2A1A5-S3	6- 47	SENSE RF 00-37 NOT(BIT 07)
2M1	2A1A6-S0	6- 49	SENSE RF 00-37 NOT(BIT 08)
2N1	2A1A5-T3	6- 47	SENSE RF 00-37 NOT(BIT 06)
2W0	2A1A6-S3	6- 49	SENSE RF 00-37 NOT(BIT 11)
2R0	2A1A6-S1	6- 49	SENSE RF 00-37 NOT(BIT 09)
2R1	2A1A6-T3	6- 49	SENSE RF 00-37 NOT(BIT 10)

BIT 11 | BIT 10 | BIT 09 | BIT 08 | BIT 07 | BIT 06

FROM PREVIOUS PAGE

10 00 14 04 30 20 34 24 11 01 15 05 31 21 35 25 12 02 16 06 32 22 36 26 13 03 17 07 33 23 37 27

4FF FF4 A14 … A25 / B14 … B25 / D14 … D25 / C14 … C25

DRFLIO ← 1N1 / 1N0 *

USED12 ← 2E0 — TERM TE2 18

USED13 ← 2E1 — TERM TE2 18

DRFLII ← 1Ø1 / 1Ø0 *

DRFLO8 → USEDIO, SRFLIO

DRFLO9 → USEDII, SRFLII

IQ1 / IQ0 * → DRFLO6 → USED08, SRFLO8

IP1 / IP0 * → DRFLO7 → USED09, SRFLO9

IS1 / IS0 * → DRFLO6 → USED06, SRFLO6

IR1 / IR0 * → DRFLO7 → USED07, SRFLO7

2D1 WOXA2X → WOXA2X 2DO → PD T422 19 → PD T104 15 → E13A, E5B, E13B, E5A

2C1 WIXA3X → WIXA3X 2CO → PD T422 19 → PD T104 11 → E14A, E6B, E14B, E6A

RIX3XU 2H1 (1) → E18B
ROX2XL 2IO → 2I1 ROX2XL → PD T612 20 (2)

ROX2XU 2HO (1) → E18A
RIX3XL 2GO → 2G1 RIX3XL → PD T612 20 12

WOXA2X TO T104
WIXA3X TO T104

ROX2XL TO F18B
RIX3XL TO F18A

TO NEXT PAGE

NOTE:
(1) TO INTERNAL TERMINATING RESISTOR
(2) ON EARLY UNITS CIRCUIT TYPE LDR WAS USED INSTEAD OF T612.

CONTROL DATA CORPORATION — DEVELOPMENT DIVISION

TITLE: REGISTER FILE LOCATIONS 00-37 LOWER 12 AND 2 CONT
2A1A3
LOC: 2A1B3 PART NO. 185301 SER. 000

PRODUCT

SIZE	DRAWING NO.	REV.
C	60181000	G

SHEET | PAGE 6-63

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1t0	2A1A5-P2	6- 45	
1t1	2A1A5-P3	6- 45	NOT DIGIT DR 03 TO RF 00-37
1u0	2A1A5-I1	6- 47	
1u1	2A1A5-I0	6- 47	NOT DIGIT DR 04 TO RF 00-37
1v0	2A1A5-F0	6- 47	
1v1	2A1A5-F1	6- 47	NOT DIGIT DR 05 TO RF 00-37
1w0	2A1A5-X2	6- 45	
1w1	2A1A5-X3	6- 45	NOT DIGIT DR 02 TO RF 00-37
1x0	2A1A5-P0	6- 45	
1x1	2A1A5-P1	6- 45	NOT DIGIT DR 01 TO RF 00-37
2s0	2A1A5-X1	6- 45	
2s1	2A1A5-X0	6- 45	NOT DIGIT DR 00 TO RF 00-37
2t0	2A1A5-H0	6- 45	SENSE RF 00-37 NOT(BIT 01)
2t1	2A1A5-C3	6- 45	SENSE RF 00-37 NOT(BIT 02)
2u1	2A1A5-D0	6- 45	SENSE RF 00-37 NOT(BIT 00)
2w0	2A1A5-S1	6- 47	SENSE RF 00-37 NOT(BIT 05)
2x0	2A1A5-A3	6- 45	SENSE RF 00-37 NOT(BIT 03)
2x1	2A1A5-S0	6- 47	SENSE RF 00-37 NOT(BIT 04)

BIT 05 BIT 04 BIT 03 BIT 02 BIT 01 BIT 00

FROM PREVIOUS PAGE

10 00 14 04 30 20 34 24 11 01 15 05 31 21 35 25 12 02 16 06 32 22 36 26 13 03 17 07 33 23 37 27

4FF FF4 A26 · A27 · A28 · A29 · A30 · A31 · A32 · A33 · A34 · A35 · A36 · A37
4FF FF4 B26 · B27 · B28 · B29 · B30 · B31 · B32 · B33 · B34 · B35 · B36 · B37
4FF FF4 D26 · D27 · D28 · D29 · D30 · D31 · D32 · D33 · D34 · D35 · D36 · D37
4FF FF4 C26 · C27 · C28 · C29 · C30 · C31 · C32 · C33 · C34 · C35 · C36 · C37

CLMP CCI A38 · CCI A39 · CCI B38 · CCI B39 · CCI C38 · CCI C39 · CCI D38 · CCI D39

DRFLO4 ← IUI IUO *
DRFLO5 ← IVI IVO *
DRFLO2 ← IWI IWO *
DRFLO3 ← ITI ITO *
DRFLOO ← 2BI 2BO *
DRFLO1 ← IXI IXO *

DR TR33 I5 · I3 · I9 · I7

F3A · F11A · F2A · F10A · F4B · F12B · F4A · F12A · F2B · F10B · F3B · F11B

DGI E24 · F24 · E23 · F23 · E22 · F22 · E21 · F21 · E28 · F28 · E27 · F27 · E26 · F26 · E25 · F25 · E32 · F32 · E31 · F31 · E30 · F30 · E29 · F29

SAI G20 · G19 · G18 · G17 · G24 · G23 · G22 · G21 · G28 · G27 · G26 · G25

CONV SA2 I10 · I9 · I11 · I12 · I14 · I13

F26A 2VO USED04 · F23A 2XI SRFL04 · F25A 2WI USED05 · F24A 2WO SRFL05 · F27B 2UO USED02 · F22B 2SI SRFL02 · F27A 2VI USED03 · F22A 2XO SRFL03 · F25B 2TO USED00 · F24B 2TI SRFL00 · F26B 2UI USED01 · F23B 2SO SRFL01

FROM PREVIOUS PAGE

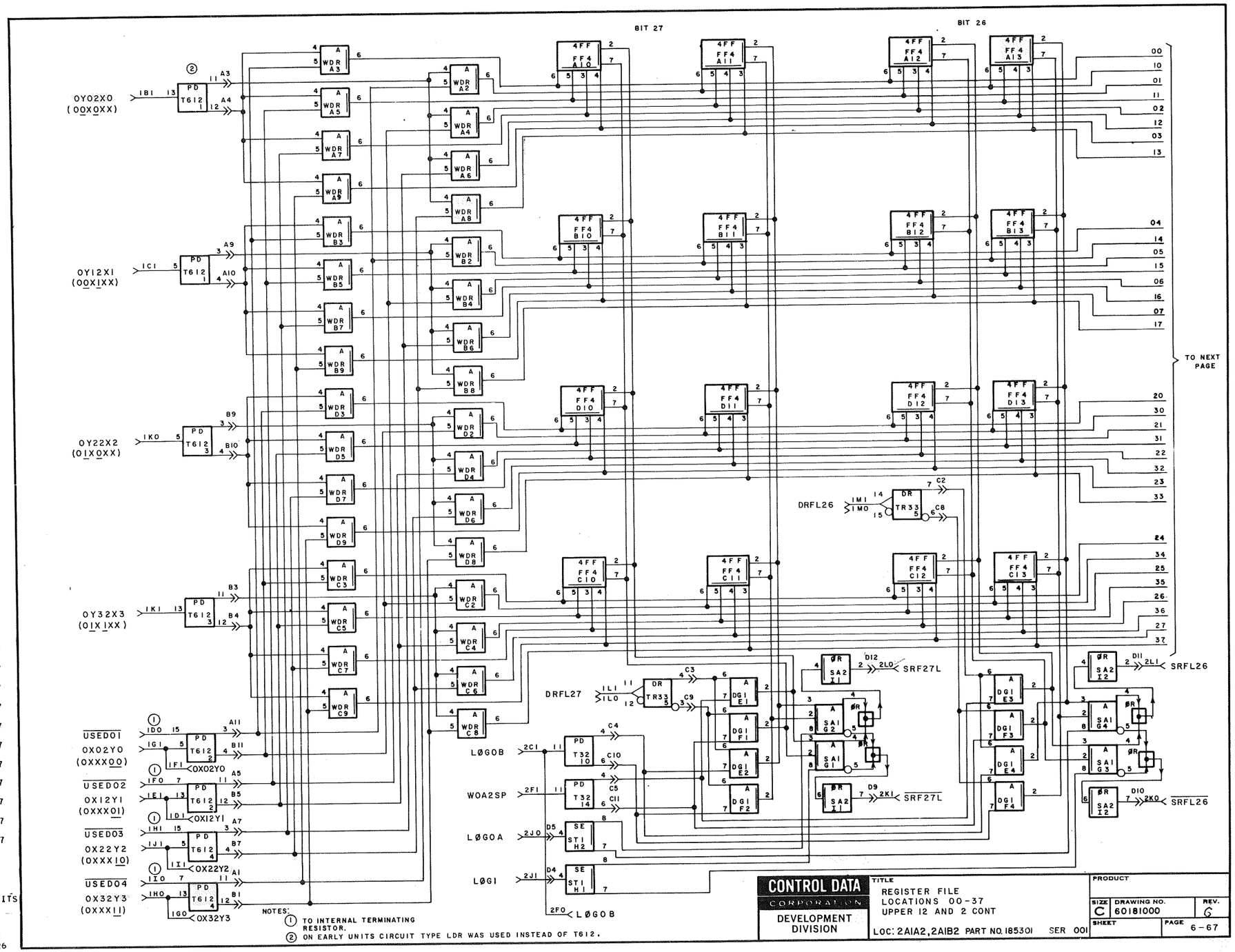
WOXA2X → PD TI04 I6 → F5A · F13A · F5B · F13B
WIXA3X → PD TI04 I2 → F6A · F14A · F6B · F14B
R1X3XL → F18A → SE STI H9
ROX2XL → F18B → SE STI H10
SE STI H11 · SE STI H12 · SE STI H13 · SE STI H14

251

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE
REGISTER FILE
LOCATIONS 00-37
LOWER I2 AND 2 CONT
2A1A3
LOC: 2A1B3 PART NO. 165301 SER 00C

PRODUCT
SIZE C | DRAWING NO. 60181000 | REV. A
PAGE 6-65



PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1B1	2A1A3-F1	6-61	S BITS 04/02 = 0 TO RF 00-37
	2A1A4-G0	6-59	
1C1	2A1A3-E1	6-61	S BITS 04/02 = 1 TO RF 00-37
	2A1A4-G1	6-59	
1U1	2A1A3-C1	6-61	S BITS 01/00 = 1 TO RF 00-37
1E1	2A1A4-H0	6-59	S BITS 01/00 = 1 TO RF 00-37
1F1	2A1A4-B1	6-59	S BITS 01/00 = 0 TO RF 00-37
1U0	2A1A4-E1	6-59	S BITS 01/00 = 3 TO RF 00-37
1U1	2A1A3-B1	6-61	S BITS 01/00 = 0 TO RF 00-37
1M0	2A1A3-K1	6-61	S BITS 01/00 = 3 TO RF 00-37
1J1	2A1A4-A0	6-59	S BITS 01/00 = 2 TO RF 00-37
	2A1A3-K0	6-61	S BITS 01/00 = 2 TO RF 00-37
1K0	2A1A3-J1	6-61	S BITS 04/02 = 2 TO RF 00-37
	2A1A4-J0	6-59	
1K1	2A1A3-H0	6-61	S BITS 04/02 = 3 TO RF 00-37
	2A1A4-K0	6-59	
1L0	2B1A7-F2	6-1	
1L1	2B1A7-F3	6-1	DIGIT DRIVE 27 TO RF 00-37
1M0	2B1A9-T3	6-23	
1M1	2B1A9-T2	6-23	DIGIT DRIVE 26 TO RF 00-37
2F1	2A1A3-F0	6-61	WRITE RF 0X AND 2X CONT. BITS
	2A1A4-A0	6-59	
2A0	2A1A4-K0	6-57	SENSE RF 00-37 NOT(BIT 26)
2A1	2A1A4-J1	6-57	SENSE RF 00-37 NOT(BIT 27)
2L0	2A1A4-G0	6-57	SENSE REG FILE 00-37 BIT 27
2L1	2A1A4-G1	6-55	SENSE REG FILE 00-37 BIT 26

CONTROL DATA CORPORATION	TITLE	PRODUCT
DEVELOPMENT DIVISION	REGISTER FILE LOCATIONS 00-37 UPPER 12 AND 2 CONT	SIZE C · DRAWING NO. 60181000 · REV. 6
	LOC: 2A1A2,2A1B2 PART NO. 185301 SER 001	SHEET · PAGE 6-67

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1W0	2A1A8-Q2	6- 55	
1W1	2A1A8-Q3	6- 55	NOT DIGIT DR 22 TO RF 00-07
1U0	2A1A8-O2	6- 55	
1U1	2A1A8-O3	6- 55	NOT DIGIT DR 23 TO RF 00-37
1P0	2A1A8-K2	6- 55	
1P1	2A1A8-K3	6- 55	NOT DIGIT DR 21 TO RF 00-37
1W0	2A1A8-J3	6- 55	
1W1	2A1A8-J2	6- 55	NOT DIGIT DR 20 TO RF 00-37
1R0	2A1A7-G1	6- 41	
1R1	2A1A7-G0	6- 41	DIGIT DRIVE 19 TO RF 00-37
1S0	2A1A7-F2	6- 41	
1S1	2A1A7-F3	6- 41	DIGIT DRIVE 18 TO RF 00-37
2L0	2A1A3-D0	6- 63	WRITE RF 0X AND 2X 24 BITS
	2A1A4-T1	6- 59	
2U0	2A1A3-C0	6- 63	WRITE RF 1X AND 3X 24 BITS
2U1	2A1A4-T0	6- 59	WRITE RF 1X AND 3X 24 BITS
2V0	2A1A3-H0	6- 63	READ RF 0X AND 2X UPPER BITS
2V1	2A1A4-L1	6- 59	READ RF 0X AND 2X UPPER BITS
2H0	2A1B3-G0	6- 63	READ RF 1X AND 3X LOWER BITS
	2A1A4-R1	6- 59	
2H1	2A1B3-I0	6- 63	READ RF 0X AND 2X LOWER BITS
	2A1A4-P0	6- 59	
2L0	2A1A3-H1	6- 63	READ RF 1X AND 3X UPPER BITS
2L1	2A1A4-G1	6- 59	READ RF 1X AND 3X UPPER BITS
2M0	2A1A8-M3	6- 53	SENSE RF 00-37 NOT(BIT 19)
2M1	2A1A8-A0	6- 55	SENSE RF 00-37 NOT(BIT 20)
2N1	2A1A8-R1	6- 53	SENSE RF 00-37 NOT(BIT 18)
2U1	2A1A4-X1	6- 57	SENSE REG FILE 00-37 BIT 19
2W0	2A1A8-N1	6- 55	SENSE RF 00-37 NOT(BIT 23)
2R0	2A1A8-C0	6- 55	SENSE RF 00-37 NOT(BIT 21)
2M1	2A1A8-M1	6- 55	SENSE RF 00-37 NOT(BIT 22)

BIT 23 | BIT 22 | BIT 21 | BIT 20 | BIT 19 | BIT 18

FROM PREVIOUS PAGE

TO NEXT PAGE

00 10 01 11 02 12 03 13 04 14 05 15 06 16 07 17 20 30 21 31 22 32 23 33 24 34 25 35 26 36 27 37

4FF FF4 A14 | 4FF FF4 A15 | 4FF FF4 A16 | 4FF FF4 A17 | 4FF FF4 A18 | 4FF FF4 A19 | 4FF FF4 A20 | 4FF FF4 A21 | 4FF FF4 A22 | 4FF FF4 A23 | 4FF FF4 A24 | 4FF FF4 A25

4FF FF4 B14 | 4FF FF4 B15 | 4FF FF4 B16 | 4FF FF4 B17 | 4FF FF4 B18 | 4FF FF4 B19 | 4FF FF4 B20 | 4FF FF4 B21 | 4FF FF4 B22 | 4FF FF4 B23 | 4FF FF4 B24 | 4FF FF4 B25

4FF FF4 D14 | 4FF FF4 D15 | 4FF FF4 D16 | 4FF FF4 D17 | 4FF FF4 D18 | 4FF FF4 D19 | 4FF FF4 D20 | 4FF FF4 D21 | 4FF FF4 D22 | 4FF FF4 D23 | 4FF FF4 D24 | 4FF FF4 D25

4FF FF4 C14 | 4FF FF4 C15 | 4FF FF4 C16 | 4FF FF4 C17 | 4FF FF4 C18 | 4FF FF4 C19 | 4FF FF4 C20 | 4FF FF4 C21 | 4FF FF4 C22 | 4FF FF4 C23 | 4FF FF4 C24 | 4FF FF4 C25

DRFL22 INI INO *

USED00 2E0 TERM TE2 18

LØGOB 2E1

DRFL23 1B1 1B0 *

DRFL20

DRFL21

DRFL18

DRFL19

IQI IQO * IPI IPO *

1S1 1S0 IR1 IRO

DR TR33 E11A E12B E10A E12A E10B E11B

USED22 SRFL22 USED23 SRFL23 USED20 SRFL20 USED21 SRFL21 USED18 SRFL18 USED19 SRFL19

SAI G7 G8 G5 G6 G11 G12 G9 G10 G15 G16 G13 G14

ØR

CONV SA2 I4 I3 I6 I5 I8 I7

2PO 2RI 2QI 2QO 2PI 2RO 2NO 2NI 2QI 2MO

DGI E10 F10 E9 F9 E8 F8 E7 F7 E14 E13 E12 F13 E11 F11 E16 F18 E17 F17 E16 F16 E15 F15

SE STI H4 H3 H6 H5 H8 H7

PD T422 19 T104 15 11 T612 20

WIXA3X 2D0 2D1

WOXA2X 2C0

ROX2XL 2H1 ROX2XU 2G0 2G1

RIX3XU 2I0 2I1

RIX3XL 2H0

E3A E5A E13A E5B E13B E6A E14A E6B E14B E18B E18A E4B E4A E2B E3B E26A E23A E25A E24A E27B E22B E27A E22A E25B E24B E26B E23B

WIXA3X TO T104

WOXA2X TO T104

RIX3XU TO F18B

ROX2XU TO F18A

TO NEXT PAGE

NOTE:

(1) TO INTERNAL TERMINATING RESISTOR

(2) ON EARLY UNITS CIRCUIT TYPE LOR WAS USED INSTEAD OF T612.

CONTROL DATA DEVELOPMENT DIVISION

TITLE: REGISTER FILE LOCATIONS 00-37 UPPER 12 AND 2 CONT 2A1A2 LOC: 2A1B2 PART NO. 185301 SER.001

PROJECT

SIZE C | DRAWING NO. 60181000 | REV.

SHEET | PAGE 6-69

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1T0	2A1A7-E3	6- 51	
1T1	2A1A7-E2	6- 51	NOT DIGIT DR 15 TO RF 00-37
1U0	2A1B8-T0	6- 53	
1U1	2A1B8-T1	6- 53	NOT DIGIT DR 16 TO RF 00-37
1V0	2A1B7-C3	6- 41	
1V1	2A1B7-C2	6- 41	DIGIT DRIVE 17 TO RF 00-37
1W0	2A1A7-H2	6- 51	
1W1	2A1A7-H3	6- 51	NOT DIGIT DR 14 TO DR 00-37
1X0	2A1A7-F0	6- 51	
1X1	2A1A7-F1	6- 51	NOT DIGIT DR 13 TO DR 00-37
2U0	2A1A7-I1	6- 51	
2U1	2A1A7-I0	6- 51	NOT DIGIT DR 12 TO RF 00-37
2S0	2A1A7-S1	6- 51	SENSE RF 00-37 NOT(BIT 13)
2S1	2A1A7-T3	6- 51	SENSE RF 00-37 NOT(BIT 14)
2T1	2A1A7-S0	6- 51	SENSE RF 00-37 NOT(BIT 12)
2W0	2A1B8-J0	6- 53	SENSE RF 00-37 NOT(BIT 17)
2X0	2A1A7-S3	6- 51	SENSE RF 00-37 NOT(BIT 15)
2X1	2A1B8-H1	6- 53	SENSE RF 00-37 NOT(BIT 16)

BIT 17 BIT 16 BIT 15 BIT 14 BIT 13 BIT 12

FROM PREVIOUS PAGE

00 10 01 11 02 12 03 13 04 14 05 15 06 16 07 17 20 30 21 31 22 32 23 33 24 34 25 35 26 36 27 37

4FF FF4 A26 · 4FF FF4 A27 · 4FF FF4 A28 · 4FF FF4 A29 · 4FF FF4 A30 · 4FF FF4 A31 · 4FF FF4 A32 · 4FF FF4 A33 · 4FF FF4 A34 · 4FF FF4 A35 · 4FF FF4 A36 · 4FF FF4 A37 → CLMP CCI A38, CCI A39

4FF FF4 B26 · 4FF FF4 B27 · 4FF FF4 B28 · 4FF FF4 B29 · 4FF FF4 B30 · 4FF FF4 B31 · 4FF FF4 B32 · 4FF FF4 B33 · 4FF FF4 B34 · 4FF FF4 B35 · 4FF FF4 B36 · 4FF FF4 B37 → CLMP CCI B38, CCI B39

4FF FF4 D26 · 4FF FF4 D27 · 4FF FF4 D28 · 4FF FF4 D29 · 4FF FF4 D30 · 4FF FF4 D31 · 4FF FF4 D32 · 4FF FF4 D33 · 4FF FF4 D34 · 4FF FF4 D35 · 4FF FF4 D36 · 4FF FF4 D37 → CLMP CCI C38, CCI C39

4FF FF4 C26 · 4FF FF4 C27 · 4FF FF4 C28 · 4FF FF4 C29 · 4FF FF4 C30 · 4FF FF4 C31 · 4FF FF4 C32 · 4FF FF4 C33 · 4FF FF4 C34 · 4FF FF4 C35 · 4FF FF4 C36 · 4FF FF4 C37 → CLMP CCI D38, CCI D39

DRFLI6 ← IUI, IUO *
DR TR33 9 · F3A · F11A
DGI E24 · DGI F24 · DGI E23 · DGI F23 · DGI F22 · DGI E21 · DGI F21
SAI G20 · SAI G19 · ØR · CONV SA2 I10 → F26A 2VO → USEDI6
SAI G19 · ØR · CONV SA2 I10 → F23A 2XI → SRFLI6

DRFLI7 ← IVI, IVO *
DR TR33 13 · F2A · F10A
DGI F23 · DGI F22 · DGI E21 · DGI F21 · DGI E24 · DGI F24 · DGI E23
SAI G18 · SAI G17 · ØR · CONV SA2 I9 → F25A 2WI → USEDI7
SAI G17 · ØR · CONV SA2 I9 → F24A 2WO → SRFLI7

DRFLI4 ← IWI, IWO *
DR TR33 13 · F4B · F12B
DGI E28 · DGI F28 · DGI E27 · DGI F27 · DGI E26 · DGI F26 · DGI E25 · DGI F25
SAI G24 · SAI G23 · ØR · CONV SA2 I12 → F27B 2UO → USEDI4
SAI G23 · ØR · CONV SA2 I12 → F22B 2SI → SRFLI4

DRFLI5 ← ITI, ITO *
DR TR33 9 · F4A · F12A
DGI E26 · DGI F26 · DGI E25 · DGI F25 · DGI E28 · DGI F28 · DGI E27
SAI G22 · SAI G21 · ØR · CONV SA2 I11 → F27A 2VI → USEDI5
SAI G21 · ØR · CONV SA2 I11 → F22A 2XO → SRFLI5

DRFLI2 ← 2BI, 2BO *
DR TR33 17 · F2B · F10B
DGI E32 · DGI F32 · DGI E31 · DGI F31 · DGI E30 · DGI F30 · DGI E29 · DGI F29
SAI G28 · SAI G27 · ØR · CONV SA2 I14 → F25B 2TO → USEDI2
SAI G27 · ØR · CONV SA2 I14 → F24B 2TI → SRFLI2

DRFLI3 ← IXI, IXO *
DR TR33 17 · F3B · F11B
DGI F31 · DGI F30 · DGI E29 · DGI F29 · DGI E32 · DGI F32 · DGI E31
SAI G26 · SAI G25 · ØR · CONV SA2 I13 → F26B 2UI → USEDI3
SAI G25 · ØR · CONV SA2 I13 → F23B 2SO → SRFLI3

FROM PREVIOUS PAGE
WIXA3X ← PD T104 16 · F5A · F13A, F5B · F13B
WOXA2X ← PD T104 12 · F6A · F14A, F6B · F14B
ROX2XU ← F18A · SE STI H9, STI H11, STI H13
RIX3XU ← F18B · SE STI H10, STI H12, STI H14

257

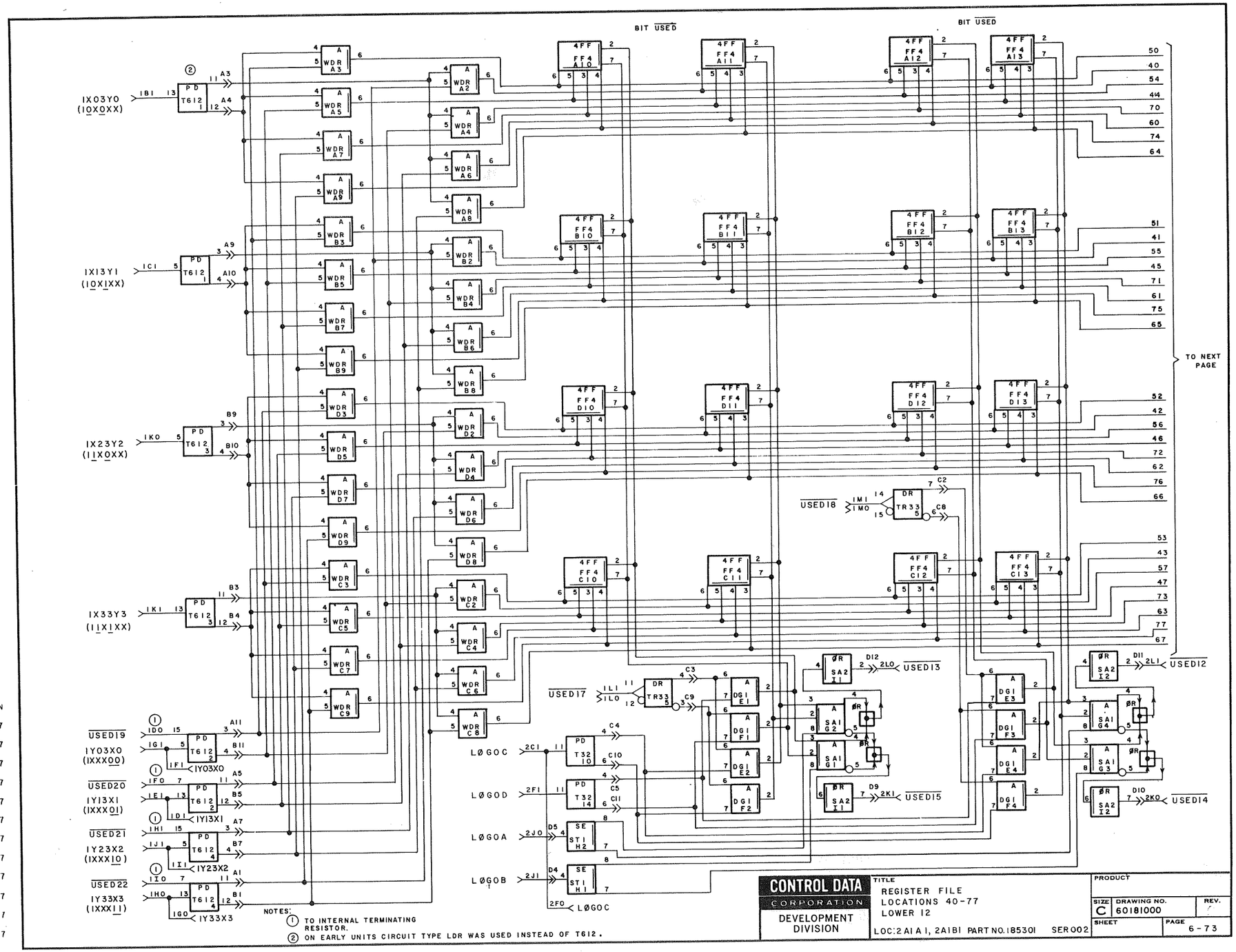
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE: REGISTER FILE
LOCATIONS 00-37
UPPER 12 AND 2 CONT
2A1A2
LOC: 2A1B2 PART NO. 185301 SER 001

PRODUCT

SIZE C | DRAWING NO. 60181000 | REV. A

SHEET | PAGE 6-71



PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1B1	2A1A0-F1	6-79	S BITS 01/00 = 0 TO RF 40-77
	2A1A4-E0	6-59	
1C1	2A1A0-E1	6-79	S BITS 01/00 = 1 TO RF 40-77
	2A1A4-H0	6-59	
1D1	2A1A4-L0	6-59	S BITS 04/02 = 1 TO RF 40-77
1E1	2A1A0-C1	6-79	S BITS 04/02 = 1 TO RF 40-77
1F1	2A1A0-H1	6-79	S BITS 04/02 = 0 TO RF 40-77
1G0	2A1A4-N0	6-59	S BITS 04/02 = 3 TO RF 40-77
1G1	2A1A4-F0	6-59	S BITS 04/02 = 0 TO RF 40-77
1H0	2A1A0-K1	6-79	S BITS 04/02 = 3 TO RF 40-77
1J1	2A1A4-K1	6-59	S BITS 04/02 = 2 TO RF 40-77
1J1	2A1A0-B0	6-79	S BITS 04/02 = 2 TO RF 40-77
1K0	2A1A0-J1	6-79	S BITS 01/00 = 2 TO RF 40-77
	2A1A4-F1	6-59	
1K1	2A1A0-H0	6-79	S BITS 01/00 = 3 TO RF 40-77
	2A1A4-J1	6-59	

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE REGISTER FILE LOCATIONS 40-77 LOWER 12 LOC:2A1A1, 2A1B1 PART NO.185301 SER002	PRODUCT	
		SIZE C	DRAWING NO. 60181000
		REV.	
		SHEET	PAGE 6-73

259

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1N0	2A1A6-D3	6- 49	
1N1	2A1A6-D2	6- 49	DIGIT DRIVE 10 TO RF 40-77
1U0	2A1A6-G3	6- 49	
1U1	2A1A6-G2	6- 49	DIGIT DRIVE 11 TO RF 40-77
1P0	2A1A6-H0	6- 49	
1P1	2A1A6-H1	6- 49	DIGIT DRIVE 09 TO RF 40-77
1W0	2A1A6-E1	6- 49	
1W1	2A1A6-E0	6- 49	DIGIT DRIVE 08 TO RF 40-77
1R0	2A1A5-G3	6- 47	
1R1	2A1A5-G2	6- 47	DIGIT DRIVE 07 TO RF 40-77
1S0	2A1A5-D3	6- 47	
1S1	2A1A5-D2	6- 47	DIGIT DRIVE 06 TO RF 40-77
2C0	2A1B0-D0	6- 81	WRITE RF 5X AND 7X 24 BITS
	2A1A4-W1	6- 59	
2U0	2A1B0-C0	6- 81	WRITE RF 4X AND 6X 24 BITS
2U1	2A1A4-V1	6- 59	WRITE RF 4X AND 6X 24 BITS
2G0	2A1B0-H0	6- 81	READ RF 5X AND 7X LOWER BITS
2G1	2A1A4-R0	6- 59	READ RF 5X AND 7X LOWER BITS
2HC	2A1B0-G0	6- 81	READ 4X AND 6X UPPER BITS
	2A104-Q0	6-59	
2H1	2A1B0-I0	6- 81	READ 5X AND 7X UPPER BITS
	2A104-S0	6-59	
2I0	2A1B0-H1	6- 81	READ RF 4X AND 6X LOWER BITS
2I1	2A1A4-P1	6- 59	READ RF 4X AND 6X LOWER BITS
2M0	2A1A5-S2	6- 47	SENSE RF 40-77 NOT(BIT 07)
2M1	2A1A6-T1	6- 49	SENSE RF 40-77 NOT(BIT 08)
2N1	2A1A5-T2	6- 47	SENSE RF 40-77 NOT(BIT 06)
2W0	2A1A6-S2	6- 49	SENSE RF 40-77 NOT(BIT 11)
2R0	2A1A6-T0	6- 49	SENSE RF 40-77 NOT(BIT 09)
2R1	2A1A6-T2	6- 49	SENSE RF 40-77 NOT(BIT 10)

BIT 11 | BIT 10 | BIT 09 | BIT 08 | BIT 07 | BIT 06

FROM PREVIOUS PAGE

50 40 54 44 70 60 74 64 51 41 55 45 71 61 75 65 52 42 56 46 72 62 76 66 53 43 57 47 73 63 77 67

4FF FF4 A14 | 4FF FF4 A15 | 4FF FF4 A16 | 4FF FF4 A17 | 4FF FF4 A18 | 4FF FF4 A19 | 4FF FF4 A20 | 4FF FF4 A21 | 4FF FF4 A22 | 4FF FF4 A23 | 4FF FF4 B24 | 4FF FF4 A25

4FF FF4 B14 | 4FF FF4 B15 | 4FF FF4 B16 | 4FF FF4 B17 | 4FF FF4 B18 | 4FF FF4 B19 | 4FF FF4 B20 | 4FF FF4 B21 | 4FF FF4 B22 | 4FF FF4 B23 | 4FF FF4 B24 | 4FF FF4 B25

4FF FF4 D14 | 4FF FF4 D15 | 4FF FF4 D16 | 4FF FF4 D17 | 4FF FF4 D18 | 4FF FF4 D19 | 4FF FF4 D20 | 4FF FF4 D21 | 4FF FF4 D22 | 4FF FF4 D23 | 4FF FF4 D24 | 4FF FF4 D25

4FF FF4 C14 | 4FF FF4 C15 | 4FF FF4 C16 | 4FF FF4 C17 | 4FF FF4 C18 | 4FF FF4 C19 | 4FF FF4 C20 | 4FF FF4 C21 | 4FF FF4 C22 | 4FF FF4 C23 | 4FF FF4 C24 | 4FF FF4 C25

TO NEXT PAGE

DRFUI0 ← 1NI 1NO — DR TR33 E11A — E3A — DGI E10 / DGI F10 / DGI E9 / DGI F9 / DGI E8 / DGI F8 / DGI E7 / DGI F7

USEDI6 ← 2EO — TERM TE2 18 (15)

LØGOC ← 2E1

DRFUI1 ← 1DI 1DO — DR TR33 E10A — E2A

SAI G7 / SAI G8 → ØR → CONV SA2 14 — E26A 2PO → USEDI0 ; E23A 2RI → SRFUI0

SAI G5 / SAI G6 → ØR → CONV SA2 15 — E25A 2QI → USEDI1 ; E24A 2QO → SRFUI1

DRFUI0 ← 1NI 1NO — DR TR33 E11A — E3A

DRFUI1 ← 1DI 1DO — DR TR33 E10A — E2A

DRFUI0 → 101 100 — DR TR33 E12B — E4B — DGI E14 / DGI F14 / DGI E13 / DGI F13 / DGI E12 / DGI F12 / DGI E11 / DGI F11

DRFUI1 → 1PI 1PO — DR TR33 E12A — E4A

SAI G11 / SAI G12 → ØR → CONV SA2 16 — E27B 2BO → USED08 ; E22B 2MI → SRFU08

SAI G9 / SAI G10 → ØR → CONV SA2 15 — E27A 2PI → USED09 ; E22A 2RO → SRFU09

DRFUI0 ← 1NI 1NO — DR TR33 E11A — E3A

DRFUI1 ← 1DI 1DO — DR TR33 E10A — E2A

DRFUI0 → 1SI 1SO — DR TR33 E10B — E2B — DGI E16 / DGI F18 / DGI E17 / DGI F17 / DGI E16 / DGI F16 / DGI E15 / DGI F15

DRFUI1 → 1RI 1RO — DR TR33 E11B — E3B

SAI G15 / SAI G16 → ØR → CONV SA2 18 — E25B 2NO → USED06 ; E24B 2NI → SRFU06

SAI G13 / SAI G14 → ØR → CONV SA2 17 — E25B 2QI → USED07 ; E23B 2MO → SRFU07

W4XA6X ← 2DI — PD T422 19 — 2DO

W5XA7X ← 2CO — PD T422 19

W4XA6X → PD T104 E13A / E13B

W5XA7X → PD T104 E14A / E14B

R5X7XU ← 2HI (1) — 2IO

R4X6XL ← 2II

PD T612 20 — E18B — SE STI H4 / SE STI H3

R4X6XU ← 2HO (1) — 2GO

R5X7XL ← 2GI

PD T612 20 — E18A — SE STI H6 / SE STI H5 / SE STI H8 / SE STI H7

W4XA6X TO T104
W5XA7X TO T104

TO NEXT PAGE

R4X6XL TO F18B
R5X7XL TO F18A

NOTE
(1) TO INTERNAL TERMINATING RESISTOR
(2) ON EARLY UNITS CIRCUIT TYPE LDR WAS USED INSTEAD OF T612.

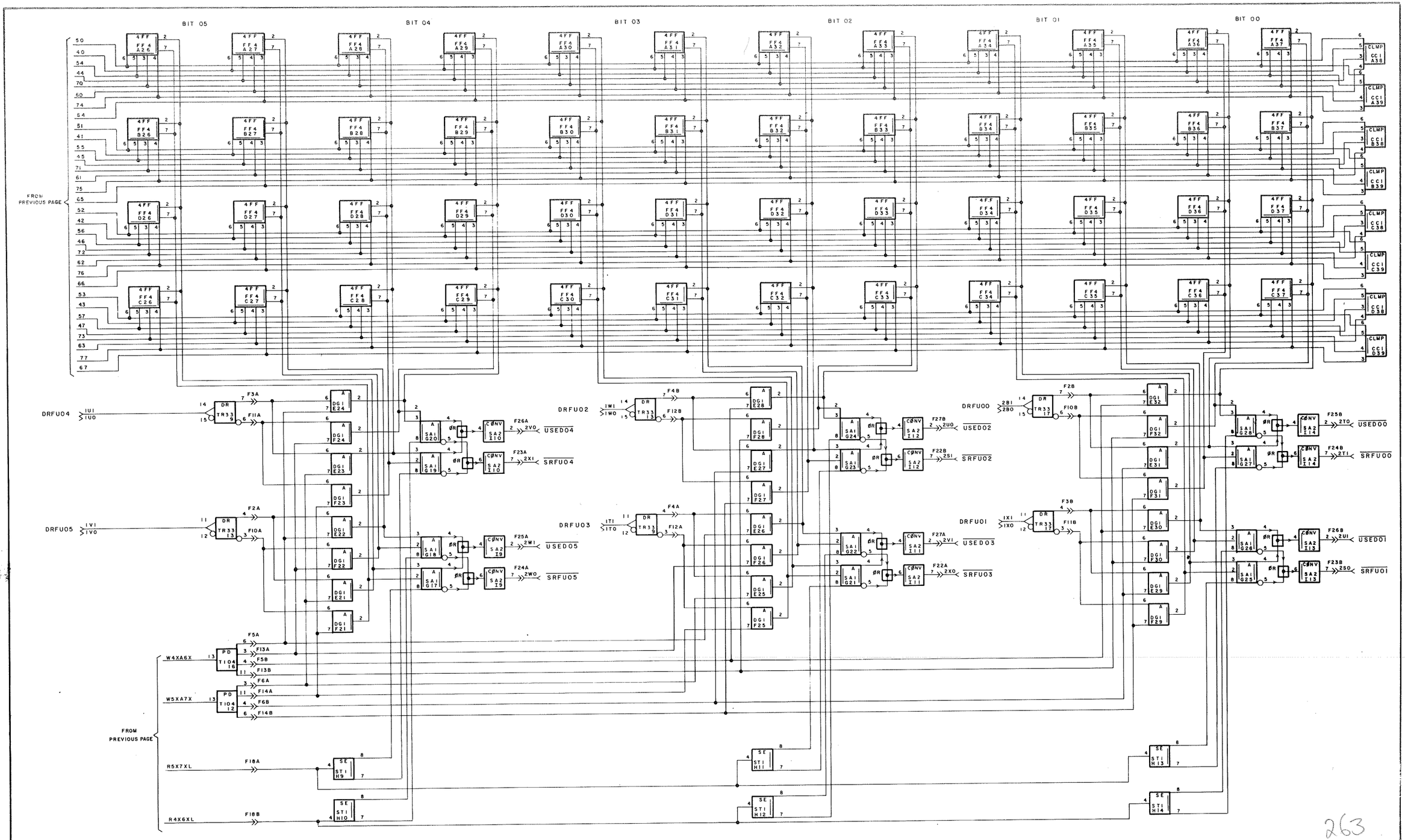
CONTROL DATA — DEVELOPMENT DIVISION

TITLE: REGISTER FILE LOCATIONS 40-77 LOWER 12
2A1A1
LOC: 2A1B1 PART NO. 185301 SER 002

SIZE C | DRAWING NO. 60181000 | REV.
SHEET | PAGE 6-75

261

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1J0	2A1H5-S3	6- 45	
1J1	2A1H5-S2	6- 45	DIGIT DRIVE 03 TO RF 40-77
1U0	2A1A5-H1	6- 47	
1U1	2A1A5-E0	6- 47	DIGIT DRIVE 04 TO RF 40-77
1V0	2A1A5-H0	6- 47	
1V1	2A1A5-H1	6- 47	DIGIT DRIVE 05 TO RF 40-77
1W0	2A1H5-Q2	6- 45	
1W1	2A1H5-Q3	6- 45	DIGIT DRIVE 02 TO RF 40-77
1X0	2A1B5-S1	6- 45	
1X1	2A1B5-S0	6- 45	DIGIT DRIVE 01 TO RF 40-77
2B0	2A1B5-Q1	6- 45	
2B1	2A1H5-Q0	6- 45	DIGIT DRIVE 00 TO RF 40-77
2J0	2A1H5-J1	6- 45	SENSE RF 40-77 NOT(BIT 01)
2J1	2A1B5-F2	6- 45	SENSE RF 40-77 NOT(BIT 02)
2L1	2A1B5-E1	6- 45	SENSE RF 40-77 NOT(BIT 00)
2W0	2A1A5-T0	6- 47	SENSE RF 40-77 NOT(BIT 05)
2X0	2A1H5-B2	6- 45	SENSE RF 40-77 NOT(BIT 03)
2X1	2A1A5-T1	6- 47	SENSE RF 40-77 NOT(BIT 04)



263

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE
REGISTER FILE
LOCATIONS 40-77
LOWER 12
2AIAI
LOC: 2AIBI PART NO 185301 SER 002

PRODUCT

SIZE C | DRAWING NO 6018[illegible] | REV A

SHEET | PAGE 6-77

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1B1	2A1A1-F1	6-73	S BITS 04/02 = 0 TO RF 40-77
	2A1A4-F0	6-59	
1C1	2A1A1-E1	6-73	S BITS 04/02 = 1 TO RF 40-77
	2A1A4-L0	6-59	
1D1	2A1A4-H0	6-59	S BITS 01/00 = 1 TO RF 40-77
1E1	2A1A1-C1	6-73	S BITS 01/00 = 1 TO RF 40-77
1F1	2A1A1-B1	6-73	S BITS 01/00 = 0 TO RF 40-77
1G0	2A1A4-J1	6-59	S BITS 01/00 = 3 TO RF 40-77
1G1	2A1A4-E0	6-59	S BITS 01/00 = 0 TO RF 40-77
1H0	2A1A1-K1	6-73	S BITS 01/00 = 3 TO RF 40-77
1J1	2A1A4-F1	6-59	S BITS 01/00 = 2 TO RF 40-77
1J1	2A1A1-K0	6-73	S BITS 01/00 = 2 TO RF 40-77
1K0	2A1A1-J1	6-73	S BITS 04/02 = 2 TO RF 40-77
	2A1A4-K1	6-59	
1K1	2A1A1-H0	6-73	S BITS 04/02 = 3 TO RF 40-77
	2A1A4-K0	6-59	

BIT $\overline{\text{USED}}$

BIT $\overline{\text{USED}}$

1Y03X0 (1OXOXX)

1Y13X1 (1OX1XX)

1Y23X2 (11XOXX)

1Y33X3 (11X1XX)

$\overline{\text{USED03}}$ 1X03Y0 (1XXX00)

$\overline{\text{USED04}}$ 1X13Y1 (1XXX01)

$\overline{\text{USED05}}$ 1X23Y2 (1XXX10)

$\overline{\text{USED06}}$ 1X33Y3 (1XXX11)

$\overline{\text{USED01}}$

$\overline{\text{USED02}}$

LØGOC

LØGOD

LØGOA

LØGOB

$\overline{\text{USED25}}$

$\overline{\text{USED24}}$

$\overline{\text{USED27}}$

$\overline{\text{USED26}}$

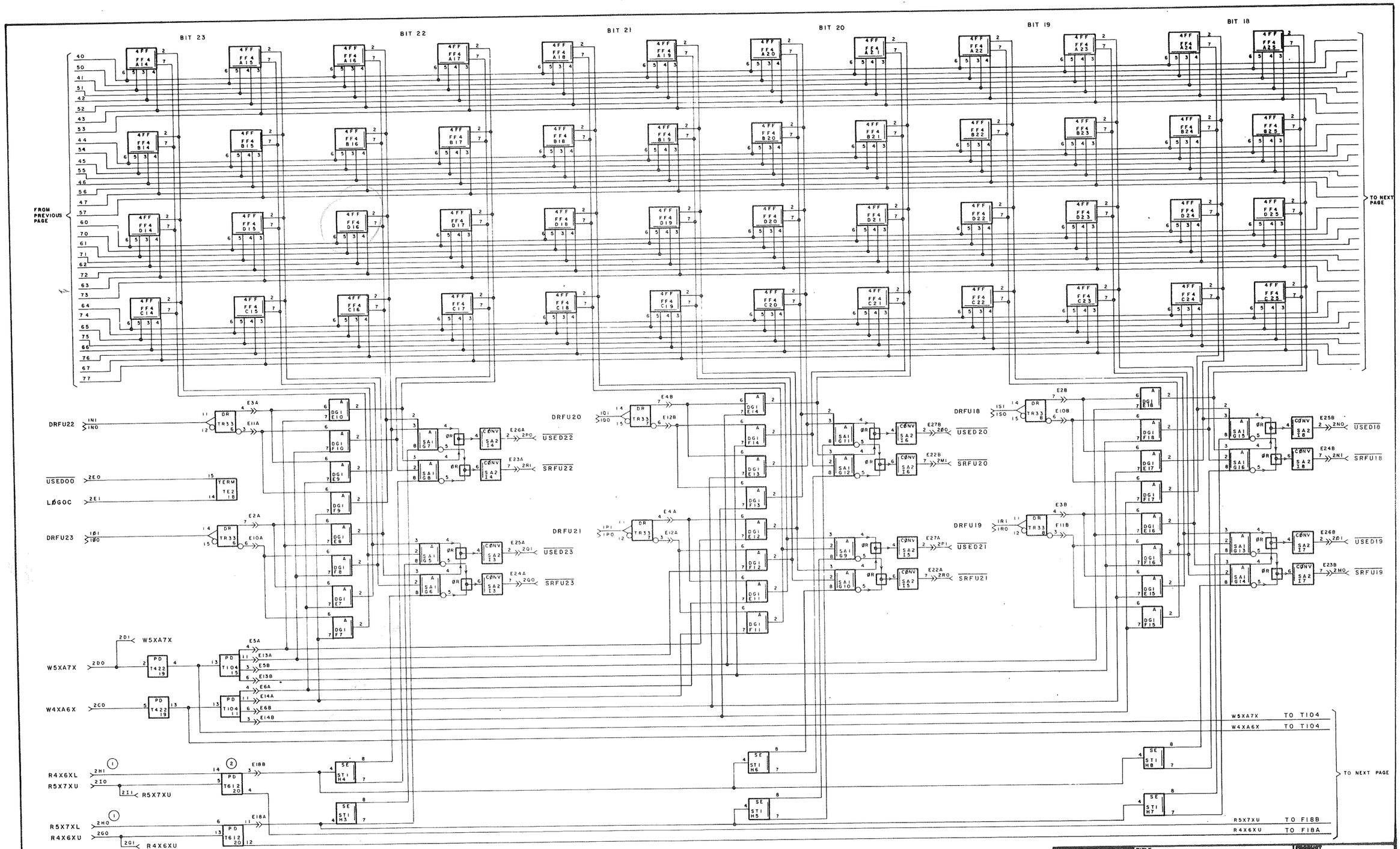
TO NEXT PAGE

NOTES:
1. TO INTERNAL TERMINATING RESISTOR.
2. ON EARLY UNITS CIRCUIT TYPE LDR WAS USED INSTEAD OF T612.

CONTROL DATA CORPORATION	TITLE: REGISTER FILE LOCATIONS 40-77 UPPER 12	PRODUCT	
DEVELOPMENT DIVISION	LOC: 2A1A0, 2A1B0 PART NO. 185301 SER003	SIZE C / DRAWING NO. 60181000 / REV.	
		SHEET	PAGE 6-79

265

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1N0	2A1A8-P3	6- 55	
1N1	2A1A8-P2	6- 55	DIGIT DRIVE 22 TO RF 40-77
1U0	2A1A8-L3	6- 55	
1U1	2A1A8-L2	6- 55	DIGIT DRIVE 23 TO RF 40-77
1P0	2A1A8-I3	6- 55	
1P1	2A1A8-I2	6- 55	DIGIT DRIVE 21 TO RF 40-77
1W0	2A1A8-G3	6- 55	
1W1	2A1A8-G2	6- 55	DIGIT DRIVE 20 TO RF 40-77
1K0	2A1A7-C1	6- 41	
1K1	2A1A7-C0	6- 41	DIGIT DRIVE 19 TO RF 40-77
1S0	2A1A7-G3	6- 41	
1S1	2A1A7-G2	6- 41	DIGIT DRIVE 18 TO RF 40-77
2C0	2A1A1-D0	6- 75	WRITE RF 4X AND 6X 24 BITS
	2A1A4-V1	6- 59	
2U0	2A1A1-C0	6- 75	WRITE RF 5X AND 7X 24 BITS
2U1	2A1A4-W1	6- 59	WRITE RF 5X AND 7X 24 BITS
2G0	2A1A1-H0	6- 75	READ RF 4X AND 6X UPPER BITS
2G1	2A1A4-D0	6- 59	READ RF 4X AND 6X UPPER BITS
2H0	2A1B1-G0	6-75	READ RF 5X AND 7X LOWER BITS
	2A1A4-R0		
2H1	2A1B1-I0	6-75	READ RF 5X AND 7X UPPER BITS
	2A1A4-P1	6-59	
2L0	2A1A1-H1	6- 75	READ RF 5X AND 7X UPPER BITS
2L1	2A1A4-S0	6- 59	READ RF 5X AND 7X UPPER BITS
2M0	2A1A8-D2	6- 53	SENSE RF 40-77 NOT(BIT 19)
2M1	2A1A8-B1	6- 55	SENSE RF 40-77 NOT(BIT 20)
2N1	2A1A8-A0	6- 53	SENSE RF 40-77 NOT(BIT 18)
2W0	2A1A8-N0	6- 55	SENSE RF 40-77 NOT(BIT 23)
2K0	2A1A8-D1	6- 55	SENSE RF 40-77 NOT(BIT 21)
2K1	2A1A8-M0	6- 55	SENSE RF 40-77 NOT(BIT 22)



NOTE

(1) TO INTERNAL TERMINATING RESISTOR

(2) ON EARLY UNITS CIRCUIT TYPE LDR WAS USED INSTEAD OF T612.

CONTROL DATA
DEVELOPMENT DIVISION

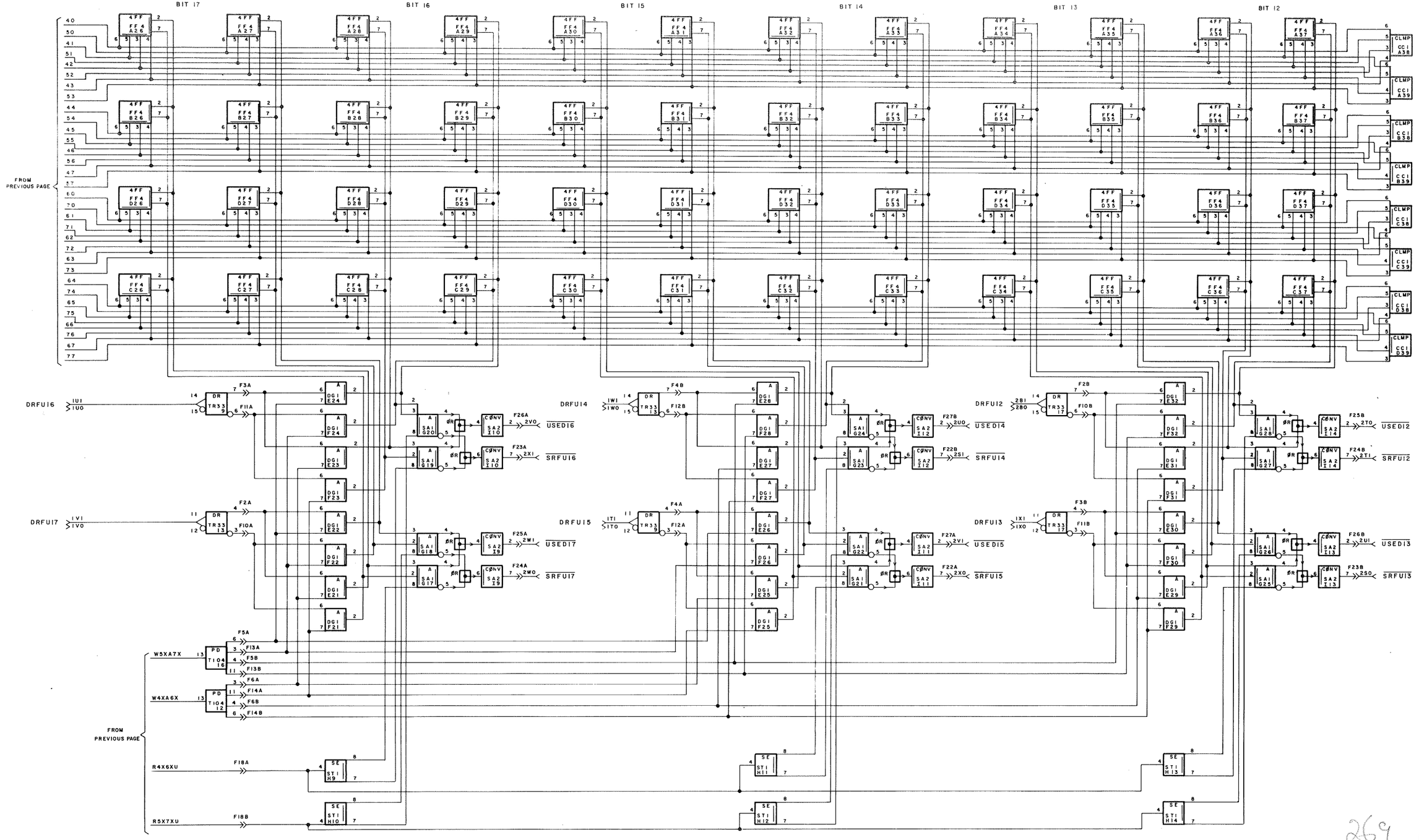
TITLE
REGISTER FILE
LOCATIONS 40-77
UPPER 12
2A1A0
LOC:2A1B0 PART NO. 185301 SER.003

PRODUCT

SIZE	DRAWING NO.	REV.
C	60181000	G
SHEET	PAGE	
	6-81	

267

PIN	ORIGIN/ DEST.	PAGE	SIGNAL DEFINITION
1 l0	2A1A7-G3	6- 51	
1 l1	2A1A7-G2	6- 51	DIGIT DRIVE 15 TO RF 40-77
1 u0	2A1A8-S0	6- 53	
1 u1	2A1A8-S1	6- 53	DIGIT DRIVE 16 TO RF 40-77
1 v0	2A1A7-H2	6- 41	
1 v1	2A1A7-H3	6- 41	DIGIT DRIVE 17 TO RF 40-77
1 w0	2A1A7-D3	6- 51	
1 w1	2A1A7-D2	6- 51	DIGIT DRIVE 14 TO RF 40-77
1 x0	2A1A7-H0	6- 51	
1 x1	2A1A7-H1	6- 51	DIGIT DRIVE 13 TO RF 40-77
2 s0	2A1A7-E1	6- 51	
2 s1	2A1A7-E0	6- 51	DIGIT DRIVE 12 TO RE 40-77
2 t0	2A1A7-T0	6- 51	SENSE RF 40-77 NOT(BIT 13)
2 t1	2A1A7-T2	6- 51	SENSE RF 40-77 NOT(BIT 14)
2 l1	2A1A7-T1	6- 51	SENSE RF 40-77 NOT(BIT 12)
2 u0	2A1A8-I1	6- 53	SENSE RF 40-77 NOT(BIT 17)
2 x0	2A1A7-S2	6- 51	SENSE RF 40-77 NOT(BIT 15)
2 x1	2A1A8-I0	6- 53	SENSE RF 40-77 NOT(BIT 16)



269

CONTROL DATA
DEVELOPMENT DIVISION

TITLE
REGISTER FILE
LOCATIONS 40-77
UPPER 12
2AIA0
LOC: 2AIB0

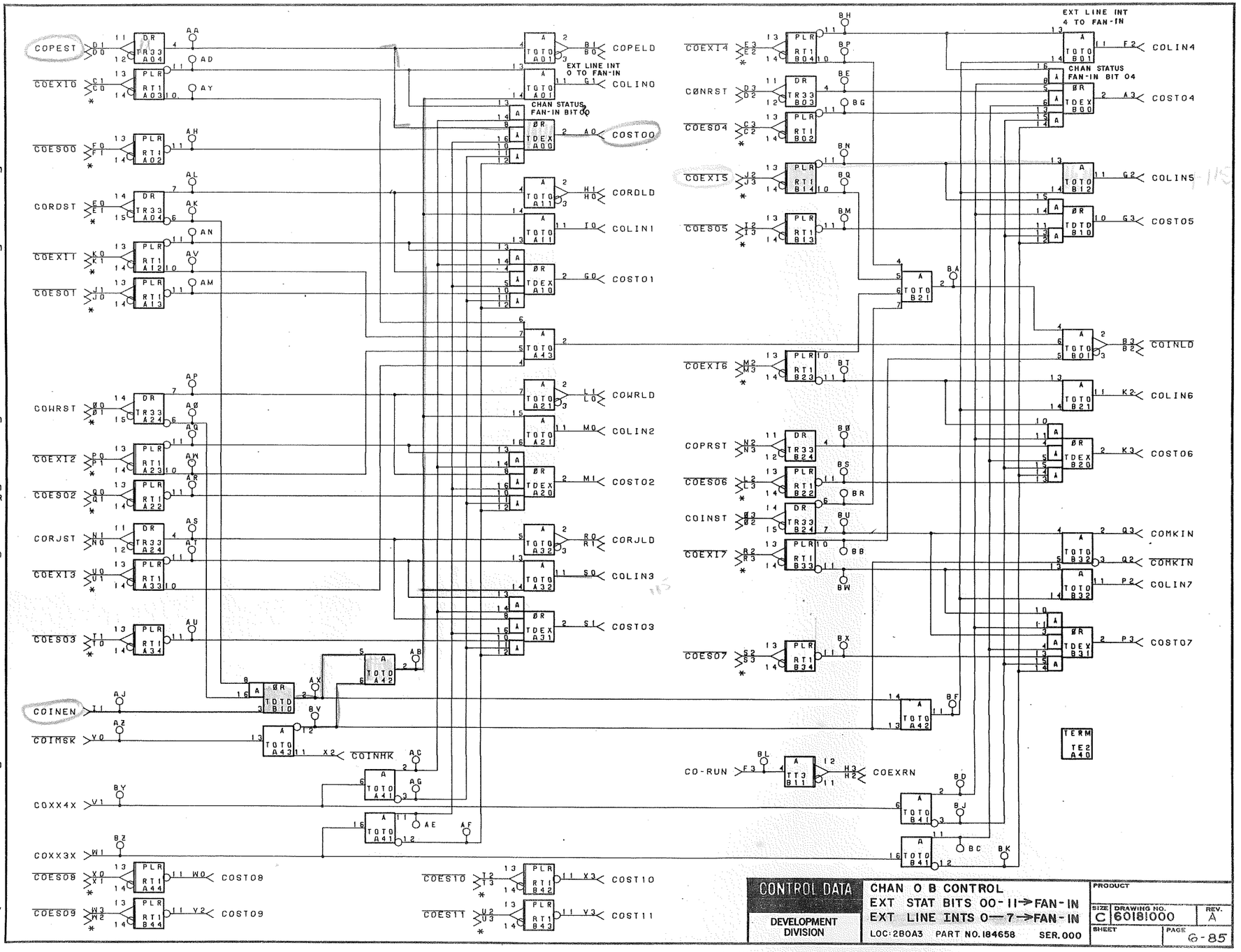
PRODUCT

SIZE C | DRAWING NO 60181000 | REV. A

SHEET | PAGE 6-83

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2R0A6-C3	6-121		CHL 0 STATUS FAN IN BIT 00
A3	2R0A6-D3	6-121		CHL 0 STATUS FAN IN BIT 04
B0	2R2R3-H2	5- 87		
B1	2R2R3-H3	5- 87		CHAN 0 PARITY ERROR LIGHT
B2	2R2R3-T1	5- 87		NOT CHAN 0 INT LIGHT DRIVER
B3	2R2R3-T0	5- 87		
C0	2A4A05J03D-01			CHL 0 EXT. LINE INTERRUPT 5
	2A4A05J04D-01			
C1	2A4A05J03D-02			
	2A4A05J04D-02			
C2	2A4A05J03A-09			CHL 0 EXTERNAL STATUS BIT 04
	2A4A05J04A-09			
C3	2A4A05J03A-10			
	2A4A05J04A-10			
D0	2A0B7-L2	6-125		
D1	2A0B7-L3	6-125		CHAN 0 PE STATUS + FAN-IN
D2	2A0B7-J2	6-125		
D3	2A0B7-J3	6-125		CHAN 0 NO RESPONSE STATUS TO FAN-IN
E0	2A0B7-V0	6-125		NOT CHAN 0 READ STAT TO FAN-IN
E1	2A0B7-V1	6-125		
E2	2A4A05J03D-09			CHL 0 EXT. LINE INTERRUPT 4
	2A4A05J04D-09			
E3	2A4A05J03D-10			
	2A4A05J04D-10			
F0	2A4A05J03A-02			
	2A4A05J04A-02			
F1	2A4A05J03A-01			CHL 0 EXTERNAL STATUS BIT 00
	2A4A05J04A-01			
F2	2R0B7-C0	6-113	2B0B7-A0	CHL 0 LINE INTERRUPT 4 - C=040
F3	2R0A4-H0	6-103	2B0A3-RL	CHAN 0 CMPTR RUNNING TO XMTR
G0	2R0A5-C3	6-123		CHL 0 STATUS FAN IN BIT 01
G1	2R0B7-A0	6-113	2B0B7-AA	CHL 0 LINE INTERRUPT 0 - C=000
G2	2R0B6-C0	6-115	2B0B6-A0	CHL 0 LINE INTERRUPT 5 - C=050
G3	2R0A5-Q3	6-123		CHAN 0 STAT FAN-IN - BIT 5
H0	2R2B2-H0	5- 89		
H1	2R2B2-H1	5- 89		CHAN 0 READ INDICATOR DRIVER
H2	2A4A05J03C-06			
	2A4A05J04C-06			
H3	2A4A05J03C-05			CHAN 0 EXTERNAL CMPTR RUNNING
	2A4A05J04C-05			
I0	2B0B6-A0	6-115	2B0B6-AA	CHL 0 LINE INTERRUPT 1 - C=010

I1	2R0A4-A0	6-103	2B0A3-AJ	CHL 0 INTERRUPT ENABLE
I2	2A4A05J03R-02			
	2A4A05J04R-02			
I3	2A4A05J03R-01			CHL 0 EXTERNAL STATUS BIT 05
	2A4A05J04R-01			
J0	2A4A05J03A-03			CHL 0 EXTERNAL STATUS BIT 01
	2A4A05J04A-03			
J1	2A4A05J03A-04			
	2A4A05J04A-04			
J2	2A4A05J03E-02			
	2A4A05J04E-02			
J3	2A4A05J03E-01			CHL 0 EXT, LINE INTERRUPT 5
	2A4A05J04E-01			
K0	2A4A05J03D-04			
	2A4A05J04D-04			
K1	2A4A05J03D-03			CHL 0 EXT, LINE INTERRUPT 1
	2A4A05J04D-03			
K2	2B0B7-D1	6-113	2B0B7-AS	CHL 0 LINE INTERRUPT 6 - C=060
K3	2B0A6-D1	6-121		CHL 0 STATUS FAN IN BIT 06
L0	2R2B2-N2	5- 89		
L1	2R2B2-N3	5- 89		CHAN 0 WRITE INDICATOR DRIVER
L2	2A4A05J03R-04			
	2A4A05J04B-04			
L3	2A4A05J03R-03			CHL 0 EXTERNAL STATUS BIT 06
	2A4A05J04R-03			
M0	2B0B7-B0	6-113	2B0B7-AK	CHL 0 LINE INTERRUPT 2 - C=020
M1	2R0A6-K3	6-121		CHL 0 STATUS FAN IN BIT 02
M2	2A4A05J03E-04			
	2A4A05J04E-04			
M3	2A4A05J03E-03			CHL 0 EXT, LINE INTERRUPT 6
	2A4A05J04F-03			
N0	2A0B7-C3	6-125		
N1	2A0B7-C2	6-125		CHAN 0 EXT REJ STAT TO FAN-IN
N2	2A0B7-G3	6-125		CHL 0 PRESET STATUS TO FAN IN
N3	2A0B7-G2	6-125		
O0	2A0B7-W1	6-125		NOT CHAN 0 WRITE STAT TO FI
O1	2A0B7-W0	6-125		
O2	2A0B7-T2	6-125		
O3	2A0B7-T3	6-125		CHAN 0 INT TO STATUS FAN-IN
P0	2A4A05J03D-06			
	2A4A05J04D-06			
P1	2A4A05J03D-05			CHL 0 EXT, LINE INTERRUPT 2
	2A4A05J04D-05			
P2	2B0B6-D1	6-115	2B0B6-AS	CHL 0 LINE INTERRUPT 7 - C=070
P3	2R0A5-D1	6-123		CHL 0 STATUS FAN IN BIT 07
Q0	2A4A05J03A-06			
	2A4A05J04A-06			
Q1	2A4A05J03A-05			CHL 0 EXTERNAL STATUS BIT 02
	2A4A05J04A-05			
Q2	2B0A8-Q2	6-109		NOT(CHL 0 MASKED INTERRUPT)
Q3	2B0B8-K0	6-111		CHL 0 MASKED INTERRUPT = C=100
R0	2R2B3-D1	5- 87		CHAN 0 REJECT INDICATOR DRIVER
R1	2R2B3-D0	5- 87		
R2	2A4A05J03E-06			
	2A4A05J04E-06			
R3	2A4A05J03E-05			CHL 0 EXT, LINF INTERRUPT 7
	2A4A05J04E-05			
S0	2B0B6-B0	6-115	2B0B6-AK	CHL 0 LINE INTERRUPT 3 - C=030
S1	2B0A5-K3	6-123		CHL 0 STATUS FAN IN BIT 03
S2	2A4A05J03B-06			
	2A4A05J04B-06			
S3	2A4A05J03B-05			CHL 0 EXTERNAL STATUS BIT 07
	2A4A05J04B-05			
T0	2A4A05J03A-07			CHL 0 EXTERNAL STATUS BIT 03
	2A4A05J04A-07			
T1	2A4A05J03A-08			
	2A4A05J04A-08			
T2	2A4A05J03C-02			
	2A4A05J04C-02			
T3	2A4A05J03C-01			CHL 0 EXTERNAL STATUS BIT 10
	2A4A05J04C-01			
U0	2A4A05J03D-08			
	2A4A05J04D-08			
U1	2A4A05J03D-07			CHL 0 EXT, LINE INTERRUPT 3
	2A4A05J04D-07			
U2	2A4A05J03C-04			
	2A4A05J04C-04			
U3	2A4A05J03C-03			CHL 0 EXTERNAL STATUS BIT 11
	2A4A05J04C-03			
V0	2R0A4-N0	6-103	2B0A3-AZ	NOT (CHAN 0 INTERRUPT MASK) TO FANOUT
V1	2R0A9-A3	6-101	2B0A3-RY	CHL 0 SELECT EXT INTERRUPT
V2	2R0A5-M0	6-123	2B0A5-RX	CHL 0 EXTERNAL STATUS BIT 09
V3	2R0A5-G1	6-123	2B0A5-AA	CHL 0 EXTERNAL STATUS BIT 11
W0	2R0A6-G1	6-121	2B0A6-AA	CHL 0 EXTERNAL STATUS BIT 08
W1	2R0A9-C3	6-101	2B0A3-RZ	CHL 0 SELECT INTERNAL STATUS
W2	2A4A05J03R-09			CHL 0 EXTERNAL STATUS BIT 09
	2A4A05J04R-09			
W3	2A4A05J03R-10			
	2A4A05J04R-10			
X0	2A4A05J03R-08			
	2A4A05J04R-08			
X1	2A4A05J03R-07			CHL 0 EXTERNAL STATUS BIT 08
	2A4A05J04R-07			
X2	2R0B7-F1	6-113		NOT(CHL 0 INTERRUPT MASK) COPY
X3	2R0A6-M0	6-121	2B0A6-PX	CHL 0 EXTERNAL STATUS BIT 10

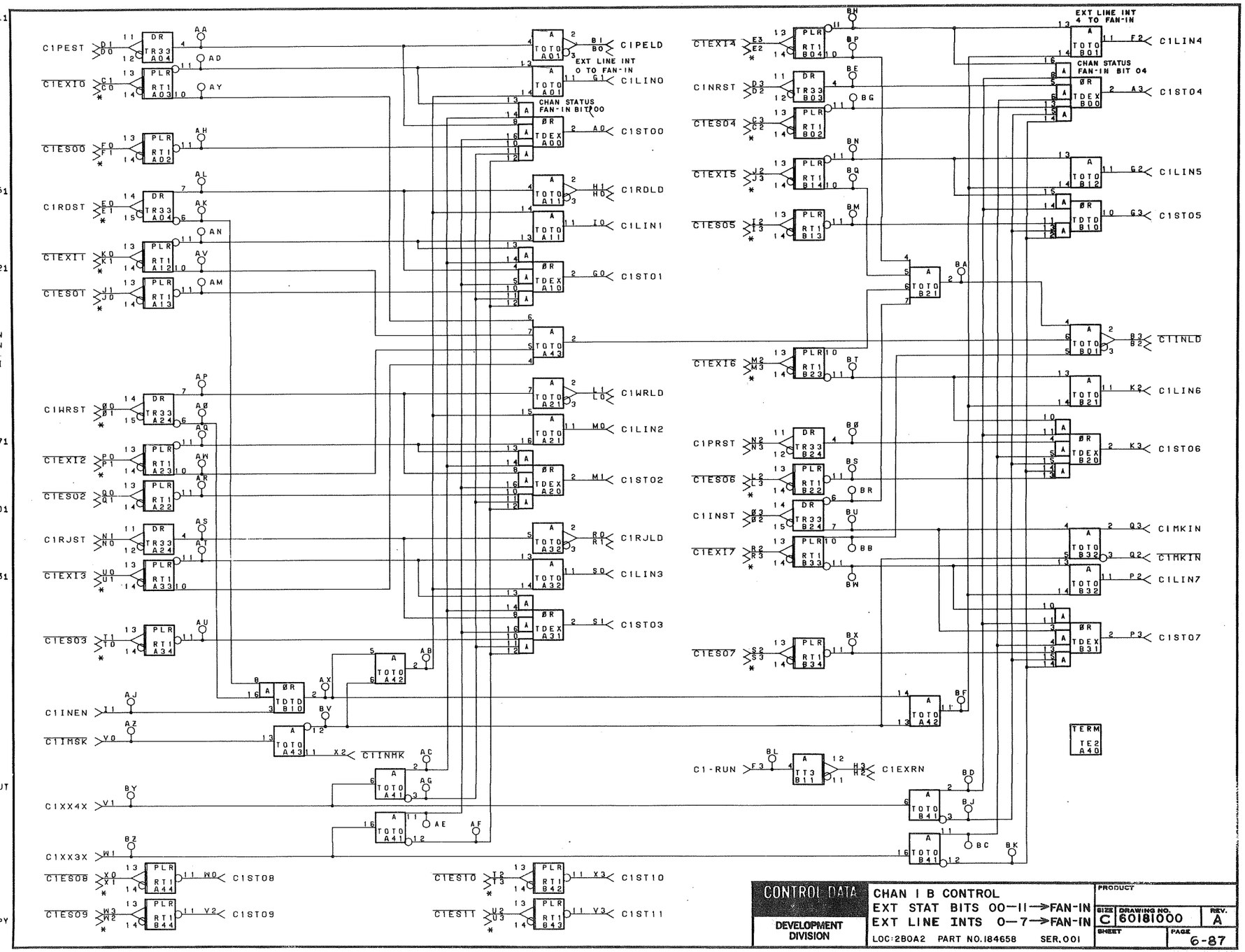


CONTROL DATA	CHAN 0 B CONTROL	PRODUCT	
	EXT STAT BITS 00-11→FAN-IN	SIZE C	DRAWING NO. 60181000 REV. A
DEVELOPMENT DIVISION	EXT LINE INTS 0—7→FAN-IN	SHEET	PAGE 6-85
	LOC: 2B0A3 PART NO. 184658 SER. 000		

271

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B0A6-A3	6-121		CHL 1 STATUS FAN IN BIT 00
A3	2B0A6-P3	6-121		CHL 1 STATUS FAN IN BIT 04
B0	2B2R3-I2	5- 87		
B1	2B2R3-I3	5- 87		CHAN 1 PARITY ERR, LT DRIVER
B2	2B2B3-S1	5- 87		NOT CHAN 1 INT LIGHT DRIVER
B3	2B2R3-S0	5- 87		
C0	2A4A05J01D-01 2A4A05J02D-01			CHL 1 EXT. LINE INTERRUPT 0
C1	2A4A05J01D-02 2A4A05J02D-02			
C2	2A4A05J01A-09 2A4A05J02A-09			CHL 1 EXTERNAL STATUS BIT 04
C3	2A4A05J01A-10 2A4A05J02A-10			
D0	2A0B6-L2	6-127		
D1	2A0B6-L3	6-127		CHAN 1 PE STATUS + FAN-IN
D2	2A0B6-J2	6-127		
D3	2A0B6-J3	6-127		CHAN 1 NO RESPONSE STATUS TO FAN-IN
E0	2A0B6-V0	6-127		NOT CHAN 1 READ STATUS TO FI
E1	2A0B6-V1	6-127		
E2	2A4A05J01D-09 2A4A05J02D-09			CHL 1 EXT. LINE INTERRUPT 4
E3	2A4A05J01D-10 2A4A05J02D-10			
F0	2A4A05J01A-02 2A4A05J02A-02			
F1	2A4A05J01A-01 2A4A05J02A-01			CHL 1 EXTERNAL STATUS BIT 00
F2	2B0B7-J1	6-113	2B0B7-AP	CHAN 1 LINE INT 4 + C=041
F3	2B0A4-I1	6-103	2B0A2-RL	CHAN 1 CMPTR RUNNING TO XMTR
G0	2B0A5-A3	6-123		CHL 1 STATUS FAN IN BIT 01
G1	2B0B7-E0	6-113	2B0B7-AB	CHL 1 LINE INTERRUPT 0 - C=001
G2	2B0B6-J1	6-115	2B0B6-AP	CHL 1 LINE INTERRUPT 5 - C=051
G3	2B0A5-P3	6-123		CHAN 1 STATUS FAN-IN - BIT 05
H0	2B2B2-C2	5- 89		
H1	2B2B2-C3	5- 89		CHL 1 READ LIGHT DRIVER
H2	2A4A05J01C-06 2A4A05J02C-06			
H3	2A4A05J01C-05 2A4A05J02C-05			CHAN 1 EXT COMPUTER RUNNING

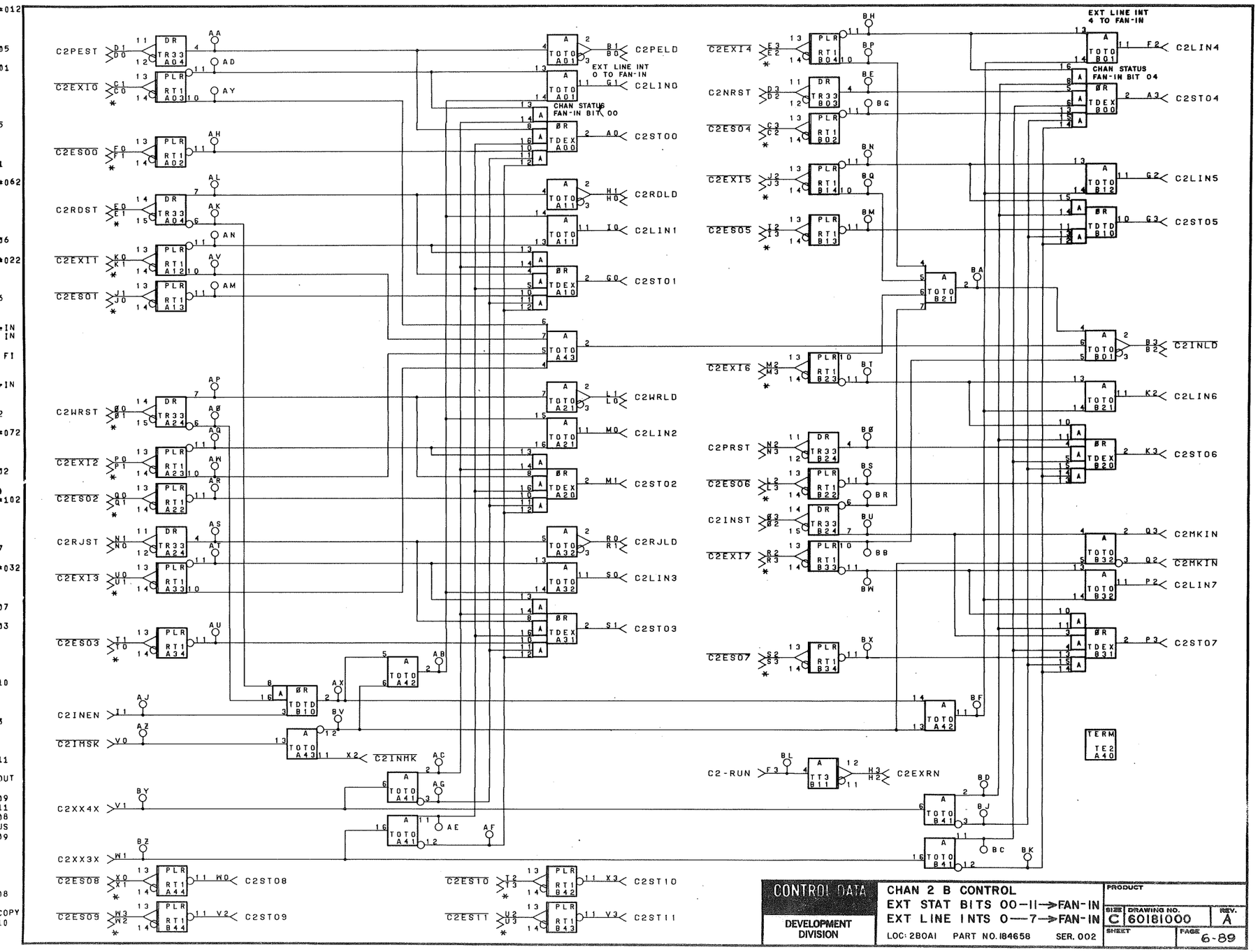
I0	2B0B6-E0	6-115	2B0B6-AB	CHL 1 LINE INTERRUPT 1 - C=011
I1	2B0A4-X0	6-103	2B0A2-AJ	CHL 1 INTERRUPT ENABLE
I2	2A4A05J01B-02			
	2A4A05J02B-02			
I3	2A4A05J01A-01			CHL 1 EXTERNAL STATUS BIT 05
	2A4A05J02A-01			
J0	2A4A05J01A-03			CHL 1 EXTERNAL STATUS BIT 01
	2A4A05J02A-03			
J1	2A4A05J01A-04			
	2A4A05J02A-04			
J2	2A4A05J01E-02			
	2A4A05J02E-02			
J3	2A4A05J01E-01			CHL 1 EXT, LINF INTERRUPT 5
	2A4A05J02E-01			
K0	2A4A05J01D-04			
	2A4A05J02D-04			
K1	2A4A05J01D-03			CHL 1 EXT, LINE INTERRUPT 1
	2A4A05J02D-03			
K2	2B0B7-K0	6-113	2B0B7-AV	CHL 1 LINE INTERRUPT 6 - C=061
K3	2B0A6-D0	6-121		CHL 1 STATUS FAN IN BIT 06
L0	2B2B2-03	5- 89		
L1	2B2B2-02	5- 89		CHL 1 WRITE LIGHT DRIVER
L2	2A4A05J01B-04			
	2A4A05J02B-04			
L3	2A4A05J01B-03			CHL 1 EXTERNAL STATUS BIT 06
	2A4A05J02B-03			
M0	2B0B7-D0	6-113	2B0B7-AH	CHL 1 LINE INTERRUPT 2 - C=021
M1	2B0A6-K2	6-121		CHL 1 STATUS FAN IN BIT 02
M2	2A4A05J01E-04			
	2A4A05J02E-04			
M3	2A4A05J01E-03			CHL 1 EXT, LINE INTERRUPT 6
	2A4A05J02E-03			
N0	2A0B6-C3	6-127		
N1	2A0B6-C2	6-127		CHAN 1 EXT REJ STAT TO FAN-IN
N2	2A0B6-G3	6-127		CHL 1 PRESET STATUS TO FAN IN
N3	2A0B6-G2	6-127		
O0	2A0B6-W1	6-127		NOT CHAN 1 WRITE STATUS TO FI
O1	2A0B6-W0	6-127		
O2	2A0B6-T2	6-127		
O3	2A0B6-T3	6-127		CHAN 1 INT TO STATUS FAN-IN
P0	2A4A05J01D-06			
	2A4A05J02D-06			
P1	2A4A05J01D-05			CHL 1 EXT, LINE INTERRUPT 2
	2A4A05J02D-05			
P2	2B0B6-K0	6-115	2B0B6-AV	CHL 1 LINE INTERRUPT 7 - C=071
P3	2B0A5-D0	6-123		CHL 1 STATUS FAN IN BIT 07
Q0	2A4A05J01A-06			
	2A4A05J02A-06			
Q1	2A4A05J01A-05			CHL 1 EXTERNAL STATUS BIT 02
	2A4A05J02A-05			
Q2	2B0A8-Q3	6-109		NOT(CHL 1 MASKED INTERRUPT)
Q3	2B0B8-K1	6-111		CHL 1 MASKED INTERRUPT - C=101
R0	2B2B3-C1	5- 87		CHL 1 REJECT LIGHT DRIVER
R1	2B2B3-C0	5- 87		
R2	2A4A05J01E-06			
	2A4A05J02E-06			
R3	2A4A05J01E-05			CHL 1 EXT, LINE INTERRUPT 7
	2A4A05J02E-05			
S0	2B0B6-D0	6-115	2B0B6-AH	CHL 1 LINE INTERRUPT 3 - C=031
S1	2B0A5-K2	6-123		CHL 1 STATUS FAN IN BIT 03
S2	2A4A05J01B-06			
	2A4A05J02B-06			
S3	2A4A05J01B-05			CHL 1 EXTERNAL STATUS BIT 07
	2A4A05J02B-05			
T0	2A4A05J01A-07			CHL 1 EXTERNAL STATUS BIT 03
	2A4A05J02A-07			
T1	2A4A05J01A-08			
	2A4A05J02A-08			
T2	2A4A05J01C-02			
	2A4A05J02C-02			
T3	2A4A05J01C-01			CHL 1 EXTERNAL STATUS BIT 10
	2A4A05J02C-01			
U0	2A4A05J01D-08			
	2A4A05J02D-08			
U1	2A4A05J01D-07			CHL 1 EXT, LINE INTERRUPT 3
	2A4A05J02D-07			
U2	2A4A05J01C-04			
	2A4A05J02C-04			
U3	2A4A05J01C-03			CHL 1 EXTERNAL STATUS BIT 11
	2A4A05J02C-03			
V0	2B0A4-L0	6-103	2B0A2-AZ	NOT(CHAN 1 INT MASK) TO FANOUT
V1	2B0A9-B2	6-101	2B0A2-RY	CHL 1 SELECT EXT INTERRUPT
V2	2B0A5-T0	6-123	2B0A5-AX	CHL 1 EXTERNAL STATUS BIT 09
V3	2B0A5-K0	6-123	2B0A5-AF	CHL 1 EXTERNAL STATUS BIT 11
W0	2B0A6-K0	6-121	2B0A6-AF	CHL 1 EXTERNAL STATUS BIT 08
W1	2B0A9-D2	6-101	2B0A2-RZ	CHL 1 SELECT INTERNAL STATUS
W2	2A4A05J01B-09			CHL 1 EXTERNAL STATUS BIT 09
	2A4A05J02B-09			
W3	2A4A05J01B-10			
	2A4A05J02B-10			
X0	2A4A05J01B-08			
	2A4A05J02B-08			
X1	2A4A05J01B-07			CHL 1 EXTERNAL STATUS BIT 08
	2A4A05J02B-07			
X2	2B0B7-J0	6-113		NOT(CHL 1 INTERRUPT MASK) COPY
X3	2B0A6-T0	6-121	2B0A6-AX	CHL 1 EXTERNAL STATUS BIT 10



CONTROL DATA	CHAN I B CONTROL	PRODUCT	
DEVELOPMENT DIVISION	EXT STAT BITS 00—11→FAN-IN	SIZE C	DRAWING NO. 60181000 REV. A
	EXT LINE INTS 0—7→FAN-IN	SHEET	PAGE 6-87
	LOC:2B0A2 PART NO.184658 SER.001		

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B0A6-C2	6-121		CHL 2 STATUS FAN IN BIT 00
A3	2B0A6-D3	6-121		CHL 2 STATUS FAN IN BIT 04
B0	2B2B3-J3	5- 87		
B1	2B2B3-J2	5- 87		CHAN 2 PARITY ERR, LT DRIVER
B2	2B2B3-R1	5- 87		NOT CHAN 2 INT LIGHT DRIVER
B3	2B2B3-R0	5- 87		
C0	2A4A06J03D-01			CHL 2 EXT, LINE INTERRUPT 0
	2A4A06J04D-01			
C1	2A4A06J03D-02			
	2A4A06J04D-02			
C2	2A4A06J03A-09			CHL 2 EXTERNAL STATUS BIT 04
	2A4A06J04A-09			
C3	2A4A06J03A-10			
	2A4A06J04A-10			
D0	2A0B3-L2	6-129		
D1	2A0B3-L3	6-129		CHAN 2 PE STATUS + FAN-IN
D2	2A0B3-J2	6-129		
D3	2A0B3-J3	6-129		CHAN 2 NO RESPONSE STATUS TO FAN-IN
E0	2A0B3-V0	6-129		NOT CHAN 2 READ STATUS TO FI
E1	2A0B3-V1	6-129		
E2	2A4A06J03D-09			CHL 2 EXT, LINE INTERRUPT 4
	2A4A06J04D-09			
E3	2A4A06J03D-10			
	2A4A06J04D-10			
F0	2A4A06J03A-02			
	2A4A06J04A-02			
F1	2A4A06J03A-01			CHL 2 EXTERNAL STATUS BIT 00
	2A4A06J04A-01			
F2	2B0B7-P1	6-113	2B0B7-AN	CHL 2 LINE INTERRUPT 4 + C=042
F3	2B0B4-H0	6-105	2B0A1-RL	CHAN 2 CMPTR RUNNING TO XMTR
G0	2B0A5-C2	6-123		CHL 2 STATUS FAN IN BIT 01
G1	2B0B7-L0	6-113	2B0B7-AE	CHL 2 LINE INTERRUPT 0 + C=002
G2	2B0B6-P1	6-115	2B0B6-AN	CHAN 2 LINE INT 5 + C=052
G3	2B0A5-03	6-123		CHAN 2 STATUS FAN-IN + BIT 05
H0	2B2B2-D2	5- 89		
H1	2B2B2-D3	5- 89		CHL 2 READ LIGHT DRIVER
H2	2A4A06J03C-06			
	2A4A06J04C-06			
H3	2A4A06J03C-05			CHAN 2 EXT COMPUTER RUNNING
	2A4A06J04C-05			

I0		2B0B6-L0	6-115	2B0B6-AE	CHL 2 LINE INTERRUPT 1 - C-012
I1		2B0B4-A0	6-105	2B0A1-AJ	CHL 2 INTERRUPT ENABLE
I2	2A4A06J03B-02				
	2A4A06J04B-02				
I3	2A4A06J03B-01				CHL 2 EXTERNAL STATUS BIT 05
	2A4A06J04B-01				
J0	2A4A06J03A-03				CHL 2 EXTERNAL STATUS BIT 01
	2A4A06J04A-03				
J1	2A4A06J03A-04				
	2A4A06J04A-04				
J2	2A4A06J03E-02				
	2A4A06J04E-02				
J3	2A4A06J03E-01				CHL 2 EXT, LINE INTERRUPT 5
	2A4A06J04E-01				
K0	2A4A06J03D-04				
	2A4A06J04D-04				
K1	2A4A06J03D-03				CHL 2 EXT, LINE INTERRUPT 1
	2A4A06J04D-03				
K2		2B0B7-P0	6-113	2B0B7-AR	CHL 2 LINE INTERRUPT 6 - C-062
K3		2B0A6-A0	6-121		CHL 2 STATUS FAN IN BIT 06
L0		2B2B2-R2	5- 89		
L1		2B2B2-R3	5- 89		CHL 2 WRITE LIGHT DRIVER
L2	2A4A06J03B-04				
	2A4A06J04B-04				
L3	2A4A06J03B-03				CHL 2 EXTERNAL STATUS BIT 06
	2A4A06J04B-03				
M0		2B0B7-L1	6-113	2B0B7-AL	CHL 2 LINE INTERRUPT 2 - C-022
M1		2B0A6-I2	6-121		CHL 2 STATUS FAN IN BIT 02
M2	2A4A06J03E-04				
	2A4A06J04E-04				
M3	2A4A06J03E-03				CHL 2 EXT, LINE INTERRUPT 6
	2A4A06J04E-03				
N0		2A0B3-C3	6-129		
N1		2A0B3-C2	6-129		CHAN 2 EXT REJ STAT TO FAN-IN
N2		2A0B3-G3	6-129		CHL 2 PRESET STATUS TO FAN IN
N3		2A0B3-G2	6-129		
O0		2A0B3-W1	6-129		NOT CHAN 2 WRITE STATUS TO FI
O1		2A0B3-W0	6-129		
O2		2A0B3-T2	6-129		
O3		2A0B3-T3	6-129		CHAN 2 INT TO STATUS - FAN-IN
P0	2A4A06J03D-06				
	2A4A06J04D-06				
P1	2A4A06J03D-05				CHL 2 EXT, LINE INTERRUPT 2
	2A4A06J04D-05				
P2		2B0B6-P0	6-115	2B0B6-AR	CHL 2 LINE INTERRUPT 7 - C-072
P3		2B0A5-A0	6-123		CHL 2 STATUS FAN IN BIT 07
Q0	2A4A06J03A-06				
	2A4A06J04A-06				
Q1	2A4A06J03A-05				CHL 2 EXTERNAL STATUS BIT 02
	2A4A06J04A-05				
Q2		2B0A8-R2	6-109		NOT(CHL 2 MASKED INTERRUPT)
Q3		2B0B8-L1	6-111		CHL 2 MASKED INTERRUPT - C-102
R0		2B2B3-J0	5- 87		CHL 2 REJECT LIGHT DRIVER
R1		2B2B3-J1	5- 87		
R2	2A4A06J03E-06				
	2A4A06J04E-06				
R3	2A4A06J03E-05				CHL 2 EXT, LINE INTERRUPT 7
	2A4A06J04E-05				
S0		2B0B6-L1	6-115	2B0B6-AL	CHL 2 LINE INTERRUPT 3 - C-032
S1		2B0A5-I2	6-123		CHL 2 STATUS FAN IN BIT 03
S2	2A4A06J03B-06				
	2A4A06J04B-06				
S3	2A4A06J03B-05				CHL 2 EXTERNAL STATUS BIT 07
	2A4A06J04B-05				
T0	2A4A06J03A-07				CHL 2 EXTERNAL STATUS BIT 03
	2A4A06J04A-07				
T1	2A4A06J03A-08				
	2A4A06J04A-08				
T2	2A4A06J03C-02				
	2A4A06J04C-02				
T3	2A4A06J03C-01				CHL 2 EXTERNAL STATUS BIT 10
	2A4A06J04C-01				
U0	2A4A06J03D-08				
	2A4A06J04D-08				
U1	2A4A06J03D-07				CHL 2 EXT, LINE INTERRUPT 3
	2A4A06J04D-07				
U2	2A4A06J03C-04				
	2A4A06J04C-04				
U3	2A4A06J03C-03				CHL 2 EXTERNAL STATUS BIT 11
	2A4A06J04C-03				
V0		2B0B4-N0	6-105	2B0A1-AZ	NOT(CHAN 2 INT MASK)TO FANOUT
V1		2B0A9-G3	6-101	2B0A1-RY	CHL 2 SELECT EXT INTERRUPT
V2		2B0A5-01	6-123	2B0A5-AT	CHL 2 EXTERNAL STATUS BIT 09
V3		2B0A5-J0	6-123	2B0A5-AE	CHL 2 EXTERNAL STATUS BIT 11
W0		2B0A6-J0	6-121	2B0A6-AE	CHL 2 EXTERNAL STATUS BIT 08
W1		2B0A9-F3	6-101	2B0A1-RZ	CHL 2 SELECT INTERNAL STATUS
W2	2A4A06J03R-09				CHL 2 EXTERNAL STATUS BIT 09
	2A4A06J04R-09				
W3	2A4A06J03R-10				
	2A4A06J04R-10				
X0	2A4A06J03R-08				
	2A4A06J04R-08				
X1	2A4A06J03R-07				CHL 2 EXTERNAL STATUS BIT 08
	2A4A06J04R-07				
X2		2B0B6-F1	6-115		NOT(CHL 2 INTERRUPT MASK) COPY
X3		2R0A6-01	6-121	2B0A6-AT	CHL 2 EXTERNAL STATUS BIT 10



CONTROL DATA	CHAN 2 B CONTROL	PRODUCT	
DEVELOPMENT DIVISION	EXT STAT BITS 00—11→FAN-IN EXT LINE INTS 0—7→FAN-IN	SIZE C	DRAWING NO. 60181000 REV. A
	LOC: 2B0A1 PART NO. 184658 SER. 002	SHEET	PAGE 6-89

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2R0A6-B3	6-121		CHL 3 STATUS FAN IN BIT 00
A3	2R0A6-P2	6-121		CHL 3 STATUS FAN IN BIT 04
B0	2R2R3-H2	5- 87		
B1	2R2R3-H3	5- 87		CHAN 3 PARITY ERR, LT DRIVER
B2	2R2R3-X1	5- 87		CHL 3 INTERRUPT LIGHT DRIVER
B3	2R2R3-X0	5- 87		
C0	2A4A06J01D-01 2A4A06J02D-01			CHL 3 EXT, LINE INTERRUPT 0
C1	2A4A06J01D-02 2A4A06J02D-02			
C2	2A4A06J01A-09 2A4A06J02A-09			CHL 3 EXTERNAL STATUS BIT 04
C3	2A4A06J01A-10 2A4A06J02A-10			
D0	2A0B2-L2	6-131		
D1	2A0B2-L3	6-131		CHAN 3 PE STATUS = FAN-IN
D2	2A0B2-J2	6-131		
D3	2A0B2-J3	6-131		CHAN 3 NO RESPONSE STATUS TO FAN-IN
E0	2A0B2-V0	6-131		NOT CHAN 3 READ STATUS TO FI
E1	2A0B2-V1	6-131		
E2	2A4A06J01D-09 2A4A06J02D-09			CHL 3 EXT, LINE INTERRUPT 4
E3	2A4A06J01D-10 2A4A06J02D-10			
F0	2A4A06J01A-02 2A4A06J02A-02			
F1	2A4A06J01A-01 2A4A06J02A-01			CHL 3 EXTERNAL STATUS BIT 00
F2	2R0R7-U0	6-113	2B0B7-AH	CHL 3 LINE INTERRUPT 4 - C=043
F3	2R0R4-J1	6-105	2B0A0-RL	CHAN 3 CMPTR RUNNING TO XMTR
G0	2R0A5-B3	6-123		CHL 3 STATUS FAN IN BIT 01
G1	2R0B7-Q0	6-113	2B0B7-AD	CHL 3 LINE INTERRUPT 0 - C=003
G2	2R0R6-U0	6-115	2B0B6-AH	CHL 3 LINE INTERRUPT 5 - C=053
G3	2R0A5-P2	6-123		CHAN 3 STATUS FAN-IN - BIT 05
H0	2R2B2-E3	5- 89		
H1	2R2B2-E2	5- 89		CHL 3 READ LIGHT DRIVER
H2	2A4A06J01C-06 2A4A06J02C-06			
H3	2A4A06J01C-05 2A4A06J02C-05			CHAN 3 EXT CMPTR RUNNING

I0	2R0B6-Q0	6-115	2B0B6-AD	CHL 3 LINE INTERRUPT 1 = C=013
I1	2B0B4-X0	6-105	2B0A0-AJ	CHL 3 INTERRUPT ENABLE
I2	2A4A06J01B-02			
	2A4A06J02B-02			
I3	2A4A06J01B-01			CHL 3 EXTERNAL STATUS BIT 05
	2A4A06J02B-01			
J0	2A4A06J01A-03			CHL 3 EXTERNAL STATUS BIT 01
	2A4A06J02A-03			
J1	2A4A06J01A-04			
	2A4A06J02A-04			
J2	2A4A06J01E-02			
	2A4A06J02E-02			
J3	2A4A06J01E-01			CHL 3 EXT, LINE INTERRUPT 5
	2A4A06J02E-01			
K0	2A4A06J01D-04			
	2A4A06J02D-04			
K1	2A4A06J01D-03			CHL 3 EXT, LINE INTERRUPT 1
	2A4A06J02D-03			
K2	2R0B7-V1	6-113	2B0B7-AU	CHL 3 LINE INTERRUPT 6 = C=063
K3	2B0A6-C0	6-121		CHL 3 STATUS FAN IN BIT 06
L0	2B2B2-S2	5- 89		
L1	2B2B2-S3	5- 89		CHL 3 WRITE LIGHT DRIVER
L2	2A4A06J01B-04			
	2A4A06J02B-04			
L3	2A4A06J01B-03			CHL 3 EXTERNAL STATUS BIT 06
	2A4A06J02B-03			
M0	2B0B7-S1	6-113	2B0B7-AJ	CHL 3 LINE INTERRUPT 2 = C=023
M1	2B0A6-J3	6-121		CHL 3 STATUS FAN IN BIT 02
M2	2A4A06J01E-04			
	2A4A06J02E-04			
M3	2A4A06J01E-03			CHL 3 EXT, LINE INTERRUPT 6
	2A4A06J02E-03			
N0	2A0B2-C3	6-131		
N1	2A0B2-C2	6-131		CHAN 3 EXT REJ STAT TO FAN-IN
N2	2A0B2-G3	6-131		CHL 3 PRESET STATUS TO FAN IN
N3	2A0B2-G2	6-131		
O0	2A0B2-W1	6-131		NOT CHAN 3 WRITE STATUS TO FI
O1	2A0B2-W0	6-131		
O2	2A0B2-T2	6-131		
O3	2A0B2-T3	6-131		CHAN 3 INT TO STATUS FAN-IN
P0	2A4A06J01D-06			
	2A4A06J02D-06			
P1	2A4A06J01D-05			CHL 3 EXT, LINE INTERRUPT 2
	2A4A06J02D-05			
P2	2R0B6-V1	6-115	2B0B6-AU	CHL 3 LINE INTERRUPT 7 = C=073
P3	2B0A5-C0	6-123		CHL 3 STATUS FAN IN BIT 07
Q0	2A4A06J01A-06			
	2A4A06J02A-06			
Q1	2A4A06J01A-05			CHL 3 EXTERNAL STATUS BIT 02
	2A4A06J02A-05			
Q2	2B0A8-R3	6-109		NOT(CHL 3 MASKED INTERRUPT)
Q3	2R0B8-M1	6-111		CHL 3 MASKED INTERRUPT = C=103
R0	2R2B3-I1	5- 87		CHL 3 REJECT LIGHT DRIVER
R1	2R2B3-I0	5- 87		
R2	2A4A06J01E-06			
	2A4A06J02E-06			
R3	2A4A06J01E-05			CHL 3 EXT, LINE INTERRUPT 7
	2A4A06J02E-05			
S0	2B0B6-S1	6-115	2B0B6-AJ	CHL 3 LINE INTERRUPT 3 = C=033
S1	2B0A5-J3	6-123		CHL 3 STATUS FAN IN BIT 03
S2	2A4A06J01B-06			
	2A4A06J02B-06			
S3	2A4A06J01B-05			CHL 3 EXTERNAL STATUS BIT 07
	2A4A06J02B-05			
T0	2A4A06J01A-07			CHL 3 EXTERNAL STATUS BIT 03
	2A4A06J02A-07			
T1	2A4A06J01A-08			
	2A4A06J02A-08			
T2	2A4A06J01C-02			
	2A4A06J02C-02			
T3	2A4A06J01C-01			CHL 3 EXTERNAL STATUS BIT 10
	2A4A06J02C-01			
U0	2A4A06J01D-08			
	2A4A06J02D-08			
U1	2A4A06J01D-07			CHL 3 EXT, LINE INTERRUPT 3
	2A4A06J02D-07			
U2	2A4A06J01C-04			
	2A4A06J02C-04			
U3	2A4A06J01C-03			CHL 3 EXTERNAL STATUS BIT 11
	2A4A06J02C-03			
V0	2R0B4-L0	6-105	2B0A0-AZ	NOT(CHAN 3 INT MASK)TO FAN-OUT
V1	2B0A9-H2	6-101	2B0A0-BY	CHL 3 SELECT EXT INTERRUPT
V2	2B0A5-U1	6-123	2B0A5-AV	CHL 3 EXTERNAL STATUS BIT 09
V3	2B0A5-K1	6-123	2B0A5-BY	CHL 3 EXTERNAL STATUS BIT 11
W0	2R6A6-K1	6-121	2B0A6-BY	CHL 3 EXTERNAL STATUS BIT 08
W1	2B0A9-G2	6-101	2B0A0-BZ	CHL 3 SELECT INTERNAL STATUS
W2	2A4A06J01B-09			CHL 3 EXTERNAL STATUS BIT 09
	2A4A06J02B-09			
W3	2A4A06J01B-10			
	2A4A06J02B-10			
X0	2A4A06J01B-08			
	2A4A06J02B-08			
X1	2A4A06J01B-07			CHL 3 EXTERNAL STATUS BIT 08
	2A4A06J02B-07			
X2	2B0B6-J0	6-115		NOT(CHL 3 INTERRUPT MASK) COPY
X3	2B0A6-U1	6-121	2B0A6-AV	CHL 3 EXTERNAL STATUS BIT 10

CONTROL DATA	CHAN 3 B CONTROL	PRODUCT	
DEVELOPMENT DIVISION	EXT STAT BITS 00—11→FAN-IN	SIZE C	DRAWING NO. 60181000
	EXT LINE INTS 0—7→FAN-IN	SHEET	PAGE 6-91
	LOC: 2B0A0 PART NO. 184658 SER. 003		REV. A

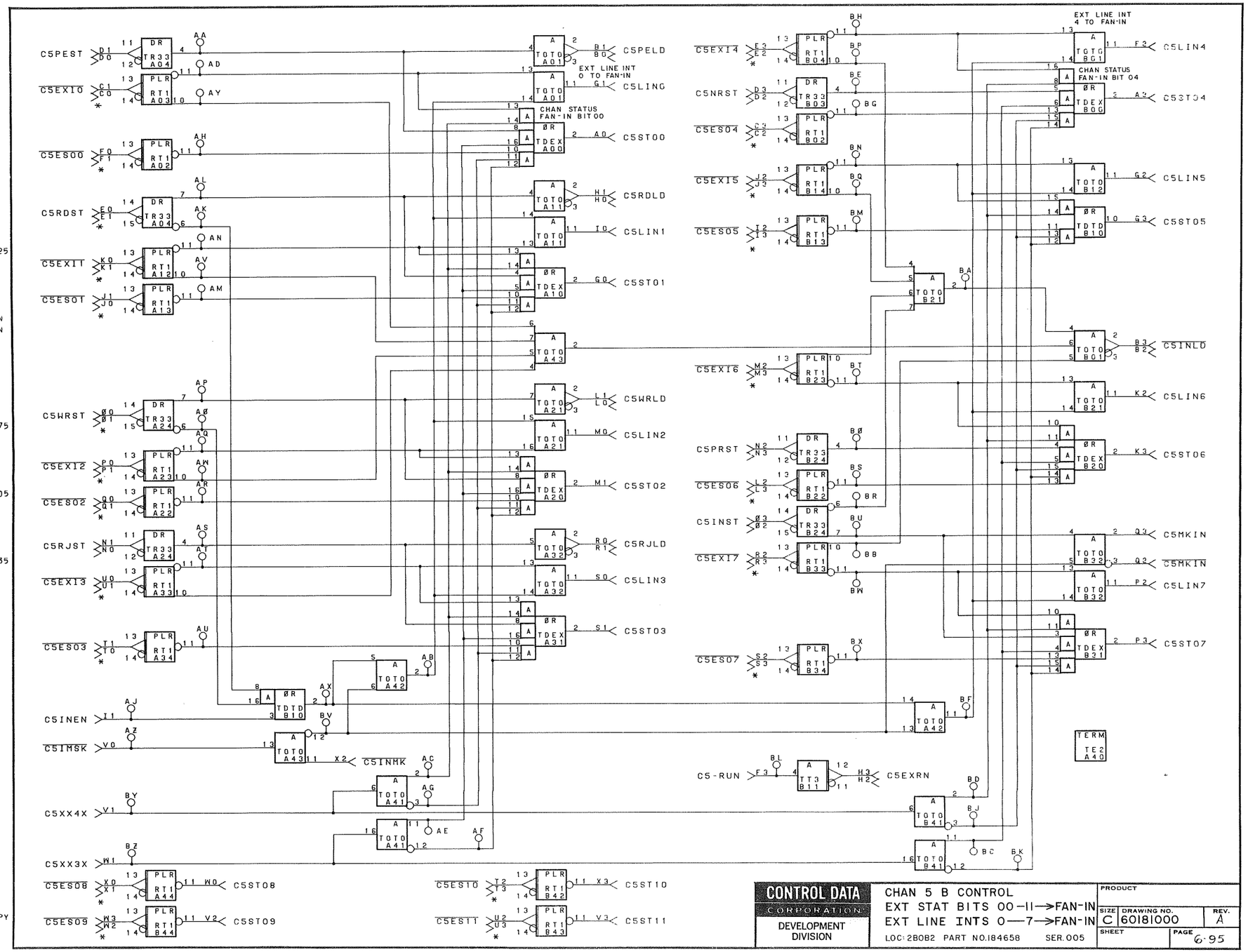
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2R0A6-H2	6-121		CHL 4 STATUS FAN IN BIT 00
A3	2R0A6-R3	6-121		CHL 4 STATUS FAN IN BIT 04
B0	2R2R3-N2	5- 87		
B1	2R2R3-N3	5- 87		CHAN 4 PARITY ERR, LT DRIVER
B2	2R2R3-W1	5- 87		NOT CHL 4 INT LIGHT DRIVER
B3	2R2R3-W0	5- 87		
C0	2A4A07J03D-01			CHL 4 EXT, LINE INTERRUPT 0
	2A4A07J04D-01			
C1	2A4A07J03D-02			
	2A4A07J04D-02			
C2	2A4A07J03A-09			CHL 4 EXTERNAL STATUS BIT 04
	2A4A07J04A-09			
C3	2A4A07J03A-10			
	2A4A07J04A-10			
D0	2C0A7-L2	6-161		
D1	2C0A7-L3	6-161		CHAN 4 PE STATUS = FAN-IN
D2	2C0A7-J2	6-161		
D3	2C0A7-J3	6-161		CHAN 4 NO RESPONSE STATUS TO FAN-IN
E0	2C0A7-V0	6-161		NOT CHL 4 READ STAT TO FI
E1	2C0A7-V1	6-161		
E2	2A4A07J03D-09			CHL 4 EXT, LINE INTERRUPT 4
	2A4A07J04D-09			
E3	2A4A07J03D-10			
	2A4A07J04D-10			
F0	2A4A07J03A-02			
	2A4A07J04A-02			
F1	2A4A07J03A-01			CHL 4 EXTERNAL STATUS BIT 00
	2A4A07J04A-01			
F2	2R0R7-R3	6-113	2B0B7-RK	CHL 4 LINE INTERRUPT 4 = C=044
F3	2R0A4-J0	6-103	2B0B3-RL	CHAN 4 CMPTR RUNNING TO XMTR
G0	2R0A5-H2	6-123		CHL 4 STATUS FAN IN BIT 01
G1	2R0B7-H2	6-113	2B0B7-RX	CHL 4 LINE INTERRUPT 0 - C=004
G2	2R0R6-R3	6-115	2B0B6-RK	CHL 4 LINE INTERRUPT 5 - C=054
G3	2R0A5-R3	6-123		CHL 4 STATUS FAN IN BIT 05
H0	2R2B2-H2	5- 89		
H1	2R2B2-H3	5- 89		CHL 4 READ LIGHT DRIVER
H2	2A4A07J03C-06			
	2A4A07J04C-06			
H3	2A4A07J03C-05			CHAN 4 EXTERNAL CMPTR RUNNING
	2A4A07J04C-05			
I0	2R0B6-H2	6-115	2B0B6-RX	CHL 4 LINE INTERRUPT 1 = C=014

I1		2R0A4-K3	6-103	2B0B3-AJ	CHL 4 INTERRUPT ENABLE
I2	2A4A07J03R-02				
	2A4A07J04R-02				
I3	2A4A07J03R-01				CHL 4 EXTERNAL STATUS BIT 05
	2A4A07J04R-01				
J0	2A4A07J03A-03				CHL 4 EXTERNAL STATUS BIT 01
	2A4A07J04A-03				
J1	2A4A07J03A-04				
	2A4A07J04A-04				
J2	2A4A07J03E-02				
	2A4A07J04E-02				
J3	2A4A07J03E-01				CHL 4 EXT. LINE INTERRUPT 5
	2A4A07J04E-01				
K0	2A4A07J03D-04				
	2A4A07J04D-04				
K1	2A4A07J03D-03				CHL 4 EXT. LINE INTERRUPT 1
	2A4A07J04D-03				
K2		2R0R7-R2	6-113	2B0B7-BF	CHL 4 LINE INTERRUPT 6 - C=064
K3		2R0A6-H1	6-121		CHL 4 STATUS FAN IN BIT 06
L0		2R2R2-T2	5- 89		
L1		2R2R2-T3	5- 89		CHL 4 WRITE LIGHT DRIVER
L2	2A4A07J03R-04				
	2A4A07J04R-04				
L3	2A4A07J03R-03				CHL 4 EXTERNAL STATUS BIT 06
	2A4A07J04R-03				
M0		2R0R7-W3	6-113	2B0B7-BL	CHL 4 LINE INTERRUPT 2 - C=024
M1		2R0A6-M2	6-121		CHL 4 STATUS FAN IN BIT 02
M2	2A4A07J03E-04				
	2A4A07J04E-04				
M3	2A4A07J03E-03				CHL 4 EXT. LINE INTERRUPT 6
	2A4A07J04E-03				
N0		2C0A7-C3	6-161		
N1		2C0A7-C2	6-161		CHAN 4 EXT REJ STAT TO FAN-IN
N2		2C0A7-G3	6-161		CHL 4 PRESET STATUS TO FAN IN
N3		2C0A7-G2	6-161		
O0		2C0A7-M1	6-161		CHL 4 WRITE STATUS TO FAN IN
O1		2C0A7-W0	6-161		
O2		2C0A7-T2	6-161		
O3		2C0A7-T3	6-161		CHL 4 INTERRUPT TO STATUS F1
P0	2A4A07J03D-06				
	2A4A07J04D-06				
P1	2A4A07J03D-05				CHL 4 EXT. LINE INTERRUPT 2
	2A4A07J04D-05				
P2		2R0R6-R2	6-115	2B0B6-BF	CHL 4 LINE INTERRUPT 7 - C=074
P3		2R0A5-H1	6-123		CHL 4 STATUS FAN IN BIT 07
Q0	2A4A07J03A-06				
	2A4A07J04A-06				
Q1	2A4A07J03A-05				CHL 4 EXTERNAL STATUS BIT 02
	2A4A07J04A-05				
Q2		2R0A8-02	6-109		NOT(CHL 4 MASKED INTERRUPT)
Q3		2R0R8-G1	6-111		CHL 4 MASKED INTERRUPT - C=104
R0		2R2R3-H1	5- 87		CHL 4 REJECT LIGHT DRIVER
R1		2R2R3-H0	5- 87		
R2	2A4A07J03E-06				
	2A4A07J04E-06				
R3	2A4A07J03E-05				CHL 4 EXT. LINE INTERRUPT 7
	2A4A07J04E-05				
S0		2R0R6-W3	6-115	2B0B6-BL	CHL 4 LINE INTERRUPT 3 - C=034
S1		2R0A5-M2	6-123		CHL 4 STATUS FAN IN BIT 03
S2	2A4A07J03R-06				
	2A4A07J04R-06				
S3	2A4A07J03R-05				CHL 4 EXTERNAL STATUS BIT 07
	2A4A07J04R-05				
T0	2A4A07J03A-07				CHL 4 EXTERNAL STATUS BIT 03
	2A4A07J04A-07				
T1	2A4A07J03A-08				
	2A4A07J04A-08				
T2	2A4A07J03C-02				
	2A4A07J04C-02				
T3	2A4A07J03C-01				CHL 4 EXTERNAL STATUS BIT 10
	2A4A07J04C-01				
U0	2A4A07J03D-08				
	2A4A07J04D-08				
U1	2A4A07J03D-07				CHL 4 EXT. LINE INTERRUPT 3
	2A4A07J04D-07				
U2	2A4A07J03C-04				
	2A4A07J04C-04				
U3	2A4A07J03C-03				CHL 4 EXTERNAL STATUS BIT 11
	2A4A07J04C-03				
V0		2R0A4-D3	6-103	2B0B3-AZ	NOT (CHAN 4 INTERRUPT MASK) TO FANOUT
V1		2R0A9-B3	6-101	2B0B3-BY	CHL 4 SELECT EXT INTERRUPT
V2		2R0A5-N1	6-123	2B0A5-AL	CHL 4 EXTERNAL STATUS BIT 09
V3		2R0A5-10	6-123	2B0A5-AD	CHL 4 EXTERNAL STATUS BIT 11
W0		2R0A6-10	6-121	2B0A6-AD	CHL 4 EXTERNAL STATUS BIT 08
W1		2R0A9-D3	6-101	2B0B3-BZ	CHL 4 SELECT INTERNAL STATUS
W2	2A4A07J03R-09				CHL 4 EXTERNAL STATUS BIT 09
	2A4A07J04R-09				
W3	2A4A07J03R-10				
	2A4A07J04R-10				
X0	2A4A07J03R-08				
	2A4A07J04R-08				
X1	2A4A07J03R-07				CHL 4 EXTERNAL STATUS BIT 08
	2A4A07J04R-07				
X2		2R0R7-S3	6-113		NOT(CHL 4 INTERRUPT MASK) COPY
X3		2R0A6-N1	6-121	2B0A6-AL	CHL 4 EXTERNAL STATUS BIT 10

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	CHAN 4 B CONTROL EXT STAT BITS 00—11→FAN-IN EXT LINE INTS 0—7→FAN-IN LOC:2B0B3 PART NO.184658 SER.004	PRODUCT	
		SIZE C	DRAWING NO. 60181000
		REV. A	
		SHEET	PAGE 6-97

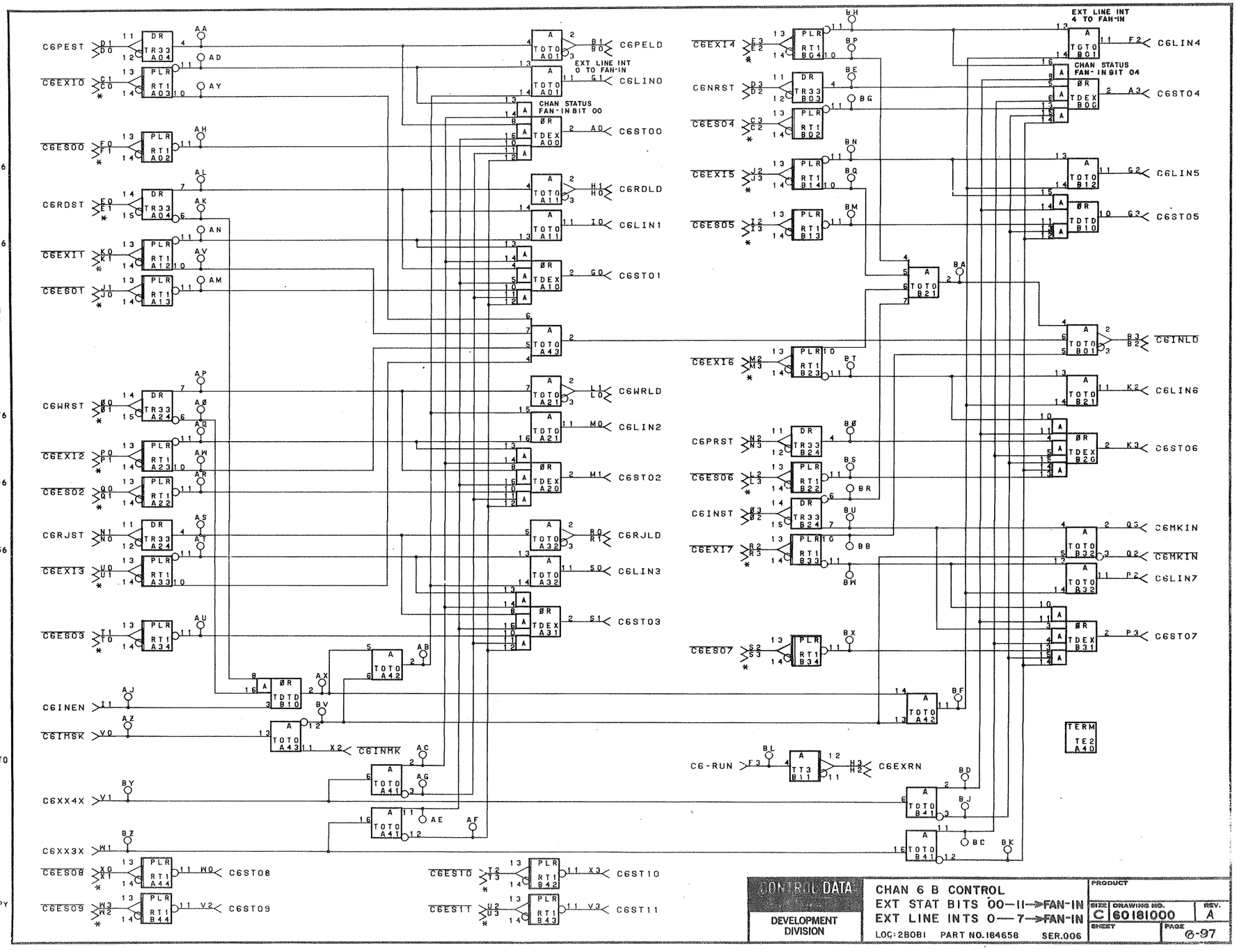
PIN	ORIGIN/ DEST,	PAGE	TEST POINT	SIGNAL DEFINITION,
A0	280A6-F3	6-121		CHL 5 STATUS FAN IN BIT 00
A3	280A6-T3	6-121		CHL 5 STATUS FAN IN BIT 04
B0	28283-03	5- 87		
B1	28283-02	5- 87		CHL 5 PARITY ERROR LIGHT DRIVE
B2	28283-C3	5- 87		CHL 5 INTERRUPT LIGHT DRIVER
B3	28283-C2	5- 87		
C0	2A4A07J01D-01 2A4A07J02D-01			CHL 5 EXT, LINE INTERRUPT 0
C1	2A4A07J01D-02 2A4A07J02D-02			
C2	2A4A07J01A-09 2A4A07J02A-09			CHL 5 EXTERNAL STATUS BIT 04
C3	2A4A07J01A-10 2A4A07J02A-10			
D0	2C0A6-L2	6-163		
D1	2C0A6-L3	6-163		CHAN 5 PE STATUS - FAN-IN
D2	2C0A6-J2	6-163		
D3	2C0A6-J3	6-163		CHAN 5 NO RESPONSE STATUS TO FAN-IN
E0	2C0A6-V0	6-163		NOT CHL 5 READ STAT TO FI
E1	2C0A6-V1	6-163		
E2	2A4A07J01D-09 2A4A07J02D-09			CHL 5 EXT, LINE INTERRUPT 4
E3	2A4A07J01D-10 2A4A07J02D-10			
F0	2A4A07J01A-02 2A4A07J02A-02			
F1	2A4A07J01A-01 2A4A07J02A-01			CHL 5 EXTERNAL STATUS BIT 00
F2	28087-K3	6-113	28087-RJ	CHL 5 LINE INTERRUPT 4 - C=045
F3	28084-J1	6-103	28082-RL	CHAN 5 CMPTR RUNNING TO XMTR
G0	28085-F3	6-123		CHL 5 STATUS FAN IN BIT 01
G1	28087-02	6-113	28087-RS	CHL 5 LINE INTERRUPT 0 - C=005
G2	28086-K3	6-115	28086-RJ	CHL 5 LINE INTERRUPT 5 - C=055
G3	28085-T3	6-123		CHAN 5 STAT FAN-IN - BIT 05
H0	28282-I2	5- 89		
H1	28282-I3	5- 89		CHL 5 READ LIGHT DRIVER
H2	2A4A07J01C-06 2A4A07J02C-06			
H3	2A4A07J01C-05 2A4A07J02C-05			CHAN 5 EXTERNAL CMPTR RUNNING
I0	28086-Q2	6-115	28086-RS	CHL 5 LINE INTERRUPT 1 - C=015

I1	2R0A4-X2	6-103	2B0B2-AJ	CHL 5 INTERRUPT ENABLE
I2	2A4A07J01H-02			
	2A4A07J02H-02			
I3	2A4A07J01H-01			CHL 5 EXTERNAL STATUS BIT 05
	2A4A07J02H-01			
J0	2A4A07J01A-03			CHL 5 EXTERNAL STATUS BIT 01
	2A4A07J02A-03			
J1	2A4A07J01A-04			
	2A4A07J02A-04			
J2	2A4A07J01F-02			
	2A4A07J02F-02			
J3	2A4A07J01F-01			CHL 5 EXT. LINE INTERRUPT 5
	2A4A07J02F-01			
K0	2A4A07J01D-04			
	2A4A07J02D-04			
K1	2A4A07J01D-03			CHL 5 EXT. LINE INTERRUPT 1
	2A4A07J02D-03			
K2	2R0B7-M2	6-113	2B0B7-RD	CHAN 5 LINE INT. 6- C=065
K3	2R0A6-H0	6-121		CHL 5 STATUS FAN IN BIT 06
L0	2R2R2-W2	5- 89		
L1	2R2R2-W3	5- 89		CHL 5 WRITE LIGHT DRIVER
L2	2A4A07J01B-04			
	2A4A07J02B-04			
L3	2A4A07J01B-03			CHL 5 EXTERNAL STATUS BIT 06
	2A4A07J02B-03			
M0	2R0B7-Q3	6-113	2B0B7-RP	CHL 5 LINE INTERRUPT 2 - C=025
M1	2R0A6-L3	6-121		CHL 5 STATUS FAN IN BIT 02
M2	2A4A07J01E-04			
	2A4A07J02F-04			
M3	2A4A07J01E-03			CHL 5 EXT. LINE INTERRUPT 6
	2A4A07J02F-03			
N0	2C0A6-C3	6-163		
N1	2C0A6-C2	6-163		CHAN 5 EXT REJ STAT TO FAN-IN
N2	2C0A6-G3	6-163		CHL 5 PRESET STATUS TO FAN IN
N3	2C0A6-G2	6-163		
O0	2C0A6-W1	6-163		NOT CHL 5 WRITE STAT TO FI
O1	2C0A6-W0	6-163		
O2	2C0A6-T2	6-163		
O3	2C0A6-T3	6-163		CHAN 5 INT TO STATUS FAN-IN
P0	2A4A07J01D-06			
	2A4A07J02D-06			
P1	2A4A07J01D-05			CHL 5 EXT. LINE INTERRUPT 2
	2A4A07J02D-05			
P2	2R0R6-M2	6-115	2B0B6-RD	CHL 5 LINE INTERRUPT 7 - C=075
P3	2R0A5-H0	6-123		CHL 5 STATUS FAN IN BIT 07
Q0	2A4A07J01A-06			
	2A4A07J02A-06			
Q1	2A4A07J01A-05			CHL 5 EXTERNAL STATUS BIT 02
	2A4A07J02A-05			
Q2	2R0A8-03	6-109		NOT(CHL 5 MASKED INTERRUPT
Q3	2R0R8-11	6-111		CHL 5 MASKED INTERRUPT - C=105
R0	2R2R3-00	5- 87		CHL 5 REJECT LIGHT DRIVER
R1	2R2R3-01	5- 87		
R2	2A4A07J01E-06			
	2A4A07J02E-06			
R3	2A4A07J01E-05			CHL 5 EXT. LINE INTERRUPT 7
	2A4A07J02F-05			
S0	2R0R6-Q3	6-115	2B0B6-RP	CHL 5 LINE INTERRUPT 3 - C=035
S1	2R0A5-L3	6-123		CHL 5 STATUS FAN IN BIT 03
S2	2A4A07J01B-06			
	2A4A07J02B-06			
S3	2A4A07J01B-05			CHL 5 EXTERNAL STATUS BIT 07
	2A4A07J02B-05			
T0	2A4A07J01A-07			CHL 5 EXTERNAL STATUS BIT 03
	2A4A07J02A-07			
T1	2A4A07J01A-08			
	2A4A07J02A-08			
T2	2A4A07J01C-02			
	2A4A07J02C-02			
T3	2A4A07J01C-01			CHL 5 EXTERNAL STATUS BIT 10
	2A4A07J02C-01			
U0	2A4A07J01D-08			
	2A4A07J02D-08			
U1	2A4A07J01D-07			CHL 5 EXT. LINE INTERRUPT 3
	2A4A07J02D-07			
U2	2A4A07J01C-04			
	2A4A07J02C-04			
U3	2A4A07J01C-03			CHL 5 EXTERNAL STATUS BIT 11
	2A4A07J02C-03			
V0	2R0A4-M3	6-103	2B0B2-AZ	NOT (CHAN 5 INT MASK) TO FANOUT
V1	2R0A9-C2	6-101	2B0B2-BY	CHL 5 SELECT EXT INTERRUPT
V2	2R0A5-W0	6-123	2R0A5-BS	CHL 5 EXTERNAL STATUS BIT 09
V3	2R0A5-M1	6-123	2R0A5-AJ	CHL 5 EXTERNAL STATUS BIT 11
W0	2R0A6-M1	6-121	2B0A6-AJ	CHL 5 EXTERNAL STATUS BIT 08
W1	2R0A9-E2	6-101	2B0B2-BZ	CHL 5 SELECT INTERNAL STATUS
W2	2A4A07J01H-09			CHL 5 EXTERNAL STATUS BIT 09
	2A4A07J02H-09			
W3	2A4A07J01H-10			
	2A4A07J02H-10			
X0	2A4A07J01H-08			
	2A4A07J02H-08			
X1	2A4A07J01H-07			CHL 5 EXTERNAL STATUS BIT 08
	2A4A07J02H-07			
X2	2R0R7-U2	6-113		NOT(CHL 5 INTERRUPT MASK) COPY
X3	2R0A6-V0	6-121	2R0A6-BS	CHL 5 EXTERNAL STATUS BIT 10



PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B0A6-G3	6-121		CHL 6 STATUS FAN IN BIT 00
A3	2B0A6-N3	6-121		CHL 6 STATUS FAN IN BIT 04
B0	2R2B3-R2	5- 87		
B1	2R2B3-R3	5- 87		CHAN 6 PARITY ERR, LT DRIVER
B2	2R2B3-D3	5- 87		NOT CHL 6 INT LIGHT DRIVER
B3	2R2B3-D2	5- 87		
C0	2A4A0AJ03D-01 2A4A0AJ04D-01			CHL 6 EXT. LINE INTERRUPT 0
C1	2A4A08J03D-02 2A4A0AJ04D-02			
C2	2A4A0AJ03A-09 2A4A0AJ04A-09			CHL 6 EXTERNAL STATUS BIT 04
C3	2A4A0AJ03A-10 2A4A0AJ04A-10			
D0	2C0A3-L2	6-165		
D1	2C0A3-L3	6-165		CHAN 6 PE STATUS + FAN-IN
D2	2C0A3-J2	6-165		
D3	2C0A3-J3	6-165		CHAN 6 NO RESPONSE STATUS TO FAN-IN
E0	2C0A3-V0	6-165		NOT CHL 6 READ STAT TO FI
E1	2C0A3-V1	6-165		
E2	2A4A08J03D-09 2A4A08J04D-09			CHL 6 EXT. LINE INTERRUPT 4
E3	2A4A08J03D-10 2A4A08J04D-10			
F0	2A4A0AJ03A-02 2A4A0AJ04A-02			
F1	2A4A0AJ03A-01 2A4A08J04A-01			CHL 6 EXTERNAL STATUS BIT 00
F2	2R0A7-E3	6-113	2B0B7-RG	CHL 6 LINE INTERRUPT 4 - C=046
F3	2R0A4-J0	6-105	2B0B1-RL	CHAN 6 CMPTR RUNNING TO XMTR
G0	2R0A5-G3	6-123		CHL 6 STATUS FAN IN BIT 01
G1	2R0A7-J3	6-113	2B0B7-RW	CHL 6 LINE INTERRUPT 0 - C=006
G2	2R0A6-E3	6-115	2B0B6-RG	CHL 6 LINE INTERRUPT 5 - C=056
G3	2R0A5-N3	6-123		CHAN 6 STATUS FAN-IN - BIT 05
H0	2R2A2-J3	5- 89		
H1	2B2B2-J2	5- 89		CHL 6 READ LIGHT DRIVER
H2	2A4A08J03C-06 2A4A08J04C-06			
H3	2A4A08J03C-05 2A4A08J04C-05			CHAN 6 EXTERNAL CMPTR RUNNING
I0	2R0B6-J3	6-115	2B0B6-RW	CHL 6 LINE INTERRUPT 1 - C=016

I1	2B0B4-K3	6-105	2B0B1-AJ	CHL 6 INTERRUPT ENABLE
I2	2A4A08J03R-02			
	2A4A08J04R-02			
I3	2A4A08J03R-01			CHL 6 EXTERNAL STATUS BIT 05
	2A4A08J04R-01			
J0	2A4A08J03A-03			CHL 6 EXTERNAL STATUS BIT 01
	2A4A08J04A-03			
J1	2A4A08J03A-04			
	2A4A08J04A-04			
J2	2A4A08J03E-02			
	2A4A08J04E-02			
J3	2A4A08J03E-01			CHL 6 EXT, LINE INTERRUPT 5
	2A4A08J04E-01			
K0	2A4A08J03D-04			
	2A4A08J04D-04			
K1	2A4A08J03D-03			CHL 6 EXT, LINE INTERRUPT 1
	2A4A08J04D-03			
K2	2B0B7-D2	6-113	2B0B7-RC	CHL 6 LINE INTERRUPT 6 - C=066
K3	2B0A6-G0	6-121		CHL 6 STATUS FAN IN BIT 06
L0	2B2B2-X2	5- 89		
L1	2B2B2-X3	5- 89		CHL 6 WRITE LIGHT DRIVER
L2	2A4A08J03B-04			
	2A4A08J04B-04			
L3	2A4A08J03B-03			CHL 6 EXTERNAL STATUS BIT 06
	2A4A08J04B-03			
M0	2B0B7-K2	6-113	2B0B7-RN	CHL 6 LINE INTERRUPT 2 - C=026
M1	2B0A6-I3	6-121		CHL 6 STATUS FAN IN BIT 02
M2	2A4A08J03E-04			
	2A4A08J04E-04			
M3	2A4A08J03E-03			CHL 6 EXT, LINE INTERRUPT 6
	2A4A08J04E-03			
N0	2C0A3-C3	6-165		
N1	2C0A3-C2	6-165		CHAN 6 EXT REJ STAT TO FAN-IN
N2	2C0A3-G3	6-165		CHL 6 PRESET STATUS TO FAN IN
N3	2C0A3-G2	6-165		
O0	2C0A3-W1	6-165		NOT CHL 6 WRITE STAT TO FI
O1	2C0A3-W0	6-165		
O2	2C0A3-T2	6-165		
O3	2C0A3-T3	6-165		CHAN 6 INT TO STATUS FAN-IN
P0	2A4A08J03D-06			
	2A4A08J04D-06			
P1	2A4A08J03D-05			CHL 6 EXT, LINE INTERRUPT 2
	2A4A08J04D-05			
P2	2B0B6-D2	6-115	2B0B6-RC	CHL 6 LINE INTERRUPT 7 - C=076
P3	2B0A5-G0	6-123		CHL 6 STATUS FAN IN BIT 07
Q0	2A4A08J03A-06			
	2A4A08J04A-06			
Q1	2A4A08J03A-05			CHL 6 EXTERNAL STATUS BIT 02
	2A4A08J04A-05			
Q2	2B0A8-P2	6-109		NOT(CHL 6 MASKED INTERRUPT)
Q3	2B0B8-G0	6-111		CHL 6 MASKED INTERRUPT - C=106
R0	2B2B3-N1	5- 87		CHL 6 REJECT LIGHT DRIVER
R1	2B2B3-N0	5- 87		
R2	2A4A08J03E-06			
	2A4A08J04E-06			
R3	2A4A08J03E-05			CHL 6 EXT, LINE INTERRUPT 7
	2A4A08J04E-05			
S0	2B0B6-K2	6-115	2B0B6-RN	CHL 6 LINE INTERRUPT 3 - C=036
S1	2B0A5-I3	6-123		CHL 6 STATUS FAN IN BIT 03
S2	2A4A08J03B-06			
	2A4A08J04B-06			
S3	2A4A08J03B-05			CHL 6 EXTERNAL STATUS BIT 07
	2A4A08J04B-05			
T0	2A4A08J03A-07			CHL 6 EXTERNAL STATUS BIT 03
	2A4A08J04A-07			
T1	2A4A08J03A-08			
	2A4A08J04A-08			
T2	2A4A08J03C-02			
	2A4A08J04C-02			
T3	2A4A08J03C-01			CHL 6 EXTERNAL STATUS BIT 10
	2A4A08J04C-01			
U0	2A4A08J03D-08			
	2A4A08J04D-08			
U1	2A4A08J03D-07			CHL 6 EXT, LINE INTERRUPT 3
	2A4A08J04D-07			
U2	2A4A08J03C-04			
	2A4A08J04C-04			
U3	2A4A08J03C-03			CHL 6 EXTERNAL STATUS BIT 11
	2A4A08J04C-03			
V0	2B0B4-O3	6-105	2B0B1-AZ	NOT (CHAN 6 INTERRUPT MASK) TO FANOUT
V1	2B0A9-H3	6-101	2B0B1-RY	CHL 6 SELECT EXT INTERRUPT
V2	2B0A5-V1	6-123	2B0A5-RZ	CHL 6 EXTERNAL STATUS BIT 09
V3	2B0A5-L1	6-123	2B0A5-AG	CHL 6 EXTERNAL STATUS BIT 11
W0	2B0A6-L1	6-121	2B0A6-AG	CHL 6 EXTERNAL STATUS BIT 08
W1	2B0A9-E3	6-101	2B0B1-RZ	CHL 6 SELECT INTERNAL STATUS
W2	2A4A08J03R-09			CHL 6 EXTERNAL STATUS BIT 09
	2A4A08J04R-09			
W3	2A4A08J03R-10			
	2A4A08J04R-10			
X0	2A4A08J03B-08			
	2A4A08J04B-08			
X1	2A4A08J03R-07			CHL 6 EXTERNAL STATUS BIT 08
	2A4A08J04R-07			
X2	2B0B6-S0	6-115		NOT(CHL 6 INTERRUPT MASK) COPY
X3	2B0A6-V1	6-121	2B0A6-RZ	CHL 6 EXTERNAL STATUS BIT 10



CONTROL DATA	CHAN 6 B CONTROL	PRODUCT	
DEVELOPMENT DIVISION	EXT STAT BITS 00—11→FAN-IN EXT LINE INTS 0—7→FAN-IN	SIZE C	DRAWING NO. 60181000 REV. A
	LOC: 2B0B1 PART NO. 184658 SER. 006	SHEET	PAGE 6-97

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2R0A6-G2	6-121		CHL 7 STATUS FAN IN BIT 00
A3	2R0A6-02	6-121		CHL 7 STATUS FAN IN BIT 04
B0	2R2B3-S2	5- 87		
B1	2R2B3-S3	5- 87		CHAN 7 PARITY ERR, LT DRIVER
B2	2R2B3-E2	5- 87		NOT CHAN 7 INT LIGHT DRIVER
B3	2R2B3-E3	5- 87		
C0	2A4A08J01D-01 2A4A08J02D-01			CHL 7 EXT, LINE INTERRUPT 0
C1	2A4A08J01D-02 2A4A08J02D-02			
C2	2A4A08J01A-09 2A4A08J02A-09			CHL 7 EXTERNAL STATUS BIT 04
C3	2A4A08J01A-10 2A4A08J02A-10			
D0	2C0A2-L2	6-167		
D1	2C0A2-L3	6-167		CHAN 7 PE STATUS • FAN-IN
D2	2C0A2-J2	6-167		
D3	2C0A2-J3	6-167		CHAN 7 NO RESPONSE STATUS TO FAN•IN
E0	2C0A2-V0	6-167		NOT CHL 7 READ STAT TO FI
E1	2C0A2-V1	6-167		
E2	2A4A08J01D-09 2A4A08J02D-09			CHL 7 EXT, LINE INTERRUPT 4
E3	2A4A08J01D-10 2A4A08J02D-10			
F0	2A4A08J01A-02 2A4A08J02A-02			
F1	2A4A08J01A-01 2A4A08J02A-01			CHL 7 EXTERNAL STATUS BIT 00
F2	2R0B7-C2	6-113	2B0B7-RH	CHL 7 LINE INTERRUPT 4 - C=047
F3	2R0R4-J1	6-105	2B0B0-RL	CHAN 7 CMPTR RUNNING TO XMTR
G0	2R0A5-G2	6-123		CHL 7 STATUS FAN IN BIT 01
G1	2R0B7-D3	6-113	2B0B7-RR	CHL 7 LINE INTERRUPT 0 - C=007
G2	2R0B6-C2	6-115	2B0B6-RH	CHL 7 LINE INTERRUPT 5 - C=057
G3	2R0A5-02	6-123		CHAN 7 STATUS FAN•IN - BIT 05
H0	2B2B2-M2	5- 89		
H1	2B2B2-M3	5- 89		CHL 7 READ LIGHT DRIVER
H2	2A4A08J01C-06 2A4A08J02C-06			
H3	2A4A08J01C-05 2A4A08J02C-05			CHAN 7 EXTERNAL CMPTR RUNNING
I0	2R0B6-D3	6-115	2B0B6-RR	CHL 7 LINE INTERRUPT 1 - C=017

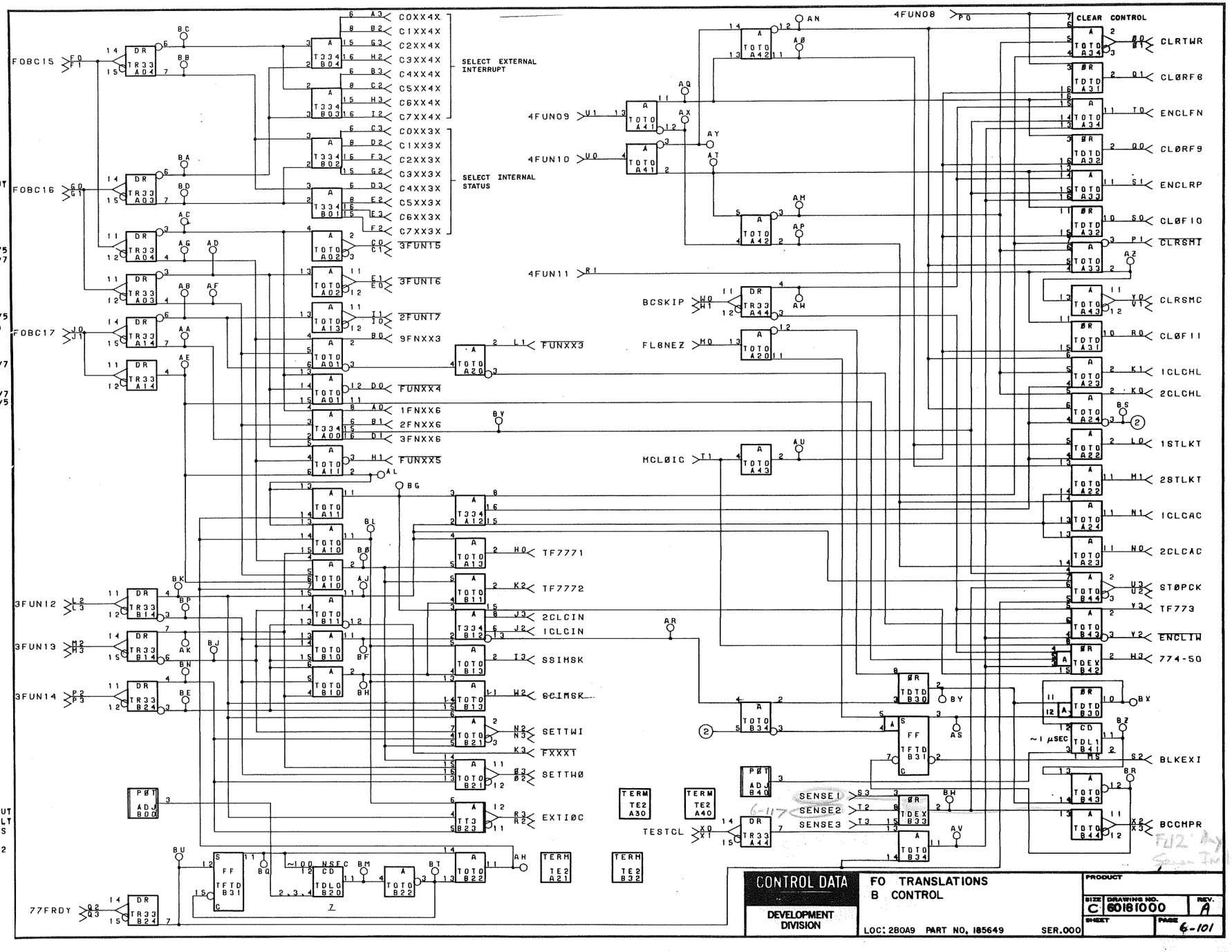
I1	2R0R4-X2	6-105	2B0H0-AJ	CHL 7 INTERRUPT ENABLE
I2	2A4A0RJ01H-02			
	2A4A0RJ02H-02			
I3	2A4A0RJ01H-01			CHL 7 EXTERNAL STATUS BIT 05
	2A4A0RJ02H-01			
J0	2A4A0RJ01A-03			CHL 7 EXTERNAL STATUS BIT 01
	2A4A0RJ02A-03			
J1	2A4A0RJ01A-04			
	2A4A0RJ02A-04			
J2	2A4A0RJ01E-02			
	2A4A0RJ02E-02			
J3	2A4A0RJ01E-01			CHL 7 EXT. LINE INTERRUPT 5
	2A4A0RJ02E-01			
K0	2A4A0RJ01D-04			
	2A4A0RJ02D-04			
K1	2A4A0RJ01D-03			CHL 7 EXT. LINE INTERRUPT 1
	2A4A0RJ02D-03			
K2	2R0R7-A3	6-113	2B0B7-RA	CHL 7 LINE INTERRUPT 6 - C=067
K3	2R0A6-F0	6-121		CHL 7 STATUS FAN IN BIT 06
L0	2R2R3-E1	5- A7		
L1	2R2R3-E0	5- A7		CHL 7 WRITE LIGHT DRIVER
L2	2A4A0RJ01R-04			
	2A4A0RJ02R-04			
L3	2A4A0RJ01R-03			CHL 7 EXTERNAL STATUS BIT 06
	2A4A0RJ02R-03			
M0	2R0R7-C3	6-113	2B0B7-R0	CHL 7 LINE INTERRUPT 2 - C=027
M1	2R0A6-L2	6-121		CHL 7 STATUS FAN IN BIT 02
M2	2A4A0RJ01E-04			
	2A4A0RJ02F-04			
M3	2A4A0RJ01F-03			CHL 7 EXT. LINE INTERRUPT 6
	2A4A0RJ02F-03			
N0	2C0A2-C3	6-167		
N1	2C0A2-C2	6-167		CHAN 7 EXT REJ STAT TO FAN-IN
N2	2C0A2-G3	6-167		CHL 7 PRESET STATUS TO FAN IN
N3	2C0A2-G2	6-167		
O0	2C0A2-W1	6-167		NOT CHL 7 WRITE STAT TO FI
O1	2C0A2-W0	6-167		
O2	2C0A2-T2	6-167		
O3	2C0A2-T3	6-167		CHAN 7 INT TO STATUS FAN-IN
P0	2A4A0RJ01B-06			
	2A4A0RJ02B-06			
P1	2A4A0RJ01B-05			CHL 7 EXT. LINE INTERRUPT 2
	2A4A0RJ02B-05			
P2	2R0R6-A3	6-115	2B0B6-RA	CHL 7 LINE INTERRUPT 7 - C=077
P3	2R0A5-F0	6-123		CHL 7 STATUS FAN IN BIT 07
Q0	2A4A0RJ01A-06			
	2A4A0RJ02A-06			
Q1	2A4A0RJ01A-05			CHL 7 EXTERNAL STATUS BIT 02
	2A4A0RJ02A-05			
Q2	2R0A8-N3	6-109		NOT(CHL 7 MASKED INTERRUPT)
Q3	2R0R8-J1	6-111		CHL 7 MASKED INTERRUPT - C=107
R0	2R2R3-M1	5- A7		CHL 7 REJECT LIGHT DRIVER
R1	2R2R3-M0	5- A7		
R2	2A4A0RJ01F-06			
	2A4A0RJ02F-06			
R3	2A4A0RJ01E-05			CHL 7 EXT. LINE INTERRUPT 7
	2A4A0RJ02E-05			
S0	2R0R6-C3	6-115	2B0B6-R0	CHL 7 LINE INTERRUPT 3 - C=037
S1	2R0A5-L2	6-123		CHL 7 STATUS FAN IN BIT 03
S2	2A4A0RJ01R-06			
	2A4A0RJ02R-06			
S3	2A4A0RJ01R-05			CHL 7 EXTERNAL STATUS BIT 07
	2A4A0RJ02R-05			
T0	2A4A0RJ01A-07			CHL 7 EXTERNAL STATUS BIT 03
	2A4A0RJ02A-07			
T1	2A4A0RJ01A-08			
	2A4A0RJ02A-08			
T2	2A4A0RJ01C-02			
	2A4A0RJ02C-02			
T3	2A4A0RJ01C-01			CHL 7 EXTERNAL STATUS BIT 10
	2A4A0RJ02C-01			
U0	2A4A0RJ01D-08			
	2A4A0RJ02D-08			
U1	2A4A0RJ01D-07			CHL 7 EXT. LINE INTERRUPT 3
	2A4A0RJ02D-07			
U2	2A4A0RJ01C-04			
	2A4A0RJ02C-04			
U3	2A4A0RJ01C-03			CHL 7 EXTERNAL STATUS BIT 11
	2A4A0RJ02C-03			
V0	2R0R4-M3	6-105	2B0H0-AZ	NOT (CHAN 7 INTERRUPT MASK) TO FANOUT
V1	2R0A9-J2	6-101	2B0B0-RY	CHL 7 SELECT EXT INTERRUPT
V2	2R0A5-U0	6-123	2B0A5-RU	CHL 7 EXTERNAL STATUS BIT 09
V3	2R0A5-L0	6-123	2B0A5-AH	CHL 7 EXTERNAL STATUS BIT 11
W0	2R0A6-L0	6-121	2B0A6-AH	CHL 7 EXTERNAL STATUS BIT 08
W1	2R0A9-F2	6-101	2B0B0-RZ	CHL 7 SELECT INTERNAL STATUS
W2	2A4A0RJ01R-09			CHL 7 EXTERNAL STATUS BIT 09
	2A4A0RJ02R-09			
W3	2A4A0RJ01H-10			
	2A4A0RJ02R-10			
X0	2A4A0RJ01R-08			
	2A4A0RJ02R-08			
X1	2A4A0RJ01R-07			CHL 7 EXTERNAL STATUS BIT 08
	2A4A0RJ02R-07			
X2	2R0R6-U2	6-115		NOT(CHL 7 INTERRUPT MASK) COPY
X3	2R0A6-U0	6-121	2B0A6-RU	CHL 7 EXTERNAL STATUS BIT 10

CONTROL DATA CORPORATION	CHAN 7 B CONTROL	PRODUCT	
DEVELOPMENT DIVISION	EXT STAT BITS 00—11→FAN-IN	SIZE C	DRAWING NO. 60181000 REV. A
	EXT LINE INTS 0— 7→FAN-IN	SHEET	PAGE 6-99
	LOC: 2B0B0 PART NO. 184658 SER. 007		

285

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2R0A6-J1	6-121		SELECT PAUSE FAN IN EVEN STAT.
A3	2R0A3-V1	6- 85	2B0A3-RY	CHL 0 SELECT EXT INTERRUPT
B0	2R0A5-T2	6-123		EN ILLEGAL WRITE TO STATUS 05
B1	2R0A5-J1	6-123		SELECT PAUSE FAN IN ODD STATUS
B2	2R0A2-V1	6- 87	2B0A2-RY	CHL 1 SELECT EXT INTERRUPT
B3	2R0B3-V1	6- 93	2B0B3-RY	CHL 4 SELECT EXT INTERRUPT
C0	2A1A7-R3	6- 51		
C1	2A1A7-R2	6- 51		NOT F0 BIT 15 TO Z REG FI
C2	2R0B2-V1	6- 95	2B0B2-RY	CHL 5 SELECT EXT INTERRUPT
C3	2R0A3-W1	6- 85	2B0A3-RZ	CHL 0 SELECT INTERNAL STATUS
D0	2R0A7-J3	6-117	2B0A7-RL	NOT(SEL INTERRUPT FAN IN)
D1	2R0A8-H3	6-109		F=XX6 TO TEST STO AVAIL, XLTN
D2	2R0A2-W1	6- 87	2B0A2-RZ	CHL 1 SELECT INTERNAL STATUS
D3	2R0B3-W1	6- 93	2B0B3-RZ	CHL 4 SELECT INTERNAL STATUS
E0	2A1B8-01	6- 53		NOT F0 BIT 16 TO Z REG FI
E1	2A1B8-00	6- 53		
E2	2R0B2-W1	6- 95	2B0B2-RZ	CHL 5 SELECT INTERNAL STATUS
E3	2R0B1-W1	6- 97	2B0B1-RZ	CHL 6 SELECT INTERNAL STATUS
F0	2A1A06P04B-09 1A4A06J10R-09 1B0A2-E0	2- 31		F0 REGISTER BIT 15

F1	2A1A06P04B-10				
	1A4A06J10B-10				
	1R0A2-E1	2- 31			
F2	2R0B0-W1	6- 99	2B0B0-RZ	CHL 7 SELECT INTERNAL STATUS	
F3	2R0A1-W1	6- 89	2B0A1-RZ	CHL 2 SELECT INTERNAL STATUS	
G0	2A1A06P04C-01			FO REGISTER BIT 16	
	1A4A06J10C-01				
	1R0A2-N0	2- 31			
G1	2A1A06P04C-02				
	1A4A06J10C-02				
	1R0A2-N1	2- 31			
G2	2R0A0-W1	6- 91	2B0A0-RZ	CHL 3 SELECT INTERNAL STATUS	
G3	2R0A1-V1	6- 89	2B0A1-RY	CHL 2 SELECT EXT INTERRUPT	
H0	2R0A7-M1	6-117	2B0A7-AJ	SET EXPONENT OVERFLOW FAULT	
H1	2R0A8-F2	6-109		NOT (F=XX5) TO 77,51 XLTN	
H2	2R0A0-V1	6- 91	2B0A0-RY	CHL 3 SELECT EXT INTERRUPT	
H3	2R0B1-V1	6- 97	2B0B1-RY	CHL 6 SELECT EXT INTERRUPT	
I0	2R1A9-R0	6- 23		NOT FO = BIT 17	
I1	2R1A9-R1	6- 23			
I2	2R0B0-V1	6- 99	2B0B0-RY	CHL 7 SELECT EXT INTERRUPT	
I3	2R0B7-N0	6-113		SEL SET INTERRUPT MASK=FAN OUT	
J0	2A1A06P04C-03			FO REGISTER BIT 17	
	1A4A06J10C-03				
	1R0A2-W1	2- 31			
J1	2A1A06P04C-04				
	1A4A06J10C-04				
	1R0A2-W0	2- 31			
J2	2R0A4-O2	6-103		CLEAR CHL INTERRUPT TO 0/1/4/5	
J3	2R0B4-O2	6-105		CLEAR CHL INTERRUPT TO 2/3/6/7	
K0	2R0B4-P2	6-105		CLEAR CHANNEL TO 2/3/6/7	
K1	2R0A4-P2	6-103		CLEAR CHANNEL TO 0/1/4/5	
K2	2R0A7-M0	6-117	2B0A7-AK	SET BCD FAULT	
K3	2R0A8-D2	6-109		NOT (F=XXX1) TO 77,5/77.6 XLTN	
L0	2R0A4-S1	6-103		SET INTERRUPT LOCKOUT= 0/1/4/5	
L1	2R0A7-I2	6-117	2B0A7-RF	NOT(SEL INTERNAL STAT FAN=IN)	
L2	2A1A7-P0	6- 51		F BIT 12 TO STATUS COMPARE	
L3	2A1A7-P1	6- 51			
M0	2R0A7-T1	6-117		FO(BITS 00-07)NOT EQUAL ZERO	
M1	2R0B4-S1	6-105		SET INTERRUPT LOCKOUT= 2/3/6/7	
M2	2A1A7-O0	6- 51		F BIT 13 TO STATUS COMPARE	
M3	2A1A7-O1	6- 51			
N0	2R0B4-M2	6-105		CLEAR CHANNEL ACTIVITY=2/3/6/7	
N1	2R0A4-M2	6-103		CLEAR CHANNEL ACTIVITY=0/1/4/5	
N2	2R1B9-Q0	6- 27		SET TYPE IN TO TWR CONTROL	
N3	2R1B9-Q1	6- 27			
O0	2R1B9-W2	6- 27		CLEAR TYPEWRITER CONTROLS	
O1	2R1B9-W3	6- 27			
O2	2R1B9-P1	6- 27			
O3	2R1B9-P0	6- 27		SET TYPE OUT TO TWR CONTROL	
P0	2R0B6-A3	6-111		F BIT 08 TO STATUS TEST XLTN	
P1	2R0A7-D3	6-117	2B0A7-RD	NOT(CLEAR S/M INTERRUPT)	
P2	2A1A7-O2	6- 51		F BIT 14 TO STATUS COMPARE	
P3	2A1A7-O3	6- 51			
Q0	2R0A7-G0	6-117		CLEAR XLTN OR F REG BIT 09	
Q1	2R0A7-F0	6-117		CLEAR XLTN OR F REG BIT 08	
Q2	2R1B8-L3	6- 11		FCN CODE = 77 AND STABLE	
Q3	2R1B8-L2	6- 11			
R0	2R0A7-R1	6-117		CLEAR XLTN OR F REG BIT 11	
R1	2R0B8-O2	6-111		F BIT 11 TO STATUS TEST XLTN	
R2	2A1A06J15C-10				
	2A1A06J25A-02			EXT INTERRUPT = ASSOC PROC	
R3	2A1A06J15C-09				
	2A1A06J25A-01				
S0	2R0A7-O1	6-117		CLEAR XLTN OR F REG BIT 10	
S1	2R0A6-C1	6-121		ENABLE CLEAR TW REPEAT FF	
S2	2R0A8-V2	6-109		NOT(BLOCK LINE INTERRUPTS)	
S3	2R0A8-A0	6-109		SEL STATUS=F BIT 00+01+04+05	
T0	2R0A5-C1	6-123		ENABLE CLEAR TW FINISH FF	
T1	2R0A8-J2	6-109		MC + INT CLR + POWER ON CLR	
T2	2R0A7-V1	6-117		SEL STATUS=F BIT 08+09+10+11	
T3	2R0A7-N2	6-117		SEL STATUS=F BIT 02+03+06+07	
U0	2R0B8-U2	6-111		F BIT 10 TO STATUS TEST XLTN	
U1	2R0B8-R2	6-111		F BIT 09 TO STATUS TEST XLTN	
U2	2R1B8-V1	6- 11			
U3	2R1B8-V0	6- 11		STOP CLOCK ON PRIORITY PAUSE	
V0	2R1A6-G2	6- 13		CLEAR SEARCH/MOVE CONTROLS	
V1	2R1A6-G3	6- 13			
V2	2R0A8-J3	6-109		NOT(CLEAR ILLEGAL WRITE EN,)	
V3	2R0A7-D2	6-117		CLEAR INTERNAL FAULTS SENSED	
W0	2A1A06P05E-09			BC NOT COMPARE FF	
	1A4A06J14E-09				
	1R0B8-P3	2- 11			
W1	2A1A06P05E-10				
	1A4A06J14E-10				
	1R0B8-P2	2- 11		SEL CLR INTERRUPT MASK=FAN OUT	
W2	2R0B6-N0	6-115		CLEAR INTERNAL INTERRUPT/FAULT	
W3	2R0A7-P0	6-117		TEST CLEAR TO INTERNAL FAULTS	
X0	2R1B1-C3	6- 9			
X1	2R1B1-C2	6- 9			
X2	2A1A06P05E-05			SEL STATUS = ANY BIT OF F L12	
	1A4A06J14E-05				
	1R0B8-K0	2- 11			
X3	2A1A06P05E-06				
	1A4A06J14E-06				
	1R0B8-K1	2- 11			

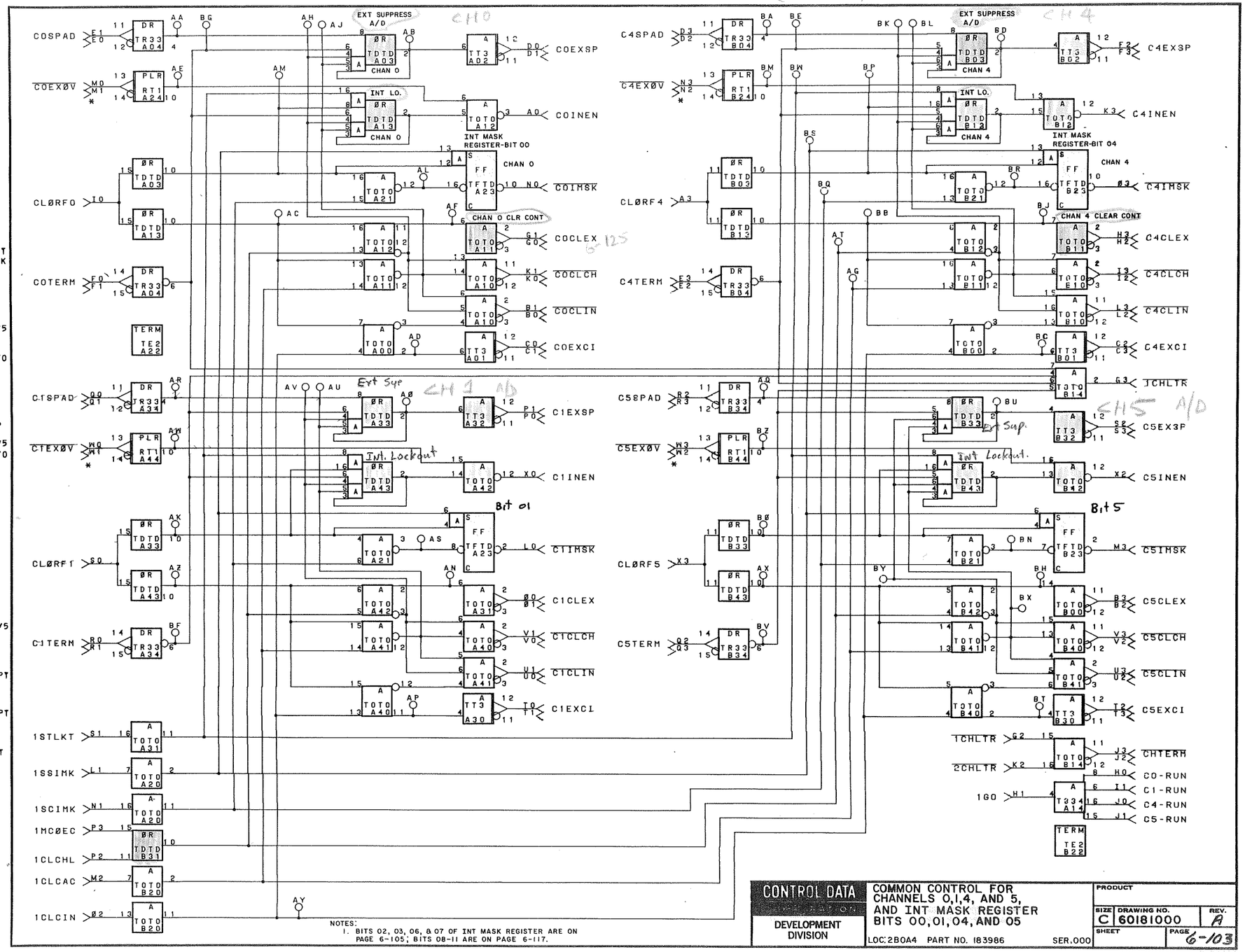


287

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2R0A3-I1	6- 85	2B0A3-AJ	CHL 0 INTERRUPT ENABLE
A3	2R0A8-L1	6-109		CLEAR XLTN OR F REG BIT 04
B0	2A0B7-X2	6-125		NOT CHAN 0 CLR CHAN INTERRUPT
B1	2A0B7-X3	6-125		
B2	2C0A6-E0	6-163		
B3	2C0A6-E1	6-163		CHL 5 CLEAR CHL AND EXT EQUIP
C0	2A4A05J03E-07			CHL 0 EXTERNAL CLEAR INTERRUPT
	2A4A05J04E-07			
C1	2A4A05J03E-08			
	2A4A05J04E-08			
C2	2A4A07J03E-07			CHL 4 EXTERNAL CLEAR INTERRUPT
	2A4A07J04E-07			
C3	2A4A07J03E-08			
	2A4A07J04E-08			
D0	2A4A05J03C-09			CHL 0 EXTERNAL SUPPRESS A/D
	2A4A05J04C-09			
D1	2A4A05J03C-10			
	2A4A05J04C-10			
D2	2R1B5-H1	6- 21		
D3	2R1B5-H0	6- 21		ACT, CHAN 4 SUPPR EXT A/D
E0	2R1A5-H1	6- 19		
E1	2R1A5-H0	6- 19		ACT, CHAN 0 SUPPRESS EXT A/D
E2	2C0A7-Q3	6-161		
E3	2C0A7-Q2	6-161		CHL 4 TERMINATE TO COMMON B
F0	2A0B7-Q2	6-125		CHL 0 TERMINATE TO COMMON B
F1	2A0B7-Q3	6-125		
F2	2A4A07J03C-09			CHL 4 EXTERNAL SUPPRESS A/D
	2A4A07J04C-09			
F3	2A4A07J03C-10			
	2A4A07J04C-10			
G0	2A0B7-E0	6-125		
G1	2A0B7-E1	6-125		CHL 0 CLEAR CHL AND EXT EQUIP

G2	2B0A4-G3	6-103		NOT(CHAN 0-3 TERMINATE) TO FAN-IN
G3	2B0A4-G2	6-103		NOT(CHAN 0-3 TERMINATE) TO FAN-IN
H0	2B0A3-F3	6- 85	2B0A3-RL	CHAN 0 CMPTR RUNNING TO XMTR
H1	2R0A5-R0	6-123		COMPUTER RUNNING TO FAN OUT
H2	2C0A7-E0	6-161		
H3	2C0A7-E1	6-161		CHL 4 CLEAR CHL AND EXT EQUIP
I0	2R0A8-A3	6-109		CLEAR XLTN OR F REG BIT 00
I1	2R0A2-F3	6- 87	2B0A2-RL	CHAN 1 CMPTR RUNNING TO XMTR
I2	2C0A7-K0	6-161		NOT CHL 4 CLR CHL ACTIVITY
I3	2C0A7-K1	6-161		
J0	2B0B3-F3	6- 93	2B0B3-RL	CHAN 4 CMPTR RUNNING TO XMTR
J1	2B0B2-F3	6- 95	2B0B2-RL	CHAN 5 CMPTR RUNNING TO XMTR
J2	2A1A06P06C-03 1A4A06J18C-03 1C0B2-T0	2- 51		NOT CHAN 0-7 TERMINATE TO BC
J3	2A1A06P06C-04 1A4A06J18C-04 1C0B2-T1	2- 51		
K0	2A0B7-K0	6-125		NOT CHAN 0 CLR CHAN ACTIVITY
K1	2A0B7-K1	6-125		
K2	2R0B4-G3	6-105		NOT(CHAN 4-7 TERMINATE) TO FAN-IN
K3	2R0B3-I1	6- 93	2B0B3-AJ	CHL 4 INTERRUPT ENABLE
L0	2B0A2-V0	6- 87	2B0A2-AZ	NOT(CHAN 1 INT MASK) TO FANOUT
L1	2B0B7-H0	6-113		SEL SET 0/1/4/5 INTERRUPT MASK
L2	2C0A7-X2	6-161		NOT CHL 4 CLR CHL INTERRUPT
L3	2C0A7-X3	6-161		
M0	2A4A05J03E-10 2A4A05J04E-10			
M1	2A4A05J03E-09 2A4A05J04E-09			NOT CHAN 0 EXT INTERRUPT LOCKOUT OVERRIDE
M2	2R0A9-N1	6-101		CLEAR CHANNEL ACTIVITY=0/1/4/5
M3	2B0B2-V0	6- 95	2B0B2-AZ	NOT (CHAN 5 INT MASK) TO FANOUT
N0	2B0A3-V0	6- 85	2B0A3-AZ	NOT (CHAN 0 INTERRUPT MASK) TO FANOUT
N1	2B0B6-H0	6-115		SEL CLR 0,1,4,5 OF INT MASK
N2	2A4A07J03E-09 2A4A07J04E-09			NOT CHAN 4 EXT INTERRUPT LOCKOUT OVERRIDE
N3	2A4A07J03E-10 2A4A07J04E-10			
O0	2A0B6-E1	6-127		CHL 1 CLEAR CHL AND EXT EQUIP
O1	2A0B6-E0	6-127		
O2	2B0A9-J2	6-101		CLEAR CHL INTERRUPT TO 0/1/4/5
O3	2B0B3-V0	6- 93	2B0B3-AZ	NOT (CHAN 4 INTERRUPT MASK) TO FANOUT
P0	2A4A05J01C-10 2A4A05J02C-10			
P1	2A4A05J01C-09 2A4A05J02C-09			CHL 1 EXTERNAL SUPPRESS A/D
P2	2B0A9-K1	6-101		CLEAR CHANNEL TO 0/1/4/5
P3	2B0A7-K2	6-117		CLR XLTN TO CHAN 0;1,4,5 FANOUT
Q0	2B1A5-G1	6- 19		ACT, CHAN 1 SUPPRESS EXT A/D
Q1	2B1A5-G0	6- 19		
Q2	2C0A6-Q2	6-163		CHL 5 TERMINATE TO COMMON B
Q3	2C0A6-Q3	6-163		
R0	2A0B6-Q2	6-127		CHL 1 TERMINATE TO COMMON B
R1	2A0B6-Q3	6-127		
R2	2B1B5-G1	6- 21		ACT, CHAN 5 SUPPR EXT A/D
R3	2B1B5-G0	6- 21		
S0	2R0A8-J1	6-109		CLEAR XLTN OR F REG BIT 01
S1	2B0A9-L0	6-101		SET INTERRUPT LOCKOUT= 0/1/4/5
S2	2A4A07J01C-09 2A4A07J02C-09			CHL 5 EXTERNAL SUPPRESS A/D
S3	2A4A07J01C-10 2A4A07J02C-10			
T0	2A4A05J01E-07 2A4A05J02E-07			CHL 1 EXTERNAL CLEAR INTERRUPT
T1	2A4A05J01E-08 2A4A05J02E-08			
T2	2A4A07J01E-07 2A4A07J02E-07			CHL 5 EXTERNAL CLEAR INTERRUPT
T3	2A4A07J01E-08 2A4A07J02E-08			
U0	2A0B6-X2	6-127		NOT CHAN 1 CLR CHAN INTERRUPT
U1	2A0B6-X3	6-127		
U2	2C0A6-X2	6-163		NOT CHL 5 CLR CHL INTERRUPT
U3	2C0A6-X3	6-163		
V0	2A0B6-K0	6-127		NOT CHAN 1 CLR CHAN ACTIVITY
V1	2A0B6-K1	6-127		
V2	2C0A6-K0	6-163		NOT CHL 5 CLR CHL ACTIVITY
V3	2C0A6-K1	6-163		
W0	2A4A05J01E-10 2A4A05J02E-10			
W1	2A4A05J01E-09 2A4A05J02E-09			NOT CHAN 1 EXT INTERRUPT LOCKOUT OVERRIDE
W2	2A4A07J01E-09 2A4A07J02E-09			NOT CHAN 5 EXT INTERRUPT LOCKOUT OVERRIDE
W3	2A4A07J01F-10 2A4A07J02F-10			
X0	2R0A2-I1	6- 87	2B0A2-AJ	CHL 1 INTERRUPT ENABLE
X2	2R0B2-I1	6- 95	2B0B2-AJ	CHL 5 INTERRUPT ENABLE
X3	2R0A8-J0	6-109		CLEAR XLTN OR F REG BIT 05

1 MR. Paged(6-105)&(117)



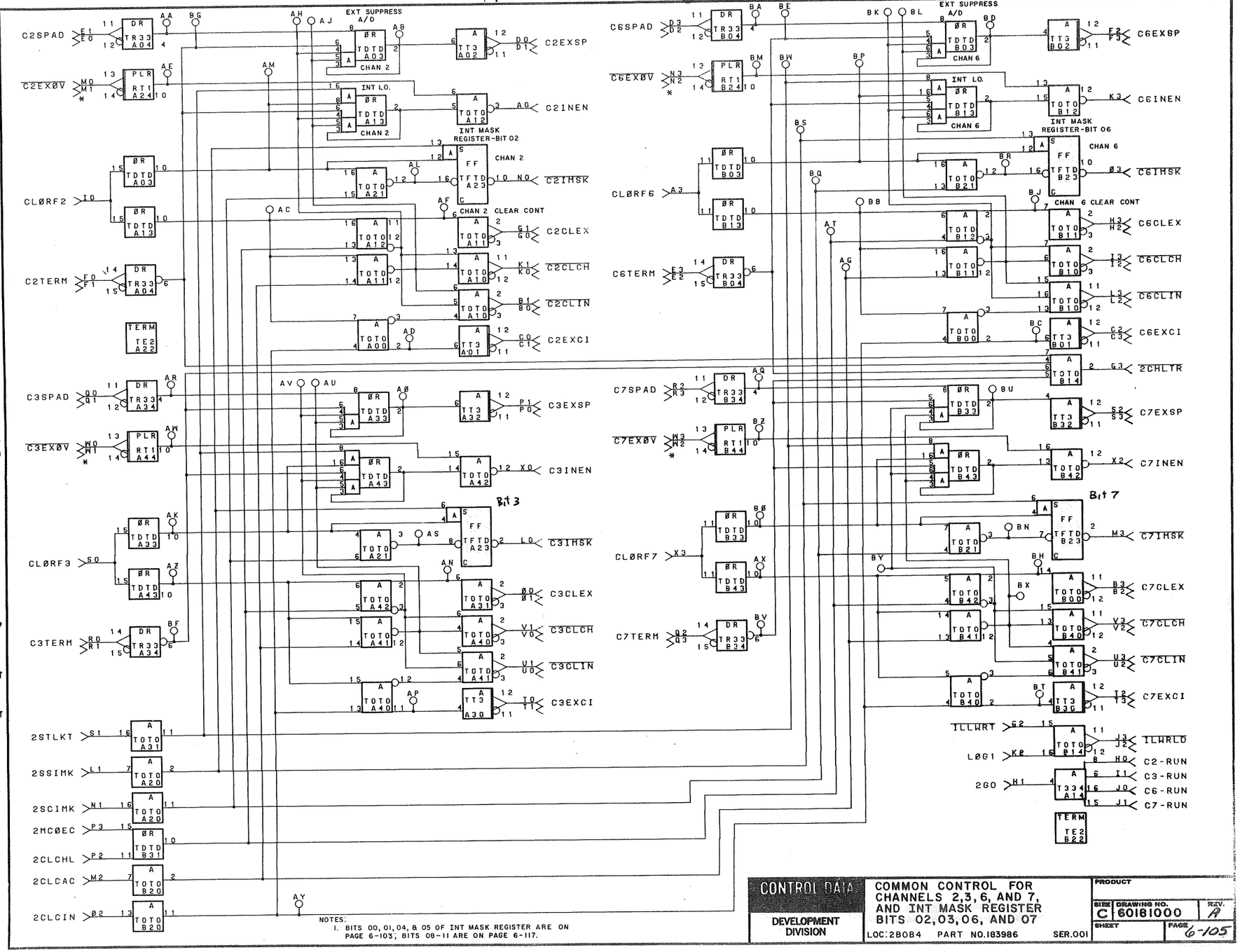
NOTES:
1. BITS 02, 03, 06, & 07 OF INT MASK REGISTER ARE ON PAGE 6-105; BITS 08-11 ARE ON PAGE 6-117.

CONTROL DATA DEVELOPMENT DIVISION	COMMON CONTROL FOR CHANNELS 0,1,4, AND 5, AND INT MASK REGISTER BITS 00,01,04, AND 05	PRODUCT	
	LOC:2B0A4 PART NO. 183986 SER.000	SIZE C / DRAWING NO. 60181000 / REV. A	
		SHEET / PAGE 6-103	

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2R0A1-I1	6- 89	2B0A1-AJ	CHL 2 INTERRUPT ENABLE
A3	2R0A7-N3	6-117		CLEAR XLTN OR F REG BIT 06
B0	2A0B3-X2	6-129		NOT CHAN 2 CLR CHAN INTERRUPT
B1	2A0B3-X3	6-129		
B2	2C0A2-E0	6-167		
B3	2C0A2-E1	6-167		CHL 7 CLEAR CHL AND EXT EQUIP
C0	2A4A06J03E-07			CHL 2 EXTERNAL CLEAR INTERRUPT
	2A4A06J04E-07			
C1	2A4A06J03E-08			
	2A4A06J04E-08			
C2	2A4A08J03E-07			CHL 6 EXTERNAL CLEAR INTERRUPT
	2A4A08J04F-07			
C3	2A4A08J03F-08			
	2A4A08J04E-08			
D0	2A4A06J03C-09			CHL 2 EXTERNAL SUPPRESS A/D
	2A4A06J04C-09			
D1	2A4A06J03C-10			
	2A4A06J04C-10			
D2	2R1B5-F0	6- 21		
D3	2R1B5-F1	6- 21		ACT, CHAN 6 SUPPR EXT A/D
E0	2R1A5-F0	6- 19		
E1	2R1A5-F1	6- 19		ACT, CHAN 2 SUPPRESS EXT A/D
E2	2C0A3-03	6-165		
E3	2C0A3-02	6-165		CHL 6 TERMINATE TO COMMON B

INT. Mask Reg Bit 8 - 9 - 10 - 11 on Page 6-1178 (6-103)

F0	2A0R3-Q2	6-129		CHL 2 TERMINATE TO COMMON B
F1	2A0R3-Q3	6-129		
F2	2A4A08J03C-09			CHL 6 EXTERNAL SUPPRESS A/D
	2A4A08J04C-09			
F3	2A4A08J03C-10			
	2A4A08J04C-10			
G0	2A0R3-E0	6-129		
G1	2A0R3-E1	6-129		CHL 2 CLEAR CHL AND EXT EQUIP
G2	2R0A8*I2	6-109		NOT(ILL. WRITE)TO LOAD XMTR
G3	2R0A4-K2	6-103		NOT(CHAN 4-7 TERMINATE) TO FAN-IN
H0	2R0A1-F3	6- 89	2B0A1-RL	CHAN 2 CMPTR RUNNING TO XMTR
H1	2R0A5-S0	6-123		COMPUTER RUNNING TO FAN OUT
H2	2C0A3-E0	6-165		
H3	2C0A3-E1	6-165		CHL 6 CLEAR CHL AND EXT EQUIP
I0	2R0A7-M2	6-117		CLEAR XLTN OR F REG BIT 02
I1	2R0A0-F3	6- 91	2B0A0-RL	CHAN 3 CMPTR RUNNING TO XMTR
I2	2C0A3-K0	6-165		NOT CHL 6 CLR CHL ACTIVITY
I3	2C0A3-K1	6-165		
J0	2R0B1-F3	6- 97	2B0B1-RL	CHAN 6 CMPTR RUNNING TO XMTR
J1	2R0B0-F3	6- 99	2B0B0-RL	CHAN 7 CMPTR RUNNING TO XMTR
J2	2R2R2-R1	5- 89		NOT ILLEGAL WRITE TO LIGHT DR
J3	2R2R2-R0	5- 89		
K0	2A0B3*K0	6-129		NOT CHAN 2 CLR CHAN ACTIVITY
K1	2A0B3-K1	6-129		
K3	2R0R1-I1	6- 97	2B0B1-AJ	CHL 6 INTERRUPT ENABLE
L0	2R0A0-V0	6- 91	2B0A0-AZ	NOT(CHAN 3 INT MASK)TO FAN-OUT
L1	2R0B7-O0	6-113		SEL SET 2,3,6,AND 7 INT MASK
L2	2C0A3-X2	6-165		NOT CHL 6 CLR CHL INTERRUPT
L3	2C0A3-X3	6-165		
M0	2A4A06J03E-10			
	2A4A06J04E-10			
M1	2A4A06J03E-09			NOT CHAN 2 EXT INTERRUPT LOCKOUT OVERRIDE
	2A4A06J04E-09			
M2	2R0A9-N0	6-101		CLEAR CHANNEL ACTIVITY-2/3/6/7
M3	2R0B0-V0	6- 99	2B0B0-AZ	NOT (CHAN 7 INTERRUPT MASK) TO FANOUT
N0	2R0A1-V0	6- 89	2B0A1-AZ	NOT(CHAN 2 INT MASK)TO FANOUT
N1	2R0B6-O0	6-115		SEL CLR 2,3,6,7 OF INT MASK
N2	2A4A08J03E-09			NOT CHAN 6 EXT INTERRUPT
	2A4A08J04E-09			LOCKOUT OVERRIDE
N3	2A4A08J03E-10			
	2A4A08J04E-10			
O0	2A0B2-E1	6-131		CHL 3 CLEAR CHL AND EXT EQUIP
O1	2A0B2-E0	6-131		
O2	2R0A9-J3	6-101		CLEAR CHL INTERRUPT TO 2/3/6/7
O3	2R0B1-V0	6- 97	2B0B1-AZ	NOT (CHAN 6 INTERRUPT MASK) TO FANOUT
P0	2A4A06J01C-10			
	2A4A06J02C-10			CHL 3 EXTERNAL SUPPRESS A/D
P1	2A4A06J01C-09			
	2A4A06J02C-09			
P2	2R0A9-K0	6-101		CLEAR CHANNEL TO 2/3/6/7
P3	2R0A7-L2	6-117		CLR XLTN TO CHAN 2,3,6, AND 7 FANOUT
Q0	2R1A5-I0	6- 19		ACT, CHAN 3 SUPPRESS EXT A/D
Q1	2R1A5-I1	6- 19		
Q2	2C0A2-Q2	6-167		CHL 7 TERMINATE TO COMMON B
Q3	2C0A2-Q3	6-167		
R0	2A0B2-Q2	6-131		CHL 3 TERMINATE TO COMMON B
R1	2A0B2-Q3	6-131		
R2	2R1B5-I0	6- 21		ACT, CHAN 7 SUPPR EXT A/D
R3	2R1B5-I1	6- 21		
S0	2R0A7-J2	6-117		CLEAR XLTN OR F REG BIT 03
S1	2R0A9-M1	6-101		SET INTERRUPT LOCKOUT- 2/3/6/7
S2	2A4A08J01C-09			CHL 7 EXTERNAL SUPPRESS A/D
	2A4A08J02C-09			
S3	2A4A08J01C-10			
	2A4A08J02C-10			
T0	2A4A06J01E-07			CHL 3 EXTERNAL CLEAR INTERRUPT
	2A4A06J02E-07			
T1	2A4A06J01E-08			
	2A4A06J02E-08			
T2	2A4A08J01E-07			CHL 7 EXTERNAL CLEAR INTERRUPT
	2A4A08J02E-07			
T3	2A4A08J01E-08			
	2A4A08J02E-08			
U0	2A0B2-X2	6-131		NOT CHAN 3 CLR CHAN INTERRUPT
U1	2A0B2-X3	6-131		
U2	2C0A2-X2	6-167		NOT CHL 7 CLR CHL INTERRUPT
U3	2C0A2-X3	6-167		
V0	2A0B2-K0	6-131		NOT CHAN 3 CLR CHAN ACTIVITY
V1	2A0B2-K1	6-131		
V2	2C0A2-K0	6-167		NOT CHL 7 CLR CHL ACTIVITY
V3	2C0A2-K1	6-167		
W0	2A4A06J01E-10			
	2A4A06J02E-10			NOT CHAN 3 EXT INTERRUPT LOCKOUT OVERRIDE
W1	2A4A06J01E-09			
	2A4A06J02E-09			NOT CHAN 7 EXT INTERRUPT
W2	2A4A08J01E-09			LOCKOUT OVERRIDE
	2A4A08J02E-09			
W3	2A4A08J01E-10			
	2A4A08J02E-10			
X0	2R0A0-I1	6- 91	2B0A0-AJ	CHL 3 INTERRUPT ENABLE
X2	2R0B0-I1	6- 99	2B0B0-AJ	CHL 7 INTERRUPT ENABLE
X3	2R0A7-M3	6-117		CLEAR XLTN OR F REG BIT 07



NOTES:
1. BITS 00, 01, 04, & 05 OF INT MASK REGISTER ARE ON PAGE 6-103; BITS 08-11 ARE ON PAGE 6-117.

CONTROL DATA
DEVELOPMENT DIVISION

COMMON CONTROL FOR CHANNELS 2,3,6, AND 7, AND INT MASK REGISTER BITS 02,03,06, AND 07

LOC:2B0B4 PART NO.183986 SER.001

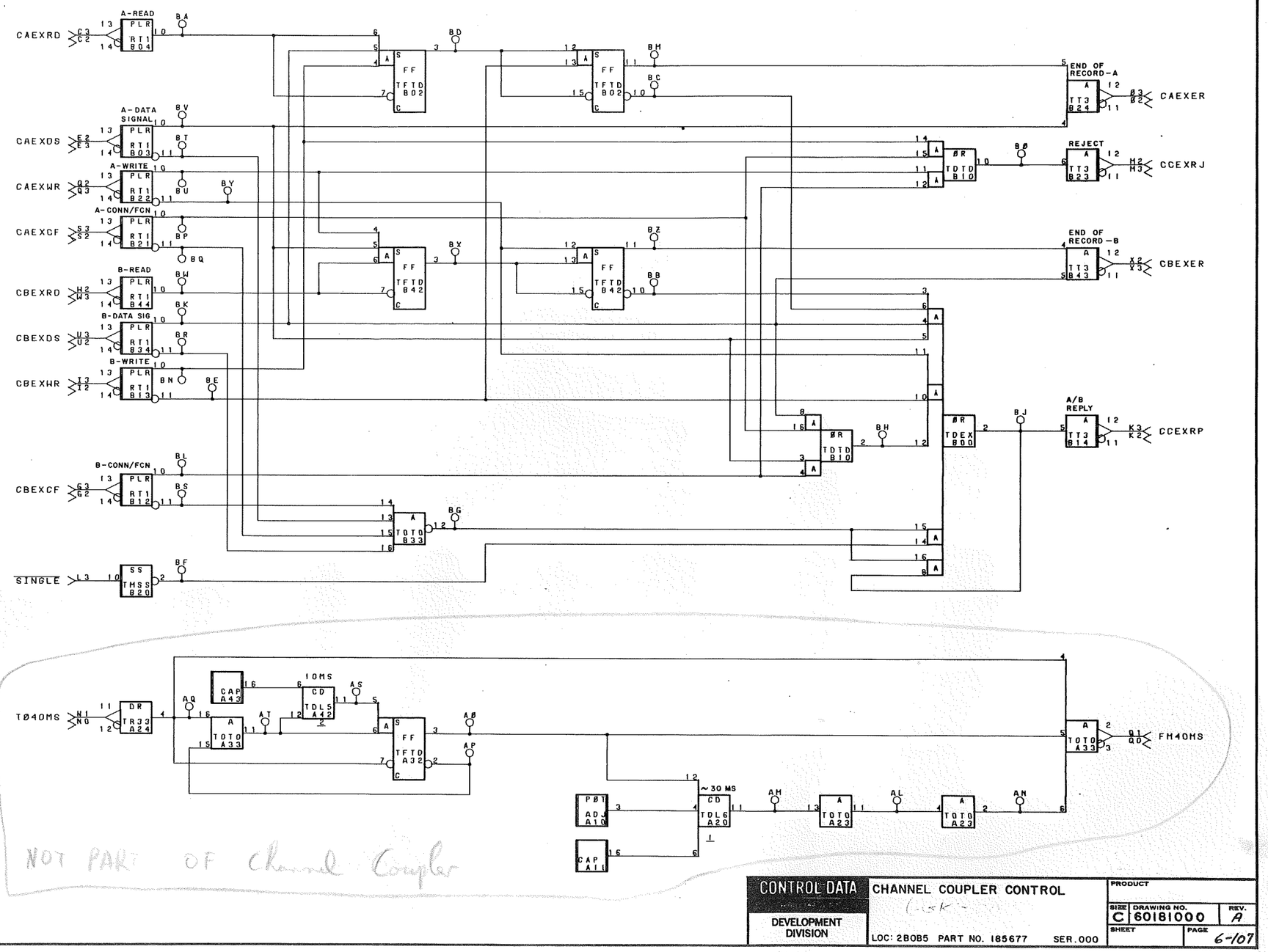
PRODUCT

SIZE	DRAWING NO.	REV.
C	60181000	A

SHEET PAGE 6-105

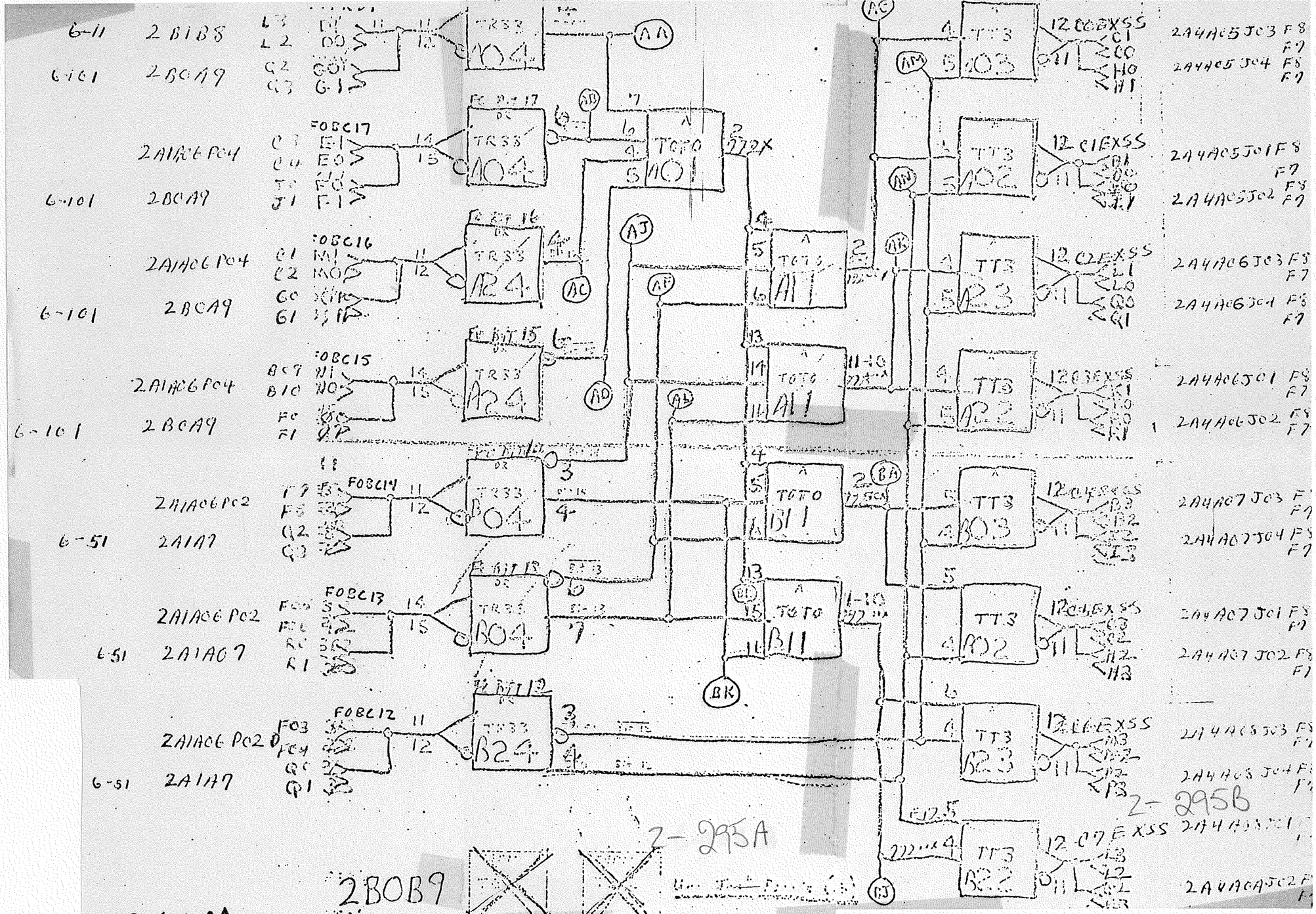
291

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
C2	2A4A13J01D-02			
	2A4A13J02C-10			
C3	2A4A13J01D-01			EXTERNAL READ - A CABLE
	2A4A13J02C-09			
E2	2A4A13J01D-09			EXTERNAL DATA SIGNAL - A CABLE
	2A4A13J02F-05			
E3	2A4A13J01D-10			
	2A4A13J02F-06			
G2	2A4A13J02D-06			
	2A4A13J02D-08			
G3	2A4A13J02D-05			EXTERNAL CONN/FCN - B CABLE
	2A4A13J02D-07			
I2	2A4A13J01E-10			
	2A4A13J02D-04			
I3	2A4A13J01E-09			EXTERNAL WRITE - CABLE B
	2A4A13J02D-03			
K2	2A4A13J01E-02			
	2A4A13J02E-02			
K3	2A4A13J01E-01			EXTERNAL REPLY - CABLE C
	2A4A13J02E-01			
L3	2A2A04J02L-03			NOT SINGLE CHANNEL
M2	2A4A13J01E-03			EXTERNAL REJECT - CABLE C
	2A4A13J02E-03			
M3	2A4A13J01E-04			
	2A4A13J02E-04			
N0	2A1A06P05D-02			
	1A4A06J14D-02			
	1B0B8-Q2	2- 11		
N1	2A1A06P05D-01			PAUSE FF TO 40 MS, DELAY
	1A4A06J14D-01			
	1B0B8-Q3	2- 11		
O2	2A4A13J01E-06			
	2A4A13J02F-08			
O3	2A4A13J01E-05			EXTERNAL EOR - CABLE A
	2A4A13J02F-07			
Q0	2A1A06P05F-02			
	1A4A06J14F-02			
	1B0B8-D3	2- 11		
Q1	2A1A06P05F-01			FROM 40 MS DELAY
	1A4A06J14F-01			
	1B0B8-D2	2- 11		
Q2	2A4A13J01D-03			EXTERNAL WRITE - A CABLE
	2A4A13J02E-09			
Q3	2A4A13J01D-04			
	2A4A13J02E-10			
S2	2A4A13J01D-08			
	2A4A13J01D-06			
S3	2A4A13J01D-07			EXTERNAL CONN/FCN - A CABLE
	2A4A13J01D-05			
U2	2A4A13J01F-06			
	2A4A13J02D-10			
U3	2A4A13J01F-05			EXTERNAL DATA SIGNAL - B CABLE
	2A4A13J02D-09			
W2	2A4A13J01C-09			EXTERNAL READ - B CABLE
	2A4A13J02D-01			
W3	2A4A13J01C-10			
	2A4A13J02D-02			
X2	2A4A13J01F-07			EXTERNAL EOR - CABLE B
	2A4A13J02E-05			
X3	2A4A13J01F-08			
	2A4A13J02E-06			



PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B0A9-S3	6-101		SEL STATUS=F BIT 00+01+04+05
A3	2B0A4-J0	6-103		CLEAR XLTN OR F REG BIT 00
B0	2B0A7-L3	6-117		CLR XLTN TO OR WITH F 01,04,05
B1	2B0A7-G1	6-117		F REG BITS (00)(01)(04)(05)=0
B2	2B1B8-I2	6- 11		
B3	2B1B8-I3	6- 11		FCN CODE=XX51 TO CLR CHAN XLTN
C0	2A1A5-01	6- 47		
C1	2A1A5-00	6- 47		F BIT 05 TO STATUS COMPARE
C2	2A1A06P03D-09			(NORMAL INTERRUPTS)(ARITH)
	1A4A06J20D-09			
	1C0A1-K0	2- 43		
C3	2A1A06P03D-10			
	1A4A06J20D-10			
	1C0A1-K1	2- 43		
D0	2A1B5-G0	6- 45		
D1	2A1B5-G1	6- 45		F BIT 00 TO STATUS COMPARE
D2	2B0A9-K3	6-101		NOT (F=XXX1) TO 77,5777,6 XLTN
D3	2B0B6-V0	6-115	2B0B6-AW	NOT(ARITH INTERRUPT PRIORITY)
E0	2A1B5-L0	6- 45		
E1	2A1B5-L1	6- 45		F BIT 01 TO STATUS COMPARE
E2	2B1B7-W0	6- 3		(NORMAL INTERRUPTS)(NOT ARITH)
E3	2B1B7-W1	6- 3		
F0	2A1A5-P0	6- 47		F BIT 04 TO STATUS COMPARE
F1	2A1A5-P1	6- 47		
F2	2B0A9-H1	6-101		NOT (F=XX5) TO 77,51 XLTN

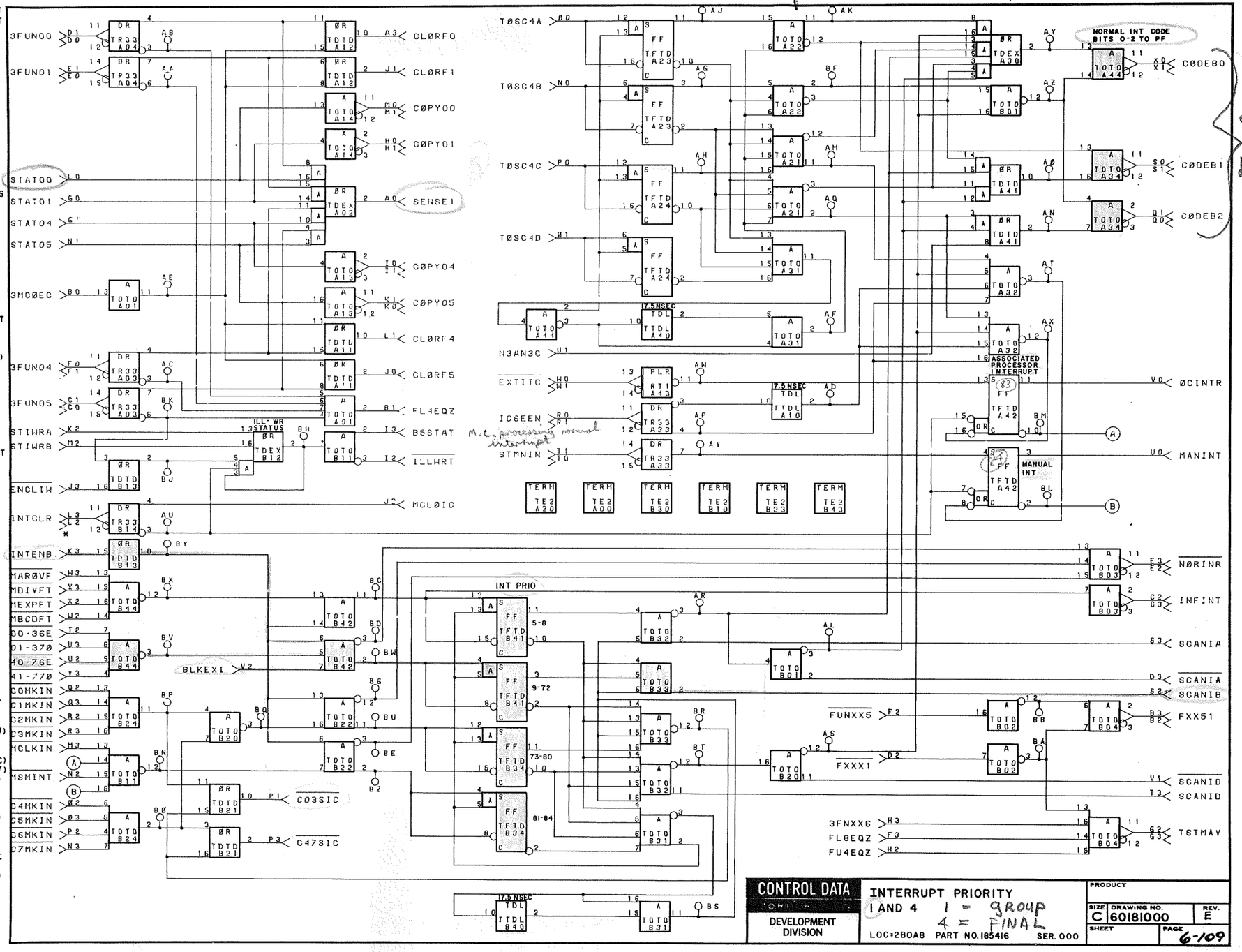
Ref Manual Interrupt Codes on Page 4-7


6-11
2 B1B8
6-101
2BCA9
2A1AC6P04
2A1AC6P02
2A1AC6P03
2A1AC6P01
2A1AC7P03
2A1AC7P02
2A1AC7P01
2A1AC7P04
6-51
2A1A7
2BOB9
FOBC17
FOBC16
FOBC15
FOBC14
FOBC13
FOBC12
TRS3 A04
TRS3 A24
TRS3 B04
TRS3 B24
TOTO A01
TOTO A11
TOTO B11
TT3 A03
TT3 A02
TT3 A23
TT3 A22
TT3 B03
TT3 B02
TT3 B23
TT3 B22
12C0BXSS
12C1BXSS
12C2BXSS
12C3BXSS
2A4AC5J03 F8 F7
2A4AC5J04 F8 F7
2A4AC5J01 F8 F7
2A4AC5J02 F8 F7
2A4AC6J03 F8 F7
2A4AC6J04 F8 F7
2A4AC6J01 F8 F7
2A4AC6J02 F8 F7
2A4AC7J03 F8 F7
2A4AC7J04 F8 F7
2A4AC7J01 F8 F7
2A4AC7J02 F8 F7
2-295A
2-295B
SAMPLE STATUS (NEW CARD)

Pg 6-108A

Reference Manual Interrupt codes — Page 4-7

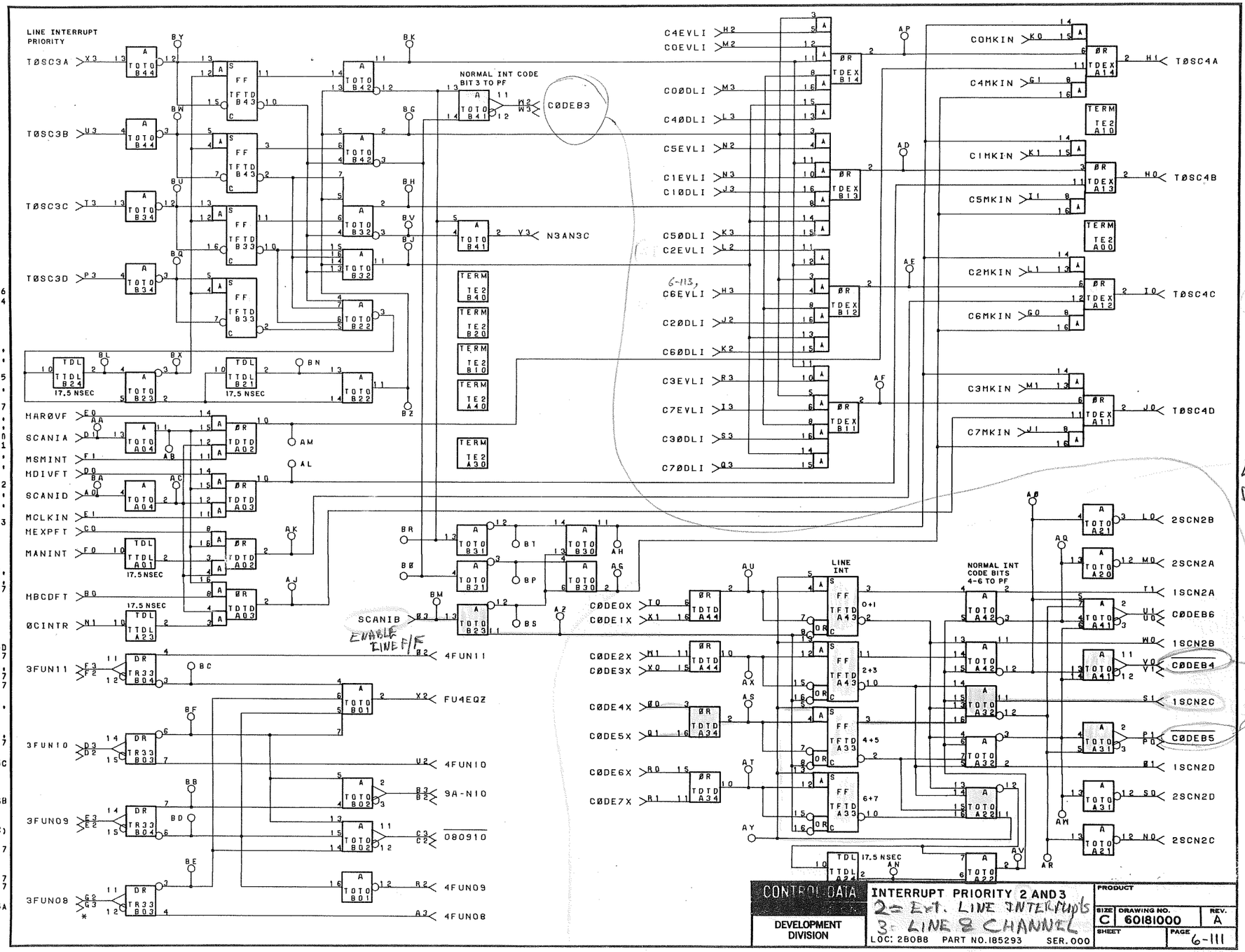
F3		2B^A7-N1	6-117	FQ(BITS 00-07) EQUAL ZERO
G0		2B^A5-R2	6-123	SELECTED STATUS BIT 01 TO TEST
G1		2B^A6-M3	6-121	SELECTED STATUS BIT 04 TO TEST
G2		2B1B8-D3	6- 11	TEST STORAGE AVAILABILITY
G3		2B1B8-D2	6- 11	
H0	2A1A06P02A-03			SELECTED STATUS BIT 01 TO D0
	1A4A06J06A-03			
		1A^A8-X1	2- 55	
H1	2A1A06P02A-04			
	1A4A06J06A-04			
		1A^A8-X0	2- 55	F BITS(08)(09)(10)(11)=ZERO
H2		2B^B8-X2	6-111	F=XX6 TO TEST STO AVAIL. XLTN
H3		2B^A9-D1	6-101	SELECTED STATUS BIT 04 TO D0
I0	2A1A06P02A-09			
	1A4A06J06A-09			
		1A^A6-X1	2- 57	
I1	2A1A06P02A-10			
	1A4A06J06A-10			
		1A^A6-X0	2- 57	NOT(ILL. WRITE)TO LOAD XMTR
I2		2B^B4-G2	6-105	ILL. WRITE TO BIT 05 OF STATUS
I3		2B^A5-S3	6-123	CLEAR XLTN OR F REG BIT 05
J0		2B^A4-X3	6-103	CLEAR XLTN OR F REG BIT 01
J1		2B^A4-S0	6-103	MC + INT CLR + POWER ON CLR
J2		2B^A9-T1	6-101	NOT(CLEAR ILLEGAL WRITE EN.)
J3		2B^A9-V2	6-101	
K0	2A1A06P02B-02			
	1A4A06J06B-02			
		1A^A6-Q1	2- 57	SELECTED STATUS BIT 05 TO D0
K1	2A1A06P02B-01			
	1A4A06J06B-01			
		1A^A6-Q0	2- 57	
K2		2B^B7-N3	6-113	SET ILL. WR FF FROM MN CONT
K3		2B^B6-M3	6-115	INTERRUPT SYSTEM ENABLE
L0		2B^A6-B2	6-121	SELECTED STATUS BIT 00 TO TEST
L1		2B^A4-A3	6-103	CLEAR XLTN OR F REG BIT 04
L2		2B1B1-E0	6- 9	
L3		2B1B1-E1	6- 9	NOT(INTERNAL CLR +MASTER CLR+ POWER ON MASTER CLR)
M0	2A1A06P02A-01			SELECTED STATUS BIT 00 TO D0
	1A4A06J06A-01			
		1A^A8-V1	2- 55	
M1	2A1A06P02A-02			
	1A4A06J06A-02			
		1A^A8-V0	2- 55	SET ILLEGAL WRITE F/F FROM RC
M2		2B^B7-M3	6-113	NOT(MASKED CLOCK INTERRUPT)
M3		2B^A7-S0	6-117	INPUT XLTN TO PRIORITY 4B
N0		2B^B8-H0	6-111	SELECTED STATUS BIT 05 TO TEST
N1		2B^A5-M3	6-123	NOT(MASKED S/M INTERRUPT)
N2		2B^A7-U0	6-117	NOT(CHL 7 MASKED INTERRUPT)
N3		2B^B0-Q2	6- 99	INPUT XLTN TO PRIORITY 4A
U0		2B^B8-H1	6-111	INPUT XLTN TO PRIORITY 4D
U1		2B^B8-J0	6-111	NOT(CHL 4 MASKED INTERRUPT)
U2		2B^B3-Q2	6- 93	NOT(CHL 5 MASKED INTERRUPT
U3		2B^B7-Q2	6- 95	INPUT XLTN TO PRIORITY 4C
P0		2B^B8-I0	6-111	NOT (CHAN 0-3 INTERRUPT PRIO)
P1		2B^B7-V0	6-113	2B0B7-AW
P2		2B^B1-Q2	6- 97	NOT(CHL 6 MASKED INTERRUPT)
P3		2B^B7-V2	6-113	2B0B7-BU NOT (CHAN 4-7 INTERRUPT PRIO)
Q0		2B2B9-00	5- 75	
Q1		2B2B9-01	5- 75	NORMAL INTERRUPT CODE BIT 02
Q2		2B^A3-Q2	6- 85	NOT(CHL 0 MASKED INTERRUPT)
Q3		2B^A2-Q2	6- 87	NOT(CHL 1 MASKED INTERRUPT)
R0	2A1A06P03D-07			NORMAL INTERRUPT CODE USED
	1A4A06J20D-07			
		1C^A1-C0	2- 43	
R1	2A1A06P03D-08			
	1A4A06J20D-08			
		1C^A1-C1	2- 43	
R2		2B^A1-Q2	6- 89	NOT(CHL 2 MASKED INTERRUPT)
R3		2B^A0-Q2	6- 91	NOT(CHL 3 MASKED INTERRUPT)
S0		2B2B9-W2	5- 75	NORMAL INTERRUPT CODE BIT 01
S1		2B2B9-W3	5- 75	
S2		2B^B8-03	6-111	2B0B8-BM EXT LINE INTERRUPT PRIORITY
S3		2B^B8-D1	6-111	ARITHMETIC INTERRUPT PRIORITY
T0		2B1A9-G1	6- 23	
T1		2B1A9-G0	6- 23	SET MANUAL INTERRUPT
T2		2B^B7-U1	6-113	NOT(FAN IN EVEN LINES CHL 0-3)
T3		2B^B8-A0	6-111	MISC. INTERRUPT PRIORITY
U0		2B^B8-F0	6-111	MANUAL INTERRUPT
U1		2B^B8-V3	6-111	NOT(PRIORITY 3A + PRIORITY 3C)
U2		2B^B7-U3	6-113	NOT(FAN IN EVEN LINES CHL 4-7)
U3		2B^B6-U1	6-115	NOT(FAN IN ODD LINES CHL 4-7)
V0		2B^B8-N1	6-111	ASSOC PROCESSOR INTERRUPT
V1		2B^B6-V2	6-115	2B0B6-BU NOT(MISC INTERRUPT PRIORITY)
V2		2B^A9-S2	6-101	NOT(BLOCK LINE INTERRUPTS)
V3		2B^B6-U3	6-115	NOT(FAN IN ODD LINES CHL 4-7)
W0	2A1A06J15D-01			
	2A1A06J26A-02			
W1	2A1A06J15D-02			EXT INTERRUPT = ASSOC PROC
	2A1A06J26A-01			EXT INTERRUPT FROM ASSOC PROC
W2		2B^A7-X1	6-117	NOT (MASKED BDP FAULT)
W3		2B^A7-P1	6-117	NOT (MASKED ARITH OVFL FAULT)
X0		2B2B9-P1	5- 75	NORMAL INTERRUPT CODE BIT 00
X1		2B2B9-P0	5- 75	
X2		2B^A7-W0	6-117	NOT(MASKED EXPONENT FAULT)
X3		2B^A7-Q0	6-117	NOT(MASKED DIVIDE FAULT)



CONTROL DATA	INTERRUPT PRIORITY 1 AND 4 1 = GROUP 4 = FINAL	PRODUCT	
DEVELOPMENT DIVISION	LOC:2B0A8 PART NO.185416 SER. 000	SIZE C	DRAWING NO. 60181000 REV. E
		SHEET	PAGE 6-109

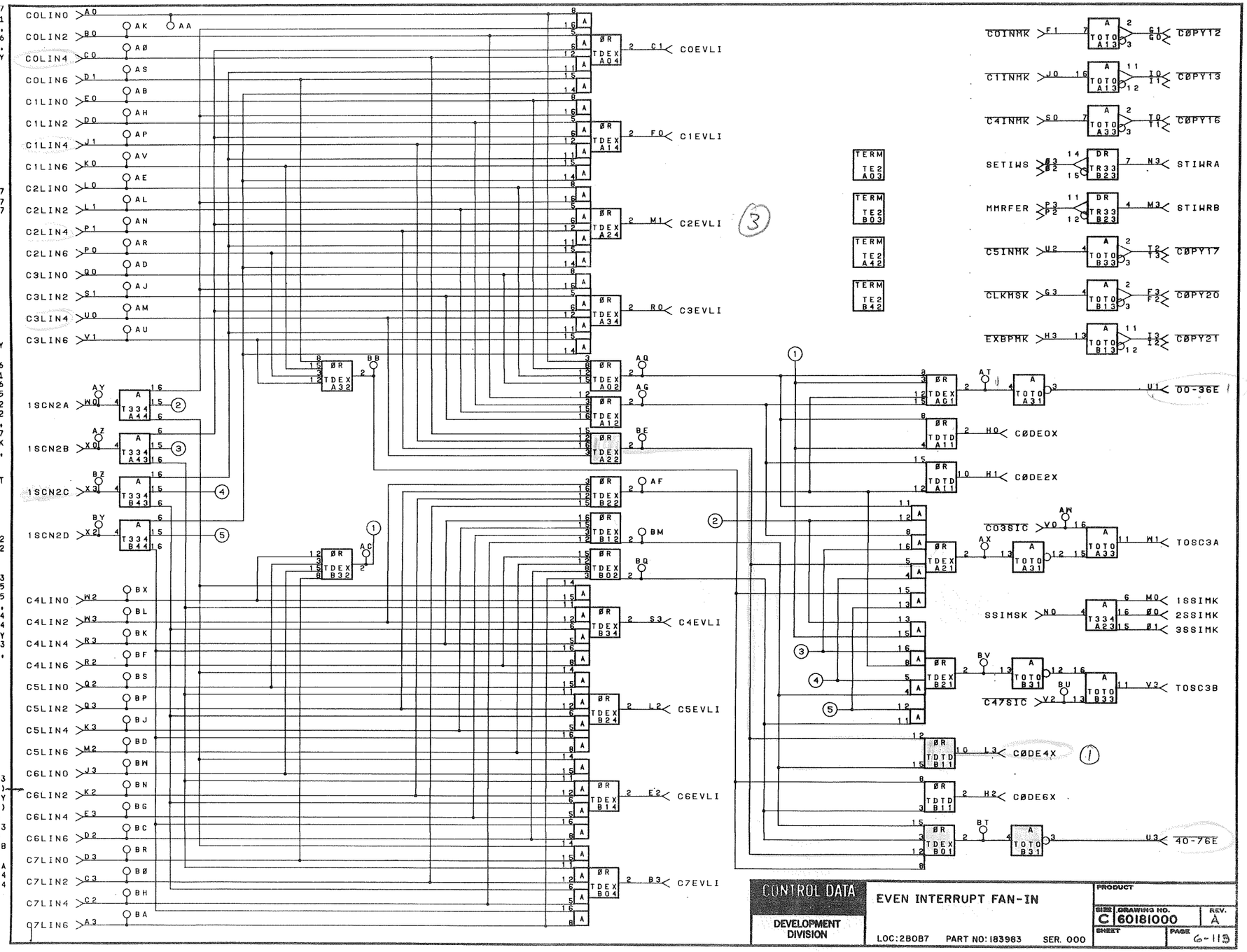
295

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B0A8-T3	6-109		MISC, INTERRUPT PRIORITY
A3	2B0A9-P0	6-101		F BIT 08 TO STATUS TEST XLTN
B0	2B0A7-X0	6-117		MASKED BDP FAULT
B2	2B1B8-J2	6- 11		
B3	2B1B8-J3	6- 11		(F BIT 09)(NOT F BIT 10)
C0	2B0A7-W1	6-117		MASKED EXPONENT FAULT
C2	2A1A06P05E-07			NOT F BIT 08 + 09 + 10 TO
	1A4A06J14E-07			MN CONT
	1B0B8-C3	2- 11		
C3	2A1A06P05E-08			
	1A4A06J14E-08			
	1B0B8-C2	2- 11		
D0	2B0A7-Q1	6-117		MASKED DIVIDE FAULT
D1	2B0A8-S3	6-109		ARITHMETIC INTERRUPT PRIORITY
D2	2A1A6-Q3	6- 49		
D3	2A1A6-Q2	6- 49		F BIT 10 TO STATUS COMPARE
E0	2B0A7-Q0	6-117		MASKED ARITH OVERFLOW FAULT
E1	2B0A7-R0	6-117		MASKED CLOCK INTERRUPT
E2	2A1A6-Q1	6- 49		
E3	2A1A6-Q0	6- 49		F BIT 09 TO STATUS COMPARE
F0	2B0A8-U0	6-109		MANUAL INTERRUPT
F1	2B0A7-T0	6-117		MASKED SEARCH/MOVE INTERRUPT
F2	2A1A6-N2	6- 49		
F3	2A1A6-N3	6- 49		F BIT 11 TO STATUS COMPARE
G0	2B0B1-Q3	6- 97		CHL 6 MASKED INTERRUPT - C#106
G1	2B0B3-Q3	6- 93		CHL 4 MASKED INTERRUPT - C#104
G2	2A1A6-P3	6- 49		F BIT 08 TO STATUS COMPARE
G3	2A1A6-P1	6- 49		
H0	2B0A8-N0	6-109		INPUT XLTN TO PRIORITY 4B
H1	2B0A8-O0	6-109		INPUT XLTN TO PRIORITY 4A
H2	2B0B7-S3	6-113		CHL 4 EVEN LINE INTERRUPT PRI,
H3	2B0B7-E2	6-113		CHL 6 EVEN LINE INTERRUPT PRI,
I0	2B0A8-P0	6-109		INPUT XLTN TO PRIORITY 4C
I1	2B0B2-Q3	6- 95		CHL 5 MASKED INTERRUPT - C#105
I3	2B0B7-B3	6-113		CHL 7 EVEN LINE INTERRUPT PRI,
J0	2B0A8-O1	6-109		INPUT XLTN TO PRIORITY 4D
J1	2B0B0-Q3	6- 99		CHL 7 MASKED INTERRUPT - C#107
J2	2B0B6-M1	6-115		CHL 2 ODD LINE INTERRUPT PRI,
J3	2B0B6-F0	6-115		CHL 1 ODD LINE INTERRUPT PRI,
K0	2B0A3-Q3	6- 85		CHL 0 MASKED INTERRUPT - C#100
K1	2B0A2-Q3	6- 87		CHL 1 MASKED INTERRUPT - C#101
K2	2B0B6-E2	6-115		CHL 6 ODD LINE INTERRUPT PRI,
K3	2B0B6-L2	6-115		CHL 5 ODD LINE INTERRUPT PRI,
L0	2B0B6-X0	6-115	2B0B6-AZ	INT PRIO 2B TO EN FAN-IN
L1	2B0A1-Q3	6- 89		CHL 2 MASKED INTERRUPT - C#102
L2	2B0B7-M1	6-113		CHL 2 EVEN LINE INTERRUPT PRI,
L3	2B0B6-S3	6-115		CHL 4 ODD LINE INTERRUPT PRI,
M0	2B0B6-W0	6-115	2B0B6-AY	INT PRIO 2A TO EN FAN-IN
M1	2B0A0-Q3	6- 91		CHL 3 MASKED INTERRUPT - C#103
M2	2B0B7-C1	6-113		CHAN 0 EVEN LINE INT PRIO
M3	2B0B6-C1	6-115		CHAN 0 ODD LINE INT PRIO
N0	2B0B6-X3	6-115	2B0B6-BZ	INT PRIO 2C TO EN FAN-IN
N1	2B0A8-V0	6-109		ASSOC PROCESSOR INTERRUPT
N2	2B0B7-L2	6-113		CHL 5 EVEN LINE INTERRUPT PRI,
N3	2B0B7-F0	6-113		CHL 1 EVEN LINE INTERRUPT PRI,
O0	2B0B7-L3	6-113		LINE 4 FAN IN FOR CHL 0 THRU 7
O1	2B0B7-X2	6-113	2B0B7-BY	INT PRIO 2D TO EN FAN-IN
O2	2B0A9-R1	6-101		F BIT 11 TO STATUS TEST XLTN
O3	2B0A8-S2	6-109	2B0B8-BM	EXT LINE INTERRUPT PRIORITY
P0	2B2B8-P1	5- 77		NOT NORMAL INT CODE BIT 05
P1	2B2B8-P0	5- 77		
P3	2B0B6-V3	6-115		INPUT TO INTERRUPT PRIORITY 3D
Q1	2B0B6-L3	6-115		LINE 5 FAN IN FOR CHL 0 THRU 7
Q3	2B0B6-B3	6-115		CHL 7 ODD LINE INTERRUPT PRI,
R0	2B0B7-H2	6-113		LINE 6 FAN IN FOR CHL 0 THRU 7
R1	2B0B6-H2	6-115		LINE 7 FAN IN FOR CHL 0 THRU 7
R2	2B0A9-U1	6-101		F BIT 09 TO STATUS TEST XLTN
R3	2B0B7-R0	6-113		CHL 3 EVEN LINE INTERRUPT PRI,
S0	2B0B6-X2	6-115	2B0B6-BY	INT PRIO 2D TO EN FAN-IN
S1	2B0B7-X3	6-113	2B0B7-BZ	INT PRIO 2C TO EN FAN-IN
S3	2B0B6-R0	6-115		CHL 3 ODD LINE INTERRUPT PRI,
T0	2B0B7-H0	6-113		LINE 0 FAN IN FOR CHL 0 THRU 7
T1	2B0B7-W0	6-113	2B0B7-AY	INT PRIO 2A TO EN FAN-IN
T3	2B0B6-W1	6-115		INPUT TO INTERRUPT PRIORITY 3C
U0	2B2B8-K0	5- 77		
U1	2B2B8-K1	5- 77		NORMAL INTERRUPT CODE BIT 06
U2	2B0A9-U0	6-101		F BIT 10 TO STATUS TEST XLTN
U3	2B0B7-V3	6-113		INPUT TO INTERRUPT PRIORITY 3B
V0	2B2B9-K0	5- 75		
V1	2B2B9-K1	5- 75		NOT NORMAL INT CODE BIT 04
V3	2B0A8-U1	6-109		NOT(PRIORITY 3A + PRIORITY 3C)
W0	2B0B7-X0	6-113	2B0B7-AZ	INT PRIO 2B TO EN FAN-IN
W1	2B0B7-H1	6-113		LINE 2 FAN IN FOR CHL 0 THRU 7
W2	2B2B8-O1	5- 77		NORMAL INTERRUPT CODE BIT 03
W3	2B2B8-O0	5- 77		
X0	2B0B6-H1	6-115		LINE 3 FAN IN FOR CHL 0 THRU 7
X1	2B0B6-H0	6-115		LINE 1 FAN IN FOR CHL 0 THRU 7
X2	2B0A8-H2	6-109		F BITS(08)(09)(10)(11)=ZERO
X3	2B0B7-W1	6-113		INPUT TO INTERRUPT PRIORITY 3A



PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	28A3-G1	6- 85	28087-AA	CHL 0 LINE INTERRUPT 0 = C=000
A3	28080-K2	6- 99	28087-RA	CHL 7 LINE INTERRUPT 6 = C=067
B0	28A3-M0	6- 85	28087-AK	CHL 0 LINE INTERRUPT 2 = C=020
B3	28088-I3	6-111		CHL 7 EVEN LINE INTERRUPT PRI.
C0	28A3-F2	6- 85	28087-A0	CHL 0 LINE INTERRUPT 4 = C=040
C1	28088-M2	6-111		CHAN 0 EVEN LINE INT PRIO
C2	28080-F2	6- 99	28087-RH	CHL 7 LINE INTERRUPT 4 = C=047
C3	28080-M0	6- 99	28087-R0	CHL 7 LINE INTERRUPT 2 = C=027
D0	28A2-M0	6- 87	28087-AH	CHL 1 LINE INTERRUPT 2 = C=021
D1	28A3-K2	6- 85	28087-AS	CHL 0 LINE INTERRUPT 6 = C=060
D2	28081-K2	6- 97	28087-BC	CHL 6 LINE INTERRUPT 6 = C=066

D3		2R0R0-G1	6- 99	2B0B7-AR	CHL 7 LINE INTERRUPT 0 - C=007
E0		2R0A2-G1	6- 87	2B0B7-AB	CHL 1 LINE INTERRUPT 0 - C=001
E2		2R0R8-H3	6-111		CHL 6 EVEN LINE INTERRUPT PRI,
E3		2R0R1-F2	6- 97	2B0B7-AG	CHL 6 LINE INTERRUPT 4 - C=046
F0		2R0R8-N3	6-111		CHL 1 EVEN LINE INTERRUPT PRI,
F1		2R0A3-X2	6- 85		NOT(CHL 0 INTERRUPT MASK) COPY
F2	2A1A06P04A-01				NOT CLOCK INT MASK TO DO
	1A4A06J10B-01				
		1R0A1-02	2- 33		
F3	2A1A06P04B-02				
	1A4A06J10A-02				
		1R0A1-03	2- 33		
G0	2A1A06P02C-05				NOT CHAN 0 INT MASK TO DO
	1A4A06J06C-05				
		1A0A0-V1	2- 63		
G1	2A1A06P02C-06				
	1A4A06J06C-06				
		1A0A0-V0	2- 63		
G3		2R0A7-S1	6-117		NOT (CLOCK MASK) TO COPY XMTR
H0		2R0R8-T0	6-111		LINE 0 FAN IN FOR CHL 0 THRU 7
H1		2R0R8-W1	6-111		LINE 2 FAN IN FOR CHL 0 THRU 7
H2		2R0R8-R0	6-111		LINE 6 FAN IN FOR CHL 0 THRU 7
H3		2R0A7-V0	6-117		NOT(FP/BDP MASK) TO COPY XMTR
I0	2A1A06P02C-08				
	1A4A06J06C-08				
		1A0A0-X0	2- 63		
I1	2A1A06P02C-07				NOT CHAN 1 INT MASK TO DO
	1A4A06J06C-07				
		1A0A0-X1	2- 63		
I2	2A1A06P04B-03				NOT FP/BDP INT MASK TO DO
	1A4A06J10B-03				
		1R0A0-K3	2- 35		
I3	2A1A06P04B-04				
	1A4A06J10B-04				
		1R0A0-K2	2- 35		
J0		2R0A2-X2	6- 87		NOT(CHL 1 INTERRUPT MASK) COPY
J1		2R0A2-F2	6- 87	2B0B7-AP	CHAN 1 LINE INT 4 + C=041
J3		2R0B1-G1	6- 97	2B0B7-BW	CHL 6 LINE INTERRUPT 0 - C=006
K0		2R0A2-K2	6- 87	2B0B7-AV	CHL 1 LINE INTERRUPT 6 - C=061
K2		2R0B1-M0	6- 97	2B0B7-BN	CHL 6 LINE INTERRUPT 2 - C=026
K3		2R0B2-F2	6- 95	2B0B7-RJ	CHL 5 LINE INTERRUPT 4 - C=045
L0		2R0A1-G1	6- 89	2B0B7-AE	CHL 2 LINE INTERRUPT 0 - C=002
L1		2R0A1-M0	6- 89	2B0B7-AL	CHL 2 LINE INTERRUPT 2 - C=022
L2		2R0B8-N2	6-111		CHL 5 EVEN LINE INTERRUPT PRI,
L3		2R0B8-00	6-111		LINE 4 FAN IN FOR CHL 0 THRU 7
M0		2R0A4-L1	6-103		SEL SET 0/1/4/5 INTERRUPT MASK
M1		2R0B8-L2	6-111		CHL 2 EVEN LINE INTERRUPT PRI,
M2		2R0B2-K2	6- 95	2B0B7-RD	CHAN 5 LINE INT, 6= C=065
M3		2R0A8-M2	6-109		SET ILLEGAL WRITE F/F FROM BC
N0		2R0A9-I3	6-101		SEL SET INTERRUPT MASK-FAN OUT
N3		2R0A8-K2	6-109		SST ILL, WR FF FROM MN CONT
O0		2R0B4-L1	6-105		SEL SET 2,3,6,AND 7 INT MASK
O1		2R0A7-J0	6-117		SEL SET INTERNAL INT MASK
O2		2A2A5-S1	5- 3		
O3		2A2A5-S0	5- 3		SET ILLEGAL WRITE STATUS FF
P0		2R0A1-K2	6- 89	2B0B7-AR	CHL 2 LINE INTERRUPT 6 - C=062
P1		2R0A1-F2	6- 89	2B0B7-AN	CHL 2 LINE INTERRUPT 4 - C=042
P2		2R1A8-D2	6- 17		
P3		2R1A8-D3	6- 17		MAINT MODE RF ERROR IRT WRITE
Q0		2R0A0-G1	6- 91	2B0B7-AD	CHL 3 LINE INTERRUPT 0 - C=003
Q2		2R0B2-G1	6- 95	2B0B7-RS	CHL 5 LINE INTERRUPT 0 - C=005
Q3		2R0B2-M0	6- 95	2B0B7-BP	CHL 5 LINE INTERRUPT 2 - C=025
R0		2R0B8-R3	6-111		CHL 3 EVEN LINE INTERRUPT PRI,
R2		2R0B3-K2	6- 93	2B0B7-BF	CHL 4 LINE INTERRUPT 6 - C=064
R3		2R0B3-F2	6- 93	2B0B7-RK	CHL 4 LINE INTERRUPT 4 - C=044
S0		2R0B3=X2	6- 93		NOT(CHL 4 INTERRUPT MASK) COPY
S1		2R0A0=M0	6- 91	2B0B7-AJ	CHL 3 LINE INTERRUPT 2 - C=023
S3		2R0B8=H2	6-111		CHL 4 EVEN LINE INTERRUPT PRI,
T0	2A1A06P04A-04				
	1A4A06J10A-04				
		1R0A2=J2	2- 31		
T1	2A1A06P04A-03				NOT CHAN 4 INT MASK TO DO
	1A4A06J10A-03				
		1R0A2=J3	2- 31		
T2	2A1A06P04A-06				
	1A4A06J10A-06				
		1R0A2-Q3	2- 31		
T3	2A1A06P04A-05				NOT CHAN 5 INT MASK TO DO
	1A4A06J10A-05				
		1R0A2-Q2	2- 31		
U0		2R0A0-F2	6- 91	2B0B7-AM	CHL 3 LINE INTERRUPT 4 - C=043
U1		2R0A8-T2	6-109		NOT(FAN IN EVEN LINES CHL 0-3)
U2		2R0B2-X2	6- 95		NOT(CHL 5 INTERRUPT MASK) COPY
U3		2R0A8-U2	6-109		NOT(FAN IN EVEN LINES CHL 4-7)
V0		2R0A8-P1	6-109	2B0B7-AW	NOT (CHAN 0=3 INTERRUPT PRIO)
V1		2R0A0-K2	6- 91	2B0B7-AU	CHL 3 LINE INTERRUPT 6 - C=063
V2		2R0A8-P3	6-109	2B0B7-RU	NOT (CHAN 4-7 INTERRUPT PRIO)
V3		2R0R8-U3	6-111		INPUT TO INTERRUPT PRIORITY 3B
W0		2R0B8-T1	6-111	2B0B7-AY	INT PRIO 2A TO EN FAN-IN
W1		2R0R8-X3	6-111		INPUT TO INTERRUPT PRIORITY 3A
W2		2R0B3-G1	6- 93	2B0B7-BX	CHL 4 LINE INTERRUPT 0 - C=004
W3		2R0B3-M0	6- 93	2B0B7-RL	CHL 4 LINE INTERRUPT 2 - C=024
X0		2R0R8-W0	6-111	2B0B7-AZ	INT PRIO 2B TO EN FAN-IN
X2		2R0B8-01	6-111	2B0B7-RY	INT PRIO 2D TO EN FAN-IN
X3		2R0R8-S1	6-111	2B0B7-RZ	INT PRIO 2C TO EN FAN-IN

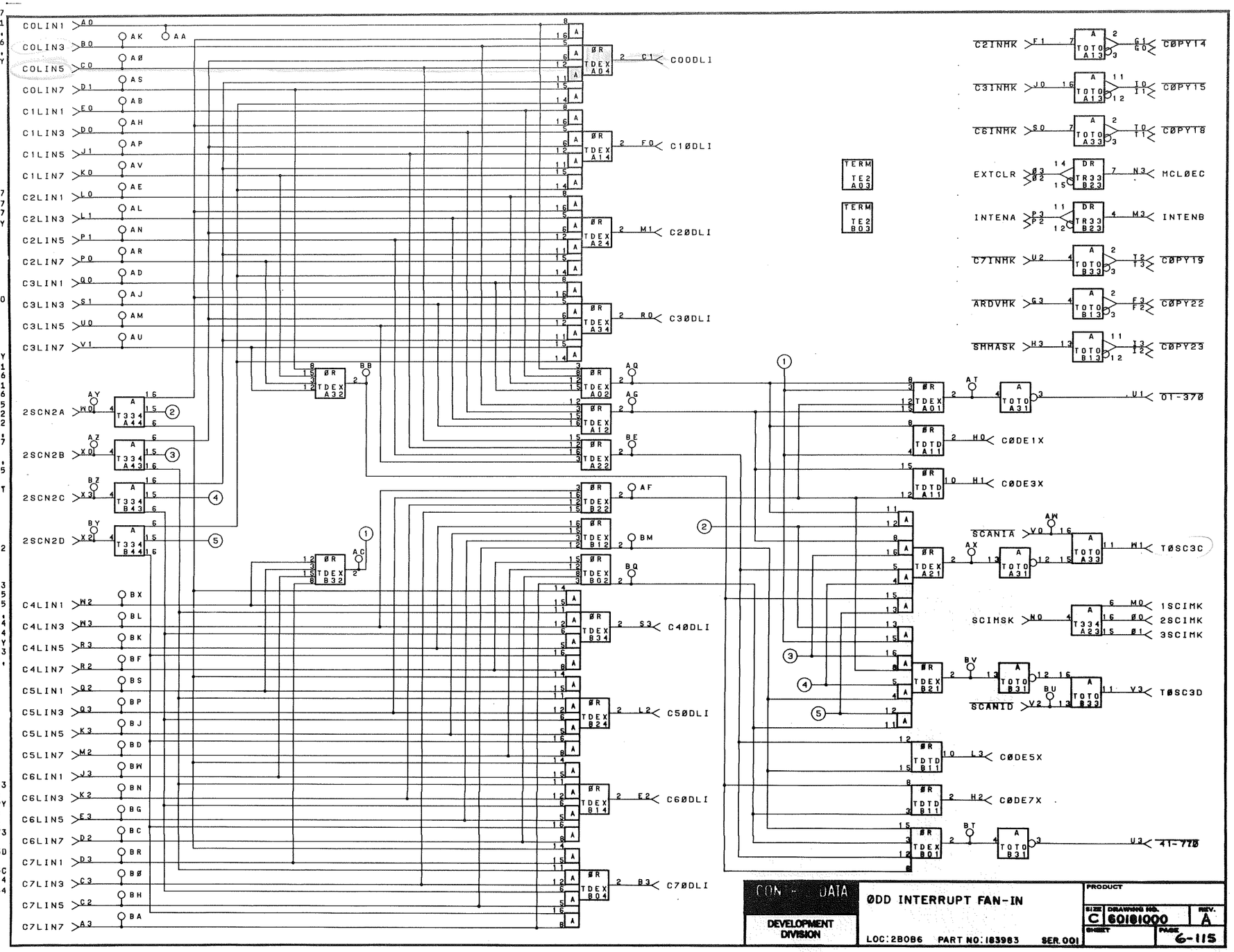


CONTROL DATA DEVELOPMENT DIVISION	EVEN INTERRUPT FAN-IN	PRODUCT	
	LOC:2B0B7 PART NO:183983 SER. 000	SIZE C	DRAWING NO. 60181000 REV. A
		SHEET	PAGE 6-113

299

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2R0A3-J0	6- 85	2B0B6-AA	CHL 0 LINE INTERRUPT 1 - C=010
A3	2R0B0-P2	6- 99	2B0B6-BA	CHL 7 LINE INTERRUPT 7 - C=077
B0	2R0A3-S0	6- 85	2B0B6-AK	CHL 0 LINE INTERRUPT 3 - C=030
B3	2R0B8-Q3	6-111		CHL 7 ODD LINE INTERRUPT PRI,
C0	2R0A3-G2	6- 85	2B0B6-AQ	CHL 0 LINE INTERRUPT 5 - C=050
C1	2R0B8-M3	6-111		CHAN 0 ODD LINE INT PRIO
C2	2R0B0-G2	6- 99	2B0B6-BH	CHL 7 LINE INTERRUPT 5 - C=057
C3	2R0B0-S0	6- 99	2B0B6-BQ	CHL 7 LINE INTERRUPT 3 - C=037
D0	2R0A2-S0	6- 87	2B0B6-AH	CHL 1 LINE INTERRUPT 3 - C=031
D1	2R0A3-P2	6- 85	2B0B6-AS	CHL 0 LINE INTERRUPT 7 - C=070
D2	2R0B1-P2	6- 97	2B0B6-BC	CHL 6 LINE INTERRUPT 7 - C=076

D3	2B0R0-I0	6- 99	2B0B6-RR	CHL 7 LINE INTERRUPT 1 - C=017
E0	2B0A2-I0	6- 87	2B0B6-AB	CHL 1 LINE INTERRUPT 1 - C=011
E2	2B0B8-K2	6-111		CHL 6 ODD LINE INTERRUPT PRI,
E3	2B0B1-G2	6- 97	2B0B6-RG	CHL 6 LINE INTERRUPT 5 - C=056
F0	2B0B8-J3	6-111		CHL 1 ODD LINE INTERRUPT PRI,
F1	2B0A1-X2	6- 89		NOT(CHL 2 INTERRUPT MASK) COPY
F2	2A1A06P04B-05			NOT ARITH INT MASK TO DO
	1A4A06J10B-05			
	1B0A0-J3	2- 35		
F3	2A1A06P04B-06			
	1A4A06J10B-06			
	1B0A0-J2	2- 35		
G0	2A1A06P02C-09			NOT CHAN 2 INT MASK TO DO
	1A4A06J06C-09			
	1A0A0-Q0	2- 63		
G1	2A1A06P02C-10			
	1A4A06J06C-10			
	1A0A0-Q1	2- 63		
G3	2B0A7-N0	6-117		NOT (ARITH MASK) TO COPY XMTR
H0	2B0B6-X1	6-111		LINE 1 FAN IN FOR CHL 0 THRU 7
H1	2B0B6-X0	6-111		LINE 3 FAN IN FOR CHL 0 THRU 7
H2	2B0B6-R1	6-111		LINE 7 FAN IN FOR CHL 0 THRU 7
H3	2B0A7-U1	6-117		NOT (SRCH + MOVE MASK) TO COPY XMTR
I0	2A1A06P04A-02			
	1A4A06J10A-02			
	1B0A2-K2	2- 31		
I1	2A1A06P04A-01			NOT CHAN 3 INT MASK TO DO
	1A4A06J10A-01			
	1B0A2-K3	2- 31		
I2	2A1A06P04B-07			NOT SRCH + MOVE INT MASK TO DO
	1A4A06J10B-07			
	1B0A0-Q2	2- 35		
I3	2A1A06P04B-08			
	1A4A06J10B-08			
	1B0A0-Q3	2- 35		
J0	2B0A0-X2	6- 91		NOT(CHL 3 INTERRUPT MASK) COPY
J1	2B0A2-G2	6- 87	2B0B6-AP	CHL 1 LINE INTERRUPT 5 - C=051
J3	2B0R1-I0	6- 97	2B0B6-RW	CHL 6 LINE INTERRUPT 1 - C=016
K0	2B0A2-P2	6- 87	2B0B6-AV	CHL 1 LINE INTERRUPT 7 - C=071
K2	2B0B1-S0	6- 97	2B0B6-RN	CHL 6 LINE INTERRUPT 3 - C=036
K3	2B0B2-G2	6- 95	2B0B6-RJ	CHL 5 LINE INTERRUPT 5 - C=055
L0	2B0A1-I0	6- 89	2B0B6-AE	CHL 2 LINE INTERRUPT 1 - C=012
L1	2B0A1-S0	6- 89	2B0B6-AL	CHL 2 LINE INTERRUPT 3 - C=032
L2	2B0B8-K3	6-111		CHL 5 ODD LINE INTERRUPT PRI,
L3	2B0B8-Q1	6-111		LINE 5 FAN IN FOR CHL 0 THRU 7
M0	2B0A4-N1	6-103		SEL CLR 0,1,4,5 OF INT MASK
M1	2B0B8-J2	6-111		CHL 2 ODD LINE INTERRUPT PRI,
M2	2B0B2-P2	6- 95	2B0B6-RD	CHL 5 LINE INTERRUPT 7 - C=075
M3	2B0A8-K3	6-109		INTERRUPT SYSTEM ENABLE
N0	2B0A9-W2	6-101		SEL CLR INTERRUPT MASK-FAN OUT
N3	2B0A7-K3	6-117	2B0A7-RO	MC + EXT CLR + POWER ON CLR
O0	2B0B4-N1	6-105		SEL CLR 2,3,6,7 OF INT MASK
O1	2B0A7-J1	6-117		SEL CLR INTERNAL INT MASK
O2	2B1B1-I1	6- 9		
O3	2B1B1-I0	6- 9		EXT CLEAR I/O THRU CHAN
P0	2B0A1-P2	6- 89	2B0B6-AR	CHL 2 LINE INTERRUPT 7 - C=072
P1	2B0A1-G2	6- 89	2B0B6-AN	CHAN 2 LINE INT 5 + C=052
P2	2B1B7-D0	6- 3		
P3	2B1B7-D1	6- 3		INTERRUPTS ENABLED
Q0	2B0A0-I0	6- 91	2B0B6-AD	CHL 3 LINE INTERRUPT 1 - C=013
Q2	2B0B2-I0	6- 95	2B0B6-BS	CHL 5 LINE INTERRUPT 1 - C=015
Q3	2B0B2-S0	6- 95	2B0B6-RP	CHL 5 LINE INTERRUPT 3 - C=035
R0	2B0B8-S3	6-111		CHL 3 ODD LINE INTERRUPT PRI,
R2	2B0B3-P2	6- 93	2B0B6-RF	CHL 4 LINE INTERRUPT 7 - C=074
R3	2B0B3-G2	6- 93	2B0B6-RK	CHL 4 LINE INTERRUPT 5 - C=054
S0	2B0B1-X2	6- 97		NOT(CHL 6 INTERRUPT MASK) COPY
S1	2B0A0-S0	6- 91	2B0B6-AJ	CHL 3 LINE INTERRUPT 3 - C=033
S3	2B0B8-L3	6-111		CHL 4 ODD LINE INTERRUPT PRI,
T0	2A1A06P04A-08			
	1A4A06J10A-08			
	1B0A1-K2	2- 33		
T1	2A1A06P04A-07			NOT CHAN 6 INT MASK TO DO
	1A4A06J10A-07			
	1B0A1-K3	2- 33		
T2	2A1A06P04A-10			
	1A4A06J10A-10			
	1B0A1-J2	2- 33		
T3	2A1A06P04A-09			NOT CHAN 7 INT MASK TO DO
	1A4A06J10A-09			
	1B0A1-J3	2- 33		
U0	2B0A0-G2	6- 91	2B0B6-AH	CHL 3 LINE INTERRUPT 5 - C=053
U1	2B0A8-U3	6-109		NOT(FAN IN ODD LINES CHL 4-7)
U2	2B0B0-X2	6- 99		NOT(CHL 7 INTERRUPT MASK) COPY
U3	2B0A8-V3	6-109		NOT(FAN IN ODD LINES CHL 4-7)
V0	2B0A8-D3	6-109	2B0B6-AW	NOT(ARITH INTERRUPT PRIORITY)
V1	2B0A0-P2	6- 91	2B0B6-AU	CHL 3 LINE INTERRUPT 7 - C=073
V2	2B0A8-V1	6-109	2B0B6-RU	NOT(MISC INTERRUPT PRIORITY)
V3	2B0B8-P3	6-111		INPUT TO INTERRUPT PRIORITY 3D
W0	2B0R8-M0	6-111	2B0B6-AY	INT PRIO 2A TO EN FAN-IN
W1	2B0B8-T3	6-111		INPUT TO INTERRUPT PRIORITY 3C
W2	2B0R3-I0	6- 93	2B0B6-RX	CHL 4 LINE INTERRUPT 1 - C=014
W3	2B0B3-S0	6- 93	2B0B6-RL	CHL 4 LINE INTERRUPT 3 - C=034
X0	2B0B8-L0	6-111	2B0B6-AZ	INT PRIO 2B TO EN FAN-IN
X2	2B0B8-S0	6-111	2B0B6-RY	INT PRIO 2D TO EN FAN-IN
X3	2B0B8-N0	6-111	2B0B6-BZ	INT PRIO 2C TO EN FAN-IN



CONTROL DATA — DEVELOPMENT DIVISION

ØDD INTERRUPT FAN-IN

LOC:2B0B6 PART NO:183983 SER.001

PRODUCT

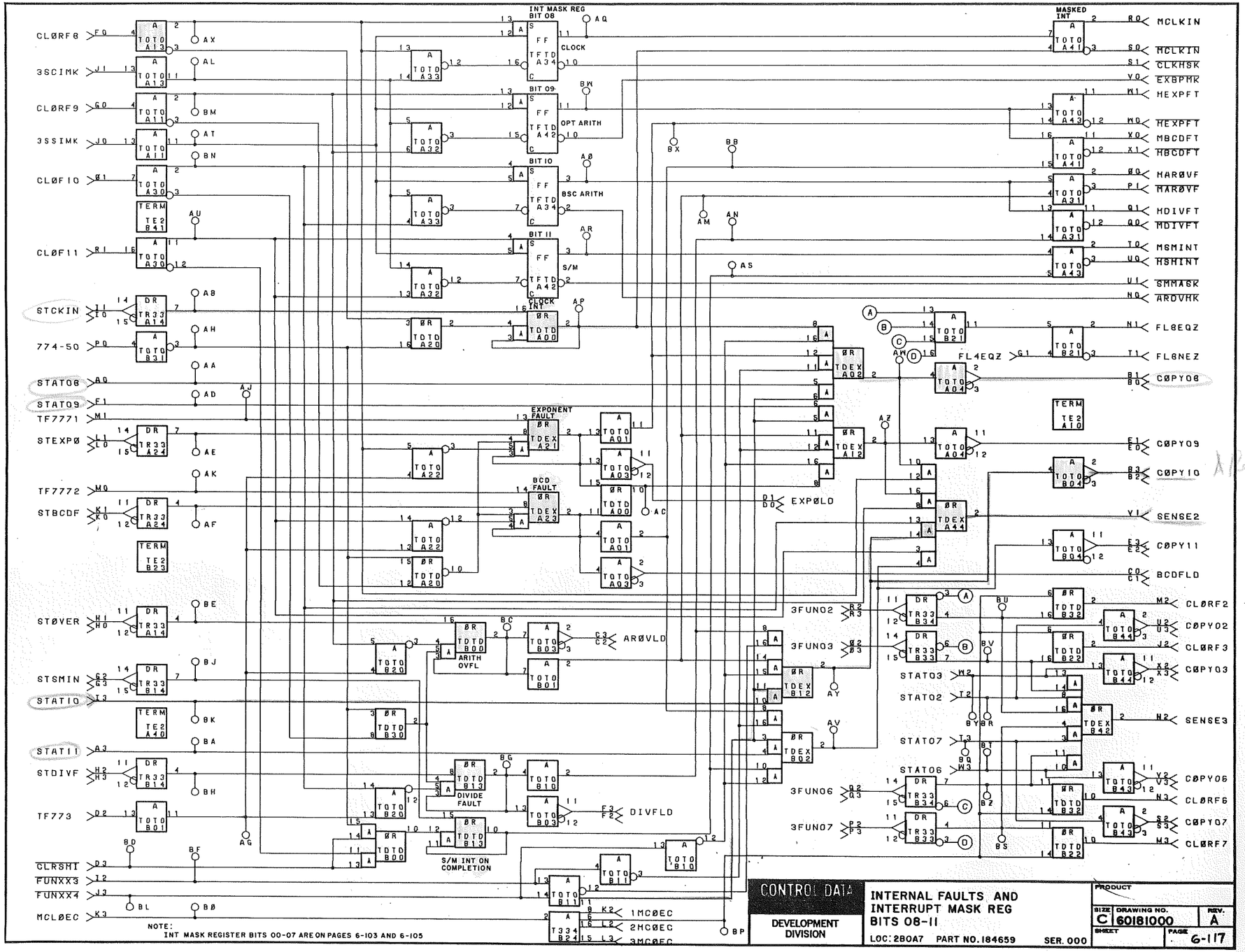
SIZE C | DRAWING NO. 60181000 | REV. A

SHEET | PAGE 6-115

301

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2R0A6-I1	6-121	2B0A7-AA	SELECTED STATUS BIT 08 TO TEST
A3	2R0A5-I1	6-123	2B0A7-BA	SELECTED STATUS BIT 11 TO TEST
B0	2A1A06P02R-08			
	1A4A06J06R-08			
	1A0A4-Q1	2- 59		
B1	2A1A06P02R-07			SELECTED STATUS BIT 08 TO DO
	1A4A06J06R-07			
	1A0A4-Q0	2- 59		
B2	2A1A06P02C-02			
	1A4A06J06C-02			
	1A0A2-X0	2- 61		
B3	2A1A06P02C-01			SELECTED STATUS BIT 10 TO DO
	1A4A06J06C-01			
	1A0A2-X1	2- 61		
C0	2R2R2-S1	5- 89		BDP FAULT INDICATOR
C1	2R2R2-S0	5- 89		
C2	2R2R2-N0	5- 89		
C3	2R2R2-N1	5- 89		ARITH OVFL INDICATOR
D0	2R2R2-T0	5- 89		
D1	2R2R2-T1	5- 89		EXPONENT OVERFLOW IND DRIVER
D2	2R0A9-V3	6-101		CLEAR INTERNAL FAULTS SENSED
D3	2R0A9-P1	6-101	2B0A7-BD	NOT(CLEAR S/M INTERRUPT)
E0	2A1A06P02R-10			
	1A4A06J06R-10			
	1A0A2-V0	2- 61		
E1	2A1A06P02R-09			SELECTED STATUS BIT 09 TO DO
	1A4A06J06R-09			
	1A0A2-V1	2- 61		
E2	2A1A06P02C-04			
	1A4A06J06C-04			
	1A0A2-Q1	2- 61		
E3	2A1A06P02C-03			SELECTED STATUS BIT 11 TO DO
	1A4A06J06C-03			
	1A0A2-Q0	2- 61		
F0	2R0A9-Q1	6-101		CLEAR XLTN OR F REG BIT 08
F1	2R0A5-N0	6-123	2B0A7-AD	SELECTED STATUS BIT 09 TO TEST
F2	2R2R2-M0	5- 89		
F3	2R2R2-M1	5- 89		DIVIDE FAULT INDICATOR DRIVER
G0	2R0A9-Q0	6-101		CLEAR XLTN OR F REG BIT 09
G1	2R0A8-B1	6-109		F REG BITS (00)(01)(04)(05)=0
G2	2B1A6-03	6- 13		SET S/M INTERRUPT ON COMPL
G3	2B1A6-02	6- 13		
H0	2A1A06P06A-04			
	1A4A06J18A-04			
	1C1B9-H1	3- 19		
H1	2A1A06P06A-03			SET OVERFLOW FF
	1A4A06J18A-03			
	1C1B9-H0	3- 19		
H2	2A1A06P06A-01			SET DIVIDE FAULT FF

	1A4A06J18A-01				
	1C1B8-E1	3- 17			
H3	2A1A06P06A-02				
	1A4A06J18A-02				
	1C1B8-E0	3- 17			
I0	2A1B4-F3	6- 57			
I1	2A1B4-F2	6- 57			SET CLOCK INTERRUPT F/F
I2	2B0A9-L1	6-101	2B0A7-RF		NOT(SEL INTERNAL STAT FAN-IN)
I3	2B0A6-N0	6-121	2B0A7-RK		SELECTED STATUS BIT 10 TO TEST
J0	2B0B7-01	6-113			SEL SET INTERNAL INT MASK
J1	2B0B6-01	6-115			SEL CLR INTERNAL INT MASK
J2	2B0B4-S0	6-105			CLEAR XLTN OR F REG BIT 03
J3	2B0A9-D0	6-101	2B0A7-RL		NOT(SEL INTERRUPT FAN IN)
K0	2A1A06J06D-02				
	1A4A06P01D-02				
	1A2A8-E1	4- 21			
K1	2A1A06J06D-01				(BCD FAULT)(BDP COMPLETE)(H03)
	1A4A06P01D-01				
	1A2A8-E0	4- 21			
K2	2B0A4-P3	6-103			CLR XLTN TO CHAN 0;1,4,5 FANOUT
K3	2B0B6-N3	6-115	2B0A7-RO		MC + EXT CLR + POWER ON CLR
L0	2A1A06J06D-04				
	1A4A06P01D-04				
	1B1B4-V1	3-115			
L1	2A1A06J06D-03				SET EXPONENT FAULT
	1A4A06P01D-03				
	1B1B4-V0	3-115			
L2	2B0B4-P3	6-105			CLR XLTN TO CHAN 2;3,6, AND 7 FANOUT
L3	2B0A8-B0	6-109			CLR XLTN TO OR WITH F 01,04,05
M0	2B0A9-K2	6-101	2B0A7-AK		SET BCD FAULT
M1	2B0A9-H0	6-101	2B0A7-AJ		SET EXPONENT OVERFLOW FAULT
M2	2B0B4-I0	6-105			CLEAR XLTN OR F REG BIT 02
M3	2B0B4-X3	6-105			CLEAR XLTN OR F REG BIT 07
N0	2B0B6-G3	6-115			NOT (ARITH MASK) TO COPY XMTR
N1	2B0A8-F3	6-109			F0(BITS 00-07) EQUAL ZERO
N2	2B0A9-T3	6-101			SEL STATUS=F BIT 02+03+06+07
N3	2B0B4-A3	6-105			CLEAR XLTN OR F REG BIT 06
O0	2B0B8-E0	6-111			MASKED ARITH OVERFLOW FAULT
O1	2B0A9-S0	6-101			CLEAR XLTN OR F REG BIT 10
O2	2A1B5-L2	6- 45			F BIT 03 TO STATUS COMPARE
O3	2A1B5-L3	6- 45			
P0	2B0A9-H3	6-101			CLEAR INTERNAL INTERRUPT/FAULT
P1	2B0A8-H3	6-109			NOT (MASKED ARITH OVFL FAULT)
P2	2A1A5-N3	6- 47			F BIT 07 TO STATUS COMPARE
P3	2A1A5-N2	6- 47			
Q0	2B0A8-X3	6-109			NOT(MASKED DIVIDE FAULT)
Q1	2B0B8-D0	6-111			MASKED DIVIDE FAULT
Q2	2A1A5-O2	6- 47			F BIT 06 TO STATUS COMPARE
Q3	2A1A5-O3	6- 47			
R0	2B0B8-E1	6-111			MASKED CLOCK INTERRUPT
R1	2B0A9-R0	6-101			CLEAR XLTN OR F REG BIT 11
R2	2A1B5-G3	6- 45			F BIT 02 TO STATUS COMPARE
R3	2A1B5-G2	6- 45			
S0	2B0A8-H3	6-109			NOT(MASKED CLOCK INTERRUPT)
S1	2B0B7-G3	6-113			NOT (CLOCK MASK) TO COPY XMTR
S2	2A1A06P02B-05				SELECTED STATUS BIT 07 TO DO
	1A4A06J06B-05				
	1A0A4-X1	2- 59			
S3	2A1A06P02B-06				
	1A4A06J06B-06				
	1A0A4-X0	2- 59			
T0	2B0B8-F1	6-111			MASKED SEARCH/MOVE INTERRUPT
T1	2B0A9-H0	6-101			F0(BITS 00-07)NOT EQUAL ZERO
T2	2B0A6-H3	6-121	2B0A7-RR		SELECTED STATUS BIT 02 TO TEST
T3	2B0A5-00	6-123	2B0A7-RQ		SELECTED STATUS BIT 07 TO TEST
U0	2B0A8-N2	6-109			NOT(MASKED S/M INTERRUPT)
U1	2B0B6-H3	6-115			NOT (SRCH + MOVE MASK) TO COPY XMTR
U2	2A1A06P02A-05				SELECTED STATUS BIT 02 TO DO
	1A4A06J06A-05				
	1A0A8-Q0	2- 55			
U3	2A1A06P02A-06				
	1A4A06J06A-06				
	1A0A8-Q1	2- 55			
V0	2B0B7-H3	6-113			NOT(FP/BDP MASK) TO COPY XMTR
V1	2B0A9-T2	6-101			SEL STATUS=F BIT 08+09+10+11
V2	2A1A06P02R-03				SELECTED STATUS BIT 06 TO DO
	1A4A06J06B-03				
	1A0A4-V1	2- 59			
V3	2A1A06P02B-04				
	1A4A06J06B-04				
	1A0A4-V0	2- 59			
W0	2B0A8-X2	6-109			NOT(MASKED EXPONENT FAULT)
W1	2B0B8-C0	6-111			MASKED EXPONENT FAULT
W2	2B0A5-H3	6-123	2B0A7-RY		SELECTED STATUS BIT 03 TO TEST
W3	2B0A6-00	6-121	2B0A7-RT		SELECTED STATUS BIT 06 TO TEST
X0	2B0B8-B0	6-111			MASKED BDP FAULT
X1	2B0A8-W2	6-109			NOT (MASKED BDP FAULT)
X2	2A1A06P02A-07				SELECTED STATUS BIT 03 TO DO
	1A4A06J06A-07				
	1A0A6-V1	2- 57			
X3	2A1A06P02A-08				
	1A4A06J06A-08				
	1A0A6-V0	2- 57			



CONTROL DATA
DEVELOPMENT DIVISION

INTERNAL FAULTS AND INTERRUPT MASK REG BITS 08-11

LOC: 2B0A7 PART NO. 184659 SER. 000

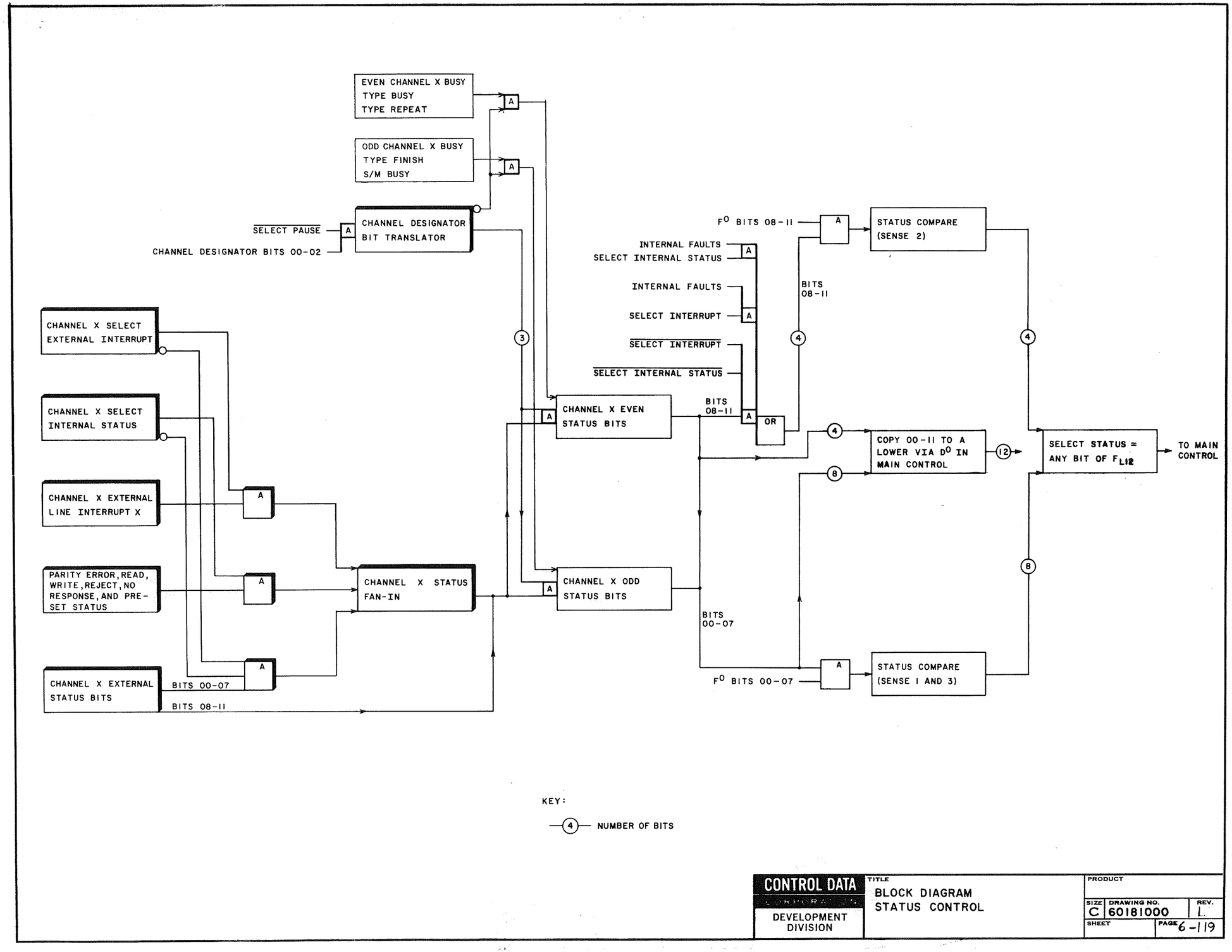
PRODUCT

SIZE	DRAWING NO.	REV.
C	60181000	A

SHEET PAGE 6-117

-otlr Bit on 6-105.

303

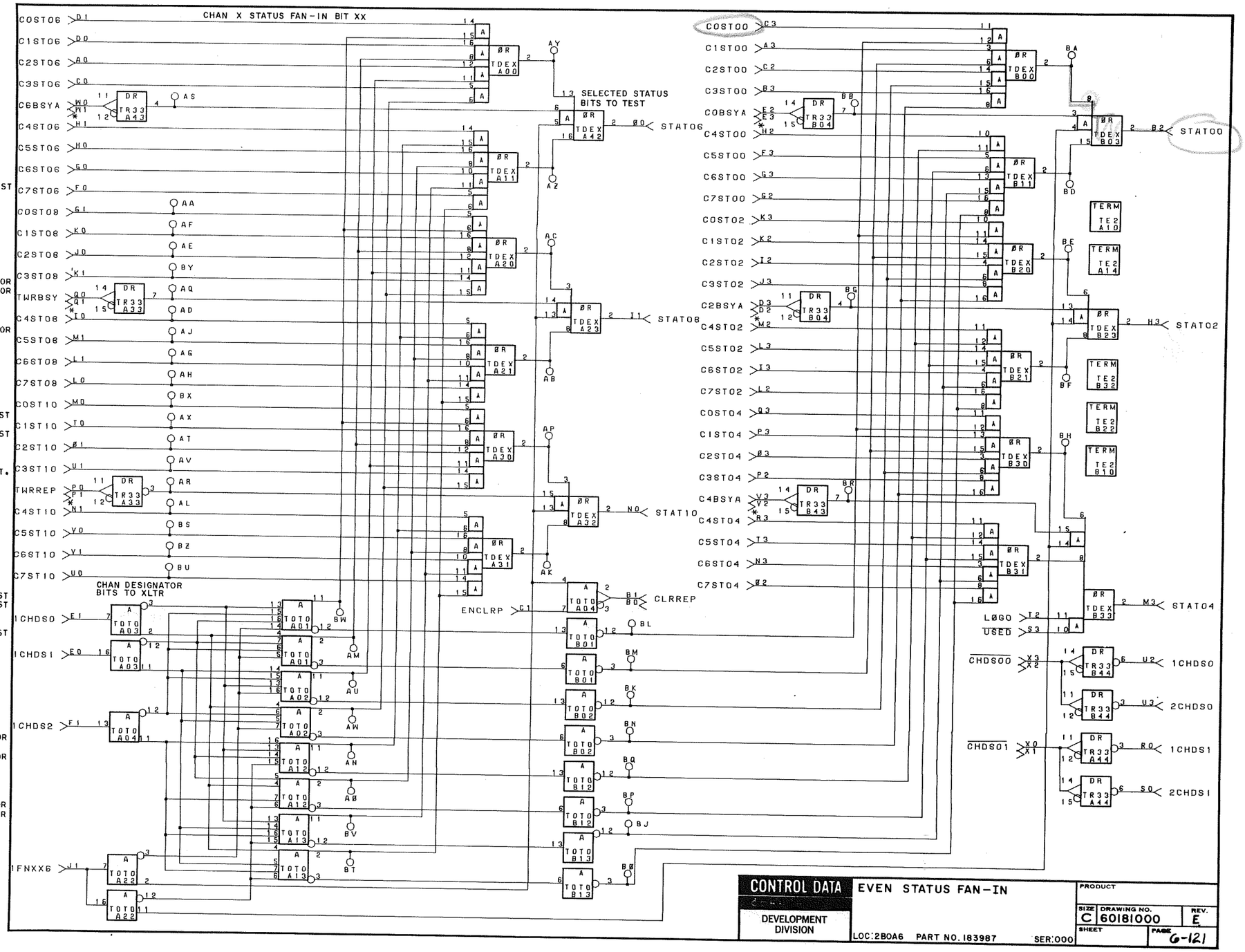


KEY:

—(4)— NUMBER OF BITS

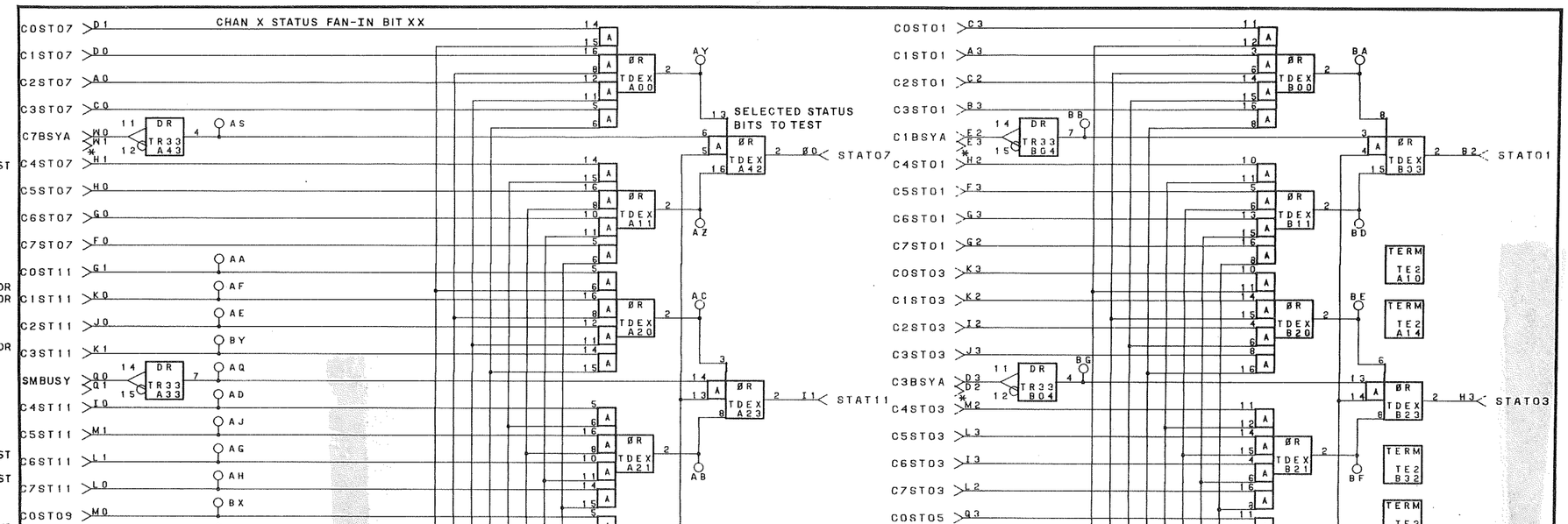
CONTROL DATA DEVELOPMENT DIVISION	TITLE: BLOCK DIAGRAM STATUS CONTROL	PRODUCT	
		SIZE C	DRAWING NO. 60181000
		REV. L	
		SHEET	PAGE 6-119

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B0A1-K3	6- 89		CHL 2 STATUS FAN IN BIT 06
A1	2B0A2-A0	6- 87		CHL 1 STATUS FAN IN BIT 00
B0	2B1B9-V3	6- 27		
B1	2B1B9-V2	6- 27		CLEAR TYPEWRITER REPEAT FF
B2	2B0A8-L0	6-109		SELECTED STATUS BIT 00 TO TEST
B3	2B0A0-A0	6- 91		CHL 3 STATUS FAN IN BIT 00
C0	2B0A0-K3	6- 91		CHL 3 STATUS FAN IN BIT 06
C1	2B0A9-S1	6-101		ENABLE CLEAR TW REPEAT FF
C2	2B0A1-A0	6- 89		CHL 2 STATUS FAN IN BIT 00
C3	2B0A3-A0	6- 85		CHL 0 STATUS FAN IN BIT 00
D0	2B0A2-K3	6- 87		CHL 1 STATUS FAN IN BIT 06
D1	2B0A3-K3	6- 85		CHL 0 STATUS FAN IN BIT 06
D2	2B1A5-I3	6- 19		
D3	2B1A5-I2	6- 19		NOT CHAN 2 BUSY TO STATUS FI
E0	2B0A6-R0	6-121		CHL DESIGNATOR BIT 01 TO XLTOR
E1	2B0A6-U2	6-121		CHL DESIGNATOR BIT 00 TO XLTOR
E2	2B1A5-R3	6- 19		NOT CHAN 0 BUSY TO STATUS FI
E3	2B1A5-R2	6- 19		
F0	2B0B0-K3	6- 99		CHL 7 STATUS FAN IN BIT 06
F1	2B0A5-U2	6-123		CHL DESIGNATOR BIT 02 TO XLTOR
F3	2B0B2-A0	6- 95		CHL 5 STATUS FAN IN BIT 00
G0	2B0B1-K3	6- 97		CHL 6 STATUS FAN IN BIT 06
G1	2B0A3-W0	6- 85	2B0A6-AA	CHL 0 EXTERNAL STATUS BIT 08
G2	2B0B0-A0	6- 99		CHL 7 STATUS FAN IN BIT 00
G3	2B0B1-A0	6- 97		CHL 6 STATUS FAN IN BIT 00
H0	2B0B2-K3	6- 95		CHL 5 STATUS FAN IN BIT 06
H1	2B0B3-K3	6- 93		CHL 4 STATUS FAN IN BIT 06
H2	2B0B3-A0	6- 93		CHL 4 STATUS FAN IN BIT 00
H3	2B0A7-T2	6-117	2B0A7-BR	SELECTED STATUS BIT 02 TO TEST
I0	2B0B3-W0	6- 93	2B0A6-AD	CHL 4 EXTERNAL STATUS BIT 08
I1	2B0A7-A0	6-117	2B0A7-AA	SELECTED STATUS BIT 08 TO TEST
I2	2B0A1-M1	6- 89		CHL 2 STATUS FAN IN BIT 02
I3	2B0B1-M1	6- 97		CHL 6 STATUS FAN IN BIT 02
J0	2B0A1-W0	6- 89	2B0A6-AE	CHL 2 EXTERNAL STATUS BIT 08
J1	2B0A9-A0	6-101		SELECT PAUSE FAN IN EVEN STAT.
J3	2B0A0-M1	6- 91		CHL 3 STATUS FAN IN BIT 02
K0	2B0A2-W0	6- 87	2B0A6-AF	CHL 1 EXTERNAL STATUS BIT 08
K1	2B0A0-W0	6- 91	2B0A6-BY	CHL 3 EXTERNAL STATUS BIT 08
K2	2B0A2-M1	6- 87		CHL 1 STATUS FAN IN BIT 02
K3	2B0A3-M1	6- 85		CHL 0 STATUS FAN IN BIT 02
L0	2B0B0-W0	6- 99	2B0A6-AH	CHL 7 EXTERNAL STATUS BIT 08
L1	2B0B1-W0	6- 97	2B0A6-AG	CHL 6 EXTERNAL STATUS BIT 08
L2	2B0B0-M1	6- 99		CHL 7 STATUS FAN IN BIT 02
L3	2B0B2-M1	6- 95		CHL 5 STATUS FAN IN BIT 02
M0	2B0A3-X3	6- 85	2B0A6-BX	CHL 0 EXTERNAL STATUS BIT 10
M1	2B0B2-W0	6- 95	2B0A6-AJ	CHL 5 EXTERNAL STATUS BIT 08
M2	2B0B3-M1	6- 93		CHL 4 STATUS FAN IN BIT 02
M3	2B0A8-G1	6-109		SELECTED STATUS BIT 04 TO TEST
N0	2B0A7-I3	6-117	2B0A7-BK	SELECTED STATUS BIT 10 TO TEST
N1	2B0B3-X3	6- 93	2B0A6-AL	CHL 4 EXTERNAL STATUS BIT 10
N3	2B0B1-A3	6- 97		CHL 6 STATUS FAN IN BIT 04
O0	2B0A7-W3	6-117	2B0A7-BT	SELECTED STATUS BIT 06 TO TEST
O1	2B0A1-X3	6- 89	2B0A6-AT	CHL 2 EXTERNAL STATUS BIT 10
O2	2B0B0-A3	6- 99		CHL 7 STATUS FAN IN BIT 04
O3	2B0A1-A3	6- 89		CHL 2 STATUS FAN IN BIT 04
P0	2B1A7-G1	6- 1		NOT TW REPEAT TO STATUS FI
P1	2B1A7-G0	6- 1		
P2	2B0A0-A3	6- 91		CHL 3 STATUS FAN IN BIT 04
P3	2B0A2-A3	6- 87		CHL 1 STATUS FAN IN BIT 04
Q0	2B1B9-G3	6- 27		NOT TW BUSY TO STATUS FI
Q1	2B1B9-G2	6- 27		
Q3	2B0A3-A3	6- 85		CHL 0 STATUS FAN IN BIT 04
R0	2B0A6-E0	6-121		CHL DESIGNATOR BIT 01 TO XLTOR
R3	2B0B3-A3	6- 93		CHL 4 STATUS FAN IN BIT 04
S0	2B0A5-E0	6-123		CHL DESIGNATOR BIT 01 TO XLTOR
T0	2B0A2-X3	6- 87	2B0A6-AX	CHL 1 EXTERNAL STATUS BIT 10
T3	2B0B2-A3	6- 95		CHL 5 STATUS FAN IN BIT 04
U0	2B0B0-X3	6- 99	2B0A6-BU	CHL 7 EXTERNAL STATUS BIT 10
U1	2B0A0-X3	6- 91	2B0A6-AV	CHL 3 EXTERNAL STATUS BIT 10
U2	2B0A6-E1	6-121		CHL DESIGNATOR BIT 00 TO XLTOR
U3	2B0A5-E1	6-123		CHL DESIGNATOR BIT 00 TO XLTOR
V0	2B0B2-X3	6- 95	2B0A6-BS	CHL 5 EXTERNAL STATUS BIT 10
V1	2B0B1-X3	6- 97	2B0A6-BZ	CHL 6 EXTERNAL STATUS BIT 10
V2	2B1B5-B2	6- 21		
V3	2B1B5-B3	6- 21		NOT CHL 4 BUSY TO STAT FAN-IN
W0	2B1B5-I2	6- 21		NOT CHL 6 BUSY TO STAT FAN-IN
W1	2B1B5-I3	6- 21		
X0	2A1B8-E3	6- 53		
X1	2A1B8-E2	6- 53		NOT CHAN SEL BIT 01 ON 7X
X2	2A1B8-C3	6- 53		NOT CHAN SEL BIT 00 ON 7X
X3	2A1B8-C2	6- 53		



PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2B0A1-P3	6- 89		CHL 2 STATUS FAN IN BIT 07
A3	2B0A2-G0	6- 87		CHL 1 STATUS FAN IN BIT 01
B0	2B1B9-U3	6- 27		
B1	2B1B9-U2	6- 27		CLEAR TYPEWRITER FINISH FF
B2	2B0A8-G0	6-109		SELECTED STATUS BIT 01 TO TEST
B3	2B0A1-G0	6- 91		CHL 3 STATUS FAN IN BIT 01
C0	2B0A0-P3	6- 91		CHL 3 STATUS FAN IN BIT 07
C1	2B0A9-T0	6-101		ENABLE CLEAR TW FINISH FF
C2	2B0A1-G0	6- 89		CHL 2 STATUS FAN IN BIT 01
C3	2B0A3-G0	6- 85		CHL 0 STATUS FAN IN BIT 01
D0	2B0A2-P3	6- 87		CHL 1 STATUS FAN IN BIT 07
D1	2B0A3-P3	6- 85		CHL 0 STATUS FAN IN BIT 07
D2	2B1A5-H2	6- 19		
D3	2B1A5-H3	6- 19		NOT CHAN 3 BUSY TO STATUS FI
E0	2B0A6-S0	6-121		CHL DESIGNATOR BIT 01 TO XLTOR
E1	2B0A6-U3	6-121		CHL DESIGNATOR BIT 00 TO XLTOR
E2	2B1A5-C2	6- 19		NOT CHAN 1 BUSY TO STATUS FI
E3	2B1A5-C3	6- 19		
F0	2B0B0-P3	6- 99		CHL 7 STATUS FAN IN BIT 07
F1	2B0A5-U3	6-123		CHL DESIGNATOR BIT 02 TO XLTOR
F3	2B0B2-G0	6- 95		CHL 5 STATUS FAN IN BIT 01
G0	2B0B1-P3	6- 97		CHL 6 STATUS FAN IN BIT 07
G1	2B0A3-V3	6- 85	2B0A5-AA	CHL 0 EXTERNAL STATUS BIT 11
G2	2B0B0-G0	6- 99		CHL 7 STATUS FAN IN BIT 01
G3	2B0B1-G0	6- 97		CHL 6 STATUS FAN IN BIT 01
H0	2B0B2-P3	6- 95		CHL 5 STATUS FAN IN BIT 07
H1	2B0B3-P3	6- 93		CHL 4 STATUS FAN IN BIT 07
H2	2B0B3-G0	6- 93		CHL 4 STATUS FAN IN BIT 01
H3	2B0A7-W2	6-117	2B0A7-BY	SELECTED STATUS BIT 03 TO TEST
I0	2B0B3-V3	6- 93	2B0A5-AD	CHL 4 EXTERNAL STATUS BIT 11
I1	2B0A7-A3	6-117	2B0A7-BA	SELECTED STATUS BIT 11 TO TEST
I2	2B0A1-S1	6- 89		CHL 2 STATUS FAN IN BIT 03
I3	2B0B1-S1	6- 97		CHL 6 STATUS FAN IN BIT 03
J0	2B0A1-V3	6- 89	2B0A5-AE	CHL 2 EXTERNAL STATUS BIT 11
J1	2B0A9-R1	6-101		SELECT PAUSE FAN IN ODD STATUS
J3	2B0A6-S1	6- 91		CHL 3 STATUS FAN IN BIT 03
K0	2B0A2-V3	6- 87	2B0A5-AF	CHL 1 EXTERNAL STATUS BIT 11
K1	2B0A6-V3	6- 91	2B0A5-BY	CHL 3 EXTERNAL STATUS BIT 11
K2	2B0A2-S1	6- 87		CHL 1 STATUS FAN IN BIT 03
K3	2B0A3-S1	6- 85		CHL 0 STATUS FAN IN BIT 03
L0	2B0B0-V3	6- 99	2B0A5-AH	CHL 7 EXTERNAL STATUS BIT 11
L1	2B0B1-V3	6- 97	2B0A5-AG	CHL 6 EXTERNAL STATUS BIT 11
L2	2B0B0-S1	6- 99		CHL 7 STATUS FAN IN BIT 03
L3	2B0B2-S1	6- 95		CHL 5 STATUS FAN IN BIT 03
M0	2B0A3-V2	6- 85	2B0A5-BX	CHL 0 EXTERNAL STATUS BIT 09
M1	2B0B2-V3	6- 95	2B0A5-AJ	CHL 5 EXTERNAL STATUS BIT 11
M2	2B0B3-S1	6- 93		CHL 4 STATUS FAN IN BIT 03
M3	2B0A8-N1	6-109		SELECTED STATUS BIT 05 TO TEST
N0	2B0A7-F1	6-117	2B0A7-AD	SELECTED STATUS BIT 09 TO TEST
N1	2B0B3-V2	6- 93	2B0A5-AL	CHL 4 EXTERNAL STATUS BIT 09
N3	2B0B1-G3	6- 97		CHAN 6 STATUS FAN-IN - BIT 05
O0	2B0A7-T3	6-117	2B0A7-BQ	SELECTED STATUS BIT 07 TO TEST
O1	2B0A1-V2	6- 89	2B0A5-AT	CHL 2 EXTERNAL STATUS BIT 09
O2	2B0B0-G3	6- 99		CHAN 7 STATUS FAN-IN - BIT 05
O3	2B0A1-G3	6- 89		CHAN 2 STATUS FAN-IN - BIT 05
P0	2B1A6-Q0	6- 5		NOT TW FINISH STATUS BIT 09
P1	2B1A6-Q1	6- 5		
P2	2B0A6-G3	6- 91		CHAN 3 STATUS FAN-IN - BIT 05
P3	2B0A2-G3	6- 87		CHAN 1 STATUS FAN-IN - BIT 05
Q0	2B1A6-T1	6- 13		S/M BFR BUSY TO STATUS FAN-IN
Q1	2B1A6-T0	6- 13		
Q3	2B0A3-G3	6- 85		CHAN 0 STAT FAN-IN - BIT 5
R0	2B0A4-H1	6-103		COMPUTER RUNNING TO FAN OUT
R3	2B0B3-G3	6- 93		CHL 4 STATUS FAN IN BIT 05
S0	2B0B4-H1	6-105		COMPUTER RUNNING TO FAN OUT
S3	2B0A8-I3	6-109		ILL. WRITE TO BIT 05 OF STATUS
T0	2B0A2-V2	6- 87	2B0A5-AX	CHL 1 EXTERNAL STATUS BIT 09
T2	2B0A9-B0	6-101		EN ILLEGAL WRITE TO STATUS 05
T3	2B0B2-G3	6- 95		CHAN 5 STAT FAN-IN - BIT 05
U0	2B0B0-V2	6- 99	2B0A5-BU	CHL 7 EXTERNAL STATUS BIT 09
U1	2B0A6-V2	6- 91	2B0A5-AV	CHL 3 EXTERNAL STATUS BIT 09
U2	2B0A6-F1	6-121		CHL DESIGNATOR BIT 02 TO XLTOR
U3	2B0A5-F1	6-123		CHL DESIGNATOR BIT 02 TO XLTOR
V0	2B0B2-V2	6- 95	2B0A5-BS	CHL 5 EXTERNAL STATUS BIT 09
V1	2B0B1-V2	6- 97	2B0A5-BZ	CHL 6 EXTERNAL STATUS BIT 09
V2	2B1B5-C3	6- 21		
V3	2B1B5-C2	6- 21		NOT CHL 5 BUSY TO STAT FAN-IN
W0	2B1B5-H3	6- 21		NOT CHL 7 BUSY TO STAT FAN-IN
W1	2B1B5-H2	6- 21		
X0	2A1A06P06C-A6			
	1A4A06J18C-A6			
	1C2B3-K0	2- 49		
X1	2A1A06P06C-A5			NOT (GO FF) TO BC
	1A4A06J18C-A5			
	1C2B3-K1	2- 49		
X2	2A1B8-D3	6- 53		NOT CHAN SEL BIT 02 ON 7X
X3	2A1B8-D2	6- 53		

PAGE 6-123



CONTROL DATA	ODD STATUS FAN-IN	PRODUCT	
DEVELOPMENT DIVISION	LOC:2B0A5 PART NO.183987 SER:001	SIZE C / DRAWING NO. 60181000	REV. E
		SHEET	PAGE 6-123

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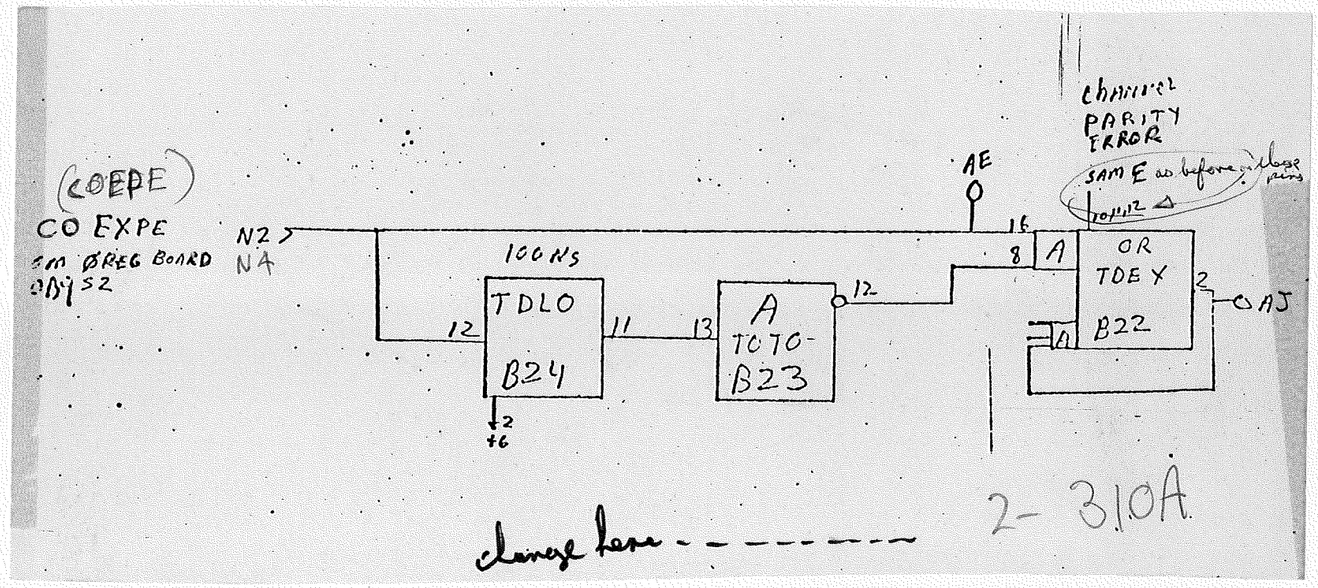
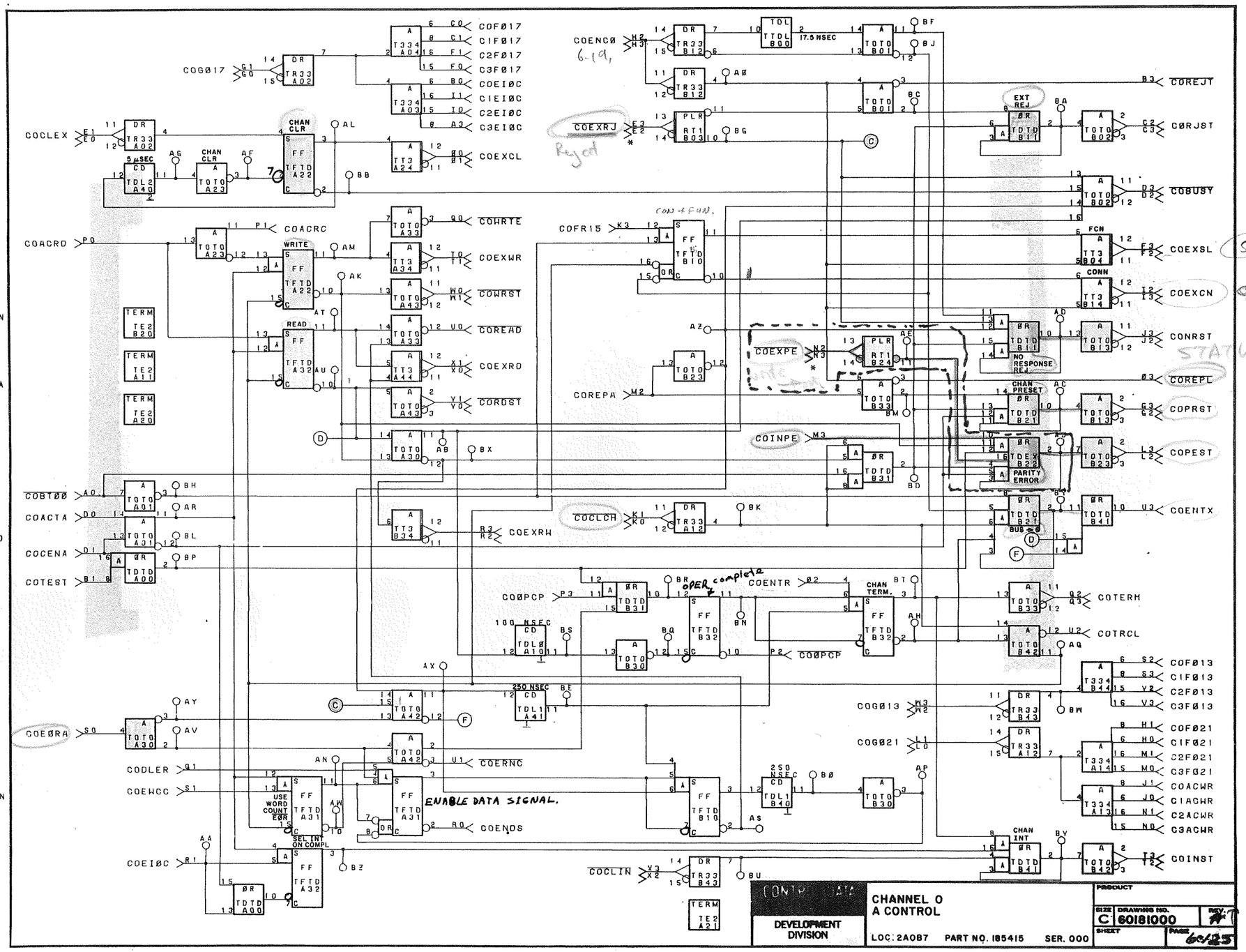
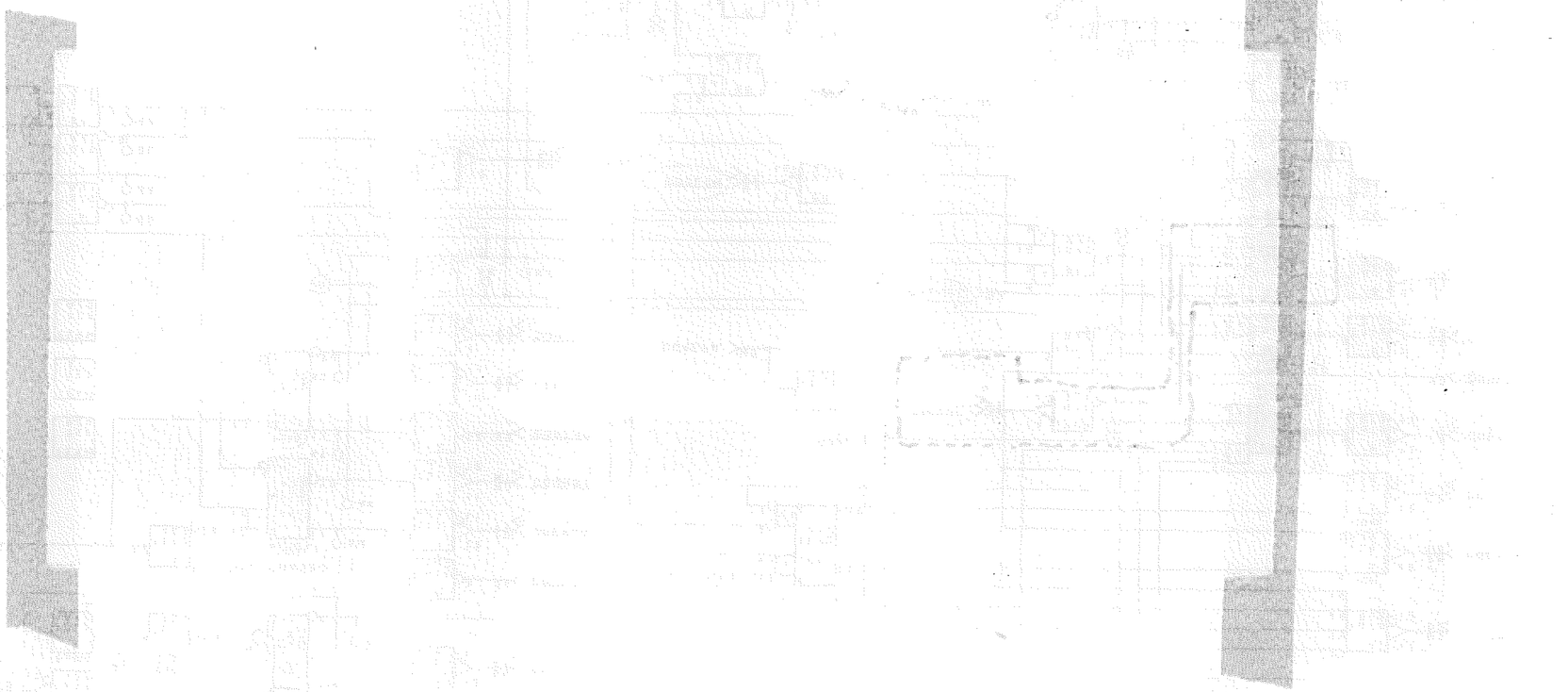
309

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A0A7-T3	6-133		CHL 0 NOT(BUS TO 0) TO CONT A
A3	2A0B2-R1	6-131	2A0B2-AA	CHL 3 EN, INTERRUPT ON COMPL.
B0	2A0B7-R1	6-125	2A0B7-AA	CHL 0 EN, INTERRUPT ON COMPL.
B1	2A0A4-T0	6-157		CHAN 0 TEST OPR COMPL/PE
B3	2A0B5-D3	6-159		CHAN 0 - NOT (EXT REJECT ON CONN + FCN)
C0	2A0B9-G0	6-143	2A0B9-AF	CHL 0 FAN OUT BIT 17 D4 TO OU
C1	2A0B8-G0	6-147	2A0B8-AF	CHL 1 FAN OUT BIT 17 D4 TO OU
C2	2B0A3-N1	6- 85		CHAN 0 EXT REJ STAT TO FAN-IN
C3	2B0A3-N0	6- 85		
D0	2A0B2-C0	6-131		CHL 0 ACTIVATE CHL CONTROL A
D1	2A0A7-F1	6-133		CHL 0 CHANNEL ENABLE TO CONT A
D2	2B1A5-G2	6- 19		NOT CHAN 0 BUSY TO TEST/STATUS
D3	2B1A5-G3	6- 19		
E0	2B0A4-G0	6-103		

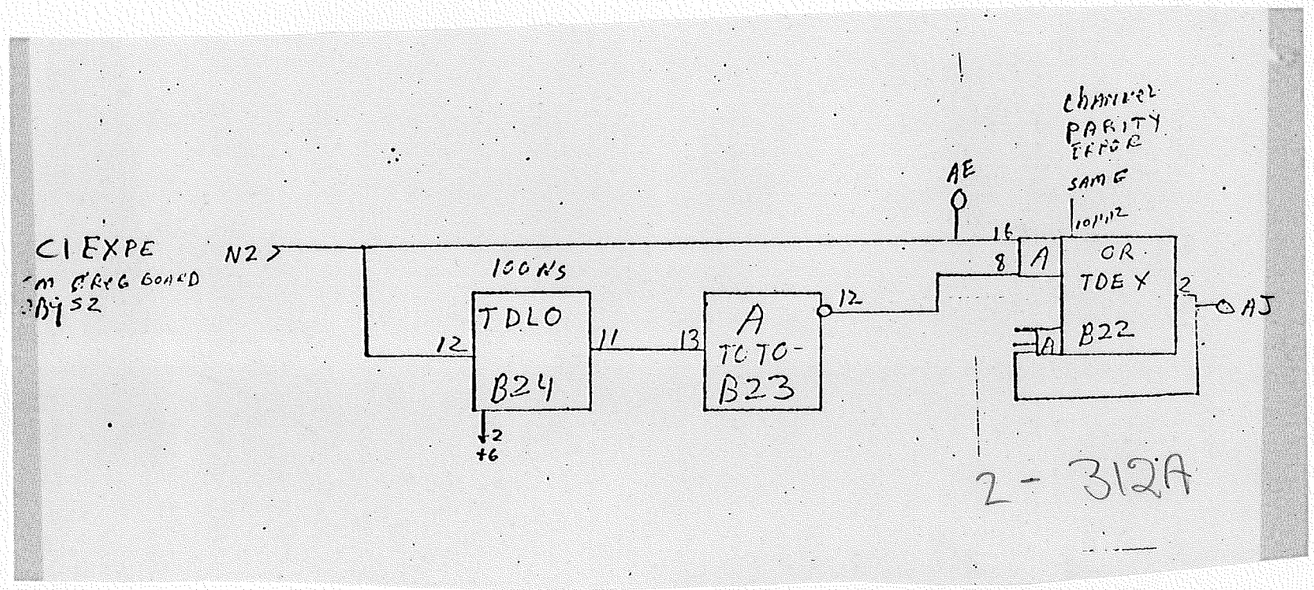

channel
PARITY
ERROR
SAME as before
(COEPE)
CO EXPE
AE
N2
NA
100 NS
TDLO
B24
A
TOTO-
B23
OR
TOEY
B22
AJ
12
11
13
16
8
A
2
+2
+6
change here
2- 310A

E1	2R0A4-G1	6-103		CHL 0 CLEAR CHL AND EXT EQUIP
E2	2A4A01J03E-03			CHL 0 EXTERNAL REJECT SIGNAL
	2A4A01J04E-03			
E3	2A4A01J03E-04			
	2A4A01J04E-04			
F0	2A0B0-G0	6-155	2A0B0-AF	CHL 3 FAN OUT BIT 17 D4 TO OU
F1	2A0B1-G0	6-151	2A0B1-AF	CHL 2 FAN OUT BIT 17 D4 TO OU
F2	2A4A01J03D-08			
	2A4A01J04D-08			
F3	2A4A01J03D-07			CHL 0 EXTERNAL SELECT SIGNAL
	2A4A01J04D-07			
G0	2B1A2-M3	6- 39		
G1	2B1A2-M2	6- 39		D4 BIT 17 TO CHAN 0-3 FANOUT
G2	2R0A3-N3	6- 85		
G3	2R0A3-N2	6- 85		CHL 0 PRESET STATUS TO FAN IN
H0	2A0B8-F3	6-147	2A0B8-RJ	CHL 1 FAN OUT BIT 21 D4 TO OU
H1	2A0B9-F3	6-143	2A0B9-RJ	CHL 0 FAN OUT BIT 21 D4 TO OU
H2	2B1A5-D2	6- 19		
H3	2B1A5-D3	6- 19		
I0	2A0B3-R1	6-129	2A0B3-AA	CHL 2 EN, INTERRUPT ON COMPL.
I1	2A0B6-R1	6-127	2A0B6-AA	CHL 1 EN, INTERRUPT ON COMPL.
I2	2A4A01J03D-05			CHL 0 EXTERNAL CONNECT SIGNAL
	2A4A01J04D-05			
I3	2A4A01J03D-06			
	2A4A01J04D-06			
J0	2A0A6-H1	6-135		CHL 1 ACTIVATE WRITE
J1	2A0A7-H1	6-133		CHL 0 ACTIVATE WRITE
J2	2B0A3-D2	6- 85		
J3	2B0A3-D3	6- 85		CHAN 0 NO RESPONSE STATUS TO FAN-IN
K0	2B0A4-K0	6-103		NOT CHAN 0 CLR CHAN ACTIVITY
K1	2B0A4-K1	6-103		
K3	2A0B3-B0	6-129		CHL 0 FAN OUT D4 FUNCTION XLTN
L0	2B1A4-X3	6- 35		
L1	2B1A4-X2	6- 35		D4 BIT 21 TO CHL 0-3 FAN OUT
L2	2B0A3-D0	6- 85		
L3	2B0A3-D1	6- 85		CHAN 0 PE STATUS = FAN-IN
M0	2A0B0-F3	6-155	2A0B0-RJ	CHL 3 FAN OUT BIT 21 D4 TO OU
M1	2A0B1-F3	6-151	2A0B1-RJ	CHL 2 FAN OUT BIT 21 D4 TO OU
M2	2A0A7-H3	6-133		CHL 0 EXTERNAL REPLY TO CONT A
M3	2A0A7-K0	6-133		CHL 0 INTERNAL PARITY ERROR
N0	2A0A2-H1	6-139		CHL 3 ACTIVATE WRITE
N1	2A0A3-H1	6-137		CHL 2 ACTIVATE WRITE
N2	2A4A01J03E-08			
	2A4A01J04E-08			
N3	2A4A01J03E-07			CHL 0 EXTERNAL PARITY ERROR
	2A4A01J04E-07			
O0	2A4A01J03F-03			CHL 0 CLEAR TO EXTERNAL EQUIP
	2A4A01J04F-03			
O1	2A4A01J03F-04			
	2A4A01J04F-04			
O2	2A0A7-L3	6-133		CHAN 0 ENABLE TERMINATION
O3	2A0A4-D3	6-157		CHAN 0 NOT(REPLY ON CONN/FCN)
P0	2A0B6-J1	6-127		CHL 0 ACTIVATE READ
P1	2A0A7-Q3	6-133		CHL 0 ACTIVATE READ TO CONT C
P2	2A0A7-Q2	6-133		CHAN 0 NOT(OPERATION COMPL FF)
P3	2A0B5-T0	6-159		CHL 0 OPERATION COMPLETE
Q0	2A0A7-P3	6-133		CHL 0 NOT(WRITE) TO CONTROL C
Q1	2A0A7-B3	6-133		CHL 0 DELAYED EOR TO CONT A
Q2	2B0A4-F0	6-103		CHL 0 TERMINATE TO COMMON B
Q3	2B0A4-F1	6-103		
R0	2A0A7-G3	6-133		CHL 0 ENABLE DATA SIGNAL FF
R1	2A0B7-B0	6-125	2A0B7-AA	CHL 0 EN, INTERRUPT ON COMPL.
R2	2A4A01J03C-08			
	2A4A01J04C-08			
R3	2A4A01J03C-07			CHL 0 EXTERNAL BUSY SIGNAL
	2A4A01J04C-07			
S0	2A0A7-K3	6-133		CHL 0 END OF RECORD TO CONT A
S1	2A0B2-J1	6-131		CHL 0 EN WORD COUNT CONTROL
S2	2A0B9-G1	6-143	2A0B9-AE	CHL 0 FAN OUT BIT 13 D4 TO OU
S3	2A0B8-G1	6-147	2A0B8-AE	CHL 1 FAN OUT BIT 13 D4 TO OU
T0	2A4A01J03D-03			CHL 0 EXTERNAL WRITE SIGNAL
	2A4A01J04D-03			
T1	2A4A01J03D-04			
	2A4A01J04D-04			
T2	2R0A3-O2	6- 85		
T3	2R0A3-O3	6- 85		CHAN 0 INT TO STATUS FAN-IN
U0	2A0A7-F3	6-133		CHL 0 NOT(READ) TO CONTROL C
U1	2A0A7-E1	6-133		CHAN 0 NOT(END OF RECORD) + WORD COUNT CONTROL
U2	2A0A7-K1	6-133		CHL 0 TERMINATE OR CLEAR
U3	2A0A7-U0	6-133		CHL 0 ENABLE O REG. XMSN
V0	2B0A3-E0	6- 85		NOT CHAN 0 READ STAT TO FAN-IN
V1	2B0A3-E1	6- 85		
V2	2A0B1-G1	6-151	2A0B1-AE	CHL 2 FAN OUT BIT 13 D4 TO OU
V3	2A0B0-G1	6-155	2A0B0-AE	CHL 3 FAN OUT BIT 13 D4 TO OU
W0	2R0A3-O1	6- 85		
W1	2R0A3-O0	6- 85		NOT CHAN 0 WRITE STAT TO FI
W2	2B1B3-M3	6- 31		
W3	2B1B3-M2	6- 31		D4 BIT 13 TO CHL 0-3 FAN OUT
X0	2A4A01J03D-02			
	2A4A01J04D-02			
X1	2A4A01J03D-01			CHL 0 EXTERNAL READ SIGNAL
	2A4A01J04D-01			
X2	2R0A4-B0	6-103		NOT CHAN 0 CLR CHAN INTERRUPT
X3	2R0A4-B1	6-103		

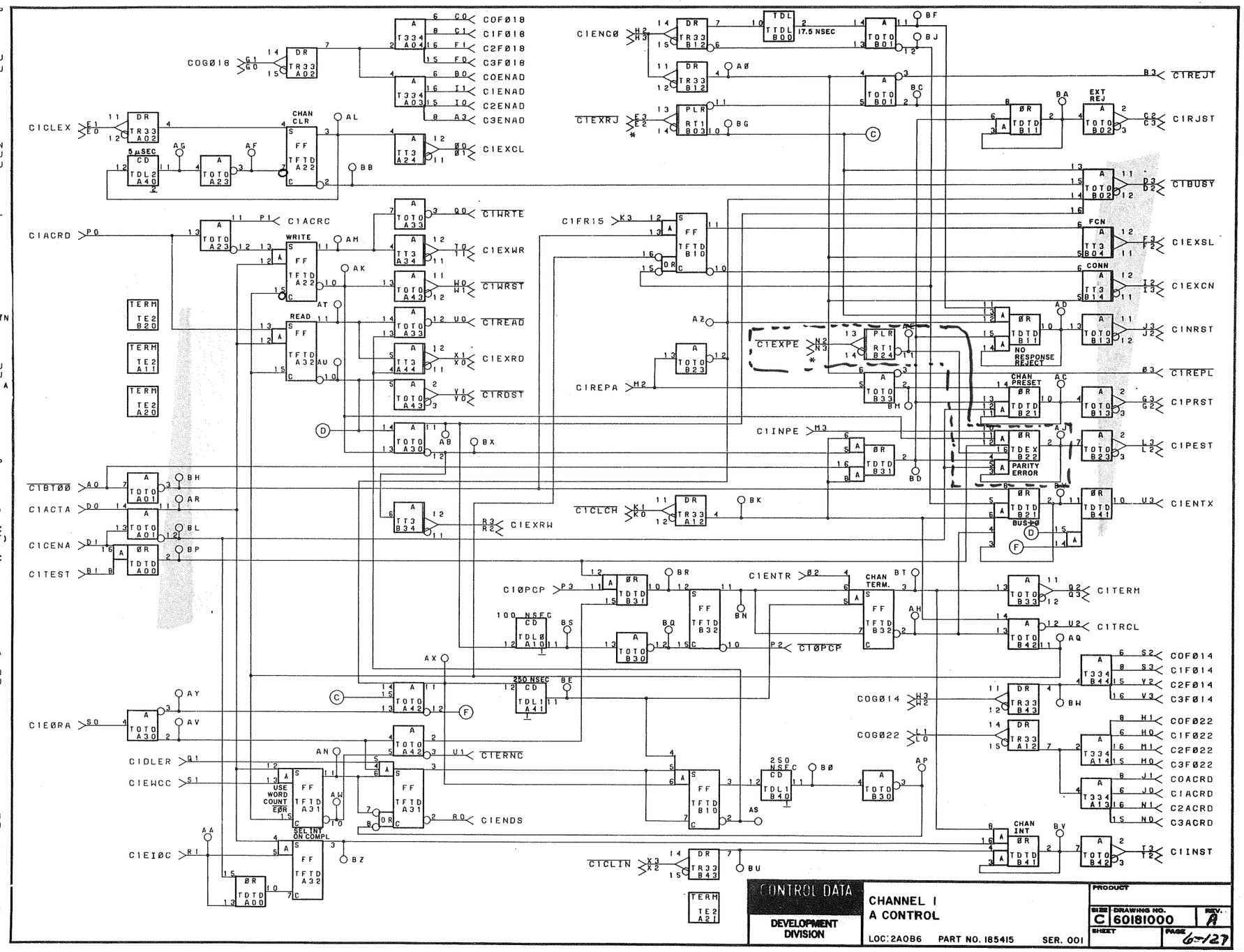


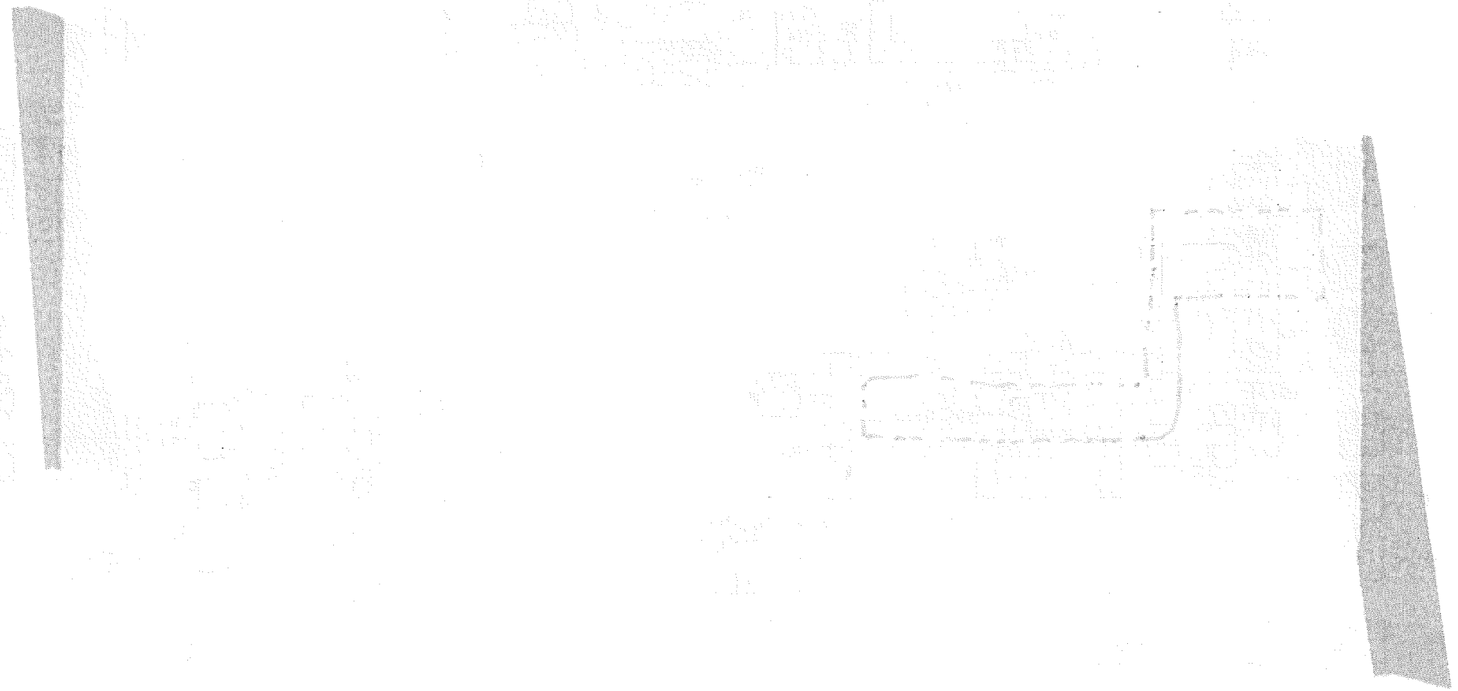


PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A0A6-T3	6-135		CHL 1 NOT(BUS TO 0) TO CONT A
A3	2A0A2-G1	6-139		CHL 3 ENABLE ASSY/DISASSY
B0	2A0A7-G1	6-133		CHL 0 ENABLE ASSY/DISASSY
B1	2A0A4-U1	6-157		CHAN 1 TEST OPR COMPL/PE
B3	2A0B5-E2	6-159		CHAN 1 NOT (EXT REJECT ON CONN + FCN)
C0	2A0B9-J3	6-143	2A0B9-BZ	CHL 0 FAN OUT BIT 18 D4 TO OU
C1	2A0B8-J3	6-147	2A0B8-BZ	CHL 1 FAN OUT BIT 18 D4 TO OU
C2	2R0A2-N1	6- 87		CHAN 1 EXT REJ STAT TO FAN-IN
C3	2R0A2-N0	6- 87		
D0	2A0B2-C1	6-131		CHL 1 ACTIVATE CHL CONTROL A
D1	2A0A6-F1	6-135		CHL 1 CHANNEL ENABLE TO CONT A
D2	2B1A5-F2	6- 19		NOT CHAN 1 BUSY TO TEST/STATUS
D3	2B1A5-F3	6- 19		
E0	2B0A4-01	6-103		

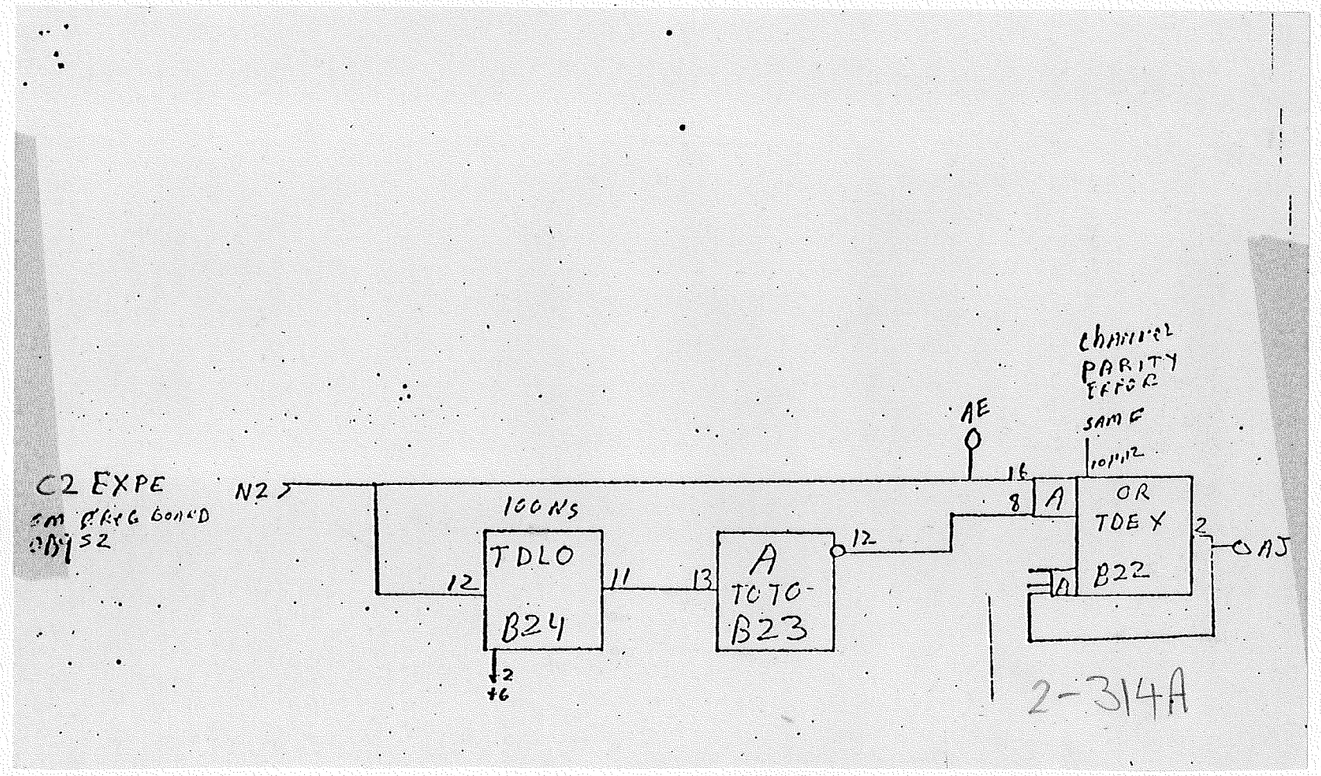

CHANNEL PARITY ERROR
SAM G
10/11/12
AE
CI EXPE
M REG BOARD
B52
N2
100 NS
TDLO
B24
12
11
13
A
TO TO-
B23
12
16
8
A
OR
TDE X
B22
2
AJ
2
+6
2 - 312A

E1	2B0A4-00	6-103		CHL 1 CLEAR CHL AND EXT EQUIP
E2	2A4A02J03E-03			CHL 1 EXTERNAL REJECT SIGNAL
	2A4A02J04E-03			
E3	2A4A02J03E-04			
	2A4A02J04E-04			
F0	2A0B0-J3	6-155	2A0B0-RZ	CHL 3 FAN OUT BIT 18 D4 TO OU
F1	2A0B1-J3	6-151	2A0B1-RZ	CHL 2 FAN OUT BIT 18 D4 TO OU
F2	2A4A02J03D-08			
	2A4A02J04D-08			
F3	2A4A02J03D-07			CHL 1 EXTERNAL SELECT SIGNAL
	2A4A02J04D-07			
G0	2B1B4-X3	6- 29		
G1	2B1B4-X2	6- 29		D4 BIT 18 TO CHL 0-3 FAN OUT
G2	2B0A2-N3	6- 87		
G3	2B0A2-N2	6- 87		CHL 1 PRESET STATUS TO FAN IN
H0	2A0B8-F2	6-147	2A0B8-RO	CHL 1 FAN OUT BIT 22 D4 TO OU
H1	2A0B9-F2	6-143	2A0B9-RO	CHL 0 FAN OUT BIT 22 D4 TO OU
H2	2B1A5-E3	6- 19		EN CHAN 1 CONN + FCN CONT
H3	2B1A5-E2	6- 19		
I0	2A0A3-G1	6-137		
I1	2A0A6-G1	6-135		CHL 2 ENABLE ASSY/DISASSY
				CHL 1 ENABLE ASSY/DISASSY
I2	2A4A02J03D-05			CHL 1 EXTERNAL CONNECT SIGNAL
	2A4A02J04D-05			
I3	2A4A02J03D-06			
	2A4A02J04D-06			
J0	2A0B6-P0	6-127		CHL 1 ACTIVATE READ
J1	2A0B7-P0	6-125		CHL 0 ACTIVATE READ
J2	2B0A2-D2	6- 87		
J3	2B0A2-D3	6- 87		CHAN 1 NO RESPONSE STATUS TO FAN-IN
K0	2B0A4-V0	6-103		NOT CHAN 1 CLR CHAN ACTIVITY
K1	2B0A4-V1	6-103		
K3	2A0B3-I1	6-129		CHL 1 FAN OUT D4 FUNCTION XLTN
L0	2B1A3-X3	6- 37		
L1	2B1A3-X2	6- 37		D4 BIT 22 TO CHL 0-3 FAN OUT
L2	2B0A2-D0	6- 87		
L3	2B0A2-D1	6- 87		CHAN 1 PE STATUS + FAN-IN
M0	2A0B0-F2	6-155	2A0B0-RO	CHL 3 FAN OUT BIT 22 D4 TO OU
M1	2A0B1-F2	6-151	2A0B1-RO	CHL 2 FAN OUT BIT 22 D4 TO OU
M2	2A0A6-H3	6-135		CHL 1 EXTERNAL REPLY TO CONT A
M3	2A0A6-K0	6-135		CHL 1 INTERNAL PARITY ERROR
N0	2B0B2-P0	6-131		CHL 3 ACTIVATE READ
N1	2A0B3-P0	6-129		CHL 2 ACTIVATE READ
N2	2A4A02J03E-08			
	2A4A02J04E-08			
N3	2A4A02J03E-07			CHL 1 EXTERNAL PARITY ERROR
	2A4A02J04E-07			
O0	2A4A02J03F-03			CHL 1 CLEAR TO EXTERNAL EQUIP
	2A4A02J04F-03			
O1	2A4A02J03F-04			
	2A4A02J04F-04			
O2	2A0A6-L3	6-135		CHL 1 ENABLE TERMINATION
O3	2A0A4-E2	6-157		CHL 1 NOT(RPLY ON CONN/FUNC)
P0	2A0B6-J0	6-127		CHL 1 ACTIVATE READ
P1	2A0A6-Q3	6-135		CHL 1 ACTIVATE READ TO CONT C
P2	2A0A6-Q2	6-135		CHL 1 NOT(OPERATION COMPL F/F)
P3	2A0B5-U1	6-159		CHL 1 OPERATION COMPLETE
Q0	2A0A6-P3	6-135		CHL 1 NOT(WRITE) TO CONTROL C
Q1	2A0A6-B3	6-135		CHL 1 DELAYED EOR TO CONT A
Q2	2B0A4-R0	6-103		CHL 1 TERMINATE TO COMMON B
Q3	2B0A4-R1	6-103		
R0	2A0A6-G3	6-135		CHL 1 ENABLE DATA SIGNAL FF
R1	2A0B7-I1	6-125	2A0B6-AA	CHL 1 EN, INTERRUPT ON COMPL,
R2	2A4A02J03C-08			
	2A4A02J04C-08			
R3	2A4A02J03C-07			CHL 1 EXTERNAL BUSY SIGNAL
	2A4A02J04C-07			
S0	2A0A6-K3	6-135		CHL 1 END OF RECORD TO CONT A
S1	2A0B2-J0	6-131		CHL 1 EN WORD COUNT CONTROL
S2	2A0B9-K0	6-143	2A0B9-AR	CHL 0 FAN OUT BIT 14 D4 TO OU
S3	2A0B8-K0	6-147	2A0B8-AR	CHL 1 FAN OUT BIT 14 D4 TO OU
T0	2A4A02J03D-03			CHL 1 EXTERNAL WRITE SIGNAL
	2A4A02J04D-03			
T1	2A4A02J03D-04			
	2A4A02J04D-04			
T2	2B0A2-02	6- 87		
T3	2B0A2-03	6- 87		CHAN 1 INT TO STATUS FAN-IN
U0	2A0A6-F3	6-135		CHL 1 NOT(READ) TO CONTROL C
U1	2A0A6-E1	6-135		CHAN 1 NOT(END OF RECORD) + WORD COUNT CONTROL
U2	2A0A6-K1	6-135		CHL 1 TERMINATE OR CLEAR
U3	2A0A6-U0	6-135		CHL 1 ENABLE O REG XMISSION
V0	2B0A2-E0	6- 87		NOT CHAN 1 READ STATUS TO FI
V1	2B0A2-E1	6- 87		
V2	2A0B1-K0	6-151	2A0B1-AR	CHL 2 FAN OUT BIT 14 D4 TO OU
V3	2A0B0-K0	6-155	2A0B0-AR	CHL 3 FAN OUT BIT 14 D4 TO OU
W0	2B0A2-01	6- 87		
W1	2B0A2-00	6- 87		NOT CHAN 1 WRITE STATUS TO FI
W2	2B1B2-M3	6- 33		
W3	2B1B2-M2	6- 33		D4 BIT 14 TO CHAN 0-3 FANOUT
X0	2A4A02J03D-02			
	2A4A02J04D-02			
X1	2A4A02J03D-01			CHL 1 EXTERNAL READ SIGNAL
	2A4A02J04D-01			
X2	2B0A4-U0	6-103		NOT CHAN 1 CLR CHAN INTERRUPT
X3	2B0A4-U1	6-103		

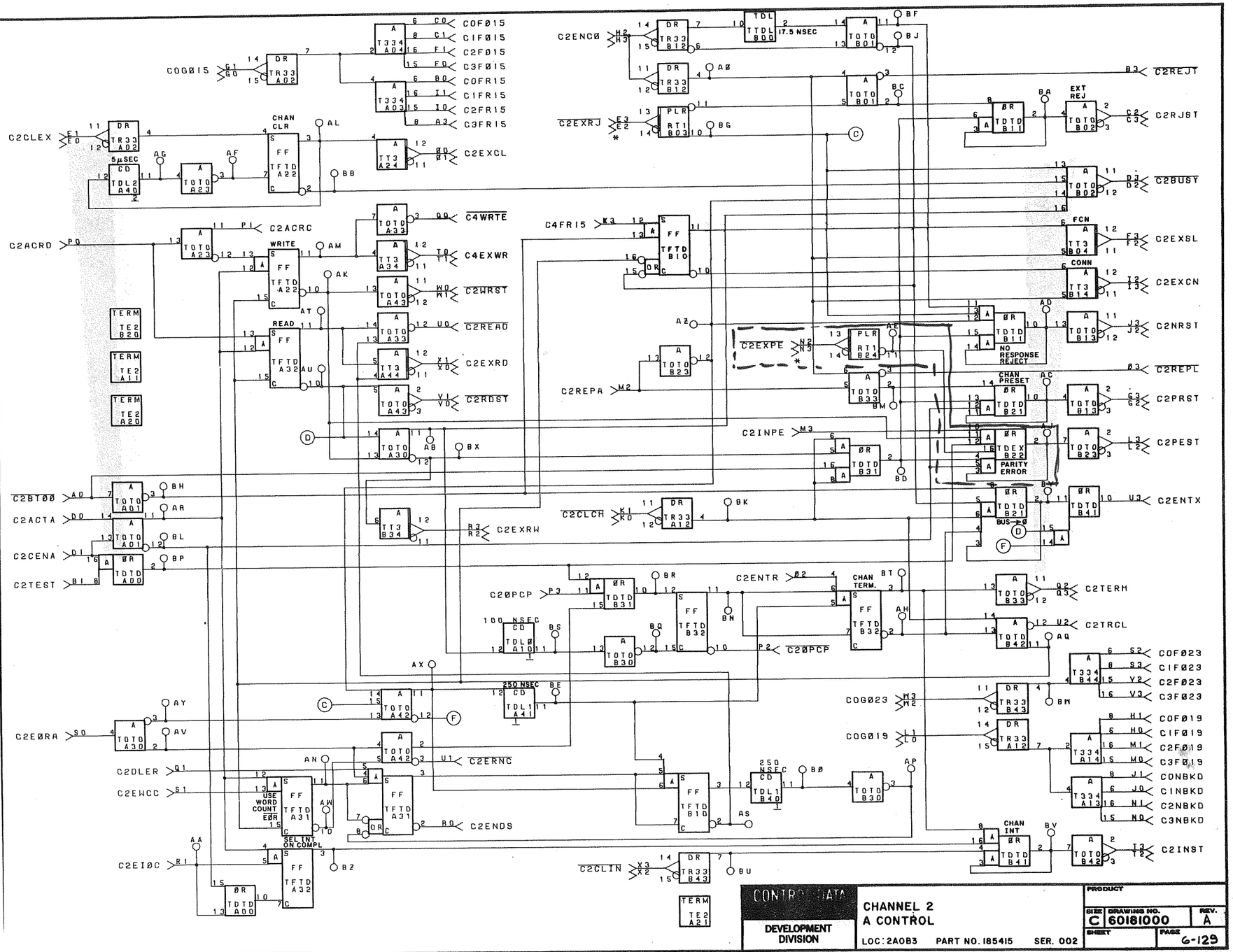




PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A0A3-T3	6-137		CHL 2 NOT(BUS TO 0) TO CONT A
A3	2A0B2-K3	6-131		CHL 3 FAN OUT D4 FUNCTION XLTN
B0	2A0B7-K3	6-125		CHL 0 FAN OUT D4 FUNCTION XLTN
B1	2A0A4-U0	6-157		CHAN 2 TEST OPR COMPL/PE
B3	2A0B5-E3	6-159		CHAN 2 NOT (EXT REJECT ON CONN + FCN)
C0	2A0B9-H1	6-143	2A0B9-AG	CHL 0 FAN OUT BIT 15 D4 TO OU
C1	2A0B8-H1	6-147	2A0B8-AG	CHL 1 FAN OUT BIT 15 D4 TO OU
C2	2R0A1-N1	6- 89		CHAN 2 EXT REJ STAT TO FAN-IN
C3	2R0A1-N0	6- 89		
D0	2A0B2-F1	6-131		CHL 2 ACTIVATE CHL CONTROL A
D1	2A0A3-F1	6-137		CHL 2 CHANNEL ENABLE TO CONT A
D2	2R1A5-M3	6- 19		NOT CHAN 2 BUSY TO TEST/STATUS
D3	2R1A5-M2	6- 19		
E0	2R0A4-G0	6-105		

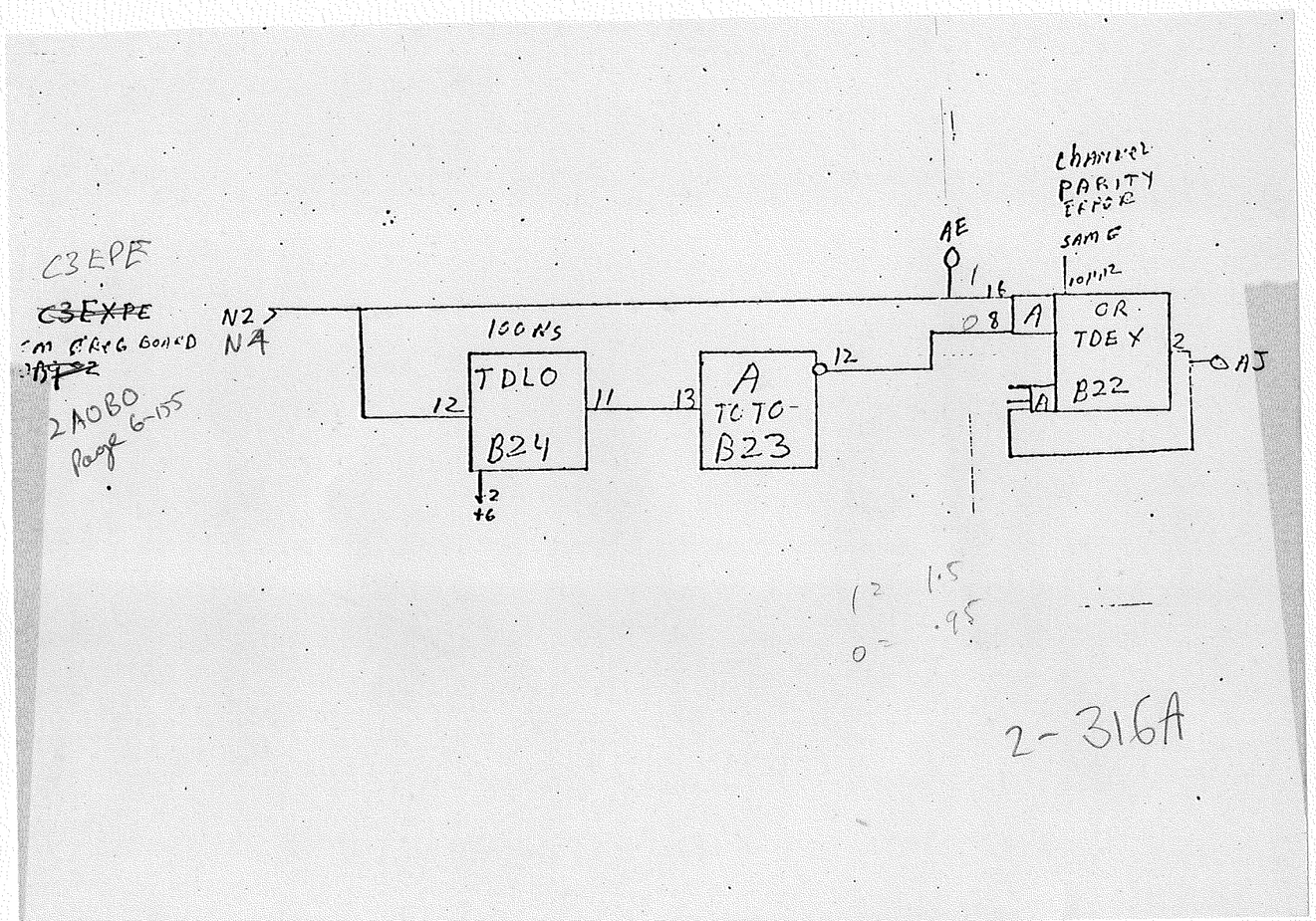

C2 EXPE
SM REG BOARD
BY SZ
N27
100 NS
TDLO
B24
12
11
13
A
TOTO-
B23
12
AE
16
8
A
OR
TDEX
B22
2
AJ
CHANNEL
PARITY
ERROR
SAME
10*11*12
2
TO
2-314A

E1	2B0B4-G1	6-105		CHL 2 CLEAR CHL AND EXT EQUIP
E2	2A4A03J03E-03			CHL 2 EXTERNAL REJECT SIGNAL
	2A4A03J04E-03			
E3	2A4A03J03E-04			
	2A4A03J04E-04			
F0	2A0B0-H1	6-155	2A0B0-AG	CHL 3 FAN OUT BIT 15 D4 TO OU
F1	2A0B1-H1	6-151	2A0B1-AG	CHL 2 FAN OUT BIT 15 D4 TO OU
F2	2A4A03J03D-08			
	2A4A03J04D-08			
F3	2A4A03J03D-07			CHL 2 EXTERNAL SELECT SIGNAL
	2A4A03J04D-07			
G0	2B1A4-H3	6- 35		
G1	2B1A4-H2	6- 35		D4 BIT 15 TO CHAN 0-3 FANOUT
G2	2B0A1-N3	6- 89		
G3	2B0A1-N2	6- 89		CHL 2 PRESET STATUS TO FAN IN
H0	2A0B8-E3	6-147	2A0B8-RE	CHL 1 FAN OUT BIT 19 D4 TO OU
H1	2A0B9-E3	6-143	2A0B9-RE	CHL 0 FAN OUT BIT 19 D4 TO OU
H2	2B1A5-J2	6- 19		EN CHAN 2 CONN + FCN CONTROL
H3	2B1A5-J3	6- 19		
I0	2A0B3-K3	6-129		CHL 2 FAN OUT D4 FUNCTION XLTN
I1	2A0B6-K3	6-127		CHL 1 FAN OUT D4 FUNCTION XLTN
I2	2A4A03J03D-05			CHL 2 EXTERNAL CONNECT SIGNAL
	2A4A03J04D-05			
I3	2A4A03J03D-06			
	2A4A03J04D-06			
J0	2A0A6-G0	6-135		CHL 1 FORWARD ASSY/DISASSY
J1	2A0A7-G0	6-133		CHL 0 FORWARD ASSY/DISASSY
J2	2B0A1-D2	6- 89		
J3	2B0A1-D3	6- 89		CHAN 2 NO RESPONSE STATUS TO FAN-IN
				NOT CHAN 2 CLR CHAN ACTIVITY
K0	2B0B4-K0	6-105		
K1	2B0B4-K1	6-105		CHL 2 FAN OUT D4 FUNCTION XLTN
K3	2A0B3-I0	6-129		
L0	2B1B3-X3	6- 31		
L1	2B1B3-X2	6- 31		D4 BIT 19 TO CHL 0-3 FAN OUT
L2	2B0A1-D0	6- 89		
L3	2B0A1-D1	6- 89		CHAN 2 PE STATUS + FAN-IN
M0	2A0B0-E3	6-155	2A0B0-RE	CHL 3 FAN OUT BIT 19 D4 TO OU
M1	2A0B1-E3	6-151	2A0B1-RE	CHL 2 FAN OUT BIT 19 D4 TO OU
M2	2A0A3-H3	6-137		CHL 2 EXTERNAL REPLY TO CONT A
M3	2A0A3-K0	6-137		CHL 2 INTERNAL PARITY ERROR
N0	2A0A2-G0	6-139		CHL 3 FORWARD ASSY/DISASSY
N1	2A0A3-G0	6-137		CHL 2 FORWARD ASSY/DISASSY
N2	2A4A03J03E-08			
	2A4A03J04E-08			CHL 2 EXTERNAL PARITY ERROR
N3	2A4A03J03E-07			
	2A4A03J04E-07			CHL 2 CLEAR TO EXTERNAL EQUIP
O0	2A4A03J03F-03			
	2A4A03J04F-03			
O1	2A4A03J03F-04			
	2A4A03J04F-04			
O2	2A0A3-L3	6-137		CHL 2 ENABLE TERMINATION
O3	2A0A4-E3	6-157		CHL 2 NOT(RPLY ON CONN/FUNC)
P0	2A0B6-N1	6-127		CHL 2 ACTIVATE READ
P1	2A0A3-03	6-137		CHL 2 ACTIVATE READ TO CONT C
P2	2A0A3-02	6-137		CHL 2 NOT(OPERATION COMPL F/F)
P3	2A0B5-U0	6-159		CHL 2 OPERATION COMPLETE
Q0	2A0A3-P3	6-137		CHL 2 NOT(WRITE) TO CONTROL C
Q1	2A0A3-B3	6-137		CHL 2 DELAYED EOR TO CONT A
Q2	2B0B4-F0	6-105		CHL 2 TERMINATE TO COMMON B
Q3	2B0B4-F1	6-105		
R0	2A0A3-G3	6-137		CHL 2 ENABLE DATA SIGNAL FF
R1	2A0B7-I0	6-125	2A0B3-AA	CHL 2 EN. INTERRUPT ON COMPL+
R2	2A4A03J03C-08			
	2A4A03J04C-08			
R3	2A4A03J03C-07			CHL 2 EXTERNAL BUSY SIGNAL
	2A4A03J04C-07			
S0	2A0A3-K3	6-137		CHL 2 END OF RECORD TO CONT A
S1	2A0B2-N1	6-131		CHL 2 EN WORD COUNT CONTROL
S2	2A0B9-E2	6-143	2A0B9-BH	CHL 0 FAN OUT BIT 23 D4 TO OU
S3	2A0B8-E2	6-147	2A0B8-BH	CHL 1 FAN OUT BIT 23 D4 TO OU
T0	2A4A03J03D-03			CHL 2 EXTERNAL WRITE SIGNAL
	2A4A03J04D-03			
T1	2A4A03J03D-04			
	2A4A03J04D-04			
T2	2B0A1-02	6- 89		
T3	2B0A1-03	6- 89		CHAN 2 INT TO STATUS + FAN-IN
U0	2A0A3-F3	6-137		CHL 2 NOT(READ) TO CONTROL C
U1	2A0A3-E1	6-137		CHAN 2 NOT(END OF RECORD) + WORD COUNT CONTROL
U2	2A0A3-K1	6-137		CHL 2 TERMINATE OR CLEAR
U3	2A0A3-U0	6-137		CHL 2 ENABLE D REG XMISSION
V0	2B0A1-E0	6- 89		NOT CHAN 2 READ STATUS TO FI
V1	2B0A1-E1	6- 89		
V2	2A0B1-E2	6-151	2A0B1-RH	CHL 2 FAN OUT BIT 23 D4 TO OU
V3	2A0B0-E2	6-155	2A0B0-BH	CHL 3 FAN OUT BIT 23 D4 TO OU
W0	2B0A1-01	6- 89		NOT CHAN 2 WRITE STATUS TO FI
W1	2B0A1-00	6- 89		
W2	2B1A2-X3	6- 39		D4 BIT 23 TO CHL 0-3 FAN OUT
W3	2B1A2-X2	6- 39		
X0	2A4A03J03D-02			
	2A4A03J04D-02			CHL 2 EXTERNAL READ SIGNAL
X1	2A4A03J03D-01			
	2A4A03J04D-01			NOT CHAN 2 CLR CHAN INTERRUPT
X2	2B0B4-B0	6-105		
X3	2B0B4-B1	6-105		

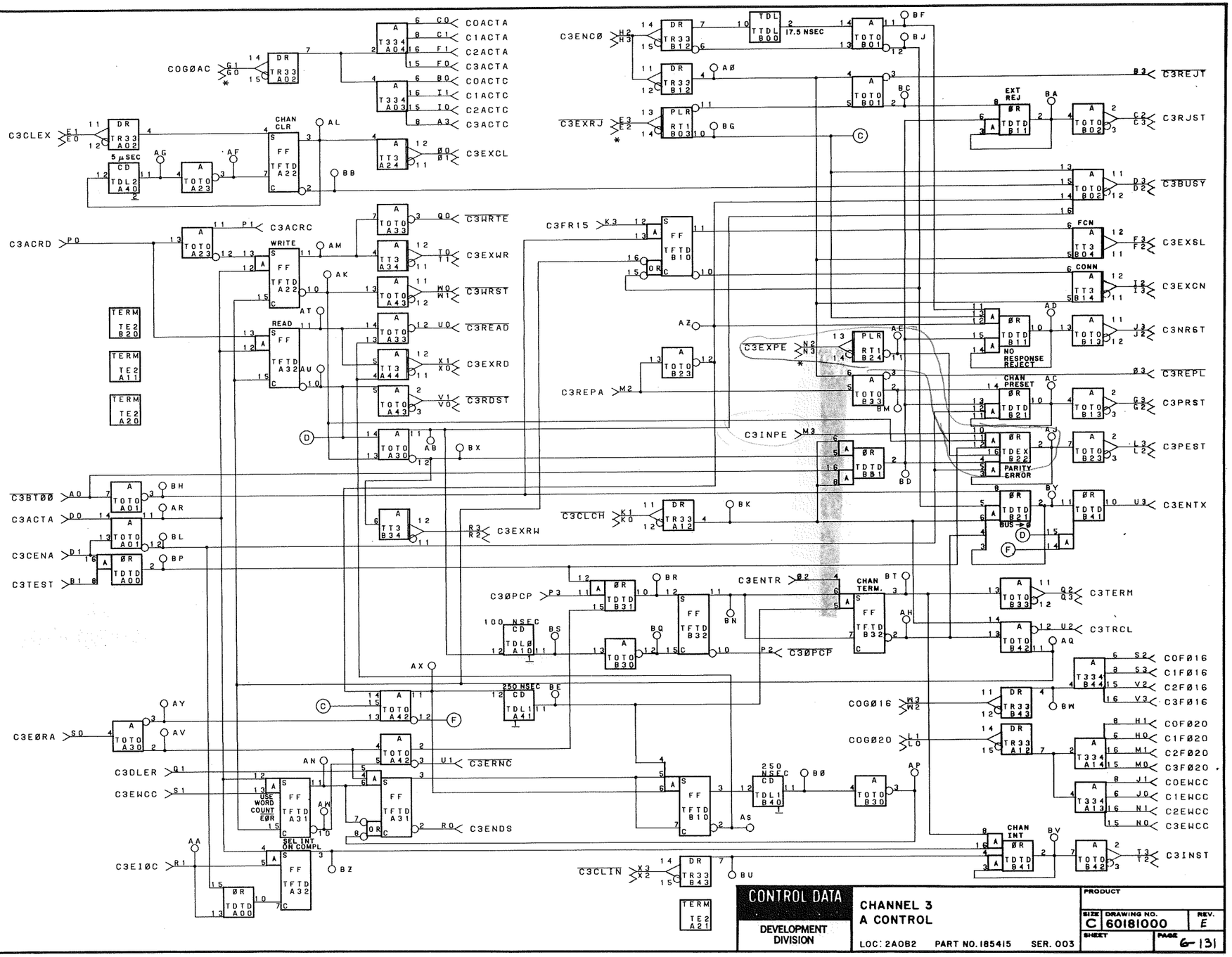


315

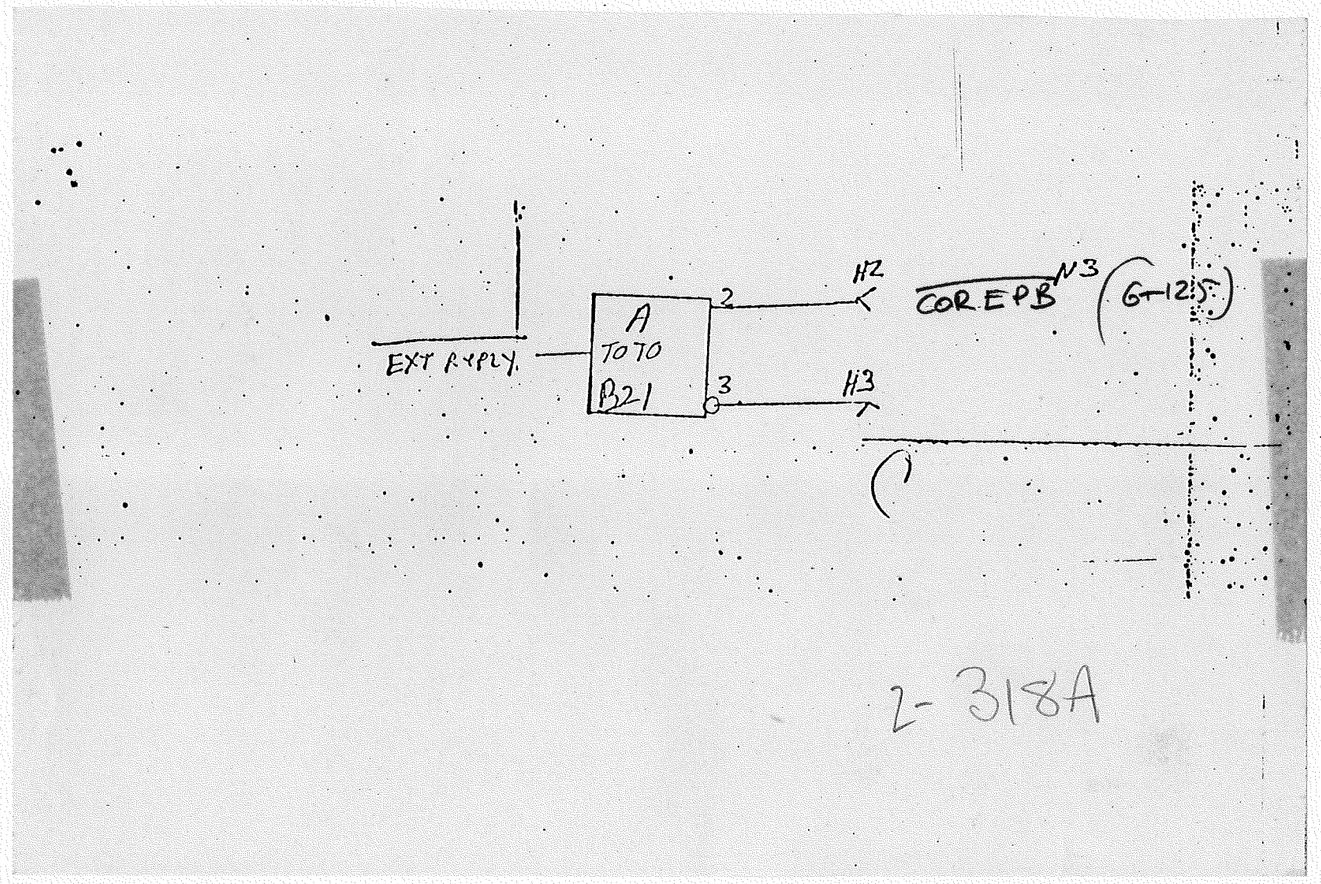
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A0A2-T3	6-139		CHL 3 NOT(BUS TO 0) TO CONT A
A3	2A0A2-N1	6-139		CHL 3 ACTIVATE CHL CONTROL C
B0	2A0A7-N1	6-133		CHL 0 ACTIVATE CHL CONTROL C
B1	2A0A4-T1	6-137		CHAN 3 TEST OPR COMPL/PE
B3	2A0B5-G2	6-159		CHAN 3 NOT(EXT REJECT ON CONN + FCN
C0	2A0B7-D0	6-125		CHL 0 ACTIVATE CHL CONTROL A
C1	2A0B6-D0	6-127		CHL 1 ACTIVATE CHL CONTROL A
C2	2B0A0-N1	6- 91		CHAN 3 EXT REJ STAT TO FAN-IN
C3	2B0A0-N0	6- 91		
D0	2A0B2-F0	6-131		CHL 3 ACTIVATE CHL CONTROL A
D1	2A0A2-F1	6-139		CHL 3 CHANNEL ENABLE TO CONT A
D2	2B1A5-L2	6- 19		NOT CHAN 3 BUSY TO TEST/STATUS
D3	2B1A5-L3	6- 19		
E0	2B0B4-01	6-105		


C3EPE
C3EXPE
2A0B0
Page 6-155
N27
N4
100NS
TDLO
B24
A
TC TO-
B23
12
11
13
12
AE
1
16
8
A
CR
TDEX
B22
2
AJ
CHANNEL
PARITY
ERROR
SAME
10,11,12
1=
1.5
0=
.95
2-316A

E1	2BAB4-00	6-105		CHL 3 CLEAR CHL AND EXT EQUIP
E2	2A4A04J03E-03			CHL 3 EXTERNAL REJECT SIGNAL
	2A4A04J04E-03			
E3	2A4A04J03E-04			
	2A4A04J04E-04			
F0	2AAB2-00	6-131		CHL 3 ACTIVATE CHL CONTROL A
F1	2AAB3-00	6-129		CHL 2 ACTIVATE CHL CONTROL A
F2	2A4A04J03D-08			
	2A4A04J04D-08			
F3	2A4A04J03D-07			CHL 3 EXTERNAL SELECT SIGNAL
	2A4A04J04D-07			
G0	2B1A6-S1	6- 13		ACT. I/O TO CHAN 0-3 FANOUT
G1	2B1A6-S0	6- 13		
G2	2BAA0-N3	6- 91		
G3	2BAA0-N2	6- 91		CHL 3 PRESET STATUS TO FAN IN
H0	2AAB8-I3	6-147	2A0B8-BW	CHL 1 FAN OUT BIT 20 D4 TO OU
H1	2AAB9-I3	6-143	2A0B9-BW	CHL 0 FAN OUT BIT 20 D4 TO OU
H2	2B1A5-K3	6- 19		
H3	2B1A5-K2	6- 19		
I0	2AAA3-N1	6-137		CHL 2 ACTIVATE CHL CONTROL C
I1	2AAA6-N1	6-135		CHL 1 ACTIVATE CHL CONTROL C
I2	2A4A04J03D-05			CHL 3 EXTERNAL CONNECT SIGNAL
	2A4A04J04D-05			
I3	2A4A04J03D-06			
	2A4A04J04D-06			
J0	2AAB6-S1	6-127		CHL 1 EN WORD COUNT CONTROL
J1	2AAB7-S1	6-125		CHL 0 EN WORD COUNT CONTROL
J2	2BAA0-D2	6- 91		
J3	2BAA0-D3	6- 91		CHAN 3 NO RESPONSE STATUS TO FAN-IN
K0	2BAB4-V0	6-105		NOT CHAN 3 CLR CHAN ACTIVITY
K1	2BAB4-V1	6-105		
K2	2AAB3-A3	6-129		CHL 3 FAN OUT D4 FUNCTION XLTN
L0	2B1B2-K3	6- 33		
L1	2B1B2-K2	6- 33		D4 BIT 20 TO CHAN 0-3 FANOUT
L2	2BAA0-D0	6- 91		
L3	2BAA0-D1	6- 91		CHAN 3 PE STATUS - FAN-IN
M0	2A0B0-I3	6-155	2A0B0-BW	CHL 3 FAN OUT BIT 20 D4 TO OU
M1	2AAB1-I3	6-151	2A0B1-BW	CHL 2 FAN OUT BIT 20 D4 TO OU
M2	2AAA2-H3	6-139		CHL 3 EXTERNAL REPLY TO CONT A
M3	2AAA2-K0	6-139		CHL 3 INTERNAL PARITY ERROR
N0	2AAB2-S1	6-131		CHL 3 EN WORD COUNT CONTROL
N1	2AAB3-S1	6-129		CHL 2 EN WORD COUNT CONTROL
N2	2A4A04J03E-08			
	2A4A04J04E-08			
N3	2A4A04J03E-07			CHL 3 EXTERNAL PARITY ERROR
	2A4A04J04E-07			
O0	2A4A04J03F-03			CHL 3 CLEAR TO EXTERNAL EQUIP
	2A4A04J04F-03			
O1	2A4A04J03F-04			
	2A4A04J04F-04			
O2	2AAA2-L3	6-139		CHL 3 ENABLE TERMINATION
O3	2AAA4-G2	6-157		CHL 3 NOT(REPLY ON CONN/FUNC)
P0	2AAB6-N0	6-127		CHL 3 ACTIVATE READ
P1	2AAA2-Q3	6-139		CHL 3 ACTIVATE READ TO CONT C
P2	2AAA2-Q2	6-139		CHL 3 NOT(OPERATION COMPL F/F)
P3	2AAB5-T1	6-159		CHL 3 OPERATION COMPLETE
Q0	2AAA2-P3	6-139		CHL 3 NOT(WRITE) TO CONTROL C
Q1	2AAA2-B3	6-139		CHL 3 DELAYED EOR TO CONT A
Q2	2BAB4-R0	6-105		CHL 3 TERMINATE TO COMMON B
Q3	2BAB4-R1	6-105		
R0	2AAA2-G3	6-139		
R1	2AAB7-A3	6-125	2A0B2-AA	CHL 3 EN. INTERRUPT ON COMPL.
R2	2A4A04J03C-08			
	2A4A04J04C-08			
R3	2A4A04J03C-07			CHL 3 EXTERNAL BUSY SIGNAL
	2A4A04J04C-07			
S0	2AAA2-K3	6-139		CHL 3 END OF RECORD TO CONT A
S1	2AAB2-N0	6-131		CHL 3 EN WORD COUNT CONTROL
S2	2AAB9-R0	6-143	2A0B9-AQ	CHL 0 FAN OUT BIT 16 D4 TO OU
S3	2AAB8-R0	6-147	2A0B8-AQ	CHL 1 FAN OUT BIT 16 D4 TO OU
T0	2A4A04J03D-03			CHL 3 EXTERNAL WRITE SIGNAL
	2A4A04J04D-03			
T1	2A4A04J03D-04			
	2A4A04J04D-04			
T2	2BAA0-02	6- 91		
T3	2BAA0-03	6- 91		CHAN 3 INT TO STATUS FAN-IN
U0	2AAA2-F3	6-139		CHL 3 NOT(READ) TO CONTROL C
U1	2AAA2-E1	6-139		CHAN 3 NOT(END OF RECORD) + WORD COUNT CONTROL
U2	2AAA2-K1	6-139		CHL 3 TERMINATE OR CLEAR
U3	2AAA2-U3	6-139		CHL 3 ENABLE 0 REG XMISSION
V0	2BAA0-E0	6- 91		NOT CHAN 3 READ STATUS TO FI
V1	2BAA0-E1	6- 91		
V2	2AAB1-R0	6-151	2A0B1-AQ	CHL 2 FAN OUT BIT 16 D4 TO OU
V3	2AAB0-R0	6-155	2A0B0-AQ	CHL 3 FAN OUT BIT 16 D4 TO OU
W0	2BAA0-01	6- 91		NOT CHAN 3 WRITE STATUS TO FI
W1	2BAA0-00	6- 91		
W2	2B1A3-M3	6- 37		D4 BIT 16 TO CHL 0-3 FAN OUT
W3	2B1A3-M2	6- 37		
X0	2A4A04J03D-02			
	2A4A04J04D-02			
X1	2A4A04J03D-01			CHL 3 EXTERNAL READ SIGNAL
	2A4A04J04D-01			
X2	2BAB4-U0	6-105		NOT CHAN 3 CLR CHAN INTERRUPT
X3	2BAB4-U1	6-105		

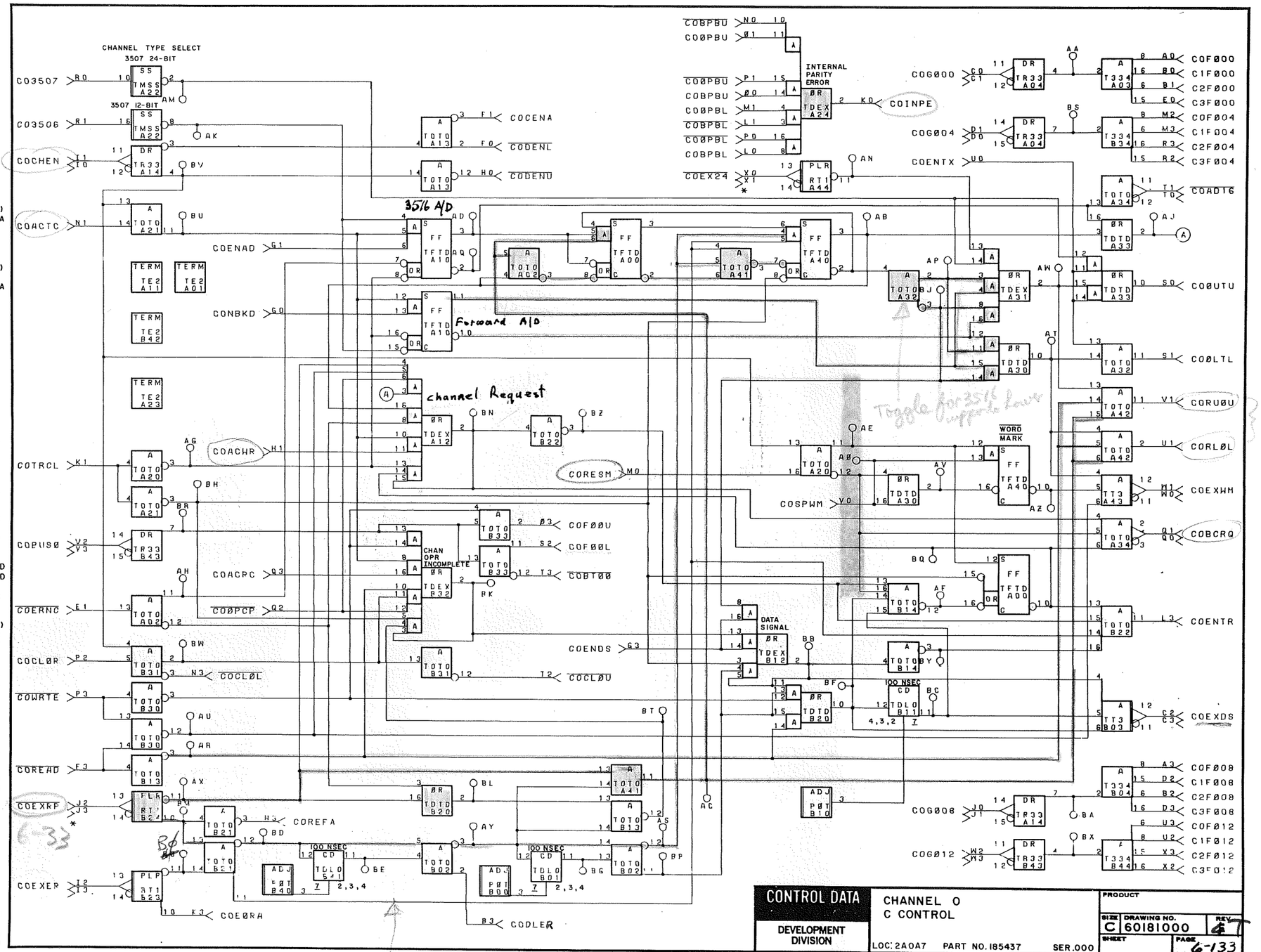


317



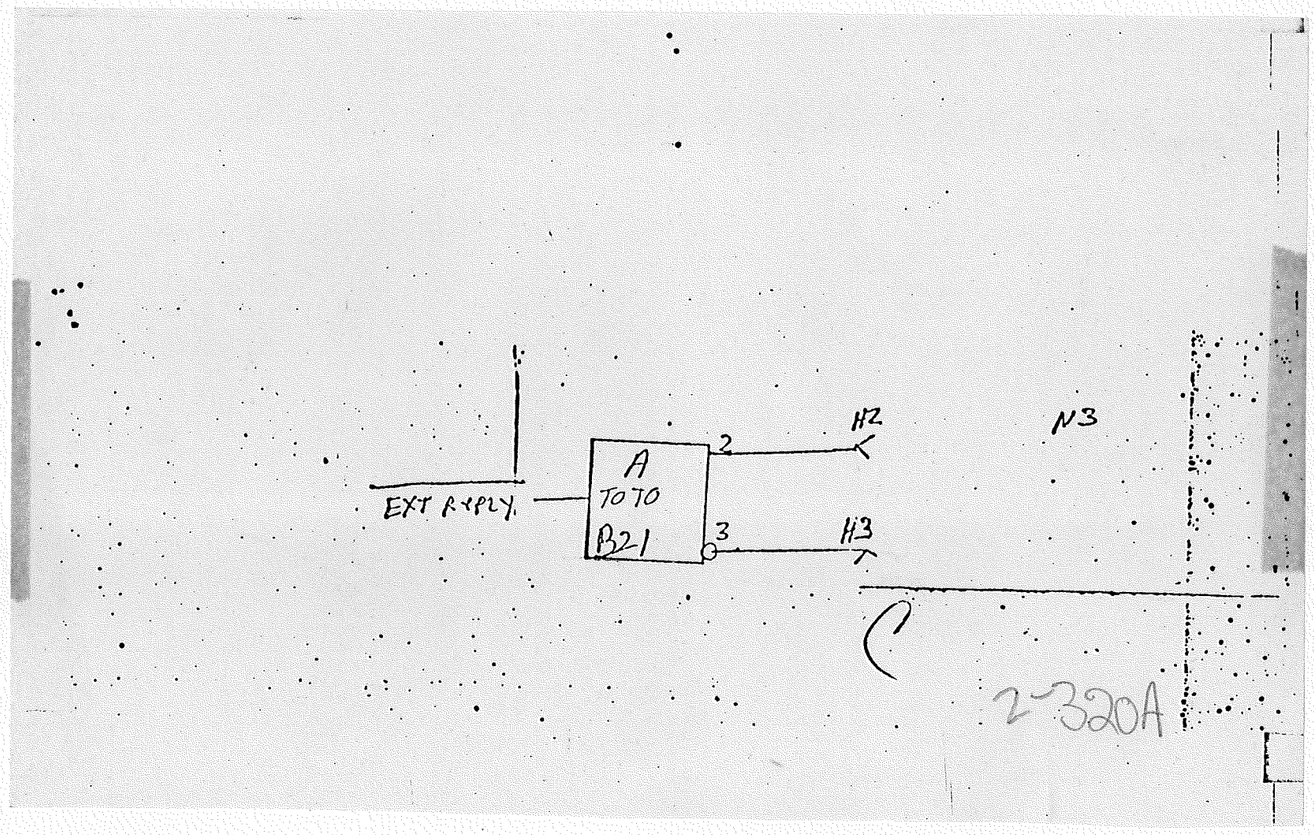
2-318A

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A∩A9-H∩	6-141	2A0A9-AS	CHL 0 FAN OUT BIT 00 D4 TO OL
A1	2A∩A9-I3	6-141	2A0A9-BW	CHL 0 FAN OUT BIT 08 D4 TO OL
B0	2A∩A8-H∩	6-145	2A0A8-AS	CHL 1 FAN OUT BIT 00 D4 TO OL
B1	2A∩A1-H1	6-149	2A0A1-AS	CHL 2 FAN OUT BIT 00 D4 TO OL
B2	2A∩A1-I3	6-149	2A0A1-BW	CHL 2 FAN OUT BIT 08 D4 TO OL
B3	2A∩B7-Q1	6-125		CHL 0 DELAYED EOR TO CONT A
C0	2B1B4-R2	6- 29		D4 BIT 00 TO CHL 0-3 FAN OUT
C1	2B1B4-R3	6- 29		
C2	2A4A01J03D-09			CHL 0 EXTERNAL DATA SIGNAL
	2A4A01J04D-09			
C3	2A4A01J03D-10			
	2A4A01J04D-10			
D0	2B1A3-R3	6- 37		
D1	2B1A3-B2	6- 37		D4 BIT 04 TO CHAN 0-3 FANOUT
D2	2A∩A8-I3	6-145	2A0A8-BW	CHL 1 FAN OUT BIT 08 D4 TO OL
D3	2A∩A0-I3	6-153	2A0A0-BW	CHL 3 FAN OUT BIT 08 D4 TO OL
E0	2A∩A0-H0	6-153	2A0A0-AS	CHL 3 FAN OUT BIT 00 D4 TO OL
E1	2A∩B7-U1	6-125		CHAN 0 NOT(END OF RECORD) * WORD COUNT CONTROL
F0	2A∩A4-A1	6-157		CHAN 0 NOT(EN 0 LWR TO FAN-IN)
F1	2A∩B7-D1	6-125		CHL 0 CHANNEL ENABLE TO CONT A
F3	2A∩B7-U∩	6-125		CHL 0 NOT(READ) TO CONTROL C
G0	2A∩B3-J1	6-129		CHL 0 FORWARD ASSY/DISASSY
G1	2A∩B6-B1	6-127		
G3	2A∩B7-R1	6-125		
H0	2A∩B5-A∩	6-159		CHAN 0 NOT(EN 0 UP. TO FAN-IN)
H1	2A∩B7-J1	6-125		CHL 0 ACTIVATE WRITE
H3	2A∩B7-M2	6-125		CHL 0 EXTERNAL REPLY TO CONT A
I0	2B1A5-N1	6- 19		
I1	2B1A5-N∩	6- 19		EN CHAN 0 TO COMMON CONTROL
I2	2A4A01J03E-05			CHL 0 EXTERNAL [redacted] SIGNAL
	2A4A01J04E-05			END RECORD.
I3	2A4A01J03E-06			
	2A4A01J04E-06			
J0	2B1B2-H2	6- 33		D4 BIT 08 TO CHL 0-3 FAN OUT
J1	2B1B2-H3	6- 33		
J2	2A4A01J03E-02			
	2A4A01J04E-02			
J3	2A4A01J03E-01			CHL 0 EXTERNAL REPLY SIGNAL
	2A4A01J04E-01			
K0	2A∩B7-M3	6-125		CHL 0 INTERNAL PARITY ERROR
K1	2A∩B7-U2	6-125		CHL 0 TERMINATE OR CLEAR
K2	2A∩B7-S∩	6-125		CHL 0 E O R.
L0	2A∩A9-C1	6-141		CHAN 0 O LWR PARITY GENERATED
L1	2A∩A9-B∩	6-141		NOT(CHAN 0 OL PAR. GENERATED)
L3	2A∩B7-O2	6-125		
M0	2A∩A6-U3	6-135		CHL 0 RESUME FROM BLOCK CONT.
M1	2A∩A9-D3	6-141		CHAN 0 O LWR PARITY RECEIVED
M2	2A∩A9-R∩	6-141	2A0A9-AQ	CHL 0 FAN OUT BIT 04 D4 TO OL
M3	2A∩A8-R∩	6-145	2A0A8-AQ	CHL 1 FAN OUT BIT 04 D4 TO OL
N0	2A∩B9-B∩	6-143		NOT(CHAN 0 OU PAR. GENERATED)
N1	2A∩B2-B∩	6-131		CHL 0 ACTIVATE CHL CONTROL C
N3	2A∩A9-U∩	6-141		CHL 0 NOT(CLEAR 0 REG LOWER)
O0	2A∩B9-C1	6-143		CHAN 0 O UP. PARITY GENERATED
O1	2A∩B9-D3	6-143		CHAN 0 O UP. PARITY RECEIVED
O3	2A∩B9-C∩	6-143		CHL 0 D4 FAN OUT TO OU REG
P0	2A∩A9-A3	6-141		NOT(CHAN 0 O LWR PAR. RECEIVED
P1	2A∩B9-A3	6-143		NOT(CHAN 0 O UP. PAR. RECEIVED
P2	2A∩A3-U3	6-137		CHL 0 CLEAR 0 REGISTERS
P3	2A∩B7-Q∩	6-125		CHL 0 NOT(WRITE) TO CONTROL C
Q0	2B1A0-I∩	6- 5		
Q1	2B1A0-I1	6- 5		CHL 0 BLOCK CONTROL REQUEST
Q2	2A∩B7-P2	6-125		CHAN 0 NOT(OPERATION COMPL FF)
Q3	2A∩B7-P1	6-125		CHL 0 ACTIVATE READ TO CONT C
R0	2A4A15J01A-01			CHAN 0 24-BIT MODE IDENTIFIER
R1	2A4A15J01B-01			CHAN 0 12-BIT IDENT FROM OU GROUND PIN
R2	2A∩A0-R∩	6-153	2A0A0-AQ	CHL 3 FAN OUT BIT 04 D4 TO OL
R3	2A∩A1-R∩	6-149	2A0A1-AQ	CHL 2 FAN OUT BIT 04 D4 TO OL
S0	2A∩B9-U1	6-143		CHL 0 ENABLE OU TRANSMISSION
S1	2A∩A9-U1	6-141		CHL 0 ENABLE OL TRANSMISSION
S2	2A∩A9-C∩	6-141		CHL 0 D4 FAN OUT TO OL REG
T0	2B1A∩-W3	6- 5		NOT((CH 0)(12-BIT MODE)(A/D))
T1	2B1A∩-W2	6- 5		
T2	2A∩B9-U∩	6-143		CHL 0 NOT(CLEAR 0 REG UPPER)
T3	2A∩B7-A∩	6-125		CHL 0 NOT(BUS TO 0) TO CONT A
U0	2A∩B7-U3	6-125		
U1	2A∩A9-A∩	6-141		CHAN 0 EXT RCVR TO 0 LOWER
U2	2A∩B8-H∩	6-147	2A0B8-AS	CHL 1 FAN OUT BIT 12 D4 TO OU
U3	2A∩B9-H∩	6-143	2A0B9-AS	CHL 0 FAN OUT BIT 12 D4 TO OU
V0	2A∩A2-U3	6-139	2A0A7-A0	CHL 0 SUPPRESS WORD MARK
V1	2A∩B9-A∩	6-143		CHAN 0 EXT RCVR TO 0 UPPER
V5	2B1A5-C∩	6- 19		EN CHAN 0 BUS TO 0 XFER/XMIT
V3	2B1A5-C1	6- 19		
W0	2A4A01J03F-02			
	2A4A01J04F-02			
W1	2A4A01J03F-01			CHL 0 EXTERNAL WORD MARK
	2A4A01J04F-01			
W2	2B1B4-M2	6- 29		D4 BIT 12 TO CHL 0-3 FAN OUT
W3	2B1B4-M3	6- 29		
X0	2A4A01J01C-08			
	2A4A01J02C-08			
X1	2A4A01J01C-07			CHAN 0 EXT 24-BIT DEVICE CONN
	2A4A01J02C-07			
X2	2A∩B9-H∩	6-155	2A0BC-AS	CHL 3 FAN OUT BIT 12 D4 TO OU
X3	2A∩B1-H∩	6-151	2A0B1-AS	CHL 2 FAN OUT BIT 12 D4 TO OU

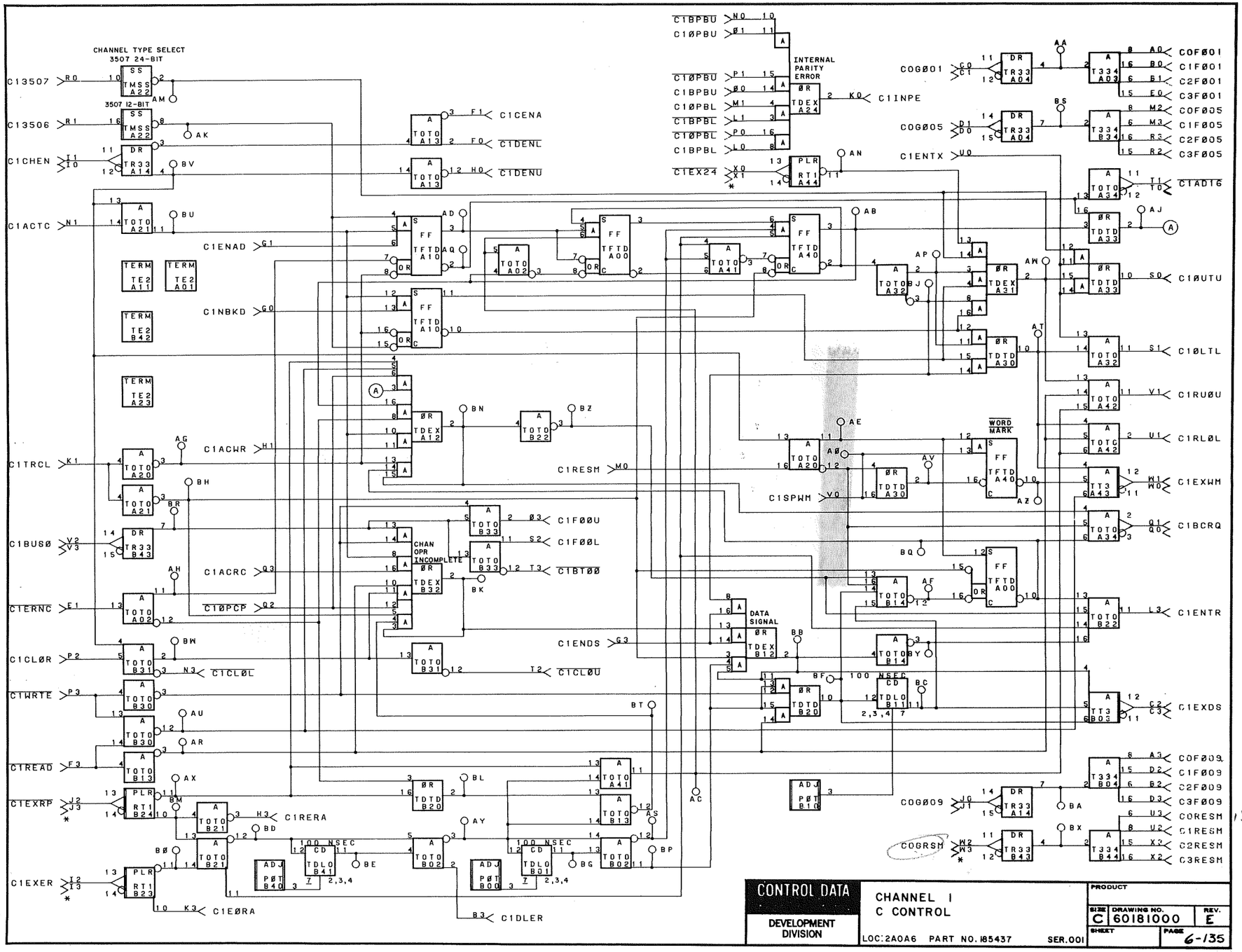


200 nS delay (knocking down data signal of 2nd Byte.)

319

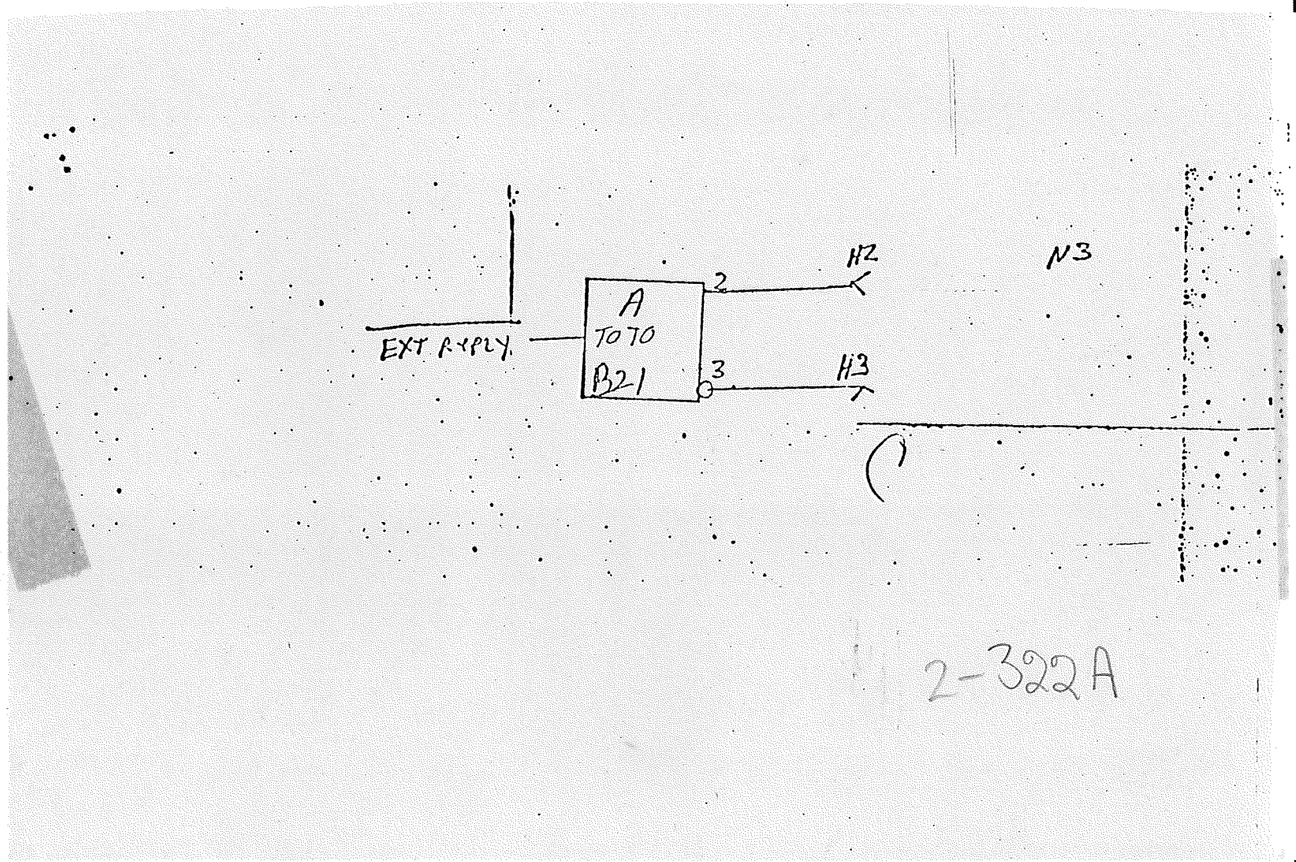

EXT REPLY
A
TO TO
B21
2
3
H2
H3
N3
2-320A

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2AAA9-G1	6-141	2A0A9-AE	CHL 0 FAN OUT BIT 01 D4 TO OL
A3	2AAA9-F3	6-141	2A0A9-BJ	CHL 0 FAN OUT BIT 09 D4 TO OL
B0	2AAA8-G1	6-145	2A0A8-AE	CHL 1 FAN OUT BIT 01 D4 TO OL
B1	2AAA1-G1	6-149	2A0A1-AE	CHL 2 FAN OUT BIT 01 D4 TO OL
B2	2AAA1-F3	6-149	2A0A1-BJ	CHL 2 FAN OUT BIT 09 D4 TO OL
B3	2AAB6-01	6-127		CHL 1 DELAYED EOR TO CONT A
C0	2B1B3-B2	6- 31		D4 BIT 01 TO CHL 0-3 FAN OUT
C1	2B1B3-R3	6- 31		
C2	2A4A02J03D-09			CHL 1 EXTERNAL DATA SIGNAL
	2A4A02J04D-09			
C3	2A4A02J03D-10			
	2A4A02J04D-10			
D0	2B1A2-B3	6- 39		
D1	2B1A2-B2	6- 39		D4 BIT 05 TO CHL 0-3 FAN OUT
D2	2AAA8-F3	6-145	2A0A8-BJ	CHL 1 FAN OUT BIT 09 D4 TO OL
D3	2AAA0-F3	6-153	2A0A0-BJ	CHL 3 FAN OUT BIT 09 D4 TO OL
E0	2AAA0-G1	6-153	2A0A0-AE	CHL 3 FAN OUT BIT 01 D4 TO OL
E1	2AFB6-U1	6-127		CHAN 1 NOT(END OF RECORD) + WORD COUNT CONTROL
F0	2AAA4-H2	6-157		CHL 1 NOT(ENABLE OL TO FAN IN)
F1	2AAB6-D1	6-127		CHL 1 CHANNEL ENABLE TO CONT A
F3	2AAB6-U4	6-127		CHL 1 NOT(READ) TO CONTROL C
G0	2AAB3-J4	6-129		CHL 1 FORWARD ASSY/DISASSY
G1	2AAB6-11	6-127		CHL 1 ENABLE ASSY/DISASSY
G3	2AAB6-R4	6-127		CHL 1 ENABLE DATA SIGNAL FF
H0	2AAB5-H2	6-159		CHL 1 NOT(ENABLE OU TO FAN IN)
H1	2AAB7-J4	6-125		CHL 1 ACTIVATE WRITE
H3	2AAB6-M2	6-127		CHL 1 EXTERNAL REPLY TO CONT A
I0	2B1A5-K1	6- 19		
I1	2B1A5-K4	6- 19		EN CHAN 1 TO COMMON CONTROL
I2	2A4A02J03E-05			CHL 1 EXTERNAL REJECT SIGNAL
	2A4A02J04E-05			
I3	2A4A02J03E-06			
	2A4A02J04E-06			
J0	2B1A4-H2	6- 35		D4 BIT 09 TO CHL 0-3 FAN OUT
J1	2B1A4-H3	6- 35		
J2	2A4A02J03E-02			
	2A4A02J04E-02			
J3	2A4A02J03E-01			CHL 1 EXTERNAL REPLY SIGNAL
	2A4A02J04E-01			
K0	2AAB6-M3	6-127		CHL 1 INTERNAL PARITY ERROR
K1	2AAB6-U2	6-127		CHL 1 TERMINATE OR CLEAR
K3	2AAB6-S4	6-127		CHL 1 END OF RECORD TO CONT A
L0	2AAA8-C1	6-145		O LOWER PARITY GENERATED CHL 1
L1	2AAA8-B4	6-145		NOT(OL PARITY GENERATED) CHL 1
L3	2AAB6-02	6-127		CHL 1 ENABLE TERMINATION
M0	2AAA6-U2	6-135		CHL 1 RESUME FROM BLOCK CONT.
M1	2AAA8-D3	6-145		O LOWER PARITY RECEIVED CHL 1
M2	2AAA9-G4	6-141	2A0A9-AF	CHL 0 FAN OUT BIT 05 D4 TO OL
M3	2AAA8-G4	6-145	2A0A8-AF	CHL 1 FAN OUT BIT 05 D4 TO OL
N0	2AAB8-R4	6-147		NOT(OU PARITY GENERATED) CHL 1
N1	2AAB2-11	6-131		CHL 1 ACTIVATE CHL CONTROL C
N3	2AAA8-U4	6-145		CHL 1 NOT(CLEAR O REG LOWER)
O0	2AAB8-C1	6-147		O UPPER PARITY GENERATED CHL 1
O1	2AAB8-D3	6-147		O UPPER PARITY RECEIVED CHL 1
O3	2AAB8-C4	6-147		CHL 1 D4 FAN OUT TO OU REG
P0	2AAA8-A3	6-145		NOT(OL PARITY RECEIVED) CHL 1
P1	2AAB8-A3	6-147		NOT(OU PARITY RECEIVED) CHL 1
P2	2AAA3-U2	6-137		CHL 1 CLEAR O REGISTERS
P3	2AAB6-Q4	6-127		CHL 1 NOT(WRITE) TO CONTROL C
Q0	2B1A6-J1	6- 5		
Q1	2B1A6-J4	6- 5		CHL 1 BLOCK CONTROL REQUEST
Q2	2AAB6-P2	6-127		CHL 1 NOT(OPERATION COMPL F/F)
Q3	2AAB6-P1	6-127		CHL 1 ACTIVATE READ TO CONT C
R0	2A4A15J01C-01			CHAN 1 24-BIT MODE IDENTIFIER
R1	2A4A15J01D-01			CHAN 1 12-BIT IDENT FROM OU GROUND PIN
R2	2AAA0-G4	6-153	2A0A0-AF	CHL 3 FAN OUT BIT 05 D4 TO OL
R3	2AAA1-G4	6-149	2A0A1-AF	CHL 2 FAN OUT BIT 05 D4 TO OL
S0	2AAB8-U1	6-147		CHL 1 ENABLE OU TRANSMISSION
S1	2AAA8-U1	6-145		CHL 1 ENABLE OL TRANSMISSION
S2	2AAA8-C4	6-145		CHL 1 D4 FAN OUT TO OL REG
T0	2B1A6-V3	6- 5		NOT((CH 1)(12-BIT MODE)(A/D))
T1	2B1A6-V2	6- 5		
T2	2AAB8-U4	6-147		CHL 1 NOT(CLEAR O REG UPPER)
T3	2AAB6-A4	6-127		CHL 1 NOT(BUS TO O) TO CONT A
U0	2AAB6-U3	6-127		CHL 1 ENABLE O REG XMISSION
U1	2AAA8-A4	6-145		CHAN 1 EXT RCVR TO O LOWER
U2	2AAA6-M4	6-135		CHL 1 RESUME FROM BLOCK CONT.
U3	2AAA7-M4	6-133		CHL 0 RESUME FROM BLOCK CONT.
V0	2AAA2-U2	6-139	2A0A6-A0	CHL 1 SUPPRESS WORD MARK
V1	2AAB8-A4	6-147		CHAN 1 EXT RCVR TO O UPPER
V2	2B1A5-D4	6- 19		EN CHAN 1 BUS TO O XFER/XMIT
V3	2B1A5-D1	6- 19		
W0	2A4A02J03F-02			
	2A4A02J04F-02			
W1	2A4A02J03F-01			CHL 1 EXTERNAL WORD MARK
	2A4A02J04F-01			
W2	2B1B9-M1	6- 7		NOT BC RESUME TO CHAN 0-3
W3	2B1B9-M4	6- 7		
X0	2A4A02J01C-08			
	2A4A02J02C-08			
X1	2A4A02J01C-07			CHL 1 EXT 24 BIT DEVICE CONNTD
	2A4A02J02C-07			
X2	2AAA2-M4	6-139		CHL 3 RESUME FROM BLOCK CONT.
X3	2AAA3-M4	6-137		CHL 2 RESUME FROM BLOCK CONT.



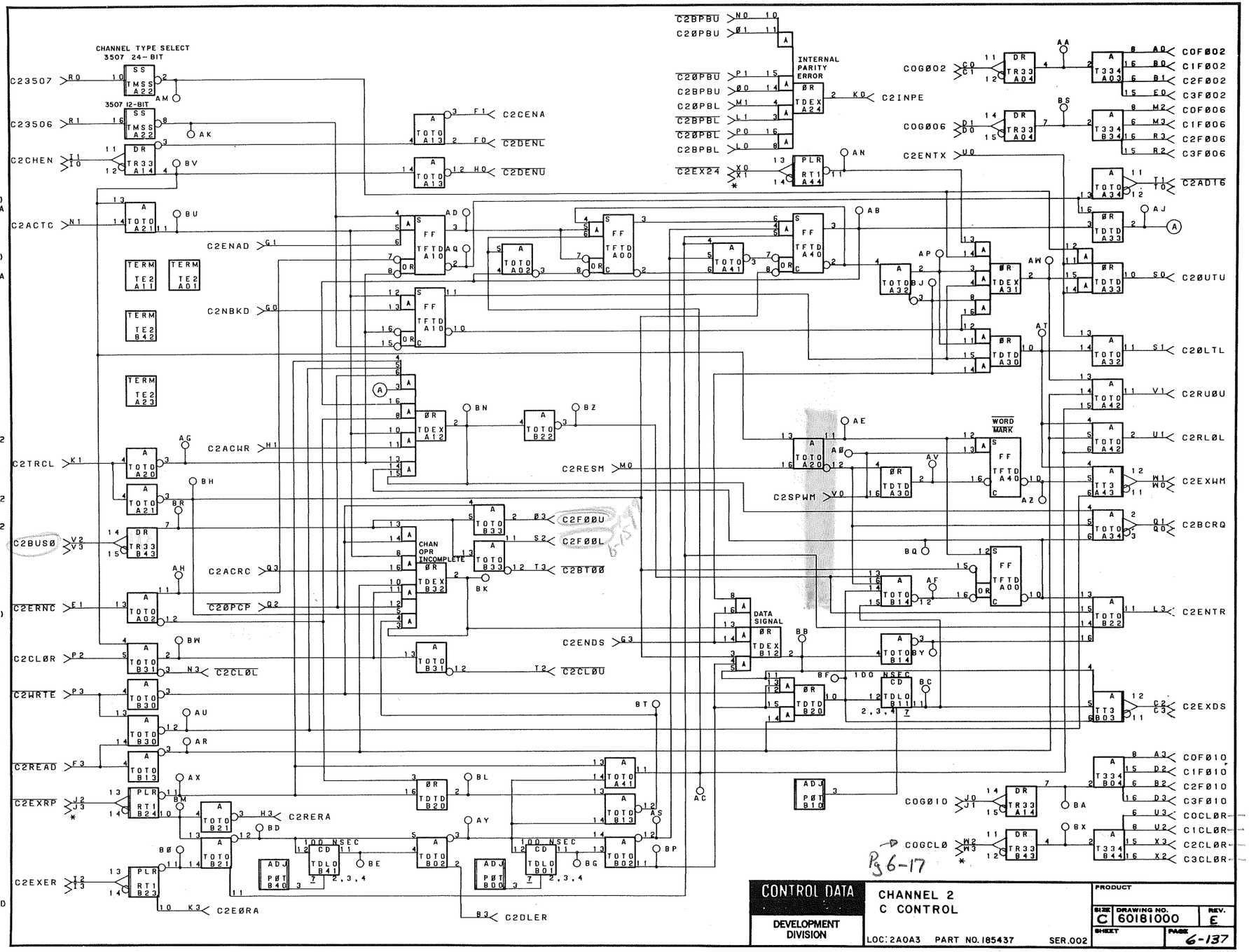
133

321

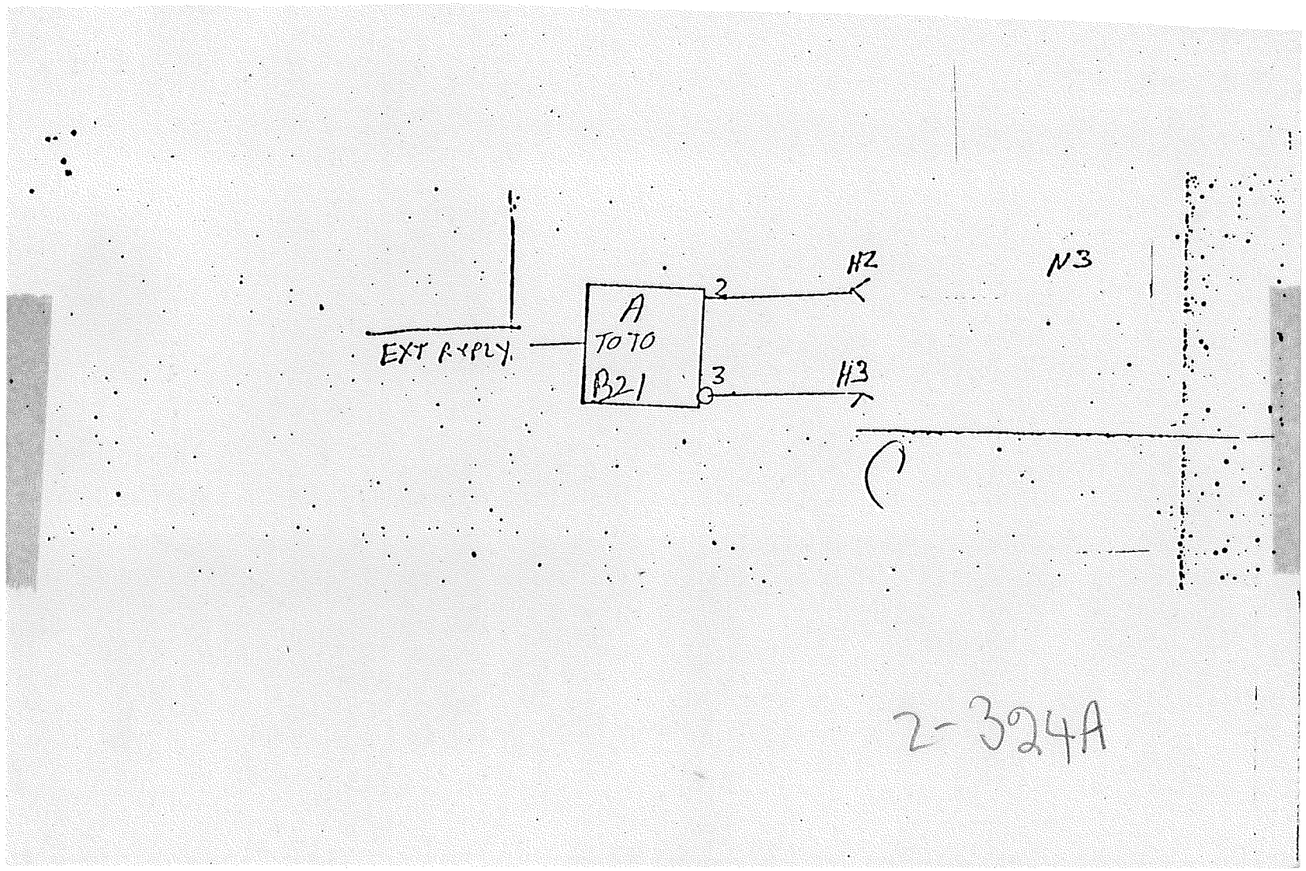


2-322A

A0	2AA9-K0	6-141	2A0A9-AR	CHL 0 FAN OUT BIT 02 D4 TO OL
A1	2AA9-F2	6-141	2A0A9-BO	CHL 0 FAN OUT BIT 10 D4 TO OL
B0	2AA8-K0	6-145	2A0A8-AR	CHL 1 FAN OUT BIT 02 D4 TO OL
B1	2AA1-K0	6-149	2A0A1-AR	CHL 2 FAN OUT BIT 02 D4 TO OL
B2	2AA1-F2	6-149	2A0A1-BO	CHL 2 FAN OUT BIT 10 D4 TO OL
B3	2A B3-Q1	6-129		CHL 2 DELAYED EOR TO CONT A
C0	2B1B2-B2	6- 33		D4 BIT 02 TO CHL 0-3 FAN OUT
C1	2B1B2-A3	6- 33		
C2	2A4A03J03D-09			CHL 2 EXTERNAL DATA SIGNAL
	2A4A03J04D-09			
C3	2A4A03J03D-10			
	2A4A03J04D-10			
D0	2B1B4-H3	6- 29		
D1	2B1B4-H2	6- 29		D4 BIT 06 TO CHAN 0-3 FANOUT
D2	2AA8-F2	6-145	2A0A8-BO	CHL 1 FAN OUT BIT 10 D4 TO OL
D3	2AA0-F2	6-153	2A0A0-BO	CHL 3 FAN OUT BIT 10 D4 TO OL
E0	2AA0-K0	6-153	2A0A0-AR	CHL 3 FAN OUT BIT 02 D4 TO OL
E1	2A B3-U1	6-129		CHAN 2 NOT(END OF RECORD) + WORD COUNT CONTROL
F0	2A A4-Q3	6-157		CHL 2 NOT(ENABLE OL TO FAN IN)
F1	2AB3-D1	6-129		CHL 2 CHANNEL ENABLE TO CONT A
F3	2A B3-U0	6-129		CHL 2 NOT(READ) TO CONTROL C
G0	2AB3-N1	6-129		CHL 2 FORWARD ASSY/DISASSY
G1	2A B6-I0	6-127		CHL 2 ENABLE ASSY/DIASSY
G3	2AB3-R0	6-129		CHL 2 ENABLE DATA SIGNAL FF
H0	2AB5-Q3	6-159		CHL 2 NOT(ENABLE OU TO FAN IN)
H1	2AB7-N1	6-125		CHL 2 ACTIVATE WRITE
H3	2AB3-M2	6-129		CHL 2 EXTERNAL REPLY TO CONT A
I0	2B1A5-00	6- 19		
I1	2B1A5-01	6- 19		EN CHAN 2 TO COMMON CONTROL
I2	2A4A03J03E-05			CHL 2 EXTERNAL REJECT SIGNAL
	2A4A03J04E-05			
I3	2A4A03J03E-06			
	2A4A03J04E-06			
J0	2B1A3-H2	6- 37		D4 BIT 10 TO CHL 0-3 FAN OUT
J1	2B1A3-H3	6- 37		
J2	2A4A03J03E-02			
	2A4A03J04E-02			
J3	2A4A03J03E-01			CHL 2 EXTERNAL REPLY SIGNAL
	2A4A03J04E-01			
K0	2AB3-M3	6-129		CHL 2 INTERNAL PARITY ERROR
K1	2AB3-U2	6-129		CHL 2 TERMINATE OR CLEAR
K3	2AB3-S0	6-129		CHL 2 END OF RECORD TO CONT A
L0	2AA1-C1	6-149		O LWR PARITY GENERATED=CHAN 2
L1	2AA1-B0	6-149		NOT(OL PARITY GENERATED) CHL 2
L3	2A B3-O2	6-129		CHL 2 ENABLE TERMINATION
M0	2AA6-X3	6-135		CHL 2 RESUME FROM BLOCK CONT.
M1	2AA1-D3	6-149		O LOWER PARITY RECEIVED CHL 2
M2	2AA9-J3	6-141	2A0A9-BZ	CHL 0 FAN OUT BIT 06 D4 TO OL
M3	2AA8-J3	6-145	2A0A8-BZ	CHL 1 FAN OUT BIT 06 D4 TO OL
N0	2AB1-B0	6-151		NOT(OU PARITY GENERATED) CHL 2
N1	2AB2-I0	6-131		CHL 2 ACTIVATE CHL CONTROL C
N3	2AA1-U0	6-149		CHL 2 NOT(CLEAR O REG LOWER)
O0	2AB1-C1	6-151		O UPPER PARITY GENERATED CHL 2
O1	2AB1-D3	6-151		O UPPER PARITY RECEIVED CHL 2
O3	2AB1-C0	6-151		CHL 2 D4 FAN OUT TO OU REG
P0	2AA1-A3	6-149		NOT(OL PARITY RECEIVED) CHL 2
P1	2AB1-A3	6-151		NOT(OU PARITY RECEIVED) CHL 2
P2	2AA3-X3	6-137		CHL 2 CLEAR O REGISTERS
P3	2AB3-Q0	6-129		CHL 2 NOT(WRITE) TO CONTROL C
Q0	2B1A0-H0	6- 5		
Q1	2B1A0-H1	6- 5		CHL 2 BLOCK CONTROL REQUEST
Q2	2AB3-P2	6-129		CHL 2 NOT(OPERATION COMPL F/F)
Q3	2AB3-P1	6-129		CHL 2 ACTIVATE READ TO CONT C
R0	2A4A15J01E-01			CHAN 2 24-BIT MODE IDENTIFIER
R1	2A4A15J01F-01			CHAN 3 12-BIT IDENT FROM OU GROUND PIN
R2	2AA0-J3	6-153	2A0A0-BZ	CHL 3 FAN OUT BIT 06 D4 TO OL
R3	2AA1-J3	6-149	2A0A1-BZ	CHL 2 FAN OUT BIT 06 D4 TO OL
S0	2AB1-U1	6-151		CHL 2 ENABLE OU TRANSMISSION
S1	2AA1-U1	6-149		CHL 2 ENABLE OL TRANSMISSION
S2	2AA1-C0	6-149		CHL 2 D4 FAN OUT TO OL REG
T0	2B1A0-U3	6- 5		NOT((CH 2)(12-BIT MODE)(A/D))
T1	2B1A0-U2	6- 5		
T2	2AB1-U0	6-151		CHL 2 NOT(CLEAR O REG UPPER)
T3	2AB3-A0	6-129		CHL 2 NOT(BUS TO O) TO CONT A
U0	2A B3-U3	6-129		CHL 2 ENABLE O REG XMISSION
U1	2AA1-A0	6-149		CHAN 2 EXT RCVR TO O LOWER
U2	2AA6-P2	6-135		CHL 1 CLEAR O REGISTERS
U3	2AA7-P2	6-133		CHL 0 CLEAR O REGISTERS
V0	2AA2-X3	6-139	2A0A3-AO	CHL 2 SUPPRESS WORD MARK
V1	2AB1-A0	6-151		CHAN 2 EXT RCVR TO O UPPER
V2	2B1A5-E0	6- 19		EN CHAN 2 BUS TO O XFER/XMIT
V3	2B1A5-E1	6- 19		
W0	2A4A03J03F-02			
	2A4A03J04F-02			
W1	2A4A03J03F-01			CHL 2 EXTERNAL WORD MARK
	2A4A03J04F-01			
W2	2B1A8-B1	6- 17		NOT CLR O REG TO CHAN 0-3
W3	2B1A8-B0	6- 17		
X0	2A4A03J01C-08			
	2A4A03J02C-08			
X1	2A4A03J01C-07			CHL 2 EXT 24 BIT DEVICE CONNTD
	2A4A03J02C-07			
X2	2AA2-P2	6-139		CHL 3 CLEAR O REGISTERS
X3	2AA3-P2	6-137		CHL 2 CLEAR O REGISTERS

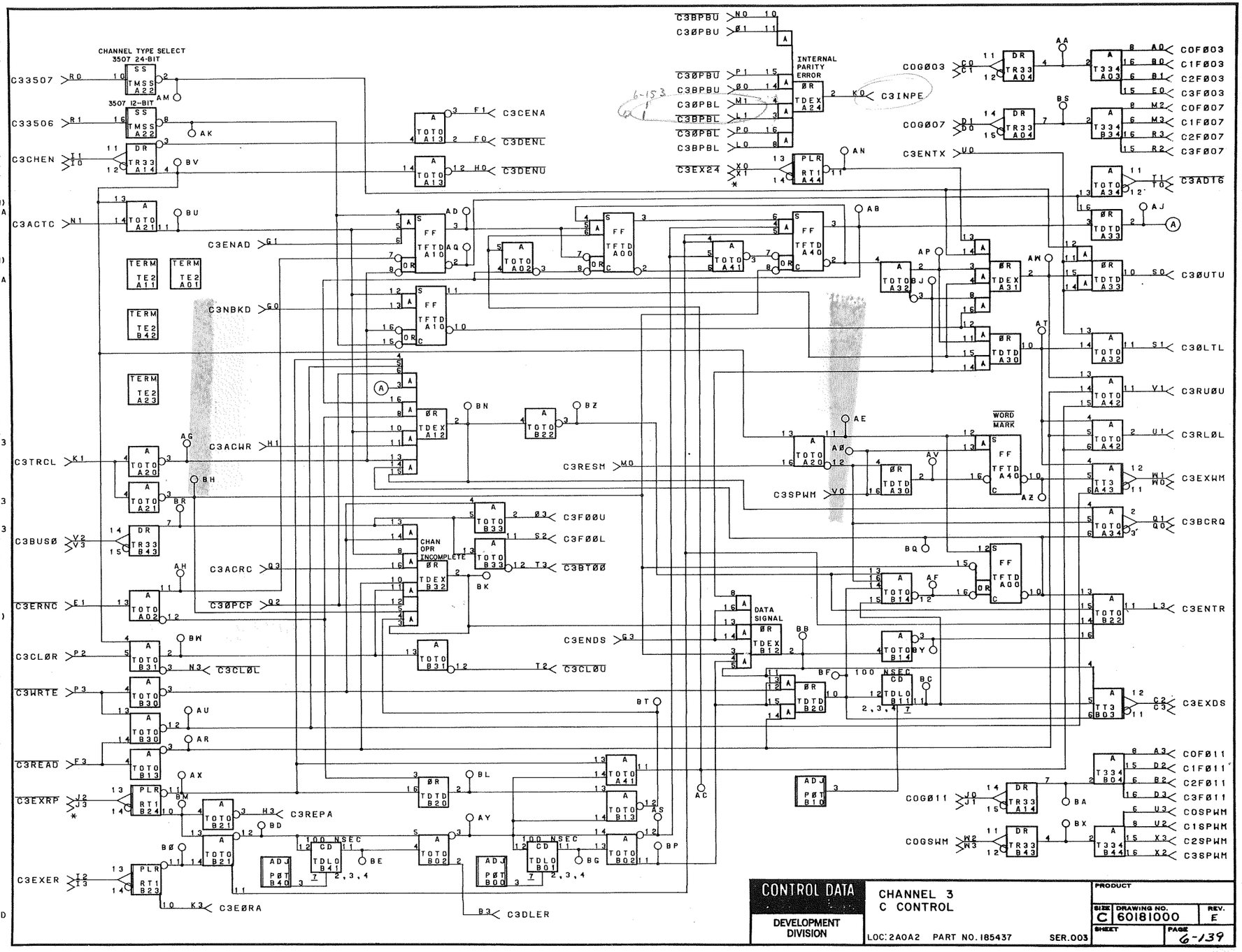


323



2-324A

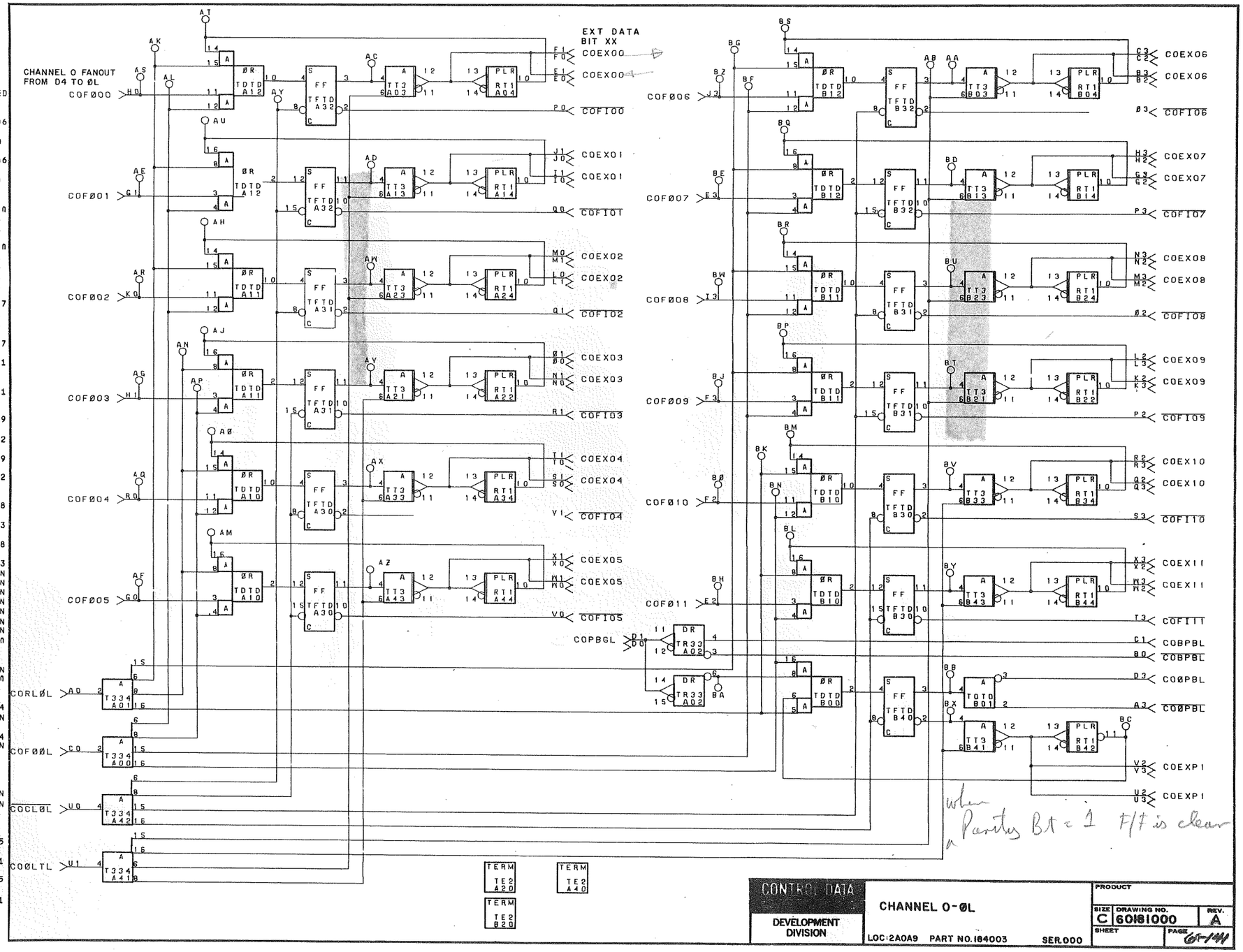
A0	2A0A9-H1	6-141	2A0A9-AG	CHL 0 FAN OUT BIT 03 D4 TO OL
A1	2A0A9-E2	6-141	2A0A9-BH	CHL 0 FAN OUT BIT 11 D4 TO OL
B0	2A0A8-H1	6-145	2A0A8-AG	CHL 1 FAN OUT BIT 03 D4 TO OL
B1	2A0A1-H1	6-149	2A0A1-AG	CHL 2 FAN OUT BIT 03 D4 TO OL
B2	2A0A1-E2	6-149	2A0A1-BH	CHL 2 FAN OUT BIT 11 D4 TO OL
B3	2A0B2-Q1	6-131		CHL 3 DELAYED EOR TO CONT A
C0	2B1A4-B2	6- 35		D4 BIT 03 TO CHAN 0-3 FANOUT
C1	2B1A4-B3	6- 35		
C2	2A4A04J03D-09			CHL 3 EXTERNAL DATA SIGNAL
	2A4A04J04D-09			
C3	2A4A04J03D-10			
	2A4A04J04D-10			
D0	2B1B3-H3	6- 31		
D1	2B1B3-H2	6- 31		D4 BIT 07 TO CHL 0-3 FAN OUT
D2	2A0A8-E2	6-145	2A0A8-BH	CHL 1 FAN OUT BIT 11 D4 TO OL
D3	2A0A0-E2	6-153	2A0A0-BH	CHL 3 FAN OUT BIT 11 D4 TO OL
E0	2A0A0-H1	6-153	2A0A0-AG	CHL 3 FAN OUT BIT 03 D4 TO OL
E1	2A0B2-U1	6-131		CHAN 3 NOT(END OF RECORD) + WORD COUNT CONTROL
F0	2A0A4-U2	6-157		CHL 3 NOT(ENABLE OL TO FAN IN)
F1	2A0B2-D1	6-131		CHL 3 CHANNEL ENABLE TO CONT A
F3	2A0B2-U6	6-131		CHL 3 NOT(READ) TO CONTROL C
G0	2A0B3-N6	6-129		CHL 3 FORWARD ASSY/DISASSY
G1	2A0B6-A3	6-127		CHL 3 ENABLE ASSY/DISASSY
G3	2A0B2-R6	6-131		CHL 3 ENABLE DATA ENABLE FF
H0	2A0B5-U2	6-159		CHL 3 NOT(ENABLE OU TO FAN IN)
H1	2A0B7-N6	6-125		CHL 3 ACTIVATE WRITE
H3	2A0B2-M2	6-131		CHL 3 EXTERNAL REPLY TO CONT A
I0	2B1A5-L1	6- 19		
I1	2B1A5-L0	6- 19		EN CHAN 3 TO COMMON CONTROL
I2	2A4A04J03E-05			CHL 3 EXTERNAL REJECT SIGNAL
	2A4A04J04E-05			
I3	2A4A04J03E-06			
	2A4A04J04E-06			
J0	2B1A2-H2	6- 39		D4 BIT 11 TO CHL 0-3 FAN OUT
J1	2B1A2-H3	6- 39		
J2	2A4A04J03E-02			
	2A4A04J04E-02			
J3	2A4A04J03E-01			CHL 3 EXTERNAL REPLY SIGNAL
	2A4A04J04E-01			
K0	2A0B2-M3	6-131		CHL 3 INTERNAL PARITY ERROR
K1	2A0B2-U2	6-131		CHL 3 TERMINATE OR CLEAR
K3	2A0B2-S6	6-131		CHL 3 END OF RECORD TO CONT A
L0	2A0A0-C1	6-153		O LWR PARITY GENERATED-CHAN 3
L1	2A0A0-B0	6-153		NOT(OL PARITY GENERATED) CHL 3
L3	2A0B2-O2	6-131		CHL 3 ENABLE TERMINATION
M0	2A0A6-X2	6-135		CHL 3 RESUME FROM BLOCK CONT.
M1	2A0A0-D3	6-153		O LOWER PARITY RECEIVED CHL 3
M2	2A0A9-E3	6-141	2A0A9-BE	CHL 0 FAN OUT BIT 07 D4 TO OL
M3	2A0A8-E3	6-145	2A0A8-BE	CHL 1 FAN OUT BIT 07 D4 TO OL
N0	2A0B0-B0	6-155		NOT(OU PARITY GENERATED) CHL 3
N1	2A0B2-A3	6-131		CHL 3 ACTIVATE CHL CONTROL C
N3	2A0A0-U0	6-153		CHL 3 NOT(CLEAR O REG LOWER)
O0	2A0B0-C1	6-155		O UPPER PARITY GENERATED CHL 3
O1	2A0B0-D3	6-155		O UPPER PARITY RECEIVED CHL 3
O3	2A0B0-C0	6-155		CHL 3 D4 FAN OUT TO OU REG
P0	2A0A0-A3	6-153		NOT(OL PARITY RECEIVED) CHL 3
P1	2A0B0-A3	6-155		NOT(OU PARITY RECEIVED) CHL 3
P2	2A0A3-X2	6-137		CHL 3 CLEAR O REGISTERS
P3	2A0B2-Q6	6-131		CHL 3 NOT(WRITE) TO CONTROL C
Q0	2B1A6-K1	6- 5		
Q1	2B1A6-K6	6- 5		CHL 3 BLOCK CONTROL REQUEST
Q2	2A0B2-P2	6-131		CHL 3 NOT(OPERATION COMPL F/F)
Q3	2A0B2-P1	6-131		CHL 3 ACTIVATE READ TO CONT C
R0	2A4A15J01G-01			CHAN 3 24-BIT IDENTIFIER
R1	2A4A15J01H-01			CHAN 3 12-BIT IDENT FROM OU GROUND PIN
R2	2A0A0-E3	6-153	2A0A0-BE	CHL 3 FAN OUT BIT 07 D4 TO OL
R3	2A0A1-E3	6-149	2A0A1-BE	CHL 2 FAN OUT BIT 07 D4 TO OL
S0	2A0B0-U1	6-155		CHL 3 ENABLE OU TRANSMISSION
S1	2A0A0-U1	6-153		CHL 3 ENABLE OL TRANSMISSION
S2	2A0A0-C6	6-153		CHL 3 D4 FAN OUT TO OL REG
T0	2B1A6-X2	6- 5		NOT((CH 3)(12-BIT MODE)(A/D))
T1	2B1A6-X3	6- 5		
T2	2A0B0-U6	6-155		CHL 3 NOT(CLEAR O REG UPPER)
T3	2A0B2-A6	6-131		CHL 3 NOT(BUS TO O) TO CONT A
U0	2A0B2-U3	6-131		CHL 3 ENABLE O REG XMISSION
U1	2A0A0-A0	6-153		CHAN 3 EXT RCVR TO O LOWER
U2	2A0A6-V6	6-135	2A0A6-AO	CHL 1 SUPPRESS WORD MARK
U3	2A0A7-V6	6-133	2A0A7-AO	CHL 0 SUPPRESS WORD MARK
V0	2A0A2-X2	6-139	2A0A2-AO	CHL 3 SUPPRESS WORD MARK
V1	2A0B0-A0	6-155		CHAN 3 EXT RCVR TO O UPPER
V2	2B1A5-B1	6- 19		EN CHAN 3 BUS TO O XFER/XMIT
V3	2B1A5-B6	6- 19		
W0	2A4A04J03F-02			
	2A4A04J04F-02			
W1	2A4A04J03F-01			CHL 3 EXTERNAL WORD MARK
	2A4A04J04F-01			
W2	2A1B4-R1	6- 57		SUPPR WORD MARK TO CHAN 0-3 FANOUT
W3	2A1B4-B6	6- 57		
X0	2A4A04J01C-08			
	2A4A04J02C-08			
X1	2A4A04J01C-07			CHL 3 EXT 24 BIT DEVICE CONNTD
	2A4A04J02C-07			
X2	2A0A2-V6	6-139	2A0A2-AO	CHL 3 SUPPRESS WORD MARK
X3	2A0A3-V6	6-137	2A0A3-AO	CHL 2 SUPPRESS WORD MARK

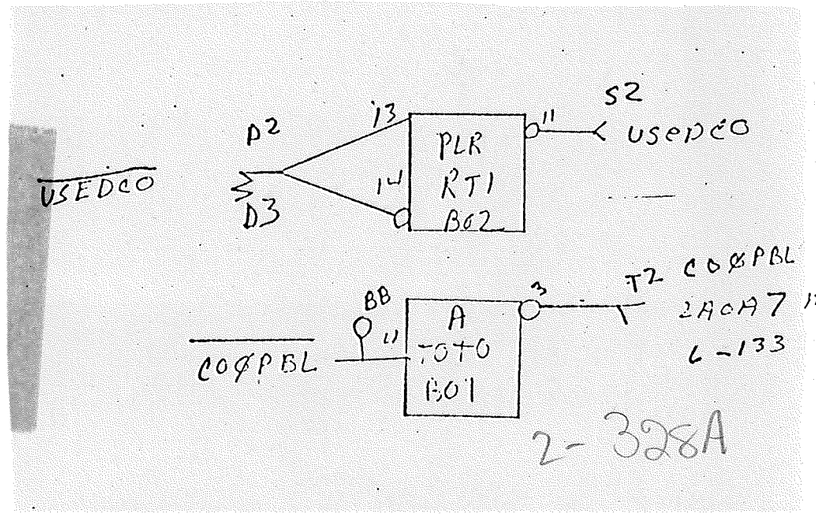


CONTROL DATA	CHANNEL 3 C CONTROL	PRODUCT	
DEVELOPMENT DIVISION	LOC: 2A0A2 PART NO. 185437 SER. 003	SIZE C	DRAWING NO. 60181000 REV. E
		SHEET	PAGE 6-139

325

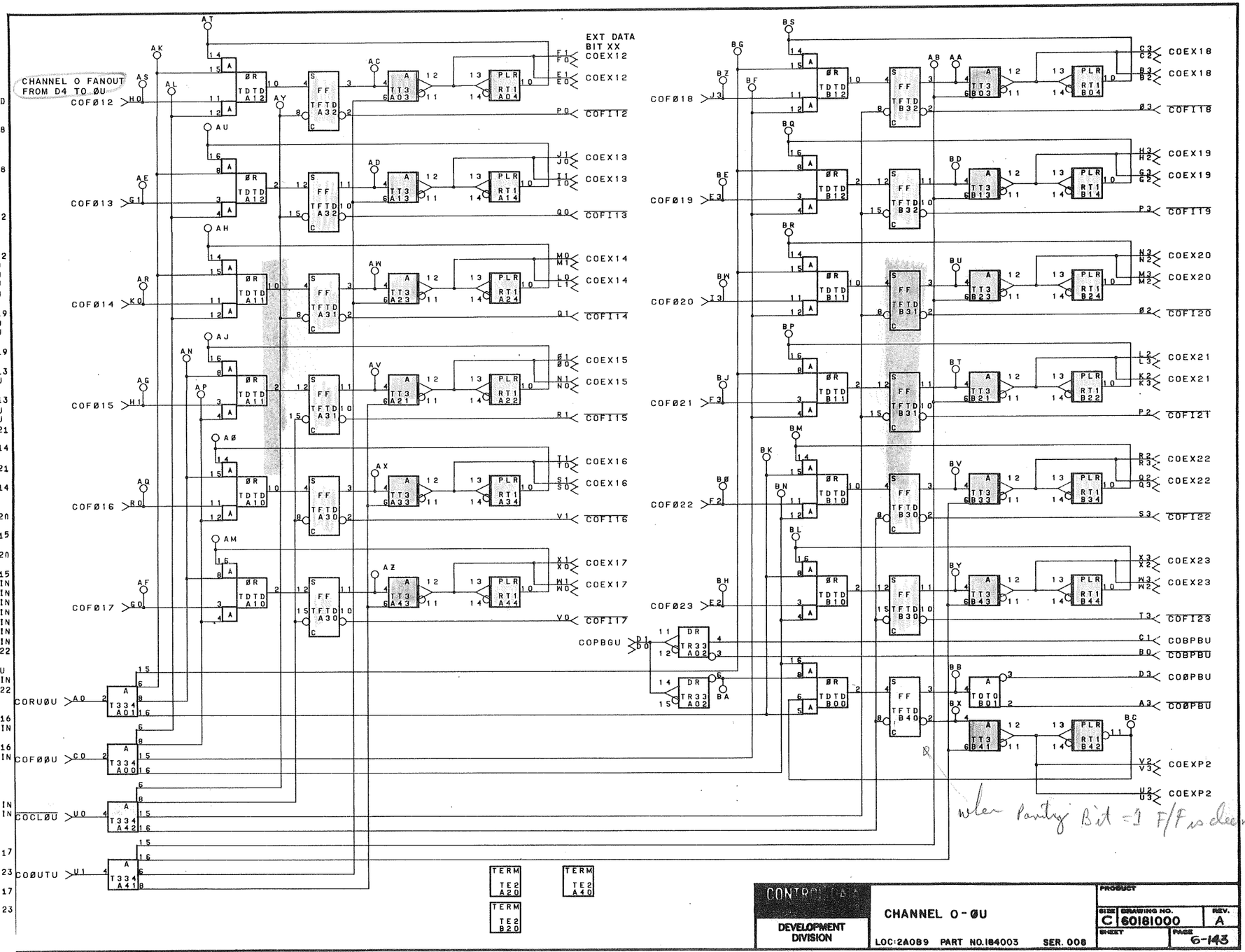
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A0A7-U1	6-133		CHAN 0 EXT RCVR TO 0 LOWER
A3	2A0A7-P0	6-133		NOT(CHAN 0 0 LWR PAR, RECEIVED
B0	2A0A7-L1	6-133		NOT(CHAN 0 OL PAR, GENERATED)
B2	2A4A01J03B-04			
B3	2A4A01J03B-03			CHANNEL 0 EXTERNAL DATA BIT 06
C0	2A0A7-S2	6-133		CHL 0 D4 FAN OUT TO OL REG
C1	2A0A7-L0	6-133		CHAN 0 0 LWR PARITY GENERATED
C2	2A4A01J04B-04			
C3	2A4A01J04B-03			CHANNEL 0 EXTERNAL DATA BIT 06
D0	2B1B0-F2	6- 7		
D1	2B1B0-F3	6- 7		LOWER PARITY BIT TO CHANNEL 0
D3	2A0A7-M1	6-133		CHAN 0 0 LWR PARITY RECEIVED
E0	2A4A01J03A-02			
E1	2A4A01J03A-01			CHANNEL 0 EXTERNAL DATA BIT 00
E2	2A0A2-A3	6-139	2A0A9-RH	CHL 0 FAN OUT BIT 11 D4 TO OL
E3	2A0A2-M2	6-139	2A0A9-BE	CHL 0 FAN OUT BIT 07 D4 TO OL
F0	2A4A01J04A-02			
F1	2A4A01J04A-01			CHANNEL 0 EXTERNAL DATA BIT 00
F2	2A0A3-A3	6-137	2A0A9-BD	CHL 0 FAN OUT BIT 10 D4 TO OL
F3	2A0A6-A3	6-135	2A0A9-RJ	CHL 0 FAN OUT BIT 09 D4 TO OL
G0	2A0A6-M2	6-135	2A0A9-AF	CHL 0 FAN OUT BIT 05 D4 TO OL
G1	2A0A6-A0	6-135	2A0A9-AE	CHL 0 FAN OUT BIT 01 D4 TO OL
G2	2A4A01J03B-06			
G3	2A4A01J03B-05			CHANNEL 0 EXTERNAL DATA BIT 07
H0	2A0A7-A0	6-133	2A0A9-AS	CHL 0 FAN OUT BIT 00 D4 TO OL
H1	2A0A2-A0	6-139	2A0A9-AG	CHL 0 FAN OUT BIT 03 D4 TO OL
H2	2A4A01J04B-06			
H3	2A4A01J04B-05			CHANNEL 0 EXTERNAL DATA BIT 07
I0	2A4A01J03A-04			
I1	2A4A01J03A-03			CHANNEL 0 EXTERNAL DATA BIT 01
I3	2A0A7-A3	6-133	2A0A9-BW	CHL 0 FAN OUT BIT 08 D4 TO OL
J0	2A4A01J04A-04			
J1	2A4A01J04A-03			CHANNEL 0 EXTERNAL DATA BIT 01
J3	2A0A3-M2	6-137	2A0A9-RZ	CHL 0 FAN OUT BIT 06 D4 TO OL
K0	2A0A3-A0	6-137	2A0A9-AR	CHL 0 FAN OUT BIT 02 D4 TO OL
K2	2A4A01J03B-09			CHANNEL 0 EXTERNAL DATA BIT 09
K3	2A4A01J03B-10			
L0	2A4A01J04A-05			CHANNEL 0 EXTERNAL DATA BIT 02
L1	2A4A01J04A-06			
L2	2A4A01J04B-09			CHANNEL 0 EXTERNAL DATA BIT 09
L3	2A4A01J04B-10			
M0	2A4A01J03A-05			CHANNEL 0 EXTERNAL DATA BIT 02
M1	2A4A01J03A-06			
M2	2A4A01J03B-08			
M3	2A4A01J03B-07			CHANNEL 0 EXTERNAL DATA BIT 08
N0	2A4A01J03A-08			
N1	2A4A01J03A-07			CHANNEL 0 EXTERNAL DATA BIT 03
N2	2A4A01J04B-08			
N3	2A4A01J04B-07			CHANNEL 0 EXTERNAL DATA BIT 08
O0	2A4A01J04A-08			
O1	2A4A01J04A-07			CHANNEL 0 EXTERNAL DATA BIT 03
O2	2A0A4-B3	6-157	2A0A4-RC	NOT(RIT 08) CHL 0 OL TO FAN IN
O3	2A0A4-A3	6-157	2A0A4-RA	NOT(RIT 06) CHL 0 OL TO FAN IN
P0	2A0A4-D1	6-157	2A0A4-AD	NOT(RIT 00) CHL 0 OL TO FAN IN
P2	2A0A4-C2	6-157	2A0A4-RD	NOT(RIT 09) CHL 0 OL TO FAN IN
P3	2A0A4-B2	6-157	2A0A4-RB	NOT(RIT 07) CHL 0 OL TO FAN IN
Q0	2A0A4-D0	6-157	2A0A4-AE	NOT(RIT 01) CHL 0 OL TO FAN IN
Q1	2A0A4-E1	6-157	2A0A4-AF	NOT(RIT 02) CHL 0 OL TO FAN IN
Q2	2A4A01J03C-01			CHANNEL 0 EXTERNAL DATA BIT 10
Q3	2A4A01J03C-02			
R0	2A0A7-M2	6-133	2A0A9-AQ	CHL 0 FAN OUT BIT 04 D4 TO OL
R1	2A0A4-E0	6-157	2A0A4-AG	NOT(RIT 03) CHL 0 OL TO FAN IN
R2	2A4A01J04C-01			CHANNEL 0 EXTERNAL DATA BIT 10
R3	2A4A01J04C-02			
S0	2A4A01J03A-10			
S1	2A4A01J03A-09			CHANNEL 0 EXTERNAL DATA BIT 04
S3	2A0A4-C3	6-157	2A0A4-RE	NOT(BIT 10) CHL 0 OL TO FAN IN
T0	2A4A01J04A-10			
T1	2A4A01J04A-09			CHANNEL 0 EXTERNAL DATA BIT 04
T3	2A0A4-D2	6-157	2A0A4-RG	NOT(RIT 11) CHL 0 OL TO FAN IN
U0	2A0A7-N3	6-133		CHL 0 NOT(CLEAR 0 REG LOWER)
U1	2A0A7-S1	6-133		CHL 0 ENABLE OL TRANSMISSION
U2	2A4A01J03C-05			CHL 0 EXTERNAL PARITY BIT 1
U3	2A4A01J03C-06			
V0	2A0A4-B0	6-157	2A0A4-AB	NOT(RIT 05) CHL 0 OL TO FAN IN
V1	2A0A4-C0	6-157	2A0A4-AC	NOT(RIT 04) CHL 0 OL TO FAN IN
V2	2A4A01J04C-05			CHL 0 EXTERNAL PARITY BIT 1
V3	2A4A01J04C-06			
W0	2A4A01J03B-02			
W1	2A4A01J03B-01			CHANNEL 0 EXTERNAL DATA BIT 05
W2	2A4A01J03C-04			
W3	2A4A01J03C-03			CHANNEL 0 EXTERNAL DATA BIT 11
X0	2A4A01J04B-02			
X1	2A4A01J04B-01			CHANNEL 0 EXTERNAL DATA BIT 05
X2	2A4A01J04C-04			
X3	2A4A01J04C-03			CHANNEL 0 EXTERNAL DATA BIT 11




S2
USEDCO
P2
D3
J3
J4
PLR
RT1
B02
J1
USEDCO
BB
J1
A
TOTO
B01
J3
T2
COMPBL
2AOA7
L-133
COMPBL

2-328A

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A0A7-V1	6-133		CHAN 0 EXT RCVR TO 0 UPPER
A3	2A0A7-P1	6-133		NOT(CHAN 0 0 UP, PAR; RECEIVED
B0	2A0A7-N0	6-133		NOT(CHAN 0 0U PAR, GENERATED)
B2	2A4A01J01B-04			
B3	2A4A01J01B-03			CHANNEL 0 EXTERNAL DATA BIT 18
C0	2A0A7-03	6-133		CHL 0 D4 FAN OUT TO 0U REG
C1	2A0A7-00	6-133		CHAN 0 0 UP, PARITY GENERATED
C2	2A4A01J02B-04			
C3	2A4A01J02B-03			CHANNEL 0 EXTERNAL DATA BIT 18
D0	2R1A0-F2	6- 5		
D1	2R1A0-F3	6- 5		UPPER PARITY BIT TO CHANNEL 0
D3	2A0A7-01	6-133		CHAN 0 0 UP, PARITY RECEIVED
E0	2A4A01J01A-02			
E1	2A4A01J01A-01			CHANNEL 0 EXTERNAL DATA BIT 12
E2	2A0B3-S2	6-129	2A0B9-RH	CHL 0 FAN OUT BIT 23 D4 TO 0U
E3	2A0B3-H1	6-129	2A0B9-RE	CHL 0 FAN OUT BIT 19 D4 TO 0U
F0	2A4A01J02A-02			
F1	2A4A01J02A-01			CHANNEL 0 EXTERNAL DATA BIT 12
F2	2A0B6-H1	6-127	2A0B9-BD	CHL 0 FAN OUT BIT 22 D4 TO 0U
F3	2A0A7-H1	6-125	2A0B9-RJ	CHL 0 FAN OUT BIT 21 D4 TO 0U
G0	2A0A7-C0	6-125	2A0B9-AF	CHL 0 FAN OUT BIT 17 D4 TO 0U
G1	2A0A7-S2	6-125	2A0B9-AE	CHL 0 FAN OUT BIT 13 D4 TO 0U
G2	2A4A01J01B-06			
G3	2A4A01J01B-05			CHANNEL 0 EXTERNAL DATA BIT 19
H0	2A0A7-U3	6-133	2A0B9-AS	CHL 0 FAN OUT BIT 12 D4 TO 0U
H1	2A0A3-C0	6-129	2A0B9-AG	CHL 0 FAN OUT BIT 15 D4 TO 0U
H2	2A4A01J02B-06			
H3	2A4A01J02B-05			CHANNEL 0 EXTERNAL DATA BIT 19
I0	2A4A01J01A-04			
I1	2A4A01J01A-03			CHANNEL 0 EXTERNAL DATA BIT 13
I3	2A0B2-H1	6-131	2A0B9-RW	CHL 0 FAN OUT BIT 20 D4 TO 0U
J0	2A4A01J02A-04			
J1	2A4A01J02A-03			CHANNEL 0 EXTERNAL DATA BIT 13
J3	2A0B6-C0	6-127	2A0B9-RZ	CHL 0 FAN OUT BIT 18 D4 TO 0U
K0	2A0B6-S2	6-127	2A0B9-AR	CHL 0 FAN OUT BIT 14 D4 TO 0U
K2	2A4A01J01B-09			CHANNEL 0 EXTERNAL DATA BIT 21
K3	2A4A01J01B-10			
L0	2A4A01J02A-05			CHANNEL 0 EXTERNAL DATA BIT 14
L1	2A4A01J02A-06			
L2	2A4A01J02B-09			CHANNEL 0 EXTERNAL DATA BIT 21
L3	2A4A01J02B-10			
M0	2A4A01J01A-05			CHANNEL 0 EXTERNAL DATA BIT 14
M1	2A4A01J01A-06			
M2	2A4A01J01B-08			
M3	2A4A01J01B-07			CHANNEL 0 EXTERNAL DATA BIT 20
N0	2A4A01J01A-08			
N1	2A4A01J01A-07			CHANNEL 0 EXTERNAL DATA BIT 15
N2	2A4A01J02B-08			
N3	2A4A01J02B-07			CHANNEL 0 EXTERNAL DATA BIT 20
O0	2A4A01J02A-08			
O1	2A4A01J02A-07			CHANNEL 0 EXTERNAL DATA BIT 15
O2	2A0B5-B3	6-159	2A0B5-RC	NOT(BIT 20) CHL 0 0U TO FAN IN
O3	2A0B5-A3	6-159	2A0B5-RA	NOT(BIT 18) CHL 0 0U TO FAN IN
P0	2A0B5-D1	6-159	2A0B5-AD	NOT(BIT 12) CHL 0 0U TO FAN IN
P2	2A0B5-C2	6-159	2A0B5-RD	NOT(BIT 21) CHL 0 0U TO FAN IN
P3	2A0B5-B2	6-159	2A0B5-RB	NOT(BIT 19) CHL 0 0U TO FAN IN
Q0	2A0B5-D0	6-159	2A0B5-AE	NOT(BIT 13) CHL 0 0U TO FAN IN
Q1	2A0A5-E1	6-159	2A0B5-AF	NOT(BIT 14) CHL 0 0U TO FAN IN
Q2	2A4A01J01C-01			CHANNEL 0 EXTERNAL DATA BIT 22
Q3	2A4A01J01C-02			
R0	2A0B2-S2	6-131	2A0B9-AQ	CHL 0 FAN OUT BIT 16 D4 TO 0U
R1	2A0B5-E0	6-159	2A0B5-AG	NOT(BIT 15) CHL 0 0U TO FAN IN
R2	2A4A01J02C-01			CHANNEL 0 EXTERNAL DATA BIT 22
R3	2A4A01J02C-02			
S0	2A4A01J01A-10			
S1	2A4A01J01A-09			CHANNEL 0 EXTERNAL DATA BIT 16
S3	2A0A5-C3	6-159	2A0B5-RE	NOT(BIT 22) CHL 0 0U TO FAN IN
T0	2A4A01J02A-10			
T1	2A4A01J02A-09			CHANNEL 0 EXTERNAL DATA BIT 16
T3	2A0B5-D2	6-159	2A0B5-RG	NOT(BIT 23) CHL 0 0U TO FAN IN
U0	2A0A7-T2	6-133		CHL 0 NOT(CLEAR 0 RES (UPPER)
U1	2A0A7-S0	6-133		CHL 0 ENABLE 0U TRANSMISSION
U2	2A4A01J01C-05			CHL 0 EXTERNAL PARITY BIT 2
U3	2A4A01J01C-06			
V0	2A0B5-B0	6-159	2A0B5-AB	NOT(BIT 17) CHL 0 0U TO FAN IN
V1	2A0B5-C0	6-159	2A0B5-AC	NOT(BIT 16) CHL 0 0U TO FAN IN
V2	2A4A01J02C-05			CHL 0 EXTERNAL PARITY BIT 2
V3	2A4A01J02C-06			
W0	2A4A01J01B-02			CHANNEL 0 EXTERNAL DATA BIT 17
W1	2A4A01J01B-01			
W2	2A4A01J01C-04			CHANNEL 0 EXTERNAL DATA BIT 23
W3	2A4A01J01C-03			
X0	2A4A01J02B-02			CHANNEL 0 EXTERNAL DATA BIT 17
X1	2A4A01J02B-01			
X2	2A4A01J02C-04			CHANNEL 0 EXTERNAL DATA BIT 23
X3	2A4A01J02C-03			



CONTROL DATA
DEVELOPMENT DIVISION

CHANNEL 0-0U

LOC:2A0B9 PART NO.184003 SER. 008

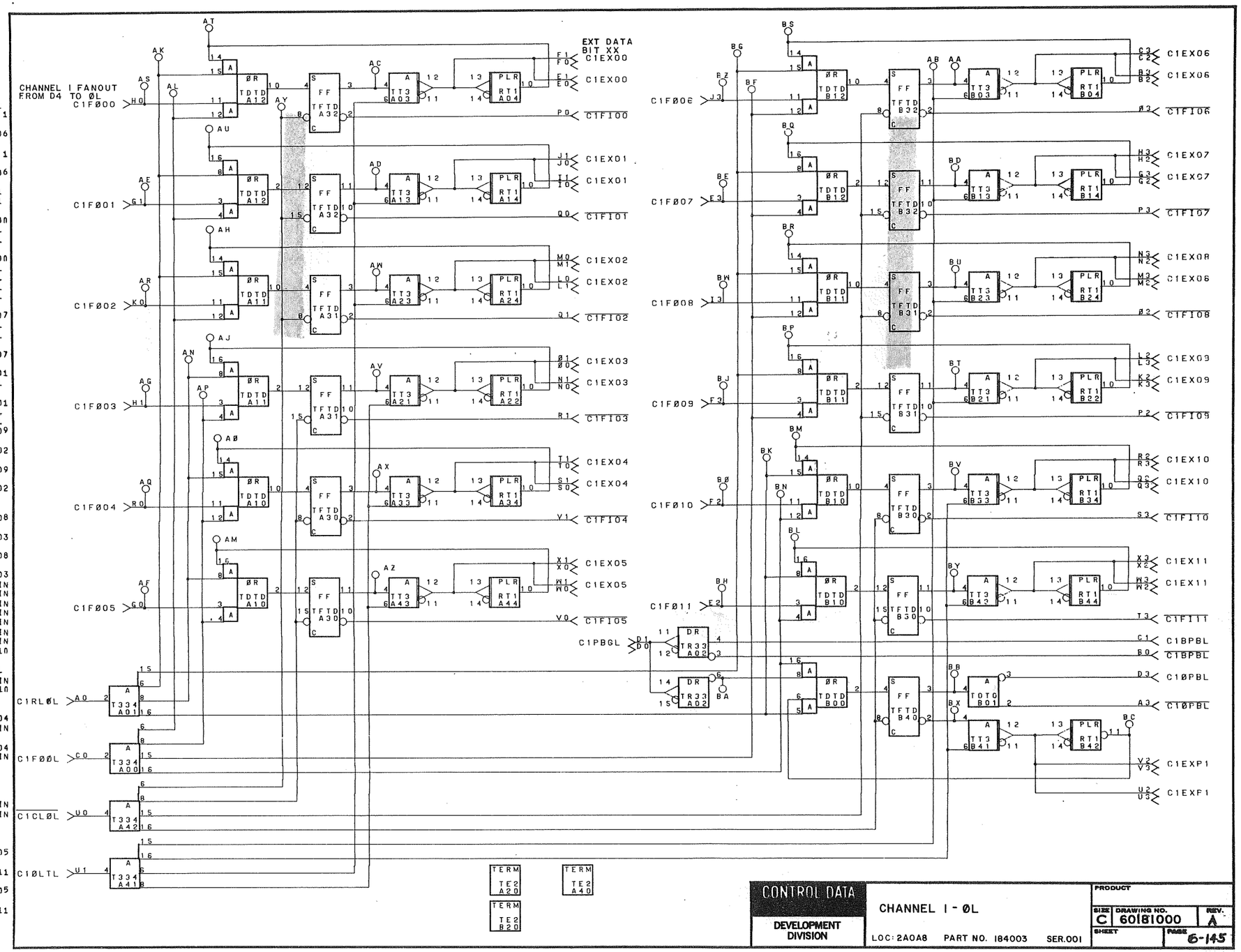
PRODUCT

SIZE C | DRAWING NO. 60181000 | REV. A

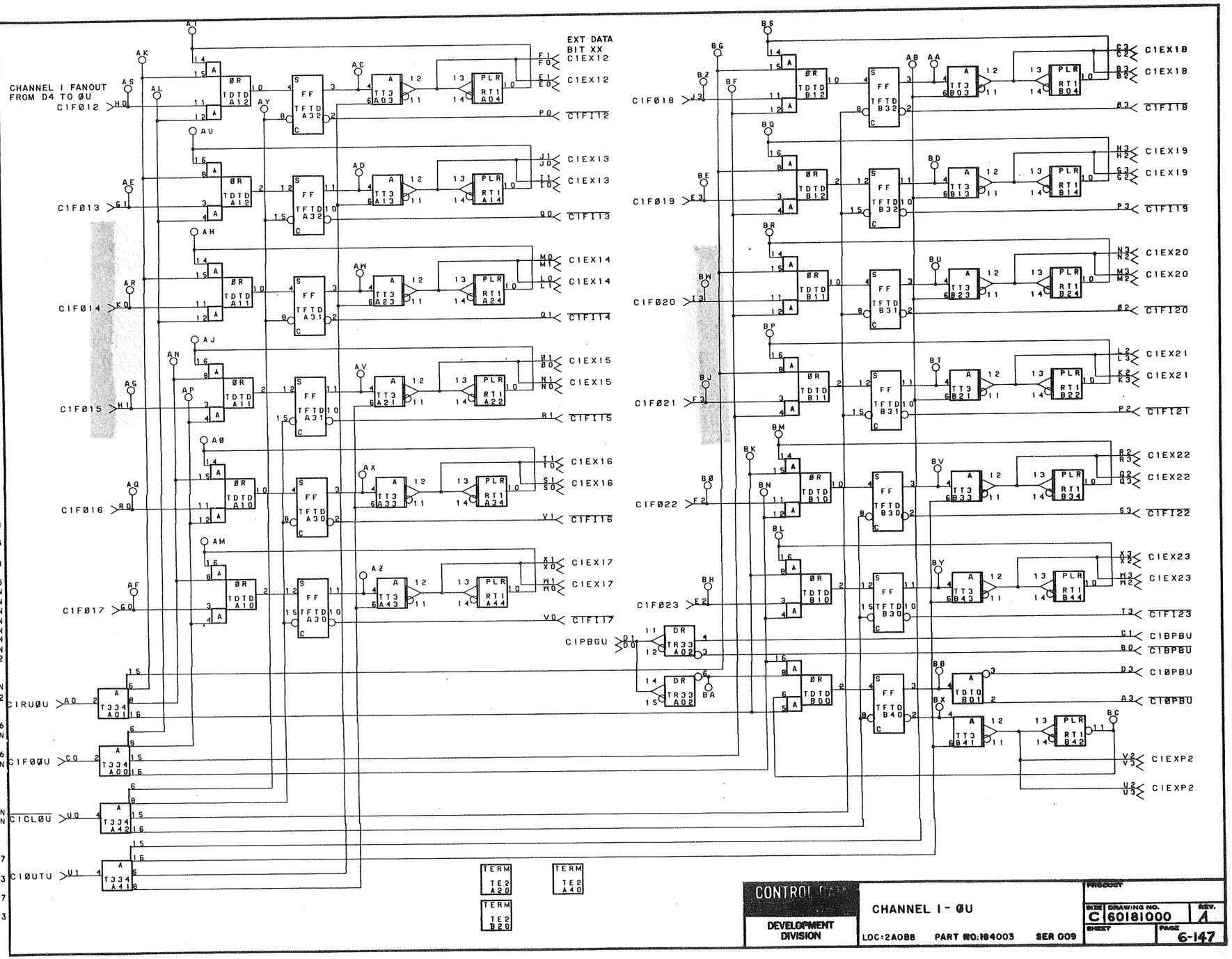
SHEET | PAGE 6-143

Set & clear ∅ upper 12 bits set parity Bit.

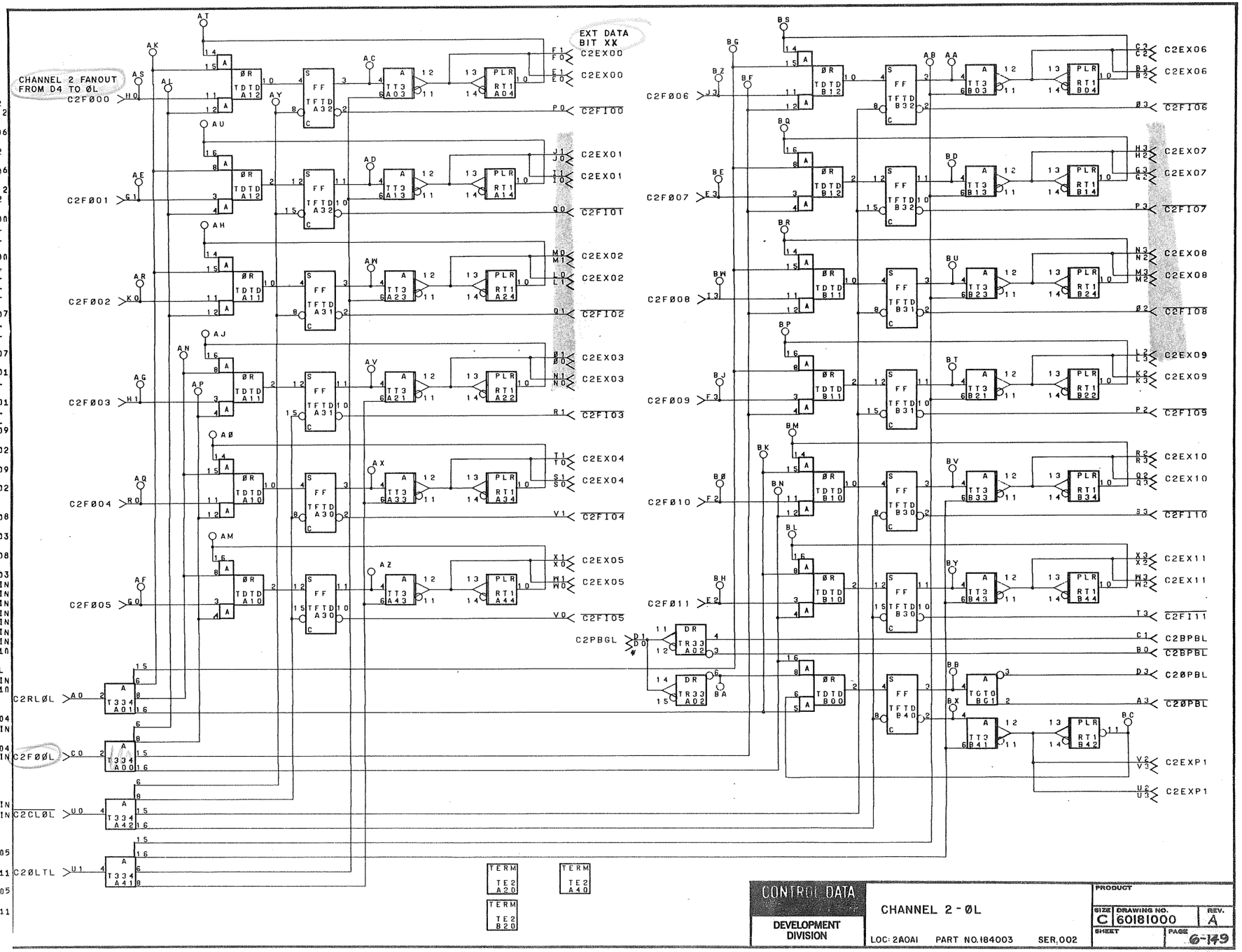
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A0A6-U1	6-135		CHAN 1 EXT RCVR TO O LOWER
A3	2A0A6-P0	6-135		NOT(OL PARITY RECEIVED) CHL 1
B0	2A0A6-L1	6-135		NOT(OL PARITY GENERATED) CHL 1
B2	2A4A02J03B-04			
B3	2A4A02J03B-03			CHANNEL 1 EXTERNAL DATA BIT 06
C0	2A0A6-S2	6-135		CHL 1 D4 FAN OUT TO OL REG
C1	2A0A6-L0	6-135		O LOWER PARITY GENERATED CHL 1
C2	2A4A02J04B-04			
C3	2A4A02J04B-03			CHANNEL 1 EXTERNAL DATA BIT 06
D0	2B1B0-E2	6- 7		
D1	2B1B0-E3	6- 7		LOWER PARITY BIT TO CHANNEL 1
D3	2A0A6-M1	6-135		O LOWER PARITY RECEIVED CHL 1
E0	2A4A02J03A-02			
E1	2A4A02J03A-01			CHANNEL 1 EXTERNAL DATA BIT 00
E2	2A0A2-D2	6-139	2A0A8-RH	CHL 1 FAN OUT BIT 11 D4 TO OL
E3	2A0A2-M3	6-139	2A0A8-RE	CHL 1 FAN OUT BIT 07 D4 TO OL
F0	2A4A02J04A-02			
F1	2A4A02J04A-01			CHANNEL 1 EXTERNAL DATA BIT 00
F2	2A0A3-D2	6-137	2A0A8-RG	CHL 1 FAN OUT BIT 10 D4 TO OL
F3	2A0A6-D2	6-135	2A0A8-RJ	CHL 1 FAN OUT BIT 09 D4 TO OL
G0	2A0A6-M3	6-135	2A0A8-AF	CHL 1 FAN OUT BIT 05 D4 TO OL
G1	2A0A6-B0	6-135	2A0A8-AE	CHL 1 FAN OUT BIT 01 D4 TO OL
G2	2A4A02J03B-06			
G3	2A4A02J03B-05			CHANNEL 1 EXTERNAL DATA BIT 07
H0	2A0A7-B0	6-133	2A0A8-AS	CHL 1 FAN OUT BIT 00 D4 TO OL
H1	2A0A2-B0	6-139	2A0A8-AG	CHL 1 FAN OUT BIT 03 D4 TO OL
H2	2A4A02J04B-06			
H3	2A4A02J04B-05			CHANNEL 1 EXTERNAL DATA BIT 07
I0	2A4A02J03A-04			
I1	2A4A02J03A-03			CHANNEL 1 EXTERNAL DATA BIT 01
I3	2A0A7-D2	6-133	2A0A8-RW	CHL 1 FAN OUT BIT 08 D4 TO OL
J0	2A4A02J04A-04			
J1	2A4A02J04A-03			CHANNEL 1 EXTERNAL DATA BIT 01
J3	2A0A3-M3	6-137	2A0A8-RZ	CHL 1 FAN OUT BIT 06 D4 TO OL
K0	2A0A3-B0	6-137	2A0A8-AR	CHL 1 FAN OUT BIT 02 D4 TO OL
K2	2A4A02J03B-09			CHANNEL 1 EXTERNAL DATA BIT 09
K3	2A4A02J03B-10			
L0	2A4A02J04A-05			CHANNEL 1 EXTERNAL DATA BIT 02
L1	2A4A02J04A-06			
L2	2A4A02J04B-09			CHANNEL 1 EXTERNAL DATA BIT 09
L3	2A4A02J04B-10			
M0	2A4A02J03A-05			CHANNEL 1 EXTERNAL DATA BIT 02
M1	2A4A02J03A-06			
M2	2A4A02J03B-08			
M3	2A4A02J03B-07			CHANNEL 1 EXTERNAL DATA BIT 08
N0	2A4A02J03A-08			
N1	2A4A02J03A-07			CHANNEL 1 EXTERNAL DATA BIT 03
N2	2A4A02J04B-08			
N3	2A4A02J04B-07			CHANNEL 1 EXTERNAL DATA BIT 08
O0	2A4A02J04A-08			
O1	2A4A02J04A-07			CHANNEL 1 EXTERNAL DATA BIT 03
O2	2A0A4-I2	6-157	2A0A4-RK	NOT(BIT 08) CHL 1 OL TO FAN IN
O3	2A0A4-H3	6-157	2A0A4-RJ	NOT(BIT 06) CHL 1 OL TO FAN IN
P0	2A0A4-H0	6-157	2A0A4-AN	NOT(BIT 00) CHL 1 OL TO FAN IN
P2	2A0A4-I3	6-157	2A0A4-RL	NOT(BIT 09) CHL 1 OL TO FAN IN
P3	2A0A4-G3	6-157	2A0A4-RH	NOT(BIT 07) CHL 1 OL TO FAN IN
Q0	2A0A4-H1	6-157	2A0A4-AM	NOT(BIT 01) CHL 1 OL TO FAN IN
Q1	2A0A4-G0	6-157	2A0A4-AL	NOT(BIT 02) CHL 1 OL TO FAN IN
Q2	2A4A02J03C-01			CHANNEL 1 EXTERNAL DATA BIT 10
Q3	2A4A02J03C-02			
R0	2A0A7-M3	6-133	2A0A8-AQ	CHL 1 FAN OUT BIT 04 D4 TO OL
R1	2A0A4-G1	6-157	2A0A4-AK	NOT(BIT 03) CHL 1 OL TO FAN IN
R2	2A4A02J04C-01			CHANNEL 1 EXTERNAL DATA BIT 10
R3	2A4A02J04C-02			
S0	2A4A02J03A-10			
S1	2A4A02J03A-09			CHANNEL 1 EXTERNAL DATA BIT 04
S3	2A0A4-J2	6-157	2A0A4-RM	NOT(BIT 10) CHL 1 OL TO FAN IN
T0	2A4A02J04A-10			
T1	2A4A02J04A-09			CHANNEL 1 EXTERNAL DATA BIT 04
T3	2A0A4-J3	6-157	2A0A4-RN	NOT(BIT 11) CHL 1 OL TO FAN IN
U0	2A0A6-N3	6-135		CHL 1 NOT(CLEAR O REG LOWER)
U1	2A0A6-S1	6-135		CHL 1 ENABLE OL TRANSMISSION
U2	2A4A02J03C-05			CHL 1 EXTERNAL PARITY BIT 1
U3	2A4A02J03C-06			
V0	2A0A4-F1	6-157	2A0A4-AH	NOT(BIT 05) CHL 1 OL TO FAN IN
V1	2A0A4-F0	6-157	2A0A4-AJ	NOT(BIT 04) CHL 1 OL TO FAN IN
V2	2A4A02J04C-05			CHL 1 EXTERNAL PARITY BIT 1
V3	2A4A02J04C-06			
W0	2A4A02J03B-02			
W1	2A4A02J03B-01			CHANNEL 1 EXTERNAL DATA BIT 05
W2	2A4A02J03C-04			
W3	2A4A02J03C-03			CHANNEL 1 EXTERNAL DATA BIT 11
X0	2A4A02J04B-02			
X1	2A4A02J04B-01			CHANNEL 1 EXTERNAL DATA BIT 05
X2	2A4A02J04C-04			
X3	2A4A02J04C-03			CHANNEL 1 EXTERNAL DATA BIT 11



PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A0A6-V1	6-135		CHAN 1 EXT RCVR TO 0 UPPER
A3	2A0A6-P1	6-135		NOT(OU PARITY RECEIVED) CHL 1
B0	2A0A6-N0	6-135		NOT(OU PARITY GENERATED) CHL 1
B2	2A4A02J01B-04			
B3	2A4A02J01B-03			CHANNEL 1 EXTERNAL DATA BIT 18
C0	2A0A6-03	6-135		CHL 1 D4 FAN OUT TO 0U REG
C1	2A0A6-00	6-135		0 UPPER PARITY GENERATED CHL 1
C2	2A4A02J02B-04			
C3	2A4A02J02B-03			CHANNEL 1 EXTERNAL DATA BIT 18
D0	2B1A0-E2	6- 5		
D1	2B1A0-E3	6- 5		UPPER PARITY BIT TO CHANNEL 1
D3	2A0A6-01	6-135		0 UPPER PARITY RECEIVED CHL 1
E0	2A4A02J01A-02			
E1	2A4A02J01A-01			CHANNEL 1 EXTERNAL DATA BIT 12
E2	2A0B3-S3	6-129	2A0B8-BH	CHL 1 FAN OUT BIT 23 D4 TO OU
E3	2A0B3-H0	6-129	2A0B8-BE	CHL 1 FAN OUT BIT 19 D4 TO OU
F0	2A4A02J02A-02			
F1	2A4A02J02A-01			CHANNEL 1 EXTERNAL DATA BIT 12
F2	2A0B6-H0	6-127	2A0B8-BD	CHL 1 FAN OUT BIT 22 D4 TO OU
F3	2A0B7-H0	6-125	2A0B8-BJ	CHL 1 FAN OUT BIT 21 D4 TO OU
G0	2A0B7-C1	6-125	2A0B8-AF	CHL 1 FAN OUT BIT 17 D4 TO OU
G1	2A0B7-S3	6-125	2A0B8-AE	CHL 1 FAN OUT BIT 13 D4 TO OU
G2	2A4A02J01B-06			
G3	2A4A02J01B-05			CHANNEL 1 EXTERNAL DATA BIT 19
H0	2A0A7-U2	6-133	2A0B8-AS	CHL 1 FAN OUT BIT 12 D4 TO OU
H1	2A0B3-C1	6-129	2A0B8-AG	CHL 1 FAN OUT BIT 15 D4 TO OU
H2	2A4A02J02B-06			
H3	2A4A02J02B-05			CHANNEL 1 EXTERNAL DATA BIT 19
I0	2A4A02J01A-04			
I1	2A4A02J01A-03			CHANNEL 1 EXTERNAL DATA BIT 13
I3	2A0B2-H0	6-131	2A0B8-BW	CHL 1 FAN OUT BIT 20 D4 TO OU
J0	2A4A02J02A-04			
J1	2A4A02J02A-03			CHANNEL 1 EXTERNAL DATA BIT 13
J3	2A0B6-C1	6-127	2A0B8-BZ	CHL 1 FAN OUT BIT 18 D4 TO OU
K0	2A0B6-S3	6-127	2A0B8-AR	CHL 1 FAN OUT BIT 14 D4 TO OU
K2	2A4A02J01B-09			CHANNEL 1 EXTERNAL DATA BIT 21
K3	2A4A02J01B-10			
L0	2A4A02J02A-05			CHANNEL 1 EXTERNAL DATA BIT 14
L1	2A4A02J02A-06			
L2	2A4A02J02B-09			CHANNEL 1 EXTERNAL DATA BIT 21
L3	2A4A02J02B-10			
M0	2A4A02J01A-05			CHANNEL 1 EXTERNAL DATA BIT 14
M1	2A4A02J01A-06			
M2	2A4A02J01B-08			
M3	2A4A02J01B-07			CHANNEL 1 EXTERNAL DATA BIT 20
N0	2A4A02J01A-08			
N1	2A4A02J01A-07			CHANNEL 1 EXTERNAL DATA BIT 15
N2	2A4A02J02B-08			
N3	2A4A02J02B-07			CHANNEL 1 EXTERNAL DATA BIT 20
O0	2A4A02J02A-08			
O1	2A4A02J02A-07			CHANNEL 1 EXTERNAL DATA BIT 15
O2	2A0B5-I2	6-159	2A0B5-RK	NOT(BIT 20) CHL 1 0U TO FAN IN
O3	2A0B5-H3	6-159	2A0B5-RJ	NOT(BIT 18) CHL 1 0U TO FAN IN
P0	2A0B5-H0	6-159	2A0B5-AN	NOT(BIT 12) CHL 1 0U TO FAN IN
P2	2A0B5-I3	6-159	2A0B5-BL	NOT(BIT 21) CHL 1 0U TO FAN IN
P3	2A0B5-G3	6-159	2A0B5-BH	NOT(BIT 19) CHL 1 0U TO FAN IN
Q0	2A0B5-H1	6-159	2A0B5-AM	NOT(BIT 13) CHL 1 0U TO FAN IN
Q1	2A0B5-G0	6-159	2A0B5-AL	NOT(BIT 14) CHL 1 0U TO FAN IN
Q2	2A4A02J01C-01			CHANNEL 1 EXTERNAL DATA BIT 22
Q3	2A4A02J01C-02			
R0	2A0B2-S3	6-131	2A0B8-AQ	CHL 1 FAN OUT BIT 16 D4 TO OU
R1	2A0B5-G1	6-159	2A0B5-AK	NOT(BIT 15) CHL 1 0U TO FAN IN
R2	2A4A02J02C-01			CHANNEL 1 EXTERNAL DATA BIT 22
R3	2A4A02J02C-02			
S0	2A4A02J01A-10			CHANNEL 1 EXTERNAL DATA BIT 16
S1	2A4A02J01A-09			NOT(BIT 22) CHL 1 0U TO FAN IN
S3	2A0B5-J2	6-159	2A0B5-BM	
T0	2A4A02J02A-10			
T1	2A4A02J02A-09			CHANNEL 1 EXTERNAL DATA BIT 16
T3	2A0B5-J3	6-159	2A0B5-BN	NOT(BIT 23) CHL 1 0U TO FAN IN
U0	2A0A6-T2	6-135		CHL 1 NOT(CLEAR 0 REG UPPER)
U1	2A0A6-S0	6-135		CHL 1 ENABLE 0U TRANSMISSION
U2	2A4A02J01C-05			CHAN 1 EXT PARITY BIT 2
U3	2A4A02J01C-06			
V0	2A0B5-F1	6-159	2A0B5-AH	NOT(BIT 17) CHL 1 0U TO FAN IN
V1	2A0B5-F0	6-159	2A0B5-AJ	NOT(BIT 16) CHL 1 0U TO FAN IN
V2	2A4A02J02C-05			CHAN 1 EXT PARITY BIT 2
V3	2A4A02J02C-06			
W0	2A4A02J01B-02			CHANNEL 1 EXTERNAL DATA BIT 17
W1	2A4A02J01B-01			
W2	2A4A02J01C-04			CHANNEL 1 EXTERNAL DATA BIT 23
W3	2A4A02J01C-03			
X0	2A4A02J02B-02			CHANNEL 1 EXTERNAL DATA BIT 17
X1	2A4A02J02B-01			
X2	2A4A02J02C-04			CHANNEL 1 EXTERNAL DATA BIT 23
X3	2A4A02J02C-03			

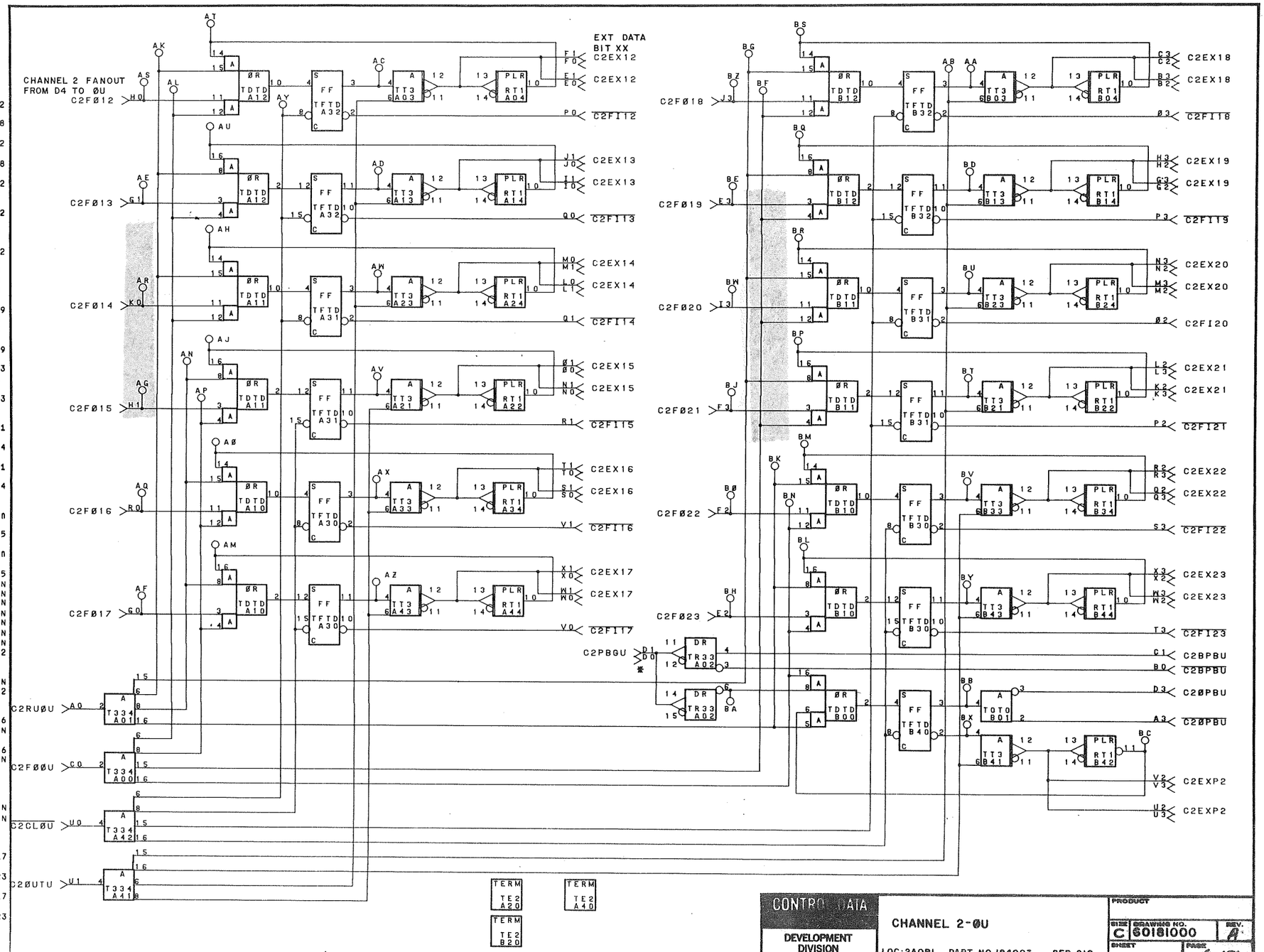


PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A0A3*U1	6-137		CHAN 2 EXT RCVR TO 0 LOWER
A3	2A0A3*P0	6-137		NOT(OL PARITY RECEIVED) CHL 2
B0	2A0A3*L1	6-137		NOT(OL PARITY GENERATED) CHL 2
B2	2A4A03J03R*04			
B3	2A4A03J03R*03			CHANNEL 2 EXTERNAL DATA BIT 06
C0	2A0A3*S2	6-137		CHL 2 D4 FAN OUT TO OL REG
C1	2A0A3*L0	6-137		0 LWR PARITY GENERATED*CHAN 2
C2	2A4A03J04B*04			
C3	2A4A03J04B*03			CHANNEL 2 EXTERNAL DATA BIT 06
D0	2R1B0*C2	6- 7		
D1	2R1B0*C3	6- 7		NOT LOWER PARITY BIT TO CHAN 2
D3	2A0A3*M1	6-137		0 LOWER PARITY RECEIVED CHL 2
E0	2A4A03J03A*02			
E1	2A4A03J03A*01			CHANNEL 2 EXTERNAL DATA BIT 00
E2	2A0A2*B2	6-139	2A0A1*RH	CHL 2 FAN OUT BIT 11 D4 TO OL
E3	2A0A2*R3	6-139	2A0A1*RE	CHL 2 FAN OUT BIT 07 D4 TO OL
F0	2A4A03J04A*02			
F1	2A4A03J04A*01			CHANNEL 2 EXTERNAL DATA BIT 00
F2	2A0A3*B2	6-137	2A0A1*RD	CHL 2 FAN OUT BIT 10 D4 TO OL
F3	2A0A6*B2	6-135	2A0A1*RJ	CHL 2 FAN OUT BIT 09 D4 TO OL
G0	2A0A6*R3	6-135	2A0A1*AF	CHL 2 FAN OUT BIT 05 D4 TO OL
G1	2A0A6*B1	6-135	2A0A1*AE	CHL 2 FAN OUT BIT 01 D4 TO OL
G2	2A4A03J03B*06			
G3	2A4A03J03B*05			CHANNEL 2 EXTERNAL DATA BIT 07
H0	2A0A7*B1	6-133	2A0A1*AS	CHL 2 FAN OUT BIT 00 D4 TO OL
H1	2A0A2*B1	6-139	2A0A1*AG	CHL 2 FAN OUT BIT 03 D4 TO OL
H2	2A4A03J04B*06			
H3	2A4A03J04B*05			CHANNEL 2 EXTERNAL DATA BIT 07
I0	2A4A03J03A*04			
I1	2A4A03J03A*03			CHANNEL 2 EXTERNAL DATA BIT 01
I3	2A0A7*B2	6-133	2A0A1*RW	CHL 2 FAN OUT BIT 08 D4 TO OL
J0	2A4A03J04A*04			
J1	2A4A03J04A*03			CHANNEL 2 EXTERNAL DATA BIT 01
J3	2A0A3*R3	6-137	2A0A1*BZ	CHL 2 FAN OUT BIT 06 D4 TO OL
K0	2A0A3*B1	6-137	2A0A1*AR	CHL 2 FAN OUT BIT 02 D4 TO OL
K2	2A4A03J03R*09			CHANNEL 2 EXTERNAL DATA BIT 09
K3	2A4A03J03R*10			
L0	2A4A03J04A*05			CHANNEL 2 EXTERNAL DATA BIT 02
L1	2A4A03J04A*06			
L2	2A4A03J04B*09			CHANNEL 2 EXTERNAL DATA BIT 09
L3	2A4A03J04B*10			
M0	2A4A03J03A*05			CHANNEL 2 EXTERNAL DATA BIT 02
M1	2A4A03J03A*06			
M2	2A4A03J03B*08			
M3	2A4A03J03B*07			CHANNEL 2 EXTERNAL DATA BIT 08
N0	2A4A03J03A*08			
N1	2A4A03J03A*07			CHANNEL 2 EXTERNAL DATA BIT 03
N2	2A4A03J04B*08			
N3	2A4A03J04B*07			CHANNEL 2 EXTERNAL DATA BIT 08
O0	2A4A03J04A*08			
O1	2A4A03J04A*07			CHANNEL 2 EXTERNAL DATA BIT 03
O2	2A0A4*U3	6-157	2A0A4*RT	NOT(BIT 08) CHL 2 0L TO FAN IN
O3	2A0A4*R2	6-157	2A0A4*RQ	NOT(BIT 06) CHL 2 0L TO FAN IN
P0	2A0A4*P0	6-157	2A0A4*AQ	NOT(BIT 00) CHL 2 0L TO FAN IN
P2	2A0A4*T3	6-157	2A0A4*RS	NOT(BIT 09) CHL 2 0L TO FAN IN
P3	2A0A4*S3	6-157	2A0A4*RR	NOT(BIT 07) CHL 2 0L TO FAN IN
Q0	2A0A4*01	6-157	2A0A4*AP	NOT(BIT 01) CHL 2 0L TO FAN IN
Q1	2A0A4*P1	6-157	2A0A4*AR	NOT(BIT 02) CHL 2 0L TO FAN IN
Q2	2A4A03J03C*01			CHANNEL 2 EXTERNAL DATA BIT 10
Q3	2A4A03J03C*02			
R0	2A0A7*R3	6-133	2A0A1*AQ	CHL 2 FAN OUT BIT 04 D4 TO OL
R1	2A0A4*00	6-157	2A0A4*AO	NOT(BIT 03) CHL 2 0L TO FAN IN
R2	2A4A03J04C*01			CHANNEL 2 EXTERNAL DATA BIT 10
R3	2A4A03J04C*02			
S0	2A4A03J03A*10			
S1	2A4A03J03A*09			CHANNEL 2 EXTERNAL DATA BIT 04
S3	2A0A4*R3	6-157	2A0A4*RP	NOT(BIT 10) CHL 2 0L TO FAN IN
T0	2A4A03J04A*10			
T1	2A4A03J04A*09			CHANNEL 2 EXTERNAL DATA BIT 04
T3	2A0A4*Q2	6-157	2A0A4*RO	NOT(BIT 11) CHL 2 0L TO FAN IN
U0	2A0A3*N3	6-137		CHL 2 NOT(CLEAR 0 REG LOWER)
U1	2A0A3*S1	6-137		CHL 2 ENABLE OL TRANSMISSION
U2	2A4A03J03C*05			CHL 2 EXTERNAL PARITY BIT 1
U3	2A4A03J03C*06			
V0	2A0A4*R0	6-157	2A0A4*AT	NOT(BIT 05) CHL 2 0L TO FAN IN
V1	2A0A4*Q0	6-157	2A0A4*AS	NOT(BIT 04) CHL 2 0L TO FAN IN
V2	2A4A03J04C*05			CHL 2 EXTERNAL PARITY BIT 1
V3	2A4A03J04C*06			
W0	2A4A03J03B*02			
W1	2A4A03J03B*01			CHANNEL 2 EXTERNAL DATA BIT 05
W2	2A4A03J03C*04			
W3	2A4A03J03C*03			CHANNEL 2 EXTERNAL DATA BIT 11
X0	2A4A03J04B*02			
X1	2A4A03J04B*01			CHANNEL 2 EXTERNAL DATA BIT 05
X2	2A4A03J04C*04			
X3	2A4A03J04C*03			CHANNEL 2 EXTERNAL DATA BIT 11



CONTROL DATA	CHANNEL 2 - ØL	PRODUCT
DEVELOPMENT DIVISION	LOC: 2A0A1 PART NO. 184003 SER. 002	SIZE C · DRAWING NO. 60181000 · REV. A · SHEET · PAGE 6-149

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A0A3*V1	6-137		CHAN 2 EXT RCVR TO 0 UPPER
A3	2A0A3*P1	6-137		NOT(0U PARITY RECEIVED) CHL 2
B0	2A0A3*N0	6-137		NOT(0U PARITY GENERATED) CHL 2
B2	2A4A03J01B-04			
B3	2A4A03J01B-03			CHANNEL 2 EXTERNAL DATA BIT 18
C0	2A0A3*03	6-137		CHL 2 D4 FAN OUT TO 0U REG
C1	2A0A3*00	6-137		0 UPPER PARITY GENERATED CHL 2
C2	2A4A03J02B-04			
C3	2A4A03J02B-03			CHANNEL 2 EXTERNAL DATA BIT 18
D0	2B1A0*C2	6- 5		
D1	2B1A0*C3	6- 5		NOT UPPER PARITY BIT TO CHAN 2
D3	2A0A3*01	6-137		0 UPPER PARITY RECEIVED CHL 2
E0	2A4A03J01A-02			
E1	2A4A03J01A-01			CHANNEL 2 EXTERNAL DATA BIT 12
E2	2A0B3*V2	6-129	2A0B1-RH	CHL 2 FAN OUT BIT 23 D4 TO 0U
E3	2A0B3*H1	6-129	2A0B1-RE	CHL 2 FAN OUT BIT 19 D4 TO 0U
F0	2A4A03J02A-02			
F1	2A4A03J02A-01			CHANNEL 2 EXTERNAL DATA BIT 12
F2	2A0B6*M1	6-127	2A0B1-RO	CHL 2 FAN OUT BIT 22 D4 TO 0U
F3	2A0B7*M1	6-125	2A0B1-RJ	CHL 2 FAN OUT BIT 21 D4 TO 0U
G0	2A0B7*F1	6-125	2A0B1-AF	CHL 2 FAN OUT BIT 17 D4 TO 0U
G1	2A0B7*V2	6-125	2A0B1-AE	CHL 2 FAN OUT BIT 13 D4 TO 0U
G2	2A4A03J01B-06			
G3	2A4A03J01B-05			CHANNEL 2 EXTERNAL DATA BIT 19
H0	2A0A7*X3	6-133	2A0B1-AS	CHL 2 FAN OUT BIT 12 D4 TO 0U
H1	2A0B3*F1	6-129	2A0B1-AG	CHL 2 FAN OUT BIT 15 D4 TO 0U
H2	2A4A03J02B-06			
H3	2A4A03J02B-05			CHANNEL 2 EXTERNAL DATA BIT 19
I0	2A4A03J01A-04			
I1	2A4A03J01A-03			CHANNEL 2 EXTERNAL DATA BIT 13
I3	2A0B2*M1	6-131	2A0B1-RW	CHL 2 FAN OUT BIT 20 D4 TO 0U
J0	2A4A03J02A-04			
J1	2A4A03J02A-03			CHANNEL 2 EXTERNAL DATA BIT 13
J3	2A0B6*F1	6-127	2A0B1-RZ	CHL 2 FAN OUT BIT 18 D4 TO 0U
K0	2A0B6*V2	6-127	2A0B1-AR	CHL 2 FAN OUT BIT 14 D4 TO 0U
K2	2A4A03J01B-09			CHANNEL 2 EXTERNAL DATA BIT 21
K3	2A4A03J01B-10			
L0	2A4A03J02A-05			CHANNEL 2 EXTERNAL DATA BIT 14
L1	2A4A03J02A-06			
L2	2A4A03J02B-09			CHANNEL 2 EXTERNAL DATA BIT 21
L3	2A4A03J02B-10			
M0	2A4A03J01A-05			CHANNEL 2 EXTERNAL DATA BIT 14
M1	2A4A03J01A-06			
M2	2A4A03J01B-08			
M3	2A4A03J01B-07			CHANNEL 2 EXTERNAL DATA BIT 20
N0	2A4A03J01A-08			
N1	2A4A03J01A-07			CHANNEL 2 EXTERNAL DATA BIT 15
N2	2A4A03J02B-08			
N3	2A4A03J02B-07			CHANNEL 2 EXTERNAL DATA BIT 20
O0	2A4A03J02A-08			
O1	2A4A03J02A-07			CHANNEL 2 EXTERNAL DATA BIT 15
O2	2A0B5*U3	6-159	2A0B5-RT	NOT(BIT 20) CHL 2 0U TO FAN IN
O3	2A0B5*R2	6-159	2A0B5-RQ	NOT(BIT 18) CHL 2 0U TO FAN IN
P0	2A0B5*P0	6-159	2A0B5-AQ	NOT(BIT 12) CHL 2 0U TO FAN IN
P2	2A0B5*T3	6-159	2A0B5-RS	NOT(BIT 21) CHL 2 0U TO FAN IN
P3	2A0B5*S3	6-159	2A0B5-RR	NOT(BIT 19) CHL 2 0U TO FAN IN
Q0	2A0B5*01	6-159	2A0B5-AP	NOT(BIT 13) CHL 2 0U TO FAN IN
Q1	2A0B5*P1	6-159	2A0B5-AR	NOT(BIT 14) CHL 2 0U TO FAN IN
Q2	2A4A03J01C-01			CHANNEL 2 EXTERNAL DATA BIT 22
Q3	2A4A03J01C-02			
R0	2A0B2*V2	6-131	2A0B1-AQ	CHL 2 FAN OUT BIT 16 D4 TO 0U
R1	2A0B5*00	6-159	2A0B5-AO	NOT(BIT 15) CHL 2 0U TO FAN IN
R2	2A4A03J02C-01			CHANNEL 2 EXTERNAL DATA BIT 22
R3	2A4A03J02C-02			
S0	2A4A03J01A-10			
S1	2A4A03J01A-09			CHANNEL 2 EXTERNAL DATA BIT 16
S3	2A0B5*R3	6-159	2A0B5-RP	NOT(BIT 22) CHL 2 0U TO FAN IN
T0	2A4A03J02A-10			
T1	2A4A03J02A-09			CHANNEL 2 EXTERNAL DATA BIT 16
T3	2A0B5*Q2	6-159	2A0B5-RO	NOT(BIT 23) CHL 2 0U TO FAN IN
U0	2A0A3*T2	6-137		CHL 2 NOT(CLEAR 0 REG UPPER)
U1	2A0A3*S0	6-137		CHL 2 ENABLE 0U TRANSMISSION
U2	2A4A03J01C-05			CHAN 2 EXT PARITY BIT 2
U3	2A4A03J01C-06			
V0	2A0B5*R0	6-159	2A0B5-AT	NOT(BIT 17) CHL 2 0U TO FAN IN
V1	2A0B5*Q0	6-159	2A0B5-AS	NOT(BIT 16) CHL 2 0U TO FAN IN
V2	2A4A03J02C-05			CHAN 2 EXT PARITY BIT 2
V3	2A4A03J02C-06			
W0	2A4A03J01A-02			
W1	2A4A03J01A-01			CHANNEL 2 EXTERNAL DATA BIT 17
W2	2A4A03J01C-04			
W3	2A4A03J01C-03			CHANNEL 2 EXTERNAL DATA BIT 23
X0	2A4A03J02B-02			
X1	2A4A03J02B-01			CHANNEL 2 EXTERNAL DATA BIT 17
X2	2A4A03J02C-04			
X3	2A4A03J02C-03			CHANNEL 2 EXTERNAL DATA BIT 23



CONTROL DATA
DEVELOPMENT DIVISION

CHANNEL 2-0U

LOC:2A0B1 PART NO.184003 SER.010

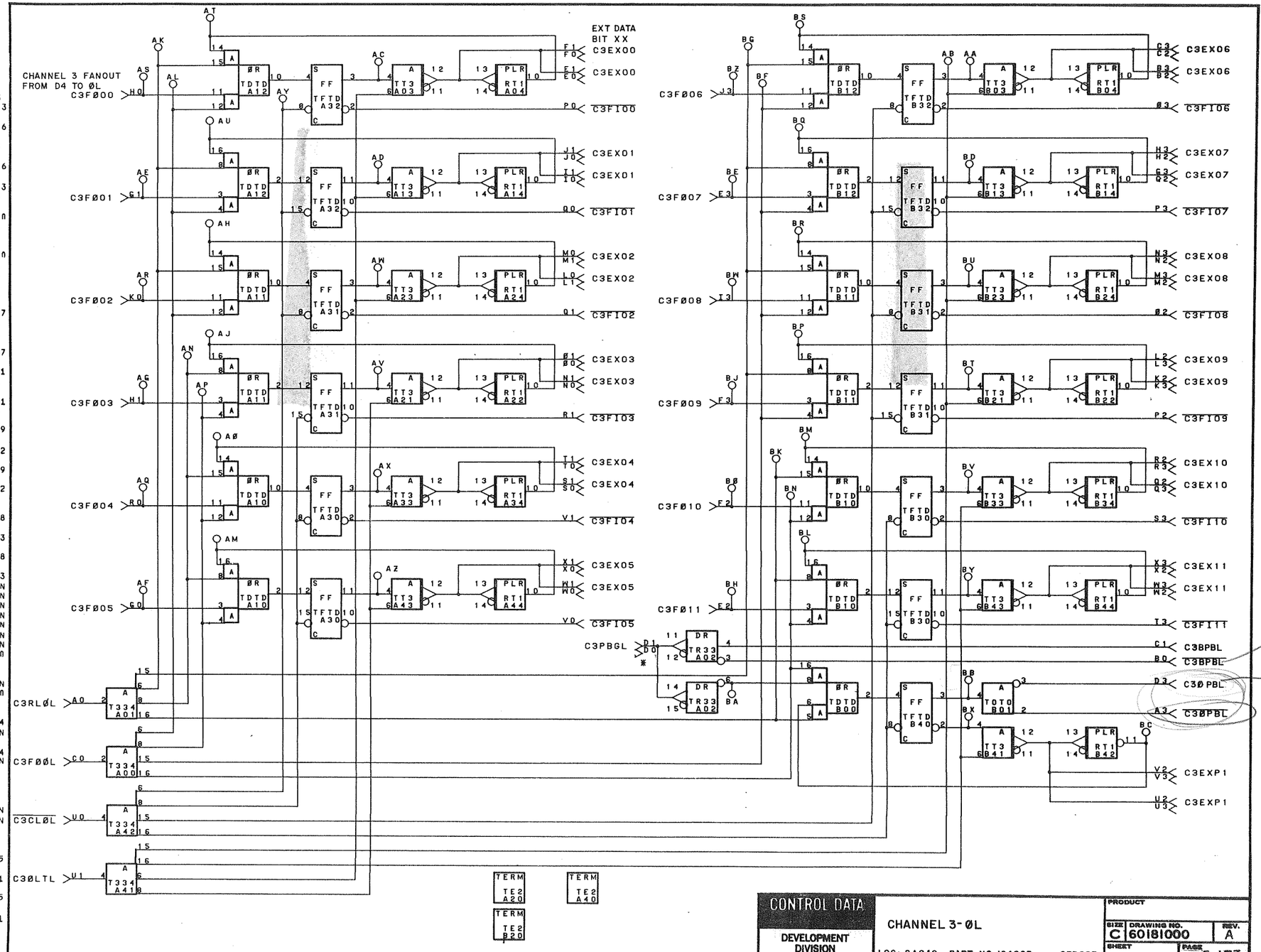
PRODUCT

SIZE C | DRAWING NO. 60181000 | REV. A

SHEET | PAGE 6-151

6-126-010

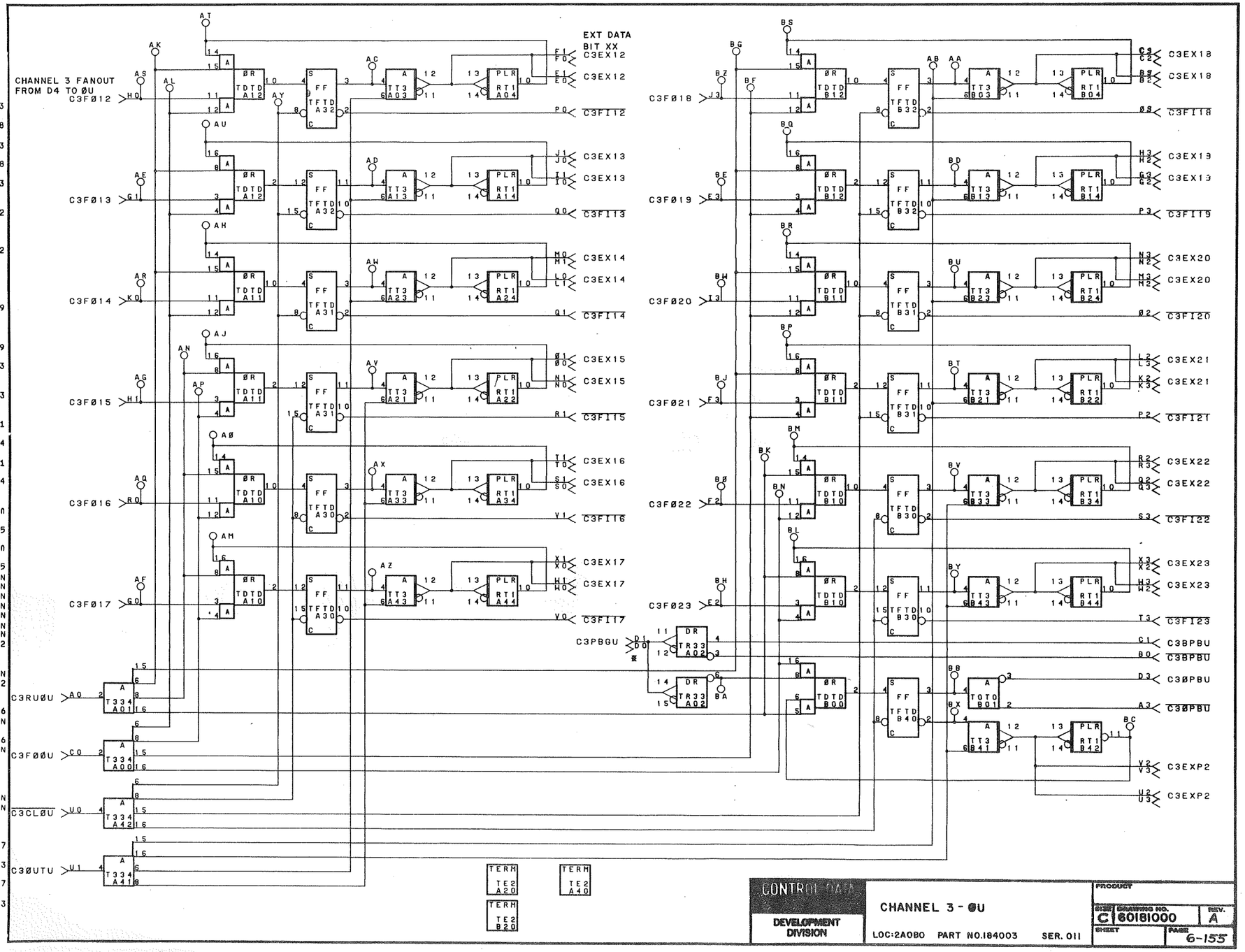
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A0A2=U1	6-139		CHAN 3 EXT RCVR TO 0 LOWER
A3	2A0A2=P0	6-139		NOT(OL PARITY RECEIVED) CHL 3
B0	2A0A2=L1	6-139		NOT(OL PARITY GENERATED) CHL 3
B2	2A4A04J03B=04			
B3	2A4A04J03B=03			CHANNEL 3 EXTERNAL DATA BIT 06
C0	2A0A2=S2	6-139		CHL 3 D4 FAN OUT TO OL REG
C1	2A0A2=L0	6-139		0 LWR PARITY GENERATED=CHAN 3
C2	2A4A04J04B=04			
C3	2A4A04J04B=03			CHANNEL 3 EXTERNAL DATA BIT 06
D0	2B1B0=D2	6= 7		
D1	2B1B0=D3	6= 7		NOT LOWER PARITY BIT TO CHAN 3
D3	2A0A2=M1	6-139		0 LOWER PARITY RECEIVED CHL 3
E0	2A4A04J03A=02			
E1	2A4A04J03A=01			CHANNEL 3 EXTERNAL DATA BIT 00
E2	2A0A2=D3	6-139	2A0A0=BH	CHL 3 FAN OUT BIT 11 D4 TO OL
E3	2A0A2=R2	6-139	2A0A0=BE	CHL 3 FAN OUT BIT 07 D4 TO OL
F0	2A4A04J04A=02			
F1	2A4A04J04A=01			CHANNEL 3 EXTERNAL DATA BIT 00
F2	2A0A3=D3	6-137	2A0A0=BD	CHL 3 FAN OUT BIT 10 D4 TO OL
F3	2A0A6=D3	6-135	2A0A0=BJ	CHL 3 FAN OUT BIT 09 D4 TO OL
G0	2A0A6=R2	6-135	2A0A0=AF	CHL 3 FAN OUT BIT 05 D4 TO OL
G1	2A0A6=E0	6-135	2A0A0=AE	CHL 3 FAN OUT BIT 01 D4 TO OL
G2	2A4A04J03B=06			
G3	2A4A04J03B=05			CHANNEL 3 EXTERNAL DATA BIT 07
H0	2A0A7=E0	6-133	2A0A0=AS	CHL 3 FAN OUT BIT 00 D4 TO OL
H1	2A0A2=E0	6-139	2A0A0=AG	CHL 3 FAN OUT BIT 03 D4 TO OL
H2	2A4A04J04B=06			
H3	2A4A04J04B=05			CHANNEL 3 EXTERNAL DATA BIT 07
I0	2A4A04J03A=04			
I1	2A4A04J03A=03			CHANNEL 3 EXTERNAL DATA BIT 01
I3	2A0A7=D3	6-133	2A0A0=BW	CHL 3 FAN OUT BIT 08 D4 TO OL
J0	2A4A04J04A=04			
J1	2A4A04J04A=03			CHANNEL 3 EXTERNAL DATA BIT 01
J3	2A0A3=R2	6-137	2A0A0=BZ	CHL 3 FAN OUT BIT 06 D4 TO OL
K0	2A0A3=E0	6-137	2A0A0=AR	CHL 3 FAN OUT BIT 02 D4 TO OL
K2	2A4A04J03B=09			CHANNEL 3 EXTERNAL DATA BIT 09
K3	2A4A04J03B=10			
L0	2A4A04J04A=05			CHANNEL 3 EXTERNAL DATA BIT 02
L1	2A4A04J04A=06			
L2	2A4A04J04B=09			CHANNEL 3 EXTERNAL DATA BIT 09
L3	2A4A04J04B=10			
M0	2A4A04J03A=05			CHANNEL 3 EXTERNAL DATA BIT 02
M1	2A4A04J03A=06			
M2	2A4A04J03B=08			
M3	2A4A04J03B=07			CHANNEL 3 EXTERNAL DATA BIT 08
N0	2A4A04J03A=08			
N1	2A4A04J03A=07			CHANNEL 3 EXTERNAL DATA BIT 03
N2	2A4A04J04B=08			
N3	2A4A04J04B=07			CHANNEL 3 EXTERNAL DATA BIT 08
O0	2A4A04J04A=08			
O1	2A4A04J04A=07			CHANNEL 3 EXTERNAL DATA BIT 03
O2	2A0A4=W3	6-157	2A0A4=BW	NOT(BIT 08) CHL 3 OL TO FAN IN
O3	2A0A4=X2	6-157	2A0A4=BZ	NOT(BIT 06) CHL 3 OL TO FAN IN
P0	2A0A4=S1	6-157	2A0A4=AW	NOT(BIT 00) CHL 3 OL TO FAN-IN
P2	2A0A4=W2	6-157	2A0A4=BX	NOT(BIT 09) CHL 3 OL TO FAN IN
P3	2A0A4=X3	6-157	2A0A4=BY	NOT(BIT 07) CHL 3 OL TO FAN IN
Q0	2A0A4=S0	6-157	2A0A4=AV	NOT(BIT 01) CHL 3 OL TO FAN IN
Q1	2A0A4=X1	6-157	2A0A4=AZ	NOT(BIT 02) CHL 3 OL TO FAN IN
Q2	2A4A04J03C=01			CHANNEL 3 EXTERNAL DATA BIT 10
Q3	2A4A04J03C=02			
R0	2A0A7=R2	6-133	2A0A0=AQ	CHL 3 FAN OUT BIT 04 D4 TO OL
R1	2A0A4=R1	6-157	2A0A4=AU	NOT(BIT 03) CHL 3 OL TO FAN IN
R2	2A4A04J04C=01			CHANNEL 3 EXTERNAL DATA BIT 10
R3	2A4A04J04C=02			
S0	2A4A04J03A=10			
S1	2A4A04J03A=09			CHANNEL 3 EXTERNAL DATA BIT 04
S3	2A0A4=V2	6-157	2A0A4=BV	NOT(BIT 10) CHL 3 OL TO FAN IN
T0	2A4A04J04A=10			
T1	2A4A04J04A=09			CHANNEL 3 EXTERNAL DATA BIT 04
T3	2A0A4=V3	6-157	2A0A4=BU	NOT(BIT 11) CHL 3 OL TO FAN IN
U0	2A0A2=N3	6-139		CHL 3 NOT(CLEAR 0 REG LOWER)
U1	2A0A2=S1	6-139		CHL 3 ENABLE OL TRANSMISSION
U2	2A4A04J03C=05			CHL 3 EXTERNAL PARITY BIT 1
U3	2A4A04J03C=06			
V0	2A0A4=X0	6-157	2A0A4=AY	NOT(BIT 05) CHL 3 OL TO FAN IN
V1	2A0A4=W0	6-157	2A0A4=AX	NOT(BIT 04) CHL 3 OL TO FAN IN
V2	2A4A04J04C=05			CHL 3 EXTERNAL PARITY BIT 1
V3	2A4A04J04C=06			
W0	2A4A04J03B=02			
W1	2A4A04J03B=01			CHANNEL 3 EXTERNAL DATA BIT 05
W2	2A4A04J03C=04			
W3	2A4A04J03C=03			CHANNEL 3 EXTERNAL DATA BIT 11
X0	2A4A04J04B=02			
X1	2A4A04J04B=01			CHANNEL 3 EXTERNAL DATA BIT 05
X2	2A4A04J04C=04			
X3	2A4A04J04C=03			CHANNEL 3 EXTERNAL DATA BIT 11



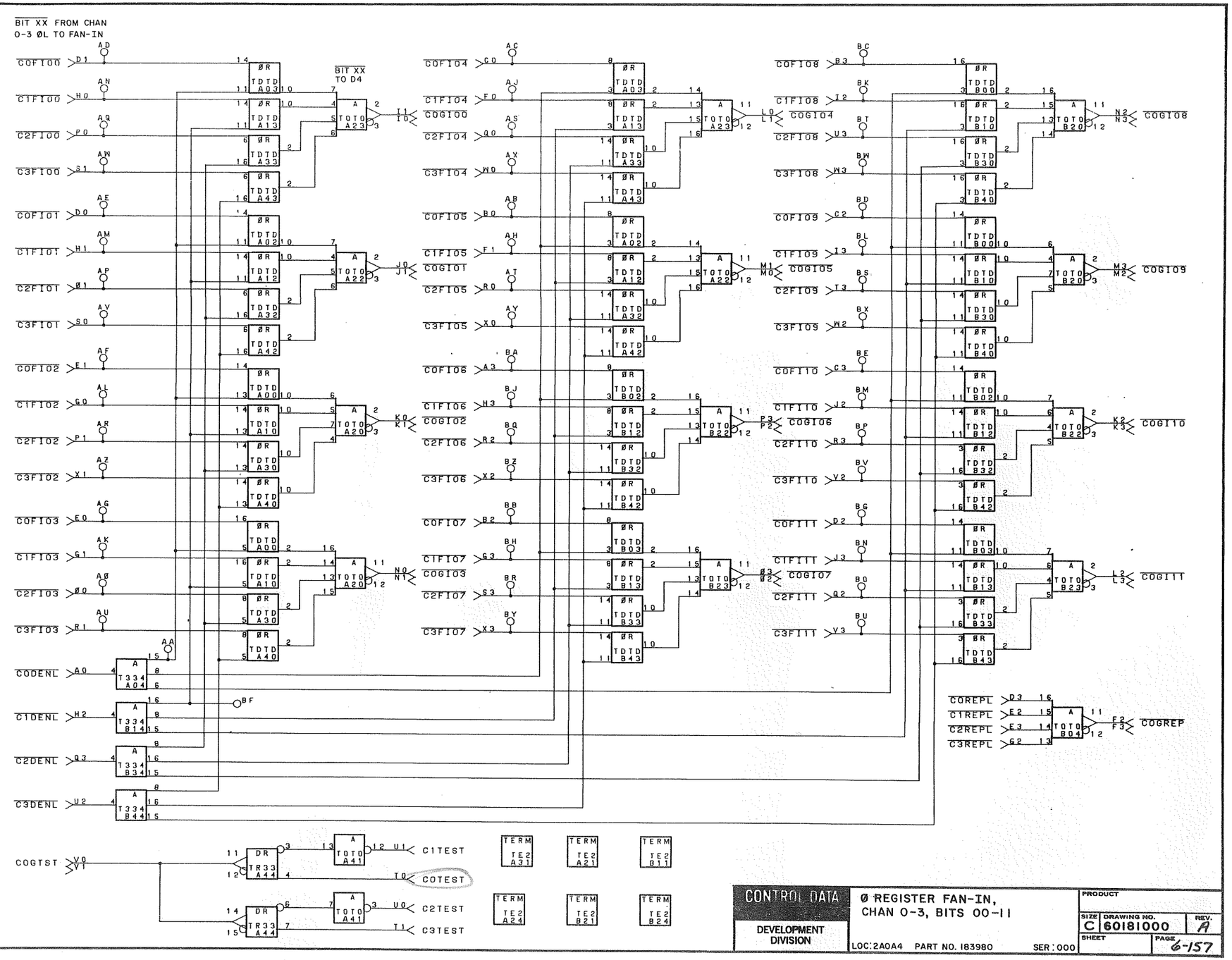
CONTROL DATA	CHANNEL 3-ØL	PRODUCT
DEVELOPMENT DIVISION	LOC: 2A0A0 PART NO. 184003 SER 003	SIZE C · DRAWING NO. 60181000 · REV. A · SHEET · PAGE 6-153

339

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A0A2*V1	6*139		CHAN 3 EXT RCVR TO 0 UPPER
A3	2A0A2*P1	6*139		NOT(OU PARITY RECEIVED) CHL 3
B0	2A0A2*N0	6*139		NOT(OU PARITY GENERATED) CHL 3
B2	2A4A04J01B*04			
B3	2A4A04J01B*03			CHANNEL 3 EXTERNAL DATA BIT 18
C0	2A0A2*03	6*139		CHL 3 D4 FAN OUT TO OU REG
C1	2A0A2*00	6*139		0 UPPER PARITY GENERATED CHL 3
C2	2A4A04J02B*04			
C3	2A4A04J02B*03			CHANNEL 3 EXTERNAL DATA BIT 18
D0	2B1A0*D2	6* 5		
D1	2B1A0*D3	6* 5		NOT UPPER PARITY BIT TO CHAN 3
D3	2A0A2*01	6*139		0 UPPER PARITY RECEIVED CHL 3
E0	2A4A04J01A*02			
E1	2A4A04J01A*01			CHANNEL 3 EXTERNAL DATA BIT 12
E2	2A0B3*V3	6*129	2A0B0*BH	CHL 3 FAN OUT BIT 23 D4 TO OU
E3	2A0B3*M0	6*129	2A0B0*BE	CHL 3 FAN OUT BIT 19 D4 TO OU
F0	2A4A04J02A*02			
F1	2A4A04J02A*01			CHANNEL 3 EXTERNAL DATA BIT 12
F2	2A0B6*M0	6*127	2A0B0*BO	CHL 3 FAN OUT BIT 22 D4 TO OU
F3	2A0B7*M0	6*125	2A0B0*BJ	CHL 3 FAN OUT BIT 21 D4 TO OU
G0	2A0B7*F0	6*125	2A0B0*AF	CHL 3 FAN OUT BIT 17 D4 TO OU
G1	2A0B7*V3	6*125	2A0B0*AE	CHL 3 FAN OUT BIT 13 D4 TO OU
G2	2A4A04J01B*06			
G3	2A4A04J01B*05			CHANNEL 3 EXTERNAL DATA BIT 19
H0	2A0A7*X2	6*133	2A0B0*AS	CHL 3 FAN OUT BIT 12 D4 TO OU
H1	2A0B3*F0	6*129	2A0B0*AG	CHL 3 FAN OUT BIT 15 D4 TO OU
H2	2A4A04J02B*06			
H3	2A4A04J02B*05			CHANNEL 3 EXTERNAL DATA BIT 19
I0	2A4A04J01A*04			
I1	2A4A04J01A*03			CHANNEL 3 EXTERNAL DATA BIT 13
I3	2A0B2*M0	6*131	2A0B0*BW	CHL 3 FAN OUT BIT 20 D4 TO OU
J0	2A4A04J02A*04			
J1	2A4A04J02A*03			CHANNEL 3 EXTERNAL DATA BIT 13
J3	2A0B6*F0	6*127	2A0B0*BZ	CHL 3 FAN OUT BIT 18 D4 TO OU
K0	2A0B6*V3	6*127	2A0B0*AR	CHL 3 FAN OUT BIT 14 D4 TO OU
K2	2A4A04J01B*09			CHANNEL 3 EXTERNAL DATA BIT 21
K3	2A4A04J01B*10			
L0	2A4A04J02A*05			CHANNEL 3 EXTERNAL DATA BIT 14
L1	2A4A04J02A*06			
L2	2A4A04J02B*09			CHANNEL 3 EXTERNAL DATA BIT 21
L3	2A4A04J02B*10			
M0	2A4A04J01A*05			CHANNEL 3 EXTERNAL DATA BIT 14
M1	2A4A04J01A*06			
M2	2A4A04J01B*08			
M3	2A4A04J01B*07			CHANNEL 3 EXTERNAL DATA BIT 20
N0	2A4A04J01A*08			
N1	2A4A04J01A*07			CHANNEL 3 EXTERNAL DATA BIT 15
N2	2A4A04J02B*08			
N3	2A4A04J02B*07			CHANNEL 3 EXTERNAL DATA BIT 20
O0	2A4A04J02A*08			
O1	2A4A04J02A*07			CHANNEL 3 EXTERNAL DATA BIT 15
O2	2A0B5*W3	6*159	2A0B5*RW	NOT(BIT 20) CHL 3 OU TO FAN IN
O3	2A0B5*X2	6*159	2A0B5*RZ	NOT(BIT 18) CHL 3 OU TO FAN IN
P0	2A0B5*S1	6*159	2A0B5*AW	NOT(BIT 12) CHL 3 OU TO FAN IN
P2	2A0B5*W2	6*159	2A0B5*RX	NOT(BIT 21) CHL 3 OU TO FAN IN
P3	2A0B5*X3	6*159	2A0B5*RY	NOT(BIT 19) CHL 3 OU TO FAN IN
Q0	2A0B5*S0	6*159	2A0B5*AV	NOT(BIT 13) CHL 3 OU TO FAN IN
Q1	2A0B5*X1	6*159	2A0B5*AZ	NOT(BIT 14) CHL 3 OU TO FAN IN
Q2	2A4A04J01C*01			CHANNEL 3 EXTERNAL DATA BIT 22
Q3	2A4A04J01C*02			
R0	2A0B2*V3	6*131	2A0B0*AQ	CHL 3 FAN OUT BIT 16 D4 TO OU
R1	2A0B5*R1	6*159	2A0B5*AU	NOT(BIT 15) CHL 3 OU TO FAN IN
R2	2A4A04J02C*01			CHANNEL 3 EXTERNAL DATA BIT 22
R3	2A4A04J02C*02			
S0	2A4A04J01A*10			
S1	2A4A04J01A*09			CHANNEL 3 EXTERNAL DATA BIT 16
S3	2A0B5*V2	6*159	2A0B5*RV	NOT(BIT 22) CHL 3 OU TO FAN IN
T0	2A4A04J02A*10			
T1	2A4A04J02A*09			CHANNEL 3 EXTERNAL DATA BIT 16
T3	2A0B5*V3	6*159	2A0B5*RU	NOT(BIT 23) CHL 3 OU TO FAN IN
U0	2A0A2*T2	6*139		CHL 3 NOT(CLEAR 0 REG UPPER)
U1	2A0A2*S0	6*139		CHL 3 ENABLE OU TRANSMISSION
U2	2A4A04J01C*05			CHL 3 EXTERNAL PARITY BIT 2
U3	2A4A04J01C*06			
V0	2A0B5*X0	6*159	2A0B5*AY	NOT(BIT 17) CHL 3 OU TO FAN IN
V1	2A0B5*W0	6*159	2A0B5*AX	NOT(BIT 16) CHL 3 OU TO FAN IN
V2	2A4A04J02C*05			CHL 3 EXTERNAL PARITY BIT 2
V3	2A4A04J02C*06			
W0	2A4A04J01B*02			
W1	2A4A04J01B*01			CHANNEL 3 EXTERNAL DATA BIT 17
W2	2A4A04J01C*04			
W3	2A4A04J01C*03			CHANNEL 3 EXTERNAL DATA BIT 23
X0	2A4A04J02B*02			
X1	2A4A04J02B*01			CHANNEL 3 EXTERNAL DATA BIT 17
X2	2A4A04J02C*04			
X3	2A4A04J02C*03			CHANNEL 3 EXTERNAL DATA BIT 23



PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A0A7-F0	6-133		CHAN 0 NOT(EN 0 LWR TO FAN-IN)
A3	2A0A9-O3	6-141	2A0A4-BA	NOT(BIT 06) CHL 0 OL TO FAN IN
B0	2A0A9-V0	6-141	2A0A4-AB	NOT(BIT 05) CHL 0 OL TO FAN IN
B2	2A0A9-P3	6-141	2A0A4-BB	NOT(BIT 07) CHL 0 OL TO FAN IN
B3	2A0A9-O2	6-141	2A0A4-BC	NOT(BIT 08) CHL 0 OL TO FAN IN
C0	2A0A9-V1	6-141	2A0A4-AC	NOT(BIT 04) CHL 0 OL TO FAN IN
C2	2A0A9-P2	6-141	2A0A4-BD	NOT(BIT 09) CHL 0 OL TO FAN IN
C3	2A0A9-S3	6-141	2A0A4-BE	NOT(BIT 10) CHL 0 OL TO FAN IN
D0	2A0A9-Q0	6-141	2A0A4-AE	NOT(BIT 01) CHL 0 OL TO FAN IN
D1	2A0A9-P0	6-141	2A0A4-AD	NOT(BIT 00) CHL 0 OL TO FAN IN
D2	2A0A9-T3	6-141	2A0A4-BG	NOT(BIT 11) CHL 0 OL TO FAN IN
D3	2A0B7-O3	6-125		CHAN 0 NOT(REPLY ON CONN/FCN)
E0	2A0A9-R1	6-141	2A0A4-AG	NOT(BIT 03) CHL 0 OL TO FAN IN
E1	2A0A9-Q1	6-141	2A0A4-AF	NOT(BIT 02) CHL 0 OL TO FAN IN
E2	2A0B6-O3	6-127		CHL 1 NOT(REPLY ON CONN/FUNC)
E3	2A0B3-O3	6-129		CHL 2 NOT(REPLY ON CONN/FUNC)
F0	2A0A8-V1	6-145	2A0A4-AJ	NOT(BIT 04) CHL 1 OL TO FAN IN
F1	2A0A8-V0	6-145	2A0A4-AH	NOT(BIT 05) CHL 1 OL TO FAN IN
F2	2B1B1-H3	6- 9		
F3	2B1B1-H2	6- 9		NOT CHAN 0-3 CONN + FCN REPLY FAN-IN
G0	2A0A8-O1	6-145	2A0A4-AL	NOT(BIT 02) CHL 1 OL TO FAN IN
G1	2A0A8-R1	6-145	2A0A4-AK	NOT(BIT 03) CHL 1 OL TO FAN IN
G2	2A0B2-O3	6-131		CHL 3 NOT(REPLY ON CONN/FUNC)
G3	2A0A8-P3	6-145	2A0A4-BH	NOT(BIT 07) CHL 1 OL TO FAN IN
H0	2A0A8-P0	6-145	2A0A4-AN	NOT(BIT 00) CHL 1 OL TO FAN IN
H1	2A0A8-Q0	6-145	2A0A4-AM	NOT(BIT 01) CHL 1 OL TO FAN IN
H2	2A0A6-F0	6-135		CHL 1 NOT(ENABLE OL TO FAN IN)
H3	2A0A8-O3	6-145	2A0A4-BJ	NOT(BIT 06) CHL 1 OL TO FAN IN
I0	2B1B4-I1	6- 29		NOT CHL 0-3 BIT 00 FI TO D4
I1	2B1B4-I0	6- 29		
I2	2A0A8-O2	6-145	2A0A4-BK	NOT(BIT 08) CHL 1 OL TO FAN IN
I3	2A0A8-P2	6-145	2A0A4-BL	NOT(BIT 09) CHL 1 OL TO FAN IN
J0	2B1B3-I0	6- 31		
J1	2B1B3-I1	6- 31		NOT CHAN 0-3 BIT 01 FI TO D4
J2	2A0A8-S3	6-145	2A0A4-BM	NOT(BIT 10) CHL 1 OL TO FAN IN
J3	2A0A8-T3	6-145	2A0A4-BN	NOT(BIT 11) CHL 1 OL TO FAN IN
K0	2B1B2-I0	6- 33		
K1	2B1B2-I1	6- 33		NOT CHAN 0-3 BIT 02 FI TO D4
K2	2B1A3-N1	6- 37		
K3	2B1A3-N0	6- 37		NOT CHAN 0-3 BIT 10 FI TO D4
L0	2B1A3-I0	6- 37		
L1	2B1A3-I1	6- 37		NOT CHAN 0-3 BIT 04 FI TO D4
L2	2B1A2-N1	6- 39		
L3	2B1A2-N0	6- 39		NOT CHAN 0-3 BIT 11 FI TO D4
M0	2B1A2-I1	6- 39		NOT CHAN 0-3 BIT 05 FI TO D4
M1	2B1A2-I0	6- 39		
M2	2B1A4-N0	6- 35		NOT CHAN 0-3 BIT 09 FI TO D4
M3	2B1A4-N1	6- 35		
N0	2B1A4-I0	6- 35		
N1	2B1A4-I1	6- 35		NOT CHAN 0-3 BIT 03 FI TO D4
N2	2B1B2-N1	6- 33		
N3	2B1B2-N0	6- 33		NOT CHAN 0-3 BIT 08 FI TO D4
O0	2A0A1-R1	6-149	2A0A4-AO	NOT(BIT 03) CHL 2 OL TO FAN IN
O1	2A0A1-Q0	6-149	2A0A4-AP	NOT(BIT 01) CHL 2 OL TO FAN IN
O2	2B1B3-N0	6- 31		NOT CHAN 0-3 BIT 07 FI TO D4
O3	2B1B3-N1	6- 31		
P0	2A0A1-P0	6-149	2A0A4-AQ	NOT(BIT 00) CHL 2 OL TO FAN IN
P1	2A0A1-Q1	6-149	2A0A4-AR	NOT(BIT 02) CHL 2 OL TO FAN IN
P2	2B1B4-N0	6- 29		NOT CHAN 0-3 BIT 06 FI TO D4
P3	2B1B4-N1	6- 29		
Q0	2A0A1-V1	6-149	2A0A4-AS	NOT(BIT 04) CHL 2 OL TO FAN IN
Q2	2A0A1-T3	6-149	2A0A4-BQ	NOT(BIT 11) CHL 2 OL TO FAN IN
Q3	2A0A3-F0	6-137		CHL 2 NOT(ENABLE OL TO FAN IN)
R0	2A0A1-V0	6-149	2A0A4-AT	NOT(BIT 05) CHL 2 OL TO FAN IN
R1	2A0A0-R1	6-153	2A0A4-AU	NOT(BIT 03) CHL 3 OL TO FAN IN
R2	2A0A1-O3	6-149	2A0A4-BQ	NOT(BIT 06) CHL 2 OL TO FAN IN
R3	2A0A1-S3	6-149	2A0A4-BP	NOT(BIT 10) CHL 2 OL TO FAN IN
S0	2A0A0-Q0	6-153	2A0A4-AV	NOT(BIT 01) CHL 3 OL TO FAN IN
S1	2A0A0-P0	6-153	2A0A4-AW	NOT(BIT 00) CHL 3 OL TO FAN-IN
S3	2A0A1-P3	6-149	2A0A4-BR	NOT(BIT 07) CHL 2 OL TO FAN IN
T0	2A0B7-B1	6-125		CHAN 0 TEST OPR COMPL/PE
T1	2A0B2-B1	6-131		CHAN 3 TEST OPR COMPL/PE
T3	2A0A1-P2	6-149	2A0A4-BS	NOT(BIT 09) CHL 2 OL TO FAN IN
U0	2A0B3-B1	6-129		CHAN 2 TEST OPR COMPL/PE
U1	2A0B6-B1	6-127		CHAN 1 TEST OPR COMPL/PE
U2	2A0A2-F0	6-139		CHL 3 NOT(ENABLE OL TO FAN IN)
U3	2A0A1-O2	6-149	2A0A4-BT	NOT(BIT 08) CHL 2 OL TO FAN IN
V0	2B1A7-O2	6- 1		TEST OPR COMPL/PE TO CHAN 0-3
V1	2B1A7-O3	6- 1		
V2	2A0A0-S3	6-153	2A0A4-BV	NOT(BIT 10) CHL 3 OL TO FAN IN
V3	2A0A0-T3	6-153	2A0A4-BU	NOT(BIT 11) CHL 3 OL TO FAN IN
W0	2A0A0-V1	6-153	2A0A4-AX	NOT(BIT 04) CHL 3 OL TO FAN IN
W2	2A0A0-P2	6-153	2A0A4-BX	NOT(BIT 09) CHL 3 OL TO FAN IN
W3	2A0A0-O2	6-153	2A0A4-BW	NOT(BIT 08) CHL 3 OL TO FAN IN
X0	2A0A0-V0	6-153	2A0A4-AY	NOT(BIT 05) CHL 3 OL TO FAN IN
X1	2A0A0-Q1	6-153	2A0A4-AZ	NOT(BIT 02) CHL 3 OL TO FAN IN
X2	2A0A0-O3	6-153	2A0A4-BZ	NOT(BIT 06) CHL 3 OL TO FAN IN
X3	2A0A0-P3	6-153	2A0A4-BY	NOT(BIT 07) CHL 3 OL TO FAN IN



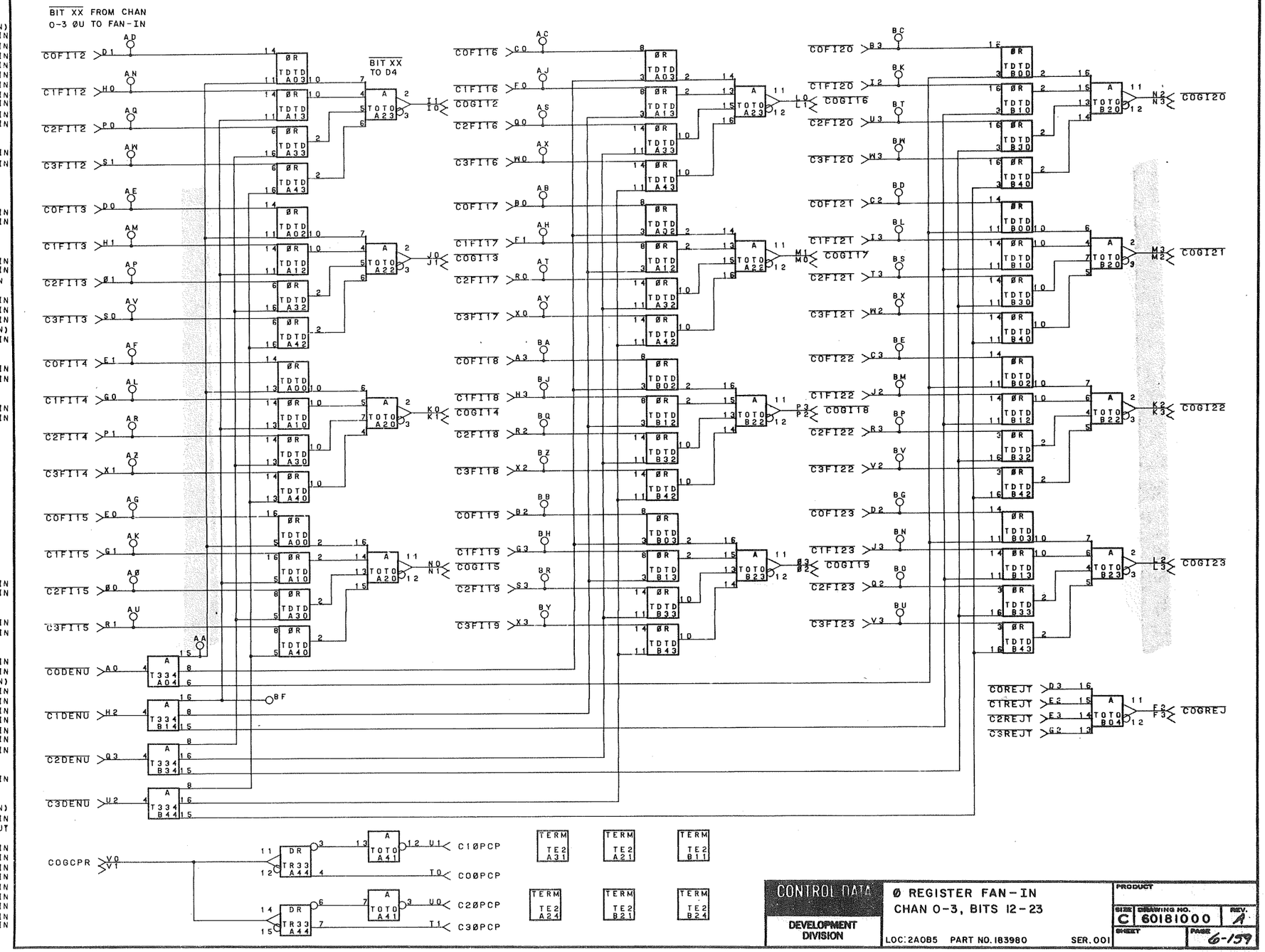
CONTROL DATA
DEVELOPMENT DIVISION

Ø REGISTER FAN-IN, CHAN 0-3, BITS 00-11

LOC:2A0A4 PART NO. 183980 SER : 000

PRODUCT
SIZE C | DRAWING NO. 60181000 | REV. A
SHEET | PAGE 6-157

PIN	ORIGIN/ DEST,	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2A0A7-H0	6-133		CHAN 0 NOT(EN 0 UP, TO FAN-IN)
A3	2A0B9-03	6-143	2A0B5-RA	NOT(BIT 18) CHL 0 OU TO FAN IN
B0	2A0B9-V0	6-143	2A0B5-AB	NOT(BIT 17) CHL 0 OU TO FAN IN
B2	2A0B9-P3	6-143	2A0B5-RB	NOT(BIT 19) CHL 0 OU TO FAN IN
B3	2A0B9-02	6-143	2A0B5-RC	NOT(BIT 20) CHL 0 OU TO FAN IN
C0	2A0B9-V1	6-143	2A0B5-AC	NOT(BIT 16) CHL 0 OU TO FAN IN
C2	2A0B9-P2	6-143	2A0B5-RD	NOT(BIT 21) CHL 0 OU TO FAN IN
C3	2A0B9-S3	6-143	2A0B5-RE	NOT(BIT 22) CHL 0 OU TO FAN IN
D0	2A0B9-Q0	6-143	2A0B5-AE	NOT(BIT 13) CHL 0 OU TO FAN IN
D1	2A0B9-P0	6-143	2A0B5-AD	NOT(BIT 12) CHL 0 OU TO FAN IN
D2	2A0B9-T3	6-143	2A0B5-RG	NOT(BIT 23) CHL 0 OU TO FAN IN
D3	2A0B7-B3	6-125		CHAN 0 - NOT (EXT REJECT ON CONN + FCN)
E0	2A0B9-R1	6-143	2A0B5-AG	NOT(BIT 15) CHL 0 OU TO FAN IN
E1	2A0B9-Q1	6-143	2A0B5-AF	NOT(BIT 14) CHL 0 OU TO FAN IN
E2	2A0B6-B3	6-127		CHAN 1 NOT (EXT REJECT ON CONN + FCN)
E3	2A0B3-B3	6-129		CHAN 2 NOT (EXT REJECT ON CONN + FCN)
F0	2A0B8-V1	6-147	2A0B5-AJ	NOT(BIT 16) CHL 1 OU TO FAN IN
F1	2A0B8-V0	6-147	2A0B5-AH	NOT(BIT 17) CHL 1 OU TO FAN IN
F2	2R1B1-I3	6- 9		
F3	2R1B1-I2	6- 9		NOT CHAN 0-3 CONN + FCN EXT REJECT FAN-IN
G0	2A0B8-Q1	6-147	2A0B5-AL	NOT(BIT 14) CHL 1 OU TO FAN IN
G1	2A0B8-R1	6-147	2A0B5-AK	NOT(BIT 15) CHL 1 OU TO FAN IN
G2	2A0B2-B3	6-131		CHAN 3 NOT(EXT REJECT ON CONN + FCN
G3	2A0B8-P3	6-147	2A0B5-RH	NOT(BIT 19) CHL 1 OU TO FAN IN
H0	2A0B8-P0	6-147	2A0B5-AN	NOT(BIT 12) CHL 1 OU TO FAN IN
H1	2A0B8-Q0	6-147	2A0B5-AM	NOT(BIT 13) CHL 1 OU TO FAN IN
H2	2A0A6-H0	6-135		CHL 1 NOT(ENABLE OU TO FAN IN)
H3	2A0B8-03	6-147	2A0B5-RJ	NOT(BIT 18) CHL 1 OU TO FAN IN
I0	2R1B4-Q1	6- 29		NOT CHAN 0-3 BIT 12 FI TO D4
I1	2R1B4-Q0	6- 29		
I2	2A0B8-02	6-147	2A0B5-RK	NOT(BIT 20) CHL 1 OU TO FAN IN
I3	2A0B8-P2	6-147	2A0B5-RL	NOT(BIT 21) CHL 1 OU TO FAN IN
J0	2R1B3-Q0	6- 31		
J1	2R1B3-Q1	6- 31		NOT CHAN 0-3 BIT 13 FI TO D4
J2	2A0B8-S3	6-147	2A0B5-RM	NOT(BIT 22) CHL 1 OU TO FAN IN
J3	2A0B8-T3	6-147	2A0B5-RN	NOT(BIT 23) CHL 1 OU TO FAN IN
K0	2R1B2-Q0	6- 33		
K1	2R1B2-Q1	6- 33		NOT CHAN 0-3 BIT 14 FI TO D4
K2	2R1A3-V0	6- 37		
K3	2R1A3-V1	6- 37		NOT CHAN 0-3 BIT 22 FI TO D4
L0	2R1A3-Q0	6- 37		
L1	2R1A3-Q1	6- 37		NOT CHAN 0-3 BIT 16 FI TO D4
L2	2R1A2-V0	6- 39		
L3	2R1A2-V1	6- 39		NOT CHAN 0-3 BIT 23 FI TO D4
M0	2R1A2-Q1	6- 39		NOT CHAN 0-3 BIT 17 FI TO D4
M1	2R1A2-Q0	6- 39		
M2	2R1A4-V1	6- 35		NOT CHAN 0-3 BIT 21 FI TO D4
M3	2R1A4-V0	6- 35		
N0	2R1A4-Q0	6- 35		
N1	2R1A4-Q1	6- 35		NOT CHAN 0-3 BIT 15 FI TO D4
N2	2R1B2-V0	6- 33		
N3	2R1B2-V1	6- 33		NOT CHAN 0-3 BIT 20 FI TO D4
O0	2A0B1-R1	6-151	2A0B5-AO	NOT(BIT 15) CHL 2 OU TO FAN IN
O1	2A0B1-Q0	6-151	2A0B5-AP	NOT(BIT 13) CHL 2 OU TO FAN IN
O2	2R1B3-V1	6- 31		NOT CHAN 0-3 BIT 19 FI TO D4
O3	2R1B3-V0	6- 31		
P0	2A0B1-P0	6-151	2A0B5-AQ	NOT(BIT 12) CHL 2 OU TO FAN IN
P1	2A0B1-Q1	6-151	2A0B5-AR	NOT(BIT 14) CHL 2 OU TO FAN IN
P2	2R1B4-V1	6- 29		NOT CHAN 0-3 BIT 18 FI TO D4
P3	2R1B4-V0	6- 29		
Q0	2A0B1-V1	6-151	2A0B5-AS	NOT(BIT 16) CHL 2 OU TO FAN IN
Q2	2A0B1-T3	6-151	2A0B5-RO	NOT(BIT 23) CHL 2 OU TO FAN IN
Q3	2A0A3-H0	6-137		CHL 2 NOT(ENABLE OU TO FAN IN)
R0	2A0B1-V0	6-151	2A0B5-AT	NOT(BIT 17) CHL 2 OU TO FAN IN
R1	2A0B0-R1	6-155	2A0B5-AU	NOT(BIT 15) CHL 3 OU TO FAN IN
R2	2A0B1-Q3	6-151	2A0B5-RQ	NOT(BIT 18) CHL 2 OU TO FAN IN
R3	2A0B1-S3	6-151	2A0B5-RP	NOT(BIT 22) CHL 2 OU TO FAN IN
S0	2A0B0-Q0	6-155	2A0B5-AV	NOT(BIT 13) CHL 3 OU TO FAN IN
S1	2A0B0-P0	6-155	2A0B5-AW	NOT(BIT 12) CHL 3 OU TO FAN IN
S3	2A0B1-P3	6-151	2A0B5-RR	NOT(BIT 19) CHL 2 OU TO FAN IN
T0	2A0B7-P3	6-125		CHL 0 OPERATION COMPLETE
T1	2A0B2-P3	6-131		CHL 3 OPERATION COMPLETE
T3	2A0B1-P2	6-151	2A0B5-RS	NOT(BIT 21) CHL 2 OU TO FAN IN
U0	2A0B3-P3	6-129		CHL 2 OPERATION COMPLETE
U1	2A0B6-P3	6-127		CHL 1 OPERATION COMPLETE
U2	2A0A2-H0	6-139		CHL 3 NOT(ENABLE OU TO FAN IN)
U3	2A0B1-02	6-151	2A0B5-RT	NOT(BIT 20) CHL 2 OU TO FAN IN
V0	2A1B4-D2	6- 57		ADDR COMPARE TO CHL 0-3 FANOUT
V1	2A1B4-D3	6- 57		
V2	2A0B0-S3	6-155	2A0B5-RV	NOT(BIT 22) CHL 3 OU TO FAN IN
V3	2A0B0-T3	6-155	2A0B5-RU	NOT(BIT 23) CHL 3 OU TO FAN IN
W0	2A0B0-V1	6-155	2A0B5-AX	NOT(BIT 16) CHL 3 OU TO FAN IN
W2	2A0B0-P2	6-155	2A0B5-RX	NOT(BIT 21) CHL 8 OU TO FAN IN
W3	2A0B0-02	6-155	2A0B5-RW	NOT(BIT 20) CHL 8 OU TO FAN IN
X0	2A0B0-V0	6-155	2A0B5-AY	NOT(BIT 17) CHL 3 OU TO FAN IN
X1	2A0B0-01	6-155	2A0B5-AZ	NOT(BIT 14) CHL 3 OU TO FAN IN
X2	2A0B0-03	6-155	2A0B5-BZ	NOT(BIT 18) CHL 3 OU TO FAN IN
X3	2A0B0-P3	6-155	2A0B5-RY	NOT(BIT 19) CHL 3 OU TO FAN IN



CONTROL DATA
DEVELOPMENT DIVISION

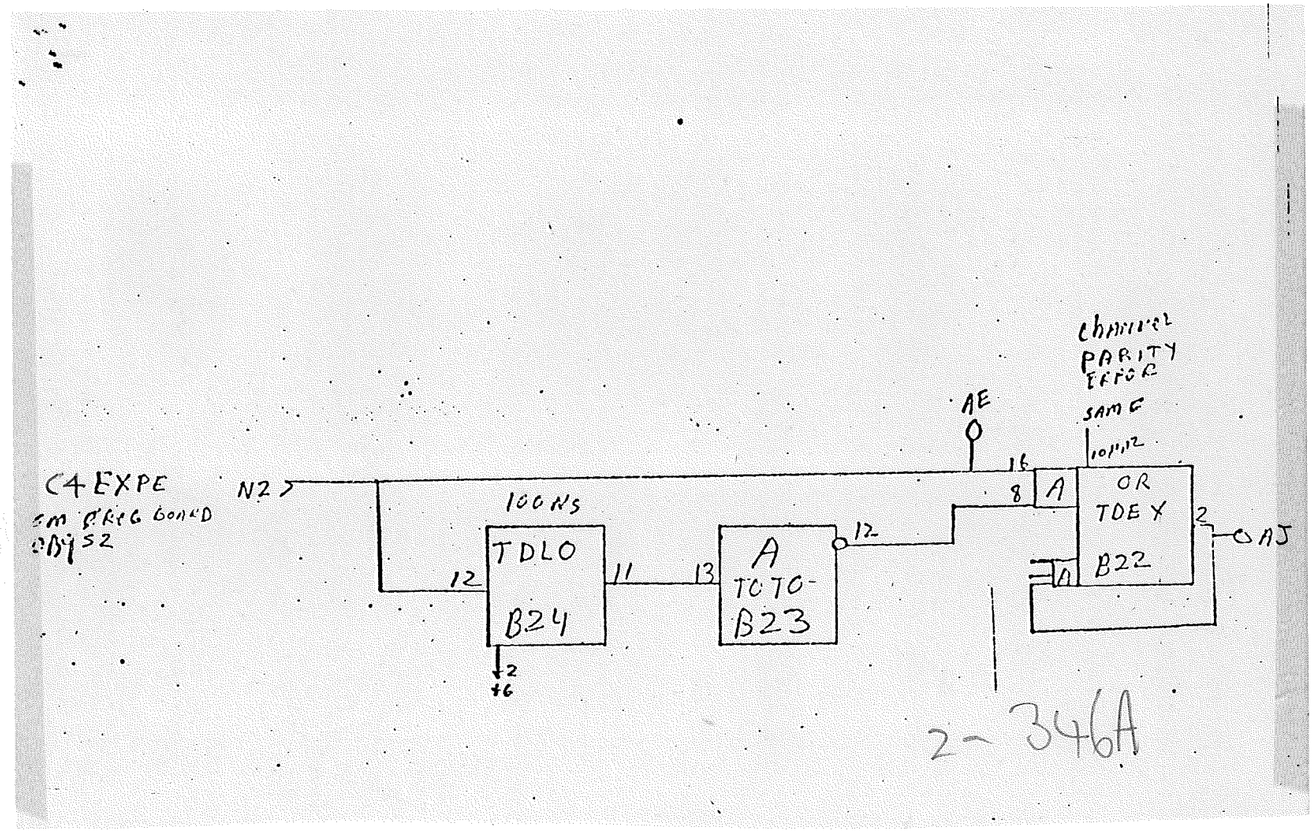
Ø REGISTER FAN-IN
CHAN 0-3, BITS 12-23

LOC: 2A0B5 PART NO. 183980 SER. 001

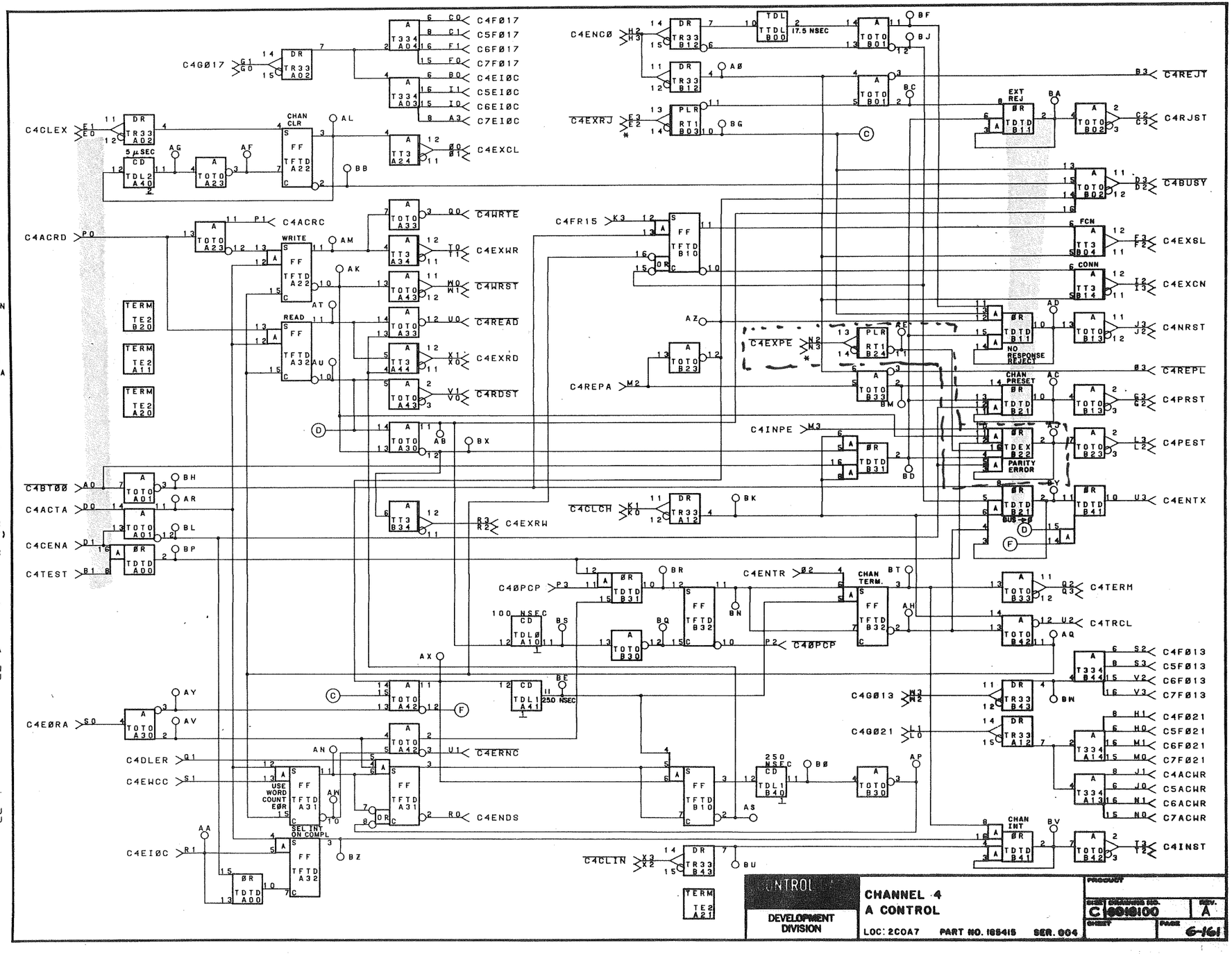
PRODUCT
SIZE C | DRAWING NO. 60181000 | REV. A
SHEET | PAGE 6-159

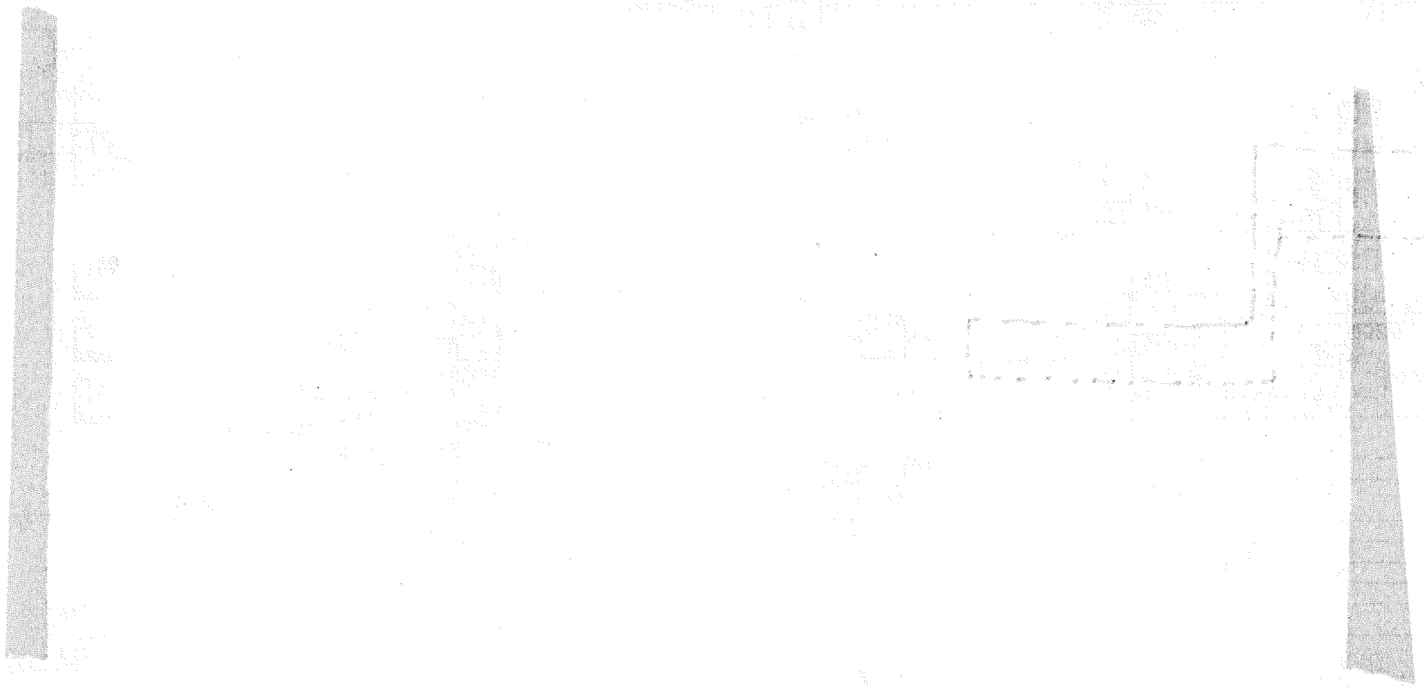
345

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C0B7-T3	6-169		CHL 4 NOT(BUS TO 0) TO CONT A
A3	2C0A2-R1	6-167	2C0A2-AA	CHL 7 EN, INTERRUPT ON COMPL,
B0	2C0A7-R1	6-161	2C0A7-AA	CHL 4 EN, INTERRUPT ON COMPL,
B1	2C0B4-T0	6-193		CHAN 4 TEST OPR COMPL/PE
B3	2C0A5-D3	6-195		CHAN 4 NOT (EXT REJ ON CONN + FCN)
C0	2C0A9-G0	6-179	2C0A9-AF	CHL 4 FAN OUT BIT 17 D4 TO OU
C1	2C0A8-G0	6-183	2C0A8-AF	CHL 5 FAN OUT BIT 17 D4 TO OU
C2	2B0B3-N1	6- 93		CHAN 4 EXT REJ STAT TO FAN-IN
C3	2B0B3-N0	6- 93		
D0	2C0A2-C0	6-167		CHL 4 ACTIVATE CHL CONTROL A
D1	2C0B7-F1	6-169		CHL 4 CHANNEL ENABLE TO CONT A
D2	2B185-Q2	6- 21		NOT CHAN 4 BUSY XLTN TO TEST/STATUS
D3	2B185-Q3	6- 21		
E0	2B0A4-H2	6-103		
E1	2B0A4-H3	6-103		CHL 4 CLEAR CHL AND EXT EQUIP


C4 EXPE
SM REG BOARD
B1S2
N2
100 NS
TDLO
B24
12
11
13
A
TO TO-
B23
12
AE
16
8
A
OR
TOE X
B22
2
AJ
CHANNEL
PARITY
ERROR
SAME
10,11,12
2
TO
2-346A

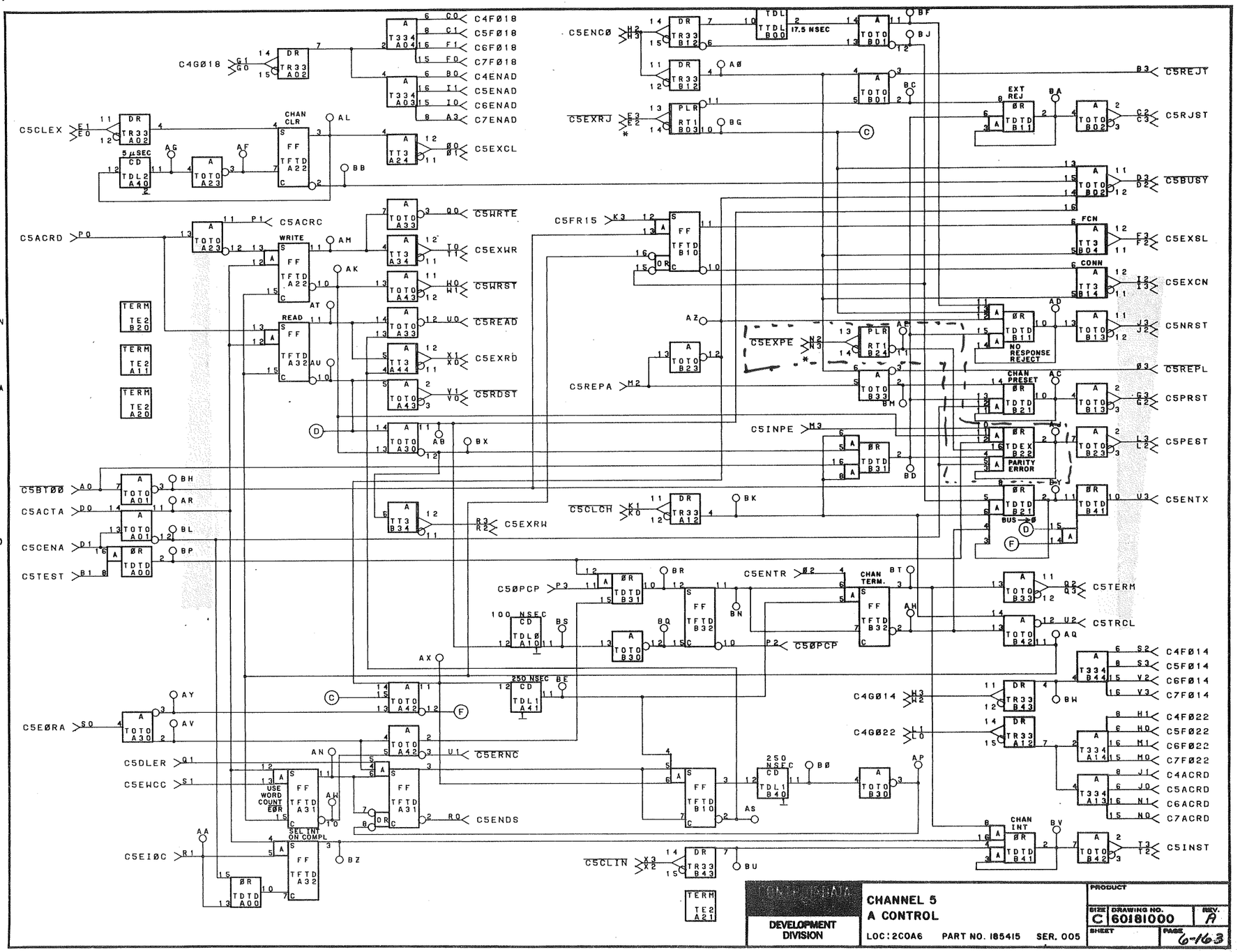
E2	2A4A09J03E-03			CHL 4 EXTERNAL REJECT SIGNAL
	2A4A09J04E-03			
E3	2A4A09J03E-04			
	2A4A09J04E-04			
F0	2C0A0-G0	6-191	2C0A0-AF	CHL 7 FAN OUT BIT 17 D4 TO OU
F1	2C0A1-G0	6-187	2C0A1-AF	CHL 6 FAN OUT BIT 17 D4 TO OU
F2	2A4A09J03D-08			
	2A4A09J04D-08			
F3	2A4A09J03D-07			CHL 4 EXTERNAL SELECT SIGNAL
	2A4A09J04D-07			
G0	2B1A2-P3	6- 39		
G1	2B1A2-P2	6- 39		D4 BIT 17 TO CHL 4-7 FAN OUT
G2	2B0B3-N3	6- 93		
G3	2B0B3-N2	6- 93		CHL 4 PRESET STATUS TO FAN IN
H0	2C0A8-F3	6-183	2C0A8-BJ	CHL 5 FAN OUT BIT 21 D4 TO OU
H1	2C0A9-F3	6-179	2C0A9-BJ	CHL 4 FAN OUT BIT 21 D4 TO OU
H2	2B1B5-D2	6- 21		
H3	2B1B5-D3	6- 21		
I0	2C0A3-R1	6-165	2C0A3-AA	CHL 6 EN, INTERRUPT ON COMPL.
I1	2C0A6-R1	6-163	2C0A6-AA	CHL 5 EN, INTERRUPT ON COMPL.
I2	2A4A09J03D-05			CHL 4 EXTERNAL CONNECT SIGNAL
	2A4A09J04D-05			
I3	2A4A09J03D-06			
	2A4A09J04D-06			
J0	2C0B6-H1	6-171		CHL 5 ACTIVATE WRITE
J1	2C0B7-H1	6-169		CHL 4 ACTIVATE WRITE
J2	2B0B3-D2	6- 93		
J3	2B0B3-D3	6- 93		CHAN 4 NO RESPONSE STATUS TO FAN-IN
K0	2B0A4-I2	6-103		NOT CHL 4 CLR CHL ACTIVITY
K1	2B0A4-I3	6-103		
K3	2C0A3-B0	6-165		CHL 4 FAN OUT D4 FUNCTION XLTN
L0	2B1A4-U2	6- 35		
L1	2B1A4-U3	6- 35		D4 BIT 21 TO CHL 4-7 FAN OUT
L2	2B0B3-D0	6- 93		
L3	2B0B3-D1	6- 93		CHAN 4 PE STATUS - FAN-IN
M0	2C0A0-F3	6-191	2C0A0-BJ	CHL 7 FAN OUT BIT 21 D4 TO OU
M1	2C0A1-F3	6-187	2C0A1-BJ	CHL 6 FAN OUT BIT 21 D4 TO OU
M2	2C0B7-M3	6-169		CHL 4 EXTERNAL REPLY TO CONT A
M3	2C0B7-K0	6-169		CHL 4 INTERNAL PARITY ERROR
N0	2C0B2-H1	6-175		CHL 7 ACTIVATE WRITE
N1	2C0B3-H1	6-173		CHL 6 ACTIVATE WRITE
N2	2A4A09J03E-08			
	2A4A09J04E-08			
N3	2A4A09J03E-07			CHL 4 EXTERNAL PARITY ERROR
	2A4A09J04E-07			
O0	2A4A09J03F-03			CHL 4 CLEAR TO EXTERNAL EQUIP
	2A4A09J04F-03			
O1	2A4A09J03F-04			
	2A4A09J04F-04			
O2	2C0B7-L3	6-169		CHL 4 ENABLE TERMINATION
O3	2C0B4-D3	6-193		CHAN 4 NOT (REPLY ON CONN + FCN)
P0	2C0A6-J1	6-163		CHL 4 ACTIVATE READ
P1	2C0B7-Q3	6-169		CHL 4 ACTIVATE READ TO CONT C
P2	2C0B7-Q2	6-169		CHL 4 NOT(OPERATION COMPL F/F)
P3	2C0A5-T0	6-195		CHL 4 OPERATION COMPLETE
Q0	2C0B7-P3	6-169		CHL 4 NOT(WRITE) TO CONTROL C
Q1	2C0B7-B3	6-169		CHL 4 DELAYED EOR TO CONT A
Q2	2B0A4-E3	6-103		CHL 4 TERMINATE TO COMMON B
Q3	2B0A4-E2	6-103		
R0	2C0B7-G3	6-169		
R1	2C0A7-B0	6-161	2C0A7-AA	CHL 4 EN, INTERRUPT ON COMPL.
R2	2A4A09J03C-08			
	2A4A09J04C-08			
R3	2A4A09J03C-07			CHL 4 EXTERNAL BUSY SIGNAL
	2A4A09J04C-07			
S0	2C0B7-K3	6-169		CHL 4 END OF RECORD TO CONT A
S1	2C0A2-J1	6-167		CHL 4 EN WORD COUNT CONTROL
S2	2C0A9-G1	6-179	2C0A9-AE	CHL 4 FAN OUT BIT 13 D4 TO OU
S3	2C0A8-G1	6-183	2C0A8-AE	CHL 5 FAN OUT BIT 13 D4 TO OU
T0	2A4A09J03D-03			CHL 4 EXTERNAL WRITE SIGNAL
	2A4A09J04D-03			
T1	2A4A09J03D-04			
	2A4A09J04D-04			
T2	2B0B3-O2	6- 93		
T3	2B0B3-O3	6- 93		CHL 4 INTERRUPT TO STATUS FI
U0	2C0B7-F3	6-169		CHL 4 NOT(READ) TO CONTROL C
U1	2C0B7-E1	6-169		CHAN 4 NOT(END OF RECORD) + WORD COUNT CONTROL
U2	2C0B7-K1	6-169		CHL 4 TERMINATE OR CLEAR
U3	2C0B7-U0	6-169		CHL 4 ENABLE O REG XMISSION
V0	2B0B3-E0	6- 93		NOT CHL 4 READ STAT TO FI
V1	2B0B3-E1	6- 93		
V2	2C0A1-G1	6-187	2C0A1-AE	CHL 6 FAN OUT BIT 13 D4 TO OU
V3	2C0A0-G1	6-191	2C0A0-AE	CHL 7 FAN OUT BIT 13 D4 TO OU
W0	2B0B3-O1	6- 93		
W1	2B0B3-O0	6- 93		CHL 4 WRITE STATUS TO FAN IN
W2	2B1B3-P3	6- 31		
W3	2B1B3-P2	6- 31		D4 BIT 13 TO CHL 4-7 FAN OUT
X0	2A4A09J03D-02			
	2A4A09J04D-02			
X1	2A4A09J03D-01			CHL 4 EXTERNAL READ SIGNAL
	2A4A09J04D-01			
X2	2B0A4-L2	6-103		NOT CHL 4 CLR CHL INTERRUPT
X3	2B0A4-L3	6-103		

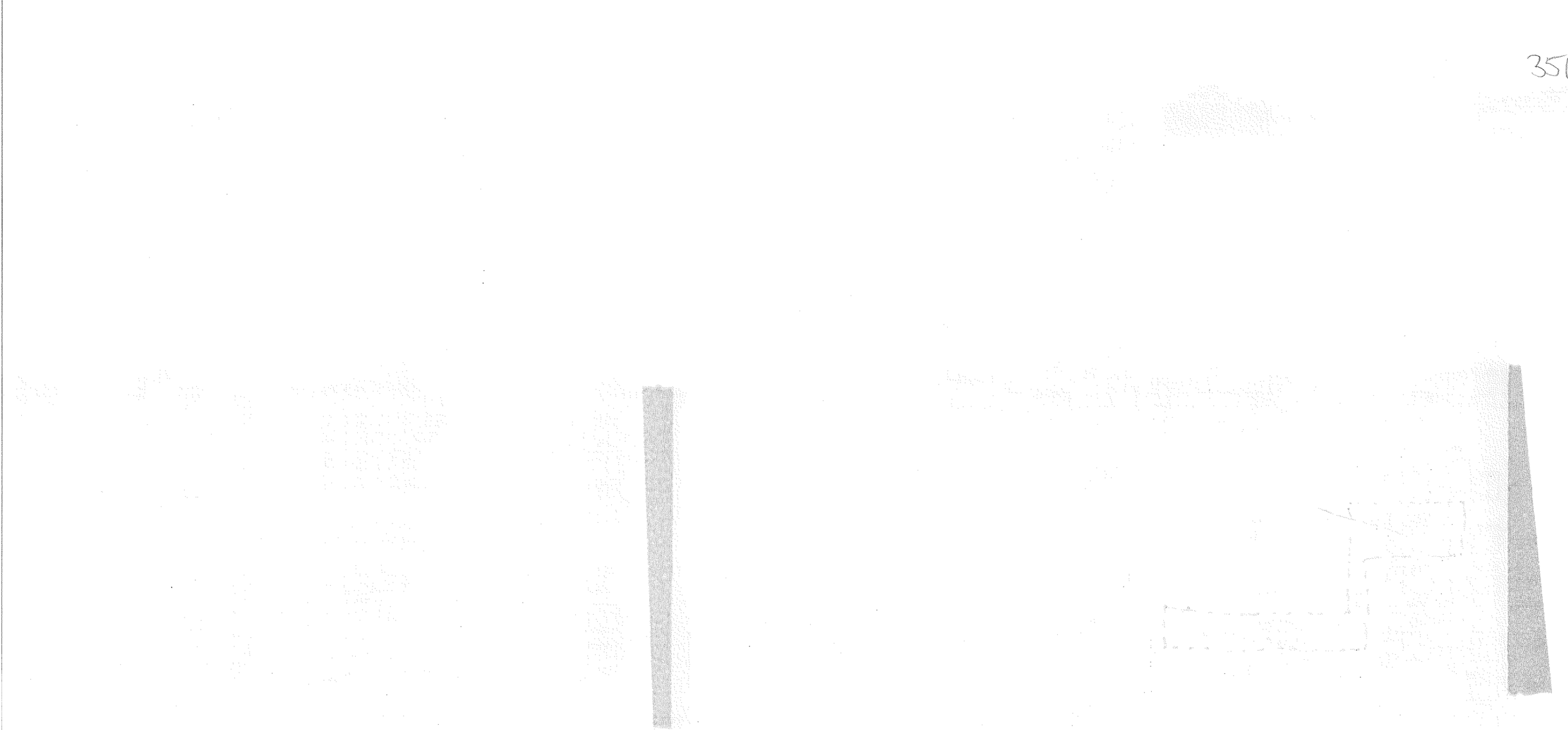




PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C0B6-T3	6-171		CHL 5 NOT(BUS TO 0) TO CONT A
A3	2C0B2-G1	6-175		
B0	2C0B7-G1	6-169		
B1	2C0B4-U1	6-193		CHAN 5 TEST OPR COMPL/PE
B3	2C0A5-E2	6-195		CHAN 5 NOT(EXT REJECT ON CONN + FCN)
C0	2C0A9-J3	6-179	2C0A9-BZ	CHL 4 FAN OUT BIT 18 D4 TO OU
C1	2C0A8-J3	6-183	2C0A8-BZ	CHL 5 FAN OUT BIT 18 D4 TO OU
C2	2B0B2-N1	6- 95		CHAN 5 EXT REJ STAT TO FAN-IN
C3	2B0B2-N0	6- 95		
D0	2C0A2-C1	6-167		CHL 5 ACTIVATE CHL CONTROL A
D1	2C0B6-F1	6-171		CHL 5 CHANNEL ENABLE TO CONT A
D2	2B1B5-F2	6- 21		NOT CHAN 5 BUSY XLTN TO TEST/STATUS
D3	2B1B5-F3	6- 21		
E0	2B0A4-B2	6-103		

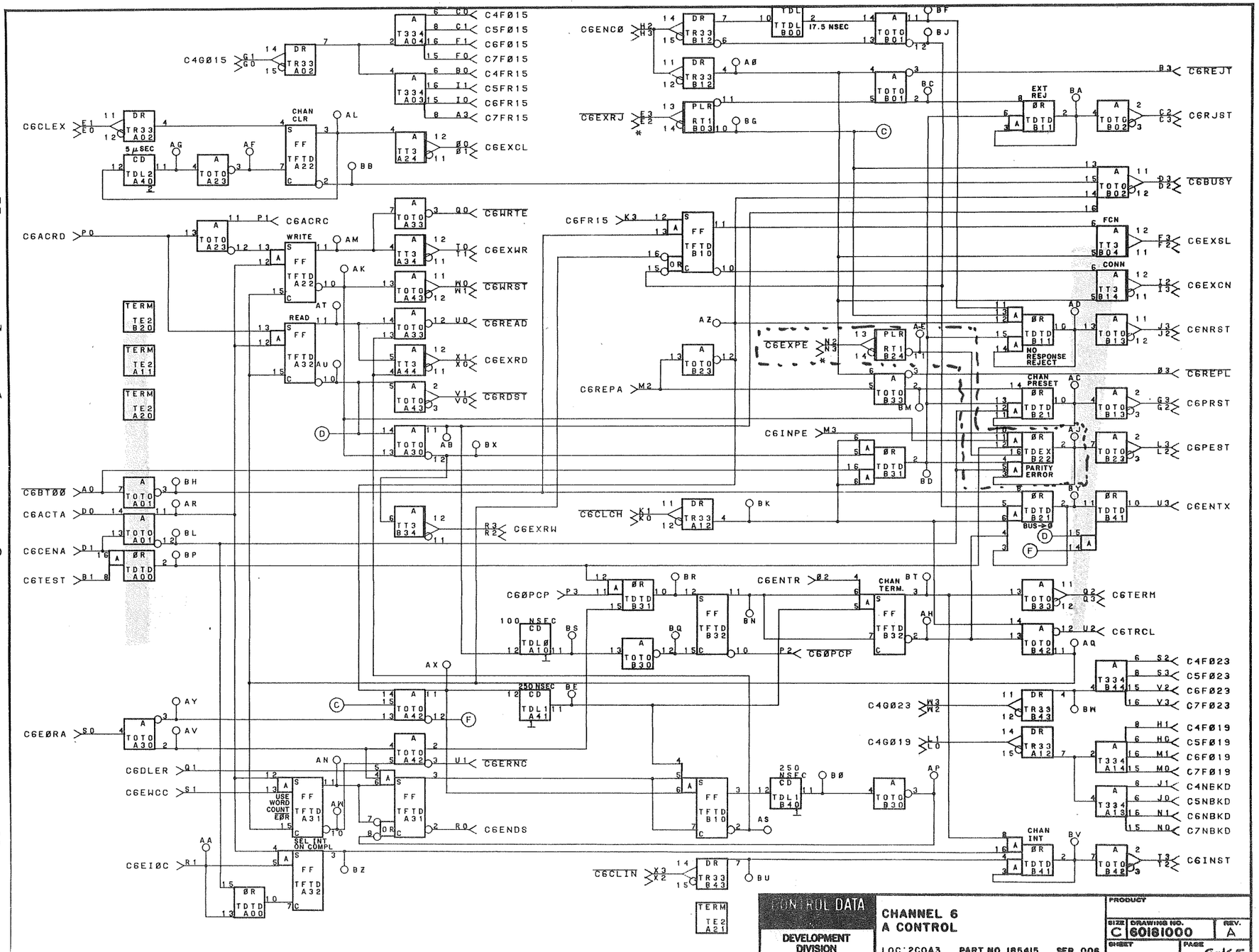
E1	2B0A4-B3	6-103		CHL 5 CLEAR CHL AND EXT EQUIP
E2	2A4A10J03E-03			CHL 5 EXTERNAL REJECT SIGNAL
	2A4A10J04E-03			
E3	2A4A10J03E-04			
	2A4A10J04E-04			
F0	2C0A0-J3	6-191	2C0A0-BZ	CHL 7 FAN OUT BIT 18 D4 TO OU
F1	2C0A1-J3	6-187	2C0A1-BZ	CHL 6 FAN OUT BIT 18 D4 TO OU
F2	2A4A10J03D-08			
	2A4A10J04D-08			
F3	2A4A10J03D-07			CHL 5 EXTERNAL SELECT SIGNAL
	2A4A10J04D-07			
G0	2B1B4-U2	6-29		
G1	2B1B4-U3	6-29		D4 BIT 18 TO CHL 4-7 FAN OUT
G2	2B0B2-N3	6-95		
G3	2B0B2-N2	6-95		CHL 5 PRESET STATUS TO FAN IN
H0	2C0A8-F2	6-183	2C0A8-BQ	CHL 5 FAN OUT BIT 22 D4 TO OU
H1	2C0A9-F2	6-179	2C0A9-BQ	CHL 4 FAN OUT BIT 22 D4 TO OU
H2	2B1B5-E3	6-21		
H3	2B1B5-E2	6-21		
I0	2C0B3-G1	6-173		
I1	2C0B6-G1	6-171		
I2	2A4A10J03D-05			CHL 5 EXTERNAL CONNECT SIGNAL
	2A4A10J04D-05			
I3	2A4A10J03D-06			
	2A4A10J04D-06			
J0	2C0A6-P0	6-163		CHL 5 ACTIVATE READ
J1	2C0A7-P0	6-161		CHL 4 ACTIVATE READ
J2	2B0B2-D2	6-95		
J3	2B0B2-D3	6-95		CHAN 5 NO RESPONSE STATUS TO FAN-IN
K0	2B0A4-V2	6-103		NOT CHL 5 CLR CHL ACTIVITY
K1	2B0A4-V3	6-103		
K3	2C0A3-I1	6-165		CHL 5 FAN OUT D4 FUNCTION XLTN
L0	2B1A3-U2	6-37		
L1	2B1A3-U3	6-37		D4 BIT 22 TO CHL 4-7 FAN OUT
L2	2B0B2-D0	6-95		
L3	2B0B2-D1	6-95		CHAN 5 PE STATUS - FAN-IN
M0	2C0A0-F2	6-191	2C0A0-BO	CHL 7 FAN OUT BIT 22 D4 TO OU
M1	2C0A1-F2	6-187	2C0A1-BO	CHL 6 FAN OUT BIT 22 D4 TO OU
M2	2C0B6-H3	6-171		CHL 5 EXTERNAL REPLY TO CONT A
M3	2C0B6-K0	6-171		CHL 5 INTERNAL PARITY ERROR
N0	2C0A2-P0	6-167		CHL 7 ACTIVATE READ
N1	2C0A3-P0	6-165		CHL 6 ACTIVATE READ
N2	2A4A10J03E-08			
	2A4A10J04E-08			
N3	2A4A10J03E-07			CHL 5 EXTERNAL PARITY ERROR
	2A4A10J04E-07			
O0	2A4A10J03F-03			CHL 5 CLEAR TO EXTERNAL EQUIP
	2A4A10J04F-03			
O1	2A4A10J03F-04			
	2A4A10J04F-04			
O2	2C0B6-L3	6-171		CHL 5 ENABLE TERMINATION
O3	2C0B4-E2	6-193		CHL 5 NOT(REPLY ON CONN/FUNC)
P0	2C0A6-J0	6-163		CHL 5 ACTIVATE READ
P1	2C0B6-Q3	6-171		CHL 5 ACTIVATE READ TO CONT C
P2	2C0B6-Q2	6-171		CHL 5 NOT(OPERATION COMPL F/F)
P3	2C0A5-U1	6-195		CHL 5 OPERATION COMPLETE
Q0	2C0B6-P3	6-171		CHL 5 NOT(WRITE) TO CONTROL C
Q1	2C0B6-B3	6-171		CHL 5 DELAYED EOR TO CONT A
Q2	2B0A4-Q2	6-103		CHL 5 TERMINATE TO COMMON B
Q3	2B0A4-Q3	6-103		
R0	2C0B6-G3	6-171		
R1	2C0A7-I1	6-161	2C0A6-AA	CHL 5 EN. INTERRUPT ON COMPL.
R2	2A4A10J03C-08			
	2A4A10J04C-08			
R3	2A4A10J03C-07			CHL 5 EXTERNAL BUSY SIGNAL
	2A4A10J04C-07			
S0	2C0B6-K3	6-171		CHL 5 END OF RECORD TO CONT A
S1	2C0A2-J0	6-167		CHL 5 EN WORD COUNT CONTROL
S2	2C0A9-K0	6-179	2C0A9-AR	CHL 4 FAN OUT BIT 14 D4 TO OU
S3	2C0A8-K0	6-183	2C0A8-AR	CHL 5 FAN OUT BIT 14 D4 TO OU
T0	2A4A10J03D-03			CHL 5 EXTERNAL WRITE SIGNAL
	2A4A10J04D-03			
T1	2A4A10J03D-04			
	2A4A10J04D-04			
T2	2B0B2-02	6-95		
T3	2B0B2-03	6-95		CHAN 5 INT TO STATUS FAN-IN
U0	2C0B6-F3	6-171		CHL 5 NOT(READ) TO CONTROL C
U1	2C0B6-E1	6-171		CHAN 5 NOT(END OF RECORD) + WORD COUNT CONTROL
U2	2C0B6-K1	6-171		CHL 5 TERMINATE OR CLEAR
U3	2C0B6-U0	6-171		CHL 5 ENABLE O REG XMISSION
V0	2B0B2-E0	6-95		NOT CHL 5 READ STAT TO FI
V1	2B0B2-E1	6-95		
V2	2C0A1-K0	6-167	2C0A1-AR	CHL 6 FAN OUT BIT 14 D4 TO OU
V3	2C0A0-K0	6-191	2C0A0-AR	CHL 7 FAN OUT BIT 14 D4 TO OU
W0	2B0B2-01	6-95		NOT CHL 5 WRITE STAT TO FI
W1	2B0B2-00	6-95		
W2	2B1B2-P3	6-33		
W3	2B1B2-P2	6-33		D4 BIT 14 TO CHL 4-7 FAN OUT
X0	2A4A10J03D-02			
	2A4A10J04D-02			
X1	2A4A10J03D-01			CHL 5 EXTERNAL READ SIGNAL
	2A4A10J04D-01			
X2	2B0A4-U2	6-103		NOT CHL 5 CLR CHL INTERRUPT
X3	2B0A4-U3	6-103		





PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C083-T3	6-173		CHL 6 NOT(BUS TO 0) TO CONT A
A3	2C0A2-K3	6-167		CHL 7 FAN OUT D4 FUNCTION XLTN
B0	2C0A7-K3	6-161		CHL 4 FAN OUT D4 FUNCTION XLTN
B1	2C084-U0	6-193		CHAN 6 TEST OPR COMPL/PE
B3	2C0A9-E3	6-195		CHAN 6 NOT(EXT REJ ON CONN OR FCN)
C0	2C0A9-H1	6-179	2C0A9-AG	CHL 4 FAN OUT BIT 15 D4 TO OU
C1	2C0A8-H1	6-183	2C0A8-AG	CHL 5 FAN OUT BIT 15 D4 TO OU
C2	28081-N1	6- 97		CHAN 6 EXT REJ STAT TO FAN-IN
C3	28081-N0	6- 97		
D0	2C0A2-F1	6-167		CHL 6 ACTIVATE CHL CONTROL A
D1	2C083-F1	6-173		CHL 6 CHANNEL ENABLE TO CONT A
D2	28189-H3	6- 21		NOT CHAN 6 BUSY XLTN TO TEST/STATUS
D3	28185-H2	6- 21		
E0	28084-H2	6-105		

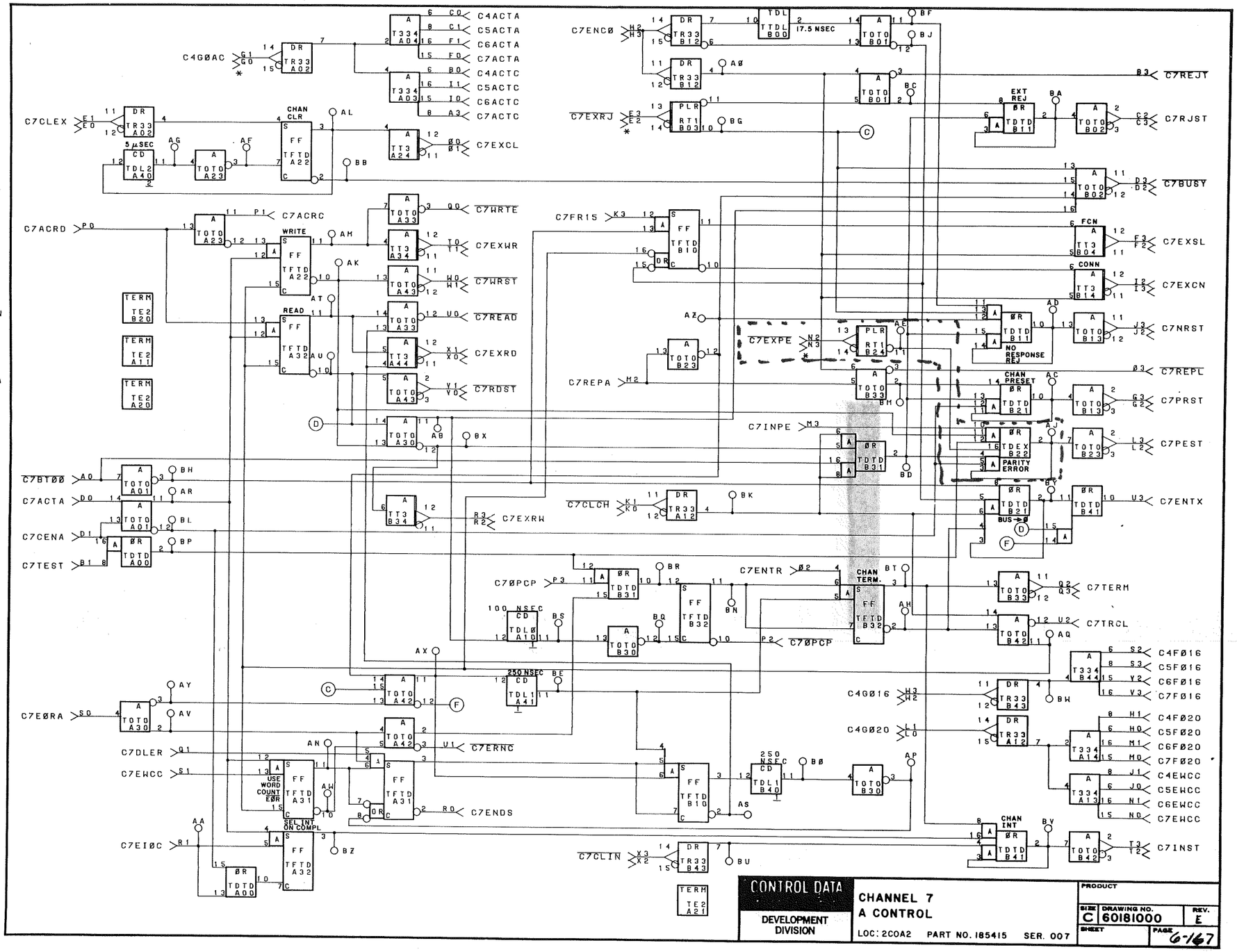
E1	2B0B4=H3	6=105		CHL 6 CLEAR CHL AND EXT EQUIP
E2	2A4A11J03E=03			CHL 6 EXTERNAL REJECT SIGNAL
	2A4A11J04E=03			
E3	2A4A11J03E=04			
	2A4A11J04E=04			
F0	2C0A0=H1	6=191	2C0A0=AG	CHL 7 FAN OUT BIT 15 D4 TO OU
F1	2C0A1=H1	6=187	2C0A1=AG	CHL 6 FAN OUT BIT 15 D4 TO OU
F2	2A4A11J03D=08			
	2A4A11J04D=08			
F3	2A4A11J03D=07			CHL 6 EXTERNAL SELECT SIGNAL
	2A4A11J04D=07			
G0	2B1A4=P3	6= 35		
G1	2B1A4=P2	6= 35		D4 BIT 15 TO CHL 4=7 FAN OUT
G2	2B0B1=N3	6= 97		
G3	2B0B1=N2	6= 97		CHL 6 PRESET STATUS TO FAN IN
H0	2C0A8=E3	6=183	2C0A8=RE	CHL 5 FAN OUT BIT 19 D4 TO OU
H1	2C0A9=E3	6=179	2C0A9=RE	CHL 4 FAN OUT BIT 19 D4 TO OU
H2	2B1B5=J2	6= 21		
H3	2B1B5=J3	6= 21		
I0	2C0A3=K3	6=165		CHL 6 FAN OUT D4 FUNCTION XLTN
I1	2C0A6=K3	6=163		CHL 5 FAN OUT D4 FUNCTION XLTN
I2	2A4A11J03D=05			CHL 6 EXTERNAL CONNECT SIGNAL
	2A4A11J04D=05			
I3	2A4A11J03D=06			
	2A4A11J04D=06			
J0	2C0B6=G0	6=171		CHL 5 FORWARD ASSY/DISASSY
J1	2C0B7=G0	6=169		CHL 4 FORWARD ASSY/DISASSY
J2	2B0B1=D2	6= 97		
J3	2B0B1=D3	6= 97		CHAN 6 NO RESPONSE STATUS TO FAN=IN
K0	2B0B4=I2	6=105		NOT CHL 6 CLR CHL ACTIVITY
K1	2B0B4=I3	6=105		
K2	2C0A3=I0	6=165		CHL 6 FAN OUT D4 FUNCTION XLTN
L0	2B1B3=U2	6= 31		
L1	2B1B3=U3	6= 31		D4 BIT 19 TO CHL 4=7 FAN OUT
L2	2B0B1=D0	6= 97		
L3	2B0B1=D1	6= 97		CHAN 6 PE STATUS = FAN=IN
M0	2C0A6=E3	6=191	2C0A0=RE	CHL 7 FAN OUT BIT 19 D4 TO OU
M1	2C0A1=E3	6=187	2C0A1=RE	CHL 6 FAN OUT BIT 19 D4 TO OU
M2	2C0B3=H3	6=173		CHL 6 EXTERNAL REPLY TO CONT A
M3	2C0B3=K0	6=173		CHL 6 INTERNAL PARITY ERROR
N0	2C0B2=G0	6=175		CHL 7 FORWARD ASSY/DISASSY
N1	2C0B3=G0	6=173		CHL 6 FORWARD ASSY/DISASSY
N2	2A4A11J03E=08			
	2A4A11J04E=08			
N3	2A4A11J03E=07			CHL 6 EXTERNAL PARITY ERROR
	2A4A11J04E=07			
O0	2A4A11J03F=03			CHL 6 CLEAR TO EXTERNAL EQUIP
	2A4A11J04F=03			
O1	2A4A11J03F=04			
	2A4A11J04F=04			
O2	2C0B3=L3	6=173		CHL 6 ENABLE TERMINATION
O3	2C0B4=E3	6=193		CHL 6 NOT(REPLY ON CONN/FUNC)
P0	2C0A6=N1	6=163		CHL 6 ACTIVATE READ
P1	2C0B3=03	6=173		CHL 6 ACTIVATE READ TO CONT C
P2	2C0B3=02	6=173		CHL 6 NOT(OPERATION COMPL F/F)
P3	2C0A5=U0	6=195		CHL 6 OPERATION COMPLETE
Q0	2C0B3=P3	6=173		CHL 6 NOT(WRITE) TO CONTROL C
Q1	2C0B3=B3	6=173		CHL 6 DELAYED EOR TO CONT A
Q2	2B0B4=E3	6=105		CHL 6 TERMINATE TO COMMON B
Q3	2B0B4=E2	6=105		
R0	2C0B3=G3	6=173		
R1	2C0A7=I0	6=161	2C0A8=AA	CHL 6 EN, INTERRUPT ON COMPL.
R2	2A4A11J03C=08			
	2A4A11J04C=08			
R3	2A4A11J03C=07			CHL 6 EXTERNAL BUSY SIGNAL
	2A4A11J04C=07			
S0	2C0B3=K3	6=173		CHL 6 END OF RECORD TO CONT A
S1	2C0A2=N1	6=167		CHL 6 EN WORD COUNT CONTROL
S2	2C0A9=E2	6=179	2C0A9=RH	CHL 4 FAN OUT BIT 23 D4 TO OU
S3	2C0A8=E2	6=183	2C0A8=RH	CHL 5 FAN OUT BIT 23 D4 TO OU
T0	2A4A11J03D=03			CHL 6 EXTERNAL WRITE SIGNAL
	2A4A11J04D=03			
T1	2A4A11J03D=04			
	2A4A11J04D=04			
T2	2B0B1=02	6= 97		
T3	2B0B1=03	6= 97		CHAN 6 INT TO STATUS FAN=IN
U0	2C0B3=F3	6=173		CHL 6 NOT(READ) TO CONTROL C
U1	2C0B3=E1	6=173		CHAN 6 NOT(END OF RECORD) = WORD COUNT CONTROL
U2	2C0B3=K1	6=173		CHL 6 TERMINATE OR CLEAR
U3	2C0B3=U0	6=173		CHL 6 ENABLE O RFG XMISSION
V0	2B0B1=E0	6= 97		NOT CHL 6 READ STAT TO FI
V1	2B0B1=E1	6= 97		
V2	2C0A1=E2	6=187	2C0A1=RH	CHL 6 FAN OUT BIT 23 D4 TO OU
V3	2C0A0=E2	6=191	2C0A0=RH	CHL 7 FAN OUT BIT 23 D4 TO OU
W0	2B0B1=01	6= 97		NOT CHL 6 WRITE STAT TO FI
W1	2B0B1=00	6= 97		
W2	2B1A2=U2	6= 39		
W3	2B1A2=U3	6= 39		D4 BIT 23 TO CHAN 4=7 FANOUT
X0	2A4A11J03D=02			
	2A4A11J04D=02			
X1	2A4A11J03D=01			CHL 6 EXTERNAL READ SIGNAL
	2A4A11J04D=01			
X2	2B0B4=L2	6=105		NOT CHL 6 CLR CHL INTERRUPT
X3	2B0B4=L3	6=105		



351

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C0B2=Y3	6=175		CHL 7 NOT(BUS TO 0) TO CONT A
A3	2C0B2=N1	6=175		CHL 7 ACTIVATE CHL CONTROL C
B0	2C0B7=N1	6=169		CHL 4 ACTIVATE CHL CONTROL C
B1	2C0B4=T1	6=193		CHAN 7 TEST OPR COMPL/PE
B3	2C0A5=Q2	6=195		CHAN 7 NOT (EXT REJECT ON CONN * FCN)
C0	2C0A7=D0	6=161		CHL 4 ACTIVATE CHL CONTROL A
C1	2C0A6=D0	6=163		CHL 5 ACTIVATE CHL CONTROL A
C2	28080=N1	6= 99		CHAN 7 EXT REJ STAT TO FAN=IN
C3	28080=N0	6= 99		
D0	2C0A2=F0	6=167		CHL 7 ACTIVATE CHL CONTROL A
D1	2C0B2=F1	6=175		CHL 7 CHANNEL ENABLE TO CONT A
D2	28185=L2	6= 21		NOT CHL 7 BUSY XLTN TO TEST/STATUS
D3	28185=L3	6= 21		
E0	28084=B2	6=105		

E1	2B0B4-R3	6-105		CHL 7 CLEAR CHL AND EXT EQUIP
E2	2A4A12J03E-03			CHL 7 EXTERNAL REJECT SIGNAL
	2A4A12J04E-03			
E3	2A4A12J03E-04			
	2A4A12J04E-04			
F0	2C0A2-D0	6-167		CHL 7 ACTIVATE CHL CONTROL A
F1	2C0A3-D0	6-165		CHL 6 ACTIVATE CHL CONTROL A
F2	2A4A12J03D-08			
	2A4A12J04D-08			
F3	2A4A12J03D-07			CHL 7 EXTERNAL SELECT SIGNAL
	2A4A12J04D-07			
G0	2B1A6-M0	6- 13		
G1	2B1A6-M1	6- 13		ACT. I/O TO CHAN 4-7 FANOUT
G2	2B0B0-N3	6- 99		
G3	2B0B0-N2	6- 99		CHL 7 PRESET STATUS TO FAN IN
H0	2C0A8-I3	6-183	2C0A8-BW	CHL 5 FAN OUT BIT 20 D4 TO OU
H1	2C0A9-I3	6-179	2C0A9-BW	CHL 4 FAN OUT BIT 20 D4 TO OU
H2	2B1B5-K3	6- 21		
H3	2B1B5-K2	6- 21		
I0	2C0B3-N1	6-173		CHL 6 ACTIVATE CHL CONTROL C
I1	2C0B6-N1	6-171		CHL 5 ACTIVATE CHL CONTROL C
I2	2A4A12J03D-05			CHL 7 EXTERNAL CONNECT SIGNAL
	2A4A12J04D-05			
I3	2A4A12J03D-06			
	2A4A12J04D-06			
J0	2C0A6-S1	6-163		CHL 5 EN WORD COUNT CONTROL
J1	2C0A7-S1	6-161		CHL 4 EN WORD COUNT CONTROL
J2	2B0B0-D2	6- 99		
J3	2B0B0-D3	6- 99		CHAN 7 NO RESPONSE STATUS TO FAN-IN
K0	2B0B4-V2	6-105		NOT CHL 7 CLR CHL ACTIVITY
K1	2B0B4-V3	6-105		
K2	2C0A3-A3	6-165		CHL 7 FAN OUT D4 FUNCTION XLTN
L0	2B1B2-U2	6- 33		
L1	2B1B2-U3	6- 33		D4 BIT 20 TO CHL 4-7 FAN OUT
L2	2B0B0-D0	6- 99		
L3	2B0B0-D1	6- 99		CHAN 7 PE STATUS - FAN-IN
M0	2C0A0-I3	6-191	2C0A0-BW	CHL 7 FAN OUT BIT 20 D4 TO OU
M1	2C0A1-I3	6-187	2C0A1-BW	CHL 6 FAN OUT BIT 20 D4 TO OU
M2	2C0B2-H3	6-175		CHL 7 EXTERNAL REPLY TO CONT A
M3	2C0B2-K0	6-175		CHL 7 INTERNAL PARITY ERROR
N0	2C0A2-S1	6-167		CHL 7 EN WORD COUNT CONTROL
N1	2C0A3-S1	6-165		CHL 6 EN WORD COUNT CONTROL
N2	2A4A12J03E-08			
	2A4A12J04E-08			
N3	2A4A12J03E-07			CHL 7 EXTERNAL PARITY ERROR
	2A4A12J04E-07			
U0	2A4A12J03F-03			CHL 7 CLEAR TO EXTERNAL EQUIP
	2A4A12J04F-03			
U1	2A4A12J03F-04			
	2A4A12J04F-04			
U2	2C0B2-L3	6-175		CHL 7 ENABLE TERMINATION
U3	2C0B4-G2	6-193		CHL 7 NOT(REPLY ON CONN/FUNC)
P0	2C0A6-N0	6-163		CHL 7 ACTIVATE READ
P1	2C0B2-Q3	6-175		CHL 7 ACTIVATE READ TO CONT C
P2	2C0B2-Q2	6-175		CHL 7 NOT(OPERATION COMPL F/F)
P3	2C0A5-T1	6-195		CHL 7 OPERATION COMPLETE
Q0	2C0B2-P3	6-175		CHL 7 NOT(WRITE) TO CONTROL C
Q1	2C0B2-B3	6-175		CHL 7 DELAYED EOR TO CONT A
Q2	2B0B4-Q2	6-105		CHL 7 TERMINATE TO COMMON B
Q3	2B0B4-Q3	6-105		
R0	2C0B2-G3	6-175		
R1	2C0A7-A3	6-161	2C0A2-AA	CHL 7 EN. INTERRUPT ON COMPL.
R2	2A4A12J03C-08			
	2A4A12J04C-08			
R3	2A4A12J03C-07			CHL 7 EXTERNAL BUSY SIGNAL
	2A4A12J04C-07			
S0	2C0B2-K3	6-175		CHL 7 END OF RECORD TO CONT A
S1	2C0A2-N0	6-167		CHL 7 EN WORD COUNT CONTROL
S2	2C0A9-R0	6-179	2C0A9-AQ	CHL 4 FAN OUT BIT 16 D4 TO OU
S3	2C0A8-R0	6-183	2C0A8-AQ	CHL 5 FAN OUT BIT 16 D4 TO OU
T0	2A4A12J03D-03			CHL 7 EXTERNAL WRITE SIGNAL
	2A4A12J04D-03			
T1	2A4A12J03D-04			
	2A4A12J04D-04			
T2	2B0B0-D2	6- 99		
T3	2B0B0-D3	6- 99		CHAN 7 INT TO STATUS FAN-IN
U0	2C0B2-F3	6-175		CHL 7 NOT(READ) TO CONTROL C
U1	2C0B2-E1	6-175		CHAN 7 NOT(END OF RECORD) + WORD COUNT CONTROL
U2	2C0B2-K1	6-175		CHL 7 TERMINATE OR CLEAR
U3	2C0B2-U0	6-175		CHL 7 ENABLE O REG XMISSION
V0	2B0B0-E0	6- 99		NOT CHL 7 READ STAT TO FI
V1	2B0B0-E1	6- 99		
V2	2C0A1-R0	6-187	2C0A1-AQ	CHL 6 FAN OUT BIT 16 D4 TO OU
V3	2C0A0-R0	6-191	2C0A0-AQ	CHL 7 FAN OUT BIT 16 D4 TO OU
W0	2B0B6-01	6- 99		
W1	2B0B0-D0	6- 99		NOT CHL 7 WRITE STAT TO FI
W2	2B1A3-P3	6- 37		
W3	2B1A3-P2	6- 37		D4 BIT 16 TO CHL 4-7 FAN OUT
X0	2A4A12J03D-02			
	2A4A12J04D-02			
X1	2A4A12J03D-01			CHL 7 EXTERNAL READ SIGNAL
	2A4A12J04D-01			
X2	2B0B4-U2	6-105		NOT CHL 7 CLR CHL INTERRUPT
X3	2B0B4-U3	6-105		



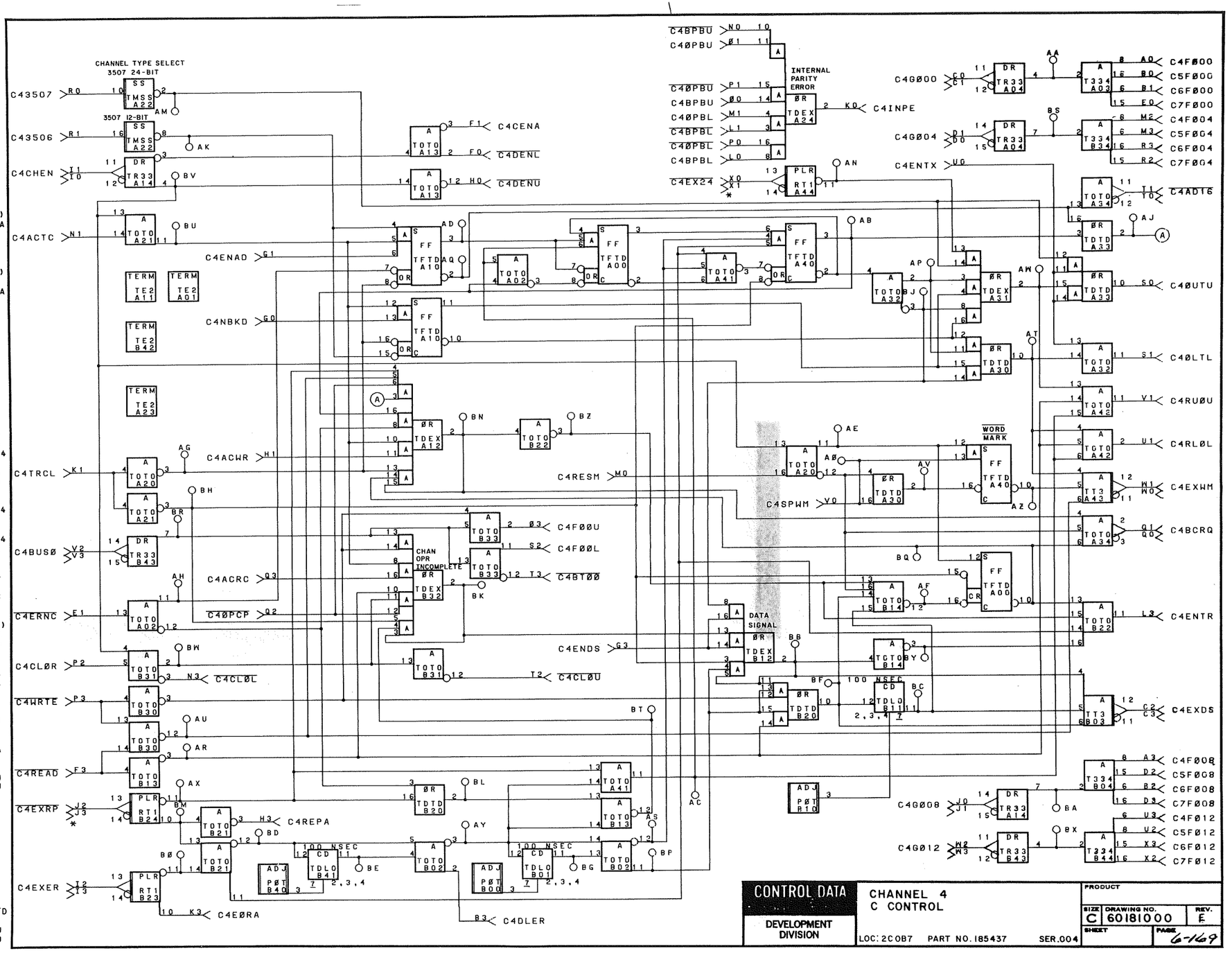
CONTROL DATA
DEVELOPMENT DIVISION

CHANNEL 7
A CONTROL
LOC: 2C0A2 PART NO. 185415 SER. 007

PRODUCT
SIZE C | DRAWING NO. 60181000 | REV. E
SHEET | PAGE 6-167

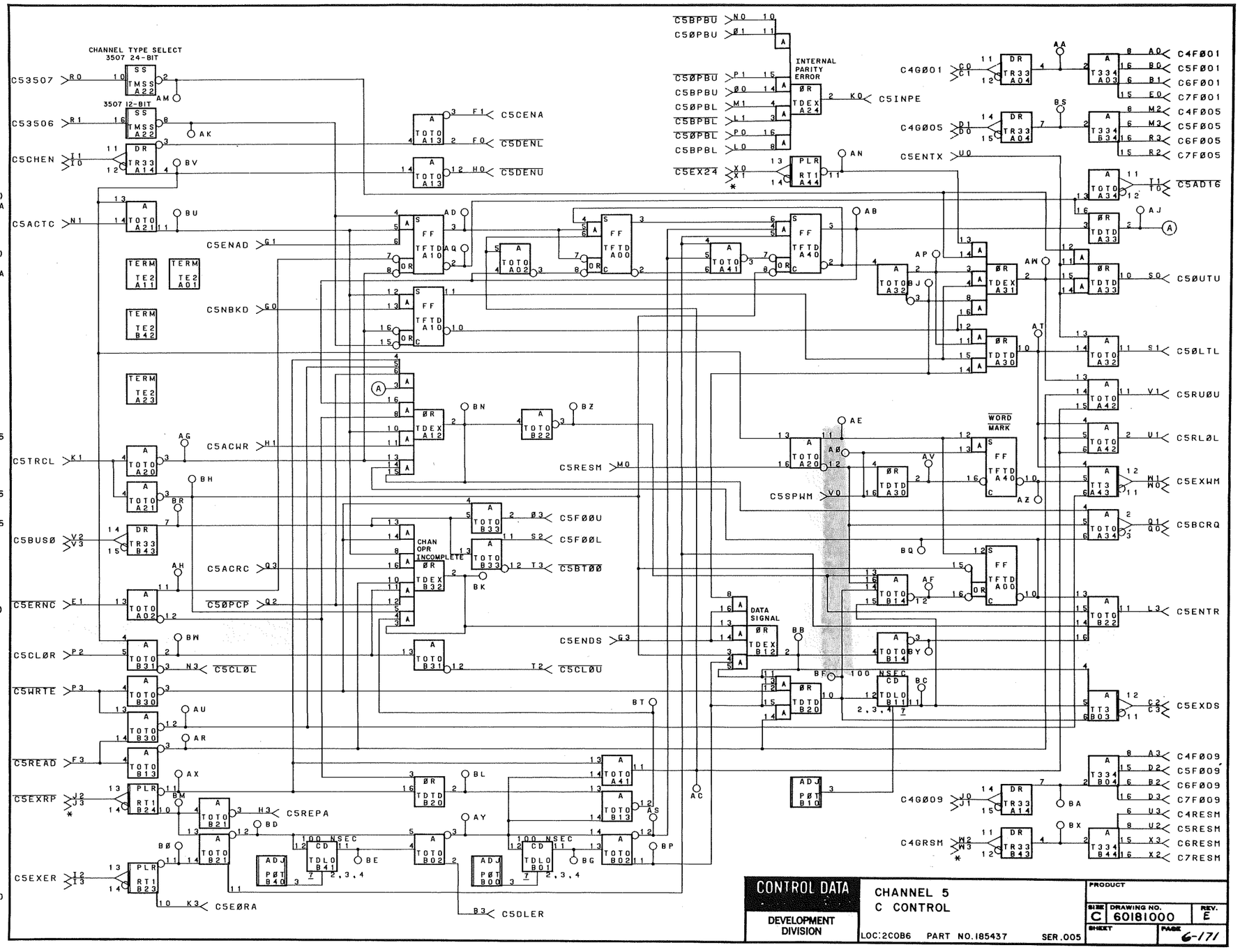
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2CØB9-HØ	6-177	2C0B9-AS	CHL 4 FAN OUT BIT 00 D4 TO OL
A1	2CØB9-I3	6-177	2C0B9-BW	CHL 4 FAN OUT BIT 08 D4 TO OL
B0	2CØB8-HØ	6-181	2C0B8-AS	CHL 5 FAN OUT BIT 00 D4 TO OL
B1	2CØB1-HØ	6-185	2C0B1-AS	CHL 6 FAN OUT BIT 00 D4 TO OL
B2	2CØB1-I3	6-185	2C0B1-BW	CHL 6 FAN OUT BIT 08 D4 TO OL
B3	2CØA7-Q1	6-161		CHL 4 DELAYED EOR TO CONT A
C0	2B1B4-C2	6- 29		D4 BIT 00 TO CHL 4-7 FAN OUT
C1	2B1B4-C3	6- 29		
C2	2A4A09J03D-09			CHL 4 EXTERNAL DATA SIGNAL
	2A4A09J04D-09			
C3	2A4A09J03D-10			
	2A4A09J04D-10			
D0	2B1A3-C3	6- 37		
D1	2B1A3-C2	6- 37		D4 BIT 04 TO CHL 4-7 FAN OUT
D2	2CØB8-I3	6-181	2C0B8-BW	CHL 5 FAN OUT BIT 08 D4 TO OL
D3	2CØB0-I3	6-189	2C0B0-BW	CHL 7 FAN OUT BIT 08 D4 TO OL
E0	2CØB0-HØ	6-189	2C0B0-AS	CHL 7 FAN OUT BIT 00 D4 TO OL
E1	2CØA7-U1	6-161		CHAN 4 NOT(END OF RECORD) + WORD COUNT CONTROL
F0	2CØB4-AØ	6-193		CHL 4 NOT(ENABLE OL TO FAN IN)
F1	2CØA7-D1	6-161		CHL 4 CHANNEL ENABLE TO CONT A
F3	2CØA7-U0	6-161		CHL 4 NOT(READ) TO CONTROL C
G0	2CØA3-J1	6-165		CHL 4 FORWARD ASSY/DISASSY
G1	2CØA6-BØ	6-163		
G3	2CØA7-RØ	6-161		
H0	2CØA5-AØ	6-195		CHL 4 NOT(ENABLE OU TO FAN IN)
H1	2CØA7-J1	6-161		CHL 4 ACTIVATE WRITE
H3	2CØA7-M2	6-161		CHL 4 EXTERNAL REPLY TO CONT A
I0	2B1B5-N1	6- 21		
I1	2B1B5-NØ	6- 21		EN CHAN 4 TO COMMON CONTROL
I2	2A4A09J03E-05			CHL 4 EXTERNAL REJECT SIGNAL
	2A4A09J04E-05			
I3	2A4A09J03E-06			
	2A4A09J04E-06			
J0	2B1B2-G2	6- 33		D4 BIT 08 TO CHL 4-7 FAN OUT
J1	2B1B2-G3	6- 33		
J2	2A4A09J03E-02			
	2A4A09J04E-02			
J3	2A4A09J03E-01			CHL 4 EXTERNAL REPLY SIGNAL
	2A4A09J04E-01			
K0	2CØA7-M3	6-161		CHL 4 INTERNAL PARITY ERROR
K1	2CØA7-U2	6-161		CHL 4 TERMINATE OR CLEAR
K3	2CØA7-S0	6-161		CHL 4 END OF RECORD TO CONT A
L0	2CØB9-C1	6-177		O LOWER PARITY GENERATED CH 4
L1	2CØB9-BØ	6-177		NOT(OL PARITY GENERATED) CHL 4
L3	2CØA7-Q2	6-161		CHL 4 ENABLE TERMINATION
M0	2CØB6-U3	6-171		CHL 4 RESUME FROM BLOCK CONT.
M1	2CØB9-D3	6-177		O LOWER PARITY RECEIVED CHL 4
M2	2CØB9-RØ	6-177	2C0B9-AQ	CHL 4 FAN OUT BIT 04 D4 TO OL
M3	2CØB8-RØ	6-181	2C0B8-AQ	CHL 5 FAN OUT BIT 04 D4 TO OL
N0	2CØA9-BØ	6-179		NOT(OU PARITY GENERATED) CHL 4
N1	2CØA2-BØ	6-167		CHL 4 ACTIVATE CHL CONTROL C
N3	2CØB9-U0	6-177		CHL 4 NOT(CLEAR O REG LOWER)
O0	2CØA9-C1	6-179		O UPPER PARITY GENERATED CHL 4
O1	2CØA9-D3	6-179		O UPPER PARITY RECEIVED CHL 4
O3	2CØA9-C0	6-179		CHL 4 D4 FAN OUT TO OU REG
P0	2CØB9-A3	6-177		NOT(OL PARITY RECEIVED) CHL 4
P1	2CØA9-A3	6-179		NOT(OU PARITY RECEIVED) CHL 4
P2	2CØB3-U3	6-173		CHL 4 CLEAR O REGISTERS
P3	2CØA7-Q0	6-161		CHL 4 NOT(WRITE) TO CONTROL C
Q0	2B1B0-I0	6- 7		
Q1	2B1B0-I1	6- 7		CHL 4 BLOCK CONTROL REQUEST
Q2	2CØA7-P2	6-161		CHL 4 NOT(OPERATION COMPL F/F)
Q3	2CØA7-P1	6-161		CHL 4 ACTIVATE READ TO CONT C
R0	2A4A15J01J-01			CHAN 4 24-BIT MODE IDENTIFIER
R1	2A4A15J01K-01			CHAN 4 12-BIT IDENT FROM OU GROUND PIN
R2	2CØB0-RØ	6-189	2C0B0-AQ	CHL 7 FAN OUT BIT 04 D4 TO OL
R3	2CØB1-RØ	6-185	2C0B1-AQ	CHL 6 FAN OUT BIT 04 D4 TO OL
S0	2CØA9-U1	6-179		CHL 4 ENABLE OU TRANSMISSION
S1	2CØB9-U1	6-177		CHL 4 ENABLE OL TRANSMISSION
S2	2CØB9-C0	6-177		CHL 4 D4 FAN OUT TO OL REG
T0	2B1B0-W3	6- 7		NOT((CH 4)(12-BIT MODE)(A/D))
T1	2B1B0-W2	6- 7		
T2	2CØA9-U0	6-179		CHL 4 NOT(CLEAR O REG UPPER)
T3	2CØA7-A0	6-161		CHL 4 NOT(BUS TO O) TO CONT A
U0	2CØA7-U3	6-161		CHL 4 ENABLE O REG XMISSION
U1	2CØB9-AØ	6-177		CHAN 4 EXT RCVR TO O LOWER
U2	2CØA8-HØ	6-183	2C0A8-AS	CHL 5 FAN OUT BIT 12 D4 TO OU
U3	2CØA9-HØ	6-179	2C0A9-AS	CHL 4 FAN OUT BIT 12 D4 TO OU
V0	2CØB2-U3	6-175	2C0B7-AQ	CHL 4 SUPPRESS WORD MARK
V1	2CØA9-AØ	6-179		CHAN 4 EXT RCVR TO O UPPER
V2	2B1B5-C0	6- 21		EN CHAN 4 BUS TO O XFER/XMIT
V3	2B1B5-C1	6- 21		
W0	2A4A09J03F-02			
	2A4A09J04F-02			
W1	2A4A09J03F-01			CHL 4 EXTERNAL WORD MARK
	2A4A09J04F-01			
W2	2B1B4-P2	6- 29		D4 BIT 12 TO CHL 4-7 FAN OUT
W3	2B1B4-P3	6- 29		
X0	2A4A09J01C-08			
	2A4A09J02C-08			
X1	2A4A09J01C-07			CHL 4 EXT 24 BIT DEVICE CONNTD
	2A4A09J02C-07			
X2	2CØA0-HØ	6-191	2C0A0-AS	CHL 7 FAN OUT BIT 12 D4 TO OU
X3	2CØA1-HØ	6-187	2C0A1-AS	CHL 6 FAN OUT BIT 12 D4 TO OU

PAGE 6-169



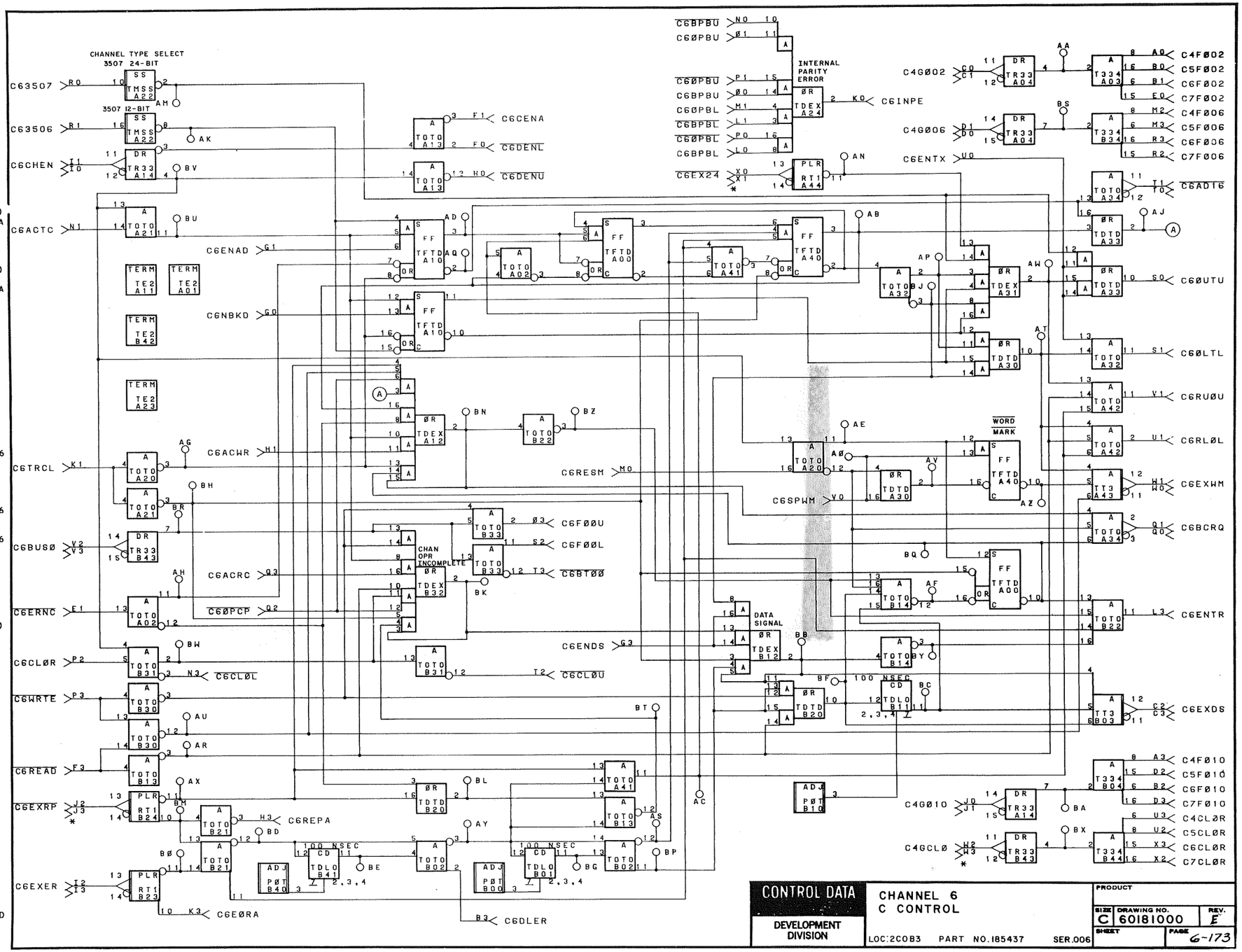
355

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C?B9-G1	6-177	2C0B9-AE	CHL 4 FAN OUT BIT 01 D4 TO OL
A1	2C?B9-F3	6-177	2C0B9-BJ	CHL 4 FAN OUT BIT 09 D4 TO OL
B0	2C?B8-G1	6-181	2C0B8-AE	CHL 5 FAN OUT BIT 01 D4 TO OL
B1	2C?B1-G1	6-185	2C0B1-AE	CHL 6 FAN OUT BIT 01 D4 TO OL
B2	2C?B1-F3	6-185	2C0B1-BJ	CHL 6 FAN OUT BIT 09 D4 TO OL
B3	2C?A6-Q1	6-163		CHL 5 DELAYED EOR TO CONT A
C0	2B1B3-C2	6- 31		D4 BIT 01 TO CHL 4-7 FAN OUT
C1	2B1B3-C3	6- 31		
C2	2A4A10J03D-09			CHL 5 EXTERNAL DATA SIGNAL
	2A4A10J04D-09			
C3	2A4A10J03D-10			
	2A4A10J04D-10			
D0	2B1A2-C3	6- 39		
D1	2B1A2-C2	6- 39		D4 BIT 05 TO CHL 4-7 FAN OUT
D2	2C?B8-F3	6-181	2C0B8-BJ	CHL 5 FAN OUT BIT 09 D4 TO OL
D3	2C?B0-F3	6-189	2C0B0-BJ	CHL 7 FAN OUT BIT 09 D4 TO OL
E0	2C?B0-G1	6-189	2C0B0-AE	CHL 7 FAN OUT BIT 01 D4 TO OL
E1	2C?A6-U1	6-163		CHAN 5 NOT(END OF RECORD) * WORD COUNT CONTROL
F0	2C?B4-H2	6-193		CHL 5 NOT(ENABLE OL TO FAN IN)
F1	2C?A6-D1	6-163		CHL 5 CHANNEL ENABLE TO CONT A
F3	2C?A6-U?	6-163		CHL 5 NOT(READ) TO CONTROL C
G0	2C?A3-J?	6-165		CHL 5 FORWARD ASSY/DISASSY
G1	2C?A6-I1	6-163		
G3	2C?A6-R?	6-163		
H0	2C?A5-H?	6-195		CHL 5 NOT(ENABLE OU TO FAN IN)
H1	2C?A7-J?	6-161		CHL 5 ACTIVATE WRITE
H3	2C?A6-M?	6-163		CHL 5 EXTERNAL REPLY TO CONT A
I0	2B1B5-K1	6- 21		
I1	2B1B5-K?	6- 21		EN CHAN 5 TO COMMON CONTROL
I2	2A4A10J03E-05			CHL 5 EXTERNAL REJECT SIGNAL
	2A4A10J04E-05			
I3	2A4A10J03E-06			
	2A4A10J04E-06			
J0	2B1A4-G2	6- 35		D4 BIT 09 TO CHL 4-7 FAN OUT
J1	2B1A4-G3	6- 35		
J2	2A4A10J03E-02			
	2A4A10J04E-02			
J3	2A4A10J03E-01			CHL 5 EXTERNAL REPLY SIGNAL
	2A4A10J04E-01			
K0	2C?A6-M3	6-163		CHL 5 INTERNAL PARITY ERROR
K1	2C?A6-U2	6-163		CHL 5 TERMINATE OR CLEAR
K3	2C?A6-S?	6-163		CHL 5 END OF RECORD TO CONT A
L0	2C?B8-C1	6-181		O LOWER PARITY GENERATED CH 5
L1	2C?B8-B?	6-181		NOT(OL PARITY GENERATED) CHL 5
L3	2C?A6-O2	6-163		CHL 5 ENABLE TERMINATION
M0	2C?B6-U2	6-171		CHL 5 RESUME FROM BLOCK CONT.
M1	2C?B8-D3	6-181		O LOWER PARITY RECEIVED CHL 5
M2	2C?B9-G?	6-177	2C0B9-AF	CHL 4 FAN OUT BIT 05 D4 TO OL
M3	2C?B8-G?	6-181	2C0B8-AF	CHL 5 FAN OUT BIT 05 D4 TO OL
N0	2C?A8-B?	6-183		NOT(OU PARITY GENERATED) CHL 5
N1	2C?A2-I1	6-167		CHL 5 ACTIVATE CHL CONTROL C
N3	2C?B8-U?	6-181		CHL 5 NOT(CLEAR O REG LOWER)
O0	2C?A8-C1	6-183		O UPPER PARITY GENERATED CHL 5
O1	2C?A8-D3	6-183		O UPPER PARITY RECEIVED CHL 5
O3	2C?A8-C?	6-183		CHL 5 D4 FAN OUT TO OU REG
P0	2C?B8-A3	6-181		NOT(OL PARITY RECEIVED) CHL 5
P1	2C?A8-A3	6-183		NOT(OU PARITY RECEIVED) CHL 5
P2	2C?B3-U?	6-173		CHL 5 CLEAR O REGISTERS
P3	2C?A6-O?	6-163		CHL 5 NOT(WRITE) TO CONTROL C
Q0	2B1B?-J1	6- 7		
Q1	2B1B?-J?	6- 7		CHL 5 BLOCK CONTROL REQUEST
Q2	2C?A6-P2	6-163		CHL 5 NOT(OPERATION COMPL F/F)
Q3	2C?A6-P1	6-163		CHL 5 ACTIVATE READ TO CONT C
R0	2A4A15J01L-01			CHAN 5 24-BIT MODE IDENTIFIER
R1	2A4A15J01M-01			CHAN 5 12-BIT IDENT FROM OU GROUND PIN
R2	2C?B?-G?	6-189	2C0B?-AF	CHL 7 FAN OUT BIT 05 D4 TO OL
R3	2C?B1-G?	6-185	2C0B1-AF	CHL 6 FAN OUT BIT 05 D4 TO OL
S0	2C?A8-U1	6-183		CHL 5 ENABLE OU TRANSMISSION
S1	2C?B8-U1	6-181		CHL 5 ENABLE OL TRANSMISSION
S2	2C?B8-C?	6-181		CHL 5 D4 FAN OUT TO OL REG
T0	2B1B?-V3	6- 7		NOT((CH 5)(12-BIT MODE)(A/D))
T1	2B1B?-V2	6- 7		
T2	2C?A8-U?	6-183		CHL 5 NOT(CLEAR O REG UPPER)
T3	2C?A6-A?	6-163		CHL 5 NOT(BUS TO O) TO CONT A
U0	2C?A6-U3	6-163		CHL 5 ENABLE O REG XMISSION
U1	2C?B8-A?	6-181		CHAN 5 EXT RCVR TO O LOWER
U2	2C?B6-M?	6-171		CHL 5 RESUME FROM BLOCK CONT.
U3	2C?B7-M?	6-169		CHL 4 RESUME FROM BLOCK CONT.
V0	2C?B2-U2	6-175	2C0B6-A0	CHL 5 SUPPRESS WORD MARK
V1	2C?A8-A?	6-183		CHAN 5 EXT RCVR TO O UPPER
V2	2B1B5-D?	6- 21		EN CHAN 5 BUS TO O XFER/XMIT
V3	2B1B5-D1	6- 21		
W0	2A4A10J03F-02			
	2A4A10J04F-02			
W1	2A4A10J03F-01			CHL 5 EXTERNAL WORD MARK
	2A4A10J04F-01			
W2	2B1B?-D?	6- 7		NOT BC RESUME TO CHLS 4-7
W3	2B1B?-D1	6- 7		
X0	2A4A10J01C-08			
	2A4A10J02C-08			
X1	2A4A10J01C-07			CHL 5 EXT 24 BIT DEVICE CONNTD
	2A4A10J02C-07			
X2	2C?B2-M?	6-175		CHL 7 RESUME FROM BLOCK CONT.
X3	2C?B3-M?	6-173		CHL 6 RESUME FROM BLOCK CONT.

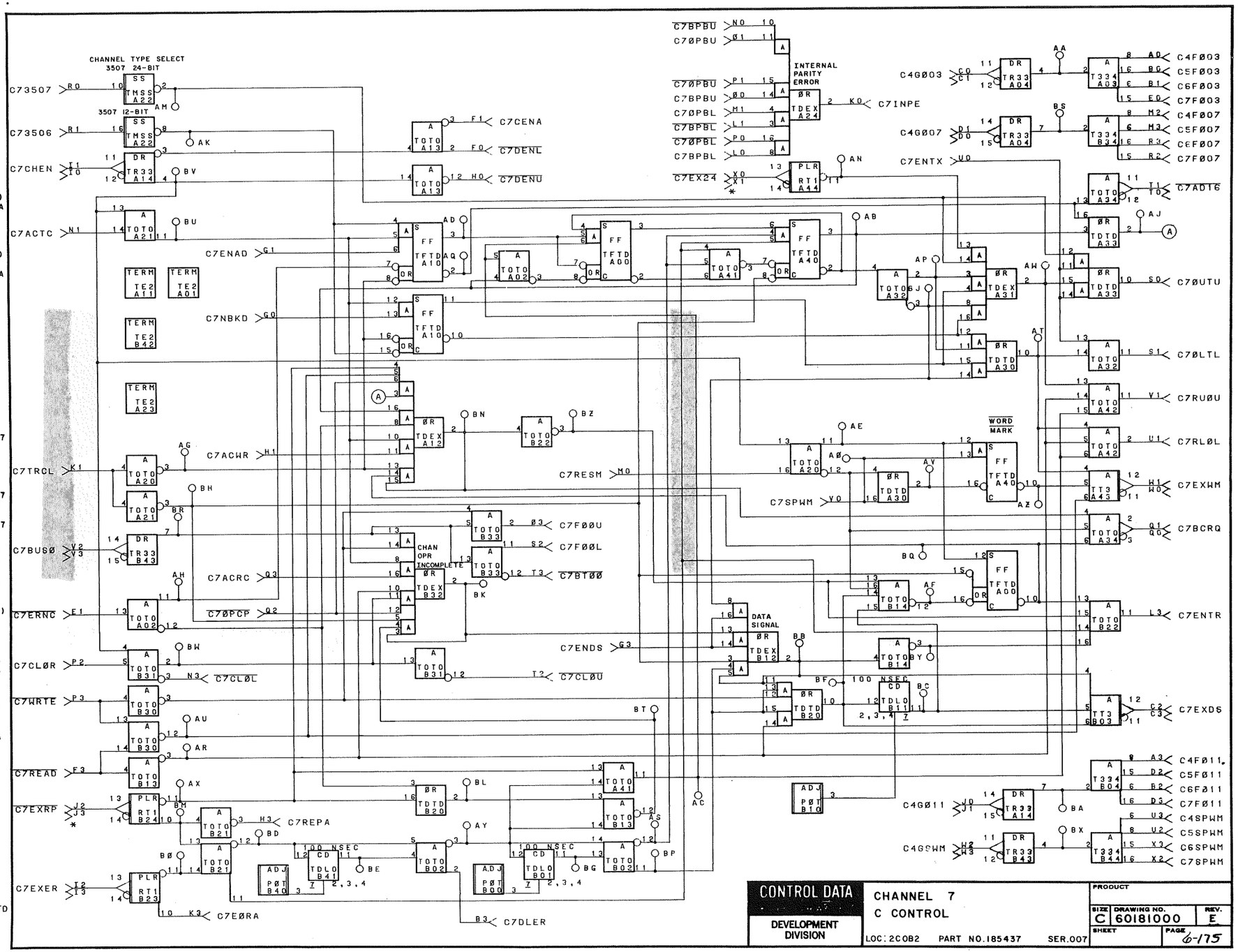


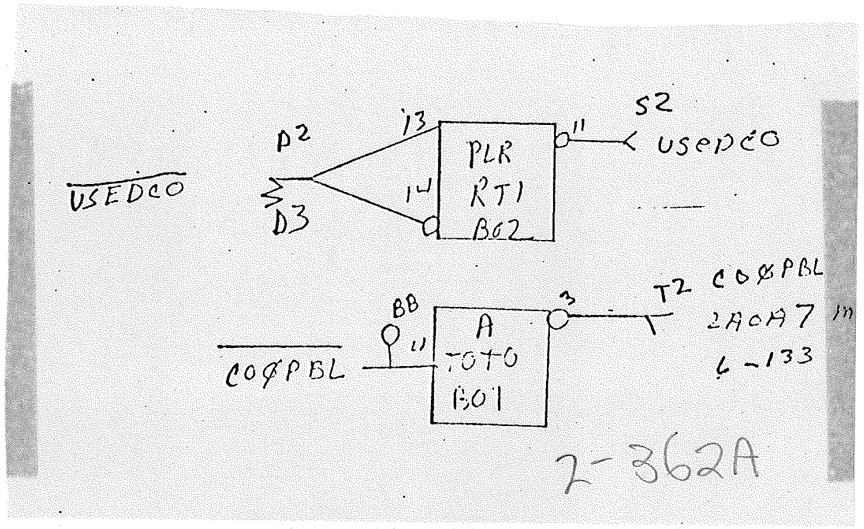
357 36

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C0B9-K0	6-177	2C0B9-AR	CHL 4 FAN OUT BIT 02 D4 TO OL
A1	2C0B9-F2	6-177	2C0B9-B0	CHL 4 FAN OUT BIT 10 D4 TO OL
B0	2C0B8-K0	6-181	2C0B8-AR	CHL 5 FAN OUT BIT 02 D4 TO OL
B1	2C0B1-K0	6-185	2C0B1-AR	CHL 6 FAN OUT BIT 02 D4 TO OL
B2	2C0B1-F2	6-185	2C0B1-B0	CHL 6 FAN OUT BIT 10 D4 TO OL
B3	2C0A3-Q1	6-165		CHL 6 DELAYED EOR TO CONT A
C0	2B1B2-C2	6- 33		D4 BIT 02 TO CHL 4-7 FAN OUT
C1	2B1B2-C3	6- 33		
C2	2A4A11J03D-09			CHL 6 EXTERNAL DATA SIGNAL
	2A4A11J04D-09			
C3	2A4A11J03D-10			
	2A4A11J04D-10			
D0	2B1B4-G3	6- 29		
D1	2B1B4-G2	6- 29		D4 BIT 06 TO CHL 4-7 FAN OUT
D2	2C0B8-F2	6-181	2C0B8-B0	CHL 5 FAN OUT BIT 10 D4 TO OL
D3	2C0B1-F2	6-189	2C0B0-B0	CHL 7 FAN OUT BIT 10 D4 TO OL
E0	2C0B0-K0	6-189	2C0B0-AR	CHL 7 FAN OUT BIT 02 D4 TO OL
E1	2C0A3-U1	6-165		CHAN 6 NOT(END OF RECORD) + WORD COUNT CONTROL
F0	2C0B4-Q3	6-193		CHL 6 NOT(ENABLE OL TO FAN IN)
F1	2C0A3-D1	6-165		CHL 6 CHANNEL ENABLE TO CONT A
F3	2C0A3-U0	6-165		CHL 6 NOT(READ) TO CONTROL C
G0	2C0A3-N1	6-165		CHL 6 FORWARD ASSY/DISASSY
G1	2C0A6-10	6-163		
G3	2C0A3-R0	6-165		
H0	2C0A5-Q3	6-195		CHL 6 NOT(ENABLE OU TO FAN IN)
H1	2C0A7-N1	6-161		CHL 6 ACTIVATE WRITE
H3	2C0A3-M2	6-165		CHL 6 EXTERNAL REPLY TO CONT A
I0	2B1B5-06	6- 21		
I1	2B1B5-01	6- 21		EN CHAN 6 TO COMMON CONTROL
I2	2A4A11J03E-05			CHL 6 EXTERNAL REJECT SIGNAL
	2A4A11J04E-05			
I3	2A4A11J03E-06			
	2A4A11J04E-06			
J0	2B1A3-G2	6- 37		D4 BIT 10 TO CHL 4-7 FAN OUT
J1	2B1A3-G3	6- 37		
J2	2A4A11J03E-02			
	2A4A11J04E-02			
J3	2A4A11J03E-01			CHL 6 EXTERNAL REPLY SIGNAL
	2A4A11J04E-01			
K0	2C0A3-M3	6-165		CHL 6 INTERNAL PARITY ERROR
K1	2C0A3-U2	6-165		CHL 6 TERMINATE OR CLEAR
K3	2C0A3-S0	6-165		CHL 6 END OF RECORD TO CONT A
L0	2C0B1-C1	6-185		O LOWER PARITY GENERATED CH 6
L1	2C0B1-R0	6-185		NOT(OL PARITY GENERATED) CHL 6
L3	2C0A3-02	6-165		CHL 6 ENABLE TERMINATION
M0	2C0B6-X3	6-171		CHL 6 RESUME FROM BLOCK CONT.
M1	2C0B1-D3	6-185		O LOWER PARITY RECEIVED CHL 6
M2	2C0B9-J3	6-177	2C0B9-BZ	CHL 4 FAN OUT BIT 06 D4 TO OL
M3	2C0B8-J3	6-181	2C0B8-BZ	CHL 5 FAN OUT BIT 06 D4 TO OL
N0	2C0A1-B0	6-187		NOT(OU PARITY GENERATED) CHL 6
N1	2C0A2-10	6-167		CHL 6 ACTIVATE CHL CONTROL C
N3	2C0B1-U0	6-185		CHL 6 NOT(CLEAR O REG LOWER)
O0	2C0A1-C1	6-187		O UPPER PARITY GENERATED CHL 6
O1	2C0A1-D3	6-187		O UPPER PARITY RECEIVED CHL 6
O3	2C0A1-C0	6-187		CHL 6 D4 FAN OUT TO OU RFG
P0	2C0B1-A3	6-185		NOT(OL PARITY RECEIVED) CHL 6
P1	2C0A1-A3	6-187		NOT(OU PARITY RECEIVED) CHL 6
P2	2C0B3-X3	6-173		CHL 6 CLEAR O REGISTERS
P3	2C0A3-Q0	6-165		CHL 6 NOT(WRITE) TO CONTROL C
Q0	2B1B0-H0	6- 7		
Q1	2B1B0-H1	6- 7		CHL 6 BLOCK CONTROL REQUEST
Q2	2C0A3-P2	6-165		CHL 6 NOT(OPERATION COMPL F/F)
Q3	2C0A3-P1	6-165		CHL 6 ACTIVATE READ TO CONT C
R0	2A4A15J01N-01			CHAN 6 24-BIT MODE IDENTIFIER
R1	2A4A15J01P-01			CHAN 6 12-BIT IDENT FROM OU GROUND PIN
R2	2C0B0-J3	6-189	2C0B0-BZ	CHL 7 FAN OUT BIT 06 D4 TO OL
R3	2C0B1-J3	6-185	2C0B1-BZ	CHL 6 FAN OUT BIT 06 D4 TO OL
S0	2C0A1-U1	6-187		CHL 6 ENABLE OU TRANSMISSION
S1	2C0B1-U1	6-185		CHL 6 ENABLE OL TRANSMISSION
S2	2C0B1-C0	6-185		CHL 6 D4 FAN OUT TO OL REG
T0	2B1B0-U3	6- 7		NOT((CH 6)(12-BIT MODE)(A/D))
T1	2B1B0-U2	6- 7		
T2	2C0A1-U0	6-187		CHL 6 NOT(CLEAR O REG UPPER)
T3	2C0A3-A0	6-165		CHL 6 NOT(BUS TO O) TO CONT A
U0	2C0A3-U3	6-165		CHL 6 ENABLE O REG XMISSION
U1	2C0B1-A0	6-185		CHAN 6 EXT RCVR TO O LOWER
U2	2C0B6-P2	6-171		CHL 5 CLEAR O REGISTERS
U3	2C0B7-P2	6-169		CHL 4 CLEAR O REGISTERS
V0	2C0B2-X3	6-175	2C0B3-A0	CHL 6 SUPPRESS WORD MARK
V1	2C0A1-A0	6-187		CHAN 6 EXT RCVR TO O UPPER
V2	2B1B5-E0	6- 21		EN CHAN 6 BUS TO O XFER/XMIT
V3	2B1B5-E1	6- 21		
W0	2A4A11J03F-02			
	2A4A11J04F-02			
W1	2A4A11J03F-01			CHL 6 EXTERNAL WORD MARK
	2A4A11J04F-01			
W2	2B1A8-C1	6- 17		NOT CLR O REG TO CHL 4-7
W3	2B1A8-C0	6- 17		
X0	2A4A11J01C-08			
	2A4A11J02C-08			
X1	2A4A11J01C-07			CHL 6 EXT 24 BIT DEVICE CONNTD
	2A4A11J02C-07			
X2	2C0B2-P2	6-175		CHL 7 CLEAR O REGISTERS
X3	2C0B3-P2	6-173		CHL 6 CLEAR O REGISTERS



PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C0B9-H1	6-177	2C0B9-AG	CHL 4 FAN OUT BIT 03 D4 TO OL
A1	2C0B9-E2	6-177	2C0B9-BH	CHL 4 FAN OUT BIT 11 D4 TO OL
B0	2C0B8-H1	6-181	2C0B8-AG	CHL 5 FAN OUT BIT 03 D4 TO OL
B1	2C0B1-H1	6-185	2C0B1-AG	CHL 6 FAN OUT BIT 03 D4 TO OL
B2	2C0B1-E2	6-185	2C0B1-BH	CHL 6 FAN OUT BIT 11 D4 TO OL
B3	2C0A2-Q1	6-167		CHL 7 DELAYED EOR TO CONT A
C0	2B1A4-C2	6- 35		D4 BIT 03 TO CHL 4-7 FAN OUT
C1	2B1A4-C3	6- 35		
C2	2A4A12J03D-09			CHL 7 EXTERNAL DATA SIGNAL
	2A4A12J04D-09			
C3	2A4A12J03D-10			
	2A4A12J04D-10			
D0	2B1B3-G3	6- 31		
D1	2B1B3-G2	6- 31		D4 BIT 07 TO CHL 4-7 FAN OUT
D2	2C0B8-E2	6-181	2C0B8-BH	CHL 5 FAN OUT BIT 11 D4 TO OL
D3	2C0B0-E2	6-189	2C0B0-BH	CHL 7 FAN OUT BIT 11 D4 TO OL
E0	2C0B0-H1	6-189	2C0B0-AG	CHL 7 FAN OUT BIT 03 D4 TO OL
E1	2C0A2-U1	6-167		CHAN 7 NOT(END OF RECORD) + WORD COUNT CONTROL
F0	2C0B4-U2	6-193		CHL 7 NOT(ENABLE OL TO FAN IN)
F1	2C0A2-D1	6-167		CHL 7 CHANNEL ENABLE TO CONT A
F3	2C0A2-U0	6-167		CHL 7 NOT(READ) TO CONTROL C
G0	2C0A3-N0	6-165		CHL 7 FORWARD ASSY/DISASSY
G1	2C0A6-A3	6-163		
G3	2C0A2-R0	6-167		
H0	2C0A5-U2	6-195		CHL 7 NOT(ENABLE OU TO FAN IN)
H1	2C0A7-N0	6-161		CHL 7 ACTIVATE WRITE
H3	2C0A2-M2	6-167		CHL 7 EXTERNAL REPLY TO CONT A
I0	2B1B5-L1	6- 21		
I1	2B1B5-L0	6- 21		EN CHAN 7 TO COMMON CONTROL
I2	2A4A12J03E-05			CHL 7 EXTERNAL REJECT SIGNAL
	2A4A12J04E-05			
I3	2A4A12J03E-06			
	2A4A12J04E-06			
J0	2B1A2-G2	6- 39		D4 BIT 11 TO CHL 4-7 FAN OUT
J1	2B1A2-G3	6- 39		
J2	2A4A12J03E-02			
	2A4A12J04E-02			
J3	2A4A12J03E-01			CHL 7 EXTERNAL REPLY SIGNAL
	2A4A12J04E-01			
K0	2C0A2-M3	6-167		CHL 7 INTERNAL PARITY ERROR
K1	2C0A2-U2	6-167		CHL 7 TERMINATE OR CLEAR
K3	2C0A2-S0	6-167		CHL 7 END OF RECORD TO CONT A
L0	2C0B0-C1	6-189		0 LOWER PARITY GENERATED CH 7
L1	2C0B0-B0	6-189		NOT(OL PARITY GENERATED) CHL 7
L3	2C0A2-O2	6-167		CHL 7 ENABLE TERMINATION
M0	2C0B6-X2	6-171		CHL 7 RESUME FROM BLOCK CONT.
M1	2C0B0-D3	6-189		0 LOWER PARITY RECEIVED CHL 7
M2	2C0B9-E3	6-177	2C0B9-BE	CHL 4 FAN OUT BIT 07 D4 TO OL
M3	2C0B8-E3	6-181	2C0B8-BE	CHL 5 FAN OUT BIT 07 D4 TO OL
N0	2C0A0-B0	6-191		NOT(OU PARITY GENERATED) CHL 7
N1	2C0A2-A3	6-167		CHL 7 ACTIVATE CHL CONTROL C
N3	2C0B0-U0	6-189		CHL 7 NOT(CLEAR O REG LOWER)
O0	2C0A0-C1	6-191		O UPPER PARITY GENERATED CHL 7
O1	2C0A0-D3	6-191		O UPPER PARITY RECEIVED CHL 7
O3	2C0A0-C0	6-191		CHL 7 D4 FAN OUT TO OU REG
P0	2C0B0-A3	6-189		NOT(OL PARITY RECEIVED) CHL 7
P1	2C0A0-A3	6-191		NOT(OU PARITY RECEIVED) CHL 7
P2	2C0B3-X2	6-173		CHL 7 CLEAR O REGISTERS
P3	2C0A2-Q0	6-167		CHL 7 NOT(WRITE) TO CONTROL C
Q0	2B1B0-K1	6- 7		
Q1	2B1B0-K0	6- 7		CHL 7 BLOCK CONTROL REQUEST
Q2	2C0A2-P2	6-167		CHL 7 NOT(OPERATION COMPL F/F)
Q3	2C0A2-P1	6-167		CHL 7 ACTIVATE READ TO CONT C
R0	2A4A15J01R-01			CHAN 7 24-BIT IDENTIFIER
R1	2A4A15J01S-01			CHAN 7 12-BIT IDENT FROM OU GROUND PIN
R2	2C0B0-E3	6-189	2C0B0-BE	CHL 7 FAN OUT BIT 07 D4 TO OL
R3	2C0B1-E3	6-185	2C0B1-BE	CHL 6 FAN OUT BIT 07 D4 TO OL
S0	2C0A0-U1	6-191		CHL 7 ENABLE OU TRANSMISSION
S1	2C0B0-U1	6-189		CHL 7 ENABLE OL TRANSMISSION
S2	2C0B0-C0	6-189		CHL 7 D4 FAN OUT TO OL REG
T0	2B1B0-X2	6- 7		NOT((CH 7)(12-BIT MODE)(A/D))
T1	2B1B0-X3	6- 7		
T2	2C0A0-U0	6-191		CHL 7 NOT(CLEAR O REG UPPER)
T3	2C0A2-A0	6-167		CHL 7 NOT(BUS TO O) TO CONT A
U0	2C0A2-U3	6-167		CHL 7 ENABLE O REG XMISSION
U1	2C0B0-A0	6-189		CHAN 7 EXT RCVR TO O LOWER
U2	2C0B6-V0	6-171	2C0B6-A0	CHL 5 SUPPRESS WORD MARK
U3	2C0B7-V0	6-169	2C0B7-A0	CHL 4 SUPPRESS WORD MARK
V0	2C0B2-X2	6-175	2C0B2-A0	CHL 7 SUPPRESS WORD MARK
V1	2C0A0-A0	6-191		CHAN 7 EXT RCVR TO O UPPER
V2	2B1B5-B1	6- 21		EN CHAN 7 BUS TO O XFER/XMIT
V3	2B1B5-B0	6- 21		
W0	2A4A12J03F-02			
	2A4A12J04F-02			
W1	2A4A12J03F-01			CHL 7 EXTERNAL WORD MARK
	2A4A12J04F-01			
W2	2A1B4-K3	6- 57		SUPPR WORD MARK TO CHAN 4-7 FANOUT
W3	2A1B4-K2	6- 57		
X0	2A4A12J01C-08			
	2A4A12J02C-08			
X1	2A4A12J01C-07			CHL 7 EXT 24 BIT DEVICE CONNTD
	2A4A12J02C-07			
X2	2C0B2-V0	6-175	2C0B2-A0	CHL 7 SUPPRESS WORD MARK
X3	2C0B3-V0	6-173	2C0B3-A0	CHL 6 SUPPRESS WORD MARK

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13
14
PLR
RT1
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11
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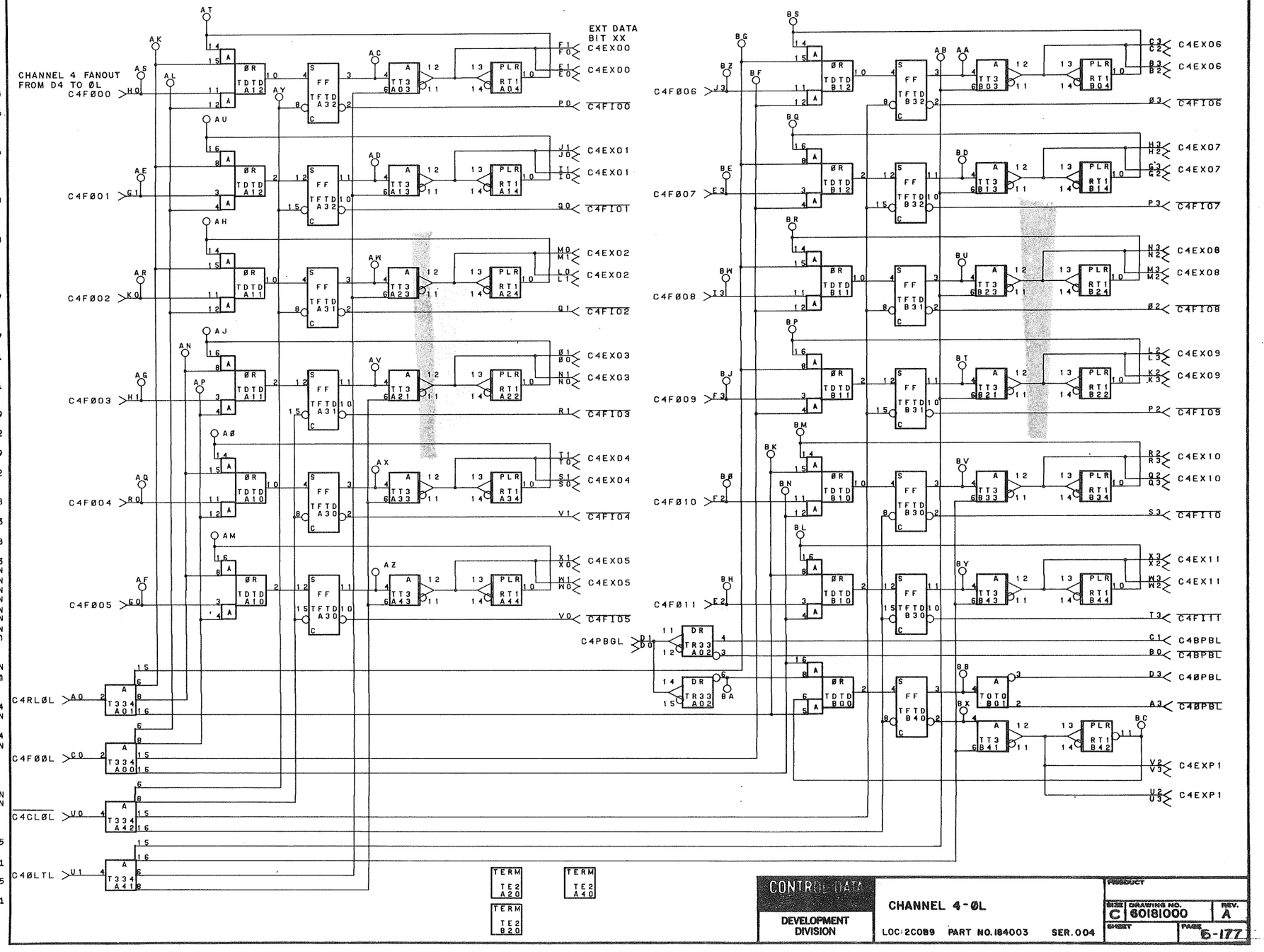
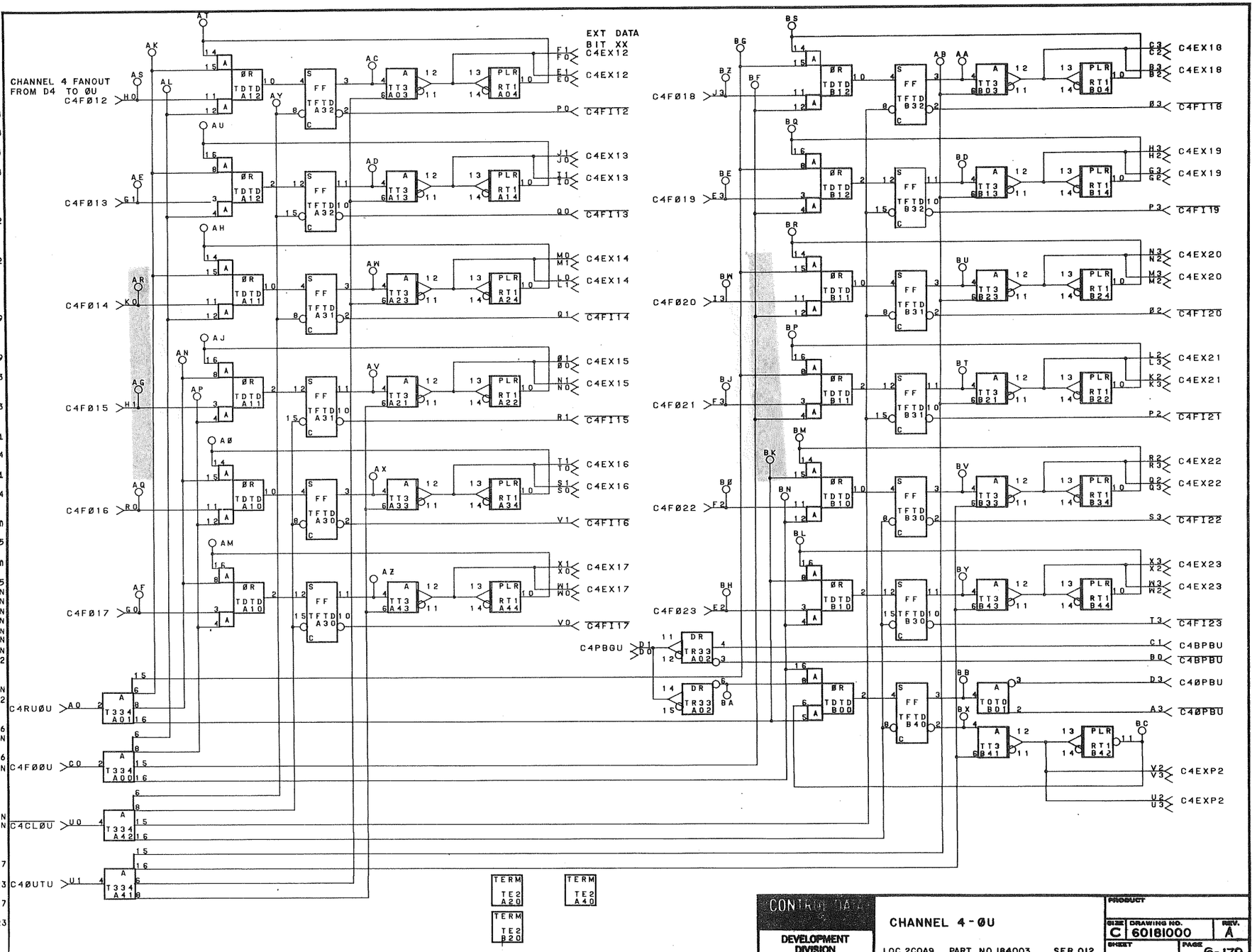
USEDCO
BB
11
A
TOTO
B01
3
T2
CO⌀PBL
CO⌀PBL
2A0A7 IN
4-133

2-362A

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C0B7-U1	6-169		CHAN 4 EXT RCVR TO 0 LOWER
A3	2C0B7-P0	6-169		NOT(0L PARITY RECEIVED) CHL 4
B0	2C0B7-L1	6-169		NOT(0L PARITY GENERATED) CHL 4
B2	2A4A09J03B-04			
B3	2A4A09J03B-03			CHANNEL 4 EXTERNAL DATA BIT 06
C0	2C0B7-S2	6-169		CHL 4 D4 FAN OUT TO 0L REG
C1	2C0B7-L0	6-169		0 LOWER PARITY GENERATED CH 4
C2	2A4A09J04B-04			
C3	2A4A09J04B-03			CHANNEL 4 EXTERNAL DATA BIT 06
D0	2B1B0-K2	6- 7		
D1	2B1B0-K3	6- 7		LOWER PARITY BIT TO CHANNEL 4
D3	2C0B7-M1	6-169		0 LOWER PARITY RECEIVED CHL 4
E0	2A4A09J03A-02			
E1	2A4A09J03A-01			CHANNEL 4 EXTERNAL DATA BIT 00
E2	2C0B2-A3	6-175	2C0B9-BH	CHL 4 FAN OUT BIT 11 D4 TO 0L
E3	2C0B2-M2	6-175	2C0B9-BE	CHL 4 FAN OUT BIT 07 D4 TO 0L
F0	2A4A09J04A-02			
F1	2A4A09J04A-01			CHANNEL 4 EXTERNAL DATA BIT 00
F2	2C0B3-A3	6-173	2C0B9-BD	CHL 4 FAN OUT BIT 10 D4 TO 0L
F3	2C0B6-A3	6-171	2C0B9-BJ	CHL 4 FAN OUT BIT 09 D4 TO 0L
G0	2C0B6-M2	6-171	2C0B9-AF	CHL 4 FAN OUT BIT 05 D4 TO 0L
G1	2C0B6-A0	6-171	2C0B9-AE	CHL 4 FAN OUT BIT 01 D4 TO 0L
G2	2A4A09J03B-06			
G3	2A4A09J03B-05			CHANNEL 4 EXTERNAL DATA BIT 07
H0	2C0B7-A0	6-169	2C0B9-AS	CHL 4 FAN OUT BIT 00 D4 TO 0L
H1	2C0B2-A0	6-175	2C0B9-AG	CHL 4 FAN OUT BIT 03 D4 TO 0L
H2	2A4A09J04B-06			
H3	2A4A09J04B-05			CHANNEL 4 EXTERNAL DATA BIT 07
I0	2A4A09J03A-04			
I1	2A4A09J03A-03			CHANNEL 4 EXTERNAL DATA BIT 01
I3	2C0B7-A3	6-169	2C0B9-BW	CHL 4 FAN OUT BIT 08 D4 TO 0L
J0	2A4A09J04A-04			
J1	2A4A09J04A-03			CHANNEL 4 EXTERNAL DATA BIT 01
J3	2C0B3-M2	6-173	2C0B9-BZ	CHL 4 FAN OUT BIT 06 D4 TO 0L
K0	2C0B3-A0	6-173	2C0B9-AR	CHL 4 FAN OUT BIT 02 D4 TO 0L
K2	2A4A09J03B-09			CHANNEL 4 EXTERNAL DATA BIT 09
K3	2A4A09J03B-10			
L0	2A4A09J04A-05			CHANNEL 4 EXTERNAL DATA BIT 02
L1	2A4A09J04A-06			
L2	2A4A09J04B-09			CHANNEL 4 EXTERNAL DATA BIT 09
L3	2A4A09J04B-10			
M0	2A4A09J03A-05			CHANNEL 4 EXTERNAL DATA BIT 02
M1	2A4A09J03A-06			
M2	2A4A09J03B-08			
M3	2A4A09J03B-07			CHANNEL 4 EXTERNAL DATA BIT 08
N0	2A4A09J03A-08			
N1	2A4A09J03A-07			CHANNEL 4 EXTERNAL DATA BIT 03
N2	2A4A09J04B-08			
N3	2A4A09J04B-07			CHANNEL 4 EXTERNAL DATA BIT 08
O0	2A4A09J04A-08			
O1	2A4A09J04A-07			CHANNEL 4 EXTERNAL DATA BIT 03
O2	2C0B4-B3	6-193	2C0B4-BC	NOT(BIT 08) CHL 4 0L TO FAN IN
O3	2C0B4-A3	6-193	2C0B4-BA	NOT(BIT 06) CHL 4 0L TO FAN IN
P0	2C0B4-D1	6-193	2C0B4-AD	NOT(BIT 00) CHL 4 0L TO FAN IN
P2	2C0B4-C2	6-193	2C0B4-BD	NOT(BIT 09) CHL 4 0L TO FAN IN
P3	2C0B4-B2	6-193	2C0B4-BB	NOT(BIT 07) CHL 4 0L TO FAN IN
Q0	2C0B4-D0	6-193	2C0B4-AE	NOT(BIT 01) CHL 4 0L TO FAN IN
Q1	2C0B4-E1	6-193	2C0B4-AF	NOT(BIT 02) CHL 4 0L TO FAN IN
Q2	2A4A09J03C-01			CHANNEL 4 EXTERNAL DATA BIT 10
Q3	2A4A09J03C-02			
R0	2C0B7-M2	6-169	2C0B9-AQ	CHL 4 FAN OUT BIT 04 D4 TO 0L
R1	2C0B4-E0	6-193	2C0B4-AG	NOT(BIT 03) CHL 4 0L TO FAN IN
R2	2A4A09J04C-01			CHANNEL 4 EXTERNAL DATA BIT 10
R3	2A4A09J04C-02			
S0	2A4A09J03A-10			
S1	2A4A09J03A-09			CHANNEL 4 EXTERNAL DATA BIT 04
S3	2C0B4-C3	6-193	2C0B4-BE	NOT(BIT 10) CHL 4 0L TO FAN IN
T0	2A4A09J04A-10			
T1	2A4A09J04A-09			CHANNEL 4 EXTERNAL DATA BIT 04
T3	2C0B4-D2	6-193	2C0B4-BG	NOT(BIT 11) CHL 4 0L TO FAN IN
U0	2C0B7-N3	6-169		CHL 4 NOT(CLEAR 0 REG LOWER)
U1	2C0B7-S1	6-169		CHL 4 ENABLE 0L TRANSMISSION
U2	2A4A09J03C-05			CHL 4 EXTERNAL PARITY BIT 1
U3	2A4A09J03C-06			
V0	2C0B4-B0	6-193	2C0B4-AB	NOT(BIT 05) CHL 4 0L TO FAN IN
V1	2C0B4-C0	6-193	2C0B4-AC	NOT(BIT 04) CHL 4 0L TO FAN IN
V2	2A4A09J04C-05			CHL 4 EXTERNAL PARITY BIT 1
V3	2A4A09J04C-06			
W0	2A4A09J03B-02			
W1	2A4A09J03B-01			CHANNEL 4 EXTERNAL DATA BIT 05
W2	2A4A09J03C-04			
W3	2A4A09J03C-03			CHANNEL 4 EXTERNAL DATA BIT 11
X0	2A4A09J04B-02			
X1	2A4A09J04B-01			CHANNEL 4 EXTERNAL DATA BIT 05
X2	2A4A09J04C-04			
X3	2A4A09J04C-03			CHANNEL 4 EXTERNAL DATA BIT 11



PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C0B7-V1	6-169		CHAN 4 EXT RCVR TO 0 UPPER
A3	2C0B7-P1	6-169		NOT(0U PARITY RECEIVED) CHL 4
B0	2C0B7-N0	6-169		NOT(0U PARITY GENERATED) CHL 4
B2	2A4A09J01B-04			
B3	2A4A09J01B-03			CHANNEL 4 EXTERNAL DATA BIT 18
C0	2C0B7-03	6-169		CHL 4 D4 FAN OUT TO 0U REG
C1	2C0B7-00	6-169		0 UPPER PARITY GENERATED CHL 4
C2	2A4A09J02B-04			
C3	2A4A09J02B-03			CHANNEL 4 EXTERNAL DATA BIT 18
D0	2B1A0-K2	6- 5		
D1	2B1A0-K3	6- 5		UPPER PARITY BIT TO CHANNEL 4
D3	2C0B7-01	6-169		0 UPPER PARITY RECEIVED CHL 4
E0	2A4A09J01A-02			
E1	2A4A09J01A-01			CHANNEL 4 EXTERNAL DATA BIT 12
E2	2C0A3-S2	6-165	2C0A9-BH	CHL 4 FAN OUT BIT 23 D4 TO 0U
E3	2C0A3-H1	6-165	2C0A9-BE	CHL 4 FAN OUT BIT 19 D4 TO 0U
F0	2A4A09J02A-02			
F1	2A4A09J02A-01			CHANNEL 4 EXTERNAL DATA BIT 12
F2	2C0A6-H1	6-163	2C0A9-BD	CHL 4 FAN OUT BIT 22 D4 TO 0U
F3	2C0A7-H1	6-161	2C0A9-BJ	CHL 4 FAN OUT BIT 21 D4 TO 0U
G0	2C0A7-C0	6-161	2C0A9-AF	CHL 4 FAN OUT BIT 17 D4 TO 0U
G1	2C0A7-S2	6-161	2C0A9-AE	CHL 4 FAN OUT BIT 13 D4 TO 0U
G2	2A4A09J01B-06			
G3	2A4A09J01B-05			CHANNEL 4 EXTERNAL DATA BIT 19
H0	2C0B7-U3	6-169	2C0A9-AS	CHL 4 FAN OUT BIT 12 D4 TO 0U
H1	2C0A3-C0	6-165	2C0A9-AG	CHL 4 FAN OUT BIT 15 D4 TO 0U
H2	2A4A09J02B-06			
H3	2A4A09J02B-05			CHANNEL 4 EXTERNAL DATA BIT 19
I0	2A4A09J01A-04			
I1	2A4A09J01A-03			CHANNEL 4 EXTERNAL DATA BIT 13
I3	2C0A2-H1	6-167	2C0A9-BW	CHL 4 FAN OUT BIT 20 D4 TO 0U
J0	2A4A09J02A-04			
J1	2A4A09J02A-03			CHANNEL 4 EXTERNAL DATA BIT 13
J3	2C0A6-C0	6-163	2C0A9-RZ	CHL 4 FAN OUT BIT 18 D4 TO 0U
K0	2C0A6-S2	6-163	2C0A9-AR	CHL 4 FAN OUT BIT 14 D4 TO 0U
K2	2A4A09J01B-09			CHANNEL 4 EXTERNAL DATA BIT 21
K3	2A4A09J01B-10			
L0	2A4A09J02A-05			CHANNEL 4 EXTERNAL DATA BIT 14
L1	2A4A09J02A-06			
L2	2A4A09J02B-09			CHANNEL 4 EXTERNAL DATA BIT 21
L3	2A4A09J02B-10			
M0	2A4A09J01A-05			CHANNEL 4 EXTERNAL DATA BIT 14
M1	2A4A09J01A-06			
M2	2A4A09J01B-08			
M3	2A4A09J01B-07			CHANNEL 4 EXTERNAL DATA BIT 20
N0	2A4A09J01A-08			
N1	2A4A09J01A-07			CHANNEL 4 EXTERNAL DATA BIT 15
N2	2A4A09J02B-08			
N3	2A4A09J02B-07			CHANNEL 4 EXTERNAL DATA BIT 20
O0	2A4A09J02A-08			
O1	2A4A09J02A-07			CHANNEL 4 EXTERNAL DATA BIT 15
O2	2C0A5-B3	6-195	2C0A5-RC	NOT(BIT 20) CHL 4 0U TO FAN IN
O3	2C0A5-A3	6-195	2C0A5-RA	NOT(BIT 18) CHL 4 0U TO FAN IN
P0	2C0A5-D1	6-195	2C0A5-AD	NOT(BIT 12) CHL 4 0U TO FAN IN
P2	2C0A5-C2	6-195	2C0A5-BD	NOT(BIT 21) CHL 4 0U TO FAN IN
P3	2C0A5-B2	6-195	2C0A5-BB	NOT(BIT 19) CHL 4 0U TO FAN IN
Q0	2C0A5-D0	6-195	2C0A5-AE	NOT(BIT 13) CHL 4 0U TO FAN IN
Q1	2C0A5-E1	6-195	2C0A5-AF	NOT(BIT 14) CHL 4 0U TO FAN IN
Q2	2A4A09J01C-01			CHANNEL 4 EXTERNAL DATA BIT 22
Q3	2A4A09J01C-02			
R0	2C0A2-S2	6-167	2C0A9-AQ	CHL 4 FAN OUT BIT 16 D4 TO 0U
R1	2C0A5-E0	6-195	2C0A5-AG	NOT(BIT 15) CHL 4 0U TO FAN IN
R2	2A4A09J02C-01			CHANNEL 4 EXTERNAL DATA BIT 22
R3	2A4A09J02C-02			
S0	2A4A09J01A-10			
S1	2A4A09J01A-09			CHANNEL 4 EXTERNAL DATA BIT 16
S3	2C0A5-C3	6-195	2C0A5-BE	NOT(BIT 22) CHL 4 0U TO FAN IN
T0	2A4A09J02A-10			
T1	2A4A09J02A-09			CHANNEL 4 EXTERNAL DATA BIT 16
T3	2C0A5-D2	6-195	2C0A5-BG	NOT(BIT 23) CHL 4 0U TO FAN IN
U0	2C0B7-T2	6-169		CHL 4 NOT(CLEAR 0 REG UPPER)
U1	2C0B7-S0	6-169		CHL 4 ENABLE 0U TRANSMISSION
U2	2A4A09J01C-05			CHL 4 EXTERNAL PARITY BIT 2
U3	2A4A09J01C-06			
V0	2C0A5-B0	6-195	2C0A5-AB	NOT(BIT 17) CHL 4 0U TO FAN IN
V1	2C0A5-C0	6-195	2C0A5-AC	NOT(BIT 16) CHL 4 0U TO FAN IN
V2	2A4A09J02C-05			CHL 4 EXTERNAL PARITY BIT 2
V3	2A4A09J02C-06			
W0	2A4A09J01B-02			
W1	2A4A09J01B-01			CHANNEL 4 EXTERNAL DATA BIT 17
W2	2A4A09J01C-04			
W3	2A4A09J01C-03			CHANNEL 4 EXTERNAL DATA BIT 23
X0	2A4A09J02B-02			
X1	2A4A09J02B-01			CHANNEL 4 EXTERNAL DATA BIT 17
X2	2A4A09J02C-04			
X3	2A4A09J02C-03			CHANNEL 4 EXTERNAL DATA BIT 23



CONTROL DATA
DEVELOPMENT DIVISION

CHANNEL 4-0U

LOC 2C0A9 PART NO. 184003 SER 012

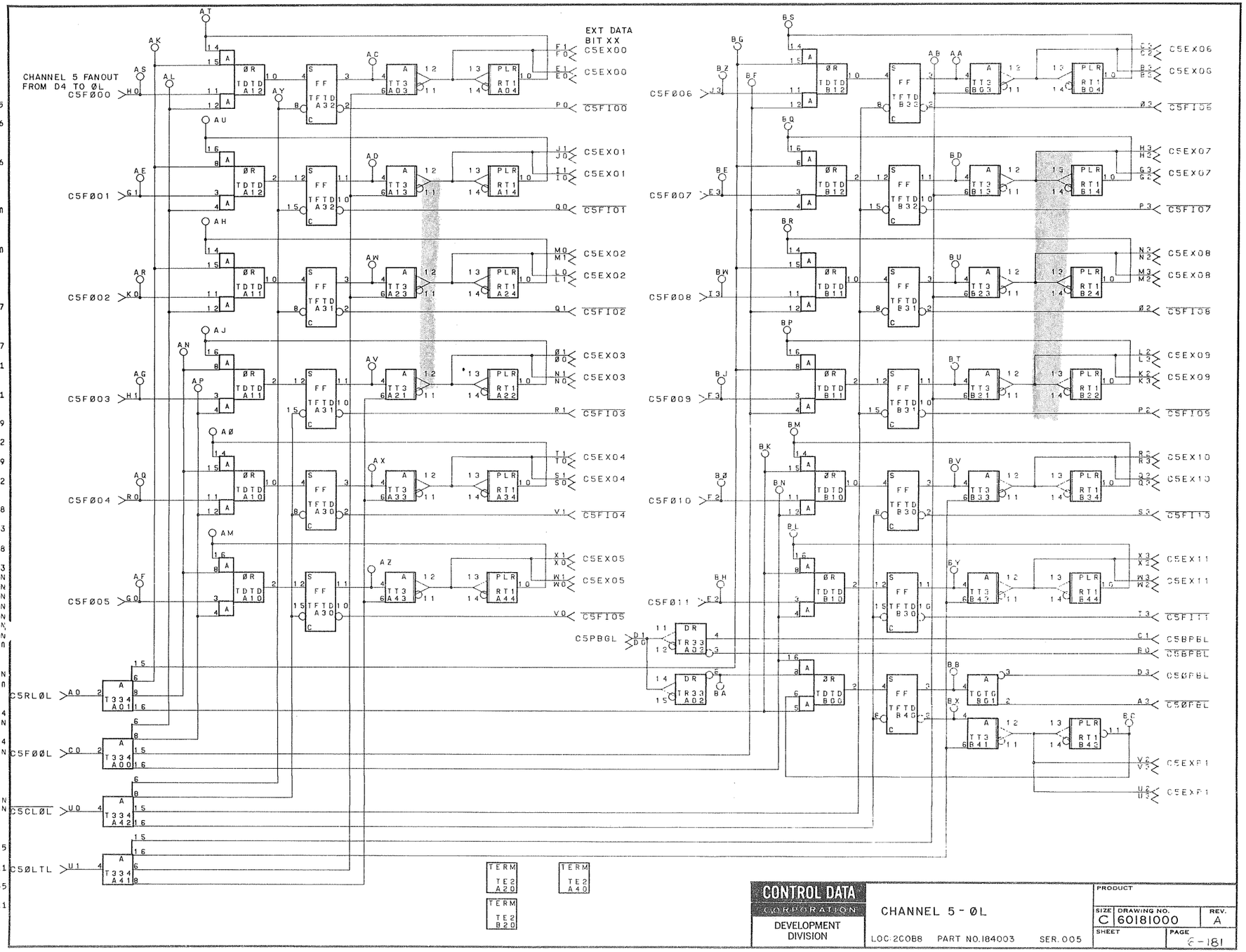
PRODUCT

SIZE	DRAWING NO.	REV.
C	60181000	A

SHEET PAGE 6-179

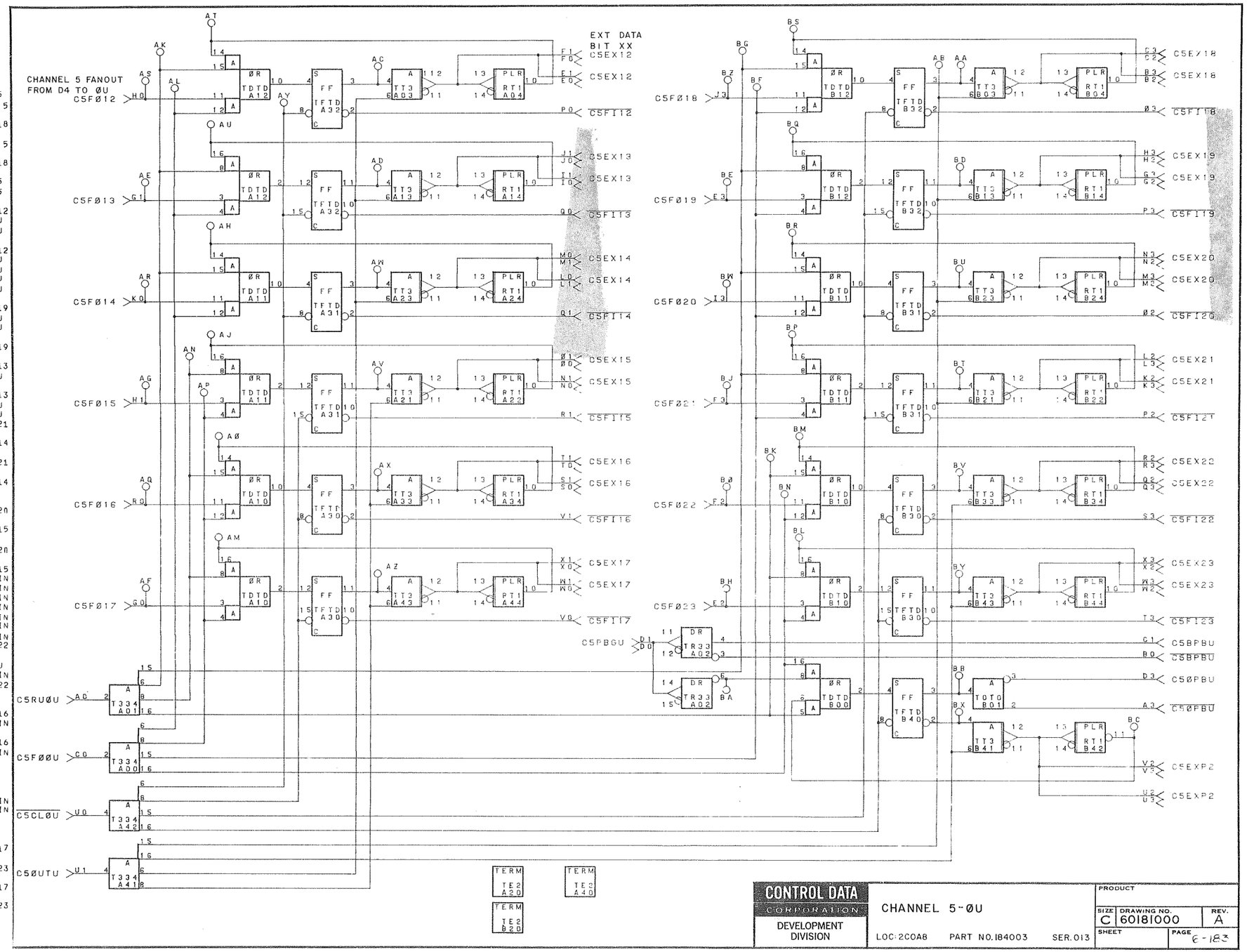
365

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C0R6-U1	6-171		CHAN 5 EXT RCVR TO 0 LOWER
A3	2C0R6-P0	6-171		NOT(OL PARITY RECEIVED) CHL 5
B0	2C0R6-L1	6-171		NOT(OL PARITY GENERATED) CHL 5
B2	2A4A10J03B-04			
B3	2A4A10J03B-03			CHANNEL 5 EXTERNAL DATA BIT 06
C0	2C0R6-S2	6-171		CHL 5 D4 FAN OUT TO OL REG
C1	2C0R6-L0	6-171		0 LOWER PARITY GENERATED CH 5
C2	2A4A10J04B-04			
C3	2A4A10J04B-03			CHANNEL 5 EXTERNAL DATA BIT 06
D0	2R1B0-J2	6- 7		
D1	2R1B0-J3	6- 7		LOWER PARITY BIT TO CHANNEL 5
D3	2C0R6-M1	6-171		0 LOWER PARITY RECEIVED CHL 5
E0	2A4A10J03A-02			
E1	2A4A10J03A-01			CHANNEL 5 EXTERNAL DATA BIT 00
E2	2C0R2-D2	6-175	2C0B8-RH	CHL 5 FAN OUT BIT 11 D4 TO OL
E3	2C0R2-M3	6-175	2C0B8-RE	CHL 5 FAN OUT BIT 07 D4 TO OL
F0	2A4A10J04A-02			
F1	2A4A10J04A-01			CHANNEL 5 EXTERNAL DATA BIT 00
F2	2C0B3-D2	6-173	2C0B8-RD	CHL 5 FAN OUT BIT 10 D4 TO OL
F3	2C0R6-D2	6-171	2C0B8-RJ	CHL 5 FAN OUT BIT 09 D4 TO OL
G0	2C0R6-M3	6-171	2C0B8-AF	CHL 5 FAN OUT BIT 05 D4 TO OL
G1	2C0B6-B0	6-171	2C0B8-AE	CHL 5 FAN OUT BIT 01 D4 TO OL
G2	2A4A10J03B-06			
G3	2A4A10J03B-05			CHANNEL 5 EXTERNAL DATA BIT 07
H0	2C0B7-B0	6-169	2C0B8-AS	CHL 5 FAN OUT BIT 00 D4 TO OL
H1	2C0B2-B0	6-175	2C0B8-AG	CHL 5 FAN OUT BIT 03 D4 TO OL
H2	2A4A10J04B-06			
H3	2A4A10J04B-05			CHANNEL 5 EXTERNAL DATA BIT 07
I0	2A4A10J03A-04			
I1	2A4A10J03A-03			CHANNEL 5 EXTERNAL DATA BIT 01
I3	2C0B7-D2	6-169	2C0B8-RW	CHL 5 FAN OUT BIT 08 D4 TO OL
J0	2A4A10J04A-04			
J1	2A4A10J04A-03			CHANNEL 5 EXTERNAL DATA BIT 01
J3	2C0B3-M3	6-173	2C0B8-RZ	CHL 5 FAN OUT BIT 06 D4 TO OL
K0	2C0R3-B0	6-173	2C0B8-AR	CHL 5 FAN OUT BIT 02 D4 TO OL
K2	2A4A10J03B-09			CHANNEL 5 EXTERNAL DATA BIT 09
K3	2A4A10J03B-10			
L0	2A4A10J04A-05			CHANNEL 5 EXTERNAL DATA BIT 02
L1	2A4A10J04A-06			
L2	2A4A10J04B-09			CHANNEL 5 EXTERNAL DATA BIT 09
L3	2A4A10J04B-10			
M0	2A4A10J03A-05			CHANNEL 5 EXTERNAL DATA BIT 02
M1	2A4A10J03A-06			
M2	2A4A10J03B-08			
M3	2A4A10J03B-07			CHANNEL 5 EXTERNAL DATA BIT 08
N0	2A4A10J03A-08			
N1	2A4A10J03A-07			CHANNEL 5 EXTERNAL DATA BIT 03
N2	2A4A10J04B-08			
N3	2A4A10J04B-07			CHANNEL 5 EXTERNAL DATA BIT 08
O0	2A4A10J04A-08			
O1	2A4A10J04A-07			CHANNEL 5 EXTERNAL DATA BIT 03
O2	2C0B4-L2	6-193	2C0B4-RK	NOT(BIT 08) CHL 5 OL TO FAN IN
O3	2C0B4-M3	6-193	2C0B4-RJ	NOT(BIT 06) CHL 5 OL TO FAN IN
P0	2C0B4-H0	6-193	2C0B4-AN	NOT(BIT 00) CHL 5 OL TO FAN IN
P2	2C0B4-L3	6-193	2C0B4-RL	NOT(BIT 09) CHL 5 OL TO FAN IN
P3	2C0B4-G3	6-193	2C0B4-RH	NOT(BIT 07) CHL 5 OL TO FAN IN
Q0	2C0B4-H1	6-193	2C0B4-AM	NOT(BIT 01) CHL 5 OL TO FAN IN
Q1	2C0B4-G0	6-193	2C0B4-AL	NOT(BIT 02) CHL 5 OL TO FAN IN
Q2	2A4A10J03C-01			CHANNEL 5 EXTERNAL DATA BIT 10
Q3	2A4A10J03C-02			
R0	2C0B7-M3	6-169	2C0B8-AQ	CHL 5 FAN OUT BIT 04 D4 TO OL
R1	2C0B4-G1	6-193	2C0B4-AK	NOT(BIT 03) CHL 5 OL TO FAN IN
R2	2A4A10J04C-01			CHANNEL 5 EXTERNAL DATA BIT 10
R3	2A4A10J04C-02			
S0	2A4A10J03A-10			
S1	2A4A10J03A-09			CHANNEL 5 EXTERNAL DATA BIT 04
S3	2C0R4-J2	6-193	2C0B4-RM	NOT(BIT 10) CHL 5 OL TO FAN IN
T0	2A4A10J04A-10			
T1	2A4A10J04A-09			CHANNEL 5 EXTERNAL DATA BIT 04
T3	2C0B4-J3	6-193	2C0B4-RN	NOT(BIT 11) CHL 5 OL TO FAN IN
U0	2C0R6-N3	6-171		CHL 5 NOT(CLEAR 0 REG LOWER)
U1	2C0R6-S1	6-171		CHL 5 ENABLE OL TRANSMISSION
U2	2A4A10J03C-05			CHL 5 EXTERNAL PARITY BIT 1
U3	2A4A10J03C-06			
V0	2C0R4-F1	6-193	2C0B4-AH	NOT(BIT 05) CHL 5 OL TO FAN IN
V1	2C0R4-F0	6-193	2C0B4-AJ	NOT(BIT 04) CHL 5 OL TO FAN IN
V2	2A4A10J04C-05			CHL 5 EXTERNAL PARITY BIT 1
V3	2A4A10J04C-06			
W0	2A4A10J03B-02			
W1	2A4A10J03B-01			CHANNEL 5 EXTERNAL DATA BIT 05
W2	2A4A10J03C-04			
W3	2A4A10J03C-03			CHANNEL 5 EXTERNAL DATA BIT 11
X0	2A4A10J04B-02			
X1	2A4A10J04B-01			CHANNEL 5 EXTERNAL DATA BIT 05
X2	2A4A10J04C-04			
X3	2A4A10J04C-03			CHANNEL 5 EXTERNAL DATA BIT 11



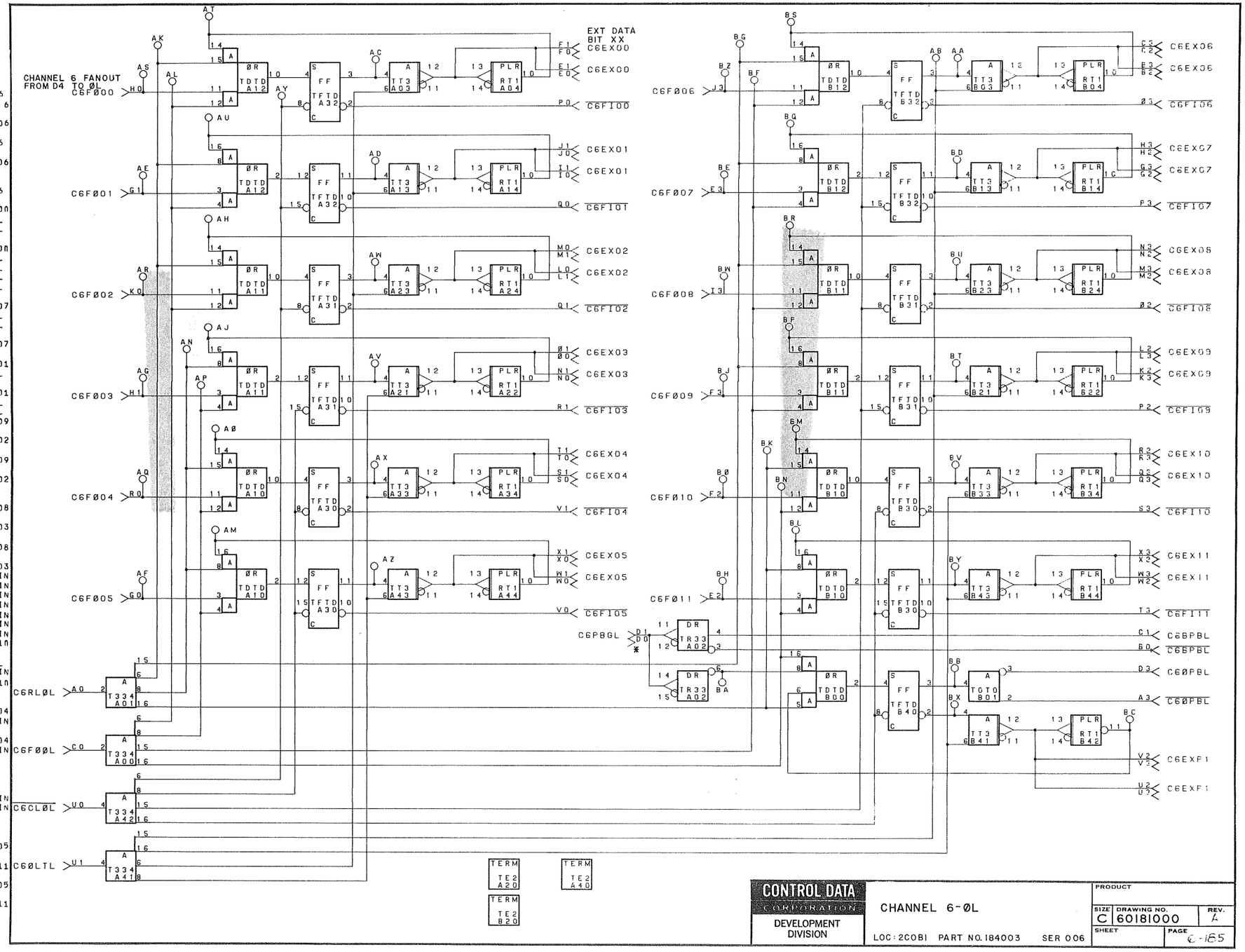
CONTROL DATA CORPORATION DEVELOPMENT DIVISION	CHANNEL 5 - ØL LOC 2C0B8 PART NO. 184003 SER. 005	PRODUCT SIZE C · DRAWING NO. 60181000 · REV. A SHEET · PAGE 6-181	

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C0B6-V1	6-171		CHAN 5 EXT RCVR TO 0 UPPER
A3	2C0B6-P1	6-171		NOT(0U PARITY RECEIVED) CHL 5
B0	2C0B6-N0	6-171		NOT(0U PARITY GENERATED) CHL 5
B2	2A4A10J01B-04			
B3	2A4A10J01B-03			CHANNEL 5 EXTERNAL DATA BIT 18
C0	2C0B6-03	6-171		CHL 5 D4 FAN OUT TO 0U REG
C1	2C0B6-00	6-171		0 UPPER PARITY GENERATED CHL 5
C2	2A4A10J02B-04			
C3	2A4A10J02B-03			CHANNEL 5 EXTERNAL DATA BIT 18
D0	2R1A0-J2	6- 5		
D1	2R1A0-J3	6- 5		UPPER PARITY BIT TO CHANNEL 5
D3	2C0B6-01	6-171		0 UPPER PARITY RECEIVED CHL 5
E0	2A4A10J01A-02			
E1	2A4A10J01A-01			CHANNEL 5 EXTERNAL DATA BIT 12
E2	2C0A3-S3	6-165	2C0A8-AH	CHL 5 FAN OUT BIT 23 D4 TO 0U
E3	2C0A3-H0	6-165	2C0A8-AE	CHL 5 FAN OUT BIT 19 D4 TO 0U
F0	2A4A10J02A-02			
F1	2A4A10J02A-01			CHANNEL 5 EXTERNAL DATA BIT 12
F2	2C0A6-H0	6-163	2C0A8-AD	CHL 5 FAN OUT BIT 22 D4 TO 0U
F3	2C0A7-H0	6-161	2C0A8-AJ	CHL 5 FAN OUT BIT 21 D4 TO 0U
G0	2C0A7-C1	6-161	2C0A8-AF	CHL 5 FAN OUT BIT 17 D4 TO 0U
G1	2C0A7-S3	6-161	2C0A8-AE	CHL 5 FAN OUT BIT 13 D4 TO 0U
G2	2A4A1NJ01A-06			
G3	2A4A10J01A-05			CHANNEL 5 EXTERNAL DATA BIT 19
H0	2C0A7-U2	6-169	2C0A8-AS	CHL 5 FAN OUT BIT 12 D4 TO 0U
H1	2C0A3-C1	6-165	2C0A8-AG	CHL 5 FAN OUT BIT 15 D4 TO 0U
H2	2A4A10J02B-06			
H3	2A4A10J02A-05			CHANNEL 5 EXTERNAL DATA BIT 19
I0	2A4A10J01A-04			
I1	2A4A10J01A-03			CHANNEL 5 EXTERNAL DATA BIT 13
I3	2C0A2-H0	6-167	2C0A8-AW	CHL 5 FAN OUT BIT 20 D4 TO 0U
J0	2A4A10J02A-04			
J1	2A4A10J02A-03			CHANNEL 5 EXTERNAL DATA BIT 13
J3	2C0A6-C1	6-163	2C0A8-AZ	CHL 5 FAN OUT BIT 18 D4 TO 0U
K0	2C0A6-S3	6-163	2C0A8-AR	CHL 5 FAN OUT BIT 14 D4 TO 0U
K2	2A4A10J01B-09			CHANNEL 5 EXTERNAL DATA BIT 21
K3	2A4A10J01B-10			
L0	2A4A10J02A-05			CHANNEL 5 EXTERNAL DATA BIT 14
L1	2A4A10J02A-06			
L2	2A4A10J02B-09			CHANNEL 5 EXTERNAL DATA BIT 21
L3	2A4A10J02B-10			
M0	2A4A10J01A-05			CHANNEL 5 EXTERNAL DATA BIT 14
M1	2A4A10J01A-06			
M2	2A4A10J01B-08			
M3	2A4A10J01B-07			CHANNEL 5 EXTERNAL DATA BIT 20
N0	2A4A10J01A-08			
N1	2A4A10J01A-07			CHANNEL 5 EXTERNAL DATA BIT 15
N2	2A4A10J02B-08			
N3	2A4A10J02B-07			CHANNEL 5 EXTERNAL DATA BIT 20
O0	2A4A10J02A-08			
O1	2A4A10J02A-07			CHANNEL 5 EXTERNAL DATA BIT 15
O2	2C0A5-L2	6-195	2C0A5-AK	NOT(BIT 20) CHL 5 0U TO FAN IN
O3	2C0A5-H3	6-195	2C0A5-AJ	NOT(BIT 18) CHL 5 0U TO FAN IN
P0	2C0A5-H0	6-195	2C0A5-AN	NOT(BIT 12) CHL 5 0U TO FAN IN
P2	2C0A5-L3	6-195	2C0A5-AL	NOT(BIT 21) CHL 5 0U TO FAN IN
P3	2C0A5-G3	6-195	2C0A5-AH	NOT(BIT 19) CHL 5 0U TO FAN IN
Q0	2C0A5-H1	6-195	2C0A5-AM	NOT(BIT 13) CHL 5 0U TO FAN IN
Q1	2C0A5-G0	6-195	2C0A5-AL	NOT(BIT 14) CHL 5 0U TO FAN IN
Q2	2A4A10J01C-01			CHANNEL 5 EXTERNAL DATA BIT 22
Q3	2A4A10J01C-02			
R0	2C0A2-S3	6-167	2C0A8-AQ	CHL 5 FAN OUT BIT 16 D4 TO 0U
R1	2C0A5-G1	6-195	2C0A5-AK	NOT(BIT 15) CHL 5 0U TO FAN IN
R2	2A4A10J02C-01			CHANNEL 5 EXTERNAL DATA BIT 22
R3	2A4A10J02C-02			
S0	2A4A10J01A-10			
S1	2A4A10J01A-09			CHANNEL 5 EXTERNAL DATA BIT 16
S3	2C0A5-J2	6-195	2C0A5-AM	NOT(BIT 22) CHL 5 0U TO FAN IN
T0	2A4A10J02A-10			
T1	2A4A10J02A-09			CHANNEL 5 EXTERNAL DATA BIT 16
T3	2C0A5-J3	6-195	2C0A5-AN	NOT(BIT 23) CHL 5 0U TO FAN IN
U0	2C0B6-T2	6-171		CHL 5 NOT(CLEAR 0 REG (UPPER)
U1	2C0B6-S0	6-171		CHL 5 ENABLE 0U TRANSMISSION
U2	2A4A10J01C-05			CHL 5 EXTERNAL PARITY BIT 2
U3	2A4A10J01C-06			
V0	2C0A5-F1	6-195	2C0A5-AH	NOT(BIT 17) CHL 5 0U TO FAN IN
V1	2C0A5-F0	6-195	2C0A5-AJ	NOT(BIT 16) CHL 5 0U TO FAN IN
V2	2A4A10J02C-05			CHL 5 EXTERNAL PARITY BIT 2
V3	2A4A10J02C-06			
W0	2A4A10J01B-02			
W1	2A4A10J01B-01			CHANNEL 5 EXTERNAL DATA BIT 17
W2	2A4A10J01C-04			
W3	2A4A10J01C-03			CHANNEL 5 EXTERNAL DATA BIT 23
X0	2A4A10J02B-02			
X1	2A4A10J02B-01			CHANNEL 5 EXTERNAL DATA BIT 17
X2	2A4A10J02C-04			
X3	2A4A10J02C-03			CHANNEL 5 EXTERNAL DATA BIT 23



CONTROL DATA CORPORATION	CHANNEL 5-0U	PRODUCT
DEVELOPMENT DIVISION	LOC 2C0A8 PART NO. 184003 SER. 013	SIZE C · DRAWING NO. 60181000 · REV. A · SHEET · PAGE 6-183

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C0B3-U1	6-173		CHAN 6 EXT RCVR TO 0 LOWER
A3	2C0B3-P0	6-173		NOT(OL PARITY RECEIVED) CHL 6
B0	2C0B3-L1	6-173		NOT(OL PARITY GENERATED) CHL 6
B2	2A4A11J03R-04			
B3	2A4A11J03R-03			CHANNEL 6 EXTERNAL DATA BIT 06
C0	2C0B3-S2	6-173		CHL 6 D4 FAN OUT TO OL REG
C1	2C0B3-L0	6-173		0 LOWER PARITY GENERATED CH 6
C2	2A4A11J04H-04			
C3	2A4A11J04B-03			CHANNEL 6 EXTERNAL DATA BIT 06
D0	2R1R0-H2	6- 7		
D1	2R1R0-H3	6- 7		NOT LOW PARITY BIT TO CHL 6
D3	2C0B3-M1	6-173		0 LOWER PARITY RECEIVED CHL 6
E0	2A4A11J03A-02			
E1	2A4A11J03A-01			CHANNEL 6 EXTERNAL DATA BIT 00
E2	2C0B2-B2	6-175	2C0B1-PH	CHL 6 FAN OUT BIT 11 D4 TO OL
E3	2C0B2-R3	6-175	2C0B1-RE	CHL 6 FAN OUT BIT 07 D4 TO OL
F0	2A4A11J04A-02			
F1	2A4A11J04A-01			CHANNEL 6 EXTERNAL DATA BIT 00
F2	2C0B3-B2	6-173	2C0B1-RD	CHL 6 FAN OUT BIT 10 D4 TO OL
F3	2C0B6-B2	6-171	2C0B1-RJ	CHL 6 FAN OUT BIT 09 D4 TO OL
G0	2C0B6-R3	6-171	2C0B1-AF	CHL 6 FAN OUT BIT 05 D4 TO OL
G1	2C0B6-B1	6-171	2C0B1-AE	CHL 6 FAN OUT BIT 01 D4 TO OL
G2	2A4A11J03R-06			
G3	2A4A11J03R-05			CHANNEL 6 EXTERNAL DATA BIT 07
H0	2C0B7-B1	6-169	2C0B1-AS	CHL 6 FAN OUT BIT 00 D4 TO OL
H1	2C0B2-B1	6-175	2C0B1-AG	CHL 6 FAN OUT BIT 03 D4 TO OL
H2	2A4A11J04B-06			
H3	2A4A11J04B-05			CHANNEL 6 EXTERNAL DATA BIT 07
I0	2A4A11J03A-04			
I1	2A4A11J03A-03			CHANNEL 6 EXTERNAL DATA BIT 01
I3	2C0B7-B2	6-169	2C0B1-RW	CHL 6 FAN OUT BIT 08 D4 TO OL
J0	2A4A11J04A-04			
J1	2A4A11J04A-03			CHANNEL 6 EXTERNAL DATA BIT 01
J3	2C0B3-R3	6-173	2C0B1-RZ	CHL 6 FAN OUT BIT 06 D4 TO OL
K0	2C0B3-B1	6-173	2C0B1-AR	CHL 6 FAN OUT BIT 02 D4 TO OL
K2	2A4A11J03R-09			CHANNEL 6 EXTERNAL DATA BIT 09
K3	2A4A11J03R-10			
L0	2A4A11J04A-05			CHANNEL 6 EXTERNAL DATA BIT 02
L1	2A4A11J04A-06			
L2	2A4A11J04R-09			CHANNEL 6 EXTERNAL DATA BIT 09
L3	2A4A11J04B-10			
M0	2A4A11J03A-05			CHANNEL 6 EXTERNAL DATA BIT 02
M1	2A4A11J03A-06			
M2	2A4A11J03R-08			
M3	2A4A11J03R-07			CHANNEL 6 EXTERNAL DATA BIT 08
N0	2A4A11J03A-08			
N1	2A4A11J03A-07			CHANNEL 6 EXTERNAL DATA BIT 03
N2	2A4A11J04B-08			
N3	2A4A11J04B-07			CHANNEL 6 EXTERNAL DATA BIT 08
O0	2A4A11J04A-08			
O1	2A4A11J04A-07			CHANNEL 6 EXTERNAL DATA BIT 03
O2	2C0B4-U3	6-193	2C0B4-RT	NOT(BIT 08) CHL 6 OL TO FAN IN
O3	2C0B4-R2	6-193	2C0B4-RQ	NOT(BIT 06) CHL 6 OL TO FAN IN
P0	2C0B4-P0	6-193	2C0B4-AQ	NOT(BIT 00) CHL 6 OL TO FAN IN
P2	2C0B4-T3	6-193	2C0B4-RS	NOT(BIT 09) CHL 6 OL TO FAN IN
P3	2C0B4-S3	6-193	2C0B4-RR	NOT(BIT 07) CHL 6 OL TO FAN IN
Q0	2C0B4-D1	6-193	2C0B4-AP	NOT(BIT 01) CHL 6 OL TO FAN IN
Q1	2C0B4-P1	6-193	2C0B4-AR	NOT(BIT 02) CHL 6 OL TO FAN IN
Q2	2A4A11J03C-01			CHANNEL 6 EXTERNAL DATA BIT 10
Q3	2A4A11J03C-02			
R0	2C0B7-R3	6-169	2C0B1-AQ	CHL 6 FAN OUT BIT 04 D4 TO OL
R1	2C0B4-D0	6-193	2C0B4-AQ	NOT(BIT 03) CHL 6 OL TO FAN IN
R2	2A4A11J04C-01			CHANNEL 6 EXTERNAL DATA BIT 10
R3	2A4A11J04C-02			
S0	2A4A11J03A-10			
S1	2A4A11J03A-09			CHANNEL 6 EXTERNAL DATA BIT 04
S3	2C0B4-R3	6-193	2C0B4-RP	NOT(BIT 10) CHL 6 OL TO FAN IN
T0	2A4A11J04A-10			
T1	2A4A11J04A-09			CHANNEL 6 EXTERNAL DATA BIT 04
T3	2C0B4-Q2	6-193	2C0B4-RO	NOT(BIT 11) CHL 6 OL TO FAN IN
U0	2C0B3-N3	6-173		CHL 6 NOT(CLEAR 0 REG LOWER)
U1	2C0B3-S1	6-173		CHL 6 ENABLE OL TRANSMISSION
U2	2A4A11J03C-05			CHL 6 EXTERNAL PARITY BIT 1
U3	2A4A11J03C-06			
V0	2C0B4-R0	6-193	2C0B4-AT	NOT(BIT 05) CHL 6 OL TO FAN IN
V1	2C0B4-D0	6-193	2C0B4-AS	NOT(BIT 04) CHL 6 OL TO FAN IN
V2	2A4A11J04C-05			CHL 6 EXTERNAL PARITY BIT 1
V3	2A4A11J04C-06			
W0	2A4A11J03R-02			
W1	2A4A11J03R-01			CHANNEL 6 EXTERNAL DATA BIT 05
W2	2A4A11J03C-04			
W3	2A4A11J03C-03			CHANNEL 6 EXTERNAL DATA BIT 11
X0	2A4A11J04B-02			
X1	2A4A11J04R-01			CHANNEL 6 EXTERNAL DATA BIT 05
X2	2A4A11J04C-04			
X3	2A4A11J04C-03			CHANNEL 6 EXTERNAL DATA BIT 11



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

CHANNEL 6-ØL

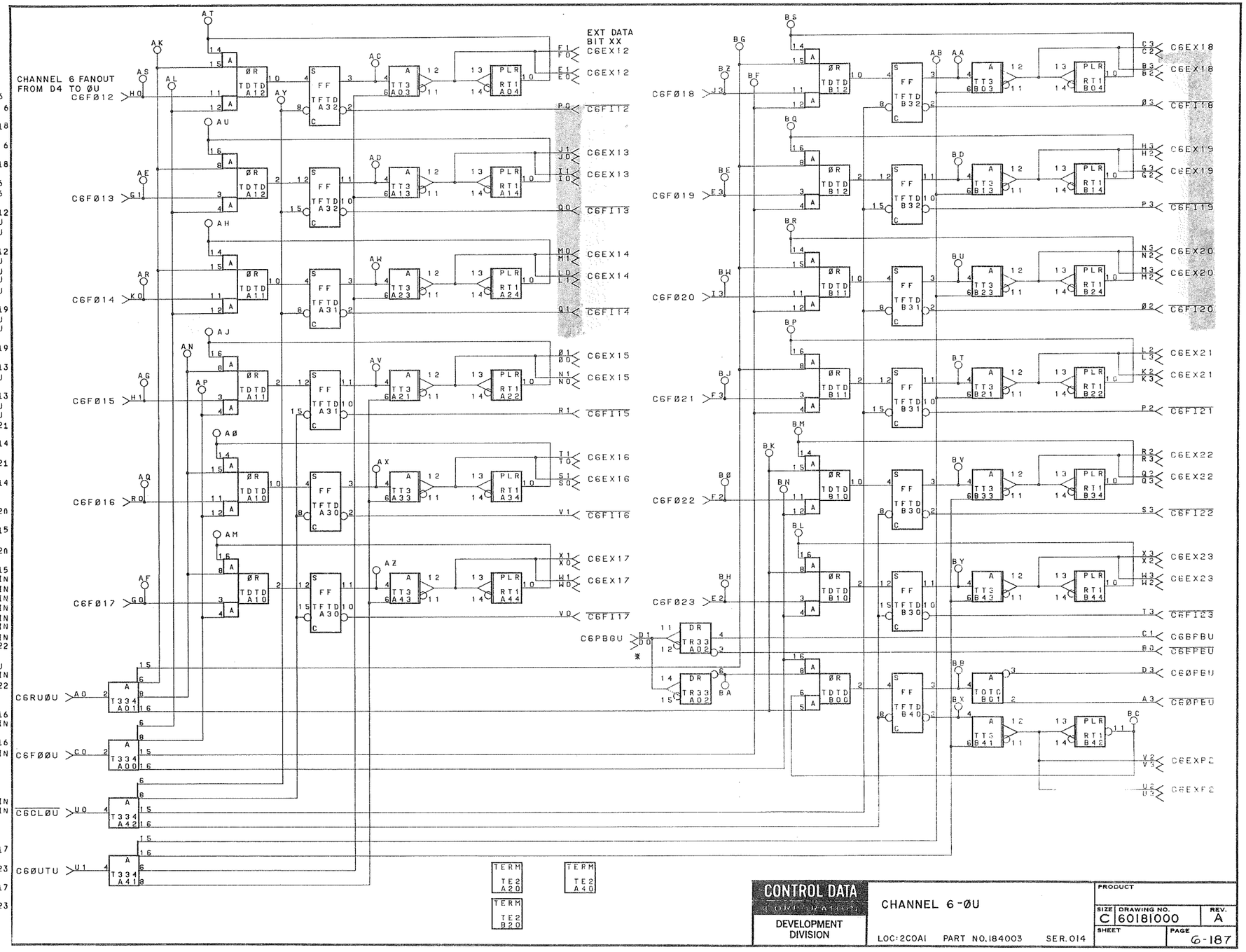
LOC: 2C0B1 PART NO. 184003 SER 006

PRODUCT

SIZE	DRAWING NO.	REV.
C	60181000	A

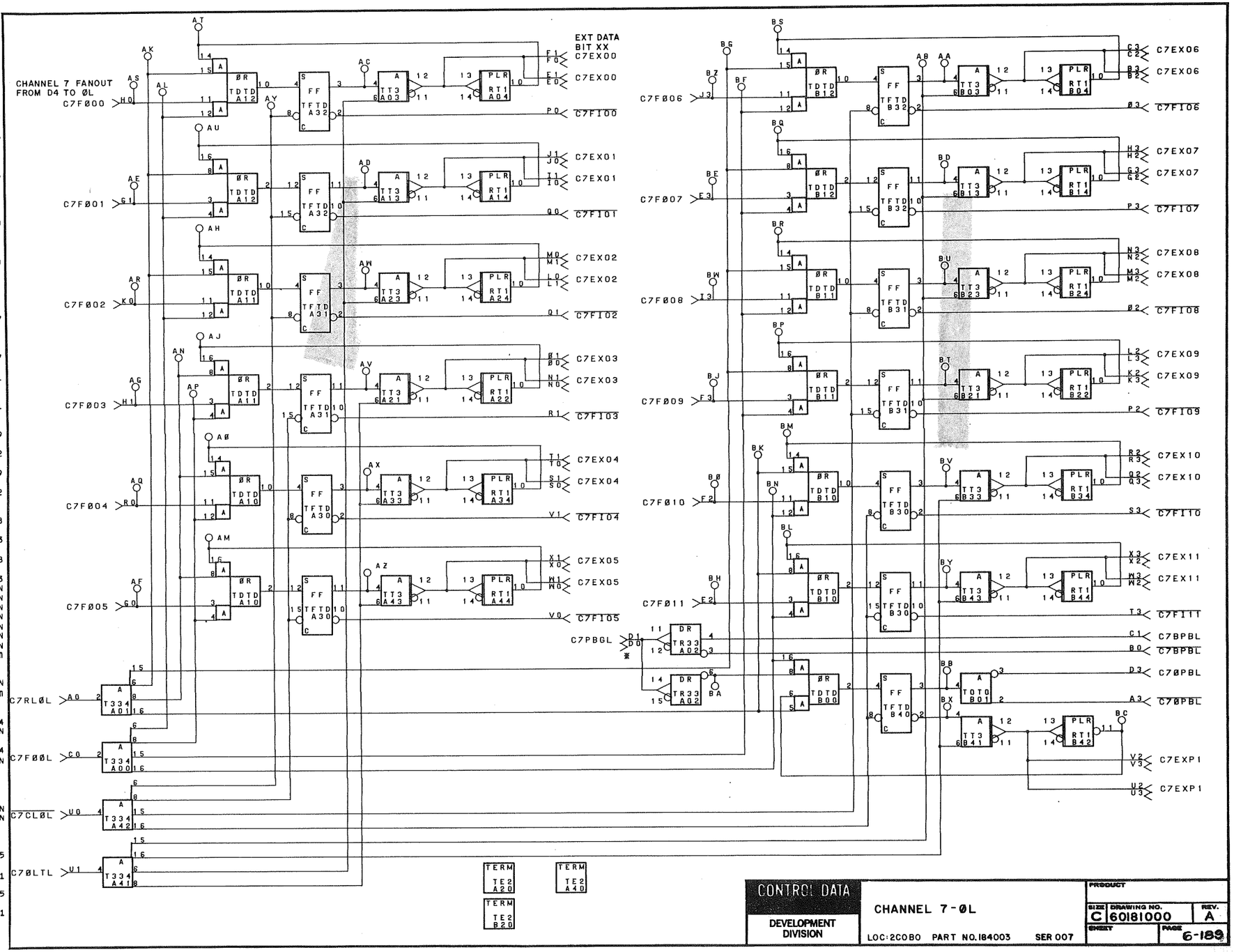
SHEET | PAGE 6-185

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C0B3-V1	6-173		CHAN 6 EXT RCVR TO 0 UPPER
A3	2C0B3-P1	6-173		NOT(0U PARITY RECEIVED) CHL 6
B0	2C0B3-N0	6-173		NOT(0U PARITY GENERATED) CHL 6
B2	2A4A11J01B-04			
B3	2A4A11J01B-03			CHANNEL 6 EXTERNAL DATA BIT 18
C0	2C0B3-03	6-173		CHL 6 D4 FAN OUT TO 0U REG
C1	2C0B3-00	6-173		0 UPPER PARITY GENERATED CHL 6
C2	2A4A11J02B-04			
C3	2A4A11J02B-03			CHANNEL 6 EXTERNAL DATA BIT 18
D0	2B1A0-H2	6- 5		
D1	2B1A0-H3	6- 5		NOT UPPER PARITY BIT TO CHL 6
D3	2C0B3-01	6-173		0 UPPER PARITY RECEIVED CHL 6
E0	2A4A11J01A-02			
E1	2A4A11J01A-01			CHANNEL 6 EXTERNAL DATA BIT 12
E2	2C0A3-V2	6-165	2C0A1-RH	CHL 6 FAN OUT BIT 23 D4 TO 0U
E3	2C0A3-M1	6-165	2C0A1-RE	CHL 6 FAN OUT BIT 19 D4 TO 0U
F0	2A4A11J02A-02			
F1	2A4A11J02A-01			CHANNEL 6 EXTERNAL DATA BIT 12
F2	2C0A6-M1	6-163	2C0A1-RO	CHL 6 FAN OUT BIT 22 D4 TO 0U
F3	2C0A7-M1	6-161	2C0A1-RJ	CHL 6 FAN OUT BIT 21 D4 TO 0U
G0	2C0A7-F1	6-161	2C0A1-AF	CHL 6 FAN OUT BIT 17 D4 TO 0U
G1	2C0A7-V2	6-161	2C0A1-AE	CHL 6 FAN OUT BIT 13 D4 TO 0U
G2	2A4A11J01B-06			
G3	2A4A11J01B-05			CHANNEL 6 EXTERNAL DATA BIT 19
H0	2C0R7-X3	6-169	2C0A1-AS	CHL 6 FAN OUT BIT 12 D4 TO 0U
H1	2C0A3-F1	6-165	2C0A1-AG	CHL 6 FAN OUT BIT 15 D4 TO 0U
H2	2A4A11J02B-06			
H3	2A4A11J02B-05			CHANNEL 6 EXTERNAL DATA BIT 19
I0	2A4A11J01A-04			
I1	2A4A11J01A-03			CHANNEL 6 EXTERNAL DATA BIT 13
I3	2C0A2-M1	6-167	2C0A1-RW	CHL 6 FAN OUT BIT 20 D4 TO 0U
J0	2A4A11J02A-04			
J1	2A4A11J02A-03			CHANNEL 6 EXTERNAL DATA BIT 13
J3	2C0A6-F1	6-163	2C0A1-RZ	CHL 6 FAN OUT BIT 18 D4 TO 0U
K0	2C0A6-V2	6-163	2C0A1-AR	CHL 6 FAN OUT BIT 14 D4 TO 0U
K2	2A4A11J01B-09			CHANNEL 6 EXTERNAL DATA BIT 21
K3	2A4A11J01R-10			
L0	2A4A11J02A-05			CHANNEL 6 EXTERNAL DATA BIT 14
L1	2A4A11J02A-06			
L2	2A4A11J02R-09			CHANNEL 6 EXTERNAL DATA BIT 21
L3	2A4A11J02B-10			
M0	2A4A11J01A-05			CHANNEL 6 EXTERNAL DATA BIT 14
M1	2A4A11J01A-06			
M2	2A4A11J01B-08			
M3	2A4A11J01B-07			CHANNEL 6 EXTERNAL DATA BIT 20
N0	2A4A11J01A-08			
N1	2A4A11J01A-07			CHANNEL 6 EXTERNAL DATA BIT 15
N2	2A4A11J02B-08			
N3	2A4A11J02B-07			CHANNEL 6 EXTERNAL DATA BIT 20
O0	2A4A11J02A-08			
O1	2A4A11J02A-07			CHANNEL 6 EXTERNAL DATA BIT 15
O2	2C0A5-U3	6-195	2C0A5-RT	NOT(BIT 20) CHL 6 0U TO FAN IN
O3	2C0A5-R2	6-195	2C0A5-RQ	NOT(BIT 18) CHL 6 0U TO FAN IN
P0	2C0A5-P0	6-195	2C0A5-AQ	NOT(BIT 12) CHL 6 0U TO FAN IN
P2	2C0A5-T3	6-195	2C0A5-RS	NOT(BIT 21) CHL 6 0U TO FAN IN
P3	2C0A5-S3	6-195	2C0A5-RR	NOT(BIT 19) CHL 6 0U TO FAN IN
Q0	2C0A5-01	6-195	2C0A5-AP	NOT(BIT 13) CHL 6 0U TO FAN IN
Q1	2C0A5-P1	6-195	2C0A5-AR	NOT(BIT 14) CHL 6 0U TO FAN IN
Q2	2A4A11J01C-01			CHANNEL 6 EXTERNAL DATA BIT 22
Q3	2A4A11J01C-02			
R0	2C0A2-V2	6-167	2C0A1-AQ	CHL 6 FAN OUT BIT 16 D4 TO 0U
R1	2C0A5-00	6-195	2C0A5-AO	NOT(BIT 15) CHL 6 0U TO FAN IN
R2	2A4A11J02C-01			CHANNEL 6 EXTERNAL DATA BIT 22
R3	2A4A11J02C-02			
S0	2A4A11J01A-10			
S1	2A4A11J01A-09			CHANNEL 6 EXTERNAL DATA BIT 16
S3	2C0A5-R3	6-195	2C0A5-RP	NOT(BIT 22) CHL 6 0U TO FAN IN
T0	2A4A11J02A-10			
T1	2A4A11J02A-09			CHANNEL 6 EXTERNAL DATA BIT 16
T3	2C0A5-02	6-195	2C0A5-RO	NOT(BIT 23) CHL 6 0U TO FAN IN
U0	2C0B3-T2	6-173		CHL 6 NOT(CLEAR 0 REG UPPER)
U1	2C0B3-S0	6-173		CHL 6 ENABLE 0U TRANSMISSION
U2	2A4A11J01C-05			CHL 6 EXTERNAL PARITY BIT 2
U3	2A4A11J01C-06			
V0	2C0A5-R0	6-195	2C0A5-AT	NOT(BIT 17) CHL 6 0U TO FAN IN
V1	2C0A5-00	6-195	2C0A5-AS	NOT(BIT 16) CHL 6 0U TO FAN IN
V2	2A4A11J02C-05			CHL 6 EXTERNAL PARITY BIT 2
V3	2A4A11J02C-06			
W0	2A4A11J01R-02			
W1	2A4A11J01R-01			CHANNEL 6 EXTERNAL DATA BIT 17
W2	2A4A11J01C-04			
W3	2A4A11J01C-03			CHANNEL 6 EXTERNAL DATA BIT 23
X0	2A4A11J02B-02			
X1	2A4A11J02R-01			CHANNEL 6 EXTERNAL DATA BIT 17
X2	2A4A11J02C-04			
X3	2A4A11J02C-03			CHANNEL 6 EXTERNAL DATA BIT 23



CONTROL DATA	CHANNEL 6-0U	PRODUCT
DEVELOPMENT DIVISION	LOC:2C0A1 PART NO.184003 SER.014	SIZE C DRAWING NO. 60181000 REV. A; SHEET; PAGE 6-187

PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C0B2=U1	6=175		CHAN 7 EXT RCVR TO 0 LOWER
A3	2C0B2=P0	6=175		NOT(0L PARITY RECEIVED) CHL 7
B0	2C0B2=L1	6=175		NOT(0L PARITY GENERATED) CHL 7
B2	2A4A12J03B=04			
B3	2A4A12J03B=03			CHANNEL 7 EXTERNAL DATA BIT 06
C0	2C0B2=S2	6=175		CHL 7 D4 FAN OUT TO 0L REG
C1	2C0B2=L0	6=175		0 LOWER PARITY GENERATED CH 7
C2	2A4A12J04B=04			
C3	2A4A12J04B=03			CHANNEL 7 EXTERNAL DATA BIT 06
D0	2B1B0=I2	6= 7		
D1	2B1B0=I3	6= 7		NOT LOW PARITY BIT TO CHL 7
D3	2C0B2=M1	6=175		0 LOWER PARITY RECEIVED CHL 7
E0	2A4A12J03A=02			
E1	2A4A12J03A=01			CHANNEL 7 EXTERNAL DATA BIT 00
E2	2C0B2=D3	6=175	2C0B0=BH	CHL 7 FAN OUT BIT 11 D4 TO 0L
E3	2C0B2=R2	6=175	2C0B0=BE	CHL 7 FAN OUT BIT 07 D4 TO 0L
F0	2A4A12J04A=02			
F1	2A4A12J04A=01			CHANNEL 7 EXTERNAL DATA BIT 00
F2	2C0B3=D3	6=173	2C0B0=BD	CHL 7 FAN OUT BIT 10 D4 TO 0L
F3	2C0B6=D3	6=171	2C0B0=BJ	CHL 7 FAN OUT BIT 09 D4 TO 0L
G0	2C0B6=R2	6=171	2C0B0=AF	CHL 7 FAN OUT BIT 05 D4 TO 0L
G1	2C0B6=E0	6=171	2C0B0=AE	CHL 7 FAN OUT BIT 01 D4 TO 0L
G2	2A4A12J03B=06			
G3	2A4A12J03B=05			CHANNEL 7 EXTERNAL DATA BIT 07
H0	2C0B7=E0	6=169	2C0B0=AS	CHL 7 FAN OUT BIT 00 D4 TO 0L
H1	2C0B2=E0	6=175	2C0B0=AG	CHL 7 FAN OUT BIT 03 D4 TO 0L
H2	2A4A12J04B=06			
H3	2A4A12J04B=05			CHANNEL 7 EXTERNAL DATA BIT 07
I0	2A4A12J03A=04			
I1	2A4A12J03A=03			CHANNEL 7 EXTERNAL DATA BIT 01
I3	2C0B7=D3	6=169	2C0B0=BW	CHL 7 FAN OUT BIT 08 D4 TO 0L
J0	2A4A12J04A=04			
J1	2A4A12J04A=03			CHANNEL 7 EXTERNAL DATA BIT 01
J3	2C0B3=R2	6=173	2C0B0=BZ	CHL 7 FAN OUT BIT 06 D4 TO 0L
K0	2C0B3=E0	6=173	2C0B0=AR	CHL 7 FAN OUT BIT 02 D4 TO 0L
K2	2A4A12J03B=09			CHANNEL 7 EXTERNAL DATA BIT 09
K3	2A4A12J03B=10			
L0	2A4A12J04A=05			CHANNEL 7 EXTERNAL DATA BIT 02
L1	2A4A12J04A=06			
L2	2A4A12J04B=09			CHANNEL 7 EXTERNAL DATA BIT 09
L3	2A4A12J04B=10			
M0	2A4A12J03A=05			CHANNEL 7 EXTERNAL DATA BIT 02
M1	2A4A12J03A=06			
M2	2A4A12J03B=08			
M3	2A4A12J03B=07			CHANNEL 7 EXTERNAL DATA BIT 08
N0	2A4A12J03A=08			
N1	2A4A12J03A=07			CHANNEL 7 EXTERNAL DATA BIT 03
N2	2A4A12J04B=08			
N3	2A4A12J04B=07			CHANNEL 7 EXTERNAL DATA BIT 08
O0	2A4A12J04A=08			
O1	2A4A12J04A=07			CHANNEL 7 EXTERNAL DATA BIT 03
O2	2C0B4=W3	6=193	2C0B4=BW	NOT(BIT 08) CHL 7 0L TO FAN IN
O3	2C0B4=X2	6=193	2C0B4=BZ	NOT(BIT 06) CHL 7 0L TO FAN IN
P0	2C0B4=S1	6=193	2C0B4=AW	NOT(BIT 00) CHL 7 0L TO FAN IN
P2	2C0B4=W2	6=193	2C0B4=BX	NOT(BIT 09) CHL 7 0L TO FAN IN
P3	2C0B4=X3	6=193	2C0B4=BY	NOT(BIT 07) CHL 7 0L TO FAN IN
Q0	2C0B4=S0	6=193	2C0B4=AV	NOT(BIT 01) CHL 7 0L TO FAN IN
Q1	2C0B4=X1	6=193	2C0B4=AZ	NOT(BIT 02) CHL 7 0L TO FAN IN
Q2	2A4A12J03C=01			CHANNEL 7 EXTERNAL DATA BIT 10
Q3	2A4A12J03C=02			
R0	2C0B7=R2	6=169	2C0B0=AQ	CHL 7 FAN OUT BIT 04 D4 TO 0L
R1	2C0B4=R1	6=193	2C0B4=AU	NOT(BIT 03) CHL 7 0L TO FAN IN
R2	2A4A12J04C=01			CHANNEL 7 EXTERNAL DATA BIT 10
R3	2A4A12J04C=02			
S0	2A4A12J03A=10			
S1	2A4A12J03A=09			CHANNEL 7 EXTERNAL DATA BIT 04
S3	2C0B4=V2	6=193	2C0B4=BV	NOT(BIT 10) CHL 7 0L TO FAN IN
T0	2A4A12J04A=10			
T1	2A4A12J04A=09			CHANNEL 7 EXTERNAL DATA BIT 04
T3	2C0B4=V3	6=193	2C0B4=BU	NOT(BIT 11) CHL 7 0L TO FAN IN
U0	2C0B2=N3	6=175		CHL 7 NOT(CLEAR 0 REG LOWER)
U1	2C0B2=S1	6=175		CHL 7 ENABLE 0L TRANSMISSION
U2	2A4A12J03C=05			CHL 7 EXTERNAL PARITY BIT 1
U3	2A4A12J03C=06			
V0	2C0B4=X0	6=193	2C0B4=AY	NOT(BIT 05) CHL 7 0L TO FAN IN
V1	2C0B4=W0	6=193	2C0B4=AX	NOT(BIT 04) CHL 7 0L TO FAN IN
V2	2A4A12J04C=05			CHL 7 EXTERNAL PARITY BIT 1
V3	2A4A12J04C=06			
W0	2A4A12J03B=02			
W1	2A4A12J03B=01			CHANNEL 7 EXTERNAL DATA BIT 05
W2	2A4A12J03C=04			
W3	2A4A12J03C=03			CHANNEL 7 EXTERNAL DATA BIT 11
X0	2A4A12J04B=02			
X1	2A4A12J04B=01			CHANNEL 7 EXTERNAL DATA BIT 05
X2	2A4A12J04C=04			
X3	2A4A12J04C=03			CHANNEL 7 EXTERNAL DATA BIT 11



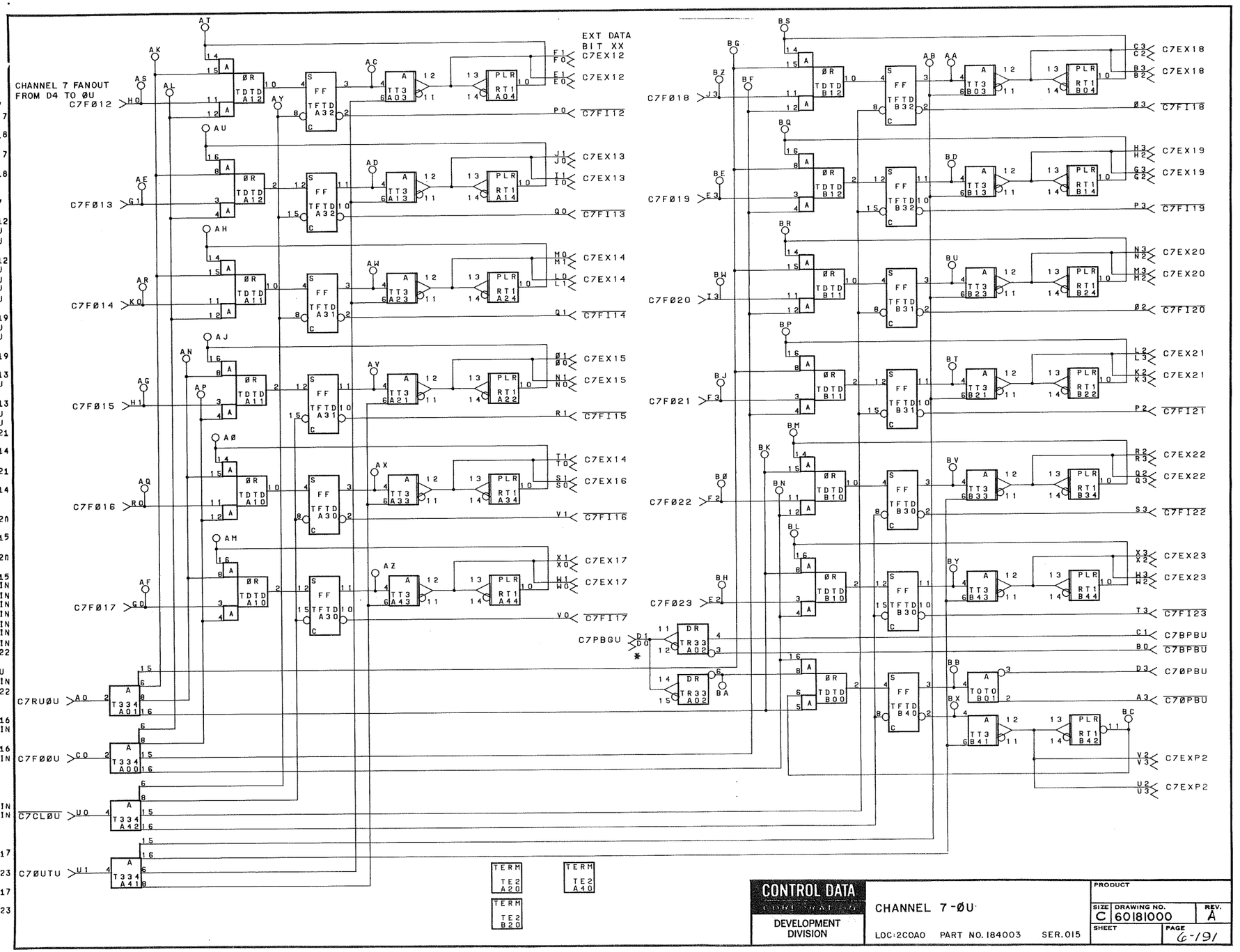
CONTROL DATA
DEVELOPMENT DIVISION

CHANNEL 7-0L

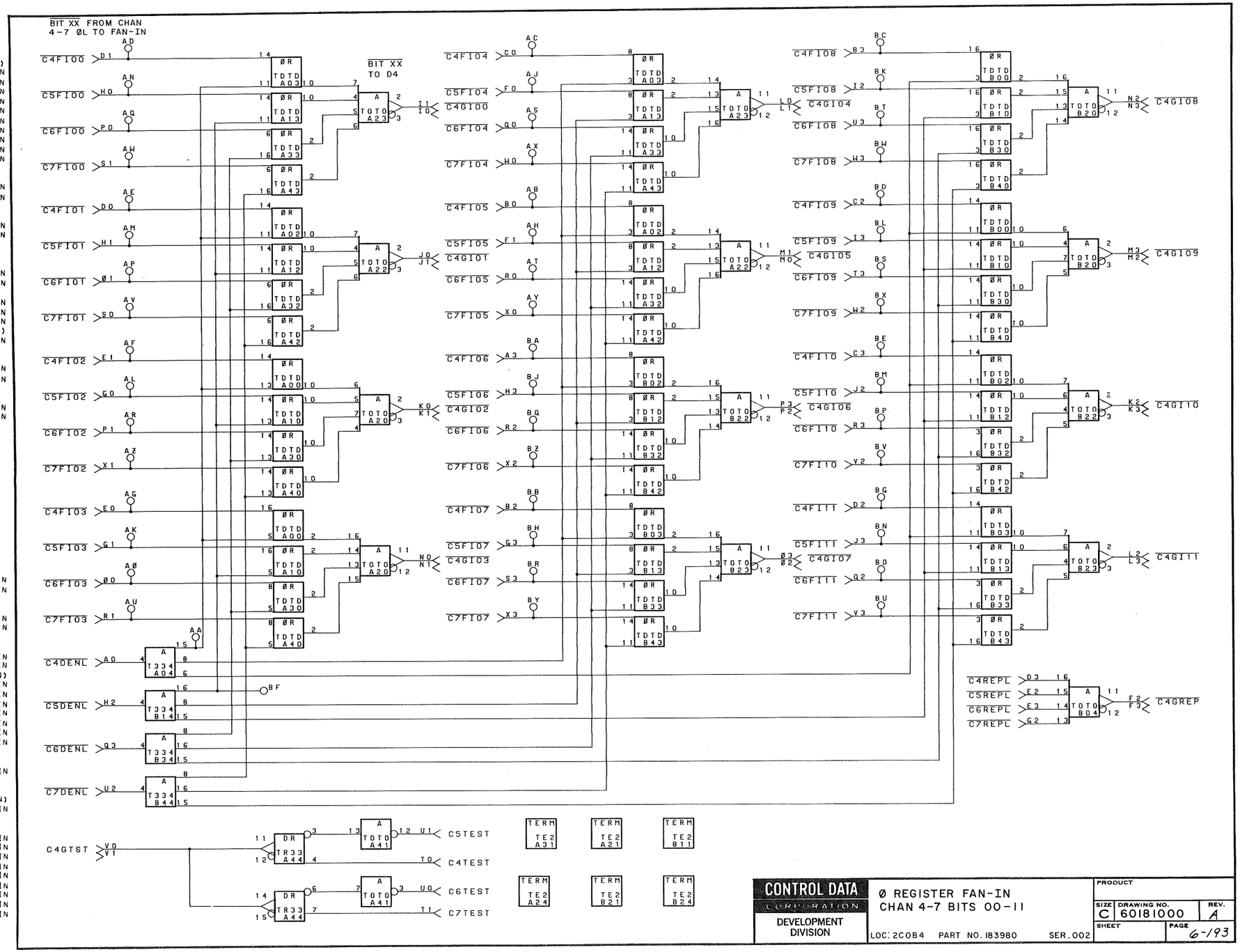
LOC:2C0B0 PART NO.184003 SER 007

PRODUCT
SIZE C | DRAWING NO. 60181000 | REV. A
SHEET | PAGE 6-189

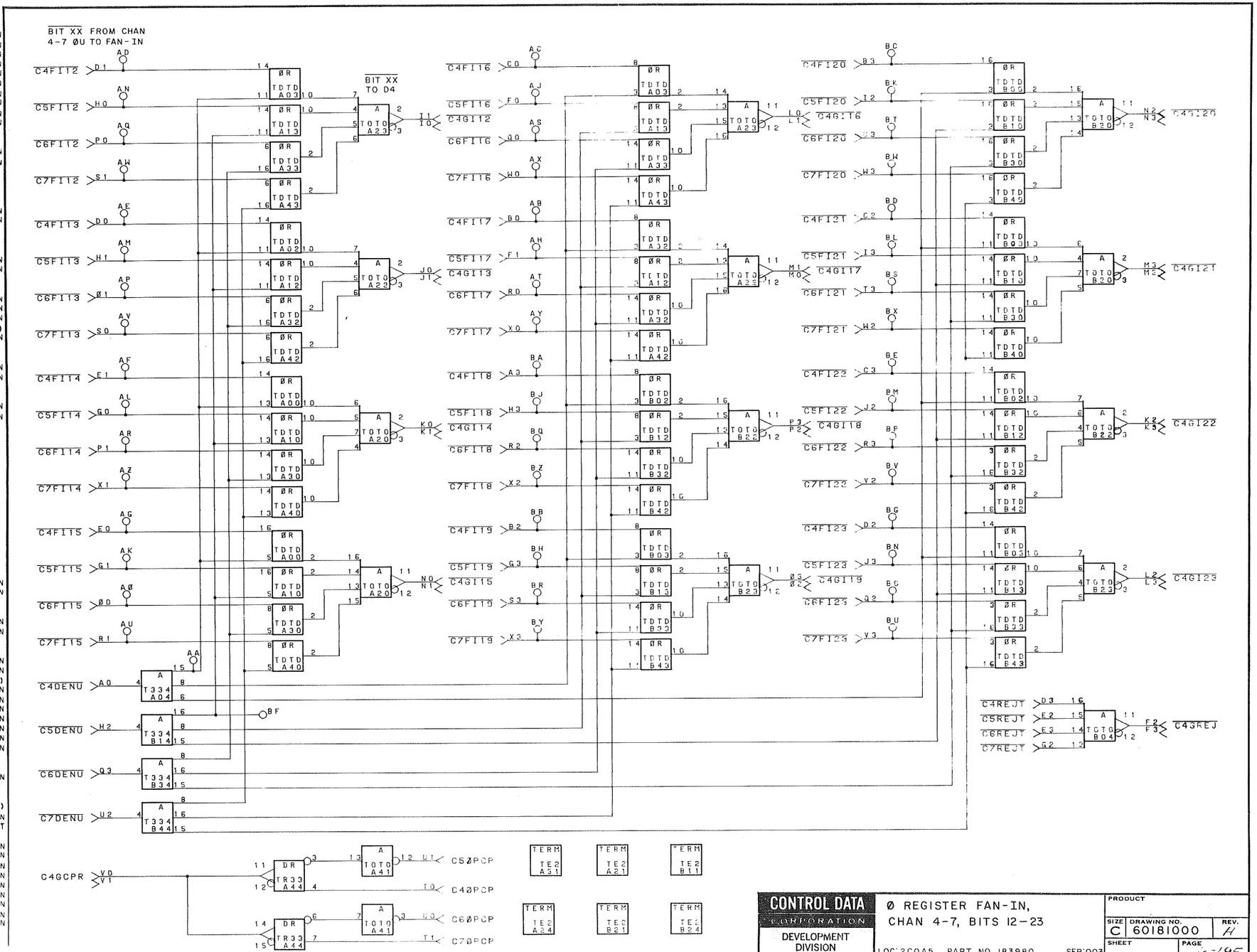
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C0B2-V1	6-175		CHAN 7 EXT RCVR TO 0 UPPER
A3	2C0B2-P1	6-175		NOT(0U PARITY RECEIVED) CHL 7
B0	2C0B2-N0	6-175		NOT(0U PARITY GENERATED) CHL 7
B2	2A4A12J01B-04			
B3	2A4A12J01B-03			CHANNEL 7 EXTERNAL DATA BIT 18
C0	2C0B2-03	6-175		CHL 7 D4 FAN OUT TO 0U REG
C1	2C0B2-00	6-175		0 UPPER PARITY GENERATED CHL 7
C2	2A4A12J02B-04			
C3	2A4A12J02B-03			CHANNEL 7 EXTERNAL DATA BIT 18
D0	2B1A0-I2	6- 5		
D1	2B1A0-I3	6- 5		NOT UP, PAR, BIT TO CHAN 7
D3	2C0B2-01	6-175		0 UPPER PARITY RECEIVED CHL 7
E0	2A4A12J01A-02			
E1	2A4A12J01A-01			CHANNEL 7 EXTERNAL DATA BIT 12
E2	2C0A3-V3	6-165	2C0A0-RH	CHL 7 FAN OUT BIT 23 D4 TO 0U
E3	2C0A3-M0	6-165	2C0A0-RE	CHL 7 FAN OUT BIT 19 D4 TO 0U
F0	2A4A12J02A-02			
F1	2A4A12J02A-01			CHANNEL 7 EXTERNAL DATA BIT 12
F2	2C0A6-M0	6-163	2C0A0-RO	CHL 7 FAN OUT BIT 22 D4 TO 0U
F3	2C0A7-M0	6-161	2C0A0-RJ	CHL 7 FAN OUT BIT 21 D4 TO 0U
G0	2C0A7-F0	6-161	2C0A0-AF	CHL 7 FAN OUT BIT 17 D4 TO 0U
G1	2C0A7-V3	6-161	2C0A0-AE	CHL 7 FAN OUT BIT 13 D4 TO 0U
G2	2A4A12J01B-06			
G3	2A4A12J01B-05			CHANNEL 7 EXTERNAL DATA BIT 19
H0	2C0B7-X2	6-169	2C0A0-AS	CHL 7 FAN OUT BIT 12 D4 TO 0U
H1	2C0A3-F0	6-165	2C0A0-AG	CHL 7 FAN OUT BIT 15 D4 TO 0U
H2	2A4A12J02B-06			
H3	2A4A12J02B-05			CHANNEL 7 EXTERNAL DATA BIT 19
I0	2A4A12J01A-04			
I1	2A4A12J01A-03			CHANNEL 7 EXTERNAL DATA BIT 13
I3	2C0A2-M0	6-167	2C0A0-BW	CHL 7 FAN OUT BIT 20 D4 TO 0U
J0	2A4A12J02A-04			
J1	2A4A12J02A-03			CHANNEL 7 EXTERNAL DATA BIT 13
J3	2C0A6-F0	6-163	2C0A0-BZ	CHL 7 FAN OUT BIT 18 D4 TO 0U
K0	2C0A6-V3	6-163	2C0A0-AR	CHL 7 FAN OUT BIT 14 D4 TO 0U
K2	2A4A12J01B-09			CHANNEL 7 EXTERNAL DATA BIT 21
K3	2A4A12J01B-10			
L0	2A4A12J02A-05			CHANNEL 7 EXTERNAL DATA BIT 14
L1	2A4A12J02A-06			
L2	2A4A12J02B-09			CHANNEL 7 EXTERNAL DATA BIT 21
L3	2A4A12J02B-10			
M0	2A4A12J01A-05			CHANNEL 7 EXTERNAL DATA BIT 14
M1	2A4A12J01A-06			
M2	2A4A12J01B-08			
M3	2A4A12J01B-07			CHANNEL 7 EXTERNAL DATA BIT 20
N0	2A4A12J01A-08			
N1	2A4A12J01A-07			CHANNEL 7 EXTERNAL DATA BIT 15
N2	2A4A12J02B-08			
N3	2A4A12J02B-07			CHANNEL 7 EXTERNAL DATA BIT 20
O0	2A4A12J02A-08			
O1	2A4A12J02A-07			CHANNEL 7 EXTERNAL DATA BIT 15
O2	2C0A5-W3	6-195	2C0A5-RW	NOT(BIT 20) CHL 7 OU TO FAN IN
O3	2C0A5-X2	6-195	2C0A5-BZ	NOT(BIT 18) CHL 7 OU TO FAN IN
P0	2C0A5-S1	6-195	2C0A5-AW	NOT(BIT 12) CHL 7 OU TO FAN IN
P2	2C0A5-W2	6-195	2C0A5-RX	NOT(BIT 21) CHL 7 OU TO FAN IN
P3	2C0A5-X3	6-195	2C0A5-RY	NOT(BIT 19) CHL 7 OU TO FAN IN
Q0	2C0A5-S0	6-195	2C0A5-AV	NOT(BIT 13) CHL 7 OU TO FAN IN
Q1	2C0A5-X1	6-195	2C0A5-AZ	NOT(BIT 14) CHL 7 OU TO FAN IN
Q2	2A4A12J01C-01			CHANNEL 7 EXTERNAL DATA BIT 22
Q3	2A4A12J01C-02			
R0	2C0A2-V3	6-167	2C0A0-AQ	CHL 7 FAN OUT BIT 16 D4 TO 0U
R1	2C0A5-R1	6-195	2C0A5-AU	NOT(BIT 15) CHL 7 OU TO FAN IN
R2	2A4A12J02C-01			CHANNEL 7 EXTERNAL DATA BIT 22
R3	2A4A12J02C-02			
S0	2A4A12J01A-10			
S1	2A4A12J01A-09			CHANNEL 7 EXTERNAL DATA BIT 16
S3	2C0A5-V2	6-195	2C0A5-RV	NOT(BIT 22) CHL 7 OU TO FAN IN
T0	2A4A12J02A-10			
T1	2A4A12J02A-09			CHANNEL 7 EXTERNAL DATA BIT 16
T3	2C0A5-V3	6-195	2C0A5-RU	NOT(BIT 23) CHL 7 OU TO FAN IN
U0	2C0B2-T2	6-175		CHL 7 NOT(CLEAR 0 REG UPPER)
U1	2C0B2-S0	6-175		CHL 7 ENABLE 0U TRANSMISSION
U2	2A4A12J01C-05			CHL 7 EXTERNAL PARITY BIT 2
U3	2A4A12J01C-06			
V0	2C0A5-X0	6-195	2C0A5-AY	NOT(BIT 17) CHL 7 OU TO FAN IN
V1	2C0A5-W0	6-195	2C0A5-AX	NOT(BIT 16) CHL 7 OU TO FAN IN
V2	2A4A12J02C-05			CHL 7 EXTERNAL PARITY BIT 2
V3	2A4A12J02C-06			
W0	2A4A12J01A-02			
W1	2A4A12J01B-01			CHANNEL 7 EXTERNAL DATA BIT 17
W2	2A4A12J01C-04			
W3	2A4A12J01C-03			CHANNEL 7 EXTERNAL DATA BIT 23
X0	2A4A12J02B-02			
X1	2A4A12J02B-01			CHANNEL 7 EXTERNAL DATA BIT 17
X2	2A4A12J02C-04			
X3	2A4A12J02C-03			CHANNEL 7 EXTERNAL DATA BIT 23



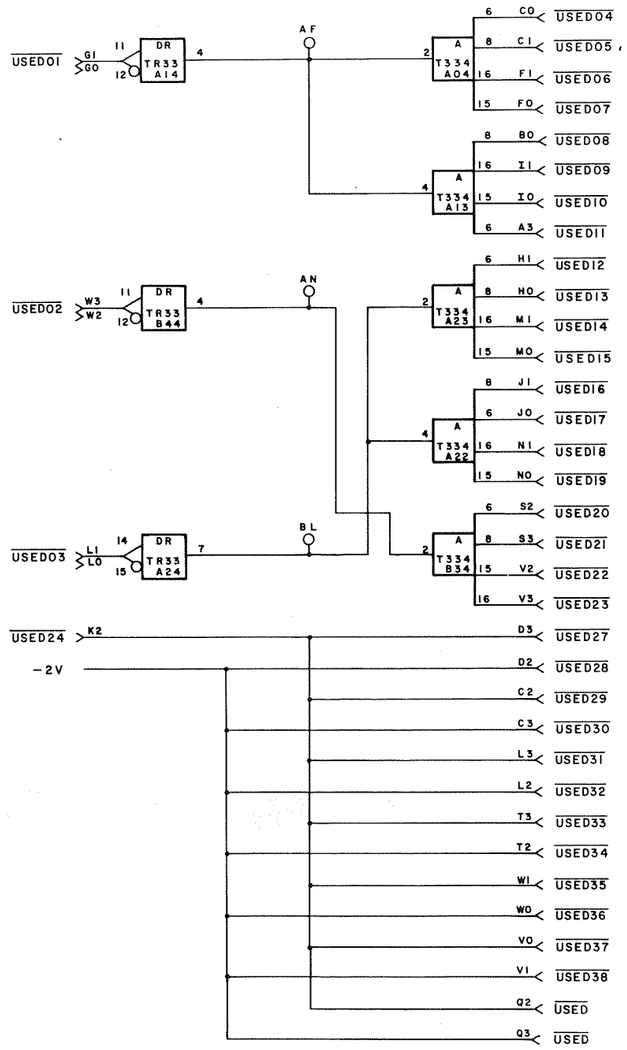
PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C0B7-F0	6-169		CHL 4 NOT(ENABLE OL TO FAN IN)
A3	2C0B9-O3	6-177	2C0B4-RA	NOT(BIT 06) CHL 4 OL TO FAN IN
B0	2C0B9-V0	6-177	2C0B4-AB	NOT(BIT 05) CHL 4 OL TO FAN IN
B2	2C0B9-P3	6-177	2C0B4-BR	NOT(BIT 07) CHL 4 OL TO FAN IN
B3	2C0B9-O2	6-177	2C0B4-BC	NOT(BIT 08) CHL 4 OL TO FAN IN
C0	2C0B9-V1	6-177	2C0B4-AC	NOT(BIT 04) CHL 4 OL TO FAN IN
C2	2C0B9-P2	6-177	2C0B4-BD	NOT(BIT 09) CHL 4 OL TO FAN IN
C3	2C0B9-S3	6-177	2C0B4-BE	NOT(BIT 10) CHL 4 OL TO FAN IN
D0	2C0B9-Q0	6-177	2C0B4-AE	NOT(BIT 01) CHL 4 OL TO FAN IN
D1	2C0B9-P0	6-177	2C0B4-AD	NOT(BIT 00) CHL 4 OL TO FAN IN
D2	2C0B9-T3	6-177	2C0B4-BG	NOT(BIT 11) CHL 4 OL TO FAN IN
D3	2C0A7-O3	6-161		CHAN 4 NOT (REPLY ON CONN + FCN)
E0	2C0B9-R1	6-177	2C0B4-AG	NOT(BIT 03) CHL 4 OL TO FAN IN
E1	2C0B9-Q1	6-177	2C0B4-AF	NOT(BIT 02) CHL 4 OL TO FAN IN
E2	2C0A6-O3	6-163		CHL 5 NOT(REPLY ON CONN/FUNC)
E3	2C0A3-O3	6-165		CHL 6 NOT(REPLY ON CONN/FUNC)
F0	2C0B8-V1	6-181	2C0B4-AJ	NOT(BIT 04) CHL 5 OL TO FAN IN
F1	2C0B8-V0	6-181	2C0B4-AH	NOT(BIT 05) CHL 5 OL TO FAN IN
F2	2B1B1-K2	6- 9		
F3	2B1B1-K3	6- 9		NOT CHL 4-7 CONN + FCN REPLY FAN-IN
G0	2C0B8-Q1	6-181	2C0B4-AL	NOT(BIT 02) CHL 5 OL TO FAN IN
G1	2C0B8-R1	6-181	2C0B4-AK	NOT(BIT 03) CHL 5 OL TO FAN IN
G2	2C0A2-O3	6-167		CHL 7 NOT(REPLY ON CONN/FUNC)
G3	2C0B8-P3	6-181	2C0B4-RH	NOT(BIT 07) CHL 5 OL TO FAN IN
H0	2C0B8-P0	6-181	2C0B4-AN	NOT(BIT 00) CHL 5 OL TO FAN IN
H1	2C0B8-Q0	6-181	2C0B4-AM	NOT(BIT 01) CHL 5 OL TO FAN IN
H2	2C0B6-F0	6-171		CHL 5 NOT(ENABLE OL TO FAN IN)
H3	2C0B8-O3	6-181	2C0B4-RJ	NOT(BIT 06) CHL 5 OL TO FAN IN
I0	2B1B4-R1	6- 29		NOT CHL 4-7 BIT 00 F1 TO D4
I1	2B1B4-R0	6- 29		
I2	2C0B8-O2	6-181	2C0B4-PK	NOT(BIT 08) CHL 5 OL TO FAN IN
I3	2C0B8-P2	6-181	2C0B4-RL	NOT(BIT 09) CHL 5 OL TO FAN IN
J0	2B1B3-R0	6- 31		
J1	2B1B3-R1	6- 31		NOT CHL 4-7 BIT 01 F1 TO D4
J2	2C0B8-S3	6-181	2C0B4-RM	NOT(BIT 10) CHL 5 OL TO FAN IN
J3	2C0B8-T3	6-181	2C0B4-RN	NOT(BIT 11) CHL 5 OL TO FAN IN
K0	2B1B2-R0	6- 33		
K1	2B1B2-R1	6- 33		NOT CHL 4-7 BIT 02 F1 TO D4
K2	2B1A3-M0	6- 37		
K3	2B1A3-M1	6- 37		NOT CHL 4-7 BIT 10 F1 TO D4
L0	2B1A3-R0	6- 37		
L1	2B1A3-R1	6- 37		NOT CHL 4-7 BIT 04 F1 TO D4
L2	2B1A2-M0	6- 39		
L3	2B1A2-M1	6- 39		NOT CHL 4-7 BIT 11 F1 TO D4
M0	2B1A2-R1	6- 39		NOT CHL 4-7 BIT 05 F1 TO D4
M1	2B1A2-R0	6- 39		
M2	2B1A4-M1	6- 35		NOT CHL 4-7 BIT 09 F1 TO D4
M3	2B1A4-M0	6- 35		
N0	2B1A4-R0	6- 35		
N1	2B1A4-R1	6- 35		NOT CHL 4-7 BIT 03 F1 TO D4
N2	2B1B2-M0	6- 33		
N3	2B1B2-M1	6- 33		NOT CHL 4-7 BIT 08 F1 TO D4
O0	2C0B1-R1	6-185	2C0B4-AO	NOT(BIT 03) CHL 6 OL TO FAN IN
O1	2C0B1-Q0	6-185	2C0B4-AP	NOT(BIT 01) CHL 6 OL TO FAN IN
O2	2B1B3-M1	6- 31		NOT CHL 4-7 BIT 07 F1 TO D4
O3	2B1B3-M0	6- 31		
P0	2C0B1-P0	6-185	2C0B4-AQ	NOT(BIT 00) CHL 6 OL TO FAN IN
P1	2C0B1-Q1	6-185	2C0B4-AR	NOT(BIT 02) CHL 6 OL TO FAN IN
P2	2B1B4-M1	6- 29		NOT CHL 4-7 BIT 06 F1 TO D4
P3	2B1B4-M0	6- 29		
Q0	2C0B1-V1	6-185	2C0B4-AS	NOT(BIT 04) CHL 6 OL TO FAN IN
Q2	2C0B1-T3	6-185	2C0B4-RO	NOT(BIT 11) CHL 6 OL TO FAN IN
Q3	2C0B3-F0	6-173		CHL 6 NOT(ENABLE OL TO FAN IN)
R0	2C0B1-V0	6-185	2C0B4-AT	NOT(BIT 05) CHL 6 OL TO FAN IN
R1	2C0B0-R1	6-189	2C0B4-AU	NOT(BIT 03) CHL 7 OL TO FAN IN
R2	2C0B1-O3	6-185	2C0B4-RQ	NOT(BIT 06) CHL 6 OL TO FAN IN
R3	2C0B1-S3	6-185	2C0B4-RP	NOT(BIT 10) CHL 6 OL TO FAN IN
S0	2C0B0-Q0	6-189	2C0B4-AV	NOT(BIT 01) CHL 7 OL TO FAN IN
S1	2C0B0-P0	6-189	2C0B4-AW	NOT(BIT 00) CHL 7 OL TO FAN IN
S3	2C0B1-P3	6-185	2C0B4-RR	NOT(BIT 07) CHL 6 OL TO FAN IN
T0	2C0A7-B1	6-161		CHAN 4 TEST OPR COMPL/PE
T1	2C0A2-B1	6-167		CHAN 7 TEST OPR COMPL/PE
T3	2C0B1-P2	6-185	2C0B4-RS	NOT(BIT 09) CHL 6 OL TO FAN IN
U0	2C0A3-B1	6-165		CHAN 6 TEST OPR COMPL/PE
U1	2C0A6-B1	6-163		CHAN 5 TEST OPR COMPL/PE
U2	2C0B2-F0	6-175		CHL 7 NOT(ENABLE OL TO FAN IN)
U3	2C0B1-O2	6-185	2C0B4-RT	NOT(BIT 08) CHL 6 OL TO FAN IN
V0	2B1A7-P3	6- 1		TEST OPR COMP/PE TO CHAN 4-7
V1	2B1A7-P2	6- 1		
V2	2C0B0-S3	6-189	2C0B4-RV	NOT(BIT 10) CHL 7 OL TO FAN IN
V3	2C0B0-T3	6-189	2C0B4-RU	NOT(BIT 11) CHL 7 OL TO FAN IN
W0	2C0B0-V1	6-189	2C0B4-AX	NOT(BIT 04) CHL 7 OL TO FAN IN
W2	2C0B0-P2	6-189	2C0B4-RX	NOT(BIT 09) CHL 7 OL TO FAN IN
W3	2C0B0-O2	6-189	2C0B4-RW	NOT(BIT 08) CHL 7 OL TO FAN IN
X0	2C0B0-V0	6-189	2C0B4-AY	NOT(BIT 05) CHL 7 OL TO FAN IN
X1	2C0B0-O1	6-189	2C0B4-AZ	NOT(BIT 02) CHL 7 OL TO FAN IN
X2	2C0B0-O3	6-189	2C0B4-RZ	NOT(BIT 06) CHL 7 OL TO FAN IN
X3	2C0B0-P3	6-189	2C0B4-RY	NOT(BIT 07) CHL 7 OL TO FAN IN



PIN	ORIGIN/ DEST.	PAGE	TEST POINT	SIGNAL DEFINITION.
A0	2C0B7-H0	6-169		CHL 4 NOT(ENABLE OU TO FAN IN)
A3	2C0A9-03	6-179	2C0A5-RA	NOT(BIT 18) CHL 4 OU TO FAN IN
B0	2C0A9-V0	6-179	2C0A5-AB	NOT(BIT 17) CHL 4 OU TO FAN IN
B2	2C0A9-P3	6-179	2C0A5-RB	NOT(BIT 19) CHL 4 OU TO FAN IN
B3	2C0A9-02	6-179	2C0A5-RC	NOT(BIT 20) CHL 4 OU TO FAN IN
C0	2C0A9-V1	6-179	2C0A5-AC	NOT(BIT 16) CHL 4 OU TO FAN IN
C2	2C0A9-P2	6-179	2C0A5-RD	NOT(BIT 21) CHL 4 OU TO FAN IN
C3	2C0A9-S3	6-179	2C0A5-RE	NOT(BIT 22) CHL 4 OU TO FAN IN
D0	2C0A9-Q0	6-179	2C0A5-AE	NOT(BIT 13) CHL 4 OU TO FAN IN
D1	2C0A9-P0	6-179	2C0A5-AD	NOT(BIT 12) CHL 4 OU TO FAN IN
D2	2C0A9-T3	6-179	2C0A5-RG	NOT(BIT 23) CHL 4 OU TO FAN IN
D3	2C0A7-B3	6-161		CHAN 4 NOT (EXT REJ ON CONN + FCN)
E0	2C0A9-R1	6-179	2C0A5-AG	NOT(BIT 15) CHL 4 OU TO FAN IN
E1	2C0A9-Q1	6-179	2C0A5-AF	NOT(BIT 14) CHL 4 OU TO FAN IN
E2	2C0A6-B3	6-163		CHAN 5 NOT(EXT REJECT ON CONN + FCN)
E3	2C0A3-B3	6-165		CHAN 6 NOT(EXT REJ ON CONN OR FCN)
F0	2C0A8-V1	6-183	2C0A5-AJ	NOT(BIT 16) CHL 5 OU TO FAN IN
F1	2C0A8-V0	6-183	2C0A5-AH	NOT(BIT 17) CHL 5 OU TO FAN IN
F2	2B1B1-J2	6- 9		
F3	2B1B1-J3	6- 9		NOT CHL 4-7 CONN + FCN EXT REJECT FAN-IN
G0	2C0A8-Q1	6-183	2C0A5-AL	NOT(BIT 14) CHL 5 OU TO FAN IN
G1	2C0A8-R1	6-183	2C0A5-AK	NOT(BIT 15) CHL 5 OU TO FAN IN
G2	2C0A2-B3	6-167		CHAN 7 NOT (EXT REJECT ON CONN + FCN)
G3	2C0A8-P3	6-183	2C0A5-RH	NOT(BIT 19) CHL 5 OU TO FAN IN
H0	2C0A8-P0	6-183	2C0A5-AN	NOT(BIT 12) CHL 5 OU TO FAN IN
H1	2C0A8-Q0	6-183	2C0A5-AM	NOT(BIT 13) CHL 5 OU TO FAN IN
H2	2C0B6-H0	6-171		CHL 5 NOT(ENABLE OU TO FAN IN)
H3	2C0A8-03	6-183	2C0A5-RJ	NOT(BIT 18) CHL 5 OU TO FAN IN
I0	2B1B4-L1	6- 29		NOT CHL 4-7 BIT 12 FI TO D4
I1	2B1B4-L0	6- 29		
I2	2C0A8-02	6-183	2C0A5-RK	NOT(BIT 20) CHL 5 OU TO FAN IN
I3	2C0A8-P2	6-183	2C0A5-RL	NOT(BIT 21) CHL 5 OU TO FAN IN
J0	2B1B3-L0	6- 31		
J1	2B1B3-L1	6- 31		NOT CHL 4-7 BIT 13 FI TO D4
J2	2C0A8-S3	6-183	2C0A5-RM	NOT(BIT 22) CHL 5 OU TO FAN IN
J3	2C0A8-T3	6-183	2C0A5-RN	NOT(BIT 23) CHL 5 OU TO FAN IN
K0	2B1B2-L0	6- 33		
K1	2B1B2-L1	6- 33		NOT CHL 4-7 BIT 14 FI TO D4
K2	2B1A3-W0	6- 37		
K3	2B1A3-W1	6- 37		NOT CHL 4-7 BIT 22 FI TO D4
L0	2B1A3-L0	6- 37		
L1	2B1A3-L1	6- 37		NOT CHL 4-7 BIT 16 FI TO D4
L2	2B1A2-W0	6- 39		
L3	2B1A2-W1	6- 39		NOT CHL 4-7 BIT 23 FI TO D4
M0	2B1A2-L0	6- 39		NOT CHL 4-7 BIT 17 FI TO D4
M1	2B1A2-L1	6- 39		
M2	2B1A4-W1	6- 35		NOT CHL 4-7 BIT 21 FI TO D4
M3	2B1A4-W0	6- 35		
N0	2B1A4-L0	6- 35		
N1	2B1A4-L1	6- 35		NOT CHL 4-7 BIT 15 FI TO D4
N2	2B1B2-W0	6- 33		
N3	2B1B2-W1	6- 33		NOT CHL 4-7 BIT 20 FI TO D4
O0	2C0A1-R1	6-187	2C0A5-AO	NOT(BIT 15) CHL 6 OU TO FAN IN
O1	2C0A1-Q0	6-187	2C0A5-AP	NOT(BIT 13) CHL 6 OU TO FAN IN
O2	2B1B3-W1	6- 31		NOT CHL 4-7 BIT 19 FI TO D4
O3	2B1B3-W0	6- 31		
P0	2C0A1-P0	6-187	2C0A5-AQ	NOT(BIT 12) CHL 6 OU TO FAN IN
P1	2C0A1-01	6-187	2C0A5-AR	NOT(BIT 14) CHL 6 OU TO FAN IN
P2	2B1B4-W1	6- 29		NOT CHL 4-7 BIT 18 FI TO D4
P3	2B1B4-W0	6- 29		
Q0	2C0A1-V1	6-187	2C0A5-AS	NOT(BIT 16) CHL 6 OU TO FAN IN
Q2	2C0A1-T3	6-187	2C0A5-RO	NOT(BIT 23) CHL 6 OU TO FAN IN
Q3	2C0B3-H0	6-173		CHL 6 NOT(ENABLE OU TO FAN IN)
R0	2C0A1-V0	6-187	2C0A5-AT	NOT(BIT 17) CHL 6 OU TO FAN IN
R1	2C0A0-R1	6-191	2C0A5-AU	NOT(BIT 15) CHL 7 OU TO FAN IN
R2	2C0A1-03	6-187	2C0A5-RQ	NOT(BIT 18) CHL 6 OU TO FAN IN
R3	2C0A1-S3	6-187	2C0A5-RP	NOT(BIT 22) CHL 6 OU TO FAN IN
S0	2C0A0-Q0	6-191	2C0A5-AV	NOT(BIT 13) CHL 7 OU TO FAN IN
S1	2C0A0-P0	6-191	2C0A5-AW	NOT(BIT 12) CHL 7 OU TO FAN IN
S3	2C0A1-P3	6-187	2C0A5-RR	NOT(BIT 19) CHL 6 OU TO FAN IN
T0	2C0A7-P3	6-161		CHL 4 OPERATION COMPLETE
T1	2C0A2-P3	6-167		CHL 7 OPERATION COMPLETE
T3	2C0A1-P2	6-187	2C0A5-RS	NOT(BIT 21) CHL 6 OU TO FAN IN
U0	2C0A3-P3	6-165		CHL 6 OPERATION COMPLETE
U1	2C0A6-P3	6-163		CHL 5 OPERATION COMPLETE
U2	2C0B2-H0	6-175		CHL 7 NOT(ENABLE OU TO FAN IN)
U3	2C0A1-02	6-187	2C0A5-RT	NOT(BIT 20) CHL 6 OU TO FAN IN
V0	2A1B4-B2	6- 57		ADDR COMPARE TO CHL 4-7 FANOUT
V1	2A1B4-B3	6- 57		
V2	2C0A0-S3	6-191	2C0A5-RV	NOT(BIT 22) CHL 7 OU TO FAN IN
V3	2C0A0-T3	6-191	2C0A5-RU	NOT(BIT 23) CHL 7 OU TO FAN IN
W0	2C0A0-V1	6-191	2C0A5-AX	NOT(BIT 16) CHL 7 OU TO FAN IN
W2	2C0A0-P2	6-191	2C0A5-RX	NOT(BIT 21) CHL 7 OU TO FAN IN
W3	2C0A0-02	6-191	2C0A5-RW	NOT(BIT 20) CHL 7 OU TO FAN IN
X0	2C0A0-V0	6-191	2C0A5-AY	NOT(BIT 17) CHL 7 OU TO FAN IN
X1	2C0A0-01	6-191	2C0A5-AZ	NOT(BIT 14) CHL 7 OU TO FAN IN
X2	2C0A0-03	6-191	2C0A5-RZ	NOT(BIT 18) CHL 7 OU TO FAN IN
X3	2C0A0-P3	6-191	2C0A5-RY	NOT(BIT 19) CHL 7 OU TO FAN IN



CONTROL DATA CORPORATION	Ø REGISTER FAN-IN, CHAN 4-7, BITS 12-23	PRODUCT
DEVELOPMENT DIVISION	LOC: 2C0A5 PART NO. 183980 SER: 003	SIZE C · DRAWING NO. 60181000 · REV. H · SHEET · PAGE 6-195



NOTES:

1. THIS MODULE REPLACES THE A-CONTROL MODULE(S) OF A CHANNEL(S) NOT PRESENT.
2. LOCATION IS DEPENDENT ON THE CHANNEL(S) THIS MODULE REPLACES.

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

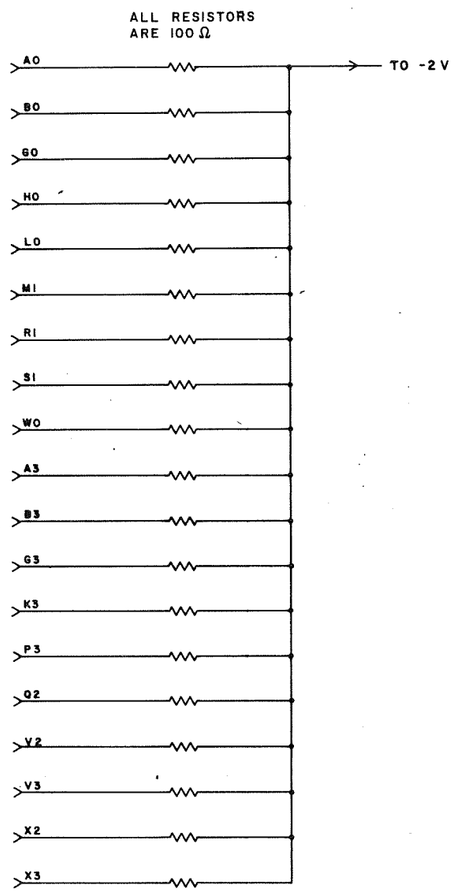
TITLE: A-CONTROL DUMMY MODULE

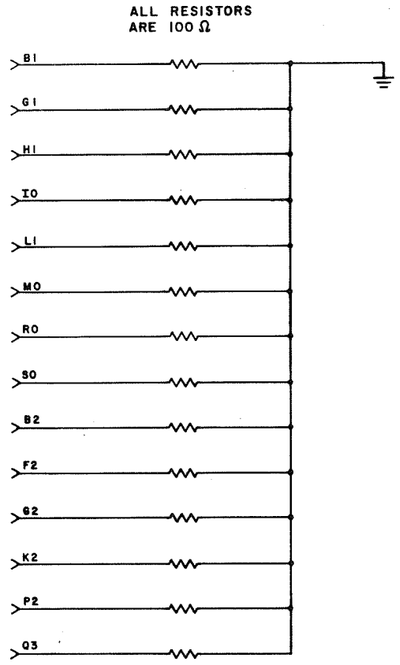
LOC: SEE NOTE 2 PART NO. 18694300

PRODUCT

SIZE C | DRAWING NO. 60181000 | REV. E

SHEET | PAGE 6-197

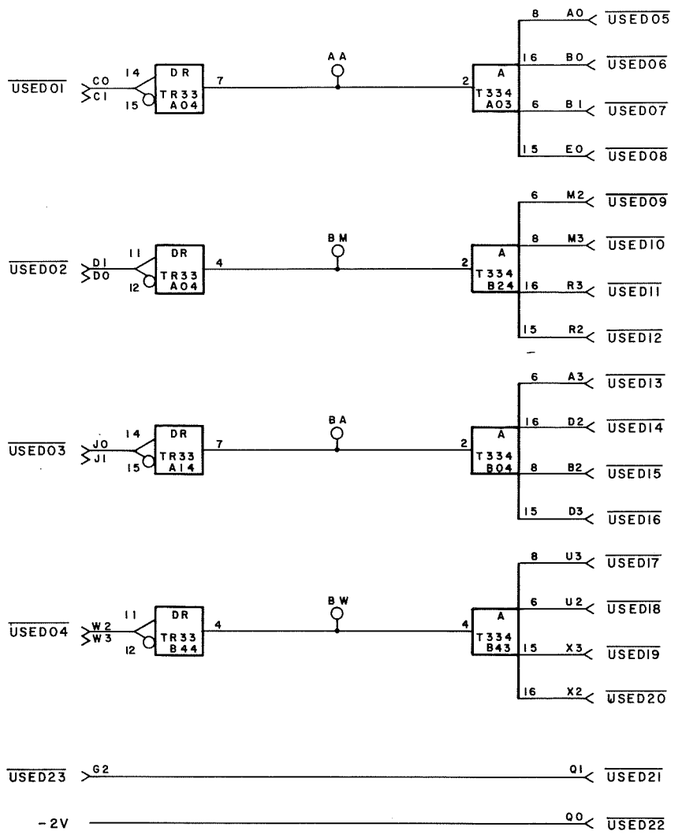




NOTES:

1. THIS MODULE REPLACES THE B-CONTROL MODULE(S) OF A CHANNEL(S) NOT PRESENT.
2. LOCATION IS DEPENDENT ON THE CHANNEL(S) THIS MODULE REPLACES.

CONTROL DATA DEVELOPMENT DIVISION	TITLE B-CONTROL DUMMY MODULE LOC: SEE NOTE 2. PART NO. 8694201	PRODUCT	
		SIZE C	DRAWING NO. 60181000
		REV. A	
		SHEET	PAGE 6-199

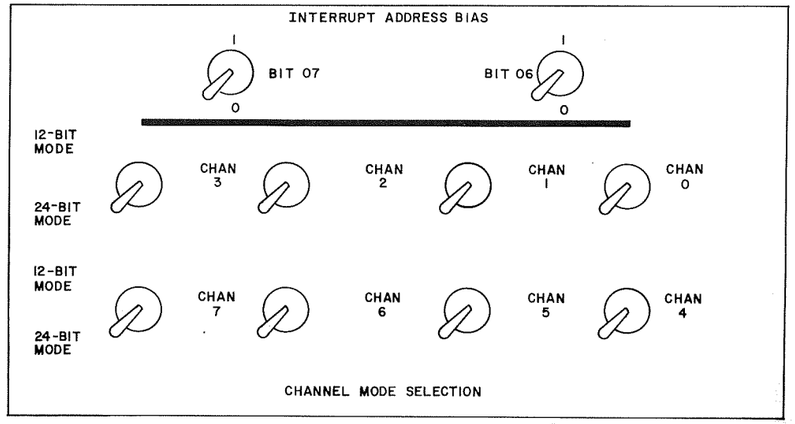


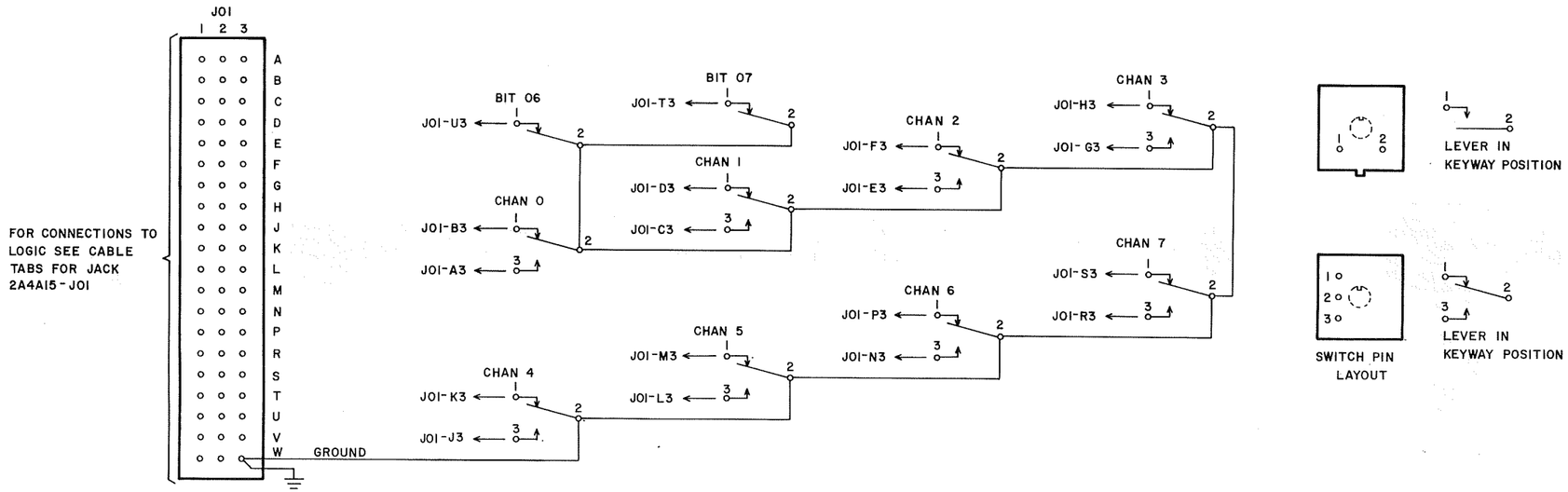
NOTES:

1. THIS MODULE REPLACES THE C-CONTROL MODULE(S) OF A CHANNEL(S) NOT PRESENT.
2. LOCATION IS DEPENDENT ON THE CHANNEL(S) THIS MODULE REPLACES.

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE C-CONTROL DUMMY MODULE LOC: SEE NOTE 2. PART NO. 1869440	PRODUCT	
		SIZE C / DRAWING NO. 60181000	REV. A
		SHEET	PAGE 6-201

PART 7
I/O SWITCH PANEL
MAINTENANCE PANEL





ASSEMBLY 2A4A15

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	I/O SWITCH PANEL	EQUIPMENT	
		SIZE C · DRAWING NO. 60181000	REV. A
		SHEET	PAGE 7-1

TABS FOR MAINTENANCE PANEL

CONNECTOR J1

MAINT PANEL CONNECTION	TAPER-PIN CONN	PIN	DESTINATION	SIGNAL NAME	DEFINITION
DS9-2	J1	A1	2A2A8-H2	S00L	STO ADDR, BIT 00
DS9-1		A2	2A2A8-H3		
		A3			SPARE
DS10-2		B1	2A2A8-E3	S01L	STO ADDR, BIT 01
DS10-1		B2	2A2A8-E2		
S20-1		B3	2A2B9-D0	SP09S1	UPPER WR LIMIT, BIT 09
DS11-2		C1	2A2A8-B2	S02L	STO ADDR, BIT 02
DS11-1		C2	2A2A8-B3		
		C3			SPARE
DS12-2		D1	2A2A8-C3	S03L	STO ADDR, BIT 03
DS12-1		D2	2A2A8-C2		
S21-1		D3	2A2B9-E1	SP10S1	UPPER WR LIMIT, BIT 10
DS13-2		E1	2A2A8-K3	S04L	STO ADDR, BIT 04
DS13-1		E2	2A2A8-K2		
		E3			SPARE
DS14-2		F1	2A2A8-J1	S05L	STO ADDR, BIT 05
DS14-1		F2	2A2A8-J0		
S22-1		F3	2A2B9-D3	SP11S1	UPPER WR LIMIT, BIT 11
DS15-2		G1	2A2A8-E1	S06L	STO ADDR, BIT 06
DS15-1		G2	2A2A8-E0		
		G3			SPARE
DS16-2		H1	2A2A8-B0	S07L	STO ADDR, BIT 07
DS16-1		H2	2A2A8-B1		
S23-1		H3	2A2B9-H3	SP12S1	UPPER WR LIMIT, BIT 12
DS17-2		J1	2A2A8-D1	S08L	STO ADDR, BIT 08
DS17-1		J2	2A2A8-D0		
		J3			SPARE
DS18-2		K1	2A2A9-H2	S09RL	STO ADDR, BIT 09
DS18-1		K2	2A2A9-H3		
S24-1		K3	2A2B9-D3	SP13S1	UPPER WR LIMIT, BIT 13
DS19-2		L1	2A2A9-E3	S10RL	STO ADDR, BIT 10
DS19-1		L2	2A2A9-E2		
		L3			SPARE
DS20-2		M1	2A2A9-B2	S11RL	STO ADDR, BIT 11
DS20-1		M2	2A2A9-B3		
S25-1		M3	2A2B9-S3	SP14S1	UPPER WR LIMIT, BIT 14
DS21-2		N1	2A2A9-C3	S12RL	STO ADDR, BIT 12
DS21-1		N2	2A2A9-C2		
		N3			SPARE
DS22-2		P1	2A2A9-K3	S13RL	STO ADDR, BIT 13
DS22-1		P2	2A2A9-K2		
		P3			SPARE
DS23-2		R1	2A2A9-J1	S14RL	STO ADDR, BIT 14
DS23-1		R2	2A2A9-J0		
		R3			SPARE
DS24-2		S1	2A2A9-E1	S15RL	STO ADDR, BIT 15
DS24-1		S2	2A2A9-E0		
		S3			SPARE
DS25-2		T1	2A2A9-B0	S16RL	STO ADDR, BIT 16
DS25-1		T2	2A2A9-B1		
		T3			SPARE
DS26-2		U1	2A2A9-D1	S17RL	STO ADDR, BIT 17
DS26-1		U2	2A2A9-D0		
		U3			SPARE
DS27-2		V1	2A2B9-I0	SLPL	STO PARITY BIT
DS27-1		V2	2A2B9-I1		
		V3			SPARE
		W1			SPARE
		W2			SPARE
	J1	W3			SPARE

CONNECTOR J2

MAINT PANEL CONNECTION	TAPER-PIN CONN	PIN	DESTINATION	SIGNAL NAME	DEFINITION
DS28-2	J2	A1	2A2B8-Q2	PFZ00L	PAGE FILE OUTPUT, BIT 0
DS28-1		A2	2A2B8-Q3		
		A3			SPARE
DS29-2		B1	2A2B8-P2	PFZ01L	PAGE FILE OUTPUT, BIT 1
DS29-1		B2	2A2B8-P3		
S20-1		B3	2A2B9-C0	SP09S0	LOWER WR LIMIT, BIT 09
DS30-2		C1	2A2B7-V2	PFZ02L	PAGE FILE OUTPUT, BIT 02
DS30-1		C2	2A2B7-V3		
		C3			SPARE
DS31-2		D1	2A2B7-S2	PFZ03L	PAGE FILE OUTPUT, BIT 03
DS31-1		D2	2A2B7-S3		
S21-1		D3	2A2B9-D1	SP10S0	LOWER WR LIMIT, BIT 10
DS32-2		E1	2A2B6-V2	PFZ04L	PAGE FILE OUTPUT, BIT 04
DS32-1		E2	2A2B6-V3		
		E3			SPARE
DS33-2		F1	2A2B6-S2	PFZ05L	PAGE FILE OUTPUT, BIT 05
DS33-1		F2	2A2B6-S3		
S22-1		F3	2A2B9-C3	SP11S0	LOWER WR LIMIT, BIT 11
DS34-2		G1	2A2B5-V2	PFZ06L	PAGE FILE OUTPUT, BIT 06
DS34-1		G2	2A2B5-V3		
		G3			SPARE
DS35-2		H1	2A2B5-S2	PFZ07L	PAGE FILE OUTPUT, BIT 07
DS35-1		H2	2A2B5-S3		
S23-1		H3	2A2B9-I3	SP12S0	LOWER WR LIMIT, BIT 12
DS36-2		J1	2A2B4-T3	PFZ08L	PAGE FILE OUTPUT, BIT 08
DS36-1		J2	2A2B4-T2		
		J3			SPARE
DS37-2		K1	2A2B4-Q0	PFZ09L	PAGE FILE OUTPUT, BIT 09
DS37-1		K2	2A2B4-Q1		
S24-1		K3	2A2B9-N3	SP13S0	LOWER WR LIMIT, BIT 13
DS38-2		L1	2A2B4-X1	PFZ10L	PAGE FILE OUTPUT, BIT 10
DS38-1		L2	2A2B4-X0		
		L3	2B0B5-L3	$\overline{\text{SINGLE}}$	CHANNEL COUPLER
DS39-2		M1	2A2B4-V2	PFZ11L	PAGE FILE OUTPUT, BIT 11
DS39-1		M2	2A2B4-V3		
S25-1		M3	2A2B9-T3	SP14S0	LOWER WR LIMIT, BIT 14
DS40-2		N1	2A2B8-C1	S09L	PAGE FILE INPUT, BIT 09
DS40-1		N2	2A2B8-C0		
S6-1		N3	2B1B8-I0	CLKON	REAL-TIME CLOCK SW
DS41-2		P1	2A2B8-B1	S10L	PAGE FILE INPUT, BIT 10
DS41-1		P2	2A2B8-B0		
S8-3		P3	2B1A8-W0	MAINT	MAINT MODE SW
DS42-2		R1	2A2B7-I0	S11L	PAGE FILE INPUT, BIT 11
DS42-1		R2	2A2B7-I1		
S8-3		R3	2A1A06-P06F-07	MAINT	MAINT MODE SW
DS43-2		S1	2A2B7-R2	S12L	PAGE FILE INPUT, BIT 12
DS43-1		S2	2A2B7-R3		
S7-3		S3	2A1A06-P09E-09	TSTMOD	TEST MODE SWITCH
DS44-2		T1	2A2B6-I0	S13L	PAGE FILE INPUT, BIT 13
DS44-1		T2	2A2B6-I1		
		T3			SPARE
DS45-2		U1	2A2B6-R2	S14L	PAGE FILE INPUT, BIT 14
DS45-1		U2	2A2B6-R3		
		U3			SPARE
DS46-2		V1	2A2B5-I0	S15L	PAGE FILE INPUT, BIT 15
DS46-1		V2	2A2B5-I1		
		V3			SPARE
		W1			SPARE
		W2			SPARE
	J2	W3			SPARE

CONNECTOR J3

MAINT PANEL CONNECTION	TAPER-PIN CONN	PIN	DESTINATION	SIGNAL NAME	DEFINITION
DS47-2	J3	A1	2A2B5-R2	S16L	PAGE FILE INPUT, BIT 16
DS47-1		A2	2A2B5-R3		
S1-3		A3	2A1A06-J17E-09	BPFSMG	BDP FAST TMG MARGIN
DS48-2		B1	2A2B4-Q2	S17L	PAGE FILE INPUT, BIT 17
DS48-1		B2	2A2B4-Q3		
S1-1		B3	2A1A06-J17E-10	BPSLMG	BDP SLOW TMG MARGIN
DS1-2		C1	2A1A06-P06E-03	MILT00	CYCLE CTR BIT 0 OR
DS1-1		C2	2A1A06-P06E-04		MAINT REG BIT 0,8, OR 16
S2-3		C3	2A1A06-P09E-05	FAST-A	ARITH FAST TMG MARG
DS2-2		D1	2A1A06-P06E-05	MILT01	CYCLE CTR BIT 1 OR
DS2-1		D2	2A1A06-P06E-06		MAINT REG BIT 1,9, OR 17
S2-1		D3	2A1A06-P09E-06	SLOW-A	ARITH SLOW TMG MARG
DS3-2		E1	2A1A06-P06E-07	MILT02	CYCLE CTR BIT 2 OR
DS3-1		E2	2A1A06-P06E-08		MAINT REG BIT 2,10, OR 18
S3-3		E3	2A2A4-P3	$\overline{\text{PFFM}}$	P.FILE FAST TMG MARG
DS4-2		F1	2A1A06-P06E-09	MILT03	CYCLE CTR BIT 3 OR
DS4-1		F2	2A1A06-P06E-10		MAINT REG BIT 3,11, OR 19
S3-1		F3	2A2A4-N3	$\overline{\text{PFSM}}$	P.FILE SLOW TMG MARG
DS5-2		G1	2A1A06-P06F-01	MILT04	CYCLE CTR BIT 4 OR
DS5-1		G2	2A1A06-P06F-02		MAINT REG BIT 4,12, OR 20
S4-3		G3	2B1B7-W2	FAST-B	B.CONT FAST TMG MARG
DS6-2		H1	2A1A06-P06F-03	MILT05	CYCLE CTR BIT 5 OR
DS6-1		H2	2A1A06-P06F-04		MAINT REG BIT 5,13, OR 21
S4-1		H3	2B1B7-V2	SLOW-B	B.CONT SLOW TMG MARG
DS7-2		J1	2A1A06-P06F-05	MILT06	CYCLE CTR BIT 6 OR
DS7-1		J2	2A1A06-P06F-06		MAINT REG BIT 6,14, OR 22
S5-3		J3	2A1A06-P09E-04	FAST	M.CONT FAST TMG MARG
DS8-2		K1	2A1A06-P06D-05	MILT07	CYCLE CTR BIT 7 OR
DS8-1		K2	2A1A06-P06D-06		MAINT REG BIT 7,15, OR 23
S5-1		K3	2A1A06-P09E-03	SLOW	M.CONT SLOW TMG MARG
		L1			SPARE
E1		L2	2A1A06-J16D-10	MMGND	GROUND TO M.MODE SW
S1-2		L3	2A1A06-J16C-09	MMENAB	ENABLE FROM M.MODE SW
		M1			SPARE
		M2			SPARE
S10-2		M3	2A1A06-J17F-01	BT13OR	MAINT REG SELECT
		N1			SPARE
		N2			SPARE
S9-3		N3	2A1A06-P06F-08	MOLT-1	SELECT MAINT REG (UPPER)
		P1			SPARE
		P2			SPARE
S9-1		P3	2A1A06-P06B-07	MOLT-2	SELECT MAINT REG (MID)
		R1			SPARE
		R2			SPARE
S9-4		R3	2A1A06-P06B-08	MOLT-3	SELECT MAINT REG (LOWER)
		S1			SPARE
		S2			
		S3			
		T1			
		T2			
		T3			
		U1			
		U2			
		U3			
		V1			
		V2			
		V3			
		W1			
		W2			
	J3	W3			SPARE

PAGE FILE INPUT

PAGE FILE ADDRESS

	BIT 17	16	15	14	13	12	11	PP 10	PP 09
J3	B2/BI	A2/AI	J2 V2/VI	U2/UI	T2/TI	S2/SI	R2/RI	P2/PI	N2/NI
	DS48	DS47	DS46	DS45	DS44	DS43	DS42	DS41	DS40

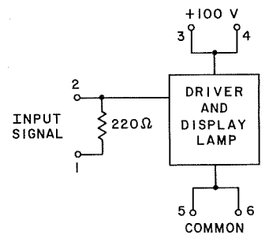
PAGE FILE OUTPUT

	E BIT 11	PL 10	PL 09	PA 08	PA 07	PA 06	PA 05	PA 04	PA 03	PA 02	PP 01	PP 00
J2	M2/MI	L2/LI	K2/KI	J2/JI	H2/HI	G2/GI	F2/FI	E2/EI	D2/DI	C2/CI	B2/BI	A2/AI
	DS39	DS38	DS37	DS36	DS35	DS34	DS33	DS32	DS31	DS30	DS29	DS28

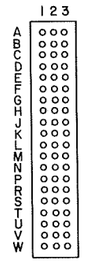
STORAGE ADDRESS

	PARITY BIT	BIT 17	16	15	14	13	12	11	10	09
J1	V2/VI	U2/UI	T2/TI	S2/SI	R2/RI	P2/PI	N2/NI	M2/MI	L2/LI	K2/KI
	DS27	DS26	DS25	DS24	DS23	DS22	DS21	DS20	DS19	DS18

SCHEMATIC FOR DS1–DS48



LAYOUT OF J1, J2, J3 TAPER-PIN BLOCKS



UPPER WRITE LIMIT

	BIT 14	13	12	11	10	09
J1	M3	K3	H3	F3	D3	B3
	S25	S24	S23	S22	S21	S20

SWITCHES S11–S16 AND S20–S26 ARE SHOWN IN THE DOWN (0) POSITION.

LOWER WRITE LIMIT

	CHANNEL COUPLER	BIT 14	13	12	11	10	09
J2	L3	M3	K3	H3	F3	D3	B3
	S26	S16	S15	S14	S13	S12	S11

A OR B TO A AND B

A TO B AND B TO A

STORAGE ADDRESS

	BIT 08	07	06	05	04	03	02	01	00
J1	J2/JI	H2/HI	G2/GI	F2/FI	E2/EI	D2/DI	C2/CI	B2/BI	A2/AI
	DS17	DS16	DS15	DS14	DS13	DS12	DS11	DS10	DS9

MAINTENANCE REGISTER SELECT

	DISPLAY SELECT	(LOWER) L	(MID) M	(UPPER) U
J3	M3	R3	P3	N3

CC, MR (DOWN), S10, S9

S9 IS SHOWN IN THE CENTER (M) POSITION. IN THE UP POSITION, CONTACTS 2–6 AND 5–3 ARE CLOSED. IN THE DOWN POSITION, CONTACTS 2–4 AND 5–1 ARE CLOSED.

MAINTENANCE REGISTER OR CYCLE COUTER

BITS	U 23	22	21	20	19	18	17	16
	M 15	14	13	12	11	10	9	8
	L 7	6	5	4	3	2	1	0
J3	K2/KI	J2/JI	H2/HI	G2/GI	F2/FI	E2/EI	D2/DI	C2/CI
	DS8	DS7	DS6	DS5	DS4	DS3	DS2	DS1

DS4–DS48 ARE WIRED AS SHOWN FOR DS1–DS3.

	MAINT MODE GRD	MAINT MODE ENABLE	MAINT MODE	TEST MODE	REAL-TIME CLOCK
J3	L2	L3			
J2			R3 P3	S3	N3

S8, S7, S6

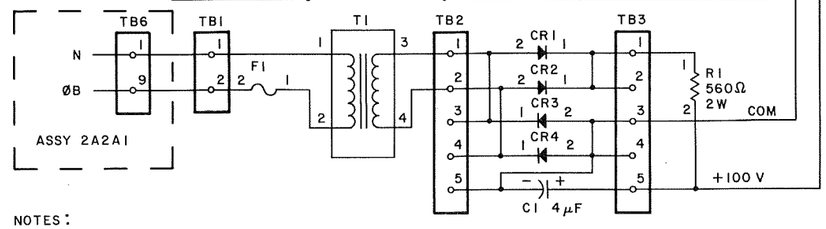
SWITCHES S6–S8 ARE SHOWN IN THE DOWN POSITION.

E1 LOGIC GROUND

TIMING MARGINS

	MC SLOW FAST	BC SLOW FAST	PF SLOW FAST	AR SLOW FAST	BDP SLOW FAST
J3	K3 J3	H3 G3	F3 E3	D3 C3	B3 A3
	S5	S4	S3	S2	S1

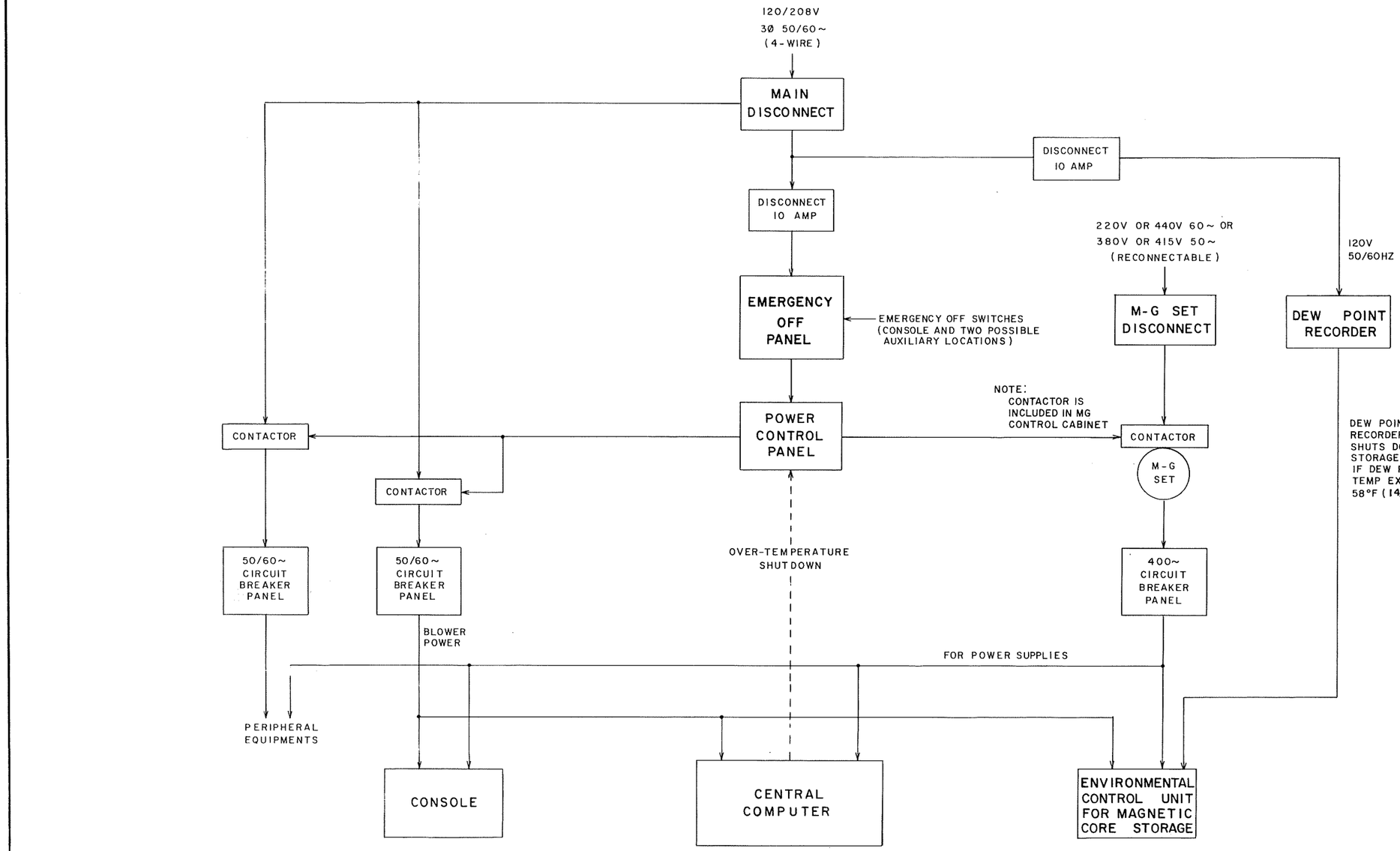
SWITCHES S1–S5 ARE SHOWN IN THE CENTER (NORMAL) POSITION.



NOTES:

1. J1, J2, AND J3 ARE TAPER-PIN CONNECTOR BLOCKS LOCATED BEHIND PANEL. (SEE LAYOUT AT LEFT, LOGIC WIRING INFORMATION IS PRESENTED ON THE FACING PAGE.)
2. WIRING FOR DISPLAYS DS1–DS3 IS SHOWN; DS4–DS48 ARE WIRED SIMILARLY.

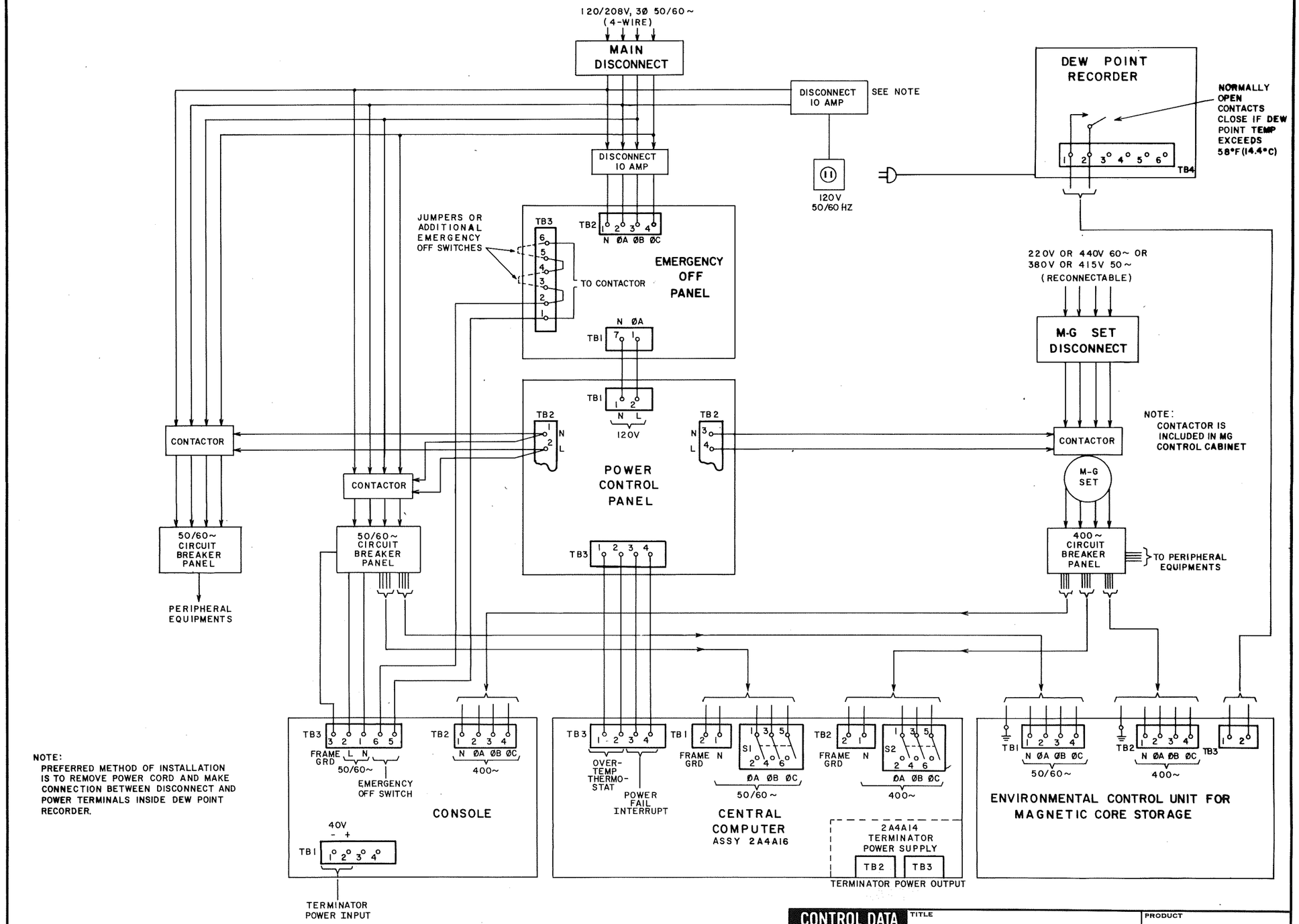
CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE COMPUTER MAINTENANCE PANEL SCHEMATIC ASSEMBLY 2A2A4	PRODUCT 3500 SIZE C · DRAWING NO. 60181000 · REV. A SHEET · PAGE 7-3	



NOTES:
THE 50~ AND 60~ SYSTEMS ARE NOT DIRECTLY INTERCHANGEABLE.

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE TYPICAL POWER DISTRIBUTION	PRODUCT	
		SIZE C	DRAWING NO. 60181000
		REV. Z	
		SHEET	PAGE 8-1

2 System



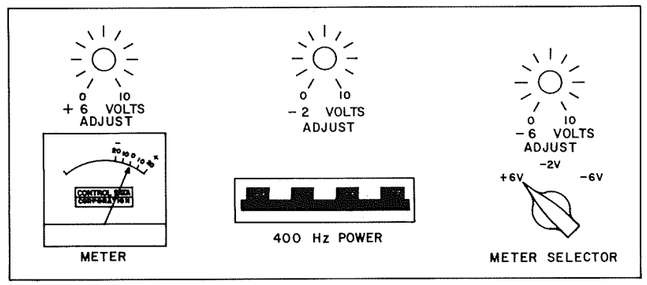
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE
INTER-UNIT POWER CONNECTIONS

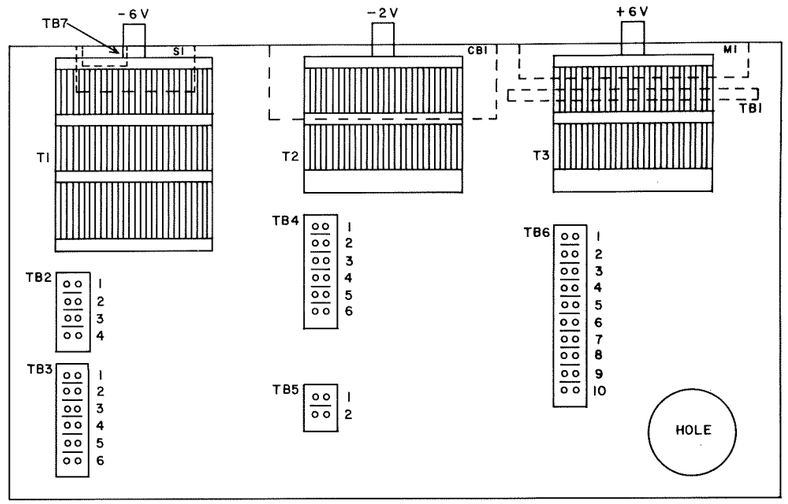
PRODUCT

SIZE	DRAWING NO.	REV.
C	60181000	Z

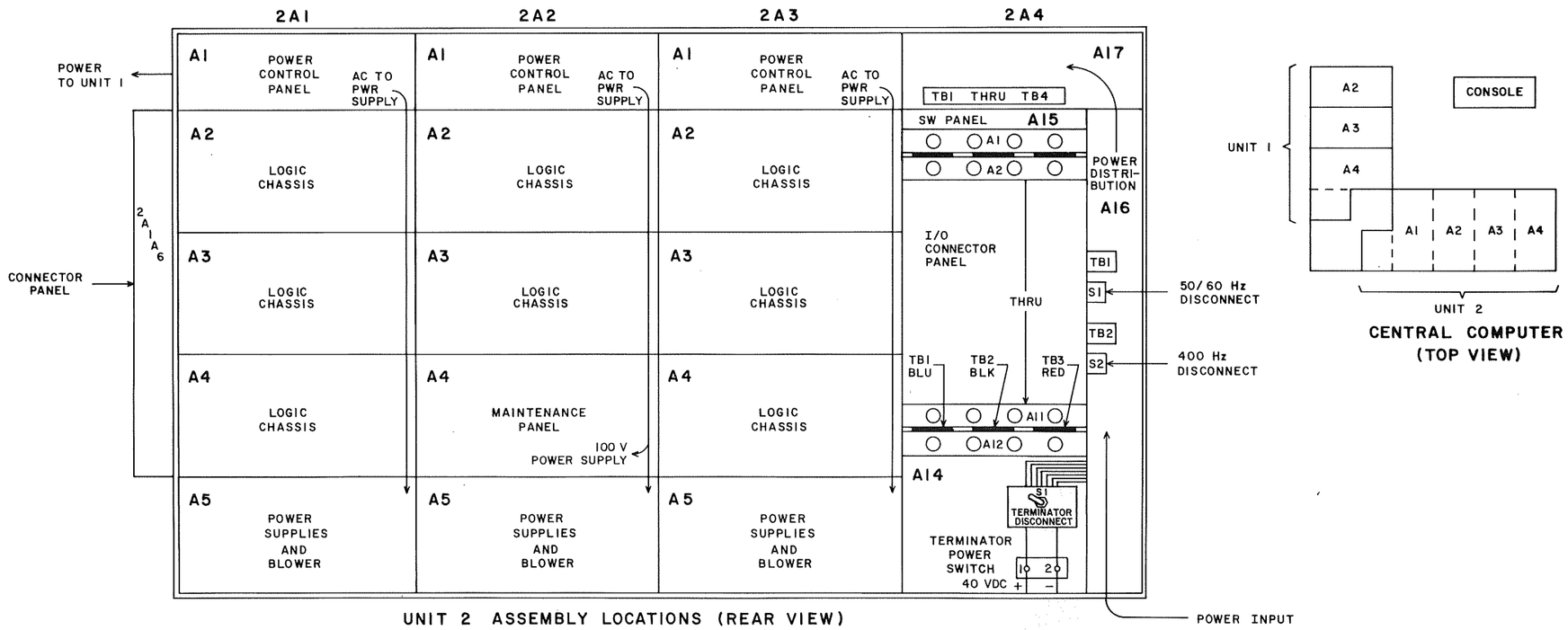
SHEET — PAGE 8-3



POWER CONTROL PANEL (FRONT VIEW)



POWER CONTROL PANEL (TOP VIEW)

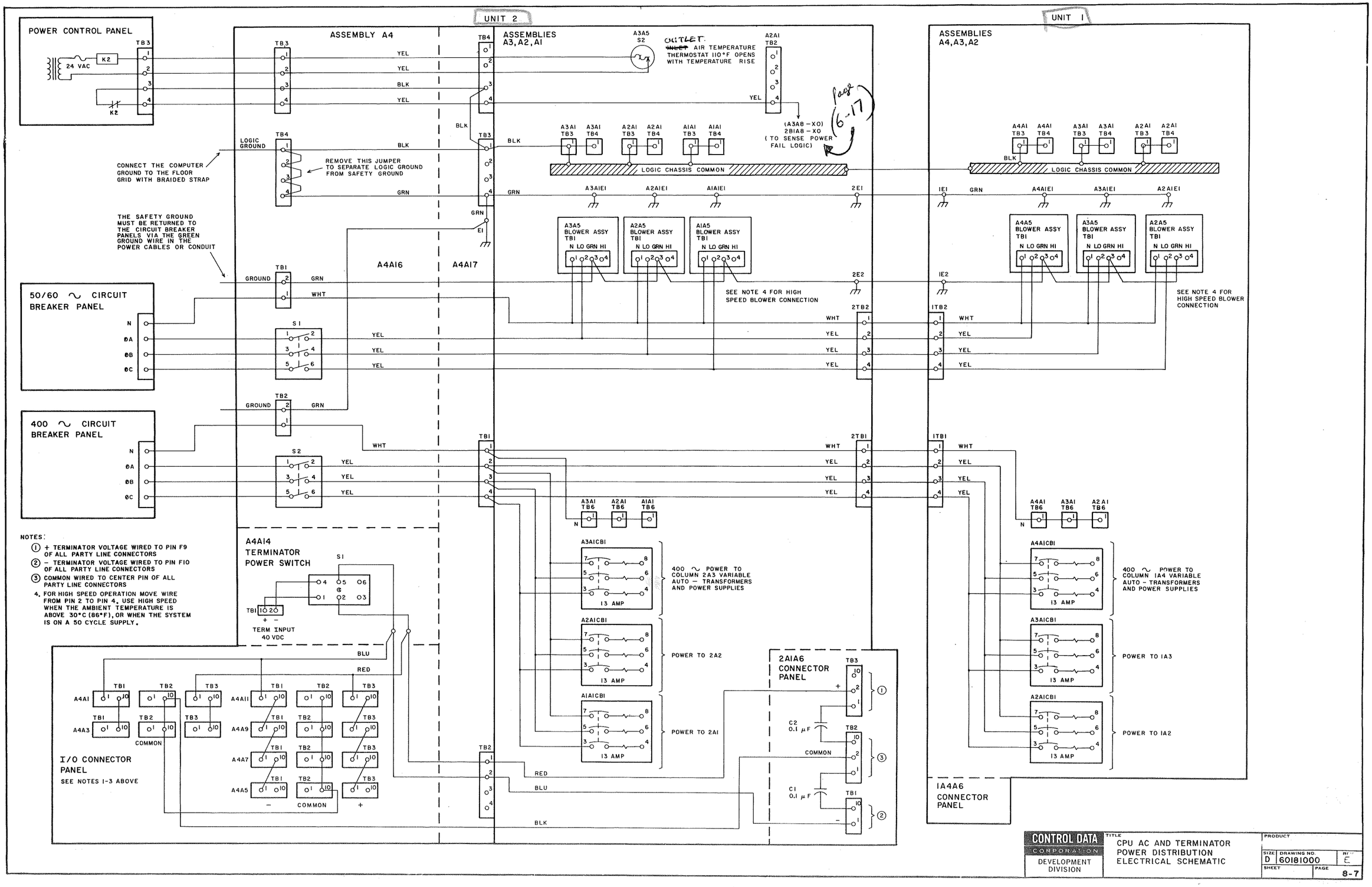


UNIT 2 ASSEMBLY LOCATIONS (REAR VIEW)

CENTRAL COMPUTER (TOP VIEW)

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE: CENTRAL COMPUTER ASSEMBLIES	PRODUCT	
		SIZE C	DRAWING NO. 60181000
		REV. Z	
		SHEET	PAGE 8-5

401


UNIT 2
UNIT 1
POWER CONTROL PANEL
24 VAC
K2
ASSEMBLY A4
A4A16
A4A17
ASSEMBLIES A3, A2, A1
ASSEMBLIES A4, A3, A2
A3A5 S2
OUTLET AIR TEMPERATURE THERMOSTAT 110°F OPENS WITH TEMPERATURE RISE
A2A1 TB2
YEL
(A3AB – XO)
2B1AB – XO
(TO SENSE POWER FAIL LOGIC)
page 6-17
LOGIC CHASSIS COMMON
BLK
GRN
YEL
WHT
LOGIC GROUND
CONNECT THE COMPUTER GROUND TO THE FLOOR GRID WITH BRAIDED STRAP
REMOVE THIS JUMPER TO SEPARATE LOGIC GROUND FROM SAFETY GROUND
THE SAFETY GROUND MUST BE RETURNED TO THE CIRCUIT BREAKER PANELS VIA THE GREEN GROUND WIRE IN THE POWER CABLES OR CONDUIT
50/60 ~ CIRCUIT BREAKER PANEL
400 ~ CIRCUIT BREAKER PANEL
N
ØA
ØB
ØC
GROUND
S1
S2
A3A1 TB3
A3A1 TB4
A2A1 TB3
A2A1 TB4
A1A1 TB3
A1A1 TB4
A4A1 TB3
A4A1 TB4
A3A1E1
A2A1E1
A1A1E1
2E1
1E1
A4A1E1
A3A1E1
A2A1E1
A3A5 BLOWER ASSY TB1
A2A5 BLOWER ASSY TB1
A1A5 BLOWER ASSY TB1
A4A5 BLOWER ASSY TB1
N LO GRN HI
SEE NOTE 4 FOR HIGH SPEED BLOWER CONNECTION
2E2
1E2
2TB2
1TB2
A3A1 TB6
A2A1 TB6
A1A1 TB6
A4A1 TB6
A3A1CBI
A2A1CBI
A1A1CBI
A4A1CBI
13 AMP
400 ~ POWER TO COLUMN 2A3 VARIABLE AUTO – TRANSFORMERS AND POWER SUPPLIES
POWER TO 2A2
POWER TO 2A1
400 ~ POWER TO COLUMN 1A4 VARIABLE AUTO – TRANSFORMERS AND POWER SUPPLIES
POWER TO 1A3
POWER TO 1A2
A4A1I4 TERMINATOR POWER SWITCH
TERM INPUT 40 VDC
I/O CONNECTOR PANEL
SEE NOTES 1-3 ABOVE
COMMON
2A1A6 CONNECTOR PANEL
1A4A6 CONNECTOR PANEL
C2 0.1 μF
C1 0.1 μF
NOTES:
① + TERMINATOR VOLTAGE WIRED TO PIN F9 OF ALL PARTY LINE CONNECTORS
② – TERMINATOR VOLTAGE WIRED TO PIN F10 OF ALL PARTY LINE CONNECTORS
③ COMMON WIRED TO CENTER PIN OF ALL PARTY LINE CONNECTORS
4. FOR HIGH SPEED OPERATION MOVE WIRE FROM PIN 2 TO PIN 4. USE HIGH SPEED WHEN THE AMBIENT TEMPERATURE IS ABOVE 30°C (86°F), OR WHEN THE SYSTEM IS ON A 50 CYCLE SUPPLY.
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
TITLE
CPU AC AND TERMINATOR POWER DISTRIBUTION ELECTRICAL SCHEMATIC
PRODUCT
SIZE D
DRAWING NO. 60181000
REV E
SHEET
PAGE 8-7
403

UNIT 2

UNIT 1

A4A17 TB1

208V,3Ø 400~ N ØA ØB ØC

WHT YEL YEL YEL

CB1 I3AMP

CIRCUIT BREAKER TERMINALS LINE LOAD

ASSY 2A3A1

VARIABLE 3Ø AUTOTRANSFORMER −6V

VARIABLE 2Ø AUTOTRANSFORMER −2V

VARIABLE 2Ø AUTOTRANSFORMER +6V

T1 T2 T3

TO CB1

ASSY 2A2A1 (SAME AS 2A3A1)

ASSY 2A1A1 (SAME AS 2A3A1)

2TB1 1TB1

ASSY 1A4A1 (SAME AS 2A3A1)

ASSY 1A3A1 (SAME AS 2A3A1 LESS +6V CONTROL)

ASSY 1A2A1 (SAME AS 2A3A1 LESS +6V CONTROL WITH INDICATED ADDITIONS)

TB7 CR1

1 MA MOVEMENT (77Ω) WITH EXTERNAL MULTIPLIER

S1 M1

TB1 R3 1K R4 2K R1 2K R2 6.49K

+6V −2V −6V

TB3 TB4

DOOR LAMPS DS1 DS2

60 AMP OVER-CURRENT RELAYS K1 K2

WV1 WV2

W1 −6V W2 −0.9V W3 −2V W4 +6V

W5 −6V W6 −0.9V W7 −2V W8 +6V

C1 0.5μF C3 2000μF C2 500μF C4 C6 C5

TB1 R1 0.5Ω 10W 0.9V POWER SUPPLY CR1

ASSY 2A3A2

ASSY 2A3A3

.9v Power Supply.

E1

-2V BUS -6V BUS

ASSY 2A2A2 (SAME AS 2A3A2)

ASSY 2A2A3 (SAME AS 2A3A3)

ASSY 2A2A4 MAINTENANCE PANEL

ASSY 2A1A2 (SAME AS 2A3A2)

ASSY 2A1A3 (SAME AS 2A3A3)

ASSY 2A1A4 (SAME AS 2A3A4)

ASSY 2A1A5 (SAME AS 2A3A5)

ASSY 1A4A2 (SAME AS 2A3A2)

ASSY 1A3A2 (SAME AS 2A3A2)

ASSY 1A2A2 (SAME AS 2A3A2 WITH INDICATED ADDITIONS)

ASSY 1A4A3 (SAME AS 2A3A3)

ASSY 1A3A3 (SAME AS 2A3A3)

ASSY 1A2A3 (SAME AS 2A3A3)

ASSY 1A4A4 (SAME AS 2A3A4)

ASSY 1A3A4 (SAME AS 2A3A4)

ASSY 1A2A4 (SAME AS 2A3A4)

ASSY 1A4A5 (SIMILAR TO 2A3A5)

ASSY 1A3A5 (SAME AS 2A3A5 LESS +6V SUPPLY)

ASSY 1A2A5 (SAME AS 2A3A5 LESS +6V SUPPLY)

ASSY 2A3A4

SIMILARLY CONNECTED TO DS2 THRU DS48

DS1 TB3-5 R1 560Ω 2W TB3-1,2 TB3-3,4 C1 4μF COMMON TB2-5 TB2-2,4

CR1 CR2 CR3 CR4

100V POWER SUPPLY TB2-1,3 T1 115V 115V,400~ F1 1/8 AMP

TB1 N WHT YEL

TB6

TO DS48-6

E7 E8 BLK W9 GRD BUS W10

C1 4000 μF

TB2 S1 VANE SWITCH IN BLOWER OPENED BY AIR FLOW

ASSY 2A3A5 POWER SUPPLIES

-2V FROM POWER SUPPLY

-6V FROM POWER SUPPLIES

+6V FROM POWER SUPPLY

3Ø 400~ POWER TO −6V POWER SUPPLIES

3Ø 400~ POWER TO −2V POWER SUPPLY

3Ø 400~ POWER TO +6V POWER SUPPLY

TO SI-8 TB3 RED CB1 AUX CONTACT 5b 3d

+6V FROM POWER SUPPLY

+6V TB3 +6V W4

NOTE:

1. ALL GROUNDS SHOWN ON THIS SCHEMATIC ARE LOGIC CHASSIS GROUNDS. THE LOGIC CHASSIS IS ATTACHED TO THE FRAME WITH INSULATORS.

CONTROL DATA CORPORATION DEVELOPMENT DIVISION

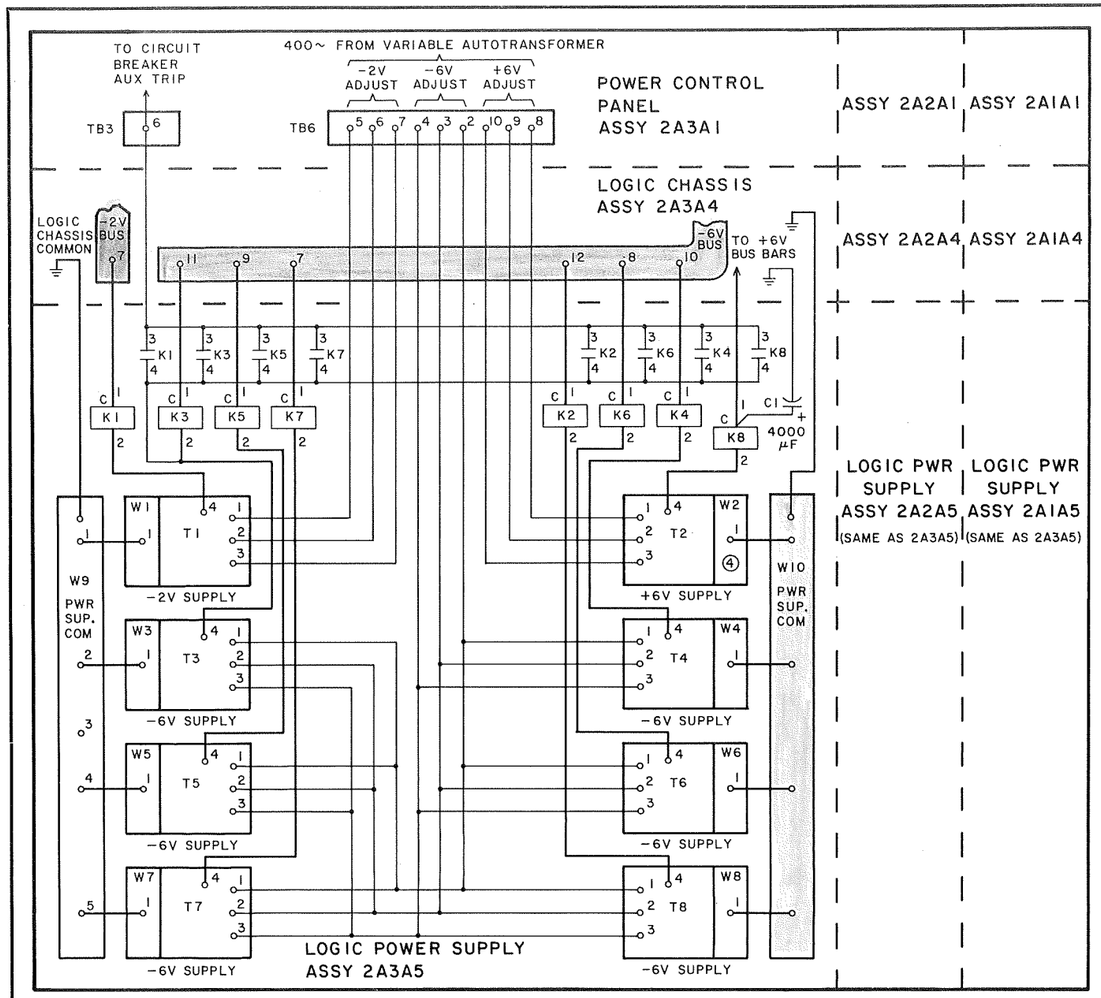
TITLE: POWER CONTROL AND LOGIC CHASSIS SCHEMATIC

PRODUCT

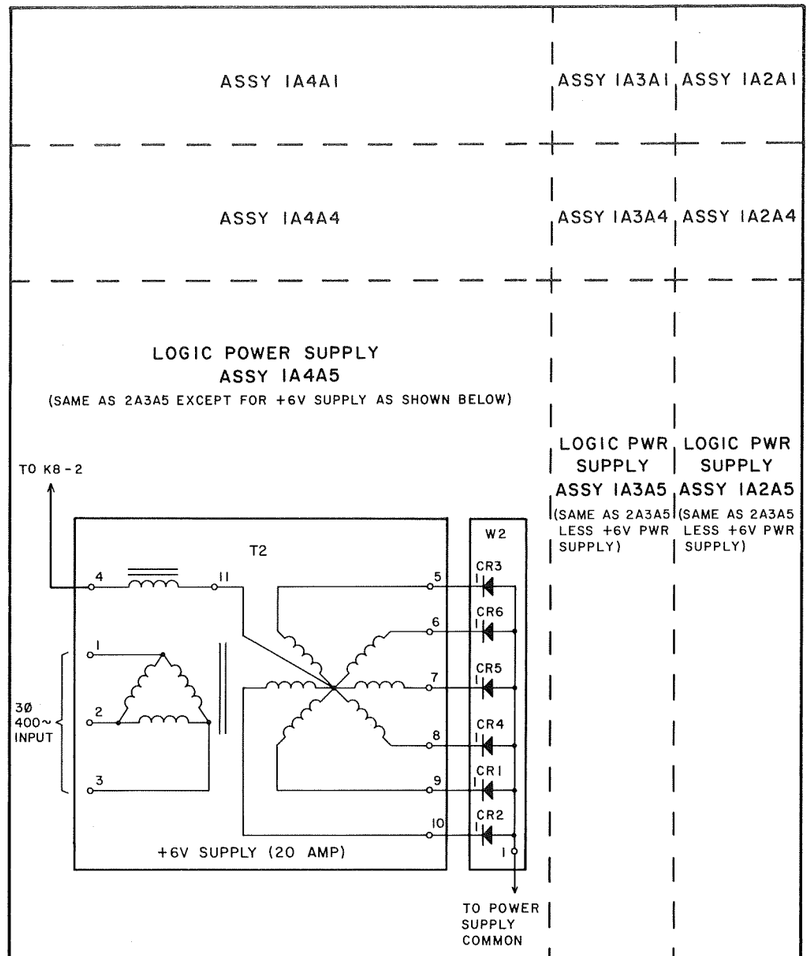
SIZE D DRAWING NO. 60181000 REV. L

SHEET PAGE 8-9

405



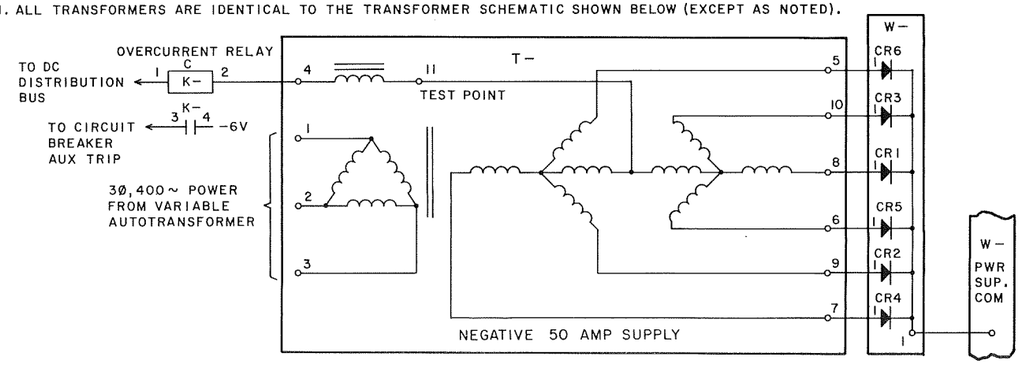
UNIT 2



UNIT 1

NOTES:

1. ALL TRANSFORMERS ARE IDENTICAL TO THE TRANSFORMER SCHEMATIC SHOWN BELOW (EXCEPT AS NOTED).



2. THE OVERCURRENT RELAYS ARE RATED AT 60 AMPERES.
3. THE BASE ASSEMBLY NUMBER FOR THE UNIT 1 POWER SUPPLIES IS 18565500, AND 18565600 FOR THE UNIT 2 SUPPLIES.
④ THE DIODE POLARITY IN THE +6V SUPPLIES IS REVERSED FROM THAT SHOWN IN NOTE 1.

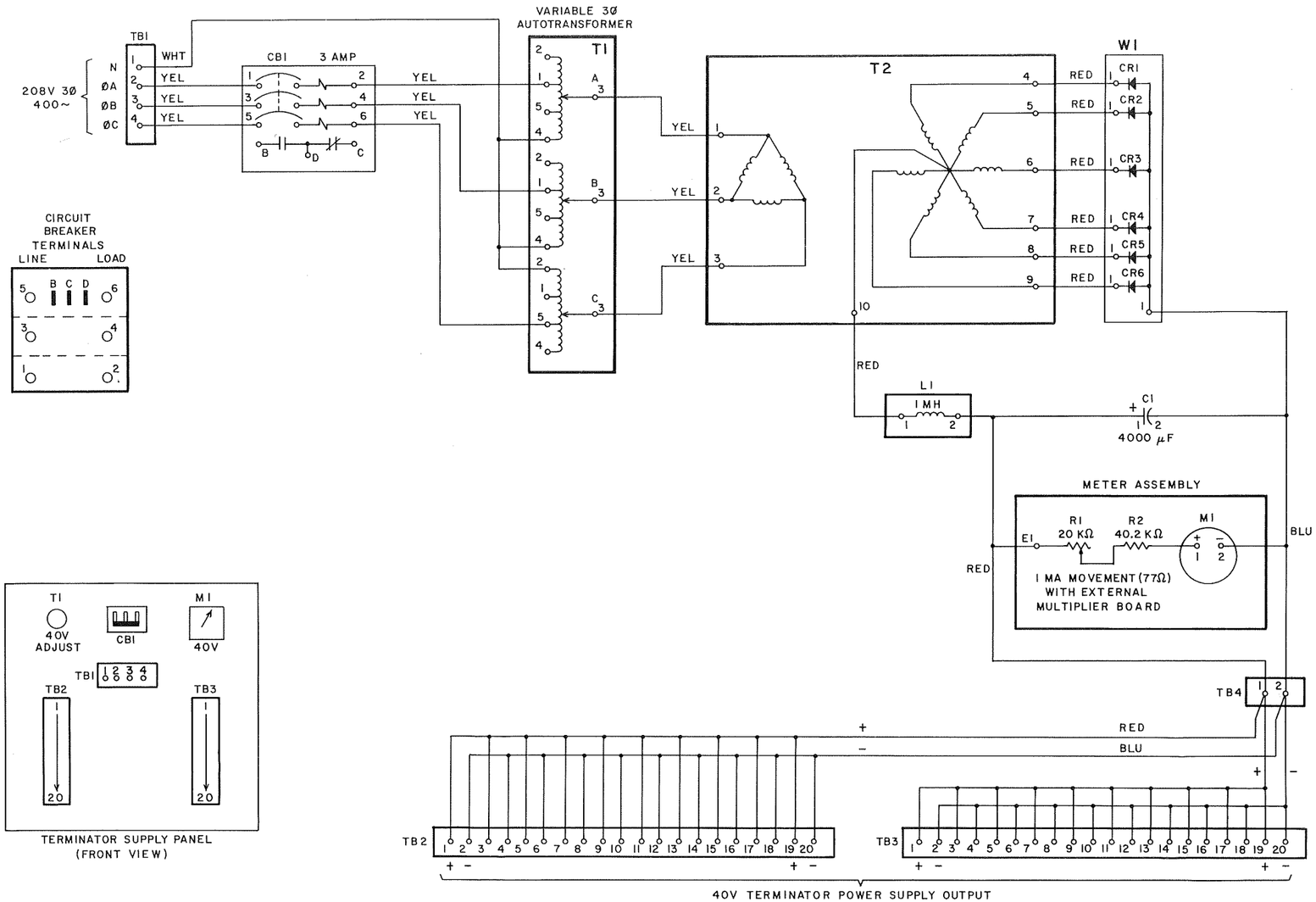
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE: LOGIC POWER SUPPLY SCHEMATIC

PRODUCT

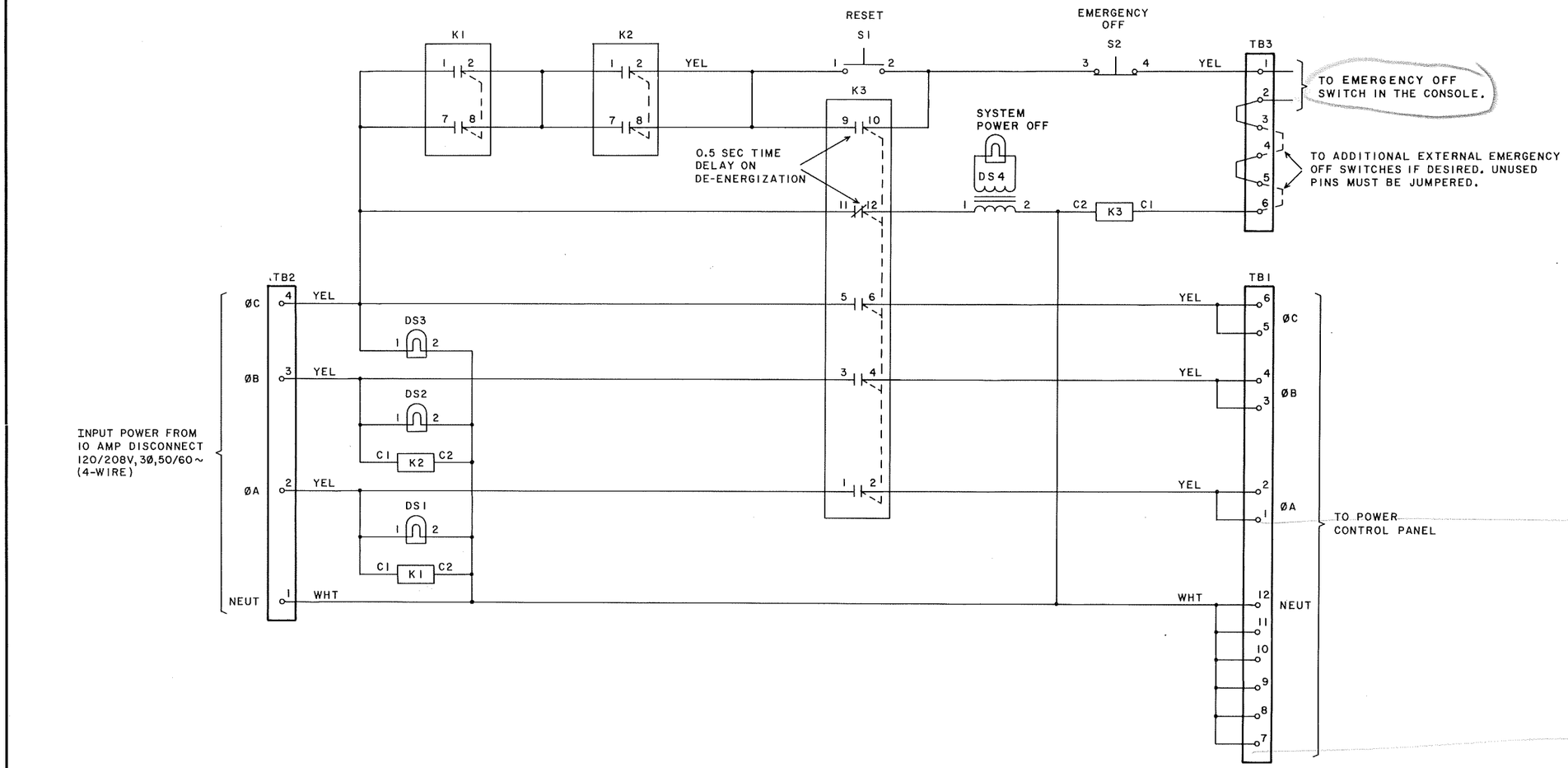
SIZE C | DRAWING NO. 60181000 | REV. A

SHEET | PAGE 8-11

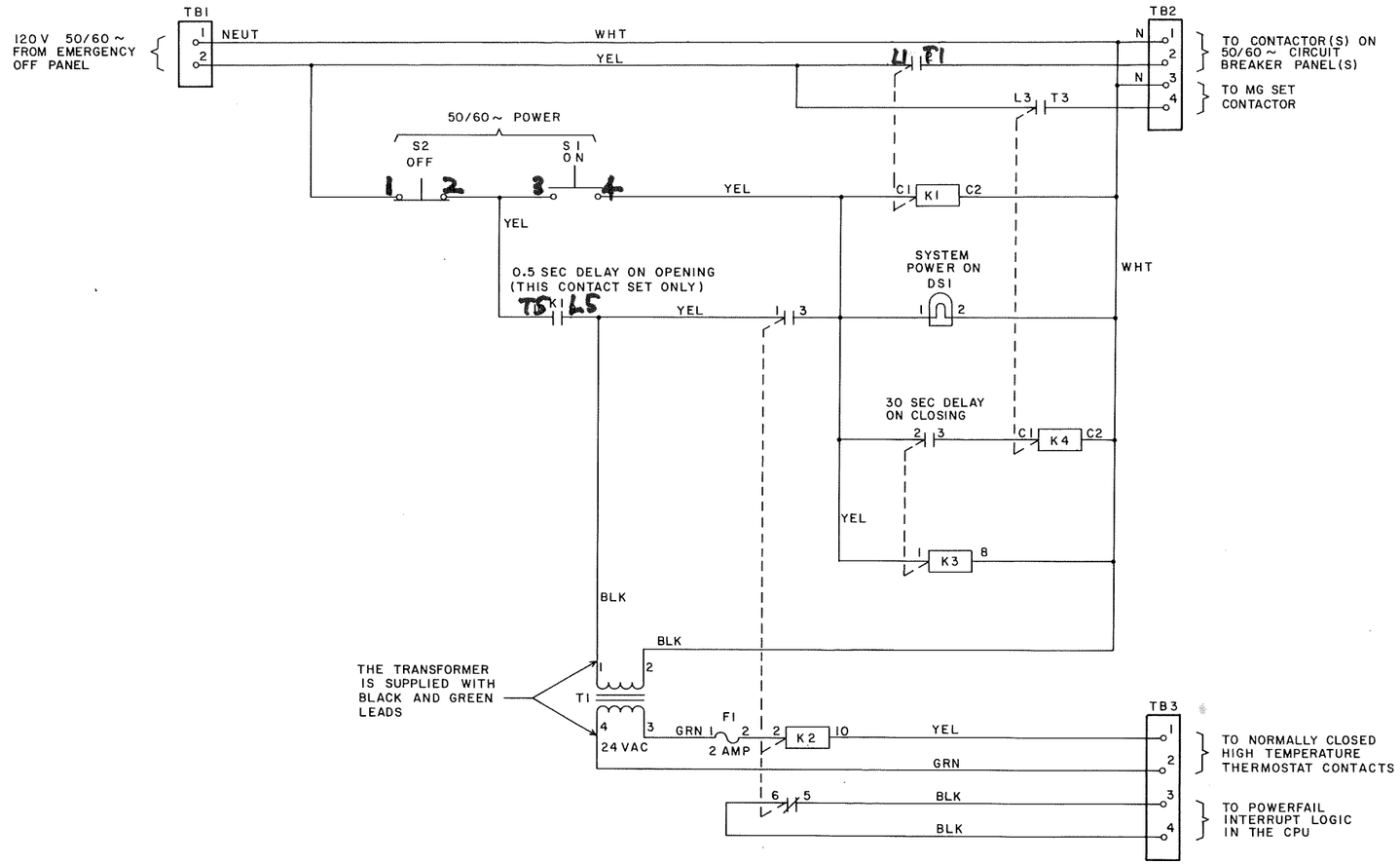


TERMINATOR SUPPLY PANEL
(FRONT VIEW)

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE TERMINATOR SUPPLY SCHEMATIC (40V, 20 AMP)	PRODUCT	
		SIZE C	DRAWING NO. 60181000
		REV. A	
		SHEET	PAGE 8-13



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE EMERGENCY OFF PANEL SCHEMATIC	PRODUCT	
		SIZE C	DRAWING NO. 60181000
		REV. A	
		SHEET	PAGE 8-15



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE POWER CONTROL PANEL SCHEMATIC	PRODUCT	
		SIZE C	DRAWING NO. 60181000 REV. 5
		SHEET	PAGE 8-17

PART 9
CENTRAL PROCESSOR
CABLE TABS

CONNECTOR		ORIGIN	PAGE	DEFINITION	SIG NAME
1A4A06	J02D-02/01	1A0A7-T1*T0	2- 77	B8 BIT 3	$B8LT03
1A4A06	J02D-04/03	1A0A7-L2*L3	2- 77	B8 BIT 4	$B8LT04
1A4A06	J02D-06/05	1A0A7-S0*S1	2- 77	B8 BIT 5	$B8LT05
1A4A06	J02D-08/07	1A0A5-T1*T0	2- 79	B8 BIT 6	$B8LT06
1A4A06	J02D-10/09	1A0A5-L2*L3	2- 79	B8 BIT 7	$B8LT07
1A4A06	J02E-02/01	1A0A5-S0*S1	2- 79	B8 BIT 8	$B8LT08
1A4A06	J02E-04/03	1A0A3-T1*T0	2- 81	B8 BIT 9	$B8LT09
1A4A06	J02E-06/05	1A0A3-L2*L3	2- 81	B8 BIT 10	$B8LT10
1A4A06	J02E-08/07	1A0A3-S0*S1	2- 81	B8 BIT 11	$B8LT11
1A4A06	J02E-10/09	1A0A1-T1*T0	2- 83	B8 BIT 12	$B8LT12
1A4A06	J02F-02/01	1A0A1-L2*L3	2- 83	B8 BIT 13	$B8LT13
1A4A06	J02F-04/03	1A0A1-S0*S1	2- 83	B8 BIT 14	$B8LT14
1A4A06	J04A-02*01	1A0B8-E0/E1	2- 65	NOT MAIN CONTROL READ, BIT 00	$MCRD00
1A4A06	J04A-04*03	1A0B8-F0/F1	2- 65	NOT MAIN CONTROL READ, BIT 01	$MCRD01
1A4A06	J04A-06*05	1A0B8-W1/W0	2- 65	NOT MAIN CONTROL READ, BIT 02	$MCRD02
1A4A06	J04A-08*07	1A0B6-E0/E1	2- 67	NOT MAIN CONTROL READ, BIT 03	$MCRD03
1A4A06	J04A-10*09	1A0B6-F0/F1	2- 67	NOT MAIN CONTROL READ, BIT 04	$MCRD04
1A4A06	J04B-02*01	1A0B6-W1/W0	2- 67	NOT MAIN CONTROL READ, BIT 05	$MCRD05
1A4A06	J04B-04*03	1A0B4-E0/E1	2- 69	NOT MAIN CONTROL READ, BIT 06	$MCRD06
1A4A06	J04B-06*05	1A0B4-F0/F1	2- 69	NOT MAIN CONTROL READ, BIT 07	$MCRD07
1A4A06	J04B-08*07	1A0B4-W1/W0	2- 69	NOT MAIN CONTROL READ, BIT 08	$MCRD08
1A4A06	J04B-10*09	1A0B2-E0/E1	2- 71	NOT MAIN CONTROL READ, BIT 09	$MCRD09
1A4A06	J04C-02*01	1A0B2-F0/F1	2- 71	NOT MAIN CONTROL READ, BIT 10	$MCRD10
1A4A06	J04C-04*03	1A0B2-W1/W0	2- 71	NOT MAIN CONTROL READ, BIT 11	$MCRD11
1A4A06	J04C-06*05	1A0B0-E0/E1	2- 73	NOT MAIN CONTROL READ, BIT 12	$MCRD12
1A4A06	J04C-08*07	1A0B0-F0/F1	2- 73	NOT MAIN CONTROL READ, BIT 13	$MCRD13
1A4A06	J04C-10*09	1A0B0-W1/W0	2- 73	NOT MAIN CONTROL READ, BIT 14	$MCRD14
1A4A06	J04D-02/01	1A0A8-C0*C1	2- 55	NOT DO REGISTER BIT 00	$MCWR00
1A4A06	J04D-04/03	1A0A8-B0*B1	2- 55	NOT DO REGISTER BIT 01	$MCWR01
1A4A06	J04D-06/05	1A0A8-H0*H1	2- 55	NOT DO REGISTER BIT 02	$MCWR02
1A4A06	J04D-08/07	1A0A6-C0*C1	2- 57	NOT DO REGISTER BIT 03	$MCWR03
1A4A06	J04D-10/09	1A0A6-B0*B1	2- 57	NOT DO REGISTER BIT 04	$MCWR04
1A4A06	J04E-02/01	1A0A6-H0*H1	2- 57	NOT DO REGISTER BIT 05	$MCWR05
1A4A06	J04E-04/03	1A0A4-C0*C1	2- 59	NOT DO REGISTER BIT 06	$MCWR06
1A4A06	J04E-06/05	1A0A4-B0*B1	2- 59	NOT DO REGISTER BIT 07	$MCWR07
1A4A06	J04E-08/07	1A0A4-H0*H1	2- 59	NOT DO REGISTER BIT 08	$MCWR08
1A4A06	J04E-10/09	1A0A2-C0*C1	2- 61	NOT DO REGISTER BIT 09	$MCWR09
1A4A06	J04F-02/01	1A0A2-B0*B1	2- 61	NOT DO REGISTER BIT 10	$MCWR10
1A4A06	J04F-04/03	1A0A2-H0*H1	2- 61	NOT DO REGISTER BIT 11	$MCWR11
1A4A06	J04F-06/05	1A0A0-C0*C1	2- 63	NOT DO REGISTER BIT 12	$MCWR12
1A4A06	J04F-08/07	1A0A0-B0*B1	2- 63	NOT DO REGISTER BIT 13	$MCWR13
1A4A06	J06A-02*01	1A0A8-V0/V1	2- 55	SELECTED STATUS BIT 00 TO DO	$COPY00
1A4A06	J06A-04*03	1A0A8-X0/X1	2- 55	SELECTED STATUS BIT 01 TO DO	$COPY01
1A4A06	J06A-06*05	1A0A8-Q1/Q0	2- 55	SELECTED STATUS BIT 02 TO DO	$COPY02
1A4A06	J06A-08*07	1A0A6-V0/V1	2- 57	SELECTED STATUS BIT 03 TO DO	$COPY03
1A4A06	J06A-10*09	1A0A6-X0/X1	2- 57	SELECTED STATUS BIT 04 TO DO	$COPY04
1A4A06	J06B-02*01	1A0A6-Q1/Q0	2- 57	SELECTED STATUS BIT 05 TO DO	$COPY05
1A4A06	J06B-04*03	1A0A4-V0/V1	2- 59	SELECTED STATUS BIT 06 TO DO	$COPY06
1A4A06	J06B-06*05	1A0A4-X0/X1	2- 59	SELECTED STATUS BIT 07 TO DO	$COPY07
1A4A06	J06B-08*07	1A0A4-Q1/Q0	2- 59	SELECTED STATUS BIT 08 TO DO	$COPY08
1A4A06	J06B-10*09	1A0A2-V0/V1	2- 61	SELECTED STATUS BIT 09 TO DO	$COPY09
1A4A06	J06C-02*01	1A0A2-X0/X1	2- 61	SELECTED STATUS BIT 10 TO DO	$COPY10
1A4A06	J06C-04*03	1A0A2-Q1/Q0	2- 61	SELECTED STATUS BIT 11 TO DO	$COPY11
1A4A06	J06C-06*05	1A0A0-V0/V1	2- 63	NOT CHAN 0 INT MASK TO DO	$COPY12
1A4A06	J06C-08*07	1A0A0-X0/X1	2- 63	NOT CHAN 1 INT MASK TO DO	$COPY13
1A4A06	J06C-10*09	1A0A0-Q1/Q0	2- 63	NOT CHAN 2 INT MASK TO DO	$COPY14
1A4A06	J06D-02/01	1A0B8-B1*B0	2- 65	F0 REGISTER BIT 0	$F0BC00
1A4A06	J06D-04/03	1A0B8-D0*D1	2- 65	F0 REGISTER BIT 1	$F0BC01
1A4A06	J06D-06/05	1A0B8-K0*K1	2- 65	F0 REGISTER BIT 2	$F0BC02
1A4A06	J06D-08/07	1A0B6-B1*B0	2- 67	F0 REGISTER BIT 3	$F0BC03
1A4A06	J06D-10/09	1A0B6-D0*D1	2- 67	F0 REGISTER BIT 4	$F0BC04
1A4A06	J06E-02/01	1A0B4-B1*B0	2- 69	F0 REGISTER BIT 6	$F0BC06
1A4A06	J06E-04/03	1A0B4-D0*D1	2- 69	F0 REGISTER BIT 7	$F0BC07
1A4A06	J06E-06/05	1A0B4-K0*K1	2- 69	F0 REGISTER BIT 8	$F0BC08
1A4A06	J06E-08/07	1A0B2-B1*B0	2- 71	F0 REGISTER BIT 9	$F0BC09
1A4A06	J06E-10/09	1A0B2-D0*D1	2- 71	F0 REGISTER BIT 10	$F0BC10
1A4A06	J06F-02/01	1A0B2-K0*K1	2- 71	F0 REGISTER BIT 11	$F0BC11
1A4A06	J06F-04/03	1A0B0-B1*B0	2- 73	F0 REGISTER BIT 12	$F0BC12
1A4A06	J06F-06/05	1A0B0-D0*D1	2- 73	F0 REGISTER BIT 13	$F0BC13
1A4A06	J06F-08/07	1A0B0-K0*K1	2- 73	F0 REGISTER BIT 14	$F0BC14
1A4A06	J08A-02/01	1A0B8-P0*P1	2- 65	C2 BIT 0	$CFLT00
1A4A06	J08A-04/03	1A0B8-T0*T1	2- 65	C2 BIT 1	$CFLT01

CONNECTOR		ORIGIN	PAGE	DEFINITION	SIG NAME
1A4A06	J08A-06/05	1A0B8-Q0*Q1	2- 65	C2 BIT 2	$CFLT02
1A4A06	J08A-08/07	1A0B6-P0*P1	2- 67	C2 BIT 3	$CFLT03
1A4A06	J08A-10/09	1A0B6-T0*T1	2- 67	C2 BIT 4	$CFLT04
1A4A06	J08B-02/01	1A0B6-Q0*Q1	2- 67	C2 BIT 5	$CFLT05
1A4A06	J08B-04/03	1A0B4-P0*P1	2- 69	C2 BIT 6	$CFLT06
1A4A06	J08B-06/05	1A0B4-T0*T1	2- 69	C2 BIT 7	$CFLT07
1A4A06	J08B-08/07	1A0B4-Q0*Q1	2- 69	C2 BIT 8	$CFLT08
1A4A06	J08B-10/09	1A0B2-P0*P1	2- 71	C2 BIT 9	$CFLT09
1A4A06	J08C-02/01	1A0B2-T0*T1	2- 71	C2 BIT 10	$CFLT10
1A4A06	J08C-04/03	1A0B2-Q0*Q1	2- 71	C2 BIT 11	$CFLT11
1A4A06	J08C-06/05	1A0B0-P0*P1	2- 73	C2 BIT 12	$CFLT12
1A4A06	J08C-08/07	1A0B0-T0*T1	2- 73	C2 BIT 13	$CFLT13
1A4A06	J08C-10/09	1A0B0-Q0*Q1	2- 73	C2 BIT 14	$CFLT14
1A4A06	J08D-02*01	1A0A2-N2/N3	2- 61	INTERRUPT CODE BIT 0	$ICODE0
1A4A06	J08D-04*03	1A0A2-M2/M3	2- 61	INTERRUPT CODE BIT 1	$ICODE1
1A4A06	J08D-06*05	1A0A0-N2/N3	2- 63	INTERRUPT CODE BIT 2	$ICODE2
1A4A06	J08D-08*07	1A0A0-M2/M3	2- 63	INTERRUPT CODE BIT 3	$ICODE3
1A4A06	J08D-10*09	1A0A9-G0/G1	2- 75	INTERRUPT CODE BIT 4	$ICODE4
1A4A06	J08E-02*01	1A0A7-G0/G1	2- 77	INTERRUPT CODE BIT 5	$ICODE5
1A4A06	J10A-02*01	1B0A2-K2/K3	2- 31	NOT CHAN 3 INT MASK TO DO	$COPY15
1A4A06	J10A-04*03	1B0A2-J2/J3	2- 31	NOT CHAN 4 INT MASK TO DO	$COPY16
1A4A06	J10A-06*05	1B0A2-Q3/Q2	2- 31	NOT CHAN 5 INT MASK TO DO	$COPY17
1A4A06	J10A-08*07	1B0A1-K2/K3	2- 33	NOT CHAN 6 INT MASK TO DO	$COPY18
1A4A06	J10A-10*09	1B0A1-J2/J3	2- 33	NOT CHAN 7 INT MASK TO DO	$COPY19
1A4A06	J10B-02*01	1B0A1-Q3/Q2	2- 33	NOT CLOCK INT MASK TO DO	$COPY20
1A4A06	J10B-04*03	1B0A0-K2/K3	2- 35	NOT FP/BDP INT MASK TO DO	$COPY21
1A4A06	J10B-06*05	1B0A0-J2/J3	2- 35	NOT ARITH INT MASK TO DO	$COPY22
1A4A06	J10B-08*07	1B0A0-Q3/Q2	2- 35	NOT SRCH + MOVE INT MASK TO DO	$COPY23
1A4A06	J10B-10/09	1B0A2-E1*E0	2- 31	F0 REGISTER BIT 15	$F0BC15
1A4A06	J10C-02/01	1B0A2-N1*N0	2- 31	F0 REGISTER BIT 16	$F0BC16
1A4A06	J10C-04/03	1B0A2-W0*W1	2- 31	F0 REGISTER BIT 17	$F0BC17
1A4A06	J10C-06*05	1B0A2-Q1/Q0	2- 31	NOT MAIN CONTROL READ, BIT 15	$MCRD15
1A4A06	J10C-08*07	1B0A2-E2/E3	2- 31	NOT MAIN CONTROL READ, BIT 16	$MCRD16
1A4A06	J10C-10*09	1B0A2-V3/V2	2- 31	NOT MAIN CONTROL READ, BIT 17	$MCRD17
1A4A06	J10D-02*01	1B0A1-Q1/Q0	2- 33	NOT MAIN CONTROL READ, BIT 18	$MCRD18
1A4A06	J10D-04*03	1B0A1-E2/E3	2- 33	NOT MAIN CONTROL READ, BIT 19	$MCRD19
1A4A06	J10D-06*05	1B0A1-V3/V2	2- 33	NOT MAIN CONTROL READ, BIT 20	$MCRD20
1A4A06	J10D-08*07	1B0A0-Q1/Q0	2- 35	NOT MAIN CONTROL READ, BIT 21	$MCRD21
1A4A06	J10D-10*09	1B0A0-E2/E3	2- 35	NOT MAIN CONTROL READ, BIT 22	$MCRD22
1A4A06	J10E-02*01	1B0A0-V3/V2	2- 35	NOT MAIN CONTROL READ, BIT 23	$MCRD23
1A4A06	J10E-04/03	1B0A2-F1*F0	2- 31	DO REGISTER BIT 15	$MCWR15
1A4A06	J10E-06/05	1B0A2-Q0*Q1	2- 31	DO REGISTER BIT 16	$MCWR16
1A4A06	J10E-08/07	1B0A2-X0*X1	2- 31	DO REGISTER BIT 17	$MCWR17
1A4A06	J10E-10/09	1B0A1-F1*F0	2- 33	DO REGISTER BIT 18	$MCWR18
1A4A06	J10F-02/01	1B0A1-Q0*Q1	2- 33	DO REGISTER BIT 19	$MCWR19
1A4A06	J10F-04/03	1B0A1-X0*X1	2- 33	DO REGISTER BIT 20	$MCWR20
1A4A06	J10F-06/05	1B0A0-F1*F0	2- 35	DO REGISTER BIT 21	$MCWR21
1A4A06	J10F-08/07	1B0A0-Q0*Q1	2- 35	DO REGISTER BIT 22	$MCWR22
1A4A06	J12A-08/07	1B0B5-N0*N1	2- 5	RNI CYCLE LIGHT	$RNILT
1A4A06	J12A-10/09	1B0B5-V0*V1	2- 5	NOT (RAD CYCLE FF)	$RADLT
1A4A06	J12B-02/01	1B0B5-M1*M0	2- 5	NOT(ROP1 OR ROP2 CYCLE)	$ROPLT
1A4A06	J12B-04/03	1B0A2-C1*C0	2- 31	C2 BIT 15	$CFLT15
1A4A06	J12B-06/05	1B0A2-J1*J0	2- 31	C2 BIT 16	$CFLT16
1A4A06	J12B-08/07	1B0A2-T0*T1	2- 31	C2 BIT 17	$CFLT17
1A4A06	J12B-10/09	1B0A1-C1*C0	2- 33	C2 BIT 18	$CFLT18
1A4A06	J12C-02/01	1B0A1-J1*J0	2- 33	C2 BIT 19	$CFLT19
1A4A06	J12C-04/03	1B0A1-T0*T1	2- 33	C2 BIT 20	$CFLT20
1A4A06	J12C-06/05	1B0A0-C1*C0	2- 35	C2 BIT 21	$CFLT21
1A4A06	J12C-08/07	1B0A0-J1*J0	2- 35	C2 BIT 22	$CFLT22
1A4A06	J12C-10/09	1B0A0-T0*T1	2- 35	C2 BIT 23	$CFLT23
1A4A06	J12D-10/09	1C0A0-T0*T1	2- 37	MONITOR STATE	$MON-LT
1A4A06	J12E-03*	1B0A4-F0	2- 1	SLOW TIMING MARGIN	SLOW
1A4A06	J12E-04*	1B0A4-G0	2- 1	FAST TIMING MARGIN	FAST
1A4A06	J12E-05*	1C0A8-D2	3- 9	NOT (FAST TIMING SELECTED)	*FAST-A
1A4A06	J12E-06*	1C0A8-A3	3- 9	NOT (SLOW TIMING SELECTED)	*SLOW-A
1A4A06	J12E-09*	1C0B2-Q0	2- 51	SWITCH, TEST MODE	TSTMOD
1A4A06	J12F-02/01	1C0A2-I3*I2	2- 53	GATE C + F DIGITS 0-3	$CFGT03
1A4A06	J12F-04/03	1C0A2-J3*J2	2- 53	GATE C + F DIGIT 4	$CFGT4
1A4A06	J12F-06/05	1C0A2-C3*C2	2- 53	GATE C + F DIGITS 5-7	$CFGT57
1A4A06	J14A-02/01	1B0A1-E1*E0	2- 33	F0 REGISTER BIT 18	$F0BC18
1A4A06	J14A-04/03	1B0A1-N1*N0	2- 33	F0 REGISTER BIT 19	$F0BC19
1A4A06	J14A-06/05	1B0A1-W0*W1	2- 33	F0 REGISTER BIT 20	$F0BC20
1A4A06	J14A-08/07	1B0A0-E1*E0	2- 35	F0 REGISTER BIT 21	$F0BC21

NOTE:

BDP Cables for Panel 1A2A06 Locate on pages 9-21 thru 9-24.

CONNECTOR		ORIGIN	PAGE	DEFINITION	SIG NAME
1A4A06	J14A-10/09	1B0A0-N1*N0	2- 35	F0 REGISTER BIT 22	$F0BC22
1A4A06	J14B-02/01	1B0A0-W0*W1	2- 35	F0 REGISTER BIT 23	$F0BC23
1A4A06	J14B-04/03	1B0B5-C3*C2	2- 5	INIT. RNI 2 CYCLE FF	$BCRNI2
1A4A06	J14B-06/05	1B0A4-V3*V2	2- 1	REQUEST BC PULSE	$REQBC
1A4A06	J14B-08/07	1B0A4-S3*S2	2- 1	FUNCTION STABLE TO BLOCK CONT	$FNSTBC
1A4A06	J14B-10/09	1B0A4-Q0*Q1	2- 1	NOT(TEST BUSY) SIG TO B CONT)	$TSBSY
1A4A06	J14C-02/01	1B0B8-T0*T1	2- 11	D0 TO BLOCK CONT, BIT 18	$D0BC18
1A4A06	J14C-04/03	1B0B8-Q1*Q0	2- 11	D0 TO BLOCK CONT, BIT 19	$D0BC19
1A4A06	J14C-06/05	1B0B1-R2*R3	2- 9	D0 TO BLOCK CONT, BIT 21	$D0BC21
1A4A06	J14C-08/07	1B0B1-C2*C3	2- 9	D0 TO BLOCK CONT, BIT 22	$D0BC22
1A4A06	J14C-10/09	1B0B1-E3*E2	2- 9	NOT (D0 TO BLOCK CONT, BIT 23)	$D0BC23
1A4A06	J14D-02/01	1B0B8-Q2*Q3	2- 11	PAUSE FF TO 40 MS. DELAY	$T040MS
1A4A06	J14D-04/03	1B0B5-U3*U2	2- 5	OPERAND REFERENCE	$OPREF
1A4A06	J14D-06/05	1B0B5-E1*E0	2- 5	OPERAND REFERENCE	$OPREFS
1A4A06	J14D-08/07	1B0A5-F2*F3	2- 29	F0 REGISTER BIT 5	$F0BC05
1A4A06	J14D-10*09	1B0B4-P1/P0	2- 7	BC REPLY 2 TO MN CONT	$BCRPY2
1A4A06	J14E-02*01	1B0B1-J3/J2	2- 9	BC REPLY 1 TO MN CONT	$BCRPY1
1A4A06	J14E-04*03	1B0B2-V3/V2	2- 23	SELECTED CHAN BUSY + REJECT CONN + FCN	$CHBUSY
1A4A06	J14E-06*05	1B0B8-K1/K0	2- 11	SEL STATUS = ANY BIT OF F L12	$BCCMPR
1A4A06	J14E-08*07	1B0B8-C2/C3	2- 11	NOT F BIT 08 + 09 + 10 TO MN CONT	08091_0$
1A4A06	J14E-10/09	1B0B8-P2*P3	2- 11	BC NOT COMPARE FF	$BCSKIP
1A4A06	J14F-02*01	1B0B8-D3/D2	2- 11	FROM 40 MS DELAY	$FM40MS
1A4A06	J14F-04*03	1B0B1-F2/F3	2- 9	STORAGE NO RESPONSE	$NORESP
1A4A06	J14F-06/05	1B0A0-X0*X1	2- 35	DO REGISTER BIT I3	$MCWR23
1A4A06	J14F-07*	1A0B7-L1	2- 91	INTERRUPT BIAS SWITCH FOR BIT6	INTSW6
1A4A06	J14F-08*	1A0B7-K1	2- 91	INTERRUPT BIAS SWITCH FOR BIT7	INTSW7
1A4A06	J15A-01*	1C0B3-H2	2- 49		GOSYNC
1A4A06	J15A-02*	1C0B3-H3	2- 49	SWITCH, NOT GO	*GOSYNC
1A4A06	J15A-04*	1C0B3-I3	2- 49	SWITCH, STOP	STOPSW
1A4A06	J15A-05*	1C0B3-X3	2- 49	SWITCH, MASTER CLEAR	MCLR
1A4A06	J15A-08*	1C0B1-X0	2- 47	SWITCH, SWEEP PAGE FILE	SWEPPF
1A4A06	J15A-09*	1C0B1-N3	2- 47	SWITCH, ENTER PAGE FILE	ENTRPF
1A4A06	J15A-10*	1B0B9-S0	2- 17	SWITCH, ENTER B3	ENB3SW
1A4A06	J15B-01*	1B0B9-T0	2- 17	SWITCH, ENTER B2	ENB2SW
1A4A06	J15B-02*	1B0B9-T1	2- 17	SWITCH, ENTER B1	ENB1SW
1A4A06	J15B-03*	1C0A2-F0	2- 53	SWITCH, SELECT P REGISTER	PSELSW
1A4A06	J15B-04*	1C0A7-T1	3- 1	CONSOLE KYBD SEL SW, A REG	*ENTRA
1A4A06	J15B-05*	1C0A7-T0	3- 1	CONSOLE KYBD SEL SW, Q REG	*ENTRQ
1A4A06	J15B-06*	1C0B1-W1	2- 47	SWITCH, ENTER	ENTER
1A4A06	J15B-07*	1C0B1-X1	2- 47	SWITCH, SWEEP	SWEEP
1A4A06	J15B-08*	1C0B1-O3	2- 47	SWITCH, WRITE STORAGE OR RF	WSTO
1A4A06	J15B-09*	1C0B1-R3	2- 47	SWITCH, READ STORAGE OR RF	RSTO
1A4A06	J15C-01*	1C0B1-J3	2- 47	SWITCH, NOT (SWEEP-ENTER CONT)	*SWENCN
1A4A06	J15C-02*	1C0B1-I3	2- 47		SWENCN
1A4A06	J15C-03*	1C0A2-N1	2- 53	GROUND IF NO DIGIT SW PRESSED	*DIGIT
1A4A06	J15C-04*	1C0A2-O0	2- 53		DIGIT
1A4A06	J15C-05*	1B0B1-W1	2- 9	SWITCH TRANSLATION, BIT 0	DIGIT$_0$
1A4A06	J15C-06*	1B0B1-W0	2- 9	SWITCH TRANSLATION, BIT 1	DIGIT1
1A4A06	J15C-07*	1B0B1-Q1	2- 9	SWITCH TRANSLATION, BIT 2	DIGIT2
1A4A06	J15C-08*	1C0B1-M3	2- 47	SWITCH, KEYBOARD CLEAR	KYBCLR
1A4A06	J15C-09*	1C0B1-P0	2- 47	SWITCH, NOT TRANSFER	*TXFER
1A4A06	J15C-10*	1C0B1-O0	2- 47		TXFER
1A4A06	J15D-03*	1C0B3-Q2	2- 49	SWITCH, POWER ON MASTER CLEAR	POMCLR
1A4A06	J15D-09*	1C0B2-A0	2- 51	SWITCH, BREAKPOINT ON INSTR.	BPI
1A4A06	J15D-10*	1C0B2-B0	2- 51	BREAKPOINT SWITCH ON OPERAND	BPO
1A4A06	J15E-01*	1C0B1-G1	2- 47	SWITCH, REGISTER FILE SELECTED	REG
1A4A06	J15E-02*	1C0B1-G0	2- 47	SWITCH, STORAGE SELECTED	STO
1A4A06	J15E-04*	1A0B0-V2	2- 73	BREAK POINT SWITCH BIT 14	BPMC14
1A4A06	J15E-05*	1A0B0-K2	2- 73	BREAK POINT SWITCH BIT 13	BPMC13
1A4A06	J15E-06*	1A0B0-L2	2- 73	BREAK POINT SWITCH BIT 12	BPMC12
1A4A06	J15E-07*	1A0B2-V2	2- 71	BREAK POINT SWITCH BIT 11	BPMC11
1A4A06	J15E-08*	1A0B2-K2	2- 71	BREAK POINT SWITCH BIT 10	BPMC10
1A4A06	J15E-09*	1A0B2-L2	2- 71	BREAK POINT SWITCH BIT 9	BPMC09
1A4A06	J15E-10*	1A0B4-V2	2- 69	BREAK POINT SWITCH BIT 8	BPMC08
1A4A06	J15F-01*	1A0B4-K2	2- 69	BREAK POINT SWITCH BIT 7	BPMC07
1A4A06	J15F-02*	1A0B4-L2	2- 69	BREAK POINT SWITCH BIT 6	BPMC06
1A4A06	J15F-03*	1A0B6-V2	2- 67	BREAK POINT SWITCH BIT 5	BPMC05
1A4A06	J15F-04*	1A0B6-K2	2- 67	BREAK POINT SWITCH BIT 4	BPMC04
1A4A06	J15F-05*	1A0B6-L2	2- 67	BREAK POINT SWITCH BIT 3	BPMC03
1A4A06	J15F-06*	1A0B8-V2	2- 65	BREAK POINT SWITCH BIT 2	BPMC02
1A4A06	J15F-07*	1A0B8-K2	2- 65	BREAK POINT SWITCH BIT 1	BPMC01
1A4A06	J15F-08*	1A0B8-L2	2- 65	BREAK POINT SWITCH BIT 0	BPMC00
1A4A06	J17A-01*	1B0B3-T3	2- 3	CONSOLE SWITCH, BDP MODE	BDPSW
1A4A06	J17A-02*	1C0B0-E1	2- 45	CONSOLE SWITCH, EXEC MODE	EXECMD
1A4A06	J17A-03*	1B0A5-J0	2- 29	SWITCH, JUMP 1	JSW1
1A4A06	J17A-04*	1B0A5-I1	2- 29	SWITCH, JUMP 2	JSW2
1A4A06	J17A-05*	1C0B3-D3	2- 49		CYCSTP
1A4A06	J17A-06*	1C0B3-C3	2- 49	SWITCH, NOT CYCLE STEP	*CYCSTP
1A4A06	J17A-09*	1C0B2-P1	2- 51	SWITCH, SELECTIVE STOP	SLSSW
1A4A06	J17B-02*	1A1A0-S1	3- 89	DISPLAY Q REG	*SHOWQ
1A4A06	J17B-03*	1A1A0-R1	3- 89	DISPLAY E UPPER REG	*SHOWEU
1A4A06	J17B-04*	1A1A0-R0	3- 89	DISPLAY E LOWER REG	*SHOWEL
1A4A06	J17B-05*	1C0B3-U1	2- 49	SWITCH, PARITY INTERRUPT	PARINT
1A4A06	J17B-06*	1C0B3-X0	2- 49	SWITCH, PARITY STOP	PARSTP
1A4A06	J17B-07*	1B0A5-J1	2- 29	SWITCH, JUMP 3	JSW3
1A4A06	J17B-08*	1B0A5-I0	2- 29	SWITCH, JUMP 4	JSW4
1A4A06	J17B-09*	1C0B3-M3	2- 49		AUTOST
1A4A06	J17B-10*	1C0B3-L2	2- 49	SWITCH, NOT AUTO STEP	*AUTOST
1A4A06	J17C-02*	1B0B4-U1	2- 7	SWITCH, DISABLE ADVANCE P	DVPSW
1A4A06	J17C-03*	1C0B2-W3	2- 51		AUDPSW
1A4A06	J17C-04*	1C0B2-V3	2- 51	SWITCH, NOT AUTO DUMP	*AUDPSW
1A4A06	J17C-08*	1C0A2-F1	2- 53	SWITCH, DISPLAY F REG	PREGSW
1A4A06	J17C-09*	1A0A0-Q2	2- 63	SWITCH, DISPLAY LJA REG	LJASW
1A4A06	J17C-10*	1C0A2-D1	2- 53	SWITCH, DISPLAY CIR	CIRSW
1A4A06	J17D-01*	1B0A5-K0	2- 29	SWITCH, JUMP 5	JSW5
1A4A06	J17D-02*	1B0A5-H1	2- 29	SWITCH, JUMP 6	JSW6
1A4A06	J17D-03*	1C0B3-E2	2- 49		INSTEP
1A4A06	J17D-04*	1C0B3-E3	2- 49	SWITCH, NOT INSTRUCTION STEP	*INSTEP
1A4A06	J17D-05*	1C0B3-X2	2- 49	SWITCH, EXTERNAL CLEAR	EXCLR
1A4A06	J17D-06*	1C0B3-Q3	2- 49	SWITCH, INTERNAL CLEAR	INCLR
1A4A06	J17D-07*	1C0B2-R2	2- 51		AULDSW
1A4A06	J17D-08*	1C0B2-U3	2- 51	SWITCH, NOT AUTO LOAD	*AULDSW
1A4A06	J17E-04*	1B0A7-C3	2- 15	SWITCH, DISPLAY B2	DSPYB2
1A4A06	J17E-05*	1B0A7-C2	2- 15	SWITCH, DISPLAY B3	DSPYB3
1A4A06	J17E-07*	1C0A3-C0	2- 39	SET SWITCH, ISR, BIT 0	ISR0
1A4A06	J17E-08*	1C0A3-C1		SET SWITCH, ISR, BIT 1	ISR1
1A4A06	J17E-09*	1C0A3-B0	2- 39	SET SWITCH, ISR, BIT 2	ISR2
1A4A06	J17E-10*	1C0A3-B1	2- 39	CLR SWITCH, ISR	CLRISR
1A4A06	J17F-01*	1C0A3-H1	2- 39	SET SWITCH, OSR, BIT 0	OSR0
1A4A06	J17F-02*	1C0A3-H0	2- 39	SET SWITCH, OSR, BIT 1	OSR1
1A4A06	J17F-03*	1C0A3-K1	2- 39	SET SWITCH, OSR, BIT 2	OSR2
1A4A06	J17F-04*	1C0A3-K0	2- 39	CLR SWITCH, OSR	CLROSR
1A4A06	J18A-02/01	1C1B8-E0*E1	3- 17	SET DIVIDE FAULT FF	$STDIVF
1A4A06	J18A-04/03	1C1B9-H1*H0	3- 19	SET OVERFLOW FF	$STOVER
1A4A06	J18A-06/05	1C1B7-S1*S0	3- 15	NOT BIT 09 OF MAINT.REGISTER	$M0BC09
1A4A06	J18A-08/07	1C1B7-R1*R0	3- 15	NOT BIT 10 OF MAINT.REGISTER	$M0BC10
1A4A06	J18A-10/09	1C0B0-C0*C1	2- 45	NOT (EXEC MODE) SIGNAL TO B.C.	$BCEXMO
1A4A06	J18B-02/01	1C0B3-T2*T3	2- 49	NOT (MASTER CLR +EXTERNAL CLR)	$EXCLBC
1A4A06	J18B-04/03	1C0B3-S2*S3	2- 49	NOT (MASTER CLR +INTERNAL CLR)	$INCLBC
1A4A06	J18B-06/05	1C0B0-F2*F3	2- 45	READ OR WRITE REGISTER FILE	$RWRF
1A4A06	J18B-07*	1C1B7-W2	3- 15	NOT (SEL. BITS 08-15 OF MAINT)	MILT-2
1A4A06	J18B-08*	1C1B7-X3	3- 15	NOT (SEL. BITS 16-23 OF MAINT)	MOLT-3
1A4A06	J18C-02*01	1C0B2-R1/R0	2- 51	AUTO-STEP OSCILLATOR	$ASOSC
1A4A06	J18C-04*03	1C0B2-T1/T0	2- 51	NOT CHAN 0-7 TERMINATE TO BC	$CHTERM
1A4A06	J18C-06/05	1C0B3-K0*K1	2- 49	NOT (GO FF) TO BC	$GO-BC
1A4A06	J18C-08/07	1C0A4-F3*F2	2- 41	INTERRUPT ENABLED FF	$IEN-LT
1A4A06	J18C-10/09	1C0A0-E0*E1	2- 37	OSR BACKGROUND LIGHT	$OSR-LT
1A4A06	J18D-02/01	1C0A0-G1*G0	2- 37	STOR CYCLE TO INDICATOR	$STOLT
1A4A06	J18D-04/03	1C0A0-S0*S1	2- 37	PROGRAM STATE	$PRO-LT

Channel ↑ Destination ↑ Origin

No Sign = Logical Level $ = twisted Pair

* ground or oper signal

817

CONNECTOR		ORIGIN
1A4A06	J18D-06/05	1C1B7-Q2*Q3
1A4A06	J18D-08/07	1A1B6-N3*O2
1A4A06	J18D-10/09	1A1B6-R3*R2
1A4A06	J18E-02/01	1A1B6-T2*T3
1A4A06	J18E-04/03	1C1B7-V0*V1
1A4A06	J18E-06/05	1C1B7-T0*T1
1A4A06	J18E-08/07	1C1B7-U0*U1
1A4A06	J18E-10/09	1C1B7-Q0*Q1
1A4A06	J18F-02/01	1C1B7-M2*M3
1A4A06	J18F-04/03	1C1B7-P3*P2
1A4A06	J18F-06/05	1C1B7-L2*L3
1A4A06	J18F-07*	1C1B6-L1
1A4A06	J18F-08*	1C1B7-X2
1A4A06	J20A-02*01	1C0A1-X2/X3
1A4A06	J20A-04*03	1C0A1-N0/N1
1A4A06	J20A-06*05	1C0B3-W1/W0
1A4A06	J20A-08/07	1C0A0-Q1*Q0
1A4A06	J20A-10/09	1C0A0-I0*I1
1A4A06	J20B-02/01	1C0A0-O0*O1
1A4A06	J20B-04/03	1C0A0-M0*M1
1A4A06	J20B-06/05	1C0A0-L1*L0
1A4A06	J20B-08*07	1C0A1-W1/W0
1A4A06	J20B-10/09	1C0A0-U3*U2
1A4A06	J20C-02/01	1C0A0-R3*R2
1A4A06	J20C-04/03	1C0A0-T2*T3
1A4A06	J20C-06/05	1C0A0-S3*S2
1A4A06	J20C-08/07	1C0A0-H2*H3
1A4A06	J20C-10/09	1C0A1-N3*N2
1A4A06	J20D-02/01	1C0A3-M1*M0
1A4A06	J20D-04/03	1C0A3-T1*T0
1A4A06	J20D-06/05	1C0A3-S1*S0
1A4A06	J20D-08/07	1C0A1-C1*C0
1A4A06	J20D-10*09	1C0A1-K1/K0
1A4A06	J20E-02/01	1C0A1-D2*D3
1A4A06	J20E-04*03	1C0A1-S1/S0
1A4A06	J20E-06/05	1C0A4-C2*C3
1A4A06	J20E-08/07	1C0A3-U3*U2
1A4A06	J20E-10/09	1C0A3-R2*R3
1A4A06	J20F-02/01	1C0A3-L2*L3
1A4A06	J20F-04/03	1C0B0-F0*F1
1A4A06	J20F-06/05	1C0B3-W3*W2
1A4A06	J20F-08/07	1C0B3-S0*S1
1A4A06	P01A-02/01	1A0B8-M3*M2
1A4A06	P01A-04/03	1A0B8-P3*P2
1A4A06	P01A-06/05	1A0B8-S2*S3
1A4A06	P01A-08/07	1A0B6-M3*M2
1A4A06	P01A-10/09	1A0B6-P3*P2
1A4A06	P01B-02/01	1A0B6-S2*S3
1A4A06	P01B-04/03	1A0B4-M3*M2
1A4A06	P01B-06/05	1A0B4-P3*P2
1A4A06	P01B-08/07	1A0B4-S2*S3
1A4A06	P01B-10/09	1A0B2-M3*M2
1A4A06	P01C-02/01	1A0B2-P3*P2
1A4A06	P01C-04/03	1A0B2-S2*S3
1A4A06	P01C-06/05	1A0B0-M3*M2
1A4A06	P01C-08/07	1A0B0-P3*P2
1A4A06	P01C-10/09	1A0B0-S2*S3
1A4A06	P01D-02/01	1A2A8-F1*E0
1A4A06	P01D-04/03	1B1B4-V1*V0
1A4A06	P01D-06/05	1B0A8-T2*T3
1A4A06	P01D-08/07	1B0B4-R0*R1
1A4A06	P01D-10*09	1B0B7-S0/S1
1A4A06	P01E-02*01	1B0B7-W2/W3
1A4A06	P01E-04*03	1A2A1-L1/L0
1A4A06	P01E-06/05	1A2A1-R2*R3
1A4A06	P01E-08/07	1A0A0-H0*H1
1A4A06	P01E-10*09	1B0B7-X1/X0
1A4A06	P02A-02/01	1A1B2-T1*T0

PAGE	DEFINITION	SIG NAME
3- 15	MAINTENANCE LIGHTS BIT 07	$M1LT07
3- 51	BIT 00 OF A	$A0BC0
3- 51	BIT 01 OF A	$A0BC1
3- 51	BIT 02 OF A	$A0BC2
3- 15	MAINTENANCE LIGHTS BIT 00	$M1LT00
3- 15	MAINTENANCE LIGHTS BIT 01	$M1LT01
3- 15	MAINTENANCE LIGHTS BIT 02	$M1LT02
3- 15	MAINTENANCE LIGHTS BIT 03	$M1LT03
3- 15	MAINTENANCE LIGHTS BIT 04	$M1LT04
3- 15	MAINTENANCE LIGHTS BIT 05	$M1LT05
3- 15	MAINTENANCE LIGHTS BIT 06	$M1LT06
3- 13		MAINT
3- 15	NOT (SEL. BITS 00-07 OF MAINT)	M0LT-I
2- 43	SET ILLEGAL WRITE	$SETIW
2- 43	BLOCK CONTROL PRIORITY	$BCPRI0
2- 49	STORAGE PARITY ERROR INTERRUPT	$MPEINT
2- 37	MONITOR STATE	$MONREF
2- 37	MAIN CONT WRITE SIGNAL TO PF	$MCWR
2- 37	WRITE PF	$WPF
2- 37	READ PF	$RPF
2- 37	STORE CYCLE,INT. PROCESSING	$INTST0
2- 43	INTERRUPT CODE BIT 6	$ICODE6
2- 37	MC PARTIAL WRITE BIT 0	$MCPW0
2- 37	MC PARTIAL WRITE BIT 1	$MCPW1
2- 37	MC PARTIAL WRITE BIT 2	$MCPW2
2- 37	MC PARTIAL WRITE BIT 3	$MCPW3
2- 37	MC PARTIAL WRITE BIT4 OR DESTRUCTIVE LOAD	$MCPW4
2- 43	NOT READ ADDRESS CYCLE	$RADREF
2- 39	C4 FAN IN BIT 0(S BUS BIT 15)	$MCSB15
2- 39	C4 FAN IN BUT 1(S BUS BIT 16)	$MCSB16
2- 39	C4 FAN IN BIT 2(S BUS BIT 17)	$MCSB17
2- 43	NORMAL INTERRUPT CODE USED	$ICSEEN
2- 43	(NORMAL INTERRUPTS)(ARITH)	$INFINT
2- 43	NOT(EN PAR ERR CODE + M CLR)	$ENPEC0
2- 43	NORMAL INT XLTN TO MN CONT	$NORINT
2- 41	INTERRUPT ENABLED FF	$INTEN
2- 39	CIR,BIT 0	$CIRBC0
2- 39	CIR,BIT 1	$CIRBC1
2- 39	CIR,BIT 2	$CIRBC2
2- 45	NOT (EXECUTIVE MODE)	$PFEXM0
2- 49	NOT (MASTER CLR +INTERNAL CLR)	$MCLPF
2- 49	DISABLE MEMORY PARITY ERROR	$DISMPE
2- 65	S6(S BUS) BIT 00	$MCSB00
2- 65	S6(S BUS) BIT 01	$MCSB01
2- 65	S6(S BUS) BIT 02	$MCSB02
2- 67	S6(S BUS) BIT 03	$MCSB03
2- 67	S6(S BUS) BIT 04	$MCSB04
2- 67	S6(S BUS) BIT 05	$MCSB05
2- 69	S6(S BUS) BIT 06	$MCSB06
2- 69	S6(S BUS) BIT 07	$MCSB07
2- 69	S6(S BUS) BIT 08	$MCSB08
2- 71	S6(S BUS) BIT 09	$MCSB09
2- 71	S6(S BUS) BIT 10	$MCSB10
2- 71	S6(S BUS) BIT 11	$MCSB11
2- 73	S6(S BUS) BIT 12	$MCSB12
2- 73	S6(S BUS) BIT 13	$MCSB13
2- 73	S6(S BUS) BIT 14	$MCSB14
4- 21	(BCD FAULT)(BDP COMPLETE)(H03)	$STBCDF
3-115	SET EXPONENT FAULT	$STEXPO
2- 13	(FIRST OPERAND)(DP INST.)	$MCDP
2- 7	MC REQUEST PAGE FILE	$MCRQPF
2- 19	PF ADDR REPLY TO MN CONTROL	$PFARMC
2- 19	NOT DATA REPLY TO MAIN CONTROL	$PFDRMC
4- 11	LEGAL WRITE FOR BDP	$LWRBDP
4- 11	READ C OPERAND REQUEST(EDIT+67(0+1))	$FIELDC
2- 63	NOT DO REGISTER BIT 14	$MCWR14
2- 19	(PF TIME 5)(MAIN CONT PRIORITY IN PF)	PFT5MC
3- 79	NOT BIT 00 OF A1+Q1+E1+E2	$AELT00

CONNECTOR		ORIGIN
1A4A06	P02A-04/03	1A1B2-U1*U0
1A4A06	P02A-06/05	1A1B2-T3*T2
1A4A06	P02A-08/07	1A1B2-U3*U2
1A4A06	P02A-10/09	1A1B1-T1*T0
1A4A06	P02B-02/01	1A1B1-U1*U0
1A4A06	P02B-04/03	1A1B1-T3*T2
1A4A06	P02B-06/05	1A1B1-U3*U2
1A4A06	P02B-08/07	1A1B0-T1*T0
1A4A06	P02B-10/09	1A1B0-U1*U0
1A4A06	P02C-02/01	1A1B0-T3*T2
1A4A06	P02C-04/03	1A1B0-U3*U2
1A4A06	P02C-06/05	1A1A2-T1*T0
1A4A06	P02C-08/07	1A1A2-U1*U0
1A4A06	P02C-10/09	1A1A2-T3*T2
1A4A06	P02D-02/01	1A1A2-U3*U2
1A4A06	P02D-04/03	1A1A1-T1*T0
1A4A06	P02D-06/05	1A1A1-U1*U0
1A4A06	P02D-08/07	1A1A1-T3*T2
1A4A06	P02D-10/09	1A1A1-U3*U2
1A4A06	P02E-02/01	1A1A0-T1*T0
1A4A06	P02E-04/03	1A1A0-U1*U0
1A4A06	P02E-06/05	1A1A0-T3*T2
1A4A06	P02E-08/07	1A1A0-U3*U2
1A4A06	P02E-09*	1A2A4-Q0
1A4A06	P02E-10*	1A2A4-R1
1A4A06	P02F-01*	1A2A0-02
1A4A06	P04A-02/01	1C0A3-O1*O0
1A4A06	P04A-04/03	1C0A3-N0*N1
1A4A06	P04A-06/05	1C0A3-P1*P0
1A4A06	P04A-08/07	1C0A3-J1*J0
1A4A06	P04A-10/09	1C0A3-Q1*Q0
1A4A06	P04B-02/01	1C0A3-L1*L0
1A4A06	P04B-04/03	1C0A3-V3*V2
1A4A06	P04B-06/05	1C0A3-P2*P3
1A4A06	P04B-08/07	1C0A3-M2*M3
1A4A06	P04B-10/09	1C0B2-N1*N0
1A4A06	P04C-02/01	1C0B2-L0*L1
1A4A06	P04C-04/03	1C0A2-L2*L3
1A4A06	P04D-02/01	1C0B1-F0*F1
1A4A06	P04D-04/03	1C0B3-J1*J0
1A4A06	P04D-06/05	1C0B3-L1*L0
1A4A06	P04D-08/07	1C0B3-O0*O1
1A4A06	P04D-04/03	1C0B3-J1*J0
1A4A06	P04D-06/05	1C0B3-L1*L0
1A4A06	P04D-08/07	1C0B3-O0*O1
1A4A06	P04E-02/01	1C0A2-G3*G2
1A4A06	P04E-04/03	1C0A2-V3*V2
1A4A06	P04E-06/05	1C0A2-V0*V1
1A4A06	P04E-08/07	1C0A2-W1*W0
1A4A06	P04E-10/09	1C0A2-N3*O2
1A4A06	P04F-02/01	1C0A2-P2*P3
1A4A06	P04F-04/03	1C0A2-R3*R2
1A4A06	P04F-06/05	1C0A2-S3*S2
1A4A06	P04F-08/07	1C0A2-W2*W3
2A1A06	J03A-02/01	2A2A8-U3*U2
2A1A06	J03A-04/03	2A2A9-U3*U2
2A1A06	J03A-06/05	2A2A8-R3*R2
2A1A06	J03A-08/07	2A2A9-R3*R2
2A1A06	J03A-10/09	2A2A8-P0*P1
2A1A06	J03B-02/01	2A2A9-P0*P1
2A1A06	J03B-04/03	2A2B4-R0*B1
2A1A06	J03B-06/05	2A2A9-M1*M0
2A1A06	J03B-08/07	2A2A8-M1*M0
2A1A06	J03B-10/09	2A2B8-S3*S2
2A1A06	J03C-02/01	2A2B8-R3*R2
2A1A06	J03C-04/03	2A2B7-J0*J1
2A1A06	J03C-06/05	2A2B7-J3*J2
2A1A06	J03C-08/07	2A2B6-J0*J1
2A1A06	J03C-10/09	2A2B6-J3*J2
2A1A06	J03D-02/01	2A2B5-J0*J1
2A1A06	J03D-04/03	2A2B5-J3*J2
2A1A06	J03D-06/05	2A2B4-R2*R3
2A1A06	J03D-08/07	2B2B9-B3*B2
2A1A06	J03D-10/09	2B2B9-E2*E3
2A1A06	J03E-02/01	2B2B8-B3*B2
2A1A06	J03E-04/03	2B2B8-E2*E3
2A1A06	J03E-06/05	2B2B8-M3*M2

PAGE	DEFINITION	SIG NAME
3- 79	NOT BIT 01 OF A1+Q1+E1+E2	$AELT01
3- 79	NOT BIT 02 OF A1+Q1+E1+E2	$AELT02
3- 79	NOT BIT 03 OF A1+Q1+E1+E2	$AELT03
3- 81	NOT BIT 04 OF A1+Q1+E1+E2	$AELT04
3- 81	NOT BIT 05 OF A1+Q1+E1+E2	$AELT05
3- 81	NOT BIT 06 OF A1+Q1+E1+E2	$AELT06
3- 81	NOT BIT 07 OF A1+Q1+E1+E2	$AELT07
3- 83	NOT BIT 08 OF A1+Q1+E1+E2	$AELT08
3- 83	NOT BIT 09 OF A1+Q1+E1+E2	$AELT09
3- 83	NOT BIT 10 OF A1+Q1+E1+E2	$AELT10
3- 83	NOT BIT 11 OF A1+Q1+E1+E2	$AELT11
3- 85	NOT BIT 12 OF A1+Q1+E1+E2	$AELT12
3- 85	NOT BIT 13 OF A1+Q1+E1+E2	$AELT13
3- 85	NOT BIT 14 OF A1+Q1+E1+E2	$AELT14
3- 85	NOT BIT 15 OF A1+Q1+E1+E2	$AELT15
3- 87	NOT BIT 16 OF A1+Q1+E1+E2	$AELT16
3- 87	NOT BIT 17 OF A1+Q1+E1+E2	$AELT17
3- 87	NOT BIT 18 OF A1+Q1+E1+E2	$AELT18
3- 87	NOT BIT 19 OF A1+Q1+E1+E2	$AELT19
3- 89	NOT BIT 20 OF A1+Q1+E1+E2	$AELT20
3- 89	NOT BIT 21 OF A1+Q1+E1+E2	$AELT21
3- 89	NOT BIT 22 OF A1+Q1+E1+E2	$AELT22
3- 89	NOT BIT 23 OF A1+Q1+E1+E2	$AELT23
4- 3	BDP FAST MARGIN	*BPFSMG
4- 3	BDP SLOW MARGIN	*BPSLMG
4- 27	CC-MR SWITCH IN CC POSITION	BT13OR
2- 39	ISR ,BIT 0	$ISRLT0
2- 39	ISR ,BIT 1	$ISRLT1
2- 39	ISR ,BIT 2	$ISRLT2
2- 39	OSR ,BIT 0	$OSRLT0
2- 39	OSR ,BIT 1	$OSRLT1
2- 39	OSR ,BIT 2	$OSRLT2
2- 39	B DISPLAY, BIT 0	$B-LT00
2- 39	B DISPLAY, BIT 1	$B-LT01
2- 39	B DISPLAY, BIT 2	$B-LT02
2- 51	AUTO LOAD LIGHT	$AL-LT
2- 51	AUTO DUMP LIGHT	$AD-LT
2- 53	GATE A,Q,E REGISTER DISPLAY	$AQBGT
2- 47	SWEEP-ENTER CONTINUOUS FF SET	$SECNLT
2- 49	NOT (GO FF)	$GO-LT
2- 49	STOP FF	$STOPLT
2- 49	MEMORY ERROR FF	$MPE-LT
2- 53	CO DISPLAY INDICATOR	$C0-LT
2- 53	BOUNCING BALL, OCTAL DIGIT 7	$BB-LT7
2- 53	BOUNCING BALL, OCTAL DIGIT 0	$BB-LT0
2- 53	BOUNCING BALL, OCTAL DIGIT 1	$BB-LT1
2- 53	BOUNCING BALL, OCTAL DIGIT 2	$BB-LT2
2- 53	BOUNCING BALL, OCTAL DIGIT 3	$BB-LT3
2- 53	BOUNCING BALL, OCTAL DIGIT 4	$BB-LT4
2- 53	BOUNCING BALL, OCTAL DIGIT 5	$BB-LT5
2- 53	BOUNCING BALL, OCTAL DIGIT 6	$BB-LT6
5- 9	ADDR BIT 00 TO INTERNAL STOR A	$INS00A
5- 11	ADDR BIT 01 TO INTERNAL STOR A	$INS01A
5- 9	ADDR BIT 02 TO INTERNAL STOR A	$INS02A
5- 11	ADDR BIT 03 TO INTERNAL STOR A	$INS03A
5- 9	ADDR BIT 04 TO INTERNAL STOR A	$INS04A
5- 11	ADDR BIT 05 TO INTERNAL STOR A	$INS05A
5- 21	ADDR BIT 06 TO INTERNAL STOR A	$INS06A
5- 11	ADDR BIT 07 TO INTERNAL STOR A	$INS07A
5- 9	ADDR BIT 08 TO INTERNAL STOR A	$INS08A
5- 13	ADDR BIT 09 TO INTERNAL STOR A	$INS09A
5- 13	ADDR BIT 10 TO INTERNAL STOR A	$INS10A
5- 15	ADDR BIT 11 TO INTERNAL STOR A	$INS11A
5- 15	ADDR BIT 12 TO INTERNAL STOR A	$INS12A
5- 17	ADDR BIT 13 TO INTERNAL STOR A	$INS13A
5- 17	ADDR BIT 14 TO INTERNAL STOR A	$INS14A
5- 19	ADDR BIT 15 TO INTERNAL STOR A	$INS15A
5- 19	ADDR BIT 16 TO INTERNAL STOR A	$INS16A
5- 21	ADDR BIT 17 TO INTERNAL STOR A	$INS17A
5- 75	PART. WR. BIT 0 TO INT STOR A	$INPW0A
5- 75	PART. WR. BIT 1 TO INT STOR A	$INPW1A
5- 77	PART. WR. BIT 2 TO INT STOR A	$INPW2A
5- 77	PART. WR. BIT 3 TO INT STOR A	$INPW3A
5- 77	PART. WR. BIT 4 TO INT STOR A	$INPW4A

Destination ↑ origin ↑

Chassis "D"

No sign = Logical level.

$ = twisted pair.

* = ground or open signal

419

CONNECTOR		ORIGIN	PAGE	DEFINITION	SIG NAME
2A1A06	J03E-08/07	2A2A7-F0*F1	5- 5	REQUEST TO INTERNAL STORAGE A	$RQINMA
2A1A06	J03E-10*09	2A2A7-D2/D3	5- 5	ADDR REPLY FROM INT STOR A	$INMARA
2A1A06	J03F-02*01	2B2B8-U2/U3	5- 77	ADDR PAR. ERR. FROM INT STOR A	$INAPEA
2A1A06	J03F-04/03	2A2B9-J1*J0	5- 23	MASTER CLEAR INTERNAL STOR A	$CLINMA
2A1A06	J03F-06/05	2A2B9-L1*L0	5- 23	ADDR LWR PAR BIT TO INT STOR A	$INSLPA
2A1A06	J03F-08*07	2A2B9-W1/W0	5- 23	INTERNAL STOR A NO RESPONSE	$INDNRA
2A1A06	J05A-02/01	2A2A8-P3*P2	5- 9	ADDR BIT 00 TO INTERNAL STOR B	$INS00B
2A1A06	J05A-04/03	2A2A9-P3*P2	5- 11	ADDR BIT 01 TO INTERNAL STOR B	$INS01B
2A1A06	J05A-06/05	2A2A8-Q2*Q3	5- 9	ADDR BIT 02 TO INTERNAL STOR B	$INS02B
2A1A06	J05A-08/07	2A2A9-Q2*Q3	5- 11	ADDR BIT 03 TO INTERNAL STOR B	$INS03B
2A1A06	J05A-10/09	2A2A8-K0*K1	5- 9	ADDR BIT 04 TO INTERNAL STOR B	$INS04B
2A1A06	J05B-02/01	2A2A9-K0*K1	5- 11	ADDR BIT 05 TO INTERNAL STOR B	$INS05B
2A1A06	J05B-04/03	2A2B4-C0*C1	5- 21	ADDR BIT 06 TO INTERNAL STOR B	$INS06B
2A1A06	J05B-06/05	2A2A9-L0*L1	5- 11	ADDR BIT 07 TO INTERNAL STOR B	$INS07B
2A1A06	J05B-08/07	2A2A8-L0*L1	5- 9	ADDR BIT 08 TO INTERNAL STOR B	$INS08B
2A1A06	J05B-10/09	2A2B8-U2*U3	5- 13	ADDR BIT 09 TO INTERNAL STOR B	$INS09B
2A1A06	J05C-02/01	2A2B8-X2*X3	5- 13	ADDR BIT 10 TO INTERNAL STOR B	$INS10B
2A1A06	J05C-04/03	2A2B7-L0*L1	5- 15	ADDR BIT 11 TO INTERNAL STOR B	$INS11B
2A1A06	J05C-06/05	2A2B7-K2*K3	5- 15	ADDR BIT 12 TO INTERNAL STOR B	$INS12B
2A1A06	J05C-08/07	2A2B6-L0*L1	5- 17	ADDR BIT 13 TO INTERNAL STOR B	$INS13B
2A1A06	J05C-10/09	2A2B6-K2*K3	5- 17	ADDR BIT 14 TO INTERNAL STOR B	$INS14B
2A1A06	J05D-02/01	2A2B5-L0*L1	5- 19	ADDR BIT 15 TO INTERNAL STOR B	$INS15B
2A1A06	J05D-04/03	2A2B5-K2*K3	5- 19	ADDR BIT 16 TO INTERNAL STOR B	$INS16B
2A1A06	J05D-06/05	2A2B4-X2*X3	5- 21	ADDR BIT 17 TO INTERNAL STOR B	$INS17B
2A1A06	J05D-08/07	2B2B9-C3*C2	5- 75	PART. WR. BIT 0 TO INT STOR B	$INPW0B
2A1A06	J05D-10/09	2B2B9-D2*D3	5- 75	PART. WR. BIT 1 TO INT STOR B	$INPW1B
2A1A06	J05E-02/01	2B2B8-C3*C2	5- 77	PART. WR. BIT 2 TO INT STOR B	$INPW2B
2A1A06	J05E-04/03	2B2B8-D2*D3	5- 77	PART. WR. BIT 3 TO INT STOR B	$INPW3B
2A1A06	J05E-06/05	2B2B8-N3*N2	5- 77	PART. WR. BIT 4 TO INT STOR B	$INPW4B
2A1A06	J05E-08/07	2A2A7-I0*I1	5- 5	REQUEST TO INTERNAL STORAGE B	$RQINMB
2A1A06	J05E-10*09	2A2A7-C2/C3	5- 5	ADDR REPLY FROM INT STOR B	$INMARB
2A1A06	J05F-02*01	2B2B8-W3/W2	5- 77	ADDR PAR. ERR. FROM INT STOR B	$INAPEB
2A1A06	J05F-04/03	2A2B9-01*00	5- 23	MASTER CLEAR INTERNAL STOR B	$CLINMB
2A1A06	J05F-06/05	2A2B9-H1*H0	5- 23	ADDR LWR PAR BIT TO INT STOR B	$INSLPB
2A1A06	J05F-08*07	2A2B9-X1/X0	5- 23	INTERNAL STOR B NO RESPONSE	$INDNRB
2A1A06	J06A-02*01	2A2B7-F3/F2	5- 15	S6(S BUS) BIT 00	$MCSB00
2A1A06	J06A-04*03	2A2B7-G3/G2	5- 15	S6(S BUS) BIT 01	$MCSB01
2A1A06	J06A-06*05	2A2B6-F3/F2	5- 17	S6(S BUS) BIT 02	$MCSB02
2A1A06	J06A-08*07	2A2B6-G3/G2	5- 17	S6(S BUS) BIT 03	$MCSB03
2A1A06	J06A-10*09	2A2B5-F3/F2	5- 19	S6(S BUS) BIT 04	$MCSB04
2A1A06	J06B-02*01	2A2B5-G3/G2	5- 19	S6(S BUS) BIT 05	$MCSB05
2A1A06	J06B-04*03	2A2B4-E0/E1	5- 21	S6(S BUS) BIT 06	$MCSB06
2A1A06	J06B-06*05	2A2A9-U1/U0	5- 11	S6(S BUS) BIT 07	$MCSB07
2A1A06	J06B-08*07	2A2A8-U1/U0	5- 9	S6(S BUS) BIT 08	$MCSB08
2A1A06	J06B-10*09	2A2B8-W1/W0	5- 13	S6(S BUS) BIT 09	$MCSB09
2A1A06	J06C-02*01	2A2B8-T1/T0	5- 13	S6(S BUS) BIT 10	$MCSB10
2A1A06	J06C-04*03	2A2B7-C1/C0	5- 15	S6(S BUS) BIT 11	$MCSB11
2A1A06	J06C-06*05	2A2B7-E2/E3	5- 15	S6(S BUS) BIT 12	$MCSB12
2A1A06	J06C-08*07	2A2B6-C1/C0	5- 17	S6(S BUS) BIT 13	$MCSB13
2A1A06	J06C-10*09	2A2B6-E2/E3	5- 17	S6(S BUS) BIT 14	$MCSB14
2A1A06	J06D-02*01	2B0A7-K0/K1	6-117	(BCD FAULT)(BDP COMPLETE)(H03)	$STBCDF
2A1A06	J06D-04*03	2B0A7-L0/L1	6-117	SET EXPONENT FAULT	$STEXP0
2A1A06	J06D-06*05	2A2A5-I2/I3	5- 3	(FIRST OPERAND)(DP INST.)	$MCDP
2A1A06	J06D-08*07	2A2A6-H1/H0	5- 1	MC REQUEST PAGE FILE	$MCRQPF
2A1A06	J06D-10/09	2A2A6-T1*T0	5- 1	PF ADDR REPLY TO MN CONTROL	$PFARMC
2A1A06	J06E-02/01	2A2A7-X2*X3	5- 5	NOT DATA REPLY TO MAIN CONTROL	$PFDRMC
2A1A06	J06E-04/03	2A2A5-V1*V0	5- 3	LEGAL WRITE FOR BDP	$LWRBDP
2A1A06	J06E-06*05	2A2A5-F0/F1	5- 3	READ C OPERAND REQUEST(EDIT+67(0+1))	$FIELDC FIELDC
2A1A06	J06E-08*07	2B2A4-X1/X0	5- 65	NOT DO REGISTER BIT 14	$MCWR14
2A1A06	J06E-10/09	2A2A5-W1*W0	5- 3	(PF TIME 5)(MAIN CONT PRIORITY IN PF)	$PFT5MC
2A1A06	J07A-02/01	2A2A8-T2*T3	5- 9	ADDR BIT 00 TO EXTERNAL STOR	$EXTS00
2A1A06	J07A-04/03	2A2A9-T2*T3	5- 11	ADDR BIT 01 TO EXTERNAL STOR	$EXTS01
2A1A06	J07A-06/05	2A2A8-S2*S3	5- 9	ADDR BIT 02 TO EXTERNAL STOR	$EXTS02
2A1A06	J07A-08/07	2A2A9-S2*S3	5- 11	ADDR BIT 03 TO EXTERNAL STOR	$EXTS03
2A1A06	J07A-10/09	2A2A8-00*01	5- 9	ADDR BIT 04 TO EXTERNAL STOR	$EXTS04
2A1A06	J07B-02/01	2A2A9-00*01	5- 11	ADDR BIT 05 TO EXTERNAL STOR	$EXTS05
2A1A06	J07B-04/03	2A2B4-N1*N0	5- 21	ADDR BIT 06 TO EXTERNAL STOR	$EXTS06
2A1A06	J07B-06/05	2A2A9-N0*N1	5- 11	ADDR BIT 07 TO EXTERNAL STOR	$EXTS07
2A1A06	J07B-08/07	2A2A8-N0*N1	5- 9	ADDR BIT 08 TO EXTERNAL STOR	$EXTS08
2A1A06	J07B-10/09	2A2B8-V2*V3	5- 13	ADDR BIT 09 TO EXTERNAL STOR	$EXTS09

CONNECTOR		ORIGIN	PAGE	DEFINITION	SIG NAME
2A1A06	J07C-02/01	2A2B8-W3*W2	5- 13	ADDR BIT 10 TO EXTERNAL STOR	$EXTS10
2A1A06	J07C-04/03	2A2B7-N0*N1	5- 15	ADDR BIT 11 TO EXTERNAL STOR	$EXTS11
2A1A06	J07C-06/05	2A2B7-L2*L3	5- 15	ADDR BIT 12 TO EXTERNAL STOR	$EXTS12
2A1A06	J07C-08/07	2A2B6-N0*N1	5- 17	ADDR BIT 13 TO EXTERNAL STOR	$EXTS13
2A1A06	J07C-10/09	2A2B6-L2*L3	5- 17	ADDR BIT 14 TO EXTERNAL STOR	$EXTS14
2A1A06	J07D-02/01	2A2B5-N0*N1	5- 19	ADDR BIT 15 TO EXTERNAL STOR	$EXTS15
2A1A06	J07D-04/03	2A2B5-L2*L3	5- 19	ADDR BIT 16 TO EXTERNAL STOR	$EXTS16
2A1A06	J07D-06/05	2A2B4-W3*W2	5- 21	ADDR BIT 17 TO EXTERNAL STOR	$EXTS17
2A1A06	J07D-08/07	2B2B9-G2*G3	5- 75	PART. WR BIT 0 TO EXT STORAGE	$EXTPW0
2A1A06	J07D-10/09	2B2B9-F2*F3	5- 75	PART. WR BIT 1 TO EXT STORAGE	$EXTPW1
2A1A06	J07E-02/01	2B2B8-G2*G3	5- 77	PART. WR BIT 2 TO EXT STORAGE	$EXTPW2
2A1A06	J07E-04/03	2B2B8-F2*F3	5- 77	PART. WR BIT 3 TO EXT STORAGE	$EXTPW3
2A1A06	J07E-06/05	2B2B8-Q2*Q3	5- 77	PART. WR BIT 4 TO EXT STORAGE	$EXTPW4
2A1A06	J07E-08/07	2A2A7-J1*J0	5- 5	REQUEST TO EXTERNAL STORAGE	$RQEXTM
2A1A06	J07E-10*09	2A2A7-E3/E2	5- 5	EXTERNAL STORAGE ADDR. REPLY	$EXTMAR
2A1A06	J07F-02*01	2B2B8-X3/X2	5- 77	ADDR PAR. ERR FROM EXT STOR	$EXTAPE
2A1A06	J07F-04/03	2A2B9-P1*P0	5- 23	MASTER CLEAR EXTERNAL STORAGE	$CLEXTM
2A1A06	J07F-06/05	2A2B9-N1*N0	5- 23	ADDR LWR PAR. BIT TO EXT STOR	$EXTSLP
2A1A06	J07F-08*07	2A2B9-T0/T1	5- 23	EXT STOR NO RESPONSE	$EXTDNR
2A1A06	J08A-02/01	2A2A8-T2*T3	5- 9	ADDR BIT 00 TO EXTERNAL STOR	$EXTS00
2A1A06	J08A-04/03	2A2A9-T2*T3	5- 11	ADDR BIT 01 TO EXTERNAL STOR	$EXTS01
2A1A06	J08A-06/05	2A2A8-S2*S3	5- 9	ADDR BIT 02 TO EXTERNAL STOR	$EXTS02
2A1A06	J08A-08/07	2A2A9-S2*S3	5- 11	ADDR BIT 03 TO EXTERNAL STOR	$EXTS03
2A1A06	J08A-10/09	2A2A8-00*01	5- 9	ADDR BIT 04 TO EXTERNAL STOR	$EXTS04
2A1A06	J08B-02/01	2A2A9-00*01	5- 11	ADDR BIT 05 TO EXTERNAL STOR	$EXTS05
2A1A06	J08B-04/03	2A2B4-N1*N0	5- 21	ADDR BIT 06 TO EXTERNAL STOR	$EXTS06
2A1A06	J08B-06/05	2A2A9-N0*N1	5- 11	ADDR BIT 07 TO EXTERNAL STOR	$EXTS07
2A1A06	J08B-08/07	2A2A8-N0*N1	5- 9	ADDR BIT 08 TO EXTERNAL STOR	$EXTS08
2A1A06	J08B-10/09	2A2B8-V2*V3	5- 13	ADDR BIT 09 TO EXTERNAL STOR	$EXTS09
2A1A06	J08C-02/01	2A2B8-W3*W2	5- 13	ADDR BIT 10 TO EXTERNAL STOR	$EXTS10
2A1A06	J08C-04/03	2A2B7-N0*N1	5- 15	ADDR BIT 11 TO EXTERNAL STOR	$EXTS11
2A1A06	J08C-06/05	2A2B7-L2*L3	5- 15	ADDR BIT 12 TO EXTERNAL STOR	$EXTS12
2A1A06	J08C-08/07	2A2B6-N0*N1	5- 17	ADDR BIT 13 TO EXTERNAL STOR	$EXTS13
2A1A06	J08C-10/09	2A2B6-L2*L3	5- 17	ADDR BIT 14 TO EXTERNAL STOR	$EXTS14
2A1A06	J08D-02/01	2A2B5-N0*N1	5- 19	ADDR BIT 15 TO EXTERNAL STOR	$EXTS15
2A1A06	J08D-04/03	2A2B5-L2*L3	5- 19	ADDR BIT 16 TO EXTERNAL STOR	$EXTS16
2A1A06	J08D-06/05	2A2B4-W3*W2	5- 21	ADDR BIT 17 TO EXTERNAL STOR	$EXTS17
2A1A06	J08D-08/07	2B2B9-G2*G3	5- 75	PART. WR BIT 0 TO EXT STORAGE	$EXTPW0
2A1A06	J08D-10/09	2B2B9-F2*F3	5- 75	PART. WR BIT 1 TO EXT STORAGE	$EXTPW1
2A1A06	J08E-02/01	2B2B8-G2*G3	5- 77	PART. WR BIT 2 TO EXT STORAGE	$EXTPW2
2A1A06	J08E-04/03	2B2B8-F2*F3	5- 77	PART. WR BIT 3 TO EXT STORAGE	$EXTPW3
2A1A06	J08E-06/05	2B2B8-Q2*Q3	5- 77	PART. WR BIT 4 TO EXT STORAGE	$EXTPW4
2A1A06	J08E-08/07	2A2A7-J1*J0	5- 5	REQUEST TO EXTERNAL STORAGE	$RQEXTM
2A1A06	J08E-10*09	2A2A7-E3/E2	5- 5	EXTERNAL STORAGE ADDR. REPLY	$EXTMAR
2A1A06	J08F-02*01	2B2B8-X3/X2	5- 77	ADDR PAR. ERR FROM EXT STOR	$EXTAPE
2A1A06	J08F-04/03	2A2B9-P1*P0	5- 23	MASTER CLEAR EXTERNAL STORAGE	$CLEXTM
2A1A06	J08F-06/05	2A2B9-N1*N0	5- 23	ADDR LWR PAR. BIT TO EXT STOR	$EXTSLP
2A1A06	J08F-08*07	2A2B9-T0/T1	5- 23	EXT STOR NO RESPONSE	$EXTDNR
2A1A06	J09A-02/01	2B2A9-F3*F2	5- 57	BIT 00 TO/FROM EXTERNAL STOR	$EXTZ00
2A1A06	J09A-04/03	2B2A9-03*02	5- 57	BIT 01 TO/FROM EXTERNAL STOR	$EXTZ01
2A1A06	J09A-06/05	2B2A9-X3*X2	5- 57	BIT 02 TO/FROM EXTERNAL STOR	$EXTZ02
2A1A06	J09A-08/07	2B2A8-F3*F2	5- 59	BIT 03 TO/FROM EXTERNAL STOR	$EXTZ03
2A1A06	J09A-10/09	2B2A8-03*02	5- 59	BIT 04 TO/FROM EXTERNAL STOR	$EXTZ04
2A1A06	J09B-02/01	2B2A8-X3*X2	5- 59	BIT 05 TO/FROM EXTERNAL STOR	$EXTZ05
2A1A06	J09B-04/03	2B2A7-F3*F2	5- 61	BIT 06 TO/FROM EXTERNAL STOR	$EXTZ06
2A1A06	J09B-06/05	2B2A7-03*02	5- 61	BIT 07 TO/FROM EXTERNAL STOR	$EXTZ07
2A1A06	J09B-08/07	2B2A7-X3*X2	5- 61	BIT 08 TO/FROM EXTERNAL STOR	$EXTZ08
2A1A06	J09B-10/09	2B2A6-F3*F2	5- 63	BIT 09 TO/FROM EXTERNAL STOR	$EXTZ09
2A1A06	J09C-02/01	2B2A6-03*02	5- 63	BIT 10 TO/FROM EXTERNAL STOR	$EXTZ10
2A1A06	J09C-04/03	2B2A6-X3*X2	5- 63	BIT 11 TO/FROM EXTERNAL STOR	$EXTZ11
2A1A06	J09C-06/05	2B2A4-F3*F2	5- 65	BIT 12 TO/FROM EXTERNAL STOR	$EXTZ12
2A1A06	J09C-08/07	2B2A4-03*02	5- 65	BIT 13 TO/FROM EXTERNAL STOR	$EXTZ13
2A1A06	J09C-10/09	2B2A4-X3*X2	5- 65	BIT 14 TO/FROM EXTERNAL STOR	$EXTZ14
2A1A06	J09D-02/01	2B2A3-F3*F2	5- 67	BIT 15 TO/FROM EXTERNAL STOR	$EXTZ15
2A1A06	J09D-04/03	2B2A3-03*02	5- 67	BIT 16 TO/FROM EXTERNAL STOR	$EXTZ16
2A1A06	J09D-06/05	2B2A3-X3*X2	5- 67	BIT 17 TO/FROM EXTERNAL STOR	$EXTZ17
2A1A06	J09D-08/07	2B2A2-F3*F2	5- 69	BIT 18 TO/FROM EXTERNAL STOR	$EXTZ18
2A1A06	J09D-10/09	2B2A2-03*02	5- 69	BIT 19 TO/FROM EXTERNAL STOR	$EXTZ19
2A1A06	J09E-02/01	2B2A2-X3*X2	5- 69	BIT 20 TO/FROM EXTERNAL STOR	$EXTZ20
2A1A06	J09E-04/03	2B2A1-F3*F2	5- 71	BIT 21 TO/FROM EXTERNAL STOR	$EXTZ21
2A1A06	J09E-06/05	2B2A1-03*02	5- 71	BIT 22 TO/FROM EXTERNAL STOR	$EXTZ22
2A1A06	J09E-08/07	2B2A1-X3*X2	5- 71	BIT 23 TO/FROM EXTERNAL STOR	$EXTZ23
2A1A06	J09E-10/09	2B2A5-M0*M1	5- 73	BIT 24 TO/FROM EXTERNAL STOR	$EXTZ24
2A1A06	J09F-02/01	2B2A5-C1*C0	5- 73	BIT 25 TO/FROM EXTERNAL STOR	$EXTZ25

CONNECTOR		ORIGIN	PAGE	DEFINITION	SIG NAME
2A1A06	J09F-04/03	2B2A5-M3*M2	5- 73	BIT 26 TO/FROM EXTERNAL STOR	$EXTZ26
2A1A06	J09F-06/05	2B2A5-D2*D3	5- 73	BIT 27 TO/FROM EXTERNAL STOR	$EXTZ27
2A1A06	J09F-08/07	2B2B9-Q2*Q3	5- 75	DISABLE ADR PAR CHK,EXT STOR	$EXTDPE
2A1A06	J10A-02/01	2B2A9-F3*F2	5- 57	BIT 00 TO/FROM EXTERNAL STOR	$EXTZ00
2A1A06	J10A-04/03	2B2A9-Q3*Q2	5- 57	BIT 01 TO/FROM EXTERNAL STOR	$EXTZ01
2A1A06	J10A-06/05	2B2A9-X3*X2	5- 57	BIT 02 TO/FROM EXTERNAL STOR	$EXTZ02
2A1A06	J10A-08/07	2B2A8-F3*F2	5- 59	BIT 03 TO/FROM EXTERNAL STOR	$EXTZ03
2A1A06	J10A-10/09	2B2A8-Q3*Q2	5- 59	BIT 04 TO/FROM EXTERNAL STOR	$EXTZ04
2A1A06	J10B-02/01	2B2A8-X3*X2	5- 59	BIT 05 TO/FROM EXTERNAL STOR	$EXTZ05
2A1A06	J10B-04/03	2B2A7-F3*F2	5- 61	BIT 06 TO/FROM EXTERNAL STOR	$EXTZ06
2A1A06	J10B-06/05	2B2A7-Q3*Q2	5- 61	BIT 07 TO/FROM EXTERNAL STOR	$EXTZ07
2A1A06	J10B-08/07	2B2A7-X3*X2	5- 61	BIT 08 TO/FROM EXTERNAL STOR	$EXTZ08
2A1A06	J10B-10/09	2B2A6-F3*F2	5- 63	BIT 09 TO/FROM EXTERNAL STOR	$EXTZ09
2A1A06	J10C-02/01	2B2A6-Q3*Q2	5- 63	BIT 10 TO/FROM EXTERNAL STOR	$EXTZ10
2A1A06	J10C-04/03	2B2A6-X3*X2	5- 63	BIT 11 TO/FROM EXTERNAL STOR	$EXTZ11
2A1A06	J10C-06/05	2B2A4-F3*F2	5- 65	BIT 12 TO/FROM EXTERNAL STOR	$EXTZ12
2A1A06	J10C-08/07	2B2A4-Q3*Q2	5- 65	BIT 13 TO/FROM EXTERNAL STOR	$EXTZ13
2A1A06	J10C-10/09	2B2A4-X3*X2	5- 65	BIT 14 TO/FROM EXTERNAL STOR	$EXTZ14
2A1A06	J10D-02/01	2B2A3-F3*F2	5- 67	BIT 15 TO/FROM EXTERNAL STOR	$EXTZ15
2A1A06	J10D-04/03	2B2A3-Q3*Q2	5- 67	BIT 16 TO/FROM EXTERNAL STOR	$EXTZ16
2A1A06	J10D-06/05	2B2A3-X3*X2	5- 67	BIT 17 TO/FROM EXTERNAL STOR	$EXTZ17
2A1A06	J10D-08/07	2B2A2-F3*F2	5- 69	BIT 18 TO/FROM EXTERNAL STOR	$EXTZ18
2A1A06	J10D-10/09	2B2A2-Q3*Q2	5- 69	BIT 19 TO/FROM EXTERNAL STOR	$EXTZ19
2A1A06	J10E-02/01	2B2A2-X3*X2	5- 69	BIT 20 TO/FROM EXTERNAL STOR	$EXTZ20
2A1A06	J10E-04/03	2B2A1-F3*F2	5- 71	BIT 21 TO/FROM EXTERNAL STOR	$EXTZ21
2A1A06	J10E-06/05	2B2A1-Q3*Q2	5- 71	BIT 22 TO/FROM EXTERNAL STOR	$EXTZ22
2A1A06	J10E-08/07	2B2A1-X3*X2	5- 71	BIT 23 TO/FROM EXTERNAL STOR	$EXTZ23
2A1A06	J10E-10/09	2B2A5-M0*M1	5- 73	BIT 24 TO/FROM EXTERNAL STOR	$EXTZ24
2A1A06	J10F-02/01	2B2A5-C1*C0	5- 73	BIT 25 TO/FROM EXTERNAL STOR	$EXTZ25
2A1A06	J10F-04/03	2B2A5-M3*M2	5- 73	BIT 26 TO/FROM EXTERNAL STOR	$EXTZ26
2A1A06	J10F-06/05	2B2A5-D2*D3	5- 73	BIT 27 TO/FROM EXTERNAL STOR	$EXTZ27
2A1A06	J10F-08/07	2B2B9-Q2*Q3	5- 75	DISABLE ADR PAR CHK,EXT STOR	$EXTDPE
2A1A06	J11A-02/01	2B2A9-D2*D3	5- 57	BIT 00 TO INTERNAL STORAGE A	$IN00A0
2A1A06	J11A-04/03	2B2A9-S2*S3	5- 57	BIT 01 TO INTERNAL STORAGE A	$IN01A0
2A1A06	J11A-06/05	2B2A9-U0*U1	5- 57	BIT 02 TO INTERNAL STORAGE A	$IN02A0
2A1A06	J11A-08/07	2B2A8-D2*D3	5- 59	BIT 03 TO INTERNAL STORAGE A	$IN03A0
2A1A06	J11A-10/09	2B2A8-S2*S3	5- 59	BIT 04 TO INTERNAL STORAGE A	$IN04A0
2A1A06	J11B-02/01	2B2A8-U0*U1	5- 59	BIT 05 TO INTERNAL STORAGE A	$IN05A0
2A1A06	J11B-04/03	2B2A7-D2*D3	5- 61	BIT 06 TO INTERNAL STORAGE A	$IN06A0
2A1A06	J11B-06/05	2B2A7-S2*S3	5- 61	BIT 07 TO INTERNAL STORAGE A	$IN07A0
2A1A06	J11B-08/07	2B2A7-U0*U1	5- 61	BIT 08 TO INTERNAL STORAGE A	$IN08A0
2A1A06	J11B-10/09	2B2A6-D2*D3	5- 63	BIT 09 TO INTERNAL STORAGE A	$IN09A0
2A1A06	J11C-02/01	2B2A6-S2*S3	5- 63	BIT 10 TO INTERNAL STORAGE A	$IN10A0
2A1A06	J11C-04/03	2B2A6-U0*U1	5- 63	BIT 11 TO INTERNAL STORAGE A	$IN11A0
2A1A06	J11C-06/05	2B2A4-D2*D3	5- 65	BIT 12 TO INTERNAL STORAGE A	$IN12A0
2A1A06	J11C-08/07	2B2A4-S2*S3	5- 65	BIT 13 TO INTERNAL STORAGE A	$IN13A0
2A1A06	J11C-10/09	2B2A4-U0*U1	5- 65	BIT 14 TO INTERNAL STORAGE A	$IN14A0
2A1A06	J11D-02/01	2B2A3-D2*D3	5- 67	BIT 15 TO INTERNAL STORAGE A	$IN15A0
2A1A06	J11D-04/03	2B2A3-S2*S3	5- 67	BIT 16 TO INTERNAL STORAGE A	$IN16A0
2A1A06	J11D-06/05	2B2A3-U0*U1	5- 67	BIT 17 TO INTERNAL STORAGE A	$IN17A0
2A1A06	J11D-08/07	2B2A2-D2*D3	5- 69	BIT 18 TO INTERNAL STORAGE A	$IN18A0
2A1A06	J11D-10/09	2B2A2-S2*S3	5- 69	BIT 19 TO INTERNAL STORAGE A	$IN19A0
2A1A06	J11E-02/01	2B2A2-U0*U1	5- 69	BIT 20 TO INTERNAL STORAGE A	$IN20A0
2A1A06	J11E-04/03	2B2A1-D2*D3	5- 71	BIT 21 TO INTERNAL STORAGE A	$IN21A0
2A1A06	J11E-06/05	2B2A1-S2*S3	5- 71	BIT 22 TO INTERNAL STORAGE A	$IN22A0
2A1A06	J11E-08/07	2B2A1-U0*U1	5- 71	BIT 23 TO INTERNAL STORAGE A	$IN23A0
2A1A06	J11E-10/09	2B2A5-K1*K0	5- 73	BIT 24 TO INTERNAL STORAGE A	$IN24A0
2A1A06	J11F-02/01	2B2A5-R0*B1	5- 73	BIT 25 TO INTERNAL STORAGE A	$IN25A0
2A1A06	J11F-04/03	2B2A5-J3*J2	5- 73	BIT 26 TO INTERNAL STORAGE A	$IN26A0
2A1A06	J11F-06/05	2B2A5-R3*B2	5- 73	BIT 27 TO INTERNAL STORAGE A	$IN27A0
2A1A06	J12A-02*01	2B2A9-L3/L2	5- 57	BIT 00 FROM INTERNAL STORAGE A	$IN00AI
2A1A06	J12A-04*03	2B2A9-J2/J3	5- 57	BIT 01 FROM INTERNAL STORAGE A	$IN01AI
2A1A06	J12A-06*05	2B2A9-R2/R3	5- 57	BIT 02 FROM INTERNAL STORAGE A	$IN02AI
2A1A06	J12A-08*07	2B2A8-L3/L2	5- 59	BIT 03 FROM INTERNAL STORAGE A	$IN03AI
2A1A06	J12A-10*09	2B2A8-J2/J3	5- 59	BIT 04 FROM INTERNAL STORAGE A	$IN04AI
2A1A06	J12B-02*01	2B2A8-R2/R3	5- 59	BIT 05 FROM INTERNAL STORAGE A	$IN05AI
2A1A06	J12B-04*03	2B2A7-L3/L2	5- 61	BIT 06 FROM INTERNAL STORAGE A	$IN06AI
2A1A06	J12B-06*05	2B2A7-J2/J3	5- 61	BIT 07 FROM INTERNAL STORAGE A	$IN07AI
2A1A06	J12B-08*07	2B2A7-R2/R3	5- 61	BIT 08 FROM INTERNAL STORAGE A	$IN08AI
2A1A06	J12B-10*09	2B2A6-L3/L2	5- 63	BIT 09 FROM INTERNAL STORAGE A	$IN09AI
2A1A06	J12C-02*01	2B2A6-J2/J3	5- 63	BIT 10 FROM INTERNAL STORAGE A	$IN10AI
2A1A06	J12C-04*03	2B2A6-R2/R3	5- 63	BIT 11 FROM INTERNAL STORAGE A	$IN11AI
2A1A06	J12C-06*05	2B2A4-L3/L2	5- 65	BIT 12 FROM INTERNAL STORAGE A	$IN12AI

CONNECTOR		ORIGIN	PAGE	DEFINITION	SIG NAME
2A1A06	J12C-08*07	2B2A4-J2/J3	5- 65	BIT 13 FROM INTERNAL STORAGE A	$IN13AI
2A1A06	J12C-10*09	2B2A4-R2/R3	5- 65	BIT 14 FROM INTERNAL STORAGE A	$IN14AI
2A1A06	J12D-02*01	2B2A3-L3/L2	5- 67	BIT 15 FROM INTERNAL STORAGE A	$IN15AI
2A1A06	J12D-04*03	2B2A3-J2/J3	5- 67	BIT 16 FROM INTERNAL STORAGE A	$IN16AI
2A1A06	J12D-06*05	2B2A3-R2/R3	5- 67	BIT 17 FROM INTERNAL STORAGE A	$IN17AI
2A1A06	J12D-08*07	2B2A2-L3/L2	5- 69	BIT 18 FROM INTERNAL STORAGE A	$IN18AI
2A1A06	J12D-10*09	2B2A2-J2/J3	5- 69	BIT 19 FROM INTERNAL STORAGE A	$IN19AI
2A1A06	J12E-02*01	2B2A2-R2/R3	5- 69	BIT 20 FROM INTERNAL STORAGE A	$IN20AI
2A1A06	J12E-04*03	2B2A1-L3/L2	5- 71	BIT 21 FROM INTERNAL STORAGE A	$IN21AI
2A1A06	J12E-06*05	2B2A1-J2/J3	5- 71	BIT 22 FROM INTERNAL STORAGE A	$IN22AI
2A1A06	J12E-08*07	2B2A1-R2/R3	5- 71	BIT 23 FROM INTERNAL STORAGE A	$IN23AI
2A1A06	J12E-10*09	2B2A5-I0/I1	5- 73	BIT 24 FROM INTERNAL STORAGE A	$IN24AI
2A1A06	J12F-02*01	2B2A5-F1/F0	5- 73	BIT 25 FROM INTERNAL STORAGE A	$IN25AI
2A1A06	J12F-04*03	2B2A5-H3/H2	5- 73	BIT 26 FROM INTERNAL STORAGE A	$IN26AI
2A1A06	J12F-06*05	2B2A5-F3/F2	5- 73	BIT 27 FROM INTERNAL STORAGE A	$IN27AI
2A1A06	J12F-08/07	2B2B9-M3*M2	5- 75	DISABLE ADR PAR CHK,INT STOR A	$INDPEA
2A1A06	J13A-02/01	2B2A9-C3*C2	5- 57	BIT 00 TO INTERNAL STORAGE B	$IN00B0
2A1A06	J13A-04/03	2B2A9-P3*P2	5- 57	BIT 01 TO INTERNAL STORAGE B	$IN01B0
2A1A06	J13A-06/05	2B2A9-V1*V0	5- 57	BIT 02 TO INTERNAL STORAGE B	$IN02B0
2A1A06	J13A-08/07	2B2A8-C3*C2	5- 59	BIT 03 TO INTERNAL STORAGE B	$IN03B0
2A1A06	J13A-10/09	2B2A8-P3*P2	5- 59	BIT 04 TO INTERNAL STORAGE B	$IN04B0
2A1A06	J13B-02/01	2B2A8-V1*V0	5- 59	BIT 05 TO INTERNAL STORAGE B	$IN05B0
2A1A06	J13B-04/03	2B2A7-C3*C2	5- 61	BIT 06 TO INTERNAL STORAGE B	$IN06B0
2A1A06	J13B-06/05	2B2A7-P3*P2	5- 61	BIT 07 TO INTERNAL STORAGE B	$IN07B0
2A1A06	J13B-08/07	2B2A7-V1*V0	5- 61	BIT 08 TO INTERNAL STORAGE B	$IN08B0
2A1A06	J13B-10/09	2B2A6-C3*C2	5- 63	BIT 09 TO INTERNAL STORAGE B	$IN09B0
2A1A06	J13C-02/01	2B2A6-P3*P2	5- 63	BIT 10 TO INTERNAL STORAGE B	$IN10B0
2A1A06	J13C-04/03	2B2A6-V1*V0	5- 63	BIT 11 TO INTERNAL STORAGE B	$IN11B0
2A1A06	J13C-06/05	2B2A4-C3*C2	5- 65	BIT 12 TO INTERNAL STORAGE B	$IN12B0
2A1A06	J13C-08/07	2B2A4-P3*P2	5- 65	BIT 13 TO INTERNAL STORAGE B	$IN13B0
2A1A06	J13C-10/09	2B2A4-V1*V0	5- 65	BIT 14 TO INTERNAL STORAGE B	$IN14B0
2A1A06	J13D-02/01	2B2A3-C3*C2	5- 67	BIT 15 TO INTERNAL STORAGE B	$IN15B0
2A1A06	J13D-04/03	2B2A3-P3*P2	5- 67	BIT 16 TO INTERNAL STORAGE B	$IN16B0
2A1A06	J13D-06/05	2B2A3-V1*V0	5- 67	BIT 17 TO INTERNAL STORAGE B	$IN17B0
2A1A06	J13D-08/07	2B2A2-C3*C2	5- 69	BIT 18 TO INTERNAL STORAGE B	$IN18B0
2A1A06	J13D-10/09	2B2A2-P3*P2	5- 69	BIT 19 TO INTERNAL STORAGE B	$IN19B0
2A1A06	J13E-02/01	2B2A2-V1*V0	5- 69	BIT 20 TO INTERNAL STORAGE B	$IN20B0
2A1A06	J13E-04/03	2B2A1-C3*C2	5- 71	BIT 21 TO INTERNAL STORAGE B	$IN21B0
2A1A06	J13E-06/05	2B2A1-P3*P2	5- 71	BIT 22 TO INTERNAL STORAGE B	$IN22B0
2A1A06	J13E-08/07	2B2A1-V1*V0	5- 71	BIT 23 TO INTERNAL STORAGE B	$IN23B0
2A1A06	J13E-10/09	2B2A5-L1*L0	5- 73	BIT 24 TO INTERNAL STORAGE B	$IN24B0
2A1A06	J13F-02/01	2B2A5-D0*D1	5- 73	BIT 25 TO INTERNAL STORAGE B	$IN25B0
2A1A06	J13F-04/03	2B2A5-L3*L2	5- 73	BIT 26 TO INTERNAL STORAGE B	$IN26B0
2A1A06	J13F-06/05	2B2A5-C2*C3	5- 73	BIT 27 TO INTERNAL STORAGE B	$IN27B0
2A1A06	J14A-02*01	2B2A9-K2/K3	5- 57	BIT 00 FROM INTERNAL STORAGE B	$IN00BI
2A1A06	J14A-04*03	2B2A9-I2/I3	5- 57	BIT 01 FROM INTERNAL STORAGE B	$IN01BI
2A1A06	J14A-06*05	2B2A9-Q2/Q3	5- 57	BIT 02 FROM INTERNAL STORAGE B	$IN02BI
2A1A06	J14A-08*07	2B2A8-K2/K3	5- 59	BIT 03 FROM INTERNAL STORAGE B	$IN03BI
2A1A06	J14A-10*09	2B2A8-I2/I3	5- 59	BIT 04 FROM INTERNAL STORAGE B	$IN04BI
2A1A06	J14B-02*01	2B2A8-Q2/Q3	5- 59	BIT 05 FROM INTERNAL STORAGE B	$IN05BI
2A1A06	J14B-04*03	2B2A7-K2/K3	5- 61	BIT 06 FROM INTERNAL STORAGE B	$IN06BI
2A1A06	J14B-06*05	2B2A7-I2/I3	5- 61	BIT 07 FROM INTERNAL STORAGE B	$IN07BI
2A1A06	J14B-08*07	2B2A7-Q2/Q3	5- 61	BIT 08 FROM INTERNAL STORAGE B	$IN08BI
2A1A06	J14B-10*09	2B2A6-K2/K3	5- 63	BIT 09 FROM INTERNAL STORAGE B	$IN09BI
2A1A06	J14C-02*01	2B2A6-I2/I3	5- 63	BIT 10 FROM INTERNAL STORAGE B	$IN10BI
2A1A06	J14C-04*03	2B2A6-Q2/Q3	5- 63	BIT 11 FROM INTERNAL STORAGE B	$IN11BI
2A1A06	J14C-06*05	2B2A4-K2/K3	5- 65	BIT 12 FROM INTERNAL STORAGE B	$IN12BI
2A1A06	J14C-08*07	2B2A4-I2/I3	5- 65	BIT 13 FROM INTERNAL STORAGE B	$IN13BI
2A1A06	J14C-10*09	2B2A4-Q2/Q3	5- 65	BIT 14 FROM INTERNAL STORAGE B	$IN14BI
2A1A06	J14D-02*01	2B2A3-K2/K3	5- 67	BIT 15 FROM INTERNAL STORAGE B	$IN15BI
2A1A06	J14D-04*03	2B2A3-I2/I3	5- 67	BIT 16 FROM INTERNAL STORAGE B	$IN16BI
2A1A06	J14D-06*05	2B2A3-Q2/Q3	5- 67	BIT 17 FROM INTERNAL STORAGE B	$IN17BI
2A1A06	J14D-08*07	2B2A2-K2/K3	5- 69	BIT 18 FROM INTERNAL STORAGE B	$IN18BI
2A1A06	J14D-10*09	2B2A2-I2/I3	5- 69	BIT 19 FROM INTERNAL STORAGE B	$IN19BI
2A1A06	J14E-02*01	2B2A2-Q2/Q3	5- 69	BIT 20 FROM INTERNAL STORAGE B	$IN20BI
2A1A06	J14E-04*03	2B2A1-K2/K3	5- 71	BIT 21 FROM INTERNAL STORAGE B	$IN21BI
2A1A06	J14E-06*05	2B2A1-I2/I3	5- 71	BIT 22 FROM INTERNAL STORAGE B	$IN22BI
2A1A06	J14E-08*07	2B2A1-Q2/Q3	5- 71	BIT 23 FROM INTERNAL STORAGE B	$IN23BI
2A1A06	J14E-10*09	2B2A5-H1/H0	5- 73	BIT 24 FROM INTERNAL STORAGE B	$IN24BI
2A1A06	J14F-02*01	2B2A5-G1/G0	5- 73	BIT 25 FROM INTERNAL STORAGE B	$IN25BI
2A1A06	J14F-04*03	2B2A5-G3/G2	5- 73	BIT 26 FROM INTERNAL STORAGE B	$IN26BI
2A1A06	J14F-06*05	2B2A5-E3/E2	5- 73	BIT 27 FROM INTERNAL STORAGE B	$IN27BI
2A1A06	J14F-08/07	2B2B9-N3*N2	5- 75	DISABLE ADR PAR CHK,INT STOR B	$INDPEB
2A1A06	J15A-02/01	2B1B9-D0*D1	6- 27	TW 0 REG BIT 00 TO CONSOLE	$EXTW00

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A1A06	J15A-04/03	2B1B9-G1*G0		6- 27	TW 0 REG BIT 01 TO CONSOLE	$EXTW01
2A1A06	J15A-06/05	2B1B9-L1*L0		6- 27	TW 0 REG BIT 02 TO CONSOLE	$EXTW02
2A1A06	J15A-08/07	2B1B9-R1*R0		6- 27	TW 0 REG BIT 03 TO CONSOLE	$EXTW03
2A1A06	J15A-10/09	2B1B9-X1*X0		6- 27	TW 0 REG BIT 04 TO CONSOLE	$EXTW04
2A1A06	J15B-02/01	2B1B9-W1*W0		6- 27	TW 0 REG BIT 05 TO CONSOLE	$EXTW05
2A1A06	J15B-04*03	2B1B8-X1/X0		6- 11	TW CONTROL BUSY	$EXTWBS
2A1A06	J15B-06*05	2B1B8-M1/M0		6- 11	EXT TW PRIORITY REQ ON LOAD	$EXTWPR
2A1A06	J15B-08/07	2B1B9-H3*H2		6- 27	TW LOAD XLTN TO CONSOLE	$EXTTWI
2A1A06	J15B-10/09	2B1B9-I3*I2		6- 27	TW DUMP XLTN TO CONSOLE	$EXTTWO
2A1A06	J15C-02/01	2B1B8-W2*W3		6- 11	TW DATA READY SIGNAL FROM BC	$EXTWDR
2A1A06	J15C-04*03	2B1B8-D0/D1		6- 11	CLOCK PULSE-50 USEC EACH MS	$CLK50U
2A1A06	J15C-06*05	2B2B9-X2/X3		5- 75	AUTO-STEP OSCILLATOR FROM CONSOLE	$ASO
2A1A06	J15C-07/08	2A2B9-X3*X2		5- 23	STOR ADDR REPLY	$STA
2A1A06	J15C-10/09	2B0A9-R2*R3		6-101	EXT INTERRUPT - ASSOC PROC	$EXTIOC
2A1A06	J15D-01*02	2B0A8-W0/W1		6-109	EXT INTERRUPT FROM ASSOC PROC	EXTITC
2A1A06	J16A-02/01	2B1B9-D0*D1		6- 27	TW 0 REG BIT 00 TO CONSOLE	$EXTW00
2A1A06	J16A-04/03	2B1B9-G1*G0		6- 27	TW 0 REG BIT 01 TO CONSOLE	$EXTW01
2A1A06	J16A-06/05	2B1B9-L1*L0		6- 27	TW 0 REG BIT 02 TO CONSOLE	$EXTW02
2A1A06	J16A-08/07	2B1B9-R1*R0		6- 27	TW 0 REG BIT 03 TO CONSOLE	$EXTW03
2A1A06	J16A-10/09	2B1B9-X1*X0		6- 27	TW 0 REG BIT 04 TO CONSOLE	$EXTW04
2A1A06	J16B-02/01	2B1B9-W1*W0		6- 27	TW 0 REG BIT 05 TO CONSOLE	$EXTW05
2A1A06	J16B-04*03	2B1B8-X1/X0		6- 11	TW CONTROL BUSY	$EXTWBS
2A1A06	J16B-06*05	2B1B8-M1/M0		6- 11	EXT TW PRIORITY REQ ON LOAD	$EXTWPR
2A1A06	J16B-08/07	2B1B9-H3*H2		6- 27	TW LOAD XLTN TO CONSOLE	$EXTTWI
2A1A06	J16B-10/09	2B1B9-I3*I2		6- 27	TW DUMP XLTN TO CONSOLE	$EXTTWO
2A1A06	J16C-02/01	2B1B8-W2*W3		6- 11	TW DATA READY SIGNAL FROM BC	$EXTWDR
2A1A06	J16C-04*03	2B1B8-D0/D1		6- 11	CLOCK PULSE-50 USEC EACH MS	$CLK50U
2A1A06	J16C-06*05	2B2B9-X2/X3		5- 75	AUTO-STEP OSCILLATOR FROM CONSOLE	$ASO
2A1A06	J16C-07/08	2A2B9-X3*X2		5- 23	STOR ADDR REPLY	$STA
2A1A06	J16C-09*	J03L-03	2A2A04		ENABLE FROM CONS MAINT MODE SW	MMENAB
2A1A06	J16C-10	J03L-02*	2A2A04		GRD FOR CONSOLE MAINT MODE SW	MMGND
2A1A06	J16D-01*	2A2A5-00		5- 3	DISABLE STORAGE PROTECT SWITCH	DISSPS
2A1A06	J16D-03*	2A2A5-01		5- 3	ENTER AUTO PROGRAM SWITCH	ENTAPS
2A1A06	J16D-07*	2B1B1-J1		6- 9	SWITCH, POWER ON MASTER CLEAR	POMCLR
2A1A06	J16D-09*	2B1B8-H0		6- 11	SWITCH, WRITE STORAGE OR RF	WSTO
2A1A06	J16E-01*	2A1A4-I3		6- 59	BREAK POINT SWITCH BIT 5	BPMC05
2A1A06	J16E-02*	2A1A4-S3		6- 59	BREAK POINT SWITCH BIT 4	BPMC04
2A1A06	J16E-03*	2A1A4-R3		6- 59	BREAK POINT SWITCH BIT 3	BPMC03
2A1A06	J16E-04*	2A1A4-J3		6- 59	BREAK POINT SWITCH BIT 2	BPMC02
2A1A06	J16E-05*	2A1A4-H3		6- 59	BREAK POINT SWITCH BIT 1	BPMC01
2A1A06	J16E-06*	2A1A4-G3		6- 59	BREAK POINT SWITCH BIT 0	BPMC00
2A1A06	J16E-07*	2B1A9-B0		6- 23	CONSOLE MANUAL INT SW	EXMNIN
2A1A06	J16E-08*	2B1A9-C1		6- 23	NOT(CONSOLE MANUAL INT SW)	*EXMNIN
2A1A06	J16E-09*	2B1B9-O3		6- 27	CONSOLE TYPE CLEAR SW	EXTWCS
2A1A06	J16E-10*	2B1B9-O2		6- 27	NOT(CONSOLE TYPE CLEAR SW)	*EXTWCS
2A1A06	J16F-01*	2B1B9-L3		6- 27	CONSOLE TYPE FINISH SW	EXTWFS
2A1A06	J16F-02*	2B1B9-L2		6- 27	NOT(CONSOLE TYPE FINISH SW)	*EXTWFS
2A1A06	J16F-03*	2B1B9-P3		6- 27	CONSOLE TYPE REPEAT SW	EXTWRS
2A1A06	J16F-04*	2B1B9-P2		6- 27	NOT(CONSOLE TYPE REPEAT SW)	*EXTWRS
2A1A06	J16F-05*	2B1B9-J3		6- 27	CONSOLE TYPE DUMP SW	EXTWOS
2A1A06	J16F-06*	2B1B9-K2		6- 27	NOT(CONSOLE TYPE DUMP SW)	*EXTWOS
2A1A06	J16F-07*	2B1B9-D3		6- 27	CONSOLE TYPE LOAD SW	EXTWIS
2A1A06	J16F-08*	2B1B9-E3		6- 27	NOT(CONSOLE TYPE LOAD SW	*EXTWIS
2A1A06	J17A-02*01	2B2B7-E1/E0		5- 79	NOT BIT 00 OF A1*Q1*E1*E2	$AELT00
2A1A06	J17A-04*03	2B2B7-D0/D1		5- 79	NOT BIT 01 OF A1*Q1*E1*E2	$AELT01
2A1A06	J17A-06*05	2B2B7-C0/C1		5- 79	NOT BIT 02 OF A1*Q1*E1*E2	$AELT02
2A1A06	J17A-08*07	2B2B7-J1/J0		5- 79	NOT BIT 03 OF A1*Q1*E1*E2	$AELT03
2A1A06	J17A-10*09	2B2B7-I0/I1		5- 79	NOT BIT 04 OF A1*Q1*E1*E2	$AELT04
2A1A06	J17B-02*01	2B2B7-H0/H1		5- 79	NOT BIT 05 OF A1*Q1*E1*E2	$AELT05
2A1A06	J17B-04*03	2B2B7-O1/O0		5- 79	NOT BIT 06 OF A1*Q1*E1*E2	$AELT06
2A1A06	J17B-06*05	2B2B7-N0/N1		5- 79	NOT BIT 07 OF A1*Q1*E1*E2	$AELT07
2A1A06	J17B-08*07	2B2B7-M0/M1		5- 79	NOT BIT 08 OF A1*Q1*E1*E2	$AELT08
2A1A06	J17B-10*09	2B2B7-T0/T1		5- 79	NOT BIT 09 OF A1*Q1*E1*E2	$AELT09
2A1A06	J17C-02*01	2B2B7-S0/S1		5- 79	NOT BIT 10 OF A1*Q1*E1*E2	$AELT10
2A1A06	J17C-04*03	2B2B7-R0/R1		5- 79	NOT BIT 11 OF A1*Q1*E1*E2	$AELT11
2A1A06	J17C-06*05	2B2B7-X0/X1		5- 79	NOT BIT 12 OF A1*Q1*E1*E2	$AELT12
2A1A06	J17C-08*07	2B2B7-W0/W1		5- 79	NOT BIT 13 OF A1*Q1*E1*E2	$AELT13
2A1A06	J17C-10*09	2B2B7-C2/C3		5- 79	NOT BIT 14 OF A1*Q1*E1*E2	$AELT14
2A1A06	J17D-02*01	2B2B7-D2/D3		5- 79	NOT BIT 15 OF A1*Q1*E1*E2	$AELT15
2A1A06	J17D-04*03	2B2B7-E3/E2		5- 79	NOT BIT 16 OF A1*Q1*E1*E2	$AELT16
2A1A06	J17D-06*05	2B2B7-H2/H3		5- 79	NOT BIT 17 OF A1*Q1*E1*E2	$AELT17
2A1A06	J17D-08*07	2B2B7-I2/I3		5- 79	NOT BIT 18 OF A1*Q1*E1*E2	$AELT18
2A1A06	J17D-10*09	2B2B7-J3/J2		5- 79	NOT BIT 19 OF A1*Q1*E1*E2	$AELT19
2A1A06	J17E-02*01	2B2B7-M2/M3		5- 79	NOT BIT 20 OF A1*Q1*E1*E2	$AELT20
2A1A06	J17E-04*03	2B2B7-N2/N3		5- 79	NOT BIT 21 OF A1*Q1*E1*E2	$AELT21
2A1A06	J17E-06*05	2B2B7-O3/O2		5- 79	NOT BIT 22 OF A1*Q1*E1*E2	$AELT22
2A1A06	J17E-08*07	2B2B7-R2/R3		5- 79	NOT BIT 23 OF A1*Q1*E1*E2	$AELT23
2A1A06	J17E-09	J03A-03*	2A2A04			BPFSMG
2A1A06	J17E-10	J03B-03*	2A2A04			BPSLMG
2A1A06	J17F-01	J03M-03*	2A2A04		CC-MR SWITCH IN CC POSITION	BT130R
2A1A06	J18A-01	2B2B7-A0*		5- 79	A/Q/E REG DISPLAY BIT 00	AQE00
2A1A06	J18A-02	2B2B7-B1*		5- 79	A/Q/E REG DISPLAY BIT 01	AQE01
2A1A06	J18A-03	2B2B7-R0*		5- 79	A/Q/E REG DISPLAY BIT 02	AQE02
2A1A06	J18A-04	2B2B7-F1*		5- 79	A/Q/E REG DISPLAY BIT 03	AQE03
2A1A06	J18A-05	2B2B7-F0*		5- 79	A/Q/E REG DISPLAY BIT 04	AQE04
2A1A06	J18A-06	2B2B7-G1*		5- 79	A/Q/E REG DISPLAY BIT 05	AQE05
2A1A06	J18A-07	2B2B7-L0*		5- 79	A/Q/E REG DISPLAY BIT 06	AQE06
2A1A06	J18A-08	2B2B7-K0*		5- 79	A/Q/E REG DISPLAY BIT 07	AQE07
2A1A06	J18A-09	2B2B7-K1*		5- 79	A/Q/E REG DISPLAY BIT 08	AQE08
2A1A06	J18A-10	2B2B7-Q0*		5- 79	A/Q/E REG DISPLAY BIT 09	AQE09
2A1A06	J18B-01	2B2B7-P0*		5- 79	A/Q/E REG DISPLAY BIT 10	AQE10
2A1A06	J18B-02	2B2B7-P1*		5- 79	A/Q/E REG DISPLAY BIT 11	AQE11
2A1A06	J18B-03	2B2B7-U0*		5- 79	A/Q/E REG DISPLAY BIT 12	AQE12
2A1A06	J18B-04	2B2B7-U1*		5- 79	A/Q/E REG DISPLAY BIT 13	AQE13
2A1A06	J18B-05	2B2B7-A3*		5- 79	A/Q/E REG DISPLAY BIT 14	AQE14
2A1A06	J18B-06	2B2B7-B2*		5- 79	A/Q/E REG DISPLAY BIT 15	AQE15
2A1A06	J18B-07	2B2B7-B3*		5- 79	A/Q/E REG DISPLAY BIT 16	AQE16
2A1A06	J18B-08	2B2B7-F2*		5- 79	A/Q/E REG DISPLAY BIT 17	AQE17
2A1A06	J18B-09	2B2B7-F3*		5- 79	A/Q/E REG DISPLAY BIT 18	AQE18
2A1A06	J18B-10	2B2B7-G3*		5- 79	A/Q/E REG DISPLAY BIT 19	AQE19
2A1A06	J18C-01	2B2B7-K2*		5- 79	A/Q/E REG DISPLAY BIT 20	AQE20
2A1A06	J18C-02	2B2B7-K3*		5- 79	A/Q/E REG DISPLAY BIT 21	AQE21
2A1A06	J18C-03	2B2B7-J3*		5- 79	A/Q/E REG DISPLAY BIT 22	AQE22
2A1A06	J18C-04	2B2B7-P2*		5- 79	A/Q/E REG DISPLAY BIT 23	AQE23
2A1A06	J18C-07	2B2B6-A0*		5- 81	GATE FOR A/Q, B REG. DISPLAYS	ABQ
2A1A06	J18C-08	2B2B6-B1*		5- 81	F GATE LOWER DISPLAY	FGTLOW
2A1A06	J18C-09	2B2B6-B0*		5- 81	F GATE MIDDLE DISPLAY	FGTMID
2A1A06	J18C-10	2B2B6-F1*		5- 81	F GATE UPPER DISPLAY	FGTUP
2A1A06	J18D-02	2B2B6-G1*		5- 81	GO INDICATOR - CONSOLE SWITCH	GO
2A1A06	J18D-03	2B2B6-L0*		5- 81	INDICATOR FOR DISPLAY C	DISC
2A1A06	J18D-04	2B2B6-K0*		5- 81	SWEEP/ENTER CONTINUOUS IND	SENT
2A1A06	J18D-05	2B2B6-K1*		5- 81	STOP SWITCH INDICATOR	STOP
2A1A06	J18D-06	2B2B6-Q0*		5- 81	AUTO DUMP SWITCH INDICATOR	ADUMP
2A1A06	J18D-07	2B2B6-P0*		5- 81	AUTO LOAD SWITCH INDICATOR	ALOAD
2A1A06	J18D-08	2B2B6-P1*		5- 81	TYPEWRITER FINISH INDICATOR	TWFN
2A1A06	J18D-09	2B2B6-U0*		5- 81	TYPEWRITER REPEAT INDICATOR	TWRP
2A1A06	J18D-10	2B2B6-U1*		5- 81	DISABLE STOR PROTECT INDICATOR	DISSP
2A1A06	J18E-01	2B2B6-A3*		5- 81	ENTER AUTO PROGRAM DISPLAY	ENTAP
2A1A06	J18F-02	2B2B6-K3*		5- 81	BACKGROUND LIGHT IN OSR	DISOSR
2A1A06	J18F-03	2B2B6-L3*		5- 81	OSR BIT 0 TO CONSOLE DISPLAY	OSR0
2A1A06	J18F-04	2B2B6-P2*		5- 81	OSR BIT 1 TO CONSOLE DISPLAY	OSR1
2A1A06	J18F-05	2B2B6-P3*		5- 81	OSR BIT 2 TO CONSOLE DISPLAY	OSR2
2A1A06	J18F-06	2B2B6-Q3*		5- 81	ISR BIT 0 TO CONSOLE DISPLAY	ISR0
2A1A06	J18F-07	2B2B6-U3*		5- 81	ISR BIT 1 TO CONSOLE DISPLAY	ISR1
2A1A06	J18F-08	2B2B6-U2*		5- 81	ISR BIT 2 TO CONSOLE DISPLAY	ISR2
2A1A06	J20A-01	2B2B5-R0*		5- 83	P BIT 00 TO CSL DISPLAY	PREG00

CONNECTOR		ORIGIN
2A1A06	J20A-02	2B2B5-F1*
2A1A06	J20A-03	2B2B5-F0*
2A1A06	J20A-04	2B2B5-G1*
2A1A06	J20A-05	2B2B5-L0*
2A1A06	J20A-06	2B2B5-K0*
2A1A06	J20A-07	2B2B5-K1*
2A1A06	J20A-08	2B2B5-Q0*
2A1A06	J20A-09	2B2B5-P0*
2A1A06	J20A-10	2B2B5-P1*
2A1A06	J20B-01	2B2B5-U0*
2A1A06	J20B-02	2B2B5-U1*
2A1A06	J20B-03	2B2B5-A3*
2A1A06	J20B-04	2B2B5-B2*
2A1A06	J20B-05	2B2B5-B3*
2A1A06	J20B-07	2B2B5-F2*
2A1A06	J20B-08	2B2B5-F3*
2A1A06	J20B-09	2B2B5-G3*
2A1A06	J20B-10	2B2B5-K2*
2A1A06	J20C-01	2B2B5-K3*
2A1A06	J20C-02	2B2B5-L3*
2A1A06	J20C-03	2B2B5-P2*
2A1A06	J20C-04	2B2B5-P3*
2A1A06	J20C-05	2B2B5-Q3*
2A1A06	J20C-06	2B2B5-U3*
2A1A06	J20C-07	2B2B5-U2*
2A1A06	J20C-08	2B2B4-A0*
2A1A06	J20C-09	2B2B4-B1*
2A1A06	J20C-10	2B2B4-B0*
2A1A06	J20D-01	2B2B4-F1*
2A1A06	J20D-02	2B2B4-F0*
2A1A06	J20D-03	2B2B4-G1*
2A1A06	J20D-04	2B2B4-L0*
2A1A06	J20D-05	2B2B4-K0*
2A1A06	J20D-06	2B2B4-K1*
2A1A06	J20D-07	2B2B4-Q0*
2A1A06	J20D-08	2B2B4-P0*
2A1A06	J20D-09	2B2B4-P1*
2A1A06	J20D-10	2B2B4-U0*
2A1A06	J20E-01	2B2B4-U1*
2A1A06	J20E-02	2B2B4-A3*
2A1A06	J20E-03	2B2B4-B2*
2A1A06	J20E-04	2B2B4-B3*
2A1A06	J20E-05	2B2B4-F2*
2A1A06	J20E-06	2B2B4-F3*
2A1A06	J20E-07	2B2B4-G3*
2A1A06	J20E-08	2B2B4-K2*
2A1A06	J21A-02*01	2B2B6-T2/T3
2A1A06	J21A-04*03	2B2B6-W2/W3
2A1A06	J21A-06*05	2B2B6-X2/X3
2A1A06	J21A-08*07	2B2B6-Q3/Q2
2A1A06	J21A-10*09	2B2B6-R2/R3
2A1A06	J21B-02*01	2B2B6-S2/S3
2A1A06	J21B-04*03	2B2B5-C0/C1
2A1A06	J21B-06*05	2B2B5-J1/J0
2A1A06	J21B-08*07	2B2B5-I0/I1
2A1A06	J21B-10*09	2B2B6-S0/S1
2A1A06	J21C-02*01	2B2B6-T0/T1
2A1A06	J21C-04*03	2B2B6-F1/E0
2A1A06	J21D-02*01	2B2B6-N0/N1
2A1A06	J21D-04*03	2B2B6-H0/H1
2A1A06	J21D-06*05	2B2B6-M0/M1
2A1A06	J21D-08*07	2B2B2-X0/X1
2A1A06	J21E-02*01	2B2B6-01/00
2A1A06	J21E-04*03	2B2B4-M2/M3
2A1A06	J21E-06*05	2B2B5-M2/M3
2A1A06	J21E-08*07	2B2B5-S2/S3
2A1A06	J21E-10*09	2B2B4-E1/E0
2A1A06	J21F-02*01	2B2B4-I0/I1
2A1A06	J21F-04*03	2B2B4-M0/M1
2A1A06	J21F-06*05	2B2B4-X0/X1
2A1A06	J21F-08*07	2B2B4-E3/E2
2A1A06	J22A-01	2B2B3-F1*
2A1A06	J22A-02	2B2B3-F0*
2A1A06	J22A-03	2B2B3-G1*

PAGE	DEFINITION	SIG NAME
5- 83	P BIT 01 TO CSL DISPLAY	PREG01
5- 83	P BIT 02 TO CSL DISPLAY	PREG02
5- 83	P BIT 03 TO CSL DISPLAY	PREG03
5- 83	P BIT 04 TO CSL DISPLAY	PREG04
5- 83	P BIT 05 TO CSL DISPLAY	PREG05
5- 83	P BIT 06 TO CSL DISPLAY	PREG06
5- 83	P BIT 07 TO CSL DISPLAY	PREG07
5- 83	P BIT 08 TO CSL DISPLAY	PREG08
5- 83	P BIT 09 TO CSL DISPLAY	PREG09
5- 83	P BIT 10 TO CSL DISPLAY	PREG10
5- 83	P BIT 11 TO CSL DISPLAY	PREG11
5- 83	P BIT 12 TO CSL DISPLAY	PREG12
5- 83	P BIT 13 TO CSL DISPLAY	PREG13
5- 83	P BIT 14 TO CSL DISPLAY	PREG14
5- 83	C/F BIT 00 TO CONSOLE DISPLAY	CF00
5- 83	C/F BIT 01 TO CONSOLE DISPLAY	CF01
5- 83	C/F BIT 02 TO CONSOLE DISPLAY	CF02
5- 83	BACKGROUND DIGIT 0 C DISPLAY	BB0
5- 83	C/F BIT 03 TO CONSOLE DISPLAY	CF03
5- 83	C/F BIT 04 TO CONSOLE DISPLAY	CF04
5- 83	C/F BIT 05 TO CONSOLE DISPLAY	CF05
5- 83	BACKGROUND DIGIT 1 C DISPLAY	BB1
5- 83	C/F BIT 06 TO CONSOLE DISPLAY	CF06
5- 83	C/F BIT 07 TO CONSOLE DISPLAY	CF07
5- 83	C/F BIT 08 TO CONSOLE DISPLAY	CF08
5- 85	BACKGROUND DIGIT 2 C DISPLAY	BB2
5- 85	C/F BIT 09 TO CONSOLE DISPLAY	CF09
5- 85	C/F BIT 10 TO CONSOLE DISPLAY	CF10
5- 85	C/F BIT 11 TO CONSOLE DISPLAY	CF11
5- 85	BACKGROUND DIGIT 3 C DISPLAY	BB3
5- 85	C/F BIT 12 TO CONSOLE DISPLAY	CF12
5- 85	C/F BIT 13 TO CONSOLE DISPLAY	CF13
5- 85	C/F BIT 14 TO CONSOLE DISPLAY	CF14
5- 85	BACKGROUND DIGIT 4 C DISPLAY	BB4
5- 85	C/F BIT 15 TO CONSOLE DISPLAY	CF15
5- 85	C/F BIT 16 TO CONSOLE DISPLAY	CF16
5- 85	C/F BIT 17 TO CONSOLE DISPLAY	CF17
5- 85	BACKGROUND DIGIT 5 C DISPLAY	BB5
5- 85	C/F BIT 18 TO CONSOLE DISPLAY	CF18
5- 85	C/F BIT 19 TO CONSOLE DISPLAY	CF19
5- 85	C/F BIT 20 TO CONSOLE DISPLAY	CF20
5- 85	BACKGROUND DIGIT 6 C DISPLAY	BB6
5- 85	C/F BIT 21 TO CONSOLE DISPLAY	CF21
5- 85	C/F BIT 22 TO CONSOLE DISPLAY	CF22
5- 85	C/F BIT 23 TO CONSOLE DISPLAY	CF23
5- 85	BACKGROUND DIGIT 7 C DISPLAY	BB7
5- 81	ISR ,BIT 0	$ISRLT0
5- 81	ISR ,BIT 1	$ISRLT1
5- 81	ISR ,BIT 2	$ISRLT2
5- 81	OSR ,BIT 0	$OSRLT0
5- 81	OSR BIT 1	$OSRLT1
5- 81	OSR ,BIT 2	$OSRLT2
5- 83	B DISPLAY, BIT 0	$B-LT00
5- 83	B DISPLAY, BIT 1	$B-LT01
5- 83	B DISPLAY, BIT 2	$B-LT02
5- 81	AUTO LOAD LIGHT	$AL-LT
5- 81	AUTO DUMP LIGHT	$AD-LT
5- 81	GATE A,Q,E REGISTER DISPLAY	$AQBGT
5- 81	SWEEP-ENTER CONTINUOUS FF SET	$SECNLT
5- 81	NOT (GO FF)	$GO-LT
5- 81	STOP FF	$STOPLT
5- 89	MEMORY ERROR FF	$MPE-LT
5- 81	C0 DISPLAY INDICATOR	$C0-LT
5- 85	BOUNCING BALL, OCTAL DIGIT 7	$BB-LT7
5- 83	BOUNCING BALL, OCTAL DIGIT 0	$BB-LT0
5- 83	BOUNCING BALL, OCTAL DIGIT 1	$BB-LT1
5- 85	BOUNCING BALL, OCTAL DIGIT 2	$BB-LT2
5- 85	BOUNCING BALL, OCTAL DIGIT 3	$BB-LT3
5- 85	BOUNCING BALL, OCTAL DIGIT 4	$BB-LT4
5- 85	BOUNCING BALL, OCTAL DIGIT 5	$BB-LT5
5- 85	BOUNCING BALL, OCTAL DIGIT 6	$BB-LT6
5- 87	CHANNEL 2 REJECT INDICATOR	C2REJ
5- 87	CHANNEL 3 REJECT INDICATOR	C3REJ
5- 87	CHANNEL 4 REJECT INDICATOR	C4REJ

CONNECTOR		ORIGIN
2A1A06	J22A-04	2B2B3-L0*
2A1A06	J22A-05	2B2B3-K0*
2A1A06	J22A-06	2B2B3-K1*
2A1A06	J22A-07	2B2B3-Q0*
2A1A06	J22A-08	2B2B3-P0*
2A1A06	J22A-09	2B2B3-P1*
2A1A06	J22A-10	2B2B3-U0*
2A1A06	J22B-01	2B2B3-U1*
2A1A06	J22B-02	2B2B3-A3*
2A1A06	J22B-03	2B2B3-B2*
2A1A06	J22B-04	2B2B3-B3*
2A1A06	J22B-05	2B2B3-F2*
2A1A06	J22B-06	2B2B3-F3*
2A1A06	J22B-07	2B2B3-G3*
2A1A06	J22B-08	2B2B3-K2*
2A1A06	J22B-09	2B2B3-K3*
2A1A06	J22B-10	2B2B3-L3*
2A1A06	J22C-01	2B2B3-P2*
2A1A06	J22C-02	2B2B3-P3*
2A1A06	J22C-08	2B2B2-A0*
2A1A06	J22C-09	2B2B2-B1*
2A1A06	J22C-10	2B2B2-B0*
2A1A06	J22D-01	2B2B2-F1*
2A1A06	J22D-02	2B2B2-F0*
2A1A06	J22D-03	2B2B2-G1*
2A1A06	J22D-04	2B2B2-L0*
2A1A06	J22D-05	2B2B2-K0*
2A1A06	J22D-06	2B2B2-K1*
2A1A06	J22D-07	2B2B2-Q0*
2A1A06	J22D-08	2B2B2-P0*
2A1A06	J22D-09	2B2B2-P1*
2A1A06	J22D-10	2B2B2-U0*
2A1A06	J22E-01	2B2B2-U1*
2A1A06	J22E-02	2B2B2-A3*
2A1A06	J22E-03	2B2B2-B2*
2A1A06	J22E-04	2B2B2-B3*
2A1A06	J22E-05	2B2B2-F2*
2A1A06	J22E-06	2B2B2-F3*
2A1A06	J22E-07	2B2B2-G3*
2A1A06	J22E-08	2B2B2-K2*
2A1A06	J22E-09	2B2B2-K3*
2A1A06	J22E-10	2B2B2-L3*
2A1A06	J22F-01	2B2B2-P2*
2A1A06	J22F-02	2B2B2-P3*
2A1A06	J22F-03	2B2B2-Q3*
2A1A06	J22F-04	2B2B2-U3*
2A1A06	J22F-05	2B2B2-U2*
2A1A06	J22F-06	2B2B3-A0*
2A1A06	J22F-07	2B2B3-B1*
2A1A06	J22F-08	2B2B3-B0*
2A1A06	J25A-02/01	2B0A9-R2*R3
2A1A06	J26A-02*01	2B0A8-W0/W1
2A1A06	P01A-02/01	2B2A9-E3*E2
2A1A06	P01A-04/03	2B2A9-N3*N2
2A1A06	P01A-06/05	2B2A9-W3*W2
2A1A06	P01A-08/07	2B2A8-E3*E2
2A1A06	P01A-10/09	2B2A8-N3*N2
2A1A06	P01B-02/01	2B2A8-W3*W2
2A1A06	P01B-04/03	2B2A7-E3*E2
2A1A06	P01B-06/05	2B2A7-N3*N2
2A1A06	P01B-08/07	2B2A7-W3*W2
2A1A06	P01B-10/09	2B2A6-E3*E2
2A1A06	P01C-02/01	2B2A6-N3*N2
2A1A06	P01C-04/03	2B2A6-W3*W2
2A1A06	P01C-06/05	2B2A4-E3*E2
2A1A06	P01C-08/07	2B2A4-N3*N2
2A1A06	P01C-10/09	2B2A4-W3*W2
2A1A06	P01D-02*01	2B2A9-E1/E0
2A1A06	P01D-04*03	2B2A9-P1/P0
2A1A06	P01D-06*05	2B2A9-X1/X0
2A1A06	P01D-08*07	2B2A8-E1/E0
2A1A06	P01D-10*09	2B2A8-P1/P0

PAGE	DEFINITION	SIG NAME
5- 87	CHANNEL 5 REJECT INDICATOR	C5REJ
5- 87	CHANNEL 6 REJECT INDICATOR	C6REJ
5- 87	CHANNEL 7 REJECT INDICATOR	C7REJ
5- 87	CHANNEL 0 INTERRUPT INDICATOR	C0INT
5- 87	CHANNEL 1 INTERRUPT INDICATOR	C1INT
5- 87	CHANNEL 2 INTERRUPT INDICATOR	C2INT
5- 87	CHANNEL 3 INTERRUPT INDICATOR	C3INT
5- 87	CHANNEL 4 INTERRUPT INDICATOR	C4INT
5- 87	CHANNEL 5 INTERRUPT INDICATOR	C5INT
5- 87	CHANNEL 6 INTERRUPT INDICATOR	C6INT
5- 87	CHANNEL 7 INTERRUPT INDICATOR	C7INT
5- 87	CHANNEL 0 PAR. ERR. INDICATOR	C0PTE
5- 87	CHANNEL 1 PAR. ERR. INDICATOR	C1PTE
5- 87	CHANNEL 2 PAR. ERR. INDICATOR	C2PTE
5- 87	CHANNEL 3 PAR. ERR. INDICATOR	C3PTE
5- 87	CHANNEL 4 PAR. ERR. INDICATOR	C4PTE
5- 87	CHANNEL 5 PAR. ERR. INDICATOR	C5PTE
5- 87	CHANNEL 6 PAR. ERR. INDICATOR	C6PTE
5- 87	CHANNEL 7 PAR. ERR. INDICATOR	C7PTE
5- 89	MONITOR STATE INDICATOR	MONT
5- 89	PROGRAM STATE INDICATOR	PROG
5- 89	INTERRUPT ENABLED INDICATOR	ENIT
5- 89	RNI CYCLE INDICATOR	RNI
5- 89	RADR CYCLE INDICATOR	RADR
5- 89	ROP CYCLE INDICATOR	ROPR
5- 89	STOR CYCLE INDICATOR	STORE
5- 89	ARITHMETIC OVERFLOW INDICATOR	ARITH
5- 89	DIVIDE FAULT INDICATOR	DIVF
5- 89	EXPONENT OVERFLOW INDICATOR	EXPOT
5- 89	BCD FAULT INDICATOR	BCDF
5- 89	ILLEGAL WRITE INDICATOR	ILLWR
5- 89	STORAGE PARITY ERROR INDICATOR	MPE
5- 89	CHANNEL 0 READ INDICATOR, CONSOLE	C0READ
5- 89	1	C1READ
5- 89	2	C2READ
5- 89	3	C3READ
5- 89	4	C4READ
5- 89	5	C5READ
5- 89	6	C6READ
5- 89	7	C7READ
5- 89	CHANNEL 0 WRITE INDICATOR	C0WR
5- 89	CHAN 1 WRITE INDICATOR,CONSOLE	C1WR
5- 89	CHAN 2 WRITE INDICATOR,CONSOLE	C2WR
5- 89	CHAN 3 WRITE INDICATOR,CONSOLE	C3WR
5- 89	CHAN 4 WRITE INDICATOR,CONSOLE	C4WR
5- 89	CHAN 5 WRITE INDICATOR,CONSOLE	C5WR
5- 89	CHAN 6 WRITE INDICATOR,CONSOLE	C6WR
5- 87	CHAN 7 WRITE INDICATOR,CONSOLE	C7WR
5- 87	CHANNEL 0 REJECT INDICATOR	C0REJ
5- 87	CHANNEL 1 REJECT INDICATOR	C1REJ
6-101	EXT INTERRUPT - ASSOC PROC	$EXTIOC
6-109	EXT INTERRUPT - ASSOC PROC	$EXTITC
5- 57	NOT MAIN CONTROL READ, BIT 00	$MCRD00
5- 57	NOT MAIN CONTROL READ, BIT 01	$MCRD01
5- 57	NOT MAIN CONTROL READ, BIT 02	$MCRD02
5- 59	NOT MAIN CONTROL READ, BIT 03	$MCRD03
5- 59	NOT MAIN CONTROL READ, BIT 04	$MCRD04
5- 59	NOT MAIN CONTROL READ, BIT 05	$MCRD05
5- 61	NOT MAIN CONTROL READ, BIT 06	$MCRD06
5- 61	NOT MAIN CONTROL READ, BIT 07	$MCRD07
5- 61	NOT MAIN CONTROL READ, BIT 08	$MCRD08
5- 63	NOT MAIN CONTROL READ, BIT 09	$MCRD09
5- 63	NOT MAIN CONTROL READ, BIT 10	$MCRD10
5- 63	NOT MAIN CONTROL READ, BIT 11	$MCRD11
5- 65	NOT MAIN CONTROL READ, BIT 12	$MCRD12
5- 65	NOT MAIN CONTROL READ, BIT 13	$MCRD13
5- 65	NOT MAIN CONTROL READ, BIT 14	$MCRD14
5- 57	NOT DO REGISTER BIT 00	$MCWR00
5- 57	NOT DO REGISTER BIT 01	$MCWR01
5- 59	NOT DO REGISTER BIT 02	$MCWR02
5- 59	NOT DO REGISTER BIT 03	$MCWR03
5- 59	NOT DO REGISTER BIT 04	$MCWR04

CONNECTOR		ORIGIN	PAGE	DEFINITION	SIG NAME
2A1A06	P01E-02*01	2B2A8-X1/X0	5- 59	NOT DO REGISTER BIT 05	$MCWR05
2A1A06	P01E-04*03	2B2A7-F1/E0	5- 61	NOT DO REGISTER BIT 06	$MCWR06
2A1A06	P01E-06*05	2B2A7-P1/P0	5- 61	NOT DO REGISTER BIT 07	$MCWR07
2A1A06	P01E-08*07	2B2A7-X1/X0	5- 61	NOT DO REGISTER BIT 08	$MCWR08
2A1A06	P01E-10*09	2B2A6-E1/E0	5- 63	NOT DO REGISTER BIT 09	$MCWR09
2A1A06	P01F-02*01	2B2A6-P1/P0	5- 63	NOT DO REGISTER BIT 10	$MCWR10
2A1A06	P01F-04*03	2B2A6-X1/X0	5- 63	NOT DO REGISTER BIT 11	$MCWR11
2A1A06	P01F-06*05	2B2A4-E1/E0	5- 65	NOT DO REGISTER BIT 12	$MCWR12
2A1A06	P01F-08*07	2B2A4-P1/P0	5- 65	NOT DO REGISTER BIT 13	$MCWR13
2A1A06	P02A-02/01	2B0A8-M1*M0	6-109	SELECTED STATUS BIT 00 TO DO	$COPY00
2A1A06	P02A-04/03	2B0A8-H1*H0	6-109	SELECTED STATUS BIT 01 TO DO	$COPY01
2A1A06	P02A-06/05	2B0A7-U3*U2	6-117	SELECTED STATUS BIT 02 TO DO	$COPY02
2A1A06	P02A-08/07	2B0A7-X3*X2	6-117	SELECTED STATUS BIT 03 TO DO	$COPY03
2A1A06	P02A-10/09	2B0A8-I1*I0	6-109	SELECTED STATUS BIT 04 TO DO	$COPY04
2A1A06	P02B-02/01	2B0A8-K0*K1	6-109	SELECTED STATUS BIT 05 TO DO	$COPY05
2A1A06	P02B-04/03	2B0A7-V3*V2	6-117	SELECTED STATUS BIT 06 TO DO	$COPY06
2A1A06	P02B-06/05	2B0A7-S3*S2	6-117	SELECTED STATUS BIT 07 TO DO	$COPY07
2A1A06	P02B-08/07	2B0A7-B0*B1	6-117	SELECTED STATUS BIT 08 TO DO	$COPY08
2A1A06	P02B-10/09	2B0A7-E0*E1	6-117	SELECTED STATUS BIT 09 TO DO	$COPY09
2A1A06	P02C-02/01	2B0A7-B2*B3	6-117	SELECTED STATUS BIT 10 TO DO	$COPY10
2A1A06	P02C-04/03	2B0A7-E2*E3	6-117	SELECTED STATUS BIT 11 TO DO	$COPY11
2A1A06	P02C-06/05	2B0B7-G1*G0	6-113	NOT CHAN 0 INT MASK TO DO	$COPY12
2A1A06	P02C-08/07	2B0B7-I0*I1	6-113	NOT CHAN 1 INT MASK TO DO	$COPY13
2A1A06	P02C-10/09	2B0B6-G1*G0	6-115	NOT CHAN 2 INT MASK TO DO	$COPY14
2A1A06	P02D-02*01	2A1B5-I0/I1	6- 45	F0 REGISTER BIT 0	$F0BC00
2A1A06	P02D-04*03	2A1B5-N1/N0	6- 45	F0 REGISTER BIT 1	$F0BC01
2A1A06	P02D-06*05	2A1B5-J2/J3	6- 45	F0 REGISTER BIT 2	$F0BC02
2A1A06	P02D-08*07	2A1B5-N3/N2	6- 45	F0 REGISTER BIT 3	$F0BC03
2A1A06	P02D-10*09	2A1A5-Q1/Q0	6- 47	F0 REGISTER BIT 4	$F0BC04
2A1A06	P02E-02*01	2A1A5-Q3/Q2	6- 47	F0 REGISTER BIT 6	$F0BC06
2A1A06	P02E-04*03	2A1A5-R3/R2	6- 47	F0 REGISTER BIT 7	$F0BC07
2A1A06	P02E-06*05	2A1A6-Q1/Q0	6- 49	F0 REGISTER BIT 8	$F0BC08
2A1A06	P02E-08*07	2A1A6-R1/R0	6- 49	F0 REGISTER BIT 9	$F0BC09
2A1A06	P02E-10*09	2A1A6-Q3/Q2	6- 49	F0 REGISTER BIT 10	$F0BC10
2A1A06	P02F-02*01	2A1A6-R3/R2	6- 49	F0 REGISTER BIT 11	$F0BC11
2A1A06	P02F-04*03	2A1A7-Q1/Q0	6- 51	F0 REGISTER BIT 12	$F0BC12
2A1A06	P02F-06*05	2A1A7-R1/R0	6- 51	F0 REGISTER BIT 13	$F0BC13
2A1A06	P02F-08*07	2A1A7-Q3/Q2	6- 51	F0 REGISTER BIT 14	$F0BC14
2A1A06	P03A-02/01	2A2A5-Q1*Q0	5- 3	SET ILLEGAL WRITE	$SETIW
2A1A06	P03A-04/03	2B2B9-R1*R0	5- 75	BLOCK CONTROL PRIORITY	$BCPRIO
2A1A06	P03A-06/05	2B2A5-T1*T0	5- 73	STORAGE PARITY ERROR INTERRUPT	$MPEINT
2A1A06	P03A-08*07	2A2A5-J1/J0	5- 3	MONITOR STATE	$MONREF
2A1A06	P03A-10*09	2A2A5-M1/M0	5- 3	MAIN CONT WRITE SIGNAL TO PF	$MCWR
2A1A06	P03B-02*01	2A2A5-V3/V2	5- 3	WRITE PF	$WPF
2A1A06	P03B-04*03	2A2A5-W3/W2	5- 3	READ PF	$RPF
2A1A06	P03B-06*05	2A2A5-T0/I1	5- 3	STORE CYCLE+INT. PROCESSING	$INTSTO
2A1A06	P03B-08/07	2B2B8-L0*L1	5- 77	INTERRUPT CODE BIT 6	$ICODE6
2A1A06	P03B-10*09	2B2B9-I2/I3	5- 75	MC PARTIAL WRITE BIT 0	$MCPW0
2A1A06	P03C-02*01	2B2B9-K3/K2	5- 75	MC PARTIAL WRITE BIT 1	$MCPW1
2A1A06	P03C-04*03	2B2B8-T2/I3	5- 77	MC PARTIAL WRITE BIT 2	$MCPW2
2A1A06	P03C-06*05	2B2B8-K3/K2	5- 77	MC PARTIAL WRITE BIT 3	$MCPW3
2A1A06	P03C-08*07	2B2B8-V2/V3	5- 77	MC PARTIAL WRITE BIT4 OR DESTRUCTIVE LOAD	$MCPW4 MCPW4
2A1A06	P03C-10*09	2B2B9-F0/F1	5- 75	NOT READ ADDRESS CYCLE	$RADREF
2A1A06	P03D-02*01	2A2B5-C1/C0	5- 19	C4 FAN IN BIT 0(S BUS BIT 15)	$MCSB15
2A1A06	P03D-04*03	2A2B5-E2/E3	5- 19	C4 FAN IN BUT 1(S BUS BIT 16)	$MCSB16
2A1A06	P03D-06*05	2A2B4-G3/G2	5- 21	C4 FAN IN BIT 2(S BUS BIT 17)	$MCSB17
2A1A06	P03D-08*07	2B0A8-R1/R0	6-109	NORMAL INTERRUPT CODE USED	$ICSEEN
2A1A06	P03D-10/09	2B0A8-C3*C2	6-109	(NORMAL INTERRUPTS)(ARITH)	$INFINT
2A1A06	P03E-02*01	2B1B7-G1/G0	6- 3	NOT(EN PAR ERR CODE + M CLR)	$ENPECO
2A1A06	P03E-04/03	2B1B7-V1*V0	6- 3	NORMAL INT XLTN TO MN CONT	$NORINT
2A1A06	P03E-06*05	2B1B7-H1/H0	6- 3	INTERRUPT ENABLED FF	$INTEN
2A1A06	P03E-08*07	2A1B8-K2/K3	6- 53	CIR,BIT 0	$CIRBC0
2A1A06	P03E-10*09	2A1B8-R3/R2	6- 53	CIR,BIT 1	$CIRBC1
2A1A06	P03F-02*01	2A1B8-S3/S2	6- 53	CIR,BIT 2	$CIRBC2
2A1A06	P03F-04*03	2A2A6-H3/H2	5- 1	NOT (EXECUTIVE MODE)	$PFEXMO
2A1A06	P03F-06*05	2A2A6-I0/I1	5- 1	NOT (MASTER CLR +INTERNAL CLR)	$MCLPF
2A1A06	P03F-08*07	2B2B9-V2/V3	5- 75	DISABLE MEMORY PARITY ERROR	$DISMPE
2A1A06	P04A-02/01	2B0B6-I0*I1	6-115	NOT CHAN 3 INT MASK TO DO	$COPY15
2A1A06	P04A-04/03	2B0B7-T0*T1	6-113	NOT CHAN 4 INT MASK TO DO	$COPY16
2A1A06	P04A-06/05	2B0B7-T2*T3	6-113	NOT CHAN 5 INT MASK TO DO	$COPY17
2A1A06	P04A-08/07	2B0B6-T0*T1	6-115	NOT CHAN 6 INT MASK TO DO	$COPY18

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A1A06	P04A-10/09	2B0B6-T2*T3		6-115	NOT CHAN 7 INT MASK TO DO	$COPY19
2A1A06	P04B-02/01	2B0B7-F3*F2		6-113	NOT CLOCK INT MASK TO DO	$COPY20
2A1A06	P04B-04/03	2B0B7-I3*I2		6-113	NOT FP/BDP INT MASK TO DO	$COPY21
2A1A06	P04B-06/05	2B0B6-F3*F2		6-115	NOT ARITH INT MASK TO DO	$COPY22
2A1A06	P04B-08/07	2B0B6-I3*I2		6-115	NOT SRCH + MOVE INT MASK TO DO	$COPY23
2A1A06	P04B-10*09	2B0A9-F1/F0		6-101	F0 REGISTER BIT 15	$F0BC15
2A1A06	P04C-02*01	2B0A9-G1/G0		6-101	F0 REGISTER BIT 16	$F0BC16
2A1A06	P04C-04*03	2B0A9-J1/J0		6-101	F0 REGISTER BIT 17	$F0BC17
2A1A06	P04C-06/05	2B2A3-E3*E2		5- 67	NOT MAIN CONTROL READ, BIT 15	$MCRD15
2A1A06	P04C-08/07	2B2A3-N3*N2		5- 67	NOT MAIN CONTROL READ, BIT 16	$MCRD16
2A1A06	P04C-10/09	2B2A3-W3*W2		5- 67	NOT MAIN CONTROL READ, BIT 17	$MCRD17
2A1A06	P04D-02/01	2B2A2-E3*E2		5- 69	NOT MAIN CONTROL READ, BIT 18	$MCRD18
2A1A06	P04D-04/03	2B2A2-N3*N2		5- 69	NOT MAIN CONTROL READ, BIT 19	$MCRD19
2A1A06	P04D-06/05	2B2A2-W3*W2		5- 69	NOT MAIN CONTROL READ, BIT 20	$MCRD20
2A1A06	P04D-08/07	2B2A1-E3*E2		5- 71	NOT MAIN CONTROL READ, BIT 21	$MCRD21
2A1A06	P04D-10/09	2B2A1-N3*N2		5- 71	NOT MAIN CONTROL READ, BIT 22	$MCRD22
2A1A06	P04E-02/01	2B2A1-W3*W2		5- 71	NOT MAIN CONTROL READ, BIT 23	$MCRD23
2A1A06	P04E-04*03	2B2A3-E1/E0		5- 67	DO REGISTER BIT 15	$MCWR15
2A1A06	P04E-06*05	2B2A3-P1/P0		5- 67	DO REGISTER BIT 16	$MCWR16
2A1A06	P04E-08*07	2B2A3-X1/X0		5- 67	DO REGISTER BIT 17	$MCWR17
2A1A06	P04E-10*09	2B2A2-E1/E0		5- 69	DO REGISTER BIT 18	$MCWR18
2A1A06	P04F-02*01	2B2A2-P1/P0		5- 69	DO REGISTER BIT 19	$MCWR19
2A1A06	P04F-04*03	2B2A2-X1/X0		5- 69	DO REGISTER BIT 20	$MCWR20
2A1A06	P04F-06*05	2B2A1-E1/E0		5- 71	DO REGISTER BIT 21	$MCWR21
2A1A06	P04F-08*07	2B2A1-P1/P0		5- 71	DO REGISTER BIT 22	$MCWR22
2A1A06	P05A-02*01	2B1A9-I1/I0		6- 23	F0 REGISTER BIT 18	$F0BC18
2A1A06	P05A-04*03	2B1A9-H1/H0		6- 23	F0 REGISTER BIT 19	$F0BC19
2A1A06	P05A-06*05	2B1A9-M1/M0		6- 23	F0 REGISTER BIT 20	$F0BC20
2A1A06	P05A-08*07	2B1A9-P3/P2		6- 23	F0 REGISTER BIT 21	$F0BC21
2A1A06	P05A-10*09	2B1A9-W1/W0		6- 23	F0 REGISTER BIT 22	$F0BC22
2A1A06	P05B-02*01	2B1A9-X1/X0		6- 23	F0 REGISTER BIT 23	$F0BC23
2A1A06	P05B-04*03	2B1B8-E3/E2		6- 11	INIT. RNI 2 CYCLE FF	$BCRNI2
2A1A06	P05B-06*05	2B1B8-G3/G2		6- 11	REQUEST BC PULSE	$REQBC
2A1A06	P05B-08*07	2B1B1-S0/S1		6- 9	FUNCTION STABLE TO BLOCK CONT	$FNSTBC
2A1A06	P05B-10*09	2B1B1-E3/E2		6- 9	NOT(TEST BUSY) SIG TO B CONT)	$TSBSY
2A1A06	P05C-02*01	2A1B6-T1/T0		6- 43	D0 TO BLOCK CONT, BIT 18	$D0BC18
2A1A06	P05C-04*03	2A1B6-S0/S1		6- 43	D0 TO BLOCK CONT, BIT 19	$D0BC19
2A1A06	P05C-06*05	2A1B8-G3/G2		6- 53	D0 TO BLOCK CONT, BIT 21	$D0BC21
2A1A06	P05C-08*07	2A1B8-F2/F3		6- 53	D0 TO BLOCK CONT, BIT 22	$D0BC22
2A1A06	P05C-10*09	2A1B8-L2/L3		6- 53	NOT (D0 TO BLOCK CONT, BIT 23)	$D0BC23
2A1A06	P05D-02*01	2B0B5-N0/N1		6-107	PAUSE FF TO 40 MS. DELAY	$T040MS
2A1A06	P05D-04*03	2A2A5-J2/J3		5- 3	OPERAND REFERENCE	$OPREF
2A1A06	P05D-06*05	2B2B9-C0/C1		5- 75	OPERAND REFERENCE	$OPREFS
2A1A06	P05D-08*07	2A1A5-R1/R0		6- 47	F0 REGISTER BIT 5	$F0BC05
2A1A06	P05D-10/09	2B1B6-W0*W1		6- 15	BC REPLY 2 TO MN CONT	$BCRPY2
2A1A06	P05E-02/01	2B1B6-R1*R0		6- 15	BC REPLY 1 TO MN CONT	$BCRPY1
2A1A06	P05E-04/03	2B1B1-Q1*Q0		6- 9	SELECTED CHAN BUSY + REJECT CONN + FCN	$CHBUSY
2A1A06	P05E-06/05	2B0A9-X3*X2		6-101	SEL STATUS = ANY BIT OF F L12	$BCCMPR
2A1A06	P05E-08/07	2B0B8-C3*C2		6-111	NOT F BIT 08 + 09 + 10 TO MN CONT	$080910
2A1A06	P05E-10*09	2B0A9-W1/W0		6-101	BC NOT COMPARE FF	$BCSKIP
2A1A06	P05F-02/01	2B0B5-Q0*Q1		6-107	FROM 40 MS DELAY	$FM40MS
2A1A06	P05F-04/03	2A2B9-Q0*Q1		5- 23	STORAGE NO RESPONSE	$NORESP
2A1A06	P05F-06*05	2B2A1-X1/X0		5- 71	DO REGISTER BIT 13	$MCWR23
2A1A06	P05F-07	J01U-03*	2A4A15		INTERRUPT BIAS SWITCH FOR BIT6	INTSW6
2A1A06	P05F-08	J01T-03*	2A4A15		INTERRUPT BIAS SWITCH FOR BIT7	INTSW7
2A1A06	P06A-02*01	2B0A7-H3/H2		6-117	SET DIVIDE FAULT FF	$STDIVF
2A1A06	P06A-04*03	2B0A7-H0/H1		6-117	SET OVERFLOW FF	$STOVER
2A1A06	P06A-06*05	2B1A7-H1/H0		6- 1	NOT BIT 09 OF MAINT.REGISTER	$M0BC09
2A1A06	P06A-08*07	2B1A8-E2/E3		6- 17	NOT BIT 10 OF MAINT.REGISTER	$M0BC10
2A1A06	P06A-10*09	2B1B0-F1/F0		6- 7	NOT (EXEC MODE) SIGNAL TO B.C.	$BCEXM0
2A1A06	P06B-02*01	2B1A7-E0/E1		6- 1	NOT (MASTER CLR +EXTERNAL CLR)	$EXCLBC
2A1A06	P06B-04*03	2B1A7-L2/L3		6- 1	NOT (MASTER CLR +INTERNAL CLR)	$INCLBC
2A1A06	P06B-05*06	2B1B8-F3/F2		6- 11	READ OR WRITE REGISTER FILE	$RWRF
2A1A06	P06B-07	J03P-03*	2A2A04		NOT (SEL. BITS 08-15 OF MAINT)	M0LT-2
2A1A06	P06B-08	J03R-03*	2A2A04		NOT (SEL. BITS 16-23 OF MAINT)	M0LT-3
2A1A06	P06C-02/01	2B2B9-T2*T3		5- 75	AUTO-STEP OSCILLATOR	$ASOSC
2A1A06	P06C-04/03	2B0A4-J3*J2		6-103	NOT CHAN 0-7 TERMINATE TO BC	$CHTERM
2A1A06	P06C-06*05	2B0A5-X1/X0		6-123	NOT (G0 FF) TO BC	$G0=BC
2A1A06	P06C-08*07	2B2B2-C0/C1		5- 89	INTERRUPT ENABLED FF	$IEN-LT
2A1A06	P06C-10*09	2B2B6-N2/N3		5- 81	OSR BACKGROUND LIGHT	$OSR-LT

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A04	J01C-02/01	2A2A8-B3*B2		5- 9	STOR ADDR BIT 02 TO INDICATOR	$S02L
2A2A04	J01D-02/01	2A2A8-C2*C3		5- 9	STOR ADDR BIT 03 TO INDICATOR	$S03L
2A2A04	J01D-03*	2A2B9-E1		5- 23	UP. STOR PROTECT BIT 10 SW = 1	SP10S1
2A2A04	J01E-02/01	2A2A8-K2*K3		5- 9	STOR ADDR BIT 04 TO INDICATOR	$S04L
2A2A04	J01F-02/01	2A2A8-J0*J1		5- 9	STOR ADDR BIT 05 TO INDICATOR	$S05L
2A2A04	J01F-03*	2A2B9-D3		5- 23	UP. STOR PROTECT BIT 11 SW = 1	SP11S1
2A2A04	J01G-02/01	2A2A8-E0*E1		5- 9	STOR ADDR BIT 06 TO INDICATOR	$S06L
2A2A04	J01H-02/01	2A2A8-B1*B0		5- 9	STOR ADDR BIT 07 TO INDICATOR	$S07L
2A2A04	J01H-03*	2A2B9-H3		5- 23	UP. STOR PROTECT BIT 12 SW = 1	SP12S1
2A2A04	J01J-02/01	2A2A8-D0*D1		5- 9	STOR ADDR BIT 08 TO INDICATOR	$S08L
2A2A04	J01K-02/01	2A2A9-H3*H2		5- 11	RELOC ADDR BIT 09 TO INDICATOR	$S09RL
2A2A04	J01K-03*	2A2B9-03		5- 23	UP. STOR PROTECT BIT 13 SW = 1	SP13S1
2A2A04	J01L-02/01	2A2A9-E2*E3		5- 11	RELOC ADDR BIT 10 TO INDICATOR	$S10RL
2A2A04	J01M-02/01	2A2A9-B3*B2		5- 11	RELOC ADDR BIT 11 TO INDICATOR	$S11RL
2A2A04	J01M-03*	2A2B9-S3		5- 23	UP. STOR PROTECT BIT 14 SW = 1	SP14S1
2A2A04	J01N-02/01	2A2A9-C2*C3		5- 11	RELOC ADDR BIT 12 TO INDICATOR	$S12RL
2A2A04	J01P-02/01	2A2A9-K2*K3		5- 11	RELOC ADDR BIT 13 TO INDICATOR	$S13RL
2A2A04	J01R-02/01	2A2A9-J0*J1		5- 11	RELOC ADDR BIT 14 TO INDICATOR	$S14RL
2A2A04	J01S-02/01	2A2A9-E0*E1		5- 11	RELOC ADDR BIT 15 TO INDICATOR	$S15RL
2A2A04	J01T-02/01	2A2A9-B1*B0		5- 11	RELOC ADDR BIT 16 TO INDICATOR	$S16RL
2A2A04	J01U-02/01	2A2A9-D0*D1		5- 11	RELOC ADDR BIT 17 TO INDICATOR	$S17RL
2A2A04	J01V-02/01	2A2B9-I1*I0		5- 23	ADDR LWR PAR. BIT TO INDICATOR	$SLPL
2A2A04	J02A-02/01	2A2B8-Q3*Q2		5- 13	BIT 00 OUT OF PF TO INDICATOR	$PFZ00L
2A2A04	J02B-02/01	2A2B8-P3*P2		5- 13	BIT 01 OUT OF PF TO INDICATOR	$PFZ01L
2A2A04	J02B-03*	2A2B9-C0		5- 23	LWR STOR PROTECT BIT 09 SW = 1	SP09S0
2A2A04	J02C-02/01	2A2B7-V3*V2		5- 15	BIT 02 OUT OF PF TO INDICATOR	$PFZ02L
2A2A04	J02D-02/01	2A2B7-S3*S2		5- 15	BIT 03 OUT OF PF TO INDICATOR	$PFZ03L
2A2A04	J02D-03*	2A2B9-D1		5- 23	LWR STOR PROTECT BIT 10 SW = 1	SP10S0
2A2A04	J02E-02/01	2A2B6-V3*V2		5- 17	BIT 04 OUT OF PF TO INDICATOR	$PFZ04L
2A2A04	J02F-02/01	2A2B6-S3*S2		5- 17	BIT 05 OUT OF PF TO INDICATOR	$PFZ05L
2A2A04	J02F-03*	2A2B9-C3		5- 23	LWR STOR PROTECT BIT 11 SW = 1	SP11S0
2A2A04	J02G-02/01	2A2B5-V3*V2		5- 19	BIT 06 OUT OF PF TO INDICATOR	$PFZ06L
2A2A04	J02H-02/01	2A2B5-S3*S2		5- 19	BIT 07 OUT OF PF TO INDICATOR	$PFZ07L
2A2A04	J02H-03*	2A2B9-I3		5- 23	LWR STOR PROTECT BIT 12 SW = 1	SP12S0
2A2A04	J02J-02/01	2A2B4-T2*T3		5- 21	BIT 08 OUT OF PF TO INDICATOR	$PFZ08L
2A2A04	J02K-02/01	2A2B4-Q1*Q0		5- 21	BIT 09 OUT OF PF TO INDICATOR	$PFZ09L
2A2A04	J02K-03*	2A2B9-N3		5- 23	LWR STOR PROTECT BIT 13 SW = 1	SP13S0
2A2A04	J02L-02/01	2A2B4-X0*X1		5- 21	BIT 10 OUT OF PF TO INDICATOR	$PFZ10L
2A2A04	J02L-03*	2B0B5-L3		6-107	NOT SINGLE CHANNEL	*SINGLE
2A2A04	J02M-02/01	2A2B4-V3*V2		5- 21	BIT 11 OUT OF PF TO INDICATOR	$PFZ11L
2A2A04	J02M-03*	2A2B9-T3		5- 23	LWR STOR PROTECT BIT 14 SW = 1	SP14S0
2A2A04	J02N-02/01	2A2B8-C0*C1		5- 13	STOR ADDR BIT 09 TO INDICATOR	$S09L
2A2A04	J02N-03*	2B1B8-I0		6- 11	CLOCK ON FROM MAINT. PANEL SW.	CLKON
2A2A04	J02P-02/01	2A2B8-B0*B1		5- 13	STOR ADDR BIT 10 TO INDICATOR	$S10L
2A2A04	J02P-03*	2B1A8-W0		6- 17	MAINT. MODE SW., MAINT. PANEL	MAINT
2A2A04	J02R-02/01	2A2B7-I1*I0		5- 15	STOR ADDR BIT 11 TO INDICATOR	$S11L
2A2A04	J02R-03*	P06F-07	2A1A06		MAINT. MODE SW., MAINT. PANEL	*MAINT
2A2A04	J02S-02/01	2A2B7-R3*R2		5- 15	STOR ADDR BIT 12 TO INDICATOR	$S12L
2A2A04	J02S-03*	2A2B9-V3		5- 23	SWITCH, TEST MODE	TSTMOD
2A2A04	J02T-02/01	2A2B6-I1*I0		5- 17	STOR ADDR BIT 13 TO INDICATOR	$S13L
2A2A04	J02U-02/01	2A2B6-R3*R2		5- 17	STOR ADDR BIT 14 TO INDICATOR	$S14L
2A2A04	J02V-02/01	2A2B5-I1*I0		5- 19	STOR ADDR BIT 15 TO INDICATOR	$S15L
2A2A04	J03A-02/01	2A2B5-R3*R2		5- 19	STOR ADDR BIT 16 TO INDICATOR	$S16L
2A2A04	J03A-03*	J17E-09	2A1A06			BPFSMG
2A2A04	J03B-02/01	2A2B4-Q3*Q2		5- 21	STOR ADDR BIT 17 TO INDICATOR	$S17L
2A2A04	J03B-03*	J17E-10	2A1A06			BPSLMG
2A2A04	J03C-02/01	P06E-04*03	2A1A06		MAINTENANCE LIGHTS BIT 00	$M1LT00
2A2A04	J03C-03*	P09E-05	2A1A06			FAST-A
2A2A04	J03D-02/01	P06E-06*05	2A1A06		MAINTENANCE LIGHTS BIT 01	$M1LT01
2A2A04	J03D-03*	P09E-06	2A1A06			SLOW-A
2A2A04	J03E-02/01	P06E-08*07	2A1A06		MAINTENANCE LIGHTS BIT 02	$M1LT02
2A2A04	J03E-03*	2A2A4-P3		5- 7	NOT PAGE FILE FAST MODE	*PFFM
2A2A04	J03F-02/01	P06E-10*09	2A1A06		MAINTENANCE LIGHTS BIT 03	$M1LT03
2A2A04	J03F-03*	2A2A4-N3		5- 7	NOT PAGE FILE SLOW MODE	*PFSM
2A2A04	J03G-02/01	P06F-02*01	2A1A06		MAINTENANCE LIGHTS BIT 04	$M1LT04
2A2A04	J03G-03*	2B1B7-W2		6- 3	NOT(BC FAST TIMING SELECTED)	FAST-B
2A2A04	J03H-02/01	P06F-04*03	2A1A06		MAINTENANCE LIGHTS BIT 05	$M1LT05
2A2A04	J03H-03*	2B1B7-V2		6- 3	NOT(BC SLOW TIMING SELECTED)	SLOW-B
2A2A04	J03J-02/01	P06F-06*05	2A1A06		MAINTENANCE LIGHTS BIT 06	$M1LT06
2A2A04	J03J-03*	P09E-04	2A1A06		FAST TIMING MARGIN	FAST
2A2A04	J03K-02/01	P06D-06*05	2A1A06		MAINTENANCE LIGHTS BIT 07	$M1LT07
2A2A04	J03K-03*	P09E-03	2A1A06		SLOW TIMING MARGIN	SLOW
2A2A04	J03L-02*	J16C-10	2A1A06		GRD FOR CONSOLE MAINT MODE SW	MMGND
2A2A04	J03L-03	J16C-09*	2A1A06		ENABLE FROM CONS MAINT MODE SW	MMENAB

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A1A06	P06D-02*01	2B2B2-01/00		5- 89	STOR CYCLE TO INDICATOR	$STOLT
2A1A06	P06D-04*03	2B2B2-D0/D1		5- 89	PROGRAM STATE	$PRO-LT
2A1A06	P06D-06*05	J03K-02/01	2A2A04		MAINTENANCE LIGHTS BIT 07	$M1LT07
2A1A06	P06D-08*07	2B1A9-03/02		6- 23	BIT 00 OF A	$ATOBC0
2A1A06	P06D-10*09	2B1A9-W3/W2		6- 23	BIT 01 OF A	$ATOBC1
2A1A06	P06E-02*01	2B1A9-V3/V2		6- 23	BIT 02 OF A	$ATOBC2
2A1A06	P06E-04*03	J03C-02/01	2A2A04		MAINTENANCE LIGHTS BIT 00	$M1LT00
2A1A06	P06E-06*05	J03D-02/01	2A2A04		MAINTENANCE LIGHTS BIT 01	$M1LT01
2A1A06	P06E-08*07	J03E-02/01	2A2A04		MAINTENANCE LIGHTS BIT 02	$M1LT02
2A1A06	P06E-10*09	J03F-02/01	2A2A04		MAINTENANCE LIGHTS BIT 03	$M1LT03
2A1A06	P06F-02*01	J03G-02/01	2A2A04		MAINTENANCE LIGHTS BIT 04	$M1LT04
2A1A06	P06F-04*03	J03H-02/01	2A2A04		MAINTENANCE LIGHTS BIT 05	$M1LT05
2A1A06	P06F-06*05	J03J-02/01	2A2A04		MAINTENANCE LIGHTS BIT 06	$M1LT06
2A1A06	P06F-07	J02R-03*	2A2A04		MAINT.MODE SW., MAINT PANEL	*MAINT
2A1A06	P06F-08	J03N-03*	2A2A04		NOT (SEL. BITS 00-07 OF MAINT)	MOLT-1
2A1A06	P07D-02*01	2B2B5-H0/H1		5- 83	B8 BIT 3	$B8LT03
2A1A06	P07D-04*03	2B2B5-01/00		5- 83	B8 BIT 4	$B8LT04
2A1A06	P07D-06*05	2B2B5-N0/N1		5- 83	B8 BIT 5	$B8LT05
2A1A06	P07D-08*07	2B2B5-M0/M1		5- 83	B8 BIT 6	$B8LT06
2A1A06	P07D-10*09	2B2B5-T0/T1		5- 83	B8 BIT 7	$B8LT07
2A1A06	P07E-02*01	2B2B5-S0/S1		5- 83	B8 BIT 8	$B8LT08
2A1A06	P07E-04*03	2B2B5-R0/R1		5- 83	B8 BIT 9	$B8LT09
2A1A06	P07E-06*05	2B2B5-X0/X1		5- 83	B8 BIT 10	$B8LT10
2A1A06	P07E-08*07	2B2B5-W0/W1		5- 83	B8 BIT 11	$B8LT11
2A1A06	P07E-10*09	2B2B5-C2/C3		5- 83	B8 BIT 12	$B8LT12
2A1A06	P07F-02*01	2B2B5-D2/D3		5- 83	B8 BIT 13	$B8LT13
2A1A06	P07F-04*03	2B2B5-E3/E2		5- 83	B8 BIT 14	$B8LT14
2A1A06	P08A-02*01	2B2B5-H2/H3		5- 83	C2 BIT 0	$CFLT00
2A1A06	P08A-04*03	2B2B5-I2/I3		5- 83	C2 BIT 1	$CFLT01
2A1A06	P08A-06*05	2B2B5-J3/J2		5- 83	C2 BIT 2	$CFLT02
2A1A06	P08A-08*07	2B2B5-N2/N3		5- 83	C2 BIT 3	$CFLT03
2A1A06	P08A-10*09	2B2B5-03/02		5- 83	C2 BIT 4	$CFLT04
2A1A06	P08B-02*01	2B2B5-R2/R3		5- 83	C2 BIT 5	$CFLT05
2A1A06	P08B-04*03	2B2B5-T2/T3		5- 83	C2 BIT 6	$CFLT06
2A1A06	P08B-06*05	2B2B5-W2/W3		5- 83	C2 BIT 7	$CFLT07
2A1A06	P08B-08*07	2B2B5-X2/X3		5- 83	C2 BIT 8	$CFLT08
2A1A06	P08B-10*09	2B2B4-D0/D1		5- 85	C2 BIT 9	$CFLT09
2A1A06	P08C-02*01	2B2B4-C0/C1		5- 85	C2 BIT 10	$CFLT10
2A1A06	P08C-04*03	2B2B4-J1/J0		5- 85	C2 BIT 11	$CFLT11
2A1A06	P08C-06*05	2B2B4-H0/H1		5- 85	C2 BIT 12	$CFLT12
2A1A06	P08C-08*07	2B2B4-01/00		5- 85	C2 BIT 13	$CFLT13
2A1A06	P08C-10*09	2B2B4-N0/N1		5- 85	C2 BIT 14	$CFLT14
2A1A06	P08D-02/01	2B2B9-Q0*Q1		5- 75	INTERRUPT CODE BIT 0	$ICODE0
2A1A06	P08D-04/03	2B2B9-I1*I0		5- 75	INTERRUPT CODE BIT 1	$ICODE1
2A1A06	P08D-06/05	2B2B9-N1*N0		5- 75	INTERRUPT CODE BIT 2	$ICODE2
2A1A06	P08D-08/07	2B2B8-N1*N0		5- 77	INTERRUPT CODE BIT 3	$ICODE3
2A1A06	P08D-10/09	2B2B9-L0*L1		5- 75	INTERRUPT CODE BIT 4	$ICODE4
2A1A06	P08E-02/01	2B2B8-Q0*Q1		5- 77	INTERRUPT CODE BIT 5	$ICODE5
2A1A06	P09A-08*07	2B2B2-J1/J0		5- 89	RNI CYCLE LIGHT	$RNILT
2A1A06	P09A-10*09	2B2B2-I0/I1		5- 89	NOT (RAD CYCLE FF)	$RADLT
2A1A06	P09B-02*01	2B2B2-H0/H1		5- 89	NOT(ROP1 OR ROP2 CYCLE)	$ROPLT
2A1A06	P09B-04*03	2B2B4-T0/T1		5- 85	C2 BIT 15	$CFLT15
2A1A06	P09B-06*05	2B2B4-S0/S1		5- 85	C2 BIT 16	$CFLT16
2A1A06	P09B-08*07	2B2B4-R0/R1		5- 85	C2 BIT 17	$CFLT17
2A1A06	P09B-10*09	2B2B4-W0/W1		5- 85	C2 BIT 18	$CFLT18
2A1A06	P09C-02*01	2B2B4-C2/C3		5- 85	C2 BIT 19	$CFLT19
2A1A06	P09C-04*03	2B2B4-D2/D3		5- 85	C2 BIT 20	$CFLT20
2A1A06	P09C-06*05	2B2B4-H2/H3		5- 85	C2 BIT 21	$CFLT21
2A1A06	P09C-08*07	2B2B4-I2/I3		5- 85	C2 BIT 22	$CFLT22
2A1A06	P09C-10*09	2B2B4-J3/J2		5- 85	C2 BIT 23	$CFLT23
2A1A06	P09D-10*09	2B2B2-F1/E0		5- 89	MONITOR STATE	$MON-LT
2A1A06	P09E-03	J03K-03*	2A2A04		SLOW TIMING MARGIN	SLOW
2A1A06	P09E-04	J03J-03*	2A2A04		FAST TIMING MARGIN	FAST
2A1A06	P09E-05	J03C-03*	2A2A04		FAST TIMING MARGIN - ARITH	FAST-A
2A1A06	P09E-06	J03D-03*	2A2A04		SLOW TIMING MARGIN - ARITH	SLOW-A
2A1A06	P09E-09	2A2B9-W2		5- 23	SWITCH, TEST MODE	TSTMOD
2A1A06	P09F-02*01	2B2B6-D0/D1		5- 81	GATE C + F DIGITS 0-3	$CFGT03
2A1A06	P09F-04*03	2B2B6-C0/C1		5- 81	GATE C + F DIGIT 4	$CFGT4
2A1A06	P09F-06*05	2B2B6-J1/J0		5- 81	GATE C + F DIGITS 5-7	$CFGT57
2A2A04	J01A-02/01	2A2A8-H3*H2		5- 9	STOR ADDR BIT 00 TO INDICATOR	$S00L
2A2A04	J01B-02/01	2A2A8-E2*E3		5- 9	STOR ADDR BIT 01 TO INDICATOR	$S01L
2A2A04	J01B-03*	2A2B9-D0		5- 23	UP. STOR PROTECT BIT 09 SW = 1	SP09S1

425

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A2A04	J03M-03*	J17F-01	2A1A06		CC-MR SWITCH IN CC POSITION	BT13OR
2A2A04	J03N-03*	P06F-08	2A1A06		NOT (SEL. BITS 00-07 OF MAINT)	M0LT-1
2A2A04	J03P-03*	P06B-07	2A1A06		NOT (SEL. BITS 08-15 OF MAINT)	M0LT-2
2A2A04	J03R-03*	P06B-08	2A1A06		NOT (SEL. BITS 16-23 OF MAINT)	M0LT-3
2A4A01	J01A-02/01	2A0B9-E0*E1		6-143	CHANNEL 0 EXTERNAL DATA BIT 12	$C0EX12
2A4A01	J01A-04/03	2A0B9-I0*I1		6-143	CHANNEL 0 EXTERNAL DATA BIT 13	$C0EX13
2A4A01	J01A-06/05	2A0B9-M1*M0		6-143	CHANNEL 0 EXTERNAL DATA BIT 14	$C0EX14
2A4A01	J01A-08/07	2A0B9-N0*N1		6-143	CHANNEL 0 EXTERNAL DATA BIT 15	$C0EX15
2A4A01	J01A-10/09	2A0B9-S0*S1		6-143	CHANNEL 0 EXTERNAL DATA BIT 16	$C0EX16
2A4A01	J01B-02/01	2A0B9-W0*W1		6-143	CHANNEL 0 EXTERNAL DATA BIT 17	$C0EX17
2A4A01	J01B-04/03	2A0B9-B2*B3		6-143	CHANNEL 0 EXTERNAL DATA BIT 18	$C0EX18
2A4A01	J01B-06/05	2A0B9-G2*G3		6-143	CHANNEL 0 EXTERNAL DATA BIT 19	$C0EX19
2A4A01	J01B-08/07	2A0B9-M2*M3		6-143	CHANNEL 0 EXTERNAL DATA BIT 20	$C0EX20
2A4A01	J01B-10/09	2A0B9-K3*K2		6-143	CHANNEL 0 EXTERNAL DATA BIT 21	$C0EX21
2A4A01	J01C-02/01	2A0B9-Q3*Q2		6-143	CHANNEL 0 EXTERNAL DATA BIT 22	$C0EX22
2A4A01	J01C-04/03	2A0B9-W2*W3		6-143	CHANNEL 0 EXTERNAL DATA BIT 23	$C0EX23
2A4A01	J01C-06/05	2A0B9-U3*U2		6-143	CHL 0 EXTERNAL PARITY BIT 2	$C0EXP2
2A4A01	J01C-08*07	2A0A7-X0/X1		6-133	CHAN 0 EXT 24-BIT DEVICE CONN	$C0EX24
2A4A01	J01C-10/09	J02C-10*09	2A4A01		NOT USED	$C0EJ00
2A4A01	J01D-02/01	J02D-02*01	2A4A01		NOT USED	$C0EJ01
2A4A01	J01D-04/03	J02D-04*03	2A4A01		NOT USED	$C0EJ02
2A4A01	J01D-06/05	J02D-06*05	2A4A01		NOT USED	$C0EJ03
2A4A01	J01D-08/07	J02D-08*07	2A4A01		NOT USED	$C0EJ04
2A4A01	J01D-10/09	J02D-10*09	2A4A01		NOT USED	$C0EJ05
2A4A01	J01E-02/01	J02E-02*01	2A4A01		NOT USED	$C0EJ06
2A4A01	J01E-04/03	J02E-04*03	2A4A01		NOT USED	$C0EJ07
2A4A01	J01E-06/05	J02E-06*05	2A4A01		NOT USED	$C0EJ08
2A4A01	J01E-08/07	J02E-08*07	2A4A01		NOT USED	$C0EJ09
2A4A01	J01E-10/09	J02E-10*09	2A4A01		NOT USED	$C0EJ10
2A4A01	J01F-02/01	J02F-02*01	2A4A01		NOT USED	$C0EJ11
2A4A01	J01F-04/03	J02F-04*03	2A4A01		NOT USED	$C0EJ12
2A4A01	J01F-06/05	J02F-06*05	2A4A01		NOT USED	$C0EJ13
2A4A01	J01F-08/07	J02F-08*07	2A4A01		NOT USED	$C0EJ14
2A4A01	J02A-02/01	2A0B9-F0*F1		6-143	CHANNEL 0 EXTERNAL DATA BIT 12	$C0EX12
2A4A01	J02A-04/03	2A0B9-J0*J1		6-143	CHANNEL 0 EXTERNAL DATA BIT 13	$C0EX13
2A4A01	J02A-06/05	2A0B9-L1*L0		6-143	CHANNEL 0 EXTERNAL DATA BIT 14	$C0EX14
2A4A01	J02A-08/07	2A0B9-Q0*Q1		6-143	CHANNEL 0 EXTERNAL DATA BIT 15	$C0EX15
2A4A01	J02A-10/09	2A0B9-T0*T1		6-143	CHANNEL 0 EXTERNAL DATA BIT 16	$C0EX16
2A4A01	J02B-02/01	2A0B9-X0*X1		6-143	CHANNEL 0 EXTERNAL DATA BIT 17	$C0EX17
2A4A01	J02B-04/03	2A0B9-C2*C3		6-143	CHANNEL 0 EXTERNAL DATA BIT 18	$C0EX18
2A4A01	J02B-06/05	2A0B9-H2*H3		6-143	CHANNEL 0 EXTERNAL DATA BIT 19	$C0EX19
2A4A01	J02B-08/07	2A0B9-N2*N3		6-143	CHANNEL 0 EXTERNAL DATA BIT 20	$C0EX20
2A4A01	J02B-10/09	2A0B9-L3*L2		6-143	CHANNEL 0 EXTERNAL DATA BIT 21	$C0EX21
2A4A01	J02C-02/01	2A0B9-R3*R2		6-143	CHANNEL 0 EXTERNAL DATA BIT 22	$C0EX22
2A4A01	J02C-04/03	2A0B9-X2*X3		6-143	CHANNEL 0 EXTERNAL DATA BIT 23	$C0EX23

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A01	J02C-06/05	2A0B9-V3*V2		6-143	CHL 0 EXTERNAL PARITY BIT 2	$C0EXP2
2A4A01	J02C-08*07	2A0A7-X0/X1		6-133	CHAN 0 EXT 24-BIT DEVICE CONN	$C0EX24
2A4A01	J02C-10*09	J01C-10/09	2A4A01		NOT USED	C0EJ00
2A4A01	J02D-02*01	J01D-02/01	2A4A01		NOT USED	C0EJ01
2A4A01	J02D-04*03	J01D-04/03	2A4A01		NOT USED	C0EJ02
2A4A01	J02D-06*05	J01D-06/05	2A4A01		NOT USED	C0EJ03
2A4A01	J02D-08*07	J01D-08/07	2A4A01		NOT USED	C0EJ04
2A4A01	J02D-10*09	J01D-10/09	2A4A01		NOT USED	C0EJ05
2A4A01	J02E-02*01	J01E-02/01	2A4A01		NOT USED	C0EJ06
2A4A01	J02E-04*03	J01E-04/03	2A4A01		NOT USED	C0EJ07
2A4A01	J02E-06*05	J01E-06/05	2A4A01		NOT USED	C0EJ08
2A4A01	J02E-08*07	J01E-08/07	2A4A01		NOT USED	C0EJ09
2A4A01	J02E-10*09	J01E-10/09	2A4A01		NOT USED	C0EJ10
2A4A01	J02F-02*01	J01F-02/01	2A4A01		NOT USED	C0EJ11
2A4A01	J02F-04*03	J01F-04/03	2A4A01		NOT USED	C0EJ12
2A4A01	J02F-06*05	J01F-06/05	2A4A01		NOT USED	C0EJ13
2A4A01	J02F-08*07	J01F-08/07	2A4A01		NOT USED	$C0EJ14
2A4A01	J03A-02/01	2A0A9-E0*E1		6-141	CHANNEL 0 EXTERNAL DATA BIT 00	$C0EX00
2A4A01	J03A-04/03	2A0A9-I0*I1		6-141	CHANNEL 0 EXTERNAL DATA BIT 01	$C0EX01
2A4A01	J03A-06/05	2A0A9-M1*M0		6-141	CHANNEL 0 EXTERNAL DATA BIT 02	$C0EX02
2A4A01	J03A-08/07	2A0A9-N0*N1		6-141	CHANNEL 0 EXTERNAL DATA BIT 03	$C0EX03
2A4A01	J03A-10/09	2A0A9-S0*S1		6-141	CHANNEL 0 EXTERNAL DATA BIT 04	$C0EX04
2A4A01	J03B-02/01	2A0A9-W0*W1		6-141	CHANNEL 0 EXTERNAL DATA BIT 05	$C0EX05
2A4A01	J03B-04/03	2A0A9-B2*B3		6-141	CHANNEL 0 EXTERNAL DATA BIT 06	$C0EX06
2A4A01	J03B-06/05	2A0A9-G2*G3		6-141	CHANNEL 0 EXTERNAL DATA BIT 07	$C0EX07
2A4A01	J03B-08/07	2A0A9-M2*M3		6-141	CHANNEL 0 EXTERNAL DATA BIT 08	$C0EX08
2A4A01	J03B-10/09	2A0A9-K3*K2		6-141	CHANNEL 0 EXTERNAL DATA BIT 09	$C0EX09
2A4A01	J03C-02/01	2A0A9-Q3*Q2		6-141	CHANNEL 0 EXTERNAL DATA BIT 10	$C0EX10
2A4A01	J03C-04/03	2A0A9-W2*W3		6-141	CHANNEL 0 EXTERNAL DATA BIT 11	$C0EX11
2A4A01	J03C-06/05	2A0A9-U3*U2		6-141	CHL 0 EXTERNAL PARITY BIT 1	$C0EXP1
2A4A01	J03C-08/07	2A0B7-R2*R3		6-125	CHL 0 EXTERNAL BUSY SIGNAL	$C0EXRW
2A4A01	J03C-10/09	J04C-10*09	2A4A01		NOT USED	$C0EXRA
2A4A01	J03D-02/01	2A0B7-X0*X1		6-125	CHL 0 EXTERNAL READ SIGNAL	$C0EXRD
2A4A01	J03D-04/03	2A0B7-T1*T0		6-125	CHL 0 EXTERNAL WRITE SIGNAL	$C0EXWR
2A4A01	J03D-06/05	2A0B7-I3*I2		6-125	CHL 0 EXTERNAL CONNECT SIGNAL	$C0EXCN
2A4A01	J03D-08/07	2A0B7-F2*F3		6-125	CHL 0 EXTERNAL SELECT SIGNAL	$C0EXSI
2A4A01	J03D-10/09	2A0A7-C3*C2		6-133	CHL 0 EXTERNAL DATA SIGNAL	$C0EXDS
2A4A01	J03E-02*01	2A0A7-J2/J3		6-133	CHL 0 EXTERNAL REPLY SIGNAL	$C0EXRP
2A4A01	J03E-04*03	2A0B7-E3/E2		6-125	CHL 0 EXTERNAL REJECT SIGNAL	$C0EXRJ
2A4A01	J03E-06*05	2A0A7-I3/I2		6-133	CHL 0 EXTERNAL REJECT SIGNAL	$C0EXER
2A4A01	J03E-08*07	2A0B7-N2/N3		6-125	CHL 0 EXTERNAL PARITY ERROR	$C0EXPE
2A4A01	J03E-10/09	J04E-10*09	2A4A01		NOT USED	$C0EJA0
2A4A01	J03F-02/01	2A0A7-W0*W1		6-133	CHL 0 EXTERNAL WORD MARK	$C0EXWM
2A4A01	J03F-04/03	2A0B7-01*00		6-125	CHL 0 CLEAR TO EXTERNAL EQUIP	$C0EXCL
2A4A01	J03F-06/05	J04F-06*05	2A4A01		NOT USED	$C0EJA1
2A4A01	J03F-08/07	J04F-08*07	2A4A01		NOT USED	$C0EJA2

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A01	J04A-02/01	2A0A9-F0*F1		6-141	CHANNEL 0 EXTERNAL DATA BIT 00	$C0EX00
2A4A01	J04A-04/03	2A0A9-J0*J1		6-141	CHANNEL 0 EXTERNAL DATA BIT 01	$C0EX01
2A4A01	J04A-06/05	2A0A9-L1*L0		6-141	CHANNEL 0 EXTERNAL DATA BIT 02	$C0EX02
2A4A01	J04A-08/07	2A0A9-O0*O1		6-141	CHANNEL 0 EXTERNAL DATA BIT 03	$C0EX03
2A4A01	J04A-10/09	2A0A9-T0*T1		6-141	CHANNEL 0 EXTERNAL DATA BIT 04	$C0EX04
2A4A01	J04B-02/01	2A0A9-X0*X1		6-141	CHANNEL 0 EXTERNAL DATA BIT 05	$C0EX05
2A4A01	J04B-04/03	2A0A9-C2*C3		6-141	CHANNEL 0 EXTERNAL DATA BIT 06	$C0EX06
2A4A01	J04B-06/05	2A0A9-H2*H3		6-141	CHANNEL 0 EXTERNAL DATA BIT 07	$C0EX07
2A4A01	J04B-08/07	2A0A9-N2*N3		6-141	CHANNEL 0 EXTERNAL DATA BIT 08	$C0EX08
2A4A01	J04B-10/09	2A0A9-L3*L2		6-141	CHANNEL 0 EXTERNAL DATA BIT 09	$C0EX09
2A4A01	J04C-02/01	2A0A9-R3*R2		6-141	CHANNEL 0 EXTERNAL DATA BIT 10	$C0EX10
2A4A01	J04C-04/03	2A0A9-X2*X3		6-141	CHANNEL 0 EXTERNAL DATA BIT 11	$C0EX11
2A4A01	J04C-06/05	2A0A9-V3*V2		6-141	CHL 0 EXTERNAL PARITY BIT 1	$C0EXP1
2A4A01	J04C-08/07	2A0B7-R2*R3		6-125	CHL 0 EXTERNAL BUSY SIGNAL	$C0EXRW
2A4A01	J04C-10*09	J03C-10/09	2A4A01		NOT USED	$C0EXRA
2A4A01	J04D-02/01	2A0B7-X0*X1		6-125	CHL 0 EXTERNAL READ SIGNAL	$C0EXRD
2A4A01	J04D-04/03	2A0B7-T1*T0		6-125	CHL 0 EXTERNAL WRITE SIGNAL	$C0EXWR
2A4A01	J04D-06/05	2A0B7-I3*I2		6-125	CHL 0 EXTERNAL CONNECT SIGNAL	$C0EXCN
2A4A01	J04D-08/07	2A0B7-F2*F3		6-125	CHL 0 EXTERNAL SELECT SIGNAL	$C0EXSL
2A4A01	J04D-10/09	2A0A7-C3*C2		6-133	CHL 0 EXTERNAL DATA SIGNAL	$C0EXDS
2A4A01	J04E-02*01	2A0A7-J2/J3		6-133	CHL 0 EXTERNAL REPLY SIGNAL	$C0EXRP
2A4A01	J04E-04*03	2A0B7-E3/E2		6-125	CHL 0 EXTERNAL REJECT SIGNAL	$C0EXRJ
2A4A01	J04E-06*05	2A0A7-I3/I2		6-133	CHL 0 EXTERNAL REJECT SIGNAL	$C0EXER
2A4A01	J04E-08*07	2A0B7-N2/N3		6-125	CHL 0 EXTERNAL PARITY ERROR	$C0EXPE
2A4A01	J04E-10*09	J03E-10/09	2A4A01		NOT USED	$C0EJA0
2A4A01	J04F-02/01	2A0A7-W0*W1		6-133	CHL 0 EXTERNAL WORD MARK	$C0EXWM
2A4A01	J04F-04/03	2A0B7-O1*O0		6-125	CHL 0 CLEAR TO EXTERNAL EQUIP	$C0EXCL
2A4A01	J04F-06*05	J03F-06/05	2A4A01		NOT USED	$C0EJA1
2A4A01	J04F-08*07	J03F-08/07	2A4A01		NOT USED	$C0EJA2
2A4A02	J01A-02/01	2A0B8-E0*E1		6-147	CHANNEL 1 EXTERNAL DATA BIT 12	$C1EX12
2A4A02	J01A-04/03	2A0B8-I0*I1		6-147	CHANNEL 1 EXTERNAL DATA BIT 13	$C1EX13
2A4A02	J01A-06/05	2A0B8-M1*M0		6-147	CHANNEL 1 EXTERNAL DATA BIT 14	$C1EX14
2A4A02	J01A-08/07	2A0B8-N0*N1		6-147	CHANNEL 1 EXTERNAL DATA BIT 15	$C1EX15
2A4A02	J01A-10/09	2A0B8-S0*S1		6-147	CHANNEL 1 EXTERNAL DATA BIT 16	$C1EX16
2A4A02	J01B-02/01	2A0B8-W0*W1		6-147	CHANNEL 1 EXTERNAL DATA BIT 17	$C1EX17
2A4A02	J01B-04/03	2A0B8-B2*B3		6-147	CHANNEL 1 EXTERNAL DATA BIT 18	$C1EX18
2A4A02	J01B-06/05	2A0B8-G2*G3		6-147	CHANNEL 1 EXTERNAL DATA BIT 19	$C1EX19
2A4A02	J01B-08/07	2A0B8-M2*M3		6-147	CHANNEL 1 EXTERNAL DATA BIT 20	$C1EX20
2A4A02	J01B-10/09	2A0B8-K3*K2		6-147	CHANNEL 1 EXTERNAL DATA BIT 21	$C1EX21
2A4A02	J01C-02/01	2A0B8-Q3*Q2		6-147	CHANNEL 1 EXTERNAL DATA BIT 22	$C1EX22
2A4A02	J01C-04/03	2A0B8-W2*W3		6-147	CHANNEL 1 EXTERNAL DATA BIT 23	$C1EX23
2A4A02	J01C-06/05	2A0B8-U3*U2		6-147	CHAN 1 EXT PARITY BIT 2	$C1EXP2
2A4A02	J01C-08*07	2A0A6-X0/X1		6-135	CHL 1 EXT 24 BIT DEVICE CONNTD	$C1EX24
2A4A02	J01C-10/09	J02C-10*09	2A4A02		NOT USED	$C1EJ00
2A4A02	J01D-02/01	J02D-02*01	2A4A02		NOT USED	$C1EJ01
2A4A02	J01D-04/03	J02D-04*03	2A4A02		NOT USED	$C1EJ02
2A4A02	J01D-06/05	J02D-06*05	2A4A02		NOT USED	$C1EJ03
2A4A02	J01D-08/07	J02D-08*07	2A4A02		NOT USED	$C1EJ04
2A4A02	J01D-10/09	J02D-10*09	2A4A02		NOT USED	$C1EJ05
2A4A02	J01E-02/01	J02E-02*01	2A4A02		NOT USED	$C1EJ06
2A4A02	J01E-04/03	J02E-04*03	2A4A02		NOT USED	$C1EJ07
2A4A02	J01E-06/05	J02E-06*05	2A4A02		NOT USED	$C1EJ08
2A4A02	J01E-08/07	J02E-08*07	2A4A02		NOT USED	$C1EJ09
2A4A02	J01E-10/09	J02E-10*09	2A4A02		NOT USED	$C1EJ10
2A4A02	J01F-02/01	J02F-02*01	2A4A02		NOT USED	$C1EJ11
2A4A02	J01F-04/03	J02F-04*03	2A4A02		NOT USED	$C1EJ12
2A4A02	J01F-06/05	J02F-06*05	2A4A02		NOT USED	$C1EJ13
2A4A02	J01F-08/07	J02F-08*07	2A4A02		NOT USED	$C1EJ14
2A4A02	J02A-02/01	2A0B8-F0*F1		6-147	CHANNEL 1 EXTERNAL DATA BIT 12	$C1EX12
2A4A02	J02A-04/03	2A0B8-J0*J1		6-147	CHANNEL 1 EXTERNAL DATA BIT 13	$C1EX13
2A4A02	J02A-06/05	2A0B8-L1*L0		6-147	CHANNEL 1 EXTERNAL DATA BIT 14	$C1EX14
2A4A02	J02A-08/07	2A0B8-O0*O1		6-147	CHANNEL 1 EXTERNAL DATA BIT 15	$C1EX15
2A4A02	J02A-10/09	2A0B8-T0*T1		6-147	CHANNEL 1 EXTERNAL DATA BIT 16	$C1EX16
2A4A02	J02B-02/01	2A0B8-X0*X1		6-147	CHANNEL 1 EXTERNAL DATA BIT 17	$C1EX17
2A4A02	J02B-04/03	2A0B8-C2*C3		6-147	CHANNEL 1 EXTERNAL DATA BIT 18	$C1EX18
2A4A02	J02B-06/05	2A0B8-H2*H3		6-147	CHANNEL 1 EXTERNAL DATA BIT 19	$C1EX19
2A4A02	J02B-08/07	2A0B8-N2*N3		6-147	CHANNEL 1 EXTERNAL DATA BIT 20	$C1EX20
2A4A02	J02B-10/09	2A0B8-L3*L2		6-147	CHANNEL 1 EXTERNAL DATA BIT 21	$C1EX21
2A4A02	J02C-02/01	2A0B8-R3*R2		6-147	CHANNEL 1 EXTERNAL DATA BIT 22	$C1EX22
2A4A02	J02C-04/03	2A0B8-X2*X3		6-147	CHANNEL 1 EXTERNAL DATA BIT 23	$C1EX23
2A4A02	J02C-06/05	2A0B8-V3*V2		6-147	CHAN 1 EXT PARITY BIT 2	$C1EXP2
2A4A02	J02C-08*07	2A0A6-X0/X1		6-135	CHL 1 EXT 24 BIT DEVICE CONNTD	$C1EX24
2A4A02	J02C-10*09	J01C-10/09	2A4A02		NOT USED	$C1EJ00

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A02	J02D-02*01	J01D-02/01	2A4A02		NOT USED	$C1EJ01
2A4A02	J02D-04*03	J01D-04/03	2A4A02		NOT USED	$C1EJ02
2A4A02	J02D-06*05	J01D-06/05	2A4A02		NOT USED	$C1EJ03
2A4A02	J02D-08*07	J01D-08/07	2A4A02		NOT USED	$C1EJ04
2A4A02	J02D-10*09	J01D-10/09	2A4A02		NOT USED	$C1EJ05
2A4A02	J02E-02*01	J01E-02/01	2A4A02		NOT USED	$C1EJ06
2A4A02	J02E-04*03	J01E-04/03	2A4A02		NOT USED	$C1EJ07
2A4A02	J02E-06*05	J01E-06/05	2A4A02		NOT USED	$C1EJ08
2A4A02	J02E-08*07	J01E-08/07	2A4A02		NOT USED	$C1EJ09
2A4A02	J02E-10*09	J01E-10/09	2A4A02		NOT USED	$C1EJ10
2A4A02	J02F-02*01	J01F-02/01	2A4A02		NOT USED	$C1EJ11
2A4A02	J02F-04*03	J01F-04/03	2A4A02		NOT USED	$C1EJ12
2A4A02	J02F-06*05	J01F-06/05	2A4A02		NOT USED	$C1EJ13
2A4A02	J02F-08*07	J01F-08/07	2A4A02		NOT USED	$C1EJ14
2A4A02	J03A-02/01	2A0A8-E0*E1		6-145	CHANNEL 1 EXTERNAL DATA BIT 00	$C1EX00
2A4A02	J03A-04/03	2A0A8-I0*I1		6-145	CHANNEL 1 EXTERNAL DATA BIT 01	$C1EX01
2A4A02	J03A-06/05	2A0A8-M1*M0		6-145	CHANNEL 1 EXTERNAL DATA BIT 02	$C1EX02
2A4A02	J03A-08/07	2A0A8-N0*N1		6-145	CHANNEL 1 EXTERNAL DATA BIT 03	$C1EX03
2A4A02	J03A-10/09	2A0A8-S0*S1		6-145	CHANNEL 1 EXTERNAL DATA BIT 04	$C1EX04
2A4A02	J03B-02/01	2A0A8-W0*W1		6-145	CHANNEL 1 EXTERNAL DATA BIT 05	$C1EX05
2A4A02	J03B-04/03	2A0A8-B2*B3		6-145	CHANNEL 1 EXTERNAL DATA BIT 06	$C1EX06
2A4A02	J03B-06/05	2A0A8-G2*G3		6-145	CHANNEL 1 EXTERNAL DATA BIT 07	$C1EX07
2A4A02	J03B-08/07	2A0A8-M2*M3		6-145	CHANNEL 1 EXTERNAL DATA BIT 08	$C1EX08
2A4A02	J03B-10/09	2A0A8-K3*K2		6-145	CHANNEL 1 EXTERNAL DATA BIT 09	$C1EX09
2A4A02	J03C-02/01	2A0A8-Q3*Q2		6-145	CHANNEL 1 EXTERNAL DATA BIT 10	$C1EX10
2A4A02	J03C-04/03	2A0A8-W2*W3		6-145	CHANNEL 1 EXTERNAL DATA BIT 11	$C1EX11
2A4A02	J03C-06/05	2A0A8-U3*U2		6-145	CHL 1 EXTERNAL PARITY BIT 1	$C1EXP1
2A4A02	J03C-08/07	2A0B6-R2*R3		6-127	CHL 1 EXTERNAL BUSY SIGNAL	$C1EXRW
2A4A02	J03C-10/09	J04C-10*09	2A4A02		NOT USED	$C1EXRA
2A4A02	J03D-02/01	2A0B6-X0*X1		6-127	CHL 1 EXTERNAL READ SIGNAL	$C1EXRD
2A4A02	J03D-04/03	2A0B6-T1*T0		6-127	CHL 1 EXTERNAL WRITE SIGNAL	$C1EXWR
2A4A02	J03D-06/05	2A0B6-I3*I2		6-127	CHL 1 EXTERNAL CONNECT SIGNAL	$C1EXCN
2A4A02	J03D-08/07	2A0B6-F2*F3		6-127	CHL 1 EXTERNAL SELECT SIGNAL	$C1EXSL
2A4A02	J03D-10/09	2A0A6-C3*C2		6-135	CHL 1 EXTERNAL DATA SIGNAL	$C1EXDS
2A4A02	J03E-02*01	2A0A6-J2/J3		6-135	CHL 1 EXTERNAL REPLY SIGNAL	$C1EXRP
2A4A02	J03E-04*03	2A0B6-E3/E2		6-127	CHL 1 EXTERNAL REJECT SIGNAL	$C1EXRJ
2A4A02	J03E-06*05	2A0A6-I3/I2		6-135	CHL 1 EXTERNAL REJECT SIGNAL	$C1EXER
2A4A02	J03E-08*07	2A0B6-N2/N3		6-127	CHL 1 EXTERNAL PARITY ERROR	$C1EXPE
2A4A02	J03E-10/09	J04E-10*09	2A4A02		NOT USED	$C1EJA0
2A4A02	J03F-02/01	2A0A6-W0*W1		6-135	CHL 1 EXTERNAL WORD MARK	$C1EXWM
2A4A02	J03F-04/03	2A0B6-O1*O0		6-127	CHL 1 CLEAR TO EXTERNAL EQUIP	$C1EXCL
2A4A02	J03F-06/05	J04F-06*05	2A4A02		NOT USED	$C1EJA1
2A4A02	J03F-08/07	J04F-08*07	2A4A02		NOT USED	$C1EJA2
2A4A02	J04A-02/01	2A0A8-F0*F1		6-145	CHANNEL 1 EXTERNAL DATA BIT 00	$C1EX00
2A4A02	J04A-04/03	2A0A8-J0*J1		6-145	CHANNEL 1 EXTERNAL DATA BIT 01	$C1EX01
2A4A02	J04A-06/05	2A0A8-L1*L0		6-145	CHANNEL 1 EXTERNAL DATA BIT 02	$C1EX02
2A4A02	J04A-08/07	2A0A8-O0*O1		6-145	CHANNEL 1 EXTERNAL DATA BIT 03	$C1EX03
2A4A02	J04A-10/09	2A0A8-T0*T1		6-145	CHANNEL 1 EXTERNAL DATA BIT 04	$C1EX04
2A4A02	J04B-02/01	2A0A8-X0*X1		6-145	CHANNEL 1 EXTERNAL DATA BIT 05	$C1EX05
2A4A02	J04B-04/03	2A0A8-C2*C3		6-145	CHANNEL 1 EXTERNAL DATA BIT 06	$C1EX06
2A4A02	J04B-06/05	2A0A8-H2*H3		6-145	CHANNEL 1 EXTERNAL DATA BIT 07	$C1EX07
2A4A02	J04B-08/07	2A0A8-N2*N3		6-145	CHANNEL 1 EXTERNAL DATA BIT 08	$C1EX08
2A4A02	J04B-10/09	2A0A8-L3*L2		6-145	CHANNEL 1 EXTERNAL DATA BIT 09	$C1EX09
2A4A02	J04C-02/01	2A0A8-R3*R2		6-145	CHANNEL 1 EXTERNAL DATA BIT 10	$C1EX10
2A4A02	J04C-04/03	2A0A8-X2*X3		6-145	CHANNEL 1 EXTERNAL DATA BIT 11	$C1EX11
2A4A02	J04C-06/05	2A0A8-V3*V2		6-145	CHL 1 EXTERNAL PARITY BIT 1	$C1EXP1
2A4A02	J04C-08/07	2A0B6-R2*R3		6-127	CHL 1 EXTERNAL BUSY SIGNAL	$C1EXRW
2A4A02	J04C-10*09	J03C-10/09	2A4A02		NOT USED	$C1EXRA
2A4A02	J04D-02/01	2A0B6-X0*X1		6-127	CHL 1 EXTERNAL READ SIGNAL	$C1EXRD
2A4A02	J04D-04/03	2A0B6-T1*T0		6-127	CHL 1 EXTERNAL WRITE SIGNAL	$C1EXWR
2A4A02	J04D-06/05	2A0B6-I3*I2		6-127	CHL 1 EXTERNAL CONNECT SIGNAL	$C1EXCN
2A4A02	J04D-08/07	2A0B6-F2*F3		6-127	CHL 1 EXTERNAL SELECT SIGNAL	$C1EXSL
2A4A02	J04D-10/09	2A0A6-C3*C2		6-135	CHL 1 EXTERNAL DATA SIGNAL	$C1EXDS
2A4A02	J04E-02*01	2A0A6-J2/J3		6-135	CHL 1 EXTERNAL REPLY SIGNAL	$C1EXRP
2A4A02	J04E-04*03	2A0B6-E3/E2		6-127	CHL 1 EXTERNAL REJECT SIGNAL	$C1EXRJ
2A4A02	J04E-06*05	2A0A6-I3/I2		6-135	CHL 1 EXTERNAL REJECT SIGNAL	$C1EXER
2A4A02	J04E-08*07	2A0B6-N2/N3		6-127	CHL 1 EXTERNAL PARITY ERROR	$C1EXPE
2A4A02	J04E-10*09	J03E-10/09	2A4A02		NOT USED	$C1EJA0
2A4A02	J04F-02/01	2A0A6-W0*W1		6-135	CHL 1 EXTERNAL WORD MARK	$C1EXWM
2A4A02	J04F-04/03	2A0B6-O1*O0		6-127	CHL 1 CLEAR TO EXTERNAL EQUIP	$C1EXCL
2A4A02	J04F-06*05	J03F-06/05	2A4A02		NOT USED	$C1EJA1
2A4A02	J04F-08*07	J03F-08/07	2A4A02		NOT USED	$C1EJA2
2A4A03	J01A-02/01	2A0B1-E0*E1		6-151	CHANNEL 2 EXTERNAL DATA BIT 12	$C2EX12

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A03	J01A-04/03	2A0B1-I0*I1		6-151	CHANNEL 2 EXTERNAL DATA BIT 13	$C2EXI3
2A4A03	J01A-06/05	2A0B1-M1*M0		6-151	CHANNEL 2 EXTERNAL DATA BIT 14	$C2EXI4
2A4A03	J01A-08/07	2A0B1-N0*N1		6-151	CHANNEL 2 EXTERNAL DATA BIT 15	$C2EXI5
2A4A03	J01A-10/09	2A0B1-S0*S1		6-151	CHANNEL 2 EXTERNAL DATA BIT 16	$C2EXI6
2A4A03	J01B-02/01	2A0B1-W0*W1		6-151	CHANNEL 2 EXTERNAL DATA BIT 17	$C2EXI7
2A4A03	J01B-04/03	2A0B1-B2*B3		6-151	CHANNEL 2 EXTERNAL DATA BIT 18	$C2EXI8
2A4A03	J01B-06/05	2A0B1-G2*G3		6-151	CHANNEL 2 EXTERNAL DATA BIT 19	$C2EXI9
2A4A03	J01B-08/07	2A0B1-M2*M3		6-151	CHANNEL 2 EXTERNAL DATA BIT 20	$C2EXI10
2A4A03	J01B-10/09	2A0B1-K3*K2		6-151	CHANNEL 2 EXTERNAL DATA BIT 21	$C2EXI11
2A4A03	J01C-02/01	2A0B1-Q3*Q2		6-151	CHANNEL 2 EXTERNAL DATA BIT 22	$C2EXI12
2A4A03	J01C-04/03	2A0B1-W2*W3		6-151	CHANNEL 2 EXTERNAL DATA BIT 23	$C2EXI13
2A4A03	J01C-06/05	2A0B1-U3*U2		6-151	CHAN 2 EXT PARITY BIT 2	$C2EXP2
2A4A03	J01C-08*07	2A0A3-X0/X1		6-137	CHL 2 EXT 24 BIT DEVICE CONNTD	$C2EXI14
2A4A03	J01C-10/09	J02C-10*09	2A4A03		NOT USED	$C2EJ00
2A4A03	J01D-02/01	J02D-02*01	2A4A03		NOT USED	$C2EJ01
2A4A03	J01D-04/03	J02D-04*03	2A4A03		NOT USED	$C2EJ02
2A4A03	J01D-06/05	J02D-06*05	2A4A03		NOT USED	$C2EJ03
2A4A03	J01D-08/07	J02D-08*07	2A4A03		NOT USED	$C2EJ04
2A4A03	J01D-10/09	J02D-10*09	2A4A03		NOT USED	$C2EJ05
2A4A03	J01E-02/01	J02E-02*01	2A4A03		NOT USED	$C2EJ06
2A4A03	J01E-04/03	J02E-04*03	2A4A03		NOT USED	$C2EJ07
2A4A03	J01E-06/05	J02E-06*05	2A4A03		NOT USED	$C2EJ08
2A4A03	J01E-08/07	J02E-08*07	2A4A03		NOT USED	$C2EJ09
2A4A03	J01E-10/09	J02E-10*09	2A4A03		NOT USED	$C2EJ10
2A4A03	J01F-02/01	J02F-02*01	2A4A03		NOT USED	$C2EJ11
2A4A03	J01F-04/03	J02F-04*03	2A4A03		NOT USED	$C2EJ12
2A4A03	J01F-06/05	J02F-06*05	2A4A03		NOT USED	$C2EJ13
2A4A03	J01F-08/07	J02F-08*07	2A4A03		NOT USED	$C2EJ14
2A4A03	J02A-02/01	2A0B1-F0*F1		6-151	CHANNEL 2 EXTERNAL DATA BIT 12	$C2EXI2
2A4A03	J02A-04/03	2A0B1-J0*J1		6-151	CHANNEL 2 EXTERNAL DATA BIT 13	$C2EXI3
2A4A03	J02A-06/05	2A0B1-L1*L0		6-151	CHANNEL 2 EXTERNAL DATA BIT 14	$C2EXI4
2A4A03	J02A-08/07	2A0B1-Q0*Q1		6-151	CHANNEL 2 EXTERNAL DATA BIT 15	$C2EXI5
2A4A03	J02A-10/09	2A0B1-T0*T1		6-151	CHANNEL 2 EXTERNAL DATA BIT 16	$C2EXI6
2A4A03	J02B-02/01	2A0B1-X0*X1		6-151	CHANNEL 2 EXTERNAL DATA BIT 17	$C2EXI7
2A4A03	J02B-04/03	2A0B1-C2*C3		6-151	CHANNEL 2 EXTERNAL DATA BIT 18	$C2EXI8
2A4A03	J02B-06/05	2A0B1-H2*H3		6-151	CHANNEL 2 EXTERNAL DATA BIT 19	$C2EXI9
2A4A03	J02B-08/07	2A0B1-N2*N3		6-151	CHANNEL 2 EXTERNAL DATA BIT 20	$C2EXI10
2A4A03	J02B-10/09	2A0B1-L3*L2		6-151	CHANNEL 2 EXTERNAL DATA BIT 21	$C2EXI11
2A4A03	J02C-02/01	2A0B1-R3*R2		6-151	CHANNEL 2 EXTERNAL DATA BIT 22	$C2EXI12
2A4A03	J02C-04/03	2A0B1-X2*X3		6-151	CHANNEL 2 EXTERNAL DATA BIT 23	$C2EXI13
2A4A03	J02C-06/05	2A0B1-V3*V2		6-151	CHAN 2 EXT PARITY BIT 2	$C2EXP2
2A4A03	J02C-08*07	2A0A3-X0/X1		6-137	CHL 2 EXT 24 BIT DEVICE CONNTD	$C2EXI14
2A4A03	J02C-10*09	J01C-10/09	2A4A03		NOT USED	$C2EJ00
2A4A03	J02D-02*01	J01D-02/01	2A4A03		NOT USED	$C2EJ01
2A4A03	J02D-04*03	J01D-04/03	2A4A03		NOT USED	$C2EJ02
2A4A03	J02D-06*05	J01D-06/05	2A4A03		NOT USED	$C2EJ03
2A4A03	J02D-08*07	J01D-08/07	2A4A03		NOT USED	$C2EJ04
2A4A03	J02D-10*09	J01D-10/09	2A4A03		NOT USED	$C2EJ05
2A4A03	J02E-02*01	J01E-02/01	2A4A03		NOT USED	$C2EJ06
2A4A03	J02E-04*03	J01E-04/03	2A4A03		NOT USED	$C2EJ07
2A4A03	J02E-06*05	J01E-06/05	2A4A03		NOT USED	$C2EJ08
2A4A03	J02E-08*07	J01E-08/07	2A4A03		NOT USED	$C2EJ09
2A4A03	J02E-10*09	J01E-10/09	2A4A03		NOT USED	$C2EJ10
2A4A03	J02F-02*01	J01F-02/01	2A4A03		NOT USED	$C2EJ11
2A4A03	J02F-04*03	J01F-04/03	2A4A03		NOT USED	$C2EJ12
2A4A03	J02F-06*05	J01F-06/05	2A4A03		NOT USED	$C2EJ13
2A4A03	J02F-08*07	J01F-08/07	2A4A03		NOT USED	$C2EJ14
2A4A03	J03A-02/01	2A0A1-E0*E1		6-149	CHANNEL 2 EXTERNAL DATA BIT 00	$C2EX00
2A4A03	J03A-04/03	2A0A1-I0*I1		6-149	CHANNEL 2 EXTERNAL DATA BIT 01	$C2EX01
2A4A03	J03A-06/05	2A0A1-M1*M0		6-149	CHANNEL 2 EXTERNAL DATA BIT 02	$C2EX02
2A4A03	J03A-08/07	2A0A1-N0*N1		6-149	CHANNEL 2 EXTERNAL DATA BIT 03	$C2EX03
2A4A03	J03A-10/09	2A0A1-S0*S1		6-149	CHANNEL 2 EXTERNAL DATA BIT 04	$C2EX04
2A4A03	J03B-02/01	2A0A1-W0*W1		6-149	CHANNEL 2 EXTERNAL DATA BIT 05	$C2EX05
2A4A03	J03B-04/03	2A0A1-B2*B3		6-149	CHANNEL 2 EXTERNAL DATA BIT 06	$C2EX06
2A4A03	J03B-06/05	2A0A1-G2*G3		6-149	CHANNEL 2 EXTERNAL DATA BIT 07	$C2EX07
2A4A03	J03B-08/07	2A0A1-M2*M3		6-149	CHANNEL 2 EXTERNAL DATA BIT 08	$C2EX08
2A4A03	J03B-10/09	2A0A1-K3*K2		6-149	CHANNEL 2 EXTERNAL DATA BIT 09	$C2EX09
2A4A03	J03C-02/01	2A0A1-Q3*Q2		6-149	CHANNEL 2 EXTERNAL DATA BIT 10	$C2EX10
2A4A03	J03C-04/03	2A0A1-W2*W3		6-149	CHANNEL 2 EXTERNAL DATA BIT 11	$C2EX11
2A4A03	J03C-06/05	2A0A1-U3*U2		6-149	CHL 2 EXTERNAL PARITY BIT 1	$C2EXP1
2A4A03	J03C-08/07	2A0B3-R2*R3		6-129	CHL 2 EXTERNAL BUSY SIGNAL	$C2EXRW
2A4A03	J03C-10/09	J04C-10*09	2A4A03		NOT USED	$C2EXRA
2A4A03	J03D-02/01	2A0B3-X0*X1		6-129	CHL 2 EXTERNAL READ SIGNAL	$C2EXRD
2A4A03	J03D-04/03	2A0B3-T1*T0		6-129	CHL 2 EXTERNAL WRITE SIGNAL	$C2EXWR
2A4A03	J03D-06/05	2A0B3-I2*I3		6-129	CHL 2 EXTERNAL CONNECT SIGNAL	$C2EXCN
2A4A03	J03D-08/07	2A0B3-F2*F3		6-129	CHL 2 EXTERNAL SELECT SIGNAL	$C2EXSL
2A4A03	J03D-10/09	2A0A3-C3*C2		6-137	CHL 2 EXTERNAL DATA SIGNAL	$C2EXDS
2A4A03	J03E-02*01	2A0A3-J2/J3		6-137	CHL 2 EXTERNAL REPLY SIGNAL	$C2EXRP
2A4A03	J03E-04*03	2A0B3-E3/E2		6-129	CHL 2 EXTERNAL REJECT SIGNAL	$C2EXRJ
2A4A03	J03E-06*05	2A0A3-I3/I2		6-137	CHL 2 EXTERNAL REJECT SIGNAL	$C2EXER
2A4A03	J03E-08*07	2A0B3-N2/N3		6-129	CHL 2 EXTERNAL PARITY ERROR	$C2EXPE
2A4A03	J03E-10/09	J04E-10*09	2A4A03		NOT USED	$C2EJA0
2A4A03	J03F-02/01	2A0A3-W0*W1		6-137	CHL 2 EXTERNAL WORD MARK	$C2EXWM
2A4A03	J03F-04/03	2A0B3-Q1*Q0		6-129	CHL 2 CLEAR TO EXTERNAL EQUIP	$C2EXCL
2A4A03	J03F-06/05	J04F-06*05	2A4A03		NOT USED	$C2EJA1
2A4A03	J03F-08/07	J04F-08*07	2A4A03		NOT USED	$C2EJA2
2A4A03	J04A-02/01	2A0A1-F0*F1		6-149	CHANNEL 2 EXTERNAL DATA BIT 00	$C2EX00
2A4A03	J04A-04/03	2A0A1-J0*J1		6-149	CHANNEL 2 EXTERNAL DATA BIT 01	$C2EX01
2A4A03	J04A-06/05	2A0A1-L1*L0		6-149	CHANNEL 2 EXTERNAL DATA BIT 02	$C2EX02
2A4A03	J04A-08/07	2A0A1-Q0*Q1		6-149	CHANNEL 2 EXTERNAL DATA BIT 03	$C2EX03
2A4A03	J04A-10/09	2A0A1-T0*T1		6-149	CHANNEL 2 EXTERNAL DATA BIT 04	$C2EX04
2A4A03	J04B-02/01	2A0A1-X0*X1		6-149	CHANNEL 2 EXTERNAL DATA BIT 05	$C2EX05
2A4A03	J04B-04/03	2A0A1-C2*C3		6-149	CHANNEL 2 EXTERNAL DATA BIT 06	$C2EX06
2A4A03	J04B-06/05	2A0A1-H2*H3		6-149	CHANNEL 2 EXTERNAL DATA BIT 07	$C2EX07
2A4A03	J04B-08/07	2A0A1-N2*N3		6-149	CHANNEL 2 EXTERNAL DATA BIT 08	$C2EX08
2A4A03	J04B-10/09	2A0A1-L3*L2		6-149	CHANNEL 2 EXTERNAL DATA BIT 09	$C2EX09
2A4A03	J04C-02/01	2A0A1-R3*R2		6-149	CHANNEL 2 EXTERNAL DATA BIT 10	$C2EX10
2A4A03	J04C-04/03	2A0A1-X2*X3		6-149	CHANNEL 2 EXTERNAL DATA BIT 11	$C2EX11
2A4A03	J04C-06/05	2A0A1-V3*V2		6-149	CHL 2 EXTERNAL PARITY BIT 1	$C2EXP1
2A4A03	J04C-08/07	2A0B3-R2*R3		6-129	CHL 2 EXTERNAL BUSY SIGNAL	$C2EXRW
2A4A03	J04C-10*09	J03C-10/09	2A4A03		NOT USED	$C2EXRA
2A4A03	J04D-02/01	2A0B3-X0*X1		6-129	CHL 2 EXTERNAL READ SIGNAL	$C2EXRD
2A4A03	J04D-04/03	2A0B3-T1*T0		6-129	CHL 2 EXTERNAL WRITE SIGNAL	$C2EXWR
2A4A03	J04D-06/05	2A0B3-I3*I2		6-129	CHL 2 EXTERNAL CONNECT SIGNAL	$C2EXCN
2A4A03	J04D-08/07	2A0B3-F2*F3		6-129	CHL 2 EXTERNAL SELECT SIGNAL	$C2EXSL
2A4A03	J04D-10/09	2A0A3-C3*C2		6-137	CHL 2 EXTERNAL DATA SIGNAL	$C2EXDS
2A4A03	J04E-02*01	2A0A3-J2/J3		6-137	CHL 2 EXTERNAL REPLY SIGNAL	$C2EXRP
2A4A03	J04E-04*03	2A0B3-E3/E2		6-129	CHL 2 EXTERNAL REJECT SIGNAL	$C2EXRJ
2A4A03	J04E-06*05	2A0A3-I3/I2		6-137	CHL 2 EXTERNAL REJECT SIGNAL	$C2EXER
2A4A03	J04E-08*07	2A0B3-N2/N3		6-129	CHL 2 EXTERNAL PARITY ERROR	$C2EXPE
2A4A03	J04E-10*09	J03E-10/09	2A4A03		NOT USED	$C2EJA0
2A4A03	J04F-02/01	2A0A3-W0*W1		6-137	CHL 2 EXTERNAL WORD MARK	$C2EXWM
2A4A03	J04F-04/03	2A0B3-Q1*Q0		6-129	CHL 2 CLEAR TO EXTERNAL EQUIP	$C2EXCL
2A4A03	J04F-06*05	J03F-06/05	2A4A03		NOT USED	$C2EJA1
2A4A03	J04F-08*07	J03F-08/07	2A4A03		NOT USED	$C2EJA2
2A4A04	J01A-02/01	2A0B0-E0*E1		6-155	CHANNEL 3 EXTERNAL DATA BIT 12	$C3EX12
2A4A04	J01A-04/03	2A0B0-I0*I1		6-155	CHANNEL 3 EXTERNAL DATA BIT 13	$C3EX13
2A4A04	J01A-06/05	2A0B0-M1*M0		6-155	CHANNEL 3 EXTERNAL DATA BIT 14	$C3EX14
2A4A04	J01A-08/07	2A0B0-N0*N1		6-155	CHANNEL 3 EXTERNAL DATA BIT 15	$C3EX15
2A4A04	J01A-10/09	2A0B0-S0*S1		6-155	CHANNEL 3 EXTERNAL DATA BIT 16	$C3EX16
2A4A04	J01B-02/01	2A0B0-W0*W1		6-155	CHANNEL 3 EXTERNAL DATA BIT 17	$C3EX17
2A4A04	J01B-04/03	2A0B0-B2*B3		6-155	CHANNEL 3 EXTERNAL DATA BIT 18	$C3EX18
2A4A04	J01B-06/05	2A0B0-G2*G3		6-155	CHANNEL 3 EXTERNAL DATA BIT 19	$C3EX19
2A4A04	J01B-08/07	2A0B0-M2*M3		6-155	CHANNEL 3 EXTERNAL DATA BIT 20	$C3EX20
2A4A04	J01B-10/09	2A0B0-K3*K2		6-155	CHANNEL 3 EXTERNAL DATA BIT 21	$C3EX21
2A4A04	J01C-02/01	2A0B0-Q3*Q2		6-155	CHANNEL 3 EXTERNAL DATA BIT 22	$C3EX22
2A4A04	J01C-04/03	2A0B0-W2*W3		6-155	CHANNEL 3 EXTERNAL DATA BIT 23	$C3EX23
2A4A04	J01C-06/05	2A0B0-U3*U2		6-155	CHL 3 EXTERNAL PARITY BIT 2	$C3EXP2
2A4A04	J01C-08*07	2A0A2-X0/X1		6-139	CHL 3 EXT 24 BIT DEVICE CONNTD	$C3EX24
2A4A04	J01C-10/09	J02C-10*09	2A4A04		NOT USED	$C3EJ00
2A4A04	J01D-02/01	J02D-02*01	2A4A04		NOT USED	$C3EJ01
2A4A04	J01D-04/03	J02D-04*03	2A4A04		NOT USED	$C3EJ02
2A4A04	J01D-06/05	J02D-06*05	2A4A04		NOT USED	$C3EJ03
2A4A04	J01D-08/07	J02D-08*07	2A4A04		NOT USED	$C3EJ04
2A4A04	J01D-10/09	J02D-10*09	2A4A04		NOT USED	$C3EJ05
2A4A04	J01E-02/01	J02E-02*01	2A4A04		NOT USED	$C3EJ06
2A4A04	J01E-04/03	J02E-04*03	2A4A04		NOT USED	$C3EJ07
2A4A04	J01E-06/05	J02E-06*05	2A4A04		NOT USED	$C3EJ08
2A4A04	J01E-08/07	J02E-08*07	2A4A04		NOT USED	$C3EJ09
2A4A04	J01E-10/09	J02E-10*09	2A4A04		NOT USED	$C3EJ10
2A4A04	J01F-02/01	J02F-02*01	2A4A04		NOT USED	$C3EJ11
2A4A04	J01F-04/03	J02F-04*03	2A4A04		NOT USED	$C3EJ12
2A4A04	J01F-06/05	J02F-06*05	2A4A04		NOT USED	$C3EJ13
2A4A04	J01F-08/07	J02F-08*07	2A4A04		NOT USED	$C3EJ14
2A4A04	J02A-02/01	2A0B0-F0*F1		6-155	CHANNEL 3 EXTERNAL DATA BIT 12	$C3EX12
2A4A04	J02A-04/03	2A0B0-J0*J1		6-155	CHANNEL 3 EXTERNAL DATA BIT 13	$C3EX13
2A4A04	J02A-06/05	2A0B0-L1*L0		6-155	CHANNEL 3 EXTERNAL DATA BIT 14	$C3EX14

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A04	J02A-08/07	2A0B0-00*01		6-155	CHANNEL 3 EXTERNAL DATA BIT 15	$C3EX15
2A4A04	J02A-10/09	2A0B0-T0*T1		6-155	CHANNEL 3 EXTERNAL DATA BIT 16	$C3EX16
2A4A04	J02B-02/01	2A0B0-X0*X1		6-155	CHANNEL 3 EXTERNAL DATA BIT 17	$C3EX17
2A4A04	J02B-04/03	2A0B0-C2*C3		6-155	CHANNEL 3 EXTERNAL DATA BIT 18	$C3EX18
2A4A04	J02B-06/05	2A0B0-H2*H3		6-155	CHANNEL 3 EXTERNAL DATA BIT 19	$C3EX19
2A4A04	J02B-08/07	2A0B0-N2*N3		6-155	CHANNEL 3 EXTERNAL DATA BIT 20	$C3EX20
2A4A04	J02B-10/09	2A0B0-L3*L2		6-155	CHANNEL 3 EXTERNAL DATA BIT 21	$C3EX21
2A4A04	J02C-02/01	2A0B0-R3*R2		6-155	CHANNEL 3 EXTERNAL DATA BIT 22	$C3EX22
2A4A04	J02C-04/03	2A0B0-X2*X3		6-155	CHANNEL 3 EXTERNAL DATA BIT 23	$C3EX23
2A4A04	J02C-06/05	2A0B0-V3*V2		6-155	CHL 3 EXTERNAL PARITY BIT 2	$C3EXP2
2A4A04	J02C-08*07	2A0A2-X0/X1		6-139	CHL 3 EXT 24 BIT DEVICE CONNTD	$C3EX24
2A4A04	J02C-10*09	J01C-10/09	2A4A04		NOT USED	$C3EJ00
2A4A04	J02D-02*01	J01D-02/01	2A4A04		NOT USED	$C3EJ01
2A4A04	J02D-04*03	J01D-04/03	2A4A04		NOT USED	$C3EJ02
2A4A04	J02D-06*05	J01D-06/05	2A4A04		NOT USED	$C3EJ03
2A4A04	J02D-08*07	J01D-08/07	2A4A04		NOT USED	$C3EJ04
2A4A04	J02D-10*09	J01D-10/09	2A4A04		NOT USED	$C3EJ05
2A4A04	J02E-02*01	J01E-02/01	2A4A04		NOT USED	$C3EJ06
2A4A04	J02E-04*03	J01E-04/03	2A4A04		NOT USED	$C3EJ07
2A4A04	J02E-06*05	J01E-06/05	2A4A04		NOT USED	$C3EJ08
2A4A04	J02E-08*07	J01E-08/07	2A4A04		NOT USED	$C3EJ09
2A4A04	J02E-10*09	J01E-10/09	2A4A04		NOT USED	$C3EJ10
2A4A04	J02F-02*01	J01F-02/01	2A4A04		NOT USED	$C3EJ11
2A4A04	J02F-04*03	J01F-04/03	2A4A04		NOT USED	$C3EJ12
2A4A04	J02F-06*05	J01F-06/05	2A4A04		NOT USED	$C3EJ13
2A4A04	J02F-08*07	J01F-08/07	2A4A04		NOT USED	$C3EJ14
2A4A04	J03A-02/01	2A0A0-E0*E1		6-153	CHANNEL 3 EXTERNAL DATA BIT 00	$C3EX00
2A4A04	J03A-04/03	2A0A0-I0*I1		6-153	CHANNEL 3 EXTERNAL DATA BIT 01	$C3EX01
2A4A04	J03A-06/05	2A0A0-M1*M0		6-153	CHANNEL 3 EXTERNAL DATA BIT 02	$C3EX02
2A4A04	J03A-08/07	2A0A0-N0*N1		6-153	CHANNEL 3 EXTERNAL DATA BIT 03	$C3EX03
2A4A04	J03A-10/09	2A0A0-S0*S1		6-153	CHANNEL 3 EXTERNAL DATA BIT 04	$C3EX04
2A4A04	J03B-02/01	2A0A0-W0*W1		6-153	CHANNEL 3 EXTERNAL DATA BIT 05	$C3EX05
2A4A04	J03B-04/03	2A0A0-B2*B3		6-153	CHANNEL 3 EXTERNAL DATA BIT 06	$C3EX06
2A4A04	J03B-06/05	2A0A0-G2*G3		6-153	CHANNEL 3 EXTERNAL DATA BIT 07	$C3EX07
2A4A04	J03B-08/07	2A0A0-M2*M3		6-153	CHANNEL 3 EXTERNAL DATA BIT 08	$C3EX08
2A4A04	J03B-10/09	2A0A0-K3*K2		6-153	CHANNEL 3 EXTERNAL DATA BIT 09	$C3EX09
2A4A04	J03C-02/01	2A0A0-Q3*Q2		6-153	CHANNEL 3 EXTERNAL DATA BIT 10	$C3EX10
2A4A04	J03C-04/03	2A0A0-W2*W3		6-153	CHANNEL 3 EXTERNAL DATA BIT 11	$C3EX11
2A4A04	J03C-06/05	2A0A0-U3*U2		6-153	CHL 3 EXTERNAL PARITY BIT 1	$C3EXP1
2A4A04	J03C-08/07	2A0B2-R2*R3		6-131	CHL 3 EXTERNAL BUSY SIGNAL	$C3EXRW
2A4A04	J03C-10/09	J04C-10*09	2A4A04		NOT USED	$C3EXRA
2A4A04	J03D-02/01	2A0B2-X0*X1		6-131	CHL 3 EXTERNAL READ SIGNAL	$C3EXRD
2A4A04	J03D-04/03	2A0B2-T1*T0		6-131	CHL 3 EXTERNAL WRITE SIGNAL	$C3EXWR
2A4A04	J03D-06/05	2A0B2-I3*I2		6-131	CHL 3 EXTERNAL CONNECT SIGNAL	$C3EXCN
2A4A04	J03D-08/07	2A0B2-F2*F3		6-131	CHL 3 EXTERNAL SELECT SIGNAL	$C3EXSL
2A4A04	J03D-10/09	2A0A2-C3*C2		6-139	CHL 3 EXTERNAL DATA SIGNAL	$C3EXDS
2A4A04	J03E-02*01	2A0A2-J2/J3		6-139	CHL 3 EXTERNAL REPLY SIGNAL	$C3EXRP
2A4A04	J03E-04*03	2A0B2-E3/E2		6-131	CHL 3 EXTERNAL REJECT SIGNAL	$C3EXRJ
2A4A04	J03E-06*05	2A0A2-I3/I2		6-139	CHL 3 EXTERNAL REJECT SIGNAL	$C3EXER
2A4A04	J03E-08*07	2A0B2-N2/N3		6-131	CHL 3 EXTERNAL PARITY ERROR	$C3EXPE
2A4A04	J03E-10/09	J04E-10*09	2A4A04		NOT USED	$C3EJA0
2A4A04	J03F-02/01	2A0A2-W0*W1		6-139	CHL 3 EXTERNAL WORD MARK	$C3EXWM
2A4A04	J03F-04/03	2A0B2-01*00		6-131	CHL 3 CLEAR TO EXTERNAL EQUIP	$C3EXCL
2A4A04	J03F-06/05	J04F-06*05	2A4A04		NOT USED	$C3EJA1
2A4A04	J03F-08/07	J04F-08*07	2A4A04		NOT USED	$C3EJA2
2A4A04	J04A-02/01	2A0A0-F0*F1		6-153	CHANNEL 3 EXTERNAL DATA BIT 00	$C3EX00
2A4A04	J04A-04/03	2A0A0-J0*J1		6-153	CHANNEL 3 EXTERNAL DATA BIT 01	$C3EX01
2A4A04	J04A-06/05	2A0A0-L1*L0		6-153	CHANNEL 3 EXTERNAL DATA BIT 02	$C3EX02
2A4A04	J04A-08/07	2A0A0-00*01		6-153	CHANNEL 3 EXTERNAL DATA BIT 03	$C3EX03
2A4A04	J04A-10/09	2A0A0-T0*T1		6-153	CHANNEL 3 EXTERNAL DATA BIT 04	$C3EX04
2A4A04	J04B-02/01	2A0A0-X0*X1		6-153	CHANNEL 3 EXTERNAL DATA BIT 05	$C3EX05
2A4A04	J04B-04/03	2A0A0-C2*C3		6-153	CHANNEL 3 EXTERNAL DATA BIT 06	$C3EX06
2A4A04	J04B-06/05	2A0A0-H2*H3		6-153	CHANNEL 3 EXTERNAL DATA BIT 07	$C3EX07
2A4A04	J04B-08/07	2A0A0-N2*N3		6-153	CHANNEL 3 EXTERNAL DATA BIT 08	$C3EX08
2A4A04	J04B-10/09	2A0A0-L3*L2		6-153	CHANNEL 3 EXTERNAL DATA BIT 09	$C3EX09
2A4A04	J04C-02/01	2A0A0-R3*R2		6-153	CHANNEL 3 EXTERNAL DATA BIT 10	$C3EX10
2A4A04	J04C-04/03	2A0A0-X2*X3		6-153	CHANNEL 3 EXTERNAL DATA BIT 11	$C3EX11
2A4A04	J04C-06/05	2A0A0-V3*V2		6-153	CHL 3 EXTERNAL PARITY BIT 1	$C3EXP1
2A4A04	J04C-08/07	2A0B2-R2*R3		6-131	CHL 3 EXTERNAL BUSY SIGNAL	$C3EXRW
2A4A04	J04C-10*09	J03C-10/09	2A4A04		NOT USED	$C3EXRA
2A4A04	J04D-02/01	2A0B2-X0*X1		6-131	CHL 3 EXTERNAL READ SIGNAL	$C3EXRD
2A4A04	J04D-04/03	2A0B2-T1*T0		6-131	CHL 3 EXTERNAL WRITE SIGNAL	$C3EXWR
2A4A04	J04D-06/05	2A0B2-I3*I2		6-131	CHL 3 EXTERNAL CONNECT SIGNAL	$C3EXCN
2A4A04	J04D-08/07	2A0B2-F2*F3		6-131	CHL 3 EXTERNAL SELECT SIGNAL	$C3EXSL

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A04	J04D-10/09	2A0A2-C3*C2		6-139	CHL 3 EXTERNAL DATA SIGNAL	$C3EXDS
2A4A04	J04E-02*01	2A0A2-J2/J3		6-139	CHL 3 EXTERNAL REPLY SIGNAL	$C3EXRP
2A4A04	J04E-04*03	2A0B2-E3/E2		6-131	CHL 3 EXTERNAL REJECT SIGNAL	$C3EXRJ
2A4A04	J04E-06*05	2A0A2-I3/I2		6-139	CHL 3 EXTERNAL REJECT SIGNAL	$C3EXER
2A4A04	J04E-08*07	2A0B2-N2/N3		6-131	CHL 3 EXTERNAL PARITY ERROR	$C3EXPE
2A4A04	J04E-10*09	J03E-10/09	2A4A04		NOT USED	$C3EJA0
2A4A04	J04F-02/01	2A0A2-W0*W1		6-139	CHL 3 EXTERNAL WORD MARK	$C3EXWM
2A4A04	J04F-04/03	2A0B2-01*00		6-131	CHL 3 CLEAR TO EXTERNAL EQUIP	$C3EXCL
2A4A04	J04F-06*05	J03F-06/05	2A4A04		NOT USED	$C3EJA1
2A4A04	J04F-08*07	J03F-08/07	2A4A04		NOT USED	$C3EJA2
2A4A05	J01A-02*01	2B0A2-F0/F1		6- 87	CHL 1 EXTERNAL STATUS BIT 00	$C1ES00
2A4A05	J01A-04*03	2B0A2-J1/J0		6- 87	CHL 1 EXTERNAL STATUS BIT 01	$C1ES01
2A4A05	J01A-06*05	2B0A2-Q0/Q1		6- 87	CHL 1 EXTERNAL STATUS BIT 02	$C1ES02
2A4A05	J01A-08*07	2B0A2-T1/T0		6- 87	CHL 1 EXTERNAL STATUS BIT 03	$C1ES03
2A4A05	J01A-10*09	2B0A2-C3/C2		6- 87	CHL 1 EXTERNAL STATUS BIT 04	$C1ES04
2A4A05	J01B-02*01	2B0A2-I2/I3		6- 87	CHL 1 EXTERNAL STATUS BIT 05	$C1ES05
2A4A05	J01B-04*03	2B0A2-L2/L3		6- 87	CHL 1 EXTERNAL STATUS BIT 06	$C1ES06
2A4A05	J01B-06*05	2B0A2-S2/S3		6- 87	CHL 1 EXTERNAL STATUS BIT 07	$C1ES07
2A4A05	J01B-08*07	2B0A2-X0/X1		6- 87	CHL 1 EXTERNAL STATUS BIT 08	$C1ES08
2A4A05	J01B-10*09	2B0A2-W3/W2		6- 87	CHL 1 EXTERNAL STATUS BIT 09	$C1ES09
2A4A05	J01C-02*01	2B0A2-T2/T3		6- 87	CHL 1 EXTERNAL STATUS BIT 10	$C1ES10
2A4A05	J01C-04*03	2B0A2-U2/U3		6- 87	CHL 1 EXTERNAL STATUS BIT 11	$C1ES11
2A4A05	J01C-06/05	2B0A2-H2*H3		6- 87	CHAN 1 EXT COMPUTER RUNNING	$C1EXRN
2A4A05	J01C-08*07	J02C-08/07	2A4A05		NEGATE BCD CONV(NOT USED)	$C1EXNC
2A4A05	J01C-10/09	2B0A4-P0*P1		6-103	CHL 1 EXTERNAL SUPPRESS A/D	$C1EXSP
2A4A05	J01D-02*01	2B0A2-C1/C0		6- 87	CHL 1 EXT. LINE INTERRUPT 0	$C1EXI0
2A4A05	J01D-04*03	2B0A2-K0/K1		6- 87	CHL 1 EXT. LINE INTERRUPT 1	$C1EXI1
2A4A05	J01D-06*05	2B0A2-P0/P1		6- 87	CHL 1 EXT. LINE INTERRUPT 2	$C1EXI2
2A4A05	J01D-08*07	2B0A2-U0/U1		6- 87	CHL 1 EXT. LINE INTERRUPT 3	$C1EXI3
2A4A05	J01D-10*09	2B0A2-E3/E2		6- 87	CHL 1 EXT. LINE INTERRUPT 4	$C1EXI4
2A4A05	J01E-02*01	2B0A2-J2/J3		6- 87	CHL 1 EXT. LINE INTERRUPT 5	$C1EXI5
2A4A05	J01E-04*03	2B0A2-M2/M3		6- 87	CHL 1 EXT. LINE INTERRUPT 6	$C1EXI6
2A4A05	J01E-06*05	2B0A2-R2/R3		6- 87	CHL 1 EXT. LINE INTERRUPT 7	$C1EXI7
2A4A05	J01E-08/07	2B0A4-T1*T0		6-103	CHL 1 EXTERNAL CLEAR INTERRUPT	$C1EXCI
2A4A05	J01E-10*09	2B0A4-W0/W1		6-103	NOT CHAN 1 EXT INTERRUPT LOCKOUT OVERRIDE	$C1EXOV
2A4A05	J01F-08*07	J02F-08/07	2A4A05		NOT USED	$C1EXSS
2A4A05	J02A-02*01	2B0A2-F0/F1		6- 87	CHL 1 EXTERNAL STATUS BIT 00	$C1ES00
2A4A05	J02A-04*03	2B0A2-J1/J0		6- 87	CHL 1 EXTERNAL STATUS BIT 01	$C1ES01
2A4A05	J02A-06*05	2B0A2-Q0/Q1		6- 87	CHL 1 EXTERNAL STATUS BIT 02	$C1ES02
2A4A05	J02A-08*07	2B0A2-T1/T0		6- 87	CHL 1 EXTERNAL STATUS BIT 03	$C1ES03
2A4A05	J02A-10*09	2B0A2-C3/C2		6- 87	CHL 1 EXTERNAL STATUS BIT 04	$C1ES04
2A4A05	J02B-02*01	2B0A2-I2/I3		6- 87	CHL 1 EXTERNAL STATUS BIT 05	$C1ES05
2A4A05	J02B-04*03	2B0A2-L2/L3		6- 87	CHL 1 EXTERNAL STATUS BIT 06	$C1ES06
2A4A05	J02B-06*05	2B0A2-S2/S3		6- 87	CHL 1 EXTERNAL STATUS BIT 07	$C1ES07
2A4A05	J02B-08*07	2B0A2-X0/X1		6- 87	CHL 1 EXTERNAL STATUS BIT 08	$C1ES08
2A4A05	J02B-10*09	2B0A2-W3/W2		6- 87	CHL 1 EXTERNAL STATUS BIT 09	$C1ES09
2A4A05	J02C-02*01	2B0A2-T2/T3		6- 87	CHL 1 EXTERNAL STATUS BIT 10	$C1ES10
2A4A05	J02C-04*03	2B0A2-U2/U3		6- 87	CHL 1 EXTERNAL STATUS BIT 11	$C1ES11
2A4A05	J02C-06/05	2B0A2-H2*H3		6- 87	CHAN 1 EXT COMPUTER RUNNING	$C1EXRN
2A4A05	J02C-08/07	J01C-08*07	2A4A05		NEGATE BCD CONV(NOT USED)	$C1EXNC
2A4A05	J02C-10/09	2B0A4-P0*P1		6-103	CHL 1 EXTERNAL SUPPRESS A/D	$C1EXSP
2A4A05	J02D-02*01	2B0A2-C1/C0		6- 87	CHL 1 EXT. LINE INTERRUPT 0	$C1EXI0
2A4A05	J02D-04*03	2B0A2-K0/K1		6- 87	CHL 1 EXT. LINE INTERRUPT 1	$C1EXI1
2A4A05	J02D-06*05	2B0A2-P0/P1		6- 87	CHL 1 EXT. LINE INTERRUPT 2	$C1EXI2
2A4A05	J02D-08*07	2B0A2-U0/U1		6- 87	CHL 1 EXT. LINE INTERRUPT 3	$C1EXI3
2A4A05	J02D-10*09	2B0A2-E3/E2		6- 87	CHL 1 EXT. LINE INTERRUPT 4	$C1EXI4
2A4A05	J02E-02*01	2B0A2-J2/J3		6- 87	CHL 1 EXT. LINE INTERRUPT 5	$C1EXI5
2A4A05	J02E-04*03	2B0A2-M2/M3		6- 87	CHL 1 EXT. LINE INTERRUPT 6	$C1EXI6
2A4A05	J02E-06*05	2B0A2-R2/R3		6- 87	CHL 1 EXT. LINE INTERRUPT 7	$C1EXI7
2A4A05	J02E-08/07	2B0A4-T1*T0		6-103	CHL 1 EXTERNAL CLEAR INTERRUPT	$C1EXCI
2A4A05	J02E-10*09	2B0A4-W0/W1		6-103	NOT CHAN 1 EXT INTERRUPT LOCKOUT OVERRIDE	$C1EXOV
2A4A05	J02F-08/07	J01F-08*07	2A4A05		NOT USED	$C1EXSS
2A4A05	J03A-02*01	2B0A3-F0/F1		6- 85	CHL 0 EXTERNAL STATUS BIT 00	$C0ES00
2A4A05	J03A-04*03	2B0A3-J1/J0		6- 85	CHL 0 EXTERNAL STATUS BIT 01	$C0ES01
2A4A05	J03A-06*05	2B0A3-Q0/Q1		6- 85	CHL 0 EXTERNAL STATUS BIT 02	$C0ES02
2A4A05	J03A-08*07	2B0A3-T1/T0		6- 85	CHL 0 EXTERNAL STATUS BIT 03	$C0ES03
2A4A05	J03A-10*09	2B0A3-C3/C2		6- 85	CHL 0 EXTERNAL STATUS BIT 04	$C0ES04
2A4A05	J03B-02*01	2B0A3-I2/I3		6- 85	CHL 0 EXTERNAL STATUS BIT 05	$C0ES05
2A4A05	J03B-04*03	2B0A3-L2/L3		6- 85	CHL 0 EXTERNAL STATUS BIT 06	$C0ES06

429

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A05	J03B-06*05	2B0A3-S2/S3		6- 85	CHL 0 EXTERNAL STATUS BIT 07	$C0ES07
2A4A05	J03B-08*07	2B0A3-X0/X1		6- 85	CHL 0 EXTERNAL STATUS BIT 08	$C0ES08
2A4A05	J03B-10*09	2B0A3-W3/W2		6- 85	CHL 0 EXTERNAL STATUS BIT 09	$C0ES09
2A4A05	J03C-02*01	2B0A3-T2/T3		6- 85	CHL 0 EXTERNAL STATUS BIT 10	$C0ES10
2A4A05	J03C-04*03	2B0A3-U2/U3		6- 85	CHL 0 EXTERNAL STATUS BIT 11	$C0ES11
2A4A05	J03C-06/05	2B0A3-H2*H3		6- 85	CHAN 0 EXTERNAL CMPTR RUNNING	$C0EXRN
2A4A05	J03C-08*07	J04C-08/07	2A4A05		NEGATE BCD CONV(NOT USED)	$C0EXNC
2A4A05	J03C-10/09	2B0A4-D1*D0		6-103	CHL 0 EXTERNAL SUPPRESS A/D	$C0EXSP
2A4A05	J03D-02*01	2B0A3-C1/C0		6- 85	CHL 0 EXT. LINE INTERRUPT 0	$C0EXI0
2A4A05	J03D-04*03	2B0A3-K0/K1		6- 85	CHL 0 EXT. LINE INTERRUPT 1	$C0EXI1
2A4A05	J03D-06*05	2B0A3-P0/P1		6- 85	CHL 0 EXT. LINE INTERRUPT 2	$C0EXI2
2A4A05	J03D-08*07	2B0A3-U0/U1		6- 85	CHL 0 EXT. LINE INTERRUPT 3	$C0EXI3
2A4A05	J03D-10*09	2B0A3-E3/E2		6- 85	CHL 0 EXT. LINE INTERRUPT 4	$C0EXI4
2A4A05	J03E-02*01	2B0A3-J2/J3		6- 85	CHL 0 EXT. LINE INTERRUPT 5	$C0EXI5
2A4A05	J03E-04*03	2B0A3-M2/M3		6- 85	CHL 0 EXT. LINE INTERRUPT 6	$C0EXI6
2A4A05	J03E-06*05	2B0A3-R2/R3		6- 85	CHL 0 EXT. LINE INTERRUPT 7	$C0EXI7
2A4A05	J03E-08/07	2B0A4-C1*C0		6-103	CHL 0 EXTERNAL CLEAR INTERRUPT	$C0EXCI
2A4A05	J03E-10*09	2B0A4-M0/M1		6-103	NOT CHAN 0 EXT INTERRUPT LOCKOUT OVERRIDE	$C0EXOV
2A4A05	J03F-08*07	J04F-08/07	2A4A05		NOT USED	$C0EXSS
2A4A05	J04A-02*01	2B0A3-F0/F1		6- 85	CHL 0 EXTERNAL STATUS BIT 00	$C0ES00
2A4A05	J04A-04*03	2B0A3-J1/J0		6- 85	CHL 0 EXTERNAL STATUS BIT 01	$C0ES01
2A4A05	J04A-06*05	2B0A3-Q0/Q1		6- 85	CHL 0 EXTERNAL STATUS BIT 02	$C0ES02
2A4A05	J04A-08*07	2B0A3-T1/T0		6- 85	CHL 0 EXTERNAL STATUS BIT 03	$C0ES03
2A4A05	J04A-10*09	2B0A3-C3/C2		6- 85	CHL 0 EXTERNAL STATUS BIT 04	$C0ES04
2A4A05	J04B-02*01	2B0A3-I2/I3		6- 85	CHL 0 EXTERNAL STATUS BIT 05	$C0ES05
2A4A05	J04B-04*03	2B0A3-L2/L3		6- 85	CHL 0 EXTERNAL STATUS BIT 06	$C0ES06
2A4A05	J04B-06*05	2B0A3-S2/S3		6- 85	CHL 0 EXTERNAL STATUS BIT 07	$C0ES07
2A4A05	J04B-08*07	2B0A3-X0/X1		6- 85	CHL 0 EXTERNAL STATUS BIT 08	$C0ES08
2A4A05	J04B-10*09	2B0A3-W3/W2		6- 85	CHL 0 EXTERNAL STATUS BIT 09	$C0ES09
2A4A05	J04C-02*01	2B0A3-T2/T3		6- 85	CHL 0 EXTERNAL STATUS BIT 10	$C0ES10
2A4A05	J04C-04*03	2B0A3-U2/U3		6- 85	CHL 0 EXTERNAL STATUS BIT 11	$C0ES11
2A4A05	J04C-06/05	2B0A3-H2*H3		6- 85	CHAN 0 EXTERNAL CMPTR RUNNING	$C0EXRN
2A4A05	J04C-08/07	J03C-08*07	2A4A05		NEGATE BCD CONV(NOT USED)	$C0EXNC
2A4A05	J04C-10/09	2B0A4-D1*D0		6-103	CHL 0 EXTERNAL SUPPRESS A/D	$C0EXSP
2A4A05	J04D-02*01	2B0A3-C1/C0		6- 85	CHL 0 EXT. LINE INTERRUPT 0	$C0EXI0
2A4A05	J04D-04*03	2B0A3-K0/K1		6- 85	CHL 0 EXT. LINE INTERRUPT 1	$C0EXI1
2A4A05	J04D-06*05	2B0A3-P0/P1		6- 85	CHL 0 EXT. LINE INTERRUPT 2	$C0EXI2
2A4A05	J04D-08*07	2B0A3-U0/U1		6- 85	CHL 0 EXT. LINE INTERRUPT 3	$C0EXI3
2A4A05	J04D-10*09	2B0A3-E3/E2		6- 85	CHL 0 EXT. LINE INTERRUPT 4	$C0EXI4
2A4A05	J04E-02*01	2B0A3-J2/J3		6- 85	CHL 0 EXT. LINE INTERRUPT 5	$C0EXI5
2A4A05	J04E-04*03	2B0A3-M2/M3		6- 85	CHL 0 EXT. LINE INTERRUPT 6	$C0EXI6
2A4A05	J04E-06*05	2B0A3-R2/R3		6- 85	CHL 0 EXT. LINE INTERRUPT 7	$C0EXI7
2A4A05	J04E-08/07	2B0A4-C1*C0		6-103	CHL 0 EXTERNAL CLEAR INTERRUPT	$C0EXCI
2A4A05	J04E-10*09	2B0A4-M0/M1		6-103	NOT CHAN 0 EXT INTERRUPT LOCKOUT OVERRIDE	$C0EXOV
2A4A05	J04F-08/07	J03F-08*07	2A4A05		NOT USED	$C0EXSS
2A4A06	J01A-02*01	2B0A0-F0/F1		6- 91	CHL 3 EXTERNAL STATUS BIT 00	$C3ES00
2A4A06	J01A-04*03	2B0A0-J1/J0		6- 91	CHL 3 EXTERNAL STATUS BIT 01	$C3ES01
2A4A06	J01A-06*05	2B0A0-Q0/Q1		6- 91	CHL 3 EXTERNAL STATUS BIT 02	$C3ES02
2A4A06	J01A-08*07	2B0A0-T1/T0		6- 91	CHL 3 EXTERNAL STATUS BIT 03	$C3ES03
2A4A06	J01A-10*09	2B0A0-C3/C2		6- 91	CHL 3 EXTERNAL STATUS BIT 04	$C3ES04
2A4A06	J01B-02*01	2B0A0-I2/I3		6- 91	CHL 3 EXTERNAL STATUS BIT 05	$C3ES05
2A4A06	J01B-04*03	2B0A0-L2/L3		6- 91	CHL 3 EXTERNAL STATUS BIT 06	$C3ES06
2A4A06	J01B-06*05	2B0A0-S2/S3		6- 91	CHL 3 EXTERNAL STATUS BIT 07	$C3ES07
2A4A06	J01B-08*07	2B0A0-X0/X1		6- 91	CHL 3 EXTERNAL STATUS BIT 08	$C3ES08
2A4A06	J01B-10*09	2B0A0-W3/W2		6- 91	CHL 3 EXTERNAL STATUS BIT 09	$C3ES09
2A4A06	J01C-02*01	2B0A0-T2/T3		6- 91	CHL 3 EXTERNAL STATUS BIT 10	$C3ES10
2A4A06	J01C-04*03	2B0A0-U2/U3		6- 91	CHL 3 EXTERNAL STATUS BIT 11	$C3ES11
2A4A06	J01C-06/05	2B0A0-H2*H3		6- 91	CHAN 3 EXT CMPTR RUNNING	$C3EXRN
2A4A06	J01C-08*07	J02C-08/07	2A4A06		NEGATE BCD CONV(NOT USED)	$C3EXNC
2A4A06	J01C-10/09	2B0B4-P0*P1		6-105	CHL 3 EXTERNAL SUPPRESS A/D	$C3EXSP
2A4A06	J01D-02*01	2B0A0-C1/C0		6- 91	CHL 3 EXT. LINE INTERRUPT 0	$C3EXI0
2A4A06	J01D-04*03	2B0A0-K0/K1		6- 91	CHL 3 EXT. LINE INTERRUPT 1	$C3EXI1
2A4A06	J01D-06*05	2B0A0-P0/P1		6- 91	CHL 3 EXT. LINE INTERRUPT 2	$C3EXI2
2A4A06	J01D-08*07	2B0A0-U0/U1		6- 91	CHL 3 EXT. LINE INTERRUPT 3	$C3EXI3
2A4A06	J01D-10*09	2B0A0-E3/E2		6- 91	CHL 3 EXT. LINE INTERRUPT 4	$C3EXI4
2A4A06	J01E-02*01	2B0A0-J2/J3		6- 91	CHL 3 EXT. LINE INTERRUPT 5	$C3EXI5
2A4A06	J01E-04*03	2B0A0-M2/M3		6- 91	CHL 3 EXT. LINE INTERRUPT 6	$C3EXI6
2A4A06	J01E-06*05	2B0A0-R2/R3		6- 91	CHL 3 EXT. LINE INTERRUPT 7	$C3EXI7
2A4A06	J01E-08/07	2B0B4-T1*T0		6-105	CHL 3 EXTERNAL CLEAR INTERRUPT	$C3EXCI
2A4A06	J01E-10*09	2B0B4-W0/W1		6-105	NOT CHAN 3 EXT INTERRUPT LOCKOUT OVERRIDE	$C3EXOV

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A06	J01F-08*07	J02F-08/07	2A4A06		NOT USED	$C3EXSS
2A4A06	J02A-02*01	2B0A0-F0/F1		6- 91	CHL 3 EXTERNAL STATUS BIT 00	$C3ES00
2A4A06	J02A-04*03	2B0A0-J1/J0		6- 91	CHL 3 EXTERNAL STATUS BIT 01	$C3ES01
2A4A06	J02A-06*05	2B0A0-Q0/Q1		6- 91	CHL 3 EXTERNAL STATUS BIT 02	$C3ES02
2A4A06	J02A-08*07	2B0A0-T1/T0		6- 91	CHL 3 EXTERNAL STATUS BIT 03	$C3ES03
2A4A06	J02A-10*09	2B0A0-C3/C2		6- 91	CHL 3 EXTERNAL STATUS BIT 04	$C3ES04
2A4A06	J02B-02*01	2B0A0-I2/I3		6- 91	CHL 3 EXTERNAL STATUS BIT 05	$C3ES05
2A4A06	J02B-04*03	2B0A0-L2/L3		6- 91	CHL 3 EXTERNAL STATUS BIT 06	$C3ES06
2A4A06	J02B-06*05	2B0A0-S2/S3		6- 91	CHL 3 EXTERNAL STATUS BIT 07	$C3ES07
2A4A06	J02B-08*07	2B0A0-X0/X1		6- 91	CHL 3 EXTERNAL STATUS BIT 08	$C3ES08
2A4A06	J02B-10*09	2B0A0-W3/W2		6- 91	CHL 3 EXTERNAL STATUS BIT 09	$C3ES09
2A4A06	J02C-02*01	2B0A0-T2/T3		6- 91	CHL 3 EXTERNAL STATUS BIT 10	$C3ES10
2A4A06	J02C-04*03	2B0A0-U2/U3		6- 91	CHL 3 EXTERNAL STATUS BIT 11	$C3ES11
2A4A06	J02C-06/05	2B0A0-H2*H3		6- 91	CHAN 3 EXT CMPTR RUNNING	$C3EXRN
2A4A06	J02C-08/07	J01C-08*07	2A4A06		NEGATE BCD CONV(NOT USED)	$C3EXNC
2A4A06	J02C-10/09	2B0B4-P0*P1		6-105	CHL 3 EXTERNAL SUPPRESS A/D	$C3EXSP
2A4A06	J02D-02*01	2B0A0-C1/C0		6- 91	CHL 3 EXT. LINE INTERRUPT 0	$C3EXI0
2A4A06	J02D-04*03	2B0A0-K0/K1		6- 91	CHL 3 EXT. LINE INTERRUPT 1	$C3EXI1
2A4A06	J02D-06*05	2B0A0-P0/P1		6- 91	CHL 3 EXT. LINE INTERRUPT 2	$C3EXI2
2A4A06	J02D-08*07	2B0A0-U0/U1		6- 91	CHL 3 EXT. LINE INTERRUPT 3	$C3EXI3
2A4A06	J02D-10*09	2B0A0-E3/E2		6- 91	CHL 3 EXT. LINE INTERRUPT 4	$C3EXI4
2A4A06	J02E-02*01	2B0A0-J2/J3		6- 91	CHL 3 EXT. LINE INTERRUPT 5	$C3EXI5
2A4A06	J02E-04*03	2B0A0-M2/M3		6- 91	CHL 3 EXT. LINE INTERRUPT 6	$C3EXI6
2A4A06	J02E-06*05	2B0A0-R2/R3		6- 91	CHL 3 EXT. LINE INTERRUPT 7	$C3EXI7
2A4A06	J02E-08/07	2B0B4-T1*T0		6-105	CHL 3 EXTERNAL CLEAR INTERRUPT	$C3EXCI
2A4A06	J02E-10*09	2B0B4-W0/W1		6-105	NOT CHAN 3 EXT INTERRUPT LOCKOUT OVERRIDE	$C3EXOV
2A4A06	J02F-08/07	J01F-08*07	2A4A06		NOT USED	$C3EXSS
2A4A06	J03A-02*01	2B0A1-F0/F1		6- 89	CHL 2 EXTERNAL STATUS BIT 00	$C2ES00
2A4A06	J03A-04*03	2B0A1-J1/J0		6- 89	CHL 2 EXTERNAL STATUS BIT 01	$C2ES01
2A4A06	J03A-06*05	2B0A1-Q0/Q1		6- 89	CHL 2 EXTERNAL STATUS BIT 02	$C2ES02
2A4A06	J03A-08*07	2B0A1-T1/T0		6- 89	CHL 2 EXTERNAL STATUS BIT 03	$C2ES03
2A4A06	J03A-10*09	2B0A1-C3/C2		6- 89	CHL 2 EXTERNAL STATUS BIT 04	$C2ES04
2A4A06	J03B-02*01	2B0A1-I2/I3		6- 89	CHL 2 EXTERNAL STATUS BIT 05	$C2ES05
2A4A06	J03B-04*03	2B0A1-L2/L3		6- 89	CHL 2 EXTERNAL STATUS BIT 06	$C2ES06
2A4A06	J03B-06*05	2B0A1-S2/S3		6- 89	CHL 2 EXTERNAL STATUS BIT 07	$C2ES07
2A4A06	J03B-08*07	2B0A1-X0/X1		6- 89	CHL 2 EXTERNAL STATUS BIT 08	$C2ES08
2A4A06	J03B-10*09	2B0A1-W3/W2		6- 89	CHL 2 EXTERNAL STATUS BIT 09	$C2ES09
2A4A06	J03C-02*01	2B0A1-T2/T3		6- 89	CHL 2 EXTERNAL STATUS BIT 10	$C2ES10
2A4A06	J03C-04*03	2B0A1-U2/U3		6- 89	CHL 2 EXTERNAL STATUS BIT 11	$C2ES11
2A4A06	J03C-06/05	2B0A1-H2*H3		6- 89	CHAN 2 EXT COMPUTER RUNNING	$C2EXRN
2A4A06	J03C-08*07	J04C-08/07	2A4A06		NEGATE BCD CONV(NOT USED)	$C2EXNC
2A4A06	J03C-10/09	2B0B4-D1*D0		6-105	CHL 2 EXTERNAL SUPPRESS A/D	$C2EXSP
2A4A06	J03D-02*01	2B0A1-C1/C0		6- 89	CHL 2 EXT. LINE INTERRUPT 0	$C2EXI0
2A4A06	J03D-04*03	2B0A1-K0/K1		6- 89	CHL 2 EXT. LINE INTERRUPT 1	$C2EXI1
2A4A06	J03D-06*05	2B0A1-P0/P1		6- 89	CHL 2 EXT. LINE INTERRUPT 2	$C2EXI2
2A4A06	J03D-08*07	2B0A1-U0/U1		6- 89	CHL 2 EXT. LINE INTERRUPT 3	$C2EXI3
2A4A06	J03D-10*09	2B0A1-E3/E2		6- 89	CHL 2 EXT. LINE INTERRUPT 4	$C2EXI4
2A4A06	J03E-02*01	2B0A1-J2/J3		6- 89	CHL 2 EXT. LINE INTERRUPT 5	$C2EXI5
2A4A06	J03E-04*03	2B0A1-M2/M3		6- 89	CHL 2 EXT. LINE INTERRUPT 6	$C2EXI6
2A4A06	J03E-06*05	2B0A1-R2/R3		6- 89	CHL 2 EXT. LINE INTERRUPT 7	$C2EXI7
2A4A06	J03E-08/07	2B0B4-C1*C0		6-105	CHL 2 EXTERNAL CLEAR INTERRUPT	$C2EXCI
2A4A06	J03E-10*09	2B0B4-M0/M1		6-105	NOT CHAN 2 EXT INTERRUPT LOCKOUT OVERRIDE	$C2EXOV
2A4A06	J03F-08*07	J04F-08/07	2A4A06		NOT USED	$C2EXSS
2A4A06	J04A-02*01	2B0A1-F0/F1		6- 89	CHL 2 EXTERNAL STATUS BIT 00	$C2ES00
2A4A06	J04A-04*03	2B0A1-J1/J0		6- 89	CHL 2 EXTERNAL STATUS BIT 01	$C2ES01
2A4A06	J04A-06*05	2B0A1-Q0/Q1		6- 89	CHL 2 EXTERNAL STATUS BIT 02	$C2ES02
2A4A06	J04A-08*07	2B0A1-T1/T0		6- 89	CHL 2 EXTERNAL STATUS BIT 03	$C2ES03
2A4A06	J04A-10*09	2B0A1-C3/C2		6- 89	CHL 2 EXTERNAL STATUS BIT 04	$C2ES04
2A4A06	J04B-02*01	2B0A1-I2/I3		6- 89	CHL 2 EXTERNAL STATUS BIT 05	$C2ES05
2A4A06	J04B-04*03	2B0A1-L2/L3		6- 89	CHL 2 EXTERNAL STATUS BIT 06	$C2ES06
2A4A06	J04B-06*05	2B0A1-S2/S3		6- 89	CHL 2 EXTERNAL STATUS BIT 07	$C2ES07
2A4A06	J04B-08*07	2B0A1-X0/X1		6- 89	CHL 2 EXTERNAL STATUS BIT 08	$C2ES08
2A4A06	J04B-10*09	2B0A1-W3/W2		6- 89	CHL 2 EXTERNAL STATUS BIT 09	$C2ES09
2A4A06	J04C-02*01	2B0A1-T2/T3		6- 89	CHL 2 EXTERNAL STATUS BIT 10	$C2ES10
2A4A06	J04C-04*03	2B0A1-U2/U3		6- 89	CHL 2 EXTERNAL STATUS BIT 11	$C2ES11
2A4A06	J04C-06/05	2B0A1-H2*H3		6- 89	CHAN 2 EXT COMPUTER RUNNING	$C2EXRN
2A4A06	J04C-08/07	J03C-08*07	2A4A06		NEGATE BCD CONV(NOT USED)	$C2EXNC

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A06	J04C-10/09	2B0B4-D1*D0		6-105	CHL 2 EXTERNAL SUPPRESS A/D	$C2EXSP
2A4A06	J04D-02*01	2B0A1-C1/C0		6- 89	CHL 2 EXT. LINE INTERRUPT 0	$C2EXI0
2A4A06	J04D-04*03	2B0A1-K0/K1		6- 89	CHL 2 EXT. LINE INTERRUPT 1	$C2EXI1
2A4A06	J04D-06*05	2B0A1-P0/P1		6- 89	CHL 2 EXT. LINE INTERRUPT 2	$C2EXI2
2A4A06	J04D-08*07	2B0A1-U0/U1		6- 89	CHL 2 EXT. LINE INTERRUPT 3	$C2EXI3
2A4A06	J04D-10*09	2B0A1-E3/E2		6- 89	CHL 2 EXT. LINE INTERRUPT 4	$C2EXI4
2A4A06	J04E-02*01	2B0A1-J2/J3		6- 89	CHL 2 EXT. LINE INTERRUPT 5	$C2EXI5
2A4A06	J04E-04*03	2B0A1-M2/M3		6- 89	CHL 2 EXT. LINE INTERRUPT 6	$C2EXI6
2A4A06	J04E-06*05	2B0A1-R2/R3		6- 89	CHL 2 EXT. LINE INTERRUPT 7	$C2EXI7
2A4A06	J04E-08/07	2B0B4-C1*C0		6-105	CHL 2 EXTERNAL CLEAR INTERRUPT	$C2EXCI
2A4A06	J04E-10*09	2B0B4-M0/M1		6-105	NOT CHAN 2 EXT INTERRUPT LOCKOUT OVERRIDE	$C2EXOV
2A4A06	J04F-08/07	J03F-08*07	2A4A06		NOT USED	$C2EXSS
2A4A07	J01A-02*01	2B0B2-F0/F1		6- 95	CHL 5 EXTERNAL STATUS BIT 00	$C5ES00
2A4A07	J01A-04*03	2B0B2-J1/J0		6- 95	CHL 5 EXTERNAL STATUS BIT 01	$C5ES01
2A4A07	J01A-06*05	2B0B2-Q0/Q1		6- 95	CHL 5 EXTERNAL STATUS BIT 02	$C5ES02
2A4A07	J01A-08*07	2B0B2-T1/T0		6- 95	CHL 5 EXTERNAL STATUS BIT 03	$C5ES03
2A4A07	J01A-10*09	2B0B2-C3/C2		6- 95	CHL 5 EXTERNAL STATUS BIT 04	$C5ES04
2A4A07	J01B-02*01	2B0B2-I2/I3		6- 95	CHL 5 EXTERNAL STATUS BIT 05	$C5ES05
2A4A07	J01B-04*03	2B0B2-L2/L3		6- 95	CHL 5 EXTERNAL STATUS BIT 06	$C5ES06
2A4A07	J01B-06*05	2B0B2-S2/S3		6- 95	CHL 5 EXTERNAL STATUS BIT 07	$C5ES07
2A4A07	J01B-08*07	2B0B2-X0/X1		6- 95	CHL 5 EXTERNAL STATUS BIT 08	$C5ES08
2A4A07	J01B-10*09	2B0B2-W3/W2		6- 95	CHL 5 EXTERNAL STATUS BIT 09	$C5ES09
2A4A07	J01C-02*01	2B0B2-T2/T3		6- 95	CHL 5 EXTERNAL STATUS BIT 10	$C5ES10
2A4A07	J01C-04*03	2B0B2-U2/U3		6- 95	CHL 5 EXTERNAL STATUS BIT 11	$C5ES11
2A4A07	J01C-06/05	2B0B2-H2*H3		6- 95	CHAN 5 EXTERNAL CMPTR RUNNING	$C5EXRN
2A4A07	J01C-08*07	J02C-08/07	2A4A07		NEGATE BCD CONV(NOT USED)	$C5EXNC
2A4A07	J01C-10/09	2B0A4-S3*S2		6-103	CHL 5 EXTERNAL SUPPRESS A/D	$C5EXSP
2A4A07	J01D-02*01	2B0B2-C1/C0		6- 95	CHL 5 EXT. LINE INTERRUPT 0	$C5EXI0
2A4A07	J01D-04*03	2B0B2-K0/K1		6- 95	CHL 5 EXT. LINE INTERRUPT 1	$C5EXI1
2A4A07	J01D-06*05	2B0B2-P0/P1		6- 95	CHL 5 EXT. LINE INTERRUPT 2	$C5EXI2
2A4A07	J01D-08*07	2B0B2-U0/U1		6- 95	CHL 5 EXT. LINE INTERRUPT 3	$C5EXI3
2A4A07	J01D-10*09	2B0B2-E3/E2		6- 95	CHL 5 EXT. LINE INTERRUPT 4	$C5EXI4
2A4A07	J01E-02*01	2B0B2-J2/J3		6- 95	CHL 5 EXT. LINE INTERRUPT 5	$C5EXI5
2A4A07	J01E-04*03	2B0B2-M2/M3		6- 95	CHL 5 EXT. LINE INTERRUPT 6	$C5EXI6
2A4A07	J01E-06*05	2B0B2-R2/R3		6- 95	CHL 5 EXT. LINE INTERRUPT 7	$C5EXI7
2A4A07	J01E-08/07	2B0A4-T3*T2		6-103	CHL 5 EXTERNAL CLEAR INTERRUPT	$C5EXCI
2A4A07	J01E-10*09	2B0A4-W3/W2		6-103	NOT CHAN 5 EXT INTERRUPT LOCKOUT OVERRIDE	$C5EXOV
2A4A07	J01F-08*07	J02F-08/07	2A4A07		NOT USED	$C5EXSS
2A4A07	J02A-02*01	2B0B2-F0/F1		6- 95	CHL 5 EXTERNAL STATUS BIT 00	$C5ES00
2A4A07	J02A-04*03	2B0B2-J1/J0		6- 95	CHL 5 EXTERNAL STATUS BIT 01	$C5ES01
2A4A07	J02A-06*05	2B0B2-Q0/Q1		6- 95	CHL 5 EXTERNAL STATUS BIT 02	$C5ES02
2A4A07	J02A-08*07	2B0B2-T1/T0		6- 95	CHL 5 EXTERNAL STATUS BIT 03	$C5ES03
2A4A07	J02A-10*09	2B0B2-C3/C2		6- 95	CHL 5 EXTERNAL STATUS BIT 04	$C5ES04
2A4A07	J02B-02*01	2B0B2-I2/I3		6- 95	CHL 5 EXTERNAL STATUS BIT 05	$C5ES05
2A4A07	J02B-04*03	2B0B2-L2/L3		6- 95	CHL 5 EXTERNAL STATUS BIT 06	$C5ES06
2A4A07	J02B-06*05	2B0B2-S2/S3		6- 95	CHL 5 EXTERNAL STATUS BIT 07	$C5ES07
2A4A07	J02B-08*07	2B0B2-X0/X1		6- 95	CHL 5 EXTERNAL STATUS BIT 08	$C5ES08
2A4A07	J02B-10*09	2B0B2-W3/W2		6- 95	CHL 5 EXTERNAL STATUS BIT 09	$C5ES09
2A4A07	J02C-02*01	2B0B2-T2/T3		6- 95	CHL 5 EXTERNAL STATUS BIT 10	$C5ES10
2A4A07	J02C-04*03	2B0B2-U2/U3		6- 95	CHL 5 EXTERNAL STATUS BIT 11	$C5ES11
2A4A07	J02C-06/05	2B0B2-H2*H3		6- 95	CHAN 5 EXTERNAL CMPTR RUNNING	$C5EXRN
2A4A07	J02C-08/07	J01C-08*07	2A4A07		NEGATE BCD CONV(NOT USED)	$C5EXNC
2A4A07	J02C-10/09	2B0A4-S3*S2		6-103	CHL 5 EXTERNAL SUPPRESS A/D	$C5EXSP
2A4A07	J02D-02*01	2B0B2-C1/C0		6- 95	CHL 5 EXT. LINE INTERRUPT 0	$C5EXI0
2A4A07	J02D-04*03	2B0B2-K0/K1		6- 95	CHL 5 EXT. LINE INTERRUPT 1	$C5EXI1
2A4A07	J02D-06*05	2B0B2-P0/P1		6- 95	CHL 5 EXT. LINE INTERRUPT 2	$C5EXI2
2A4A07	J02D-08*07	2B0B2-U0/U1		6- 95	CHL 5 EXT. LINE INTERRUPT 3	$C5EXI3
2A4A07	J02D-10*09	2B0B2-E3/E2		6- 95	CHL 5 EXT. LINE INTERRUPT 4	$C5EXI4
2A4A07	J02E-02*01	2B0B2-J2/J3		6- 95	CHL 5 EXT. LINE INTERRUPT 5	$C5EXI5
2A4A07	J02E-04*03	2B0B2-M2/M3		6- 95	CHL 5 EXT. LINE INTERRUPT 6	$C5EXI6
2A4A07	J02E-06*05	2B0B2-R2/R3		6- 95	CHL 5 EXT. LINE INTERRUPT 7	$C5EXI7
2A4A07	J02E-08/07	2B0A4-T3*T2		6-103	CHL 5 EXTERNAL CLEAR INTERRUPT	$C5EXCI
2A4A07	J02E-10*09	2B0A4-W3/W2		6-103	NOT CHAN 5 EXT INTERRUPT LOCKOUT OVERRIDE	$C5EXOV
2A4A07	J02F-08/07	J01F-08*07	2A4A07		NOT USED	$C5EXSS
2A4A07	J03A-02*01	2B0B3-F0/F1		6- 93	CHL 4 EXTERNAL STATUS BIT 00	$C4ES00
2A4A07	J03A-04*03	2B0B3-J1/J0		6- 93	CHL 4 EXTERNAL STATUS BIT 01	$C4ES01
2A4A07	J03A-06*05	2B0B3-Q0/Q1		6- 93	CHL 4 EXTERNAL STATUS BIT 02	$C4ES02

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A07	J03A-08*07	2B0B3-T1/T0		6- 93	CHL 4 EXTERNAL STATUS BIT 03	$C4ES03
2A4A07	J03A-10*09	2B0B3-C3/C2		6- 93	CHL 4 EXTERNAL STATUS BIT 04	$C4ES04
2A4A07	J03B-02*01	2B0B3-I2/I3		6- 93	CHL 4 EXTERNAL STATUS BIT 05	$C4ES05
2A4A07	J03B-04*03	2B0B3-L2/L3		6- 93	CHL 4 EXTERNAL STATUS BIT 06	$C4ES06
2A4A07	J03B-06*05	2B0B3-S2/S3		6- 93	CHL 4 EXTERNAL STATUS BIT 07	$C4ES07
2A4A07	J03B-08*07	2B0B3-X0/X1		6- 93	CHL 4 EXTERNAL STATUS BIT 08	$C4ES08
2A4A07	J03B-10*09	2B0B3-W3/W2		6- 93	CHL 4 EXTERNAL STATUS BIT 09	$C4ES09
2A4A07	J03C-02*01	2B0B3-T2/T3		6- 93	CHL 4 EXTERNAL STATUS BIT 10	$C4ES10
2A4A07	J03C-04*03	2B0B3-U2/U3		6- 93	CHL 4 EXTERNAL STATUS BIT 11	$C4ES11
2A4A07	J03C-06/05	2B0B3-H2*H3		6- 93	CHAN 4 EXTERNAL CMPTR RUNNING	$C4EXRN
2A4A07	J03C-08*07	J04C-08/07	2A4A07		NEGATE BCD CONV(NOT USED)	$C4EXNC
2A4A07	J03C-10/09	2B0A4-F3*F2		6-103	CHL 4 EXTERNAL SUPPRESS A/D	$C4EXSP
2A4A07	J03D-02*01	2B0B3-C1/C0		6- 93	CHL 4 EXT. LINE INTERRUPT 0	$C4EXI0
2A4A07	J03D-04*03	2B0B3-K0/K1		6- 93	CHL 4 EXT. LINE INTERRUPT 1	$C4EXI1
2A4A07	J03D-06*05	2B0B3-P0/P1		6- 93	CHL 4 EXT. LINE INTERRUPT 2	$C4EXI2
2A4A07	J03D-08*07	2B0B3-U0/U1		6- 93	CHL 4 EXT. LINE INTERRUPT 3	$C4EXI3
2A4A07	J03D-10*09	2B0B3-F3/E2		6- 93	CHL 4 EXT. LINE INTERRUPT 4	$C4EXI4
2A4A07	J03E-02*01	2B0B3-J2/J3		6- 93	CHL 4 EXT. LINE INTERRUPT 5	$C4EXI5
2A4A07	J03E-04*03	2B0B3-M2/M3		6- 93	CHL 4 EXT. LINE INTERRUPT 6	$C4EXI6
2A4A07	J03E-06*05	2B0B3-R2/R3		6- 93	CHL 4 EXT. LINE INTERRUPT 7	$C4EXI7
2A4A07	J03E-08/07	2B0A4-C3*C2		6-103	CHL 4 EXTERNAL CLEAR INTERRUPT	$C4EXCI
2A4A07	J03E-10*09	2B0A4-N3/N2		6-103	NOT CHAN 4 EXT INTERRUPT LOCKOUT OVERRIDE	$C4EXOV
2A4A07	J03F-08*07	J04F-08/07	2A4A07		NOT USED	$C4EXSS
2A4A07	J04A-02*01	2B0B3-F0/F1		6- 93	CHL 4 EXTERNAL STATUS BIT 00	$C4ES00
2A4A07	J04A-04*03	2B0B3-J1/J0		6- 93	CHL 4 EXTERNAL STATUS BIT 01	$C4ES01
2A4A07	J04A-06*05	2B0B3-Q0/Q1		6- 93	CHL 4 EXTERNAL STATUS BIT 02	$C4ES02
2A4A07	J04A-08*07	2B0B3-T1/T0		6- 93	CHL 4 EXTERNAL STATUS BIT 03	$C4ES03
2A4A07	J04A-10*09	2B0B3-C3/C2		6- 93	CHL 4 EXTERNAL STATUS BIT 04	$C4ES04
2A4A07	J04B-02*01	2B0B3-I2/I3		6- 93	CHL 4 EXTERNAL STATUS BIT 05	$C4ES05
2A4A07	J04B-04*03	2B0B3-L2/L3		6- 93	CHL 4 EXTERNAL STATUS BIT 06	$C4ES06
2A4A07	J04B-06*05	2B0B3-S2/S3		6- 93	CHL 4 EXTERNAL STATUS BIT 07	$C4ES07
2A4A07	J04B-08*07	2B0B3-X0/X1		6- 93	CHL 4 EXTERNAL STATUS BIT 08	$C4ES08
2A4A07	J04B-10*09	2B0B3-W3/W2		6- 93	CHL 4 EXTERNAL STATUS BIT 09	$C4ES09
2A4A07	J04C-02*01	2B0B3-T2/T3		6- 93	CHL 4 EXTERNAL STATUS BIT 10	$C4ES10
2A4A07	J04C-04*03	2B0B3-U2/U3		6- 93	CHL 4 EXTERNAL STATUS BIT 11	$C4ES11
2A4A07	J04C-06/05	2B0B3-H2*H3		6- 93	CHAN 4 EXTERNAL CMPTR RUNNING	$C4EXRN
2A4A07	J04C-08/07	J03C-08*07	2A4A07		NEGATE BCD CONV(NOT USED)	$C4EXNC
2A4A07	J04C-10/09	2B0A4-F3*F2		6-103	CHL 4 EXTERNAL SUPPRESS A/D	$C4EXSP
2A4A07	J04D-02*01	2B0B3-C1/C0		6- 93	CHL 4 EXT. LINE INTERRUPT 0	$C4EXI0
2A4A07	J04D-04*03	2B0B3-K0/K1		6- 93	CHL 4 EXT. LINE INTERRUPT 1	$C4EXI1
2A4A07	J04D-06*05	2B0B3-P0/P1		6- 93	CHL 4 EXT. LINE INTERRUPT 2	$C4EXI2
2A4A07	J04D-08*07	2B0B3-U0/U1		6- 93	CHL 4 EXT. LINE INTERRUPT 3	$C4EXI3
2A4A07	J04D-10*09	2B0B3-E3/E2		6- 93	CHL 4 EXT. LINE INTERRUPT 4	$C4EXI4
2A4A07	J04E-02*01	2B0B3-J2/J3		6- 93	CHL 4 EXT. LINE INTERRUPT 5	$C4EXI5
2A4A07	J04E-04*03	2B0B3-M2/M3		6- 93	CHL 4 EXT. LINE INTERRUPT 6	$C4EXI6
2A4A07	J04E-06*05	2B0B3-R2/R3		6- 93	CHL 4 EXT. LINE INTERRUPT 7	$C4EXI7
2A4A07	J04E-08/07	2B0A4-C3*C2		6-103	CHL 4 EXTERNAL CLEAR INTERRUPT	$C4EXCI
2A4A07	J04E-10*09	2B0A4-N3/N2		6-103	NOT CHAN 4 EXT INTERRUPT LOCKOUT OVERRIDE	$C4EXOV
2A4A07	J04F-08/07	J03F-08*07	2A4A07		NOT USED	$C4EXSS
2A4A08	J01A-02*01	2B0B0-F0/F1		6- 99	CHL 7 EXTERNAL STATUS BIT 00	$C7ES00
2A4A08	J01A-04*03	2B0B0-J1/J0		6- 99	CHL 7 EXTERNAL STATUS BIT 01	$C7ES01
2A4A08	J01A-06*05	2B0B0-Q0/Q1		6- 99	CHL 7 EXTERNAL STATUS BIT 02	$C7ES02
2A4A08	J01A-08*07	2B0B0-T1/T0		6- 99	CHL 7 EXTERNAL STATUS BIT 03	$C7ES03
2A4A08	J01A-10*09	2B0B0-C3/C2		6- 99	CHL 7 EXTERNAL STATUS BIT 04	$C7ES04
2A4A08	J01B-02*01	2B0B0-I2/I3		6- 99	CHL 7 EXTERNAL STATUS BIT 05	$C7ES05
2A4A08	J01B-04*03	2B0B0-L2/L3		6- 99	CHL 7 EXTERNAL STATUS BIT 06	$C7ES06
2A4A08	J01B-06*05	2B0B0-S2/S3		6- 99	CHL 7 EXTERNAL STATUS BIT 07	$C7ES07
2A4A08	J01B-08*07	2B0B0-X0/X1		6- 99	CHL 7 EXTERNAL STATUS BIT 08	$C7ES08
2A4A08	J01B-10*09	2B0B0-W3/W2		6- 99	CHL 7 EXTERNAL STATUS BIT 09	$C7ES09
2A4A08	J01C-02*01	2B0B0-T2/T3		6- 99	CHL 7 EXTERNAL STATUS BIT 10	$C7ES10
2A4A08	J01C-04*03	2B0B0-U2/U3		6- 99	CHL 7 EXTERNAL STATUS BIT 11	$C7ES11
2A4A08	J01C-06/05	2B0B0-H2*H3		6- 99	CHAN 7 EXTERNAL CMPTR RUNNING	$C7EXRN
2A4A08	J01C-08*07	J02C-08/07	2A4A08		NEGATE BCD CONV(NOT USED)	$C7EXNC
2A4A08	J01C-10/09	2B0B4-S3*S2		6-105	CHL 7 EXTERNAL SUPPRESS A/D	$C7EXSP
2A4A08	J01D-02*01	2B0B0-C1/C0		6- 99	CHL 7 EXT. LINE INTERRUPT 0	$C7EXI0
2A4A08	J01D-04*03	2B0B0-K0/K1		6- 99	CHL 7 EXT. LINE INTERRUPT 1	$C7EXI1
2A4A08	J01D-06*05	2B0B0-P0/P1		6- 99	CHL 7 EXT. LINE INTERRUPT 2	$C7EXI2
2A4A08	J01D-08*07	2B0B0-U0/U1		6- 99	CHL 7 EXT. LINE INTERRUPT 3	$C7EXI3
2A4A08	J01D-10*09	2B0B0-E3/E2		6- 99	CHL 7 EXT. LINE INTERRUPT 4	$C7EXI4
2A4A08	J01E-02*01	2B0B0-J2/J3		6- 99	CHL 7 EXT. LINE INTERRUPT 5	$C7EXI5

431

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A08	J01E-04*03	2B0B0-M2/M3		6- 99	CHL 7 EXT. LINE INTERRUPT 6	$C7EXI6
2A4A08	J01E-06*05	2B0B0-R2/R3		6- 99	CHL 7 EXT. LINE INTERRUPT 7	$C7EXI7
2A4A08	J01E-08/07	2B0B4-T3*T2		6-105	CHL 7 EXTERNAL CLEAR INTERRUPT	$C7EXCI
2A4A08	J01E-10*09	2B0B4-W3/W2		6-105	NOT CHAN 7 EXT INTERRUPT LOCKOUT OVERRIDE	$C7EXOV
2A4A08	J01F-08*07	J02F-08/07	2A4A08		NOT USED	$C7EXSS
2A4A08	J02A-02*01	2B0B0-F0/F1		6- 99	CHL 7 EXTERNAL STATUS BIT 00	$C7ES00
2A4A08	J02A-04*03	2B0B0-J1/J0		6- 99	CHL 7 EXTERNAL STATUS BIT 01	$C7ES01
2A4A08	J02A-06*05	2B0B0-Q0/Q1		6- 99	CHL 7 EXTERNAL STATUS BIT 02	$C7ES02
2A4A08	J02A-08*07	2B0B0-T1/T0		6- 99	CHL 7 EXTERNAL STATUS BIT 03	$C7ES03
2A4A08	J02A-10*09	2B0B0-C3/C2		6- 99	CHL 7 EXTERNAL STATUS BIT 04	$C7ES04
2A4A08	J02B-02*01	2B0B0-I2/I3		6- 99	CHL 7 EXTERNAL STATUS BIT 05	$C7ES05
2A4A08	J02B-04*03	2B0B0-L2/L3		6- 99	CHL 7 EXTERNAL STATUS BIT 06	$C7ES06
2A4A08	J02B-06*05	2B0B0-S2/S3		6- 99	CHL 7 EXTERNAL STATUS BIT 07	$C7ES07
2A4A08	J02B-08*07	2B0B0-X0/X1		6- 99	CHL 7 EXTERNAL STATUS BIT 08	$C7ES08
2A4A08	J02B-10*09	2B0B0-W3/W2		6- 99	CHL 7 EXTERNAL STATUS BIT 09	$C7ES09
2A4A08	J02C-02*01	2B0B0-T2/T3		6- 99	CHL 7 EXTERNAL STATUS BIT 10	$C7ES10
2A4A08	J02C-04*03	2B0B0-U2/U3		6- 99	CHL 7 EXTERNAL STATUS BIT 11	$C7ES11
2A4A08	J02C-06/05	2B0B0-H2*H3		6- 99	CHAN 7 EXTERNAL CMPTR RUNNING	$C7EXRN
2A4A08	J02C-08/07	J01C-08*07	2A4A08		NEGATE BCD CONV(NOT USED)	$C7EXNC
2A4A08	J02C-10/09	2B0B4-S3*S2		6-105	CHL 7 EXTERNAL SUPPRESS A/D	$C7EXSP
2A4A08	J02D-02*01	2B0B0-C1/C0		6- 99	CHL 7 EXT. LINE INTERRUPT 0	$C7EXI0
2A4A08	J02D-04*03	2B0B0-K0/K1		6- 99	CHL 7 EXT. LINE INTERRUPT 1	$C7EXI1
2A4A08	J02D-06*05	2B0B0-P0/P1		6- 99	CHL 7 EXT. LINE INTERRUPT 2	$C7EXI2
2A4A08	J02D-08*07	2B0B0-U0/U1		6- 99	CHL 7 EXT. LINE INTERRUPT 3	$C7EXI3
2A4A08	J02D-10*09	2B0B0-E3/E2		6- 99	CHL 7 EXT. LINE INTERRUPT 4	$C7EXI4
2A4A08	J02E-02*01	2B0B0-J2/J3		6- 99	CHL 7 EXT. LINE INTERRUPT 5	$C7EXI5
2A4A08	J02E-04*03	2B0B0-M2/M3		6- 99	CHL 7 EXT. LINE INTERRUPT 6	$C7EXI6
2A4A08	J02E-06*05	2B0B0-R2/R3		6- 99	CHL 7 EXT. LINE INTERRUPT 7	$C7EXI7
2A4A08	J02E-08/07	2B0B4-T3*T2		6-105	CHL 7 EXTERNAL CLEAR INTERRUPT	$C7EXCI
2A4A08	J02E-10*09	2B0B4-W3/W2		6-105	NOT CHAN 7 EXT INTERRUPT LOCKOUT OVERRIDE	$C7EXOV
2A4A08	J02F-08/07	J01F-08*07	2A4A08		NOT USED	$C7EXSS
2A4A08	J03A-02*01	2B0B1-F0/F1		6- 97	CHL 6 EXTERNAL STATUS BIT 00	$C6ES00
2A4A08	J03A-04*03	2B0B1-J1/J0		6- 97	CHL 6 EXTERNAL STATUS BIT 01	$C6ES01
2A4A08	J03A-06*05	2B0B1-Q0/Q1		6- 97	CHL 6 EXTERNAL STATUS BIT 02	$C6ES02
2A4A08	J03A-08*07	2B0B1-T1/T0		6- 97	CHL 6 EXTERNAL STATUS BIT 03	$C6ES03
2A4A08	J03A-10*09	2B0B1-C3/C2		6- 97	CHL 6 EXTERNAL STATUS BIT 04	$C6ES04
2A4A08	J03B-02*01	2B0B1-I2/I3		6- 97	CHL 6 EXTERNAL STATUS BIT 05	$C6ES05
2A4A08	J03B-04*03	2B0B1-L2/L3		6- 97	CHL 6 EXTERNAL STATUS BIT 06	$C6ES06
2A4A08	J03B-06*05	2B0B1-S2/S3		6- 97	CHL 6 EXTERNAL STATUS BIT 07	$C6ES07
2A4A08	J03B-08*07	2B0B1-X0/X1		6- 97	CHL 6 EXTERNAL STATUS BIT 08	$C6ES08
2A4A08	J03B-10*09	2B0B1-W3/W2		6- 97	CHL 6 EXTERNAL STATUS BIT 09	$C6ES09
2A4A08	J03C-02*01	2B0B1-T2/T3		6- 97	CHL 6 EXTERNAL STATUS BIT 10	$C6ES10
2A4A08	J03C-04*03	2B0B1-U2/U3		6- 97	CHL 6 EXTERNAL STATUS BIT 11	$C6ES11
2A4A08	J03C-06/05	2B0B1-H2*H3		6- 97	CHAN 6 EXTERNAL CMPTR RUNNING	$C6EXRN
2A4A08	J03C-08/07	J04C-08/07	2A4A08		NEGATE BCD CONV(NOT USED)	$C6EXNC
2A4A08	J03C-10/09	2B0B4-F3*F2		6-105	CHL 6 EXTERNAL SUPPRESS A/D	$C6EXSP
2A4A08	J03D-02*01	2B0B1-C1/C0		6- 97	CHL 6 EXT. LINE INTERRUPT 0	$C6EXI0
2A4A08	J03D-04*03	2B0B1-K0/K1		6- 97	CHL 6 EXT. LINE INTERRUPT 1	$C6EXI1
2A4A08	J03D-06*05	2B0B1-P0/P1		6- 97	CHL 6 EXT. LINE INTERRUPT 2	$C6EXI2
2A4A08	J03D-08*07	2B0B1-U0/U1		6- 97	CHL 6 EXT. LINE INTERRUPT 3	$C6EXI3
2A4A08	J03D-10*09	2B0B1-E3/E2		6- 97	CHL 6 EXT. LINE INTERRUPT 4	$C6EXI4
2A4A08	J03E-02*01	2B0B1-J2/J3		6- 97	CHL 6 EXT. LINE INTERRUPT 5	$C6EXI5
2A4A08	J03E-04*03	2B0B1-M2/M3		6- 97	CHL 6 EXT. LINE INTERRUPT 6	$C6EXI6
2A4A08	J03E-06*05	2B0B1-R2/R3		6- 97	CHL 6 EXT. LINE INTERRUPT 7	$C6EXI7
2A4A08	J03E-08/07	2B0B4-C3*C2		6-105	CHL 6 EXTERNAL CLEAR INTERRUPT	$C6EXCI
2A4A08	J03E-10*09	2B0B4-N3/N2		6-105	NOT CHAN 6 EXT INTERRUPT LOCKOUT OVERRIDE	$C6EXOV
2A4A08	J03F-08*07	J04F-08/07	2A4A08		NOT USED	$C6EXSS
2A4A08	J04A-02*01	2B0B1-F0/F1		6- 97	CHL 6 EXTERNAL STATUS BIT 00	$C6ES00
2A4A08	J04A-04*03	2B0B1-J1/J0		6- 97	CHL 6 EXTERNAL STATUS BIT 01	$C6ES01
2A4A08	J04A-06*05	2B0B1-Q0/Q1		6- 97	CHL 6 EXTERNAL STATUS BIT 02	$C6ES02
2A4A08	J04A-08*07	2B0B1-T1/T0		6- 97	CHL 6 EXTERNAL STATUS BIT 03	$C6ES03
2A4A08	J04A-10*09	2B0B1-C3/C2		6- 97	CHL 6 EXTERNAL STATUS BIT 04	$C6ES04
2A4A08	J04B-02*01	2B0B1-I2/I3		6- 97	CHL 6 EXTERNAL STATUS BIT 05	$C6ES05
2A4A08	J04B-04*03	2B0B1-L2/L3		6- 97	CHL 6 EXTERNAL STATUS BIT 06	$C6ES06
2A4A08	J04B-06*05	2B0B1-S2/S3		6- 97	CHL 6 EXTERNAL STATUS BIT 07	$C6ES07
2A4A08	J04B-08*07	2B0B1-X0/X1		6- 97	CHL 6 EXTERNAL STATUS BIT 08	$C6ES08
2A4A08	J04B-10*09	2B0B1-W3/W2		6- 97	CHL 6 EXTERNAL STATUS BIT 09	$C6ES09
2A4A08	J04C-02*01	2B0B1-T2/T3		6- 97	CHL 6 EXTERNAL STATUS BIT 10	$C6ES10
2A4A08	J04C-04*03	2B0B1-U2/U3		6- 97	CHL 6 EXTERNAL STATUS BIT 11	$C6ES11
2A4A08	J04C-06/05	2B0B1-H2*H3		6- 97	CHAN 6 EXTERNAL CMPTR RUNNING	$C6EXRN
2A4A08	J04C-08/07	J03C-08*07	2A4A08		NEGATE BCD CONV(NOT USED)	$C6EXNC
2A4A08	J04C-10/09	2B0B4-F3*F2		6-105	CHL 6 EXTERNAL SUPPRESS A/D	$C6EXSP
2A4A08	J04D-02*01	2B0B1-C1/C0		6- 97	CHL 6 EXT. LINE INTERRUPT 0	$C6EXI0
2A4A08	J04D-04*03	2B0B1-K0/K1		6- 97	CHL 6 EXT. LINE INTERRUPT 1	$C6EXI1
2A4A08	J04D-06*05	2B0B1-P0/P1		6- 97	CHL 6 EXT. LINE INTERRUPT 2	$C6EXI2
2A4A08	J04D-08*07	2B0B1-U0/U1		6- 97	CHL 6 EXT. LINE INTERRUPT 3	$C6EXI3
2A4A08	J04D-10*09	2B0B1-E3/E2		6- 97	CHL 6 EXT. LINE INTERRUPT 4	$C6EXI4
2A4A08	J04E-02*01	2B0B1-J2/J3		6- 97	CHL 6 EXT. LINE INTERRUPT 5	$C6EXI5
2A4A08	J04E-04*03	2B0B1-M2/M3		6- 97	CHL 6 EXT. LINE INTERRUPT 6	$C6EXI6
2A4A08	J04E-06*05	2B0B1-R2/R3		6- 97	CHL 6 EXT. LINE INTERRUPT 7	$C6EXI7
2A4A08	J04E-08/07	2B0B4-C3*C2		6-105	CHL 6 EXTERNAL CLEAR INTERRUPT	$C6EXCI
2A4A08	J04E-10*09	2B0B4-N3/N2		6-105	NOT CHAN 6 EXT INTERRUPT LOCKOUT OVERRIDE	$C6EXOV
2A4A08	J04F-08/07	J03F-08*07	2A4A08		NOT USED	$C6EXSS
2A4A09	J01A-02/01	2C0A9-E0*E1		6-179	CHANNEL 4 EXTERNAL DATA BIT 12	$C4EX12
2A4A09	J01A-04/03	2C0A9-I0*I1		6-179	CHANNEL 4 EXTERNAL DATA BIT 13	$C4EX13
2A4A09	J01A-06/05	2C0A9-M1*M0		6-179	CHANNEL 4 EXTERNAL DATA BIT 14	$C4EX14
2A4A09	J01A-08/07	2C0A9-N0*N1		6-179	CHANNEL 4 EXTERNAL DATA BIT 15	$C4EX15
2A4A09	J01A-10/09	2C0A9-S0*S1		6-179	CHANNEL 4 EXTERNAL DATA BIT 16	$C4EX16
2A4A09	J01B-02/01	2C0A9-W0*W1		6-179	CHANNEL 4 EXTERNAL DATA BIT 17	$C4EX17
2A4A09	J01B-04/03	2C0A9-B2*B3		6-179	CHANNEL 4 EXTERNAL DATA BIT 18	$C4EX18
2A4A09	J01B-06/05	2C0A9-G2*G3		6-179	CHANNEL 4 EXTERNAL DATA BIT 19	$C4EX19
2A4A09	J01B-08/07	2C0A9-M2*M3		6-179	CHANNEL 4 EXTERNAL DATA BIT 20	$C4EX20
2A4A09	J01B-10/09	2C0A9-K3*K2		6-179	CHANNEL 4 EXTERNAL DATA BIT 21	$C4EX21
2A4A09	J01C-02/01	2C0A9-Q3*Q2		6-179	CHANNEL 4 EXTERNAL DATA BIT 22	$C4EX22
2A4A09	J01C-04/03	2C0A9-W2*W3		6-179	CHANNEL 4 EXTERNAL DATA BIT 23	$C4EX23
2A4A09	J01C-06/05	2C0A9-U3*U2		6-179	CHL 4 EXTERNAL PARITY BIT 2	$C4EXP2
2A4A09	J01C-08*07	2C0B7-X0/X1		6-169	CHL 4 EXT 24 BIT DEVICE CONNTD	$C4EX24
2A4A09	J01C-10/09	J02C-10*09	2A4A09		NOT USED	$C4EJ00
2A4A09	J01D-02/01	J02D-02*01	2A4A09		NOT USED	$C4EJ01
2A4A09	J01D-04/03	J02D-04*03	2A4A09		NOT USED	$C4EJ02
2A4A09	J01D-06/05	J02D-06*05	2A4A09		NOT USED	$C4EJ03
2A4A09	J01D-08/07	J02D-08*07	2A4A09		NOT USED	$C4EJ04
2A4A09	J01D-10/09	J02D-10*09	2A4A09		NOT USED	$C4EJ05
2A4A09	J01E-02/01	J02E-02*01	2A4A09		NOT USED	$C4EJ06
2A4A09	J01E-04/03	J02E-04*03	2A4A09		NOT USED	$C4EJ07
2A4A09	J01E-06/05	J02E-06*05	2A4A09		NOT USED	$C4EJ08
2A4A09	J01E-08/07	J02E-08*07	2A4A09		NOT USED	$C4EJ09
2A4A09	J01E-10/09	J02E-10*09	2A4A09		NOT USED	$C4EJ10
2A4A09	J01F-02/01	J02F-02*01	2A4A09		NOT USED	$C4EJ11
2A4A09	J01F-04/03	J02F-04*03	2A4A09		NOT USED	$C4EJ12
2A4A09	J01F-06/05	J02F-06*05	2A4A09		NOT USED	$C4EJ13
2A4A09	J01F-08/07	J02F-08*07	2A4A09		NOT USED	$C4EJ14
2A4A09	J02A-02/01	2C0A9-F0*F1		6-179	CHANNEL 4 EXTERNAL DATA BIT 12	$C4EX12
2A4A09	J02A-04/03	2C0A9-J0*J1		6-179	CHANNEL 4 EXTERNAL DATA BIT 13	$C4EX13
2A4A09	J02A-06/05	2C0A9-L1*L0		6-179	CHANNEL 4 EXTERNAL DATA BIT 14	$C4EX14
2A4A09	J02A-08/07	2C0A9-Q0*Q1		6-179	CHANNEL 4 EXTERNAL DATA BIT 15	$C4EX15
2A4A09	J02A-10/09	2C0A9-T0*T1		6-179	CHANNEL 4 EXTERNAL DATA BIT 16	$C4EX16
2A4A09	J02B-02/01	2C0A9-X0*X1		6-179	CHANNEL 4 EXTERNAL DATA BIT 17	$C4EX17
2A4A09	J02B-04/03	2C0A9-C2*C3		6-179	CHANNEL 4 EXTERNAL DATA BIT 18	$C4EX18
2A4A09	J02B-06/05	2C0A9-H2*H3		6-179	CHANNEL 4 EXTERNAL DATA BIT 19	$C4EX19
2A4A09	J02B-08/07	2C0A9-N2*N3		6-179	CHANNEL 4 EXTERNAL DATA BIT 20	$C4EX20
2A4A09	J02B-10/09	2C0A9-L3*L2		6-179	CHANNEL 4 EXTERNAL DATA BIT 21	$C4EX21
2A4A09	J02C-02/01	2C0A9-R3*R2		6-179	CHANNEL 4 EXTERNAL DATA BIT 22	$C4EX22
2A4A09	J02C-04/03	2C0A9-X2*X3		6-179	CHANNEL 4 EXTERNAL DATA BIT 23	$C4EX23
2A4A09	J02C-06/05	2C0A9-V3*V2		6-179	CHL 4 EXTERNAL PARITY BIT 2	$C4EXP2
2A4A09	J02C-08*07	2C0B7-X0/X1		6-169	CHL 4 EXT 24 BIT DEVICE CONNTD	$C4EX24
2A4A09	J02C-10*09	J01C-10/09	2A4A09		NOT USED	$C4EJ00
2A4A09	J02D-02*01	J01D-02/01	2A4A09		NOT USED	$C4EJ01
2A4A09	J02D-04*03	J01D-04/03	2A4A09		NOT USED	$C4EJ02
2A4A09	J02D-06*05	J01D-06/05	2A4A09		NOT USED	$C4EJ03
2A4A09	J02D-08*07	J01D-08/07	2A4A09		NOT USED	$C4EJ04
2A4A09	J02D-10*09	J01D-10/09	2A4A09		NOT USED	$C4EJ05
2A4A09	J02E-02*01	J01E-02/01	2A4A09		NOT USED	$C4EJ06
2A4A09	J02E-04*03	J01E-04/03	2A4A09		NOT USED	$C4EJ07
2A4A09	J02E-06*05	J01E-06/05	2A4A09		NOT USED	$C4EJ08
2A4A09	J02E-08*07	J01E-08/07	2A4A09		NOT USED	$C4EJ09
2A4A09	J02E-10*09	J01E-10/09	2A4A09		NOT USED	$C4EJ10
2A4A09	J02F-02*01	J01F-02/01	2A4A09		NOT USED	$C4EJ11
2A4A09	J02F-04*03	J01F-04/03	2A4A09		NOT USED	$C4EJ12

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A09	J02F-06*05	J01F-06/05	2A4A09		NOT USED	$C4EJ13
2A4A09	J02F-08*07	J01F-08/07	2A4A09		NOT USED	$C4EJ14
2A4A09	J03A-02/01	2C0B9-E0*E1		6-177	CHANNEL 4 EXTERNAL DATA BIT 00	$C4EX00
2A4A09	J03A-04/03	2C0B9-I0*I1		6-177	CHANNEL 4 EXTERNAL DATA BIT 01	$C4EX01
2A4A09	J03A-06/05	2C0B9-M1*M0		6-177	CHANNEL 4 EXTERNAL DATA BIT 02	$C4EX02
2A4A09	J03A-08/07	2C0B9-N0*N1		6-177	CHANNEL 4 EXTERNAL DATA BIT 03	$C4EX03
2A4A09	J03A-10/09	2C0B9-S0*S1		6-177	CHANNEL 4 EXTERNAL DATA BIT 04	$C4EX04
2A4A09	J03B-02/01	2C0B9-W0*W1		6-177	CHANNEL 4 EXTERNAL DATA BIT 05	$C4EX05
2A4A09	J03B-04/03	2C0B9-B2*B3		6-177	CHANNEL 4 EXTERNAL DATA BIT 06	$C4EX06
2A4A09	J03B-06/05	2C0B9-G2*G3		6-177	CHANNEL 4 EXTERNAL DATA BIT 07	$C4EX07
2A4A09	J03B-08/07	2C0B9-M2*M3		6-177	CHANNEL 4 EXTERNAL DATA BIT 08	$C4EX08
2A4A09	J03B-10/09	2C0B9-K3*K2		6-177	CHANNEL 4 EXTERNAL DATA BIT 09	$C4EX09
2A4A09	J03C-02/01	2C0B9-Q3*Q2		6-177	CHANNEL 4 EXTERNAL DATA BIT 10	$C4EX10
2A4A09	J03C-04/03	2C0B9-W2*W3		6-177	CHANNEL 4 EXTERNAL DATA BIT 11	$C4EX11
2A4A09	J03C-06/05	2C0B9-U3*U2		6-177	CHL 4 EXTERNAL PARITY BIT 1	$C4EXP1
2A4A09	J03C-08/07	2C0A7-R2*R3		6-161	CHL 4 EXTERNAL BUSY SIGNAL	$C4EXRW
2A4A09	J03C-10/09	J04C-10*09	2A4A09		NOT USED	$C4EXRA
2A4A09	J03D-02/01	2C0A7-X0*X1		6-161	CHL 4 EXTERNAL READ SIGNAL	$C4EXRD
2A4A09	J03D-04/03	2C0A7-T1*T0		6-161	CHL 4 EXTERNAL WRITE SIGNAL	$C4EXWR
2A4A09	J03D-06/05	2C0A7-I3*I2		6-161	CHL 4 EXTERNAL CONNECT SIGNAL	$C4EXCN
2A4A09	J03D-08/07	2C0A7-F2*F3		6-161	CHL 4 EXTERNAL SELECT SIGNAL	$C4EXSL
2A4A09	J03D-10/09	2C0B7-C3*C2		6-169	CHL 4 EXTERNAL DATA SIGNAL	$C4EXDS
2A4A09	J03E-02*01	2C0B7-J2/J3		6-169	CHL 4 EXTERNAL REPLY SIGNAL	$C4EXRP
2A4A09	J03E-04*03	2C0A7-E3/E2		6-161	CHL 4 EXTERNAL REJECT SIGNAL	$C4EXRJ
2A4A09	J03E-06*05	2C0B7-I3/I2		6-169	CHL 4 EXTERNAL REJECT SIGNAL	$C4EXER
2A4A09	J03E-08*07	2C0A7-N2/N3		6-161	CHL 4 EXTERNAL PARITY ERROR	$C4EXPE
2A4A09	J03E-10/09	J04E-10*09	2A4A09		NOT USED	$C4EJA0
2A4A09	J03F-02/01	2C0B7-W0*W1		6-169	CHL 4 EXTERNAL WORD MARK	$C4EXWM
2A4A09	J03F-04/03	2C0A7-01*00		6-161	CHL 4 CLEAR TO EXTERNAL EQUIP	$C4EXCL
2A4A09	J03F-06/05	J04F-06*05	2A4A09		NOT USED	$C4EJA1
2A4A09	J03F-08/07	J04F-08*07	2A4A09		NOT USED	$C4EJA2
2A4A09	J04A-02/01	2C0B9-F0*F1		6-177	CHANNEL 4 EXTERNAL DATA BIT 00	$C4EX00
2A4A09	J04A-04/03	2C0B9-J0*J1		6-177	CHANNEL 4 EXTERNAL DATA BIT 01	$C4EX01
2A4A09	J04A-06/05	2C0B9-L1*L0		6-177	CHANNEL 4 EXTERNAL DATA BIT 02	$C4EX02
2A4A09	J04A-08/07	2C0B9-00*01		6-177	CHANNEL 4 EXTERNAL DATA BIT 03	$C4EX03
2A4A09	J04A-10/09	2C0B9-T0*T1		6-177	CHANNEL 4 EXTERNAL DATA BIT 04	$C4EX04
2A4A09	J04B-02/01	2C0B9-X0*X1		6-177	CHANNEL 4 EXTERNAL DATA BIT 05	$C4EX05
2A4A09	J04B-04/03	2C0B9-C2*C3		6-177	CHANNEL 4 EXTERNAL DATA BIT 06	$C4EX06
2A4A09	J04B-06/05	2C0B9-H2*H3		6-177	CHANNEL 4 EXTERNAL DATA BIT 07	$C4EX07
2A4A09	J04B-08/07	2C0B9-N2*N3		6-177	CHANNEL 4 EXTERNAL DATA BIT 08	$C4EX08
2A4A09	J04B-10/09	2C0B9-L3*L2		6-177	CHANNEL 4 EXTERNAL DATA BIT 09	$C4EX09
2A4A09	J04C-02/01	2C0B9-R3*R2		6-177	CHANNEL 4 EXTERNAL DATA BIT 10	$C4EX10
2A4A09	J04C-04/03	2C0B9-X2*X3		6-177	CHANNEL 4 EXTERNAL DATA BIT 11	$C4EX11
2A4A09	J04C-06/05	2C0B9-V3*V2		6-177	CHL 4 EXTERNAL PARITY BIT 1	$C4EXP1
2A4A09	J04C-08/07	2C0A7-R2*R3		6-161	CHL 4 EXTERNAL BUSY SIGNAL	$C4EXRW
2A4A09	J04C-10*09	J03C-10/09	2A4A09		NOT USED	$C4EXRA
2A4A09	J04D-02/01	2C0A7-X0*X1		6-161	CHL 4 EXTERNAL READ SIGNAL	$C4EXRD
2A4A09	J04D-04/03	2C0A7-T1*T0		6-161	CHL 4 EXTERNAL WRITE SIGNAL	$C4EXWR
2A4A09	J04D-06/05	2C0A7-I3*I2		6-161	CHL 4 EXTERNAL CONNECT SIGNAL	$C4EXCN
2A4A09	J04D-08/07	2C0A7-F2*F3		6-161	CHL 4 EXTERNAL SELECT SIGNAL	$C4EXSL
2A4A09	J04D-10/09	2C0B7-C3*C2		6-169	CHL 4 EXTERNAL DATA SIGNAL	$C4EXDS
2A4A09	J04E-02*01	2C0B7-J2/J3		6-169	CHL 4 EXTERNAL REPLY SIGNAL	$C4EXRP
2A4A09	J04E-04*03	2C0A7-E3/E2		6-161	CHL 4 EXTERNAL REJECT SIGNAL	$C4EXRJ
2A4A09	J04E-06*05	2C0B7-I3/I2		6-169	CHL 4 EXTERNAL REJECT SIGNAL	$C4EXER
2A4A09	J04E-08*07	2C0A7-N2/N3		6-161	CHL 4 EXTERNAL PARITY ERROR	$C4EXPE
2A4A09	J04E-10*09	J03E-10/09	2A4A09		NOT USED	$C4EJA0
2A4A09	J04F-02/01	2C0B7-W0*W1		6-169	CHL 4 EXTERNAL WORD MARK	$C4EXWM
2A4A09	J04F-04/03	2C0A7-01*00		6-161	CHL 4 CLEAR TO EXTERNAL EQUIP	$C4EXCL
2A4A09	J04F-06*05	J03F-06/05	2A4A09		NOT USED	$C4EJA1
2A4A09	J04F-08*07	J03F-08/07	2A4A09		NOT USED	$C4EJA2
2A4A10	J01A-02/01	2C0A8-E0*E1		6-183	CHANNEL 5 EXTERNAL DATA BIT 12	$C5EX12
2A4A10	J01A-04/03	2C0A8-I0*I1		6-183	CHANNEL 5 EXTERNAL DATA BIT 13	$C5EX13
2A4A10	J01A-06/05	2C0A8-M1*M0		6-183	CHANNEL 5 EXTERNAL DATA BIT 14	$C5EX14
2A4A10	J01A-08/07	2C0A8-N0*N1		6-183	CHANNEL 5 EXTERNAL DATA BIT 15	$C5EX15
2A4A10	J01A-10/09	2C0A8-S0*S1		6-183	CHANNEL 5 EXTERNAL DATA BIT 16	$C5EX16
2A4A10	J01B-02/01	2C0A8-W0*W1		6-183	CHANNEL 5 EXTERNAL DATA BIT 17	$C5EX17
2A4A10	J01B-04/03	2C0A8-B2*B3		6-183	CHANNEL 5 EXTERNAL DATA BIT 18	$C5EX18
2A4A10	J01B-06/05	2C0A8-G2*G3		6-183	CHANNEL 5 EXTERNAL DATA BIT 19	$C5EX19
2A4A10	J01B-08/07	2C0A8-M2*M3		6-183	CHANNEL 5 EXTERNAL DATA BIT 20	$C5EX20
2A4A10	J01B-10/09	2C0A8-K3*K2		6-183	CHANNEL 5 EXTERNAL DATA BIT 21	$C5EX21
2A4A10	J01C-02/01	2C0A8-Q3*Q2		6-183	CHANNEL 5 EXTERNAL DATA BIT 22	$C5EX22
2A4A10	J01C-04/03	2C0A8-W2*W3		6-183	CHANNEL 5 EXTERNAL DATA BIT 23	$C5EX23
2A4A10	J01C-06/05	2C0A8-U3*U2		6-183	CHL 5 EXTERNAL PARITY BIT 2	$C5EXP2

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A10	J01C-08*07	2C0B6-X0/X1		6-171	CHL 5 EXT 24 BIT DEVICE CONNTD	$C5EX24
2A4A10	J01C-10/09	J02C-10*09	2A4A10		NOT USED	$C5EJ00
2A4A10	J01D-02/01	J02D-02*01	2A4A10		NOT USED	$C5EJ01
2A4A10	J01D-04/03	J02D-04*03	2A4A10		NOT USED	$C5EJ02
2A4A10	J01D-06/05	J02D-06*05	2A4A10		NOT USED	$C5EJ03
2A4A10	J01D-08/07	J02D-08*07	2A4A10		NOT USED	$C5EJ04
2A4A10	J01D-10/09	J02D-10*09	2A4A10		NOT USED	$C5EJ05
2A4A10	J01E-02/01	J02E-02*01	2A4A10		NOT USED	$C5EJ06
2A4A10	J01E-04/03	J02E-04*03	2A4A10		NOT USED	$C5EJ07
2A4A10	J01E-06/05	J02E-06*05	2A4A10		NOT USED	$C5EJ08
2A4A10	J01E-08/07	J02E-08*07	2A4A10		NOT USED	$C5EJ09
2A4A10	J01E-10/09	J02E-10*09	2A4A10		NOT USED	$C5EJ10
2A4A10	J01F-02/01	J02F-02*01	2A4A10		NOT USED	$C5EJ11
2A4A10	J01F-04/03	J02F-04*03	2A4A10		NOT USED	$C5EJ12
2A4A10	J01F-06/05	J02F-06*05	2A4A10		NOT USED	$C5EJ13
2A4A10	J01F-08/07	J02F-08*07	2A4A10		NOT USED	$C5EJ14
2A4A10	J02A-02/01	2C0A8-F0*F1		6-183	CHANNEL 5 EXTERNAL DATA BIT 12	$C5EX12
2A4A10	J02A-04/03	2C0A8-J0*J1		6-183	CHANNEL 5 EXTERNAL DATA BIT 13	$C5EX13
2A4A10	J02A-06/05	2C0A8-L1*L0		6-183	CHANNEL 5 EXTERNAL DATA BIT 14	$C5EX14
2A4A10	J02A-08/07	2C0A8-00*01		6-183	CHANNEL 5 EXTERNAL DATA BIT 15	$C5EX15
2A4A10	J02A-10/09	2C0A8-T0*T1		6-183	CHANNEL 5 EXTERNAL DATA BIT 16	$C5EX16
2A4A10	J02B-02/01	2C0A8-X0*X1		6-183	CHANNEL 5 EXTERNAL DATA BIT 17	$C5EX17
2A4A10	J02B-04/03	2C0A8-C2*C3		6-183	CHANNEL 5 EXTERNAL DATA BIT 18	$C5EX18
2A4A10	J02B-06/05	2C0A8-H2*H3		6-183	CHANNEL 5 EXTERNAL DATA BIT 19	$C5EX19
2A4A10	J02B-08/07	2C0A8-N2*N3		6-183	CHANNEL 5 EXTERNAL DATA BIT 20	$C5EX20
2A4A10	J02B-10/09	2C0A8-L3*L2		6-183	CHANNEL 5 EXTERNAL DATA BIT 21	$C5EX21
2A4A10	J02C-02/01	2C0A8-R3*R2		6-183	CHANNEL 5 EXTERNAL DATA BIT 22	$C5EX22
2A4A10	J02C-04/03	2C0A8-X2*X3		6-183	CHANNEL 5 EXTERNAL DATA BIT 23	$C5EX23
2A4A10	J02C-06/05	2C0A8-V3*V2		6-183	CHL 5 EXTERNAL PARITY BIT 2	$C5EXP2
2A4A10	J02C-08*07	2C0B6-X0/X1		6-171	CHL 5 EXT 24 BIT DEVICE CONNTD	$C5EX24
2A4A10	J02C-10*09	J01C-10/09	2A4A10		NOT USED	$C5EJ00
2A4A10	J02D-02*01	J01D-02/01	2A4A10		NOT USED	$C5EJ01
2A4A10	J02D-04*03	J01D-04/03	2A4A10		NOT USED	$C5EJ02
2A4A10	J02D-06*05	J01D-06/05	2A4A10		NOT USED	$C5EJ03
2A4A10	J02D-08*07	J01D-08/07	2A4A10		NOT USED	$C5EJ04
2A4A10	J02D-10*09	J01D-10/09	2A4A10		NOT USED	$C5EJ05
2A4A10	J02E-02*01	J01E-02/01	2A4A10		NOT USED	$C5EJ06
2A4A10	J02E-04*03	J01E-04/03	2A4A10		NOT USED	$C5EJ07
2A4A10	J02E-06*05	J01E-06/05	2A4A10		NOT USED	$C5EJ08
2A4A10	J02E-08*07	J01E-08/07	2A4A10		NOT USED	$C5EJ09
2A4A10	J02E-10*09	J01E-10/09	2A4A10		NOT USED	$C5EJ10
2A4A10	J02F-02*01	J01F-02/01	2A4A10		NOT USED	$C5EJ11
2A4A10	J02F-04*03	J01F-04/03	2A4A10		NOT USED	$C5EJ12
2A4A10	J02F-06*05	J01F-06/05	2A4A10		NOT USED	$C5EJ13
2A4A10	J02F-08*07	J01F-08/07	2A4A10		NOT USED	$C5EJ14
2A4A10	J03A-02/01	2C0B8-E0*E1		6-181	CHANNEL 5 EXTERNAL DATA BIT 00	$C5EX00
2A4A10	J03A-04/03	2C0B8-I0*I1		6-181	CHANNEL 5 EXTERNAL DATA BIT 01	$C5EX01
2A4A10	J03A-06/05	2C0B8-M1*M0		6-181	CHANNEL 5 EXTERNAL DATA BIT 02	$C5EX02
2A4A10	J03A-08/07	2C0B8-N0*N1		6-181	CHANNEL 5 EXTERNAL DATA BIT 03	$C5EX03
2A4A10	J03A-10/09	2C0B8-S0*S1		6-181	CHANNEL 5 EXTERNAL DATA BIT 04	$C5EX04
2A4A10	J03B-02/01	2C0B8-W0*W1		6-181	CHANNEL 5 EXTERNAL DATA BIT 05	$C5EX05
2A4A10	J03B-04/03	2C0B8-B2*B3		6-181	CHANNEL 5 EXTERNAL DATA BIT 06	$C5EX06
2A4A10	J03B-06/05	2C0B8-G2*G3		6-181	CHANNEL 5 EXTERNAL DATA BIT 07	$C5EX07
2A4A10	J03B-08/07	2C0B8-M2*M3		6-181	CHANNEL 5 EXTERNAL DATA BIT 08	$C5EX08
2A4A10	J03B-10/09	2C0B8-K3*K2		6-181	CHANNEL 5 EXTERNAL DATA BIT 09	$C5EX09
2A4A10	J03C-02/01	2C0B8-Q3*Q2		6-181	CHANNEL 5 EXTERNAL DATA BIT 10	$C5EX10
2A4A10	J03C-04/03	2C0B8-W2*W3		6-181	CHANNEL 5 EXTERNAL DATA BIT 11	$C5EX11
2A4A10	J03C-06/05	2C0B8-U3*U2		6-181	CHL 5 EXTERNAL PARITY BIT 1	$C5EXP1
2A4A10	J03C-08/07	2C0A6-R2*R3		6-163	CHL 5 EXTERNAL BUSY SIGNAL	$C5EXRW
2A4A10	J03C-10/09	J04C-10*09	2A4A10		NOT USED	$C5EXRA
2A4A10	J03D-02/01	2C0A6-X0*X1		6-163	CHL 5 EXTERNAL READ SIGNAL	$C5EXRD
2A4A10	J03D-04/03	2C0A6-T1*T0		6-163	CHL 5 EXTERNAL WRITE SIGNAL	$C5EXWR
2A4A10	J03D-06/05	2C0A6-I3*I2		6-163	CHL 5 EXTERNAL CONNECT SIGNAL	$C5EXCN
2A4A10	J03D-08/07	2C0A6-F2*F3		6-163	CHL 5 EXTERNAL SELECT SIGNAL	$C5EXSL
2A4A10	J03D-10/09	2C0B6-C3*C2		6-171	CHL 5 EXTERNAL DATA SIGNAL	$C5EXDS
2A4A10	J03E-02*01	2C0B6-J2/J3		6-171	CHL 5 EXTERNAL REPLY SIGNAL	$C5EXRP
2A4A10	J03E-04*03	2C0A6-E3/E2		6-163	CHL 5 EXTERNAL REJECT SIGNAL	$C5EXRJ
2A4A10	J03E-06*05	2C0B6-I3/I2		6-171	CHL 5 EXTERNAL REJECT SIGNAL	$C5EXER
2A4A10	J03E-08*07	2C0A6-N2/N3		6-163	CHL 5 EXTERNAL PARITY ERROR	$C5EXPE
2A4A10	J03E-10/09	J04E-10*09	2A4A10		NOT USED	$C5EJA0
2A4A10	J03F-02/01	2C0B6-W0*W1		6-171	CHL 5 EXTERNAL WORD MARK	$C5EXWM
2A4A10	J03F-04/03	2C0A6-01*00		6-163	CHL 5 CLEAR TO EXTERNAL EQUIP	$C5EXCL
2A4A10	J03F-06/05	J04F-06*05	2A4A10		NOT USED	$C5EJA1
2A4A10	J03F-08/07	J04F-08*07	2A4A10		NOT USED	$C5EJA2

433

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A10	J04A-02/01	2C0B8-F0*F1		6-181	CHANNEL 5 EXTERNAL DATA BIT 00	$C5EX00
2A4A10	J04A-04/03	2C0B8-J0*J1		6-181	CHANNEL 5 EXTERNAL DATA BIT 01	$C5EX01
2A4A10	J04A-06/05	2C0B8-L1*L0		6-181	CHANNEL 5 EXTERNAL DATA BIT 02	$C5EX02
2A4A10	J04A-08/07	2C0B8-O0*O1		6-181	CHANNEL 5 EXTERNAL DATA BIT 03	$C5EX03
2A4A10	J04A-10/09	2C0B8-T0*T1		6-181	CHANNEL 5 EXTERNAL DATA BIT 04	$C5EX04
2A4A10	J04B-02/01	2C0B8-X0*X1		6-181	CHANNEL 5 EXTERNAL DATA BIT 05	$C5EX05
2A4A10	J04B-04/03	2C0B8-C2*C3		6-181	CHANNEL 5 EXTERNAL DATA BIT 06	$C5EX06
2A4A10	J04B-06/05	2C0B8-H2*H3		6-181	CHANNEL 5 EXTERNAL DATA BIT 07	$C5EX07
2A4A10	J04B-08/07	2C0B8-N2*N3		6-181	CHANNEL 5 EXTERNAL DATA BIT 08	$C5EX08
2A4A10	J04B-10/09	2C0B8-L3*L2		6-181	CHANNEL 5 EXTERNAL DATA BIT 09	$C5EX09
2A4A10	J04C-02/01	2C0B8-R3*R2		6-181	CHANNEL 5 EXTERNAL DATA BIT 10	$C5EX10
2A4A10	J04C-04/03	2C0B8-X2*X3		6-181	CHANNEL 5 EXTERNAL DATA BIT 11	$C5EX11
2A4A10	J04C-06/05	2C0B8-V3*V2		6-181	CHL 5 EXTERNAL PARITY BIT 1	$C5EXP1
2A4A10	J04C-08/07	2C0A6-R2*R3		6-163	CHL 5 EXTERNAL BUSY SIGNAL	$C5EXRW
2A4A10	J04C-10*09	J03C-10/09	2A4A10		NOT USED	$C5EXRA
2A4A10	J04D-02/01	2C0A6-X0*X1		6-163	CHL 5 EXTERNAL READ SIGNAL	$C5EXRD
2A4A10	J04D-04/03	2C0A6-T1*T0		6-163	CHL 5 EXTERNAL WRITE SIGNAL	$C5EXWR
2A4A10	J04D-06/05	2C0A6-I3*I2		6-163	CHL 5 EXTERNAL CONNECT SIGNAL	$C5EXCN
2A4A10	J04D-08/07	2C0A6-F2*F3		6-163	CHL 5 EXTERNAL SELECT SIGNAL	$C5EXSL
2A4A10	J04D-10/09	2C0B6-C3*C2		6-171	CHL 5 EXTERNAL DATA SIGNAL	$C5EXDS
2A4A10	J04E-02*01	2C0B6-J2/J3		6-171	CHL 5 EXTERNAL REPLY SIGNAL	$C5EXRP
2A4A10	J04E-04*03	2C0A6-E3/E2		6-163	CHL 5 EXTERNAL REJECT SIGNAL	$C5EXRJ
2A4A10	J04E-06*05	2C0B6-I3/I2		6-171	CHL 5 EXTERNAL REJECT SIGNAL	$C5EXER
2A4A10	J04E-08*07	2C0A6-N2/N3		6-163	CHL 5 EXTERNAL PARITY ERROR	$C5EXPE
2A4A10	J04E-10*09	J03E-10/09	2A4A10		NOT USED	$C5EJA0
2A4A10	J04F-02/01	2C0B6-W0*W1		6-171	CHL 5 EXTERNAL WORD MARK	$C5EXWM
2A4A10	J04F-04/03	2C0A6-01*00		6-163	CHL 5 CLEAR TO EXTERNAL EQUIP	$C5EXCL
2A4A10	J04F-06*05	J03F-06/05	2A4A10		NOT USED	$C5EJA1
2A4A10	J04F-08*07	J03F-08/07	2A4A10		NOT USED	$C5EJA2
2A4A11	J01A-02/01	2C0A1-E0*E1		6-187	CHANNEL 6 EXTERNAL DATA BIT 12	$C6EX12
2A4A11	J01A-04/03	2C0A1-I0*I1		6-187	CHANNEL 6 EXTERNAL DATA BIT 13	$C6EX13
2A4A11	J01A-06/05	2C0A1-M1*M0		6-187	CHANNEL 6 EXTERNAL DATA BIT 14	$C6EX14
2A4A11	J01A-08/07	2C0A1-N0*N1		6-187	CHANNEL 6 EXTERNAL DATA BIT 15	$C6EX15
2A4A11	J01A-10/09	2C0A1-S0*S1		6-187	CHANNEL 6 EXTERNAL DATA BIT 16	$C6EX16
2A4A11	J01B-02/01	2C0A1-W0*W1		6-187	CHANNEL 6 EXTERNAL DATA BIT 17	$C6EX17
2A4A11	J01B-04/03	2C0A1-B2*B3		6-187	CHANNEL 6 EXTERNAL DATA BIT 18	$C6EX18
2A4A11	J01B-06/05	2C0A1-G2*G3		6-187	CHANNEL 6 EXTERNAL DATA BIT 19	$C6EX19
2A4A11	J01B-08/07	2C0A1-M2*M3		6-187	CHANNEL 6 EXTERNAL DATA BIT 20	$C6EX20
2A4A11	J01B-10/09	2C0A1-K3*K2		6-187	CHANNEL 6 EXTERNAL DATA BIT 21	$C6EX21
2A4A11	J01C-02/01	2C0A1-Q3*Q2		6-187	CHANNEL 6 EXTERNAL DATA BIT 22	$C6EX22
2A4A11	J01C-04/03	2C0A1-W2*W3		6-187	CHANNEL 6 EXTERNAL DATA BIT 23	$C6EX23
2A4A11	J01C-06/05	2C0A1-U3*U2		6-187	CHL 6 EXTERNAL PARITY BIT 2	$C6EXP2
2A4A11	J01C-08*07	2C0B3-X0/X1		6-173	CHL 6 EXT 24 BIT DEVICE CONNTD	$C6EX24
2A4A11	J01C-10/09	J02C-10*09	2A4A11		NOT USED	$C6EJ00
2A4A11	J01D-02/01	J02D-02*01	2A4A11		NOT USED	$C6EJ01
2A4A11	J01D-04/03	J02D-04*03	2A4A11		NOT USED	$C6EJ02
2A4A11	J01D-06/05	J02D-06*05	2A4A11		NOT USED	$C6EJ03
2A4A11	J01D-08/07	J02D-08*07	2A4A11		NOT USED	$C6EJ04
2A4A11	J01D-10/09	J02D-10*09	2A4A11		NOT USED	$C6EJ05
2A4A11	J01E-02/01	J02E-02*01	2A4A11		NOT USED	$C6EJ06
2A4A11	J01E-04/03	J02E-04*03	2A4A11		NOT USED	$C6EJ07
2A4A11	J01E-06/05	J02E-06*05	2A4A11		NOT USED	$C6EJ08
2A4A11	J01E-08/07	J02E-08*07	2A4A11		NOT USED	$C6EJ09
2A4A11	J01E-10/09	J02E-10*09	2A4A11		NOT USED	$C6EJ10
2A4A11	J01F-02/01	J02F-02*01	2A4A11		NOT USED	$C6EJ11
2A4A11	J01F-04/03	J02F-04*03	2A4A11		NOT USED	$C6EJ12
2A4A11	J01F-06/05	J02F-06*05	2A4A11		NOT USED	$C6EJ13
2A4A11	J01F-08/07	J02F-08*07	2A4A11		NOT USED	$C6EJ14
2A4A11	J02A-02/01	2C0A1-F0*F1		6-187	CHANNEL 6 EXTERNAL DATA BIT 12	$C6EX12
2A4A11	J02A-04/03	2C0A1-J0*J1		6-187	CHANNEL 6 EXTERNAL DATA BIT 13	$C6EX13
2A4A11	J02A-06/05	2C0A1-L1*L0		6-187	CHANNEL 6 EXTERNAL DATA BIT 14	$C6EX14
2A4A11	J02A-08/07	2C0A1-O0*O1		6-187	CHANNEL 6 EXTERNAL DATA BIT 15	$C6EX15
2A4A11	J02A-10/09	2C0A1-T0*T1		6-187	CHANNEL 6 EXTERNAL DATA BIT 16	$C6EX16
2A4A11	J02B-02/01	2C0A1-X0*X1		6-187	CHANNEL 6 EXTERNAL DATA BIT 17	$C6EX17
2A4A11	J02B-04/03	2C0A1-C2*C3		6-187	CHANNEL 6 EXTERNAL DATA BIT 18	$C6EX18
2A4A11	J02B-06/05	2C0A1-H2*H3		6-187	CHANNEL 6 EXTERNAL DATA BIT 19	$C6EX19
2A4A11	J02B-08/07	2C0A1-N2*N3		6-187	CHANNEL 6 EXTERNAL DATA BIT 20	$C6EX20
2A4A11	J02B-10/09	2C0A1-L3*L2		6-187	CHANNEL 6 EXTERNAL DATA BIT 21	$C6EX21
2A4A11	J02C-02/01	2C0A1-R3*R2		6-187	CHANNEL 6 EXTERNAL DATA BIT 22	$C6EX22
2A4A11	J02C-04/03	2C0A1-X2*X3		6-187	CHANNEL 6 EXTERNAL DATA BIT 23	$C6EX23
2A4A11	J02C-06/05	2C0A1-V3*V2		6-187	CHL 6 EXTERNAL PARITY BIT 2	$C6EXP2
2A4A11	J02C-08*07	2C0B3-X0/X1		6-173	CHL 6 EXT 24 BIT DEVICE CONNTD	$C6EX24
2A4A11	J02C-10*09	J01C-10/09	2A4A11		NOT USED	$C6EJ00
2A4A11	J02D-02*01	J01D-02/01	2A4A11		NOT USED	$C6EJ01
2A4A11	J02D-04*03	J01D-04/03	2A4A11		NOT USED	$C6EJ02
2A4A11	J02D-06*05	J01D-06/05	2A4A11		NOT USED	$C6EJ03
2A4A11	J02D-08*07	J01D-08/07	2A4A11		NOT USED	$C6EJ04
2A4A11	J02D-10*09	J01D-10/09	2A4A11		NOT USED	$C6EJ05
2A4A11	J02E-02*01	J01E-02/01	2A4A11		NOT USED	$C6EJ06
2A4A11	J02E-04*03	J01E-04/03	2A4A11		NOT USED	$C6EJ07
2A4A11	J02E-06*05	J01E-06/05	2A4A11		NOT USED	$C6EJ08
2A4A11	J02E-08*07	J01E-08/07	2A4A11		NOT USED	$C6EJ09
2A4A11	J02E-10*09	J01E-10/09	2A4A11		NOT USED	$C6EJ10
2A4A11	J02F-02*01	J01F-02/01	2A4A11		NOT USED	$C6EJ11
2A4A11	J02F-04*03	J01F-04/03	2A4A11		NOT USED	$C6EJ12
2A4A11	J02F-06*05	J01F-06/05	2A4A11		NOT USED	$C6EJ13
2A4A11	J02F-08*07	J01F-08/07	2A4A11		NOT USED	$C6EJ14
2A4A11	J03A-02/01	2C0B1-E0*E1		6-185	CHANNEL 6 EXTERNAL DATA BIT 00	$C6EX00
2A4A11	J03A-04/03	2C0B1-I0*I1		6-185	CHANNEL 6 EXTERNAL DATA BIT 01	$C6EX01
2A4A11	J03A-06/05	2C0B1-M1*M0		6-185	CHANNEL 6 EXTERNAL DATA BIT 02	$C6EX02
2A4A11	J03A-08/07	2C0B1-N0*N1		6-185	CHANNEL 6 EXTERNAL DATA BIT 03	$C6EX03
2A4A11	J03A-10/09	2C0B1-S0*S1		6-185	CHANNEL 6 EXTERNAL DATA BIT 04	$C6EX04
2A4A11	J03B-02/01	2C0B1-W0*W1		6-185	CHANNEL 6 EXTERNAL DATA BIT 05	$C6EX05
2A4A11	J03B-04/03	2C0B1-B2*B3		6-185	CHANNEL 6 EXTERNAL DATA BIT 06	$C6EX06
2A4A11	J03B-06/05	2C0B1-G2*G3		6-185	CHANNEL 6 EXTERNAL DATA BIT 07	$C6EX07
2A4A11	J03B-08/07	2C0B1-M2*M3		6-185	CHANNEL 6 EXTERNAL DATA BIT 08	$C6EX08
2A4A11	J03B-10/09	2C0B1-K3*K2		6-185	CHANNEL 6 EXTERNAL DATA BIT 09	$C6EX09
2A4A11	J03C-02/01	2C0B1-Q3*Q2		6-185	CHANNEL 6 EXTERNAL DATA BIT 10	$C6EX10
2A4A11	J03C-04/03	2C0B1-W2*W3		6-185	CHANNEL 6 EXTERNAL DATA BIT 11	$C6EX11
2A4A11	J03C-06/05	2C0B1-U3*U2		6-185	CHL 6 EXTERNAL PARITY BIT 1	$C6EXP1
2A4A11	J03C-08/07	2C0A3-R2*R3		6-165	CHL 6 EXTERNAL BUSY SIGNAL	$C6EXRW
2A4A11	J03C-10/09	J04C-10*09	2A4A11		NOT USED	$C6EXRA
2A4A11	J03D-02/01	2C0A3-X0*X1		6-165	CHL 6 EXTERNAL READ SIGNAL	$C6EXRD
2A4A11	J03D-04/03	2C0A3-T1*T0		6-165	CHL 6 EXTERNAL WRITE SIGNAL	$C6EXWR
2A4A11	J03D-06/05	2C0A3-I3*I2		6-165	CHL 6 EXTERNAL CONNECT SIGNAL	$C6EXCN
2A4A11	J03D-08/07	2C0A3-F2*F3		6-165	CHL 6 EXTERNAL SELECT SIGNAL	$C6EXSL
2A4A11	J03D-10/09	2C0B3-C3*C2		6-173	CHL 6 EXTERNAL DATA SIGNAL	$C6EXDS
2A4A11	J03E-02*01	2C0B3-J2/J3		6-173	CHL 6 EXTERNAL REPLY SIGNAL	$C6EXRP
2A4A11	J03E-04*03	2C0A3-E3/E2		6-165	CHL 6 EXTERNAL REJECT SIGNAL	$C6EXRJ
2A4A11	J03E-06*05	2C0B3-I3/I2		6-173	CHL 6 EXTERNAL REJECT SIGNAL	$C6EXER
2A4A11	J03E-08*07	2C0A3-N2/N3		6-165	CHL 6 EXTERNAL PARITY ERROR	$C6EXPE
2A4A11	J03E-10/09	J04E-10*09	2A4A11		NOT USED	$C6EJA0
2A4A11	J03F-02/01	2C0B3-W0*W1		6-173	CHL 6 EXTERNAL WORD MARK	$C6EXWM
2A4A11	J03F-04/03	2C0A3-01*00		6-165	CHL 6 CLEAR TO EXTERNAL EQUIP	$C6EXCL
2A4A11	J03F-06/05	J04F-06*05	2A4A11		NOT USED	$C6EJA1
2A4A11	J03F-08/07	J04F-08*07	2A4A11		NOT USED	$C6EJA2
2A4A11	J04A-02/01	2C0B1-F0*F1		6-185	CHANNEL 6 EXTERNAL DATA BIT 00	$C6EX00
2A4A11	J04A-04/03	2C0B1-J0*J1		6-185	CHANNEL 6 EXTERNAL DATA BIT 01	$C6EX01
2A4A11	J04A-06/05	2C0B1-L1*L0		6-185	CHANNEL 6 EXTERNAL DATA BIT 02	$C6EX02
2A4A11	J04A-08/07	2C0B1-O0*O1		6-185	CHANNEL 6 EXTERNAL DATA BIT 03	$C6EX03
2A4A11	J04A-10/09	2C0B1-T0*T1		6-185	CHANNEL 6 EXTERNAL DATA BIT 04	$C6EX04
2A4A11	J04B-02/01	2C0B1-X0*X1		6-185	CHANNEL 6 EXTERNAL DATA BIT 05	$C6EX05
2A4A11	J04B-04/03	2C0B1-C2*C3		6-185	CHANNEL 6 EXTERNAL DATA BIT 06	$C6EX06
2A4A11	J04B-06/05	2C0B1-H2*H3		6-185	CHANNEL 6 EXTERNAL DATA BIT 07	$C6EX07
2A4A11	J04B-08/07	2C0B1-N2*N3		6-185	CHANNEL 6 EXTERNAL DATA BIT 08	$C6EX08
2A4A11	J04B-10/09	2C0B1-L3*L2		6-185	CHANNEL 6 EXTERNAL DATA BIT 09	$C6EX09
2A4A11	J04C-02/01	2C0B1-R3*R2		6-185	CHANNEL 6 EXTERNAL DATA BIT 10	$C6EX10
2A4A11	J04C-04/03	2C0B1-X2*X3		6-185	CHANNEL 6 EXTERNAL DATA BIT 11	$C6EX11
2A4A11	J04C-06/05	2C0B1-V3*V2		6-185	CHL 6 EXTERNAL PARITY BIT 1	$C6EXP1
2A4A11	J04C-08/07	2C0A3-R2*R3		6-165	CHL 6 EXTERNAL BUSY SIGNAL	$C6EXRW
2A4A11	J04C-10*09	J03C-10/09	2A4A11		NOT USED	$C6EXRA
2A4A11	J04D-02/01	2C0A3-X0*X1		6-165	CHL 6 EXTERNAL READ SIGNAL	$C6EXRD
2A4A11	J04D-04/03	2C0A3-T1*T0		6-165	CHL 6 EXTERNAL WRITE SIGNAL	$C6EXWR
2A4A11	J04D-06/05	2C0A3-I3*I2		6-165	CHL 6 EXTERNAL CONNECT SIGNAL	$C6EXCN
2A4A11	J04D-08/07	2C0A3-F2*F3		6-165	CHL 6 EXTERNAL SELECT SIGNAL	$C6EXSL
2A4A11	J04D-10/09	2C0B3-C3*C2		6-173	CHL 6 EXTERNAL DATA SIGNAL	$C6EXDS
2A4A11	J04E-02*01	2C0B3-J2/J3		6-173	CHL 6 EXTERNAL REPLY SIGNAL	$C6EXRP
2A4A11	J04E-04*03	2C0A3-E3/E2		6-165	CHL 6 EXTERNAL REJECT SIGNAL	$C6EXRJ
2A4A11	J04E-06*05	2C0B3-I3/I2		6-173	CHL 6 EXTERNAL REJECT SIGNAL	$C6EXER
2A4A11	J04E-08*07	2C0A3-N2/N3		6-165	CHL 6 EXTERNAL PARITY ERROR	$C6EXPE
2A4A11	J04E-10*09	J03E-10/09	2A4A11		NOT USED	$C6EJA0
2A4A11	J04F-02/01	2C0B3-W0*W1		6-173	CHL 6 EXTERNAL WORD MARK	$C6EXWM
2A4A11	J04F-04/03	2C0A3-01*00		6-165	CHL 6 CLEAR TO EXTERNAL EQUIP	$C6EXCL
2A4A11	J04F-06*05	J03F-06/05	2A4A11		NOT USED	$C6EJA1
2A4A11	J04F-08*07	J03F-08/07	2A4A11		NOT USED	$C6EJA2
2A4A12	J01A-02/01	2C0A0-E0*E1		6-191	CHANNEL 7 EXTERNAL DATA BIT 12	$C7EX12

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A12	J01A-04/03	2C0A0-I0*I1		6-191	CHANNEL 7 EXTERNAL DATA BIT 13	$C7EX13
2A4A12	J01A-06/05	2C0A0-M1*M0		6-191	CHANNEL 7 EXTERNAL DATA BIT 14	$C7EX14
2A4A12	J01A-08/07	2C0A0-N0*N1		6-191	CHANNEL 7 EXTERNAL DATA BIT 15	$C7EX15
2A4A12	J01A-10/09	2C0A0-S0*S1		6-191	CHANNEL 7 EXTERNAL DATA BIT 16	$C7EX16
2A4A12	J01B-02/01	2C0A0-W0*W1		6-191	CHANNEL 7 EXTERNAL DATA BIT 17	$C7EX17
2A4A12	J01B-04/03	2C0A0-B2*B3		6-191	CHANNEL 7 EXTERNAL DATA BIT 18	$C7EX18
2A4A12	J01B-06/05	2C0A0-G2*G3		6-191	CHANNEL 7 EXTERNAL DATA BIT 19	$C7EX19
2A4A12	J01B-08/07	2C0A0-M2*M3		6-191	CHANNEL 7 EXTERNAL DATA BIT 20	$C7EX20
2A4A12	J01B-10/09	2C0A0-K3*K2		6-191	CHANNEL 7 EXTERNAL DATA BIT 21	$C7EX21
2A4A12	J01C-02/01	2C0A0-Q3*Q2		6-191	CHANNEL 7 EXTERNAL DATA BIT 22	$C7EX22
2A4A12	J01C-04/03	2C0A0-W2*W3		6-191	CHANNEL 7 EXTERNAL DATA BIT 23	$C7EX23
2A4A12	J01C-06/05	2C0A0-U3*U2		6-191	CHL 7 EXTERNAL PARITY BIT 2	$C7EXP2
2A4A12	J01C-08*07	2C0B2-X0/X1		6-175	CHL 7 EXT 24 BIT DEVICE CONNTD	$C7EX24
2A4A12	J01C-10/09	J02C-10*09	2A4A12		NOT USED	$C7EJ00
2A4A12	J01D-02/01	J02D-02*01	2A4A12		NOT USED	$C7EJ01
2A4A12	J01D-04/03	J02D-04*03	2A4A12		NOT USED	$C7EJ02
2A4A12	J01D-06/05	J02D-06*05	2A4A12		NOT USED	$C7EJ03
2A4A12	J01D-08/07	J02D-08*07	2A4A12		NOT USED	$C7EJ04
2A4A12	J01D-10/09	J02D-10*09	2A4A12		NOT USED	$C7EJ05
2A4A12	J01E-02/01	J02E-02*01	2A4A12		NOT USED	$C7EJ06
2A4A12	J01E-04/03	J02E-04*03	2A4A12		NOT USED	$C7EJ07
2A4A12	J01E-06/05	J02E-06*05	2A4A12		NOT USED	$C7EJ08
2A4A12	J01E-08/07	J02E-08*07	2A4A12		NOT USED	$C7EJ09
2A4A12	J01E-10/09	J02E-10*09	2A4A12		NOT USED	$C7EJ10
2A4A12	J01F-02/01	J02F-02*01	2A4A12		NOT USED	$C7EJ11
2A4A12	J01F-04/03	J02F-04*03	2A4A12		NOT USED	$C7EJ12
2A4A12	J01F-06/05	J02F-06*05	2A4A12		NOT USED	$C7EJ13
2A4A12	J01F-08/07	J02F-08*07	2A4A12		NOT USED	$C7EJ14
2A4A12	J02A-02/01	2C0A0-F0*F1		6-191	CHANNEL 7 EXTERNAL DATA BIT 12	$C7EX12
2A4A12	J02A-04/03	2C0A0-J0*J1		6-191	CHANNEL 7 EXTERNAL DATA BIT 13	$C7EX13
2A4A12	J02A-06/05	2C0A0-L1*L0		6-191	CHANNEL 7 EXTERNAL DATA BIT 14	$C7EX14
2A4A12	J02A-08/07	2C0A0-O0*O1		6-191	CHANNEL 7 EXTERNAL DATA BIT 15	$C7EX15
2A4A12	J02A-10/09	2C0A0-T0*T1		6-191	CHANNEL 7 EXTERNAL DATA BIT 16	$C7EX16
2A4A12	J02B-02/01	2C0A0-X0*X1		6-191	CHANNEL 7 EXTERNAL DATA BIT 17	$C7EX17
2A4A12	J02B-04/03	2C0A0-C2*C3		6-191	CHANNEL 7 EXTERNAL DATA BIT 18	$C7EX18
2A4A12	J02B-06/05	2C0A0-H2*H3		6-191	CHANNEL 7 EXTERNAL DATA BIT 19	$C7EX19
2A4A12	J02B-08/07	2C0A0-N2*N3		6-191	CHANNEL 7 EXTERNAL DATA BIT 20	$C7EX20
2A4A12	J02B-10/09	2C0A0-L3*L2		6-191	CHANNEL 7 EXTERNAL DATA BIT 21	$C7EX21
2A4A12	J02C-02/01	2C0A0-R3*R2		6-191	CHANNEL 7 EXTERNAL DATA BIT 22	$C7EX22
2A4A12	J02C-04/03	2C0A0-X2*X3		6-191	CHANNEL 7 EXTERNAL DATA BIT 23	$C7EX23
2A4A12	J02C-06/05	2C0A0-V3*V2		6-191	CHL 7 EXTERNAL PARITY BIT 2	$C7EXP2
2A4A12	J02C-08*07	2C0B2-X0/X1		6-175	CHL 7 EXT 24 BIT DEVICE CONNTD	$C7EX24
2A4A12	J02C-10*09	J01C-10/09	2A4A12		NOT USED	$C7EJ00
2A4A12	J02D-02*01	J01D-02/01	2A4A12		NOT USED	$C7EJ01
2A4A12	J02D-04*03	J01D-04/03	2A4A12		NOT USED	$C7EJ02
2A4A12	J02D-06*05	J01D-06/05	2A4A12		NOT USED	$C7EJ03
2A4A12	J02D-08*07	J01D-08/07	2A4A12		NOT USED	$C7EJ04
2A4A12	J02D-10*09	J01D-10/09	2A4A12		NOT USED	$C7EJ05
2A4A12	J02E-02*01	J01E-02/01	2A4A12		NOT USED	$C7EJ06
2A4A12	J02E-04*03	J01E-04/03	2A4A12		NOT USED	$C7EJ07
2A4A12	J02E-06*05	J01E-06/05	2A4A12		NOT USED	$C7EJ08
2A4A12	J02E-08*07	J01E-08/07	2A4A12		NOT USED	$C7EJ09
2A4A12	J02E-10*09	J01E-10/09	2A4A12		NOT USED	$C7EJ10
2A4A12	J02F-02*01	J01F-02/01	2A4A12		NOT USED	$C7EJ11
2A4A12	J02F-04*03	J01F-04/03	2A4A12		NOT USED	$C7EJ12
2A4A12	J02F-06*05	J01F-06/05	2A4A12		NOT USED	$C7EJ13
2A4A12	J02F-08*07	J01F-08/07	2A4A12		NOT USED	$C7EJ14
2A4A12	J03A-02/01	2C0B0-E0*E1		6-189	CHANNEL 7 EXTERNAL DATA BIT 00	$C7EX00
2A4A12	J03A-04/03	2C0B0-I0*I1		6-189	CHANNEL 7 EXTERNAL DATA BIT 01	$C7EX01
2A4A12	J03A-06/05	2C0B0-M1*M0		6-189	CHANNEL 7 EXTERNAL DATA BIT 02	$C7EX02
2A4A12	J03A-08/07	2C0B0-N0*N1		6-189	CHANNEL 7 EXTERNAL DATA BIT 03	$C7EX03
2A4A12	J03A-10/09	2C0B0-S0*S1		6-189	CHANNEL 7 EXTERNAL DATA BIT 04	$C7EX04
2A4A12	J03B-02/01	2C0B0-W0*W1		6-189	CHANNEL 7 EXTERNAL DATA BIT 05	$C7EX05
2A4A12	J03B-04/03	2C0B0-B2*B3		6-189	CHANNEL 7 EXTERNAL DATA BIT 06	$C7EX06
2A4A12	J03B-06/05	2C0B0-G2*G3		6-189	CHANNEL 7 EXTERNAL DATA BIT 07	$C7EX07
2A4A12	J03B-08/07	2C0B0-M2*M3		6-189	CHANNEL 7 EXTERNAL DATA BIT 08	$C7EX08
2A4A12	J03B-10/09	2C0B0-K3*K2		6-189	CHANNEL 7 EXTERNAL DATA BIT 09	$C7EX09
2A4A12	J03C-02/01	2C0B0-Q3*Q2		6-189	CHANNEL 7 EXTERNAL DATA BIT 10	$C7EX10
2A4A12	J03C-04/03	2C0B0-W2*W3		6-189	CHANNEL 7 EXTERNAL DATA BIT 11	$C7EX11
2A4A12	J03C-06/05	2C0B0-U3*U2		6-189	CHL 7 EXTERNAL PARITY BIT 1	$C7EXP1
2A4A12	J03C-08/07	2C0A2-R2*R3		6-167	CHL 7 EXTERNAL BUSY SIGNAL	$C7EXRW
2A4A12	J03C-10/09	J04C-10*09	2A4A12		NOT USED	$C7EXRA
2A4A12	J03D-02/01	2C0A2-X0*X1		6-167	CHL 7 EXTERNAL READ SIGNAL	$C7EXRD
2A4A12	J03D-04/03	2C0A2-T1*T0		6-167	CHL 7 EXTERNAL WRITE SIGNAL	$C7EXWR
2A4A12	J03D-06/05	2C0A2-I3*I2		6-167	CHL 7 EXTERNAL CONNECT SIGNAL	$C7EXCN
2A4A12	J03D-08/07	2C0A2-F2*F3		6-167	CHL 7 EXTERNAL SELECT SIGNAL	$C7EXSL
2A4A12	J03D-10/09	2C0B2-C3*C2		6-175	CHL 7 EXTERNAL DATA SIGNAL	$C7EXDS
2A4A12	J03E-02*01	2C0B2-J2/J3		6-175	CHL 7 EXTERNAL REPLY SIGNAL	$C7EXRP
2A4A12	J03E-04*03	2C0A2-E3/E2		6-167	CHL 7 EXTERNAL REJECT SIGNAL	$C7EXRJ
2A4A12	J03E-06*05	2C0B2-I3/I2		6-175	CHL 7 EXTERNAL REJECT SIGNAL	$C7EXER
2A4A12	J03E-08*07	2C0A2-N2/N3		6-167	CHL 7 EXTERNAL PARITY ERROR	$C7EXPE
2A4A12	J03E-10/09	J04E-10*09	2A4A12		NOT USED	$C7EJA0
2A4A12	J03F-02/01	2C0B2-W0*W1		6-175	CHL 7 EXTERNAL WORD MARK	$C7EXWM
2A4A12	J03F-04/03	2C0A2-Q1*O0		6-167	CHL 7 CLEAR TO EXTERNAL EQUIP	$C7EXCL
2A4A12	J03F-06/05	J04F-06*05	2A4A12		NOT USED	$C7EJA1
2A4A12	J03F-08/07	J04F-08*07	2A4A12		NOT USED	$C7EJA2
2A4A12	J04A-02/01	2C0B0-F0*F1		6-189	CHANNEL 7 EXTERNAL DATA BIT 00	$C7EX00
2A4A12	J04A-04/03	2C0B0-J0*J1		6-189	CHANNEL 7 EXTERNAL DATA BIT 01	$C7EX01
2A4A12	J04A-06/05	2C0B0-L1*L0		6-189	CHANNEL 7 EXTERNAL DATA BIT 02	$C7EX02
2A4A12	J04A-08/07	2C0B0-O0*O1		6-189	CHANNEL 7 EXTERNAL DATA BIT 03	$C7EX03
2A4A12	J04A-10/09	2C0B0-T0*T1		6-189	CHANNEL 7 EXTERNAL DATA BIT 04	$C7EX04
2A4A12	J04B-02/01	2C0B0-X0*X1		6-189	CHANNEL 7 EXTERNAL DATA BIT 05	$C7EX05
2A4A12	J04B-04/03	2C0B0-C2*C3		6-189	CHANNEL 7 EXTERNAL DATA BIT 06	$C7EX06
2A4A12	J04B-06/05	2C0B0-H2*H3		6-189	CHANNEL 7 EXTERNAL DATA BIT 07	$C7EX07
2A4A12	J04B-08/07	2C0B0-N2*N3		6-189	CHANNEL 7 EXTERNAL DATA BIT 08	$C7EX08
2A4A12	J04B-10/09	2C0B0-L3*L2		6-189	CHANNEL 7 EXTERNAL DATA BIT 09	$C7EX09
2A4A12	J04C-02/01	2C0B0-R3*R2		6-189	CHANNEL 7 EXTERNAL DATA BIT 10	$C7EX10
2A4A12	J04C-04/03	2C0B0-X2*X3		6-189	CHANNEL 7 EXTERNAL DATA BIT 11	$C7EX11
2A4A12	J04C-06/05	2C0B0-V3*V2		6-189	CHL 7 EXTERNAL PARITY BIT 1	$C7EXP1
2A4A12	J04C-08/07	2C0A2-R2*R3		6-167	CHL 7 EXTERNAL BUSY SIGNAL	$C7EXRW
2A4A12	J04C-10*09	J03C-10/09	2A4A12		NOT USED	$C7EXRA
2A4A12	J04D-02/01	2C0A2-X0*X1		6-167	CHL 7 EXTERNAL READ SIGNAL	$C7EXRD
2A4A12	J04D-04/03	2C0A2-T1*T0		6-167	CHL 7 EXTERNAL WRITE SIGNAL	$C7EXWR
2A4A12	J04D-06/05	2C0A2-I3*I2		6-167	CHL 7 EXTERNAL CONNECT SIGNAL	$C7EXCN
2A4A12	J04D-08/07	2C0A2-F2*F3		6-167	CHL 7 EXTERNAL SELECT SIGNAL	$C7EXSL
2A4A12	J04D-10/09	2C0B2-C3*C2		6-175	CHL 7 EXTERNAL DATA SIGNAL	$C7EXDS
2A4A12	J04E-02*01	2C0B2-J2/J3		6-175	CHL 7 EXTERNAL REPLY SIGNAL	$C7EXRP
2A4A12	J04E-04*03	2C0A2-E3/E2		6-167	CHL 7 EXTERNAL REJECT SIGNAL	$C7EXRJ
2A4A12	J04E-06*05	2C0B2-I3/I2		6-175	CHL 7 EXTERNAL REJECT SIGNAL	$C7EXER
2A4A12	J04E-08*07	2C0A2-N2/N3		6-167	CHL 7 EXTERNAL PARITY ERROR	$C7EXPE
2A4A12	J04E-10*09	J03E-10/09	2A4A12		NOT USED	$C7EJA0
2A4A12	J04F-02/01	2C0B2-W0*W1		6-175	CHL 7 EXTERNAL WORD MARK	$C7EXWM
2A4A12	J04F-04/03	2C0A2-O1*O0		6-167	CHL 7 CLEAR TO EXTERNAL EQUIP	$C7EXCL
2A4A12	J04F-06*05	J03F-06/05	2A4A12		NOT USED	$C7EJA1
2A4A12	J04F-08*07	J03F-08/07	2A4A12		NOT USED	$C7EJA2
2A4A13	J01A-02*01	J02A-02/01	2A4A13		NOT USED	$CCEX00
2A4A13	J01A-04*03	J02A-04/03	2A4A13		NOT USED	$CCEX01
2A4A13	J01A-06*05	J02A-06/05	2A4A13		NOT USED	$CCEX02
2A4A13	J01A-08*07	J02A-08/07	2A4A13		NOT USED	$CCEX03
2A4A13	J01A-10*09	J02A-10/09	2A4A13		NOT USED	$CCEX04
2A4A13	J01B-02*01	J02B-02/01	2A4A13		NOT USED	$CCEX05
2A4A13	J01B-04*03	J02B-04/03	2A4A13		NOT USED	$CCEX06
2A4A13	J01B-06*05	J02B-06/05	2A4A13		NOT USED	$CCEX07
2A4A13	J01B-08*07	J02B-08/07	2A4A13		NOT USED	$CCEX08
2A4A13	J01B-10*09	J02B-10/09	2A4A13		NOT USED	$CCEX09
2A4A13	J01C-02*01	J02C-02/01	2A4A13		NOT USED	$CCEX10
2A4A13	J01C-04*03	J02C-04/03	2A4A13		NOT USED	$CCEX11
2A4A13	J01C-06*05	J02C-06/05	2A4A13		NOT USED	$CCEXP1
2A4A13	J01C-10*09	2B0B5-W3/W2		6-107	EXTERNAL READ - B CABLE	$CBEXRD
2A4A13	J01D-02*01	2B0B5-C2/C3		6-107	EXTERNAL READ - A CABLE	$CAEXRD
2A4A13	J01D-04*03	2B0B5-Q3/Q2		6-107	EXTERNAL WRITE - A CABLE	$CAEXWR
2A4A13	J01D-06*05	2B0B5-S2/S3		6-107	EXTERNAL CONN/FCN - A CABLE	$CAEXCF
2A4A13	J01D-08*07	2B0B5-S2/S3		6-107	EXTERNAL CONN/FCN - A CABLE	$CAEXCF
2A4A13	J01D-10*09	2B0B5-E3/E2		6-107	EXTERNAL DATA SIGNAL - A CABLE	$CAEXDS
2A4A13	J01E-02/01	2B0B5-K2*K3		6-107	EXTERNAL REPLY - CABLE C	$CCEXRP
2A4A13	J01E-04/03	2B0B5-M3*M2		6-107	EXTERNAL REJECT - CABLE C	$CCEXRJ
2A4A13	J01E-06/05	2B0B5-O2*O3		6-107	EXTERNAL EOR - CABLE A	$CAEXER
2A4A13	J01E-10*09	2B0B5-I2/I3		6-107	EXTERNAL WRITE - CABLE B	$CBEXWR
2A4A13	J01F-06*05	2B0B5-U2/U3		6-107	EXTERNAL DATA SIGNAL - B CABLE	$CBEXDS
2A4A13	J01F-08/07	2B0B5-X3*X2		6-107	EXTERNAL EOR - CABLE B	$CBEXER
2A4A13	J02A-02/01	J01A-02*01	2A4A13		NOT USED	$CCEX00
2A4A13	J02A-04/03	J01A-04*03	2A4A13		NOT USED	$CCEX01
2A4A13	J02A-06/05	J01A-06*05	2A4A13		NOT USED	$CCEX02
2A4A13	J02A-08/07	J01A-08*07	2A4A13		NOT USED	$CCEX03
2A4A13	J02A-10/09	J01A-10*09	2A4A13		NOT USED	$CCEX04
2A4A13	J02B-02/01	J01B-02*01	2A4A13		NOT USED	$CCEX05
2A4A13	J02B-04/03	J01B-04*03	2A4A13		NOT USED	$CCEX06

435

CONNECTOR		ORIGIN		PAGE	DEFINITION	SIG NAME
2A4A13	J02B-06/05	J01B-06*05	2A4A13		NOT USED	$CCEX07
2A4A13	J02B-08/07	J01B-08*07	2A4A13		NOT USED	$CCEX08
2A4A13	J02B-10/09	J01B-10*09	2A4A13		NOT USED	$CCEX09
2A4A13	J02C-02/01	J01C-02*01	2A4A13		NOT USED	$CCEX10
2A4A13	J02C-04/03	J01C-04*03	2A4A13		NOT USED	$CCEX11
2A4A13	J02C-06/05	J01C-06*05	2A4A13		NOT USED	$CCEXP1
2A4A13	J02C-10*09	2B0B5-C2/C3		6-107	EXTERNAL READ - A CABLE	$CAEXRD
2A4A13	J02D-02*01	2B0B5-W3/W2		6-107	EXTERNAL READ - B CABLE	$CBEXRD
2A4A13	J02D-04*03	2B0B5-I2/I3		6-107	EXTERNAL WRITE - CABLE B	$CBEXWR
2A4A13	J02D-06*05	2B0B5-G2/G3		6-107	EXTERNAL CONN/FCN - B CABLE	$CBEXCF
2A4A13	J02D-08*07	2B0B5-G2/G3		6-107	EXTERNAL CONN/FCN - B CABLE	$CBEXCF
2A4A13	J02D-10*09	2B0B5-U2/U3		6-107	EXTERNAL DATA SIGNAL - B CABLE	$CBEXDS
2A4A13	J02E-02/01	2B0B5-K2*K3		6-107	EXTERNAL REPLY - CABLE C	$CCEXRP
2A4A13	J02E-04/03	2B0B5-M3*M2		6-107	EXTERNAL REJECT - CABLE C	$CCEXRJ
2A4A13	J02E-06/05	2B0B5-X3*X2		6-107	EXTERNAL EOR - CABLE B	$CBEXER
2A4A13	J02E-10*09	2B0B5-Q3/Q2		6-107	EXTERNAL WRITE - A CABLE	$CAEXWR
2A4A13	J02F-06*05	2B0B5-E3/E2		6-107	EXTERNAL DATA SIGNAL - A CABLE	$CAEXDS
2A4A13	J02F-08/07	2B0B5-02*03		6-107	EXTERNAL EOR - CABLE A	$CAEXER
2A4A13	J03A-02/01	J04D-02*01	2A4A13			$CBEXI0
2A4A13	J03A-04/03	J04D-04*03	2A4A13			$CBEXI1
2A4A13	J03A-06/05	J04D-06*05	2A4A13			$CBEXI2
2A4A13	J03A-08/07	J04D-08*07	2A4A13			$CBEXI3
2A4A13	J03A-10/09	J04D-10*09	2A4A13			$CBEXI4
2A4A13	J03B-02/01	J04E-02*01	2A4A13			$CBEXI5
2A4A13	J03B-04/03	J04E-04*03	2A4A13			$CBEXI6
2A4A13	J03B-06/05	J04E-06*05	2A4A13			$CBEXI7
2A4A13	J03B-08/07	J04E-10*09	2A4A13			$CBEXOV
2A4A13	J03D-02*01	J04A-02/01	2A4A13			$CAEXI0
2A4A13	J03D-04*03	J04A-04/03	2A4A13			$CAEXI1
2A4A13	J03D-06*05	J04A-06/05	2A4A13			$CAEXI2
2A4A13	J03D-08*07	J04A-08/07	2A4A13			$CAEXI3
2A4A13	J03D-10*09	J04A-10/09	2A4A13			$CAEXI4
2A4A13	J03E-02*01	J04B-02/01	2A4A13			$CAEXI5
2A4A13	J03E-04*03	J04B-04/03	2A4A13			$CAEXI6
2A4A13	J03E-06*05	J04B-06/05	2A4A13			$CAEXI7
2A4A13	J03E-10*09	J04B-08/07	2A4A13			$CAEXOV
2A4A13	J04A-02/01	J03D-02*01	2A4A13			$CAEXI0
2A4A13	J04A-04/03	J03D-04*03	2A4A13			$CAEXI1
2A4A13	J04A-06/05	J03D-06*05	2A4A13			$CAEXI2
2A4A13	J04A-08/07	J03D-08*07	2A4A13			$CAEXI3
2A4A13	J04A-10/09	J03D-10*09	2A4A13			$CAEXI4
2A4A13	J04B-02/01	J03E-02*01	2A4A13			$CAEXI5
2A4A13	J04B-04/03	J03E-04*03	2A4A13			$CAEXI6
2A4A13	J04B-06/05	J03E-06*05	2A4A13			$CAEXI7
2A4A13	J04B-08/07	J03E-10*09	2A4A13			$CAEXOV
2A4A13	J04D-02*01	J03A-02/01	2A4A13			$CBEXI0
2A4A13	J04D-04*03	J03A-04/03	2A4A13			$CBEXI1
2A4A13	J04D-06*05	J03A-06/05	2A4A13			$CBEXI2
2A4A13	J04D-08*07	J03A-08/07	2A4A13			$CBEXI3
2A4A13	J04D-10*09	J03A-10/09	2A4A13			$CBEXI4
2A4A13	J04E-02*01	J03B-02/01	2A4A13			$CBEXI5
2A4A13	J04E-04*03	J03B-04/03	2A4A13			$CBEXI6
2A4A13	J04E-06*05	J03B-06/05	2A4A13			$CBEXI7
2A4A13	J04E-10*09	J03B-08/07	2A4A13			$CBEXOV
2A4A15	J01A-01*	2A0A7-R0		6-133	CHAN 0 24-BIT MODE IDENTIFIER	C03507
2A4A15	J01A-02*	2B1A0-P2		6- 5	CHAN 0 24-BIT MODE	C0EQ07
2A4A15	J01B-01*	2A0A7-R1		6-133	CHAN 0 12-BIT IDENT FROM OU GROUND PIN	C03506
2A4A15	J01B-02*	2B1A0-R2		6- 5	CHAN 0 12-BIT MODE	C0EQ06
2A4A15	J01C-01*	2A0A6-R0		6-135	CHAN 1 24-BIT MODE IDENTIFIER	C13507
2A4A15	J01C-02*	2B1A0-P3		6- 5	CHAN 1 24-BIT MODE	C1EQ07
2A4A15	J01D-01*	2A0A6-R1		6-135	CHAN 1 12-BIT IDENT FROM OU GROUND PIN	C13506
2A4A15	J01D-02*	2B1A0-R3		6- 5	CHAN 1 12-BIT MODE	C1EQ06
2A4A15	J01E-01*	2A0A3-R0		6-137	CHAN 2 24-BIT MODE IDENTIFIER	C23507
2A4A15	J01E-02*	2B1A0-Q3		6- 5	CHAN 2 24-BIT MODE	C2EQ07
2A4A15	J01F-01*	2A0A3-R1		6-137	CHAN 3 12-BIT IDENT FROM OU GROUND PIN	C23506
2A4A15	J01F-02*	2B1A0-Q3		6- 5	CHAN 2 12-BIT MODE	C2EQ06
2A4A15	J01G-01*	2A0A2-R0		6-139	CHAN 3 24-BIT IDENTIFIER	C33507
2A4A15	J01G-02*	2B1A0-Q2		6-139	CHAN 3 12-BIT IDENT FROM OU GROUND PIN	C33506
2A4A15	J01H-01*	2A0A2-R1				
2A4A15	J01H-02*	2B1A0-S3		6- 5	CHAN 3 12-BIT MODE	C3EQ06
2A4A15	J01J-01*	2C0B7-R0		6-169	CHAN 4 24-BIT MODE IDENTIFIER	C43507
2A4A15	J01J-02*	2B1B0-R2		6- 7	CHAN 4 24-BIT MODE	C4EQ07
2A4A15	J01K-01*	2C0B7-R1		6-169	CHAN 4 12-BIT IDENT FROM OU GROUND PIN	C43506
2A4A15	J01K-02*	2B1B0-P2		6- 7	CHAN 4 12-BIT MODE	C4EQ06
2A4A15	J01L-01*	2C0B6-R0		6-171	CHAN 5 24-BIT MODE IDENTIFIER	C53507
2A4A15	J01L-02*	2B1B0-R3		6- 7	CHAN 5 24-BIT MODE	C5EQ07
2A4A15	J01M-01*	2C0B6-R1		6-171	CHAN 5 12-BIT IDENT FROM OU GROUND PIN	C53506
2A4A15	J01M-02*	2B1B0-P3		6- 7	CHAN 5 12-BIT MODE	C5EQ06
2A4A15	J01N-01*	2C0B3-R0		6-173	CHAN 6 24-BIT MODE IDENTIFIER	C63507
2A4A15	J01N-02*	2B1B0-Q3		6- 7	CHAN 6 24-BIT MODE	C6EQ07
2A4A15	J01P-01*	2C0B3-R1		6-173	CHAN 6 12-BIT IDENT FROM OU GROUND PIN	C63506
2A4A15	J01P-02*	2B1B0-03		6- 7	CHAN 6 12-BIT MODE	C6EQ06
2A4A15	J01R-01*	2C0B2-R0		6-175	CHAN 7 24-BIT IDENTIFIER	C73507
2A4A15	J01R-02*	2B1B0-S3		6- 7	CHAN 7 24-BIT MODE	C7EQ07
2A4A15	J01S-01*	2C0B2-R1		6-175	CHAN 7 12-BIT IDENT FROM OU GROUND PIN	C73506
2A4A15	J01S-02*	2B1B0-02		6- 7	CHAN 7 12-BIT MODE	C7EQ06
2A4A15	J01T-03*	P05F-08	2A1A06		INTERRUPT BIAS SWITCH FOR BIT7	INTSW7
2A4A15	J01U-03*	P05F-07	2A1A06		INTERRUPT BIAS SWITCH FOR BIT6	INTSW6

CONNECTOR		ORIGIN
1A2A06	J01A-02/01	1B1B9-G2*G3
1A2A06	J01A-04/03	1B1B8-D0*D1
1A2A06	J01A-06/05	1B1B9-K1*K0
1A2A06	J01A-08/07	1B1B9-C1*C0
1A2A06	J01A-10/09	1B1B9-D0*D1
1A2A06	J01B-02/01	1B1B9-I3*I2
1A2A06	J01B-04/03	1B1B9-H3*H2
1A2A06	J01B-06/05	1B1B9-L0*L1
1A2A06	J01B-08/07	1B0A7-K1*K0
1A2A06	J01B-10*09	1B0B9-P0/P1
1A2A06	J01C-02*01	1B0A7-P1/P0
1A2A06	J01C-04*03	1B0A7-Q1/Q0
1A2A06	J01C-06*05	1C1A9-P3/P2
1A2A06	J01C-08*07	1B0B4-F0/F1
1A2A06	J01C-10*09	1B0B7-T0/T1
1A2A06	J01D-02*01	1B0B4-E0/E1
1A2A06	J01D-04/03	1B0B4-Q2*Q3
1A2A06	J01D-06*05	1B0B1-K3/K2
1A2A06	J01D-08*07	1C1B7-D2/D3
1A2A06	J01D-10*09	1C1B7-F2/F3
1A2A06	J01E-02*01	1C1B7-E2/E3
1A2A06	J01E-04*03	1C1B7-K2/K3
1A2A06	J01E-06*05	1C1B7-I2/I3
1A2A06	J01E-08*07	1C1B7-H2/H3
1A2A06	J01E-10*09	1C1B7-J2/J3
1A2A06	J01F-02*01	1C0B7-E0/E1
1A2A06	J01F-04*03	1C0B9-P0/P1
1A2A06	J01F-06*05	1C0B8-P0/P1
1A2A06	J01F-08*07	1C0B7-Q0/Q1
1A2A06	J02A-02/01	1C1B3-E1*F0
1A2A06	J02A-04*03	1C1A9-T3/T2
1A2A06	J02A-06/05	1B0A0-G3*G2
1A2A06	J02A-08/07	1C1B3-P1*P0
1A2A06	J02A-10/09	1B0A0-Q2*Q3
1A2A06	J02B-02*01	1C1A9-Q3/Q2
1A2A06	J02B-04/03	1C1B3-D1*D0
1A2A06	J02B-06*05	1C1A9-S3/S2
1A2A06	J02B-08/07	1B0A0-X2*X3

PAGE	DEFINITION
3-125	MAINT REG BIT 06
3-127	MAINT REG BIT 13
3-125	MAINT REG BIT 02
3-125	MAINT REG BIT 00
3-125	MAINT REG BIT 01
3-125	MAINT REG BIT 05
3-125	MAINT REG BIT 04
3-125	MAINT REG BIT 03
2- 15	INCREMENT FOR BDP COMPLETE
2- 17	NOT DECREMENT ON/ADDRESS MOD.
2- 15	(EDIT)(NOT FIRST CYCLE)(SPECIAL INCREMENT CYCLE FOR F1 ADDRESS PRECEDING ADDR TO S ON ROPC)
2- 15	ROPC(FIRST CYCLE EDIT+67.(0+1))-BLOCK INCR.F2
3- 41	READ A OPERAND REQUEST
2- 7	STORE MEMORY REQUEST
2- 19	READ A OPERAND REQUEST
2- 7	READ OPERAND REQUEST
2- 7	START BDP PULSE
2- 9	NOT BDP RESUME PULSE FOR STORAGE REQUEST OR EXIT RESUME
3- 15	BIT 13 OF MAINTENANCE REGISTER
3- 15	BIT 02 OF MAINTENANCE REGISTER
3- 15	MAINTENANCE REGISTER,BIT 03
3- 15	MAINTENANCE REGISTER,BIT 05
3- 15	BIT 04 OF MAINTENANCE REGISTER
3- 15	MAINTENANCE REGISTER,BIT 01
3- 15	BIT 00 OF MAINTENANCE REGISTER
3- 3	BIT 06 OF MAINTENANCE REGISTER
3- 7	BDP INSTRUCTION(NOT ROPC)
3- 5	BDP INSTRUCTION(NOT ROPA)
3- 3	ADVANCE-START ARITH
3- 29	F0 BIT 15 (FOR 70.X XLTN)
3- 41	STORE COMPLEMENT OF AQ ON 66.0
2- 35	F1 REGISTER BIT 21
3- 29	F0 BIT 17 (FOR 70.X XLTN)
2- 35	F1 REGISTER BIT 22
3- 41	66.0 XLTN TO ARITH AFTER RNI 3
3- 29	F0 BIT 16 (FOR 70.X XLTN)
3- 41	LAST CHARACTER
2- 35	F1 REGISTER BIT 23

CONNECTOR		ORIGIN	
1A2A06	J02B-10/09	1C1B0-R2*R3	
1A2A06	J02C-02/01	1C1B0-P3*P2	
1A2A06	J02C-04/03	1C1B0-D2*D3	
1A2A06	J02C-06/05	1C1B0-Q3*Q2	
1A2A06	J02C-08/07	1C1B0-S2*S3	
1A2A06	J02C-10*09	1B0B9-G0/G1	
1A2A06	J02D-02*01	P01D-02/01	1A4A06
1A2A06	J02D-04/03	1C0A8-T1*T0	
1A2A06	J02D-04/03	1C0A8-T1*T0	
1A2A06	J02D-06/05	1C0A8-01*00	
1A2A06	J02D-08*07	1C0B7-J0/J1	
1A2A06	J02D-10*09	1C1B6-R1/R0	
1A2A06	J02E-02*01	1C1B6-Q1/Q0	
1A2A06	J02E-04/03	P01E-04*03	1A4A06
1A2A06	J02E-06*05	P01E-06/05	1A4A06
1A2A06	J02E-08/07	1C0A1-L3*L2	
1A2A06	J02E-09	P02E-09*	1A4A06
1A2A06	J02E-10	P02E-10*	1A4A06
1A2A06	J02F-02/01	1C0B9-01*00	
1A2A06	J02F-04/03	1C0A1-I3*I2	
1A2A06	J02F-06/05	1C0B3-U3*U2	
1A2A06	J02F-08*07	1B0A3-D2/D3	
1A2A06	J03A-02/01	1A0B2-W3*W2	
1A2A06	J03A-04/03	1A0B2-T2*T3	
1A2A06	J03A-06*05	1B1B5-K3/K2	
1A2A06	J03A-08*07	1B1B5-L3/L2	
1A2A06	J03A-10*09	1B1B5-M1/M0	
1A2A06	J03B-02*01	1B1B5-N1/N0	
1A2A06	J03B-04*03	1B1B5-L1/L0	
1A2A06	J03B-06*05	1B1B5-W3/W2	
1A2A06	J03B-08*07	1C0A0-D2/D3	
1A2A06	J03B-10*09	1C0A0-L3/L2	
1A2A06	J03C-02*01	1C0A0-K3/K2	
1A2A06	J03C-04*03	1C0A0-E2/E3	
1A2A06	J03C-06/05	1C0A0-Q2*Q3	
1A2A06	J03C-08/07	1C0A0-N3*N2	
1A2A06	J03C-10/09	1B1B5-B3*B2	
1A2A06	J03D-02/01	1B1B5-F3*F2	
1A2A06	J03D-04/03	1B1B5-D2*D3	
1A2A06	J03D-06/05	1B1B5-H2*H3	

PAGE	DEFINITION
3- 23	ARI. FNC. 66
3- 23	ARI. FNC. 65
3- 23	ARI. FNC. 70
3- 23	ARI. FNC. 67
3- 23	ARI. FNC. 64
2- 17	BDP INSTRUCTION IS NO-OP (BCD FAULT)(BDP COMPLETE)(H03)
3- 9	CLEAR BDP OR ENABLE ROP+STO
	PRIORITY (AT2)
3- 9	66.0 EXIT RESUME (ARITH TIME2) (ENABLE EXIT FROM 66.0)(AR T2)
3- 3	NOT(64+65+66+67+70.6+70.7)
3- 13	ENABLE I0 TO I4 FOR BDP
3- 13	D5=K8-I3-I5=D2 FOR 64+65+67+ 66.(1-5)+70.6+66.0 EXIT PATH
	LEGAL WRITE FOR BDP
	READ C OPERAND REQUEST(EDIT+ 67(0+1))
	INTERRUPT PRESENT
02- 43	NOT(INTERRUPT PRESENT)
	BDP FAST MARGIN
	BDP SLOW MARGIN
	(66.0 ARITH RESUME)(ARITH T0)
03- 7	66.0 RESUME TO BDP (ARITH T0)
2- 43	ILLEGAL WRITE INTERRUPT FF
2-49	MASTER CLEAR+INTERNAL CLEAR
2- 21	RNI TO THE NEXT INST FOR (NOT 2ND PASS)(OPERATION COM- PLETE)(NOT ILL. WRITE)+(NO-OP) (NOT INT STOP)(NOT ILL. WRITE)
	*MAINTENANCE STOP
2- 71	F1 REGISTER BIT 0
2- 71	F1 REGISTER BIT 1
4- 39	GATE J1,BITS 12-19,TO J3
4- 39	GATE J1,BITS 6-13,TO J3
4- 39	GATE J2,BITS 0-5,TO J4
4- 39	GATE J2,BITS 6-11,TO J4
4- 39	GATE J2,BITS 12-17 TO J4
4- 39	GATE J1,BITS 3-7,TO J3
2- 37	PARTIAL WRITE,BITS 00-05
2- 37	PARTIAL WRITE,BITS 12-17
2- 37	PARTIAL WRITE,BITS 18-23
2- 37	PARTIAL WRITE,BITS 06-11
2- 37	F0 REG,BIT 1, TO BDP
2- 37	F0 REG,BIT 0, TO BDP
4- 39	J1 TO J3 BIT 00
4- 39	J1 TO J3 BIT 01
4- 39	J1 TO J3 BIT 06
4- 39	J1 TO J3 BIT 07

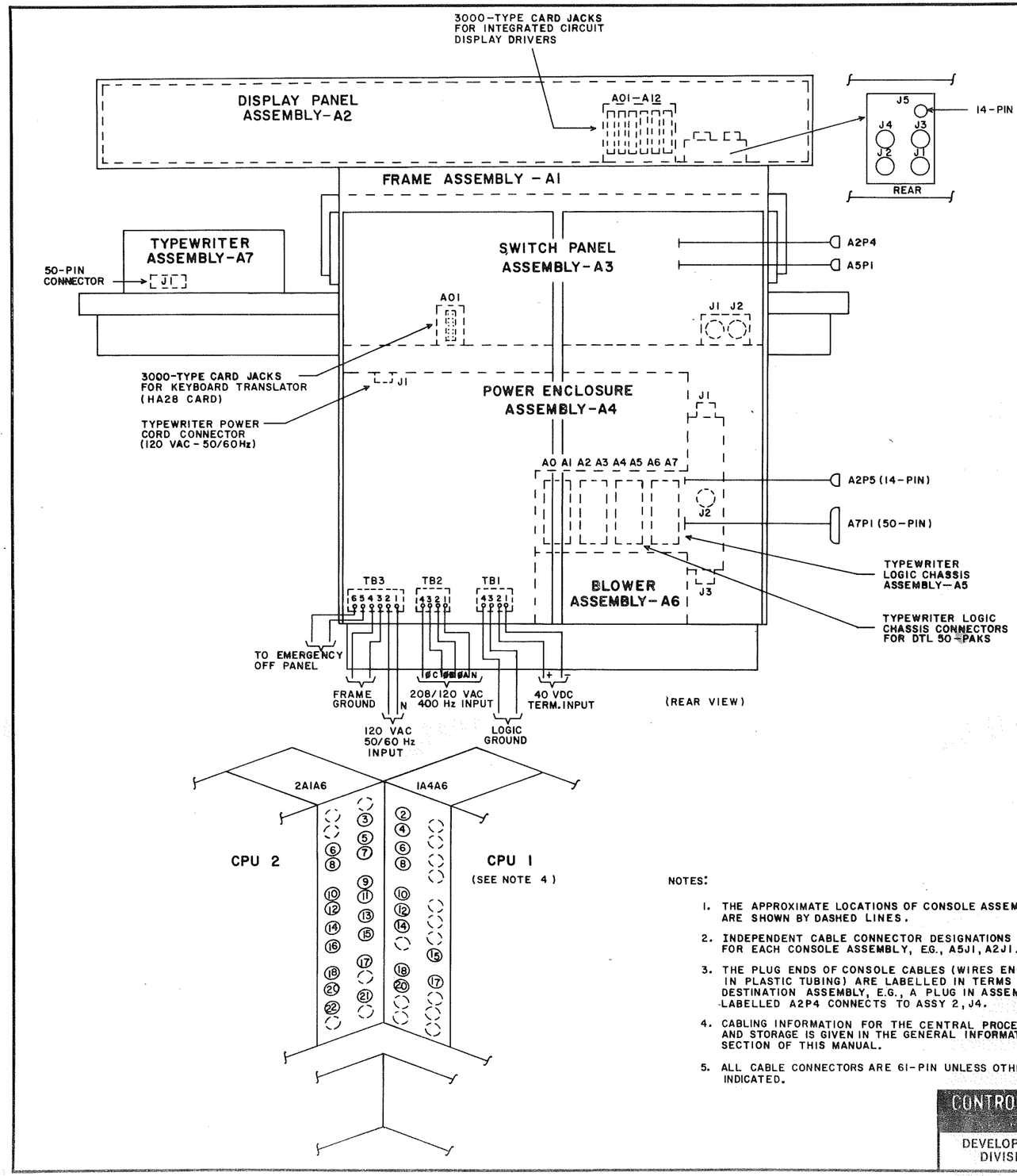
CONNECTOR		ORIGIN		PAGE	DEFINITION
1A2A06	J03D-08/07	1B1B5-R3*R2		4- 39	J1 TO J3 BIT 03
1A2A06	J03D-10/09	1B1B5-H1*H0		4- 39	J2 TO J4 BIT 02
1A2A06	J03E-02/01	1B1B5-B1*B0		4- 39	J2 TO J4 BIT 00
1A2A06	J03E-04/03	1B1B5-N3*N2		4- 39	J1 TO J3 BIT 02
1A2A06	J03E-06/05	1B1B5-U0*U1		4- 39	J1 TO J3 BIT 05
1A2A06	J03E-08/07	1B1B5-X1*X0		4- 39	J1 TO J3 BIT 04
1A2A06	J03E-10/09	1B1B5-J0*J1		4- 39	J2 TO J4 BIT 03
1A2A06	J03F-01	P02F-01*	1A4A06		CC=MR SWITCH IN CC POSITION
1A2A06	J03F-04/03	1B1B5-V0*V1		4- 39	J2 TO J4 BIT 05
1A2A06	J03F-06/05	1B1B5-W1*W0		4- 39	J2 TO J4 BIT 04
1A2A06	J03F-08/07	1B1B5-G1*G0		4- 39	J2 TO J4 BIT 01
1A2A06	J04A-02*01	1B0A7-D0/D1		2- 15	INTERRUPT START + FETCH SIGN 1
1A2A06	J04A-04*03	1B0A3-K1/K0		2- 21	NOT((CONDITION REG=01)(70.0)+ (CONDITION REG=00)(70.1)+ (CONDITION REG=10)(70.2))
1A2A06	J04A-06*05	1B0A3-P3/P2		2- 21	ADD 3 TO P REGISTER
1A2A06	J04A-08/07	1B1B9-W3*W2		3-125	I9 BIT 07 TO W5, L2, FORCE *
1A2A06	J04A-10/09	1B1B8-J0*J1		3-127	I9 BIT 14 TO W3, L1, BCD FAULT
1A2A06	J04B-02/01	1B1B8-E0*F1		3-127	I9 BIT 13 TO W3, L1, CARRY A
1A2A06	J04B-04/03	1B1B8-B0*A1		3-127	I9 BIT 12 TO W3, L1, 2ND PASS
1A2A06	J04B-06/05	1B1B8-S3*S2		3-127	I9 BIT 21 TO W3 AND L1
1A2A06	J04B-08/07	1B1B9-Q2*Q3		3-125	I9 BIT 04 TO W5, L2, FLTG SIGN
1A2A06	J04B-10/09	1B1B9-T3*T2		3-125	I9 BIT 19 TO W3 AND L1
1A2A06	J04C-02/01	1B1B9-X2*X3		3-125	I9 BIT 06 TO W5, L2, FORCE *
1A2A06	J04C-04/03	1B1B9-S3*S2		3-125	I9 BIT 17 TO W3 AND L1
1A2A06	J04C-06/05	1B1B9-L2*L3		3-125	I9 BIT 05 TO W5, L2, FORCE $
1A2A06	J04C-08/07	1B1B8-T3*T2		3-127	I9 BIT 23 TO W3 AND L1
1A2A06	J04C-10/09	1B1B9-B0*B1		3-125	I9 BIT 00 TO W5, L2, COND REG0
1A2A06	J04D-02/01	1B1B9-E0*F1		3-125	I9 BIT 01 TO W5, L2, COND REG1
1A2A06	J04D-04/03	1B1B8-U2*U3		3-127	I9 BIT 22 TO W3 AND L1
1A2A06	J04D-06/05	1B1B9-V0*V1		3-125	I9 BIT 16 TO W3 AND L1
1A2A06	J04D-08/07	1B1B9-U2*U3		3-125	I9 BIT 18 TO W3 AND L1
1A2A06	J04D-10/09	1B1B9-J0*J1		3-125	I9 BIT 02 TO W5, L2, CR OR DB
1A2A06	J04E-02/01	1B1B8-V0*V1		3-127	I9 BIT 20 TO W3 AND L1
1A2A06	J04E-04/03	1B1B9-M0*M1		3-125	I9 BIT 03 TO W5, L2, ZERO SUPR
1A2A06	J04E-06/05	1B1B8-M0*M1		3-127	I9 BIT 15 TO W3 AND L1
1A2A06	J04E-08/07	1B1B8-X2*X3		3-127	I9 BIT 10 TO W5, L2, SIGNS ≠
1A2A06	J04E-10/09	1B1B8-W3*W2		3-127	I9 BIT 11 TO W5, L2, INT START
1A2A06	J04F-02/01	1B1B8-L2*L3		3-127	I9 BIT 09 TO W5, L2, OPERAND=0
1A2A06	J04F-04/03	1B1B8-Q2*Q3		3-127	I9 BIT 08 TO W5, L2, FORC FLTG
1A2A06	J05A-02*01	1B1A9-N3/N2		3-107	D5 TO I3 BIT 04
1A2A06	J05A-04*03	1B1A9-Q3/Q2		3-107	D5 TO I3 BIT 03
1A2A06	J05A-06*05	1B1A9-C0/C1		3-107	D5 TO I3 BIT 00
1A2A06	J05A-08*07	1B1A9-U3/U2		3-107	D5 TO I3 BIT 02
1A2A06	J05A-10*09	1B1A9-E1/E0		3-107	D5 TO I3 BIT 01
1A2A06	J05B-02*01	1B1A9-I3/I2		3-107	D5 TO I3 BIT 05
1A2A06	J05B-04*03	1B1A8-U3/U2		3-109	D5 TO I3 BIT 08
1A2A06	J05B-06*05	1B1A8-Q3/Q2		3-109	D5 TO I3 BIT 09
1A2A06	J05B-08*07	1B1A8-N3/N2		3-109	D5 TO I3 BIT 10
1A2A06	J05B-10*09	1B1A8-I3/I2		3-109	D5 TO I3 BIT 11
1A2A06	J05C-02*01	1B1A7-I3/I2		3-111	D5 TO I3 BIT 17
1A2A06	J05C-04*03	1B1A7-N3/N2		3-111	D5 TO I3 BIT 16
1A2A06	J05C-06*05	1B1A7-Q3/Q2		3-111	D5 TO I3 BIT 15
1A2A06	J05C-08*07	1B1A7-U3/U2		3-111	D5 TO I3 BIT 14
1A2A06	J05C-10*09	1B1A7-C0/C1		3-111	D5 TO I3 BIT 12
1A2A06	J05D-02*01	1B1A7-E1/E0		3-111	D5 TO I3 BIT 13
1A2A06	J05D-04*03	1B1A6-U3/U2		3-113	D5 TO I3 BIT 20
1A2A06	J05D-06*05	1B1A6-Q3/Q2		3-113	D5 TO I3 BIT 21
1A2A06	J05D-08*07	1B1A8-E1/E0		3-109	D5 TO I3 BIT 07
1A2A06	J05D-10*09	1B1A8-C0/C1		3-109	D5 TO I3 BIT 06
1A2A06	J05E-02*01	1B1A6-C0/C1		3-113	D5 TO I3 BIT 18
1A2A06	J05E-04*03	1B1A6-N3/N2		3-113	D5 TO I3 BIT 22
1A2A06	J05E-06*05	1B1A6-E1/E0		3-113	D5 TO I3 BIT 19
1A2A06	J05E-08*07	1B1A6-I3/I2		3-113	D5 TO I3 BIT 23
1A2A06	J05E-10*09	1C1A9-X3/X2		3- 41	(BDP INSTRUCTION)(NOT A FIELD LEGAL CHARACTER)

CONNECTOR		ORIGIN	PAGE	DEFINITION
1A2A06	J06A-02/01	1C0A6-E2*F3	4-	ASCII CHAR BIT 1(BCD TO ASCII)
1A2A06	J06A-04/03	1C0A6-G2*G3	4-	ASCII CHAR BIT 2(BCD TO ASCII)
1A2A06	J06A-06/05	1C0A6-N3*N2	4-	ASCII CHAR BIT 4(BCD TO ASCII)
1A2A06	J06A-08/07	1C0A6-L3*L2	4-	ASCII CHAR BIT 3(BCD TO ASCII)
1A2A06	J06A-10/09	1C0A6-H2*H3	4-	ASCII CHAR BIT 6(BCD TO ASCII)
1A2A06	J06B-02/01	1C0A6-Q3*Q2	4-	ASCII CHAR BIT 5(BCD TO ASCII)
1A2A06	J06B-04/03	1C0A5-E2*F3	4-	BCD CHAR BIT 1 (ASCII TO BCD)
1A2A06	J06B-06/05	1C0A5-B2*B3	4-	BCD CHAR BIT 0 (ASCII TO BCD)
1A2A06	J06B-08/07	1C0A6-B2*B3	4-	ASCII CHAR BIT 0(BCD TO ASCII)
1A2A06	J06B-10/09	1C0A5-L3*L2	4-	BCD CHAR BIT 3 (ASCII TO BCD)
1A2A06	J06C-02/01	1C0A5-G2*G3	4-	BCD CHAR BIT 2 (ASCII TO BCD)
1A2A06	J06C-04/03	1C0A5-N3*N2	4-	BCD CHAR BIT 4 (ASCII TO BCD)
1A2A06	J06C-06/05	1C0A5-Q3*Q2	4-	BCD CHAR BIT 5 (ASCII TO BCD)
1A2A06	J06C-08*07	1C0A6-J3/J2	4-	J3 TO W1 BIT 00
1A2A06	J06C-10*09	1C0A5-C2/C3	4-	J3 TO W0 BIT 00
1A2A06	J06D-02*01	1C0A5-D2/D3	4-	J3 TO W0 BIT 01
1A2A06	J06D-04*03	1C0A6-D2/D3	4-	J3 TO W1 BIT 02
1A2A06	J06D-06*05	1C0A6-C2/C3	4-	J3 TO W1 BIT 03
1A2A06	J06D-08*07	1C0A5-K3/K2	4-	J3 TO W0 BIT 02
1A2A06	J06D-10*09	1C0A6-P2/P3	4-	J3 TO W1 BIT 01
1A2A06	J06E-02*01	1C0A6-K3/K2	4-	J3 TO W1 BIT 05
1A2A06	J06E-04*03	1C0A6-D2/D3	4-	J3 TO W1 BIT 04
1A2A06	J06E-06*05	1C0A5-D2/D3	4-	J3 TO W0 BIT 05
1A2A06	J06E-08*07	1C0A5-J3/J2	4-	J3 TO W0 BIT 03
1A2A06	J06E-10*09	1C0A5-P2/P3	4-	J3 TO W0 BIT 04
1A2A06	P01A-02*01	1A2A0-W3/W2	4- 27	MAINT REG BIT 06
1A2A06	P01A-04*03	1A2A0-V3/V2	4- 27	MAINT REG BIT 13
1A2A06	P01A-06*05	1A2A0-Q1/Q0	4- 27	MAINT REG BIT 02
1A2A06	P01A-08*07	1A2A0-D0/D1	4- 27	MAINT REG BIT 00
1A2A06	P01A-10*09	1A2A0-I0/I1	4- 27	MAINT REG BIT 01
1A2A06	P01B-02*01	1A2A0-K2/K3	4- 27	MAINT REG BIT 05
1A2A06	P01B-04*03	1A2A0-H2/H3	4- 27	MAINT REG BIT 04
1A2A06	P01B-06*05	1A2A0-D2/D3	4- 27	MAINT REG BIT 03
1A2A06	P01B-08*07	1A2A1-U0/U1	4- 11	INCREMENT FOR BDP COMPLETE
1A2A06	P01B-10/09	1A2A0-X1*X0	4-27	NOT(DECREMEND ON ADDRESS MOD)
1A2A06	P01C-02/01	1A2A1-C3*C2	4- 11	(EDIT)(NOT FIRST CYCLE)(SPE= INCREMENT CYCLE FOR F1 ADDRESS PRECEDING ADDR TO S ON ROPC)
1A2A06	P01C-04/03	1A2A2-I1*T0	4- 9	ROPC(FIRST CYCLE EDIT+ 67:(0+1))=BLOCK INCR.F2
1A2A06	P01C-06/05	1A2A1-K0*K1	4- 11	READ A OPERAND REQUEST
1A2A06	P01C-08/07	1A2A1-P3*P2	4- 11	STORE MEMORY REQUEST
1A2A06	P01C-10/09	1A2A1-N2*N3	4- 11	READ A OPERAND REQUEST
1A2A06	P01D-02/01	1A2A1-G2*G3	4- 11	READ OPERAND REQUEST
1A2A06	P01D-04*03	1A2A1-M1/M0	4- 11	START BDP PULSE
			0	START BDP PULSE
1A2A06	P01D-06/05	1A2A1-00*01	4- 11	NOT BDP RESUME PULSE FOR STORAGE REQUEST OR EXIT RESUME
1A2A06	P01D-08/07	1A2A0-T3*T2	04- 27	BIT 13 OF MAINTENANCE REGISTER
1A2A06	P01D-10/09	1A2A0-J0*J1	04- 27	BIT 02 OF MAINTENANCE REGISTER
1A2A06	P01E-02/01	1A2A0-B2*B3	04- 27	MAINTENANCE REGISTER,BIT 03
1A2A06	P01E-04/03	1A2A0-I2*I3	04- 27	MAINTENANCE REGISTER,BIT 05

CONNECTOR		ORIGIN	PAGE	DEFINITION
1A2A06	P01E-06/05	1A2A0-F3*F2	4- 27	BIT 04 OF MAINTENANCE REGISTER
1A2A06	P01E-08/07	1A2A0-F1*F0	4- 27	MAINTENANCE REGISTER,BIT 01
1A2A06	P01E-10/09	1A2A0-C0*C1	4- 27	BIT 00 OF MAINTENANCE REGISTER
1A2A06	P01F-02/01	1A2A0-R3*R2	4- 27	BIT 06 OF MAINTENANCE REGISTER
1A2A06	P01F-04/03	1A2A1-F3*F2	4- 11	BDP INSTRUCTION(NOT ROPC)
1A2A06	P01F-06/05	1A2A1-K3*K2	4- 11	BDP INSTRUCTION(NOT ROPA)
1A2A06	P01F-08/07	1A2A2-M0*M1	4- 9	ADVANCE-START ARITH
1A2A06	P02A-02*01	1A2B4-X0/X1	4- 29	F0 BIT 15 (FOR 70.X XLTN)
1A2A06	P02A-04/03	1A2A3-J2*J3	4- 1	STORE COMPLEMENT OF AQ ON 66.0
1A2A06	P02A-06*05	1A2B4-C0/C1	4- 29	F1 REGISTER BIT 21
1A2A06	P02A-08*07	1A2B4-V1/V0	4- 29	F0 BIT 17 (FOR 70.X XLTN)
1A2A06	P02A-10*09	1A2B4-D0/D1	4- 29	F1 REGISTER BIT 22
1A2A06	P02B-02/01	1A2A8-M1*M0	4- 21	66.0 XLTN TO ARITH AFTER RNI 3
1A2A06	P02B-04*03	1A2B4-I1/I0	4- 29	F0 BIT 16 (FOR 70.X XLTN)
1A2A06	P02B-06/05	1A2A3-E0*E1	4- 1	LAST CHARACTER
1A2A06	P02B-08*07	1A2B4-J0/J1	4- 29	F1 REGISTER BIT 23
1A2A06	P02B-10*09	1A2B4-X2/X3	4- 29	ARI. FNC. 66
1A2A06	P02C-02*01	1A2B4-W1/W0	4- 29	ARI. FNC. 65
1A2A06	P02C-04*03	1A2B5-E0/F1	4- 33	ARI. FNC. 70
1A2A06	P02C-06*05	1A2B4-P2/P3	4- 29	ARI. FNC. 67
1A2A06	P02C-08*07	1A2B4-D0/D1	4- 29	ARI. FNC. 64
1A2A06	P02C-10/09	1A2A8-I3*I2	4- 21	BDP INSTRUCTION IS NO-OP
1A2A06	P02D-02/01	1A2A8-E1*E0	4- 21	(BCD FAULT)(BDP COMPLETE)(H03)
1A2A06	P02D-04*03	1A2B5-F1/F0	4- 33	CLEAR BDP OR ENABLE ROP*STO
1A2A06	P02D-04*03	1A2B5-F1/F0		PRIORITY (AT2)
1A2A06	P02D-06*05	1A2A3-K0/K1	4- 1	66.0 EXIT RESUME (ARITH TIME2)
1A2A06	P02D-08/07	1A2B6-W2*W3	4- 31	NOT(64*65*66*67*70.6*70.7)
1A2A06	P02D-10/09	1A2A8-L2*L3	4- 21	ENABLE I0 TO I4 FOR BDP
1A2A06	P02E-02/01	1A2A8-J1*J0	4- 21	D5-K8-I3-I5-D2 FOR 64*65*67* 66.(1-5)*70.6*66.0 EXIT PATH
1A2A06	P02E-04*03	1A2A1-L1/L0	04- 11	LEGAL WRITE FOR BDP
1A2A06	P02E-06/05	1A2A1-R2*R3	4- 11	READ C OPERAND REQUEST(EDIT* 67(0*1))
1A2A06	P02E-08*07	1A2A7-C3/C2	4- 5	NOT(INTERRUPT PRESENT)
1A2A06	P02E-09*	1A2A4-R0	4- 3	BDP FAST MARGIN
1A2A06	P02E-10*	1A2A4-R1	4- 3	BDP SLOW MARGIN
1A2A06	P02F-02*01	1A2A3-L1/L0	4- 1	66.0 RESUME TO BDP (ARITH T0)
1A2A06	P02F-04*03	1A2A7-E0/E1	4- 5	ILLEGAL WRITE INTERRUPT FF
1A2A06	P02F-06*05	1A2A7-M1/M0	4- 5	NOT (MASTER CLR +INTERNAL CLR)
1A2A06	P02F-08/07	1A2A8-R1*R0	4- 21	RNI TO THE NEXT INST FOR - (CONT. NEXT COL.)

CONNECTOR		ORIGIN	PAGE	DEFINITION
				(NOT 2ND PASS)(OPERATION COM- PLETE)(NOT ILL. WRITE)*(NO-OP) (NOT INT STOP)(NOT ILL. WRITE) *MAINTENANCE STOP
1A2A06	P03A-02*01	1A2B1-T2/T3	4- 37	F1 REGISTER BIT 0
1A2A06	P03A-04*03	1A2B1-U3/U2	4- 37	F1 REGISTER BIT 1
1A2A06	P03A-06/05	1A2B2-X3*X2	4- 35	GATE J1,BITS 12-19,TO J3
1A2A06	P03A-08/07	1A2B2-T0*T1	4- 35	GATE J1,BITS 6-13,TO J3
1A2A06	P03A-10/09	1A2B1-M0*M1	4- 37	GATE J2,BITS 0-5,TO J4
1A2A06	P03B-02/01	1A2B1-P1*P0	4- 37	GATE J2,BITS 6-11,TO J4
1A2A06	P03B-04/03	1A2B1-K1*K0	4- 37	GATE J2,BITS 12-17 TO J4
1A2A06	P03B-06/05	1A2B2-R1*R0	4- 35	GATE J1,BITS 3-7,TO J3
1A2A06	P03B-08/07	1A2B0-W3*W2	4- 25	PARTIAL WRITE,BITS 00-05
1A2A06	P03B-10/09	1A2B0-U3*U2	4- 25	PARTIAL WRITE,BITS 12-17
1A2A06	P03C-02/01	1A2B0-H3*H2	4- 25	PARTIAL WRITE,BITS 18-23
1A2A06	P03C-04/03	1A2B0-E3*E2	4- 25	PARTIAL WRITE,BITS 06-11
1A2A06	P03C-06*05	1A2B2-N2/N3	4- 35	F0 REG,BIT 1, TO BDP
1A2A06	P03C-08*07	1A2B2-U2/U3	4- 35	F0 REG,BIT 0, TO BDP
1A2A06	P03C-10*09	1B2A2-W1/W0	4- 49	J1 TO J3 BIT 00
1A2A06	P03D-02*01	1B2A2-V1/V0	4- 49	J1 TO J3 BIT 01
1A2A06	P03D-04*03	1B2A2-X1/X0	4- 49	J1 TO J3 BIT 06
1A2A06	P03D-06*05	1B2A2-J0/J1	4- 49	J1 TO J3 BIT 07
1A2A06	P03D-08*07	1B2A2-S1/S0	4- 49	J1 TO J3 BIT 03
1A2A06	P03D-10*09	1B2A3-N0/N1	4- 51	J2 TO J4 BIT 02
1A2A06	P03E-02*01	1B2A3-X3/X2	4- 51	J2 TO J4 BIT 00
1A2A06	P03E-04*03	1B2A2-E0/F1	4- 49	J1 TO J3 BIT 02
1A2A06	P03E-06*05	1B2A2-M1/M0	4- 49	J1 TO J3 BIT 05
1A2A06	P03E-08*07	1B2A2-R1/R0	4- 49	J1 TO J3 BIT 04
1A2A06	P03E-10*09	1B2A3-X0/X1	4- 51	J2 TO J4 BIT 03
1A2A06	P03F-01*	1A2A0-02	4- 27	CC-MR SWITCH IN CC POSITION
1A2A06	P03F-04*03	1B2A3-J0/J1	4- 51	J2 TO J4 BIT 05
1A2A06	P03F-06*05	1B2A3-T0/T1	4- 51	J2 TO J4 BIT 04
1A2A06	P03F-08*07	1B2A3-E0/F1	4- 51	J2 TO J4 BIT 01
1A2A06	P04A-02/01	1A2B7-H1*H0	4- 15	INTERRUPT START + FETCH SIGN 1
1A2A06	P04A-04/03	1A2B8-V2*V3	4- 17	NOT((CONDITION REG=01)(70.0)* (CONDITION REG=10)(70.2))
1A2A06	P04A-06/05	1A2B9-00*01	4- 19	ADD 3 TO P REGISTER
1A2A06	P04A-08*07	1B2A8-S0/S1	4- 69	I9 BIT 07 TO W5, L2, FORCE *
1A2A06	P04A-10*09	1B2A7-M1/M0	4- 67	I9 BIT 14 TO W3, L1, BCD FAULT
1A2A06	P04B-02*01	1B2A7-G1/G0	4- 67	I9 BIT 13 TO W3, L1, CARRY A
1A2A06	P04B-04*03	1B2A7-F0/F1	4- 67	I9 BIT 12 TO W3, L1, 2ND PASS
1A2A06	P04B-06*05	1B2A7-V3/V2	4- 67	I9 BIT 21 TO W3 AND L1
1A2A06	P04B-08*07	1B2A8-M1/M0	4- 69	I9 BIT 04 TO W5, L2, FLTG SIGN
1A2A06	P04B-10*09	1B2A7-I3/I2	4- 67	I9 BIT 19 TO W3 AND L1
1A2A06	P04C-02*01	1B2A8-T0/T1	4- 69	I9 BIT 06 TO W5, L2, FORCE *
1A2A06	P04C-04*03	1B2A7-G2/G3	4- 67	I9 BIT 17 TO W3 AND L1
1A2A06	P04C-06*05	1B2A8-V1/V0	4- 69	I9 BIT 05 TO W5, L2, FORCE $
1A2A06	P04C-08*07	1B2A7-T3/T2	4- 67	I9 BIT 23 TO W3 AND L1
1A2A06	P04C-10*09	1B2A8-W2/W3	4- 69	I9 BIT 00 TO W5, L2, COND REG0
1A2A06	P04D-02*01	1B2A8-X2/X3	4- 69	I9 BIT 01 TO W5, L2, COND REG1
1A2A06	P04D-04*03	1B2A7-S3/S2	4- 67	I9 BIT 22 TO W3 AND L1
1A2A06	P04D-06*05	1B2A7-H3/H2	4- 67	I9 BIT 16 TO W3 AND L1
1A2A06	P04D-08*07	1B2A7-F2/F3	4- 67	I9 BIT 18 TO W3 AND L1
1A2A06	P04D-10*09	1B2A8-E0/F1	4- 69	I9 BIT 02 TO W5, L2, CR OR DB
1A2A06	P04E-02*01	1B2A7-U3/U2	4- 67	I9 BIT 20 TO W3 AND L1
1A2A06	P04E-04*03	1B2A8-F1/F0	4- 69	I9 BIT 03 TO W5, L2, ZERO SUPR
1A2A06	P04E-06*05	1B2A7-L0/L1	4- 67	I9 BIT 15 TO W3 AND L1
1A2A06	P04E-08*07	1B2A8-I2/I3	4- 69	I9 BIT 10 TO W5, L2, SIGNS #
1A2A06	P04E-10*09	1B2A8-J2/J3	4- 69	I9 BIT 11 TO W5, L2, INT START
1A2A06	P04F-02*01	1B2A8-D2/D3	4- 69	I9 BIT 09 TO W5, L2, OPERAND=0
1A2A06	P04F-04*03	1B2A8-E2/E3	4- 69	I9 BIT 08 TO W5, L2, FORC FLTG
1A2A06	P05A-02/01	1B2A0-S1*S0	4- 59	D5 TO I3 BIT 04

CONNECTOR		ORIGIN	PAGE	DEFINITION
1A2A06	P05A-04/03	1B2A0-D0*D1	4- 59	D5 TO I3 BIT 03
1A2A06	P05A-06/05	1B2A0-B1*B0	4- 59	D5 TO I3 BIT 00
1A2A06	P05A-08/07	1B2A0-C1*C0	4- 59	D5 TO I3 BIT 02
1A2A06	P05A-10/09	1B2A0-G1*G0	4- 59	D5 TO I3 BIT 01
1A2A06	P05B-02/01	1B2A0-X1*X0	4- 59	D5 TO I3 BIT 05
1A2A06	P05B-04/03	1B2B0-D0*D1	4- 61	D5 TO I3 BIT 08
1A2A06	P05B-06/05	1B2B0-C1*C0	4- 61	D5 TO I3 BIT 09
1A2A06	P05B-08/07	1B2B0-G1*G0	4- 61	D5 TO I3 BIT 10
1A2A06	P05B-10/09	1B2B0-B1*B0	4- 61	D5 TO I3 BIT 11
1A2A06	P05C-02/01	1B2A0-D2*D3	4- 59	D5 TO I3 BIT 17
1A2A06	P05C-04/03	1B2A0-C3*C2	4- 59	D5 TO I3 BIT 16
1A2A06	P05C-06/05	1B2A0-E2*E3	4- 59	D5 TO I3 BIT 15
1A2A06	P05C-08/07	1B2A0-B3*B2	4- 59	D5 TO I3 BIT 14
1A2A06	P05C-10/09	1B2A0-W3*W2	4- 59	D5 TO I3 BIT 12
1A2A06	P05D-02/01	1B2A0-X3*X2	4- 59	D5 TO I3 BIT 13
1A2A06	P05D-04/03	1B2B0-E2*E3	4- 61	D5 TO I3 BIT 20
1A2A06	P05D-06/05	1B2B0-B3*B2	4- 61	D5 TO I3 BIT 21
1A2A06	P05D-08/07	1B2B0-S1*S0	4- 61	D5 TO I3 BIT 07
1A2A06	P05D-10/09	1B2B0-X1*X0	4- 61	D5 TO I3 BIT 06
1A2A06	P05E-02/01	1B2B0-D2*D3	4- 61	D5 TO I3 BIT 18
1A2A06	P05E-04/03	1B2B0-X3*X2	4- 61	D5 TO I3 BIT 22
1A2A06	P05E-06/05	1B2B0-C3*C2	4- 61	D5 TO I3 BIT 19
1A2A06	P05E-08/07	1B2B0-W3*W2	4- 61	D5 TO I3 BIT 23
1A2A06	P05E-10/09	1B2A6-F3*F2	4- 45	(BUP INSTRUCTION)(NOT A FIELD LEGAL CHARACTER)
1A2A06	P06A-02*01	1B2B1-P3/P2	4- 57	ASCII CHAR BIT 1(BCD TO ASCII)
1A2A06	P06A-04*03	1B2B1-S2/S3	4- 57	ASCII CHAR BIT 2(BCD TO ASCII)
1A2A06	P06A-06*05	1B2B1-W3/W2	4- 57	ASCII CHAR BIT 4(BCD TO ASCII)
1A2A06	P06A-08*07	1B2B1-X3/X2	4- 57	ASCII CHAR BIT 3(BCD TO ASCII)
1A2A06	P06A-10*09	1B2B1-U3/U2	4- 57	ASCII CHAR BIT 6(BCD TO ASCII)
1A2A06	P06B-02*01	1B2B1-Q3/Q2	4- 57	ASCII CHAR BIT 5(BCD TO ASCII)
1A2A06	P06B-04*03	1B2B1-E0/F1	4- 57	BCD CHAR BIT 1 (ASCII TO BCD)
1A2A06	P06B-06*05	1B2B1-B1/B0	4- 57	BCD CHAR BIT 0 (ASCII TO BCD)
1A2A06	P06B-08*07	1B2B1-H3/H2	4- 57	ASCII CHAR BIT 0(BCD TO ASCII)
1A2A06	P06B-10*09	1B2B1-L1/L0	4- 57	BCD CHAR BIT 3 (ASCII TO BCD)
1A2A06	P06C-02*01	1B2B1-I0/I1	4- 57	BCD CHAR BIT 2 (ASCII TO BCD)
1A2A06	P06C-04*03	1B2B1-M0/M1	4- 57	BCD CHAR BIT 4 (ASCII TO BCD)
1A2A06	P06C-06*05	1B2B1-P1/P0	4- 57	BCD CHAR BIT 5 (ASCII TO BCD)
1A2A06	P06C-08/07	1B2A1-G1*G0	4- 53	J3 TO W1 BIT 00
1A2A06	P06C-10/09	1B2A1-F1*F0	4- 53	J3 TO W0 BIT 00
1A2A06	P06D-02/01	1B2A1-I0*I1	4- 53	J3 TO W0 BIT 01
1A2A06	P06D-04/03	1B2A1-P0*P1	4- 53	J3 TO W1 BIT 02
1A2A06	P06D-06/05	1B2A1-F2*F3	4- 53	J3 TO W1 BIT 03
1A2A06	P06D-08/07	1B2A1-01*00	4- 53	J3 TO W0 BIT 02
1A2A06	P06D-10/09	1B2A1-H0*H1	4- 53	J3 TO W1 BIT 01
1A2A06	P06E-02/01	1B2A1-N2*N3	4- 53	J3 TO W1 BIT 05
1A2A06	P06E-04/03	1B2A1-H3*H2	4- 53	J3 TO W1 BIT 04
1A2A06	P06E-06/05	1B2A1-P3*P2	4- 53	J3 TO W0 BIT 05
1A2A06	P06E-08/07	1B2A1-E3*E2	4- 53	J3 TO W0 BIT 03
1A2A06	P06E-10/09	1B2A1-T2*T3	4- 53	J3 TO W0 BIT 04
1A4A06	J02D-02/01	1A0A7-T1*T0	2- 77	B8 BIT 3
1A4A06	J02D-04/03	1A0A7-L2*L3	2- 77	B8 BIT 4
1A4A06	J02D-06/05	1A0A7-S0*S1	2- 77	B8 BIT 5
1A4A06	J02D-08/07	1A0A5-T1*T0	2- 79	B8 BIT 6
1A4A06	J02D-10/09	1A0A5-L2*L3	2- 79	B8 BIT 7
1A4A06	J02E-02/01	1A0A5-S0*S1	2- 79	B8 BIT 8
1A4A06	J02E-04/03	1A0A3-T1*T0	2- 81	B8 BIT 9
1A4A06	J02E-06/05	1A0A3-L2*L3	2- 81	B8 BIT 10
1A4A06	J02E-08/07	1A0A3-S0*S1	2- 81	B8 BIT 11
1A4A06	J02E-10/09	1A0A1-T1*T0	2- 83	B8 BIT 12
1A4A06	J02F-02/01	1A0A1-L2*L3	2- 83	B8 BIT 13
1A4A06	J02F-04/03	1A0A1-S0*S1	2- 83	B8 BIT 14
1A4A06	J04A-02*01	1A0B8-E0/F1	2- 65	NOT MAIN CONTROL READ, BIT 00
1A4A06	J04A-04*03	1A0B8-E0/F1	2- 65	NOT MAIN CONTROL READ, BIT 01
1A4A06	J04A-06*05	1A0B6-W1/W0	2- 65	NOT MAIN CONTROL READ, BIT 02
1A4A06	J04A-08*07	1A0B6-E0/F1	2- 67	NOT MAIN CONTROL READ, BIT 03



CABLE ROUTING

DISPLAY PANEL - A2		
CONNECTOR	ORIGIN/DEST	DEFINITION
J1	2A1A6 - J18	CPU DISPLAY CABLE 1
J2	2A1A6 - J20	CPU DISPLAY CABLE 2
J3	2A1A6 - J22	CPU DISPLAY CABLE 3
J4	ASSY 3 - A2P4	SWITCH LIGHTS
J5	ASSY 5 - A2P5	A REG (BITS 21-23) AND MISC CONT TO/FROM TYPE CHASSIS
A01 — A12		DATA INTERCHANGE AND COMPUTE STATUS DISPLAY DRIVER CONNECTORS

SWITCH PANEL - A3		
CONNECTOR	ORIGIN/DEST	DEFINITION
J1	1A4A6 - J17	CPU SWITCH CABLE
J2	1A4A6 - J15	CPU SWITCH CABLE
A2P4	ASSY 2 - J4	SWITCH LIGHTS
A5P1	ASSY 5 - J1	TYPEWRITER SWITCHES AND MISC CONTROLS
A01		KEYBOARD TRANSLATOR CONNECTOR

LOGIC CHASSIS - A5		
CONNECTOR	ORIGIN/DEST	DEFINITION
J1	A5P1	TYPEWRITER SWITCHES AND MISC CONTROLS
	J3	(PART OF J1 IS JUMPERED TO J3)
J2	(TERMINATOR)	
J3	2A1A6 - J16	TYPEWRITER SWITCHES AND MISC CONTROLS
A2P5	ASSY 2 - J5	A REG (BITS 21-23) AND MISC CONT TO/FROM TYPE CHASSIS
A7P1	ASSY 7 - J1	50-PIN TYPEWRITER CABLE
A00-A07		TYPEWRITER LOGIC CHASSIS CONNECTORS (DTL 50-PAK)

TYPEWRITER - A7		
CONNECTOR	ORIGIN/DEST	DEFINITION
J1	ASSY 5-A7P1	50-PIN TYPEWRITER CABLE

NOTES:

1. THE APPROXIMATE LOCATIONS OF CONSOLE ASSEMBLIES ARE SHOWN BY DASHED LINES.
2. INDEPENDENT CABLE CONNECTOR DESIGNATIONS EXIST FOR EACH CONSOLE ASSEMBLY, E.G., A5J1, A2J1.
3. THE PLUG ENDS OF CONSOLE CABLES (WIRES ENCLOSED IN PLASTIC TUBING) ARE LABELLED IN TERMS OF THE DESTINATION ASSEMBLY, E.G., A PLUG IN ASSEMBLY 3 LABELLED A2P4 CONNECTS TO ASSY 2, J4.
4. CABLING INFORMATION FOR THE CENTRAL PROCESSOR AND STORAGE IS GIVEN IN THE GENERAL INFORMATION SECTION OF THIS MANUAL.
5. ALL CABLE CONNECTORS ARE 61-PIN UNLESS OTHERWISE INDICATED.

CONTROL DATA
DEVELOPMENT DIVISION

TITLE: CONSOLE ASSEMBLY AND CABLING DIAGRAM

PRODUCT

SIZE	DRAWING NO.	REV.
C	60181000	A

SHEET | PAGE 10-1

TABS FOR DISPLAY PANEL

CONNECTOR J1

CPU CONNECTOR	PIN	SIGNAL DEFINITION	CONSOLE CONNECTOR	PIN	DESTINATION
2A1A6-J18	A1	A/Q/E,BIT 00	J1	A1	DS2-5
	A2	A/Q/E,BIT 01		A2	DS2-4
	A3	A/Q/E,BIT 02		A3	DS2-3
	A4	A/Q/E,BIT 03		A4	DS3-5
	A5	A/Q/E,BIT 04		A5	DS3-4
	A6	A/Q/E,BIT 05		A6	DS3-3
	A7	A/Q/E,BIT 06		A7	DS4-5
	A8	A/Q/E,BIT 07		A8	DS4-4
	A9	A/Q/E,BIT 08		A9	DS4-3
	A10	A/Q/E,BIT 09		A10	DS5-5
	B1	A/Q/E,BIT 10		B1	DS5-4
	B2	A/Q/E,BIT 11		B2	DS5-3
	B3	A/Q/E,BIT 12		B3	DS6-5
	B4	A/Q/E,BIT 13		B4	DS6-4
	B5	A/Q/E,BIT 14		B5	DS6-3
	B6	A/Q/E,BIT 15		B6	DS7-5
	B7	A/Q/E,BIT 16		B7	DS7-4
	B8	A/Q/E,BIT 17		B8	DS7-3
	B9	A/Q/E,BIT 18		B9	DS8-5
	B10	A/Q/E,BIT 19		B10	DS8-4
	C1	A/Q/E,BIT 20		C1	DS8-3
	C2	A/Q/E,BIT 21 TO LOGIC		C2	J5-B
	C3	A/Q/E,BIT 22 TO LOGIC		C3	J5-C
	C4	A/Q/E,BIT 23 TO LOGIC		C4	J5-D
	C5	SPARE		C5	
	C6	SPARE		C6	
	C7	A,B,P REG GATE		C7	BUS
	C8	F REG GATE (LOW)		C8	BUS
	C9	F REG GATE (MID)		C9	DS21-6
	C10	F REG GATE (UPPER)		C10	BUS
	D1	SPARE		D1	
	D2	GO		D2	A11-6
	D3	KYBD ACTIVE		D3	J5-A
	D4	SW/EN CONT		D4	A12-1
	D5	STOP		D5	A12-2
	D6	AUTO DUMP		D6	A12-3
	D7	AUTO LOAD		D7	A12-4
	D8	FINISH		D8	A12-5
	D9	REPEAT		D9	A12-6
	D10	DISABLE STO PRO		D10	A10-4
	E1	ENT AUTO PROG		E1	A10-5
	E2	SPARE		E2	
	E3	NOT USED		E3	
	E4			E4	
	E5			E5	
	E6			E6	
	E7			E7	
	E8			E8	
	E9			E9	
	E10	NOT USED		F1	
	F1	SPARE		F2	DS26-7
	F2	$\not\Omega$SR BKGRD LT		F3	DS26-5
	F3	$\not\Omega$SR LT, BIT 0		F4	DS26-4
	F4	$\not\Omega$SR LT, BIT 1		F5	DS26-3
	F5	$\not\Omega$SR LT, BIT 2		F6	DS27-5
	F6	ISR LT, BIT 0		F7	DS27-4
	F7	ISR LT, BIT 1		F8	DS27-3
	F8	ISR LT, BIT 2		F9	
	F9	NOT USED			
2A1A6-J18	F10	NOT USED	J1	F10	

CONNECTOR J2

CPU CONNECTOR	PIN	SIGNAL DEFINITION	CONSOLE CONNECTOR	PIN	DESTINATION
2A1A6-J20	A1	B^b,P,MISC-BIT 00	J2	A1	DS11-5
	A2	B^b,P,MISC-BIT 01		A2	DS11-4
	A3	B^b,P,MISC-BIT 02		A3	DS11-3
	A4	B^b,P,LJA-BIT 03		A4	DS12-5
	A5	B^b,P,LJA-BIT 04		A5	DS12-4
	A6	B^b,P,LJA-BIT 05		A6	DS12-3
	A7	B^b,P,LJA-BIT 06		A7	DS13-5
	A8	B^b,P,LJA-BIT 07		A8	DS13-4
	A9	B^b,P,LJA-BIT 08		A9	DS13-3
	A10	B^b,P,LJA-BIT 09		A10	DS14-5
	B1	B^b,P,LJA-BIT 10		B1	DS14-4
	B2	B^b,P,LJA-BIT 11		B2	DS14-3
	B3	B^b,P,LJA-BIT 12		B3	DS15-5
	B4	B^b,P,LJA-BIT 13		B4	DS15-4
	B5	B^b,P,LJA-BIT 14		B5	DS15-3
	B6	SPARE		B6	
	B7	F + C, BIT 00		B7	DS17-5
	B8	F + C, BIT 01		B8	DS17-4
	B9	F + C, BIT 02		B9	DS17-3
	B10	DIGIT 0 BKGRD LT		B10	DS17-7
	C1	F + C, BIT 03		C1	DS18-5
	C2	F + C, BIT 04		C2	DS18-4
	C3	F + C, BIT 05		C3	DS18-3
	C4	DIGIT 1 BKGRD LT		C4	DS18-7
	C5	F + C, BIT 06		C5	DS19-5
	C6	F + C, BIT 07		C6	DS19-4
	C7	F + C, BIT 08		C7	DS19-3
	C8	DIGIT 2 BKGRD LT		C8	DS19-7
	C9	F + C, BIT 09		C9	DS20-5
	C10	F + C, BIT 10		C10	DS20-4
	D1	F + C, BIT 11		D1	DS20-3
	D2	DIGIT 3 BKGRD LT		D2	DS20-7
	D3	F + C, BIT 12		D3	DS21-5
	D4	F + C, BIT 13		D4	DS21-4
	D5	F + C, BIT 14		D5	DS21-3
	D6	DIGIT 4 BKGRD LT		D6	DS21-7
	D7	F + C, BIT 15		D7	DS22-5
	D8	F + C, BIT 16		D8	DS22-4
	D9	F + C, BIT 17		D9	DS22-3
	D10	DIGIT 5 BKGRD LT		D10	DS22-7
	E1	F + C, BIT 18		E1	DS23-5
	E2	F + C, BIT 19		E2	DS23-4
	E3	F + C, BIT 20		E3	DS23-3
	E4	DIGIT 6 BKGRD LT		E4	DS23-7
	E5	F + C, BIT 21		E5	DS24-5
	E6	F + C, BIT 22		E6	DS24-4
	E7	F + C, BIT 23		E7	DS24-3
	E8	DIGIT 7 BKGRD LT		E8	DS24-7
	E9	NOT USED		E9	
	E10			E10	
	F1			F1	
	F2			F2	
	F3			F3	
	F4			F4	
	F5			F5	
	F6			F6	
	F7			F7	
	F8			F8	
	F9			F9	
2A1A6-J20	F10	NOT USED	J2	F10	

CONNECTOR J3

CPU CONNECTOR	PIN	SIGNAL DEFINITION	CONSOLE CONNECTOR	PIN	DESTINATION
2A1A6-J22	A1	CHAN 2 REJECT	J3	A1	A04-1
	A2	CHAN 3 REJECT		A2	A04-2
	A3	CHAN 4 REJECT		A3	A04-3
	A4	CHAN 5 REJECT		A4	A04-4
	A5	CHAN 6 REJECT		A5	A04-5
	A6	CHAN 7 REJECT		A6	A04-6
	A7	CHAN 0 INT		A7	A02-3
	A8	CHAN 1 INT		A8	A02-4
	A9	CHAN 2 INT		A9	A02-5
	A10	CHAN 3 INT		A10	A02-6
	B1	CHAN 4 INT		B1	A03-1
	B2	CHAN 5 INT		B2	A03-2
	B3	CHAN 6 INT		B3	A03-3
	B4	CHAN 7 INT		B4	A03-4
	B5	CHAN 0 PAR ERR		B5	A01-1
	B6	CHAN 1 PAR ERR		B6	A01-2
	B7	CHAN 2 PAR ERR		B7	A01-3
	B8	CHAN 3 PAR ERR		B8	A01-4
	B9	CHAN 4 PAR ERR		B9	A01-5
	B10	CHAN 5 PAR ERR		B10	A01-6
	C1	CHAN 6 PAR ERR		C1	A02-1
	C2	CHAN 7 PAR ERR		C2	A02-2
	C3	SPARE		C3	
	C4	SPARE		C4	
	C5	SPARE		C5	
	C6	SPARE		C6	
	C7	SPARE		C7	
	C8	MONITOR STATE		C8	A09-1
	C9	PROGRAM STATE		C9	A09-2
	C10	INT ENABLED		C10	A09-3
	D1	READ NEXT INST		D1	A09-4
	D2	READ ADDRESS		D2	A09-5
	D3	READ OPERAND		D3	A09-6
	D4	STORE OPERAND		D4	A10-1
	D5	ARITH OVFL		D5	A07-5
	D6	DIVIDE FAULT		D6	A07-6
	D7	EXP FAULT		D7	A08-1
	D8	BCD FAULT		D8	A08-2
	D9	ILLEGAL WRITE		D9	A08-3
	D10	STO PAR ERR		D10	A08-4
	E1	CHAN 0 READ		E1	A06-3
	E2	CHAN 1 READ		E2	A06-4
	E3	CHAN 2 READ		E3	A06-5
	E4	CHAN 3 READ		E4	A06-6
	E5	CHAN 4 READ		E5	A07-1
	E6	CHAN 5 READ		E6	A07-2
	E7	CHAN 6 READ		E7	A07-3
	E8	CHAN 7 READ		E8	A07-4
	E9	CHAN 0 WRITE		E9	A05-1
	E10	CHAN 1 WRITE		E10	A05-2
	F1	CHAN 2 WRITE		F1	A05-3
	F2	CHAN 3 WRITE		F2	A05-4
	F3	CHAN 4 WRITE		F3	A05-5
	F4	CHAN 5 WRITE		F4	A05-6
	F5	CHAN 6 WRITE		F5	A06-1
	F6	CHAN 7 WRITE		F6	A06-2
	F7	CHAN 0 REJECT		F7	A03-5
	F8	CHAN 1 REJECT		F8	A03-6
	F9	NOT USED		F9	
2A1A6-J22	F10	NOT USED	J3	F10	

CONNECTORS J4 & J5

CONSOLE CONNECTOR	PIN	SIGNAL DEFINITION	CONSOLE CONNECTOR	PIN	DESTINATION
A2P4	A1	GO SWITCH LT	J4	A1	A11-10
	A2	SW/EN CONT SW LT		A2	A12-14
	A3	STOP SWITCH LT		A3	A12-15
	A4	AUTO DUMP SW LT		A4	A12-13
	A5	AUTO LOAD SW LT		A5	A12-12
	A6	FINISH SW LT		A6	A12-11
	A7	REPEAT SW LT		A7	A12-10
	A8	DIS STO PRO SW LT		A8	A10-12
	A9	ENT AUTO PROG SW LT		A9	A10-11
	A10	SPARE		A10	
	B1	SELECT E_L REG		B1	DS10-12
	B2	SELECT A REG		B2	DS10-8
	B3	SELECT Q REG		B3	DS10-10
	B4	SELECT E_U REG		B4	DS10-11
	B5	SELECT P REG		B5	DS16-3
	B6	SELECT B1 REG		B6	DS16-6
	B7	SELECT B2 REG		B7	DS16-7
	B8	SELECT B3 REG		B8	DS16-9
	B9	SELECT LJA REG		B9	DS16-2
	B10	SELECT CIR		B10	DS16-5
	C1	NOT USED		C1	
	D10	NOT USED		D10	
	E1	TYPE LOAD		E1	A11-13
	E2	TYPE DUMP		E2	A11-12
	E3			E3	
	E4			E4	
	E5			E5	
	E6	NOT USED		E6	
	E7	ISR,BIT 0 (SW)		E7	S5-2
	E8	ISR,BIT 1 (SW)		E8	S6-2
	E9	ISR,BIT 2 (SW)		E9	S7-2
	E10	CLR ISR (SW)		E10	S8-2
	F1	$\not\Omega$SR, BIT 0 (SW)		F1	S1-2
	F2	$\not\Omega$SR, BIT 1 (SW)		F2	S2-2
	F3	$\not\Omega$SR, BIT 2 (SW)		F3	S3-2
	F4	CLR $\not\Omega$SR (SW)		F4	S4-2
	F5	NOT USED		F5	
	F6			F6	
	F7			F7	
	F8			F8	
	F9			F9	
A2P4	F10	NOT USED	J4	F10	

CONSOLE CONNECTOR	PIN	SIGNAL DEFINITION	CONSOLE CONNECTOR	PIN	DESTINATION
A2P5	A	KYBD ACTIVE	J5	A	J1-D3
	B	A/Q/E,BIT 21 TO LOGIC		B	J1-C2
	C	A/Q/E,BIT 22 TO LOGIC		C	J1-C3
	D	A/Q/E,BIT 23 TO LOGIC		D	J1-C4
	E	TYPE LOAD		E	A11-3
	F	A/Q/E, BIT 21		F	DS9-5
	H	A/Q/E, BIT 22		H	DS9-4
	J	A/Q/E, BIT 23		J	DS9-3
	K	F REG SEL		K	A10-2
	L	C REG SEL		L	A10-3
	M	STORAGE ACTIVE		M	A08-6
	N	TERM FAULT		N	A08-5
	P	MAINT MODE ACT		P	A10-6
A2P5	R	TYPE DUMP	J5	R	A11-4

(FROM CPU-2, 2A1A6-J18)
ARITHMETIC REGISTER DISPLAY

(FROM ASSY 5-A2P5)
ARITH REG DISPLAY

(FROM ASSY 3-A2P4
ARITH REGISTER SELECT DISPLAY

(FROM CPU-2, 2A1A6-J20)
INDEX AND MISCELLANEOUS REG DISPLAY

(FROM ASSY 3-A2P4)
SELECT INDEX AND MISC REGISTER FOR DISPLAY

J1 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 C1

A/Q/E, BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

J5 F H J 21 22 23

J4 B1 B2 B3 B4 — E_L A Q E_U

J2 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 B1 B2 B3 B4 B5

BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14

J4 B5 B6 B7 B8 B9 B10

P B1 B2 B3 LJA CIR

DS2 DS3 DS4 DS5 DS6 DS7 DS8 DS9 DSI0 DSI1 DSI2 DSI3 DSI4 DSI5 DS16

WIRES CONNECT TO PINS ON OCTAL TRANSLATOR ASSEMBLY (SEE PAGE FOR SCHEMATIC)

ABP - GATE
COMMON
+7 VDC
F - GATE (LOWER)
F - GATE (MIDDLE)
F - GATE (UPPER)

DSI7 DSI8 DSI9 DSI20 DSI21 DSI22 DSI23 DS24 DS25 S1 S2 S3 S4 DS26 S5 S6 S7 S8 DS27

BOUNCING BALL BACKGROUND LIGHT, DIGIT 0

BB 0 BB 1 BB 2 BB 3 BB 4 BB 5 BB 6 BB 7

FOR C, BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

J2 B7 B8 B9 B10 C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 E1 E2 E3 E4 E5 E6 E7 E8

LD DLD — LOCATION A10

INSTRUCTION (F) AND COMMUNICATION (C) REGISTER DISPLAY (FROM CPU-2, 2A1A6-J20)

J5 K L — F C

F AND C REG SELECT DISPLAY (FROM ASSY 5-A2P5)

J4 F1 F2 F3 F4 — ØSR BIT 0, ØSR BIT 1, ØSR BIT 2, CLR ØSR — E7 E8 E9 E10 — ISR BIT 0, ISR BIT 1, ISR BIT 2, CLR ISR

ØSR AND ISR SWITCHES (TO ASSY 3-A2P4)

J1 F6 F7 F8 F3 F4 F5 F2 C10 C9 C8 C7

ØSR AND ISR DISPLAYS, REGISTER GATE CONTROLS (FROM CPU-2, 2A1A6-J18)

J2 SPARE B6

J3 SPARE C6 C5 C4 C3 C7

UPPER BLOWER ASSY A8

TB1 TB5-1 TB5-2

B1 BLOWERS B2

TO POWER ENCLOSURE ASSY A4

TB1 TB7-1 TB7-2 TB6-1 TB6-2

LOCATION A12
LOCATION A01
+6V POWER WIRING FOR A02-A11 IS THE SAME AS SHOWN.

INTEGRATED CIRCUIT DISPLAY DRIVERS MOUNTED ON 3000-TYPE CARDS

(FROM CPU-2 2A1A6-J18)

J1 J4

LOCATION A11

GO D2 A1
SW/EN CONT D4 A2
STOP D5 A3
AUTO DUMP D6 A4
AUTO LOAD D7 A5
FINISH D8 A6
REPEAT D9 A7
DIS STOR PROTECT D10 A8
ENTER AUTO-PROG E1 A9

LOCATION A10
SPARE A10
LOCATION A11
E1
E2

TYPE LOAD
TYPE DUMP

KEYBOARD ACTIVE D3 E
A/Q/E BITS TO LOGIC 21 C2 22 C3 23 C4 — R A B C D

J5 (TO ASSY 5-A2P5)

(TO ASSY 3-A2P4)

DATA INTERCHANGE
(FROM CPU-2, 2A1A6-J22)

PARITY ERROR DSI-A — LOCATION A01 — J3 B5 B6 B7 B8 B9 B10 C1 C2 — CHAN 0 CHAN 1 CHAN 2 CHAN 3 CHAN 4 CHAN 5 CHAN 6 CHAN 7 COM

INTERRUPT DSI-B — LOCATION A02 — J3 A7 A8 A9 A10 B1 B2 B3 B4 — CHAN 0 CHAN 1 CHAN 2 CHAN 3 CHAN 4 CHAN 5 CHAN 6 CHAN 7 COM

REJECT DSI-C — LOCATION A03 — J3 F7 F8 A1 A2 A3 A4 A5 A6 — CHAN 0 CHAN 1 CHAN 2 CHAN 3 CHAN 4 CHAN 5 CHAN 6 CHAN 7 COM

WRITE DSI-D — LOCATION A05 — J3 E9 E10 F1 F2 F3 F4 F5 F6 — CHAN 0 CHAN 1 CHAN 2 CHAN 3 CHAN 4 CHAN 5 CHAN 6 CHAN 7 COM

READ DSI-E — LOCATION A06 — J3 E1 E2 E3 E4 E5 E6 E7 E8 — CHAN 0 CHAN 1 CHAN 2 CHAN 3 CHAN 4 CHAN 5 CHAN 6 CHAN 7 COM

+6V

COMPUTER INTERNAL CONDITIONS
(2A1A6-J22 FROM CPU-2 CONNECTS TO J3, A2P5 FROM ASSY 5 CONNECTS TO J5)

LOCATION A08

ARITH OVERFLOW — DIVIDE FAULT — EXP FAULT — BCD FAULT — ILLEGAL WRITE — STORAGE PARITY ERROR — TERM FAULT — MAINT MODE ACTIVE

DSI-G — LOCATION A07 — J3 D5 D6 D7 D8 D9 D10 N P — J5 — COM

LOCATION A09

STORAGE ACTIVE — MONITOR STATE — PROGRAM STATE — INTERRUPT ENABLE — READ NEXT INST — READ ADDRESS — READ OPERAND — STORE OPERAND

DSI-H — LOCATION A08 — J5 M C8 C9 C10 D1 D2 D3 D4 — LOCATION A10 — COM

INTEGRATED CIRCUIT DISPLAY DRIVERS TYPE DLD MOUNTED ON 3000-TYPE CARDS. SEE PAGE 10-10 FOR LAYOUT OF DRIVER CARD.

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE
SCHEMATIC-CONSOLE DISPLAY PANEL ASSEMBLY A2

PRODUCT
SIZE D | DRAWING NO. 60181000 | REV. G
SHEET | PAGE 10-3

TABS FOR CONSOLE SWITCH PANEL

CONNECTOR J1

CPU CONNECTOR	PIN	SIGNAL* DEFINITION	CONSOLE CONNECTOR	PIN	DESTINATION
1A4A6-J17	A1	BDP MODE	J1	A1	S31-3
	A2	EXEC MODE		A2	S41-3
	A3	SEL JUMP 1		A3	S9-3
	A4	SEL JUMP 2		A4	S8-3
	A5	STO CY STEP		A5	S38-5
	A6	STO CY STEP (NC)		A6	S38-3
	A7	SPARE		A7	
	A8	SPARE		A8	
	A9	SEL STOP		A9	S29-3
	A10	SPARE		A10	
	B1	SELECT A DIS		B1	S4-D1
	B2	SELECT Q DIS		B2	S4-C1
	B3	SELECT E_U DIS		B3	S4-B1
	B4	SELECT E_L DIS		B4	S4-A1
	B5	PAR INT		B5	S30-3
	B6	PAR STOP		B6	S40-3
	B7	SEL JUMP 3		B7	S7-3
	B8	SEL JUMP 4		B8	S16-3
	B9	AUTO STEP		B9	S28-3
	B10	AUTO STEP (NC)		B10	S28-5
	C1	SPARE		C1	
	C2	DIS ADV P		C2	S27-3
	C3	AUTO DUMP		C3	S17-5
	C4	AUTO DUMP (NC)		C4	S17-3
	C5	SPARE		C5	
	C6	SPARE		C6	
	C7	SPARE		C7	
	C8	SELECT P DIS		C8	S5-F1
	C9	SELECT LJA DIS		C9	S5-B1
	C10	SELECT CIR DIS		C10	S5-A1
	D1	SEL JUMP 5		D1	S15-3
	D2	SEL JUMP 6		D2	S14-3
	D3	INST STEP		D3	S37-5
	D4	INST STEP (NC)		D4	S37-3
	D5	EXT CLEAR		D5	S18-5
	D6	INT CLEAR		D6	S19-5
	D7	AUTO LOAD		D7	S32-5
	D8	AUTO LOAD (NC)		D8	S32-3
	D9	COM VOLT LEVEL		D9	TB1-3
	D10	COM VOLT LEVEL		D10	TB1-3
	E1	COM VOLT LEVEL		E1	TB1-6
	E2	COM VOLT LEVEL		E2	TB1-6
	E3	SELECT B1 DIS		E3	S5-E1
	E4	SELECT B2 DIS		E4	S5-D1
	E5	SELECT B3 DIS		E5	S5-C1
	E6	SPARE		E6	
	E7	ISR, BIT 0 TO DIS		E7	A2P4-E7
	E8	ISR, BIT 1 TO DIS		E8	A2P4-E8
	E9	ISR, BIT 2 TO DIS		E9	A2P4-E9
	E10	CLR ISR TO DIS		E10	A2P4-E10
	F1	$\overline{ISR}$, BIT 0 TO DIS		F1	A2P4-F1
	F2	$\overline{ISR}$, BIT 1 TO DIS		F2	A2P4-F2
	F3	$\overline{ISR}$, BIT 2 TO DIS		F3	A2P4-F3
	F4	CLR $\overline{ISR}$ TO DIS		F4	A2P4-F4
	F5	SPARE		F5	
	F6	SPARE			
	F7	SPARE			
	F8	SPARE		F8	
	F9	NOT USED		F9	
1A4A6-J17	F10	NOT USED	J1	F10	

CONNECTOR J2

CPU CONNECTOR	PIN	SIGNAL* DEFINITION	CONSOLE CONNECTOR	PIN	DESTINATION
1A4A6-J15	A1	GO (NC)	J2	A1	S36-3
	A2	GO		A2	S36-5
	A3	STOP (NC)		A3	S35-3
	A4	STOP		A4	S35-5
	A5	MASTER CLR		A5	S20-5
	A6	SPARE		A6	
	A7	SPARE		A7	
	A8	SWEEP PF		A8	S13-C2
	A9	ENTER PF		A9	S13-B2
	A10	KYBD SEL B3		A10	S13-J2
	B1	KYBD SEL B2		B1	S13-K2
	B2	KYBD SEL B1		B2	S13-L2
	B3	KYBD SEL P		B3	S13-M2
	B4	KYBD SEL A		B4	S13-12
	B5	KYBD SEL Q		B5	S13-H2
	B6	ENTER		B6	S13-F2
	B7	SWEEP		B7	S13-G2
	B8	WRITE STO		B8	S13-D2
	B9	READ STO		B9	S13-E2
	B10	SPARE		B10	
	C1	SW/EN CONT (NC)		C1	S26-3
	C2	SW/EN CONT		C2	S26-5
	C3	NO DIGIT SEL (NC)		C3	S23-A2
	C4	DIGIT ZERO SEL		C4	A01-12
	C5	DIGIT, BIT 0		C5	A01-13
	C6	DIGIT, BIT 1		C6	A01-14
	C7	DIGIT, BIT 2		C7	A01-15
	C8	KYBD CLEAR		C8	S25-3
	C9	TRANSFER (NC)		C9	S21-2
	C10	TRANSFER		C10	S21-3
	D1	SPARE		D1	
	D2	SPARE		D2	
	D3	SPARE		D3	
	D4	PWR-ON MC		D4	A5P1-D4
	D5	SPARE		D5	
	D6	SPARE		D6	
	D7	COM VOLT LEVEL		D7	TB1-5
	D8	COM VOLT LEVEL		D8	TB1-5
	D9	BRKPT-BP1		D9	S6-F8
	D10	BRKPT-BP0		D10	S6-F6
	E1	BRKPT-REG		E1	S6-F3
	E2	BRKPT-STO		E2	S6-F1
	E3	SPARE		E3	
	E4	BRKPT,BIT 14		E4	S6-E4
	E5	BRKPT,BIT 13		E5	S6-E6
	E6	BRKPT,BIT 12		E6	S6-E8
	E7	BRKPT,BIT 11		E7	S6-D4
	E8	BRKPT,BIT 10		E8	S6-D6
	E9	BRKPT,BIT 09		E9	S6-D8
	E10	BRKPT,BIT 08		E10	S6-C4
	F1	BRKPT,BIT 07		F1	S6-C6
	F2	BRKPT,BIT 06		F2	S6-C8
	F3	BRKPT,BIT 05		F3	S6-B4
	F4	BRKPT,BIT 04		F4	S6-B6
	F5	BRKPT,BIT 03		F5	S6-B8
	F6	BRKPT,BIT 02		F6	S6-A4
	F7	BRKPT,BIT 01		F7	S6-A6
	F8	BRKPT,BIT 00		F8	S6-A8
	F9	NOT USED		F9	
1A4A6-J15	F10	NOT USED	J2	F10	

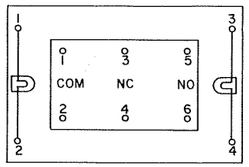
CONNECTOR A2P4

CONSOLE CONNECTOR	PIN	SIGNAL DEFINITION	CONSOLE CONNECTOR	PIN	DESTINATION
ASSY 2-J4	A1	GO SW LT	A2P4	A1	DS36-4
	A2	SW/EN CONT SW LT		A2	DS26-4
	A3	STOP SW LT		A3	DS35-4
	A4	AUTO DUMP SW LT		A4	DS17-4
	A5	AUTO LOAD SW LT		A5	DS32-4
	A6	FINISH SW LT		A6	DS11-4
	A7	REPEAT SW LT		A7	DS2-4
	A8	DIS STO PRO SW LT		A8	DS39-4
	A9	ENT AUTO PROG SW LT		A9	DS33-4
	A10	SPARE		A10	
	B1	SEL E_L DIS LT		B1	S4-A4
	B2	SEL A DIS LT		B2	S4-D4
	B3	SEL Q DIS LT		B3	S4-C4
	B4	SEL E_U DIS LT		B4	S4-B4
	B5	SEL P DIS LT		B5	S5-F4
	B6	SEL B1 DIS LT		B6	S5-E4
	B7	SEL B2 DIS LT		B7	S5-D4
	B8	SEL B3 DIS LT		B8	S5-C4
	B9	SEL LJA DIS LT		B9	S5-B4
	B10	SEL CIR DIS LT		B10	S5-A4
	C1	NOT USED		C1	
	D10	NOT USED		D10	
	E1	TYPE LOAD SW LT		E1	DS10-4
	E2	TYPE DUMP SW LT		E2	DS1-4
	E3	SPARE		E3	
	E4	SPARE		E4	
	E5	SPARE		E5	
	E6	SPARE		E6	
	E7	ISR SW, BIT 0		E7	J1-E7
	E8	ISR SW, BIT 1		E8	J1-E8
	E9	ISR SW, BIT 2		E9	J1-E9
	E10	CLR ISR SW		E10	J1-E10
	F1	$\overline{ISR}$ SW, BIT 0		F1	J1-F1
	F2	$\overline{ISR}$ SW, BIT 1		F2	J1-F2
	F3	$\overline{ISR}$ SW, BIT 2		F3	J1-F3
	F4	CLR $\overline{ISR}$ SW		F4	J1-F4
	F5	NOT USED		F5	
	F6	NOT USED			
	F7	NOT USED			
	F8	NOT USED			
	F9	NOT USED			
ASSY 2-J4	F10	NOT USED	A2P4	F10	

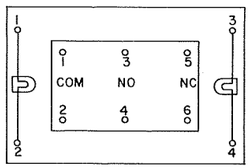
CONNECTOR A5P1

CONSOLE CONNECTOR	PIN	SIGNAL* DEFINITION	CONSOLE CONNECTOR	PIN	DESTINATION
ASSY 5-J1	A1	NOT USED	A5P1	A1	
	B10	NOT USED		B10	
	C1	SPARE		C1	
	C10	SPARE		C10	
	D1	DIS STO PRO		D1	S39-5
	D2	SPARE		D2	
	D3	ENT AUTO PROG		D3	S33-5
	D4	PWR-ON MC		D4	J2-D4
	D5	ENCODE FCN (NC)		D5	S3-5
	D6	AUTO STEP RATE		D6	R1-2
	D7	SPARE		D7	
	D8	SPARE		D8	
	D9	WRITE STO		D9	S13-D2
	D10	SPARE		D10	
	E1	BRKPT,BIT 5		E1	S6-B4
	E2	BRKPT,BIT 4		E2	S6-B6
	E3	BRKPT,BIT 3		E3	S6-B8
	E4	BRKPT,BIT 2		E4	S6-A4
	E5	BRKPT,BIT 1		E5	S6-A6
	E6	BRKPT,BIT 0		E6	S6-A8
	E7	MANUAL INT (NC)		E7	S34-3
	E8	MANUAL INT		E8	S34-5
	E9	TYPE CLEAR (NC)		E9	S12-3
	E10	TYPE CLEAR		E10	S12-5
	F1	FINISH (NC)		F1	S11-3
	F2	FINISH		F2	S11-5
	F3	REPEAT (NC)		F3	S2-3
	F4	REPEAT		F4	S2-5
	F5	TYPE DUMP (NC)		F5	S1-3
	F6	TYPE DUMP		F6	S1-5
	F7	TYPE LOAD (NC)		F7	S10-3
	F8	TYPE LOAD		F8	S10-5
	F9	NOT USED		F9	
ASSY 5-J1	F10	NOT USED	A5P1	F10	

S1	S26
S2	S32
S10	S33
S11	S34
S12	S35
S17	S36
S18	S37
S19	S38
S20	S39



MOMENTARY

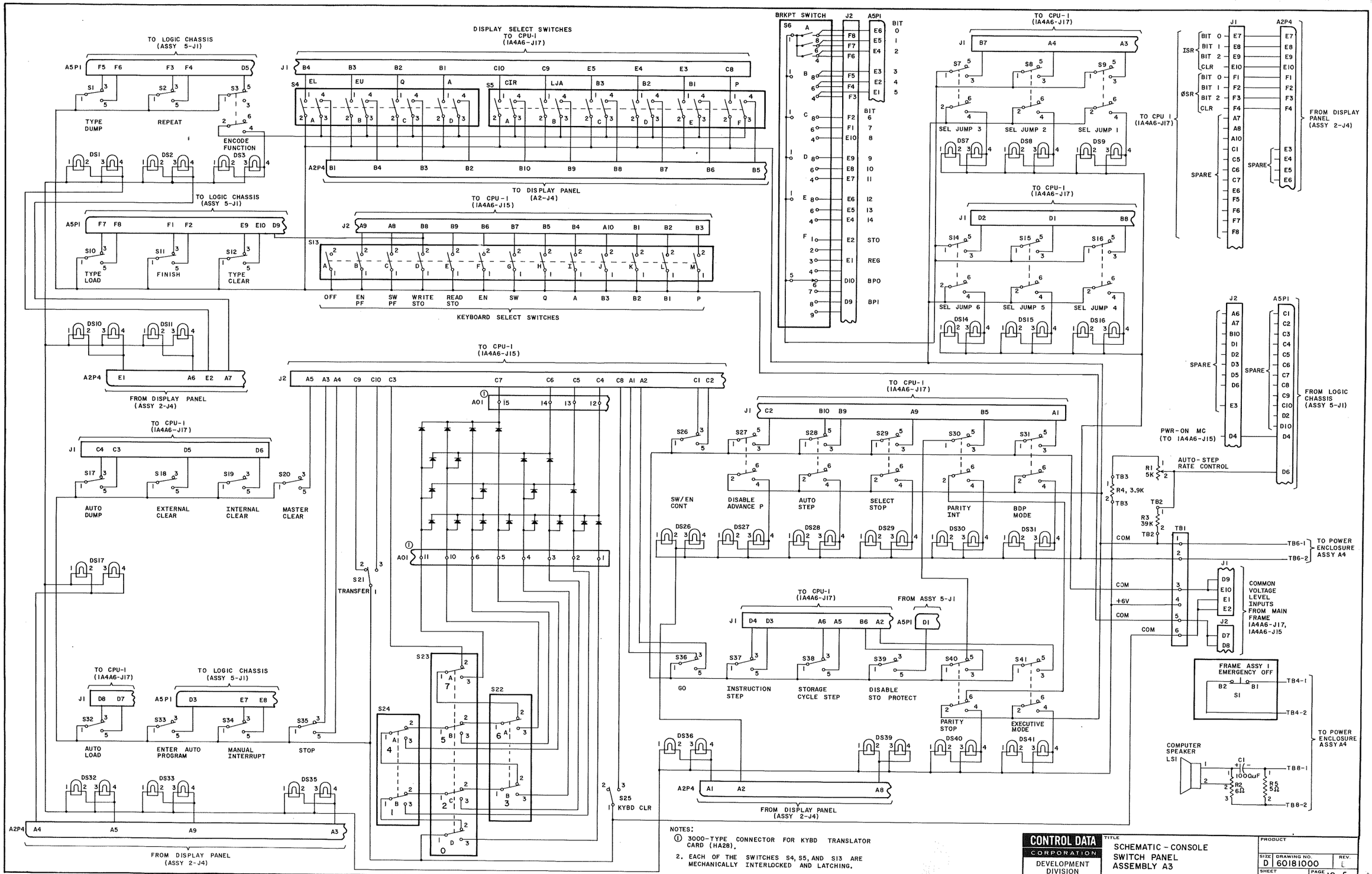


ALTERNATE

S3	S27
S7	S28
S8	S29
S9	S30
S14	S31
S15	S40
S16	S41

TERMINAL DESIGNATIONS FOR INDICATOR/SWITCHES

* SIGNALS RESULT FROM NORMALLY OPEN SWITCH CONTACTS UNLESS OTHERWISE INDICATED (NC).



NOTES:

① 3000-TYPE CONNECTOR FOR KYBD TRANSLATOR CARD (HA28).

2. EACH OF THE SWITCHES S4, S5, AND S13 ARE MECHANICALLY INTERLOCKED AND LATCHING.

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE: SCHEMATIC - CONSOLE SWITCH PANEL ASSEMBLY A3

PRODUCT		
SIZE D	DRAWING NO. 60181000	REV. L
SHEET	PAGE 10-5	

OUTPUT +6V (TO TB1 ON DISPLAY PANEL) + COM TB6

C2 7000 µF 10 V

C4 7000 µF 10 V

OUTPUT +7V (TO TB1 ON DISPLAY PANEL) + COM TB7

C3 7000 µF 10V

TO COMPUTER SPEAKER ON SWITCH PANEL TB8

UPPER BLOWER ASSEMBLY A8 TB5

BLOWER ASSEMBLY – A6 TB1 B1 B2

CHASSIS ASSY A5 TB2

CR18 CR13 CR14 CR15 CR16 CR17

CR24 CR19 CR20 CR21 CR22 CR23

CR6 CR5 CR4 CR3 CR2 CR1

CR10 CR11 CR12 CR7 CR8 CR9

C5 4000 µF 50V

K3

METER ASSY M1 2KΩ R1 1 MA MOVEMENT (77Ω) WITH EXT MULTIPLIER BOARD 6490Ω R2 E1

S2

TB2: -45 V, -6V, COM, +6V, – TERM. POWER +

T4 T6 T3 T5 T2 T1

TB1: DRIVE FROM LOGIC CHASSIS; MAINT MODE LIGHT; POWER-ON MASTER CLEAR; MAINT MODE ENABLE; MAINT MODE GROUND; TIME METER CONTROL; TERMINATOR FAULT; TYPE FUNCTION

R1 2Ω R2 7Ω

THERMAL RELAY K5 CR25 CR26

KEY-OPERATED MAINT SWITCH S1A

K4 K3 K1 K2

KEY-OPERATED SWITCH S1B

TB10

R5 470Ω 1W

OPERATING TIME METER TT2

MAINT TIME METER TT1

C1 1 µF 300V

CR27 CR28

R4 470 Ω 1W

TB9

CB1 1 AMP

FROM EMERGENCY OFF SWITCH TB4

J1 TO TYPEWRITER MOTOR

TB3 N FRAME GROUND TO EMERGENCY OFF PANEL

120 VAC 60~ INPUT

CB2 1 AMP

TB2 N ØA ØB ØC 208/120 VAC 400~ INPUT

TB1 – + 40VDC TERM INPUT; LOGIC GROUND

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE: SCHEMATIC – CONSOLE POWER SUPPLIES, ASSEMBLY A4	PRODUCT	
		SIZE D	DRAWING NO. 60181000
		REV. E	
		SHEET	PAGE 10-7

449

TABS FOR TYPEWRITER LOGIC CHASSIS

CONNECTOR J1

CONSOLE CONNECTOR	PIN	SIGNAL* DEFINITION	CONSOLE CONNECTOR	PIN	DESTINATION
A5P1	A1	NOT USED	J1	A1	
FROM SWITCH PANEL	C10	NOT USED		C10	
	D1	DIS STO PRO SW		D1	J3-D1
	D2	NOT USED		D2	
	D3	ENT AUTO PROG SW		D3	J3-D3
	D4	PWR-ON MC		D4	TB1-5
	D5	ENCODE FCN SW		D5	A02-C1
	D6	AUTO STEP RATE		D6	A05-B0
	D7	SPARE		D7	
	D8	SPARE		D8	
	D9	WRITE STO		D9	J3-D9
	D10	SPARE		D10	
	E1	BRKPT, BIT 5		E1	J3-E1
	E2	BRKPT, BIT 4		E2	J3-E2
	E3	BRKPT, BIT 3		E3	J3-E3
	E4	BRKPT, BIT 2		E4	J3-E4
	E5	BRKPT, BIT 1		E5	J3-E5
	E6	BRKPT, BIT 0		E6	J3-E6
	E7	MAN. INT (NC)		E7	J3-E7
	E8	MAN. INT		E8	J3-E8
	E9	TYPE CLR (NC)		E9	J3-E9
	E10	TYPE CLR		E10	J3-E10
	F1	FINISH (NC)		F1	J3-F1
	F2	FINISH		F2	J3-F2
	F3	REPEAT (NC)		F3	J3-F3
	F4	REPEAT		F4	J3-F4
	F5	TYPE DUMP (NC)		F5	J3-F5
	F6	TYPE DUMP		F6	J3-F6
	F7	TYPE LOAD (NC)		F7	J3-F7
	F8	TYPE LOAD		F8	J3-F8
	F9	NOT USED		F9	
A5P1	F10	NOT USED	J1	F10	

CONNECTOR J2

CONSOLE CONNECTOR	PIN	SIGNAL* DEFINITION	CONSOLE CONNECTOR	PIN	DESTINATION
TERMINATOR	A1	TYPE DATA,BIT 0	J2	A1	A04-D1
	A2	TYPE DATA,BIT 0	TYPE-WRITER CABLE TERMINATION	A2	A04-D0
	A3	TYPE DATA,BIT 1		A3	A04-I1
	A4	TYPE DATA,BIT 1		A4	A04-I0
	A5	TYPE DATA,BIT 2		A5	A04-Q0
	A6	TYPE DATA,BIT 2		A6	A04-Q1
	A7	TYPE DATA,BIT 3		A7	A04-Q1
	A8	TYPE DATA,BIT 3		A8	A04-Q0
	A9	TYPE DATA,BIT 4		A9	A04-W1
	A10	TYPE DATA,BIT 4		A10	A04-W0
	B1	TYPE DATA,BIT 5		B1	A04-V2
	B2	TYPE DATA,BIT 5		B2	A04-V3
	B3	CONTROL BUSY		B3	A07-N1
	B4	CONTROL BUSY		B4	A07-N0
	B5	INPUT READY		B5	A07-W0
	B6	INPUT READY		B6	A07-W1
	B7	TYPE LOAD		B7	A04-I0
	B8	TYPE LOAD		B8	A07-I1
	B9	TYPE DUMP		B9	A07-H1
	B10	TYPE DUMP		B10	A07-H0
	C1	OUTPUT READY		C1	A07-D1
	C2	OUTPUT READY		C2	A07-D0
	C3	CLOCK PULSE		C3	A05-J0
	C4	CLOCK PULSE		C4	A05-J1
	C5	AUTO-STEP OSC		C5	A05-E0
	C6	AUTO-STEP OSC		C6	A05-E1
	C7	STORAGE ACT		C7	A07-N3
	C8	STORAGE ACT		C8	A07-N2
	C9	NOT USED		C9	
	F8	NOT USED		F8	
	F9	TERM PWR (+)		F9	TB2-8
TERMINATOR	F10	TERM PWR (-)	J2	F10	TB2-7

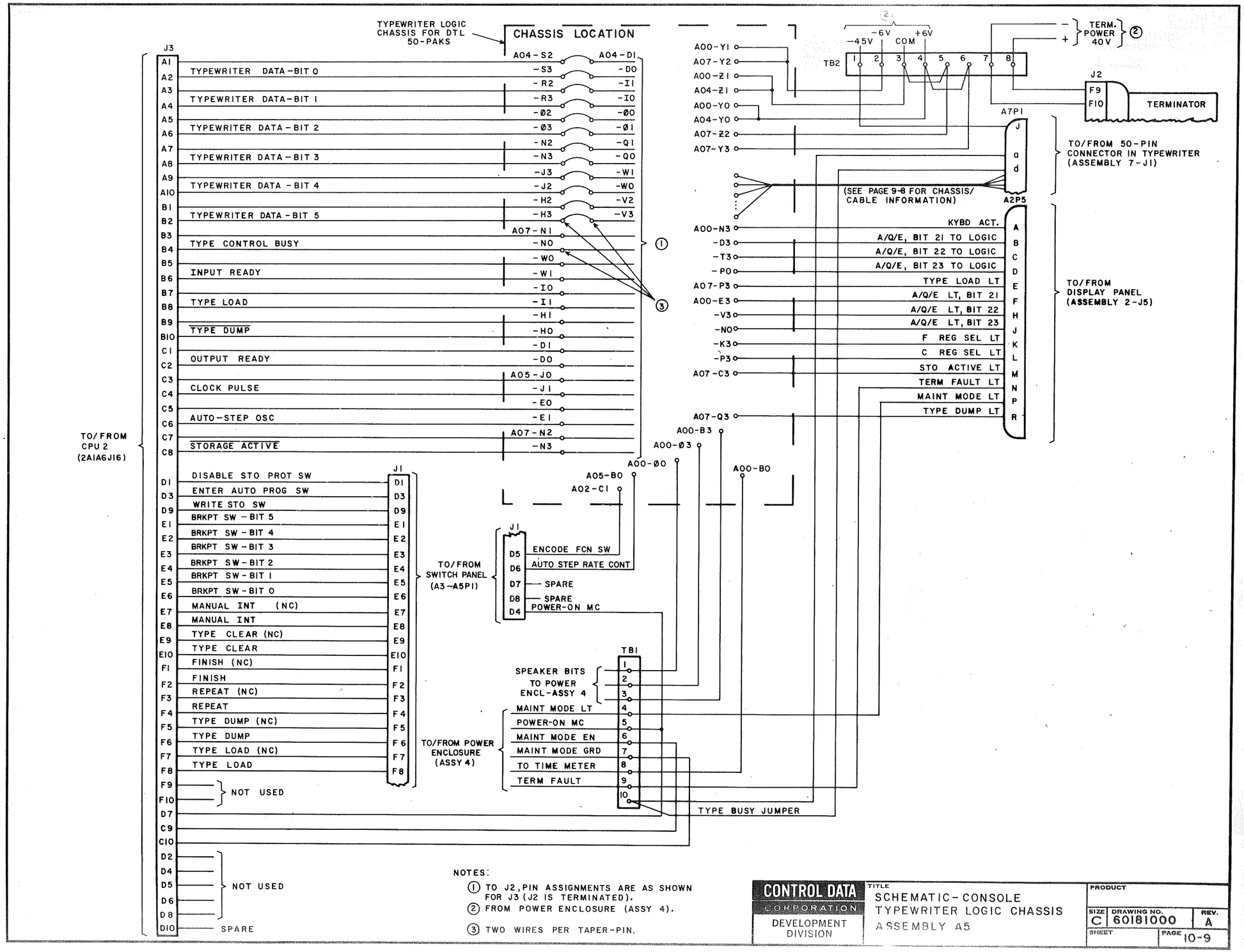
CONNECTOR J3

CPU CONNECTOR	PIN	SIGNAL* DEFINITION	CONSOLE CONNECTOR	PIN	DESTINATION
2A1A6-J16	A1	TYPE DATA,BIT 0	J3	A1	A04-S2
	A2	TYPE DATA,BIT 0		A2	A04-S3
	A3	TYPE DATA,BIT 1		A3	A04-R2
	A4	TYPE DATA,BIT 1		A4	A04-R3
	A5	TYPE DATA,BIT 2		A5	A04-D2
	A6	TYPE DATA,BIT 2		A6	A04-D3
	A7	TYPE DATA,BIT 3		A7	A04-N2
	A8	TYPE DATA,BIT 3		A8	A04-N3
	A9	TYPE DATA,BIT 4		A9	A04-J3
	A10	TYPE DATA,BIT 4		A10	A04-J2
	B1	TYPE DATA,BIT 5		B1	A04-H2
	B2	TYPE DATA,BIT 5		B2	A04-H3
	B3	CONTROL BUSY		B3	A07-N1
	B4	CONTROL BUSY		B4	A07-N0
	B5	INPUT READY		B5	A07-W0
	B6	INPUT READY		B6	A07-W1
	B7	TYPE LOAD		B7	A07-I0
	B8	TYPE LOAD		B8	A07-I1
	B9	TYPE DUMP		B9	A07-H1
	B10	TYPE DUMP		B10	A07-H0
	C1	OUTPUT READY		C1	A07-D1
	C2	OUTPUT READY		C2	A07-D0
	C3	CLOCK PULSE		C3	A05-J0
	C4	CLOCK PULSE		C4	A05-J1
	C5	AUTO-STEP OSC		C5	A05-E0
	C6	AUTO-STEP OSC		C6	A05-E1
	C7	STORAGE ACT		C7	A07-N3
	C8	STORAGE ACT		C8	A07-N2
	C9	MAINT MODE EN		C9	TB1-6
	C10	MAINT MODE GRD		C10	TB1-7
	D1	DIS STO PROT SW		D1	J1-D1
	D2	NOT USED		D2	
	D3	ENT AUTO PROG		D3	J1-D3
	D4	NOT USED		D4	
	D5	NOT USED		D5	
	D6	NOT USED		D6	
	D7	PWR-ON MC		D7	TB1-5
	D8	NOT USED		D8	
	D9	WRITE STO		D9	J1-D9
	D10	SPARE		D10	
	E1	BRKPT, BIT 5		E1	J1-E1
	E2	BRKPT, BIT 4		E2	J1-E2
	E3	BRKPT, BIT 3		E3	J1-E3
	E4	BRKPT, BIT 2		E4	J1-E4
	E5	BRKPT, BIT 1		E5	J1-E5
	E6	BRKPT, BIT 0		E6	J1-E6
	E7	MAN. INT (NC)		E7	J1-E7
	E8	MAN. INT		E8	J1-E8
	E9	TYPE CLEAR (NC)		E9	J1-E9
	E10	TYPE CLEAR		E10	J1-E10
	F1	FINISH (NC)		F1	J1-F1
	F2	FINISH		F2	J1-F2
	F3	REPEAT (NC)		F3	J1-F3
	F4	REPEAT		F4	J1-F4
	F5	TYPE DUMP (NC)		F5	J1-F5
	F6	TYPE DUMP		F6	J1-F6
	F7	TYPE LOAD (NC)		F7	J1-F7
	F8	TYPE LOAD		F8	J1-F8
	F9	NOT USED		F9	
2A1A6-J16	F10	NOT USED	J3	F10	

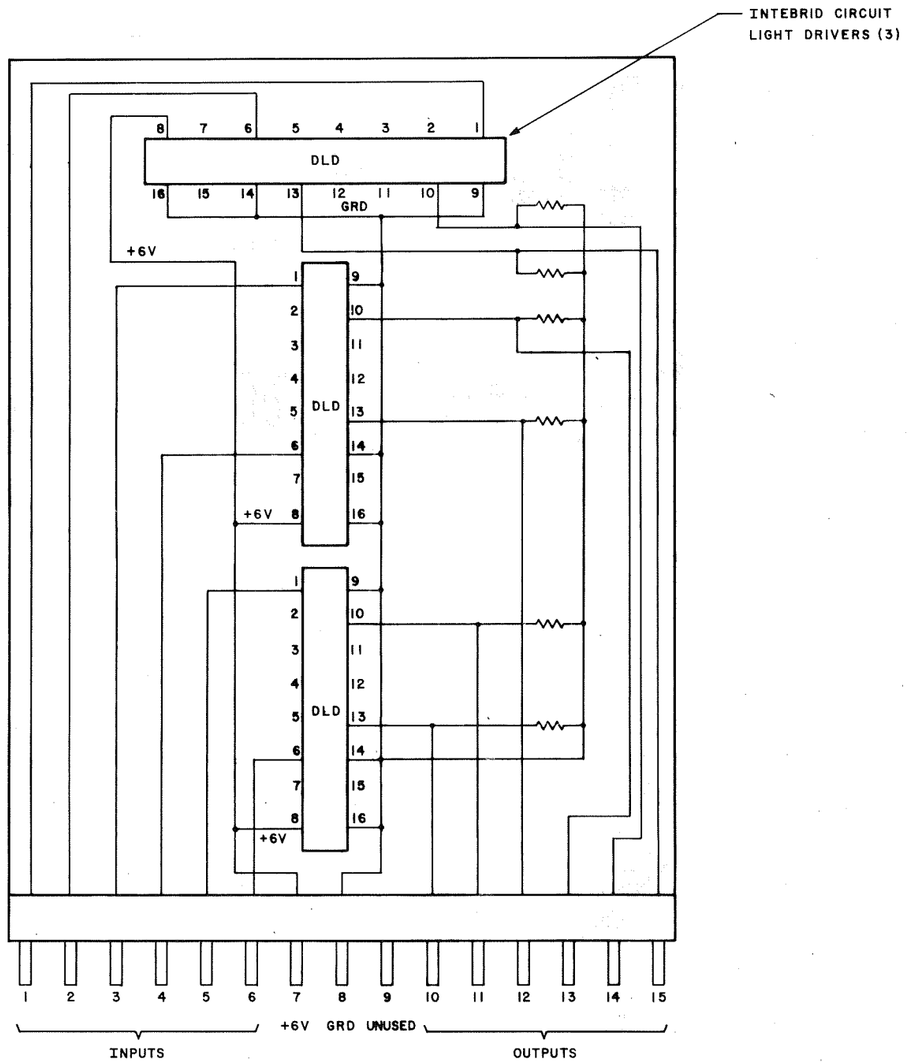
CONNECTOR J4

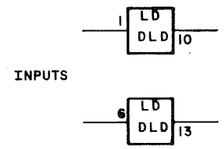
TYPE CONNECTOR	PIN	SIGNAL DEFINITION	CONSOLE CONNECTOR	PIN	CHASSIS DESTINATION
ASSY 7-J1	A	PRINT MAG,BIT 0	A7P1	A	A00-X3
	B	PRINT MAG,BIT 2		B	A00-L3
	C	PRINT MAG,BIT 1		C	A00-R3
	D	PRINT MAG,BIT 4		D	A00-I3
	E	PRINT MAG,BIT 5		E	A00-C3
	F	PRINT MAG,BIT 3		F	A00-F3
	H	TO PARITY MAG		H	A00-C0
	J	-45V PWR		J	TB2-1
	K	TO KYBD LOCK MAG		K	A00-U3
	L	TO TAB MAGNET		L	A00-L0
	M	TO SPACE MAG		M	A00-F0
	N	TO BACKSPACE MAG		N	A00-I0
	P	TO CRG RET MAG		P	A00-X0
	R	NOT USED		R	
	S	TO U.C.SHIFT MAG		S	A00-R0
	T	TO L.C.SHIFT MAG		T	A00-U0
	U	NOT USED		U	
	V	NOT USED		V	
	W	TIMING CONT C1		W	A07-I3
	X	GROUND		X	A05-A1
	Y	TYPE BUSY		Y	A07-C1
	Z	L.CASE STATUS		Z	A02-A3
	a	CONTACTS C2-C6		a	TB1-10
	b	NOT USED		b	
	c	NOT USED		c	
	d	INTERLOCK CONTS			TB1-10
	e	NOT USED			
	f	END OF LINE			A02-U1
	h	NOT USED		h	
	j			j	
	k			k	
	m			m	
	n			n	
	p	NOT USED		p	
	r	BIT 0 FROM TW		r	A04-A0
	s	BIT 2 FROM TW		s	A04-K1
	t	BIT 1 FROM TW		t	A04-N0
	u	BIT 3 FROM TW		u	A04-W3
	v	BIT 5 FROM TW		v	A04-U2
	w	BIT 4 FROM TW		w	A04-U1
	x	NOT USED		x	
	y	GROUND		y	A05-A2
	z	TAB SWITCH		z	A02-C0
	AA	SPACE SWITCH		AA	A02-E0
	BB	BACKSPACE SW		BB	A02-I1
	CC	CRG RTN SW		CC	A02-D0
	DD	NOT USED		DD	
	EE	U.CASE SWITCH		EE	A02-G1
	FF	L.CASE SWITCH		FF	A02-F1
ASSY 7-J1	HH	NOT USED	A7P1	HH	
ASSY 2-J5	A	KYBD ACTIVE	A2P5	A	A00-N3
	B	A/Q/E,BIT 21 TO LOGIC		B	A00-D3
	C	A/Q/E,BIT 22 TO LOGIC		C	A00-T3
	D	A/Q/E,BIT 23 TO LOGIC		D	A00-P0
	E	TYPE LOAD LT		E	A07-Q3
	F	A/Q/E LT, BIT 21		F	A00-E3
	H	A/Q/E LT, BIT 22		H	A00-V3
	J	A/Q/E LT, BIT 23		J	A00-N0
	K	F REG SEL LT		K	A00-K3
	L	C REG SEL LT		L	A00-P3
	M	STO ACTIVE LT		M	A07-C3
	N	TERM FAULT LT		N	TB1-9
	P	MAINT MODE ACT LT		P	TB1-4
ASSY 2-J5	R	TYPE DUMP LT	A2P5	R	A07-C3

* SIGNALS RESULT FROM NORMALLY OPEN SWITCH CONTACTS UNLESS OTHERWISE INDICATED (NC).

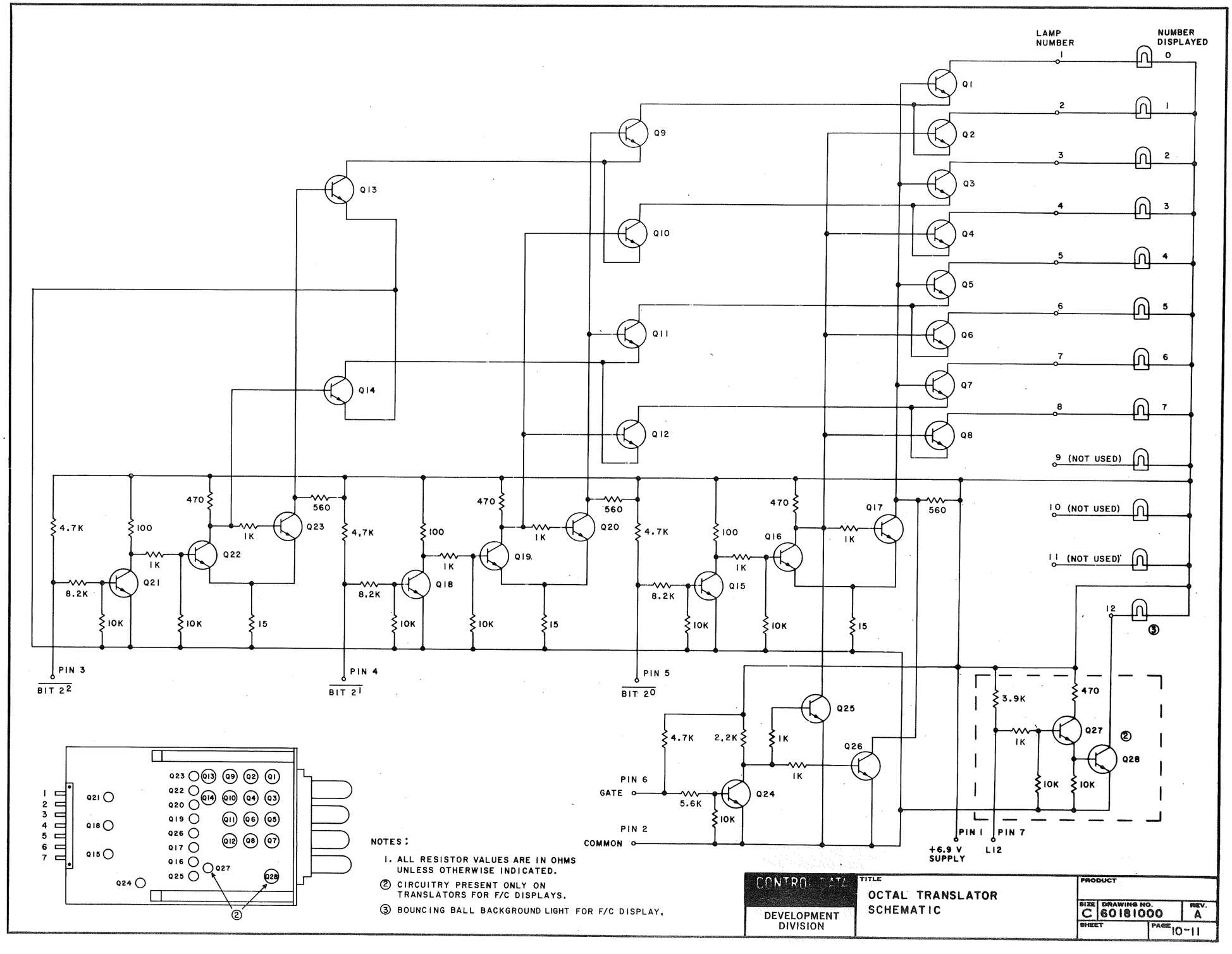

TYPEWRITER LOGIC CHASSIS FOR DTL 50-PAKS
CHASSIS LOCATION
J3
TYPEWRITER DATA-BIT 0
TYPEWRITER DATA-BIT 1
TYPEWRITER DATA-BIT 2
TYPEWRITER DATA-BIT 3
TYPEWRITER DATA-BIT 4
TYPEWRITER DATA-BIT 5
TYPE CONTROL BUSY
INPUT READY
TYPE LOAD
TYPE DUMP
OUTPUT READY
CLOCK PULSE
AUTO-STEP OSC
STORAGE ACTIVE
TO/FROM CPU 2 (2A1A6J16)
DISABLE STO PROT SW
ENTER AUTO PROG SW
WRITE STO SW
BRKPT SW - BIT 5
BRKPT SW - BIT 4
BRKPT SW - BIT 3
BRKPT SW - BIT 2
BRKPT SW - BIT 1
BRKPT SW - BIT 0
MANUAL INT (NC)
MANUAL INT
TYPE CLEAR (NC)
TYPE CLEAR
FINISH (NC)
FINISH
REPEAT (NC)
REPEAT
TYPE DUMP (NC)
TYPE DUMP
TYPE LOAD (NC)
TYPE LOAD
NOT USED
NOT USED
SPARE
J1
TO/FROM SWITCH PANEL (A3-A5P1)
ENCODE FCN SW
AUTO STEP RATE CONT
SPARE
SPARE
POWER-ON MC
TBI
SPEAKER BITS TO POWER ENCL-ASSY 4
MAINT MODE LT
POWER-ON MC
MAINT MODE EN
MAINT MODE GRD
TO TIME METER
TERM FAULT
TO/FROM POWER ENCLOSURE (ASSY 4)
TYPE BUSY JUMPER
TB2
-6V
+6V
-4.5V
COM
TERM. POWER 40V
J2
F9
F10
TERMINATOR
A7P1
TO/FROM 50-PIN CONNECTOR IN TYPEWRITER (ASSEMBLY 7-J1)
(SEE PAGE 9-8 FOR CHASSIS/ CABLE INFORMATION)
A2P5
KYBD ACT.
A/Q/E, BIT 21 TO LOGIC
A/Q/E, BIT 22 TO LOGIC
A/Q/E, BIT 23 TO LOGIC
TYPE LOAD LT
A/Q/E LT, BIT 21
A/Q/E LT, BIT 22
A/Q/E LT, BIT 23
F REG SEL LT
C REG SEL LT
STO ACTIVE LT
TERM FAULT LT
MAINT MODE LT
TYPE DUMP LT
TO/FROM DISPLAY PANEL (ASSEMBLY 2-J5)
NOTES:
1 TO J2, PIN ASSIGNMENTS ARE AS SHOWN FOR J3 (J2 IS TERMINATED).
2 FROM POWER ENCLOSURE (ASSY 4).
3 TWO WIRES PER TAPER-PIN.
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
TITLE
SCHEMATIC - CONSOLE TYPEWRITER LOGIC CHASSIS ASSEMBLY A5
PRODUCT
SIZE C
DRAWING NO. 60181000
REV. A
SHEET
PAGE 10-9

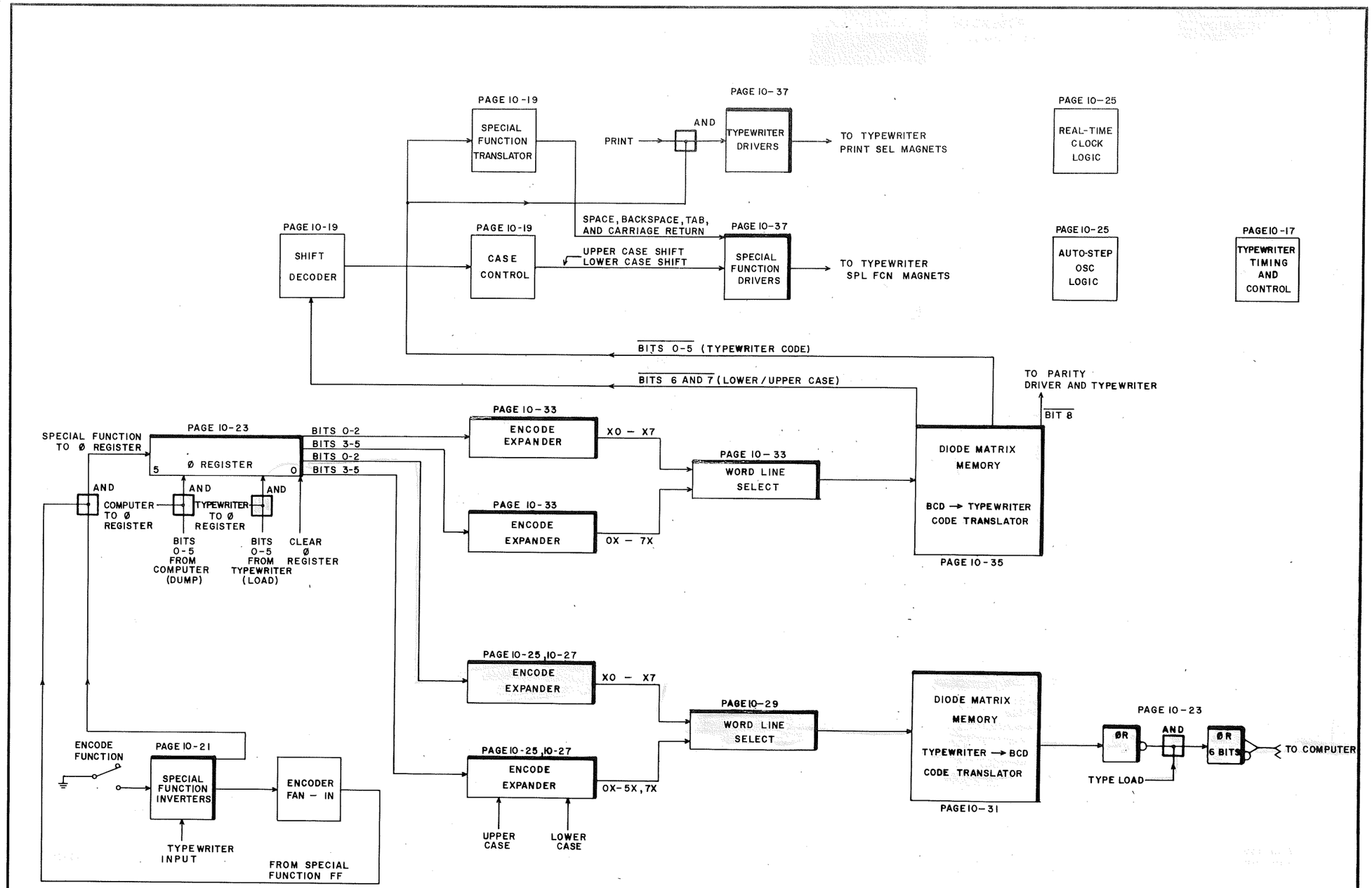
451





CONTROL DATA DEVELOPMENT DIVISION	LIGHT DRIVER CARD	EQUIPMENT	
		SIZE C	DRAWING NO. 60181000 REV. A
		SHEET	PAGE 10-10


LAMP NUMBER
NUMBER DISPLAYED
1
0
2
1
3
2
4
3
5
4
6
5
7
6
8
7
9 (NOT USED)
10 (NOT USED)
11 (NOT USED)
12
③
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
4.7K
100
470
1K
560
8.2K
10K
15
2.2K
5.6K
3.9K
PIN 3
BIT 2²
PIN 4
BIT 2¹
PIN 5
BIT 2⁰
PIN 6
GATE
PIN 2
COMMON
PIN 1
+6.9 V SUPPLY
PIN 7
L12
NOTES:
1. ALL RESISTOR VALUES ARE IN OHMS UNLESS OTHERWISE INDICATED.
② CIRCUITRY PRESENT ONLY ON TRANSLATORS FOR F/C DISPLAYS.
③ BOUNCING BALL BACKGROUND LIGHT FOR F/C DISPLAY.
CONTROL DATA
DEVELOPMENT DIVISION
TITLE
OCTAL TRANSLATOR SCHEMATIC
PRODUCT
SIZE C
DRAWING NO. 60181000
REV. A
SHEET
PAGE 10-11



CONTROL DATA
DEVELOPMENT DIVISION

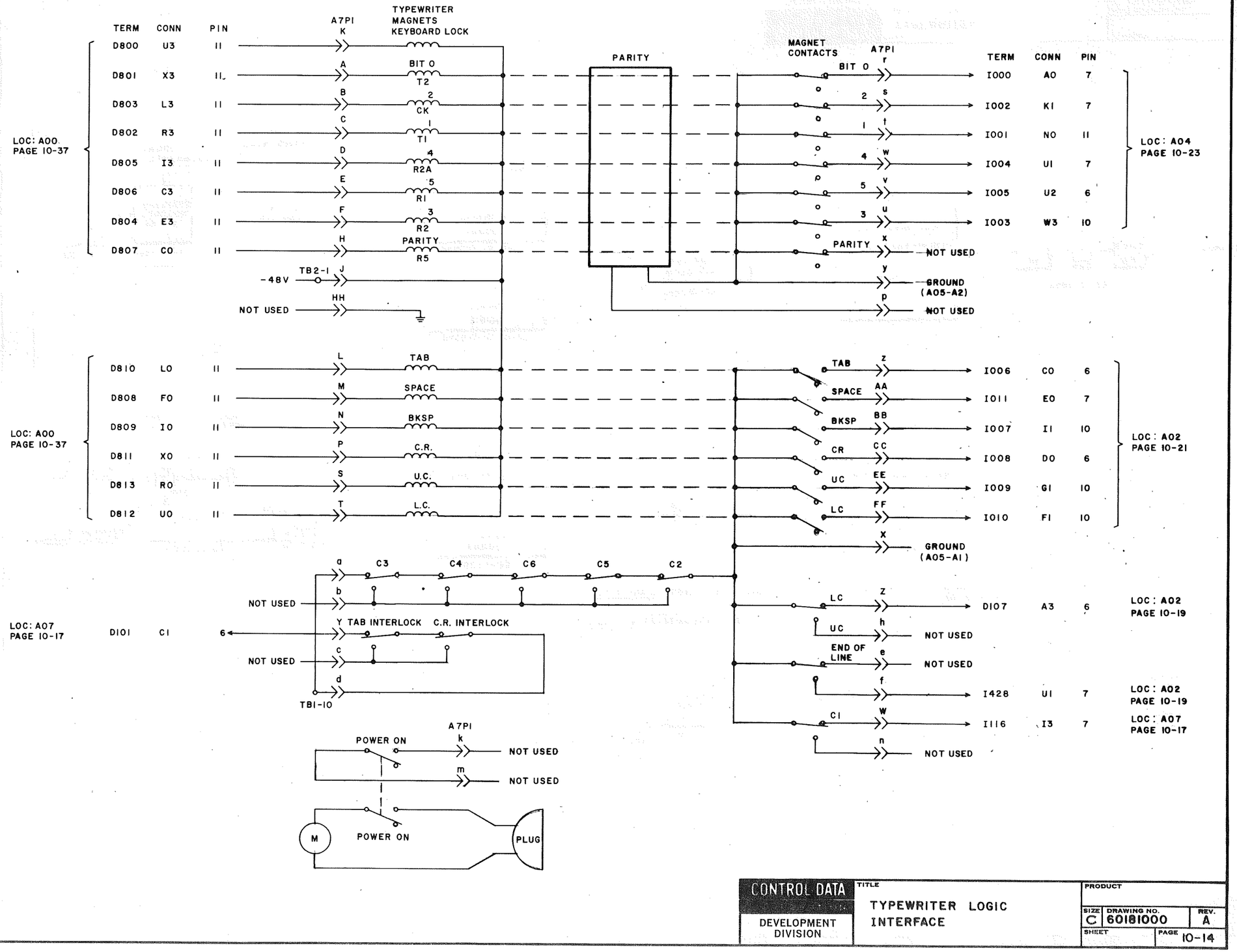
TITLE
TYPEWRITER
BLOCK DIAGRAM

PRODUCT

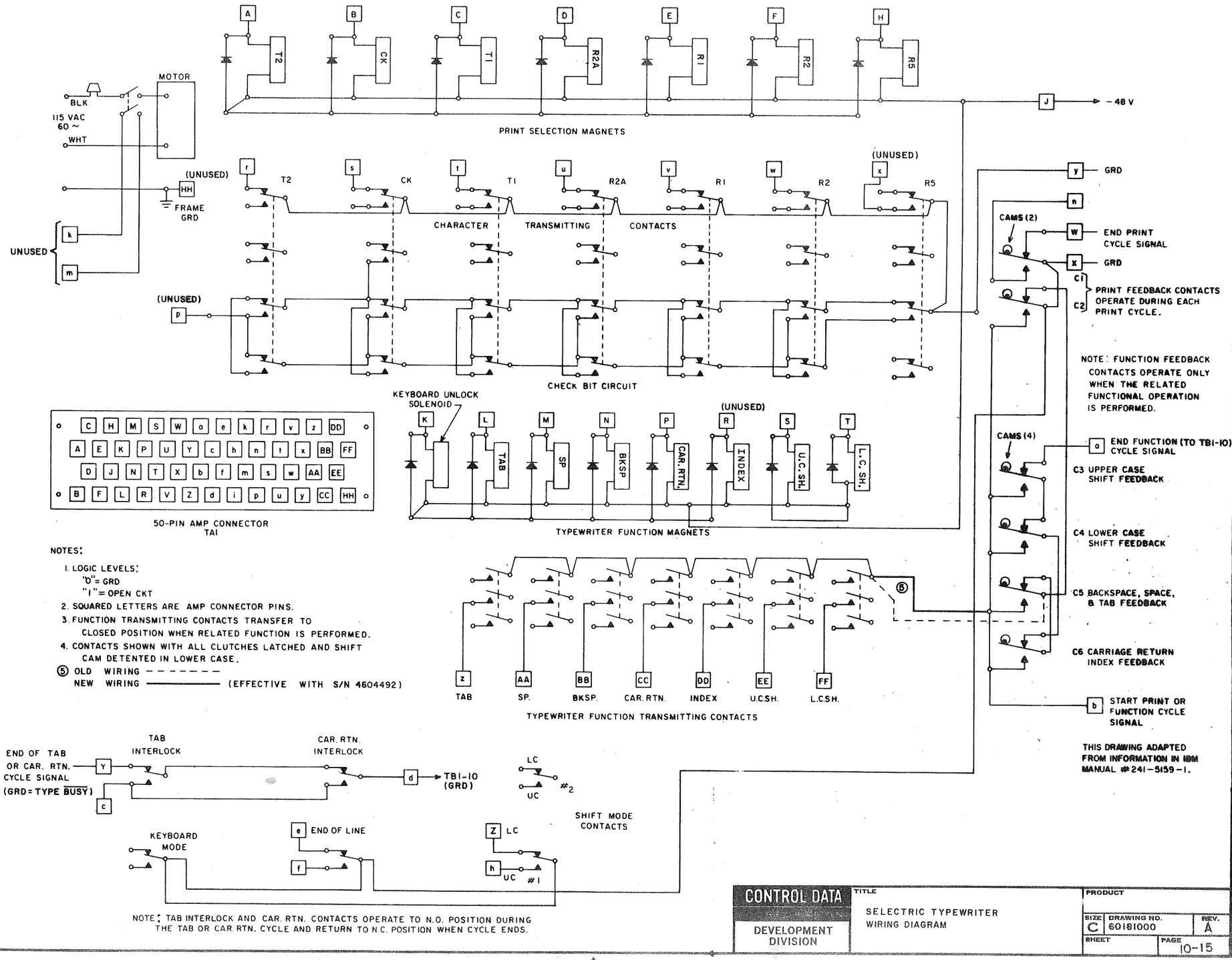
SIZE	DRAWING NO.	REV.
C	60181000	A

SHEET PAGE 10-13

455



CONTROL DATA DEVELOPMENT DIVISION	TITLE TYPEWRITER LOGIC INTERFACE	PRODUCT	
		SIZE C · DRAWING NO. 60181000	REV. A
		SHEET	PAGE 10-14

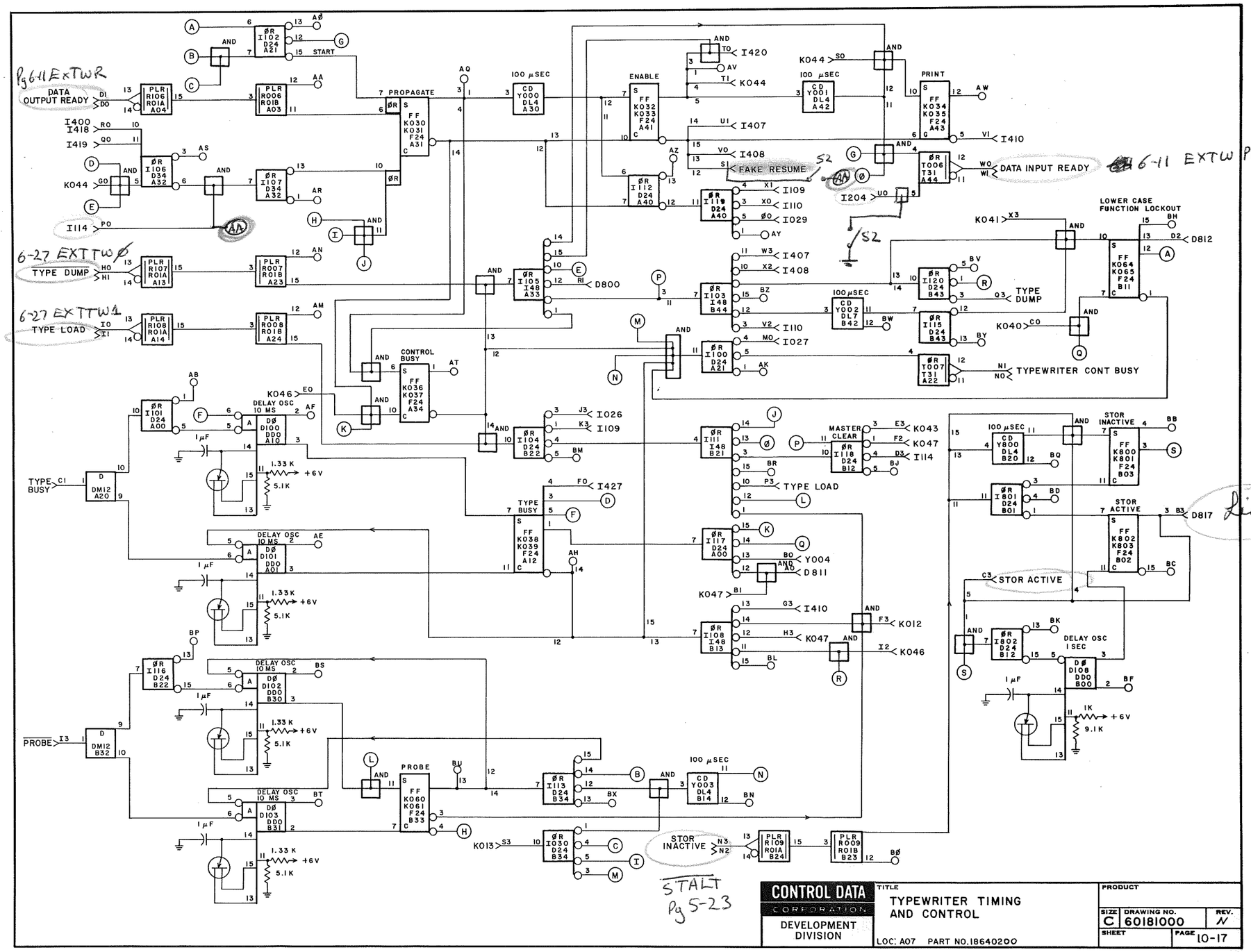


1. LOGIC LEVELS:
   "0" = GRD
   "1" = OPEN CKT
2. SQUARED LETTERS ARE AMP CONNECTOR PINS.
3. FUNCTION TRANSMITTING CONTACTS TRANSFER TO CLOSED POSITION WHEN RELATED FUNCTION IS PERFORMED.
4. CONTACTS SHOWN WITH ALL CLUTCHES LATCHED AND SHIFT CAM DETENTED IN LOWER CASE.

⑤ OLD WIRING - - - - - - -
NEW WIRING ——— (EFFECTIVE WITH S/N 4604492)

CONTROL DATA	TITLE	PRODUCT
DEVELOPMENT DIVISION	SELECTRIC TYPEWRITER WIRING DIAGRAM	SIZE C · DRAWING NO. 60181000 · REV. A · SHEET · PAGE 10-15

A0	A00-X1	10-37	(CRG RET)(TYPE NOT BUSY)
B0	A02-J3	10-19	TYPE NOT BUSY
B1	A02-V1	10-19	AUTO. CRG RET
B3	A00-C1	10-37	STORAGE ACTIVE
C0	A02-S3	10-19	LWR CASE STATUS
C1	A7P1-Y		TYPE BUSY
C3	A2P5-M		STORAGE ACTIVE
D0	A5J2/J3 C-2		
	2A1A6J15/J16 C-2		
	2B1B8-W2	6-11	
D1	A5J2/J3 C-1		TW DATA READY TO BC
	2A1A6J15/J16 C-1		
	2B1B8-W3	6-11	
D2	A00-V0	10-37	LWR CASE FCN LOCKOUT
D3	A02-P3	10-19	MASTER CLEAR
E0	A02-X0	10-19	NOT AUTO. CRG RET.
E3	A02-X3	10-19	MASTER CLEAR
F0	A02-Q3	10-19	TYPE BUSY
F2	A02-W1	10-19	MASTER CLEAR
F3	A02-B1	10-21	(TW LOAD)(TW BUSY)(NOT PROBE)
G0	A02-R2	10-19	NOT CHANGE CASE
G3	A02-N1	10-19	TYPE BUSY
H0	A5J2/J3 B-10		NOT TYPE DUMP
	2A1A6J15/J16 B-10		
	2B1B9-I3	6-27	
H1	A5J2/J3 B-9		
	2A1A6J15/J16 B-9		
	2B1B9-I2	6-27	
H3	A02-X2	10-19	TYPE BUSY
I0	A5J2/J3 B-7		TYPE LOAD
	2A1A6J15/J16 B-7		
	2B1B9-H2	6-27	
I1	A5J2/J3 B-8		
	2A1A6J15/J16 B-8		
	2B1B9-H3	6-27	
I2	A02-W0	10-19	(TW BUSY)(TW DUMP)
I3	A7P1-W		FROM TW TIMING CONTACT C-1
J3	A04-C3	10-23	CONT BUSY + NOT TYPE LOAD
K3	A04-K0	10-23	CONT BUSY + NOT TYPE LOAD
M0	A04-F0	10-23	TYPE CONT BUSY
N0	A5J2/J3 B-4		
	2A1A6J15/J16 B-4		
	2B1B8-X1	6-11	
N1	A5J2/J3 B-3		TW CONTROL BUSY
	2A1A6J15/J16 B-3		
	2B1B8-X0	6-11	
N2	A5J2/J3 C-7		
	2A1A6J15/J16 C-7		
	2A2B9-X2	5-23	
N3	A5J2/J3 C-8		STORAGE INACTIVE
	2A1A6J15/J16 C-8		
	2A2B9-X3	5-23	
O0	A04-F1	10-23	NOT DATA TO 0 REGISTER
P0	S1-2		FROM AUTO-STEP SW
P0	A02-P2	10-19	AUTO-STEP
P3	A5J1D-07		TYPE LOAD
Q0	A02-X1	10-19	SHIFT TO LWR CASE
Q3	A5J01D-08		TYPE DUMP
R0	A02-L0	10-19	SHIFT TO UP. CASE
R1	A00-W2	10-37	TW CONT BUSY + TYPE DUMP
S0	A02-R3	10-19	NOT CHANGE CASE
S1	S1-1		FAKE RESUME
S3	A02-A0	10-21	SPECIAL FUNCTION
T0	A02-V0	10-19	(TW EN)(TW DUMP + CONT BUSY)
T1	A02-U3	10-19	TW ENABLE
U0	S1-6		FROM AUTO STEP SW
U0	A05-A0	10-25	AUTO-STEP
U1	A02-U2	10-19	NOT TW ENABLE
U3	A07-I3	10-17	FROM TW TIMING CONTACT C-1
V0	A02-M3	10-19	NOT TW ENABLE
V1	A02-O0	10-19	NOT PRINT
V2	A04-U0	10-23	NOT TYPE DUMP
W0	A5J2/J3 B-5		EXT TW PRIO REQ ON TW LOAD
	2A1A6J15/J16 B-5		
	2B1B8-M0	6-11	
W1	A5J2/J3 B-6		
	2A1A6J15/J16 B-6		
	2B1B8-M1	6-11	
W3	A02-T3	10-19	NOT TYPE DUMP
X0	A04-V1	10-23	NOT DATA TO 0 REGISTER
X1	A04-M1	10-23	NOT DATA TO 0 REGISTER
X2	A02-L3	10-19	NOT TYPE DUMP
X3	A02-V2	10-19	UP. CASE STATUS



Pg 6-11 EXTW

6-27 EXTTW0

6-27 EXTTW1

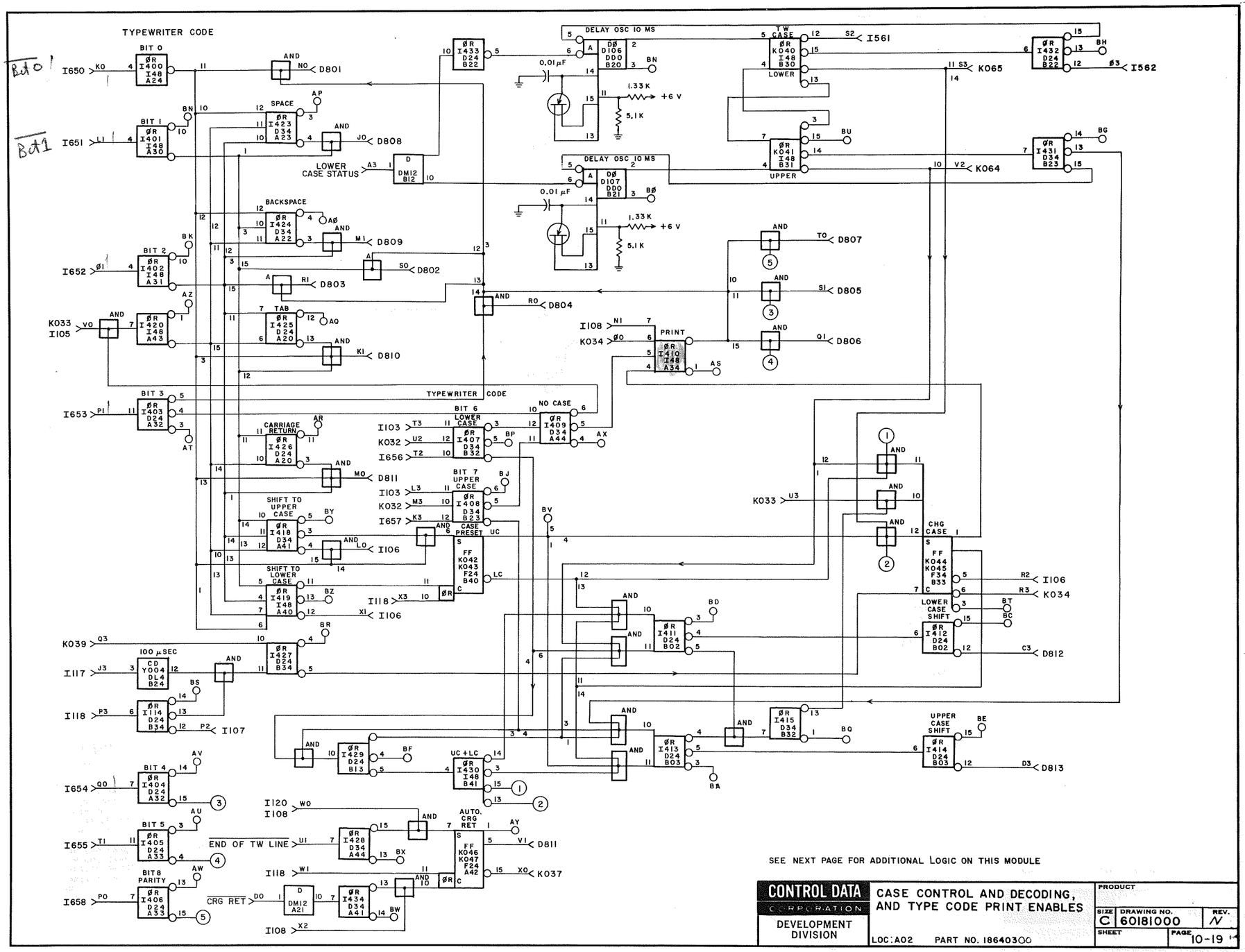
6-11 EXTW PR

Light

STALT Pg 5-23

463

S2 Fake Resume Switch in console

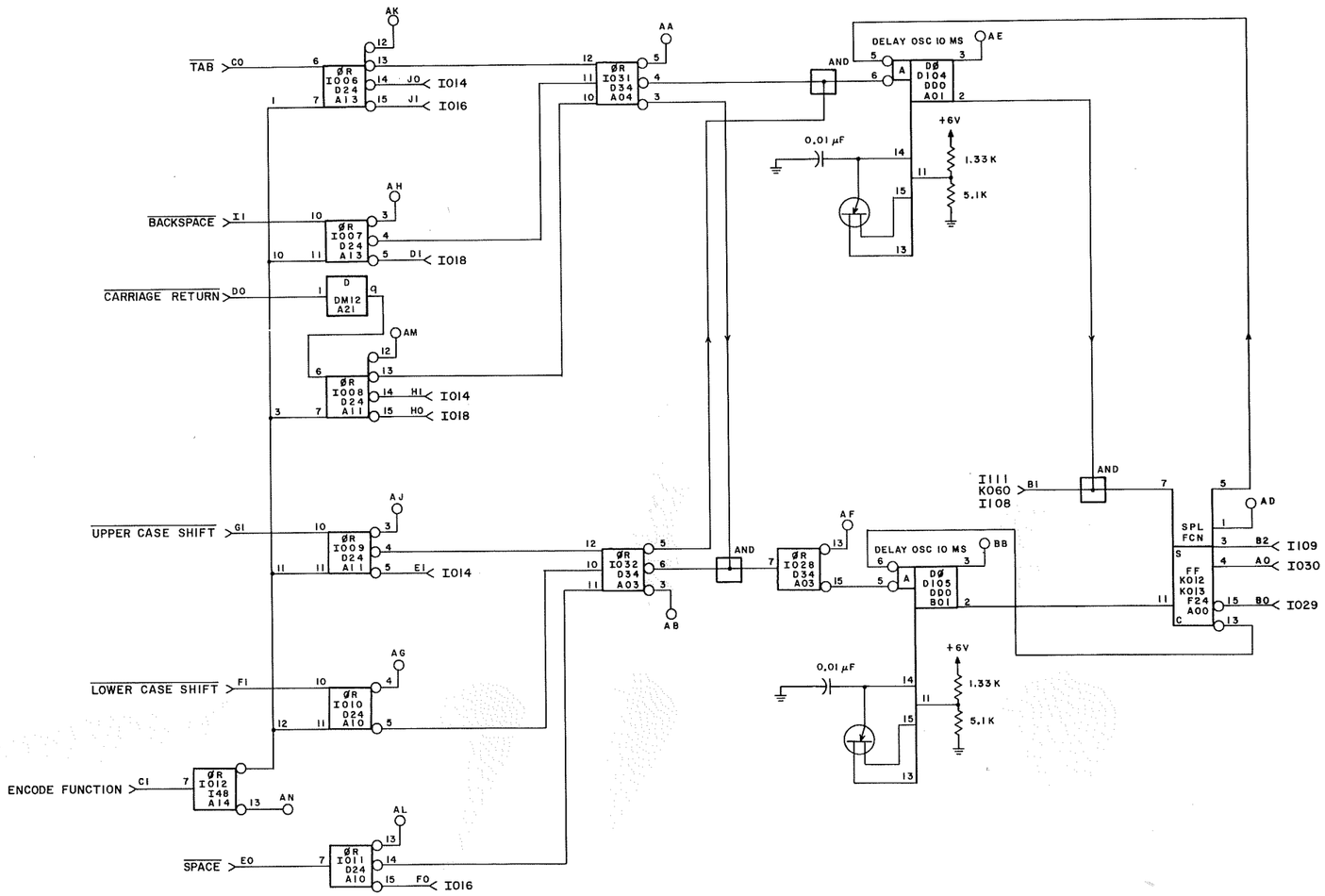


*	DO A02-DO	10-21	NOT CRG RET.
	A3	A7P1-Z	LWR CASE STATUS FROM SW
	C3	A00-V1	10-37 LOWER CASE SHIFT
	D3	A00-S0	10-37 UPPER CASE SHIFT
	J0	A00-E0	10-37 (TYPE CODE NOT BIT 1)(SPACE)
	J3	A07-B0	10-17 TYPE NOT BUSY
	K0	A03-B0	10-35 BCD TO TW CODE - NOT BIT 0
	K1	A00-K0	10-37 (TYPE CODE NOT BIT 0)(TYPE CODE NOT BIT 1)(TAB)
	K3	A03-C0	10-35 BCD TO TW CODE - NOT UP. CASE
	L0	A07-R0	10-17 SHIFT TO UP. CASE
	L1	A03-E0	10-35 BCD TO TW CODE - NOT BIT 1
	L3	A07-X2	10-17 NOT TYPE DUMP
	M0	A00-W1	10-37 (TYPE CODE NOT BIT 0)(TYPE CODE NOT BIT 2)(CRG RET)
	M1	A00-M0	10-37 (TYPE CODE NOT BIT 2)(BKSP)
	M3	A07-V0	10-17 NOT TW ENABLE
	N0	A00-W3	10-37 (TYPE CODE NOT BIT 0)(PRINT)
	N1	A07-G3	10-17 TYPE BUSY
	O0	A07-V1	10-17 NOT PRINT
	O1	A03-E1	10-35 BCD TO TW CODE - NOT BIT 2
	O3	A06-B3	10-27 NOT LWR CASE STATUS
	P0	A03-D0	10-35 BCD TO TW CODE - NOT PARITY
	P1	A03-D1	10-35 BCD TO TW CODE - NOT BIT 3
	P2	A07-P0	10-17 TYPE LOAD + TYPE DUMP
	P3	A07-D3	10-17 MASTER CLEAR
	Q0	A03-C1	10-35 BCD TO TW CODE - NOT BIT 4
	Q1	A00-B2	10-37 (TYPE CODE NOT BIT 5)(PRINT)
	Q3	A07-F0	10-17 TYPE BUSY
	R0	A00-H3	10-37 (TYPE CODE NOT BIT 3)(PRINT)
	R1	A00-M3	10-37 (TYPE CODE NOT BIT 2)(PRINT)
	R2	A07-G0	10-17 NOT CHANGE CASE
	R3	A07-S0	10-17 NOT CHANGE CASE
	S0	A00-S3	10-37 (TYPE CODE NOT BIT 1)(PRINT)
	S1	A00-G3	10-37 (TYPE CODE NOT BIT 4)(PRINT)
	S2	A06-C2	10-27 LWR CASE STATUS
	S3	A07-C0	10-17 LWR CASE STATUS
	T0	A00-D0	10-37 PARITY
	T1	A03-B1	10-35 BCD TO TW CODE - NOT BIT 5
	T2	A03-A0	10-35 BCD TO TW CODE - NOT LWR CASE
	T3	A07-W3	10-17 NOT TYPE DUMP
	U1	A7P1-F	NOT END OF TW LINE
	U2	A07-U1	10-17 NOT TW ENABLE
	U3	A07-T1	10-17 TW ENABLE
	V0	A07-T0	10-17 (TW EN)(TW DUMP + CONT BUSY)
	V1	A07-B1	10-17 AUTO. CRG RET.
	V2	A07-X3	10-17 UP. CASE STATUS
	W0	A07-I2	10-17 (TYPE BUSY)(TW DUMP)
	W1	A07-F2	10-17 MASTER CLEAR
	X0	A07-E0	10-17 NOT AUTO. CRG RET.
	X1	A07-Q0	10-17 SHIFT TO LWR CASE
	X2	A07-H3	10-17 TYPE BUSY
	X3	A07-E3	10-17 MASTER CLEAR

* TERM NOT IN ORDER

CONTROL DATA CORPORATION	DEVELOPMENT DIVISION	CASE CONTROL AND DECODING, AND TYPE CODE PRINT ENABLES	LOC:A02 PART NO. 18640300
PRODUCT	SIZE C	DRAWING NO. 60181000	REV. N
SHEET	PAGE 10-19		

465



A0 A07-S3	10-17	SPECIAL FCN
B0 A04-C0	10-23	NOT SPECIAL FCN
B1 A07-F3	10-17	(TW BUSY) (NOT PROBE) (TYPE LOAD)
B2 A04-V0	10-23	SPECIAL FCN
C0 A7P1-Z*		FROM TAB CONTACT
C1 A5,J010-05		FROM ENCODE FCN SW
D0 A7P1-CC		FROM CRG RET. CONTACT
D0 A02-U0	10-19	NOT CRG RET.
D1 A04-P1	10-23	BACKSPACE
E0 A7P1-AA		FROM SPACE CONTACT
E1 A04-C1	10-23	UPPER CASE SHIFT
F0 A04-H1	10-23	SPACE
F1 A7P1-FF		FROM LWR CASE SHIFT CONTACT
G1 A7P1-EE		FROM UP. CASE SHIFT CONTACT
H0 A04-P0	10-23	CARRIAGE RETURN
H1 A04-B1	10-23	CARRIAGE RETURN
I0 A04-B0	10-23	TAB
I1 A7P1-BB		FROM BACKSPACE CONTACT
J1 A04-H0	10-23	TAB

* LOWER CASE Z

SEE PREVIOUS PAGE FOR ADDITIONAL LOGIC ON THIS MODULE

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

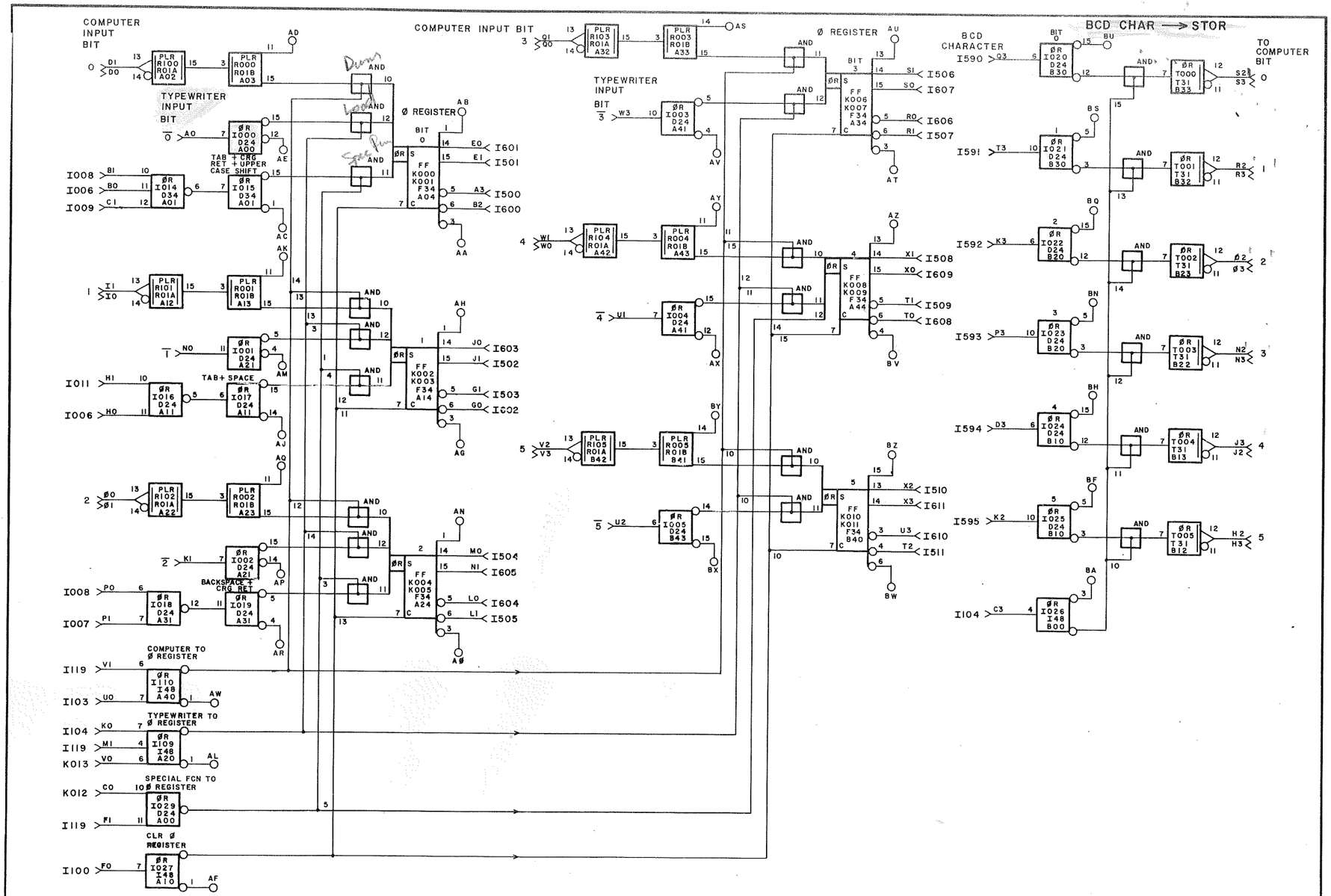
TITLE: SPECIAL FUNCTION
LOC: A02 PART NO. 18640300

PRODUCT
SIZE C | DRAWING NO. 60181000 | REV. N
SHEET | PAGE 10-21

A0	A7P1-R		NOT BIT 0 FROM TW
A3	A05-N2	10-25	O REG NOT BIT 0
B0	A02-I0	10-21	TAB
B1	A02-H1	10-21	CARRIAGE RETURN
B2	A03-E3	10-33	O REG NOT BIT 0
C0	A02-B0	10-21	NOT SPECIAL FCN
C1	A02-E1	10-21	UPPER CASE SHIFT
C3	A07-J3	10-17	CONT BUSY + NOT TYPE LOAD
D0	A5J2/J3 A-2		TW O REG BIT 00 FROM BC
	A04-S3		
	2A1A6J15/J16 A-2		
	2B1B9-D0	6-27	
D1	A5J2/J3 A-1		
	A04-S2		
	2A1A6J15/J16 A-1		
	2B1B9-D1	6-27	
D3	A06-E0	10-31	TYPE TO BCD CODE - NOT BIT 4
E0	A03-C2	10-33	O REG BIT 0
E1	A05-T3	10-25	O REG BIT 0
F0	A07-M0	10-17	TYPE CONT BUSY
F1	A07-00	10-17	NOT DATA TO O REGISTER
G0	A03-D3	10-33	O REG NOT BIT 1
G1	A05-X3	10-25	O REG NOT BIT 1
H0	A02-J1	10-21	TAB
H1	A02-F0	10-21	SPACE
H2	A5J2/J3 B-1		TW O REG BIT 05
	A04-V2		
	2A1A6J15/J16 B-1		
	2B1B9-W0	6-27	
H3	A5J2/J3 B-2		
	A04-V3		
	2A1A6J15/J16 B-2		
	2B1B9-W1	6-27	
I0	A5J2/J3 A-4		
	A04-R3		
	2A1A6J15/J16 A-4		
	2B1B9-G1	6-27	
I1	A5J2/J3 A-3		TW O REG BIT 01 FROM BC
	A04-R2		
	2A1A6J15/J16 A-3		
	2B1B9-G0	6-27	
J0	A03-B2	10-33	O REG BIT 1
J1	A05-U2	10-25	O REG BIT 1
J2	A5J2/J3 A-10		
	A04-W0		
	2A1A6J15/J16 A-10		
	2B1B9-X1	6-27	
J3	A5J2/J3 A-9		TW O REG BIT 04
	A04-W1		
	2A1A6J15/J16 A-9		
	2B1B9-X0	6-27	
K0	A07-K3	10-17	CONT BUSY + NOT TYPE LOAD
K1	A7P1-S		NOT BIT 2 FROM TW
K2	A06-B0	10-31	TYPE TO BCD CODE - NOT BIT 5
K3	A06-D1	10-31	TYPE TO BCD CODE - NOT BIT 2

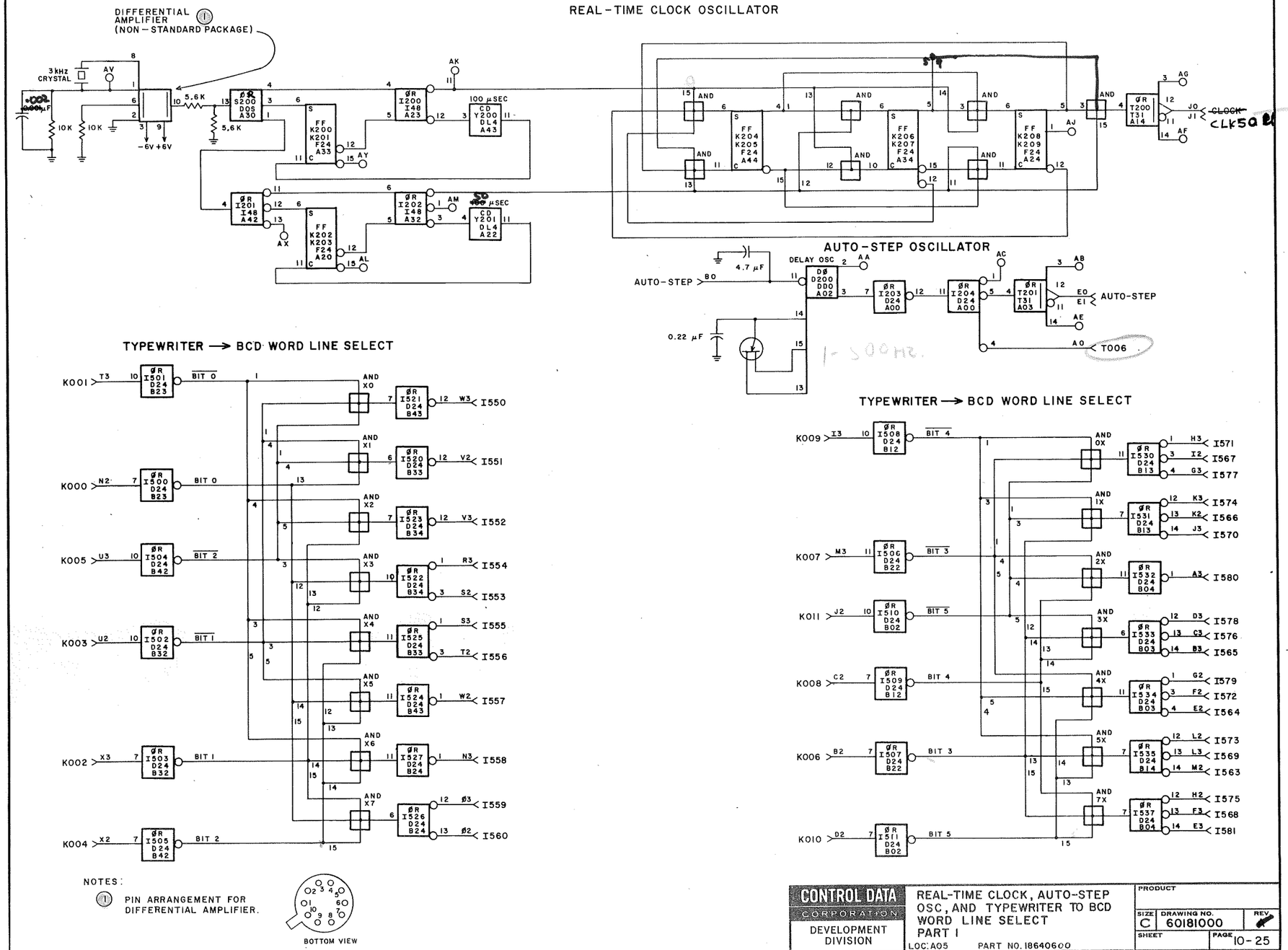
L0	A03-B3	10-33	0 REG NOT BIT 2
L1	A05-X2	10-25	0 REG NOT BIT 2
M0	A05-U3	10-25	0 REG BIT 2
M1	A07-X1	10-17	NOT DATA TO 0 REGISTER
N0	A7P1-t*		NOT BIT 1 FROM TW
N1	A03-C3	10-33	0 REG BIT 2
N2	A5J2/J3 A-7		TW 0 REG BIT 03
	A04-Q1		
	2A1A6J15/J16 A-7		
	2B1B9-R0	6-27	
N3	A5J2/J3 A-8		
	A04-Q0		
	2A1A6J15/J16 A-8		
	2B1B9-R1	6-27	
O0	A5J2/J3 A-5		TW 0 REG BIT 02 FROM BC
	A04-O2		
	2A1A6J15/J16 A-5		
	2B1B9-L0	6-27	
O1	A5J2/J3 A-6		
	A04-O3		
	2A1A6J15/J16 A-6		
	2B1B9-L1	6-27	
O2	A5J2/J3 A-5		TW 0 REG BIT 02
	A04-O0		
	2A1A6J15/J16 A-5		
	2B1B9-L0	6-27	
O3	A5J2/J3 A-6		
	A04-O1		
	2A1A6J15/J16 A-6		
	2B1B9-L1	6-27	
P0	A02-H0	10-21	CARRIAGE RETURN
P1	A02-D1	10-21	BACKSPACE
P3	A06-E1	10-31	TYPE TO BCD CODE - NOT BIT 3
Q0	A5J2/J3 A-8		
	A04-N3		
	2A1A6J15/J16 A-8		
	2B1B9-R1	6-27	
Q1	A5J2/J3 A-7		TW 0 REG BIT 03 FROM BC
	A04-N2		
	2A1A6J15/J16 A-7		
	2B1B9-R0	6-27	
Q3	A06-B1	10-31	TYPE TO BCD CODE - NOT BIT 0
R0	A03-L3	10-33	0 REG NOT BIT 3
R1	A05-B2	10-25	0 REG NOT BIT 3
R2	A5J2/J3 A-3		TW 0 REG BIT 01
	A04-I1		
	2A1A6J15/J16 A-3		
	2B1B9-G0	6-27	
R3	A5J2/J3 A-4		
	A04-I0		
	2A1A6J15/J16 A-4		
	2B1B9-G1	6-27	
S0	A03-O3	10-33	0 REG BIT 3
S1	A05-M3	10-25	0 REG BIT 3
S2	A5J2/J3 A-1		TW 0 REG BIT 00
	A04-O1		
	2A1A6J15/J16 A-1		
	2B1B9-O1	6-27	
S3	A5J2/J3 A-2		
	A04-O0		
	2A1A6J15/J16 A-2		
	2B1B9-O0	6-27	
T0	A03-J3	10-33	0 REG NOT BIT 4
T1	A05-C2	10-25	0 REG NOT BIT 4
T2	A05-D2	10-25	0 REG NOT BIT 5
T3	A06-C1	10-31	TYPE TO BCD CODE - NOT BIT 1
U0	A07-V2	10-17	NOT TYPE DUMP
U1	A7P1-w*		NOT BIT 4 FROM TW
U2	A7P1-V*		NOT BIT 5 FROM TW
U3	A03-K3	10-33	0 REG NOT BIT 5
V0	A02-B2	10-21	SPECIAL FCN
V1	A07-X0	10-17	NOT DATA TO 0 REGISTER
V2	A5J2/J3 B-1		TW 0 REG BIT 05 FROM BC
	A04-H2		
	2A1A6J15/J16 B-1		
	2B1B9-W0	6-27	
V3	A5J2/J3 B-2		
	A04-H3		
	2A1A6J15/J16 B-2		
	2B1B9-W1	6-27	
W0	A5J2/J3 A-10		
	A04-J2		
	2A1A6J15/J16 A-10		
	2B1B9-X1	6-27	
W1	A5J2/J3 A-9		TW 0 REG BIT 04 FROM BC
	A04-J3		
	2A1A6J15/J16 A-9		
	2B1B9-X0	6-27	
W3	A7P1-U		NOT BIT 3 FROM TW
X0	A03-I3	10-33	0 REG BIT 4
X1	A05-I3	10-25	0 REG BIT 4
X2	A05-J2	10-25	0 REG BIT 5
X3	A03-H3	10-33	0 REG BIT 5

* These pins on plug designated by lower case letters.



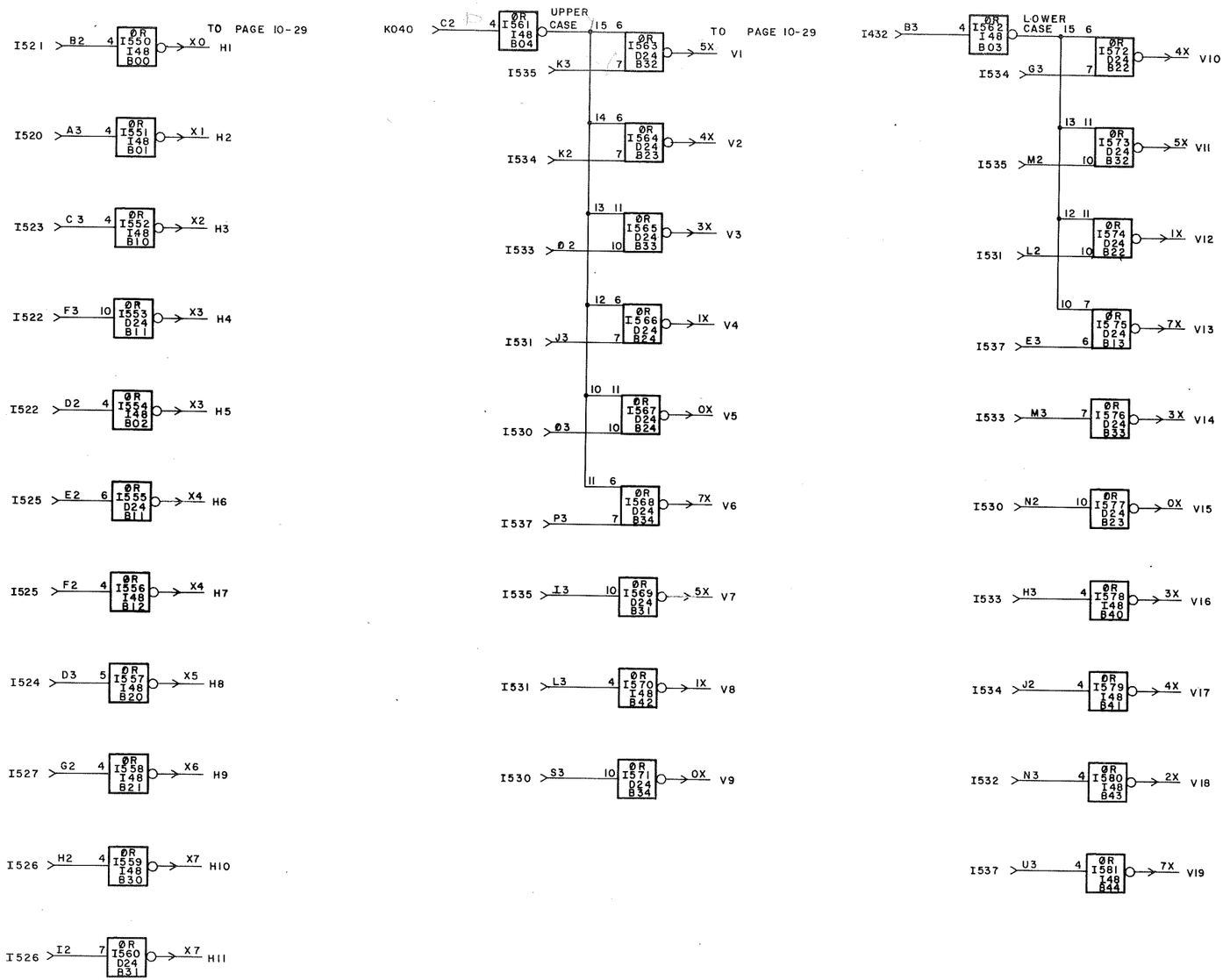
CONTROL DATA	TITLE		EQUIPMENT
DEVELOPMENT DIVISION	Ø REGISTER BITS 0 — 5 AND BCD CHAR TO STORAGE TRANSMIT ENABLE		SIZE C · DRAWING NO. 60181000 · REV. A
	LOC: A04	PART NO. 18640400	SHEET · PAGE 10-23

A0	A07-U0	10-17	AUTO-STEP
A3	A06-N3	10-27	TW TO BCD CODE SEL - NOT 2X
B0	A5J01D-06		AUTO-STEP
B2	A04-R1	10-23	O REG NOT BIT 3
B3	A06-02	10-27	TW TO BCD CODE SEL - NOT 3X
C2	A04-T1	10-23	O REG NOT BIT 4
C3	A06-M3	10-27	TW TO BCD CODE SEL - NOT 3X
D2	A04-T2	10-23	O REG NOT BIT 5
D3	A06-H3	10-27	TW TO BCD CODE SEL - NOT 3X
E0	A5J2/J3 C-5		AUTO STEP OSC TO PF
	2A1A6J15/J16 C-5		
	2B289-X3	5-75	
E1	A5J2/J3 C-6		
	2A1A6J15/J16 C-6		
	2B289-X2	5-75	
E2	A06-K2	10-27	TW TO BCD CODE SEL - NOT 4X
E3	A06-U3	10-27	TW TO BCD CODE SEL - NOT 7X
F2	A06-G3	10-27	TW TO BCD CODE SEL - NOT 4X
F3	A06-P3	10-27	TW TO BCD CODE SEL - NOT 7X
G2	A06-J2	10-27	TW TO BCD CODE SEL - NOT 4X
G3	A06-N2	10-27	TW TO BCD CODE SEL - NOT 0X
H2	A06-E3	10-27	TW TO BCD CODE SEL - NOT 7X
H3	A06-S3	10-27	TW TO BCD CODE SEL - NOT 0X
I2	A06-03	10-27	TW TO BCD CODE SEL - NOT 0X
I3	A04-X1	10-23	O REG BIT 4
J0	A5J2/J3 C-3		CLOCK PULSE-50 USEC EACH MS
	2A1A6J15/J16 C-3		
	2B188-D1	6-11	
J1	A5J2/J3 C-4		
	2A1A6J15/J16 C-4		
	2B188-D0	6-11	
J2	A04-X2	10-23	O REG BIT 5
J3	A06-L3	10-27	TW TO BCD CODE SEL - NOT 1X
K2	A06-J3	10-27	TW TO BCD CODE SEL - NOT 1X
K3	A06-L2	10-27	TW TO BCD CODE SEL - NOT 1X
L2	A06-M2	10-27	TW TO BCD CODE SEL - NOT 5X
L3	A06-I3	10-27	TW TO BCD CODE SEL - NOT 5X
M2	A06-K3	10-27	TW TO BCD CODE SEL - NOT 5X
M3	A04-S1	10-23	O REG BIT 3
N2	A04-A3	10-23	O REG NOT BIT 0
N3	A06-G2	10-27	TW TO BCD CODE SEL - NOT X6
O2	A06-I2	10-27	TW TO BCD CODE SEL - NOT X7
O3	A06-H2	10-27	TW TO BCD CODE SEL - NOT X7
R3	A06-D2	10-27	TW TO BCD CODE SEL - NOT X3
S2	A06-F3	10-27	TW TO BCD CODE SEL - NOT X3
S3	A06-E2	10-27	TW TO BCD CODE SEL - NOT X4
T2	A06-F2	10-27	TW TO BCD CODE SEL - NOT X4
T3	A04-E1	10-23	O REG BIT 0
U2	A04-J1	10-23	O REG BIT 1
U3	A04-M0	10-23	O REG BIT 2
V2	A06-A3	10-27	TW TO BCD CODE SEL - NOT X1
V3	A06-C3	10-27	TW TO BCD CODE SEL - NOT X2
W2	A06-D3	10-27	TW TO BCD CODE SEL - NOT X5
W3	A06-B2	10-27	TW TO BCD CODE SEL - NOT X0
X2	A04-L1	10-23	O REG NOT BIT 2
X3	A04-G1	10-23	O REG NOT BIT 1



CONTROL DATA CORPORATION	REAL-TIME CLOCK, AUTO-STEP OSC, AND TYPEWRITER TO BCD WORD LINE SELECT PART I	PRODUCT	
DEVELOPMENT DIVISION	LOC: A05 PART NO. 1864060O	SIZE C	DRAWING NO. 60181000 REV. P
		SHEET	PAGE 10-25

+2.2v = "1"
+0.9v = "0"



A3 A05-V2	10-25	TW TO BCD CODE SEL - NOT X1
B2 A05-W3	10-25	TW TO BCD CODE SEL - NOT X0
B3 A02-03	10-19	NOT LWR CASE STATUS
C2 A02-S2	10-19	LWR CASE STAUS
C3 A05-V3	10-25	TW TO BCD CODE SEL - NOT X2
D2 A05-R3	10-25	TW TO BCD CODE SEL - NOT X3
D3 A05-W2	10-25	TW TO BCD CODE SEL - NOT X5
E2 A05-S3	10-25	TW TO BCD CODE SEL - NOT X4
E3 A05-H2	10-25	TW TO BCD CODE SEL - NOT 7X
F2 A05-T2	10-25	TW TO BCD CODE SEL - NOT X4
F3 A05-S2	10-25	TW TO BCD CODE SEL - NOT X3
G2 A05-N3	10-25	TW TO BCD CODE SEL - NOT X6
G3 A05-F2	10-25	TW TO BCD CODE SEL - NOT 4X
H2 A05-03	10-25	TW TO BCD CODE SEL - NOT X7
H3 A05-D3	10-25	TW TO BCD CODE SEL - NOT 3X
I2 A05-02	10-25	TW TO BCD CODE SEL - NOT X7
I3 A05-L3	10-25	TW TO BCD CODE SEL - NOT 5X
J2 A05-G2	10-25	TW TO BCD CODE SEL - NOT 4X
J3 A05-K2	10-25	TW TO BCD CODE SEL - NOT 1X
K2 A05-E2	10-25	TW TO BCD CODE SEL - NOT 4X
K3 A05-M2	10-25	TW TO BCD CODE SEL - NOT 5X
L2 A05-K3	10-25	TW TO BCD CODE SEL - NOT 1X
L3 A05-J3	10-25	TW TO BCD CODE SEL - NOT 1X
M2 A05-L2	10-25	TW TO BCD CODE SEL - NOT 5X
M3 A05-C3	10-25	TW TO BCD CODE SEL - NOT 3X
N2 A05-G3	10-25	TW TO BCD CODE SEL - NOT 0X
N3 A05-A3	10-25	TW TO BCD CODE SEL - NOT 2X
O2 A05-B3	10-25	TW TO BCD CODE SEL - NOT 3X
O3 A05-12	10-25	TW TO BCD CODE SEL - NOT 0X
P3 A05-F3	10-25	TW TO BCD CODE SEL - NOT 7X
S3 A05-H3	10-25	TW TO BCD CODE SEL - NOT 0X
U3 A05-E3	10-25	TW TO BCD CODE SEL - NOT 7X

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE
TYPEWRITER TO BCD
WORD LINE SELECT
PART 2

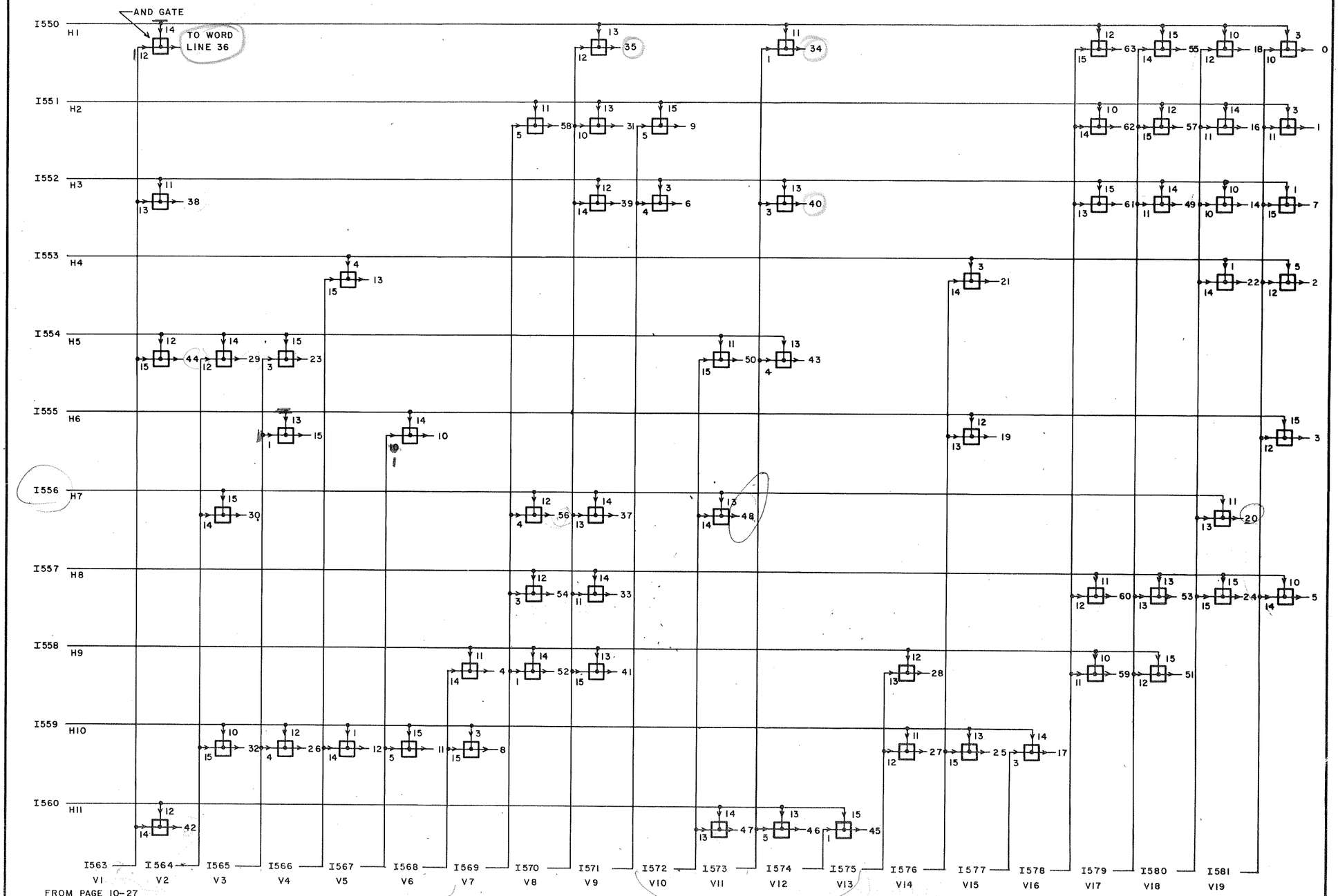
LOC: A06 PART NO. 18704900

PRODUCT

SIZE	DRAWING NO.	REV.
C	60181000	A

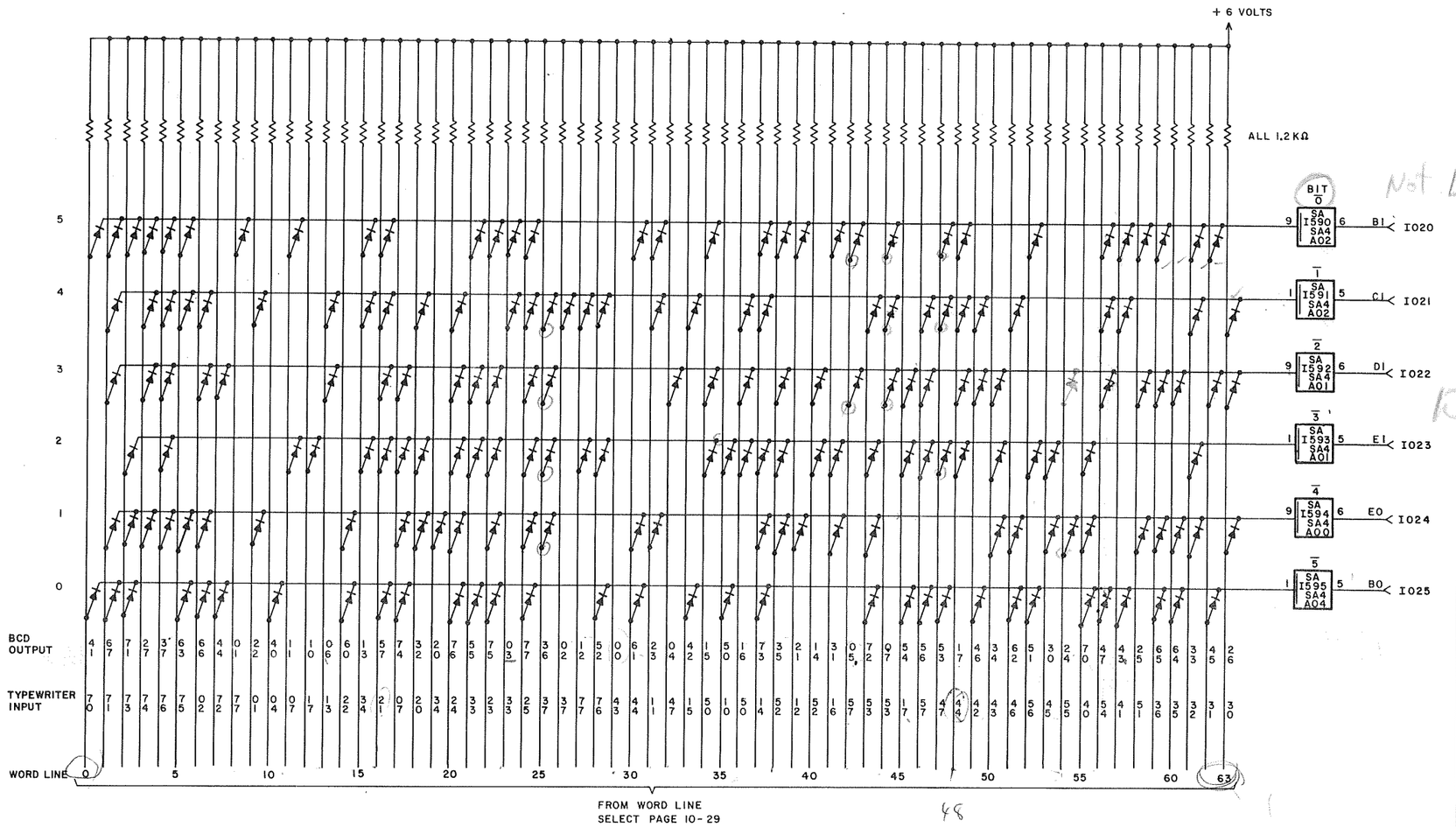
SHEET PAGE 10-27

FROM PAGE 10-27



FROM PAGE 10-27

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE TYPEWRITER TO BCD WORD LINE SELECT PART 3 LOC: A06 PART NO. 18704900	PRODUCT	
		SIZE C	DRAWING NO. 60181000
		REV. A	
		SHEET	PAGE 10-29



B0 A04-K2	10-23	TYPE TO BCD CODE = NOT BIT 5
B1 A04-Q3	10-23	TYPE TO BCD CODE = NOT BIT 0
C1 A04-T3	10-23	TYPE TO BCD CODE = NOT BIT 1
D1 A04-K3	10-23	TYPE TO BCD CODE = NOT BIT 2
E0 A04-D3	10-23	TYPE TO BCD CODE = NOT BIT 4
E1 A04-P3	10-23	TYPE TO BCD CODE = NOT BIT 3

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE
TYPEWRITER TO BCD
DIODE MATRIX MEMORY TRANSLATOR

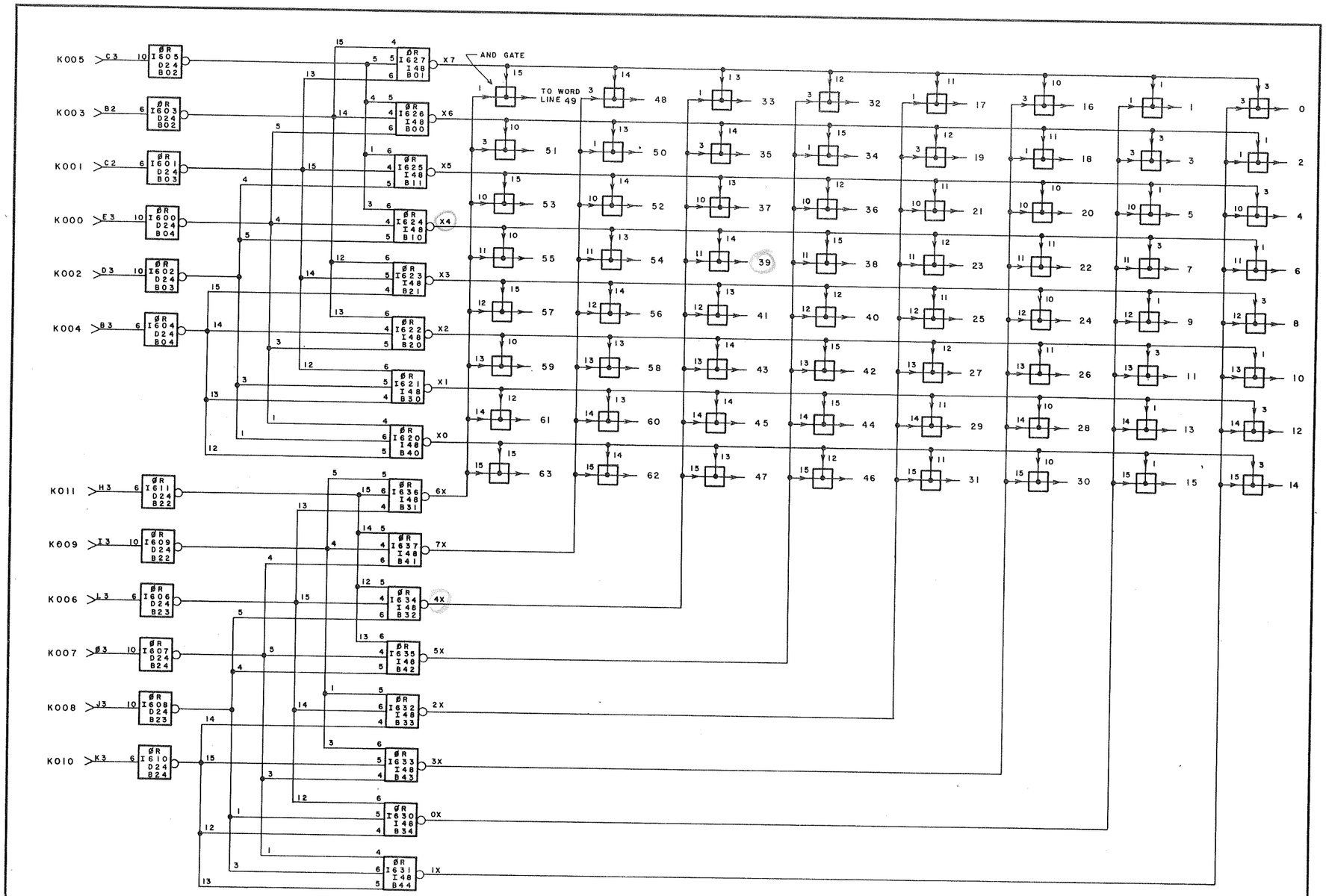
LOC: A06 PART NO. 1870490

PRODUCT

SIZE	DRAWING NO.	REV.
C	60181000	A

SHEET

PAGE 10-31



B2	A04-J0	10-23	0 REG BIT 1
B3	A04-L0	10-23	0 REG NOT BIT 2
C2	A04-E0	10-23	0 REG BIT 0
C3	A04-N1	10-23	0 REG BIT 2
D3	A04-G0	10-23	0 REG NOT BIT 1
E3	A04-B2	10-23	0 REG NOT BIT 0
H3	A04-X3	10-23	0 REG BIT 5
I3	A04-X0	10-23	0 REG BIT 4
J3	A04-T0	10-23	0 REG NOT BIT 4
K3	A04-U3	10-23	0 REG NOT BIT 5
L3	A04-R0	10-23	0 REG NOT BIT 3
03	A04-S0	10-23	0 REG BIT 3

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

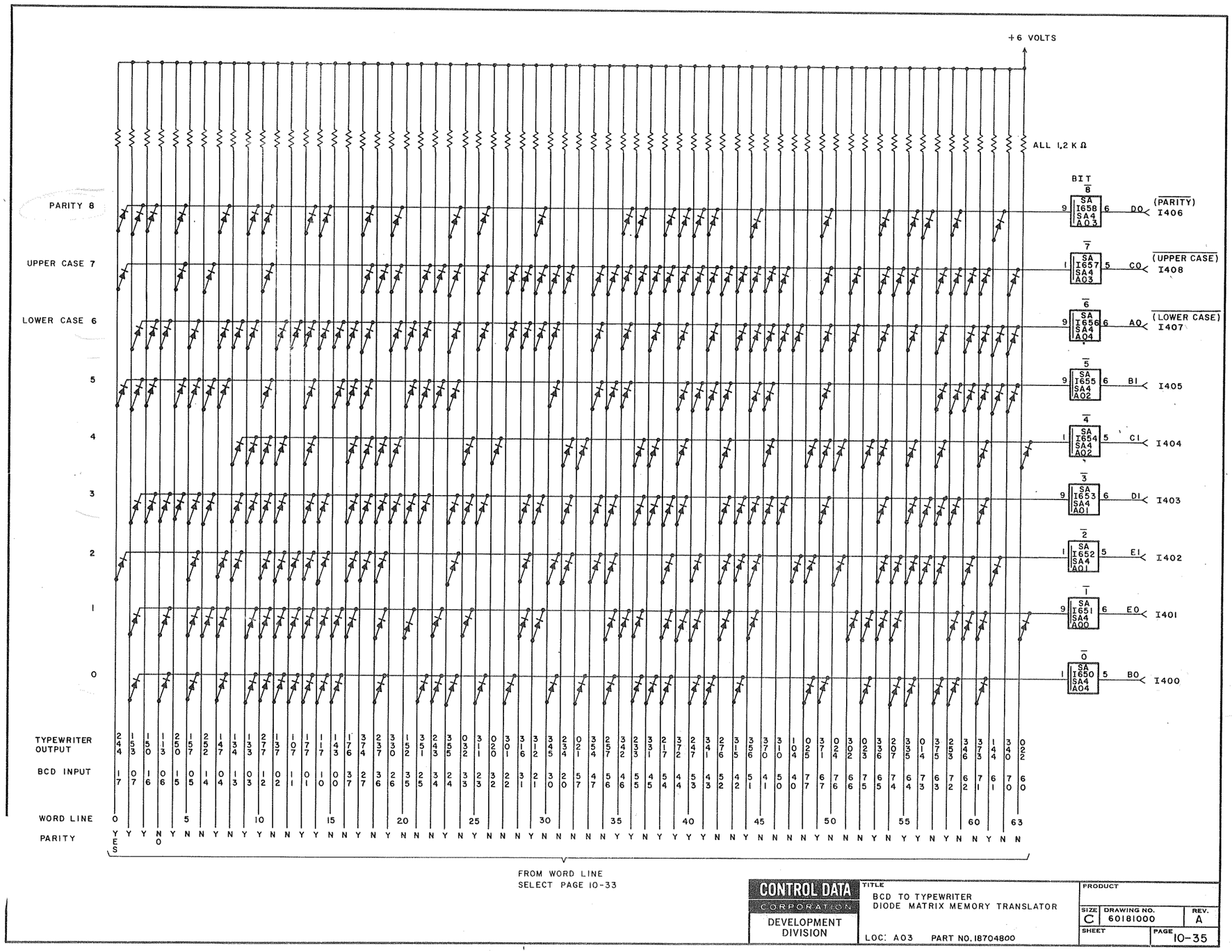
TITLE
BCD TO TYPEWRITER
WORD LINE SELECT

LOC: A03 PART NO. 18704800

PRODUCT

SIZE	DRAWING NO.	REV.
C	60181000	A

SHEET | PAGE 10-33



A0	A02-T2	10-19	BCD TO TW CODE=NOT LWR CASE
B0	A02-K0	10-19	BCD TO TYPE CODE = NOT BIT 0
B1	A02-T1	10-19	BCD TO TYPE CODE = NOT BIT 5
C0	A02-K3	10-19	BCD TO TW CODE=NOT UP. CASE
C1	A02-Q0	10-19	BCD TO TYPE CODE = NOT BIT 4
D0	A02-P0	10-19	BCD TO TW CODE=NOT PARITY
D1	A02-P1	10-19	BCD TO TYPE CODE = NOT BIT 3
E0	A02-L1	10-19	BCD TO TYPE CODE = NOT BIT 1
E1	A02 01	10-19	BCD TO TYPE CODE = NOT BIT 2

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE
BCD TO TYPEWRITER
DIODE MATRIX MEMORY TRANSLATOR

LOC: A03 PART NO. 18704800

PRODUCT

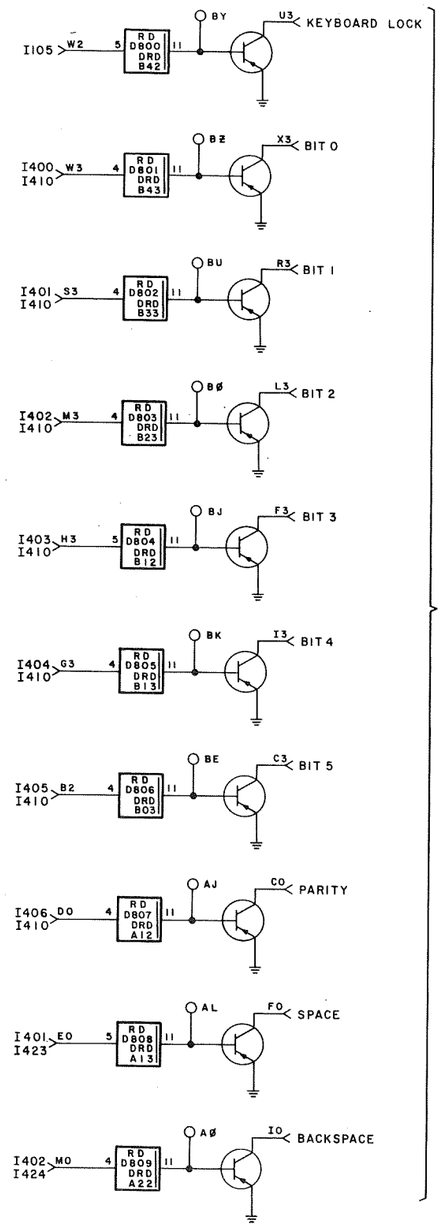
SIZE	DRAWING NO.	REV.
C	60181000	A

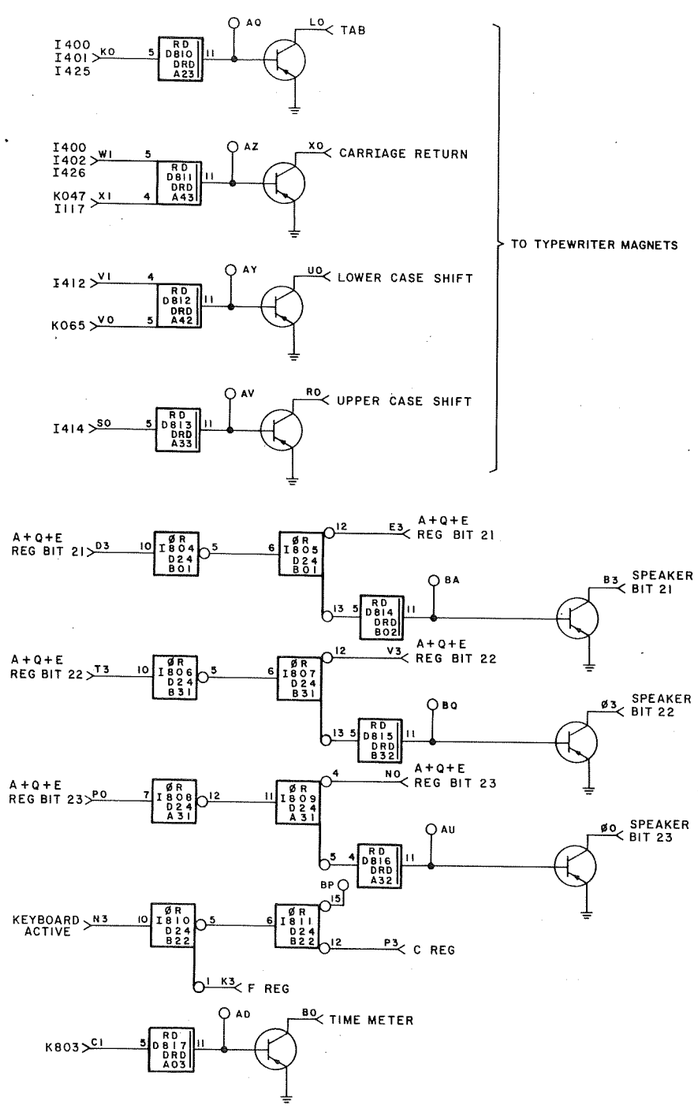
SHEET

PAGE 10-35

481

B0	A2P5TB1-8		TO TIME METER
B2	A02-Q1	10-19	(TYPE CODE NOT BIT 5)(PRINT)
B3	A2P5TB1-3		SPEAKER BIT 21
C0	A7P1-H		TO PARITY MAGNET
C1	A07-B3	10-17	STOR ACTIVE
C3	A7P1-E		TO TW PRINT SEL MAGNET BIT 5
D0	A02-T0	10-19	PARITY
D3	A2P5-B		A + Q + E REG BIT 21
E0	A02-J0	10-19	(TYPE CODE NOT BIT 1)(SPACE)
F3	A7P1-F		TO TW PRINT SEL MAGNET BIT 3
E3	A2P5-F		A + Q + E REG BIT 21
F0	A7P1-M		TO SPACE MAGNET
G3	A02_S1	10-19	(TYPE CODE NOT BIT 4)(PRINT)
H3	A02-R0	10-19	(TYPE CODE NOT BIT 3)(PRINT)
I0	A7P1-N		TO BACKSPACE MAGNET
I3	A7P1-D		TO TW PRINT SEL MAGNET BIT 4
K0	A02_K1	10-19	(TYPE CODE NOT BIT 0)(TYPE CODE NOT BIT 1)(TAB)
K3	A2P5-K		F REGISTER
L0	A7P1-L		TO TAB MAGNET
L3	A7P1-B		TO TW PRINT SEL MAGNET BIT 2
M0	A02-M1	10-19	(TYPE CODE NOT BIT 2)(BKSP)
M3	A02-R1	10-19	(TYPE CODE NOT BIT 2)(PRINT)
N0	A2P5-J		A + Q + E REG BIT 23
N3	A2P5-A		KEYBOARD ACTIVE
O0	A2P5TB1-1		SPEAKER BIT 23
O3	A2P5TB1-2		SPEAKER BIT 22
P0	A2P5-D		A + Q + E REG BIT 23
P3	A2P5-L		C REGISTER
R0	A7P1-S		TO UPR CASE SHIFT MAGNET
R3	A7P1-C		TO TW PRINT SEL MAGNET BIT 1
S0	A02-D3	10-19	UPPER CASE SHIFT
S3	A02-S0	10-19	(TYPE CODE NOT BIT 1)(PRINT)
T3	A2P5-C		A + Q + E REG BIT 22
U0	A7P1-T		TO LWR CASE SHIFT MAGNET
U3	A7P1-K		TO KEYBOARD LOCK MAGNET
V0	A07-D2	10-17	LOWER CASE FCN LOCKOUT
V1	A02-C3	10-19	LOWER CASE SHIFT
V3	A2P5-H		A + Q + E REG BIT 22
W1	A02-M0	10-19	(TYPE CODE NOT BIT 0)(TYPE CODE NOT BIT 2)(CRG RET)
W2	A07_R1	10-17	TW CONT BUSY + TYPE DUMP
W3	A02-N0	10-19	(TYPE CODE NOT BIT 0)(PRINT)
X0	A7P1-P		TO CARRIAGE RETURN MAGNET
X1	A07_A0	10-17	(CRG RET)(TYPE NOT BUSY)
X3	A7P1-A		TO TW PRINT SEL MAGNET BIT 0





CONTROL DATA CORPORATION	TITLE: RELAY DRIVERS	PRODUCT	
DEVELOPMENT DIVISION	LOC: A00 PART NO. 186405 00	SIZE C / DRAWING NO. 60181000 / REV. A	
		SHEET	PAGE 10-37

INTRODUCTION

This part contains maintenance information on the AC104 Central Processor, DC111 Communications Channel, and CR105 Console. For maintenance information on the storage modules and peripheral devices, refer to Literature Distribution Center Catalog.

INSTRUMENTS, TOOLS, AND MATERIALS

Item	Quantity	Part Number
Oscilloscope, Tektronix Model 547	1	
Oscilloscope Preamp, Tektronix Model 1A1	1	
Oscilloscope Cart, Tektronix Model 202-1	1	
Voltohmmeter, Triplett Model 630	1	
Oscilloscope Probe (1:1 Attenuation Ratio)	2	12208508

3500-T CEM TOOL KIT

Item	Quantity	Part Number
Tip, Nylon Module Shock Test		12209308
Cutter, Copper Tubing, 0.25-1.375	1	12209850
Tool, Copper Tubing Flaring	1	12209851
Reamer, Inner and Outer Copper Tube	1	12209852
Leak Detector, Freon	1	12209853
Wrench, Flare Nut, .875 x 1.1251	1	12209854
Wrench, Flare Nut, .750 x .8751	1	12209855
Socket, .312, 4 Point, .25 Drive	1	12209968
Refrigerant, 12 lb, CC12F2	1	12210065
Tweezer, Fine Point, 4.75 inch	1	12210275
Iron, Soldering, 15W Miniature	1	12210314
Tip, Soldering Iron, .046-inch Spade	12	12210315
Stripper, Wire, 20-20 gauge	1	12210433
Knife, X-Acto, 5 inch w/Blade	1	12210434
Desoldering Tool		12210436
Solder, 60/40, 24 gauge (.022 inch)	1	12210437
Pyrometer	1	12210570
Insertion Tool (Taper Pin)		12210773
Tool, Crimping Buchanan		12210781
Tool, Crimping (Pin Socket)	1	12210813
Insert, Positioner (Buchanan)		12210897

Item	Quantity	Part Number
Filter, Fluid Aerosol	2	12210958
Tool, Pin Removal (61 Pin)		12210988
Psychrometer, Sling Taylor 1328	1	12210991
Magnifier, 12 Power	1	12210995
Element Soldering	1	12212786
Tool, Insertion Ground Pin	1	12213235
Tool, Punch Ground Pin	1	12213236
Tool, Insertion Wire Side/Plate	1	12213237
Tool, Insertion Pin Side/Plate	1	12213238
Wire, 30G Sol Blk	1	16963400
Extender, 50 PAK Integrated Circuit	2	18662200
Adapter, Scope Probe DTL 50 PAK	2	18672000
Cable, Test Point	2	18697522
Adapter Probe and Term		18697527
Adapter Scope Probe TCS 50 PAK	2	18762700
Tool, Extraction Receptacle	1	18934700
Tip, Desoldering (50 PAK Chips)	1	20258200
Pin, Receptor for 61 Pin Connector	25	30000902
Tubing, Head Shrink, .7501D		93154136
50 PAK Shock Testing Head	1	
6000-Type Shock Testing Head	1	12209308

PUBLICATIONS

The following publications, in addition to this manual, should be available to personnel maintaining the AC104 Central Processor, DC111 Communications Channel, and CR105 Console.

	Title	Publication Number
1.	3500 Computer System Reference Manual	60200300
2.	3300/3500 Computer Systems Instruction Codes	60189600
3.	3L00 System Maintenance Monitor Reference Manual	60118600
4.	Parts Data for AC104-A, DC111-A, and CR105-A	60233100
5.	3500 Computer System Site Preparation Manual	60212700
6.	Maintenance Aids for AC104-A (Command Timing Charts)	60234100
7.	IBM Selectric Series 73 Reference Manual (Contains maintenance information and parts catalog for IBM Selectric Typewriter used in console)	60095900

	Title	Publication Number
8.	Preventive Maintenance Index (PMI) and Preventive Maintenance Procedures (PMP) for IBM Selectric Typewriter. Available from Customer Engineering.	None
9.	3000 Series Computer Systems Input/Output Specification	60048800
10.	INTEBRID Circuits Manual	60201000
11.	Refrigeration Units for Cordwood Modules (Parts List)	60227400

Manuals for the storage modules and peripheral devices are listed in the Literature Distribution Center Catalog.

MAINTENANCE PANEL

The maintenance panel (Figure 11-1) is located in Unit 2 of the Central Processor; it is designated assembly 2A2A4. The panel has switches for selecting maintenance operations and conditions, and display lamps for monitoring maintenance registers and page file operations. The storage protection switches used during normal program operations are also located on this panel.

The panel assembly contains its own power supply which provides the display lamps with +100 vdc power from a 120 vac/400 Hz input.

MAINTENANCE DISPLAYS

Page File Input/Output Display

The Page File Input display is driven by the upper 9 bits of the original unrelocated storage address received from Main Control or Block Control. The upper 7 bits (Page File Address) select the 12-bit Page Index that is referenced during relocation.

Bits 9 and 10 are partial page modifiers which, when added to bits 0 and 1 of the Page File output, form a partial sum that designates the quarter-page (0-3) where storage addressing begins. This partial sum becomes bits 9 and 10 of the storage address. The display lamps for these bits are aligned on the panel to allow convenient monitoring of the Partial Page Adder operation.

The Page File Output display monitors the contents of the Page Index that is referenced. The PA (Page Address) portion of the index becomes bits 11-17 of the storage address and designates the page referenced in storage. A fully expanded storage system has 128 (000-177_8 addresses) pages, each page consisting of 2048 absolute locations. The Pl (Page Length) and E (Exclusion Bit) portions of the Page Index are not used directly in the address, but are flags sensed internally to establish boundary conditions and storage protection.

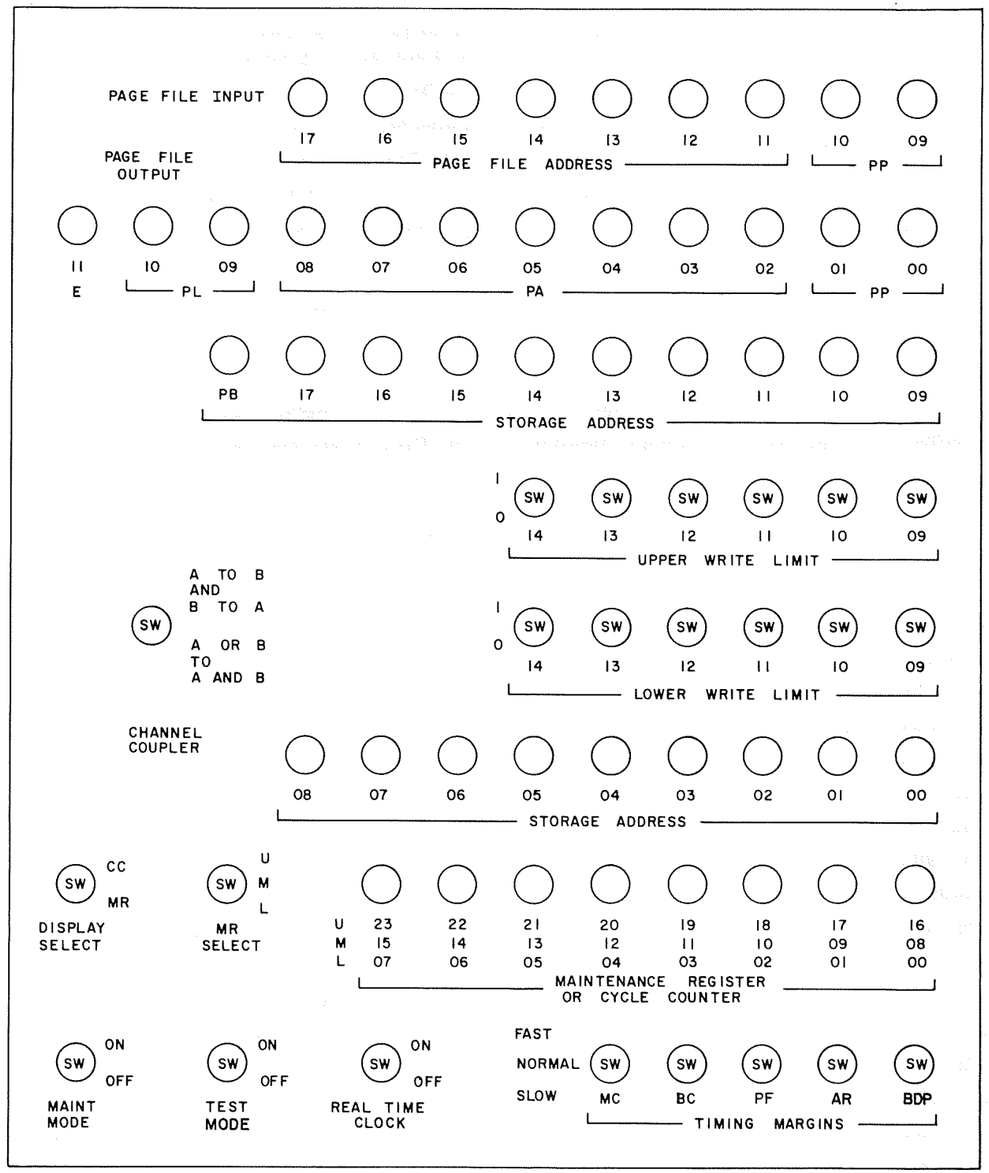


Figure 11-1. Computer Maintenance Panel

Storage Address Display

The Storage Address display is driven by a fan-out from the address parity generator in the Relocation section. The parity bit is displayed as the uppermost bit.

The lower 9 bits of the Storage Address display indicate the portion of the original storage address sent to the Relocation section but are unchanged by the relocation process. Bits 9 and 10 reflect the output of the Partial Page Adder. Bits 11-17 are identical to the Page Address portion of the Page File Output.

Storage Protect Switches

The Storage Protect switches allow two separate areas within a designated 32K of storage to be protected. The binary switches labeled UPPER WRITE LIMIT and LOWER WRITE LIMIT are set to select the range of addresses protected within each area. Each binary setting of the switches represents one multiple of 512 locations, with 64 (77_8) different settings possible. See Table 11-1. The switches do not provide single-address protection, and during Executive Mode operations, apply only to areas referenced through the lower 16 indexes (State 0) of the Page Index File. All storage protect switches are disabled by pressing the DISABLE STO PROTECT switch on the console.

With the UPPER WRITE LIMIT switches, blocks of addresses decreasing from address 77777 are protected. The switch settings are compared for equality with bits 9-14 of the storage address. The lower 9 bits of the Upper Write Limit are always "1's".

The LOWER WRITE LIMIT switches protect blocks of addresses increasing from address 00000. The switch settings are compared for equality with bits 9-14 of the storage address, etc. The lower 9 bits of the Lower Write Limit are always "0's".

TABLE 11-1. SAMPLE STORAGE PROTECT SETTINGS

Upper Write Limit Setting	Address Range Protected	Lower Write Limit Setting	Address Range Protected	No. of Locations Protected
76	76777-77777	01	00000-01000	512
75	75777-77777	02	00000-02000	1024
67	67777-77777	10	00000-10000	4096
57	67777-77777	20	00000-20000	8192
37	37777-77777	40	00000-40000	16384
20 20	20777-77777	57	00000-57000	24064
00	00000-77777	77	00000-77777	32768

MAINTENANCE SWITCHES

CHANNEL COUPLER Switch

With the CHANNEL COUPLER switch in the A TO B AND B TO A (up) position, the Channel Coupler logic interfaces with two I/O channels cabled to the coupler connectors. Any two channels can be connected to the channel coupler. Control signals can be timed and data transfers performed between any two channels. In the A OR B TO A AND B (down) position, the CHANNEL COUPLER switch exchanges control signals with any single channel cabled to the coupler.

A complete description of the Channel Coupler feature is included later in this part.

DISPLAY SELECT and MR SELECT Switches

DISPLAY SELECT is a two-position switch which selects the Arithmetic Cycle Counter (CC) or the Maintenance register (MR) for display.

The switch is spring-loaded in the CC position. The upper (U), middle (M), or lower (L) portion of the Maintenance register is selected by the MR SELECT switch. The Maintenance register should not be displayed when the computer is running. The display may interfere with the proper execution of a BDP section diagnostic program.

MAINT MODE, TEST MODE, REAL-TIME CLOCK, and TIMING MARGINS Switches

These switches are active only when the key-operated switch on the back control panel of the console is turned ON. With the console switch OFF, Maintenance mode and Test mode are disabled, the Real-Time Clock is running, and all timing margins are normal.

In Maint Mode the cycling of arithmetic instructions can be controlled and the contents of registers and networks that normally are invisible to the program can be stored. The Maintenance mode feature is described later in this part.

A Test mode operation forces the computer to repeat the following sequences at Auto Step rate: GO, STOP, 25 μsec, MASTER CLEAR.

The TIMING MARGINS switches change the internal timing of the central processor by enabling different outputs from the tapped delay line circuits (TTDL) used in timing chains. Each switch on the panel corresponds to a section of the machine having its own timing chain. In the FAST position, a timing chain runs faster and the pulses are narrower. In the SLOW position, the timing chain runs slower and the pulses are wider.

CHANNEL COUPLER

The Channel Coupler permits the testing of I/O channels independent of any peripheral equipment. This testing may include the running of diagnostics and observing timing signals with a scope. The coupler consists of a control logic module and four 61-pin cable jacks (assembly 2A4A13) located in the I/O connector panel assembly (Figure 11-2).

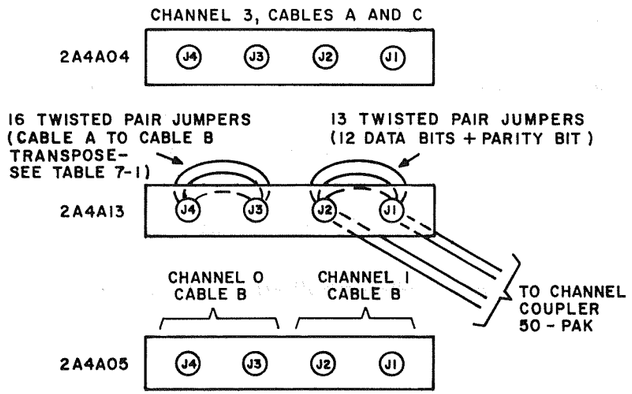


Figure 11-2. I/O Connector Panel

The actual cabling used between the channels tested and the coupler connector depends on the type of test performed. A two-position switch on the Computer Maintenance Panel selects the mode of operation.

SINGLE CHANNEL MODE

With the CHANNEL COUPLER switch in the A OR B TO A AND B (down) position, tests are performed on a single channel. One "A" cable* from the channel tested is connected to coupler connector J1 or J2. A cable terminator assembly must be installed on the other connector. The Channel Coupler returns a Reply signal to the channel for each Connect, Function, or Data Signal transmitted to the coupler. This test is primarily intended to facilitate adjustment of delay circuits in the channel to meet I/O specifications. Parity errors occur during Read operations since data is not provided by the coupler. This doesn't affect the operation, however. If two channels are cabled to the coupler, both receive Reply signals.

DUAL CHANNEL MODE

With the CHANNEL COUPLER switch in the A TO B AND B TO A (up) position, the coupler interfaces with two I/O channels cabled to the coupler connectors and permits testing during actual data transfer between the channels. One "A" cable from each of the two channels is connected to coupler connectors J1 and J2. Connectors J3 and J4 are not used.

The coupler responds to operations on both channels as indicated below. For explanatory purposes, one channel is called Channel A, the other Channel B.

1. If Channel A performs a Connect or Function operation while Channel B is neither reading nor writing, the coupler does not provide a response. The No-Response condition causes the Connect or Function reject instruction to be read from P + 1 after 100 μsec.
2. If a Write operation is initiated on Channel B, with Channel A inactive, no reply is received and Channel B remains busy. If a Connect or Function is then performed on Channel A, both channels receive a Reject from the coupler and although the data is placed on the lines, no data transfer occurs. To avoid having more than one transmitter ON per twisted pair, "1" bits should not be set in the same bit position of the code and the data, including the parity bit.
3. If a Read operation is initiated on Channel B, with Channel A inactive, no Reply is received and Channel B remains busy. If a Connect or Function is then performed on Channel A, both channels receive a Reply from the coupler. The reading channel (Channel B) transfers the Connect or Function code to storage.
4. If Channel A performs a Read and Channel B performs a Write, each channel acts like a peripheral equipment to the other. Core to core transfers occur as programmed. If Channel A requests a larger input block than the output block for Channel B, the coupler provides an End of Record signal to terminate the READ operation. If the Read on Channel A terminates before the Write on Channel B, Channel B hangs-up and remains busy.

The reading channel (Channel A), in conjunction with Block Control, checks parity on the data received and places a "1" on Internal Status Line 0, if a parity error exists. Parity Error indications are not sent to the writing channel.

---

* The "A" cable carries the I/O control signals (Reply, Reject) and 12 data bits.

INTERRUPT AND STATUS TESTING

Coupler connectors J3 and J4 are used to test the interrupt priority checking system. Jumpers between connectors J3 and J4 enable transposition of the data from the "A" cable of any I/O channel to the interrupt bit positions of the "B" cables for one to eight channels, depending on the cabling used. The signal transposition wired into the coupler connector assembly is listed in Table 11-2. The cabling scheme used between the channels tested is shown in Figure 11-3.

Channel A can transmit simulated Interrupt and Status signals to the other channels by executing Connect, Function, Input, and Output instructions.

TABLE 11-2. TRANSPOSITION SCHEME

Connector J3		Connector J4	
Pin	Signal	Pin	Signal
A1-2	Data Bit 00	D1-2	Interrupt Line 0
A3-4	01	D3-4	1
A5-6	02	D5-6	2
A7-8	03	D7-8	3
A9-10	04	D9-10	4
B1-2	05	E1-2	5
B3-4	06	E3-4	6
B5-6	07	E5-6	7
D1-2	Read	A1-2	Status Bit 00
D3-4	Write	A3-4	01
D5-6	Connect	A5-6	02
D7-8	Function	A7-8	03
D9-10	Data Signal	A9-10	04
E1-2	Reply	B1-2	05
E3-4	Reject	B3-4	06
E5-6	End of Record	B5-6	07

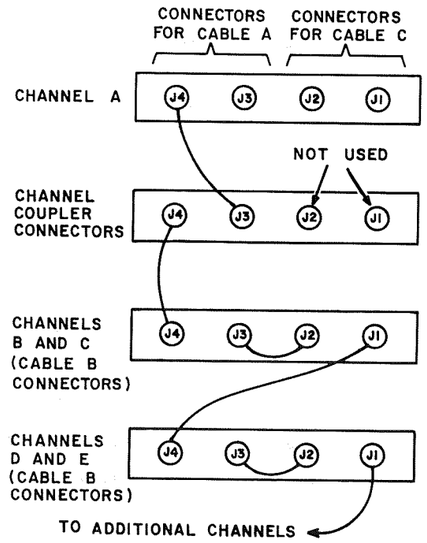


Figure 11-3. Channel Test Cabling

CHANNEL COUPLER LIMITATIONS

The Channel Coupler cannot be used to check the ability of the Communications Channels to transmit the following signals:

Cable A

- Channel Busy
- Reverse Assembly
- Word Mark
- Master Clear

Cable B

- Computer Running
- Negate BCD Conversion
- Suppress Assembly-Disassembly
- Clear External Interrupt

491

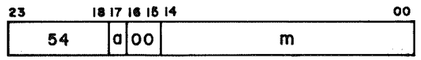
MAINTENANCE MODE

When Maintenance Mode is in effect, the operation of several instructions can be modified to provide functions useful for diagnostic programs. The main features are:

1. Iterative arithmetic and BDP instructions can be terminated at the end of any cycle and later restarted.
2. The contents of several "hidden" arithmetic registers can be transferred to storage.
3. Address incrementing can be inhibited for Block Control instructions (such as Search and Move) which process a block of sequential addresses.

The MAINT MODE switch on the maintenance panel activates Maintenance mode; the key-operated switch on the console must also be ON.

A 24-bit Maintenance register controls the modification of instructions. Each bit in this register has a specific purpose (see Table 11-3). The 54.0 instruction loads the Maintenance register from storage. The contents of the Maintenance register cannot be changed in any other way.



a = 1 FOR INDIRECT ADDRESSING
m = STORAGE ADDRESS

Instruction Description: Load the 24-bit Maintenance register with the contents of storage address 'm'. Indirect addressing, but no indexing, is possible. This instruction is a No-Op when the MAINT MODE switch on the console is OFF.

The contents of the Maintenance register can be displayed on the maintenance panel. Refer to the maintenance panel description.

TABLE 11-3. MAINTENANCE REGISTER

Bit	Function
00-05*	CYCLE COUNT. ~~Function depends on bit 13 of Maintenance register.~~ ~~a. If bit 13 = "0", bits 0-5 are terminating cycle count for arithmetic instructions.~~ ~~b. If bit 13 = "1", bits 0-5 are terminating character count for BDP instructions.~~
06*	USED ~~Function depends on bit 13 of Maintenance register.~~ ~~a. If bit 13 = "0", bit 6 causes force-terminated arithmetic instruction to restart when the instruction is executed again.~~ ~~b. If bit 13 = "1", bit 6 specifies whether the A or C field count will be used to terminate BDP instructions: Bit 6 = "0"; select A-field Bit 6 = "1"; select C-field~~
07	Block carry throughout arithmetic adder.
08	Force carry throughout arithmetic adder.
09	Inhibit address increment in Block Control.
10	Not used - must always be set to "0". {Set illegal work status to RF. does not equal output on IRT into the Reg File.
11	Block ~~Inhibit~~ setting of A^2 and Q^2 registers.
12	~~Terminate iterative arithmetic instructions after each cycle.~~
13*	a. ~~a. If "0", iterative arithmetic instructions terminate when cycle count = bits 0-5 of Maintenance register.~~ ** ~~b. If "1", BDP instructions terminate when A- or C-field character count = bits 0-5 of Maintenance register.~~
14	Enable force store of E1.
15	Enable force store of E2.
16	Enable force store of X1.
17	Enable force store of X2.
18	Enable force store of shift network, bits 24-47. [E3]
19	Enable force store of shift network, bits 00-23. [E4]
20	Enable force store of A adder (A is destroyed).
21	Enable force store of Q adder (Q is destroyed).
22	Not used - must always be set to "0".
23	Enable force store of shift count and exponent.

* ~~When Maintenance mode is used for BDP testing, all bits except bits 00-06 and 13 must be "0".~~

** Bit 12 must also be "0".

MAINTENANCE MODE IN THE ARITHMETIC SECTION

When bit 13 in the Maintenance register is "0" the following iterative arithmetic instructions can be terminated at the end of any cycle:

34 Replace Add	53 (5-7)4 (B^b) + (A) B^b
35 Selectively Set A	56 Multiply AQ
50 Multiply A	57 Divide AQ
51 Divide A	60-63 floating point instructions

The instructions are terminated as follows:

1. The instruction terminates when the arithmetic timing chain cycle count equals the count in bits 0-5 of the Maintenance register, or
2. The instruction terminates after each iteration if bit 12 of the Maintenance register is set. In this case, the count in bits 0-5 of the Maintenance register is not significant.

When the instruction terminates, a new instruction is read from P+1; however, the controls for the terminated instruction are not cleared. Thus, the terminated instruction can later be restarted if no instructions have been executed which clear the arithmetic controls.

After an instruction is forced to terminate and new instructions are read up, one of the following will occur:

1. If the new instruction is either a store (4X) or 54.0 instruction, that instruction will be executed without changing anything in the arithmetic section.
2. If the new instruction is neither a 4X nor a 54.0 instruction, and bit 06 of Maintenance register is cleared, all controls for the terminated instruction will be cleared and the new instruction executed.
3. If the new instruction is identical to the terminated instruction and bit 6* of the Maintenance register is set, the instruction restarts from the point where it was stopped. However, if the controls for the terminated instruction have been cleared, the instruction starts from the beginning.
4. If the new instruction is not identical to the terminated instruction (except 4X or 54.0) and bit 6 of the Maintenance register is set, the results will be unpredictable. The controls for the terminated instruction will probably be cleared.

---

* Bit 13 of the Maintenance register must be "0" in this case. Bit 6 has a totally different meaning when bit 13 is "1"; see Table 11-3.

When Maintenance Mode is active, the Store A (40) instruction is modified by bits 14-23 of the Maintenance register. Each of these bits specifies a register or network to be stored (see Table 11-3). If none of these bits are set, the 40 instruction executes normally (A is stored). If one bit is set, the associated register or network is stored. If two or more bits are set, all zeros will probably be stored.

If bit 7 in the Maintenance register is set, carrys are blocked throughout the adder.

If bit 8 in the Maintenance register is set, carrys are forced throughout the adder.

If bit 11 of the Maintenance register is set, arithmetic registers A^2 and Q^2, which feed the A and Q adders, will be held clear.

Arithmetic Maintenance Mode Examples

Example Number 1

Store the results of $A^1Q^1X^1X^2$ after the sixth cycle of divide A (51 instruction). Then continue the instruction to completion.

1.	Execute 54.0 instruction	(Load Maintenance register = 0000 0006)
2.	Execute 51. instruction	(Terminates on sixth cycle)
3.	Execute 54.0 instruction	(Load Maintenance register = 0040 0000)
4.	Execute 40. instruction	(Force store X^2)
5.	Execute 54.0 instruction	(Load Maintenance register = 0020 0000)
6.	Execute 40. instruction	(Force store X^1).
7.	Execute 54.0 instruction	(Load Maintenance register = 0000 0000)
8.	Execute 45. instruction	(Store A^1Q^1)
9.	Execute 54.0 instruction	(Set Maintenance register = 0000 0100)
10.	Execute 51 instruction	(Instruction proceeds from sixth iteration to completion)
11.	Execute 54.0 instruction	(Load Maintenance register = 0000 0000)
12.	Continue with program	

Example Number 2

Exit after each iteration of multiply AQ (56) instruction and store the partial results of the shift network.

1.	Execute 54.0 instruction	(Load Maintenance register = 0001 0000)
2.	Execute 56. instruction	(Exits after each iteration)
3.	Execute 54.0 instruction	(Load Maintenance register = 0200 0000)
4.	Execute 40. instruction	(Store shift network 00-23)
5.	Execute 54.0 instruction	(Load Maintenance register = 0100 0000)
6.	Execute 40. instruction	(Store shift network 24-47)
7.	Execute 54.0 instruction	(Load Maintenance register = 0001 0100) and repeat steps 2-7

Note: In this example a loop cannot be used to repeat steps 1 through 7 because a jump instruction clears the controls for the terminated instruction. A separate sequence of instructions for steps 1 through 7 is required for each iteration of the 56 instruction.

MAINTENANCE MODE IN BLOCK CONTROL

If bit 9 in the Maintenance register is 1, address incrementing is inhibited for the following Block Control instructions:

71	Search
72	Move
73.0-3	Character-Addressed Input to Storage
74.0-3	Word-Addressed Input to Storage
75.0-3	Character-Addressed Output from Storage
76.0-3	Word-Addressed Output from Storage
77.75	Set Console Typewriter Input
77.76	Set Console Typewriter Output

When these instructions are executed with bit 9 in the Maintenance register set, the specified operation repeats indefinitely using the initial operand address. The operation can be terminated by a Master Clear or 77.51 (Clear I/O, Typewriter, or Search/Move) instruction.

MAINTENANCE MODE IN THE BDP

If bit 13 of the Maintenance register is set, a character count, placed in bits 0-5 of the Maintenance register, is used to terminate BDP instructions. The instructions terminate when the A- or C-field character count equals the count in the Maintenance register plus one. Bit 6 in the Maintenance register selects the A- or C-field count as follows:

Bit 6 = 1	Select C-field for termination.
Bit 6 = 0	Select A-field for termination.

When termination occurs, a BDP Complete signal is sent to Main Control and the Interrupt flag* is set in the BDP. The BDP completes the current character operation and stores the data in memory. Normally the next instruction will be read from P + 3. However, if a Scan or Compare instruction is satisfied on the same character that causes forced termination, the exit will be to P + 4.

The diagnostic program can store the BDP operating conditions and check the data and flags against simulated results. The instruction can be restarted from the point of force-termination using normal Interrupt recovery techniques.

When Maintenance mode is used for BDP testing, all bits in the Maintenance register other than bits 0-6 and bit 13 must be cleared.

Limitations

Cycle counter will not stop at a count of 1 or 2. Therefore, the lowest exit cycle should be cycle 3. If a count of 1 or 2 is specified, the instruction goes to completion.

---

* The Interrupt Flag is bit 11 of the BDP operating conditions (see LBR instruction).

MARGIN TESTING

Margin testing is the process of running diagnostic programs while the power supply voltages and timing chain speeds are varied within specified limits (or margins). It is one of the most useful preventive maintenance techniques because it allows maintenance personnel to find areas of potential failure before actual failure occurs.

The computer system will run reliably over a relatively wide margin range: ±7-1/2 percent voltage variations and ±8 percent timing variations. However, over a period of time, the operation of a few circuits slowly decays. Often these circuits perform satisfactorily under normal operating conditions but fail if the voltage or timing is varied. Thus, margin testing can be used to find borderline circuits. If the degraded circuits are not found, they eventually will decay to the point where the machine will fail under normal operating conditions.

Since some circuit degradation is inevitable, maintenance personnel must conscientiously follow the margin testing procedure outlined in this manual for the central processor and console. Though it is sometimes possible to maintain satisfactory system operation for a long period without doing any margin testing, the result will be a build-up of marginal conditions in the machine and finally, failure during normal operation. Once a number of marginal conditions has accumulated, failures will occur frequently and it is difficult and time-consuming to troubleshoot the failures.

The margins specified in this manual are fully within safe operating limits and do not contribute to circuit degradation or early failure. The system can be operated for extended periods at maximum margins without adverse effects.

VOLTAGE MARGIN CONTROLS

A power control panel in each of the six CPU columns permits adjustment of +6V*, -6V, and -2V dc power supplies within the column. Each voltage can be separately adjusted upward or downward. A meter on each panel, calibrated in percentage, indicates the deviation from the normal settings. Similar power controls in the console allow adjustment of the +6V and -6V typewriter logic power supplies. The +7V display light power supply and the -45V typewriter magnet power supply in the console cannot be adjusted.

The range of adjustment is -100 percent and +20 percent; however, adjustments greater than ±10% are not safe and may cause circuit damage. Any combination of adjustments in the six columns within the ±10 percent range is safe.

* Columns 1 and 2 in Unit 1 do not contain +6V supplies; however, +6V margins in column 2 can be adjusted from column 0.

TIMING MARGIN CONTROLS

Five TIMING MARGINS Switches, located on the maintenance panel, increase or decrease the speed of the timing chains in the Central Processor. There is a separate switch for each of the main sections in the Central Processor:

Main Control	MC
Relocation	PF
Arithmetic	AR
Block Control	BC
BDP	BDP

In the FAST position, timing chain speed is increased by 8 percent and pulse length is reduced by about 8 percent. In the SLOW position, timing chain speed is decreased by 8 percent and pulse length is increased by about 8 percent.

PERFORMANCE AT MARGINS

The Central Processor and console should run all operational software and diagnostic programs satisfactorily with any combination of fast and slow timing margins and ±7-1/2 percent voltage margins. Any errors that occur within these limits indicate a marginal condition in the machine.

PERIODIC MARGIN TESTING

Items 2.4 and 3.1 of the Preventive Maintenance Procedure, included in this manual, specify the schedule for margin testing. Diagnostic programs are run each week under a different set of margin conditions. Once a month a typical customer job is run at margins.

SCHEDULED MAINTENANCE

The Preventive Maintenance Index (PMI) is a schedule of maintenance activities to be performed periodically. The associated Preventive Maintenance Procedures (PMP) contain detailed instructions for each item listed in the PMI.

The PMI and PMP in this manual cover only the AC104 Central Processor, the DC111 Communication Channel, and CR105 Console.

PREVENTIVE MAINTENANCE INDEX

Level 1: Daily	
Level 2: Weekly or	150 hours
Level 3: Monthly or	500 hours
Level 4: Quarterly or	1500 hours
Level 5: Semi-annually or	3000 hours
Level 6: Annually	

TABLE 11-4. PREVENTIVE MAINTENANCE INDEX

Level	Item	Procedure
1	1.1	Check fans and blowers
1	1.2	Check power supply voltmeters
1	1.3	Check keyboard and register displays
1	1.4	Run diagnostic routines
1	1.5	Clean equipment exterior
2	2.1	Clean CPU air filters
2	2.2	Clean console filters
2	2.3	Check console typewriter
2	2.4	Run diagnostic routines at margins
2	2.5	Check console switches and indicators
3	3.1	Margin test a typical customer job
3	3.2	Clean cabinet interiors
3	3.3	Seat 50-Paks in Central Processor and console
4	4.1	Check meter calibration in CPU
4	4.2	Check power supply ripple in CPU
4	4.3	Check meter calibration in console
4	4.4	Check power supply ripple in console
5	5.1	Data parity test
6	6.1	Shock test CPU

PREVENTIVE MAINTENANCE PROCEDURES

1.1 Check Fans and Blowers

CHECK/Conditions	Action
1. Check for proper air flow in all six central processor columns.	
2. Check to see that all four fans in the console are operating.	

CHECK: Are blowers and fans O.K. ?

Yes → Go to next item

No → Shut down central processor or console until blowers are repaired.
Reference: Power wiring diagrams in Customer Engineering Manual.

1.2 Check Power Supply Voltmeters

CHECK/Conditions	Action
1. Check meters on all six CPU power control panels. Meters should read zero for +6V, -6V, and -2V. Note Two of the columns in Unit 1 do not have +6V.	
2. Check to see that the motor on the terminator power supply in Unit 2 reads zero.	
3. Check meter in console power assembly. Meter should read zero for the +6V and -6V setting.	
CHECK: Are meters O.K.? Yes ↓ Go to the next item No →	Adjust power controls to zero meters.

1.3 Check Keyboard and Register Displays

CHECK/Conditions	Action
1. Enter the Communication register with a quantity containing all digits (0-7). Check for correct display.	
2. Select the A Register entry and display switches. Enter all 7's and check for proper display. Repeat for Q, P, and Index registers.	
3. See that register display lights when selected for E_U, E_L, LJA, and CIR.	
4. Check Read/Write Register File functions. a. Set Breakpoint Mode switch to REG. b. Set Breakpoint Switches to any Register File address ($00\text{-}77_8$). c. Press WRITE STO switch. d. Enter all 7's. e. Press READ STO switch. f. Check C-Register display for all 7's. g. Repeat items c through f for all 0's.	
CHECK: Do items 1 through 4 work properly? Yes ↓ Go to next item. No →	Troubleshoot and repair.

497

1.4 Run Diagnostic Routines

CHECK/Conditions	Action
1. Run the following diagnostic routines at normal operating voltages: a. COM - Command Test Run one pass. Specify a different initial pass number each day so that new sets of random numbers are used daily. This may find number sensitive failures over a period of time. b. LOG - Logic diagnostics Run one pass. B5P c. BDP - Business Data Processor Test Run one pass. Specify all sections of the test including Illegal Write and Interrupt testing. Do not run the long tests for 66.0, 66.1, 67.0 and 67.1 instructions specified by setting bits in Q. d. EX2 - Executive Mode test Run one pass.	
CHECK: Do all diagnostics run without indicating errors?	
Yes ↓ Go to next item No →	Troubleshoot and repair.

1.5 Clean Equipment Exterior

CHECK/Conditions	Action
	1. Inspect exterior of equipment and clean as necessary. Close all doors. Turn system over to customer.

2.1 Clean CPU Air Filters

CHECK/Condition

1. CPU power off

Action

1. Remove the six air filters in the CPU. The filters are located inside the power supply grilles at the base of each column.
2. Wash the filters using the following procedure:
   a. Flush with warm water. Do not use a high pressure stream.
   b. Shake out moisture and let dry thoroughly.
   c. Spray intake side of filters with a light coat of Super Filter Coat adhesive, CDC Part No. 12210958.
   d. Let adhesive dry before replacing filters.

   Go to next item

2.2 Clean Console Filters

CHECK/Condition

1. Console power off.

Action

1. Remove the air filter located immediately below the typewriter logic chassis at the rear of the console.
2. If there is any visible deposit of dust, clean and reactivate the filter. Follow the procedure used for the CPU filters (item 2.1).
3. Check the screens on the two muffin fans located in the upper right section of the console (viewed from rear). Remove any deposit with vacuum cleaner.

   Go to next item

2.3 Check Console Typewriter

CHECK/Conditions	Action
1. Typewriter power off 2. Typewriter power on	1. Check condition of ribbon and replace, if necessary. 2. Clean print ball. 3. Type complete character set. Go to next item

2.4 Run Diagnostic Routines at Margins

CHECK/Conditions	Action
1. Adjust the voltage and timing controls in the CPU and console to one of the combinations listed in Table 11-5. Select a different combination each week. During any six-month period, margin tests should be run at least once for each combination listed in the table. 2. Run the diagnostic tests listed in Table 11-5 for the selected margin combination. CHECK: Do all diagnostics run without indicating errors?	
Yes ↓ Turn system over to customer.	No → 1. Repeat failing test under normal operating conditions. a. If errors also occur at normal conditions, trouble-shoot and repair. b. If the errors do not repeat at normal conditions, make a record of the failure. Troubleshoot and repair during scheduled maintenance periods.

TABLE 11-5. MARGIN TESTS

Test Variables	Margin Combinations																
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Unit 1, Col 0, +6V	0	0	+	-	-	+	0	0	0	0	0	0	0	0	0	0	0
Unit 1, Col 0, -6V	0	0	+	-	+	-	0	0	0	0	0	0	0	0	0	0	0
Unit 1, Col 0, -2V	0	0	+	-	-	+	0	0	0	0	0	0	0	0	0	0	0
Unit 1, Col 1, -6V	0	0	+	-	+	-	0	0	0	0	0	0	0	0	0	0	0
Unit 1, Col 1, -2V	0	0	+	-	-	+	0	0	0	0	0	0	0	0	0	0	0
Unit 1, Col 2, -6V	0	0	+	-	+	-	0	0	0	0	0	0	0	0	0	0	0
Unit 1, Col 2, -2V	0	0	+	-	-	+	0	0	0	0	0	0	0	0	0	0	0
Unit 2, Col 0, +6V	0	0	+	-	-	+	0	0	0	0	0	0	0	0	0	0	0
Unit 2, Col 0, -6V	0	0	+	-	+	-	0	0	0	0	0	0	0	0	0	0	0
Unit 2, Col 0, -2V	0	0	+	-	-	+	0	0	0	0	0	0	0	0	0	0	0
Unit 2, Col 1, +6V	0	0	+	-	-	+	0	0	0	0	0	0	0	0	0	0	0
Unit 2, Col 1, -6V	0	0	+	-	+	-	0	0	0	0	0	0	0	0	0	0	0
Unit 2, Col 1, -2V	0	0	+	-	-	+	0	0	0	0	0	0	0	0	0	0	0
Unit 2, Col 2, +6V	0	0	+	-	-	+	0	0	0	0	0	0	0	0	0	0	0
Unit 2, Col 2, -6V	0	0	+	-	+	-	0	0	0	0	0	0	0	0	0	0	0
Unit 2, Col 2, -2V	0	0	+	-	-	+	0	0	0	0	0	0	0	0	0	0	0
Console +6V	0	0	0	0	0	0	+	-	+	-	0	0	0	0	0	0	0
Console -6V	0	0	0	0	0	0	+	-	-	+	0	0	0	0	0	0	0
Memory +6V	0	0	0	0	0	0	0	0	0	0	+5	-5	+2½	-2½	0	0	0
Memory -6V	0	0	0	0	0	0	0	0	0	0	+5	-5	-2	+2	0	0	0
Mem Drive Margin	0	0	0	0	0	0	0	0	0	0	N	N	N	N	*	N	N
Mem Bias Margins	0	0	0	0	0	0	0	0	0	0	N	N	N	N	N	H	L
Timing Margins	F	S	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
Diagnostic Tests																	
Com	X	X	X	X	X	X											
Log	X	X	X	X	X	X											
FPT	X	X	X	X	X	X											
B5P	X	X	X	X	X	X											
EX2	X	X	X	X	X	X											
MT1	X	X	X	X	X	X											
TP1							X	X	X	X							
PFT	X	X	X	X	X	X											
BC1	X	X	X	X	X	X											
MM4											X	X	X	X	X	X	X

*Drive margins are defined as a current regulator setting for each stack so that a margin of plus and minus 0.5 volts on either side of a nominal setting for each stack should have been previously determined during manufacture.

+	Means	+7 1/2 percent
-	Means	-7 1/2 percent
0	Means	0 percent
F	Means	all timing margins switches fast
S	Means	all timing margins switches slow
N	Means	all timing margins switches normal and memory drive margins and bias margins normal
H	Means	high
L	Means	low
+5	Means	+5 percent high
-5	Means	-5 percent low
-2 1/2	Means	-2 1/2 percent low
+2 1/2	Means	+2 1/2 percent high

2.5 Check Console Switches and Indicators

CHECK/Conditions	Action
1. Set the ISR and OSR to all 7's. Clear the ISR and OSR.	
2. Operate all console switches to see that they are working mechanically. See that all indicating switches light.	
CHECK: Do all switches and indicators operate properly?	
Yes ↓ Go to next item.	No → Troubleshoot and repair

3.1 Margin Test a Typical Customer Job

CHECK/Conditions	Action
1. Run one of the customer's production jobs at one of the margin conditions listed in Table 11-5. Compare results with same job run at normal operating conditions. A different margin condition should be selected each time this test is run.	
CHECK: Did job run O.K.?	
Yes ↓ Go to next item.	No → 1. Run diagnostic routines with same margin conditions to isolate error. 2. If diagnostic indicates error at margins, run diagnostic under normal operating conditions. 3. If error occurs only at margin condition, record error and troubleshoot during scheduled maintenance period. 4. If error occurs at normal operating conditions, troubleshoot and repair immediately.

3.2 Clean Cabinet Interiors

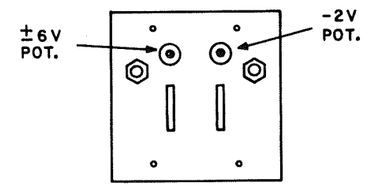
CHECK/Conditions	Action
1. Power off in CPU and console.	1. Inspect and clean inside of CPU cabinets. a. Logic chassis, six columns. b. Power supplies, six columns. c. Power Control Enclosures, six columns - accessible through top of cabinet. d. End section in Unit 2. e. Terminator power supply - four screws must be removed to free cover. 2. Check inside of console and clean as necessary. 3. Wipe down exterior of cabinets using a mild detergent solution. Turn system over to customer.

3.3 Seat 50-Paks in Central Processor and Console

CHECK/Conditions	Action
	Press each 50-Pak toward chassis to insure proper seating. Go to next item.

4.1 Check Meter Calibration in CPU

CHECK/Conditions	Action
1. Make certain that power supply meters read zero for +6v, -6v, and -2v in all six columns. Adjust power controls if necessary. Note Two of the columns in Unit 1 do not have +6v.	
2. Measure the voltage between a -6v bus and a ground bus in each column. Use a Triplett model 630 volt-ohmmeter. The reading should be -6.0v.	
3. Repeat for -2v in each column. The reading should be -2.0v.	
4. Repeat for +6v in the four columns that have +6v supplies. The reading should be +6.0v.	
CHECK: Do voltage readings meet specifications?	
Yes → Go to next item No →	1. Adjust potentiometer on rear of panel meter so that meter indicated zero when volt-ohmmeter reads correct voltage. Note Use 10-inch insulated screwdriver through back. Turn power off, when screwdriver is inserted. Turn power on when screwdriver is in place.
5. Check to see that meter on the terminator power supply reads zero. Adjust control if necessary.	



4.1

CHECK/Conditions

6. Measure the voltage between TB2 and TB3 on the terminator power supply panel. Use the Triplett volt-ohmmeter.

CHECK: Does volt-ohmmeter read 40.0 volts?

Yes → Go to next item.

No → Action: Adjust potentiometer on rear of panel meter so that meter reads zero when volt-ohmmeter indicates 40.0 volts.

4.2 Check Power Supply Ripple in CPU

The most common cause of high power supply ripple is open diodes in the rectifier assemblies. This procedure checks to see that all diodes are conducting.

CHECK/Conditions — Action

1. Computer stopped, power on.
2. Oscilloscope settings:
   a. Channel A Input Selector: AC position
   b. TIME/CM control: 0.5 ms/cm.
   c. TRIGGER COUPLING switch: AC
   d. TRIGGER SLOPE switch: INT(+)
   e. TRIGGER SOURCE: NORMAL
   f. TRIGGER MODE switch: AUTO STABILITY
   g. HORIZONTAL DISPLAY control: A
   h. 0.5 v/cm
3. Look at pin 11 on the transformers in the base of each column. You will see the AC component of the unfiltered DC output. Normal and abnormal waveforms are shown in Figure 11-4.

CHECK: Are waveforms normal?

Yes → Go to next item.

No → Action:
1. If waveform is similar to those on the upper right in Figure 11-4, a diode is bad.
2. Change TIME/CM control on scope to 1.0 ms/cm. Decrease v/cm control to give good display.

503

CHECK/Conditions	Action
	3. To find which of the six diodes in a rectifier assembly are open, look at the drop across each diode (place probe on transformer side of each diode). See Figure 11-4 for normal and abnormal waveforms. If one or more of the diodes in the assembly is open, the waveform will be similar to those on the lower right.
	4. Replace defective diodes and repeat ripple check.

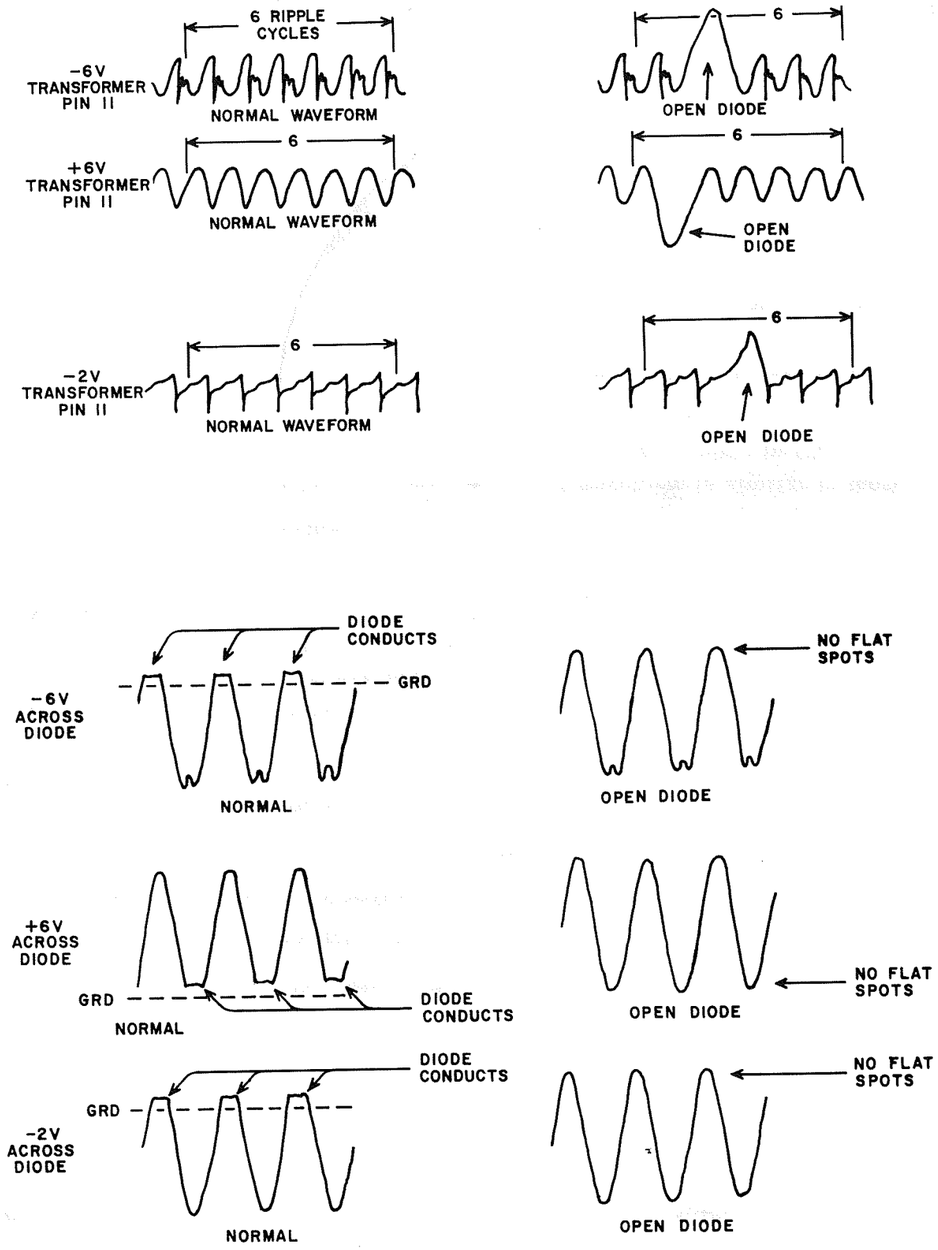


Figure 11-4. CPU Power Supply Waveforms

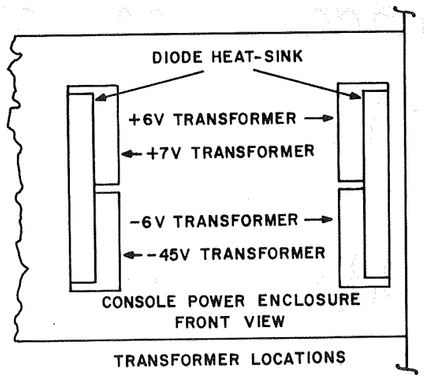
4.3 Check Meter Calibration in Console

CHECK/Conditions	Action
1. Check to see that the voltmeter at the rear of the console reads zero for +6v and -6v. Adjust power controls if necessary to zero meter.	
2. +6v/-6v switch: +6v position.	
3. Measure voltage between pins 3 and 4 of TB2 on the typewriter logic chassis. Use the Triplett model 630 meter.	
CHECK: Does Triplett meter read 6.0v?	
Yes → Go to next item.	No → 1. Adjust potentiometer on rear of console voltmeter so that meter indicates zero when Triplett meter reads 6.0v. The potentiometer is accessible from the front of the console (inside lower enclosure; remove door).

4.4 Check Power Supply Ripple in Console

This procedure insures that all diodes in the four console power supplies are conducting.

CHECK/Conditions	Action
1. Power on, computer stopped.	
2. Oscilloscope settings:	
a. Channel A Input Selector: AC position	
b. TIME/CM control: 0.5 ms/cm	
c. TRIGGER COUPLING switch: AC	
d. TRIGGER SLOPE switch: INT(+)	
e. TRIGGER SOURCE: NORMAL	
f. TRIGGER MODE switch: AUTO STABILITY	
g. HORIZONTAL DISPLAY control: A	
3. Look at pin 11 on the +6v and -6v transformers (see location sketch). You will see the AC component of the unfiltered DC output. Normal and abnormal waveforms are shown in Figure 11-4.	
4. Look at pin 4 on the +7v transformer. Again you will see unfiltered DC output. Figure 11-5 shows normal and abnormal waveforms.	



TRANSFORMER LOCATIONS

CHECK/Conditions	Action
5. Look at pin 10 or 11 of the 45v transformer. See Figure 11-5 for normal and abnormal waveforms.	
CHECK: Are waveforms normal?	
Yes → Go to next item.	
No →	1. If waveform is similar to those on the upper right in Figure 11-5, a diode is bad.
	2. Change TIME/CM control on scope to 1 ms/cm.
	3. To find which of the six diodes in a rectifier assembly are open, look at the drop across each diode (place probe on transformer side of each diode). See Figure 11-5 for normal and abnormal waveforms. If one or more of the diodes in the assembly is open, the waveform will be similar to those on the lower right.
	4. Replace defective diodes and repeat check.

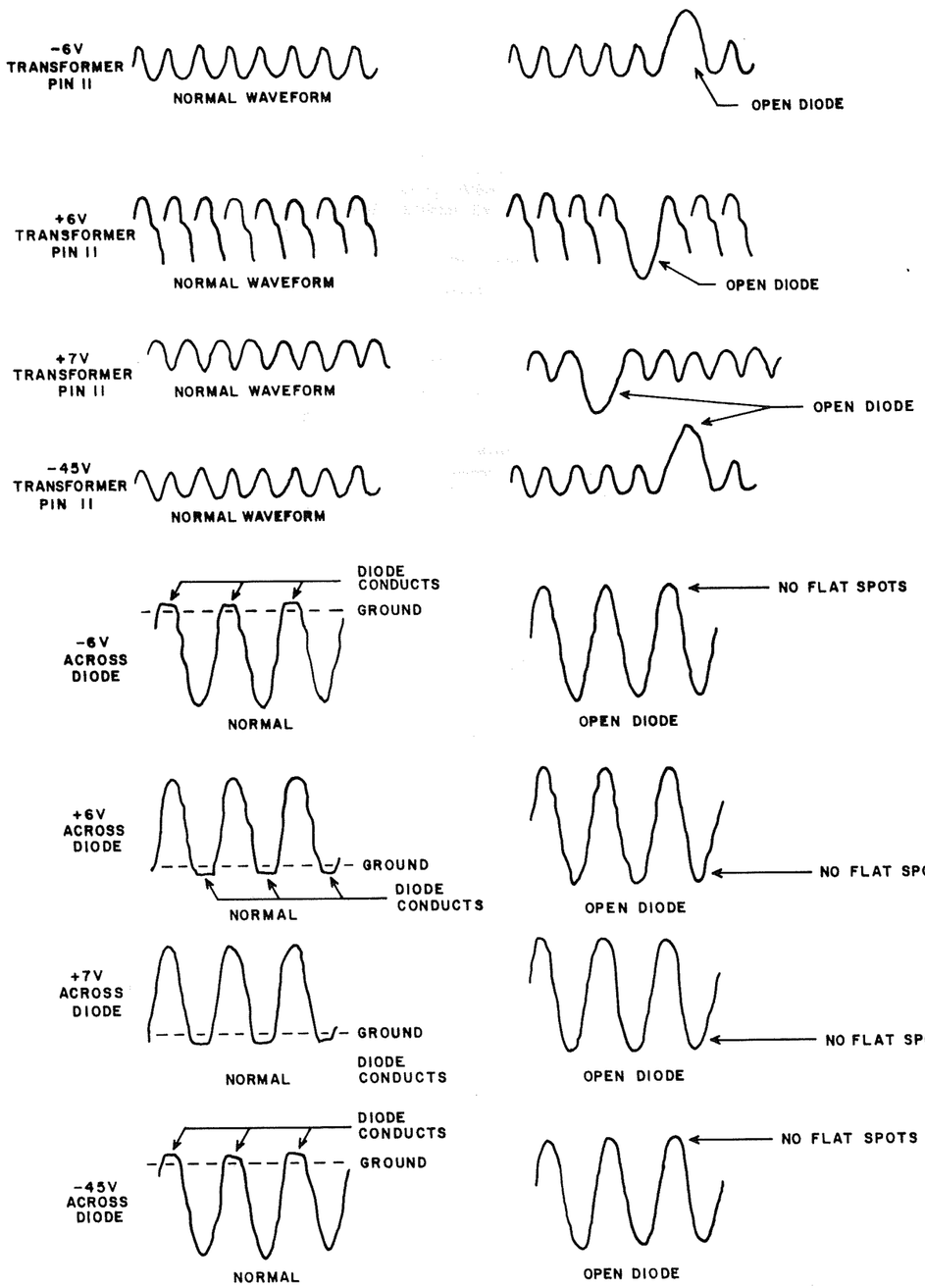


Figure 11-5. Console Power Supply Waveforms

5.1 Data Parity Test

This procedure verifies that the Data Parity Checker is functional.

CHECK/Conditions	Action
1. Enter all of memory with zeros and sweep continuous.	
2. Ground data bit zero by grounding the test point indicated below. If the Parity Checking network is working properly, this should turn the Storage Parity Error indicator ON.	
3. Master Clear and repeat for remaining 23 data bits.	

TABLE 11-6. DATA BIT TEST POINTS

Bit	Test Point	Location
00	BF	2B2A9
01	BH	2B2A9
02	BY	2B2A9
03, 04, 05	BF, BH, BY	2B2A8
06, 07, 08	BF, BH, BY	2B2A7
09, 10, 11	BF, BH, BY	2B2A6
12, 13, 14	BF, BH, BY	2B2A4
15, 16, 17	BF, BA, BY	2B2A3
18, 19, 20	BF, BH, BY	2B2A2
21, 22, 23	BF, BH, BY	2B2A1

6.1 Mainframe Shock Test

The mainframe should be completely shock tested annually. Shock must be done in sections with a maximum of one column per week.

NOTE

Do not exceed the limit of one column per week for the shock test. This limit will preclude any massive, latent-type problems from degrading the system operation.

Use the AMP insertion tool calibrated to 10 pounds and the special 50-PAK shock testing head. Shock test the PAKS by rapping each once in the middle of the PAK, while running the appropriate test shown in Figure 11-6.

Additional test information and a 20-panel map is shown in Figure 11-6.

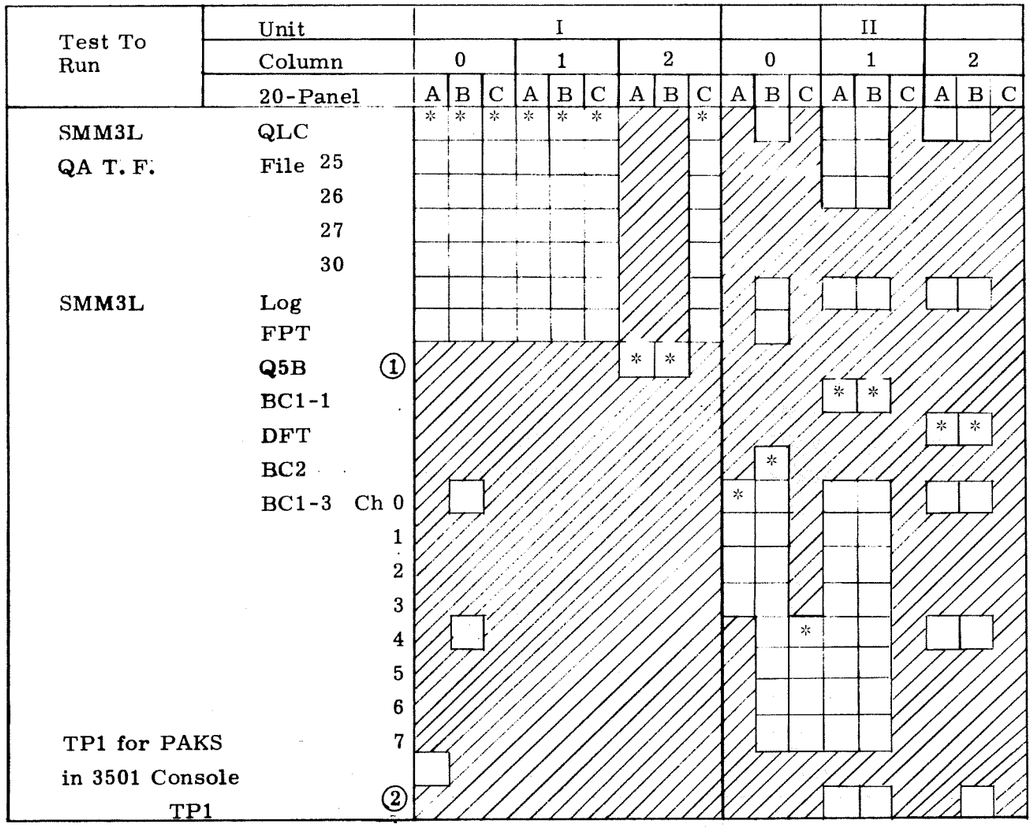


Figure 11-6. 20-Panel Shock Testing Map

* While running, use the 6000-type shock testing head (Part No. 12209308) to shock test indicated backpanels by rapping three times across the center of the panel and once at each corner.

① Additional PAKS to be tested with this test are at locations 1B1B5, 1C0A6, and 1C0A5.

② Additional PAKS to be tested with this test are at locations 2B1B8 and 2B1B9.

EMERGENCY MAINTENANCE PROCEDURES

ADJUSTABLE DELAY TUNING PROCEDURE

Table 11-7 indicates the location of all adjustable delays in the central processor. It may be necessary to adjust these delays if:

1. A module containing an adjustable delay is replaced.
2. An adjustable delay circuit is replaced.
3. A circuit or module associated with an adjustable delay is replaced.

TABLE 11-7. DELAY ADJUSTMENT

Location of Delay Adjustment	Procedure Number
2B0B5-A10	No. 1
2A0A7-B00, B10, B40	
2A0A6-B00, B10, B40	
2A0A3-B00, B10, B40	
2A0A3-B00, B10, B40	
2A0A2-B00, B10, B40	No. 2
2C0B7-B00, B10, B40	
2C0B6-B00, B10, B40	
2C0B3-B00, B10, B40	
2C0B2-B00, B10, B40	
2B1B1-A00	No. 3
2B1B1-B10, A30	No. 4
2B1B1-B20	No. 5
2B0A9-B00, B40	No. 6
2B1B8-B40	No. 7
2A2B9-A20	No. 8
1A2A2-A40	No. 9

GENERAL PROCEDURE

1. A short program loop that repeatedly pulses the delay to be adjusted is run.
2. The output of the delay and a signal that has a specified time relationship to the delay output are simultaneously displayed on an oscilloscope.
3. The delay potentiometer is adjusted to give the specified time relationship between the leading edges of the two signals.

Detailed procedures for each delay appear on the following pages.

A Tektronix type 547 oscilloscope, or equivalent, with a Type 1A1 dual channel preamp, is required.

The oscilloscope should be set up to sync internally on the signal observed with probe A.

Unless otherwise specified in the adjustment procedures, the computer should be in Non-Executive mode.

PROCEDURE 1

Location of delay adjustment: 2B0B5-A10.

Function: Controls 40-millisecond delay for Pause instruction (77.60 XXXX).

Reference: Logic diagram, page 6-107.

Procedure:

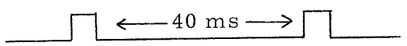
1. Enter the following program from the keyboard:

Address	Instruction	
00000	76000000	Activate channel that is not connected.
00001	00000000	
00002	00000000	
00003	53420022	Clear Real Time Clock
00004	77600377	Pause for 40 ms
00005	01000007	Jump to 00007
00006	00000000	
00007	53010022	Clock to Q
00010	41000100	Store Q at 00100
00011	01000003	Jump to 00003

2. Set console switches as follows:
   a. READ STO switch: ON
   b. BREAKPOINT Mode Selector switch: STO position
   c. BREAKPOINT Address: 00100
   d. STEPRATE CONTROL: maximum rate
3. Master clear and press the GO switch. The Communication Register display will show the delay in milliseconds (in octal 50_8).
4. Adjust the potentiometer at 2B0B5-A10 for 40_{10}-milliseconds delay.

If the console is not visible from the Central Processor, the scope can be used to measure the delay.

1. Probe A on 2B0B5-TP AQ
2. Adjust the potentiometer at 2B0B5-A10 for 40 milliseconds between pulses.



PROCEDURE 2

Location of delay adjustments: locations B00, B10, and B40 on the C-control module for each communication channel. The C-control modules are located as follows:

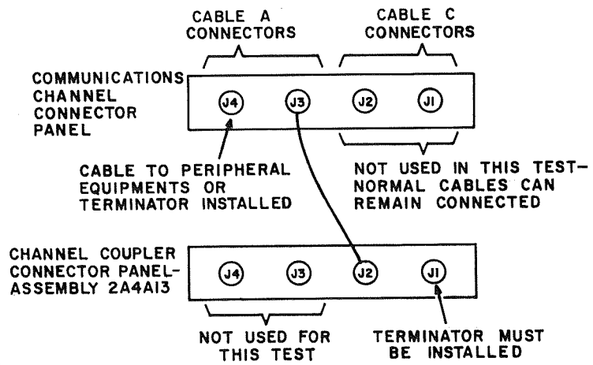
Channel 0	2A0A7	Page 6-133
Channel 1	2A0A6	Page 6-135
Channel 2	2A0A3	Page 6-137
Channel 3	2A0A2	Page 6-139
Channel 4	2C0B7	Page 6-169
Channel 5	2C0B6	Page 6-171
Channel 6	2C0B3	Page 6-173
Channel 7	2C0B2	Page 6-175

Functions:

1. Delay at B10 causes Data signal to be sent 100 nanoseconds after data is placed on lines during output operation.
2. Delay at B40 causes Data signal to drop 100 nanoseconds after external equipment sends Reply during input or output operation.
3. Delay at B00 controls the setting of the Data Signal FF 200 nanoseconds after the previous Data Signal drops.

Procedure:

1. Connect the channel to be adjusted to the channel coupler as shown in the following illustration.



2. Set the CHANNEL MODE switch for the channel connected to the Channel Coupler to 12-Bit Mode.
3. Set CHANNEL COUPLER switch on maintenance panel to A OR B TO A AND B (down) position.
4. Enter the following program from the keyboard:

Address	Instruction	
00000	76400000	Output word from A
00001	C0000000*	On channel C
00002	00000000	Halt
00003	01000000	Jump to 00000

5. Master Clear and press Go switch.
6. Probe A on TP BF on C control module for the channel C_A.
7. Probe B on TP BC of the C-control module for the channel being adjusted.
8. Adjust the potentiometer at location B10 of this module for 100-nanosecond delay from leading edge of A trace to leading edge of B trace.
9. Probe A on TP BD of the C-control module for the channel being adjusted.
10. Probe B on TP BE of the same module.
11. Adjust the potentiometer at location B40 for 100-nanosecond delay from leading edge of A trace to leading edge of B trace.
12. Probe A on TP AY of the C-control module for the channel being adjusted.
13. Probe B on TP BG of the same module.
14. Adjust the potentiometer at B00 for 100-nanosecond delay from leading edge of A trace to leading edge of B trace. This 100-nanosecond delay and the 100-nanosecond delay previously adjusted provides a 200-nanosecond delay between the trailing edge of the Data Signal and the setting of the Data Signal FF.

PROCEDURE 3

Location of delay adjustment: 2B1B1-A00

Function: Master Clear Block Control priority circuits after 15 μsec if Master Clear does not gain priority.

Reference: Logic diagram, page 6-9.

Procedure:

1. MAINTENANCE MODE switch (on maintenance panel): ON.
2. TEST MODE switch (on maintenance panel): ON.
3. Key-operated MAINTENANCE MODE switch on console: ON.
4. Ground TP AW at location 2B1A0 (page 6-5).
5. Probe A on 2B1B1-TP AW.
6. Probe B on 2B1B1-TP AE.
7. Adjust potentiometer at 2B1B1-A00 for 15-μsec delay from leading edge of A trace to leading edge of B trace.

* C = Number of channel connected to channel coupler

PROCEDURE 4

Location of delay adjustments: 2B1B1-B10, 2B1B1-A30

Function: Generates no-response reject for Connect and Select Function instructions.

Reference: Logic diagram, page 6-9.

Procedure:

1. Enter the following program from the keyboard:

Address	Instruction	
00000	770CXXXX	(Connect)
00001	01000000	(Jump to 00000)
00002	00000000	Halt

   C = Channel Number for any channel in the system

   XXXX = Connect Code that does not correspond to any equipment on channel C. Thus, there will be no response to the Connect instruction and the exit will be to P+1.

2. Master Clear and press GO switch.
3. Probe A on 2B1B1-TP BF.
4. Adjust potentiometer at 2B1B1-B10 for 10-μsec pulse width.
5. Probe A on 2B1B1-TP AS.
6. Adjust potentiometer at 2B1B1-A30 for 90-μsec pulse width.

PROCEDURE 5

512

Location of delay adjustment: 2B1B1-B20

Function: Delays Control Enable FF for 250 nanoseconds after Connect code is transmitted to allow for deskew time.

Reference: Logic diagram, page 6-9.

Procedure:

1. Enter the following program from the keyboard:

Address	Instruction	
00000	770CXXXX	(Connect)
00001	01000000	(Jump to 00000)
00002	00000000	(Halt)

   C = Channel Number for any channel present in the system.

   XXXX = Connect code that does not correspond to any equipment on channel C.

2. Master Clear and press GO switch.
3. Probe A on any bit in the O register (for channel C) that corresponds to a "1" in the Connect code XXXX. The lower 12 bits of the O register hold the Connect code.

The O registers are located as follows:

Channel 0	2A0A9	Page 6-141
Channel 1	2A0A8	Page 6-145
Channel 2	2A0A1	Page 6-149
Channel 3	2A0A0	Page 6-153
Channel 4	2C0B9	Page 6-177
Channel 5	2C0B8	Page 6-181
Channel 6	2C0B1	Page 6-185
Channel 7	2C0B0	Page 6-189

4. Probe B on TP AO on the A-control module for channel C. The A-control modules are located as follows:

Channel 0	2A0B7	Page 6-125
Channel 1	2A0B6	Page 6-127
Channel 2	2A0B3	Page 6-129
Channel 3	2A0B2	Page 6-131
Channel 4	2C0A7	Page 6-161
Channel 5	2C0A6	Page 6-163
Channel 6	2C0A3	Page 6-165
Channel 7	2C0A2	Page 6-167

5. Adjust the potentiometer at location 2B1B1-B20 for 200 nanoseconds delay from leading edge of A trace to leading edge of B trace.

6. Repeat the measurement for all channels to be certain that no channel has less than 200 nanoseconds deskew time. If necessary, re-adjust the potentiometer at 2B1B1-B20 to obtain a minimum delay of 200 nanoseconds.

PROCEDURE 6

Location of delay adjustments:

1. 2B0A9-B00

   Function: Controls timing between Block Control and Main Control on 77 instructions handled by Block Control.

2. 2B0A9-B40

   Function: Blocks external interrupts during 77.500XXX instructions.

Reference: Logic diagram, page 6-101.

Procedure:

1. Enter the following program from the keyboard:

Address	Instruction	
00000	77500377	(Clear external interrupts)
00001	14000000	No-op
00002	01000000	(Jump to 00000)

2. Master Clear and press GO switch.
3. Probe A on 2B0A9-TP AH.
4. Adjust potentiometer at 2B0A9-B00 for 100-nanosecond pulse width.
5. Probe A on 2B0A9-TP BX.
6. Probe B on 2B0A9-TP BZ (a very narrow pulse will be visible).
7. Adjust potentiometer at 2B0A9-B40 for 1-μsec delay from leading edge of A trace to leading edge of B trace.

PROCEDURE 7

Location of delay adjustment: 2B1B8-B40

Function: Delays Data Ready signal to typewriter.

Reference: Logic diagram, page 6-11.

Procedure:

1. Turn on FAKE RESUME switch inside back of console.
2. Enter the following program from the keyboard:

Loc	00000	77760000	(Set Typewriter Output)
	00001	01000000	(Jump to 00000)

3. Probe A on 2B1B8-TP BZ.
4. Probe B on 2B1B8-TP BY.
5. Adjust potentiometer at 2B1B8-B40 for 250-nanosecond delay from leading edge of A trace to leading edge of B trace.

PROCEDURE 8

514

Location of delay adjustment: 2A2B9-A20

Function: Generates No-Response signal if storage does not respond to a Memory Request within 2.5 μsec.

Reference: Logic diagrams, pages 5-23 and 5-5.

Procedure:

1. EXECUTIVE MODE switch ON.
2. Enter all zeros into page index 000 from keyboard.
3. Enter the following quantity into page index 001 from the keyboard: $000XXX000000_2$.

   Where XXX_2 = the module select bits (address bits 15, 16, and 17) for a non-existent storage module.
4. Enter the following program from the keyboard:

Address	Instruction	
00000	20004000	Load A through page index 001
00001	01000000	Jump to 00000

5. PARITY STOP and PARITY INTERRUPT switches OFF.
6. Master Clear and press the GO switch.
7. Probe A on 2A2B9-TP AT.
8. Probe B on 2A2B9-TP AO.
9. Adjust the potentiometer at 2A2B9-A20 for 2.5-μsec delay from leading edge of A trace to leading edge of B trace.

PROCEDURE 9

Location of delay adjustment: 1A2A2-A40

Function: Exit from BDP instructions (64-67).

Reference: Logic diagrams, pages 4-9 and 4-3.

Procedure:

1. BDP MODE switch ON.
2. Enter the following program from the keyboard:

Address	Instruction	
00000	14400000	Enter A with all zeros
00001	40000000	Store zeros at 00010
00002	70600010	Load BDP Conditions from 00010
00003	64000000	
00004	00000000	Move Characters from field A to field C
00005	00000000	
00006	10000003	Jump to 00003

3. Master Clear and press GO switch.
4. Probe A on 1A2A2-TP AG (page 4-9).
5. Probe B on 1A2A4-TP AM (page 4-3).
6. Adjust potentiometer at 1A2A2-A40 for 150-nanoseconds delay between leading edges.

BACK PANEL AND GROUND PIN REPLACEMENT PROCEDURES

1. Connector Pins
   a. From the front of the cabinet, carefully position Receptacle Extraction Tool, Part No. 18934700, over the defective pin. Hold the "barrel" of the tool firmly against the panel, then hit the plastic handle sharply with the heel of the hand to dislodge the pin.
   b. From the back of the panel, install a replacement double-pin assembly using Insertion Tool, Part No. 12213237, then disconnect the back panel wires from the old pin assembly and connect them to the corresponding new pins.

NOTE

If two people are to handle pin replacement, one person should hold Insertion Tool, Part No. 12213238, against the pin side of the plate (for support only) while the other person drives in the new pin assembly from the back of the panel.

2. Ground Pins
   a. Remove ground wire, if present, then drive out the defective ground pin from the back of the panel using Ground Pin Punch, Part No. 12213236.
   b. Install new ground pin from the front side of the panel using Ground Pin Insertion Tool, Part No. 12213235. Use care to insure that the pin is not driven too far back into the panel; otherwise, it may not make proper connection with the 50-PAK. Reinstall ground wire (if present).

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