CONTROL DATA® 1700
COMPUTER SYSTEM

1704-A/B, 1705-A, 1708-A
(Including Standard Options
10040-10043), AA101-A/B

DIAGRAMS &
CIRCUIT DESCRIPTION
CARD PLACEMENT

CONTROL DATA
CORPORATION

CUSTOMER ENGINEERING MANUAL

RECORD of REVISIONS

REVISION	NOTES
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FORM CA 230-2

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FORM CA 230-2

FOREWORD

The 1700 Customer Engineering Manual provides logic diagrams and circuit descriptions of the CONTROL DATA* 1700 Computer System. This manual contains information on all units contained in the main computer cabinet with the exception of the Basic Peripheral Equipment, which is in Publication Number 60164200.

The circuit descriptions and diagrams are arranged to give a general continuity of logic flow. Thus, the Clock and Timing controls are given first, followed by the Register groupings, Adder/Shifter, etc. A special reference is made to the Command Timing sequences. These sequences give the detailed timing of each instruction. Thus, the Command Timing sequences logically interconnect various diagrams on a timed sequence basis. Refer to the 1700 Computer System Command Timing Charts, Pub. No. 60194500.

The logic diagram symbol description and the block diagram description precede the detailed circuit descriptions. The Logic Diagram Symbol section lists each of the standard logic symbols used on the diagrams and a brief description of their meaning and use.

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CONTENTS

Part 1. Diagrams

CONTENTS (Cont'd)

PART 1

DIAGRAMS AND CIRCUIT DESCRIPTION

MAIN COMPUTER

Two signals, a logical "0" and a logical "1", are the possible input or output conditions of a circuit. By convention, "1" is considered "up" and "0" is considered "down" on a timing chart, for example. Detailed descriptions of logic symbols and their associated electronic representations are contained in the Printed Circuits Manual, Vols. 3 and 4.

STANDARD LOGIC SYMBOLS

The 1700 Computer logic is mainly composed of the CONTROL DATA 6000 Series printed circuit modules. Standard logic diagram symbols for this type of printed circuit modules are inverters, test points, flip-flops, and twisted pair line drivers.

INVERTERS

An inverter is a logic element which provides an output that is an inversion of its input. When an inverter receives more than one input, "0's" take precedence over "1's" and drive the output of the inverter to "1". Because all of the several inputs have to be "1" to drive the output of the inverter to a "0", the inverter may be considered an inverting AND (or NAND) gate when more than one input is present. Logic diagrams show the basic inverter as an arrow into either a circle or a square (see Figure 1). Both symbols represent the same electronic circuit and have the same logical interpretation. In a logic sequence of inverters, circle and square symbols are usually alternated as an aid in tracing signals, e.g., a "1" output from a square symbol implies a "1" output from subsequent squares in the logic chain if each symbol in the chain has only one input.

Acceptable conventions for showing multiple inputs and outputs are given in Figure 2. Note that the output of inverter A is "0" only if inputs X, Y, and Z are all "1". The multiple outputs are identical.

Figure 3 shows an example of an inverter network. Because multiple outputs are identical, Figure 4 shows only one arrow in cases where an inverter (A) serves as the single input to several succeeding inverters. In more complex inverter networks, multiple arrows are used (B to C and D because B is not the only input to C or D).

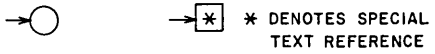


Figure 1. Inverter Symbols

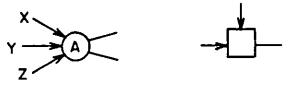


Figure 2. Multiple Inputs/Outputs

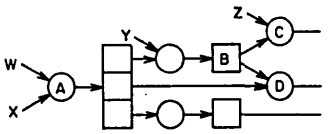


Figure 3. Inverter Networks

TEST POINTS

A test point performs no logic function. Logic diagrams show the test point as a triangle (see Figure 4). Test points are numbered from 1 to 6.

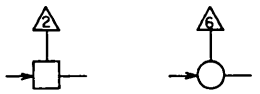


Figure 4. Test Point Symbols

FLIP-FLOPS (FF)

The flip-flop is composed of two inverters and functions as a storage device with two stable states designated as set and clear (see Figure 5). The flip-flop is set when the set output (B) is a "1" and clear when it is a "0". Note that the input (A) must be "0" to set the flip-flop, and (C) must be "0" to clear it.

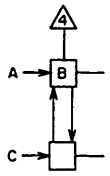


Figure 5. Flip-Flop Symbol

WIRE TAB DESIGNATIONS

Wire tab designations written next to a pin indicate where in the drawings the pin is connected. 3,5,7 - C37 - 6 indicates a connection with pin 6 of module C37, found on pages 3, 5, and 7. See Figure 5.1.

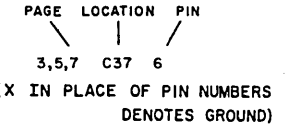


Figure 5.1. Wire Tab Designations

TWISTED PAIR DRIVERS

A Line Driver circuit transmits logic signals from one module to another. Modules are connected by twisted-pair lines. The standard square or circle represents the twisted-pair driver. However, the output of the square or circle connects to a pin of the module. The pin is then wired to a pin on another module (see Figure 6). The ground wire of the pair is wired to the connector ground bus of each module. The pins are represented by small circles and are numbered from 1 to 28. (Pins 29 and 30 are ground and +6 volts, respectively, and generally are not shown in logic diagrams.) The module location is shown above the card, and the module type is denoted in the upper right-hand corner.

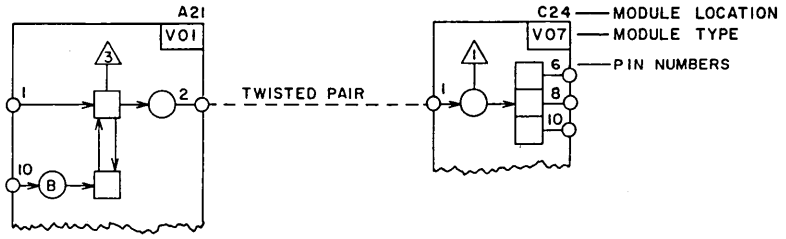


Figure 6. Twisted-Pair Line Driver

RECEIVER/TRANSMITTER CIRCUITS

The Receiver and Transmitter circuits detect and transmit signals from and to I/O interface respectively. The Receiver and Transmitter circuits are modifications of the standard 3000 Series circuits of the same name. These circuits are contained on a printed circuit module along with the standard inverter circuits.

Figures 7 and 8 shows that Receiver and Transmitter circuits are represented by the square symbol with an "R" or "T" respectively. The two inputs to the receiver are each connected to two pins on the module.

In Figure 7, a "1" input to R is inverted, causing a "1" output from pin 6 and a "0" output from pin 13. Thus, with a "1" input, the Receiver circuit produces both True and Not outputs.

The Transmitter circuit receives a "1" input signal from a standard inverter or FF and transmits a "1" output signal to the I/O interface. In Figure 7, a "1" input to pins 7 and 9 causes a "1" output from T and thus to the I/O line.

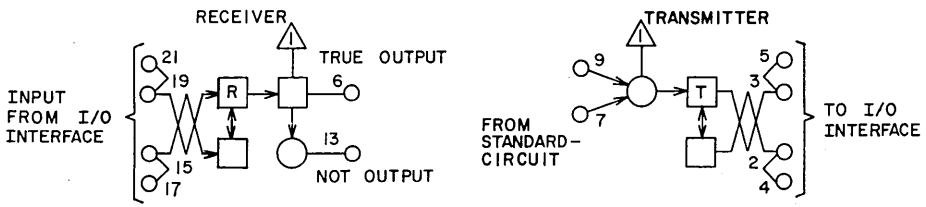


Figure 7. Receiver/Transmitter Circuit Examples

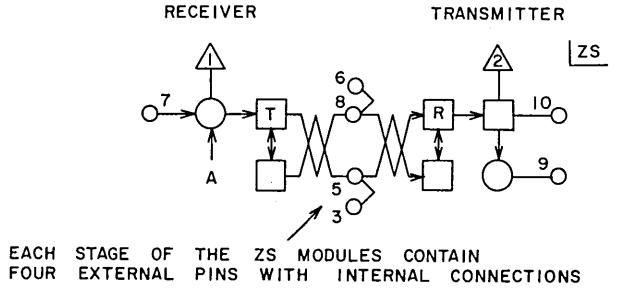


Figure 8. Z5 Transmitter/Receiver Module

SPECIAL CIRCUITS

In addition to the standard symbols, the diagrams also use symbols representing special nonstandard circuits. The symbols for these circuits along with a brief description are given below.

Special variations of the standard building block are indicated by the symbols shown on Figure 9. The symbol and schematic for the corresponding special circuit are shown on the applicable logic diagram and also on the module schematic in the Printed Circuits Manual.

Figure 9. Special Circuits

CAPACITIVE DELAY CIRCUITS

Capacitive Delay circuits delay input "1" signals a prescribed time before issuing an output "1" signal. The 1700 uses both fixed and variable delay circuits. Figure 10 shows examples of both types. The delay time of the circuit and capacitor value are listed beside the capacitor symbol. The variable potentiometer enables adjustment of the delay time of the circuit within certain limits.

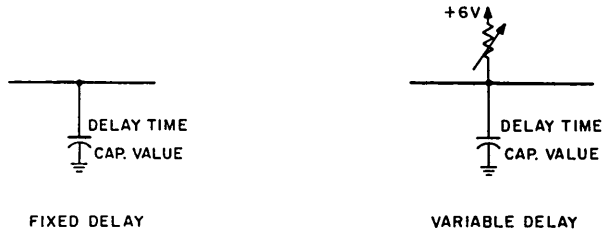


Figure 10. Capacitive Delay Circuits

BLOCK DIAGRAM

The block diagram shows the main circuits in the 1704 Arithmetic and Control portion of the CONTROL DATA 1700 small industrial computer. The I/O and memory interfaces are indicated.

As shown, the 1704 consists mainly of registers, the adder/shifter network, and control circuits. In general, the registers contain quantities for some period of time. When the quantities require an Arithmetic, Logical, or Transfer operation, they are transmitted through the adder/shifter network. The adder/shifter combines the quantities with one another in a Logical or Arithmetic operation, operates on them independently as in a shift, or simply serves as a path for the contents of one register to transfer to another register. Thus, the adder/shifter serves as the main path for all Arithmetic, Logical, or Inter-Register Transfer operations.

MAIN REGISTERS

The function of the main registers shown on the block diagram is briefly described in the following paragraphs.

Z REGISTER

The 18-bit Z register temporarily stores all data words being read from or written into storage. Bits 16 and 17 are not part of the data but are the program protect and parity bits respectively. Control operates on these bits independently from the data bits.

In a Read Memory operation, the 16 data bits transfer to the X register. In a Write operation, the data bits to be written are transferred from X to Z register.

X REGISTER

The 16-bit X register holds the data bits transferring to or from the Z register. This register holds one of the parameters in most Arithmetic operations. When the X register contains an instruction, the high-order 8 bits transfer to the F register for translation.

F REGISTER

The 8-bit F register contains the instruction code and/or addressing mode bits. The translation of these bits direct the execution of the instructions.

Y REGISTER

The 16-bit Address register contains the storage address for transfer to the S register during a storage reference. The Y register in conjunction with the Y Decrementer also functions as a counter during the multiply and shift instructions. The Y register temporarily stores the incomplete addresses during address modification and the final effective address when modification is complete.

S REGISTER

The 15-bit Storage Address register contains the effective storage address transferred from the Y register or from the external storage access. All address selection for internal storage access is controlled by the contents of the Y register.

P REGISTER

The 15-bit P register contains the program address of the instruction currently being executed. In the later stages of instruction execution, except in certain Jump and Skip instructions, the P register is advanced by adding +1 in the adder/shifter network for referencing the next instruction.

A REGISTER

The 16-bit A register functions as the principal register in most Arithmetic and Logical operations.

Q REGISTER

The 16-bit Q register serves as the auxiliary register in most Arithmetic and Logical operations.

MASK REGISTER

The 16-bit Mask register contains the interrupt mask bits. Each bit in the Mask register corresponds to a particular interrupt line. In order for a particular type of interrupt to be recognized when it occurs, the corresponding bit in the Mask register must be a "1".

ADDEND/AUGEND GATES

The addend/augend gates serve as the input gate control for the adder/shifter. In most Arithmetic, Logical, or Register Transfer operations, one input is selected by the addend gates and one by the augend gates. Thus, four inputs are applied to addend and augend gates respectively.

ADDER/SHIFTER

The adder/shifter performs all Arithmetic and Logical operations on the register contents. The adder/shifter also serves as the transfer path for all Inter-Register Transfer operations.

MAIN CONTROL

The main control circuits are shown on the right side of the block diagram.

MANUAL CONTROLS

The manual controls consist of the start, stop, manual set, and indicator control circuits. Thus, the manual controls initiate all start, stop, and manual selection operations in the computer.

CLOCK

The clock circuit produces 4-phase, 25-nsec clock pulses which form the timing base for all control operations in the computer.

TIMING CHAIN

With an input from the clock and manual controls, the timing chain produces a series of eight controlled 25-nsec timing pulses at 50-nsec intervals.

SEQUENCE CONTROL

The sequence control circuit controls the mode of operation for the execution of a given instruction. There are five general modes of operation:

1) Read Next Instruction (RNI)
2) Address Mode (ADR)
3) Read Operand (ROP)
4) Store Operand (STO)
5) Register Transfer Mode (REG)

The execution of an instruction may pass through two or more modes of operation. All instructions begin in the RNI mode and then enter one or more of the other modes in sequence.

CYCLE CONTROL

Three main timing cycles control instruction operation: the A cycle, B cycle, and C cycle. The A cycle begins with an initial start or resume from storage. The A cycle enables such operations as addressing, initial register transfers, etc.

The B cycle is initiated immediately after the A cycle except in multiply, divide, and shift operations. The B cycle initiates storage operations.

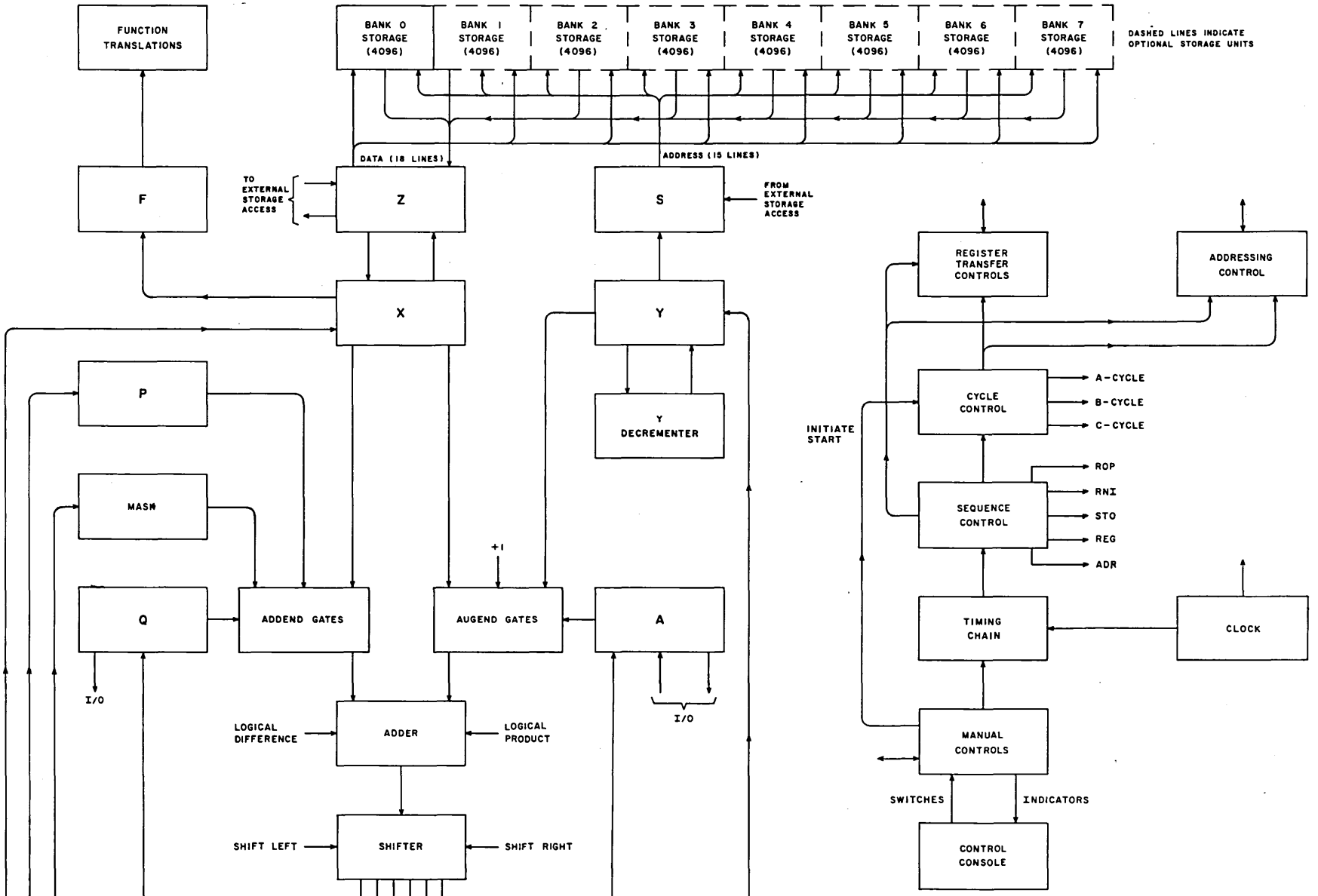
The C cycle begins after the A cycle and performs multiply, divide, or shift cycle iterations.

REGISTER TRANSFER CONTROLS

This circuit controls the transfer of registers in the computer based on the cycle, sequence mode, and instruction being executed.

ADDRESSING CONTROL

This circuit controls the modification of the address in storage reference instruction. The addressing control circuit receives inputs from cycle control, sequence control, and the address control bits in the instruction.

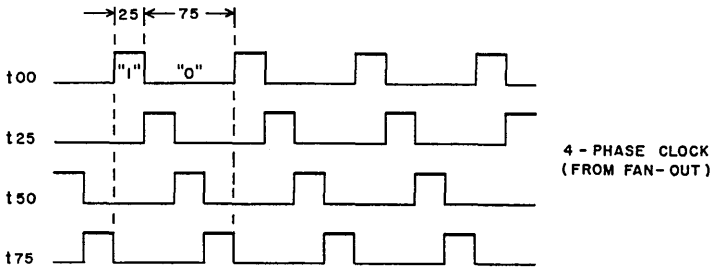


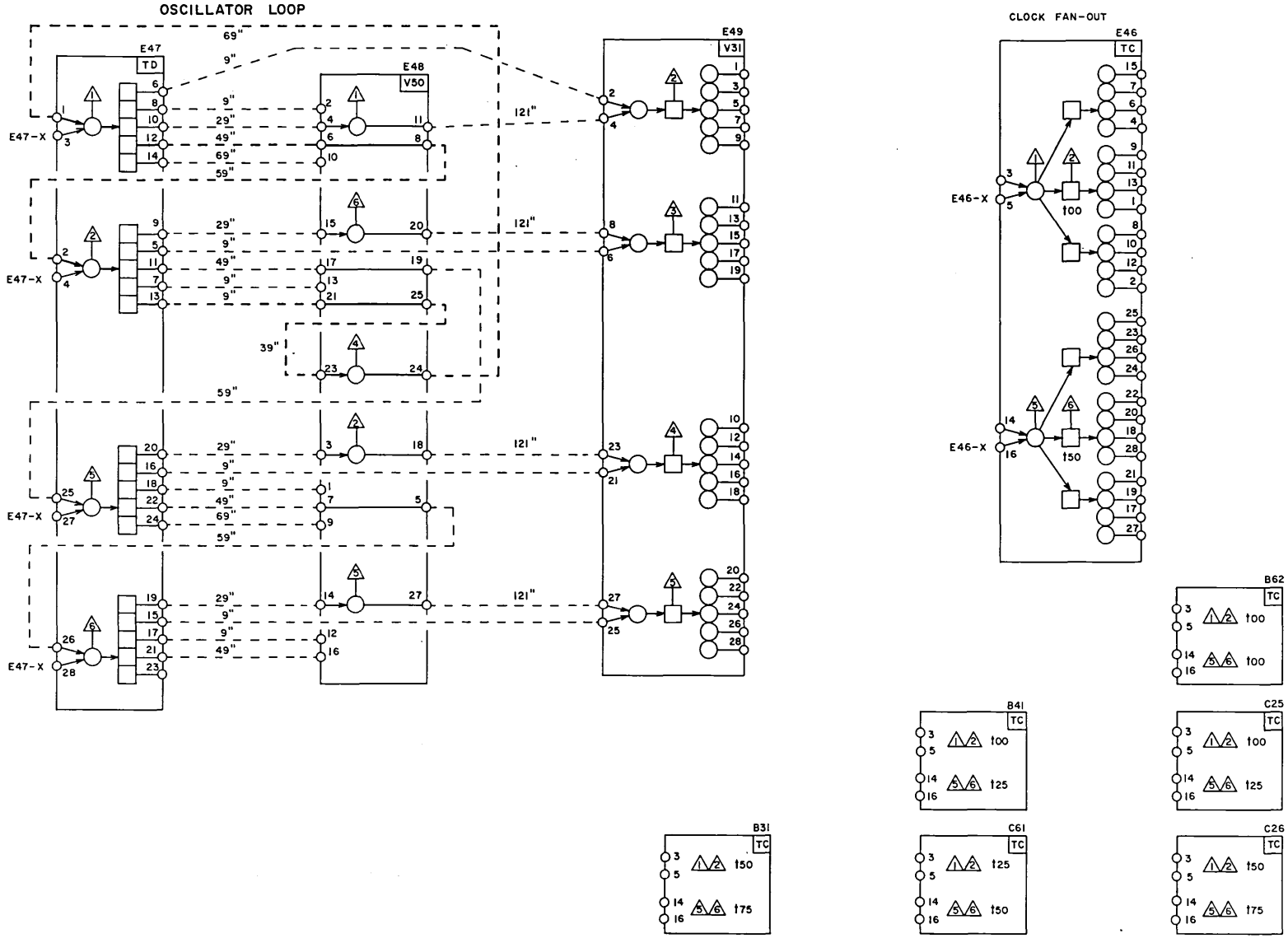
CONTROL DATA CORPORATION	TITLE: BLOCK DIAGRAM — MAIN ARITHMETIC AND CONTROL	PRODUCT 1700	
COMPUTER DIVISION		SIZE C · DRAWING NO. 60152700 · REV A	
		SHEET 4 · PAGE 1	

MASTER CLOCK - NORMAL SPEED

Timing in the 1700 is controlled by a 4-phase master clock. Four 25-nsec pulses are issued each minor cycle to control movement of data and instructions.

The master clock oscillator consists of a TD module and a V50 module. To form the 25-nsec pulses, a pulse from the TD is ANDed with a similar pulse which has been delayed and inverted by the V50. The result is a series of pulses (primary clock) which are fanned out through V31 and TC modules to be used as timing control.





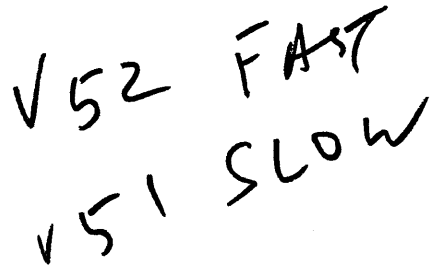
CONTROL DATA CORPORATION	TITLE: CLOCK – NORMAL SPEED	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C · DRAWING NO.: 60152700 · REV: U	
		SHEET: 5 · PAGE: 3	

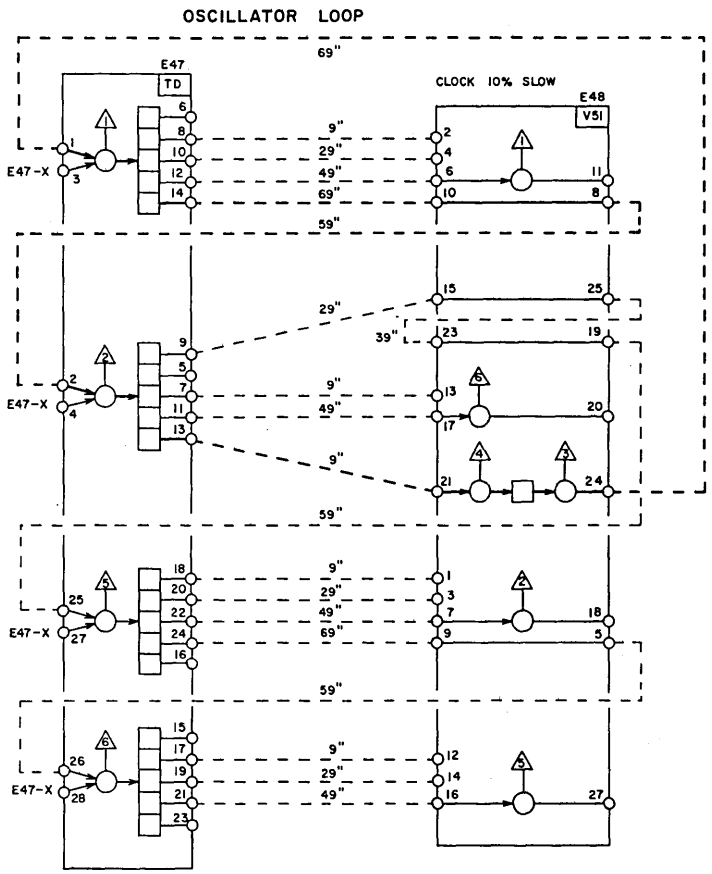
MASTER CLOCK - SLOW AND FAST

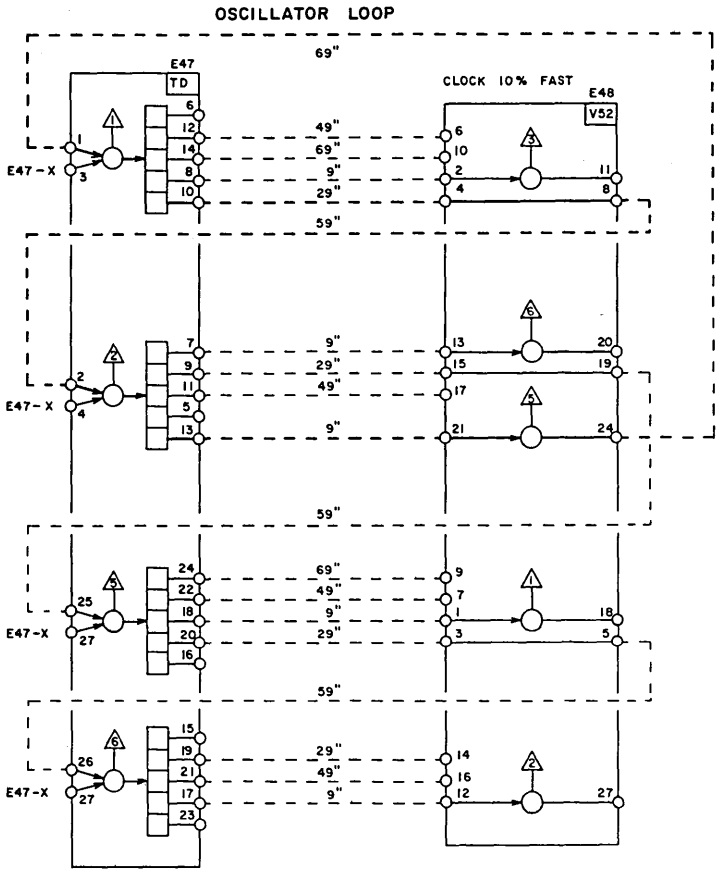
The master clock pulse rate may be increased or decreased by substitution of a V51 or V52 in place of a V50 module. The V51 module has a longer oscillator loop than the normal V50 module.

The V52 module has a shorter oscillator loop which increases the clock speed by shortening the wires between the TD and V52 module.

The V51 and V52 modules are for maintenance only and can not be used for normal computer operation.







CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CLOCK – SLOW AND FAST	PRODUCT 1704	
		SIZE C	DRAWING NO. 60152700
		SHEET 6	PAGE 5

TIMING CHAIN AND CONTROL

The timing chain for the 1700 Computer consists of two V69 modules. Each module contains four FFs connected together, forming a chain of eight FFs (H00-H07). Each FF is gated by a clock pulse. As a "1" passes down the chain, each FF is set for 75 nsec. The FFs alternately set at t00 and t50 and clear at t25 and t75, thus overlapping each other by 25 nsec. Normally, the total cycle time for one pass of the timing chain is 400 nsec. The exception is explained below under Short Cycle 1.

The timing chain enables the V000-V350 25-nsec pulses. The V pulses occur at t00 and t50, simultaneous to the setting of the timing chain FFs.

T pulses, V pulses, and H--FFs control computer timing, with the exception of storage control. Storage control uses a separate timing chain consisting of K--FFs.

Shown on the top of page 7 are a number of fan-outs for the timing chain. The fan-outs are shown as partial modules, because they are included on modules of unrelated logic.

SHORT CYCLE 1

During Multiply and Shift instructions, time 250 occurs 100 nsec early. This sequence occurs only during the C cycle when the Short Cycle 1 (SC1) signal is present. FF H02 sets at time 100, but an SC1 signal blocks the setting of H03 at time 150. Instead, the H02 enable leaves module V69 through pin 5 and enters the second V69 module at pin 25. The SC1 signal at pin 23 enables the setting of H05 at time 250. FFs H03 and H04 are not set during the SC1 condition.

START TIMING CHAIN

Initially, the timing chain starts by enabling the RUN/STEP or TEST MODE switches. The Run/Step or Test Mode switch sets the Go 1 FF on module V49, p. 19. The Go 2 FF (module V55) sets and starts the timing chain if the Go 1 signal is present and the Display FF set. The Go 2 FF sets at time 25 and the timing chain starts 75 nsec later at time 00.

RESTART TIMING CHAIN

There are three main gates for restarting the timing chain without using the manual switches. These are the conditions for restarting the computer during program control.

1) Stop 2 FF clear and Storage Resume signal present
2) H07 $(\overline{MC})\left[\overline{B\ cycle} + (IM.OP.)\ (ROP)\right]$

   or
3) H05 and SC 2

   or
4) Go 2 FF set

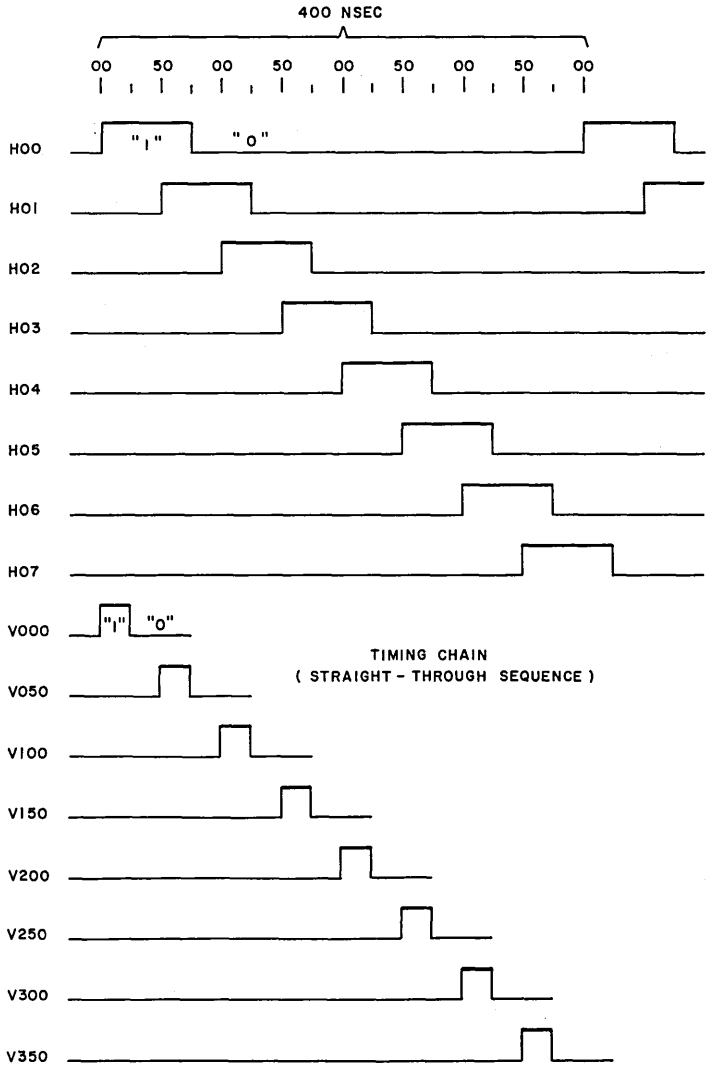
The first condition restarts the timing chain after a storage reference. The second condition restarts the timing chain at the end of the B cycle if no storage reference is initiated or at the end of the A and C cycles. The third condition occurs during the C cycle of a Shift instruction. The SC 2 signal blocks H06 and H07 and restarts the timing chain early.

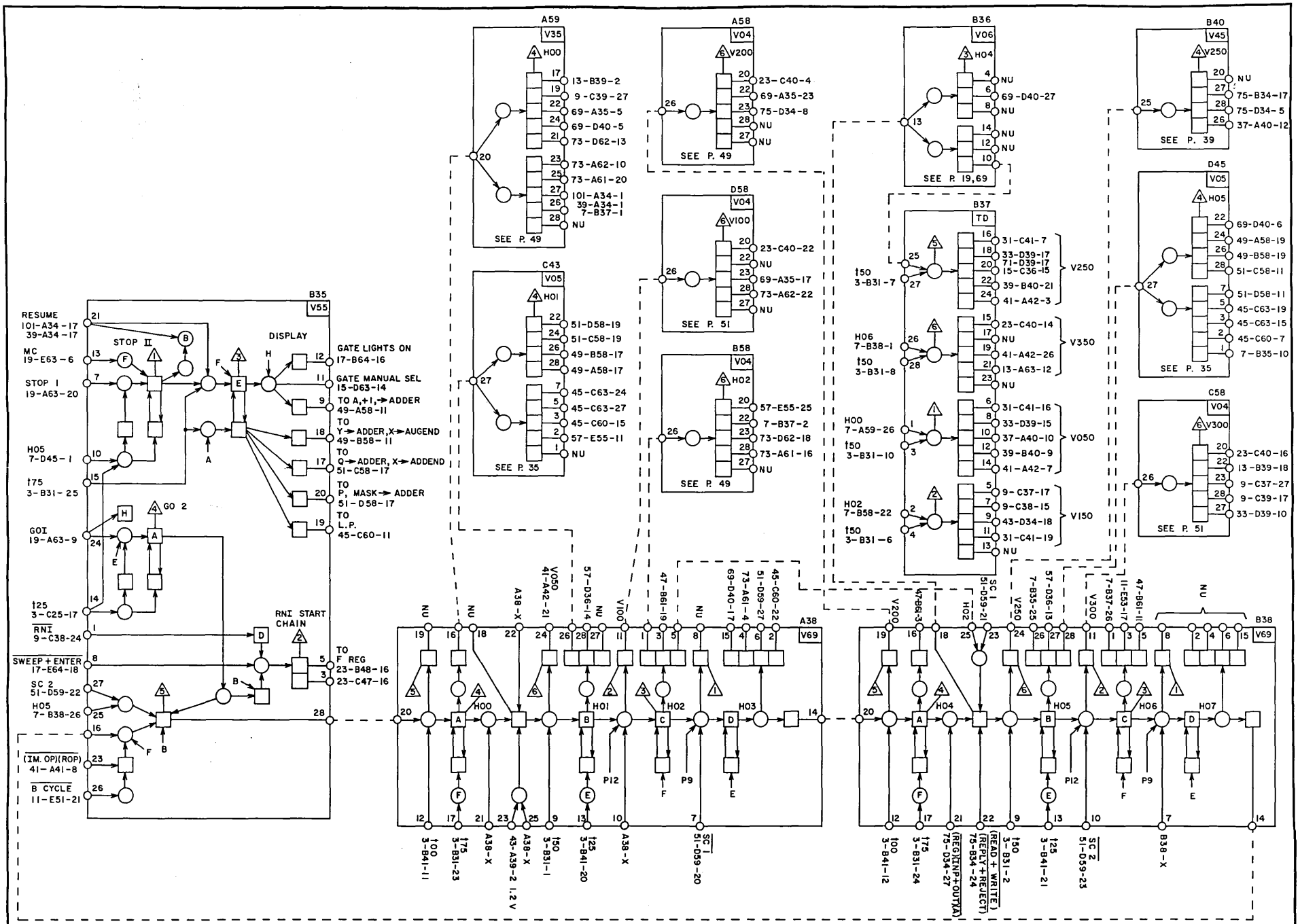
SET F REGISTER

Output pins 3 and 5 of module V55 enable the setting of the F register under the following conditions:

1) $\overline{Sweep + Enter}$ (RNI) (Go 2)
2) $\overline{Sweep + Enter}$ (RNI) (Resume) $(\overline{Stop\ 2})$

The Run/Step or Test Mode switches enable the first condition and the storage resume enables the second condition.


400 NSEC
00
50
00
50
00
50
00
50
00
H00
"1"
"0"
H01
H02
H03
H04
H05
H06
H07
V000
"1"
"0"
TIMING CHAIN
(STRAIGHT - THROUGH SEQUENCE)
V050
V100
V150
V200
V250
V300
V350



CONTROL DATA CORPORATION	TITLE: TIMING CHAIN	PRODUCT 1704	
COMPUTER DIVISION		SIZE C · DRAWING NO. 60152700 · REV AP	
		SHEET · PAGE 7	

There are five modes of operation in the 1700 which enable a general series of commands for groups of instructions.

1) RNI = Read Next Instruction
2) ADR = Addressing
3) REG = Register Transfer
4) ROP = Read Operand from Storage
5) STO = Store Operand in Storage

RNI

The command timing for all instructions starts in the RNI mode. During RNI, the instruction code transfers from the Z register to the X register and from the X register to the F register. While in the F register, the instruction code is translated to determine whether it is addressable. If it is addressable, the ADR mode is initiated. If it is not addressable, the REG mode is initiated. A block diagram on the lower portion of the diagram shows the possible sequence paths.

The RNI Control FF is located on module V71 and has five main setting gates. If any one of the gates is satisfied, the RNI mode is enabled.

1) Master Clear - before starting a program.
2) (B150) (STO) - after storing an operand
3) (B150) (ROP 2) $\left[\overline{\text{RAO}}\ (\text{ROP})\right]$ - after reading an operand (except Replace Add One instruction)
4) (B150) (ADR) $\left[(\text{JMP})\ (\text{End ADR})\right]$ - after addressing (Jump instruction only)
5) (B150) $\left[(\text{REG})\ \overline{(\text{SPB} + \text{CPB} + \text{EXI} + \text{INT})}\right]$ - after REG mode (except Set/Clear Program Protect, Exit Interrupt, and interrupt during REG)

The RNI Control FF clears at time 150 of the B cycle (B150) if none of the setting gates are satisfied.

ADR

Instructions which are read from or written into storage use the ADR mode. The only exceptions are Set/Clear Program Protect, Exit Interrupt, and Interrupt During REG mode in which the address is already determined. During the ADR mode, storage is always requested.

The ADR Control FF is located on module V70 and has one main setting gate which enables the ADR mode.

(RNI) (A050) (F ≠ 0) $\left[\overline{(\text{Protect Fault})}\ \overline{(\text{Sweep} + \text{Enter})}\right]$ - after reading next instruction, if F ≠ 0, not addressing a protected instruction from an unprotected instruction and Sweep or Enter switch not enabled.

Storage is referenced when the Sweep switch is on but not during an ADR mode.

The ADR Control FF clears at time V300, providing the RNI, ROP, or STO Control FF is set. The setting of the two control FFs overlap but the mode remains ADR until the ADR FF clears.

REG

Instructions which do not reference storage for reading or writing operands are considered as being in the Register Transfer mode (REG). During REG, computer control enables control FFs, enables register transfers, updates the address for the next instruction, and requests storage. The exceptions are Set/Clear Program Protect, and Exit Interrupt, where the REG mode is followed by an ROP mode. During the REG mode of these instructions the address is modified and storage requested. The address for the next instruction is updated during the ROP mode. If the computer is in REG mode when an interrupt occurs, the STO FF sets and enables STO mode.

The REG control FF is located on module V70 and has one main setting gate which enables the REG mode.

$$(\text{Protect Fault}) + \left[(\text{RNI})(\text{A050})(\ [\text{Sweep} + \text{Enter}]\ + \text{F} = 0)\right]$$

A Protect Fault signal enables the REG mode and treats the instruction as a nonprotected "Pass" with REG mode updating the address of the next instruction. The Sweep or Enter signal enables the REG mode during RNI, and the next address is updated without using ADR mode. If the upper 4 bits of the instruction equal zero (F = 0) the REG FF sets during the RNI mode.

The REG Control FF clears at time B300 whenever the set input is not satisfied.

ROP

The ROP mode applies to instructions which read operands from storage and the EXI, SPB, and CPB instructions.

The ROP Control FF (ROP 1) is located on module V64 and has two main setting gates. The ROP 2 FF on module V71 provides a delay which prevents the RNI FF from setting at the same time (B150) as ROP or STO. The setting gates for ROP I are as follows:

1) (B150) (ADR) $\left[\overline{(\text{End ADR} + \text{STQ} + \text{RTJ} + \text{STA} + \text{SPA})}\ (\text{End ADR})\ \overline{(\text{JMP} + \text{End ADR})}\right]$ - not a Store instruction, end of addressing, and not a Jump instruction. The End ADR condition is not considered in the setting of the FF.

2) (B150) $(\overline{\text{INT}})$ [REG (SPB + CPB + EXI)] - an interrupt during REG mode enables STO.

The ROP 1 FF clears at time B300 if the RNI or STO 1 FF is set. The normal sequence path is from ROP to RNI, as a Replace Add One instruction is necessary to set STO.

STO

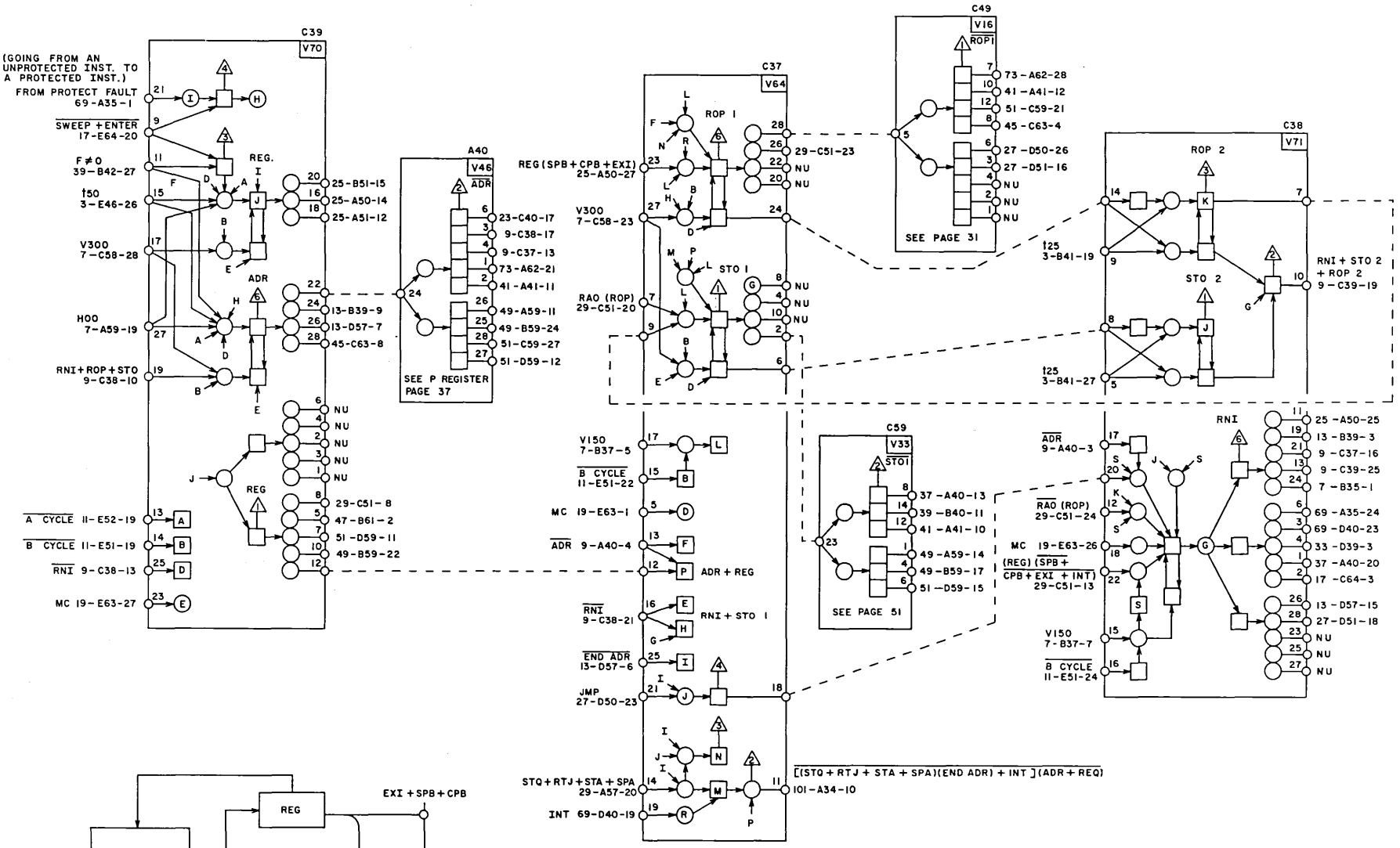
The STO mode applies to instructions which write operands into storage and interrupts occurring during the ADR or REG modes.

The STO Control FF (STO 1) is located on module V64 and has two main setting gates. The STO 2 FF on module V71 provides a delay which prevents the RNI FF from setting at the same time (B150) as ROP or STO. The setting gates for STO 1 are as follows:

1) (B150) (ADR + REG) [(End ADR) (STQ + RTJ + STA + SPA) + INT] - interrupt enables STO 1 from ADR or REG mode, other instructions come from ADR mode only.

2) (B150) (ROP 2 (RAO) - Replace Add One instruction came from ROP mode. It reads from and then writes into storage.

The STO 1 FF clears at time B300 if the RNI FF is set. The computer always initiates an RNI mode after writing into storage.


C39
V70
(GOING FROM AN UNPROTECTED INST. TO A PROTECTED INST.)
FROM PROTECT FAULT 69-A35-1
SWEEP + ENTER 17-E64-20
F≠0 39-B42-27
↑50 3-E46-26
V300 7-C58-28
H00 7-A59-19
RNI + ROP + STO 9-C38-10
REG.
ADR
REG
25-B51-15
25-A50-14
25-A51-12
13-B39-9
13-D57-7
45-C63-8
29-C51-8
47-B61-2
51-D59-11
49-B59-22
A CYCLE 11-E52-19
B CYCLE 11-E51-19
RNI 9-C38-13
MC 19-E63-27
A40
V46
ADR
23-C40-17
9-C38-17
9-C37-13
73-A62-21
41-A41-11
49-A59-11
49-B59-24
51-C59-27
51-D59-12
SEE P REGISTER PAGE 37
C37
V64
ROP 1
STO 1
REG (SPB + CPB + EXI) 25-A50-27
V300 7-C58-23
RAO (ROP) 29-C51-20
29-C51-23
SEE PAGE 31
C49
V16
ROP1
73-A62-28
41-A41-12
51-C59-21
45-C63-4
27-D50-26
27-D51-16
C38
V71
ROP 2
STO 2
↑25 3-B41-19
↑25 3-B41-27
RNI + STO 2 + ROP 2 9-C39-19
V150 7-B37-5
B CYCLE 11-E51-22
MC 19-E63-1
ADR 9-A40-4
RNI 9-C38-21
END ADR 13-D57-6
JMP 27-D50-23
ADR + REG
RNI + STO 1
C59
V33
STO1
37-A40-13
39-B40-11
41-A41-10
49-A59-14
49-B59-17
51-D59-15
SEE PAGE 51
ADR 9-A40-3
RAO (ROP) 29-C51-24
MC 19-E63-26
(REG) (SPB + CPB + EXI + INT) 29-C51-13
V150 7-B37-7
B CYCLE 11-E51-24
RNI
25-A50-25
13-B39-3
9-C37-16
9-C39-25
7-B35-1
69-A35-24
69-D40-23
33-D39-3
37-A40-20
17-C64-3
13-D57-15
27-D51-18
STQ + RTJ + STA + SPA 29-A57-20
INT 69-D40-19
[(STQ + RTJ + STA + SPA)(END ADR) + INT](ADR + REQ)
101-A34-10
START
RNI
REG
ADR
ROP
STO
EXI + SPB + CPB
INT
RAO
JMP
SEQUENCE PATHS
CONTROL DATA CORPORATION
COMPUTER DIVISION
TITLE
SEQUENCE CONTROLS
PRODUCT 1704
SIZE C
DRAWING NO. 60152700
REV E
SHEET
PAGE 9

CYCLE CONTROL

One pass down the timing chain is considered a cycle. The 1700 Computer has three unique cycles.

1) A cycle (storage resume)
2) B cycle (storage request)
3) C cycle (iterative)

The normal cycle sequence is resume, request, resume, request, etc. or A → B → A → B, etc.

The Multiply, Divide, and Shift instructions use a C cycle in addition to the A and B cycles. The C cycle is iterative because the computer stays in the C cycle until shifting for that particular instruction is complete. The C cycle occurs between the resume and the next request.

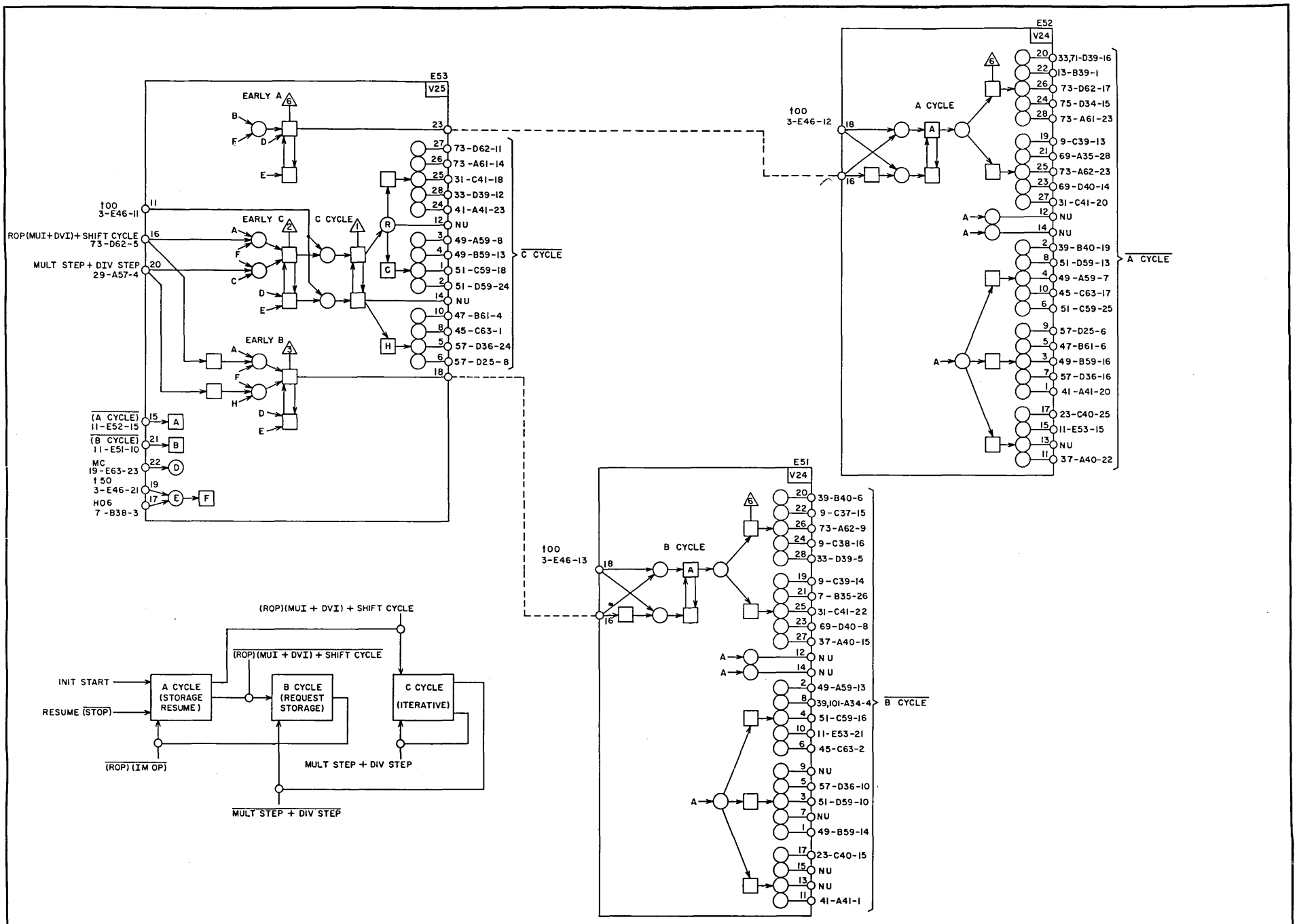
A → C → B

A and B cycles are always 400 nsec long. C cycles are either 200, 300 (short cycle) or 400 nsec long. Shift C cycles are 200 nsec long and multiply C cycles are 300 nsec long until the last C cycle (Y00-04 = 0), which is 400 nsec long. All C cycles for divide are 400 nsec long.

Cycle control, sequence control, and timing chain times are combined to enable specific conditions in command timing. For example, an instruction may have two or more B cycles and time 100s. The sequence mode combined with B100 enables a unique condition such as ADR (B100), ROP (B100), or RNI (B100).

The three modules below contain two Control FFs and the fan-out for each cycle. The Early Cycle FFs set at time 350 and clear at the following 350 time. The Normal Cycle FFs set at time 00 and clear at the following time 00 providing the corresponding Early Cycle FF is set.

A Master Clear pulse starts the computer in the A cycle. At time A350 the Early B or Early C Cycle FF sets, depending upon the condition (ROP) (MUI + DVI) + Shift Cycle. At the same time the Early A FF clears. The A Cycle FF clears and the B or C Cycle FF sets 50 nsec later. B cycles are followed by A cycles either upon a storage resume or $\overline{(ROP)\ (IM.OP)}$ condition. C cycles are followed by B cycles or another C cycle. The Multiply Step +Divide Step condition reinitiates the C cycle. The C Cycle FF does not need a reinitiation pulse for Shift instructions. During the shift cycle the Early C Cycle FF does not clear because the H06 pulse is not available. Short Cycle 2 (SC 2 blocks the setting of H06 and H07 during a shift cycle (see Timing Chain, page 7). The (H05) (SC 2 pulse (page 7 module V55) restarts the timing chain after each shift, and the computer remains in the C cycle. On the last iteration of shift, the $\overline{SC\ 2}$ pulse enables H06, and the Early C Cycle FF clears.



CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE: CYCLE CONTROLS

PRODUCT: 1704
SIZE: C
DRAWING NO.: 60152700
REV: AP
SHEET: 9
PAGE: 11

ADDRESSING CONTROLS

The outputs of the four modules below are addressing conditions used in command timing. These addressing translations enable commands used in assembling the effective address. Module V63 contains three addressing control FFs.

READ INDEX

The setting of the Read Index FF indicates that the present storage reference is for the Index register (address 00FF). The Read Index FF sets at time A300 when the following condition is present:

$$\overline{ind}\ (i)\ (\overline{RNI} + \Delta \neq 0)\ (\overline{INT})$$

This condition does not mean that the Indirect and Relative signals are unused in forming the effective address. It means that these conditions are not available when indexing. Indexing is the last operation in forming the effective address.

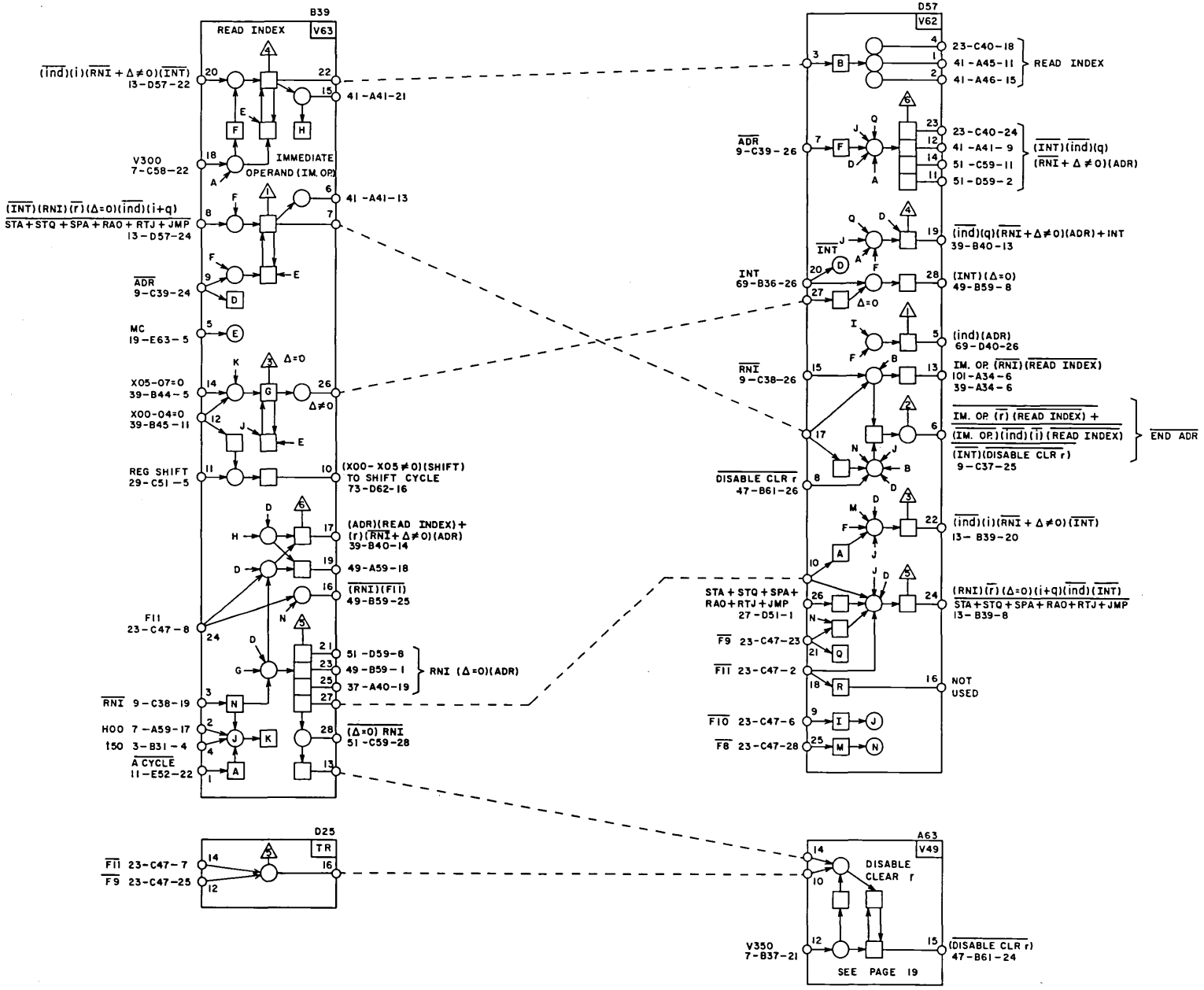
The output of the Read Index FF is used in forming other addressing conditions. When the set condition is disabled, the Read Index FF clears at time A300.

IMMEDIATE OPERAND (IM. OP.)

The IM. OP. FF sets at time A300 when the indicated condition is present. The IM. OP. signal means that the effective address is the operand for Read Operand instructions. The three addressing modes which use IM. OP. are marked by an 6 at the bottom of the chart on page 115. The IM. OP. FF clears at the first A300 time after addressing is complete.

$\Delta = 0$

The $\Delta = 0$ FF sets at time A050 of the RNI mode when $\Delta = 0$. This FF enables the P + 1 portion of the effective address and is combined with other translations to form addressing conditions. This FF stays set until the next A050 time of RNI.



CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE: ADDRESSING CONTROLS	PRODUCT 1704 SIZE C · DRAWING NO. 60152700 · REV F SHEET 10 · PAGE 13	

MANUAL CONTROLS (REGISTER SELECTION AND CLEAR CONTROLS)

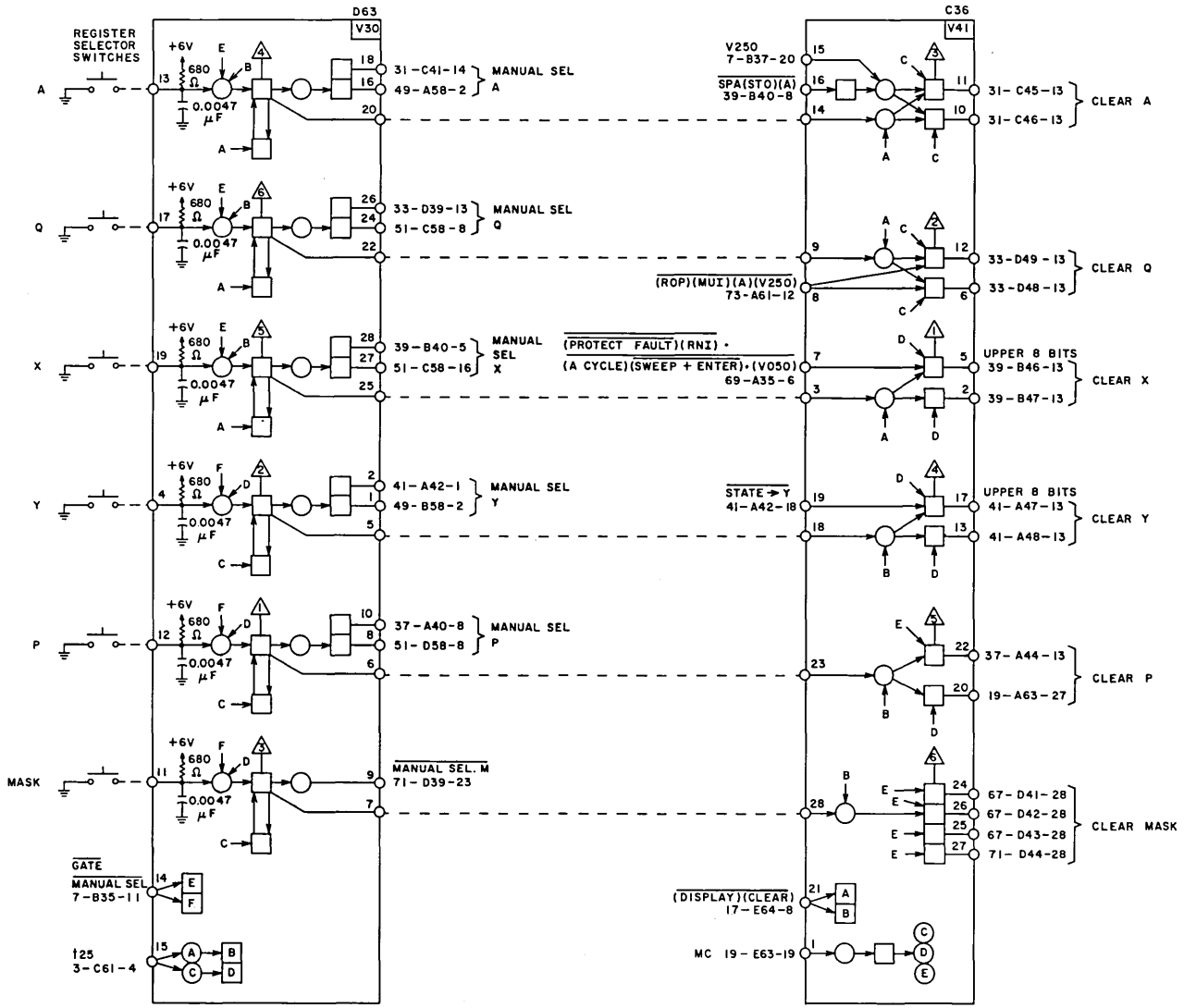
A six-position Register Selector switch and associated logic selects one of the X, A, Q, P, y, and Mask registers for manual display and entry.

The condition (Register Selector switch set) (Display) (T25) sets a FF in the V30 module that corresponds to the Register Selector switch position. (Since only one position of the Register Selector switch can be engaged at one time, two or more registers are not available simultaneously.)

The output from the set FF goes to the V41 module enabling an inverter if the condition (Display) (Clear) exists. Then the selected register is cleared. The following table shows the other conditions which cause a register to clear.

CONDITION	CLEARS
SPA (STO)(A cycle)(V250)	entire A register
ROP (A cycle)(V250)(MUI)	entire Q register
$\overline{\text{(Protect Fault)}}$(RNI)(A cycle)$\overline{\text{(Sweep+ ENTER)}}$(V050)	upper 8 bits of X register
Interrupt STATE → Y	upper 8 bits of Y register

If the Master Clear switch is set, all six registers clear simultaneously.



NOTES:

1. CAPACITOR VALUES ON V30 MODULE MAY BE 0.1 μF ON SOME MACHINES. SEE CHANGE ORDER NO. 14392.

CONTROL DATA CORPORATION	TITLE: MANUAL CONTROLS (REGISTER SELECTION AND CLEAR CONTROLS)	PRODUCT 1704	
COMPUTER DIVISION		SIZE C · DRAWING NO. 60152700	REV -
		SHEET · PAGE 15	

MANUAL CONTROLS (SWITCH AND INDICATOR DRIVERS)

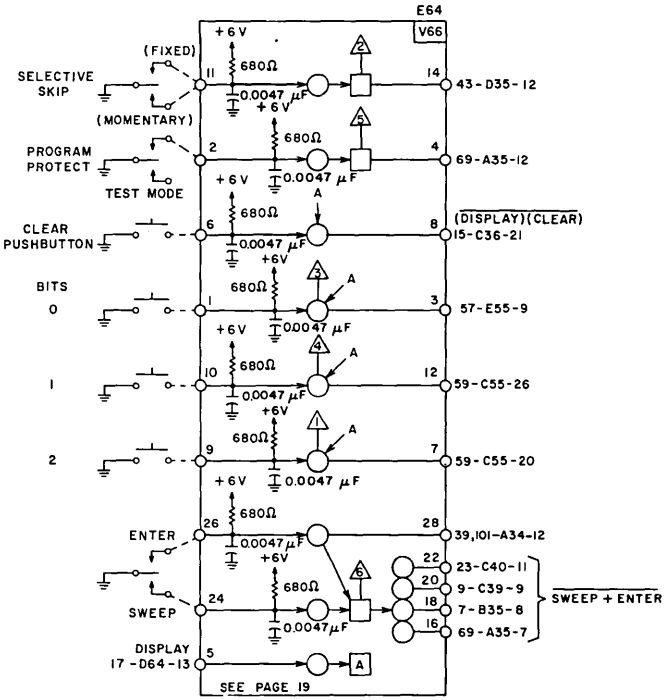
The Selective Skip, Program Protect, and Enter/Sweep switches connect to the V66 module. The Selective Skip switch is a 3-position lever switch that is OFF in the center position; ON in the up and down position. The up position is fixed and the down position is momentary. The Selective Skip switch in the ON position conditions the Selective Skip instruction shown on page 43. Placing the Program Protect switch in the up position, conditions the Program Protect logic shown on page 69.

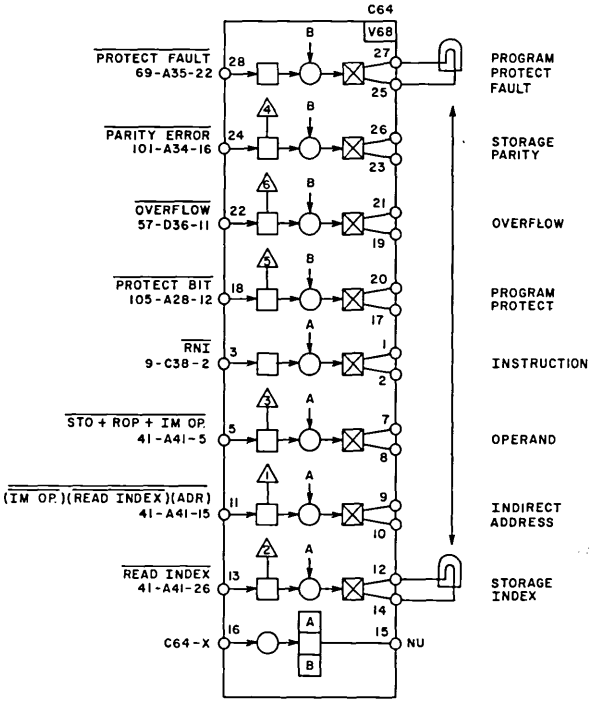
The Enter/Sweep switch is a 3-position lever switch which is fixed in all positions with the center position OFF. In the ENTER position, each step operation of the Run/Stop switch stores the contents of the X register at the location specified by the P register and advances the P register by one. In the SWEEP position, each step operation of the Run/Stop switch transfers the contents of the storage location whose address is in the P register into the X register and advances the P register by one.

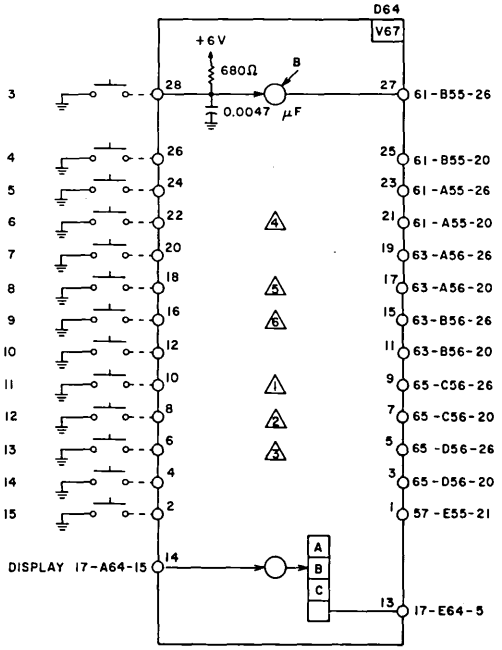
The 16 pushbuttons connected to the V66 and V67 modules control manual entry into a selected register. A set pushbutton ANDed with the Display condition sends a "0" to the Adder/Shifter. This puts a "1" into the corresponding bit position of the selected register. The indicators on the two V68 modules (locations A64 and B64) display the contents of the selected register (Display condition present). An enabled indicator represents "1" in that location.

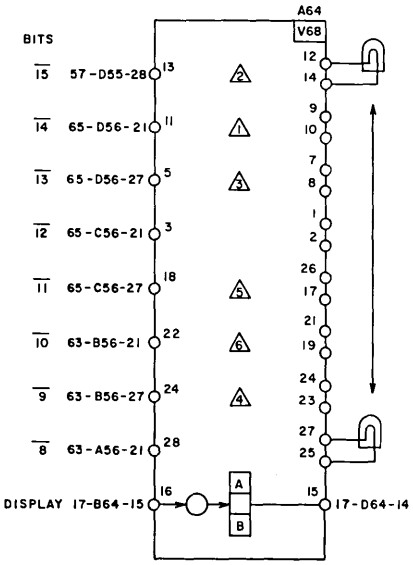
When set, the Clear pushbutton attached to the V66 module clears the contents of the selected register. When a bit is manually set, it remains in that state until the Clear pushbutton is enabled.

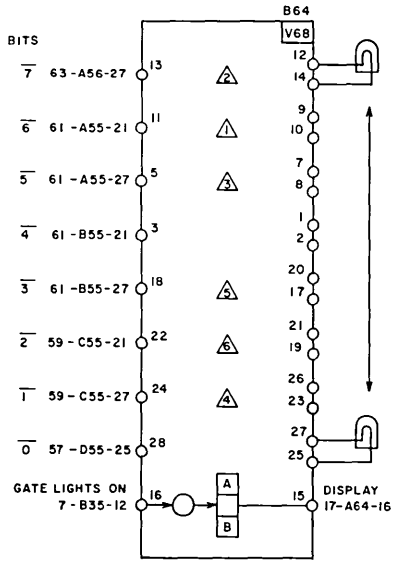
A V68 module (location C64) controls the eight indicators (excluding TEMP) located on the left side of the 1700 console. Note that a "0" input enables the corresponding indicator.











NOTES:

1. CAPACITOR VALUES ON V66 AND V67 MODULES MAY BE 0.1 μF ON SOME MACHINES. SEE CHANGE ORDER NO. 14392.

CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE: MANUAL CONTROLS (SWITCH & INDICATOR DRIVERS)

PRODUCT 1704
SIZE C | DRAWING NO. 60152700 | REV
SHEET 12 | PAGE 17

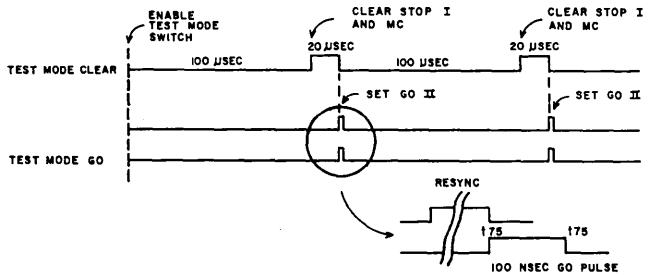
The Test Mode switch connects to module V85. Modules V85 and V88 contain the Test Mode logic. The computer executes the following sequence of events when the Test Mode switch is placed in the down position:

1) 20 usec Master Clear. This clears the P register and all other operational registers.

2) 100 usec program run starting from P = 0000.

3) Return to step 1 and repeat.

The accompanying timing chart shows the setting and clearing of the three Test Mode FFs. The Test Mode Go FF enables a 100 usec Go pulse to the Go1 FF on module V49. The Go1 FF sets the Go2 FF 75 nsec later. The Go2 pulse starts the timing chain which runs for 100 usec or until a Program Stop is enabled. At the end of 100 usec the Test Mode Clear FF enables the Master Clear and the timing chain stops.



MASTER CLEAR (MC)

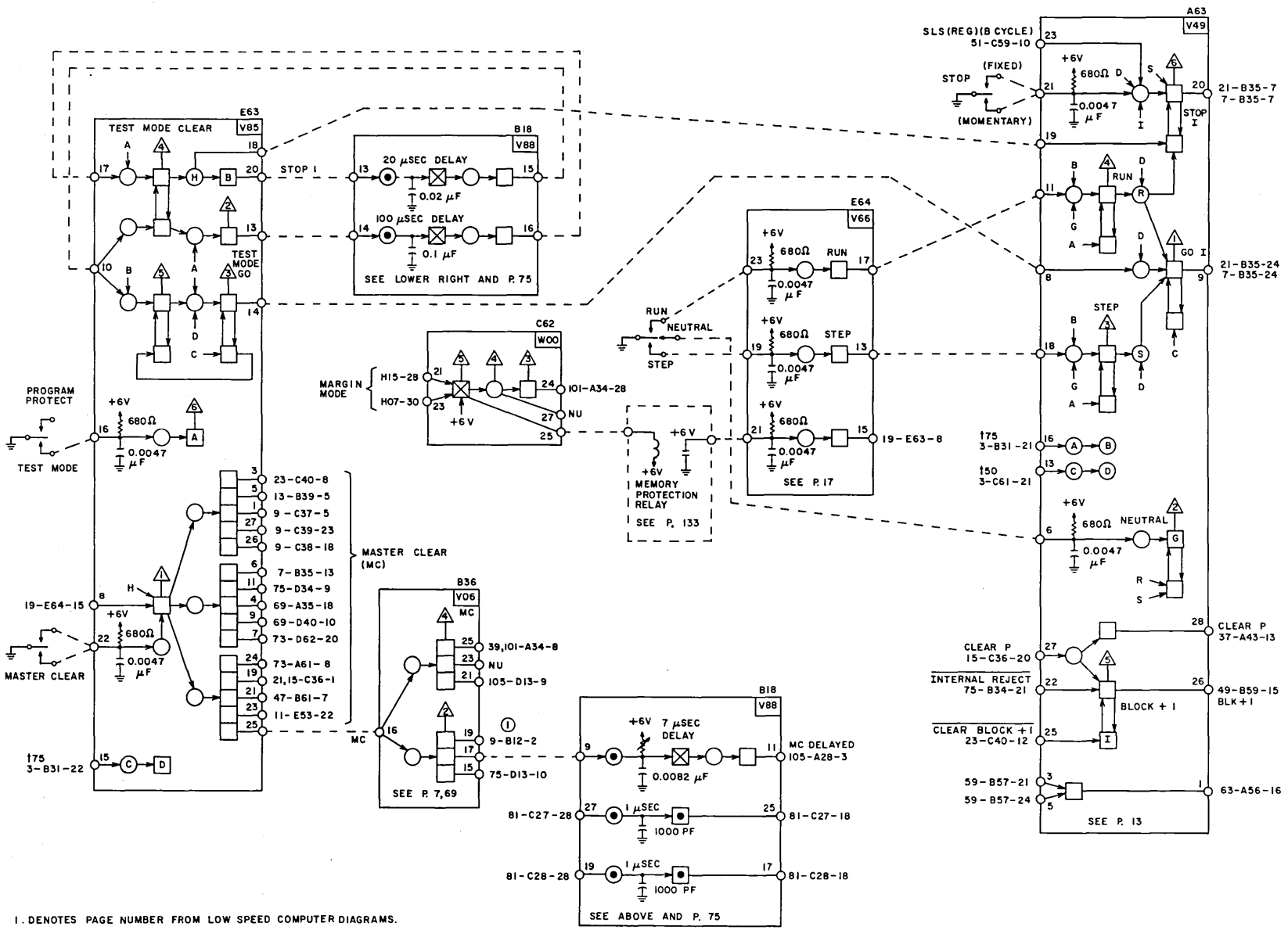
The Master Clear switch connects to module V85. A Master Clear is executed when the switch is momentarily placed in the up or down position. The Master Clear disables the timing chain, clears all registers, and clears most Control FFs. Modules V85 and V06 contain Master Clear fan-outs.

Module V88 contains a delayed Master Clear for storage control. This allows the completion of the present storage reference and prevents unnecessary fault conditions from occurring.

LOGIC VOLTAGE SENSOR

Module W00 is used to determine power failures by sensing the +6-volt logic bus. When the voltage drops below a preset value, the special circuit de-energizes relay K4 and protects memory. Another output of module W00 is used to generate interrupt 00 on power failure. Approximately 8 milliseconds of program execution time is available between relay coil de-energization and contact closure.

The logic voltage sensor can be disabled for voltage margin checking by turning the MARGIN MODE switch on (this switch is located on the memory power supply).



1. DENOTES PAGE NUMBER FROM LOW SPEED COMPUTER DIAGRAMS.
2. CAPACITOR VALUES ON V49, V66 AND V85 MODULES MAY BE 0.1 μF ON SOME MACHINES. SEE CHANGE ORDER NO. 14392.

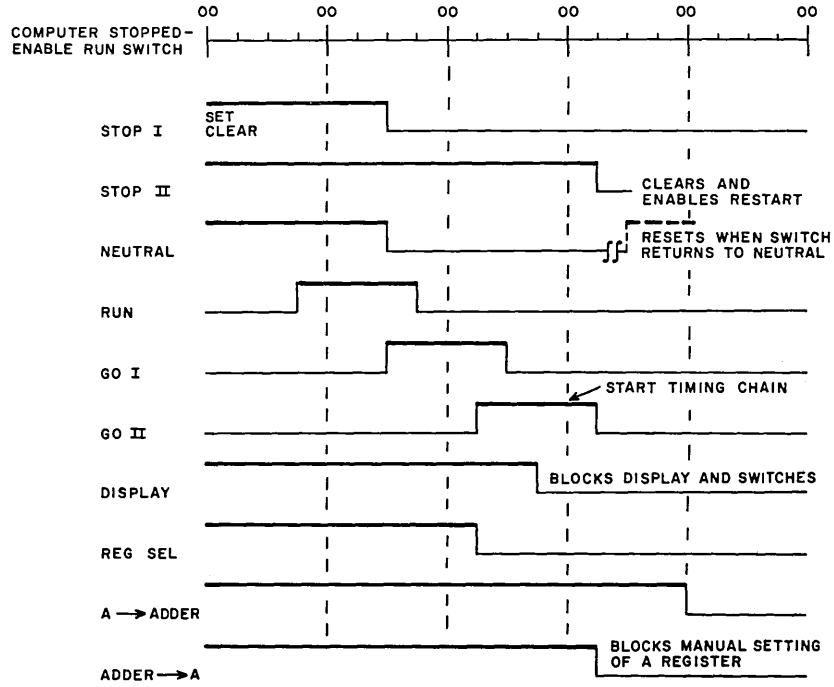
CONTROL DATA CORPORATION	TITLE: MANUAL CONTROLS (TEST MODE AND RUN/STEP)	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C	DRAWING NO.: 60152700 REV: A
			SHEET: PAGE: 19

TYPICAL REGISTER DISPLAY

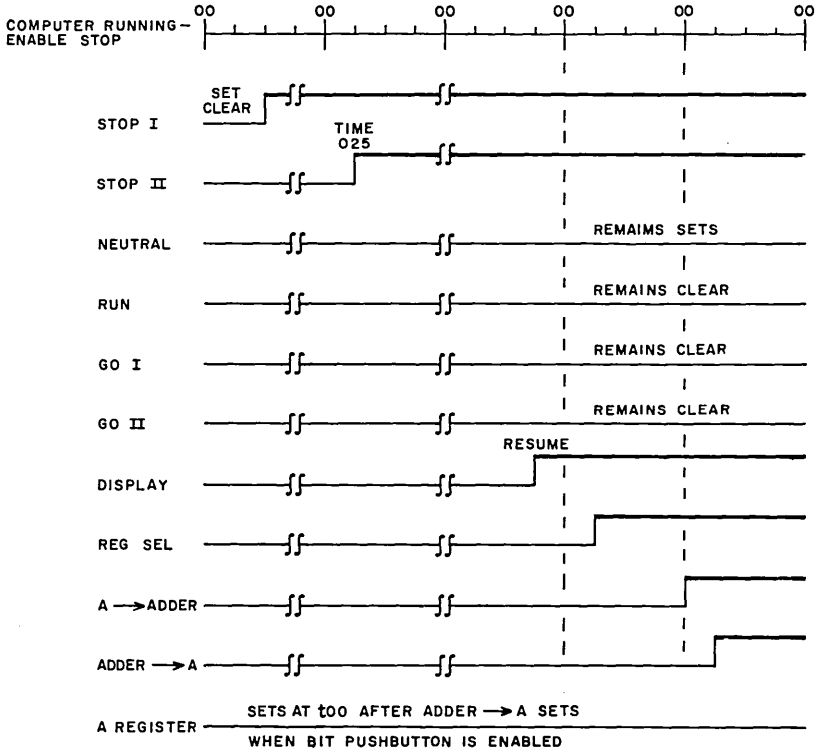
The diagram below shows a typical register display sequence using the A register. For a starting reference, assume the following conditions:

1) Power on
2) A register selector button pressed
3) Timing chain stopped
4) Display FF set (enabling pushbuttons and display)

When the Run/Step switch is momentarily placed in the up position (RUN), the timing chain starts and the switches and display are disabled. The following timing chart shows the setting and clearing of Control FFs for starting the computer.



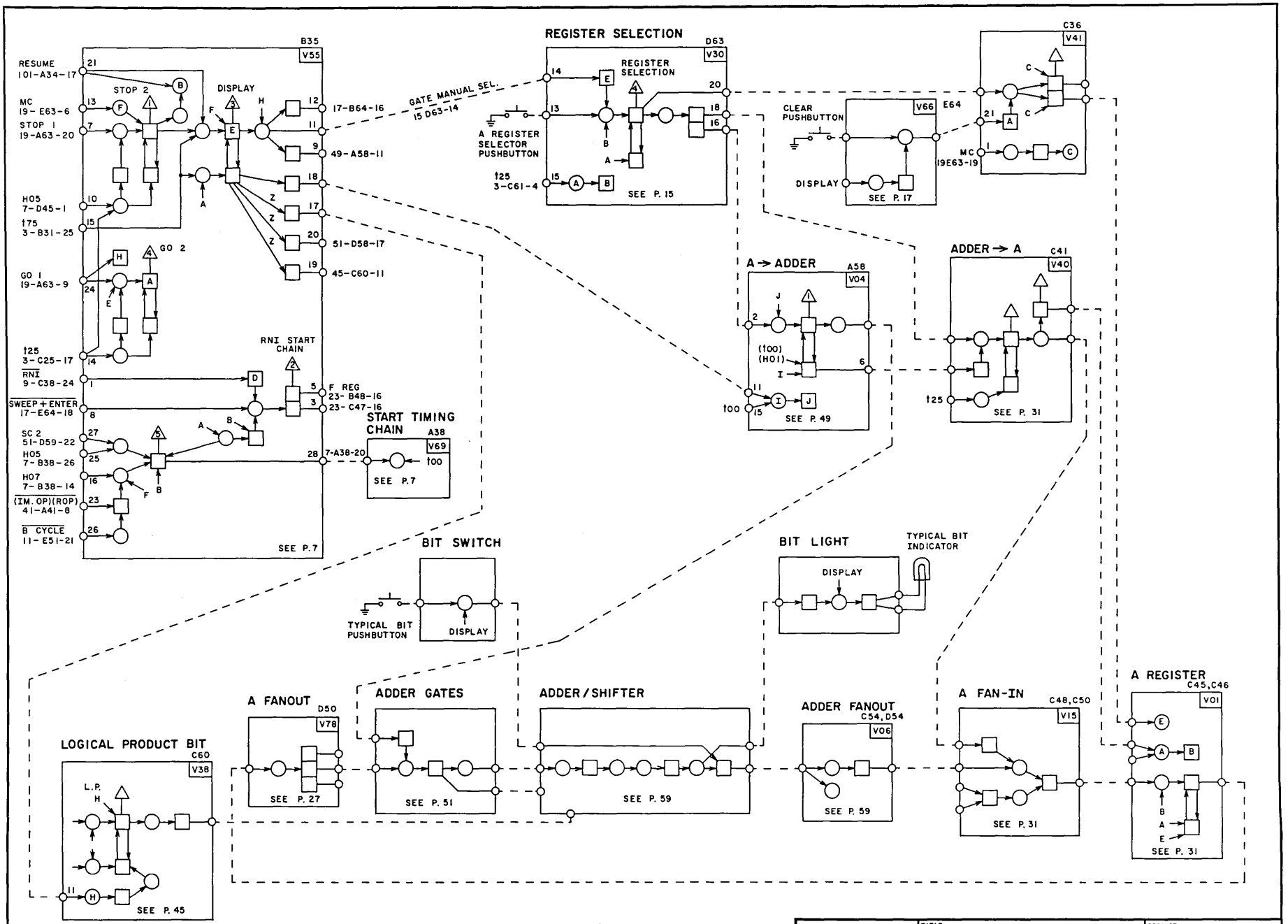
The timing chain is disabled and the display enabled when the Stop FFs set. The timing chain can not be restarted until the Run/Step switch is activated. The individual bits of the A registers are manually set by the bit pushbuttons while the Display FF is set. Pressing a bit pushbutton enables the Adder/Shifter to set the corresponding bit in the A register and light the corresponding bit indicator. The raw clock pulses enable the setting of the A register, although the timing chain is stopped. The following timing chart shows the setting of Control FFs for stopping the computer.



Pressing the Clear pushbutton clears the A register if the Display FF is set. Other registers may be selected while the Display FF is set by pressing the corresponding register selector switch. For example, if the X register is selected, the Adder/Shifter samples the X register and the corresponding bit indicators light.

The computer is stopped momentarily by placing the Run/Step switch in the down position. If the switch is repeatedly placed in the down position, the computer steps through the program, stopping after each storage reference. The significance of the storage reference just made is indicated by the instruction sequence indicators.

This diagram shows a typical register display sequence (A register). The register selector switch must be set for the A register. With the Run-Step switch (page 19) in the center position, the Neutral FF is set. When the switch is placed in the STEP position, the timing chain stops at the end of the current storage reference and the display is enabled. During the step sequence, the Go 2 FF remains cleared and the Stop 2 FF sets, thus disabling the timing chain at the end of the B cycle. The Display FF sets when Stop 2 is set and a Resume and 75 time are present. Each step pulse sets Go 1, Go 2, and moves the timing chain one storage reference. The chain is stopped by the 125 pulse clearing Go 2 before the next storage reference.



CONTROL DATA CORPORATION	TITLE: MANUAL CONTROLS (TYPICAL REGISTER DISPLAY)	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C	DRAWING NO.: 60152700
		REV: Y	
		SHEET	PAGE: 21

F REGISTER

The 8-stage F register is divided into two 4-stage groups contained on two V57 modules. The low-order four stages (F8-F11) contain the f^1 instruction designator bits. The high-order four stages (F12-F15) contain the f instruction designator bits. The stages of the F register are numbered 8-15 to coincide with the instruction bit positions that they contain. The outputs of the F register translate into the various function codes.

In storage reference instructions, the low-order stages of the F register contain the relative (r), indirect (ind), Q register index (q), and storage index (i) designators as shown on the diagram. In this type of instruction, the designators control the addressing mode of instruction execution.

X → F CONTROL

At t25 time of each RNI sequence, inverter A forces a "0" input to B on the V57 modules. The outputs of A and B transfer the high-order eight bits in X to F. Thus, the f and f^1 designator portions of the instruction are transferred at this time.

F REGISTER CLEAR CONTROL

The diagram shows the conditions under which both the f and f^1 positions are cleared. The enabling of one of these conditions, e.g., Protect Fault, produces "0" outputs from inverters E and F on the V56 module. The resulting "1" outputs from the output inverters on this module clear the F register.

During the ADR mode of storage reference instructions, the r, ind, q, and i designators in the f^1 portion are cleared individually. The following table lists the conditions for clearing each of the designators.

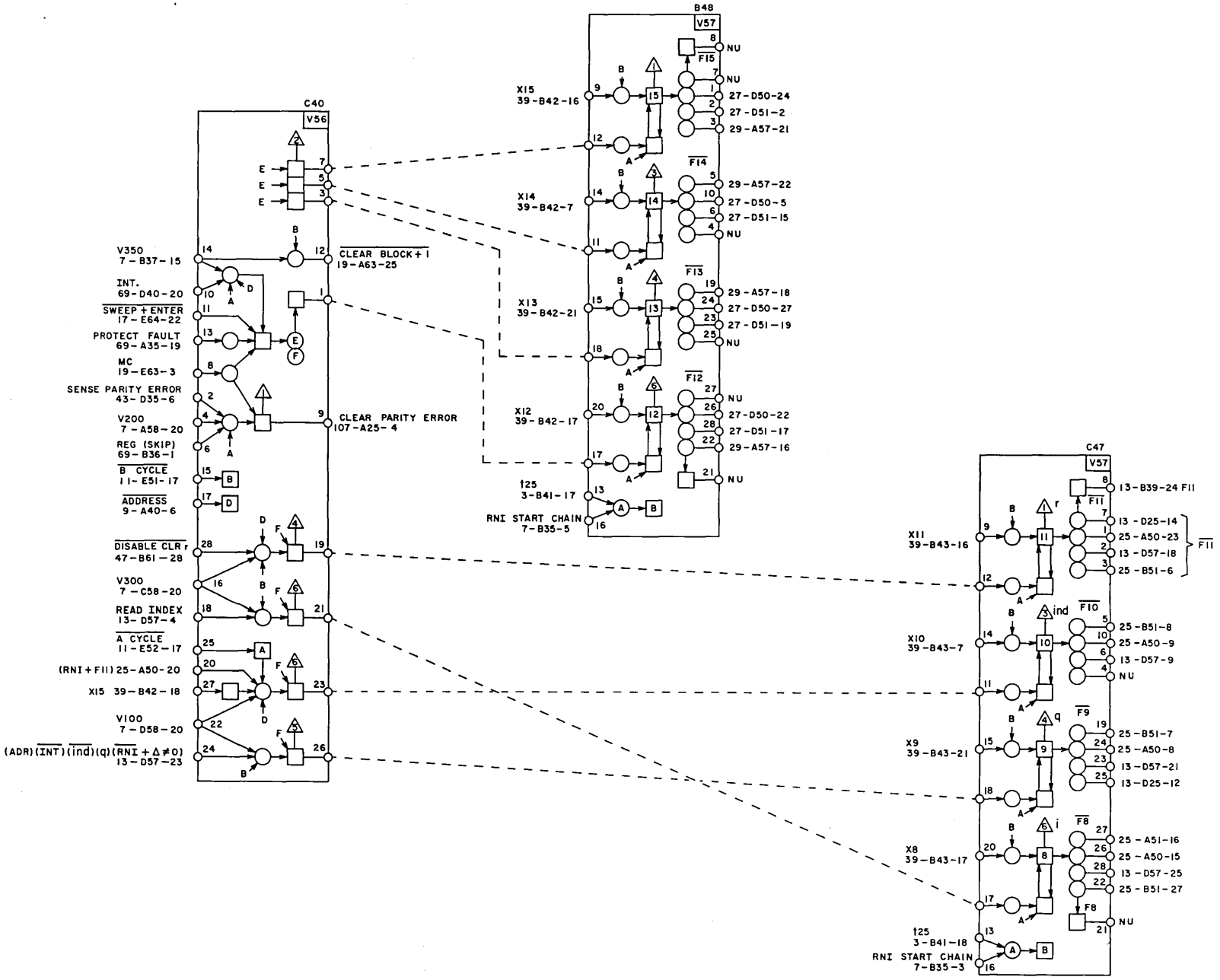
Designator	Conditions	Time
r (F11)	(ADR) (B cycle) (Disable Clr r)	V300
ind (F10)	(ADR) (A cycle) ($\overline{X15}$) ($\overline{RNI}$) ($\overline{F11}$)	V100
q (F9)	(ADR) ($\overline{INT}$) ($\overline{ind}$) (q) ($\overline{RNI} + \Delta \neq 0$) (B cycle)	V100
i (F8)	(Read Index) (B cycle)	V300

Timing pulse V300 clears the r designator during the B cycle of the ADR mode if condition (Disable Clr r) is present. At this time, all relative addressing is complete. If r was not initially set, the operation becomes irrelevant.

The above table shows that the clearing of ind during the A cycle of ADR following the reading of the indirect address ($\overline{RNI}$) ($\overline{F11}$) depends on the state of bit 15 contained in the X register. If this bit is a "1" indicating that the address corresponds to another indirect address, V100 does not clear ind. If this bit is a "0", indirect addressing is complete and ind is cleared.

The V100 pulse clears q during the ADR mode on a $\overline{INT}$ condition. If indirect or relative or both Addressing modes were initially specified, these operations are completed first. The condition for clearing q specifies that q must be initially set.

The V300 pulse clears i during the B cycle on a Read Index operation. The condition for clearing i need not specify the ADR mode since a Read Index can occur only during this mode. The adding of the i index always takes place last if any other addressing mode designators were initially set.

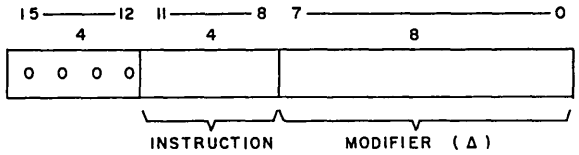


CONTROL DATA CORPORATION	TITLE: F REGISTER	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C · DRAWING NO.: 60152700 · REV: P	
		SHEET: 15 · PAGE: 23	

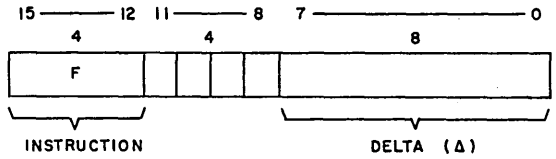
FUNCTION TRANSLATORS

The Function Translators translate the contents of the F register to obtain the current instruction. The 1700 repertoire of instructions may be grouped into Storage Reference instructions (F portion) and Register Reference instructions (F^1 portion). In the table of instructions on page 26, the Storage Reference instructions are in column one (beginning with JMP) and the Register Reference instructions are in column three (beginning with SLS).

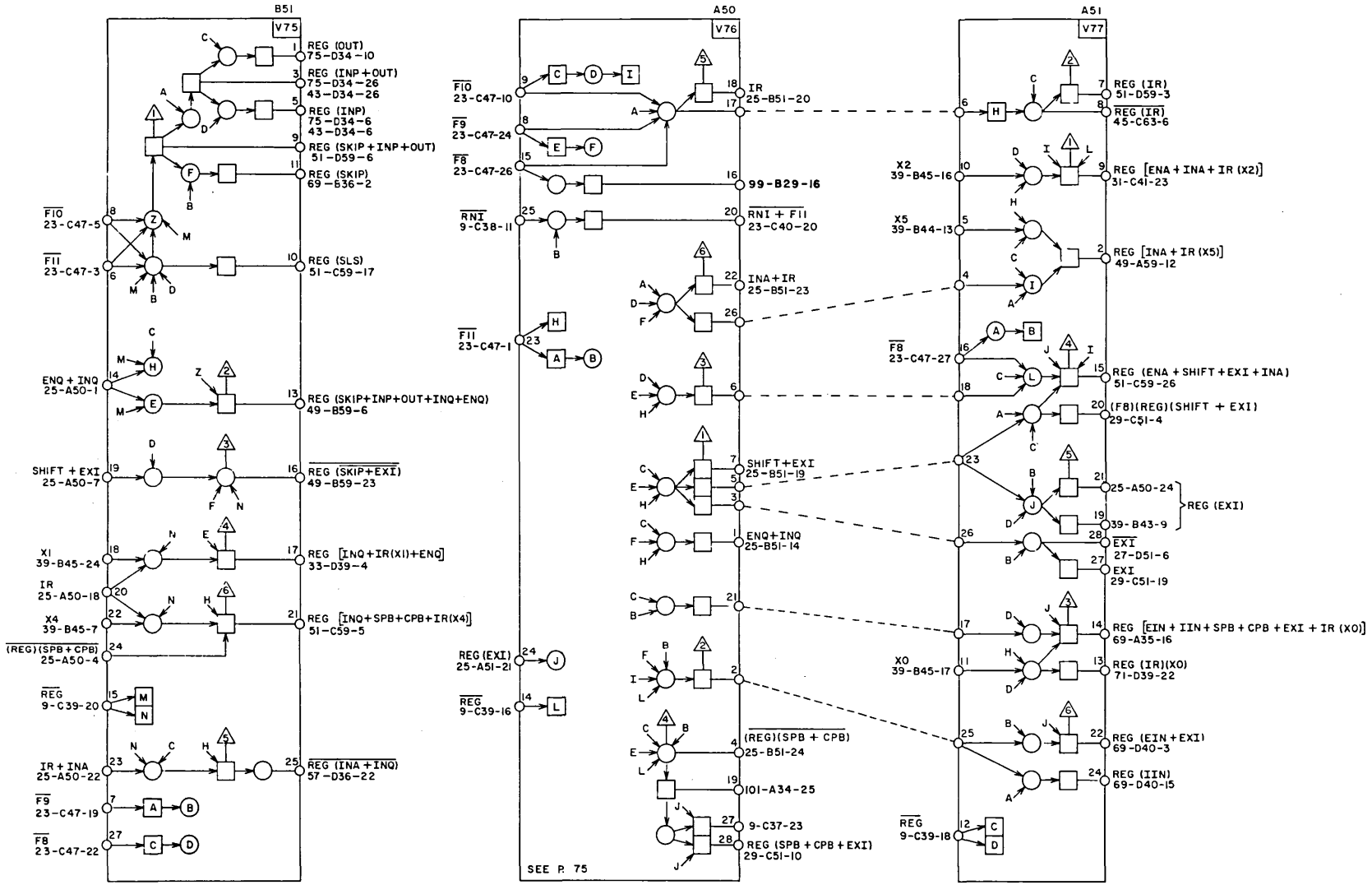
Register Reference instructions are identified when the upper 4 bits (15-12) of the instruction are all "0's". The format of Register Reference is diagrammed below:



Storage Reference instructions have their instruction code in bits 15-12, and bits 11-08 become the address mode. Storage Reference instruction format is diagrammed below:



The static logic of the Function Translator translates the 16-bit input to the selected instruction. The logic searches through the input until it recognizes a unique instruction. The Function Translator dispenses the signals that enable the selected instruction and its associated logic.



CONTROL DATA CORPORATION	TITLE: FUNCTION TRANSLATIONS (F')	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C · DRAWING NO: 60152700 · REV: AP	
		SHEET: 16 · PAGE: 25	

FUNCTION TRANSLATIONS

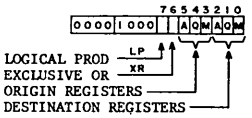
ADDRESSABLE

F			
1	0001	JMP	Jump
2	0010	MUI	Multiply
3	0011	DVI	Divide
4	0100	STQ	Store Q
5	0101	RTJ	Ret. Jump
6	0110	STA	Store A
7	0111	SPA	STA, Parity A
8	1000	ADD	Add to A
9	1001	SUB	Sub. from A
A	1010	AND	AND with A
B	1011	EOR	Exc. OR/A
C	1100	LDA	Load A
D	1101	RAQ	Replace Add 1
E	1110	LDQ	Load Q
F	1111	ADQ	Add to Q

REGISTER REFERENCE

F_1			
0	0000	SLS	Selective Stop
1	0001		SKIPS
2	0010	INP	Input to A
3	0011	OUT	Output from A
4	0100	EIN	Enable Int.
5	0101	IIN	Inhibit Int.
6	0110	SPB	Set Prgm. Pro.
7	0111	CPB	Clr. Prgm. Pro.
8	1000		IRTS
9	1001	INA	Increase A
A	1010	ENA	Enter A
B	1011		NO-OP
C	1100	ENQ	Enter Q
D	1101	INQ	Increase Q
E	1110	EXI	Exit Int.
F	1111		Shifts

INTER-REGISTER



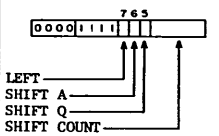
ORIGIN REGISTERS
- If A(B+5)=0; OP1 = FFFF
- If Bits 3+4 = 0; OP2 = FFFF
- If Bits 3+4 = 1; OP2 = (Q)+(M)

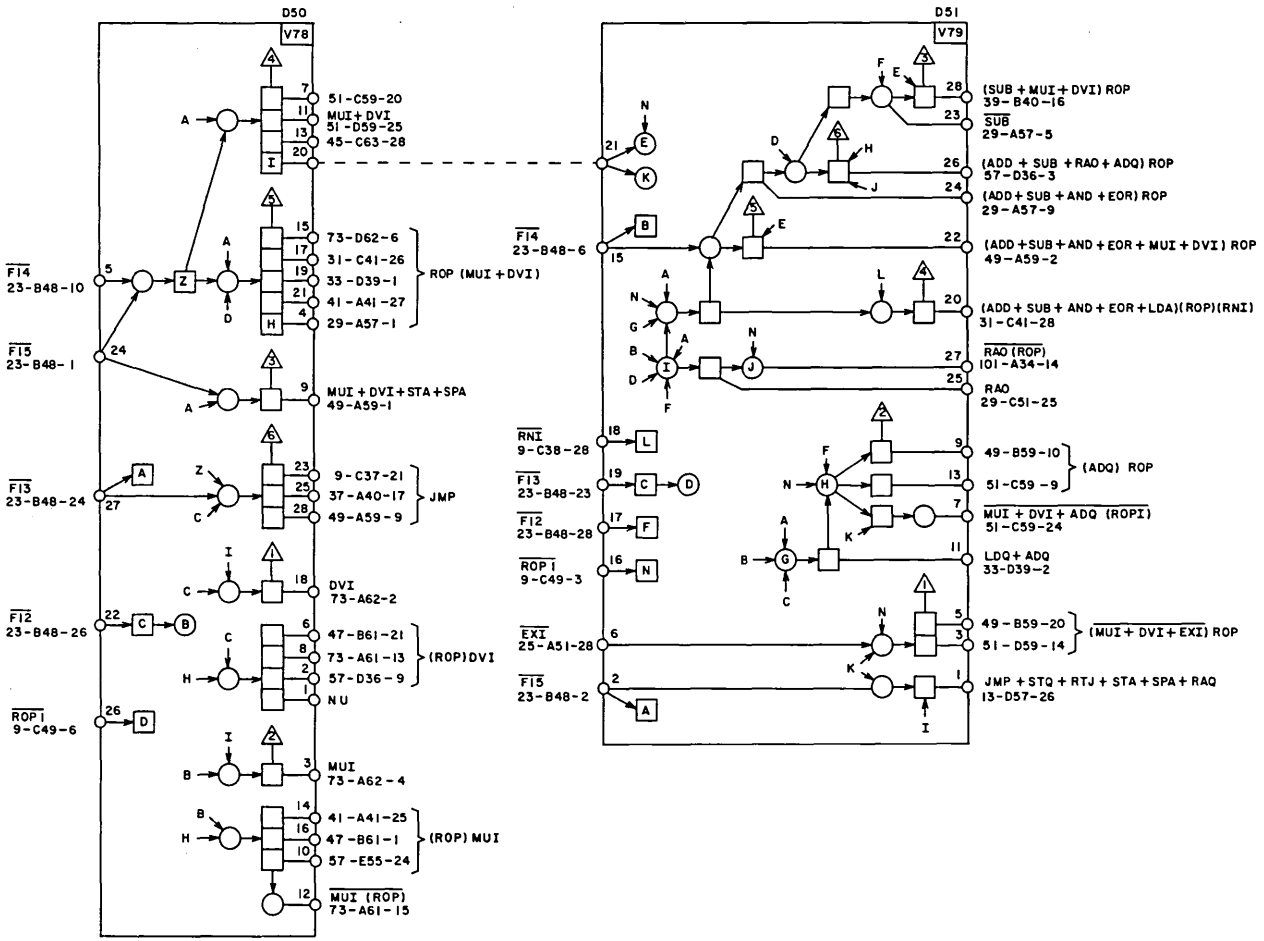
LP+XR
- Both = 0; Sum of OP1 + OP2
- Both = 1; Complement of LP

SKIPS

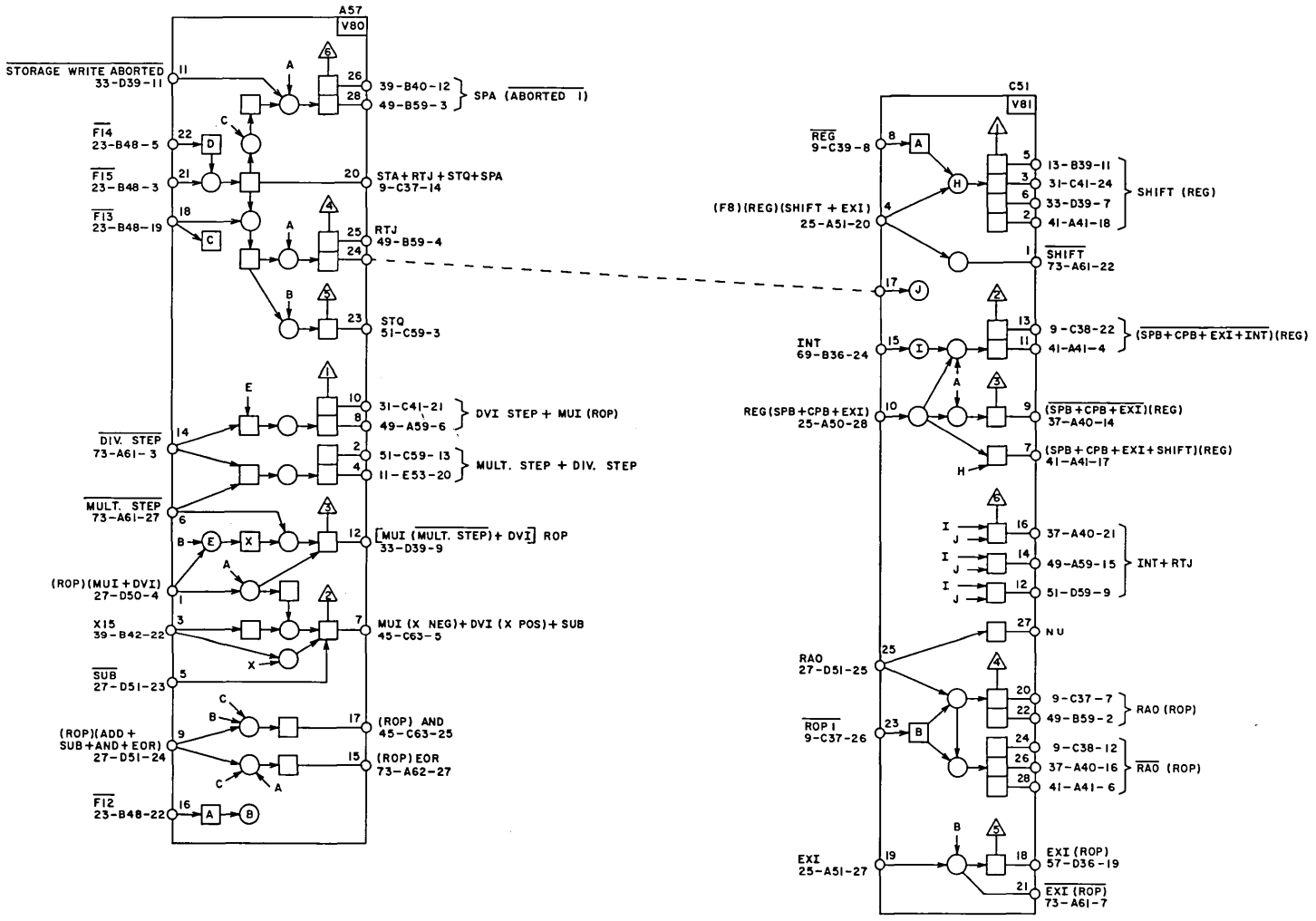
F_2			
0	0000	SAZ	A = +0
1	0001	SAN	A ≠ +0
2	0010	SAP	A = +
3	0011	SAM	A = -
4	0100	SQZ	Q = +0
5	0101	SQN	Q ≠ -0
6	0110	SQP	Q = +
7	0111	SQM	Q = -
8	1000	SWS	Skip SW.
9	1001	SWN	Skip SW.
A	1010	SOV	Overflow
B	1011	SNO	Overflow
C	1100	SPE	Parity Error
D	1101	SNP	Parity Error
E	1110	SPP	Prgm. Pro. Fault
F	1111	SNP	Prgm. Pro. Fault

SHIFTS





CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE: FUNCTION TRANSLATIONS	PRODUCT 1704 SIZE C · DRAWING NO. 60152700 · REV E SHEET 17 · PAGE 27	



CONTROL DATA CORPORATION	TITLE: FUNCTION TRANSLATIONS	PRODUCT 1704	
COMPUTER DIVISION		SIZE C · DRAWING NO. 60152700 · REV P	
		SHEET · PAGE 29	

A REGISTER

The 16-stage A register functions as the Main Arithmetic register. The main functions of the A register are:

1) To contain one operand during many Arithmetic and Logical operations, such as ADD, SUB, AND, etc.
2) To provide a means of loading operands into the arithmetic section (LDA) and of storing the results of Arithmetic or Logical operations in storage (STA, SPA).
3) during multiplication operations, to initially contain the multiplier. At the completion of the multiply, the A register contains the low-order 16 bits of the 32-bit product.
4) during divide operations, to initially contain the low-order 16 bits of the dividend, and at the completion of the divide, to contain the quotient.
5) in input or output operations, to contain the input or output data respectively.

The A reigster is divided into two 8-stage portions contained on two V01 modules. The outputs of the A register transfer to the Adder/Shifter through the A fan-out modules. The A register receives inputs from theAdder/Shifter fan-out, the input receiver modules in the A/Q interface, or the receiver modules in the low-speed interface through the A register fan-in modules. The input selection is controlled by the Adder→A and Input →A FFs on the V40 module.

ADDER →A

The Adder →A FF selects the Adder/Shifter input to the A register. The diagram shows that this FF is set at one of three V-50 timing periods by the enabling of the corresponding conditions. The setting of the Adder →A FF forces a "0" input to inverters A and B on the V15 and to inverter A on the V16 fan-in modules. The "1" outputs of these inverters enable theAdder/Shifter outputs to the corresponding inverters on the V15 and V16 modules. The following t00 pulse gates the outputs of the fan-in modules into the A register. Thus, the Adder →A FF is set on the t50 time preceeding the t00 pulse that loads the A register, allowing 50 nsec for the inputs to stabilize. The t25 pulse always clears the Adder →A FF. The A →Adder pulse also sets the Adder →A FF on a manual selection of the A register.

The A register receives an input from the Adder/Shifter in four main types of instruction operations. Each of the four types is given below with a brief description of the conditions for each type.

Shift

In (A) Shift instructions, the Adder →A FF is set at two unique times. The V050 pulse sets Adder →A in each C cycle with the A →Adder enable through inverter F. The V250 pulse also sets Adder →A in the C cycle under the same conditions. Thus, Adder →A is set twice (A shifted twice) during each C cycle if Y (shift count) is not found to be "0" before each shift.

During short cycle (SC1) operations in Multiply and Shift instructions, the V250 pulse occurs 100 nsec earlier, corresponding to the short cycle of the operand transmission through the adder/shifter.

In (AQ) shifts, Adder →A is set only at V250 time since the A →Adder signal is not present at the V050 time.

Multiply Divide

In Multiply or Divide operations, Adder →A is set during the B and C cycles in the ROP mode. The setting of Adder →A on the B cycle at 250 time transfers the complemented A (A initially negative) or the uncomplimented A (A initially positive) back to the A register. In Multiply operations, the V150 pulse sets Adder →A which transfers the low-order bits of the final product to the A register. In Divide Step operations, the setting of Adder →A at this time transfers the shifted partial dividend back to the A register.

IR + ENA + INA

The Adder →A FF is set on V250 time of the A cycle in the REG mode in the Enter A (ENA) and Increase A (INA) instructions. In either of these instructions, the new quantity is transferred to A at this time. In IR instructions, the setting of X2 selects the A register as the destination register. In this case, the V250 pulse sets the Adder →A FF in the A cycle.

LDA + ADD + AND + EOR + SUB

In these instructions, the V250 pulse sets Adder →A during the B cycle which enables the transfer of the arithmetic or logical result to the A register.

SPA

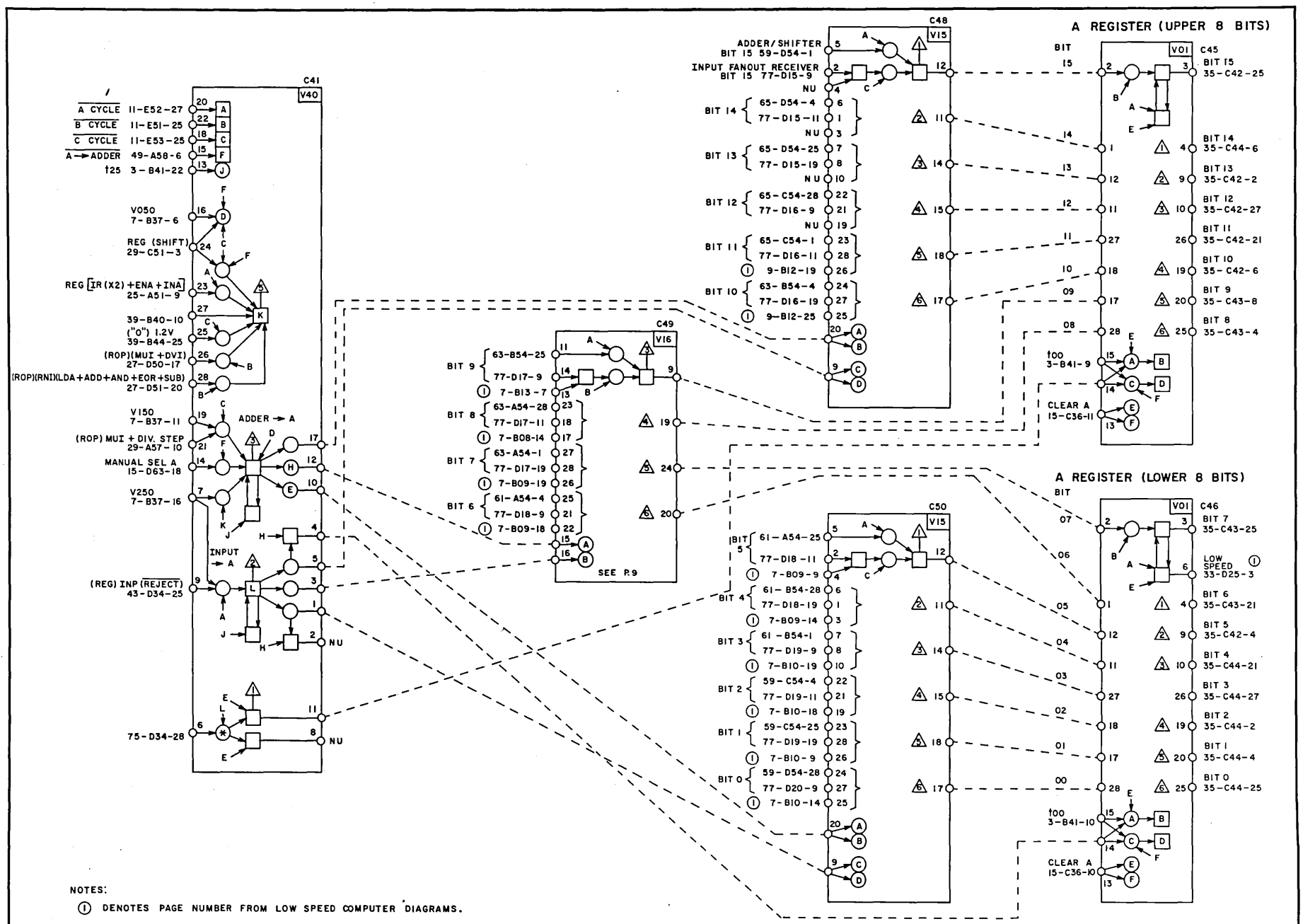
The V250 pulse sets Adder →A in the SPA instruction during the A cycle of the STO mode if the parity bit of the word being written in storage is a "1" (parity even). The setting of Adder →A at this time enables the transfer of a +1 to the A register.

INPUT →A

The Input →A FF enables the transfer of the output of the input receivers in the A/Q or low-speed interface to the A register through the fan-in modules. The setting of Input →A in Character mode forces "1" outputs from the output inverters C and D on the V15 modules and inverter B on the V16 modules. The outputs of these inverters enable the selected input receivers to the fan-in modules. The t00 pulse transfers the 16-bit data word to the A register.

In the Character mode, the "0" input to the * inverter disables the input transfer to the high-order eight stages of the A register. The 8-bit character transfers to the low-order eight stages of the A register at t00.

The V250 pulse sets the Input →A FF during the A cycle of the INP instruction if the selected input device sends no Reject signal.



NOTES:

(1) DENOTES PAGE NUMBER FROM LOW SPEED COMPUTER DIAGRAMS.

CONTROL DATA CORPORATION	TITLE: A REGISTER	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C	DRAWING NO.: 60152700 REV: AC
			SHEET: PAGE: 31

Q REGISTER

The 16-bit Q register (auxiliary arithmetic) assists the A register in performing arithmetic and logical operations. The Q register is also used as an Index register for storage reference instructions and as an Output Address register for non-buffered I/O.

The Q register is divided into two V01 modules and receives its inputs from four V06 Adder/Shifter fan-out modules. The outputs of the Q register return to the Adder/Shifter via the A, Q fan-out modules and addend gates.

The Adder → Q FF controls the input to Q register selection.

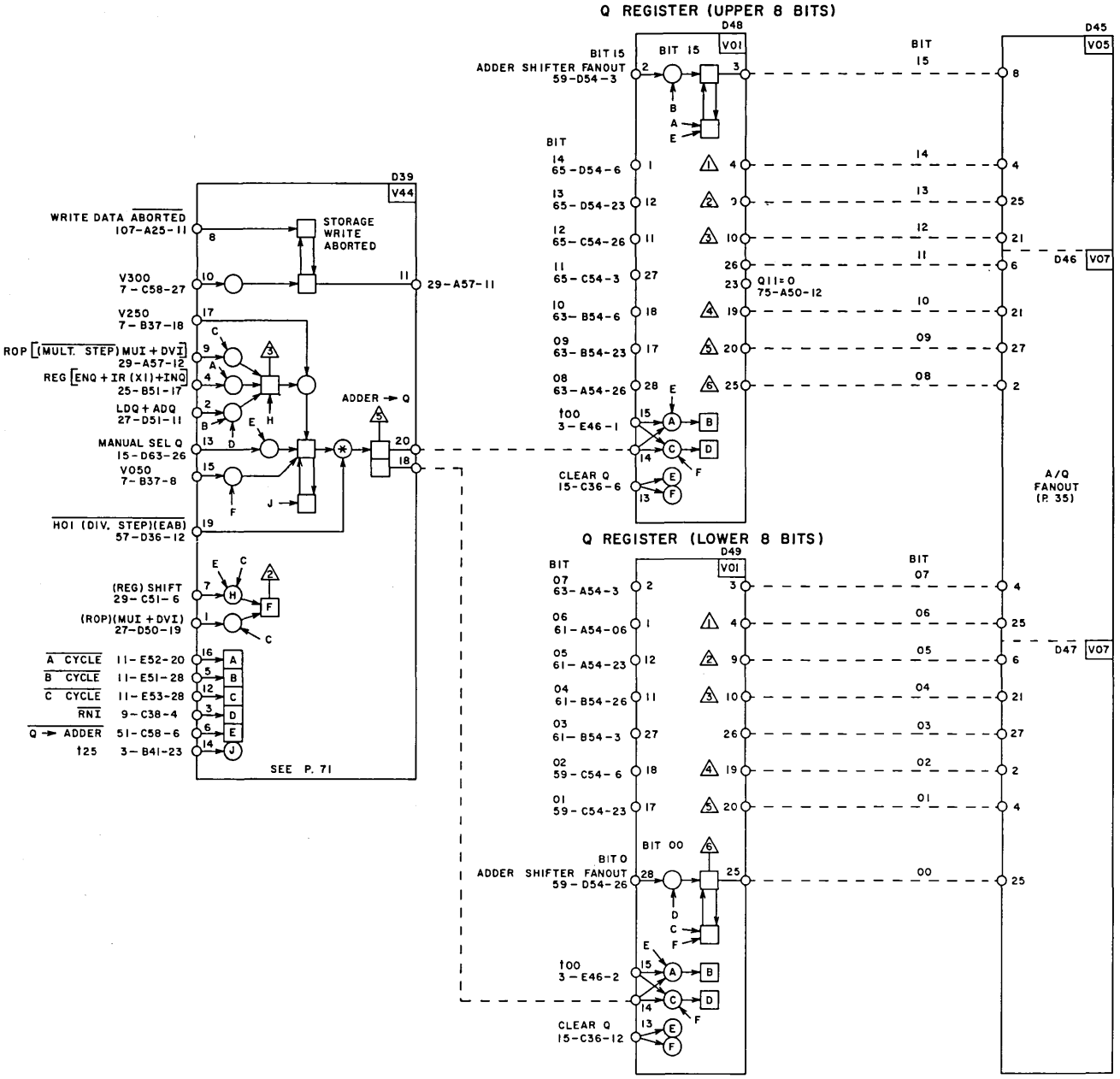
ADDER → Q CONTROL

The Adder → Q FF has three main setting gates. The first is satisfied if the manual Q register selector on the console is activated and the Q → Adder FF is set. At time V050 of the C cycle, the second gate is enabled if one of the indicated conditions is satisfied. At time V250, the third gate is enabled if one of the indicated conditions is satisfied. The t25 pulse clears the Adder → Q FF in all cases.

The setting of the Adder → Q FF enables a pulse to the A and C inverters of the V01 modules at t00. Therefore, the transfer from the Adder/Shifter to the Q register occurs 50 nanoseconds after the Adder → Q FF is set.

If the condition $\overline{\text{H01 (Div. Step)(EAB)}}$ is not satisfied, inverter * has a "1" output and the transfer of data to the Q register is blocked, even though the Adder → Q FF is set. This condition may occur during a divide step when subtracting (X) from (Q). An EAB occurs when X > Q.

The Q register clears when either the manual clear or Master Clear is selected. The inverters on V41 send a pulse to inverters E and F on the two V01 modules, clearing all Q register FFs.



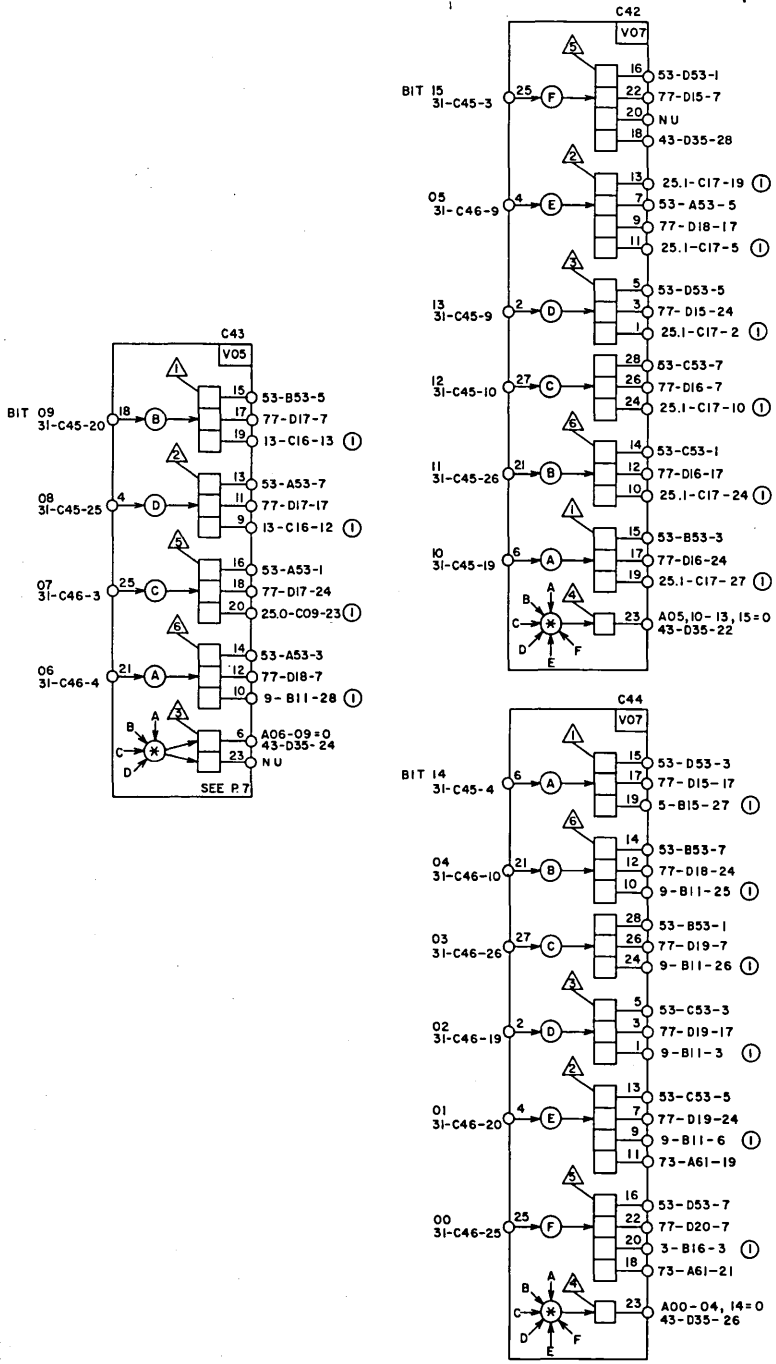
CONTROL DATA CORPORATION	TITLE: Q REGISTER	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C · DRAWING NO.: 60152700 · REV: A	
		SHEET · PAGE: 33	

A, Q FAN-OUT

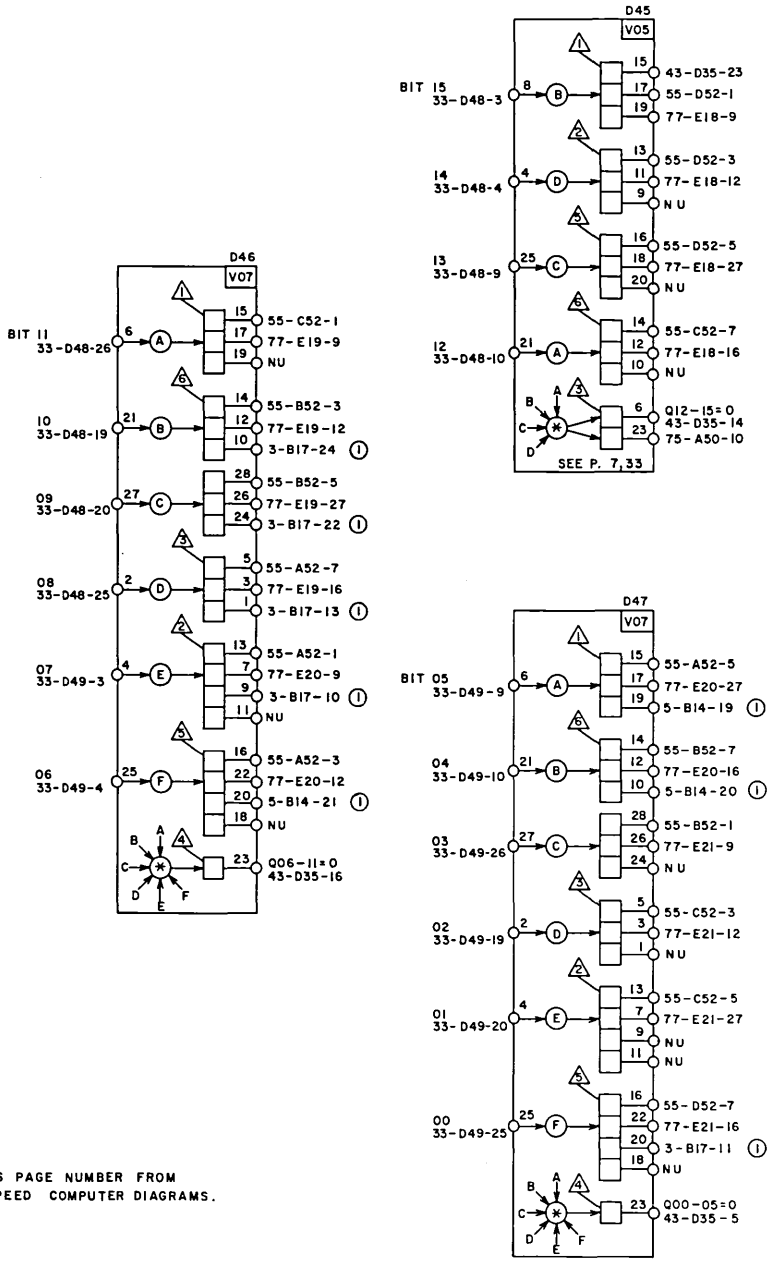
The A, Q FANOUT provides three additional outputs for the A and Q register.

The Adder/Shifter Fan-In, AQ I/O, and Skip FF receive the contents of the A, Q FANOUT. The * inverters in each Module send several bits in a group to the Skip FF. If the group of bits in "0", the output of the * inverter is a "0", which is inverted and sent to the Skip FF. The Skip FF searches for Zero contents of the A or Q registers.

A FANOUT



Q FANOUT



NOTES:

(1) DENOTES PAGE NUMBER FROM LOW SPEED COMPUTER DIAGRAMS.

CONTROL DATA CORPORATION	TITLE: A,Q FANOUT	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C · DRAWING NO.: 60152700 · REV: AC	
		SHEET · PAGE: 35	

P REGISTER

The P register contains the address of the current instruction. In most cases, the P register advances by one near the completion of each instruction. The outputs of the P register enter the addend gates of the Adder/Shifter. The Adder/Shifter forms the next instruction address, returning it to the P register.

The P register consists of 15 stages divided into two V01 modules. The P register receives inputs from four V06 Adder/Shifter fan-out modules. The V06 modules provide the input gates which select the Adder/Shifter inputs.

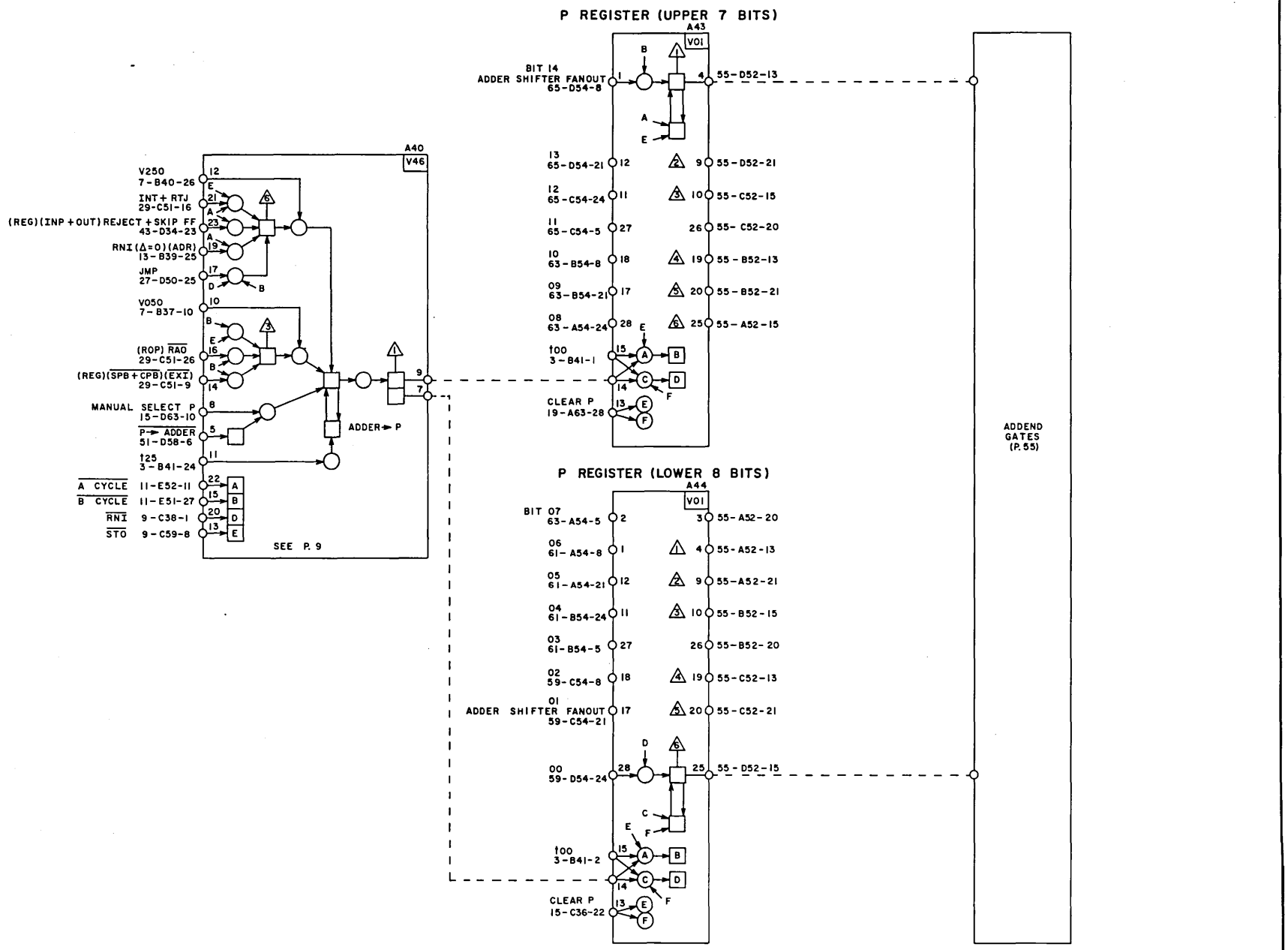
The Adder → P FF controls the input to P register selection.

ADDER → P CONTROL

The Adder → P FF has three main setting gates. The first gate is satisfied if the manual P register selector on the console is activated and the P → Adder FF is set. At time V050 of the B cycle, the second gate is enabled if one of the indicated conditions is satisfied. At time V250, the third gate is enabled if one of the indicated conditions is satisfied. The t25 pulse clears the Adder → P FF in all cases.

The setting of the Adder → P FF enables a pulse to the A and C inverters of the V01 modules at t00. Therefore, the transfer from the Adder/Shifter to the P register occurs 50 nanoseconds after the Adder → P FF is set.

The P register clears when either the manual clear or Master Clear is selected. The inverters on V41 send a pulse to inverters E and F on the two V01 modules, clearing all P register FFs.



CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE: P REGISTER	PRODUCT: 1704 SIZE: C · DRAWING NO.: 60152700 · REV: A SHEET · PAGE: 37	

X REGISTER

The X register consists of 16 stages divided into two V01 modules. The X register receives inputs from the Z register and the Adder/Shifter through the two V19 fan-in modules. The V19 modules provide the input gates which select the Z register or Adder/Shifter inputs.

The Resume and Adder → X FFs control the input to X register selection. The Resume and Adder → X control FFs are described below.

Z → X CONTROL (RESUME)

The Storage Resume signal sets the Resume FF at time t50 and clears the Req. Mem. FF. This time is relative to 50 nsec before the Resume transfer actually takes place. A Storage Write operation causes F to block the Resume output of V82. Thus the Resume transfer occurs only on Storage Read operations.

The outputs pass through inverters G and H and apply "1" inputs to A and C in the V01 modules. Additional Resume outputs enter C and D in the fan-in (V19) modules. As a result, the Z register "1" bits enter the X register at time t00. The X register stages corresponding to "0's" are cleared.

The t25 pulse clears the Resume FF. Thus, this FF remains enabled for 75 nsec after it is set.

ADDER → X CONTROL

The Adder → X FF has four main setting gates. The first of these sets the Adder → X FF during a B cycle at time V050 if one of the indicated conditions is satisfied. The remaining three main gates set the Adder → X FF at time V250 if the necessary conditions are satisfied. The X → Adder enable also sets the FF in a manual selection. The t25 pulse clears the Adder → X FF in all cases.

The setting of the Adder → X FF enables the Adder/Shifter input to the X register through inverters A and B on each V19 module. Thus, the t00 pulse transfers the Adder/Shifter output to the X register.

X REGISTER FAN-OUT

The X register output passes through four fan-out modules to obtain additional outputs and for control functions such as the extending of the Δ sign bit.

The low-order five stages of the X register pass through the V26 module. Each of the low-order four of these stages has four outputs that go to destinations indicated. (Stage 04 has one additional output to the translator.) The Δ = 0 translation is also sensed on this module for the low-order five stages.

Stages 5, 6, and 7 pass through the V27 module. These stages each have six outputs as indicated.

The high-order eight stages of the X register pass through two V28 modules. These stages have four outputs as shown except the sign bit (stage 15) and stage 11. The extra outputs of stage 11 are not used. The V28 modules also sense for the F ≠ 0 condition of the corresponding bits.

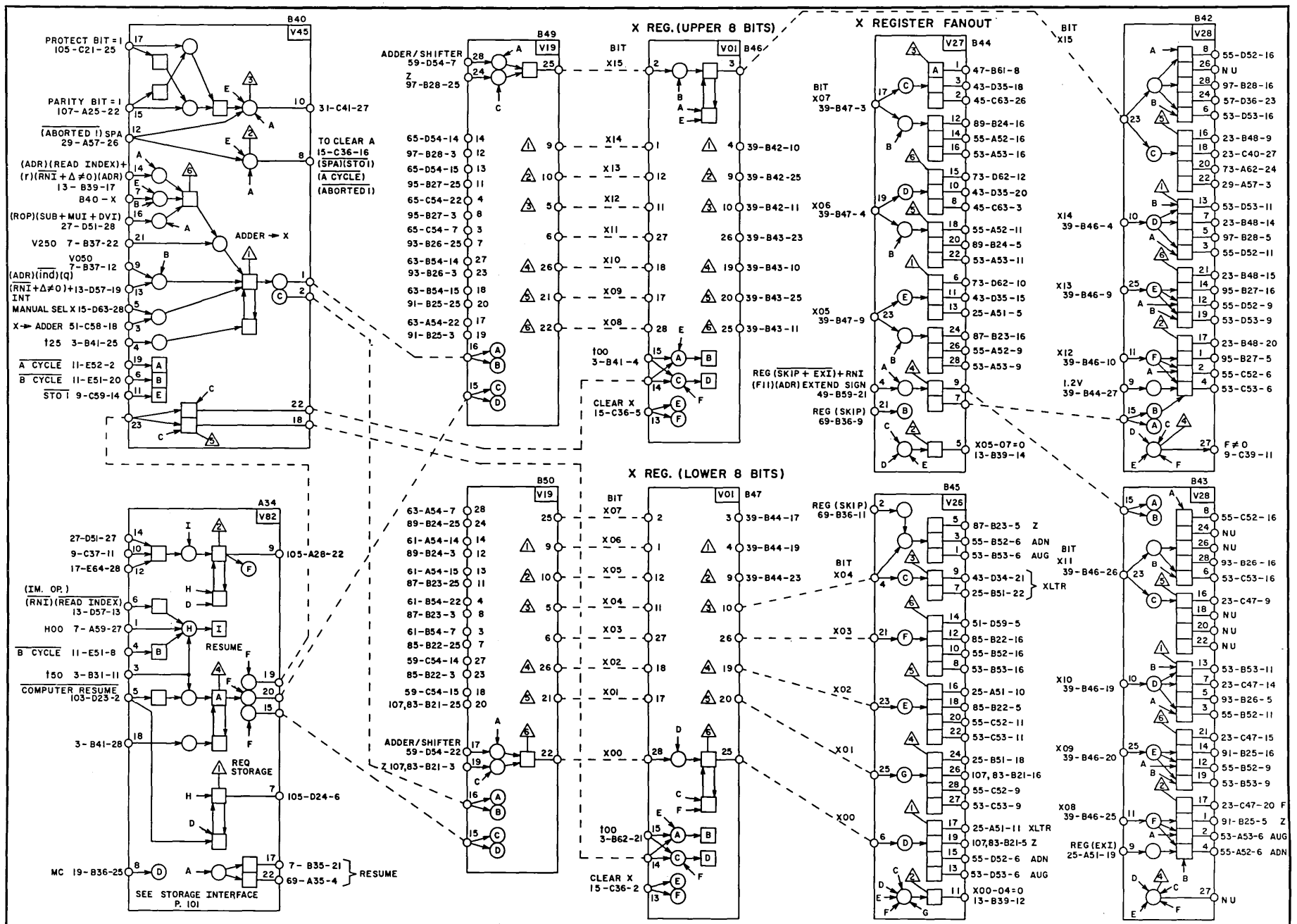
SKIP TRANSFERS

In the execution of a Skip instruction, the low-order four bits of the instruction, and thus the X register, contain the skip count. The outputs from stages 04-07 at this time are "0's". Thus a REG operation during a Skip instruction forces "0" outputs of stages 04-07 to the Addend gates and the Augend gates.

EXTEND SIGN

In the type of operations indicated, the sign bit of Δ (stage 07) is extended in the high-order eight outputs. If one of the indicated conditions is enabled and bit 07 is a "1" (negative sign), the output of the sign extension inverters on the V27 module enter inverters A and B on the two V28 modules. The outputs of A and B force "0" inputs to the fan-out inverters that feed the Addend and Augend gates. Thus, the high-order eight outputs to these gates are all "1's".

If, in a sign extension operation stage 07 contains a "0" (positive), inverter A on the V27 module forces "0" outputs from the sign extension inverters. The resulting outputs of A and B on the V28 modules gate the outputs of the high-order eight stages of the X register, which are cleared, at V050 time of each RNI sequence to the augend and addend gates.


X REG. (UPPER 8 BITS)
X REGISTER FANOUT
X REG. (LOWER 8 BITS)
B40 V45
PROTECT BIT = 1
105-C21-25
PARITY BIT = 1
107-A25-22
(ABORTED I) SPA
29-A57-26
(ADR)(READ INDEX)+
(r)(RNI+Δ≠0)(ADR)
13-B39-17
B40-X
(ROP)(SUB+MUI+DVI)
27-D51-28
V250 7-B37-22
V050 7-B37-12
(ADR)(ind)(q)
(RNI+Δ≠0)+13-D57-19
INT
MANUAL SEL X 15-D63-28
X→ ADDER 51-C58-18
↑25 3-B41-25
A CYCLE 11-E52-2
B CYCLE 11-E51-20
STO I 9-C59-14
ADDER → X
31-C41-27
TO CLEAR A
15-C36-16
(SPA)(STO I)
(A CYCLE)
(ABORTED I)
B49 V19
ADDER/SHIFTER
59-D54-7
Z
97-B28-25
65-D54-14
97-B28-3
65-D54-15
95-B27-25
65-C54-22
95-B27-3
65-C54-7
93-B26-25
63-B54-14
93-B26-3
63-B54-15
91-B25-25
63-A54-22
91-B25-3
BIT X15
V01 B46
X14
X13
X12
X11
X10
X09
X08
↑00 3-B41-4
CLEAR X
15-C36-5
39-B42-10
39-B42-25
39-B42-11
39-B43-23
39-B43-10
39-B43-25
39-B43-11
V27 B44
BIT X07 39-B47-3
BIT X06 39-B47-4
BIT X05 39-B47-9
REG (SKIP + EXI) + RNI
(FII)(ADR) EXTEND SIGN
49-B59-21
REG (SKIP)
69-B36-9
X05-07=0
13-B39-14
47-B61-8
43-D35-18
45-C63-26
89-B24-16
55-A52-16
53-A53-16
73-D62-12
43-D35-20
45-C63-3
55-A52-11
89-B24-5
53-A53-11
73-D62-10
43-D35-15
25-A51-5
87-B23-16
55-A52-9
53-A53-9
B42 V28
X14 39-B46-4
X13 39-B46-9
X12 39-B46-10
1.2V 39-B44-27
55-D52-16
NU
97-B28-16
57-D36-23
53-D53-16
23-B48-9
23-C40-27
73-A62-24
29-A57-3
53-D53-11
23-B48-14
97-B28-5
55-D52-11
23-B48-15
95-B27-16
55-D52-9
53-D53-9
23-B48-20
95-B27-5
55-C52-6
53-C53-6
F≠0
9-C39-11
A34 V82
27-D51-27
9-C37-11
17-E64-28
105-A28-22
(IM. OP.)
(RNI)(READ INDEX)
13-D57-13
H00 7-A59-27
B CYCLE 11-E51-8
↑50 3-B31-11
COMPUTER RESUME
103-D23-2
3-B41-28
RESUME
REQ STORAGE
105-D24-6
MC 19-B36-25
7-B35-21
69-A35-4
RESUME
SEE STORAGE INTERFACE P. 101
B50 V19
63-A54-7
89-B24-25
61-A54-14
89-B24-3
61-A54-15
87-B23-25
61-B54-22
87-B23-3
61-B54-7
85-B22-25
59-C54-14
85-B22-3
59-C54-15
107,83-B21-25
ADDER/SHIFTER
59-D54-22
Z 107,83-B21-3
↑00 3-B62-21
CLEAR X
15-C36-2
B47
39-B44-17
39-B44-19
39-B44-23
B45 V26
REG (SKIP)
69-B36-11
BIT X04
BIT X03
BIT X02
BIT X01
BIT X00
87-B23-5 Z
55-B52-6 ADN
53-B53-6 AUG
43-D34-21
25-B51-22
XLTR
51-D59-5
85-B22-16
55-B52-16
53-B53-16
25-A51-10
85-B22-5
55-C52-11
53-C53-11
25-B51-18
107,83-B21-16
55-C52-9
53-C53-9
25-A51-11 XLTR
107,83-B21-5 Z
55-D52-6 ADN
53-D53-6 AUG
X00-04=0
13-B39-12
B43 V28
BIT X11 39-B46-26
X10 39-B46-19
X09 39-B46-20
X08 39-B46-25
REG (EXI) 25-A51-19
55-C52-16
NU
NU
93-B26-16
53-C53-16
23-C47-9
NU
NU
NU
53-B53-11
23-C47-14
93-B26-5
55-B52-11
23-C47-15
91-B25-16
55-B52-9
53-B53-9
23-C47-20 F
91-B25-5 Z
53-A53-6 AUG
55-A52-6 ADN
NU
CONTROL DATA CORPORATION
COMPUTER DIVISION
TITLE
X REGISTER
PRODUCT 1704
SIZE C
DRAWING NO. 60152700
REV
SHEET
PAGE 39

Y REGISTER

The 16-bit Y register is contained on two V01 modules. The Y register contains storage addresses for subsequent transfer during a storage reference. The Y register is also used as a counter during Multiply, Divide, and Shift instructions.

The first V01 module contains bits 00-06 and bit 08. The second V01 module contains bit 07 and bits 09-15. Bits 00-05 and bit 08 receive inputs from a V22 module, and bit 06 receives its input from a V42 module. The second V01 module receives its inputs from the V06 Adder/Shifter fan-out modules.

The control FFs for the Y register are contained on the V42 module and receive set inputs from the V43 module. The Y register outputs feed V13 and V14 fan-out modules and are gated to the S register, Adder/Shifter or Y decrementer. All control FFs set at t50 and clear at t25. The Y register gating occurs at t00. Therefore, the actual transfer to the Y register occurs 50 nsec after the control FFs are set.

The Y register clears when either the manual clear or Master Clear is selected. The clear pulse enters inverters E and F on the two V01 modules, clearing all Y register FFs.

ADDER → Y CONTROL

The Adder → Y FF has three main setting gates. The first gate is satisfied if the manual Y register selector on the console is activated and Y → Adder FF is set. At time V050 (V42) of the B cycle (V43), the second gate is set if one of the indicated conditions is satisfied. The third gate is set at time V250 (V42) of the A cycle (V43) if one of the indicated conditions is satisfied. The setting of the Adder → Y FF enables inverters A and B on the V22 module and A and C on the second V01 module. The V22 module provides the Adder/Shifter input gates for selecting bits 00-05 and bit 08 of the Y register. Module V42 provides the input selection for bit 06. The second V01 module receives its inputs from the V06 Adder/Shifter fan-out modules.

For Shift instructions, the Adder → Y FF enables the lower 8 bits of the shift instruction format into the Y register. Bits 00-04 contain the shift count.

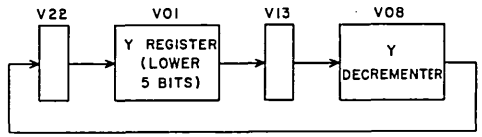
For other instructions, the Adder → Y FF enables the effective address or partially modified address into the Y register. The effective address is held in the Y register until transfer to the S register during a storage reference. Bit 15 does not transfer to the S register. Bit 15 is a sign bit when the effective address is an operand for Read Operand instructions.

DECREMENT Y CONTROL

The Decrement Y FF has three main setting gates. If any one of the following gates are satisfied, the Decrement Y FF sets and the value in the lower 5 bits of the Y register decreases by one.

	Time (V42)	Cycle (V43)	Condition
1)	V050	C	(Y00-04 ≠ 0) (REG)(SHIFT)($\overline{\text{QA SHIFT}}$)
2)	V250	C	(Y00-04 ≠ 0)
		or	
	V250	A	(Y00-04 ≠ 0) (ROP) (MUI)
3)	V350	A	(Y00-04 ≠ 0) (REG)(SHIFT)

The Decrement Y FF enables the C inverter on the V22 module, and the A and C inverters on the first V01 module. This gates the decremented value of Y back into the lower 5 bits of the Y register to t00. Five bits are used to express the maximum shift count of $31_{10} = 37_8 = 1E_{16}$. Five bits are also needed for the multiply and divide when the Y register decrements from 10_{16} ($20_8 = 16_{10}$) to 0.



In short cycle (SC1) operations which occur only in shift or MUI instructions, the V250 pulse occurs 100 nsec earlier. This case effects only condition 2 listed previously. In this condition, the Decrement Y FF is set 100 nsec earlier since the short cycle requires 100 nsec to transmit the operand through the Adder/Shifter.

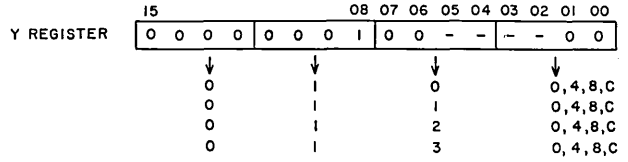
10_{16} → Y CONTROL

The 10_{16} → Y FF establishes the starting Y register count (10_{16}) for Multiply and Divide instructions. As each shift and compare sequence is done, the Y register decrements by one until Y00-04 = 0.

The 10_{16} → Y FF sets at time V050 (V42) of the A cycle (V43) when ROP and MUI + DVI signals are present. The 10_{16} → Y FF enables bit 04 of the Y register to set at time 00, thus forming a binary 10000 (10_{16}).

STATE → Y CONTROL

The State → Y FF enables the forming of an address to locate the return addresses for each of the 16 possible interrupt states. The table on page 71 shows the interrupt states and location of return addresses. The location of the return addresses may be formed by changing bits 02, 03, 04, and 05 and setting bit 08 to a "1".



The State → Y FF sets at time V050 (V42) of the B cycle (V43) when an Interrupt signal is present. The State → Y FF enables inverter D on the V22 module and inverters A and C on the first V01 module. Four interrupt

state inputs are gated into the V22 module from the V11 and V12 module on page 71. At t00, the state inputs are gated into bits 02, 03, 04, and 05 of the Y register and bit 08 is set to a "1". The address to locate the return address transfers through the V13 and V14 modules to the S register.

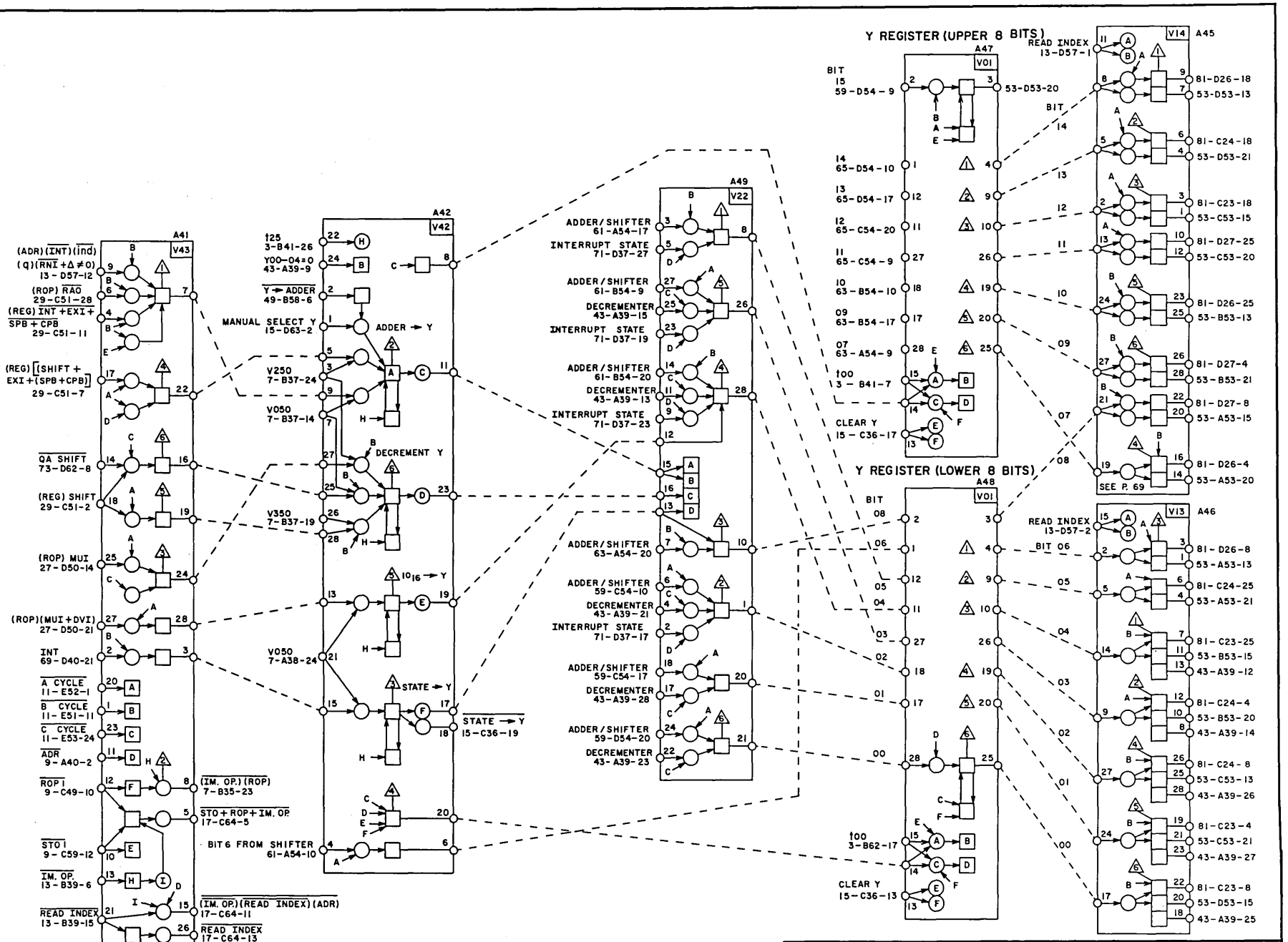
CONSOLE INDICATOR CONTROL

Module V43 contains the control for three console indicators. The three indicator outputs are enabled by a display pulse on module V55, page 21. The display pulse enables the indicators only if the following conditions are present:

1) Indirect Address = $\overline{(\text{IM. OP.})}$ $\overline{(\text{READ INDEX})}$ ADR
2) Storage Index = READ INDEX
3) Operand = STO + ROP + IM. OP.

$\overline{(\text{IM. OP. (ROP)}}$ CONTROL

An inverter whose output is $\overline{(\text{IM. OP.})}$ $\overline{(\text{ROP})}$ is located on the bottom of module V43. This pulse feeds module V55, page 7, and is one of the conditions which stops the timing chain.



CONTROL DATA CORPORATION	TITLE	PRODUCT	
COMPUTER DIVISION	Y REGISTER	1704	
		SIZE C	DRAWING NO. 60152700 REV E
			SHEET PAGE 41

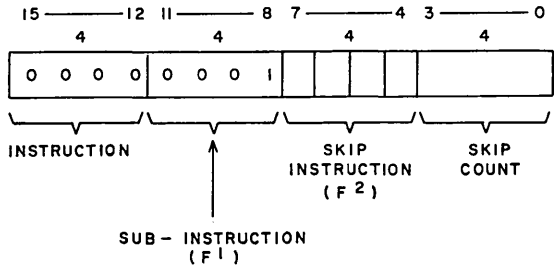
Y-DECREMENTER

The Y-Decrementer operates as a counter during Multiply, Divide, and Shift instructions. The lower 5 bits of the Y register hold the shift count which decreases by one on each pass through the decrementer. The decrementing is performed logically by inspecting each bit in order, starting with Y00. Each bit is complemented until the decrementer reaches a "1". The "1" is complemented and the remaining higher bits (if any) are transferred through the decrementer without being changed. For example, if Y00 is a "1" it is complemented, but Y01-04 remain unchanged during this particular pass.

When the count is reduced to zero (Y00-04=0), the gate in the lower-right corner of the V08 module is enabled, the Y-Decrementer is disabled, and the shifting in the current instruction is completed.

SKIP FF

A zero is the instruction field and a one in the sub-instruction field identifies a Skip instruction. Diagrammed below is the Skip instruction format.



When the skip condition is met, the contents of the skip count +1 is added to P to obtain the address of the next instruction (e.g., when the skip count is zero, go to P + 1). When the skip condition is not met, the address of the next instruction is P + 1 (skip count ignored). The skip count does not have a sign bit.

The Z81 and V53 modules examine X04-07 to determine which skip instruction is to be executed. The table following illustrates the possible skip instruction translations and their conditions.

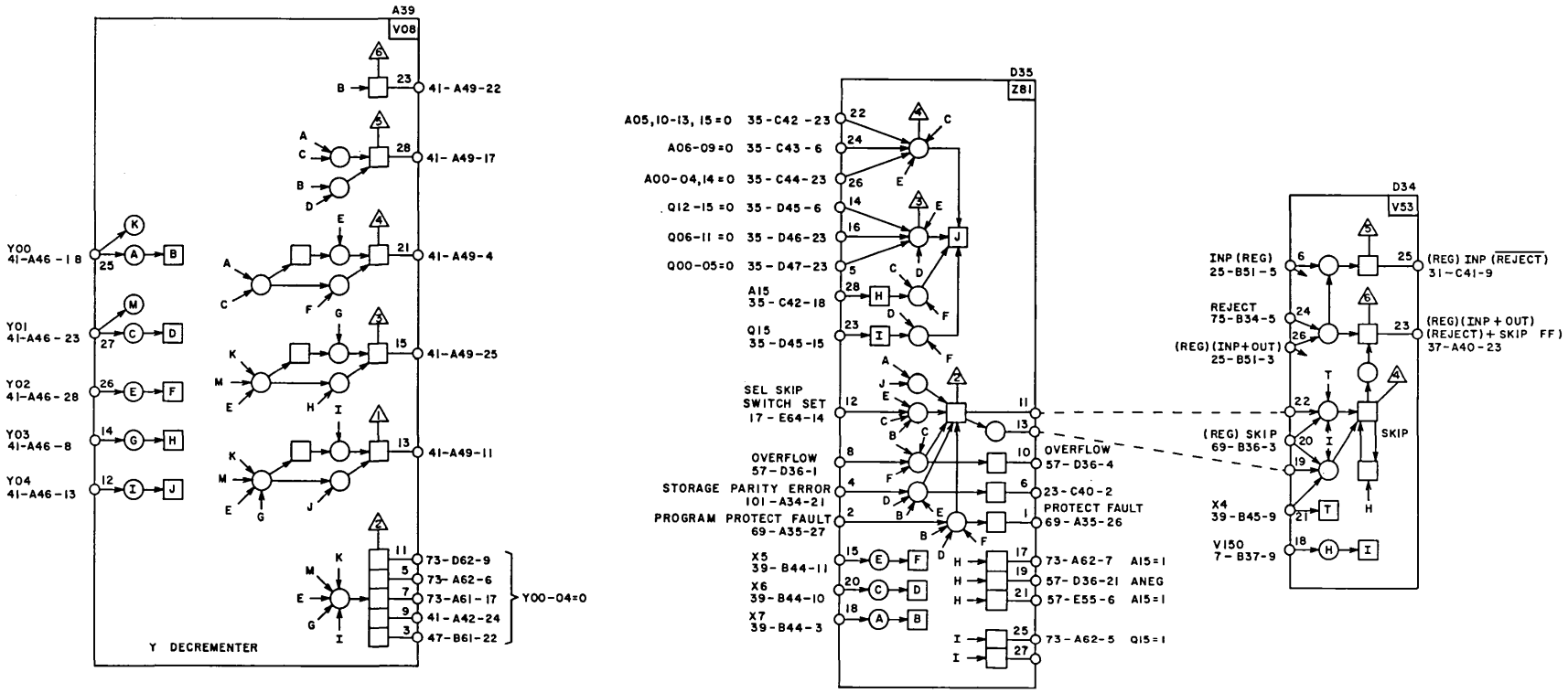
The Skip instruction conditions (contents of A and Q registers, Selective Skip switch, Overflow, Storage Parity Error, and Program Protect Fault) enter the Z81 module. The contents of the A and Q registers are sensed for sign and for zero or not zero.

Skip Instruction (Hex.)	Bits 7 6 5 4	Skip If
0	0000	A = +0
1	0001	A ≠ +0
2	0010	A = +
3	0011	A = -
4	0100	Q = +0
5	0101	Q ≠ +0
6	0110	Q = +
7	0111	Q = -
8	1000	Switch set
9	1001	Switch not set
A	1010	Overflow
B	1011	No overflow
C	1100	Storage Parity Error
D	1101	No Storage Parity Error
E	1110	Program Protect Fault
F	1111	No Program Protect Fault

The logic in the Z81 and V53 modules recognizes the selected Skip instruction and determines if its conditions are satisfied. The conditions (V150) (REG) (SKIP) and the Skip instruction satisfied enable the Skip FF. The setting of the Skip FF sends a "1" through two inverters to the Adder → P FF shown on page 37.

The condition (REG) (INP + OUT) (Reject) sends a "1" through two inverters to the same Adder → P FF as the Skip FF.

The condition (INP) (REG) ($\overline{\text{Reject}}$) sets the I/O→A FF shown on page 31.



CONTROL DATA CORPORATION	TITLE: Y DECREMENTER AND SKIP FF	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C · DRAWING NO.: 60152700 · REV: Y	
		SHEET · PAGE: 43	

ADDER CONTROLS (XR AND LP)

The Exclusive OR (XR) and Logical Product (LP) control FFs enable the corresponding logical operations on the Adder/Shifter modules. The XR and LP FFs are contained on the V38 module. The inputs to the corresponding inverters on the V39 module specify the conditions for setting and clearing XR and LP.

EXCLUSIVE OR (XR) CONTROL

When set, the XR FF enables the Exclusive OR (A⊻B) function in the Adder/Shifter. The Exclusive OR can take place between two operands, as in an IR instruction, or between an operand and all "1's", as in complementing a negative operand in the Multiply instruction. Examples of both cases are shown below:

15	14	13	12	11	10	-	-	-	-	0	Bit Positions
1	0	1	1	0	1	-	-	-	-	1	Operand A
0	1	1	0	1	1	-	-	-	-	0	Operand B
1	1	0	1	1	0	-	-	-	-	1	Result

15	14	13	12	11	10	-	-	-	-	0	Bit Positions
1	0	1	1	0	1	-	-	-	-	1	Operand A
1	1	1	1	1	1	-	-	-	-	1	All "1's" for Operand B
0	1	0	0	1	0	-	-	-	-	0	Result

In both examples, a "1" appears in the result only when a "1" is in a certain bit position of one operand and a "0" in the same bit position of the other operand. Thus, a "1" results when a "1" exists in operand A or B but not in both. In the second example, all "1's" are used as a mask to complement operand A. In this way, a number can be converted to the ones-complement equivalent. The second example shows a negative number (operand A) converted to its positive equivalent through the XR function.

The XR FF has two Set/Clear gates (A, B and C, D) and one Clear gate (E). The A, B gate sets XR at V100 time while the C, D input sets the FF at V300 time if one of the corresponding inverter inputs is satisfied on the V39 module. Inverter E clears XR at V200 time if the input to the corresponding inverter on the V39 module is satisfied: (MUI) (SR1) (C CYCLE) + (DVI) (Y00-04 = 0) (SR 2) (C CYCLE).

A typical XR operation for the first example is had by assuming an IR instruction in the REG mode, A cycle enabled and bit X_6 of the instruction code set. The setting of X_6 specifies an XR operation between the operands in the origin registers (X_3, X_4, and X_5). In this case, XR is set at V100 time (B, C) and the Exclusive OR function is enabled in the Adder/Shifter modules. When the selected operands are gated into the Adder/Shifter, the Exclusive OR operation takes place.

An XR operation for the second example takes place during the A cycle of the ROP mode for a DVI instruction with SR 2 set. In this case, the initial dividend is negative (SR 2 set) and (Q) is complemented prior to the first divide step. Thus, XR is set at V300 time (C, D). Since (Q) is now gated to the addend gates while all "1's" are enabled into the augend gates, the XR enable complements the (Q) in the Adder/Shifter.

LOGICAL PRODUCT (LP)

The setting of the LP FF enables the Logical Product (AND) function on the Adder/Shifter modules. The LP function takes place between two operands, as in IR or AND instructions, or between an operand and all "1's" to enable a straight-through transfer of an operand through the Adder/Shifter, as in a Multiply instruction. Examples of both cases are shown below:

15	14	13	12	11	10	-	-	-	-	0	Bit Positions
1	0	1	1	0	1	-	-	-	-	1	Operand A
1	1	1	1	0	0	-	-	-	-	0	Operand B
1	0	1	1	0	0	-	-	-	-	0	Result

15	14	13	12	11	10	-	-	-	-	0	Bit Positions
1	0	1	1	0	1	-	-	-	-	1	Operand A
1	1	1	1	1	1	-	-	-	-	1	All "1's" for Operand B
1	0	1	1	0	1	-	-	-	-	1	Result

In both examples, a "1" appears in the result only when a "1" exists in corresponding bit positions of the two operands. Thus, a "1" results when a "1" exists in operand A and B.

The LP function is often used to mask out certain portions of an operand, as in the first example. In this case the low-order 12 bits of operand B are all "0's", and the high-order 4 bits are all "1's". Thus, all but the high-order 4 bits of operand A are masked out.

For example, assume an AND instruction in the ROP mode, B cycle, and V100 time (H01) (t00). In this case, the operand read from storage (X) and the operand in A transfer to the Adder/Shifter simultaneously with the setting of LP. As a result, LP enables a Logical Product operation in the Adder/Shifter between the two operands.

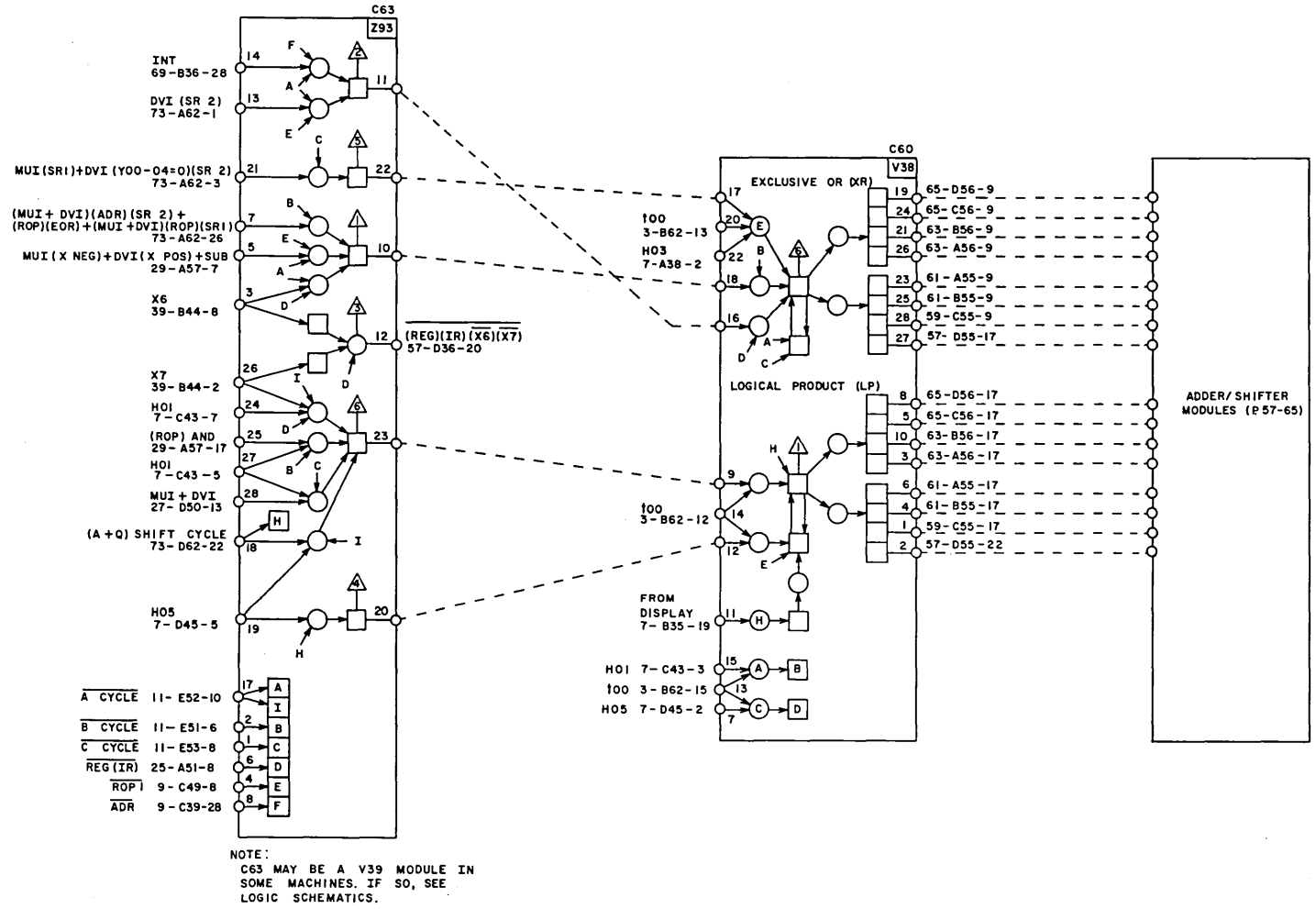
The LP function also enables a straight-through transfer of an operand through the Adder/Shifter. In this case, all the bits of one operand are "1's". Thus, operand A transfers through the Adder/Shifter either unchanged or shifted right or left.

An example of this type of LP operation is had by assuming a Multiply instruction, C cycle, and V100 time (H01 and t00). These conditions set LP simultaneously with the transfer of (A) → Adder. Since the Shift-Right control was previously set, LP enables the (A) to be shifted one place to the right.

The LP FF has two Set gates and two Clear gates. The Stopped mode sets LP through inverter H. The setting of LP at this time enables the transfer of the manually selected register output through the Adder/Shifter.

The other Set gate is enabled at t00 time if the input conditions to one of the corresponding inverters on the V39 module are satisfied. Three of the inverter gates are enabled at V100 time (H01 and t00) while the remaining gate is enabled at V300 time (H05 and t00).

The output of inverter E clears LP at V200 time (H03 and t00) simultaneously with XR. Inverter E is enabled at the termination of the C cycle of a Multiply or Divide instruction. The other Clear gate to LP is enabled at V300 time (H05 and t00) if the input conditions to one of the corresponding inverters on the V39 module are enabled. For example, LP is cleared during the B cycle of each ROP mode at V300 time.



NOTE:
C63 MAY BE A V39 MODULE IN SOME MACHINES. IF SO, SEE LOGIC SCHEMATICS.

CONTROL DATA CORPORATION	TITLE: ADDER CONTROLS (XR + LP)	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C	DRAWING NO.: 60152700 REV: A
			SHEET PAGE: 45

ADDER CONTROLS (SHIFT)

The Shift Adder Controls enable the left or right Shift operations on the Adder/Shifter modules. These controls consist mainly of the Right Shift (RS) and Left Shift (LS) FFs, the Set/Clear input conditions, and the fan-outs for these FFs.

The RS and LS FFs and the input Set/Clear enables are contained on the V37 module. The RS, LS, and $\overline{\text{shift}}$ fan-outs to the Adder/Shifter modules are contained on the V23 module.

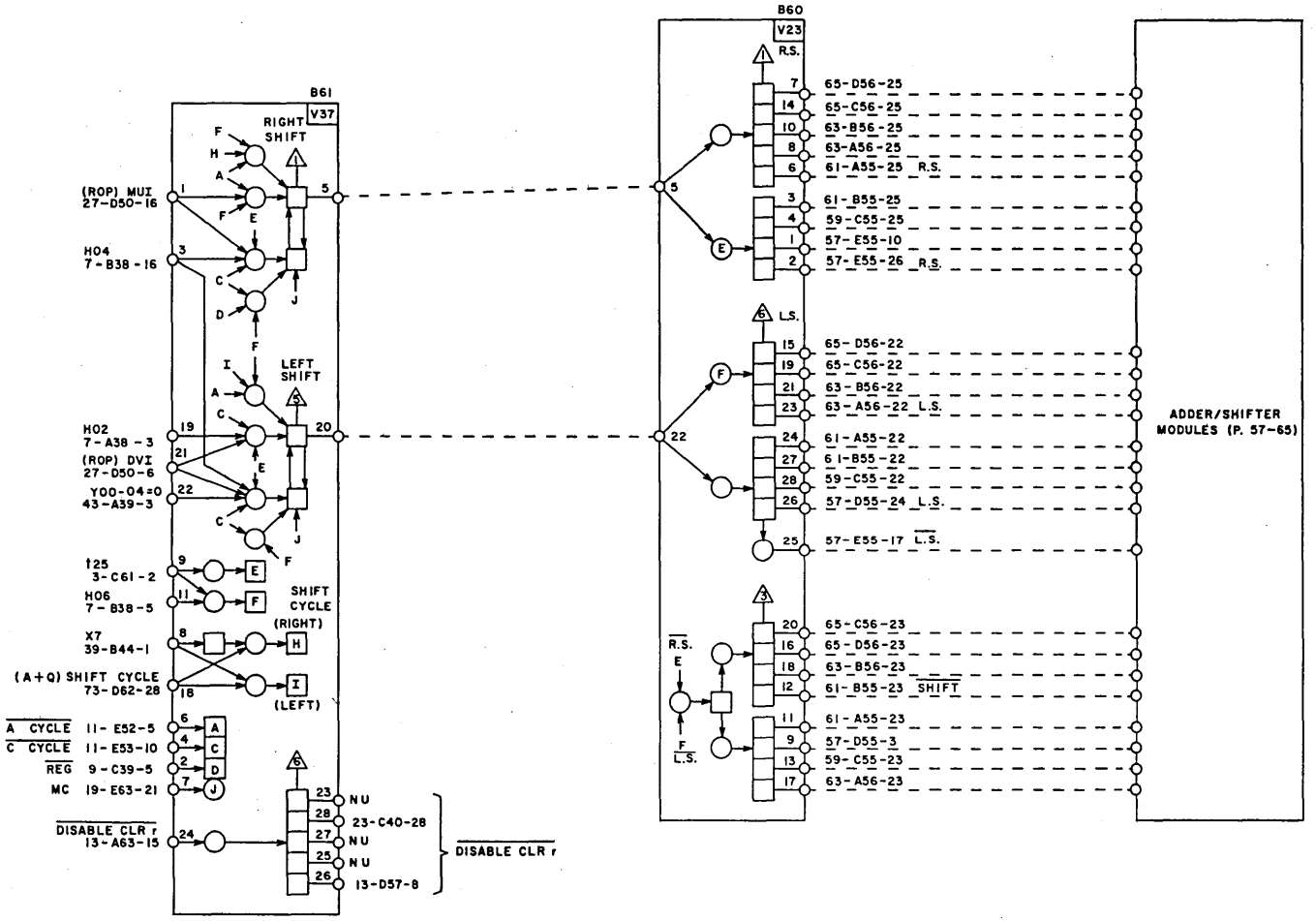
The RS and LS FFs are set and cleared under similar conditions. In Shift cycle operations, RS or LS is set by inverter F at V325 time (t25 and H06) in the A cycle. If bit 7 (X_7) of the instruction code is a "1" at this time indicating a Left Shift, inverter 1 enables the setting of LS. If X_7 = "0", RS is set.

The RS or LS FFs are cleared by inverter F in the C cycle. Since H06 is not set in the C cycle until V300 time of the last shift cycle, the clearing of LS or RS at this time indicates the completion of the shifting operation.

In Multiply operations inverter F sets RS in the A cycle of the ROP mode. Since H04 is not set until V200 time of the C cycle for the last multiply iteration, inverter E clears RS at V225 of the last multiply iteration.

In Divide operations, inverter E sets LS at V100 time (H02 and t25) of the C cycle for each divide iteration. Inverter F clears LS at V325 time of each iteration. When Y_{00-04} = 0 indicating the divide is complete, inverter E clears LS at V225 time of the last iteration.

The V23 module provides eight outputs for the RS and LS enables. One output from each connects to each of the Adder/Shifter modules. The V23 module also provides the $\overline{\text{shift}}$ enable to the Adder/Shifter module. If either the RS or LS is set, inverter E or F on the V23 module enters a "0" in the $\overline{\text{shift}}$ enable fan-out. As a result, the $\overline{\text{shift}}$ enable becomes a "0".



CONTROL DATA CORPORATION	TITLE: ADDER CONTROLS (SHIFT)	PRODUCT 1704
COMPUTER DIVISION		SIZE C · DRAWING NO. 60152700 · REV P
		SHEET · PAGE 47

ADDER GATE CONTROLS

The Adder Gate Control FFs enable the input to the augend and addend gates according to the translaged conditions of the instruction being executed. Only one input is enabled to the augend and/or addend gates at a time. If no input is enabled to the augend or addend gates, the corresponding adder inputs receives -0. This input enables the adder to add -0 to the other input, such as in a simple register transfer, to perform an exclusive OR, or logical product function.

AUGEND GATES

Four FFs control the inputs to the augend gates: A → Adder, +1 → Adder, Y → Adder, and X → Augend. The block diagram (p.1) shows that these four quantities enter the augend gates. Since the X register enters both the augend and addend gates, a separate FF controls the entry of the X register to the augend and addend gates.

The Augend Control FFs are contained on two V04 modules. The FFs are set at V100 (H01 and t00) or V300 time (H05 and t00). The manual selection of A or Y for display enables the setting of the corresponding control FF at time t00. For example, if A is manually selected, the manual input becomes a "1". The Stopped condition of the computer partially enables inverter I. The t00 pulse produces a "1" output of I which sets the A → Adder FF. As a result, the contents of A are displayed on the indicators connected to the Adder outputs.

On Multiply (MUI) or Divide (DVI) operations, the A→ Adder FF is cleared on every V200 time of the C cycle by inverter O.

A→ ADDER

The A→ Adder FF gates the outputs of the A register to the augend gates of the Adder/Shifter when set. The conditions determining the setting of this FF are enabled at the inputs to the two groups of inverters on the V35 module.

For example, during each shift cycle of a Shift A instruction, the V300 pulse sets the A→ Adder FF on both the A cycle and C cycle. This function gates the contents of the A register into the Adder/Shifter for the Shift operation.

For another example, assume that the X_5 bit of the IR instruction is set, designating A as the origin register for the inter-register transfer. Thus, in the A cycle portion of the REG mode, the V100 pulse sets the A→ Adder FF, enabling the transfer of the contents of the A register to the Adder/Shifter.

The Command Timing Sequences list the specific conditions and times for the setting of the A → Adder FF for the applicable instruction.

+1 → ADDER

The setting of the +1 → Adder FF gates a +1 input to the augend gates of the Adder/Shifter. This input is used mainly to add one to the address of the present instruction (P) to get the address of the next instruction. For example, during the A cycle of the ROP mode of all instructions except EXI, MUI, or DVI, the V300 pulse sets the +1 → Adder FF which initiates the advancing of P for the next instruction. The Block +1 function inhibits, through inverter D, the setting of the +1 → Adder FF which initiates the advancing of P for the next instruction. The Block +1 function inhibits the advancing of P under certain instruction conditions, such as after Clear P or an internal reject.

In the B cycle of the ADR mode in the RTJ instruction, the +1 → Adder FF is set at V100 time. This function performs the P + 1 function which is stored at the effective address. The P + 1 value represents the return instruction address following the completion of the subroutine.

Y → ADDER

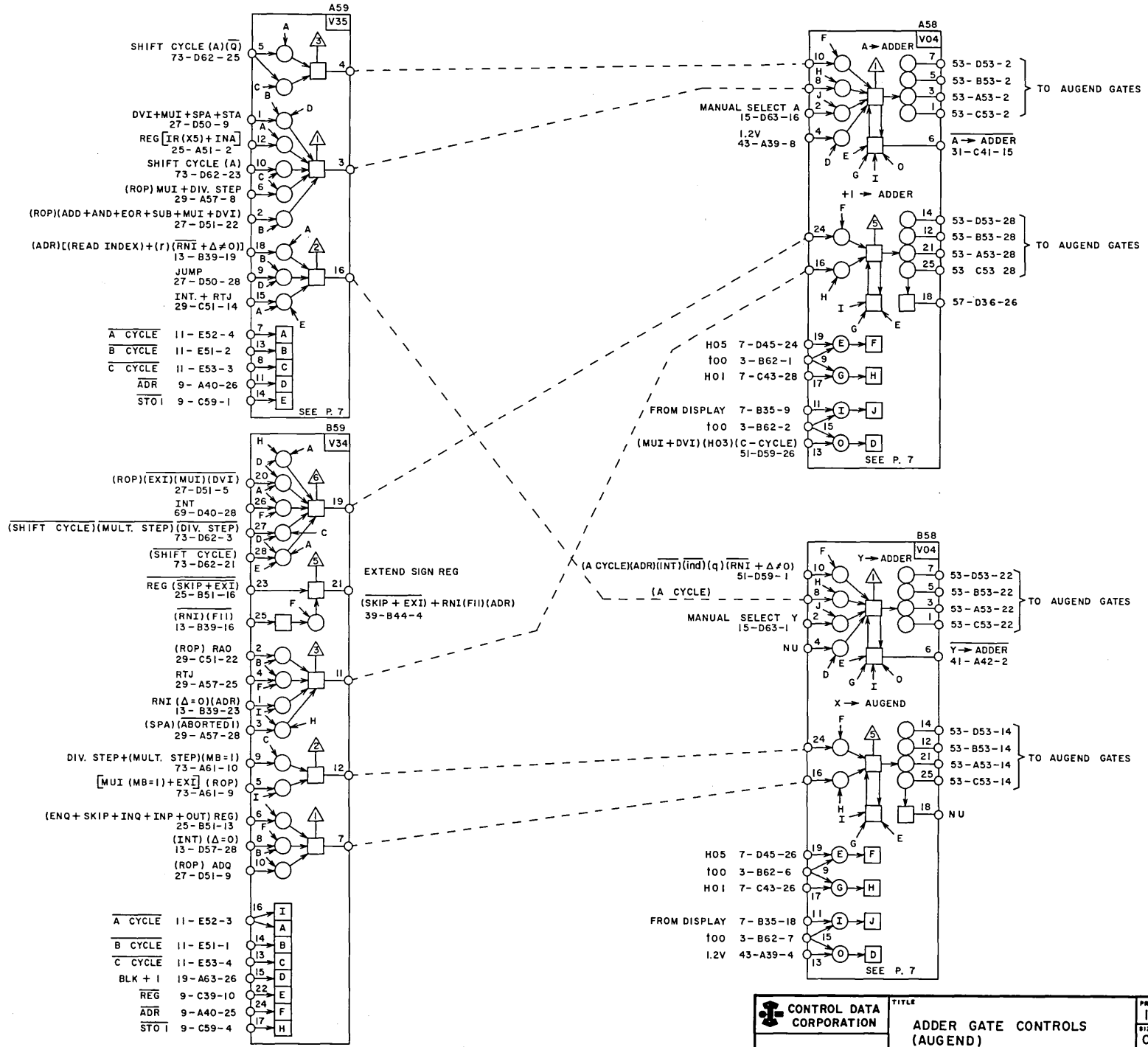
The Y → Adder is used mainly in address modification functions. In this case, the quantity in the Y register which represents base address or partially formed effective address is gated to the adder. The adder adds the quantity to another value in order to form the final effective address.

For example, assume the following conditions: (ADR) $\overline{\text{(INT)}}$ (ind) (q) (A cycle). Thus, in an indirect address function, the contents of the Q register (q index) is added to the base address (Δ in the Y register) to form the effective address. In this case, the V300 pulse sets the Y → Adder FF which gates the contents of the Y register to the augend gates. Simultaneously, the contents of the Q register transfer to the addend gates.

X → AUGEND

The setting of the X → Augend FF gates the contents of the X register to the augend gates. The inputs to the corresponding inverters on the V34 module specify the conditions for setting the X → Augend FF.

For example, in the C cycle of the Mult. Step operation with MB = 1, the X → Augend FF is set at V300 time. This function transfers X to the augend gates while the simultaneous setting of the Q → Adder FF gates Q to the addend gates. Thus, Q (partial product) is added to X (multiplicand) which produces the next partial product or final product in the case of the last Mult. Step.



CONTROL DATA CORPORATION	TITLE: ADDER GATE CONTROLS (AUGEND)	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C	DRAWING NO.: 60152700
		REV: AP	SHEET: PAGE 49

ADDEND GATES

Four FFs control the inputs to the addend gates: Q → Adder, X → Addend, P → Adder, and Mask → Adder. Thus, the setting of one of these FFs transfers the output of the corresponding register to the addend gates of the Adder/Shifter. Only one of the Addend Control FFs is set at a time. If none of these FFs are set, the addend gates receive an input of all "1's"

The Addend Control FFs are contained on two V04 modules. The FFs are set at V100 (H01 and t00) or V300 (H05 and t00). The manual selection of Q, X, P, or Mask for display enables the setting of the corresponding control FF at time t00. The FFs are set in the display condition in the same manner as the Augend Control FFs.

The Command Timing Sequences list the times and specific conditions for setting the Addend Control FFs.

Q → ADDER

When set, the Q → Adder FF gates the output of the Q register into the addend gates of the Adder/Shifter. The inputs of two groups of inverters on the V33 module establish the conditions for setting the Q → Adder FF.

An example of the setting of the Q → Adder FF is made by assuming the following conditions: (ADR) ($\overline{INT}$) ($\overline{ind}$) (q) ($\overline{RNI}$ + Δ = 0). Thus, the contents of Q (q index) are added to the base address to form the effective address. At V300 time of the A cycle (H005 and t00), the output of inverter J on the V04 module sets the Q → Adder FF.

During MUI or DVI operations, the Q → Adder is set at the V300 time of the A cycle during the ROP mode. In a Multiplication operation, this action initiates the initial adding of Q to the multiplicand in X if MB is set. On each following Mult. Step., the Q → Adder FF is reset at V300 of the C cycle.

X → ADDEND

The inputs to the four corresponding inverters on the V33 card specify the conditions for setting the X → Addend. For example, the V100 pulse sets the X → Addend FF on every A cycle of the ROP mode.

In addressing operations $\overline{RNI\ (\Delta = 0)}$ (ADR), V100 of the A cycle sets the X → Addend FF. This operation transfers the base address in X to the adder for possible address modification.

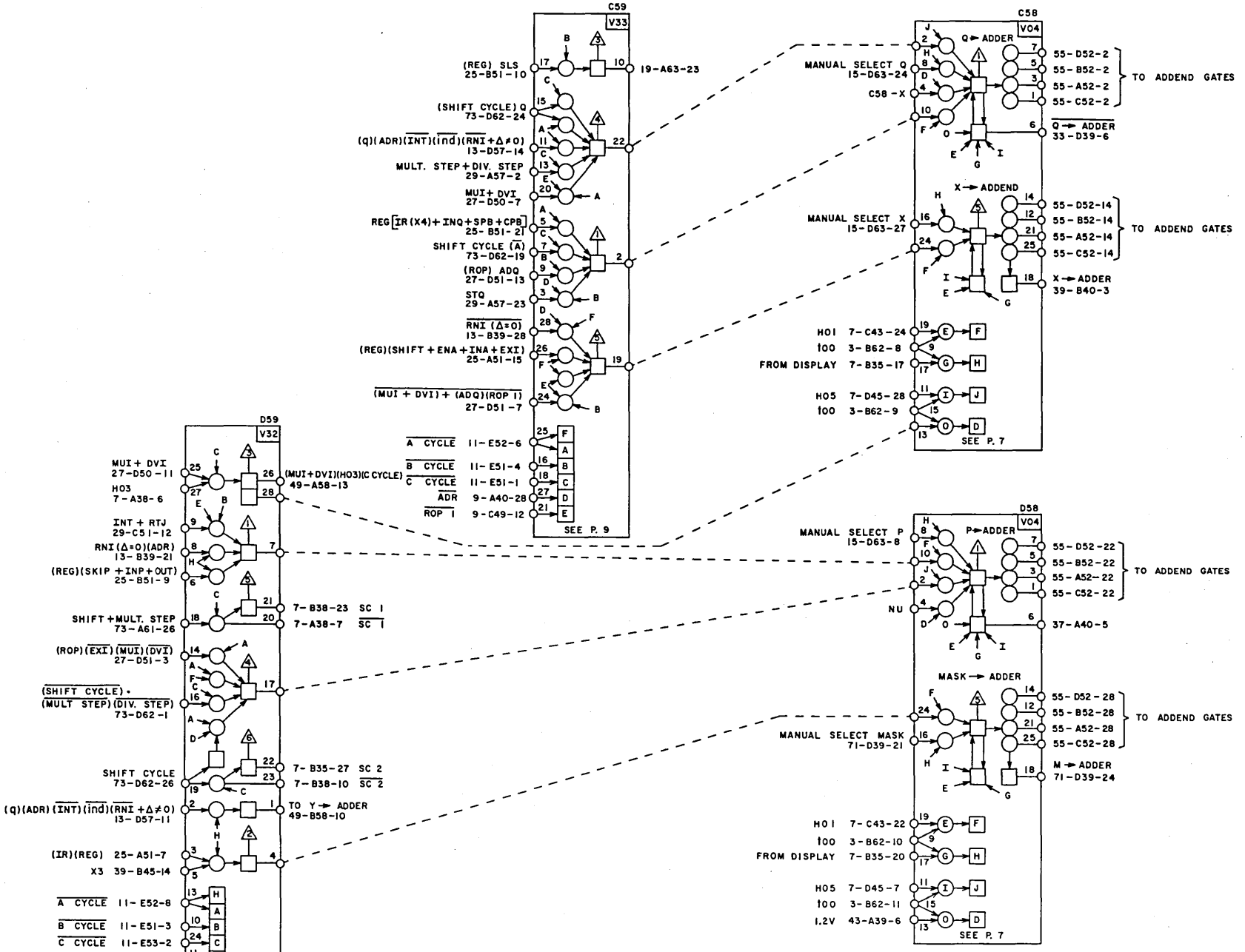
P → ADDER

The setting of the P → Adder FF transfers the current program address in P to the adder for modification. In most cases, a +1 is added to P to obtain the address of the next sequential instruction. Thus, at V300 of the A cycle in the ROP mode of all instructions except EXI, MUI, or DVI, the P → Adder FF is set simultaneously with the +1 → Adder (augend gates) which adds +1 to P.

The V300 pulse sets the P → Adder FF in the A cycle of the STO mode of every applicable instruction. The P → Adder FF is also set at the V300 time of the A cycle in the REG mode of every applicable instruction except during Shift Cycle operations.

MASK → ADDER

The Mask → Adder FF is set at V100 time of the A cycle only on IR instructions when bit 3 of the X register is set (Mask is origin register). In this case, the contents of the Mask register transfers to the addend gates of the adder for subsequent transfer to the selected destination register.


C59
V33
(REG) SLS 25-B51-10
19-A63-23
(SHIFT CYCLE) Q 73-D62-24
(q)(ADR)(INT)(ind)(RNI+Δ≠0) 13-D57-14
MULT. STEP+DIV. STEP 29-A57-2
MUI+DVI 27-D50-7
REG[IR(X4)+INQ+SPB+CPB] 25-B51-21
SHIFT CYCLE (A) 73-D62-19
(ROP) ADQ 27-D51-13
STQ 29-A57-23
RNI (Δ=0) 13-B39-28
(REG)(SHIFT+ENA+INA+EXI) 25-A51-15
(MUI+DVI)+(ADQ)(ROP 1) 27-D51-7
A CYCLE 11-E52-6
B CYCLE 11-E51-4
C CYCLE 11-E51-1
ADR 9-A40-28
ROP 1 9-C49-12
SEE P. 9
C58
V04
Q→ADDER
MANUAL SELECT Q 15-D63-24
C58-X
55-D52-2
55-B52-2
55-A52-2
55-C52-2
TO ADDEND GATES
Q→ADDER 33-D39-6
X→ADDEND
MANUAL SELECT X 15-D63-27
55-D52-14
55-B52-14
55-A52-14
55-C52-14
TO ADDEND GATES
X→ADDER 39-B40-3
H01 7-C43-24
100 3-B62-8
FROM DISPLAY 7-B35-17
H05 7-D45-28
100 3-B62-9
SEE P. 7
D59
V32
MUI+DVI 27-D50-11
H03 7-A38-6
(MUI+DVI)(H03)(C CYCLE) 49-A58-13
INT+RTJ 29-C51-12
RNI(Δ=0)(ADR) 13-B39-21
(REG)(SKIP+INP+OUT) 25-B51-9
SHIFT+MULT. STEP 73-A61-26
7-B38-23 SC 1
7-A38-7 SC 1
(ROP)(EXI)(MUI)(DVI) 27-D51-3
(SHIFT CYCLE)·(MULT STEP)(DIV. STEP) 73-D62-1
SHIFT CYCLE 73-D62-26
7-B35-27 SC 2
7-B38-10 SC 2
(q)(ADR)(INT)(ind)(RNI+Δ≠0) 13-D57-11
TO Y→ADDER 49-B58-10
(IR)(REG) 25-A51-7
X3 39-B45-14
A CYCLE 11-E52-8
B CYCLE 11-E51-3
C CYCLE 11-E53-2
REG 9-C39-7
ADR 9-A40-27
STO 1 9-C59-6
D58
V04
P→ADDER
MANUAL SELECT P 15-D63-8
55-D52-22
55-B52-22
55-A52-22
55-C52-22
TO ADDEND GATES
NU
37-A40-5
MASK→ADDER
MANUAL SELECT MASK 71-D39-21
55-D52-28
55-B52-28
55-A52-28
55-C52-28
TO ADDEND GATES
M→ADDER 71-D39-24
H01 7-C43-22
100 3-B62-10
FROM DISPLAY 7-B35-20
H05 7-D45-7
100 3-B62-11
1.2V 43-A39-6
SEE P. 7
CONTROL DATA CORPORATION
COMPUTER DIVISION
TITLE
ADDER GATE CONTROLS (ADDEND)
PRODUCT 1704
SIZE C
DRAWING NO. 60152700
REV Y
SHEET
PAGE 51

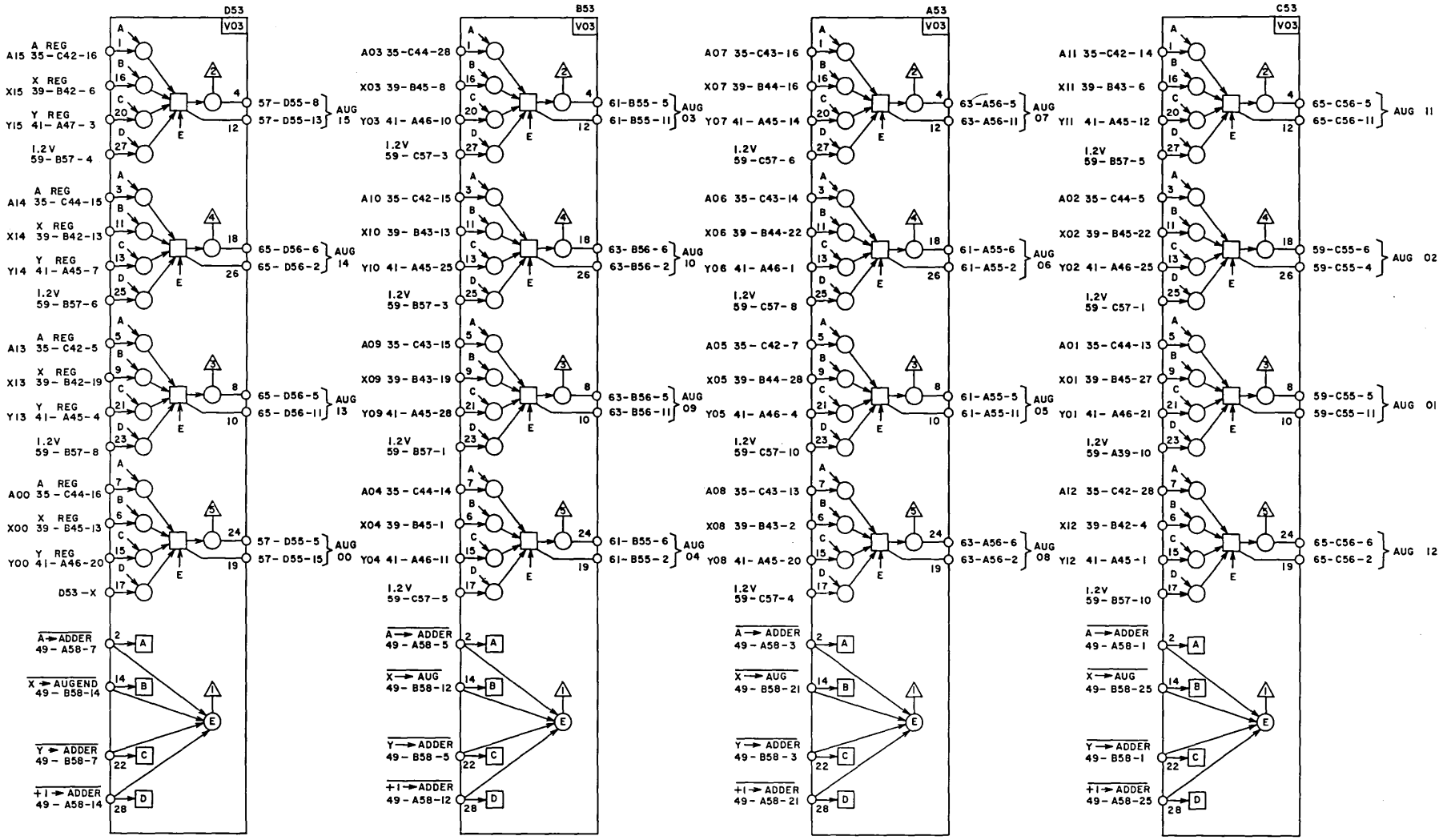
ADDER/SHIFTER FAN-IN GATES (AUG)

The augend (AUG) gates of the Adder/Shifter receives enables from the augend adder gate controls which enable the inputs from the corresponding register. Thus if the X → Augend FF on the augend gate control module is set, the $\overline{\text{X} \rightarrow \text{Augend}}$ input to each of the AUG gates becomes a "0". The resulting "1" output from inverter A enables the inputs from the X register into the corresponding inverters on the AUG gate modules.

The AUG gates are contained on four V03 modules. The bit positions on each module are divided in pairs according to the chassis locations of the V03 module and the adder/shifter module to which they connect. For example, bit positions 1 and 2 are on the V03 module at location C53. Bit positions 1 and 2 for the Adder/Shifter are on the V00 module at location C55. This system is used to reduce the lengths of the connecting wires between the two modules to a minimum.

Each bit position on the V03 modules consists of four input inverters and a True and Not output inverter. When one of the enables from the augend gate controls in a "0", the corresponding inverter (A, B, C, or D) enables the corresponding bit position inputs. The "1" inputs from the selected register produce "1" outputs on the AUG— lines and "0" outputs on the $\overline{\text{AUG}}$— lines. If none of the enables is a "0" indicating that no input is selected for the augend gates, inverter E produces a "0" output. All the AUG— outputs now become "1's" whenever no input is selected for the AUG gates.

In the case of a +1 → Adder selection, inverter D enables a GND ("1") input to bit position 0 and 1.2v ("0") inputs to the remaining bit positions. Thus, the Adder/Shifter receives a +1 input from the AUG gates.

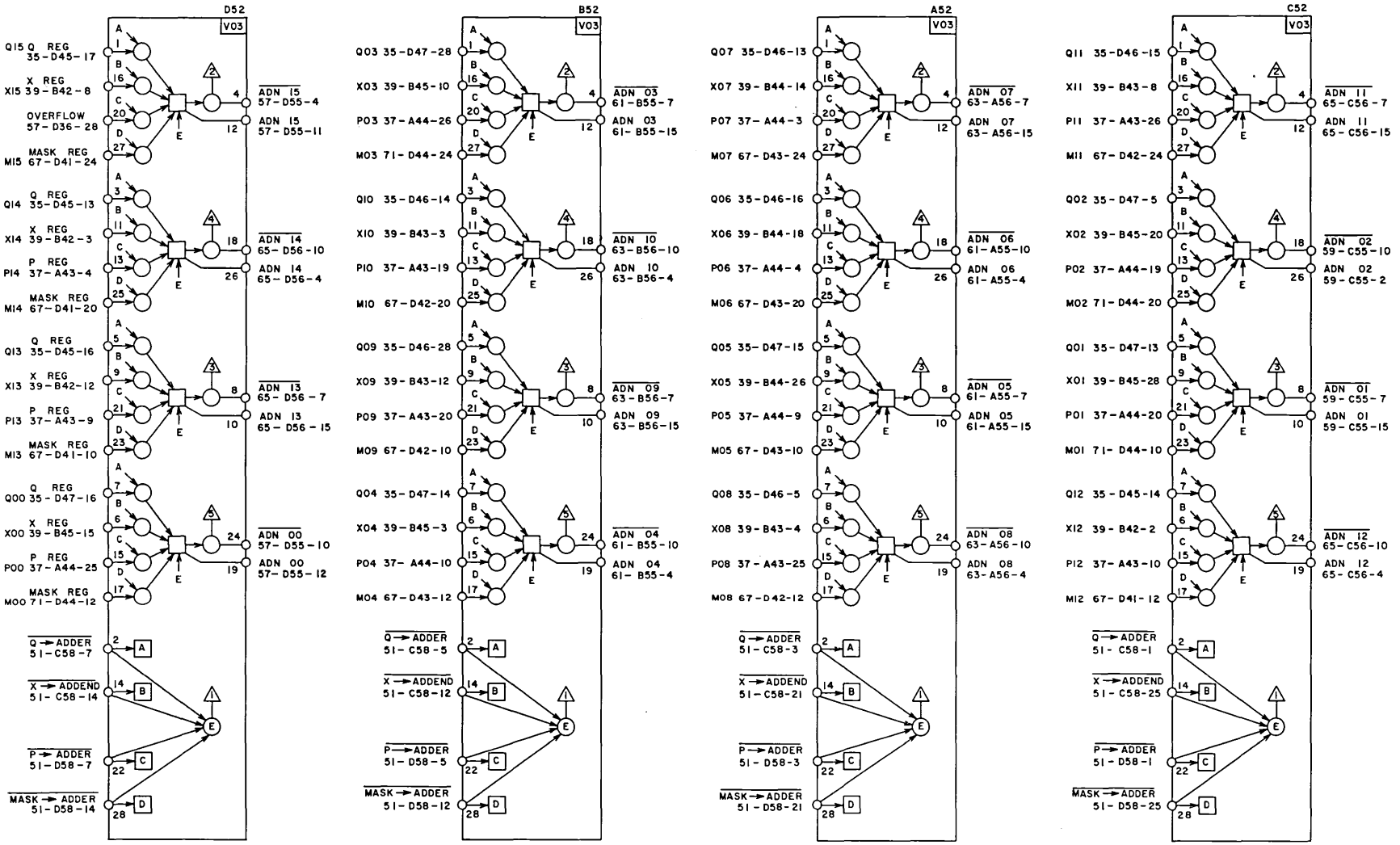


CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE ADDER SHIFTER FAN-IN AUGEND (AUG) GATES	PRODUCT 1704	
		SIZE C	DRAWING NO. 60152700 REV S
			SHEET PAGE 53

ADDER/SHIFTER FAN-IN GATES (ADN)

The addend (ADN) Adder/Shifter fan-in gates receive enables from the addend adder gate controls which enable inputs from the corresponding register. If a particular Addend Adder Control FF is set, the enable to the ADN gates becomes a "0". The output of the corresponding inverter (A, B, C, or D) enables the input from the selected register into the ADN gates. The True and Not outputs of the ADN gates connect to the Adder/Shifter modules.

The ADN gates function in the same manner as the AUG gates as described on page 53.



CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE
ADDER SHIFTER FAN-IN
ADDEND (ADN) GATES

PRODUCT 1704
SIZE C | DRAWING NO. 60152700 | REV P
SHEET 55

ADDER LOGIC

The adder portion of group 0 is contained on the V60 module. The adder logic functions on this module in an identical manner to the equivalent logic on the other groups of the adder (page 59). However, in place of the group borrow input, the V60 module receives the $\overline{\text{Section 1 Borrow}}$ + $\overline{\text{(Section 0 Borrow) (Section 1 Enable)}}$ conditions. Thus, group 0 of the adder receives a group borrow input from a Section 1 Borrow or from a Section 0 Borrow and a Section 1 Enable.

End Around Borrow (EAB)

A stage 15 borrow (H) or a stage 15 enable (E15) and a group borrow input corresponds to an EAB condition. In the V60 module, the EAB functions the same as a stage borrow in the other modules since stage 0 is contained on the same module.

OVERFLOW

The V60 module detects the Adder Overflow condition. The Adder Overflow occurs when the result of an arithmetic operation exceeds the modulus of the adder in the ones complement system. An overflow can occur in the positive or negative direction. The overflow condition can also be expressed logically as follows:

Overflow = (S15B) (Bit 15="1") + (Bit 15="0") (S15S)

S15B - Stage 15 borrow

S15S - Stage 15 satisfy

The first two terms correspond to a positive overflow and the second two to a negative overflow. Simplified examples of both types are as follows.

3210	Bit Positions
0111	Augend ($+7_8$)
0111	Addend ($+7_8$)
1111	Stage Difference
1110	Borrow Corrected Difference (-1)
EAB	

Positive Overflow

3210	Bit Position
1000	Augend (-7_8)
1000	Addend (-7_8)
1111	Stage Difference
0<-0<-0<-1	Borrow Corrected Difference (+1)

Negative Overflow

In the first example, the sum of the two positive numbers exceeds the modulus of the simplified adder. This condition corresponds to the first two terms in the logical equation above. Thus, the detection of an EAB and a "1" in stage 15 of the sum denotes a positive overflow.

The second example shows a negative overflow. In this example, the sum of two negative numbers exceeds the modulus of the simplified adders. A negative overflow is detected when bit 15 is a "0" (positive result) and bit 15 of the augend and addend produce a satisfied condition.

The detection of an overflow on the V60 module produces a "0" output on pin 27. The enabling of either the two main input gates sets the Overflow FF (H) on the V58 module. For example, V275 (H005 and t75) sets H on the B cycle during the ROP mode on an ADD instruction if an overflow is detected.

In an Inter Register instruction, the setting of bits 6 or 7 (X_6 or X_7) of the instruction code denoting an Exclusive Or or Logical Product disables the setting of H. Thus, the setting of H is disabled unless the overflow resulted from an arithmetic Add or Subtract operation.

An overflow can also result from a divide instruction. In this case, an overflow results when the quotient in the A-register becomes negative at the completion of the Divide operation ($\overline{\text{Divide Step}}$). An overflow during a Divide instruction occurs when the answer exceeds the modulus of the 16-bit register.

The Overflow FF is also set at V275 time of the A cycle during an Exit Interrupt (EXI) instruction if bit 15 of the word read from storage (containing the return address) is a "1". A "1" in this position denotes the Overflow FF was initially set at the time the interrupt occurred. If X_{15} is a "0" at this time, H is cleared.

In an Interrupt operation (INT), the state of the Overflow FF transfers to bit 15 of the addend gates. The P → Adder command is also enabled at this time. Since the P register now contains the return address for the EXI instruction, the state of the Overflow FF is combined with the return address.

The Sense Overflow command during a Skip instruction clears H at V275 of the A- cycle. The setting of the Overflow FF also lights the Overflow Fault indicator during the Display mode.

SHIFTING OPERATIONS

Shifting operations for group 0 of the adder take place on the V61 module. Left or right short shifts take place in the same manner as in the other groups of the adder. In the case of left shifts, which are always end-around, bit 15 transfers from pin 21 to the V60 module to pin 14 of the V61 module. The LS enable shifts bit 15 to the bit 0 output. Bit 0 transfers from pin 16 of the V60 module to the group 1 V00 module (page 59). The LS enable shifts bit 0 to the bit 1 output.

All right shifts (RS) are end-off. Thus, bit 1 shifts to the bit 0 output of the V61 module. The bit 0 output is not used in RS operations. Bit 15 transfers from pin 23 of the V60 module to the group 7 V00 module (page 65). The RS enable shifts bit 15 to the bit 14 output. Since it is assumed that the LRS2 and MUI controls are not enabled in this case, bit 15 transfers to the bit 15 output of the V61 module, extending the sign.

Long Shift

A long shift takes place when both bits 5 and 6 of the Shift instruction are "1", indicating that both A and Q are to be shifted. A long shift also takes place for each iteration of a Multiply or Divide instruction. In any of these instructions, V125 (t25 and H02) sets the Long Shift FF. The setting of the Long Shift FF enables a LLS2 or LRS2 operation depending on whether a left or right shift is selected.

Long Left Shift (LLS): The LLS operation takes place in two steps: LLS1 and LLS2. The LLS1 operation is enabled by the following conditions:

$$\text{LLS1} = (\text{MUI} + \text{DVI} + \text{Shift QA})\ (\overline{\text{Long Shift}})\ (\text{LS})$$

Thus, LLS1 takes place before the setting of the Long Shift FF, which enables LLS2.

In a typical LLS operation (fig. 1, page 56.2), Q is shifted first followed by the shift of A. In the shift of Q, LLS1 enables the shift of bit 15 of A directly to the output of bit 0 of Q on the V61 module. At V100 time (t00 and H01), Q15 transfers from the V60 module to set the Bit Bucket FF. The Bit Bucket FF retains the state of Q15 until the shift of A. At V125 time, the Long Shift FF is set which disables LLS1 and enables LLS2. The LLS2 enables the shift of the bit bucket to bit 0 of the shifted A output.

During Divide Step operations, the detection of the $\overline{\text{EAB}}$ condition which indicates that (Q) $\geq$ (X) sets the bit bucket at V100 time. The contents of the bit bucket is shifted to bit 0 of the shifted A output.

Long Right Shift (LRS): The setting of the Long Shift FF enables LRS2. The LRS2 output enables the shift of the state of the bit bucket to the bit 15 output of A.

During (QA) or MUI operations, bit 0 of Q transfers to the bit bucket on the shift of Q. Bit 0 subsequently shifts from the bit bucket to bit 15 of the A output. Fig. 2, page 56.2, shows a simplified illustration of a LRS operation.

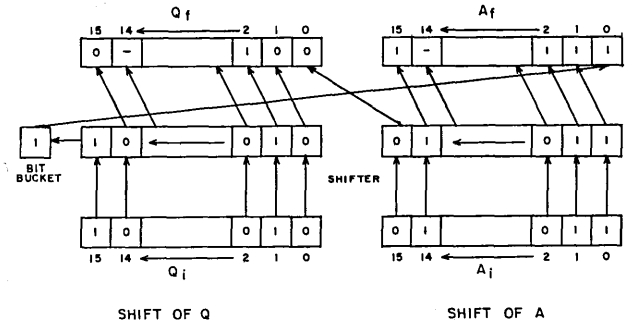


Fig. 1 -- Simplified Example Of LLS.

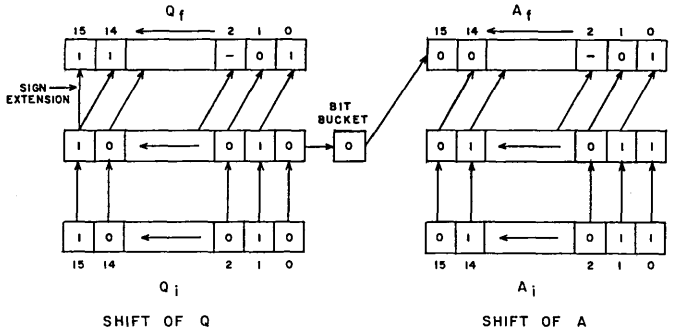
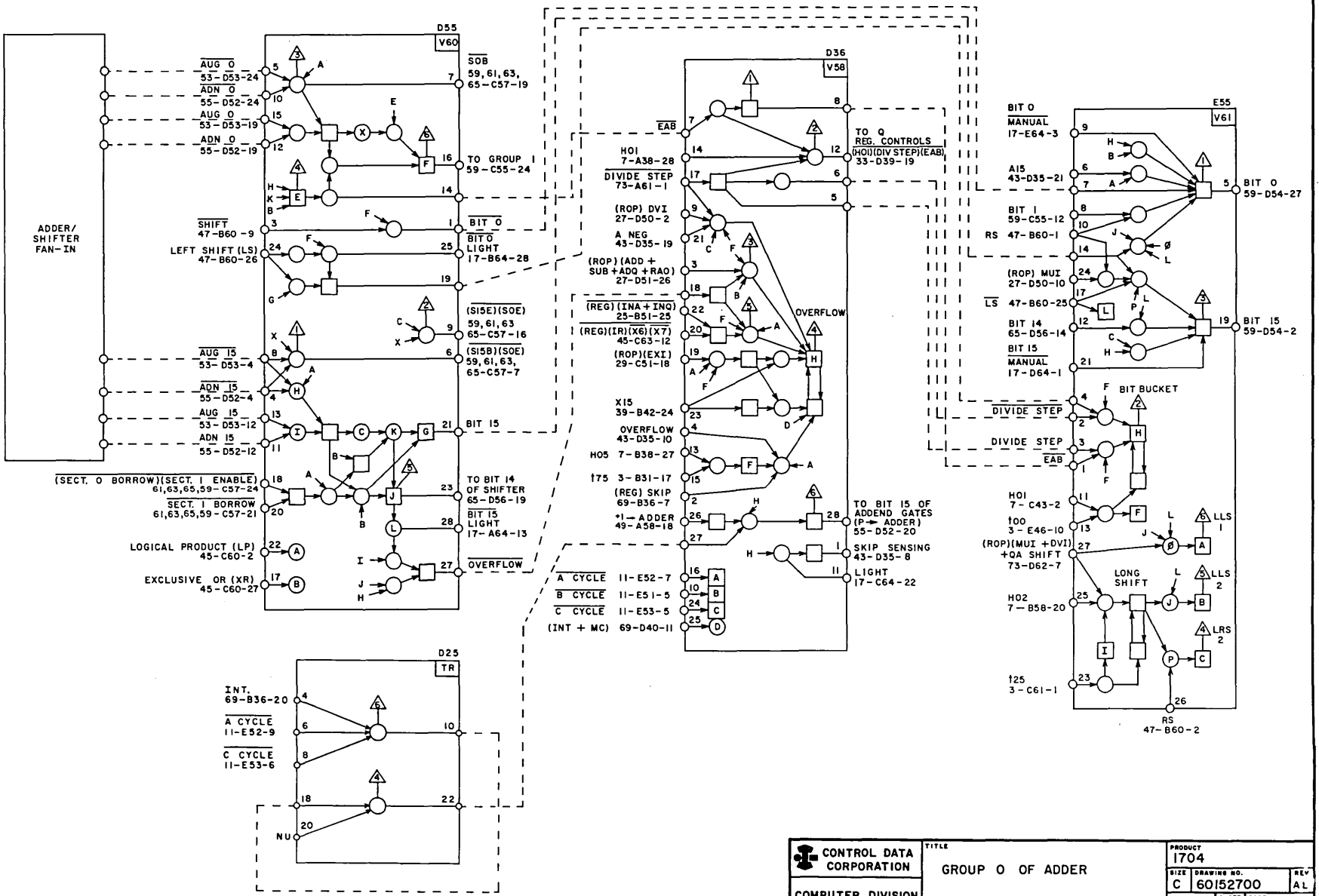


Fig. 2 -- Simplified Example Of LRS.



CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE: GROUP 0 OF ADDER	PRODUCT: 1704	
		SIZE: C	DRAWING NO.: 60152700 REV: AL
			SHEET: PAGE: 57

The block diagram in Figure 1 to the right shows that the Adder/Shifter circuit is divided into three main divisions:

1) Adder/Shifter modules (V00) - perform stage borrow and enable, shifting, Exclusive OR, and Logical Product functions.
2) Borrow Look - Ahead modules (V10) sense stage borrow and enable conditions. The V10 modules produce group borrow and section borrow and enable conditions.
3) Fan-out modules (V06) provide the required number of outputs from the Adder/Shifter to the registers indicated.

ADDER PYRAMID

One of the main functions of the Adder/Shifter is the adding operation. The adder is divided into eight groups. Each group is contained on a V00 module. All groups except group 0 are logically identical. Thus, the following description is based on the operation of a typical group of the adder (group 1). The basic logical operation of group 0 is similar to the other groups. However, this group contains some additional features and is described separately on page 56.1.

STAGE BORROWS AND ENABLES

Figure 3 shows that each group operates on two adjacent bits of the addend and augend. (Bits 0 and 15 are considered adjacent bits in the adder pyramid.) Thus, group 1 compares bits 1 and 2 of the augend and addend.

The adder pyramid uses a subtractive pyramid circuit to perform the Add function: AUG - (-ADN) = AUG + ADN = SUM. The principles of a subtractive pyramid are shown in Figure 4.

A stage borrow results whenever a "1" is subtracted from a "0". Thus, in Figure 4, the borrow generated in stage 0 propagates to stage 1 where it is satisfied. Enables result when a "1" is subtracted from a "1" or a "0" from a "0". Enables propagate borrows but are toggled as a borrow passes through as shown in Figure 5.

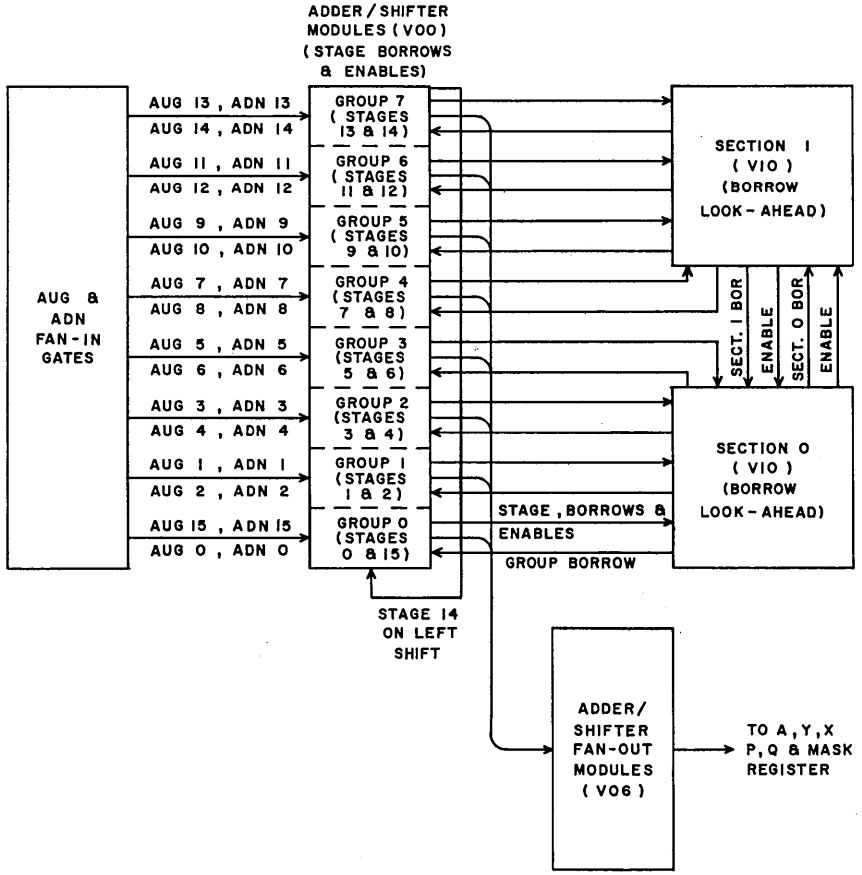


Figure 3. Adder/Shifter Block Diagram

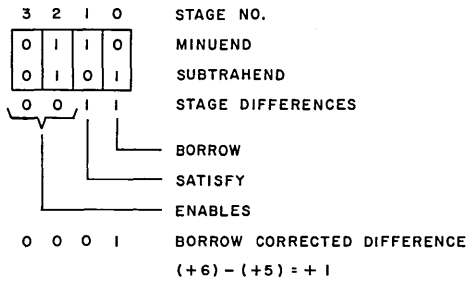


Figure 4. Principles of a Subtractive Pyramid

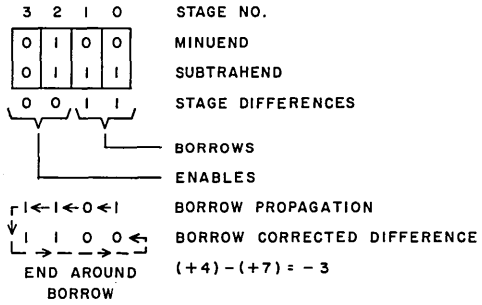


Figure 5. Example of Borrow Propagation

Figure 5 shows that the borrow generated in stage 0 propagates to stage 1 which it toggles. Stage 1 also generates a borrow which propagates through enables at stages 2 and 3 which are toggled. The end-around borrow toggles the stage 0 difference which produces the final difference.

Since the output of the subtractive pyramid is a sum, the ADN inputs are complimented in the stage comparisons according to the principles shown in Figure 6.

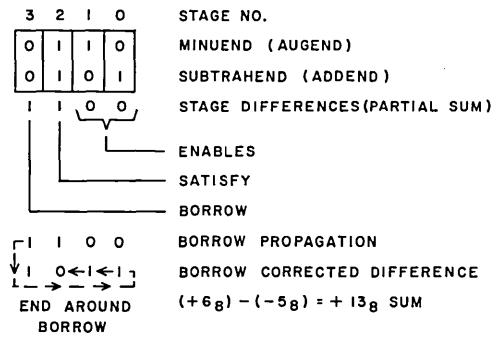


Figure 6. Principles of the Adder Pyramid

Because the addend bits are complimented in the bit comparisons, Figure 6 shows that a "1" subtracted from a "0" or a "0" from a "1" produces an enable. The subtraction of a "1" from a "1" results in a satisfy while the subtraction of a "0" from a "0" produces a borrow. All other logical conditions for a subtractive pyramid apply to the adder. The example in Figure 6 shows the final sum of $+13_8$ for the quantities used.

The stage borrow and enable conditions are sensed at the input inverters on the V00 modules. The enable for stage 1 (SIE) is defined by the following logical equation: $SIE = \left[(AUG\ 1)\ (\overline{ADN\ 1}) + (ADN\ 1)\ (\overline{AUG\ 1})\right]\ (\overline{LP})$

If the $\overline{LP}$ term is disregarded in this case, the SIE condition is sensed when the corresponding bits in the augend and addend are unlike. This logical arrangement corresponds to the example in Figure 6.

The stage 1 borrow (S_1B) is defined by the following equation:

$$S_1B = (\overline{AUG\ 1})\ (\overline{ADN\ 1})\ (\overline{LP})$$

Disregarding the $\overline{LP}$ term, a stage borrow results when corresponding bits in the augend and addend are both "0's", which also corresponds to Figure 6. The stage borrow and enable conditions are sensed in the same manner on all V00 modules.

Borrow Propagation

The propagation of borrows in the V00 modules takes place in the following three ways:

1) Borrows generated by the low-order adjacent stage within a group.
2) Borrows generated by the high-order stage within a group (group borrow).
3) Borrows generated by the adjacent lower-order group.

A case 1 borrow propagates directly to the adjacent stage in the group, regardless of the group borrow input to the generating stage. For example, assume a borrow input to stage 1 of group 1 exists. Inverter * produces a "0" output which propagates the borrow directly to stage 2 through the interconnecting inverter, regardless of the group 0 borrow input.

Case 2 borrows are transmitted to the group borrow logic on the corresponding V10 module through pin 8 on the V00 module. For example, assume a borrow input to stage 2 of group 1. The $\overline{S_2B}$ output on pin 8 becomes a "0", indicating a stage 2 borrow. The S_2B condition corresponds to a group 1 borrow which is described in more detail in a subsequent paragraph.

The case 3 borrows probe the enable condition of the low-order stage in a group. If an enable exists in that stage, the output of that stage becomes a "1" (toggled) and the borrow is propagated to the adjacent stage in the group. For example, assume a group 0 borrow input to group 1. The group 0 borrow input probes the output of inverter E_1 through the interconnecting inverters. If an enable exists in stage 1, E_1 produces a "1" output and the group 0 borrow propagates to stage 2 where it probes the E_2 output. If the group borrow probe detects an enable in a stage, it forces the output of that stage to a "1" corresponding to the toggling of the "0" output in the partial sum.

GROUP BORROWS

Each group produces three outputs to the corresponding section (V10) module. These outputs determine whether a borrow is generated by the corresponding group. For example, group 1 produces the $\overline{S_2B}$, $\overline{(S_1B)\ (S_2E)}$ and $\overline{(S_1E)\ (S_2E)}$ conditions from pins 8, 1, and 3 respectively.

The corresponding V10 module generates group borrow, section borrow, and section enable outputs according to the enable and borrow condition of the groups in that section. The section 0 module, for example, generates group borrows for groups 0, 1, 2 and 3. The group 3 borrow corresponds to the section 0 borrow. The following logical equations represent the group borrow function for a typical group (group 1) in section 0.

Group 1 Borrow = $\overline{[S2B + (S1B)\ (S2E)]} + \overline{[(S1E)\ (S2E)\ (S0B) + (S1E)\ (S2E)\ (S0E)\ (S15B)]} + \overline{[(S15E)\ (S0E)\ (S1E)\ (S2E)\ (J)]}$

J (Section 0 Borrow Input) = Section 1 Borrow + (Section 1 Enable) (Section 0 Borrow)

The equations above show that in general a group borrow results when any of the following conditions are present:

1) The higher-order stage in the group generates a borrow.
2) The higher-order stage in the group produces an enable and the lower order stage in the group generates a borrow.
3) A stage in a lower-order group generates a borrow and all higher-order stages in all groups up to and including the generating group produce enables. This condition is represented by the third term in the group 1 borrow equation.

The group borrow outputs go to the next higher-order group.

SECTION BORROWS

The section borrows are generated on a V10 module when a borrow propagates through all the groups in a section. For example, the borrow can either originate in section 0 or originate in section 1 and propagate through section 0.

Section borrows are generated under the same conditions as a group borrow. Thus, the section borrow can also be termed the group 3 borrow because group 3 is the highest order group in section 0. Figure 7 shows a simplified example of a section borrow.

In Figure 7, the borrow originates in group 3 and propagates to section 1 as the section 0 borrow. Since all the groups in section 1 generate enables, the borrow propagates through section 1. The combination of a section 1 enable and section 0 borrow enters a borrow input to section 0.

SECTION ENABLES

Each section generates a section enable when all the groups in the section produce enables. In Figure 7, section 1 generates an enable because groups 4-7 all produce enables.

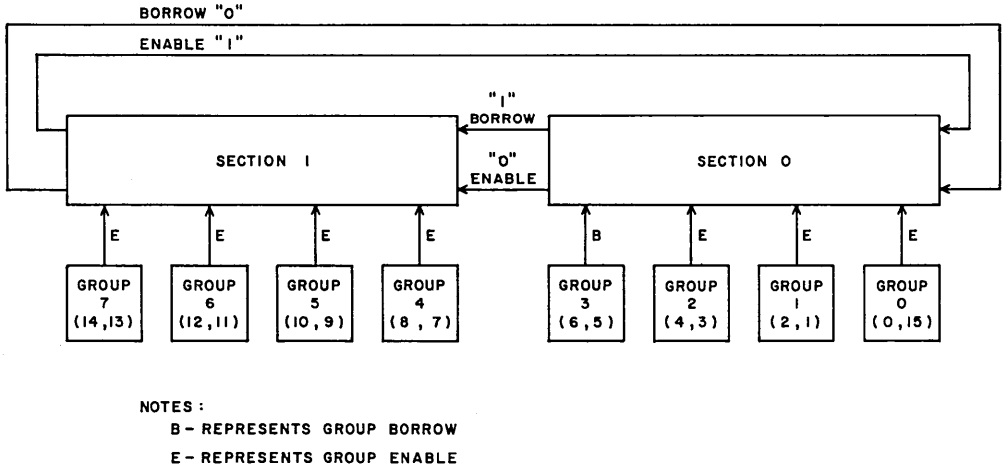


Figure 7. Simplified Section Borrow

ADDER OUTPUTS

The output of the B-inverters on the V00 modules represents the output of the corresponding stage of the Adder. For example, B_1 on the group 1 module represents the output of stage 1 of the Adder. The Adder outputs connect to the Shifter circuit, to the corresponding indicator light and to the fan-out module. The logical equation below represents the conditions for a typical Adder output.

$$B_1 = (E_1)\,(\text{Group 0 Borrow})\,(\overline{LP}) + (E_1)\,(XR) + (\overline{XR})\,(LP)\,(\text{AUG 1})\,(\text{ADN 1}) + (\overline{XR})\,(\overline{\text{Group 0 Borrow}})\,(\overline{LP})\,(\overline{\text{AUG 1}})\,(\overline{\text{ADN 1}})$$

By assuming $(\overline{LP})\,(\overline{XR})$ conditions, the above equation becomes:

$$B_1 = (E_1)\,(\text{Group 0 Borrow}) + (\overline{\text{Group 0 Borrow}})\,(\overline{\text{AUG 1}})\,(\overline{\text{ADN 1}})$$

Thus, stage 1 of the Adder produces a "1" output with a stage 1 enable and a group 0 borrow or a stage 1 borrow and no group 0 borrow. In all other borrow and enable conditions, B_1 produces a "0" output. With the exception of Shift operations, B_1 represents the output of stage 1 of the Adder/Shifter.

LOGICAL PRODUCT

The Adder/Shifter modules also perform Logical Product (LP) operations. The LP function produces a "1" output from a stage of the Adder that corresponds to "1's" in the same bit position of the addend and augend as shown by the simplified example below.

15	3 2 1 0	Bit Positions
0 - - - -	1 0 1 0	Augend
0 - - - -	1 1 0 0	Addend
0 - - - -	1 0 0 0	Result

Setting the LP Control FF enables the input to each V00 module. Assuming an (LP) $(\overline{XR})$ condition, the output of inverter A blocks all inputs to B_1 except the input corresponding to the third term in the equation for B_1 above. Thus, B_1 produces a "1" output on an LP operation when stage 1 of the augend and addend both contain "1's".

EXCLUSIVE OR

The Adder/Shifter modules perform Exclusive OR (XR) functions. The XR function produces a "1" output from a stage of the Adder that corresponds to

a "1" in the same stage of the addend or augend but not both as shown below:

15 - - - - 3 2 1 0	Bit Positions
0 - - - - 1 0 1 0	Augend
0 - - - - 1 1 0 0	Addend
0 - - - - 0 1 1 0	Result

The setting of the XR Control FF enables the XR input to all V00 modules. Assuming the (XR) ($\overline{LP}$) condition, the "0" output of inverter B blocks all inputs to B_1 except the (E_1) (XR) term. Since the E_1 output represents an enable condition (the bits in stage 1 of the addend and augend are different), B_1 produces a "1" output.

SHIFT CIRCUIT

In a Shift operation, the operand in the A or Q register is shifted a specified number of positions left or right. The bits in the designated register are shifted one position each time the operand is transmitted through the Adder/Shifter. In (QA) Long Shift operations, the operands in the A and Q register are shifted separately in the Shift circuit for each shift cycle.

The shifting operation takes place on the V00 modules at the output of the Adder. Thus, the outputs of the B-inverters are shifted left or right one position.

The setting of the LS or RS Control FFs transmits a "0" to the $\overline{Shift}$ input to each Adder/Shifter module. This input disables the normal output of the B-inverters. Thus, the LS or RS paths determine the output of each stage of the Adder/Shifter modules.

In a shifting operation, the LP FF is set coincident with the $\overline{Shift}$ and LS or RS enables. As a result, the LP input enables an LP operation in the Adder at the same time as the shift. The operand is gated into the augend or addend gates, and the gates not selected receive an input of all "1's". The output of the B inverters represents the operand.

LEFT SHIFT

The Left Shift takes place on the Adder/Shifter modules when the LS Control FF is set. The LS enable enters each Adder/Shifter module. Since the $\overline{Shift}$ enable blocks the normal output of the B-inverters, the outputs of these inverters are enabled by the LS input. Thus, the B outputs, which represent the bits of the operand, appear as outputs shifted one position to the left.

All Left Shifts are end-around. Thus, on a Long Left Shift (LLS), the bit in stage 15 of Q shifts to stage 0 of A. The LLS function is described in more detail in the Adder Group 0 section (page 57). In the Short Left Shifts, bit 15 shifts to bit 0. The simplified illustration in Figure 8 shows an example of a Left Shift operation of (A).

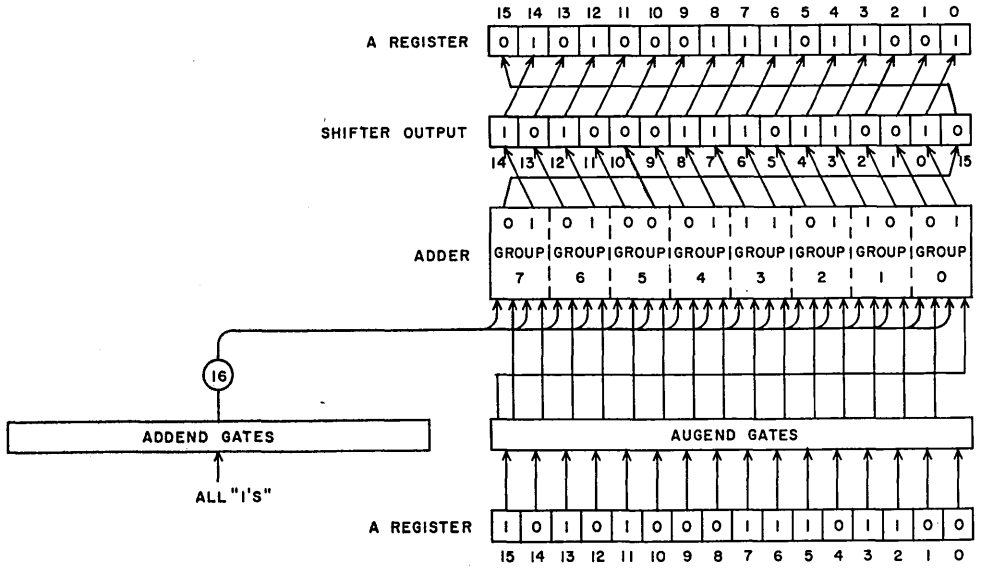


Figure 8. Example of an (A) Left Shift

Figure 8 shows the bit positions of the Adder outputs relative to their positions in the groups. For example, the stage 0 output is shown adjacent to the stage 15 output in group 0. The shift of the low-order stage of a group to the high-order stage takes place on the corresponding V00 module. The output of the high-order stage on a group transfers to the output of the low-order stage on the adjacent high-order group.

RIGHT SHIFT

The setting of the RS Control FF enables the RS input to each Adder/Shifter module. The $\overline{\text{Shift}}$ input disables the normal Adder output. Thus, the RS enable shifts the output of the B&C-inverters one-position to the right. All right shifts are end-off. Thus, the bit in stage 0 is lost. The sign bit (stage 15) is extended. If the sign bit is initially negative ("1"), the stage 15 output remains a "1" for each shift as the other bits shift to the right.

MANUAL SET AND DISPLAY

The Adder/Shifter modules serve as the means of manually setting and displaying the output bits of the selected register. Each manual set switch on the console connects to the corresponding output stage of the Adder/Shifter modules. Pressing the manual set switch during the Display mode enters a "0" into the output inverter on the V00 module. The output becomes a "1".

The output of the selected register enters the Adder/Shifter modules through the addend or augend gates. The gates not selected receive an input of all "1's". In the Display mode, the LP FF is also set. Thus, a Logical Product operation takes place between the selected register and all "1's". The contents of the selected register are displayed on the indicator lights connected to the output of each stage of the Adder/Shifter. The Manual Controls (see display example, page 21) describes the manual set and display operation in more detail.

FAN-OUT MODULES

The output stages of the Adder/Shifter connect to the output registers (A, Y, X, etc.) through fan-outs on the V06 modules. Each fan-out produces six outputs, required by the number of registers that connect to the Adder/Shifter.

ADDER/SHIFTER TIMING

The Adder/Shifter operates in a static mode. Thus, the input is gated into the Adder at a timed period and the output is gated at a timed period. In all operations except short cycles (SC) the output of the Adder is gated into the enabled register 200 nsec after the input was enabled. This delay allows sufficient time for the Adder circuit to stabilize.

In most cases, the enabled input is gated to the Adder at the same time as the output of the Adder is gated to the enabled register. The input data does not interfere with the output since the minimum path through the Adder of eight inversions (including fan-out) is a sufficient delay.

Figure 9 shows the Adder timing sequence for an Add to A (ADD) instruction. In this instruction, an operand is read from storage and is transferred to the X register from where it is added to the contents of the A register. The example shows only those commands that apply to the Adder.

In the first Adder cycle (A cycle), the operand in the X register is gated to the addend gates at 100 time. However, the output is not used. At 300 time, (P) and +1 are combined in the Adder to give the address of the next instruction. At 50 time of the B cycle, storage is requested which initiates the reading of the next instruction. At 100 time (P+1) transfers from the Adder to Y and P at the same time (X) and (A) are transferred to the addend and augend gates respectively. The output sum (A + X) transfers to the A register at 300 time.

SHORT CYCLE (SC) OPERATIONS

During SC operations, as in Shift and Multiply instructions, the output of the Shifter is gated 100 nsec after the gating of the selected input. A delay of 100 nsec is sufficient for these operations since the full Adder circuit is not used. Figure 10 shows the Adder timing sequence in a Shift (A) instruction for a portion of one C cycle.

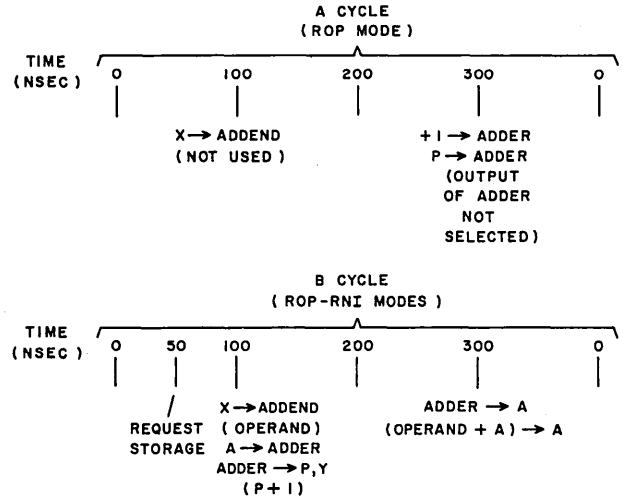


Figure 9. Example of Adder Timing Sequence in a Normal Cycle

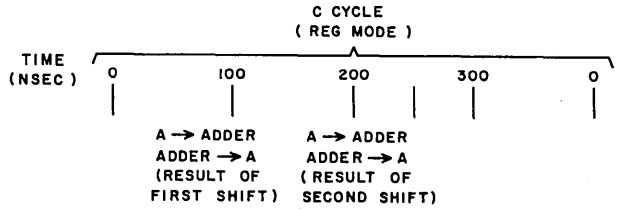
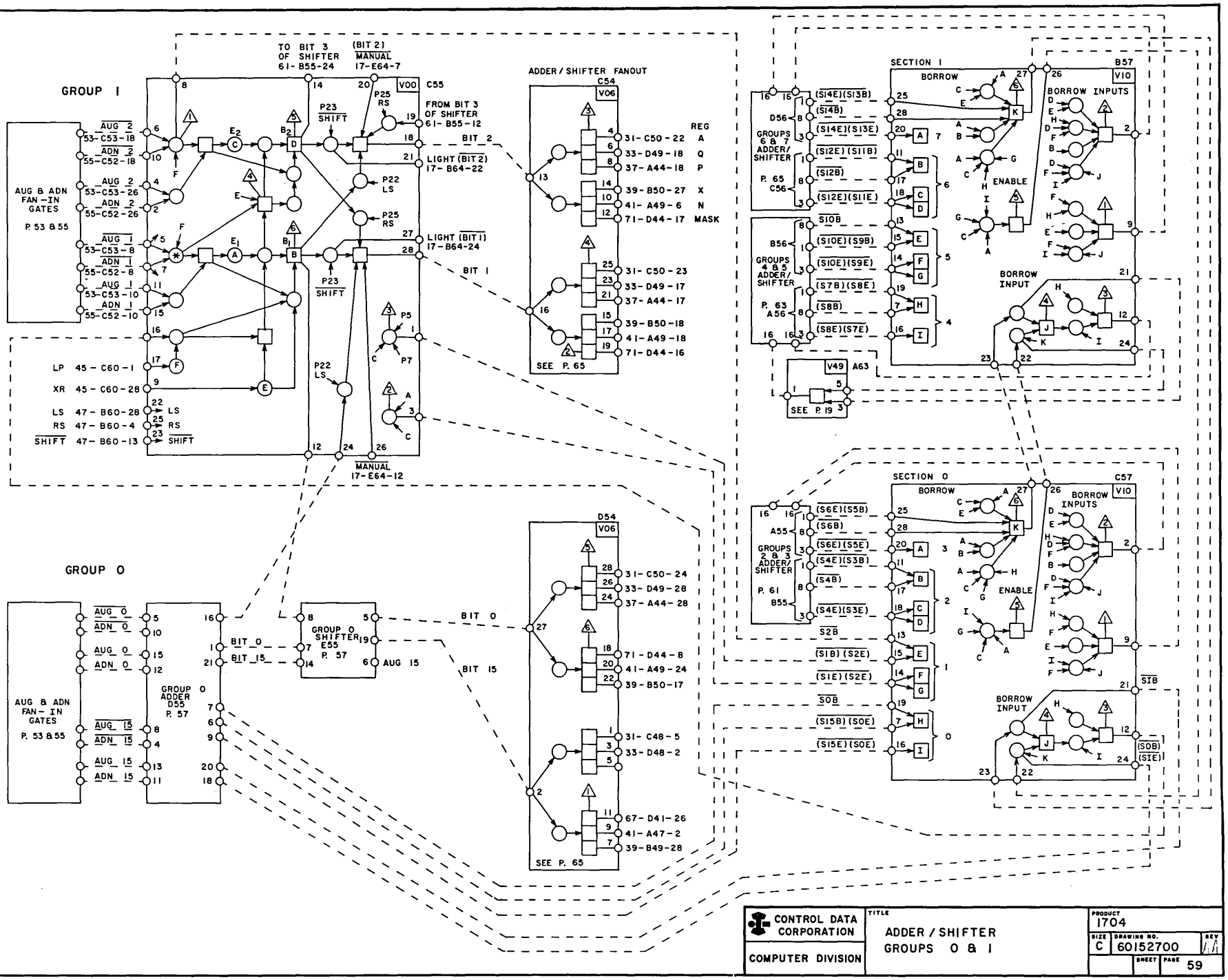


Figure 10. Example of Adder Timing Sequence in a Short Cycle



CONTROL DATA CORPORATION	TITLE: ADDER / SHIFTER GROUPS 0 & 1	PRODUCT 1704	
COMPUTER DIVISION		SIZE C · DRAWING NO. 60152700 · REV A	
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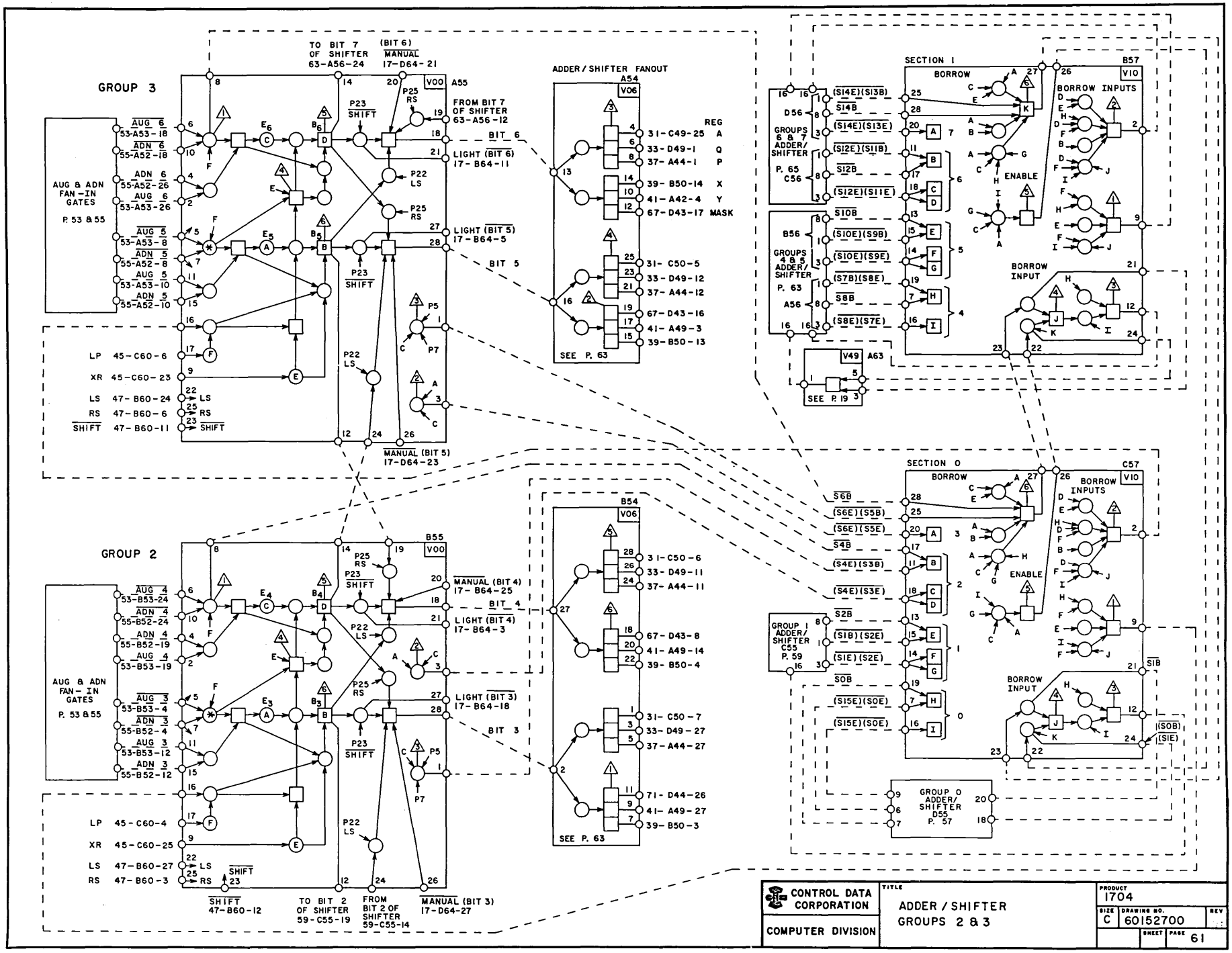
GROUP 3
GROUP 2
TO BIT 7 OF SHIFTER 63-A56-24
(BIT 6) MANUAL 17-D64-21
FROM BIT 7 OF SHIFTER 63-A56-12
BIT 6
LIGHT (BIT 6) 17-B64-11
LIGHT (BIT 5) 17-B64-5
BIT 5
MANUAL (BIT 5) 17-D64-23
AUG 6 53-A53-18
ADN 6 55-A52-18
ADN 6 55-A52-26
AUG 6 53-A53-26
AUG 5 53-A53-8
ADN 5 55-A52-8
AUG 5 53-A53-10
ADN 5 55-A52-10
AUG & ADN FAN-IN GATES
P. 53 & 55
LP 45-C60-6
XR 45-C60-23
LS 47-B60-24
RS 47-B60-6
SHIFT 47-B60-11
P23 SHIFT
P22 LS
P25 RS
P5
P7
ADDER / SHIFTER FANOUT
A54
V06
REG
31-C49-25 A
33-D49-1 Q
37-A44-1 P
39-B50-14 X
41-A42-4 Y
67-D43-17 MASK
31-C50-5
33-D49-12
37-A44-12
67-D43-16
41-A49-3
39-B50-13
SEE P. 63
SECTION 1
SECTION 0
BORROW
BORROW INPUTS
BORROW INPUT
ENABLE
B57
C57
V10
V49
A63
SEE P. 19
D56
B56
A56
GROUPS 6 & 7 ADDER/ SHIFTER P. 65 C56
GROUPS 4 & 5 ADDER/ SHIFTER P. 63
GROUP 1 ADDER/ SHIFTER C55 P. 59
GROUP 0 ADDER/ SHIFTER D55 P. 57
(S14E)(S13B)
S14B
(S14E)(S13E)
(S12E)(S11B)
S12B
(S12E)(S11E)
S10B
(S10E)(S9B)
(S10E)(S9E)
(S7B)(S8E)
S8B
(S8E)(S7E)
S6B
(S6E)(S5B)
(S6E)(S5E)
S4B
(S4E)(S3B)
(S4E)(S3E)
S2B
(S1B)(S2E)
(S1E)(S2E)
S0B
(S15E)(S0E)
(S15E)(S0E)
S1B
(S0B)
(S1E)
B55
V00
A55
MANUAL (BIT 4) 17-B64-25
BIT 4
LIGHT (BIT 4) 17-B64-3
LIGHT (BIT 3) 17-B64-18
BIT 3
MANUAL (BIT 3) 17-D64-27
AUG 4 53-B53-24
ADN 4 55-B52-24
ADN 4 55-B52-19
AUG 4 53-B53-19
AUG 3 53-B53-4
ADN 3 55-B52-4
AUG 3 53-B53-12
ADN 3 55-B52-12
AUG & ADN FAN-IN GATES
P. 53 & 55
LP 45-C60-4
XR 45-C60-25
LS 47-B60-27
RS 47-B60-3
SHIFT 47-B60-12
TO BIT 2 OF SHIFTER 59-C55-19
FROM BIT 2 OF SHIFTER 59-C55-14
B54
V06
31-C50-6
33-D49-11
37-A44-11
67-D43-8
41-A49-14
39-B50-4
31-C50-7
33-D49-27
37-A44-27
71-D44-26
41-A49-27
39-B50-3
SEE P. 63
CONTROL DATA CORPORATION
COMPUTER DIVISION
TITLE
ADDER / SHIFTER GROUPS 2 & 3
PRODUCT 1704
SIZE C
DRAWING NO. 60152700
REV
SHEET
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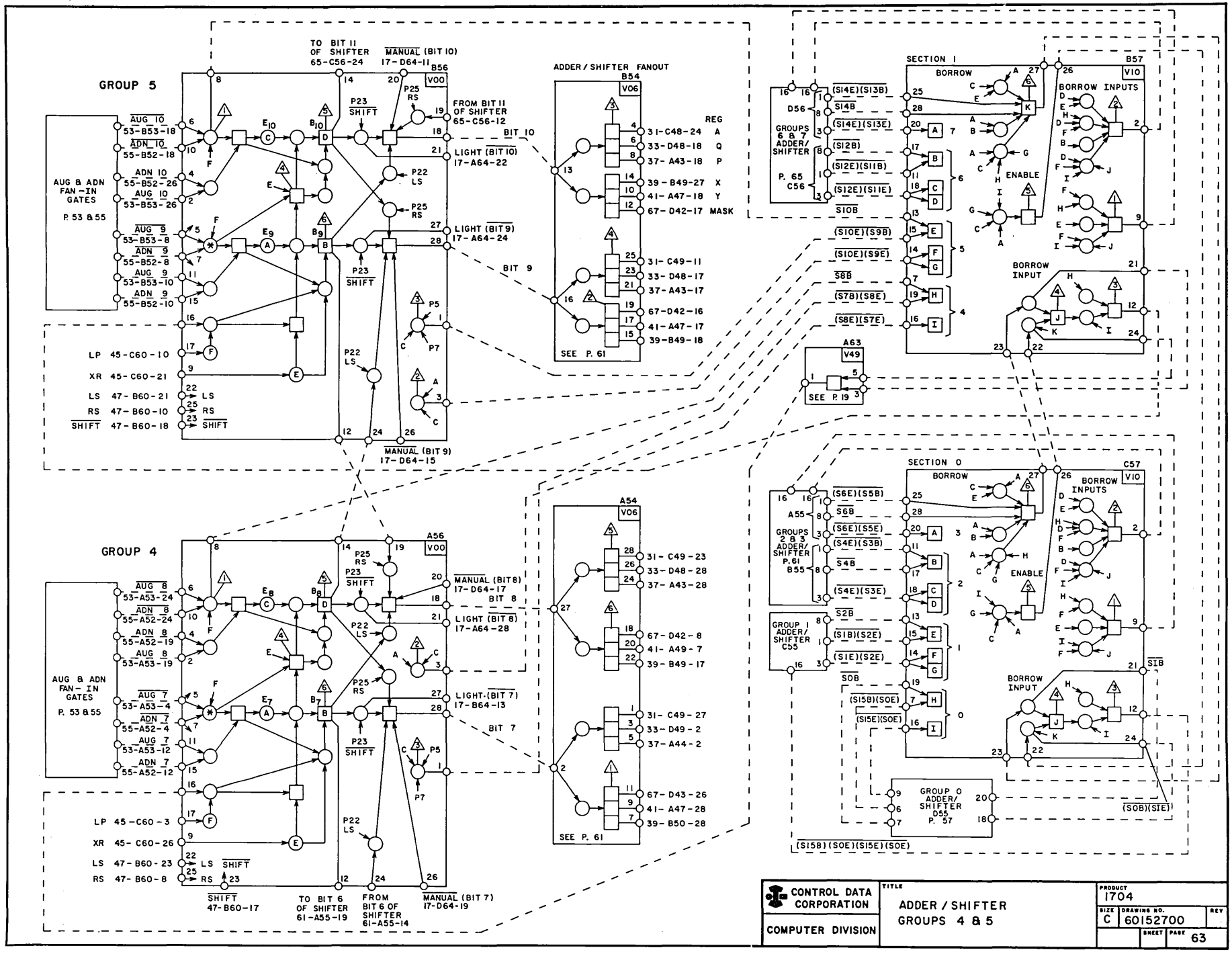
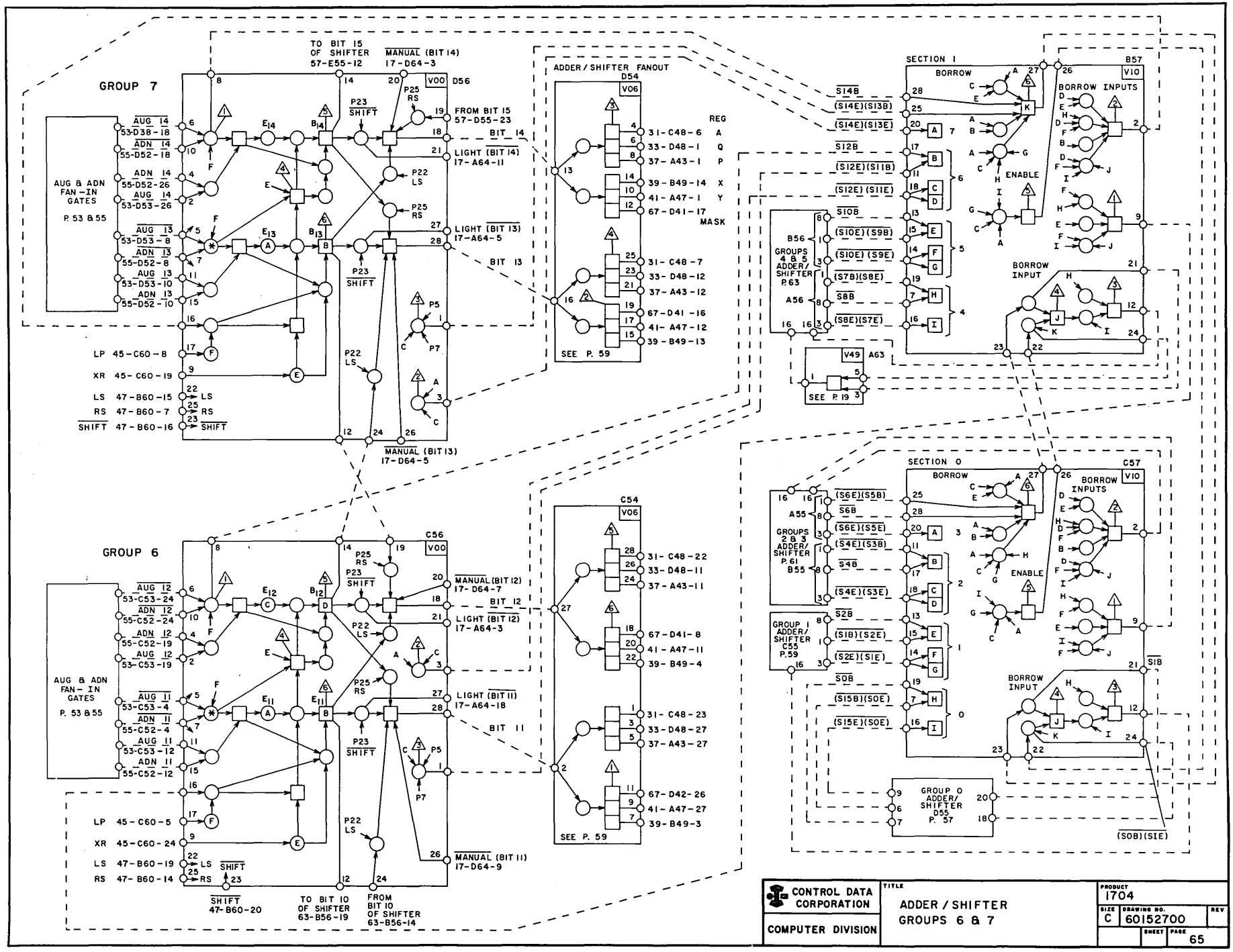
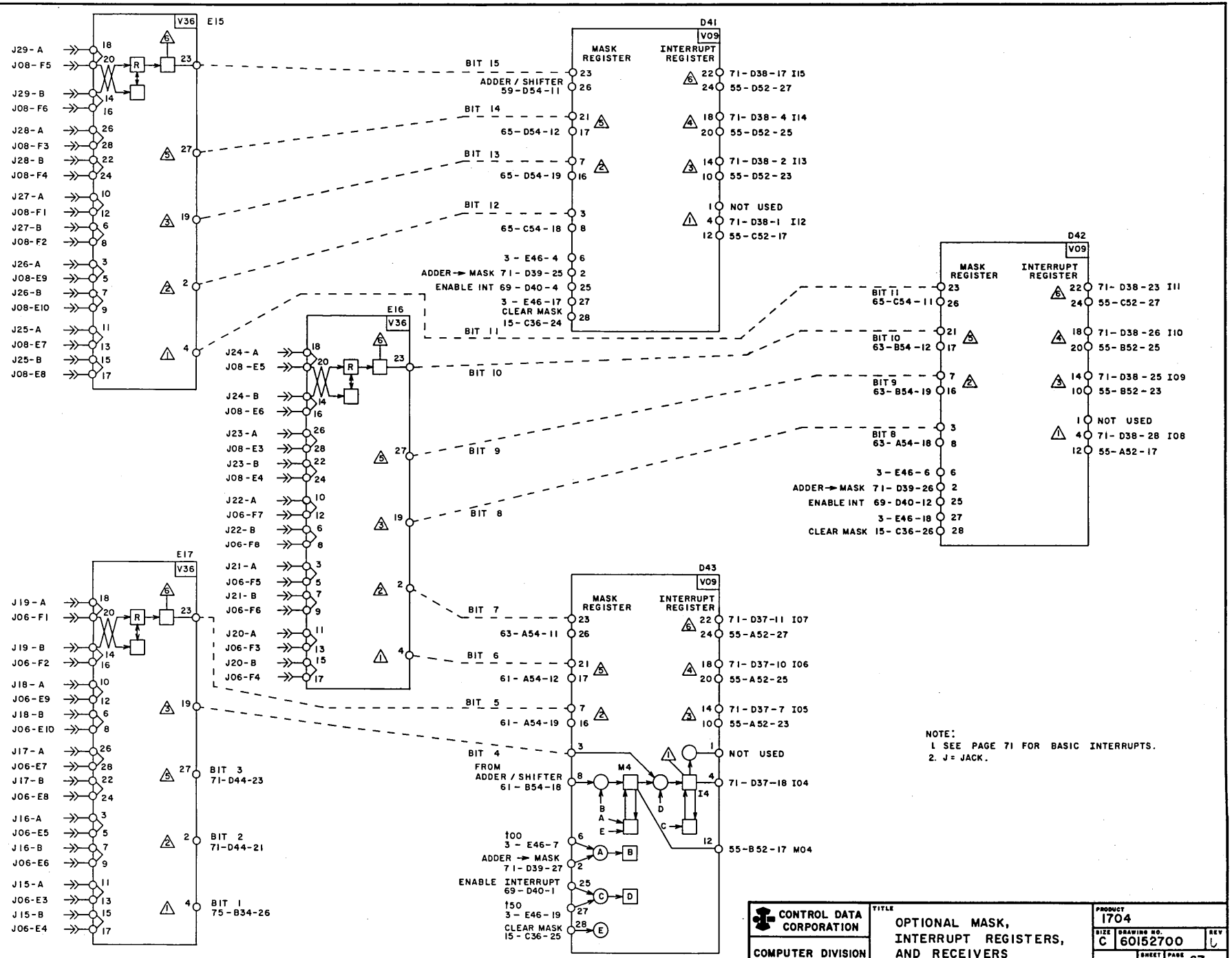


CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE ADDER / SHIFTER GROUPS 4 & 5	PRODUCT 1704 SIZE C · DRAWING NO. 60152700 · REV SHEET · PAGE 63	



CONTROL DATA CORPORATION	TITLE: ADDER / SHIFTER GROUPS 6 & 7	PRODUCT 1704	
COMPUTER DIVISION		SIZE C · DRAWING NO. 60152700 · REV	
		SHEET · PAGE 65	


E15
V36
J29-A
J08-F5
J29-B
J08-F6
J28-A
J08-F3
J28-B
J08-F4
J27-A
J08-F1
J27-B
J08-F2
J26-A
J08-E9
J26-B
J08-E10
J25-A
J08-E7
J25-B
J08-E8
BIT 15
BIT 14
BIT 13
BIT 12
BIT 11
BIT 10
BIT 9
BIT 8
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
71-D44-23
BIT 2
71-D44-21
BIT 1
75-B34-26
D41
V09
MASK REGISTER
INTERRUPT REGISTER
ADDER / SHIFTER 59-D54-11
65-D54-12
65-D54-19
65-C54-18
3-E46-4
ADDER→MASK 71-D39-25
ENABLE INT 69-D40-4
3-E46-17
CLEAR MASK 15-C36-24
71-D38-17 I15
55-D52-27
71-D38-4 I14
55-D52-25
71-D38-2 I13
55-D52-23
NOT USED
71-D38-1 I12
55-C52-17
E16
V36
J24-A
J08-E5
J24-B
J08-E6
J23-A
J08-E3
J23-B
J08-E4
J22-A
J06-F7
J22-B
J06-F8
D42
V09
BIT 11 65-C54-11
BIT 10 63-B54-12
BIT 9 63-B54-19
BIT 8 63-A54-18
3-E46-6
ADDER→MASK 71-D39-26
ENABLE INT 69-D40-12
3-E46-18
CLEAR MASK 15-C36-26
71-D38-23 I11
55-C52-27
71-D38-26 I10
55-B52-25
71-D38-25 I09
55-B52-23
NOT USED
71-D38-28 I08
55-A52-17
E17
V36
J19-A
J06-F1
J19-B
J06-F2
J18-A
J06-E9
J18-B
J06-E10
J17-A
J06-E7
J17-B
J06-E8
J16-A
J06-E5
J16-B
J06-E6
J15-A
J06-E3
J15-B
J06-E4
J21-A
J06-F5
J21-B
J06-F6
J20-A
J06-F3
J20-B
J06-F4
D43
V09
63-A54-11
61-A54-12
61-A54-19
FROM ADDER / SHIFTER 61-B54-18
100 3-E46-7
ADDER→MASK 71-D39-27
ENABLE INTERRUPT 69-D40-1
150 3-E46-19
CLEAR MASK 15-C36-25
71-D37-11 I07
55-A52-27
71-D37-10 I06
55-A52-25
71-D37-7 I05
55-A52-23
NOT USED
71-D37-18 I04
55-B52-17 M04
M4
I4
NOTE:
1. SEE PAGE 71 FOR BASIC INTERRUPTS.
2. J = JACK.
CONTROL DATA CORPORATION
COMPUTER DIVISION
TITLE
OPTIONAL MASK, INTERRUPT REGISTERS, AND RECEIVERS
PRODUCT 1704
SIZE C
DRAWING NO. 60152700
REV L
SHEET
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PROGRAM PROTECT

Module V54 contains three FFs which control program protect and protect violations. The Instruction Protected FF retains the state of the previous instruction. If the FF is set, the previous instruction was protected. If the FF is clear, the previous instruction was not protected. An interrupt occurring during the B cycle also sets the Instruction Protected FF. This simulates a protected operation while writing a return address.

Whenever a violation of the program protect system is detected, the Protect Fault FF sets and an internal interrupt is enabled. A 00 interrupt occurs if mask bit 00 is set and the interrupt system is active. A violation indicates that the nonprotected program has attempted an operation which could harm the protected program. The four program protect violations and their setting inputs to the Protect Fault FF are:

Violation	Input
1. A nonprotected instruction attempts to write into a storage location containing a protected instruction/operand. The contents of the storage location are not changed.	from pin 20
2. An attempt is made to write into a protected storage location via the external storage access when a nonprotected instruction was the ultimate source of the attempt. The contents of the storage location are not changed.	from pin 20
3. An attempt is made to execute a protected instruction following execution of a nonprotected instruction. The protected instruction is executed as a nonprotected Selective Stop instruction. It is not a violation, however, if an interrupt caused this sequence of instructions.	from inverter J
4. An attempt is made to execute the following instructions when they are not protected: Interregister with bit 0 = 1, EIN, IIN, EXI, SPB, or CPB. These instructions become nonprotected Selective Stop instruction under these circumstances.	from inverter*

The FF at the bottom of module V54 sets when violation number 3 is present. The output of this FF blocks the setting of the ADR FF and sets the REG FF in the Sequence controls. Therefore, if either violation 3 or 4 is present and REG mode selected, the F register clears. The computer recognizes the 00 code in the F register as a Selective Stop instruction. If the Selective Stop switch is in the stop position, the computer stops. If the switch is in the neutral position the instruction is executed as a nonprotected pass instruction. A "0" output at pin 6 clears the upper portion of the X register.

INTERRUPT

All three FFs on module V59 must be set for the computer to process an interrupt. The order of events for enabling the interrupt system is as follows:

1) Set first Enable Interrupt FF
2) Set second Enable Interrupt FF (interrupt system active)
3) Set Interrupt registers
4) Interrupt priority is checked
5) Interrupt FF is set (there is an interrupt)

The first Enable Interrupt FF is set at time 250 of the B cycle during REG of an Enable Interrupt or Exit Interrupt instruction. The second Enable Interrupt FF sets at time 200 of the B cycle when the ADR (ind) condition is present and the first Enable Interrupt FF is set. For the Enable Interrupt instruction, this delay allows one more instruction to be executed before enabling the interrupt system. There is no delay when using the Exit Interrupt instruction.

At time 50 of the A cycle, the second Enable Interrupt FF sets the Interrupt register, providing the Interrupt FF is cleared. The Interrupt FF must be cleared to insure that an interrupt is not in process at the same time the Interrupt register is being set.

At time 250 of the A cycle, the Interrupt FF sets if all of the following conditions are present:

1) The second Enable Interrupt FF set
2) Interrupt signal present from interrupt priority
3) ADR (ind) + RNI

The interrupt occurs reading an instruction from storage or reading an indirect address.

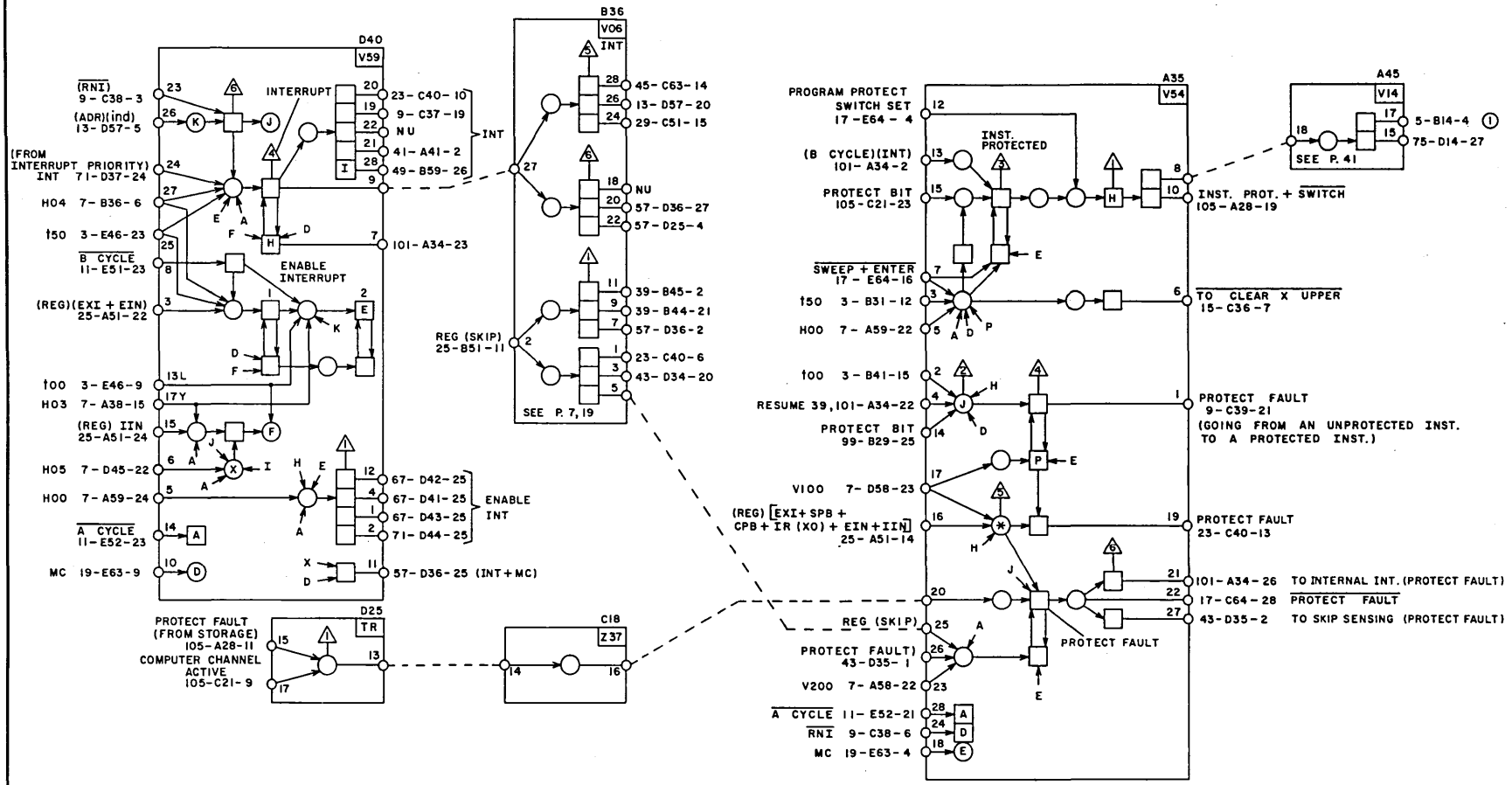
Two main gates clear all three FFs and disable the interrupt system. The first gate clears all three FFs when an interrupt state is entered and the following conditions exist:

1) A cycle
2) time 300
3) $\overline{\text{ADR (ind)}}$
4) $\overline{\text{RNI}}$

This gate disables interrupt while the computer stores the registers and sets the new mask. The second gate clears the FFs and disables interrupt when the following conditions exist:

1) A cycle
2) time 200
3) REG (ITN)

This gate disables interrupt while the computer restores the registers in preparation of exiting from an interrupt state.



NOTES:

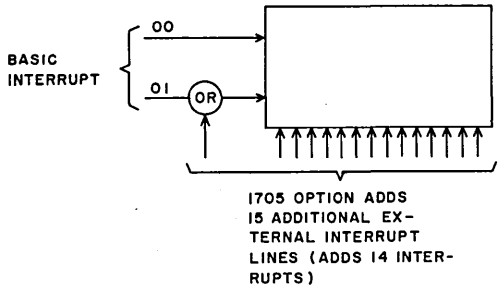
(1) DENOTE PAGE NUMBER FROM LOW SPEED COMPUTER DIAGRAMS.

CONTROL DATA CORPORATION	TITLE: PROGRAM PROTECT AND INTERRUPT	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C	DRAWING NO.: 60152700 REV: -L
			SHEET / PAGE: 69

The basic 1700 Computer has two interrupts. They are as follows:

1) Interrupt state 00 = (internal) Storage Parity Error or Program Protect Fault
2) Interrupt state 01 = (external) Low-Speed I/O

An option may be added which gives an additional 14 external interrupt lines. Thus, the computer may have 16 different interrupts. The discussions that follow assume the computer has 16 interrupts.



MASK REGISTER

The 16-bit Mask register is the enable for each interrupt state or line. Bit 00 of the Mask register corresponds to interrupt line 0, bit 01 to line 1, etc. To enable an interrupt line, its corresponding bit in the Mask register must be set. The Mask register is set by the Inter-Register instruction.

Module V09 shows the first 4 bits of the Mask register and Interrupt register. Three additional V09 modules are added if 16 interrupts are used. The Mask register is set by the Adder → Mask Control FF on module V44. The output of the Mask register returns to the Adder/Shifter.

ADDER → MASK CONTROL

The Adder → Mask FF has two main setting gates. The first gate is satisfied if the manual Mask register selector on the console is activated and the Q → Adder FF is set. At time V250 of the A cycle, the second gate is enabled if (REG) (IR) (X_0) = 1. X_0 (X register, bit 0) indicates that the Mask register is the destination register during an Inter-Register instruction. The Mask register sets at time 300 according to its selected Adder/Shifter inputs if the Adder → Mask FF is set.

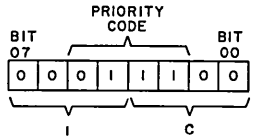
INTERRUPT REGISTER

The 16-bit Interrupt register is a holding register for the 16 interrupt lines and sets if all of the following conditions are present:

1) The corresponding bit in the Mask register must be set.
2) The corresponding interrupt line signal present.
3) The Enable Interrupt FF set (by an EXI + EIN instruction), t50 (A cycle), and INT FF clear.

INTERRUPT PRIORITY

The interrupt priority consists of modules V11 and V12. When one of the Interrupt register bits sets, the priority network recognizes which interrupt line is present and forms a 4-bit code. The code specifies Δ for the Exit instruction from that particular interrupt state. For example, if the priority input comes from Interrupt register bit 07, then the output code is a binary 0111. The first three columns in Table 1 show the relationship between interrupt states, Δ portion of EXI instruction, and location of the return address. When an interrupt state is recognized, the Δ portion of the EXI instruction is formed. Delta defines the interrupt state from which the exit is taken. The EXI instruction automatically reads the address containing the return address and jumps to the return address.



Δ PORTION OF EXI INSTRUCTION

If two or more interrupts have equal priority and occur at the same time, the computer recognizes the lowest interrupt line. For example, if interrupt states 05 and 12 occur at the same time, the priority network recognizes interrupt 05 and forms a binary output code of 0101.

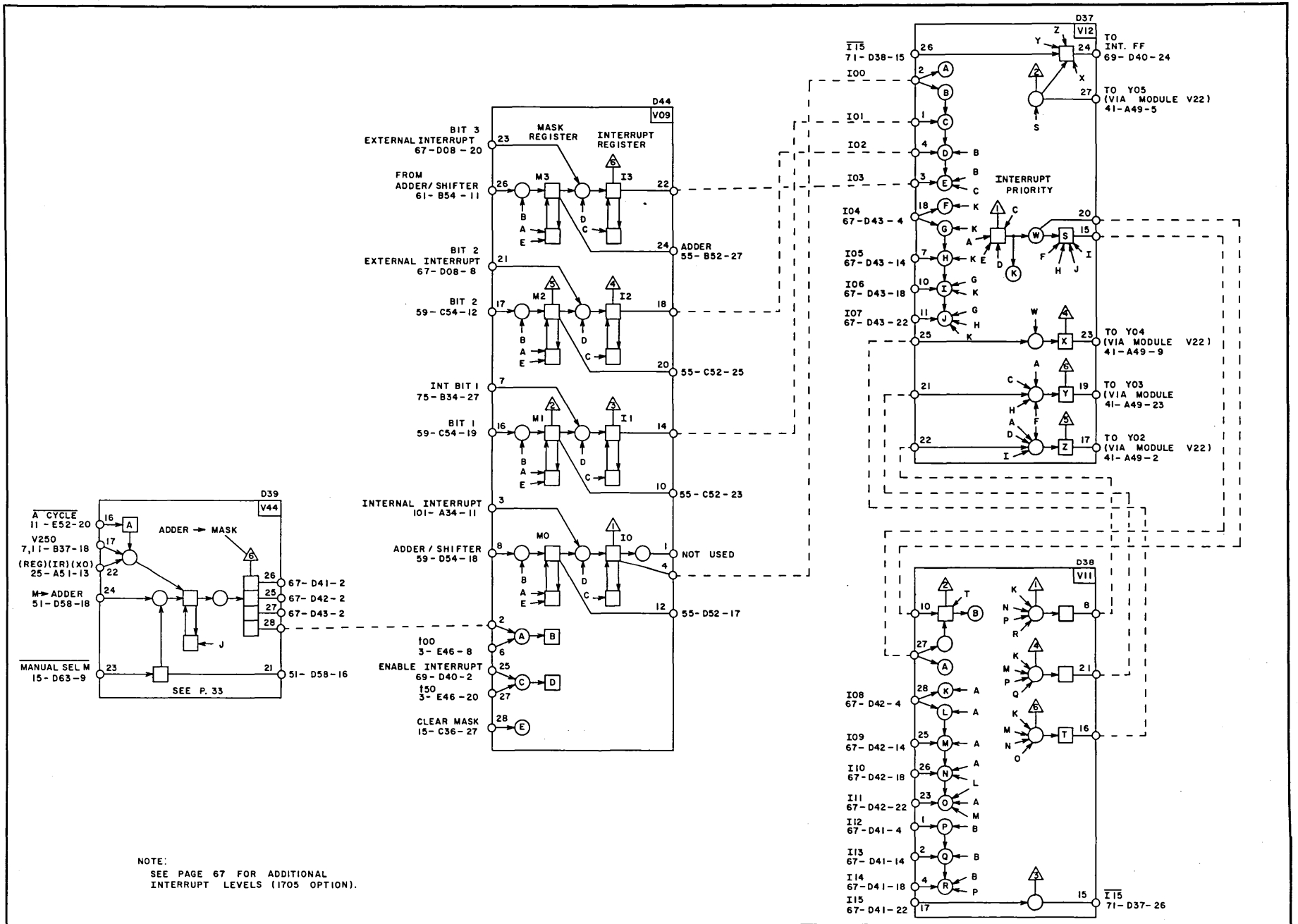
The interrupt state priority code output transfers to the Y register via the V22 module on page 41.

TABLE 1. INTERRUPT STATE DEFINITIONS

Interrupt State$_{10}$	Value of Δ to Exit State$_{16}$	Location of Return Address	Location of First Instruction After Interrupt Occurs$_{16}$
* 00	00	0100	0101
* 01	04	0104	0105
02	08	0108	0109
03	0C	010C	010D
04	10	0110	0111
05	14	0114	0115
06	18	0118	0119
07	1C	011C	011D
** 08	20	0120	0121
09	24	0124	0125
10	28	0128	0129
11	2C	012C	012D
12	30	0130	0131
13	34	0134	0135
14	38	0138	0139
15	3C	013C	013D

*Interrupts in basic computer

**Interrupts added by 1705 Interrupt/Data Channel option

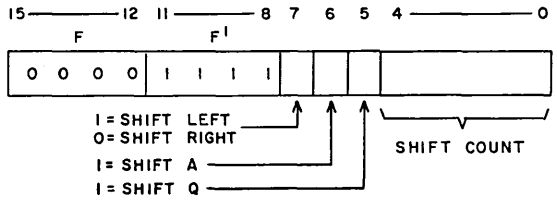


NOTE:
SEE PAGE 67 FOR ADDITIONAL INTERRUPT LEVELS (1705 OPTION).

CONTROL DATA CORPORATION	TITLE: MASK REGISTER AND INTERRUPT PRIORITY	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C	DRAWING NO.: 60152700
		REV: S	
		SHEET	PAGE: 71

SHIFT, MUI, AND DVI CONTROLS

The V72 module contains the logic that controls the shift instructions. Shift instructions are identified by a zero instruction field (F) and a hexidecimal F in the sub-instruction field (F^1) Bit positions X05-07 identify the type of shift instruction. Below is the format for the shift instructions.



The Shift Cycle FF controls the shifting required by the shift instructions. The first shift occurs during the A cycle and the remaining shifts occur during the C cycle. At time 250 of the A cycle, the shift count (currently in bit positions X00-04) is sensed for a count of zero. If the shift count is zero, the Shift Cycle FF is not enabled and the logic proceeds to B cycle RNI. If the shift count is not zero, the Shift Cycle FF is set and a shift occurs. The shift count then replaces the lower 5 bits of the Y register and is decremented by one. The Y register now contains the shift count.

At time 250 of each pass of the C cycle, a shift occurs and the shift count decrements by one. The logic proceeds to B cycle RNI when the shift count decrements to zero and at time 250 of the C cycle.

The SR1 and SR2 FFs on the V65 modules sense the sign of the operands used in Multiply and Divide operations and determine the sign of the result. Any negative operand must be complemented because the associated logic recognizes only positive numbers. The two SR FFs record the complemented operands.

The SR2 FF senses the signs of the operand in the Multiply or Divide operations and becomes enabled if it is negative and the corresponding conditions are met. The SR1 FF senses the sign of the operand in the X register and becomes enabled if it is negative and the corresponding conditions are met. The output from pin 26 goes to the Adder controls and enables the complementing of the negative operand.

Note that the SR1 FF senses the sign during Multiply operations and the SR1 and SR2 FFs sense the sign during Divide operations. The SR1 FF senses the sign of the quotient and the SR2 FF senses the sign of the remainder. The remainder maintains the sign of the dividend.

The output of pins 1 and 3 of the V63 module control the complementing of the product, quotient, and remainder. The condition Y00-04=0 signifies that shifting is completed (MUI or DVI instruction is finished) and the result is ready to be complemented if it is negative.

A Multiply instruction multiplies the contents of the storage location specified by the effective address by the contents of the A register. The 32-bit product replaces the contents of Q and A with the most significant bits in the Q register. Bit Q15 is the sign bit.

The lower 5 bits of the Y register hold the shift count that is set to 10_{16} at the start of each Multiply instruction. The shift count is decremented by one before each shift operation.

The Adder/Shifter can shift a maximum of 16_{10} bits (one register at a time). It is therefore necessary to have a bit bucket to hold the lowest order bit of the Q register during a shift that impliments both the A and Q registers (32 bits). During a Multiply instruction, the contents of QA are shifted right, end off, one place. The lowest order bit of the Q register is placed in the bit bucket and the contents of the Q register are right shifted one place. The contents of the A register are then right shifted one place

with the contents of the bit bucket replacing bit position A_{15}. A more detailed description of the bit bucket logic is on page 56.1.

The Multiply bit (MB) is in bit position A00 during the first shift operation (A cycle) and is in bit position A_{01} during the remaining 15_{10} shift operations (C cycle). If MB=0, the contents of QA are right shifted in as previously described. If MB=1, the contents of the X register (storage location specified by the effective address) are added to the contents of the Q register and the sum replaces the contents of the Q register. The contents of QA are then right shifted as previously described.

Below is an example of how the Multiply instruction operates.

Example: (A) = $1FA2_{16}$
(X) = 5_{16}
(A)(X) = $9E2A_{16}$

Q	A	MB	Y	Bit Bucket
		0		
0000000000000000	0001111110100010	1	F	0
000	0000111111010001	0	E	1
010	1000011111101000	0	D	0
001	0100001111110100	0	C	1
000	1010000111111010	1	B	0
000	0101000011111101	0	A	1
010	1010100001111110	1	9	0
001	0101010000111111	1	8	0
011	0010101000011111	1	7	0
100	0000010100001111	1	6	1
100	1000101010000111	1	5	1
100	1100010101000011	1	4	1
100	1110001010100001	0	3	1
100	1111000101010000	0	2	0
010	0111100010101000	0	1	0
001	0011110001010100	0	0	1
000	1001111000101010		0	

ex: MB=1
(Q)=000
(X)=101
101
(Q) → Bit Bucket

ex: MB=1
(Q)=001
(X)=101
110
(Q) → Bit Bucket

$1001111000101010_2 = 9E2A_{16}$

During a Divide instruction the contents of the effective address (X register) is compared with the contents of the Q register. If (X) > (Q) a "1" enters EAB (End Around Borrow) and a "0" enters the bit bucket. A Long Left Shift shifts QA one place with the "0" in the bit bucket replacing bit position A00. Note that the bit bucket always contains the complement of the state of the EAB.

If (X) $\leq$ (Q) a "0" enters EAB and a "1" enters the bit bucket. The contents of the X register is subtracted from the contents of the Q register and the difference enters the Q register. A Long Left Shift shifts QA one place with the "1" in the bit bucket replacing bit position A00. In a QA shift, the Q and A registers are shifted separately since a maximum of 16 bits can be shifted at one time. Bit A15 replaces bit Q00 through the associated logic of the Adder/Shifter. A more detailed discussion of the logic of this process is on page 58.6.

This comparing and shifting process continues until the shift count reduces to zero. The shift count in the Y register operates the same as in the previously described Multiply instruction.

The Divide instruction divides the contents of Q and A registers with the contents of the effective address. The Q register contains the most significant bits before execution. The quotient is in the A register and the remainder in the Q register at the end of the Divide operation.

Below is an example of a Divide instruction.

Divide: $\frac{(A)}{(X)\ \lceil\ (QA)}$

$Q = 0$
$A = 272E_{16} = 0010011100101110_2$
$X = 2_{16}$

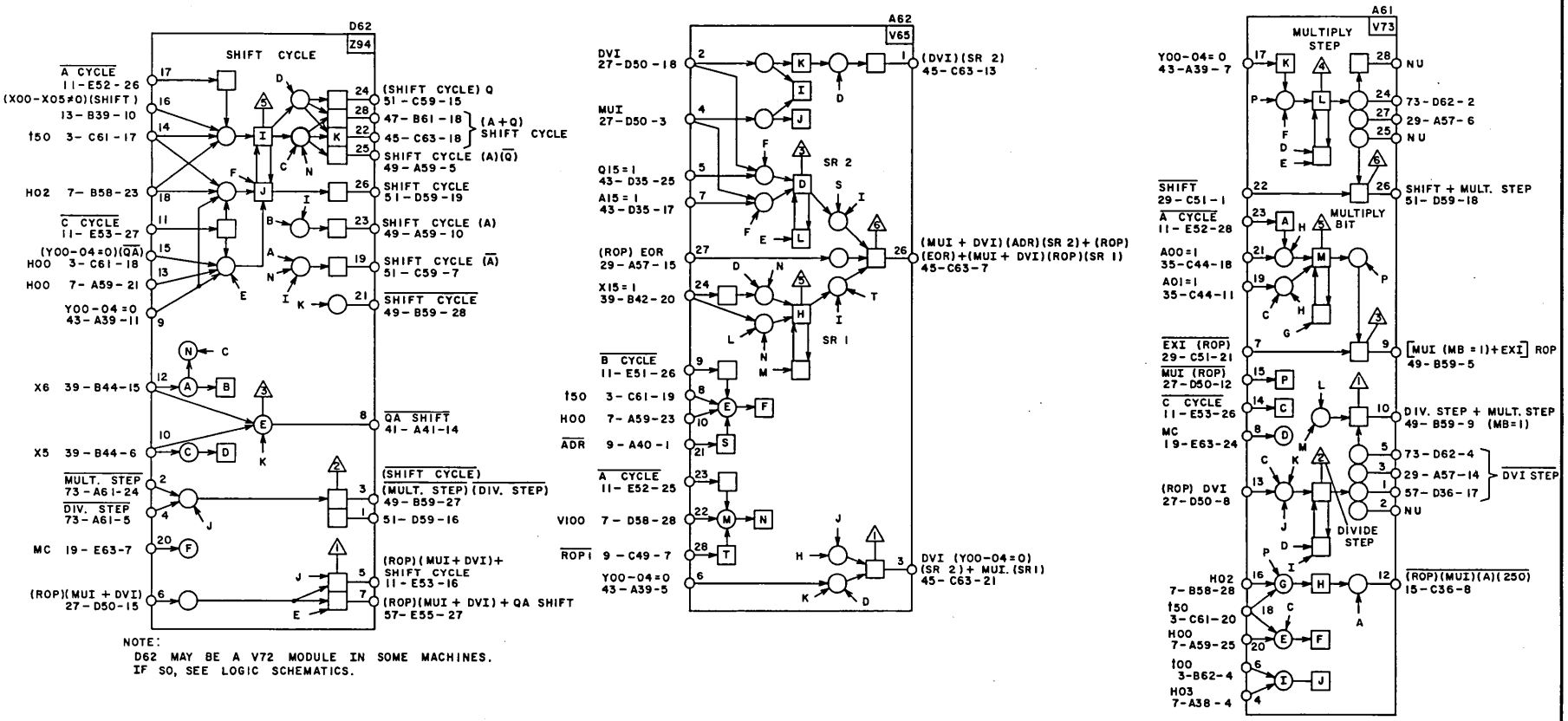
Q	A	Y	EAB		
0000000000000000	0010011100101110	F			Bit Bucket
000			1	0	
	0100111001011100	E			
000			1	0	ex: Q ≥ X
	1001110010111000	D			EAB = 0
001			1	0	Bit Bucket = 1
	0011100101110000	C			
010			0	1	(Q) = 010
000	0111001011100001	B			(X) = 010
000			1	0	000
	1110010111000010	A			
001			1	0	Replaces (Q)
	1100101110000100	9			
011			0	1	
001	1001011100001001	8			
011			0	1	
001	0010111000010011	7			
010			0	1	
000	0101110000100111	6			
000			1	0	
	1011100001001110	5			
001			1	0	
	0111000010011100	4			
010			0	1	
000	1110000100111001	3			
001			1	0	
	1100001001110010	2			
011			0	1	
001	1000010011100101	1			
011			0	1	
001	0000100111001011	0			
010			0	1	
000	0001001110010111				

Remainder | Answer

The V73 module contains the Multiply Step, Multiply Bit, and Divide Step FFs. These three FFs enable the logic that controls the Multiply and Divide instructions.

The Multiply Bit FF senses bit location A00 during the A cycle and bit location A01 during the C cycle. If the sensed bit is a "1" and the corresponding conditions are present, the Multiply Bit FF sets and enables the logic that performs the adding of (Q) and (X) as previously described in the description of the multiply procedure.

The Multiply Step FF sets on the condition (MUI) (ROP) (050) (Y00-04≠0) (C cycle). The Multiply Step FF enables the shifting and associated logic that performs a Multiply instruction. The Divide Step FF enables the shifting and associated logic that performs a Divide instruction.



CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE SHIFT, MUI, & DVI CONTROLS	PRODUCT 1704 SIZE C · DRAWING NO. 60152700 · REV Y SHEET · PAGE 73	

The AQ I/O Channel operates in such a way that the Q register of the computer contains the address of the peripheral device and the data transfer occurs to/from the A register of the computer.

INPUT ON AQ CHANNEL

A single word transfers to the A register whenever the computer executes the Input to A instruction (Q00=0). The request for data by the computer is signified by a "1" signal on the Read line. The peripheral device whose address is in the Q register responds with a Reply when data is available to the A register.

If no data is available the peripheral device responds with a Reject. In either case the peripheral device must respond with a Reject or Reply within 4 microseconds. If no response is obtained in 6 microseconds the computer generates an internal Reject. Reply causes the computer to go to address P + 1. (P is the address of the input instruction). Internal Reject causes the computer to go to address P + Δ, where Δ is the lowest 8 bits of the input instruction, the highest of which is a sign bit. External Reject causes the computer to go to address P + 1 + Δ.

OUTPUT ON AQ CHANNEL

The output on AQ operates similar to Input on AQ. The presence of the output data is signified by the presence of a "1" on the Write line. The responses are identical for input and output.

LOGIC FOR AQ I/O

Module V53 contains the Read FF for Input instructions and Write FF for output instructions. The "0" signal at pin 27 disables the computer timing chain when an Input or Output instruction is recognized.

The Read or Write signals enable transmitter circuits on the ZT module, a 7 usec delay on the V88 module, and a signal at pin 24 of the V74 module. The "0" output at pin 24 enables the computer timing chain when the following condition is present:

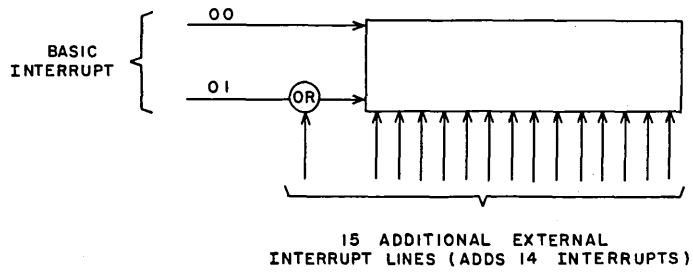
$$(\text{Read} + \text{Write})(\text{Reply} + \text{Reject})$$

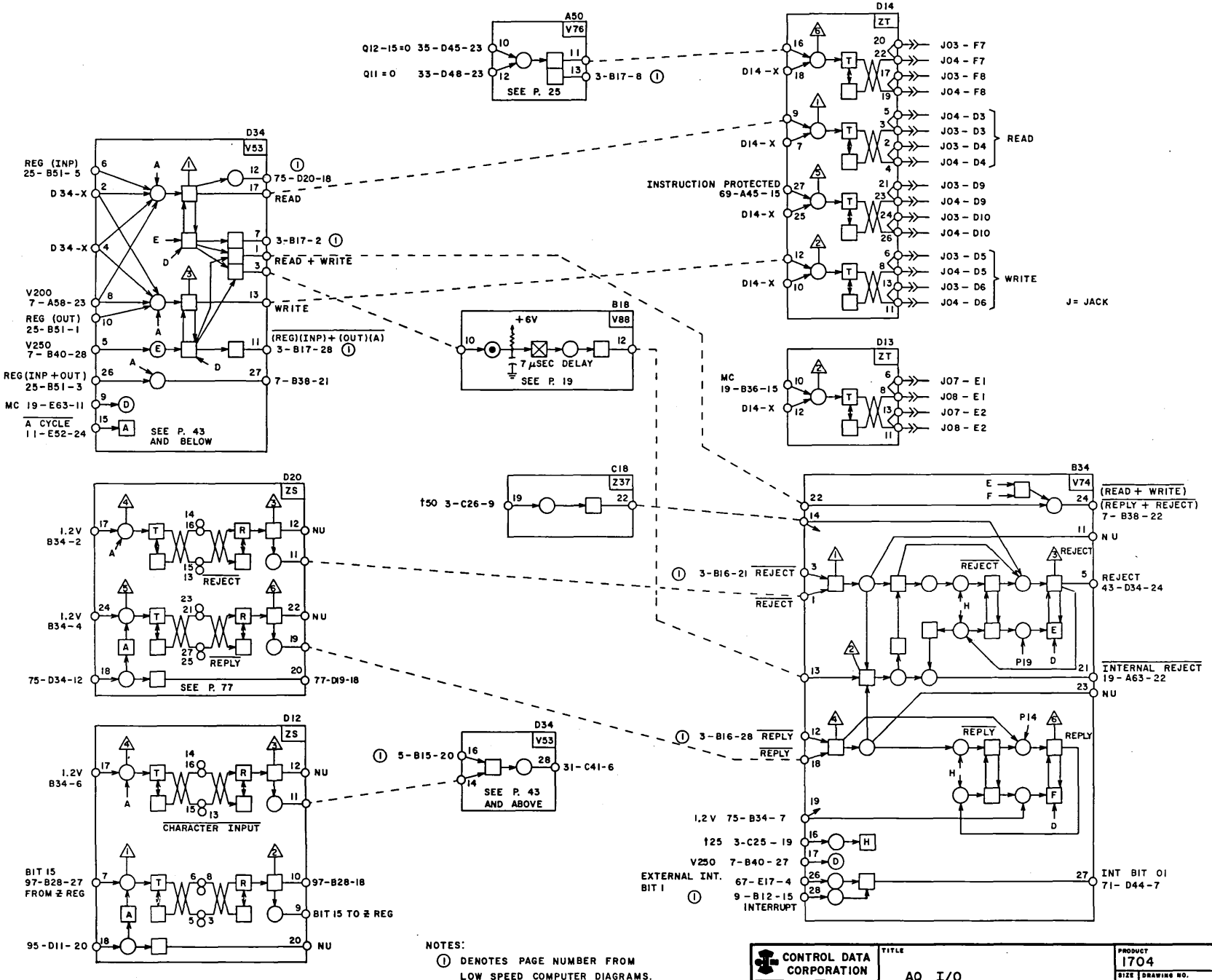
The Reply or Reject signals enter receiver circuits on a ZS module (location D20). These signals then set the appropriate FFs on module V74. If neither a Reject or Reply signal is received within 7 usec, an internal Reject is generated and the Reject FF sets.

The Character Input signal is received on a ZS module (location D12). This is a "1" signal sent to the computer during Input operations. If this signal is present during an Input to A the lower 8-bit character is loaded into the lower 8 bits of A without disturbing the upper 8 bits of A.

EXTERNAL INTERRUPT

Pins 26 and 28 of module V74 are external interrupt lines. These interrupts are OR'ed together in forming interrupt 01. The following figure shows the interrupt system including the 1705 option.





NOTES:

(1) DENOTES PAGE NUMBER FROM LOW SPEED COMPUTER DIAGRAMS.

CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE: AQ I/O PART 1

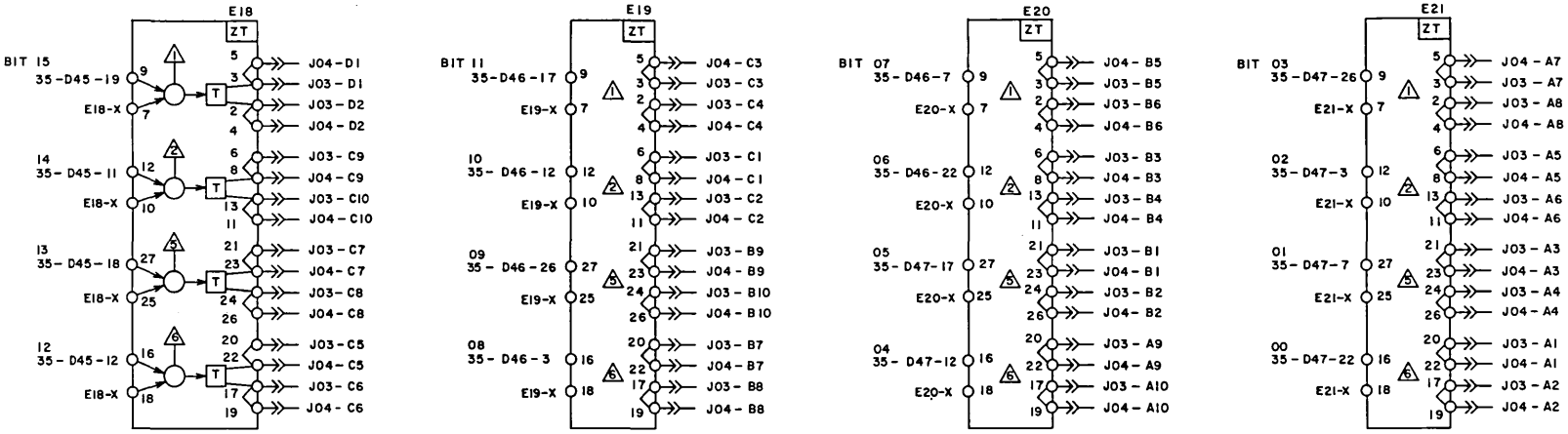
PRODUCT 1704
SIZE C | DRAWING NO. 60152700 | REV AA
SHEET | PAGE 75

TABLE 2. ZS MODULE CABLING

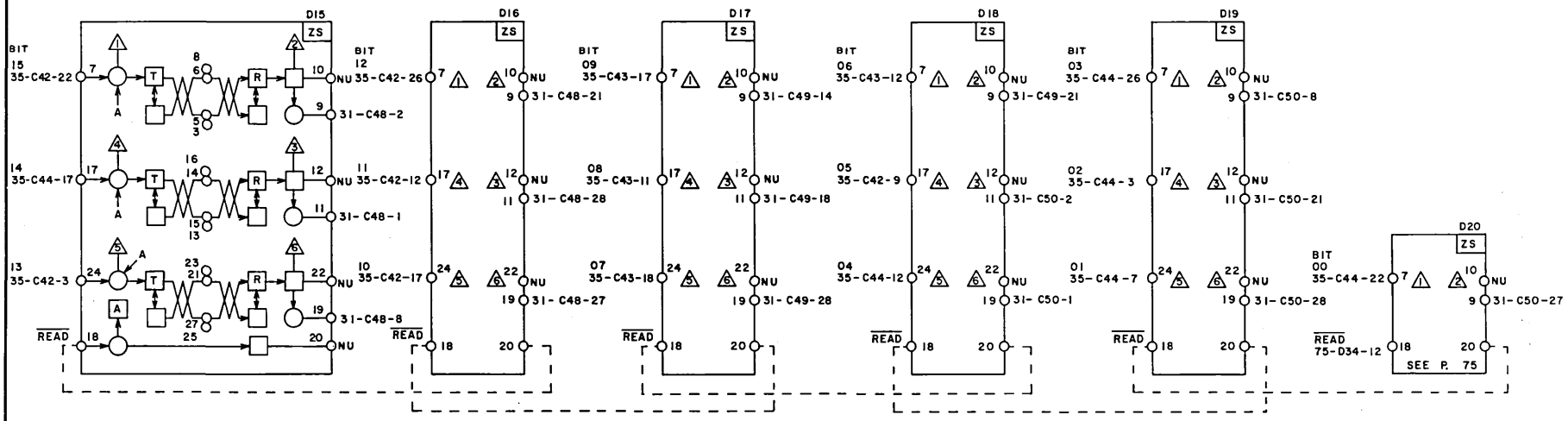
Module Location	Pin	Destination	Module Location	Pin	Destination	Module Location	Pin	Destination	Module Location	Pin	Destination
D12	3	J06-D2	D15	3	J02-D2	D16	3	J02-C6	D17	3	J02-B10
	5	J05-D2		5	J01-D2		5	J01-C6		5	J01-B10
	6	J05-D1		6	J01-D1		6	J01-C5		6	J01-B9
	8	J06-D1		8	J02-D1		8	J02-C5		8	J02-B9
	13	J02-D8		13	J02-C10		13	J02-C4		13	J02-B8
	14	J02-D7		14	J02-C9		14	J02-C3		14	J02-B7
	15	J01-D8		15	J01-C10		15	J01-C4		15	J01-B8
	16	J01-D7		16	J01-C9		16	J01-C3		16	J01-B7
	21			21	J02-C7		21	J02-C1		21	J02-B5
	23			23	J01-C7		23	J01-C1		23	J01-B5
	25			25	J02-C8		25	J02-C2		25	J02-B6
	27			27	J01-C8		27	J01-C2		27	J01-B6

Module Location	Pin	Destination	Module Location	Pin	Destination	Module Location	Pin	Destination
D18	3	J02-B4	D19	3	J02-A8	D20	3	J02-A2
	5	J01-B4		5	J01-A8		5	J01-A2
	6	J01-B3		6	J01-A7		6	J01-A1
	8	J02-B3		8	J02-A7		8	J02-A1
	13	J02-B2		13	J02-A6		13	J02-D6
	14	J02-B1		14	J02-A5		14	J02-D5
	15	J01-B2		15	J01-A6		15	J01-D6
	16	J01-B1		16	J01-A5		16	J01-D5
	21	J02-A9		21	J02-A3		21	J02-D3
	23	J01-A9		23	J01-A3		23	J01-D3
	25	J02-A10		25	J02-A4		25	J02-D4
	27	J01-A10		27	J01-A4		27	J01-D4

Q REGISTER



A REGISTER

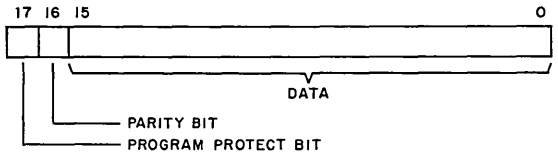


CONTROL DATA CORPORATION	TITLE: AQ I/O PART 2	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C · DRAWING NO.: 60152700 · REV: S	
		SHEET · PAGE: 77	

STORAGE

GENERAL INFORMATION

The 1700 storage consists of up to eight banks of magnetic core storage. Each bank contains 4096 locations for 18-bit words. The format of the storage words is shown below.



The circuits for the eight banks are identical. The storage timing and control circuits select the storage bank from the translation of the three high-order stages of the address (S register).

The description of the storage circuits is based on bank 0 which is provided with the basic system. Unless otherwise stated, the description of the bank 0 storage circuits applies to the banks contained in any of the 1700 storage options.

Each storage bank consists of the storage stack, inhibit decks, and drive decks. The storage stack contains 18 planes of magnetic cores assembled in the conventional matrix arrangement.

Current-carrying wires pass through the cores and magnetize them in one direction or the other. The direction of current flow determines the direction of magnetization. Approximately 400 ma-turns of magnetizing force are needed to switch a core into one of its two stable states ("1" or "0").

Five wires pass through each core. They are:

- A horizontal drive (x wire)
- A vertical drive (y wire)
- A horizontal inhibit (I_x wire)
- A vertical inhibit (I_y wire)
- A diagonal sense (S wire)

Coincident currents (one x and one y) switch the cores. A core is addressed by simultaneously transmitting half-amplitude (200-ma) current pulses through a selected x wire and a selected y wire.

Only the core at the intersection of the selected x and y wires receives sufficient magnetizing current to switch its state. All other cores in the same row or column as the selected core receive half-amplitude current pulses which are not sufficient to switch the core. In Figure 11, if the left-most y wire and the top x wire carry current pulses, core A switches; cores B and C receive half-amplitude currents; and core D receives no current pulses.

The polarity of the residual magnetization determines the binary information in a core. The read current pulse on the selected x or y wire stores a "0". The write pulse without a coincident current on the I wires stores a "1" in the core.

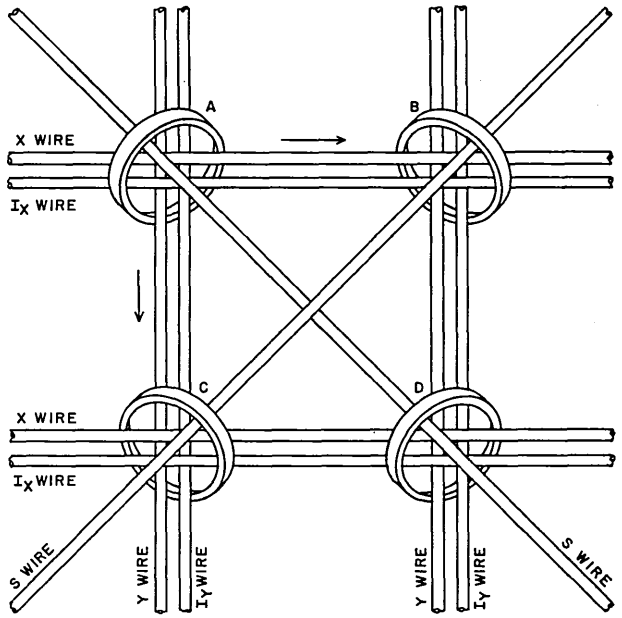


Figure 11. Portion of Magnetic Core Matrix

Applying a read pulse to the selected x and y wires reads information from the selected core. If the core previously stored a "1", the pulse switches the core to a "0". This change induces a pulse on the S wire. The pulse on the S wire is interpreted as a "1" bit from the core. If the core previously stored a "0", the read pulse does not affect it. Thus, no pulse is induced on the S wire.

One memory plane contains 4096 cores in a 64-by-64 array. Each bit of a word is stored in a separate plane. Thus, the stack contains 18 planes.

MAGNETIC CORES

The magnetic cores used in the 1700 storage planes have two stable magnetic states ("1" and "0") because of the square hysteresis loop properties of the ferrite material. A current sufficient to cause enough flux density switches the core to positive or negative saturation when applied to the selected x and y wires. When the current is removed, the flux density drops to the residual positive or negative state. The positive residual state corresponds to a "0" and the negative to a "1".

If a core receives only a half-amplitude current, the core does not switch but remains in the residual state caused by the last coincident half-amplitude pulses.

Any change in the magnetic state of a core causes a change in the total flux linking the core and any winding passing through it. Such a change produces a voltage on the sense winding. During the time read current is applied, the output voltage is sampled to determine if the core switches. If a large voltage is sensed, the core was in the "1" state. If a small voltage is detected, the core was in the "0" state and merely shifted from the positive residual state to the positive saturation state and back.

A common sense line threads through all 4096 cores in a storage plane. When reading, 64 x and 64 y cores contribute to the sense voltage. The total voltage induced by the 126 partially selected cores is less than the voltage induced on the line by the one selected core switching from a "1". The sense line passes diagonally through the cores in such a way that voltages from unselected cores tend to cancel.

STORAGE PLANES

A storage plane is a 4-by-4-inch printed circuit board which holds 4096 cores in a 64-by-64 matrix. Five wires pass through each core. Figure 12 shows a simplified storage plane containing a 24-by-24 matrix; however, all the principles of this matrix apply to the larger matrix.

The wires that suspend the cores terminate on the inside edges of the board, and printed wiring carries the connections to the outside edges (top and bottom) for easier access. The 64 horizontal x drive lines are brought to connections on each of the two opposite edges of the board. In plane 0, which is used as an example in Figure 12, the even-numbered drive lines enter the plane from the DC edge and the odd-numbered lines from the AB edge. The letters at the corners of the plane in Figure 12 fix the reference points of the plane in respect to the two views of the stack on the block diagram. The 64 vertical y drive lines enter the plane on the other edges in a similar manner. The sense line is a single line threading all the cores as shown in Figure 12. The two ends of the sense line terminate at one corner of the plane. Inhibit line connections enter the stack on the other three corners.

The inhibit lines are arranged in four vertical and four horizontal stripes or quadrants. Thus, the vertical inhibit lines run parallel to the y drive lines and the horizontal parallel to the x drive lines. The inhibit drive line for each stripe runs through 16 rows or columns of cores. During the write cycle of storage, one horizontal and one vertical inhibit stripe is energized coincident with the write drive. Thus, one 16-by-16 area of cores receives full inhibit drive in each plane that corresponds to a "0" in the Z register. The cores that receive full inhibit drive are prevented from switching to a "1". Since the read drive pulse preceded the write and switched the reference core to a "0", the full inhibit drive maintains the referenced core at the "0" state if the corresponding bit position of the word to be restored is a "0".

The direction of inhibit current in the energized stripes is opposite to the x or y drive current of the write pulse, thus preventing the magnetization of the referenced core to the "1" state. For example, if write drive current enters the plane on lines y0 and x0 (Figure 12) and a "0" is to be stored in the plane, the 0 vertical and horizontal inhibit stripes are energized with current in the opposite direction. The contents of the Z register select the planes that are to be inhibited. The address contained in the S register selects the horizontal and vertical stripes to be energized.

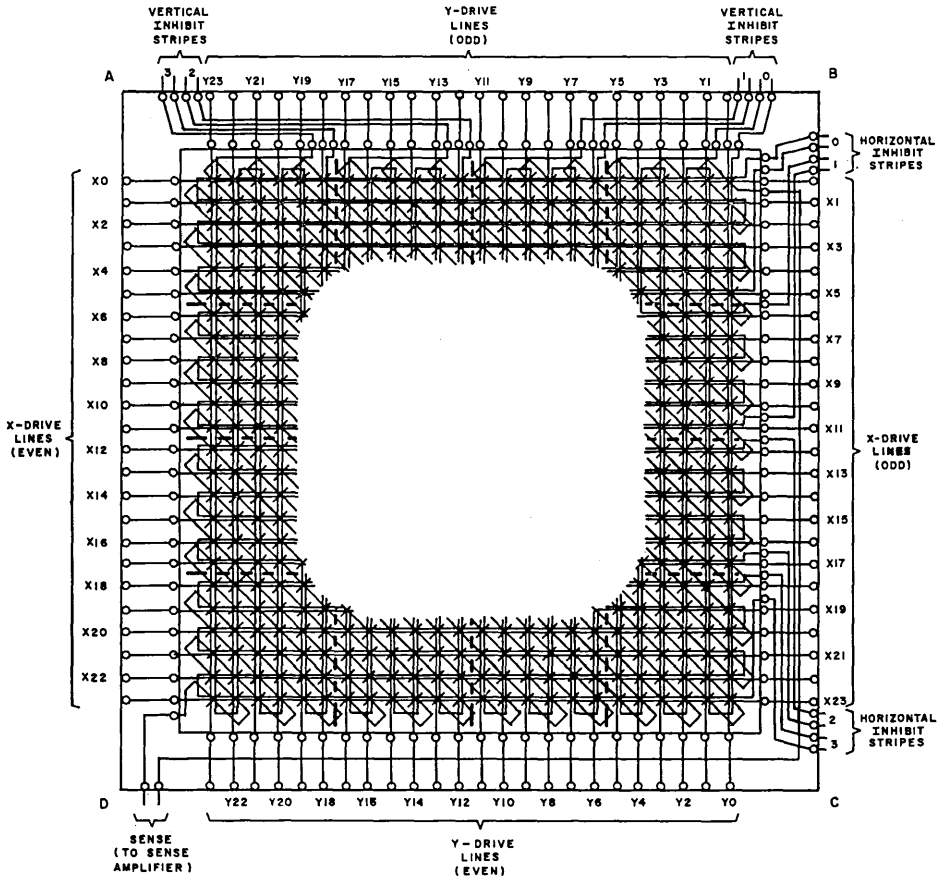


Figure 12. Simplified Storage Plane

STACK

The 18 storage planes are assembled into a stack as shown on the block diagram. A thin metal plate between each plane and on the top and bottom of the stack provides shielding and acts as a cold plate for cooling.

The x and y drive lines thread through the 18 planes as shown in Figure 13. The drive lines connect back to the drive deck. Each drive deck connects to 32 drive lines on the two sides of the stack as shown on the block diagram. The x and y drive decks are identical. The y drive deck mounts on the top of the stack and the x drive on the bottom.

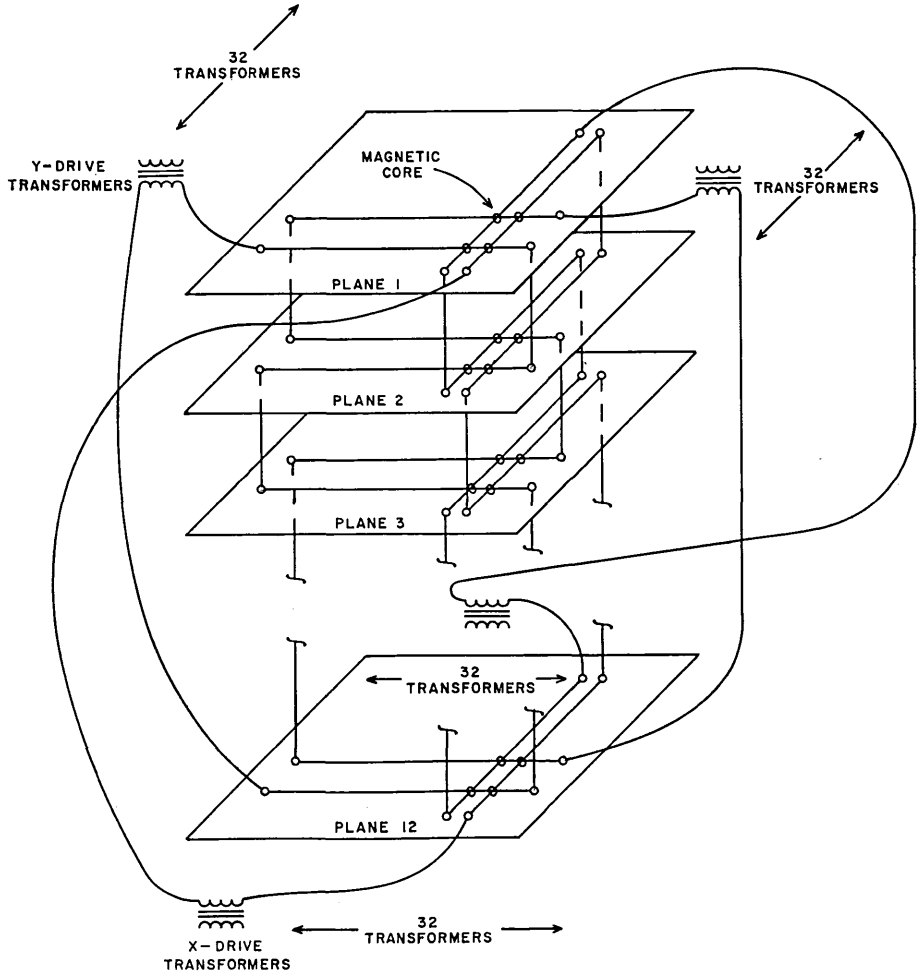


Figure 13. X and Y Drive Lines

Consecutively numbered planes in the top half (nine planes) of the stack are rotated 90° in respect to each other. For example, plane 1 is rotated 90° counterclockwise in respect to plane 0, etc. The bottom nine planes are also rotated 90° in respect to each other. In this half, plane 16 is rotated 90° in respect to plane 17. The rotation of planes gives a balance of connections at the corners of the stack.

One inhibit deck is mounted on each side of the stack and connects to the corners of the planes according to the horizontal and vertical stripe connection terminals at the corners (caused by the rotation of the planes). For example, vertical inhibit stripes 0 and 1 connect at corner B for planes 0, 1, 4, 5, 8, etc. Vertical inhibit stripes 2 and 3 connect to corner A for the same planes. Thus, inhibit deck V21-2 connects to corners A and B for those planes as shown on the block diagram. The two types of inhibit decks (V21 and V20) differ only in the order of the inhibit stripes in the planes to which they connect.

DRIVE DECKS

One drive deck supplies current to the x drive lines, and the other deck supplies current to the y drive lines. The two decks are identical.

A deck has two printed circuit boards with printed wiring on both surfaces of the board. Components are mounted on and between the boards.

A deck contains a read and write current source and circuits to select each of the 64 drive lines.

INHIBIT DECK

The four inhibit decks supply current to the horizontal and vertical inhibit lines. The inhibit decks are two types (V21 and V22), and differ only in printed wiring layout.

Inhibit lines on a plane are arranged in four 16-line groups in horizontal and vertical directions. Each deck has six current sources and circuits to select one of four groups on nine planes.

ADDRESS SELECTION

The address at which a storage reference takes place is determined by the 15 bits in the S register. The address is transmitted to the S register from the Y register at the beginning of the storage reference. The address in the S register remains effective throughout the storage reference.

Bits 12, 13, and 14 of the address select the one of eight (maximum storage option) banks. If an attempt is made to reference a storage bank that is not plugged in, the same address is referenced in another bank that is plugged in. This wrap-around storage feature of the 1700 is described in detail in the S register description (page 81).

The low-order 12 bits of the address select one of 64 x drive lines and one of 64 y drive lines during the read and write phases of the storage reference. Bits 0-5 select the y drive line, and bits 6-11 select the x drive line.

In the y drive line selection, bits 1, 2, and 3 of the address select one of eight current source transformers on the y drive deck. Bits 0, 4, and 5 select one of eight current diverter circuits. The combination of these two selections selects one of 64 drive transformers on the y drive deck which transmits the read and write current pulses through the corresponding y drive line. The selection of the x drive line functions in an identical manner in the x drive deck with bits 7, 8, and 9 and bits 6, 10, and 11 respectively.

Bits 4 and 5 of the address also select one of four inhibit stripes on inhibit decks V20-2 and V21-2. Thus, these inhibit decks select one of four vertical inhibit stripes on the corresponding planes. Bits 10 and 11 perform an identical function in inhibit decks V20-1 and V21-1, selecting one of four horizontal inhibit stripes.

Z REGISTER

The sense line from each plane connects to a corresponding sense amplifier circuit. The sense amplifier circuit detects the switching of a core from the "1" to the "0" state. During the read phase of each storage reference, the output of the sense amplifiers transfers to the Z register. Thus, in the read phase, the Z register contains the word read from the stack.

In storage Read operations, the word in the Z register is later transferred to the X register. The word in the Z register is then restored in the storage stack at the selected address during the write phase.

In storage Write operations, the word in the Z register is replaced by the word transferred from the X register. The new word in the Z register is then stored at the selected address during the write phase.

TIMING AND CONTROL

The timing and control circuit receives input Request Storage and Write signals from the external storage and computer accesses. The timing and control circuit, in conjunction with the timing chain, then synchronizes and controls the entire storage reference operations, such as read, write, and inhibit timing. The timing and control circuit also performs such operations as bank selection, priority control between the external and computer storage requests, and transmitting the Resume signal which releases the computer or external accesses.

STORAGE BANK CONNECTORS

Each storage bank connects to the input, output, and control logic through four 30-pin connectors. Thus, a storage stack simply plugs into the corresponding connectors on the chassis. The connectors are identified according to the same chassis coordinate system as the logic connectors. Inputs and outputs from the stack are shown on the logic diagrams in this manner. For example, the output of pin 14 on the V17 module at C23 (page 42) lists the destination as H08-9. Thus, this output connects to connector H8, pin 9.

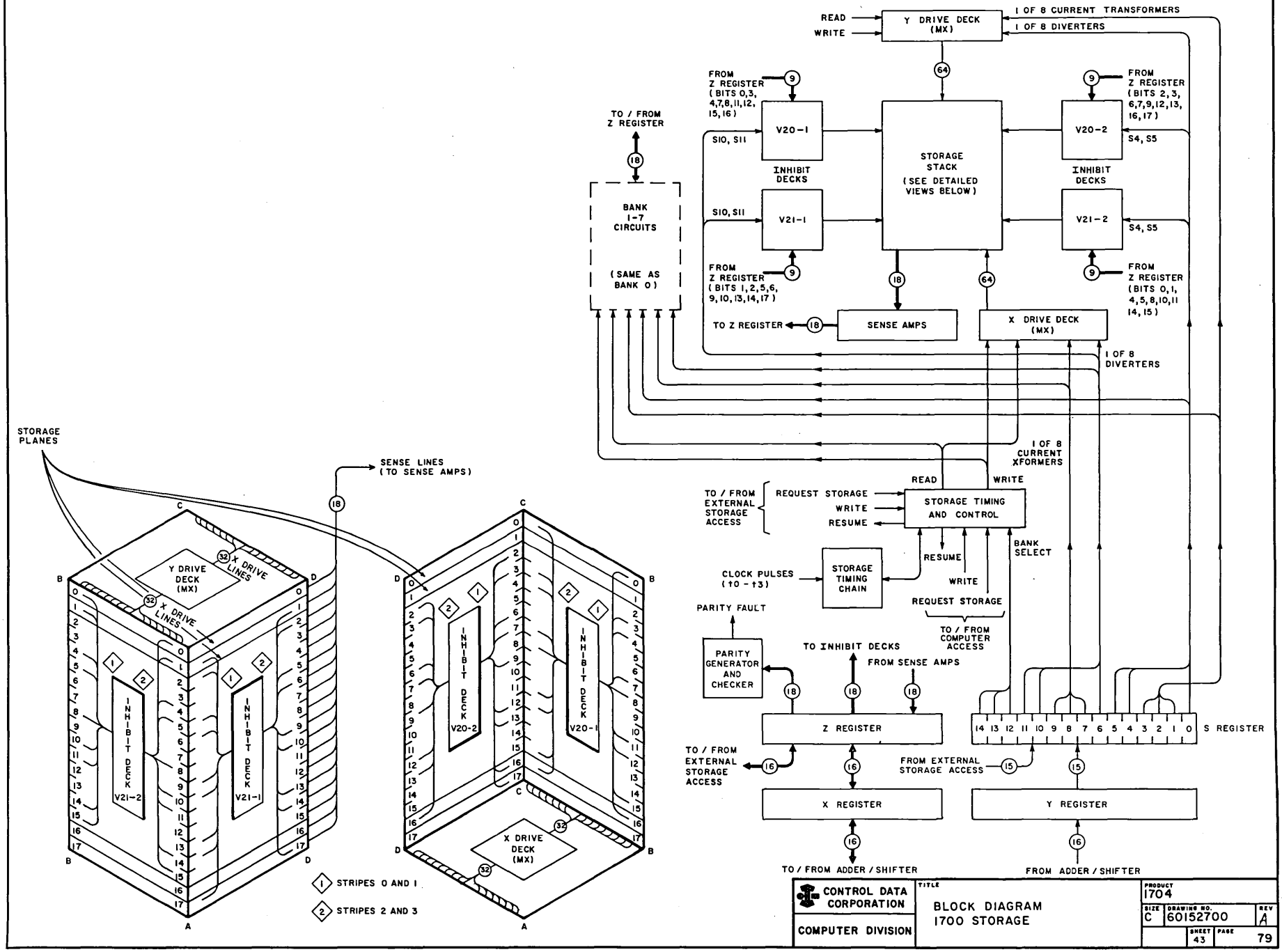
The storage module connector format is listed in Table 3. The table shows the format for bank 0. The format for the other banks is the same.

TABLE 3. 18-BIT STORAGE MODULE CONNECTOR FORMAT

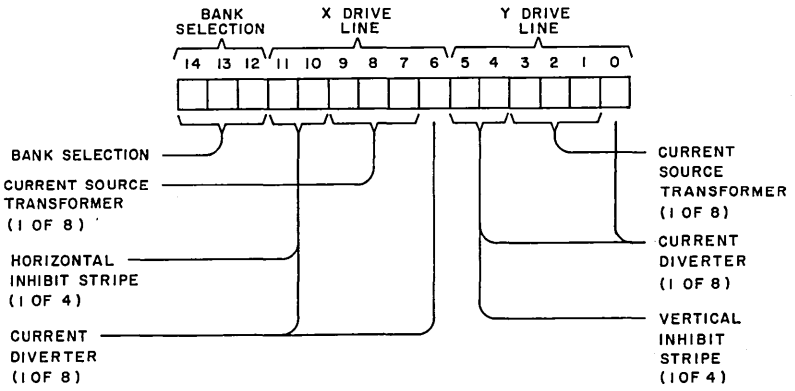
	J1	J2	J3	J4		J1	J2	J3	J4
PIN	H8	H7	H2	H1	PIN	H8	H7	H2	H1
1	Z^1	*Sense 3	J3-3	*Sense 11	16	Ground	J2-14	S^{10} I	S^8
2	*Sense 12	J2-4	*Sense 0	Z^2	17	$\overline{\text{Read}}$	Mass Inhibit Adjustment	J3-19	
3	Z^5	*Sense 3	J3-1	*Sense 11	18	**Adapter +4.5v	J2-20	S^{11} I	S^9
4	*Sense 12	J2-2	*Sense 0	Z^6	19	$\overline{\text{Write}}$	*Sense 9	J3-17	Ground
5	Z^{10}	*Sense 7	J3-7	*Sense 15	20	**Adapter +4.5v	J2-18	S^{10}	S^0
6	*Sense 16	J2-8	*Sense 4	Z^9	21	Z^{15}	*Sense 9	J3-23	+16v Drive
7	Z^{14}	*Sense 7	J3-5	*Sense 15	22	+6v (Drive)	+6v Inhibit V21B #1	S^{11}	S^1
8	*Sense 16	J2-6	*Sense 4	Z^{13}	23	Z^{11}	*Sense 6	J3-21	*Sense 14
9	S^4	S^4 I	J3-11		24	*Sense 17	+8v Inhibit	*Sense 5	Z^{16}
10	Master Reset	J2-12	*Sense 8	Z^{17}	25	Z^8	*Sense 6		*Sense 14
11	S^5	S^5 I	J3-9		26	*Sense 17	+8v Inhibit	*Sense 5	Z^{12}
12	Master Reset	J2-10	*Sense 8	S^2	27	Z^4	*Sense 2	Mass Drive Adjustment	*Sense 10
13	S^6	Ground	J3-15	Core Protect	28	*Sense 13	Overload disable	*Sense 1	Z^7
14	+6v Inhibit V21B #2	J2-16	Ground	S^3	29	Z^0	*Sense 2	Mass Drive Adjustment	*Sense 10
15	S^7	Mass Inhibit Adjustment	J3-13	Core Protect	30	*Sense 13	Overload disable	*Sense 1	Z^3

*Indicates twisted pair

**Storage module tester input


READ
WRITE
Y DRIVE DECK (MX)
1 OF 8 CURRENT TRANSFORMERS
1 OF 8 DIVERTERS
64
FROM Z REGISTER (BITS 0,3, 4,7,8,11,12, 15,16)
9
V20-1
SI0, SI1
INHIBIT DECKS
TO / FROM Z REGISTER
18
BANK 1-7 CIRCUITS
(SAME AS BANK 0)
V21-1
FROM Z REGISTER (BITS 1,2,5,6, 9,10,13,14,17)
STORAGE STACK (SEE DETAILED VIEWS BELOW)
FROM Z REGISTER (BITS 2,3, 6,7,9,12,13, 16,17)
V20-2
S4, S5
V21-2
FROM Z REGISTER (BITS 0,1, 4,5,8,10,11 14,15)
TO Z REGISTER
SENSE AMPS
X DRIVE DECK (MX)
1 OF 8 DIVERTERS
1 OF 8 CURRENT XFORMERS
STORAGE PLANES
SENSE LINES (TO SENSE AMPS)
Y DRIVE DECK (MX)
32
X DRIVE LINES
INHIBIT DECK V20-2
INHIBIT DECK V21-2
INHIBIT DECK V21-1
INHIBIT DECK V20-1
X DRIVE DECK (MX)
1 STRIPES 0 AND 1
2 STRIPES 2 AND 3
TO / FROM EXTERNAL STORAGE ACCESS
REQUEST STORAGE
WRITE
RESUME
STORAGE TIMING AND CONTROL
BANK SELECT
CLOCK PULSES (t0 - t3)
STORAGE TIMING CHAIN
PARITY FAULT
PARITY GENERATOR AND CHECKER
TO INHIBIT DECKS
FROM SENSE AMPS
TO / FROM COMPUTER ACCESS
Z REGISTER
S REGISTER
14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
FROM EXTERNAL STORAGE ACCESS
15
16
X REGISTER
Y REGISTER
TO / FROM ADDER / SHIFTER
FROM ADDER / SHIFTER
CONTROL DATA CORPORATION
COMPUTER DIVISION
TITLE
BLOCK DIAGRAM
1700 STORAGE
PRODUCT
1704
SIZE
C
DRAWING NO.
60152700
REV
A
SHEET
43
PAGE
79

The 15-bit S register contains the address of the current storage reference. The bit format of the S register is shown below.



The high-order three bits select the storage bank; bits 6-11 select the x drive line; and bits 0-5 select the y drive line. In addition, bits 4 and 5 select the vertical inhibit stripe, and bits 10 and 11 select the horizontal inhibit stripe.

The S register is contained on four V17 modules. The bit positions are arranged on the V17 modules for the convenience of the format shown above. Thus, each module contains two of the low-order drive-line bits, one of the inhibit-stripe bits, and one of the bank-selection bits. The high-order bit positions on the V17 module at D27 are not connected since there are only three bank-selection bits. The outputs of the low-order three bits on each module and the corresponding fan-out modules go to the drive and inhibit decks where the address and inhibit stripe selection is made. The output of the bank-selection bits connects to the inputs of bank-selection module 1 (Z80).

The S register receives inputs from the 1705 external channel through the Address Receiver modules or from the computer Y register. The address is transferred to the S register approximately 75 nsec after the initiation of storage. The external channel active enable or the computer channel active enable from storage timing and control gates the respective input into the S register stages through the inverters on the V17 modules.

BANK SELECTION

Bits 12, 13, and 14 determine the storage bank selection. The Z80 modules perform the bank selection. The selection of a given bank by the corresponding Z80 module enables the Read and Write (R and W) drive signals to only that storage bank.

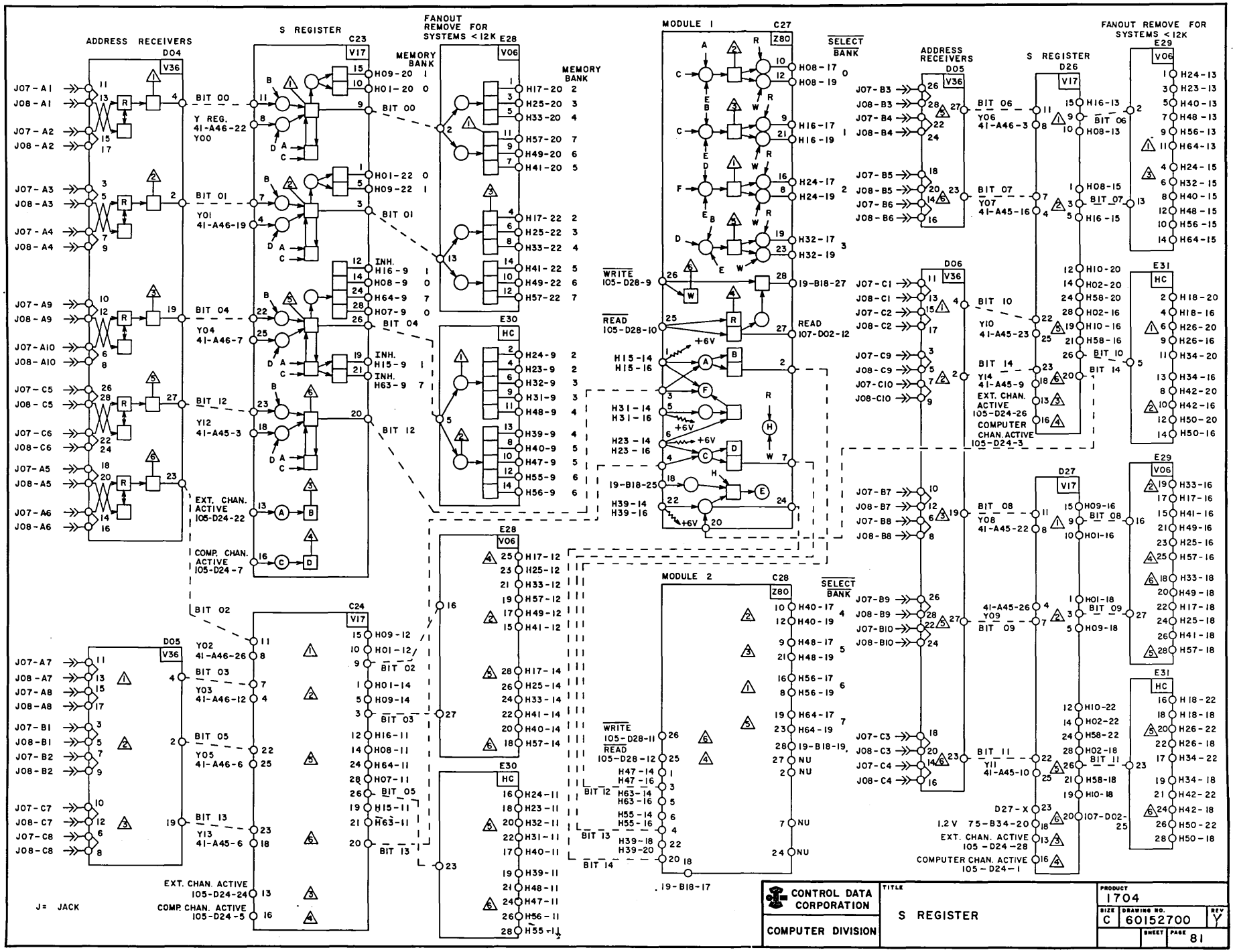
The bank selection circuit performs a wrap-around function in bank selection. For example, if the bank-designator bits attempt to select a storage bank not included in a particular system, the bank selection circuit selects an existing bank according to a fixed order of selection. The table below lists each possible storage option size, the corresponding module and pin connections, and the storage bank selected for a given bank designation.

If a particular module size does not exist in a system, pins 5, 6, 22 and 1 receive +1.2v ("0") inputs. If the banks exist, the pins receive a grd ("1") input. The input pins are grounded on the storage module connectors. For any storage bank option less than 20K, Z80 module 2 is removed.

As an example of storage bank selection, assume a bank designator of 6 and a storage size of 20K. In this case, pins 5, 6, 22 and 1 in module 1 are grounded ("1" inputs). In module 2, pin 1 is grounded and pins 5, 6 and 22 receive "0" inputs (banks 5, 6, and 7 are not plugged in). Since the bank designator is 6, pins 14, 13, and 12 on module 1 receive 110 inputs respectively. As a result all bank selection outputs of module 1 are disabled. In bank selection, a "1" output of the Z80 module disables the selection of the corresponding bank. The ACE AND input in module 2 enables the following R and W signals to pass through the output inverters for pins 27 and 28. These outputs provide Read and Write drive currents for bank 4, according to the table below.

BANK SELECTION TABLE

STORAGE SIZE	REMOVE MODULE	IN MOD 1 GND PIN	IN MOD 2 GND PIN	ORDER OF BANK ACCESS BANK DESIG. 0 1 2 3 4 5 6 7
4K	2			0 0 0 0 0 0 0 0
8K	2	1		0 1 0 1 0 1 0 1
12K	2	1, 6		0 1 2 2 0 1 2 2
16K	2	1, 5, 6		0 1 2 3 0 1 2 3
20K		1, 5, 6, 22	22	0 1 2 3 4 4 4 4
24K		1, 5, 6, 22	1, 22	0 1 2 3 4 5 4 5
28K		1, 5, 6, 22	1, 6, 22	0 1 2 3 4 5 6 6
32K		1, 5, 6, 22	1, 5, 6, 22	0 1 2 3 4 5 6 7


ADDRESS RECEIVERS
D04
V36
S REGISTER
C23
V17
FANOUT REMOVE FOR SYSTEMS < 12K
E28
V06
MEMORY BANK
MODULE 1
C27
Z80
SELECT BANK
ADDRESS RECEIVERS
D05
V36
S REGISTER
D26
V17
FANOUT REMOVE FOR SYSTEMS < 12K
E29
V06
J07-A1
J08-A1
J07-A2
J08-A2
J07-A3
J08-A3
J07-A4
J08-A4
J07-A9
J08-A9
J07-A10
J08-A10
J07-C5
J08-C5
J07-C6
J08-C6
J07-A5
J08-A5
J07-A6
J08-A6
BIT 00
BIT 01
BIT 04
BIT 12
BIT 02
BIT 03
BIT 05
BIT 13
Y REG. 41-A46-22 Y00
Y01 41-A46-19
Y04 41-A46-7
Y12 41-A45-3
Y02 41-A46-26
Y03 41-A46-12
Y05 41-A46-6
Y13 41-A45-6
EXT. CHAN. ACTIVE 105-D24-22
COMP. CHAN. ACTIVE 105-D24-7
EXT. CHAN. ACTIVE 105-D24-24
COMP. CHAN. ACTIVE 105-D24-5
J= JACK
H09-20 1
H01-20 0
H17-20 2
H25-20 3
H33-20 4
H57-20 7
H49-20 6
H41-20 5
H01-22 0
H09-22 1
H17-22 2
H25-22 3
H33-22 4
H41-22 5
H49-22 6
H57-22 7
INH. H16-9 1
H08-9 0
H64-9 7
H07-9 0
INH. H15-9 1
INH. H63-9 7
H24-9 2
H23-9 2
H32-9 3
H31-9 3
H48-9 4
H39-9 4
H40-9 5
H47-9 5
H55-9 6
H56-9 6
H09-12
H01-12
H01-14
H09-14
H16-11
H08-11
H64-11
H07-11
H15-11
H63-11
H17-12
H25-12
H33-12
H57-12
H49-12
H41-12
H17-14
H25-14
H33-14
H41-14
H40-14
H57-14
H24-11
H23-11
H32-11
H31-11
H40-11
H39-11
H48-11
H47-11
H56-11
H55-11
H08-17 0
H08-19
H16-17 1
H16-19
H24-17 2
H24-19
H32-17 3
H32-19
WRITE 105-D28-9
READ 105-D28-10
19-B18-27
READ 107-D02-12
H15-14
H15-16
H31-14
H31-16
H23-14
H23-16
19-B18-25
H39-14
H39-16
+6V
MODULE 2
C28
Z80
SELECT BANK
WRITE 105-D28-11
READ 105-D28-12
H47-14
H47-16
H63-14
H63-16
H55-14
H55-16
H39-18
H39-20
BIT 12
BIT 13
BIT 14
19-B18-17
H40-17 4
H40-19
H48-17 5
H48-19
H56-17 6
H56-19
H64-17 7
H64-19
19-B18-19
NU
J07-B3
J08-B3
J07-B4
J08-B4
J07-B5
J08-B5
J07-B6
J08-B6
J07-C1
J08-C1
J07-C2
J08-C2
J07-C9
J08-C9
J07-C10
J08-C10
J07-B7
J08-B7
J07-B8
J08-B8
J07-B9
J08-B9
J07-B10
J08-B10
J07-C3
J08-C3
J07-C4
J08-C4
BIT 06
BIT 07
BIT 10
BIT 14
BIT 08
BIT 09
BIT 11
Y06 41-A46-3
Y07 41-A45-16
Y10 41-A45-23
Y14 41-A45-9
Y08 41-A45-22
41-A45-26 Y09
Y11 41-A45-10
EXT. CHAN. ACTIVE 105-D24-26
COMPUTER CHAN. ACTIVE 105-D24-3
D27-X
1.2V 75-B34-20
EXT. CHAN. ACTIVE 105-D24-28
COMPUTER CHAN. ACTIVE 105-D24-1
H08-13
H16-15
H08-15
H16-13
H10-20
H02-20
H58-20
H02-16
H10-16
H58-16
H10-22
H02-22
H58-22
H02-18
H58-18
H10-18
H09-16
H01-16
H01-18
H09-18
H107-D02-25
E31
HC
H18-20
H18-16
H26-20
H26-16
H34-20
H34-16
H42-20
H42-16
H50-20
H50-16
H33-16
H17-16
H41-16
H49-16
H25-16
H57-16
H33-18
H49-18
H17-18
H25-18
H41-18
H57-18
H18-22
H18-18
H26-22
H26-18
H34-22
H34-18
H42-22
H42-18
H50-22
H50-18
CONTROL DATA CORPORATION
COMPUTER DIVISION
TITLE
S REGISTER
PRODUCT 1704
SIZE C
DRAWING NO. 60152700
REV Y
SHEET
PAGE 81

Z REGISTER

The Z register serves as an intermediate storage for data being read from storage or being written into storage. The 18-bit Z register is contained on nine V47 modules. The Z register and associated input and control logic is shown on pages 83 through 99. Except where specifically noted in the text, the following description of the Z register is based on stages 0 and 1.

READ OPERATION

The Z register receives inputs from the sense amplifiers on the read phase at approximately 475 nsec of the storage cycle. At this time, the output of inverter B gates the output of the sense amplifiers from the selected bank into Z. If a particular storage bank option (2-7) is present, the corresponding input to the Z register or V84 fan-in module is grounded. For example, if bank 4 is plugged in, pin 14 is grounded ("1") causing C to enable the output of the bank 4 sense amplifiers. If a bank is not present, the corresponding input pins receive "0" inputs since the sense amplifier modules for that bank are not included with the system.

Sense Amplifiers

The sense amplifiers for each bank are contained on three V02 modules. Each V02 module contains six sense amplifier stages. If a storage bank option is not included, the corresponding V02 modules are not plugged into the chassis.

The detection of a core switching from a "1" to a "0" in a storage plane induces a voltage on the sense line. This voltage appears as a "1" to the two inputs of the corresponding sense amplifier stage. Assuming the "1" was detected in plane 0 and bank 0, stage 0 of the V02 module at E06 produces a "1" output at pin 3. At 475 time of the storage cycle, the Read Strobe gates the "1" output of pin 3 into stage 0 of the Z register.

The Z register diagrams show only the sense amplifier stages for banks 0 and 7. The table opposite page 85 lists the locations, test point and output pin information for sense amplifier modules for all storage bank options.

WRITE OPERATION

In a Write operation, the Z register receives inputs from the 1705 direct storage access receivers or the computer X register. If a 1705 option is included in the system, the receiver modules are plugged into the chassis. Thus, if an external storage write request is accepted by storage control, the Receivers → Z signal and the write strobe enable the transfer of the receiver outputs to the Z register at 600 nsec of the storage cycle. If the computer write request is accepted, the X → Z transfer takes place at the same time. Later in the write phase, the "0" bits in the Z register turn on inhibit drive currents for the corresponding planes of the selected bank.

INHIBIT FAN-OUTS

Two inhibit fan-out modules connect to each stage of the Z register. The V87 modules provide inhibit inputs for banks 0 and 1, and the V86 module functions for banks 2 through 7. The Inhibit enable which occurs at 675 nsec of the storage cycle gates the "0" state of the Z register stages to the inhibit decks on all existing banks.

PARITY GENERATOR

The parity generator circuit consists of two V18 modules. Each V18 module generates parity for nine Z register stages. Both modules operate identically. Thus, the following description is based on the V18 module that generates parity for the low-order nine stages.

The V18 module generates parity based on three 3-stage groups. The inverter inputs to each of the three groups examine the contents of the three stages for an odd combination of "1" bits. For example, if stages 0, 1, and 2 of the Z register are all "1's", AND inputs A, C, and E produce a "1" output of S indicating these stages contain an odd number of "1" bits. The output inverters examine the four possible odd combinations of the three groups. Thus, if the nine stages contain an odd number of bits, the corresponding output is a "0". If the nine stages contain an even number of "1" bits, all the outputs are "1's".

STAGES 16 AND 17

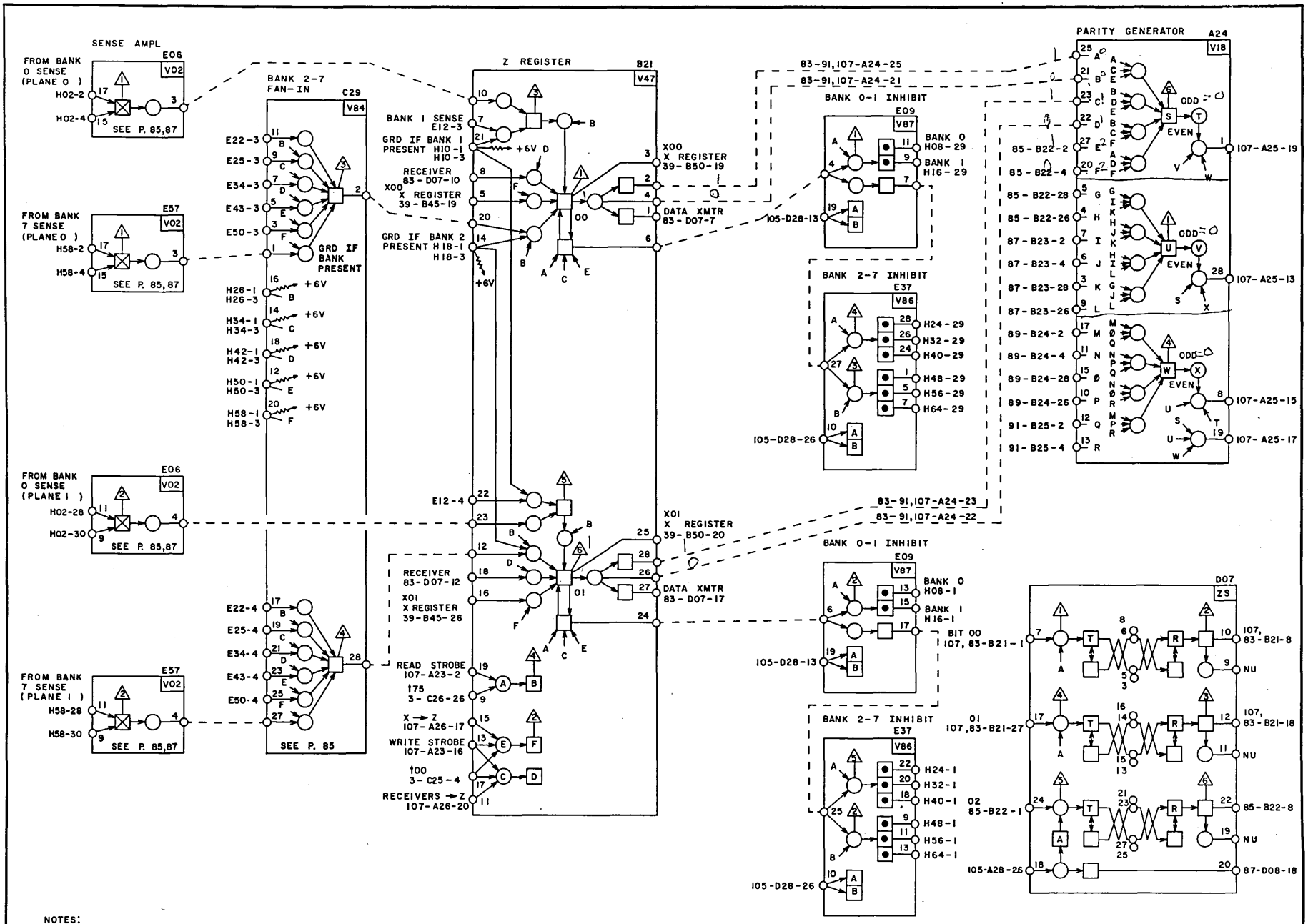
Stages 16 and 17 (page 99) function differently from the other stages. The sense amplifier inputs and control for these stages are the same as for the other stages. However, these stages do not receive inputs from the X register or the external receivers during a Write operation. The parity bit (stage 16) receives no inputs except from the sense amplifiers. However, the program protect bit (stage 17) is set by the following two other conditions:

1. $\overline{\text{(Write Protect)}}$ (t00) (Write Strobe) (Z17 = "1")
2. (Write Protect) (t00) (Write Strobe) $\overline{\text{(F8)}}$

In condition 1, the $\overline{\text{Write Protect}}$ function = (External Write) (External Channel Active) [(External Protect) + $\overline{\text{(External Protect)}}$ (Parity Error) (Storage Protect $\overline{\text{Fault)}}$] + (Computer Channel Active) (Computer Write) [Computer Protect + $\overline{\text{(Computer Protect)}}$ (Parity Error) (Storage Protect Fault)].

In condition 2, the Write Protect function = $\overline{\text{(Parity Error)}}$ $\overline{\text{(Storage Protect Fault)}}$ (Write Protect Bit = "1") (Computer Channel Active). The Write Protect Bit FF is set during the computer REG mode in the SPB or CPB instructions with the $\overline{\text{Interrupt}}$ condition.

Thus, in condition 1, the $\overline{\text{Write Protect}}$ function enables the transfer of the previous state of Z17 back to stage 17 at 600 nsec of the storage cycle. In condition 2, the Write Protect function enables the setting of stage 17 at 600 nsec on a SPB instruction ($\overline{\text{F8}}$).



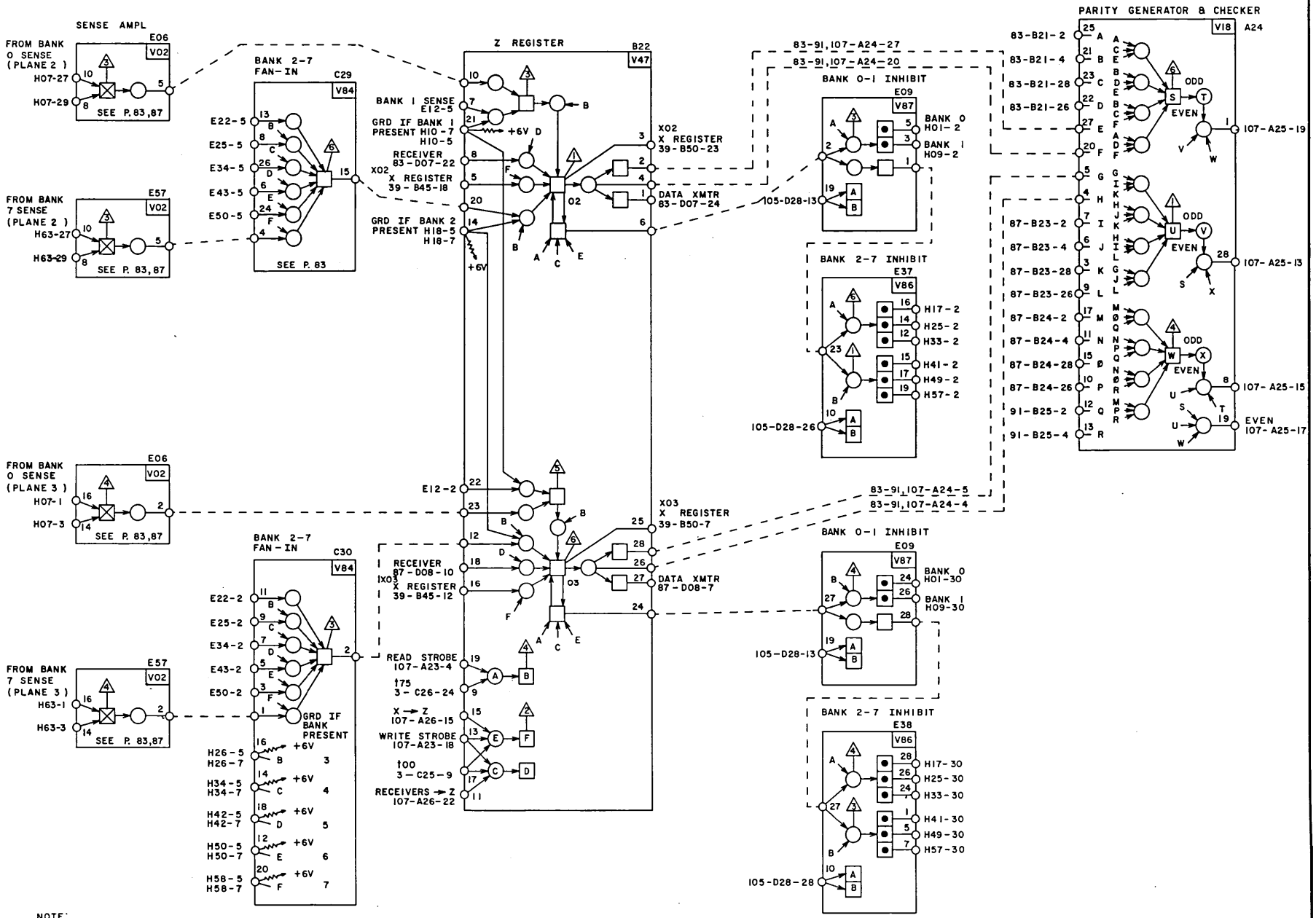
NOTES:

1. ● REPRESENTS LINE DRIVER WITH NO OUTPUT DIODE.
2. SEE OPPOSITE PAGE 87 FOR ZS MODULE CABLING.

CONTROL DATA CORPORATION	TITLE: Z REGISTER (STAGES 0 & 1)	PRODUCT 1704	
COMPUTER DIVISION		SIZE C · DRAWING NO. 60152700 · REV E	
		SHEET · PAGE 83	

TABLE 4. SENSE AMPLIFIER AND DATA RECEIVER-TRANSMITTER LOCATIONS AND TEST POINTS

Bit	DATA Receivers Transmitters					Bank 0			Bank 1			Bank 2			Bank 3			Bank 4			Bank 5			Bank 6			Bank 7			Bit
		Input		Output																									
	Loc.	T. P.	Pin	T. P.	Pin	Loc.	T. P.	Output Pin	Loc.	T. P.	Output Pin	Loc.	T. P.	Output Pin	Loc.	T. P.	Output Pin	Loc.	T. P.	Output Pin	Loc.	T. P.	Output Pin	Loc.	T. P.	Output Pin	Loc.	T. P.	Output Pin	
0	1D07	1	7	2	10	1E06	1	3	1E12	1	3	1E22	1	3	1E25	1	3	1E34	1	3	1E43	1	3	1E50	1	3	1E57	1	3	0
1		4	17	3	12		2	4		2	4		2	4		2	4		2	4		2	4		2	4		2	4	1
2	↓	5	24	6	22		3	5		3	5		3	5		3	5		3	5		3	5		3	5		3	5	2
3	1D08	1	7	2	10		4	2		4	2		4	2		4	2		4	2		4	2		4	2		4	2	3
4		4	17	3	12		5	25		5	25		5	25		5	25		5	25		5	25		5	25		5	25	4
5	↓	5	24	6	22	↓	6	24	↓	6	24	↓	6	24	↓	6	24	↓	6	24	↓	6	24	↓	6	24	↓	6	24	5
6	1D09	1	7	2	10	1E07	1	3	1E13	1	3	1E23	1	3	1E26	1	3	1E35	1	3	1E44	1	3	1E54	1	3	1E58	1	3	6
7		4	17	3	12		2	4		2	4		2	4		2	4		2	4		2	4		2	4		2	4	7
8	↓	5	24	6	22		3	5		3	5		3	5		3	5		3	5		3	5		3	5		3	5	8
9	1D10	1	7	2	10		4	2		4	2		4	2		4	2		4	2		4	2		4	2		4	2	9
10		4	17	3	12		5	25		5	25		5	25		5	25		5	25		5	25		5	25		5	25	10
11	↓	5	24	6	22	↓	6	24	↓	6	24	↓	6	24	↓	6	24	↓	6	24	↓	6	24	↓	6	24	↓	6	24	11
12	1D11	1	7	2	10	1E08	1	3	1E14	1	3	1E24	1	3	1E27	1	3	1E36	1	3	1E45	1	3	1E56	1	3	1E59	1	3	12
13		4	17	3	12		2	4		2	4		2	4		2	4		2	4		2	4		2	4		2	4	13
14	↓	5	24	6	22		3	5		3	5		3	5		3	5		3	5		3	5		3	5		3	5	14
15	1D12	1	7	2	10		4	2		4	2		4	2		4	2		4	2		4	2		4	2		4	2	15
16							5	25		5	25		5	25		5	25		5	25		5	25		5	25		5	25	16
17						↓	6	24	↓	6	24	↓	6	24	↓	6	24	↓	6	24	↓	6	24	↓	6	24	↓	6	24	17



NOTE:

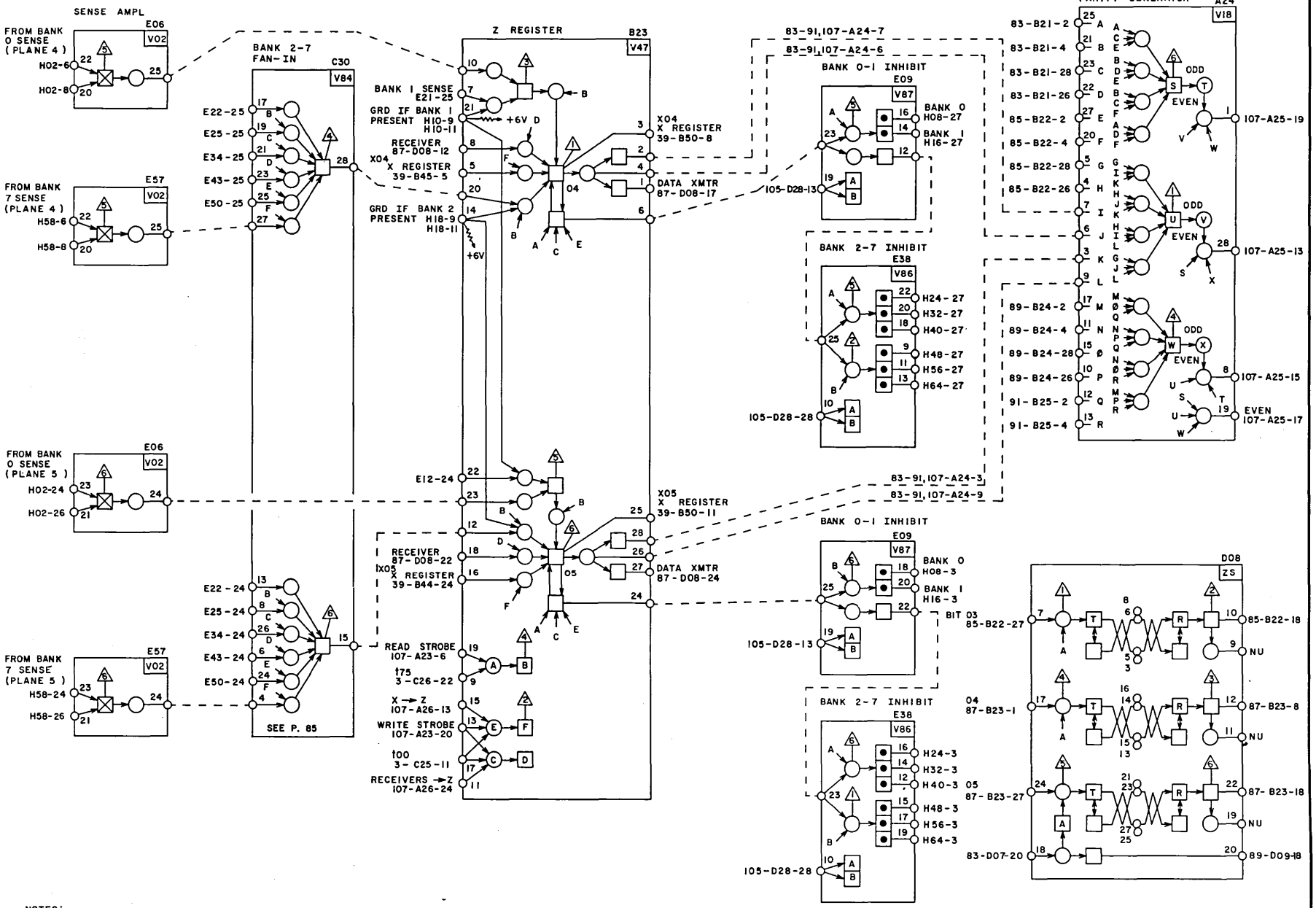
● REPRESENTS LINE DRIVER WITH NO OUTPUT DIODE.

CONTROL DATA CORPORATION	TITLE: Z REGISTER (STAGES 2 & 3)	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C · DRAWING NO.: 60152700 · REV: E	
		SHEET · PAGE: 85	

TABLE 5. ZS MODULE CABLING

Module Location	Pin	Destination	Module Location	Pin	Destination	Module Location	Pin	Destination
D07	3	J06-A2	D08	3	J06-A8	D09	3	J06-B4
	5	J05-A2		5	J05-A8		5	J05-B4
	6	J05-A1		6	J05-A7		6	J05-B3
	8	J06-A1		8	J06-A7		8	J06-B3
	13	J06-A4		13	J06-A10		13	J06-B6
	14	J06-A3		14	J06-A9		14	J06-B5
	15	J05-A4		15	J05-A10		15	J05-B6
	16	J05-A3		16	J05-A9		16	J05-B5
	21	J06-A5		21	J06-B1		21	J06-B7
	23	J05-A5		23	J05-B1		23	J05-B7
	25	J06-A6		25	J06-B2		25	J06-B8
	27	J05-A6		27	J05-B2		27	J05-B8

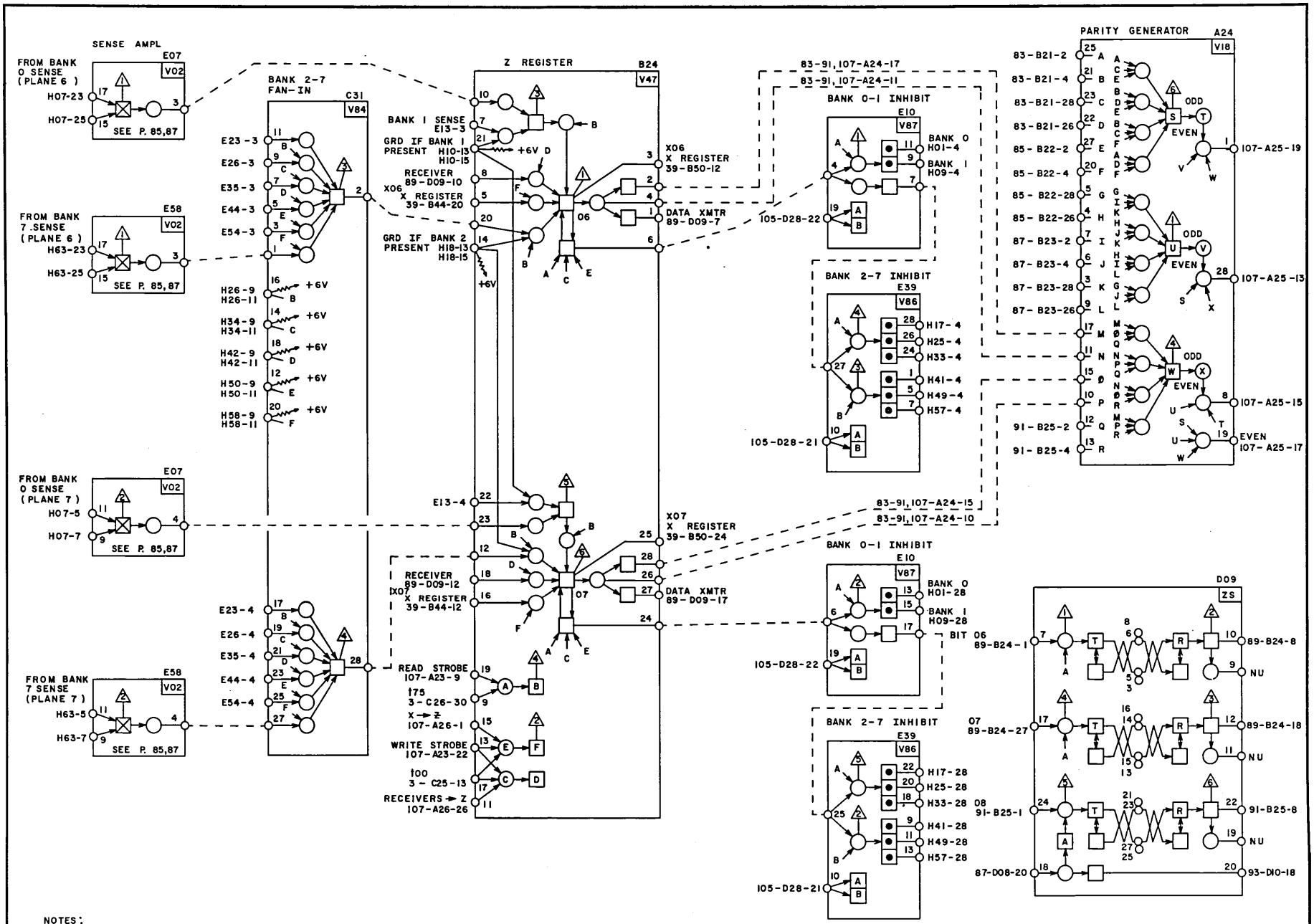
Module Location	Pin	Destination	Module Location	Pin	Destination
D10	3	J06-B10	D11	3	J06-C6
	5	J05-B10		5	J05-C6
	6	J05-B9		6	J05-C5
	8	J06-B9		8	J06-C5
	13	J06-C2		13	J06-C8
	14	J06-C1		14	J06-C7
	15	J05-C2		15	J05-C8
	16	J05-C1		16	J05-C7
	21	J06-C3		21	J06-C9
	23	J05-C3		23	J05-C9
	25	J06-C4		25	J06-C10
	27	J05-C4		27	J05-C10



NOTES:

1. ● REPRESENTS LINE DRIVER WITH NO OUTPUT DIODE.
2. SEE OPPOSITE PAGE 87 FOR ZS MODULE CABLING.

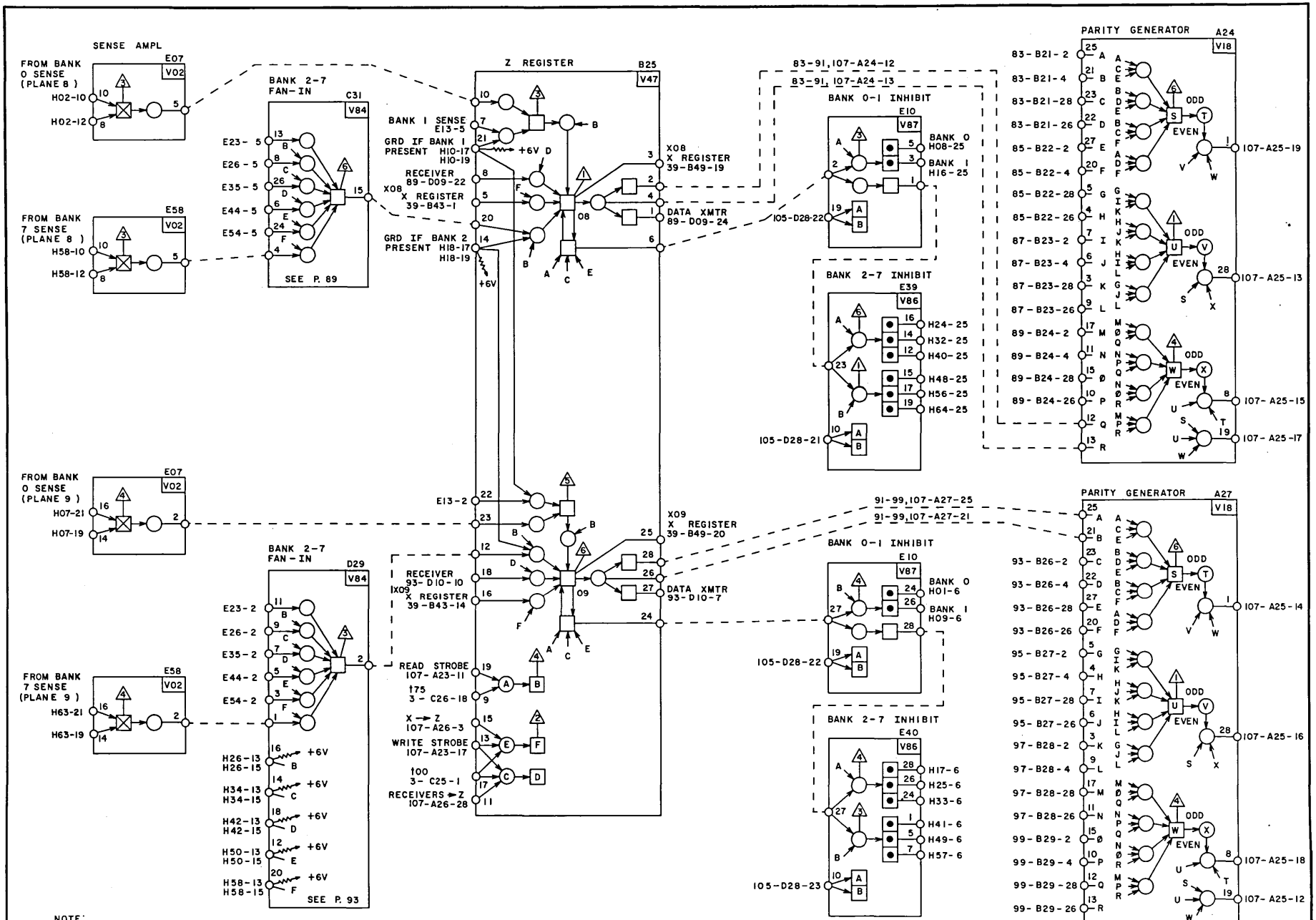
CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE Z REGISTER (STAGES 4 & 5)	PRODUCT 1704 SIZE C · DRAWING NO. 60152700 · REV E SHEET · PAGE 87



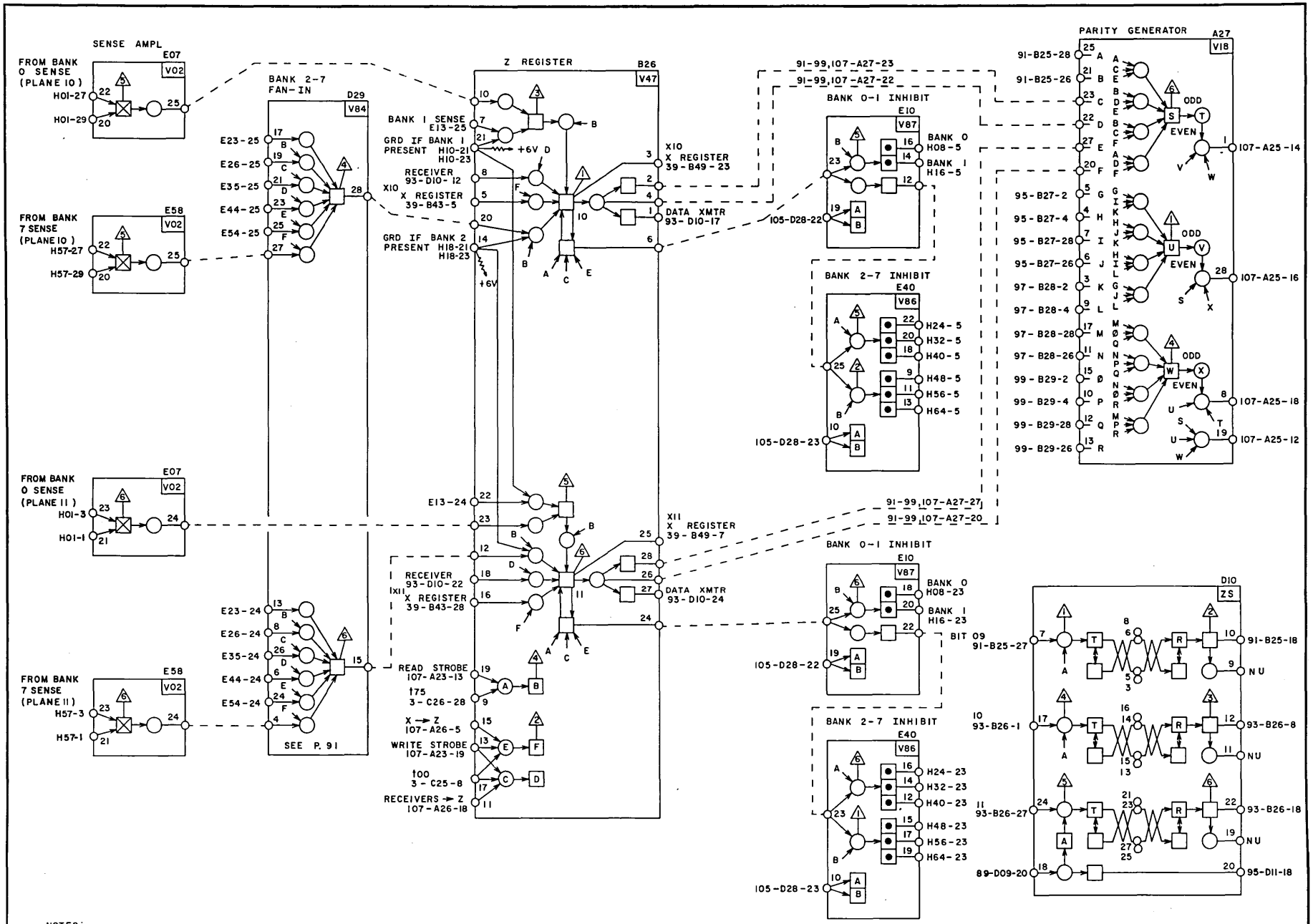
NOTES:

1. ● REPRESENTS LINE DRIVER WITH NO OUTPUT DIODE.
2. SEE OPPOSITE PAGE 87 FOR ZS MODULE CABLING.

CONTROL DATA CORPORATION	TITLE: Z REGISTER (STAGES 6 & 7)	PRODUCT 1704	
COMPUTER DIVISION		SIZE C	DRAWING NO. 60152700 REV
			SHEET PAGE 89



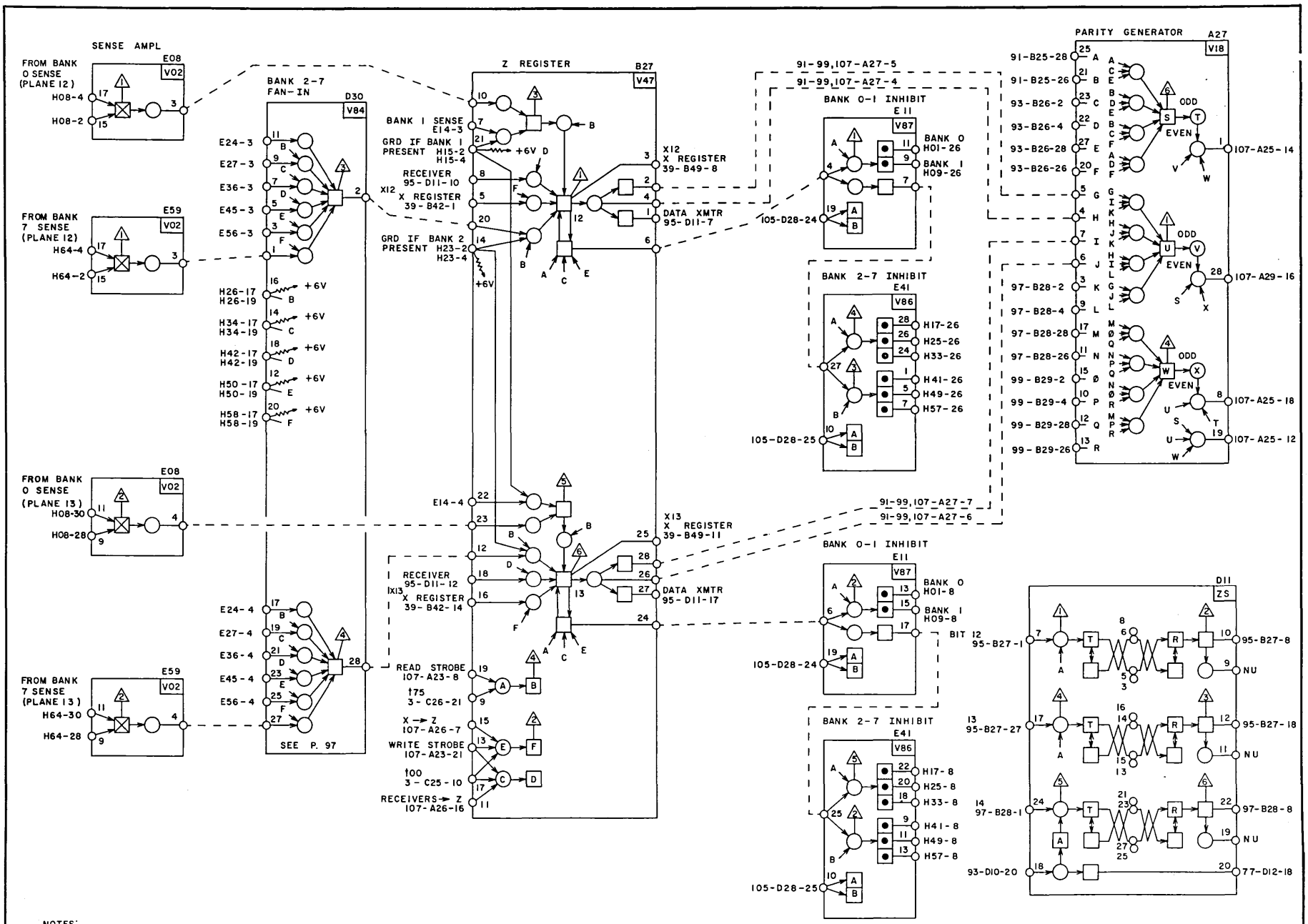
CONTROL DATA CORPORATION	TITLE: Z REGISTER (STAGES 8 & 9)	PRODUCT 1704	
COMPUTER DIVISION		SIZE C · DRAWING NO. 60152700 · REV E	
		SHEET · PAGE 91	



NOTES:

1. ● REPRESENTS LINE DRIVER WITH NO OUTPUT DIODE.
2. SEE OPPOSITE PAGE 87 FOR ZS MODULE CABLING.

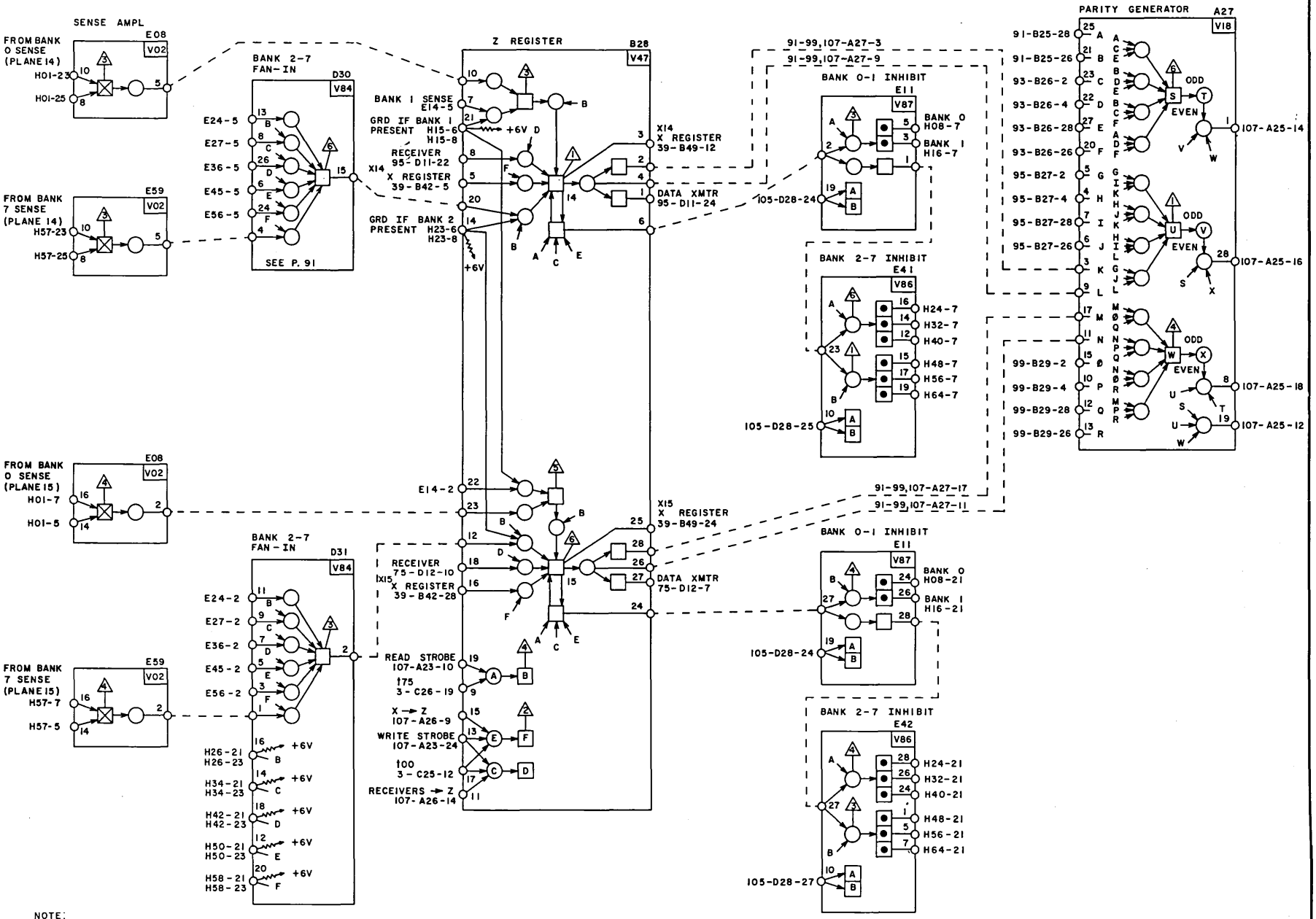
CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE Z REGISTER (STAGES 10 & 11)	PRODUCT 1704 SIZE C · DRAWING NO. 60152700 · REV E SHEET · PAGE 93



NOTES:

1. ▣ REPRESENTS LINE DRIVER WITH NO OUTPUT DIODE.
2. SEE OPPOSITE PAGE 87 FOR ZS MODULE CABLING.

CONTROL DATA CORPORATION	TITLE: Z REGISTER (STAGES 12 & 13)	PRODUCT 1704	
COMPUTER DIVISION		SIZE C · DRAWING NO. 60152700 · REV F	
		SHEET · PAGE 95	



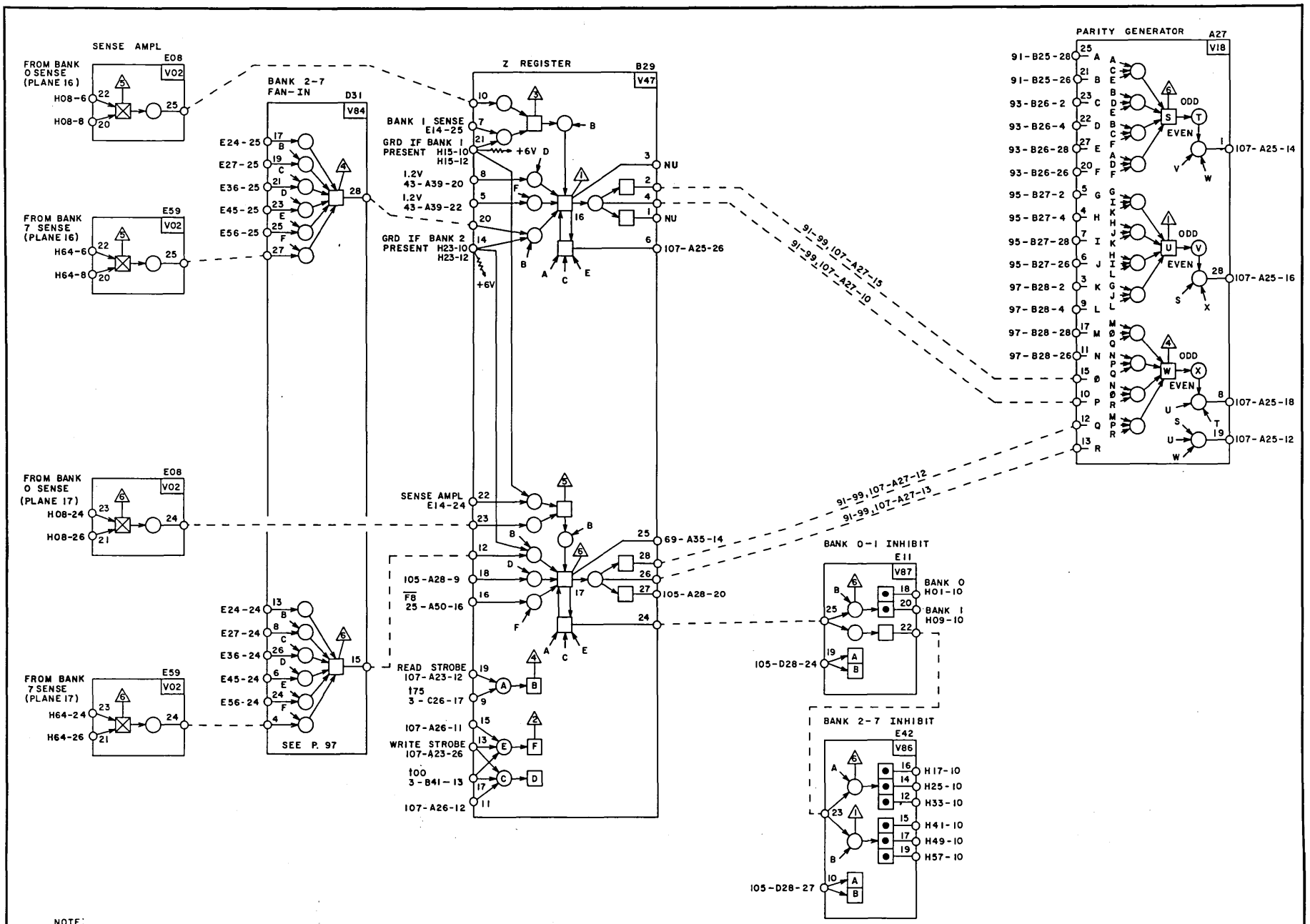
NOTE:

REPRESENTS LINE DRIVER WITH NO OUTPUT DIODE.

CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE: Z REGISTER (STAGES 14 & 15)

PRODUCT 1704
SIZE C | DRAWING NO. 60152700 | REV E
SHEET | PAGE 97



NOTE:

REPRESENTS LINE DRIVER WITH NO OUTPUT DIODE.

CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE Z REGISTER (STAGES 16 & 17)	PRODUCT 1704 SIZE C · DRAWING NO. 60152700 · REV SHEET · PAGE 99	

STORAGE INTERFACE

The storage interface module (V82) provides communication between computer control and storage timing and control. The V82 module contains the request storage, write, protect and parity fault outputs to internal interrupt, Z → X, (Resume) and write protect bit controls.

REQUEST STORAGE

The setting of the Request Storage FF by computer control initiates a complete storage cycle. The Request Storage FF remains set until the computer Resume is issued by storage control at 425 nsec of the storage cycle. A subsequent computer request could then be made. However, a storage cycle is not initiated until the Storage Busy condition is disabled at the end of the complete storage cycle.

The Request Storage FF is set at V050 time of the B cycle if under the following conditions:

$$\overline{(\text{Immediate Operand} + \text{RNI} + \text{Read Index})}$$

WRITE

The Request Storage enable (I) sets the Write FF if a word is to be written in storage. Each Request Storage enable clears Write (H) before probing the set conditions. The Write FF is set on the following conditions:

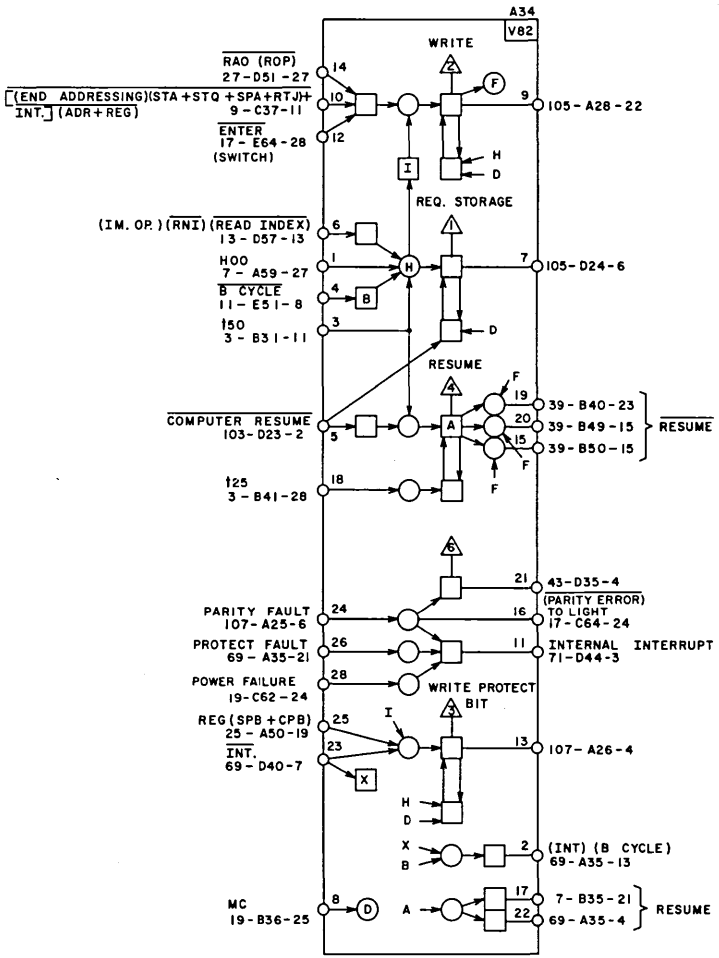
$$(\text{Request Storage})\left[(\text{ADR}+\text{REG})\left[(\text{End Addressing})\,(\text{STA}+\text{STQ}+\text{SPA}+\text{RTJ})+\text{INT}\right]+(\text{RAD})\,(\text{ROP})+\text{Enter}\right]$$

Z → X

The Computer Resume signal sets the Z → X FF at 450 nsec of a storage reference. The actual Z to X register transfer does not take place until 500 nsec. The setting of the Write FF blocks the Z to X transfer through inverter F.

WRITE PROTECT BIT

The Computer Resume signal sets the Write Protect Bit FF in the REG mode of an SPB or CPB instruction if there is no interrupt. The setting of this FF enables the setting of the Protect bit (Z17) on the SPB instruction and the clearing of the Protect bit on the CPB instruction.



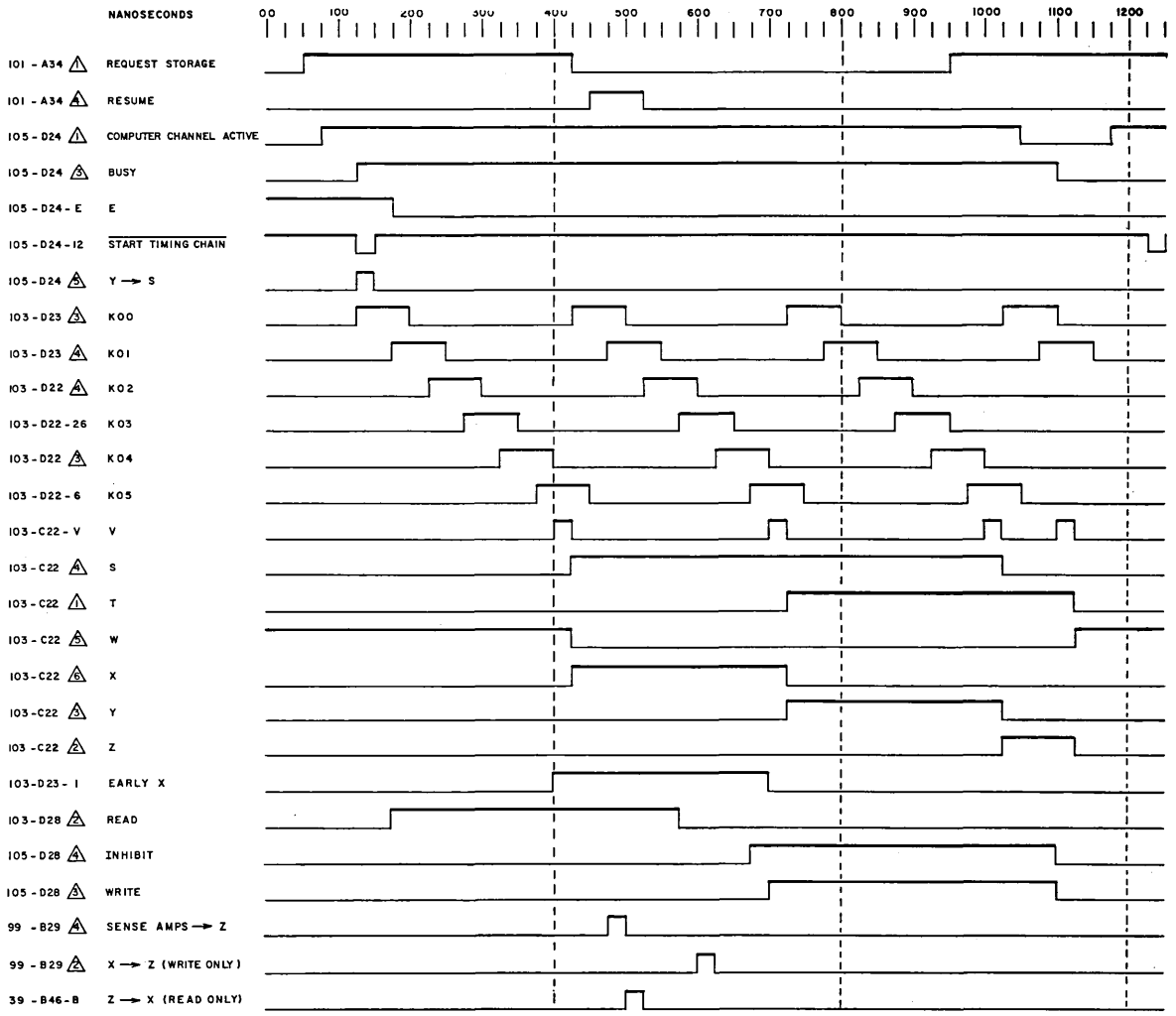
NOTE :
SEE Z→X & REQ. STORAGE (P. 39).

CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE STORAGE INTERFACE	PRODUCT 1704 SIZE C · DRAWING NO. 60152700 · REV — SHEET · PAGE 101

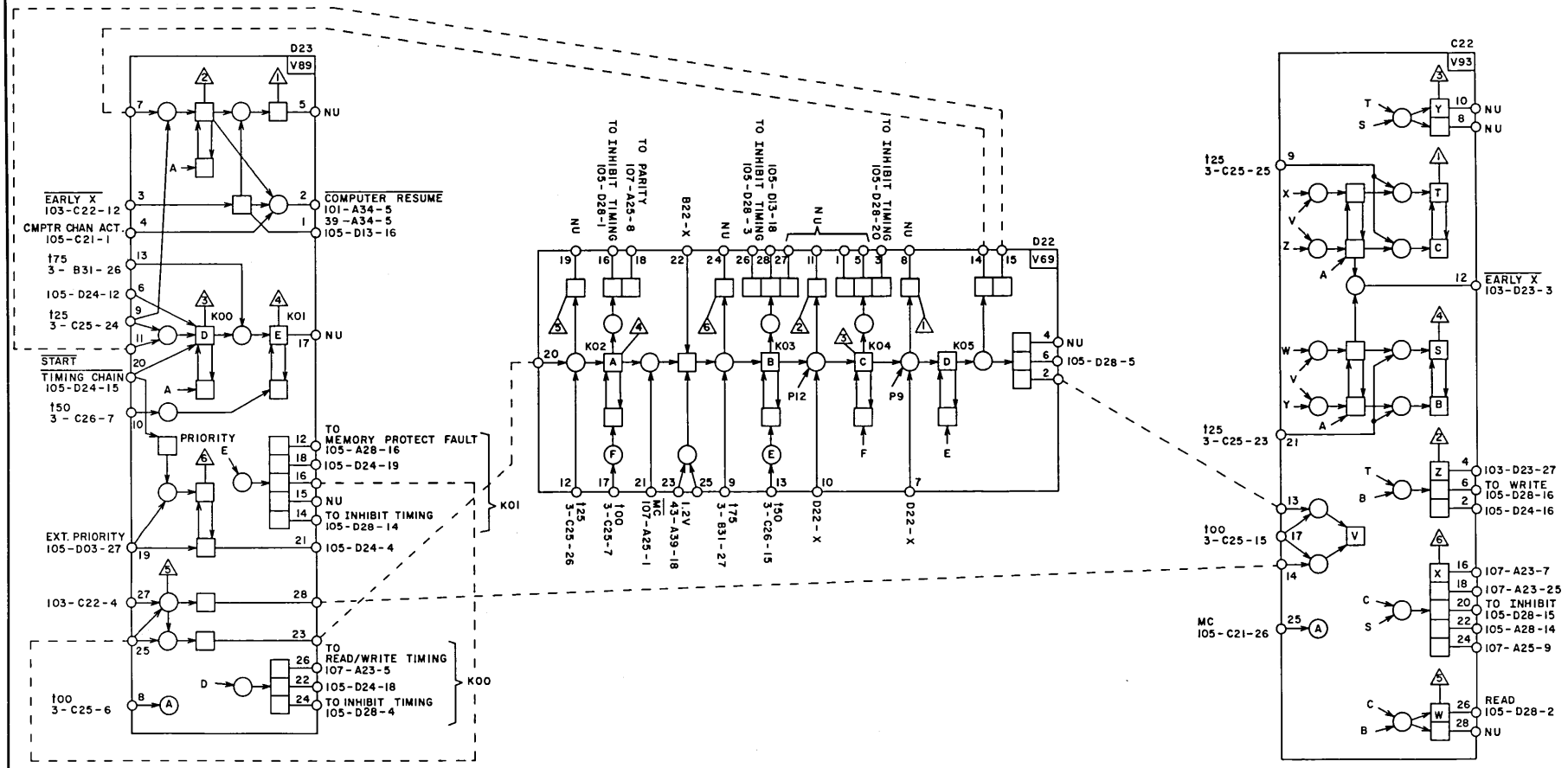
STORAGE TIMING CHAIN

The storage timing chain circuits control the timing sequence of all storage cycle operations. The timing chain is contained on the V69 module with the input and output control circuits on the V89 and V93 modules.

The storage control circuit initiates the operation of the timing chain with the Start Timing Chain signal which sets K00. Flip-flops K00 through K05 sequentially set and clear which produces the basic storage timing sequence. The timing chain goes through three complete sequences for each storage cycle.



NOTES:
1. THE UP PORTION OF ALL WAVEFORMS INDICATES THE "1" STATE OF THE CORRESPONDING SIGNAL OR ENABLE.
2. THE STORAGE SEQUENCE SHOWN ASSUMES A COMPUTER REFERENCE THROUGHOUT. THE EXTERNAL REFERENCE SIGNALS ARE IN THE SAME TIME RELATIONSHIP.



CONTROL DATA CORPORATION	TITLE: STORAGE TIMING CHAIN	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C · DRAWING NO.: 60152700 · REV:	
		SHEET: · PAGE: 103	

The storage timing and control circuit controls such functions as Storage Access, Storage Protect Fault, Read, Write, Inhibit, Parity Bit, and Parity Fault. The timing chain sequences the control functions. The following paragraphs describe each of the main functions listed above with reference to the Storage Timing Chain (page 102).

STORAGE ACCESS CONTROL

Storage access control functions take place on the V90 module. The request storage enable from the computer or external interface sets the corresponding Channel Active FF. The External Channel Active FF is set at t50 time. The Computer Channel Active FF is set at t75 time if the Priority FF (page 103) is not set. The setting of either of the Channel Active FFs starts the timing chain and sets the Busy FF. The Busy FF blocks the Start Timing Chain output and the setting of the Channel Active FFs until Busy is cleared at the end of the present storage reference. The setting of the Channel Active FF enables the gating of the corresponding address and data (Write only) into the S and Z registers respectively.

STORAGE PROTECT FAULT CONTROL

The storage protect fault control is contained on the V94 module. The computer and external write and protect inputs enter this module. The state of the protect bit (Z17) is gated into inverter G at 525 nsec if the computer or external channels are active and the corresponding protect and write inputs are enabled.

If Z17 equals "1", the output of G sets the storage protect fault according to the following conditions:

EXTERNAL

STORAGE PROTECT FAULT = (Z17 = "1") (525 nsec) (EXTERNAL CHANNEL ACTIVE) (EXTERNAL WRITE) ($\overline{\text{EXTERNAL PROTECT}}$)

COMPUTER

STORAGE PROTECT FAULT = (Z17 = "1") (525 nsec) (COMPUTER CHANNEL ACTIVE) (WRITE) [($\overline{\text{INSTRUCTION PROTECTED}}$) ($\overline{\text{PROTECT SWITCH ACTIVE}}$)]

The above equations show that the storage protect fault is detected if either the external or computer accesses attempt to write in a protected address. The setting of the Storage Protect Fault FF blocks the X to Z or Receivers to Z transfer and transmits the storage protect fault enable to the computer.

READ, WRITE, AND INHIBIT CONTROL

The Read, Write, and Inhibit Control FFs enable the corresponding storage phase when set. These FFs are contained on the V91 module. These FFs are set at the proper times in the storage cycle according to the storage timing sequence page 102).

PARITY BIT AND PARITY FAULT CONTROL

The parity bit and fault control is contained on the V95 module (page 107).

Parity Bit Control

The writing of the parity bit in storage depends on the gate new parity enable from the V92 module. A new parity bit is written into storage under the following conditions:

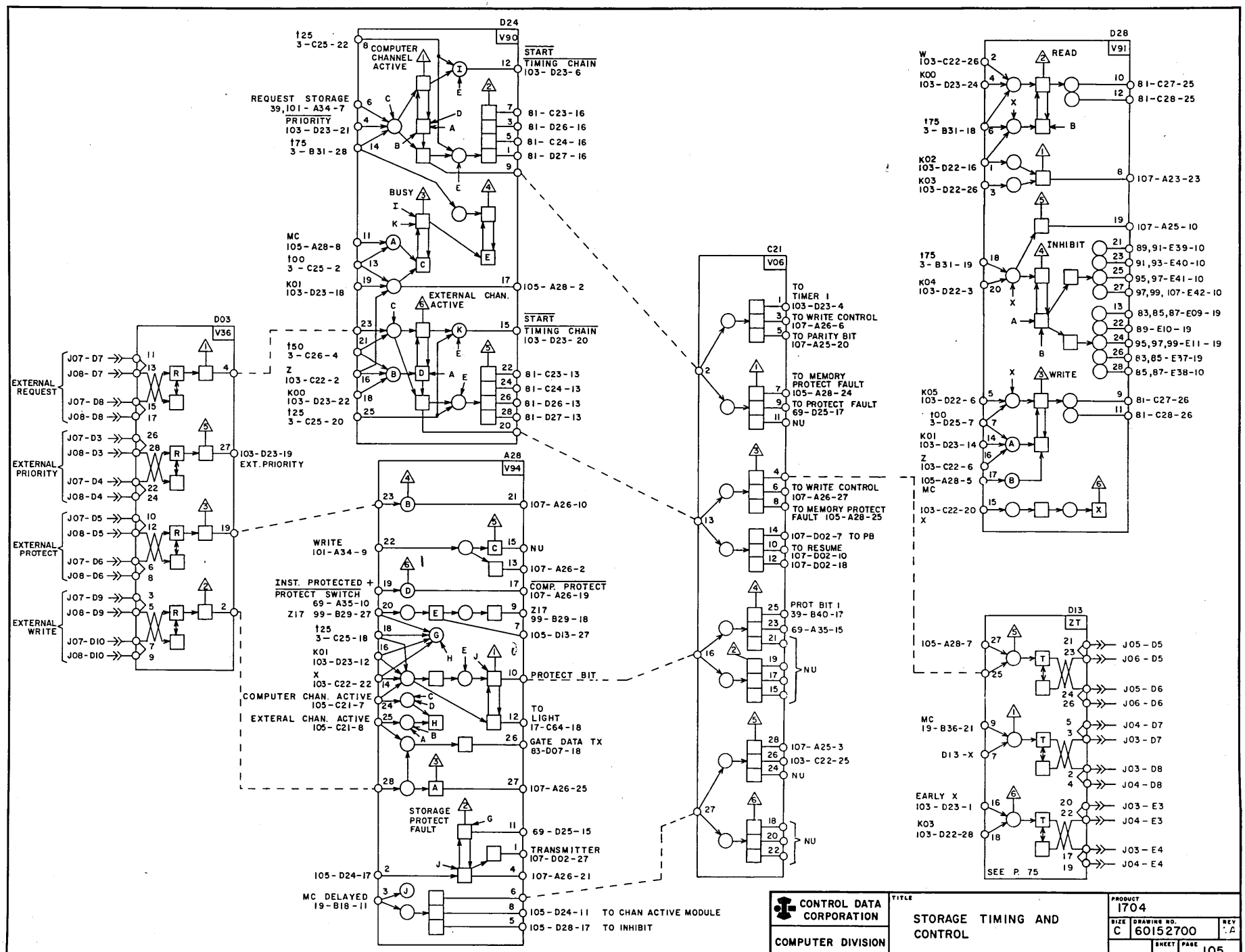
GATE NEW PARITY = [EXTERNAL PROTECT + ($\overline{\text{PARITY FAULT}}$) ($\overline{\text{STORAGE PROTECT FAULT}}$)] [(EXTERNAL CHANNEL ACTIVE) (EXTERNAL WRITE)] + [(PARITY FAULT) (STORAGE PROTECT FAULT) (WRITE PROTECT BIT) (COMPUTER CHANNEL ACTIVE)] + [(PARITY FAULT) (STORAGE PROTECT FAULT + (COMPUTER PROTECT) (WRITE) (COMPUTER CHANNEL ACTIVE)]

If any of the conditions in the above equation are satisfied, pin 5 of the V95 module receives a "0" input. The outputs of the parity generator modules (V18) are sampled. If the total number of bits is odd, the Parity Bit FF is not set and the inhibit fan-outs receive a "0" input which stores a "0" in bit 16. If the total number of bits is even, the inverse operation takes place.

Parity Fault Detection

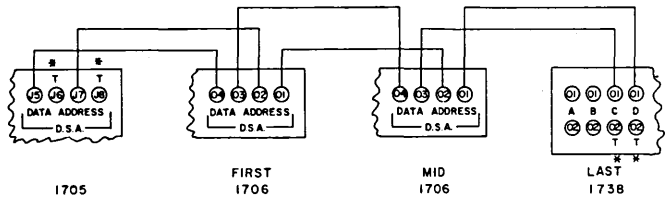
A parity fault is detected at the input inverters to the Parity Fault FF on the V95 module. The inputs to these inverters compare the parity generator outputs for the two halves of the word. If the two halves of the word (including parity bit) both contain an odd number of "1's", a parity fault is detected, and the Parity Fault FF is set. Likewise, if both halves contain an even number of bits, the Parity Fault FF is set. Thus, one-half of the word must contain an even number of "1's" and the other half must contain an odd number of "1's" due to the odd parity employed in the data word.

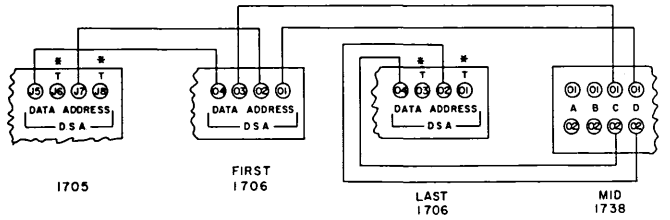
The Parity Fault condition is transmitted to the computer where it is used in the internal interrupt and fault indicator circuits. A parity fault also blocks a write operation if the location is not protected.

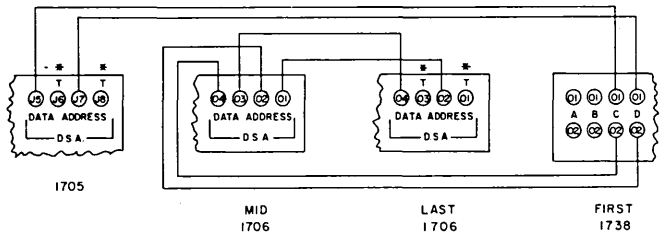


CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE STORAGE TIMING AND CONTROL	PRODUCT 1704 SIZE C · DRAWING NO. 60152700 · REV A SHEET · PAGE 105	

When more than one piece of Equipment is connected to the Direct Storage Access (DSA) Bus, Cables must be correctly installed to insure proper operation of the Scanner. The attached Diagram shows three pieces of Equipment using direct storage access, and the correct Cable connections for proper Scanner operation in the "First", "Mid", and "Last" settings. If any of the Cables are connected other than as shown, the Scanner will not function properly. Any change in Scanner priority will require the Equipment to be re-cabled to correspond with one of the examples shown. When the Scanner switch is dialed to "Out", that piece of Equipment is effectively removed from the DSA Bus, and the Scanner switches on all other Equipment must be changed to correspond with their new position on the DSA Bus.

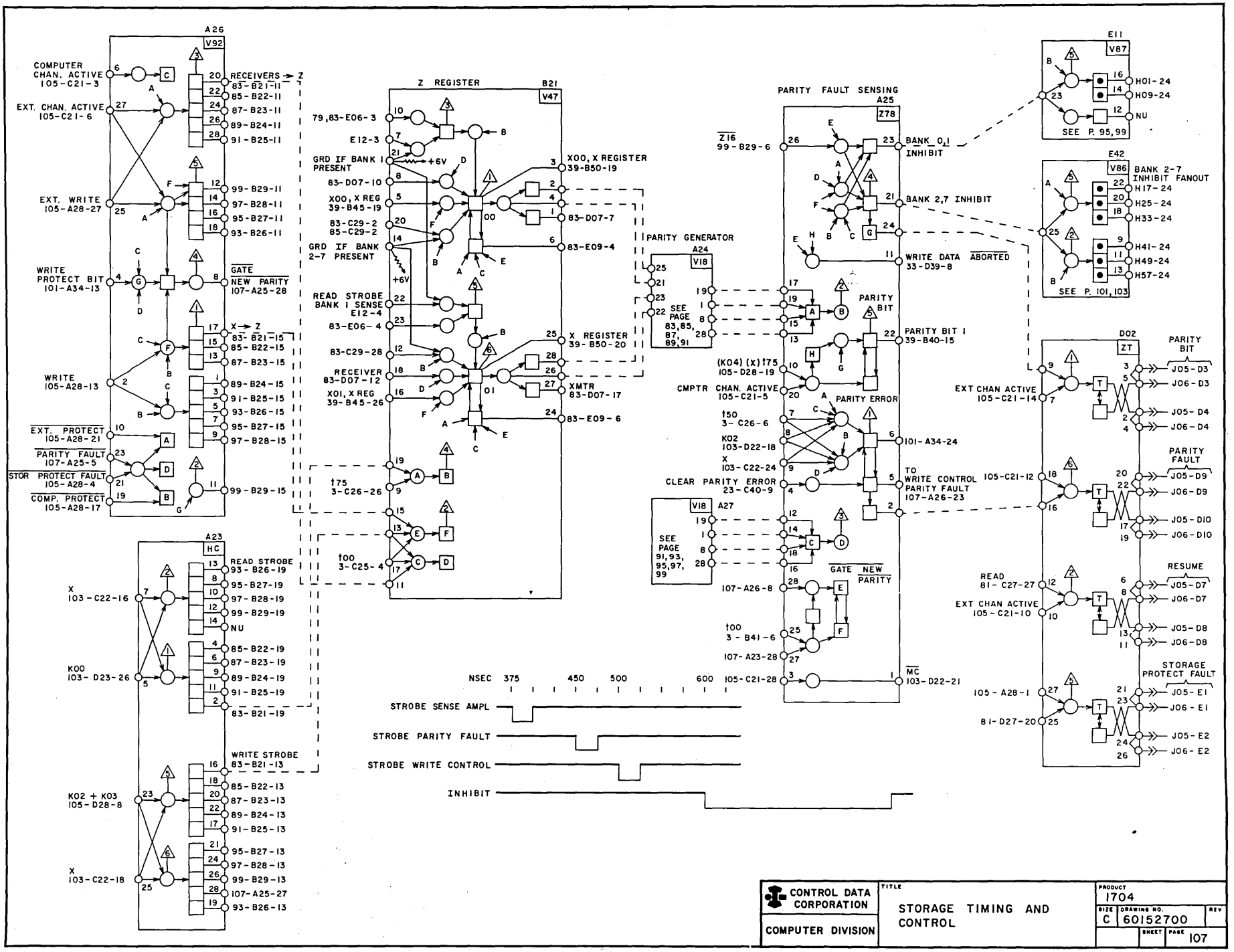






*NOTE
"T" INDICATES TERMINATOR

CONTROL DATA DEVELOPMENT DIVISION	TITLE DIRECT STORAGE ACCESS	PRODUCT 1704	
		SIZE C DRAWING NO. 60152700	REV. AA
		SHEET	PAGE 106



CONTROL DATA CORPORATION	TITLE: STORAGE TIMING AND CONTROL	PRODUCT: 1704	
COMPUTER DIVISION		SIZE: C	DRAWING NO.: 60152700
		SHEET:	PAGE: 107

X AND Y DRIVE DECKS (TYPE Z77)

The two type MX drive decks control the selection of the x and y drive lines. The y drive deck mounts on the top of the stack and the x drive deck on the bottom. The two decks are physically and logically identical.

The low-order 6 bits of the address select the y drive line, and the high-order 6 bits select the x drive line, thus selecting one of 4096 cores in each plane. The following description applies specifically to the y drive deck. However, the description also applies to the x drive deck with the interchange of bit positions.

The drive circuits have separate primary read (RC) and write (WC) current sources, and both feed eight current transformers through a double primary winding circuit. These transformers provide eight current sources. Each source feeds one drive line transformer in each of eight groups. The drive transformer secondary winding connects to the ends of the drive line which threads all 18 planes.

Each of eight diverter circuits feeds eight successive driver transformers. The selection of one of eight diverters diverts current to the proper drive line transformer and its drive line. Thus, a single current source is diverted to one of the 64 drive lines. Translations of S register bits 1, 2, and 3 select one of eight current source transformers. S register bits 0, 4, and 5 select one of eight diverters.

Since both drive decks are turned on at the same time, a coincident current passes through one core in each plane.

The 64 drive transformers on each deck are so arranged that the 32 odd line transformers are on one edge and the 32 even are on the opposite edge (page 79). Thus, opposite sides of the deck drive successive lines. This arrangement provides an opposing current relationship with the inhibit drive lines.

CURRENT SOURCE

The primary read or write current source consists of a large inductance connected between the +6v supply and the eight current transformers. Transistor Q1 (and Q2) and its collector resistor (several in parallel) shunt current of about 250 ma to ground during non-write-or-read times. The load network keeps the power supply load nearly constant at all times. After losses in the current transformer and drive line transformer, approximately 200 ma pass through the drive line during the storage cycle.

Bits 1, 2, and 3 of the address select one of eight transformers from a 2-by-4 transformer matrix. Bits 2 and 3 select one of four transformer groups, and bit 1 selects one of two in that group. The Read or Write Drive signal is combined with the one of two selection. The simplified drive and diverter circuits shown in the lower left-hand corner of the diagram assumes a --100- binary code in the 3-bit drive position. The example also shows that transistors Q5 and Q6 turn off (shown as an AND) and Q7 turns on to select transformers T4 and T5 in the one of four group; transistors Q8 and Q9 turn off and Q3 turns on to select the read side of T4. Read load network transistor Q1 turns off, and current flows from ground to the +6v source through transistors Q7 and Q3, transformer T4, diode CR1, and inductor L1.

A high impedance is presented to inductor L1 when read-load network transistor Q1 turns off, and the voltage level at the junction of diode CR1 and inductor L1 rises rapidly. However, diode CR4 conducts to place stabistor CR10 in the circuit, and the latter limits the peak voltage at the junction to 15v. Current loss in T4 is about 25 ma, so 225 ma flow in the secondary and is diverted to a drive transformer.

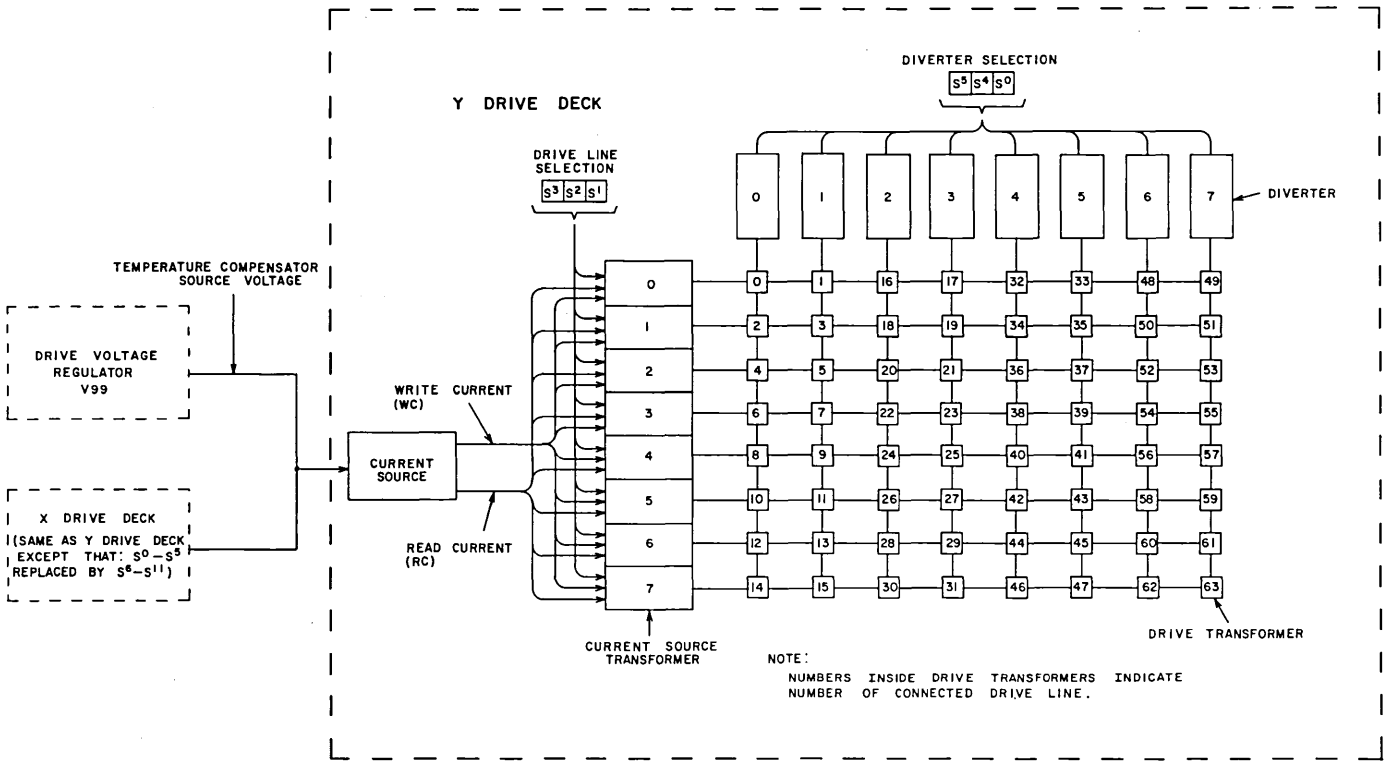
The circuit operates in a similar manner in the write cycle except that the polarities in the current transformer are reversed.

DIVERTER CIRCUITS

The eight diverter circuits divert read and write current to the drive transformers. Each circuit feeds eight drive transformers, one for each current source transformer. Thus, the selected current source transformer drives eight lines and only one of the eight is diverted.

The diagram shows one of eight diverter circuits and its selection from the 3 address bits used for divert. The collectors of Q10, Q11, and Q12 feed the base of NPN transistor Q14 directly and the base of PNP transistor Q15 indirectly via transistor Q13 which inverts the combined collector signal. The action establishes positive and negative turn-on signals for the bases of Q14 and Q15. Emitter bias on these two transistors is established by the divider network of R01, C01, and diodes CR7, 8, and 9. The diode threshold is about 0.7v for a combined drop of about 2.2v and proper emitter bias.

The circuit operates in a similar manner in the write cycle except the polarities in the current transformers are reversed.



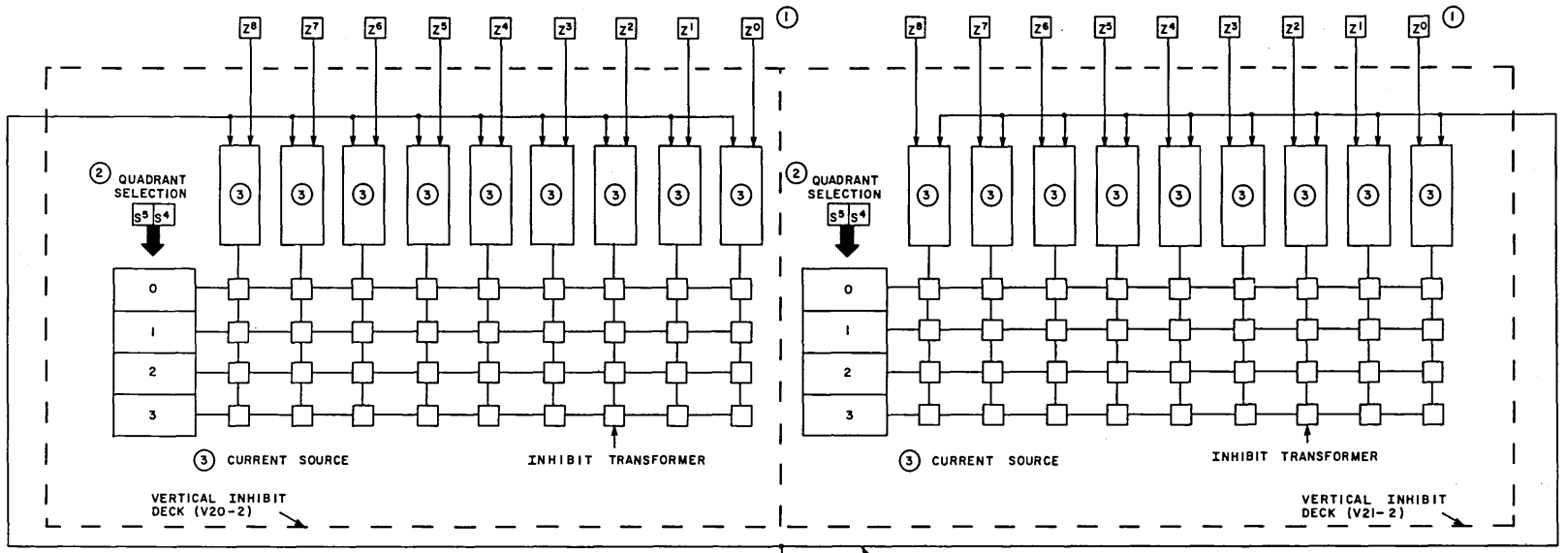
CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE: X AND Y DRIVE DECKS	PRODUCT: 1704 SIZE: C · DRAWING NO.: 60152700 · REV: A SHEET · PAGE: 109	

INHIBIT DRIVE DECKS (TYPES V20 AND V21)

Four inhibit decks provide the inhibit current for the writing of a "0" in the corresponding plane. An inhibit deck is mounted on each of the four sides of the stack (page 79).

The inhibit lines in each plane are divided into four vertical and four horizontal stripes or quadrants. Each quadrant threads through 16 rows (horizontal) or columns (vertical) of cores. If a particular stage of the Z register contains a "0" at the time of the inhibit phase of the storage cycle, one horizontal and one vertical inhibit quadrant is energized in the corresponding plane simultaneously with the write current. Thus, one 16-by-16 core portion of the plane receives full inhibit current. The quadrant that receives full inhibit current corresponds to the portion of the plane containing the selected core. S register bits 4 and 5 select the vertical inhibit quadrant and bits 10 and 11 select the horizontal quadrant.

Two types of inhibit decks are used, the V20 and V21. The two types differ only in the order of inhibit quadrant connections. There are two of each type mounted on the stack. The tables on the diagram list the inhibit decks and the Z register and S register connections.



(1) CODES $Z^0 - Z^8$ HAVE THE FOLLOWING SIGNIFICANCE

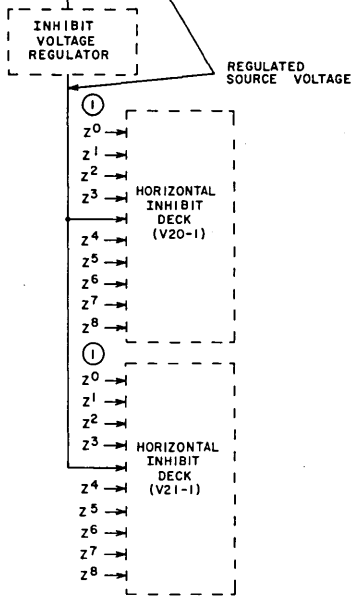
MODULE	Z^8	Z^7	Z^6	Z^5	Z^4	Z^3	Z^2	Z^1	Z^0
V20-1	16	15	12	11	8	7	4	3	0
V20-2	17	16	13	12	9	7	6	3	2
V21-1	17	14	13	10	9	6	5	2	1
V21-2	15	14	11	10	8	5	4	1	0

BIT INHIBITED

(2) CODES S^4, S^5 HAVE THE FOLLOWING SIGNIFICANCE

MODULE	S^5	S^4
V20-1	S^{11}	S^{10}
V20-2	S^5	S^4
V21-1	S^{11}	S^{10}
V21-2	S^5	S^4

EQUIVALENT S REGISTER BIT



CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE: INHIBIT DRIVE DECKS	PRODUCT 1704 SIZE C · DRAWING NO. 60152700 · REV A SHEET · PAGE 111	

TRANSFERS

ADDRESSING MODES

The table below shows the register transfers necessary in forming the 32 possible effective address modes. The storage reference instructions contain three fields: Instruction, Address Mode, and Delta. The format of the storage reference instruction is shown in the lower right hand corner. The effective address is formed by setting various combinations of the four address mode bits and delta. Delta is a signed 8-bit address modifier where the most significant bit (bit 7) is the sign bit.

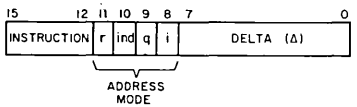
The computer assembles the effective address in the following order if the corresponding address flag is set.

1) checks r and Δ and forms P+Δ, P+1 or Δ.
2) checks ind and completes indirect addressing.
3) checks q and adds the contents of the Q register.
4) checks i and adds the contents of storage location 00FF.

F_{11}	r																F_{11}
$X_0 - X_7$	$\Delta = 0$								$\Delta \neq 0$								$X_0 - X_7$
F_{10}	IND				$\overline{IND}$				IND				$\overline{IND}$				F_{10}
F_9	q		$\overline{q}$		q		$\overline{q}$		q		$\overline{q}$		q		$\overline{q}$		F_9
F_8	i	$\overline{i}$	i	$\overline{i}$	i	$\overline{i}$	i	$\overline{i}$	i	$\overline{i}$	i	$\overline{i}$	i	$\overline{i}$	i	$\overline{i}$	F_8
$F_8 - F_{11}$ HEXADECIMAL	F	E	D	C	B	A	9	8	F	E	D	C	B	A	9	8	$F_8 - F_{11}$ HEXADECIMAL
P+I⇒Y P+I⇒P	P+I⇒Y P+I⇒P	P+I⇒Y P+I⇒P	P+I⇒Y P+I⇒P	P+I⇒Y P+I⇒P	P+I⇒Y P+I⇒P	P+I⇒Y P+I⇒P	P+I⇒Y P+I⇒P	X+Y⇒Y	X+Y⇒Y	X+Y⇒Y	X+Y⇒Y	X+Y⇒Y	X+Y⇒Y	X+Y⇒Y	X+Y⇒Y		
Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S										
Z⇒X X+Y⇒Y	Z⇒X X+Y⇒Y	Z⇒X X+Y⇒Y	Z⇒X X+Y⇒Y	Z⇒X X+Y⇒Y	Z⇒X X+Y⇒Y	Z⇒X X+Y⇒Y	Z⇒X X+Y⇒Y										
Y⇒S	Y⇒S	Y⇒S	Y⇒S					Y⇒S	Y⇒S	Y⇒S	Y⇒S						
Z⇒X X⇒Y BIT 15=1= NO ↓ YES Y⇒S								Z⇒X X⇒Y BIT 15=1= NO ↓ YES Y⇒S									
Y·Q⇒Y	Y·Q⇒Y				Y+Q⇒Y			Y+Q⇒Y	Y+Q⇒Y			Y+Q⇒Y	Y·Q⇒Y				
00FF⇒S		00FF⇒S		00FF⇒S		00FF⇒S		00FF⇒S		00FF⇒S		00FF⇒S		00FF⇒S			
Z⇒X X·Y⇒Y		Z⇒X X·Y⇒Y		Z⇒X X·Y⇒Y		Z⇒X X·Y⇒Y		Z⇒X X·Y⇒Y		Z⇒X X·Y⇒Y		Z⇒X X·Y⇒Y		Z⇒X X·Y⇒Y			
Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S		
(P+I+Q+00FF)	(P+I+Q)	(P+I)+00FF	(P+I)	(P+I)+(Q)+00FF	(P+I)+(Q)	(P+I)+00FF	(P+I)	(P+Δ+Q)+00FF	P+Δ+Q	P+Δ+00FF	P+Δ	P+Δ+Q+00FF	P+Δ+Q	P+Δ+00FF	P+Δ		
EFFECTIVE ADDRESS =																	= EFFECTIVE ADDRESS

NOTES:

1. r = F_{11} - RELATIVE ADDRESSING
2. ind = F_1 - INDIRECT ADDRESSING
3. q = F_2 - USE Q REGISTER AS INDEX
4. i = F_3 - USE ADDRESS 00FF (377_8) AS INDEX
5. PARENTHESES USED IN THE EFFECTIVE ADDRESS INDICATE "CONTENTS OF".



STORAGE REFERENCE FORMAT

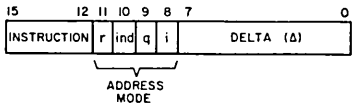
CONTROL DATA CORPORATION	TITLE	PRODUCT
DEVELOPMENT DIVISION	ADDRESSING MODES FOR STORAGE REFERENCE INSTRUCTIONS (r)	1704
		SIZE C · DRAWING NO. 60152700 · REV A
		SHEET · PAGE 113

F_{11}	$\overline{r}$																F_{11}
$X_0 - X_7$	$\Delta = 0$								$\Delta \neq 0$								$X_0 - X_7$
F_{10}	IND				$\overline{IND}$				IND				$\overline{IND}$				F_{10}
F_9	q		$\overline{q}$		q		$\overline{q}$		q		$\overline{q}$		q		$\overline{q}$		F_9
F_8	i	$\overline{i}$	i	$\overline{i}$	i	$\overline{i}$	i	$\overline{i}$	i	$\overline{i}$	i	$\overline{i}$	i	$\overline{i}$	i	$\overline{i}$	F_8
$F_8 - F_{11}$ HEXADECIMAL	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	$F_8 - F_{11}$ HEXADECIMAL
	P+I⇒Y P+I⇒P	P+I⇒Y P+I⇒P	P+I⇒Y P+I⇒P	P+I⇒Y P+I⇒P	P+I⇒Y P+I⇒P	P+I⇒Y P+I⇒P	P+I⇒Y P+I⇒P	P+I⇒Y P+I⇒P	0⇒X_U X⇒Y	0⇒X_U X⇒Y	0⇒X_U X⇒Y	0⇒X_U X⇒Y	0⇒X_U X⇒Y	0⇒X_U X⇒Y	0⇒X_U X⇒Y	0⇒X_U X⇒Y	
	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S					
	Z⇒X X⇒Y BIT 15 1-NO YES Y⇒S				Z⇒X X⇒Y	Z⇒X X⇒Y	Z⇒X X⇒Y	Z⇒X X⇒Y	Z⇒X X⇒Y BIT 15 ··· 1 - NO YES Y⇒S								
	Y·Q⇒Y	Y·Q⇒Y			Y·Q⇒Y	Y·Q⇒Y Y·Q⇒X			Y·Q⇒Y	Y·Q⇒Y			Y·Q⇒Y	Y·Q⇒Y			
	OOFF⇒S		OOFF⇒S		OOFF⇒S		OOFF⇒S		OOFF⇒S		OOFF⇒S		OOFF⇒S		OOFF⇒S		
	Z⇒X X·Y⇒Y		Z⇒X X·Y⇒Y		Z⇒X X·Y⇒Y X·Y⇒X		Z⇒X X·Y⇒Y X·Y⇒K		Z⇒X X·Y⇒Y		Z⇒X X·Y⇒Y		Z⇒X X·Y⇒Y		⇒X X·Y⇒Y		
	Y⇒S	Y⇒S	Y⇒S	Y⇒S					Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	Y⇒S	
EFFECTIVE ADDRESS =	(P·I)+Q)+(OOFF)	(P·I)+Q)	(P·I)+OOFF)	(P·I)	(P·I)+Q)+(OOFF)	(P·I)+Q)	(P·I)+(OOFF)	P·I	((Δ)+Q)+OOFF)	(Δ)+Q)	Δ)+OOFF)	Δ)	Δ+Q)+OOFF)	Δ+Q)	Δ+OOFF)	Δ	= EFFECTIVE ADDRESS
	⑥	⑥	⑥														

NOTES:

1. r - F_{11} - RELATIVE ADDRESSING
2. ind - F_{10} - INDIRECT ADDRESSING
3. q - F_9 - USE Q REGISTER AS INDEX
4. i - F_8 - USE ADDRESS OOFF (OOFF$_8$) AS INDEX
5. PARENTHESES USED IN THE EFFECTIVE ADDRESS INDICATE "CONTENTS OF".

⑥ EFFECTIVE ADDRESS OPERAND FOR READ OPERAND INSTURCTIONS.



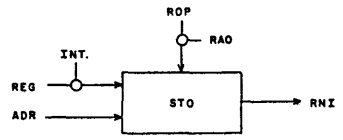
STORAGE REFERENCE FORMAT

CONTROL DATA CORPORATION	TITLE	PRODUCT	
DEVELOPMENT DIVISION	ADDRESSING MODES FOR STORAGE REFERENCE INSTRUCTIONS ($\overline{r}$)	1704	
		SIZE C	DRAWING NO. 60152700 REV A
			SHEET PAGE 115

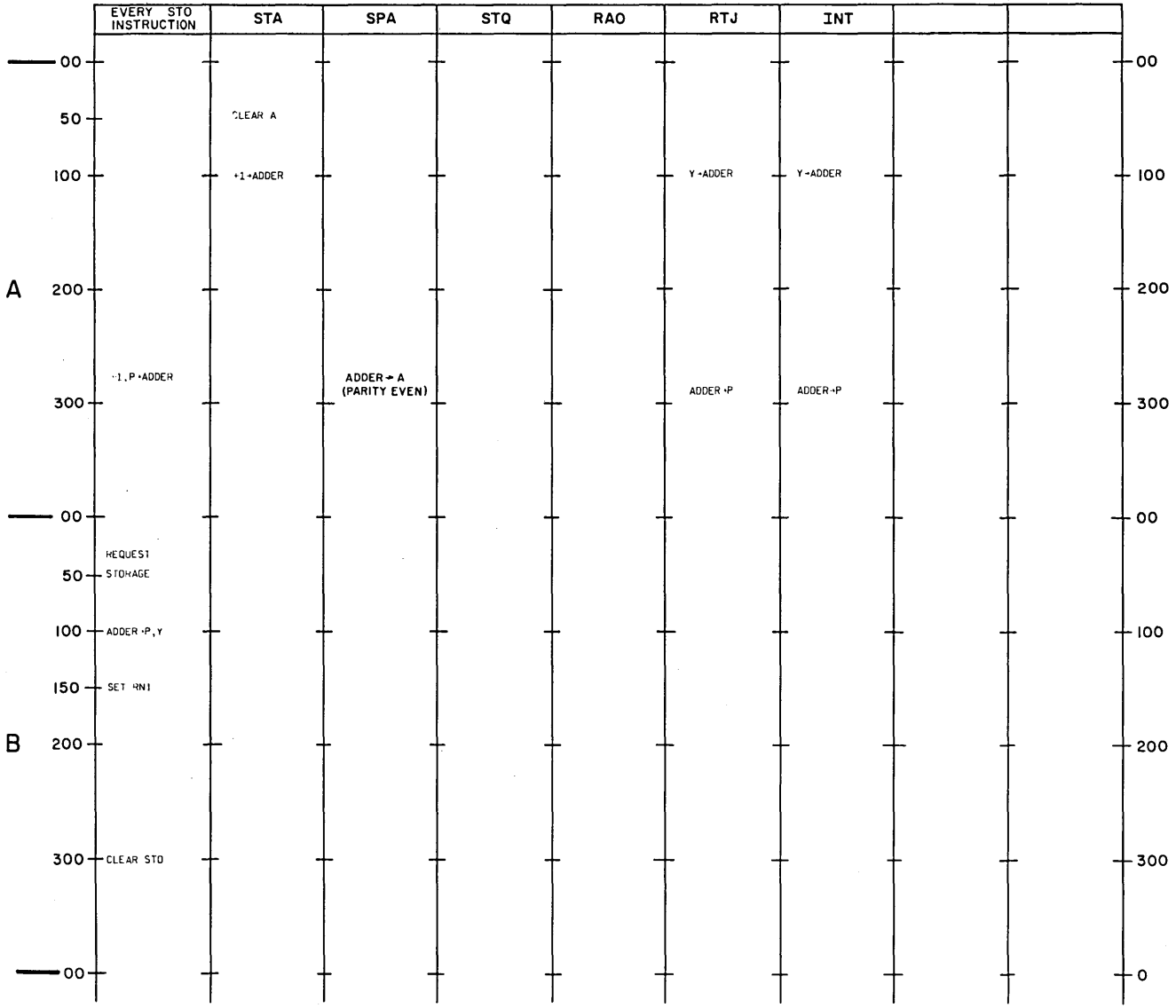
STO TRANSFERS

The following table shows the transfers and commands necessary for instructions using the Store Operand mode (STO). Storage is requested at time B050 for every STO instruction.

The sequence paths for entering and exiting STO mode are shown below:



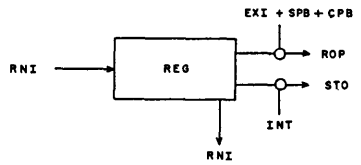
STORE OPERAND MODE (STO)



CONTROL DATA CORPORATION	TITLE: STO TRANSFERS	PRODUCT: 1704
DEVELOPMENT DIVISION		SIZE: C · DRAWING NO.: 60152700 · REV: A
		SHEET · PAGE: 117

The following table shows the transfers and commands necessary for instructions using the Register Transfer mode (REG). The table is especially useful for showing the absence of certain conditions and transfers during the execution of the listed instructions. For example, at time B100 the Adder ⟶ Y, P transfer is not used for the EXI, SPB and CPB instructions. Also, note that a C cycle occurs during a Shift instruction when the shift count ≠ 0.

The sequence paths for entering and exiting the REG mode are shown below:



REGISTER TRANSFER MODE (REG)

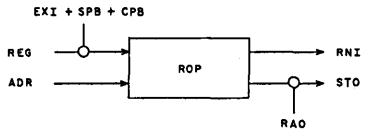
	SLS	ENQ	ENA	INA	INQ		INP + OUT	EXI	SKIPS	SPB + CPB	EIN + IIN	SHIFTS: SHIFT COUNT = 0	SHIFTS: SHIFT COUNT ≠ 0	
00														00
100		X⇐AUGEND	X⇐ADDEND	A⇐ADDER X⇐ADDEND	Q⇐ADDER X⇐AUGEND		X⇐AUGEND P⇐ADDER	X⇐ADDEND	X⇐AUGEND (LOWER 4) P⇐ADDER	Q⇐ADDER		X⇐ADDEND	X⇐ADDEND	100
									SET + CLEAR SKIP FF					
A 200											CLR ENABLE INT (IIN)			200
250							STOP AND WAIT FOR REPLY						SET SHIFT CYCLE	
300	+1,P⇐ADDER	ADDER⇐Q +1,P⇐ADDER	ADDER⇐A +1,P⇐ADDER	ADDER⇐A +1,P⇐ADDER	ADDER⇐Q -1,P⇐ADDER		ADDER⇒P (REJECT) +1,P⇐ADDER 1'S⇐A	ADDER⇐Y +1,P⇐ADDER	ADDER⇒P (SKIP) -1,P⇐ADDER	ADDER⇐Y +1,P⇐ADDER	+1,P⇐ADDER	ADDER⇐Y +1,P⇐ADDER	ADDER⇐Y A OR Q ⇐ADDER SET L.P. SET SHIFT R +L	300
												SET EARLY B	SET DECR.Y	
													SET EARLY C	
00												SET B CYCLE	DECR Y SET C CYCLE	00
													C CYCLE	
50	REQ.STORAGE SET STOP 1	REQ. STORAGE	REQ. STORAGE	REQ. STORAGE	REQ. STORAGE		REQ. STORAGE	REQ. STORAGE	REQ. STORAGE	REQ. STORAGE	REQ. STORAGE	REQ. STORAGE	REQ. STORAGE	
100	ADDER⇐Y,P	ADDER⇐Y,P	ADDER⇐Y,P	ADDER⇐Y,P	ADDER⇐Y,P		ADDER⇐Y,P		ADDER⇐Y,P		ADDER⇐Y,P	ADDER⇐Y,P	ADDER⇐Y,P	100
	SET RNI	SET RNI	SET RNI	SET RNI	SET RNI		SET RNI	SET ROP	SET RNI	SET ROP CLEAR RNI	SET RNI	SET RNI	SET RNI	
B 200														200
								SET ENABLE INT			SET ENABLE INT			
300	CLEAR REG.	CLEAR REG.	CLEAR REG.	CLEAR REG.	CLEAR REG.		CLEAR REG.	CLEAR REG.	CLEAR REG.	CLEAR REG.	CLEAR REG.	CLEAR REG.	CLEAR REG.	300
325	SET STOP 2													
00														00

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE: REG TRANSFERS	PRODUCT: 1704 SIZE: C · DRAWING NO.: 60152700 · REV: P SHEET · PAGE: 119	

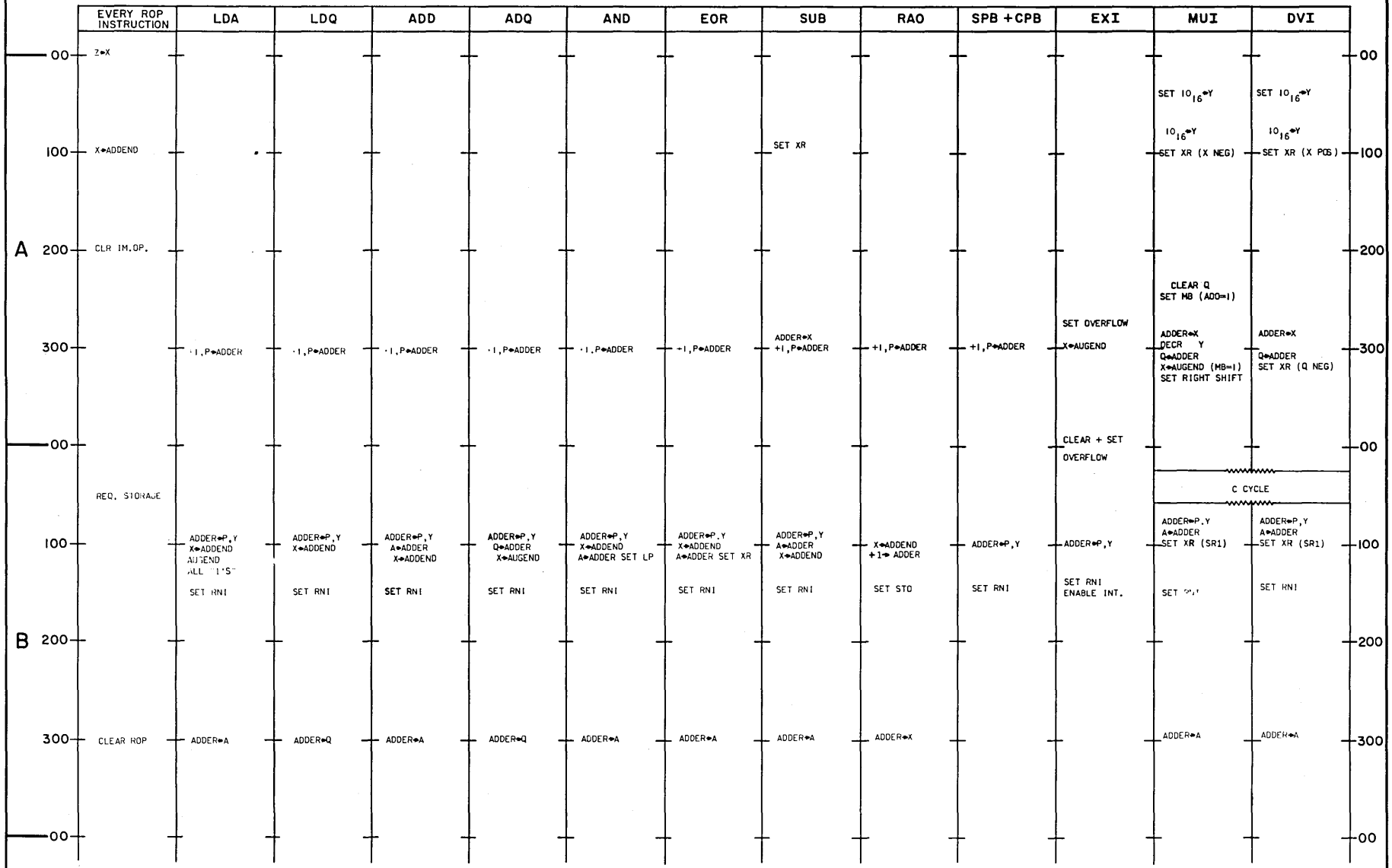
ROP TRANSFERS

The following table shows the transfers and commands necessary for instructions using the Read Operand mode (ROP). At time A000 the computer receives a Storage Resume signal and at time B050 storage is requested. Note that a C cycle occurs during the ROP mode for MUI and DVI instructions.

The sequence paths for entering and exiting the ROP mode are shown below:



READ OPERAND MODE (ROP)



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE: ROP TRANSFERS

PRODUCT: 1704
SIZE: C | DRAWING NO.: 60152700 | REV: Y
SHEET | PAGE: 121

THIS TABLE SHOWS THE TRANSFERS THAT MAY OCCUR DURING THE LAST TIME OF THE ADDRESSING SEQUENCE AND THE TRANSITION TO THE NEXT SEQUENCE.
(B CYCLE OF ADDRESSING)

	JMP	MUI + DVI	STA + SPA	STQ	RTJ	INT.	
00	(ADDR) (B)	(ADDR) (B)	(ADDR) (B)	(ADDR) (B)	(ADDR) (B)	(ADDR) (B)	00
	REQUEST STORAGE	REQUEST STORAGE (BLOCK REG.)	REQUEST STORAGE	REQUEST STORAGE	REQUEST STORAGE	REQUEST STORAGE	
100	Y→ADDER	A→ADDER SET XR (MUI) (A NEG)→(DVI) (Q NEG)	A→ADDER	Q→ADDER	+1, P→ADDER	P→ADDER X→ADDER (Δ=0)	100
	SET RNI (END ADDR)	SET ROP (END ADDR)	SET STO (END ADDR)	SET STO (END ADDR)	SET STO (END ADDR)	SET STO	
200							200
	(RNI) (B)	(ROP) (B)	(STO) (B)	(STO) (B)	(STO) (B)	(STO) (B)	
300	ADDER→P CLEAR ADDR.	ADDER→A CLEAR ADDR.	ADDER→Y CLEAR ADDR.	ADDER→X CLEAR ADDR.	ADDER→X CLEAR ADDR.	ADDER→X CLEAR ADDR.	300
400							400

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE: B CYCLE TRANSFERS

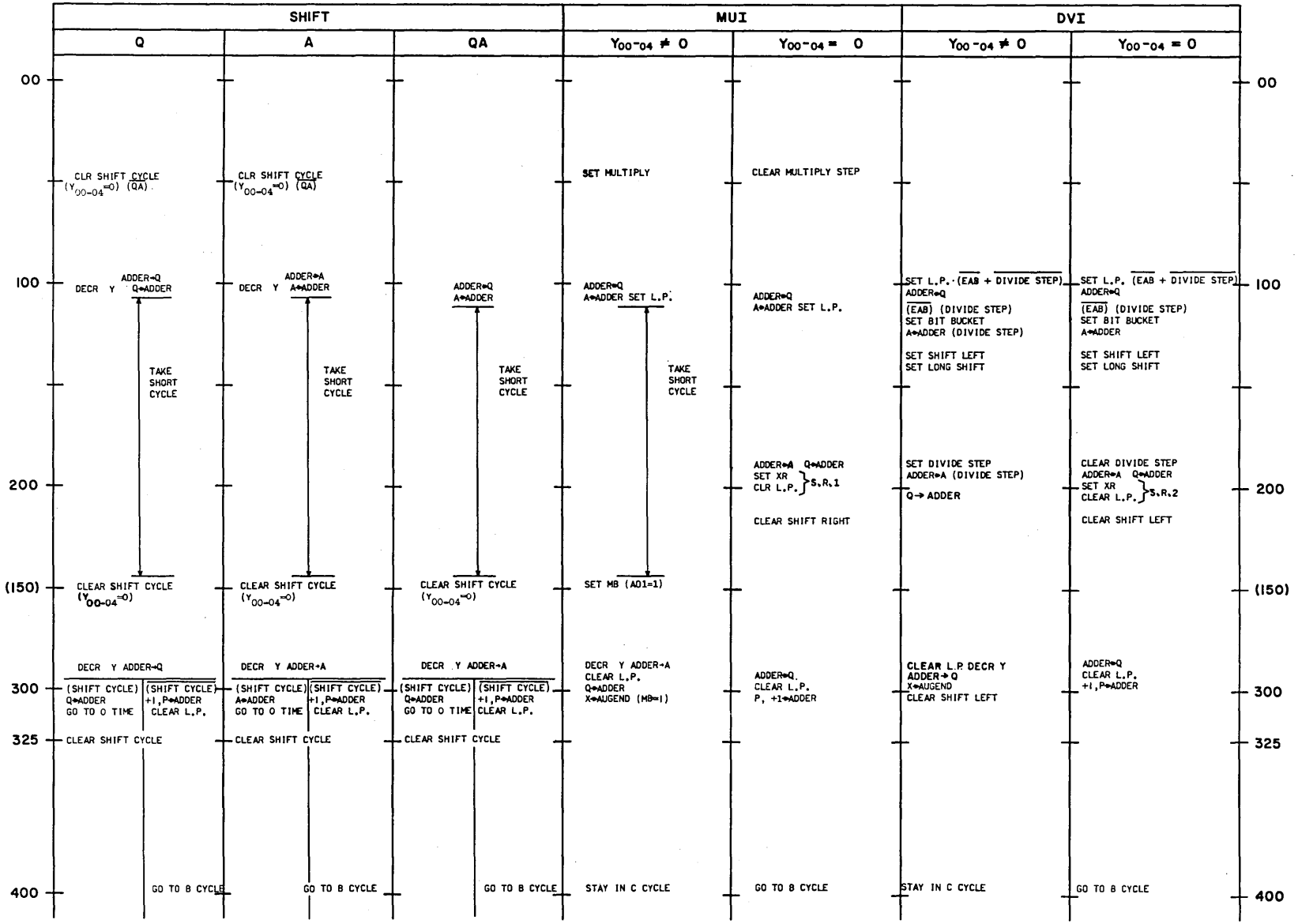
PRODUCT: 1704
SIZE: C | DRAWING NO.: 60152700 | REV: Y
SHEET | PAGE: 123

C CYCLE TRANSFERS

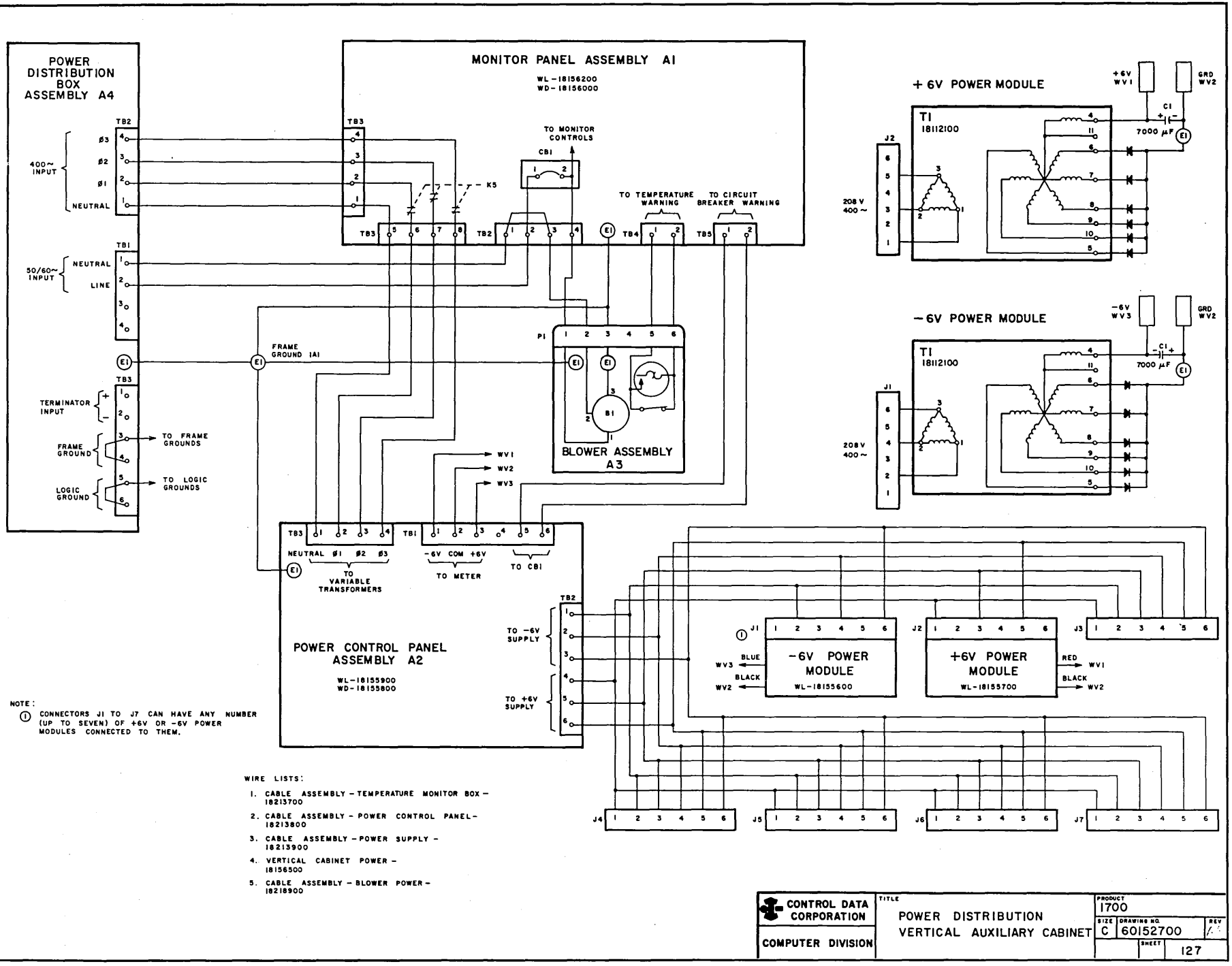
The following table shows the transfers and commands necessary during the C cycle of Shift, MUI,and DVI instructions. Time 150 occurs 100 nsec early for Shift and MUI instructions when the short cycle through the Adder/Shifter is used. This effectively reduces the Adder/Shifter time from 200 nsec to 100 nsec. A DVI instruction uses the complete Adder/Shifter and therefore does not use the short cycle.

If Y00-04 $\neq$ 0 at the end of the C cycle, the C cycle is repeated. If Y00-04 = 0 at the end of the C cycle, the B cycle is initiated.

TRANSFERS DURING C CYCLE
(ITERATIVE CYCLE FOR MUI, DVI AND SHIFT)



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE: C CYCLE TRANSFERS	PRODUCT: 1704 SIZE: C · DRAWING NO.: 60152700 · REV: AA SHEET · PAGE: 125	



NOTE:
① CONNECTORS J1 TO J7 CAN HAVE ANY NUMBER (UP TO SEVEN) OF +6V OR -6V POWER MODULES CONNECTED TO THEM.

WIRE LISTS:

1. CABLE ASSEMBLY - TEMPERATURE MONITOR BOX - 18213700
2. CABLE ASSEMBLY - POWER CONTROL PANEL - 18213800
3. CABLE ASSEMBLY - POWER SUPPLY - 18213900
4. VERTICAL CABINET POWER - 18156500
5. CABLE ASSEMBLY - BLOWER POWER - 18218900

CONTROL DATA CORPORATION
COMPUTER DIVISION

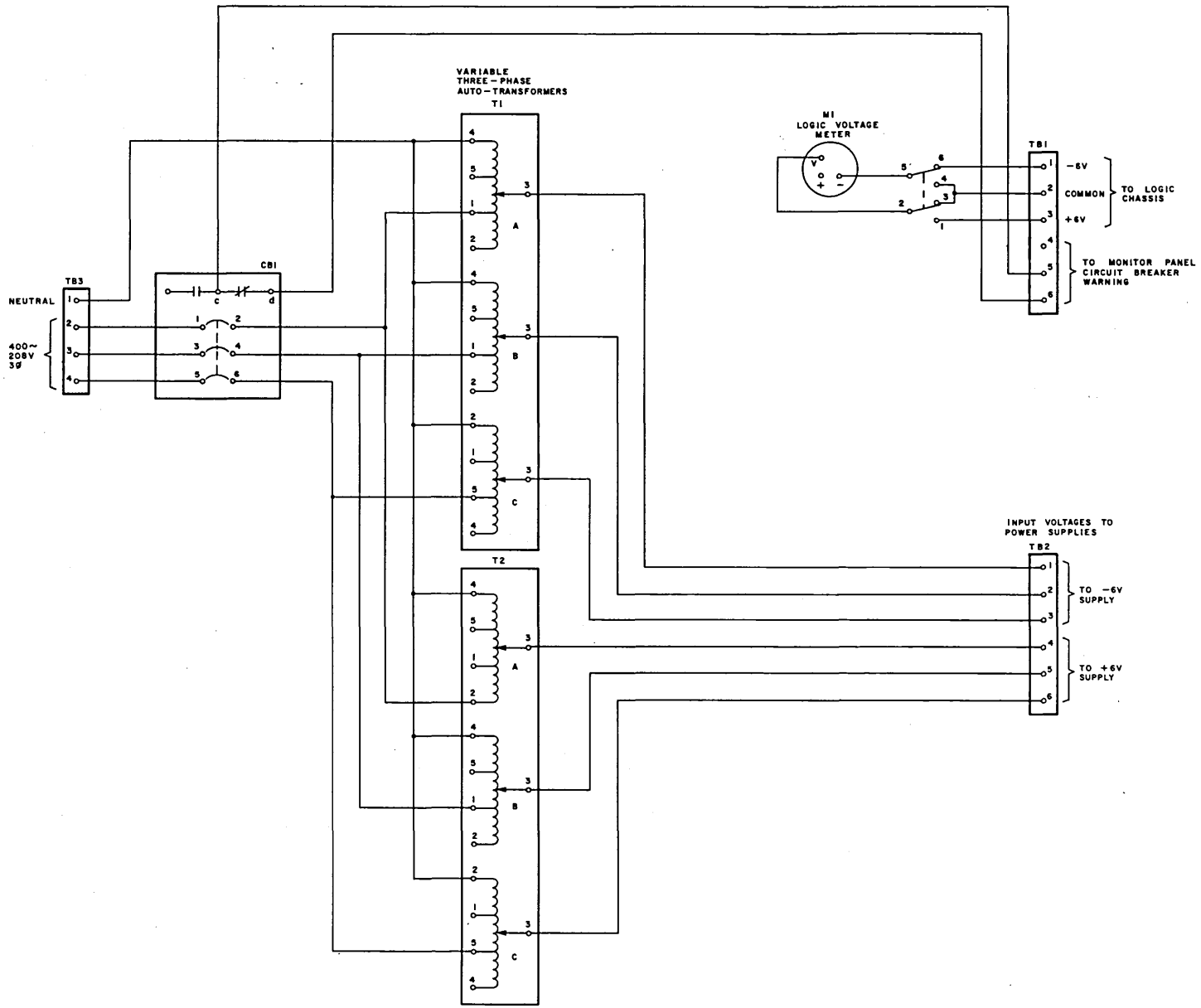
TITLE
POWER DISTRIBUTION
VERTICAL AUXILIARY CABINET

PRODUCT 1700
SIZE C | DRAWING NO. 60152700 | REV
SHEET 127

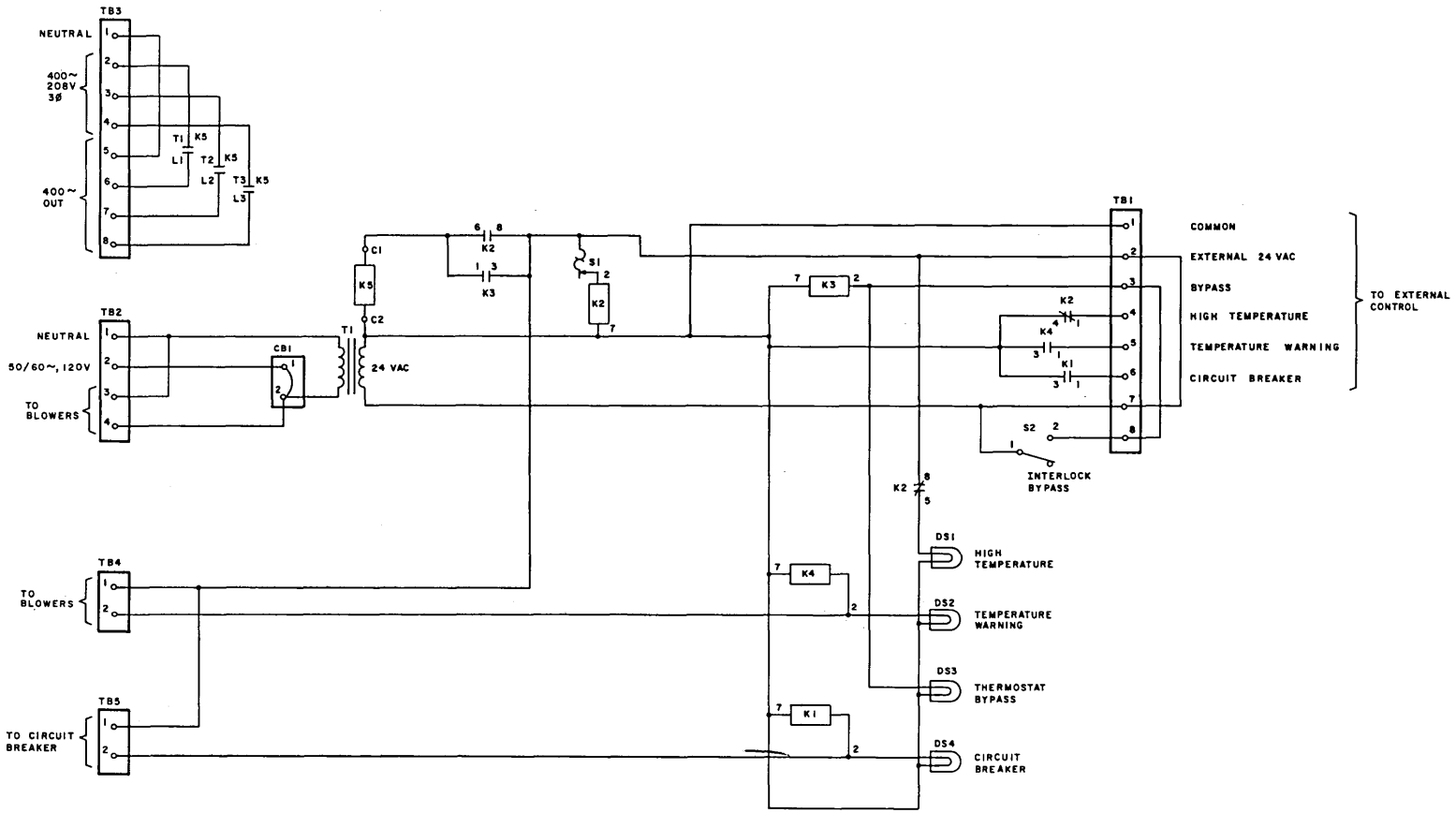
POWER AND CABLING

The following diagrams may be found in the 1700 Site Preparation manual. Pub. No. 60158400.

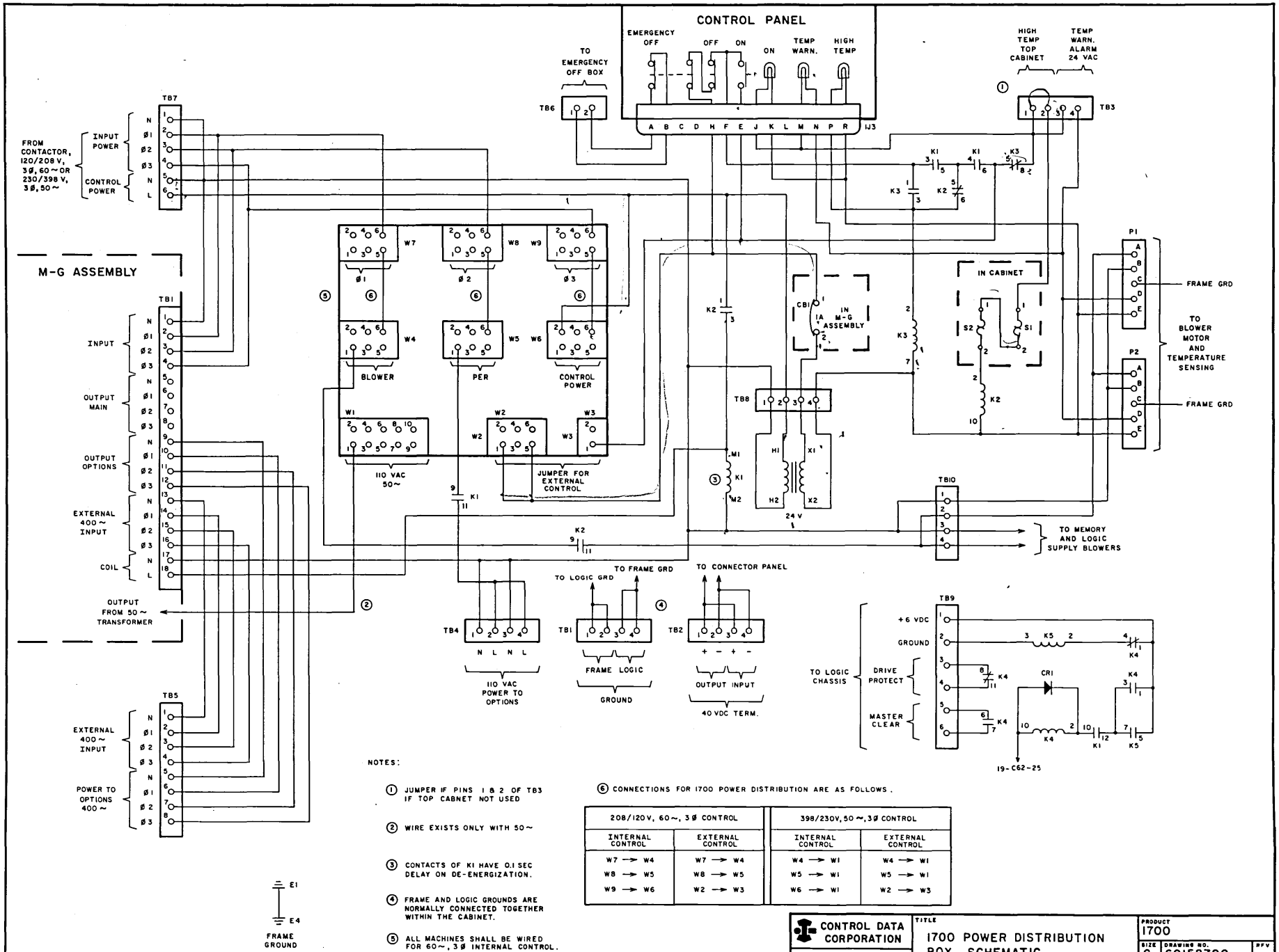
Power Distribution, 50 Cycle Internal M-G.
Power Distribution, 60 Cycle Internal M-G.
Typical 1700 System Using Both Internal and External M-G Sets.
Typical 1700 System Using an External M-G Set.



CONTROL DATA CORPORATION	TITLE: POWER CONTROL PANEL ASSEMBLY A2 VERTICAL AUXILIARY CABINET	PRODUCT: 1700	
COMPUTER DIVISION		SIZE: C · DRAWING NO.: 60152700 · REV: R	
		SHEET: 129	



CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE MONITOR PANEL ASSEMBLY AI VERTICAL AUXILIARY CABINET	PRODUCT 1700 SIZE C · DRAWING NO. 60152700 · REV SHEET 131	



NOTES:

① JUMPER IF PINS 1 & 2 OF TB3 IF TOP CABNET NOT USED

② WIRE EXISTS ONLY WITH 50~

③ CONTACTS OF K1 HAVE 0.1 SEC DELAY ON DE-ENERGIZATION.

④ FRAME AND LOGIC GROUNDS ARE NORMALLY CONNECTED TOGETHER WITHIN THE CABINET.

⑤ ALL MACHINES SHALL BE WIRED FOR 60~, 3Ø INTERNAL CONTROL.

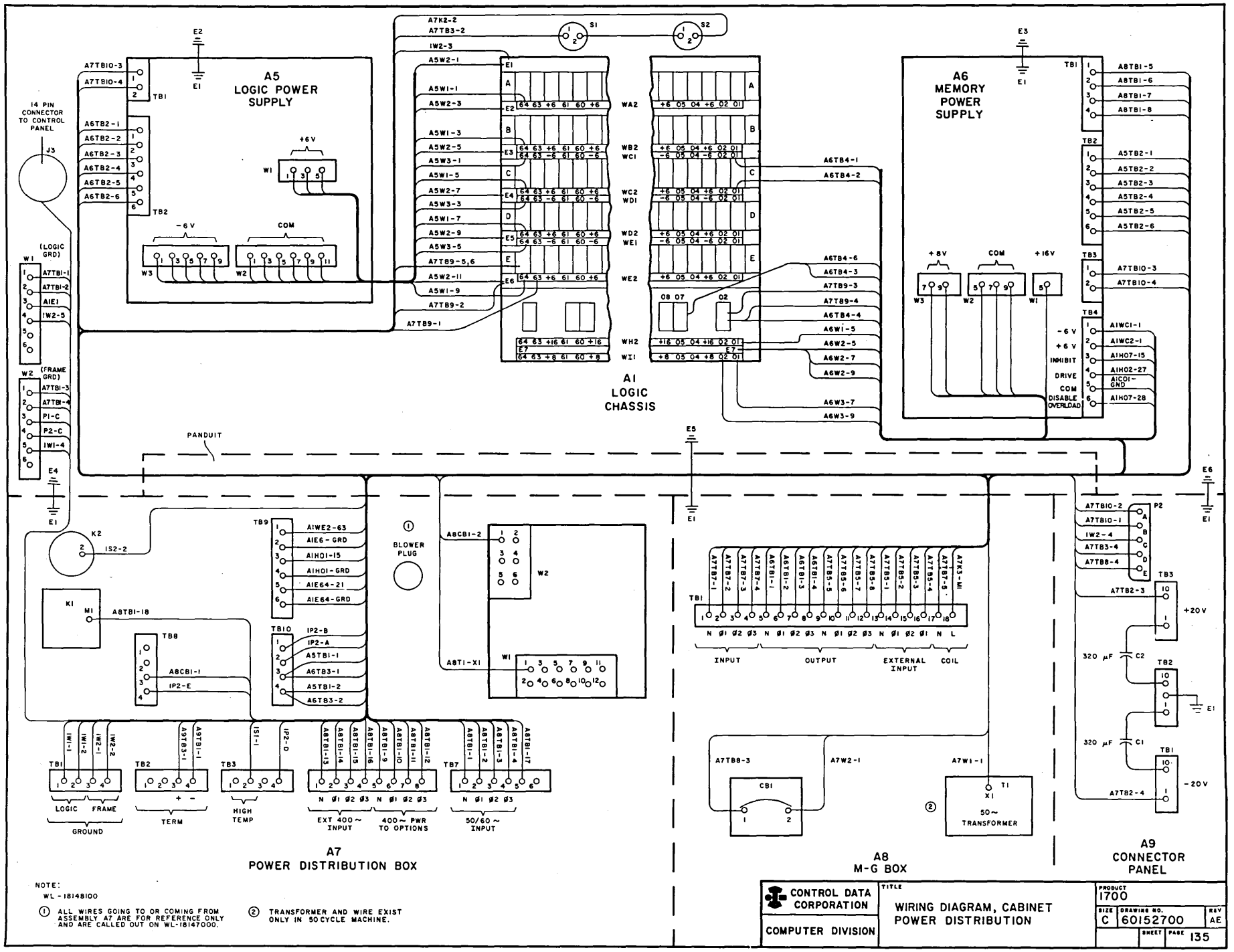
⑥ CONNECTIONS FOR 1700 POWER DISTRIBUTION ARE AS FOLLOWS.

208/120V, 60~, 3Ø CONTROL		398/230V, 50~, 3Ø CONTROL	
INTERNAL CONTROL	EXTERNAL CONTROL	INTERNAL CONTROL	EXTERNAL CONTROL
W7 → W4	W7 → W4	W4 → W1	W4 → W1
W8 → W5	W8 → W5	W5 → W1	W5 → W1
W9 → W6	W2 → W3	W6 → W1	W2 → W3

CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE: 1700 POWER DISTRIBUTION BOX, SCHEMATIC. ASSEMBLY - A7

PRODUCT: 1700
SIZE: C
DRAWING NO.: 60152700
REV
SHEET
PAGE: J33

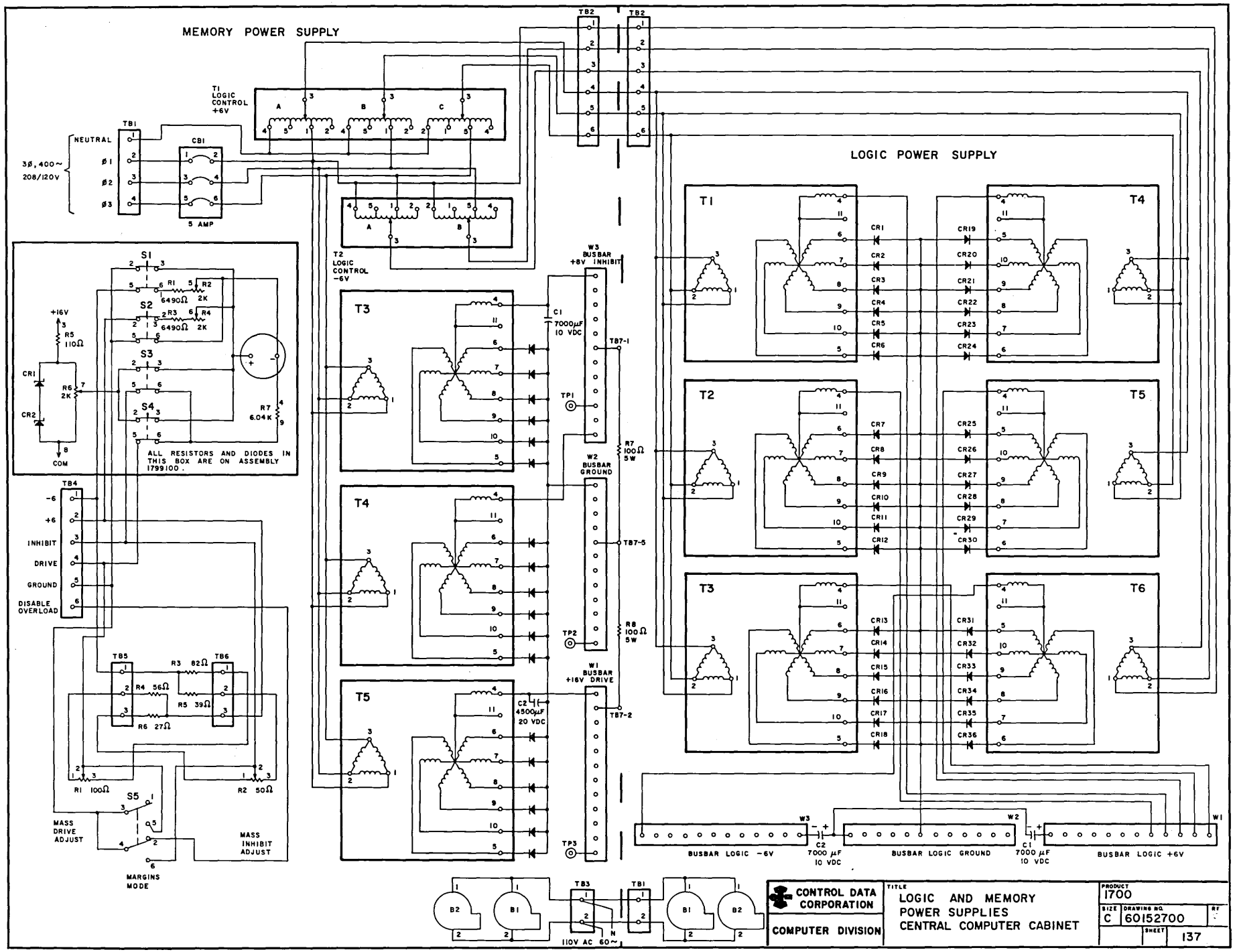


NOTE:
WL - 18148100

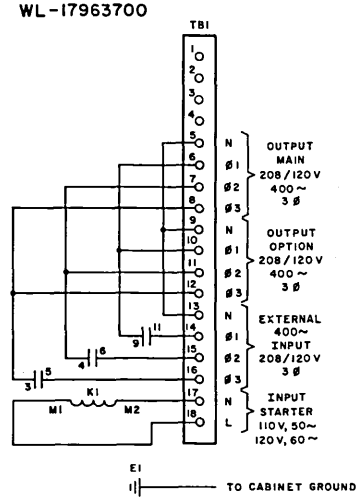
① ALL WIRES GOING TO OR COMING FROM ASSEMBLY A7 ARE FOR REFERENCE ONLY AND ARE CALLED OUT ON WL-18147000.

② TRANSFORMER AND WIRE EXIST ONLY IN 50 CYCLE MACHINE.

CONTROL DATA CORPORATION	TITLE: WIRING DIAGRAM, CABINET POWER DISTRIBUTION	PRODUCT 1700	
COMPUTER DIVISION		SIZE C	DRAWING NO. 60152700 REV AE
			SHEET PAGE 135


MEMORY POWER SUPPLY
LOGIC POWER SUPPLY
T1 LOGIC CONTROL +6V
T2 LOGIC CONTROL -6V
TB1
TB2
TB3
TB4
TB5
TB6
CB1
NEUTRAL
3Ø, 400~ 208/120V
Ø1
Ø2
Ø3
5 AMP
S1
S2
S3
S4
S5
R1 6490Ω
R2 2K
R3 6490Ω
R4 2K
R5 110Ω
R6 2K
R7 6.04K
+16V
COM
CR1
CR2
ALL RESISTORS AND DIODES IN THIS BOX ARE ON ASSEMBLY 1799100.
-6
+6
INHIBIT
DRIVE
GROUND
DISABLE OVERLOAD
R3 82Ω
R4 56Ω
R5 39Ω
R6 27Ω
R1 100Ω
R2 50Ω
MASS DRIVE ADJUST
MASS INHIBIT ADJUST
MARGINS MODE
W3 BUSBAR +8V INHIBIT
W2 BUSBAR GROUND
W1 BUSBAR +16V DRIVE
C1 7000μF 10 VDC
C2 4500μF 20 VDC
TB7-1
TB7-5
TB7-2
TP1
TP2
TP3
R7 100Ω 5W
R8 100Ω 5W
T1
T2
T3
T4
T5
T6
CR1 CR2 CR3 CR4 CR5 CR6
CR7 CR8 CR9 CR10 CR11 CR12
CR13 CR14 CR15 CR16 CR17 CR18
CR19 CR20 CR21 CR22 CR23 CR24
CR25 CR26 CR27 CR28 CR29 CR30
CR31 CR32 CR33 CR34 CR35 CR36
BUSBAR LOGIC -6V
C2 7000 μF 10 VDC
BUSBAR LOGIC GROUND
C1 7000 μF 10 VDC
BUSBAR LOGIC +6V
B1
B2
110V AC 60~
N
CONTROL DATA CORPORATION
COMPUTER DIVISION
TITLE
LOGIC AND MEMORY POWER SUPPLIES CENTRAL COMPUTER CABINET
PRODUCT 1700
SIZE C
DRAWING NO. 60152700
SHEET 137

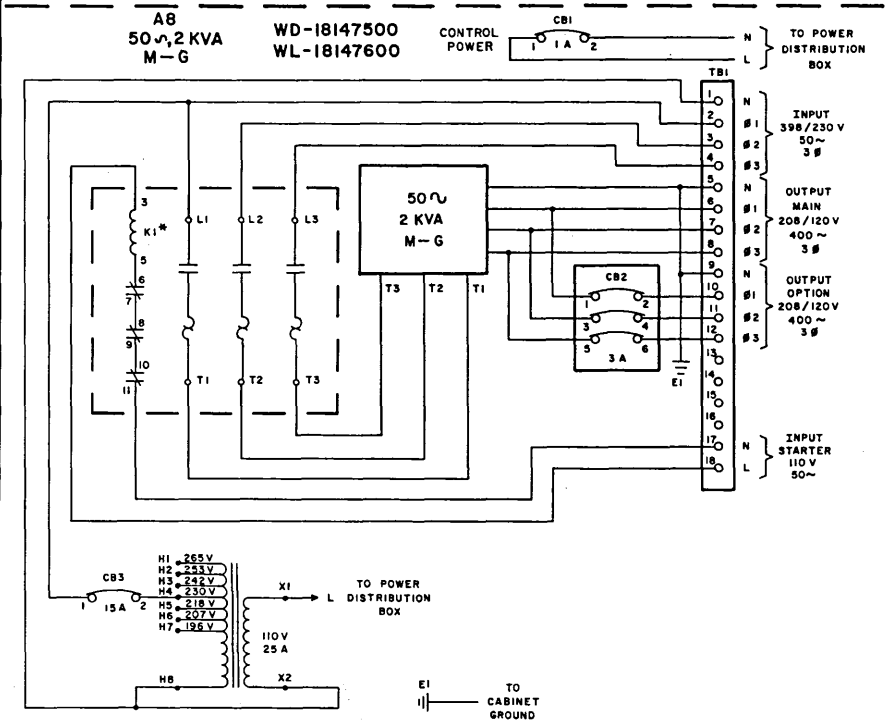
A8
400∿
POWER BOX
WL-17963700



* NOTE: CONTACTS OF RELAY K1 HAVE 1.0 SECOND DELAY WHEN RELAY IS DE-ENERGIZED.

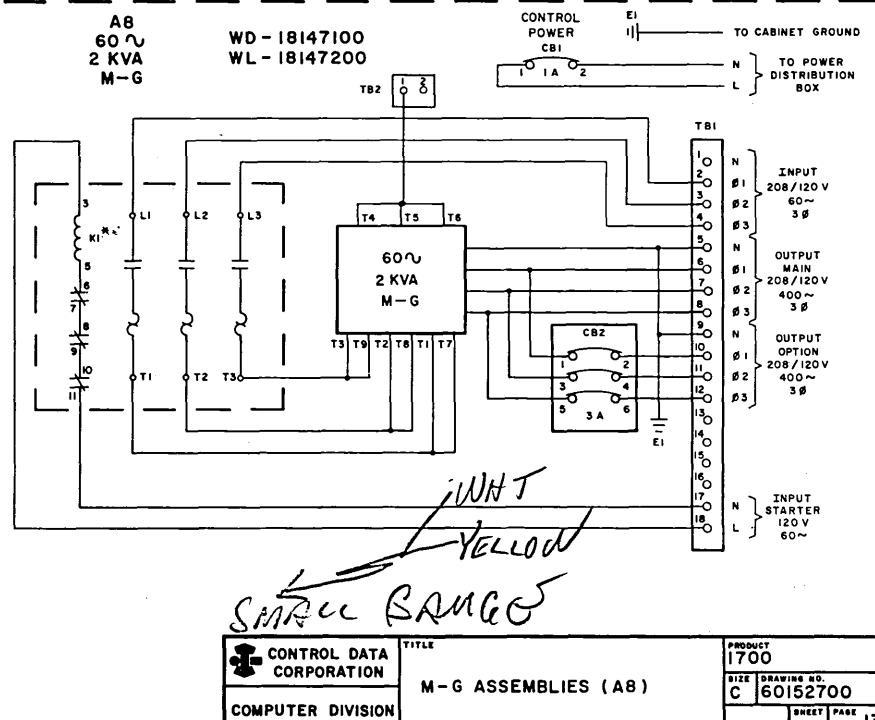
A8
50∿, 2 KVA
M-G

WD-18147500
WL-18147600

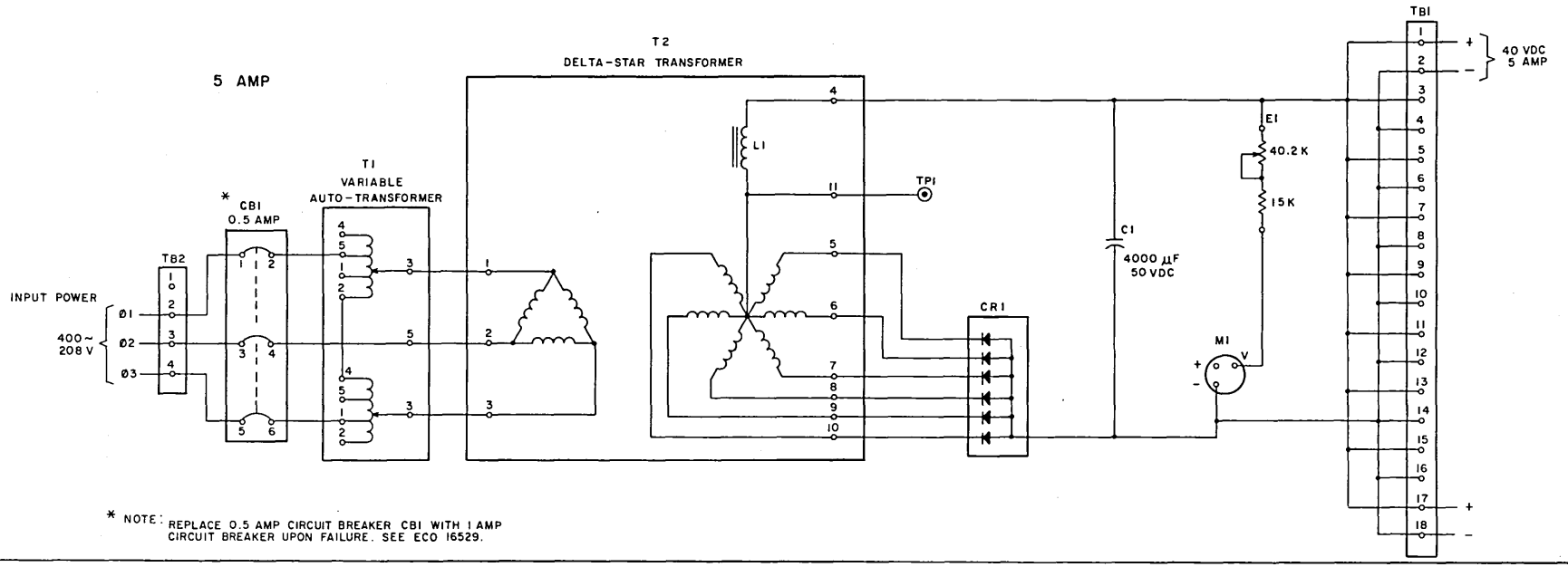


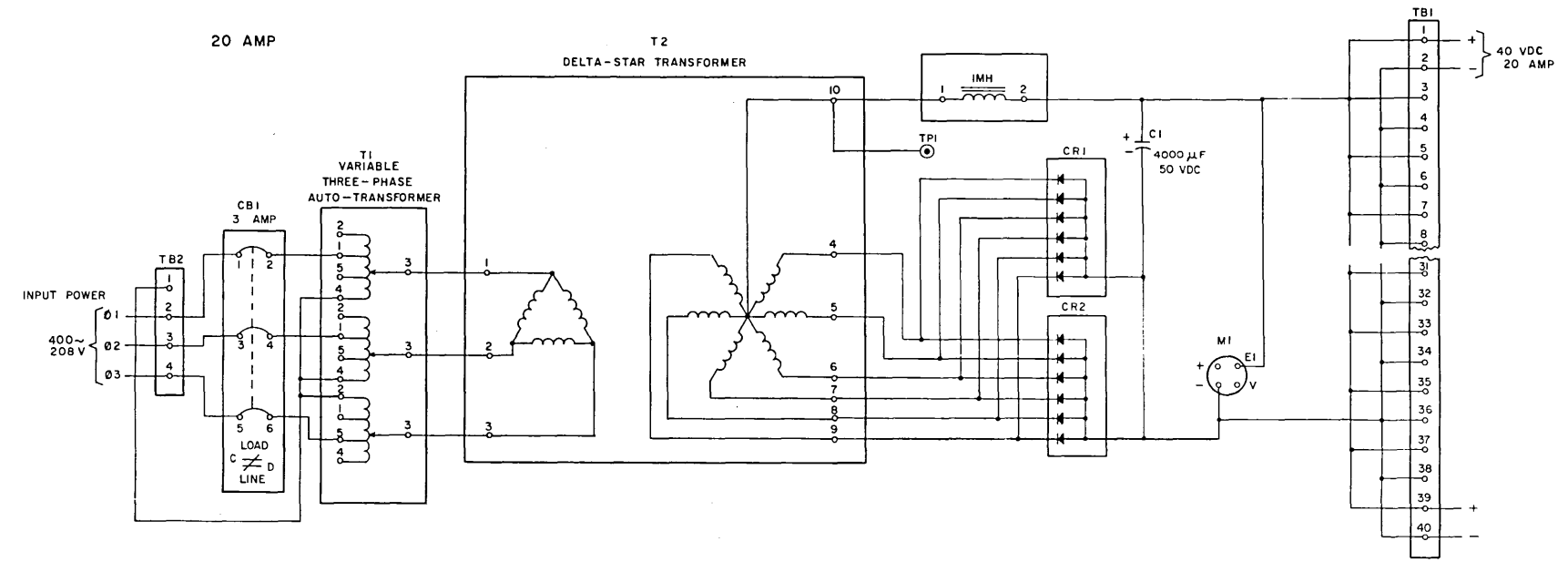
A8
60∿
2 KVA
M-G

WD-18147100
WL-18147200

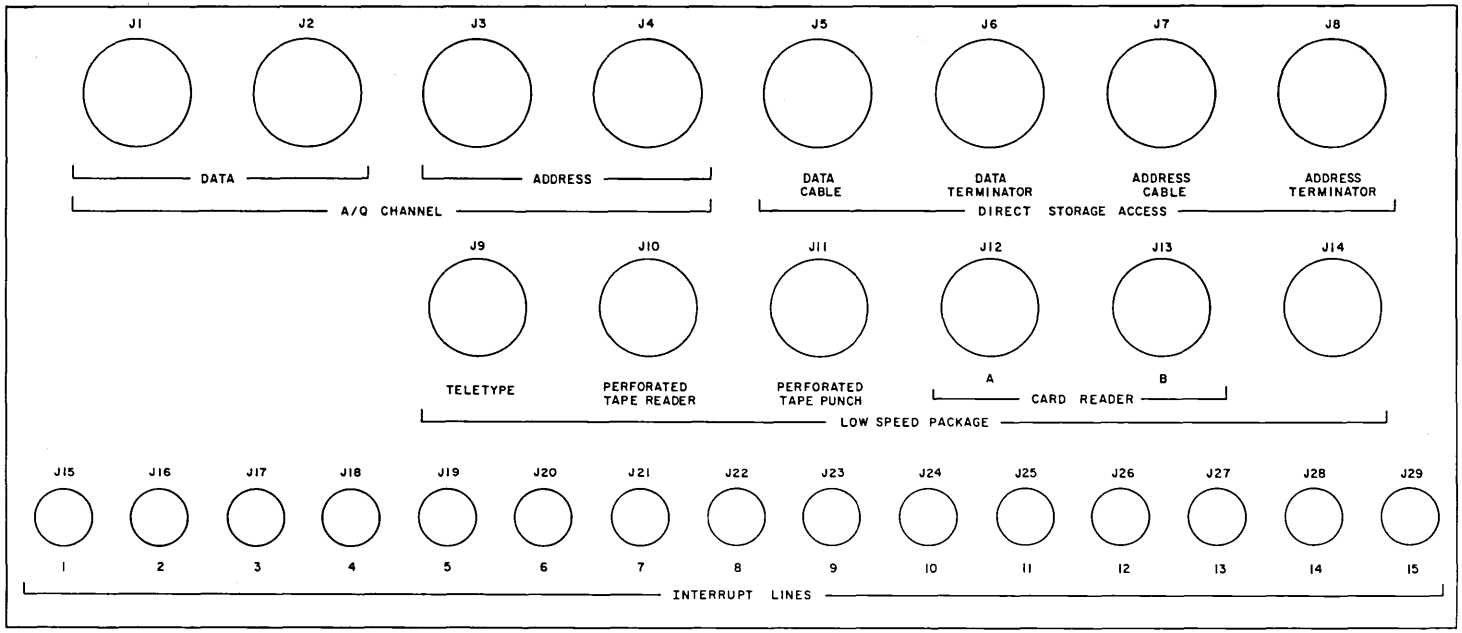


CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE M-G ASSEMBLIES (A8)	PRODUCT 1700 SIZE C DRAWING NO. 60152700 REV AP SHEET PAGE 139	

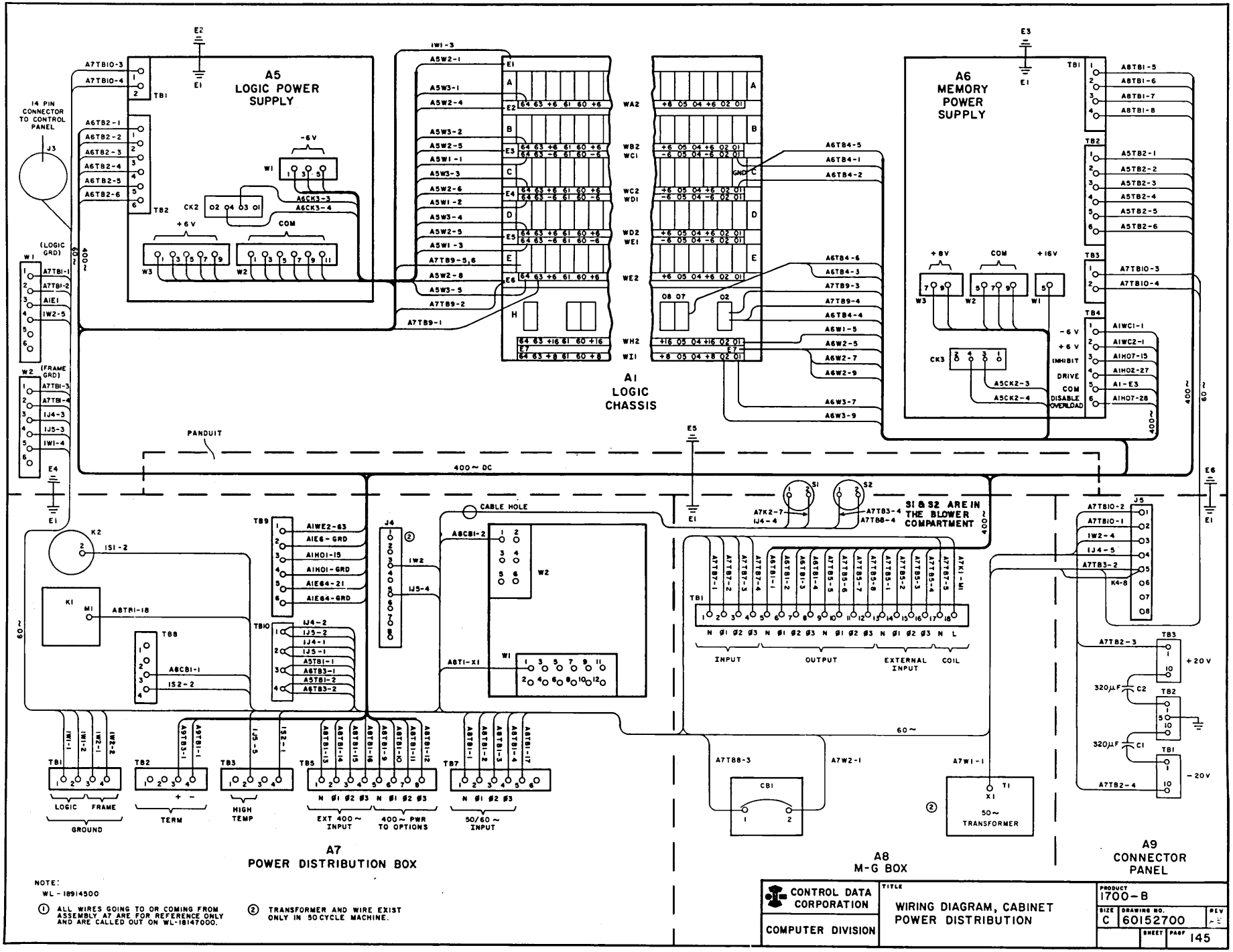




CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE 400 ~ TERMINATOR POWER SUPPLY 40 VDC	PRODUCT 1700 SIZE C · DRAWING NO. 60152700 · REV. AD SHEET · PAGE 141	



CONTROL DATA CORPORATION	TITLE: CABLING DIAGRAM	PRODUCT: 1700	
COMPUTER DIVISION		SIZE: C	DRAWING NO.	REV: R
		SHEET: 70	PAGE: 143

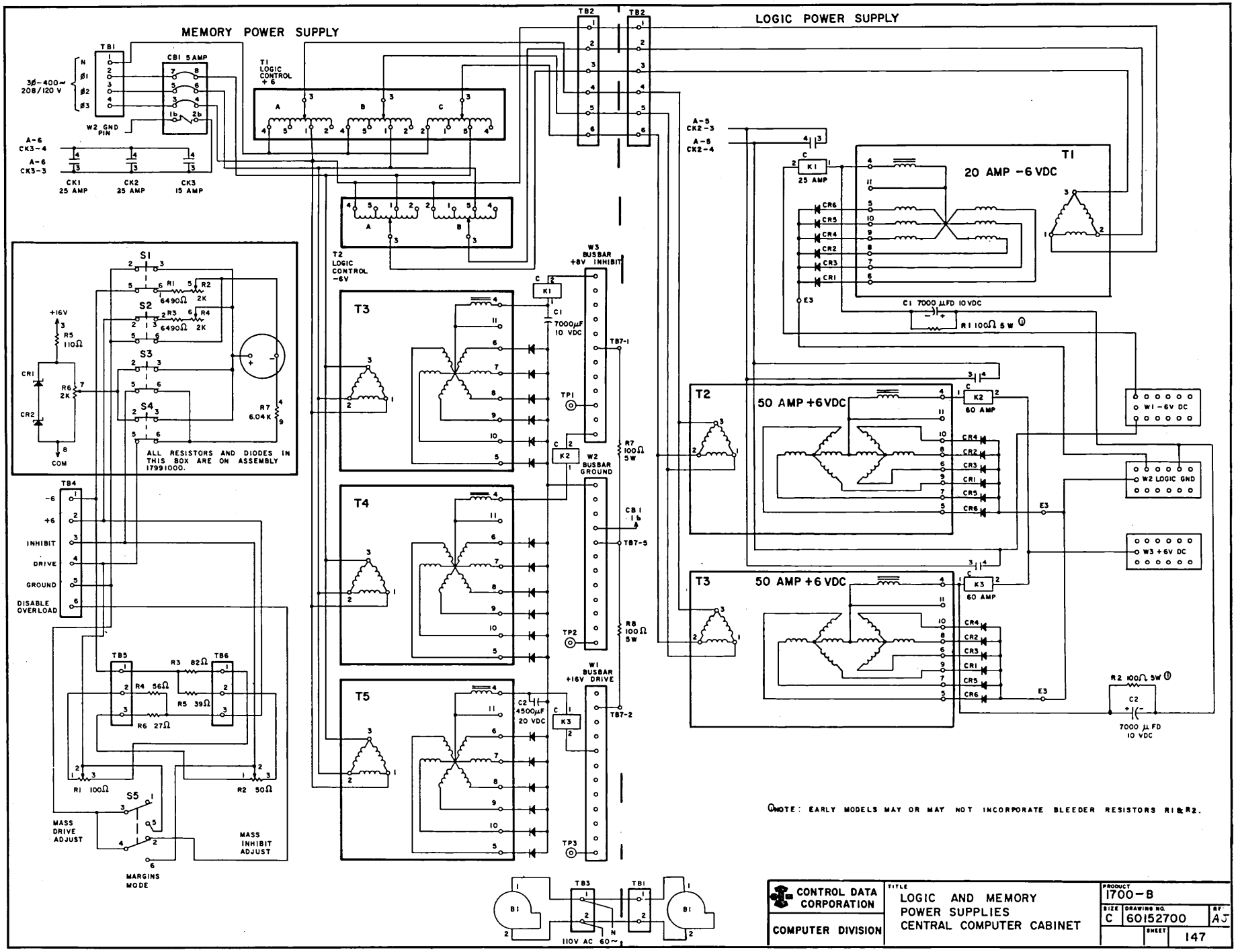


NOTE:
WL - 18914500

① ALL WIRES GOING TO OR COMING FROM ASSEMBLY A7 ARE FOR REFERENCE ONLY AND ARE CALLED OUT ON WL-18147000.

② TRANSFORMER AND WIRE EXIST ONLY IN 50 CYCLE MACHINE.

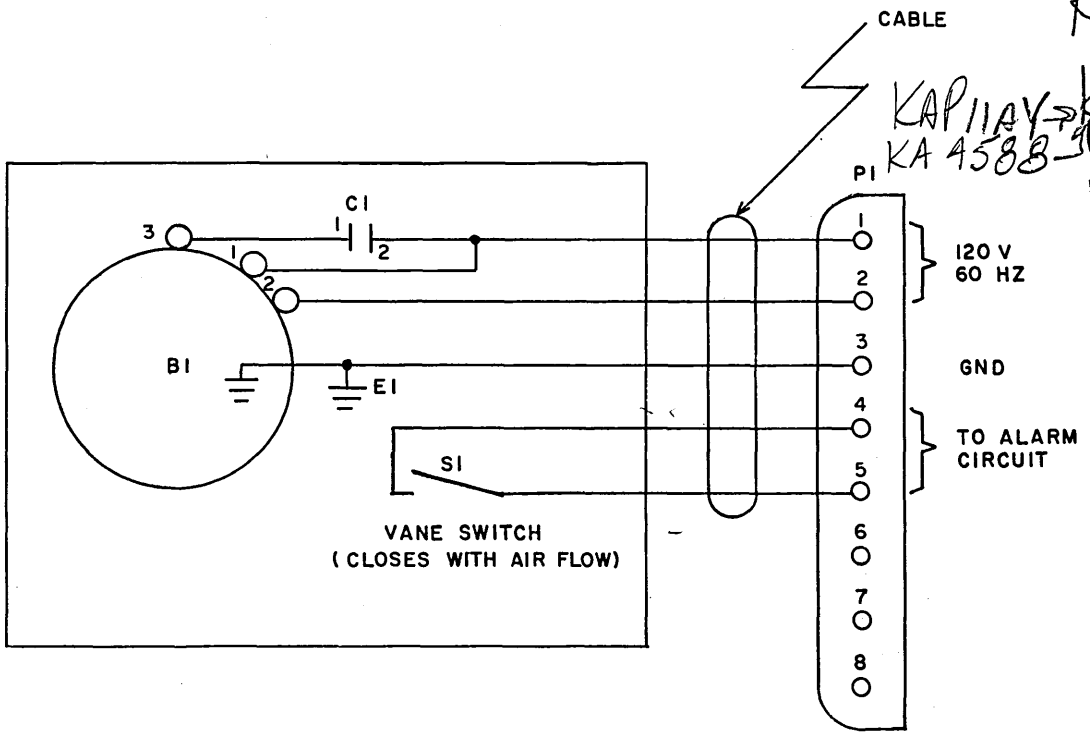
CONTROL DATA CORPORATION	TITLE: WIRING DIAGRAM, CABINET POWER DISTRIBUTION	PRODUCT: 1700-B	
COMPUTER DIVISION		SIZE: C	DRAWING NO.: 60152700
		SHEET:	PAGE: 145



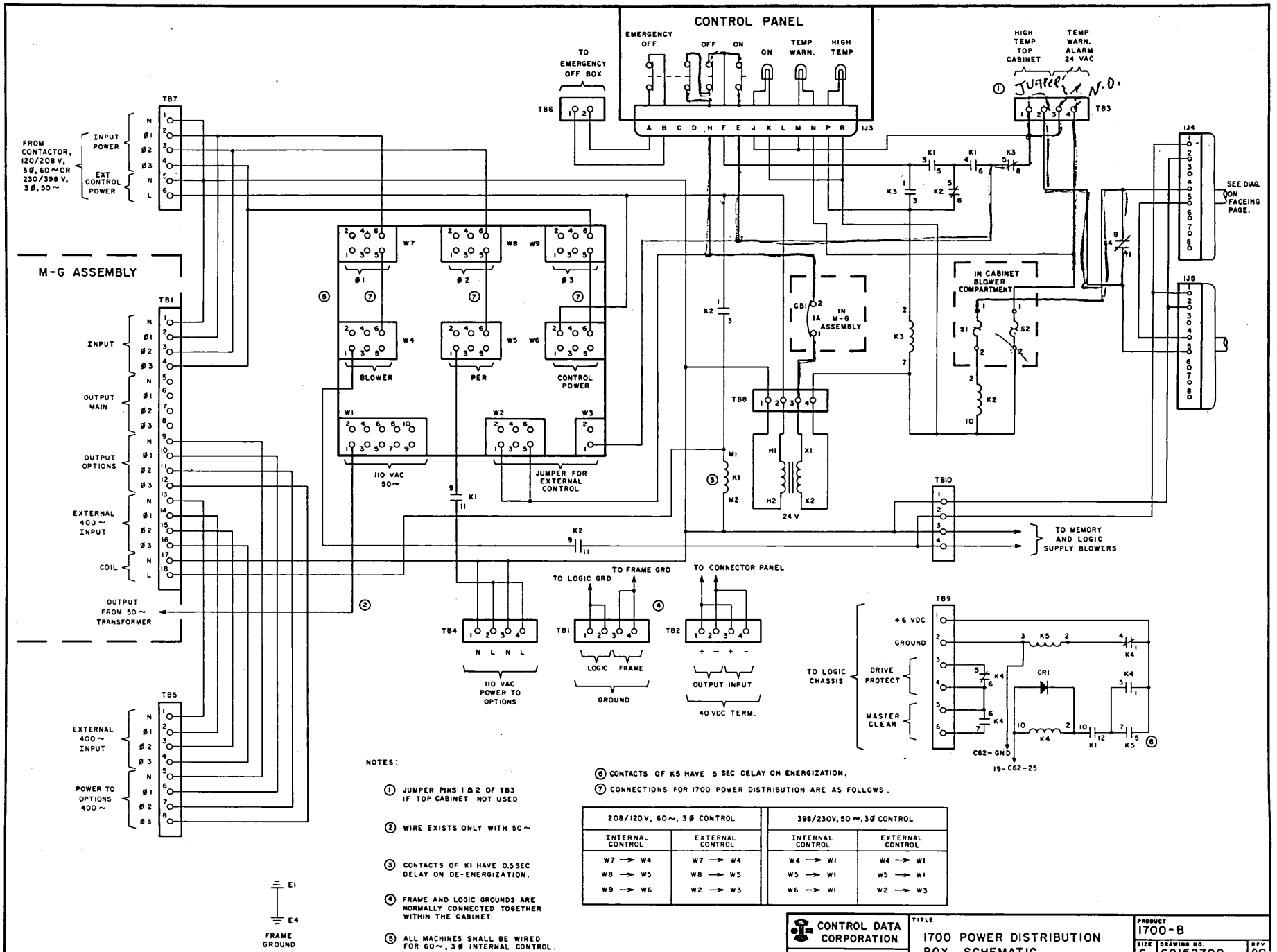
CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE LOGIC AND MEMORY POWER SUPPLIES CENTRAL COMPUTER CABINET	PRODUCT 1700-B SIZE C · DRAWING NO. 60152700 · REV. AJ SHEET 147	

K3 = POTTER & BRUMFIELD

K2 = 24 VAC
K3 = 24 VDC
K4 = 6 VDC



BLOWER ASSEMBLY



NOTES:

1. JUMPER PINS 1 & 2 OF TB3 IF TOP CABINET NOT USED
2. WIRE EXISTS ONLY WITH 50~
3. CONTACTS OF K1 HAVE 0.5 SEC DELAY ON DE-ENERGIZATION.
4. FRAME AND LOGIC GROUNDS ARE NORMALLY CONNECTED TOGETHER WITHIN THE CABINET.
5. ALL MACHINES SHALL BE WIRED FOR 60~, 3Ø INTERNAL CONTROL.
6. CONTACTS OF K5 HAVE 5 SEC DELAY ON ENERGIZATION.
7. CONNECTIONS FOR 1700 POWER DISTRIBUTION ARE AS FOLLOWS.

208/120V, 60~, 3Ø CONTROL		398/230V, 50~, 3Ø CONTROL	
INTERNAL CONTROL	EXTERNAL CONTROL	INTERNAL CONTROL	EXTERNAL CONTROL
W7 → W4	W7 → W4	W4 → W1	W4 → W1
W8 → W5	W8 → W5	W5 → W1	W5 → W1
W9 → W6	W2 → W3	W6 → W1	W2 → W3

CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE: 1700 POWER DISTRIBUTION BOX, SCHEMATIC. ASSEMBLY - A7

PRODUCT: 1700-B
SIZE: C
DRAWING NO.: 60152700
DFV: AB
SHEET:
PAGE: 149

CARD PLACEMENT (CROSS REFERENCE)
CONTROL DATA CORPORATION
COMPUTER DIVISION
PRODUCT 1700
SIZE C
DRAWING NO. 60152700
SHEET 71
PAGE 151
REV
TITLE
CARD TYPE
PAGE
LOGICAL FUNCTION
A
B
C
D
E
PROGRAM PROTECT & STORAGE PROTECT FAULT
PARITY CHECKER BITS 9-17
WRITE CONTROL
PARITY CONTROL
PARITY CHECKER BITS 0-8
STORAGE TIMING FANOUT
RAW CLOCK FANOUT 150 & 175
Z REGISTER BITS 16,17
BITS 14,15
BITS 12,13
BITS 10,11
BITS 8,9
BITS 6,7
BITS 4,5
BITS 2,3
Z REGISTER BITS 0,1
SEE LOW SPEED SYNCHRONIZER MANUAL
Z FAN-IN, BITS 6-8
BITS 3-5
Z FAN-IN, BITS 0-2
BANK DRIVE SELECTION BANKS 4-7
BANK DRIVE SELECTION BANKS 0-3
RAW CLOCK FANOUT 150 & 175
RAW CLOCK FANOUT 100 & 125
S REGISTER BITS 2,3,5,13
S REGISTER BITS 0,1,4,12
STORAGE TIMING CHAIN EXCURSION COUNTER
CHANNEL ACTIVE FANOUT
LOGICAL FUNCTION MISCELLANEOUS
Z FAN-IN, BITS 15-17
BITS 12-14
Z FAN-IN, BITS 9-11
READ/WRITE INHIBIT FF
S REGISTER BITS 8,9,11
S REGISTER BITS 6,7,10,14
LOGIC FUNCTION-MISC.
STORAGE CHANNEL ACTIVE
STORAGE TIMING CHAIN 1
STORAGE TIMING CHAIN 2
TRANSMITTER/RECEIVER A/Q DATA BIT 0 REJECT, REPLY
TRANSMITTER/RECEIVER A/Q DATA BITS 1-3
BITS 4-6
BITS 7-9
BITS 10-12
TRANSMITTER/RECEIVER A/Q DATA BITS 13-15
TRANSMITTER; READ, WRITE, W=0, PROGRAM PROTECT
TRANSMITTER; MC AQ, MC EXT., Z17
TRANSMITTER/RECEIVER STORAGE DATA BIT 15
BITS 12-14
BITS 9-11
BITS 6-8
BITS 3-5
TRANSMITTER/RECEIVER STORAGE DATA BITS 0-2
ADDRESS RECEIVERS BITS 8,9,10,11,14
BITS 3,5,13,6,7
ADDRESS RECEIVERS BITS 0,1,2,4,12
CONTROL RECEIVERS
CONTROL TRANSMITTERS
S REG FANOUT BITS 10,11
BITS 4,5
BITS 6-9
S REG FANOUT BITS 0-3
BANK 3 SENSE AMPS BITS 12-17
BITS 6-11
BANK 3 SENSE AMPS BITS 0-5
BANK 2 SENSE AMPS BITS 12-17
BITS 6-11
BANK 2 SENSE AMPS BITS 0-5
TRANSMITTER; Q REGISTERS BITS 0-3
BITS 4-7
BITS 8-11
TRANSMITTER; Q REGISTERS BITS 12-15
INTERRUPT RECEIVERS, LINES 1-5
LINES 6-10
INTERRUPT RECEIVERS LINES 11-15
BANK 1 SENSE AMPS BITS 12-17
BITS 6-11
BANK 1 SENSE AMPS BITS 0-5
Z FANOUT BANK 0,1 BITS 12-17
BITS 6-11
Z FANOUT BANK 0,1 BITS 0-5
BANK 0 SENSE AMPS BITS 12-17
BITS 6-11
BANK 0 SENSE AMPS BITS 0-5
NOTES:
COLUMNS 32 & 33 HAVE BEEN REPLACED BY A DIVIDER STRIP.
① REPLACED BY A V48 MODULE WHEN A 1705 IS NOT INCLUDED.
② INCLUDED ONLY WITH 1705.
③ INCLUDED ONLY WITH CORRESPONDING STORAGE BANK OPTION.
④ REMOVE IF 8K OR LESS.
⑤ REMOVE IF 16K OR LESS

	A	CARD TYPE	PAGE	LOGICAL FUNCTION	B	CARD TYPE	PAGE	LOGICAL FUNCTION	C	CARD TYPE	PAGE	LOGICAL FUNCTION	D	CARD TYPE	PAGE	LOGICAL FUNCTION	E	CARD TYPE	PAGE	LOGICAL FUNCTION
64	V68	V68	17	REGISTER DISPLAY, BITS 8-15	V68	V68	17	REGISTER DISPLAY, BITS 0-7	V68	V68	17	STATUS DISPLAYS	V67	V67	17	PANEL SWITCH CONTROLS	V66	V66	17, 19, 21	PANEL SWITCH CONTROLS
63	V49	V49	13,19 59	STOP-GO CONTROLS					Z93	Z93	45	XR & LP CONTROLS	V30	V30	15,21	REGISTER SELECTION	V85	V85	19	TEST MODE & MASTER CLEAR
62	V65	V65	73	SIGN RECORD FF'S	TC	TC	3	RAW CLOCK FANOUT, †00	W00	W00	19	LOGIC VOLTAGE SENSOR	Z94	Z94	73	SHIFT CYCLE FF	V52	V52		CARD STORAGE
61	V73	V73	73	MULTIPLY & DIVIDE STEP	V37	V37	47	SHIFT FF'S	TC	TC	3	RAW CLOCK FAN-OUT, †25 & †50					V51	V51		CARD STORAGE
60					V23	V38	47	SHIFT SIGNAL FAN-OUTS	V38	V38	21,45	XR & LP FF'S								
59	V35	V35	7,49	AUGEND INPUT CONTROLS	V34	V34	49	AUGEND INPUT CONTROLS	V33	V33	9,51	STO I FAN-OUT & ADDEND INPUT CONTROLS	V32	V32	51	ADDEND INPUT CONTROLS	V02	V02	④ ⑤	BANK 7 SENSE AMPS BITS 12-17
58	V04	V04	7,49	AUGEND INPUT TRANSFERS (A,+1)	V04	V04	7,49	AUGEND INPUT TRANSFERS (Y,X)	V04	V04	7-51	ADDEND INPUT TRANSFERS (Q,X)	V04	V04	7,51	ADDEND INPUT TRANSFERS (P, MASK)	V02	V02	④ ⑤	89, 93, 91,93 97,99 BITS 6-11
57	V80	V80	29	F TRANSLATIONS	V10	V10	59-65	SECTION 1, LOOK AHEAD	V10	V10	59-65	SECTION 0, LOOK AHEAD	V62	V62	13	ADDRESS CONTROL II	V02	V02	④ ⑤	83, 85, 85,87 87,89 BANK 7 SENSE AMPS BITS 0-5
56	V00	V00	63	ADDER, GROUP 4	V00	V00	63	ADDER, GROUP 5	V00	V00	65	ADDER, GROUP 6	V00	V00	65	ADDER, GROUP 7	V02	V02	④	BANK 6 SENSE AMPS BITS 12-17
55	V00	V00	61	ADDER, GROUP 3	V00	V00	61	ADDER, GROUP 2	V00	V00	59	ADDER, GROUP 1	V60	V60	57	ADDER, GROUP 0	V61	V61	57	ADDER/SHIFTER OUTPUT, BITS 0,15
54	V06	V06	61,63	ADDER/SHIFTER FAN-OUT, BITS 5-8	V06	V06	61,63	ADDER/SHIFTER FAN-OUT, BITS 3,4,9,10	V06	V06	21,59, 65	ADDER/SHIFTER FAN-OUT, BITS 1,2,11,12	V06	V06	21,59, 65	ADDER/SHIFTER FAN-OUT, BITS 0,13-15	V02	V02	④	BANK 6 SENSE AMPS BITS 6-11
53	V03	V03	53	AUGEND, BITS 5-8	V03	V03	53	AUGEND, BITS 3,4,9,10	V03	V03	53	AUGEND, BITS 1,2,11,12	V03	V03	53	AUGEND, BITS 0,13-15	V25	V25	11	CYCLE CONTROL & C CYCLE
52	V03	V03	55	ADDEND, BITS 5-8	V03	V03	55	ADDEND, BITS 3,4,9,10	V03	V03	55	ADDEND, BITS 1,2,11,12	V03	V03	55	ADDEND, BITS 0,13-15	V24	V24	11	A CYCLE
51	V77	V77	25	F TRANSLATIONS	V75	V75	25	F TRANSLATIONS	V81	V81	29	F TRANSLATIONS	V79	V79	27	F TRANSLATIONS	V24	V24	11	B CYCLE
50	V76	V76	25,75	F TRANSLATIONS	V19	V19	39	X REGISTER FAN-IN, BITS 0-7	V15	V15	21,31	A REGISTER FAN-IN, BIT 0-5	V78	V78	21,27	F TRANSLATIONS	V02	V02	④	BANK 6 SENSE AMPS BITS 0-5
49	V22	V22	41	Y REGISTER FAN-IN, BITS 0-5	V19	V19	39	X REGISTER FAN-IN, BITS 8-15	V16	V16	9,21,31	ROP I FAN-OUT & A REGISTER FAN-IN, BITS 6-9	V01	V01	33	Q REGISTER, BITS 0-7	V31	V31	3	CLOCK FAN-OUT
48	V01	V01	41	Y REGISTER, BITS 0-6, 8	V57	V57	23	F REGISTER, BITS 12-15	V15	V15	31	A REGISTER FAN-IN, BITS 10-15	V01	V01	33	Q REGISTER, BITS 8-15	V30 V31	TD	3,5	CLOCK ADJUST; NORMAL (V50), SLOW (V51), FAST (V52)
47	V01	V01	41	Y REGISTER, BITS 7,9-15	V01	V01	39	X REGISTER, BITS 0-7	V57	V57	23	F REGISTER, BITS 8-11	V07	V07	33,35	Q REGISTER FAN-OUT, BITS 0-5	TD	TD	3,5	10 MC OSCILLATOR
46	V13	V13	41	Y REGISTER FAN-OUT, BITS 0-6	V01	V01	39	X REGISTER, BITS 8-15	V01	V01	21,31	A REGISTER, BITS 0-7	V07	V07	33,35	BITS 6-11	TC	TC	3	RAW CLOCK FAN-OUT, †00 & †50
45	V14	V14	41,69	Y REGISTER FAN-OUT, BITS 7-14	V26	V26	39	X REGISTER FAN-OUT, BITS 0-4	V01	V01	21,31	A REGISTER, BITS 8-15	V05	V05	7,33,35	Q REGISTER FAN-OUT, BITS 12-15	V02	V02	④	BANK 5 SENSE AMPS BITS 12-17
44	V01	V01	37	P REGISTER, BITS 0-7	V27	V27	39	BITS 5,7	V07	V07	35	A REGISTER FAN-OUT, BITS 0-5	V09	V09	71	MASK & INTERRUPT REG. BITS 0-3	V02	V02	④	BITS 6-11
43	V01	V01	37	P REGISTER, BITS 8-14	V28	V28	39	BITS 8-11	V05	V05	7,35	BITS 6-9	V09	V09	① 67	BITS 4-7	V02	V02	④	BANK 5 SENSE AMPS BITS 0-5
42	V42	V42	41	Y REGISTER CONTROLS	V28	V28	39	X REGISTER FAN-OUT, BITS 12-15	V07	V07	35	A REGISTER FAN-OUT, BITS 10-15	V09	V09	① 67	BITS 8-11	V86	V86	④ 97,99,00	Z REGISTER FAN-OUT BANKS 2-7 BITS 15-17
41	V43	V43	41	Y REGISTER CONTROLS	TC	TC	3	RAW CLOCK FAN-OUT, †00 & †25	V40	V40	21,31	A REGISTER CONTROL	V09	V09	① 67	MASK & INTERRUPT REG. BITS 12-15	V86	V86	④ 95,97	BITS 12-14
40	V46	V46	9,37	ADR FAN-OUT & ADDER → P	V45	V45	7,39	ADDER → X	V56	V56	23	F REGISTER CONTROL	V59	V59	69	INTERRUPT CONTROL	V86	V86	④ 91,93	BITS 9-11
39	V08	V08	43	Y DECREMENTER	V63	V63	13	ADDRESS CONTROL I	V70	V70	9	REG & ADR FF'S	V44	V44	33,71	Q & MASK REGISTER CONTROLS	V86	V86	④ 89,91	BITS 6-8
38	V69	V69	7,21	TIMING CHAIN (H00-H03)	V69	V69	7	TIMING CHAIN (H04-H07)	V71	V71	9	ROP II, STO II & RNI FF'S	V11	V11	① 71	INTERRUPT PRIORITY BITS 8-15	V86	V86	④ 85,87	BITS 3-5
37					TD	TD	7	X50 TIME FAN-OUTS	V64	V64	9	ROP I & STO I FF'S	V12	V12	71	INTERRUPT PRIORITY BITS 0-7	V86	V86	④ 83,85	Z REGISTER FAN-OUT BANKS 2-7 BITS 0-2
36					V06	V06	7,19,69	GENERAL FAN-OUTS	V41	V41	15,21	REGISTER CLEAR CONTROLS	V58	V58	57	OVERFLOW FAULT FF	V02	V02	④	BANK 4 SENSE AMPS BITS 12-17
35	V54	V54	69	PROGRAM PROTECT FAULT	V55	V55	7,21	TIMING CHAIN & DISPLAY CONTROL					Z81	Z81	43	SKIP TRANSLATIONS	V02	V02	④	BITS 6-11
34	V82	V82	39,101	STORAGE INTERFACE	V74	V74	75	REPLY & REJECT					V53	V53	43,75	SKIP & I/O CONTROL	V02	V02	④	BANK 4 SENSE AMPS BITS 0-5

NOTES:
① REPLACED BY A V48 MODULE WHEN A 1705 IS NOT INCLUDED.
② INCLUDED ONLY WITH 1705.
③ INCLUDED ONLY WITH CORRESPONDING STORAGE BANK OPTION.
④ REMOVE IF 8K OR LESS.

CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE: CARD PLACEMENT (CROSS REFERENCE)

PRODUCT 1700 | SIZE C | DRAWING NO. 60152700 | REV 4K | SHEET 72 | PAGE 153

MAINTENANCE

AA 101 & 1704

PREVENTIVE MAINTENANCE INDEX

Level 1 ---------- Weekly

Level 2 ---------- Monthly

Level 3 ---------- 6 Months

LEVEL 3 2 1	ITEM	PREVENTIVE MAINTENANCE
	0.1	Preliminary Information
X*	2.1	Clean Air Filters
X	2.2	Check Logic Voltages
X	2.3	Check Indicators
X	2.4	Check Console Controls
X	2.5	Run Diagnostics (Margins Applied)
X	2.6	Check Logic Voltages
X	3.1	Perform Shock Testing (Memory Stacks and Sense Amps)
X	3.2	Check Indicators
X	3.3	Check Emergency Off - On
X	3.4	Run Diagnostics (Logic Voltage Margins Applied)
X	3.5	Perform Shock Testing

*Level 1 if necessary.

0.1 PRELIMINARY INFORMATION

MARGIN TABLE

CONDITIONS	LOGIC VOLTAGE		DRIVE	INHIBIT	CLOCK FREQUENCY
	+6	-6			
1	Normal	Normal	Normal	Normal	Normal
2	+10%	+10%	Normal	Normal	Normal
3	-10%	-10%	Normal	Normal	Normal
4	Normal	Normal	Normal	Normal	+10%
5	Normal	Normal	Normal	Normal	-10%

NOTES

1. Where level 2 or level 3 PM procedures overlap level 1 or level 2 procedures, only the highest level procedures need be performed.
2. Shock testing (Item 2.1) should be performed using the standard AMP insertion tool with the special nylon shock testing tip (P/N 12209308).

2.1 CLEAN AIR FILTERS

CHECK/Conditions	Action
1. System power on.	1. Remove each of the bottom air filters from both of the air filter compartments (base of the 1704). 2. If the filter is not extremely dirty, it may be cleaned with a vacuum cleaner. If required, the filter should be washed gently in a detergent - water solution. Place the filter vertically while washing to avoid damaging it. 3. Replace corroded filters with new filters. 4. Replace the new or clean filter on top of the filters still in each filter compartment.

2.2 CHECK LOGIC VOLTAGE

CHECK/Conditions | Action

1. System power on.

+6 VOLT LOGIC SUPPLY

2. Depress the +6 volt button on the memory power supply.

CHECK: Does the percentage meter read 0%?

Yes ↓

No → 1. Adjust the +6 volts.
2. Repeat CHECK.

-6 VOLT LOGIC SUPPLY

3. Depress the -6 volt button on the memory power supply.

CHECK: Does the percentage meter read 0%?

Yes ↓

No → 1. Adjust the -6 volts.
2. Repeat CHECK.

Go to next item.

2.3 CHECK INDICATORS

NOTE

The 1700 Computer Reference Manual explains in detail the operation and indication of all console switches and bit switches. This manual should be readily available for reference while completing these CHECKS. In the event that a given switch, indicator or display does not perform properly, isolate and correct the problem.

CHECK/Conditions	Action
1. System power on.	
2. While manually operating all bit switches and display switches, complete the following:	
CHECK: Do all the bit switches set and clear all six (6) register displays correctly without sticking or binding?	
Yes ↓	No → 1. Take appropriate action. 2. Correct discrepancy. 3. Repeat CHECK.
CHECK: Are all the Drive and Inhibit lights on the memory stacks lit?	
Yes ↓	No → 1. Correct discrepancy. 2. Repeat CHECK.
Go to next item.	

2.4 CHECK CONSOLE CONTROLS

CHECK/Conditions

1. System power on.
2. While performing the operations listed in Item 1.5 (Run Diagnostics; No Margins).

CHECK: Do the console toggle switches operate correctly? (Reference: 1700 Computer Reference Manual) (Reference: SMM Manual).

Action

Yes

No → 1. Isolate and correct problem.

2. Repeat CHECK.

↓

Go to next item.

2.5 RUN DIAGNOSTICS (MARGINS APPLIED)

NOTE

Use an accurate D.C. Voltmeter when setting margins. On a rotational basis, run all operational tests under all conditions as set forth below, such that all conditions are covered at least once a month.

DO NOT PERFORM MARGIN TEST WHILE COMPUTER IS ACTIVELY MONITORING ANY PROCESS CONTROL FUNCTION.

TABLE 1

1.	SMM17	Command Test	(3 Passes)
2.	SMM17	Memory Test	(3 Passes)
3.	Random Protect Test		(1 Pass)

CHECK/Conditions	Action
1. System power on.	
2. With logic voltages at condition 1 (see margin table; item 0.1, Preliminary information).	1. Run all tests in Table 1 and - 2. Correct any errors.
3. Set margins at condition 2 (see margin table).	1. Run all tests in Table 1 (excluding the memory test) and - 2. Correct any errors.
4. Set margins at condition 3 (see margin table).	1. Run all tests in Table 1 (excluding the memory test) and - 2. Correct any errors.

2.5 (Continued)

CHECK/Conditions	Action
5. Determine the best operating point for each memory stack, as per the procedure in revision E of the 1700 Maintenance Manual.	
NOTE Step 5 may be omitted if previously performed, and if the margins in Step 6 have not deteriorated from those found previously.	
CHECK: Does each stack have at least 1.0 volt drive swing at the best operating point?	
Yes ↓	No → 1. Correct by replacing defective module or stack.
6. After the stacks have been adjusted to their best operating point, determine the mass memory margins by varying the mass memory pots while running the worst pattern of the 1700 SMM memory test. Record these margins (from the meter on the power supply) for future reference.	

2.6 CHECK LOGIC VOLTAGES

CHECK/Conditions

1. System power on.
2. Ensure that the +16 volt memory bus bar - is at least +16 volts.
3. Ensure that the +8 volt memory bus bar - is at least +8 volts.
4. Use your most accurate D.C. Voltmeter to check the +6 volt logic voltage setting. Ensure that the percentage meter says 0% when the actual measured voltage is +6.0 volts.

CHECK: Is the percentage meter zeroed with a +6 volt setting?

Yes

No → Action

1. To zero the percentage meter, remove the memory power supply access panel. Adjust the correct potentiometer on the printed circuit board (upper left hand corner of the power supply).
2. Replace access panel.
3. Repeat CHECK

5. Use your most accurate D.C. Voltmeter to check the -6 volt logic voltage setting: Ensure that the percentage meter says 0% when the actual measured voltage is -6.0 volts.

2.6 (Continued)

CHECK/Conditions	Action
CHECK: Is the percentage meter zeroed with a -6 volt setting?	
Yes: Go to next item.	
No →	1. To zero the percentage meter: Remove the memory power supply access panel. Adjust the correct potentiometer on the printed circuit board (upper left hand corner of the power supply).
	2. Replace access panel.
	3. Repeat CHECK.

3.1 PERFORM SHOCK TESTING

NOTE

DO NOT PERFORM SHOCK TEST WHILE COMPUTER IS ACTIVELY MONITORING ANY PROCESS CONTROL FUNCTION.

CHECK/Conditions	Action
1. System power on.	
2. Load and execute the SMM17 Memory Test. Select parameters to test one stack at a time.	
3. While monitoring test, shock test the selected memory sense amp module and memory stack (use shock test tip).	
CHECK: Is test still running?	
Yes	No → 1. Repair or replace shock sensitive module or stack.
	2. Repeat CHECK.
4. Go back to Step 2 and select the next stack.	

3.2 CHECK INDICATORS

CHECK/Conditions — Action

1. System power on.

OVERFLOW, PROGRAM PROTECT, PARITY ERROR

2. All console switches to neutral.
   Set the ENTER switch. Enter $0901_{(16)}$ in the X register.
3. Place computer in run.
   Do not step or clear the computer until Step 6 has been completed.
4. Return ENTER switch to neutral.

CHECK: Did the overflow light come on?

Yes — No → 1. Isolate and correct problem.
2. Repeat CHECK.

5. Set the ENTER switch again.
   Set the PROGRAM PROTECT switch.

CHECK: Is the Program Protect Fault Light Lit?

Yes — No → 1. Isolate and correct problem.
2. Repeat CHECK.

6. Return ENTER switch to neutral.
   Return the PROGRAM PROTECT switch to neutral.

3.2 (Continued)

CHECK/Conditions | Action

Ground B21, test point 6.

CHECK: Is the Parity Error Light Lit?

Yes ↓ | No → 1. Isolate and correct problem.
2. Repeat CHECK.

INSTRUCTION, INDIRECT ADDRESS, STORAGE INDEX, OPERAND

1. Enter C501 $_{(16)}$ in memory at P = 0000.
   Enter 0000 $_{(16)}$ in memory at P = 0001.
   Enter 0000 $_{(16)}$ in memory at P = 00FF.
2. Master clear.
3. All toggle switches in neutral.

CHECK: Are the Instruction and Program Protect Bit lights lit?

Yes ↓ | No → 1. Isolate and correct problem.
2. Repeat CHECK.

4. Depress the STEP switch once.

CHECK: Does the INDIRECT Address light come on?

Yes ↓ | No → 1. Isolate and correct problem.
2. Repeat CHECK.

5. Depress the STEP switch once.

3.2 (Continued)

CHECK/Conditions		Action
CHECK: Does the Storage Index light come on?		
Yes	No →	1. Isolate and correct problem. 2. Repeat CHECK.
↓		
6. Depress the STEP switch once.		
CHECK: Does the Operand light come on?		
Yes	No →	1. Isolate and correct problem. 2. Repeat CHECK.
↓		
Go to next item.		

3.3 CHECK EMERGENCY OFF-ON

CHECK/Conditions	Action
1. System power on. 2. No program in operation.	1. Verify that the EMERGENCY OFF switch works correctly.

3.4 RUN DIAGNOSTICS (LOGIC VOLTAGE MARGINS APPLIED)

NOTE

Use an accurate D.C. Voltmeter when setting margins. On a rotational basis, run the Command Test under the conditions listed, such that all conditions are covered at least once each six months.

DO NOT PERFORM MARGIN TESTS WHILE COMPUTER IS ACTIVELY MONITORING ANY PROCESS CONTROL FUNCTION.

CHECK/Conditions — Action

1. System power on.
2. Load and execute the SMM17 Command Test (three passes for each of the conditions listed).
   a. Condition 2 (Ref. Margin Table: Item 0.1, preliminary information)
   b. Condition 3 (Ref. Margin Table)
   c. Condition 4 (Ref. Margin Table)
   d. Condition 5 (Ref. Margin Table)

CHECK: Does the Command Test successfully run three passes under each of the four marginal conditions?

Yes → Go to next item.

No → 1. Isolate and correct
2. Repeat CHECK.

3.5 PERFORM SHOCK TESTING

NOTE

Schedule shock testing on a rotational basis so that each module is completed once each six months.

CHECK/Conditions	Action
1. System power on.	
2. D.C. Chassis Voltages a. +6 volts b. -6 volts	
3. Storage Drive Margins a. Normal	
4. Clock frequency a. Normal	
5. Load and execute the SMM17 Command Test with parameters selected for 100 operands.	
6. While monitoring test - Shock test each module (use shock test tip).	

CHECK: Does the Command Test run successfully?

Yes ↓

No → 1. Isolate and correct.
2. Repeat CHECK.

3.5 Continued

CHECK/Conditions	Action
7. Load and execute SMM 17 program protect test.	
8. While monitoring test, shock test each module.	
CHECK: Does Program Protect Test run successfully?	
Yes ↓ END	No → 1. Isolate and correct.
	2. Repeat CHECK.

APPENDIX A

INSTRUCTION FLOW CHARTS

This appendix contains flow charts that show the steps in execution of the following instructions.

- Shift Instructions

  ARS - A Right Shift
  ALS - A Left Shift
  QRS - Q Right Shift
  QLS - Q Left Shift
  LRS - Long Right Shift (QA Shift, Right)
  LLS - Long Left Shift (QA Shift, Left)

- Multiply

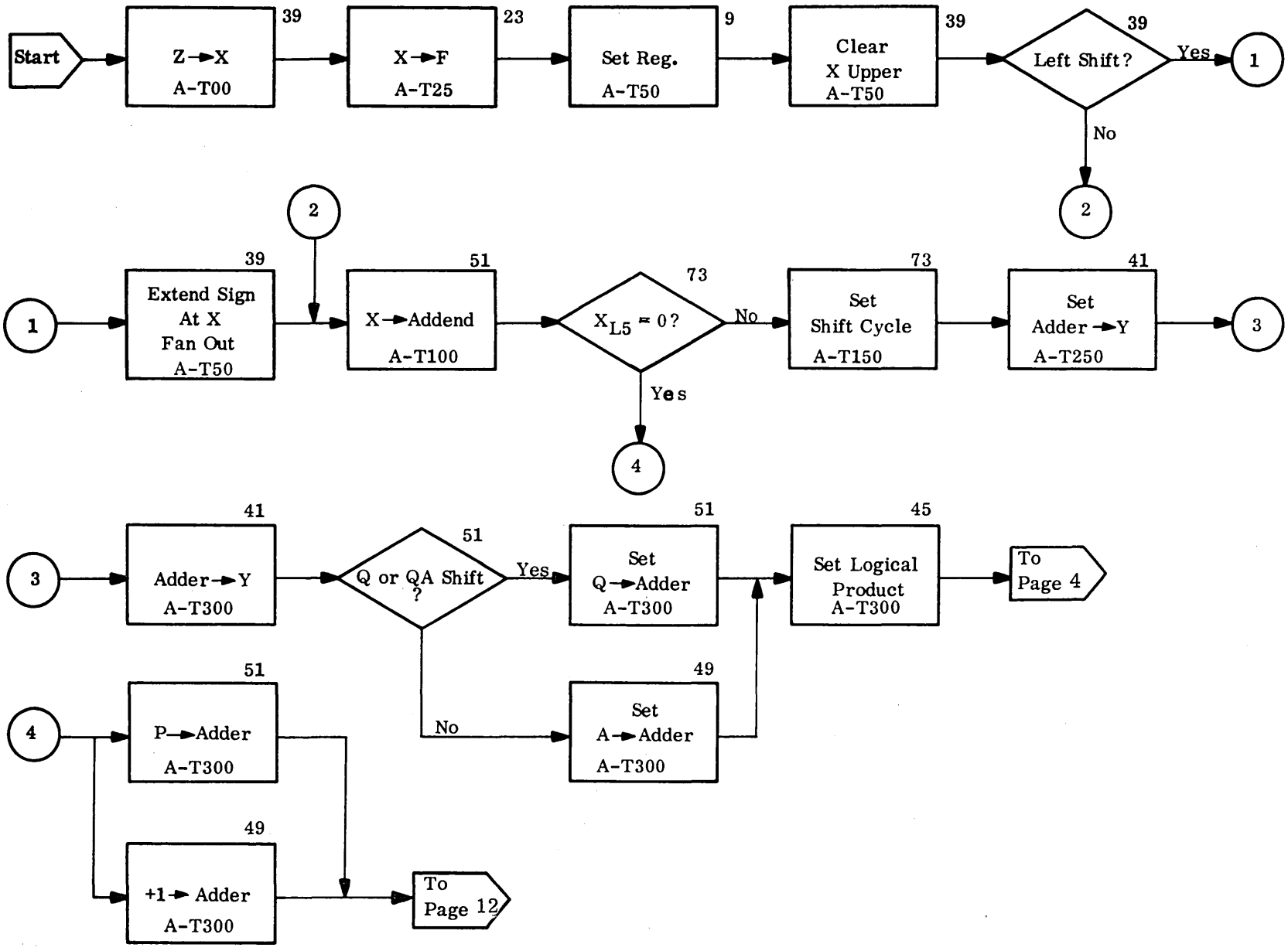
  MUI - Multiply Integer

- Divide

  DVI - Divide Integer

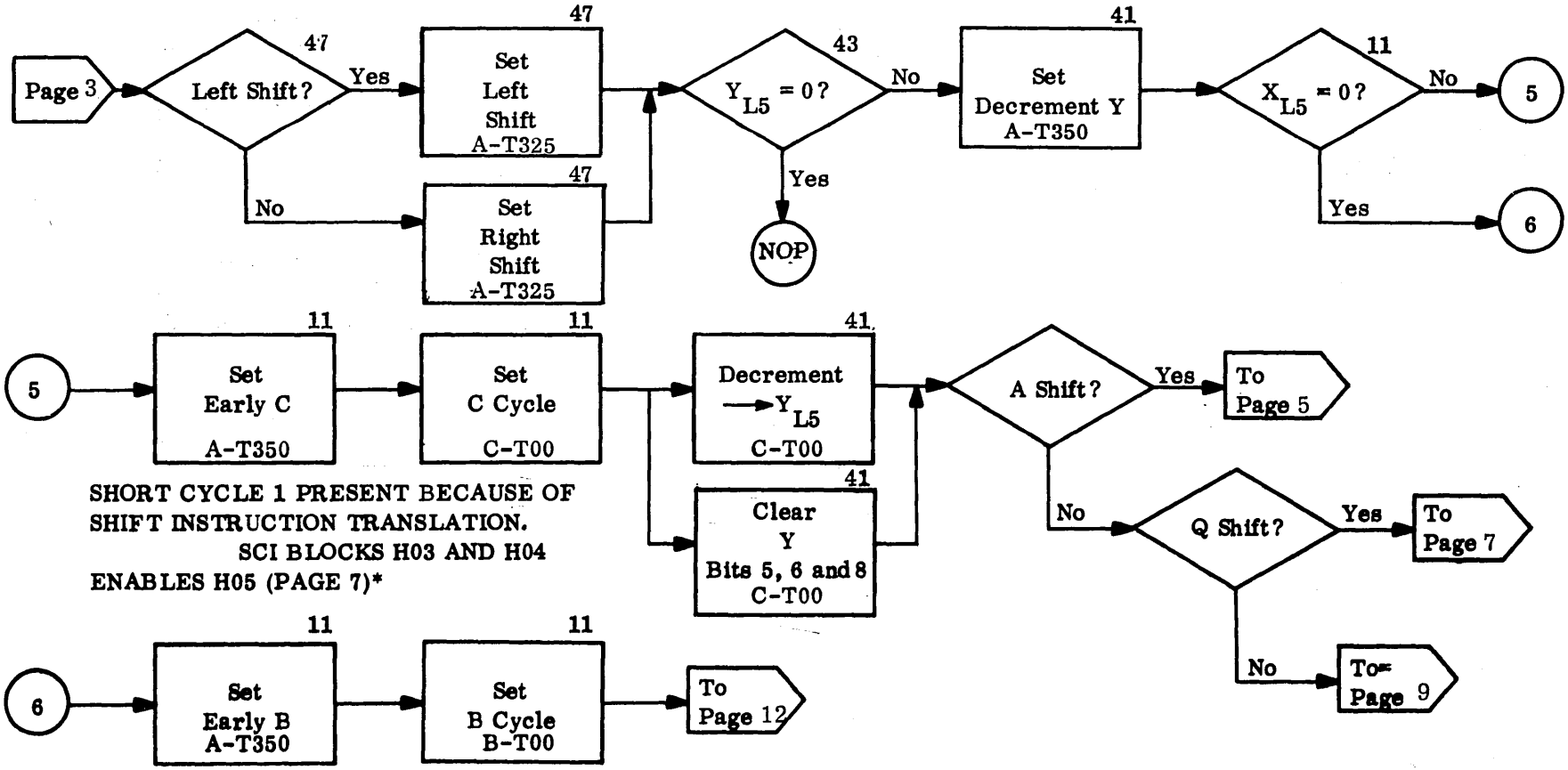
1700 SHIFT OPERATIONS

1700 COMPUTER SHIFT OPERATIONS - ALL SHIFTS



1700 COMPUTER SHIFT OPERATIONS

ALL SHIFTS

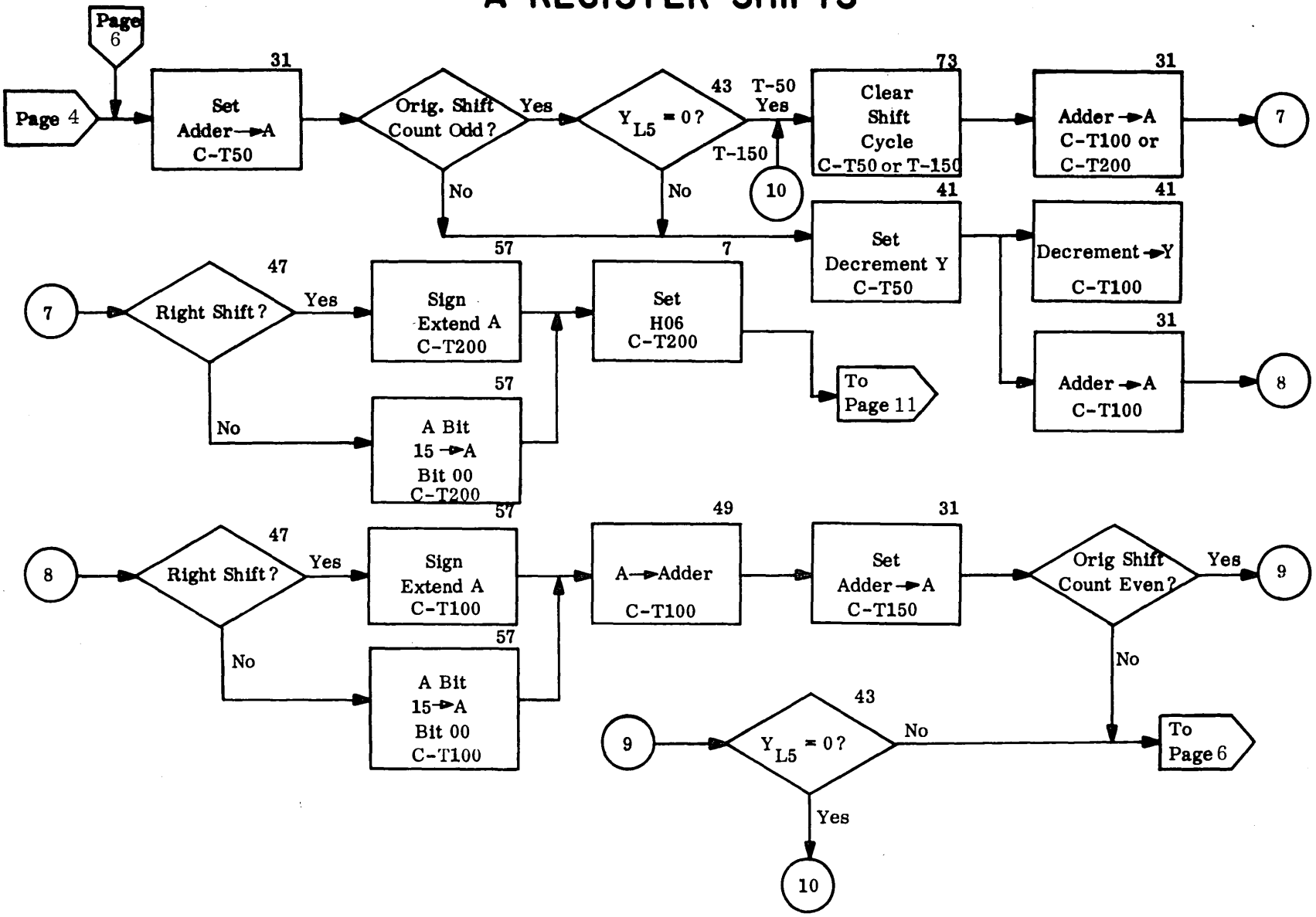


SHORT CYCLE 1 PRESENT BECAUSE OF SHIFT INSTRUCTION TRANSLATION.
SCI BLOCKS H03 AND H04 ENABLES H05 (PAGE 7)*

*SHORT CYCLE 2 PRESENT BECAUSE SHIFT CYCLE F/F IS SET.
SC2 BLOCKS H06 AND H07, ENABLES H00 (PAGE 7)

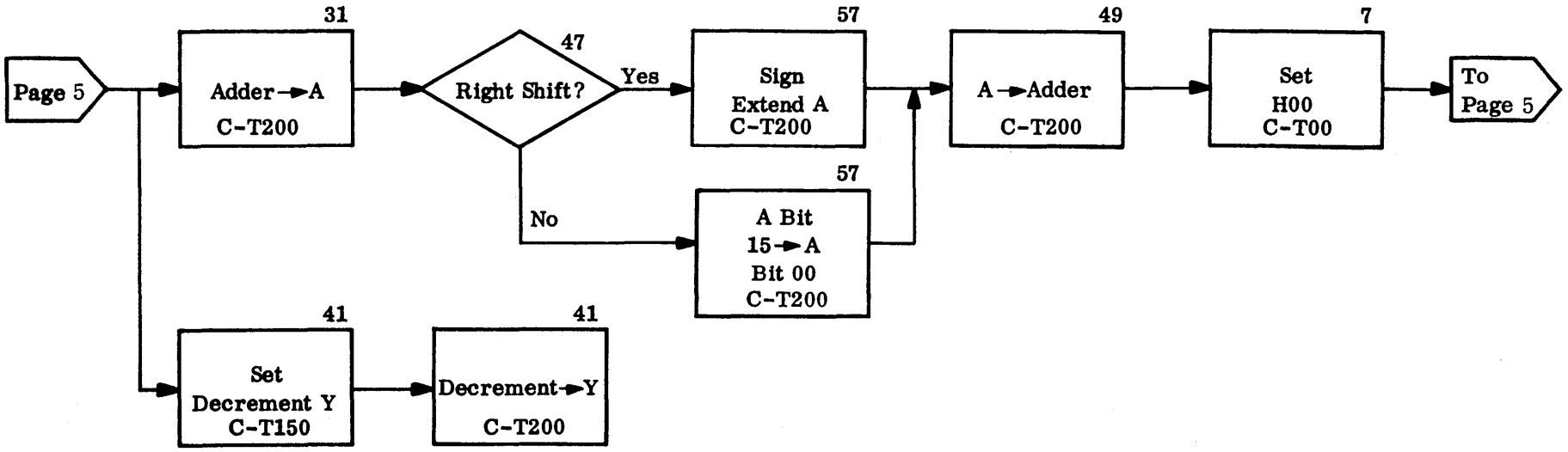
1700 COMPUTER SHIFT OPERATIONS

A REGISTER SHIFTS



1700 COMPUTER SHIFT OPERATIONS

A REGISTER SHIFTS



1700 COMPUTER SHIFT OPERATIONS

Q SHIFTS

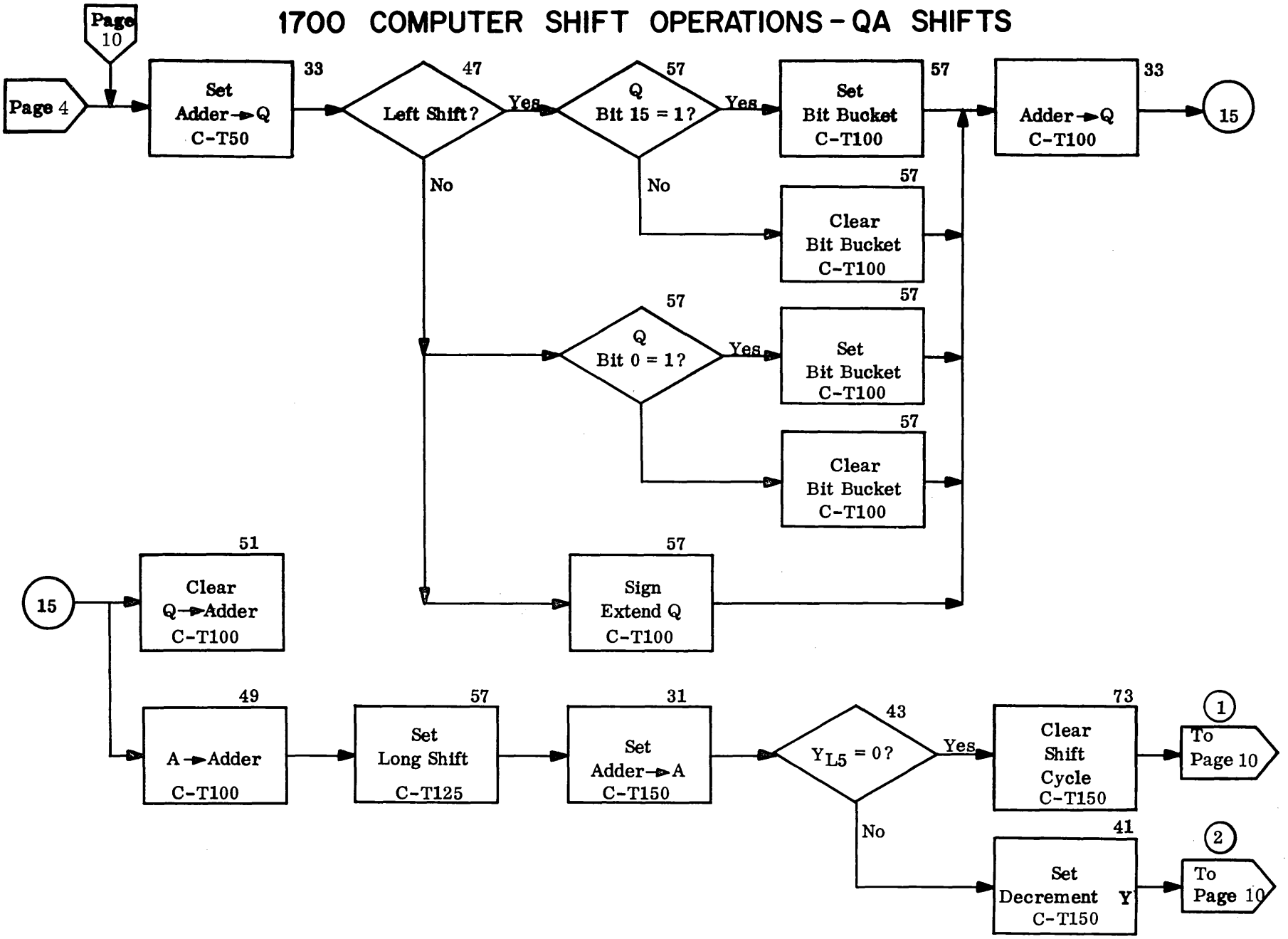
IDENTICAL WITH PAGE 3 OF A SHIFTS BUT WITH Q REGISTER

1700 COMPUTER SHIFT OPERATIONS

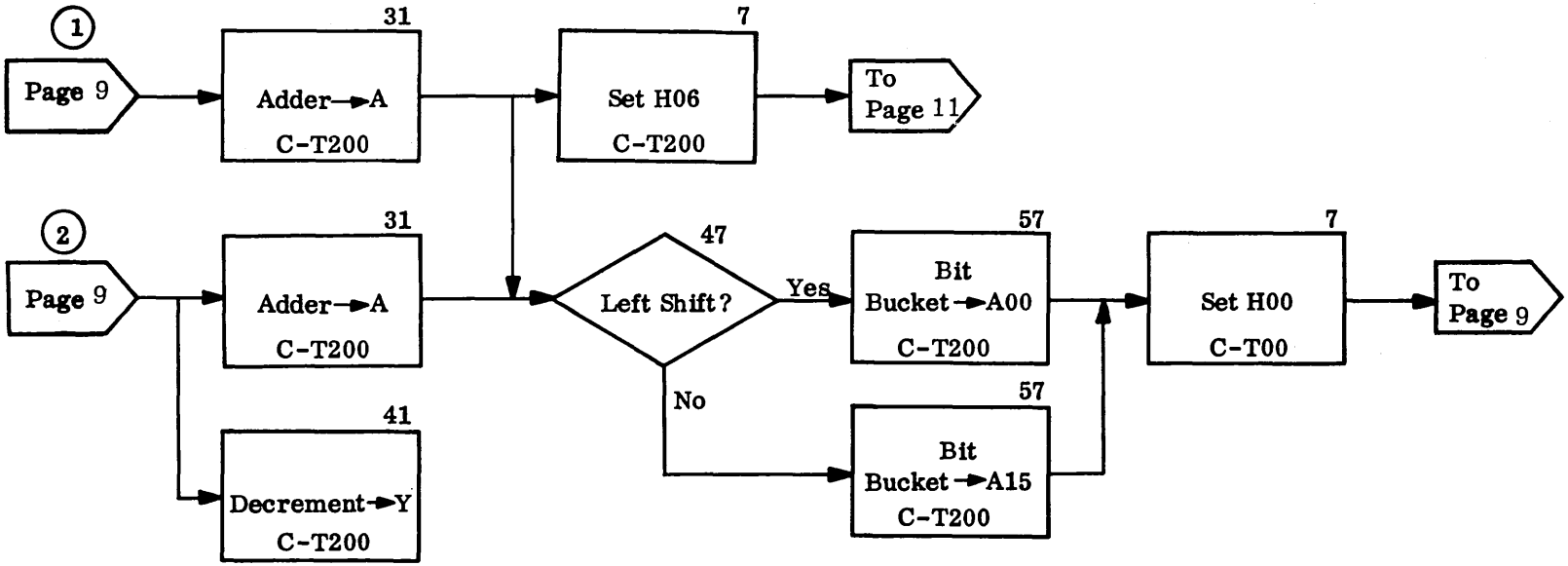
Q SHIFTS

IDENTICAL WITH PAGE 4 OF A SHIFTS BUT WITH Q REGISTER

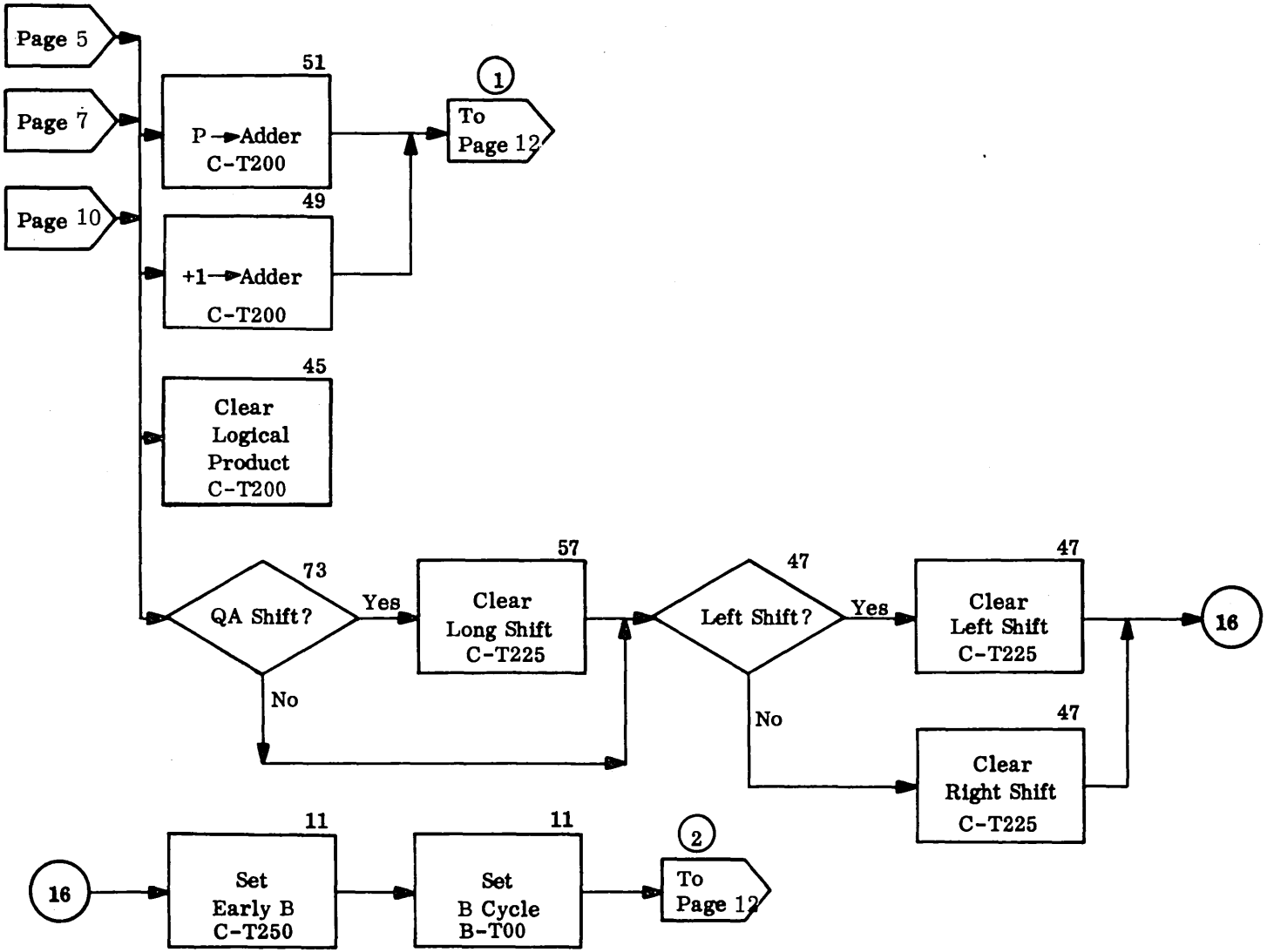
1700 COMPUTER SHIFT OPERATIONS - QA SHIFTS



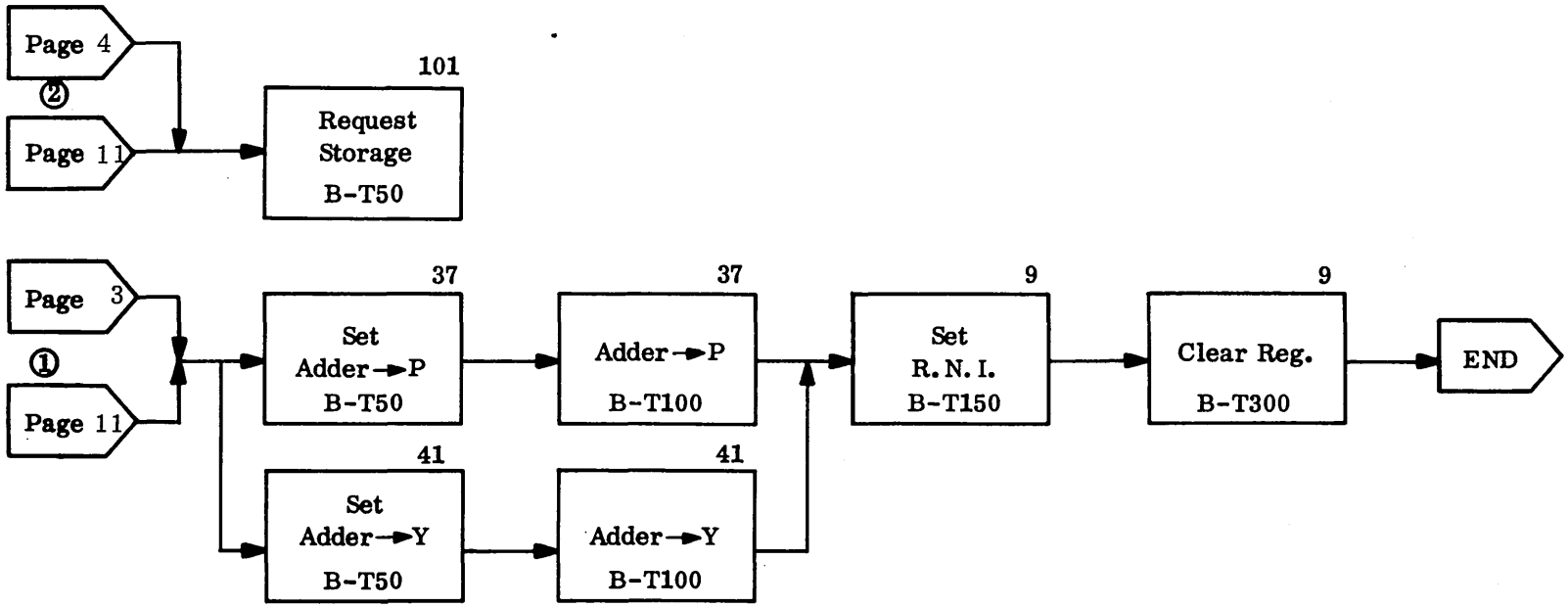
1700 COMPUTER SHIFT OPERATIONS
QA SHIFTS



1700 COMPUTER SHIFT OPERATIONS
ALL SHIFTS



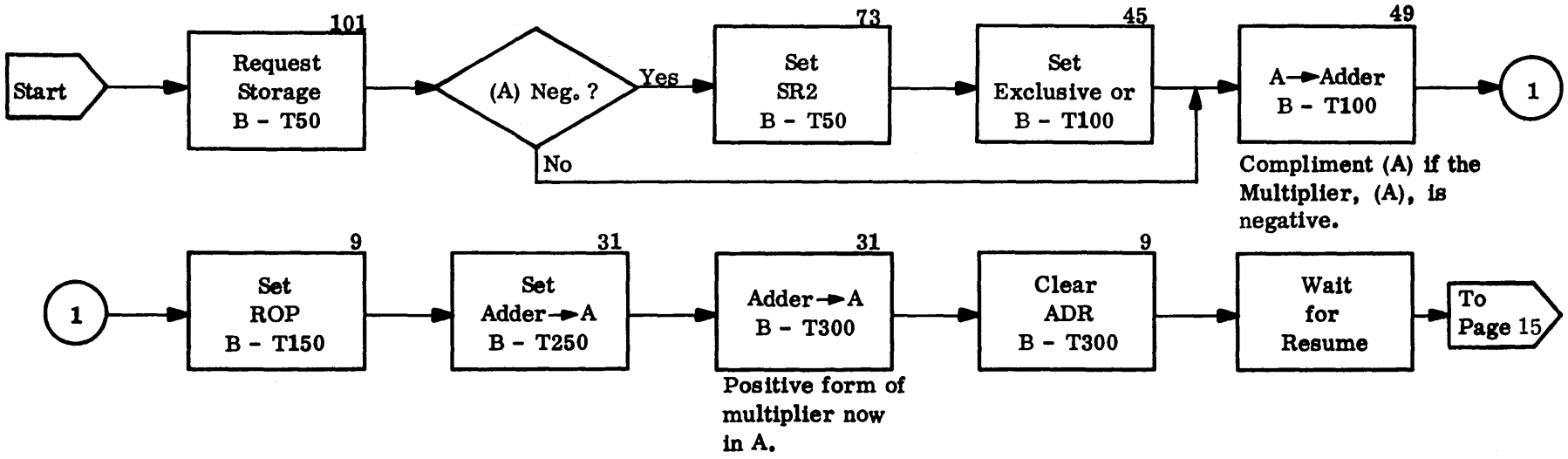
1700 COMPUTER SHIFT OPERATIONS
ALL SHIFTS



1700 MULTIPLY OPERATIONS

1700 COMPUTER MULTIPLY OPERATION

THIS FLOW CHART BEGINS AT T50 OF THE LAST B CYCLE OF ADDRESSING



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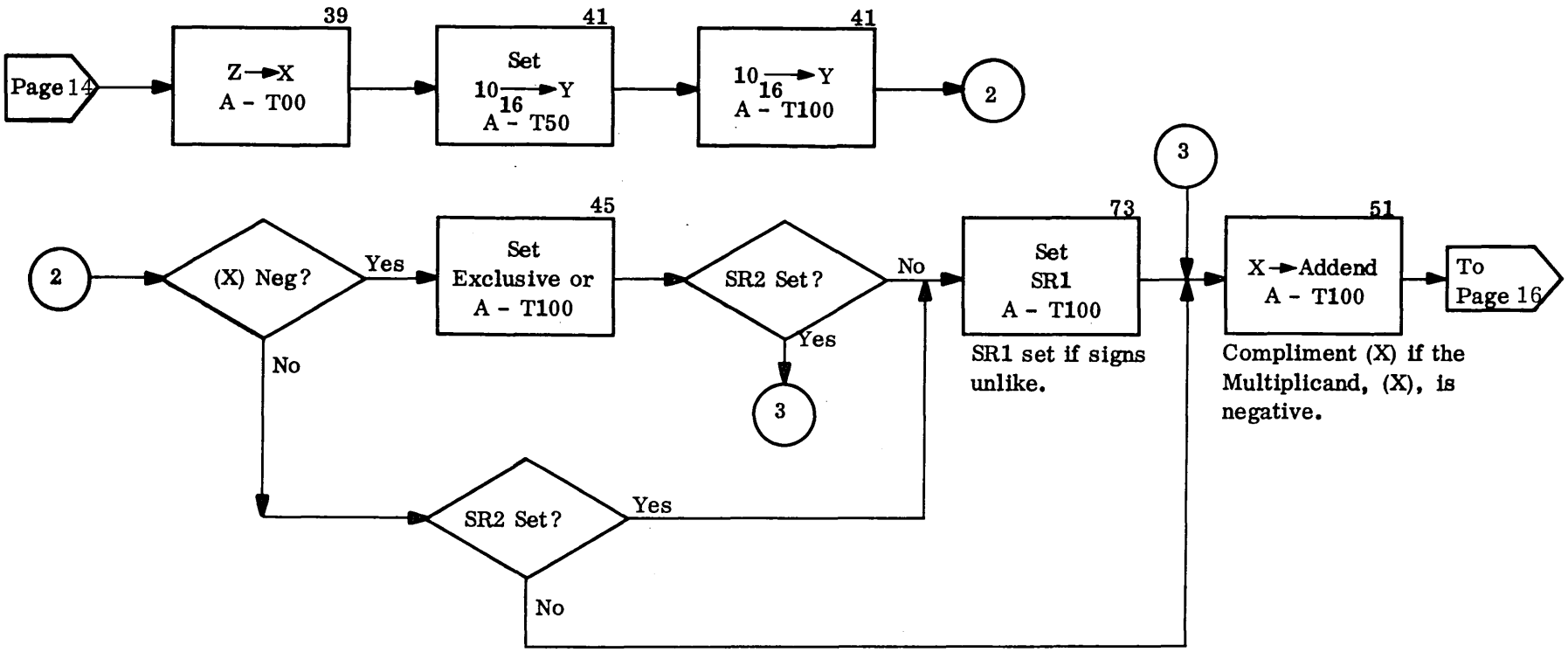

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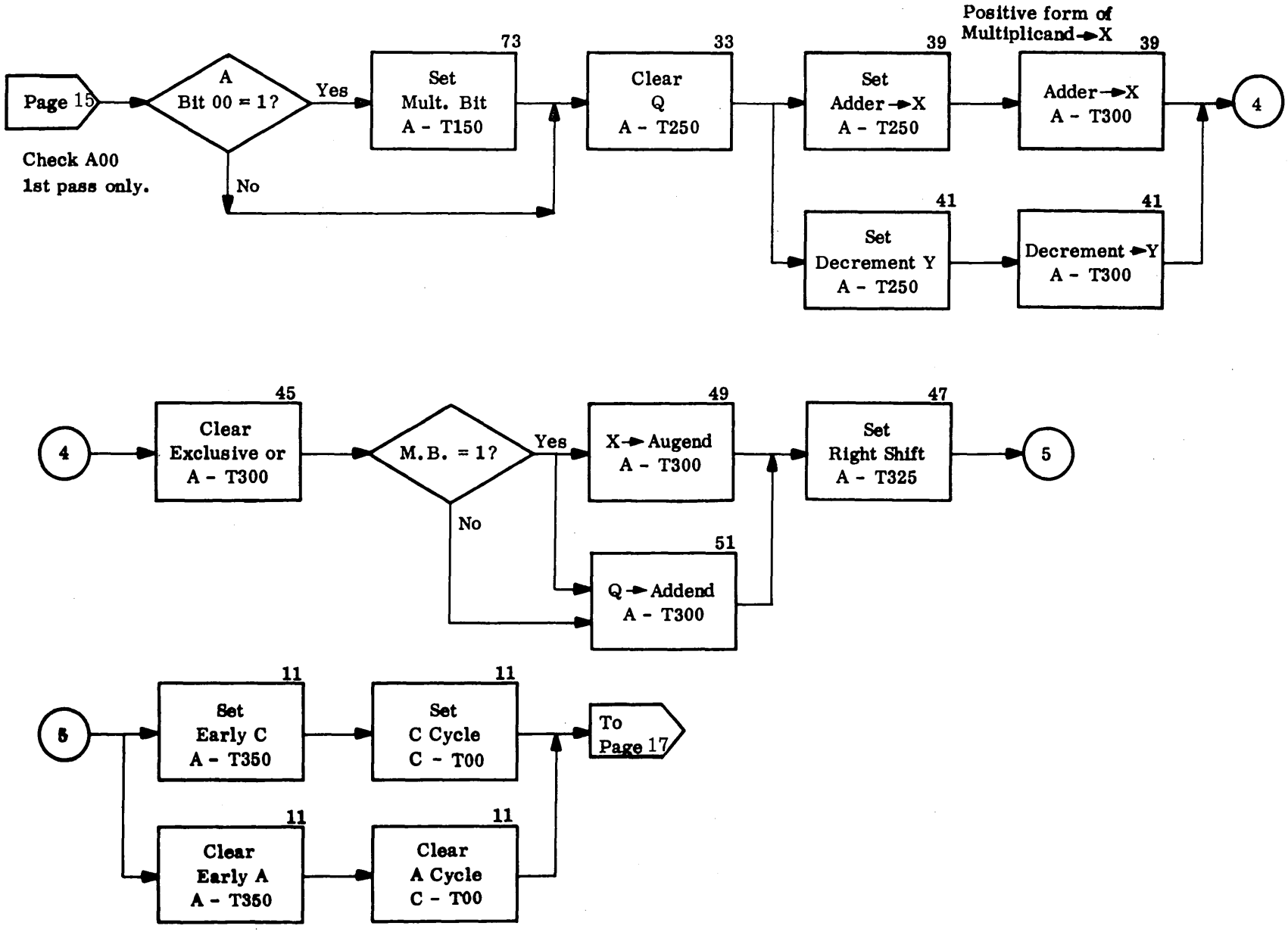

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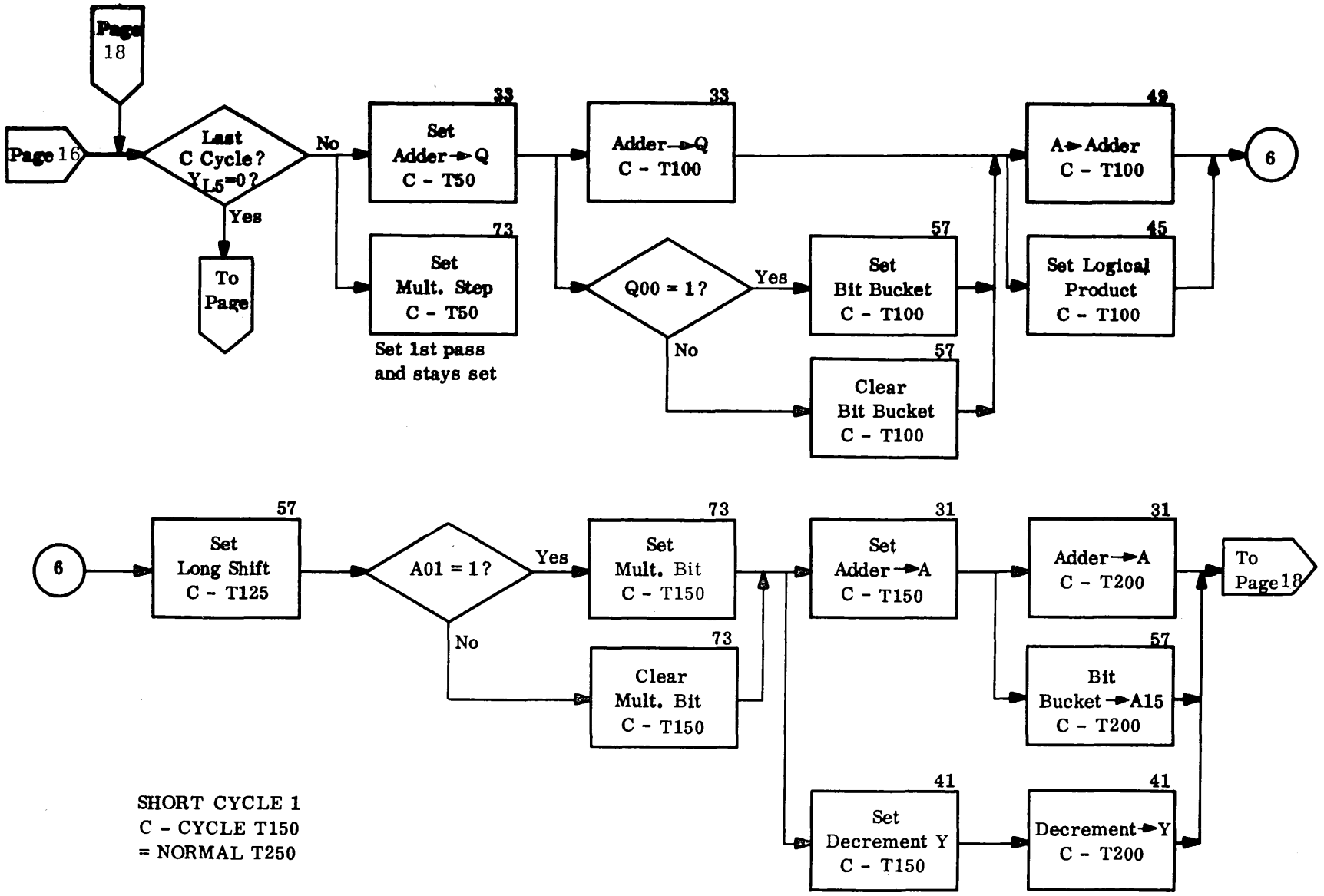

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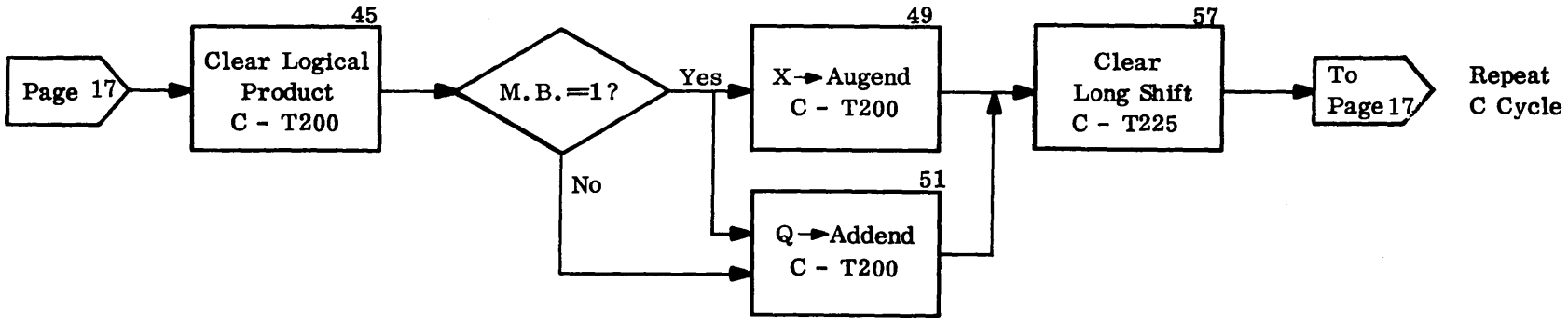

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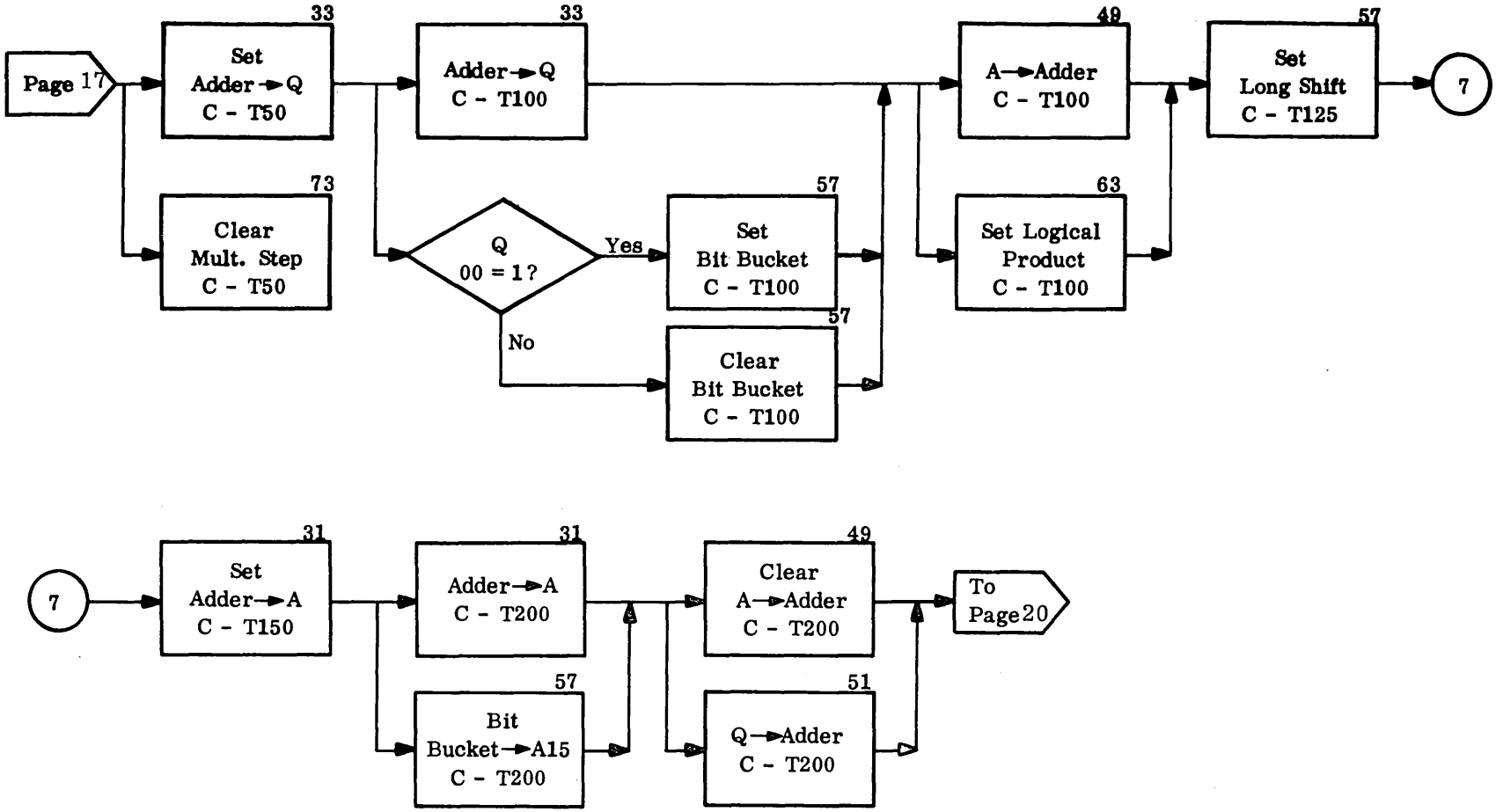
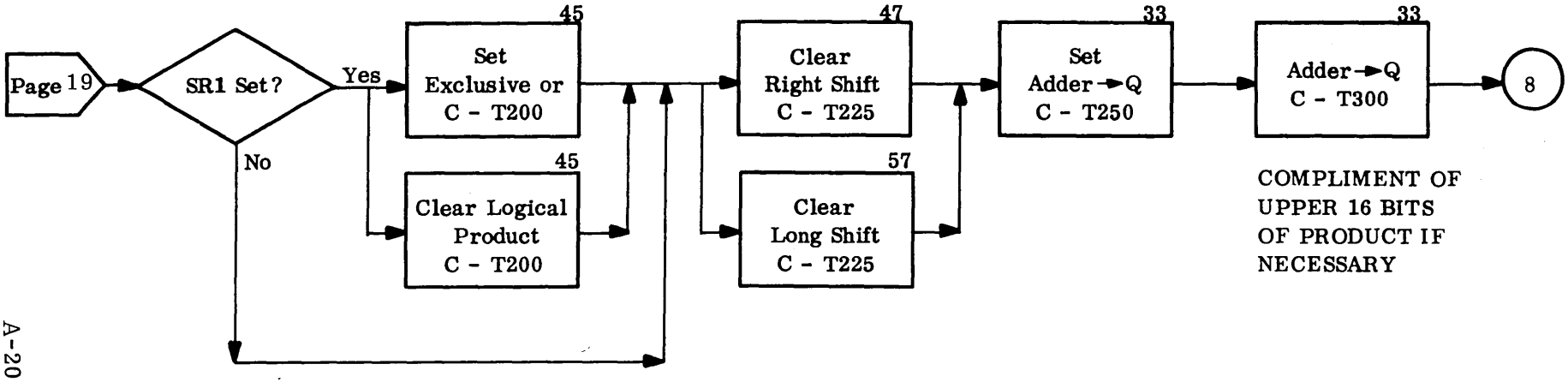
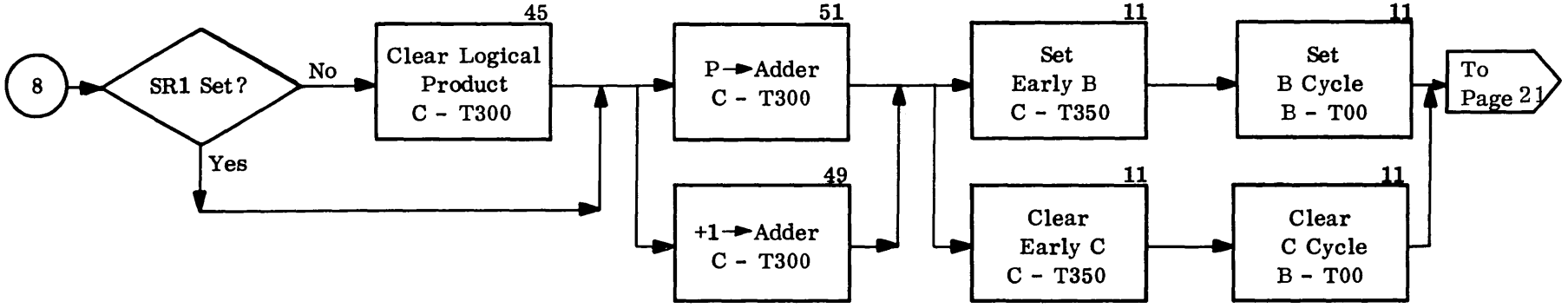


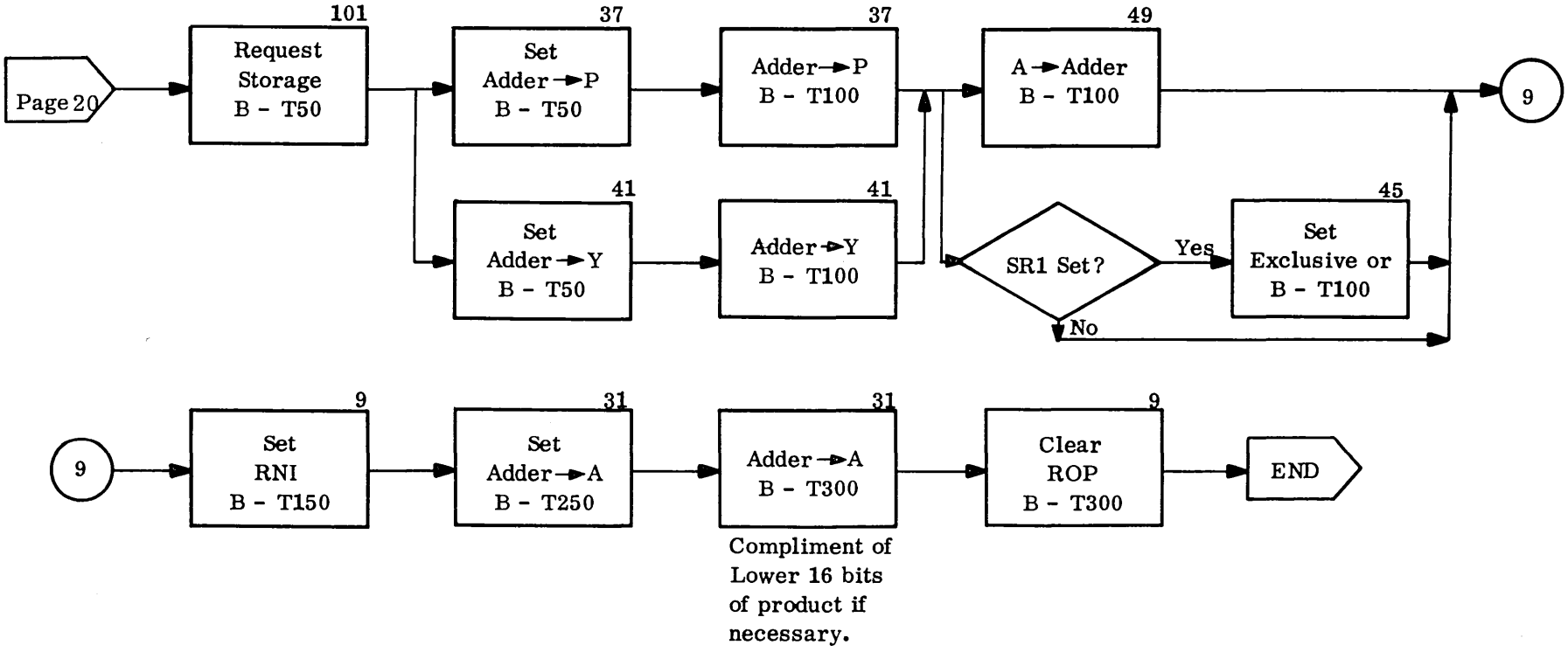
NO SHORT CYCLE
NORMAL TIMING

1700 COMPUTER MULTIPLY OPERATION





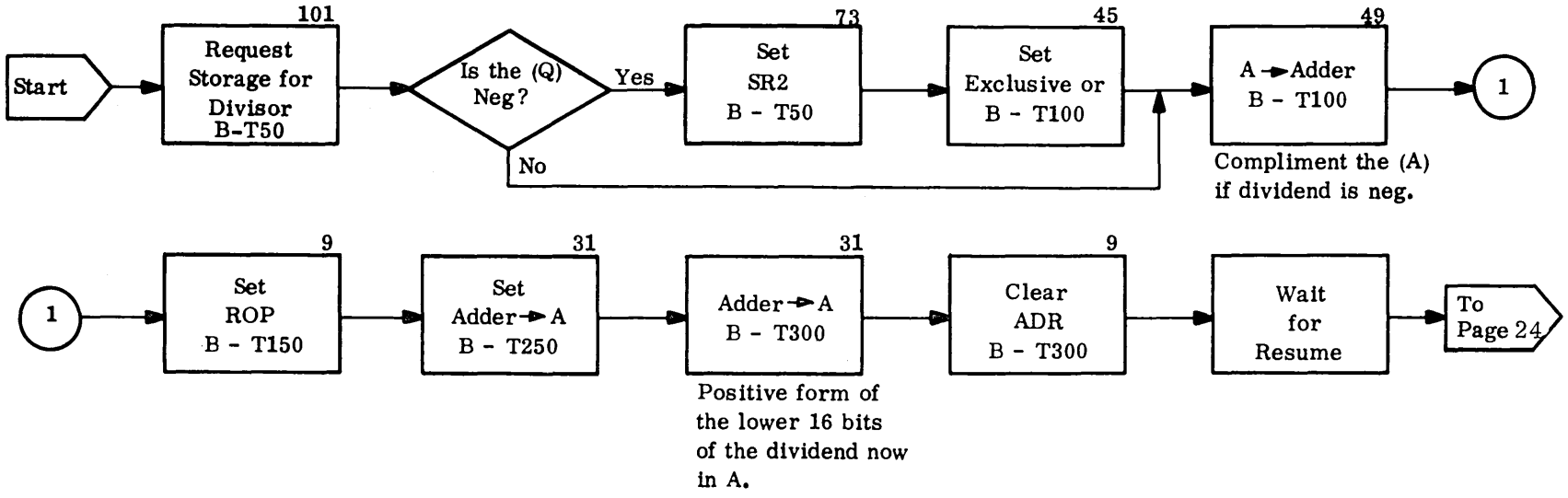
1700 COMPUTER MULTIPLY OPERATION



1700 DIVIDE OPERATION

1700 COMPUTER DIVIDE OPERATION

QA MUST CONTAIN THE DIVIDEND BEFORE EXECUTION OF A DIVIDE INSTRUCTION. THIS FLOWCHART BEGINS AT T50 OF THE LAST B CYCLE OF ADDRESSING.



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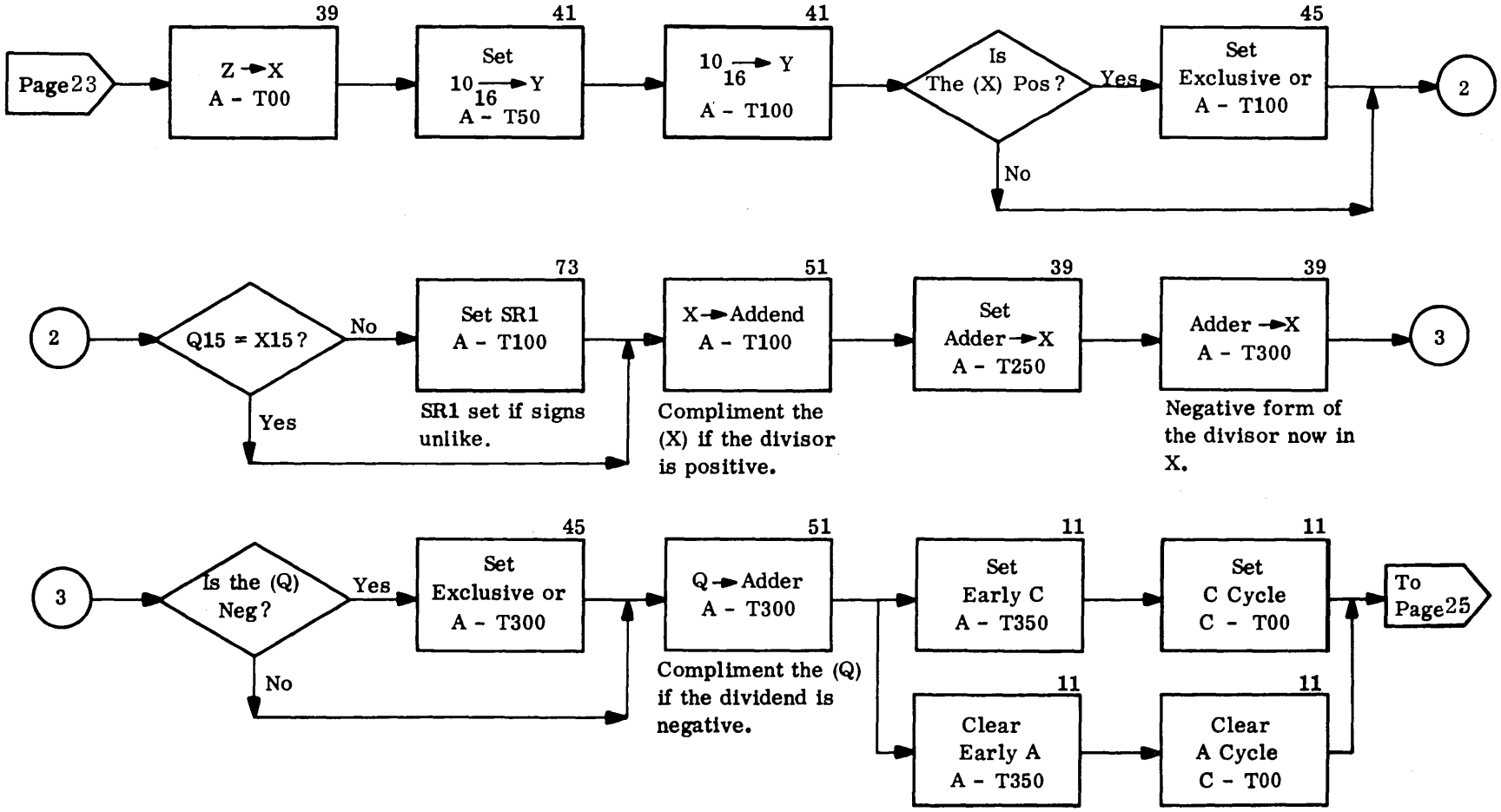

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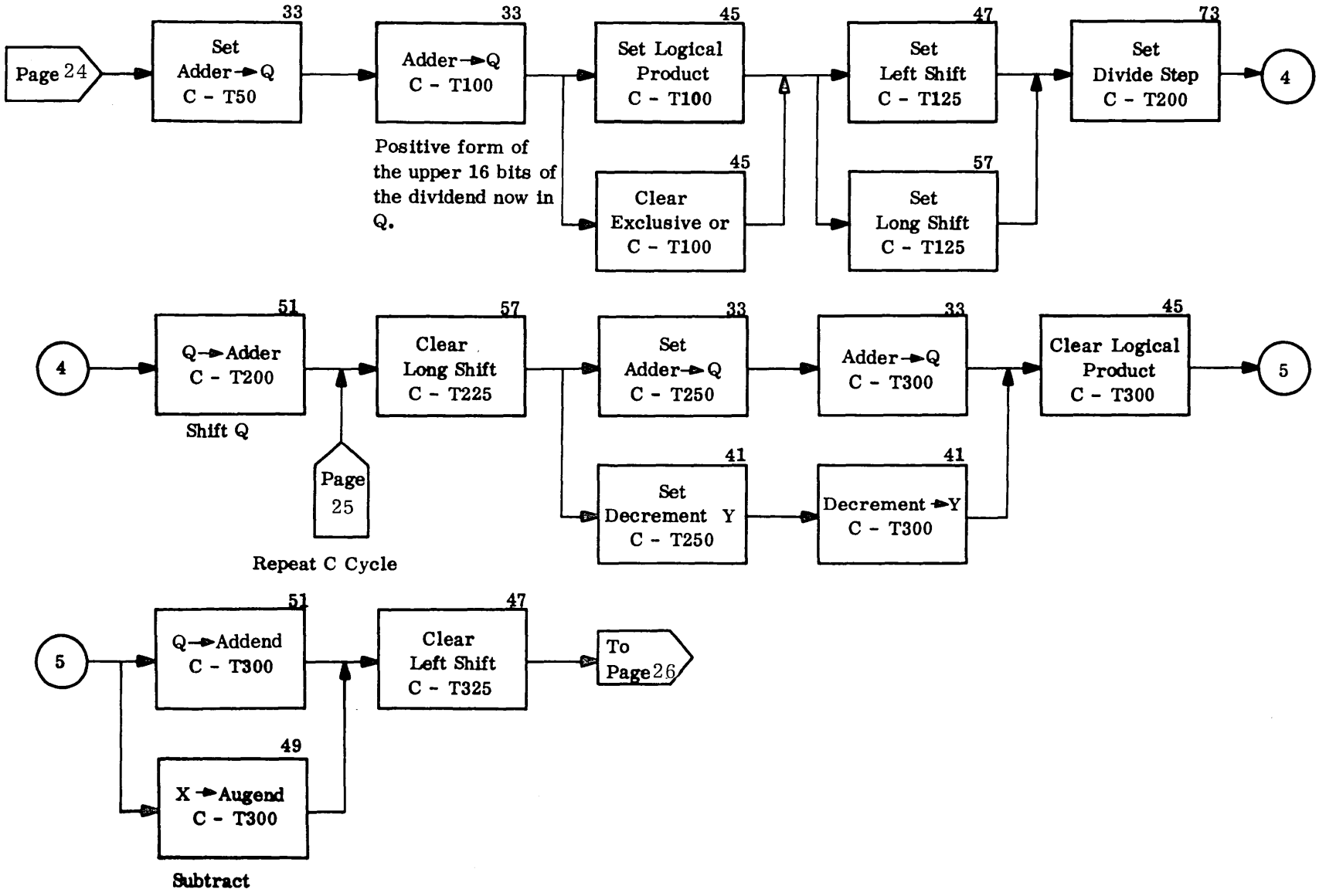

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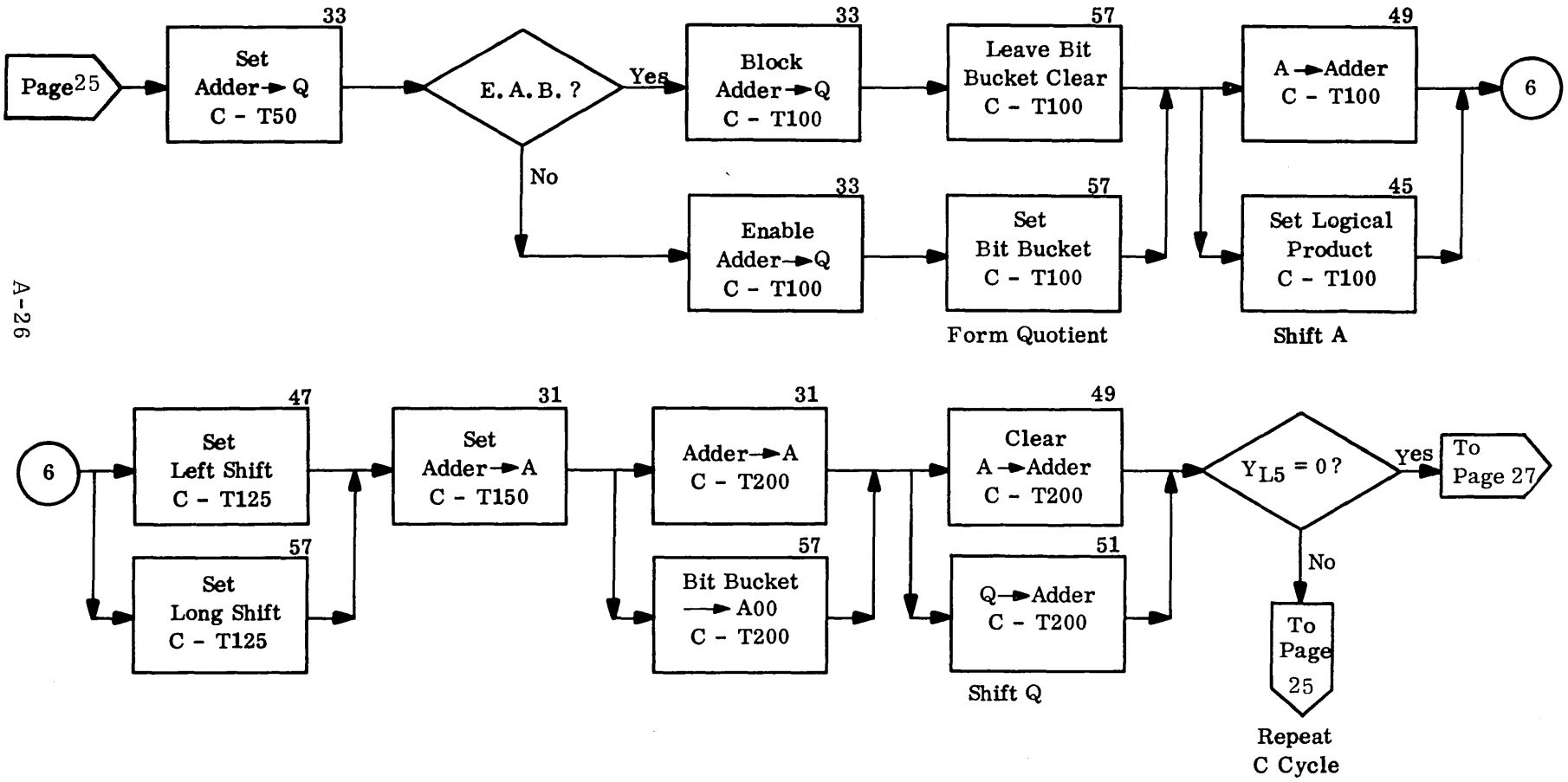

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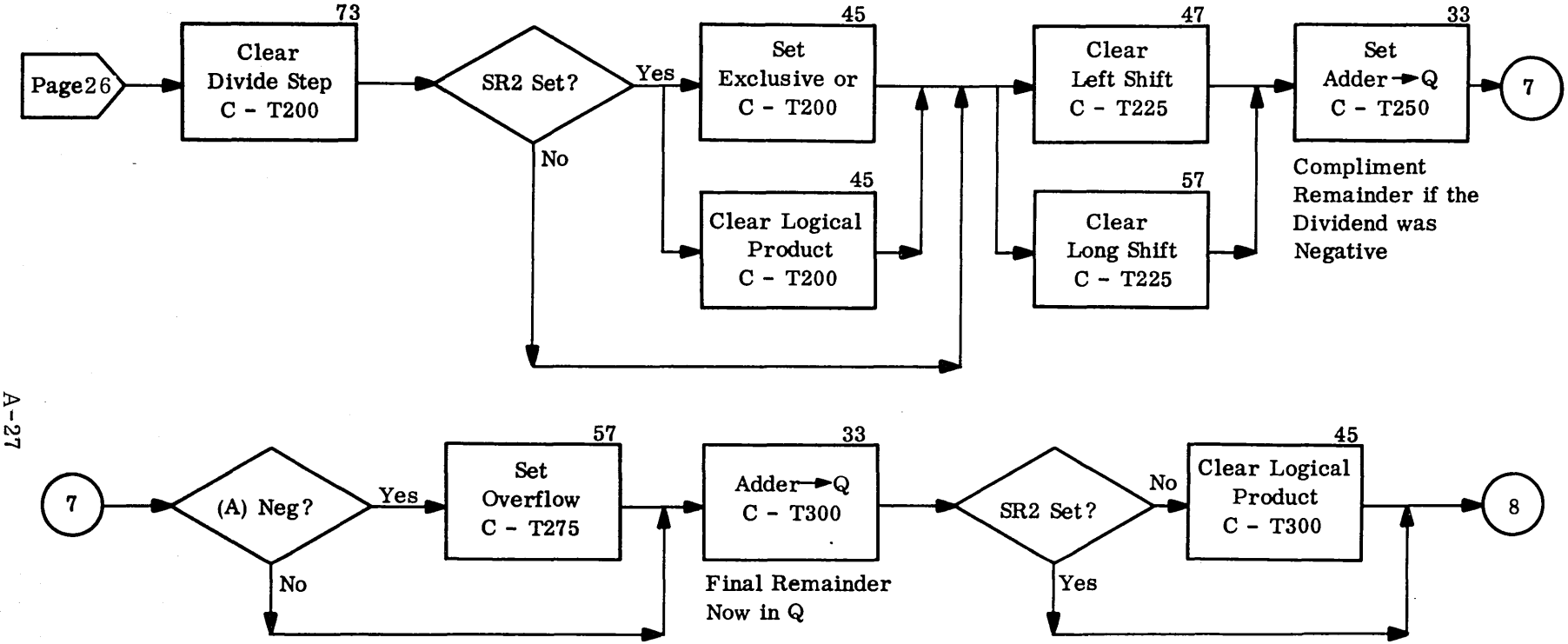

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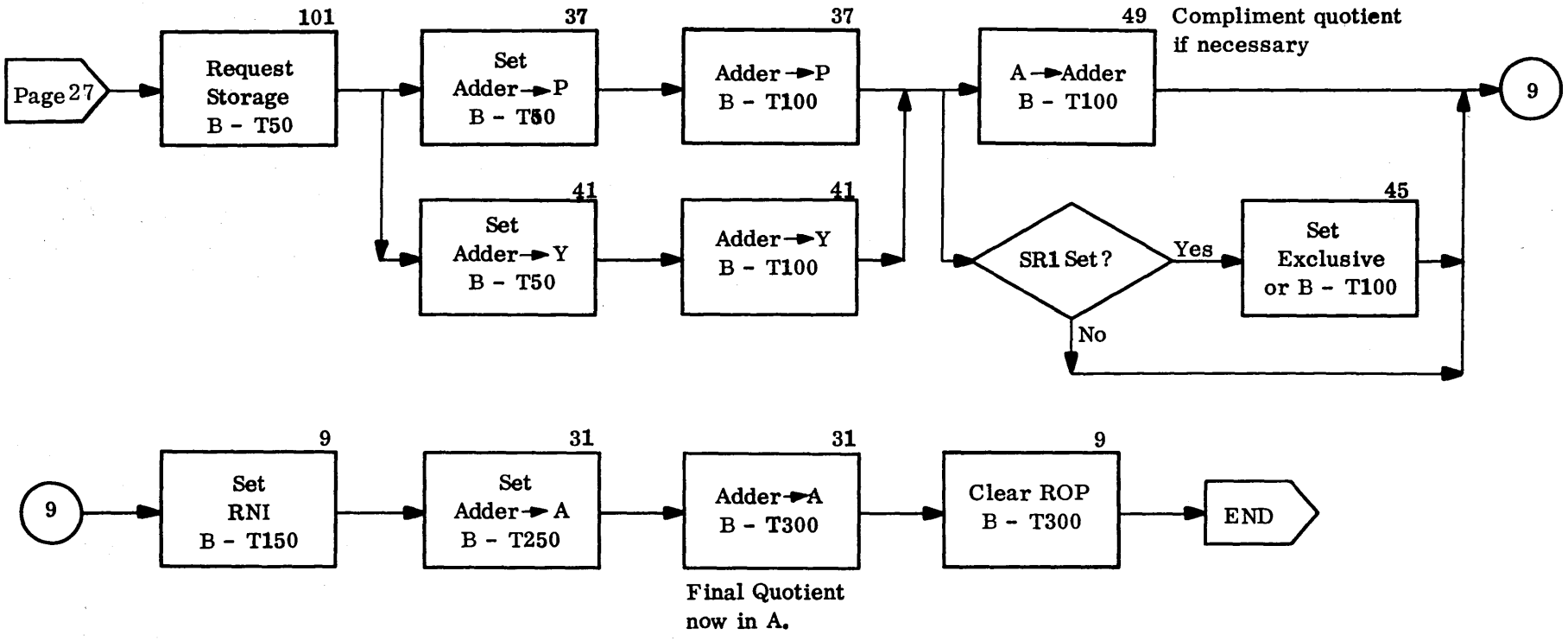

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