Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

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BURROUGHS CORPORATION
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INTRODUCTION AND OPERATION
FUNCTIONAL DETAIL
CIRCUIT DETAIL
ADJUSTMENTS (N/A)
MAINTENANCE PROCEDURES
INSTALLATION PROCEDURES
RELIABILITY IMPROVEMENT NOTICES
OPTIONAL FEATURES (N/A)

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Introduction and Operation

INTRODUCTION

The B0392 magnetic tape cassette I/O control (or device dependent port, DDP), hereinafter called the tape IOC, provides the interface between the A9490-25 magnetic tape cassette and the B700 Processor. The tape IOC provides the necessary control functions for directing tape unit operations and also provides the buffering required for transferring information to and from the tape cassette.

The tape IOC acts upon control words from the B700 Processor, performs the specified operation, and upon completion of the operation, generates a status word containing operating status and/or error information. The Port Select Unit (PSU) controls the synchronization of the tape IOC interface with the B700 Processor.

The tape IOC is contained on four plug-in chip boards which are housed in DDP/IOC locations of the processor cabinet. All operating voltages are derived from the internal power supplies of the processor cabinet.
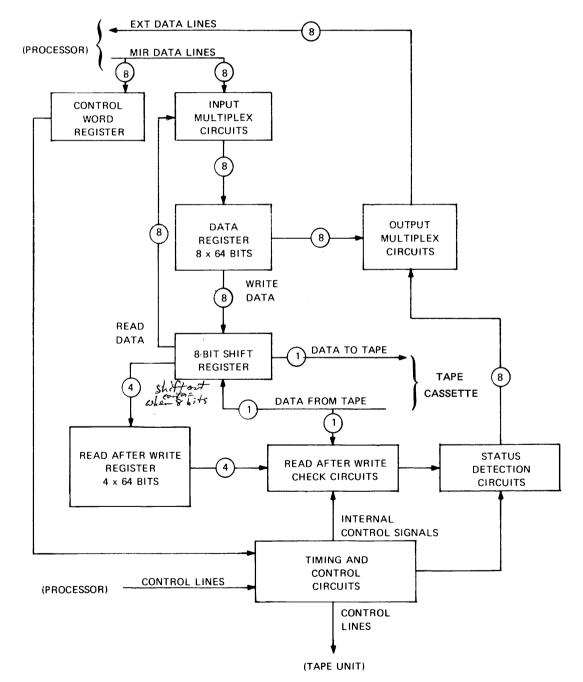

Fig. I-1 FUNCTIONAL BLOCK DIAGRAM OF TAPE IOC

Introduction and Operation

FUNCTIONAL DESCRIPTION OF TAPE IOC

As shown in Figure I-1, the tape IOC consists of the following functional sections:

a. Control Word Register. The control word register is used to store the various control bits of the control word sent to the tape IOC by the processor.

b. Input Multiplex Circuits. These circuits are used to multiplex the MIR data line inputs and the read data outputs into the data register.

c. Data Buffer Register. The data buffer register is an 8x64 bit (64 character) register which functions on the first-in-first-out (FIFO) principle; that is, the first character loaded into the register is the first character transferred out of the register.

d. Output Multiplex Circuits. These circuits are used to multiplex the data register outputs (during read operations) and the status outputs onto the EXT data lines to the processor.

e. Eight-Bit Shift Register. This register is used on both read and write operations to store the tape data. During write operations, tape data is loaded into the shift register from the data register eight bits at a time. The least significant bit of this register constitutes the tape data. Each time a data bit is transferred to the tape unit, the data remaining in the shift register is shifted towards the least significant bit location of the register. During read operations, the tape data is loaded into the shift register one bit at a time and shifted in a like manner. When the shift register is full, the read data is transferred to the output multiplex circuits eight bits at a time.

f. Read After Write Register. This register is a 4x64 (32 character) register used to temporarily store write data as it is read back (read after write check feature) from tape. This register functions on the FIFO principle.

g. Read After Write Check Circuits. These circuits are used to compare the contents of the read after write register (write data) with the data actually written on the tape.

h. Status Detection Circuits. These circuits are used to detect status conditions and generate the applicable status signal input to the output multiplex circuits.

i. Timing and Control Circuits. These circuits produce the various clock and control signals used in the operation of the tape IOC as well as the control signals transferred between the tape IOC and the processor, and the tape IOC and the tape unit.

A9490-25 CHARACTERISTICS

TAPE TRANSPORT

The recording method is non-return to zero (NRZI)

on a single information track with a parallel clock track recorded simultaneously. The normal tape speed is 10 inches per second with a write clock rate of 8 KHz for a recording density of 800 bits per inch. The tape speed in the high-speed mode is 30 inches per second; the rewind speed is 60 inches per second. The start time is 85 milliseconds, minimum. The stop time is 75 milliseconds, minimum. The nominal rewind time for 300 feet is 60 seconds. File protection is provided by removing a write enable plug from the cassette.

TAPE FORMAT

The tape cassette unit uses a tape cartridge which contains approximately 300 feet of tape. This tape is a special tape which contains a clear leader at both ends. At a distance of approximately 40 inches from the clear leader, a small hole has been inserted in the tape signifying the electrical beginning of tape and end of tape. The tape contains two parallel tracks: an information track and a clock track. Data is recorded on the information track serially by bit and by character. Each character is located in a byte of eight bit positions along the track. Data is recorded in the ASCII 7-bit code, and is located in the seven least significant bit positions of the byte. The eighth bit position of the byte (the most significant bit position) always contains a zero bit. (There is no parity bit.) The least significant bit of the character is recorded first.

RECORD FORMAT

The data characters are grouped in blocks which are called records. Each record is separated by a 1-inch record gap. Groups of records are separated by a 7-inch gap in which a tape mark is written. Record sizes can vary from a minimum of one character to a maximum of 256 characters. The sequence of characters within a record corresponds to the normal left-to-right sequence of a written line. In addition to the data characters, a record contains the following control characters:

a. The preamble character, which is recorded immediately preceding the data in each record. The preamble has a code of 10101010. The left-most bit occupies the most significant bit position and is recorded as the last bit of the preamble. When reading data in the forward direction, the first bit of each record is a 0 and the eighth bit is a 1.

b. The Cyclic Redundancy Check (CRC) character, which is recorded immediately following the data portion of every record. It consists of 16 bits and is generated by the polynominal (X-power 16 + X-power 15 + X-power 2+1) from all bits of the corresponding record, excluding the preamble.

c. The postamble character, which is recorded immediately following the CRC character and is identical to the preamble character.

		TYPICAL	TYPICAL	
	POSTAMBLE	CRC	DATA	PREAMBLE
	CHARACTER	CHARACTER	CHARACTER	CHARACTER

INFORMATION TRACK   1 0 1 0 1 0 1 0 1 1 0 1 1 0 1 0 1 0 1 1 1 0 1 1 0 1 0 1 1 1 0 1 1 0 1 0 1 0 1 0

CLOCK TRACK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

TAPE TRAVEL IN
FORWARD DIRECTION

Fig. I-2 FORMAT OF A ONE-CHARACTER RECORD

Figure I-2 illustrates the format of a minimum sized record. This format applies to all records; the only variable is the number of data characters contained in the record.

Tape Mark Record

A tape mark is a record containing a preamble, two null characters, and a postamble. The tape mark record does not contain a CRC.

End of Tape

A properly written tape should always end with a tape mark. A status interrupt is generated when a "Tape Read" operation is requested beyond the end of tape marker. The status returned is BOT, which is interpreted as the physical end of tape. In this case, operator intervention is required to move the tape off the clear leader prior to tape rewind.

A9490-25 TAPE CASSETTE INTERFACE

As shown in Figure I-3, control signals and data are interchanged between the tape IOC and the tape cassette unit. Data is transferred to the tape cassette on interface line TWIL/. The data is transferred one bit at a time, serially. Data is transferred to the tape IOC from the tape cassette unit on interface line TRIP/ in the same one-bit serial method. Interface signals are transferred between the tape IOC and the tape cassette unit as false levels. The tape IOC/ tape cassette interface control signals are as follows:

a.   Clear Leader Position Level (CLPL). When false, CLPL/ indicates that the clear leader portion of the tape is positioned in front of the read/write heads (tape leader at physical beginning of tape).

b.   Tape Position Ready Level (TPRL). When false, TPRL/ indicates that tape is positioned properly (read/write heads are positioned between BOT and EOT) and that the tape cassette can be operated in the write or read mode.

c.   Tape Read Cell Level (TRCL). When false, TRCL/ indicates cell duration time; leading edge defines beginning of cell and trailing edge defines end of cell. The minimum time between cell periods is 1.5 microseconds.

d.   Tape Ready Level (TREL). When false, TREL/ indicates that the tape cassette is ready to accept commands from the tape IOC.

e.   Tape Read Information Pulse (TRIP). When false, TRIP/ indicates that a 1-bit is being read for the cell period defined by signal TRCL/. No pulse during a cell period indicates that a 0 is being read. The minimum pulse width for this signal is 600 nanoseconds.

f.   Tape Write Ready Level (TWRL). When false, TWRL/ indicates that a tape cartridge is properly installed in the tape cassette unit and a write enable tab is installed on the tape cartridge.

g.   Backward Drive Level (BDL). When false, BDL/ causes tape to move in backward direction. Used for backspace operations only.

h.   Busy (BSY). When false, BSY/ indicates that the "clear" leader portion of the tape is not positioned in front of the read/write heads and the tape cartridge should not be removed from the unit.

i.   Forward Drive Level (FDL). When false, FDL/ causes tape to move in the forward direction.

j.   High Speed Level (HSL). When false, HSL/ indicates that tape is in high-speed mode. (Tape moves forward at 30 inches per second when signal FDL/ is false.) When true, HSL/ indicates that tape is in normal speed mode. (Tape moves forward or backward at 10 inches per second when signals FDL/ or BDL/ are false.)

k.   Read Clipping Level (RCL). When false, RCL/ selects high clipping level (used for read-after-write check). Signal is true during normal read operations.

l.   Tape Rewind Pulse (TRWP). When false, TRWP/ initiates a tape rewind operation. The rewind operation ends when it is at beginning of tape ("Clear" leader). Pulse width is 0.015 microseconds.

m.   Tape Write Clock Pulse (TWCP). When false, TWCP/ strobes information from the TWIL/ line to the write amplifier. One clock pulse (0.5 microseconds) is required for each information bit transferred.

n.   Tape Write Information Level (TWIL). When false in conjunction with a tape write clock pulse (TWCP/), TWIL/ indicates a 1-bit of data. When true in con-
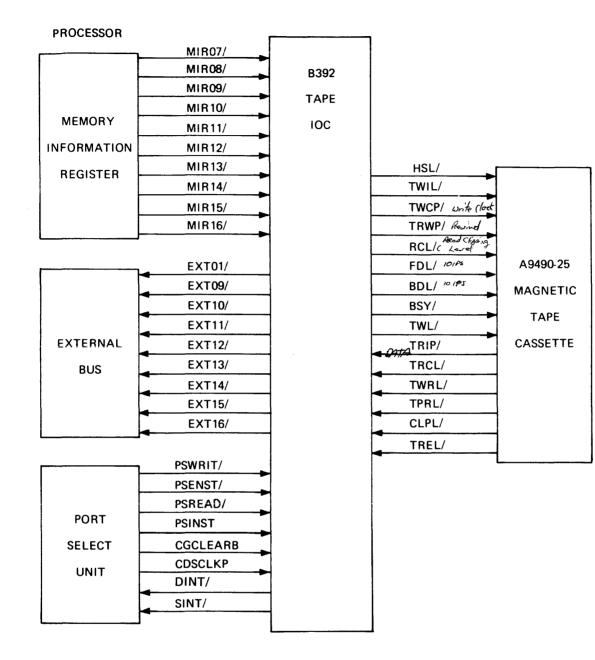
Introduction and Operation

PROCESSOR

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MEMORY         MIR07/
INFORMATION    MIR08/        B392
REGISTER       MIR09/        TAPE
               MIR10/        IOC
               MIR11/
               MIR12/
               MIR13/                    HSL/
               MIR14/                    TWIL/
               MIR15/                    TWCP/ write clock
               MIR16/                    TRWP/ Rewind
                                         RCL/c Read Clipping
                                               Level                A9490-25
               EXT01/                    FDL/ 10 ips
               EXT09/                    BDL/ 10 ips              MAGNETIC
               EXT10/                    BSY/
               EXT11/                    TWL/                        TAPE
EXTERNAL       EXT12/                    TRIP/ Data              CASSETTE
BUS            EXT13/                    TRCL/
               EXT14/                    TWRL/
               EXT15/                    TPRL/
               EXT16/                    CLPL/
                                         TREL/
               PSWRIT/
               PSENST/
               PSREAD/
PORT           PSINST
SELECT         CGCLEARB
UNIT           CDSCLKP
               DINT/
               SINT/
```

Fig. I-3 INTERFACE BLOCK DIAGRAM

junction with a tape write clock pulse, TWIL indicates a 0 bit of data.

o. Tape Write Level (TWL). When false, TWL/ holds drive in write status. This signal must be false before forward drive is initiated, and must remain false until tape motion stops (approximately 50 milliseconds after forward drive level is removed).

B700 PROCESSOR INTERFACE

As shown in Figure I-3, interface communications between the tape IOC and the processor consists of input data lines (MIR07/ through MIR16/), output data lines

(EXT01/ and EXT09/ through EXT16/), and various control signal lines. The tape IOC/processor interface control signals are as follows:

a. Write Line (PSWRIT). When false, PSWRIT/ initiates a one-character data transfer from the processor to the tape IOC for write or erase operations.

b. Read Line (PSREAD). When false, PSREAD/ initiates a one-character data transfer from the tape IOC to the processor for a read operation.

c. Enable Status Line (PSENST). When false, PSENST/ initiates transfer of the status word from the tape IOC to the processor.

Introduction and Operation

d. Instruction Line (PSINST). When false in conjunction with singal PSWRIT/, PSINST/ indicates that the data on the MIR input data lines is a control word. When false in conjunction with signal PSREAD, signal PSINST/ enables transmission of the status word from the IOC to the processor.

e. Clear Line (CGCLEARB). When true, CGCLEARB clears all control flip-flops in tape IOC.

f. Data Interrupt (DINT). When false, DINT/ indicates to the processor that the tape IOC is ready for another data transfer operation.

g. Status Interrupt (SINT). When false, SINT/ indicates that the tape IOC has a status word for the processor. The SINT/ line to the processor is activated by the IOC when one of the following conditions occurs:

    1. Tape reaches the load point (beginning of tape) during a rewind, backspace, or tape mark search reverse operation.
    2. A record gap is detected in any operation.
    3. A 5-millisecond time mark occurs.
    4. Tape cassette unit is not ready and a command is received from the processor.

h. System Clock Pulse (CDSCLK). When true, CDSCLKP indicates a 1-MHz clock pulse.

TAPE IOC/PROCESSOR OPERATIONS

The initiation of an information transfer between the processor and an IOC is controlled by the firmware and is the same for all devices. The distinction is made by the device address contained in the Base Register (BR1 or BR2) of the processor output select gates. The Port Select Unit decodes three bit-groups from the processor to completely define the operation that is to take place. The command field (nanobits 51-54) establishes whether the operation is to be a device read (DR) or a device write (DW). The four least significant bits of BR1 or BR2 contain the specific device address; the most significant bit of BR1/BR2, in conjunction with the command type, determines whether the data transfer is a control word, data word, or status word. (See Figure I-4.)

Control Word

A control word is a 10-bit word which is sent to the tape IOC by the processor to initiate a tape operation. The control word contains various control bits which define the operation to be performed by the tape IOC. The following is a description of the control word bits:

Bit	Function
1-6	Unused
7	Tape Erase; erase the next tape record while moving the tape in the forward direction.
8	Tape Rewind; rewind the tape at 60 inches per second until BOT is sensed.
9	Threshold Select; selects the high threshold read setting. This function must be set during a write operation for the read after write check.
10	High Speed; initiates tape operation in the high-speed mode (30 inches per second). This function is used only for tape mark search.
11	Enable 5 msec. Mark; returns a time mark status to the processor every 5 milliseconds.
12	Enable Data Interrupts; enables data interrupts to the processor when ready to receive or transmit a character.
13	Write Inhibit; sets the file protect status bit during tape rewind. This bit will be reset when the cassette drive door is opened.
14	Tape Write; writes the next record while moving the tape in the forward direction.
15	Tape Read; reads the next record while moving the tape in the forward direction.
16	Backspace; initiates a backspace operaton to the previous record gap.

	MSB															LSB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
CONTROL WORD	–	–	–	–	–	–	TAPE ERASE	TAPE REWIND	THRESH SELECT	HIGH SPEED	ENABLE 5 MSEC MARK	ENABLE DATA INTER	WRITE INHIBIT	TAPE WRITE	TAPE READ	BACK SPACE
DATA WORD	–	–	–	–	–	–	–	–	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
STATUS WORD	DATA REQ	–	–	DEV ADDR 4	DEV ADDR 3	DEV ADDR 2	DEV ADDR 1	DEV ADDR 0	5 MSEC TIME MARK	SERV TOO LATE	RECORD GAP	BEGIN OF TAPE	END OF TAPE	FILE PROT	TAPE ERROR	DEVICE NOT READY

NOTE: DEVICE ADDRESS BITS OF STATUS WORD ARE INSERTED AT PSU.

Fig. I-4 INTERFACE WORD FORMATS

Data Word

Data words are eight-bit words which are transferred between the tape IOC and the processor on eight of the 16 parallel data lines which interface the tape IOC with the processor. The data words are transferred on lines 9 through 16; bit 16 is the least significant bit.

Status Word

The status word is sent to the processor by the tape IOC in order to notify the processor that a failure or a specific functional condition has occurred. The status word consists of a device status field (bits 9 through 16) and a data request bit (bit 1). Before the status word is sent to the processor, the Port Select Unit (PSU) inserts a device address field (bits 4 through 8). The following is a description of the status word format:

Bit	Condition Indicated
1	Data Request; IOC is ready to receive or transmit the next character. This status condition follows the Data Interrupt (DINT/) signal to the processor.
2,3	Unused.
4-8	Device Address; IOC address inserted at the PSU.
9	5 msec. Time Mark; returned to processor every 5 milliseconds in response to a control word with this bit set.
10	Service Too Late; the firmware failed to service the IOC data buffer within a given time interval.
11	Record Gap; the IOC detected a record gap indicating end of data.
12	Beginning of Tape; the tape transport sensed a BOT,. signifying that the tape is at load point.
13	End of Tape; the tape transport sensed an EOT while the tape was moving in a forward direction. This status is reset upon issuance of a rewind command.
14	File Protect; rewind inhibit or the write inhibit tab is in inhibit position.
15	Tape Error; the IOC detected a read after write error during a write operation.
16	Device Not Ready; the tape transport is not ready to accept an external command.

Tape Write Operation

The firmware performs the following functions to execute a tape write operation in the forward direction:

a. Transfers a control word with the "Tape Write", "Enable 5 msec. Mark" and "Threshold Select" bit set.

b. Counts 5 msec time marks for 100 milliseconds and then transfers a control word with the "Enable 5 msec Mark" reset and the "Enable Data Interrupt" bit set. (If the write is from BOT, 140 milliseconds is used in place of 100 milliseconds.)

c. Transfers a character to the tape IOC for each data interrupt received, for a total of one preamble character, up to 256 data characters, two CRC characters, and one postamble character.

d. When the character count reaches zero at the postamble character, waits 45 milliseconds and then transfers a control word with the "Enable Data Interrupt" bit reset. The "Enable Data Interrupt" bit reset command notifies the tape IOC that the previous character is the last character of the record.

e. Upon receipt of a "Record Gap" status interrupt, transfers a control word with the "Enable 5 msec Mark" bit set.

f. If the next S-level instruction is a "Tape Write", counts 5 msec time marks for 25 milliseconds and returns to step a. Otherwise, counts 5 msec time marks for 55 milliseconds and then transfers a control word with the "Tape Write" and the "Threshold Select" bits reset.

g. Counts 5 msec time marks for 75 milliseconds and then transfers a control word with "Enable 5 msec Mark" bit reset. The firmware may then initiate the next tape operation.

Write Tape Mark Operation

In this operation, the firmware performs the same functions as in the "Tape Write" operation except that in step b, 350 milliseconds is used in place of 100 milliseconds; in step c the data transfer consists of one preamble character, 16 bits of zero's, and one postamble character; and in step f use 350 milliseconds in place of 55 milliseconds. There is no CRC in the tape mark record.

Tape Erase Operation

The firmware performs the same functions for this operation as in the "Tape Write" operation except that in step a, the "Tape Erase" bit is set in place of the "Tape Write" bit and in step c the data transfer consists of null characters.

Introduction and Operation

Tape Read Operation

The firmware performs the following functions to execute a "Tape Read" operation in the forward direction:

a. Transfers a control word with the "Tape Read" and "Enable Data Interrupt" bits set.

b. Reads a character for each data interrupt (DINT/) received from the tape IOC, for a total of one preamble character, up to 256 data characters, two CRC characters, and one postamble character.

c. Upon receipt of a "Record Gap" status interrupt (specifies that the previous character is the last character of the record) if the next S-level instruction is a "Tape Read", returns to step a. Otherwise, transfers a control word with the "Enable 5 msec Mark" bit set and "Enable Data Interrupt" bit reset.

d. Counts 5 msec time marks for 45 milliseconds and then transfers a control word with the "Tape Read" bit reset.

e. Counts 5 msec time marks for 75 milliseconds and then transfers a control word with the "Enable 5 msec Mark" bit reset. The firmware may then initiate the next tape operation.

Backspace Operation

The firmware performs the following functions to execute a backspace operation:

a. Transfers a control word with "Backspace" bit set.

b. Upon receipt of a "Record Gap" status condition, (specifies that the record gap of the previous record has been reached) if the next S-level instruction is a "Backspace," returns to step a. Otherwise, transfers a control word with the "Enable 5 msec Mark" bit set.

c. Counts 5 msec time marks for 55 milliseconds and then transfers a control word with the "Backspace" bit reset.

d. Counts 5 msec time marks for 75 milliseconds and then transfers a control word with the "Enable 5 msec Mark" bit reset. The firmware may then initiate the next tape operation.

Rewind Operation

The firmware performs the following functions to execute a "Tape Rewind" operation:

a. Transfers a control word with the "Tape Rewind" bit set.

b. Upon receipt of a BOT status condition from the IOC (specifies that the tape is at load point but requires an additional 200 milliseconds to stop) transfers a control word with the "Enable 5 msec Mark" bit set.

c. Counts 5 msec time marks for 200 milliseconds and then transfers a control word with the "Enable 5 msec Mark" bit reset. The firmware may then initiate the next tape operation.

Tape Mark Search Forward Operation

The firmware performs the following functions to search for a tape mark in the forward direction:

a. Transfers a control word with the "Tape Read," "High Speed," and the "Enable Data Interrupt" bits set.

b. Transfers a control word with the "Enable Data Interrupt" bit reset upon receipt of the first one to four characters followed by a "Record Gap" status interrupt or upon the receipt of a fifth character. Receipt of three or four characters followed by a record gap indicates a tape mark. Receipt of less than three characters or more than four characters indicates that the record is not a tape mark.

c. If additional records are to be searched for a tape mark, then upon receipt of the "Record Gap" status interrupt (if not already received) return to step a. Otherwise transfer a control word with the "Enable 5 msec Mark" bit set.

d. Count 5 msec time marks for 25 milliseconds and then transfer a control word with the "Tape Read" and "High Speed" bits reset.

e. Counts 5 msec time marks for 200 milliseconds and then transfers a control word with the "Enable 5 msec Mark" bit reset. The firmware may then initiate the next tape operation.

Tape Mark Search Reverse Operation

This function is performed as in "Tape Mark Search Forward" operation except that in step a the "Backspace" bit in the control word is also set, and in step e the "Backspace" bit is also reset.

DISK MULTI-RECORD LOCKOUT

The firmware ensures that disk data streams are not attempted during a tape data transfer operation. This function is accomplished by treating the tape unit as a character device, which automatically causes a delay in starting a disk data stream operation until the present operation of each active character device has been completed and by prohibiting the start of a new character device operation until the disk data stream operation has been completed.

Introduction and Operation

GLOSSARY OF TERMS AND SYMBOLS

The following list defines the terms (signal mnemonics) used in the tape IOC. Also given are the sheet numbers of the FT&R logic diagrams on which the terms originate.

Name	Logic Diagram	Definition
BACKSP	SH.T.041	Backspace Instruction
BDL	SH.T.033	Backward Drive Level
(TC)BIR	SH.T.032	Buffer Input Ready
(TC)BNWRIT	SH.T.042	Not BOT, Write Operation
(TC)BOR	SH.T.021	Buffer Output Ready
(TC)BOT	SH.T.042	Beginning of Tape
BRESET	SH.T.012	Buffer Reset
BSIN	SH.T.021	Buffer Shift In
BSOUT	SH.T.021	Buffer Shift Out
BSY	SH.T.033	Busy
(TC)B0-B7	SH.T.022	Buffer Register Data
CLPL	SH.T.033	Clear Leader Position
CLR	SH.T.012	Clear
CNT4	SH.T.013	Bit Count of 4
DATA	SH.T.012	Tape Read Data
DINT	SH.T.032	Data Interrupt
(TC)DNR	SH.T.042	Device Not Ready
DREF	SH.T.012	Data Reference Bit
ENDI	SH.T.041	Enable Data Interrupt
ENEXT	SH.T.021	Enable External Bus
ENWSTR	SH.T.032	Enable Write Strobe
EN5MS	SH.T.041	Enable 5 Millisecond Mark
EOT	SH.T.042	End of Tape
ERASE	SH.T.041	Erase Instruction
EXT01	SH.T.032	External Bus Data Line 1
EXT9-EXT16	SH.T.022	External Bus
FDL	SH.T.042	Forward Drive Level
(TC)GAP	SH.T.032	Record Gap
(TC)HSL	SH.T.021	High Speed Level
IB0-IB7	SH.T.021	Input Data Bits
(TC)LDBUF	SH.T.013	Load Buffer
(LU)MIR07-(LU)MIR16	SH.T.021	Processor Memory Information Register Bits
NEWFP	SH.T.021	New File Protect

Name	Logic Diagram	Definition
(TC)PE	SH.T.013	Parallel Enable
(TC)PENST	SH.T.011	Processor Enable Status
(TC)PINST	SH.T.011	Processor Instruction Enable
(TC)PREAD	SH.T.011	Process Read Enable
(TC)PWRITE	SH.T.011	Processor Write Enable
RCL	SH.T.041	Read Clipping Level
RDBKS	SH.T.032	Read Backspace
RDSTAT	SH.T.041	Read Status
(TC)RDSTRB	SH.T.012	Read Strobe
(TC)READ	SH.T.041	Read Instruction
ROP	SH.T.041	Read Operation
RRDS	SH.T.032	Read Data Strobe
RWND	SH.T.04	Rewind Instruction
(CD)SCLKPr	SH.T.031	System Clock
SELSAT	SH.T.021	Select Status
SHIFT	SH.T.011	Shift Time
SINT	SH.T.042	Status Interrupt
(TC)STL	SH.T.042	Processor Service Too Late
(TC)TE	SH.T.012	Tape Error
TPRL	SH.T.033	Tape Position Ready Level
TRCL	SH.T.012	Tape Read Cell Level
TREL	SH.T.033	Tape Ready Level
TRIP	SH.T.012	Tape Read Information Pulse
TRWP	SH.T.041	Tape Rewind Pulse
TWCP	SH.T.013	Tape Write Clock Pulse
TWIL	SH.T.011	Tape Write Information Lead
TWL	SH.T.041	Tape Write Level
TWRL	SH.T.021	Tape Write Ready Level
(TC)T0-T7	SH.T.011	Tape Data
WINST	SH.T.041	Write Instruction
WOP	SH.T.031	Write Operation
Write	SH.T.041	Write
(TC)WSTR	SH.T.031	Write Strobe
(TC)1STPE	SH.T.032	1st Parallel Enable
5M	SH.T.031	5 Millisecond Clock
(TC)5MS	SH.T.042	5 Millisecond Strobe
256	SH.T.031	False Start Time
4096	SH.T.031	Record Gap Time

Functional Detail

CIRCUIT DESCRIPTIONS

Functionally, the tape IOC is divided into three circuit sections: data control, status control, and timing control. The data control circuits decode the signals received from the processor and provide the necessary control signals for the operation of the tape cassette unit. The status control circuits monitor the tape operations and detect the various status conditions that occur. The timing control circuits provide the control signals used in the operation of the data control and status control circuits.

DATA CONTROL

The data control circuits are shown in Figure II-1 and consist of the following:

a.   Read Strobe Generator. The read strobe generator (logic diagram sheet T.012) detects the occurrence of the tape read clock to produce a DATA signal and a
•   read strobe (RDSTRB) signal.

b.   Shift Register Control. The shift register control logic (logic diagram sheet T.011) detects the occurrence of a write strobe signal for tape write operations or the read strobe signal for read operations to produce the SHIFT signal used to shift data in the shift register and to count up the shift counter.

c.   Shift Register. The shift register (logic diagram sheet T.011) is an eight-bit register used to store the data character to be written on or read from tape. During tape write operations, all eight bits of the data character (B0-B7) are entered simultaneously by the parallel enable (PE) input and are shifted out one bit at a time, starting with the least significant bit (TO), to the tape unit. During read operations, data is entered into the shift register one bit at a time into the most significant bit location and shifted to the least significant bit location. When the register is full, all eight bits of the data character (TO-T7 are shifted out simultaneously.
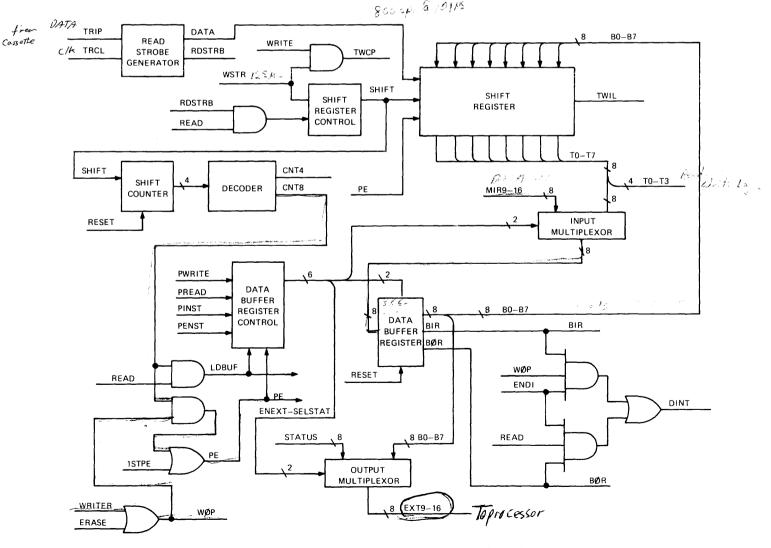

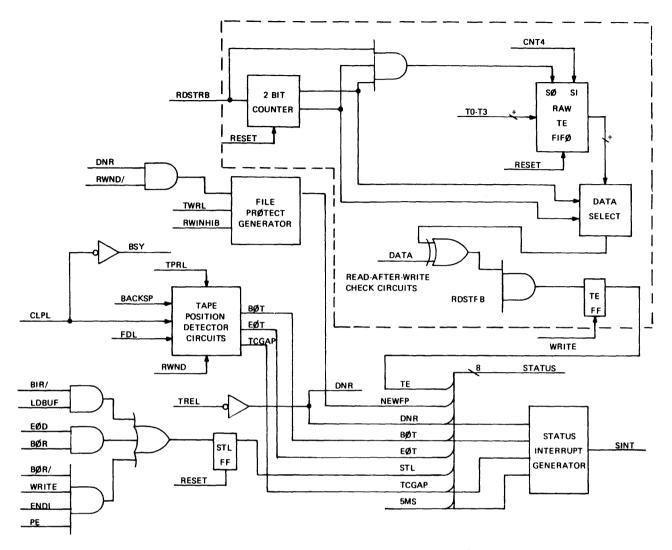
Fig. II-1 DATA CONTROL BLOCK DIAGRAM

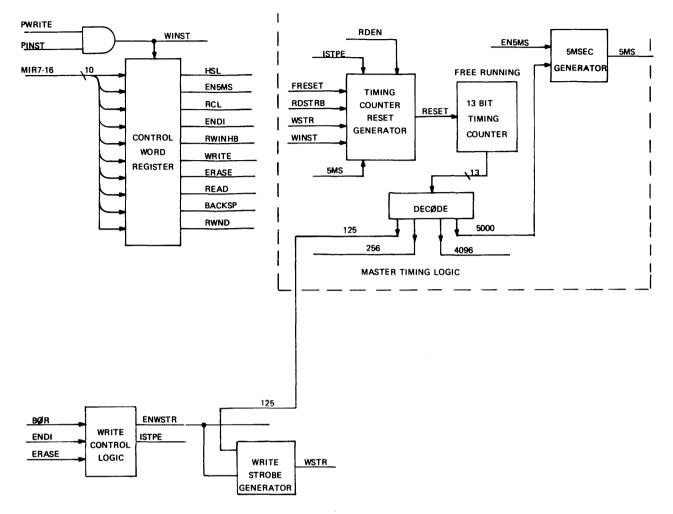Functional Detail

Fig. II-2 STATUS CONTROL BLOCK DIAGRAM

d. Shift Counter. The shift counter (logic diagram sheet T.013) consists of an eight-bit counter and decode circuits. The counter is incremented by signal SHIFT. Counts of 0 and 4 are decoded for use in the read-after-write circuitry, and a count of 8 is decoded to generate the load buffer (TCLDBUF) signal to load the data buffer register and the parallel enable (PE) signal to load the shift register.

e. Data Buffer Register Control. These circuits (logic diagram sheet T.021) are used to produce the control signals used to load data into and out of the data buffer register, the input multiplexer, and the output multiplexer.

f. Data Buffer Register. The data buffer register (logic diagram sheet T.022) is a 64-character (8x64) register used to store data characters awaiting transfer to the tape unit (write operation) or processor (read operation). The data buffer register consists of two FIFO (first-in first-out) chips. Refer to Section III for a description of the FIFO chip.

g. Input Multiplexer. The input multiplexer (logic diagram sheet T.021) multiplexes the data input lines (MIR09-MIR16) from the processor with the shift register output lines for input to the data buffer register.

h. Output Multiplexer. The output multiplexer (logic diagram sheet T.022) multiplexes the data buffer register output lines (B0-B7) with the status lines for output to the processor.

STATUS CONTROL

The status control circuits are shown in Figure II-2 and consist of the following:

a. Tape Position Detector Circuits. These circuits (logic diagram sheets T.032 and T.042) detect the beginning of tape (BOT), end of tape (EOT), and record gap (TCGAP) status conditions.

Functional Detail

Fig. II-3 TIMING CONTROL BLOCK DIAGRAM

b. File Protect Generator. The file protect generator (logic diagram sheet T.021) produces the file protect status signal (NEWFP) upon receipt of a "tape write inhibit" control bit from the processor or upon receipt of TWRL/ (tape not ready to write) signal from the tape unit.

c. Read-After-Write Check Circuits. The read-after-write (RAW) check circuits (logic diagram sheet T.012) consists of a two-bit counter, a read after write register, and a data selector. The two-bit counter provides decoded counts of 0 to 3 which are gated with the outputs of the RAW register in the data selector. The data selector selects the data bit of the RAW register which corresponds to the data bit read back from the tape unit. These two data bits are applied as inputs to an exclusive OR gate. If the two inputs do not agree, the tape error (TE) flip-flop is set.

d. Status Interrupt Generator. The status interrupt generator (logic diagram sheet T.042) detects the presence of a status error condition and as a result, generates the status interrupt signal (SINT) which is sent to the processor.

e. Service Too Late Detector Circuits. These circuits produce signal STL when the processor has not responded to the data interrupt request in the required time period.

TIMING CONTROL

The timing control circuits are shown in Figure II-3 and consist of the following:

a. Control Word Register. The control word register (logic diagram sheet T.041) stores the control word sent by the processor. The outputs of this register are used to indicate the operation to be performed.

b. Write Control Logic. The write control logic (logic diagram sheet T.032) produces the enable write strobe (ENWSTR) and first parallel enable (1STPE) signals which are used to control the transfer of write data to the tape unit. Signal 1STPE is used to load the first write character into the shift register. Signal ENWSTR is produced by a flip-flop which is set when the first write character appears at the output stage of the data buffer register. Flip-flop ENWSTR remains set, thus enabling write strobes to the tape unit, until the data buffer register is empty.

Functional Detail

c. Write Strobe Generator. The write strobe generator (logic diagram sheet T.031) produces signal WSTR every 125 microseconds when flip-flop ENWSTR is set.

d. Master Timing Logic. The master timing logic (logic diagram sheet T.031) consists of a 13-bit counter, counter reset circuits, and decode circuits. The outputs of the 13-bit counter are decoded to produce a 125-microsecond signal (used to produce signal WSTR), a 256-microsecond signal (used during read operations to detect when tape is not up to speed or a false start has occurred), a 4.096-millisecond signal (used in the detection of record gap), and a 5-millisecond signal (used as the 5 msec tape mark to the processor).

FUNCTIONAL OPERATION

Initially, the processor sends a write (PSWRIT) signal along with an instruction (PSINST) signal to signify the presence of a control word on the MIR data lines. The control word is loaded into the control word register and the various bits are decoded to determine the operation to be performed. There are eight operations which can be performed, as described in the following subparagraphs.

WRITE OPERATION

A write operation is signified by the receipt of the "tape write" bit in the control word. (See Figure II-4.) In addition to the "tape write" bit, the processor sends the "threshold select" and "enable 5 msec mark" control bits for write operations. Receipt of the "tape write" bit generates signal WOP (write operation). Signal WOP is used to produce the forward drive level (FDL) and the tape write level (TWL) signals which are sent to the tape unit. Receipt of the "threshold" control bit generates the read clipping level (RCL) which is sent to the tape unit to enable the read-after-write feature.

Signal TWL enables the tape write circuitry, and signal FDL enables the tape forward-drive circuitry. While the tape is moving forward, the tape IOC is detecting the 5 msec timing counts produced by the master timing counter. For every 5 msec timing count detected, the "5 msec time mark" status bit is enabled and the tape IOC sends signal SINT (status interrupt) to the processor. The processor responds to each SINT signal with signals PSREAD and PSINST. When these signals are received from the processor, signal SELSTAT is produced.

This signal enables the output multiplexer for the status lines, and the status word is sent to the processor over the EXT data lines. The processor counts the number of 5 msec time marks sent by the tape IOC. If the write operation was started from the beginning of tape (BOT) position, the 5 msec tape marks are counted for a period of

140 milliseconds. If the write operation is not from the BOT position, only 100 milliseconds are counted.

When the proper timing period is complete, the processor sends a control word along with signals PSWRIT and PSINST to the tape IOC. This control word is identical to the first control word except that the "enable 5 msec mark" bit is reset and the "enable data interrupt" (ENDI) bit is set. Signal ENDI along with signal TCBIR enables the data interrupt signal (DINT), which is sent to the processor as a request for data. Signal TCBIR (buffer input ready) is true whenever the first input character location in the data register is empty.

The processor responds to the data request by sending a data word along with signal PSWRIT. (See Figure II-5.) Signal PSWRIT enables signal BSIN (buffer shift in), which gates the input data through the input multiplexer and into the data register. The data word (character) is shifted internally in the data register towards the output stage of the register. The first input character location becomes empty again and signal TCBIR goes true. As a result, another data interrupt is sent to the processor and the next data character is sent to the tape IOC. This action of loading data characters into the data register and shifting them to the output stages continues until the data register is full (64 characters). At that point, signal DINT is no longer generated. During the remainder of this write operation, signal DINT will only be generated when a data character is sent to the tape, thereby causing the characters in the data register to be shifted one character position toward the output stage. This one-character shift empties the input character location. When the processor has sent the last data character of the operation, it waits 45 milliseconds for the last character to reach the output stage of the data buffer register and then sends another write operation control word, this time, however, the "enable data interrupt" bit is reset. This action ends the input data character loading process.

Simultaneous with the character loading process just described, the tape IOC performs the actions necessary to write the data onto tape. This sequence of operations is shown on Figure II-6.

When the first data character reaches the output stage of the data register (approximately 20 microseconds after it is entered into the input stage), signal TCBOR goes true. Signal TCBOR enables the first parallel enable signal (TC1STPE) and sets the enable write strobe flip-flop (ENWSTR). Signal TC1STPE enables the parallel enable (PE) signal, which gates the output character of the data register into the shift register. At this point in the operation, the shift counter is at 0. As a result, the four least significant bits of the data character contained in the shift register are also loaded into the read-after-write (RAW) register, where the data is stored for the ensuing read-after-write check.
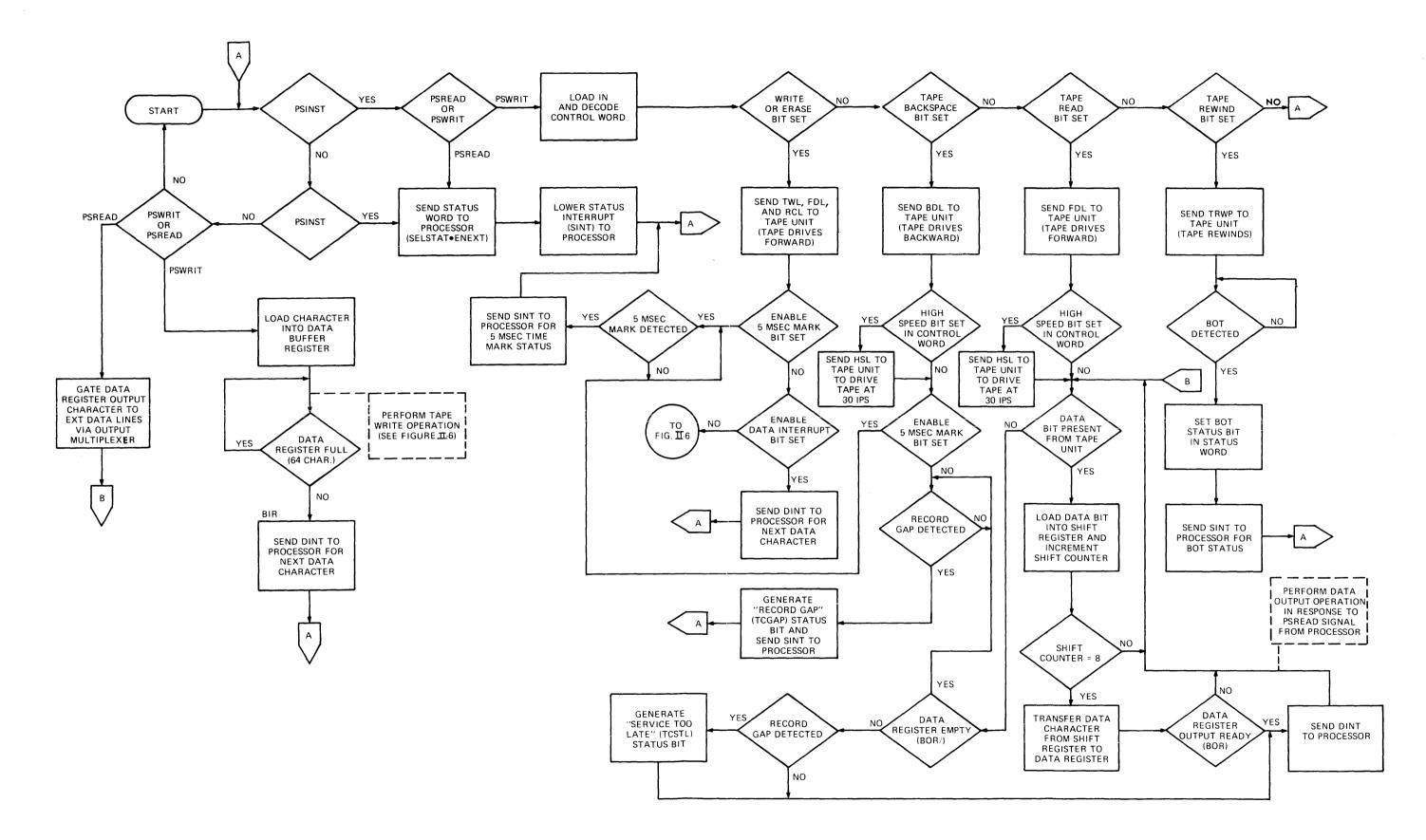
Fig. II-4 TAPE IOC, FLOW DIAGRAM

Functional Detail

When signal ENWSTR is true and a timing count of 125 microseconds is decoded from the master timing counter, the write strobe signal (WSTR) is generated. Signal WSTR is used to produce the tape write clock pulse (TWCP) for the tape unit. Signal TWCP is used to write a bit on the clock track of the tape. Also, signal TWCP enables the tape unit to gate in the data bit present on the tape write information line (TWIL). The tape write information line reflects the content of the least significant bit location of the shift register.

Signal WSTR also enables signal SHIFT which is used

to count up the shift counter. The shift counter is used to count the number of shifts (1 to 8) which occur in the shift register for each data character. A decoded signal (CTN4) is produced at counts of 0 and 4. What this does in effect is to detect when the least significant four bits and the most significant four bits are present in shift register bit locations TCT0 through TCT3, thus splitting the 8-bit character into two 4-bit digits. The read-after write register is a 4x64 bit register, therefore, the data characters have to be entered in two 4-bit groups.
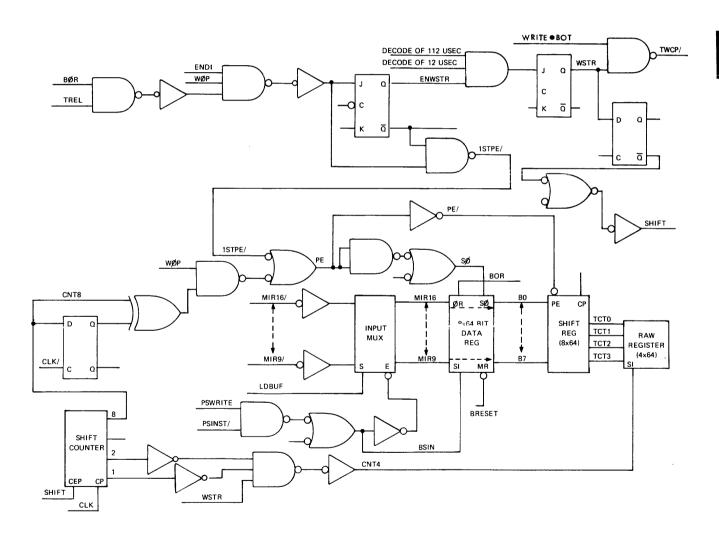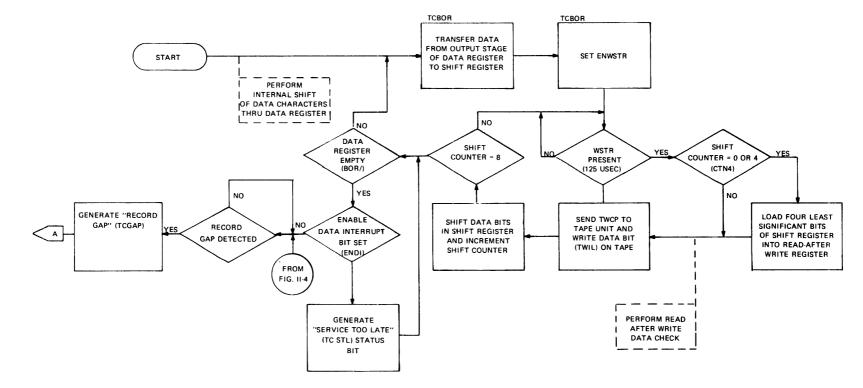

Fig. II-5 WRITE OPERATION, SIMPLIFIED LOGIC DIAGRAM

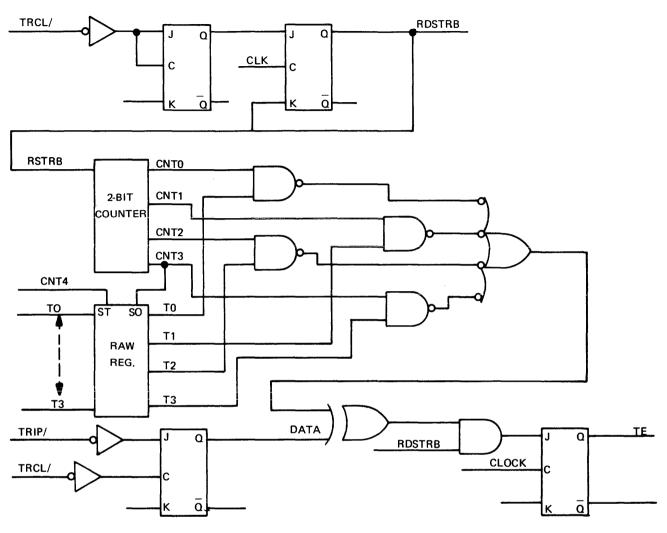Fig. II-6 WRITE OR ERASE OPERATION, FLOW DIAGRAM

Functional Detail

Fig. II-7 READ AFTER WRITE, SIMPLIFIED LOGIC DIAGRAM

When the next 125-microsecond time period is detected, another WSTR signal is generated and the next bit of the data character, along with its corresponding tape clock bit, is sent to the tape unit.

This cycle continues until the complete data character is sent to the tape unit. At this point in the operation (shift counter equals 8), another data character is transferred to the shift register, if one is present in the output stage of the data buffer register (BOR is true), and the cycle to transfer a data character to the tape unit is repeated. If another data character is not present in the data buffer register output stage at this time and the "enable data interrupt" bit is still set, the "service too late" status bit is enabled.

The read-after-write data check portion of the write operation is accomplished by temporarily storing in the read-after-write (RAW) register a record of the data characters sent to the tape. (See Figure II-7.) The RAW register, at all times during the operation, reflects the most recent data characters sent to the tape unit (approximately 15 characters are present in the RAW register at one time).

A two-stage bit counter is used to count the bits read back from tape over the tape read information line (TRIP). The counts decoded from this counter are 0 through 3. These counts correspond to the four bits present at the output stage of the RAW register at any given time. Output bits 0 through 3 of the RAW register are ANDED with outputs 0 through 3 of the bit counter in a decoding network. As a result, the counter output enables the corresponding RAW register bit to be applied to one input of an exclusive OR gate. At the beginning of the operation, the first four data bits sent to the tape unit are reflected in the contents of the four-bit output stage of the RAW register. When the first data bit written on tape is read back, it is applied to the other input of the exclusive OR gate. If both inputs to the exclusive OR gate do not agree, the gate is satisfied and the tape error flip-flop (TCTE) is set. As a result, the tape error status bit is enabled. When the bit counter is at a count of 3, the four-bit digit present at the RAW register output stage is shifted out of the register. As a result, the next four-bit digit is shifted into the output stage.

Functional Detail

When signal BOR goes false (data buffer register is empty) and the "enable data interrupt" bit is reset, flip-flop ENWSTR is reset. Signals ENWSTR/ and EN5MS/ are gated with signal RDSTRB (read strobe) to produce signal RRDS. Signal RRDS resets the master timing counter. As a result, the master timing counter is reset every time a data bit is read back from tape. After the last data bit is read back, the master timing counter proceeds to count up to its maximum count. When the count reaches 4096 (4.096 milliseconds), the record gap flip-flop is set.

The record gap flip-flop enables the record gap status bit (TCGAP), and a status interrupt is sent to the processor. The processor responds to the status interrupt with signals PSINT and PSREAD, and the status word is sent to the processor through the output multiplexer gates and the EXT data lines. This status word may contain, in addition to the record gap status bit, a "tape error" status bit or a "service too late" status bit if either or both of these conditions occurred during the operation.

Following receipt of the status word from the tape IOC, the processor sends a control word with the "enable 5 msec mark" bit set. The tape IOC responds with a status word for every 5 msec time mark detected. If another tape write operation is to follow, the processor counts 5 msec time marks for a period of 25 milliseconds; after which another tape write operation is initiated. Otherwise, the processor counts 5 msec time marks for a period of 55 milliseconds and then sends a control word with the "tape write" and "threshold select" bits reset and the "enable 5 msec mark" bit set. The resetting of the tape write bit causes signal FDL to go false. As a result, the forward movement of the tape stops. This 55 millisecond additional forward movement of tape is used to ensure a record gap of 1 inch (minimum). The tape IOC continues to send a status word for every 5 msec time mark detected. When the processor detects that a time period of 75 milliseconds has elapsed since the last control word was sent, it sends another control word to the tape IOC. This time the "enable 5 msec" control word bit is reset and the operation is terminated.

TAPE ERASE OPERATION

A tape erase operation is the same as that described for the tape write operation, except that the processor sends the "tape erase" bit instead of the "tape write" bit in the operation control word. The erase control bit produces signal ERASE in the tape IOC. The functions of signal ERASE are the same as signal WRITE except for the following differences:

a. Signal TWCP is not produced because no characters are to be written on tape. As a result, the clock track is erased.

b. Because data characters containing all 0's (null characters) are transferred to the tape IOC by the

processor during a tape erase operation, detection of the record gap is different. During an erase operation, the record gap flip-flop is set when signal BOR goes false (data register is empty).

WRITE TAPE MARK OPERATION

The write tape mark operation is very similar to the tape write operation. In the beginning of the operation, the processor counts 5 msec tape marks for a period of 350 milliseconds instead of 100 milliseconds as in the tape write operation. The actual data transfer consists of four characters: a preamble character, two data characters of all 0's, and a postamble character. The final difference occurs in the terminate portion of the operation. Following receipt of the record gap status word from the tape IOC, the processor counts 5 msec time marks for a period of 350 milliseconds instead of 55 milliseconds as in the tape write operation.

TAPE BACKSPACE OPERATION

A backspace operation is signified by the receipt of the "backspace" bit in the control word. (See Figure II-4.) The backspace control bit generates signal BACKSP which gates the backward drive level (BDL) to the tape unit. The tape is driven backward at the normal 10-inch per second speed. The data bits of the previous record are read out to the tape IOC. As in the read-after-write data check, receipt of a data bit resets the master timing counter. When the record has completely passed the read heads, the master timing counter is no longer inhibited. When the counter reaches a count of 4096, the record gap flip-flop is set and a record gap status word is sent to the processor. The processor responds with a backspace control word that has the "enable 5 msec mark" control bit set. The tape IOC sends a status word for each 5 msec tape mark detected. The processor counts the tape 5 msec tape marks for a period of 55 milliseconds; after which, it sends a control word with the backspace bit reset and the "enable 5 msec tape mark" bit still set. As a result, the backward drive level goes false. The tape IOC continues to send 5 msec tape mark status to the processor. When another 75 milliseconds has elasped, the processor sends a control word with the " "enable 5 msec mark" bit reset and the operation is terminated.

READ OPERATION

A read operation (Figure II-4) is signified by the receipt of the "tape read" bit in the control word. The tape read control bit generates signal TCREAD in the tapes IOC. Signal TCREAD is used to enable signal FDL to the tape unit. The tape is driven forward. As the read heads pass over the data, the data bits are sent to the tape IOC serially, where they are loaded into the shift register. (See Figure II-8.) The shift register is shifted each time a new

Functional Detail

data bit is entered. The clock bits received from the tape unit are used to produce signal RDSTRB (read strobe). Signal RDSTRB enables signal SHIFT, which increments the shift counter. During read operations, the shift counter is used to indicate when the shift register is full (count of 8).

When the shift counter output equals a count of 8, signal TCLDBUF (load buffer) is enabled. Signal TCLDBUF generates the buffer shift in signal (BSIN), which transfers the data character contained in the shift register into the first input location of the data buffer register via the input multiplexer. If the second data character read is not received within 256 microseconds of the first data bit, a false start is indicated. A false start can occur because of dirt on the tape being read as a clock bit or because the tape is not up to speed. As a result, the data buffer register and shift register are reset. The next data character read is then considered the first character of data. When two characters are read within 256 microseconds of each other, the false start circuitry is disabled.

This cycle of loading characters into the data buffer register continues until the first character loaded into the data buffer register is shifted through and appears at the output stage. A character present at the output stage of the data buffer register produces signal BOR (buffer output ready). Signal BOR enables the data interrupt (DINT) signal, which is sent to the processor to request a data transfer.

The processor responds to the data input request with signal PSREAD. This signal enables signals BSOUT (buffer shift out) and ENEXT (enables EXT lines). Signal BSOUT transfers the output character of the data buffer register to the output multiplexer. Signal ENEXT enables the transfer of the output data to the EXT data lines and the data character is sent to the processor.

This cycle continues until the last character is read from tape. At this point in the operation, the master timing counter is allowed to count. (The master timing counter is reset each time a data bit is received from tape.) When the timing counter reaches a count of 4096 (4.096 milliseconds), the record gap flip-flop (TCGAP) is set. If at this time characters are still present in the data buffer register (BOR is true), the "service too late" status bit (TCSTL) is set in the status word. In either case, the "record gap" status bit is set upon detection of the record gap and signal SINT is sent to the processor. The processor responds to the status interrupt with signals PSREAD and PSINST. These signals generate signal SELSAT, which enables the output multiplexer for the status word. If the next S-level instruction in the processor is another read operation, the processor sends a control word to the tape IOC to initiate the operation. However, if another read operation is not indicated, the processor sends a control word with the "enable 5 msec mark" bit set and the "enable data interrupt" bit reset. The tape IOC responds with signal SINT for every 5 msec tape mark detected. The processor counts the 5 msec tape marks for a period of 45 milliseconds and sends a control word with the "enable 5 msec" bit reset, thus terminating the operation.
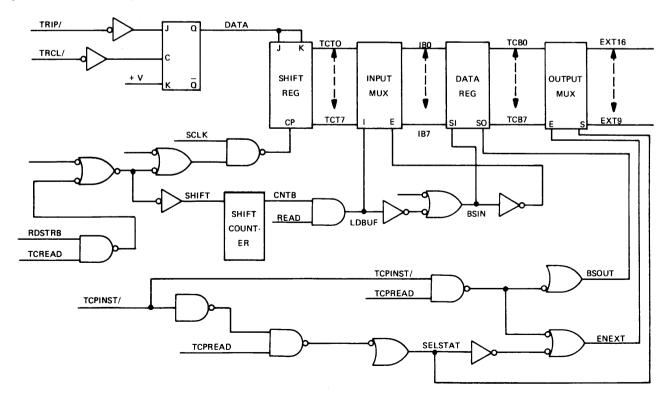

Fig. II-8 READ OPERATION, SIMPLIFIED LOGIC DIAGRAM

Functional Detail

TAPE MARK SEARCH FORWARD OPERATION

The tape mark search forward operation is the same as that described for the read operation, except that the "high-speed" control bit is set along with the "tape-read" and "enable data interrupt" control bits. The "high speed" control bit sets the high speed level flip-flop (TCHSL), which gates the high speed level (HSL) to the tape unit. The high speed level in conjunction with the forward level causes the tape to drive forward at a speed of 30 inches per second. The tape IOC sends data back to the processor as in a normal read operation. Each time a non-tape mark record is detected (five or more characters), the processor sends a control word with the "enable data interrupt" bit reset. When the record gap following the non-tape mark record is detected, record gap status is sent to the processor. The processor responds with another control word containing the "enable data interrupt" bit.

When the tape mark record is detected followed by a record gap, record gap status is sent to the processor. The processor responds with a control word in which the "enable data interrupt" bit is reset and the "enable 5 msec mark" bit set. The processor counts the tape IOC 5 msec tape mark status interrupts for a period of 25 milliseconds, after which a control word with the "tape read" and "high speed" bits reset is sent to the type IOC. The tape IOC continues to send 5 msec status interrupts to the processor. After an additional period of 200 milliseconds, the processor sends a control word with the "enable 5 msec mark" bit reset and operation is terminated.

TAPE MARK SEARCH REVERSE OPERATION

The tape mark search reverse operation is identical to the tape mark forward search operation except for the direction of tape movement. The control word for this operation contains the "backspace" bit in addition to the other control bits sent for the tape mark forward search operation.

REWIND OPERATION

A rewind operation is signified by receipt of the "tape rewind" bit in the control word. The tape rewind control bit generates signal RWND which resets the EOT and TWL flip-flops. (See Figure II-4.) When the TWL flip-flop is reset and signal RWND is true, the tape rewind pulse (TWRP) is sent to the tape unit. The tape rewinds at a speed of 60 inches per second. When the clear leader is detected by the tape sensors, the clear leader position level (CLPL) is sent to the tape IOC. Signal CLPL sets the BOT flip-flop. (The BOT flip-flop is wired in reverse fashion in order to provide a non-clocked setting capability.) When the BOT flip-flop is set, the BOT status bit (TCBOT) is set in the status word and the status interrupt (SINT) is sent to the processor. The processor responds with a control word which contains the "enable 5 msec mark" bit. The processor counts the 5 msec tape mark status interrupts from the tape IOC for a period of 200 milliseconds (time required for tape to come to a complete stop); after which the processor sends a control word with the "enable 5 msec mark" bit reset.

Circuit Detail

GENERAL

The integrated circuit chips contained in the tape IOC consist of the following types:

Type	PART NO.
CB	1447 3771
DF	1447 3607
JF	1447 3615
RAF	1448 9165
SU	1447 3755
S2	· 1447 3797
T1	1447 3532
T2	1447 3516
T2A	1447 3524
T2C	1447 3581
T2H	1479 0240
T3	1447 3540
T3A	1447 3557
T4	1447 3565
X4	1447 3698

These chips, with the exception of the RAF chip, are described in the B700 processor manual, form 1064482. The RAF chip is described in the following paragraphs.

RAF 4-BIT X 64-WORD FIFO SERIAL MEMORY

The RAF 4X64 FIFO (first-in first-out) serial memory chip is shown in Figure III-1.

The RAF chip is a 4-bit X 64-word memory chip that operates on the first-in first-out concept; that is, the first word entered is shifted through all 64 locations and be-

comes the first word available for output. Inputs and outputs are completely independent; however, for every input (even if the data are zeroes) there will be an output. This is accomplished by internally counting all shift-in (SI) signals and decrementing the count for every shift-out (SO) signal. When the input stage of the RAF memory is empty, signal IR (input ready) is generated. Conversely, when the output stage contains a word, signal OR (output ready) is generated. Signal OR stays high as long as the count of SI signals is greater than zero.

Figure III-2 is a functional block diagram of the RAF chip. The four bits of the data word are entered at inputs D0-D3 when both signals IR and SI are high. Data in the input stage causes signal IR to go low. When signal SI goes low, the data word is propagated to the second data location, provided that location is empty. Signal IR goes high again because the input stage is empty. Once data is transferred to the second data location, the transfer of any full data location to the next (adjacent) empty data location is automatic. This transfer is activated by an on-chip control. Thus the data words stack up at the output stage of the chip. When a data word is present at output pins Q0-Q3, signal OR goes high. When signals OR and SO are both high together, the data word is shifted out. As a result, signal OR goes low. However, the outputs at Q0-Q3 are maintained until both signals OR and SO are low. When these signals are low, the contents of the memory are shifted to the adjacent empty location. Thus, signal OR goes high again. However, if the memory is empty, signal OR stays low.
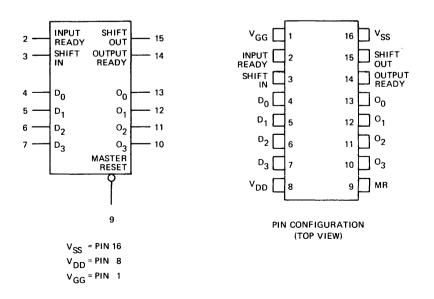
V_{SS} = PIN 16
V_{DD} = PIN 8
V_{GG} = PIN 1

PIN CONFIGURATION
(TOP VIEW)

Fig. III-1 RAF 4X64 FIFO MEMORY (1448 9165)
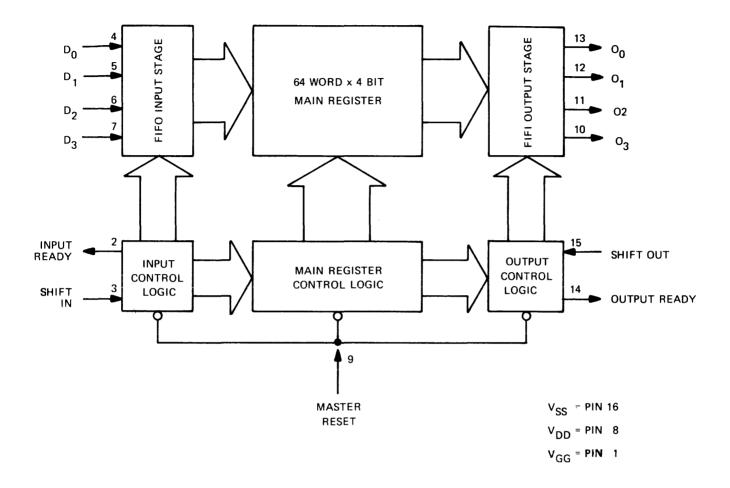
Circuit Detail

Fig. III-2 RAF MEMORY, FUNCTIONAL BLOCK DIAGRAM

Maintenance Procedures

MAINTENANCE PHILOSOPHY

The approach used in detecting, diagnosing, and repairing failures in the tape IOC is to run the appropriate Maintenance Test Routines (MTR's) and then replace or repair defective circuit chips or discrete components in accordance with the diagnostic information obrained from the MTR's. Additional manual diagnostic operations, using this technical manual, FT&R documentation, and test equipment may be required by the Field Engineer to further diagnose and repair failures if the MTR's do not locate the defective component/circuit.

MAINTENANCE AIDS AND EQUIPMENT

The following maintenance aids are required to implement the MTR's and perform maintenance on the tape IOC:
a.   Field Engineering (F.E.) cards FE-1 through FE-4.
b.   MTR meter.
c.   Tektronix Model 453 oscilloscope.
d.   Processor card extender kit (1447 7102).
e.   Applicable MTR's.
f.   Special maintenance tools (insertion/extraction, wire wrap/unwrap, pin extractor, and card puller tools).
g.   A scratch (blank) cassette with 40-inch BOT and write enabled.

The B700 Processor Technical Manual, form 1064482 Section V, contains descriptions and identification/application data for the F.E. cards, MTR meter, and card extender kit.

MAINTENANCE TEST ROUTINES (MTR'S)

Each B700 system installation is provided a set of MTR's on site-compatible media, tailored to the installation configuration and revision level. The MTR Configuration Document (2601 8200), issued by the respective branch office to each installation, provides a complete list of MTR reference data, including the revision status and applicability.

The MTR provided for the B0392 tape IOC is the TCMTR (1449 0916). A program listing, complete operating instructions, a failure dictionary, and waveforms are provided in the TCMTR Operator Instructions Document (Listing), 1449 0833.

When implemented, the TCMTR detects and diagnoses failures within the tape IOC, or validates the operation of the tape IOC and interfacing magnetic tape cassette. The TCMTR cannot diagnose a failure in the magnetic tape cassette, but can be interpreted to indicate or point to a failure in the magnetic tape cassette.

Note that, for complete diagnosis or validation of the tape IOC and magnetic tape cassette operations, the FEMT, MEMLDR, PROC, BSW, MCU, CONS or CONS96 (or SPO in B771), and DPM MTR'S must be run in the sequence indicated before the TCMTR is run. Also note the minimum revision level requirements when testing a tape IOC used in B771 applications. Refer to Section V of the B700 Processor Technical Manual, form 1064482, for a description of the MTR implementation and diagnostic process.

<p align="center">Installation Procedures</p>

INSTALLATION OF B0392 IOC

The B0392 IOC consists of the following:
1. Four P.C. Cards (TC1-TC4).
2. Two frontplane connectors.
3. One adapter cable (1449 0288).
4. Two backplane templates.
5. One set of instructions.
6. One set of FT & R documents.
7. One decal.
8. One bracket to install tape unit under console table top.

Insure that all parts are present before installation.

Installation.
1. Ensure that all components are seated properly in their receptacles.
2. Install P. C. cards in their proper IOC location as listed in Table VI-1 (B705/711) or Table VI-2 (B771).
3. Install frontplane connectors to P. C. cards.
4. Install decal on DDP decal corresponding to the IOC location.
5. Install adapter cable from processor backplane plug corresponding to IOC location as listed in Table VI.1, or Table VI.2.
6. Install I/O end of adapter cable to processor adapter panel.
7. Write in the adapter cable type on the adapter panel decal in the corresponding block.
8. Install the I/O cable to the adapter cable (refer to B700 Processor Manual Section VI).
9. Check +5 volts as described in Vol. I of the Central Processing Unit FT & R documents.
10. Run the appropriate MTR to insure proper system operation.

TABLE VI-1. TAPE IOC CARDS, LOCATIONS, AND CONNECTORS (B705/711 PROCESSOR)

TYPE	PART NO.	FUNCTION	1 (J97)	2 (J96)	3 (J95)	4 (J94)	5 (J93)	6 (J92)	7 (J91)
TC1	1448 9108	Control	FW6	DW6	FV4	DV4	FU2	DU2	DTO
TC2	1448 9132	Data 9-16	FW3	DW3	FV1	DV1	FT9	DT9	DS7
TC3	1448 9074	Data 1-8	FWO	DWO	FU8	DU8	FT6	DT6	DS4
TC4	1449 0312	Special	FV7	DV7	FU5	DU5	FT3	DT3	DS1

TABLE VI-2. TAPE IOC CARDS, LOCATIONS, AND CONNECTORS (B771 PROCESSOR)

TYPE	PART NO.	FUNCTION	2 (J96)	3 (J95)	4 (J94)	5 (J93)	6 (J92)	7 (J91)
TC1	1448 9108	Control	DW6	FV4	DV4	FU2	DU2	DP1
TC2	1448 9132	Data 9-16	DW3	FV1	DV1	FT9	DT9	DN8
TC3	1448 9074	Data 1-8	DWO	FU8	DU8	FT6	DT6	DN5
TC4	1449 0312	Special	DV7	FU5	DU5	FT3	DT3	DN2