Burroughs Corporation
Field Engineering Training
Detroit

Course No. BMG 320527
INT 303360

B 1714

MAINTENANCE AND BASIC SOFTWARE PERFORMANCE ORIENTED TRAINING

Printed in U.S. America 3-1-76

Form 1093671

TABLE OF CONTENTS

INTRODUCTION

These performance objectives are intended to be the testing criteria for students learning the B1700 Mainframe. Successful completion of the course consists of the student demonstrating his ability to properly perform each of the objectives to the instructors satisfaction.

The objectives are designed to be used in conjunction with formal lectures on each subject area or as the basis for a supervised self paced learning program.

The objectives are arranged in a particular sequence and it is intended that they be accomplished in that sequence. This is of particular importance for the less experienced students. Those objectives flagged by the letter "M" in the right hand margin require the student to perform the action on the machine while those without the "M" can be performed without direct access to a system.

The references given for each objective are intended to provide the student with sufficient background and detail to perform the objective. In the event that the student is unable to determine what is expected of him or he cannot obtain sufficient information from the references, he should consult with the instructor before proceeding.

MATERIAL PROVIDED EACH FIELD ENGINEER

1. B1714 Technical Manual
2. B1700 Reference Manual
3. B1700 Software Operation Guide
4. B1714 Performance Oriented Training Course

MATERIALS AVAILABLE IN THE LAB

1. B1700 Element Rule Book
2. System Documentation
3. Card Tester Manual
4. B1700 MTR Listing
5. B1700 Planning and Installation Manual

TITLE: B1714 Maintenance and Basic Software

COURSE DESIGNATION: 320527

LENGTH: 160 Hours

DESCRIPTION: The course is designed to train the field engineer to install, operate and repair the B1712/14 processor on a MTR (card tester) basis to include:

1. B1712/14 Mainframe
2. Burroughs Logic Power Supply
3. PMI Logic Power Supply
4. Memory Power
5. Memory Sub-system

SUBJECT MATTER:

Ref: Welcome Package

A. INTRODUCTION & ORIENTATION

1. Welcome
2. Housing
3. Transportation
4. Meals
5. Laundry
6. Professionalism at training center
7. Week-end trip
8. Course Schedule
9. Tour of training area

Ref: B1700 SOG Section I & II

B. B1700 OPERATING SYSTEM (8 Hrs)

1. Define
2. Functions
3. Controlling of MCP
4. How Loaded
5. Disk Structures

Ref: B1700 SOG
Section II & III
Release Letter

C. OPERATOR TRAINING (32 Hrs)

1. SPO Message (Selected)
2. Control Statements
3. MCP Options
4. Utility Programs

Section IV

5. Compiles

B1700 SOG Section I & II

6. File Concepts

Section III SOG

7. Sorts

Form MKT. 6269

8. MCP II/ANALYZER
9. Dump/Analyzer
10. System Log Operation

Ref: B1714 TM, Sec. I
B1700 Ref. Manual
Viewgraphs

D. B1700 SYSTEM CONCEPTS (5 Hrs)

1. Basic Block Diagram
2. Clock Rate
3. Memory Size
4. Type of Memory
5. Type of logic
6. I/O Subsystem
7. Micro Concepts
8. Maintenance Philosophy
9. System in-depth diagram

Ref: Element Rule &
B1714 TM
Section V

E. MACHINE LAYOUT (2 HRS)

1. Card Layout

   a. Integrated components
   b. Voltage/Ground Busses
   c. FP Connector
   d. BP Pin designation
   e. Resistor locations
   f. Wire wrap levels

2. Subassembly Layout

   a. Processor
   b. I/O Base
   c. Logic Power
   d. Memory Power
   e. Memory Sub-system
   f. 24 Volt Chasis
   g. Console
   h. Cassette
   i. I/O Cable Panel

3. Backplane Layout

   a. Letter/Number designations
   b. Pin Numbers

4. Voltage/Ground Bussing

   a. +4.75 volts
   b. $\pm$ 12 volts
   c. -2 volts
   d. Ground

Ref: B1700

F. CARD TESTER OPERATION (6 hrs)

1. Function
2. Principles of Card Testing
3. How to operate

Ref: Element Rules
Student Worksheets
System Documentation
Viewgraphs

G. FIELD TEST AND REFERENCE (8 hrs)

1. Element Rules

NOTE: Worksheets examples taken from B1714 schematics

2. Documentation

a. Card schematics
b. Circuit list
c. History sheets
d. Special instruction
e. Test routines

Ref: Card Tester Manual
Training Handout &
Card Tester Schematics

H. REPAIRING THE CARD TESTER (5 hrs)

1. Theory of Operation
2. Troubleshooting

Ref: B1714 TM, Section V
Training Handout &
MTR Listing

I. MAINTENANCE PROCEDURES (3 hrs)

1. Test Routines
2. Confidence Routines
3. Isolating to a failing unit

Ref: B1714 TM, Section I, pg. 2, Section I, pg. 12-24

J. CENTRAL PROCESSOR (40 Hrs)

1. Processor Block Diagram

2. Selected Micro Instructions

B1712, TM, Sec. 2, pg 8

3. Clock Circuit

Sec. II, pg. 34, 41 & 90

4. Local Memory Block Diagram

Sec. II, pg. 53
Sec. II, pg. 75 & 77

5. Function Box Block Diagram

   a. 24 bit
   b. 4 bit

B9490 TM

6. Cassette

   a. Function
   b. Drive circuits
   c. Processor Control
   d. U Reg
   e. Error checking concept

Ref: Sec. II, pg. 171

K. MEMORY (22 Hrs)

1. Type of memory used

2. Bit addressability concept

   a. S-Proc. 1
   b. S-Proc. 2

3. Reverse memory operation

4. Develop diagram (chalkboard) of memory writes and reads at different addresses.

Sec. II, pg. 192
Training handout
Viewgraph

5. Data path to/from memory

   a. Source/destination regs.
   b. Rotator
   c. MIR

Sec. II, pg. 174

6. Physical/Electrical layout of Data Path

Sec. II, pg. 175, 177

7. Storage Boards

   a. S-Proc. 1
   b. S-Proc 2

K. CONT.

Ref: Sec. II, pg. 189-191

Test Routine Listing

B1714, Sec. IV, TM & TIN 4468

Section II, pg. 93

8. Memory Timing
9. Memory Test Routing
10. Memory Voltages & Margins
11. Micro Instruction Fetch

Ref: ALL

L. PROCESSOR/MEMORY REVIEW (2 Hrs)

1. Relating B/D to schematics
2. Relating schematics to boards

Ref: Sec. I, pg. 33-36

Sec. II, pg. 201-229
Sec. IV, pg. 29-36

Sec. I, pg. 36
Sec. IV, pg. 30, 31

M. SYSTEM POWER (24 Hrs)

1. Power Distribution
2. PMI Power Supply
3. Burroughs Manufactured Supply
4. Memory Power
   a. DC voltage input
   b. +19 & +23 volt supply
   c. Adjustment
   d. Troubleshooting

Ref: Planning & Installation Manual TIN 4464

N. PLANNING & INSTALLATION

1. RINS
2. LINS
3. TINS
4. CARES Forms
5. Power Requirements
6. Heat Requirements
7. Site Planning

Prepared by: M. Murray
(Originator)

Approved by: M. L. Sokol
(Training Project Supervisor)

Approved by: L. L. Turnbow
(Manager, Field Engineering Training) 2/18/76
DATE

B1700 SYSTEM OPERATION UNDER MCP CONTROL	
Software Operating Guide (SOG) Sec. II, & III	M 1. PERFORM A CLEAR/START TO INCLUDE SETTING OF THE TIME AND DATE.
Software Operation Guide (SOG) Sec. II	M 2. DIRECT MCP TO KEEP A LOG OF THE SYSTEM OPERATIONS.
SOG. Sec. II	M 3. OBTAIN A SOFTWARE RELEASE LETTER FROM THE SYSTEMS DISK SUPPLIED BY YOUR INSTRUCTOR.
SOG	M 4. EXECUTE "TESTER" AND PERFORM ALL OF THE OBJECTIVES. SHOW THE SPO SHEET TO THE LAB INSTRUCTOR.
SOG SEC. III	M 5. INITIALIZE BOTH A USER AND A SYSTEM DISK.
Release Letter	M 6. USE DISK/DUMP TO MAKE A DUPLICATE COPY OF THE SYSTEM DISK.
Software Operation Guide Sec. III	M 7. VERIFY A DISK CARTRIDGE AFTER COMPLETION OF A DISK/DUMP ROUTINE.
Software Operation Guide Sec. III	M 8. COPY ALL OF THE SDL. INTRIN/= FILES TO THE USER DISK GIVING THEM NEW NAMES USING THE PROGRAM DISK/COPY. THEN COPY THEM BACK ONTO THE SYSTEM DISK GIVING THEM THEIR ORIGINAL NAMES.

B1700 SYSTEM OPERATION UNDER MCP CONTROL	
3-15 Software Operation Guide Sec. III	M 9. USING DMPALL PRINT THE FOLLOWING TYPES OF DATA FILES: A. CARD B. DISK C. ~~MAGNETIC TAPE~~ D. ~~PAPER TAPE~~
3-15 Software Operation Guide Sec. III	3-15 M 10. USING DMPALL PRINT A DISK FILE BEGINNING WITH A SPECIFIED RECORD AND TERMINATE AFTER A SPECIFIED NUMBER OF RECORDS ARE PRINTED.
3-15 Software Operation Guide Sec. III	M 11. USING DMPALL REPRODUCE THE FOLLOWING TYPES OF DATA FILES CHANGING THE BLOCKING FACTOR FOR THE DISK FILE: A. CARD B. DISK C. ~~MAGNETIC TAPE~~ D. ~~PAPER TAPE~~
Software Operation Guide Sec. III	3-23 M 12. USE FILE/PUNCHER TO PUNCH OUT A SMALL CODE FILE.
Software Operation Guide Sec. III	M 13. LOAD A CARD DECK CODE FILE TO DISK USING FILE/LOADER.
Software Operation Guide Sec. III	M 14. GIVEN A DECK OF CARDS CONTAINING A LIST OF STUDENTS IN CLASS, PRINT ~~20~~ 3 COPIES OF THAT DATA DECK.

B1700 SYSTEM OPERATION UNDER MCP CONTROL	
Software Operation Guide Sec. II	M 15. OBTAIN A PRINTOUT OF THE SYSTEM LOG USING SYSTEM/LOGOUT.
Software Operation Guide Sec. II	M 16. OBTAIN A PRINTOUT OF THE SYSTEM LOG USING QWIKLOG.
Software Operations Guide Sec. III	M 17. PERFORM A COLD/START OPERATION.
Software Operation Guide Sec. II	18. GIVEN A KA LISTING, DETERMINE THE RECORDS PER AREA FOR ANY GIVEN DATA FILE.
Software Operations Guide	19. DETERMINE THE NUMBER OF AVAILABLE DISK SEGMENTS ON A USER DISK.
Software Operating Guide See Instructor	M 20. GIVEN A CARD DECK LABELLED "SUPPLY/SALES" PERFORM A SORT OF THAT FILE. SORT ON THE SOCIAL SECURITY NUMBER, AND PLACE THE OUTPUT ON A USER DISK. CARD FORMAT: NAME — COLUMN SSN — 1-11 LAST NAME — 13-19 FIRST INIT. — 22 REGION — 29 DISTRICT — 36-37 BRANCH — 46-48 QUOTA — 57-60 SALES — 69-72

B1700 SYSTEM OPERATION UNDER MCP CONTROL	
Software Operations Guide Sec. III	M 21. USE DMPALL TO PRINT THE SORTED FILE FROM DISK.
Software Operations Guide Sec. III	M 22. SORT THE ABOVE DISK FILE USING THE FOLLOWING FOUR KEYS TOGETHER. DIRECT THE OUTPUT TO THE PRINTER. A. REGION B. DISTRICT C. BRANCH D. COMPLETE NAME
Software Operation Guide Sec. II	M 23. OBTAIN A PRINTOUT OF THE SYSTEM LOG.
RPG Reference Manual Software Operation Guide Sec. IV	M 24. GIVEN A RPG SOURCE DECK, COMPILE THE PROGRAM FOR SYNTAX.
COBOL Reference Manual Software Operations Guide (S.O.G.) Sec. IV	M 25. USING THE COBOL SOURCE DECK SUPPLIED BY YOUR INSTRUCTOR, COMPILE FOR SYNTAX USING SINGLE SPACE FORMAT. SHOW CODE, HEX ADDRESSING AND VERIFY THE CORRECT SEQUENCE.
Software Operating Guide (S.O.G.) Small System Tec. Newsletter-020	M 26. YOU MUST BE ABLE TO HALT THE SYSTEM, PERFORM A MEMORY DUMP AND OBTAIN MEANINGFUL INFORMATION FROM THIS DUMP TO INCLUDE THE FOLLOWING: A. DISK DESCRIPTOR CHAIN B. STATUS OF PERIPHERALS C. MIX STATUS D. OPTION STATUS E. ADDRESS (PORT & CHANNEL) OF PERIPHERALS F. INTERPRETERS PRESENT

B1700 SYSTEM OPERATION UNDER MCP CONTROL	
Software Operation Guide Sec. II	M 27. CAUSE A DUMP OF A USER PROGRAM. OBTAIN MEANINGFUL INFORMATION CONCERNING THE FOLLOWING: A. RUN STRUCTURE NUCLEUS B. I/O DESCRIPTORS C. FILE INFORMATION BLOCK
Software Operation Guide MKTG-6269	M 28. IF AND WHEN THE MCP HALTS WITH A HEX VALUE IN THE "L" REGISTER, PERFORM THE MEMORY DUMP PROCEDURE AND COMPLETE THE B1700 SYSTEMS "SOFTWARE ASSISTANCE REQUISITION" REPORT.
All	M 29. INVESTIGATE FOR 30 MINUTES A TROUBLE IN A B1714 SYSTEM, PREPARING A LIST OF FACTS ABOUT THE TROUBLE. REPORT YOUR FINDINGS TO THE INSTRUCTOR AND BE PREPARED TO ANSWER PROGRAMMATICAL AND TECHNICAL QUESTIONS REGARDING THE TROUBLE.
All	M 30. GIVEN A TROUBLE IN A B1714 SYSTEM, PERFORM THE FOLLOWING, USING ANY TROUBLESHOOTING AID OR TEST ROUTINE: A. RECOGNIZE AND IDENTIFY SYMPTOMS. B. DEFINE SYMPTOMS AS A GENERAL FUNCTIONAL FAILURE. C. RECREATE (IF POSSIBLE) THE CONDITIONS WHICH PRODUCED THE SYMPTOMS.

SYSTEM INTRODUCTION AND FAMILIARIZATION	
Instructor	31. LOCATE AND MAINTAIN THE FOLLOWING: A. TOOL CABINET B. SYSTEM DOCUMENTATION CABINET
All	M 32. GAIN ACCESS TO ANY SPECIFIED AREA OF THE B1714 SYSTEM.
B1714 TM Sec. II, Pg. 1-2 Sec. V Pg 14-16	M 33. DETERMINE THE CONTENTS OF ANY REGISTER THROUGH USE OF THE CONSOLE SWITCHES.
B1714 TM Sec. II, Pg. 1-2 Sec. V, Pg. 14-16 6 3 2 5 04	M 34. GIVEN A SPECIFIC BIT PATTERN IN HEXIDECIMAL, LOAD IT INTO ANY GIVEN REGISTER VIA THE CONSOLE SWITCHES.
B1714 TM, Sec. I, Pg. 3 Sec. V, Pg. 16	M 35. DEMONSTRATE YOUR ABILITY TO OPERATE THE CASSETTE READER BY PERFORMING THE FOLLOWING: A. POWER-ON CASSETTE READER B. LOAD CASSETTE INTO READER. C. MAKE CASSETTE READER READY. D. REWIND CASSETTE.

SYSTEM INTRODUCTION AND FAMILIARIZATION	
Processor MTR and Dynamic Test Routine Listing	M 36. INSURE THAT THE PROCESSOR IS FUNCTIONING PROPERLY BY LOADING AND EXECUTING THE PROCESSOR MTR AND DYNAMIC TEST ROUTINES.
B1714 IM Sec. II, Pg. 1-2 Sec. V, Pg. 14-16	M 37. GIVEN A HEX BIT PATTERN, WRITE THAT PATTERN INTO THE FIRST TEN BYTES OF MEMORY.
B1714 TM Sec. II, Pg. 1-2 Sec. V, Pg. 14-16	M 38. VERIFY THAT THE INFORMATION IN MEMORY AS A RESULT OF THE PREVIOUS OBJECTIVE, WAS WRITTEN CORRECTLY.
S-Memory Dynamic Test Listing	M 39. INSURE THAT THE S-MEMORY IS FUNCTIONING PROPERLY BY LOADING AND EXECUTING THE S-MEMORY DYNAMIC TEST.

SYSTEM LAYOUT	
B1714 T.M. Sec. V, Pg. 20	M 40. GIVEN THE CO-ORDINATES FOR THE LOCATION OF A PRINTED CIRCUIT CARD, FIND THE CARD IN THE SYSTEM.
B1714 R.M. Sec. V, Pg. 2-7	41. GIVEN THE CO-ORDINATES FOR A COMPONENT ON A PRINTED CIRCUIT CARD, FIND THE COMPONENT ON THE CARD.
B1714 T.M. Sec. V Pg. 25-33	M 42. LOCATE AND IDENTIFY ANY CONSOLE COMPONENT.
B1714 T.M. Sec. VI, Pg. 1 and Planning & Installation Manual Sec. IV, Pg. 6	M 43. VERIFY THAT THE CORRECT CARD IS LOCATED IN ANY SPECIFIED CARD LOCATION.

CARD TESTER OPERATION	
B1714 TM Sec. I	M 44. POWER UP THE B1714 SYSTEM.
Card Tester Documentation and Handout	M 45. DEMONSTRATE YOUR ABILITY TO USE THE CARD TESTER BY PERFORMING THE FOLLOWING: A. CONNECT TESTER TO THE SYSTEM. B. VERIFY SWITCH POSITIONS. C. PERFORM THE GO/NO-GO CHECK OF THE CARD TESTER D. INSERT A CARD E. APPLY POWER F. DISCONNECT PINS ON A CARD
Card Tester Documentation and Handout	M 46. PERFORM THE EXHAUSTIVE SELF-CHECK OF THE CARD TESTER.
Card Tester Documentation and Handout	M 47. USING THE CARD TESTER, PERFORM THE "GO-NO-GO" TEST ON ANY GIVEN CARD.
Card Tester Documentation and Handout	M 48. USING THE FAULT ISOLATION MODE, DISPLAY THE NODE COUNT FOR ANY GIVEN SIGNAL ON THE CARD.

PROCESSOR T & F DOCUMENTS	
B1714 Element Rules Book	49. FROM ANY LOGIC CIRCUIT WITH A GIVEN INPUT, DETERMINE THE OUTPUT.
Card Tester Documentation and Handout	M 50. USING THE CHIP CLIP, VERIFY THE OPERATION OF ANY GIVEN CHIP ON A CARD.
B1714 T & F Documents, and T.M., Sec. V Pg. 25-33	M 51. TRACE THE SIGNAL GENERATED BY ANY GIVEN CONSOLE SWITCH TO A POINT WHERE IT EXISTS ON THE BACKPLANE.
B1714 T & F Documents, and T.M. Sec. V Pg. 2-12	M 52. USING A CARD EXTENDER, DISPLAY A LOGIC SIGNAL WHICH DOES NOT APPEAR AT A BACKPLANE PIN.
B1714 T & F Documents	M 53. GIVEN ANY TERM, LOCATE A POINT ON THE BACKPLANE WHERE THIS SIGNAL MAY BE MEASURED OR OBSERVED.
B1714 Circuit List	54. GIVEN THE LOCATION OF A BACKPLANE PIN TO WHICH ONE END OF A WIRE IS CONNECTED, LOCATE THE PIN CO-ORDINATES FOR THE OTHER END OF THE WIRE.

PROCESSOR T & F DOCUMENTS	
B1714 Schematics, Circuit Lists, and T.M. Sec. V, Pg. 2-12	55. GIVEN ANY LOGIC TERM THAT APPEARS ON THE BACKPLANE, FOLLOW IT THROUGH THE SCHEMATICS EITHER TO ITS ORIGIN OR DESTINATION.
B1714 Schematics	56. VERIFY THAT ANY GIVEN SIGNAL ON A CIRCUIT CARD IS PROPERLY WIRED AS REFLECTED BY THE SCHEMATICS.
B1714 Element Rules Book	57. GIVEN ANY LOGIC CIRCUIT SYMBOL, IDENTIFY IT BY NAME AND DESCRIBE ITS FUNCTION.
Special Instructions T & F Documents (See Instructor)	M 58. IDENTIFY THE HARDWARE OPTIONS INSTALLED IN A B1714 SYSTEM.
Tektronics Tech. Manual	M 59. DISPLAY ANY SPECIFIED SIGNAL ON AN OSCILLOSCOPE AND DETERMINE THE FOLLOWING: A. AMPLITUDE B. REPITITION RATE C. PULSE WIDTH
See Instructor	60. DEMONSTRATE YOUR ABILITY TO REMOVE AND REPLACE A CHIP FROM A LOGIC CARD.

PROCESSOR T & F DOCUMENTS	
B1714 T.M. Sec. V, Pg. 89	61. DEMONSTRATE YOUR ABILITY TO REMOVE AND INSTALL A WIRE-WRAP CONNECTION.
See Instructor	62. DEMONSTRATE YOUR ABILITY TO REPAIR A BREAK IN A SOLDER RUN ON A LOGIC CARD.
See Instructor	M 63. DEMONSTRATE YOUR ABILITY TO INSTALL A RIN/LIN IN THE SYSTEM.

CARD TESTER FAULT ISOLATING	
	M
Card Tester Documentation and Handouts	64. ISOLATE A MALFUNCTION ON ANY OR ALL CARDS IN THE B1714 SYSTEM TO THE FAILING COMPONENT BY USING THE CARD TESTER.
	M
Card Test Documentation Handout	65. GIVEN A MALFUNCTION IN THE CARD TESTER, ISOLATE THE PROBLEM TO THE FAILING COMPONENT.

REGISTER CONCEPTS AND MICRO INSTRUCTIONS	
	M
B1714 T.M. Sec. VI, Pg. 3-7	66. PERFORM THE SYSTEM CONSOLE STATIC TESTS 1-15, AS SPECIFIED BY THE TECH. MANUAL.
	M
B1714 T.M. Sec. I, Pg. 12-24	67. LOAD AND EXECUTE AT LEAST ONE EXAMPLE OF EACH OF THE FOLLOWING TYPES OF MICRO INSTRUCTIONS: A. 1C REGISTER MOVE MICRO B. 7C READ/WRITE MICRO C. 9C LITERAL MOVE MICRO D. 145C CALL MICROS E. 2E CASSETTE MICRO
	M
B1714 T.M. Sec. I, Pg. 12-24	68. VERIFY THAT THE RESULTS OF THE MICROS EXECUTED IN THE PREVIOUS OBJECTIVES ARE CORRECT.
B1714 T.M. Sec. I, Pg. 12-24 Micro Worksheets	69. GIVEN A MICRO INSTRUCTION IN HEXIDECIMAL, DETERMINE THE SPECIFIC FUNCTION OF THAT INSTRUCTION.
	M
B1714 T.M. Sec. II, Pg. 135- 193	70. THROUGH USE OF THE CONSOLE SWITCHES, FORCE GOOD PARITY INTO THE FIRST TWENTY-ONE BYTES OF MEMORY.

REGISTER CONCEPTS AND MICRO INSTRUCTIONS

	M
B1714 T.M. Sec. II, Pg. 135,193	71. WRITE AND EXECUTE A MICRO PROGRAM THAT WILL FORCE GOOD PARITY THROUGHOUT MEMORY. (NOTE: THE PREVIOUS OBJECTIVE MUST BE DONE IMMEDIATELY PRIOR TO EXECUTION OF THIS OBJECTIVE).

Clear All memory

1. set X = All '0'
2. set FA = All '0'
3. set A = All '0'
4. Step Mode
5. Load 'M' = @ 7919 @ (in OCTF
6. Push Load then start & Load 8 times
7. Press clear
8. Load FA = @ 000030 @
9. select write
10. Write @ 7919 @ To Hex (in ABCD)
11. Press inc.
12. Write @ 84000 @ - @ 20FF @
13. Run Mode
14. clear & start

SYSTEM CLOCK

B1714 T.M. Sec. IV, Pg. 4-7	M 72. PERFORM THE SYSTEM CLOCK CHECKS AS SPECIFIED BY THE TECH. MAN.
T. & F Documents B1714 T.M. Sec. II, Pg. 8,9	73. DETERMINE THE DIFFERENCE BETWEEN B1712 & B1714 CLOCK.
A11	M 74. GIVEN A MALFUNCTION IN THE SYSTEM CLOCK CIRCUITRY, ISOLATE THE PROBLEM TO THE DEFECTIVE COMPONENT.

READ ONLY CASSETTE	
	M
B1714 T.M. Sec. V, Pg. 25-33 and A9490 T.M. Sec. V	75. LOCATE AND IDENTIFY ALL COMPONENTS ASSOCIATED WITH THE CASSETTE READER.
	M
A9490 T.M. Sec. IV	76. PERFORM THE CASSETTE ADJUSTMENTS AS OUTLINED IN THE TECH. MANUAL.
	M
B9490 T.M.	77. GIVEN A MALFUNCTION IN THE CASSETTE, ISOLATE THE PROBLEM TO THE FAILING COMPONENT.

MEMORY	
B1714 T.M. Sec. II, Pg. 180	78. GIVEN A SPECIFIC MEMORY ADDRESS, DETERMINE THE FOLLOWING: A. CARD GROUP B. CHIP ROW C. BYTE D. BIT
B1714 T.M. Sec. I, Pg. 8 and Sec. II, Pg. 180	M 79. DETERMINE THE SIZE OF MEMORY IN BYTES CONTAINED IN A GIVEN SYSTEM THROUGH USE OF THE CONSOLE SWITCHES.
B1714 T.M. Sec. VI, Pg. 9-12, T & F DOCUMENTS	M 80. DEMONSTRATE YOUR ABILITY TO CHANGE THE SIZE OF MEMORY IN A SYSTEM IN 4K BYTE, 8K BYTE OR 16K BYTE INCREMENTS.
B1714 T.M. Sec. IV, Pg. 8-29	M 81. VERIFY THE MEMORY TIMING ADJUSTMENTS AS OUTLINED IN THE TECH MANUAL. (NOTE: IF ADJUSTMENT SEEMS NEEDED, SEE INSTRUCTOR FIRST).
B1714 T.M. Sec. IV, Pg. 29-31	M 82. VERIFY THE MEMORY POWER SUPPLY VOLTAGE AS OUTLINED IN TM.
All	83. LOCATE THE SPECIFIC STORAGE CHIP ASSOCIATED WITH ANY GIVEN MEMORY ADDRESS ON BOTH STYLES OF MEMORY CARDS.

MEMORY	
All	84. GIVEN AN S-MEMORY TEST FAILURE CODE, DEFINE THE FOLLOWING: A. FAILING FUNCTION. B. LOCATION OF FAILING ROUTINE IN THE LISTING. C. CONTENTS OF REGISTERS USED IN FAILING ROUTINE. D. FAILING ADDRESS.
All	M 85. GIVEN A MALFUNCTION IN S-MEMORY ISOLATE THE PROBLEM TO THE FAILING COMPONENT.

POWER	
B1714 T.M. Sec. IV, Pg. 29-31	M 86. PERFORM THE MEMORY POWER SUPPLY ADJUSTMENTS AS OUTLINED IN THE TECH. MANUAL.
B1714 T.M. Sec. V, Pg. 42-67	M 87. LOCATE AND IDENTIFY ALL POWER SUPPLIES, FUSES AND CIRCUIT BREAKERS ON THE SYSTEM.
B1714 T.M. Sec. V, Pg. 42-67	M 88. LOCATE ALL POWER SUPPLY CONNECTIONS WHICH SUPPLY VOLTAGES TO THE BACKPLANES.
B1714 T.M. Sec. IV, Pg. 14-19	M 89. PERFORM ALL ADJUSTMENTS OF THE LOGIC POWER SUPPLY AS OUTLINED IN THE TECH. MANUAL.
All	M 90. GIVEN A MALFUNCTION IN THE POWER SUB-SYSTEM ISOLATE THE PROBLEM TO THE FAILING COMPONENT.

INSTALLATION	
B1700 Planning & Install. Man Pg. 1-15	91. DETERMINE THE BTU REQUIREMENTS FOR ANY GIVEN SYSTEM.
B1700 Planning & Install. Man. Pg. 1-18	92. DETERMINE THE KVA REQUIREMENTS FOR ANY GIVEN SYSTEM.
B1700 Planning & Install. Man. Pg. 1-30	93. DETERMINE WHICH BURROUGHS FORMS ARE REQUIRED AT A GIVEN B1700 SITE.
B1700 Planning & Install. Man. Pg. 1-31	94. DETERMINE THE STANDARD TEST EQUIPMENT REQUIRED FOR A B1700 INSTALLATION.
B1700 Planning & Install. Man. Pg. 1-31	95. DETERMINE THE SPECIAL TOOLS REQUIRED FOR A GIVEN B1700 SITE.
B1700 Planning & Install. Man. Pg. IV-6 thru 17	96. BE ABLE TO PERFORM ALL 27 STEPS OF THE B1700 INSTALLATION PROCEDURE.

LAB WORKSHEET DOCUMENTATION OBJECTIVES

1. Locate the signal TWS...DO in the schematics. What is the backplane pin it exits? PIN _____ TO _____

2. Trace the signal to its destination point. Pin _____

3. Verify that the system is powered off and using a multimeter verify that a wire exists between the two points on the backplane. Pin _____ to Pin _____. Use backplane wire list.

4. Find the signal on the card of destination and note that passing through an element it changes names on this card. Name changed to _____.

5. Using the new signal name look the signal up in the card circuit list for that card. List the pins that the signal goes to on this card.

6. Remove the card from the system and using a multimeter verify a wire between the pins listed in #5.

7. Trace the signal that is needed to produce TWS....H1. Look up the ~~RFAN~~ FFAN in the Hardware Rules Book to determine its function.

8. It is noted that the signal MARCD1H1 comes into Pin F of the ~~RFAN~~ FFAN. Trace this signal to its origin in the schematics. Card _____ page _____ of _____.

9. It is noted that MARCD1H1 is developed by a DFAN with inputs MARCM1FO and MARCMOFO. Determine the status of these two signals, if MARCD1H1 is to be true. MARCM1FO must be _____ MARCMOFO must be _____. Use the hardware rules book to determine.

10. It is known that MARCM1FO and MARCMOFO are developed on the F card. Locate this in the schematics.

11. Determine what must be true for the EFAN which develops MARCM1FO and MARCMOFO to develop both signals true. Pin _____ must be _____. Use the Hardware Rules to determine the operation of the EFAN.

12. It is determined that this EFAN is bad and you wish to order another, the part number is _____.

SOFTWARE QUIZ

1. What interpreter is required to run the MCP?

   A. COBOL
   B. RPG
   C. SDL
   D. UPL

2. What interpreter is provided to run the COBOL Compiler?

   A. COBOL
   B. RPG
   C. SDL
   D. UPL

3. What routine (Micro Coded) performs all I/O operations in the system?

   A. CSM
   B. SYSTEM/INIT
   C. MCP
   D. SDL/INTERP.

4. The function of the Clear/Start routine is to:

   A. Clear all registers so a cold start may be performed.
   B. Clear all peripheral devices.
   C. Load the MCP and its interpreter in order to restore the system to an operable state.
   D. None of the above.

5. What SPO message would be used to discontinue a job and release the peripheral devices?

   A. DC
   B. DS
   C. RM
   D. WT

6. What SPO message would be used to obtain a printout on the line printer of all files on disk.

   A. KA
   B. KP
   C. PD
   D. PM

7. When a user pack is loaded, what SPO message is required to notify the MCP the unit is ready?

   A. IL
   B. OL
   C. RL
   D. RY

SOFTWARE QUIZ

8. Before a removable disk cartridge is removed from the unit:

   A. KA should be performed
   B. Disk should be purged
   C. PO message should be entered
   D. Nothing special required.

9. The total amount of processor time a program has been running may be obtained by:

   A. TI
   B. TR
   C. WT
   D. Subtracting EOJ time from BOJ time.

10. What utility should be used on a new disk cartridge to make it ready for use on the system?

   A. Disk Initializer
   B. MIL Disk
   C. I/O Debug
   D. Disk/Copy

11. What utility is used to copy one disk to another?

   A. Disk/Copy
   B. Disk/Dump
   C. DMPALL
   D. File/Loader

12. What program converts Source Code to Object Code?

   A. Compiler
   B. Interpreter
   C. MCP
   D. Converter

13. In order for the system to keep a log of all jobs run, what must be done?

   A. Nothing special - system does this automatically
   B. Charge option must be set
   C. Log option must be set
   D. System will not perform this function

14. A Control Card may be distinguished by:

   A. An Asterisk (*) in column one
   B. A Hyphen (-) in column one
   C. A Question Mark (?) in column one
   D. By fact it is first card in deck

SOFTWARE QUIZ

15. A file is named by:

    A. Either one name of 10 Characters or two names divided by a Hyphen.
    B. One name only of 10 Characters.
    C. Files are not named but given numbers
    D. Either one name of up the 10 Characters or two names divided by a slash, each of which may be up to 10 Characters.

16. The table on disk which contains a list of all permanent files on that disk is called:

    A. Directory
    B. Name Table
    C. Master Available Table
    D. Cold Start Variables

17. What program is called by the SORT program when an "in place" sort has been specified?

    A. No other program is called
    B. SORT/QSORT 3-20
    C. SORT/VSORT
    D. SORT/COMPILER

18. What SPO message is used to obtain a printout of the file SYSTEM/DUMPFILE?

    A. DM
    B. DP
    C. KA
    D. PM 2-96

19. Briefly define the following terms:

    A. File
    B. Record
    C. Blocking Factor

20. Briefly outline the procedure to perform an "MCP DUMP". 2-6

    Dump offon must be set, PM

BASIC PROCESSOR QUIZ

1. What is the basic word length of the B1700 processor?

   A. 4
   B. 8
   C. 16
   D. 24

2. What is the word length of B1700 memory?

   A. 8
   B. 16
   C. 32
   D. 64

3. How long is a micro instruction word?

   A. 4
   B. 8
   C. 16
   D. 32

4. On what card is the X register located?

   A. A
   B. B
   C. A and B
   D. None of the above

5. When a local memory register is specified as sink, where is MEX data temporarily stored prior to being written?

   A. TEMPB
   B. LBUF
   C. MIR
   D. MAR (A)

6. What is the first location of BDATA referred to as?

   A. X
   B. Y
   C. T
   D. L

7. In what bit of the C register would a carry or borrow be stored?

   A. BICN (0)
   B. MSBX
   C. LSUX
   D. CYF

BASIC PROCESSOR QUIZ

8. What is the function of the 3 LSB of the MAR?

   A. Not used
   B. Bit address
   C. BYTE address
   D. Selects storage card

9. During a micro fetch, what register accepts the memory data?

   A. U Reg
   B. ML Reg
   C. MIR
   D. CMND

10. To see if an interrupt has occurred, what bit could be tested?

    A. CPU (1)
    B. CC (3)
    C. XXST (2)
    D. CD (0)

11. What registers are used for storage of Data when reading/writing memory?

    A. BR, LR, X, T
    B. FA, FB, CP
    C. X and Y only
    D. X, Y, T and L

12. Which micros could be classified as "branch relative" type micros?

    A. 4C, 5C, 123C, 145C
    B. 6D and 3E
    C. 3F and 1C
    D. 3C, 7D and 8D

13. What is the destination register in the micro 18A2?

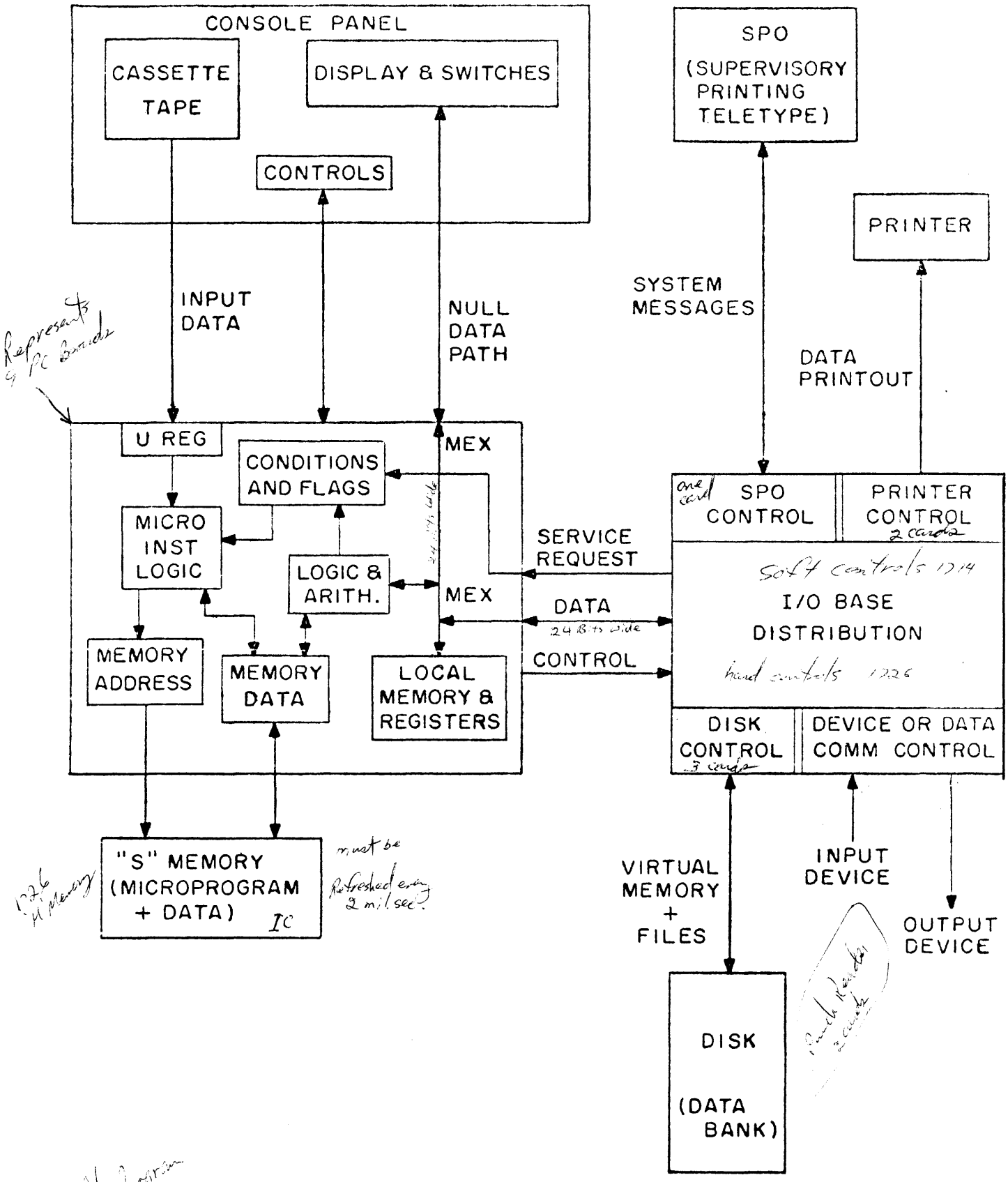
    A. X
    B. Y
    C. L
    D. None of the above

14. When performing a 7C micro, what register must be loaded with the memory address to be read/written?

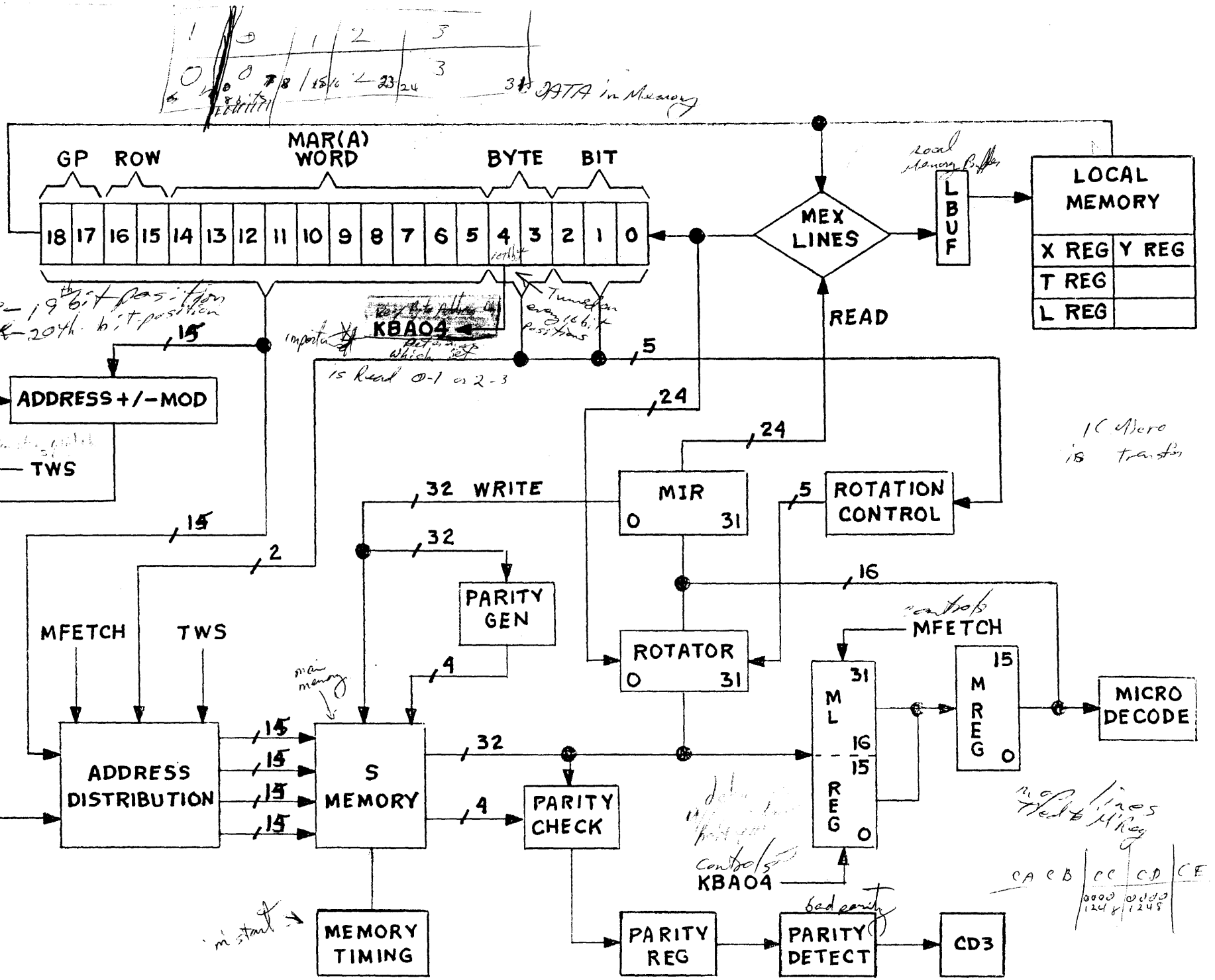
    A. MAR (A)
    B. FA
    C. BR
    D. MIR

BASIC PROCESSOR QUIZ

15. X = 795436 Y = 207258 CP = 84
What is the HEX Bit pattern that would be displayed when selecting REG GRP 0 and Select 3?



SIMPLIFIED SYSTEM BLOCK DIAGRAM

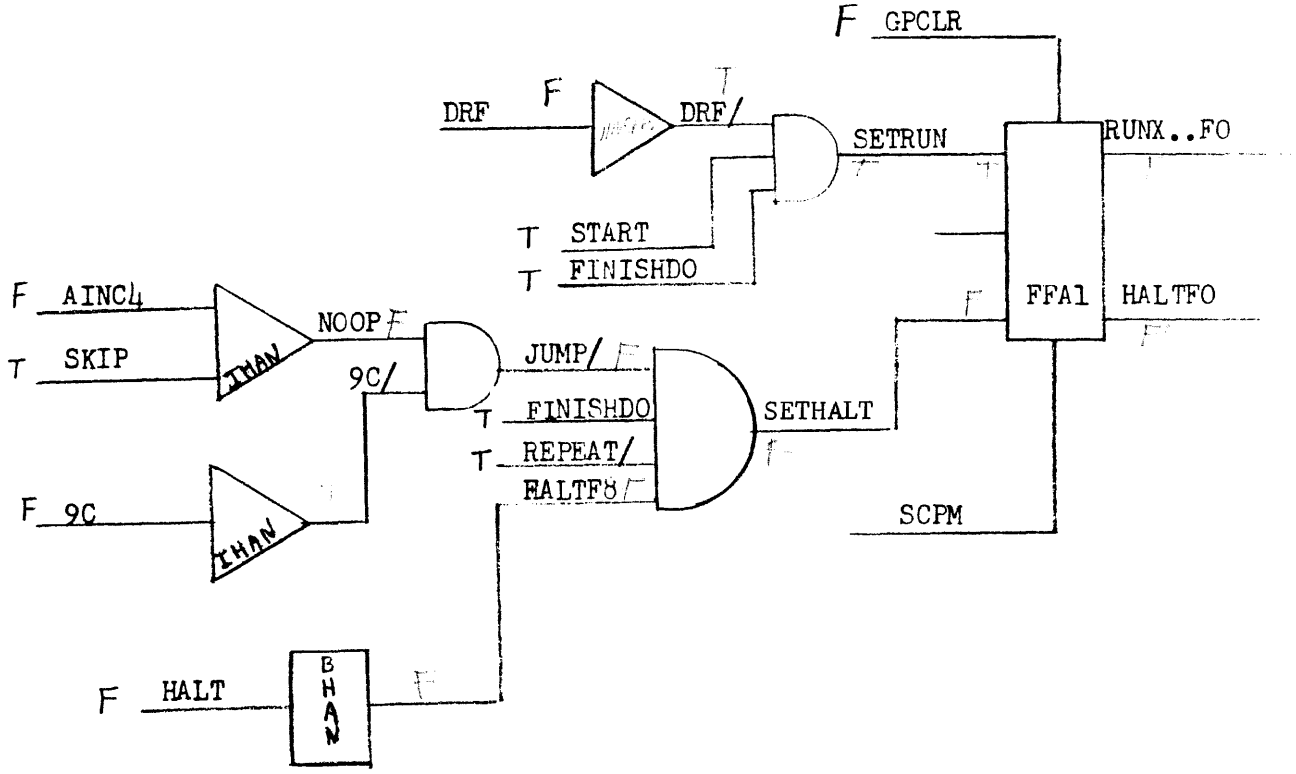


S-/MEMORY FUNCTIONAL BLOCK DIAGRAM

WORKSHEET GATES, INVERTERS, BUFFERS

AND FLIP-FLOPS

(CARD F SH 4 OF 6)



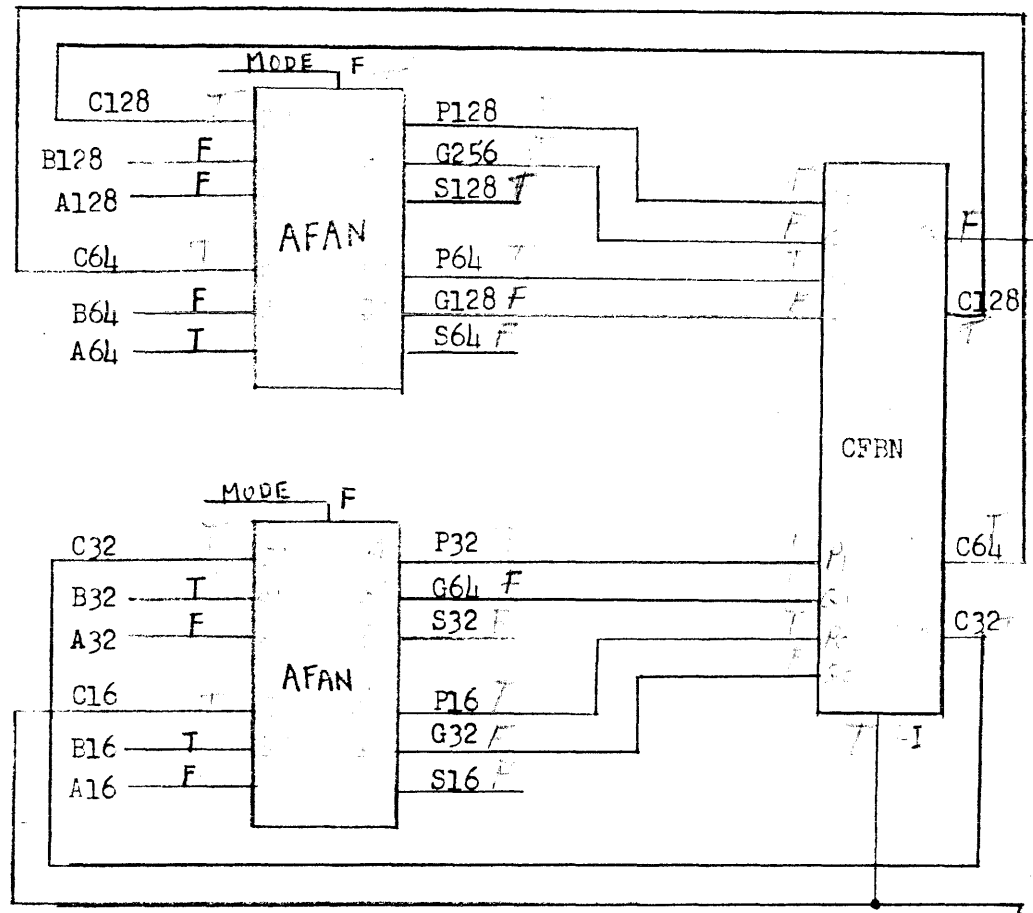
1.

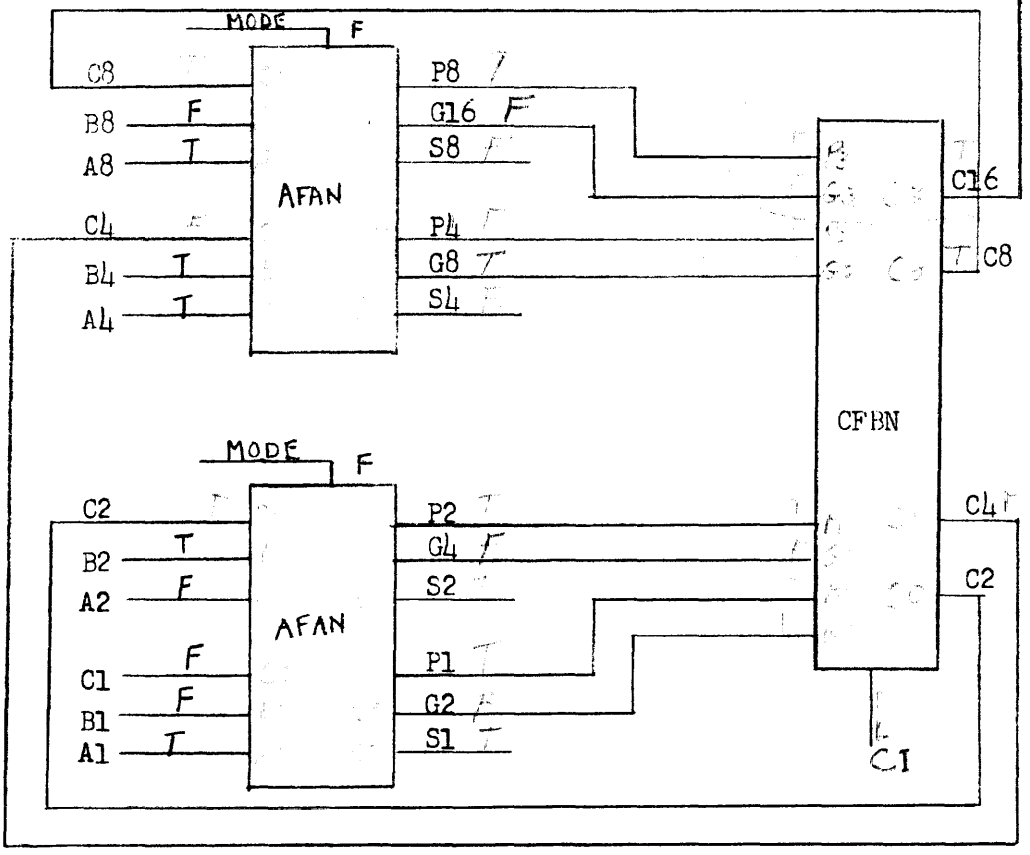
TERM	T OR F
NOOP	F
9C/	T
HALTF8	F
DRF/	T
SETRUN	T
RUNX..FO	T

*AFTER CLOCK

2. HOW WOULD THE TERM GPCLR GOING TRUE EFFECT THE TERMS RUNX..FO AND HALTFO?

8 BIT ADDER WORKSHEET

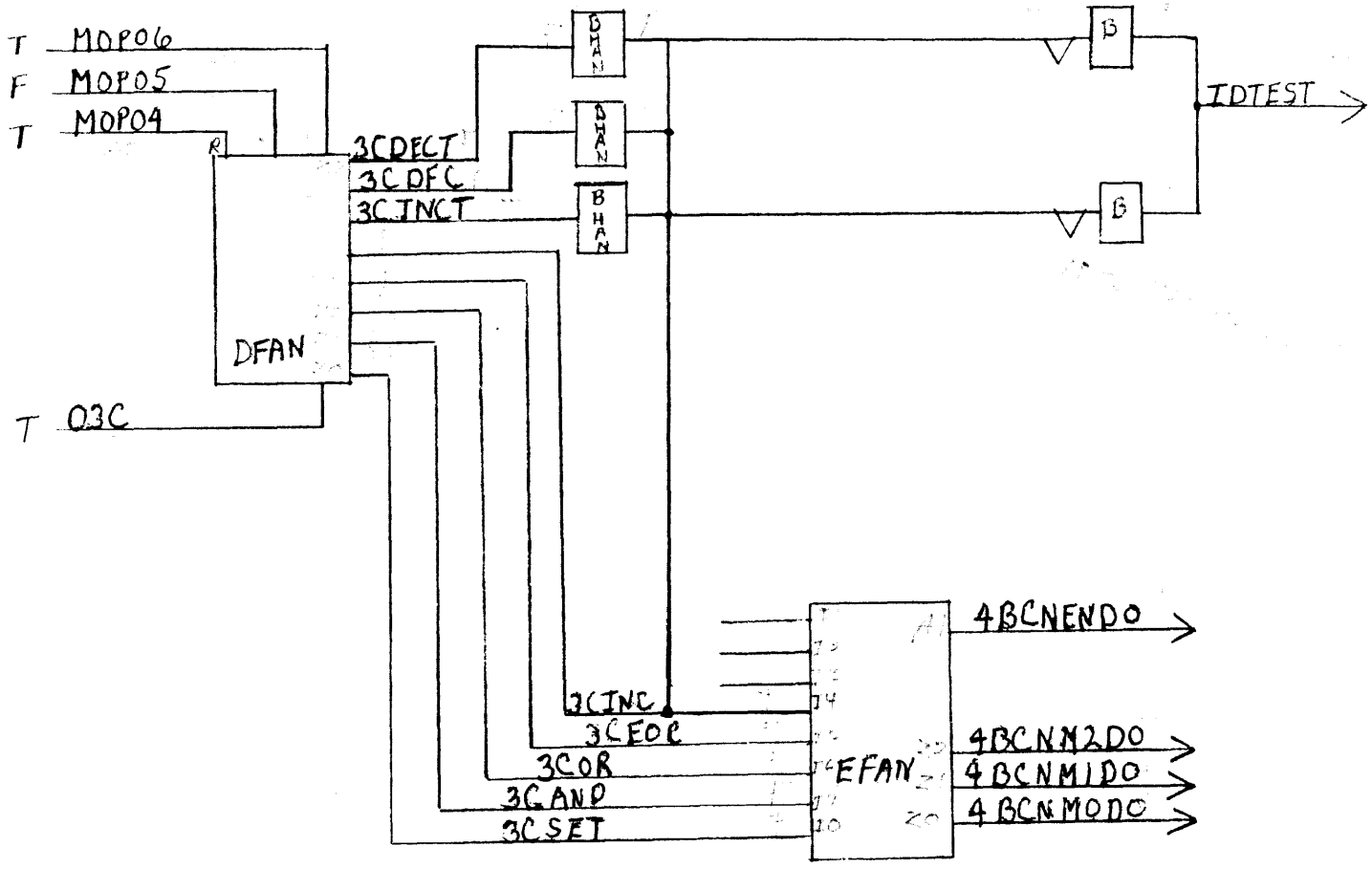




TERM	T OR F
S1	T
S2	T
S16	T
S128	F
P1	T
P2	T
P4	F
G8	T
G16	F
C4	F
C8	T
C128	F
CYL	T

COMPLETE ABOVE TABLE USING T OR F

ELEMENT RULES WORKSHEET DFAN'S AND EFAN'S
CARD D SH 1 OF 6



GIVEN THE INPUTS AS NOTED, LABEL THE LOGIC STATE OF THE OUTPUT TERMS WITH A T OR F.

1. IDTEST _____
2. 4BCNENDO _____
3. 4BCNM2DO _____
4. 4BCNM1DO _____
5. 4BCNM0DO _____

6. Describe the meaning of the triangles on the input of the buffers which make the term IDTEST.

MICRO INSTRUCTION WORKSHEET 1

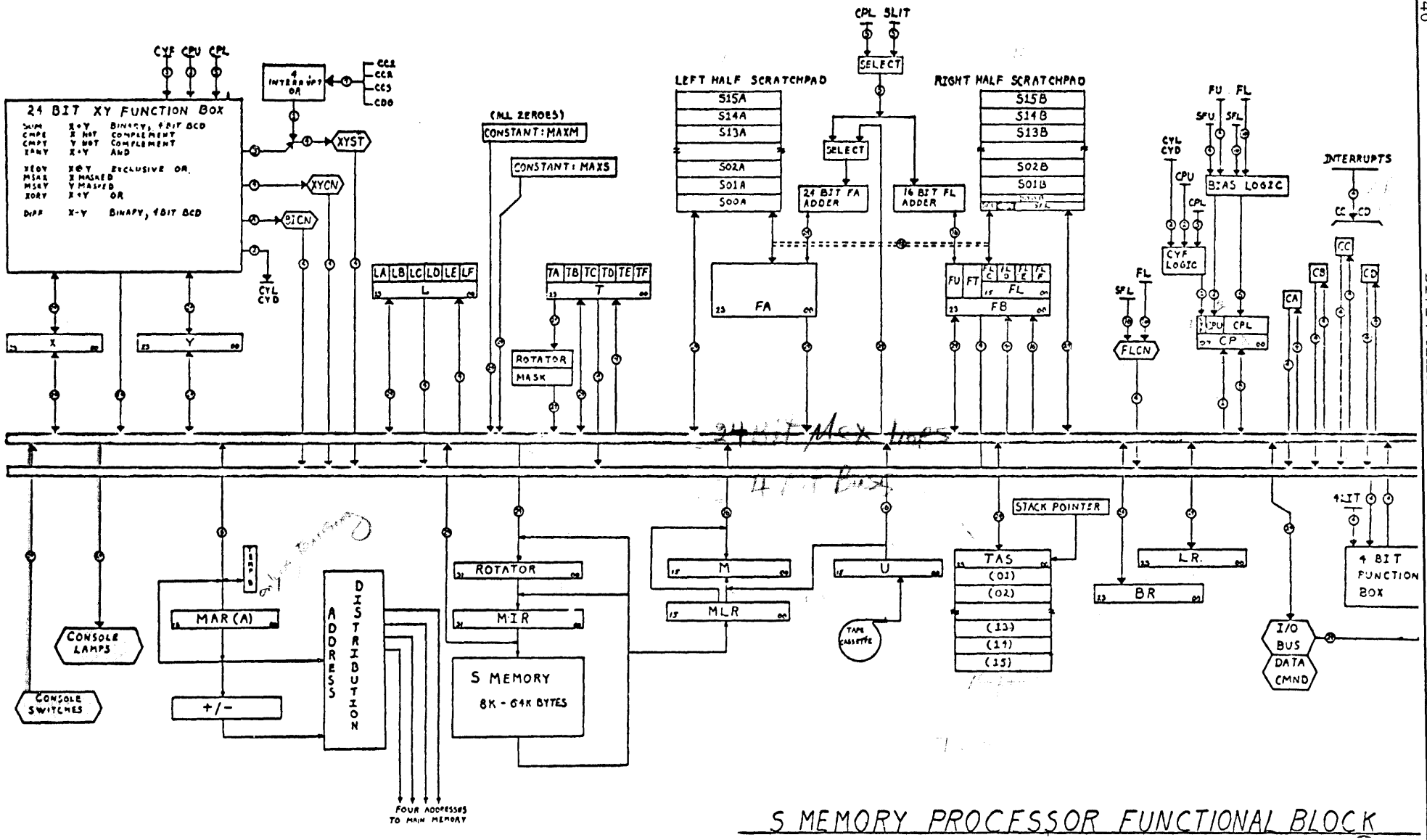
MICRO IN HEX	MICRO NAME	REGISTER	BEFORE EXECUTION	AFTER EXECUTION
18A0		FA X Y	123456 ABCDEF 098765	
10E1		CPL X Y	18 123456 876543	
12BE		Y T CMND	56789A 100005 000000	
7998		A FA T X MEMORY 0001C0 MEMORY 008000	0001C0 008000 FEDCBA ABCDEF 7998B0 000000	
70D8		FA T L MEMCRY 000000	000000 ABCDEF 234567 AFAFAF	

MICRO INSTRUCTION WORKSHEET 2

MICRO IN HEX	MICRO NAME	REGISTERS	BEFORE EXECUTION	AFTER EXECUTION
9000 0100		Y X	000200 000300	
8306		T L	ABCDEF 123456	
E003		A TAS	000100 003450	
F009		A TAS	003450 000100	
C002		A	000000	
0022		X Y	123456 123456	
0000		FA X	AAAAAA FFFFFF	
0001		FA A	000100 000010	
0700		FA SPAD(0) LEFT SPAD(0) RIGHT FB	000000 555555 AAAAAA FFFFFF	

TRAINING SUPPLEMENT

TABLE OF CONTENTS



S MEMORY PROCESSOR FUNCTIONAL BLOCK

TRAINING SUPPLEMENT

MICRO WORKSHEET

NAME _____

MICRO	DESCRIPTION	REGISTERS	BEFORE	AFTER	REMARKS
#1		FA	123456		
18A0		X	ABCDEF		
		Y	098765		
#2		CPL	18		
10E1		X	123456		
		Y	876543		
#3					
2881		FA	FFFFFF		
		SPAD(1) LEFT	AAAAAA		
		SPAD (1) RIGHT	BBBBBB		
#4					
21A1		SPAD(0) LEFT	ABCDEF		
		SPAD(1) LEFT	123456		
		FA	654321		
		Y	F1F2F3		
#5					
3928		L	000000		
		X	FFFFFF		
#6					
4C61		A	000050		
		L	999999		
		T	000000		
#7					
5B01		A	000100		
		L	666666		
		T	999999		

TRAINING SUPPLEMENT

MICRO WORKSHEET

MICRO	DESCRIPTION	REGISTERS	BEFORE	AFTER	REMARKS
#8					
6125		A	000100		
		L	555555		
		T	999999		
#9					
7998		A	000100		
		FA	008000		
		T	FEDCBA		
		X	ABCDEF		
		Memory	000100 = 7998D0		
		Memory	008000 = 000000		
#10					
8306		T	ABCDEF		
		L	123456		
#11					
9000		Y	000200		
0100		X	000300		
#12		CPL	18		
A180		T	555555		
		Y	999999		
		X	123456		
#13					
BC47		X	ABCDEF		
		T	665544		
#14					
C002		A	000000		

TRAINING SUPPLEMENT

MICRO WORKSHEET

MICRO	DESCRIPTION	REGISTERS	BEFORE	AFTER	REMARKS
#15					
D00A		A	000090		
#16					
E003		A	000100		
		TAS	003450		
#17					
F009		A	003450		
		TAS	000100		
#18					
0404		Y	123456		
		X	654321		
#19					
0501		Y	123456		
		X	654321		
#20					
06C0		CP	10		
		FL	0020		
		FA	000010		
#21					
0700		FA	000000		
		SPAD(0)LEFT	5A5A5A		
		SPAD(0)RIGHT	A5A5A5		
		FB	FFFFFF		
#22					
0800		FA	0000A0		
		SPAD(0)LEFT	000060		
		SPAD(0)RIGHT	000000		

TRAINING SUPPLEMENT

MICRO WORKSHEET

MICRO	DESCRIPTION	REGISTERS	BEFORE	AFTER	REMARKS
#23					
0998		ALL REG'S EQUAL ZEROS			
#24					
0022		X	123456		
		Y	123456		
#25		FL	0019		
		SPAD(O)RIGHT	000020		
		CPL	10		
		CPU	1		

TRAINING SUPPLEMENT

MICRO PROGRAM

NAME _____

Assume initial register conditions as follows:

X = F1F2F3
CP = 18
FA = 008000
Y = 009000
All others = zero

MICRO	S-MEMORY ADDRESS	RESULTS
3F00	00000	
781A	00010	
6F60	00020	
C001	00030	
0001	00040	
7098	00050	
6F68	00060	
C001	00070	
0001	00080	
0638	00090	
18A0	000A0	
4CA1	000B0	
D00D	000C0	
4E04	000D0	
97AA	000E0	
AAAA	000F0	
0001	00100	

What is the overall function of this program?

Burroughs Corporation
BUSINESS MACHINES GROUP
PASADENA PLANT

CIRCU LIST

CODE 72278AEAD

CIRCUIT NUMBER	LINE NO.	FROM LOCATION	Z	TO LOCATION	Z	GROUP	PIVOT OR SHIELD PINS		FROM TO ELEM TYPE	FT CD	WIRE TYPE	LENGTH	CABLE NAME SPEC. NUMBER	CONTROL
20003353360	01													
CSTPG.DO	02	PU		PU										
	03	+ XB3I	1	YA0Q	1	1	XA1J		BHANBHAN	3		9.6		11 23 23 RR 4
	04											9.6>		
20003354330	05													
MIC.3EF0	06	PU		PU										
	07	XA3X	2	+ XB7P	2	1	XA4Q		DFANBHAN	36		4.2		11 23 23 RR 4
	08	+ XB7P	1	XB4F	1	1	XB5N		BHANBHAN	63		2.4		11 23 23 RR 4
	09											6.6>		
20003367960	10													
MOPQ8BTO	11	PU		PU										
	12	+ XA0V	1	+ XA3V	1	1			BGLNXXXX	3		0.6		11 23 23 RR 4
	13	+ XA3V	2	XB3V	2	1			XXXXDFAN	33		1.8		11 23 23 RR 4
	14	XB3V	1	XB6V	1	1			DFANIHAN	36		0.6		11 23 23 RR 4
	15											3.0>		
20003375600	16													
MASKSTCO	17	PU		PU										
	18	+ YA4A	2	YB4A	2	1			EFANEFAN	33		1.8		11 23 23 RR 4
	19	YB4A	1	YB7C	1	1	YB5B		EFANGFEN	36		1.0		11 23 23 RR 4
	20	YB7C	2	YC4A	2	1	YB8B		GFENBGLN	63		1.6		11 23 23 RR 4
	21											4.4>		
20003377400	22													
DATASTCO	23	PU		PU										
	24	+ YA3A	1	YB4B	1	1	BA4C	BB3C	EFANGFJN	33		3.0		11 23 23 RR 4
	25	YB4B	2	YC3A	2	1	BB5D	BC2D	GFJNBGLN	33		2.2		11 23 23 RR 4
	26											5.2>		
20004305160	27													
PE3...E0	28	PU		PU										
	29	+ YA0L	2	YB6M	2	1	YA1N	YB5N	FFANBHAN	6		3.6		11 23 23 RR 4
	30											3.6>		

CIRCUIT LIST NO.	SYSTEM NAME	UNIT NAME	UNIT NUMBER	FILE	CIRCUIT INDEX	PAGE NO.	REV.
T 2205 1767	B1500	PROCESSOR-MEMORY UNIT	2205 0967	620	20003353360	25.000	AE

Burroughs Corporation
BUSINESS MACHINES GROUP
PASADENA PLANT

CIRCUIT LIST

CODE 72237AF

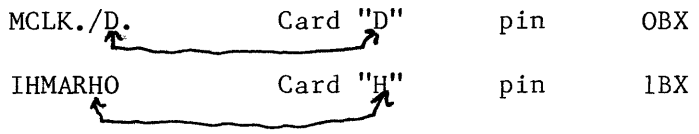
CIRCUIT NUMBER	LINE NO.	FROM LOCATION	Z	TO LOCATION	Z	GROUP	PIVOT OR SHIELD PINS	FROM ELEM TYPE	TO ELEM TYPE	FT CD	WIRE TYPE	WIRE LENGTH	CABLE NAME / SPEC. NUMBER	CONTROL
CSAGPFD0	01													
0	02	WB		WB										
	03	FBEP	2	GIRC	2	1	GIPA	0EYG2 F				8.5		11 23 23 RR 4
	04											8.5>		
CSAPADA1	05													
0	06	WB		WB										
	07	ELCC	1	GLCC	1	1	ELIE	GLIA	I0 BG0 B			2.2		11 23 23 RR 4
	08	GLCC	2	GLLC	2	1	GLEC	GLIC	G0 B SIY			0.4		11 23 23 RR 4
	09	GLLC	1	JLCC	1	1		JLIA	SIYE0 B			2.8		11 23 23 RR 4
	10	JLCC	2	HJEA	2	1	JLGA	HLGC	E0 BG2 P			4.2		11 23 23 RR 4
	11											9.6>		
CSAPADD0	12													
0	13	WB		WB										
	14	GBEP	2	GJEC	2	1	GBGE		0AYG2 A			9.4		11 23 23 RR 4
	15											9.4>		
CSBGRPA1	16													
0	17	WB		WB										
	18	FLLP	1	FKAC	1	1	FLIE		SKYH1 B			2.2		11 23 23 RR 4
	19	FKAC	2	HIMA	2	1	FJIE	GJGP	H1 BG2 S			3.1		11 23 23 RR 4
	20	HIMA	1	IKAC	1	1	IIPA		G2 SF1 B			2.5		11 23 23 RR 4
	21	IKAC	2	KKAC	2	1	IHIE	KHIA	F1 BD1 B			7.4		11 23 23 RR 4
	22	KKAC	1	LLLE	1	1		KLIE	D1 BSYX			2.5		11 23 23 RR 4
	23											17.7>		
CSBGRPT0	24													
0	25	WB		WB										
	26	FBEG	2	GIMC	2	1	GBGA		0GYG2 R			8.7		11 23 23 RR 4
	27											8.7>		

CIRCUIT LIST NO.	SYSTEM NAME	UNIT NAME	UNIT NUMBER	FILE	CIRCUIT INDEX	PAGE NO.	REV
T 2203 9358	B710	WB-1501 PROC CD A -AH	2200 3149	999	CSAGPFD0	66.000	AF

TRAINING SUPPLEMENT

CONTINUOUS EXECUTION OF ONE MICRO

Load M Register with desired micro, then jumper the following signals true on processor backplane:



TRAINING SUPPLEMENT

USE OF MONITOR MICRO

The 9D Monitor micro may be monitored with test equipment when it is executed. The Monitor micro is useful when the use of backplane jumpers prove to be insufficient for continuous execution of one micro. An example of the use of the Monitor micro in cycling a Normalize X micro is shown below. (Cycling the Normalize X would not be sufficient because of the fact that the source data would change.)

ADDR	MICRO	DESCRIPTION
00000	90EF	Initialize X
00010	FFFF	
00020	8A18	Initialize FL
00030	8C18	Initialize CPL
00040	0900	Monitor
00050	0003	Normalize X
00060	D007	Cycle

OSCILLOSCOPE

Set up to sync external negative on signal at $HX on card "F". The beginning of the oscilloscope trace will be there at the same time as the beginning of the Normalize X micro.

TRAINING SUPPLEMENT

B1714 PROC DYN LOADER

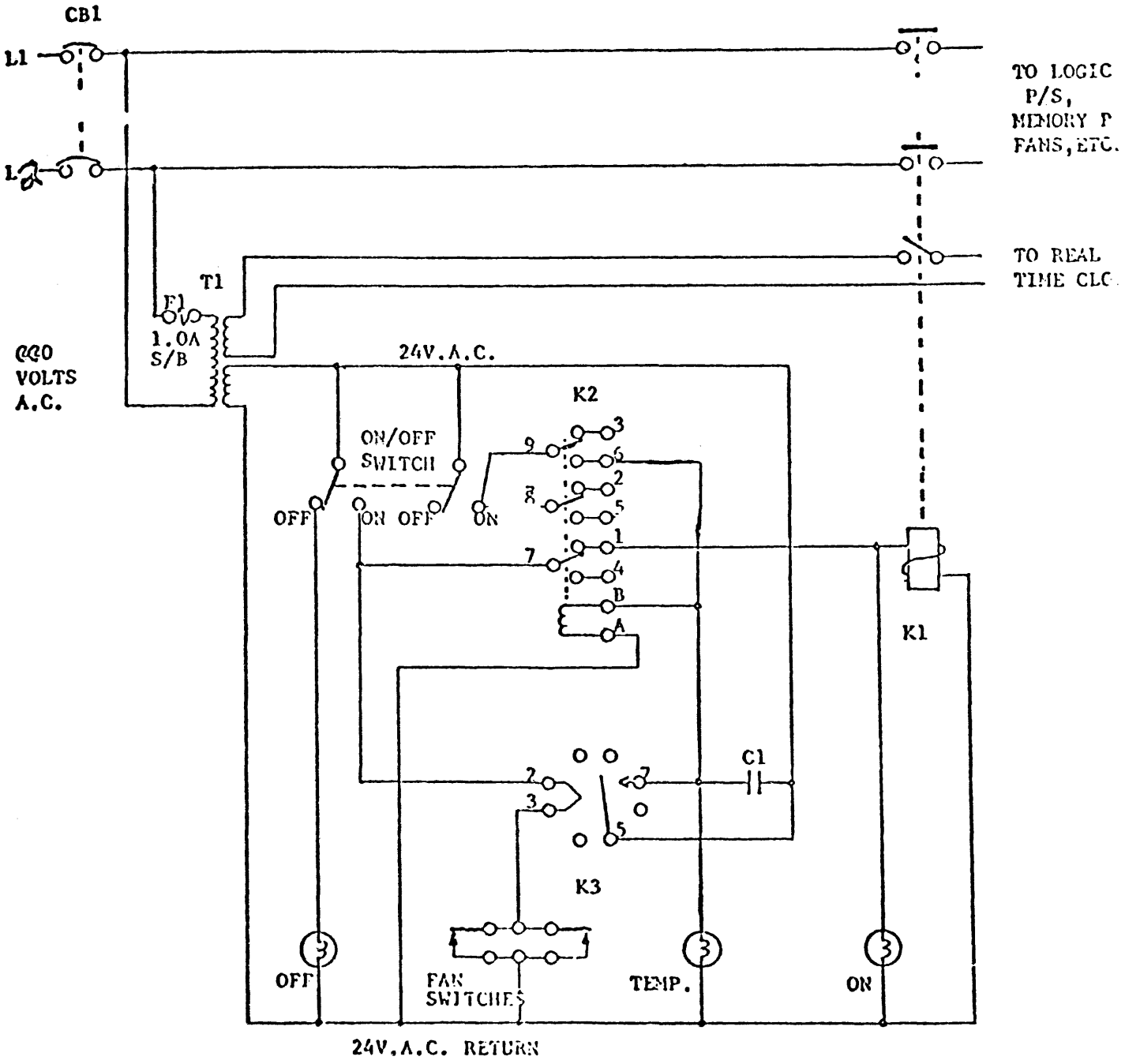
ADDRESS	MICRO	DESCRIPTION
0	9800	24 Bit Lit (4096) to FA
10	1000	
20	0000	NOP
30	9000	24 Bit Lit (32768) to X
40	8000	
50	79D9	Write 25 Bits from L Inc FA
60	18A1	Move FA to Y
70	5C93	If X>Y to Addr 50
80	9800	24 Bit Lit (4096) to FA
90	1000	
A0	0020	Cassette Start
B0	1BE3	Move U to L
C0	79D0	Write 16 bits from L Inc FA
D0	6A29	Skip when LC = 9
E0	C003	Go to Addr 120
F0	1BE3	Move U to L
100	79D0	Write 16 bits from L Inc FA
110	D007	Go to Addr B0
120	6D22	Skip when LF = 2
130	D009	Go to Addr B0
140	6C22	Skip when LE = 2
150	D00B	Go to Addr B0
160	6B20	Skip when LD = 0

TRAINING SUPPLEMENT

B1714 PROC DYN LOADER

ADDRESS	MICRO	DESCRIPTION
170	D00D	Go to Addr B0
180	GA20	Skip when LC = 0
190	D00F	Go to Addr B0
1A0	0022	Cassette Stop
1B0	860A	Move 10 to BR
1C0	0000	NOP
1D0	9400	24 Bit Lit (4096) to A
1E0	1000	(All sections start @ 1000)
1F0	0000	NOP

TRAINING SUPPLEMENT



24 VOLT A.C. CONTROL.

TRAINING SUPPLEMENT

USE OF THE LOGIC POWER SUPPLY DUMMY LOAD

REFER TO FIGURE 1.

Correct functioning of the Logic Power Supply requires that it be presented with a load drawing at least 25 Amps. A dummy load is available to allow operation of the power supply when extended on its slides and disconnected from the backplane load. Use of the dummy load will assist in isolation of a logic power problem to either the mainframe or the power supply and will allow the field engineer to work on the supply in a power-up situation.

The dummy load may be connected in one of two ways---

1. With load from +4.75V to Ground, -2.0V shorted to ground.
2. With load from +4.75V to Ground, -2.0V open.

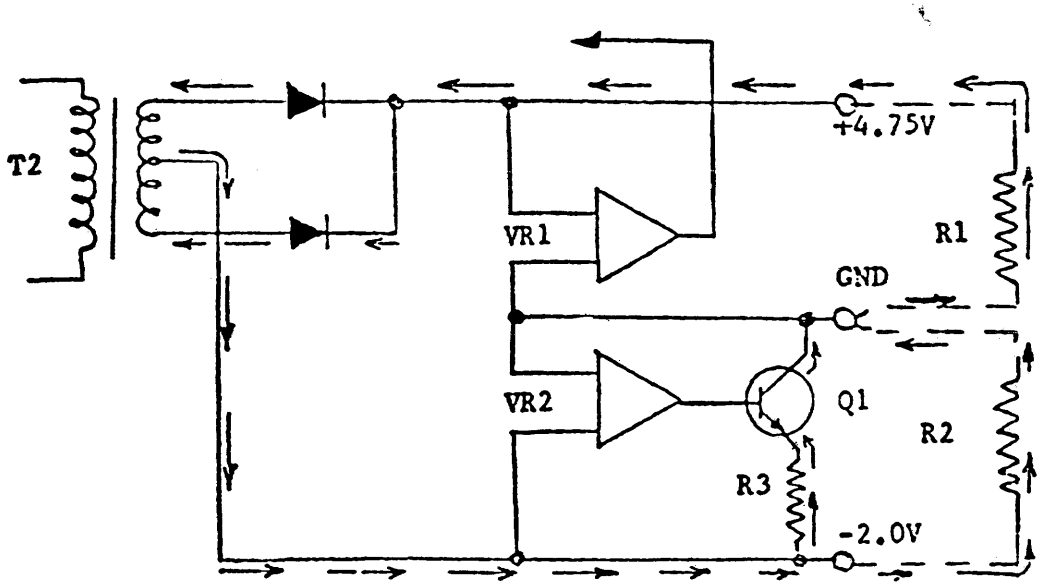


FIGURE 1. Simplified diamgram showing Logic Voltage Current Flow Paths.

The transformer T2 may be considered as a variable voltage current source for the +4.75V and -2.0V loads. All current drawn by the +4.75V load (R1) will return through the -2.0V load (R2) and/or the shunt resistors (R3) and Transistors (Q1). Voltage regulator VR1 will adjust the output of the

TRAINING SUPPLEMENT

THE DUMMY LOAD (CONT.)

Inverter to T2 so that +4.75V is always maintained between +4.75V and Ground. V2 will control Q1 and thus the current flow through R3 so that the voltage drop across the parallel resistances Q1 - R3 and R2 is maintained at 2.0V.

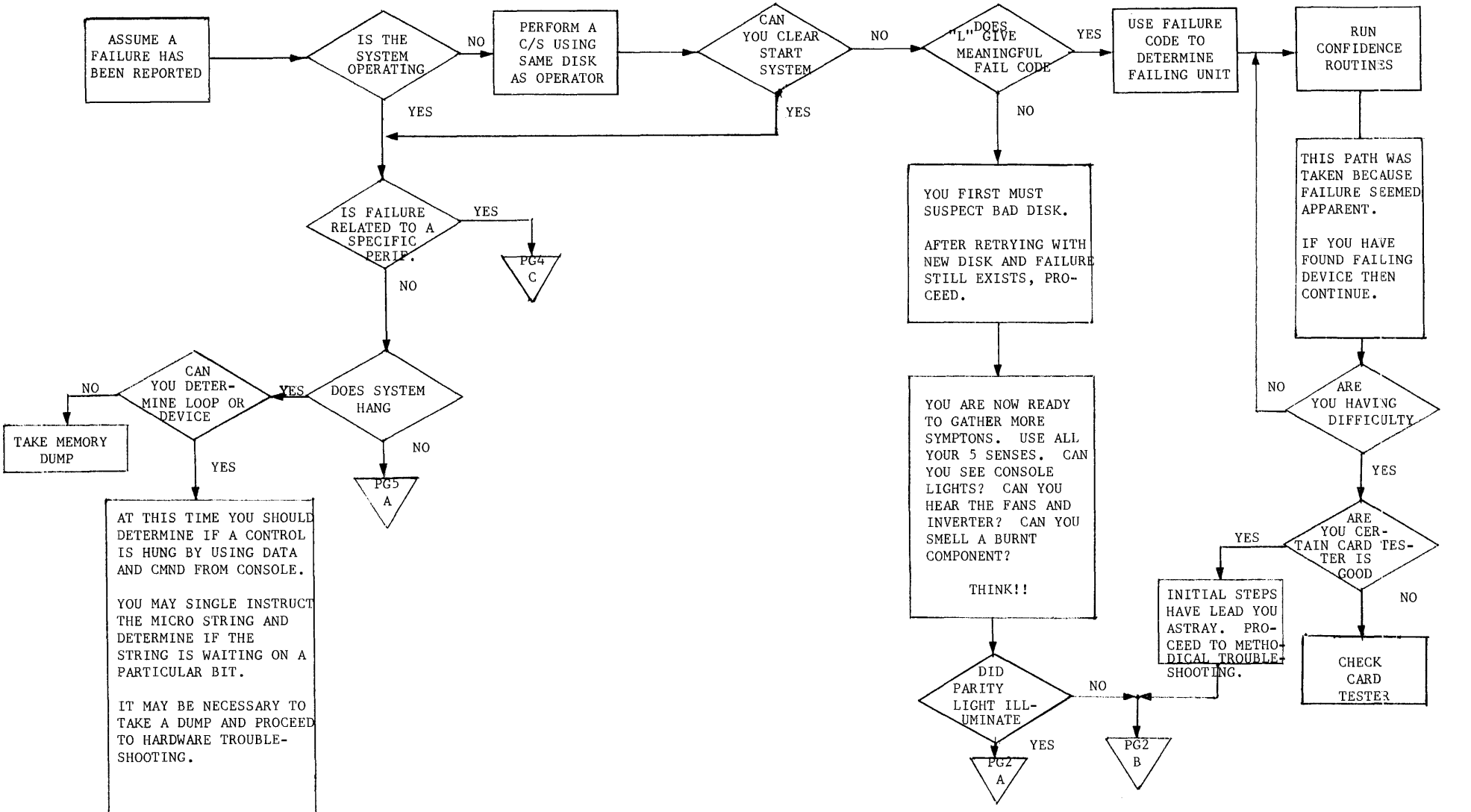
When troubleshooting the power supply, the shorting bar on the dummy load will normally be used to short circuit the Ground and -2.0V terminals. This will eliminate the -2.0V shunt circuit but allow the rest of the power supply to operate normally. The VCO will run at a reduced rate as the inverter is required to maintain a voltage drop of only 4.75V between the +4.75V and -2.0V terminals, instead of the normal 6.75V.

If it is required to troubleshoot the -2.0V shunt circuits, the dummy load will be connected without short circuiting the Ground and -2.0V terminals. This will cause all the current drawn by the dummy load (approx. 95 amps) to flow through the shunt circuit Q1 - R3.

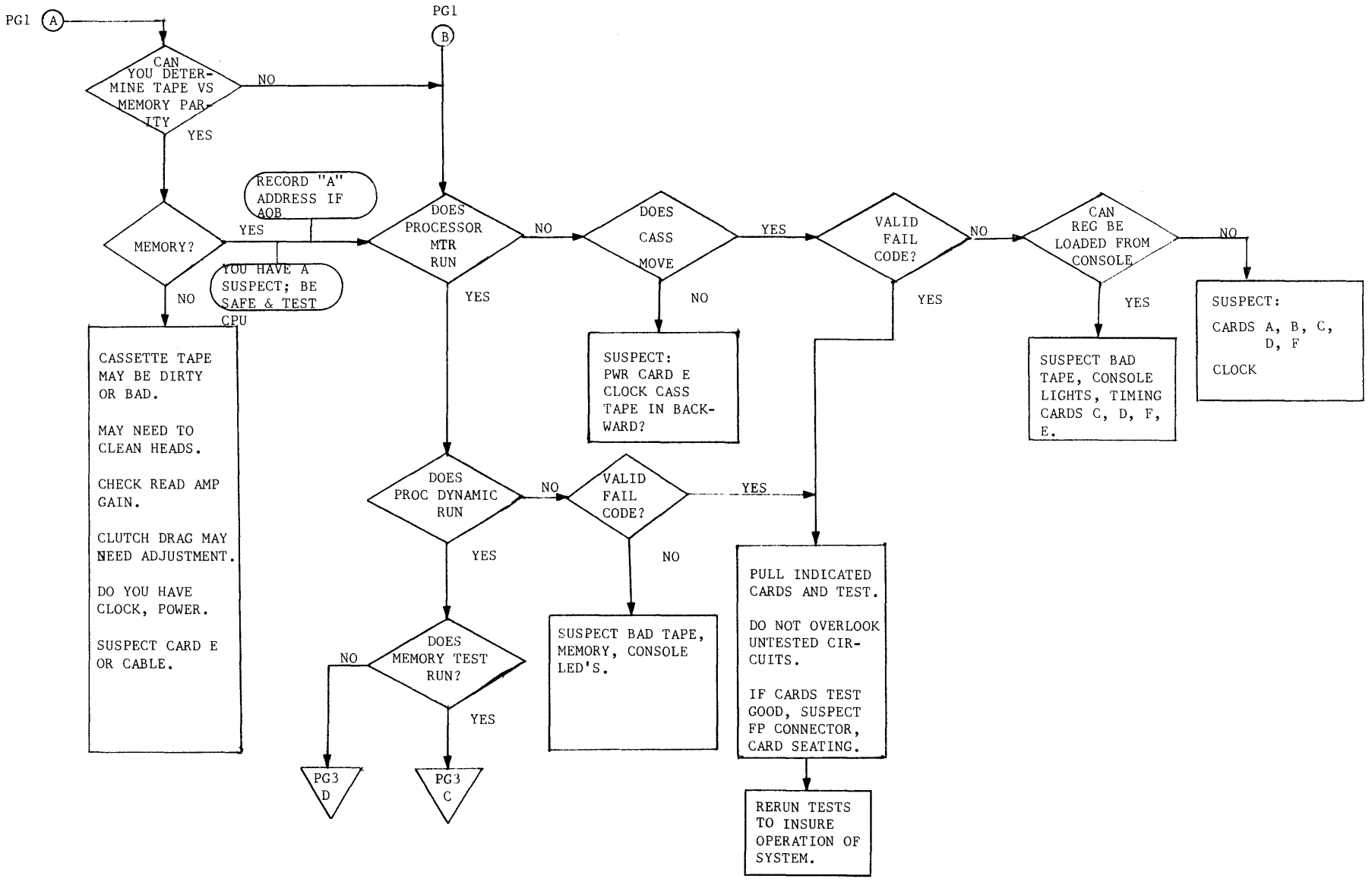
If the dummy load is connected across the +4.75V and -2.0V terminals, no ground reference can be established by the power supply. Therefore, the load should not be connected in this manner.

CAUTION

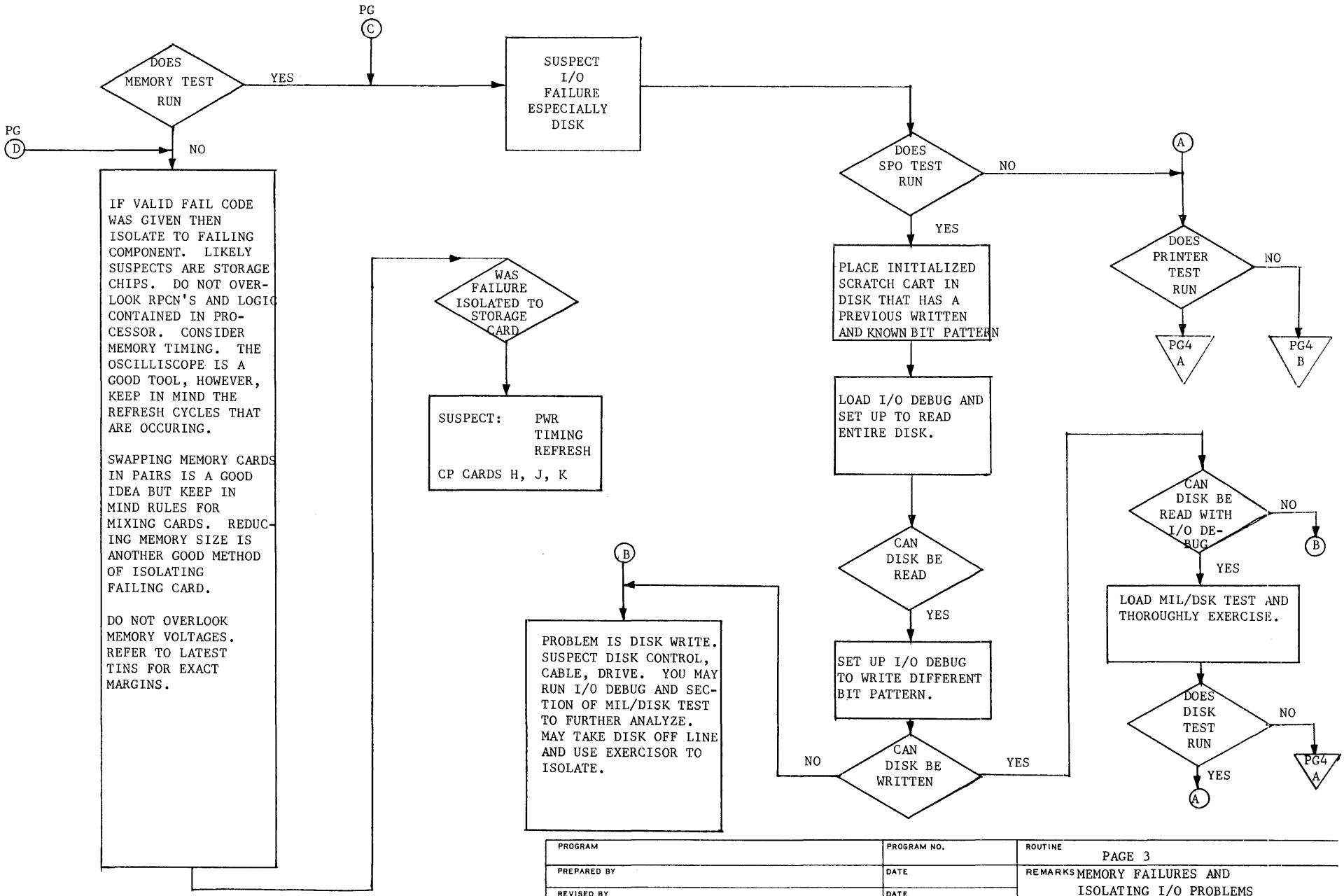
The four transistors Q1 and resistors R3 are rated to handle a total of 100 Amps. Therefore, no attempt should be made to load the +4.75V beyond 100 Amps (e.g., use of two dummy loads in parallel) without shorting or providing an external load for -2.0V.



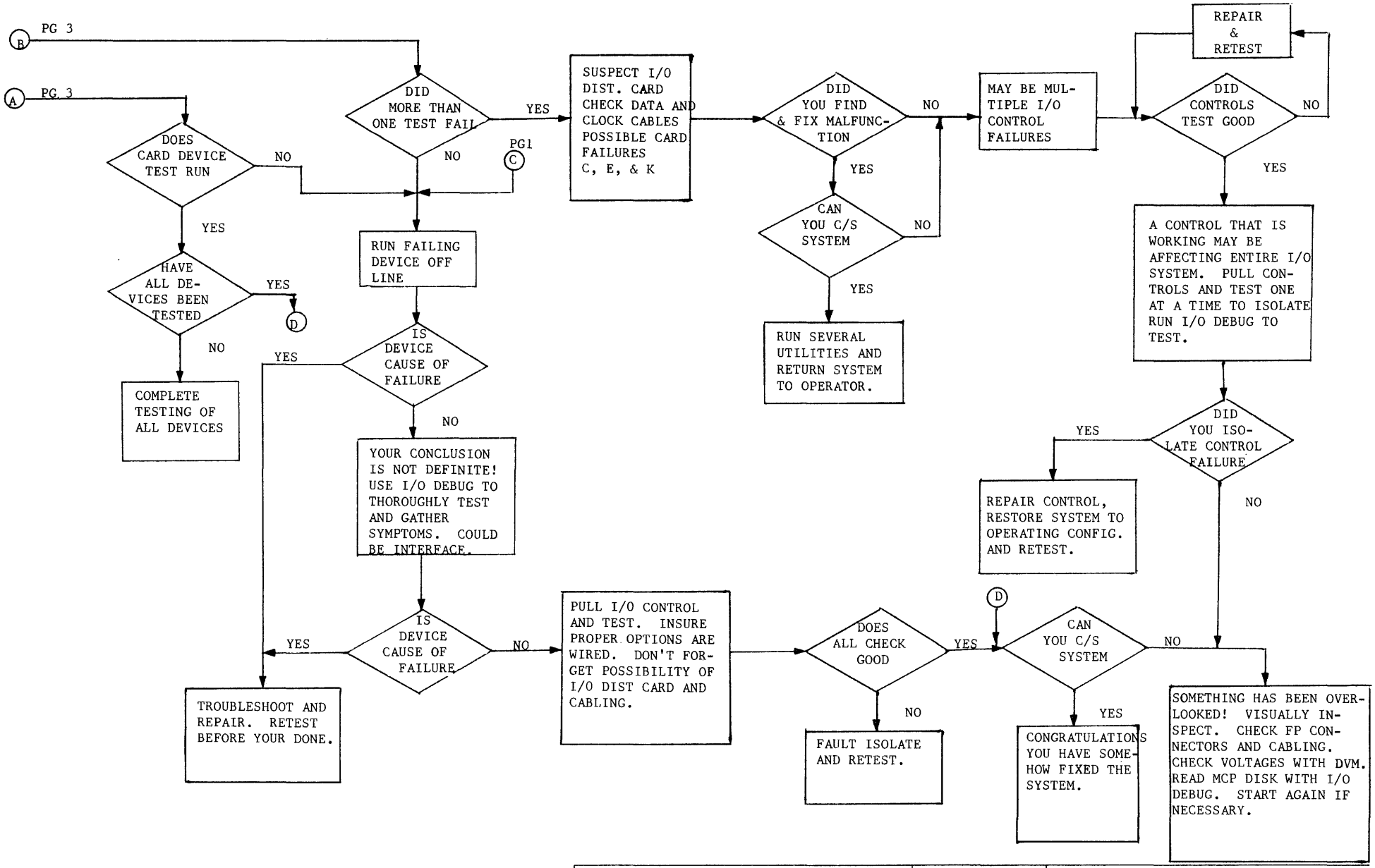
PROGRAM		ROUTINE
B1700 TROUBLESHOOTING FLOW		PAGE 1
		REMARKS DETERMINING WHETHER TO SUSPECT HARDWARE PATH OR SOFTWARE.



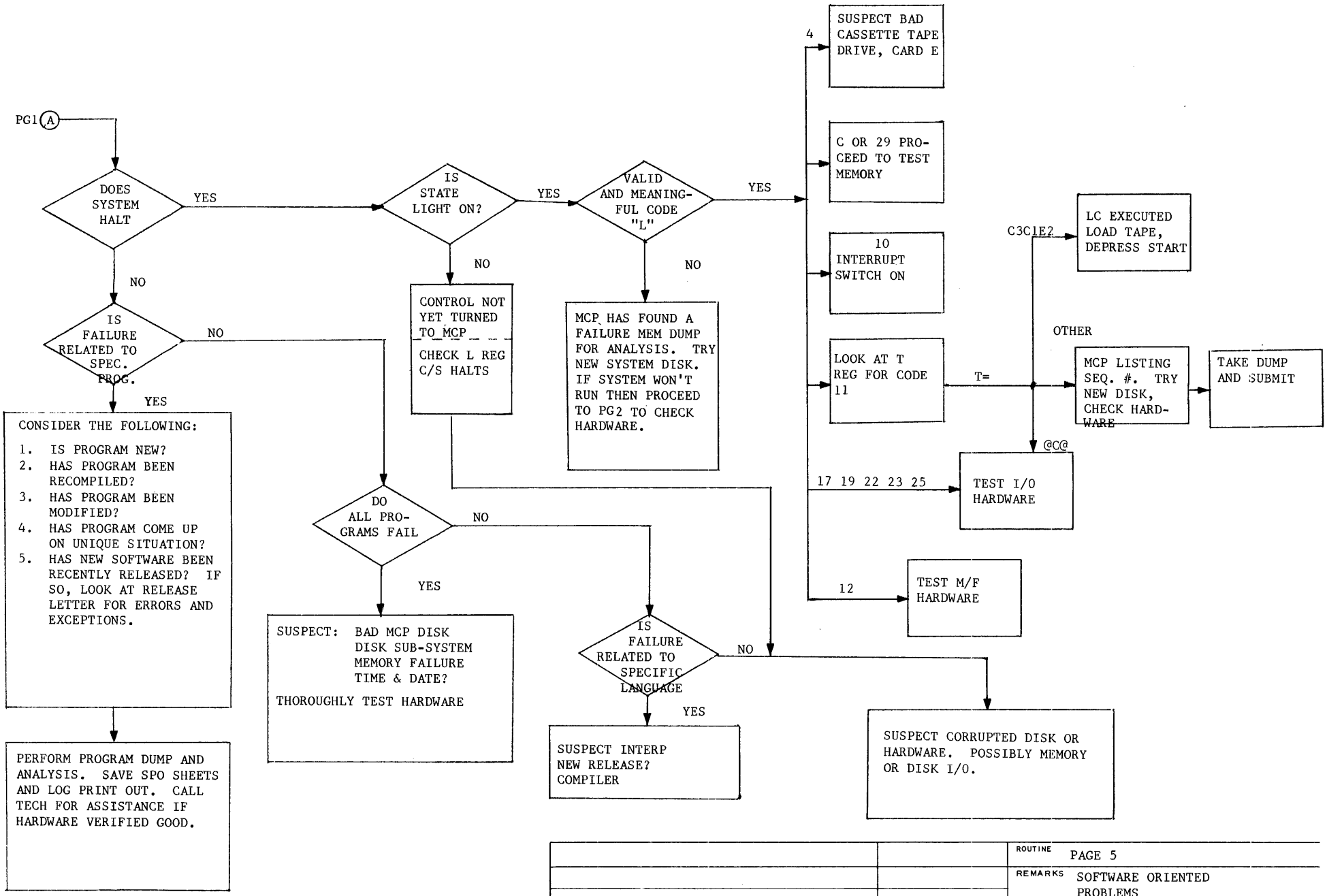
		ROUTINE PAGE 2
		REMARKS RUNNING PROCESSOR ORIENTED TESTS



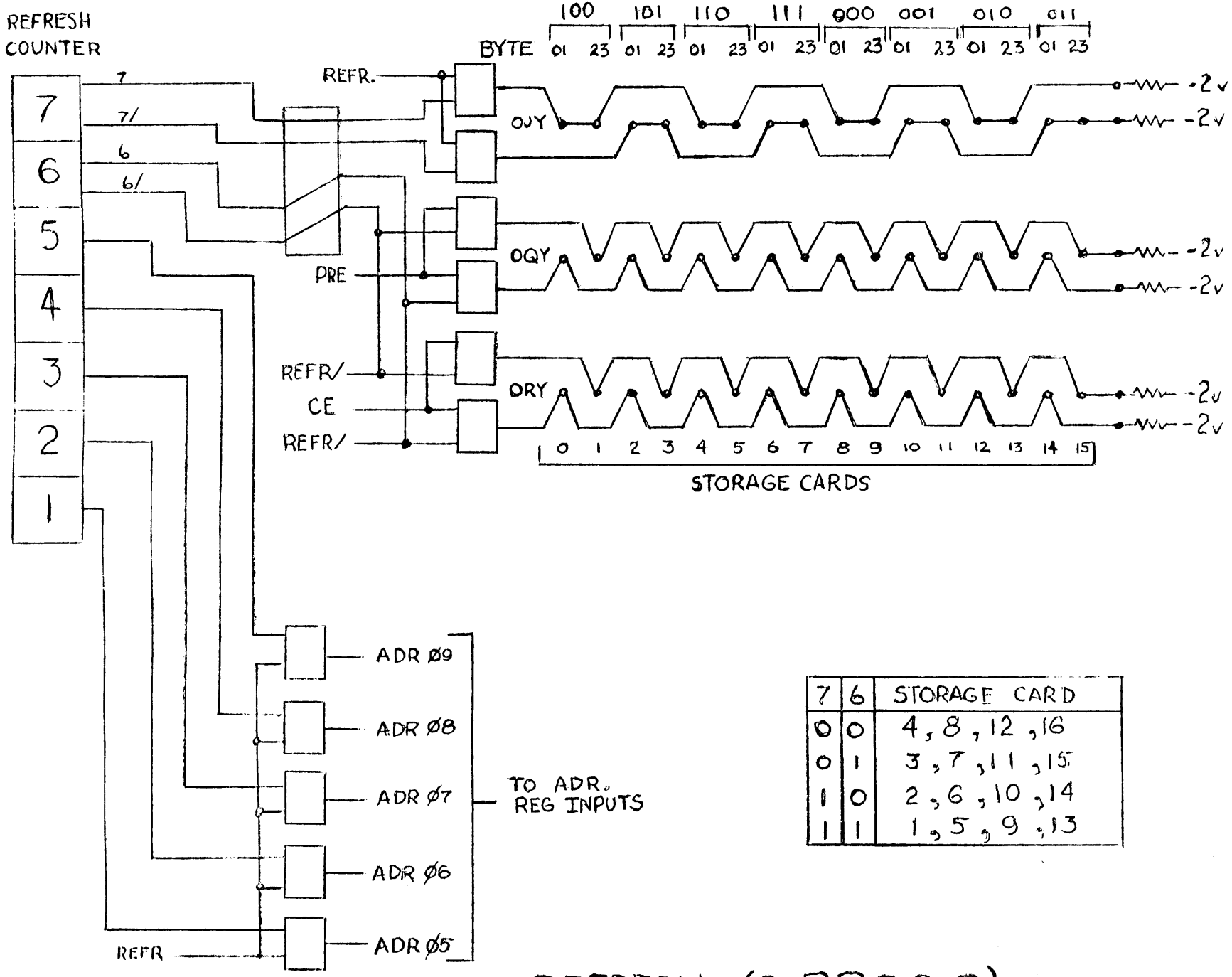
PROGRAM	PROGRAM NO.	ROUTINE
		PAGE 3
PREPARED BY	DATE	REMARKS MEMORY FAILURES AND ISOLATING I/O PROBLEMS
REVISED BY	DATE	



		ROUTINE PAGE 4
		REMARKS ISOLATING & TROUBLESHOOTING I/O FAILURES

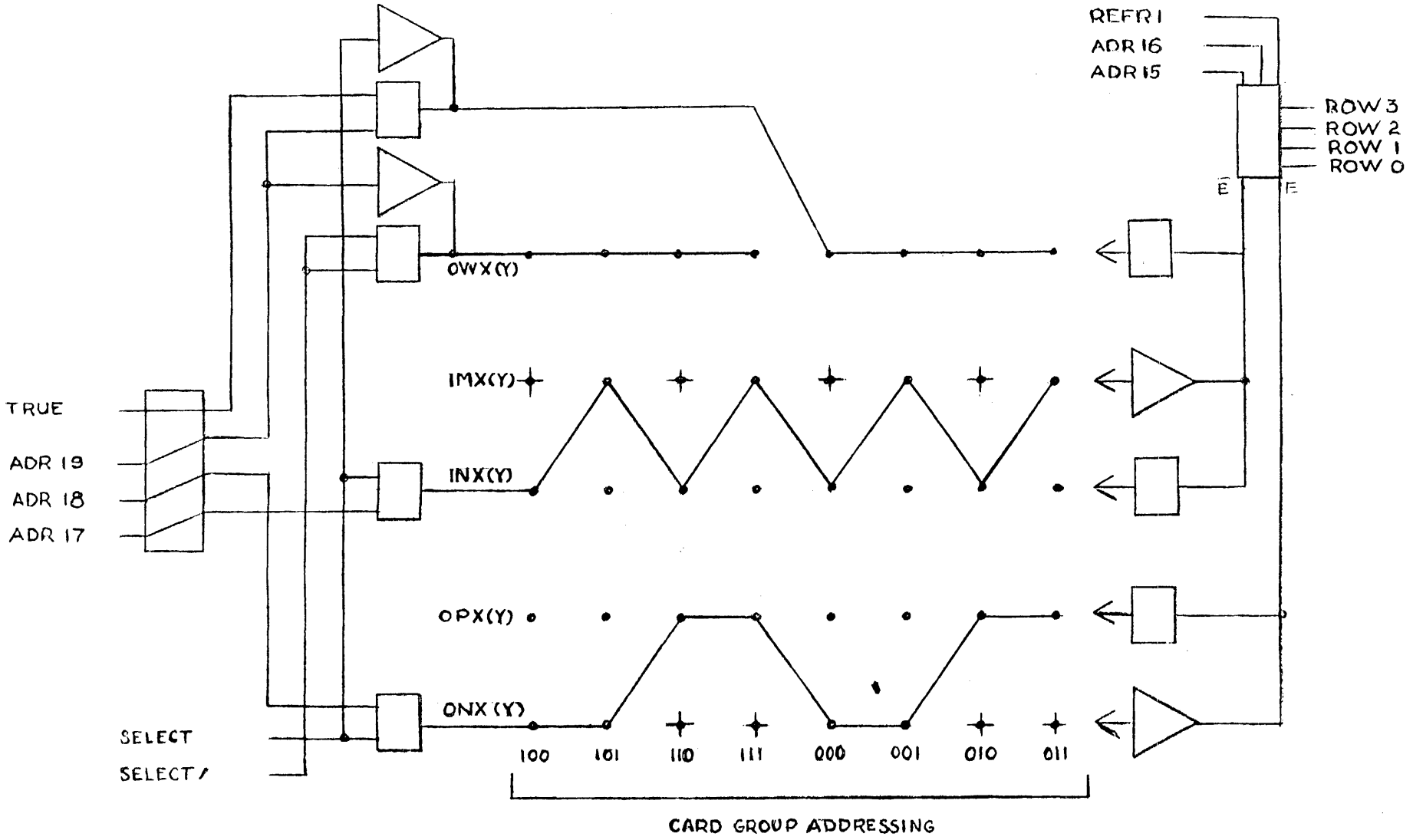


		ROUTINE PAGE 5
		REMARKS SOFTWARE ORIENTED PROBLEMS



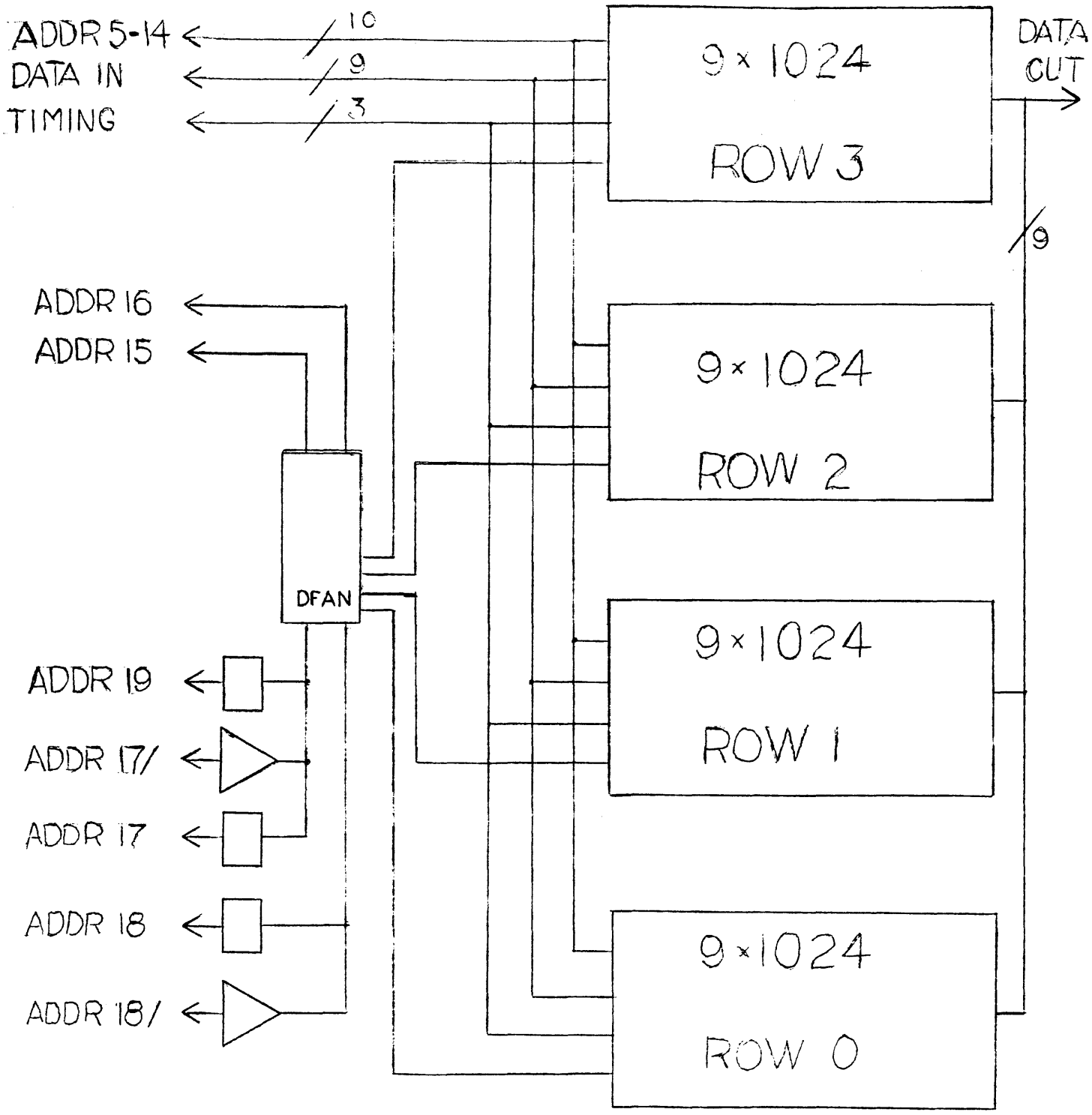
7	6	STORAGE CARD
0	0	4, 8, 12, 16
0	1	3, 7, 11, 15
1	0	2, 6, 10, 14
1	1	1, 5, 9, 13

REFRESH (S-PROC 2)



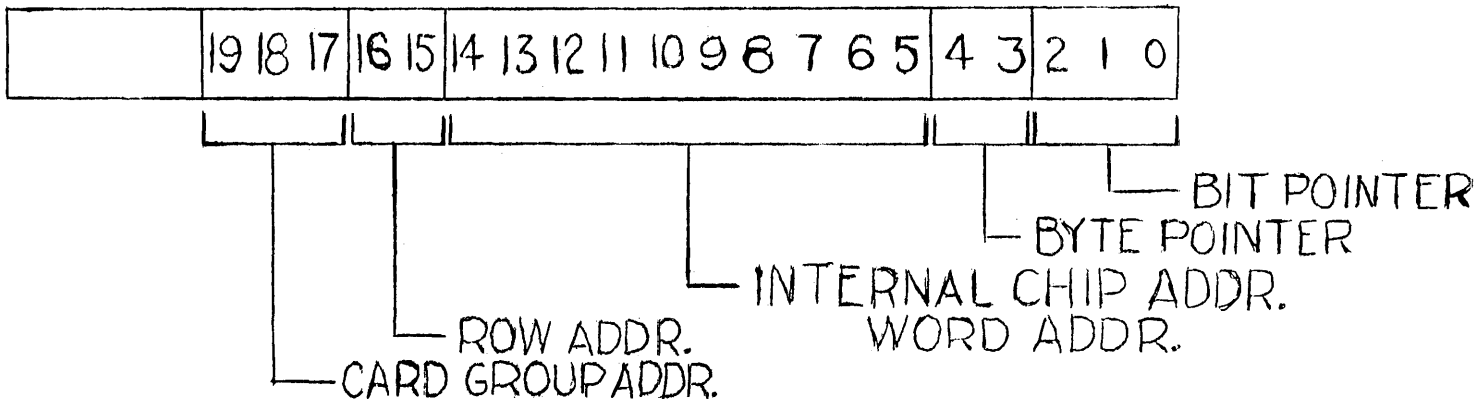
NOTE: ✦ REPRESENTS A FORCED TRUE

S-PROC 2 MEMORY MOD SELECTION



½ - 2 LAYER STORAGE BOARD (S-PROC 2)

MAR A (S-PROC 2)


19 18 17
16 15
14 13 12 11 10 9 8 7 6 5
4 3
2 1 0
BIT POINTER
BYTE POINTER
INTERNAL CHIP ADDR.
WORD ADDR.
ROW ADDR.
CARD GROUP ADDR.