SERIES 9491

MAGNETIC TAPE UNIT

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

Burroughs

Printed in U.S. America Revised 2-7-72

Form 1051166

✓ CHANGES OR ADDITIONS

On "Revised" pages, the check mark (✓) shown to the left of items or subject titles indicates changes or additions since last issue.

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1-4. FUNCTIONAL DESCRIPTION

Figure 1-2 shows a block diagram of the system. The Tape Unit utilizes a single capstan drive for controlling tape motion during the synchronous write, synchronous read, and rewind modes. The tape is under a constant tension of 7 ounces, thus eliminating the possibility of tape "cinch" when the tape reel is placed on a computer transport.

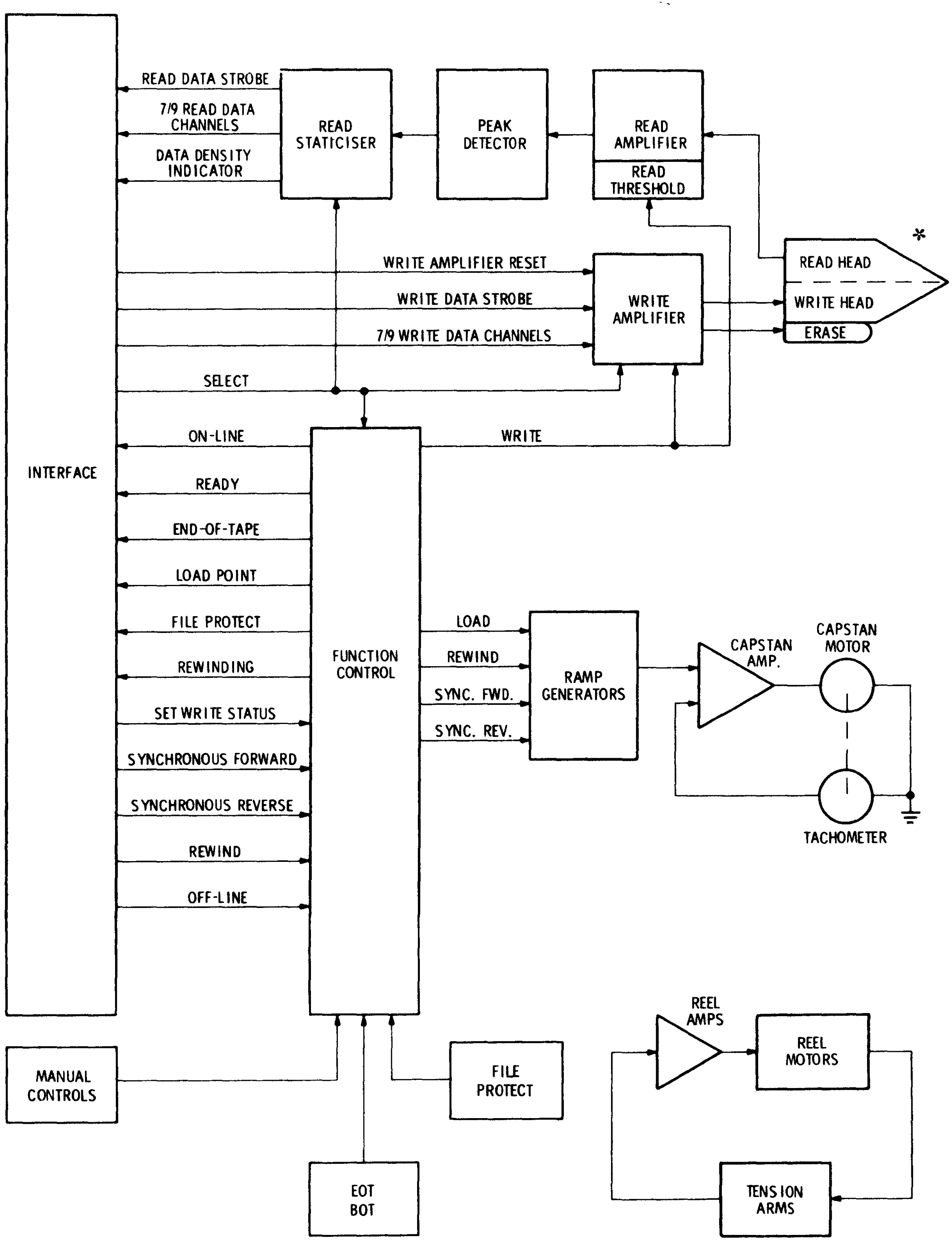
The capstan is controlled by a velocity servo. The velocity information is generated by a dc tachometer that is directly coupled to the capstan motor shaft and produces a voltage that is proportional to the angular velocity of the capstan. This voltage is compared to the reference voltage from the ramp generators using operational amplifier techniques and the difference is used to control the capstan motor. This capstan control technique gives precise control of tape accelerations and tape velocities, thus minimizing tape tension transients.

During a writing operation, the tape is accelerated in a controlled manner to the required velocity. This velocity is maintained constant and data characters are written on the tape at a constant rate such that:

$$\text{Bit density} = \frac{\text{Character Rate}}{\text{Tape Velocity}}$$

When data recording is complete, the tape is decelerated to zero velocity in a controlled manner.

Since the writing operation relies on a constant tape velocity, Inter-Record Gaps (IRGs) (containing no data) must be provided to allow for the tape acceleration and deceleration periods. Control of tape motion to produce a defined IRG is provided externally by the customer controller, in conjunction with the tape acceleration and deceleration characteristics defined within the Tape Unit.



*Only on dual gap units.

FIGURE 1-2
BLOCK DIAGRAM OF TAPE UNIT

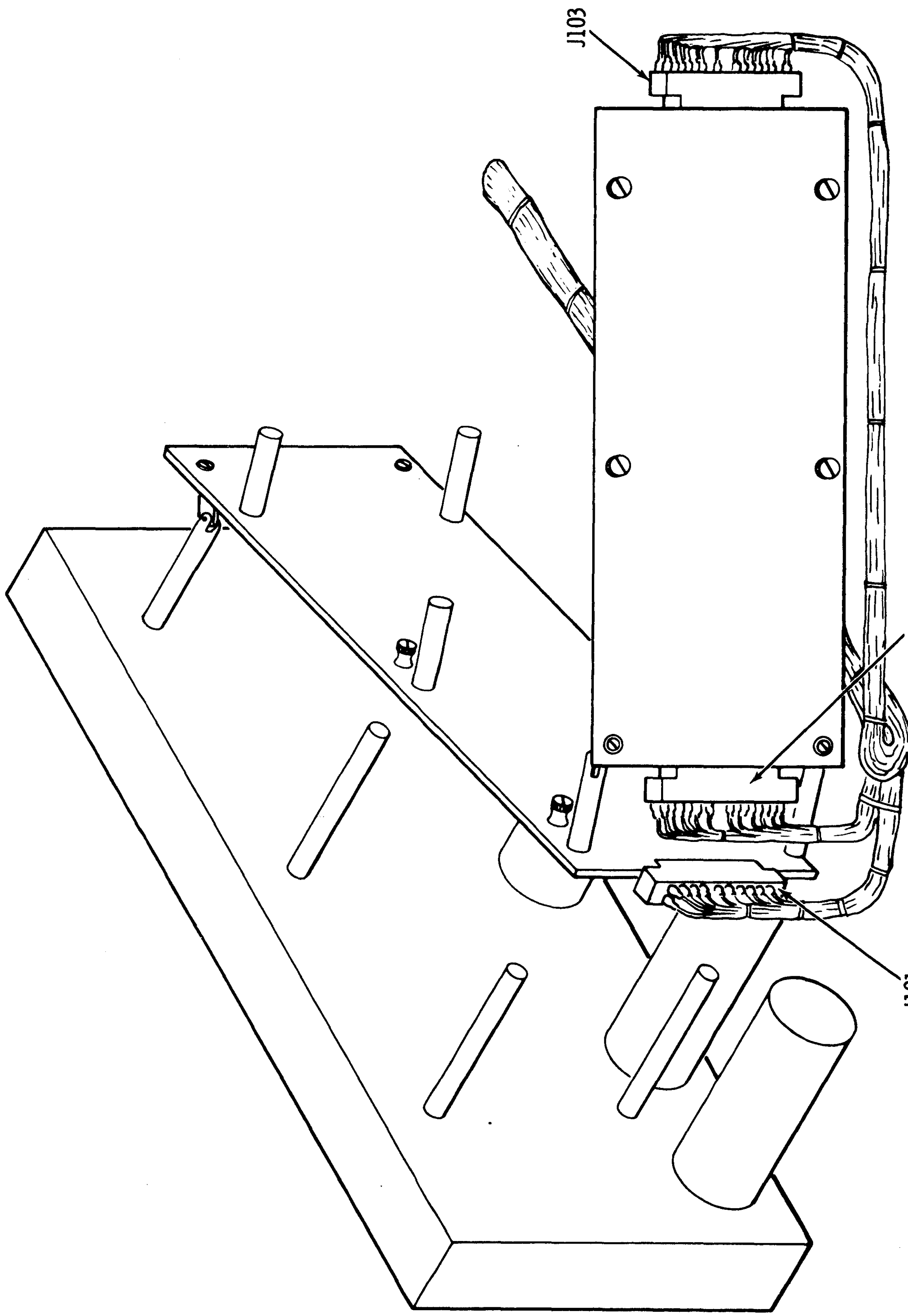


Figure 2-1. Interface Cable Installation

Table 2-1

Interface Connections

Transport Connector Mating Connector			36 Pin Etched PC Edge Connector 36 Pin ELCO 00-6007-036-980-002
Connector (Reference Figure 2-1)	Live Pin	Ground Pin	Signal*
J101	J	8	→ SELECT (SLT)
	C	3	→ SYNCHRONOUS FORWARD Command (SFC)
	E	5	→ SYNCHRONOUS REVERSE Command (SRC)
	H	7	→ REWIND Command (RWC)
	L	10	→ OFF-LINE Command (OFFC)
	K	9	→ SET WRITE STATUS (SWS)
	D	4	→ DATA DENSITY SELECT (DDS) (Optional)
	T	16	← READY (RDY)
	M	11	← ON-LINE Command
	N	12	← REWINDING (RWD)
	U	17	← END OF TAPE (EOT)
	R	14	← LOAD POINT (LDP)
	P	13	← FILE PROTECT (FPT)
	F	6	← DATA DENSITY INDICATOR (DDI)
J102	A	1	→ WRITE DATA STROBE (WDS)
	C	3	→ WRITE AMPLIFIER RESET (WARS)
	L	10	→ WRITE DATA PARITY (WDP)
	M	11	→ WRITE DATA 0 (WD0) } Omit for
	N	12	→ WRITE DATA 1 (WD1) } 7-Channel Head
	P	13	→ WRITE DATA 2 (WD2)
	R	14	→ WRITE DATA 3 (WD3)
	S	15	→ WRITE DATA 4 (WD4)
	T	16	→ WRITE DATA 5 (WD5)
	U	17	→ WRITE DATA 6 (WD6)
	V	18	→ WRITE DATA 7 (WD7)
J103	2	B	← READ DATA STROBE (RDS)
	1	A	← READ DATA PARITY (RDP)
	3	C	← READ DATA 0 (RD0) } Omit for
	4	D	← READ DATA 1 (RD1) } 7-Channel Head
	8	J	← READ DATA 2 (RD2)
	9	K	← READ DATA 3 (RD3)
	14	R	← READ DATA 4 (RD4)
	15	S	← READ DATA 5 (RD5)
	17	U	← READ DATA 6 (RD6)
	18	V	← READ DATA 7 (RD7)

*See Section III for definitions of interface functions.

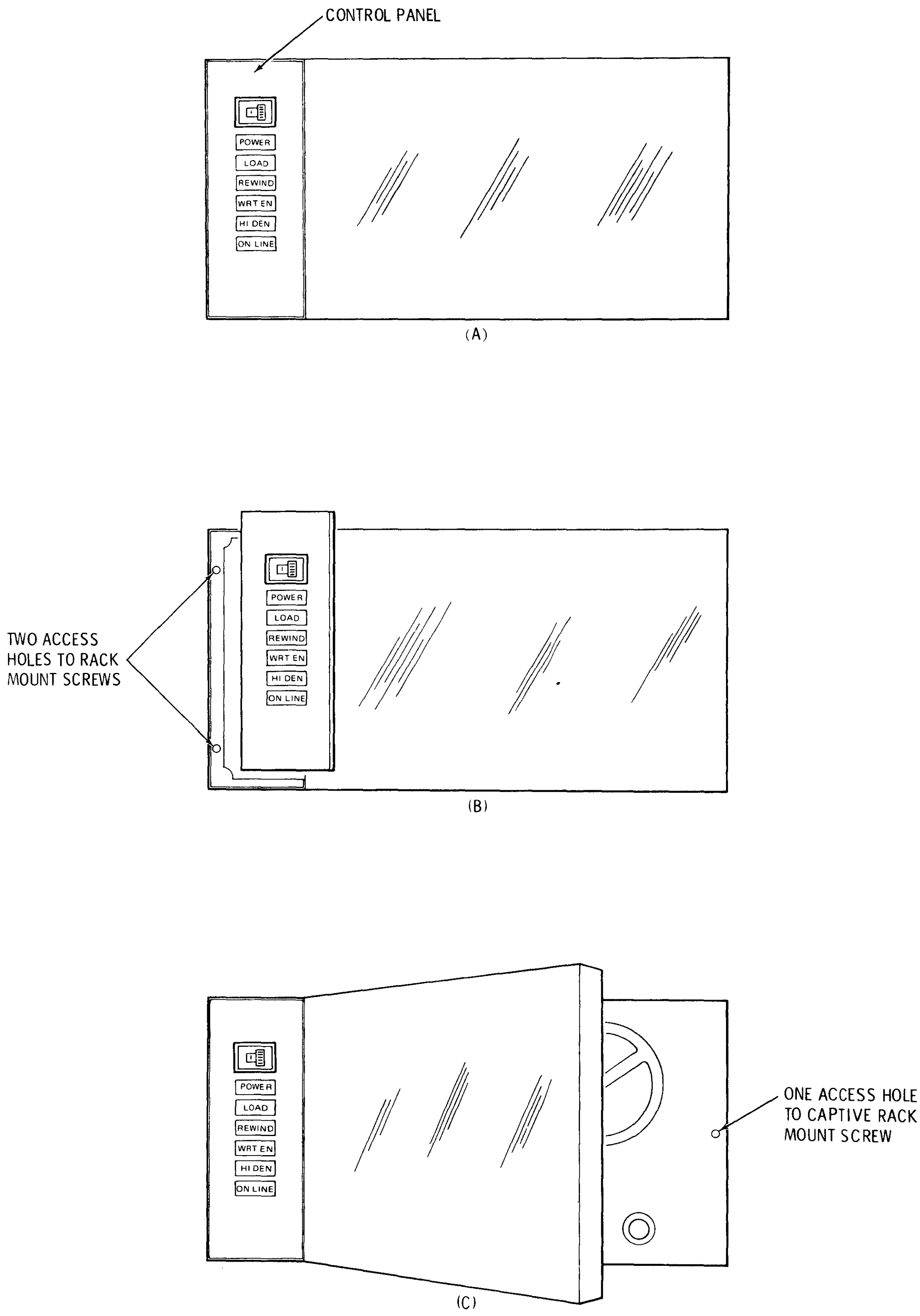


Figure 2-2. Rack Mounting the Transport

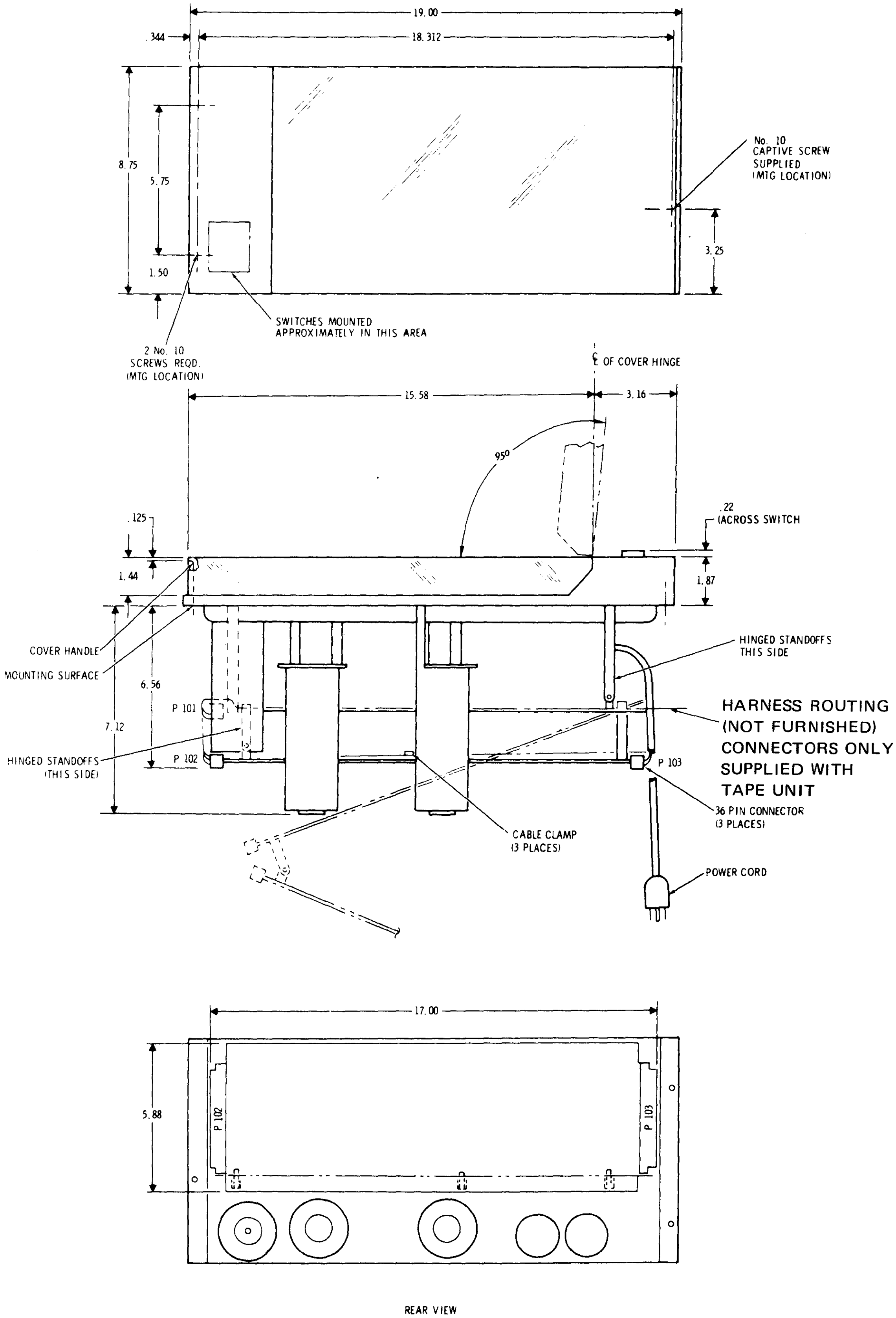


Figure 2-3. Installation Diagram

GLOSSARY

Symbol	Description	Symbol	Description
B1B	Buffer 1 Busy	D8CT	Disable 8 Count
BCD10	Binary Coded Decimal	DBY	Data Busy
BOT*	Beginning of Tape	DDI	Data Density Indicator
BOTD	Beginning of Tape Delay	DDS	Data Density Select
BOTDP	Beginning of Tape Delay Pulse	DDSX	Data Density Select External
BOTI	Beginning of Tape Input	DMC	Disable Manual Controls
BOTO	Beginning of Tape Output	EAO	Encoder Amplifier Output
CBY	Command Busy	ECC	Enable Check Character
CCS	Check Character Strobe	ECD	Echo Check Disable
CMP1, 2	Clamp Waveform 1, 2	ECE	Echo Check Error
CRC0 through CRC7	Cyclic Redundancy Check, Channels 0 through 7	ECO0 through ECO7	Echo Check Output, Channels 0 through 7
CRCC	Cyclic Redundancy Check Character	ECOP	Echo Check Output Parity
		ECR	Echo Check Reset
CRCP	Cyclic Redundancy Check Parity	ECRC	Enable CRC
CT 0 through CT 7	Center Tap 0 through 7	EEC	Enable Echo Check
		EEP	Enable Encoder Pulse
CTP	Center Tap Parity	EF	Erase Winding Finish
CT4	Count 4	EFM	Enable File Mark
CT8	Count 8	EOT*	End of Tape
CUR	Clean-up Ramp	EOTI	End of Tape Input

* An N preceding these symbols indicates a false condition.

GLOSSARY (continued)

Symbol	Description	Symbol	Description
EOTO	End of Tape Output	MOTION	Tape Motion as a result of SFC or SRC Command
EPNP	Encoder Pulse Narrow Powerful		
EPS	Erase Power Start	OFFC	Off-Line Input Command
EPW	Encoder Pulse Wide	OOLL	On-Line/Off-Line Lamp
ES	Erase Winding Start	ORD	OR'd Data
EWPC	Enable Write Power Control	PSO0 through PSO7	Peak Sensor Output, Channels 0 through 7
EWRS	Enable Write/Read Status		
FGC	File Gap Command	PSOP	Peak Sensor Output Parity
FGL	File Gap Lamp	PSP	Peak Sensor Parity
FGR	File Gap Ramp	RA01, RA02	Read Amplifier Track 0, Output 1, Output 2
FLR	First Load - or Rewind		
FM	File Mark	RA11, RA12, RA21, etc.	Read Amplifier Track n, Output 1 or 2
FPT	File Protect		
GIP	Gap In Process	RAC	Read Amplifier Clamp
HID	Hi Density	RACT	Read Amplifier Center Tap
GRS	General Reset	RAP1, RAP2	Read Amplifier Parity, Output 1, Output 2
INTLK	Transport Interlock Signal		
IRGC	Record Gap Command	RD0 through RD7	Read Data, Channels 0 through 7
LD	Lamp Driver		
LDP	Load Point	RDI	Relay Driver Input
LFC	Load Forward Command	RDP	Read Data Parity
LFR	Load Forward Ramp	RDS	Read Data Strobe
LRCC	Longitudinal Redundancy Check Character		

GLOSSARY (continued)

Symbol	Description
RDY	Ready
RF0 through RF7	Read Finish 0 through 7
RFP	Read Finish Parity
RGC	Inter-Record Gap Command
RGR	Inter-Record Gap Ramp
RRS	Remote Reset
RS0 through RS7	Read Start 0 through 7
RSP	Read Start Parity
RST	Reset
RTH	Read Threshold
RTN1	Front Panel Switches Ground Return 1
RWC	Rewind Command
RWD	Rewinding
RWR	Rewind Ramp
RYC	Ready Command
SBY	Start Busy Delay
SFC	Synchronous Forward Command
SFCD	Synchronous Forward Command Delayed
SFL1 through SFL4	Step Forward Level 1 through 4
SLT	Select Transport
SRC	Synchronous Reverse Command
SRO	Select, Ready, and On Line
SWS	Set Write Status
TAD	Turnaround Delay
TBY	Turnaround Busy
TNT	Tape Not Tensioned
TRR	Transport Ready
WARS	Write Amplifier Reset
WCRC	Write CRC
WD0 through WD7	Write Data, Channels 0 through 7
WDP	Write Data Parity
WDS	Write Data Strobe
WDSN	Write Data Strobe Narrow
WDSW	Write Data Strobe Wide
WF0 through WF7	Write Finish, Channels 0 through 7
WFM	Write File Mark

GLOSSARY (continued)

Symbol	Description	Symbol	Description
WFP	**Write Finish Parity**		
WLO	**Write Lockout**		
WPC	**Write Power Control**		
W/RF0 through W/RF7	**Write/Read Head Winding Finish, Channels 0 through 7**		
W/RFP	**Write/Read Head Winding Finish Parity**		
WRO	**Write/Read Output**		
WRP	**Write Pulse**		
WRS	**Write/Read Status**		
W/RS0 through W/RS7	**Write/Read Head Winding Start, Channels 0 through 7**		
W/RSP	**Write/Read Head Winding Start, Parity**		
WRT EN	**Write Enable**		
WS0 through WS7	**Write Start, Channels 0 through 7**		
WSC	**Write Step Command**		
WSP	**Write Start Parity**		

SECTION II
INSTALLATION AND INITIAL CHECKOUT

2-1. INTRODUCTION

This section contains a summary of interface lines, information for uncrating the transport, as well as the procedure for electrically connecting and initially checking out the Tape Unit.

2-2. UNCRATING THE TAPE UNIT

The Tape Unit is shipped in a protective container to minimize the possibility of damage during shipping.

Place the shipping container in the position indicated on the container.

Open the shipping container and remove the packing material so that the Tape Unit and its shipping frame can be lifted from the container.

Lift the Tape Unit out of the container using the shipping frame and set it down so that access to both front and rear of the deck is available.

Check the contents of the shipping container against the packing slip and investigate for possible damage. If there is any damage, notify the carrier.

Check the printed circuit boards and all connectors for correct installation. Check the plug-in relay on the printed circuit board immediately above the power transformer.

Check that the identification label on the back of the tape deck bears the correct model number and line voltage requirement. If the actual line voltage at the installation differs from that on the identification label, the power transformer tap should be changed as shown in Figure 4-3. The POWER switch indicator wire should not be moved.

2-3. POWER CONNECTIONS

A fixed, strain-relieved power cord with polarized plug is supplied on those transports factory wired for 115-volt AC operation. Transports wired to operate on 240-volt AC are supplied with the plug removed from the power cord.

2-4. INITIAL CHECKOUT PROCEDURE

Section III contains a detailed description of all controls. To check the proper operation of the transport before placing it in the system, follow the specified procedure.

(1) Connect the power cord (install power plug and change transformer connections if necessary).

(2) Load tape on the Tape Unit as described in Paragraph 3-3.

(3) Turn the Tape Unit power on by depressing the POWER control.

(4) Depress the LOAD control momentarily to apply capstan-motor and reel-motor power.

(5) Depress the LOAD control momentarily a second time to initiate the Load sequence. The tape will move forward until it reaches the BOT tab, when it stops. The LOAD indicator should light when the BOT reaches the photosensor and remain lit until the tape moves off the Load Point. At this point, there will be no action when the LOAD control is depressed.

(6) Run several feet of tape onto the take-up reel by using the following procedure. Switch off transport while at the load point. Move the BOT tab toward the take-up reel and again turn on the power. When the LOAD control is depressed momentarily the tape moves forward as before. However, this time it does not find a BOT tab because it is already on the take-up reel. If no further action is taken, the tape would run to the end of the reel.

(7) Depress the REWIND control momentarily to initiate the rewind mode and light the REWIND indicator. The tape will rewind past the BOT tab, enter the Load sequence, and return to the BOT tab and stop with the LOAD indicator lit. If the REWIND control is momentarily depressed at BOT the LOAD indicator will be extinguished, the REWIND indicator lit, and the tape will rewind until tape tension is lost. This action is used to unload tape. The reel can be removed as outlined in Paragraph 3-5.

(8) Visually check the components of the tape path for correct tape tracking (tape rides smoothly in the head guides, etc.).

2-5. INTERFACE CONNECTIONS

Two interface configurations are available with the Tape Unit they are:

(1) Twisted Pair Interface. Each signal uses a twisted pair interface where distances greater than 3 feet and less than 20 feet are necessary. The twisted pair should have the following specifications.

(a) Not less than 1 twist per inch.

(b) 22 or 24 gauge conductor with minimum insulation thickness of 0.01 inch.

(c) The ground side of each twisted pair should be connected within a few inches of the receiver or transmitter ground.

(2) Single Line Interface. Where a distance of less than 3 feet is possible, only 1 ground with each interface connector is used.

2-6. RACK MOUNTING THE TAPE UNIT

The physical dimensions of the Tape Unit are such that it may be mounted in a standard EIA rack; 8-3/4 inch panel space is required. It requires a depth behind the mounting surface of at least 8 inches. Unless free access to the back of the deck is available, it is desirable to install the interface connectors before rack mounting.

The Tape Unit's mounting holes are for a standard EIA rack. Figure 2-2 illustrates the procedure for mounting and Figure 2-3 is an installation diagram with dimensions. To rack mount the Tape Unit, follow this procedure.

(1) Place the Tape Unit on a flat surface with the reels facing the operator. Locate the socket wrench and the mounting screws supplied with the Tape Unit.

(2) Remove the control panel located on the left front of the Tape Unit (Figure 2-2(A)). Removal is most easily accomplished by tapping the control panel corners (from the rear) with a screwdriver handle or similar object.

CAUTION

CARE SHOULD BE TAKEN TO ENSURE THAT THE CONTROL PANEL WIRING IS NOT STRESSED.

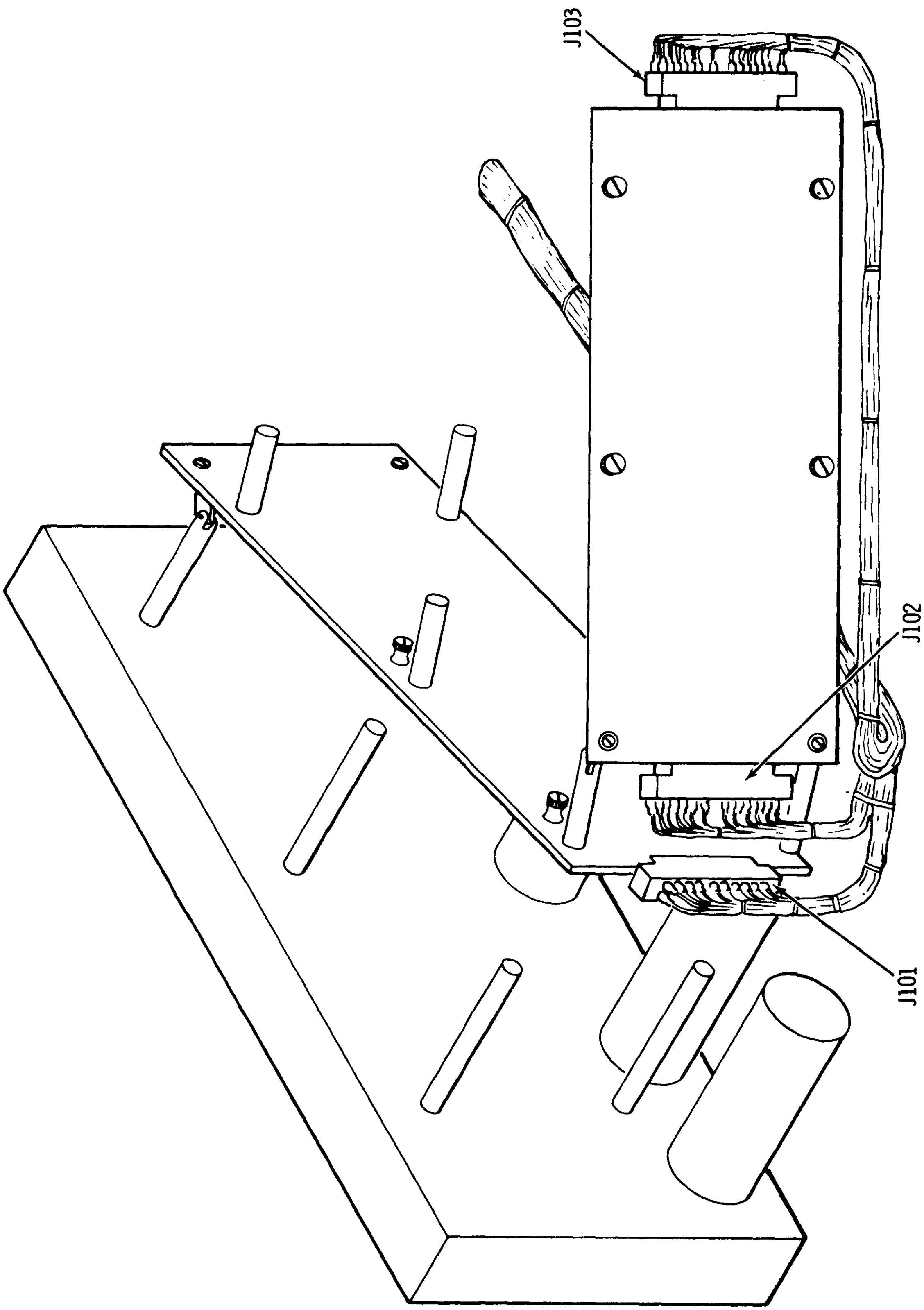


Figure 2-1. Interface Cable Installation

Table 2-1

Interface Connections

Tape Unit Connector			36 Pin Etched PC Edge Connector
Mating Connector			36 Pin ELCO 00-6007-036-980-002
Connector (Reference Figure 2-1)	Live Pin	Ground Pin	Signal*
J101	C	3	→ SYNCHRONOUS FORWARD Command (SFC)
	E	5	→ SYNCHRONOUS REVERSE Command (SRC)
	H	7	→ REWIND Command (RWC)
	K	9	→ SET WRITE STATUS (SWS)
	T	16	← READY (RDY)
	U	17	← END OF TAPE (EOT)
	R	14	← LOAD POINT (LDP)
	P	13	← FILE PROTECT (FPT) (optional)
J102	A	1	→ WRITE DATA STROBE (WDS)
	C	3	→ WRITE AMPLIFIER RESET (WARS)
	E	5	→ READ THRESHOLD (RTH)
	L	10	→ WRITE DATA PARITY (WDP)
	M	11	→ WRITE DATA 0 (WD0) Omit for
	N	12	→ WRITE DATA 1 (WD1) 7-Channel Head
	P	13	→ WRITE DATA 2 (WD2)
	R	14	→ WRITE DATA 3 (WD3)
	S	15	→ WRITE DATA 4 (WD4)
	T	16	→ WRITE DATA 5 (WD5)
	U	17	→ WRITE DATA 6 (WD6)
	V	18	→ WRITE DATA 7 (WD7)
J103	1	A	← READ DATA PARITY (RDP)
	3	C	← READ DATA 0 (RD0) Omit for
	4	D	← READ DATA 1 (RD1) 7-Channel Head
	8	J	← READ DATA 2 (RD2)
	9	K	← READ DATA 3 (RD3)
	14	R	← READ DATA 4 (RD4)
	15	S	← READ DATA 5 (RD5)
	17	U	← READ DATA 6 (RD6)
	18	V	← READ DATA 7 (RD7)

*See Section III for definitions of interface functions.

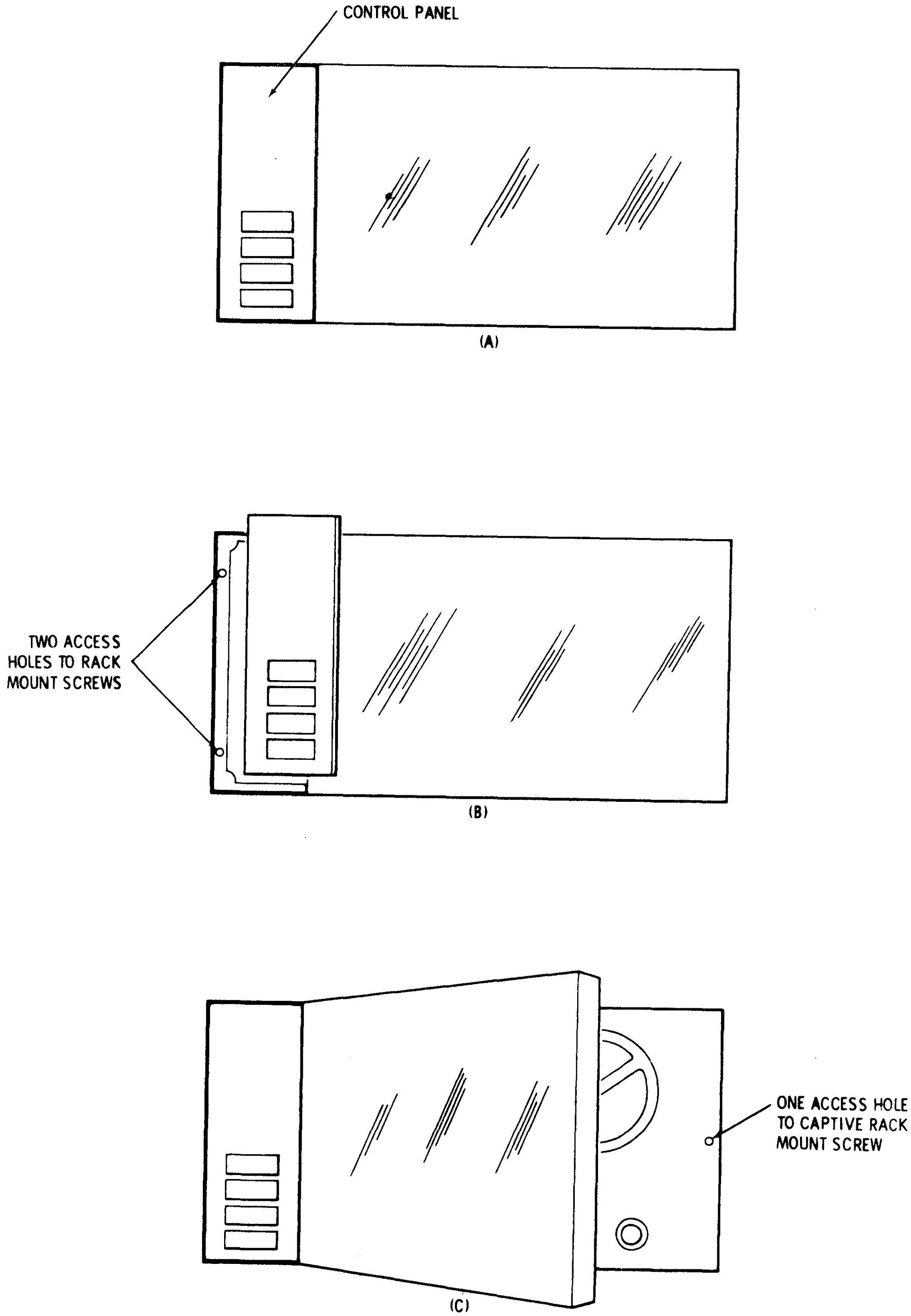


Figure 2-2. Rack Mounting the Tape Unit

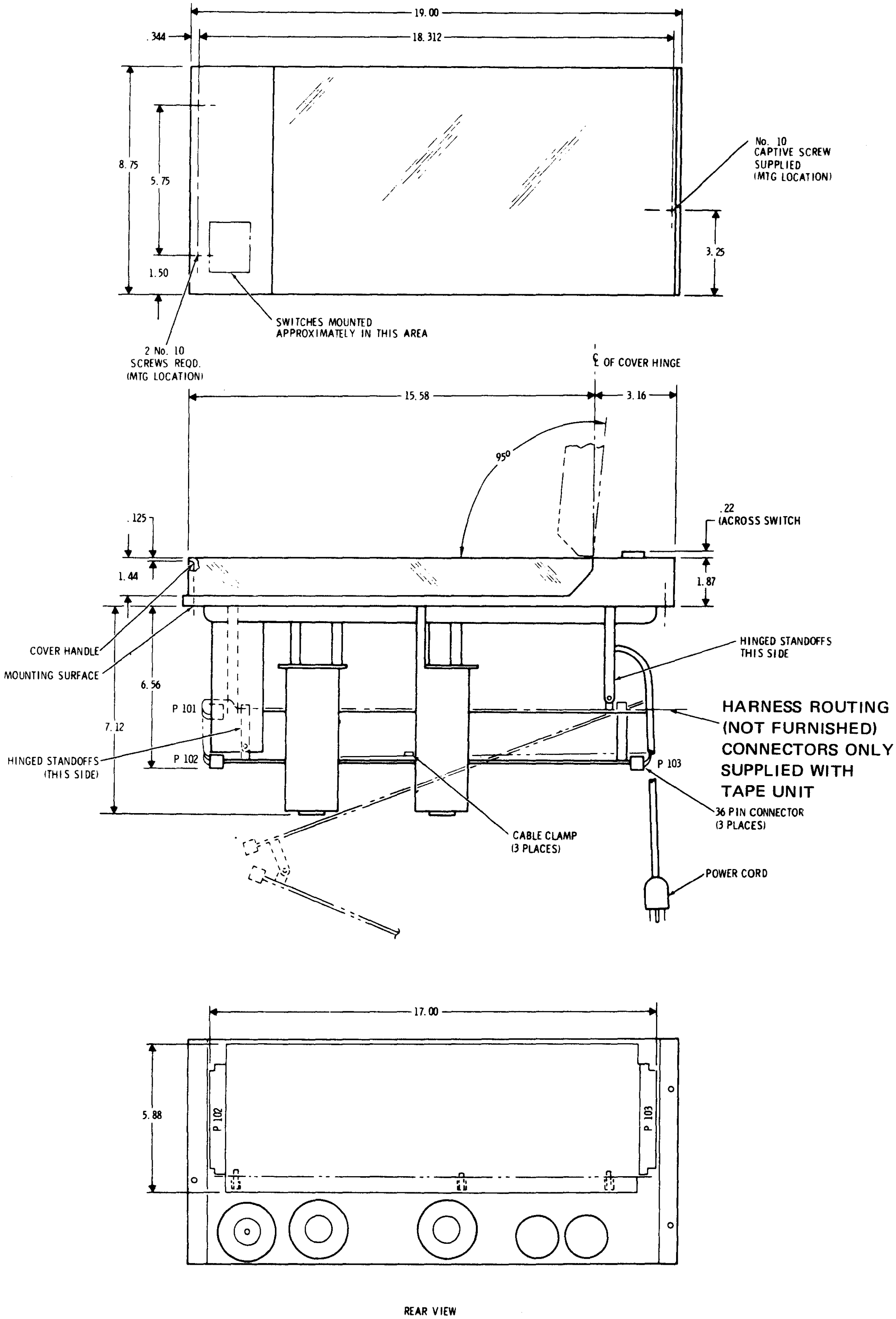


Figure 2-3. Installation Diagram

(3) Remove the three No. 8 1-inch screws holding the Tape Unit to the shipping frame (Figure 2-2 (B) and (C)).

(4) Locate the Tape Unit in the rack and insert the two socket head screws in the access holes on the left front of the transport. Do not tighten at this point.

(5) Open the dust cover and locate the single captive screw on the right over the hole in the rack (using the socket wrench) and tighten the screw.

(6) Tighten the two screws on the left and snap the control panel into position.

SECTION III
OPERATION

3-1. INTRODUCTION

This section explains the manual operation of the tape transport and defines the interface functions with regard to timing, levels and interrelationships.

3-2. CLEANING THE HEAD AND GUIDES

The brief operation described in Paragraph 6-4 must be performed daily to realize the data reliability capabilities of the Tape Unit

3-3. LOADING TAPE ON TRANSPORT

The Tape Unit, in the position shown in Figure 3-1, has the supply reel (reel to be recorded or reproduced on the left side, adjacent to the manual controls. The tape must unwind from the supply reel when the reel is turned in a clockwise direction. Note that if the File Protect option is used, a Write Enable ring on the reel is required to close the interlocks which allow writing.

To load a tape reel (maximum reel size is 7 inches in diameter with 600 feet of tape), position the reel over the quick-release hub and depress the center plunger. This allows the reel to slip over the rubber ring on the hub. Press the reel evenly and firmly against the back flange of the hub with the center plunger depressed. Release the center plunger. The reel is now properly aligned in the tape path and ready for tape threading.

Thread tape along the path shown in Figure 3-1. The tape path is delineated by a fine line on the overlay. The take-up or fixed reel is equipped with a retaining strip which greatly facilitates take-up of the tape. It is necessary only to lay 3 inches of tape onto the take-up reel and apply a wiping action quickly with the finger to produce adequate friction between the tape and reel when tension is applied.

3-4. BRINGING TAPE TO LOAD POINT

The tape should be manually tensioned and checked for correct seating in the guides by rotating the supply hub. To bring the tape to the Load Point:

(1) Turn power on by depressing the POWER control.

(2) Depress and release the LOAD control. This applies power to the capstan and reel motors and brings the tape to the correct operating tension. The tape storage arms are now in the operating position.

CAUTION

CHECK THAT THE TAPE IS POSITIONED CORRECTLY ON ALL GUIDES OR TAPE DAMAGE MAY RESULT.

(3) Depress and release the LOAD control a second time. This causes tape to move forward at the prescribed operating velocity. Check tape tracking in the guides again and close the dust cover.

CAUTION

THE DUST COVER SHOULD REMAIN CLOSED AT ALL TIMES WHEN TAPE IS ON THE TAKE-UP REEL. DATA RELIABILITY MAY BE IMPAIRED BY CONTAMINANTS IF THE COVER IS LEFT OPEN.

When the reflective BOT tab reaches the Load Point, the tape stops with the front edge of the tab approximately 1 inch from the magnetic head gap. The Tape Unit is now ready to receive external commands.

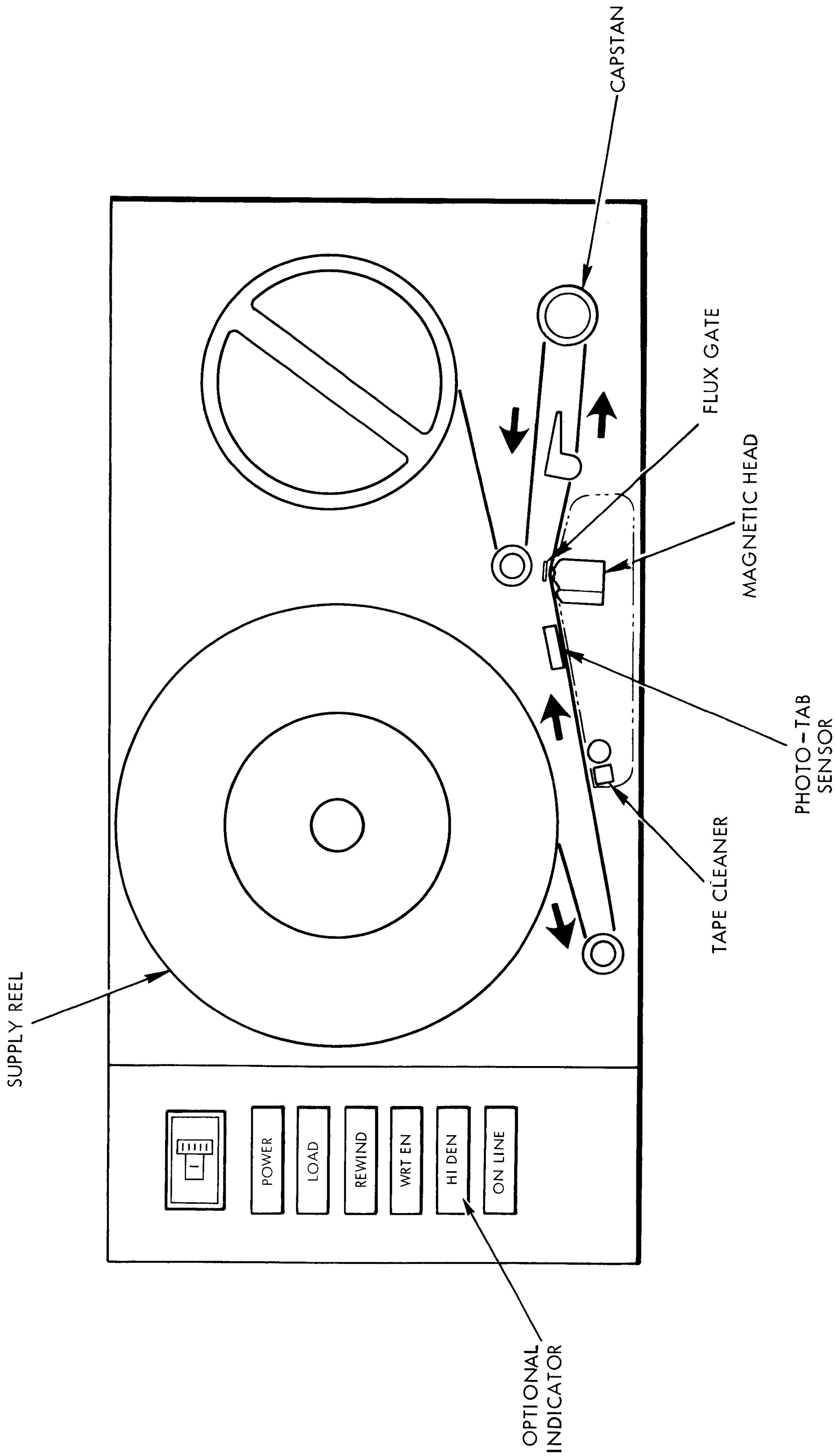


Figure 3-1. Tape Path and Controls

3-5. UNLOADING THE TAPE

To unload a recorded tape, complete the following procedure if the power has been switched off. (If power is on, start at step (3).)

(1) Turn the power on by depressing the POWER control.

(2) Depress and release the LOAD control, this applies tape tension.

(3) Depress and release the REWIND control. When the tape has rewound to the BOT tab, it comes to a controlled stop. The tape overshoots and the transport enters the Load sequence to bring the tape to rest at the BOT.

(4) Depress and release the REWIND control a second time. This initiates a further rewind action which continues until tension is lost.

(5) Open the dust cover and wind the end of the tape onto the supply reel. Depress the hub center plunger and remove the reel. Close the dust cover.

3-6. MANUAL CONTROLS

The operational controls with indicators are located on the control panel on the front of the Tape Unit (see Figure 3-1). The following paragraphs describe the function of these controls.

3-7. POWER

The POWER control is an alternate action switch/indicator which connects AC power to the transformer. When power is turned on:

(1) All power supplies are established.

(2) The ground returns of all motors are open-circuited.

(3) A reset signal is applied to appropriate control flip-flops.

3-8. LOAD

The LOAD control is a momentary switch/indicator. Depressing and releasing the control for the first time after power has been applied to the Tape Unit:

(1) Energizes the reel servo system by applying ground returns to all motors.

(2) Removes the reset signal applied to the control flip-flops.

(3) Tensions the tape.

Depressing and releasing the LOAD control a second time causes the tape to advance to and stop at the BOT tab. The Tape Unit is now conditioned to receive external commands. While the BOT tab is located over the photo-tab sensor (see Figure 3-1), the LOAD switch/indicator is lit.

The LOAD control is disabled after the first LOAD or manual REWIND command has been given. The control is re-enabled only after a loss of tape tension or restoration of power after the Tape Unit power has been turned off.

3-9. REWIND

The REWIND control is a momentary switch/indicator. The REWIND control is enabled whenever the tape is tensioned and will override a LOAD or any external command that is currently in progress.

Depressing and releasing the REWIND control causes the tape to rewind at 50 ips to the BOT. When the tape reaches BOT, the rewind drive ceases and a Load sequence is automatically initiated. The BOT tab will overshoot the photo-tab sensor, move forward, and stop at the Load Point.

When the REWIND control is activated when the tape is at Load Point (LOAD switch/indicator lit) the tape rewinds off the take-up reel and tension is lost.

The REWIND switch/indicator is lit for the duration of any rewind operation including the subsequent Load sequence where relevant.

3-10. WRT EN (Write Enable)

The WRT EN indicator is provided on those Tape Unit employing the File Protect option. The indicator is lit whenever power is applied and a reel of tape, with a Write Enable ring installed, is mounted on the transport.

3-11. INTERFACE INPUTS (Controller to Tape Unit)

All waveform names are chosen to correspond to the logical true condition. Drivers and receivers belong to the DTL 830 series where the True level is 0 volt and the False level is between +3 and +5 volts. Figure 1-3 is a schematic of the Interface circuits.

3-12. SYNCHRONOUS FORWARD COMMAND (SFC)

This is a level which, when true, and the transport is READY (see Paragraph 3-22) causes the tape to move forward at the specified velocity. When the level goes false, tape motion ceases. The velocity profile is trapezoidal with nominally equal rise and fall times.

3-13. SYNCHRONOUS REVERSE COMMAND (SRC)

This is a level which, when true, and the Tape Unit is READY (see Paragraph 3-22) causes the tape to move in the reverse direction at the specified velocity. When the level goes false, tape motion ceases. The velocity profile is trapezoidal with nominally equal rise and fall times. An SRC will be terminated upon encountering BOT, or ignored if given at BOT.

3-14. REWIND COMMAND (RWC)

This is a pulse (minimum width of 2 microseconds) which causes the tape to move in the reverse direction at 50 ips. Upon reaching BOT, the rewind ceases and the Load sequence is automatically initiated. The tape now moves forward and comes to rest at BOT.

The REWIND indicator is lit for the duration of the Rewind and the following Load sequence.

An RWC is ignored if the tape is already at BOT, or if the Tape Unit is not READY.

The velocity profile is trapezoidal with nominally equal rise and fall times of approximately 250 milliseconds.

3-15. SET WRITE STATUS (SWS)

This is a level which must be set true before tape motion begins (before the SFC or SRC is given) when writing the first data record, and held true until tape motion ceases after writing the last data record. When SWS is true (and a Write Enable ring is fitted on the supply reel for those Tape Unit with the File Protect option), write current is allowed to pass through the magnetic head windings.

This waveform is gated with READY in the transport ensuring that writing cannot take place:

(1) Until the initial LOAD or REWIND command is completed

(2) During subsequent REWIND commands

(3) When tape tension is lost.

3-16. WRITE DATA LINES (WDP, WD0-7 9-Channel; WDP, WD2-7 7-Channel)

These are levels which, when true, at Write Data Strobe (WDS) time (when the Tape Unit is in WRITE status) result in a flux reversal being recorded on the corresponding tape track.

These lines must be held steady during the WDS, and for 0.5 microsecond before and after the WDS pulse.

3-17. WRITE DATA STROBE (WDS)

This is a pulse (2 microseconds minimum) for each character to be recorded. It samples each of the WRITE DATA Lines and toggles the appropriate flip-flops in the write register when a "1" is to be written. The WDP and WD0-7 levels must be steady during and for 0.5 microsecond before and after the WDS. Toggling of the write register is initiated by the trailing edge of WDS.

The recording density is determined by the tape speed and the frequency of the WDS pulses. Frequency stability should normally be better than 0.25 percent.

An additional WDS pulse, accompanied by the appropriate levels on WDP, WD0-7 is required to write the Cyclic Redundancy Check Character (CRCC) in 9-channel systems, four character spaces after the last data character. The Longitudinal Redundancy Check Character (LRCC) is written by a pulse on control line WARS, 8 character spaces after the last data character (4 character spaces for 7-channel).

3-18. WRITE AMPLIFIER RESET (WARS)

This is a pulse (2 microseconds minimum) which causes the LRCC to be written onto tape 8 character spaces (4 for 7-channel) after the last data character has been written. The pulse resets the write register causing all channels to be erased in a uniform direction in the Inter-Record Gap. The LRCC is written coincident with the leading edge of this pulse.

3-19. READ THRESHOLD (RTH)

This is a level which, when true, selects the higher of two read amplifier threshold levels. RTH must be held steady for the duration of each record. The high threshold level should be selected only when it is desired to perform a read after write data check. When reading a pre-recorded tape, the RTH line should be in the false state.

3-20. INTERFACE OUTPUTS (Tape Unit to Controller)

3-21. READY (RDY)

This is a level which is true when the Tape Unit is ready to accept any external command; i.e., when

(1) Tape tension is established

(2) The initial LOAD or REWIND command has been completed

(3) There is no subsequent REWIND command in progress.

3-22. READ DATA (RDP, RD0-7 9-Channel; RDP, RD2-7 7-Channel)

This is a true-going pulse for each "1" bit read from tape. The trailing edge of each pulse corresponds to the detected flux change. The pulse width is approximately half-a-character period but varies with the data pattern. These lines must be suitably processed by the controller to obtain the Read Data Strobe. These lines should be deselected by the controller when writing, or when tape is not up to speed when reading.

3-23. END OF TAPE (EOT)

This is a level which, when true, indicates that the EOT reflective tab is positioned under the photo-tab sensor.

3-24. LOAD POINT (LDP)

This is a level which, when true, indicates that the BOT reflective tab is positioned under the photo-tab sensor, and the Tape Unit is READY. The signal goes false after the tab leaves the photosensor area.

3-25. FILE PROTECT (FPT) (Optional)

This is a level which is true when power is on and there is no Write Enable ring mounted on the supply reel.

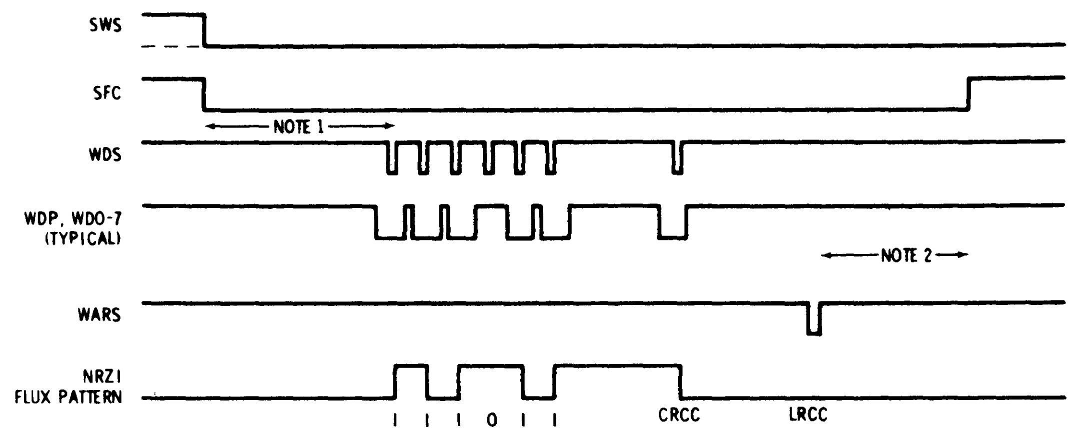
3-26. <u>INTERFACE TIMING</u>

3-27. WRITE WAVEFORMS

Figure 3-2 shows the write waveforms. The controller generates all command waveforms.

3-28. READ WAVEFORMS

Figure 3-3 shows the read waveforms.



NOTES:

1. Pre-record delay should be calculated to produce 3.5 inches of travel when starting from BOT; otherwise 0.4 inch in a 9-channel Tape Unit and 0.51 inch in a 7-channel Tape Unit.
2. The post-record delay should be calculated to produce 0.075 inch of travel after the LRCC, before removing the SFC.

Figure 3-2. Write Waveforms

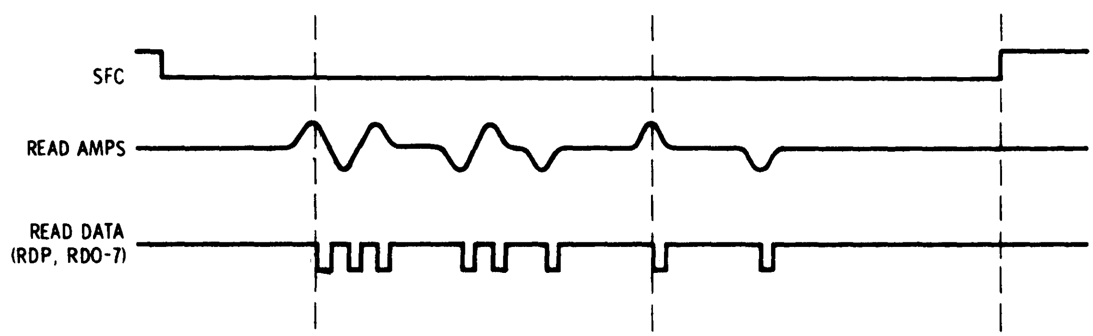


Figure 3-3. Read Waveforms

RESERVED FOR EXPANSION

3-29. ON-LINE

The ON-LINE control is a momentary switch/indicator which is enabled after an initial Load or Rewind sequence has been initiated.

Depressing and releasing the switch after an initial Load or Rewind sequence is initiated, switches the transport to an On-line mode and lights the indicator.

In this condition the transport can accept external commands provided it is also Ready and Selected.

The transport will revert to the Off-line mode if any of the following occur.

(1) The ON-LINE control is depressed a second time.

(2) An external Off-line command (OFFC) is received.

(3) Tape tension is lost.

3-30. HI DEN (High Density)

The HI DEN control is an alternate action switch/indicator. It is provided only for 7-track operation where it selects the character packing density at which the Read electronics operates.

When the indicator is lit, the Read electronics is conditioned to operate in the High Density mode. If the indicator is not lit, the transport will be in the Low Density mode.

The following possible combinations are available.

Density Combination
800/556
800/200
556/200

3- 31. SELECT

The SELECT control is a thumbwheel switch which is not connected internally in the tape transport.

3-32. SELECT (SLT)

This is a level which, when true, enables all of the interface drivers and receivers in the transport, thus connecting the transport to the controller.

It is assumed that all of the interface inputs discussed in the following paragraphs are gated with SELECT (SLT).

3- 33. OFF-LINE (OFFC)

This is a level or pulse of a minimum width of 2 μseconds which resets the On-Line flip-flop to the false state, placing the transport under manual control.

It is gated in the transport by SELECT only, allowing an OFF-LINE command to be given while a rewind is in progress. OFF-LINE must be separated by at least 2 μseconds from a REWIND command.

3- 34. REWINDING (RWD)

This is a level which is true when the transport is engaged in any Rewind operation or the Load sequence following a rewind operation.

3-35. READY (RDY)

This is a level which is true when the transport is ready to accept any external command; i.e., when:

(1) Tape tension is established.

(2) The initial LOAD or REWIND command has been completed.

(3) There is no subsequent REWIND command in progress.

(4) The transport is On-line.

3-36. DATA DENSITY INDICATOR (DDI)

This is a level which is true whenever the Read electronics are conditioned to operate in the High Density mode.

3-37. READ DATA STROBE (RDS)

This is a pulse with a minimum width of 2 μseconds for each data character read from tape. The trailing edge of this pulse should be used to sample the Read Data lines.

Although the average time between adjacent RDS pulses is $\frac{1}{BV}$, where B is the bit density and V is the tape velocity, this may vary considerably because of skew and bit crowding effects.

3-38. ON-LINE

This is a level which is true when the On-line flip-flop is set. When true, the transport is under remote control. When false, the transport is under local control.

SECTION IV

THEORY OF OPERATION

4-1. INTRODUCTION

This section gives a detailed description of the operation of the Tape Unit.

The Tape Unit consists of mechanical and electronic components necessary to handle magnetic tape in such a manner that data can be reproduced from tape recorded on a NRZ1 digital tape transport or its equivalent and a tape can be generated from which data can be completely recovered when played back on a NRZ1 transport.

The Tape Unit consists of the following components.

(1) Power supply.

(2) Capstan drive system.

(3) Tape storage and reel servo systems.

(4) Magnetic write/read head and associated tape guides and cleaner.

(5) Data electronics.

(6) Control logic and interlock system.

4-2. ORGANIZATION OF TAPE UNIT

A highly modular construction has been adopted. All of the major components and subassemblies are interconnected by means of connectors rather than the more conventional wiring techniques.

Two printed circuit boards are employed; the first, the Tape Control A1 board, is mounted on hinged standoffs adjacent to the tape deck.

It contains the control logic, reel and capstan servo amplifiers, voltage regulators and photo-tab sensor amplifiers (see Figure 4-1). With the exception of the magnetic head, all of the deck-mounted components, motors, manual controls, tension arm position sensors, photo-tab sensors, etc., plug directly into locations at the hinged end of this board. A printed circuit edge connector carries interface signals to and from the board.

The second hinged board, the Data A1 board, is only concerned with writing and reading of data. Write data enters by means of a printed circuit edge connector at one end of the board; it is encoded and the result transmitted to the magnetic head through the connector in the middle of the board. Read signals pass in the same direction, this time from the head connector to the amplifiers, peak detectors, and transmitters (see Figure 4-1). Digital read signals are transmitted by means of a second interface edge connector.

DC power and three control levels are passed between the two boards via a single harness.

The harnesses from the three interface connectors are merged, strain relieved, and leave the transport.

4-3. FUNCTIONAL SUBSYSTEMS DESCRIPTION

4-4. POWER SUPPLY

Figure 4-2 is a block diagram of the power supply, which is in two parts. The first part, the power supply module with rectifiers, capacitors, transformer, power cord, etc., is fastened to the deck; it is connected to the second part, the +5- and -5-volt regulators, on the Tape Control A1 board by a 6-pin connector.

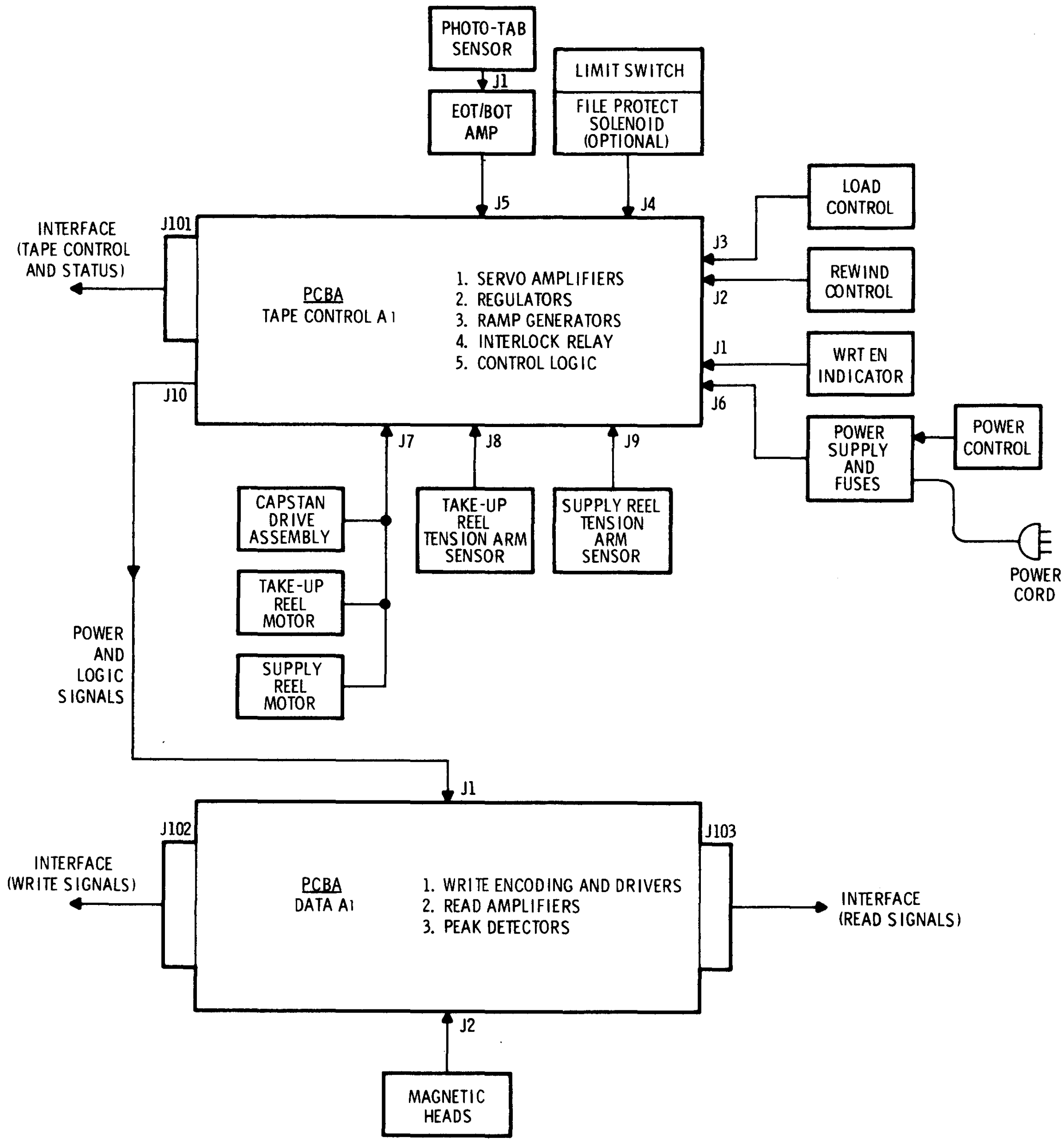


Figure 4-1. Organization of the Tape Unit

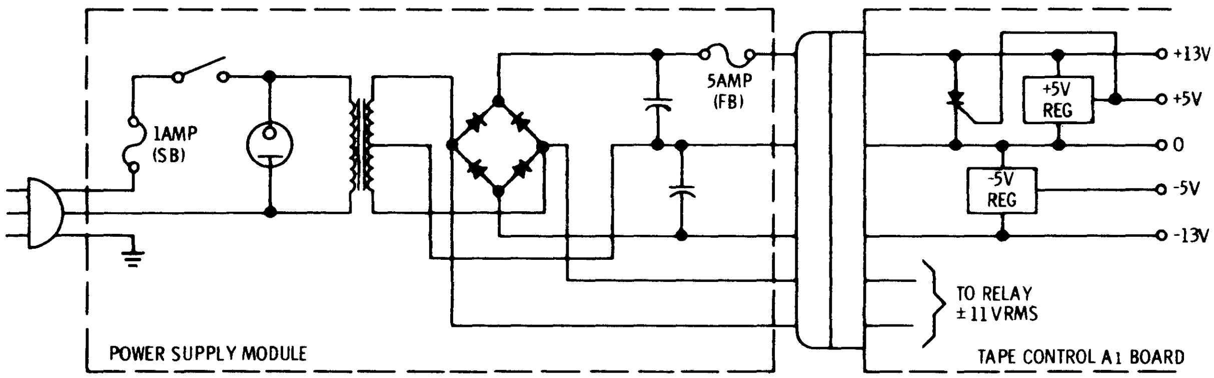


Figure 4-2. Block Diagram of Power Supplies

The transformer primary connections are shown in Figure 4-3 for several line voltages. The line voltage is connected across the transformer primary when the POWER control is depressed. The POWER control neon indicator is connected across terminals 1 and 2; i.e., 115 volts ac, independent of selected line voltage. Unregulated dc (at a nominal ±13 volts under load) is used to power the motors and voltage regulators. Two regulated supplies are generated. The ±5-volt supplies are adjusted and regulated within ±0.2 percent and can supply up to 2.0 amps. Since DTL integrated circuits are widely used, it is necessary to use an SCR for "crowbar" protection against overvoltage on the +5-volt line. The circuits used can withstand up to 12 volts for 1 second. When the +5-volt line rises to +8 volts, the SCR connected between +13 volts and 0 volt is turned on. This holds the voltage on the ICs down until the fuse opens a few milliseconds later.

4-5. CAPSTAN SERVO

Figure 4-4 is a block diagram of the capstan servo. It consists of two parts: the deck-mounted capstan drive assembly consisting of the motor-tachometer combination and the capstan, and the amplifier and ramp generators on the Tape Control A1 board. A relay contact disconnects the motor when tape tension is lost.

The tape is moved by the capstan whose velocity is determined by the velocity servo, and the output of one of the two ramp generators. If the Reverse ramp generator is selected by the logic, the voltage at R1 rises at a rate corresponding to the specified start time of the tape. The amplifier then accelerates the motor and the tape; the feedback voltage from the tachometer produces current in R4 which tends to reduce the amplifier input current produced by the ramp generator. The voltage at R1 stops rising after the specified start time and the velocity builds up to the point where the current in R4 approximately equals that in R1.

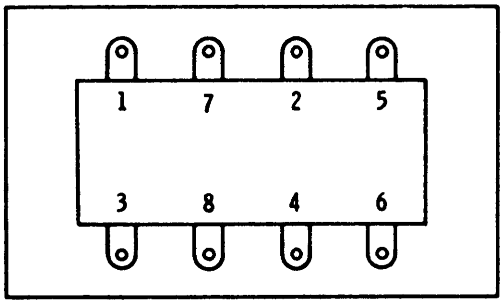


Table A

Line Voltage	Line Between	Lamp	Connect
100	4 and 7	5	7 to 8, 2 to 4
110	6 and 7	5	7 to 8, 5 to 6
115	4 and 1	2	1 to 3, 2 to 4
125	6 and 1	2	1 to 3, 5 to 6
200	4 and 7	5	2 to 8
208/210	6 and 7	5	2 to 8
220	6 and 7	5	5 to 8
230	4 and 1	2	2 to 3
240	6 and 1	2	2 to 3
250	6 and 1	2	3 to 5

Table B

Line Voltage	Line Between	Lamp	Connect
100	7 and 4	3	7 to 8, 2 to 4
110	7 and 6	8	7 to 8, 5 to 6
115	1 and 4	3	1 to 3, 2 to 4
125	1 and 6	8	1 to 3, 5 to 6
200	7 and 4	3	2 to 8
208/210	7 and 6	8	2 to 8
220	7 and 6	8	5 to 8
230	1 and 4	3	2 to 3
240	1 and 6	8	2 to 3
250	1 and 6	8	5 to 3

Note:

Transports have been shipped wired to either of the configurations shown in Table A and Table B.

To determine which table to use, note where the white power wire is connected. If the white wire is on Terminal 4 (for 115v ac) or Terminal 6 (for 240v ac), refer to Table A. If the white wire is on Terminal 1, refer to Table B.

Figure 4-3. Transformer Primary Connections

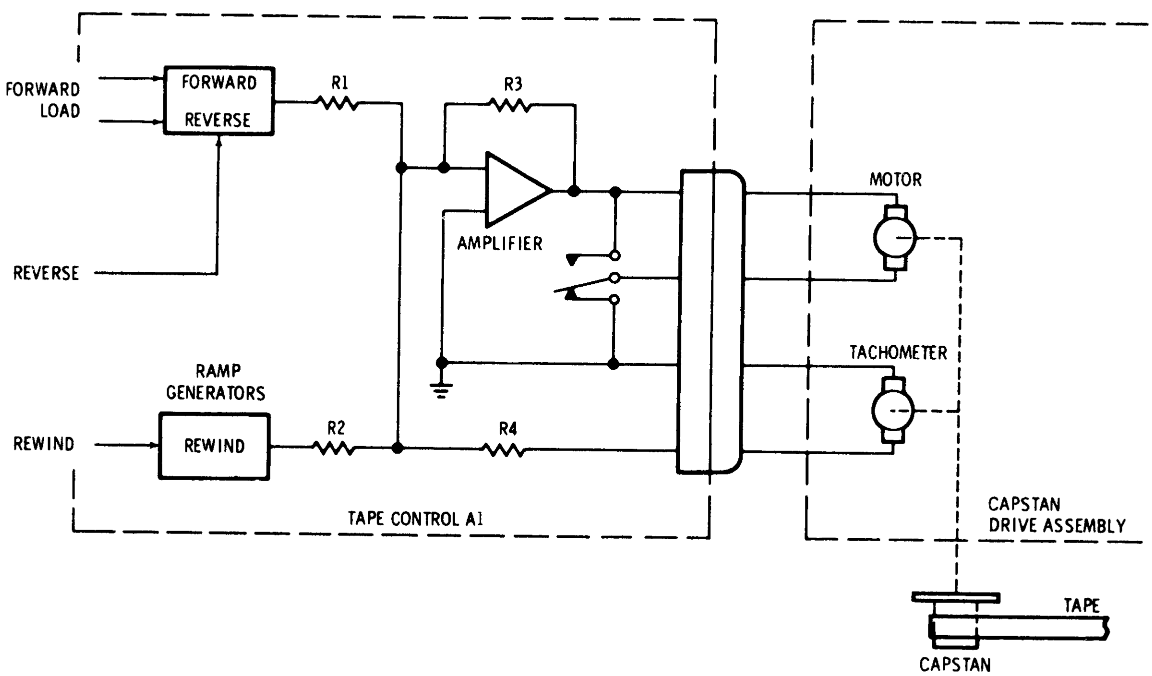


Figure 4-4. Capstan Servo Block Diagram

The Forward ramp generator is activated by the SYNCHRONOUS FORWARD command or a Load sequence. The Reverse ramp generator is activated by a SYNCHRONOUS REVERSE command and the Rewind ramp generator by a REWIND command, either remote or manual. When the transport is in the standby condition, neither ramp generator is activated. In this case, the capstan position is maintained by motor friction.

Both Forward and Reverse ramps rise and fall in a time calculated to produce a tape movement of 0.19 ±0.02 inch when the tape reaches the specified velocity; e.g., 30 milliseconds for a 12.5 ips transport.

The Rewind ramp rise and fall time is not critical; it is approximately 0.25 second and simply long enough to allow the reel servos to keep up with the rise or fall in tape speed. Typical waveforms are shown in Figure 4-5.

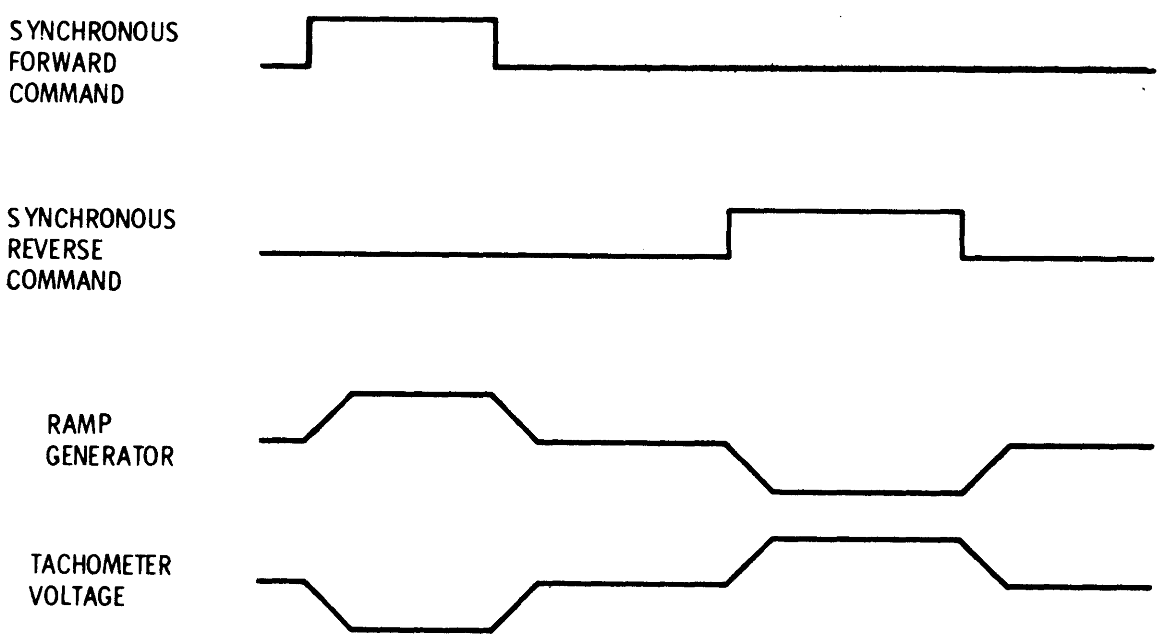


Figure 4-5. Typical Capstan Servo Waveforms

4-6. REEL SERVOS

Identical linear position servos control the supply and take-up of tape by the reels. Figure 4-6 is a diagram of one complete reel servo together with a part of a second and the relevant interconnections.

The components of the servo are: (1) tension-arm position sensor, (2) pulley, belt, tension arm, and tape reel, (3) reel motor, and (4) servo amplifier on the Tape Control A1 board.

The tension arms establish tape tension and isolate the inertia of the reels from the capstan. Low-friction ball bearing guides are used to minimize tape tension variations. The angular position of the tension arm is sensed by a photosensitive potentiometer which produces a voltage output proportional to the arm position. This output is amplified and drives the reel motor in the direction to center the tension arm. The geometry of the tension arm and spring ensures that only negligible tape tension changes occur as the storage arm moves through a 30-degree arc.

With the tape stationary, the storage arms take a position such that the amplified tension arm sensor output, when applied to the reel motor, produces enough torque to balance the spring torque. Initially, the sensor is set by rotating the shutter on the tension arm shaft so that the tension arms operate in the center of their range. The position of the tension arm changes for different steady-state capstan velocities. This occurs because the amplifier output varies with the motor back-emf, requiring corresponding changes in voltages from the potentiometer.

When the capstan injects a tape velocity transient in either direction, the arm moves and the sensor output changes, driving the reel motor in the direction to recenter the arm.

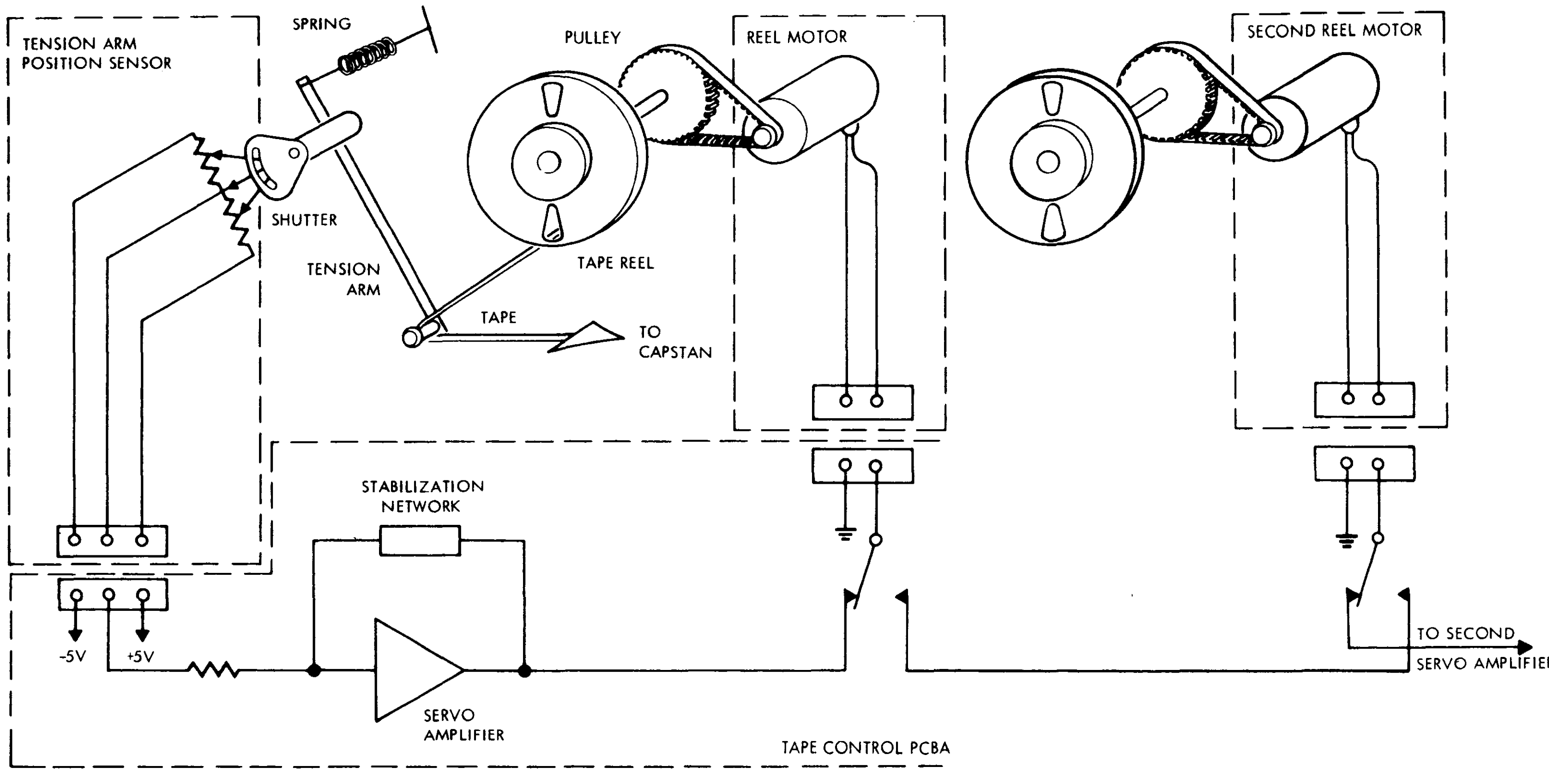


Figure 4-6. Reel Servo Diagram

Without tape, the arms rest against the stops and the tension-arm limit switch is open, removing power to all motors.

Each reel motor is driven by a linear amplifier with transitional lead servo stabilization. The low-frequency gain of the amplifier is 6 volts per volt. The zero of the stabilization network is at 1.5 Hz and the pole is at 7.5 Hz.

With 10 volts across the potentiometer, the gain is 3 volts per radian. The amplifier gain is 6 volts per volt and the motor gain is 15 radians/second/volt. The motor velocity is stepped down by a pulley ratio of 4 to 1, so that the open-loop gain (reel velocity divided by arm displacement) is 70 radians/second/radian. From this description, the arm displacement for the change in velocity from 12.5 ips forward to 12.5 ips reverse (i.e., 10 radians per second) is approximately 1/7 radian or 8 degrees. A voltage derived from the Rewind ramp generator is added to the feedback from the tension arm sensor. Therefore, displacement of the tension arm is not required to generate the amplifier output at 50 ips, thus minimizing the tension arm stroke requirement.

4-7. DATA ELECTRONICS

Information is recorded in the NRZI mode; i.e., a "1" on the information line causes a change of direction of magnetization between positive and negative saturation levels. Two tape formats are in general use. They are the NRZ1 7-track format which can operate at 200, 556, and 800 cpi, and the NRZ1 9-track format which operates at 800 cpi.

Figures 4-7 and 4-8 illustrate the relevant 9- and 7-track allocations and spacing. In the 9-track system, consecutive data channels are not allocated to consecutive tracks. This organization increases tape system reliability because the most used data channels are located

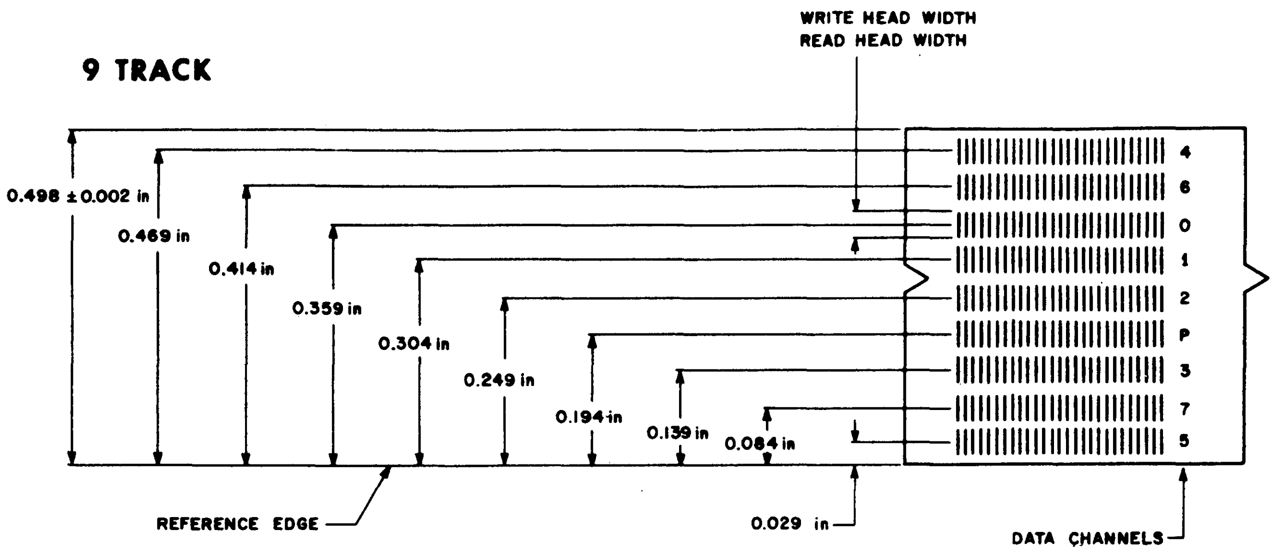


Figure 4-7. 9-Track Allocation and Spacing

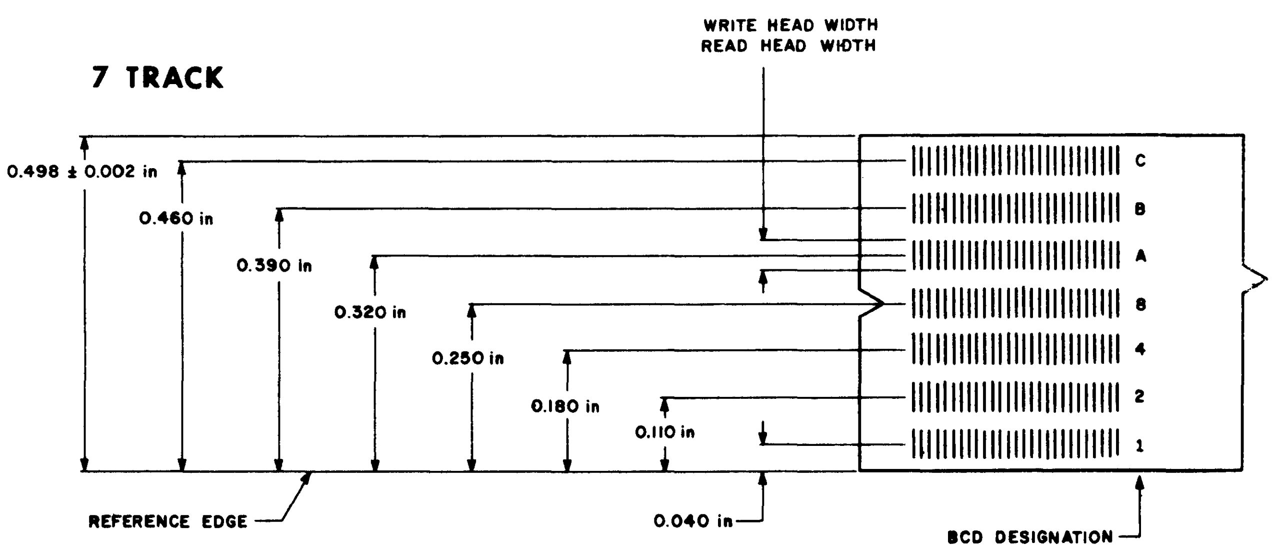


Figure 4-8. 7-Track Allocation and Spacing

near the center of the tape. Consequently, they are least subject to errors caused by contamination of the tape.

Illustrated in Figure 4-9 are waveforms that occur on a channel during a write operation; also shown are the read-back waveforms. Magnetization transitions recorded on the tape are not perfectly sharp because of the limited resolution of the magnetic recording process.

During reading, the amplifier read-back voltage is full-wave rectified (because no significance is attributable to the polarity of the read-back voltage) and clipped to remove baseline noise. This is necessary because there is no read signal output for a recorded "0". The output of the rectifier is peak detected and passed to the interface.

Figure 4-10 is a functional diagram of one channel of data electronics and is used only for purposes of describing system operation.

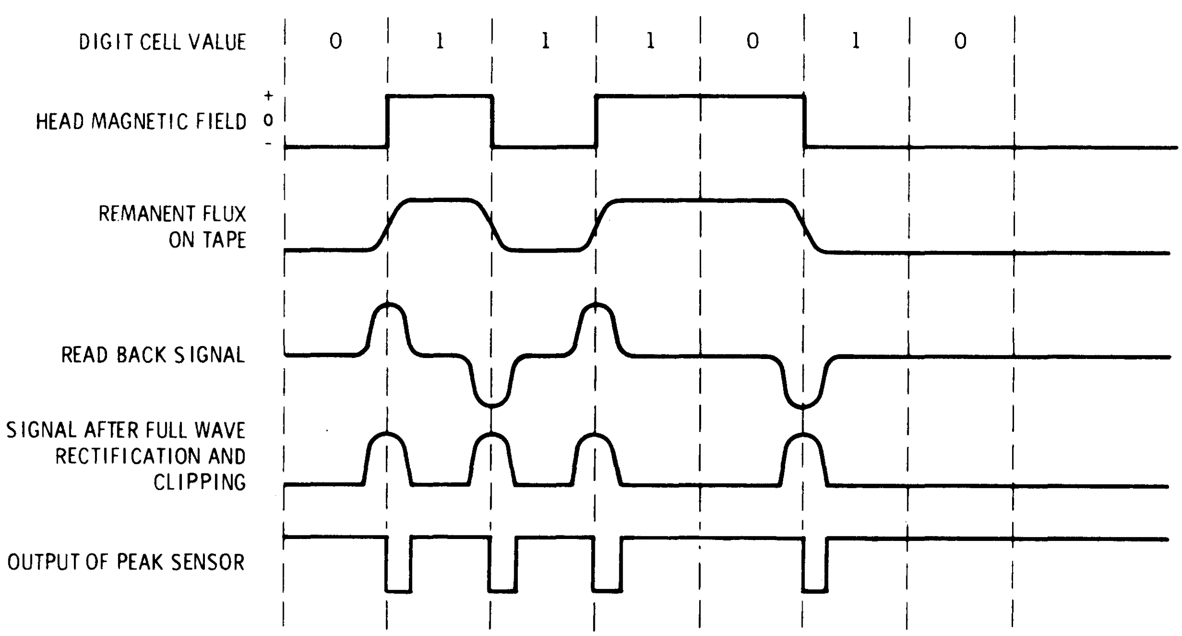


Figure 4-9. Write and Read Waveforms

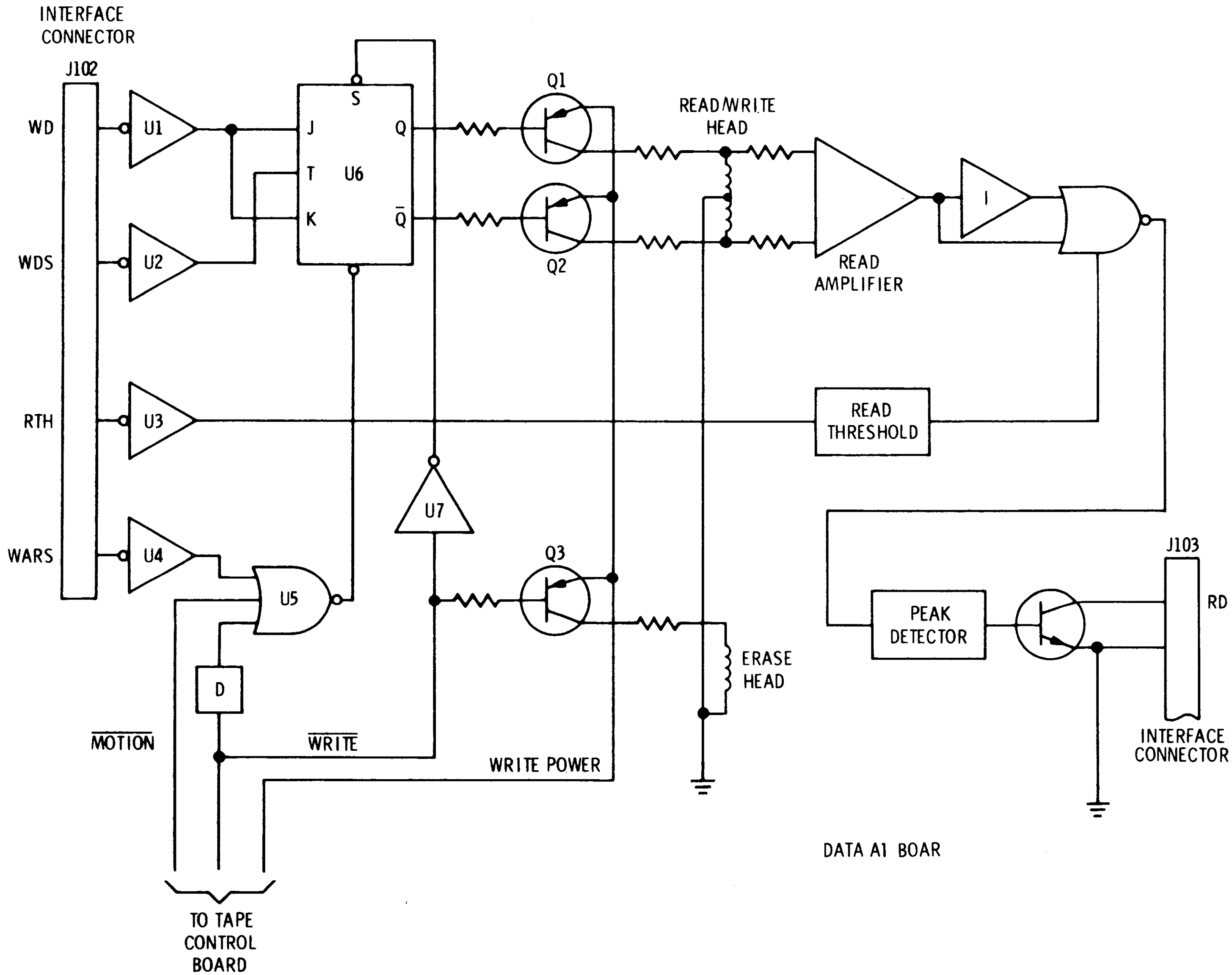


Figure 4-10. One Channel of Data Electronics

4-8. Data Recording

In operation, a SYNCHRONOUS FORWARD command (SFC) enables the ramp generator which causes the tape to accelerate to the prescribed velocity.

After a time determined by the required Inter-Record Gap (IRG) displacement, the WRITE DATA inputs together with WRITE DATA STROBEs (WDS) are supplied through the interface connector.

The WRITE DATA input is received by interface receiver U1 (see Figure 4-10) and, when true, enables both the J and K inputs of flip-flop U6. WDS signals are received by interface receiver U2 and will cause flip-flop U6 to change state on the trailing edge of the strobe, provided the WRITE DATA signal is true at this time.

The characteristics of the flip-flop are such that the WRITE DATA signal must be stable (in the appropriate direction) throughout the period of the strobe.

Both outputs of flip-flop U6 are fed to the head driver circuit, which causes current to flow in one half or the other half of the center-tapped head winding. Consequently, magnetization on the tape is maintained in the appropriate direction between changeovers and changes direction for each "1" bit to be recorded (as required by the NRZ1 format).

At the end of each record, check characters have to be recorded and an IRG inserted. Figures 4-11 and 4-12 show the IRG format for 9- and 7-track systems.

In a 9-track system, both a CRCC and LRCC are written. The CRCC is supplied by the customer to the interface, together with

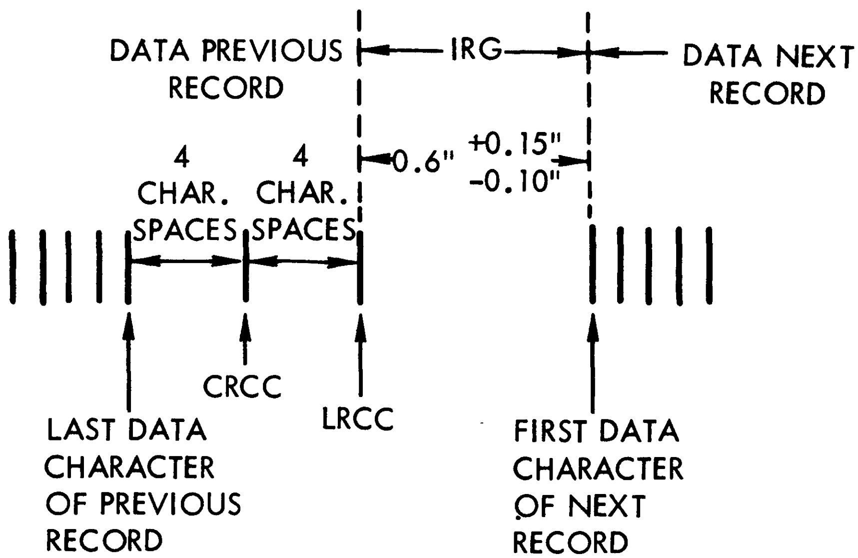


Figure 4-11. .9-Track IRG Format

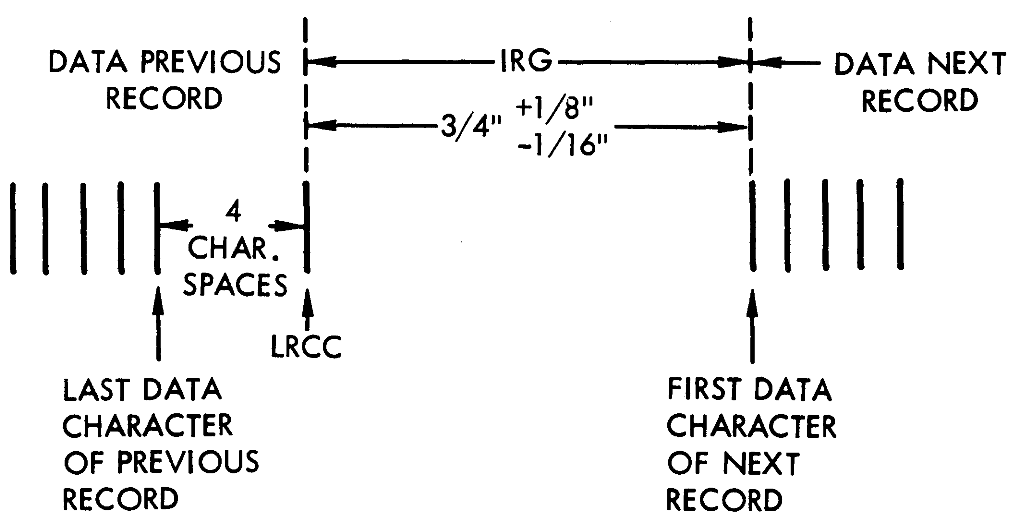


Figure 4-12. 7-Track IRG Format

a single WDS signal whose trailing edge is separated by four character times from that of the last WDS. The LRCC is written by resetting all the write flip-flops with OR gate U5, using the WRITE AMPLIFIER RESET signal (IWARS) received by interface receiver U4. The write flip-flops are reset on the leading edge of WARS, which should be separated by eight character times from the trailing edge of the last WDS.

The LRCC is written such that the total number of magnetization transitions in any track is even.

In a 7-track system, only the LRCC is written; this is achieved by the WARS. In this case, the leading edge must be separated four character times from the trailing edge of the last WDS.

When the LRCC has been recorded, the SFC goes false, the ramp generator is disabled, and the tape decelerates to zero velocity.

The IRG displacement consists of the following.

(1) The stop distance: the distance traveled during the tape deceleration period to zero velocity.

(2) The start distance: the distance traveled while the tape is accelerating to the prescribed velocity.

(3) An additional distance determined by the time T, from SFC going true to the time of the first WDS.

Time delay T is provided by the customer's controller.

To separate files of information on tape, a File Gap is used. This is identified by a special character on the tape followed by its LRCC. Figures 4-13 and 4-14 describe the IRG File Gap* format for 9- and 7-track systems.

*Commonly referred to as Interrecord Gap or IRG.

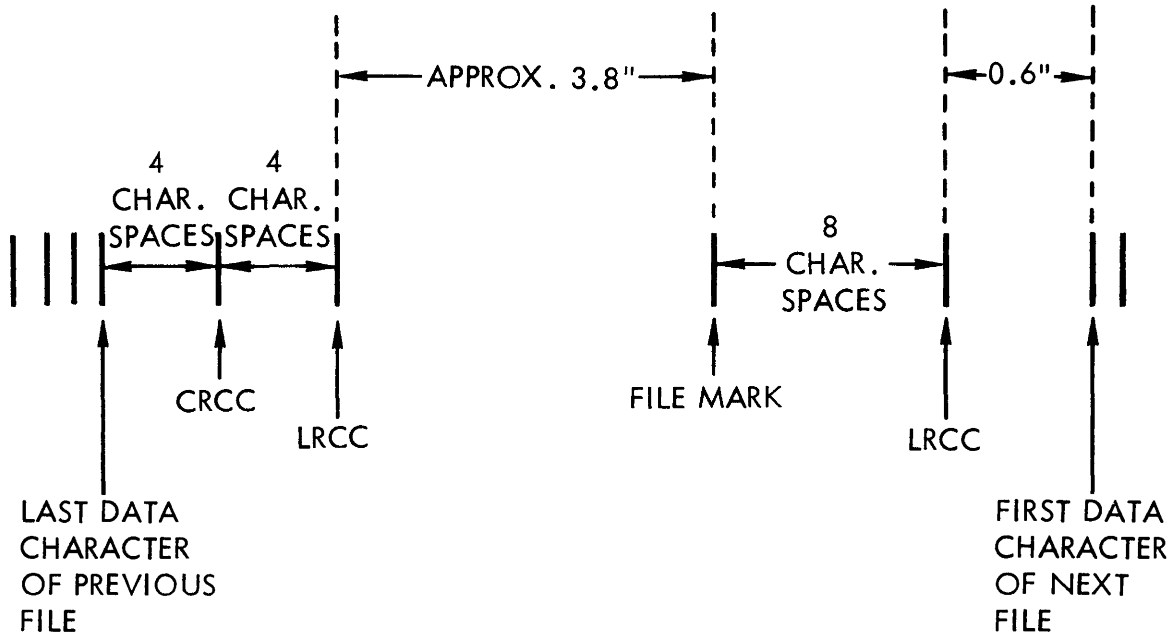


Figure 4-13. 9-Track File Gap Format

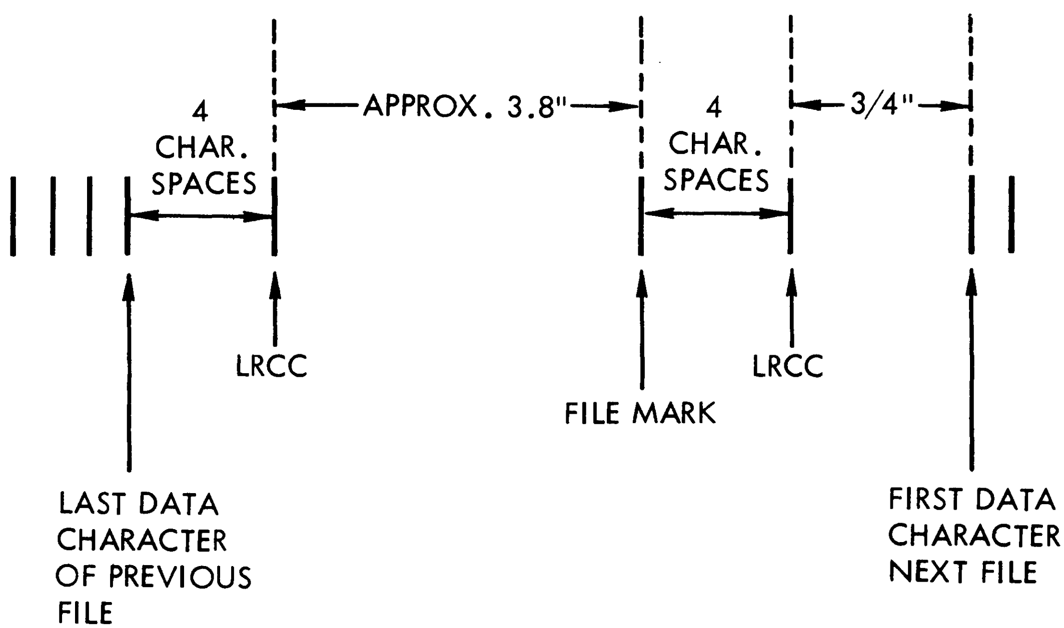


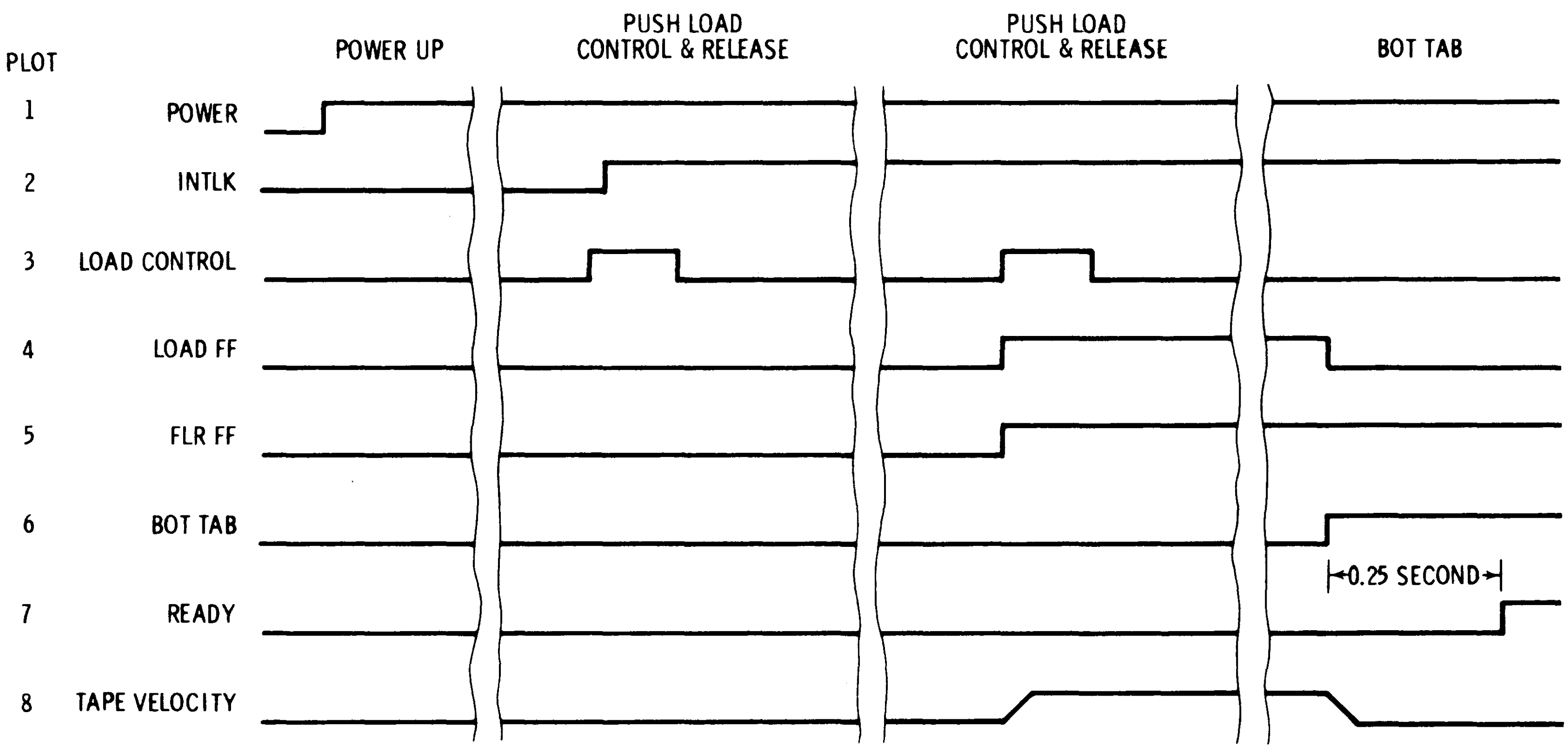
Figure 4-14. 7-Track File Gap Format

A File Gap is inserted under external control by the customer's controller. An SFC is given, followed at the appropriate time by the File Mark character (a "1" in data bit positions WD4, 5, 6, and 7 for 7-track systems and a "1" in data bit positions WD3, 6, and 7 for 9-track systems), together with its WDS followed by the LRCC (written using WARS) after four character times in a 7-track system and after eight character times in a 9-track system.

4-9. Data Reproduction

When an SFC is received the Forward ramp generator is enabled and the tape accelerates to the prescribed velocity. Data signals from the magnetic head at a level of approximately 5 millivolts peak-to-peak are transmitted by a shielded cable to the connector on the Data A1 board. When the transport is in the Read mode, both Q1 and Q2 (see Figure 4-10) are cut off. The read amplifier boosts the signal level to 12 volts peak-to-peak. The signal is full-wave rectified and base-line clipped. The clip level is variable and controlled by the READ THRESHOLD (RTH) interface line. A false level results in a clip level of approximately 20 percent and should be used when reading a pre-recorded tape. A true level results in a clip level of approximately 50 percent and should be used when performing a read-after-write check. The high clip level ensures that data are written with enough margin to ensure data recovery when the tape is read on another transport.

After clipping, the signal is differentiated to detect the peaks which correspond to the flux transitions on the tape. The peak-detected signal is squared and passed to the interface transmitters. A "1" signal



NOTE: 1. HIGH LEVEL IS TRUE

Figure 4-16. Tape Control Waveforms During Load Sequence

The write lockout (WLO) switch is located on the File Protect assembly located behind the supply reel. The switch is closed when a Write Enable ring is mounted on the supply reel. The probe, which detects the Write Enable ring, is retracted when power is switched on and K1D is closed. A solenoid whose transistor driver is supplied with base current through the WLO switch and K1D retracts the probe.

Write current is also supplied on demand through K1D, the WLO switch and the write enable circuitry.

The File Protect facility is optional equipment designed to protect a tape file from inadvertent erasure. Where it is omitted, the WLO switch is replaced by a jumper wire.

4-12. Actuate Power Control

After power is initially turned on (Plot 1), the relay contacts and tension-arm limit switch are open. The INTLK signal is low and is connected either directly or through an "OR" gate to the RESET inputs of the four control flip-flops, RW1, RW2, Load, and FLR.

4-13. Depress LOAD Control (First Time)

When the LOAD control is depressed for the first time (Plot 3), the relay driver for K1 is energized, the four contacts close, activating the reel servos which tension the tape, thus closing the tension-arm limit switch. The tension-arm limit switch supplies an alternate source of base current for the relay driver, thus latching the relay (which remains activated after the LOAD control is released). When K1D closes, a high level appears at the INTLK output (Plot 2), removing the reset from the control flip-flops. The Load flip-flop is not set by the first operation of the LOAD control because at the time its C input goes low (which would normally set the flip-flop) the INTLK signal is still holding the reset input low (the closure of the relay contacts is delayed from the appearance of the command level by two or three milliseconds while the relay contacts close).

If, at any time, the tension arm moves outside its operating region, the interlock relay de-energizes. This removes the power from the motors, and the INTLK signal returns to the low state, resetting the four control flip-flops.

4-14. Depress LOAD Control (Second Time)

The following sequence of events occur when the LOAD control is momentarily depressed a second time (Plot 3).

(1) Since the INTLK signal is high, the Load flip-flop sets (Plot 4). The false or $\overline{Q}$ output of the Load flip-flop is connected to the Forward ramp generator (not shown in Figure 4-15) which requires a low-true input. Therefore, the ramp generator which drives the capstan servo is enabled. Setting the load flip-flop causes the FLR flip-flop to set (Plot 5).

(2) The tape accelerates to the specified velocity (Plot 8) and advances until the BOT photo-tab sensor is detected.

(3) When the BOT photo-tab sensor is detected, the BOT signal (Plot 6) goes high, enabling the AND gate and resetting the Load flip-flop (Plot 4).

(4) The tape decelerates to rest with the photo-tab under the photo-tab sensor.

(5) The Q output of the FLR flip-flop enables the READY "AND" gate. Resetting the Load flip-flop causes the NBUSY signal to go high. The set output of the FLR flip-flop, in conjunction

with the NBUSY signal and the NBOTD signal going high, causes the READY line (Plot 7) to go true after a 0.25-second delay. The LOAD POINT line is also true at this time.

(6) The setting of the FLR flip-flop disables the "AND" gate used to set the Load flip-flop from the Load Control, thus eliminating the possibility of further manual LOAD commands.

The Tape Unit is now ready to receive external commands. A low signal on the SFC interface line will cause the transport to move tape at the prescribed velocity. A low signal on the SRC interface line will then cause the transport to move tape back to the Load Point where tape motion is automatically halted. Upon encountering the BOT tab, the READY line is dropped for the duration of the 0.25-second delay.

4-15. Rewind Sequence

4-16. Case 1 — Tape Not at Load Point

This is the normal rewind to Load Point sequence that results from either a remote or local command. Figure 4-17 shows the waveforms that occur during the operation.

In response to either a remote or a local command, the RW1 flip-flop is set (Plot 1). The $\overline{Q}$ output of this flip-flop enables the Rewind ramp generator and the tape accelerates to a reverse velocity of 50 ips with a 0.25-second start time (Plot 8). The NBUSY gate is disabled by the setting of the RW1 flip-flop, thus disabling the READY "AND" gate and causing the READY signal to go low (Plot 7).

When the leading edge of the BOT tab is detected (Plot 3), flip-flop RW2 sets (Plot 2). The single-shot is triggered and the 0.25-second

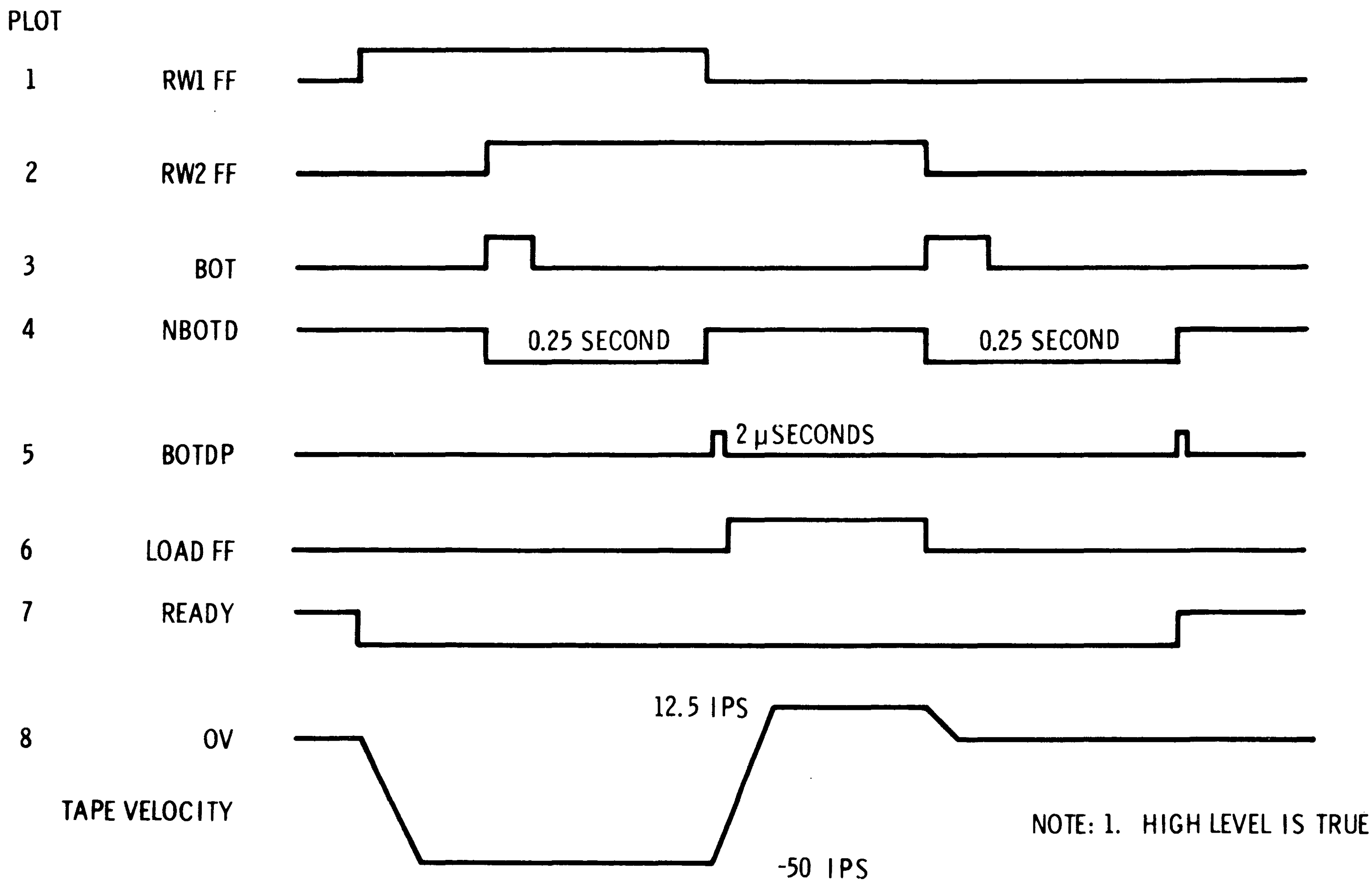


Figure 4-17. Tape Control Waveforms During Rewind to Load Point Sequence

NBOTD pulse is started (Plot 4). At the trailing edge of the 0.25-second delay, a BOTDP pulse is generated (Plot 5). This pulse is gated with the RW2 level and resets flip-flop RW1, which causes the Rewind ramp to begin to fall; also, the Load flip-flop is set (Plot 6), which causes the Forward ramp to begin to rise. The net effect of the interacting ramp inputs to the capstan servo is that the tape velocity goes from 50 ips reverse to the specified forward velocity within about 0.25 second. The timing characteristics of the ramp generators are such that the tape overshoots the BOT tab in the reverse direction and subsequently goes forward until the BOT tab is detected the second time. The leading edge of the tab causes the reset of both the Load and RW2 flip-flops. The network that delays the LOAD input to the gate is used to ensure the reset of both flip-flops. The Tape Unit READY line goes true again after the 0.25-second delay.

4-17. Case 2 — Tape at Load Point

A manual REWIND command initiates the Rewind sequence as previously described. However, in this case, the tape unwinds from the take-up reel and tape tension is lost. Remote rewind commands are inhibited by the NBOT waveform; i.e., it is impossible to unload tape remotely — operator intervention is required.

4.18. Introduction to Read after Write Units

The following pages are detailed operation of circuits utilized by "dual gap" units. "Single gap" units used different data boards with additional circuitry for the Read while writing capabilities of a dual gap head. The "7" channel and "9" channel "Read after Write" Units are identical in operation with circuitry for two additional channels available on the 9 track data board. There are several "data" boards and control boards available. The following descriptions are given to clarify the different boards.

Data "A1" (-03 on Assembly Drawing) for 9 track single gap.
Data "A1" (-04 on A sembly Drawing) for 7 track single gap.
Data "B1" (-01 on Assembly Drawing) for 7 track unit selectable
Data "C19" (-01 on Assembly Drawing) for 9 track dual gap
Data "C17" (-01 on Assembly Drawing) for 7 track dual gap
Control "A1" (-02 on Assembly Drawing) for all non-selectable units
Control "B2" (-01 on Assembly Drawing) for all selectable units.

Schematics and assembly drawings are located in Section VII.

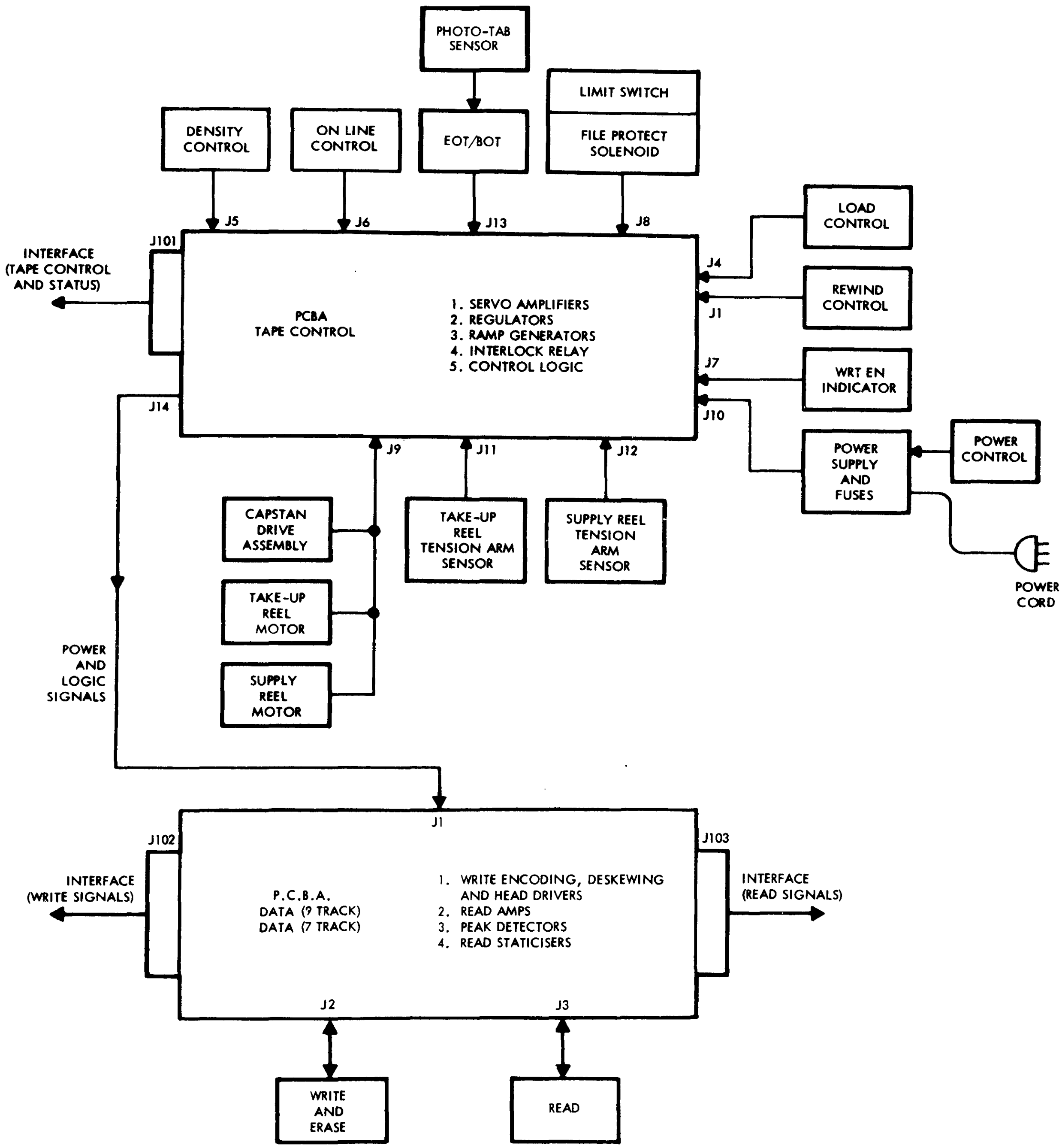


FIGURE 4-18
ORGANIZATION OF DUAL GAP TRANSPORT

4-19. Operation with a Dual-Gap Head

This transport utilizes a dual-gap head which enables simultaneous read and write operations to take place, thus allowing writing and checking of data in a single pass.

Gap scatter in both the write and read heads is held within tight limits so that correction is not necessary. Conversely, the azimuth angle of both heads is not held within such tight limits and correction is therefore necessary.

The read head azimuth adjustment is provided by shimming the fixed head guides adjacent to the head so that the tape tracks at 90 degrees to the read head azimuth. Since the write and read heads are constructed in the same block, an independent method of azimuth adjustment is required for the write head. This is achieved electronically by triggering the write waveform generators for different channels sequentially and at such times that the azimuth error in the write head is nullified.

4-20. Data Recording

Figure 4-22 shows a timing diagram for data recording. Assume that the transport is Selected, Ready, On-line, and has a Write Enable ring installed. The WRT PWR control line will therefore be at approximately +5 volts, providing power for the head driver circuits.

When a SYNCHRONOUS FORWARD command (SFC) is received, the MOTION signal generated on the Tape Control circuit board goes high, removing one input of OR gate U8.

In operation, the front edge of the SFC is delayed and differentiated and the resulting pulse used to sample the condition of the SET WRITE STATUS (SWS) line. If this is true, the following action takes place.

(1) The Write/Read mode flip-flop (U20, see Paragraph 4-11) is set.

(2) The NWRT waveform becomes low.

(3) Erase driver Q3 is energized.

(4) Both the S_D and C_D inputs of flip-flop U4 go high. The action of the "Stretcher" circuit is to delay the rise of the C_D input relative to the S_D input ensuring that the flip-flop is in the reset state before recording commences.

The polarity of the field from the erase and write heads under these conditions is such that tape will be erased in an NRZ compatible direction.

(5) The C_D input of control flip-flop U9 goes high, unclamping the flip-flop.

The SYNCHRONOUS FORWARD command (Plot 1) also enables the ramp generator, which causes the tape to accelerate to the prescribed velocity (Plot 2). After a time (T1) determined by the required inter-record gap (IRG) displacement, the WRITE DATA (WD) inputs together with the WRITE DATA STROBE (WDS) are supplied to the interface connector.

The WRITE DATA (IWD*) input is received by interface receiver U1 and, when true, enables one input of AND gate U2. The IWDS pulse is received by interface receiver U5 and fed to AND gate U2. The output of gate U2 is thus a positive-going pulse at WDS time whose leading edge enables the J input of the J-K write waveform generator flip-flop U4 directly, and the K input of the flip-flop via OR gate U3. Since the clock input of U4 is high at this time, the master section of U4 is toggled whenever the IWD signal is true.

Each WDS (Plot 3) is also fed to flip-flop U9 which is set on the trailing edge (Plot 4). This unclamps the oscillator, which then generates a series of pulses at a high frequency (Plot 5). The pulses are fed to the shift register, which produces 10 negative-going outputs consecutively on 10 wires.

The nine outputs (T1 through T9) are used to toggle the output (slave) sections of the write waveform generator flip-flops (U4 typically) in the appropriate time order so as to achieve azimuth deskewing of the recording system. Plots 6 and 7 show the write current in the WD5 and WD2 channels for a 9-track system. The tenth output (T10) resets flip-flop U9, terminating the sequence of events. In practice, the oscillator frequency is adjusted to compensate for the azimuth error in the particular head being used.

Both outputs of flip-flop U4 are fed to head driver transistors Q1 and Q2, which cause current to flow in one half or the other of the center-tapped head winding. Consequently, magnetization on the tape is maintained in the appropriate direction between changeovers and changes direction for each "1" bit to be recorded (as required by the NRZ format).

All interface lines connecting the transport to the controller are prefixed by "I".

In a 9-track system, both a CRCC and LRCC are written. The CRCC is supplied by the customer to the interface, together with a single WRITE DATA STROBE (WDS) signal whose trailing edge is separated by four character times from the trailing edge of the last WDS. The LRCC is written by resetting all the write waveform generator flip-flops using the WRITE AMPLIFIER RESET (IWARS) signal received by interface receiver U6. The timing of this reset operation is controlled by the leading edge of the WARS signal, which should be separated by eight character times from the trailing edge of the last WDS (Plot 8).

The output of U6 is fed to OR gate U3 and the positive-going output is fed to the K inputs of the write waveform generator flip-flops (typically U4) and resets the master sections of these flip-flops. In addition, the leading edge of the WRITE AMPLIFIER RESET (WARS) signal is differentiated and sets flip-flop U9. A sequence of pulses is produced as described which toggles the write waveform generator flip-flops to the reset state in the appropriate order. The LRCC is written such that the total number of magnetization transitions in any track is even.

In a 7-track system, only the LRCC is written; this is achieved again by the WARS signal. Consequently, the leading edge must be separated four character times from the trailing edge of the last WDS.

When the LRCC has been recorded, the SFC goes false after the post-record delay time (T2), the ramp generator is disabled and the tape decelerates to zero velocity.

The IRG displacement consists of the following.

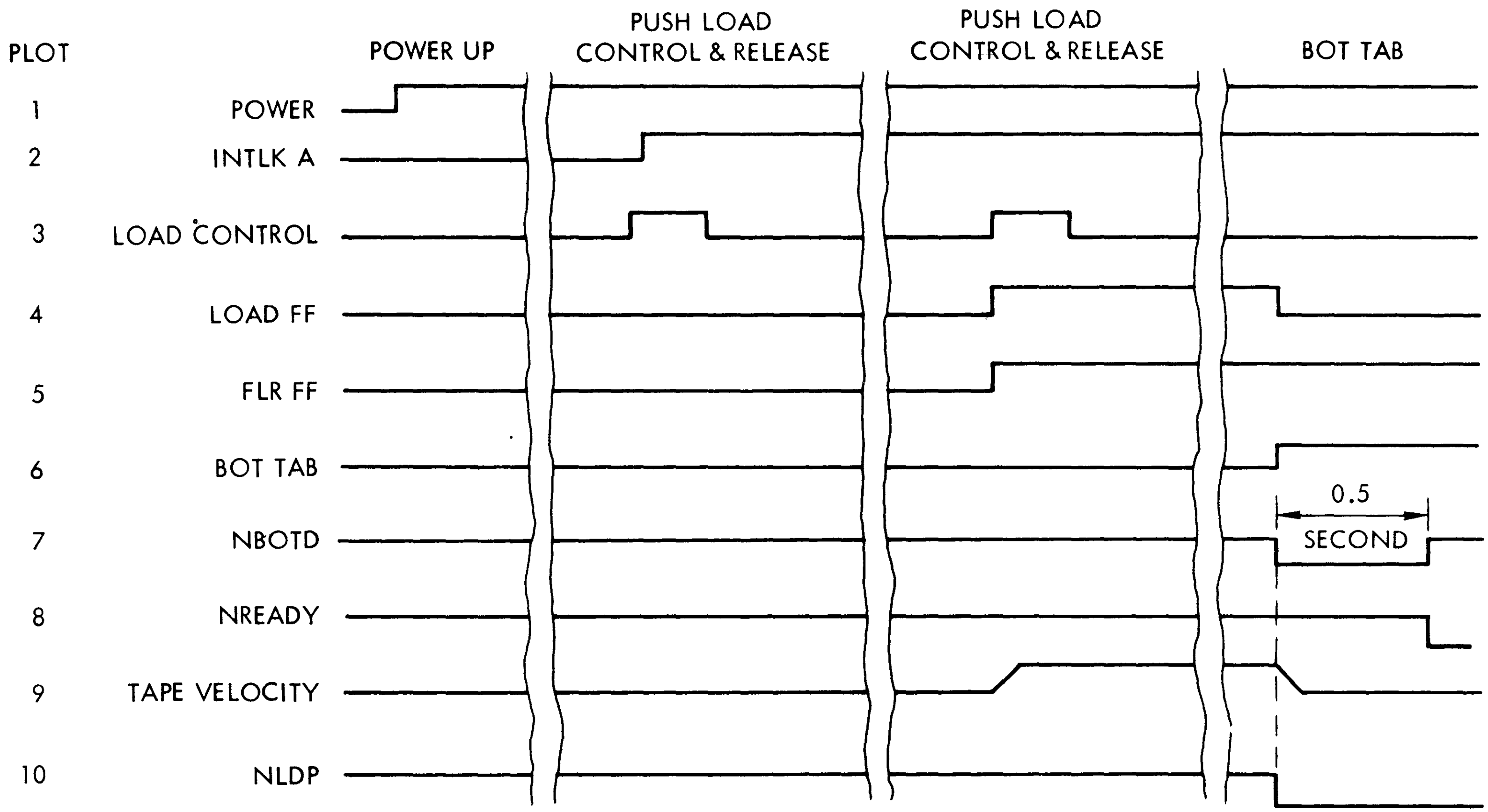
(1) The stop distance: the distance traveled during the tape deceleration period to zero velocity.

(2) The start distance: the distance traveled while the tape is accelerating to the prescribed velocity.

(3) An additional distance determined by the pre-record time (T1), from the SYNCHRONOUS FORWARD command going true to the time of the first WDS and the post-record time (T2) from the LRCC to the SFC going false. (Time delays T1 and T2 are provided by the customer's controller.)

To separate files of information on tape, a file gap is used. This is identified by a special character on the tape followed by its LRCC. Figures 4-11 and 4-12 describe the NRZ file gap formats for 9- and 7-track systems.

A file gap is inserted under external control by the customer controller. A SYNCHRONOUS FORWARD command is given, followed at the appropriate time by the File Mark character (a "1" in data bit positions WD4, 5, 6, and 7 for 7-track systems and a "1" in data bit positions WD3, 6, and 7 for 9-track systems), together with its WDS, followed by the LRCC (written using the WARS) after four character times in a 7-track system and after eight character times in a 9-track system.



NOTES:
1. HIGH LEVEL IS TRUE

Figure 4- 19. Tape Control Waveforms During Load Sequence

4-21. TAPE CONTROL SYSTEM

The second major electronic subsystem consists of the circuits necessary to control tape motion. This includes manual controls, interlocks, and logic. The operation can best be described by detailing the Bring-to-Load Point sequence, subsequent tape motion commands, the Rewind sequence, and subsequent unloading of the tape.

Figure 4- 24 is a logic diagram for the Tape Control system. Note that the identification of the elements in Figure 4- 24 is closely related to the Tape Control schematic. One-hundred percent correspondence is not possible since the schematic contains many functions which are only represented in simplified form in Figure 4- 24.

4-22. Bring-to-Load-Point Sequence

The system will be described by considering the sequence required to bring a tape to the BOT (Load Point). Figure 4-19 shows the waveforms during the operation.

Associated with each of the momentary manual control switches is a "switch clean-up" flip-flop (U13-C, U11-B, U1-D) which eliminates the problems of switch contact bounce. Relay K1 has four changeover contacts, three of which (K1A, K1B, and K1C) are used to disconnect the reel and capstan servo motors, the fourth (K1D) is used in conjunction with the tension-arm limit switch as a system interlock. The tension-arm limit switch is operated by a cam on the take-up reel tension arm and is closed when the arm is in its normal operating position. The tension-arm limit switch opens at both extremes of the arm travel so that protection against over-tension as well as under-tension conditions is provided.

The Write Lockout (WLO) switch is located on the File Protect assembly located behind the supply reel. The switch is closed when a

4-23. Depress LOAD Control (Second Time)

When the LOAD control is depressed momentarily a second time (Plot 3), the following sequence occurs.

(1) Since the INTLK A signal is high, the Load flip-flop sets and its Q output goes high enabling the Forward ramp generator (not shown) that drives the capstan servo. The tape accelerates to the specified speed (Plot 9) and continues to move until the BOT tab reaches the BOT sensor, at which time the BOT signal goes high, enabling one input of AND gate U20-B. Also, the single-shot is triggered, generating an 0.5-second negative-going waveform (NBOTD) (Plot 7).

(2) Since the LOAD waveform and the NRW1 waveform are high at this time, AND gate U20-B is enabled (Plot 10) and the Load flip-flop is reset. This causes the tape to decelerate to rest with the photo-tab under the photo-tab sensor.

At this time, all three inputs to AND gate U22-B are high so that the ILDP waveform is low, indicating that the transport is at Load Point; the Load lamp driver is enabled.

At the end of the 0.5-second delay, the NBOTD waveform goes high and, since the other inputs to gate U22-A are high at this time, the NREADY waveform at the output of gate U22-A goes low (Plot 8), enabling one input to AND gate U13-B.

(3) The setting of the FLR flip-flop causes the NFLR waveform to go low, disabling AND gate U17-A which inhibits the possibility of action from further manual LOAD commands.

Write Enable ring is mounted on the supply reel. The probe, which detects the Write Enable ring, is retracted when power is switched on and relay K1 is closed. A solenoid, whose transistor driver is supplied with base current when the LOAD control is depressed or the tension arm limit switch is closed, retracts the probe.

Write current is also supplied upon demand through K1D and the WLO switch.

4-24. Actuate Power Control

When power is turned on initially (Plot 1), the relay contacts and the tension-arm limit switch are open. The INTLK A signal is low and is connected either directly or through appropriate gates to the reset inputs of the five control flip-flops RW1, RW2, On-line, Load, and FLR (U14-A, U15-B, U9-B, U15-A, and U17-C).

4-25. Depress LOAD Control (First Time)

When the LOAD control is depressed for the first time (Plot 3), the relay driver for K1 is energized, the four contacts close, activating the reel servos which tension the tape, thus closing the tension-arm limit switch. The tension-arm limit switch supplies an alternate source of base current for the relay driver, thus latching the relay (which then remains activated after the LOAD control is released). When K1D closes, a high level appears at the INTLK A output (Plot 2), removing the reset from the control flip-flops. The Load flip-flop U15-A is not set by the first operation of the LOAD control because at the time that the T input of U15-A goes low (which normally sets the flip-flop), the INTLK A signal is still holding the reset input low.

If, at any time, the tension arm moves outside its operating region, the interlock relay de-energizes, power is disconnected from the motors, and the INTLK A signal returns to the low state, resetting the five control flip-flops.

4-26. Depress ON LINE Control

If the ON LINE control is momentarily depressed, the on-line flip-flop U9-B is set (if it is depressed a second time, U9-B is reset), enabling the second input of AND gate U13-B. The $\overline{Q}$ output of flip-flop U9-B enables the on line lamp driver. The output of Gate U3-B goes low, indicating that the transport is ready. If the transport is selected, the output of inverter U4-C (Selected, Ready, On-line (SRO)) goes high.

Whenever the transport is On-line the manual REWIND control is disabled by gate U6-B.

If the transport is Selected, the ISLT waveform is low and the SLT waveform goes high-true. The status lines are gated with the SLT waveform.

Whenever the FLR or INTLK A waveforms are low, the on-line flip-flop is held reset by OR gate U11-C, ensuring that the on-line flip-flop cannot be set until the interlock has been made and the First-Load-or-Rewind (FLR) sequence has been entered.

The on-line flip-flop can be reset from the interface by the OFF LINE command (OFFC) via interface receiver U10-D.

The transport is now ready to receive external commands.

4-27. Operation From External Commands

Assuming the transport is Selected, Ready, and On-line (SRO is high), receipt of a SYNCHRONOUS FORWARD command will cause the output of interface receiver U4-D to go high and the output of AND gate U12-C to go low. The MOTION signal will go high and the Forward ramp generator will be enabled.

The MOTION signal is delayed approximately 10 μseconds, differentiated, and a positive-going "GO" pulse generated at the output of differentiator $\delta 1$. This pulse samples the status of the SET WRITE STATUS (ISWS) line. If ISWS is true, indicating that the Write mode is required, then the Write/Read flip-flop U14-B is set and the NWRT waveform goes low. If ISWS is false, flip-flop U14-B is held reset and the NWRT waveform is high. In the case of a SYNCHRONOUS REVERSE command, a similar sequence of events occurs.

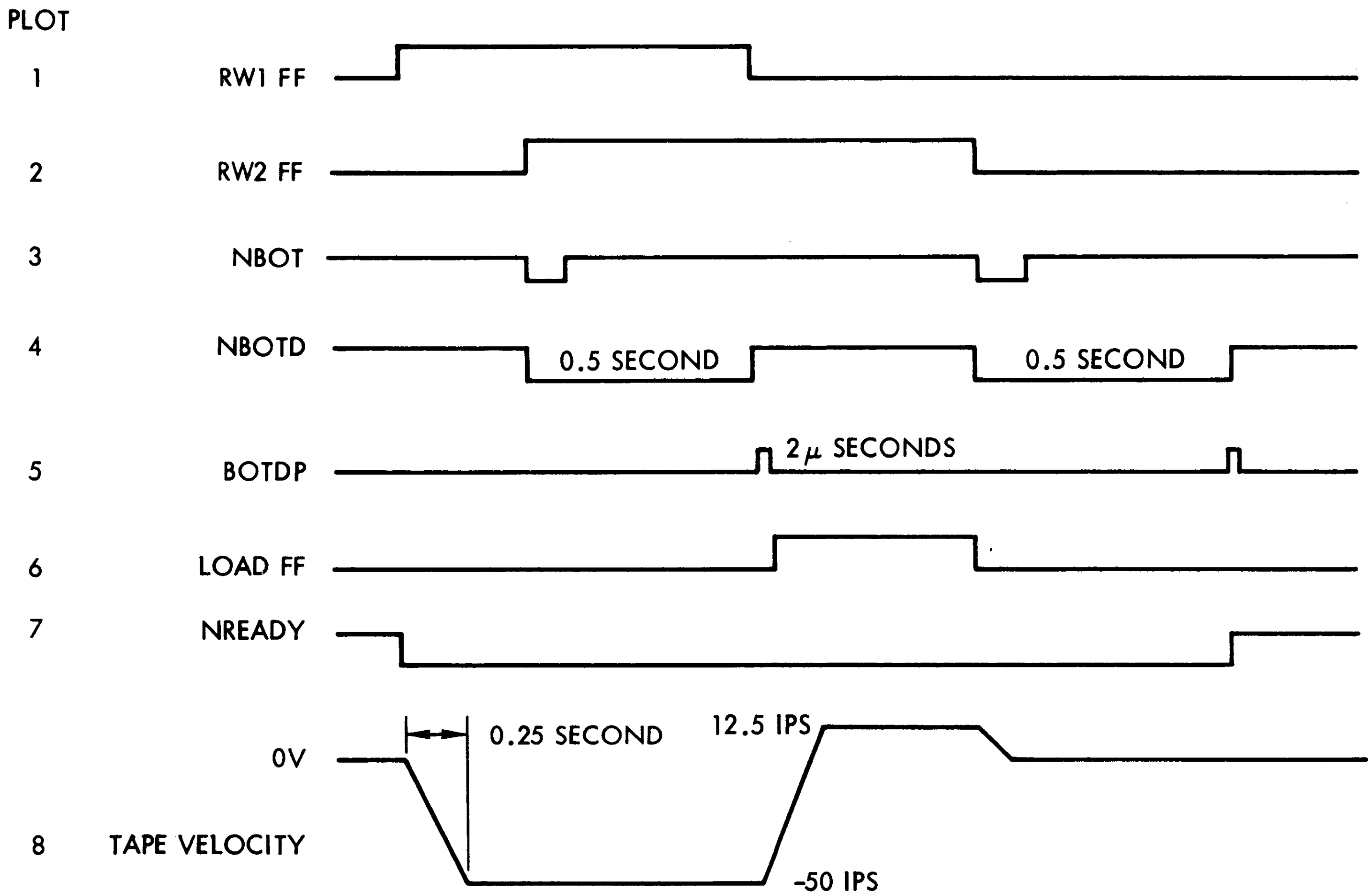
If the BOT tab is encountered during the execution of a SYNCHRONOUS REVERSE command, the BOT signal goes high, and the single-shot is triggered. As a result, AND gate U12-D is disabled, inhibiting the action of the SYNCHRONOUS REVERSE command. The NBOTD waveform goes low for 0.5 second so that the transport becomes Not Ready (via gates U22-A, U13-B, and U3-B) for this period of time.

4-28. <u>Operation From Control Panel (Rewind Sequence)</u>

4-29. Case 1 — Tape Not at Load Point

This is the normal Rewind-to-Load Point sequence that results from either a remote or manual command. Figure 4-19 shows the waveforms that occur during the operation.

In response to either a remote or manual REWIND command given the correct conditions, the RW1 flip-flop U14-A is set (Plot 1). The $\overline{Q}$ output of the flip-flop enables the Rewind ramp generator and the tape accelerates to a reverse velocity of 50 ips in approximately 0.25 second (Plot 8).



NOTES:
1. HIGH LEVEL IS TRUE

Figure 4-20. Tape Control Waveforms During Rewind to Load Point Sequence

When the BOT tab is detected, flip-flop RW2 (U15-B) is set on the leading edge of the NBOT waveform (Plot 3). The 0.5-second single-shot is triggered (Plot 4). At the end of the 0.5-second delay, the trailing edge of the NBOTD waveform is differentiated by differentiator $\delta 2$, generating a positive-going BOTDP pulse (Plot 5), which resets RW1 via U17-B. The $\overline{Q}$ output of flip-flop RW1 goes high, disabling the Rewind ramp generator so that the tape decelerates to rest. The Load flip-flop U15-A is also set via gates U17-B and U16-E. This enables the Forward ramp generator (Plot 6).

The timing characteristics of the ramp generators are such that the BOT tab overshoots the photosensor and then returns. When the BOT tab is detected for the second time, the 0.5-second single-shot is triggered (Plot 4) and AND gate U20-B is enabled and its output goes low, resetting the RW2 and Load flip-flops (Plots 2 and 6). The Forward ramp generator is thus disabled and the tape decelerates to rest. The delay between the LOAD waveform and AND gate U20-B ensures that the reset waveform is sufficiently long. At the end of the 0.5-second period, the NBOTD waveform goes high which causes NREADY to go low and, if SLT is high at this time, gate U6-C is enabled and the SRO waveform goes true.

The $\overline{Q}$ output of the RW2 flip-flop is low throughout the Rewind sequence and is used to generate the REWINDING (IRWD) interface waveform.

4-30. Case 2 — Tape at Load Point

A manual REWIND command initiates the Rewind sequence as just described. In this case, however, the tape unwinds from the takeup reel and tape tension is lost. Remote REWIND commands are inhibited by the NBOT waveform at AND gate U5-A; i.e., it is impossible to unload tape remotely — operator intervention is required.

4-31. Ready Mode from Tape Not at Load Point

The transport may be placed in the Ready mode after a Power-off, Power-on sequence even though tape has previously been brought beyond the Load Point; e.g., in the middle of a reel. Depress the LOAD control once to establish tape tension, then depress the ON-LINE control. The READY line will go true and the transport can accept remote commands.

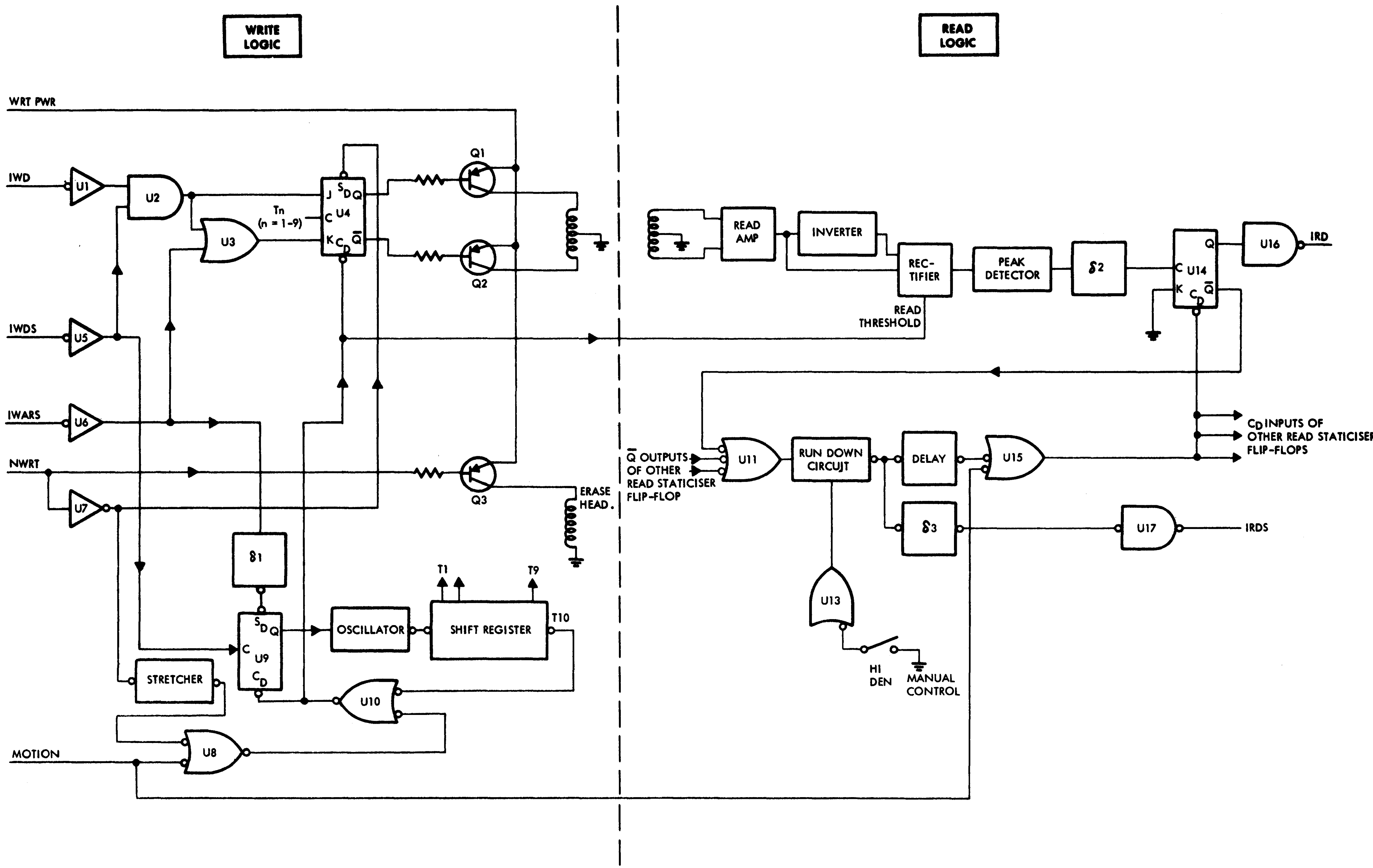


Figure 4-21 . Block Diagram, One Channel of Data Electronics

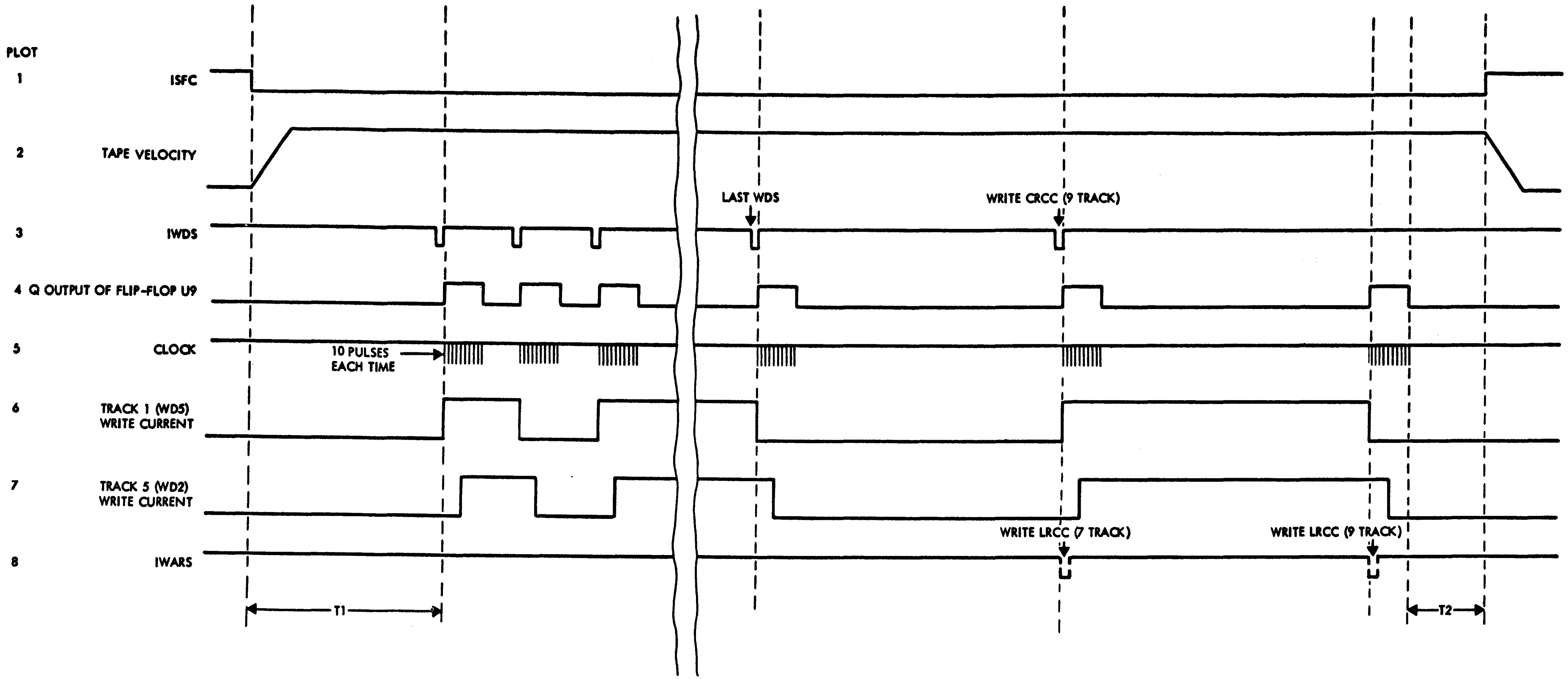
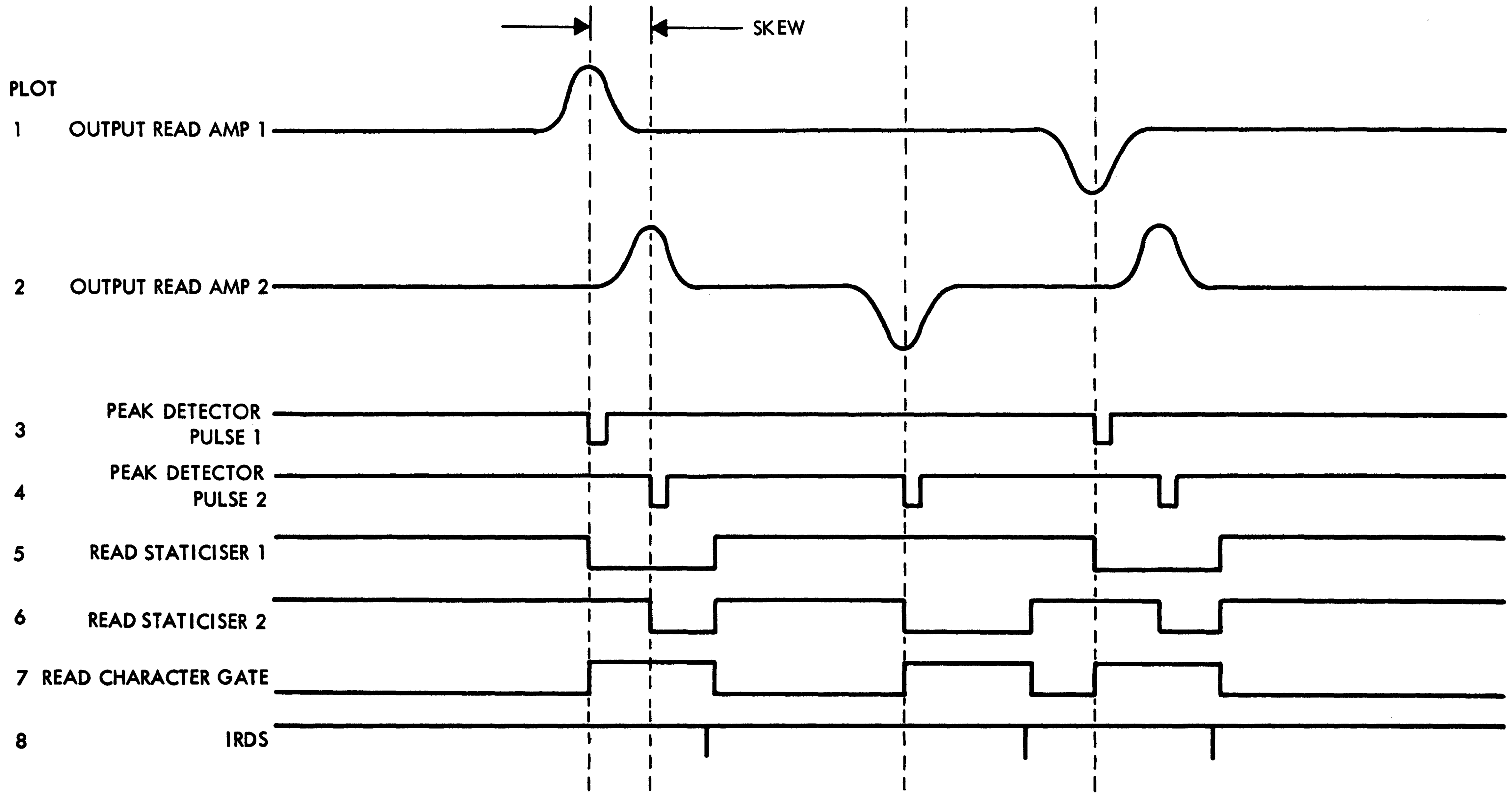


Figure 4-22 . Timing Diagram, Data Recording

NOTES:

1. DIAGRAM IS FOR 9-TRACK OPERATION. FOR 7-TRACK OPERATION, THE WDS PULSE (LABELLED WRITE CRCC) AND THE WARS PULSE (LABELLED WRITE LRCC (9-TRACK)) ARE OMITTED AND THE DOTTED WARS PULSE (LABELLED WRITE LRCC (7-TRACK)) IS USED.



NOTES:

1. SKEW AS SHOWN IS THE TIME DISPLACEMENT BETWEEN THE READ SIGNALS FROM THE TWO TRACKS.

2. THE TOTAL TIME DISPLACEMENT WHILE READING IS THE SUM OF THE SKEW COMPONENT WHICH WAS PRODUCED WHEN THE TAPE WAS WRITTEN (ON THIS OR ANY OTHER TRANSPORT) AND THE SKEW COMPONENT PRODUCED DURING THIS READING PROCESS.

Figure 4-23. **Timing Diagram, Data Reproduction**

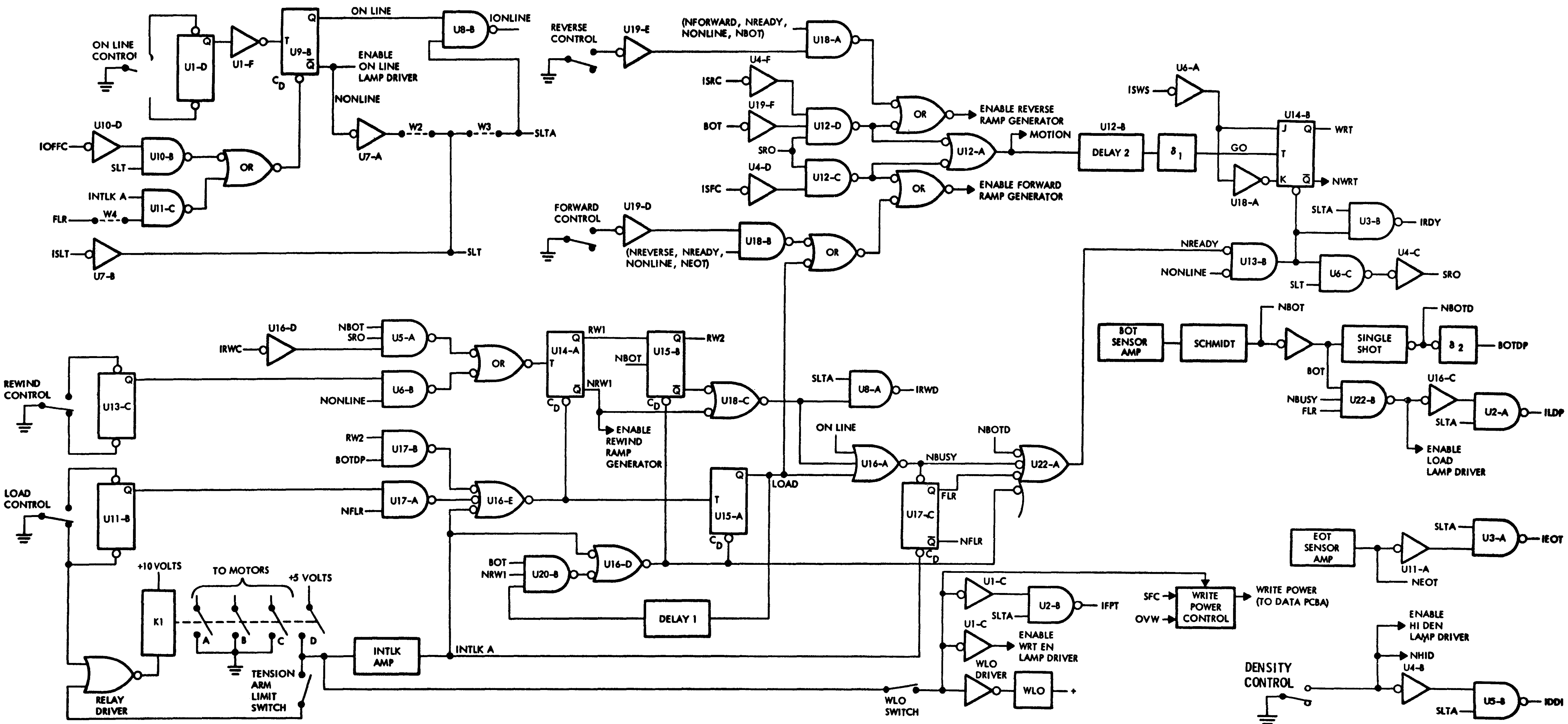


Figure 4-24. Block Diagram, Tape Control Logic

SECTION V

PRINTED CIRCUIT BOARDS THEORY OF OPERATION

5-1. INTRODUCTION

This section contains the theory of operation of the two Printed circuit boards used in the Tape Unit. The schematic and assembly drawing for each board is contained at the end of Section VII.

A better understanding of the logic utilized in the tape transport can be gained when the operation of the J-K flip-flop is fully understood. The following paragraphs provide a brief summary of the operation of the 852 J-K flip-flop, which is the type most commonly used in the system.

This flip-flop operates on a "Master-Slave" principle. A logic diagram of the flip-flop is shown in Figure 5-1. The flip-flop is designed so that the threshold voltage of AND gates 101 and 102 is higher than that of AND gates 103 and 104. Since operation depends exclusively on voltage levels, any waveform of the proper voltage levels can trigger the J-K flip-flop.

Assume that the trigger voltage is initially low. When the trigger voltage goes high, AND gates 103 and 104 are disabled. Subsequently, AND gates 101 and 102 are enabled by the trigger pulse, the J and K inputs, and the information previously stored at the output of the "slave" unit. The J and K input information at this time is transferred to the input of the "master" unit. When the trigger voltage goes

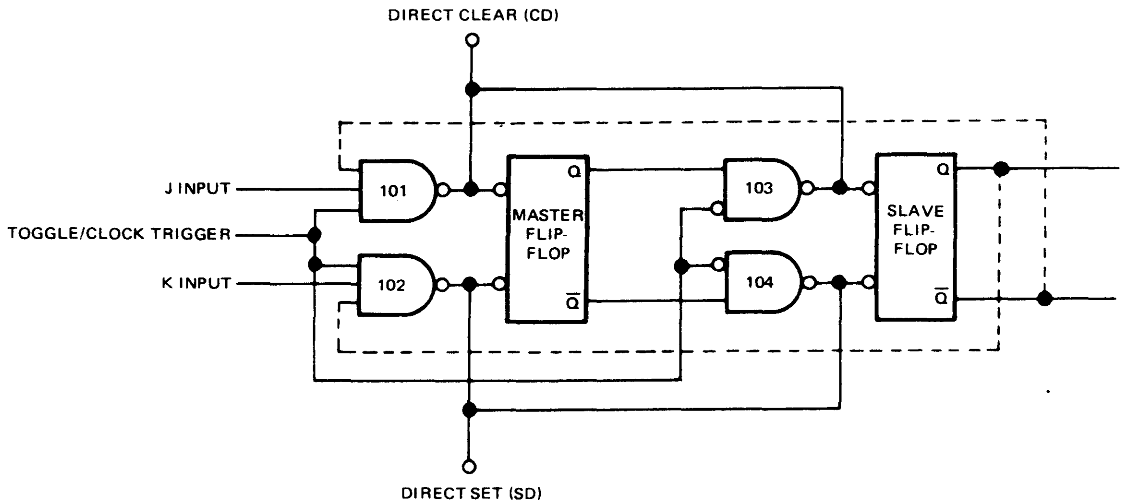


Figure 5-1. Simplified Logic Diagram, "Master-Slave" Flip-Flop

low, AND gates 101 and 102 are disabled. AND gates 103 and 104 are then enabled and the information stored in the "master" unit is transferred to the output of the "slave" unit.

5-2. THEORY OF OPERATION

5-3. DATA A1

The following is a description of the Data A1 printed circuit board assembly.

The Data A1 is approximately 16 inches long with edge connectors at each end (J102 and J103); these are the interface connectors and are slotted to mate with keys in the mating plugs. There are an additional two connectors on the Data A1. J1 is used to connect power and control signals from the Tape Control A1 circuit board. J2 is the connector into which the read/write head cable plugs.

5-4. Circuit Description

The board operation is described with reference to circuit 100, which is identical to circuits 200 through 900. All interface signals relevant to writing data (seven or nine WRITE DATA signals (IWD0, etc.), WRITE DATA STROBE (IWDS), and WRITE AMPLIFIER RESET (IWARS) enter via J102 and are terminated by a resistor combination and an integrated circuit inverter.

Referring to circuit 100, the Write Data Parity (IWDP) data line is terminated by resistors R101, R102, and inverter U3-C. The inverter output is connected to the J and K inputs of the write flip-flops so that a "true" interface signal results in the toggling of the flip-flop when a WDS pulse is received by U2-A and bussed to all the clock inputs.

The outputs of the write flip-flops drive the write amplifier transistors Q101 and Q102, whose emitters are taken to +5 volts when the WRT POWER level (J1-4) is high. This allows current to flow in the transistor whose flip-flop output is low. When the WRT POWER level is low (close to 0 volt), writing is inhibited because the write amplifier transistors cannot be turned on. In the same way, the erase current supplied by Q1 is inhibited when WRT POWER is low. Unless the transport is fitted with a Write Lockout Assembly WRT POWER is permanently at +5 volts.

The write flip-flops are primed for writing by the NWRT line (J1-9). This signal is inverted by power gate U1-B and bussed to all set inputs of the write flip-flops. This signal is also connected through an R-C delay to a pair of inverting stages (U1-A and U2-B) and bussed to all reset inputs of the write flip-flops. Thus, when the NWRT level is high, the ability to write is removed because both "true" and "false" outputs of the write flip-flops are raised to +5 volts. When the NWRT level is lowered to allow writing, the R-C network delays the removal of the reset input with respect to the set input, leaving the flip-flops in the reset state.

The head windings are so phased that the reset flip-flops cause current to flow in the standard "erase" direction. Lowering of the NWRT level also turns on the erase current driver (Q1). The MOTION level received at J1-6 prevents write current from flowing unless the tape is in motion.

The IWARS signal is used to write the LRCC at the end of a record. The leading edge of the IWARS pulse resets all the write flip-flops causing the head currents to be switched in those tracks where a "1" is required in the LRCC. The write current is defined by R105 and R106 and the damping resistor across the head is the sum of R107 and R108.

During reading, transistors Q101 and Q102 are held non-conducting and, for practical purposes, the effect of the write circuits is removed; therefore the head windings are loaded by the read amplifier input resistors R107 and R108. The signals at this point, during read, are so low that CR101 and CR102 do not conduct. The read amplifier is one-half of a dual operational amplifier IC (U10-B). The amplifier output is maintained close to 0 volt in the absence of an input signal by the feedback path of R109 and R112, which produces a relatively low dc gain. The low frequency cutoff is determined by capacitors C103 and C104. Diodes CR103 and CR104 shunting capacitors C103 and C104 are used to prevent large voltages from building up during a write operation that might prevent recovery of the amplifier during the available time prior to a subsequent read operation. The operating gain of the amplifier is defined by the resistor network R110, R111, and R113. R111 is a variable resistor used in the initial set-up to set the output peak-to-peak amplitude to 12 volts.

The read amplifier output is fed to a unity gain inverting amplifier, using transistors Q103, Q104, and Q105. The negative-going halves of the two phases of the read signal are added by means of diodes CR105 and CR106 and transistors Q106 and Q107. The exact voltage at which CR105 and CR106 conduct is controlled by the level at the Test Point 2, to which R119 is connected. This level is controlled by the IRTH interface line of J102. When IRTH is high (false), a voltage close to 0 volt is obtained at TP2, which results in a clip level of close to 20 percent of the read amplitude. When IRTH is low (true), a voltage close to -2 volts is obtained at TP2, which results in a clip level of close to 50 percent of the read amplitude.

The double emitter-follower stage Q106 and Q107 is used to drive the input of the peak detector.

The peak detector is essentially a differentiator circuit which uses one-half of a dual operational amplifier (U15-B). The amplifier is prevented from saturating by feedback diodes CR107, CR108, CR109, and CR110. The amplifier is biased to a negative output in the absence of an input signal by the resistor R122. At this point, a negative-going transition from approximately +1 volt to -1 volt corresponds to a peak of the read waveform. Resistor R125 and the corresponding resistors of the other eight circuits are connected to TP3. Examination of the output at TP3 with an oscilloscope while reading an "all 1's" tape allows an approximate estimate of the condition of the tape path. Skew is indicated by a progression of steps on the negative-going edge and the magnitude of skew by the ratio of the fall time to the total character time (see Paragraph 6-17).

The output of the peak detector operational amplifier is passed to Q108 which serves as the line transmitter. The collector and emitter of Q108 are routed to the interface edge connector (J103).

No attempt is made to generate a read data strobe on the Data A1.

The seven-channel version of the Data A1 is obtained by omitting circuits 200 and 300 from both the write and read sections of the circuit board.

5-5. TAPE CONTROL A1

The following is a description of the Tape Control A1 printed circuit board assembly.

The Tape Control A1 is approximately 16.5 inches long with an edge connector at one end (J101). This is the interface connector and is slotted to mate with a key in the mating plug. An additional connector (J10) is at the same end of the board and transmits power and control levels to the Data A1 circuit board. At the opposite end of the board is a row of connectors which are used to connect all deck-mounted sub-assemblies to the Tape Control A1. The power, motors, controls, tension-arm sensors, photo-tab sensors, and interlocks are all connected to the Tape Control A1 through these connectors (J1 through J9).

5-6. Circuit Description

A description of the logic sequences used in tape control is detailed in Section IV; comparison of Figure 4-15 and Schematic 101514 will show that the **RW1** and **RW2** flip-flops are U8, the **Load** flip-flop is U7, and the **FLR** flip-flop is U10. The switch "clean-up" flip-flops are U12.

Further description of the Tape Control A1 will be confined to a discussion of the circuits associated with each of the connectors.

J1 (zone C24), J2 (zone F24), and J3 (zone E24) are used to connect the REWIND, LOAD, and WRT EN controls or indicators. The WRT EN is used only when the File Protect option is taken. Both normally open and closed contacts are used and the switch "bounce" is removed by the "clean-up" flip-flops created from U12. The lamp drivers of circuits 100, 200, and 700 supply the 60-milliamp lamp current in response to a low input. Depressing the LOAD control turns on relay driver Q1.

J4 (zone B15) connects the tension arm interlock switch and the Write Lockout switch and solenoid, when required, to the associated circuits on Tape Control A1 PCBA. When the Write Lockout assembly is omitted, pins 6 and 1 are connected by a jumper wire to allow write current to pass to J10-4. Write current also passes through relay contacts 15 and 16.

When the interlock switch is closed, relay driver Q1 is held conducting, closing the normally open relay contacts. The relay voltage is derived from an auxiliary supply which decays very rapidly upon loss of line voltage. This ensures that the relay drops out, removing motor power and write current before the main power supplies have had time to decay to the point where inadvertent writing or motor motion could occur.

Diodes CR1, CR2, CR3, and CR4 eliminate relay arcing when the contacts are opened. The WLO solenoid driver (Q2) is turned on by the appearance of the WRT POWER level and causes the WLO solenoid to retract the Write Enable ring probe.

The BOT signal is connected from J5 to a "schmitt trigger" (circuit 600) to remove the possibility of multiple pulses at the leading and trailing edges of the BOT tab. The schmitt trigger uses one-half of a dual operational amplifier IC connected in the positive feedback mode and set to switch at approximately +1.5 volts. The output of the BOT and EOT amplifiers typically drop from +3.4 volts to +0.4 volt upon detection of the photo-tab. The output of the schmitt trigger is inverted and connected to a single-shot (circuit 800), which produces a 0.25-second pulse triggered by the leading edge of the tab. The single-shot pulse width is determined by C801, R803, and R804. The single-shot pulse-(NBOTD) is inverted and the trailing edge triggers a narrow pulse (BOTDP), whose width is determined by C4, R12, and R11.

J6 (zone D15) connects the unregulated +13 and -13 volts and the auxiliary 22 volts ac for the relay to the Tape Control A1. The unregulated +13 and -13 volts is used by servo amplifier circuits 1000, 1100, and 1200, and the +5 and -5 volt regulators (circuit 1300).

The regulators supply +5 and -5 volts to the digital ICs, photo-tab sensors, tension arm sensors, etc., and consist of two identical circuits whose output is set up by potentiometers R1302 and R1308. The +5 and -5 volt references are breakdown diodes CR1301 and CR1305. The output transistors (Q1304 and Q1308) of each regulator are located on the heatsink. A "crowbar" overvoltage protection circuit is provided and uses CR1303 to detect an increase in the +5-volt level to 8 volts, in which case the SCR (CR1304) is fired, which blows the 5-amp fuse on the external power supply module and removes the +13 volts.

J7 (zone G15) connects the three motor assemblies to the servo amplifiers and the relay contacts on the Tape Control A1. The capstan drive assembly has an additional pair of leads which are connected to a tachometer, integral with the motor. When the relay is de-energized, the contacts short the motor leads, which provides regenerative braking to prevent tape spillage. When the relay is energized, one side of each motor is connected to 0 volt and the other to its servo amplifier.

The capstan servo amplifier (circuit 1000) uses one-half of a dual operational amplifier as an input stage and discrete transistors to drive the high currents in the motor. Output transistors Q1002 and Q1006 are mounted on the heatsinks. The overall gain of the tachometer input is determined by R1012 divided by the sum of R1004 and R1005. Pin 9 of the IC is the virtual earth point into which the currents from the forward/reverse ramp generator, rewind ramp generator, circuit 900, the tachometer, and the amplifier output are summed. The tape speed is adjusted for both directions simultaneously by means of R1001.

J8 (zone F18) and J9 (zone G18) connect the take-up and supply tension arm sensors to the reel servo amplifiers on the Tape Control A1. The signals from the tension arm sensors are amplified by circuits 1100 and 1200, the supply reel servo amplifier, and the take-up reel servo amplifier. The low-frequency gain of the supply amplifier is defined by the ratio of R1111 plus R1113 to R1102; i. e., approximately 6. The high-frequency gain is increased by means of C1102, C1103, and R1112, to about 30. Output transistors Q1107, Q1109, Q1207, and Q1209 are located on the heatsink. Resistor R1101 is a supplementary input driven from the rewind ramp generator which removes the need for the tension arm to move through a large angle during rewind. Resistor R1201 performs the same task for the take-up servo.

J10 (zone C25) is the outlet for connections between the Tape Control A1 and Data A1 boards. The power supplies, +13 and -13 volts, +5 and -5 volts, and 0 volt, as well as the MOTION, NWRT, and WRT POWER signals associated with the writing of data, are picked-off from this connector.

J101 (zone G25) is the interface connector for tape motion and status commands. ISFC, ISRC, and IRWC commands are received and gated with the READY status. They then pass on to the ramp generator (circuit 900), where the digital signals are converted to analog levels with controlled transition times, which are the inputs to the capstan servo. The SFC and SRC are dealt with by a dual-operational amplifier circuit whose output levels are determined by the +5 and -5 volts, and the ratios of R903, R905 to R912, and whose rise and fall times are determined by the +5 and -5 volts, R913, R914, and C904. The transition times are varied by means of R913. The RWC is dealt with by the circuit which includes Q903 and Q904. The rewind speed is determined by the -5-volt line to which Q904 saturates when a rewind is in process, and resistor Q1003 on the capstan servo amplifier. The rise and fall time of the rewind speed is determined by R917, R918 and C908.

5-7. EOT/BOT AMPLIFIER — B PCBA

The following is a description of the EOT/BOT Amplifier — B circuit board assembly.

5-8. Circuit Description

J1 (zone C8) connects the photo-tab sensor, mounted on the tape deck, to the EOT/BOT Amplifier — B circuit board which is mounted on the write lockout bracket.

Transistors Q4 and Q5 form a differential pair which compares the BOT sensor output voltage at TP2 to a reference voltage supplied by the EOT sensor at the bases of transistors Q3 and Q4. When this voltage difference is positive with respect to the reference, no current will flow through Q5 and NBOT will be floating. When the voltage difference is negative by more than 0.6 volt, transistor Q5 conducts which causes transistor Q6 to conduct and clamps NBOT to 0 volt. Transistors Q1, Q2, and Q3 complete the symmetry for the EOT circuit. Potentiometers R3 and R9 are utilized to set TP1 and TP2 to +4.0 volts.

The output of the EOT/BOT amplifier board is connected to the Tape Control PCBA through J5.

5-9. INTRODUCTION

This section contains the theory of operation of the two printed circuit boards used in the dual gap NRZ Tape Transport. The schematic and assembly drawing for each board is contained at the end of Section VII.

5-10. THEORY OF OPERATION

5-11. DATA C

The following is a description of the Data C19 printed circuit board assembly (refer to Schematic 101538 and Assembly 101537).

5-12. Circuit Description

The board operation is described with reference to circuit 100, which is identical to circuits 200 through 900. All interface signals relevant to writing data (seven or nine WRITE DATA signals (IWD0, etc.), WRITE DATA STROBE (IWDS), and WRITE AMPLIFIER RESET (IWARS)) enter via J102 and are terminated by a resistor combination and an IC inverter.

Referring to circuit 100, the IWDP data line is terminated by resistors R101, R102, and inverter U2A. Inverters U2-A and U2-B perform a low-true AND function between IWDP and the WDS pulse received by U2-D, boosted by power gate U1-A, and bussed to all channels. Thus, a true signal on the IWDP line at WDS time results in a positive-going pulse being fed directly to the J input of the write waveform generator flip-flop U9-A and via inverter U2-C and OR gate U8-A to the K input of U9-A. Since the clock input level is high at this time, the "master" section of U9-A is toggled.

The WDS pulse also toggles clock control flip-flop U9-B which initiates the Write Deskewing operation. The Q output goes high, switching clamp transistor Q2 off for the clock oscillator Q3, Q4. This is an emitter-coupled multivibrator which generates negative pulses at the base of Q4 of a width (100-nanosecond) determined by resistor R19 and capacitor C6; the frequency is determined by resistors R17 and R18 and capacitor C6.

The pulses are fed to two 5-bit shift registers (U17 and U16), which generate 10 negative-going edges which occur sequentially on 10 output pins. Outputs T1 through T9 are fed to the relevant write waveform generator flip-flops and cause the "slave" section of the flip-flop to toggle on the negative-going edge.

The tenth output "C" resets the control flip-flop U9-B via U8-B and U8-C. The $\overline{Q}$ output of U9-B goes high, clamping the shift register. Also, the Q output goes low, clamping the oscillator.

The outputs of the write waveform generator flip-flops drive write amplifier transistors Q101 and Q102, whose emitters are taken to +5 volts when the WRT POWER line (J1-4) is high. The transistor connected to the low (approximately 0 volt) output of the flip-flop will conduct and a current will flow in the associated half of the head winding. When the WRT POWER line is low (approximately 0 volt), writing is inhibited because the write amplifier transistors cannot be turned on. Similarly, the erase current supplied by transistor Q1 is inhibited when the WRT POWER line is low. In operation, the write current is defined by resistors R105 and R106, while R107 is the associated damping resistor.

The write waveform generator flip-flops are primed for writing by the NWRT line (J1-9). This signal is inverted by power gate U7-B and bussed to the S_D inputs of the write waveform generator flip-flops. The signal is also connected via an R-C delay to OR gate U8-D and power gate U7-A. The output of U7-A is bussed to the C_D inputs of all the write waveform generator flip-flops. Thus, when the NWRT line is high, the ability to write is removed because both the Q and $\overline{Q}$ outputs of the write waveform generator flip-flops are at +5 volts. When the NWRT level is lowered to allow writing, the R-C network delays the removal of the C_D input with respect to the S_D input, leaving the flip-flops in the reset state.

The head windings are so phased that the reset flip-flops cause current to flow in the standard "erase" direction. Lowering of the NWRT level also turns on the erase current driver (Q1). The MOTION level received at J1-6 prevents write current from flowing unless the tape is in motion.

The IWARS pulse received by inverter U2-E is used to reset all the write waveform generator flip-flops as required to write the LRC character at the end of the record. The pulse is fed to the K inputs of all write waveform generator flip-flops via inverter OR gates U8-A, U11-D, etc., resetting the "master" section of all flip-flops.

The leading edge of the IWARS pulse is differentiated by capacitor C4 and resistors R12 and R13 and sets clock control flip-flop U9-B. This initiates a Write Deskewing sequence resulting in toggling of the write waveform generator flip-flops and the writing of the LRC character in a deskewed manner.

During reading, signals from the read head at a level of 5 to 10 millivolts are fed via connector J3 to the read amplifier, which is one-half of a dual operational amplifier IC (U18-B). The amplifier output is maintained close to 0 volt in the absence of an input signal by the feedback path of resistors R110 and R113, which determine relatively low dc gain. The low frequency cutoff is determined by capacitors C101 and C102. The operating gain of the amplifier is defined by resistor network R111, R114, and R112. R112 is a variable resistor used in the initial adjustment to set the output peak-to-peak amplitude.

The read amplifier output is fed to a unity gain inverting amplifier, consisting of transistors Q103, Q104, and Q105. The positive-going halves of the two phases of the read signal are added by means of diodes CR101, CR102, and transistors Q106 and Q107. The exact voltage at which CR101 and CR102 conduct is controlled by the level at TP12, to which R120 is connected. This level is controlled by the NWRT line. When NWRT is low, indicating a write operation, a voltage close to +2 volts is obtained at TP12 which results in a clip level of close to 50 percent of the read amplitude.

When NWRT is high indicating a read operation, a voltage close to 0 volt is obtained at TP12, which results in a clip level of close to 20 percent of the read amplitude.

The double emitter-follower stage Q106, Q107 is used to drive the input of the peak detector.

The peak detector is essentially a feedback differentiator circuit which uses one-half of a dual operational amplifier (U23-B). The amplifier is prevented from saturating by feedback diodes CR103, CR104, CR105, and CR106. The amplifier is biased to a negative output in the absence of an input signal by resistor R123. At this point, a positive-going transistion from -1 to +1 volt corresponds to a peak of the read waveform. The output of the peak detector operational amplifier is passed to Q108, which converts the signal to standard logic levels. At this point, a negative-going edge corresponds to the peak of the read waveform. Resistor R128 and the corresponding resistors of the other eight circuits are connected to TP15. Examination of the output at TP15 with an oscilloscope while reading an all "1s" tape allows a good estimate to be made of the condition of the tape path. Skew is indicated by a progression of steps on the negative-going edge and the magnitude of skew by the ratio of fall time to the character time.

The output of Q108 is differentiated by capacitor C108 and resistor R129 and fed to the clock input of Read Staticiser flip-flop U31-A, setting it.

The Q output of U31-A together with those of the other eight Read Staticiser flip-flops are OR'd by gate U28-B. The first flip-flop to be set causes a positive-going transition at TP10, which switches off clamp transistor Q8. This initiates run-down circuit Q7, Q8, Q9, and Q10. The voltage at the cathode of CR2 decays toward -5 volts from +4.5 volts with a time constant (R31 + R32) x (C10).

At approximately 0 volt, Q9 starts to cut off and this action is regenerative due to the positive feedback via capacitor C11 and resistor R36, resulting in a negative-going transition at the collector of Q10 (TP3). This transition is differentiated to form a 2-μsecond READ DATA STROBE pulse which is fed to the interface via power gate U30-B.

In addition, the negative transition is delayed via U29-F, resistor R41, capacitor C14, and inverter U29-A and fed via OR gate U30-A and power gate U32-B to the reset inputs of the Read Staticiser flip-flops. This causes the output of U28-B to go negative, turning on Q8; therefore, reapplying the clamp to the run-down circuit.

The delay is such that the data lines reset a minimum of 0.5 μsecond after the trailing edge of the READ DATA STROBE.

The Read Staticisers are reset whenever the MOTION signal (J1-6) is false; i.e., tape is not in motion.

The 7-channel version of the Data C circuit board (Data C17) has a different configuration. Circuits 200 and 300 are omitted from both the write and read sections of the board and the deskewing connections from the shift register to the write waveform generator flip-flops are different to accommodate the different track layout format (see Figures 4-7 and 4-8).

5-13. TAPE CONTROL B2

The following is a description of the Tape Control B2 printed circuit board assembly (refer to Schematic 101526 and Assembly 101527).

The Tape Control B2 is approximately 16.5 inches long with an edge connector at one end (J101). This is the interface connector and is slotted to mate with a key in the mating plug. An additional connector

(J14) is at the same end of the board and transmits power and control levels to the Data circuit board. The power, motors, controls, tension-arm sensors, photo-tab sensors, and interlocks are all connected to the Tape Control through a row of connectors at the opposite end of the board (J1 through J13).

5-14. Circuit Description

A description of the logic sequences used in the tape control is detailed in Paragraph 4-11.

J1, J4, and J6 are used to connect the REWIND, LOAD, and ON-LINE controls and indicators. Both normally open and closed contacts are used and the switch "bounce" is removed by the "clean-up" flip-flops. The lamp drivers of circuits 100, 200, and 300 supply the lamp current in response to a low input. Depressing the LOAD control turns on relay driver Q3.

J8 is used to connect the tension-arm interlock switch and the Write Lockout switch and solenoid, when required for writing, to the associated circuits on the Tape Control circuit board.

When the interlock switch is closed, relay driver Q3 is held conducting, closing the normally open relay contacts. The relay voltage is derived from an auxiliary supply which decays very rapidly upon loss of line voltage. This ensures that the relay drops out, removing motor power and write current before the main power supplies have had time to decay to the point where inadvertent writing or tape motion could occur.

Diodes CR3, CR4, CR5, and CR6 eliminate relay arcing when the contacts are opened. The WLO solenoid driver (Q2) is turned on by the appearance of the WRT POWER level and causes the WLO solenoid to retract the Write Enable ring probe.

The BOT signal is connected to a "Schmitt trigger" (circuit 800) to remove the possibility of multiple pulses at the leading and trailing edges of the BOT tab. The Schmitt trigger uses one-half of a dual operational amplifier IC connected in the positive feedback mode and is set to switch at approximately +1.5 volts. The output of the BOT and EOT amplifiers drop from approximately +3 volts to approximately 0 volt upon detection of the photo-tab. The output of the Schmitt trigger is inverted and connected to a single-shot (circuit 900), which produces a 0.5-second pulse triggered by the leading edge of the tab. The single-shot pulse width is determined by C901, R903, and R904. The single-shot pulse (NBOTD) is inverted and the trailing edge triggers a narrow pulse (BOTDP), whose width is determined by C6, R27, and R28.

J10 connects the unregulated +13 and -13 volts and the auxiliary 22 volts ac for the relay to the Tape Control board. The unregulated +13 and -13 volts is used by servo amplifiers (circuits 1300, 1400, and 1500) and the +5 and -5 volt regulators (circuit 1200).

The regulators supply +5 and -5 volts to the digital ICs, photo-tab sensors, tension arm sensors, etc., and consist of two essentially identical circuits whose outputs are set by potentiometers R1202 and R1208. The +5 and -5 volt references are zener diodes CR1201 and CR1205. The output transistors (Q1204 and Q1208) of each regulator are located on the heatsink. A "crowbar" overvoltage protection circuit is provided and uses zener diode CR1203 to detect an increase in the +5 volt level to +8 volts, in which case the SCR (CR1204) is fired, which blows the 5-amp fuse on the external power supply module and removes the +13 volts.

J9 connects the three motor assemblies to the servo amplifiers and the relay contacts on the Tape Control board. The capstan drive assembly has an additional pair of leads which are connected to a tachometer, integral with the motor. When the relay is de-energized, the contacts short the motor leads, which provides dynamic braking to prevent tape spillage. When the relay is energized, one side of each motor is connected to 0 volt and the other to its servo amplifier.

The capstan servo amplifier (circuit 1500) uses one-half of a dual operational amplifier as an input stage and discrete transistors to drive the high currents in the motor. Output transistors Q1504 and Q1506 are mounted on the heatsinks. The overall gain of the tachometer input is determined by R1511 divided by the sum of R1504 and R1505. Pin 5 of the IC is the virtual ground point into which the currents from the forward/reverse ramp generator and the rewind ramp generator (circuit 1100), the tachometer, and the amplifier output are summed. The tape speed is adjusted for both directions by means of R1501.

J11 and J12 connect the take-up and supply tension arm sensors to the reel servo amplifiers on the Tape Control board. The signals from the tension arm sensors are amplified by circuits 1300 and 1400, the supply reel servo amplifier, and the take-up reel servo amplifier. The low-frequency gain of the supply reel amplifier is defined by the ratio of (R1312 plus R1313) to R1303; i.e., approximately 6. The high-frequency gain is increased by means of C1302, C1303, and R1314, to about 30. Output transistors Q1306, Q1309, Q1406, and Q1409 are located on the heatsink. Resistor R1301 is a supplementary input driven from the rewind ramp generator which removes the need for the tension arm to move through a large angle during rewind. Resistor R1402 performs the same task for the take-up servo.

J14 is the output for connections between the Tape Control and Data boards. The power supplies, +13 and -13 volts, +5 and -5 volts, and 0 volt, as well as the MOTION, NWRT, WRT POWER, and NHID signals associated with the writing and reading of data, are picked-off from this connector.

J101 is the interface connector for tape motion and status signals, ISFC, ISRC, and IRWC commands are received and gated with the SELECT, READY, and ON LINE status. They then pass on to the ramp generator (circuit 1100), where the digital signals are converted to analog levels with controlled transition times, which are the inputs to the capstan servo. The SFC and SRC are dealt with by a dual-operational amplifier circuit whose output levels are determined by the +5 and -5 volts, and the ratios of R1103, R1105 to R111, and whose rise and fall times are determined by the +5 and -5 volts, R113, R114, and C1104. The transition times are varied by means of R113. The RWC is dealt with by the circuit which includes Q1103 and Q1104. The rewind speed is determined by the -5 volt line to which Q1104 saturates when a rewind is in process, and resistor R1502 on the capstan servo amplifier. The rise and fall time of the rewind speed is determined by R118, R119, and C1108.

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Table 6-2

Part Replacement Adjustments

Part Replaced	Auxiliary Adjustments	Time Required (Minutes)	Manual Paragraph Reference
Control Switch	None	2	—
Photo-Tab Sensor	EOT/BOT Potentiometers on EOT/BOT Amplifier PCBA	10	6-54
Tension Arm Sensor	Tension Arm Shutter	10	6-42
Limit Switch Assembly	None	10	6-41
Capstan Drive Assembly	Tape Speed, Ramp on Tape Control PCBA	20	6-56
Reel Motors Assembly	Belt Tension	10	6-57
Power Supply Assembly	None	20	—
Tape Control	+5v and -5v Regulators, Tape Speed and Ramps, EOT/BOT		6-8 through 6-27
Data PCBA	Read Amplifier Gain	15	6-28
EOT/BOT Amplifier Assembly	EOT/BOT	10	6-28
Head	Skew Adjustment, Read Amplifier Gain, Read Strobe Delay	30	6-47, 6-28, 6-34
Write Lockout Assembly	None	10	—
Take-up Hub	None	5	—

The following equipment (or equivalent) is required.

(1) Oscilloscope, Tektronix 453 (vertical and horizontal) sensivitity specified to ± percent accuracy).

(2) Voltmeter Model 630 NA (Triplett) or equivalent.

(3) Jacquet's Indicator - Model 252

(4)* Master Skew Tape

(5)* Standard Level Tape

*Tape may have to be transferred to a 600 foot reel to allow use on this Tape Unit.

6-7. ADJUSTMENT PHILOSOPHY

Acceptable limits are defined in each adjustment procedure, taking into consideration the assumed accuracy of the test equipment specified in Paragraph 6-6.

When the measured value of any parameter is within the specified acceptable limits NO ADJUSTMENTS should be made. Should the measured value fall outside the specified acceptable limits, adjustment should be made in accordance with the relevant procedure.

CAUTION

SOME ADJUSTMENTS MAY REQUIRE CORRESPONDING ADJUSTMENTS IN OTHER PARAMETERS. ENSURE CORRESPONDING ADJUSTMENTS ARE MADE AS SPECIFIED IN THE INDIVIDUAL PROCEDURES. THE +5 AND -5V REGULATOR VOLTAGES MUST BE CHECKED PRIOR TO ATTEMPTING ANY ELECTRICAL ADJUSTMENT.

When adjustments are made, the value set should be the exact value specified (to the best of the operator's ability)..

6-8. +5V AND -5V REGULATORS

The +5V and -5V regulators are located on the Tape Control circuit board. The regulators are adjusted by means of variable resistors R1302 (+5V) and R1308 (-5V). The numerical value of the voltage difference, disregarding polarity, between the +5V and -5V lines must be less than 0.07 volt. (Adjust R1202 and R1208 on B2 Boards).

6-9. Test Configuration

(1) Load a 7-inch reel of tape with a Write Lockout ring in place.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlocks and tension the tape.

(4) Depress and release the LOAD control a second time. Tape will advance to the load point and stop.

6-10. Test Procedure

✓ (1) Using a 630 NA voltmeter measure and note the voltage between TP9 (+5V) and TP7 (0V) on the Tape Control PCBA. Measure between TP17 and TP22 for +5V on B2 Boards.

✓ (2) Using the 630 NA voltmeter (or equivalent) measure and note the voltage between TP8 (-5V) and TP7 (0V) on the Tape Control PCBA. Measure between TP23 and TP22 for -5V on B2 Boards.

(3) Acceptable Limits

(a) +5V Regulator

- +4.85V minimum
- +5.15V maximum

(b) -5V Regulator

- -4.85V minimum
- -5.15V maximum

(4) Compare the voltages obtained in Steps (1) and (2). Voltages must fall within the acceptable limits and the difference between the +5V and -5V lines must be less than 0.07 volt.

6-11. Adjustment Procedure

When the acceptable limits are exceeded or the voltage difference between the absolute value of the +5V and -5V lines must be less than 0.07 volt.

✓ (1) Adjust variable resistor B1302 on the Tape Control PCBA 3A to +5 volts. Adjust R1202 on Control B2 Boards.

✓ (2) Adjust variable resistor R1308 on the Tape Control PCBA to -5 volts. Adjust B1208 on Control B2 Boards.

6-12. Related Adjustments

The following areas must be checked and adjusted subsequent to adjusting the +5 and -5 volt regulators.

(1) Ramp Timing (Paragraph 6-28).

(2) Tape Speed (Paragraph 6-33).

6-13. BOT/EOT AMPLIFIER

The EOT/BOT amplifier system is located on a small printed circuit board (approximately 2 inches by 4 inches) which is mounted on a bracket at the rear of the tape deck.

NOTE

Measurements and adjustments to the EOT/BOT amplifier should be performed at room temperature.

6-14. Test Configuration

(1) Load a 7-inch reel of tape with a Write Lockout ring in place.

(2) Apply power to the transport.

(3) Depress and release the LOAD control to establish interlocks and tension the tape.

(4) Depress and release the LOAD control a second time. Tape will advance to the load point and stop.

6-15. Test Procedure

(1) Advance the tape until the reflective BOT tab is past the photo-sensor.

✓ (2) Using a 630 NA voltmeter (or equivalent) measure and note the off-tab voltage between TP1 (EOT) on the EOT/BOT amplifier PCBA and 0V (TP7 on Control A, TP22 on Control B).

✓ (3) Using a 630 NA voltmeter (or equivalent) measure and note the off-tab voltage between TP2 (BOT) on the EOT/BOT amplifier PCBA and 0V. (TP7 on Control A, TP22 on Control B).

(4) Acceptable Limits (off-tab)

- +3.80V minimum
- +4.20V maximum

(5) Compare the voltages obtained in Steps (2) and (3). Voltages must fall between the acceptable limits and the difference between TP1 (EOT) and TP2 (BOT) voltages must be less than 0.10 volt.

(6) Manually position the tape until the reflective BOT tab is located under the photo-sensor.

✓ (7) Measure and note the on-tab voltage between TP1 (EOT) on the EOT/BOT amplifier amplifier PCBA and 0V. (TP7 on Control A, TP22 on Control B).

(8) Advance the tape until the EOT tab is positioned under the photo-sensor.

(9) Measure and note the on-tab voltage between TP1 (EOT) on the EOT/BOT amplifier PCBA and 0V (Gnd).

(10) Acceptable Limits (on-tab)

- +2.80V maximum

6-16. Adjustment Procedure

When the acceptable limits are exceeded or the off-tab voltage difference compared in Paragraph 6-15, Step (5), is greater than 0.10 volt, the following adjustments are performed.

✓ (1) Verify that the adjusting screws of variable resistors R402 and R502 located on the Control A; R602 and R702 on B2 Boards are turned fully clockwise.

(2) Position the tape so that the EOT/BOT reflective tabs are clear of the photo-sensor area.

(3) Adjust variable resistor R3 on the EOT/BOT amplifier PCBA to +4.0 volts as observed at TP1.

(4) Adjust variable resistor R9 on the EOT/BOT amplifier PCBA to +4.0 volts as observed at TP2.

(5) Verify that the voltage at TP1 on the EOT/BOT amplifier PCBA is within 0.10 volt of the voltage at TP2. Repeat Steps (3) and (4) if required.

(6) Position the tape so that the EOT reflective tab is located under the photo-sensor.

(7) Verify that the on-tab voltage at TP1 of the EOT/BOT amplifier PCBA falls within the limits specified in Paragraph 6-15, Step (10).

(8) Depress and release the REWIND control. Tape will rewind to the BOT, enter a load sequence, and stop.

(9) Manually position the BOT reflective tab under the photosensor.

(10) Verify that the on-tab voltage at TP2 of the EOT/BOT amplifier PCBA falls within the limits specified in Paragraph 6-15, Step (10).

6-17. Related Adjustments

The +5V and -5V regulators (Paragraph 6-8) must be checked and/or adjusted prior to adjusting the EOT/BOT amplifier system.

6-18. RAMP TIMING

The four tape acceleration and deceleration ramps (Forward and Reverse, Start and Stop) are controlled by a single potentiometer adjustment located on the Tape Control PCBA.

This adjustment controls the Start/Stop time and its value is dependent upon the tape speed. Start/Stop times should be calculated from the following formula which will result in a constant Start and Stop distance of 0.19 inch when the tape speed is correct.

$$\text{Start/Stop Time (milliseconds)} = \frac{375}{\text{Speed (ips)}}$$

Example: 30 millisecond Start/Stop time @ 12.5 ips

The ramp adjustment time is chosen to ensure that the correct Start/Stop distance is correlated to the specified Start/Stop time.

6-19. Test Configuration

(1) Load a 7-inch reel of tape with a Write Lockout ring in place.

(2) Apply power to the Tape Unit.

(3) Depress and release the LOAD control to establish interlocks and tension the tape.

(4) Depress and release the LOAD control a second time. Tape will advance to the load point and stop.

✓ 6-20. Test Procedure

(1) Connect a signal probe of a Tektronix Model 453 or equivalent oscilloscope to TP 6 on Control A, TP18 on Control B2.

✓ (2) Connect the oscilloscope reference probe to TP7 (0V) on Tape Control PCBA; TP22 on Control B2.

(3) Apply a 5Hz symmetrical square wave with a 3V amplitude (+3.0V to 0V) to the interface line ISFC (J101 pin C

(4) Synchronize the oscilloscope on the negative going edge of the square wave input.

(5) Adjust the oscilloscope Variable Vertical (volts/div) control to display 0 to 100 percent of the ramp waveform over four large divisions of the oscilloscope graticule.

(6) Observe that the ramp adjustment time intersects 90 percent of the ramp amplitude (18 small divisions of oscilloscope graticule). Figure 6-1 illustrates ramp levels and timing.

NOTE

For reverse operation the ramp is a negative going waveform.

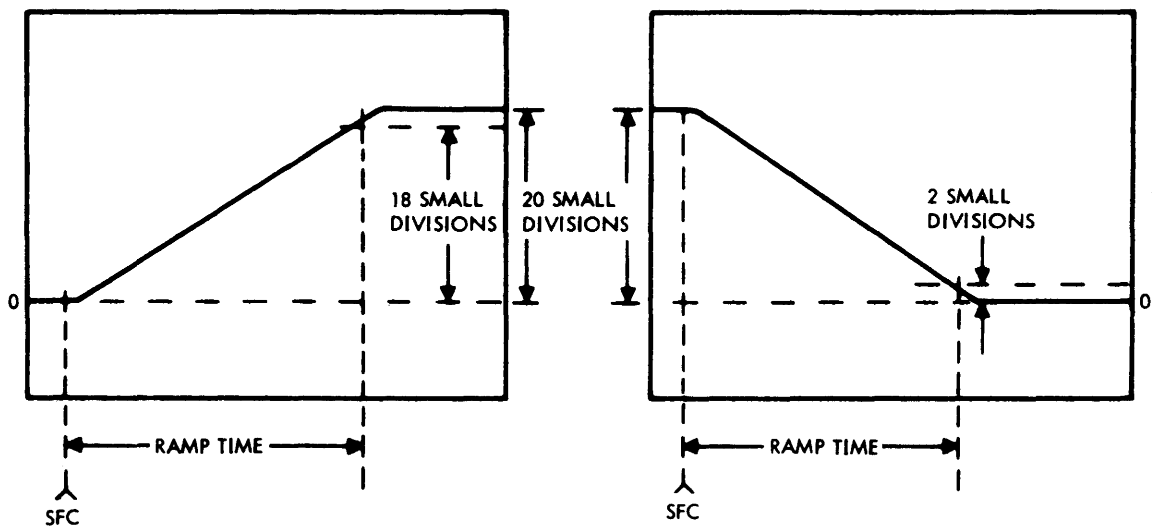


Figure 6-1. Ramp Levels and Timing

(7) Acceptable Limits (90 percent of Actual Speed)

- 22.5 – 25.4 milliseconds

(8) Remove the square wave input from J101 pin C (ISFC) and apply the square wave input to ISRC line (J101 pin E)

(9) With the oscilloscope connected as specified in Step (5), observe that the reverse ramp timing is within the limits specified in Step (7).

6-21. Adjustment Procedure

When the acceptable limits are exceeded the following adjustments are performed.

(1) Establish test configuration described in Paragraph 6-19.

(2) Perform Test Procedure described in Paragraph 6-20, Steps (1) through (5).

(3) Adjust variable resistor R913 on Tape Control PCBA to obtain ramp adjustment time of 24.0 milliseconds. Adjust R1113 on B2 Boards.

NOTE

Specified times result in oscilloscope display illustrated in Figure 6-1. The ramp adjustment time intersects 90 percent of ramp amplitude when accelerating and 10 percent of ramp amplitude when decelerating.

(4) Remove the square wave input from ISFC line (J101 pin C) and apply the square wave input to the interface line ISRC (J101 pin E).

(5) Observe oscilloscope display of reverse ramp and readjust R913 to obtain ramp times as specified in Step (3).

6-22. Related Adjustments

The +5V and -5V regulators (Paragraph 6-8) must be checked and/or adjusted prior to adjusting the Ramp Timing.

6-23. TAPE SPEED

Only the Synchronous Forward speed is adjustable. The Synchronous Reverse function utilizes the same voltage reference as Synchronous Forward and is not independently adjustable.

Tape speeds are checked and adjusted utilizing a 500-line optical encoder and a frequency counter.

Alternatively, a revolution counter can be employed; 12.5 ips is the equivalent of 398 rpm.

Field adjustment and test can be made using the Jacquet's indicator. The speed should be measured at the Capstan while driving tape forward continuously.

The nominal counter frequency reading to which tape speed is adjusted is 3325. Tape speed may be calculated from the following formula used in conjunction with the specified counter timer.

$$V \text{ ips} = \text{Counter Frequency (Hz)} \times \frac{C}{500} \text{ inches}$$

where

C = Capstan Circumference

NOTE

Capstan circumference for the 7000 Series transports is 1.884 inches.

6-24. Test Configuration

(1) Couple an Optical Encoder to the rear of the capstan shaft utilizing a coupling device. Five volts dc must be applied to the Optical Encoder lamp input (pins 1 and 2). This voltage can be obtained between TP9 (+5V) and TP7 (0V) on the Tape Control PCBA.

Tape Control PCBA.

(2) Load a 7-inch reel of tape with a Write Lockout ring in place.

(3) Apply power to the Tape Unit.

(4) Depress and release the LOAD control to establish interlocks and tension the tape.

(5) Depress and release the LOAD control a second time. Tape will advance to the load point and stop.

6-25. Test Procedure

(1) Connect input probes of Counter Timer, Monsanto Model 100B (or equivalent) to pins 6 and 7 of the Optical Encoder.

(2) Connect the interface line ISFC (J101 pin C or TP3) to ground. Tape will move in the forward direction.

(3) Adjust the sample interval of the counter timer to monitor the encoder output over a one-second interval.

(4) Acceptable Limits

- Maximum - 3358
- Minimum - 3292

(5) Remove the ground from J101 pin C (ISFC) and apply a ground to the interface line ISRC (J101 pin E or TP1). Tape will move in the reverse direction.

(6) With the Counter Timer connected as specified in Step (1) monitor the output of the optical encoder.

(7) The reverse tape speed as monitored with the counter timer must be within the following limits:

- Maximum - 3424
- Minimum - 3226

6-26. Adjustment Procedure

When the forward or reverse tape speeds exceed the specified limits the following adjustments are performed.

(1) Establish the test configuration described in Paragraph 6-24.

(2) Perform the Test Procedure described in Steps (1) through (3), Paragraph 6-25.

√ (3) Adjust the variable resistor R1001 on the Tape Control PCBA for the following counter timer value.Adjust R1501 on B2 Boards for proper timer value.

(4) Remove the ground from J101 pin C (ISFC) and apply a ground to the interface line ISRC (J101 pin E).

(5) Monitor the counter timer to ensure that the reverse speed is within the acceptable limits established in Paragraph 6-25, Step (7). Repeat Steps (2) through (5) as required.

6-27. Related Adjustments

The +5V and -5V regulators must be checked and/or adjusted prior to adjusting the tape speed.

6-28. READ AMPLIFIER GAIN

The gain of each of the read amplifiers, located on the Data PCBA is independently adjustable.

Read Amplifier gain may be determined by reading (in the Read Only mode) an all-ones tape which was recorded on the transport. Paragraph 6-32 details a method for generating an all-ones tape. A quality tape, such as Burroughs Standard amplitude tape.

6-29. Test Configuration

(1) Clean the head assembly and tape path as described in Paragraph 6-4.

(2) Load a prerecorded tape (see Paragraph 6-32).

*This tape is supplied on 1200 foot reels and may require transfer of 600 feet of tape to a smaller reel to fit on the Tape Unit.

(3) Apply power to the transport.

(4) Depress and release the LOAD control to establish interlocks and tension the tape.

(5) Depress and release the LOAD control a second time. Tape will advance to the Load Point and stop.

6-30. Test Procedure

(1) Connect the interface line ISFC (J101 pin C) to ground. Tape will move forward at the specified velocity.

(2) Using the signal probe of a Tektronix 453 oscilloscope (or equivalent), measure and record the peak-to-peak amplitude of the read amplifier waveforms viewed at TP103 through TP903 on the Data PCBA.

NOTE

Oscilloscope vertical sensitivity should be set to display 2 volts per division.

(3) Acceptable Limits (peak-to-peak limits when utilizing an all-ones tape generated on the transport).

- 13.5 volts maximum
- 9.5 volts minimum

6-31. **Adjustment Procedure**

When the acceptable limits are exceeded the following adjustments are performed.

(1) Establish the test configuration described in Paragraph 6-28.

(2) Connect the interface line ISFC (J101 pin C), to ground.

✓ (3) Using the signal probe of a Tektronix oscilloscope (or equivalent) observe TP103 through TP903 on the Data PCBA. Adjust variable resistors R111 through R911 associated with test points to 12V peak-to-peak. On C17 or C19 Boards, adjust R112 through R912 for the 12V P/P signal.

6-32. **All-Ones Tape**

An all-ones tape may be generated as follows.

(1) Ensure that head assembly and tape path are clean.

(2) Load a work tape, which is known to be in good condition, on the Tape Unit.

(3) Bring Tape Unit to Load Point as described in Paragraph 6-14.

(4) Apply a ground to the interface line ISWS (J101 pin K).

(5) Apply a ground to the interface line ISFC (J101 pin C).

(6) Apply a ground to interface lines IWDP-IWD7 (J102 pins L, M, N, P, R, S, T, U, and V).

(7) Apply negative-going pulses (+3V to 0V) of 2 μseconds duration at the specified transfer rate to the interface line IWDS (J101 pin A).

(8) Maintain the Tape Unit in this record mode for approximately 5 minutes.

(9) Remove the signal source from the interface line IWDS (J101 pin A).

(10) Remove the ground from the interface lines ISWS and ISFC (J101 pin K and J101 pin C respectively).

(11) Depress and release the REWIND control. The tape will rewind to the Load Point and stop.

In considering the overall gain of the read system it is important to note that the output of the read head is particularly dependent upon the type of magnetic tape used and the condition of the tape; i. e., new or used.

The read amplifier output should be adjusted as detailed in Paragraph 6-31 (3). A read amplifier whose gain is adjusted too high will result in amplifier saturation; gain which is set too low will increase the susceptibility to data errors due to drop-outs.

6-33. Related Adjustments

The tape speed (Paragraph 6-23) must be checked and/or adjusted prior to adjusting the Read Amplifier gain.

6-34. MECHANICAL ADJUSTMENTS

6-35. TENSION ARM LIMIT SWITCH

When the tension arm is resting against its backstop, the position of the limit switch roller with respect to the cam should be as shown in Figure 6-2. At this time the switch contacts should be open. If the relative positions of the roller and cam are not as illustrated, the following adjustment is performed.

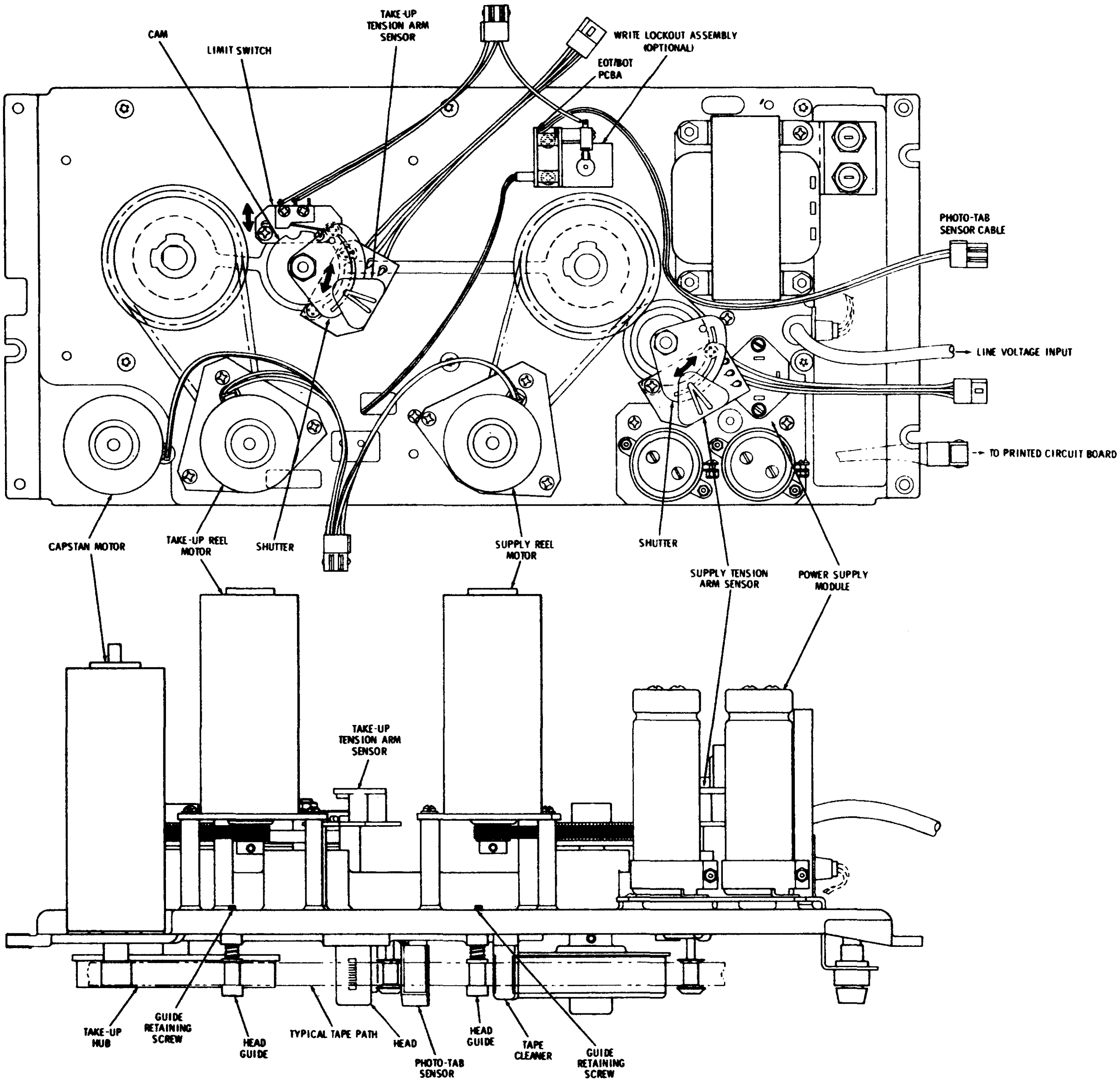


Figure 6-2. Tape Deck Diagram (Rear View)

(1) Loosen the cam retaining set-screw.

(2) Rotate the cam on its shaft until the limit switch roller is in the position illustrated in Figure 6-2.

(3) Firmly tighten the cam retaining set-screw.

CAUTION

THE CAM RETAINING SET-SCREW MUST BE TIGHTENED SUFFICIENTLY TO PREVENT ROTATION OF THE CAM WHEN THE TENSION ARM IMPACTS ON ITS BACKSTOP.

The limit switch plate is slotted at one mounting screw and may be rotated about the second screw to facilitate setting the switching point of the limit switch. The plate should be rotated to a position where the limit switch trips with its roller one-half of the distance up the slope from its rest position. The switch should be closed when the roller moves on the cam lobe between the semi-circular cutouts.

Replacement of the limit switch is accomplished as follows.

(1) Unplug the limit switch connector (P4) from J4 of the Tape Control circuit board.

(2) Remove yellow and green leads from the limit switch connector (P4) using an extractor tool.

(3) Remove the two mounting screws which mount the limit switch to its plate and remove the switch.

(4) Attach the new limit switch to the plate using the two mounting screws removed in Step (3).

(5) Adjust the limit switch position as described in the preceeding paragraph.

(6) Tighten the two mounting screws and recheck position of the limit switch roller.

(7) Connect the limit switch connector (P4) to J-4 of the Tape Control circuit board.

6-36. TENSION ARM POSITION SENSOR

There are two tension-arm position sensors: one on the take-up tension arm, the second on the supply arm. Each of the sensors has a three-pin plug which connects the output of the sensor to the reel servo amplifier on the Tape Control circuit board.

CAUTION

ENSURE THAT THE +5V AND -5V REGULATED VOLTAGES, RAMP TIMING, AND TAPE SPEED ARE CORRECT AS DETAILED IN PARAGRAPHS 6-8, 6-28, AND 6-23, RESPECTIVELY, BEFORE ADJUSTING THE TENSION ARM POSITION SENSORS.

6-37. Preliminary Adjustment

The tension arm photo-sensors on the supply reel and take-up reel are initially adjusted as follows.

(1) Remove tape from the transport.

(2) Establish an environment which ensures that the tension arm sensors are shielded from high ambient light. Failure to do so will result in a shift in the arm operating region when the unit is rack-mounted.

(3) Loosen the No. 10 retaining nut securing the optical shutter to the tension arm shaft.

NOTE

Loosen the nut in such a manner that the shutter can be rotated by hand, yet there is sufficient friction to prevent the setting from changing when the nut is tightened.

(4) Apply power to the transport.

(5) Rotate the shutter until moving the tension arm to the middle of its range stops reel motion.

NOTE

The LOAD control must be continuously depressed or the limit switch shorted to facilitate this procedure.

(6) Load a 7-inch reel of tape on the transport.

(7) Depress and release LOAD control to establish interlocks and tension the tape.

(8) Depress and release LOAD control a second time. Tape will advance to Load Point and stop.

6-38. Supply Arm Adjustment - Optical Shutter

When the preliminary adjustments described in Paragraph 6-47 are completed, proceed as follows.

(1) Apply ground to the interface line ISFC (J101 pin C or TP3). Tape will move forward at the specified velocity.

(2) When the supply reel is nearly empty remove the ground from the interface line ISFC.

(3) Alternately ground the interface line ISRC (J101 pin E or TP1) and the interface line ISFC (J101 pin C or TP3) so that the tape shuttles back and forth.

(4) Note the total arm movement.

(5) Readjust the shutter so that the arm displacement forward and reverse is approximately equi-distant about the center of the arm cutout in the overlay.

(6) Torque the optical shutter retaining nut to 35 inch-pounds taking care that the shutter does not move.

6-39. Take-up Arm Adjustment - Optical Shutter

When the supply arm adjustments are completed, proceed as follows.

(1) Ensure that the limit switch cam (Paragraph 6-35) is centered (limit switch actuating roller rests in approximately the same position in the cut-out with the tension arm at each stop).

(2) Apply ground to interface line ISRC (J101 pin E or TP1). Tape will move in the reverse direction at the specified velocity.

(3) When the take-up reel is nearly empty, remove the ground from the interface line ISRC (J101 pin E or TP1).

(4) Alternately ground the interface line ISFC (J101 pin C or TP3) and the interface line ISRC (J101 pin E or TP1) so that the tape shuttles back and forth.

(5) Rotate the optical shutter until the limit switch roller remains on the top surface of the cam during forward and reverse motion of the tape.

(6) Depress and release the REWIND control and observe that the limit switch roller remains on the top surface of the cam. If necessary, rotate the take-up reel shutter so that the roller remains on the top surface of the cam.

(7) During the rewind operation, observe that the supply arm is not displaced more than one inch from the neutral position.

(8) Repeat Steps (1) through (7) as required.

(9) Torque the optical shutter retaining nut to 35 inch-pounds, taking care that the shutter does not move.

6-40. Tension Arm Sensor Replacement

The tension arm optical sensors are replaced as follows.

(1) Loosen the No. 10 retaining nut which secures the optical shutter to the tension arm.

(2) Rotate the shutter to clear the countersunk screws which retain the tension arm sensor printed circuit board to the deck standoffs.

(3) Remove two retaining screws from the tension arm sensor printed circuit board.

NOTE

Retain the two screws removed in Step (3). They will be used to mount the replacement sensor.

(4) Unplug the connector (P8 for take-up reel sensor, and P9 for supply reel sensor) from the Tape Control circuit board and remove sensor assembly.

(5) Mount the replacement assembly on the deck standoffs using the two screws which were removed in Step (3).

(6) Plug the connector (P8 for take-up reel sensor, P9 for supply reel sensor) into the respective jack on the Tape Control circuit board.

(7) Perform the relevant adjustment procedure detailed in Paragraph 6-36.

6-41. SKEW MEASUREMENT AND ADJUSTMENT

Read system skew will be considered in two components: static and dynamic. Static skew is caused by head azimuth misalignment and can be observed (on an oscilloscope) as the average of the read waveform slope. Dynamic skew is caused by defects in the magnetic tape or misalignment of the tape path. Dynamic skew can be observed as temporary excursions in excess of the average skew.

6-42. Skew Measurement

✓ An indication of the total system skew may be obtained during a read operation by observing the algebraic sum of the peak detectors at TP3 on the Data PCBA while reading a Master Skew Tape, Refer to Sec. VI, Pg. 6. Figure 6-3 illustrates an example of correctly adjusted skew as observed at TP3. Figure 6-4 is an example of excessive skew. Observe TP15 on Data C17 or Data C19 Boards.

A more precise method of determining the system read skew is:

(1) Clean the head assembly and tape path as described in Paragraph 6-4.

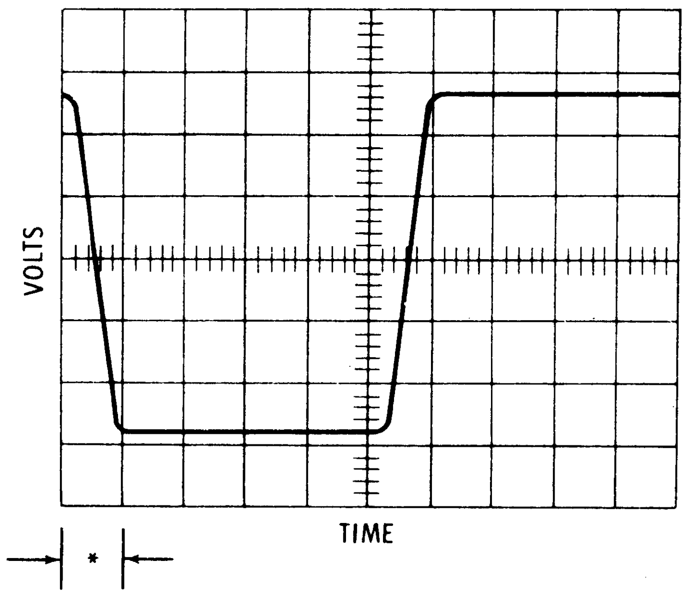
(2) Load a Master Skew Tape.

(3) Apply power to the transport.

(4) Depress and release the LOAD control to establish interlocks and tension the tape.

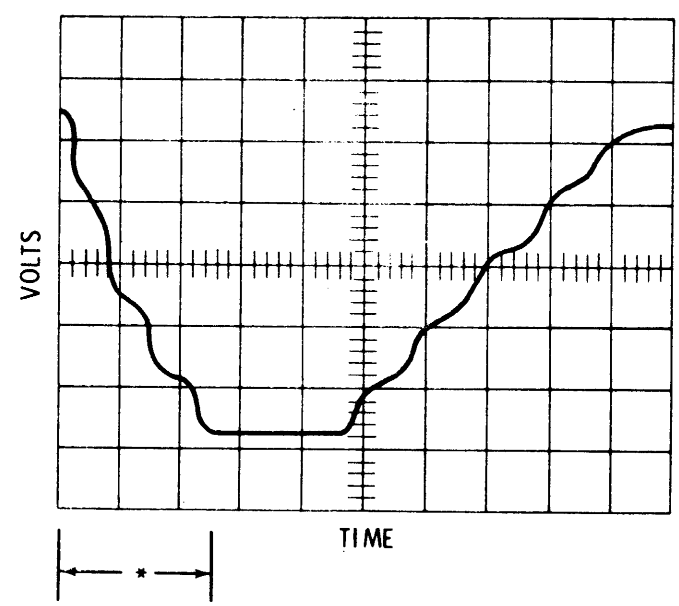
(5) Depress and release the LOAD control a second time. Tape will advance to the Load Point and stop.

(6) Set the vertical sensitivity of a Tektronix Model 561 oscilloscope (or equivalent) to 1.0 volt/cm and the horizontal range to 5 μsec/cm.



* FALL TIME MUST BE LESS THAN ONE DIVISION

Figure 6-3. Skew Waveform (Good)



* FALL TIME EXCEEDS ONE DIVISION

Figure 6-4. Skew Waveform (Poor)

(7) Set the oscilloscope to trigger on oscilloscope Channel 1 negative slope, alternate mode.

NOTE

Ensure that both oscilloscope signal probes are calibrated.

(8) Apply ground to ISFC interface line (J101 pin C); tape will advance at the specified velocity.

(9) Connect the oscilloscope Channnel 1 signal probe to TP405 (9-track) or TP105 (7-track) on the Data PCBA and observe the read waveform.

(10) Observe oscilloscope Channel 1 waveform and adjust the horizontal time/division "variable" control to display one complete cycle (10 cm).

NOTE

With an 800 cpi tape, each cycle represents 1250 μinches. The scope graticule is divided into 10 major divisions, each of which is divided into 5 divisions; therefore

$$\frac{1250\ \mu\text{inch}}{50\ \text{divisions}} = 25\ \mu\text{inch/division}$$

(11) Position the positive (+) going edge of the oscilloscope Channel 1 trace on the vertical center line of the scope graticule.

(12) Using the oscilloscope Channel 2 probe, observe the remaining test points (TP105 - TP905). The maximum allowable horizontal difference between the positive-going edge of the waveform displayed on the oscilloscope Channel 1 and the positive-going edge of the waveform displayed on the oscilloscope Channel 2 is six small divisions; i.e., 150μinches.

(13) Note which observation in Step (12) indicated the greatest amount of skew with respect to TP405 (or TP105).

(14) Move the oscilloscope Channel 1 signal probe to the test point determined in Step (13).

NOTE

It may be necessary to reposition the positive-going edge of the oscilloscope Channel 1 trace as described in Step (11).

(15) Using the oscilloscope Channel 2 signal probe, repeat Step (12).

(16) Determine which observation indicates the greatest amount of skew.

(17) Remove ground from ISFC interface line (J101 pin C).

(18) Apply ground to ISRC interface line (J101 pin E).

(19) Repeat Steps (9) through (16) to determine reverse skew.

(20) Acceptable Limits:

Static - 100 μinches
Dynamic - 50 μinches
Total - 150 μinches

6-43. Static Skew Adjustment

To reduce the read system static skew to within acceptable limits the following procedure is followed.

(1) Perform skew measurement procedure described in Paragraph 6-42.

(2) While reading a Master Skew Tape (Paragraph 6-42) in the forward direction, observe the test point exhibiting the greatest amount of skew.

(3) Ease the edge of the tape off of the head guide toward the spring-loaded washer. This should be done on first one guide, then the other.

NOTE

Moving the tape one- to two-thousandths of an inch from one of the guides will reduce the skew to within acceptable limits.

(4) Observe the waveform to determine which movement (left guide or right guide) improves the display. If moving the tape off of the left-hand guide improved the display, the right hand guide should be shimmed.

NOTE

The shims are burr-free, etched, one-half of a thousandths inch thick berrylium copper.

(5) Remove the ground from ISFC interface line (J101 pin C).

(6) Remove power from the transport.

(7) Remove the head guide retaining screw (accessible from the rear of the deck) and remove the guide; also remove any previously installed shims.

NOTE

When removing the guide, care should be taken not to drop the spring and washer.

(8) Calculate the required number of shims needed to correct the skew. Since the character spacing at 800 cpi is 1250 μinches each small division on the oscilloscope graticule is equal to 25 μinches. Determine the amount of

skew correction needed (in micro-inches) and multiply this by a factor of ten to determine the number of 500-μinch shims to use; i.e., 150 μinches of correction x 10 = 1500 μinches. Thus, three 500-μinch shims are required.

NOTE

Shim only one head guide. A maximum of 4 shims (two-thousandths of an inch) may be used.

(9) Insert the required number of shims and replace the head guides.

(10) Recheck skew by performing skew measurement procedure described in Paragraph 6-31.

NOTE

Reverse skew may be adjusted only by realignment of the supply arm tension guide. Refer to Paragraph 6-38.

6-44. Dynamic Skew Adjustment

Correction of dynamic skew is a function of realignment of the tape path at the supply reel tension arm guide. Refer to Paragraph 6-38 for this procedure.

6-45. HEAD REPLACEMENT

The head may require replacement for one of two reasons: internal fault in the head or cable, or wear. The first reason can be established by reading a master tape; the second can be verified by measuring the depth of the wear on the head crown. In those heads which have "guttering" (grooves cut on the crown, each side of the tape path), the head should be replaced when it has worn down to the depth of the gutter. In those heads which do not have guttering, the head should be measured with a brass shim that is ten-thousandths of an inch thick. The shim width should be less than the minimum tape width (0.496 inch). The shim should be placed in the worn portion of the head crown with one side butted against the outer worn step. When the upper surface of the shim is below the unworn surface of the head crown (i.e., the head has worn to a depth of greater than 0.010 inch), the head should be replaced.

Replacement of the head is accomplished as follows.

(1) Remove the head cover.

(2) Disconnect the head connector from the Data PCBA.

(3) Loosen the screws that retain the overlay.

(4) Remove the two screws that attach the head to the deck.

(5) Ease the head cable through the hole in the deck and, by moving the overlay outward from the deck, make clearance for the head connector to pass through the deck and overlay.

(6) Check the replacement head for particles adhering to the mounting surface.

NOTE

The mounting surface must be free of all foreign substances or excessive skew will result.

(7) Route the head connector and cable through the overlay and the deck.

(8) Mate the cable connector to J2 on the Data PCBA.

(9) Attach the head with the two screws removed in Step (4).

(10) Set up the read amplifier gains as described in Paragraph 6-28.

(11) Observe the skew and adjust as necessary using procedure contained in Paragraph 6-40.

NOTE

Shim only one head guide.

(12) Replace the head cover.

6-46. PHOTO-TAB SENSOR REPLACEMENT

Replacement of the photo-tab sensor is accomplished as follows.

(1) Disconnect the cable connecting the photo-tab sensor to the EOT/BOT Amplifier PCBA.

(2) Remove the screw that retains the sensor assembly. The screw is accessible from the rear of the deck.

(3) Loosen the screws that retain the overlay.

(4) Ease the cable through the hole in the deck and, by moving the overlay outward from the deck, make clearance for the connector to pass through the deck and overlay.

(5) Insert the cable and connector of the replacement photo-sensor through the overlay and deck following the procedure outlined in Step (4).

(6) Align the surface of the photo-sensor parallel to the tape and tighten the retaining screw.

(7) Adjust the BOT and EOT amplifiers as previously described.

6-47. CAPSTAN MOTOR ASSEMBLY REPLACEMENT

Replacement of the capstan motor assembly is accomplished as follows.

(1) Remove the head cover.

(2) Remove the take-up hub by loosening one set screw accessible through the hole in the rim of the hub.

(3) Remove the capstan by loosening one set screw accessible between the overlay and the deck.

(4) Remove the screws that retain the trim assembly. These screws, with the exception of two which are located under the control panel, are accessible from the rear of the deck.

(5) Remove the trim assembly.

(6) Disconnect the plug which connects the three deck-mounted motors to the Tape Control PCBA.

(7) Remove the four leads from the capstan motor (at the connector) using the molex pin extractor tool.

(8) Remove the four screws that hold the capstan assembly.

(9) Remove the capstan assembly.

(10) Mount the replacement capstan assembly and replace the four retaining screws.

NOTE

The mounting surface must be free of all foreign substances to ensure the perpendicularity of the capstan to the tape path.

(11) Insert the four leads in the correct location in the plug. Refer to Schematic 101514 for corresponding lead colors and pin numbers.

(12) Connect the plug which connects the motor to the Tape Control PCBA.

(13) Remount the capstan and take-up hub temporarily and check the read system skew as described in Paragraph 6-40.

(14) Remove the capstan and take-up hub and reinstall the trim assembly.

(15) Reinstall the capstan and take-up hub. Tighten the set screws.

(16) Replace the head cover.

6-48. REEL SERVO BELT TENSION

The toothed belts that couple the motors to the reel hubs must have sufficient tension to prevent the teeth from skipping or servo instability due to backlash. The belts must not have excessive tension as this will cause overloading of the motor or reel shaft bearings in the radial direction. The belt tension can be adjusted as follows.

(1) Loosen the three screws that fasten the motor mounting plate to the deck stand-offs.

NOTE

The slots in the motor mounting plate allow motion of the motor in the line of action of belt tension.

(2) Adjust the pulley so that the timing belt is snug. Note the last belt tooth that is completely seated in a slot on the large pulley. (Refer to Figure 6-5.)

(3) Count two to three teeth from the last engaged tooth. Hold the large pulley to ensure that it does not turn. Depress the toothed belt at the point between the second and third teeth with sufficient force to deflect the belt flush against the gear.

CAUTION

DO NOT APPLY EXCESSIVE FORCE ON THE TOOTHED BELT.

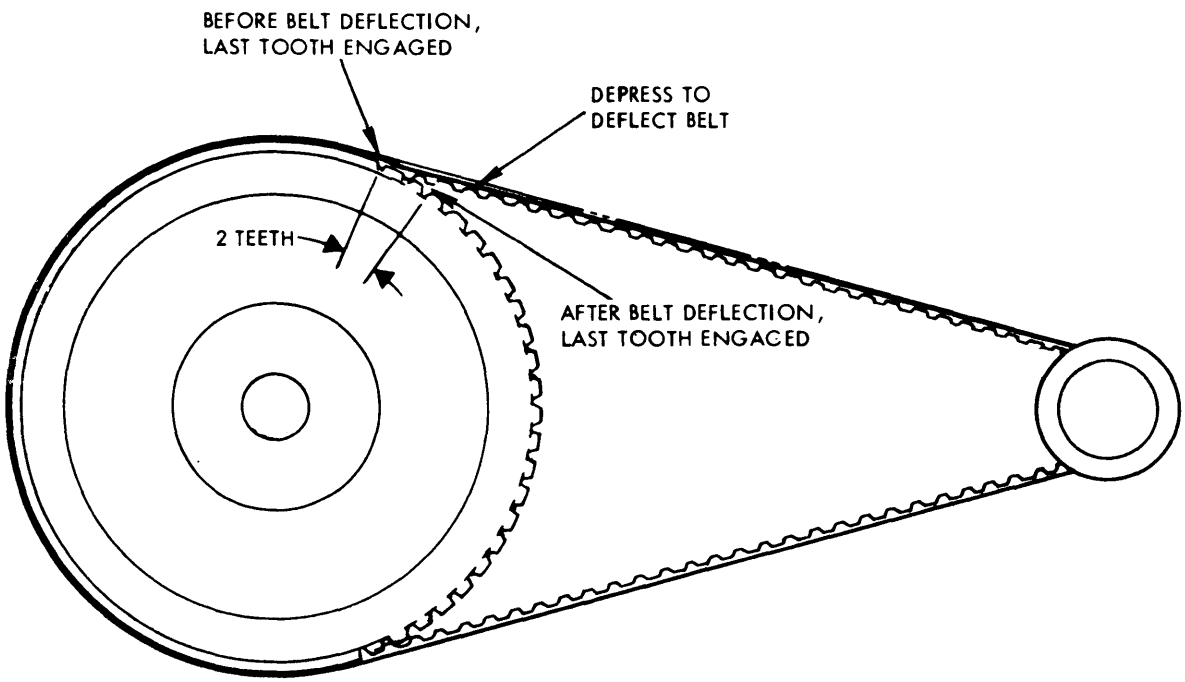


Figure 6-5. Reel Servo Belt Tension Adjustment

(4) Adjust the drive motor assembly so that the second tooth is firmly engaged in a slot on the large pulley, but the third belt tooth is not engaged.

(5) Tighten the three screws on the motor mounting plate and recheck for the condition in Step (2).

6-49. TENSION ARM GUIDES

Alignment of the tension arm guides to the head guides is most efficiently accomplished with a special tool.
The use of this tool is illustrated in Figure 6-6. Alignment is accomplished as follows. *

(1) Remove the overlay as described in Paragraph 6-46, Steps (1) through (5).

(2) Loosen the two swivel nut knobs and the two knurled nuts (refer to Figure 6-6) and slip the special tool over the head guide caps.

(3) Tighten the knurled nuts and swivel nut knobs in such a manner that the hinged clamps hold the tool's outside surface at right angles to the guide and in contact with the reference surface of the head guide caps.

(4) Loosen the tension arm lock screw and the roller guide set screw on the supply (left) tension arm.

(5) Rotate the supply tension arm until the tension arm guide mates with the end of the tool.

(6) Clamp the guide shaft in place by tightening the set screw.

(7) Adjust the parallelism of the guide and tool surface by twisting the tension arm with an Allen wrench inserted in the rotation adjustment access.

(8) Illuminate junction of the roller guide and tool surface as illustrated in Figure 6-6. Visually check alignment.

(9) Tighten the tension arm lock screw to 25 inch-pounds.

(10) Adjust the take-up tension arm in the same manner as the supply tension arm.

*Alignment is done at the factory and should not be required in the Field. Instructions are given for information only.

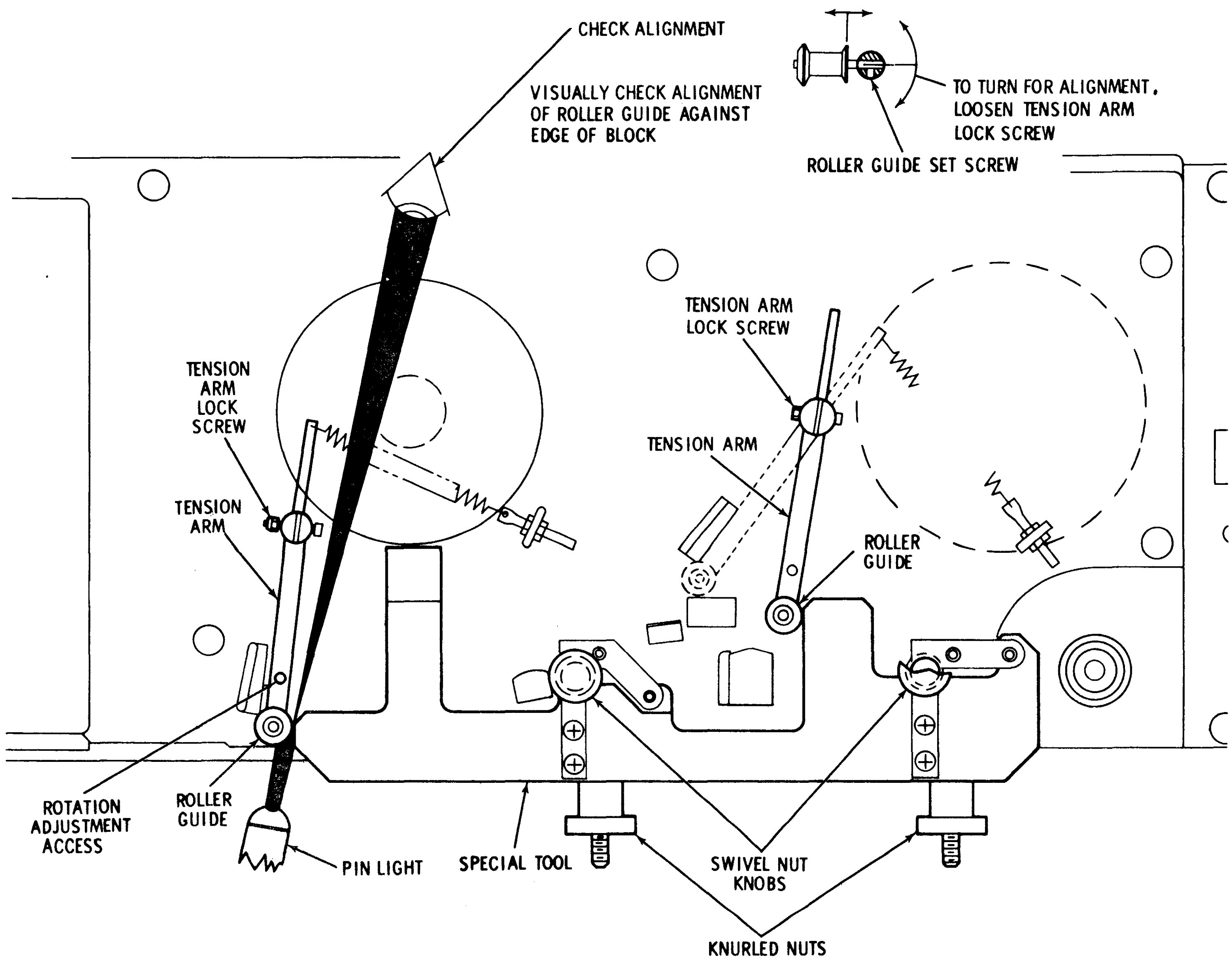


Figure 6-6. Tension Arm Guide Alignment

(11) Carefully remove the special tool and tighten the knurled nuts and the swivel nut knobs.

(12) Reinstall the capstan, take-up hub, trim, and head cover.

6-50. TAPE TENSION

Tape tension is controlled by the spring attached to each of the tension arms. The tension is adjusted by means of the anchor screws. Figure 6-7 shows the measurement and adjustment of the supply tape tension. A two-foot length of tape with loops at each end is used and after removing the trim as described in Paragraph 6-48 the tape is mounted as shown. A one-pound force gauge is used to measure the tape tension. Care must be taken to zero the scale in the correct orientation and to pull on the tape in the direction shown. The anchor screw is adjusted until the tension is 7 ounces with the arm in the center of its operating region.

Figure 6-8 shows the measurement and adjustment of the take-up tape tension. Using the same piece of tape mounted as shown with the gauge zeroed again in the correct orientation, the anchor screw is adjusted until the tension is 7 ounces with the arm in the center of its operating region.

6-51. MAINTENANCE TOOLS

The following list of tools is required to maintain the Tape Unit.

(1) Hex socket keys for 5/32, 1/8, 3/32 set screws and a splined drive socket key for a 4-40 set screw.

(2) Open-end wrenches for 3/16-, 1/4-, 5/16-, and 3/8-inch bolts.

(3) Long-nose pliers.

(4) Phillips screwdriver set.

(5) Standard blade screwdriver set.

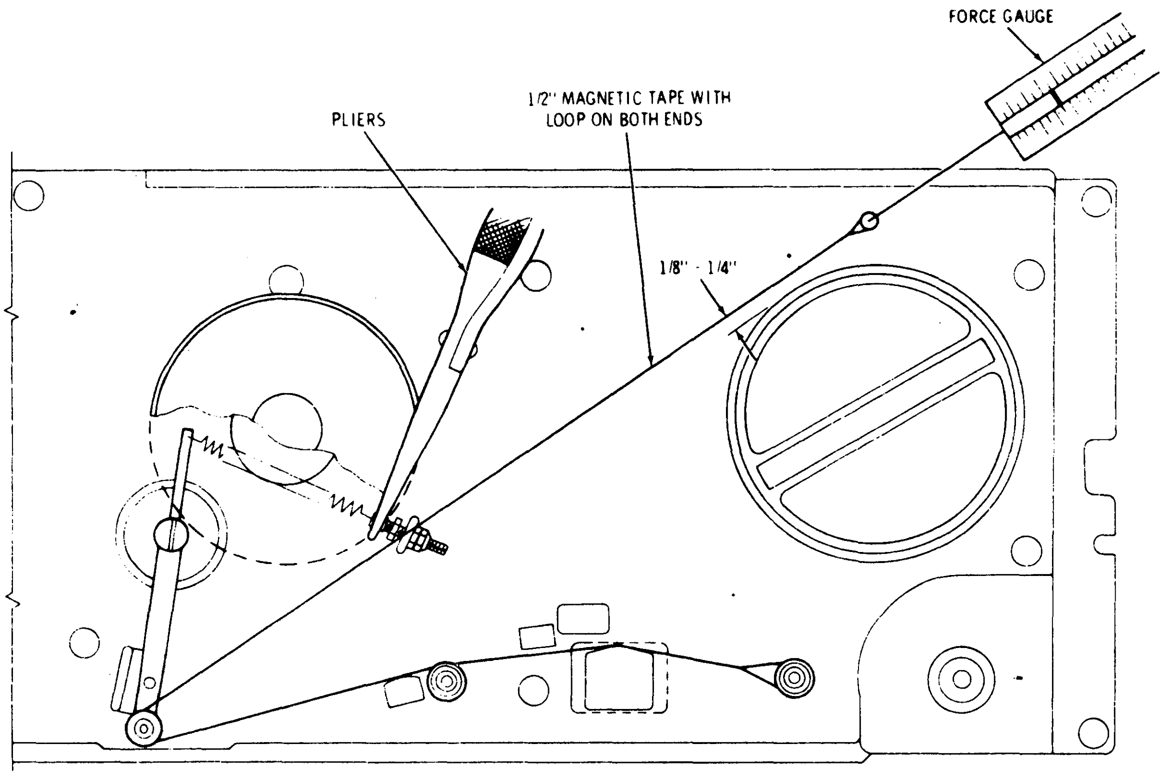


Figure 6-7. Tension Adjustment for Supply Reel

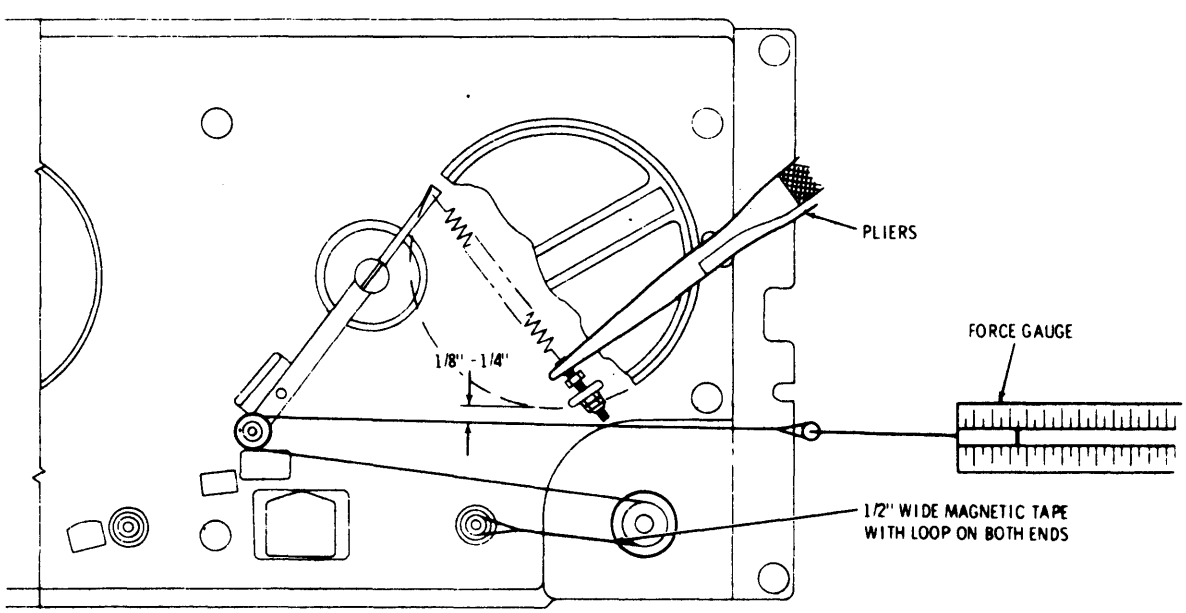


Figure 6-8. Tension Adjustment for Take-up Reel

(6) Soldering aid.

(7) Soldering iron.

(8) One-pound force gauge.

(9) Lint-free cloth.

(10) Cotton swabs.

(11) Isopropyl alcohol.

(12) Torque wrench, 0-50 inch/pounds.

(13) 0.010 brass shims (head wear measurement).

6-52. READ STATICISER DENSITY ADJUSTMENT

The duration of the read character gate is adjusted by means of variable resistors located on the Data PCBA. Nominally, the duration of the character gate is one-half of the character time.

6-53. Test Procedure

(1) Connect the interface line ISFC (J101 pin C or TP3) on the Tape Control PCBA to ground. The tape will move forward at the specified velocity.

(2) Using the signal probe of a Tektronix 543 oscilloscope (or equivalent) measure and note the duration of the waveform observed at TP10 on the Data PCBA.

NOTE

The oscilloscope should be set to trigger on the positive-going edge of the observed waveform.

(3) Calculate the ideal character gate duration using the following formula.

$$t\ (\ \text{sec}) = \frac{10^6}{2\ DV} = \text{one-half character time}$$

where

D = density in cpi (recorded tape)

V = tape speed in ips

(4) Acceptable Limits

(a) 800 cpi density, 12.5 ips, for Data C17 and Data C19 PCBA
- 52.5 μsec maximum
- 47.5 μsec minimum

(b) 556 cpi density, 12.5 ips, for Data C17 PCBA
- 75.6 μsec maximum
- 68.4 μsec minimum

(c) 200 cpi density, 12.5 ips, for Data C17 PCBA
- 210.0 μsec maximum
- 190.0 μsec minimum

6-54. Adjustment Procedure (7-track Transports)

When the acceptable limits are exceeded the following procedure is performed.

(1) Establish test configuration described in Paragraph 6-29.

(2) Connect the interface line ISFC (J101 pin C or TP3) on the Tape Control PCBA to ground. The tape will move forward at the specified velocity.

(3) Select the lower of the two packing densities (HI DEN control extinguished) on versions equipped for dual density operation.

(4) Connect a signal probe of a Tektronix (453 oscilloscope or equivalent) to TP10 on the Data C17 PCBA

(5) Connect the oscilloscope reference probe to TP13 on the Data C17 PCBA

(6) Adjust variable resistor R32 on the Data C17 PCBA to display a character gate waveform according to speed and density as follows.

(a) 556 cpi density, 12.5 ips
- 72 μsec

(b) 200 cpi density, 12.5 ips

- 200 μsec

(7) Select the higher of the two packing densities (HI DEN control illuminated) on versions equipped for dual density operation.

(8) Adjust variable resistor R27 on the Data C17 PCBA to display a character gate waveform according to speed as follows.

(a) 800 cpi density, 12.5 ips

- 50 μsec

(b) 556 cpi density, 12.5 ips

- 72 μsec

NOTE

The foregoing adjustments must be performed in the order specified.

√ 6-55. Adjustment Procedure (9-track Transports)

When the acceptable limits are exceeded the following adjustments are performed.

(1) Establish test configuration described in Paragraph 6-29.

(2) Connect the interface line ISFC (J101 pin C or TP3) on the Tape Control PCBA to ground. The tape will move forward at the specified velocity.

(3) Connect a signal probe of a Tektronix 561 oscilloscope (or equivalent) to TP10 on the Data C19 PCBA.

(4) Connect the oscilloscope reference probe to TP13 on the Data C19 PCBA.

(5) Adjust R32 onthe Data C19 PCBA to display the positive-going portion of the character gate waveform as follows for 800 cpi at 12.5 ips

- 50 μsec

6-56. Related Adjustments

The following areas must be checked and/or adjusted prior to adjusting the Read Staticisers.

(1) Read amplifier gain.

(2) Tape speed.

6-57. WRITE SKEW MEASUREMENT AND ADJUSTMENT

The read skew adjustment procedure (Paragraph 6-42) should be accomplished prior to adjustment of the write skew.

6-58. Write Skew Measurement

Measurement of write skew is accomplished by writing and simultaneously reading an all-ones tape. This is accomplished as follows.

(1) Set the vertical sensitivity of a Tektronix 543 oscilloscope (or equivalent) to 1.0 volt/cm and the horizontal range to 5 μsec/cm.

(2) Set the oscilloscope to trigger on channel 1, negative slope, alternate mode.

(3) Ensure that head assembly and tape path are clean.

(4) Load a good quality work tape with a write enable ring in place on the transport.

(5) Bring the transport to Load Point.

(6) Put the transport on-line.

(7) Apply a ground to TP6 on the Tape Control PCBA.

(8) Apply a ground to the interface line ISLT (J101 pin J) on the Tape Control PCBA.

(9) Apply a ground to the interface line ISFC (J101 pin C) on the Tape Control PCBA.

(10) Apply a ground to interface lines IWDP and IWD0 through IWD7 (J102 pins L, M, N, P, R, S, T, U, and V) of the Data PCBA.

(11) Apply negative-going pulses (+3v to 0v) of 2 μsec duration at the specified transfer rate to the interface line IWDS (J102 pin A) on the Data PCBA.

NOTE

Transfer Rate = D x V
where D = Density in cpi
V = Speed in ips
i.e., 10Kc at 800 cpi, 12.5 ips

(12) Connect the oscilloscope signal probe to TP15 in the Data PCBA and adjust the horizontal time/division "variable" control to display one complete cycle.

NOTE

With an 800 cpi tape, each cycle represents 1250 μinches. The scope graticule is divided into 10 major divisions, each of which is divided into 5 divisions; therefore

$$\frac{1250 \ \mu\text{inch}}{50 \text{ divisions}} = 25 \ \mu\text{inch/division}$$

(13) Observe that the fall time of the waveform viewed at TP15 is less than nine small divisions of the oscilloscope graticule; i.e., 225μinches. Note that this value includes the effect of gap scatter of the read head. The tape will actually be recorded with less than 150 μinches of skew.

6-59. Write Skew Adjustment

To reduce write skew to within acceptable limits the following procedure is accomplished.

(1) Perform write skew measurement procedure described in Paragraph 6-58.

(2) While observing the waveform viewed at TP15 on the Data PCBA adjust R18 on the Data PCBA to reduce the skew to less than nine small divisions of the oscilloscope graticule; i.e., 225 μinches. (See Paragraph 6-58, Step (13).)

✓ 6-60. FLUX GATE ADJUSTMENT

Crosstalk can be checked and, if necessary, reduced to within acceptable limits by mechanically positioning the flux gate. The check and adjustment procedure is accomplished as follows.

(1) Load a reel of tape with a write enable ring installed on the transport. Do not pass tape over the capstan.

(2) Apply power to the transport.

(3) Bring the transport to Load Point artificially by placing a white card between the tape and photosensor assembly and depressing the LOAD control.

(4) Place the transport on-line.

(5) Apply a ground to TP6 on the Tape Control PCBA.

(6) Apply a ground to interface line ISLT (J101 pin J) on the Tape Control PCBA.

(7) Apply a ground to interface line ISFC (J101 pin C) on the Tape Control PCBA.

(8) Apply a ground to interface lines IWDP and IWD0 through IWD7 (J102 pins L, M, N, P, S, T, U, and V) on the Data PCBA.

(9) Apply negative-going (+5v to 0v) pulses of 2 μsecond duration to the interface line IWDS (J102 pin A) on the Data PCBA.

(10) Using a Tektronix 543 oscilloscope (or equivalent) observe the waveforms at TP103 through TP903 on the Data C19 PCBA, or TP103 and TP403 through TP903 on the Data C17 PCBA.

(11) Observe that the waveforms viewed in Step (10) are approximately sinusoidal with no pronounced peaks. The

maximum allowable crosstalk voltage is 1. 0v peak-to-peak.

NOTE

If the observed waveforms in Step (10) falls within the limit specified in Step (11) no adjustment should be attempted.

(12) Partially loosen the screws which secure the flux gate assembly. Care should be taken to ensure that the flux gate spring does not move the assembly.

(13) Place a white card (e. g. , business card) between the flux gate and the magnetic head and press the flux gate assembly lightly against the head.

(14) Figure 6-9 illustrates the correct relationship between the magnetic head and the flux gate. Nominally, the correct position of the flux gate is with the center of the ferrite level with the junction between the read and write heads.

NOTE

It may be necessary to move or rotate the assembly slightly to achieve the best compromise between all tracks.

(15) Tighten the flux gate assembly screws and repeat Steps (1) through (11).

CAUTION

ENSURE ADEQUATE CLEARANCE BETWEEN THE FLUX GATE AND THE MAGNETIC HEAD (0. 005 INCH MINIMUM). FAILURE TO ALLOW CORRECT CLEARANCE WILL RESULT IN DAMAGE TO THE HEAD.

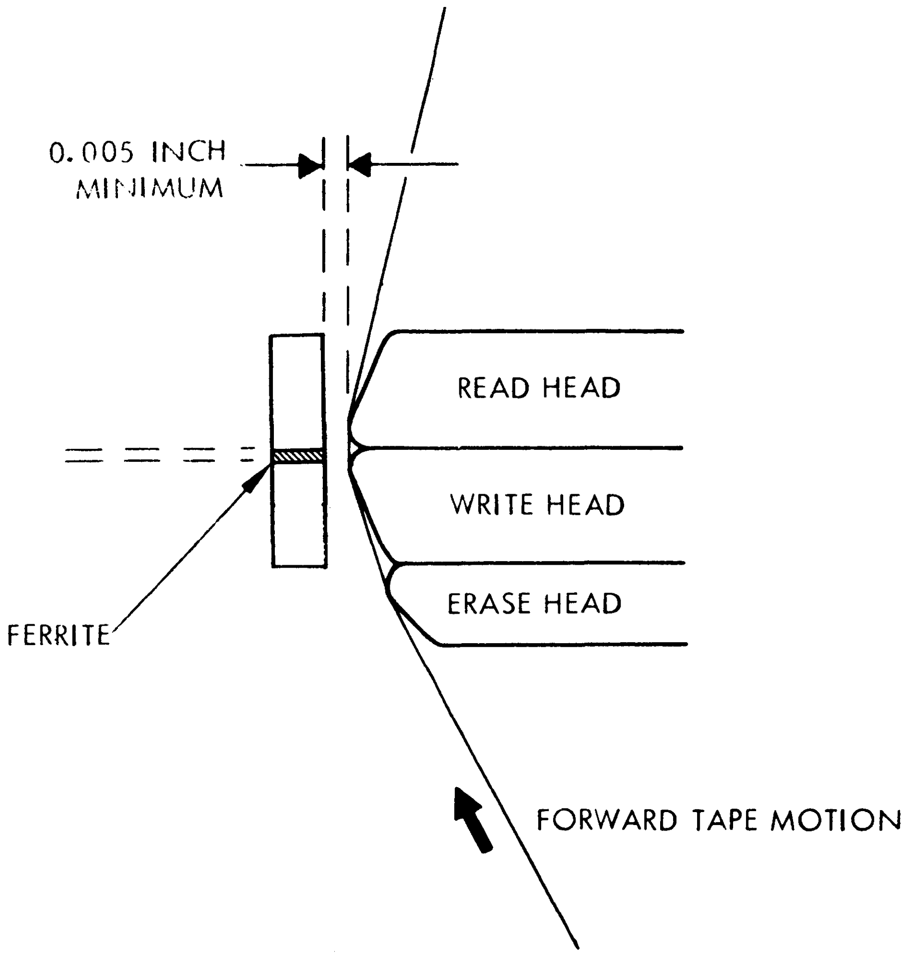


Figure 6-9. Flux Gate Adjustment

6-61. TROUBLESHOOTING

Table 6-3, System Troubleshooting chart, provides a means of isolating faults, possible causes, and remedies. The troubleshooting chart is used in conjunction with the schematics, assembly drawings, and wiring diagrams in Section VII.

Table 6-3

System Troubleshooting

Symptom	Probable Cause	Remedy	Reference
Tape does not tension and the capstan shaft rotates freely when the LOAD control is depressed for the first time after threading tape.	Interlock relay K1 does not close.	Check operation of relay. Replace if necessary.	Paragraph 5-5
	LOAD control is not operative.	Check operation of control. Replace if necessary.	Paragraph 5-5
	Relay driver defective.	Check collector voltage of Q1 with LOAD control depressed. It should be less than +1 volt. If greater, isolate defective relay driver component and replace.	Paragraph 5-5
Tape is tensioned when the LOAD control is depressed, but tension is lost when control is released.	Relay latching contacts 15 and 16 do not make.	Check that voltage at TP13 goes to +5 volts when LOAD control is depressed.	Paragraph 5-5
	Limit switch is not operative.	Adjust as described in Paragraph 6-41 possibly replace limit switch assembly.	Paragraph 6-41
Tape unwinds or tension arm hits stop when the LOAD control is depressed for the first time.	Tape is improperly threaded.	Rethread tape - see molded arrows on overlay.	Paragraph 3-3
	+5 or -5 volts is missing from tension arm sensor.	Check tension arm sensor lamps. Isolate problem if lamp is extinguished.	Paragraph 6-42
	Fault in reel servo amplifier.	Check that movement of reels responds to tension arm position without tape on the transport.	Paragraph 5-5

Table 6-3

System Troubleshooting (Continued)

Symptom	Probable Cause	Remedy	Reference
Tape "runs away" or rewinds when LOAD control is depressed for the second time.	Fault on Tape Control PCBA or capstan motor assembly.	Replace or repair Tape Control PCBA or capstan motor assembly.	Paragraph 5-4 or Paragraph 6-56
Tape runs past the BOT marker.	BOT tab dirty or tarnished.	Replace tab or increase sensitivity of photosensor amplifier.	Paragraph 6-13
	Photosensor not adjusted.	Adjust photosensor amplifier.	Paragraph 6-13
	Photosensor or amplifier defective.	Check for +3.8v to +4.2v at TP2 on EOT/BOT amplifier PCBA with blank tape under sensor. Check that voltage drops to at least +2.8v when tab is under the photosensor.	Paragraph 6-13
	Logic fault (Load flip-flop does not reset).	Replace or repair Tape Control PCBA.	Paragraph 5-5
Transport does not move in response to SYNCHRONOUS FORWARD or SYNCHRONOUS REVERSE commands.	Interface cable fault or receiver fault.	Check levels at outputs and inputs of receivers on Tape Control PCBA. Replace or repair cable or Tape Control board.	Paragraph 5-5
	Transport is not READY.	Replace or repair Tape Control board.	Paragraph 5-5
	Fault in ramp generator or capstan servo amplifier.	Check TP6 on Tape Control board. Replace or repair Tape Control board.	Paragraph 5-5

Table 6-3

System Troubleshooting (Continued)

Symptom	Probable Cause	Remedy	Reference
Transport responds to SYNCHRONOUS FORWARD command, but tape is not written.	Write current is not enabled.	Check presence of Write Enable ring on supply reel (WRT EN indicator should be lit). Check TP8 on Tape Control board (should be +5v for writing). Replace Write Lockout assembly if faulty. Check that WRT POWER level is +5v on Data board.	Paragraph 5-5
	Write status or MOTION signal to Data board is not correct.	Check receiver on Tape Control board for WRITE status and on Data board for WRITE status.	Paragraph 5-5
		Check Data board for MOTION signal. Replace or repair Data board or Tape Control board if faulty.	Paragraph 5-5
	WRITE DATA or WRITE DATA STROBE is not received correctly on Data board from interface.	Check presence of correct levels on Data board. Replace or repair Data board or interface cable if faulty.	Paragraph 5-5
	Head not plugged in.	Check J2 on Data board.	—

Table 6-3

System Troubleshooting (Continued)

Symptom	Probable Cause	Remedy	Reference
Data are incorrectly written.	Incorrect data format.	Use correct format.	
	Fault on one track due to failure in write circuits.	Check receiver and write amplifier on Data board. Replace or repair Data board if faulty.	Paragraph 5-3
	Intermittent WRT POWER, WRITE, MOTION, or WARS signal.	Examine those signals and replace or repair Tape Control board or Write Lockout assembly or Data board if faulty.	Paragraph 5-3 and Paragraph 5-5
	Write deskew circuit faulty.	Check TP5 for a sequence of 10 pulses for each WRITE DATA STROBE. Replace Data board if necessary.	Paragraph 5-3
Correct Tape cannot be read.	Interface cable or transmitter fault.	Replace or repair interface cable or Data board.	Paragraph 5-3
	Head is not plugged in.	Check J2 on Data board. Check J3 on Data board.	—
	Tape tracking skew is badly adjusted.	Readjust according to description in Section VI.	Paragraph 6-47

Table 6-3

System Troubleshooting (Continued)

Symptom	Probable Cause	Remedy	Reference
Correct tape cannot be read (continued)	Head and guides need cleaning.	Clean head and guides.	Paragraph 6-4
	Tape cleaner needs emptying.	Remove tape cleaner and clean.	Paragraph 6-4
	Read amplifier gains are incorrectly adjusted.	Check and adjust amplifier gains.	Paragraph 6-28
	Faulty write amplifier causes current to be passed through head while reading.	Check write amplifier output test points and replace or repair Data board if faulty.	Paragraph 5-3
	Component fault in read channel.	Check test points on Data board. Replace or repair Data board.	Paragraph 5-3
	Read Staticiser adjustment faulty.	Check TP10 on Data board. Check duration of positive portion of waveform is one-half of a bit time.	Paragraph 6-34

SECTION VII

SCHEMATICS, CARD ASSEMBLIES, LOGIC LEVELS AND WAVEFORMS

7-1. INTRODUCTION

This section includes the schematics, card assemblies, and logic level and waveform definitions.

7-2. Reserved for future use.

7-3 Reserved for future use.

7-4. LOGIC LEVELS AND WAVEFORMS

The Tape Unit control and interface logic uses the DTL 800 Series of logic elements. Logic levels are defined as follows.

+5 volts	logical true
+0.4 volt	logical false

All basic waveform names are chosen to correspond to the logical true condition; e.g., SET WRITE STATUS (SWS) enables the write circuits when it is logically true (+5 volts), or disables the write circuits when it is logically false (0 volt).

The inverse of a waveform is denoted by the prefix "N". Therefore, NBOT will be +0.4 volt when the BOT tab is under the photosensor head, or a minimum of +3.4 volts otherwise.

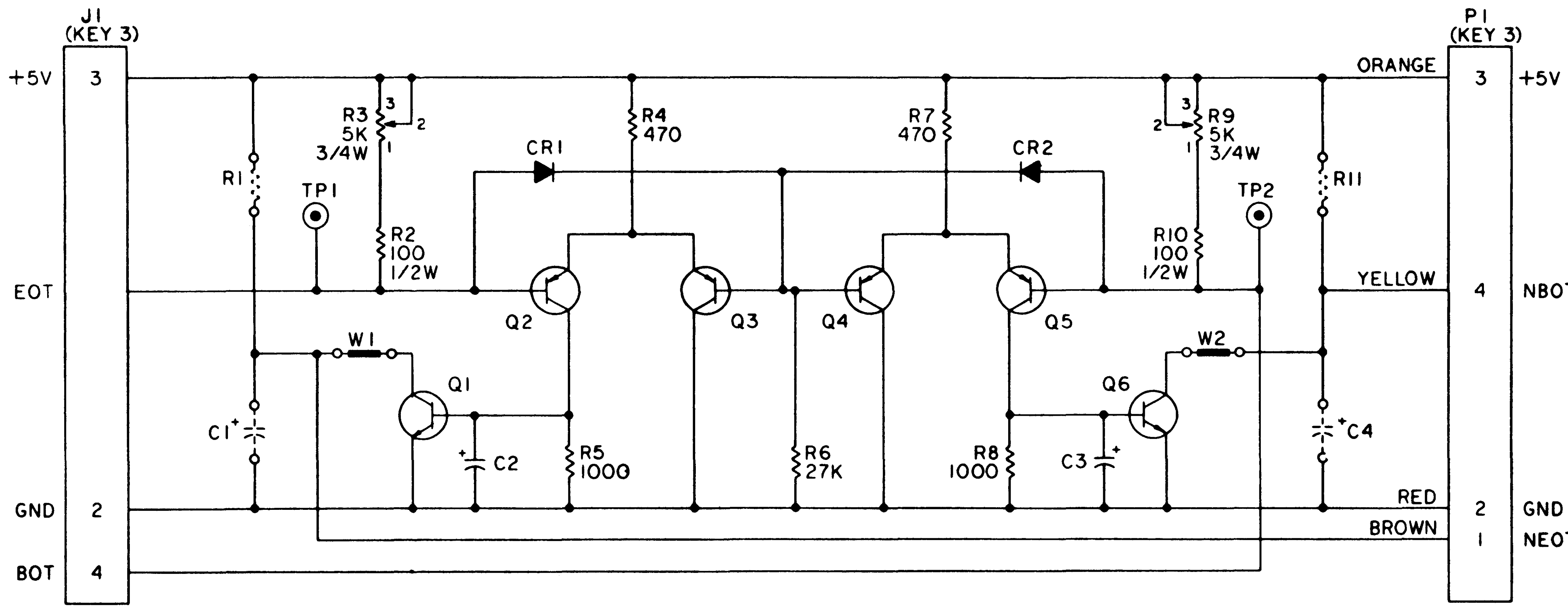
All interface lines connecting the Tape Unit to the controller are prefixed by "I".

All interface waveforms are low true with logic levels as follows.

1000 ohm pullup	+5 volts	logical false
220/330 ohm divider	+3 volts	
	0.4 volt	logical true

For example, ISFC (SYNCHRONOUS FORWARD command) will be 0.4 volt when the transport is being driven in the forward direction, or +3 volts (+5v) otherwise.

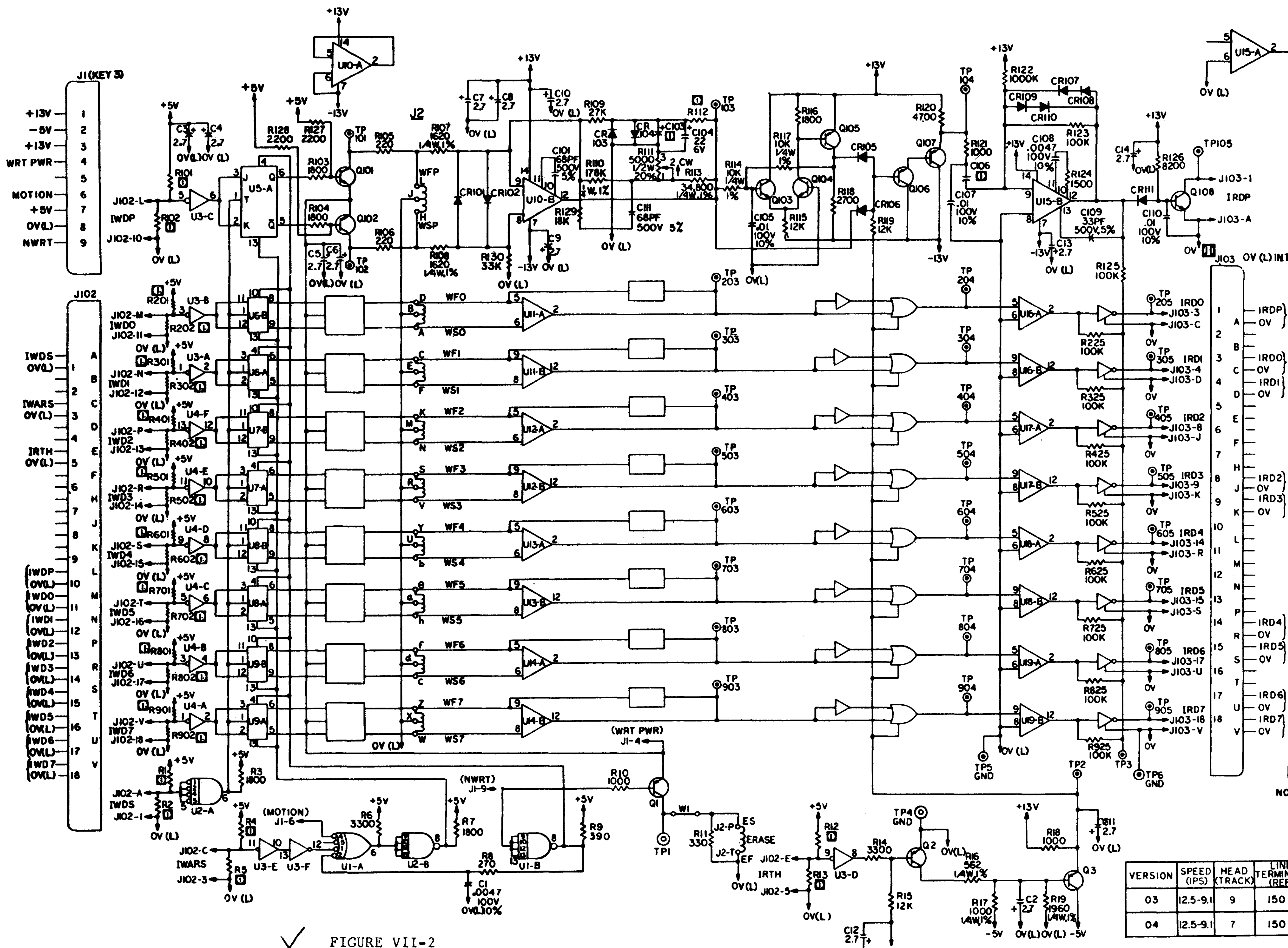
The Glossary contains the waveform mnemonics referred to in this manual.



3. ALL RESISTORS ARE 1/4W, ±5%.
2. ALL CAPACITORS ARE 2.7UF, 35V, ±20%.

NOTES: UNLESS OTHERWISE SPECIFIED:

FIGURE VII-1
EOT/BOT AMPLIFIER



2 REFERENCE DESIGNATIONS		
LAST	USED	DELETED
C911	C14	C102-C902
CR911		
R930	R19	
Q908	Q3	
	U19	
TP905	TP6	
	W-1	

8 PIN 7 OF ALL ICS IS OV (L)
PIN 14 OF ALL ICS IS +5V.

6. ALL CAPACITORS IN MICROFARADS, 35V, 20%.

4. ALL RESISTORS IN OHMS, 1/4 W, 5 %.

3. CIRCUIT 100 IS TYPICAL OF CIRCUIT 200 THRU 900.

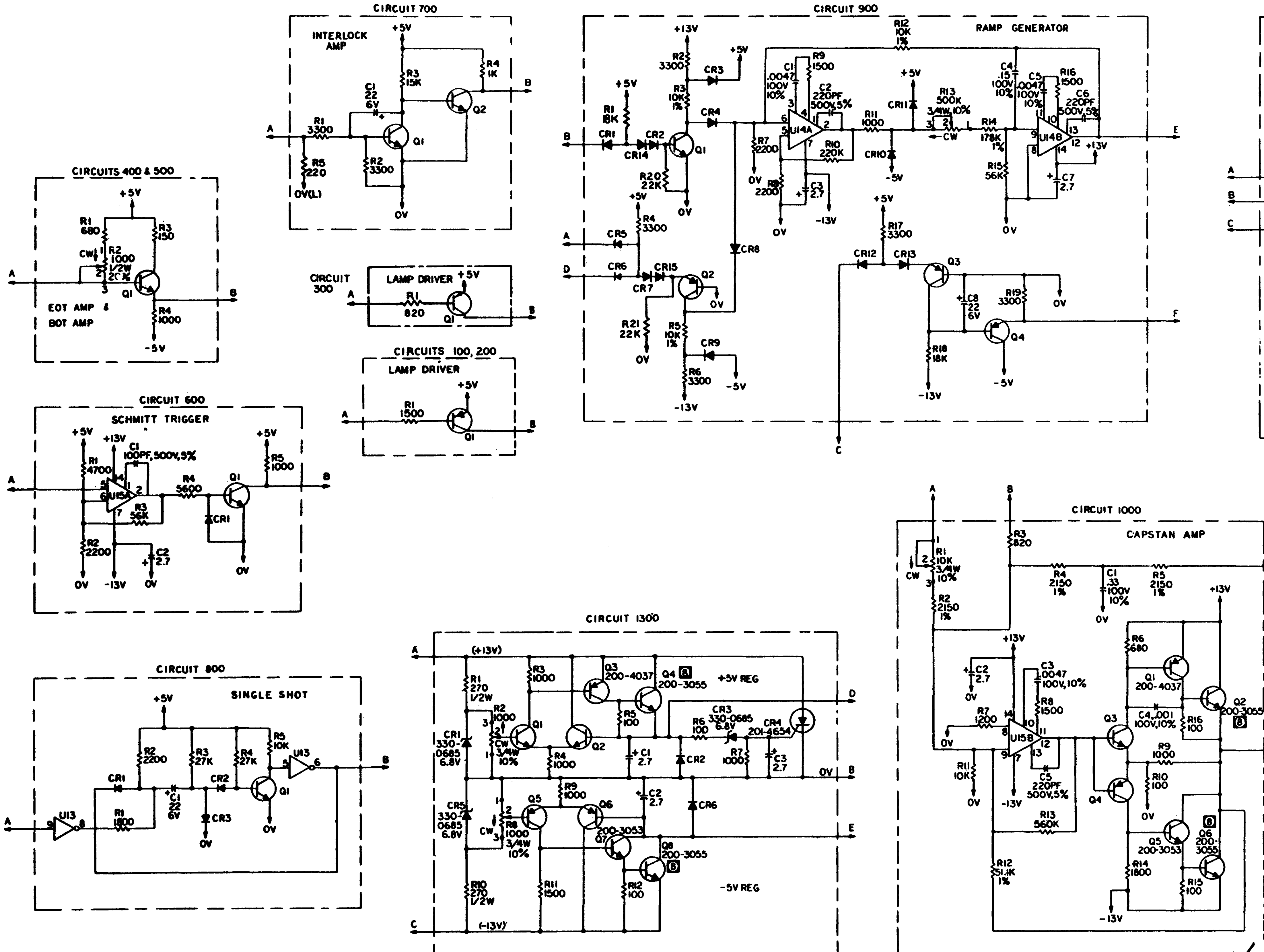
2 3 DIGIT REF. NOS. ARE ASSIGNED TO REPETITIOUS CIRCUITS EX: TP101 IS CIRCUIT 100 TP901 IS CIRCUIT 900 SINGLE DIGIT NOS. ARE ASSIGNED TO NON-REPETITIVE CIRCUITS: EX: TP1-TP2

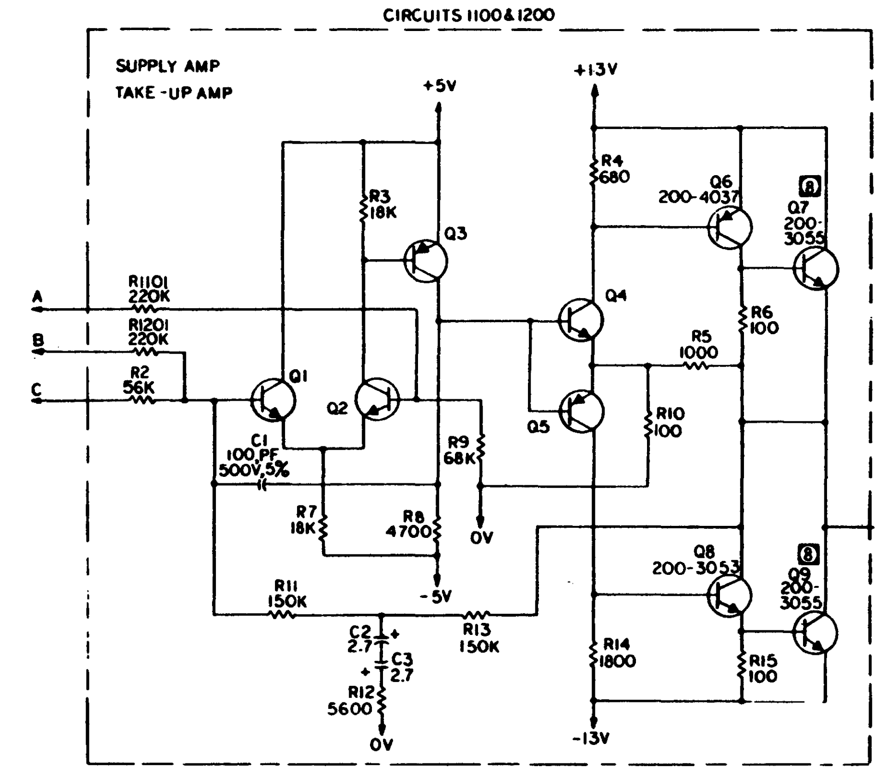
1 SEE VERSION TABLE FOR VALUE.

NOTES: UNLESS OTHERWISE SPECIFIED

VERSION	SPEED (IPS)	HEAD (TRACK)	LINE TERMINATOR (REF)	C103-903	R112-912	C106-906	R101-901 R1,R4,R12	R102-R902 R2,R5,R13	CKTS USED
03	12.5-9.1	9	150	OMIT	8200	0.0068UF 100V 10%	220	330	ALL
04	12.5-9.1	7	150	OMIT	8200		220	330	100, 400-900

FIGURE VII-2
DATA "A"



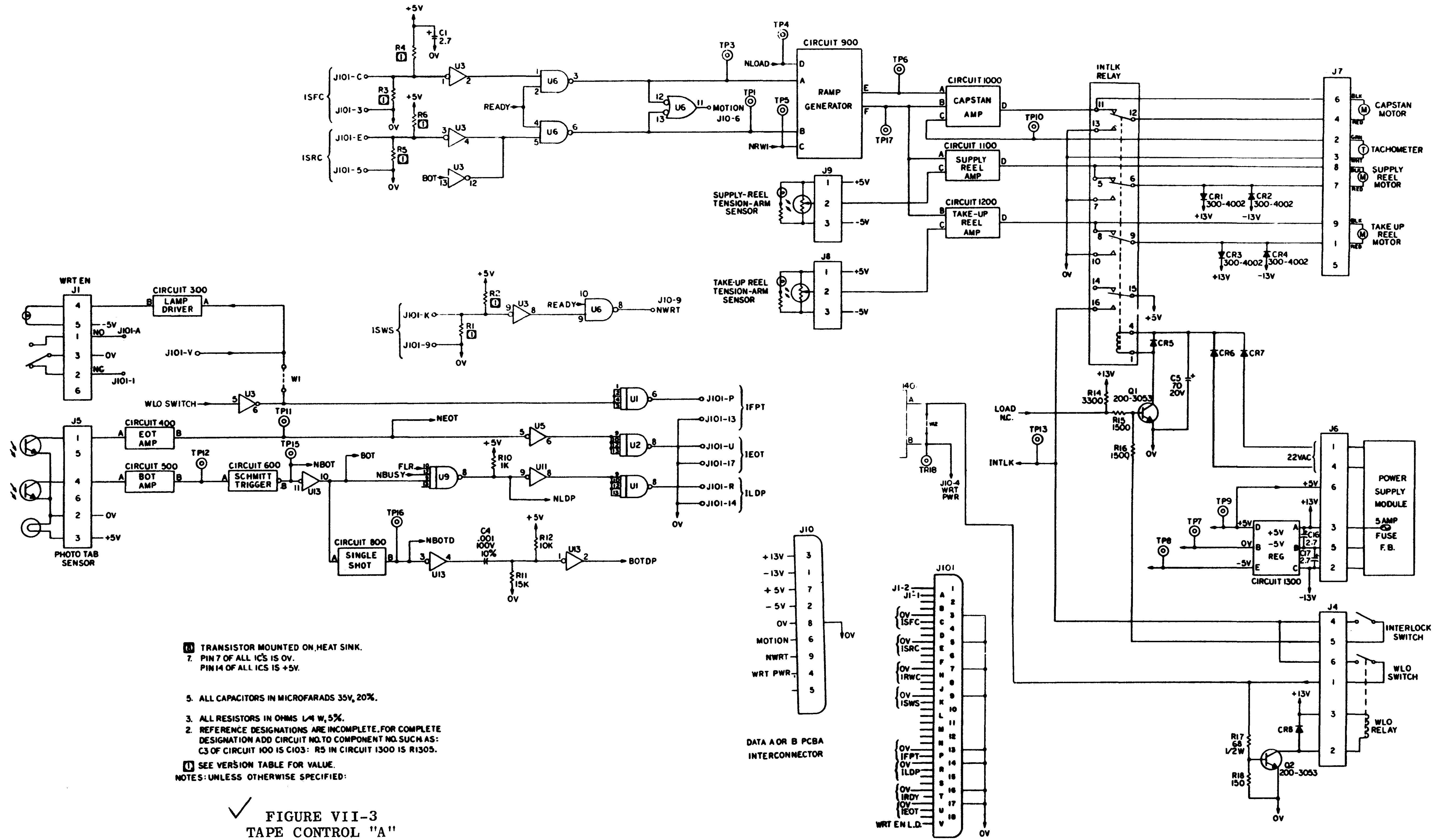


VERSION	R2, R4, R6, R8	R1, R3, R5, R7
-02	220	330

REFERENCE DESIGNATIONS 2

LAST USED		DELETED
C1303	C17	C1401
CR1306	CR8	R1401 THRU R1404
R1312	R18	R19, R20
Q1308	Q2	Q1401,1402
U1015	U15	U16
	TP18	
	W1	

FIGURE VII-2
TAPE CONTROL "A"
SHEET 1 OF 3



NOTES: UNLESS OTHERWISE SPECIFIED:

1. SEE VERSION TABLE FOR VALUE.
2. REFERENCE DESIGNATIONS ARE INCOMPLETE. FOR COMPLETE DESIGNATION ADD CIRCUIT NO. TO COMPONENT NO. SUCH AS: C3 OF CIRCUIT 100 IS C103; R5 IN CIRCUIT 1300 IS R1305.
3. ALL RESISTORS IN OHMS 1/4 W, 5%.
5. ALL CAPACITORS IN MICROFARADS 35V, 20%.
7. PIN 7 OF ALL IC'S IS 0V. PIN 14 OF ALL ICS IS +5V.
8. TRANSISTOR MOUNTED ON HEAT SINK.

FIGURE VII-3
TAPE CONTROL "A"
SHEET 2 OF 3

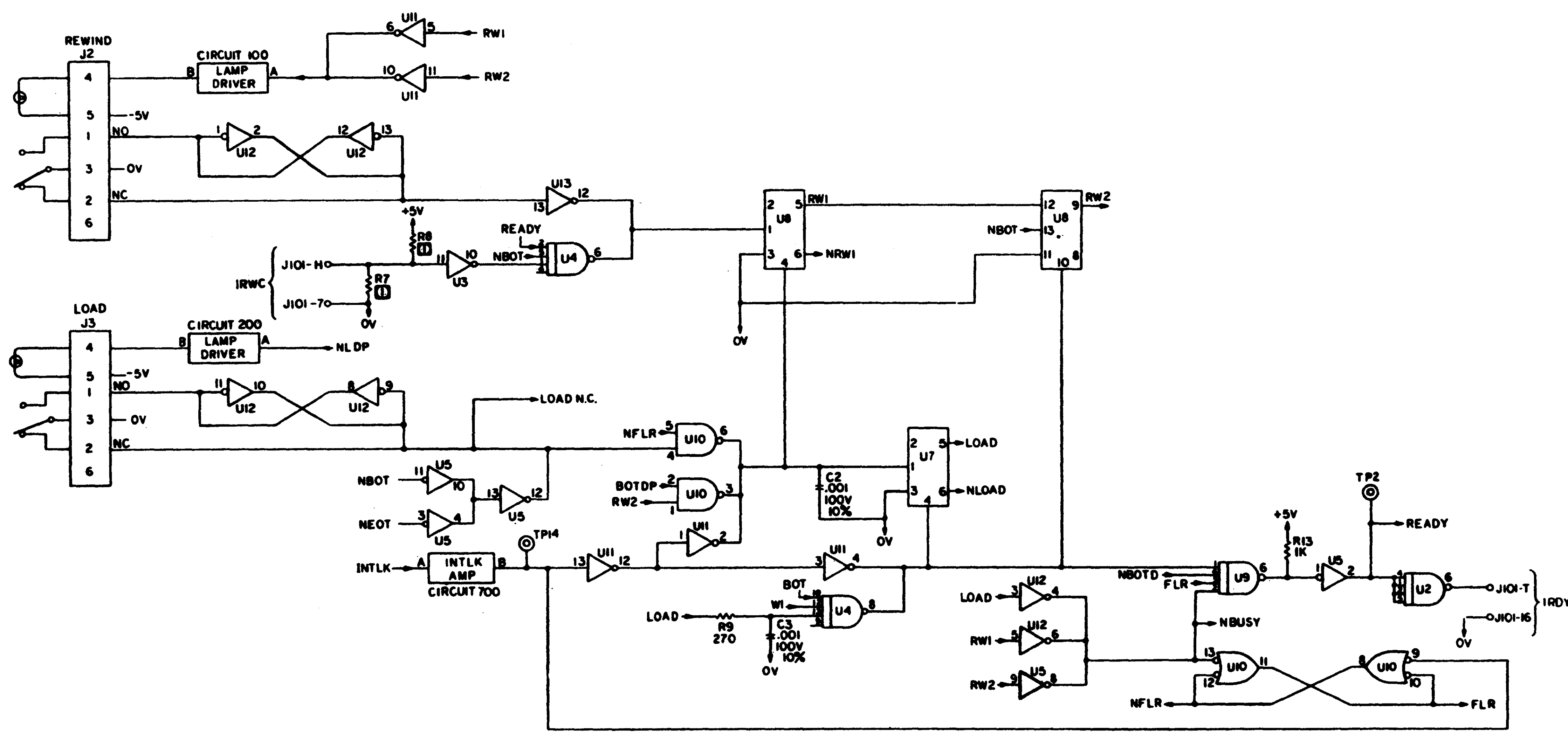


FIGURE VII-4
TAPE CONTROL "A"
SHEET 3 OF 3

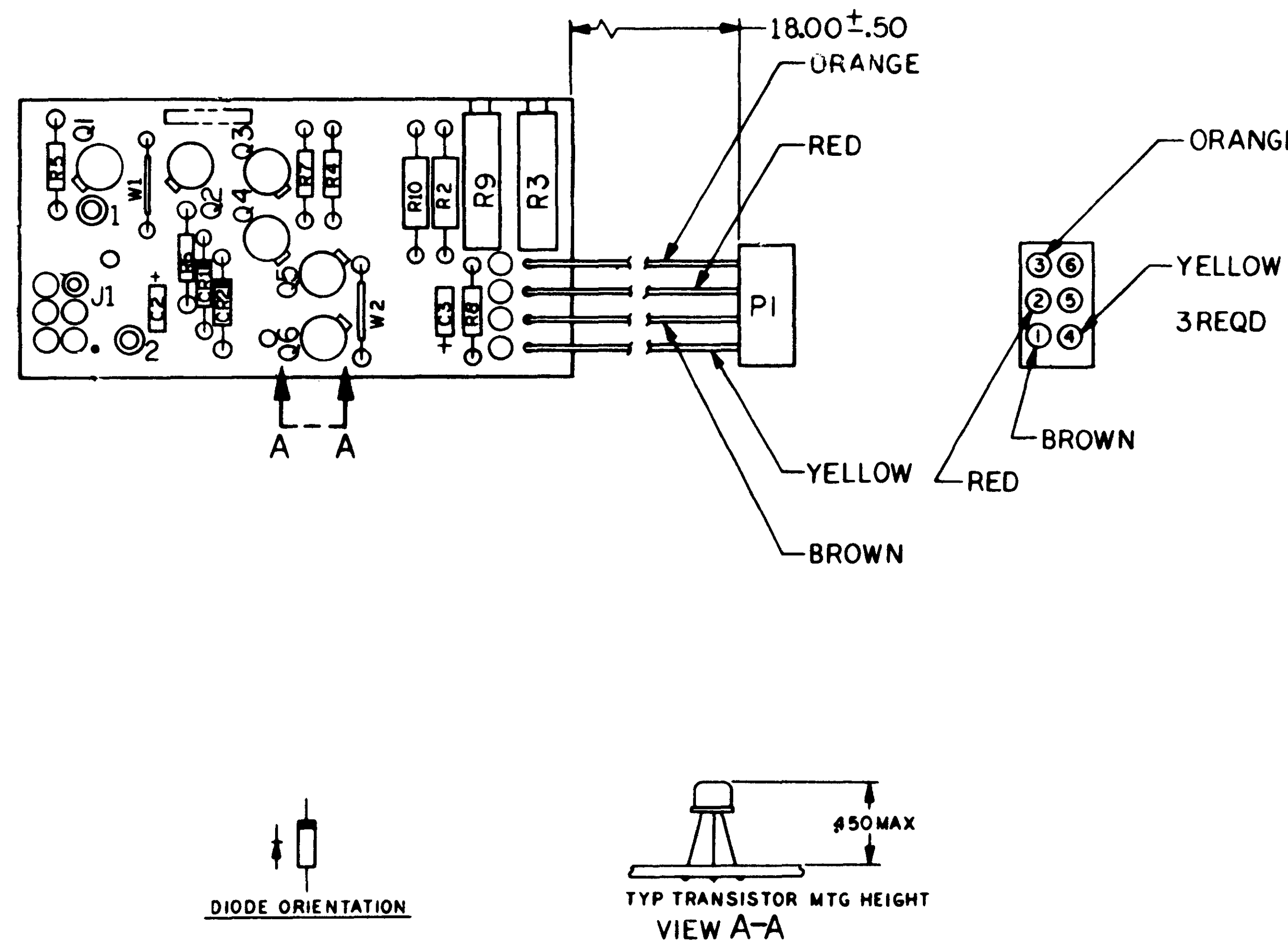
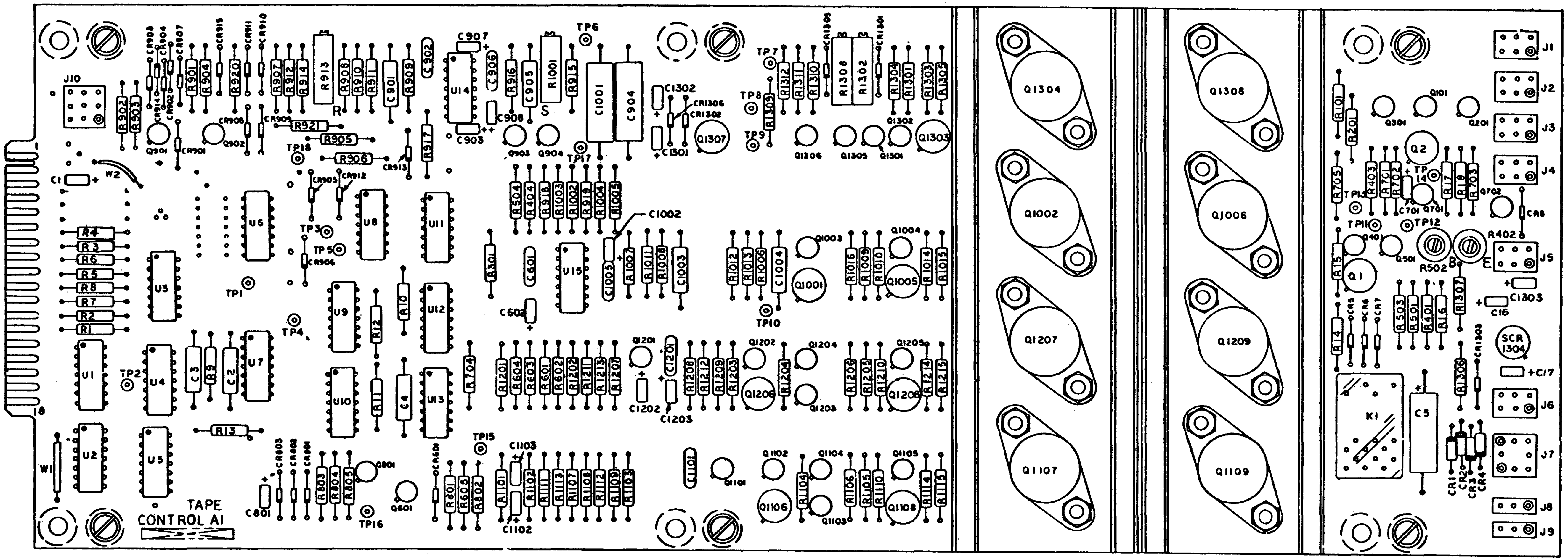
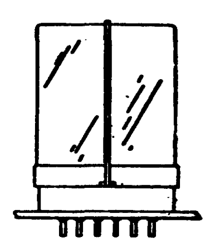


FIGURE VII-5
EOT/BOT AMPLIFIER ASSEMBLY DRAWING

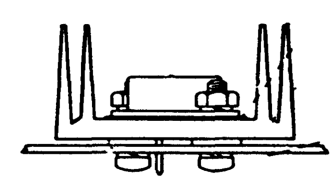




VIEW E-E

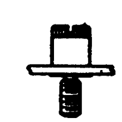
VERSION NUMBER AND ISSUE LETTER.
2. ASSEMBLE PER STANDARD MFG. METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED



VIEW B-B
TYPICAL - 2 PLACES

VIEW D-D
ROTATED 90° CW
TYP TO-5 MTG CONFIG.



VIEW A-A
TYPICAL - 6 PLACES

TYPICAL TRANSISTOR MTG HEIGHT
VIEW C-C ROTATED 90° CCW

FIGURE VII-6
CONTROL "A" ASSEMBLY DRAWING

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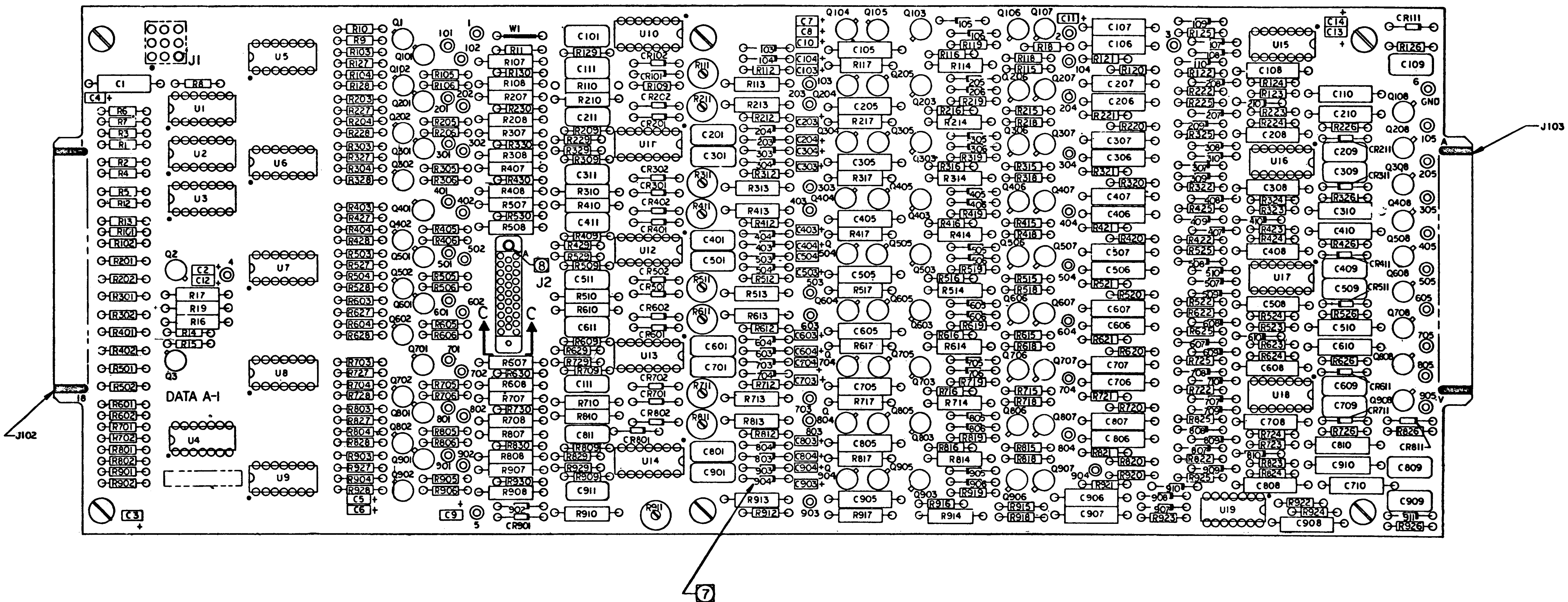
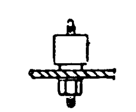
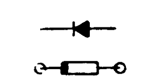


8 CONNECTOR ORIENTATION.

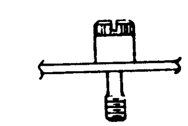
7 DESIGNATION CR, IS INTENTIONALY OMITED ON SOME DIODES FOR CLARITY.



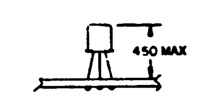
SECTION C-C
MTG DETAIL FOR J2



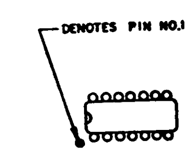
DIODE ORIENTATION



VIEW A-A
TYP-6 PLACES



TYP TRANSISTOR MTG HEIGHT
VIEW B-B



IC ORIENTATION

2 ASSEMBLE PER STANDARD MANUFACTURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED.

FIGURE VII-7
DATA "A" ASSEMBLY

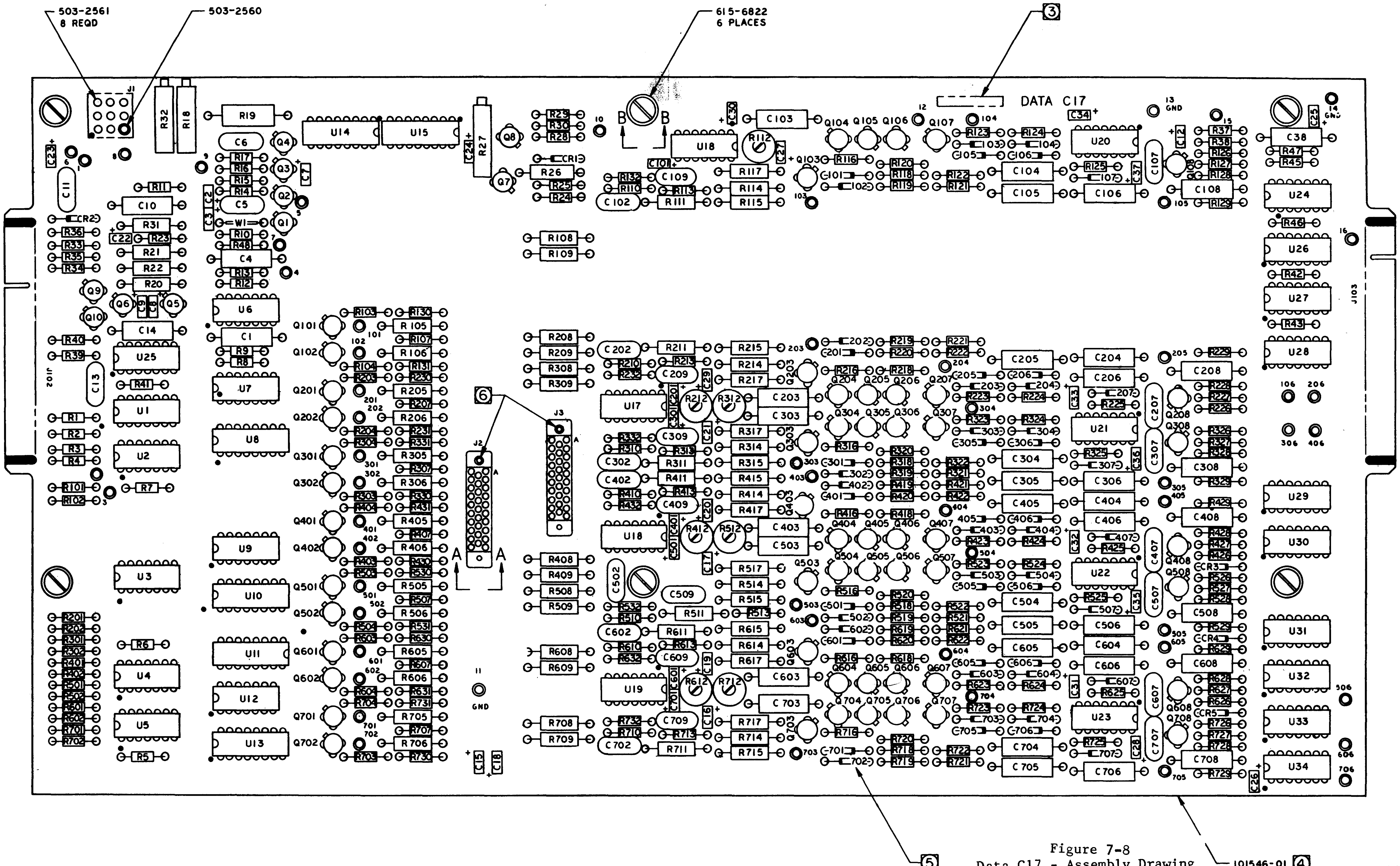


Figure 7-8
Data C17 - Assembly Drawing

Printed in U.S America 2-7-72

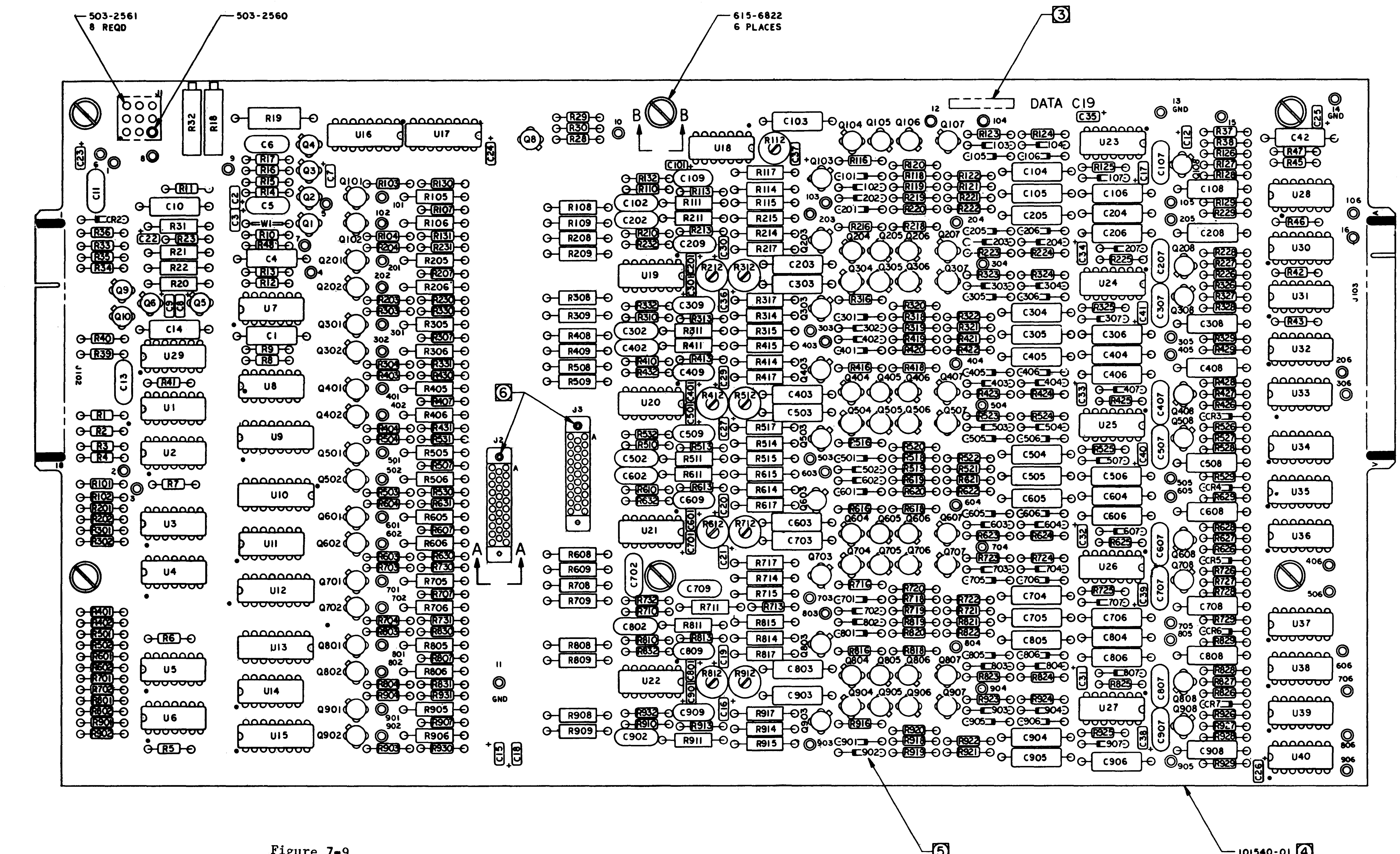
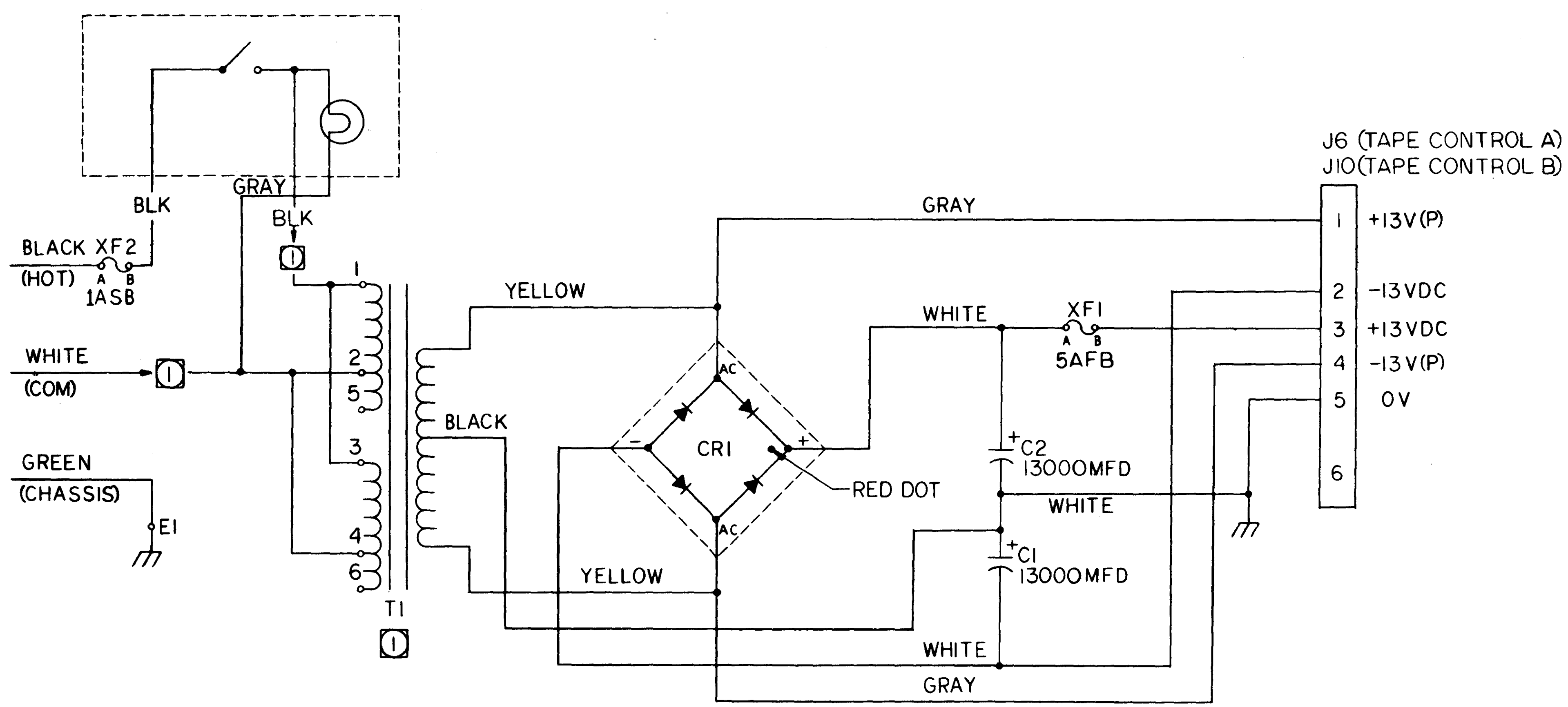


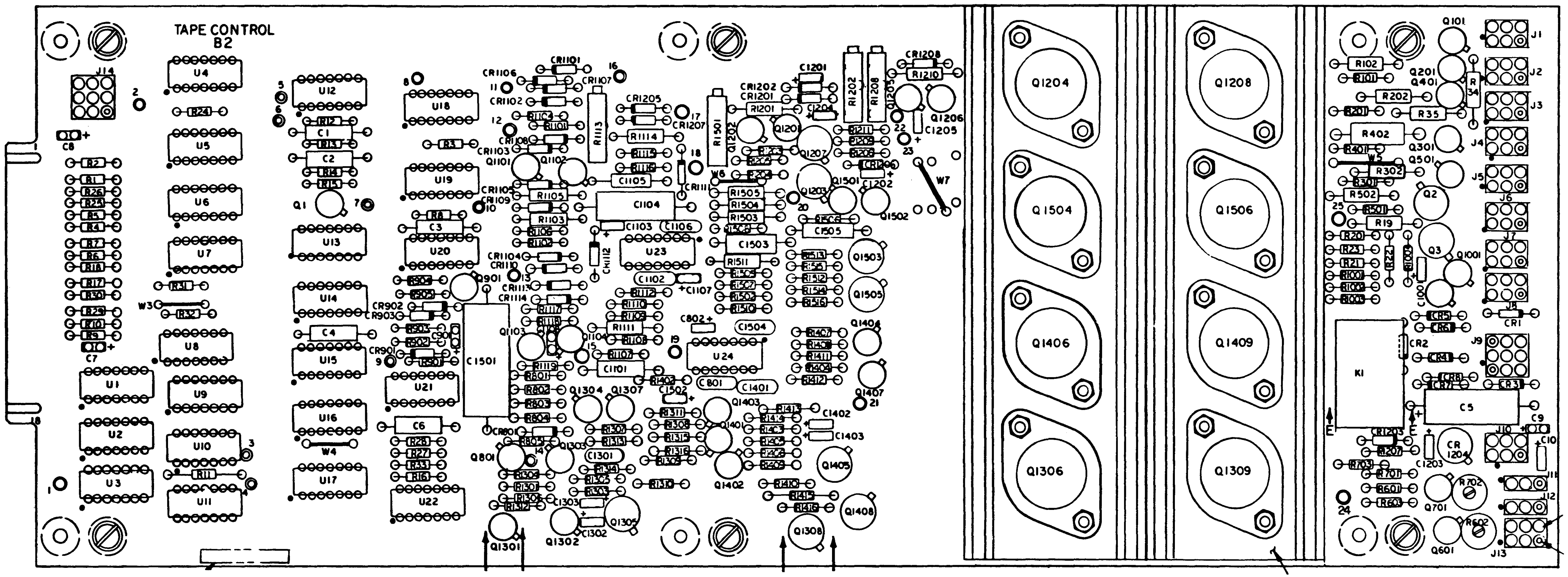
Figure 7-9
Data C19 - Assembly Drawing



1 TABLE I

TERMINAL CONNECTORS FOR LINE VOLTAGE VARIATIONS		
LINE VOLTS	LINE INPUT	CONNECT:
115	1 & 2	1 TO 3 & 2 TO 4
125	1 & 5	1 TO 3 & 5 TO 6
230	1 & 4	2 TO 3
240	1 & 4	5 TO 3
250	1 & 6	5 TO 3

Figure 7-10
Power Supply



MODEL	ASSY	W1	W2	W3	W4	W5	W6	W7
HI DEN LOCAL/ SELECT/ONLINE AT BOT	10527-01			X	X	X	X	X

REFERENCE DESIGNATIONS 2

LAST USED		DELETED
C1505	C10	
CR1208	CR8	
R1516	R35	
Q1506	Q3	
	U24	
	TP21	
	W7	

11. R1 USED ON CIRCUIT 1300 ONLY
    R2 USED ON CIRCUIT 1400 ONLY
10. U1,U4,U13,U16,U19,U21 ARE 700-8360.
    U2,U3,U5,U7,U8,U20,U22,U18 ARE 700-8440.
    U6,U10 THRU U12,U17, ARE 700-8460.
    U9,U14,U15 ARE 700-8530
    U23,U24 ARE 400-1437.
9. FOR ASSEMBLY DRAWING SEE 101527
   FOR SPECIFICATION DRAWING SEE 101530
8. TRANSISTOR MOUNTED ON HEAT SINK.
7. PIN 7 OF ALL IC'S IS 0V, EXCEPT U23 & U24
   PIN 14 OF ALL IC'S IS +5V, EXCEPT U24 & U23
6. ALL NPN TRANSISTORS ARE PEC 200-3946
   ALL PNP TRANSISTORS ARE PEC 200-3251
5. ALL CAPACITORS IN MICROFARADS 35V, 20%.
4. ALL DIODES ARE PEC 300-4446
3. ALL RESISTORS IN OHMS 1/4W, 5%.
2. REFERENCE DESIGNATIONS ARE INCOMPLETE. FOR COMPLETE DESIGNATION ADD CIRCUIT NO. TO COMPONENT NO. SUCH AS: C3 OF CIRCUIT 100 IS C103: R5 IN CIRCUIT 1300 IS R1305.
1. SEE VERSION TABLE FOR USE.

NOTES UNLESS OTHERWISE SPECIFIED

Figure 7-11
Tape Control B2 - Assembly Drawing

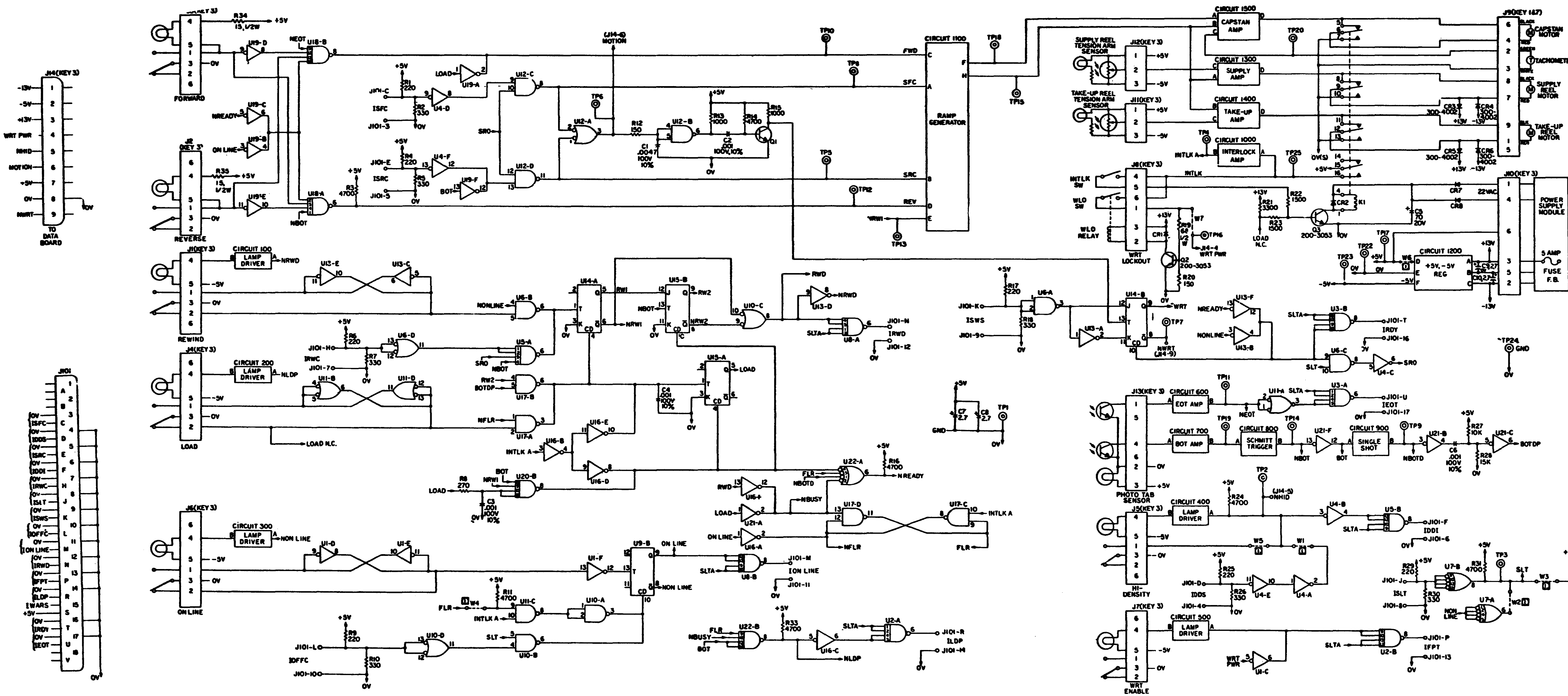


Figure 7-12
Tape Control B2 - Logic Schematics

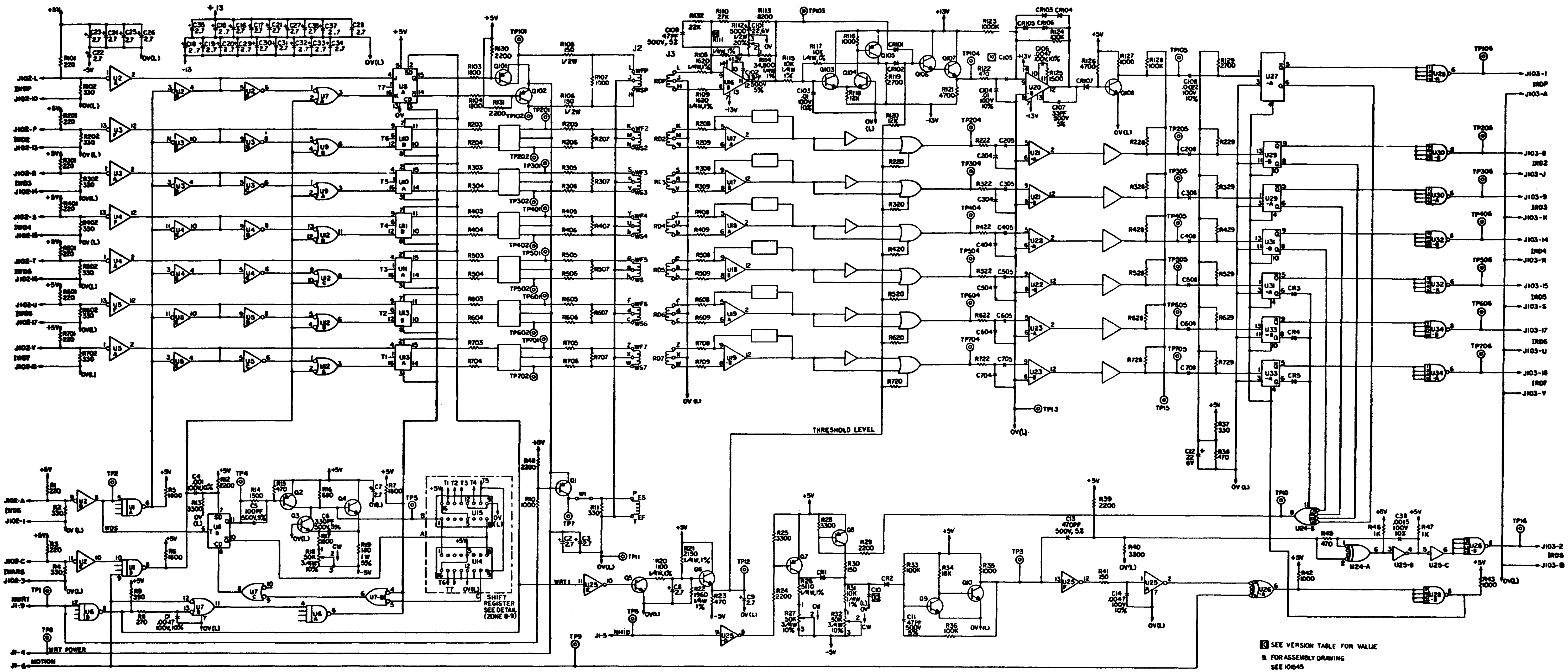


Figure 7-13
Data C17 - Logic Schematic

REFERENCE DESIGNATOR

LAST USED		NOT USED
R732	R48	R44
C709	C38	
Q708	Q10	
CR707	CR5	
TP706	TP16	
	U34	
	W1	

VERSION TABLE

VERSION	SPEED (IPS)		C10	C105-705		RII-711
-01	9.1 THRU 12.5		131-6820	131-3320		104-1783

[C] SEE VERSION TABLE FOR VALUE

9. FOR ASSEMBLY DRAWING SEE 101545
FOR SPECIFICATION DRAWING SEE 101548.

8. U2-5,25 ARE 701-8360.
U16,24,26,28,30,32,34 ARE 701-8440.
U7,9,12 ARE 701-8460.
U27,29,31,33 ARE 701-8530.
U16-23 ARE 400-1437.
U8,10,11,13 ARE 701-7476
U14,15 ARE 701-7496.

7. PIN 7 OF ALL IC'S IS OV
PIN 14 OF ALL IC'S IS +5V

6. ALL NPN TRANSISTORS ARE 200-3946.
ALL PNP TRANSISTORS ARE 200-3251.

5. ALL CAPACITORS IN MICROFARADS, 35V, 20%.

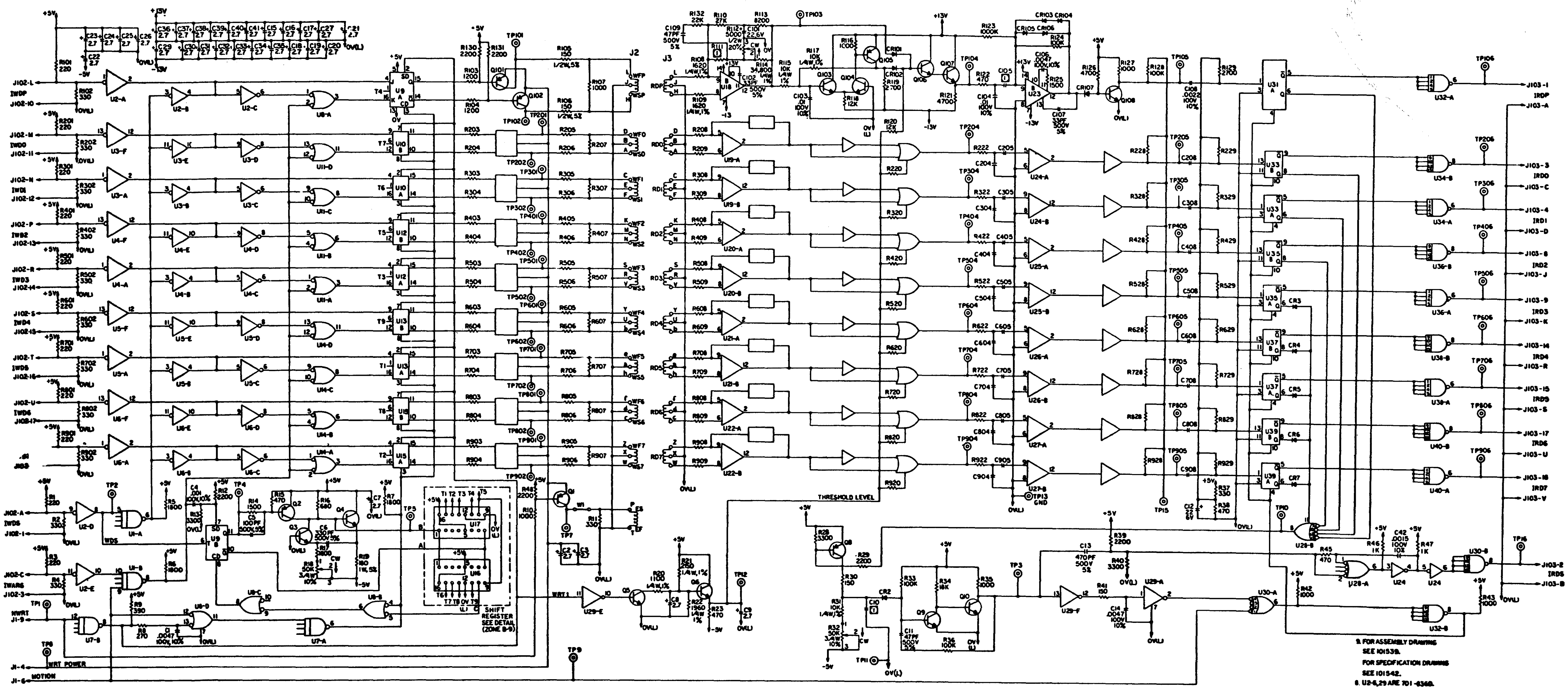
4. ALL DIODES ARE 300-4446.

3. ALL RESISTORS IN OHMS, 1/4W, 5%.

2. CIRCUIT 100 IS TYPICAL OF CIRCUIT 200 THRU 700.

1. 3 DIGIT REF NOS. ARE ASSIGNED TO REPETITIVE CIRCUITS. EX: TP101 IS CIRCUIT 100. TP 701 IS CIRCUIT 700. SINGLE DIGIT NOS. ARE ASSIGNED TO NON REPETITIVE CIRCUITS. EX: TP1-TP2.

NOTES: UNLESS OTHERWISE SPECIFIED:



VERSION TABLE

VERSION	SPEED(IPS)		C10	C105-905		R111-911 1/4, 1%
-01	9.1 THRU 12.5		.0068UF	.0068UF		178K

REFERENCE DESIGNATION

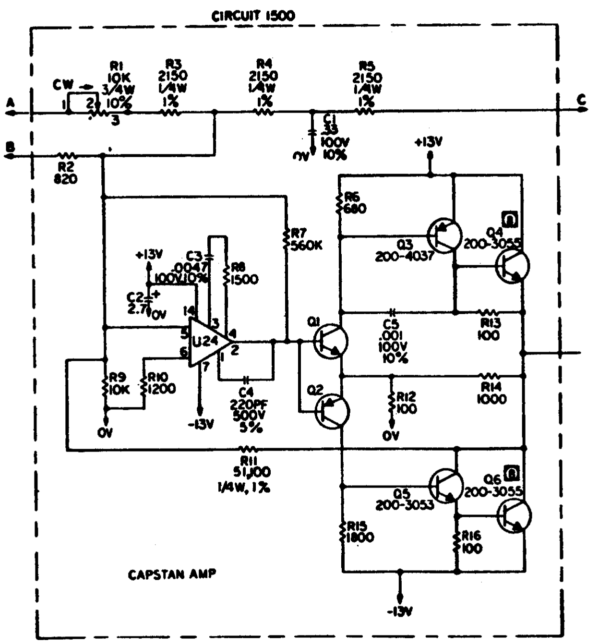
LAST USED		NOT USED
R132	R48	R44
C909	C42	C28
Q908	Q10	
CR907	CR7	CR1
TP906	TP16	
	U40	
	W1	

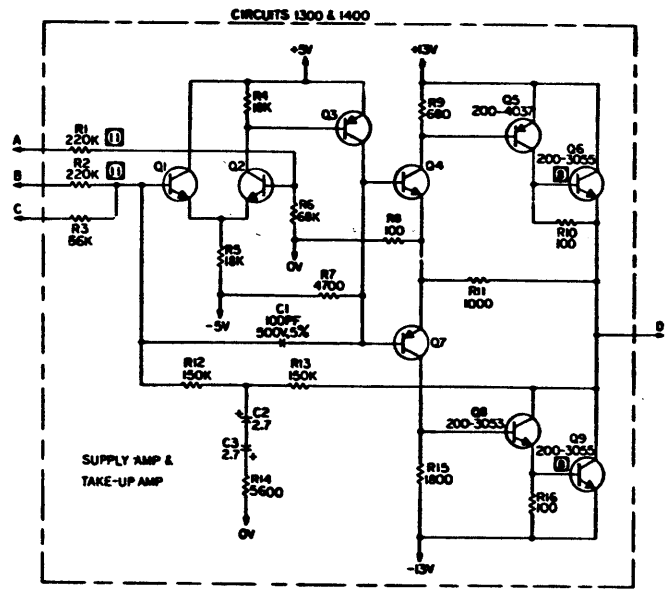
9. FOR ASSEMBLY DRAWING SEE 101539.
   FOR SPECIFICATION DRAWING SEE 101542.
8. U2-6,29 ARE 701-8360.
   U1,7,28,30,32,34,36,38,40 ARE 701-8440.
   U8,11,14, ARE 701-8460.
   U31,33,35,37,39 ARE 701-8530.
   U18-27 ARE 400-1437.
   U9,10,12,13,15 ARE 701-7476.
   U16,17 ARE 701-7496.
7. PIN 7 OF ALL IC'S IS 0V
   PIN 14 OF ALL IC'S IS +5V.
6. ALL NPN TRANSISTORS ARE 200-3946.
   ALL PNP TRANSISTORS ARE 200-3251.
5. ALL CAPACITORS IN MICROFARADS, 35V, 20%.
4. ALL DIODES ARE 300-4446.
3. ALL RESISTORS IN OHMS, 1/4 W, 5%.
2. CIRCUIT 100 IS TYPICAL OF CIRCUIT 200 THRU 900.
1. 3 DIGIT REF NOS. ARE ASSIGNED TO REPETITIVE CIRCUITS. EX: TP101 IS CIRCUIT 100. TP 901 IS CIRCUIT 900. SINGLE DIGIT NOS. ARE ASSIGNED TO NON. REPETITIVE CIRCUITS. EX: TP1-TP2.

① SEE VERSION TABLE FOR VALUE

NOTES: UNLESS OTHERWISE SPECIFIED:

Figure 7-14
Data C19 - Logic Schematic





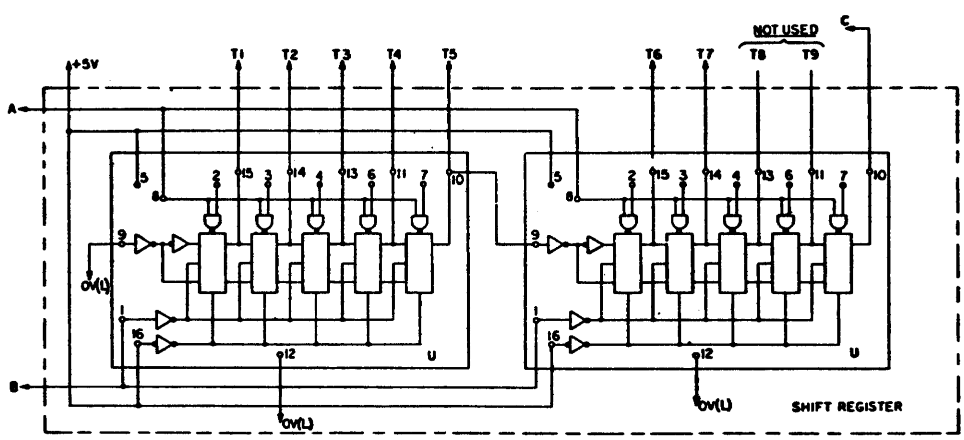


Figure 7-15
MISC. CIRCUITS