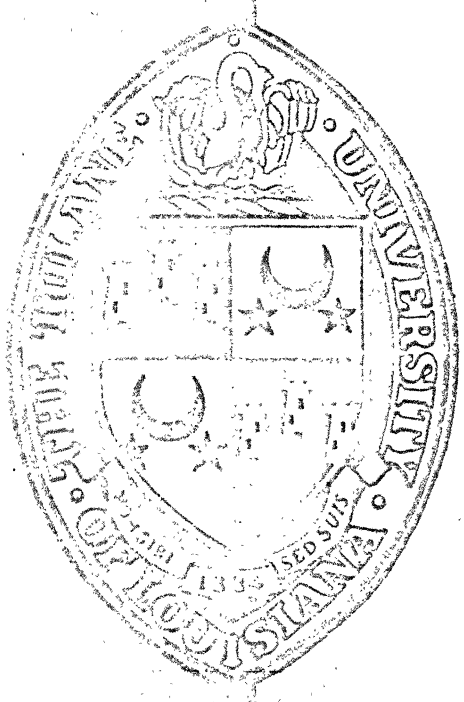
PROCEEDINGS
OF THE
SECOND MEETING
OF THE
MINUTEMAN COMPUTER
USERS GROUP

SYSTEMS LABORATORY REPORT NO. TSL-3-71



Tulane University

School of Engineering

Meeting held
November 16, 1970
UNIVERSITY OF HOUSTON
Houston, Texas

PROCEEDINGS*

OF THE

SECOND MEETING

of the

MINUTEMAN COMPUTER

USERS GROUP

Edited By

Charles H. Beck

Professor and Director

SYSTEMS LABORATORY

Department of Electrical Engineering

School of Engineering

TULANE UNIVERSITY

Systems Laboratory Report No. TSL-3-71

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PREFACE

The Minuteman Computer Users Group is composed of those who are involved with the use and development of the Minuteman D17B computers in many fields of research, education, and applications in the computer field. Those who are members of this cooperative, voluntary group assist each other by sharing results, programs, and applications.

The first meeting of the MCUG, held at the Disneyland Hotel in Annaheim, California on June 11-12, 1970, was attended by 65 persons. The second meeting, held November 16, 1970 on the campus of the University of Houston, was attended by 80 persons from 32 states, the District of Columbia, and Germany. The registration list is included in the appendix.

These *PROCEEDINGS* are a permanent record of the material presented at the meeting held on November 16, 1970. This material describes checkout and trouble-shooting procedures, hardware interface developments, applications, and programming related to the D17B computers. The agenda also included a demonstration of the input/output panel for the D17B computer located in the Electrical Engineering Department at the University of Houston. In addition to the technical sessions, there was considerable exchange of information during informal discussions at the breaks and at the luncheon.

The editor is grateful for research support relating to the D17B under *Air Force Office of Scientific Research*, *Army Medical Research & Development Command*, and the *NSF Office of Computing Activities*. We also thank our host, Dr. James D. Bargainer, Assoc. Professor of Electrical Engineering, University of Houston, and his colleagues for the warm hospitality and the time and effort required to plan for the local arrangements. The assistance and encouragement of Mr. James W. Neal of ONR and Mr. Richard F. Babler of DSA are gratefully acknowledged. Information provided by Autonetics has been especially helpful.

MCUG Executive Committee members who were present were the following:

Chairman - Dr. Charles H. Beck, Professor of Electrical Engineering, Tulane University

Hardware - Dr. James D. Bargainer, Associate Professor of Electrical Engineering, University of Houston
- Mr. Cedric B. Wernicke, Psychology Service, Brentwood VA Hospital, Los Angeles

Software - Mr. Donald E. Geister, Research Engineer, Aerospace Engineering, University of Michigan

Spare Parts and Maintenance - Mr. Charles M. Swanson, Instructor of Electronics, Mankato Area Voc-Tech Institute

The persons who attended the meeting represented 61 organizations with potential use of the D17B. Among these, 14 had D17B's (4 operational), 20 had submitted requisitions, and 17 were considering acquisition of a D17B.

Methods of joining the MCUG

1. Send a check for $100 to the address given below, made out to the MCUG.
2. Send a purchase order for $100 to the following address. This purchase order can specify documentation for checkout, trouble-shooting, operation, and programming of the Minuteman D17B computer.
3. Request invoice for $100 to cover documentation listed in item 2 above.

Dr. Charles H. Beck
Professor of Electrical Engineering
Tulane University
New Orleans, Louisiana 70118

These *PROCEEDINGS* of the *SECOND MEETING OF THE MINUTEMAN COMPUTER USERS GROUP* can be obtained at $15 per copy. Please make check or purchase order payable to the MCUG and mail to the chairman at the above address. Specify SYSTEMS LABORATORY Report No. TSL-3-71. MCUG members will receive one copy of these *PROCEEDINGS*, as well as other reports, a programming manual, and other documentation which will assist in the utilization of the D17B.

Charles H. Beck
Chairman, MCUG

MINUTEMAN COMPUTER USERS GROUP MEMBERSHIP

1. Arizona State University, Electrical Engineering
2. Arnold Research Organization, Arnold AFB, Tennessee
3. Auguatana College, Physics
4. Austin College, Computer Center
5. Bureau of Mines, Laramie, Wyoming
6. California Institute of Technology, Geology
7. Colorado State University, Atomspheric Science
8. Dillard University, Mathematics and Science
9. Indiana University of Pennsylvania, Physics
10. Louisiana State University Medical School, Neurology
11. Massachusetts General Hospital, Boston
12. McDonnell Douglas, St. Louis, Missouri
13. Milwaukee Area Technical College, Electronics
14. MIT, Draper Laboratory
15. Naval Ordnance Station, Indian Head, Maryland
16. Oklahoma State University, Physics
17. Pennsylvania State University, Chemistry
18. Princeton University, Psychology
19. Raytheon Corp., Bristol, Tennessee
20. Southwest Minnesota State College, Electronics
21. Tektronix, Inc., Beaverton, Oregon
22. Tulane University, Electrical Engineering
23. University of Colorado, Electrical Engineering
24. University of Delaware, Electrical Engineering
25. University of Houston, Electrical Engineering
26. University of Oklahoma, Mathematics
27. University of South Florida, Physics
28. University of Texas, Applied Research Laboratory
29. University of Washington, Electrical Engineering
30. University of Wyoming, Electrical Engineering
31. Wright State University, Computer Center

TABLE OF CONTENTS

RECOMMENDED CHECKOUT AND TROUBLE-SHOOTING PROCEDURES FOR THE D17B COMPUTER

C. H. Beck
Tulane University

As a result of the current modernization of the Minuteman ICBM force, a quantity of Inertial Guidance Systems (Model NS-10Q), each costing $234,000, have been declared excess by the USAF. Since over 1,000 of these advanced computer systems from the LGM 30/Minuteman Missiles are scheduled to be declared excess, success of this reutilization project can effect a savings of nearly a quarter of a billion dollars.

NS-10Q systems contain a D17B computer, the associated stable platform, and power supplies. Detailed specifications for the D17B computer are given in Table 1. It is a small, extremely versatile, multipurpose, serial-binary computer.[1] The high degree of reliability and ruggedness of the computer are evidenced by the strict requirements of the weapons system.

Mr. Ray E. Close, System Manager, LGM 30 Systems Management Division, Hill AFB, stated at the first Minuteman Computer Users Group meeting in Anaheim, California on June 12, 1970, that the average MTBF for the over 1,000 D17B's had exceeded 5.5 years. During the time that the D17B has been operating in the Systems Laboratory at Tulane University, a few failures have occurred. These failures were created by occasional inadvertant, improper procedures when measurements were being taken under difficult circumstances. For normal laboratory operating conditions, the D17B can be powered up and shut down frequently without experiencing malfunctions, as has been the case during the past 15 months of extensive operation in the Systems Laboratory.

Thus, the reliability of the D17B will hopefully reduce the occurrence of equipment breakdowns, the need for technical maintenance personnel, and the

MANUFACTURER: Autonetics, a Division of North American Rockwell, Inc.
MODEL: D17B
YEAR: 1962
TYPE: Serial, synchronous
NUMBER SYSTEM: Binary, fixed point, 2's complement
LOGIC LEVELS: 0 or False, 0V; 1 or True, -10V
DATA WORD LENGTH (bits): 11 or 24 (double precision)
INSTRUCTION WORD LENGTH (bits): 24
MAXIMUM I/O (words/s): 25,600
NUMBER OF INSTRUCTIONS: 39 types from a 4-bit op code by using five bits of the operand address field for instructions which do not access memory
EXECUTION TIMES:
Add (us): 78 1/8
Multiply (us): 546 7/8 or 1,015 5/8 (double precision)
Divide: (software)
(Note: Parallel processing such as two simultaneous single precision operations is permitted without additional execution time.)
CLOCK CHANNEL: 345.6 kHz
ADDRESSING:
Direct addressing of entire memory
Two-address (unflagged) and three-address (flagged) instructions
MEMORY:
Word Length (bits): 24 plus 3 timing
Type: Ferrous-oxide-coated NDRO disk
Cycle Time (us): 78 1/8 (minimal)
Capacity (words): 5,454 or 2,727 (double precision)
INPUT/OUTPUT:
Input Lines: 48 digital
Output Lines: 28 digital
12 analog
3 pulse
Program: 800 5-bit char/s
PHYSICAL CHARACTERISTICS:
Dimensions: 20" high, 29" diam.
Power: 28V dc at 25A
Circuits: DRL and DTL
Double copper clad, gold plated, glass fiber laminate, flexible polyurethane coated circuit boards
SOFTWARE:
Minimal delay coding using machine language
Modular special-purpose subroutines
RELIABILITY: 5.5 years MTBF

Table 1. Minuteman D17B computer specifications.

associated maintenance costs once the system is in operation. This is partly because of the use of high reliability components. Also, since the D17B is available to authorized government agencies and contractors for use on contracts or grants on a non-reimbursable basis, there will be insignificant cost increase with usage. And, with the assistance of the MCUG, it is expected that many users will take over complete system responsibility including maintenance. It is expected that less-skilled technicians can be trained to provide the necessary service. The very high MTBF of the D17B should be considered when planning a computer system which should not be interrupted.

The following items should be considered in planning for a D17B system.

1. Shipping for the D17B and I/O devices, available through DSA.
2. Interfaces for connecting peripheral I/O devices to the D17B.*
3. 28V dc power supply rated at 19A (25A surge).
4. Air duct and blower.
5. Operator control panel.*
6. Engineering effort and labor for installation and checkout of the D17B.*
7. Software development, trouble-shooting, and maintenance.*

It is estimated that four man-days are required for preparing the D17B for operation and interfacing it to a Flexowriter. An additional two man-days will be sufficient for checkout of a manual control panel and Flexowriter I/O. Considerable efficiency is possible since a single system design will suffice for the application of several D17B's to similar tasks. The MCUG can assist in this regard. Despite the difficulties of limited documentation during the early phases of this project and the associated frustration, the D17B is now performing useful functions in the Systems Laboratory at minimal cost.

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*Available through the Minuteman Computer Users Group.

PHYSICAL CHARACTERISTICS

The NS-10Q was located just beneath the payload in the nose cone of the Minuteman I Missile. The D17B computer portion, built by Autonetics, a division of North American Rockwell, occupies 180° of the chassis structure of the NS-10Q as shown in Figure 1. The power supply section occupies the other half of the chassis structure toroid. The outer body skin, which provides the NS-10Q the capability of becoming an integral part of the missile frame, may be unbolted and removed when the NS-10Q is to be used for other purposes. Removal of this body section will have no effect on the operation of the D17B.

The D17B is 20 in high, 5 in deep, has a 29 in diameter, and weighs approximately 62 lbs. Components include approximately 1521 transistors, 6282 diodes, 1116 capacitors, and 5094 resistors. These components are mounted on 75 circuit boards of double-copper-clad, engraved, gold-plated, glass-fiber laminate. They have been coated with polyurethane.

The design of the D17B placed a premium on reliability since there is no second chance when an airborne computer controlled mission is executed.[2] Hence, DRL logic was used extensively rather than DTL except where gain was required. Extensive use was made of silicon and mesa-germanium semiconductor devices in this fully solid-state computer. A logic level of 1 or True is represented by approximately -10V, and a 0 or False by approximately 0V.

Power Supply

A 28V dc regulated power supply capable of supplying a 25A starting surge must be provided for operation of the computer. Other required voltages are obtained internally by converting the 28V dc into secondary power using solid-state D17B circuitry. The current drawn from the 28V dc supply will vary from 0 to 25A with a steady-state value of approximately 19A referred to as full load. The positive terminal of the 28V dc supply should be connected to

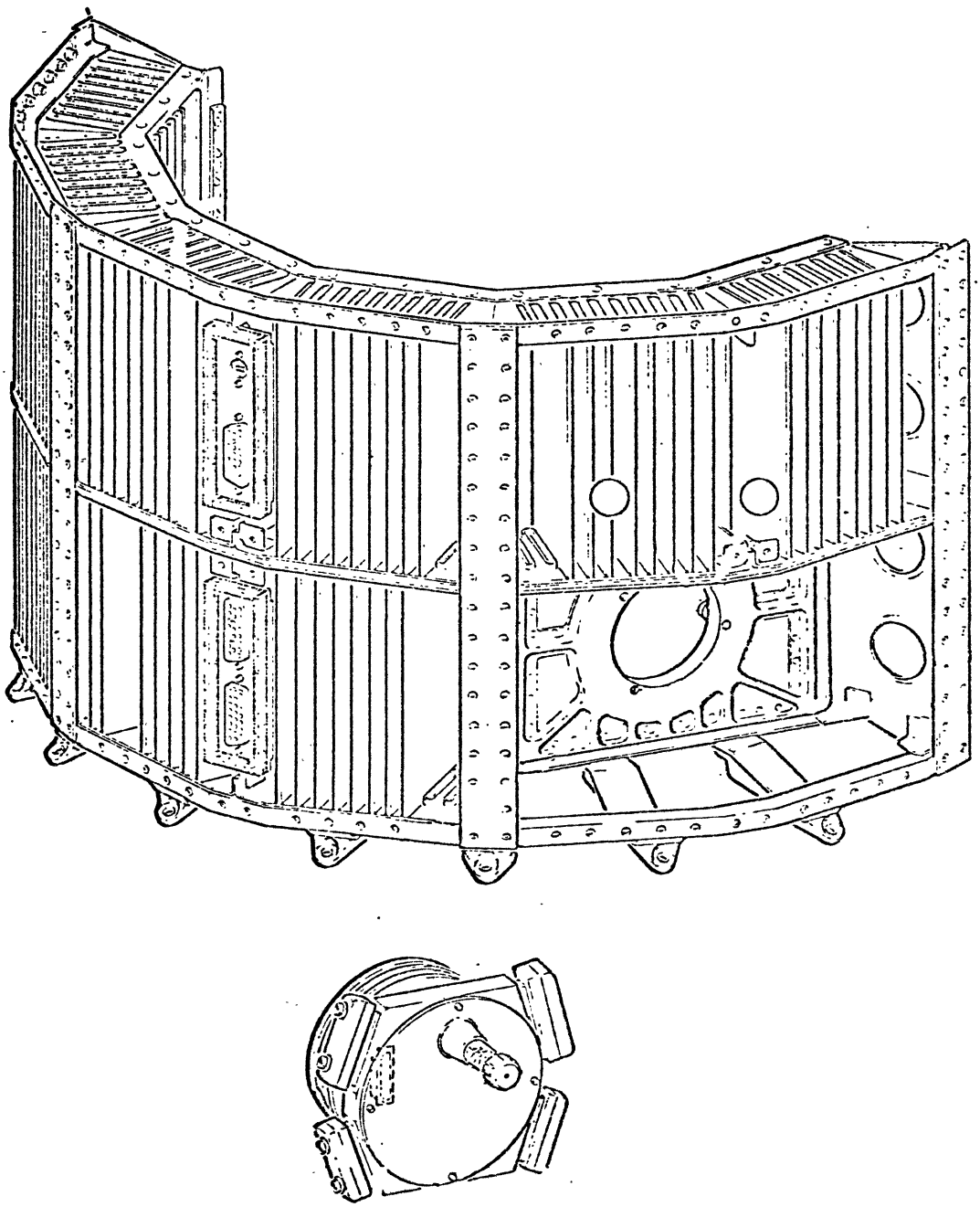


Figure 1. Minuteman D17B computer sketch.

terminal E2 on the base structure, and the ground terminal should be connected to E3. The secondary power requirements include 400Hz, 3ϕ, and various dc voltages as shown in Figure 2.

Power can be applied for a short time to determine that the memory motor is operational or that a secondary power supply is functioning. The 28V, 400 Hz, 3ϕ can be checked on TB6 - 1, 2, 3 which is the connection to the fan located on top of the D17B. If this fan has been removed, the lead will be easily accessible.

The secondary dc power supplies can be monitored most conveniently at the checkout connector, J2, on the terminals listed in Table 2.

Location	Voltage	Location	Voltage
J2- 3	~~+28V dc~~ 2 vdc	J2-19	+35
- 9	+15	-20	-10
-13	- 1	-21	-28
-14	-25	-22	+ 6
-16	+10	-23	-35
-17	+25	-24	- 5
-18	- 3		

Table 2. Tabulation of secondary power supply monitoring locations.

Cooling

Continuous operation requires that air be passed through the D17B to maintain an ambient temperature of 77°F $\pm$ 9°F (25°C to $\pm$ 5°C). A D17B has been operating in the Systems Laboratory for over 1,000 hours using a blower to circulate room air to effect cooling.

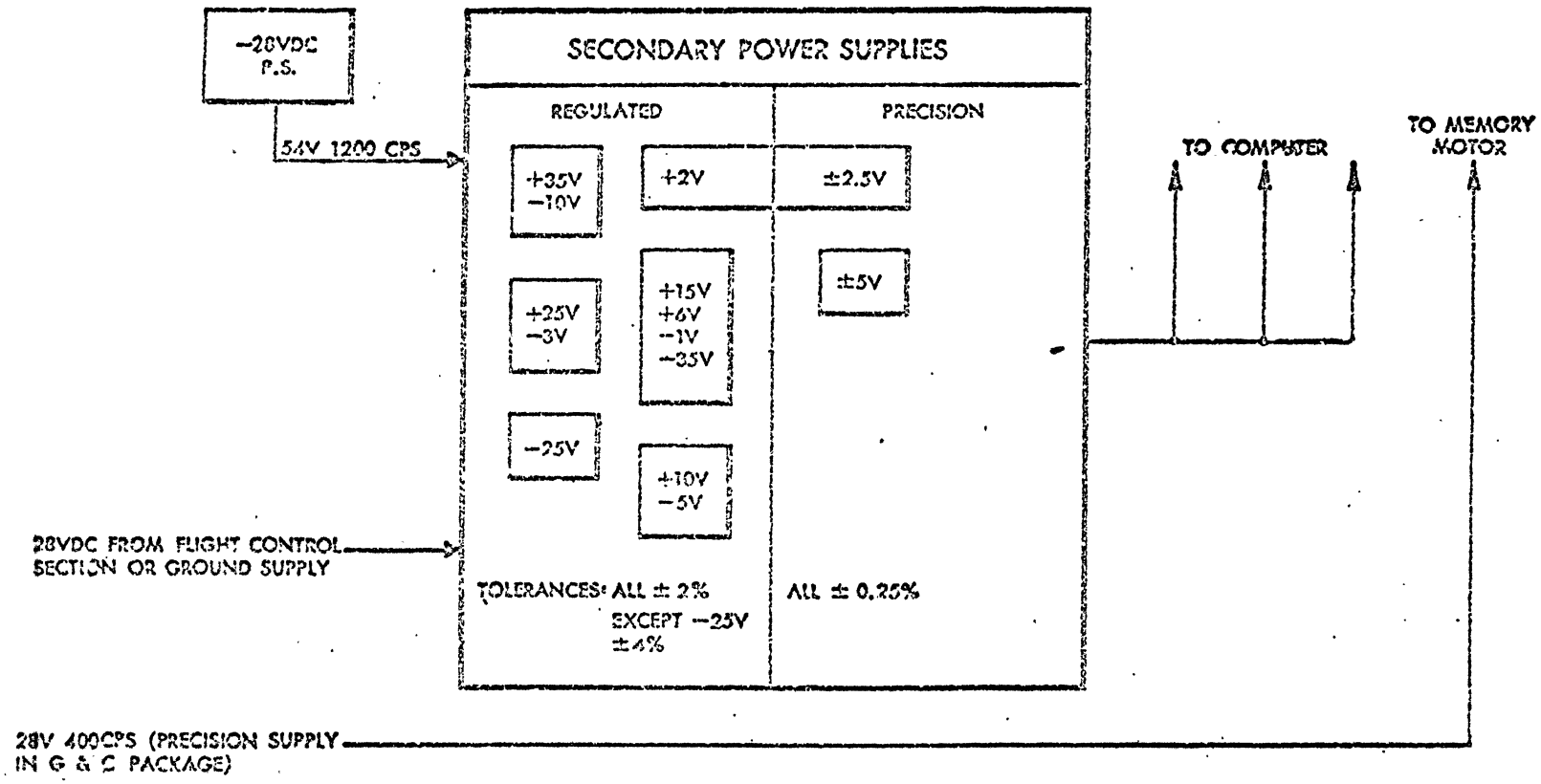


Figure 2. D17B power supplies.

Input Connections

Most of the connections for control signals, instruction and data character inputs, and character outputs and for some of the external discrete inputs are available on the 100-pin umbilical connector which was mounted in the outer body skin. These connections, listed in Table 3, can easily be disconnected and attached to a patch panel.

FUNCTIONAL CHARACTERISTICS[3,4]

The D17B was designed primarily to solve real-time inertial guidance and flight control problems associated with the Minuteman I missile. It has the following general capabilities:

1. Sampling and processing of input data in the form of control signals, digital data, or pulse-type signals.
2. Logical decision-making and performance of arithmetic operations using an instruction repertoire containing the 39 types of machine language instructions listed in Table 4.
3. Transmission of output data in the form of analog, digital, and pulse-type signals under program control.

The characteristics of the D17B which will be of specific interest in checkout will be described. The breakdown of these characteristics along functional subdivisions as identified in Figure 3 is not intended to infer that these elements exist as separate physical entities.[5]

Central Processing Unit

Since the D17B is a serial-binary computer, simultaneous access to all the bits of a memory location is not needed either for instructions or data. Hence, the arithmetic registers need not be constructed entirely of flip-flops. Instead, they are in the form of circulating loops in memory as illustrated in Figure 4. The D17B has four double-rank arithmetic registers

Pin	Function	
1	I1C	Character Input
2	I2C	
3	I3C	
4	I4C	
5	Parity	
6	Timing Prime TC'	
7	Precision Time Pulse	
9	SC10	Character Output
10	SC20	
11	SC30	
12	SC40	
14	Parity Bit	
15	Timing	
13	Parity or Verify Error, PVEC	
23	Disable Discrete, DDC	
90	Master Reset, MRC	
91	Halt Prime, KHC'	
93	Enable Write, EWC	
96	X1C	Discrete Inputs
97	X2C	
98	X3C	
99	X4C	
95	V5C	
94	V6C	

Table 3. Tabulation of selected functions accessible through the umbilical connector.

Numeric Code	Code	Description
00 20, s	SAL	Split accumulator left shift
00 22, s	ALS	Accumulator left shift
00 24, 2	SLL	Split left word left shift
00 26, s	SLR	Split left word right shift
00 30, s	SAR	Split accumulator right shift
00 32, s	ARS	Accumulator right shift
00 34, s	SRL	Split right word left shift
00 36, s	SRR	Split right word right shift
00 60, s	COA	Character output A
04 c, s	SCL	Split Compare and limit
10 c, s	TMI	Transfer on minus
20 c, s	SMP	Split multiply
24 c, s	MPY	Multiply
30 c, s	SMM	Split multiply modified
34 c, s	MPM	Multiply modified
40 02, s	BOC	Binary output C
40 10, s	BOA	Binary output A
40 12, s	BOB	Binary output B
40 20, s	RSD	Reset detector
40 22, s	HPR	Halt and Proceed
40 26, s	DOA	Discrete output A
40 30, s	VOA	Voltage output A
40 32, s	VOB	Voltage output B
40 34, s	VOC	Voltage output C
40 40, s	ANA	And to accumulator
40 44, s	MIM	Minus magnitude
40 46, s	COM	Complement
40 50, s	DIB	Discrete input B
40 52, s	DIA	Discrete input A
40 60, s	HFC	Halt fine countdown
40 7-, s	LPR	Load phase register
44 c, s	CLA	Clear and Add
50 c, s	TRA	Transfer
54 c, s	STO	Store accumulator
60 c, s	SAD	Split add
64 c, s	ADD	Add
70 c, s	SSU	Split subtract
74 c, s	SUB	Subtract

Table 4. D17B instruction repertoire.

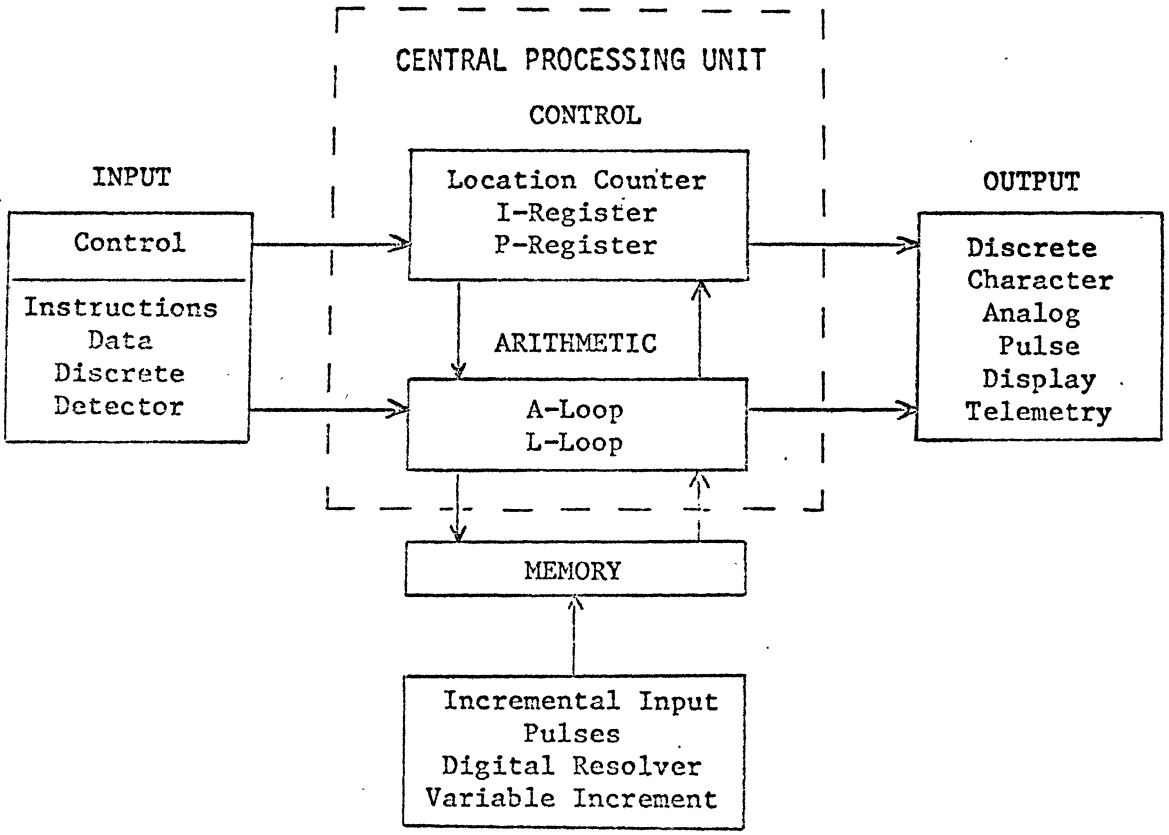


Figure 3. MINUTEMAN D17B computer functional block diagram (conceptual)

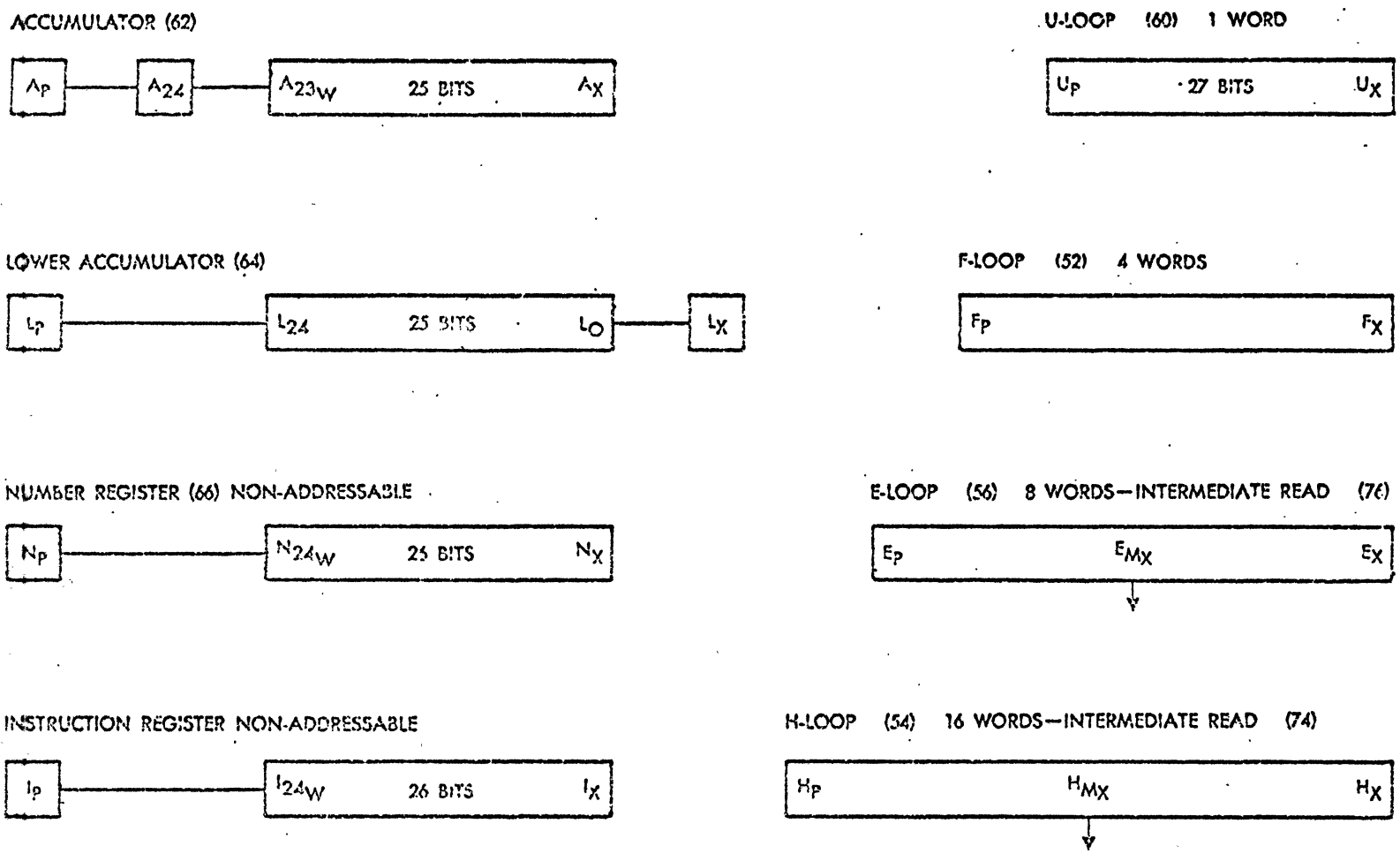


Figure 4. Arithmetic registers and rapid-access memory loops.

which are the accumulator (A), lower accumulator (L), instruction register (I), and number register (N). Because (L) is addressable, it can be used as rapid-access storage in addition to performing normal arithmetic functions. There are two additional non-addressable registers, which are used without programmer control, and one 3-bit pseudo-index (phase) register. The functional locations of these registers and loops are illustrated in Figure 5.

The central processing unit (CPU) has I/O access to four rapid-access memory loops of 1, 4, 8, and 16 words in addition to the main memory which is arranged in 21 channels of 128 words each. Two input buffer loops of 4 words each provide additional input capability from memory.

Programmed data channels cause data transfers into the arithmetic registers. All machine functions are processed and interpreted in the CPU. The memory channel address from which the next instruction is to be taken is determined by the location counter. When the CPU is ready to accept another instruction from memory, the address is specified by the channel address stored in the location counter and the sector address specified in the previous instruction.

The index register can modify the operand channel address of one of the multiply instructions. This register also serves as a selector switch for choosing one of two pairs of inputs to one of the incremental pulse-type input loops and for selecting one of four external positions for each of the three D-A analog voltage outputs.

The accumulator holds the results of all arithmetic operations and serves as an output register for parallel digital data, pulse-type signals, D-A analog voltage outputs, and telemetry data. The lower accumulator is involved in certain arithmetic, input, and logical operations. A real-time clock is provided by internal timing signals derived from the clock channel of the disk memory.[6]

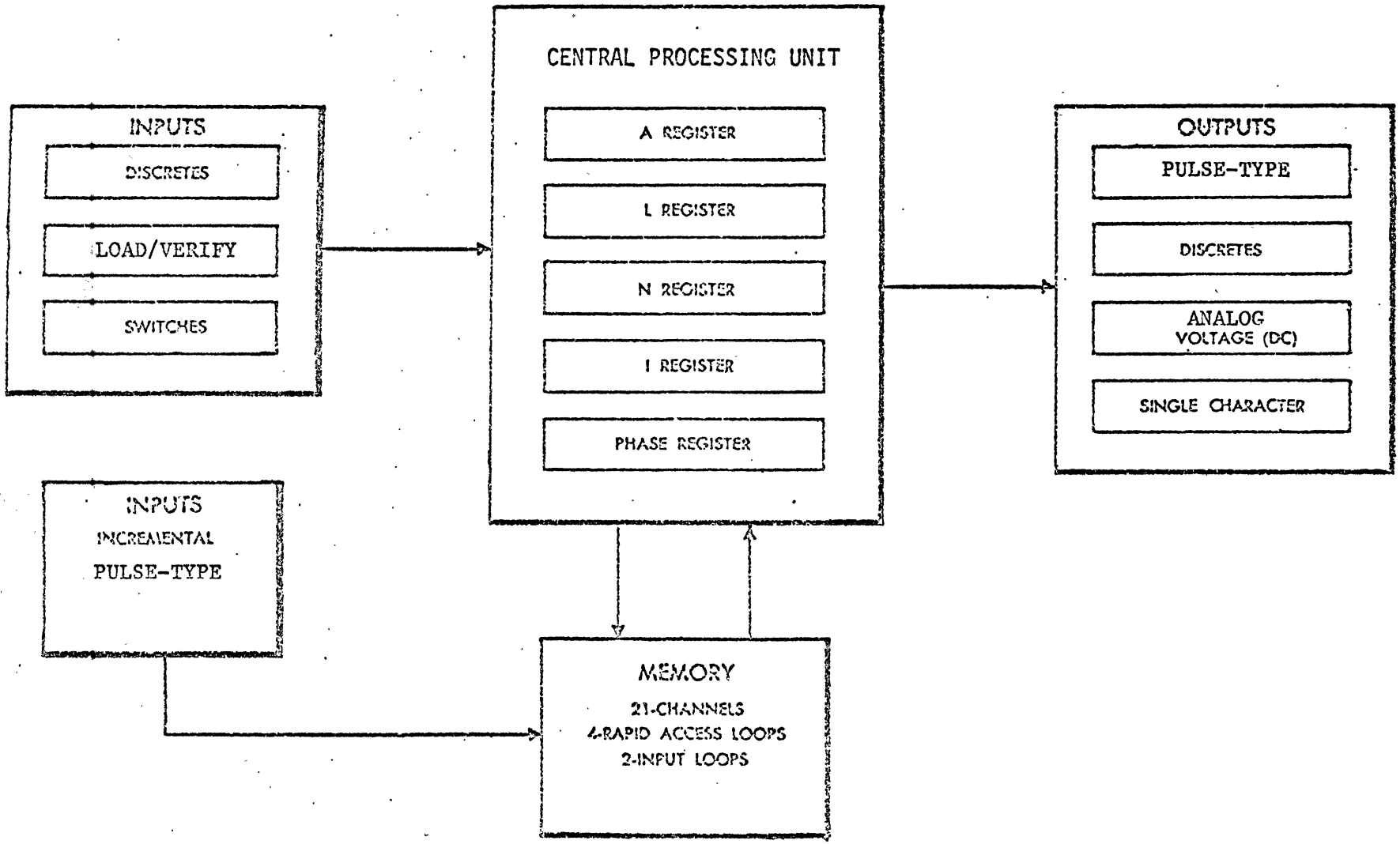


Figure 5. Functional location of arithmetic registers and rapid-access memory loops.

Memory[7]

The delay-type memory is a 6,000 r/min, ferrous-oxide-coated disk as illustrated in Figure 6. The disk is driven by a 400 Hz, 3 ϕ hysteresis-synchronous motor. Non-return-to-zero recording is used. The addressable memory capacity is 5,454 11-bit (single-precision) or 2,727 24-bit (double-precision) words. The format of these words is shown in Figure 7. Main memory is arranged in 21 channel of 128 double-precision words each. These channels are numbered in even octal from 00 to 50.

Main memory channels are non-volatile in the event of a power failure or if the system is shut down. The clock channel contains a permanently recorded 345.6 kHz sinusoidal signal. Sector information is also permanently recorded on another channel. The total non-destructive readout memory is designed to be completely programmable in conjunction with ground support equipment.

The addressable memory also includes rapid-access loops of 1, 4, 8, and 16 words, two arithmetic registers, and two 4-word input buffer loops for direct data entry. There are two additional non-addressable arithmetic registers. These rapid-access loops and registers are actually reserved memory locations as illustrated in Figure 8.

The memory cycle time is 78 1/8 μs if the memory location is coincident with a read head. This is the time required to read one 24-bit serial word and is defined as one word time. The cycle time for the 1-word registers is one word time. The worst-case cycle times for the 4, 8, and 16-word loops are 4, 4, and 8 word times respectively. The worst-case cycle time for the main memory channels is 128 word times.

Program security or memory protect can be maintained by disabling the write heads to a portion of the memory to effect read-only memory. By enabling these write heads it is possible to perform instruction and address modification under program control.[8]

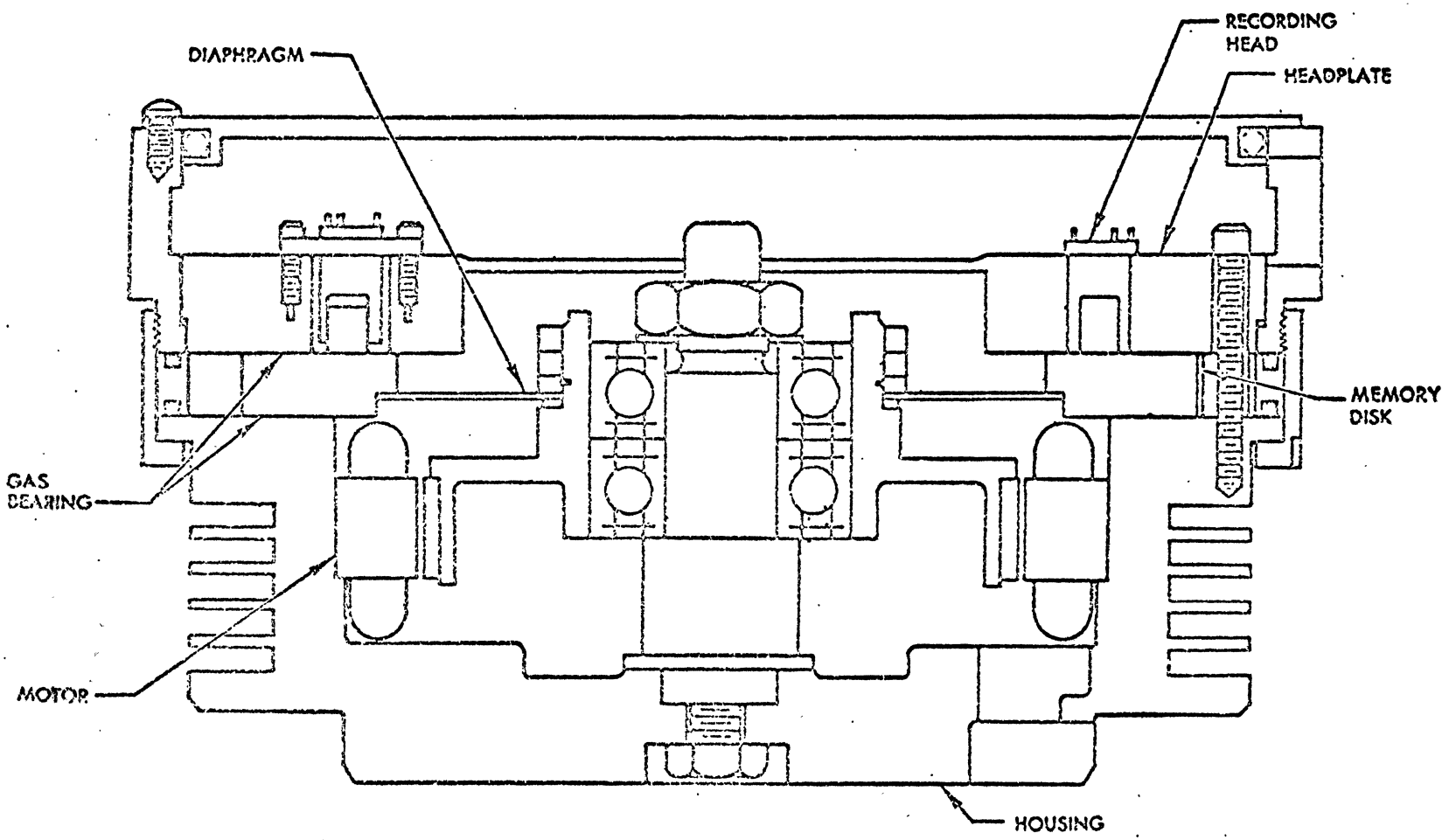
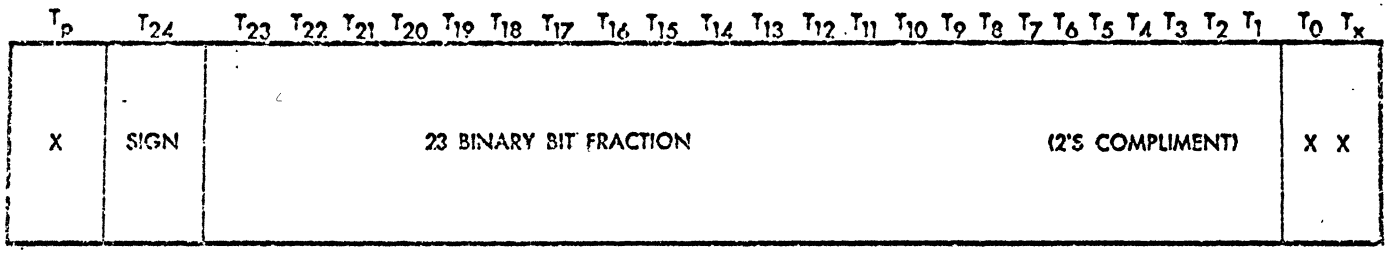


Figure 6. Sectional view of the disk-type memory unit.

WHOLE NUMBER



SPLIT NUMBER

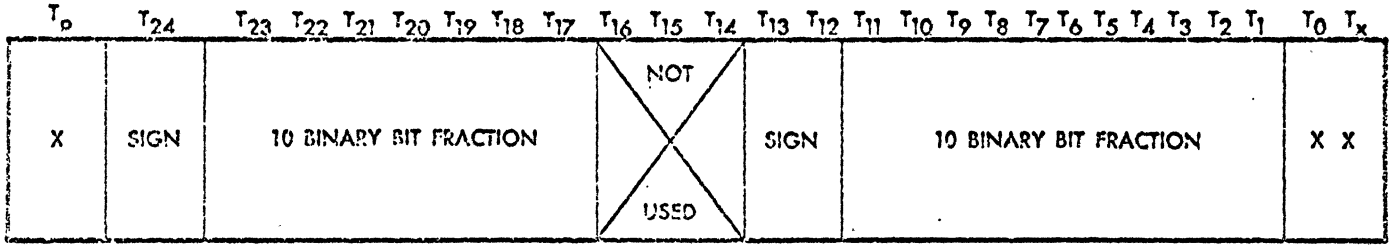


Figure 7. D17B data word format.

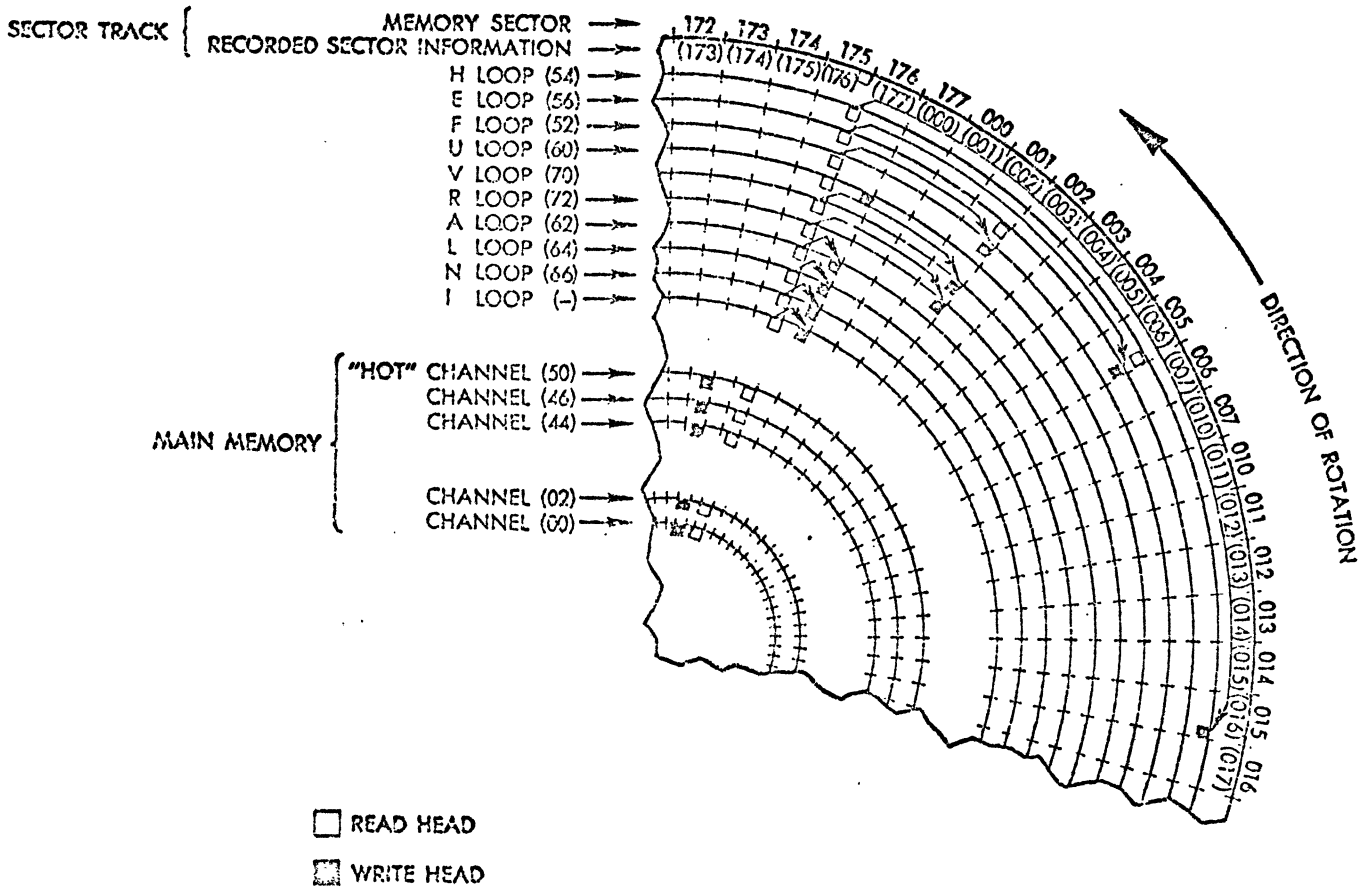


Figure 8. Conceptual diagram of the arrangement of memory loops and registers.

Input/Output[9,10]

The program, composed of instruction and data words, is initially punched on cards or paper tape as illustrated in Figure 9, or is recorded on magnetic tape. This program is then entered into memory. Specific console initializing and interactive inputs must be supplied under operator manual control using push buttons and switches to cause logical synchronization, conditioning of logic circuitry, and sequential state transitions between submodes of computer operation. The console control inputs initially cause the D17B to enter the load/verify mode to prepare for entering the program. These console control inputs and the voltage used in the Systems Laboratory are listed in Table 5.

Instruction and data characters can be read in during the load/verify mode; sequential memory locations are assumed unless a location control character is present. The maximum rate of loading into or comparing with the contents of memory is 100 words/s. This is equivalent to 800 characters/s since each 24-bit word is composed of eight octal characters, as illustrated in Figure 10. Negative data must be represented in two's complement form. Control characters read in during the load/verify mode condition logic circuitry to effect appropriate computer operation.

Additional data represented by 48 discrete lines can be entered under program control. One of these discrete lines monitors the detector flip-flop, DR, which can be set by an external source; setting DR produces a logic signal that indicates the status of external equipment. This function serves as a hardware interrupt. If DR is set, certain discrete outputs are inhibited. DR can be reset under program control.

Incremental inputs of +1, -1, and 0 can be added to the respective contents of eight memory locations in input loops through direct data entry. These inputs are independent of program control. This capability provides for direct

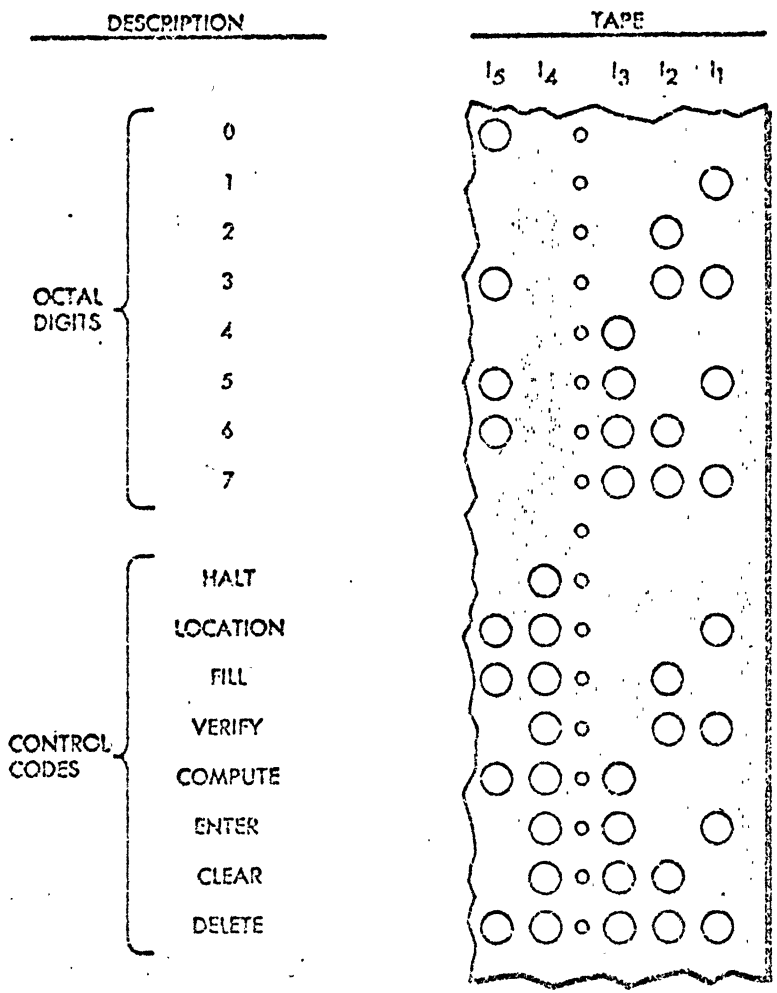


Figure 9. D17B control and octal character codes.

FUNCTION	SYMBOL	POSITION	VOLTAGE	CONNECTION
Character Input	I1C-I5C	1	-10V	J1-1 to J1-5, TB1B-17 to TB1B-21, or (J7-1 to J7-5)
		0	Floating	
Disable Discrete	DDC	1	+25V	J1-23, P2-12, P2-5, TB1B-30, J3-17, J7-14, or J10-33
		0	Floating	
Enable Write	EWC	1	+25V	J1-92, P2-11, P2-6, TB1B-32, or (J7-16)
		0	Floating	
Fill Mode	FSC	1	-10V	(J8-24)
		0	Floating	
Halt Prime	KHC'	RUN	-10V	J1-91, TB1B-33, or (J7-17)
		HALT	Floating	
Master Reset	MRC	1	-10V	J1-90, P2-22, P2-15, TB1B-31, or (J7-15)
		0	Floating	
Run Prime	KRC'	HALT	-10V	(J8-16)
		RUN	Floating	
Single Prime	KSC'	1	+25V	(J8-15)
		0	Floating	
Timing	TC	1	0V	(J8-38)
		0	+25V	
Timing Prime	TC'	1	+25V	J1-6, TB1B-22, or (J7-6)
		0	0V	

Table 5. List of voltages and connections for the Tulane D17B manual control panel.

SIGN	WHOLE NUMBER																						
T_{24}	T_{23}	T_{22}	T_{21}	T_{20}	T_{19}	T_{18}	T_{17}	T_{16}	T_{15}	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	T_7	T_6	T_5	T_4	T_3	T_2	T_1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7			7			7			7			7			7			7			7		

SIGN	10 BIT BINARY FRACTION										X	X	SIGN	10 BIT BINARY FRACTION									
T_{24}	T_{23}	T_{22}	T_{21}	T_{20}	T_{19}	T_{18}	T_{17}	T_{16}	T_{15}	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	T_7	T_6	T_5	T_4	T_3	T_2	T_1
1	1	1	1	1	1	1	1	1	1	1	X	X	1	1	1	1	1	1	1	1	1	1	1
7			7			7			6			3			7			7			7		

Figure 10. D17B data word coding.

digital integration of eight functions--five of 11-bits each, two of 24-bits each, and one of 48-bits. Variable-increment inputs can also be added to the respective contents of memory locations in input loops through direct data entry. These inputs enter the computer on two sets of three lines. One line indicates the sign, and the other two mutually-exclusive input lines indicate increments of one or four. The state of the phase register determines which of the two pairs of inputs is selected. A pulse-type input can be added to the contents of a specific memory location at the maximum rate of 1000 pulses/s.

The variety of output transfers available from the D17B under program control include 3-bit, 4-bit, or 8-bit parallel data channels, discrete logic signals, pulse-type signals, 24-bit serial words, and analog signals. Parity or verify error outputs are also provided as hardware-controlled features. Specific discrete logic signals are disabled by a hardware interrupt if DR is ON.

With these output features, the D17B can output data to an automatic typewriter, light indicators, audible alarms, and other off-on devices. An array of light indicators can be used to display data in various coded forms. Continuous analog output signals can be monitored on a meter, or a permanent and continuous record can be preserved by using a strip chart recorder. Other peripheral devices can be used to prepare punched cards, punched paper tape, or magnetic tape for subsequent data entry into the D17B or another computer for later processing off-line.[11]

The location of jacks involved in the functional checkout and trouble-shooting of the D17B are illustrated in Figure 11. All flip-flop monitoring locations are listed in Table 6.

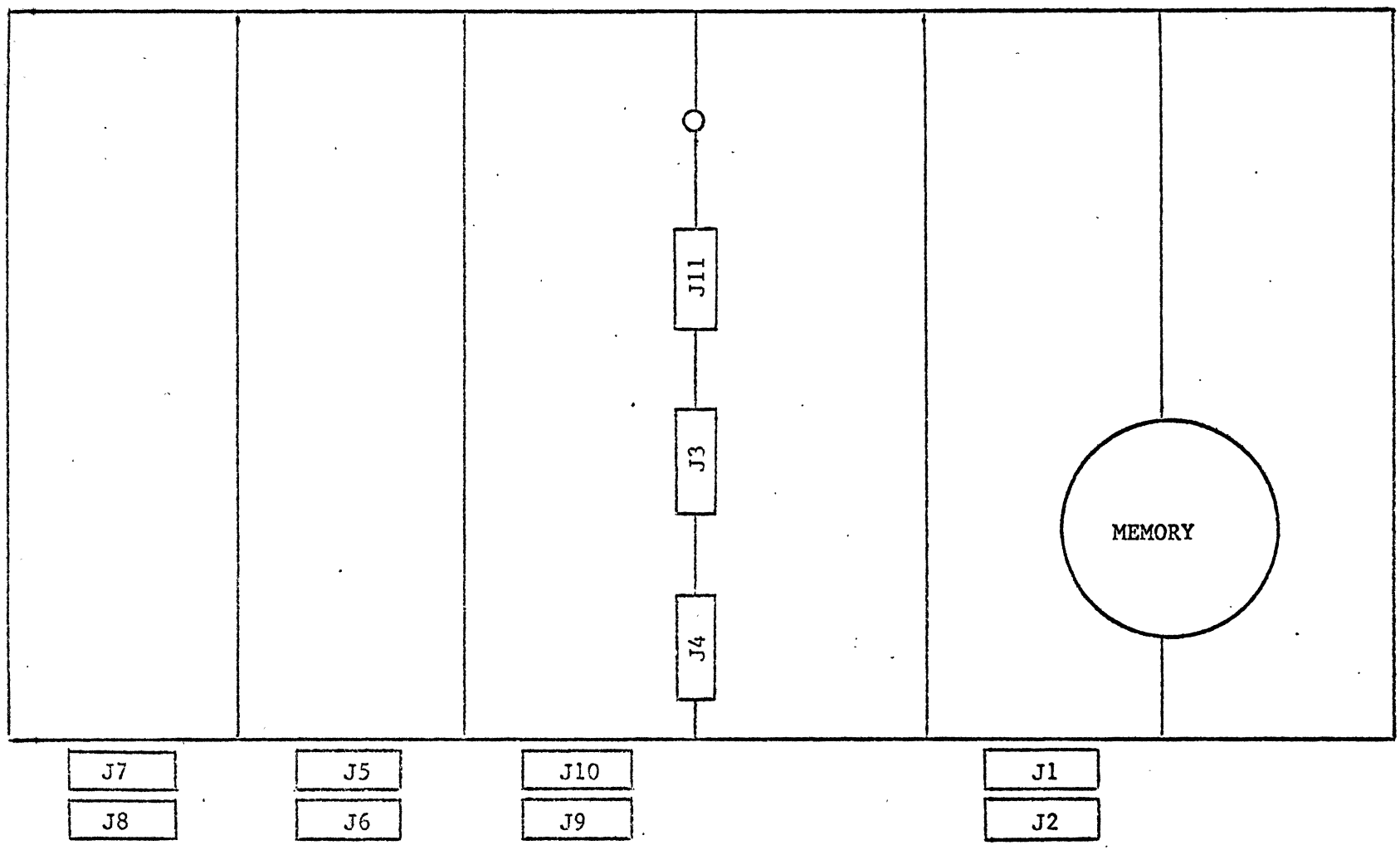


Figure 11. Location of I/O jacks on the D17B.

FUNCTION	LOCATION	FUNCTION	LOCATION	FUNCTION	LOCATION	FUNCTION	LOCATION
AC	J3-23	DR	J4-17	OB3	J4-31	V13	J11-11
AK	-45	D1	11- 1	O1	-11	V14	-12
AP	-41	D2	- 2	-2	-12	V15	-13
A24	-44	D3	- 3	-3	-13	V16	-14
B1	- 1	D4	- 4	O4	-14	V17	-16
B2	- 2	D5	- 5	P1	-34	V18	-17
B3	- 3	E	3-38	P2	-35	V21	-18
B4	- 4	FC	3-34	P3	-36	V22	-19
B5	- 5	G1	11- 6	Q	3-39	V23	-20
B6	- 6	G2	- 7	RC	-36	V24	-21
CB1	4- 1	G3	- 8	RK	-37	V25	-22
CB2	- 2	HS	3-16	RS	-38	V26	-23
CB3	- 3	IC	-24	RT	-39	V27	-24
CB4	- 4	ID	4-33	SB1	4-26	V28	-25
CB5	- 5	IP	3-42	SB2	-27	V31	-26
CP1	-18	J	-13	SB3	-28	V32	-27
CP2	-19	JT	4-46	S1	-23	V33	-28
CP3	-20	K	3-14	S2	-24	V34	-29
CP4	-21	LC	-25	S3	-25	V35	-30
CP5	-22	CP	-43	TO	3-50	V36	-31
C1	- 6	LX	-21	TP	-48	V37	-32
C2	- 7	MPX	-46	TX	-49	V38	-33
C3	- 8	Nc	-22	VC	-35	WA	4-42
C4	- 9	ND	4-32	VK	4-40	WB	-43
C5	-10	DP	3-40	VS	-41	Z1	-44
D	3-37	OB1	4-29	V11	11- 9	Z2	-45
DC	4-47	OB2	-30	V12	-10		

Table 6 . Tabulation of flip-flop monitoring locations.

REFERENCES

1. G. Lapidus, "A look at minicomputer applications," Control Engineering, pp. 82-91, November 1969.

2. R. L. Hooper and L. D. Amdahl, "Trends in aerospace computers," Datamation, vol. 13, pp. 22-26, November 1967.

3. D. O. Baechler, "State of the art of aerospace digital computers, 1962-1967," Computer Group News, vol. 2, pp. 1-12, January 1968.

4. A. S. Buchman, "Aerospace computers," Advances in Computers, vol. 9, pp. 239-284, 1968.

5. A. Epstein and D. Bessel, "Minicomputers are made of this," Computer Decisions, pp. 10-22, August 1970.

6. D. J. Theis and L. C. Hobbs, "Mini-computers for real-time applications," Datamation, vol. 15, pp. 39-61, March 1969.

7. R. T. Ollivier, "A technique for selecting small computers," Datamation, vol. 16, pp. 141-145, January 1970.

8. R. L. Hooper, "The minicomputer, a programming challenge," Proc. AFIPS 1968 FJCC, part 1, pp. 649-654, 1968.

9. R. Rinder, "The input/output architecture of minicomputers," Datamation, vol. 16, 119-124, May 1970.

10. W. H. Roberts, "Minicomputer architecture," IEEE Computer Group News, vol. 3, pp. 5-9, July/August 1970.

11. F. Gruenberger, "Are small free-standing computers here to stay?" Datamation, vol 12, pp. 67-68, April 1966.

HARDWARE INTERFACE DEVELOPMENTS FOR THE D17B COMPUTER

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The hardware interfaces that have been developed by the Systems Laboratory consist of the I/O interfaces required to connect the D17B to an electric typewriter and a paper tape reader/punch. Table 1 lists the D17B code for octal and control characters. The peripheral device currently being used is a Friden Flexowriter. This device is commonly available as government excess ADP equipment. Figure 1 is a schematic of the interconnections between the Flexowriter and the D17B. Interface design requires electronic and functional considerations. Table 2 lists the Flexowriter code modifications.

Figure 2 is a block diagram of the electronic circuits required for conditioning the input signals to the D17B from the Flexowriter. These circuits are required for the purposes of suppressing noise, changing voltage levels, inverting the signals from positive to negative logic, shortening the pulses, delaying the timing pulse, and generating the complement. Figure 3 illustrates the effect of these circuits on the Flexowriter waveforms. Figure 4 illustrates the waveshaping accomplished for the timing pulse. Figure 5 is a block diagram of the electronic circuits required for conditioning the input signals to the Flexowriter from the D17B. These circuits are required for stretching or storing the information pulses, delaying the timing pulse, changing voltage levels, and inverting the signals from negative to positive logic.

The Flexowriter provides for typewriter keyboard or paper tape entry of data or instructions into the D17B in octal format rather than binary. The capability of retaining a hard copy typed record or a punched paper tape corresponding to the program and data being loaded is very desirable.

Hard copy typed output and punched paper tape output are also available. ACRT display scope is available for output monitoring of any memory location.

NUMBER AND COMMAND CODING

		I1	I2	I3	I4	I5	TC	TC'
NUMBER	0	0	0	0	0	1	1	0
	1	1	0	0	0	0	1	0
	2	0	1	0	0	0	1	0
	3	1	1	0	0	1	1	0
	4	0	0	1	0	0	1	0
	5	1	0	1	0	1	1	0
	6	0	1	1	0	1	1	0
	7	1	1	1	0	0	1	0
	HALT	0	0	0	1	0	1	0
	LOCATION	1	0	0	1	1	1	0
	FILL	0	1	0	1	1	1	0
	VERIFY	1	1	0	1	0	1	0
	COMPUTE	0	0	1	1	1	1	0
	ENTER	1	0	1	1	0	1	0
	CLEAR	0	1	1	1	0	1	0
	DELETE	1	1	1	1	1	1	0

Table 1. D17B codes for octal and control characters.

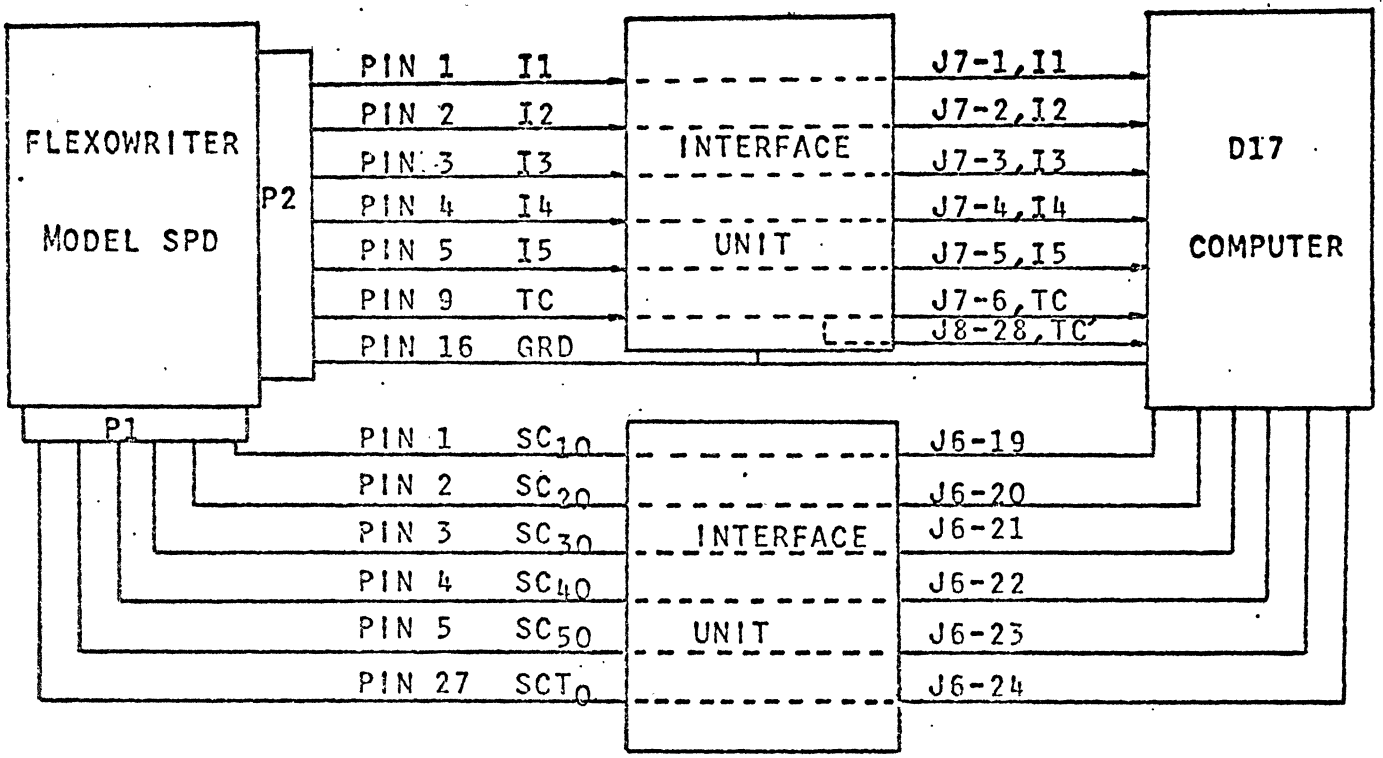


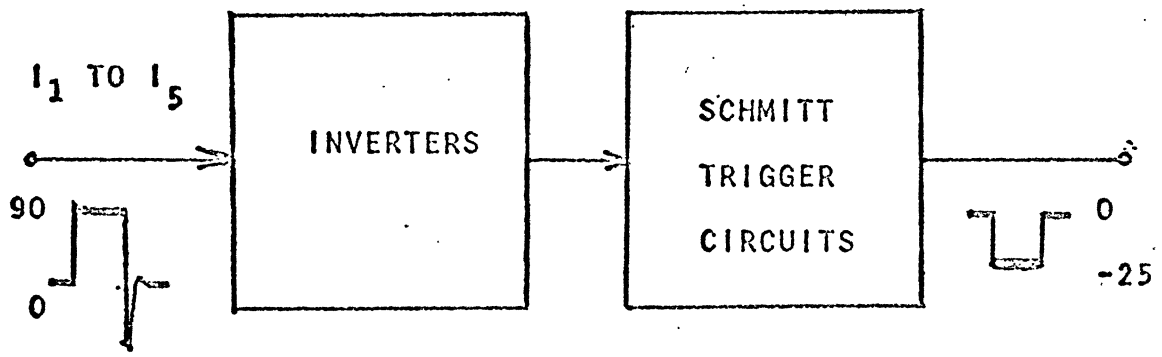
Figure 1. Schematic diagram of the Flexowriter-DlyB interface.

KEY	FUNCTION	FLEXOWRITER OUTPUTS I1	I2	I3	I4	I5	MODIFIED FLEXOWRITER OUTPUTS I1	I2	I3	I4	I5
SPACE	0	0	0	0	0	1	0	0	0	0	1
I	LOCATION	1	0	0	1	1	1	0	0	1	1
=	ENTER	1	0	1	0	1	1	0	1	1	0
,	FILL	1	1	0	1	1	0	1	0	1	1
;	COMPUTE	0	0	0	0	1	0	0	1	1	1
.	VERIFY	1	1	0	1	0	1	1	0	1	0
?	CLEAR	1	1	1	0	0	0	1	1	1	0
'	HALT	1	0	0	0	0	0	0	0	1	0

Table 2. Flexowriter code modifications.

INTERFACE

[A] INFORMATION SIGNALS



[B] TIMING PULSE

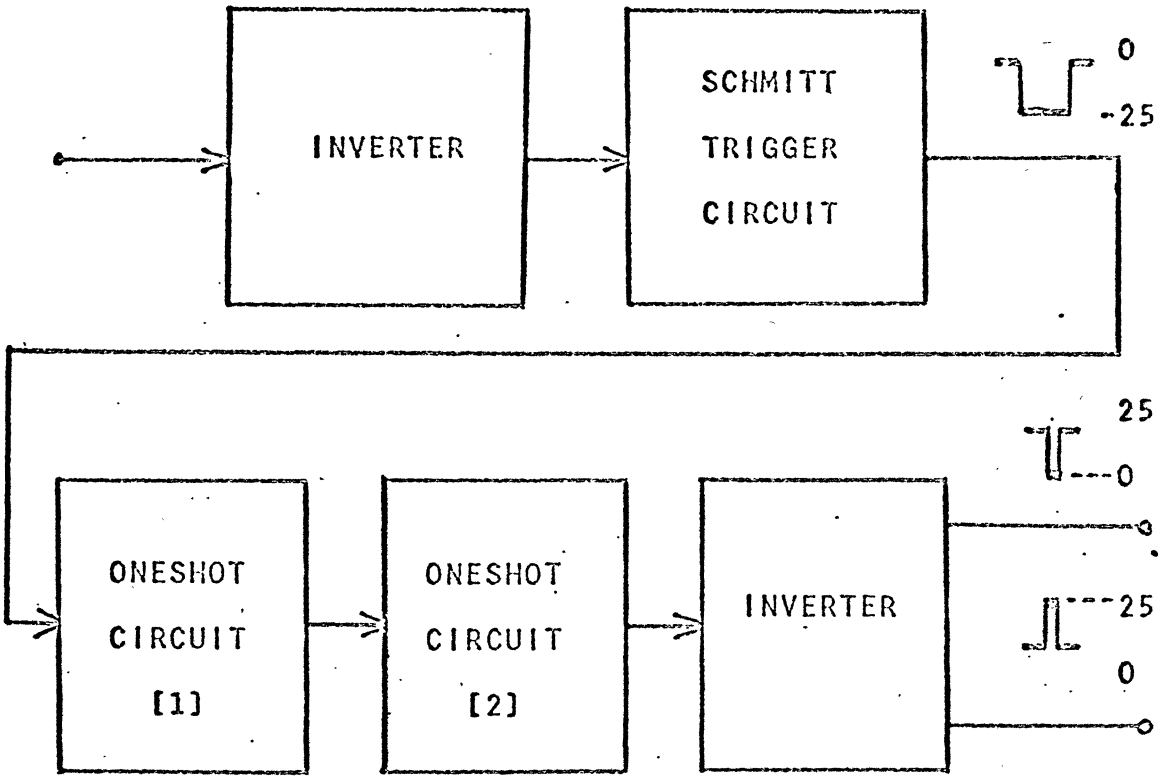


Figure 2. Block diagram of the Flexowriter to D17B interface.

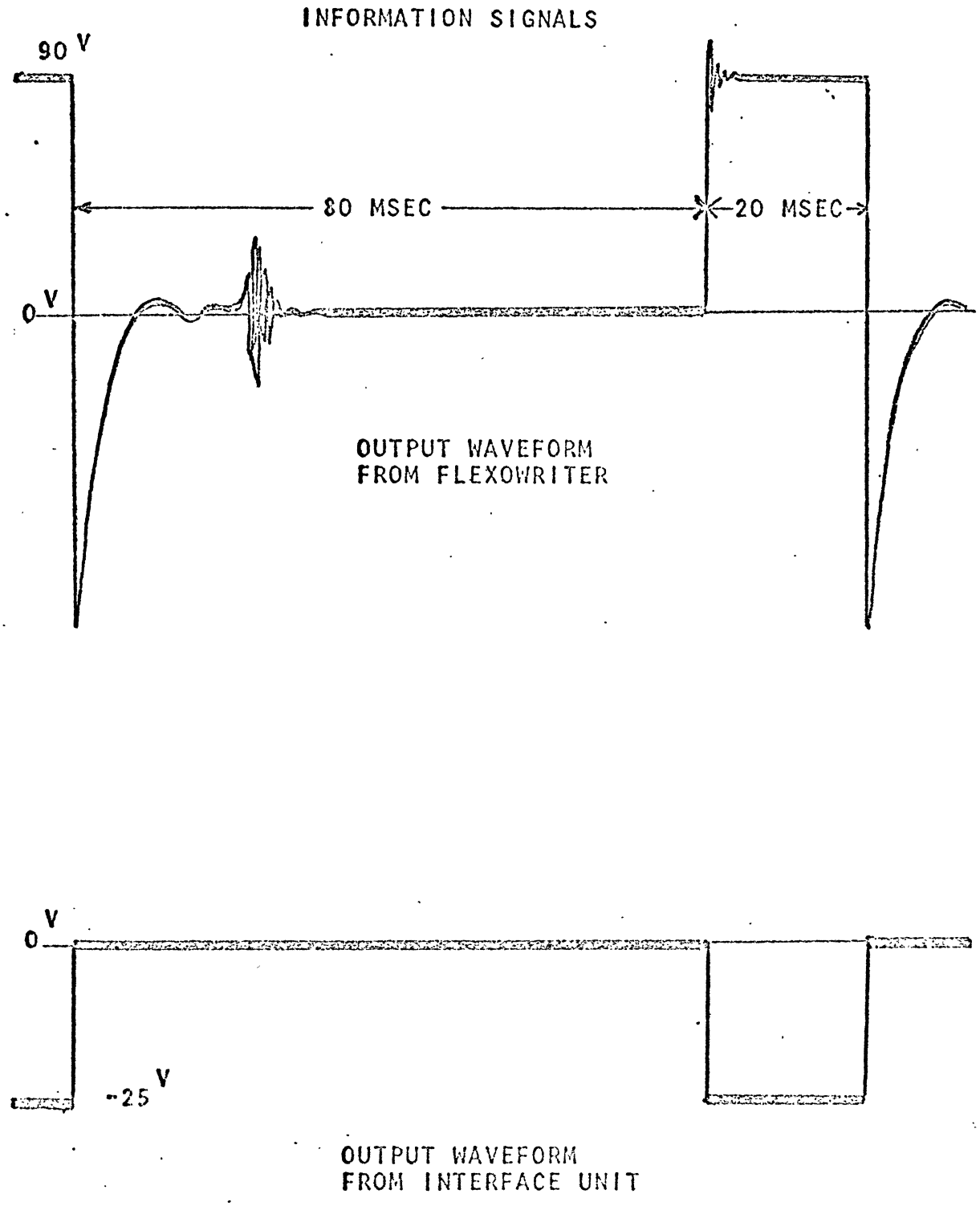


Figure 3. Shaped output waveform from the Flexowriter.

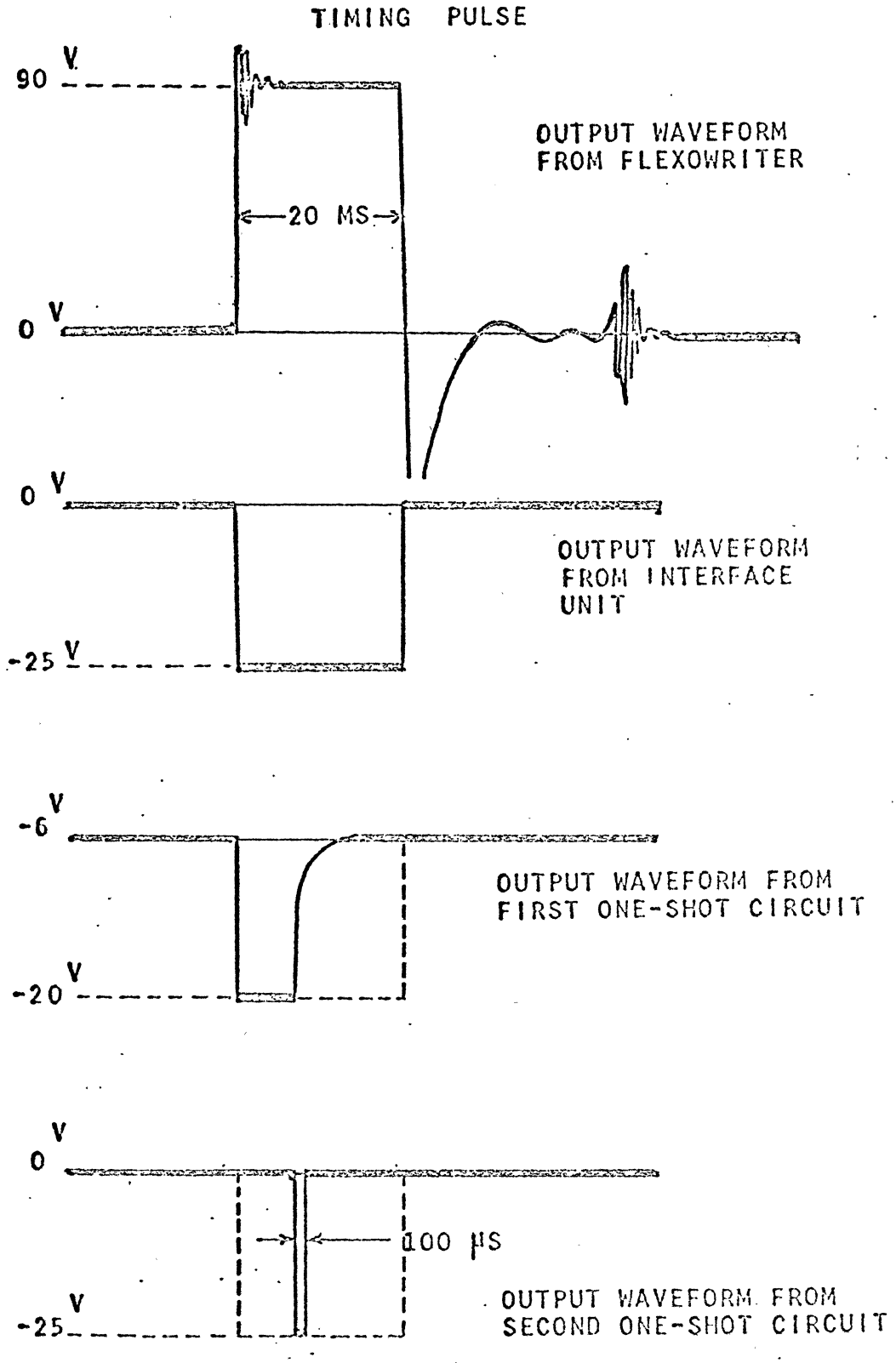


Figure 4. Shaping the delayed output timing pulse from the Flexowriter.

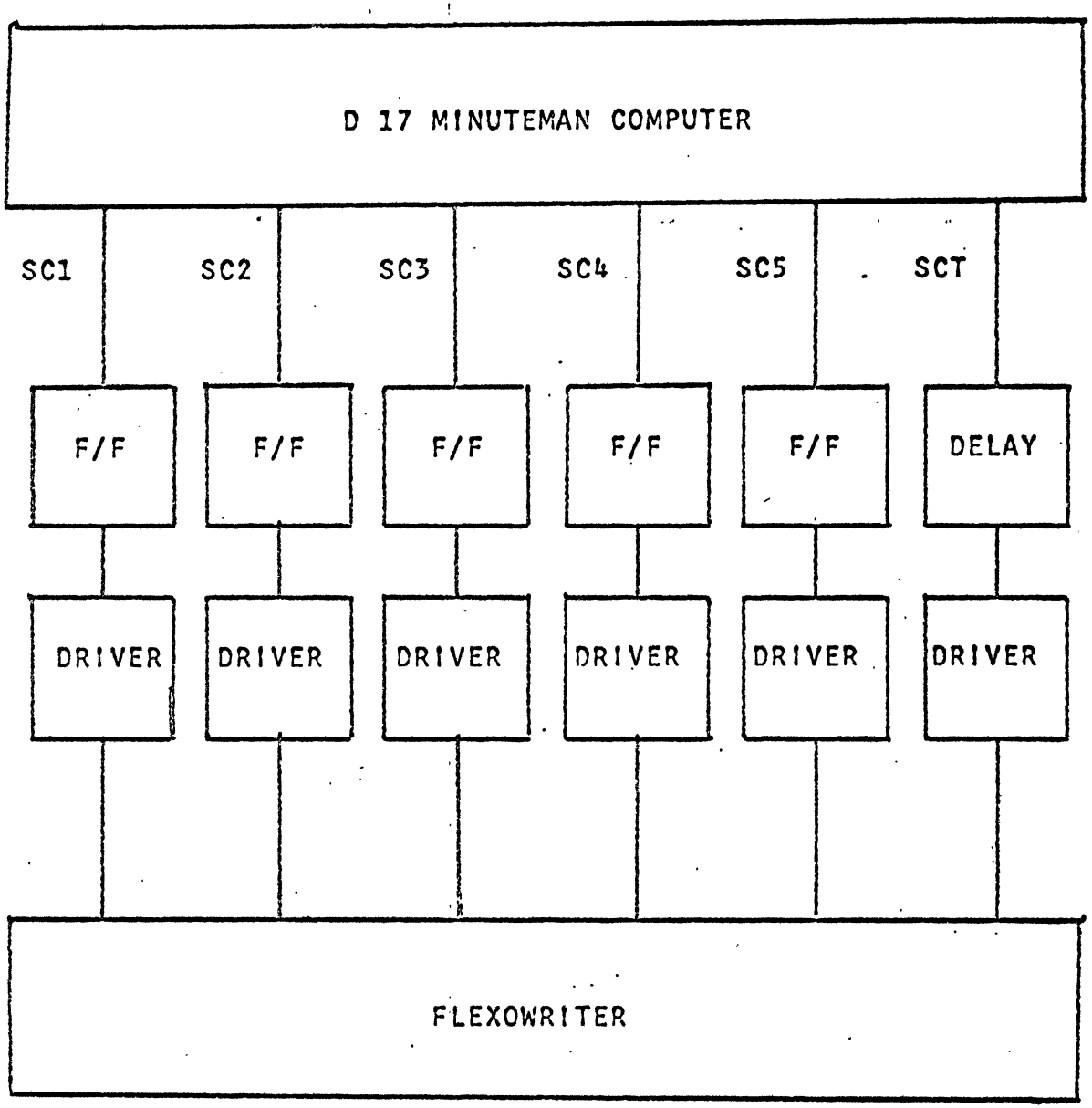


Figure 5 . Block diagram of the D17B to Flexowriter interface.

D17B COMPUTER APPLICATIONS

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Although the D17B does not provide all the desirable features of large general-purpose machines, it does resemble them functionally and it possesses a number of similar festures. It is a versatile multipurpose computer capable of solving a wide range of problems;[1,2] however, it has limited capability both in storage capacity and computation speed. Unlike the large general-purpose computer which is designed to efficiently process many different programs, the multipurpose D17B is better suited to dedicated or fixed tasks that can be served effectively by economical use of the available memory and speed of execution.[3,4]

Consequently, the D17B, like commercial minicomputers with small memories, is not well suited for general-purpose computing when compared to a large computer.[5] General-purpose computation in minicomputer terminology refers to stand-alone operation. Some minicomputers are used as stand-alone computers for scientific and engineering use, but most are used in real-time applications such as control, data acquisition, communication concentrators and processors, peripheral controllers and preprocessors for large computer systems, display controllers, buffer memories, bio-medical monitoring, automated testing, automated instrumentation and telemetry.[6-23]

In a practical sense, the capability for general computing is determined by the ability to perform a large variety of calculations. This ability, in turn, is determined basically by the instruction set. Available subroutines simplify the programming, and assemblers and compilers simplify the task further. The goal in providing general-purpose software for the D17B is to minimize the amount

of time, effort, and knowledge required for a user to arrive at a point of useful return for his investment in the development of the D17B. But, generality always comes at a price. The D17B is limited at present to a small number of real-time, special-purpose machine language programs.

The apparent lack of speed is not such an important factor when the D17B is used as a dedicated control computer since much computing speed available in a large general-purpose computer is commonly lost in system overhead and I/O.[24,25] Furthermore, the 4-bit and 8-bit parallel output data channels available on the D17B should prove to be very advantageous in communications systems that operate on 8-bit ASCII characters, becuase the overhead operations of packing and unpacking are minimized. The 24-bit double precision data word used on the D17B appears to have considerable utility for computation associated with these 8-bit codes for character representation which are now becoming standard. Therefore, the 24-bit word of the D17B not only offers more precision than most minicomputers, but it provides for outputting 8-bit submultiples.

Computer control applications may include monitoring and data processing, start-up and shut-down procedures, and optimal control. The main attributes of computer control are computational speed, storage capability, and decision-making ability. If sufficient computational speed is available, optimal control can be accomplished. The storage capability provides for economical and efficient data recording and processing. Decision-making ability provides the capability for direct digital control.

A direct digital control system must provide a means for measuring the condition to be controlled, compare the measured value with a desired value, and automatically cause the two values to agree. Data logging can be performed as one phase of the control operation. Feed-forward control requires the solution of equations which represent a predictive mathematical model. A

control computer can also be used for supervisory functions such as start-up or shut down operations. Direct digital control requires that each variable be compared in turn with the desired values.

Logical decisions and constraints can be employed in computer control, and the results of intermediate calculations and control actions can be recorded to produce a historical file. The general-purpose capabilities of the D17B permit the control program to be modified and expanded within the limits of memory capacity to fit system growth, new instruments, or changing control policy. The versatility available with a computer control system involving a general-purpose computer is an important consideration.

If the D17B is to be used for control computing applications, it must be capable of not only performing control calculations, but a number of other essential functions also. For example, raw input data are generally subjected to individual limit checks to detect instrument failures or out-or-normal conditions, averaged or smoothed to minimize the effects of random variations, and then recorded or used in calculations. As a typical example of a limit check in terms of D17B instructions, the following could be executed:

1. DIA - data input to A
2. MIM - replace the contents of A by the negative of the present magnitude of the contents of A
3. ADD - add the limit tolerance to the contents of A
4. TMI - transfer on minus

These four instructions would accomplish the limit check by performing a conditional branch. Similar operations could be equally useful for general or special-purpose computing.

It is appropriate that the D17B be considered for dedicated control applications involving control over a single unit or a limited portion of a process. Such an application may not only be appropriate considering the

limited memory and execution speed of the D17B, but the system reliability consideration makes D17B's ideally suited to such tasks. Process-wide control may require several interconnected D17B's. The real-time aspect of control applications is compatible with the current requirement of machine language programming for the D17B.

Considerable benefit can be gained by using dedicated computers which decentralize system design and simplify software requirements. The major advantages of using several dedicated control computers are the complete independence of each unit from failures in other units and the reduced sophistication required to program the computations. Dedicated control computers make automated start-up a practical consideration.

Since A-D and D-A converters and multiplexers are required for each computer, the use of several dedicated D17B's could represent too large an expenditure in conversion equipment. But, because conversion and other subsystem costs have been reduced considerably, the use of several dedicated computers appears to be feasible. Delays caused by breakdown can be avoided by using a dedicated on-line machine, and there is no question about program security.

As new instruments are added and as knowledge of a process increases, better control policies can be developed. Hence, control programs are constantly in need of change. Also, the characteristics of the process will often change as its operation is improved through computer control. Because of these factors, the programmable feature of the D17B is extremely desirable as well as its flexible I/O capabilities, which can accomodate a variety of control devices. The D17B can provide digital, pulse-type, and analog output signals under program control for manipulating process variables. This flexible I/O capability provides for efficient interaction between the D17B and the devices being controlled.

In addition to capabilities required for general computing applications, control computing applications require a flexible I/O structure to accomodate a variety of devices. As described previously, the I/O capability of the D17B is extremely versatile.

For real-time control applications, the D17B must be able to accept and process input data sufficiently fast that the results of this processing can be used to influence and control the appropriate variables. The D17B was designed to accomplish real-time computation as required for missile guidance; however, the bandwidth of the particular application will dictate the speed requirement. The D17B performed real-time communication with external devices such as velocity meters, accelerometers, and D-A converters to obtain data and issue commands necessary for navigation, guidance, telemetry, and control functions.

As indicated in the specifications, the D17B has a maximum I/O data rate of 25,600 words per second. Direct data entry is also provided. Hence, within the limits of its capabilities the D17B appears to be very appropriate for a variety of control and special-purpose applications.

Certain special-purpose applications such as on-line digital data processing, computer interfacing, peripheral buffering, and data monitoring require very little CPU sophistication, limited arithmetic capability, and perhaps low-speed performance compatible with the D17B specifications. The dominant requirment of many special-purpose computer applications relates to the I/O architecture as is the case for control applications. The importance of I/O channels is particularly significant where data is being transmitted continuously between the computer and peripheral devices.

On-line digital data processing often requires that analog information be converted to digital form using an A-D converter. With the 24-bit double

precision word of the D17B, the output from two 12-bit A-D converters can be inputted simultaneously under program control. The required speed of I/O transfers and arithmetic for special-purpose data acquisition can be much slower than for control applications because real-time analysis and control response commands are not necessary. Hence, the D17B is flexible enough to be used in these areas formerly requiring special-purpose computers. As requirements change, the D17B can easily be re-programmed. In such fields as medical research, biological studies, and experimental physics, the D17B can be programmed to control the monitoring, measuring, and recording of a variety of quantities such as pressures, flow rates, EKG, and heart rate. Automation of chemical laboratory instruments such as chromatographs, spectrometers and AutoAnalyzers using the D17B also appears feasible. Calculation of desired parameters, recording of results, and graphic display are appropriate applications areas for this computer. Simultaneous measurements of several quantities are possible through the use of sample-and-hold devices, a multiplexer, and an A-D converter.

A flexible, reliable, mobile data monitoring system can be developed using the D17B computer with interface to any of the following: operational amplifiers, sample-and-hold devices, multiplexers, analog-to-digital converters, digital voltmeters, counters, CRT displays, plotters, programmable signal generators and power supplies, transducers, and sensors. This combination will provide for the automatic testing of electronics components, IC, logic cards, complete logic assemblies, and other devices and circuits. Programmed transducer testing and high-quality data collection of signal characteristics such as amplitude, current, and phase which can be accomplished at high speeds have significant advantages over manual methods. These techniques are also applicable to non-destructive testing as employed in the inventory of aircraft

parts based on the characteristics of the steel as represented by the electrical output of spectrometer-type instruments.

On-line communication is also an important applications area to be considered for the D17B. A data-concentration buffer storage system for teletype and other low speed I/O devices can be developed. Programmed multiplexing of parallel information for serial transmission over a narrow-band communication channel is possible since the D17B can provide for changing the scan rate. Preprocessing for analysis and computation by a large-scale computer will also be an appropriate consideration.

REFERENCES

1. E. D. DeCastro, "What can you do with a minicomputer," Industrial Research, November 1969.

2. M. J. Lowenstein, "The minicomputer: The machine with an endless future," Electronic Design, vol. 18, no. 9, April 1970.

3. R. Rinder, "The input/output architecture of minicomputers," Datamation, vol. 16, pp. 119-124, May 1970.

4. W. H. Roberts, "Minicomputer architecture," IEEE Computer Group News, vol. 3, pp. 5-9, July/August 1970.

5. F. Gruenberger, "Are small free-standing computers here to stay?" Datamation, vol. 12, pp. 67-68, April 1966.

6. E. Abrahamson, "Minicomputers for large-scale process control," Datamation, vol. 16, pp. 123-126, February 1970.

7. R. E. Anderson, "Dedicated computers for instrument control," March 15, 1968, Contract W-7405-eng-48. (UCRL-70638).

8. R. E. Anderson and J. W. Frazer, "Computer control in chemistry at the lawrence radiation laboratory," J. Comp. Phys. vol. 2, p. 484, 1968.

9. D. A. Babroff, "Avoid pitfalls in computerized testing," Electronic Design, vol. 17, pp. 196-201, August 1969.

10. S. J. Bailey, "On-line computer users polled," Control Engineering, pp. 86-94, January 1969.

11. H. Cole, "Computer-operated X-ray laboratory equipment," IBM Journal of Research and Development, vol. 13, pp. 5-14, January 1969.

12. R. A. Edwards and B. H. Polishook, "Laboratory automation based (LAB) systems," Instrument Society of America, 23rd Annual Conference, New York, October 28-31, 1968.

13. J. W. Frazer, "Digital control computers," Anal. Chem. vol. 40, p. 26A, 1968, and "Instruments and computers," Science and Tech., p. 41, July 1968.

14. J. W. Frazer, "Instruments and computers," Science and Technology, no. 79, p. 41, July 1968.

15. W. D. Gwinn, et al, "On-line control, data collection, and reduction for chemical experiments," J. Comp. Phys., vol. 2, p. 439, 1968.

16. J. A. Jones, "On-line computers: A survey of techniques and concepts applied to low-energy nulear research," IEEE Trans. Nucl. Sci., p. 576, February 1967.

REFERENCES (continued)

17. J. N. Kessler, "Where EE and MD link up to prolong life," Electronic Design, vol. 18, no. 4, pp. 24-28, February 1970.

18. M. H. Mueller, L. Heaton, and L. Amiot, "A computer controlled experiment," Research and Development, p. 34, August 1968.

19. R. P. Noonan, "What kind of computer for your plant," Chemical Engineering, pp. 114-116, June 1969.

20. R. E. Penczer, "Automation in data acquisition," American Laboratory, April 1969.

21. R. J. Spinrad, "Automation in the laboratory," Science, vol. 158, p. 55, 1967.

22. T. M. Stout, "Process control," Datamation, vol. 12, pp. 22-27, February 1966.

23. N. F. Young, "Distributed computer systems," Automation, October 1969.

24. F. Coury, "A systems approach to minicomputer I/O," Proc. AFIPS 1970 SJCC, 1970

25. E. Holland, "Minicomputer I/O and peripherals," IEEE Computer Group News, vol. 3, pp. 10-14, July/August 1970.

PROGRAMMING THE D17B COMPUTER

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The logical power of general-purpose computers is uniquely common to all such machines, but speed of execution, memory size, cost, reliability, and ease of communication (convenience to the user) differ widely. Size and weight limitations, a high degree of reliability and strength, plus program requirements dictated a small, slow, serial memory for the D17B. However, many minicomputers have less than half the memory of the D17B.[1,2] Requirements for real-time operation imply the need for the D17B to sequentially perform its assigned tasks fast enough so that all tasks are accomplished during a given period of time and yet slow enough to ensure accurate noise-free computation.[3]

In addition to the usual capabilities common to small general-purpose computers, it can be seen in Figure 1 that the D17B has analog, pulse-type, and serial output systems. Parallel or multiprocessing such as the simultaneous execution of two identical single-precision add, subtract, or multiply instructions is another unusual operational capability.

The need for store instructions arises frequently because of the need to preserve intermediate results while some related intervening series of operations is being performed as in the evaluation of a general polynomial. Simultaneous execution of a store operation is possible on the D17B coincident with the initiation of other operations without requiring an additional instruction. The contents of the accumulator will be stored in the channel specified by the S_F address as illustrated in Figure 2.

Instruction and address modification give the program the ability to branch to alternative sequences of instructions under program control as a result of calculations in addition to the use of conditional and unconditional

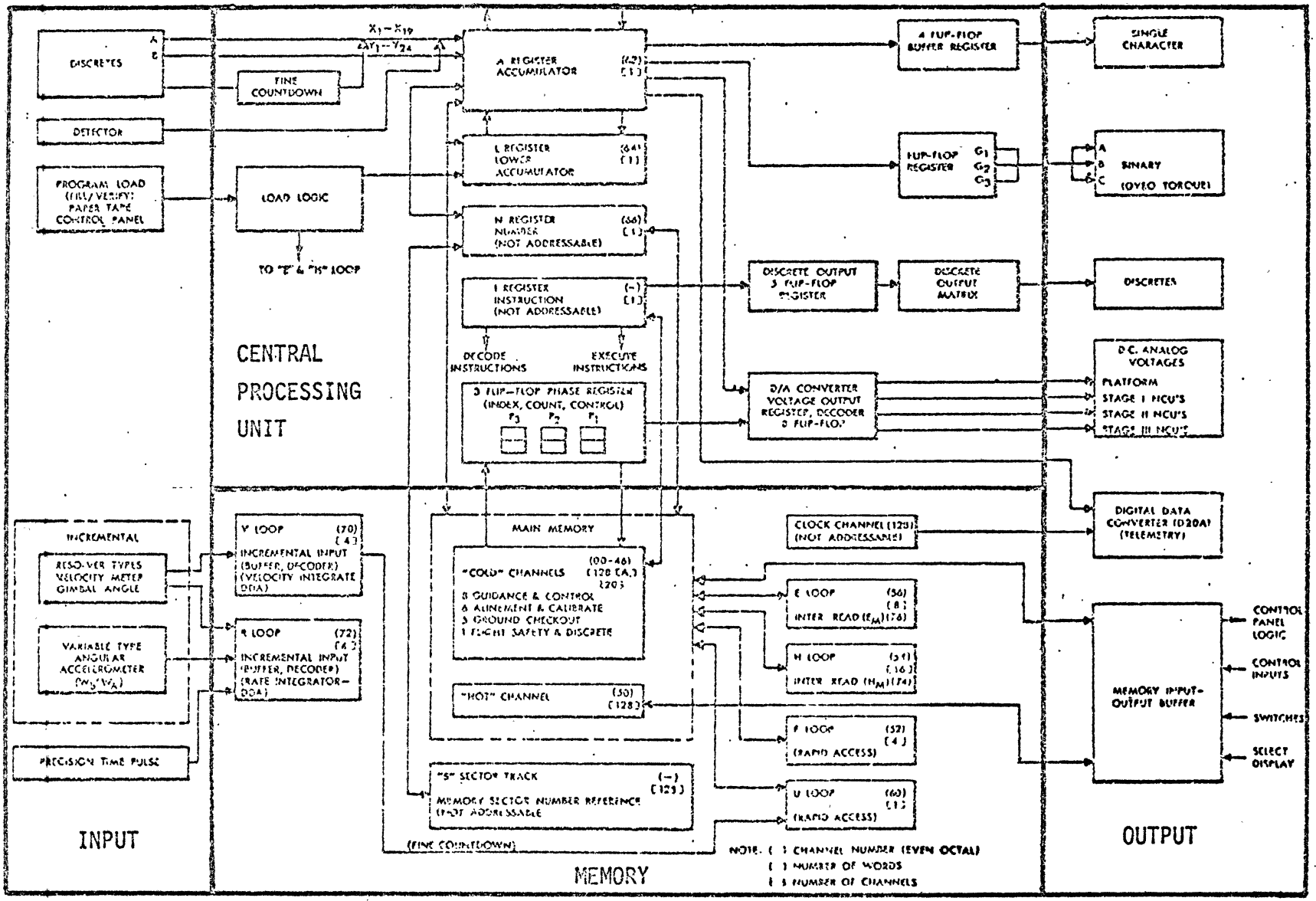
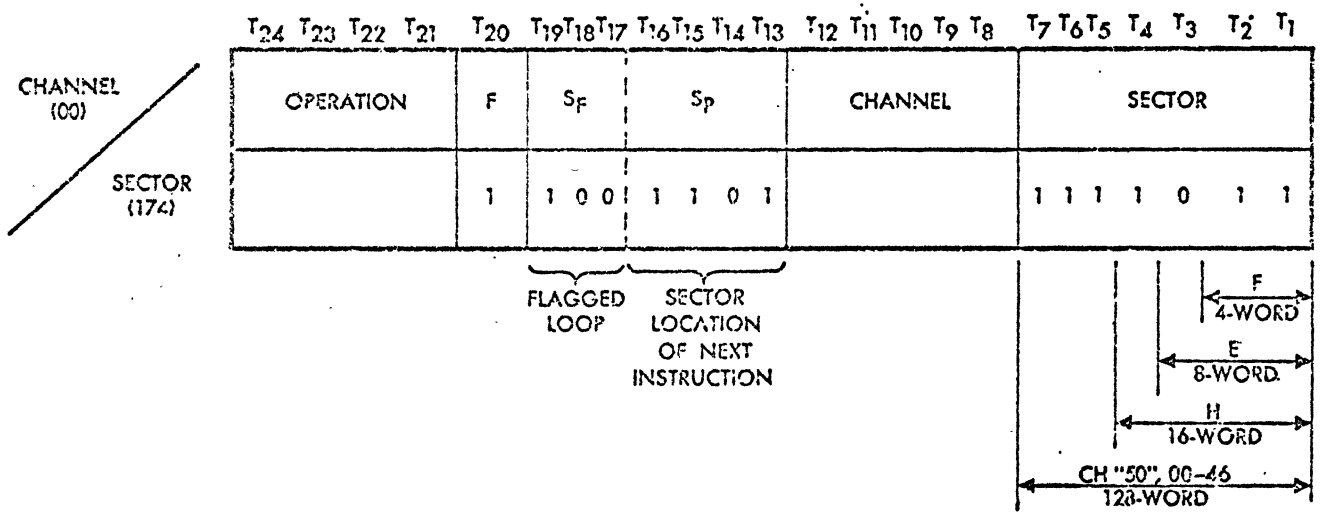


Figure 1. D17B functional data flow diagram.



① THE NEXT INSTRUCTION WILL COME FROM ONE OF THE NEXT 16 SECTORS AFTER OPERAND AGREEMENT.

② THE CONTENTS OF THE A-REGISTER WILL BE COPIED INTO THE FLAGGED CHANNEL UPON EXECUTION OF THE FLAGGED INSTRUCTION. THE WORD LOCATION OF THE FLAGGED CHANNEL, WHERE THE CONTENTS OF THE A-REGISTER WILL BE STORED IS DEPENDENT UPON THE APPROPRIATE OPERAND SECTOR BITS.

Figure 2. Flag store instruction sector coding.

branching instructions. Bit manipulation is also possible if the accumulator is masked by using the logical AND instruction.

The instruction repertoire listed in Table 1 contains 39 types of machine language instructions. Although each type of instruction executed by the D17B differs from the others, the kinds of actions performed occur in a common sequence. This makes it convenient to describe the execution of each instruction as being accomplished in the following five phases which are usually common to delay-type memories:

1. Instruction search (IS)
2. Instruction read (IR)
3. Operand search (OS)
4. Operand read (OR)
5. Execute (EX)

Figure 3 shows that the D17B can perform several of these phases simultaneously with increased efficiency compared to sequential operation. This figure assumes minimal delay coding of instructions which require an execution time of one word time. The advantage of this minimized access timing is that, once a minimal delay coded program is initiated, the effective completion time of any instruction is equal to the basic execution time of the instruction. If random access addressing were used in the D17B, the search operations (IS and OS) could each require up to 128 word times or one disk revolution of 10 ms. Minimal delay coding places the next instruction at a location which will pass the read head immediately after completion of the current instruction.

The word size for minicomputers ranges from 8 to 24 bits.[4] Providing for direct addressing of the entire memory of the D17B as illustrated in Figure 4 by using a 12-bit operand address field is a feature of considerable value. A typical two-address (unflagged) D17B instruction as illustrated in Figure 5 has three parts: an op code and two addresses. One address

Numeric Code	Code	Description
00 20, s	SAL	Split accumulator left shift
00 22, s	ALS	Accumulator left shift
00 24, 2	SLL	Split left word left shift
00 26, s	SLR	Split left word right shift
00 30, s	SAR	Split accumulator right shift
00 32, s	ARS	Accumulator right shift
00 34, s	SRL	Split right word left shift
00 36, s	SRR	Split right word right shift
00 60, s	COA	Character output A
04 c, s	SCL	Split Compare and limit
10 c, s	TMI	Transfer on minus
20 c, s	SMP	Split multiply
24 c, s	MPY	Multiply
30 c, s	SMM	Split multiply modified
34 c, s	MPM	Multiply modified
40 02, s	BOC	Binary output C
40 10, s	BOA	Binary output A
40 12, s	BOB	Binary output B
40 20, s	RSD	Reset detector
40 22, s	HPR	Halt and Proceed
40 26, s	DOA	Discrete output A
40 30, s	VOA	Voltage output A
40 32, s	VOB	Voltage output B
40 34, s	VOC	Voltage output C
40 42, s	ANA	And to accumulator
40 44, s	MIM	Minus magnitude
40 46, s	COM	Complement
40 50, s	DIB	Discrete input B
40 52, s	DIA	Discrete input A
40 60, s	HFC	Halt fine countdown
40 62, s	EFC	Enter fine countdown
40 7-, s	LPR	Load phase register
44 c, s	CLA	Clear and Add
50 c, s	TRA	Transfer
54 c, s	STO	Store accumulator
60 c, s	SAD	Split add
64 c, s	ADD	Add
70 c, s	SSU	Split subtract
74 c, s	SUB	Subtract

Table 1. D17B instruction repertoire.

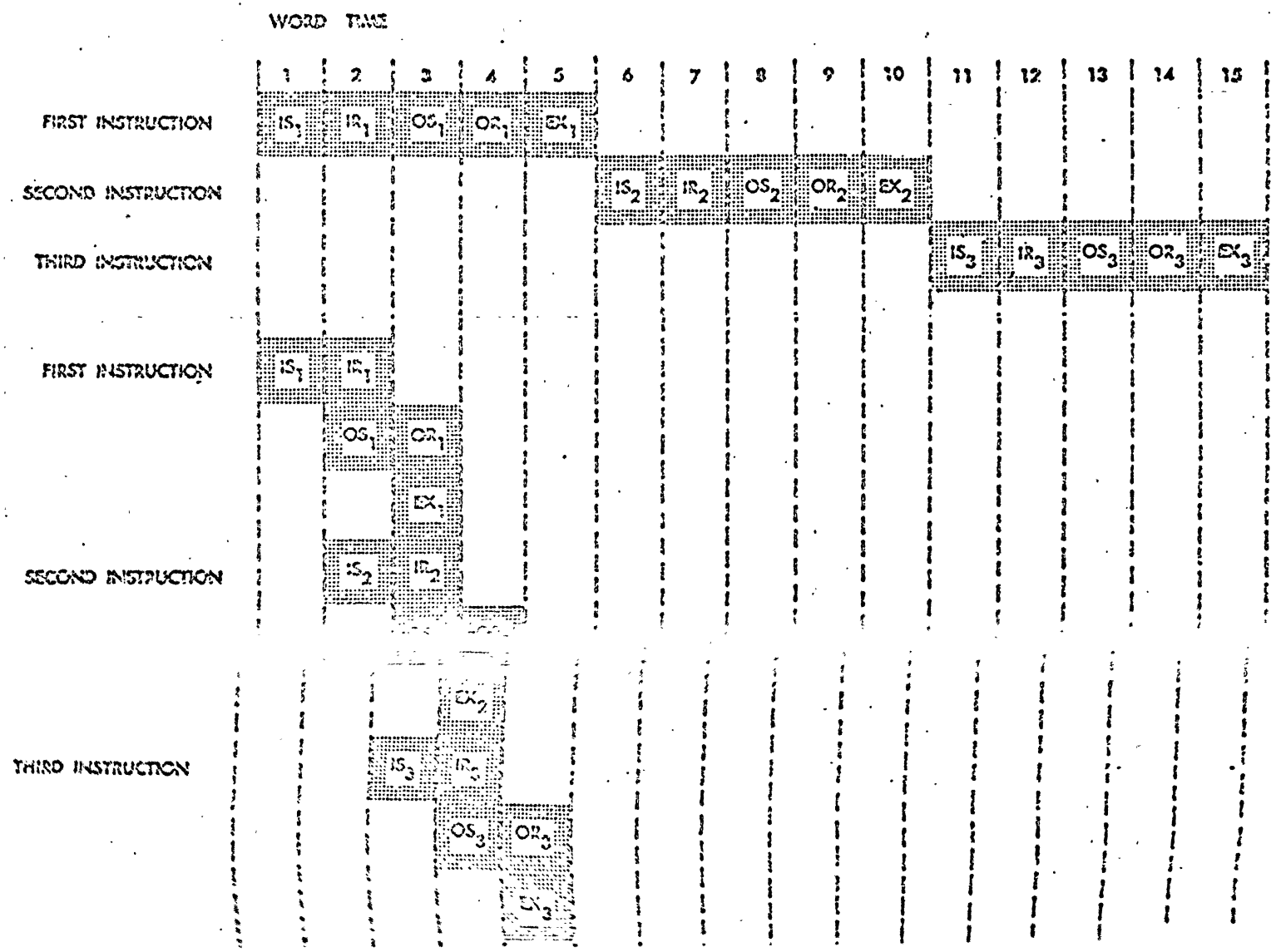


Figure 5. Five phases of D17B instruction execution compared to sequential operation.

UNFLAGGED INSTRUCTION ($T_{20}=0$)

T_P	T_{24} T_{23} T_{22} T_{21}	T_{20}	T_{19} T_{18} T_{17} T_{16} T_{15} T_{14} T_{13}	T_{12} T_{11} T_{10} T_9 T_8	T_7 T_6 T_5 T_4 T_3 T_2 T_1	T_0 T_X
X	OPERATION CODE Op	FLAG F	NEXT INSTRUCTION SECTOR ADDRESS Sp	CHANNEL NUMBER C	SECTOR NUMBER S	X X

FLAGGED INSTRUCTION ($T_{20}=1$)

T_P	T_{24} T_{23} T_{22} T_{21}	T_{20}	T_{19} T_{18} T_{17} T_{16}	T_{15} T_{14} T_{13}	T_{12} T_{11} T_{10} T_9 T_8	T_7 T_6 T_5 T_4 T_3 T_2 T_1	T_0 T_X
X	OPERATION CODE	FLAG	FLAG STORAGE LOCATION S_f	SECTOR OF NEXT INSTRUCTION S_p	CHANNEL NUMBER	SECTOR NUMBER	X X

Figure 4. D17B instruction word format.

UNFLAGGED INSTRUCTION

OP CODE				F	NEXT INSTRUCTION SECTOR							OPERAND												
T_{24}	T_{23}	T_{22}	T_{21}	T_{20}	T_{19}	T_{18}	T_{17}	T_{16}	T_{15}	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	T_7	T_6	T_5	T_4	T_3	T_2	T_1	
OP				F	SP							C					S							
1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	BINARY
7			4	0	1	7			7			7			6		1	7			7			QUASI-OCTAL
7			5		7				7			7			7		7				7			OCTAL (MAXIMUM VALUE)

CODE	RANGE	NUMBERING SYSTEM
SECTOR	000 ϕ 177;	SEQUENTIAL OCTAL (0, 1, 2, 3, 4, 5, 6,...177)
CHANNEL	00 ϕ 76;	EVEN OCTAL (0, 2, 4, 6, 10, 12,...76)
INSTRUCTION SECTOR	000 ϕ 177;	SEQUENTIAL OCTAL (0, 1, 2, 3, 4, 5, 6,...177)
UNFLAGGED INSTRUCTION	0;	UNFLAGGED INSTRUCTION
OPERATION	00 ϕ 74;	LAST OCTAL DIGIT ENDS IN 0 OR 4

Figure 5. Two-address (unflagged) D17B instruction coding.

identifies the operand which fulfills the same function as the address field in a single address machine; the second is the address mode field S_P which is used to specify the address of the next instruction within the active memory channel. One bit (F-flag) in the address mode field permits the use of two alternate address modes. If the flag bit is ON, an instruction is interpreted as a three-address word. A typical three-address (flagged) instruction as illustrated in Figure 6 has four parts: an op code and three addresses. One address again identifies the operand; the second is used to specify the channel S_F in which the present contents of the accumulator are to be stored; the third is used to specify the address S_P of the next instruction within the next sixteen successive memory locations in the active channel. A program in a single address machine is likely to require much more memory than is required by the D17B.

In the two-address format, the 12-bit operand address is required for direct addressing of the total memory, 7 bits are required to specify the address of the next instruction if any sector within the active channel is allowed, one bit is required for the flag, and the 4 remaining bits are allocated for the op code field. This limits the D17B to 16 unique 4-bit codes and a 12-bit operand address field. Two of the remaining 4-bit op codes are used for instructions that do not reference memory (control, logic, I/O and shifts). A 5-bit portion of the operand address field is used as an extension of the op code.

Considerable expansion of the instruction repertoire appears to be possible. Op code 14 is not used, hence the addition of one instruction that requires access to memory could be considered. Also, there are numerous unused 5-bit op code extensions which could be considered.

FLAGGED INSTRUCTION

O_P CODE				F	NEXT INST SECTOR							OPERAND												
T_{24}	T_{23}	T_{22}	T_{21}	T_{20}	T_{19}	T_{18}	T_{17}	T_{16}	T_{15}	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	T_7	T_6	T_5	T_4	T_3	T_2	T_1	
O_P				F	S_F			S_P				C					S							
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	BINARY CODING
7			4	2	1	6		1	7			7			6		1	7			7			QUASI-OCTAL CODING
7			7		7			7				7			7		7				7			OCTAL CODING

FLAGGED CHANNEL CODING

T_{19}	T_{18}	T_{17}	T_{11}	CODE	FUNCTION
0	0	0		0 0	IDLE
0	0	1		0 2	(F) 4-WORD LOOP
0	1	0		0 4	(T) TELEMETRY
0	1	1		0 6	(50) HOT CHANNEL
1	0	0		1 0	(E) 8-WORD LOOP
1	0	1		1 2	"L" 1-WORD REGISTER
1	1	0		1 4	(H) 16-WORD LOOP
1	1	1		1 6	(U) 1-WORD LOOP

Figure 6. Three-address (flagged) D17B instruction coding.

Compiler routines which have the advantage of reducing programming effort are not currently available for the D17B. The relative ineffiency of memory requirement for compiler-produced programs compared with programs written in machine language makes the on-line compiler approach questionable at this time.[5,6] The modular approach to the writing of special-purpose subroutines, such as required for I/O operations, can result in considerable savings in time and effort. Certain features such as dedicated I/O registers reduce the programmer's housekeeping task. The use of rapid-access memory loops provides programming versatility and efficiency that help to overcome the limited speed of execution and memory size of the D17B.

REFERENCES

1. J. Cohen, "Mini-computers," Modern Data, vol. 2, No. 8, 1969.

2. R. T. Ollivier, "A technique for selecting small computers," Datamation, vol. 16, pp. 141-145, January 1970.

3. D. J. Theis and L. C. Hobbs, "Mini-computers for real-time applications," Datamation, vol. 15, pp. 39-61, March 1969.

4. A. Epstein and D. Bessel, "Minicomputers are made of this," Computer Decisions, pp. 10-22, August 1970.

5. R. L. Hooper, "The minicomputer, a programming challenge," Proc. AFIPS 1968 FJCC, part 1, pp. 649-654, 1968.

6. H. W. Spencer, et al, "Small computer software," IEEE Computer Group News, vol. 3, pp. 15-20, July/August 1970.

An Input/Output Panel for the D17 Computer

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The D17 computer is a general purpose, serial computer. It is a negative logic machine with Logic 1 =-10volts and Logic 0 = 0 volts. These levels are generally applicable within the machine although input and output signals have different levels. The machine, as received,has no input or output equipment although it has the internal logic for interfacing to devices similar to Flexowriter.

Because of the absence of I/0 equipment it was decided to build a control panel consisting of a set of switches for input and control and a set of lights for output monitoring. The lights are used only as a convenience since the registers are easily monitored using an oscilloscope. The T_o signal which is a negative pulse occurring at the beginning of each word can be used to synch the oscilloscope externally and the accumulator (A_x) I-register (I_x) and L-register (L_x) can be displayed on the scope.

The block diagram for the panel is shown in Figure 1. The numbers on signal lines are the pin number for the D-17 and the number of the cable where applicable (each wire from J-1 and J-3 has an identification number). The circuitry for the switching section is shown in Figures 1 and 2. The relay and cross coupled NAND gates insure against multiple entry of a digit into the machine because of contact bounce of the switch. The Halt-Run switch is a 2-pole wafer switch and the Halt-Single Step switch is a telephone leaf switch. These were chosen to minimize contact bounce.

Figure 4 shows the timing diagrams for the control circuit. The clock signal, B_1 is a square wave which represents the beginning of bit at each transition. Some bits therefore follow

a positive transition of B_1 while others follow a negative-transition. The signal B_1 is then sent through a differentiating circuit which produces a positive pulse for the positive transition while the negative pulses are chipped. The clock signal is also inverted and sent through a differentiating circuit. These signals are then added together and inverted to produce a negative pulse for each bit. The time constants are adjusted so that the trailing edge (positive going) occurs near the center of each bit.

The control circuit is used to produce a single word length of clock pulses so that data can be shifted into the shift registers in 1-word increments. A master oscillator (M_p) is used to produce one word of clock pulses and therefore update the output registers every 3 milliseconds. The control circuit resets each time MD is low and at the next T_o pulse a both flip-flops go high until the second T_o pulse and then Flip-Flop 2 goes low. The outputs of the flip-flops then are used to gate the clock pulses into the shift input of the shift registers.

In order to obtain negative levels, the integrated circuits of the controller and the shift register are operated with the V_{cc} inputs at ground and the ground inputs at -5v. This results in a 0 to -5v logic swing. The shift registers are constructed with Type D flip flops. The outputs then drive lamps through discrete transistor driver circuits. These techniques are used to monitor A_x, L_x and I_x. Other signals could easily be monitored using similar techniques.

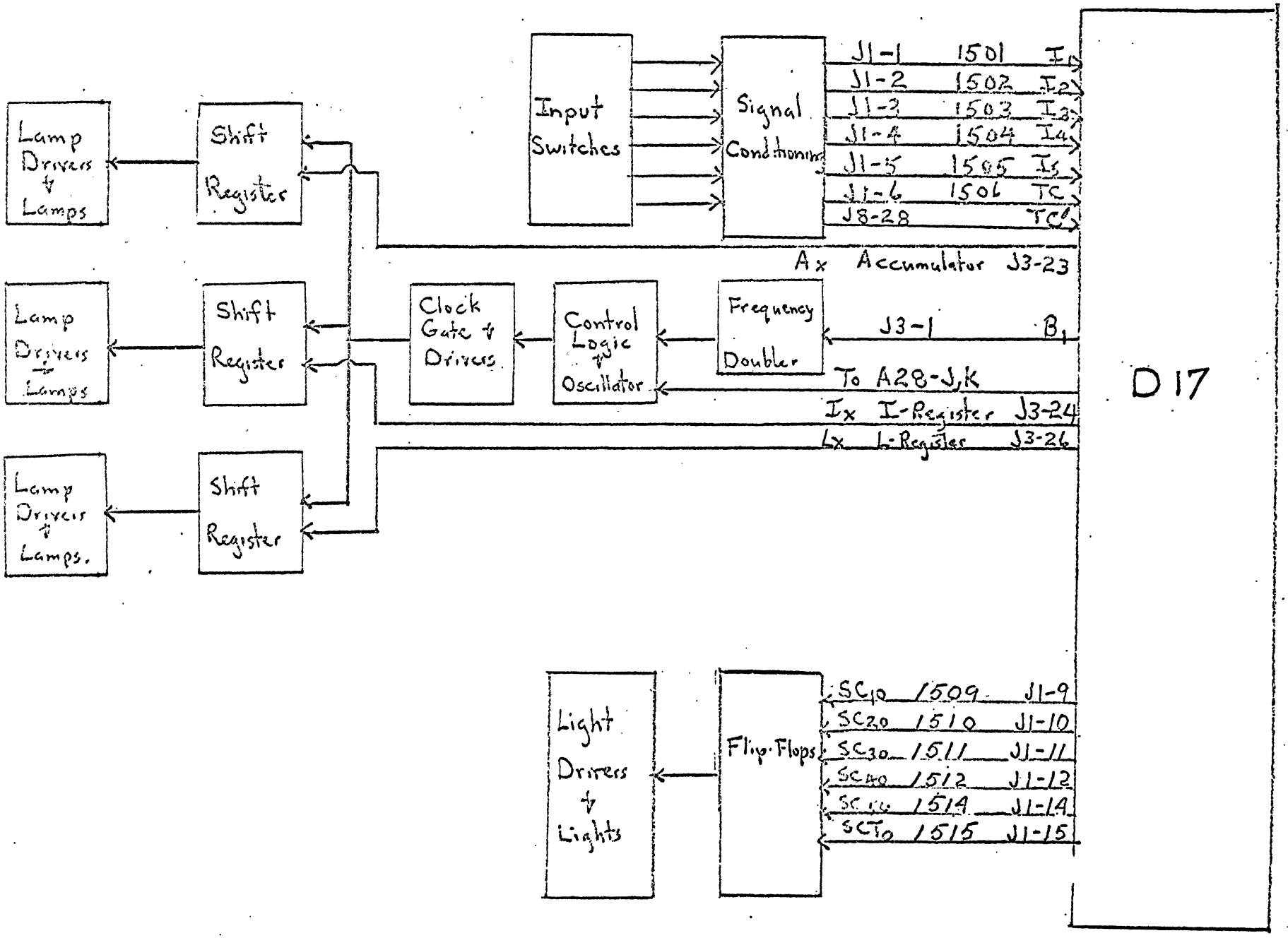


Figure 1 Block Diagram of I/O Panel

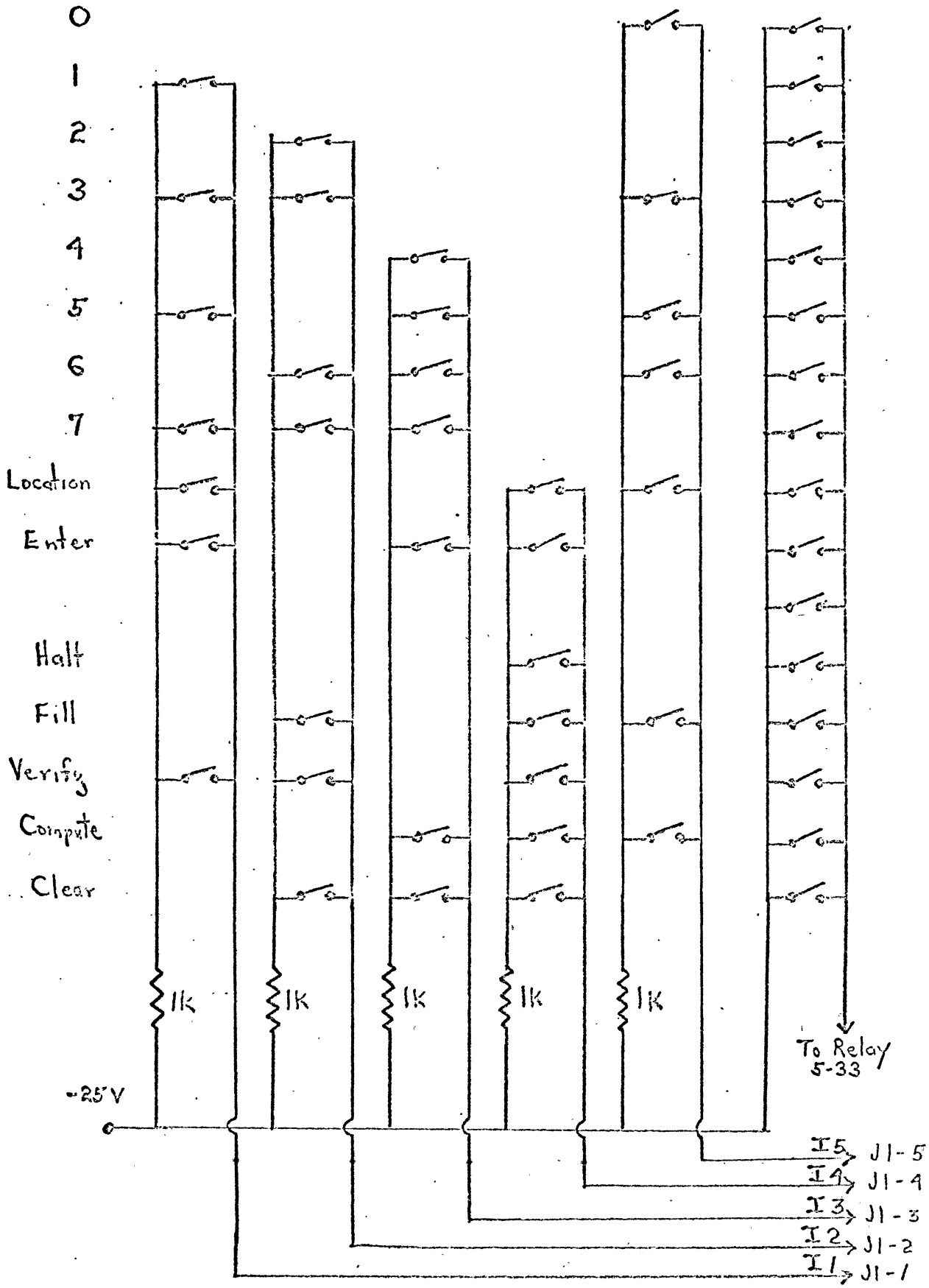
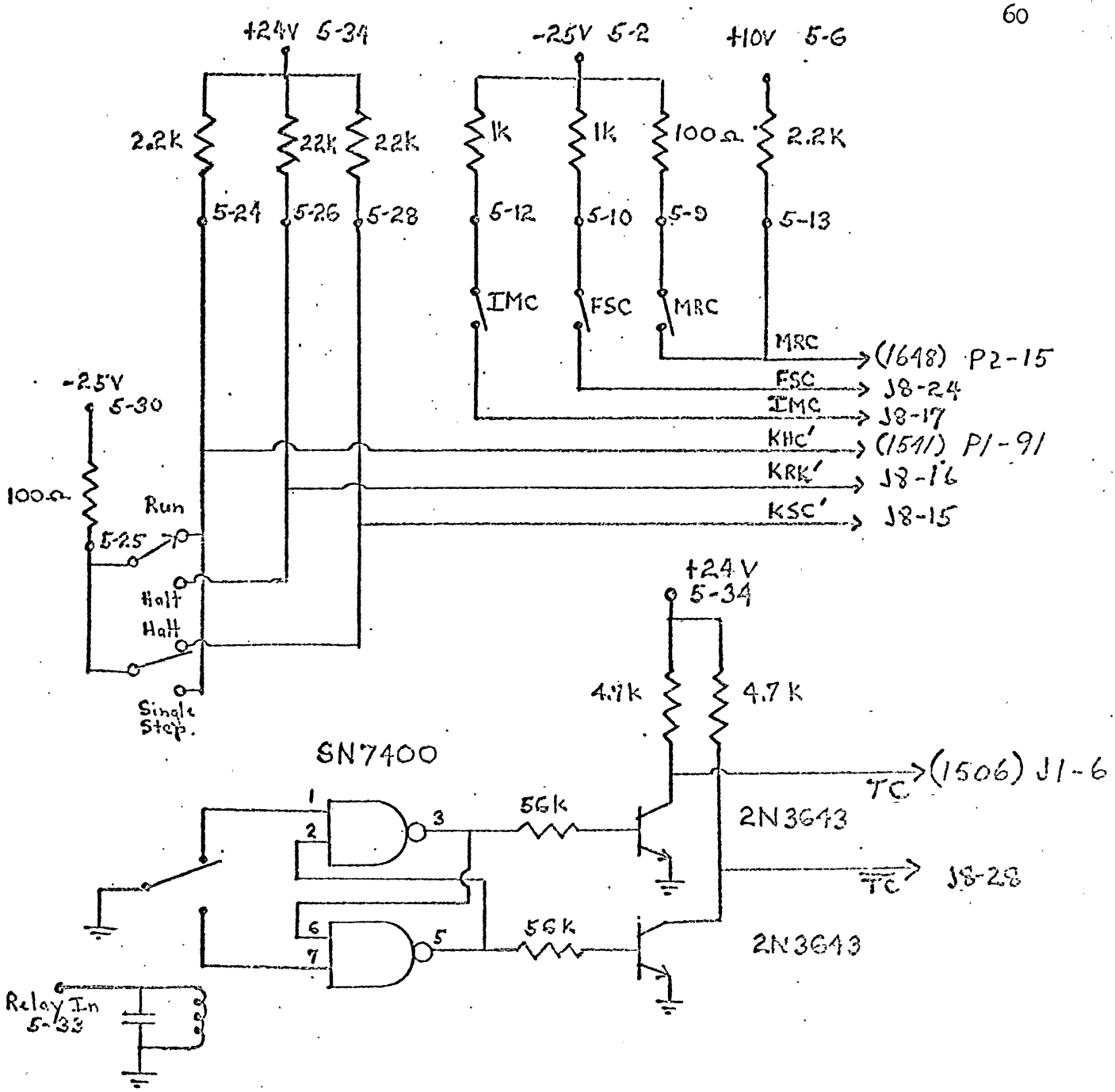
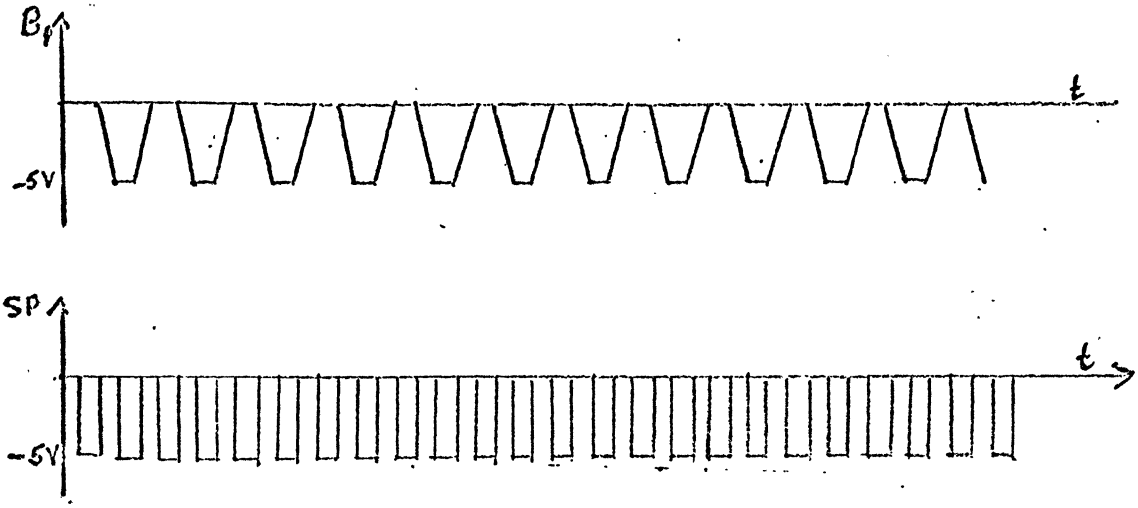


Figure 2: Main Switching Network

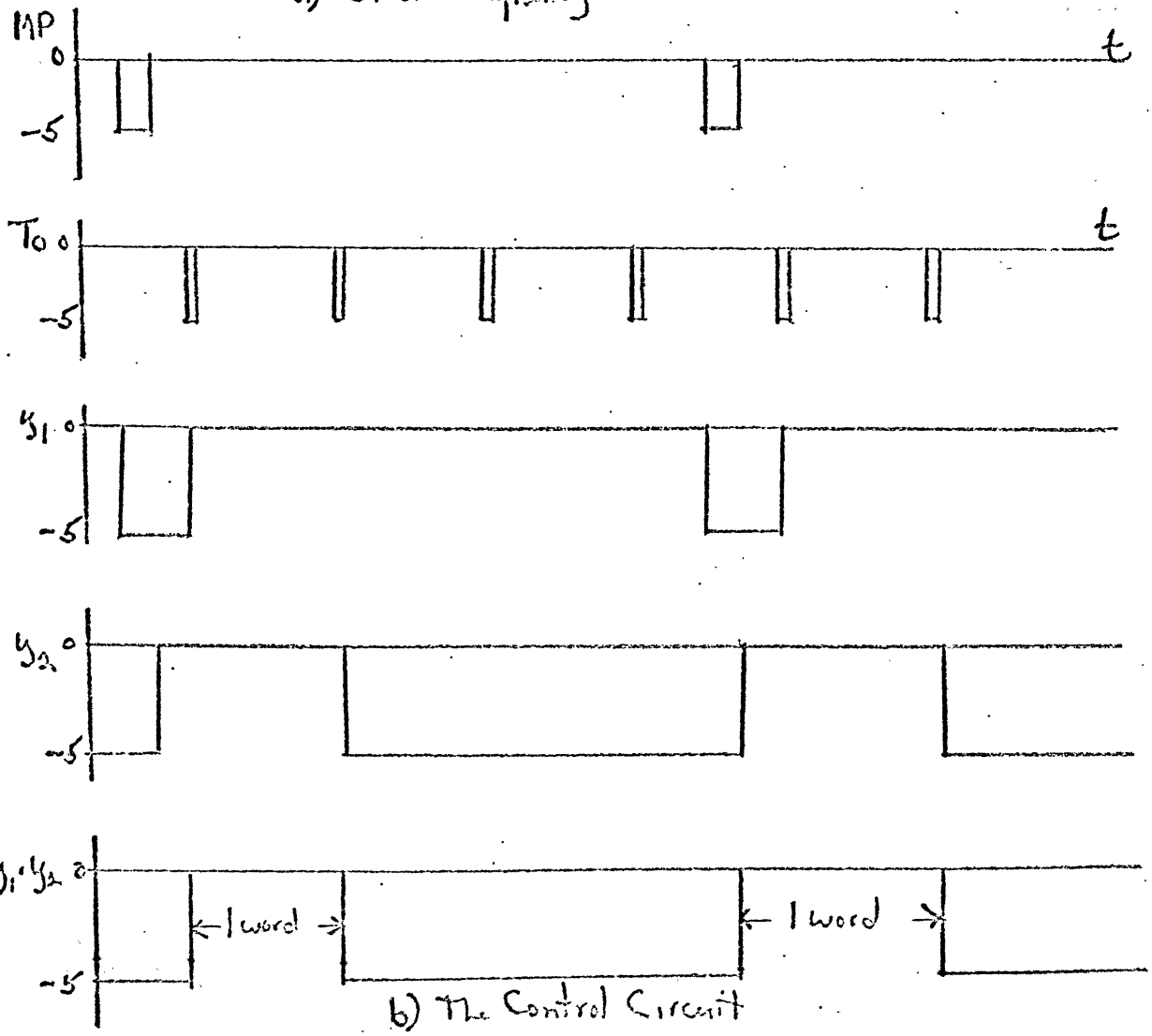


Note: ALL Connections to J8 Must be Made Up IN a New connector And Brought externally Through New Cable.

Figure 3 Switching Control



a) Clock Frequency Doubler



b) The Control Circuit

Figure 4 Timing for Shift Pulse Generator.

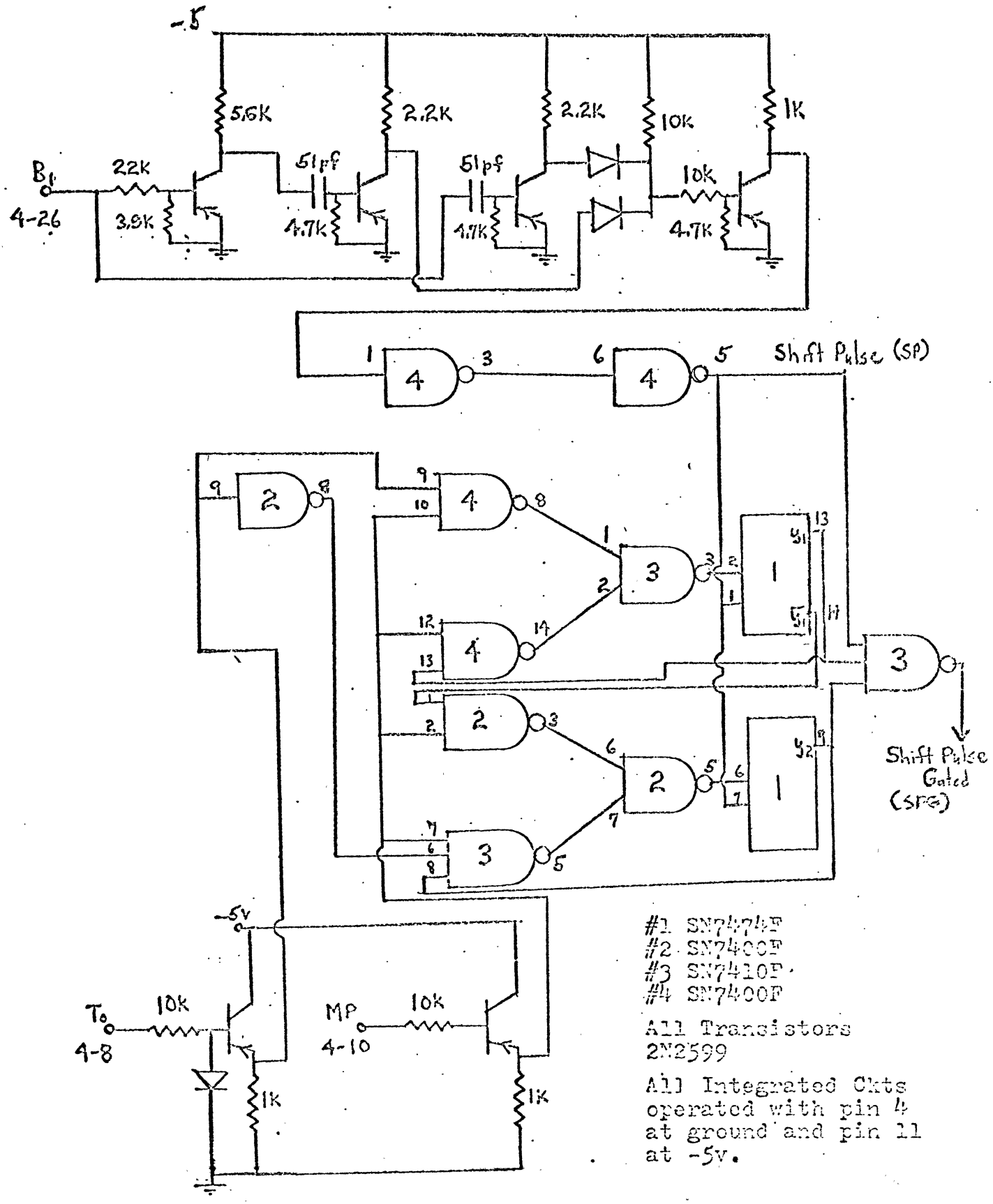
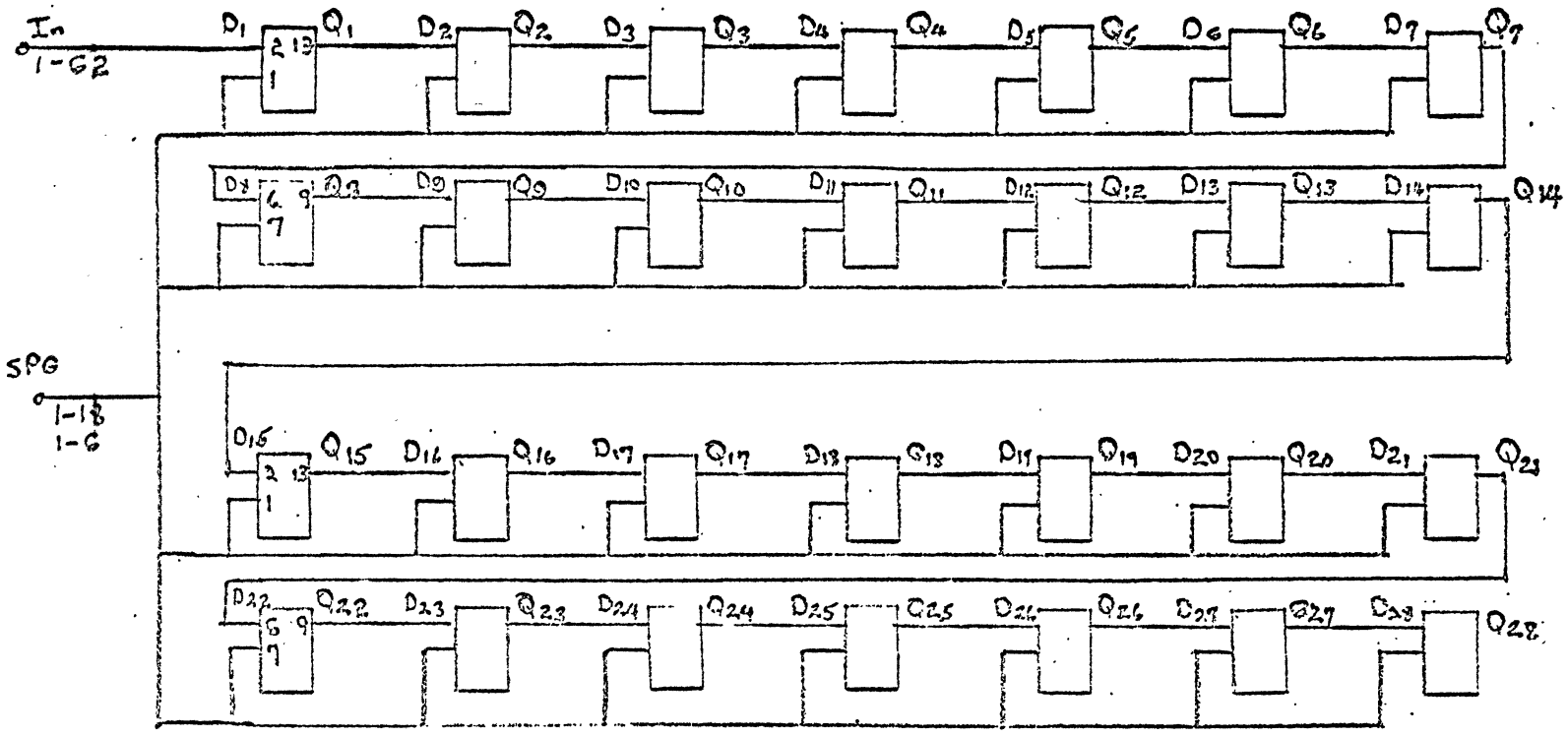


Figure 5 Shift Pulse Generator



All Integrated Ckts SN7474F operated with pin 4 at ground and pin 11 at -5v.

Figure 6. Shift Register Card.

Connections to J1

J1(100)	Wire #		Connected To	Function
1	1501		P7-1	I_1
2	1502		P7-2	I_2
3	1503		P7-3	I_3
4	1504		P7-4	I_4
5	1505		P7-5	I_5
6	1506		P7-6	I_6
7	1507		P7-7	Precision Time Puls
8	1508		P6-31	
9	1509		P6-19	SC_{10}
10	1510		P6-20	SC_{20}
11	1511		P6-21	SC_{30}
12	1512		P6-22	SC_{40}
13	1513		P6-25	PVEC
14	1514		P6-23	SC_{50}
15	1515		P6-24	SC_{TO}
16	{1516, 1517}		E5→CR4	
17	{1518, 1519}		TB4-6	
18	1520		E6→CR1	
19	1521		TB4-7→	
20				
21				
22	1524		anode CR3	
23	1525		P2-10	Dd
24	1526		E4	
25	1527		TB4-22	
26	1722	white	P1-N	
27	1722	red	P1-P	
28	1722	green	P1-R	
29	1722		P1-S	
30	1721	black	P1-j	
31	1721	white	P1-k	

J1(100)	Wire #		Connected to
32	1721	red	P1-m
33	1721	green	P1-n
34	1721	orange	P1-p
35	1721	blue	P1-r
36	1522		P2-13
37	1523		P2-23
38			
39			
40	1546		P1-J
41	1720		P1-L
42			
43			
44			
45			
46	1722	black	P1-K
47	1720	black	P1-M
48	1549	white	P2-3
49	1549	black	P2-2
50	1528	white	}
51	1528	black	
52	1720	red	P1-c
53			
54	1554		TB4-5
55	1555	white	
56	1555	black	
57	1556		P2-9
58	1557		P2-16
59	1558		P2-8
60			
61			
62			
63			
64			
65			
66			

J1(100)	Wire #	Connected to	Function
67	1559	P2-17	
68	1683	P2-4	
69			
70			
71			
72			
73			
74			
75			
76			
77			
78			
79			
80			
81			
82			
83	1563	J1-84	
84	1563	J1-83	
85	1544	P5-19	
86	1545	P5-18	
87	1652	P5-37	
88			
89			
90	1560	P2-22	M_{rc}
91	1541	P7-17	K_{HC}
92			
93	1562	P2-12	E_{WC}
94	1542	P7-13	V_{6C} Discrete Input
95	1543	P7-12	V_{5C} Discrete Input
96	1537	P7-8	X1C Discrete Input
97	1538	P7-9	X2C Discrete Input
98	1539	P7-10	X3C Discrete Input
99	1540	P7-11	X4C Discrete Input
100			

J3 (100)	Wire #	Connected to
1	1580	TB4-3
2	1581	TB4-6
3	1610	TB3-15
4	1601 red	P7-22
5	1601 white	P7-27
6	1601 black	P6-17
7	1638	P2-6
8	1604	P6-1
9	1604	P6-2
10	1600	P6-40
11	1600	P6-41
12	1585	(TB2)
13	1585	(TB2)
14	1609	TB3-6
15	1602 red	P6-27
16	1602 white	P6-16
17	1602 black	P6-15
18	1618	P6-10
19	1599	P6-46
20	1599	P6-47
21	1598	P6-35
22	1598	P6-36
23	1586	TB3-8
24	1608	TB3-7
27	1603	P7-35
28	1603	P6-14
29	1603	P6-13
30	shield ground	
31	1594	J4-1
32	1595	J4-2
33	1596	J4-3
34	1597	J4-4
35	1583	chassis ground
36	1606-1640	TB3-5
38	shield ground	

J3(100)	Wire #	Connected to
39	1731	J4-5
40	1732	J4-6
41	1733	J4-7
42	1734	J4-8
43	1584	chassis ground
44	1725	J4-16
45	1725	J4-17
46	1591	P6-37
47	1591	P6-38
48	1617	P6-9
49	1582	TB3-21
50	1605-1640	TB3-5
51	1639-1676	TB3-3
52	1592	P6-48
53	1592	P6-49
54	1607-1640	TB3-5
55	1726	J4-18
56	1727	J4-19
58	1593	P6-42
59	1593	P6-43
60	1632	TB3-14
61	1633	TB3-13
63	1615	P6-8
64	1588	P6-6
65	1589	P6-11
66	1590	P6-12
67	1680	P7-24
68	1631	TB3-16
69	1634	TB3-17
71	1622	TB3-10
72	1730	J4-15
73	1611	(TB-2)
74	1627	P2-19
76	1616	P7-26

J3 (100)	Wire #	Connected to
77	1619	P6-38
78	1619	P6-39
79	shield ground	
80	1635	P7-21
81	1636	P2-20
82	1637	P2-2
83	1729	J4-14
84	1629	TB3-9
85	1624	P7-19
86	1624	P7-37
87	1620	P6-50
88	1620	P6-33
90	1737	J4-9
91	1738	J4-10
92	1739	J4-11
93	1740	J4-12
94	1728	J4-13
95	1628	TB3-11
96	1623	P7-32
97	1623	P7-31
98	1621	P6-44
99	1621	P6-45
100	1612	P6-7

J3(50)	Connected to	Function
1	A28-$\overline{c}$	$B_1(1)$
2	A28-$\overline{M}$	B_2
3	A28-1	B_3
4	A28-T	B_4
5	A28-11	B_5
6	A28-30	B_6
7	A28-$\overline{F}$	$B_1(0)$
8	A28-$\overline{P}$	$B_2(0)$
9	A28-B	$B_3(0)$
10	A28-W	$B_4(0)$
11	A28-R	$B_5(0)$
12	A28-$\overline{K}$	$B_6(0)$
13	A34-$\overline{M}$	j
14	A34-D	k
15		
16	A71-$\overline{M}$	s
17	A43-V	15
18	A70-14	data
19	A61-5	
20	A63-37	
21	A59-J	L_x
22	A59-11	N_c
23	A34-$\overline{V}$	A_c
24	A30-37	I_c
25	A27-$\overline{u}$	
26	A59-T	L_c
27	A70-V	
28	A54-26	
29	A70-19	
30	A70-W	
31	A70-23	
32	A70-10	
33	A70-13	

J3(50)	Connected to	Function
34	A22-1	F_c
35	A58-J	V_c
36	A30-$\overline{M}$	R_c
37	A34-30	D
38	A34-J	E
39	A28-J	Q
40	A22-D	N_p
41	A34-$\overline{c}$	A_p
42	A22-J	I_p
43	A59-$\overline{M}$	L_p
44	A34-37	A_{24}
45	A34-12	
46	A71-30	
47	A71-20	
48	A28-37	
49	A28-D	
50	A28-J	

J4 (50)	Connected to	Function
1	A26-37	C_{B_1}
2	A26-30	C_{o_2}
3	A26-D	C_{B_3}
4	A26-1	C_{B_4}
5	A26-T	C_{B_5}
6	A30-T	C_1
7	A30-$\overline{V}$	C_2
8	A30-J	C_3
9	A30-1	C_4
10	A30-11	C_5
11	A22-37	0_1
12	A22-T	0_2
13	A22-$\overline{c}$	0_3
14	A22-$\overline{M}$	0_4
15	A23-$\overline{N}$	
16		
17	A38-D	
18	(A26-J)	C_{P_1}
19	A26-$\overline{C}$	C_{P_2}
20	A26-$\overline{M}$	C_{P_3}
21	A26-11	C_{P_4}
22	A26-J	C_{P_5}
23	A58-11	S_1
24	A58-37	S_2
25	A58-$\overline{V}$	S_3
26	A59-$\overline{C}$	S_{B_1}
27	A59-D	S_{B_2}
28	A59-1	S_{B_3}
29	A59-37	$0B_1$
30	A59-30	$0B_2$
31	A59-$\overline{V}$	$0B_3$
32	A34-1	N_D
33	A34-T	I_p

J4 (50)	Connected to	Function
34	A22-$\overline{V}$	P_1
35	A22-11	P_2
36	A22-30	P_3
37	A30-30	R_k
38	A30-D	R_s
39	A30-$\overline{c}$	R_T
40	A58-1	V_k
41	A58-D	V_s
42	A58-$\overline{c}$	W_a
43	A58-T	W_B
44	A58-30	Z_1
45	A58-$\overline{M}$	Z_2
46	A71-$\overline{V}$	J_T
47	A38-J	D_c
48	A21-40, A72-38, A24-$\overline{R}$ & A31-35	
49	A57-8	
50	A57-$\overline{E}$	

J11(50)	Connected to	Function
1	A38-$\overline{W}$	D_1
2	A38-$\overline{M}$	D_2
3	A38-31	D_3
4	A38-38	D_4
5	A38-1	D_5
6	A38-11	G_1
7	A38-$\overline{C}$	G_2
8	A38-T	G_3
9	A40-1	V_{11}
10	A40-D	V_{12}
11	A40-J	V_{13}
12	A71-$\overline{C}$	V_{14}
13	A71-1	V_{15}
14	A71-D	V_{16}
15		
16	A71-J	V_{17}
17	A71-11	V_{18}
18	A40-$\overline{C}$	V_{21}
19	A40-T	V_{22}
20	A40-11	V_{23}
21	A73-37	V_{24}
22	A73-T	V_{25}
23	A73-$\overline{C}$	V_{26}
24	A73-$\overline{M}$	V_{27}
25	A73-$\overline{W}$	V_{28}
26	A40-30	V_{31}
27	A40-$\overline{M}$	V_{32}
28	A40-37	V_{33}
29	A73-1	V_{34}
30	A73-D	V_{35}
31	A73-J	V_{36}
32	A73-11	V_{37}

J11(50)	Connected to	Function
33	A73-30	V_{38}
34	A61-7	10
35	A61-33	10
36	A63-17	0
37	A63-27	10
38	A63-28	10
39	A63-$\overline{F}$	10
40	A63-Z	10
41	A63-$\overline{c}$	10
42	A63-$\overline{E}$	10
43	A63-42	10
44	A69-33	10
45	A65-33	10
46	A65-$\overline{R}$	
47	A62-18	
48	A62-$\overline{E}$	
49	A62-J	
50	A62-$\overline{R}$	

P7	Wire No.	Connected To:	Function
1	1501	J1-1	I_1
2	1502	J1-2	I_2
3	1503	J1-3	I_3
4	1504	J1-4	I_4
5	1505	J1-5	I_5
6	1506	J1-6	T_c
7	1507	J1-7	Precision Time Pulse
8	1537	J1-96	X1C Discrete Input
9	1538	J1-97	X2C Discrete Input
10	1539	J1-98	X3C Discrete Input
11	1540	J1-99	X4C Discrete Input
12	1543	J1-95	V5C Discrete Input
13	1542	J1-94	V6C Discrete Input
14	1647	P2-5	
15	1648	P2-15	
16	1649	P2-6	E_{wc}
17	1541	J1-91	K_{HC}
18	Blank		
19	1624	J3-85	
20		TB1-1 (Blank)	
21	1635	J3-80	
22	1601	J3-4	
23		TB1-4 (Blank)	
24	1680	J3-67	
25	1723	J2-3	
26	1616	J3-76	
27	1601W	J3-5	
28	1567	J2-4	
29	1569	J2-6	
30	1724	J2-7	
31	1623	J3-97	
32	1623	J3-96	
33		TB1-14 (Blank)	
34	Blank		
35			
36			
37	1624	J3-86	