REV.	ZONE	ECO#	REVISION	APPD	DATE
A		R1416	PRODUCTION RELEASE		
A		R2162	RECORD CHANGE MT 8-9-90		

NOTE:
MANUFACTURERS RECEIVING APPLE APPROVED VENDOR STATUS FOR THEIR PRODUCT UNDER THIS PART NUMBER PLEASE NOTE: You must not change your part design, materials or manufacturing process from those used for the original samples submitted to and approved by Apple without written approval of Apple. Proposed changes determined by Apple to be significant, will require the manufacturer to submit new samples and/or data for review and approval prior to product shipments to Apple.

	METRIC				Apple Computer, Inc.	
DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS IN BRACKETS [ ] ARE IN INCHES. TOLERANCES X.X ± 0.3 [.01] X.XX ± 0.13 [.005] X.XXX ± 0.03 [.001] ANGLEs ± 0.1 or as noted DO NOT SCALE DRAWING	DRAFT M.T.	12/7/88	DESIGN CK S.R.	12/8/88	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: (i) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE (ii) NOT TO REPRODUCE OR COPY IT (iii) NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART	
	ENG APPD D.I.	12/12/88	MFG APPD A.A.	1/31/89		
	QA APPD	/ /	DESIGNER	/ /	TITLE IC, CUSTOM, TFB2.2 144-QFP	
	RELEASE D.B.	2/3/89	SCALE NONE			
	MATERIAL/FINISH NOTED AS APPLICABLE		SIZE A		DRAWING NUMBER 343S0077-A	SHT 1/30

1.0 SCOPE:

This specifies the parametric requirements of TFB2.2. The TFB2.2 is designed to interface with NuBus, to sense what monitor is used, and generate the corresponding monitor timing, video RAM timing, control and video data for Color look-up table. It is packaged in a 144 pin plastic square quad flat pack.
The TFB2.2 is designed to replace Apple P/N 343S0019 (TFB2.0) The main difference between TFB2.2 and TFB2.0 are as follow:

1. TFB2.2 extend the enable outputs of AD8, AD9, AD10, AD11 (pin 49, 50, 51, and 52) by 25 ns.
2. TFB2.2 support the NuBus Block Move Access, it effects /ACK, /TM1, and /TM0 (pin 43, 53, and 45).
3. TFB2.2 support 1bit/pxl and 2bit/pxl modes, it presents the correct data on the CA Bus (pin 118-125, 128-135).

Note: A copy of TFB2.2 schematic is on file in Documentation for Apple Internal use only. Do not remove the original schematic 062-0071 from Documentation files.

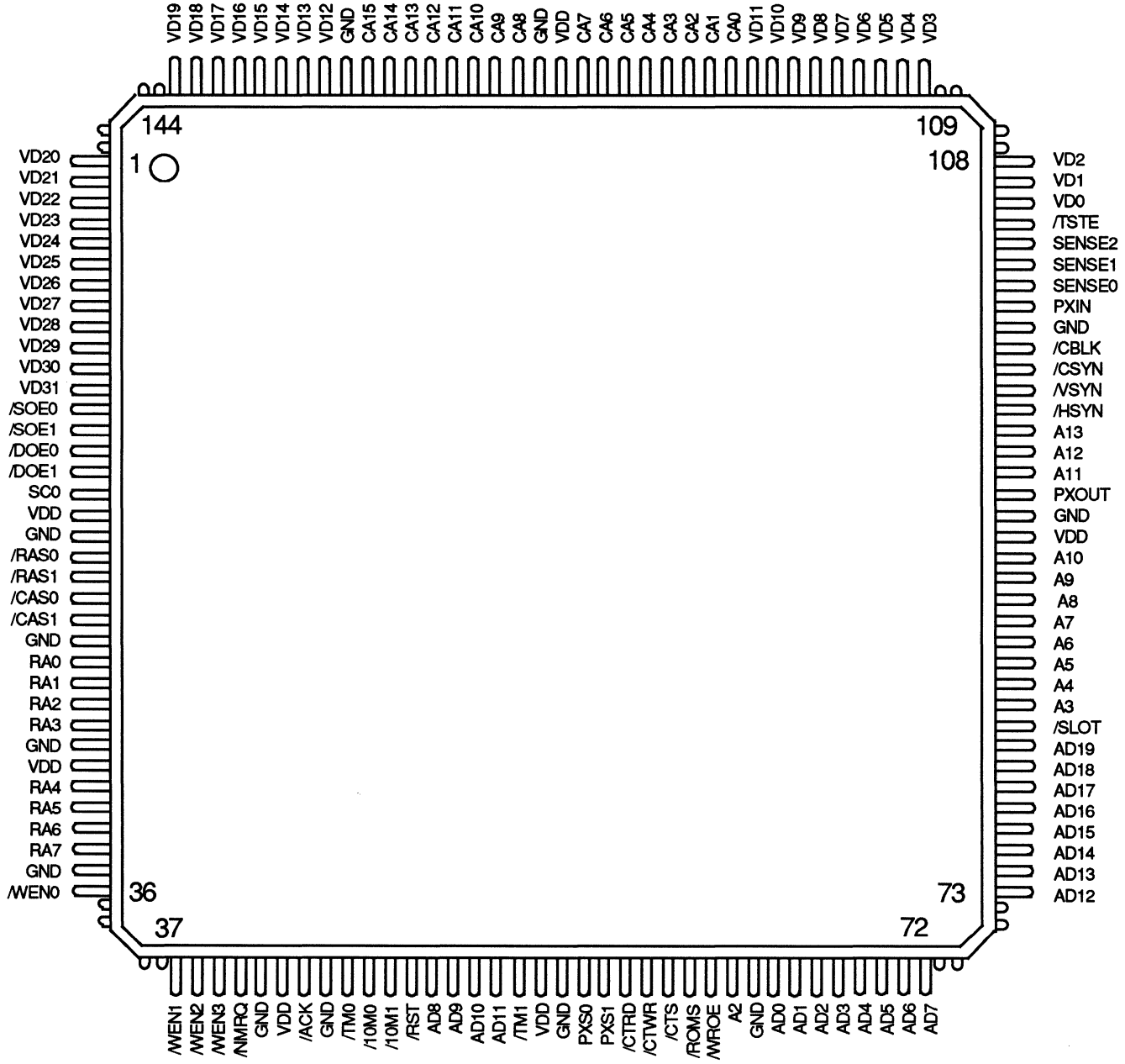


FIGURE 1. PIN CONFIGURATION

1.1 PIN DESCRIPTION

INPUTS		
PIN NAME	**PIN #**	**DESCRIPTION**
/10M0	46	Nubus 10 MHz clock.
/10M1	47	Nubus10MHz signal delayed 50ns.
/RESET	48	Reset pin for TFB2.
AD(7:0)	72-65	Address Data signals from the Nubus.
AD(19:12)	80-73	Address Data signals from the Nubus.
/SLOTSEL	81	Nubus Slot select signal
PXIN	101	Pixel clock input
SENSE(2:0)	104-102	Monitor encoding signals.
VD(31:0)	12-1,144-137, 117-106	Serial data outputs of the VRAMs that connect directly to the TFB2.
/TESTEN	105	When asserted, puts the TFB2 into test mode.
BIDIRECT		
/ACK	43	Nubus acknowlege signal.
/TM0	45	Nubus /TM0 signal.
/TM1	53	Nubus /TM0 signal.
AD(11:8)	52-49	Address Data signals from the Nubus. AD(11:8) provide bits to read the state of the SENSE pins and the internal vertical blank signal. SENSE (2:0) lines are placed on AD(10:8) and the vertical blank signal is placed on AD11 when a color table read access is made to the chip.
/HSYNC	96	Horizontal sync signal. /HSYNC is bidirectional so that the TFB2 can synchronize to an external video source.
/VSYNC	97	Vertical sync signal. /VSYNC is bidirectional to allow genlocking.
OUTPUTS		
/NMRQ	40	Nubus non master request signal.
PXS(1:0)	57,56	Mux selects for desired pixel clock.
/CTRD	58	Color Table read control signal.
/CTWR	59	Color table write control signal.
/CTS	60	Color table select signal.
/ROMSEL	61	Select and output enable signal for the configuration ROM.
/WROE	62	This signal determines the direction of the buffer of the AD bus from the Nubus.
A(13:2)	95-93,89-82,63	These signals are the latched addresses from the AD bus.
RAS(1:0)	21,20	Row address strobes for each bank of RAM.
CAS(1:0)	23,22	Column address strobes for each bank of RAM.
DOE(1:0)	16,15	Data output enable signals for each bank of RAM.
WEN(3:0)	39-36	Enable signals for each byte lane of the RAM.
SCLK	17	SCLK clocks the video data from the RAMs to the TFB2.
SOE(1:0)	14,13	SOE selects which bank is to put its data onto the VD pins of the TFB2.
RA(7:0)	34-31,28-25	8-bit RAM address buss.
PXOUT	92	This is a delayed version of the PIXIN input.
/CBLANK	99	RS170 compatible composite blank signal.
PXD(15:0)	135-128,125-118	16-bit Pixel data buss.
/CSYNC	98	RS170 compatible composite sync signal.

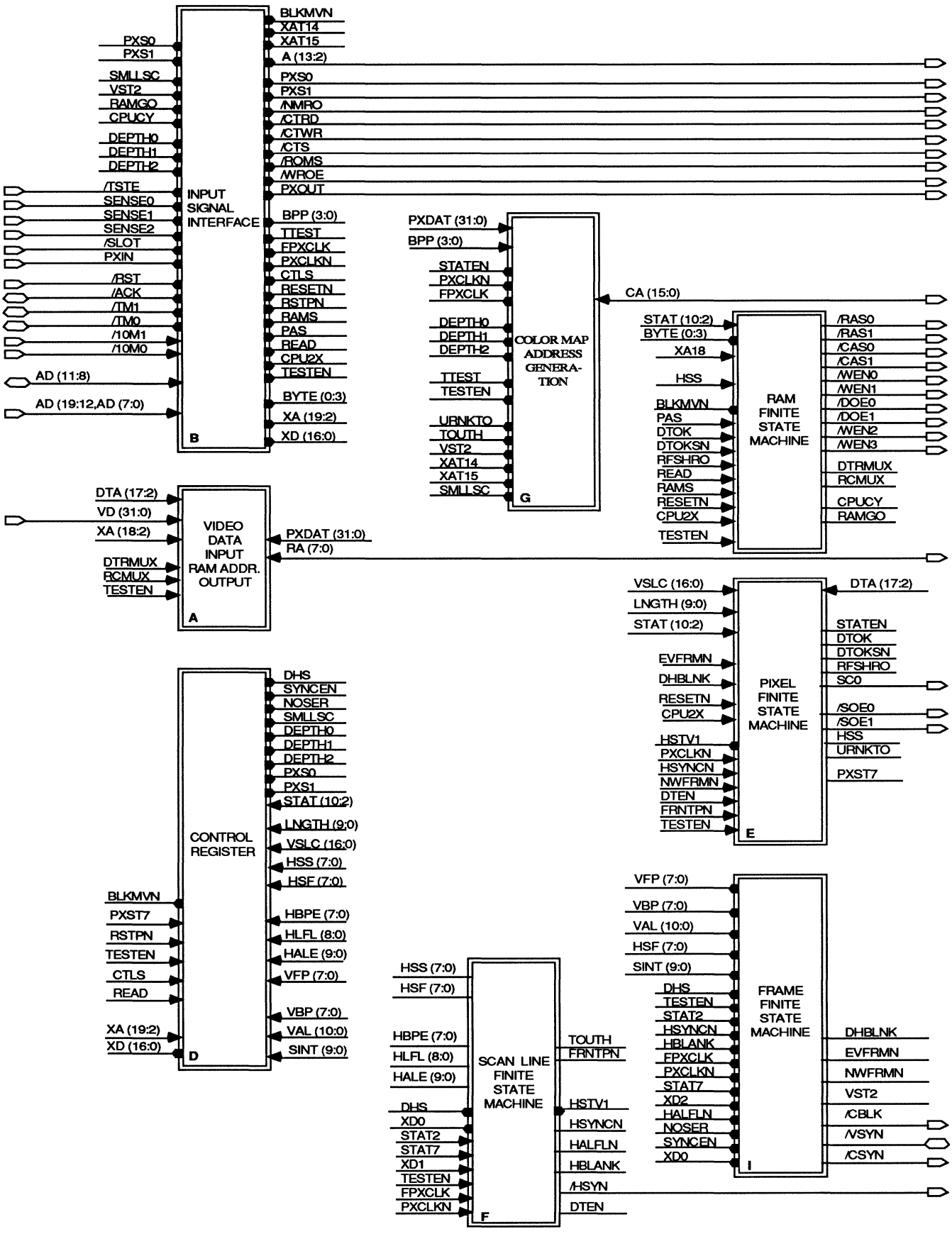


FIGURE 2. TFB2.2 BLOCK DIAGRAM

Apple Computer, Inc.	SIZE	DRAWING NUMBER 343S0077-A
	SCALE	SHT 4 OF 30

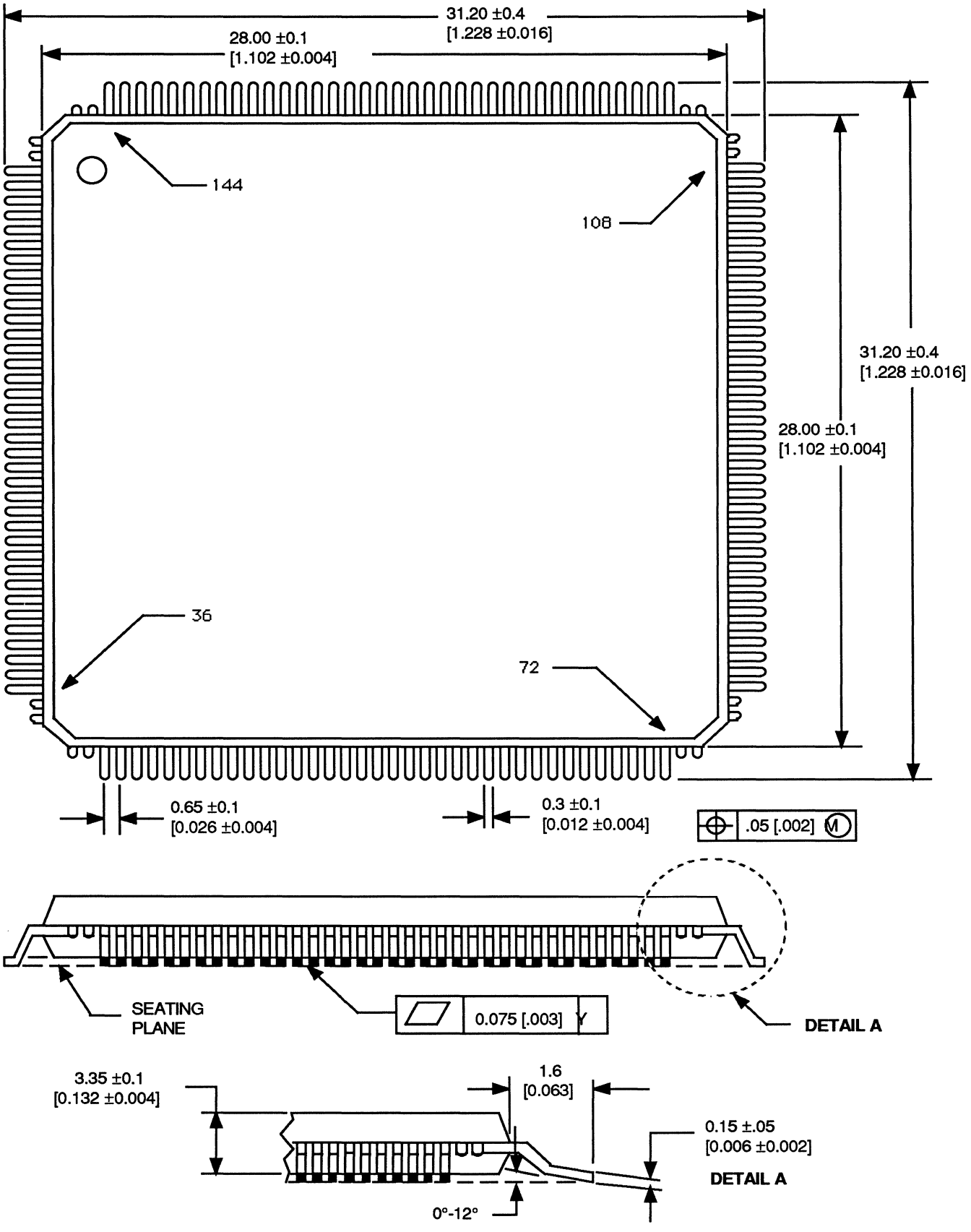


FIGURE 3. DIMENSIONS, VERSION 1

Apple Computer, Inc.	SIZE	DRAWING NUMBER 343S0077-A
	SCALE	SHT 5 OF 30

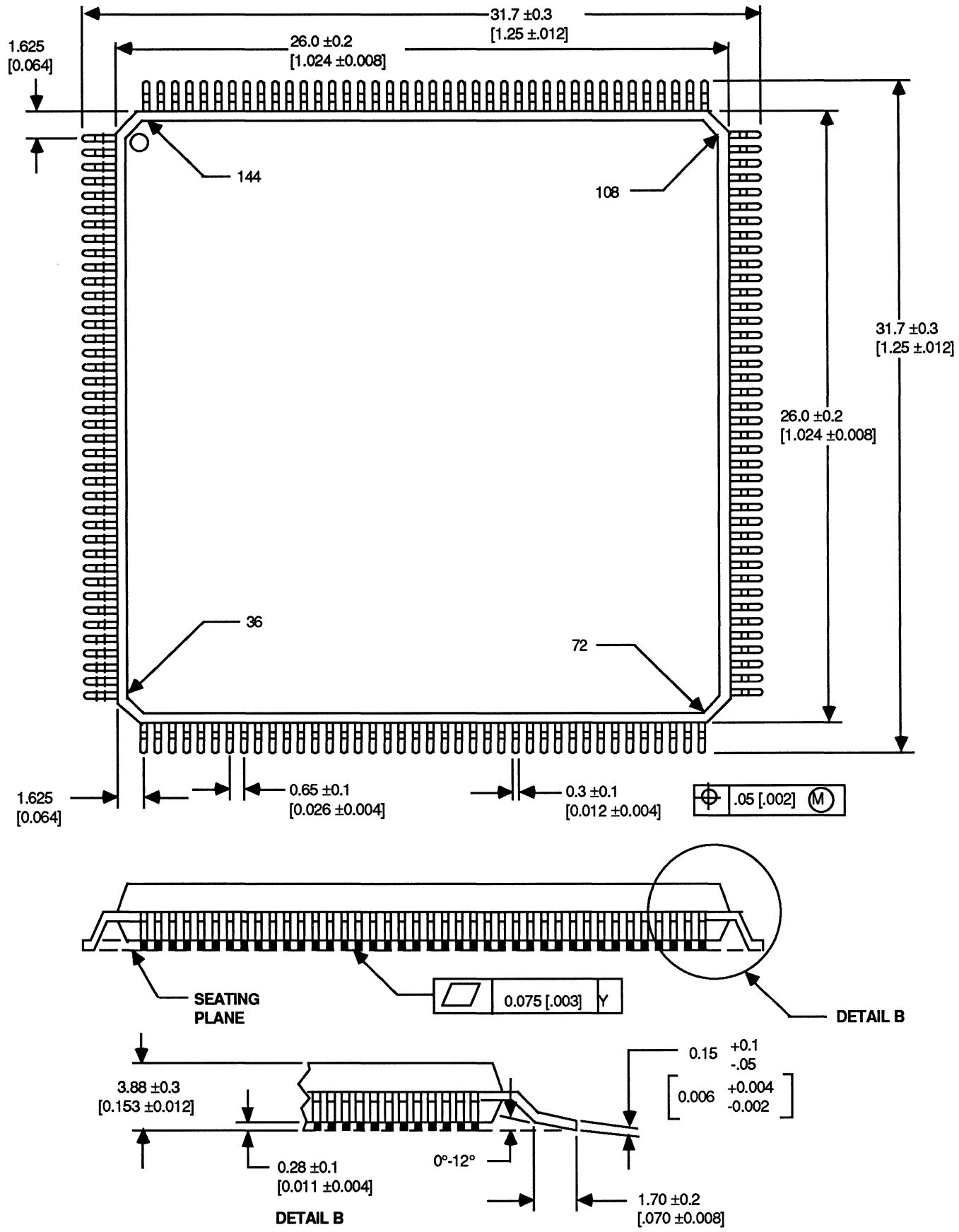


FIGURE 3. DIMENSIONS, VERSION 2

2.0 APPLICABLE DOCUMENTS:

MIL-STD-202 Test methods for Electronic Component Parts.
MIL-STD-883 Test methods and procedures for Micro Electronics.

3.0 REQUIREMENTS:

3.1 PHYSICAL:

3.1.1 PACKAGE: Void free plastic 144 pin Quad Flat Pack (QFP-144). See Figure 3 for dimensions and Figure 1 for pin configuration.

3.1.2 SOLDERABILITY: Contacts shall be solderable per MIL-STD-202, Method 208.

3.1.3 MARKINGS: Manufacturer's name or industry recognized logo, Apple P/N (344S0077), current revision level, mask symbol, copyright symbol, year, "Apple" name or logo, and date code.

EXAMPLE: 343S0077-A
Ⓜ Ⓒ 88 Apple
XXXX

3.2 ELECTRICAL:

3.2.1 ELECTROSTATIC DISCHARGE SENSITIVITY: The minumum electrostatic discharge voltage per pin is ±2000 volts as specified in MIL-STD-883C, method 3015.3 (i.e., C = 100pF; R = 1.5Ω).

3.2.2 LATCHUP TEST: The minimum latchup current for all pins except ground is 50mA in both positive and negative directions. This applies to full temperature and power supply ranges.

3.2.3 ABSOLUTE MAXIMUM RATINGS: Per Table 1.

3.2.4 STATIC PARAMETERS: Per Table 2.

3.2.5 DYNAMIC PARAMETERS: Per Tables 3, 4.

3.3 ENVIRONMENTAL:

3.3.1 RESISTANCE TO SOLDERING HEAT: 260°C for 10 sec in molten solder after 218°C for 30 sec. in vapor phase, 60/40 solder and 260°C for 10 sec in molten solder after 240°C for 30 sec in I.R., 60/40 solder. Rate of temperature rise is 3°C/sec to within 100°C of the final temperature.

4.0 QUALITY ASSURANCE PROVISIONS: Parts shall be inspected to assure compliance to the requirements of this document.

5.0 PACKAGING: Parts shall be packaged according to the vendor's normal commercial practices for safe delivery at Apple Computer or Apple designated contractor.

TABLE 1 . ABSOLUTE MAXIMUM RATINGS

Supply Voltage:	-.3 to +7 .0V
Input Voltage:	-.3 to VDD +.3V
Operating Temperature Range:	TA = 0 to 70°C
Storage Temperature Range:	Tstg = -40° to +125°C

TABLE 2 . DC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
I DD	Quiescent Current	VDD = 5.25		200	µA
VIH	Input High Voltage	All Inputs	2.0		Volts
VIL	Input Low Voltage	All Inputs		0.8	Volts
I I	Input Current	VI = VDD or 0V	-200		µA
IOZ	Output High-Z Current	VO = VDD or 0V	-10	+10	µA
/DOE0, /DOE1, ESC0, /RAS0, /RAS1, /CAS0, /CAS1, RA(0-7)					
IOL	Output Low Current	VOL = 0.4V	8.0		mA
IOH	Output High Current	VOH = VDD - 0.4V		-8.0	mA
/ACK, /TM0, /TM1					
IOL	Output Low Current	VOL = 0.4V	16		mA
IOH	Output High Current	VOH = VDD - 0.4V		-16	mA
All other outputs					
IOL	Output Low Current	VOL = 0.4V	4.0		mA
IOH	Output High Current	VOH = VDD - 0.4V		-4.0	mA

TABLE 3 . AC CHARACTERISTICS
Capacitance: FO = 1MHz, TA = 0° to 70°C

SYMBOL	PARAMETER	CONDITIONS	MAX	UNITS
CIN	Input Capacitance		10	pF
COUT	Output Capacitance	Unmeasured pins	10	pF
CI/O	Bidirectional Capacitance	returned to GND	15	pF

TABLE 4. DYNAMIC PARAMETERS SPECIFICATIONS

NUM	DESCRIPTION	MIN	MAX	UNIT	FIG.
1	NuClk to /10M0	85	95	ns	4,5
2	NuClk to /10M1	35	45		
3	/Slot_Sel to /10M0 hold time	10	-		
4	/Slot_Sel to /10M1 setup time	10	-		
5	/10M0 rising to /TM0,1, /ACK asserted	15	40		
6	/10M0 rising to /TM0,1, /ACK negated	15	40		
7	/10M1 falling to /RAS asserted	-	40		
8	/10M1 falling to /CAS asserted	-	30		
9	/10M* falling to /RAS, /CAS, /DTOE negated	_	30		
10	RADD & /WEN* hold time after /RAS	50	-		
11	RADD & /WEN* setup time to /CAS	10	-		
12	/10M0 rising to /CT_SEL, /ROMSEL asserted	-	40		6,7
13	/10M0 rising to /CT_SEL, /ROMSEL negated A(13:2) invalid	-	40		
14	/CBLANK, CSYNC, /HSYNC, /VSYNC, CMA setup time to /PCLKOUT falling edge	10	-		8
15	/CBLANK, CSYNC, /HSYNC, /VSYNC, CMA hold time after /PCLKOUT falling edge	10	-		

6.0 SUPPLEMENTARY INFORMATION:

6.1.0 Features:

The most significant features of the TFB2.2 are:

- Latched addresses for the configuration ROM.
- Support for sensing what monitor is connected to the video card.
- The ability to disable sync generation on the /CSYNC output.
- The ability to remove serration and equalizing pulses from the /CSYNC output.
- Datapath additions to provide support for the Bt454.
- RAM interface that allows arbitrary non power of two rowbytes.
- The TFB2.2 can support 100MHz video.

6.1.1 System Interface

The TFB2.2 is optimized to be interfaced with the NuBus found on the Macintosh II. The TFB2.2 provides a direct connection to most of the NuBus control signals and provides all of the control signals needed by the rest of the video card. A block diagram for a typical video system is given below:

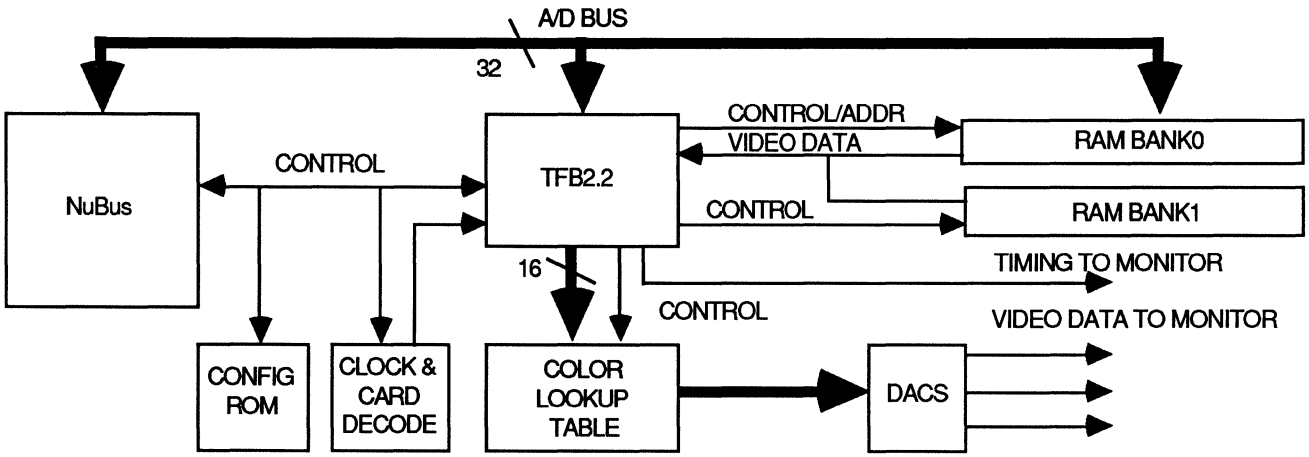


FIGURE 9

The graphics system above consists of eight major blocks:

The TFB2.2 is optimized for a NuBus interface. The chip latches the addresses at the start of the cycle. It inverts the sense of the address bus to account for NuBus and it provides control signals compatible with NuBus operation.

The TFB2.2 latches 12 address bits and provides a select for, the configuration ROM required by NuBus.

The TFB2.2 requires a slot select signal which is derived from a comparator of the NuBus slot ID and NuBus address bits 31:28 with NuBus address bits 27:24 and ground respectively.

The NuBus requires the ability to provide very high current drivers for the A/D bus, so the A/D bus must be buffered onto the card.

The frame buffer memory will support either 256K or 512K bytes of dynamic RAM consisting of the NEC 256K bit video RAMs. By having a built-in shift-register and a separate serial port for video data, these RAMs allow up to 97% of the frame buffer memory bandwidth to be available to the processor.

No parity is provided for the frame buffer RAM. Since the parts are organized by four, 8 are required to fill out a 32-bit bus. Up to two ranks of memory can be accessed to yield a maximum RAM configuration of 512K bytes.

The color lookup table shown in the block diagram is needed for color systems. Several integrated color lookup tables and DACs are now available from various chip manufacturers. The TFB2.2 interfaces easily with the Bt453 and Bt454.

In addition to providing a flexible and inexpensive video solution, the TFB2.2 supports a number of additional features:

- The TFB2.2 will operate with either 60Hz interlaced, RS170/NTSC compatible timing, or with 67Hz non-interlaced timing. PAL and SECAM timing should be achievable given the programable nature of the TFB's sync generation. Almost any non-standard video refresh rate can also be supported.
- Merging of external video source with the frame buffer video stream is supported.
- The TFB2.2 will support a wide range of screen resolutions, pixel depths, and pixel data rates up to 80 MBytes per second, all under software control. Pixel depths of 1, 2, 4, 8 or 16 bits per pixel can be achieved using a single pixel clock, and no external logic. The master pixel clock on the TFB2.2 can be prescaled under software control to support any of these color depths. Pixel clocks up to 40MHz are achievable at 16 bits per pixel. Higher clock speeds can be achieved at shallower pixel depths as long as the 80MBytes per second data rate is not exceeded.

6.2.0 DATA ORGANIZATION

The memory map below shows the layout of the various frame buffer memory spaces, and how they relate to the screen image.

$00000	FRAME BUFFER
$80000	BASE(16:0)
$80004	LENGTH(9:0)
$80008	DLYHS,PXS(1:0),Bt453,SYNCEN,NOSER,DEPTH(2:0),RFSH(2:0),INTRLC,GNLCK,SETUP(2:0)
$8000C	SYNCINTERVAL(9:0)
$80010	VFRONTPORCH(7:0)
$80014	VBACKPORCH(7:0)
$80018	VLINES(10:0)
$8001C	HFRONTPORCH(7:0)
$80020	HSYNCPULSE(7:0)
$80024	HBACKPORCH(7:0)
$80028	HFIRST(8:0)
$8002C	HLAST(9:0)
$80030	SOFTRESET
$90000	CLUT
$A0000	CLEAR VERTICAL INTERRUPT
$D0000	READ /VSYNC STATE,SENSE(2:0)
$F0000	ROM

NuBus SLOT SPACE MEMORY MAP

TABLE 5

The frame buffer memory is a 32 bit wide, 256K-512K byte linear address space in which pixels are organized in a "chunky" manner. That is, a pixel's color value is determined by contiguous bits in memory rather than separate bit planes. The number of longwords of data in a horizontal scan line for the frame buffer is fully programmable, as is the screen's horizontal resolution. Either 256K or 512K byte memory configurations are possible.

The control address space is independent of the RAM data space for the frame buffer. The first 52 bytes of this space are reserved for control registers. Control registers are 8 bits wide, and located at every 4th address in the control space starting at address 1. A complete description of the control registers is given in section 6.3.0.

TFB2.2 provides selects for controlling either the Bt453 or Bt453 CLUT/DAC chip.

It also generates the /NMRQ NuBus dumb interrupt signal directly and will allow clearing of the /VSYNC signal through accesses to the address spaces shown above.

The TFB2.2 allows reading of the state of the VBLANK signal internal to the chip and allows reading of the SENSE lines from the monitor indicating which monitor is connected to the video card.

Finally, the TFB2.2 provides select signals and latches addresses for the configuration ROM.

6.3.0 Control Register Description

A set of 13 control registers in the TFB2.2 provides the parameters determining screen resolution, sync generation, and system configuration required. The original TFB did not have a straight forward register model. TFB2.2 has a slightly less confusing register interface.

All parameters have separate register locations with the exception of several parameters that require only a few bits of definition. These parameters are grouped together in the register at address $80008.

The following is a description of the parameters required to configure the TFB2.2. For each parameter the parameter name is given and a schematic name is given to help in following the TFB2.2 schematic. It should be noted that the addresses given for the parameters are NuBus long word addresses. The 68020 on the Mac II mother board swaps the byte ordering. This will affect the way in which those registers larger than 8 bits get addressed on the Mac II.

6.3.1 System Configuration Parameters

These parameters give global definitions of how and where the pixel data is to be organized, how RAM is to be refreshed, whether the TFB2.2 is running interlaced or non-interlaced and so on.

BASE(16:0) VSLC(16:0)

This parameter gives the offset, in long words, from the base of the frame buffer memory, to the upper leftmost pixel to be displayed. If the frame buffer base is set so high that there is not enough memory to display the full screen, unpredictable data will be displayed after the point at which the 512K barrier is reached. If BASE is set to start in the 2nd rank when the 2nd rank is not present, unpredictable data will be displayed.

LENGTH(9:0) LNGTH(9:0)

This parameter equals rowbytes/4 for the screen width, where rowbytes is defined to be the number of bytes between successively scanned lines. For a byte per pixel, non-interlaced, 640 pixel wide screen, this parameter should be set to $A0 (decimal 160). Notice rowbytes must be divisible by 4. For an interlaced display with these characteristics, this parameter is set to $140 (decimal 320), since interlace displays successively scan every other line.

DLYHS DHS

When HIGH, this bit causes the /HSYNC and /CSYNC signals to be delayed two pixel clock periods to account for the pipeline delay in the CLUT/DAC chip.

PXS(1:0) PXS(1:0)

The state of these two bits is reflected on the PXS output pins on the TFB2.2. They can be used as control inputs to a mux for selecting the desired pixel clock.

Bt453 SMLLSC

When HIGH, this bit causes the CT_/SEL pin to be compatible with the timing required by the Bt453. When LOW, this bit causes the CT_/SEL pin to have timing compatible with the Bt454.

SYNCEN SYNCEN

When HIGH, this bit inhibits the generation of the /CSYNC signal by tying the /CSYNC output low.

NOSER NOSER

When HIGH, this bit inhibits the generation of the equlizing pulses on the /CSYNC pin.

DEPTH(2:0) DEPTH(2:0)

This parameter determines the depth of the pixels which the TFB2.2 is to generate. This parameter will cause the TFB2.2 to prescale the pixel clock, and multiplex the pixel data so as to produce the desired pixel depth. Note that all parameters which are given in pixel times, are given in relation to the scaled pixel clock, and not necessarily the pixel clock fed into the TFB2.2. The pixel depth determined by the DEPTH parameter is given in the table below:

TABLE 6

DEPTH parameter value	Pixel Depth with 453	Pixel Depth with 454
100	1 bit per pixel	
101	2 bits per pixel	
110	4 bits per pixel	
111	8 bits per pixel	
000		4 bits per pixel
001		2 bits per pixel
010		1 bit per pixel
011		Test Mode

It is important that this parameter be initialized before the /SOFTRESET parameter is set HIGH so as to allow time for the pixel clock generation circuitry to stabalize before the TFB2.2 is taken out of reset mode. Refer to Table 4 for a description of how the DEPTH parameter affects the definition of the PIXDAT bus.

RFSH(2:0) STAT(6:4)

This parameter equals the number of RAM refresh cycles to be executed per scan line time. If the TFB2.2 is running with NTSC timing, then the scan lines are 63.56µsec apart. Since RAM must be refreshed every 4000µsec there will be 62.9 scan lines per refresh period. Dividing 256 rows by 62.9 scan lines gives 4.07 rows refreshed per scan line. We round up to 5, so this field should contain a 101B. Unpredictable results will occur if this parameter is set to zero.

INTRLC STAT3

If this bit is set HIGH, then the TFB2.2 runs in interlaced mode; otherwise the TFB2.2 runs in non-interlaced mode. This has implications on how scan line addresses get generated as described below in section 5.2.

GNLCK STAT2

When HIGH, this bit indicates that the horizontal and vertical sync signals are externally generated. When in genlock mode, many of the parameter definitions change. These changes will be outlined in an appendix to this document to be added later. Normally this bit will be set to 0.

SETUP STAT10-8

This 3 bit field determines the time required to synchronize the parts of the TFB2.2 concerned with pixel generation, to the parts of the TFB2.2 concerned with RAM timing. This field is calculated as follows:

SETUP :=($FF-(20 * Trunc((Nubus clock period)/(EffPXCLK period))) DIV 8) - 56

Where the EffPXCLK = (16/depth of pixels)*PXCLK period.

Clearly some black magic is going on here. The operation of this field is described in detail in section 5.2. A full understanding of this equation requires careful study of the chip's schematics and timing, and is probably not worth the effort. Suffice to say that this field is needed to assure proper synchronization between the the pixel generation and RAM control portions of the TFB2.2.

/SOFTRESET STAT7

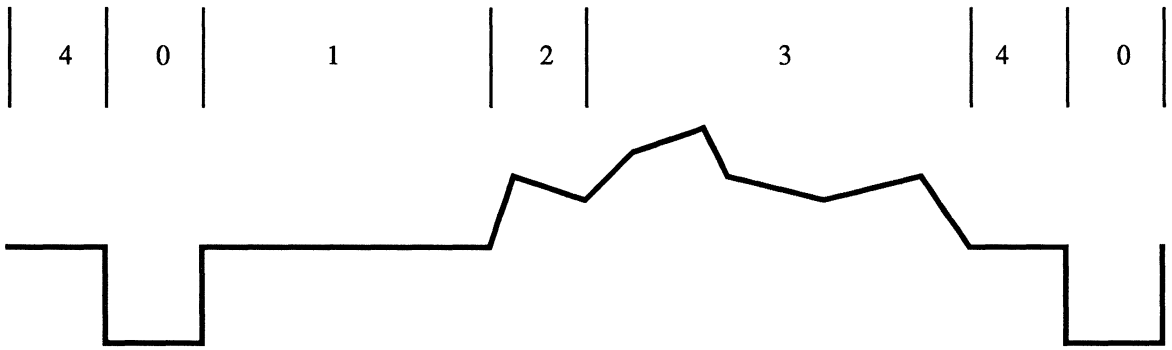
This bit is used to reset the pixel generation circuitry in the TFB2.2. At system reset, this bit is cleared and the pixel generation circuitry of the TFB2.2 enters a reset mode waiting for /SOFTRESET to be set. /SOFTRESET should not be set until all of the configuration parameters are loaded with their proper values. At system reset, all configuration registers but this one are in an unknown state. No RAM refresh will take place until after /SOFTRESET is set.

6.3.2 Horizontal Timing Configuration Parameters

The following seven parameters determine the timing characteristics of a single scan line. The first six parameters set the length of the various regions of the scan line. All region lengths are given in scaled pixel clock periods from the end of the last region. The length of the scaled pixel clock equal to (pixel clock) * 16/(depth in bits per pixel).

Each scan line is broken up into five regions which define the duration of the horizontal front porch, horizontal sync pulse, horizontal back porch, and the region of the horizontal scan line in which active video is displayed. Additionally, these first five parameters must indicate the midpoint of the scan line for use in generating the equalizing pulses found in the RS170 composite sync signal.

The figure below shows each of these regions and gives the parameter name which defines its duration.



0 - HSYNCPULSE + 2 pixel times.
1 - HBACKPORCH + 4 pixel times.
2 - HFIRST +2 pixel times.
3 - HLAST + 2 pixel times.
4 - HFRONTPORCH +2 pixel times

FIGURE 10

HFRONTPORCH HSS(7:0)

This parameter equals two less than the number of scaled pixel clocks from the beginning of region 5 above to the start of the next scan line. This is equal to the length of the horizontal front porch.

HSYNCPULSE HSF(7:0)

This parameter equals two less than the number of scaled pixel clocks defining the duration of the horizontal sync pulse in region 0 above. This parameter also determines the duration of the equalizing pulses found in the RS170 composite sync signal. The equalizing pulses are equal to HSYNCFINISH/2 scaled pixel clock periods.

HBACKPORCH HBPE(7:0)

This parameter equals four less than the length of region 1 above.

HALFLINE HLFL(8:0)

This parameter equals two less than the length of region 3 above. The end of region 3 marks the middle of the scan line as measured from falling edge of HSYNC to falling edge of HSYNC for the next scan line. This "midpoint" determines the time at which the equalizing pulses found in the RS170 composite sync signal are to start.

HPIXELS HALE(9:0)

This parameter equals two less than the length of region 4 above. It is the number of pixels to be displayed from the midpoint of the scan line to the start of the horizontal front porch.

SYNCINTERVAL SINT(9:0)

This parameter has no bearing on the length of the horizontal scan line, but instead is used to determine the duration of the interval between the vertical serrations found in the RS170 composite sync signal. If composite sync is not being used, then this parameter need not be set to anything. A section of the RS170 composite sync signal is shown below:

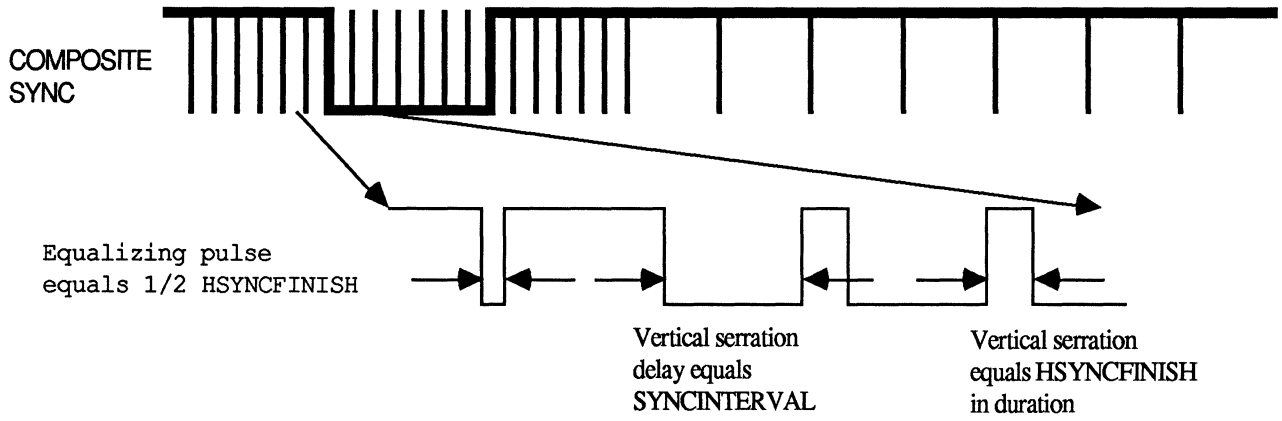


FIGURE 11

The SYNCINTERVAL parameter determines the time from the middle of the scan line to the rising edge of the vertical serration in scaled pixel clock periods.

6.3.3 Vertical Timing Configuration Parameters

The next three parameters define the timing of the vertical sync generation circuitry. The vertical field is broken up into four regions, the duration of which is given by the four parameters below in terms of half scan lines. The four regions determine the vertical front porch, vertical sync pulse width, vertical back porch, and the number of active scan lines to be displayed.

Note that for interlaced displays, the number of half lines in a field must be odd in order to provide an offset from one field to the next. The INTERLACE parameter described earlier impacts address generation. Proper interlace timing still depends on placing interlaced compatible values in the vertical timing parameters.

In addition to defining the vertical timing, some of the following parameters have a bearing on where vertical serrations and equalizing pulses will appear in the composite sync signal. For strict adherence to NTSC, some additional attention should be given to the lengths of the VFRONTPORCH and VSYNCFINISH parameters.

The figure below shows each of the vertical timing regions, and gives the parameter name which defines its duration.

0 - VFRONTPORCH + 1 half line time.
1 - Sync pulse width = 3 lines.
2 - VBACKPORCH + 8 half line times.
3 - VLINES + 1 half line time.

FIGURE 12

VFRONTPORCH VFP(7:0)

This parameter is equal to one less than the number of half lines in region 0 of the figure above. This is the "front porch" of the vertical field. The composite sync signal will have equalizing pulses inserted during the front porch portion of the vertical field.

VBACKPORCH VBP(7:0)

This parameter equals eight less than the number of half-lines in region 2 of the figure above. This is the 'back porch' portion of the vertical field.

This parameter equals one less than the number of half-lines in region 3 above. This is the active portion of the video field. For interlaced display, this parameter is set to half of the total number of lines to be scanned.

All of the TFB's parameters can be determined from just a few assumptions about the length of the scan line, the number of lines in a frame and so on.

6.3.4 Other Address Spaces

The TFB2.2 provides software interfaces for the CLUT/DAC chip, managing the vertical interrupt, reading the ID of the monitor connected to the card, and ROM. These interfaces are defined below.

CLUT/DAC Interface

The TFB2.2 supports two CLUT/DAC chips, the Bt453 and Bt454.

For the Bt454 a select is provided that is asserted to accesses to $90000 in the slot space. It is up to the individual designer to map reads and writes within this address space. For each of these accesses, some offset may need to be added to get at the desired register on the Bt454. This address is determined by the card designer.

For the Bt453, the TFB2.2 provides a chip selects as well as the READ and WRITE signals to the chip. Reads are made by reading $90010 in the slot space. Writes are made by writing to $90020 in the slot space. For each of these accesses, some offset may need to be added to get at the desired register on the Bt453. This address is determined by the card designer.

Sense Line Reading

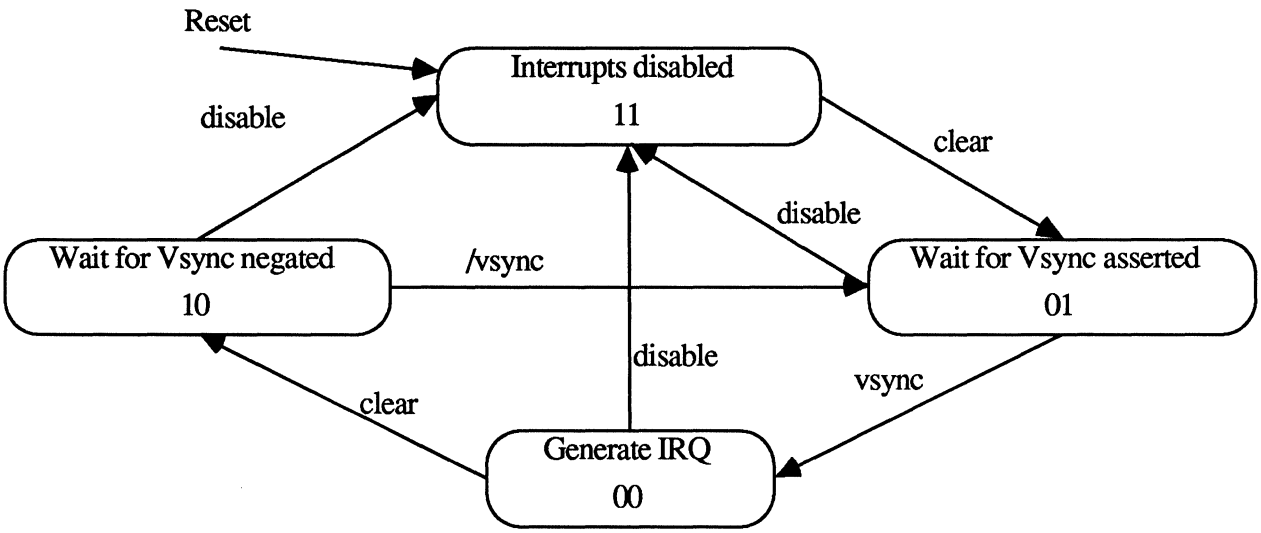
Monitors plugged into cards implemented with the TFB2.2 can identify themselves by encoding themselves on three sense lines available to the TFB2.2. Software can read the state of these lines by examining bits (10:8) of address $90000. Note that these are Nubus bits, the Big Endian nature of the 68020 will route these bits to bits (18:16) in the 68020 address space.

ROM Interface

The ROM is located at every 4th address in the high 16K bytes of the slot space.

Vertical Interrupt Management

The Nubus Non Master Request signal is used to generate the vertical interrupt from the TFB2.2. Control of this signal is determined by the following state diagram:



disable = a19 & /a18 & a17 & /a16 & a2
clear = a19 & /a18 & a17 & /a16 & /a2

FIGURE 13

6.3.5 Initialization Procedure

Before loading any values into the TFB's control registers, a soft reset should be issued to the TFB2.2. All but the register at $30 can be be loaded in any order. Finally, the value for register $30 is loaded to clear the soft reset state. The TFB2.2 should be taken out of the soft reset state only after all bits in all registers are in the desired state.

6.4.0 SIGNAL DESCRIPTION

The following lists the TFB's signal names, pin numbers, I/O direction The format for the signals is as follows:

<pin name> <pin #> <I/O>

6.4.1 Bus Interface

These signals are used to interface to the NuBus. In general, they are designed to be easily interfaced with that bus.

/10M0 46 INPUT

This is the Nubus 10 MHz clock.

/10M1 47 INPUT

This signal is a version of the 10MHz Nubus signal that is delayed 50ns. It is NANDed with the Nubus clock to form a 20MHz signal used internally to the TFB2.2 for generation of the various RAM control signals.

/RESET 48 INPUT

When /RESET is asserted, the TFB2.2 is initialized to a known state. Many of the control parameters are cleared or set when /RESET is asserted, so the control registers should be assummed to be in a random state.

The bus interface logic is initialized to a wait condition. No refresh of memory will take place until the video is enabled via the SOFTRESET parameter bit described above, after the /RESET signal is asserted.

/RESET is internally synchronized to both PXIN and NU10M0, so /RESET must be asserted for at least five cycles of the slower of PIXCLK and NU10M0.

/ACK 43 BIDIRECT

This signal is the Nubus acknowlege signal. It has enough drive to connect directly to the bus.

/TM0 45 BIDIRECT

This signal is the Nubus /TM0 signal. It has enough drive to connect directly to the bus.

/TM1 53 BIDIRECT

This signal is the Nubus /TM0 signal. It has enough drive to connect directly to the bus.

/SLOTSEL 81 INPUT

This signal is generated by comparing Nubus addresses AD(31:28) to ground and addresses AD(27:24) to the slot ID for the card during the START cycle. A 74F521 with the compare enable line tied to /START works nicely for generating the /SLOTSEL signal.

/NMRQ 40 OUTPUT

This signal connects directly to the Nubus non master request signal. The control of this signal is described above in section 6.3.4

EAD(7:0) 72-65 INPUT
EAD(11:8) 52-49 BIDIRECT
EAD(19:12) 80-73 INPUT

These are the address data signals from the Nubus. They should be buffered, as they do not provide adequate drive for Nubus. AD(11:8) provide bits to read the state of the SENSE pins and the internal vertical blank signal. SENSE (2:0) lines are placed on AD(10:8) and the vertical blank signal is placed on AD11 when a color table read access is made to the chip.

6.4.2 Card Control

These signals provide selects and control signals to control the other chips found on the video card.

PXS(1:0) 57,56 OUTPUT

These two signals provide selects for a mux used to select the desired pixel clock. CMOS being a rail to rail technology, these signals can be connected to either ECL or TTL muxes.

/CTRD 58 OUTPUT

This is a color table read control signal compatible with the Bt453.

/CTWR 59 OUTPUT

This is a color table write control signal compatible with the Bt453.

/CTS60 OUTPUT

This is a color table select signal compatible with either the Bt453 or Bt454 depending on the state of the Bt453 control bit described above.

/ROMSEL 61 OUTPUT

This signal is a select and output enable signal for the configuration ROM.

/WROE 62 OUTPUT

This signal determines the direction of the 74F245s used to buffer the AD bus from the Nubus.

A(13:2) 95-93, 89-82,63 OUTPUT

These signals are the latched addresses from the AD bus. They are used to address the ROM and any other peripheral chips needing latched addresses.

SENSE(2:0) 104-102 OUTPUT

These signals provide a mechanism for encoding what monitor is hooked up to the video card. Software can read the state of these bits by reading the color table space described above. The software driver can then configure the video card to deliver the proper timing for the monitor that is hooked up to the video card.

6.4.3 RAM Interface

These signals are used to interface to the VRAM on the card. They are compatible with the control signals for the NEC 150ns VRAM (and many others).

RAS(1:0) 21,20 OUTPUT

These signals are row address strobes for each bank of RAM.

CAS(1:0) 23,22 OUTPUT

These signals are column address strobes for each bank of RAM.

DOE(1:0) 16,15 OUTPUT

These are the data output enable signals for each bank of RAM.

WEN(3:0) 39-36 OUTPUT

These are the write enable signals for each byte lane of the RAM.

SCLK 17 OUTPUT

SCLK clocks the video data from the RAMs to the TFB2.2. Each SCLK signal is capable of driving 8 RAM chips at full speed. Buffering of SCLK is recommended for any system using the 16 bit per pixel mode of operation, otherwise buffering is not necessary.

SOE(1:0) 14,13 OUTPUT

SOE selects which bank is to put its data onto the VD pins of the TFB2.2.

RA(7:0) 34-31,
28-25 OUTPUT

These are the RAM address bits provided by the TFB2.2. Addresses come from either the refresh address generation circuitry on the TFB2.2, the next scan line address generation circuitry on the chip, or the CPU addresses presented during a RAM access cycle.

6.4.4 Video Data Interface

These signals control the pixel datapath between the serial data outputs of the VRAM to the pixel data inputs of the CLUT/DAC chip.

VD(31:0) 12-1,
144-137,
117-106 INPUT

These are the serial data outputs of the VRAMs that connect directly to the TFB2.2.

PXIN 101 INPUT

This is the pixel clock input from an oscillator or mux providing a pixel clock from which the rest of the timing is derived. When interfacing with the Bt454, This input is equal to the pixel clock divided by 4.

PXOUT 92 OUTPUT

This is a delayed version of the PIXIN input which can be used to ease the timing constraints of the PXD bus and the video sync signals.

/CBLANK 99 OUTPUT

This is an RS170 compatible composite blank signal.

PXD(15:0) 135-128,
125-118 OUTPUT

Pixel values are shifted through the PXD bits once every rising edge of PXCLK. Unpredictable values are clocked out when CBLANK is high.

In order to facilitate use of the TFB2.2 in very high performance systems, the PXD bus generates pixel data in a rather unique manner. By multiplexing the 16-bit PXD bus down to 8 bits, the pixel generation speed of the TFB2.2 can be effectively doubled. When running in this configuration, the TFB2.2 can support up to 66MHz video rates from 1 to 8 bits per pixel. This process is facilitated by placing certain PXD bits onto more than one pin as per the following table:

PXD PINS

DEPTH	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
000	PX15	PX14	PX13	PX12	PX11	PX10	PX09	PX08	PX07	PX06	PX05	PX04	PX03	PX02	PX01	PX00
001	0	0	PX07	PX06	0	0	PX05	PX04	0	0	PX03	PX02	0	0	PX01	PX00
010	0	0	0	PX03	0	0	0	PX02	0	0	0	PX01	0	0	0	PX00
100	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PX00
101	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PX01	PX00
110	0	0	0	0	0	0	0	0	0	0	0	0	PX03	PX02	PX01	PX00
111	0	0	0	0	0	0	0	0	PX07	PX06	PX05	PX04	PX03	PX02	PX01	PX00

TABLE 7

The table above shows the pixel value at each of the PXD pins for each of the possible programmed depths.

6.4.5 Monitor Timing Interface

These signals interface to the monitor.

/HSYNC 96 BIDIRECT

This is a programmable horizontal sync signal. /HSYNC is bidirectional so that the TFB2.2 can synchronize to an external video source. The direction of this signal is determined by the GNLCK parameter described above.

/VSYNC 97 BIDIRECT

This is a programmable vertical sync signal. /VSYNC is bidirectional to allow genlocking. The direction is determined by the GNLCK parameter described above.

/CSYNC 98 OUTPUT

This is an RS170 compatible composite sync signal.

6.4.6 Test Pins

/TESTEN 105 INPUT

When asserted, TESTEN puts the TFB2.2 into test mode. This mode can be used to examine some internal state of the TFB2.2. During normal operation, this input must be tied HIGH.

When /TESTEN is LOW, with SENSE0 LOW, all of the TFB2.2 outputs are tristated to allow for in circuit test.

When /TESTEN is LOW, with SENSE0 HIGH, all outputs but PXD(3:1) are tristated. In this mode, PXD(3:1) are the last stages of 3 internal shift register chains used for scan test. These chains were chosen for their deeply embedded nature and for the fact that they are not speed critical paths.

6.5.0 BUS OPERATION

Three kinds of accesses can be made through the TFB2.2 to the video RAM:

- RAM cycle
- Video register data transfer cycle
- RAS only refresh cycle

6.5.1 RAM Cycle

The RAM read or write cycle begins on the falling edge of /10M0 when /SLOTSEL is sampled LOW. On the following falling edge of /10M1, /RAS is asserted and the RAM access continues to completion. On occasion, during RAM refresh cycles or during data transfer cycles, the RAM access will not complete immediately. The TFB2.2 will hold off /ACK until the access is complete. Best case timing for any Nubus access is 400ns.

6.5.2 Data Transfer Cycle

The data transfer cycle is executed to set up the shift register found inside the NEC video RAMs for putting out the proper pixel data for display on the CRT. Data transfer cycles are requested by the pixel state machine part of the controller and have higher priority than CPU accesses so that, at times, CPU accesses will be forced to wait for a data transfer cycle to complete. At most, two data transfer cycles will be executed during a single scan line.

One data transfer cycle is always performed during horizontal sync. This instance of the cycle takes 5 Nubus clock cycles to complete. Since no pixels are being sent to the CRT during this time, no synchronization is required between the RAM state machine and the pixel state machine. The horizontal sync data transfer cycle sets the shift register up to begin outputting data at the start of the next scan line.

Calculation of the start of the next scan line in memory is fairly complicated. At the start of each scan line, the longword address is calculated by summing together two out of five possible numbers:

<Next Scan Line Address> = (BASE or <previous scan line address>) +
(4*LENGTH or 8*LENGTH or 0)

If the next scan line is the start of a new field, then BASE is selected as the first addend; otherwise the previous scan line address is taken.

If the next scan line is the start of a new field, and the INTRLC parameter is set, then 8*LENGTH is selected as the second addend.

If the next scan line is the start of a new field, and the INTRLC parameter is set, and the current field is 'odd' (where the fields alternate between even and odd), then zero is selected as the second addend.

Finally, if the INTRLC parameter is not set, then 4*LENGTH is selected as the next addend.

Often, a second data transfer cycle will be executed during the active portion of the scan line. Very careful synchronization between the bus controller and the pixel controller is required for this access so that pixel data being sent to the CRT is not disrupted. This means the exact time for this access to complete cannot be predicted.

As pixel data is scanned out, a counter on the TFB2.2 keeps track of which 32-bit longword in the shift register is currently being read out. If this 8-bit counter reaches $FF during the active portion of the scan line, then a data transfer cycle must be executed to reload the shift register. The data transfer cycle needed for reloading the shift register can be a lengthy one. As the shift register counter nears $FF, the TFB2.2 must detect the coming end of the shift register and request a data transfer cycle be started by the RAM state machine. This request must come early enough to allow any CPU access to memory to complete and to allow the data transfer cycle to nearly complete just as the last longword is read from the shift register. Since the ratio of the PXIN period to the Nubus clock period can have a very wide range depending upon the application, the setup time required by this data transfer cycle is somewhat programmable.

The setup time required for any data transfer cycle is a minimum of 12 Nubus clock periods. When the SETUP parameter is equal to bits 2, 3 and 4 of the shift register counter, and bits 5,6 and 7 of the counter are high, a data transfer cycle is requested.

6.5.3 Refresh Cycle

After the data transfer cycle during each horizontal sync period, the TFB2.2 executes a number of refresh cycles to the RAM. Since horizontal scanning frequencies will vary from system to system, the number of refresh cycles executed is programmable and is given by the 3 bit RFSH parameter. The refresh cycles are CAS before RAS type cycles.