LISA

HARDWARE MANUAL

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PREFACE

(Full Version Only)

The LISA Hardware Manual is concerned with the internal functioning of the LISA system. It is intended for use by people concerned with the detailed functional operation of the LISA hardware. It is divided into two sections.

Section I provides information on the functional performance and specification of the system. Chapter 1 provides a general introduction to the Lisa system, while giving a brief description of the system architecture. Chapter 2 will be of interest to programmers who need to know the address and interrupt structure, as well as the operation of the Memory Mapping Unit. Chapter 3 contains information on dimensions and environmental requirements and interfaces to the system, which are of use to design engineers wishing to interface to the Lisa.

Section II of the manual contains full functional descriptions and theory of operation for each of the modules in the Lisa system. It will not be of interest to the general reader and is intended for use only by design and service personnel. Section II includes chapters on:

* The processor board
* The memory board
* The I/O board
* The video board
* The operator interface
* The floppy disk unit
* The power supply
* System assembly

The appendices supply schematics for the system components. Other documents relevant to the system are:

* LISA Hardware Manual (Condensed Version)
* LISA Floppy Disk Drive Manual
* LISA Owner's Guide
* LISA Operating System Manual

* Motorola 68000 User's Manual
* Motorola 6504 User's Manual
* Motorola 6522 Data Sheet
* COPS421 User's Manual
* 8530 SCC User's Manual
* AMD 9512 Data Sheet

TABLE OF CONTENTS

Chapter 6 THE I/O BOARD

Chapter 7 THE VIDEO BOARD

Chapter 8 OPERATOR INTERFACES

Chapter 9 FLOPPY DISK DRIVES

Chapter 10 POWER SUPPLY

Chapter 11 SYSTEM ASSEMBLIES

LIST OF FIGURES

-- Section I --

-- Section II --

SECTION I

CHAPTER 1

SYSTEM ARCHITECTURE

The LISA is an extraordinarily powerful and compact personal computer system. It features a large amount of memory, integral display and disk storage, and an extensive mix of I/O devices. Perhaps the most striking hardware feature is the ease with which the operator can talk to the computer through use of the mouse device in conjunction with the extensive system graphics.

(Insert Figure 1-1)

Details of the operation and use of the LISA can be found elsewhere. A list of related documents for the LISA system can be found in the Preface. The purpose of this Hardware Manual is to provide an exhaustive description of the internal workings of LISA for those who need to know how the hardware functions in order to diagnose, repair and expand the system.

1.1 System Layout

The LISA consists of several replaceable hardware modules that are assembled in the main chassis, plus the keyboard and mouse that are external to it. Refer to Figure 1-2, which shows the physical location of each major component.

(Insert Figure 1-2)

The system components are accessed by removal of the front and rear panels. Note that removal of these panels causes the unit to lose power due to the panel safety interlocks.

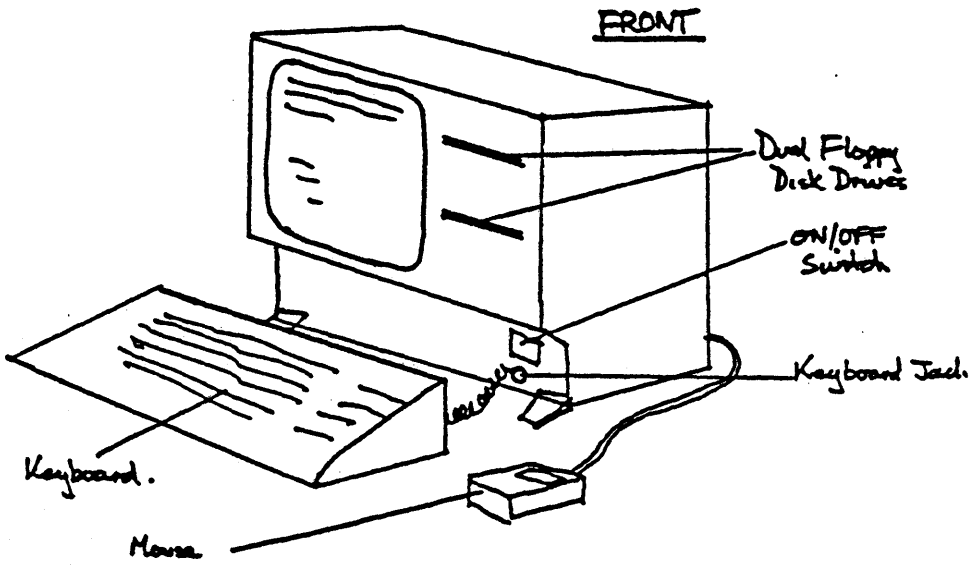

Figure 1-1. System Front View

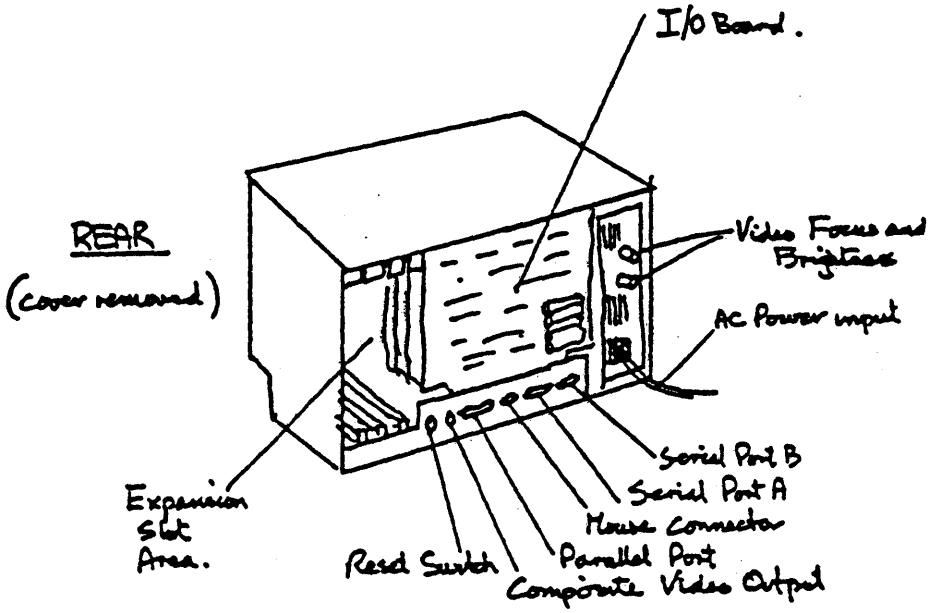

Figure 1-2. System Rear View

Chapter 3 describes the general assembly of system components in the LISA in more detail. Assembly/disassembly procedures are available in other LISA documents.

1.2 Hardware Structure

The logic components of the LISA system are interconnected by means of several buses, as shown in Figure 1-3. The main system bus connects the processor board with the I/O board and the extension slots.

(Insert Figure 1-3)

The heart of the system is the processor board, which contains the system CPU, timing, memory management unit (MMU), video generation logic, I/O decode and interrupt logic. It also provides the necessary control and timing signals for the memory boards. The memory boards can be in several possible configurations, depending on the size and type of memory installed. The memory board contains the main system RAM matrix, plus parity generation and checking and some address decoding logic.

The system communicates with the outside world principally through the I/O board. This board provides controllers and interfaces for two serial I/O ports, a parallel port (for use with peripherals like a hard disk or printer), the keyboard, the mouse, the speaker and the floppy disk drives. Video contrast is also under the control of logic on this board. In addition, the CPU may have the use of an optional arithmetic processing unit, located on the I/O board.

The video board is controlled both by the logic present on the processor board and by the contrast latch on the I/O board. It provides the analog logic necessary to drive the video monitor. The video memory is used to display an image organized as a bit map in main system memory.

The expansion slots on the motherboard provide locations for additional logic modules to connect with the basic system. A description of the bus interface itself can be found in Chapter 3 of this manual.

The floppy disk drives accept LISA standard 5.25" floppies. They are described in a separate manual. An overview of the drive is given in Chapter 9.

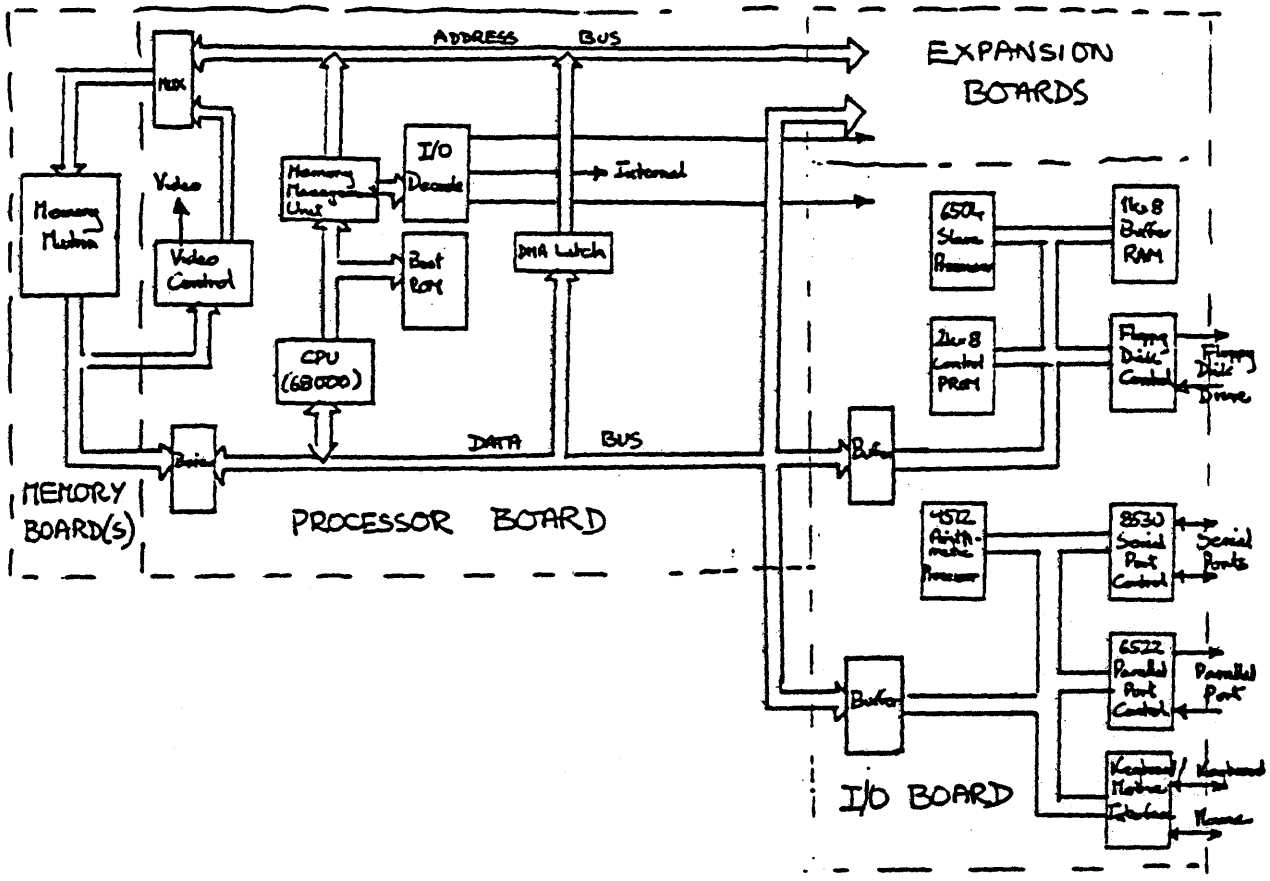

Figure 1-3. System Block Diagram

The monitor is a high-resolution 12" diagonal tube with a P4 phosphor screen which uses a 60Hz refresh rate. It displays individual pixels as black or white only. There is no gray scale as such. Grays are displayed by intermixing black and white pixels in the same area.

1.3 The Central Processing Unit

The intelligence of the LISA system is based on the Motorola 68000 processor chip. This advanced 16-bit, single-chip device offers a very powerful instruction set. A block diagram of the 68000 is shown in Figure 1-4.

(Insert Figure 1-4)

The 68000 offers the following features to the system:

* 32-bit data and address registers
* 16-megabyte addressing range
* Memory-mapped I/O
* 14 addressing modes

In addition to the seventeen 32-bit registers, a 32-bit program counter, and a 16-bit status register, there exists the possibility of configuring the general purpose registers to allow for the width of the data actually being used.

In the LISA, the 68000 is driven by a 5 MHz clock (period 200 nanoseconds). The processor memory access time is 800 nanoseconds. The CPU and the video logic interleave memory accesses. Instruction execution times must be a multiple of 800 nanoseconds. All instructions which are longer than 800 nanoseconds have wait states inserted if required so that all instructions execute in multiples of 800 nsecs.

1.4 Memory

The 68000 CPU generates 24-bit logical addresses to access data in the system. These are considered logical addresses and the set of all possible addresses is the 16 Mbyte logical address space of the LISA. The logical address space is used to access all ROM, RAM and I/O present in the system.

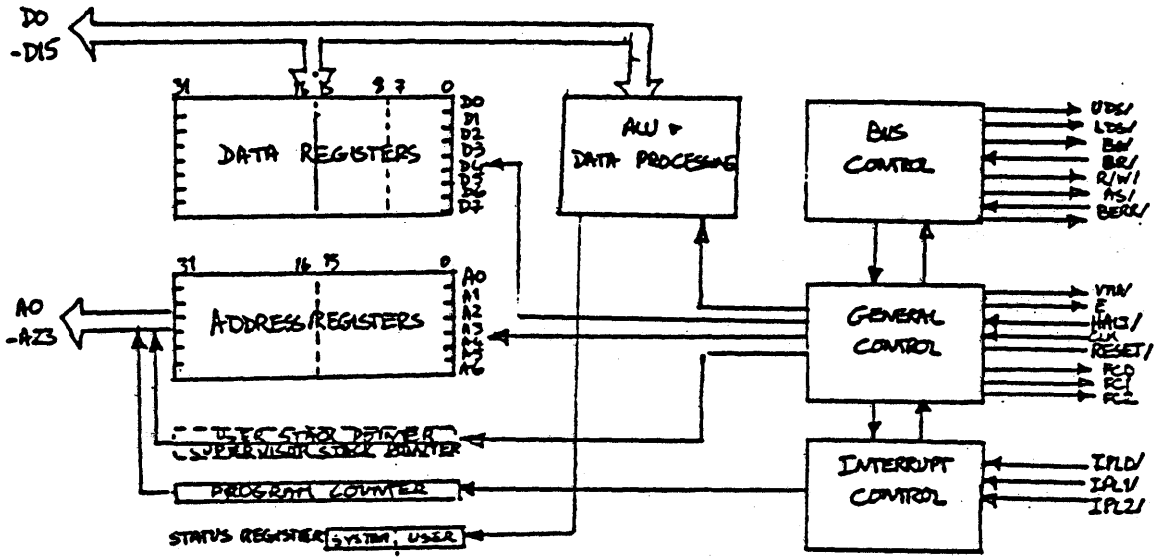

Figure 1-4. Processor Block Diagram

In order to access one of these physical locations, each logical address must be transformed into a physical address. A physical address may point to one of the three possible physical address spaces in the system. These are:

* Main memory (2 Mbytes of system RAM)
* I/O space (I/O devices and latches)
* Special I/O (MMU registers and boot ROM)

The transformation is performed by a method known as relocation. It is implemented by a section of logic on the processor board known as the memory management unit (MMU).

The main memory is where programs and data are stored while in use by the system. The MMU provides both the transformation of the address and flags which provide further information on the type and the accessibility of the data. This is described in Section 2.3

The I/O space is used to access peripheral controllers and status and control registers.

The Special I/O space is used only to access bootstrap routines stored in non-volatile ROM and also to access the registers internal to the MMU in which transformation data is stored. This latter storage area permits the operating system to control the entire relocation process.

Within the MMU there are in fact four identical sets of transformation registers, each representing a different mapping of logical addresses into the three physical address spaces. Each set is called a context. Context 0 is reserved for use by the operating system, while 1, 2 and 3 are available for the user programs. Only one context is current at any given time. By switching contexts, rapid switching between processes can be effected under operating system control.

User programs only need to be aware which segments of logical space are available to them and which of these point to RAM and to valid I/O addresses. The MMU performs access checks and classifies the type of storage to which they point, such as stack memory, ROM and I/O space.

The maximum configuration of RAM storage that can be present in the main memory is 2 Megabytes. This restriction derives from limits on the size and number of memory boards which can be placed in a LISA system.

Hexadecimal Address Range	Physical Address Space	Function
000000-1FFFFF	Main Memory	System RAM storage
000000-001FFF	I/O	Slot 1 low decode
002000-003FFF	I/O	Slot 1 high decode
004000-005FFF	I/O	Slot 2 low decode
006000-007FFF	I/O	Slot 2 high decode
008000-009FFF	I/O	Slot 3 low decode
00A000-00BFFF	I/O	Slot 3 high decode
00C000-00CFFF	I/O	FD Controller memory
00D000-00DFFF	I/O	I/O board devices
00E000-00EFFF	I/O	CPU board devices
xx0000-xx3FFF	Special I/O	Boot & self-test ROM

Figure 1-5. Physical Memory Map

Each physical memory space within LISA is divided as shown in Figure 1-5.

(Insert Figure 1-5)

Special I/O space is not invoked during normal operation. It is only used during system startup, and when the registers which configure the MMU are being modified. During normal operation, only the operating system has access to Special I/O space.

Note that the operating system is capable of providing this ability to any program, although it would not be advisable practice to do so.

Since logical addresses make no distinction among the three possible address spaces, each can be operated on by the full 68000 command set. Each physical address space shown in Figure 1-5 is distinguished by signals generated within the MMU. There is therefore no physical overlap of memory space and no masking of any memory area.

1.5 Internal Buses

The LISA system makes use of two bus structures for communication between system components.

Most components of the LISA system communicate by means of the system bus. This bus interconnects the processor board with the I/O board and the expansion slots.

The system bus is based on the interface signals of the 68000 CPU device. Operations and timing on the bus follow those of the 68000 closely, although not identically. Refer to Chapter 4 for a discussion of the system bus and its operation.

The second bus is the memory bus. This is a specialized set of signals which are used by the processor board to provide timing and control signals to the memory board(s).

1.6 Storage Media

The LISA system has two high-density mini floppy disk drives. Disks from non-LISA systems may not be freely interchanged with those used in LISA, due to the special encoding of disks format and meadia type. Details of the drives themselves can be obtained from Chapter 9 or from the relevant drive manual.

In addition, a compatible hard disk drive, such as Apple's Profile, may be connected to the parallel port to provide enhanced data storage capacity and access time. Details of this interface can be found in Chapter 3. Format and storage capacity of this drive are a function of the actual unit used. Details are beyond the scope of this document.

1.7 User Interfaces

The user communicates with the LISA by means of the keyboard, as on a conventional computer system, or by means of the mouse.

The mouse is a very powerful device when used in conjunction with the resident LISA software. It permits the use of the CRT screen as a work surface and as a means of selecting among the available functions. Many tasks can be performed without the need to type in commands on the keyboard.

1.8 Additional Features

A real-time clock has been incorporated in the I/O board. This shows the correct time, and is available to the programmer for use in a number of applications where measurement of elapsed time or the current date and time is important.

The I/O board includes a socket for an optional arithmetic unit, which is available to the operating system to perform complex calculations without making excessive demands on CPU time.

The system is also equipped with a battery-backup unit. This enables the real-time-clock to function while the system is entirely disconnected from a power source. It also preserves the contents of the parameter memory in the floppy disk controller.

CHAPTER 2

SYSTEM PROGRAMMING

This chapter describes the interface which the LISA hardware provides to the system software. It is not intended as an exhaustive description of the operating system, nor should it be regarded as a specification of required parameters for an operating system on the unit. Details on programming may be found in manuals listed in the preface.

2.1 The Instruction Set

The instruction set of the LISA is essentially that of the 68000 processor. Differences occur only in the details of addressing the memory and I/O in the LISA.

Instructions may be categorized into four possible modes of logical addressing:

* Data -- When an effective address mode refers to data operands, it is considered as a data address mode.

* Memory -- When an effective address mode refers to memory operands, it is considered a memory address mode.

* Alterable -- When an effective address mode is used to refer to writeable operands, it is considered an alterable address mode.

* Control -- When an effective address is used to refer to memory operands without an associated size, it is considered a control address mode.

It is possible to combine these categories within the instruction set, resulting in more specialized categories. For example, data alterable would refer to address modes which are both data and alterable.

Note that the status register addressing mode is not permitted unless it is explicitly mentioned as a legal addressing mode.

The full instruction set is not discussed here. Details are available in the 68000 User's Manual.

2.2 CPU Registers and Their Use

There are a number of 32-bit registers in the CPU that are available to the user. These are:

- 8 Data registers
- 7 Address registers
- 1 User stack pointer
- 1 Supervisor stack pointer
- 1 Program counter

In addition, there is a 16-bit status register, which consists of a user byte and a system byte.

The data registers may be used for bit, byte, word or long-word operations. The address registers can be used as word or long-word registers. Both the address registers and the system stack pointer may be used as software stack pointers and base-address registers. All data, address and stack pointer registers may be used as index registers.

Where a data register is used to store less than the full 32-bit capacity, the bit, byte or word is stored in the low-order part of the register. The least significant bit is bit zero and the most significant bit is bit 31.

Address registers provide either the low-order word, or the full 32-bit long word as the source operand, depending on the operation. When used as a destination, the entire register is affected, regardless of the size of the operand required in the operation.

The status register contains a number of coded bits, divided into a user and a supervisor byte. The supervisor byte contains the trace and supervisor flags, plus a three-bit code showing the current interrupt mask. The user byte contains the condition codes. Refer to the 68000 User's Manual for a full discussion.

2.3 Memory Management Scheme

The MMU is a hardware device which translates logical addresses emitted by the CPU into physical addresses for objects in the system main memory or I/O space. At the same time, it provides access controls, preset by the operating system. These prevent a particular program from accessing areas of memory outside of the portion assigned to it.

The logical address provided by the CPU consists of 24 bits. These are interpreted by the MMU in three sections. The first section consists of bits 24 through 17 and defines the logical segment. The second section consists of bits 16 through 9 and provides the logical page displacement. The third section consists of bits 8 through 0 and gives the displacement (both logical and physical) within the page. This can be seen in Figure 2-1.

(Insert Figure 2-1)

Logical addresses may point to any part of the 16 Mbyte addressing space. The MMU interprets these logical addresses on the basis of translation parameters loaded into its registers by the operating system.

The LISA system memory physically occupies 2 megabytes of physical address space. This would imply that only 16 segments, each of 128K-bytes can be meaningfully used. However, each segment's physical address space does not necessarily occupy the full 128 Kbytes allotted to it in logical address space. Each segment can be mapped into as little as one 512-byte page of physical memory. Therefore many more than 16 logical segments can map into the 2-megabyte system memory space.

Within the MMU, each segment has two registers associated with it. The first is known as the Segment Origin Register (SOR). It describes the physical origin of the segment, which is a page boundary within the memory. The second is the Segment Limit Register (SLR). It describes both the size in terms of 512-byte pages and the type of space being addressed.

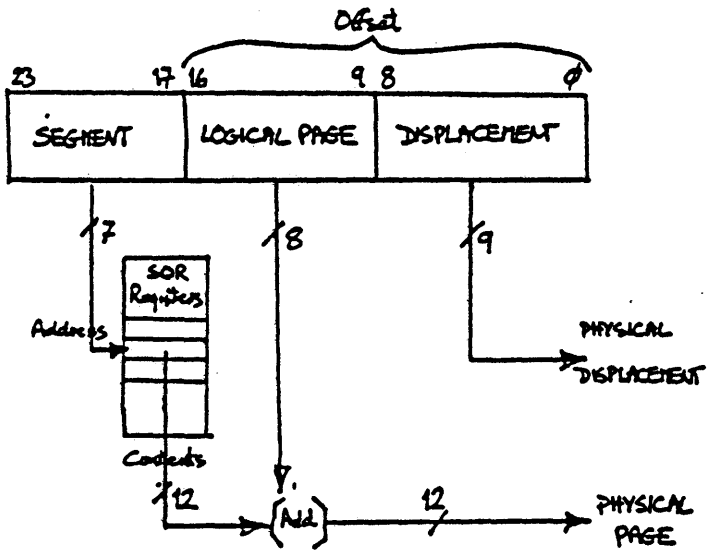

Figure 2-1. Address Word Decode

2.3.1 Address Transformation

Logical address space is divided into 128 logical segments on 256-page boundaries. Each page consists of 512 bytes.

The SOR register contains the 12-bit page address in physical space where the corresponding physical segment begins. The entire segment is located in physical space with respect to this origin. The address of the segment origin is calculated using the first section of the logical address word to address the SOR register. The logical page displacement given by the second section of the logical address is added to the contents of SOR to produce the physical page address being accessed. The logical operation is shown in Figure 2-1. The least-significant nine bits of the logical address translate directly into the physical displacement.

The SLR contains the size limit of the physical segment, given as a number of pages, plus control bits which define the type of the segment. This indicates which of the three physical address spaces the segment is contained in (memory, I/O or special I/O). It may also indicate the memory use, such as read-only or stack.

Once the SOR contents and logical page displacement have been added, the MMU performs a limit check to see whether the resulting physical page lies within the limits given by the SLR. The logical operation performed is shown in Figure 2-2.

(Insert Figure 2-2)

The same logical segment address is used to access the SLR as the SOR. The SLR contains control and limit data. The high-order four bits of the register contain control information. The low-order eight bits contain the number of pages in the segment, which is compared with the page offset in the logical address.

If the address is within the physical segment, the instruction proceeds. If the address lies outside the segment, the instruction is terminated and an error condition is presented to the CPU.

The physical address word consists only of 21 bits (12 bits page number and 9 bits displacement). These 21 bits are sufficient to address a space of 2 Mbytes.

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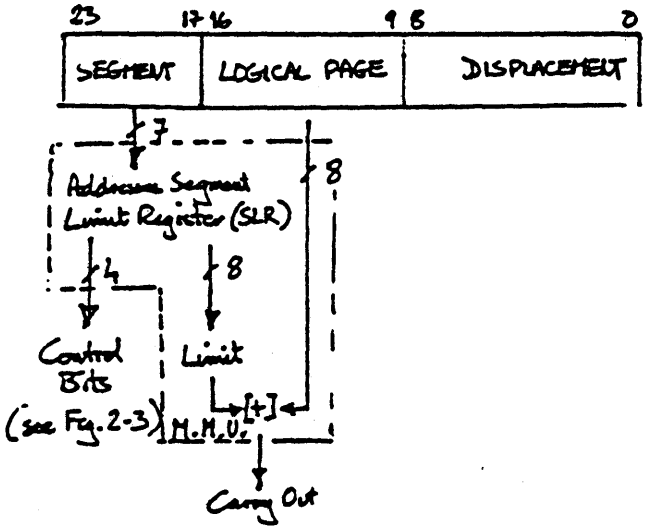


Figure 2-2

Figure 2-2. Segment Limit Check

2.3.2 The MMU Registers

The MMU registers are physically a matrix of 1024 12-bit registers. These are divided into four sets of 128 pairs of registers, one for each of the four contexts in which the system may operate. The technique of switching contexts is used to rapidly reconfigure the system when switching between processes.

All MMU registers are addressed in Special I/O space (refer to Figure 1-5). The contents of the Segment Origin Registers (SOR) are modified or read by accessing an address in Special I/O space shown in Figure 2-3.

(Insert Figure 2-3)

A segment which was to begin at the physical address 000200 would have its corresponding Segment Origin Register set to 0001. The SOR contains the origin in terms of multiples of 512-byte pages in the physical space.

The segment length is interpreted by the system IN TWO'S COMPLEMENT FORM. Care should therefore be taken in loading the limit to be used. A length of 00 implies a segment of maximum length (128 Kbytes). A length of FFH implies the minimal segment length of 512 bytes (one page).

An exception to the above occurs in the case of a stack segment, which is flagged as such by the control bits. In the case of a stack, usage of the segment begins at the top of the segment and decrements. Thus 00H implies one page (512 bytes) and FFH implies 128-kilobytes for a stack segment only.

The access control bits are used to restrict program manipulation of the data pointed to in the area of memory. The bit significance is shown in Figure 2-4.

(Insert Figure 2-4)

To set up the MMU registers, the SOR and SLR registers must be set up by the operating system for each of the 128 possible segments.

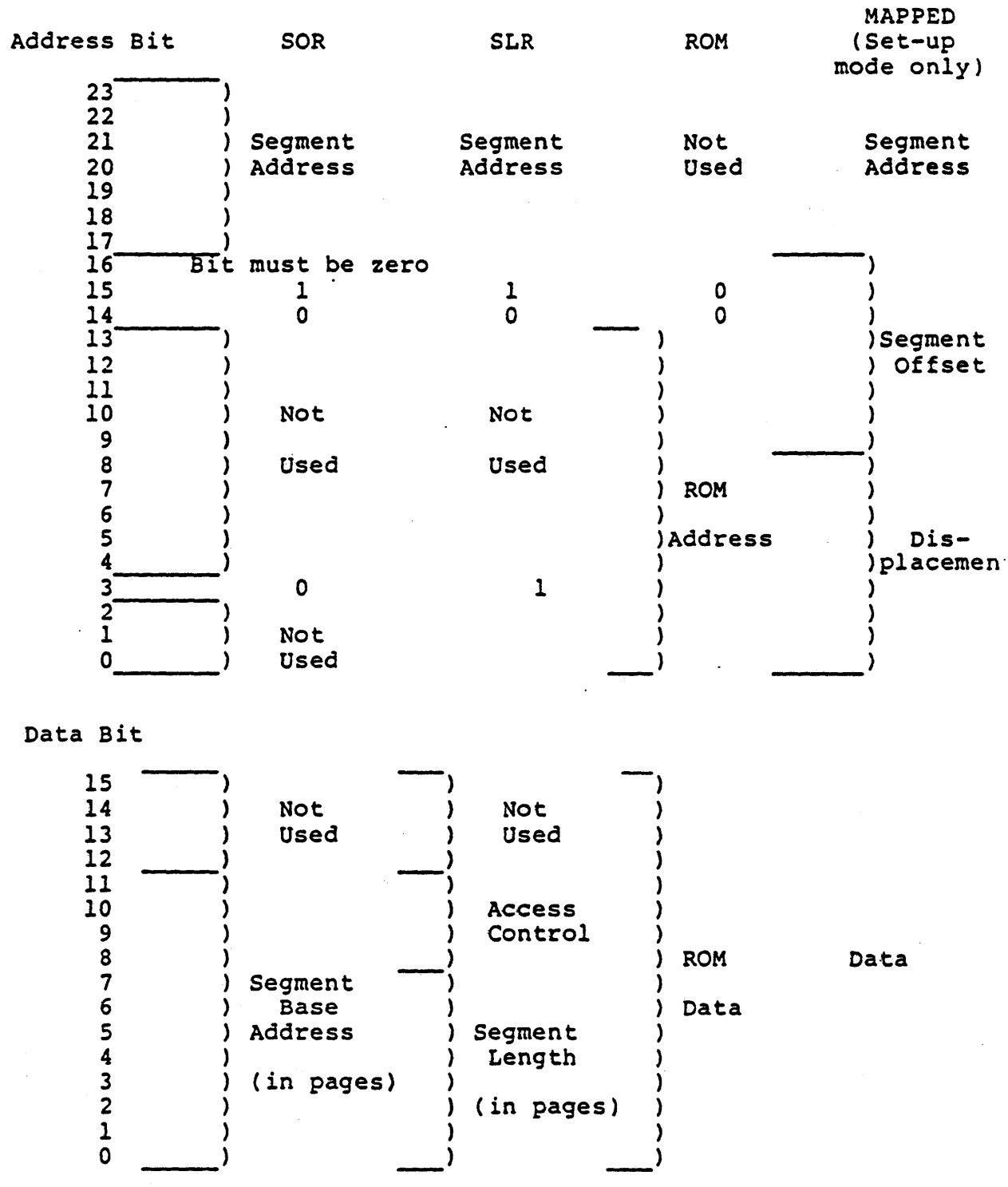


Figure 2-3. Special I/O Addressing

Bit 11	10	9	8	Address space and access limitation
0	1	0	0	Main memory -- read only from stack
0	1	0	1	Main memory -- read only
0	1	1	0	Main memory -- read/write to stack
0	1	1	1	Main memory -- read/write
1	0	0	1	I/O space
1	1	0	0	Page invalid (segment not present)
1	1	1	1	Special I/O space
0	0	0	0	)
0	0	0	1	)
0	0	1	0	) Invalid Codes
1	0	0	0	)
1	0	1	0	) (Unpredictable results
1	0	1	1	) will occur)
1	1	0	1	)
1	1	1	0	)

Figure 2-4. MMU Access Control Bits

2.3.3 MMU Initialization

When the system performs a Power-On Reset (POR), the MMU registers are in an unknown state. In order to write to the MMU registers, the system must be in setup mode. This is satisfied automatically at power-on time, or by software accessing I/O address 00E010H.

In setup mode, the system operates only in special I/O space. This means that only the system boot ROM and the MMU register set are accessible. Bit 14 of the address acts as a switch between system RAM and system boot ROM. During initialization, the RAM does not yet contain meaningful data and bit 14 must be reset to operate from ROM. When the program is to be run via the MMU in setup mode, such as access to RAM, bit 14 of the physical address must be set. In the former case, ROM is not accessed using the mapping of the MMU, and therefore will function during initialization.

An 1111 code output for the system access bits of the SLR registers is provided by hardware in setup mode. The MMU is not used to address the boot ROM, so the boot program does not require mapping to be operational.

The MMU registers are normally initialized in the scheme shown in Figure 2-5. The example shows a configuration for a 1 Mbyte memory size. For a 2 Mbyte memory, the number of System RAM segments would be increased accordingly.

(Insert Figure 2-5)

Note that since the seven bits which address the segment in question are the MSB's of the address, the address actually embedded in the address word appears to be left-shifted by one bit. Thus, 7E would actually read FC.

To set the MMU registers, usually the memory map is disabled. This is done by setting the SETUP bit. This bit is set automatically at power-up when the map registers are uninitialized. It must be set whenever the map registers are being loaded.

In order that a program in system RAM may continue to execute when setup mode is entered, a hardware switch is incorporated which permits execution via the MMU when in setup mode. This avoids the need to invoke a subroutine in ROM, which would otherwise be necessary. This option should not be invoked unless the program is executing out of system RAM with address bit 14 set (see above).

Segment Address	Physical Address	Usage
00	512k to 640k	System RAM
01	640K to 768K	System RAM
02	768k to 896k	System RAM
03	896k to 1024k	System RAM
04	1024k to 1152k	System RAM
05	1152k to 1280k	System RAM
06	1280k to 1408k	System RAM
07	1408k to 1536k	System RAM
08 to 7D	no access	Page Invalid
7E	I/O Devices	I/O Space
7F	ROM & MMU	Special I/O Space

Note: The system RAM memory configures from the 1-megabyte boundary in both directions.

Figure 2-5. Initial MMU Configuration Example

RAM continues to be accessible via the MMU whenever address bit 14 is high while in setup mode. Thus any access to a location whose address has bit 14 asserted will result in the MMU performing an address transformation, just as in normal processing. By utilizing this feature, it is possible to access both normal, mapped address space and non-mapped special I/O space under control of program addressing. In the former case, such as during an access to RAM, A12 is asserted. In the latter, such as during an MMU register access, A12 is deasserted.

A program which alters any of the MMU register contents will typically be run only in supervisor mode.

2.3.4 System Contexts

To permit fast switching among program environments, the LISA MMU provides four contexts in which programs may run. The context in which the system is currently running is given by two control bits SEG1 and SEG2. The operating system typically runs in context 0. User programs execute in one of the other three contexts. When transfer of control to the system and back is required, such as might happen for interrupt handling, the SEG bits are configured to select the new context. Since the MMU has completely independent sets of SOR and SLR registers for each context, context maps are independent of each other.

These bits are located on the processor board and modified as described in subsection 2.5.5. Context is selected by configuring the SEG1 and SEG2 bits to give the required context as shown below:

SEG2	SEG1	Context
0	0	0
0	1	1
1	0	2
1	1	3

Context 0 is intended for exclusive use of the operating system, while contexts 1, 2 and 3 are intended for general purpose use. The LISA will automatically select context 0 whenever an access is made in supervisor mode. Thus a TRAP instruction may be used to generate a call from a user process to the operating system.

The context system is implemented by means of four sets of

hardware registers associated with the MMU. The SEG1 and SEG2 bits are normally manipulated only in supervisor mode. The operating system selects the context which is loaded into these two bits by the instruction.

If the context is changed while operating in context 0, the system begins execution in the new context with the instruction which follows that which changed the context. If context is changed in any other context, execution in the new context begins after exit from the operating system.

The context is loaded by a read or write to certain addresses in I/O space, as follows:

00E00AH	set SEG1
00E008H	reset SEG1
00E00EH	set SEG2
00E00CH	reset SEG2

2.4 Addressing in Special I/O Space

In Special I/O space, it is misleading to talk in terms of the memory maps that are used in normal memory space. Rather, the address word in Special I/O space has two separate significances, depending on the state of bits 14 and 15.

The word is divided into a number of fields. Either the segment number used to address an MMU register will be present in bits 17 thru 23 or a ROM address will be present in bits 1 thru 13, but not both.

The exact significance of the bits is shown in Figure 2-3 above.

The format of a word which is used to alter an MMU register is:

SSSSSSS010xxxxxxxxxx1xxx

The S designates the bits which select the segment for which the registers are to be altered. The x indicates a "don't care" condition.

When the ROM is to be addressed, the word has the format:

xxxxxxx000RRRRRRRRRRRRR (in setup mode, A12=0)

OR

SSSSSSS000RRRRRRRRRRRRR (via the MMU)

Each x bit is ignored. The S bits are the address of the segment that points to special I/O space. The R bits are used as an address for the boot memory directly. That is, they are not translated by the MMU.

A program which alters any of the MMU registers should only be run in supervisor mode.

2.5 System I/O Map

As outlined in Chapter 1, the LISA system contains memory-mapped I/O and an additional Special I/O space which is invoked only at powerup time and during accesses to the MMU registers.

A full list of the I/O address significances within the LISA is given here, along with the bit significance of the data written to and read from each address. An overview of the full I/O space map is given in Figure 2-6.

(Insert Figure 2-6)

2.5.1 Floppy Disk Control

The Floppy Disk Controller is located on the I/O board and is controlled by addressing the portion of physical I/O space in the range FCC001-FCC7FFH. This area contains command and status data as described below.

The Floppy Disk Controller actually consists of a 6504-based microcomputer, which has 4 Kbytes of program ROM for its own exclusive use and 1 Kbyte of buffer RAM which is shared with the main CPU. This RAM is provided with power backup by means of a battery system. Parameters stored in the FD Controller RAM are therefore not lost during power down.

The low 16 words of the 6504 address space are treated as a command block. The first byte is used for communication between the CPU and the 6504. The others are used to pass parameters for use in defining command data and status.

Controller commands are written to FCC001H and have the significance shown in Figure 2-7.

(Insert Figure 2-7)

The main part of the dedicated 6504 code consists of a Read/Write/Track/Sector (RWTS) routine. This utilizes a command block in the 8 bytes of memory which should be configured by the CPU in accordance with Figure 2-8.

Address	Function
000000-001FFFH	Expansion slot #1 Low Decode
002000-003FFFH	" " " High Decode
004000-005FFFH	Expansion slot #2 Low Decode
006000-007FFFH	" " " High Decode
008000-009FFFH	Expansion slot #3 Low Decode
00A000-00BFFFH	" " " High Decode
FCC001-FCC7FFH	Floppy Disk Control (see 2.5.1)
00D000-00D3FFH	Serial Ports Control (see 2.5.2)
00D400-00D7FFH	9512 Floating Point (see data sheet)
00D800-00DBFFH	Parallel Port Control (see 2.5.3)
00DC00-00DFFFH	Keyboard/Mouse Control (see 2.5.4)
00E000-00E01EH	CPU board Control (see 2.5.5)
00E01F-00E7FFH	(not used)
00E8xxH	Video Address Latch
00F0xxH	Memory Error Address Latch
00F8xxH	Status Register

Figure 2-6. System I/O Space Overview

Code	Operation
81H	Execute the RWTS routine (parameters are given by FCC003-FCC00FH)
82H	Not used
83H	Seek to side/track
84H	JSR to routine pointed to by 00C003-5
85H	Clear Interrupt Status
86H	Set Interrupt Mask
87H	Clear Interrupt Mask
88H	Wait in ROM until called to do cold start
89H	Loop in ROM

Figure 2-7. Floppy Disk Commands

(Insert Figure 2-8)

The disk drives generate an interrupt to the CPU whenever a disk is inserted or removed. An interrupt is also generated upon completion of an "81H" command. The status of the controller can be found by examining location FCC07FH. Note that the interrupt flag must first be enabled or a bus error will occur. The enable bit must be high in order to be able to access the Floppy RAM which is shared by the FD Controller and the processor board. The interrupt source is identified by this status byte, the bit interpretation being coded according to Figure 2-9.

(Insert Figure 2-9)

The disk controller has an area of memory which may be used for CPU storage of parameters. It is located between FCC181H and FCC1FFH.

The memory area used for information transfer to and from the disk controller is shared by the CPU and the 6504 and is located between FCC501H and FCC7FFH.

2.5.2 Serial Port Control

The serial logic interface is implemented by means of a SCC dual channel device, which is described in the 8530 SCC device manual.

The two serial interfaces in the LISA are accessed via the peripheral control device by accessing four distinct addresses in I/O space, as shown below:

Channel A	Data:	$00D247
	Control:	$00D243
Channel B	Data:	$00D245
	Control:	$00D241

Address	Operation
FCC003H	Command Code 00H Read 01H Write 02H Unclamp 03H Format 04H Verify 05H Format Track 06H Verify Track 07H Read (without checksum verify) 08H Write (without checksum)
FCC005H	Drive Select 00H Drive 2 (lower) 80H Drive 1 (upper)
FCC007H	Side Select 0xH Side 1 (upper) 1xH Side 2 (lower)
FCC009H	Sector Number (0 to 22)
FCC00BH	Track Number (0 to 44)
FCC00DH	Speed Byte
FCC00FH	Format Confirmation Byte
FCC011H	Error Status
FCC013H	Disk ID Value

Figure 2-8. Floppy Disk Command Block

Bit	Significance
7	Set if bits 4, 5 or 6 set
6	Set if RWTS complete for Drive 1
5	Set when button on Drive 1 is pushed
4	Set when disk in place on Drive 1
3	Set if bits 0, 1 or 2 set
2	Set if RWTS complete for Drive 2
1	Set when button on drive 2 is pushed
0	Set when disk in place on Drive 2

Figure 2-9. Floppy Disk Interrupt Source

The baud rate for each of the two channels is defined in terms of two time constants, which must be loaded into the SCC device. The time constants are governed by the formulae:

TC(A) = 4,000,000/(2xBaudrate) - 2

TC(B) = 3,686,400/(2xBaudrate) - 2

This results in a table of baud rate values shown in Figure 2-10.

(Insert Figure 2-10)

The serial ports use autovectoring, which eliminates the need for the SCC to supply interrupt vectors to indicate the source of the interrupt to the CPU.

2.5.3 Parallel Port Control

The parallel port is controlled by a 6522 Versatile Interface Adapter (VIA). There is a direct correspondance between the hardware lines on the physical connector and the assigned line within the 6522's two-byte ports. Refer to Subsection 3.5.2 for a discussion of the signal lines on the interface. The relationship between the 6522 port bits and the interface signals is shown in Figure 2-11.

(Insert Figure 2-11)

Note that some bits on this 6522 are used for signals other than those for the parallel port. Note also that two bits for the parallel port are controlled via the keyboard 6522 device. The programming of the 6522 device is described in the 6522 data sheet. The device addressing scheme is given in Figure 2-12.

(Insert Figure 2-12)

If CA1 is in pulse handshake mode and the DEN bit is low, the CA1 line pulses to transfer data to or from the parallel port each time that data is read from or written to the A port. CA1 is fed directly to CA2 to allow latch mode to be used on the A port while data is being read.

Baud Rate	Clock Multiplier	TC(A)	Error (%)	TC(B)	Error (%)
19200	16	--	--	4	0
9600	16	11	-0.16	10	0
4800	16	24	-0.16	22	0
2400	16	50	-0.16	46	0
1200	16	102	-0.16	94	0
300	16	414	-0.16	382	0
110	16	1134	-0.03	1045	-0.026042
19200	1	102	-0.16	94	0
9600	1	206	-0.16	190	0
4800	1	414	-0,16	382	0
2400	1	831	-0.04	766	0
1200	1	1664	-0.04	1534	0
300	1	6664	-0.01	6142	0
224000(Applebus)	1	--	--	6	0

Figure 2-10. Serial Port Baud Rates

6522 Controller line		Parallel Port line		Pin
PA0-PA7	Peripheral A port	DD0-DD7	Data Lines	
CA2	Control Line 2 A	PSTRB/	ProcessorStrobe	15
CA1	Control Line 1 A	BSY	Busy	16
PB0	Periph. B Port 0	OCD	Open Cable Detect	19
PB1	Periph. B Port 1	BSY	Busy	16
PB2	Periph. B Port 2	DEN	Disk Enable	-
PB3	Periph. B Port 3	DRW	Read/Write	3
PB4	Periph. B Port 4	CMD/	Command	17
PB5	Periph. B Port 5	DIAGPAR	Diagnostic Parity	-
PB2	Control Line 2 B	PARITY/	Interface Parity	18
(PB5)	Keyboard B Port 5	PRES/	Parity Reset	-
(PB7)	Keyboard B Port 7	CRES/	Controller Reset	21
(PAx)	Keyboard A Port x	CHK	Check	25

Notes: The last three signals are connected to the keyboard 6522 device.

The BSY signal connects to both the CA1 and PB1 lines.

Figure 2-11. Parallel Port Bit Correspondance

Address	Register #	Function
00D901H	0	ORB/IRB (Input/Output Register)
00D909H	1	ORA/IRA (Input/Output Register)
00D911H	2	DDRB (Data Direction Register)
00D919H	3	DDRA (Data Direction Register)
00D921H	4	T1C-L (Low-order Latch/Counter)
00D929H	5	T1C-H (High-order Counter)
00D931H	6	T1C-L (Low-order Latches)
00D939H	7	T1C-H (High-order Latches)
00D941H	8	T2C-L (Low-order Latch/Counter)
00D949H	9	T2C-H (High-order Counter)
00D951H	10	SR (Shift Register)
00D959H	11	ACR (Auxiliary Control Register)
00D961H	12	PCR (Peripheral Control Register)
00D969H	13	IFR (Interrupt Flag Register)
00D971H	14	IER (Interrupt Enable Register)
00D979H	15	ORA/IRA (as for 1 w/o handshake)

Figure 2-12. Parallel Port Addressing

The CR/ signal is generated by manipulation of the B port on the keyboard interface. Refer to Subsection 2.5.4 for details.

2.5.4 Keyboard/Mouse Control

The keyboard/mouse control is performed by a dedicated slave processor, known as a COPS. It provides communication with four peripheral devices via the A port of the keyboard 6522 VIA port controller. These devices are:

* The keyboard
* The mouse
* The real time clock
* The software power-off

Commands to these peripherals are written to the A port of the 6522 and data is fetched from the same location. The keyboard and mouse are addressed using the 6522 registers as shown in Figure 2-13.

(Insert Figure 2-13)

The abbreviations used in Figure 2-13 refer to registers within the 6522 device, similar to Figure 2-12. The device is described in the 6522 data sheet.

The command format to the COPS is shown in Figure 2-14.

(Insert Figure 2-14)

Note that, in addition to the keyboard and mouse, several other peripherals are interfaced to the system via the keyboard 6522 device. These are summarized as:

* Three parallel port lines
* Three video contrast lines
* Speaker tone line
* Floppy disk interrupt

The COPS receives power from the backup supply. This voltage is available at all times, whether the system is powered down or even unplugged. The only time the COPS will cease functioning is if the battery is allowed to run down by having the system unplugged over a long period.

Address	6522 Register #	Function
00DD81H	0	ORB/IRB
00DD83H	1	ORA/IRA
00DD85H	2	DDRB
00DD87H	3	DDRA
00DD89H	4	T1C-L
00DD8BH	5	T1C-H
00DD8DH	6	T1C-L
00DD8FH	7	T1C-H
00DD91H	8	T2C-L
00DD93H	9	T2C-H
00DD95H	10	SR
00DD97H	11	ACR
00DD99H	12	PCR
00DD9BH	13	IFR
00DD9DH	14	IER
00DD9FH	15	ORA/IRA (Same as in register 1 but without handshak

Refer to 6522 Data Sheet for details

Figure 2-13. Keyboard/Mouse Addressing

PA7-PA0	Function
0000 0000	Turn I/O port on
0000 0001	Turn I/O port off
0000 0010	Read Clock Data
0001 nnnn	Write nnnn to clock
0010 spmm	Set Clock Modes, where: s=enable (1) or disable (0) clock set mode p=power on (1) or off (0) mm = 00 Clock/Timer Disable 01 Timer Disable 10 Timer Underflow Interrupt 11 Timer Underflow Power-On
0011 nnnn	Write nnnn to low KBD indicator bits
0100 nnnn	Write nnnn to high KBD indicator bits
0101 nnnn	Set NMI character high nibble to nnnn
0110 nnnn	Set NMI character low nibble to nnnn
1xxx xxxx	No operation

Figure 2-14. Keyboard COPS Commands

This means that the COPS is always operational. It is therefore particularly useful as a device for monitoring real elapsed time and also for providing software control of the power on and off functions.

Keyboard

The keyboard on the LISA is a true N-key rollover design. An arbitrary number of keys can be depressed without causing phantom key problems. The key codes returned by the interface are in the form:

drrr nnnn

where d indicates direction of keystroke (down=1, up=0), and rrr and nnnn are given in Figure 2-15.

(Insert Figure 2-15)

System software must interpret such functions as shift and auto-repeat. Any key can be programmed to generate a non-maskable interrupt.

In addition to key information, the COPS resident in the keyboard itself produces a number of two-byte sequences which are known as reset codes. Each sequence consists of a resetr character (80H), followed by a code number. The significance of the code numbers is shown in Figure 2-16.

(Insert Figure 2-16)

Mouse

The mouse connects to the keyboard COPS device. Mouse commands have the format:

0111 ennn

If e is set, mouse interrupts are enabled. The n bits define the time interval which will separate mouse interrupts. The time interval in real time is this figure times 4 milliseconds. Whenever the mouse moves, it will interrupt the processor with this period.

Mouse data is transferred to the CPU in three bytes. These are polled from the keyboard 6522 A port. The significance of the bytes is as follows:

nnnn ↓ / rrr->	010	011	100	101	110	111
0000	CLEAR		_ -	(9	E	A
0001	/		+ =	) 0	© 6	@ 2
0010	*		EUROPEAN KEY	U	& 7	# 3
0011	=			I	* 8	$ 4
0100	7		P	J	% 5	! 1
0101	8		BACKSPACE	K	R	Q
0110	9			[	T	S
0111	-			]	Y	W
1000	4		RETURN	M	"	TAB
1001	5		0	L	F	Z
1010	6			: ;	G	X
1011	+			" '	H	D
1100	.		? /	SPACE	V	LEFT OPTION
1101	2		1	, <	C	ALPHA LOCK
1110	3		RIGHT OPTION	. >	B	SHIFT
1111	NUMERIC RETURN			O	N	COMMAND

NOTE: Final Diagram to be supplied by POS Engineering

Figure 2-15. LISA Keyboard Codes

Reset Code	Significance
FF	Keyboard COPS failure detected
FE	I/O Board COPS failure detected
FD	Keyboard unplugged. The reset code of the keyboard identification follows when the keyboard is plugged back in.
FC	Clock timer interrupt
FB	"Soft power off" switch has been depressed
FA) .) .) .) F0)	Reseved for future use
Ey	Clock data follows. Five bytes are transferred after this. "y" is the year, coded in the reset byte. The other bytes have the format: (80 Ey) dd dh hm ms st where ddd is the day, hh the hour, mm the minute, ss the second and t the tenths of a second.
DF) .) .) 00)	Keyboard ID number. This code is produced whenever the keyboard COPS is reset. At present, the only valid code is 01.

Figure 2-16. Keyboard COPS Reset Codes

00	Mouse data follows
dx	Change in x direction (-127 to 127)
dy	Change in y direction (-127 to 127)

Each time the value is accepted by the CPU, the bytes are reset. Should the CPU not respond immediately, the data is updated to show a cumulative value. The mouse button is returned as keycode d000 0110. The d bit defines whether the button is pressed (1) or not (0).

If the mouse is plugged in, a code of 1000 0111 will be returned. If the mouse is unplugged, the code will be 0000 0111.

Real Time Clock

The real-time-clock is capable of resolution to 1/10th of a second and need be reset only every 16 years. An alarm can be programmed via the RTC to generate an interrupt and/or sound an audible warning after a timeout of up to FFFFFH seconds, or about 12 days.

The clock commands are coded as shown in Figure 2-14. The p bit in Figure 2-14 is used to power the system on or off under software control. A "0" turns power off. The s bit enables and disables Clock Set Mode.

In Clock Set Mode, only as many nibbles as are required need be sent. Once the s bit is cleared, the peripheral assumes that the data was complete. The clock and timer must be stopped while the clock is being set. The clock can be left running while setting up the timer.

Time information is entered as a series of nibbles in the form:

aaaaa y ddd hh mm ss t

The a nibbles are the timer delay value in seconds (0-FFFFFH), y is the year (0-15), ddd is the day (1-366), hh is the hour (0-23), mm is the minute (00-59), ss is the second (0-59) and t is the 1/10th of a second value (0-9).

All nibbles are maintained in decimal format, except for the timer and year nibbles, which are binary. When reading the clock, the data is returned as a series of reset codes in the form:

80 Ey dd dh hm ms st

Software Power-Off

System power is under software control in the LISA. When the power switch on the lower front chassis is pressed during operation, a reset code is presented to the CPU. This allows system software to finish operations in progress and store work files before shutting down system power.

2.5.5 Processor Board Control

The processor board has a number of control bits which are set and reset by access to a particular address in I/O space. A summary of these is shown in Figure 2-17.

(Insert Figure 2-17)

Context selection is discussed in Subsection 2.3.4. Memory errors are discussed in Section 2.7.

The video address latch is used to point to the location in the 32K-byte video page in main memory for the next data byte which is to be sent to the video display circuits.

The memory error address latch is used to hold the address at which the system was processing when a memory error occurs. This may then be interrogated by system software for statistical analysis of memory errors which occur.

The status register is discussed in Section 2.8.

2.6 Interrupt Handling

The LISA interrupt structure takes advantage of the flexible structure available in the 68000 CPU. Interrupts may be generated by one of three sources:

* External devices
* System errors
* Program errors

Address	Function	
00E000H	Memory Diagnostic DIAG1	Reset
00E002H	" " "	Set
00E004H	Memory Diagnostic DIAG2	Reset
00E006H	" " "	Set
00E008H	Context Selection SEG1	Reset
00E00AH	" " "	Set
00E00CH	Context Selection SEG2	Reset
00E00EH	" " "	Set
00E010H	SETUP Register	Reset
00E012H	" "	Set
00E014H	Enable Soft Memory Error Detect	Reset
00E016H	" " " " "	Set
00E018H	Enable Vertical Retrace Intrpt	Reset
00E01AH	" " " "	Set
00E01CH	Enable Hard Memory Error Detect	Reset
00E01EH	" " " " "	Set
00E800H	Video Address Latch	
00F000H	Memory Error Address Latch	
00F800H	Status Register	

Figure 2-17. Processor Board Control Addressing

Upon detection of an interrupt, the CPU enters supervisor mode automatically. It then uses a table in memory, known as the Exception Vector Table to point to the location at which the routine to handle the interrupt can be found. The priority level of the source of the interrupt can be used as an index into the table, or the interrupt level itself may be used directly as the exception vector.

The fixed priority interrupts in the system are:

Level	Type
7	Non-maskable interrupt (highest)
6	Serial I/O ports
5	Expansion slot #1
4	Expansion slot #2
3	Expansion slot #3
2	Keyboard/Mouse/Real-Time-Clock/Power-on
1	All others (lowest)

Figure 2-18 shows the exception vector table assignment for the LISA system. All addresses are logical addresses. This means that their physical location is a function of the MMU setup.

(Insert Figure 2-18)

A non-maskable interrupt may come from one of four sources:

* Power fail
* Hard memory error
* Soft memory error
* Keyboard reset

Level-1 interrupts may be generated by one of three sources:

* Hard disk interface (the parallel port)
* Floppy disk controller
* Video circuit controller

The power reset vector is not shown here because it is located in the system ROM, which is not accessed except in Special I/O space during powerup processing.

Exception	Vector Address
Reset: Initial SSP	000000H
Reset: Initial PC	000004H
Bus Error	000008H
Address Error	00000CH
Illegal Instruction	000010H
Zero Divide	000014H
CHK Instruction	000018H
TRAP Instruction	00001CH
Privilege Violation	000020H
Trace	000024H
Unimplemented Instruction 1010	000028H
Unimplemented Instruction 1111	00002CH
Reserved, unassigned	000030 - 00005FH
Spurious Interrupt	000060H
Other Internal Interrupt	000064H
Keyboard Interrupt	000068H
Slot 2 Autovector	00006CH
Slot 1 Autovector	000070H
Slot 0 Autovector	000074H
RS232 Interrupt	000078H
Non-Maskable Interrupt	00007CH
TRAP Instruction Vectors	000080 - 0000BFH
Reserved, unassigned	0000C0 - 0000FFH
User Interrupt Vectors	000100 - 0003FFH

Figure 2-18. Exception Vector Table

2.7 Error Processing

The LISA system operates with a flexible system of hand-shaking on the bus. When a device is addressed, the CPU will wait 30-300 microseconds for some response from the addressed device before timing out. Upon timeout, control is vectored via the Exception Vector Table, shown in Figure 2-18.

Memory errors in the LISA system can be one of two kinds: hard or soft.

A hard memory error is the result of a parity error during memory access on a parity memory board or an uncorrectable error on an ECC memory board.

A soft memory error is the result of detection of a correctable error on an ECC memory board.

In either case, the appropriate status bit is set (see Section 2.8) and a non-maskable interrupt is generated to the CPU. A latch contains the address at which the error was detected. The MMU can be used to map out bad pages in memory, should this become necessary.

The address of the word which caused the error can be read from the Memory Error Address Latch at 00F000H in I/O space.

Detection of either a hard or a soft memory error can be disabled, as described in Figure 2-17.

2.8 System Status

The System Status Register is located at 00F800H in I/O space and is a read-only 16-bit register. A bus error exception routine can use the status register to determine the cause of bus errors.

A breakdown of the significance of the bits in the System Status Register is shown in Figure 2-19.

(Insert Figure 2-19)

Bit	Name	Significance
0	Soft Error	A soft memory error has occurred.
1	Hard Error	A hard memory error has occurred.
2	Vertical Retrace	The video circuit has begun a vertical retrace and an interrupt has been generated. The video circuit continues to set this bit for 90 microseconds after the start of the retrace. Enable Vertical Retrace Interrupt can be reset to inhibit this bit.
3	Bus Timeout	A timer attached to AS/ (Address Strobe) waits for 30-300 microseconds before generating a Bus Error condition.
4	Video Bit	Available to the CPU for diagnostic purposes, this bit corresponds to the output of the video circuit.
5	Horiz. Sync	Reflects the state of the horizontal sync signal. It is available to the CPU for diagnostic purposes.
6	Video Mode	Reserved for future use.
7-15		Not used.

Figure 2-19. System Status Register

CHAPTER 3

SYSTEM PARAMETERS

This chapter describes specifications for the LISA and the manner in which it interfaces with the outside world.

3.1 System Packaging

The configuration of the components within the LISA package has been discussed briefly in Chapter 1. The following components are detachable from the system for inspection or replacement:

* Front panel cover
* Floppy disk drives
* Rear panel cover
* Power supply
* Motherboard
* CPU board
* I/O board
* Memory boards
* Keyboard
* Mouse
* Expansion boards

Disassembly procedures for user-servicable parts are described in the user documentation. Access to other system assemblies is described in Chapter 11.

The top front of the chassis is taken up by the CRT monitor and the two floppy disk drives. Access to these devices may be obtained by removing the system front panel. The drives are held in place by a finger-nut below the lower drive, and both drives may be slid out once this is undone. Care must be taken not to snag or overextend the drive cables before these are removed.

From the rear of the chassis, removal of the rear cover gives access to the power supply and the main motherboard assembly. The motherboard carries all the logic printed circuit boards and conceptually consists of two parts.

The first part carries boards that are parallel to the back of the unit. These are the main logic components of the system; they include the Processor board, the I/O board and either one or two memory boards. Not all of these are immediately visible from the back of the unit as they are arranged one behind the other.

The second part carries the boards at right angles to the rear of the unit, and is known as the expansion bus section. This is where additional boards, such as interface or controller boards, are inserted in the LISA system. The entire motherboard may be slid out from the chassis by gently pulling to the rear, which disengages the two edge connectors through which the motherboard connects into the system. It is not necessary, however, to remove the whole card assembly to remove one of the boards in the expansion slots. These are held in place by special card edge connectors which allow the boards to slide out towards the rear of the unit.

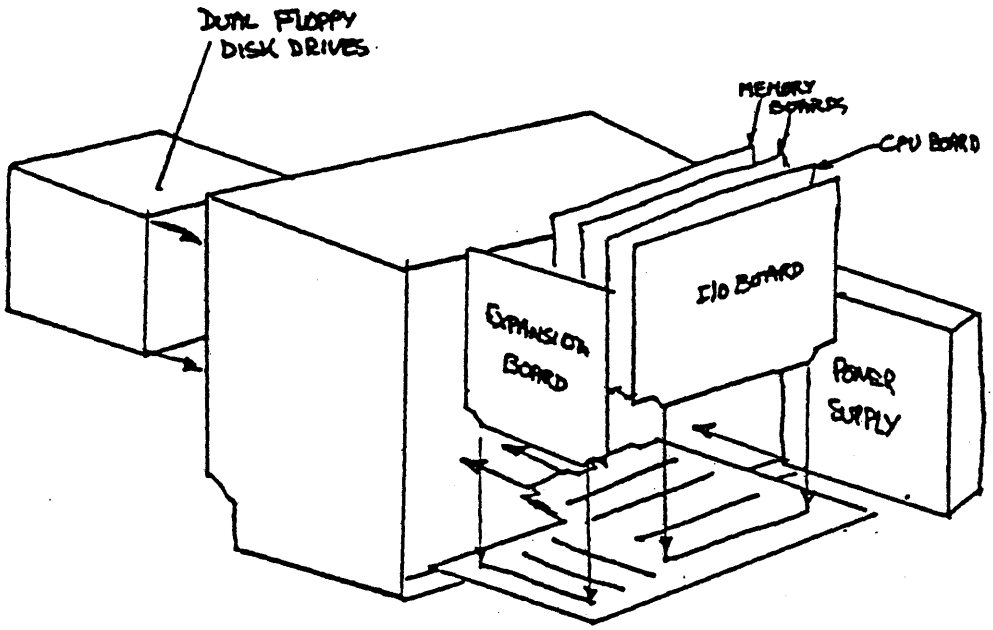
The power supply is the rectangular enclosure occupying the right side of the chassis, and can be removed separately from the other components. To do this, the finger-nut beneath the unit should be unfastened, and the whole power supply may then be slid gently backwards out of the chassis.

Electrical connections between components and the rest of the system are made by means of tongue and socket connectors. These are made automatically when the components are replaced in the system and pushed home. Only the floppy disk drives require their connecting cable to be carefully removed before the unit can be fully removed from the system.

Refer to Figure 3-1 for an exploded view of the system and the connections to the various system components.

(Insert Figure 3-1)

No component should be removed from the system when the power is on. There are interlock switches on both the front and rear panels which inhibit power to the system components when any panel is removed.



All components except the disk drives have plug-in connections.

Figure 3-1. System Component Exploded View

The three expansion slots to the right-rear of the unit are designed to accept add-on logic boards. These may be used to expand on the basic system by adding such features as a custom interface to another system or a specialized controller to a peripheral which does not readily interface with either of the ports available. Such expansion boards must be compatible with the specification for the expansion bus, given in Section 3.4.

Expansion boards are easily removed from the system with the end-opening connectors used to house them. The lever for each slot is turned one quarter turn counterclockwise, and the board can be slid out of the connector. This avoids the need to remove the entire motherboard assembly when access to one of the expansion boards is required.

3.2 System Specifications

This section specifies environmental, electrical and performance parameters in the LISA system. Interfaces to the LISA are defined in later sections of this chapter.

3.2.1 Environmental Specification

The LISA system has been designed to operate in an office environment. The purpose of this section is to define environmental limits for the unit which, if exceeded, may result in system malfunction.

Note that the data apply only to the basic LISA system. Additional equipment, such an external hard disk or printer are specified separately in the relevant documentation.

Operating Temperature	0 to 40 Degrees C
Operating Humidity	10% to 80% (non-condensing)
Storage Temperature	-20 to 70 Degrees C
Storage Humidity	0% to 90% (non-condensing)

3.2.2 Physical Specification

These dimensions apply to the basic LISA system, which includes both mouse and keyboard, but not such additions as a printer and a hard disk drive unit.

Main Assembly Dimensions	13.9" (354mm) High 18.6" (474mm) Wide 15.6" (396mm) Deep
Keyboard dimensions	3.1" (79mm) High 18.8" (479mm) Wide 6.5" (166mm) Deep
Mouse operating space	2.1"x6.3" (55mmx160mm)
Keyboard cable extension	4ft. (1.2m) maximum
Main assembly weight	44.81bs (20.4Kg)
Keyboard weight	4.131bs (1.88Kg)
Power cord length	7.5ft. (2.26m)

The LISA should be used with an acceptable operating space around it. Under no circumstances should the air flow through the chassis vents, particularly those on the bottom, be restricted.

The mouse operating space should be approximately 6" from the side of the LISA and 6" in from the edge of the work surface for ease of operation. The choice of side is open.

3.2.3 Electrical Specification

These values apply to the basic LISA system without hard disk or printer.

AC power requirements	150VA @ 115VAC (single phase)
Acceptable input voltages	90 to 130VAC
Input AC frequency	60 +/- 2 Hz
Maximum power dissipation	160 watts @ 70 deg.F
Voltages available on bus	+5V,-5V,+12V,-12V, +5VSTBY DC

The currents available on these voltages is a function of the system configuration. Refer to Subsection 3.3.2 for the total power capacity of the power supply.

3.3 System Components

The components of the LISA system have been engineered to provide a highly modular system. They may easily be dismounted from the chassis for test or replacement. The LISA system consists of the following component assemblies:

* Main chassis assembly
* CRT screen assembly
* Power supply assembly
* Motherboard assembly
* Dual floppy disk drive assembly
* Video board
* Processor board
* I/O board
* 2 memory boards (maximum)
* Keyboard assembly
* Mouse assembly
* Switch/Disk cable assembly
* Power supply harness

Refer to Chapter 11 and Appendix H for details.

3.3.1 Main Chassis

The main chassis of the LISA consists of the sheet metal frame plus the plastic cladding parts. In addition to this, the following components are not easily accessed and may be considered as a part of this assembly.

* CRT monitor assembly
* Switch/Disk cable assembly
* Power supply harness

The general view of the main chassis with these components is shown in Figure 3-2.

(Insert Figure 3-2)

3.3.2 Power Supply

The LISA power supply is a self-contained modular unit, located in the right rear of the main chassis assembly. The power supply weighs approximately 3.5lbs and supplies the following voltages to the LISA system:

+5V	@	8.0 Amps
-5V	@	0.2 Amps
+12V	@	2.0 Amps
-12V	@	0.2 Amps
+33V	@	0.6 Amps
+5STBY	@	0.1 Amps

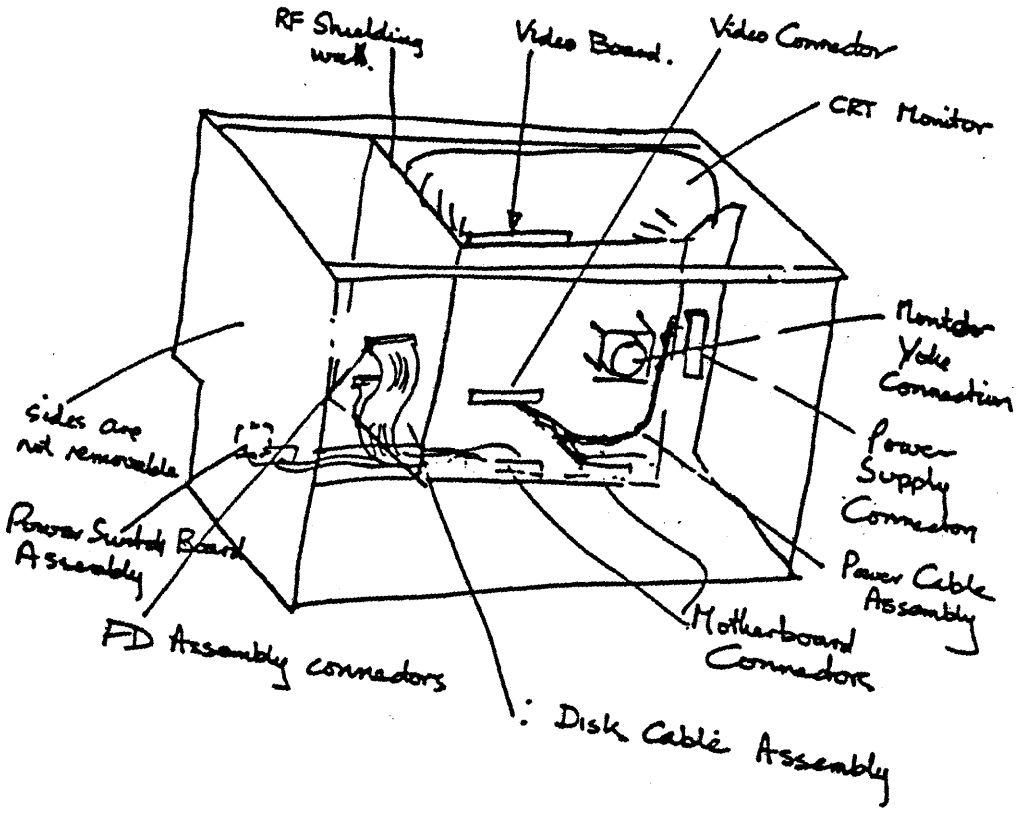


Figure 3-2. Main Chassis Assembly

3.3.3 Floppy Disk Units

The floppy disk assembly in the LISA consists of a dual floppy disk drive assembly. This attaches to the main chassis by being slid into the upper right front. Before the drives are inserted in the system, the disk cable must be connected to the rear of both floppy disks in the drive assembly. The longer cable goes to the upper drive.

The assembly is held in place by a finger screw. It can be accessed by removal of the front cover of the LISA.

3.3.4 Printed Circuit Boards

The printed circuit boards in the LISA are physically configured to fit the chassis assembly. Their dimensions and connector locations are shown in Figure 3-3.

(Insert Figure 3-3)

The circuit boards are keyed such that it is not possible to insert a board in the incorrect slot. For this reason, care should be taken not to force a board into a slot. The extraction handles of all logic boards in the LISA are color-coded to illustrate the correct slot and orientation.

3.3.5 Keyboard and Mouse Assemblies

The keyboard is a stand-alone component which connects to the switch assembly at the lower right of the main chassis. It receives its power input and transmits key data down this cable. The keyboard assembly consists of a single PCB which carries all keys and logic components, sandwiched between the two halves of the plastic housing.

The mouse is a stand-alone component which connects to the special 9-pin D-connector at the center rear of the motherboard.

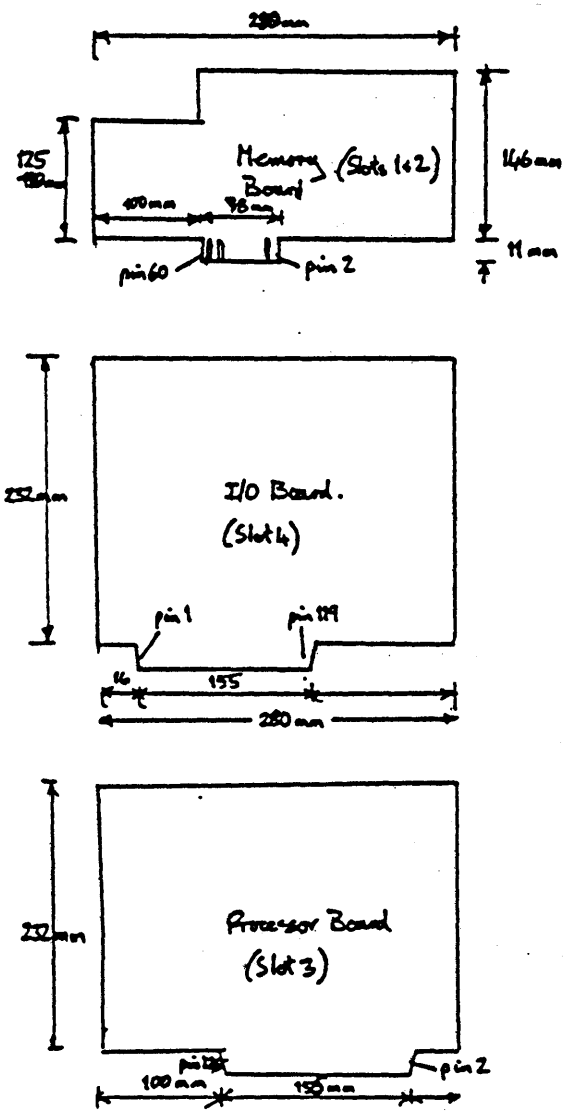


Figure 3-3. Circuit Board Dimensions

3.4 The Expansion Bus

A subset of the internal system bus is made available on three slots in the motherboard. These are accessible from the rear of the system when the rear panel cover is removed. They are equipped with end-opening connectors, which allow expansion PCB's to be inserted or removed from the system without requiring removal of the motherboard from the main chassis. However, the AC line cable should be disconnected whenever an expansion board is being removed or inserted.

The purpose of this section is to provide a specification of the expansion bus and its physical configuration to permit an interface to be designed which will plug into the expansion bus.

Software to handle such a component must also be generated. The generation of such software lies beyond the scope of this manual. Refer to Chapter 2 above and the documents listed in the Preface for assistance.

3.4.1 Bus Signal List

The expansion bus is an extension of the system bus. It provides sufficient data, address and control lines to enable peripherals in addition to those implemented on the processor and I/O boards to operate within the LISA system environment.

Many signal names will be recognized as corresponding to those available on the 68000 processor chip. In all such cases, these are simply buffered versions of the 68000 signal, with the function being identical to the original. Refer to the 68000 User's Manual for details of individual signals.

Other signals, such as the slot high and low decode signals are generated or received by the processor board logic. A diagram of the signal layout on the connector is shown in Figure 3-4.

(Insert Figure 3-4)

Front of machine

+5 Volts	!	56	!	55	!	+5 Volts
Digital Ground	!	54	!	53	!	Digital Ground
+5 Stdby	!	52	!	51	!	SPKRIN
UDS/	!	50	!	49	!	LDS/
READ	!	48	!	47	!	AS/
DTACK/	!	46	!	45	!	+12 Volts
VPA/	!	44	!	43	!	VMA/
BA12	!	42	!	41	!	BA11
BA10	!	40	!	39	!	BA9
BA8	!	38	!	37	!	BA7
BA6	!	36	!	35	!	BA5
BA4	!	34	!	33	!	BA3
BA2	!	32	!	31	!	BA1
BD0	!	30	!	29	!	BD1
BD2	!	28	!	27	!	BD3
BD4	!	26	!	25	!	BD5
BD6	!	24	!	23	!	BD7
BD8	!	22	!	21	!	BD9
BD10	!	20	!	19	!	BD11
BD12	!	18	!	17	!	BD13
BD14	!	16	!	15	!	BD15
BGout	!	14	!	13	!	BGin
BR	!	12	!	11	!	E
BGACK/	!	10	!	09	!	LDMA/
CPUCK	!	08	!	07	!	RESET
IAKn/	!	06	!	05	!	INTn/
SHn/	!	04	!	03	!	SLn/
-12 Volts	!	02	!	01	!	-5 Volts

Back of the machine

Figure 3-4. Signal Pin Layout

3.4.2 Bus Signal Descriptions

BD0-BD15 These 16 buffered data lines are the system data bus. The bidirectional lines are connected to pullup resistors on the motherboard to ensure a defined state when not being actively driven. BD0-BD7 are driven when LDS/ is asserted. BD8-BD15 are driven when UDS/ is asserted.

BA1-BA12 These 12 buffered address lines select one of 4096 words in either the high or low area of memory. The area in question is defined by the SHn/ or SLn/ signals. Each expansion card may therefore have a maximum memory size of 8192 words or 16384 bytes. Since the lines are derived from the low-order 12 lines from the MMU, a process which is assigned a segment enclosing the 16384 bytes on an expansion card can address the I/O card from 0-3FFFH. The slot location is unimportant.

AS/ This signal is the address strobe which indicates that the CPU has initiated a memory cycle. Due to the MMU delay on the processor board, only bits BA1 to BA8 are definitely stable at this time; the high-order 4 bits may still be changing.

UDS/ Upper Data Strobe indicates that, during a write operation, the upper byte on the bus (BD8-BD15) is active in the current bus cycle.

LDS/ Lower Data Strobe indicates that, during a write operation, the lower byte on the bus (BD0-BD7) is active in the current bus cycle.

DTACK/ Data Transfer Acknowledge indicates to the CPU that the expansion device has performed whatever data transfer had been requested by the CPU and that the current cycle can be completed.

READ This signal indicates the direction of data transfer to be performed on the buffered data lines. The signal being asserted indicates that the CPU expects the I/O device to present data on the bus.

VPA/ Valid Peripheral Address indicates to the CPU that the device currently being addressed operates with a 6800-compatible bus cycle. VPA/ must never be asserted concurrent with DTACK/.

VMA/ Valid Memory Address signals the peripheral that the CPU has recognised the VPA signal and is now executing a 6800 cycle.

E This is the equivalent of the 6800 phi2 clock. It is high for 4 clock cycles and low for 6, giving E a frequency of 500 KHz in the LISA system.

BR/ Bus Request tells the processor that a peripheral device is requesting control of the bus.

BGin/ A Bus Grant-in is issued by the CPU once a DMA device has been given control of the bus. If the expansion card had requested the bus and no higher-priority peripheral controls it, this signal allows the card to assume control of the bus.

BGout/ A Bus Grant-out reflects the condition of BGin if the peripheral does not wish to use the bus.

BGACK/ Bus Grant Acknowledge is driven by the expansion card when it assumes control of the bus and is de-asserted only when it wishes top relinquish control.

LDMA/ Load DMA is used to load the high address of the DMA latch. Due to the number of bus lines available, the high 8 address bits are latched on the CPU board from the contents of the 8 bits (BD5-BD12). The expansion device must control both the signal and the contents of the latch, which must be loaded at the beginning of any DMA transfer.

CPUCK This is a buffered 5MHz CPU clock, which is available for general timing use.

RESET/ When this signal is asserted by the CPU board, all peripheral devices must return to their power-on state.

+5Stdby This is a +5 volt source that is drawn from a battery, and is thus available even when system power is off. No more than 40mA should be drawn at any time, and this source should never be used when normal system power is available.

INTn/ This signal is used by the expansion device to interrupt the CPU. It should be held asserted until the interrupt is acknowledged from the CPU.

IAKn/ This signal is used to acknowledge an interrupt made by a peripheral device.

SLn/ This signal is used by the CPU to select the low-order contiguous 4096 words on the expansion device that are addressed by BA1-BA12.

SHn/ This signal is used by the CPU to select the high-order contiguous 4096 words on the expansion device that are addressed by BA1-BA12.

3.4.3 Bus Parameters

The expansion bus provides five DC voltages to devices which may be connected there. The total current which may be drawn on them for all devices connected to the bus is as follows:

+5 VDC	2.0 A
-5 VDC	0.075 A
+12 VDC	0.83 A
-12 VDC	0.1 A
+5 VSTBY	0.040A (always available)

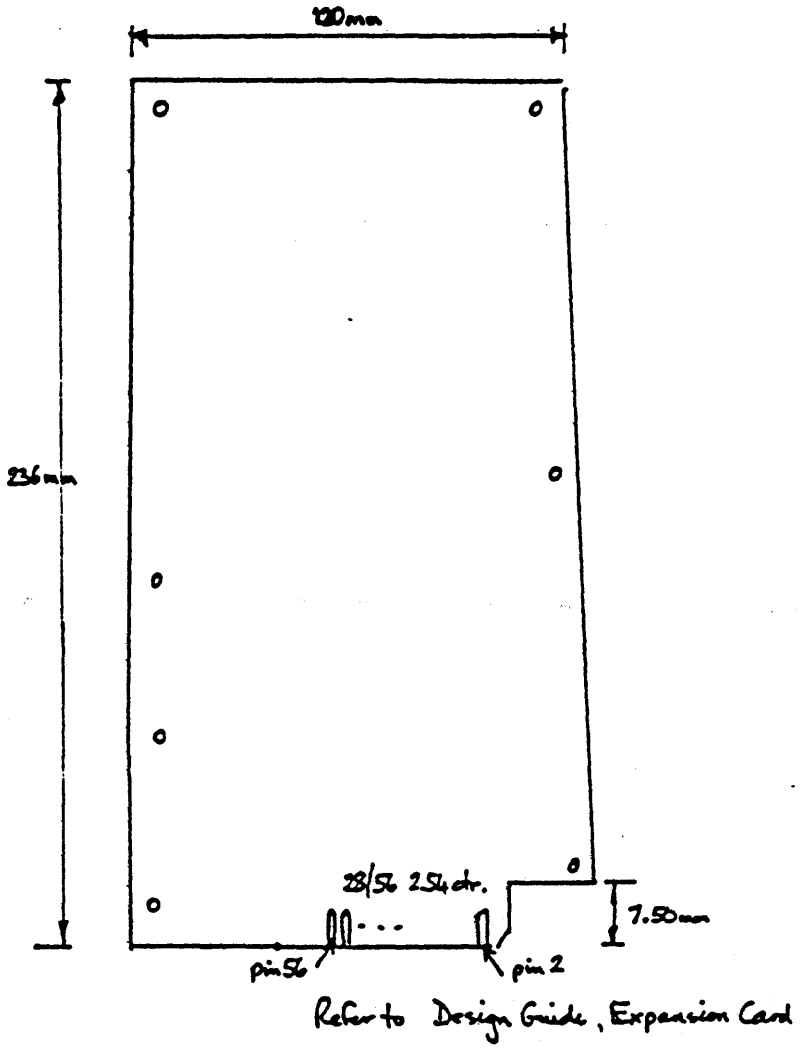
The +5VSTBY voltage is at a level of 5.7V whenever AC power is applied to the system. The mechanical layout of an expansion board must conform to the parameters shown in Figure 3-5.

(Insert Figure 3-5)

All signals on the expansion bus are TTL. Drivers to the bus are of the following types:

BA1-BA8	LS244
BA9-BA12	LS374/LS373
BD0-BD15	LS245
SHn,SLn	LS138
BGin, ...	Depends on next board
UDS,LDS,AS,READ,VMA,E	LS244
BGACK	F02
RESET	7417 (wired OR)
IAKn	LS156

All signals with an "n" are unique to the slot being used and need not be buffered. All other signals should be buffered on the expansion board to minimize loading on the bus itself.



Board thickness: 1.57mm
Board material: Glass epoxy
Finger material: Gold
Finger deposition thickness: 50 microns

Figure 3-5. Expansion Board Dimensions

Signals not mentioned above are input to the bus from the expansion board. A bus driver device should drive these.

3.4.4 Bus Timing

Timing on the expansion bus closely follows that of the 68000 CPU device. Refer to the 68000 User's Manual for details.

Expansion bus timing is controlled by the slot decode signals from the processor board and by the acknowledge signal from the controller on the expansion bus. Since the expansion bus is merely an extension of the system bus, signal timing is identical on both.

Normal data transfer on the bus begins with the address strobe signal being asserted. At this time, the bus address lines will not be valid due to time delays in the MMU. The slot decode signal will be asserted during the S5 state of the processor cycle after the address and data strobe lines are stable.

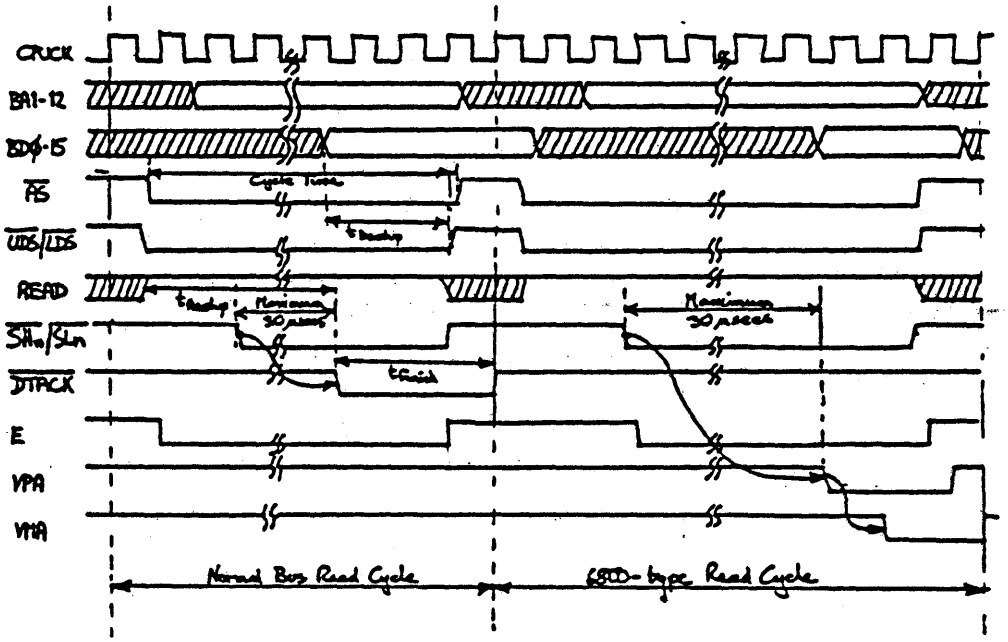
The signal sequence for a read operation from the expansion bus by the CPU is shown in Figure 3-6. The CPU waits for the DTACK/ signal from the addressed expansion peripheral before completing the cycling by reading the data from the data bus. Should the peripheral not respond, the CPU will time out after approximately 30 milliseconds with a bus error condition. This is shown in the first cycle of Figure 3-6.

(Insert Figure 3-6)

Data transfer from a 6800-type peripheral is performed with the assistance of the VMA and VPA handshake signals, plus the E clock signal. These signals are described in the signal list following Figure 3-5 and the 68000 User's Manual. The transfer cycle is similar to a normal data transfer with the VPA and VMA signals operating as handshake signals instead of SLn and DTACK.

Data is written to a peripheral in a similar manner. The slot decode being asserted indicates that valid data is being presented to the bus by the CPU. The DTACK signal acknowledges receipt of the data. This is shown in Figure 3-7, along with a 6800-type write cycle.

(Insert Figure 3-7)



	Min	Max
Cycle time	800ns	300us
TAsetup	100ns	--
TDsetup	100ns	--
Tfinish	100ns	260ns

Figure 3-6. Expansion Bus Read Timing Diagram

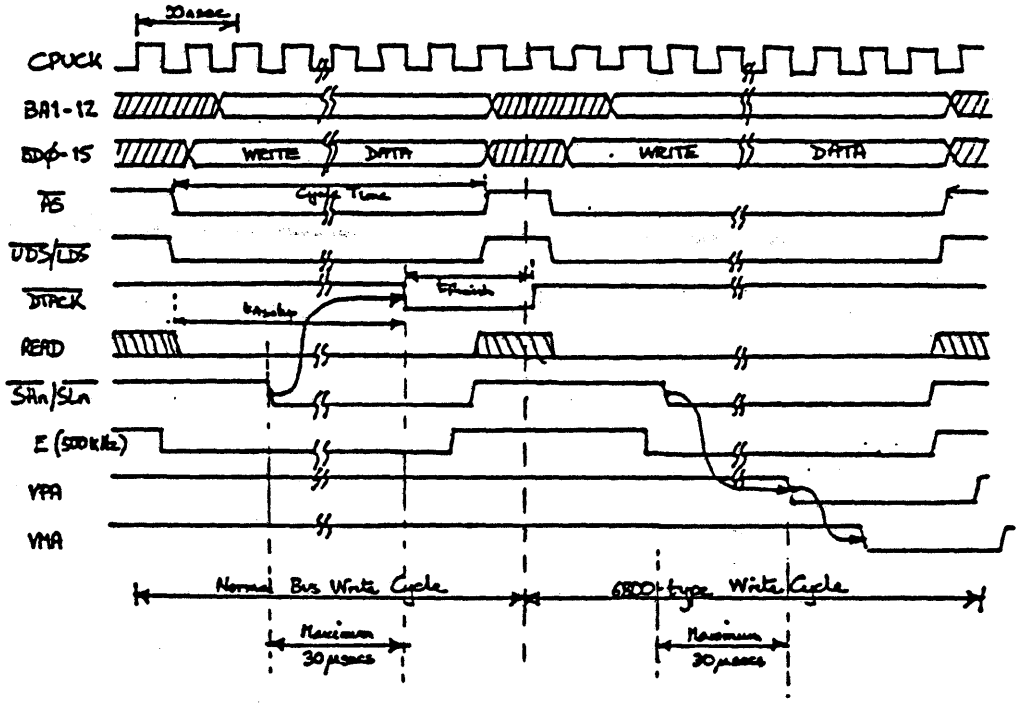


Figure 3-7. Expansion Bus Write Timing Diagram

Expansion peripherals normally use the slot decode to drive the acknowledge signal. Any peripheral using DMA must follow the timing described in the 68000 User's Manual.

3.4.5 DMA Scheme

The DMA scheme used in the LISA system corresponds closely with that used in the 68000 CPU. The BG lines are daisy-chained on the motherboard. The priority assigned to an expansion device is therefore a function of the interface design and the choice of physical location of the card in the expansion slots.

The hardware priority for DMA devices is:

Highest	I/O Board
	Slot 3
	Slot 2
Lowest	Slot 1

In order that the priority chain is not interrupted, any card which does not use DMA must hard wire its BGin signal to BGout.

Since this propagation will not occur if no card is present, it is essential that the slots using DMA are filled beginning with slot 3.

DMA transfers should be limited to 1 msec in order not to interfere with the processor's ability to proceed with normal program execution.

In addition to those lines mentioned in Subsection 3.4.2, an expansion device which uses DMA must also be capable of driving the following signals:

* All 16 data lines
* All 12 address lines
* AS,UDS,LDS and READ

Timing of these signals should follow those generated by the 68000 as given in the 68000 User's Manual and Figures 3-6 and 3-7.

The high-order 8 bits of the DMA address are held in a latch located on the processor board. This latch must be loaded by asserting the desired byte on BD5-BD12 and asserting LDMA/ before any transfer is attempted.

3.4.6 Bootstrap Protocol

If an expansion device is to be used to boot the operating system at power-on time, it must be self-identifying and an identification protocol must be followed.

Each device must contain ROM storage, the contents of which must be programmed to include the information shown in Figure 3-8.

(Insert Figure 3-8)

The first word of the ROM defines a type code. This code is a 16-bit female byte sex number with the most significant byte in location 0 abd the least significant byte in location 1. It has the following form:

bsit nnnn nnnn nnnn

where b = 1 if device is bootable
s = 1 if device has status program
i = 1 if device has an icon(s) to be displayed
t = 1 if device is a test card
n = device (or board) identification number

If the expansion device is selected for booting, the boot ROM will first check that the card is bootable by checking the b bit. If this bit is not set to a 1, the boot will be aborted and the boot ROM will display an error to the user.

If the status bit is on when the expansion device is selected for booting, the boot ROM will first execute the status program by using the status routine entry pointer. Register A1 will be loaded with the address of the expansion slot's low select (SLn) to enable the status and boot programs to access the device by addressing relative to A1. The status program must always return to the boot ROM with the result in register D0. A status of 0 will indicate that all is well, while a nonzero status will abort the boot and the boot ROM will display an error to the user.

The icon pointer provides a method for expansion devices to display to the user a boot option in a pictorial manner. If the icon bit is set to a 1, the boot ROM will scan the expansion device ROM using the icon pointer and expect the following format:

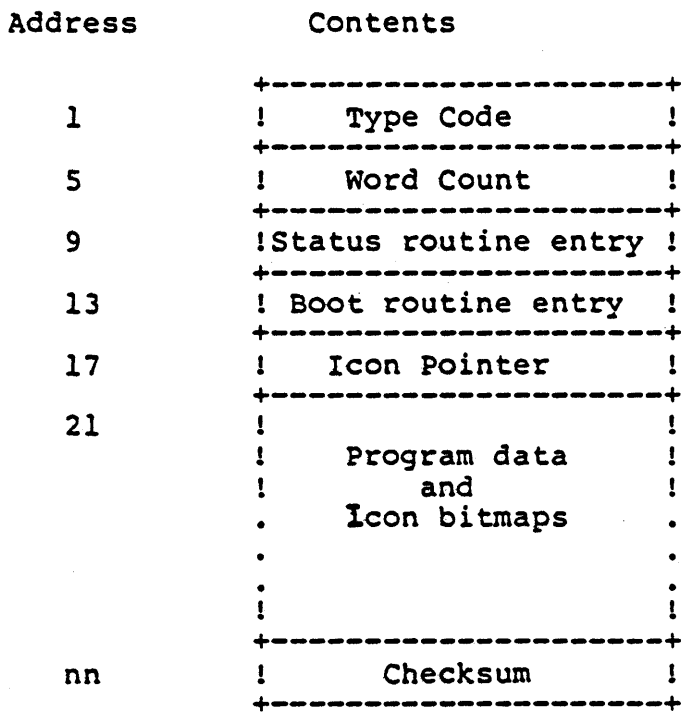


Figure 3-8. Bootstrap ROM Format

Icon Pointer (one word) - points to:

Icon count (one byte up to three icons)
Pointer to first icon (word)
Pointer to second icon (word)
Pointer to third icon (word)
First icon (bitmap)
Second icon (bitmap)
Third icon (bitmap)

The icon pointer must be a one-word value containing the byte offset from the base ROM address to the byte containing the icon count. The pointers to the actual icon(s) must also be in this format. The icons themselves can be stored in a compressed manner, and, if so, the icon count byte must have its msb = 1 (with the remainder of the byte being the actual count). The compressed format must be the same as that used by the boot ROM (a special program is currently available to do the compression). If not compressed, the icon(s) must be standard 48x32-bit LISA icons, and should be stored as 32 horizontal rows of 6 bytes each (192 bytes total).

If the user requests the boot icon menu at power-up time, the boot ROM will display the standard boot icon options along with the expansion-device icons, if present. Up to three icons can be displayed per expansion device, and the boot ROM will assign them unique boot id's as follows:

I/O Slot	Boot id's
1	4,5,6
2	7,8,9
3	A,B,C

If an expansion-device icon is selected for booting, the boot id will be relayed to the loaded boot program in register D0.

The final two parameters in the expansion device ROM are the word count and checksum. The word count should be a 16-bit female byte sex number indicating the length in words of the ROM data starting from the status routine entry point up to, but not including, the checksum word. The boot program will be read into memory starting at address 128K as 16-bit female words. As the words are loaded they will be added to an ongoing 16-bit sum, which is rotated to the left one bit position after each add. The 2-byte checksum should produce a 0 result when added to this calculated sum and all the rest of the

data in the ROM, including the type code, routine entry points, icon pointer, word count and icon bitmaps.

3.5 The External Ports

The LISA is equipped with several standard interfaces by means of which additional devices may be attached to the system. The purpose of this section is to provide a convenient specification for these interfaces for use with devices above and beyond those already functional on these interfaces.

The external plugs and sockets available on the LISA are:

* 2 serial RS232-C ports
* 1 25-pin D-type parallel port
* 1 9-pin D-type mouse connector
* 1 3-pin keyboard connector
* 1 co-axial composite video jack

Signal Name	Description	Channel A	Channel B
TxD	Transmit Data	2	2
RxD	Receive Data	3	3
RTS	Request to Send	4	4
CTS	Clear to Send	5	n/a
DTR	Data Terminal Ready	20	20
DCD	Data Carrier Detect	8	n/a
TxC	Transmit Clock Input	15	n/a
RxC	Receive Clock Input	17	n/a
TEXT	Transmit Clock Output	24	n/a
DSR	Data Set Ready	n/a	6
RxD	Applebus Receive Data	n/a	19

Figure 3-9. Serial Port Pin Assignments

3.5.1 Serial Port Interface

The two built-in RS232-C serial communication ports can support local asynchronous communication at rates up to 19.2 Kbaud. In addition, port #1 conforms to RS232-C type D specifications, which enables full modem control with either synchronous or asynchronous protocols.

The pin assignments and their use on both ports are shown in Figure 3-9. Both channels are set up to be the data terminal equipment (DTE) end of the communications system.

(Insert Figure 3-9)

In order to connect other DTE equipment, a modem eliminator or "null modem" is required. An Apple null modem (590-0029-00) with a communications card cable may be used to connect a serial printer to the LISA via a serial port.

Both ports are standard 25-pin D-type female sockets.

3.5.2 Parallel Interface Port

This interface is normally used to connect a hard disk, such as the Apple Profile to the LISA system. It may alternatively be used to connect a device which has a high data transfer rate and for which the serial ports are not appropriate.

The port is a general-purpose 8-bit interface which is presented on a standard 25-pin D-type connector. The pin assignments are shown in Figure 3-10.

(Insert Figure 3-10)

The meaning of the individual signals on the interface is as follows:

DD0-DD7 Eight bidirectional data lines. Bit DD7 is the MSB.

RW This line is driven high by the LISA to indicate that data is expected to be input on the data lines. It is driven low to indicate that data is being output.

PARITY Bidirectional line which must be configured on the basis of the data currently on the data lines to give odd parity.

PSTRB/ Processor strobe line used as a signal by the LISA to indicate valid data being output.

CMD/ This line is asserted by the LISA to indicate that a command has been placed on the data lines.

BSY/ This line is asserted by the peripheral to indicate to the LISA that it is busy and unable to process commands on the interface.

OCD The LISA monitors this line. If it is high, it is assumed that no device is connected to the interface.

CRES/ This line is asserted by the LISA when the peripheral is to be reset to its power-on state.

CHK This signal may be used to interrupt the CPU in the event that a fault condition has occurred in the device connected to the interface.

3.5.3 The Mouse Interface

The mouse is connected to the LISA by means of a 9-pin D-type jack, located in the middle of the connector panel at the back. The connector pin assignment is shown in Figure 3-11.

(Insert Figure 3-11)

3.5.4 The Keyboard Interface

The keyboard interface consists of a simple 3-pin Molex-type connector. It has a pin allocation as follows:

Pin 1	Data
Pin 2	Ground
Pin 3	+5V

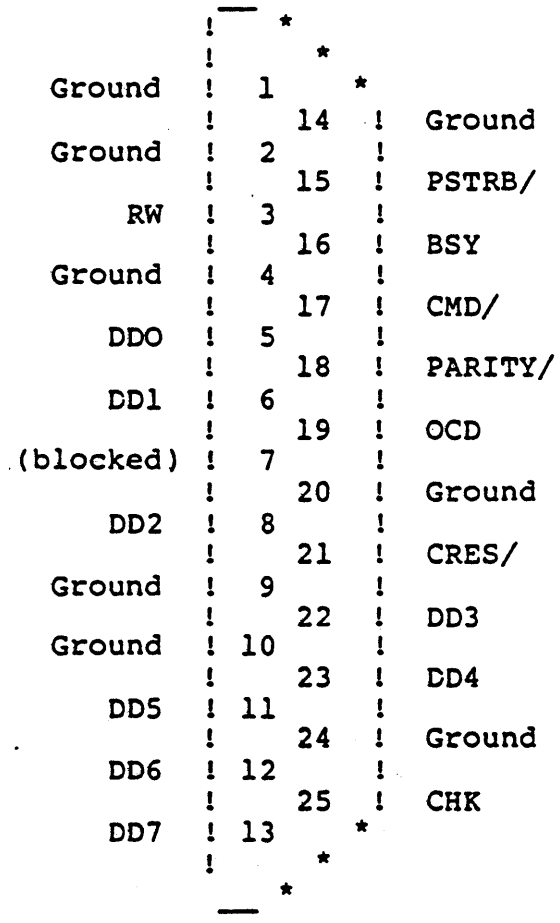


Figure 3-10. Parallel Port Pin Assignments

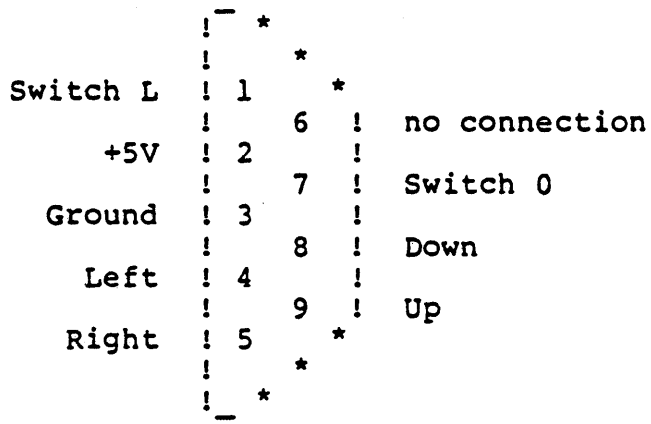


Figure 3-11. Mouse Interface Pin Assignment

3.5.5 Composite Video Interface

This interface consists of a standard shielded video jack at the rear of the unit. It is available to drive an external CRT monitor.

The data stream consists of the composite horizontal and vertical sync signals or'ed with the video data stream. The LISA screen page consists of 364 lines of 720 pixels each. The vertical retrace occupies 15 additional lines which are not displayed.

The screen refresh rate is 60Hz. Refer to Figure 4-11 for a timing diagram of the video signals.

SECTION II

CHAPTER 4

THE PROCESSOR BOARD

The heart of the LISA system is the Processor board. It contains the following major logic components:

* Central Processing Unit (CPU)
* Memory Management Unit (MMU)
* System Timing Generation
* Memory Timing
* Video Generation
* Interrupt Control
* I/O Decode
* DMA, Error Address and Flag Latches

The processor board is so called because it houses the logic associated with the 68000 central processing unit. It also contains the main memory management and bus control functions for the system. Some additional circuitry, such as error latches and video control have been located on this board for convenience.

The function of the processor board is to execute the LISA software, provide main timing for communication within the LISA system and provide additional control functions for the video logic.

4.1 Processor Board Block Diagram

An overview of how the components on the processor board logically interact is shown in Figure 4-1.

(Insert Figure 4-1)

Refer also to Figure 1-2 in Chapter 1, which gave an overview of the LISA system in block diagram form.

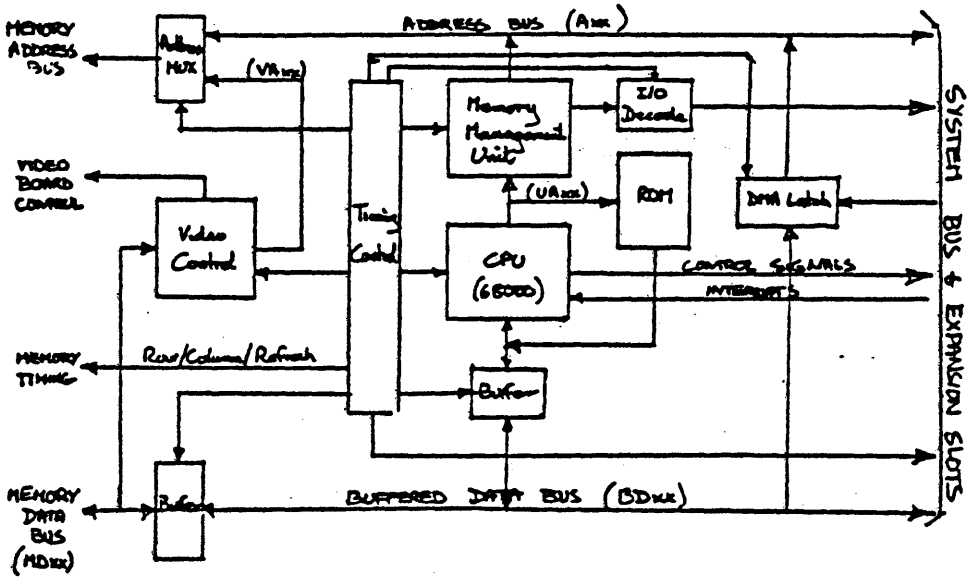


Figure 4-1. Processor Board Block Diagram

The processor board is capable of performing a number of operations which involve data flow within the board. Since both processor and video memory cycles are interleaved within one machine cycle, this leads to two major data paths during operation. Additionally, data transfer to and from peripheral devices during normal or DMA cycles give rise to two others, plus the path which loads the DMA address latch.

Addresses generated by the CPU are transformed from logical to physical addresses by means of the Memory Management Unit. A discussion of MMU programming can be found in Section 2.3. Addresses generated by the video or the DMA logic are not subject to transformation, i.e. they are physical addresses.

System ROM provides non-volatile storage which is used during system power-up initialization for bootstrap of the operating system. It may be addressed either with or without use of the MMU.

Internal timing on the board and on the bus conforms to the timing requirments of the 68000 CPU device, as described in the 68000 User's Manual. Operation of the system RAM memory is controlled by additional timing logic on the processor board.

The data-flow paths within the processor board are classified as follows:

* CPU Memory Access
* Video Memory Access
* CPU Access to I/O
* I/O Access to the DMA Address Latch
* I/O Access to Memory

Video memory access and I/O memory access can occur simultaneously due to the separation of the control lines and data paths involved.

These classes are discussed in the following subsections.

4.1.1 CPU Access to Memory

Memory access by the CPU occurs during the half of the instruction cycle in which the CPU may access memory. The other half of the cycle is used by the video circuitry to access screen refresh data.

The paths used in memory access are shown in Figure 4-2.

(Insert Figure 4-2)

The CPU generates the 24-bit logical memory address during the previous video half of the cycle. This address is presented to the MMU, which performs access checks and address translation in time to present a physical address to the memory board at the beginning of the CPU half of the CPU memory access cycle. In fact, the address is not fully formed at this point but the details of the row and column addressing within the memory matrix permit a degree of overlap into the actual CPU half of the cycle. This is discussed in Section 4.2 (Instruction Cycle and Timing).

The buffered data bus is used to transfer data between memory and the CPU under control of bus signals manipulated by the CPU. No other data transfers may occur in the system at the same time.

4.1.2 Video Access to Memory

Memory access by the video logic occurs during the half of the machine cycle used by the video board. It is used to access the bit-mapped display data located in the main system memory. Video access can be thought of as a pattern of consecutive DMA transfers out of memory in a manner transparent to the applications software.

The paths used by the video control to access memory data is shown in Figure 4-3.

(Insert Figure 4-3)

The video control generates physical addresses which are presented to the memory addressing multiplexor on the processor board for direct access to the required memory location. Data that is read out of memory in this way is presented to the video control via the memory data bus.

Note that the processor board is free to communicate with any I/O port over the system bus at the same time that memory is being addressed. Such an I/O cycle may occur in parallel with a video memory access.

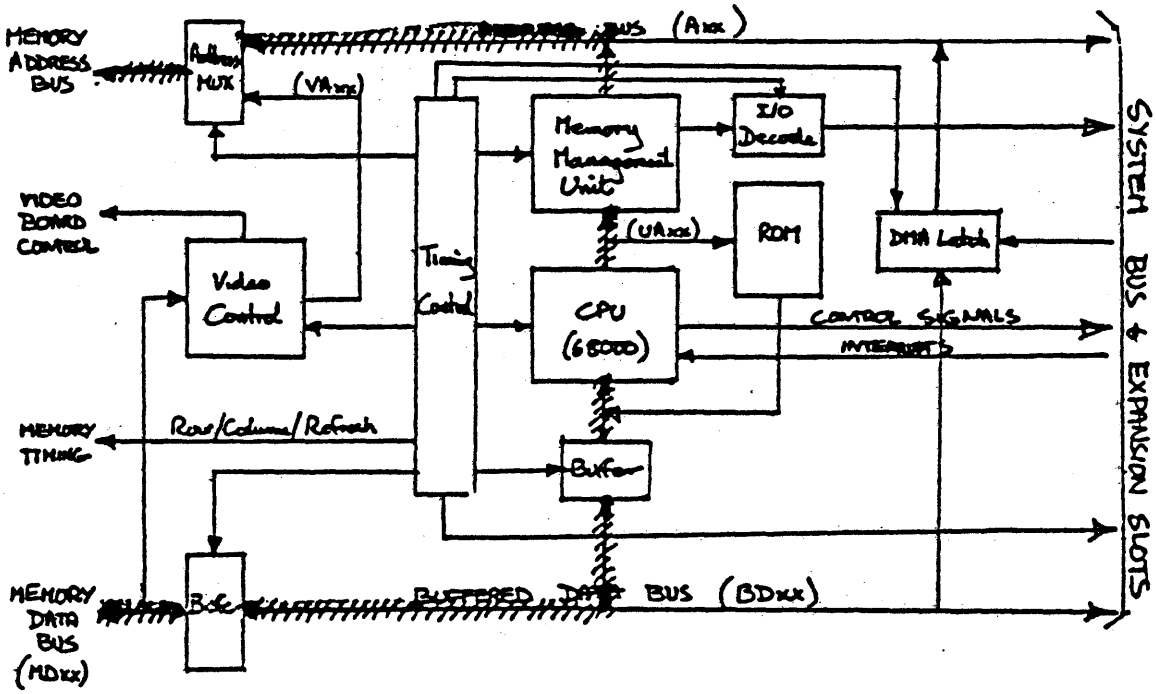


Figure 4-2. CPU Access to Memory

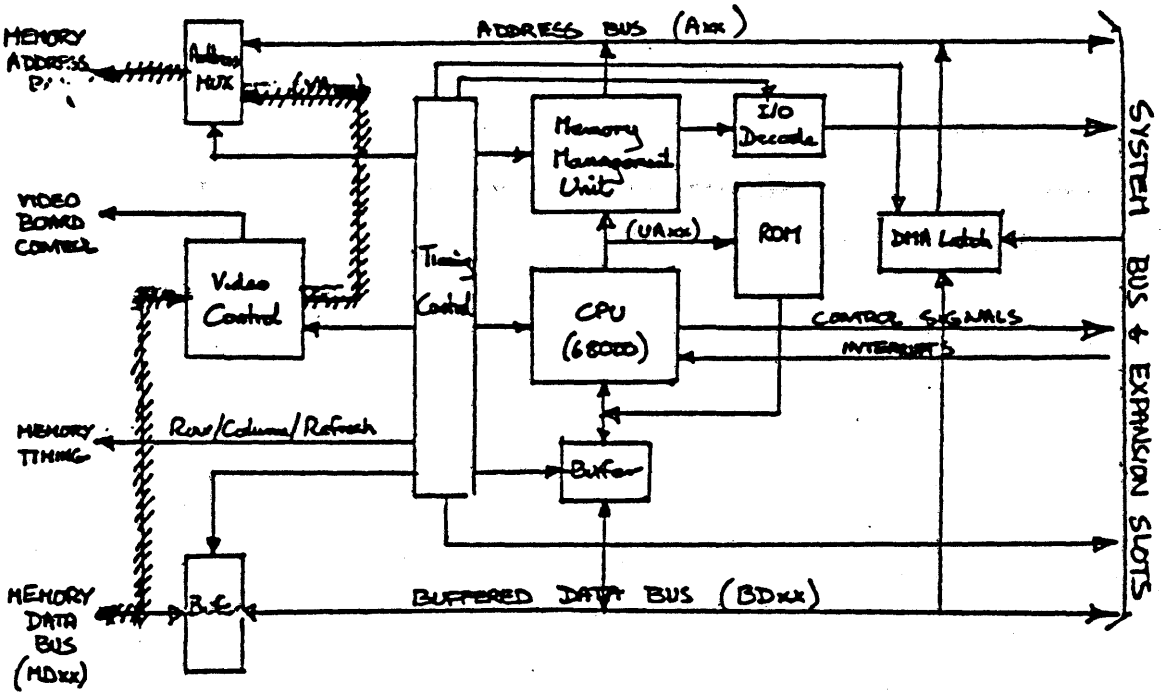


Figure 4-3. Video Access of Memory

4.1.3 CPU Access to I/O

The CPU communicates with I/O over the main system bus. I/O may be either a device located on the I/O board, which is always resident in the system, or it may be located on an expansion board in one of the expansion slots.

The CPU generates the logical address of the I/O device with which it wishes to communicate and presents it to the MMU in a manner similar to a normal memory access.

Within the MMU, the Segment Limit Register (SLR) contains information which defines the segment being accessed as being valid I/O space. This condition inhibits any memory access and instead presents the address generated by the MMU to the I/O decode logic.

The I/O decode logic generates an enabling signal to the board on which the device is resident, and the data transfer takes place via the main system bus. Refer to Figure 4-4 for an overview of the paths taken.

(Insert Figure 4-4)

Note that this cycle may be simultaneous with an access to memory by the video control, since no logic or data path is common to both.

4.1.4 I/O Access to DMA Address Latch

Transfer of data between main system memory and I/O devices in the LISA may take place under direct memory access (DMA) by the peripheral in question. This relieves the CPU from involvement in the transfer of every byte to and from the peripheral.

In order to generate the required physical addresses and to present them to memory, the processor board is equipped with a latch to hold the high-order byte of the memory address while the low-order bits are being manipulated by the peripheral to access sequential locations within the block of memory containing the data transferred by DMA.

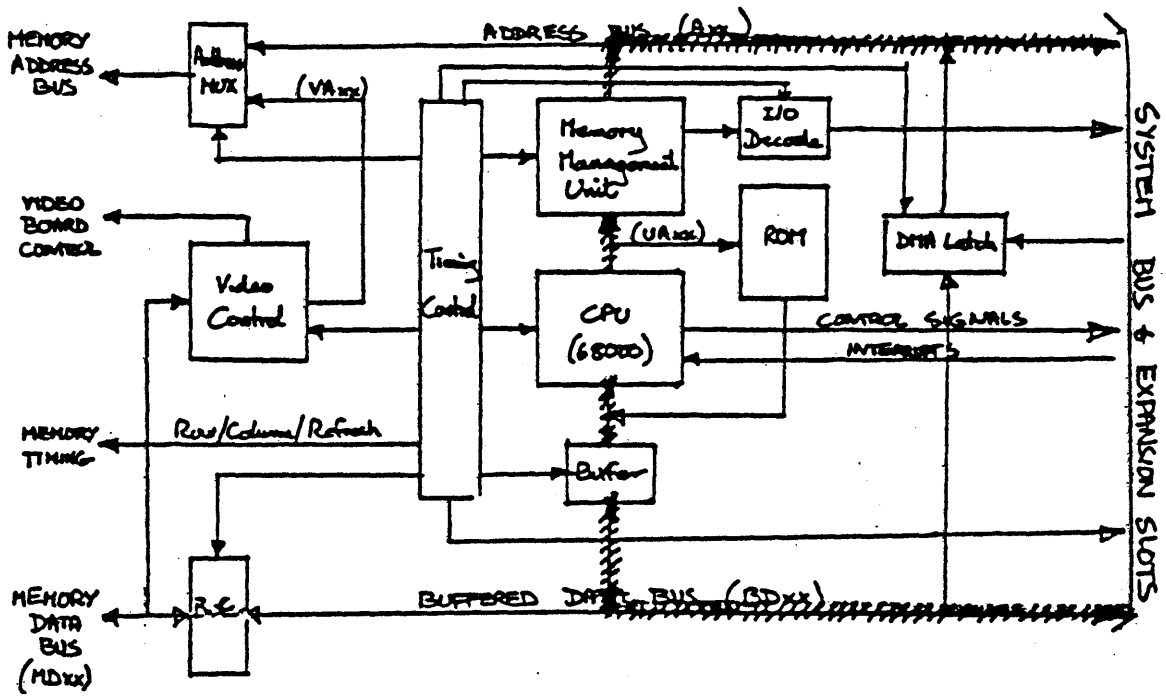


Figure 4-4. CPU Access to I/O

When the high-order byte is to be changed to allow access to another block, the I/O Board can load the latch as shown in Figure 4-5.

(Insert Figure 4-5)

Note that this operation does not require use of the memory bus and can therefore proceed in parallel with a video access to memory.

4.1.5 I/O Access to Memory (DMA)

As discussed in the previous subsection, the LISA system can use DMA to transfer data between memory and peripherals in a manner essentially transparent to the CPU.

The paths used to perform this are shown in Figure 4-6.

(insert Figure 4-6)

A physical memory address is generated on the I/O board from the DMA address latch contents for the high-order byte and address lines A1-A12 (from the expansion board generating the DMA) to give the full address.

This address is presented to the system memory in a manner which is identical to a normal CPU access, and the data is transferred via the buffered data bus.

No other data transfer may take place in the system during this half of an instruction cycle. Each series of DMA cycles begins with a procedure in which the CPU relinquishes control of the bus. From this time, all signals on the bus which are required for data transfer are generated by either the I/O board or the expansion board, whichever is making the transfer.

It is important that the design of I/O cards which use DMA takes into consideration the overall system timing and software constraints as described in Section 4.2. Since the CPU is not processing instructions at this time, the I/O card effectively "replaces" the CPU and must generate signal patterns which are indistinguishable from those of the CPU.

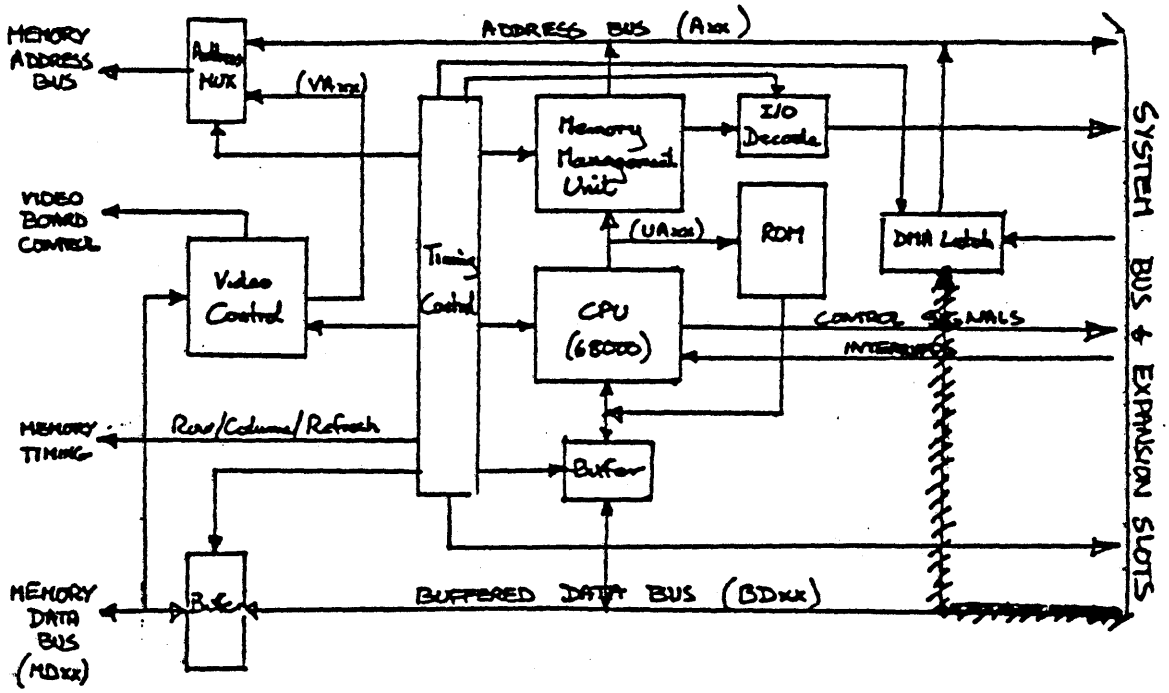


Figure 4-5. I/O Access to DMA Address Latch

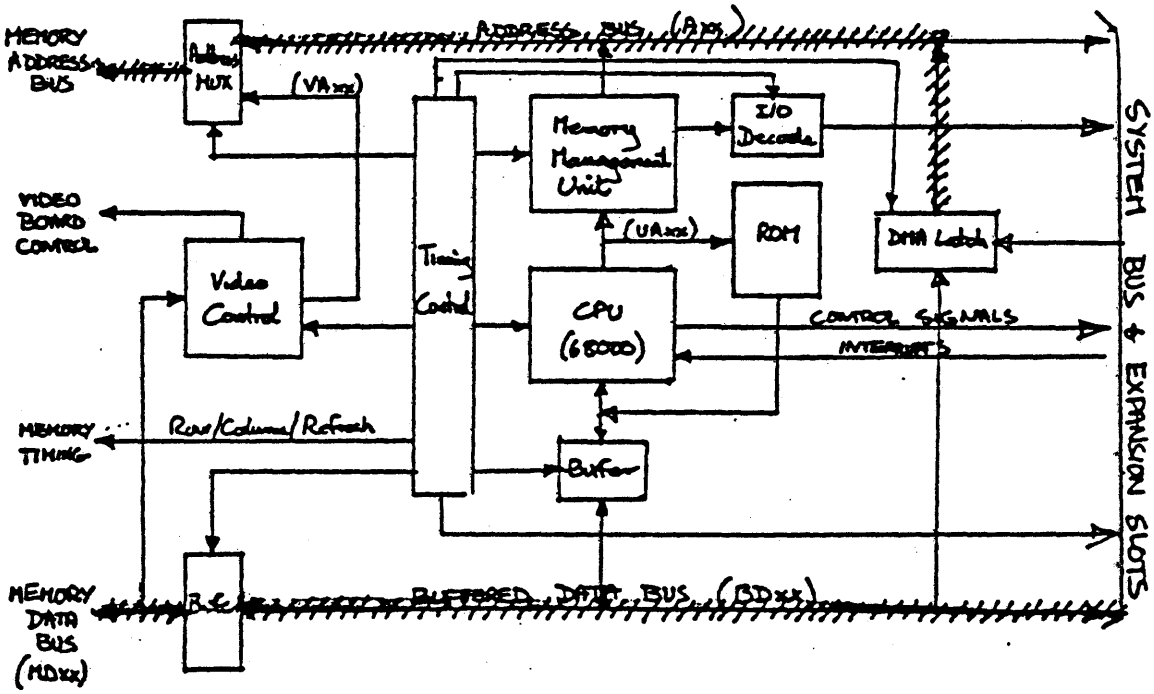


Figure 4-6. I/O Access to Memory (DMA)

4.2 Instruction Cycle and Timing

Apart from internal signals used on the board itself, the main signals generated by the processor board are used to control timing to the memory array, data refresh on the CRT screen via the video control and data transfer on the main system bus.

4.2.1 Internal Timing

The timing internal to the processor board is based on the timing of the 68000 CPU device. The basic 800 nanosecond instruction cycle is divided into two equal halves. A 400 nanosecond video cycle is followed by a 400 nanosecond processor cycle.

A timing diagram of the principal signals internal to the processor board is shown in Figure 4-7.

(Insert Figure 4-7)

Each half of the instruction cycle is in turn divided into eight timing periods t0 through t7, each of 50 nanoseconds. These periods are generated by a 20.375 MHz signal called DOTCK. DOTCK is divided by four to provide the 5 MHz CPUCK signal used to clock the 68000. The processor board synchronizes to the 68000 so that the S-states of the 68000 correspond as shown in Figure 4-7.

This timing results in the AS (address strobe) signal being recognized during the video cycle, which permits the MMU to calculate and check the physical address in time for the result to be ready for the processor cycle.

The CPUC1 signal signifies the first cycle of a CPU instruction execution. The IOCY and SPIO signals indicate that an I/O or special I/O cycle is in progress. The IOCY and SPIO signals are generated from information contained in the MMU.

The MALE signal is used as the selector between the two registers in the MMU that are associated with each logical address. When MALE is true, the SOR register is being accessed and the MMU is in the process of calculating the origin of the page being addressed. When MALE goes false, the SLR register is selected and the MMU calculates whether the address lies within the page limits.

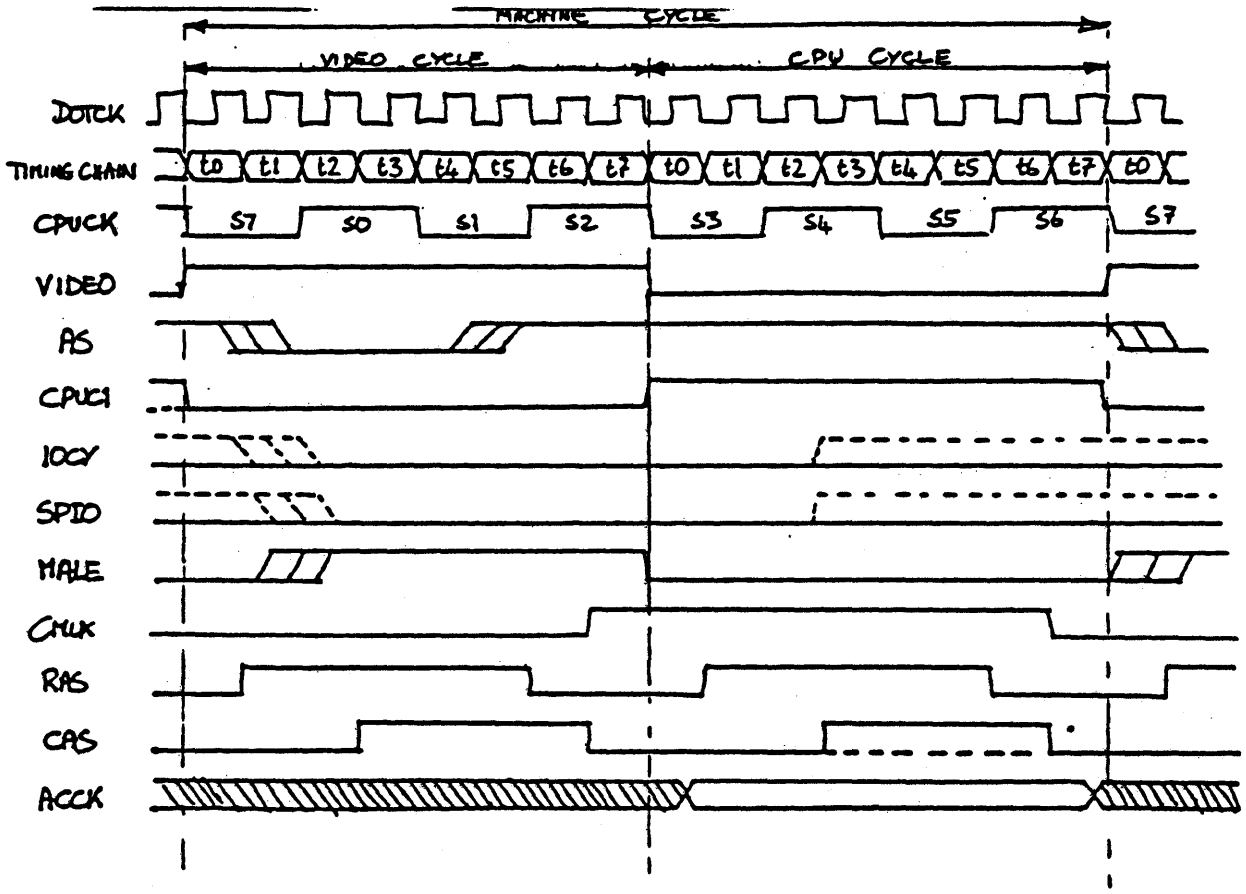


Figure 4-7. Processor Board Internal Timing

The CMUX signal is used to select the source of the address which is to be presented to the memory. When deasserted, it gates the video address. When asserted, it gates the physical address presented by either the MMU or the DMA control.

Memory timing is controlled by the row and column address strobes RAS and CAS. These and all of the other signals listed above are generated with reference to one or more of the t0 through t7 time periods.

4.2.2 Memory Management Timing

A logical address is being output from the 68000 when the address strobe signal is asserted. The MMU must process this and present the result to the rest of the system on the basis of the type of access. In the case of a memory cycle, the physical address must be stable in time for presentation to the memory along with the row and column strobes.

In addition, the timing of each Special I/O cycle with which data is written into an MMU register involves signals not used in any other operation. Figure 4-8 shows a sequence of operations as follows:

* The beginning of a calc/check cycle
* The execution of a write to the MMU

The MMU calc/check cycle is completed during the following cycle after the MMU access is complete.

(Insert Figure 4-8)

The MALE signal selects between calculate mode (based on the SOR register) and check mode (based on the SLR register). MALE directly generates the B/L/ (base/limit) selection signal.

The FC2 signal originates in the 68000. It is asserted to indicate that the processor is currently in supervisor mode. Mapping will be forced to the supervisor context (context 0) when FC2 is asserted unless a read/write access to the MMU registers is being performed.

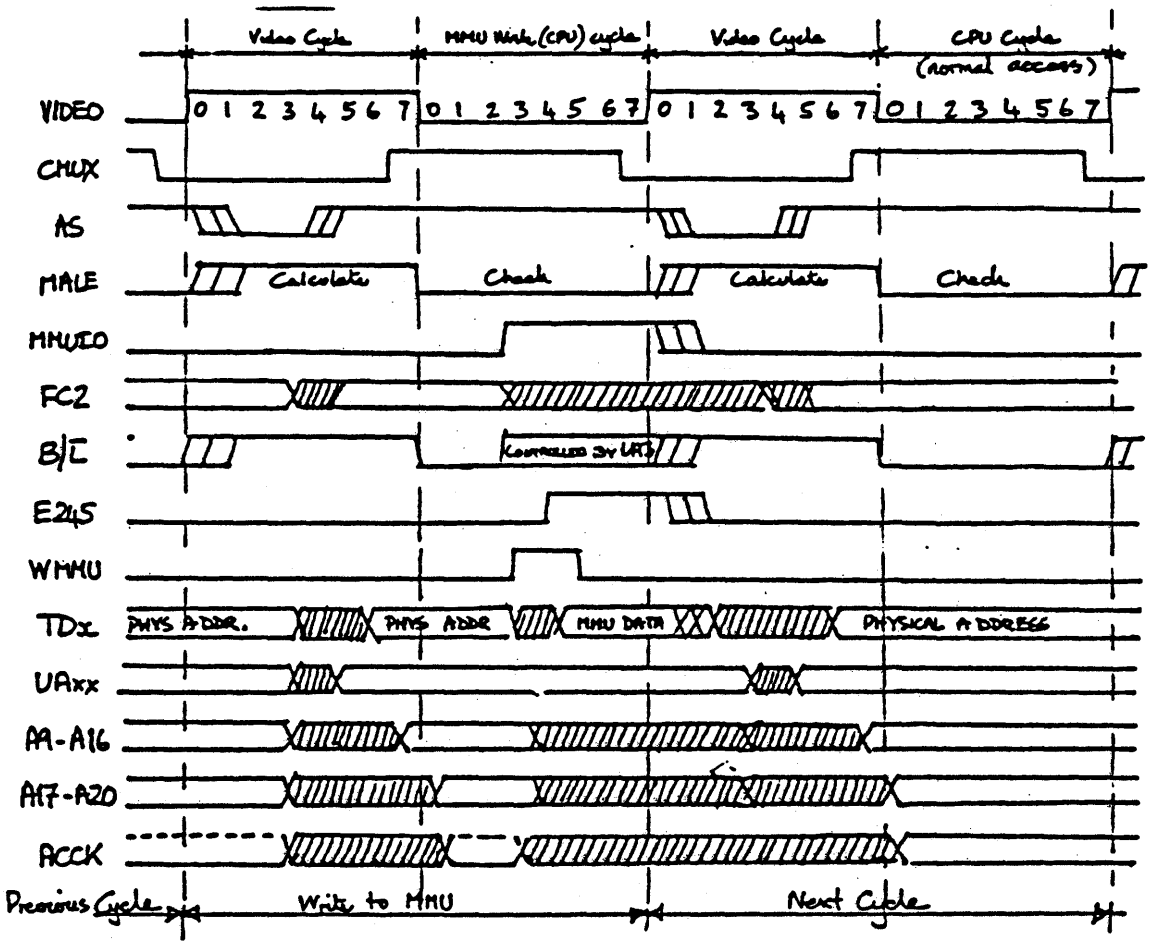


Figure 4-8. MMU Timing Diagram

A write cycle to the MMU is a special I/O cycle and begins with the assertion of the SPIO signal, which directly generates the MMUIO signal. This causes the B/L/ signal to be controlled by the UA3 address line to select between the SOR and the SLR registers.

The output of the MMU memory is disabled when the WMMU signal is asserted and the data to be written is placed on the TD lines by means of the E245 signal.

Note that the address lines are divided into three groups as regards timing. These are:

* The UA (unbuffered address) lines. These do not pass through the MMU and are therefore stable first.
* The A9-A16 lines. These are generated by the MMU and presented almost directly to the I/O decode and memory after the skew inherent in the MMU access time.
* The A17-A20 lines. These suffer an additional delay due in the adder chain.

Note that the A17-A20 lines are not yet stable at the time when RAS is sent to the memory. This is acceptable since these address lines are used only in the column address.

4.2.3 Memory Timing

The memory boards contain principally the memory array itself, some error-detection circuitry and the necessary latches and drivers. Most of the memory control signals are generated by the processor board and presented to the memory board via the memory bus.

The 800 nanosecond instruction cycle includes two separate 400 nanosecond memory cycles. The signals which control these on the interface to the memory boards are shown in Figure 4-9.

(Insert Figure 4-9)

The CMUX signal is used to select between the video and the processor addresses being presented to the multiplexer. The contents of the RA signals is controlled both by the CMUX and the RAS signals.

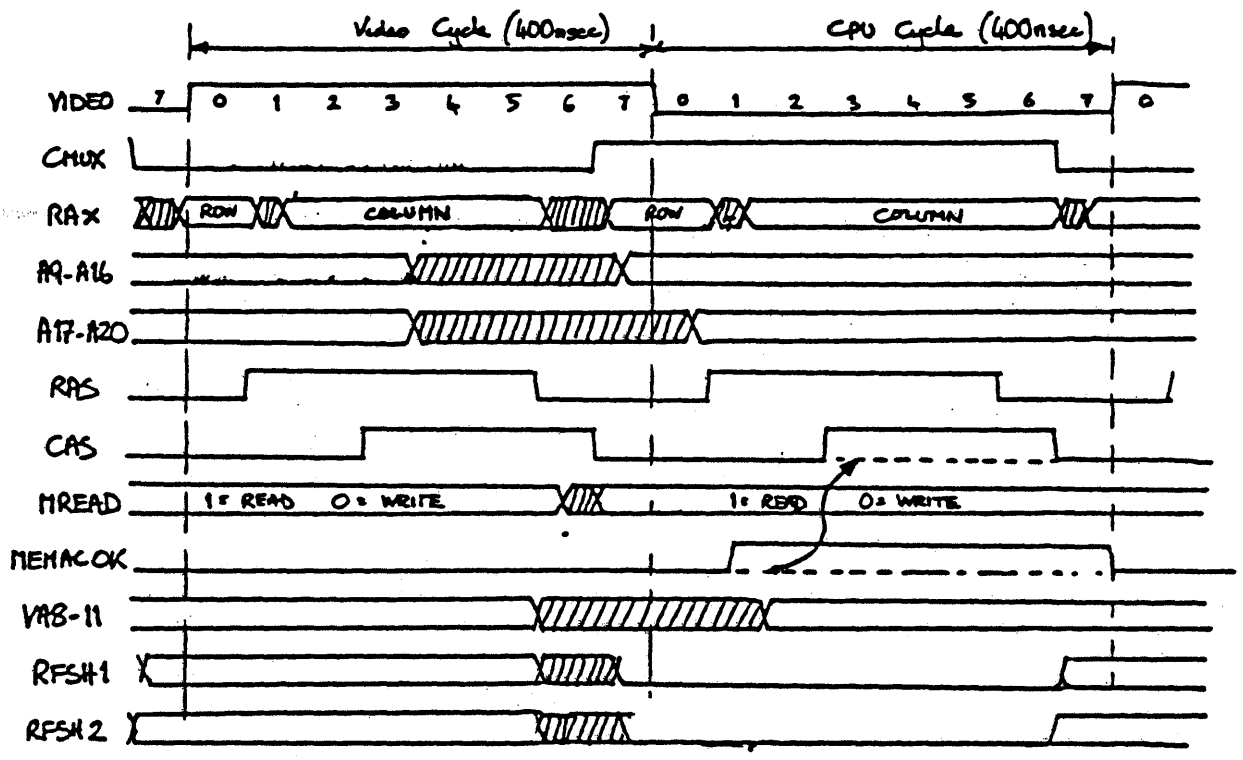


Figure 4-9. Memory Control Timing Diagram

The A9-A16 and A17-A20 are generated by the MMU and are used to generate column address and board or device selection within the system memory.

The CAS signal is generated for each video cycle, but may be absent from a processor cycle if no memory access is taking place. This is indicated if the MEMACOK is deasserted and there is no DMA cycle in progress, which will inhibit CAS.

The RAS signal is present for every cycle unless the cycle is a cycle of a multi-cycle processor access other than the first.

The VA8-11 are representative of the timing of all video address signals. These are also used in the generation of the refresh address in the memory since video accesses are always to sequential locations. Refresh takes place during the video cycle to devices not currently being accessed.

Selection of refresh for a particular board is controlled by the RFSH1 and RFSH2 signals. Refresh details are discussed in Section 5.3.

4.2.4 Video Timing

The video board in the LISA is described in Chapter 8 and contains the analog circuits necessary for control of the CRT. It is fully under control of the processor board. This means that all control and timing signals for the transfer of data to the CRT screen is done under processor board control. Figure 4-10 shows the timing diagram for the signals generated.

(Insert Figure 4-10)

The video control contains a shift register which is loaded at the end of a video access and then shifted out at a rate of 1bit/50nsec (20MHz) to provide the bit-serial data stream to the video board.

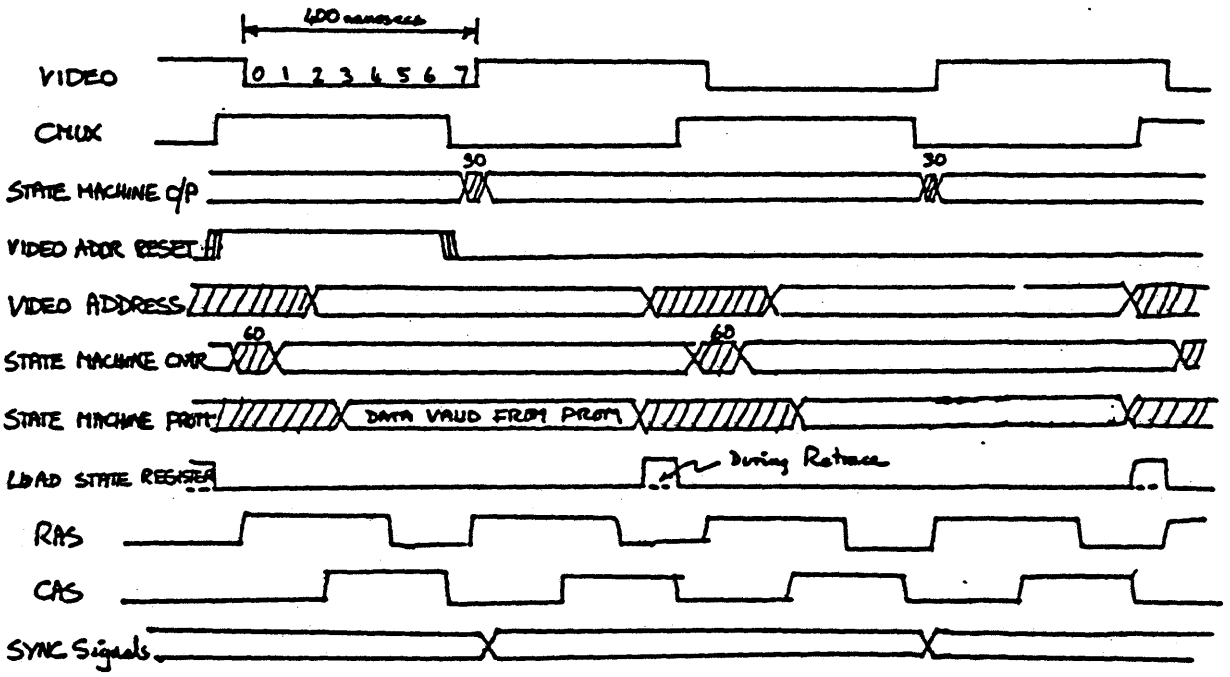


Figure 4-10. Video Control Timing Diagram

The data stream continues to be read whenever the end of a line is reached and a horizontal retrace is being performed. However, the data is ignored and the video address counter is not incremented. In a similar fashion, data is not read out during the vertical retrace at the end of a full screen.

The timing for the video control area is performed by a state machine and is synchronized with the VIDEO and CMUX signals. The shifting of the bits out to the video board is performed by the DOTCK.

The state machine counter is clocked with the falling edge of the VIDEO signal. The rising edge of this signal latches the current output from the state machine PROM.

The output of the state machine provides signals which provide synchronization of the CRT and also control within the video control circuitry.

The video address is reset only once per page. This occurs after 379 lines of 720 pixels each. Only 364 lines are displayed on the screen. The timing of the video data within a page is shown in Figure 4-11.

(Insert Figure 4-11)

The last pixel of each page must be asserted in order that the retrace is black. This is done by having a "one" in the least significant bit of the 32,767th byte displayed.

4.3 The Central Processing Unit

The heart of the LISA system is the 68000 16-bit processor unit. It is described in detail in the 68000 User's Manual. Refer to drawing 050-4009 in Appendix A for schematics of the devices discussed in this section.

Page 3 of the schematics shows the CPU at location A3-D3.

4.3.1 Clock Generation

Timing generation is shown on sheet 2. At B-4, crystal X1 and its associated oscillator circuit is used to generate the DOTCK and CK signals. These both have a period of 50 nanoseconds and have a waveform shown on Figure 4-12.

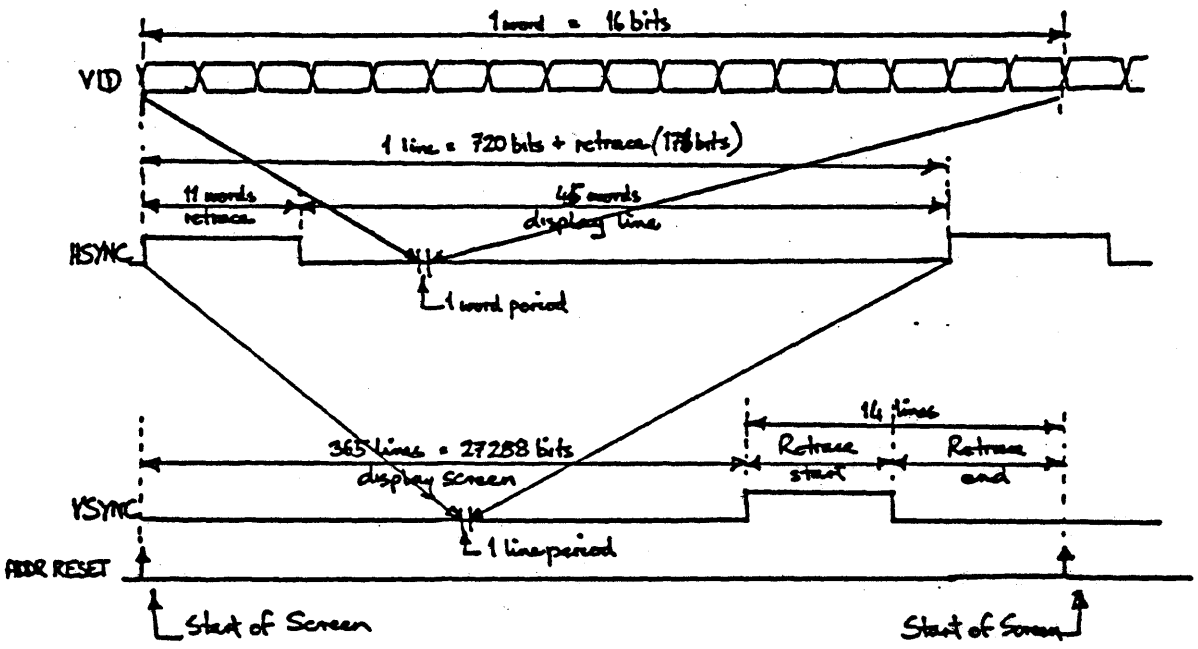


Figure 4-11. Video Page Timing

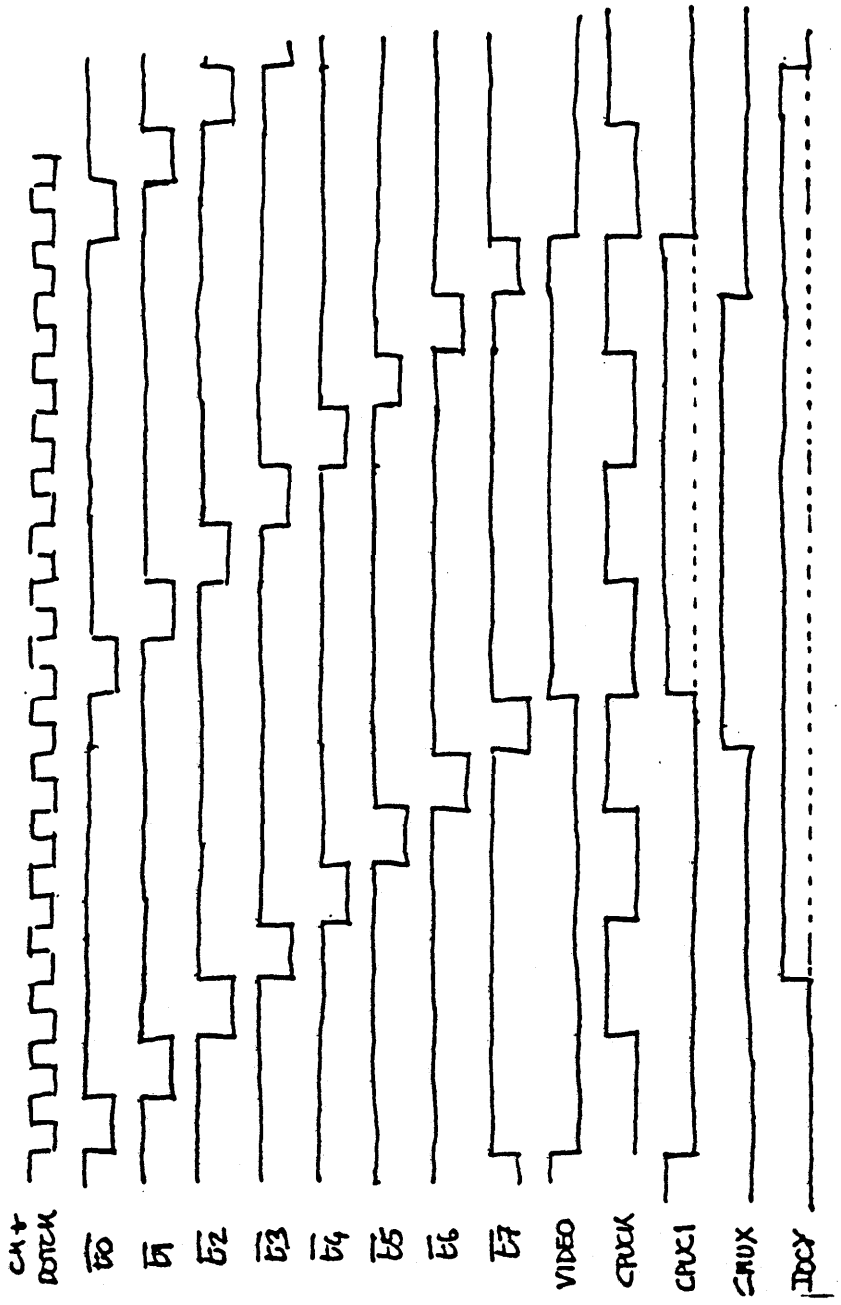


Figure 4-12. Processor Board Timing Generation

(Insert Figure 4-12)

The DOTCK signal is used to provide timing to the video control which shifts bits serially to the video board. These bits are then displayed on the screen. CK drives the 4-bit synchronous counter at D-3 whose outputs are decoded to provide the eight timing states t0/ through t7/, plus the VIDEO signal, as shown in Figure 4-12.

The QB output has a period of 200 nanoseconds. It is used as the 68000 clock and also generates the main system clock CPUCK, which is distributed through the LISA system.

4.3.2 Processor Control Signals

The six main bus control signals are buffered by the LS244 at C-3 on sheet 3. This is enabled when the BGACK/ (bus grant acknowledge) signal has been deasserted. In other words, the bus is released at the same time that the bus grant acknowledge is generated, which allows the slave device to take control of the bus.

Note that UAS/ constitutes an unbuffered address strobe, which is not gated as above. The system is synchronized with the AS (address strobe) signal. This signal should be used for synchronization on the board whether the bus is under CPU control or not.

The status signals FC0, FC1 and FC2 are decoded to provide the IAK and IAK/ signals. These latter signals are used to gate the address of the device which generated an interrupt. The FC2 signal is used to distinguish between read and write cycles.

Incoming interrupts are encoded by priority through the LS148 at C-4 and presented to the IPL0-IPL2 inputs of the 68000.

The system RESET is buffered and chained through the 7417 at D-3 whose output is pulled up through R12.

Other control signals interface directly to the bus drivers, with no buffering.

4.3.3 Address and Data Lines

Address lines A9 to A23 are presented directly to the MMU since these are the bits which define the segment and page of memory which is being addressed. (Refer to Section 2.3 for a discussion of the MMU address translation process).

The low-order eight bits, A1 to A8, are buffered through the LS244 at A-3, which is gated with BGACK/ to release the memory bus when the CPU relinquishes bus control.

The 16 data lines D0 to D15 are buffered by the bidirectional LS245's at A-4 and B-4. These are enabled by the DBON/. The direction is selected by the READ signal.

4.3.4 Bootstrap ROM

The bootstrap ROM is used during system power-up to provide initial programs which will permit the operating system to be loaded from a mass storage peripheral and the system itself to be initialized to a known configuration.

The ROM is accessed by means of special I/O cycles. The ROM consists of the two devices shown at locations A-2 and B-2 on sheet 3.

Note that the ROM is addressed directly by the address lines from the 68000. This means that the ROM addressing does not require that the MMU be operational. Therefore system bootstrap routines will execute correctly out of ROM before the MMU has been configured at initialization time.

The ROM is enabled by the ROM/ signal. This signal is asserted whenever a special I/O cycle is in process while UA15 is asserted and UA16 is deasserted.

4.4 The Memory Management Unit (MMU)

The function of the MMU is to transform logical addresses used by the software running on the LISA system into physical addresses. This is performed in terms of logical pages of 512 bytes within logical segements of 128K-bytes.

The operation of the MMU is discussed in Section 2.3 above. Address lines UA1-UA8 are not operated on by the MMU. UA17-UA23 are used to select one of the 128 possible logical segments, while UA9-UA16 address a page within that segment.

At the same time, the entire logical system operates in one of four possible contexts, selected by the SEG1 and SEG2 signals. The MMU has four identical sets of registers, one for each context of 128 segments.

Each segment has two registers associated with it. The origin register (SOR) contains 12 bits which give the page number with which the segment begins. The limit register (SLR) contains 8 bits which supply the number of physical pages assigned to this segment, plus 4 bits which indicate the physical address space and other data about the physical segement.

In simplified form, the MMU is shown in Figure 4-13.

(Insert Figure 4-13)

The MMU is used to define three distinct physical address spaces. This is discussed in Chapter 2 in some detail. Refer also to Figure 2-4. The system can access a maximum of 2 Mbytes of RAM which is located on up to two boards, plus a distinct I/O space and an additional "special I/O" space.

Each address space occupies a 2 Mbyte block of the physical address space of the system.

The MMU logic is shown on sheet 4 of schematic 050-4009 in Appendix A. It consists of RAM storage for the segment registers, address latches and logic which permits the contents of the registers to be manipulated.

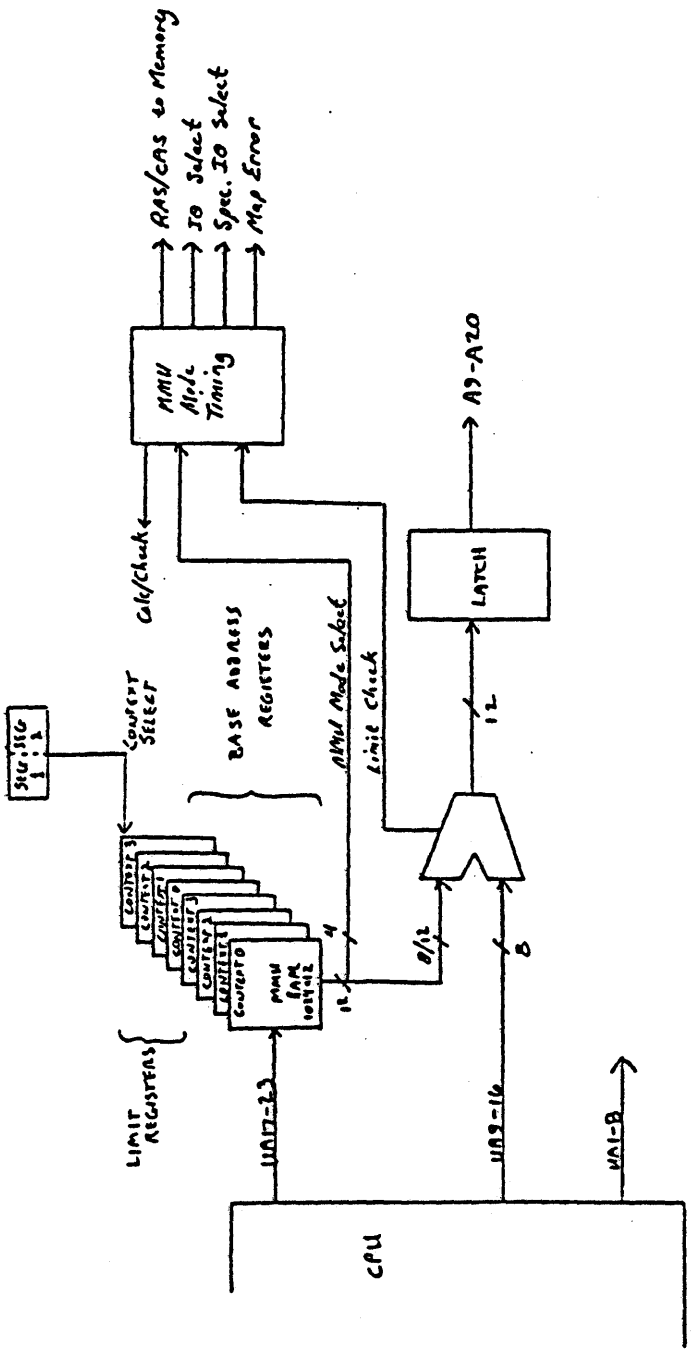


Figure 4-13. MMU Block Diagram

4.4.1 MMU RAM Storage

The registers of the MMU are organized within a 1Kx12 bit RAM memory matrix. These can be altered by software when the system is in any mode. The operating system is responsible for controlling access to these registers. The register addresses are generated from the logical address. Their contents define the physical address.

The LISA system has a 16M-byte logical address space due to the architecture of the 68000. This entire space may function in one of four contexts, depending on the configuration of the SEG lines.

Each 16M space is divided logically into 128 segments, each of which is allocated a pair of registers in the MMU which define segment parameters. This results in a total of 1024 registers, since the four contexts each contain 128 segments and each segment requires a pair of registers. This is shown in Figure 4-14.

(Insert Figure 4-14)

The two registers for each segment are known as the SOR and the SLR registers, as described in Chapter 2.

The SOR (segment origin register) defines the physical address of the first byte of the segment. This is given as a multiple of 128K-word blocks. The first block in memory thus is defined by address 000000H.

The SLR (segment limit register) defines the size of the segment in terms of multiples of 512-word pages. It also contains a 4-bit code which defines the type of space as outlined in Figure 2-4.

The MMU memory is thus logically divided into four sets of 128 pairs of 12-bit registers, each set being used only when the system is running in the corresponding context. This enables system software to perform context switching very rapidly.

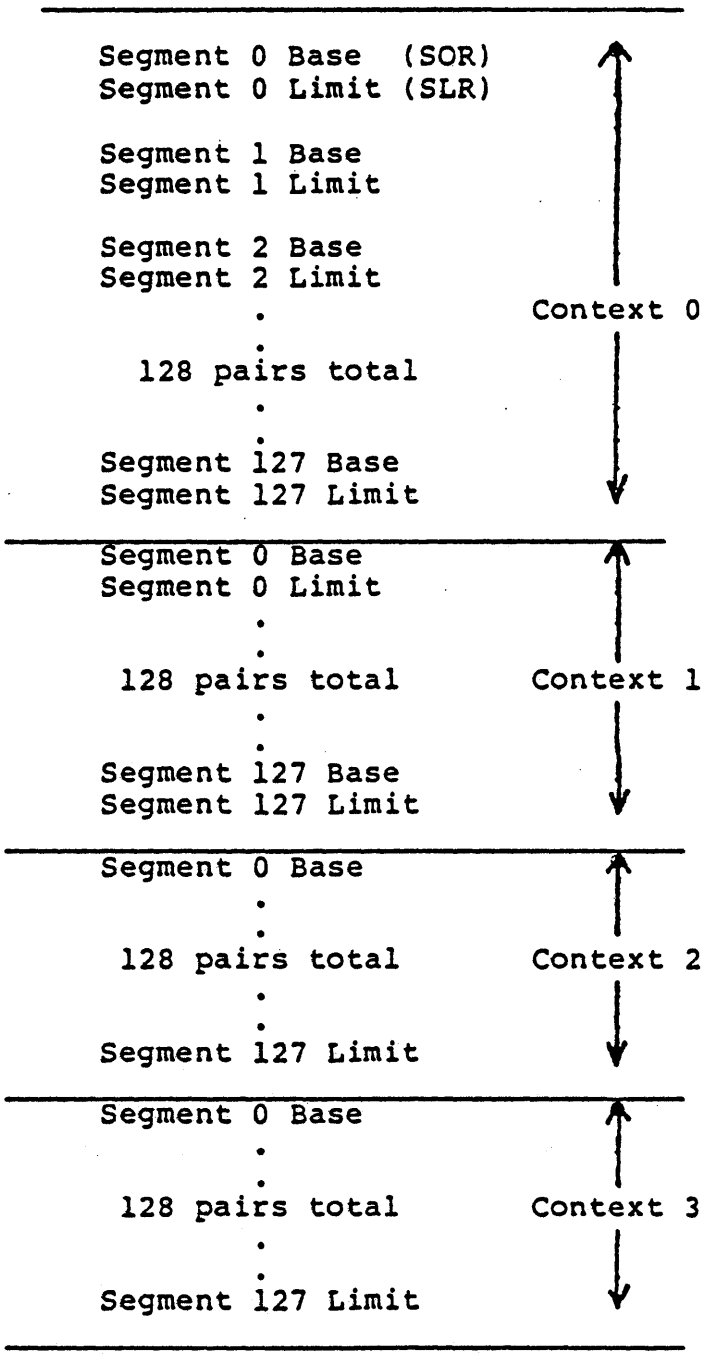


Figure 4-14. MMU Memory Configuration

Referring to schematic 050-4009, page 4, the ten lines used to address the MMU RAM may be seen as consisting of the following:

* UA17-UA23 (7 address lines)
* MS1 & MS2 (from SEG1 & SEG2 lines)
* B/L/ (the base/limit select)

The address lines are the unbuffered high-order address lines from the 68000 CPU on sheet 3. The other signals are generated in the logic at C-4. Refer to Figure 4-8 for the timing relationships.

The crucial element of operation in the MMU is that it must first generate the physical address which is the origin of the memory page to be accessed. Then it must check whether the address lies within the limits of the page addressed.

These two functions are selected by the MALE (memory address latch enable) signal, which originates in a S109 JK Flop on sheet 2. MALE is asserted at the end of a CPU cycle when the AS signal becomes deasserted. This typically occurs around the t3 period of the video cycle. This asserts the B/L/ signal through the ALS00 gate at D-3 which selects the base register.

The SEG1 and SEG2 latch is shown on sheet 5. The software defines the context in which the system is currently running by means of these two signals, except if the system is running in supervisor mode. Supervisor mode is indicated by the FC2 signal being asserted. The segment being addressed is defined by the UA17-UA23 signals.

When the conditions exist to set the CPUC1 JK flop at B-2 on sheet 2, the same term is used to reset the MALE flop at B-2. This occurs at the end of t7 time during the video cycle. With MALE deasserted, the B/L/ term also becomes deasserted and the SLR register which corresponds to the SOR register just accessed is used to check the access limits and also give the type of cycle to be performed.

4.4.2 SOR and SLR Register Initialization

The MMU registers are in an undefined state when the LISA system is first powered on. The bootstrap ROM is not addressed via the MMU. This enables the system to initially operate without requiring that the MMU is functional.

Before system RAM can be used, the registers which correspond to the contexts and segments being used must be initialized. The RAM which is used as the MMU register storage is accessed via Special I/O space. This is decoded by the LS139 device at C-2 on sheet 5. The MMUIO/ signal enables the WMMU/ signal via the JK Flop at C-4. Refer to Figure 4-9 for signal timing relationships.

Each register is written to in a separate write cycle. The SEG1 and SEG2 lines are configured to the appropriate context and the UA17-UA23 lines select the segment. When the registers are being written to, the SOR or SLR are selected by the state of the UA3 line through the ALS00 gate at D-3.

The MMUIO signal is asserted when the following conditions exist:

1) The SPIO signal is asserted
2) UA15is asserted
3) UA16 is deasserted.

When MMUIO becomes asserted, the clear input of both S109 JK flops at D-4 are released, allowing the E245 signal to be asserted at t4 time and WMMU to be asserted at t3 time if the 68000 is performing a read cycle.

The data which is to be written into the registers is presented to the MMU RAM via the two LS245 bidirectional drivers at C-3 and D-3. The direction in which the data is moved is controlled by the READ signal from the CPU.

The TD lines from the lower LS245 write the low order two nibbles into the lower RAMs. The upper nibble is base data for the SOR register or access-type data for the SLR register.

Register contents can be read via the same path.

4.4.3 Address Translation

During the video half of the instruction cycle, the SOR contents are read out as a 12-bit physical address which defines the physical address of the beginning of the segment at a 128K-word boundary.

This value is added to the page address which is presented to the other inputs of the adder by UA9-UA16. Note that the high-order input nibble is forced to zero. The result is presented to the LS373 latch at C-2 and the LS374 latch at B-2. On the falling edge of the MALE signal, which

occurs at the end of the calculation involving SOR, the combined segment and page address is latched. This will be stable on the A9-A20 lines if the BGACK/ signal is deasserted (no DMA access in process) and CMUX is asserted to avoid conflict with the video address.

MALE being deasserted signals the second half of the instruction cycle, when the access limits are checked. The B/L/ signal changes polarity and the contents of the SLR register is read out.

The low-order eight bits, which indicate the number of pages contained in this segment, are also added to the page address given by the UA9-UA16 lines from the CPU. The overflow line from the second nibble is the ACCK (access check) signal. If ACCK is asserted, this indicates that the desired page lies outside the limit set for the segment in question.

An exception to this occurs when the control bits indicate that the segment being accessed is a stack segment. Since the stack begins at the high-order address within the block, the significance of ACCK is inverted in this one case. This function is implemented in the S86 gate at B-3 on sheet 2.

An overflow results in the suppression of the CAS/ signal, which prevents any memory operation from taking place. The output of the high-order nibble of the adder is ignored since it is irrelevant at this point.

The high-order nibble of the SLR contents provide flags for the type of segment which is being accessed. These indicate:

* Segment in memory space (MEM)
* Segment in I/O space (IO)
* Segment which is read-only (RO)
* Segment which contains the stack (STK)

Refer to Figure 2-4 for the full coding permutations possible, since all combinations are neither valid nor covered by the above . These signals in turn generate the appropriate control signals for the type of segment indicated.

The MEM term being asserted (MEM/ low) enables the CAS signal for a memory access via the LS02 gate at C-3 on sheet 2.

The IO term being asserted initiates an I/O cycle via the IOCY flop at B-1 on sheet 2.

The RO term being asserted inhibits a write cycle to memory via the ALS32 gate at B-3 on sheet 2. It also inhibits an SPIO cycle by being one of the terms on the LS260 gate at C-1.

The STK term being asserted causes a shift input to be presented to the low-order adder via the F02 gate at A-2 on sheet 4. This is done because of the stack configuration, which begins at the top of the segment and decrements through memory from there.

4.4.4 Memory Timing Generation

Memory control timing is shown in Figure 4-9. Since the low-order nine bits of the address are presented directly from the CPU, these are used as memory row addresses. This avoids the need to wait for the output of the MMU to become stable before any memory addressing can be done.

The row address strobe (RAS) is enabled through the LS32 OR gate at D-4 on page 2 of the schematics. It comes true at the end of the t0 state and goes false at the end of t5. Note that RAS is generated even for cycles which turn out to be I/O or erroneous. This does no harm provided that CAS is not generated for such cycles. The only time that RAS is not generated for a memory cycle is if the current cycle is not a video cycle and is not the first of a multi-cycle CPU access.

The column address strobe (CAS) has an enable signal which is conditional upon a number of terms:

* If a video cycle is in process
* If a DMA cycle is in process (BGACK.CPUC1)
* If no error was detected in a memory cycle

This last term requires that a number of factors be satisfied:

* A memory cycle is in process (MEM.CPUC1)
* No attempt is made to write to a read-only segment (READ/.RO)
* The segment limit was not exceeded (ACCK)

If CAS is enabled, it will go true at the end of t2 and go false at the end of t6.

The signal requesting a read from the memory is MREAD. It is generated through the S02 gate at B-2.

Refresh of the memory is generated by two gates at A-2. One of the two signals R1 and R2 is provided to memory board for use as a refresh enable. Each occurs when either but not both of the VA8 and VA11 video address signals is asserted.

4.5 Video Control Section

All control functions of the video monitor are located on the processor board. The video board provides the analog circuits to interface digital data to the LISA CRT screen.

The video format on the screen is a bit map located in main RAM memory, organized as 364 lines, each containing 720 dots. In addition to this, four words are displayed at the bottom of the screen.

The video control is shown in Figure 4-15 and consists of the following components:

* Video Address Counter (VA1-VA14)
* Shift Register
* Video State Machine
* Video Page Register (VA15-VA20)

(Insert Figure 4-15)

The 32K-bytes of memory in which a full video screen is stored is sequentially accessed once every 1/60th of a second.

4.5.1 Video Address Counter

The video address counter points to the location in the 32K-byte video page of the next data byte to be fed to the display. It is incremented once for every 16 active pixels that are fed into the video board and it is reset at the end of each vertical retrace.

The circuitry is shown on sheet 5 of schematic 050-4009. It consists of the two LS393 counters at B-4. The counters are arranged in series and the outputs fed to the memory address MUX in the lower right of sheet 1. The counter is clocked on the leading edge of each t7 state via the JK flop at B-3. It is reset synchronously with CMUX when the video state machine determines that the vertical retrace has been completed.

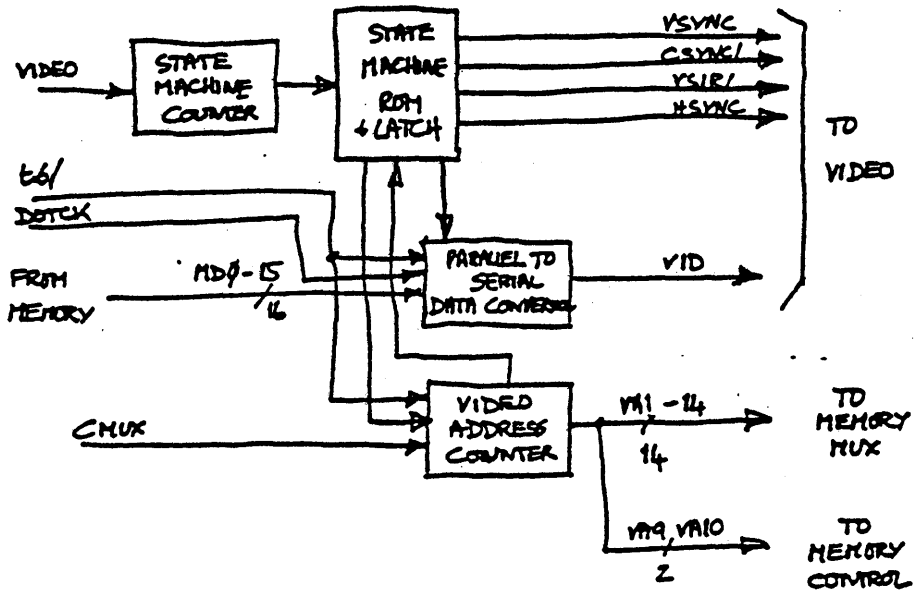


Figure 4-15. Video Control Block Diagram

4.5.2 Video Data Shift Register

This is used to convert the 16-bit words of video data read out of memory into the serial data stream required by the video board.

The circuit is also shown on sheet 3 of the schematics. It consists of the two LS166 devices at B-2 and some associated circuitry. The clock which increments the video address counter is also used to parallel load the shift register with data presented on MD0-MD15.

The DOTCK signal from D-4 on sheet 1 is used to shift the data out to the VID output via the JK Flop at B-1. This flop has been inserted in the data path to ensure a uniform hold length for each data bit. If this were not present, the final bit in each word could be curtailed since the next word is parallel-loaded into the shift register.

The INVID/ signal provides an inverted polarity of the video signal. It may also be used as a serial input to the shift register for test purposes. The Shift Register presents a pixel to the video board every 50 nanoseconds.

4.5.3 Video State Machine

The video state machine is used to monitor the position on the screen at which the current data is to be placed. It counts up to the number of words in one line, performs a horizontal retrace, resets itself and then resumes. At the bottom of the screen it performs a vertical retrace.

The machine is shown on sheet 3 of the schematics and consists of the LS393 counter at C-4, the 6309-1 PROM at B-4 and the LS374 latch at B-4. The counter is clocked with each video access to the memory. The video does access memory during the video retrace periods. Both the counter outputs and the VA9 and VA15 signals are used to address the PROM. The data output from the PROM is latched in the LS374 with the opposite edge of the same signal that clocks the counter.

The HSYNC/ and VSYNC/ signals are presented to the video board for use in horizontal and vertical synchronization of the data on the screen. Other outputs are used to clear the video address counter at the end of vertical retrace, generate the VSIR/ to interrupt the CPU during vertical retrace for cursor positioning and reset the shift register load flop and the state machine counter itself.

The state machine performs 45 normal word fetches and shifts in each line before performing a horizontal retrace and resetting itself. When it detects the 364th line by monitoring VA15, it generates a vertical sync of 6 lines duration, followed by vertical sync termination of an additional 9 lines duration.

4.5.4 Video Page Register

The Video Page Register contains the high-order 6 bits of the address to be presented to memory, which are not provided by the Video Address Counter (A15-A20). This provides a physical address to the memory, i.e. it is not translated by the MMU.

The circuit consists of the LS374 at D-2 on sheet 2. It is loaded by the VAL/ signal, which is decoded from an I/O command at B-1. It is gated as an address whenever the CMUX signal is false.

4.6 Bus Interfaces

The processor board interfaces to three other components within the LISA. These are:

* System bus
* Memory board(s)
* Video board

The bus interfaces to all three are made by a single connector to the motherboard and are shown schematically in Figure 4-16.

(Insert Figure 4-16)

The system bus on the motherboard is extended in part to become the expansion bus. This bus is effectively a subset of the system bus used by the I/O board. It is described in detail in Section 3.4 of this manual.

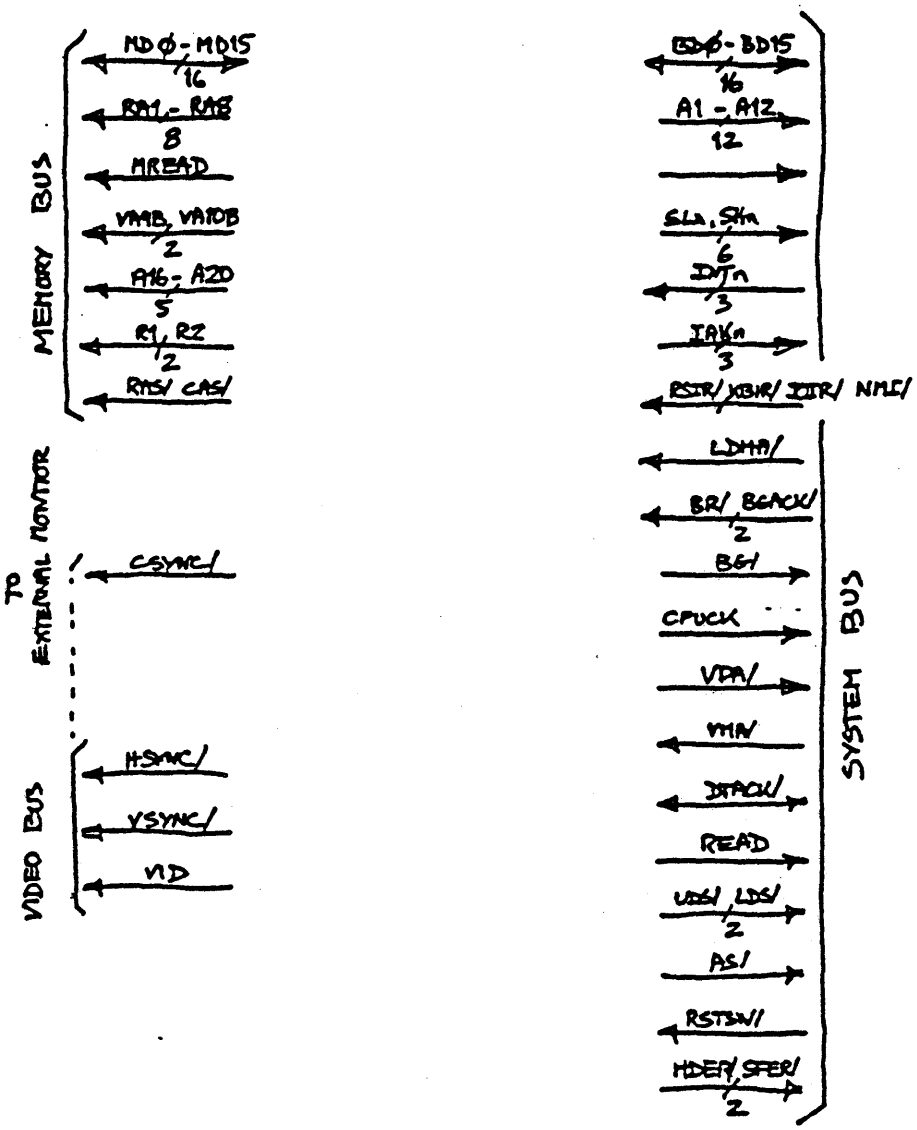


Figure 4-16. Processor Board Bus Interfaces

4.6.1 System Bus Interface

The system bus operates under control of the processor board during most normal operations in the LISA. An exception occurs when a peripheral controller performs data transfer to or from the system memory by means of a DMA operation.

Refer to Figure 4-16 for a signal list and pin assignment. An overview is also shown on sheet 4 of schematic 050-4009.

The system bus interface signals may be broken down into the following categories:

* Address Lines
* Data Lines
* Asynchronous Control Lines
* Bus Arbitration Lines
* Interrupt Control Lines
* System Control Lines
* I/O Slot Enable Lines

Address Lines These consist of the 12 lines A1 through A12 which are used to provide a physical address on the bus. A1 through A8 originate in the LS244 at A-3 on sheet 1, while A9 through A12 come from the MMU output latches at B-2 and C-2 on sheet 2. All signals to the bus are disabled by the BGACK/ signal being asserted.

Data Lines These consist of the 16 lines BD0 through BD16 which are used to transfer data on the bus. All 16 lines originate in the LS245 bidirectional drivers of both the CPU and the memory matrix at A-4 and B-4 on sheet 1. The CPU lines are enabled by the DBON/ signal, which is generated at C-1 on sheet 2 by having both the BGACK/ and SPIO/ signals deasserted. The memory lines are enabled by the MDEN/ signal which is synchronous with the CPUC1 signal whenever both IOCY/ and SPIO/ are false. This is shown at A-4 of sheet 1.

Asynchronous Control These are used to control data transfers made on the bus.

AS/ strobes a valid address which is present on the A1-A12 lines. It originates at C-3 on sheet 1.

READ defines the cycle to be from memory to the accessing peripheral or processor. It originates at C-3 on sheet 1.

UDS/ & LDS/ are upper and lower data strobe to define which half of the BD0-BD15 lines a byte transfer is being made. They originate at C-3 on sheet 1.

DTACK/ is a data transfer acknowledge which indicates to the current bus master that the asynchronous operation has been completed.

CPUCK is the clock used for the CPU itself which is presented on the bus for synchronization purposes.

Bus Arbitration These signals are used to determine which device can operate as a bus master.

BR/ is the bus request line which is asserted by a slave device which wishes to have control of the bus.

BG/ is the grant signal with which the current master allows the requesting slave to take control of the bus. The signal originates directly on the CPU at C-3.

BGACK/ is the signal with which the slave acknowledges that it has accepted the bus grant and has taken control of the bus.

Interrupt Control These are used to determine the source of an interrupt and to acknowledge that the interrupt is being processed.

NMI/, RSIR/, INT0/, INT1/, INT2/, KBIR/ & IOIR/ are all signals presented to the processor board as an interrupt request.

IAK0/-IAK2/ are the coded response to an interrupt request which indicates which requesting device is being serviced.

System Control These signals are used for general control and information within the system.

RESET is a signal to the system to return to its original power-on state.

LDMA/ is the signal to load the upper DMA address latch which is located at D-1 on sheet 4 of the schematics. This signal originates in the peripheral performing the DMA which needs to have the DMA upper address altered.

E is the enable signal for use with 6800-type peripheral devices.

VPA/ is an indication that a 6800-type peripheral is attached to the bus and has been addressed.

VMA/ is the response of the CPU to a VPA/ signal and notifies the peripheral that a valid address is present on the bus.

Slot Enable Lines These lines decode the addresses of I/O slots which are not present on the processor board. They are presented to the bus as enable signals.

SL0/-SL2/ indicate that a slot low decode has been made for an I/O transfer to or from one of the three possible expansion boards. The signals originate in the decode logic at B-1 on sheet 2

SH0/-SH2/ indicate the same for a high decode.

INTIO/ indicates a decode of the processor board I/O space.

4.6.2 Memory Bus Interface

The memory bus is used to provide control signals to the memory boards installed in the system and also to perform transfers of data between the memory matrix and the rest of the system. The signals are located on the same common connector to the motherboard as the system bus interface.

The signals which comprise the memory bus are described below.

A16-A20 are address lines used for internal decoding within the memory matrix and between installed memory boards. Refer to Chapter 5 for details.

RA1-RA8 are the multiplexed address lines used to address the dynamic RAM array in conjunction with the RAS/ and CAS/ timing signals.

MD0-MD15 are the data lines across which a word of data is transferred to and from the memory array. They originate at A-4 to B-4 on sheet 1

MREAD is the memory read signal which indicates the direction of transfer. It is generated from the coincidence of the CPUC1 and READ/ terms at B-2 on sheet 2.

RAS/ and CAS/ are the row and column strobes which indicate the contents of the RA1-RA8 lines. They are generated at D-4 and C-4 on sheet 2.

HDER/ indicates a hard memory error, which is an error found to be uncorrectable if any ECC is present in the memory. It originates at A-3 on sheet 4.

SFER/ indicates a soft memory error, which is an error in memory which could be corrected by any ECC present in the memory.

VA9B and VA10B are video address lines presented to the memory board for use in row refreshing.

R1 and R2 are signals which indicate which of the two possible memory boards in the LISA is to be refreshed.

4.6.3 The Video Interface

The Video Interface also shares the main connector to the motherboard and consists of the signal group listed below.

HSYNC/ is the horizontal sychronization pulse used to indicate to the video circuit that the end of a line has been reached. It originates in the output of the video state machine and is shown at A-3 on sheet 3.

VSYNC/is the vertical sychronization pulse used to indicate to the video board that the bottom of the screen has been reached. It originates in the video state machine at A-3 on sheet 3.

CSYNC/ is a composite of the above two signals and is used as an output to an external video monitor. It originates in the video state machine at A-3 on sheet 3.

VID is the data bit-stream output to the video board. It originates at B-1 on sheet 3.

4.7 Decode and Latches

This section includes the miscellaneous circuitry present on the processor board but not included in the preceding. It can be considered under the following heads:

* I/O decode
* System control latch
* Memory error latch
* System status latch
* Time delay logic

4.7.1 I/O Decode

This is located at the extreme right of sheet 2 of schematic 050-4009. The first stage consists of the LS138 1-of-8 decode device at A-2. This is enabled when an I/O cycle is in process via the IOCY term and the JK Flop at A-2. Both the A9/ and A16 terms must be asserted.

The resulting decode of the A13-A15 terms results in the eight decodes for the ranges shown. All but the high-order decode are presented to the system on the system bus as described in Subsection 4.6.1 above. The final term is CPUIO/ which is used to enable the processor board I/O decode performed by the LS139 decoder at B-2.

The A11 and A12 terms are decoded to give the address block decodes as follows:

RBES/ (F800-FFFF) is the Read Bus Error Status, which is used to gate the status latch at B-2 on sheet 5 onto the data bus.

RMEA/ (F000-F7FF) is the Read Memory Error Address signal, which gates the latched address at B-2 on sheet 3 onto the data bus.

VAL/ (E800-EFFF) is the Video Address Latch signal, which is used to load the upper 6 bits of the video address (A15-A20) at B-2 on sheet 4.

SYSC/ (E000-E7FF) is the System Control Register signal, which is used to load the processor latch. This is the LS259 latched decoder at D-2 on sheet 5. Refer to Subsection 4.7.2.

Decode during special I/O is done by the other half of the LS139 at B-2. It is enabled by the SPIO/ term and decodes UA15 and UA16 to give the ROM/ or MMUIO/ signals. These respectively enable the system boot ROM on sheet 3 and allow data in the MMU registers to be modified or read.

4.7.2 System Control Latch

The processor board control latch is shown at D-2 on sheet 5. It is used to hold control signals used internally on the board. It is loaded by the SYSC/ signal as described in the previous subsection. The signals latched have the following functions:

DIAG1/ & DIAG2/ These are used to force a soft and a hard memory error respectively for diagnostic purposes. They do this when a write operation is performed to memory. This can be seen by the gating terms at D-2 on this sheet.

SEG1 & SEG2 These are used by the system software to select the context in the MMU in which the address translation will take place. They are input to the MMU RAM addressing logic at C-4 on sheet 4. Functional details are discussed in Section 2.3.

START/ This signal is used to disable the start-up mode. It is used when the program is to execute out of RAM after the system has performed a power-on or reset. It enables access to the MMU RAM via the LS32 gate at B-4 on sheet 4.

SFMSK/ This signal is used to suppress the detection of a soft memory error. It is applied to the LS279 Quad RS device at C-2 on sheet 3 to inhibit detection of the SFER/ signal.

VTMSK/ This is used to suppress the vertical retrace interrupt to the CPU. It is input to the interrupt latch at B-2 on sheet 3.

HDMSK/ This signal is similar to SFMSK/ above, but suppresses the detection of a hard memory error. It is input to the latch at B-2 on sheet 3.

4.7.3 Memory Error Address Latch

When either a hard or a soft memory error occurs, the processor board makes the address at which the error occurred available to system software.

The latch consists of two LS374 octal latches, shown at D-1 and D-2 on sheet 3. The address is updated each memory cycle by using the CAS signal from sheet 2 as the gating term to the LS11 gate at C-1 which provides the clock to the latches. The occurrence of either type of memory error prevents any updating by blocking CAS at the This gate.

Resetting the error latch permits normal operation again until the next error occurs.

Note that only the high-order 15 memory lines (A6-A20) are latched because this defines a 64-byte block within memory, which is sufficient to locate the physical page of memory causing the error. System software can map out faulty memory using the MMU in pages as small as 512 bytes.

The low-order bit in the latch is not a memory address bit. It indicates whether a CPU access or a video access was in progress when the error occurred.

For the case of a video error, only bits A15-A20 contain valid information. Bits A6-A14 are undefined.

4.7.4 System Status Latch

The system status latch is shown at B-1 on sheet 3. It consists of an LS279 quad RS flop and an LS244 octal driver. It is interrogated by the RBES/ signal, which originates in the I/O decode logic on sheet 5.

Four of the bits are latched by the LS279. These are:

SFER/ Soft Memory Error, which indicates a recoverable error in memory. This can be inhibited or reset by means of the SFMSK/ signal, in the system control latch at D-1 on sheet 3.

HDER/ Hard Memory Error, which indicates an unrecoverable error in memory. This can be inhibited or reset by means of the HDMSK/ signal from the system control latch at D-2 on sheet 3.

VTIR/ Vertical Retrace Interrupt, which originates in the video state machine on sheet 5. It can be inhibited by means of the VTMSK/ signal from the system control latch on sheet 5.

BUST/ Bus Timeout Error, which originates in the Time Delay Logic at D-4 on sheet 3. This is reset by reading the Memory Error Address latch, which generates the RMEA/ signal./

The other three bits available are not latched and all originate in the Video Control logic on sheet 3. They are:

INVID Inverted video, which may be hand-wired to provide the inverse of the video data normally presented to the video board.

VID Video Data, which is a direct sense of the current bit stream being presented as data to the video board.

CSYNC/ Composite Synchronization pulse, which originates in the video state machine as a composite of horizontal and vertical retrace signals.

4.7.5 Time Delay Logic

The time delay logic is shown at D-4 on sheet 3 and serves two purposes:

* Generation of Power-on Reset
* Detection of Bus Time-out

The logic consists of a 556 dual one-shot, with some associated circuitry.

The POR (Power-on Reset) signal is generated whenever the RSTSW/ (Reset Switch) input from the system bus is pulsed low. The POR signal is true for approximately 1 second.

The BUST/ (Bus Timeout) signal is generated whenever a period of 30-300 microseconds elapses without an AS/ (Address Strobe) signal occurring. This usually indicates that the CPU is awaiting a response from a peripheral which is either not present or unable to respond.

CHAPTER 5

THE MEMORY BOARDS

The LISA system is designed to allow for a flexible configuration of memory with the rest of the system.

The main memory constitutes one of the three spaces into which the LISA physical memory space is divided. The other two are I/O space and Special I/O space.

The main memory occupies 2 MBytes of space and is further subdivided into two spaces of 1 MByte each, which correspond to each of the two memory boards which may be present in the system. Each memory board is capable of sensing which of the two slots it is presently located in because one pin of the board socket is grounded on slot 2 and left open on slot 1. The lower memory board occupies slot 2 and the higher occupies slot 1.

In order to have memory that is contiguous, when each board may not necessarily have a full 1 MByte available on it, a scheme is implemented whereby both boards begin at their mutual boundary of 100000H and fill outward from this point to the capacity of the board.

To accommodate partially-stuffed boards and to maintain interchangability between slots, the physical top row of the board in slot 2 (the lower board) must be the top of that board's address space. Conversely, the top row of the board in slot 1 (the upper board) must be the bottom of that board's address space.

The amount of memory in slot 2 determines the physical starting address of the memory available in the system. Likewise the amount of memory in slot 1 defines the physical ending address. Since the current memory boards are designed around 64K-bit dynamic RAMs, the smallest possible increments are of 128K-bytes each (64K-words of 16 bits each).

Because both the beginning and ending physical addresses are a function of the amount of memory present, the boot ROM must contain a routine which establishes the size and the location of the memory available in each particular LISA system. The routine must then configure the MMU RAM to place some part of the physical address at logical address zero.

Since the memory boards can be installed in any order or configuration, the operating system must add the required base address when modifying the MMU RAM contents for any reason.

Note that the Video Page Address latch contains a physical address, which must take the actual physical memory configuration into account.

5.1 Memory Block Diagram

Since each memory board is functionally identical, this section discusses the block diagram of a single board only.

The memory board consists of an address decode section, the memory matrix itself and a parity detection and generation section. The bulk of the memory control and timing signals are generated on the processor board and provided on the memory bus. Refer to Section 4.6 for a discussion of how these signals are generated.

The memory block diagram is shown in Figure 5-1.

(Insert Figure 5-1)

The matrix itself consists of four rows of 18 64Kx1 bit dynamic RAM devices. The extra 2 bits are used as parity bits to check the integrity of data being read from the memory.

The parity logic both generates and checks the parity of data being written and read respectively. The decode logic is used to interpret the control signals to allow the correct RAS and CAS signals to select the proper row.

The latches and drivers are used to reduce loading on certain critical signal lines.

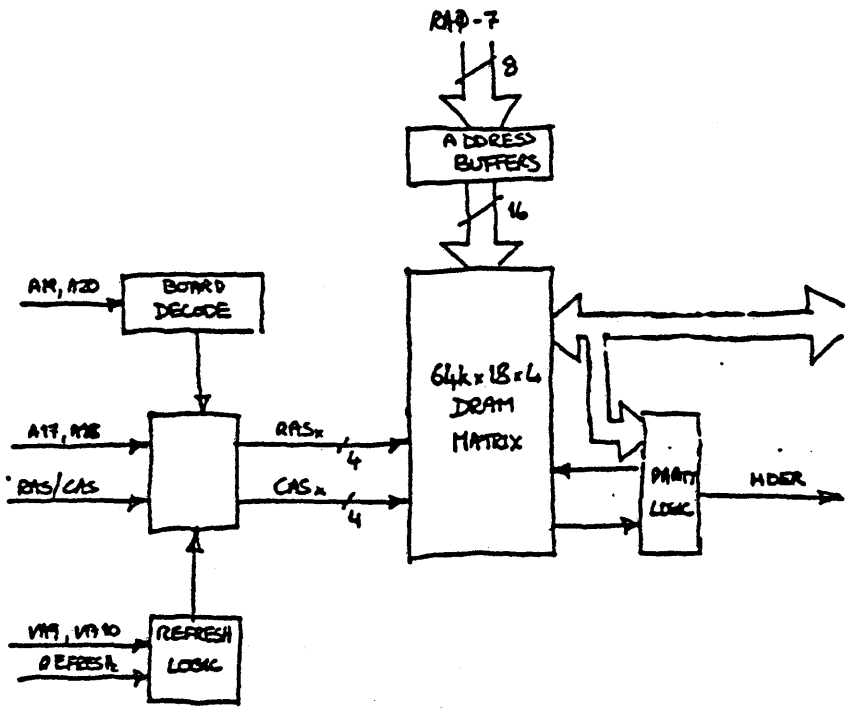


Figure 5-1. Memory Block Diagram

5.2 Row and Column Addressing

There are three types of memory accesses -- CPU, Video and DMA. The CPU and DMA accesses are identical with the exception of some timing differences, due to inconsistencies in the DMA controller's reproduction of CPU signals. All accesses appear identical to the memory board. The address multiplexers on the processor board multiplex not only the CPU/DMA address with the Video address, but also multiplex the matrix row address with the matrix column address in sync with the row and column address strobe signals.

Refer to schematic 050-4010 from Appendix B in the following discussion.

5.2.1 Address Lines

The eight multiplexed address lines RA1-RA8 at D-4 on sheet 1 come from the processor board via the memory bus on P1. These are loaded into the dual S373 transparent latches at D-3 in duplicate form by the LTCH/ signal.

The LTCH/ signal originates in the JK Flop at C-3, and can be seen to be the DOTCK signal divided by two. It is active only when CAS/ is deasserted to ensure that the address for the RAMs is stable for a sufficient period.

The address lines to the matrix consist of the duplicated and latched RA1-RA8 signals, organized as an upper and a lower address line to minimize signal loading and delay. These are shown at D-2.

5.2.2 Slot Decode

The SLOT signal is shown at C-4 on sheet 1. Depending on the slot in which the board is located, this will be pulled to GROUND in slot 2 (low-order board) or allowed to be pulled up to +5V in slot 1 (high-order board).

SLOT is presented to the matrix decode logic and also to the pair of LS02 gates at B-3. The other leg of these gates is a decode of the A19 and A20 terms by the LS139 decoder at B-3.

As can be seen from the connection of the Y1 and Y2 outputs to the gate, a logic high will be output from the S32 gate at C-3 if either:

* SLOT & A20 are low while A19 is high
* SLOT & A20 are high while A19 is low

This selects between the two boards using A19 and A20. The addressing system is shown schematically in Figure 5-2.

(Insert Figure 5-2)

Note that the output signal from this section is used to gate only the CAS signal to the matrix. This is because no change is made to the contents of RAM when a RAS-only cycle is performed.

5.2.3 Matrix Device Decode

The A17 and A18 signals from the memory bus are presented to the S138 3-to-8 decoder at B-3. The third input is the SLOT signal from the previous subsection. This results in two groups of four outputs, the high-order ones being for the high-order board slot and the low-order four being for the low-order board slot.

These signals are presented to the two rows of gates which follow to allow for memory to be physically located next to the 100000H boundary discussed in the introduction to this chapter.

Note that the RAS0/ output to the matrix on sheet 3 is a product of the Y4 decode output if SLOT is high but a product of the Y3 output if SLOT is zero. That means that it corresponds to the high-order block of the matrix in the low-order slot, but the low-order block in the high-order slot. Examination of all the other matrix strobe signals will reveal a similar pattern.

5.2.4 Matrix Address Strobes

The RAS/ signal from the processor board enters the memory board from the memory bus at A-4. It is used to gate whichever of the inputs to the four S00's at A-2 has been enabled by the matrix decode logic, described in the preceding subsection.

(SLOT.A20) -> Board 1 selected

(SLOT/.A19) -> Board 0 selected

(A17/.A18/.CAS/.SLOT) + (A17.A18.CAS/.SLOT/) -> CAS0/

(A17.A18/.CAS/.SLOT) + (A17/.A18.CAS/.SLOT/) -> CAS1/

(A17/.A18.CAS/.SLOT) + (A17.A18/.CAS/.SLOT/) -> CAS2/

(A17.A18.CAS/.SLOT) + (A17/.A18/.CAS/.SLOT/) -> CAS3/

This scheme permits the system memory space to be filled from the 1 Mbyte midpoint in both directions. This eliminates gaps in the physical present when the full 2Mbytes of memory are not installed.

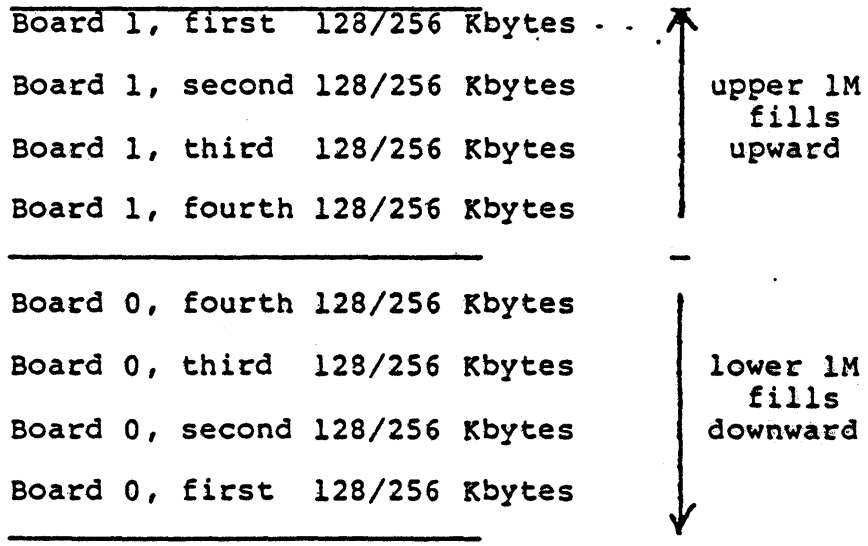


Figure 5-2. Memory Address Decoding

The third input leg to the S10 gates at A-3 which drives the S00's derives from the decode of VA8 and VA10 from the LS139 2-to-4 decoder at A-3. This is enabled by the RFSH/ (Refresh) signal. Since the video address register increments sequentially, it is used to provide refresh to a block of memory not currently being accessed concurrent with a video access of memory.

The CAS/ signal from the processor board enters the memory board at C-4 and gates the selected CASx signal, provided that the LS00 gates at B-3 are enabled.

Only one CASx/ will be active during any one access. During a CPU or DMA access, only one RASx/ per board will be active, but in a video access, a second RASx/ will be active to perform matrix refresh.

5.3 Data and Parity

The logic concerned with data transfer and parity is located on sheet 2 of schematic 050-4010. Parity is stored in odd form for each byte in the memory matrix and generates a hard memory error if read as an even parity. There is no error correction circuitry implemented in the current LISA memory. As a consequence, soft memory errors are not generated by the memory board.

5.3.1 Memory Data Lines

The bidirectional data lines on the memory bus MD0-MD15 are connected directly to the DxIN inputs of the matrix.

They are also connected to two LS280 parity generator/checkers at C-3 and A-3, which generate the odd parity for each of the upper and lower bytes being written into memory. The EVEN outputs are written into the corresponding bit in the matrix, resulting in an 18-bit word being used to store the two bytes, each with odd parity.

Data being read from the matrix appear at the DxOUT outputs, and is passed into the two LS373 transparent octal latches shown at A-2 and C-2. The data is latched on the trailing edge of the main RAS signal.

At the same time, the corresponding two parity bits are latched into the LS375 shown at C-4 and A-4. These are then gated with the MREAD signal to ensure that the ninth bit is in fact stable during a write operation before

being presented to the parity generator/checkers to establish if parity is good for both bytes being read.

Output data is enabled onto the MD0-MD15 lines of the data bus by the S03 AND gate output at C-3. This term is asserted if both MREAD and LBDSL are asserted. The LBDSL originates at C-3 on sheet 1. It shows that the board has been selected clocked on the trailing edge of RAS.

A single byte can be written to or read from memory under control of the LDS/ and UDS/ bus signals at C-4 and A-4 respectively. The other half of the memory word is read from memory, but is not passed through the LS373.

5.3.2 Memory Parity

Odd, byte-wide parity is generated and tested in the LISA memory by means of two LS280 devices. Each data byte has its own device associated with it. The lower byte generates the PIL bit at C-2, while the upper byte generates the PIU at A-2.

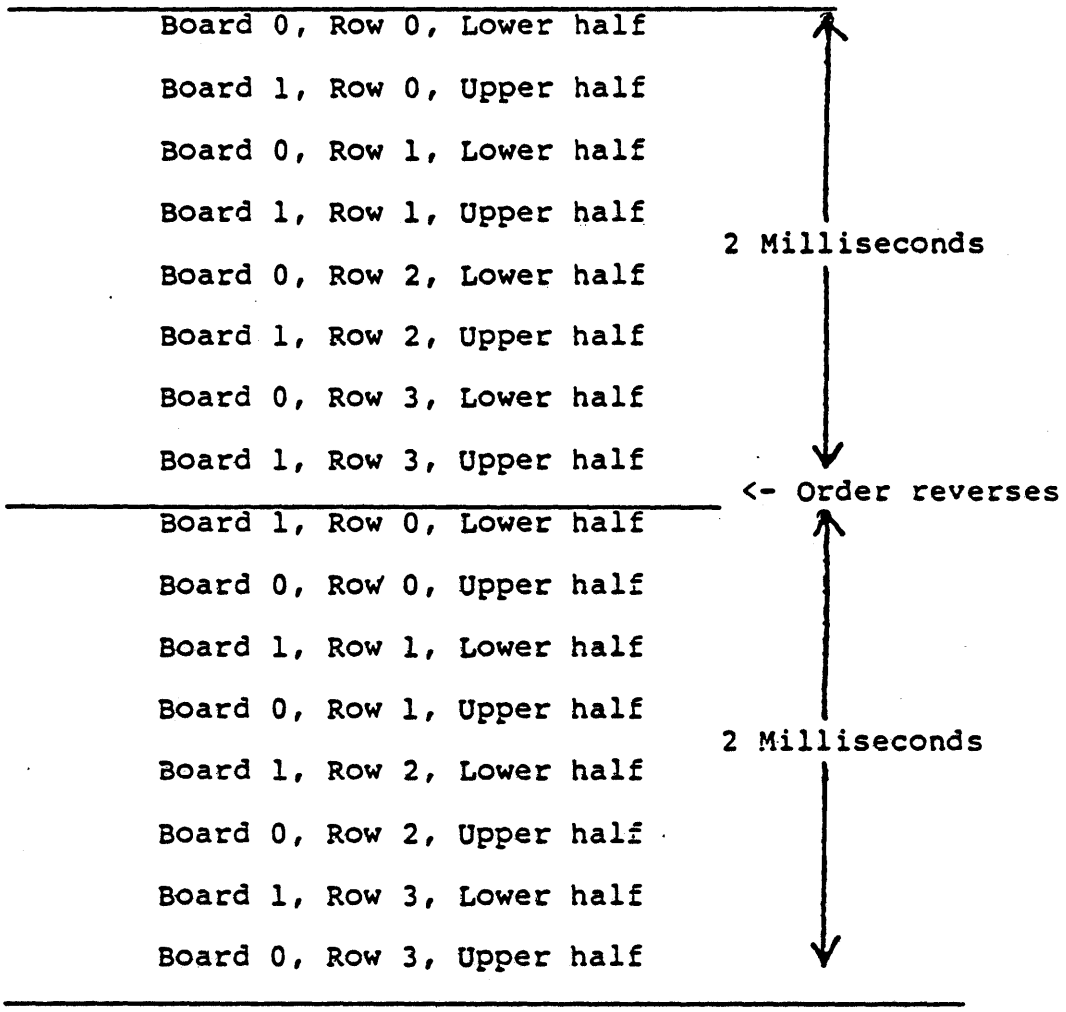
When a word is read from memory, the corresponding two parity bytes are read and latched while the parity is checked. For a word access, if either byte results in an even parity, the JK Flop at B-3 is set. This results in a HDER/ signal being presented to the processor board to denote a memory error. For a byte access, parity is checked only for the byte being accessed. The parity of the other byte is ignored.

The HDER/ signal is also fed back into the parity logic for use in parity diagnostics. Note that it is also latched until a write operation is performed to clear this.

If a parity error occurs during video access to memory, it will be reported to the CPU 60 times per second until the parity is re-masked or the word causing the error is rewritten. This is true even if the CPU itself never accesses the memory location causing the parity error.

5.3.3 Memory Refresh

Refresh cycles occur during a video access by selecting multiple rows of memory devices on the board. Since the video addresses cycle through all device row addresses every 128 accesses, this feature is used in place of a separate hardware refresh address generator.



The upper and lower halves of 64Kbit RAM devices are selected by the polarity of the RA8 input at RAS time.

RAM devices which require refresh every 128 cycles have their upper and lower halves refreshed simultaneously and therefore require only 2 msecs for full refresh.

RAM devices which require refresh every 256 cycles need the full 4 msec refresh cycle time for full refresh.

Figure 5-3. LISA Memory Refresh Pattern

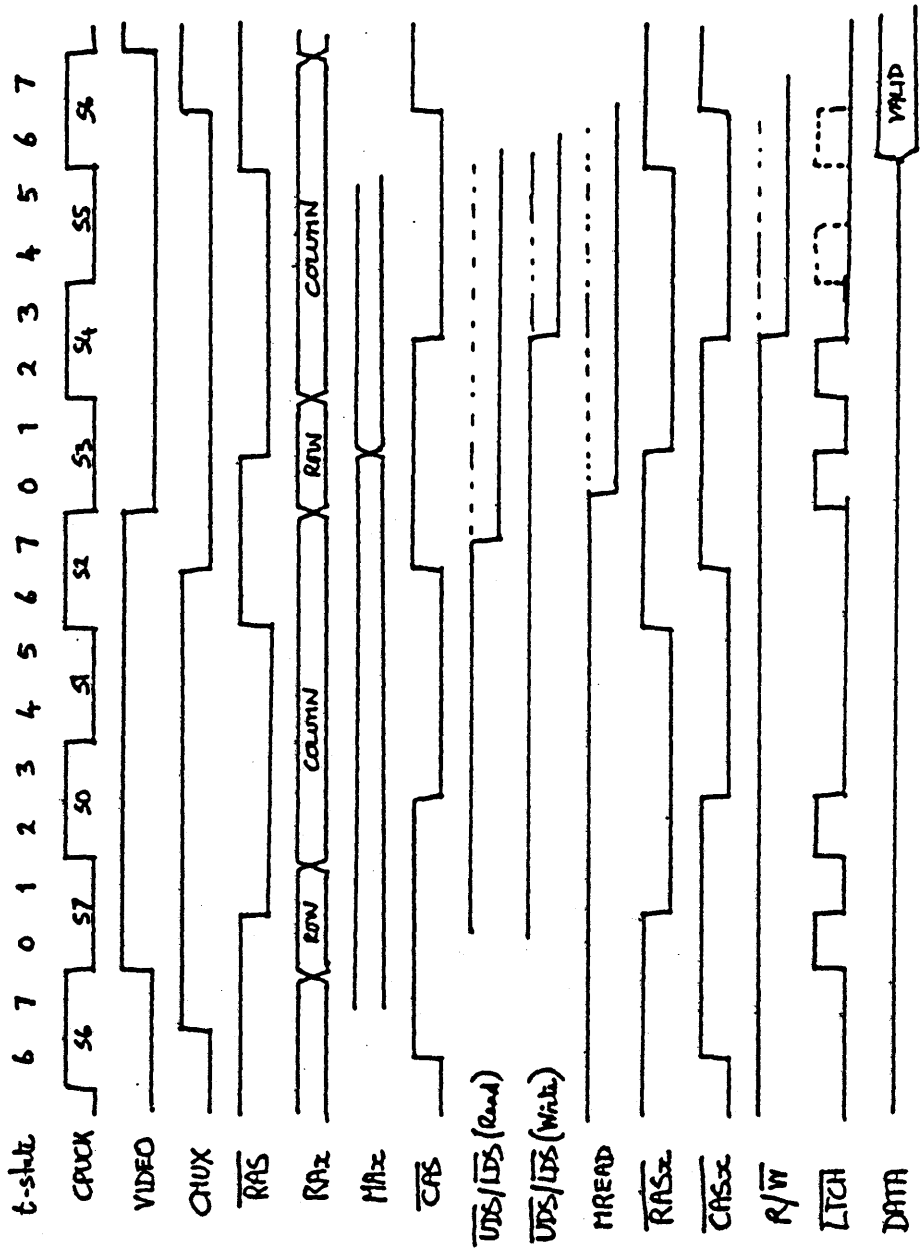


Figure 5-4. LISA Memory Timing Diagram

Refresh alternates between installed memory boards every 128 cycles. The order of alternation is reversed after every refresh pass in order to supply the correct refresh to 256-cycle refresh RAM's, should these be installed. This is done by means of the VA8 and VA11 signals from the processor board. This results in the pattern shown in Figure 5-3.

(Insert Figure 5-3)

5.4 Memory Timing

As with most system, the timing associated with memory access is one of the critical constraints around which the system has been designed. The timing diagram for the memory board is shown in Figure 5-4.

(Insert Figure 5-4)

5.4.1 Row Selection Timing

The most critical timing in the memory system involves the decode of the A17 and A18 address lines. Both these lines are the product of the address translation within the MMU on the processor board, and consequently reach the memory board with some delay after the AS/ signal which begins the cycle. Since these signals are also used to generate the correct RASx/ signal within the matrix, it may not be possible to select the board before RAS time.

The difficulty is solved by generating RAS on both boards in any case and using the CAS signal to define which part of the matrix is in fact being accessed. This is shown in Figure 5-5.

(Insert Figure 5-5)

5.4.2 Address Multiplex Timing

In order for the correct word in memory to be accessed, the address is presented to the matrix in two "halves". This is also shown in Figure 5-5.

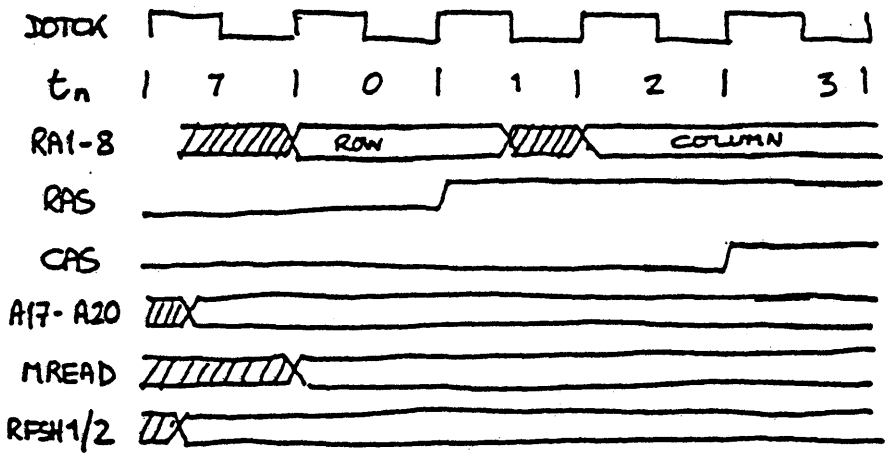


Figure 5-5. Memory Row Address Timing

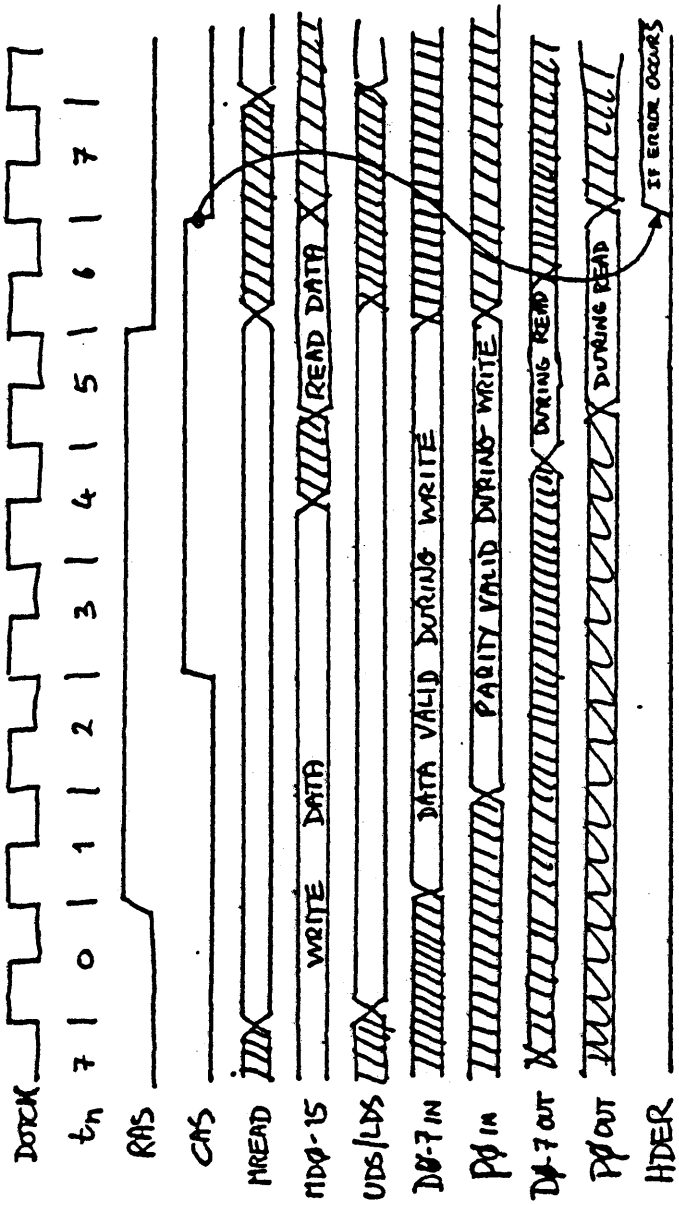


Figure 5-6. Memory Data and Parity Timing

The two "halves" correspond to the row address and the column address of the word being accessed. The processor board makes each of these available in turn on the RA1-RA8 lines. It uses the RAS/ or CAS/ signals to strobe the appropriate one.

The multiplexed address is latched into the S373's with the LTCH/ term. This has the waveform shown in Figures 5-4 and 5-6. The Flop generating it toggles at the frequency of DOTCK whenever the CAS/ term is deasserted. Otherwise, it remains asserted.

5.4.3 Data and Parity Timing

The constraints on the data and parity signals of the matrix are less rigorous than those for the address selection. The timing is shown in Figure 5-6.

(Insert Figure 5-6)

CHAPTER 6

THE I/O BOARD

The LISA I/O board is the principal means by which the system communicates with its peripherals. The board contains the peripheral controllers for the external interface connectors of the LISA. The board must be present in any LISA system.

6.1 I/O Board Block Diagram

The main features on the I/O board can be itemized as follows:

* Floppy Disk (FD) Controller
* Dual Serial I/O Port Interfaces
* Parallel Port Interface
* Keyboard/Mouse Interface
* Miscellaneous Logic

These are shown diagrammatically in Figure 6-1.

(Insert Figure 6-1)

The data bus on the I/O board consists of three separate sections, which are shown in Figure 6-1. These are:

* The System Bus data lines from off-board
* The Disk Bus, internal to the FD controller
* The D-Bus connecting to all other peripherals

Note that some control functions are grouped together on the same interface device. This is done both for convenience and to minimize hardware.

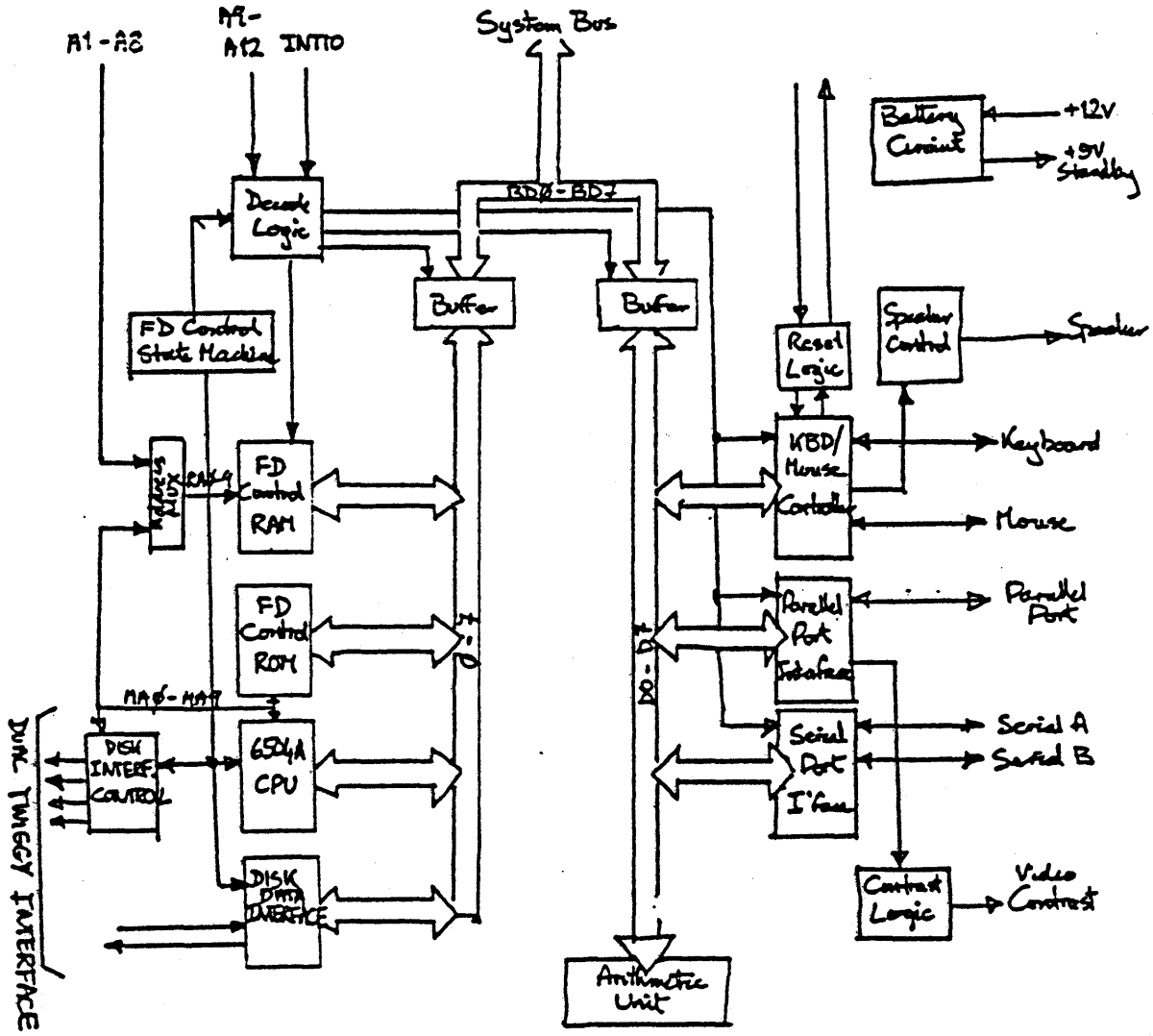


Figure 6-1. I/O Board Block Diagram

6.2 Floppy Disk Controller

The floppy disk controller is designed around a 6504A slave processor and its associated memory and logic, as shown in Figure 6-2.

(Insert Figure 6-2)

The logic schematic of the controller can be found on sheet 4 of schematic 050-4008, shown in Appendix C. The controller communicates with the main LISA system by means of an area in its dedicated memory. The CPU places commands and data to be written on the disk at locations in this RAM. The CPU can also access status information and data read from the disk which is placed in the RAM by the slave processor.

Operation of the FD controller is described in Section 6.3.

Timing for the controller is generated asynchronous to the main system by a clock generator internal to the controller. This provides clocking to the slave processor and to control latches.

The control lines to the dual disk drives are generated by addressable latches which are loaded by slave processor operation.

The data interface to the drives is controlled by a state machine, which is used to monitor and control this interface under control of the 6504A.

6.2.1 Slave Processor and Memory

The heart of the controller is a 6504A 8-bit processor at D-3, which accesses two types of memory. A 4Kx8 program ROM at D-3 contains the slave processor control routines with which it performs manipulation of the interface to the dual floppy disk drives and also transfer of data to and from the main system.

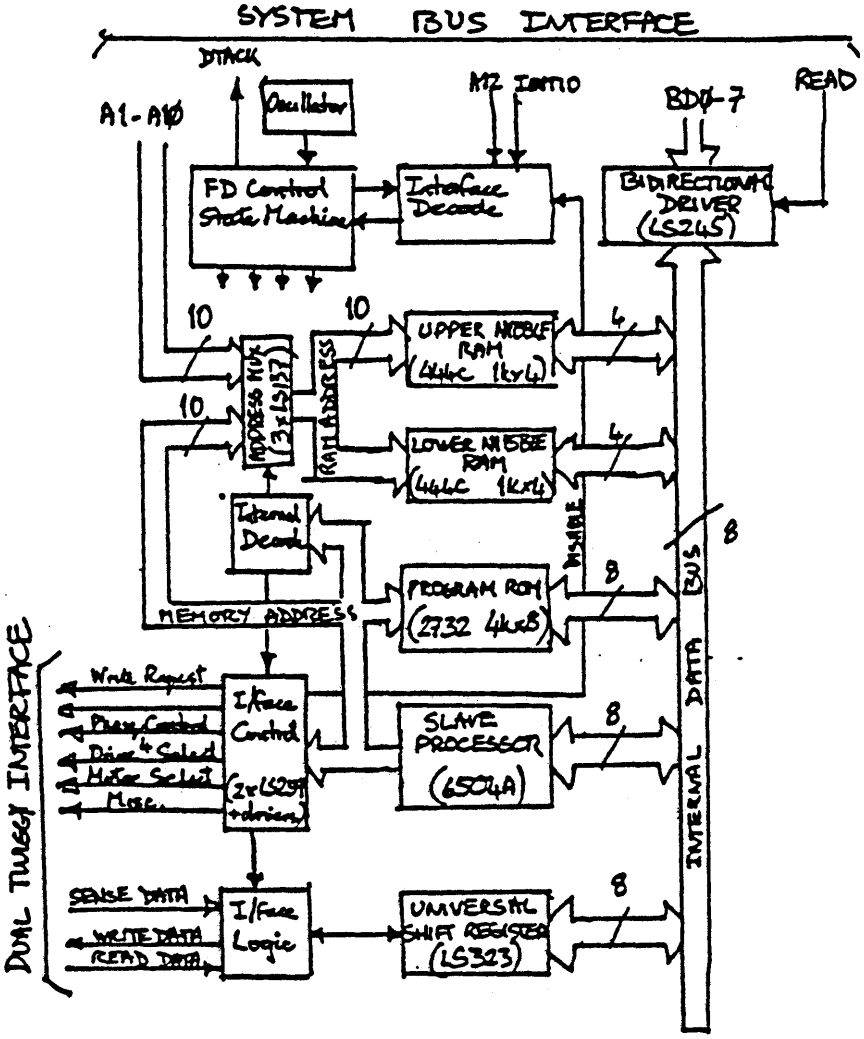


Figure 6-2. Floppy Disk Controller Block Diagram

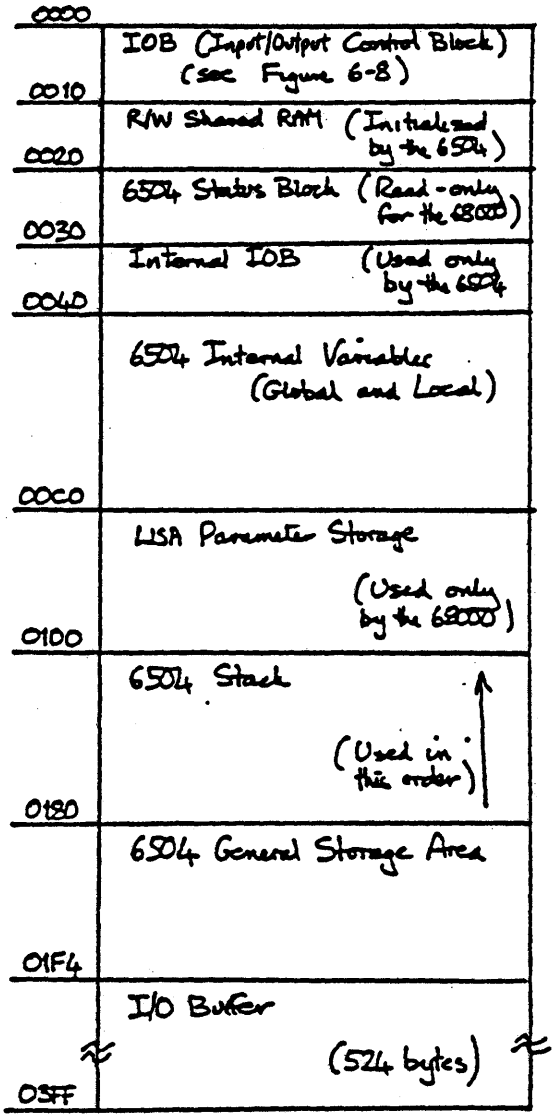


Figure 6-3. Floppy Disk Controller Address Space

Data in the process of being transferred is stored in the two parallel 1Kx4 RAM devices at D-3 and D-4. These provide a 1K-byte buffer space, common to both the 6504A and the main processor, for use as a data buffer. The RAM is also used for storage of command strings from the system to the controller and for status information from the disk. The RAM is functionally divided as shown in Figure 6-3.

The bidirectional LS245 octal buffer at D-4 divides the internal floppy disk controller data bus from the main system bus data lines BD0-BD7. The internal bus connects to the 2732 PROM, the 6504A processor and the upper and lower nibbles are connected to one 444C RAM each. In addition, the bus connects to the LS323 universal shift register at D-2.

The 8K-byte address space of the processor is addressed by means of the internal address bus MA0-MA12. These connect directly to the program ROM and are multiplexed with system bus address lines for accesses to the buffer RAM.

The internal memory bus is also used to select the control lines to be manipulated on the disk interface via the LS259 selectable latches at B-1 and C-2. It provides internal decodes using the LS139 dual 2-to-4 decoder shown at B-2 and B-3.

6.2.2 System Bus Interface

The interface to the system bus consists of the devices shown on the left-hand side of sheet 4 of the schematic. It consists of the bidirectional data bus transceiver at D-4, the three LS157 2-to-1 Multiplexer devices at C-4 to A-4 and some control circuitry at A-3 and A-4.

The slave processor is capable of locking out any communication on the main bus by means of the DIS signal. This is done because many routines within the disk controller are time-critical. Accesses from the main system would render this impossible.

DIS is one of the inputs to the LS32 gates at A-3. When this signal is asserted, the J input of the JK Flop at A-3 is always asserted. This means that the output is always true, and that the second JK Flop at A-3 is always set, giving an output at pin 6 which is always asserted. This forces the S input on the LS157 Multiplexer to select the MAx inputs at all times and disables the bus transceiver at D-4.

The Q/ output of the second LS109 flop at A-3 is gated into another LS109 JK Flop at A-2. This generates the DTACK/ signal on the system bus only if the Q/ output from A-3 is asserted. This can happen only when DIS is deasserted.

Thus any system attempt to communicate with the controller while DIS is high will not result in a DTACK/ acknowledgement signal. The access cycle will hang, waiting for this signal until the bus timeout on the processor board triggers and the BERR/ signal is generated. Refer to Section 4.7 for a discussion of this.

Note that the DTACK/ signal is generated by an LS367 tristate driver device, which is enabled only when the Flop at A-3 is reset (Q output low.)

6.2.3 Timing Generation

The floppy disk controller runs asynchronous to the the main LISA system. Its timing is controlled by logic built around an LS161A 4-bit counter.

Timing is provided by a 16MHz oscillator, located at B-3 on sheet 4 of schematic 050-4008. The output is cleaned up by the schmitt trigger NAND gates before being presented to the LS161A counter at B-3. Pin 5 of device U6A may be used to provide an alternative clock input if pin 1 is pulled to ground to disable the normal clock.

The timing state sequence that the counter passes through is dependent on whether the controller is communicating with the system or if it is performing internal control functions with the system locked out. The state machine goes through eight states in the former case and nine in the latter. Refer to Figure 6-4 for an overview of the states which are passed through.

(Insert Figure 6-4)

If the controller is communicating with the system, the DIS signal will be deasserted. This means that the LS109 JK flop at A-3 will be in the reset condition, resulting in a low condition on the P0 input to the LS161A at B-2.

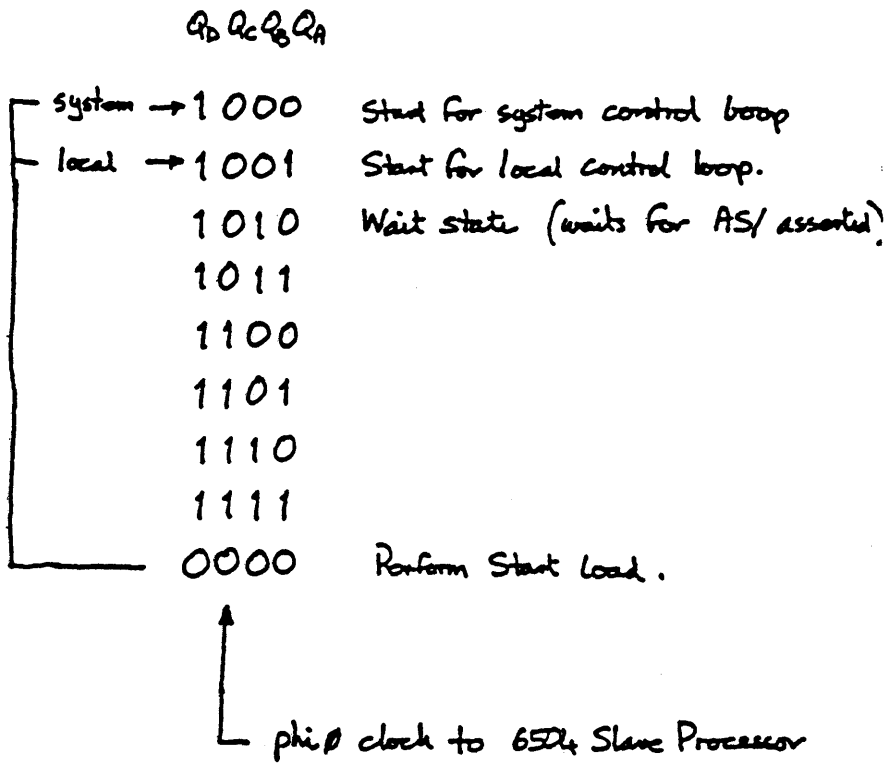


Figure 6-4. FD Counter Timing States

When the counter rolls over to zero, the Q3 output goes low and causes the P-inputs to be loaded. In this case, an 8 will be loaded since the P3 input is pulled high and all other inputs are low. At this point, the Q1 output is low, which results in the CEP input being asserted. Since the CET input is pulled high, the counter is enabled and will begin to count.

The clock input is running and the machine will clock up from state 8 to 9. This causes the Q0 output to go high and to sample whether the CPU is attempting to access the controller by clocking the lower LS109 JK flop at A-3. The Q output becomes deasserted in this case, which enables the DTACK driver at A-2. It is also presented to the upper flop at A-3, which acts as the system/internal mode selector and uses the 6504A's phi2 clock to present a high to pin 4 of the LS00 at A-2.

When the counter clocks from 9 to 10, the Q1 output goes high, which presents a low input to the j input of the LS109 JK flop at A-2. This in turn asserts the DTACK/ signal to the processor to initiate the I/O data transfer cycle. This also deasserts the CEP input to the counter, which means that the counter and thus the entire controller hangs waiting for the processor to respond.

Processor response is detected by means of the AS signal. When this is deasserted, the upper flop at A-3 is preset, which drives the CEP to its asserted state again. The AS also presets the lower flop, which disables the DTACK/ signal. The counter then proceeds in sequence through states 11 to 15 before rolling over and beginning the sequence again.

In the case where the system is not attempting to access the controller, the lower flop at A-3 will be set. This causes the counter to begin in state 9, since the P0 input is high when the PE load signal is asserted.

The Q0 output is used solely to clock the disable flop at A-3. Due to the asynchronous nature of this clocking with the system interface, the second flop at B-3 has been added to give a stable period to the state.

The Q1 output performs two functions. Firstly, it is used as a clock to drive the disk state machine at D-1 and D-2. Secondly, it is used as a gating term for the DTACK flop at A-2, which also halts the counter to wait for processor response.

The Q2 output is used only to provide the input clock to the processor at C-2. This defines the period of the phi2 clock output by the processor.

The Q3 output is used exclusively to reset the counter to its initial count state.

The phi2 clock from the 6502A is used to clock the upper flop at A-2 and also to provide timing for loading the control latches at B-1 and C-2.

6.2.4 Disk State Machine

The interface to the drive itself includes a state machine whose purpose it is to organize the data byte parallel/bit serial translation during transfer to and from the drive.

The state machine consists of three main devices, as shown in Figure 6-5. The central device is a 256x8-bit ROM at D-2, which works in conjunction with the hex D-Flop LS174 at D-1 and the 74LS323 8-bit universal shift register at D-2.

(Insert Figure 6-5)

The processor uses two outputs of the LS259 to select one of four operations within the state machine. In addition, data is made available on the internal controller data bus for parallel loading into the shift register.

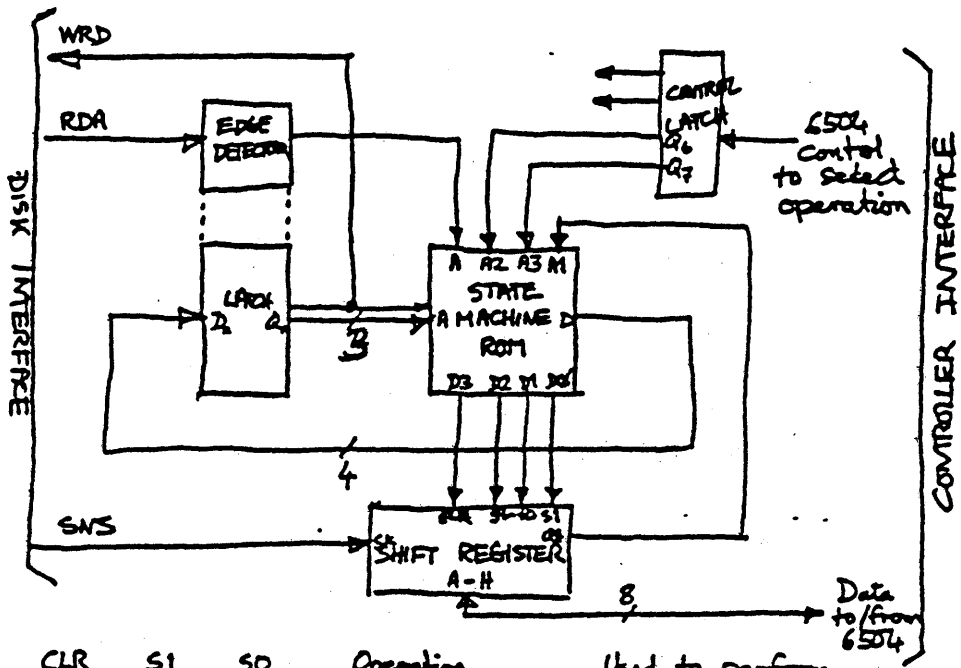
The state machine is clocked by the Q2 output of the timing counter described in Subsection 6.2.3 above.

The interface signals which connect to this section of the logic are as follows:

RDA is input from the drive and is the Read Data line containing serial data from the selected head and drive.

WRD output to the drive is the Write Data line for the serial data written by the selected drive and head.

SNS is input from the drive and is the sense line which presents the selected status information on the dual drive system.



CLR	S1	S0	Operation	Used to perform
1	0	0	Hold	Present data to controller
1	0	1	Shift Left	Receive data from disk
1	1	0	Shift right	Present data to disk
1	1	1	Load.	Receive data from controller
0	x	x	Clear.	

Q_H holds MSB. When it is a "1", the byte is assembled.

Figure 6-5. Disk State Machine

6.2.5 Stepper Motor Control

The control of the stepper motor in the drives is performed with the LS259 8-bit addressable latch at C-2. The various bits are selected by means of the low-order internal controller address lines.

These are passed through line drivers to provide the following signals. Note that the first two signals do not actually control stepper movement. The signals are:

WRQ/ is the Write Request line, which is output to the drive to permit write operations to be performed.

HDS is the Head Select line, which is output to the drive to indicate which of the two heads on the selected drive is to be used to write or read data. It also is used to select which status data is to be read on the sense line.

Phi0-Phi3 are the four phase control lines output to the drive to control the carriage motion performed by the stepper motor. In addition, the Phi0 signal is used in the selection of status data read on the sense line.

The first two signals are placed here only for convenience. The motor phase control line operation is described in Subsection 6.3.5

6.2.6 General Drive Control

The function of the general drive control logic is to manipulate lines on the drive interface. This is performed by the LS259 8-bit addressable latch at B-1 with some additional logic.

The latched bits are addressed by the low-order four lines on the internal controller address bus.

Two bits are used to provide information to the CPU:

FDIR is the Floppy Disk Interrupt Request. It is fed into the inverting driver shown at B-4 on sheet 3 where it generates the IOIR/ interrupt request to the processor. It is also presented to the PB4 inputs of the keyboard interface device for polling by the CPU.

DSKDIAG is the Disk Diagnostic line which is presented to the PB7 input of the Parallel Port interface device for polling by the CPU to indicate that the controller is performing disk diagnostics.

One bit is used for internal control on the I/O board:

DIS (Disable) This is the control signal which the 6504A uses to inhibit the interface to the system when it is the process of an operation which must not be interrupted.

Four bits are used as control signals to the disk drives:

MT0/ & MT1/ are the motor control lines. They are output to the two individual disk drives to control the spindle rotation speed.

DR0/ & DR1/ are the drive select lines which select between the two drives in the dual drive assembly.

6.3 FD Controller Operation

The FD controller manipulates the control lines to the drives to read data from and write data to all tracks and surfaces of the disk drive. It communcates with the CPU by means of a common RAM space on the I/O board, shown in Figure 6-3.

The CPU requests the FD controller to perform operations by means of commands placed in the GOBYTE in location 0000, plus other parameters within the I/O block as required. The 6504 command structure is shown in Figures 6-6a through 6-6r

(Insert Figure 6-6)

Execution of the macro commands received from the CPU are fully under control of the 6504. Upon completion of the operation, the status of the controller is available in the I/O control block for interrogation by the CPU. Figure 6-7 shows the general flow of macro command transfer and execution.

(Insert Figure 6-7)

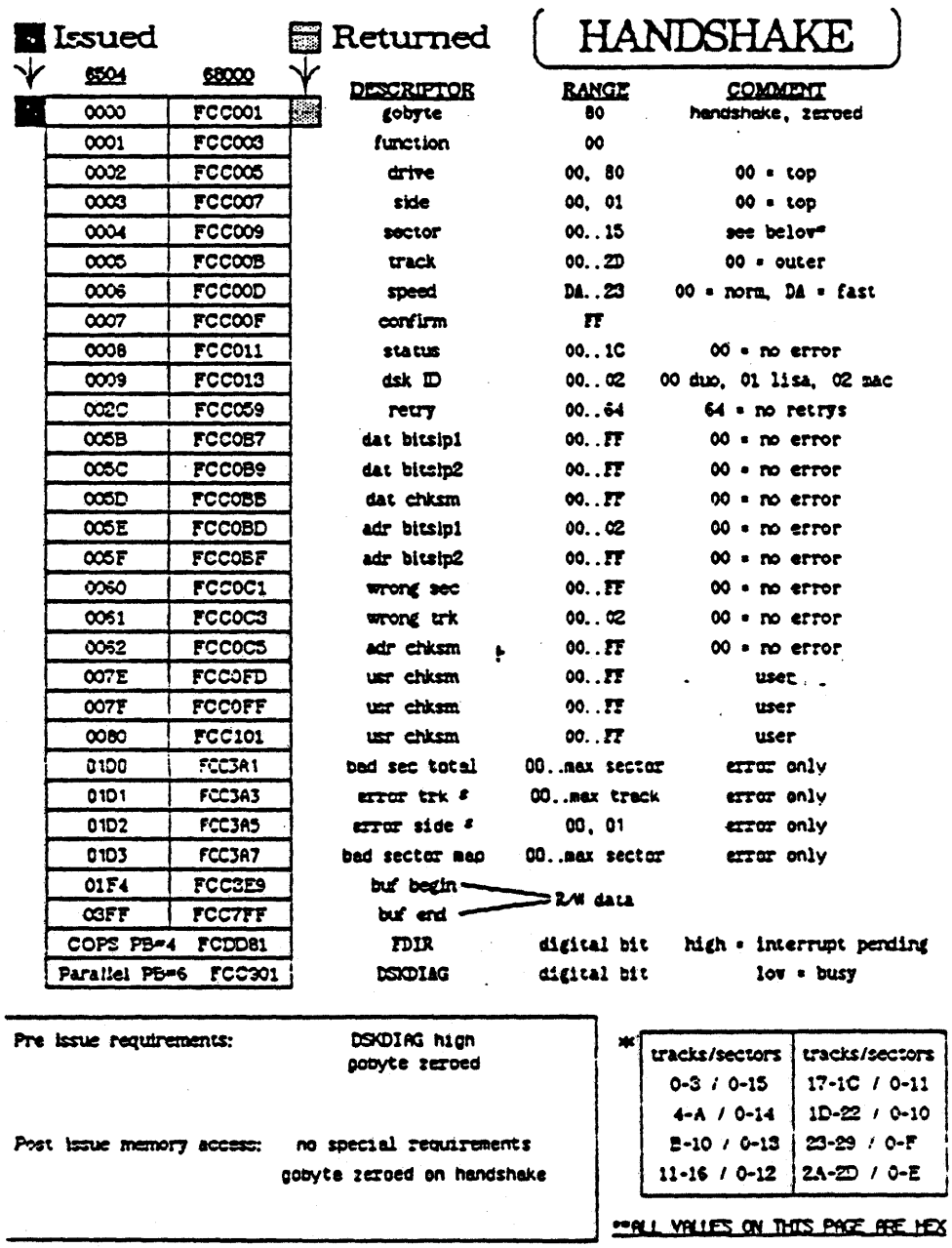


Figure 6-6a. FD Controller Handshake Command

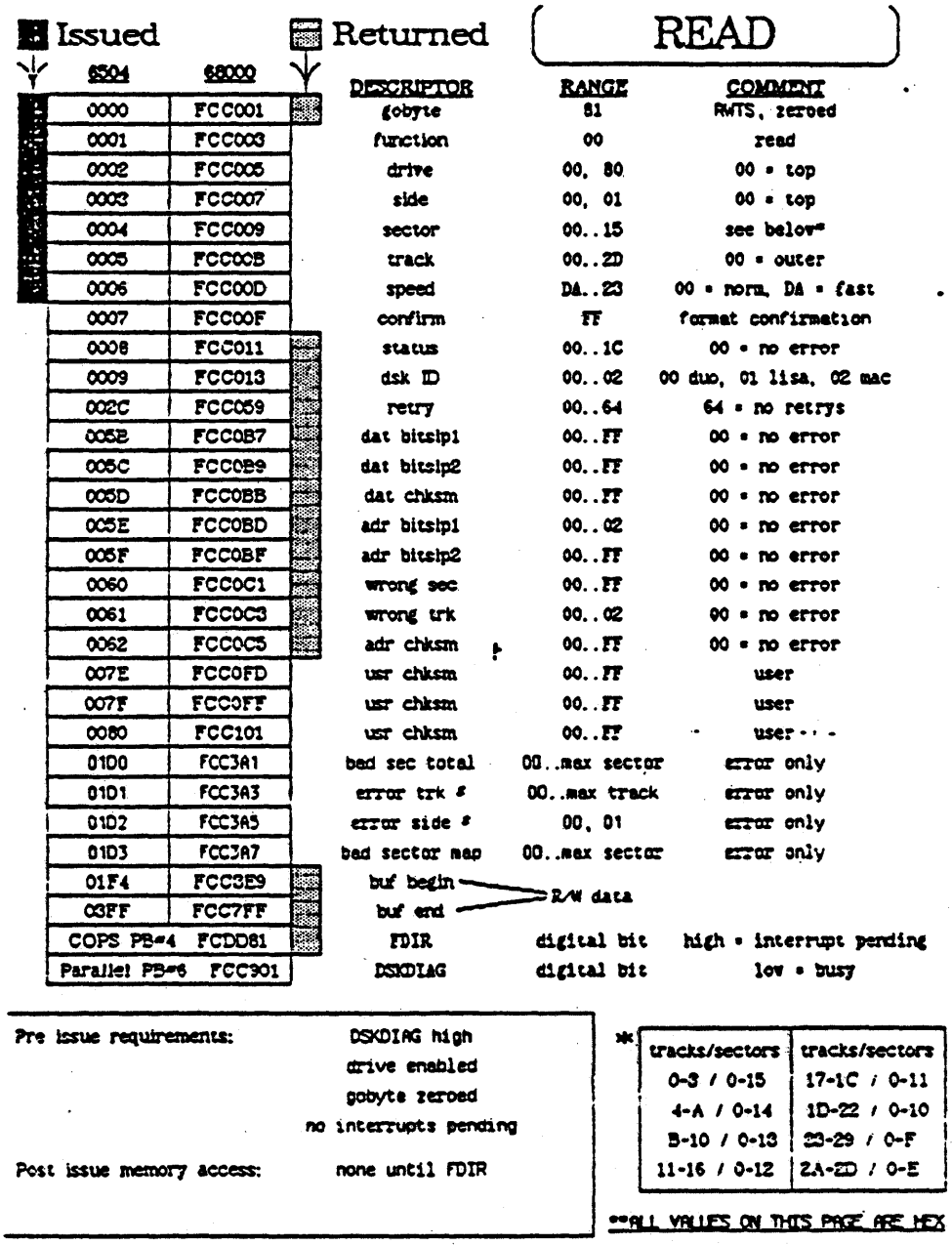


Figure 6-6b. FD Controller Read Command

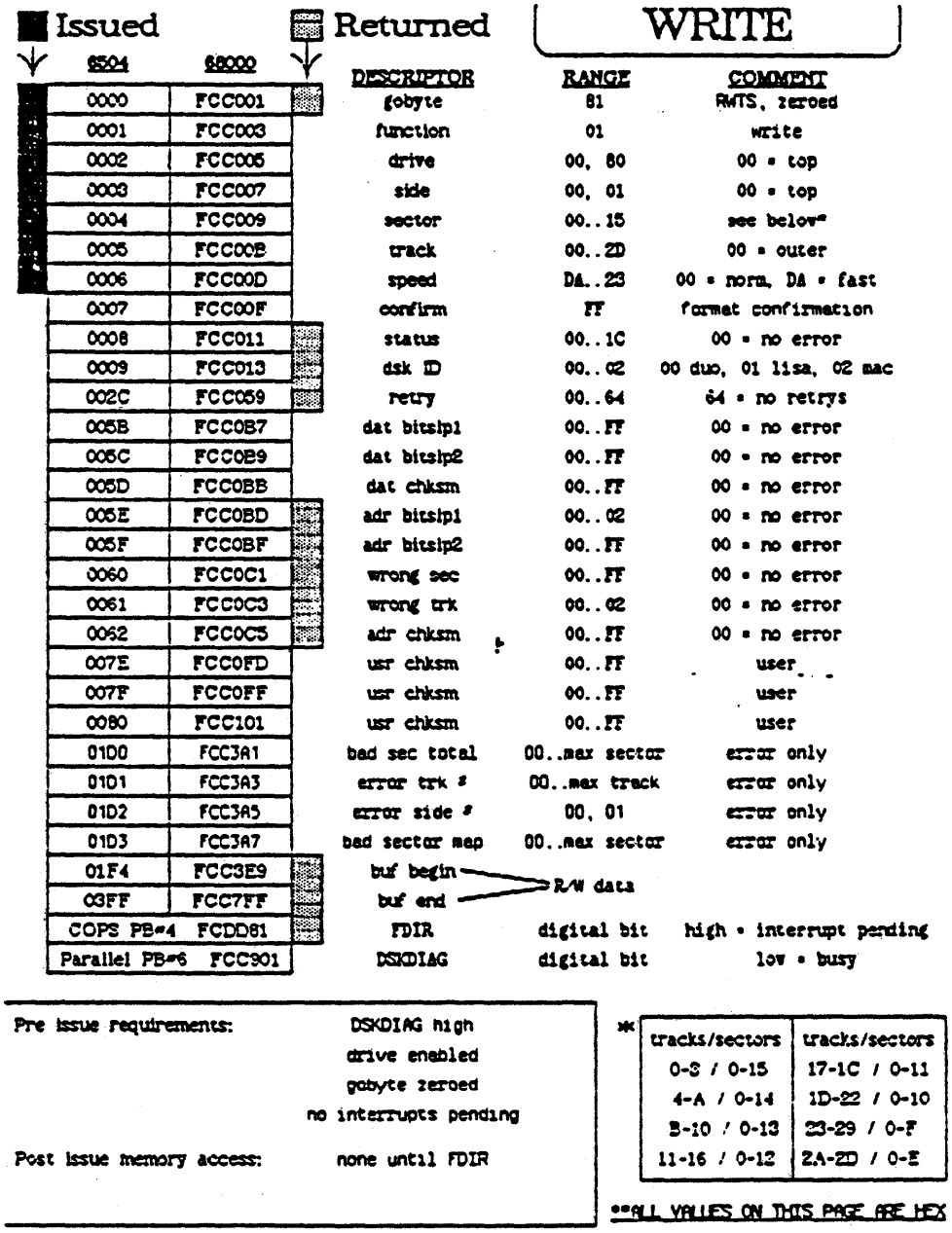


Figure 6-6c. FD Controller Write Command

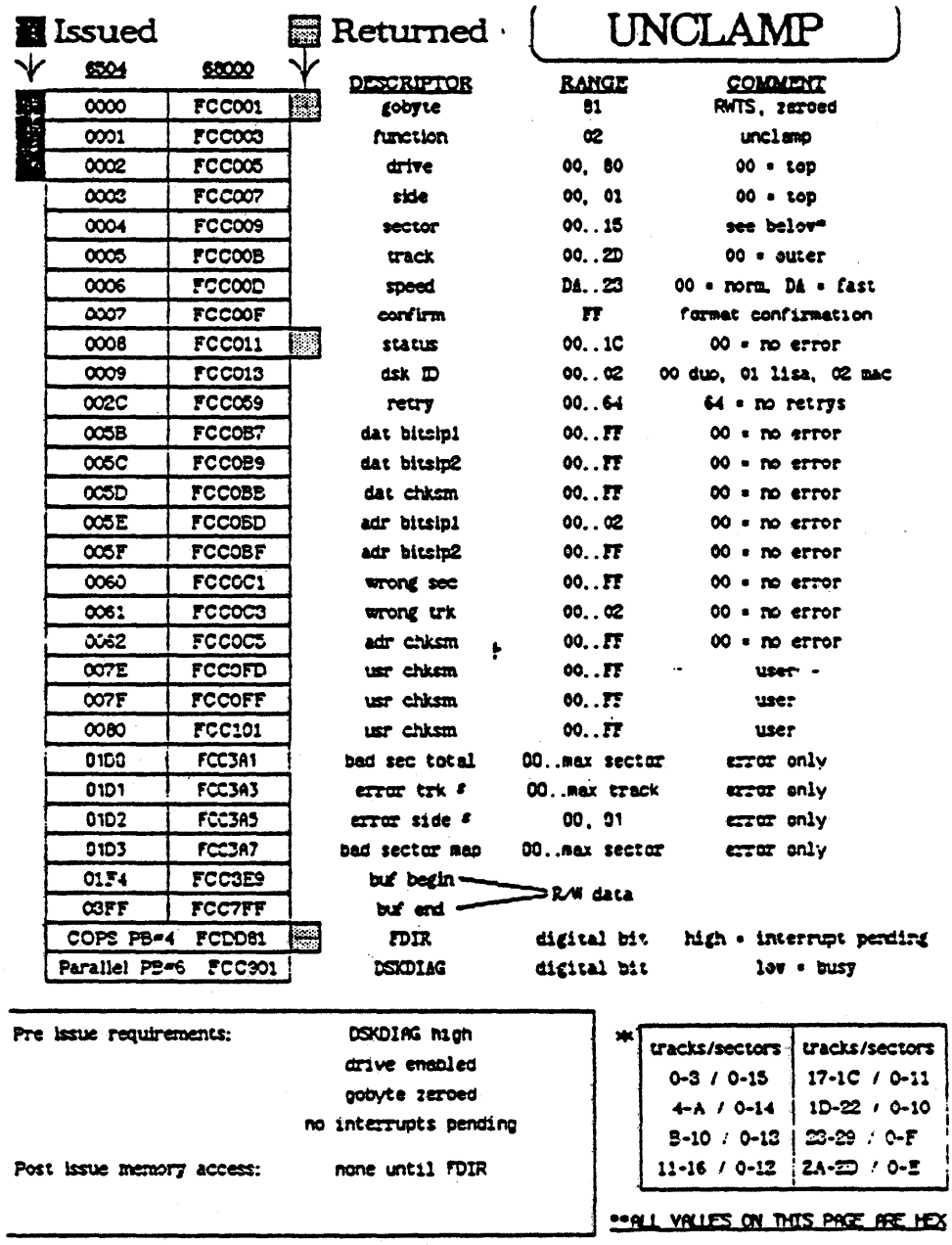


Figure 6-6d. FD Controller Unclamp Command

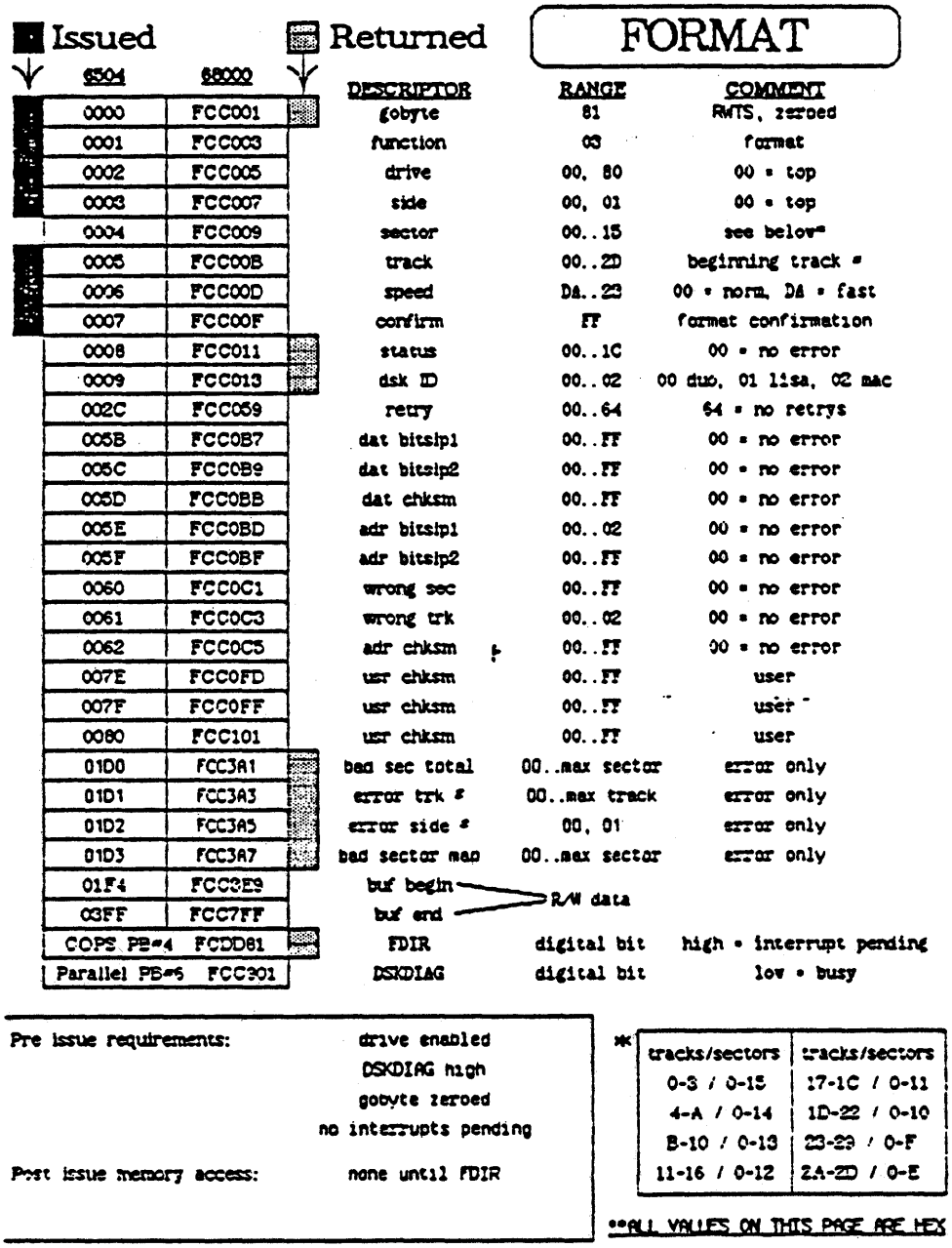


Figure 6-6e. FD Controller Format Command

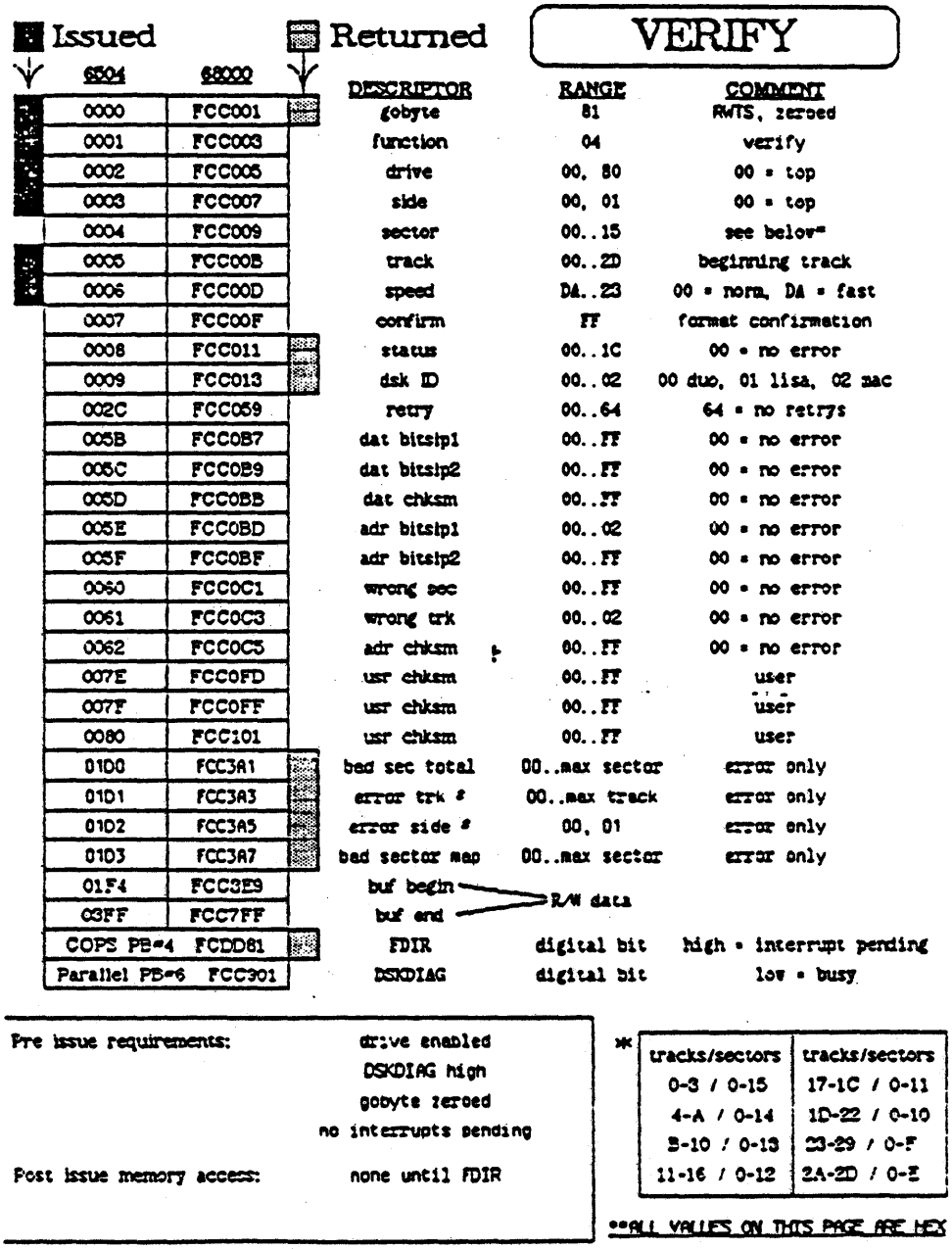


Figure 6-6f. FD Controller Verify Command

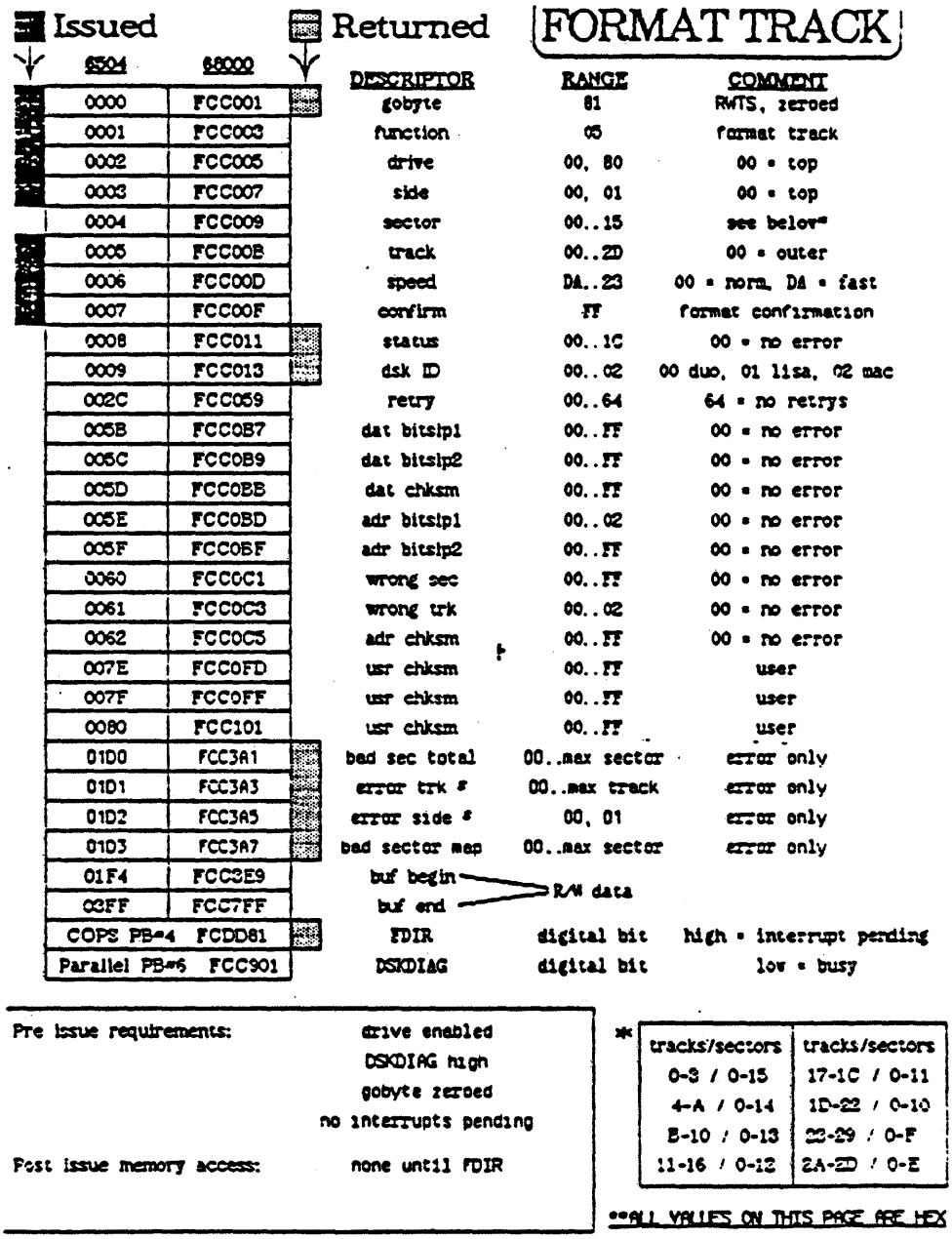


Figure 6-6g. FD Controller Format Track Command

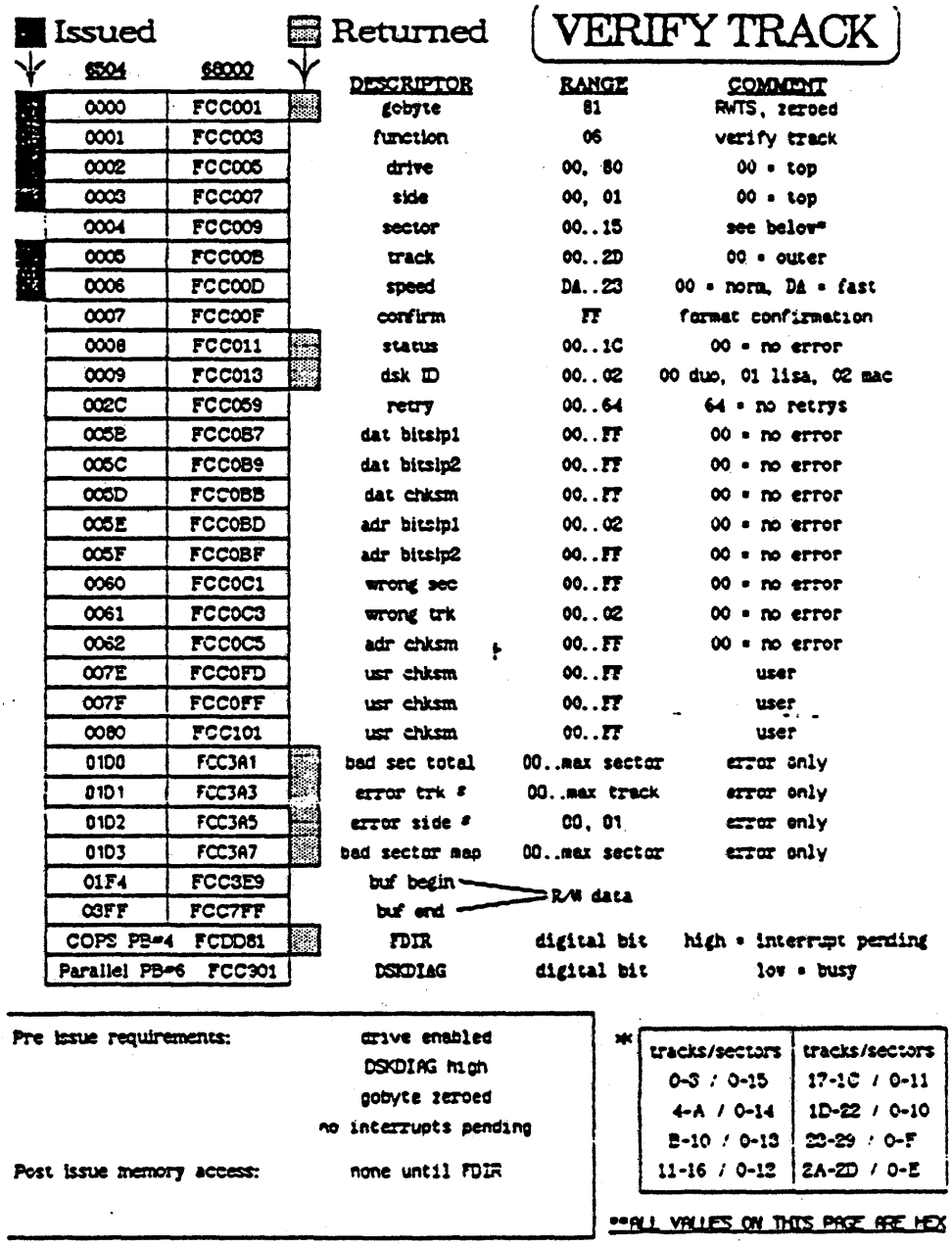


Figure 6-6h. FD Controller Verify Track Command

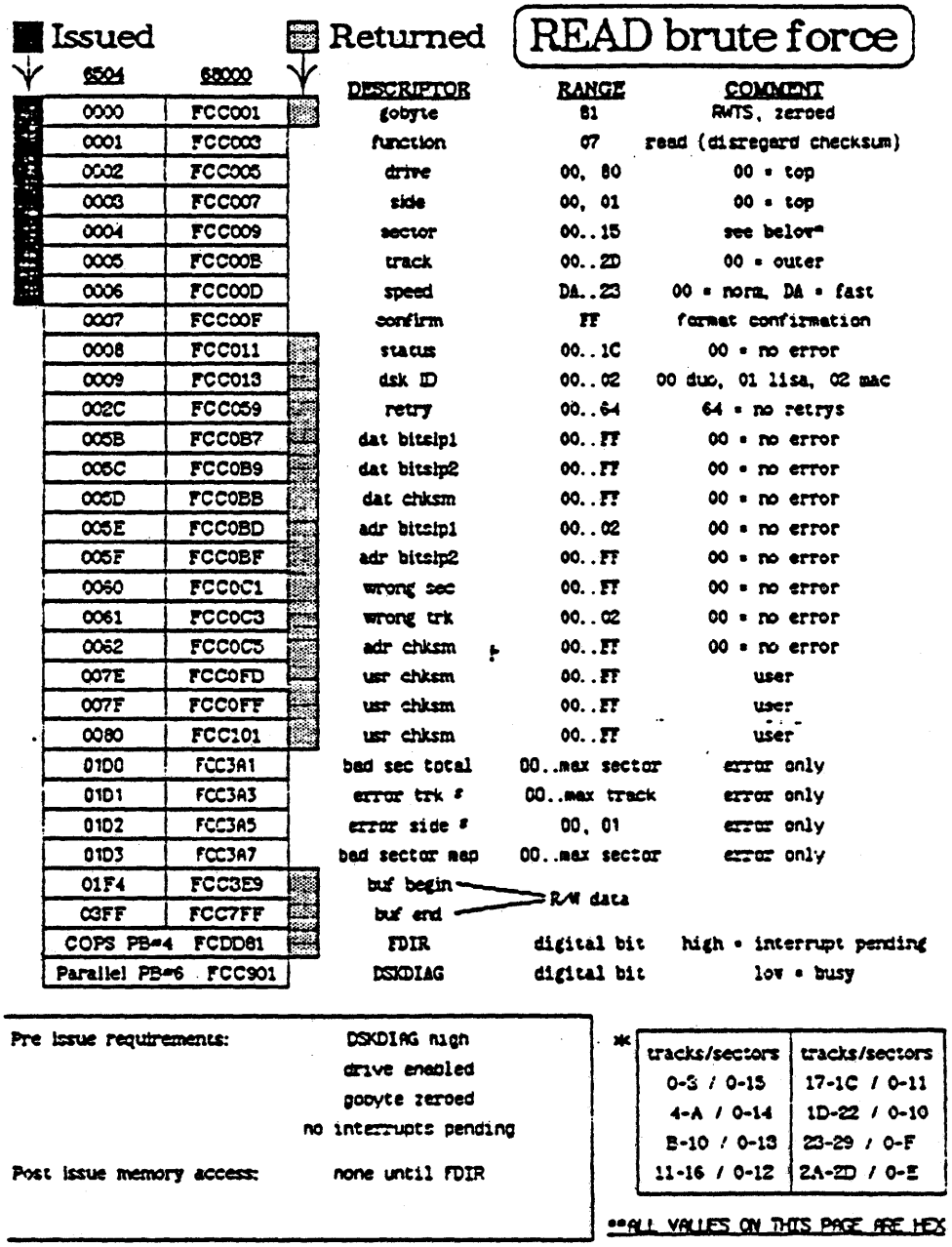


Figure 6-6i. FD Controller Read Brute Force Command

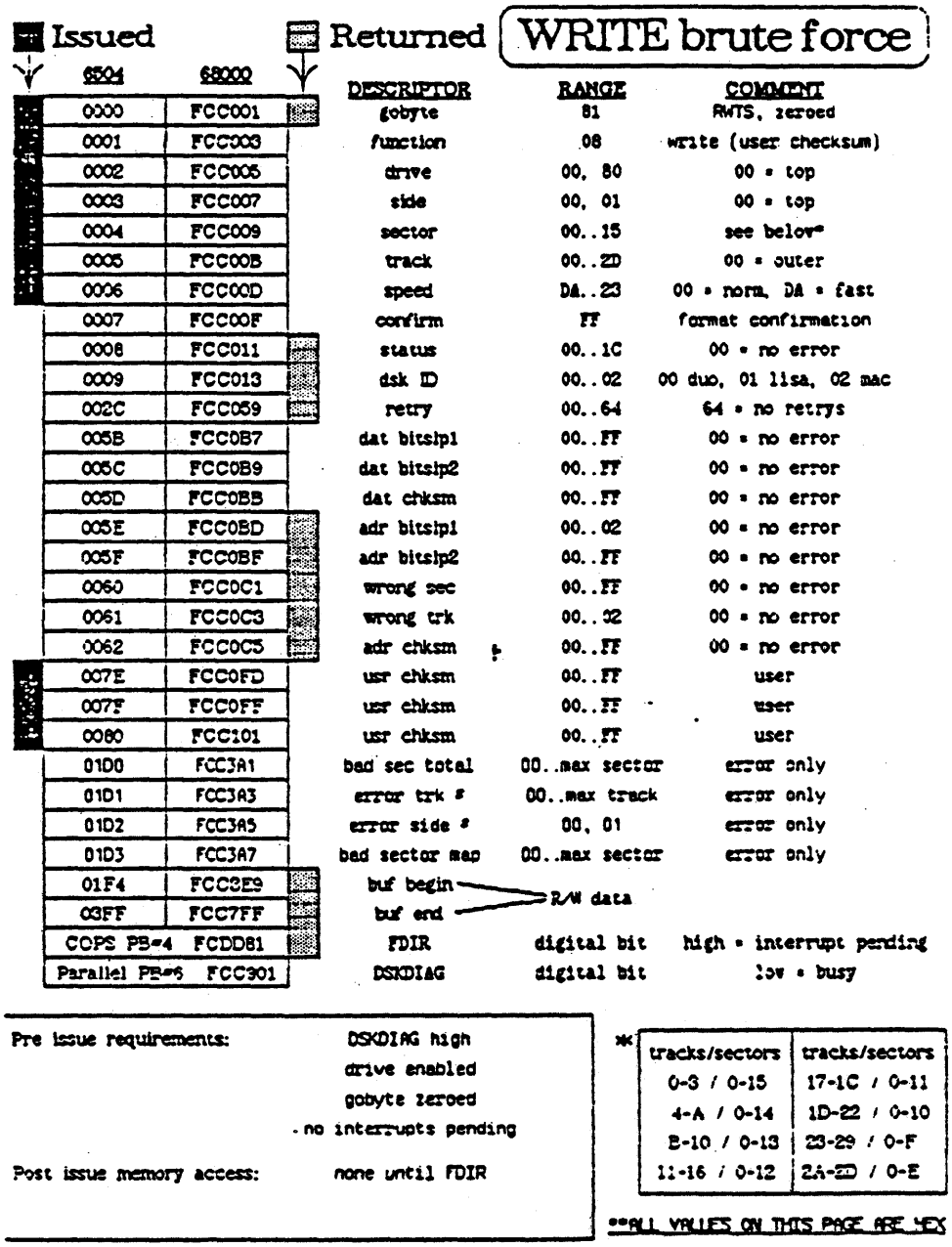


Figure 6-6j. FD Controller Write Brute Force Command

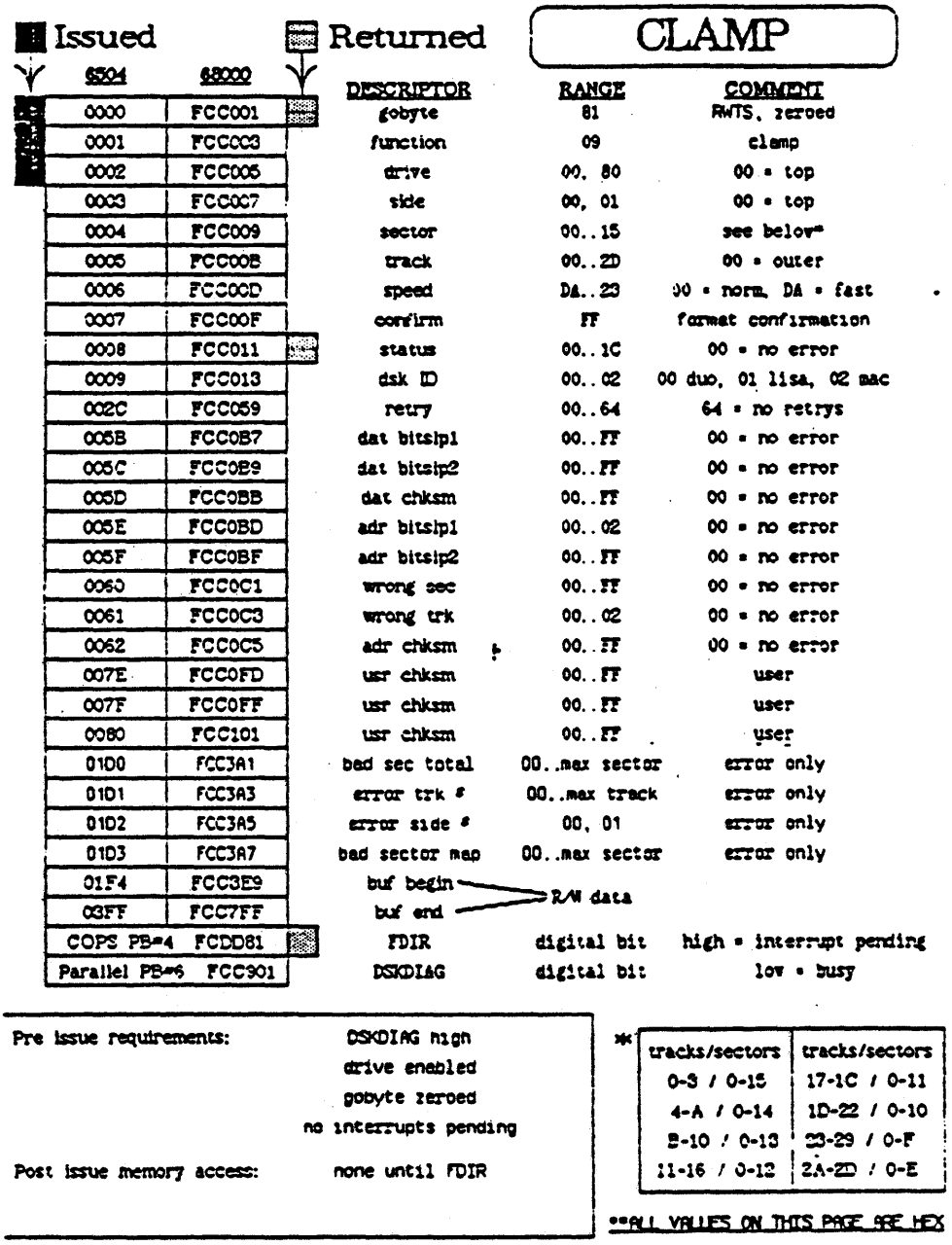


Figure 6-6k. FD Controller Clamp Command

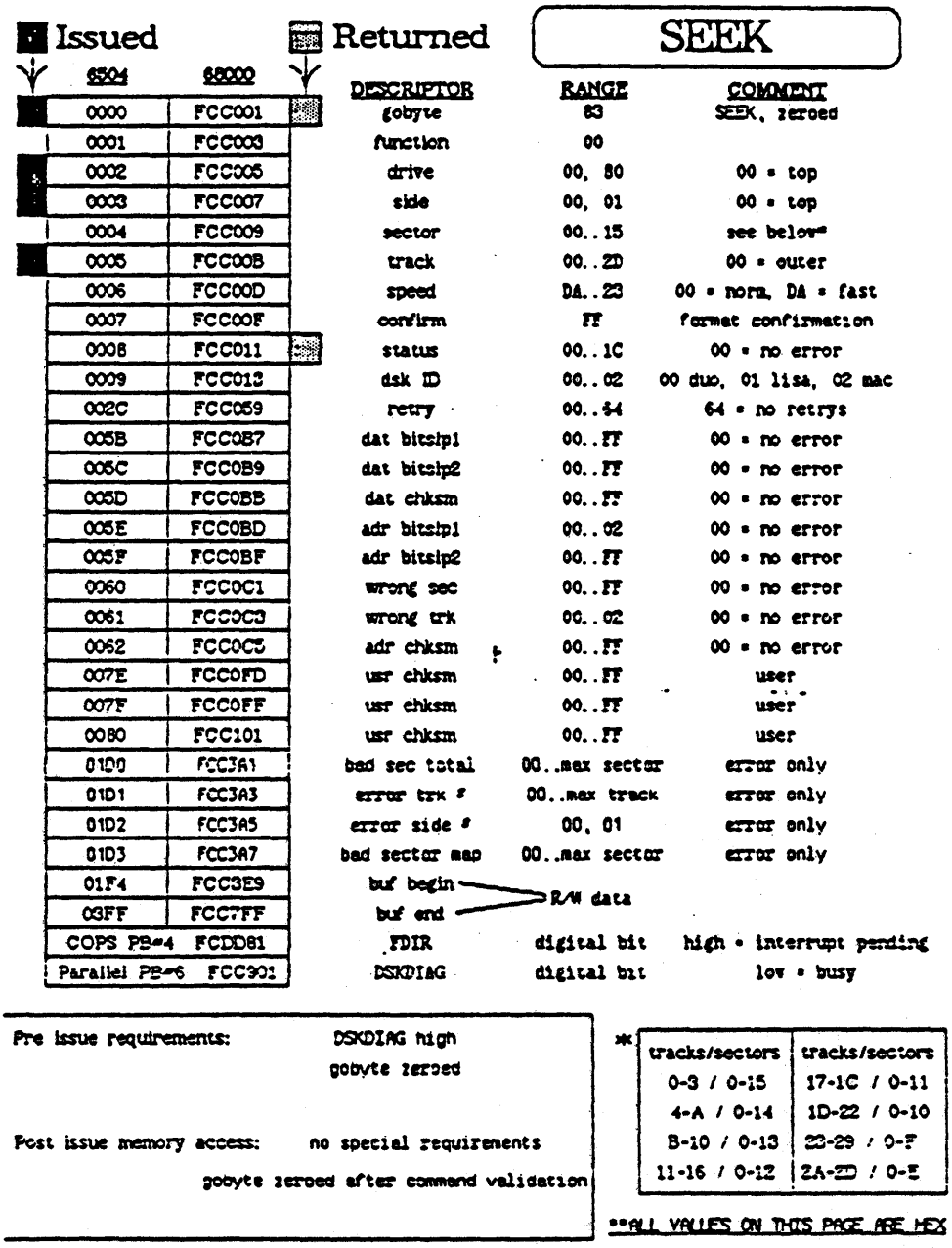


Figure 6-61. FD Controller Seek Command

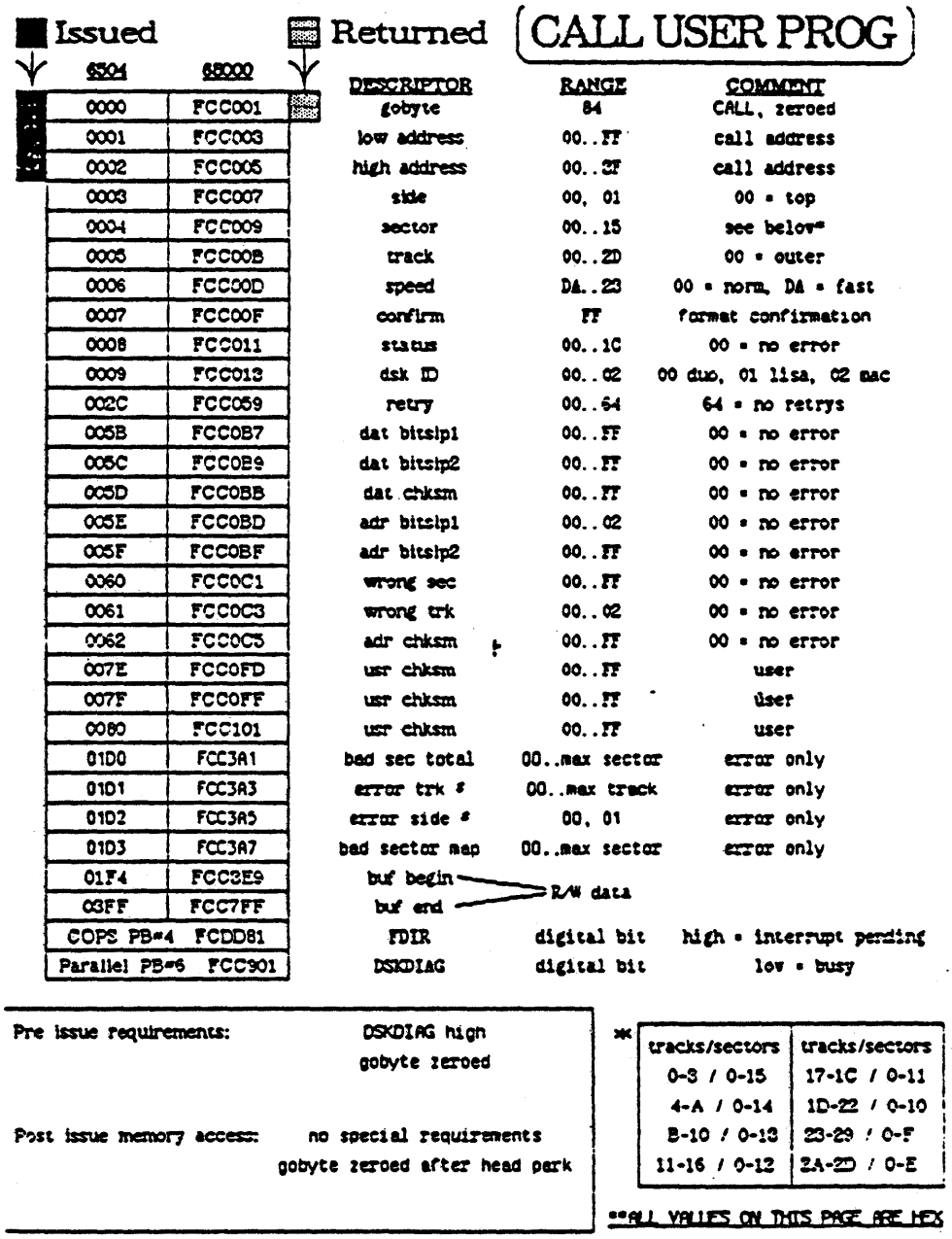


Figure 6-6m. FD Controller Call User Program Command

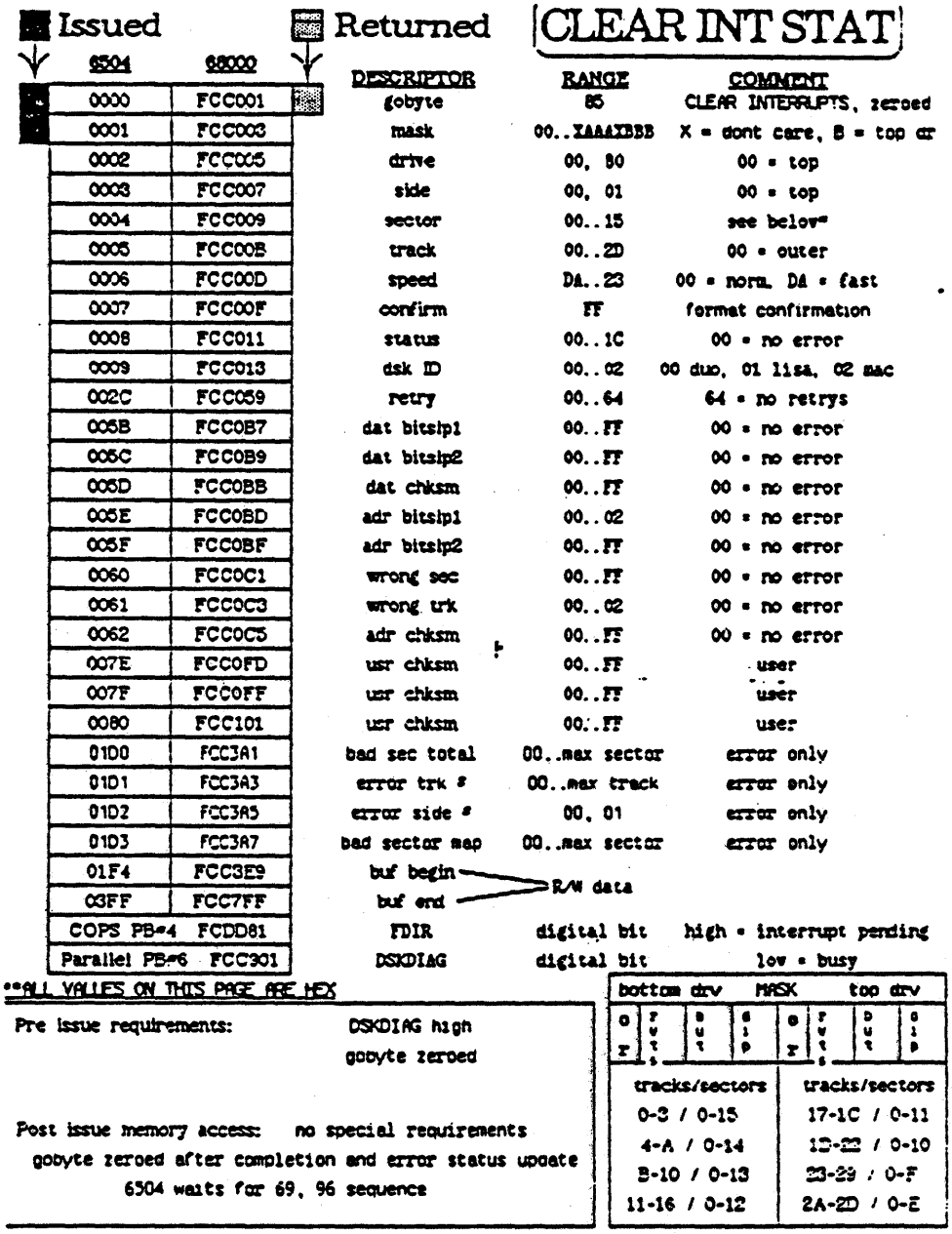


Figure 6-6n FD Controller Clear Interrupt Status Command

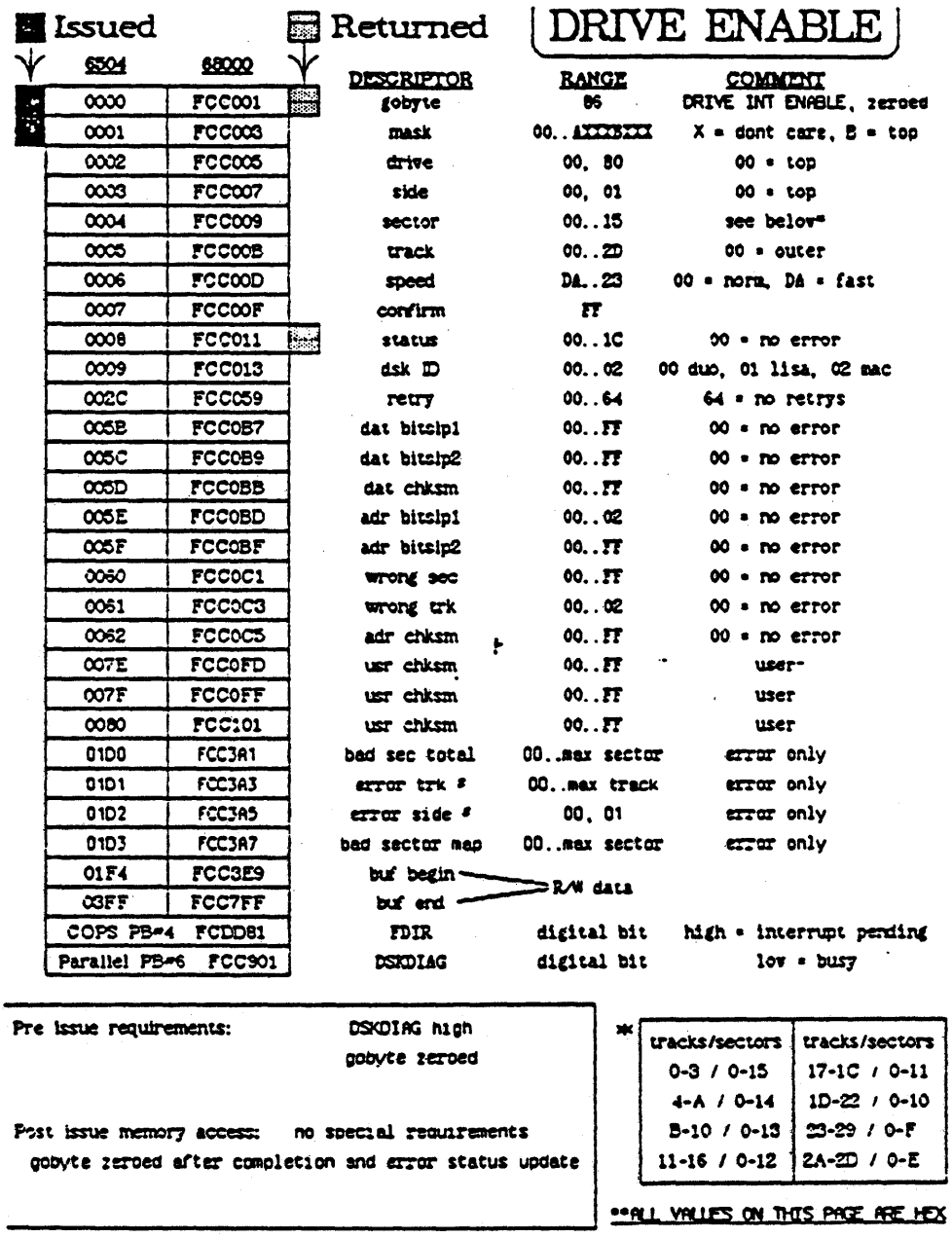


Figure 6-6o. FD Controller Drive Enable Command

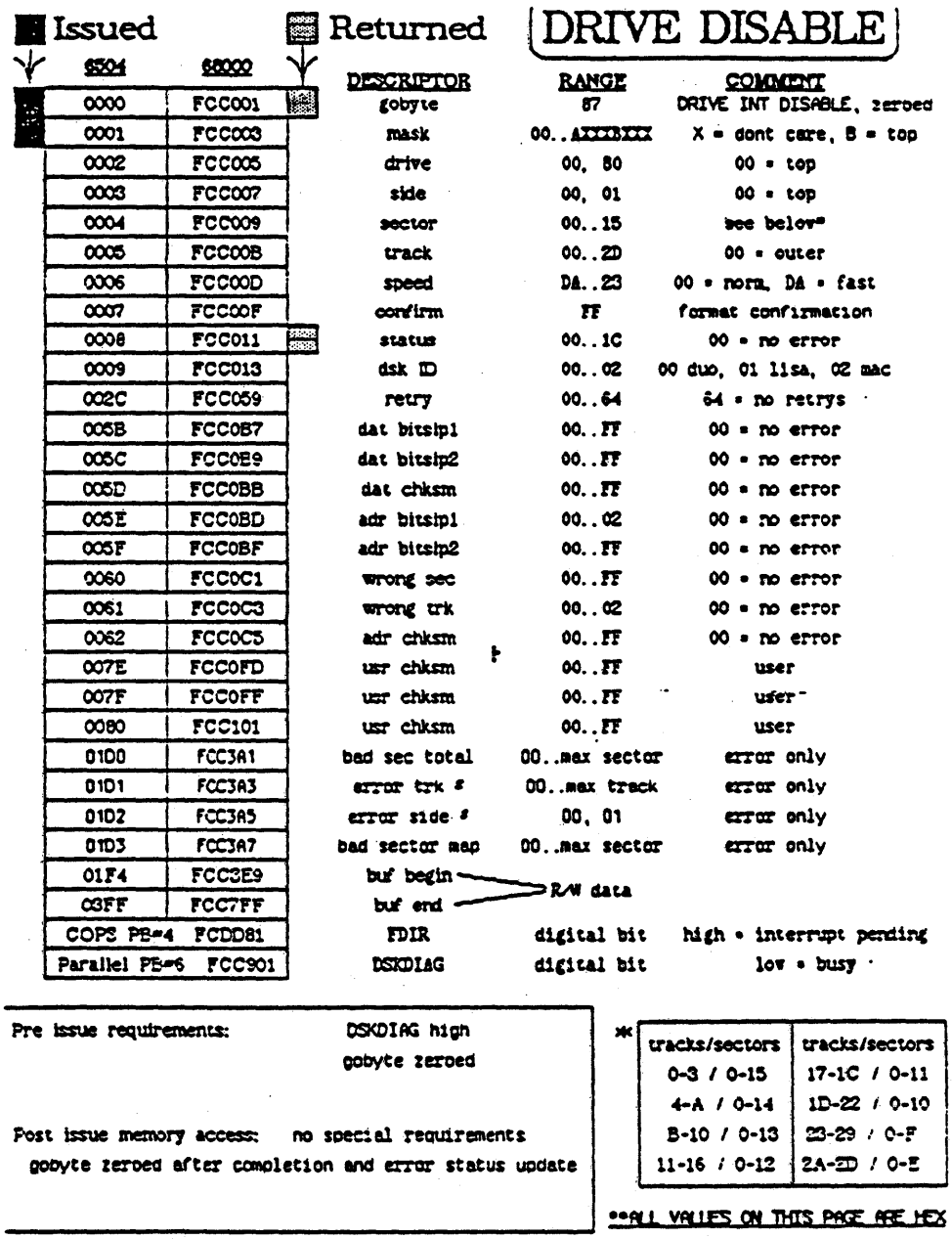


Figure 6-6p. FD Controller Drive Disable Command

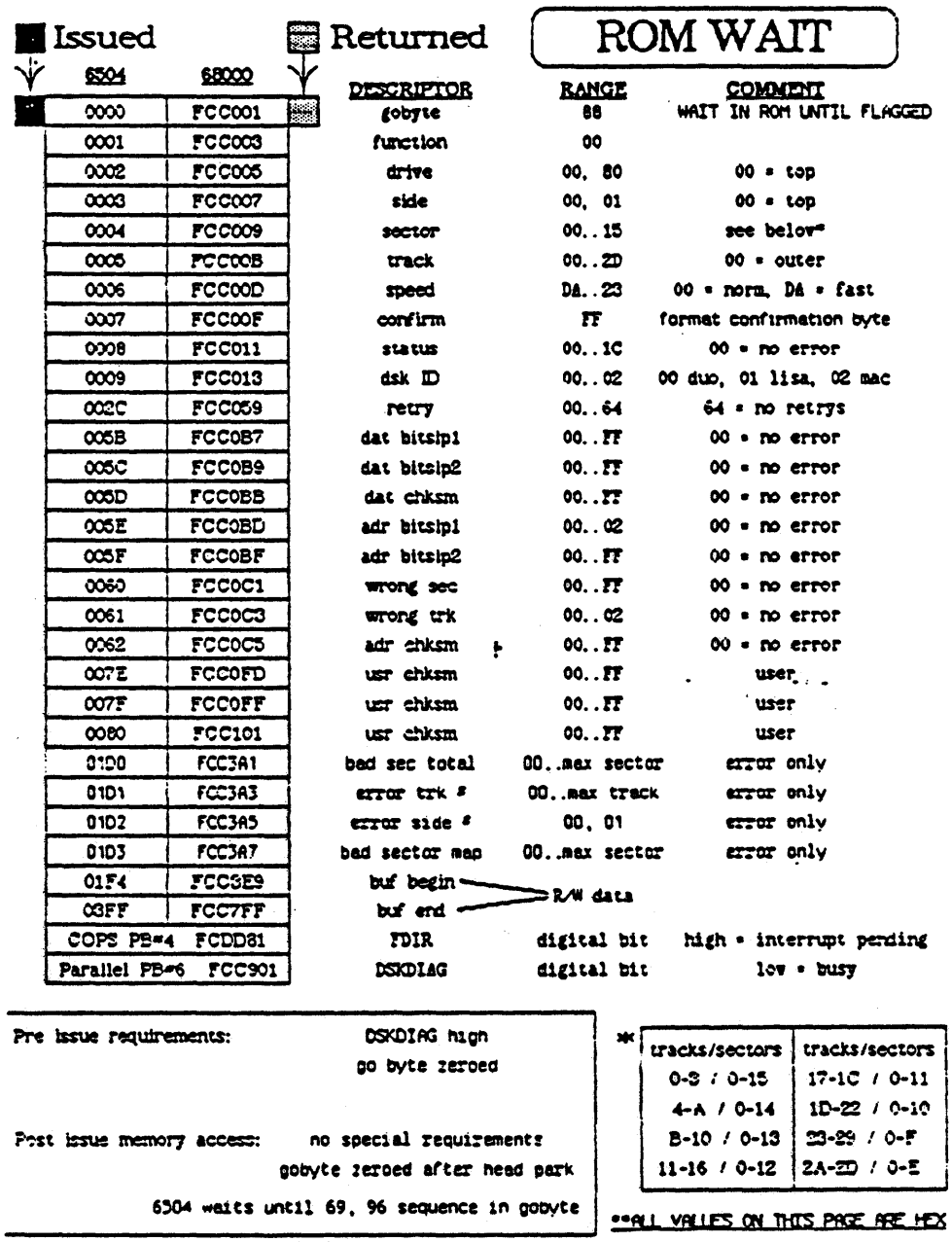


Figure 6-6q. FD Controller ROM Wait Command

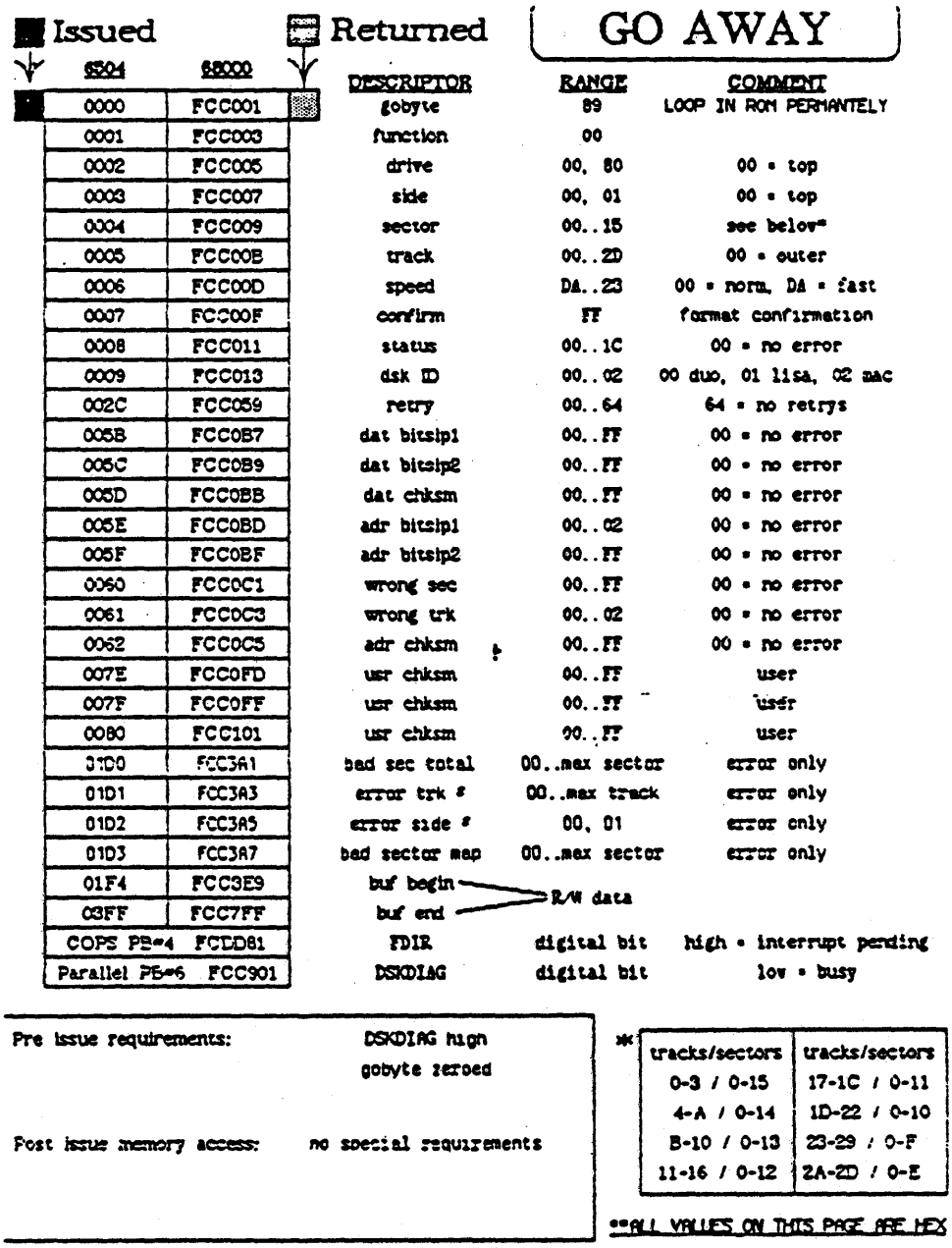


Figure 6-6r. FD Controller Go Away Command

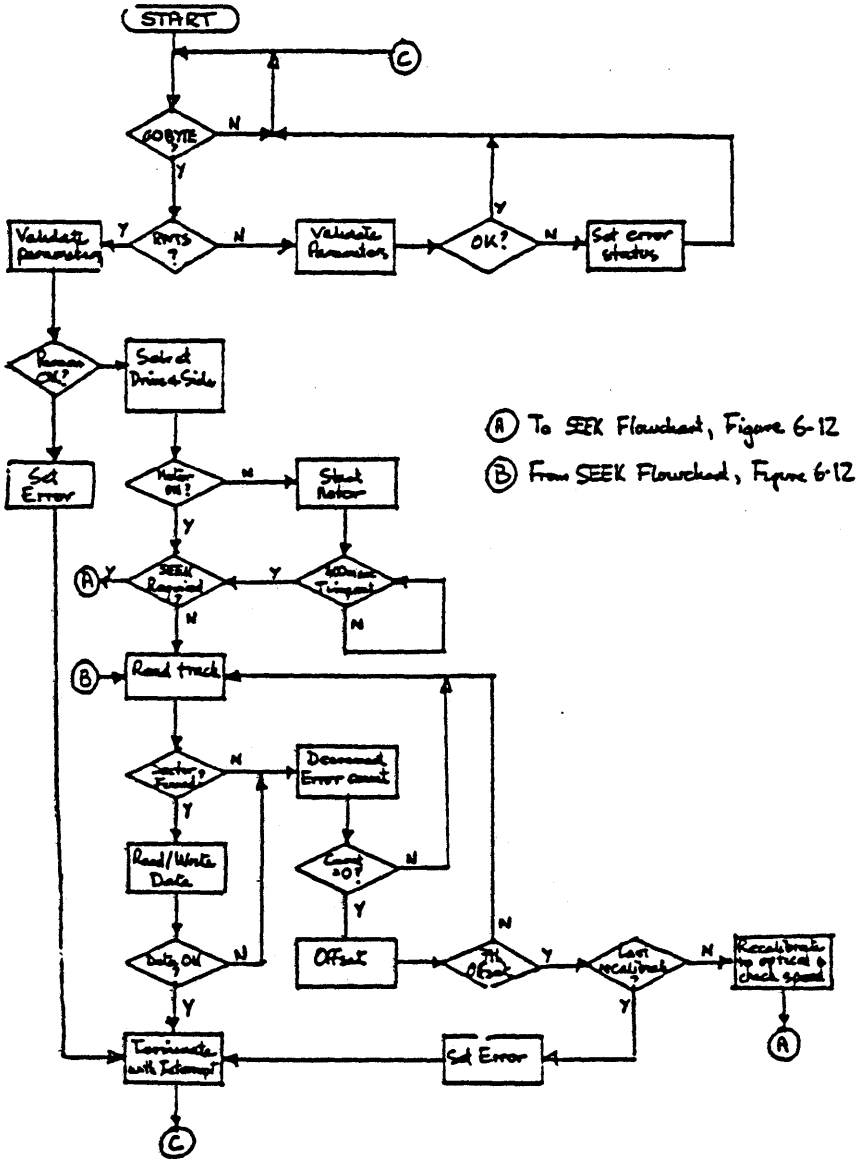


Figure 6-7. FD Macro Command Flowchart

6.3.1 Slave Processor Operation

The 6504 slave processor executes code from the local ROM storage within the FD controller. It is routed to the routines contained therein on the basis of the macro command placed in the I/O control block of the local RAM by the 68000.

The 6504 is also responsible for the encoding and decoding of the data for transfer to and from the FD drive.

The command RAM available to the 6504 is logically divided as shown in Figure 6-8.

(Insert Figure 6-8)

The I/O control block is shown in detail in Figure 6-3. The read/write shared RAM is initialized by the 6504 at power-on time. The status block is used by the 6504 to indicate the result of execution of a macro command. The internal I/O block is used by the 6504 for internal flags indicating progress in execution of an operation. Variables used by the 6504 include both local and variable intermixed. The parameter storage is a space available to the 68000 and is not accessed by the 6504. The 6504 stack fills the space assigned to it from the high-order position downwards. The I/O Buffer is a space of 524 bytes used to transfer data between the floppy disk and the main system.

In order to proceed with disk operations, the 6504 inhibits interruption by the system. This enables the timing routines which are performed by the 6504 to be performed in real time until the operation is complete and termination status is available to be interrogated by the system.

The 6504 firmware always executes in one of three possible states:

* Waiting for a macro command from the 68000
* Checking the status of the drives
* Executing a macro command

6.3.2 Disk Macro Commands

The 6504 detects that the CPU has transmitted a macro command to the FD controller by monitoring the high-order bit of the GOBYTE in the I/O block for a non-zero condition.

Upon detecting this, the first eight bytes of the IOB is copied to the internal I/O block (IIOB). Before any execution, interrupts are checked to see if any are pending. If there are, the Clear Interrupt Status command is allowed to execute.

The macro commands divide into two classes by whether they do or do not interrupt the CPU upon completion. Those that do interrupt are generally those which require extensive processing by the 6504 and the CPU is locked out of shared memory for the duration of instruction execution. Once the class of the command has been determined, the GOBYTE is cleared and the command parameters checked for errors. Any error causes the reason to be placed in the ERRSTAT byte and the command is aborted.

The macro commands which may be received are listed below. The details of the command and its associated parameters are shown in Figure 6-6 above.

READ/WRITE DATA These operations involve an implied seek operation. The I/O command block therefore contains information on the desired drive, side, track and sector. The information returned to the CPU includes the status upon command completion, a pointer to the buffer containing data read and a counter for the number of retries which were required.

UNCLAMP This is used to release the disk currently inserted in the drive so that it may be removed. The input data states which drive (00 or 80) and the CPU is interrupted by means of the FDIR signal.

CLAMP This is used to clamp a disk which has been inserted in a drive for which interrupts are enabled.

FORMAT and FORMAT TRACK These overwrite all data and markers on the given track(s). They provide status information which includes the location of bad sectors which could not be correctly formatted.

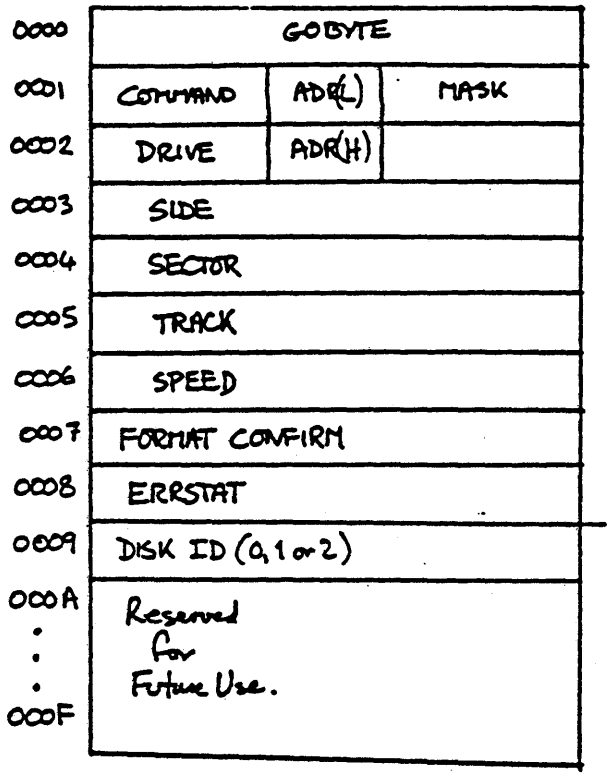


Figure 6-8. FD Controller I/O Block

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CLAMP This is used to clamp a disk which has been inserted in a drive for which interrupts are enabled.

FORMAT and FORMAT TRACK These overwrite all data and markers on the given track(s). They provide status information which includes the location of bad sectors which could not be correctly formatted.

VERIFY and VERIFY TRACK These attempt to read track(s) and inform the system where errors are present in a manner similar to the FORMAT. However, no write operation is performed.

READ BRUTE FORCE (Ignore Checksum) This is identical to a READ operation, except that agreement of the data with the three checksum bytes written at the end of each sector is ignored. It enables partly erroneous data to be read.

WRITE BRUTE FORCE (User Checksum) This is identical to the WRITE operation, except that The command supplies the three checksum bytes to be written at the end of the sector. The controller does not attempt to write the bytes which it would normally generate. Ordinarily, data thus written can only be read without error by a READ DATA (Ignore Checksum) operation.

SEEK This operation moves the selected head to the track required, but does not transfer any data.

CALL USER PROGRAM This initiates a routine which has been down-loaded to the 6504 RAM area.

CLEAR INTERRUPT STATUS This operation clears the interrupt status to the data output with the execution of this command.

DRIVE ENABLE/DISABLE These commands are used to control the availabliity of either of the two disk drives to the system.

ROM WAIT This continually reads RAM, looking for a two-byte sequence of 69 and 96. Once these are found, the system performs a cold start. The purpose of this operation is primarily to remove the 6504 from the RAM area while diagnostics are being performed.

GO AWAY This is used only in an emergency, such as occurs with a power loss during an operation. It causes the FD controller to terminate whatever operation is in progress.

These operations will result in a number of possible status codes being returned to the system via the status byte, which indicates an error when it is non-zero. In addition, error counters give the number of occurrences of specific errors during the performance of a given operation.

The FD controller will attempt to retry an operation on the disk which results in an error condition. This will be attempted repeatedly until the error count is exceeded. Retries involve moving the head off track in increments of 1/8th of a track and recalibrating the head using the optical sensor on the drive.

The significance of the possible error codes and the error counters is shown in Figure 6-9.

(Insert Figure 6-9)

6.3.3 Data Encoding/Decoding

Data transferred to the FD controller by the system for storage on the drives is not written directly onto the disk. A transformation is performed to enable the maximum storage density of data on the disk.

Data is written on the disk according to the following rules:

* Three 8-bit bytes become four 6-bit bytes.
* Each byte on the disk begins with a one bit.
* No more than two zeroes occur consecutively.

The data is transformed under control of the 6504 after it has been placed in the buffer by the system. It is transformed as shown by Figure 6-10.

(Insert Figure 6-10)

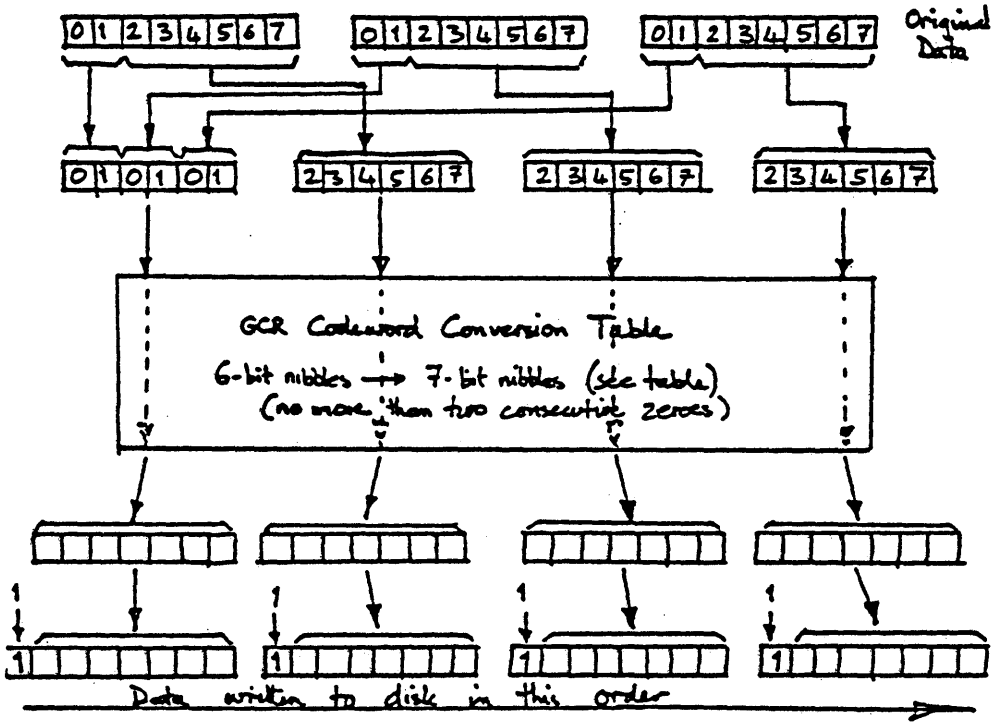
The requirement of each leading bit being a one is in order that the drive state machine can identify byte boundaries when the data is being read from disk. The requirement that no more than two zeroes occur consecutively permits data to be written without intervening clock bits. Transistions from the data bits themselves occur frequently enough to permit the state machine to remain synchronized with the data being read.

The data is reformed from groups of three 8-bit bytes into four 6-bit bytes by a table lookup operation. It so happens that within the 128 possible codings of the other seven bits written to the disk within one byte, there are more than 64 codings that satisfy the requirement of no more than two consecutive zeroes.

ERROR CODES	SIGNIFICANCE
01 (hex)	Invalid Command
02	Invalid Drive
03	Invalid Sector
04	Invalid Side
05	Invalid Track
06	Invalid Clear Mask
07	No Disk
08	Drive Not Enabled
09	Interrupts Pending
0A	Invalid Format Confirmation
0B	ROM Selftest Failure
0C	Unexpected IRQ or NMI
14	Write Protect Error
15	Unable to Verify
16	Unable to Clamp
17	Unable to Read
18	Unable to Write
19	Unable to Unclamp
1A	Unable to Find Calibration
1B	Unable to Adjust Speed
1C	Unable to Write Calibration

ERROR COUNTER ADDRESS	SIGNIFICANCE
005B (hex)	Bitslip Error Count (data field start header)
005C	Bitslip Error Count (data field trailer)
005D	Checksum Error Count
005E	Bitslip Error Count (ID field start header)
005F	Bitslip Error Count (ID field trailer)
0060	Wrong Sector
0061	Wrong Track
0062	Header Checksum Error

Figure 6-9. FD Controller Error Codes



GCR Codeword Table

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	96	97	9A	9B	9D	9E	9F	A6	A7	AB	AC	AD	AE	AF	B2	B3
10	B4	B5	B6	B7	B9	BA	BB	BC	BD	BE	BF	CB	CD	CE	CF	D3
20	D6	D7	D9	DA	DB	DC	DD	DE	DF	E5	E6	E7	E9	EA	EB	EC
30	ED	EE	EF	F2	F3	F4	F5	F6	F7	F9	FA	FB	FC	FD	FE	FF

Figure 6-10. FD Data Encoding Scheme

6.3.4 Disk Formatting

The format of tracks in the LISA is similar to that used in the Apple II and Apple III systems, with the addition of a side number. Data encoding has been changed, as described in the preceding subsection.

A number of codings which are not used in data translation are used to indicate a number of special codes, such as headers within the format and speed synchronization bytes.

The number of sectors and tracks are shown in Figure 6-11. Note that the number of sectors is dependent on the track. This is due to the technique of varying the rotational speed of the drive to allow for the increased density possible on the outer tracks of a disk.

(Insert Figure 6-11)

Tracks 0 through 45 are normal data tracks. The number of sectors contained on each track depends on the track position as shown. This is due to differing lengths of each track. The speed of disk rotation is dynamically changed by the FD controller to take advantage of this.

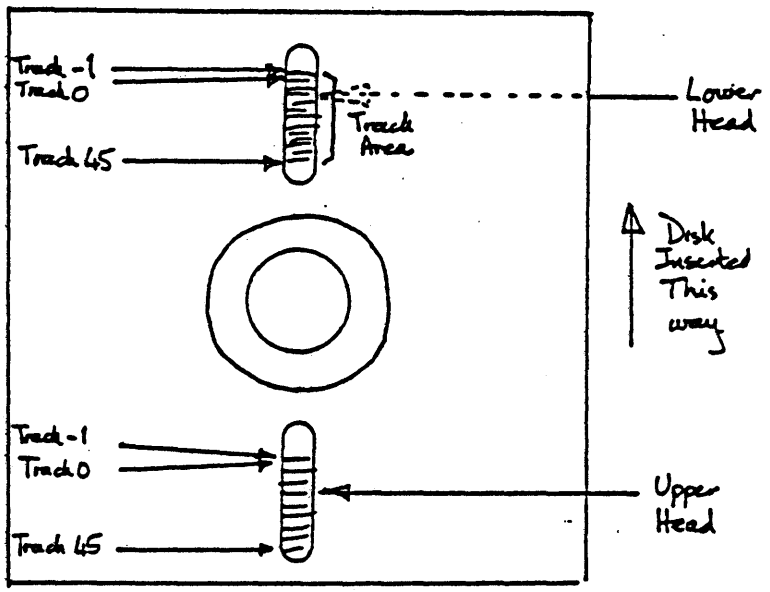
Track -1 is used as a speed synchronization track. It is never written to except during disk formatting. The 6504 makes use of this track to adjust the speed of rotation to within 0.4% of the desired speed.

Each sector is divided into four distinct fields, as described below:

* Header sync field
* Header field
* Data sync field
* Data field

HEADER SYNC FIELD This contains a pattern of ones and zeroes that permit the disk state machine to synchronize with the data coming from disk. It consists of the following pattern:

32 "Bit slip" FF's
10 bytes A9 Speed Synchronization
(only before Sector #0)



Tracks	Sectors	r.p.m.	Speed Code
0-3	22	218.3	DC (hex)
4-10	21	228.7	CC
11-16	20	240.1	B8
17-22	19	252.7	A4
23-28	18	266.8	8E
29-34	17	282.5	75
35-41	16	300.1	59
42-45	15	320.1	38

Figure 6-11. LISA Disk Format

HEADER FIELD This identifies the sector uniquely on the disk, using the following pattern:

D5)	
AA)	Header field identification
96)	
1 byte	TRACK identification number
1 byte	SECTOR identification number
1 byte	SIDE identification. 00 or 01
1byte	VOLUME identification.May beone of 00=AppleII/III, 01=LISA, 02=Mac
1 byte	CHECKSUM coding. This is formed by XOR'ing the previous four bytes
DE)	
AA)	"Bit slip" marks
1 byte	Pad byte where head was turned off

DATA SYNC FIELD This is similar in purpose to the header sync field. It has the pattern:

5 "Bit slip" FF's

DATA FIELD This field contains the data written to the drive. Normally this is the only field written to except during a format operation. It has the pattern:

D5)	
AA)	Data marks which identify a data field
AD)	
1 byte	Sector number
524 bytes	User data
3 bytes	Checksum formed by adding data
DE)	
AA)	"Bit slip" marks
1 byte	Pad byte where head is turned off

Note that the format is given in terms of the bytes handled by the system side of the controller. The actual number of bytes written to the disk is greater since three normal bytes map into four bytes on the disk, as given by Figure 6-10.

Bit slip refers to a technique whereby two zeroes are inserted between each byte written to the disk. The state machine requires no more than six bit slip bytes to synchronize its read operation with disk rotation.

6.3.5 Disk State Machine Operation

The state machine which controls the flow of data across the drive interface is shown in Figure 6-5 above.

Data is written onto the disk in the LISA system using a group-encoding technique. Data bytes are transformed by a mapping function from the 8-bit bytes presented by the controller into 6-bit bytes. These 6-bit bytes are in turn transformed into an 8-bit code in which the MSB is always a one and no bit sequence contains more than two consecutive zeroes. This is shown schematically in Figure 6-10 above.

The 6504A slave processor performs all encoding and decoding of nibbles.

The disk state machine is programmed to perform a limited number of operations, depending on the state of the inputs presented to it.

There are five external inputs to the state machine. These include the RDA, WRD and SNS lines from the disk and the A2 and A3 control lines from the control outputs of the LS259 shown at C-2 on sheet 4. The latter two are used to control the command which the state machine is currently operating. The four possible commands are:

* Sense
* Read
* Write
* Write Load

In addition, there are two signals which are input to the state machine ROM. These are the Qa output of the shift register, which provides the data stream to be written to the disk and the output of the edge detector at D-1 which presents the data transitions to the ROM as ones.

SPINDLE MOTOR SPEED CONTROL

This is performed when a disk is inserted to bring the spindle up to speed. During normal operation, the disk drive controls the rotation by means of an integral speed control circuit. When the drive performs a seek operation outside of the current range of tracks, the speed is adjusted according to the values given in Figure 6-11.

Disk speed is maintained within 0.4% of that desired.

DRIVE REZERO and SEEK

These are performed in a similar manner in that they both involve carriage motion. The four lines Phi0-Phi3 are manipulated to cause the carriage motor to step the required amount of tracks. In the case of a rezero, a sense operation determines whether the optical recalibration line is asserted to indicate that the carriage is at the known position of track -1.

Carriage movement is defined by the order in which the Phi lines are manipulated. Thus a step through phi 3,2,1 and 0 moves the heads toward the calibration point (towards the front of the LISA) by one half track. Stepping through 0, 1, 2, and 3 moves the heads away from the calibration point by one half track.

In order to minimize the positioning error from mechanical tolerances, seeks are always completed by moving the carriage in the same direction (towards the calibration point) for the last half track (four increments). This means that seek direction is reversed during a seek away from the calibration point.

Carriage movement is performed in increments of 1/8th of a track. Allowance is made for head inertia by having three distinct time durations of each-phi state before proceeding to the next. An example of a seek is shown in Figure 6-12.

(Insert Figure 6-12)

WRITE and WRITE LOAD

These commands operate together to provide the write function to the drive. Each command consists of 16 states in the Phase-Lock-Loop state machine. Each state is passed through in one clock cycle of 250 nanoseconds.

Since the bit time on the disk is 2 microseconds, the 16 states correspond to two bit times. The timing of the program loops in the 6504A is such that exactly eight bit times occur between each time that data is written to the shift register. This write operation also causes the upper control decoder to alter the A2 and A3 input configuration to the ROM at D-2, which alters the state machine into the Write Load command.

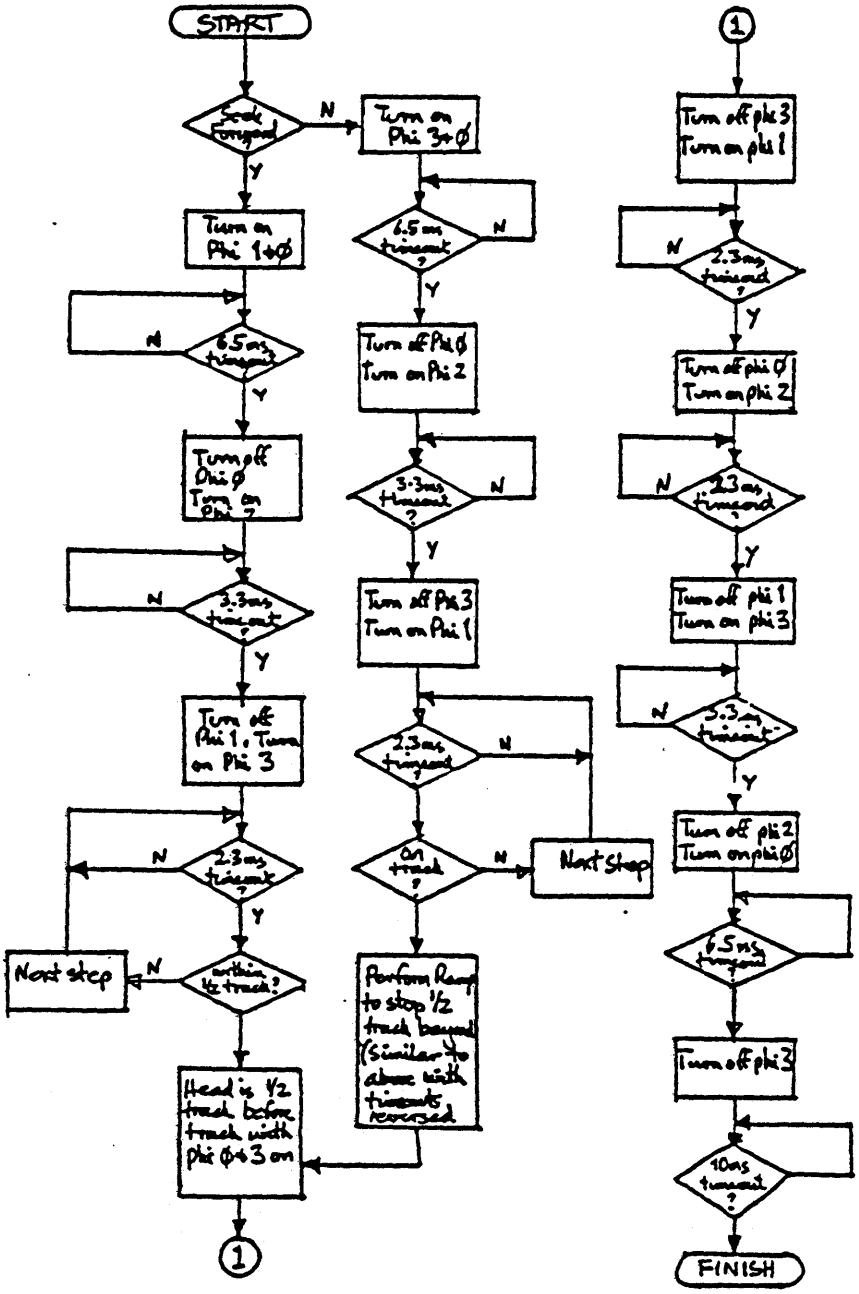


Figure 6-12. Seek Flowchart

The state transitions in both the Write and Write Load programs are designed so that that the WRD signal is connected to the high-order state bit. The QA output of the shift register thus controls the data that is written to the disk.

READ

All inputs to the state machine are used for a read operation. The read data is passed through two flops in series to detect transitions. The format of the LISA disks is such that no more than two zeroes may occur sequentially. The read command shifts a one into the shift register when a transition occurs and shifts in a zero when 2 microseconds pass without a transition.

It also attempts to hold the data in the shift register for as long as possible when QA goes high to indicate that an entire byte is correctly aligned in the shift register. Following this, the byte is transferred to RAM and cleared in preparation for the next byte. Recall that all bytes written to disk had a one in the MSB position after data had been encoded.

SENSE

This is used to poll the status within the disk drives. The HDS and Phi0 lines are used to select which of the four data bits are to be read according to the following scheme:

HDS	Phi0	Status Data
0	0	Write Protect
0	1	Optical Recalibration
1	0	Eject Button
1	1	Disk in Place

After the control lines have been configured to sense the required data, the command is initiated by setting the A@ and A3 inputs to 01. The MSB of the shift register will contain the sense bit. All 16 possible states in the sense command are identical and cause a shift right operation. Since the D and QA inputs are irrelevant to this operation, all 64 bytes of the ROM associated with this command contain the code 0A.

6.4 The Serial I/O Controller

The I/O Board contains two RS232A serial interface ports which are under control of a single serial I/O controller. The software interface to this controller is discussed in Chapter 2.

The A-port conforms to the RS232A specification, while the B-port conforms to RS422, of which RS232A is a subset.

The control logic is shown on the right side of sheet 3 of schematic 050-4008. Refer to the block diagram of the board in Figure 6-1 for a view of the hardware context in which the serial controller operates.

Programming of the ports is discussed in Subsection 3.5.1.

6.4.1 The Controller Device

The serial ports are under the control of an 8530 dual serial port controller. A discussion of this device can be found in the device user manual.

The device connects to the internal I/O Board D bus. The device is always selected when a VMA signal coincides with an AS. This appears to mean that any time that system performs a cycle to any 6800-type peripheral, the 8530 will consider itself selected. However, the actual select is performed on the read and write inputs, which are derived from the port decoding logic at B-3 on sheet 1.

The WSIO/ signal enables a write to the device, while a RSIO/ enables a read from it. These signals originate in the device decode logic at A-3 on sheet 2. A configuration of address lines A11-A9 of 001 will select the Serial Port controller. The READ line distinguishes a read from a write.

The low-order two address bits of the system address bus A2 and A1 are used to select between the two ports and to define whether control information or data is being transferred.

The PCLK device clock is derived from the 4M (4 Megaherz) clock signal at A-3 on sheet 2. This is in turn derived from the 16 MHz clock from the FD controller.

The device interrupts the system through the RSIR/ signal on the system bus. Selection of registers and functions within the device is made by means of the D/C/ and A/B/ pins. The first indicates whether data or command

information is present on the bus lines. The second selects between the A and B ports. Address lines A1 and A2 enable system software to control this.

6.4.2 The Serial Ports

The two serial ports are provided in the form of two RS-232A 25-pin D-type connectors, as described in Subsection 3.5.1.

The logic interface is shown on sheet 3 of the schematics at A-1 through D-1. Standard bus driver devices are used to convert the signals to and from TTL.

The signals which correspond to port A are in the upper section of the page and have signal names ending in "1". The signal names and their function correspond to standard RS232A nomenclature. The 1488 and 1489 devices convert the TTL signals from the controller into the +/-12V levels of the interface and vice-versa.

Port B signals are in the lower part of the page. They provide an RS422-standard interface through use of the 26LS30 and 26LS32 devices.

6.4.3 Baud Rate Generation

Selection of the baud rate used in either of the two ports is performed internally by the 8530 device with the aid of the 3.68MHz oscillator between the SYNB and TRXCB lines.

Refer to the device user manual for details on how baud rates are selected.

6.4.4 Serial Port Operation

The two serial ports operate independently of one another. For details, refer to the device user manual.

6.5 Parallel Port Controller

The parallel port is used to interface a high-speed peripheral to the LISA system. A typical application is in the attachment of an Apple hard disk drive, which can offer significant improvement in on-line storage capacity and data access speed over floppy disk drives.

The interface is discussed operationally in Chapter 2 of this manual. The logic is shown on sheet 3 of schematic 050-4008.

The controller intelligence is resident in the main LISA software. The hardware consists of a 6522 I/O port device and some associated logic. The 6522 device is a 6800-type peripheral device and is described in the 6522 data sheet.

6.5.1 System Bus Interface

This is provided by the 6522. The I/O Board internal D-bus connects to the data lines of the device, while addressing within the 16 locations contained in the port device is performed with the system bus address lines A3 through A6.

Device selection is performed by having both the DSKPT/ and VMA signals true. The former is provided by the I/O decode at B-3 on sheet 1, while the latter indicates that the processor is aware that it is communicating with a 6800-type device and has modified the bus signals accordingly. Refer to the 68000 user manual for a discussion of the VMA signal.

The resulting address map for the port is shown in Figures 2-11 and 2-12.

Device reset is performed at the same time as system reset by means of the RESET/ signal at D-4, which originates on the system bus.

The device interrupts the system by means of the IOIR/ line, which is wired-ORed with the floppy disk controller interrupt FDIR/ originating at B-1 on sheet 4.

Device clocking is performed by the E signal from the system bus, which is connected to the phi2 input and provides a 6800-type compatible clock.

6.5.2 Parallel Port Interface

The 6522 provides two 8-bit ports -- the A port and the B port -- for use in the interface itself. The A port is used as the 8-bit parallel data interface, while the B port is used for control lines.

The LS280 at C-3 is used to check parity as data is being read from the interface into the LISA. The result of the check is latched in the LS109 JK Flop at D-3. The input is presented as PRES/ to the keyboard port at C-3 on sheet 1 to permit the flip-flop to be reset. The Q output is connected to the #2 control line of port B on the 6522. The second LS280 at D-3 is used to generate parity.

The lines on the B port are used as control and status lines on the interface as follows:

BSY connects to PB1 and indicates to the 6522 that the interface is busy and is unable to accept any transfer operations. It also connects to CA1 to inhibit the data port for the duration of the busy condition.

OCD is Open Carrier Detect and connects to the PB0 line of the 6522. This signal is normally held low at the peripheral end to signify that the cable is connected. The system monitors this line and assumes that no transfer can be performed when it is high/true.

The signal which is driven by PB2 is used as an enable to the entire interface. When it is asserted, both the LS245 8-bit data transceiver and the LS244 control line drivers are enabled.

DR/W/ is output to the peripheral as an indication of the direction of data transfer from the PB3 line. It is also used to define the direction of the data transceiver's drivers.

CMD/ is output to the peripheral from the PB4 line. When it is asserted, it indicates that the data on the bus is to be interpreted as a command when DR/W/ is low and as status from the peripheral when DR/W/ is high.

DSKDIAG is not input from the peripheral but originates in the FD Controller section at B-1 on sheet 3. It indicates on PB6 that the system is operating the interface in diagnostic mode.

The port control lines of the 6522 are used as follows:

CA1 is used to monitor the state of the BSY line from the peripheral and to strobe the data on the A port accordingly.

CA2 is used to provide the PSTRB/ (Peripheral Strobe) signal to the interface, which indicates that either data is available for a write or data has been received for a read operation.

CB1 is used as a control signal to the adjacent 9512 arithmetic device and is not used on the parallel interface.

CB2 is used to monitor the parity status of the interface.

6.5.3 Parallel Port Operation

Operation of the parallel port is fully under system software control and lies outside the scope of this manual. Refer to system software documentation and Chapter 2 of this manual for programming information on this port.

6.5.4 Parallel Port Timing

Timing on the parallel port is programmable and a function of software. It therefore lies outside the scope of this manual. Refer to the data sheet for a discussion of the timing limitations on the 6522 device.

6.6 The Keyboard/Mouse Controller

The interface to the keyboard and the mouse on the LISA system is implemented by means of a 6522 VIA peripheral port device and a COPS dedicated slave processor. It is also used to provide software control of the power on/off function and to provide an interface to a real-time-clock.

Details on the 6522 can be found in the data sheet. Refer to the COPS user manual for information on the device. The logic that comprises the interface controller is shown on sheet 2 of schematic 050-4008 (Appendix C).

Programming of the controller is discussed in Subsection 2.5.4.

6.6.1 The System Bus Interface

The system bus interface is implemented with the 6522 device. The internal I/O Board D-bus connects to the D0-D7 data lines. Selection among the 16 internal register destinations is performed by the A1 through A4 address lines from the system bus.

The device is selected when both the VMA/ signal on the system bus and the I/O decode output at pin 7 of device

U4E are asserted. This indicates that the Processor Board is performing an access to the Keyboard/Mouse controller in a 6800-type compatible cycle.

The address map of the controller as seen by the system software is shown in Figure 2-15.

The device is clocked by the 6800-type compatible E signal and reset concurrent with the main system through the RESET/ line.

6.6.2 The COPS Slave Processor

The COP421 device shown at D-3 on sheet 2 is described in detail in the COPS user manual.

As well as controlling data flow from the keyboard and mouse, the COP421 is responsible for maintaining the Time of Day clock. In order to be able to do that, it requires a power supply which is independent of the main supply and remains on even when the LISA system is in a power-off state. This is described in the next subsection.

The COPS connects to the A port of the 6522, with the CA1 and CA2 control signals of the 6522 being attached to the S0 and S1 lines of the COPS. In addition, the port PB6 control output signal connects with D3.

The other lines from the COPS are used as follows:

SK is the output to the keyboard. In conjunction with the D2 line, it is used to send a synchronization pulse to the keyboard to initiate data transfer.

D1 and D2 are the multiplexed data inputs from the keyboard and the mouse.

G0 and G1 are the select signals which are used to control the data multiplexer which provides keyboard and mouse data on D1 and D2.

D0 is used to switch the LISA system on and off under control of firmware resident in the COPS.

G2 is used to interrupt the system by means of the NMI/ (non-maskable interrupt) at B-2, which is presented to the processor board via the system bus.

G3 is used to sense the state of the system power switch on the lower left of the LISA chassis.

CK1 and CK2 are inputs to the COPS oscillator from timing circuit at D-2. They are used to generate TOD data as well as provide internal clocking to the COPS.

RST is the COPS internal reset input which is used to perform a power-on reset in the COPS should its own power have failed for any reason.

6.6.3 Keyboard/Mouse Interface

The mouse interface is simple and consists of the LS153 dual 4-to-1 Multiplexer at D-2. The selection of data to be input to the COPS is performed by configuring the G0 and G1 outputs from the COPS.

The COPS polls the signal states by cycling through the signals input to the mulitiplexer to poll their status. The movement of the mouse is detected by pulse edges on the relevant direction lines. The three inputs SW0-SW2 reflect the state of up to three switches on the mouse. In the current LISA only one mouse switch is present and is connected to the SW0 line.

Keyboard data is input on the KBD line. This line is pulled low by the COPS in a SYNC pulse to signal the keyboard to send data if it has any. This is done via the COPS SK output with the D2 output being asserted simultaneously.

The keyboard responds with an ACK pulse on the KBD line, followed by a serial 8-bit byte which indicates the code for a key pressed or released. The keycodes are outlined in Figure 2-14. If no key has changed its state, no ACK pulse will be sent.

Refer to Chapter 8 for a discussion of the keyboard side of this interface.

The data presented to the COPS is selected as shown in Figure 6-13.

(Insert Figure 6-13)

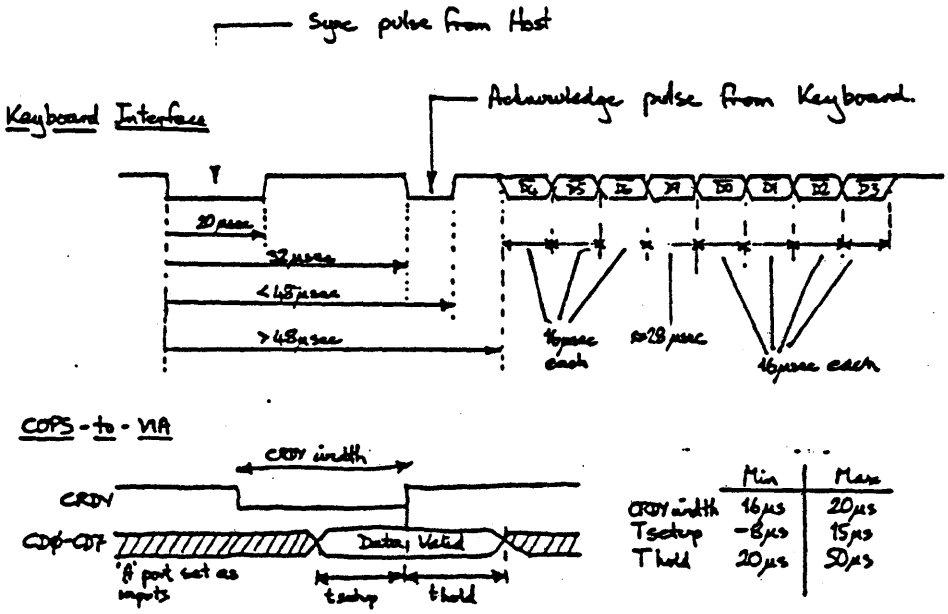


Figure 6-13. Keyboard Data Format and Timing

6.6.4 Power-on/Reset Logic

This logic is connected to the Keyboard/Mouse controller since the COPS has control of the system power through the ON signal. It is shown at C-1 and C-2 on sheet 2.

The power-on switch is sensed through the PWRSW/ signal, and is wired-ORed with the reset line which gates Q11. Either signal results in the input to G3 being asserted.

The COPS has control over the system power, via the ON line. The COPS may be programmed to turn system power on under control of the real-time-clock. The RTC is not capable of turning the system off.

6.6.5 Other Control Lines

The keyboard/mouse controller makes use of only the A port of the 6522. The B port is used to provide an interface to the system for several control lines which would otherwise require additional hardware to implement.

The use of the B port lines is as follows:

PB0 is used to reset the keyboard under software control.

PB1-PB3 are used for output of the digital value of the alarm speaker volume, used in the speaker control circuitry at C-4 on sheet 5.

PB4 is used to input the FDIR (Floppy Disk Interrupt) status, which has been latched by the FD slave processor in the LS259 at B-1 on sheet 4.

PB5 is used to sense the PRES/ reset, derived from the CRES/ bus signal at C-3. The CRES/ signal is pulled low at power-on time to reset all controller devices. PB5 can be used to reset a parity error on the parallel interface at D-3 on sheet 3.

PB6 is used for the COPS handshake as described above.

PB7 is used to output the CRES/ reset signal to the parallel port interface at pin 117 of the J1 connector.

6.7 Miscellaneous Logic

The I/O Board contains several blocks of logic, which have been located there for optimal use of board space within the LISA system.

This section describes the hardware implementation of the following functions:

* Arithmetic Processor
* Speaker Volume Control
* Battery Power Control
* Video Contrast Latch

6.7.1 The Arithmetic Processor

An arithmetic processor device may be optionally installed in a LISA system. It provides enhanced capacity to handle large amounts of arithmetic calculations, freeing the CPU for other tasks. The function is provided by the 9512 device shown on sheet 3 of the schematics. It is described in detail in the 9512 data sheet.

The device is addressed by means of the SEL9512/ signal, which originates in the decode logic at B-4 on sheet 3. This is asserted when address line A10 is high and A11 low. The A3 line is used to indicate whether data or a command is being transferred.

The device is clocked at a 2MHz rate with the 2M signal. It uses the PAUSE signal to inhibit DTACK/ to the system until calculation results are ready.

The CB1 line of the parallel port controller 6522 is used to detect the END signal.

6.7.2 Speaker Volume Control

The LISA system is equipped with a speaker, the volume of which can be controlled by the system software.

The value of the volume is presented to the PB1-PB3 lines of the Keyboard 6522, and these are input to the D-to-A ladder network shown at C-4 on sheet 5.

The resulting analog value is presented as a voltage to pin 10 of device U10A. This operates as a voltage follower to present a low input impedance to the D-to-A ladder network.

The resulting output amplitude is used to define the level of the tone frequency input to the base of Q5. The output signal is presented to pin 13 of A10, which drives the power transistors Q3 and Q4 to give the speaker output signal.

6.7.3 Battery Supply and Control

The LISA system is equipped with a battery power system which is located on the I/O Board. It provides a +5V supply to operate the COPS in the Keyboard/Mouse controller should the system be completely disconnected from a source of power in order that the Time-of-Day clock logic will continue to function.

The battery automatically recharges itself when the system is on. The battery is capable of running the COPS for 10 hours without loss of data. Once battery power is exhausted, the battery supply shuts down in a matter of milliseconds to avoid erratic COPS operation.

The circuit is shown at the bottom of sheet 5. It is designed around the 4193 voltage regulator. Recharge power for the batteries is provided by the +12VDC supply through diode D7. Zener D8 prevents excessive voltage being put on the 5V supply being output.

The 4193 operates essentially by pulling the LX output to ground, then allowing it to fly back up to produce the output voltage. L1 is the flyback inductor, while capacitor C12 smoothes the output.

The frequency with which the 4193 does this depends on the voltage sensed by the LBR and VF inputs on the precision voltage-divider formed by resistors R19-R21. The VF input looks for a 1.3V reference. This voltage is higher than this when the +5V STBY supply is operational. This supplies a level of approximately 5.7V. Allowing for a diode drop of 0.3V across D3 still results in the +5B level being pulled to over 5 volts. At this time, the battery is being recharged.

When the main system is disconnected from a source of power, the +5 STBY is removed and the +5B level begins to drop, which triggers the 4193 through the sensing inputs from the ladder to attempt to restore the level. The 4193 is capable of providing an acceptable +5 volt output for battery voltages as low as +2.4 volts.

The LBR input detects the level being unacceptably low on the output, which pulls the LBD output low. This resets the flop formed by the two gates of CMOS device U14B and pin 4 goes low. This forces Q6 to be back-biased and disconnects the load from the battery output. This is done to avoid cell reversal, which can destroy nickel/cadmium battery cells.

When the normal 5V supply is operational, the pin 10 output of the inverter causes the flop to be held off and transistor Q4 is always on.

6.7.4 Video Contrast Latch

This is shown in the upper part of sheet 5 of the schematics.

The data is input via the parallel port interface 6522 A port, which is latched in the CMOS 74C174 at D-3. The data is presented to the summing network, which presents the result of the D-to-A conversion as a DC voltage to pin 3 of the low-input-impedance voltage follower in the first stage of device U10A.

The output of this is fed through R19 to the second stage of device U10A, which functions as an inverting amplifier with a gain of unity. The bias network formed by resistors R10 and R11 provides a bias voltage of approximately 3.5V to pin 5. The RESET signal will pull this point to ground, which blanks the screen.

The CONT output can vary between +2V (fully black) and +7V (fully white). This signal is an input to the video board, which is described in Chapter 7.

CHAPTER 7

THE VIDEO BOARD

The video board is a PCB which provides most of the analog circuitry for operation of the CRT display in LISA. It is located in the CRT enclosure, mounted on the rear wall.

The video board is driven by the video digital control logic on the processor board. Refer to Section 4.5 for a description of the video control.

Note that the video board contains hazardous voltages. Extreme care should be taken when operating the LISA system with the video board exposed for troubleshooting or any other reason.

7.1 Video Board Block Diagram

The video board can be functionally divided into several major blocks in order to better understand its operation. These are:

* Power supply circuits
* Video amplifier circuits
* Vertical deflection circuits
* Horizontal deflection circuits

The function of the video board is to process the bit stream of serial display data it receives from the processor board and translate it into a display by means of the raster scan on the screen. To perform this, signals which synchronize the raster sweep with the data are also provided by the processor board.

An overview of the video board in the form of a block diagram is shown in Figure 7-1.

(Insert Figure 7-1)

This chapter will refer to the video board schematic, number 050-4012-A, located in Appendix D.

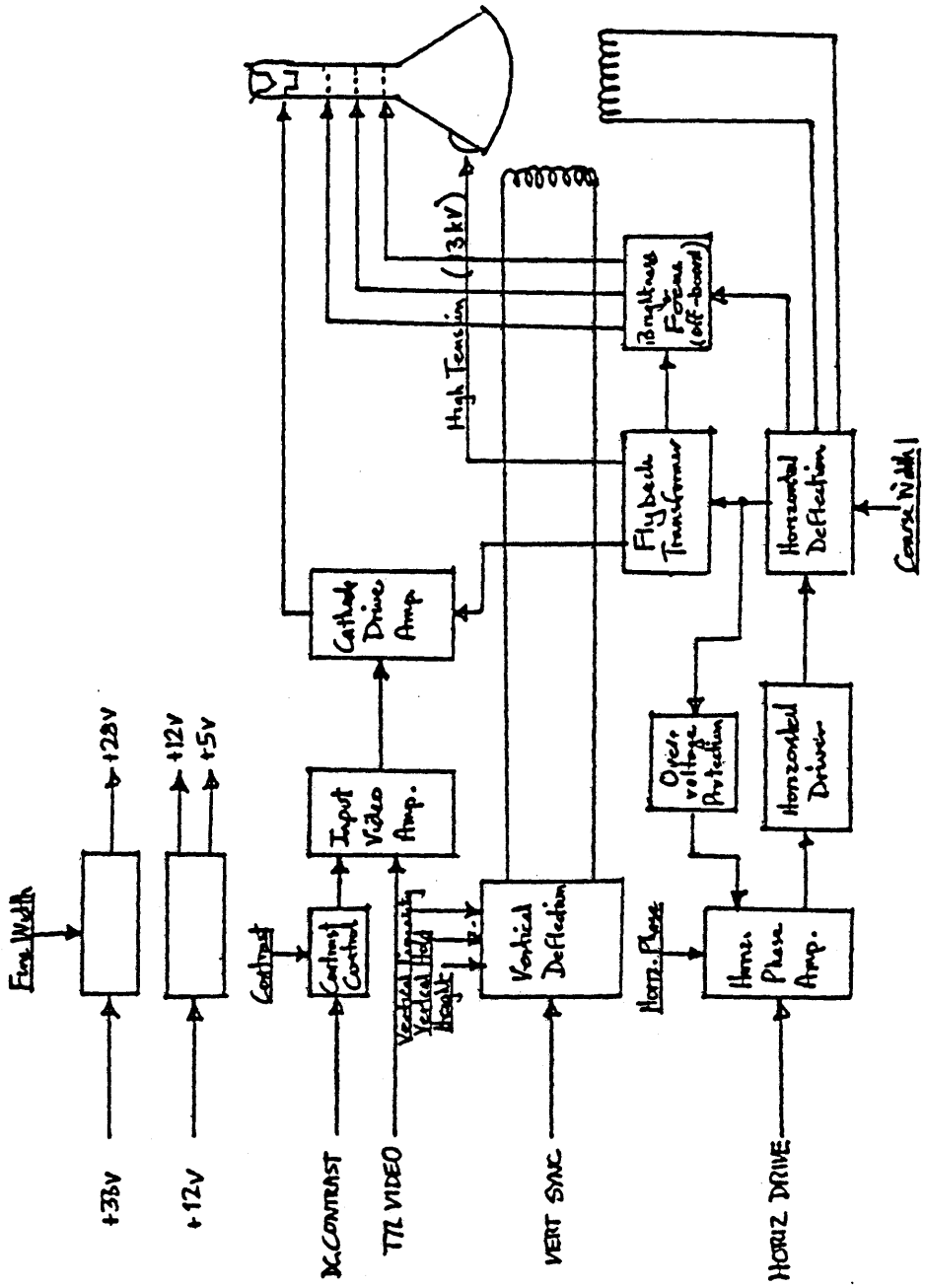


Figure 7-1. Video Board Block Diagram

7.2 Power Supply Circuits

Power is supplied to the video board via the connector at the upper left of the schematic (see Appendix D). The +12VDC is the same as that supplied to other circuits in the system. The +33VDC is used exclusively by the video board. Refer to Chapter 10 for a discussion of the power supply and its capabilities.

7.2.1 The +12VDC and +5VDC Supply

The +12VDC input is a semi-regulated voltage from the power supply. It is applied to pin P of the connector and is used to provide the following:

* Power to the +5VDC regulator
* Power for the CRT filament
* Collector supply to transistor Q8

The +5V regulator consists of the current-limiting resistor R4, the 5.1V zener diode CR1, and the filter capacitor C3. This supply is used to provide the collector supply of transistor Q7 and also to provide base-bias for Q2. The current provided by the +5VDC supply is in the order of 30 milliamps.

7.2.2 The +33VDC Supply

The +33VDC input is an semi-regulated voltage provided by the power supply. It is applied to pin 5 of the connector and is connected directly to the 24-volt 3-terminal voltage regulator U1. The regulator may accept voltages in the range +33 to +36VDC and continue to operate correctly. Voltages below about +32VDC will prevent the regulator from performing properly.

The reference terminal at pin 2 of U1 is biased above ground by the resistor ladder formed by R1, R2 and R3. Adjustment of the potentiometer R2 will result in an output voltage at pin 3 which will be 24V plus the DC voltage on pin 2. The normal voltage range at pin 3 will be between +26 and +30VDC. The function of this adjustment is to provide a fine control of the width of the display on the CRT screen.

Capacitors C1 and C32 are provided to suppress parasitic oscillations in the regulator. and C2 acts as a storage capacitor for the load.

The regulated +28VDC (nominal) provided by the supply provides power for the rest of the video board and the CRT.

7.3 The Video Amplifier Circuit

The function of the video amplifier circuit is to take the serial TTL data provided by the processor board and convert the digital information into black (logical 0) or white (logical 1) pixels on the screen by controlling the cathode emission in the CRT.

7.3.1 Video Data Input and Contrast Control

TTL-level video data is presented to the video board on pin 1 of the connector. It is impressed on the base of transistor Q6 by way of the current-limiting resistor R51. Resistors R51 and R52 form a voltage-divider network to increase the noise-rejection of Q6, which effectively acts as a high-speed switch. The collector of Q6 is therefore at ground or at a DC level, depending on the digital state of the TTL input.

The actual DC voltage level is controlled by the contrast control circuitry. The programmed contrast DC level is provided by circuitry on the I/O board. Refer to Chapter 6 for details of this signal. Potentiometer R5 provides manual adjustment of the level actually presented to the emitter-follower amplifier formed by transistor Q1. Resistor R6 C47 make up a low-pass filter which provides smoothing of the incoming DC contrast level.

Transistor Q1 is connected as an emitter-follower in order to provide the high current required to drive the low impedance of R8. The higher the voltage on R8, the larger the contrast between black and white in the final pixel on the CRT.

Note that there are no gray levels in the LISA video circuitry. Gray tones may be generated by pixel interleaving under software control. The details of this lie outside the scope of this manual.

7.3.2 Cathode Drive Circuit

The collector output of trnsistor Q6 is passed on to the base of the stacked transistor pair Q2/Q3. The advantage of this circuit is that it combines the advantages of the high gain of Q3 with the ability to withstand high

voltages of Q2. Capacitor C6 and resistor R11 are used for high-frequency peaking. Resistor R10 was added to the circuit to prevent transistor Q2 from going into cutoff when the screen is blank.

The collector load for Q2 consists of the peaking coil L1 and collector load resistor R14, with R13 providing a shunt to damp L1. The collector voltage on Q2 is dependent on the polarity of the pixel being displayed. For black, it is about +60VDC, while for white it will be from 10 to 30 Volts lower. The exact voltage level for white depends on the setting of the contrast R5 and the input DC contrast level at pin B on the board control circuit.

The flyback transformer assembly at B-2 of the schematic provides a +60VDC power source at pin 2 on connector P-3. This is modulated by the storage capacitor C8. Capacitor C7 and diode CR3 form a decoupling network, which ensures that the beam current to the cathode is removed at power-off time. This is known as a "spot-killer" and prevents the burnout of phosphorus at one point on the screen.

The output of Q2 is passed through the 220 ohm arc-protecting resistor in the cathode lead. This prevents any arcing voltages in the tube reaching the video amplifier circuitry. Diode CR2 is normally reverse-biased. In the case of an arc occurring in the CRT, this shunts the high-voltage on the lead, acting as an arc-suppressor. The lead connects to pin 2 (cathode) of the CRT itself.

7.4 Vertical Deflection Circuitry

The vertical deflection circuitry is used to position the horizontal scan of the CRT at the appropriate position in the vertical axis. It is shown in the left center part of the schematic and consists largely of integrated circuit U2 and its associated components.

Vertical synchronization pulses are provided by the processor board on pin A of the connector. This TTL signal is passed through coupling capacitor C9 and current-limiting resistor R17. The resulting signal pulses are fed into the input of the TDA 1170 at pin 8.

7.4.1 Vertical Deflection Oscillator

The RC network formed by C10 and R19/R20 provides a timing period for the oscillator internal to U2. Potentiometer R19 enables the period to be varied into sychronization

with the periodic screen refresh. This acts as a vertical hold.

The network connects to pins 6 and 9 of U2.

7.4.2 Vertical Voltage Amplifier

Internal to U2 is a circuit used to control the amplitude of the vertical deflection.

The gain of this amplifier is controlled by the amount of current sunk to ground from pin 7 of U2. This is a function of the resistance provided by R21 and R22. Potentiometer R22 allows this value to be varied; this adjusts the amplitude of the vertical saw-tooth voltage and thus the physical height of the display on the CRT screen.

The voltage amplifier output is present on pin 1 of U2. It is utilized in two distinct places:

The first use is as an input to the feedback network formed by R31, R32, C15 and C16. This controls the linearity of the sawtooth waveform which is output at pin 1. This can be adjusted by potentiometer R31. The network feeds back to pin 12 of U2.

The second use is as an input to the power amplifier stage through summing resistor R29 to pin 10 of U2.

7.4.3 Vertical Power Amplifier

Input to the power amplifier is at pin 10. The amplified output is available at pin 4 of U2. The output signal follows four paths:

The first path is fed back into the power amplifier via C14 and R27 to limit the high-frequency response and to prevent parasitic oscillations.

The second path is passed through the vertical deflection coils via pins 1 and 2 of connector P1 and is passed to ground via resistor R33 and capacitor C19.

The third path passes through the snubbing network R25 and R17 to ground. The circuit is effectively in shunt with the deflector coils and prevents any ringing effects in the coils themselves.

The fourth path effectively takes the signal DC component, sampled by R26 and filtered by C18, and passes it on to the summing resistor R28. This is then fed back as a part of the amplifier input signal on pin 10. This is used to establish the DC operating point of the power amplifier to ensure DC stability.

AC current passing through the deflection coils is sampled across R33. This is fed through summing resistor R30 and also presented as a component of the input signal on pin 10. This controls the AC voltage gain of the power amplifier and enhances AC stability.

7.4.4 Bootstrap Circuit

The power input to U2 is pin 2, which should have a DC voltage between +11 and +16VDC. This is provided by the voltage drop from +28V, which in turn is provided by R24 with storage capacitor C12. This voltage is also used to provide the collector supply for the emitter-follower circuit of Q1 in the video amplifier section.

Part of the output signal of the power amplifier, presented at pin 4 of U2 is also presented at pin 5. This forces pin 5 above the DC input voltage at pin 2 and reverse-biases CR5.

This forces pin 3 above the DC input voltage because of the charge stored in C11.

7.5 Horizontal Deflection Circuits

The horizontal deflection circuits provide the timing and control of the sweep of the beam across the CRT screen in the horizontal direction.

The horizontal frequency of the LISA video circuit is approximately 22.7 KHz.

7.5.1 Horizontal Input Circuit

A TTL signal indicating the horizontal drive pulse is provided by the processor board and presented to the video board on pin C of the connector.

Summing resistor R53 presents the signal to Q7, which operates as a controlled Miller integrator. Control is achieved by controlling the amount of feedback to the

input by way of the horizontal phase-control potentiometer R34. Feedback to the base of Q7 by way of resistor R36 and the Miller capacitor C20.

This circuit controls the amount of rise and fall in the input signal by means of the Miller effect. This, in turn, controls the switching point of Q8, which operates as a high-speed saturated switch.

7.5.2 Horizontal Sweep Amplifier

The output of Q8 is used to drive the base of the horizontal driver transistor Q4. The output of Q4 is in turn coupled to the base of the horizontal output transistor Q5 by way of the coupling transformer T1 and the base-current limiting resistor R45.

The RC network formed by R41 and C24 is used to control the damping across the primary windings of T1. Similarly, R44 is used to damp the secondary windings.

Power for the driver stage of the amplifier is derived from the +28VDC supply via the decoupling network formed by R39 and C23.

7.5.3 Horizontal Deflection

Transistor Q5 turns off when the base voltage goes negative. When this occurs, the stored charge in the horizontal flyback transformer and the horizontal deflection coils collapses. This causes the collector voltage of Q5 to rise to approximately 280 Volts. The rate of rise is controlled by the timing capacitor C25, which lies between the collector of Q5 and ground. Diode CR9 is used as a damper to prevent the collector of Q5 from going negative by passing the negative half of the current cycle to ground.

Energy is coupled out of the horizontal circuit by way of the flat-faced correction capacitor C26. Current is then passed through the horizontal deflection coils, through the horizontal linearity coil L2, and to ground

Coarse picture width is controlled by varying the inductance of L3, which is in parallel with the deflection coils.

The action of coil L2 is to increase the linear current ramp through the deflection coils. A magnet in the coil is used to bias it in one direction. As current is passed,

this adds to or detracts from the magnetic bias. This in turn alters the value of the inductor. R46 is used to damp any high-frequency oscillation within the horizontal deflection coil circuit.

7.5.4 Horizontal Flyback

The flyback transformer also connects to the horizontal output transistor Q5. It is used to step the voltage on the collector of Q5 either up or down.

This is used to generate the high-voltage supply for the CRT at 13KVDC, the 60VDC supply for the video amplifier and also +600VDC for the G2 voltage on pin 6 in the CRT. It also provides power for the brightness and focus circuit, which is physically located on the power supply in order that the controls are available to the operator of the LISA.

Power input to the flyback assembly comes from the +28VDC supply on pin 3 (violet).

A portion of the horizontal output signal is coupled by C27 to R47 and CR10. This provides a -100VDC source to operate the brightness and focus circuit.

7.5.5 Overvoltage Crowbar

A sample voltage from the collector of Q5 is made by the precision divider formed by R42 and R43. This is fed through the peak-detector circuit formed by CR8 and C22 and placed on the cathode of CR7.

If the voltage on the collector of Q5 should rise above acceptable limits, CR7 will conduct and provide a forward bias on SCR CR6. This latches CR6 on, shunting the collector supply of Q8 to ground. It also turns the horizontal circuits off and avoids a damaging high voltage being present on Q5. SCR CR6 will remain in this condition until power is removed from the system. It also prevents excessive voltage to the CRT, thus keeping it within the safe X-ray rating of the tube.

7.5.6 Brightness and Focus

The control circuits for these two functions are logically a part of the horizontal deflection circuit, but are physically a part of the LISA power supply for ease of operator access to these controls.

The +600 VDC high-voltage power for these circuits is provided by the components CR11, R48 and C33 from the secondary windings of the flyback transformer. The negative voltage comes from components C27, R47 and CR10.

The brightness of the CRT is controlled by adjustment of the DC voltage on pin 1 (the control grid) of the CRT. This can vary from +12 to -38VDC with respect to ground. This is adjusted by means of the 2Megohm resistor marked Brightness.

The Focus is a voltage placed on pin 7 of the CRT. It may vary between -100 and +300VDC, depending on the adjustment of the 2 Megohm resistor marked Focus.

CHAPTER 8

OPERATOR INTERFACES

The LISA system uses the CRT screen and a speaker to communicate with the operator. The operator in turn may use either the keyboard or the mouse to communicate with the system. In addition, there is a video jack available on the motherboard at the rear of the system which supplies a composite video signal and can be used to drive a secondary CRT.

8.1 The CRT Screen

The CRT screen is controlled by a combination of system software and hardware elements on the processor board and the video Board. Refer to Section 4.5 and to Chapter 7 for a discussion of the hardware.

8.2 The Keyboard

The 76-key LISA keyboard is a movable assembly containing a full key set and function keys. It is connected to the system by a standard 1/4" phone jack, located in the lower left of the front of the LISA. The keyboard layout for the standard (North American) keyboard is shown in Figure 8-1.

(Insert Figure 8-1)

8.2.1 Keyboard Logic

The keyboard logic is shown in schematic 050-4008 (Appendix E). It operates under control of the COPS device shown on the schematic at C-1.

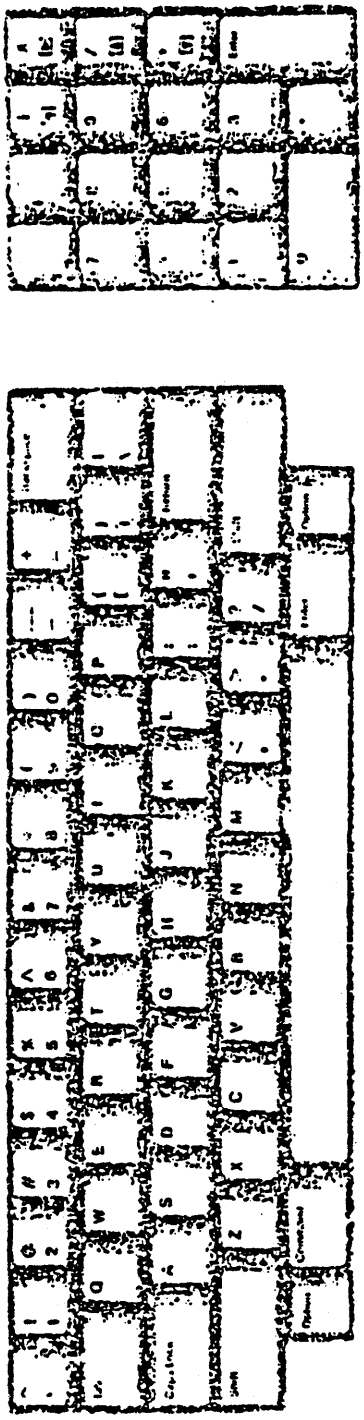


Figure 8-1. LISA Keyboard Layout

The COPS is identical to that found in the keyboard control logic on the I/O board. Refer to Section 6.5 for details of this. The same routines are present in both devices. Only those routines which apply to the actual location of the device are used.

The keys interface to five 4067 16-to-1 multiplexer devices. The COPS polls these in an upper and lower bank by means of the SK signal and the LS03 gate at C-2. The configuration of the COPS D0-D3 outputs defines which of the sixteen switches attached to each device is being selected.

The state of the switches in the bank of 4067 devices is presented to the COPS on the three lines G1-G3. The lower bank uses all three but the upper bank uses only G2 and G3.

Key data is passed to the LISA in serial form from the S0 output of the COPS via the LS03 gates at B-1 and pin 1 of the Molex connector. Synchronization pulses from the LISA are also input to the keyboard on pin 1 and passed to the G0 input of the COPS via the final LS03 gate at B-1.

8.2.2 Keyboard Timing

Transfer of data from the keyboard to the LISA is only performed when the LISA keyboard controller initiates it. This is shown in Figure 6-13. The keycodes are discussed in Section 2.4.5.

Data transfer is initiated when the keyboard data line is pulled low by the LISA for approximately 20 microseconds. The keyboard COPS senses the leading and trailing edges of this SYNC pulse and transmits an ACK pulse to indicate to the keyboard controller that data is about to be transferred.

A data byte which specifies the key is transferred in a lower and upper nibble as shown in Figure 8-2. The byte is interpreted as a key and a polarity (up or down) by the keyboard controller.

If no data is present in the keyboard COPS, no ACK pulse will be sent and the interface becomes quiescent until the next SYNC pulse.

8.2.3 Keyboard Interface

The keyboard interface to the LISA system consists of a 3-wire shielded cable which is terminated by a 3-pin Molex connector attached to the keyboard PCB at one end and a standard 1/4" phone jack plug at the other.

This arrangement is shown in Figure 8-2.

(Insert Figure 8-2)

8.3 The Mouse

The mouse is an electromechanical device which is used to move the cursor rapidly and easily around the CRT screen to perform LISA functions.

The mouse consists of a rolling ball arrangement on the under side and a cover and button on the top side. A cable connects the mouse with the 9-pin DB connector in the center of the motherboard at the rear of the LISA.

The mouse provides an alternative method of communication with the LISA system other the keyboard. The specific functions are dependent on the software currently running, but the two controls on the mouse provide the same general function in all cases: the mouse is rolled along a flat surface to move the cursor on the video screen; pressing the button on the mouse selects functions to which the cursor is currently pointing.

8.3.1 Mouse Operation

The internal components of the mouse consist basically of a switch and two directional wheels. One directional wheel detects motion forward and back (corresponding to up and down on the screen), while the other detects motion left and right.

Each wheel has a number of slots cut around the rim. These pass two photoelectric diode assemblies as the mouse is moved in that axis and the wheel turns. The two diode assemblies produce a series of pulses to the mouse interface on the I/O board.

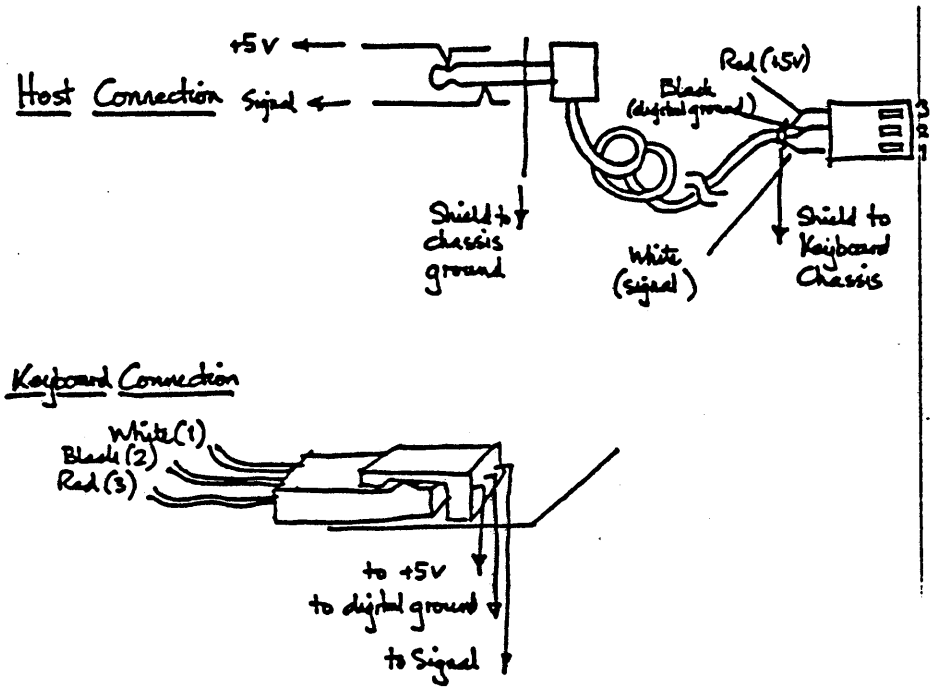


Figure 8-2. Keyboard Interface

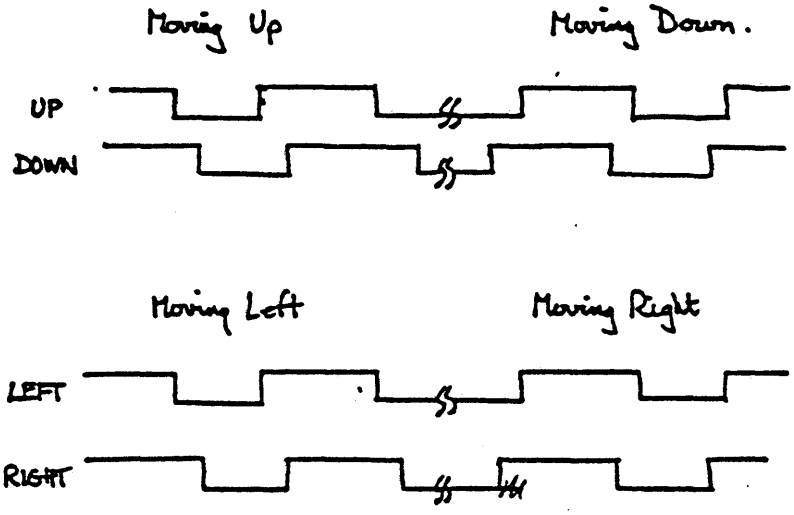


Figure 8-3. Mouse Movement Waveforms

The relationship of one set of pulses to the other indicates the polarity of the direction in which the mouse is moving and the number of pulses is proportional to the distance travelled. Refer to Figure 8-3, which illustrates this.

(Insert Figure 8-3)

8.3.2 Mouse Interface

The mouse interface is described in Section 3.5. The 9-pin DB connector is located in the middle of the connector panel at the back of the LISA. Refer to Figure 3-11 for the connector layout.

Only SWITCH1 is operational in the LISA mouse. Each pair of the LEFT/RIGHT and UP/DOWN inputs to the system both pulse as shown in Figure 8-3 when the mouse moves one increment in that direction. One increment equals a constant unit of movement in that direction on the flat surface.

8.4 Other Operator Controls

Several operator-oriented features of the system are described elsewhere in this manual in more detail but are mentioned here for convenience.

8.4.1 The Power On/Off Switch

The power switch on the LISA is located on the lower right of the front of the system. Pressing the switch when power is off will cause power to be provided to all parts of the system under control of the system boot software.

Pressing this switch when system power is on causes an interrupt to software which in turn cleans up its environments and then ejects any floppy disks in use. The system is then powered down under software control. This removes power from the entire system, with the exception of the control COPS. This device handles the real-time-clock and power-on control and receives its power from a standby supply in the power supply. Refer to Section 10.5 for details.

Whenever the system is isolated from a power source, such as might happen if the LISA is disconnected from main power or the building power is removed, a self-recharging battery maintains the voltages necessary for operation of the standby supply voltages for a period up to approximately 10 hours. The battery is automatically recharged whenever the system is turned on. Refer to Section 6.7 for a discussion of this.

8.4.2 The Reset Switch

The RESET switch is located on the motherboard at the rear of the unit, next to the video connector. It is used to restart the system in the event that an unrecoverable error has put the system in an undefined state. This should never be activated during normal processing or loss of data will almost certainly result.

The reset switch is shown at location A-4 on the motherboard logic schematic 050-4013 in Appendix G.

8.4.3 The Speaker

The built-in speaker in the LISA may be used to provide an audible warning to the operator. It is controlled by logic on the I/O board under software control for volume and tone. Refer to Section 6.7 for a discussion of speaker control.

8.4.4 The Composite Video Output

The composite video output is available on the J10 video jack at the rear of the LISA motherboard. The circuit is located on the motherboard and uses the CVOUT and VID signal outputs from the processor board (refer to Section 4.5).

The logic is shown on schematic 50-0400 in area A-3. Both the VID and CVOUT signals are effectively ORed to the base of transistor Q2. This controls the amount of current passing through Q2 and consequently through R3, which controls the amount of current passing through Q1.

The composite video signal is output to the jack via resistor R1.

CHAPTER 9

THE FLOPPY DISK DRIVES

The LISA system is equipped with two floppy disk drives for data file storage which are located one above the other at the right side of the machine. These interface to the system by means of a floppy disk controller, which is located on the I/O board and is described in Section 6.2.

This chapter does not present an exhaustive documentation on the drive. Refer to other documentation on the disk drive for further details.

9.1 Drive Specifications

9.1.1 Media Specifications

Disk size	5 1/4 inch
Media	qualified double-sided
	10,000 FCPI
Track density	62.5 TPI

9.1.2 Speed Specifications

Motor speed settle time	150 msec
Motor on time	400 msec
Head settling time	10 msec
Carriage movement	linear stepper actuator
Spindle rotation	DC Motor

9.1.3 Electrical Specifications

+5VDC standby	75mA
+5VDC running	80mA
+12VDC standby	42mA
+12VDC running	850mA
+12VDC maximum (during motor start)	1.6A

-5VDC standby	5mA
-5VDC running	8mA

9.1.4 Environmental Specifications

Same as for main system. See Section 3.2.

9.2 Drive Block Diagram

The floppy disk drive is an assembly which enables 5 1/4" flexible diskettes to be used as data storage media. In the LISA system, there are two functionally identical drives, which are controlled by logic on the I/O board.

The drive itself can be thought of as consisting of a number of component blocks, as shown in Figure 9-1.

(Insert Figure 9-1)

The motors, relays and detectors present in the drive chassis are directly controlled by the digital board, while the head read/write functions are performed by the analog board under control of the digital board.

9.3 Drive Interface

The interface to the drives is performed in the LISA by signals provided on motherboard connector J1, under control of the I/O board's floppy disk controller. Refer to Section 6.2.

9.3.1 Drive Interface Signals

The interface signals to the drive are shown in Figure 9-2.

(Insert Figure 9-2)

9.3.2 Drive Interface Timing

The density of data written on the disk is a function of the FD controller and the capacity of the medium to store bit transitions. Refer to Sections 6.2 and 6.3 for a discussion of controller operation.

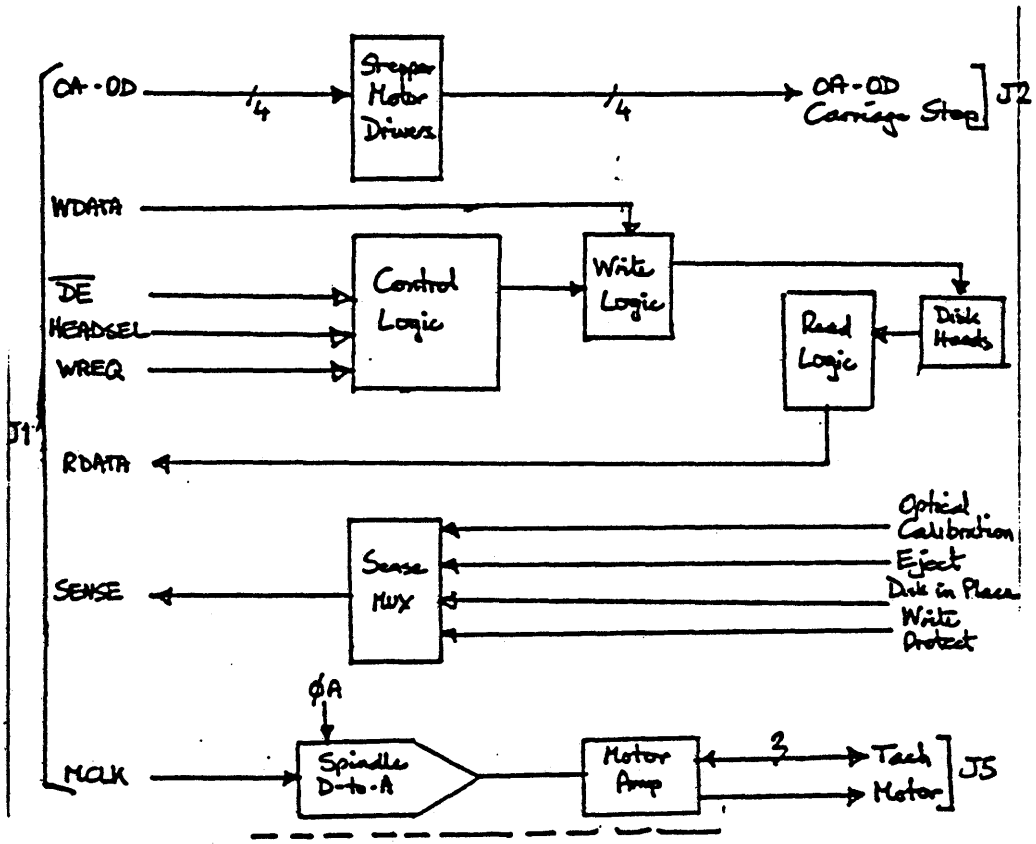


Figure 9-1. Drive Block Diagram

Signal	Pin #		Signal
+12VDC	1	2	Phase 0/motor data/sense select
+12VDC	3	4	Phase 1
+12VDC	5	6	Phase 2
+12VDC	7	8	Phase 3
Ground	9	10	Write Data
Ground	11	12	/Write Request
Ground	13	14	Read Data
Ground	15	16	/Drive Select
not used	17	18	Head Select
not used	19	20	Sense
+5VDC	21	22	Motor Data Clock
+5VDC	23	24	/IRQ
+5VDC	25	26	not used

Figure 9-2. Drive Interface Signals

Timing of the stepper motor which controls head movement is defined by the four phase lines on the interface. These are manipulated to move the heads forward or backwards.

In order to avoid inaccurate head positioning due to mechanical tolerances in the carriage mechanism, all seeks in a LISA system finish with a final motion in a direction towards the towards the optical calibration point. Note that this means that the upper head is moving away from the spindle while the lower is moving towards it. Refer to Figure 6-11.

In order to overcome the inertia during carriage acceleration and deceleration, three different periods are employed between speed transitions on the phi lines. This can be seen in Figure 9-3.

(Insert Figure 9-3)

In the quiescent state, all four phase lines are deasserted. Motion is begun by asserting two of the lines. In the forward direction (towards the optical calibration point), this would mean phi3 and phi0. In the reverse direction, phi0 and phi1. At the end of the first period, one phase is deasserted and another asserted, as shown in Figure 9-3. Note that one phase remains on while others are being changed.

When the carriage is at the required position, phi0 is always the last phase to remain asserted alone for the final period before all phases are again deasserted and the carriage is at rest.

Note that for a seek in the reverse direction, the carriage will be brought to a halt four steps beyond the desired position, and then a seek forward of four steps will be made to restore the head to the center-track position. This operation is known as overshoot.

Each step corresponds to 1/8th of a track in the LISA system. Thus all tracks are eight steps apart. In the case of difficulty in reading data from the required track, the FD controller attempts to offset by 1/8th track steps to allow for misalignment.

The optical disk calibration signal is available to the controller as an aid in overcoming differences in mechanical alignment between disks. It provides an accurate radial reference point from which seeks can be made. This is a slo known as the rezero function.

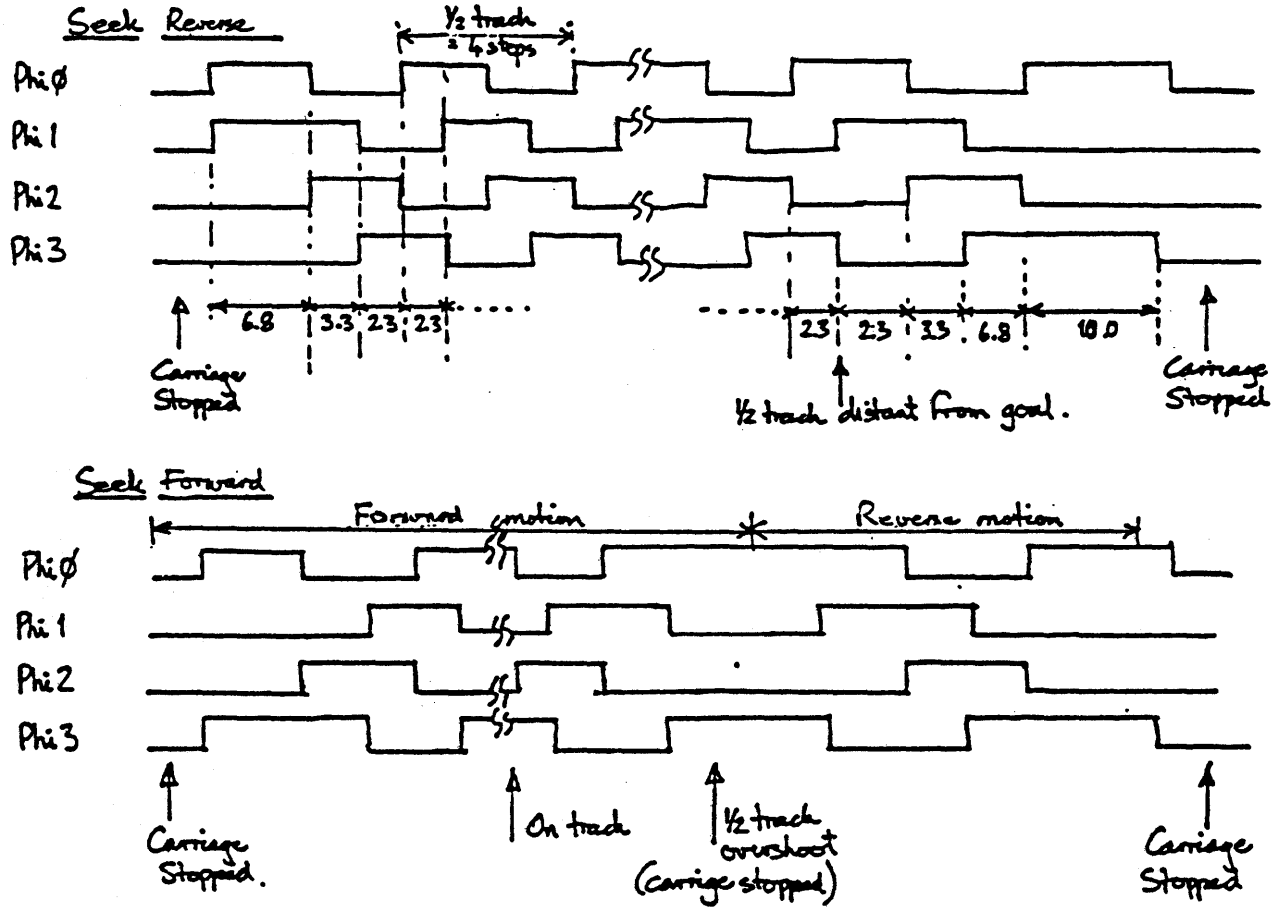


Figure 9-3. Carriage Movement Timing

9.4 Basic Drive Operation

The drive is capable of performing a number of operations under control of the signals on the drive interface.

9.4.1 Disk Insertion and Removal

When a disk is inserted in the drive, the eject mechanism is armed and a switch is activated to indicate that the disk is in place. This can be detected by the controller on the STATUS signal line (pin 20) if both the HEADSEL (pin 18) and the OA (pin 2) are asserted by the controller.

Pressing the eject button on the front of the drive causes a line to be asserted in the drive. This state can be detected on the STATUS line by holding the HEADSEL signal asserted with the OA signal deasserted.

The controller should then move the heads away from the disk until the disk-in-place signal becomes deasserted. At this point, the heads should be moved nine tracks further in order to activate and reseat the eject mechanism.

9.4.2 Head Loading

When the presence of a disk in the drive is detected, the disk heads may be loaded. This is performed in the following sequence:

* The drive motor is activated and brought to speed
* A centering cone is pressed into the disk hole
* The spindle begins rotating
* The disk is clamped to the spindle
* The heads are moved inward towards track 45
* The head load mechanism presses the heads against the disk surfaces

The steps in the above sequence are performed mechanically when the carriage is being moved to bring the heads over the disk surface. The spindle begins to rotate when clock pulses are presented to the spindle motor control via the MCLK line on pin 22.

The spindle is already spinning before being brough into contact with the disk. The clamper forces the disk to be seated centrally on the spindle with the rotation of the spindle assisting in this.

The heads are moved by pulsing the four control lines of the stepper motor OA (pin 2), OB (pin 4), OC (pin 6) and OD (pin 8) in the correct sequence.

9.4.3 Head Positioning

The two read/write heads in the drive are mounted on a single carriage, which is driven by a head positioning actuator. This consists of a linear stepper motor and lead screw.

This mechanism not only provides head-to-track positioning but also actuates a disk clamping/unclamping mechanism. This clamps the disk as the heads are moved into the reading surface and unclamps it as the heads are moved clear of the surface.

9.4.4 Data Read/Write

The ceramic heads in the drive operate in direct contact with the disk surfaces. Each head is a single element with straddle erase elements to clear the inter-track gap.

During a read operation, the heads transform the polarity reversals on the disk surface into a stream of analog pulses. These are converted to serial digital data and presented to the controller as the RDATA signal on pin 14. It is the function of the controller to interpret this data as clocking, header or true data information in accordance with the scheme with which the disk has been formatted.

The write circuitry takes the serial digital data presented on the WDATA line (pin 10) by the controller and converts it to the correct analog pulses for the write heads.

Data will be written to whichever head is currently selected, irrespective of the write protection condition of the disk currently in place. The controller senses the write protection condition of a disk by deasserting both the HEADSEL and A0 signals before polling the SENSE line.

The write-protect sense condition informs the controller that the disk currently inserted has its write-protect slot uncovered. There is no hardware protection circuit in the drive to inhibit writing to a disk which is write-protected. It is a function of the controller to decide whether or not the disk will be written to. Currently, the LISA FD controller will not write to a protected disk.

CHAPTER 10

POWER SUPPLY

The LISA power supply is a flyback-type switcher supply. The circuit diagram is shown in schematic 050-4011, which can be found in Appendix F. The supply provides the power levels and voltages shown in Figure 10-1.

(Insert Figure 10-1)

In addition to the main power supply, an auxiliary standby supply is used to provide the minimal +5V power required to run the soft-power-on and real-time-clock circuitry which is active while the LISA is in a power-off condition.

The focus and brightness controls for the video display are located on the power supply and are accessible from the rear of the LISA. They are placed here for the operator's convenience, there is no internal electrical connections between these controls and the power supply proper.

All power output lines are fully-isolated from the input AC power by means of transformers or opto-isolators, which are tested to 3.75kV on each power supply.

10.1 Power Supply Block Diagram

The LISA power supply consists of the following major components shown in Figure 10-2:

* AC Input Circuitry
* Flyback Oscillator
* DC Output Circuitry
* Standby Power Supply
* Video Focus/Brightness

(Insert Figure 10-2)

Voltage	Variance	Current
+5V	+/-5% (5.25V/4.76V)	4 to 8 Amps
+12V	+/-8% (13.0V/11.1V)	0.35 to 2.0 Amps
+33V	+36V Max. +32V Min.	0.3 to 0.7 Amps
-5V	+/-10% (-5.5V/-4.5V)	0.0 to 0.2 Amps
-12V	+/-10% (-13.2V/11.8V)	0.01 to 0.2 Amps
+5VSTBY	+/-5% (5.25V/4.75V)	0.0 to 0.1 Amp

NOTE:

The standby +5 Volts is not switched off by the ON/OFF signal.

Figure 10-1. LISA Supply Current Output

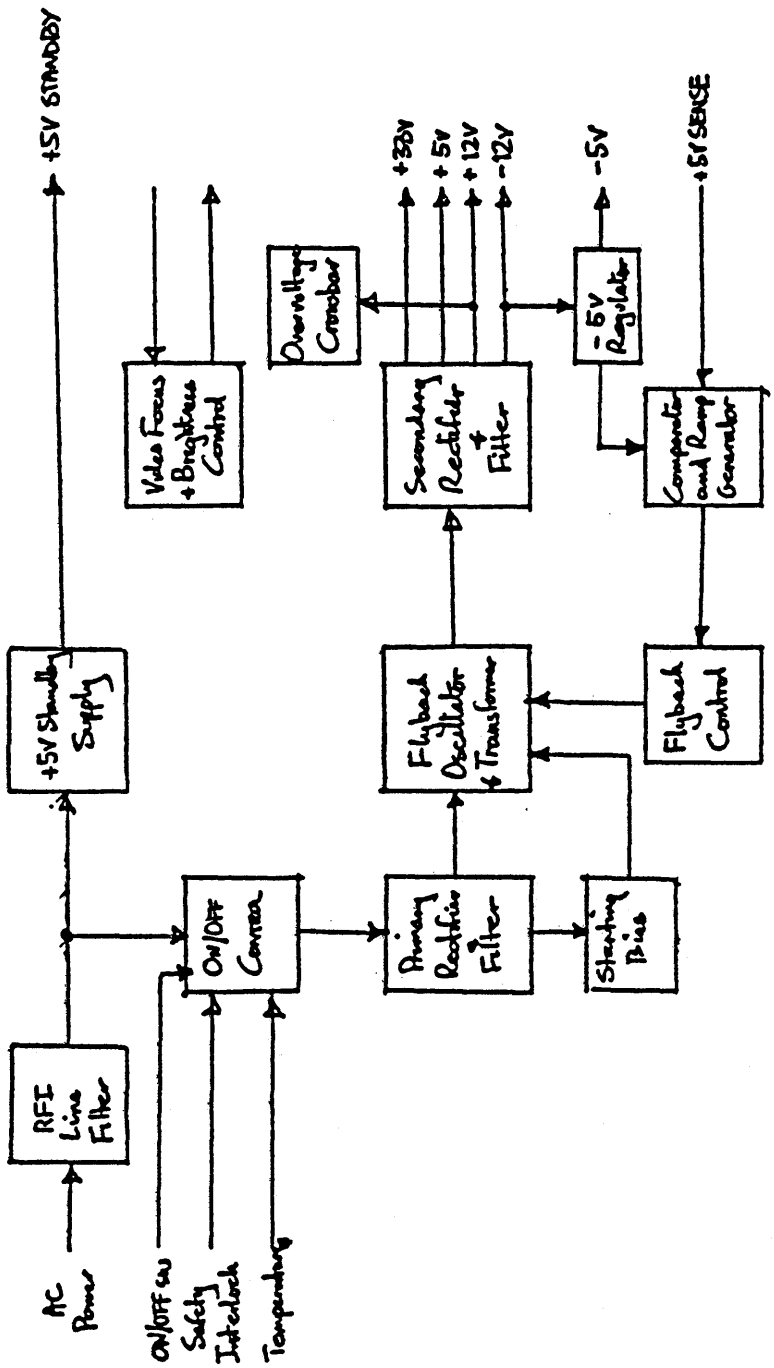


Figure 10-2. Power Supply Block Diagram

As can be seen from Figure 10-2, both conducted and radiated noise generated by the switcher is reduced by the input filter on the AC line.

* Front Panel Control
* Safety Interlock
* Over-temperature Monitor

The input AC power is then rectified and filtered before being presented to the main flyback oscillator.

The flyback oscillator operates by storing a controlled amount of energy in the switcher-transformer core during the forward cycle as the core is being charged in the form of a magnetic field. During the flyback cycle, the core discharges this energy to the load placed across the secondary windings.

The secondary windings are connected to the secondary rectifier and filter circuits which provide the DC power outputs.

These outputs are monitored by a regulator circuit, which senses the voltage level and adjusts the power being provided. In addition, there is a crowbar circuit which shuts the power supply down if the output voltages exceed the preset limits.

10.2 AC Input Circuits

Refer to schematic 050-4011 (Appendix F). The AC input circuits are shown in the upper left quadrant.

10.2.1 AC Line Connection

The AC connector P3 supplies power via the power cord and inductor L7 to the J2/P2 connector. This presents the power to the input line filter, which consists of transformer T1, chokes L1 and L2, and capacitors C1, C2, C3 and C4.

Thermistor R9 and fusable resistor R8 are provided to limit the inrush current to the power supply.

10.2.2 ON/OFF Control

Power ON/OFF is controlled by opto-isolators U3, which controls the switching triac CR2. U3 is provided with +5V from the standby supply via Q5, which biases a light-

emitting diode between pins 1 and 16. Pins 8 and 10 operate as a photosensitive zero-crossing Triac. Power is switched to the main supply via CR2.

Resistor R33 is a temperature-sensitive varistor, which biases Q2. Excessive temperature will cause Q6 to draw enough current to ground out pin X of the terminal block.

The power supply is switched on by applying a high voltage level to the base of transistor Q5, which causes transistor Q5 to conduct, which grounds pin 1 of U3. The power supply will switch on and stay on until this level is removed.

A low level on the base of Q5 keeps the power supply in the OFF condition. This may be achieved by either driving it low via the software ON/OFF or by grounding the safety interlock switch.

10.2.3 Primary Rectification

The jumper below R9 is used to select the input AC voltage which is being provided.

If 110V is selected, the connection is made to the midpoint of C12 and C13. Using these capacitors and the diodes CR5 and CR6, the input voltage is doubled using half-wave rectification. The DC voltage output from this rectification and filtering is used to charge up the core of transformer T3 through the 84-turn primary winding between pins 23 and 24.

In the case of a 220V AC line input, this voltage is full-wave rectified, using diodes CR3, CR4, CR5 and CR6. The resulting rectified DC voltage is again smoothed by the filtering capacitors C12 and C13.

Residual voltage which might be stored in the filtering capacitors when the supply is shut OFF is bled to ground via the large resistance provided by R14 and R15 in series.

10.3 The Flyback Oscillator

The focus of the flyback switching oscillator is transistor Q1 and its associated circuitry in the lower left of the schematic.

A simplified diagram of the flyback oscillator circuit is

shown in Figure 10-3.

(Insert Figure 10-3)

The points labelled in Figure 10-3 refer to the locations where waveforms, given in the following figures, may be observed.

10.3.1 Flyback Starting Bias

In order for the oscillator to begin to oscillate when power is first applied, the emitter of Q1 must be biased negative with respect to its base.

This is done by isolation of the base from the emitter by means of diode CR15. Approximately 1 milliamp of current will flow from the emitter to ground via resistors R20 and R21. This is sufficient to forward bias Q1 enough for it to switch and begin the oscillation cycle.

10.3.2 Flyback Oscillator Operation

Pulse transformer T4 receives a pulse of current each time the regulator circuit saturates. This provides a voltage to the programmable unijunction CR 17. When the voltage at pin 2 exceeds that at pin 3, the unijunction effectively operates as an SCR and shorts the input.

This grounds the base of Q1, causing it to switch off. To prevent the transistor from immediately switching on again, C30 holds the emitter positive for a short period of time, assuring a negative base-to-emitter bias.

Since current no longer flows in the collector and the primary windings of T3, the core begins to discharge its energy into the secondary windings which provide the output DC power.

During this time, transistor Q1's emitter continues to be held positive by the charge in C31, which is discharging through R40/R41 and CR15 to ground via the primary winding 28/22.

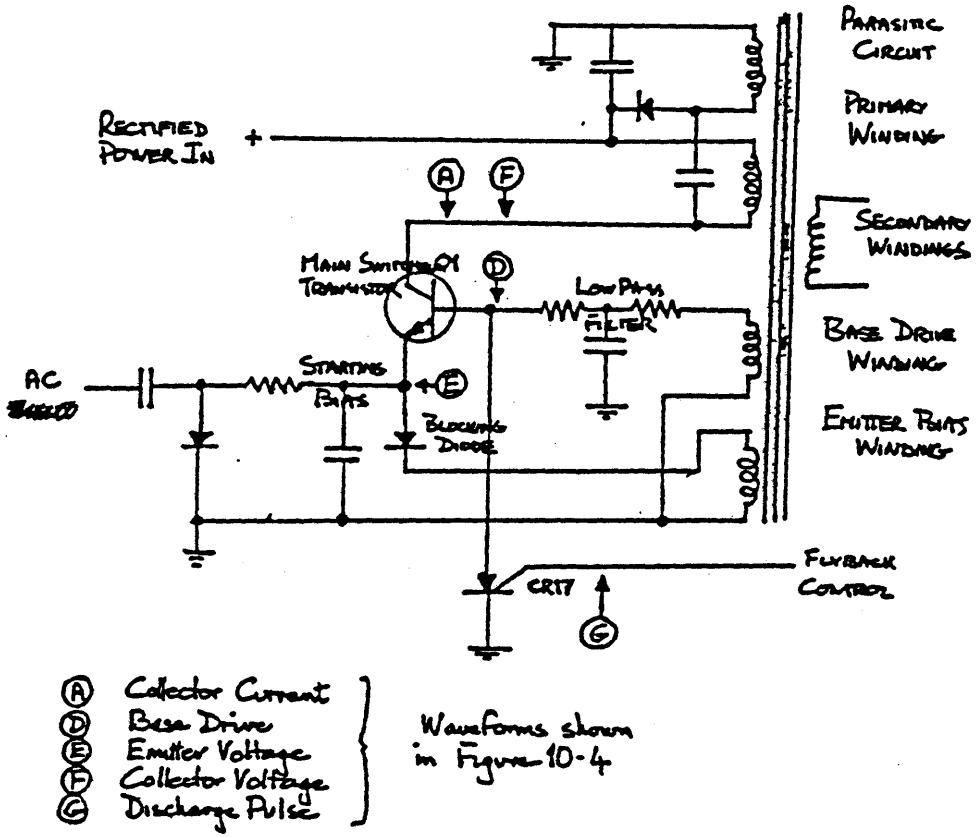


Figure 10-3. Flyback Oscillator Circuit

Once this charge has leaked away, the current on C25 biases the emitter negative again to provide a starting bias as explained in Subsection 10.3.1 above, and transistor Q1 begins to conduct. This causes current to flow through the collector and the primary winding 23/24. This induces a magnetic field in the transformer T3 core.

The waveforms at several critical points in the flyback section are shown in Figure 10-4. The letters correspond to the positions where these may be observed, as shown in Figure 10-4.

(Insert Figure 10-4)

The parasitic winding of transformer T3 provided by the primary 25/26 is used in conjunction with CR12, CR23 and C23 to minimize high-voltage transients, which can be generated in T3 and which could damage Q1.

10.3.3 Flyback Control Circuit

The amount of power output by the supply is a function of the amount of power which is permitted to be stored in the core before the discharge pulse transfers it to the secondary windings.

The discharge pulse is generated by the circuits at the lower right of the schematic, which are shown in block diagram form in Figure 10-5.

(Insert Figure 10-5)

The level of the +5V line is taken as the measure of all voltage levels being presented to their loads, since all voltages are effectively proportional in the switcher-type supply. This is sensed via pin N of the terminal block and presented to the the top of the voltage adjustment pot R29 via resistors R26 and R27.

A -5V reference from U2 is fed through resistor R30 and the temperature compensating diode Q4 to the bottom of R29. When the voltages are in balance, the adjustment tap on R29 will have a nominal zero volt bias. Otherwise, a voltage bias is applied to the base of Q3, which operates

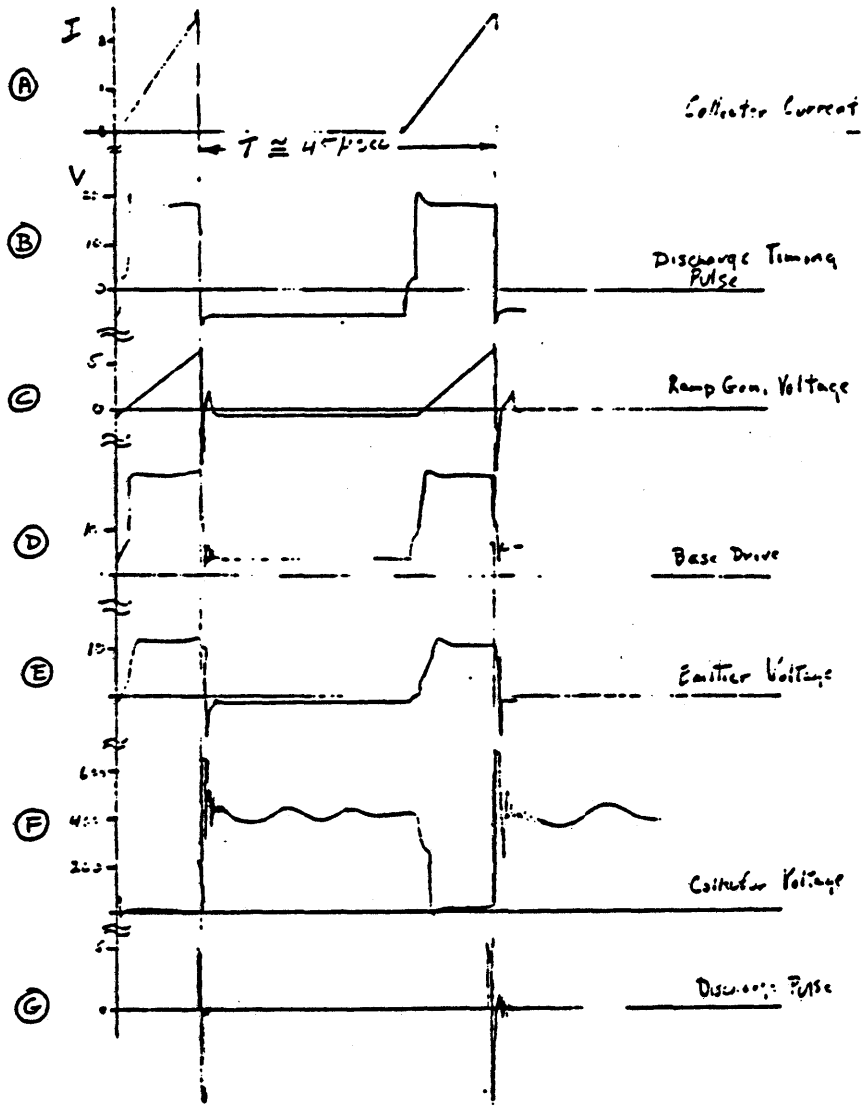


Figure 10-4. Flyback Oscillator Waveforms

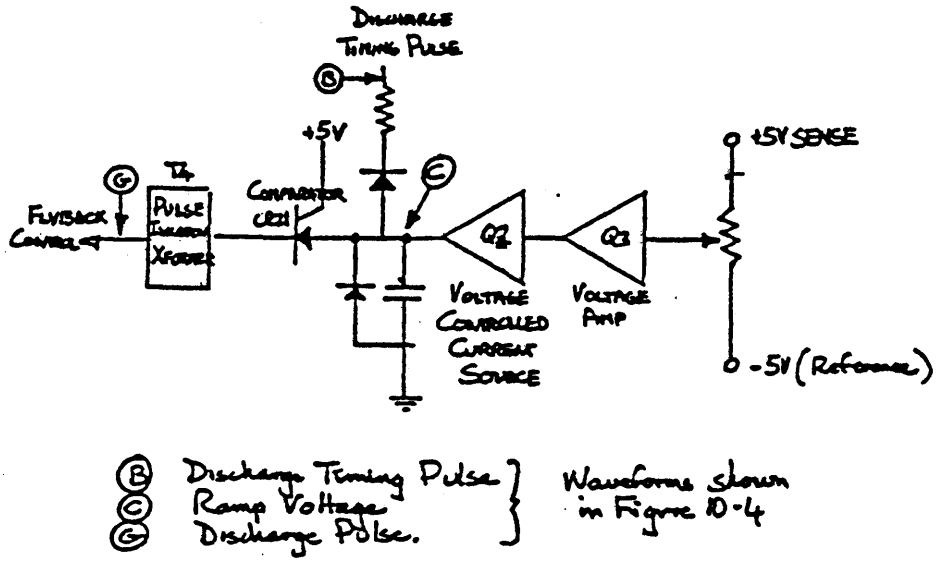


Figure 10-5. Flyback Control Block Diagram

as a voltage amplifier in conjunction with R25 and R32.

The amplified voltage is presented to the base of Q4 through R28. This permits current to flow in proportion to the voltage applied to its base, operating then as a voltage-controlled current source.

The path provided to the -12V line via CR19 and R24 causes the voltage on C34 to start up from zero volts at the same time that transistor Q1 in the main flyback circuit is turned on.

The voltage at C34 rises at a rate in proportion to the current being presented to it via Q4. When the voltage reaches the +5V level being simiultaneously presented to pin 2 of programmable unijunction CR21, the junction suddenly conducts. This discharges C34 to ground, which generates a pulse through the secondary winding of T4, which generates a corresponding pulse in the primary windings, which is used to turn Q1 off, as described above.

The result is a sawtooth waveform at C34. The rate of voltage rise is controlled by the error current from the transconductance amplifier. The total energy stored in the switching transformer T3 is controlled by the rate of voltage rise across C34.

10.4 DC Output Circuitry

The DC output circuitry consists of the secondary circuits to the right of the switching transformer T3 in the schematic. The power supply provides five voltages from the main switcher. These are

+5V
-5V
+12V
-12V
+33V

Of these voltages, the last three originate in their own separate secondary windings. The +5V supply originates in two windings in parallel, and the -5V supply is provided by a simple voltage regulator attached to the -12V supply.

10.4.1 DC Voltage Outputs

The +33V supply comes from secondary winding 16/34 on T3, is smoothed by the C9, C10 and L3 network, and presented on pin D of the terminal block. C11 removes high frequency noise.

The +12V supply originates in the 20/33 winding, with pin 20 already being biased by the +5V supply section. It is smoothed by C14, C15 and L4 and presented on pins 5,9,10,E,K and L on the terminal block. It is also equipped with a crowbar over-voltage protection circuit, described in Subsection 10.4.2. Capacitor C16 removes high-frequency noise on the voltage. The +12V supply provides the power for the voltage-controlled current source in the oscillator control section. Refer to Section 10.3.3.

The +5V supply is taken from two secondary windings ganged together and passed through the smoothing circuit formed by C18, C19 and C21, with C22 removing high-frequency noise. It is available on pins 11, 12 and M of the terminal block.

The -12V supply comes from the 17/34 secondary winding of T3 and after smoothing through C27, C28 and L6 it is placed on pin W. The -12V supply is also used to provide the current being fed through Q2 in the oscillator control circuit (see Section 10.3.3).

The -5V supply is tapped from the -12V supply by means of the voltage regulator U2. It is smoothed with C24 and presented on pin 19.

Diodes CR7, CR8, CR11 and CR18 prevent reverse power leakage through the transformer during the charging portion of the cycle.

High-frequency noise originates in switching supplies and thus must be removed from the output voltages by the 0.1 microfarad capacitors C11, C15, C16 and C29.

10.4.2 DC Voltage Controls

There are two mechanisms by which the output voltages are monitored in the LISA power supply:

First, voltages are maintained at the level selected by potentiometer R29 by means of the oscillator control section described in Section 10.3.3. Adjustment of the pot raises and lowers all voltages proportionately.

Second, protection for the power supply load is provided by a crowbar circuit attached to the +12V supply line. The +12V level is presented to the 12-volt zener CR9 through R12. Should the voltage rise enough above +12V to trigger the diode breakdown, the voltage is applied to pin 3 of The SCR at CR10, causing it to conduct. This effectively shorts the +12V line to ground, which removes the current source for the oscillator control circuit at Q2. This halts the oscillation, as no firing of CR21 can now take place. Q1 is never switched off and the core ceases to be repetitively charged, causing all output voltages to decay to zero.

10.5 Standby and Auxiliary Video Circuits

In addition to the main switcher supply itself, two other circuits are present in the LISA power supply. These are:

* +5V standby supply
* Video focus/brightness adjustments

These are described in this separate section because they function independently of the main supply.

10.5.1 The Standby Supply

The standby +5V supply is a "brute force" type and is shown across the top of the schematic. Input AC power from the line filter is presented to the transformer T2. The secondary windings 10/11 and 8/9 each provide approximately 10VAC 180 degrees out of phase. These are rectified by diodes CR1 and CR22.

The resulting DC voltage has its ripples smoothed by C7 and AC transients removed by C17, before being presented to the 5-volt regulator U1. The resulting +5V output is made available on pin 20 of the terminal strip.

Note that this line has a low current capacity and is not intended for general usage within the system.

10.5.2 The Video Controls

The video controls consist of the resistor network shown towards the upper right of the schematic.

Focus is controlled by the potentiometer R3, while brightness is controlled by R5. Both potentiometers are

adjusted by means of the knobs projecting from the rear of the power supply. They receive their power from the video board via the +300V level on pin 1 and the -100V level on pin B.

CHAPTER 11

SYSTEM ASSEMBLIES

The Lisa system has been engineered to provide maximal serviceability of system components by the user. Refer to Section 3.1 for a discussion of system packaging. A general view of the system assemblies is given in Figures 3-1 and 3-2.

The LISA system assembly components are displayed in the LISA Product Tree (Appendix H). An overview of the major components is shown in Figure 11-1.

(Insert Figure 11-1)

As can be seen from the figure, system components can be categorized into two classes -- user-serviceable and non-user-serviceable. This chapter is concerned principally with the latter as the former are discussed in other LISA documents.

Note that any nuts or screws lost in the base of the LISA can be retrieved by tipping the unit forward. It will then slide out of the air vents at the lower front of the chassis. Removing the bottom cover should not be necessary.

11.1 User-Serviceable Components

Access to and replacement of user-serviceable components is described in step-by step detail in the user documentation. Refer to the list of documentation in the preface of this manual.

Components which are user serviceable through replacement with a functioning unit are:

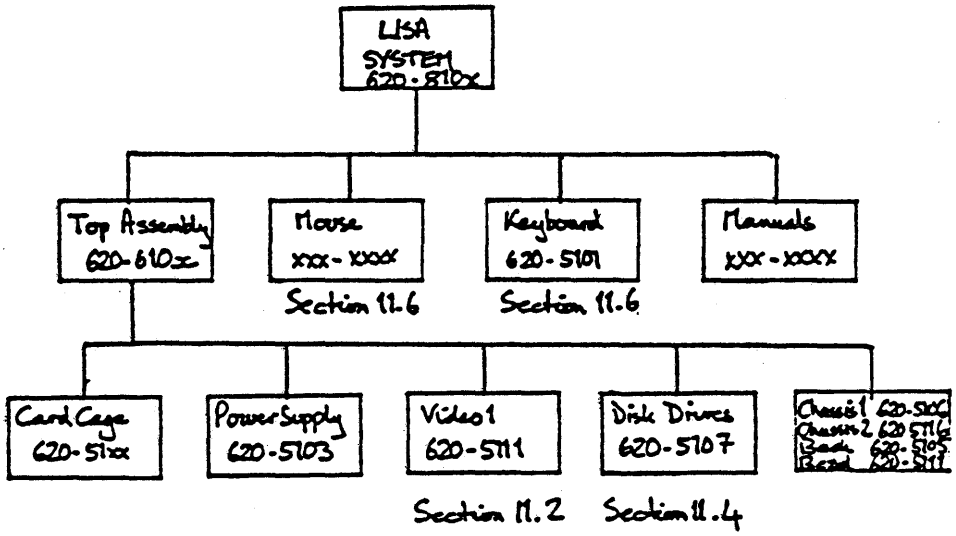


Figure 11-1. LISA Assembly Overview

* Floppy disk drive assembly
* Power supply
* Motherboard
* Processor board
* I/O board
* Memory boards
* Expansion boards
* Keyboard
* Mouse

Servicing of the non-user-serviceable components requires a knowledge which includes high-voltage power supply and video electronics. Dangerous voltages are present and all service personnel must be trained in their use.

11.2 CRT Monitor Assemblies

The CRT monitor assembly includes the assemblies shown in Appendix H under "subassembly, video one" (620-5115) branch of the tree. These are:

* Cathode ray tube 707-0007
* Deflection yoke 159-0007
* Video board PCB assy. 620-x121
* Video board PCB fab. 820-4012
* Flyback transformer xxx-xxxx

Refer to assembly drawing 620-5115 (Appendix I). This shows an exploded view of the basic LISA chassis with the CRT monitor components.

11.2.1 Tube Access

To remove the CRT tube itself, perform the following steps:

a) Remove the front panel, rear panel, power supply and card cage, as shown in the Owner's Guide.

b) Use a Phillips screwdriver to remove the two screws underneath the top rear of the unit. Lift the top of the unit up from the rear, unhook the front where it is hooked in place and remove the top.

c) Remove the white ground lead from the CRT gun. This is attached to the chassis immediately above the gun.

d) Unplug the gun harness from the end of the CRT. Take care to to exert to much pressure on the tube itself.

e) Disconnect the two yoke cables (yellow/green and red/blue) from the video board by unplugging the two 6-pin connectors.

f) Pry the plastic cover up from the HT lead which connects to the side of the CRT. Press in one side of the connector under the cover to disengage and remove the lead.

g) The CRT tube itself is held in place by four screws, one at each corner of the tube. Prepare a cushioned area on which to place the tube upon removal. Remove the four screws with a 1/4" nutdriver.

g) The tube may then be lifted out of the chassis with the yoke assembly still connected.

The tube may be installed in the chassis in the reverse order to the above. Connect the gun cables with the CRT almost in place. Connect the HT lead and connectors to the video board after the tube has been screwed in place. Ensure that the correct yoke plugs are inserted in the corresponding sockets on the video board.

At all times, handle the tube with extreme care.

11.2.2 Deflection Yoke

Access to the deflection yoke is performed in a manner identical to the CRT tube. Once the tube has been removed from the chassis by following the steps in Subsection 11.2.1, the deflection yoke may be slid off the rear of the CRT tube by loosening the clamping screw.

Reassembly is performed in the reverse order.

Readjustment of picture orientation by means of the video board controls may be necessary if this component has been changed.

11.2.3 Video Board

Access to the video board is performed first by removing the CRT tube, as outlined in Subsection 11.2.1. The procedure is then continued as follows:

a) Disconnect the cabling to the flyback transformer from connector P3 on the video board.

b) Release the gun cable from the two cable tiedowns.

c) Use a Phillips screwdriver to remove the screws that hold the top of the video board onto the rear wall of the CRT enclosure.

d) The board may now be removed from the connector on its lower edge and removed from the system.

Replacement of the video board is performed by following the reverse order.

A new video board will not have the correct adjustments for contrast and focus. These should be adjusted after the system is reassembled and operational by means of the controls at the rear of the power supply until the picture is of acceptable quality.

Picture size and centering may be required after replacement of a video board. This is done by controls on the board itself.

11.2.4 Flyback Transformer

The flyback transformer is attached to the floor of the tube enclosure. It is removed by performing the following steps:

a) Remove the CRT tube by following Subsection 11.2.1.

b) Disconnect the flyback transformer cable from P3 on the video board.

c) Remove the flyback transformer cable from any cable tiedowns.

d) Remove the bottom panel of the main LISA chassis by removing the six screws in the logic enclosure.

e) Remove the two 4-40 nuts underneath the chassis, taking care to hold the transformer to prevent it falling once these are removed

When replacing the assembly, ensure that the white HT lead is to the rear. Clip the bottom of the transformer at the front first and follow the disassembly procedure in the reverse order.

11.3 System Cabling

Due to the modular nature of the LISA logic electronics, the system interconnections within the LISA has been kept to a minimum. Interconnections fall into four categories:

* Power cabling
* Disk cabling
* Interface connections
* Logic connections

11.3.1 Power Cabling

Power is supplied to the LISA system through a normal three-wire wall connector and standard Apple power cable directly to a socket in the power supply assembly.

The power supply assembly in turn provides power to the system via an edge connector which mates into a plug in the CRT tube enclosure. This plug is part of the power cabling harness which distributes power to the following assemblies in the system:

* Motherboard
* Video board
* Speaker
* Cover interlock

The power cable harness is assembly 591-0003 on the LIsa product tree (Appendix H).

Should it become necessary to remove the power harness, the procedure in Subsection 11.2.1 must be followed to first remove the CRT tube. The following steps are then followed:

a) Remove the two screws that hold the video board connector to the wall of the CRT enclosure.

b) Remove the two screws that hold the power supply connector plug to the rear wall of the CRT enclosure. Hold on to the nuts.

c) Disconnect the speaker plug on the floor of the tube enclosure.

d) Remove the screw which holds the cover interlock to the chassis beside the speaker.

e) Remove the two screws that hold the motherboard connector to the wall of the logic board enclosure. Hold on to the nuts.

f) Remove any tiedowns holding the cabling to the chassis.

g) The harness may then be removed from the chassis.

Installation of a power cable harness is performed in the reverse order. Before installing any tiedowns, ensure that the cable is correctly positioned and that all connectors can reach their proper locations.

If difficulty is encountered mounting the motherboard connector, removal of the flyback transformer makes this connector more accessible.

Ensure that the ground connectors are correctly attached by one of the mounting screws for both the power supply and the video board connectors.

11.3.2 Disk Cabling

The dual floppy disk drives in the LISA are installed as a single unit in the right front of the chassis. They are connected to the system logic by means of flat ribbon cables, one for each drive.

The cable also provides the logic connection to the board which carries the power switch and the keyboard phone jack at the lower right front of the chassis.

To gain access to the cable, first remove the drive assembly 620-5107. Then all steps called for in Subsection 11.2.1 must be performed to remove the card cage, power supply and CRT.

The disk cable is then removed by performing the following:

a) Release the cable from the two tiedowns.

b) Unplug the connector to the switch board which contains the power switch and the keyboard jack.

c) Remove the two screws that hold the disk cable motherboard connector to the rear of the logic enclosure wall. Hold on to the nuts.

Installation is performed in the reverse order. Ensure that the cable has sufficient slack to allow the drives to be placed in front of the system with the cable attached.

11.3.3 Interface Connections

Interface cabling in the LISA consists exclusively of those connectors at the rear of the motherboard. No disassambly procedure is required here. It is however recommended that connections are made and broken with power off.

The interface connectors themselves are soldered to the motherboard and are not separately replaceable.

11.3.4 Logic Connections

All logic cabling in the LISA is made by means of edge connectors between logic cards, with the exception of the disk cable, described in Subsection 11.3.2 above. There is therefore no disassembly procedure.

11.4 Disk Drive Assembly

The disk drive assembly is shown as subassembly 620-5107 in Appendix H. It consists of the following components:

* Drive carrier 805-4014
* Drive carrier shelf 805-4013
* Upper disk drive xxx-xxxx
* Lower disk drive xxx-xxxx

There is no difference between the upper and lower drives. They are distinguished logically by the connections made by the two plugs on the disk drive cable.

To remove the bottom drive, remove the four 6-32 Phillips screws on the under surface of the assembly and slide the drive out.

To remove the top drive, remove the six 6-32 Phillips screws which hold the drive carrier shelf in the middle of the assembly (three on each side). The shelf and top drive can than be slid out of the assembly. The shelf is detached by removal of the four screws on the underside.

11.5 Miscellaneous

The following assemblies are present in the chassis in addition to those covered in the Owner's Guide and the preceding sections. These are:

* Speaker assembly
* Power switch assembly
* Motherboard assembly
* Chassis assemblies

11.5.1 Speaker Assembly

The speaker is located on the floor of the CRT tube enclosure. In order to remove it, it is necessary to remove the CRT, as described in Subsection 11.2.1. Then the following procedure is followed:

a) Disconnect the speaker from the power cable harness by unplugging the plastic connector.

b) Remove the three screws holding the speaker to the chassis.

c) Remove the speaker.

The speaker may be installed by following the steps in the reverse order. It is shown as assembly 620-0001 on the LISA product tree.

11.5.2 Power Switch Board Assembly

The power switch board is located on the lower right of the front of the system. In order to remove the power switch board, the disk drive assembly must first be removed from the system. Then perform the following:

a) Unplug the disk cable from the connector on the switch board.

b) Use a long-reach Phillips screwdriver to remove the two screws which hold the board to the base of the chassis.

c) Remove the board.

Reassembly is performed in the reverse order.

11.5.3 Motherboard Assembly

The card cage assembly is shown as 620-51xx in the product tree. The "xx" is used to denote the size of the memory installed in the individual system.

The motherboard assembly is the carrier unit for all the logic cards in the system. It consists of the basic PCB with card edge connectors and interface connectors attached plus card guides and a metal frame.

The top of the expansion board card guides can be removed by removing the three Phillips screws which hold it to the top of the left-hand main card guide.

The card guides can be detached by removing the six 4-40 Phillips screws that hold the main card guide assembly in place. The two main card guides are attached to one another by three support bars, each of which is held at each end by a Phillips screw.

The metal motherboard frame can be detached from the motherboard itself by removing the fifteen 4-40 Phillips screws that hold the two together. Eight of the screws hold the interface connectors in place. The other seven hold the motherboard to the frame.

11.5.4 Chassis Assemblies

The assemblies which comprise the main chassis do not have disassembly procedures. They are:

* Chassis one 620-5106
* Chassis two 620-5116
* Back 620-5105
* Bezel 620-5111

11.6 Keyboard and Mouse

The keyboard and mouse are not part of the main LISA assembly as they are physically separate units. Both may be disassembled if the need arises.

11.6.1 Keyboard Assembly

The keyboard consists of a single PCB which carries all the keys sandwiched between two halves of the case.

To access the assembly, perform the following:

a) Disconnect the keyboard from the LISA by removing the keyboard jack from the plug at the lower right of the LISA chassis.

b) Using a Phillips screwdriver, remove the five plastic screws that hold the keyboard together.

c) Remove the keyboard PCB and place it on a flat surface.

Reassembly is performed in the reverse order. Care must be taken not to apply excessive torque to the threads of the plastic screws.

The keyboard cable is held in place by a Molex-type connector, which provides strain relief. This can be removed as required.

11.6.2 Mouse Assembly

The mouse is a stand-alone unit which has a few moving parts. To access the mouse assembly, disconnect its plug from the rear of the LISA and remove the three plastic screws on the underside which hold the body together.

APPENDIX A. TECHNICAL APPENDIX

OVERVIEW

The two ports on the board are electronically similar to the parallel port built into the Lisa system, so software driving the internal port can also drive the external parallel ports with little modification. There is also a ROM on the board which contains self-test diagnosic software as well as a program that allows Lisa to boot from peripherals attached to the ports.

TECHNICAL SPECIFICATIONS

- Two parallel interface ports
- Standard Apple parallel interface protocol
- 2K Bytes on-board ROM
- Allows system booting from port
- Self-test diagnostics
- 625K bytes/second maximum data transfer rate
- Port control based on 6522 Versatile Interface Adapters
- Supports several read/write handshake modes
- 4 programmable timers
- Interrupt capability
- Parity check on data lines
- Dimensions: 9.3" high x 5" wide x 0.7" deep (236mm x 127mm x 18mm)
- Power consumption: 1 Amp @ 5 Volts

ELECTRICAL DESCRIPTION

The parallel port electronics consist basically of two 6522 Versatile Interface Adapter (VIA) chips. Each VIA contains two 8-bit parallel ports, associated handshake signals, programmable timer/counter and shift register. See the 6522 data sheet for more information. One 6522 is dedicated to each parallel port.

The pin functions are as follows:

DD0-DD7 Eight bidirectional data lines. DD7 is the most significant bit.

RW Read/write. The Lisa drives this line high to indicate that it expects data to be input on the data lines. The Lisa drives this line low when there is data to output.

PARITY ~~Bidirectional~~ Input line which must be configured on the basis of data currently on the data lines to give odd parity.

PSTRB/ Processor strobe line used as a signal by the Lisa to indicate valid data being output or input.

CMD/ The Lisa asserts this line to indicate that a command has been placed on the data lines.

BSY/ The attached periperhal asserts this line to indicate that it is busy and unable to process commands on the interface. Used as an interrupt input.

OCD If this line is high, Lisa assumes no device is connected to the port.

CRES/ Lisa asserts this line to reset the peripheral to its power-on state.

CHK/ This signal may be used to interrupt the CPU in the event that a fault condition has occurred in the device connected to the port.

Table 1 shows the signals on the parallel port DB-25 connector and their respective connections to a 6522 chip. PBx corresponds to port B, bit x on a 6522 chip, and CAx and CBx are control input/output bits. See the 6522 data sheet for more information.

Signal	Pin	Port Connection
PSTRB	15	CA2
R/W	3	PB3
CMD	17	PB4
CHK	25	CB1
BSY	16	PB1,CA1
OCD	19	PB0
CRES (out)	21	PB7
CRES (in)	21	PB5
Reset Parity	--	PB5
Parity Latch	--	CB2

Table 1. Parallel Port Pin Assignments and Connections

SOFTWARE CONSIDERATIONS

See the 6522 data sheet for information regarding programming the 6522 chip registers and I/O ports. Basic port addresses are shown in Table 2; add 2000_H, 6000_H, or $A000_H$ to these addresses depending on whether the Parallel Board is in slot 1, 2, or 3 respectively. Note that these addresses are in system I/O space, as defined in the Lisa Hardware Reference Manual.

The built-in 2K byte ROM starts at 0, 4000_H, or 8000_H, depending on which slot is being used. The byte-wide ROM appears in the low (D0-D7) byte of each word.

Register	Reg #	Port A Address (Hex)	Port B Address (Hex)
ORB/IRB	0	0	800
ORA/IRA (w/hndshk)	1	09	809
DDRB	2	11	811
DDRA	3	19	819
T1C-L	4	21	821
T1C-H	5	29	829
T1L-L	6	31	831
T1L-H	7	39	839
T2C-L	8	41	841
T2C-H	9	49	849
SR	10	51	851
ACR	11	59	859
PCR	12	61	861
IFR	13	69	869
IER	14	71	871
ORA/IRA (no hndshk)	15	79	879

Table 2. 6522 Register Addresses

DIFFERENCES FROM LISA INTERNAL PORT

As mentioned above, both the Lisa and the Parallel Interface Board use 6522 VIAs to drive the parallel ports. However, there are a few minor differences that the programmer should note.

1. Timing. The Lisa parallel port is driven by a 500 kHz clock. The Parallel Board supports a faster clock operating at 1.25 MHz. This affects software using 6522 internal timers.

2. Port Connections. Software driving the Lisa internal port references signals through two 6522 chips (see the Lisa Hardware Reference Manual for more information). The Parallel Board connects signals for a single port in a single 6522.

GLOSSARY

Acknowledge A signal which is used during handshake operations to indicate that the current step has been completed.

Arithmetic Unit An optional peripheral device in LISA implemented by a dedicated device located on the I/O board. Its purpose is to free the CPU of tasks which involve considerable calculation.

Asserted A signal is said to be asserted when it is in a true state. This means that the term SIGNAL would be in a "high" or "1" state. The term SIGNAL/ would be in a "low" or "0" state if it is asserted.

Asynchronous modem A modem which handles asynchronous transmissions. In asynchronous communication, each character is transmitted with its own framing information telling the receiver where the character starts and stops. Since each character is a complete message, the time interval between successive characters need not be fixed.

Autovector To handle certain interrupts, the 68000 automatically jumps to a location predefined for the given interrupt. The jump to the interrupt handler preloaded at this location is called an autovector.

Battery Backup The LISA I/O board is equipped with rechargeable Nickel/Cadmium batteries. Whenever the LISA is disconnected from a power source, the COPS device continues to receive power from these batteries to allow it to provide a true Real Time Clock and also initiate software-controlled power-up.

Baud rate The rate at which a Modem sends and/or receives information. 110 baud means the Modem is handling approximately 110 bits per second. If there are two stop bits, a start bit, a parity bit, and a seven bit ASCII character code, 110 bits per second translates into about 10 characters per second.

Bit An acronym for binary digit. A bit is an

item of data with only two possible states, 1 or 0.

Bitslip A technique of data encoding on the LISA floppy disk whereby two zero bits are inserted between each byte written to the disk. This is quite separate from data encoding and is used for data synchronization.

Block A contiguous set of data in the system. It normally refers to a unit of data written to and read from disk (524 bytes). When referring to memory, it may be of any length, but all addresses of the block are contiguous.

Boot When a computer is turned on, it has to "bootstrap" itself into a useable state. The process of getting the operating system software into place and executing is called booting.

Buffer A logic device used as a bus driver, whether it had latch capability or not.

Bus A set of parallel wires (traces, paths) which carry related data and control information from one device to another.

Bus Timeout A feature of the LISA which permits the CPU to give peripherals a large amount of time in which to respond to a transfer request. If the peripheral does not respond to a cycle after approximately 30 microseconds, a bus timeout occurs and the CPU logs an error.

Byte A group of bits. On the Lisa, a byte is always 8 bits.

Byte parity When bytes of data are being moved around, one or more bits in the byte can get improperly flipped. These incorrect bits can sometimes be detected by checking the byte parity. The byte's parity is odd if there is an odd number of 1 bits in the byte. If another bit is available in the byte, the sender can insure that every byte has even parity upon being transmitted. The receiver can then check each byte's parity, and if any are odd, it can inform the system that something has gone wrong.

Calc/Check Refers to the two modes in which the MMU may find itself. During calculation, the physical address of the page being accessed is calculated. During check, the validity of the access is

checked.

Card cage The metal frame in which the printed circuit boards reside.

Checksum Similar to byte parity. A number used to ensure that data has not suffered degradation during transfer. A checksum is usually generated by addition of all the bytes in a block in a certain pattern. It is written at the end of blocks of data written to disk on the LISA.

Clock A continuous, regular waveform used to control the timing of logic decisions.

CMOS Complementary Metal Oxide Semiconductor. CMOS combines N-channel and P-channel MOS transistors to give rather high speed operation, good noise rejection, low power consumption, and large fan-out. Since the non-volatile parameter memory must not consume much power, it is implemented with CMOS chips.

Context The LISA system is configured to operate in one of four contexts. Each context has a complete set of 128 pairs of registers within the MMU. The operating system normally executes in context 0. Switching between programs can be quickly done simply be changing context.

COPS Control Oriented Processor System. In the LISA, this slave processor is used as a controller at both ends of the keyboard interface.

Counter A logic device which sequentially increments or decrements each time a clocking pulse occurs.

CPU Central Processing Unit: Motorola 68000 16-bit general-purpose device in the case of the LISA.

CVSD Continuously Variable Slope Delta Modulator: type of analog to digital and digital to analog converter.

Cycle The interval between the same phase position of two adjacent clock pulses.

Daisy chain A daisy chain is a method of connecting several devices to a single I/O port. All devices share the same signal lines and are usually

selected by means of an addressing cycle on the bus.

Deasserted A signal is considered deasserted when it is in a false state. This means that the term SIGNAL would be deasserted if it is "low" or "0". The term SIGNAL/ is deasserted if it is "high" or "1".

Decode The opposite of a select. The decoder's input address determines which of its many outputs be asserted.

Disable A term used to mean holding any signal in a deasserted state, irrespective of other inputs.

DMA Direct Memory Access. Normal memory access goes through the 68000 and its memory manager. A device can, however, read and write memory locations directly, without any intervention from the CPU.

Driver A logic device capable of driving signals which have a large electrical load, such as occurs on a bus.

D/A Digital to Analog. When a digital signal is used to control an analog device, the bits in the digital word must be converted into analog voltage levels.

ECC Error Correction Code. Used in memory storage as a method to regenerate erroneous data bits which have occurred in memory storage. Not yet implemented on LISA.

Edge Detector Logic which is capable of detecting a signal transition high-to-low or low-to-high.

Enable A term used to mean either allowing a signal to respond to its gating inputs or the act of gating data into a further stage of the logic.

Expansion Bus In the LISA, this refers to the signal subset of the internal system bus which is made available on three card slots in the chassis for the addition of other logic components.

FIFO First In First Out: device used to transmit data between interfaces at an asynchronous rate. The storage RAM in the disk controller in LISA operates in this fashion when

transferring data to and from floppy disk.

Flag — A status bit which indicates the occurrence of some condition in the LISA. It is usually available for interrogation by the CPU.

Flip flop — A digital circuit used to store one bit of data. There are variants on the basic theme but generally, the state changes synchronously with a clock edge, depending on the input state. Also known as "flop" and "FF".

Format — An exact description of the sequence of bits as they are organized on a disk.

Gate — A gate is a switch which controls the flow of data according to some Boolean function of its inputs. An AND gate, for instance, has two inputs, a data line and a control line. If the control line deasserted, data from the input line cannot get to the output. If the control line is asserted, any data on the data line is allowed to pass through the gate.

Gobyte — The flag byte used to tell the FD controller that the CPU wishes to have a macro instruction executed.

Handshake — Handshaking controls the transfer of data between devices. Each device has a way to tell the other that its side of the operation is complete. For example, a processor writes data to a register, then sends a signal to a device that data is ready to be read. The device reads the data, then sends the processor a signal that it has finished reading and is ready for more. The handshaking insures that the processor does not write new data to the register (destroying the old data) before the device has had a chance to read the old data.

Hang — A computer hangs when it gets into some infinite loop or wait state. If the operating system is unable to recover from this, the only recourse is to reboot the machine.

Hard disk — A disk that is not floppy. Higher data densities can be supported by a hard disk because it does not change size and position as much as the floppy disk does.

Hard error — A non-recoverable error during access to the main memory.

Header The series of bytes at the beginning of a sector on disk which identifies the sector.

Hexadecimal The number system used within LISA. The digits in this base-16 system are 0-9 and A-F. All addresses and data are expressed in terms of hexadecimal numbers

High A voltage state. A high voltage can signify either true or false, depending on the logic being used.

Horizontal retrace
The period of time when the electron beam in the monitor screen is returning from the end of a line to begin the next.

KHz Kilo-Hertz: 1,000 cycles per second.

I/O Input/Output: generic term used to describe the peripheral system with which the CPU communicates with the outside world or with data storage other than main memory.

IOB Input/Output Block: block of memory used to control and communicate with the floppy disk controller.

Interrupt A method used by portions of the system to cause the CPU to suspend its current operation and establish what the portion of the system requires to have done.

Latch A register which contains data for a transient period of time. Usually it stores data until read.

LED Light Emitting Diode: semiconductor device that emits light when a small current passes through it.

Logical An expression used to describe the address space generated by the CPU. Since logical addresses are translated into physical addresses by the MMU, these are not physical addresses. They can therefore remain constant even if physical addresses change, provided the MMU is informed of the change.

Loop A part of a program which repeats itself indefinitely. It is normally used to wait for an

interrupt which provides a way out.

Low — A voltage state: low voltage can signify either true or false, depending on the logic being used.

ma — Milliampere: common measurement of current in a digital system.

Main memory. — A term which refers to the RAM located on the memory boards in LISA. It is used as memory storage by the CPU only and can vary in size installed from 256 Kbytes to 2 Mbytes.

Memory bus — The collection of signals which interface the memory boards with the processor board.

Map — A term used to mean the transformation of one addressing system into another. In the LISA, it is used to describe the process of logical addresses being converted into physical addresses.

Mask — A pattern of bits used to control the contents of a register. Mask bits need not be contiguous.

Matrix — A term used to describe the two-dimensional array of bits in memory.

MHz — Mega-Hertz: 1,000,000 cycles per second.

MMU — Memory Management Unit: hardware in the LISA which is used to provide a feature called relocation. This allows the CPU and therefore resident software to operate on logical addresses, which are translated into physical addresses by the MMU.

Modem — Modulator/Demodulator: to send digital data over a telephone line, the Modem transforms the bit patterns into a stream of modulations of a carrier signal. At the receiving end, the signal is demodulated to recover the data.

Motherboard — The printed circuit board whose main function is to provide interconnection between the other PCB's in the system.

Mouse — A device connected to the LISA system which is rolled across a flat surface to direct cursor movement on the screen.

ms Millisecond: 1/1000th of a second.

mV Millivolt: 1/1000th of a Volt.

Nested A software term which applies particularly to subroutines. It means that subroutines may themselves have subroutines. The number of times this may be repeated is called the degree of nesting.

N-key rollover Nearly all keyboard interfaces work by scanning the keys and forming a two dimensional matrix representation of the state of the keys. The logic involved can tell when two keys are being pressed simultaneously (rollover), but when three or more keys are held down, phantom keys can appear. (There are hidden paths through the logic array.) N-key rollover design adds a diode in series with every key switch to eliminate the hidden paths.

Nibble A set of bits smaller than a byte. On the Lisa, a nibble is 4 bits.

NMI Non-Maskable Interrupt. When the processor receives an interrupt, it usually checks a mask to see whether it should pass control to that interrupt's handler. A non-maskable interrupt is always honored.

ns Nanosecond. 1/1,000,000,000th (a billionth) of a second. Also abbreviated as nsec.

Oscillator A device which provides an accurate period. It is usually used in clock generation.

Page In the LISA, this is used to define a contiguous area of main memory which is 512 bytes long. A logical page is this size of area within the CPU's logical address space. A physical page is this size of area within the main memory.

Parameter memory
A non-volatile block of RAM set aside for such things as the system serial number, configuration data, and user-defined information.

Parity Parity is a function of the number of bits in a word which are high. If there are an even number, the word has even parity. Parity can be checked to insure that one bit in a word has not been incorrectly flipped during transmission.

PC Program Counter. A register within the CPU itself used to keep track of the next instruction to be executed after the current one is complete.

PIA Peripheral Interface Adapter. An LSI logic device which assists the CPU in interfacing to peripheral logic. On the LISA, Motorola 6522 VIA devices are used.

Pixel The smallest controllable unit of area on the CRT screen. It corresponds to one bit of video data and can only be on or off (black or white).

Port An I/O address location within I/O space. In general, any group of addresses within the same PIA is termed a port also.

Privilegeviolation The 68000 has two state of privilege, User and Supervisor. Certain instructions (RESET, for example) can occur only in supervisor state. An attempt to execute a privileged instruction from user state causes a privilege violation interrupt to be generated.

PROM Programmable Read Only Memory. This refers to the fact that the device can be programmed after it has been fabricated. It is not usually alterable while it is within a computer system.

RAM Random Access Memory (actually ROM is also random access memory--RAM, however, is read/write memory).

Real Time Clock A function implemented on the LISA I/O board by the COPS device. Since power is always available to this device, it is used to calculate the real elapsed time at all times. This is available to software for interrogation.

Refresh The operation whereby the dynamic RAM's used for data storage are refreshed with the data they contain.

Relocation The technique implemented in the LISA MMU to map the logical address space used by the CPU into the physical address space which reflects the actual configuration of the LISA system.

Retry The act of repeating the execution of an instruction or routine in an attempt to avoid an error result. Used most frequently on disk access.

Return Address A software term for the address at which program execution will resume upon completion of a subroutine.

Rezero A technique of establishing absolute track position of the disk heads be returning to a known position.

ROM Read Only Memory. Consists of memory devices which are fabricated with a program already present. The contents cannot be altered.

RS232-C This refers to an interface standard which defines a bit-serial interface for use in conjunction with a modem, plus a corresponding communication protocol.

RWTS Read/Write/Track/Sector. This refers to the controlling routines that drive the floppy disk in the LISA. The RWTS is that part of the FD controller's resident program which interrupts the CPU upon completion since it involves actual disk control.

Schematic A drawing which represents the logical interconnections within a piece of hardware. Also known as a logic diagram.

Sector — The smallest addressable portion of a disk. Each track normally contains several segments.

Seek — The act of moving the heads across the disk surface to position them above a particular track.

Segment — A segment is an area of the system address space. It is the main unit of memory dealt with by the MMU. A logical segment is a contiguous block of 128 Kbytes in the CPU addressing space (logical address space). It consists of 256 logical pages. A physical segment consists of between 1 and 256 physical pages, depending on the size allocated to it by software via the MMU. Each logical segment has a corresponding physical segment. There are 128 of each in LISA.

Sense — The operation of interrogating status.

Shared Memory — An area of memory that can be accessed by more than one processor. In the LISA, the disk controller storage area is shared between the 6504 slave processor and the CPU.

Shift register — A register is a device which can store information. A shift register is able to shift all its bits left or right.

Slave — Hardware that is dependent on another section of hardware for instructions.

Slot — A term used to refer to one of the three expansion slots available in LISA.

SLR — Segment Limit Register. One of the registers within the four sets of 128 such registers contained in the MMU. It is used to define both the size of the physical segment being accessed in 1 page increments and the type of storage being accessed.

SOR — Segment Origin Register. One of the registers within the four sets of 128 such registers contained in the MMU. It is used to define the lowest address of the physical segment being accessed in terms of pages from the lowest address in memory.

Speed — In this context refers to the rotational speed of a disk.

SSP Supervisor Stack Pointer. This is a register in the CPU used to keep track of the return addresses for subroutines in Supervisor mode. See also Privilege violation.

Stack A software term that refers to the area of memory used to store return addresses from subroutines.

Standby Refers to the power available from the system battery when all other power sources have been disconnected.

State Machine A collection of logic devices capable of executing a very simple series of steps sequentially. It is the simplest form of computer.

Status An array of bits which is available to the CPU to inform it of the state of certain portions of the LISA.

Strobe A signal used to indicate that data is being transferred for the time that the strobe signal is asserted.

Subroutine Any portion of a program which is executed within the body of another portion of program although it would not normally be sequentially accessed in the order executed. Subroutines may be nested.

Sync A synchronization signal which permits other signals to assume a known state at a known time.

Synchronous Modem
Synchronous transmission puts the framing information around a group of characters. The transmitter then automatically inserts fill characters into the stream whenever necessary to maintain synchronicity. Because more of the bits are data (there are fewer stop and start bits than in asynchronous transmission), data transfers can go at a faster rate.

System Bus The main bus within LISA that is used to communicate between the processor and I/O boards. A subset of it extends to the expansion slots and is called the expansion bus.

Tristate A logic output that can be inactive, asserted or deasserted. These three states may also be termed active high, active low, and open.

TTL Transistor-Transistor Logic. The most common type of digital device in the LISA. A logic "high" is usually over 3.5V and a logic "low" usually below 1V.

Vertical Retrace The period of time during which the electron beam in the monitor is returned from the bottom of the screen to the top.

VIA Versatile Interface Adapter: name used by Motorola for the 6522 peripheral port control devices.

Video A term used generally to describe items that have to do with the monitor screen and its control circuitry.

Word A group of bytes. On the Lisa, a word is usually 16 bits, or two bytes. Long Words are 32 bits or four bytes.

Write Protect An operation which inhibits any writing operation to the item protected. This technique can be used for both memory and disks.

Yoke The control windings on the CRT tube which are used to control the amount of beam deflection.

ZIF Zero Insertion Force. This refers to the type of connectors used for the three expansion slots in the LISA. Since the slots are accessed from the side, a locking device is used to open the connector and permit the PCB's to be slid in from the side of the connector before being locked in place.