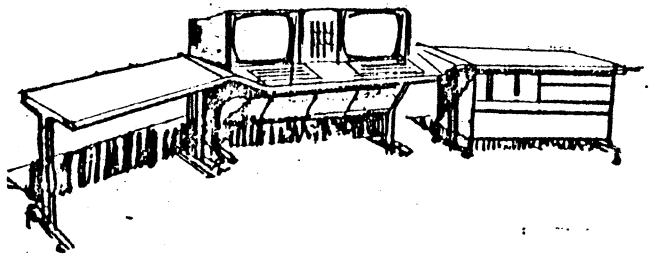
OSLO TECHNICAL UPDATE

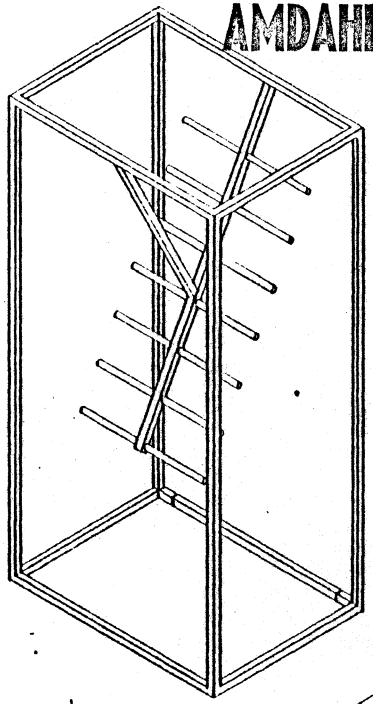
AUGUST 7, 1979

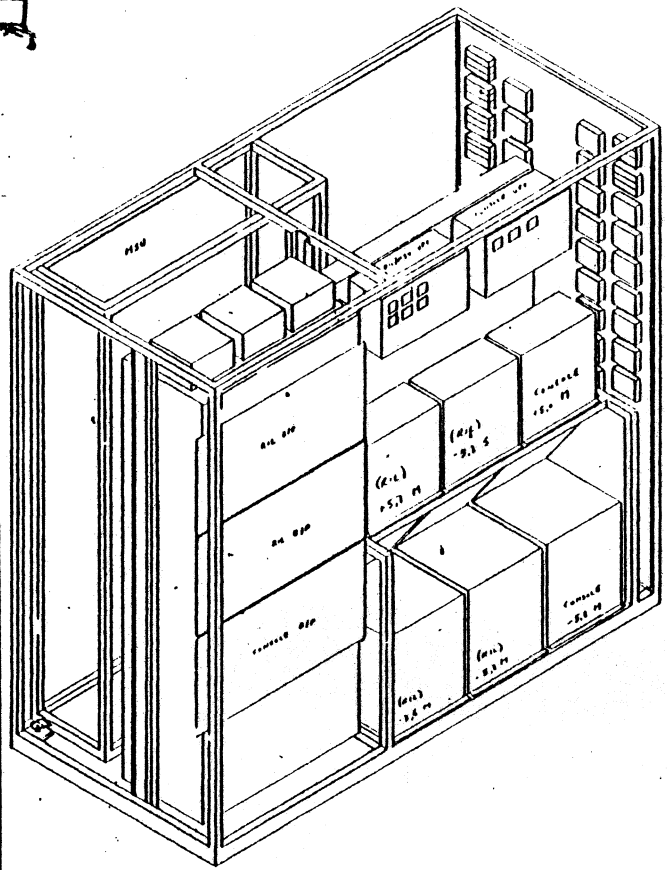
AGENDA

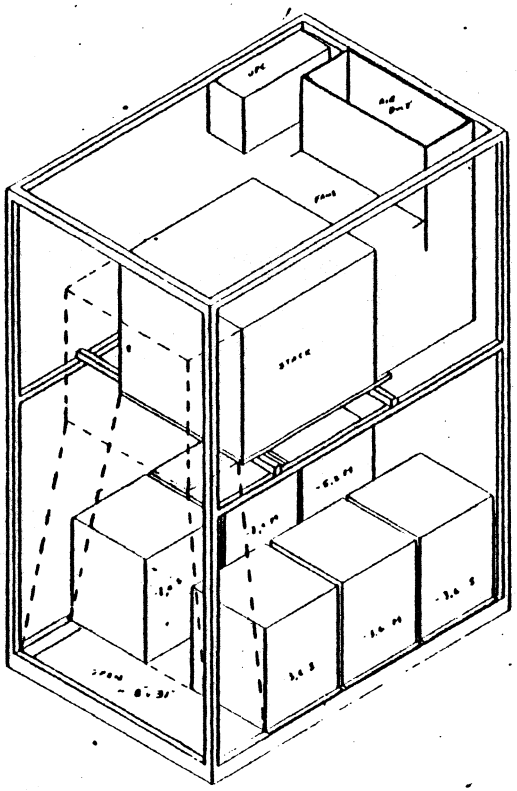
INTRODUCTION	R. LARSEN
I-UNIT	M. BEGLEY
E-UNIT	S. LEE
CPU PERFORMANCE	M. BEGLEY S. RAWLINSON
S-UNIT/BUFFER	G. WOFFINDEN
MBC/MAINSTORE	R. KREUZENSTEIN
IOP	D. COOK
CONSOLE	P. DAWSON R. ZIMMERMAN

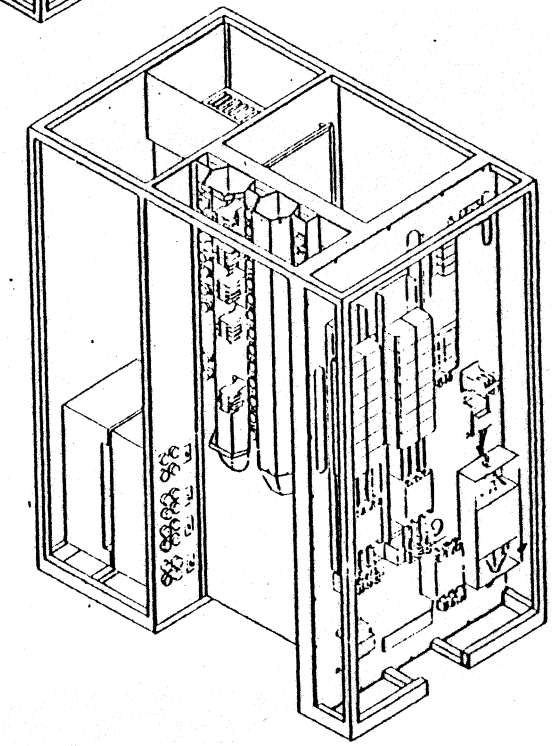
AMDAHL COMPANY PRIVATE











OSLO UNI-PROCESSOR CONCEPT

STACK PARTITION

- 10 MCC'S CONTAIN ALL LSI
  - 5 CPU
    - 1 I-UNIT
    - 1 E-UNIT
    - 1 S-UNIT
    - 2 BUFFER
  - 2 IOP
  - 1 CONSOLE
  - 1 MAINSTORE/BUS CONTROL
  - 1 HARDWARE MEASUREMENT INTERFACE
- 1400 STACK I/O
  - 1100 NON-LSI
  - 300 MP

NON-LSI

- STORAGE ARRAYS
  - MAINSTORE
  - CONSOLE MEMORY
- INTERFACES
  - CHANNELS
  - CONSOLE PERIPHERALS
  - DIRECT CONTROL
  - CHANNEL TO CHANNEL ADAPTERS
- OSCILLATORS

LSI AND RAM USAGE

	P/N'S	NO. LSI	NO. RAM'S	TOTAL CHIPS
E-UNIT	43	89	18	107
I-UNIT	54	90	18	108
S-UNIT	33	70	29	99
BUFFER	9	43	75	118
MBC	31	77	29	106
IOP	28	75	43	118
CONSOLE	10	59	42	101
INT. HANDLE. (18/SYSTEM)	7	162 (9/CHANNEL)	18 (1/CHANNEL)	180
TOTALS	215	665	272	937
BRING UP	2	16	0	16

AMDAHL COMPANY PRIVATE

amdahl OSLO CHIP RELEASE

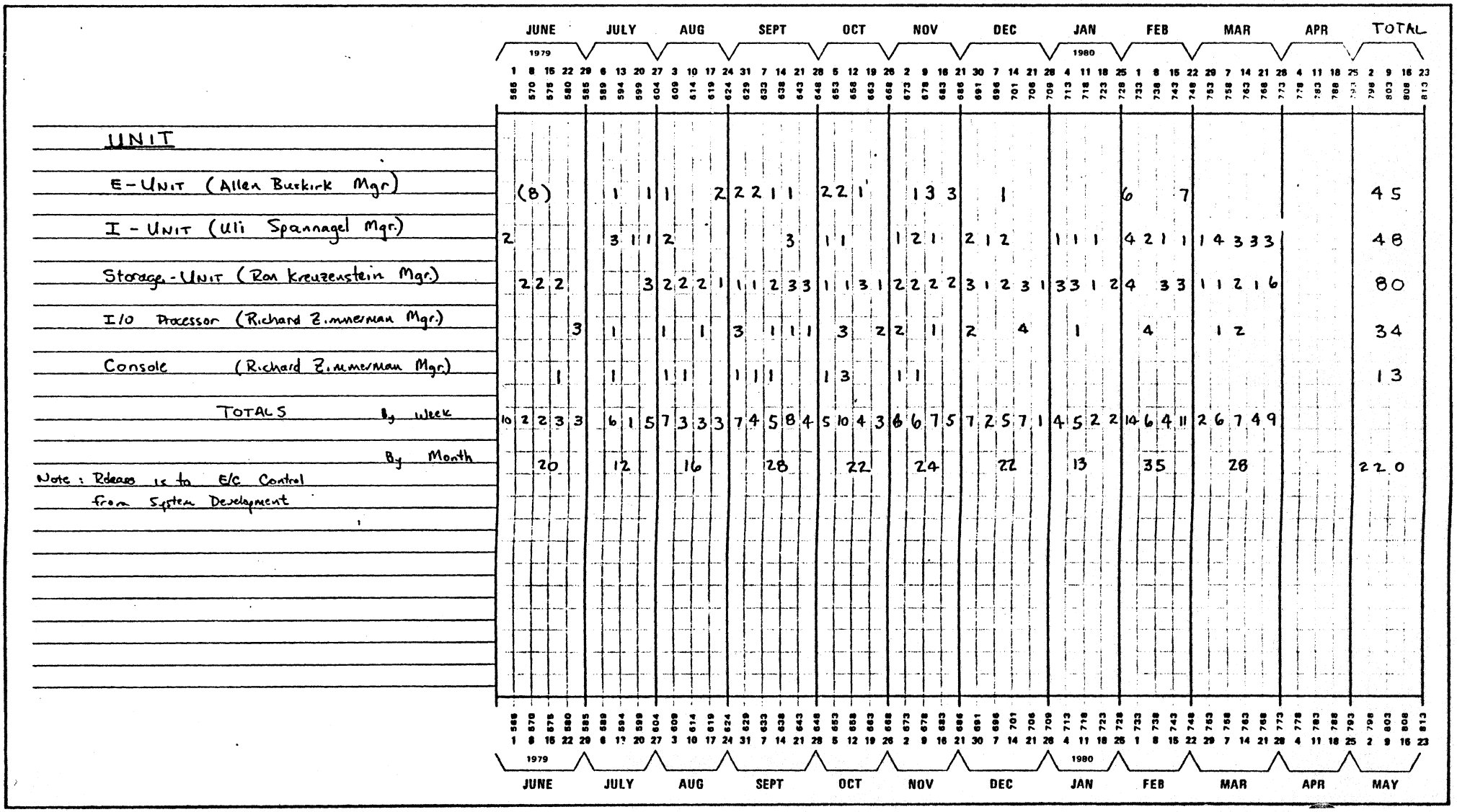
JUNE '79 THROUGH MAY '80

Revision B 7/12/79

System Development

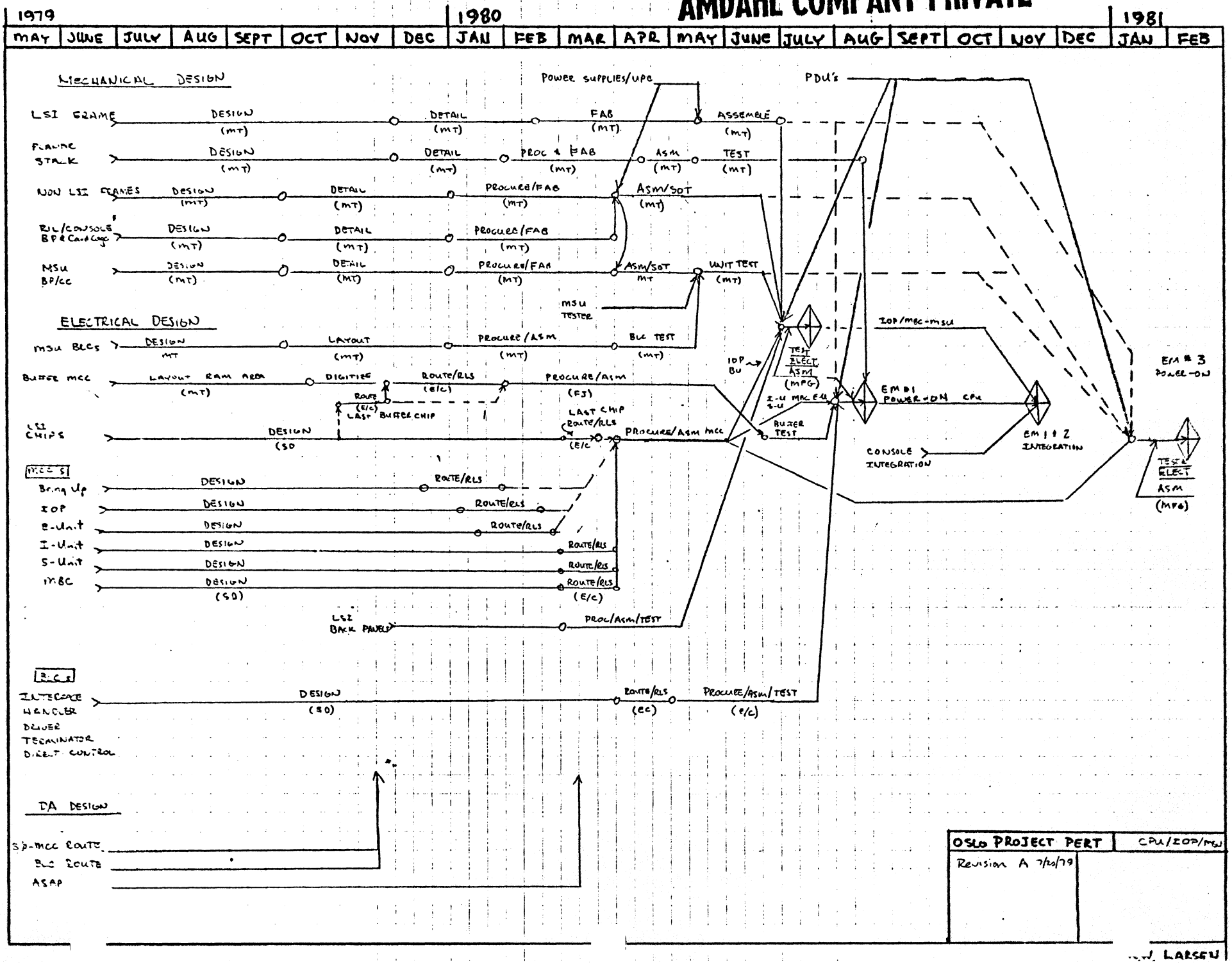
MANAGER Reed Larsen

FOR AMDAHL USE ONLY



AM 1486 (Rev 8/79)

AMDAHL COMPANY PRIVATE



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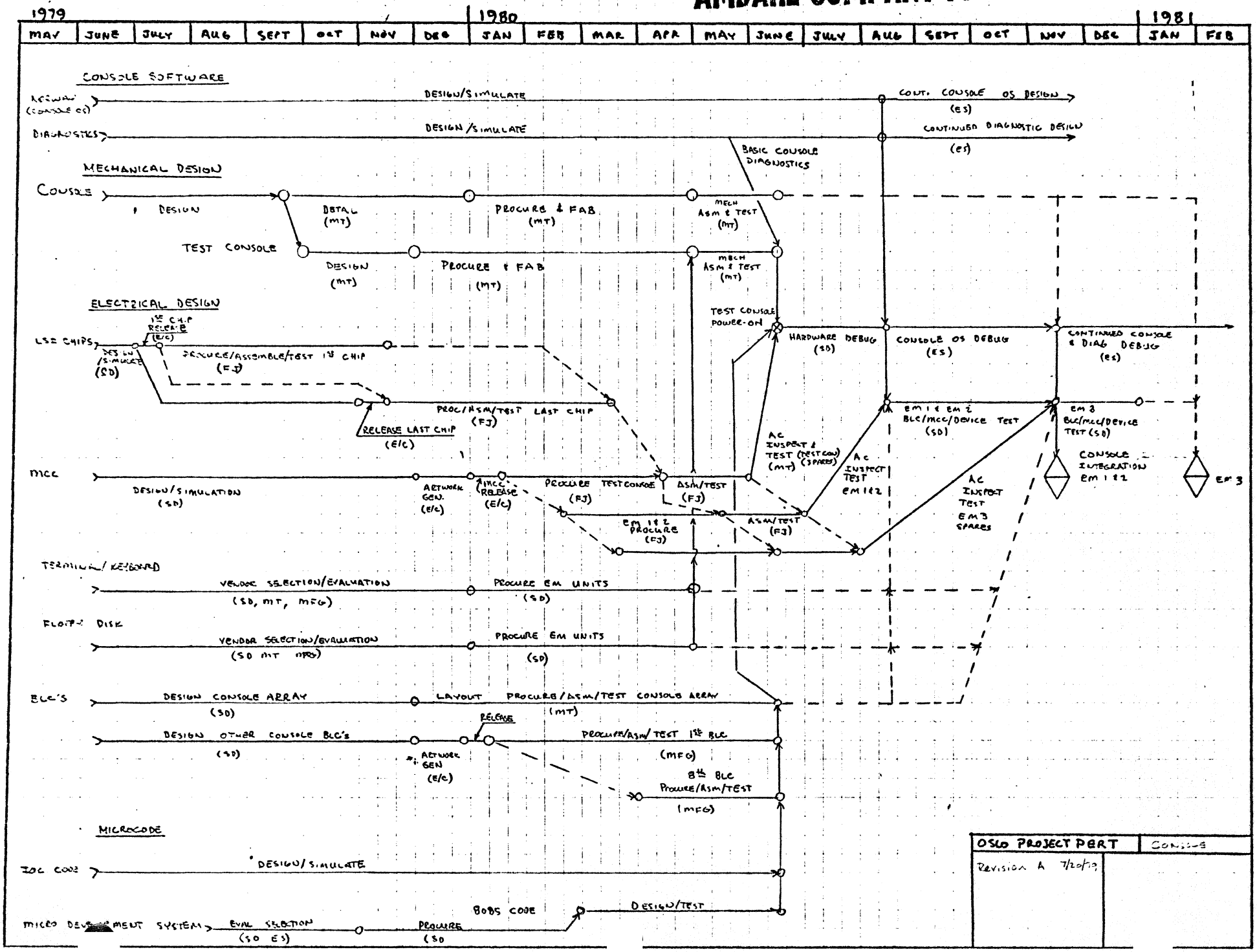
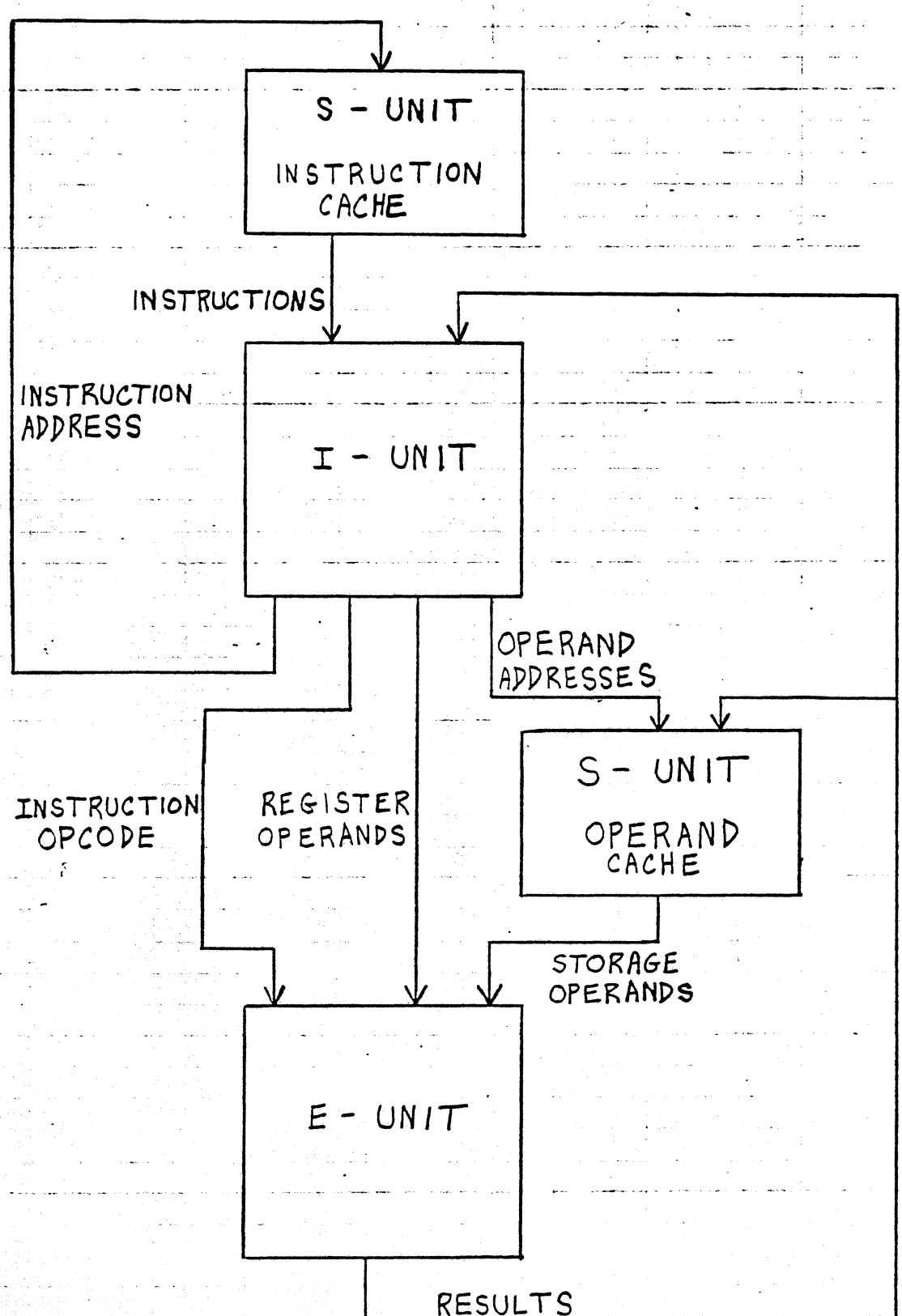
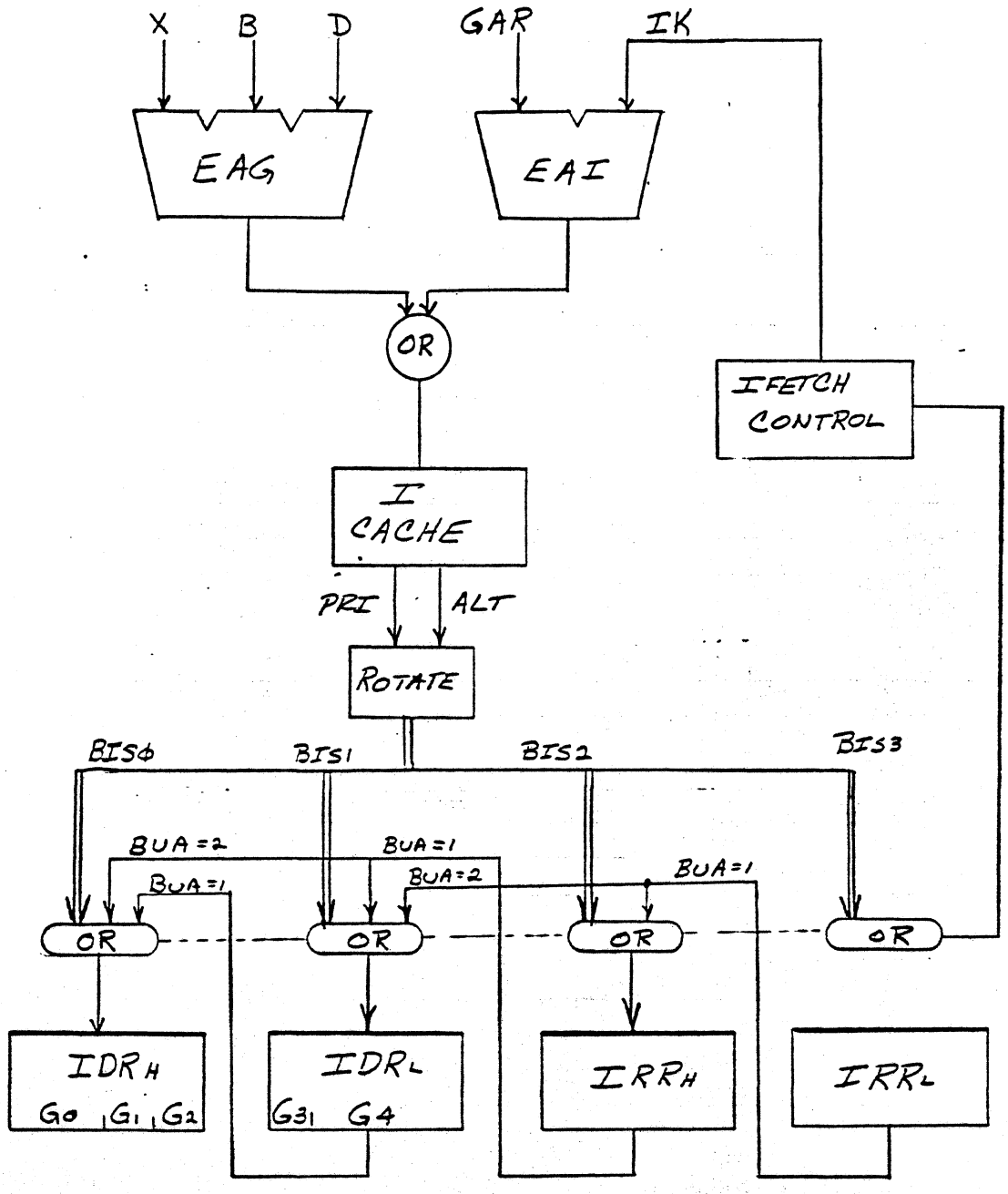


OSLO - INSTRUCTION UNIT

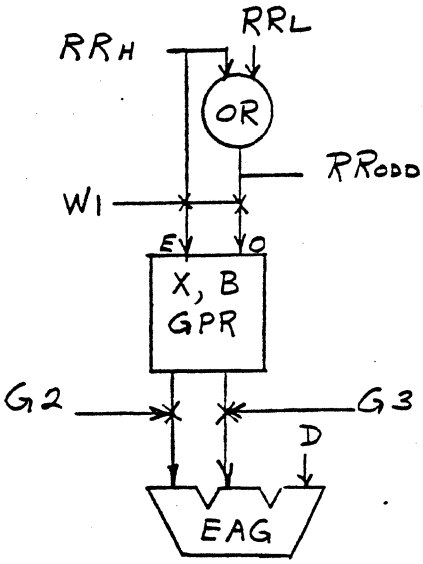
- INTRODUCTION
- IFETCH
- I-UNIT DATA FLOW
- EAG
- CONTROL STORE DATA FLOW
- CONTROL STORE WORD FORMAT
- CURRENT STATUS
- REMAINING TASKS

BLOCK DIAGRAM OF CPU



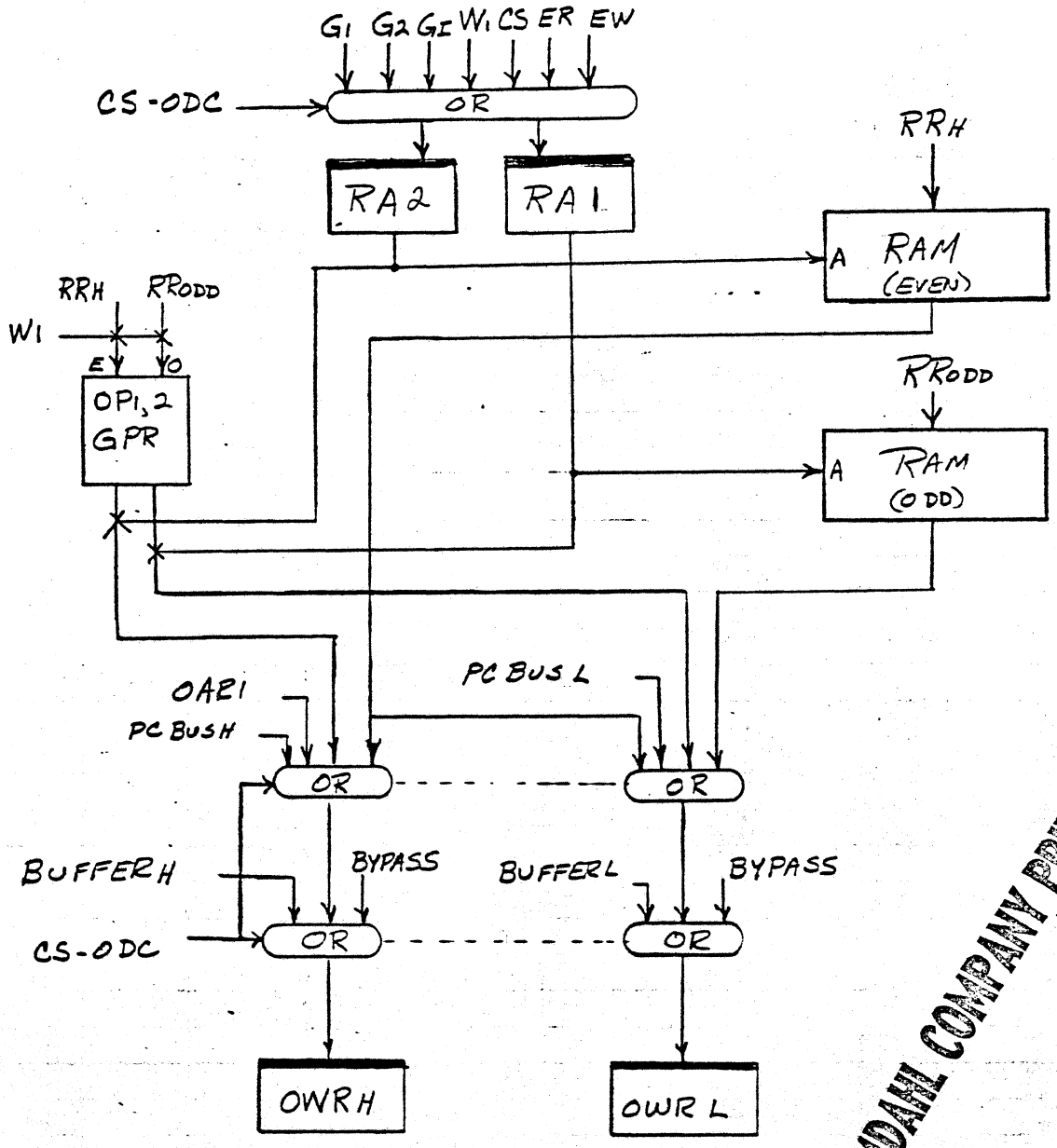


INSTRUCTION FETCH



RAM CONTENTS

- CONTROL REGISTERS
- SYSTEM REGISTERS
- FLOATING PT REGS
- SCRATCH REGISTERS
- USER GPRS (COPY)
- SYSTEM GPRS (COPY)



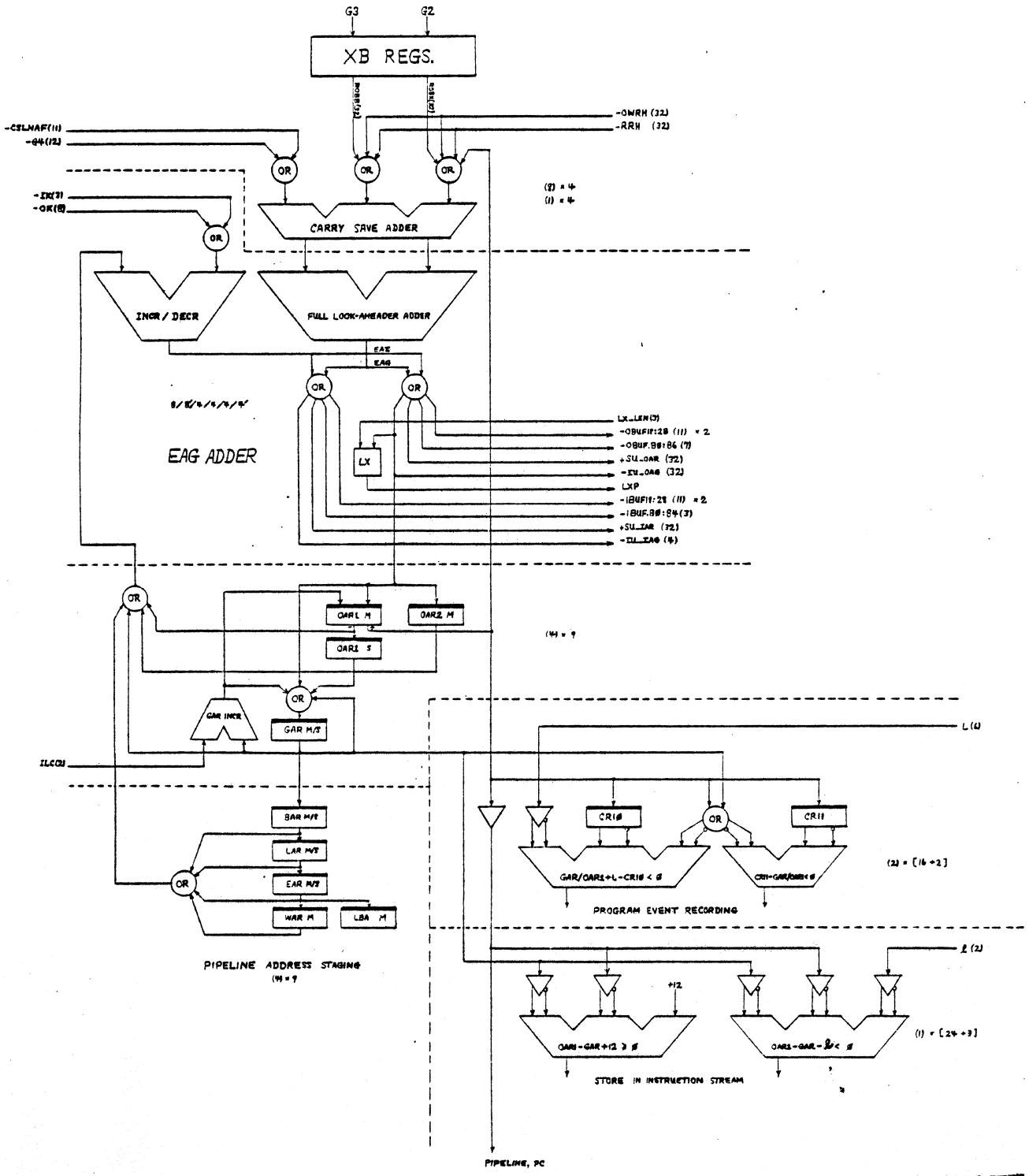
I-UNIT DATA FLOW

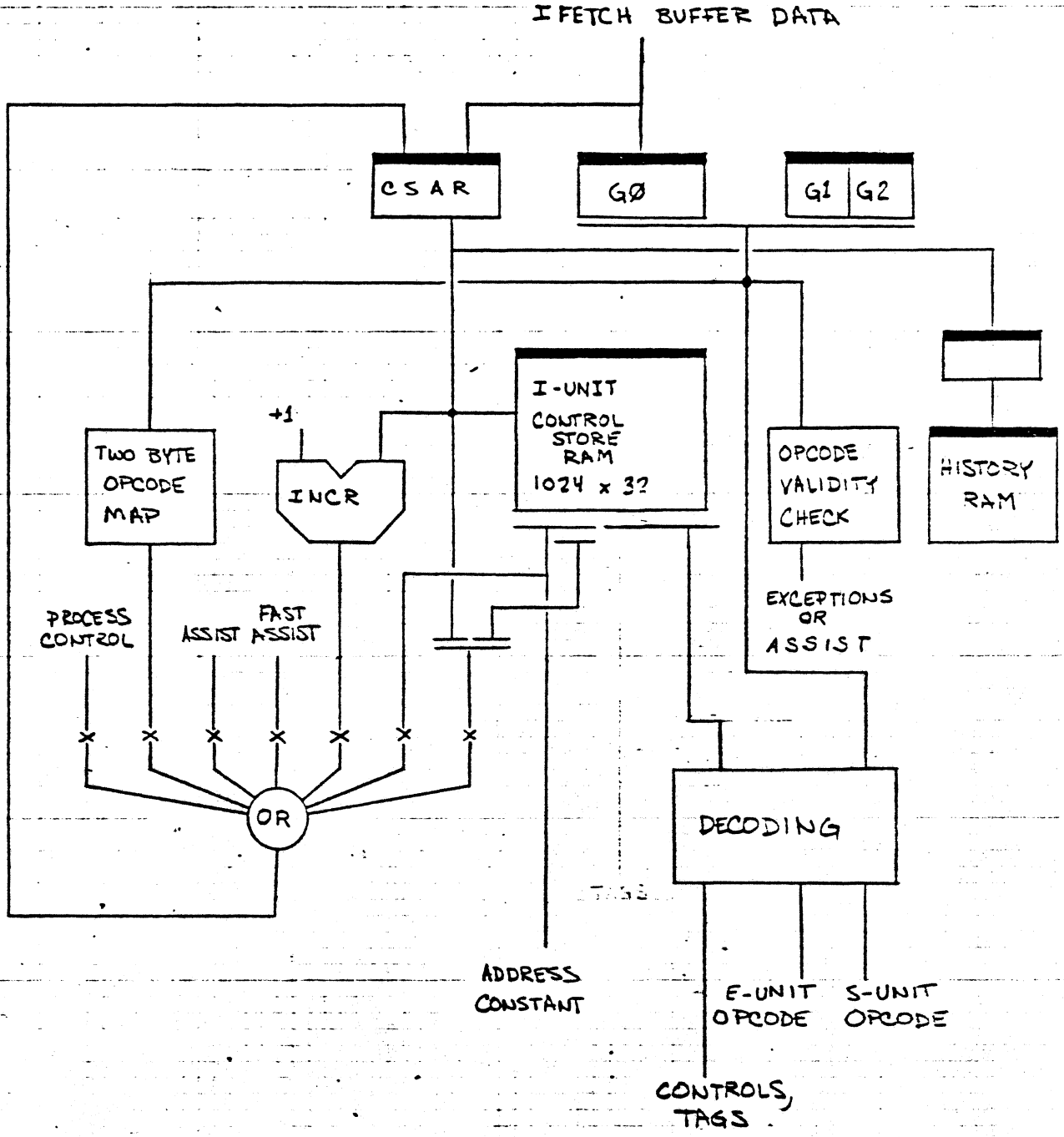
OPERAND REGISTER ORGANIZATION

- OPERAND REGISTERS ONE MONTH AGO
  - TWO COPIES OF ALL OPERAND REGISTERS IN RAM'S FOR OPERAND 1 AND 2 ACCESSES
  - CAPABLE OF READING AND WRITING RAM'S IN ONE CYCLE
  - PROBLEM: 27 NSEC RAM CYCLE TIME
- OPERAND REGISTER DESIGN CHANGE
  - READ OR WRITE RAM'S IN ONE CYCLE. THIS MEANS A RAM WRITE WILL DELAY RAM READS OF A FOLLOWING INSTRUCTION.
  - NEW SET OF 16 LSI GPR'S TO AVOID RAM READ DELAYS DURING GPR READS
  - RAM'S ORGANIZED TO ALLOW READING OR WRITING A DOUBLEWORD PAIR OF REGISTERS
- PERFORMANCE IMPACT OF DESIGN CHANGE
  - CR, SR: VERY LITTLE IMPACT, INFREQUENTLY ACCESSED
  - GPR: NO IMPACT DUE TO NEW LSI COPIES
  - FPR: 2% DEGRADATION IN SCIENTIFIC SHORT MIXES
    .5% DEGRADATION IN SCIENTIFIC LONG MIXES
  - SCR: VERY LITTLE IMPACT
    SOME E-UNIT ALGORITHMS WERE MODIFIED

OSLO EAG DATAFLOW

5/31/79





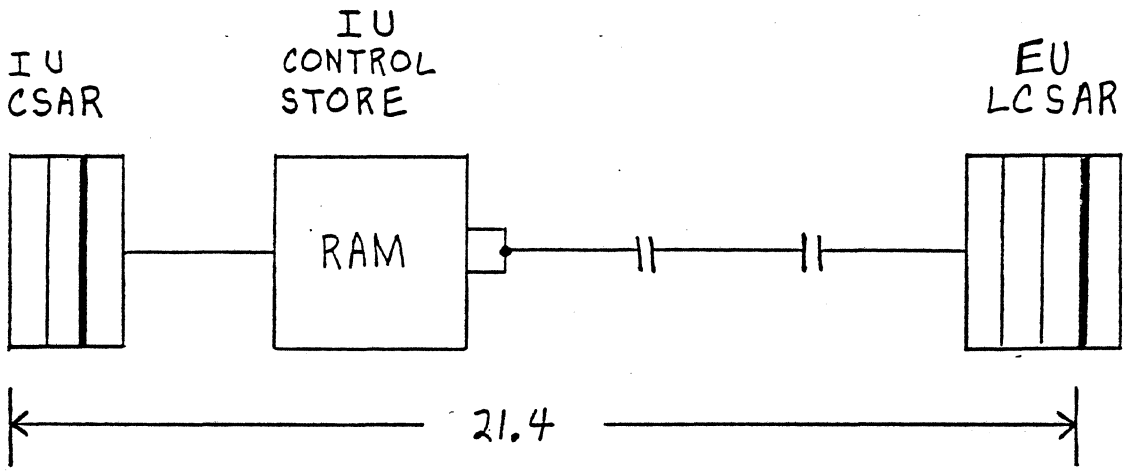
I UNIT CONTROL STORE

JRE 7/26/79

I-UNIT CONTROL STORE WORD

FIELD WIDTH	FIELD USAGE
4	NEXT G CYCLE CONTROL - SELECTS EAG INGATTING - SELECTS OAR INGATING
4	OPERAND DATA CONTROL - SELECTS OPERAND REGISTER ADDRESSES - SELECTS OWR INGATING - SPECIFIES REGISTER ACCESS TAGS - SPECIFIES DOUBLE TAG
5	E-UNIT AND S-UNIT OPCODE SELECTION - SPECIFIES THE OPCODES TO THE E AND S UNITS - STORE TAG
5	PIPELINE TAGS - WRITE TAG - CONDITION CODE SETTER (CCS) TAG - LAST PIPELINE SEQUENCE (LPS) TAG - RE INSTRUCTION FETCH - MULTIPLE E-CYCLE TAG - SET SCRATCH REGISTER INTERLOCK
12	NEXT ADDRESS FIELD - SELECTS NEXT CONTROL WORD - CAN BE USED TO LOAD FUNCTION NUMBER - SELECTS BETWEEN NORMAL & FAST ASSIST - USED AS A MEMORY ADDRESS - USED AS A REGISTER ADDRESS
2	PARITY

CONTROL STORE E UNIT OPCODE TIMING



LSI DELAYS

IU CSAR	3.379	
EU CSAR	3.973	
	7.352	7.352

RAM DELAYS

RAM IN	2.149	
DEVICE	7.200	
RAM OUT	1.578	
	10.927	10.927

WIRE DELAYS

IUCS ADDRESS	1.020	
IUCS DATA		
IU MCC	525	
BACKPANEL	378	
EU MCC	1.181	
	3.104	3.104

TOTAL PATH DELAY 21.383 N SEC

CURRENT STATUS

- ALGORITHM DEFINITION - 95% COMPLETE
- INITIATED ALGORITHM ANALYSIS AND ASSEMBLY
- COMPLETED PARTITION OF
  - IFETCH
  - EAG
  - GPR
  - CONTROL STORE
  - PROCESS CONTROL
- RELEASED CHIPS TO E/C CONTROL
  - IFETCH (2)
  - EAG (4)
  - GPR (2)
  - CONTROL STORE (1)

OSLO I-UNIT CHIPS

SECTION	CHIP DESCRIPTION	USAGE	STATUS
IFETCH	IFETCH DATA	8	RELEASED
	IFETCH STATUS	1	RELEASED
	IFETCH CONTROL #1	1	IN DESIGN
	IFETCH CONTROL #2	1	IN DESIGN
EAG	EAG 8 BIT A	1	RELEASED
	EAG 8 BIT B	1	RELEASED
	EAG 4 BIT A	3	RELEASED
	EAG 4 BIT B	1	RELEASED
	EFF. ADDR REG	4	DA ENTRY
	INST. ADDR REG	4	SIZED
	IFETCH-STORE PER	2	SIZED
	STORE IN INST STREAM	1	SIZED
DATA FLOW	X, B GPR & CSA DATA	8	RELEASED
	X, B GPR & CSA PARITY	1	RELEASED
	OPERAND 1, 2 REG ADDR	2	DA ENTRY
	REGISTER BYP - INLK #1	1	DA ENTRY
	REGISTER BYP - INLK #2	1	DA ENTRY
	OP GPR & DATA BUS #1	8	SIZED
	OP GPR & DATA BUS #2	4	SIZED
CONTROL STORE	CONTROL STORE ADDRESS	1	DA ENTRY
	CS SCAN POWERING	1	RELEASED
	CS ERROR CHECK & HISTORY	1	DA ENTRY
	CS OPCODE VALIDITY	1	SIZED
PIPELINE CONTROL	EAG CONTROL #1	1	-
	EAG CONTROL #2	1	-
	SEQUENTIAL CONTROL/ BRANCH #1	1	-
	SEQUENTIAL CONTROL/ BRANCH #2	1	-
	SEQUENTIAL CONTROL/ BRANCH #3	1	-
	INSTRUCTION STG #1	1	-
	INSTRUCTION STG #2	1	-

SECTION	CHIP DESCRIPTION	USAGE	STATUS
PIPELINE CONTROL	OPDECODE #1	1	-
	OPDECODE #2	1	-
	OPDECODE #3	1	-
	OPERAND LENGTH #1	1	-
	OPERAND LENGTH #2	1	-
	END FUNCTION ANALYSIS #1	1	-
	END FUNCTION ANALYSIS #2	1	-
	EU-SU INTERFACE #1	1	-
	EU-SU INTERFACE #2	1	-
	PROGRAM EXCEPTIONS	1	-
	CLOCK DISTRIBUTION	1	-
	HMI	1	-
PROCESS CONTROL	PC STATE CONTROL	1	SIZED
	INTERRUPT HANDLER	1	SIZED
	MACHINE CHECK	1	-
	IU ERROR DETECT	1	-
	PC DATA BUS #1	1	-
	PC DATA BUS #2	1	-

I-UNIT MCC

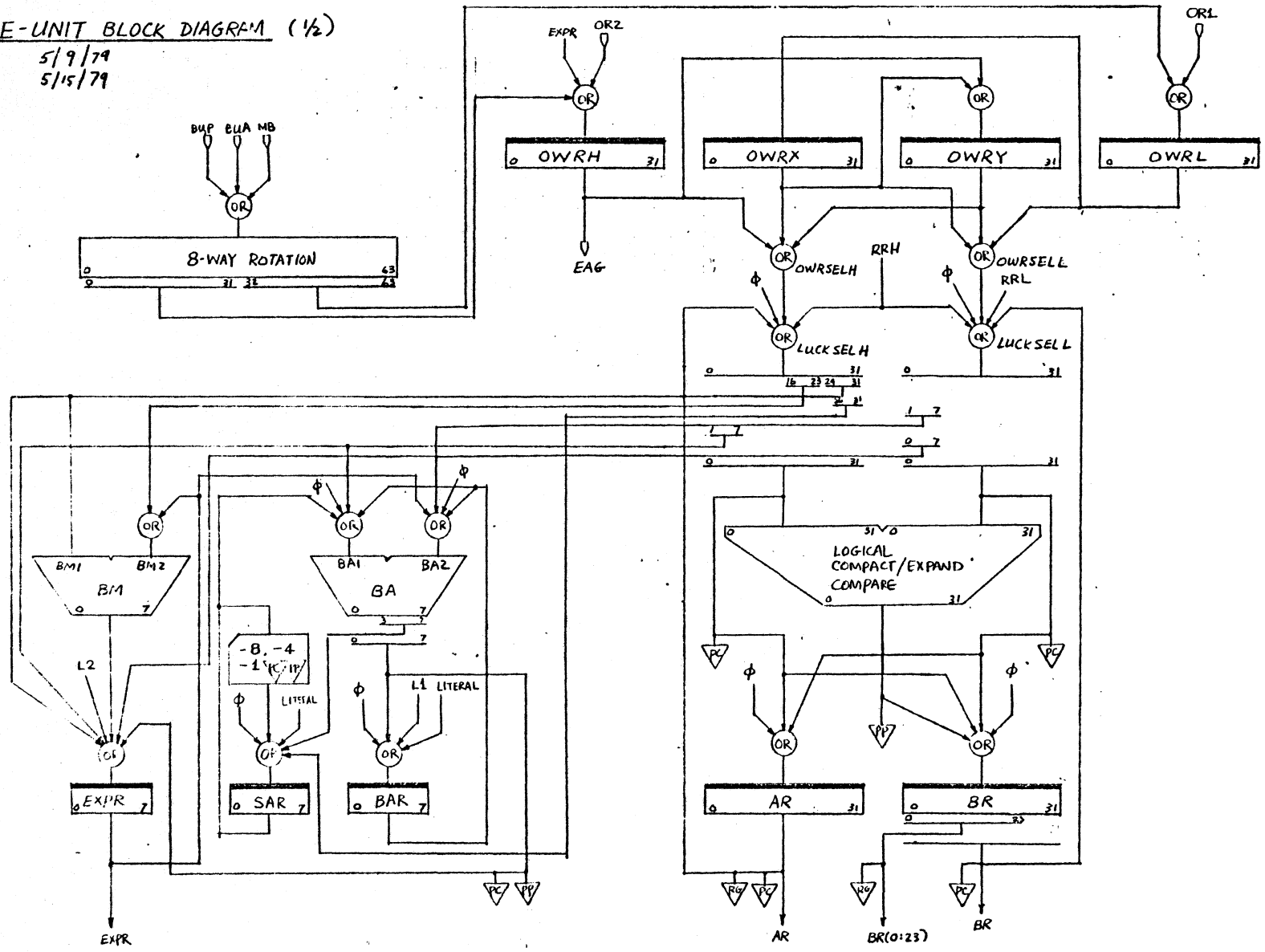
CHIP TYPE	P/N	TOTAL
LSI (IU)	50	84
LSI (SU)		6
RAM (IU)	-	14
RAM (SU)	-	4
		108
MCC I/O		704

REMAINING TASKS

- COMPLETE ALGORITHM DEFINITION AND ANALYSIS
- DEFINE CONTROL WORD FORMAT
- PARTITION PIPELINE CONTROL LOGIC
- DESIGN AND RELEASE REMAINING CHIPS
- PERFORM UNIT LEVEL SIMULATION

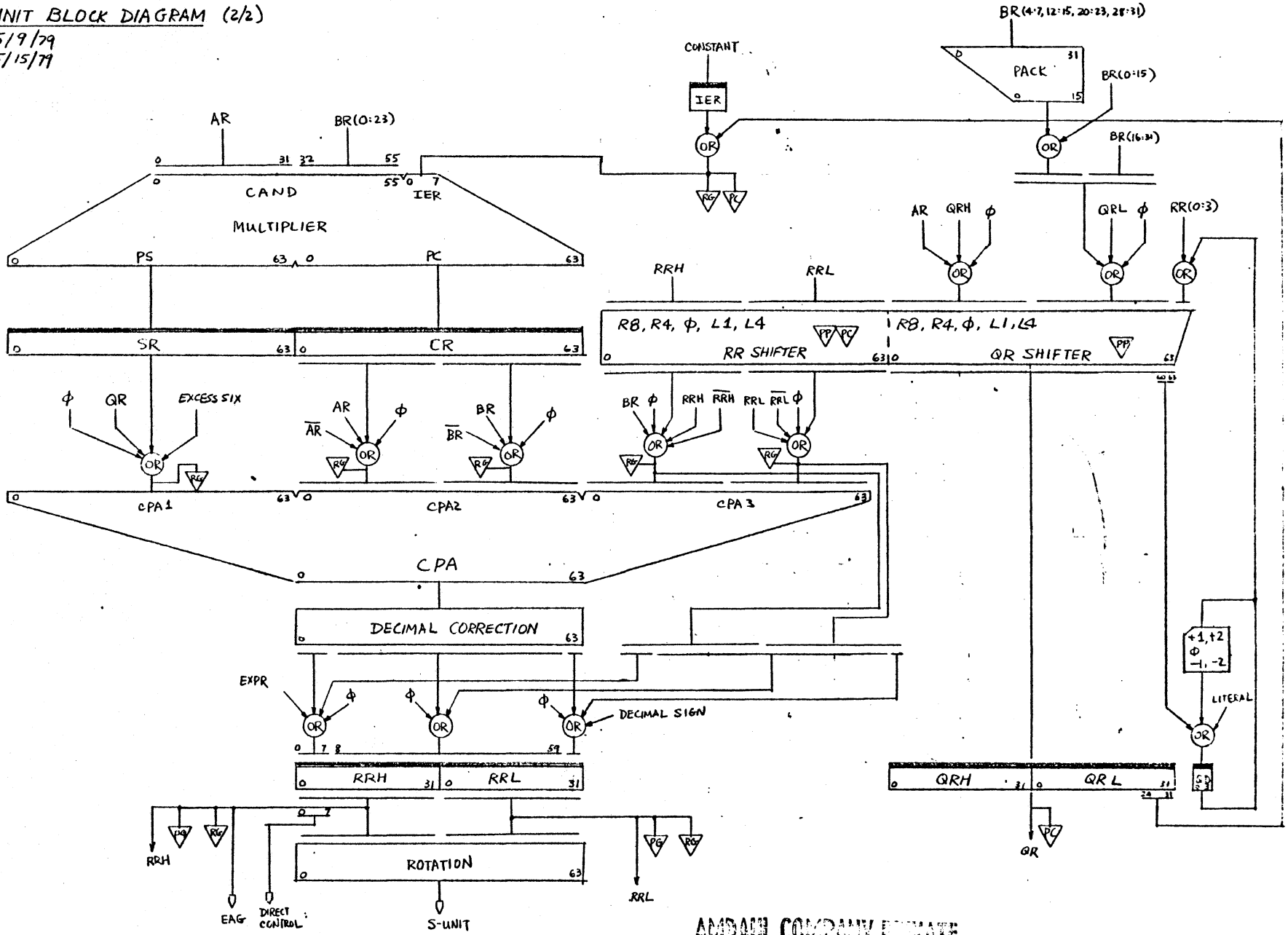
OSLO E-UNIT BLOCK DIAGRAM (1/2)

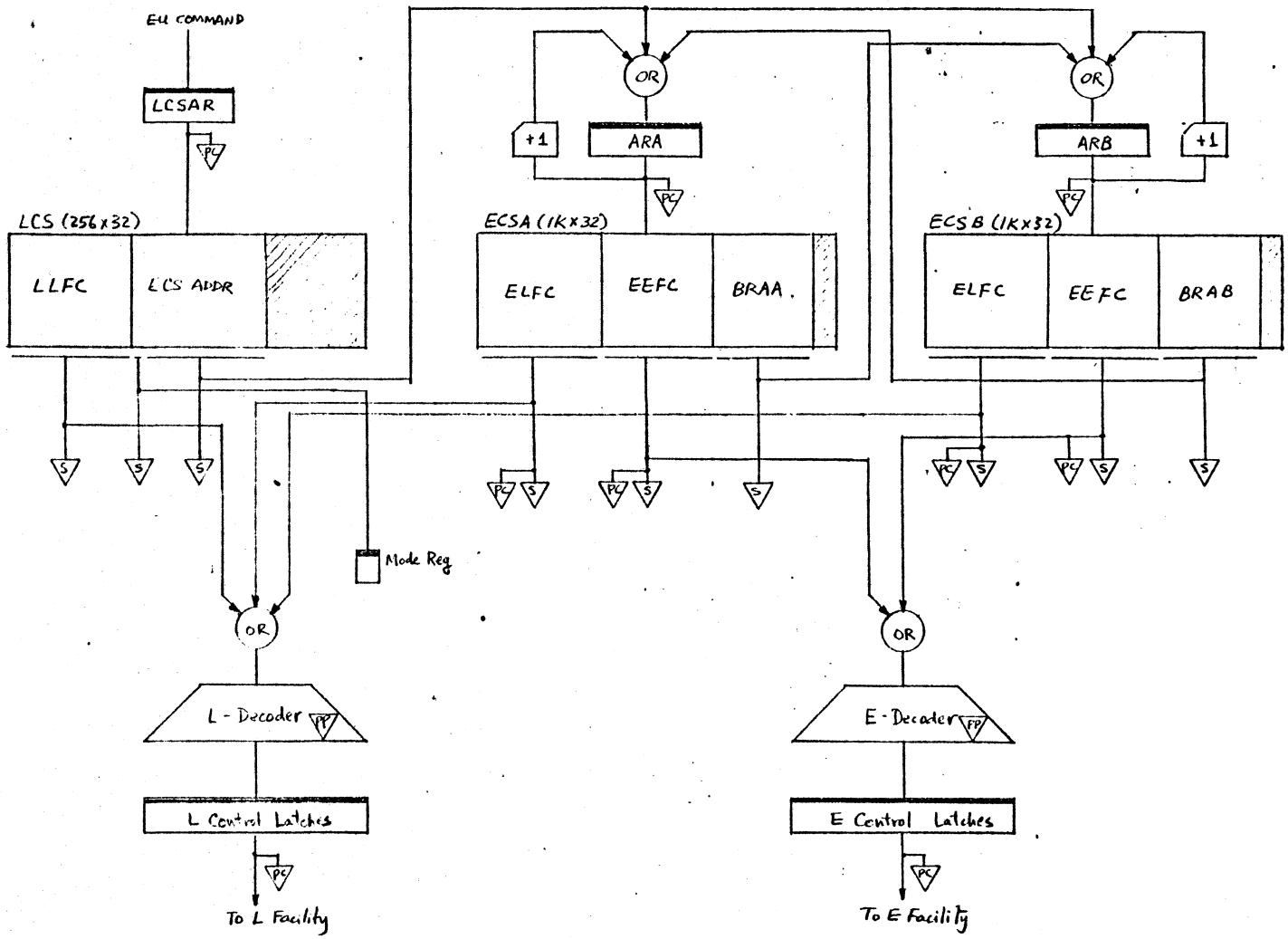
S. Lee 5/9/79
5/15/79



OSLO E-UNIT BLOCK DIAGRAM (2/2)

S. Lee 5/9/79
5/15/79

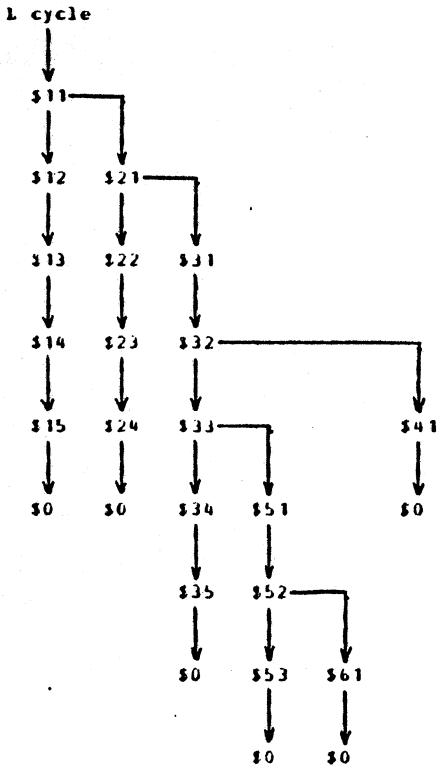




OSLO E-UNIT CONTROL

Sherman Lee
5/31/79

Two-Mode Control Store Scheme



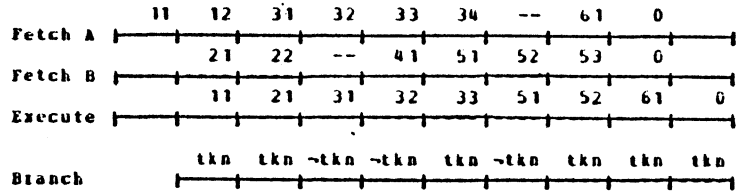
Module A

addr		BRAA
0	cw 0	0
=	=	=
11	cw 11	21
12	cw 12	--
13	cw 13	--
14	cw 14	--
15	cw 15	0
=	=	=
31	cw 31	--
32	cw 32	41
33	cw 33	51
34	cw 34	--
35	cw 35	0
=	=	=
61	cw 61	0
=	=	=
1023		

Module B

addr		BRAB
0	cw 0	0
=	=	=
21	cw 21	31
22	cw 22	--
23	cw 23	--
24	cw 24	0
=	=	=
41	cw 41	0
=	=	=
51	cw 51	--
52	cw 52	61
53	cw 53	0
=	=	=
1023		

Suppose that the algorithm has to go through the cycle sequence 11-21-31-32-33-51-52-61. The fetching and the execution of each machine cycle is as follows.



Based on this structure, the E-unit microprogram is limited to a two way branch.

OSLO E-UNIT STATUS

CHIP USAGE

43 CHIP TYPES

89 LSI CHIPS

18 RAM CHIPS TOTAL: 107CHIPS

I/O USAGE

604 COUNTED SO FAR.

ESTIMATED FINAL COUNT: 640

CONTROL STORE USAGE

LCS: 176 WORDS USED OUT OF 256 AVAILABLE.

ECS: 1589 WORDS USED OUT OF 2048 AVAILABLE.

ESTIMATED FINAL COUNT: 10% MORE.

CONTROL STORE SIZE

LCS: 2 CHIPS - 256 WORDS X 32 BITS.

ECS: 16 CHIPS - 2 X 1K WORDS X 32 BITS.

CONTROL PATTERN

L FACILITY: 653 UNIQUE PATTERNS X 127 BITS.

E FACILITY: 440 UNIQUE PATTERNS X 104 BITS.

ESTIMATED FINAL COUNT: 10% MORE.

DECODER SIZE ESTIMATION

L DECODER: 6 - 7 CHIPS.

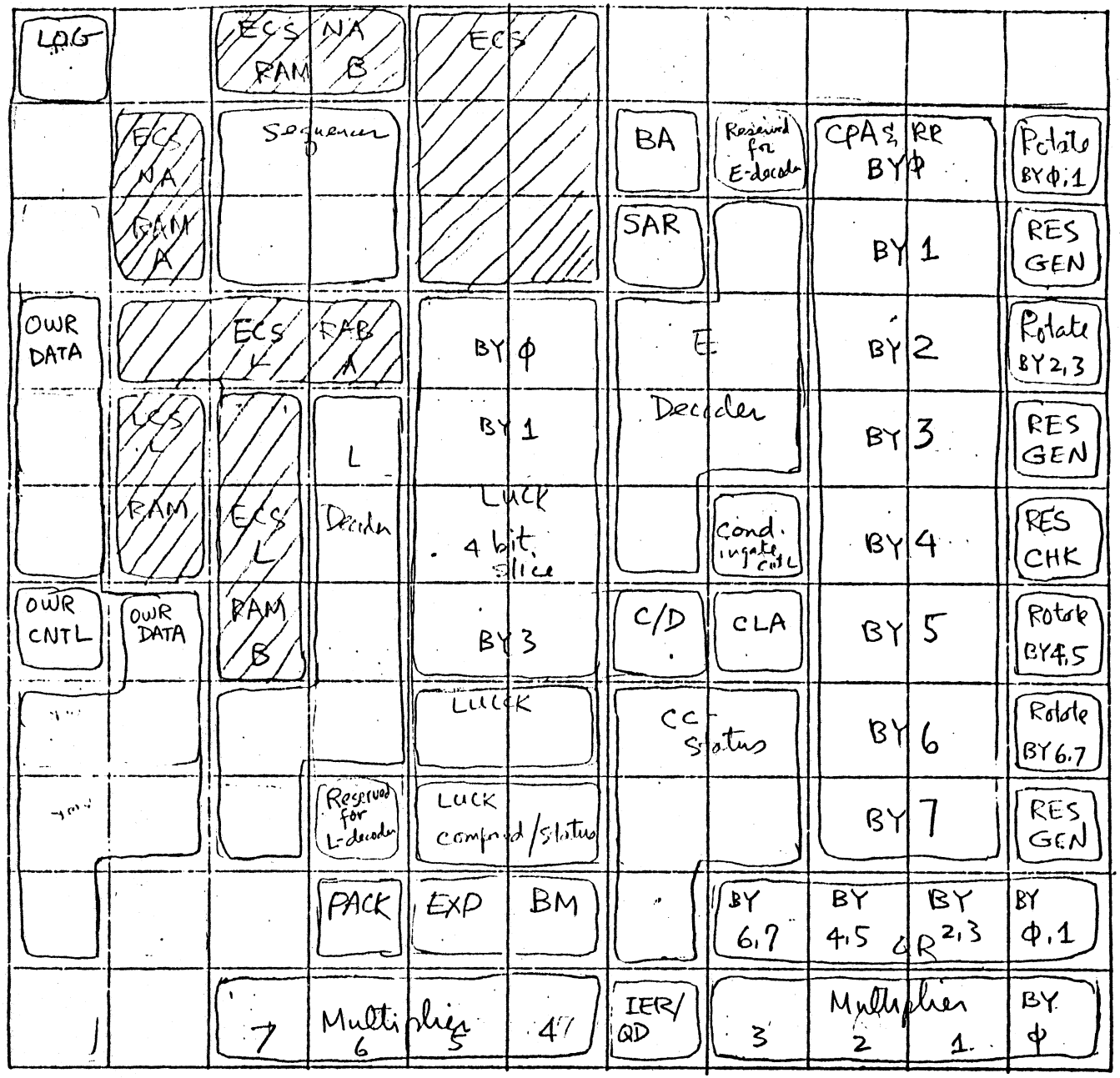
E DECODER: 5 - 6 CHIPS.

OSLO E-UNIT CHIPS 7/17/79 Sherman Lee

Chip Description	Usage	P/N	Date	Scan	Designer	FJ	S
BA/BAR	1	100119-1	6/26/9	P	JCO-JCW	411	R
BM/Edit	1	100208-1	(8/24/9)	S	JCO-JCW		
CLA	1	100006-1	(7/20/9)		JCW-PHS		
CPA #1	1	100003-3	(7/16/9)	S	JCW-JCO	405	
CPA #2	1	100004-3	(7/16/9)	S	JCW-JCO	406	
CPA #3	14	100005-3	(7/16/9)	S	JCW-JCO	410	
Clock Distribution	1		(9/14/9)		PHS-SHL		
Conditional Inqate Ctl	1	100157-2	7/05/9		PHS-DFM		R
Control Sequence #1	2		(9/09/9)	S	DFM-PHS		
Control Sequence #2	2		(9/16/9)	S	DFM-PHS		
CC-Status #1	1		(12/14/9)	S	PHS-SHL		
CC-Status #2	1		(11/21/9)	S	ALH-GLZ		
CC-Status #3	1		(2/22/0)	S	SHL-ALH		
CC-Status #4	1		(10/05/9)	S	GLZ-PHS		
CC-Status #5	1		(11/21/9)	S	GLZ-PHS		
EXP	1	100222-1	(9/07/9)	S	BTC-JCO		
E-Decoder #1	1		(2/01/9)	P	ALH-SSS		
E-Decoder #2	1		(2/01/9)	P	JCW-JCO		
E-Decoder #3	1		(2/01/9)	P	DFM-GLZ		
E-Decoder #4	1		(2/01/9)	P	SSS-ALH		
E-Decoder #5	1		(2/01/9)	P	JCO-JCW		
E-Decoder #6	1		(2/01/9)	P	GLZ-DFM		
IER/QD/Residue Check	1	100002-2	(7/20/9)	S	JCO-JCW	402	
LUCK 4-bit Slice	8	100125-1	(10/05/9)	S	JCW-JCO		
LUCK Magnitude Compare	1	100126-1	(10/19/9)		JCW-JCO		
LUCK Parity	1	100127-1	(10/12/9)	S	JCW-JCO		
LUCK Stat/Compact/Expand	2	100128-1	(8/24/9)		JAW-JCW		
L-Decoder #1	1		(2/22/0)	P	ALH-SSS		
L-Decoder #2	1		(2/22/0)	P	JCW-JCO		
L-Decoder #3	1		(2/22/0)	P	DFM-GLZ		
L-Decoder #4	1		(2/22/0)	P	SSS-ALH		
L-Decoder #5	1		(2/22/0)	P	JCO-JCW		
L-Decoder #6	1		(2/22/0)	P	GLZ-DFM		
Multiplier	8	100007-1	5/16/9	P	JCO-JCW	400	R
OWR Control	1		(11/21/9)	S	JCO-SSS		
OWR Data	9		(10/12/9)	S	JCO-SSS		
Pack	1	100205-1	(8/31/9)		SSS-DFM		
QR	4	100066-2	(7/16/9)	S	DFM-SSS	401	
RR Rotate and Status	4	100168-1	(9/21/9)		SHL-JCO		
Residue Generation	3	100171-1	(8/31/9)		ALH-SHL		
Residue Checking	1		(9/07/9)	S	ALH-SHL		
SAR/Decrementer	1	100131-1	(8/03/9)	S	JCO-JCW		
Scan	1	100194-1	(7/27/9)		DFM-SSS		
			43 p/n				
			89 LSI chips				
RAM Type I	16		18 RAM chips				
RAM Type III	2		107 Total Chips				

OSLO E-UNIT MCC LAYOUT

7/19/79
S. Lee



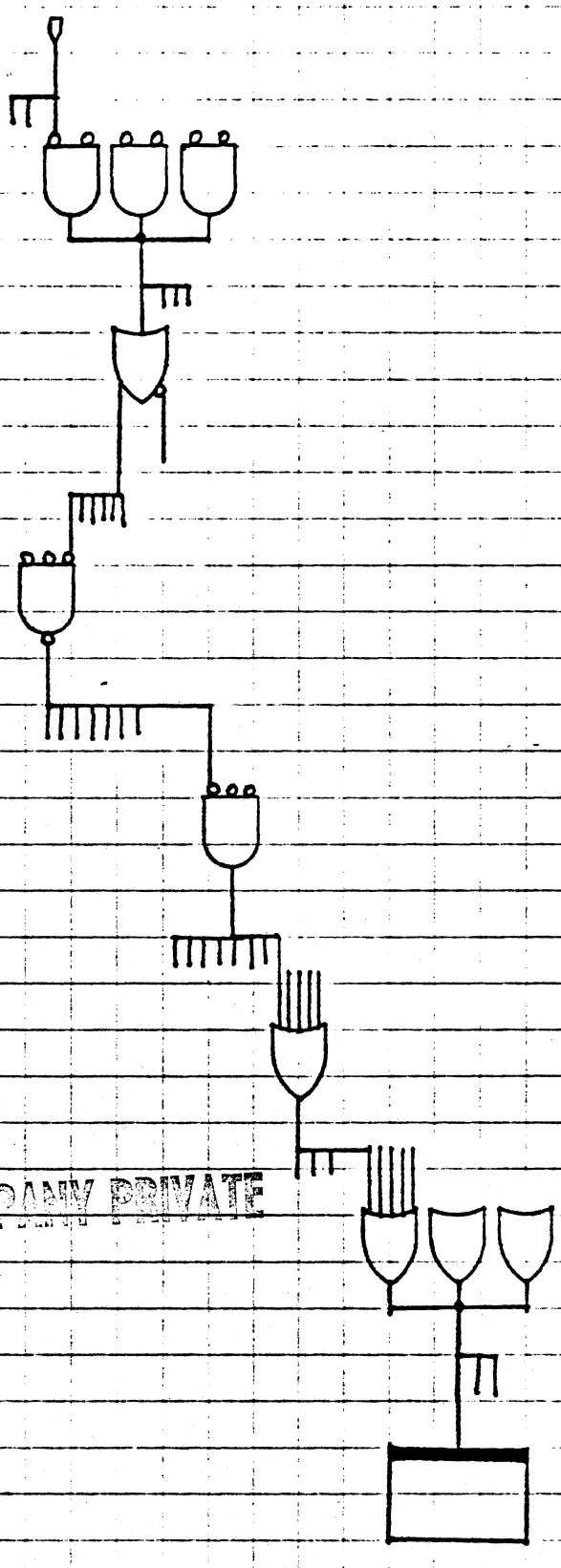
DECODER DESIGN APPROACH

* FIND ALL UNIQUE PATTERNS.
* FORM PATTERN MATRIX - ROW: PATTERN

  COLUMN: CONTROL SIGNAL
* COMPLEMENT COLUMNS WITH MORE 1's THAN 0's.
* SORT COLUMNS ACCORDING TO SIMILARITY.
* SORT ROWS IN ASCENDING ORDER.
* INTENTION IS TO MOVE THE 1's CLOSE TO EACH OTHER TO MAKE GROUPING EASIER.
* ADD DON'T CARE ROWS WHERE HELPFUL.
* PUT AS MANY SIMILAR COLUMNS AS POSSIBLE ONTO A CHIP.

Decoder

7/13/79



DECODER CHIPS ARE GATE LIMITED

FOR A CHIP THAT GENERATES 25 OUTPUT SIGNALS:

* 25 - 37.5 CELLS FOR LATCHES.

* 4.5 CELLS FOR SCAN LOGIC.

* 9 CELLS FOR SELECTION AND POWERING.

* APPROXMITELY 39 - 51 CELLS ARE USED FOR OVERHEAD LOGIC.

I-UNIT ALGORITHM PERFORMANCE

I. DESIGN PHILOSOPHY

II. DESIGN DECISIONS

III. INSTRUCTION TIMING - EXAMPLES

IV. CONCLUSIONS

I. I-UNIT ALGORITHM DESIGN PHILOSOPHY

- OPTIMIZE FREQUENTLY USED INSTRUCTIONS
- IMPLEMENT REMAINING INSTRUCTIONS AS FAST AS POSSIBLE USING MINIMAL ADDITIONAL HARDWARE

II. OSLO DESIGN DECISIONS

DESIGN DECISION WHICH IMPROVED INSTRUCTION PERFORMANCE

- ONE CYCLE PIPELINE
- IMPROVED EFFICIENCY OF I-FETCH MECHANISM
- REDUCED S-UNIT ACCESS DELAYS
  - SEPARATE I-FETCH AND OP BUFFERS
  - GREATLY REDUCED CHANNEL INTERFERENCE
  - ONE CYCLE ACCESS
- INCREASED WIDTH OF DATA PATHS
- REDUCTION OF I-UNIT PIPELINE INTERLOCKS

DESIGN DECISIONS WHICH HAVE LIMITED INSTRUCTION PERFORMANCE

- NOT BEING ABLE TO FETCH AND STORE BUFFER DATA IN ONE CYCLE
- NOT BEING ABLE TO READ AND WRITE FLOATING POINT AND SCRATCH REGISTERS IN ONE CYCLE

III. INSTRUCTION TIMING - EXAMPLES

L, LR, LA, LTR (f_i = .26)

- FACTORS IMPROVING PERFORMANCE:
  - OWR AND RR BYPASS TO EAG
  - RR, AR AND BR BYPASS TO LUCK
  - ONE CYCLE PIPELINE

• PERFORMANCE	V/6	OSLO
INSTRUCTION TIME	2	1
EXECUTE-GENERATE (EAG) DELAYS	1.0	.4
EXECUTE-EXECUTE (LUCK) DELAYS	0	0
TOTAL AVERAGE LOAD TIME	3	1.4

NOTE: L, LR, LA, LTR ACCOUNT FOR 85% OF ALL EXECUTE-GENERATE DEPENDENCIES

BC, BCR (f_i = .20)

- FACTORS IMPROVING BRANCH PERFORMANCE:
  - SHORT PIPELINE
  - EARLY CONDITION CODE SETTING INSTRUCTIONS (TM, CLI, LTR)

• PERFORMANCE	V/6	OSLO
CONDITIONAL TAKEN	5+	2.7 (2.3 + P)
CONDITIONAL FALLTHROUGH	2+	1.4 (1 + P)
UNCONDITIONAL TAKEN	5+	2.1
UNCONDITIONAL FALLTHROUGH	2	1.0
AVERAGE	3.9	2.2

P = PROBABILITY THAT BC IS PRECEDED BY CONDITION CODE SETTER OTHER THAN TM, CLI, LTR

P≤.45

OTHER BRANCHES (f_i = .04)

- PERFORMANCE (TAKEN/FALLTHROUGH)

BAL, BALR	8+	2.1/1.0
BCT, BCTR	7+/4+	3.1/1 or 2
BXLE, BXH	9+/6+	6.3/5
EX	8+	3.2

LOGICAL AND DATA MOVEMENT ALGORITHMS

- FACTORS WHICH HAVE IMPROVED PERFORMANCE:
  - WIDER DATA PATHS
  - ONE CYCLE PIPELINE
  - IMPROVED S-UNIT STORE ALGORITHM
    - FEWER CACHE ACCESSES REQUIRED TO MOVE A UNIT OF DATA

PERFORMANCE:	V6	OSLO
MOVING DATA	$4\left\lceil \frac{L}{4} \right\rceil$	$2\left\lceil \frac{L}{8} \right\rceil$
PROPAGATING OR CLEARING	$4\left\lceil \frac{L}{4} \right\rceil$	$2\left\lceil \frac{L}{32} \right\rceil$

LOGICAL AND DATA MOVEMENT ALGORITHM PERFORMANCE

	V6	OSLO
MVC (f_i = .03)		
MOVE CASE	$6 + 4\left\lceil\frac{L}{4}\right\rceil$ + ALIGN	$1 + 2\left\lceil\frac{L}{8}\right\rceil$ + ALIGN
1 - 4 BYTES	10	3
5 - 8 BYTES	14	3
128 BYTES	134 - 136	35 - 37
ONE BYTE OPERAND OVERLAP	6 + 4L	$5 + 2\left\lceil\frac{L}{32}\right\rceil$ + ALIGN
128 BYTES	518	13 - 19
XC (f_i = .002)		
OPERAND ADDRESSES EQUAL	6L	$2 + 2\left\lceil\frac{L}{32}\right\rceil$ + ALIGN
40 BYTES	240	6 - 12
LM (f_i = .013)	2R	$1.5 + \left\lceil\frac{R}{2}\right\rceil$
2 REGISTERS	4	2 - 3
5 REGISTERS	10	4 - 5
16 REGISTERS	32	9 - 10

	V6	OSLO
STM (f_i = .010)	2R	$1.5 + \left\lceil \frac{R}{2} \right\rceil + S$
2 REGISTERS	4	2 - 3
5 REGISTERS	10	4 - 5
16 REGISTERS	32	12 - 13
CLC (f_i = .017)	$2 + 4\left\lceil \frac{L}{4} \right\rceil + 6$ MM	$1 + 2\left\lceil \frac{L}{8} \right\rceil + 2.5$ MM
8 BYTES	10	3
MVCL (f_i = .0002)		
MOVE CASE ($L \leqslant 2K$)	$35 + 4\left\lceil \frac{L}{4} \right\rceil$	$21 + 2\left\lceil \frac{L}{8} \right\rceil$
400 BYTES	435	121
CLEAR CASE (R2 ODD = 0)	$80 + 4\left\lceil \frac{L}{4} \right\rceil$	$27 + 2\left\lceil \frac{L}{32} \right\rceil$
4096 BYTES	4176	283
MVI, NI, OI, XI (f_i = .035)	4	1 + S
STORE (f_i = .04)	2	1 + S (0<S<1)
OTHER ONE CYCLE INSTRUCTIONS (f_i = .23)	2	1

	V6	OSLO
EDIT (f_i = .003)	6L	4L + 1
10 BYTES	60	41
EDMK (f_i = -)	6L + 6	4L + 4
10 BYTES	66	44
TR (f_i = .00001)	$5\ \frac{L}{4} + 4 + 4L$	4L + 1.5
1 BYTE	13	5
128 BYTES	676	514
TRT (f_i = .0002)	$5\ \frac{L}{4} + 4 + 4L$	3L + 3 + 2NZ
128 BYTES	676	389

IV. CONCLUSIONS

- THE INSTRUCTIONS DISCUSSED ON PREVIOUS SLIDES COMPRISE APPROXIMATELY 84% OF INSTRUCTIONS EXECUTED - BY OPCODE FREQUENCY - IN A HYPOTHETICAL ENVIRONMENT CONSISTING OF:

  50% SUPERVISOR CODE
  35% COMMERCIAL CODE
  15% SCIENTIFIC CODE

- DESIGN GOALS FOR INSTRUCTION PERFORMANCE, AS PUBLISHED IN THE "OSLO PERFORMANCE ESTIMATES" (P/N 820292-700A, 3-28-79), HAVE BEEN CLOSELY FOLLOWED

E-UNIT ALGORITHMS - STATUS

- ALL MAJOR COMPUTATIONAL ALGORITHMS HAVE BEEN WRITTEN
- SOME DATA MOVEMENT ALGORITHMS STILL NEED TO BE WRITTEN
- SIMULATION HAS BEGUN

		CAPACITY	CURRENT UTILIZATION
CONTROL STORE DEPTH:	ECSA	1024	814
	ECSB	1024	775
	TOTAL	2048	1589

ESTIMATED TOTAL UTILIZATION: 1800

	OP 1 LENGTH	OP 2 LENGTH	OSLO CYCLES	470 CYCLES
AP, SIGNS ALIKE	1 - 4		4	13
SP, SIGNS DIFFER	5 - 8		4	23
	9 - 12		9	33
	13 - 16		9	43
SP, SIGNS ALIKE	1 - 4		5	15
AP, SIGNS DIFFER	5 - 8		5	25
	9 - 12		11	36
	13 - 16		11	47
MP	1 - 4	1	19	21
	1 - 4	2	26	39
	1 - 4	3	33	57
	5 - 8	3	33	91
	5 - 8	7	61	185
	9	1	31	42
	9	8	80	300
	16	1	50	56
	16	7	134	365
	16	8	80	409
DP	2	1	24	48
	8	1	95	374
	8	4	65	212
	8	5	55	241
	12	1	151	592
	12	5	93	579
	16	1	211	810
	16	5	159	917

PERFORMANCE FOR DECIMAL ALGORITHMS

ALGORITHM IMPROVEMENTS (12/78 - 4/79)

		CURRENT OSLO CYCLES	PREVIOUS OSLO CYCLES	470 CYCLES
MR, M:	BOTH FACTORS POSITIVE	6	6	7
	EITHER FACTOR NEGATIVE	7	9	7
MH:	BOTH FACTORS POSITIVE	8	8	8
	EITHER FACTOR NEGATIVE	8	10	8
DR, D:	32 SIGNIFICANT QUOTIENT BITS	40	36	50
	24 SIGNIFICANT QUOTIENT BITS	34	36	50
	16 SIGNIFICANT QUOTIENT BITS	28	36	50
	8 SIGNIFICANT QUOTIENT BITS	22	36	50
	0 SIGNIFICANT QUOTIENT BITS			
	- NONZERO REMAINDER	14	36	50
	- ZERO REMAINDER	5	5	50
	(NEGATIVE OPERAND)	(ADD 1 - 2)	(ADD 2 - 3)	(ADD 0)
CVD:	OPERAND = 0	6	6	42
	$1 \leqslant$ OPERAND $<$ 1,000	20	51	42
	1,000 $\leqslant$ OPERAND $<$ 1,000,000	30	51	42
	1,000,000 $\leqslant$ OPERAND	48	51	42
	(NEGATIVE OPERAND)	(ADD 2)	(ADD 3)	(ADD 1)
PACK:	OP1 LENGTH = 9 BYTES	7 - 8	15	36
	% OF COMMERCIAL MIX TIME SPENT IN PACK	11%	20%	17%

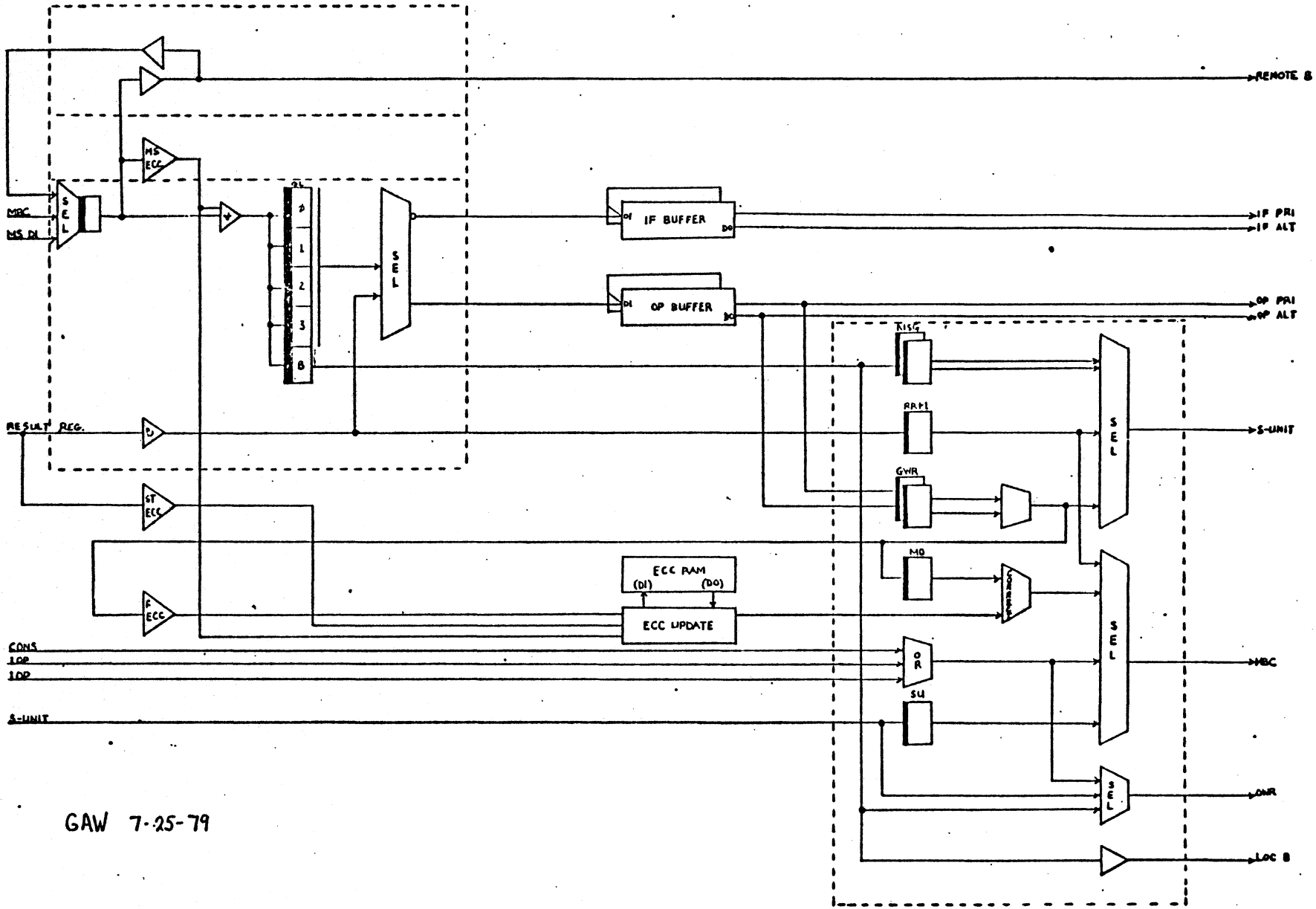
- EXCEPT FOR PACK, ALGORITHM IMPROVEMENTS REQUIRED NO SIGNIFICANT CHANGE IN HARDWARE

- CHANGE TO PACK REQUIRED A NEW CHIP

OSLO BUFFER MCC SUMMARY

- TWO MCC'S PER SYSTEM
- 32K BYTE TWO WAY ASSOCIATIVE OPERAND BUFFER
- 32K BYTE TWO WAY ASSOCIATIVE INSTRUCTION BUFFER
- 8 BYTE DATA PATHS - 4 PATHS PER MCC
- PROVIDES ECC ON OPERAND BUFFER DATA
- 32 BYTE DATA LINE WIDTH
- ACTIVE "OR" FOR ALL A-BUS SOURCES
- SOURCE OF LOCAL AND REMOTE B-BUS
- TWO CYCLE BRANCH PATH TIMING 46.0 NS
- BUFFER DATA WRITE CYCLE 24.0 NS
- BUFFER ECC UPDATE CYCLE 23.5 NS

OSLO BUFFER MCC BLOCK DIAGRAM



GAW 7-25-79

```
1 layout.data(buffer)
 LAYOUT.DATA(BUFFER)
```

OSLO BUFFER MCC LAYOUT

	RAM	RAM	RAM	RAM	DI	RAM	RAM	RAM	RAM		DO	
CONNECTOR	RAM	RAM	RAM	RAM	DI	RAM	RAM	RAM	RAM	ECC UPD	DO	CONNECTOR
	RAM	RAM	RAM	RAM	DI	RAM	RAM	RAM	RAM	ECC RAM	DO	
	RAM	RAM	RAM	RAM	DI	RAM	RAM	RAM	RAM	ST ECC	DO	
	BLK	BLK	BLK	BLK	MS ECC	BLK	BLK	BLK	BLK		BUS	
CONNECTOR	ADD	ADD	ADD	ADD	CLK	ADD	ADD	ADD	ADD		BUS	CONNECTOR
	RAM	RAM	RAM	RAM	DI	RAM	RAM	RAM	RAM	FETCH ECC	DO	
	RAM	RAM	RAM	RAM	DI	RAM	RAM	RAM	RAM	ECC UPD	DO	
CONNECTOR	RAM	RAM	RAM	RAM	DI	RAM	RAM	RAM	RAM	ECC RAM	DO	CONNECTOR
	RAM	RAM	RAM	RAM	DI	RAM	RAM	RAM	RAM	ECC UPD	DO	
	RAM	RAM	RAM	RAM	DI	RAM	RAM	RAM	RAM	ECC RAM	DO	

```
READY
losoff
D442GAW LOGGED OFF TSO AT 17:53:28 ON AUGUST 6, 1979
```

BUFFER MCC I/O

DATA BUSES	I/O
1. RESULT REGISTER DATA IN	36
2. MAINSTORE DATA IN	36
3. MBC DATA IN	36
4. S-UNIT DATA IN	36
5. CONSOLE DATA IN	36
6. IOP1 DATA IN	36
7. IOP2 DATA IN	36
8. IF BUFFER DATA OUT	72
9. OP BUFFER DATA OUT	72
10. OWR BUFFER BYPASS	36
11. S-UNIT DATA OUT	18
12. MBC DATA OUT	36
13. LOCAL B-BUS SOURCE	36
14. REMOTE B-BUS	36
	558
ECC CROSS COUPLING	
1. MAINSTORE ECC	18
2. BUFFER ECC	28
	46
ADDRESS	
I-UNIT ADDRESS	30
S-UNIT ADDRESS	30
WRITE BYTE MARKS	14
	74
CONTROL	
ADDRESS CONTROL	8
DATA IN CONTROL	9
DATA OUT CONTROL	18
	35
TOTAL MCC I/O	**713**

BUFFER MCC CHIP COUNT

BUFFER DATA RAM'S - TYPE VI	72
BUFFER ECC RAM'S - TYPE VI	3
BUFFER ADDRESS DRIVE	8
BUFFER BLOCK SELECT	8
BUFFER DATA IN	9
BUFFER DATA OUT	9
MAINSTORE ECC	1
STORE/FETCH ECC	2
ECC UPDATE	3
B-BUS DRIVE	2
CLOCK DISTRIBUTION/SCAN/ERROR	1

PART NUMBERS

LSI PART TYPES	9
RAM PART TYPES	1

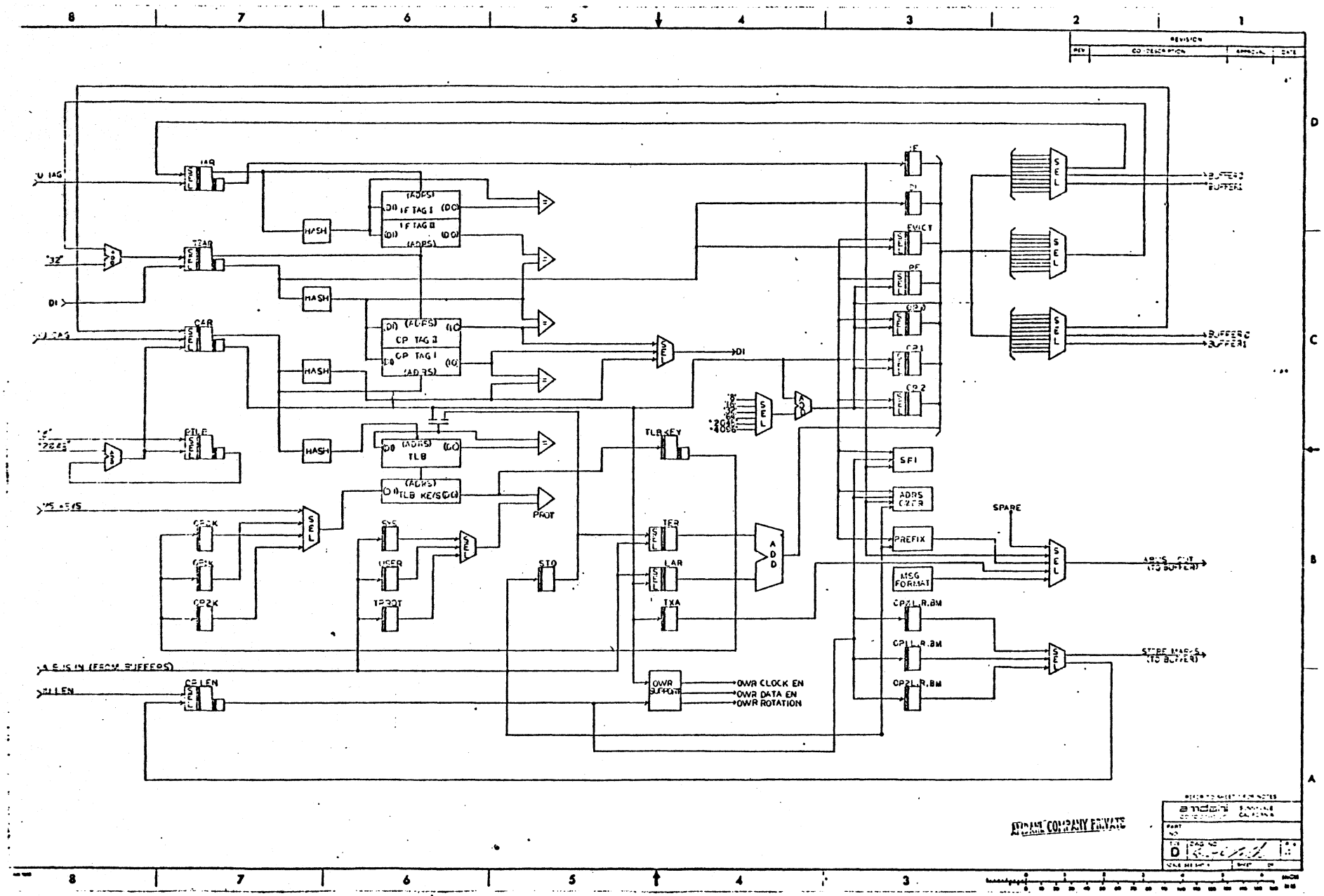
CHIP COUNT

LSI	43
RAM	75
TOTAL	118

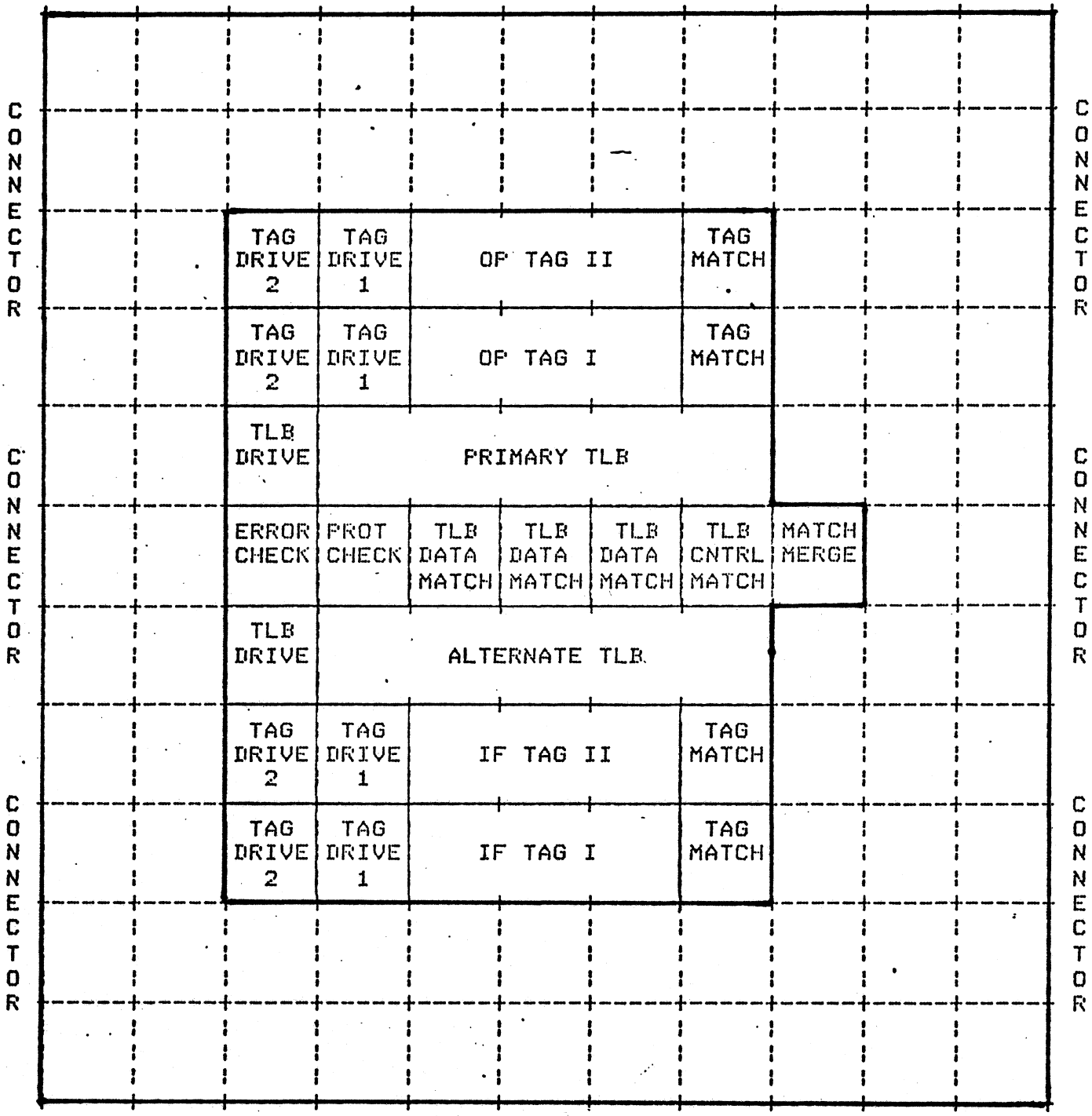
OSLO S-UNIT CHANGE SUMMARY

- ADDITION OF TAG 2 TO ELIMINATE DOUBLE CYCLING
- ELIMINATION OF TAG ECC DUE TO DUPLICATION
- REFERENCE AND CHANGE BITS NOT STORED IN THE TLB
- BLT REPLACED BY A LINKED LIST OF PSEUDO-SYNONYMS

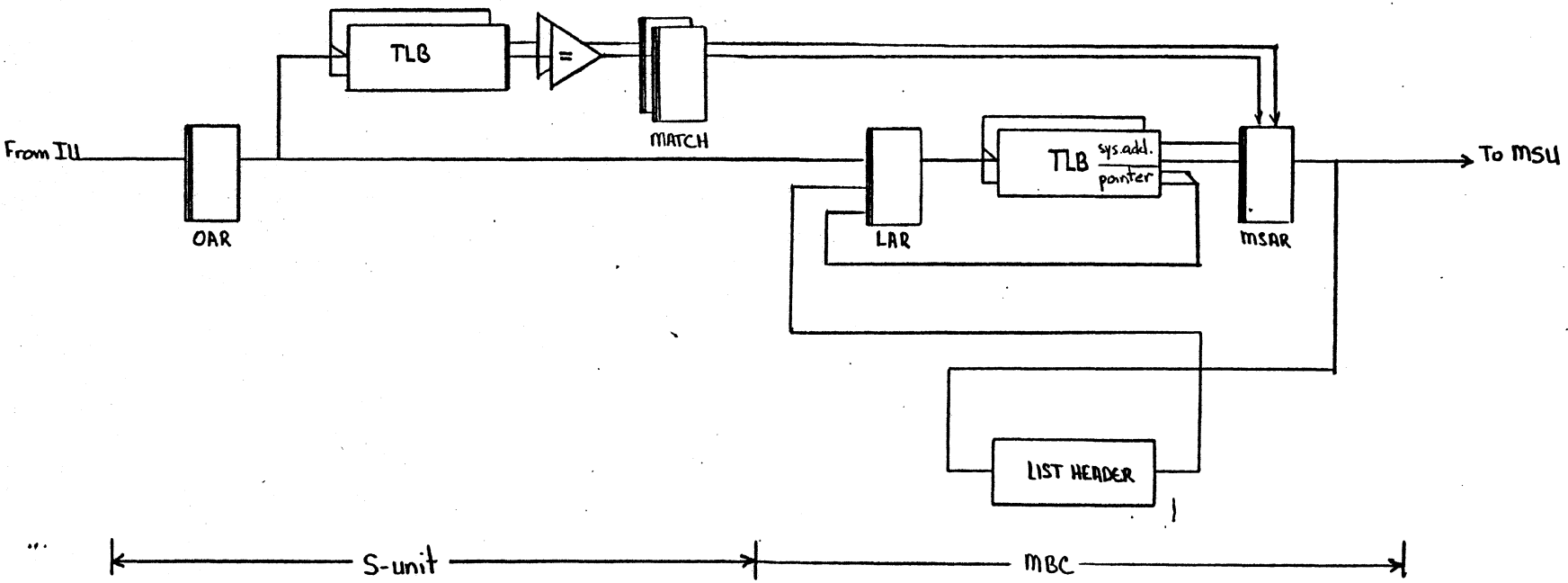
OSLO S-UNIT BLOCK DIAGRAM



OSLO TAG AND TLB LAYOUT



OSLO DATA INTEGRITY ADDRESS PATHS



S-UNIT CHIP COUNT

MAJOR FUNCTIONS	P/N'S	LSI	RAM	TOTAL
ADDRESS PATH	20	49	23	72
CONTROL	14	18	6	24
CLOCKS AND CONSOLE	3	3	0	3
S-UNIT MCC TOTAL	37	70	29	99

S-UNIT MCC I/O COUNT

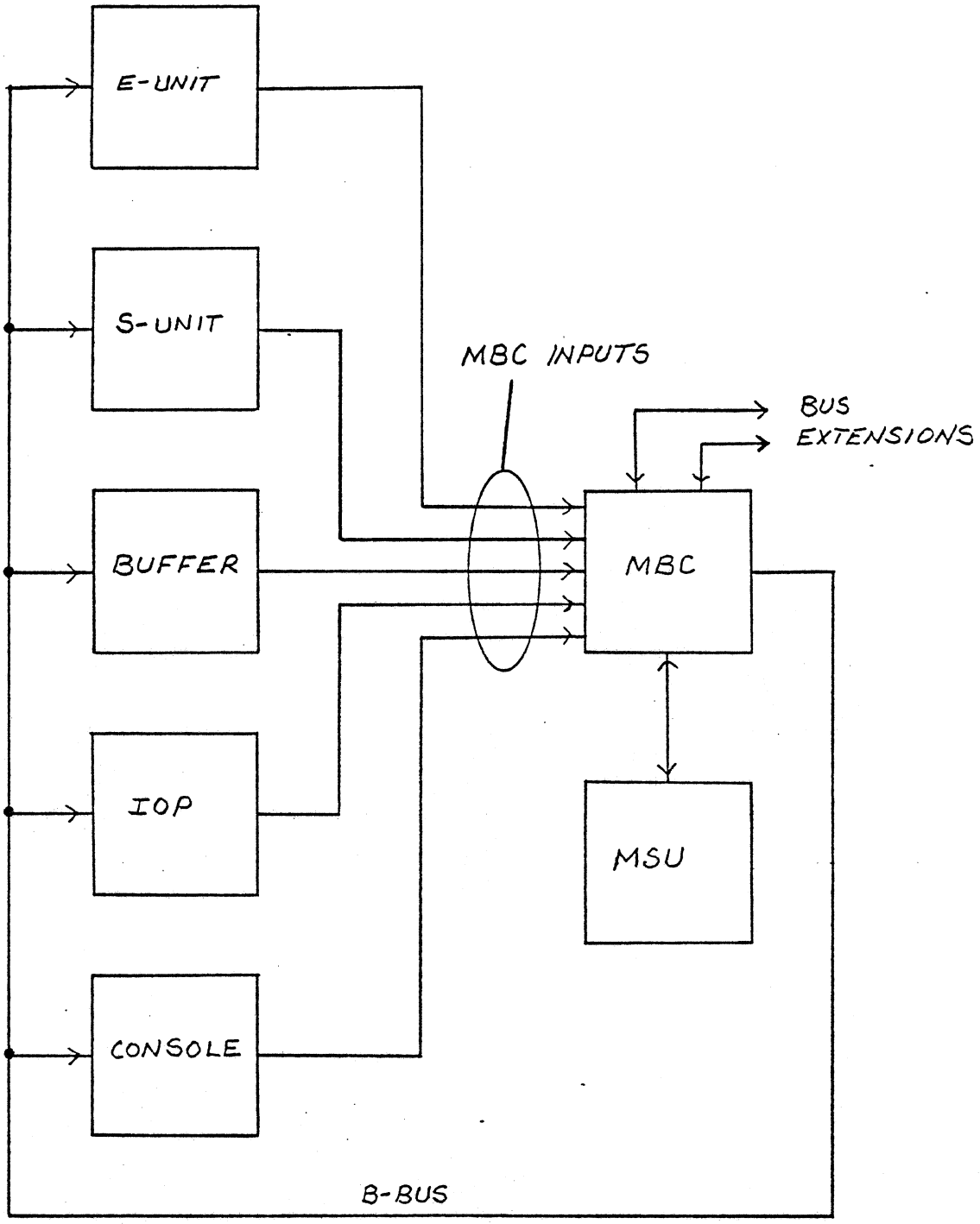
MCC FUNCTION	I/O'S
I-UNIT	131
E-UNIT	16
BUFFERS	171
MBC	172
CONSOLE	16
S-UNIT MCC TOTAL	506

BUS SYSTEM

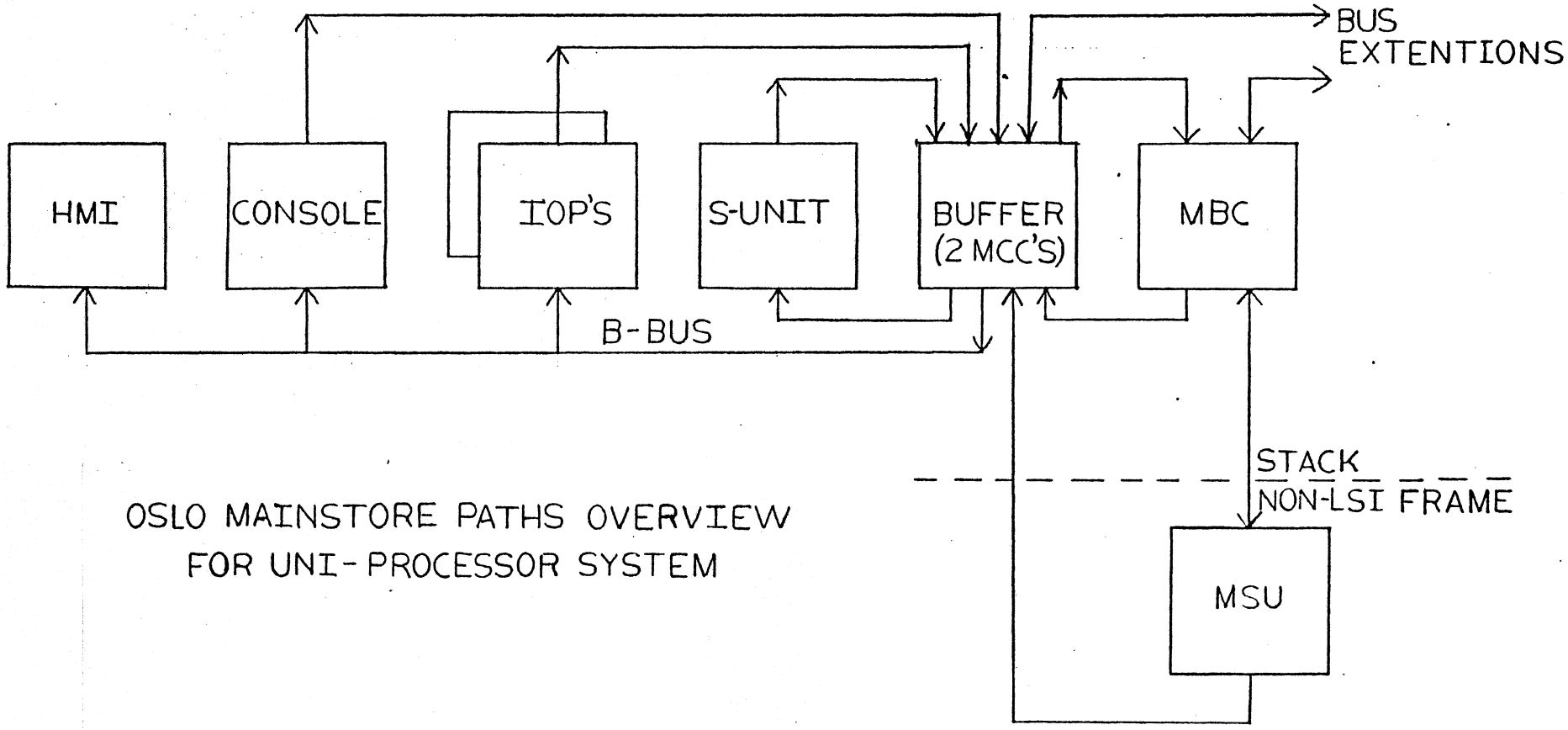
- PROVIDES COMMUNICATION PATHS BETWEEN UNITS:
  - CPU (I, E, S, BUFFER)
  - IOP (1 OR 2)
  - CONSOLE
  - HMI
  - MAINSTORE
  - REMOTE SYSTEM (MP)

- OPTIMIZED FOR MAINSTORE DATA FETCHES

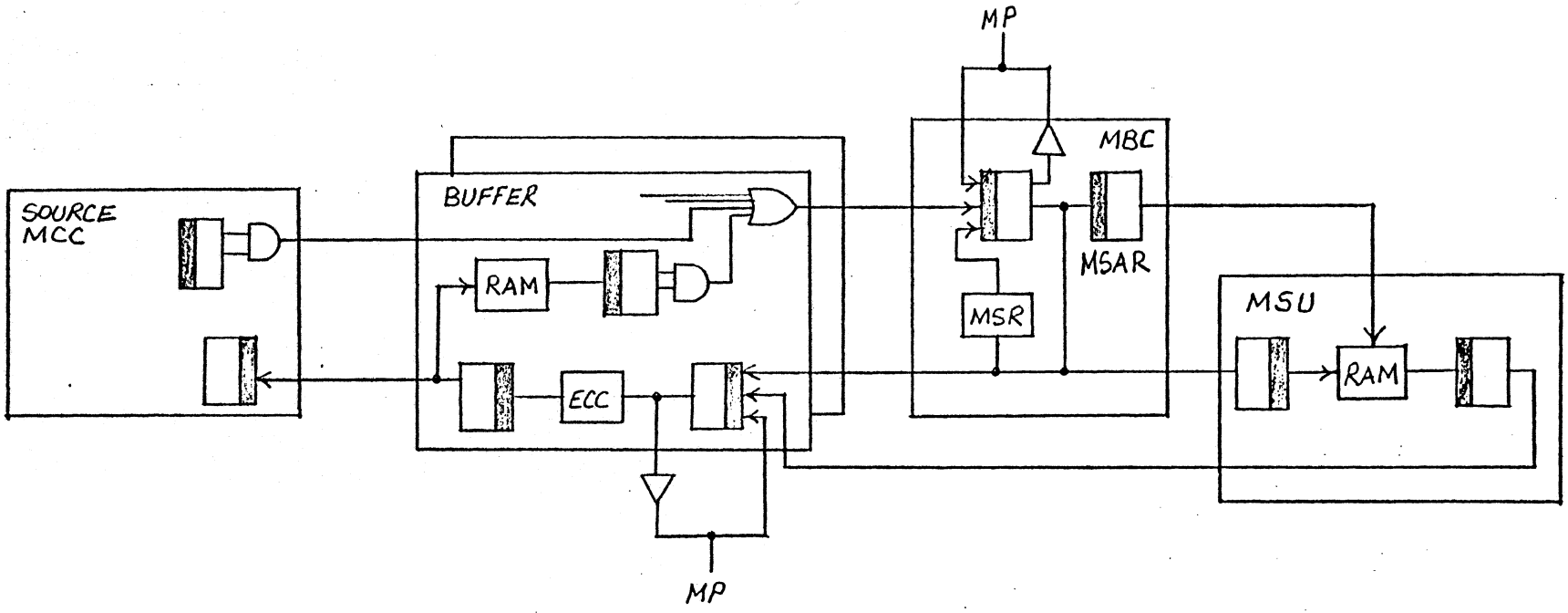
- METHOD:
  - COMMUNICATION BY FORMATTED MESSAGES
  - SIMULTANEOUS TRANSFER OF TWO MESSAGES:
    - 1 TO MBC MCC (A-BUS)
    - 1 FROM MBC MCC (B-BUS)
  - 8-BYTE DATA PATHS



OSLO BUS SYSTEM



OSLO MAINSTORE PATHS OVERVIEW
FOR UNI-PROCESSOR SYSTEM

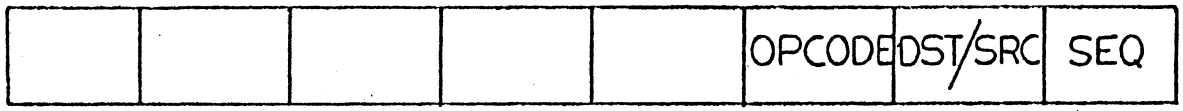


MESSAGE DATA PATHS

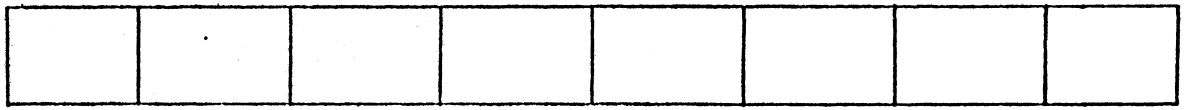
MESSAGE FORMAT

GENERAL:

HEADER



DATA



MESSAGE FORMAT

EXAMPLES:

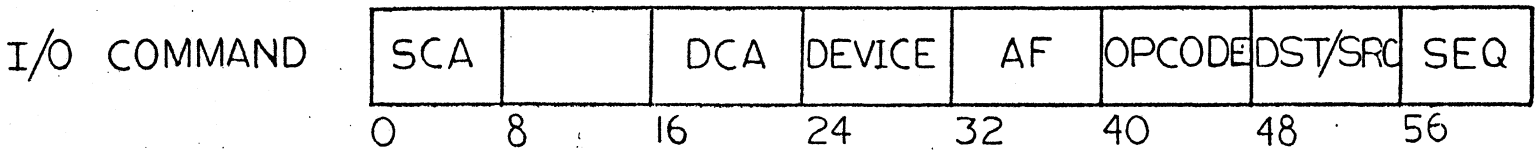
MS FETCH REQ.

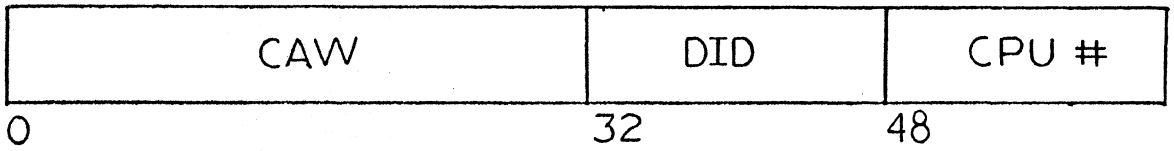
ADDRESS	KEY	OPCODE	DST/SRC	SEQ

MS STORE REQ.

ADDRESS	KEY	OPCODE	DST/SRC	SEQ
DATA				
DATA				
DATA				
DATA				

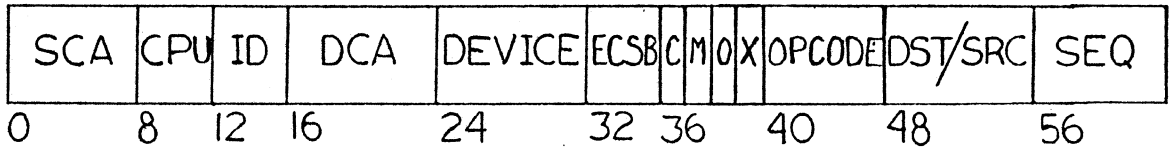
MESSAGE FORMAT

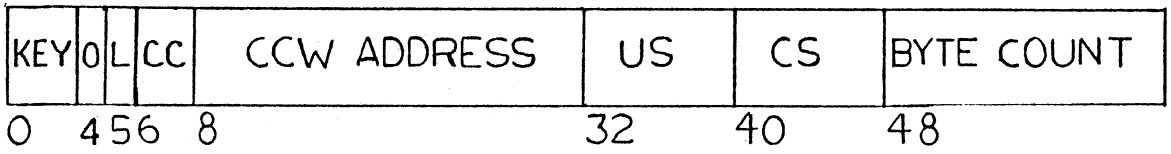




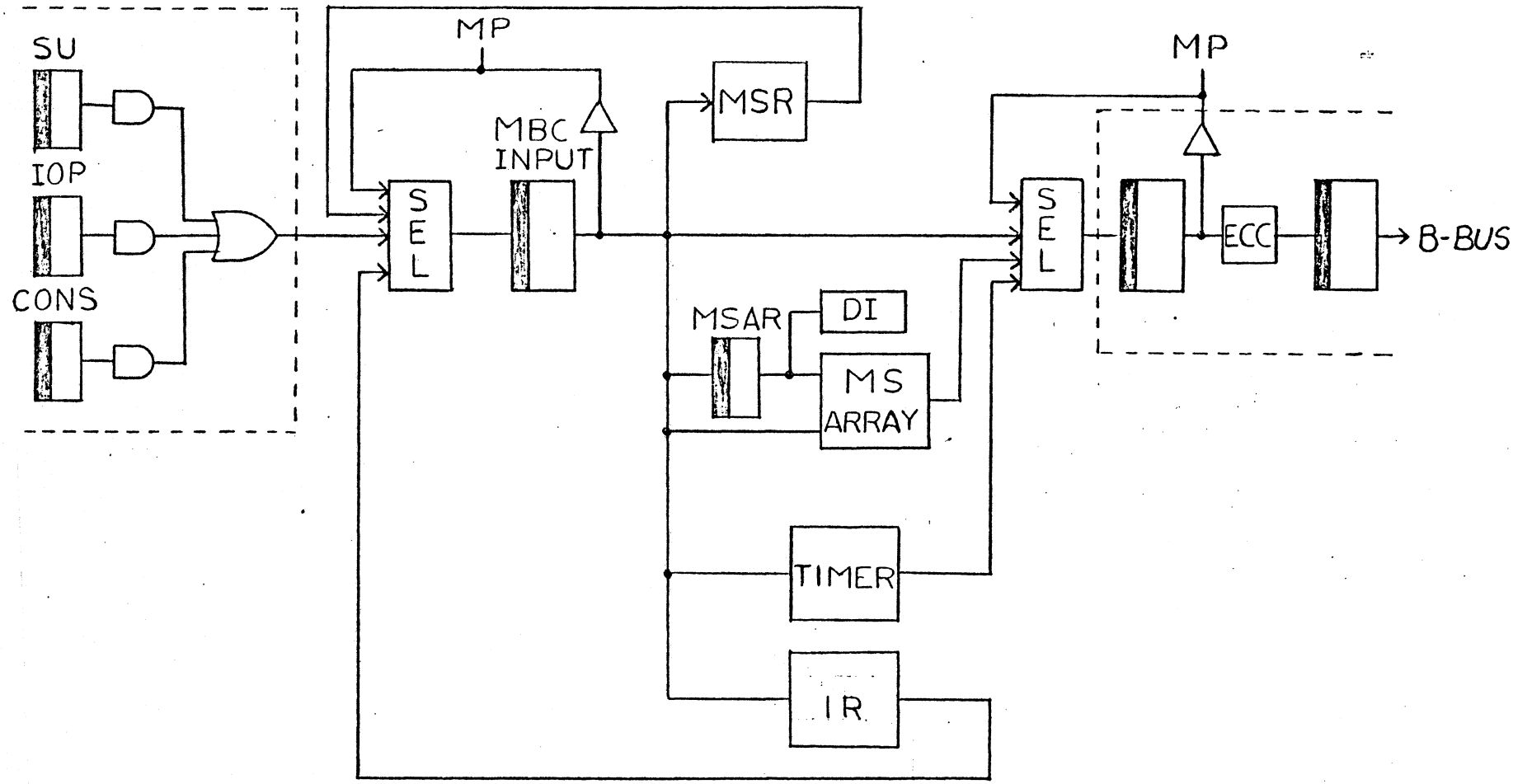
MESSAGE FORMAT

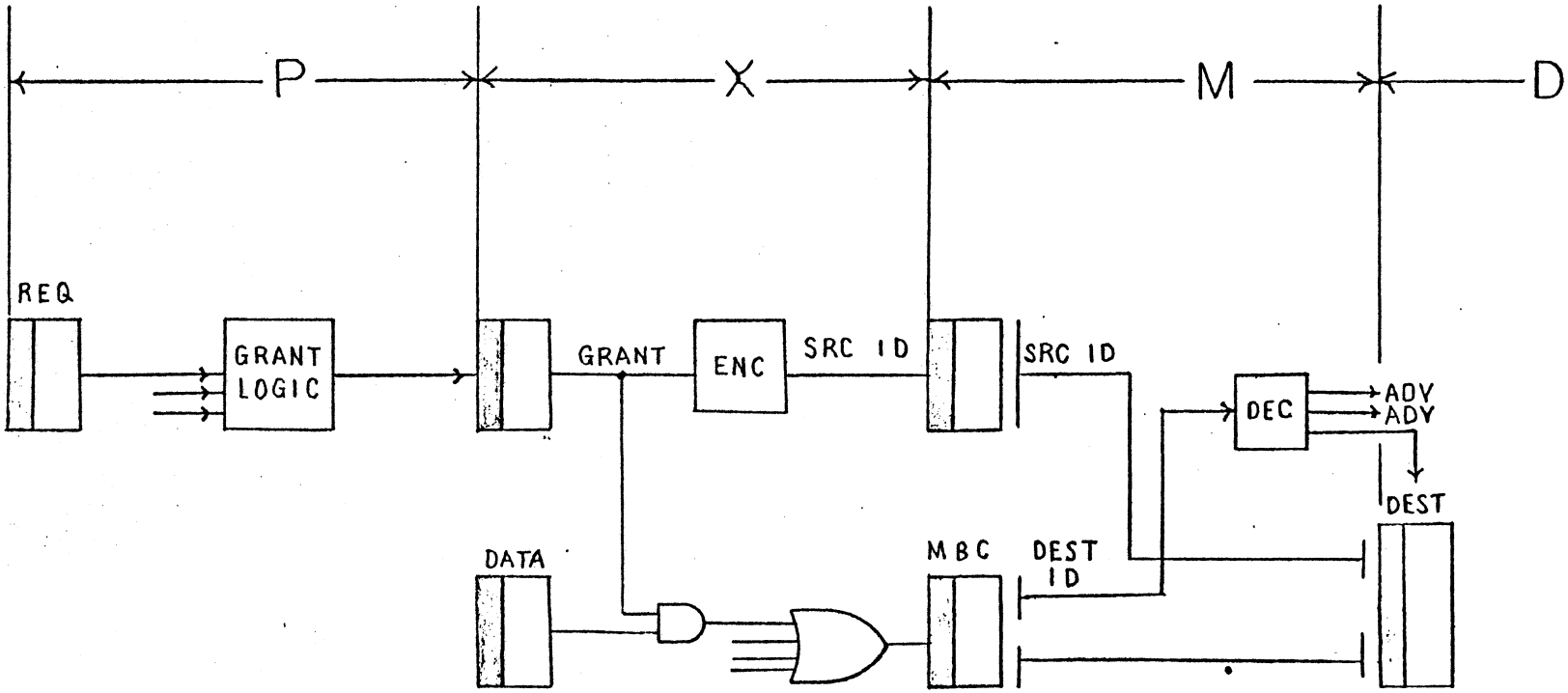
INTERRUPT REQUEST





BASIC MBC DATA PATHS





SOURCE/ DESTINATION ID HANDLING

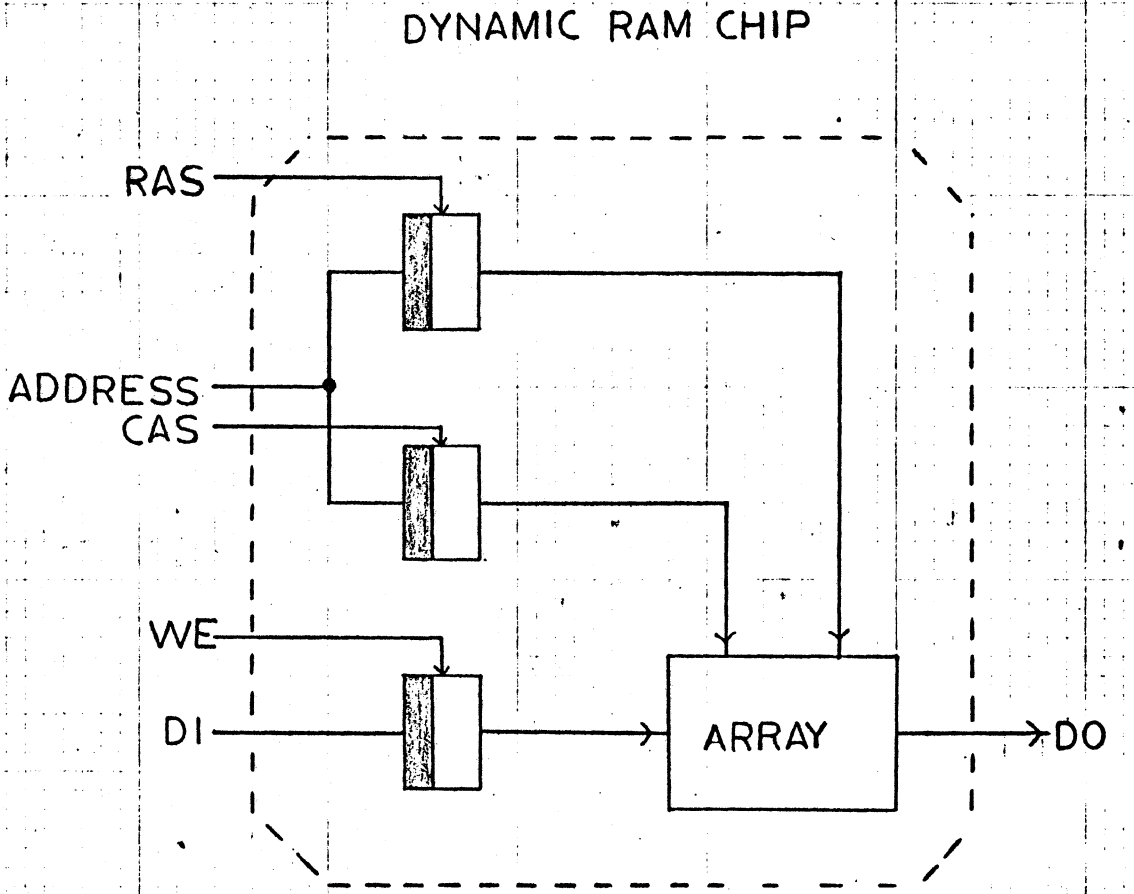
MAINSTORE

- CAPACITY/MSU
  - 16K RAM: 32 MBYTES
  - 64K RAM: 128 MBYTES

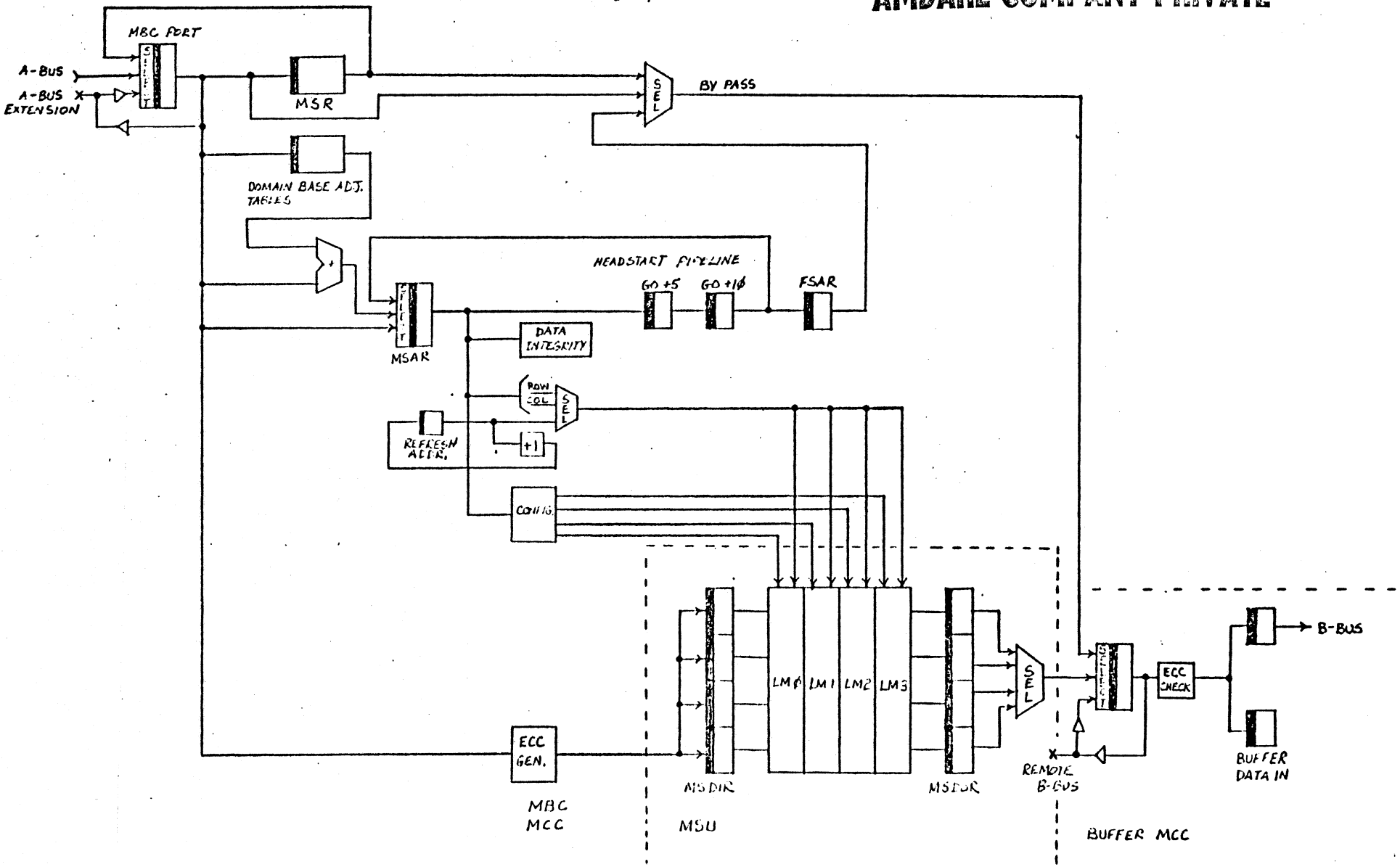
- INCREMENT SIZE
  - 16K FULLY POPULATED CARDS: 4 MBYTES
  - 64K HALF POPULATED CARDS: 8 MBYTES
  - 64K FULLY POPULATED CARDS: 16 MBYTES

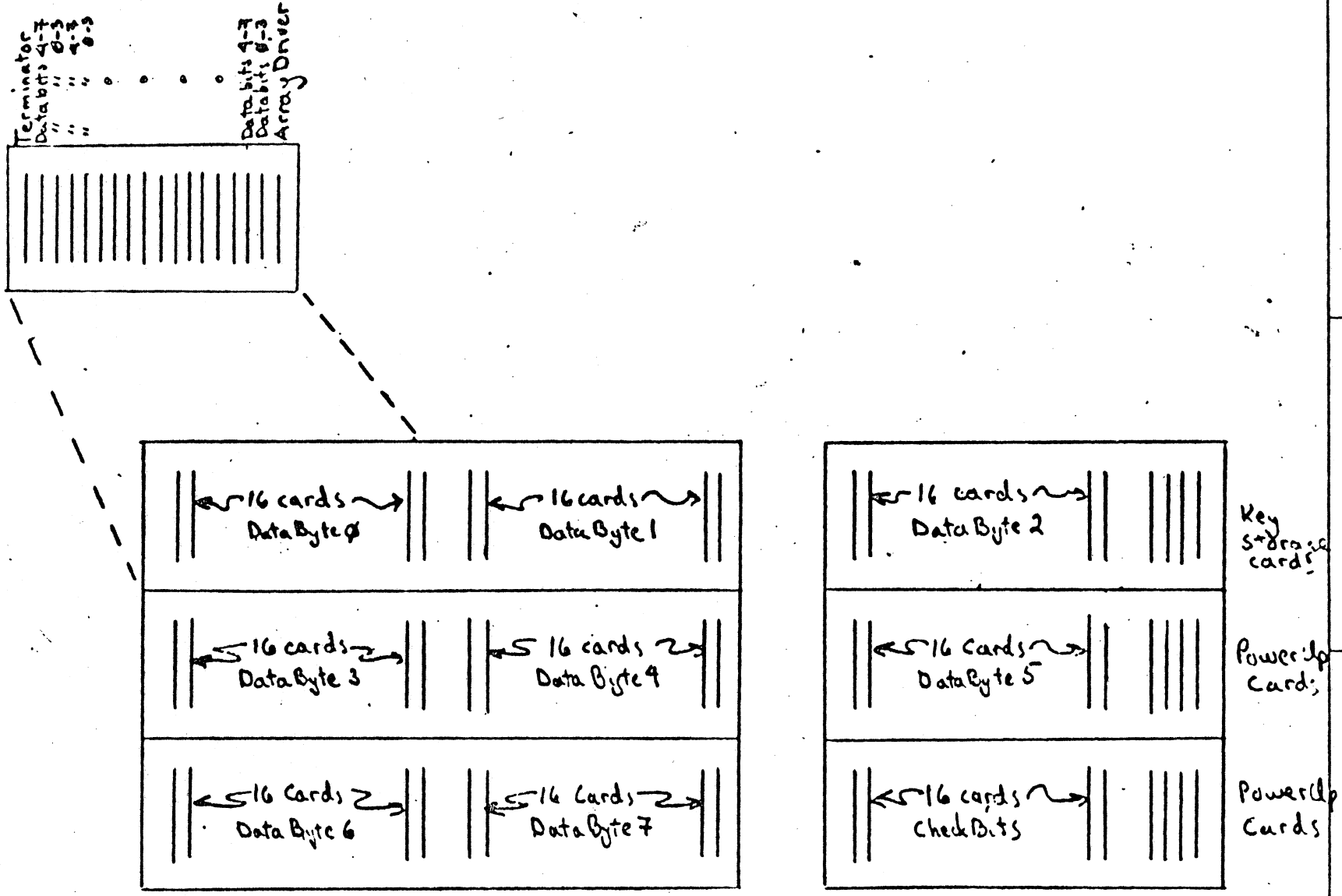
- PERFORMANCE
  - PEAK BANDWIDTH: 320 MBYTES/SEC.
  - ACCESS TIME: 10 CYCLES @ 20 NSEC/CYCLE

- FEATURES
  - 4 WAY INTERLEAVED
  - ALL CONTROL LOGIC IMPLEMENTED IN LSI

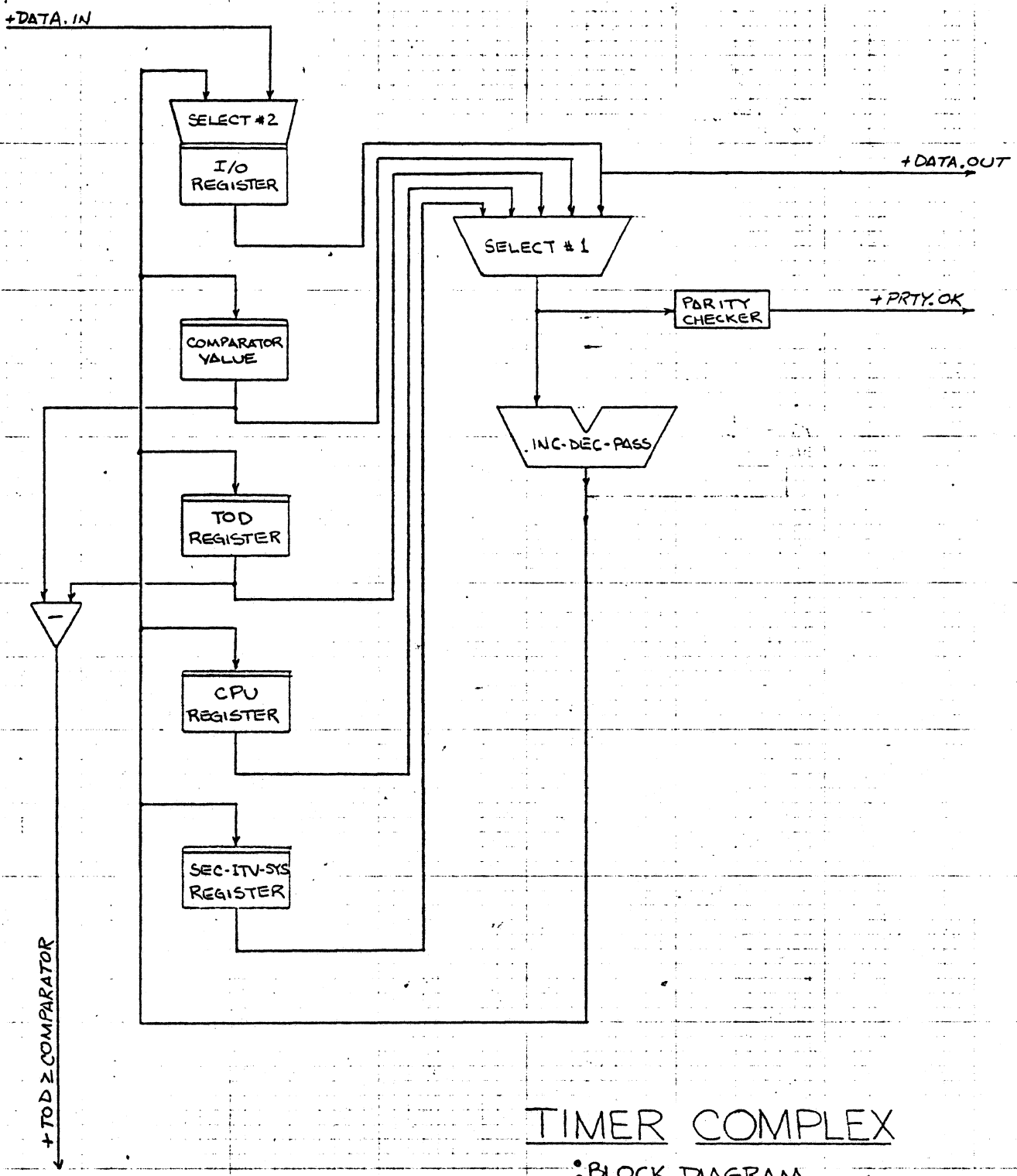


OSLO
MAIN STORE
DATA/ADDRESS PATHS





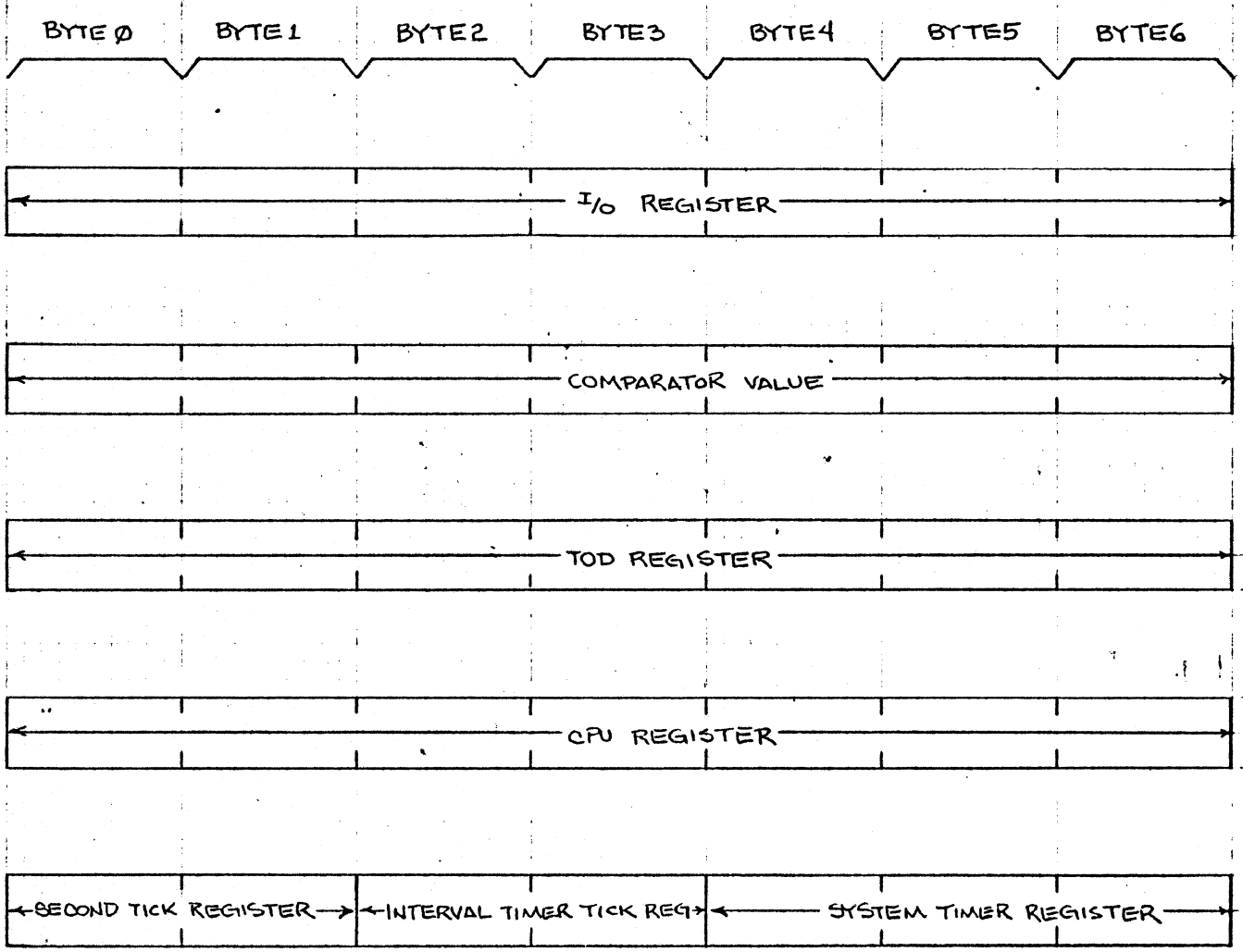
OSKO MS Backpanel Layout (card side)



TIMER COMPLEX

: BLOCK DIAGRAM

DINO 23:7:79

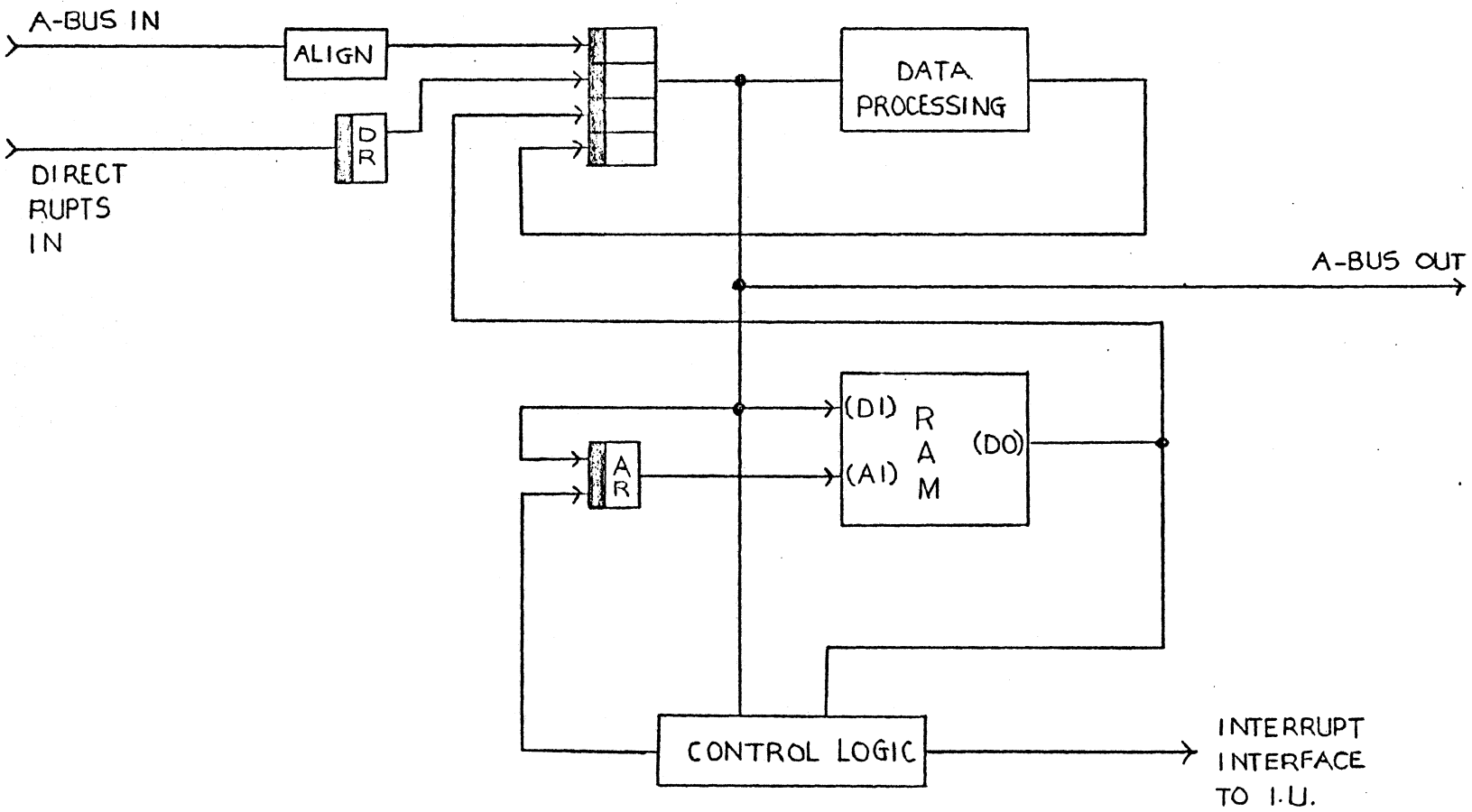


TIMER COMPLEX

: REGISTER ASSIGNMENTS

AMDAHL COMPANY PRIVATE

DINO 23:7:79



INTERRUPT ROUTER

MBC MCC

FUNCTION	P/N'S	CHIPS	RAM'S	I/O
BUS CONTROL	5	23	11	301
MAINSTORE CONTROL	8	20	2	278
DATA INTEGRITY	6	8	14	76
INTERRUPT ROUTER	5	10	2	25
TIMER COMPLEX	3	10	0	14
CLOCK CONTROL	4	6	0	25
	31	77	29	719
TOTAL				
	31	106		719

CRITICAL PATHS - MBC

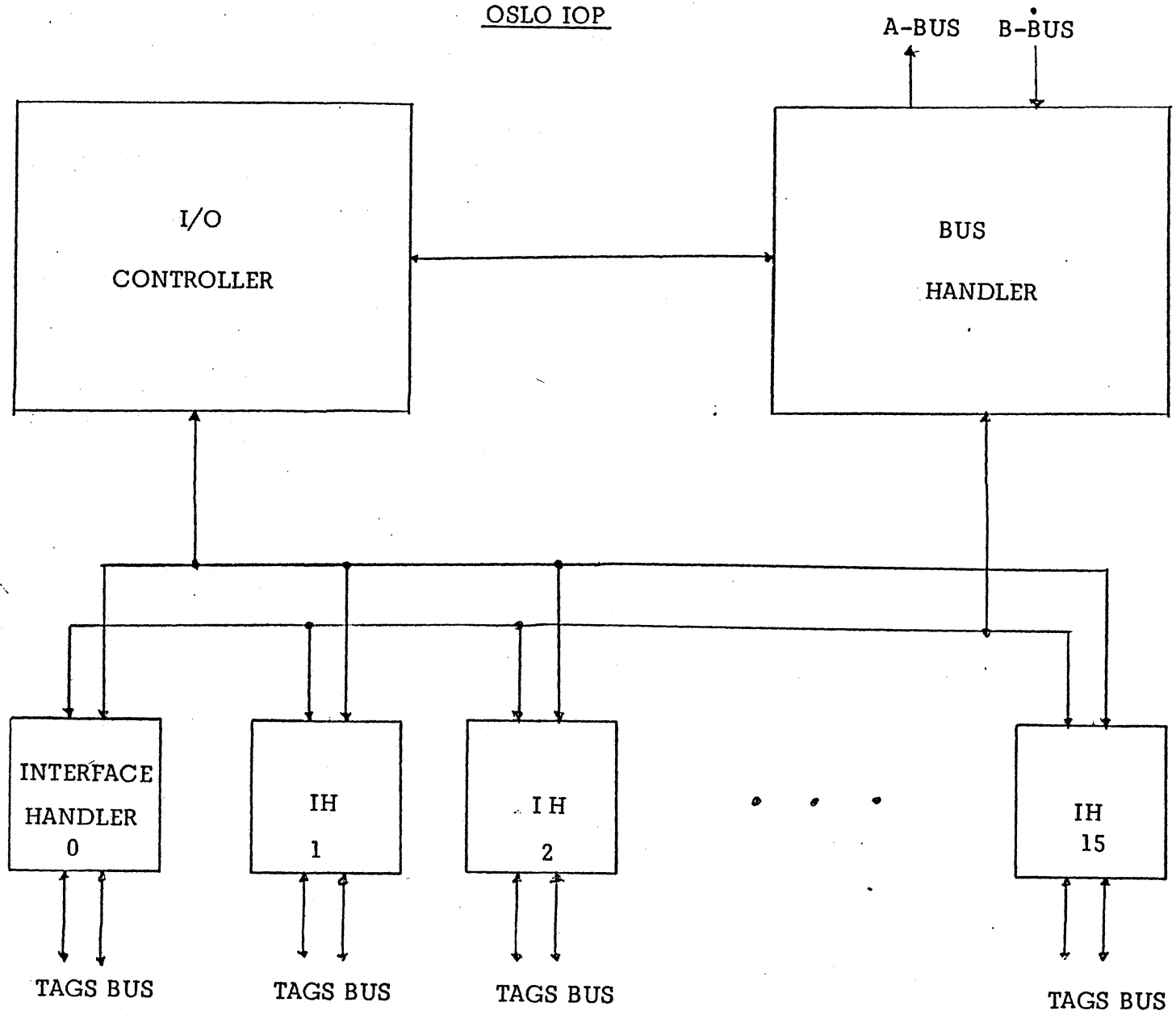
	DELAY	AVAILABLE
TLB SA ACCESS & MATCH	20.7	20
DOMAIN BASE ACCESS & ADJUST	26.2	26
MAINSTORE ACCESS	196	200
KEY READ/MODIFY/WRITE	94	100
INTER-STACK DATA TRANSFER (4')	18	20

I O P G O A L S

- IMPLEMENT ALL CHANNEL FEATURES REQUIRED BY THE ALTA POO
  - SUBCHANNEL QUEUING
  - CHANNEL CROSS-CALL
  - LOGICAL PROCESSOR FACILITY
  - CHANNEL DAT
- PROVIDE A HIGH DATA TRANSFER RATE FOR INDIVIDUAL CHANNELS AND AGGREGATE
- MINIMIZE INTERFERENCE BETWEEN CHANNELS
  - BARREL IOC TO ELIMINATE CONTENTION FOR PROCESSOR (SIOF, CHAINING, INTERRUPTS)
  - DATA BUFFERING DONE AT I/O INTERFACE
- MODULAR DESIGN WITH SIMPLE INTERFACES BETWEEN FIRST LEVEL MODULES
- ALLOW CHANGES TO I/O INTERFACE WITHOUT REDESIGN OF ENTIRE IOP

DLC 8/7/79

OSLO IOP



I / O C O N T R O L L E R (IOC)

- PROVIDES ALL CONTROL FUNCTIONS FOR IOP
  - PERFORMS I/O INSTRUCTIONS
  - FETCHES CHANNEL COMMAND WORDS
  - REQUESTS INTERRUPTS
  - PERFORMS LIMITED ERROR RECOVERY AND LOGOUT
- EXPLICITLY CONTROLS ALL OTHER MODULES
- CAN ACTIVATE AUTOMATIC FUNCTIONS IN OTHER MODULES OR PERFORM SAME FUNCTIONS BY ITSELF
- MICROPROGRAMMED
- EFFICIENT MICROINSTRUCTIONS TAILORED FOR CONTROL FUNCTIONS

BUS HANDLER (BH)

- INTERFACE TO CPU AND MAIN STORAGE VIA MEMORY BUS CONTROLLER (MBC)
- SENDS MESSAGES TO OTHER UNITS FROM IOC
- RECEIVES MESSAGES FROM OTHER UNITS FOR IOC
- ASSEMBLY OF DATA BYTES FROM IH INTO LINES FOR TRANSFER TO MAIN STORAGE
- NOT PRIMARILY USED FOR DATA BUFFERING
- IH DATA REQUESTS SERVICED BY A MODIFIED ROUND ROBIN SCHEME

I N T E R F A C E H A N D L E R (IH)

- LSI LOGIC (IN NON-LSI FRAME)
- ONE PER CHANNEL
- BUFFERS INTERFACE DATA IN UNALIGNED FORM
- PERFORMS TAG CONTROL FOR DEVICE SELECTION, DATA TRANSFER, AND CHAINING
- HIGH SPEED VERSION TO BE DESIGNED WHEN ITS INTERFACE IS KNOWN

I O P M I C R O C O D E

FUNCTION

- DIRECT ALL CHANNEL ACTIVITY BY
  - CARRYING OUT CPU I/O COMMANDS
  - SUPERVISING DEVICE CONTROL BY IH
  - SUPERVISING DATA TRANSFER

FEATURES

- MICROCODE SIZE IS <4K MICROWORDS
- ONE COPY OF MICROCODE IS SHARED BY ALL CHANNELS
- MICROCODE ENHANCES DESIGN FLEXIBILITY AND EXTENSION

ORGANIZATION

- EACH CHANNEL ACTIVITY IS PERFORMED BY A SEPARATE MICROCODE PROCEDURE
- PROCEDURES ARE STRUCTURED IN A HIERARCHY
- MICROLANGUAGE AND STRUCTURED PROCEDURES MAKE MICROCODE EASY TO PRODUCE, UNDERSTAND, AND MAINTAIN

I / O C O N T R O L L E R (IOC) O V E R V I E W

- ACHIEVES LOGIC COMPACTION BY USING 'BARREL' PROCESSING APPROACH
  - ALLOWS INTERLOCK-FREE MULTI-CYCLE PIPELINE
  - MORE POWERFUL MICROINSTRUCTIONS

- MICROINSTRUCTION FORMAT

  (B) ← (A) OP (B), BRANCH;

- MEMORY INTENSIVE DESIGN
  - INTERLEAVED WORKING STORAGE ALLOWS ONE EXECUTE PER CYCLE
  - INTERLEAVED CONTROL STORE USES DENSE 2K x 8 CHIPS
  - SECOND LEVEL CONTROL-STORE (NAND-STORE) SAVES SPACE IN FIRST LEVEL MICROSTORE

- NO MICROINTERRUPTS

- CHIP COUNT

  30 LOGIC 30 MEMORY

- PN COUNT

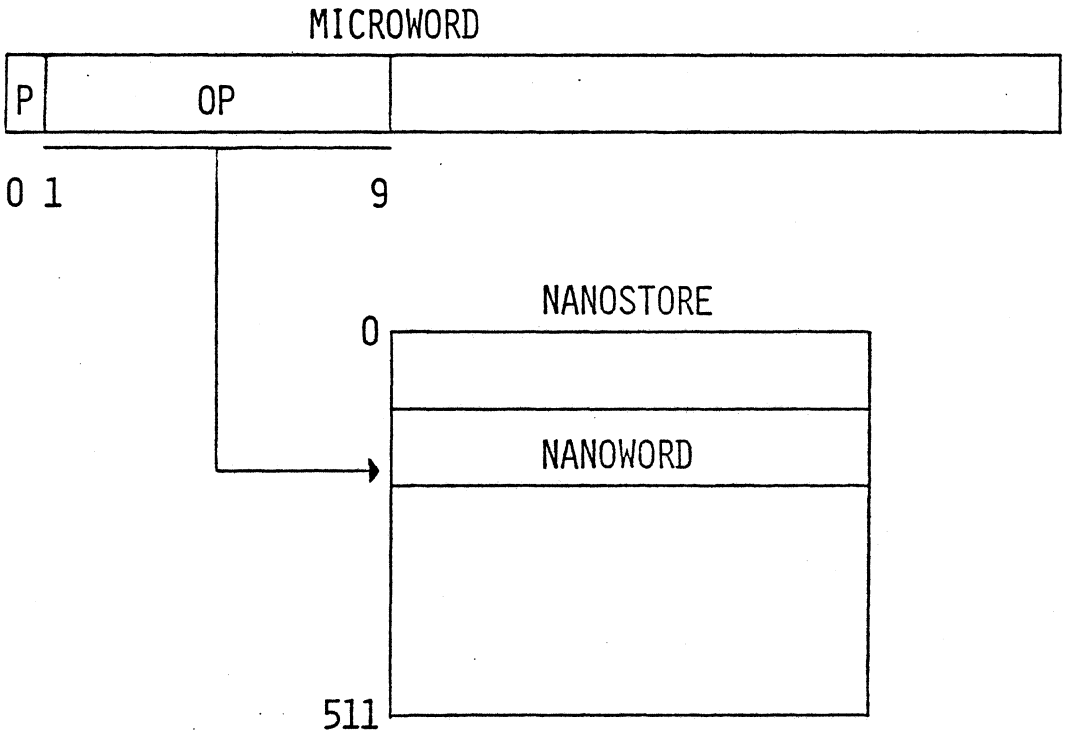
  11 LOGIC 4 MEMORY

  (4 RELEASED) VII - 16, III - 6

  IV - 4, VI - 4

M I C R O W O R D S / N A N O W O R D S

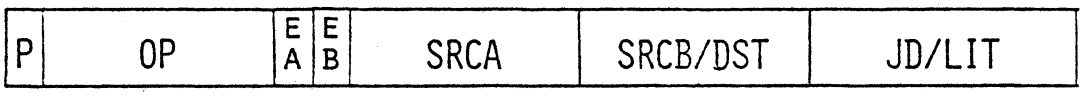
MICROINSTRUCTION = MICROWORD + NANOWORD



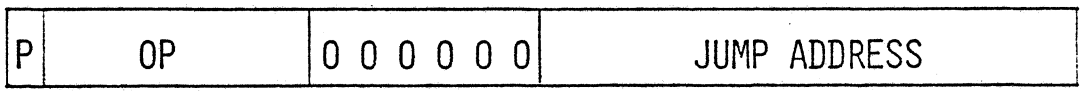
THE RELATIONSHIP BETWEEN A MICROWORD AND A NANOWORD IS ONE-TO-ONE, BUT THE SAME NANOWORD MAY BE USED BY MANY MICROWORDS.

M I C R O W O R D F O R M A T S

- DATA MANIPULATE/RELATIVE JUMP (+ 127, - 128)

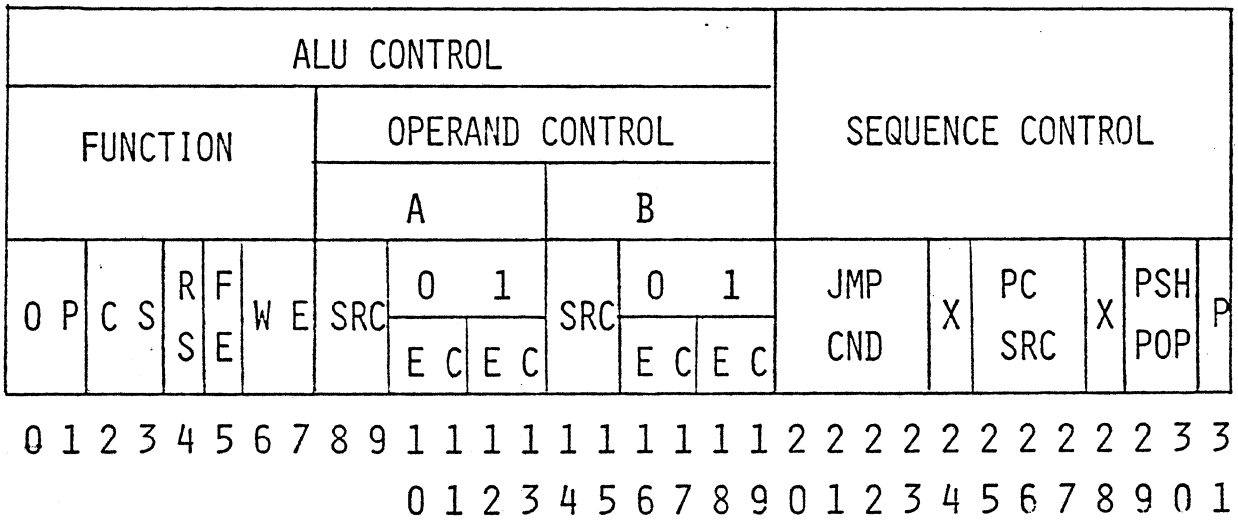


- FULL RANGE JUMP



- TEST WITH LITERAL/SHORT RELATIVE JUMP (+ 31, - 32)

N A N O W O R D F O R M A T



ALU FUNCTION

- ALU-OP - AND, OR, XOR, ADD
- ALU-CS - CARRY SELECT (0, 1, CARRY FLAG)
- ALU-RS - RIGHT SHIFT (ONE BIT POSITION)
- ALU-FE - FLAG UPDATE ENABLE
- ALU-WE - BYTE ENABLE FOR WRITING RESULT

ALU IN-GATING

- SRC - OPERAND SOURCE SELECT (WS, EXTERNAL, LITERAL)
- EC - ENABLE & COMPLEMENT CONTROLS

  00: OPERAND = ZEROS
  01: OPERAND = ONES
  10: OPERAND = OPERAND SOURCE
  11: OPERAND = ¬ OPERAND SOURCE

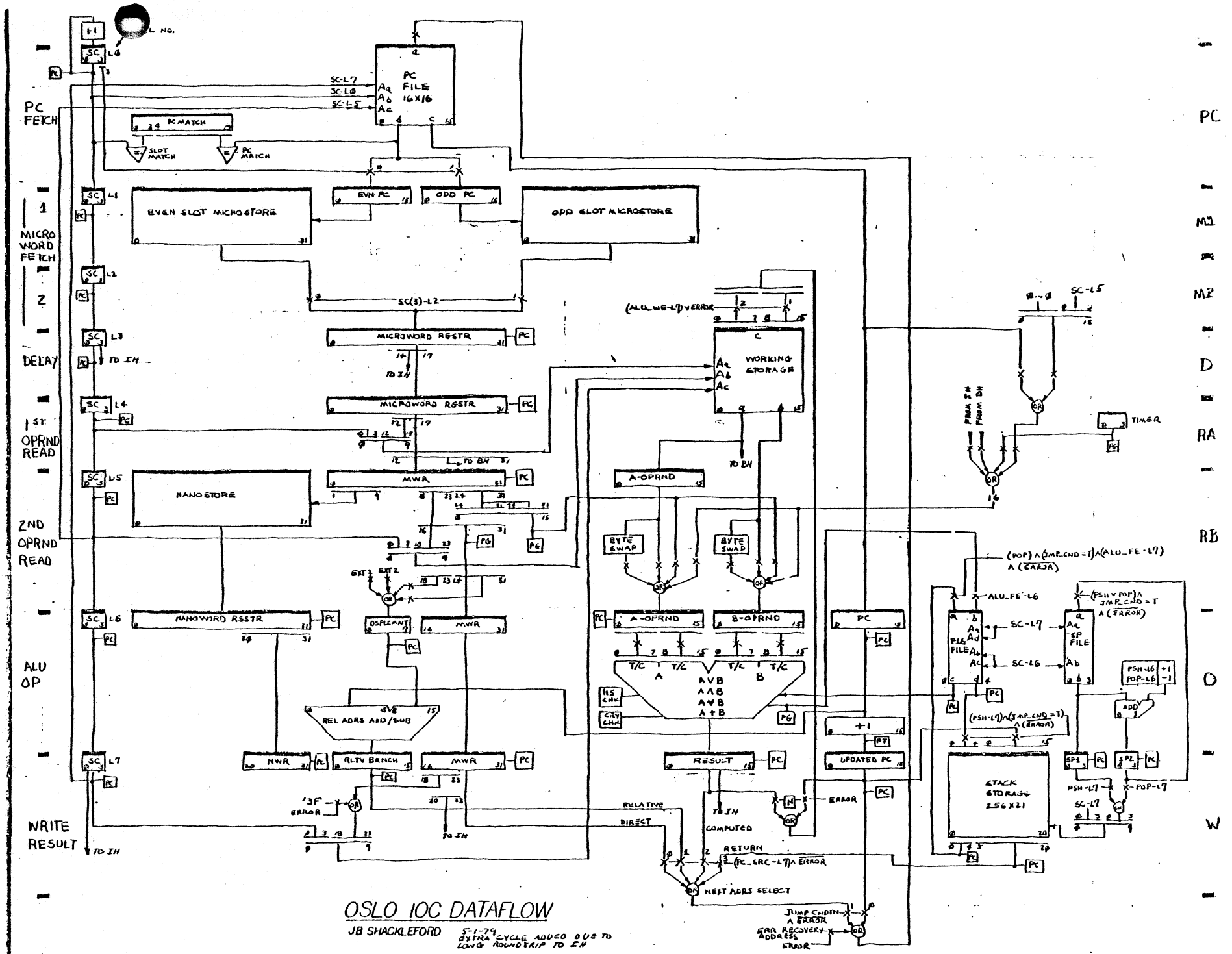
S E Q U E N C E C O N T R O L

- JMP-CND - JUMP CONDITIONS
  - ALWAYS
  - NEVER (NEXT SEQUENTIAL MICROWORD)
  - VARIOUS FLAG CONDITIONS

- PC-SRC - SOURCE OF NEXT PROGRAM COUNTER IF JUMP CONDITION IS SATISFIED

- PSH-POP - STACK CONTROL

  A PUSH OR A POP STACK OPERATION IS PERFORMED IF THE JUMP CONDITION IS SATISFIED

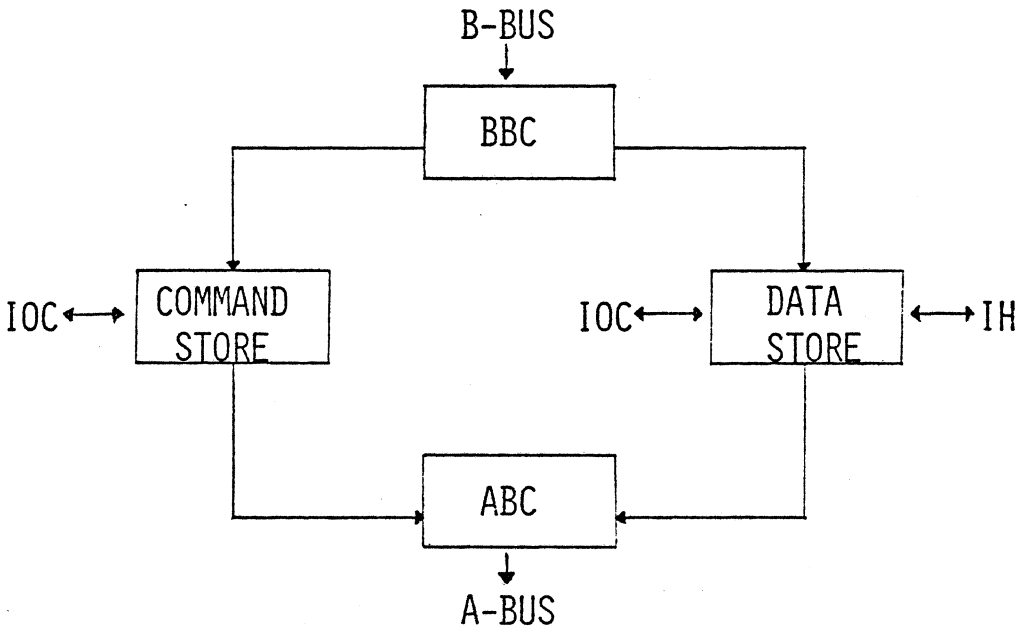


OSLO IOC DATAFLOW

JB SHACKLEFORD 5-1-79

EXTRA CYCLE ADDED DUE TO LONG ROUNDTRIP TO IH

B U S H A N D L E R (BH)



- ABC: A-BUS (LOCAL) CONTROLLER
- BBC: B-BUS (LOCAL) CONTROLLER

B U S H A N D L E R (BH)

- COMMAND STORE CHARACTERISTICS
  - IOC'S COMMUNICATION PATH TO CPU, MAINSTORE, ETC.
  - ASSEMBLY AREA FOR OUTGOING MESSAGES
  - BUFFER AREA FOR INCOMING MESSAGES
  - IOC INTERFACE WIDTH (2 BYTES)
  - ABC INTERFACE (8 BYTES)
  - BBC INTERFACE (8 BYTES)

- DATA STORE CHARACTERISTICS
  - ASSEMBLES AND ALIGNS I/O DATA
  - UPDATES DATA ADDRESS DURING DATA TRANSFER
  - SERVICES ONLY 'ACTIVE' INTERFACE HANDLERS IN A ROUND-ROBIN FASHION
  - CONTROL INFORMATION IS SETUP BY IOC
  - IOC INTERFACE WIDTH (2 BYTES)
  - IH INTERFACE WIDTH (2 BYTES)
  - ABC INTERFACE WIDTH (8 BYTES)
  - BBC INTERFACE WIDTH (8 BYTES)

B U S H A N D L E R (BH)

- CHIP COUNT

  44 LOGIC 13 MEMORY

- PN COUNT

  17 LOGIC 1 MEMORY

  (1ST CHIP 8/31) III

I N T E R F A C E H A N D L E R (IH)

- ONE PER CHANNEL

- PRIMARY DATA BUFFER IN IOP

  - 256 BYTES DEEP
  - 1 BYTE WIDE

- CIRCULAR BUFFER CONTROLLED BY POINTERS

  - IN
  - OUT
  - STOP

- PERFORMS TAG CONTROL FOR SELECTION, DATA TRANSFER, AND COMMAND CHAINING

- GIVES FAST RESPONSE TO DEVICE

- CHIP COUNT

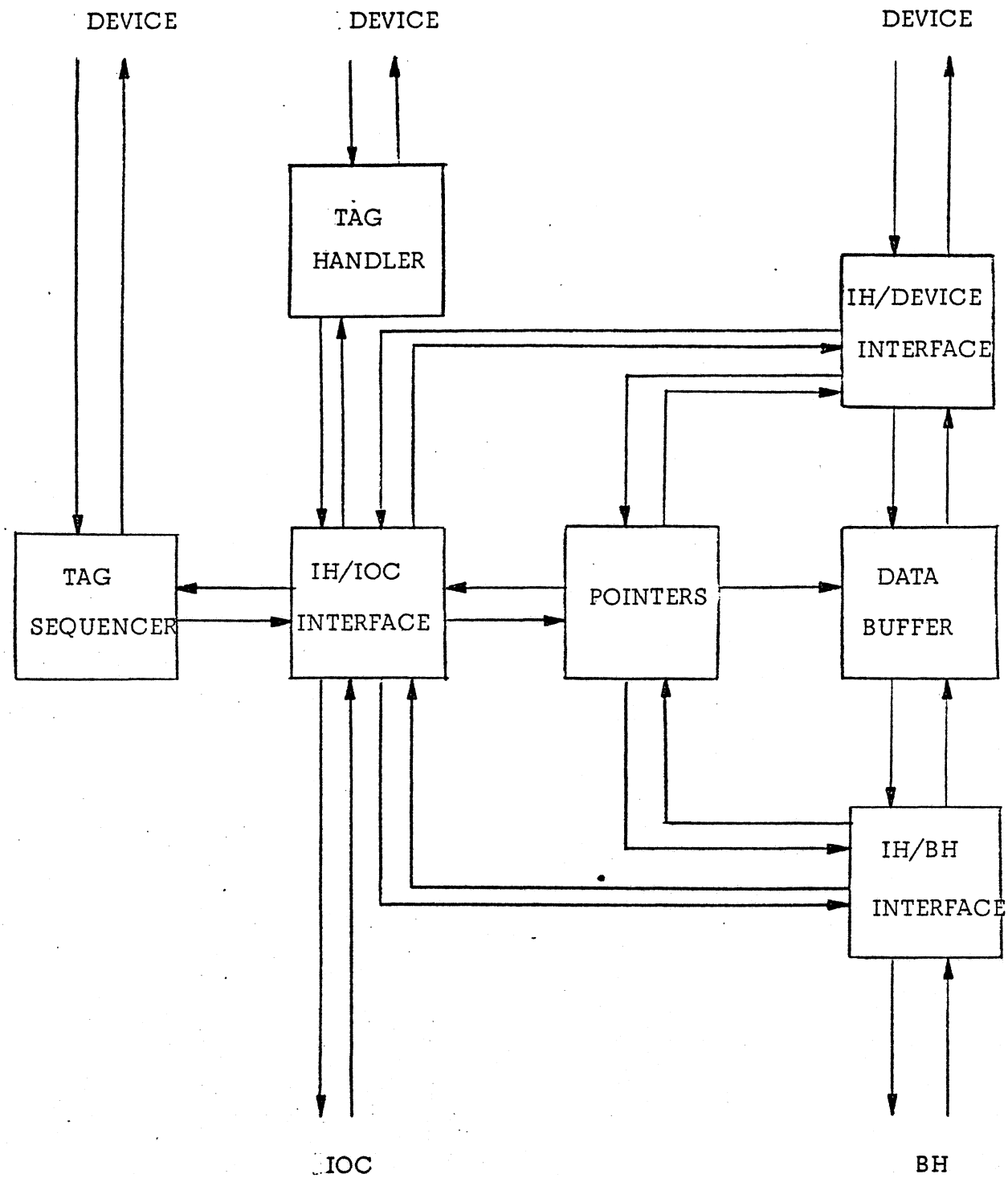
  9 LOGIC 1 MEMORY 4 LEVEL TRANSLATORS

- PN COUNT

  7 LOGIC 1 MEMORY 1 LEVEL TRANSLATOR

  (1ST CHIP 8/79) TYPE III

INTERFACE HANDLER



OSLO IOP - CHIP COUNT SUMMARY

	P/N	USAGE
IOC:		
LSI	12	31
RAM	4	30
BH:		
LSI	17	44
RAM	1	13
TOTAL ON MCC:		
LSI	28	74
RAM	5	43
	33	118
IH:		
LSI	7	9
RAM	1	1
LEVEL TRANSLATOR	1	4

I M L : I O C M I C R O C O D E L A N G U A G E

CHARACTERISTICS

- ASSEMBLY LANGUAGE GIVES LOW LEVEL CONTROL
  - ONE MICROINSTRUCTION → ONE MICROWORD

- LANGUAGE SYNTAX AND POWERFUL MICROINSTRUCTIONS GIVE HIGH LEVEL ADVANTAGES
  - ONE THOUGHT → ONE MICROINSTRUCTION
  - EASE OF CODING
  - EASE OF DEBUGGING
  - MAINTAINABILITY
  - SELF-DOCUMENTING

T Y P I C A L M I C R O C O D E P R O C E D U R E

```
/* * * * * * * * * * * * * * * * * * * * * * * * * * * * */
/*        SUBROUTINE TO MAP DEVICE NUMBER                */
/*              TO SUBCHANNEL ADDRESS                    */
/* * * * * * * * * * * * * * * * * * * * * * * * * * * * */

    SB-CH-GEN:  IF (DEVICE-# < MAX-SB-CH)
                   THEN GO TO NON-SHARED;

                /* GET SHARED SUBCHANNEL; AND ITS DISPLACEMENT*/
        SHARED: DISPLACEMENT ← ZEROS || DEVICE-#;
                DISPLACEMENT-R ← DEVICE-# & SB-CH-MASK;
                DISPLACEMENT ← DISPLACEMENT + DISPLACEMENT,
                   GO TO CALCULATE-ADR;

                /*MULTIPLY DEVICE NUMBER BY 32 */
    NON-SHARED: DISPLACEMENT ← DEVICE-# || ZEROS:
                DISPLACEMENT ← SHR (ZERO, DISPLACEMENT);
                DISPLACEMENT ← SHR (ZERO, DISPLACEMENT);
                DISPLACEMENT ← SHR (ZERO, DISPLACEMENT);

                /* ADD DISPLACEMENT TO BASE ADDRESS */
CALCULATE-ADR:  SB-CH-ADR2 ←* SBS-BASE-ADR2 + DISPLACEMENT;
                SB-CH-ADR1 ← SBS-BASE-ADR1 + HØØ + CIN,
                   RETURN;
```

M I C R O C O D E T O O L S

- ASSEMBLER (DEVELOPED BY ENGINEERING SOFTWARE)

  OPERATIONAL 7/79

- IOC SIMULATOR

  OPERATIONAL 5/79

- IOP SIMULATOR

  OPERATIONAL 10/79

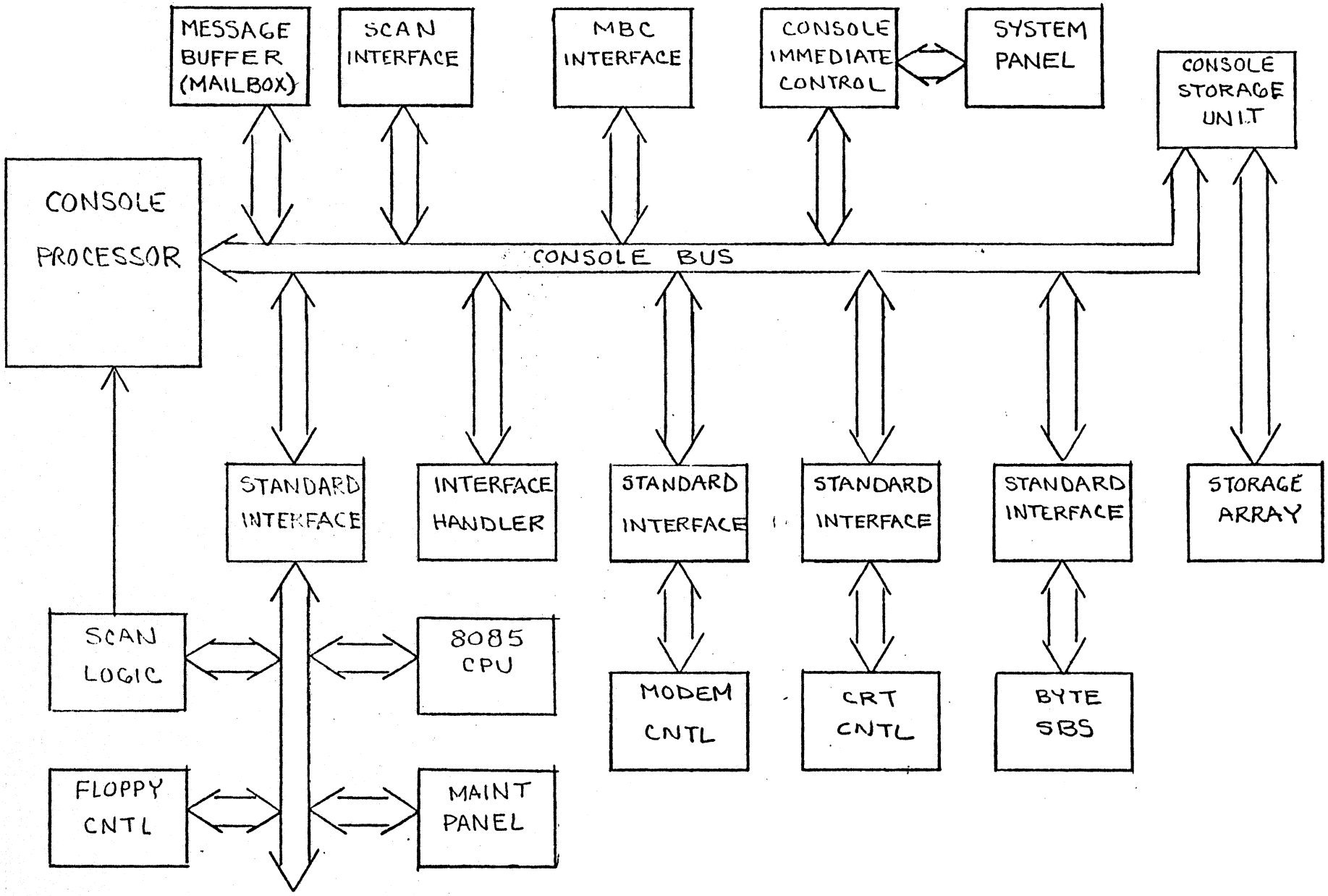
OSLO IOP PERFORMANCE

	V/6	PROCESSOR 3033 (NORMAL/RPQ)	V/7	V/8 (EST.)	OSLO (EST.) (16 SLOTS/8 SLOTS)
SIO (μSEC)	30 - 120	30 - 120	30 - 120	30 - 120	30 - 120
SIOF (μSEC)	1 - 2	10/5	1.5	1	7/3.5
PRIMARY INTERRUPT (μSEC)	3.8	15.2/7.6	3.5	3.2	1
SECONDARY INTERRUPT (μSEC)	105	15.2/ -	105	105	-
COMMAND CHAINING (μSEC)	11 - 15		10 - 13.5	9 - 12	12/6
BANDWIDTH:					
CHANNEL (MB/S) (SINGLE CHANNEL/QUAD OR PAIR)	1.9/3.8		2.1/4.3	2.4/4.8	15/ -
AGGREGATE (MB/S)	12		18	20	> 50
CYCLE TIME (NS)	32.5		29	26	20

DC 8/6/79

OSLO IOP

- OVERVIEW
- I/O CONTROLLER (IOC)
- BUS HANDLER (BH)
- INTERFACE HANDLER (IH)
- MICROCODE
- PERFORMANCE



CONSOLE

SYSTEM DIAGRAM

C O N S O L E O R G A N I Z A T I O N

FUNCTIONAL UNITS

- CONSOLE PROCESSOR
- CONSOLE STORAGE UNIT
- SCAN INTERFACE
- MESSAGE BUFFER (MAILBOX)
- MBC INTERFACE
- CONSOLE IMMEDIATE CONTROL
- CRT/KEYBOARD CONTROL
- MODEM CONTROL
- FLOPPY DISC CONTROL
- 8085 MICROPROCESSOR
- MAINTENANCE PANEL
- SYSTEM PANEL
- BYTE SBS

8/7/79 PD

C O N S O L E P R O C E S S O R

- 8 SLOT VERSION OF IOP UNIT

  SLOT #

  Ø - 37Ø CPU

  1 - BYTE MVX 1

  2 - MULTIDEVICE CONTROLLER

  3 - CHANNEL

  4 - TIMER/SAM

  5 - BYTE MVX 2

  6 - FLOPPY DISC/HARD DISC

  7 - MBH

- DIFFERENT MICROCODE FOR EVEN SLOT
  ODD SLOTS/SHARE CODE

- NO ADDITIONAL PART NUMBERS REQUIRED

8/7/79 PD

C O N S O L E 3 7 Ø C P U

FEATURES

- EXECUTES (83) OF THE IBM 37Ø INSTRUCTION SET

- CONTAINS

  DYNAMIC ADDRESS TRANSLATION

  CPU TIMER

  EC MODE OPERATION

  2-8 MEGABYTES OF MAINSTORE

  1 CHANNEL WITH 16 SUBCHANNELS

- DEVICES ACT LIKE INTEGRATED CONTROL UNITS WITH DMA

- I/O DOESN'T DEGRADE THE PROCESSOR PERFORMANCE

8/7/79 PD

CONSOLE 370 CPU

MICROCODE REQUIREMENTS

- CONSOLE 370 INSTRUCTIONS

  1750 MICROINSTRUCTIONS

- SYSTEM CONTROL

DAT	100 MICROINSTRUCTIONS
CPU, TIMER	50
RESETS, IPL	350
INTERRUPTS	400
MACHINE CHECKS	300
MISCELLANEOUS	122
TOTAL	3072 MICROINSTRUCTIONS

C O N S O L E 3 7 Ø C P U

PERFORMANCE

- TYPICAL INSTRUCTION TIMES

INSTRUCTION	TIME (μSEC)	
L RX	2.4	
LR RR	1.4	
ST RX	3.3	
BC RX	1.6	BR NOT TAKEN
	2.4	BR TAKEN
A RX	3.Ø	
C RX	3.2	

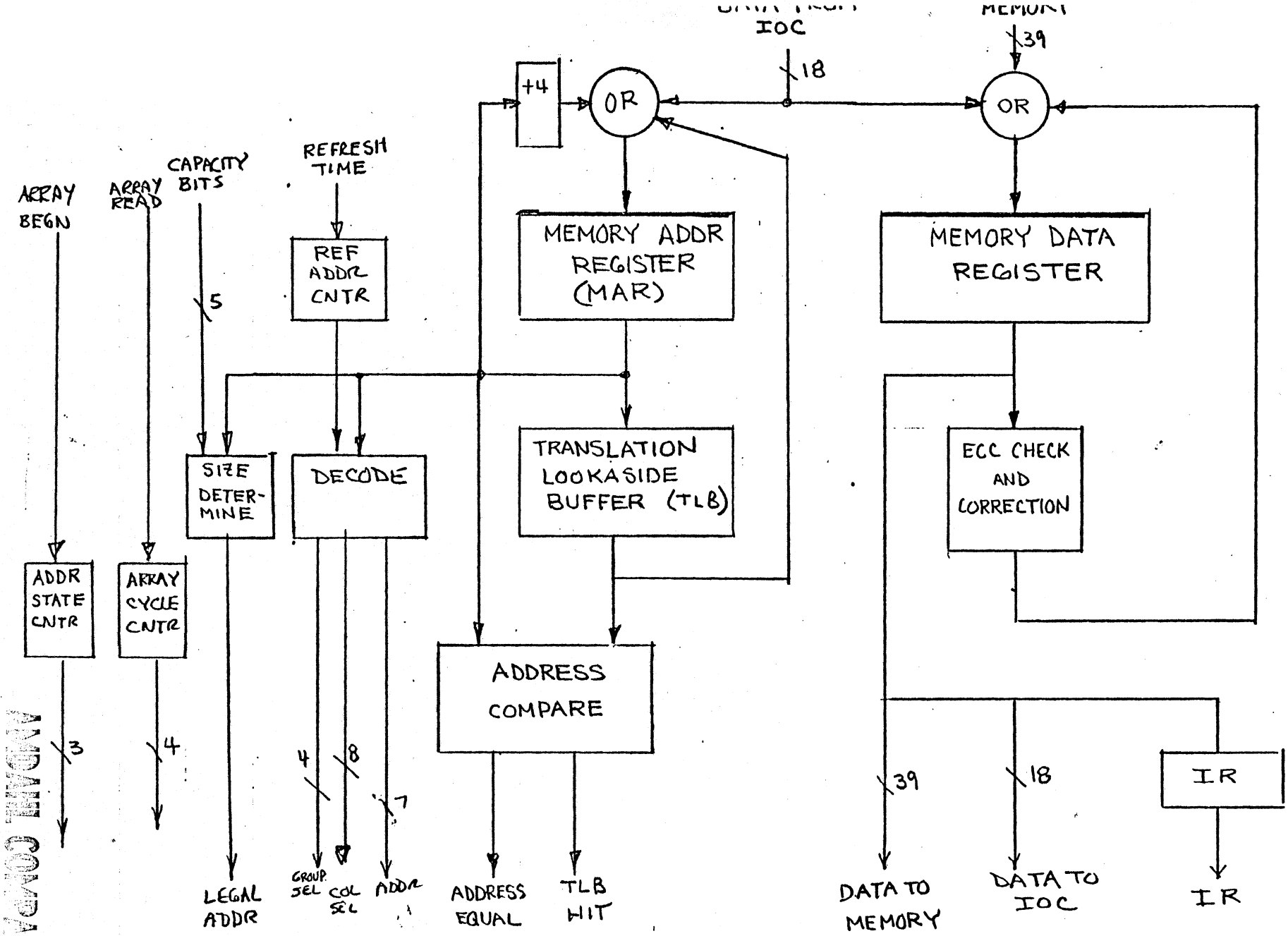
- OVERALL INSTRUCTION RATE

SINGLE ADDRESS TRANSLATE - 3.2 μSEC
AVERAGE INSTRUCTION TIME - 2.5 μSEC

- MIPS / 20 NS CYCLE TIME

TABLE HITS	MIPS
1ØØ%	Ø.4
95%	Ø.35
9Ø%	Ø.32

8/7/79 PD



CONSOLE STORAGE UNIT

8/3/79

CONSOLE STORAGE UNIT

FUNCTIONAL UNITS

- MEMORY DATA REG
- ECC CHECKING & CORRECTION
- MEMORY ADDRESS REG (MAR)
- TRANSLATION LOOKASIDE BUFFER
- ADDRESS COMPARATORS
- ARRAY STATE COUNTER
- ARRAY CYCLE COUNTER
- REFRESH ADDRESS COUNTER

PERFORMANCE

FULL WORD (32 BITS) READ/WRITE	500 NSEC
HALL WORD BOUNDARY FW RD	820 NSEC
I-FETCH	540 NSEC
HALF WORD READ OR I-FETCH	340 NSEC
BAND WIDTH (AT 2ONS CYCLE)	≈ 1.95 M WORDS/SEC

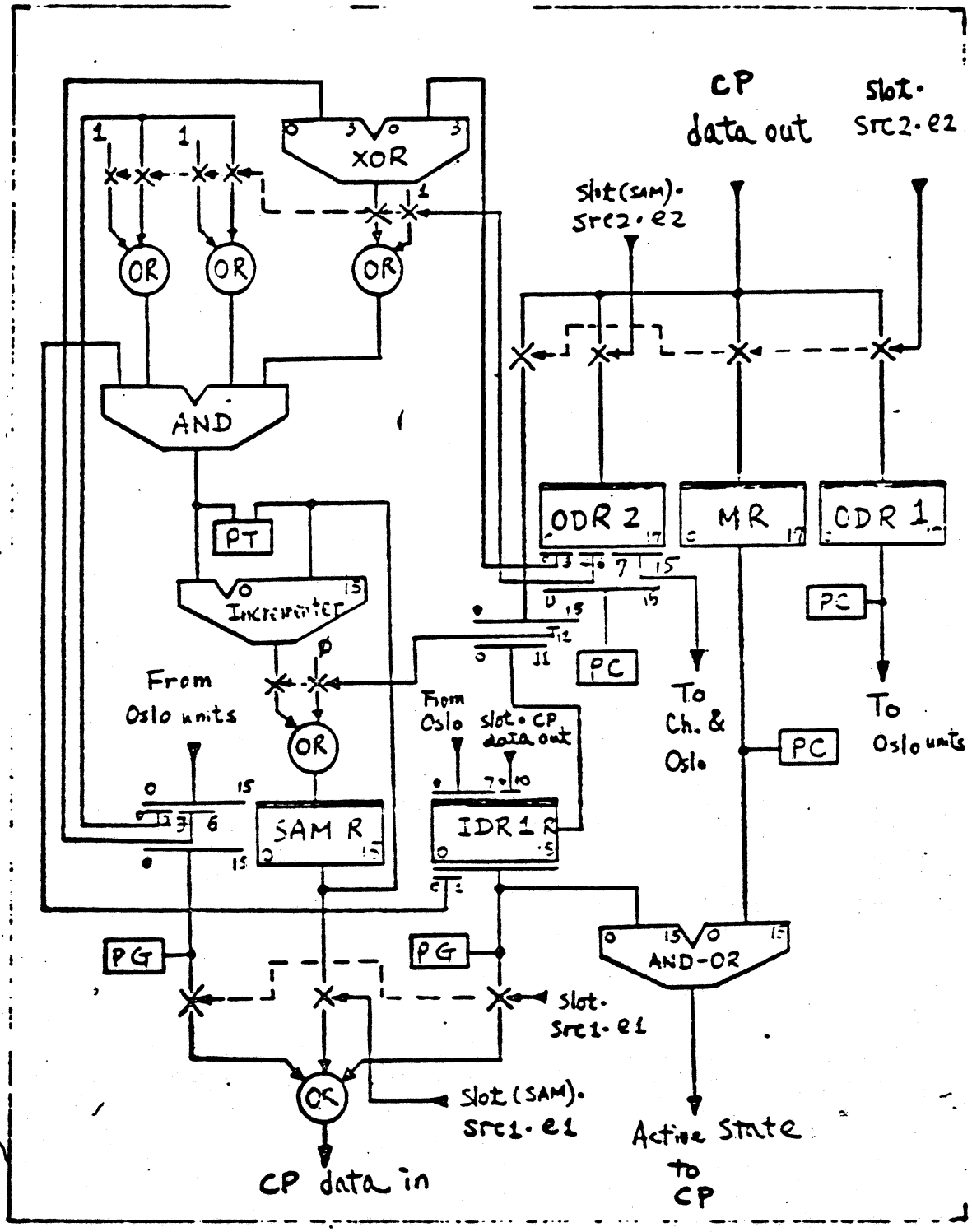
C O N S O L E S T O R A G E U N I T

- DESIGN USES 6 PART NUMBERS ON 16 CHIPS

- BLC'S USE 3 PART NUMBERS ON 13 BOARDS
  TO PROVIDE A MAXIMUM OF 8 MBYTES

- STATUS
  2 PART NUMBERS RELEASED

8/7/79 PD



CIC Data Flow Diagram

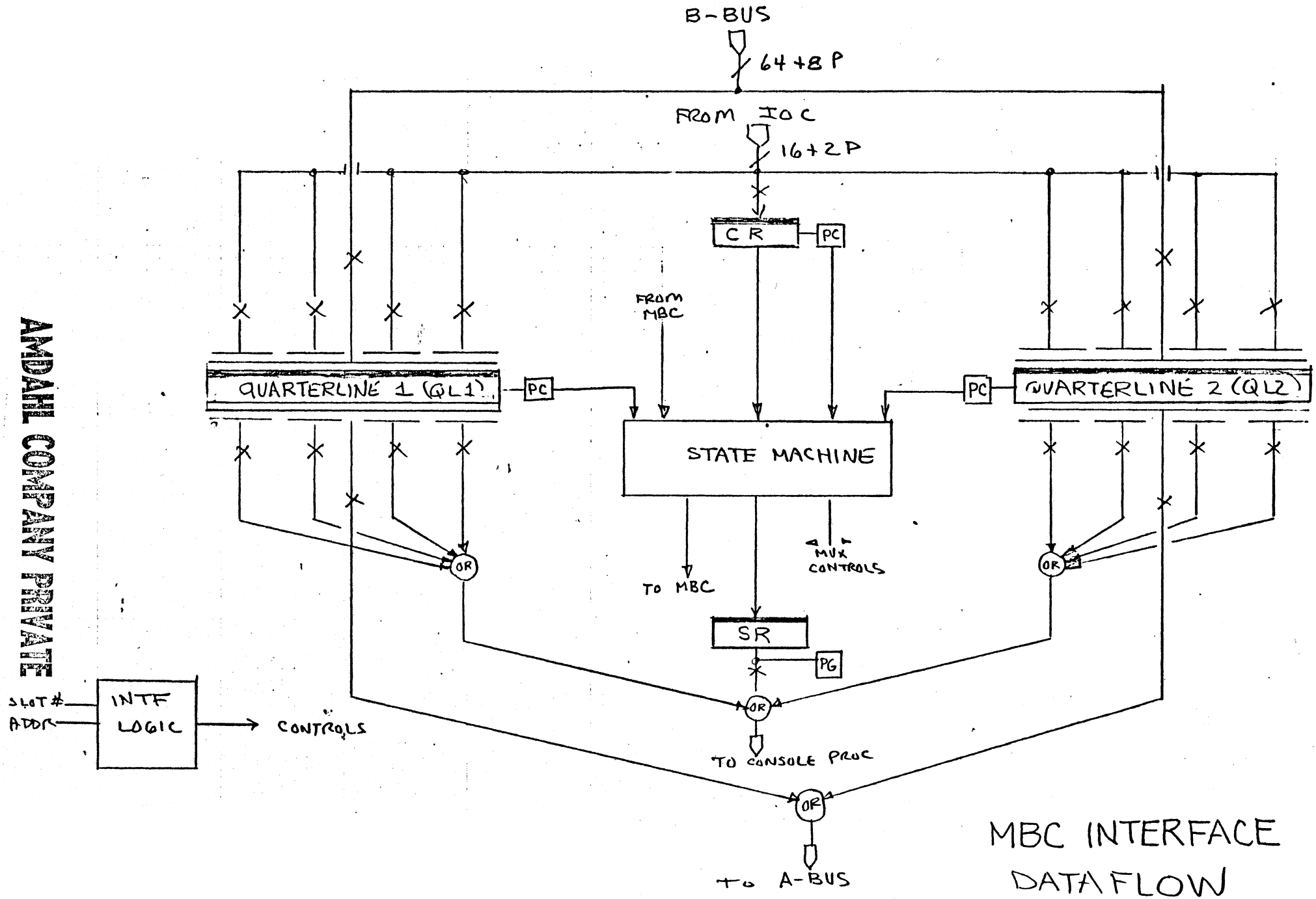
CONSOLE IMMEDIATE CONTROL (CIC)

- PROVIDES HARDWARE INTERFACE BETWEEN CONSOLE AND THE OSLO SYSTEM
- USED TO PERFORM CONTROL FUNCTIONS OTHER THAN BUS MESSAGES AND SCAN
- DESIGN REQUIRES (2) PART NUMBERS AND 2 PARTS
- STATUS
  - BOTH P/N'S IN DESIGN

MESSAGE BUFFER (MAILBOX)

FUNCTION

- ACTS AS AN INTERCONNECTION LINK BETWEEN SLOTS
- EACH SLOT HAS ITS OWN AREA IN THE MAILBOX
- COMPOSED OF FAST RAM'S IN A 256 X 16 ORGANIZATION
- ONLY ONE SLOT AT A TIME CAN ACCESS MAILBOX



MBC INTERFACE DATA FLOW

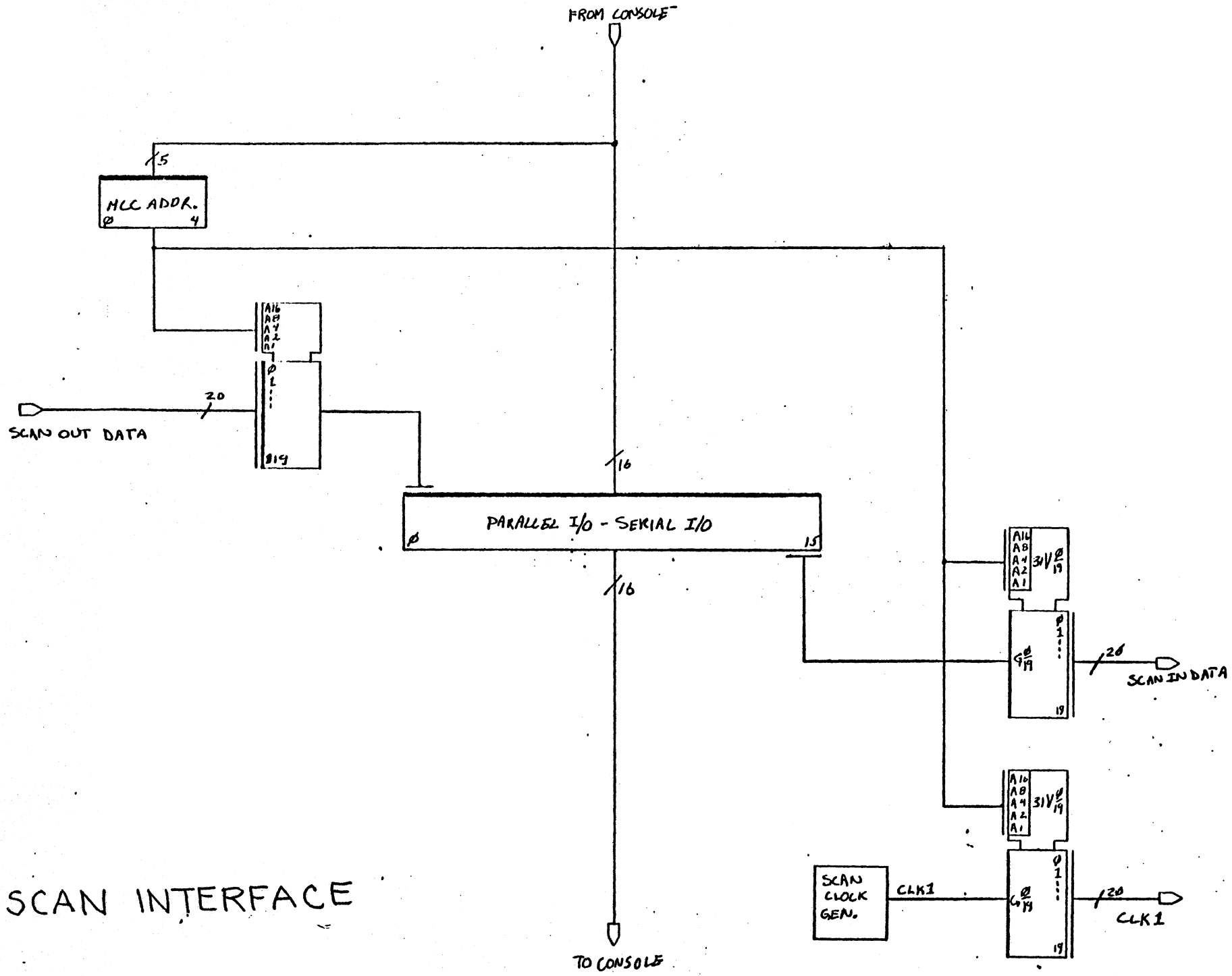
MBC INTERFACE

- A MINIMAL HARDWARE DESIGN

- EXTENSIVE USE OF MICROCODE
  - TO PROVIDE OSLO BUS INTERFACE
  - TO PROVIDE BYTE MUX COMMUNICATION
  - TO PROVIDE SOFTWARE COMMUNICATION
  - PROVIDES CONSOLE ASSIST FUNCTIONS

- DESIGN WILL USE (1) PART NUMBER (8) TIMES

- STATUS
  - CHIP PARTITIONING IN PROCESS



SCAN INTERFACE

SCAN INTERFACE

- MINIMAL HARDWARE DESIGN WITH HEAVY USE OF MICROCODE

- USES STANDARD I/O COMMANDS FROM CONSOLE SOFTWARE TO
  - WRITE INTO LATCHES/RAM'S
  - READ FROM LATCHES/RAM'S

- DESIGN USES ONE PART NUMBER (2) TIMES

- STATUS
  - CHIP DESIGN IN PROCESS

NON-LSI FUNCTIONS (BLC'S)

- FUNCTIONS
  - STANDARD INTERFACE
  - 8085 MICROPROCESSOR
  - MODEM CONTROL
  - CRT/KEYBOARD CONTROL (1 CRT/KEYBOARD + 3 OPTIONAL)
  - BYTE/SBS (2 BYTE MUX)
  - INTERFACE HANDLER (2 EA.)
  - MEMORY ARRAY (UP TO 10 BDS 0.5 - 8 MBYTES)

- NUMBER OF BLC'S = 26

- STATUS
  - NOT STARTED

CONSOLE MCC SUMMARY

	P/N'S	CHIPS
IOC	0	69
CSU	6	16
SCAN	1	5
MBC	1	8
CIC	2	2
CLK CHIP	0	1
	10	101

OEM STATUS

- FLOPPY DISK SELECTED
  - CDC 9406-3 PRIME
  - SHUGART 851 SECOND
- CDC DRIVES IN-HOUSE (2)
  - FUNCTIONAL TESTS BY 1/1/80
- SHUGART DRIVES ON ORDER
- TERMINAL SELECTED
  - ZENTEC ZMS-90

    *EMULATES 3274-1B/3278-1
- SECOND SOURCES

  A) AMDAHL BUILT ZMS-90

  B) DELTA DATA