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AMDAHL 4705
Communications Processor
Principles of Operation

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REVISION NOTICE
This is the second edition. The publication number of the first edition was P1056 0-01A.

ABSTRACT
This manual describes the principles of operation and system features for the Amdahl 4705 Communications Processor.

The topics covered include machine organization and configuration, operational and system characteristics.

READER COMMENT FORM
A reader comment form is provided at the end of this manual. If this form is not available, comments and suggestions may be sent to Amdahl Corporation Technical Publications Department, Mail Stop 325, P.O. Box 470, Sunnyvale, CA 94086. All comments and suggestions become the property of Amdahl Corporation.

PREFACE

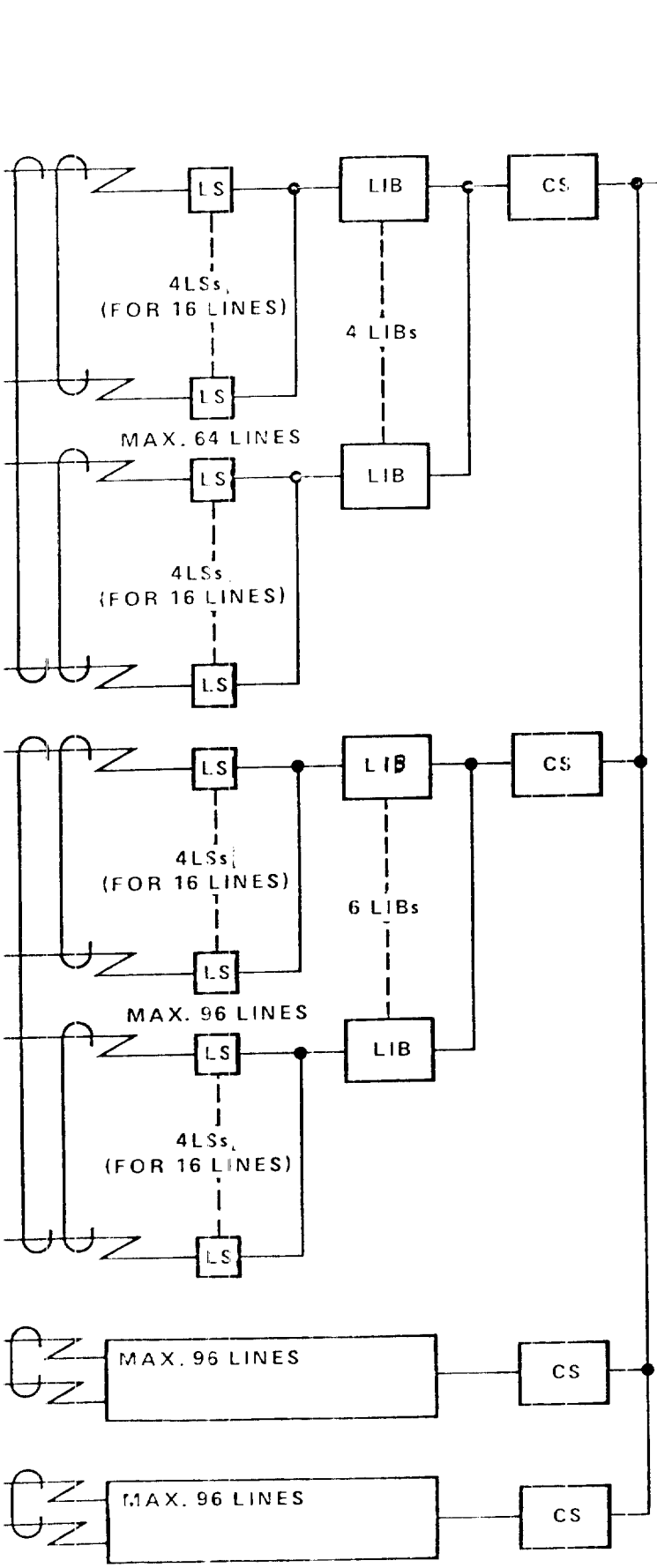
This manual describes the differences between the IBM 3705-II Communications Processor (CP) and the Amdahl 4705 CP. It is assumed that the reader has knowledge of the 3705-II in that the Amdahl 4705's hardware architecture is compatible with that of the Release 4 fifth edition), of the IBM 3705 Principles of Operation.

CONTENTS

CHAPTER 1

DIFFERENCES IN HARDWARE FEATURES

- CS1 (Type 1 Communication Scanner): Not supported.
- CA1 (Type 1 Channel Adapter) : Not supported.



NOTE: 'May have up to 4 CAs installed

KEY

CC: Central Control
MS: Main Storage
AB: Attachment Base
CA: Channel Adapter
TCS: Two Channel Switch
CS: Communication Scanner
LIB: Line Interface Base
LS: Line Set

A02312

Fig. 1.1 4705 Logic block diagram (Maximum configuration)

CHAPTER 2

CENTRAL CONTROLLER

This chapter describes the differences between the 3705-II and 4705 with regard to central controller

Table 2.1 Symbols in "Difference" column
(in Table 2.2, 3.1, 4.1, 5.1)

Symbol	3705-II	4705	Description
A	x	o	The function is supported by 4705 but not by 3705-II IBM software * can be used in the 4705 (compatible).
IN	o	4705 3705-II	The 4705 function is equivalent or includes the 3705-II function. IBM software * can be used in the 4705 (compatible).
I	o	x	The function is supported by the 3705-II but not by the 4705, or the definition is different.

*: The term "IBM software" indicates the following program categories:

EP (Emulation Program)

NCP (Network Control Program)

PEP (Partitioned Emulation Program)

Table 2.2 Differences between 3705-II and 4705 with regard to central controller

Item No.	Item	Difference	3705-II	4705	Remarks 3705-II P00 page No., etc.)
1	Main storage capacity Basic capacity Expanded capacity Maximum capacity Values in parentheses are those that can be read by IN X'70'.	IN	32K bytes (32K bytes) 32K bytes (32K bytes) 256K bytes (256K bytes)	64K bytes 64K bytes 512K bytes Note: The maximum capacity differs by model.	1-3 Storage
2	Full-bit configuration (data composed of bytes X, 0, and 1) 16 bits (byte X: Nothing) 18 bits (byte X: 2 bits) 20 bits (byte X: 4 bits)	 IN IN A	 Without extended addressing With extended addressing Not defined	 Defined as 4705 BC mode Defined as 4705 EC mode See Appendix B	3-1 Storage addressing Basic control mode Extended control mode
3	Instruction execution time			See Appendix A	4-2 Figure 4.1
4	IN X'00 ∿ 1F' Bit X.4 ∿ X.5	A	Not defined	Not defined	Bits X4 and X5 of each GR

Table 2.2 - continued

<table>
<tr><th>Item No.</th><th>Item</th><th>Differ-ence</th><th>3705-II</th><th>4705 BC mode</th><th>4705 EC mode</th><th>Remarks 3705-II P00 page No., etc.)</th></tr>
<tr><td>5</td><td>OUT X'00 ∿ 1F'
Bit X.4 ∿ X.5</td><td>A</td><td>Not defined</td><td>Not defined</td><td>Bits X4 and X5 of each GR</td><td></td></tr>
<tr><td rowspan="2">6</td><td>IN X'70'
Bit 0.1</td><td>A</td><td>Not defined</td><td>Not defined</td><td>1024K bytes</td><td rowspan="2">B-37</td></tr>
<tr><td>IN X'70'
Bit 0.2</td><td>A</td><td>Not defined</td><td>Not defined</td><td>512K bytes</td></tr>
<tr><td>7</td><td>IN X'71'
Bit X.4 ∿ X.5</td><td>A</td><td>Not defined</td><td>Not defined</td><td>Bits 0 and 1 of digit A</td><td>B-37</td></tr>
<tr><td>8</td><td>IN X'74'
Bit X.4 ∿ X.5</td><td>A</td><td>Not defined</td><td>Not defined</td><td>Bits X4 and X5 of LAR</td><td>B-38</td></tr>
<tr><td rowspan="3">9</td><td>IN X'75'
Bit X.4 ∿ X.5</td><td>A</td><td>Not defined</td><td>Not defined</td><td>Bits X4 and X5 of LER</td><td rowspan="3"></td></tr>
<tr><td>IN X'75'
Bit X.6 ∿ 0.5</td><td>A</td><td>Not defined</td><td>Bits X5 and X6 of LER (lagging error register) Upper address when a 1 - or 2 - bit error occurs in MS</td><td>Same as on the left</td></tr>
<tr><td>IN X'75'
Bit 0.6 ∿ 0.7</td><td>A</td><td>Not defined</td><td>MS type
<table><tr><th>0.6</th><th>0.7</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>Not defined</td></tr><tr><td>0</td><td>1</td><td>MS type of this CCP</td></tr><tr><td>1</td><td>0</td><td>Not defined</td></tr><tr><td>1</td><td>1</td><td>Not defined</td></tr></table></td><td>Same as on the left</td></tr>
</table>

Note: BC = Basic Control; EC = Extended Control

Table 2.2 - continued

Item No.	Item	Difference	3705-II	4705 BC mode	4705 EC mode	Remarks 3705-II -P00 Page No., etc.)
	1.1 ∿ 1.7	A	Not defined	Syndrome bits 0 ∿ 6: Indicate the error bit position in code when 1 bit errors occur in MS.	Same as on the left	
10	IN X'76' Bit 0.7	I	Remote Prog. loader L1	FDC L1	Same as on the left	B-38 (*)
11	IN X'77' Bit 1.1	I	Remote Prog. loader L3	FDC L3	Same as on the left	B-38 (*)
12	IN X'7E' Bit 1.5	A	Not defined	1-bit error L1 (ECC corrected): L1 interrupt indicates occurrence of 1-bit error	Same as on the left	B-40
	Bit 1.7	A	Not defined	Program trace L1: L1 interrupt occurs at each instruction execution in L2-5.		
13	IN X'7F' Bit 0.5	A	Not defined	ANS L3: L3 interrupt caused by ANS signal from external device.	Same as on the left	B-41
14	OUT X'71' Bit X.4 ∿ X.5	A	Not defined	Not defined	DR1 Bit X4 ∿ X5	B-41
15	OUT X'72' Bit X.4 ∿ X.5	A	Not defined	Not defined	DR2 bit X4 ∿ X5	B-41

Table 2.2 - continued

Item No.	Item	Difference	3705-II	4705 BC mode	4705 EC mode	Remarks 3705-II -P00 page No., etc.)
16	OUT X'73' Bit X.6 ∿ X.7	A	Not defined	Not defined	Storage Key Address SKA bit X6 ∿ X7	B-41
17	Out X'77' Bit 0.3	A	Not defined	Reset ANS L3	Same as on the left	B-41
	Bit 0.4	A	Not defined	Set ANS Busy		
	Bit 0.5	A	Not defined	Reset ANS Busy ANS Busy: Signal to indicate ANS execution to external device.		
18	OUT X'78 Bit 0.0 Bit 0.1 Bit 1.0 Bit 1.1 Bit 1.2 Bit 1.5 Bit 1.6	I	Refer to P00, I3705II	Set EC mode (Extended control) Reset EC mode MS force bit LR force bit IR force bit Force modifier bit 1 Force modifier bit 2	Same as on the left	B-42
19	OUT X'79 Bit 0.3	I	Set FET Diagnostic mode	Not defined	Not defined	B-43
20	OUT X'7E' Bit 1.0	A	Not defined	Set mask bit for 1 bit error L1	Same as on the left	B-49

Table 2.2 - continued

Item No.	Item	Difference	3705-II	4705 BC mode	4705 EC mode	Remarks (3705-II-P00 page No., etc.)
21	OUT X'7F' Bit 1.0	A	Not detined	Reset mask bit for 1 bit error L1	Same as on the left	B-49

*: FDC for CP diagnosis as additional functions. The FDC hardware interface is the same as that of the RPL

CHAPTER 3

TYPE 2 COMMUNICATION SCANNER AND LINE UNIT

This chapter describes the differences between the 3705-II and 4705 with regard to Type 2 Communication scanner CS2 and LUT (Line Unit).

Table 3.1 Differences between 3705-II and 4705 CS2 and LUT

Item No.	Item	Difference	3705-II	4705	Remarks 3705-II P00 page No., etc.)
1	Local storage	IN	96 words x 48 bits (46 + 2P)	128 words x 54 bits (51 + 3P)	7-1 Local Storage
2	Line address of line address bus	IN	8 bits	7 bits	7-3 Scan Addressing
3	Number of line addresses scanned	IN	96	96	7-3 Scan Counter

Note: See Table 2.1 for symbols in the "Difference" column.

Table 3.1 - continued

Item No.	Item	Difference	3705-II	4705	Remarks 3705-II P00 page No., etc.)
4	Scan limit example	IN	When the scan limit is B'11', 4 times as many addresses are scanned as without the scan limit (96 lines).	When the scan limit is B'11', 8 times as many addresses are scanned as without the scan limit (96 lines).	7-3 Upper Scan Limit
5	Scan limit list	IN	See below	See below	7-4 Fig. 7.2 Upper scan limit
6	Scan period of Address substitution	IN	12.8 μs	11.6 μs	7-4 Address substition

Item 5 detail:

Upper scan limit	Number of interfaces scanned	Interface addresses scanned	Interface addresses not scanned	Scan period (μs)
3705-II				
00	96	Addr 0∿F,LIB1∿6	-	153.6
10	48	" ,LIB1∿3	Addr 0∿F,LIB4∿6	76.8
11	16	" , LIB1	" ,LIB2∿6	25.6
01	8	Addr 0∿7, LIB1	Addr 8∿F,LIB1 and Addr 0∿F,LIB2-6	12.8
4705				
00	96	Addr 0∿F,LIB1∿6	-	185.1
10	48	" ,LIB1∿4	Addr 0∿F,LIB5∿6	92.5
11	16	" ,LIB1	" ,LIB2∿6	23.1
01	8	Addr 0∿7,LIB1	Addr 8∿F,LIB1 and Addr 0∿F,LIB2∿6	11.6

Note: See Table 2.1 for symbols in the "Difference" column.

Table 3.1 - continued

Item No.	Item	Difference	3705-II	4705	Remarks 3705-II P00 page No., etc.)
7	ICW	IN	46 bits + 2 parity bits (96 ICWs)	51 bits + 3 parity bits (128 ICWs)	7-5 Interface Control Word
8	ICW Input/Output instruction	IN	Input X'44', X'45', and X'47' Output X'43', X'44', X'45', X'46', and X'47'	Input X'44', X'45', X'47', and X'48' Output X'43', X'44', X'45', X'46', X'47' X'48'	7-5 ICW Modification
9	ICW bit 3 (Modem check)	IN	1. DR Off PCF X'5', 'X7', X'8',X'9', X'A', X'B', X'D' X'C', X'D', X'E'	1. DR Off PCF X'5', X'7', X'8', X'9', X'A', X'B',	7-6 Bit 3 Modem Check
		IN	2. CS Off PCF X'9', X'A', X'B', X'D'	2. CS Off PCF X'9', X'A', X'B', X'C', X'D', X'E'	
		I	3. TTY echo check detection	3. None (Not supported)	
10	ICW drawing	IN	Fig. 7.4	See Appendix C Fig. 7.4	7-7 Fig. 7.4
11	ICW bits 34 ∿ 36	IN	Used as SDLC counter.	Used as the SDLC counter, and as the start-stop 10-bit space counter.	7-8 ICW Bits 34 ∿ 36
12	ICW bit 37	IN	Used by SDLC. Used by the	SDLC, and the start-stop 10-bit space counter (ICW bits 34 ∿ 37 are used).	7-8 ICW Bit 37
13	ICW bit 39	A	Reserved	Does not set ICW bit 3 (Modem Check) when this bit is '1'. Sets PCF = 9 even when PCF = 8 and CS is OFF.	7-9 ICW Bits 39 ∿ 40

Note: See Table 2.1 for symbols in the "Difference" column.

Table 3.1 - continued

Item No.	Item	Difference	3705-II	4705	Remarks (PDD page No., etc.)
14	ICW bit 52	A	None	Specifies 1-bit/10-bit Space detection for receive break. 1: 10-bit space supervision 0: 1 bit space supervision	7-9
15	ICW bit 53	A	None	Sets to CS2 wrap mode when this bit is 1. Data is looped in the CS2.	7-9
16	LCD state X'1'	A	Reserved	Start-stop 8/6 bit control This state is for start-stop interfaces with an 8/6 format (that is, 1 start bit, 6 data bits, and 1 stop bit). When a character is sent to an interface, the 6 data bits must be placed in bits 2 ∿ 7 of the PDF field as shown below. Characters received from the interface are in the same format when the scanner requests a character service interrupt. PDF bit positions 0 1 2 3 4 5 6 7 Character bits 0 0 X6 X5 X4 X3 X2 X1	7.9 LCD State X'1'
17	LCD state X'E'	A	Reserved	Enables BSC with arbitrary 5-8 unit SYN codes specified by OUT X'48'	7.10 LCD State X'E'

Note: See Table 2.1 for symbols in the "Difference" column.

Table 3.1 - continued

Item No.	Item	Difference	3705-II	4705	Remarks (3705-II PO page No., etc.)
18	LCD state X'F'	I	See 7.10, "LCD State X'F'".	Sets LCD = F when Set mode/ transmission/reception specification error for line address or data in bus parity errors are detected.	7.10 LCD State X'F'
19	PCF state X'1'	I	With data rate selector bit	Without data rate selector bit	7.11 PCF State X'1'
20	LCD state X'1'	A	Reserved	Start-Stop 8/6	7.11 PCF State X'7'
21	PCF state X'E'	A	Not used	Transmission completion RS ON	7.12 PCF State X'9'
22	PCF state X'E'	A	Not used	Same as PCF X'D' except that PCF X'E' is retained.	7.13
23	SDF bit 2 in Set mode	A	Not used	SDF bit 2: Send Data Control (SDC) Reverses all transmission data polarities by setting this bit to 1 in Set mode.	7.13 SDF Bits 0 ~ 2
24	Feedback Check caused by SDF bits 5 and 6 in Set mode	I	• Sets to Feedback Check by setting SDF bit 5 to 1 in Set mode for the LS supporting start-stop only. • Sets to Feedback Check by setting SDF bit 6 to 1 in Set mode for the LS only for business machine clock control.	Does not set to Feedback Check for the 2 items on the left.	7.14 SDF Bit 5 SDF Bit 6

Note: See Table 2.1 for symbols in the "Difference" column.

Table 3.1 - continued

Item No.	Item	Difference	3705-II	4705	Remarks (3705-II P00 page No., etc.)
25	SDF bit 7 in Set mode	I	See 7.14 SDF Bit 7.	Not used	7.14 SDF Bit 7
26	Warm up after POWER ON reset	IN	See 7.14 and Fig. 6.4.	Unnecessary	7.14 Business Machine Clocks
27	INPUT X'48' OUTPUT X'48'	A	Not used	Used	7.15 and 7.16 I/O Programming Considerations
28	ACU Line Set	IN	Line Set 1E	LS - NC1	7.16 Autocall Interface Operation
29	ACU Interface Feedback Check	I	See 7.17 "SDF Bits 2 and 5"	None	7.17 SDF Bits 2 and 5
30	ACU Interface SDF bit 8	A	Not used	SDF bit 8 Retry Call Indication (RCI) Indicates that retry call is possible.	7.18 SDF Bits 8 and 9
31	Number of Input instructions	IN	6	8 (Input X'48' and Input X'4D' are added.)	7.18 Input Instructions
32	INPUT X'47'	IN	The ones counter, last line state, and NRZI control bit are used by the SDLC.	As stated on the left and the ones counter and last line state are also used as the start-stop 10-bit space supervisory counter.	7.19 INPUT X'47'

Note: See Table 2.1 for symbols in the "Difference" column.

Table 3.1 - continued

Item No.	Item	Difference	3705-II	4705	Remarks (3705-II P00 page No., etc.)
33	INPUT X'48'	A	Not used	Input X'48 (ICW Input Register Bits 52, 53) This instruction may be used to determine the state of the LNG and LCL in the ICW that is set in the ICW input register. The interface address in the ABAR selects the proper scanner. Refer to I/O Programming Considerations for conditions that set the ICW input register. For an interpretation of these bits, see the Interface Control Word Format.	7.19
34	OUTPUT X'40'	IN	See 7.19 "OUTPUT X'40'".	• ICW: 51 bits • INPUT X'48' and INPUT X'4D' are added. • The OUTPUT X'40' and INPUT X'40' bit positions are different in EC mode (see OUTPUT X'78' CC). See Input/Output instruction table.	7.19 OUTPUT X'40

Note: See Table 2.1 for symbols in the "Difference" column.

Item No.	Item	Difference	3705-II	4705	Remarks (3705-II P00 page No., etc.)
35	OUTPUT X'48'	A	Not used	OUTPUT X'48 (ICW bits 52 and 53) This instruction is used to set the state of ICW bits 52 and 53. The interface address in the ABAR at execution time selects the proper scanner and the associated ICW. For a detailed interpretation of these bits, see the Interface Control Word Format of this chapter.	7.20
36	SDLC PCF X'E'	A	None	Same function as PCF X'D'	7.21 ICW Bits 34 ∿ 36 ICW Bit 44 7.23 PCF State X'9'
37	Diagnostic Functions	See items 45 ∿ 48	(1) Diagnostic wrap (2) Modem wrap See 7.23. See items 45 ∿ 48.	Provided with the following CS2 diagnostic functions: (1) CS2 wrap (2) Diagnostic wrap (3) LUT loop These cannot be used in the ACU interface.	7.23 Diagnostic Function
38	Diagnostic wrap test	A	OUTPUT X'46' Byte 1, bit 0: This bit is 0.	OUTPUT X'46' Byte 1, bit 0: SDC (ICW bit 26) This bit must be set to 0	7.23 Diagnostic Wrap Test

Note: See Table 2.1 for symbols in the "Difference" column.

Table 3.1 - continued

Item No.	Item	Difference	3705-II	4705	Remarks (3705-II P00 page No., etc.)
38	(Continued)	I	Byte 1, bit 5: Data Rate Select (ICW bit 31) This bit may be 1 or 0.	Byte 1 bit 5: This bit is 0.	
39	Modem wrap test	I	Used	None	7.24 Modem Wrap Test
40	CS2 wrap	A	None	CS2 wrap Loops one arbitrary transmission line and more than one reception line in the same CS2 by the control program specification. This function does not affect the lines without CS2 internal loop specification. The CS2 internal loop is specified by OUTPUT X '48' byte 0 bit 5 (LCL). The Set mode is not necessary since a line set is not used. Timing generated in the CS2 is used for setting the transmission speed; approximately 1400 bps. The modem information (CD, DR, and CI) are forcibly set to 1. The CS is set on when RS is on, and off when RS is off.	7.23 Diagnostic Functions

Note: See Table 2.1 for symbols in the "Difference" column.

Table 3.1 - continued

Item No.	Item	Difference	3705-II	4705	Remarks 3705-II POC page No., etc.)
41	LUT loop	A	None	LUT loop Loops all lines in the line set with the LUT LOOP switch on the operator panel. This function simultaneously loops all lines (cannot loop specific lines only). Transmission speed is selected by Oscillator Select 1 and 2. Modem information is the same as for the diagnostic wrap.	7.23 Diagnostic Functions
42	INPUT X'40'	A	Without EC mode	In EC mode, line address is set in from byte 0 bit 5 to byte 1 bit 5 of the register specified in the R operand.	B.6 INPUT X'40'
43	INPUT X'43'	IN	B.6 From byte 0 bit 0 to byte 1 bits 4 ∿ 7.	Byte 0 bit 0: LIB1 bit Clock Check This bit is set to 1 in the following cases: • Local Store or Data Out bus parity errors are detected in LIB1.	B.6 INPUT X'43'

Note: See Table 2.1 for symbols in the "Difference" column.

Table 3.1 - continued

Item No.	Item	Difference	3705-II	4705	Remarks 3705-II P00 page No., etc.)
43	(Continued)		(Continued)	• SWR or ICW address parity errors are detected during LIB1 scanning. Byte 0 bits 2 ∿ 5 and byte 1 bits 4 and 5: Same as above. Byte 0 bit 6: Interface Address Check	
				This bit is set to 1 when parity errors are detected in the line address for transmission from the CS2 to the LUT. Byte 0 bit 7 and byte 1 bits 0 - 3: Same as for 3705-II. Byte 1 bits 6 and 7: These bits are 0. Byte 1, bits 0 and 3: Indicate the corresponding address in LIB Units and sets the corresponding LIB1-6 Bit Clock Checks when a parity error is detected in the SC cycle.	

Note: See Table 2.1 for symbols in the "Difference" column.

Item No.	Item	Difference	3705-II	4705	Remarks 3705 II POC page No., etc.)
44	INPUT X'46'	IN	B.7	Forcibly sets byte 0 bit 1 (CI), byte 1 bit 2 (DK), and byte 0 bit 3 (CD) to 1 in CS2 internal loop, diagnostic wrap, and LUT loop respectively. Sets byte 0 bit 0 (CS) to 1 when RS is on.	B.7 INPUT X'46'
45	ACU INPUT X'46'	A	Byte 0 bit 4: This bit is 0.	Byte 0 bit 4: This bit is set to 1 when RCI is on.	B.7 Autocall Interface Bits for INPUT X'46'
46	INPUT X'47'	A	Byte 0 bit 7 is '0'.	Byte 0 bit 7: FNCU bit	B.7 INPUT X'47'
47	INPUT X'48'	A	None	This instruction determines the state of the LNG and LCL bits. The interface address in the ABAR selects the proper scanner and associated ICW. When this instruction is executed, the contents of the ICW input register, bit positions 52 and 53, are placed in the register specified by the Roperand. Byte 0 bits 0 - 3 and 6, and byte 1 bit 7 are set to 0.	B.8

Note: See Table 2.1 for symbols in the "Difference" column.

Table 3.1 - continued

Item No.	Item	Difference	3705-II	4705	Remarks 3705-II P00 page No., etc.)
47	(Continued)		(Continued)	See I/O Programming Considerations in Chapter 7 for conditions that cause the ICW input register to be set. For an interpretation of these bits, see the Interface Control Word Format in Chapter 7.	
48	INPUT X'4D'	A	None	This instruction is used to check the state of CS2 and LUT connection. Sets 1 when the CS2 and LUT are connected.	B.8 Addition
49	OUTPUT X'40'	A	Without EC mode	The contents of byte 0 bit 5 to byte 1 bit 5 in the register specified in the R operand are set to ABAR for EC mode. Instructions related to the ICW Input register are Input X'44', X'45', X'47', and X'48'.	B.8 OUTPUT X'40'
50	Scan limit	IN	Bit 6 7 / Scan limit: 0 1 / 8; 1 1 / 16; 1 0 / 48; 0 0 / 96	Bit 6 7 / Scan limit: 0 1 / 8; 1 1 / 16; 1 0 / 48; 0 0 / 96	B.8 OUTPUT X'42'

Note: See Table 2.1 for symbols in the "Difference" column.

Table 3.1 - continued

Item No.	Item	Difference	3705-II	4705	Remarks (3705-II P00 page No., etc.)
51	OUTPUT X'43'	A	Byte 0 bits 5 and 6 are not used.	Reserve	B.8 OUTPUT X'43'
52	OUTPUT X'43'	IN	• Byte 1 bit 6 Disable Interrupt Request • Two scan periods (307.2 microseconds)	• Byte 1 bit 6: This bit functions as follows: 0.0 = 1 and 1.6 = 1: LUT connection request cancellation 0.1 = 1 and 1.6 = 1: LUT connection request • Two scan periods (370.2 microseconds)	B.9 OUTPUT X'43' Byte 1 Bit 6 Programming Note
53	OUTPUT X'47' Byte 1 bit 3	A	Reserved	FNCU The setting of this bit is placed in ICW bit position 39.	B.10 OUTPUT X'47
54	OUTPUT X'48'	A	None	This instruction is used to specify the number of units and SYN code used in long-space supervision, CS2 internal loop, and LCD X'E'. Byte 0 bits 0, 2, and 3: Not used.	B.10

Note: See Table 2.1 for symbols in the "Difference" column.

Table 3.1 - continued

<table>
<tr><th>Item No.</th><th>Item</th><th>Difference</th><th>3705-II</th><th>4705</th><th>Remarks 3705-II P00 page No., etc.)</th></tr>
<tr><td>54</td><td>(Continued)</td><td></td><td>(Continued)</td><td>Byte 0 bit 1: SET UNIT & SYN CODE
This bit must be set to 1 to specify an arbitrary unit (5-8) SYN code in BSC with OUTPUT X'48.
Byte 0 bit 4: 10-bit Space Watch
This bit is used to detect breaks with 10-bit/1-bit spacing when PCF X'9' is set in start-stop.
1: 10-bit spacing
0: 1-bit spacing

Byte 0 bit 5: CS local performs CS2 internal loop when this bit is 1.
Byte 0 bits 6 and 7: Units 0 and 1
Specifies the number of units in LCD X'E'.
<table><tr><th colspan="2">Bit
0.6 0.7</th><th>Number of units</th></tr><tr><td>1</td><td>1</td><td>8</td></tr><tr><td>1</td><td>0</td><td>7</td></tr><tr><td>0</td><td>1</td><td>6</td></tr><tr><td>0</td><td>0</td><td>5</td></tr></table>Byte 1 bit 0 ∿ 7
Specifies SYN code in LCD X'E'.</td><td></td></tr>
</table>

Note: See Table 2.1 for symbols in the "Difference" column.

Table 3.1 - continued

<table>
<tr><th>Item No.</th><th>Item</th><th>Difference</th><th>3705-II</th><th>4705</th><th>Remarks 3705-II P00 page No., etc.)</th></tr>
<tr><td>54</td><td>(Continued)</td><td></td><td>(Continued)</td><td>
<table>
<tr><th>OUT X'48'
Number of units</th><th>1.0</th><th>1.1</th><th>1.2</th><th>1.3</th><th>1.4</th><th>1.5</th><th>1.6</th><th>1.7</th></tr>
<tr><td>8</td><td>X8</td><td>X7</td><td>X6</td><td>X5</td><td>X4</td><td>X3</td><td>X2</td><td>X1</td></tr>
<tr><td>7</td><td>X7</td><td>X6</td><td>X5</td><td>X4</td><td>X3</td><td>X2</td><td>X1</td><td>1</td></tr>
<tr><td>6</td><td>X6</td><td>X5</td><td>X4</td><td>X3</td><td>X2</td><td>X1</td><td>1</td><td>1</td></tr>
<tr><td>5</td><td>X5</td><td>X4</td><td>X3</td><td>X2</td><td>X1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Note: Number of units/SYN code cannot be specified for each line. All LCD X'E' lines in the same CS2 operate with the same number of units/SYN code.</td><td>X1: 2^0 bits
X8: 2^7 bits</td></tr>
<tr><td>55</td><td>Input/Output Instruction Summary Charts</td><td>IN</td><td>C.4 through C.6</td><td>See Appendix E. (External register list)</td><td>C.4 through C.6</td></tr>
</table>

Note: See Table 2.1 for symbols in the "Difference" column.

CHAPTER 4

TYPE 2 AND TYPE 3 CHANNEL ADAPTERS

This chapter outlines the differences between the 3705-II and 4705 with regard to Type 2 and Type 3 channel adapters.

See Table 2.2 for symbols in the "Difference" column.

Table 4.1 Differences between 3705-II and 4705 CA2/3

Item No.	Item	Difference	3705-II	4705	Remarks
1	INPUT X'5F'	A	Not defined	Used for diagnoses. Input: Channel Bus In Byte 0 bits 0 ∿ 7: Channel Bus In bits 0 ∿ 7 Byte 1 bit 0: Channel Bus In parity bit	
2	Supports EC mode	A	Not defined	See B.3 for details.	

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CHAPTER 5

TYPE4 CHANNEL ADAPTER

Table 5.1 indicates the differences between 3705-II and 4705 in the type-4 channel adapter (CA4).

Table 5.1 Differences between 3705-II and 4705 CA4

No.	Items	Difference	3705-II	4705	Remarks
1	Output X'58'	A	Unused	Used for diagnosis. Sets Channel Bus-Out data. Byte 0 bits 0-7: Channel Bus Out Bits 0-7 Byte 1 bit 1: Channel Bus-Out parity bit.	Effective only when CA4 is in Diag Wrap mode.
2	Input X'58'	A	Unused	Used for diagnosis. Inputs Channel Bus-Out data. Bits 0-7 in byte 0: Channel Bus-Out bits 0-7 Bit 0 in byte 1: Channel Bus-Out parity bit.	Effective only when CA4 is in Diag Wrap mode.

Table 5.1 - continued

No.	Items	Difference	3705-II	4705	Remarks
3	Output X'5B'	A	Unused	Used for diagnosis. Sets Channel Tag-Out data. Bits 0-5 in byte 0: Channel Tag-Out data	Effective only when CA4 is in Diag Wrap mode.
4	Input X'5B'	A	Unused	Used for diagnosis. Inputs Channel Tag-Out and Channel Tag-In data. Bits 0-5 in byte 0: Channel Tag-In data Bits 0-5 in byte 1: CA is in busy state.	Effective only when CA4 is in Diag Wrap mode.
5	Input X'5F'	A	Unused	Used for diagnosis. Inputs Channel Bus-Out data. Bits 0-7 in byte 0: Channel Bus-In bits 0-7 Byte 1, bit 0: Channel Bus-In parity bit.	Effective only when CA4 is in Diag Wrap mode.
6	Input X'60'	A	Undefined	Byte 1, bit 7 CA4 Diag Wrap Mode.	
7	Output X'61'	A	Undefined	Byte 0, bit 0 Set Diag Wrap Mode.	

APPENDIX A

4705 INSTRUCTION EXECUTION TIME

(1) An instruction execution time can be approximated according to the instruction listing Table A.4. To calculate an accurate instruction execution time the following data must be considered.

(2) One machine cycle (1 τ) is 0.145 μs.

(3) A main storage (MS) cycle is as follows:
Read cycle: 3 τ
Write cycle: 4 τ

(4) One access to main storage allows 4-byte reading and writing.
- Only one read/write cycle is required when the Load/Store instruction data address is 4n (4-byte boundary); however, two read/write cycles are required when the Load/Store instruction data address is 4n + 2 (2-byte boundary)
- The prefetching effect of branching at a 4n instruction data address is greater than that of one of 4n + 2.

(5) If no instruction prefetching effect is expected, a fetch cycle time must be added.
- An ordinary instruction execution time includes fetch and execute cycle times.
- If prefetching effect is expected, the fetch cycle of the A4705 is '0' because the instruction prefetching buffer comprises 4-6 bytes. In this condition, instruction execution cycle is given in ① and ③ of the "machine cycle" time columns in Table A.4.
  If prefetching effect is not expected, a maximum of one read cycle time is necessary as a fetch cycle.
- Give attention to the following to expect prefetching effect.

- When an instruction branches as shown in (4) above, the address must be 4n.
- Instructions of Type A (RR and RE: more than 2) and Type B (RS and RSA) must be mixed correctly.

Table A.1 Instruction step combinations and fetch cycles

		Fetch cycle
Instruction step combination	A only	0
	A, A, A,B,A, A B A - - -	0
	A A B A A B A A B - - -	0
	A B A B A B - - -	When A requires 2 or more instruction execution cycles, the fetch cycle is 0.
	A B B A B B A B B - - -	The fetch cycle is not 0.

Prefetch effect increases in the arrow direction

Note: Upper lines of combination are more effective in prefetching.

- Since RA type instructions, especially LA instruction (the execution cycle is 1 for 4705 and 3 for 4705), are 4 bytes instruction, the prefetching effect is reduced; therefore, use of these instructions is not recommended.

- The execution time of a branching instruction or (the equivalent instruction) includes the fetch cycle for the succeeding instruction. See ② in the "Machine Cycle" columns in Table A.4.

For example, the execution time of instruction B is execution cycle for B plus fetch cycle for RR.

(1) RR
(2) RI — Branch
(3) B

The fetch cycle at branching depends on the length of the instruction: halfword or 2 halfword instruction.

Table A.2 Fetch cycle at branching

Instruction address	4n	4n + 2	
Instruction length	-	HW	2 HW
MS read cycle	Once		Twice
Fetch cycle	3 ∿ 6τ		6 ∿ 9τ

(6) Load and Store instruction execution cycles

The Load and Store instruction execution cycles correspond to the cycles in ① the 'Machine cycle" columns in Table A.4. The details are as follows:

Table A.3 Load and Store execution cycles

Model	4705	
Data address	4n	4n + 2
Read or write cycle	Once	Twice
Load execution cycle	6	9
Store execution cycle	7	11

(7) The central controller is occupied when the following hardware conditions occur i.e., execution of an instruction is delayed by the time corresponding to the occupied area size.

- One interrupt occurrence: Instruction execution is delayed 4τ or 5τ
  - PCI interrupt : 5τ
  - Other interrupt: 4τ
- One cycle stealing: Instruction execution is delayed 4τ.
- Refresh time (3τ) is necessary every 15 μs to protect the main storage, i.e., instruction execution is delayed 3τ.

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Instruction name	Pseudo code for instruction	Format code	Operand field format	Machine cycle *3 ①	Machine cycle *3 ②	Instruction code 2^{15} 00 0	2^{14} 01 1	2^{13} 02 2	2^{12} 03 3	2^{11} 04 4	2^{10} 05 5	2^{9} 06 6	2^{8} 07 7	2^{7} 10 8	2^{6} 11 9	2^{5} 12 10	2^{4} 13 11	2^{3} 14 12	2^{2} 15 13	2^{1} 16 14	2^{0} 17 15	hex. ∿37 ∿31	C latch	Z latch	X byte operation	Function (*2)
Branch	B	RT	T	-	-	1	0	1	0	1	T (-2047∿2047: Only multiple)										0:+ 1:-	A800				NA+T→IAR
Branch on C latch	BCL					1	0	0	1	1												9800				C=1 NA+T→IAR
Branch on Z latch	BZL			4	4	1	0	0	0	1												8800				Z=1
Branch on count	BCT		R(N),T			1	0	1	1	1				1	T (-127∿+127: Only mul.)							8800				① (R)N-1→RN ② (R)N≠0 NA+T→IAR
Branch on bit	BB		R(N,M), T			1	1	M	M	1				M								C800				Indication bit=1 NA+T→IAR
Load reg immediate	LRI	RI	R(N),I			1	0	0	0	0	R	N	L (8 bits)									8000	≠0	= 0		I→RN
Add reg immediate	ARI					1	0	0	1	0												9000	OV	= 0	Performed	(R)N+I→RN
Subtract reg immediate	SRI					1	0	1	0	0												A000	<0	= 0	Performed	(R)N-I→RN
Compare reg immediate	CRI			3	-	1	0	1	1	0												B000	<	=		(R)N-I *→RN
EOR reg immediate	XRI					1	1	0	0	0												C000	≠ 0	= 0		(R)N ⊕ I→RN
OR reg immediate	ORI					1	1	0	1	0												D000	≠ 0	= 0		(R)N ∨ I→RN
AND reg immediate	NRI					1	1	1	0	0												E000	≠ 0	= 0		(R)N ∧ I→RN
Test reg under mask	TRM					1	1	1	1	0												F000	≠ 0	= 0		(R)N ∧ I *→RN
Load character reg	LCR	RR	R1(N1) R2(N2)			0	R2		N2	0	R1	N1	0	0	0	0	1	0	0	0		0008	E	= 0		(R)N2→RN1
Add character reg	ACR					0				0			0	0	0	1	1	0	0	0		0018	OV	= 0	Performed	(R)N1+(R)N2→RN1
Subtract character reg	SCR			4	-	0				0			0	0	1	0	1	0	0	0		0028	<0	= 0	Performed	" - " → "
Compare character reg	CCR					0				0			0	0	1	1	1	0	0	0		0038	<	=		" - " → "
EOR character reg	XCR					0				0			0	1	0	0	1	0	0	0		0048	≠ 0	= 0		" ⊕ " → "

When conditions are not satisfied. NA→IAR

Table A.4 - continued

Instruction name	Pseudo code for instruction	Format code	Operand field format	Machine cycle *3 ①	Machine cycle *3 ②	Instruction code 2^15 2^14 2^13 2^12	2^11 2^10 2^9 2^8	2^7 2^6 2^5 2^4	2^3 2^2 2^1 2^0	hex.	C latch	Z latch	X byte operation	Function (*2)
						00 01 02 03	04 05 06 07	10 11 12 13	14 15 16 17	∿37				
						0 1 2 3	4 5 6 7	8 9 10 11	12 13 14 15	∿31				
OR character reg	OCR	RR	R1(N1) R2(N2)		4 -	0 R2 N2	0 R1 N1	0	1 0 1 1 0 0 0	0058	≠ 0	= 0		(R)N1 ∨ (R)N2 → RN1
AND character reg	NCR					0	0	0	1 1 0 1 0 0 0	0068	≠ 0	= 0		" ∧ " → "
L chr. offset reg	LCOR					0	0	0	1 1 1 1 0 0 0	0078	S	= 0		(R)N2 1 bit shift to right → RN1
Insert CH and count	ICT	RSA	R(N),B		7 -	0 B = 0 should not be set.	0 R N	0	0 0 1 0 0 0 0	0010				① (B)+1 → B ② (R)N (B before execution) → RN
Store CH and count	STCT				8	0	0	0	0 1 1 0 0 0 0	0030				① (B)+1 → B ② (R)N → (B before execution)
Insert character	IC	RS	R(N), D(B)		6 -	0 B Give attention to B = 0.	1 R	0 D (0 ∿ 127)		0800	E	= 0		((B)+D) → RN B=0 = (B) = 680
Store character	STC				7	0	1	1		0880				(R)N → (B)+D " = 680
Load halfword	LH		R,D(B)		6 7	0	0 R	0 D (0∿127: only mul.)	1	0001	≠ 0	= 0	0	((B)+D) → R " = 700
Store halfword	STH				7 -	0	0	1	1	0081				(R) → (B)+D " = 700
Load	L				6,9 7,10	0	0 (R) = 0	0	1 0	0002	≠ 0	= 0	Performed	((B)+D) → R " = 780
Store	ST				7,11 -	0	0	1 D (0∿127: only multiple of 4)	1 0	0082			Performed	(R) → (B)+D " = 780
Load halfword reg	LHR	RR	R1,R2		4 5	0 R2	0 R1	1	0 0 0 0 0 0 0	0080	≠ 0	= 0		(R2) o (R1) → R1 (Operation defined by the instruction) See RRC type.
Add halfword reg	AHR					0	0	1	0 0 0 0 0 0 0	0090	OV	= 0		
Subtract halfword reg	SHR					0	0	1	0 0 0 0 0 0 0	00A0	<0	= 0		
Compare halfword reg	CHR					0	0	1	1 0 0 0 0 0 0	00B0	<	=		
EOR halfword reg	XHR					0	0	1	1 0 0 0 0 0 0	00C0	≠ 0	= 0		
OR halfword reg	OHR					0	0	1	1 0 1 0 0 0 0	00D0	≠ 0	= 0		
AND halfword reg	NHR					0	0	1	1 1 0 0 0 0 0	00E0	≠ 0	= 0		
L.HW with offset reg	LHOR					0	0	1	1 1 1 0 0 0 0	00F0	S	= 0		

Instruction name	Pseudo code for instruction	Format code	Operand field format	Machine cycle *3 ①	Machine cycle *3 ②	Instruction code hex.	C latch	Z latch	X byte operation	Function (*2)
						2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0}				
						00 01 02 03 04 05 06 07 10 11 12 13 14 15 16 17	∿37			
						0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	∿31			
Load reg	LR	RR	R1,R2	4	5	0 R2 0 R1 1 0 0 0 1 0 0 0	0088	≠ 0	= 0	Performed	(R2) o (R1)→R1 (Operation defined by the instruction) See RRC type.
Add reg	AR					0 R2 0 R1 1 0 0 1 1 0 0 0	0098	0V	= 0	"	
Subtract reg	SR					0 R2 0 R1 1 0 1 0 1 0 0 0	00AB	<0	= 0	"	
Compare reg	CR					0 R2 0 R1 1 0 1 1 1 0 0 0	00B8	<	=	"	
EOR reg	XR					0 R2 0 R1 1 1 0 0 1 0 0 0	00C8	≠ 0	= 0	"	
OR reg	OR					0 R2 0 R1 1 1 0 1 1 0 0 0	00D8	≠ 0	= 0	"	
AND reg	NR					0 R2 0 R1 1 1 1 0 1 0 0 0	00E8	≠ 0	= 0	"	
L. with offset reg	LOR					0 R2 0 R1 1 1 1 1 1 0 0 0	00F8	S	= 0	"	
Branch and link reg	BALR			–	4	0 R2 0 R1 0 1 0 0 0 0 0 0	0040				① NA→R1 ② (R2 before execution)→IAR
Input	IN	RE	R,E	5	6	0 E 0 R 1 1 0 0	000C			Performed	(E)→R
Output	OUT			4	5	0 E 0 R 0 1 0 0	0004			"	(R)→E
Branch and link	BAL	RA	R,A	–	4	1 0 1 1 1 0 0 0 A	B800			"	① NA→R ② A→IAR
Load address	LA			3	4	1 0 1 1 1 0 0 1 A	B820			"	A→R
Exit	EXIT	EXIT		–	4	1 0 1 1 1 0 0 0 0 1 0 0 0 0 0 0	B840				The program in the current level is completed and the program in the suspended level is executed.
						00 01 02 03 04 05 06 07 10 11 12 13 14 15 16 17					

Notes: 1) C Latch

= 0	Operation result = 0
< 0	Operation result <
<	R1 < R2 or I
E	Bit 1 is even
OV	Operation result overflows.
S	Right shift-out bit = 1

Z Latch

= 0	Operation result = 0
=	R1 = R2 or I

2) NA: Next Address, (IAR) + 2 or (IAR) + 4

May not coincide with the next execution address (NEA)

3) The machine cycle of this CP is 0.145 μs.

(1) Stepping to NA

(2) Branching

The 2 halfword instruction in the 2-type boundary: Value in the table + 3

(1), (2) A475 EN1

4) List: The value depend on whether it is in the 4-type boundary.

	4n + 0, 1	4n + 2, 3
L	6	9
ST	7	11

5) A 0.435 μs refresh time must be reserved every 15 μs, i.e., a 15 μs instruction requires 15 435 μs for execution.

6) An interrupt requires an extra 4 or 5τ.

APPENDIX B

BASIC CONTROL AND EXTENDED CONTROL MODES

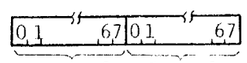
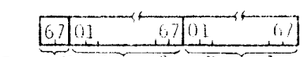
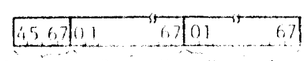
B.1 CENTRAL CONTROLLER

B.1.1 Mode Names

. Data comprising bytes X, 0, and 1 is defined as "Full Bits".

. Modes are named according to bit width.

Table B.1 Mode names

Item number	Number of bits of full bits	Data configuration	Difference	3705-II	4705	Remarks 3705-II P00 page No.,etc.)
1	16 bits		IN	Without Extended Addressing	Defined as 4705 BC mode	Basic Control Mode
2	18 bits		IN	With Extended Addressing		
3	20 bits		A	Not defined	Defined as 4705 EC mode	Extended Control Mode

B.1.2 Differences between BC and EC Mode

Table B.2 Differences between BC and EC modes (CC)

Item No.	Item	Difference	3705-II 4705 BC mode	4705 EC mode	Remarks 3705-II P00 page No., etc.)
1	Accessible storage addresses				3-1
	X'0' ∿ X'3FFFF'	IN	Can be accessed.	Can be accessed.	
	X'40000' ∿ X'FFFFF'	A	Cannot be accessed.	Can be accessed.	
2	Full-bit operation of ART, SRT, ACR, SCR, LR, AR, SR, CR, XR, OR, NR, and LOR	IN	18 bits	20 bits	Items 4-10 show examples of instruction operations.
3	AEXC IN X'70' value is 32-214K bytes	IN	AEXC occurs when the storage address is the value specified by IN X'70' or more.	AEXC occurs when the storage address is the value specified by IN X'70' or more.	5-10 Address Exception
	AEXC IN X'70' value is 256K bytes	IN	AEXC does not occur.	"	
	AEXC IN X'70' value is 288 ∿ 992K bytes	A	------	"	
	AEXC IN X'70' value is 1024K bytes	A	-----	AEXC does not occur.	
4	AR instruction full-bit operation example	A	(R1) = X'3FFFF' (R2) = X'00001' Result of (R1) + (R2)→R1 (R1) = X'00000' C = 1 (bytes X, 0 and 1 overflowed) Z = 1 (bytes X, 0, and 1 = 0)	(R1) = X'FFFFF' (R2) = X'00001' Result of (R1) + (R2)→R1 (R1) = X'00000' C = 1 (bytes X, 0 and 1 overflowed) Z = 1 (bytes X, 0, and 1 = 0)	4-7 Add Register

Table B.2 - continued

Item No.	Item	Difference	3705-II 4705 BC mode	4705 EC mode	Remarks 3705-II P00 page No., etc.)
5	ACR instruction full-bit operation example	A	(R1 N1 = 1) = X'3FFFF' (R2 N2 = 1) = X'00001' Result of (R1 N1 = 1) + (R2 N2 = 1) → R1 N1 (R1 N1) = X'00000' C = 1 (bytes 0 and 1 overflowed) Z = 1 (bytes 0 and 1 = 0)	(R1 N1 = 1) = X'3FFFF' (R2 N2 = 1) = X'00001' Result of (R1 N1 = 1) + (R2 N2 = 1) → R1 N1 (R1 N1) = X'40000' C = 1(bytes 0 and 1 overflowed) Z = 1 (bytes 0 and 1 = 0)	4-7 Add Character Register
6	ARI instruction full-bit operation example	A	(R N = 1) = X'3FFFF' I = X' 01' Result of (R N = 1) + I → R N (R N) = X'00000' C = 1 (bytes 0 and 1 overflowed) Z = 1 (bytes 0 and 1 = 0)	(R N=1) = X'3FFFF' I = X' 01' Result of (R N = 1) + I R N (R N) = X'40000' C = 1 (bytes 0 and 1 overflowed) Z = 1 (bytes 0 and 1 = 0)	4-8 Add Register
7	SR instruction full-bit operation example	A	(R1) = X'00000' (R2) = X'00001' Result of (R1) - (R2) → R1 (R1) = X'3FFFF' C = 1 (bytes X, 0, and 1 < 0) Z = 0 (bytes X, 0, and 1 ≠ 0)	(R1) = X'00000' (R2) = X'00001' Result of (R1) - (R2) → R1 (R1) = X'FFFFF' C = 1 (bytes X, 0, and 1 < 0) Z = 0 (bytes X, 0, and 1 ≠ 0)	4-8 Subtract Register

Table B.2 - continued

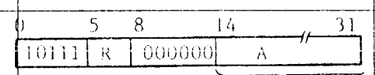
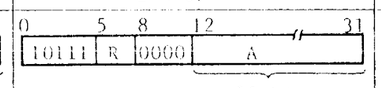
Item No.	Item	Difference	3705-II 4705 BC mode	4705 EC mode	Remarks 3705-II P00 page No., etc.)
8	SCR instruction full-bit operation example	A	(R1 N1 = 1) = X'30000' (R2 N2 = 1) = X'00001' Result of (R1 N1=1) - - (R2 N2=1) → R1 N1 (R1 N1) = X'2FFFF' C = 1 (bytes 0 and 1 < 0 Z = 0 (bytes 0 and 1 ≠ 0	(R1 N1 = 1) = X'F0000' (R2 N2 = 1) = X'00001' Result of (R1 N1=1) - (R2 N2=1) → R1 N1 (R1 N1) = X'EFFFF' C = 1 (bytes 0 and 1 < 0 Z = 0 (bytes 0 and 1 ≠ 0	4-8 Subtract Character Register
9	SRI instruction full-bit operation example	A	(R N = 1) = X'30000' I = X' 01' Result of (R N=1) - I → RN (RN) = X'2FFFF' C = 1 (bytes 0 and 1 < 0 Z = 0 (bytes 0 and 1 ≠ 0	(R N = 1) = X'F0000' I = X' 01' Result of (R N=1) - I → RN (RN) = X'2FFFF' C = 1 (bytes 0 and 1 < 0 Z = 0 (bytes 0 and 1 ≠ 0	4-9 Subtract Register Immediate
10	LOR Instruction full-bit operation example	A	(R2) = X'3FFFF' Result of (R2) shifted 1 bit to right → R1 (R1) = X'1FFFF' C = 1 (Shift-out bit = 1) Z = 0 (bytes X, 0, and 1 ≠ 0)	(R2) = X'FFFFF' Result of (R2) shifted 1 bit to right → R1 (R1) = X'7FFFF' C = 1 (Shift-out bit = 1) Z = 0 (byte X, 0, and 1 ≠ 0)	4-11 Load with Offset Register
11	When BAL instruction field A is used in full bits	A	 Field A is bits 14-31 (18 bits). F2806BC does not regard BAL as invalid instruction even when bits 12 and 13 are 1.	 Field A is bits 12-32 (20 bits).	4-6 Branch and Link

Table A.4 - continued

Notes: 1) C Latch

= 0	Operation result = 0
< 0	Operation result <
<	R1 < R2 or I
E	Bit 1 is even
OV	Operation result overflows.
S	Right shift-out bi = 1

Z Latch

= 0	Operation result = 0
=	R1 = R2 or I

2) NA: Next Address, (IAR) + 2 or (IAR) + 4

May not coincide with the next execution address (NEA)

3) The machine cycle of this CP is 0.145 μs.

(1) Stepping to A

(2) Branching

The 2 halfword instruction in the 2-type boundary: Value in the table + 3

(1), (2) A47 5 EN1

4) List: The value depend on whether it is in the 4-type boundary.

	4n + 0, 1	4n + 2, 3
L	6	9
ST	7	11

5) A 0.435 μs refresh time must be reserved every 15 μs, i.e., a 15 μs instruction requires 15 435 μs for execution.

6) An interrupt requires an extra 4 or 5τ.

APPENDIX B

BASIC CONTROL AND EXTENDED CONTROL MODES

B.1 CENTRAL CONTROLLER

B.1.1 Mode Names

. Data comprising bytes X, 0, and 1 is defined as "Full Bits".

. Modes are named according to bit width.

Table B.1 Mode names

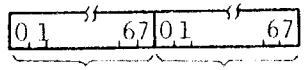
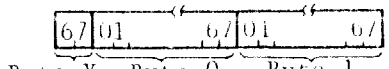
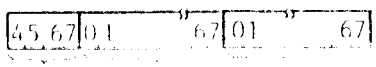
Item number	Number of bits of full bits	Data configuration	Difference	3705-II	4705	Remarks 3705-II P00 page No.,etc.)
1	16 bits		IN	Without Extended Addressing	Defined as 4705 BC mode	Basic Control Mode
2	18 bits		IN	With Extended Addressing		
3	20 bits		A	Not defined	Defined as 4705 EC mode	Extended Control Mode

Table B.2 Differences between BC and EC modes (CC)

Item No.	Item	Difference	3705-II 4705 BC mode	4705 EC mode	Remarks (3705-II P00 page No., etc.)
1	Accessible storage addresses				3-1
	X'0' ∿ X'3FFFF'	IN	Can be accessed.	Can be accessed.	
	X'40000' ∿ X'FFFFF'	A	Cannot be accessed.	Can be accessed.	
2	Full-bit operation of ARI, SRI, ACR, SCR, LR, AR, SR, CR, XR, OR, NR, and LOR	IN	18 bits	20 bits	Items 4-10 show examples of instruction operations.
3	AEXC: IN X'70' value is 32-214K bytes	IN	AEXC occurs when the storage address is the value specified by IN X'70' or more.	AEXC occurs when the storage address is the value specified by IN X'70' or more.	5-10 Address Exception
	AEXC: IN X'70' value is 256K bytes	IN	AEXC does not occur.	"	
	AEXC: IN X'70' value is 288 ∿ 992K bytes	A	------	"	
	AEXC: IN X'70' value is 1024K bytes	A	-----	AEXC does not occur.	
4	AR instruction full-bit operation example	A	(R1) = X'3FFFF' (R2) = X'00001' Result of (R1) + (R2)→R1 (R1) = X'00000' C = 1 (bytes X, 0 and 1 overflowed) Z = 1 (bytes X, 0, and 1 = 0)	(R1) = X'FFFFF' (R2) = X'00001' Result of (R1) + (R2)→R1 (R1) = X'00000' C = 1 (bytes X, 0 and 1 overflowed) Z = 1 (bytes X, 0, and 1 = 0)	4-7 Add Register

Table B.2 - continued

Item No.	Item	Difference	3705-II 4705 BC mode	4705 EC mode	Remarks 3705-II P00 page No., etc.)
5	ACR instruction full-bit operation example	A	(R1 N1 = 1) = X'3FFFF' (R2 N2 = 1) = X'00001' Result of (R1 N1 = 1) + (R2 N2 = 1) → R1 N1 (R1 N1) = X'00000' C = 1 (bytes 0 and 1 overflowed) Z = 1 (bytes 0 and 1 = 0)	(R1 N1 = 1) = X'3FFFF' (R2 N2 = 1) = X'00001' Result of (R1 N1 = 1) + (R2 N2 = 1) → R1 N1 (R1 N1) = X'40000' C = 1(bytes 0 and 1 overflowed) Z = 1 (bytes 0 and 1 = 0)	4-7 Add Character Register
6	ARI instruction full-bit operation example	A	(R N = 1) = X'3FFFF' I = X' 01' Result of (R N = 1) + I → R N (R N) = X'00000' C = 1 (bytes 0 and 1 overflowed) Z = 1 (bytes 0 and 1 = 0)	(R N=1) = X'3FFFF' I = X' 01' Result of (R N = 1) + I → R N (R N) = X'40000' C = 1 (bytes 0 and 1 overflowed) Z = 1 (bytes 0 and 1 = 0)	4-8 Add Register
7	SR instruction full-bit operation example	A	(R1) = X'00000' (R2) = X'00001' Result of (R1) - (R2) → R1 (R1) = X'3FFFF' C = 1 (bytes X, 0, and 1 < 0) Z = 0 (bytes X, 0, and 1 ≠ 0)	(R1) = X'00000' (R2) = X'00001' Result of (R1) - (R2) → R1 (R1) = X'FFFFF' C = 1 (bytes X, 0, and 1 < 0) Z = 0 (bytes X, 0, and 1 ≠ 0)	4-8 Subtract Register

Table B.2 - continued

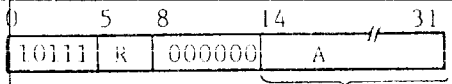
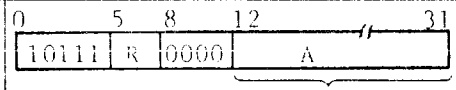
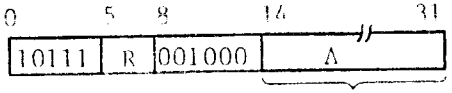
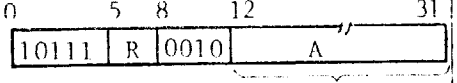
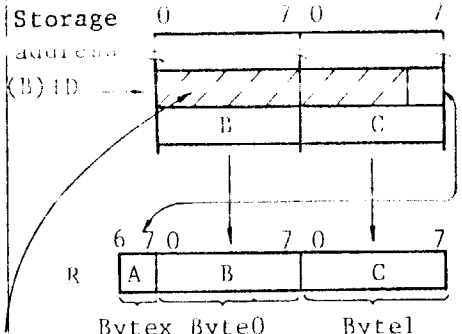
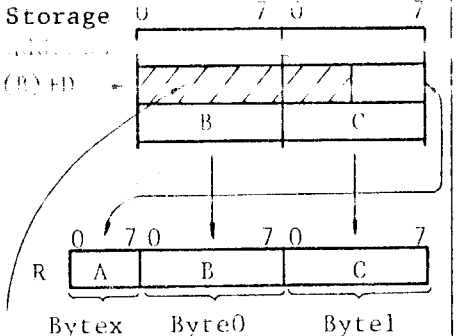
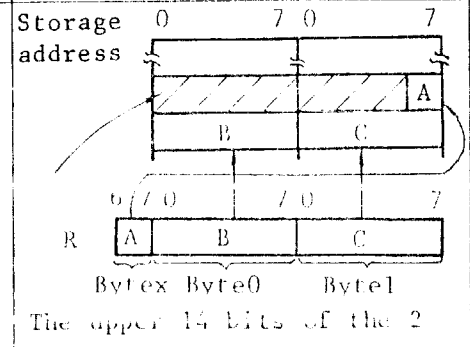
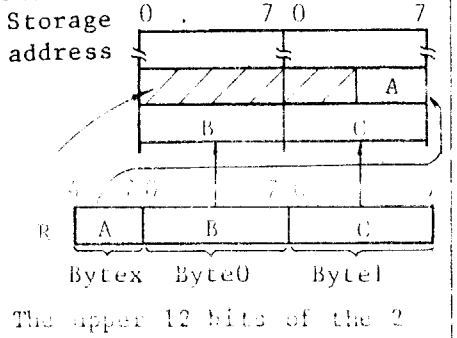
Item No.	Item	Difference	3705-II 4705 BC mode	4705 EC mode	Remarks 3705-II P00 page No., etc.)
8	SCR instruction full-bit operation example	A	(R1 N1 = 1) = X'30000' (R2 N2 = 1) = X'00001' Result of (R1 N1=1) - (R2 N2=1) → R1 N1 (R1 N1) = X'2FFFF' C = 1 (bytes 0 and 1 < 0 Z = 0 (bytes 0 and 1 ≠ 0	(R1 N1 = 1) = X'F0000' (R2 N2 = 1) = X'00001' Result of (R1 N1=1) - (R2 N2=1) → R1 N1 (R1 N1) = X'EFFFF' C = 1 (bytes 0 and 1 < 0 Z = 0 (bytes 0 and 1 ≠ 0	4-8 Subtract Character Register
9	SRI instruction full-bit operation example	A	(R N = 1) = X'30000' I = X' 01' Result of (R N=1) - I → RN (RN) = X'2FFFF' C = 1 (bytes 0 and 1 < 0 Z = 0 (bytes 0 and 1 ≠ 0	(R N = 1) = X'F0000' I = X' 01' Result of (R N=1) - I → RN (RN) = X'2FFFF' C = 1 (bytes 0 and 1 < 0 Z = 0 (bytes 0 and 1 ≠ 0	4-9 Subtract Register Immediate
10	LOR Instruction full-bit operation example	A	(R2) = X'3FFFF' Result of (R2) shifted 1 bit to right → R1 (R1) = X'1FFFF' C = 1 (Shift-out bit = 1) Z = 0 (bytes X, 0, and 1 ≠ 0)	(R2) = X'FFFFF' Result of (R2) shifted 1 bit to right → R1 (R1) = X'7FFFF' C = 1 (Shift-out bit = 1) Z = 0 (byte X, 0, and 1 ≠ 0)	4-11 Load with Offset Register
11	When BAL instruction field A is used in full bits	A	 Field A is bits 14-31 (18 bits). F2806BC does not regard BAL as invalid instruction even when bits 12 and 13 are 1.	 Field A is bits 12-32 (20 bits).	4-6 Branch and Link

Table B.2 - continued

Item No.	Item	Difference	3705-II, 4705 BC mode	4705 EC mode	Remarks 3705-II P00 page No., etc.)
12	When LA Instruction field A is used in full bits	A	 Field A is bits 14-32 (18 bits).	 Field A is bits 12-31 (20 bits).	4-11 Load Address
13	L instruction full-bit operation	A	Storage address  The upper 14 bits of the 2 halfwords are ignored.	Storage address  The upper 12 bits of the 2 halfwords are ignored.	4-9 Load
14	ST instruction full-bit operation	A	Storage address  The upper 14 bits of the 2 halfwords are not updated.	Storage address  The upper 12 bits of the 2 halfwords are not updated.	4-12 Store

Note: See Table 2.2 for symbols in the "Item" column.

B.1.3 Mode Switching Instruction

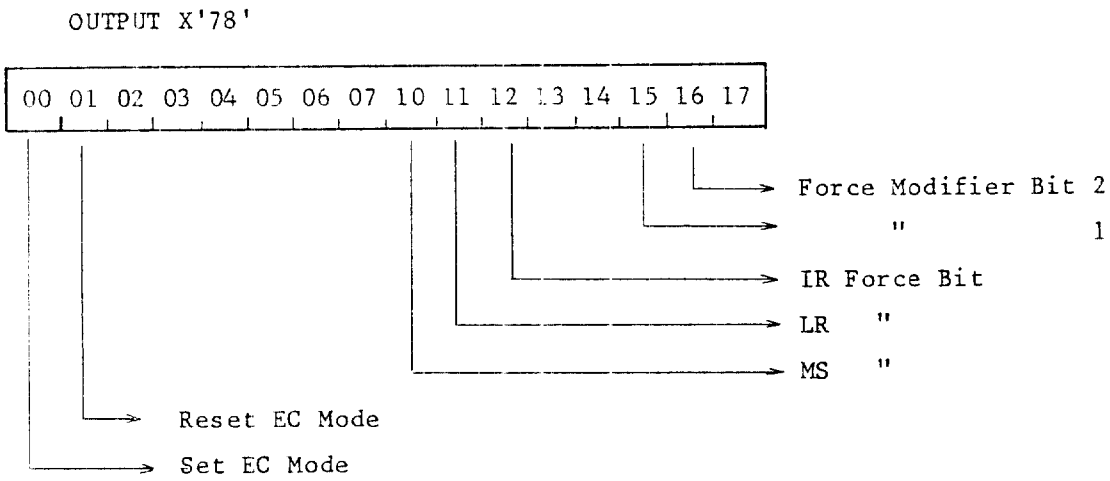
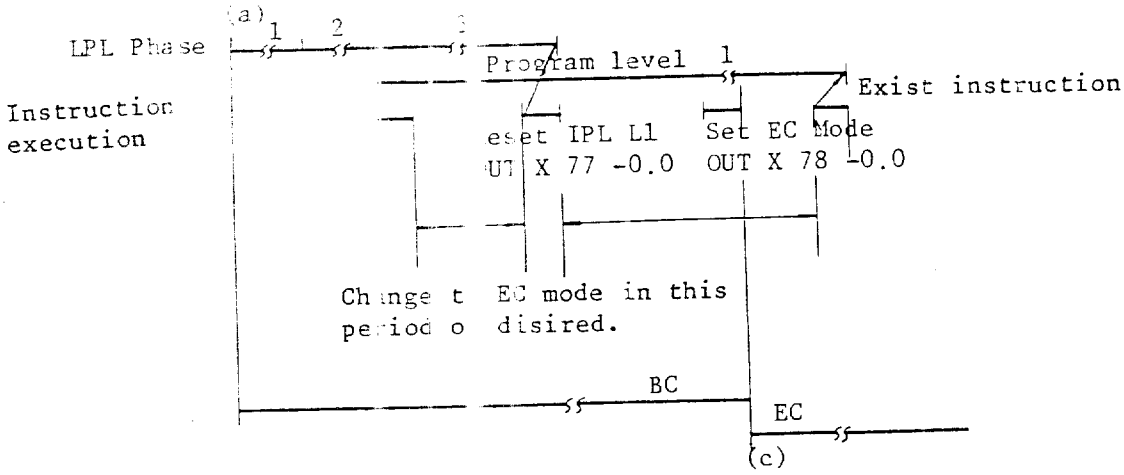


Fig. B.1 CUTPUT X'78'

(1) Set all other bits to 0 for EC mode set or reset.

(2) Set all unused bits to 0 for force check.

(3) Time chart



a. Automatically set to BC mode when IPL phase starts.

   IPL phase starts in the following conditions:

   - Power on
   - OUT X'79' bit 0.2 execution
   - Panel RESET switch on
   - CA receives WIPL command
   - Panel LOAD switch on
   - Machine check causes detected in other than IPL phase

b. Set to EC mode with program L1 caused by the IPL between the first ST instruction and the last EXIT instruction.

c. Restrictions of EC/BC operation immediately after switching to the EC mode:

   Central controller: None

   Each adapter: See each adapter specifications

Fig. B.2 IPL time chart

B.1.4 Programming Notes

(1) The operation is set to BC mode after the IPL phase (BC mode even after ROS execution). The OUT instruction in the Set EC mode can be executed only once during Initial Load Program Phase 1.

(2) Use the Reset EC mode for diagnoses only (do not use in normal operations).

(3) Execute the Set IPL OUT Instruction when the dump program is completed and programs will be restarted.

(4) General register bits X4 and X5 data cannot be transferred or retained between the BC and EC.

a. LA instruction in EC X'C0000' — R1
b. LR instruction in BC R1 — R2 (R2) = X'00000'
c. LA instruction in BC X'0FFFF' — R1
d. LR instruction in EC R1 — R2 (R2) = X'0FFFF'

R2 bits X4 and X5 become '0' (not '1') as a result of d. when executing instructions from a. to d. in this order.

B.2 TYPE 2 COMMUNICATION SCANNER

Input/Output instructions in BC/EC mode

BC mode IN X'40' format
OUT X'40' format

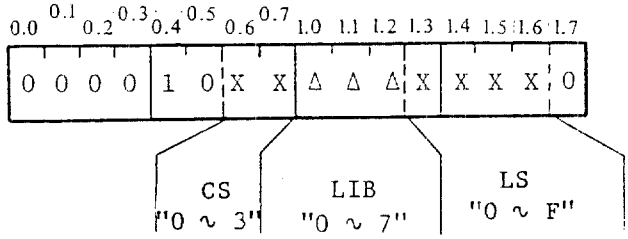


Fig. B.3 IN X'40'/OUT X'40' format

B.3 TYPE 2 AND TYPE 3 CHANNEL ADAPTER

Table B.3 Differences between BC and EC modes (CA2/3)

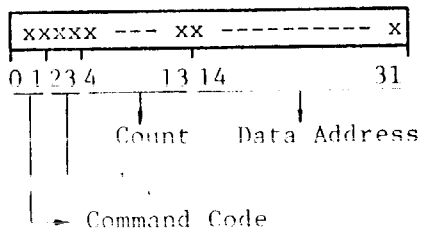
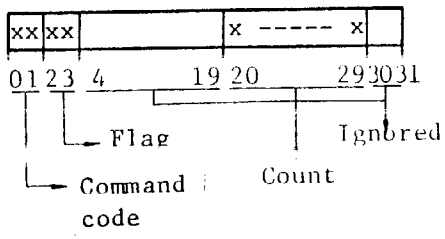
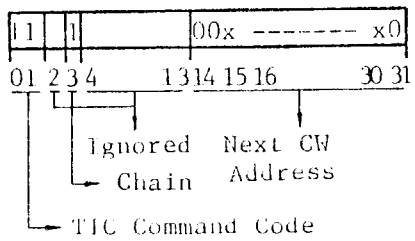
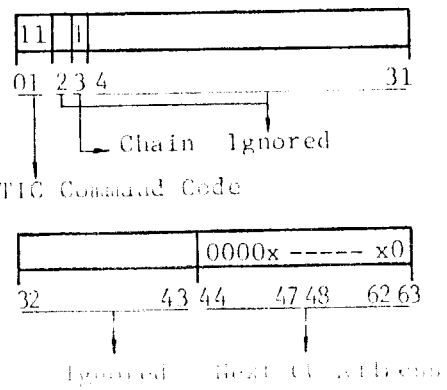
Item No.	Item	Difference	3705-II 4705 BC mode	4705 EC mode	Remarks 3705-II P00 page No., etc.)
1	Control word (CW) formats 1) Format for IN, OUT and OUT STOP	A		Composed of 2 consecutive words (64 bits) 	10-5
	2) Format for TIC				

Table B.3 - continued

Item No.	Item	Difference	3705-II 4705 BC mode	4705 EC mode	Remarks 3705-II P00 page No., etc.)
2	INPUT X'52'	A	Byte 0 bits 0 ∿ 5 : These bits are 0.	Byte 0 bits 0 ∿ 3 : CSAR byte X, bits 4 ∿ 7. Byte 0 bits 4 ∿ 5 : These bits are 0.	B-25
3	INPUT X'58'	A	Byte 1 bits 6 ∿ 7 : CSAR byte X, bits 6 ∿ 7.	Byte 1 bits 6 and 7 : CSAR byte X, bits 6 ∿ 7. Programming note: Ignore this bit.	B-28

Note: See Table 2.1 for symbols in the "Difference" column.

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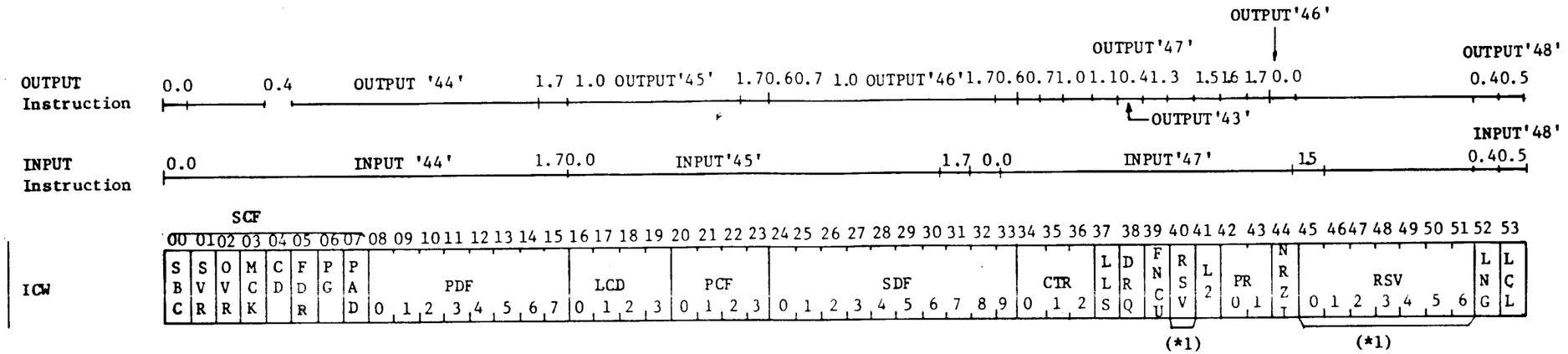
APPENDIX C

INTERFACE CONTROL WORD



- **SBC** : Stop bit check/receive break/abort (SDLC)
- **SVR** : Service Request
- OVR : Character Overrun Underrun
- **MCK** : Modem Check
- **CD** : Carrier Detect
- **FDR** : Flag Detection (SDLC)/Disable Zero Insert Remembrance (SDLC)
- **PG** : Program Flag
- **PAD** : Pad Flag (SS)/CD Detection (SS)/ Disable Zero Insert Control (SDLC)
- **CTR** : Ones Counter (SDLC)] 10 bit long space counter (SS)
- **LLS** : Last Line State (SDLC)
- **DRQ** : Display Request
- **L2** : Level 2 Interrupt Pending
- PRO,1: Priority 0.1
- **NRZI** : NRZI Control (SDLC)
- **LNG** : Long Space Bit←Long-space (10 bits) Supervision [ON: 10-bit space supervision / OFF: 1-bit space supervision]
- **LCL** : CS2 Local Test

SDF (Serial Data Field)

	Set mode	ACU
0		IR
1		PI
2	SDC	CRQ
3	WRP	DLO
4	ER	PMD
5	SYN	DPR
6	EXT	DSC
7		ACL
8	OSC0	RCI
9	OSC1	

PDF (Parallel Data Field)

	ACU	Other than ACU	
		Send mode	Receive mode
0		SD7	RD7
1		" 6	" 6
2		" 5	" 5
3		" 4	" 4
4	Digit No. 8	" 3	" 3
5	Digit No. 4	" 2	" 2
6	Digit No. 2	" 1	" 1
7	Digit No. 1	" 0	" 0

LCD (Line Control Definer)

	LCD Definition	Remarks
0	Start/stop 9/6	
1	Start/stop 8/6	
2	Start/stop 8/5	
3	ACU	
4	Start/stop 8/7	
5	Start/stop 10/7	
6	Start/stop 10/8	
7	Start/stop 11/8	
8	Monitor SDLC FLAG	
9	SDLC 8 BIT BYTE length	
A	Not used	
B	Not used	
C	BSC EBCDIC	
D	BSC USASCII	
E	BSC SBT etc.	Specified by OUT '48'
F	Feedback Error	Data in errors, etc.

PCF (Primary Control Field)

	Start-stop	Synchronous	SDLC	ACU
0	No op	No op	No op	No op
1	Set mode	Set mode	Set mode	
2	DR ON supervision	DR ON supervision	DR ON supervision	
3	CI/DR ON supervision	CI/DR ON supervision	CI/DR ON supervision	
4		SYN supervision	Flag supervision (ignores DR)	ACL, DSC, PWD supervision
5		SYN supervision (supervision DR)	Flag supervision (supervision DR)	ACL, DSC, and RCI supervision
6			Flag reception	
7	Reception	Reception	INFO reception	
8	Transmission (initial)	Transmission (initial)	Transmission (initial)	Digit valid
9	Transmission (normal)	Transmission (normal)	Transmission (normal)	
A	Break transmission	Transmission with NEW SYNC	Transmission with NEW SYNC	
B	Transmission inversion setup			
C	Transmission inversion RS OFF	Transmission inversion RS OFF	Transmission inversion RS OFF	
D	Transmission inversion RS ON	Transmission inversion RS ON	Flag transmission	
E	Transmission completion RS ON	Transmission completion RS ON	Flag transmission	
F	Disable	Disable	Disable	Disable

Note: ICW bits 40 and 45-51 are not used.

Fig. C.1 ICW

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