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# HOW TO MAINTAIN THE CONSUL 520/580 & MRD 380

HOW TO MAINTAIN THE  
CONSUL 520/580 & MRD 380



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This revision of the maintenance documentation for the 520/580 and 380 terminals supersedes the last version dated 3/78.

Service personnel should also refer to the User Manual for the 500 Series Terminals (#511-32900B).

A list of changed pages appears below; a margin bar indicates the changes on affected text pages.

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## SECTION 1:

### INTRODUCTION

This manual is intended for use by personnel who must perform fault diagnosis and repair on the Consul 520, 580 and MRD 380.

#### GENERAL DESCRIPTION

Both the Consul 520 and 580 are low cost TTY-compatible CRT display terminals. They are designed for users who wish to take advantage of a CRT's silent operation, fast transmission speed and inherent reliability. They are self-contained desktop units.

Each displays data in a format of 24 lines with 80 characters per line, making a total of 1920 characters. Data is displayed as black characters on a white background. Communications with the data processing system or a minicomputer takes place a character at a time on a conversational basis, a method that is identical to that used by teletypewriters.

A rack-mountable version of the 580 is available; it is designated the MRD 380 Series. This equipment consists of:

An electronics package which consists of the terminal electronics (same P.C. cards as the 580) in a chassis suitable for mounting in standard 19" RETMA racks. Vertical panel height is 5 1/4 inches.

A separate keyboard, in its own housing, which plugs into the 380 electronics package.

A TV monitor which connects via 75-ohm coaxial cable to the electronics package.

#### FEATURES OF THE CONSUL 580 AND MRD 380

##### EIA and Current Loop Interfaces

An EIA RS232C voltage interface and a 20 milliamperere current loop interface are standard; both are operational over the full speed range of the terminal, up to 9600 baud.

##### Five Transmission Speeds

Transmission rates of 110, 300, 1200, 2400 or 9600 baud are selectable by means of a switch on the rear panel of the 580.



CONSUL 580



ADDIS Applied Digital Data Systems Inc. CONSUL 580

MRD 380



### Selection of Half and Full Duplex

The operator's FULL DUP switch permits selection of full or half duplex operation.

### Automatic Line Feed Selection

A switch labeled AUTO LF allows the operator to inhibit or enable an automatic internal Line Feed after receipt of a Carriage Return code.

### Roll Mode Selection

The operator of a 580 can inhibit or enable the upward scrolling of data through use of the ROLL switch. Depressing this switch enables data to scroll upward if the cursor is in the bottom line and a Cursor Down or Line Feed command is received from the keyboard or CPU.

### Cursor Control

Cursor controls to position the cursor up, down, forward, backward and home are available. Home is the lower left corner of the screen when the 580 is scrolling data. When scrolling is inhibited, home is the upper left corner of the screen.

### Printer Interface

A printer interface allows attachment of any serial EIA printer. The operator can control the flow of data to the printer by using the PRINT ON and PRINT OFF keys on the 580 keyboard.

### Audible Alarm

The BEL code causes an audible alarm in the 580 to be activated.

### Remote Control

Remote control commands for the 580 are available to perform Carriage Return and Line Feed operations, erase the screen and move the cursor up, down, forward, backward and home. In addition, the CPU can lock and unlock the keyboard, activate the audible alarm and turn the printer interface on and off.

### Cursor Addressing

The computer can address the cursor to any given position on the screen. Addressing is provided by two command codes, a Vertical Address command and a Horizontal Address command. Each of these commands is followed by a character that determines the desired cursor position.

## FEATURES OF THE CONSUL 520

### EIA and Current Loop Interface

An EIA RS232C voltage interface and a 20 milliampere current loop interface are standard; both are operational over the full speed range of the terminal, up to 9600 baud.

### Five Transmission Speeds

Transmission rates of 110, 300, 1200, 2400 or 9600 baud are selectable by means of a switch on the rear panel of the 520.

### Selection of Half and Full Duplex

The operator's FULL DUP switch permits selection of full or half duplex operation.

### Automatic Line Feed Selection

A switch labeled AUTO LF allows the operator to inhibit or enable an automatic internal Line Feed after receipt of a Carriage Return code.

### Roll Mode Selection

The operator of a 520 can inhibit or enable the upward scrolling of data through use of the ROLL switch. Depressing this switch enables data to scroll upward if the cursor is in the bottom line and a Cursor Down or Line Feed command is received from the keyboard or CPU.

### Cursor Control

Cursor controls to position the cursor up, down, forward, backward and home are available. These functions are produced with the CONTROL key from the keyboard. Home is the lower left corner of the screen when the 520 is scrolling data. When scrolling is inhibited, home is the upper left corner of the screen.

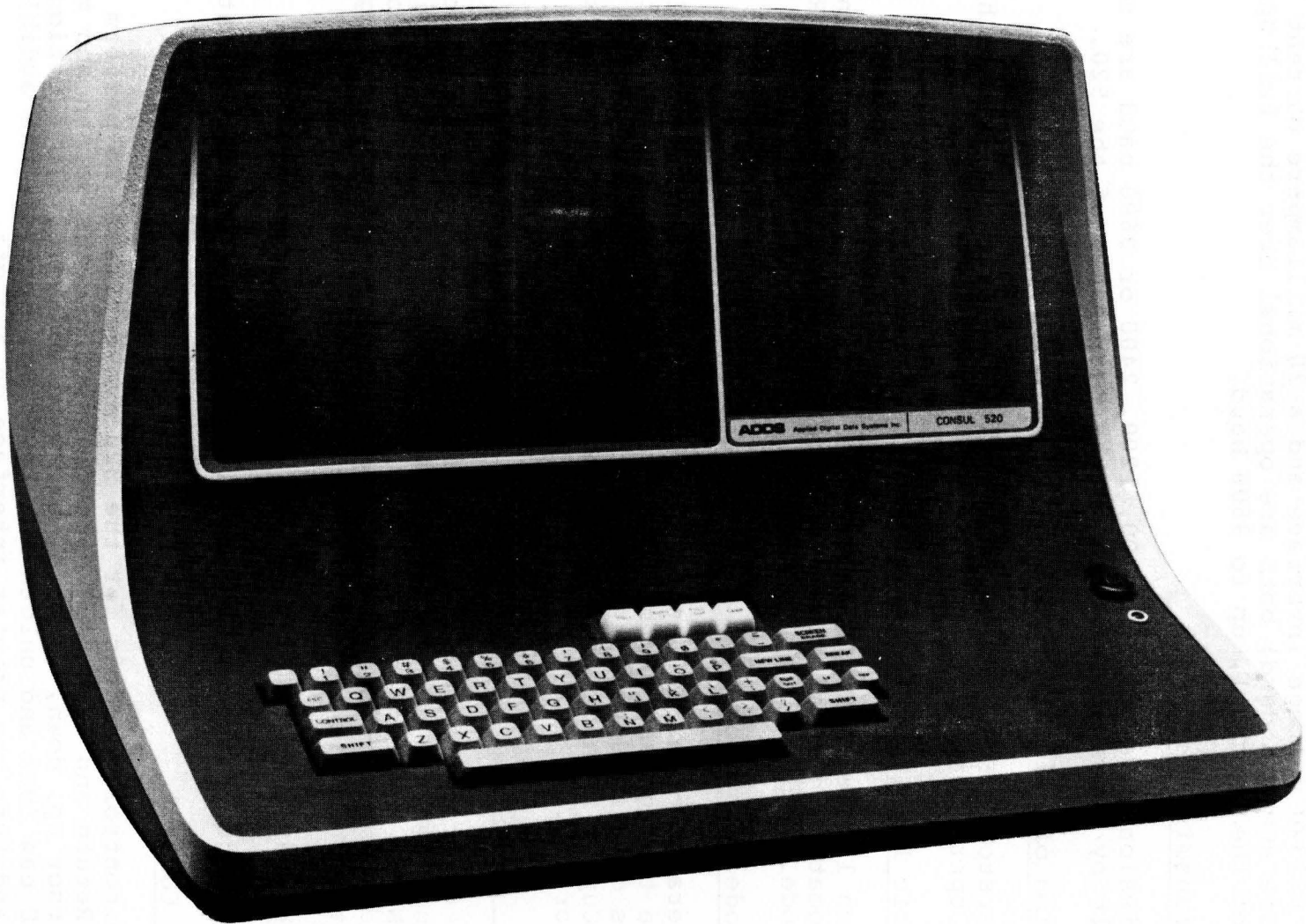
### Audible Alarm

The BEL code causes an audible alarm in the 520 to be activated.

### Remote Control

Remote control commands for the 520 are available to perform Carriage Return and Line Feed operations, erase the screen and move the cursor up, down, forward, backward and home. In addition, the CPU can lock and unlock the keyboard, activate the audible alarm and turn the printer interface on and off.

CONSUL 520



### Cursor Addressing

The computer can address the cursor to any given position on the screen. Addressing is provided by two command codes, a Vertical Address command and a Horizontal Address command. Each of these commands is followed by a character that determines the desired cursor position.

## SECTION 2:

### THEORY OF OPERATION

This section presents a block diagram overview of the 580 electronics, followed by a detailed circuit description at the chip level.

Diagrams which should be referenced when reading more than one page of the manual are designed as "fold-out" drawings to aid in following the discussion. An alphabetic Glossary of Signal Names is presented in Section 3 for convenience in following circuit descriptions.

#### GENERAL SUMMARY

The Consul 580 electronics package is made up of three basic blocks--the Front End, the Memory and Control logic, and the Video Generator. Each block comprises one printed circuit card.

#### Front End

The Front End block contains the Serial-to-Parallel Converter, EIA level shifters, TTY current loop converters, keyboard interface, the control decoding logic, the baud rate clock, and the RS232C control logic.

#### Memory and Control Logic

This block contains the Display Buffer memory, the one-line Refresh Buffer memory, cursor generation logic, scroll logic, and the logic necessary to control access to the Display Buffer memory.

#### Video Generator

The Video Generator contains the master oscillator counters for controlling all video signals, the video amplifier and mixer, sync and blanking generator, Memory timing generator, character generator, Display Buffer address register, and the Address comparison circuitry for memory input.

#### OVERALL BLOCK DIAGRAM DESCRIPTION (Figure 2-1)

The block diagram shows the three major sections divided by dashed lines.

#### Front End

##### 1. Input Data Path

Input data to the Front End can be either current loop or EIA serial data. The serial data stream is converted to TTL

levels and applied to the Serial-to-Parallel Converter (UAR/T, Universal Asynchronous Receiver/Transmitter) which changes the serial data to parallel data. The parallel data (a character) together with a strobe pulse, is presented to the decoding and control logic. If the character is displayable, it is presented to the Memory and Control Logic for input to the Display Buffer memory. If the character is an active control character (Erase, Carriage Return, Cursor Up, etc.) the control logic performs the proper task. If the character is from the sixth or seventh column on the ASCII chart (lower case), it is translated to columns 4 and 5 (upper case). All other characters and Rubout are ignored by the CRT.

## 2. Output Data Path

Output data is generated only by the keyboard. When the user depresses a key, the ASCII code, together with a strobe, is presented in parallel to the output character latch. If the proper conditions exist at the RS232C control logic, the character is passed on to the UAR/T with a strobe for parallel-to-serial conversion. The serialized character is then converted from TTL levels to EIA or current loop signals and passed on to the modem or CPU.

## 3. Full/Half Duplex Modes

Full/Half Duplex is controlled by a switch above the keyboard. In Full Duplex mode (switch depressed) the serial TTL output goes only to the level converters for output. When the FDX/HDX switch is in the Half Duplex position (released), the TTL output data is applied to the serial input of the UAR/T. This causes the character from the keyboard to be treated as an input character from the CPU.

## 4. RS232C Control Logic

The RS232C Control Logic handles all the necessary control lines to and from the serial data connector. Request-to-Send is raised when the first character of a message is keyed. As soon as Clear-to-Send is true (from the modem or CPU), the latched character is loaded into the UAR/T for transmission. The reverse channel signals SCF and SCA are also controlled by this logic.

## Memory and Control Logic

### 1. Access Control

The Access Control accepts control signals from the Front End and performs the task requested. These tasks include data input, erase functions, and scrolling. In addition, there is logic to generate the cursor and logic to handle the updating of the one line Refresh Memory.



## 2. Display Buffer

The Display Buffer memory is composed of MOS shift registers that recirculate their contents at a 1.6 MHz shift rate. The memory is modular in that it is divided into three sections. Each section has a capacity of 3840 bits or 640 6-bit characters.

## 3. Refresh Memory

The Refresh Memory has a capacity sufficient to hold 100 6-bit characters out of which only 80 are used for display. This MOS shift register is used to hold one line of characters during the time the Video Generator is generating that particular line of data on the T.V. screen. It is updated from the Display Buffer before the next line is to be displayed.

## Video Generator

### 1. Character Generator

The Character Generator accepts one character at a time from the Refresh memory and then outputs the proper portion of the character to be displayed. The line of characters in the Refresh memory is presented to the Video Generator seven times to complete the display of that data line.

### 2. Blank and Sync Generators

The Blank and Sync generators mix their signals with the display video to produce the proper signals to frame the data and drive the T.V. monitor.

### 3. Clock and Timing Chain

The Clock and Timing Chain is used to generate all the timing concerned with the video presentation and the memories.

### 4. Address Register

The Address Register contains the address of the next location in which a character may be entered into the Display Buffer.

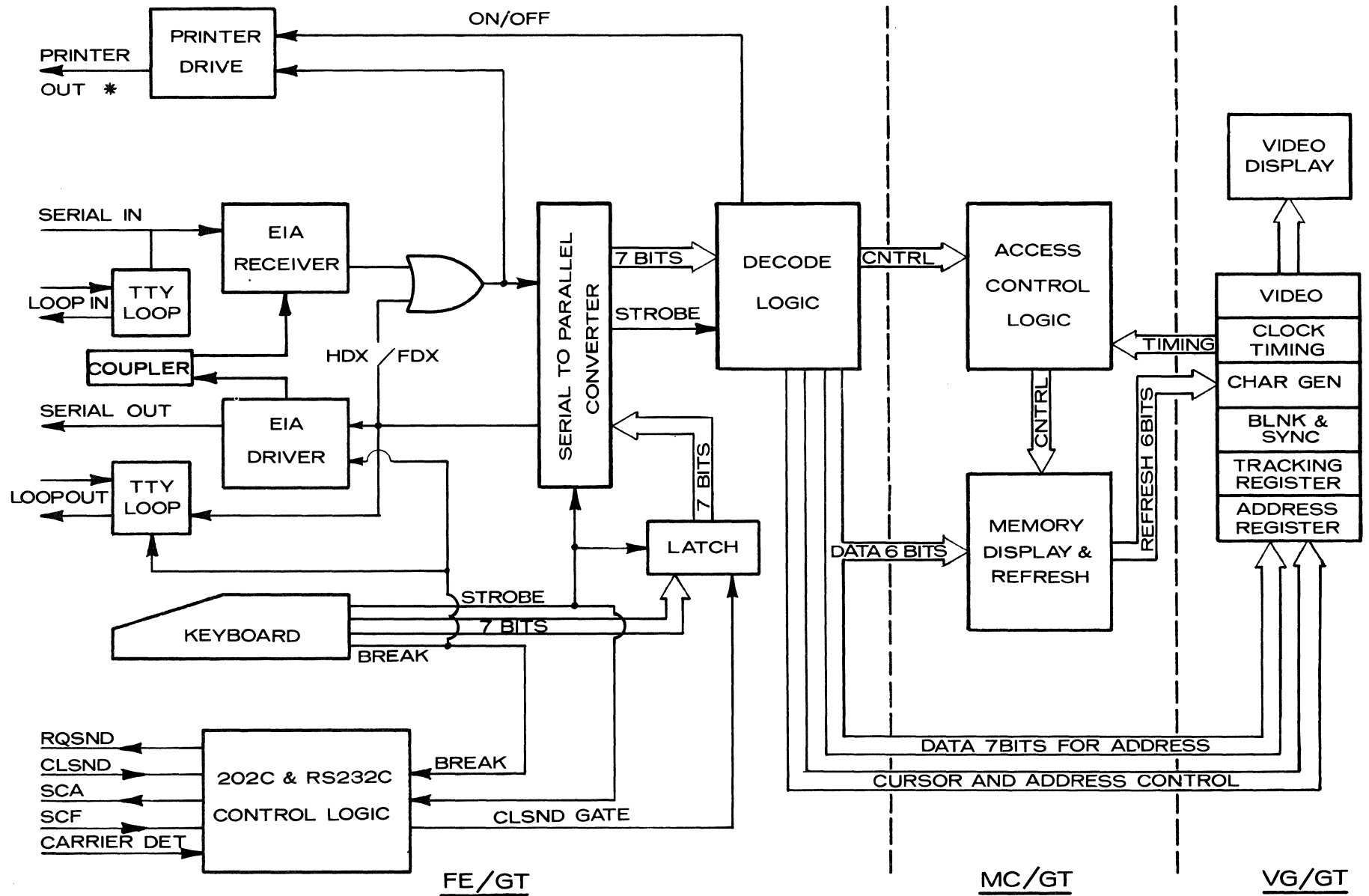
### 5. Tracking Register

The Tracking Register counts the shift pulses to the Display Buffer. Its contents at any given time contain the address of the Memory Buffer location that may be accessed.

# 520/580 BLOCK DIAGRAM

Fig. 2.1

\* PRINTER DRIVE LOGIC ON 580/380 ONLY



## DETAILED DESCRIPTION - VIDEO GENERATOR

The Video Generator will be discussed first because a large portion of the overall timing and control is generated by this P.C. card.

### Video Generator Block Diagram Description (Figure 2.2)

#### 1. Clock and Timing Chain

The heart of the Video Generator is the crystal clock and count down timing chain. The clock is a square wave generator with a frequency of 12.528 MHz. This is the video shift frequency or the rate at which the individual bits of a character are written on the T.V. screen.

The first counter divides this by 8 to a frequency of 1.566 MHz which is the rate at which complete characters are written on the screen. Timing is derived from this counter for all intracharacter clocks and strobes.

The character rate is then divided by 100 to produce the video scan line rate of 15,660 HZ. The signals Horizontal Blank, Horizontal Drive, and Horizontal sync are decoded from this counter.

The next counter divides by 9 to obtain the character line rate of 1740 HZ. Seven of the video scan lines are used to generate the data line and two are used for separation and the cursor mark. The counter outputs are used by the ROM (Read Only Memory) Character Generator to determine which one of the seven horizontal segments of a character should be output to the video.

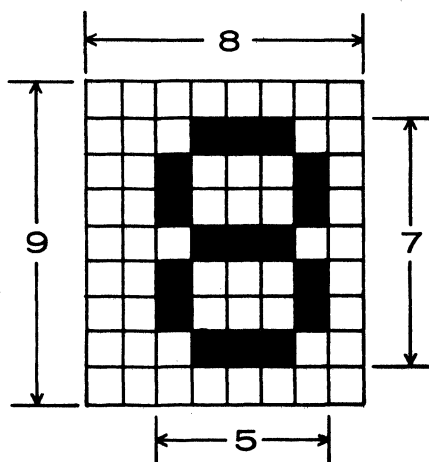
The last counter divides down to the screen refresh rate of 60 HZ (50HZ for overseas models). Signals such as Vertical Blank, Vertical Drive and Memory Select are obtained by decoding this counter.

#### 2. Character Generator

The 580 employs a 5 x 7 dot matrix to generate the 64 displayable characters. Each 5 x 7 character is displayed in an 8 by 9 field (see Figure 2-2). This gives a three dot horizontal spacing between characters and a two scan line spacing between rows of characters.

## CHARACTER MATRIX

Fig. 2-2



To generate a character on the screen the Read Only Memory, ROM, must supply seven five-bit words to the video shift register, one for each of the seven scan lines used to display the character. During each scan line at the given character position, the video shift register shifts the five bits to the video mixer at the 12.528 MHz rate. These bits make the video black for ones and white for zeroes, assuming a normal black on white presentation.

The pattern in the ROM is selected by the 6-bit (1 of 64) character latched from the Refresh Buffer memory. This 6-bit word is used as an address to select one of the 64 possible dot patterns. The three inputs S1, S2, and S4 are bits from the scan line counter which select which one of the seven five-bit words is to be output by the ROM.

### 3. Video Mixer and Amplifier

The character bits from the video shift register are mixed with Horizontal Blank, Vertical Blank, Interline Blank and the cursor mark. The Horizontal and Vertical blank signals always cause the screen to be black. The interline blank causes the screen to be white for black-on-white characters and black for white-on-black characters. The cursor mark always inverts the contrast of the interline blank signal.

The video amplifier takes the mixed signal and drives the internal monitor with a 0 to +5V signal. This same output is also resistively mixed with a composite sync signal to generate a 1V. peak-to-peak composite video signal for external monitors.

#### 4. Display Select Generator

Since the Display Buffer is divided into three modules, the video generator must select from one of the three sections to request a new line of characters. The outputs SECT 1 and SECT 2 are used by the Memory and Control card to load the Refresh Buffer memory with the proper line of data. SECT 1 and SECT 2 are low for the top third of the screen. SECT 1 is high for the middle and SECT 2 is high for the bottom. These two signals are obtained from the last counter in the countdown chain which is counting groups of 9 scan lines, or data lines.

#### 5. Internal Video Drive Generator

The internal monitor (Consul 580 only) requires separate signals for Vertical and Horizontal drive. These are TTL levels and are decoded from the timing chain.

#### 6. Memory Clock Generator

All the timing for the memory shift registers is obtained from the Dot Counter. The two phases  $\phi 1$  and  $\phi 2$  are TTL level 25% duty cycle pulses.

#### 7. Memory Address and Tracking Registers

The Memory Address register is made up of four counters. The first is a decade counter (0 - 9). The second is binary and counts from 0 to 7. These two counters together determine a single line (0 - 79 characters). The third counter counts from 0 to 7 which represents the number of 80-character lines in any one memory module. The last counter is a count of three (0 - 2) which determines which of the three memory modules is to be accessed. All four are synchronous up/down counters. The Address Counter is static and can be changed by the cursor controls or by direct addressing. The contents are automatically updated by an access to memory.

The Tracking Register is made up from three counters which are the same as the first three stages of the Address Register. This keeps track of the position of the circulating Memory Buffer registers. Since the three memory modules are running in parallel, only eighty characters (one module) have to be tracked.

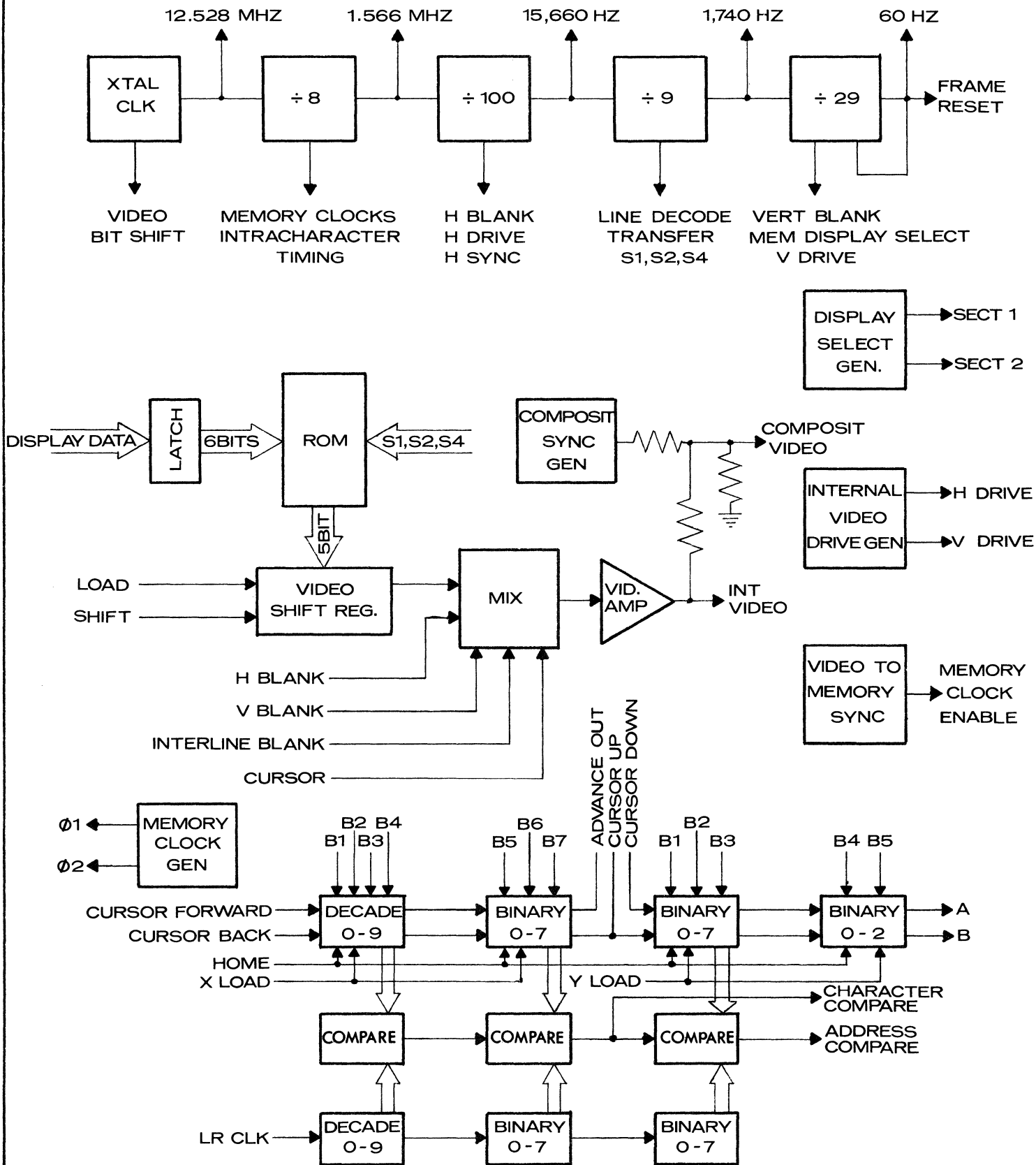
A comparison is made between the Tracking Register and the Address Register. When they have the same value it means that the Memory is at a position such that the character at the location indicated by the Address Register may be accessed. A sub-comparison of only the horizontal location (one of 80 positions) is also made and is used by the Memory and Control board to generate the cursor.

#### 8. Video to Memory Sync Circuit

When the Video Generator finishes a complete scan of the screen the Display Buffer memory is not in sync with the video. The memory sync circuit causes the memory to pause every other scan line until the system is back in sync again.

# VIDEO GENERATOR BLOCK DIAGRAM

Figure 2-3



## Circuit Description - Schematic #135-080

### 1. Clock and Timing Chain

The crystal oscillator is located in the upper left corner of the print. It consists of a common base amplifying stage Q1, driving an emitter follower Q2, which drives the crystal in the feedback path. The output signal is picked off the collector of Q2 to avoid disturbing the oscillator circuit and drives Q3 in switching mode. The diode, D1, is used to insure a symmetrical load on Q2 and also to protect the base of Q3 from excessive negative voltage. The collector of Q3 drives two Schottky hex inverters (L7,3 and L7,5) in parallel to provide the main clock signal, CLK.

The signal, CLK (12,528 MHZ), drives the first stage of the timing chain K7. K7 is an SN74175N, a quad D-type flip-flop. K7, the Dot Counter, is used as a Johnson or Ring counter. The stages are wired as a shift register with the last stage's complimented output fed to the first stage input. This causes the register to sequentially fill with ones, then zeroes. An entire period takes eight clock pulses. Since only one stage changes state at a time, any state may be decoded with a two-input gate. The three-input nand gate, J6, is used to insure that no illegal state, such as 1010, may exist for more than one period. All intra-character timing is derived from this counter.

The output of the Dot Counter, D4\* (1.566 MHZ or 639 nanoseconds) represents one character time and drives the decade counter chip J7. J7 is an SN74162 which is a synchronous decade counter. The carry output from J7,15 and the clock, D4\* drive the next decade counter H7. These two chips, the Character Counter, perform a divide by 100 which represents one video scan line including Horizontal sync and blank times. The period of this counter is 63.9 microseconds or 15,660 HZ.

The output of H7 is inverted and applied as C80\* to the input of F7, another decade counter. This chip is wired such that the output S8 is inverted and fed to the synchronous clear input on pin 1. When S8 goes high, the next clock signal at pin 2 will clear the chip to all zeroes, resulting in a divide by 9 function. This is the Scan Line Counter and its outputs S1, S2, S4, and S8 are used for timing within one data line of characters.

Finally, the output S8 drives a binary ripple-through counter consisting of E7, an SN7493N, and C7, an SN7474 wired in toggle mode. This is the Data Line Counter. For 60 HZ devices it counts 29 data lines (261 scan lines) and then is reset to zero. For 50 HZ the count is 35 data lines or 315 scan lines. The crystal frequencies 12.528MHZ for 60 HZ



devices and 12.6 MHz for 50 HZ devices were picked to produce a 60 HZ or 50 HZ refresh rate, while keeping the number of scan lines an integral of 9.

The signal RST1 is the reset signal for the Data Line Counter and is generated by the cross-coupled latch B7,3 and B7,6. The latch is set by the four-input nand gate D7,5. Its output goes low for a count of 29 or 35, setting B7,3 high. The other half of the latch is driven by D4\* which has just gone true. One half character later D4\* goes false, resetting the latch. Meanwhile, RST1 has reset E7 and RST1\* has reset both halves of C7. K7, J7, H7 and F7 returned to zero when E7 and C7 reached the reset count.

## 2. Horizontal Timing

### a. Horizontal Blank

The Horizontal Blank signal determines the size of the white page on the screen in the horizontal dimension. One character space is left at each end of the 80-character line to form a border, resulting in an 18-character time blank signal. HBLANK (A6,6) is set true when a count of 97 (C80, C10, C4, C2, C1) is reached by B1,8 going false. C10C4G is a combination of C10 and C4 with a Strobe CLK\* (see three-input "and" gate E6,6). HBLANK resets at a count of 15 (C80\*, C10, C4, C1), resulting in a blank time of 18 characters.

### b. Horizontal Drive

HDRIVE is used by the internal monitor to develop the horizontal sweep. It begins with HBLANK and ends at character position 31 (C20, C10, C1).

### c. Horizontal Sync

This signal is needed by an external monitor in order to synchronize its horizontal oscillator. It is contained within the combined sync circuit (section F-4) and is the output of E6,12. It starts during HDV when C8 returns false (character position 0) and lasts until C8 goes true again (C10 and C20 are low). When C8 goes false again, either C10 or C20 is high, keeping E6,12 low. This results in a horizontal sync pulse lasting for 8 character times or 5.1 microseconds.

### d. Data Gate

DATAGT is a signal lasting for 80 character times or 51 microseconds. This period is the time during which the Display Buffer memory shifts (80 shifts). During the balance of the scan line time (12.8 microseconds) the

memory pauses. DATAGT is used to begin the shifting and also to gate one line of data from the Display Buffer to the one-line Refresh Buffer.

DATAGT is the output of a cross-coupled latch (section G-4) B7,11. Since there is a one character delay time through the ROM, DATAGT must start one character time before the first character is displayed on the screen. Since there is a one character boundary, DATAGT may begin when HBLANK ends. Note that B7,13 is driven low by the same signal that resets the HBLANK latch (HBRST\*). HBRST\* occurs at character position 15. For 80 characters, therefore, DATAGT must end at character position 95. Note that J6,12 will pulse low at location 95 (C80, C10, C4, C1, CLK\*). The input CLK\* is used as a strobe to insure no false clocking.

### 3. Vertical Timing

#### a. Vertical Blank

The vertical blank signal, VBLNK (Section F-1) is generated by a cross-coupled latch A2,8. This signal determines the top and bottom borders of the white page. To allow for one scan line under the cursor in the bottom line, one scan line is added to the page after the last data line. To keep the page symmetrical, a scan line is also added to the top of the page, allowing two scan lines of white above and below the top and bottom data lines.

For 60 HZ devices, VBLNK starts when scan line one, SL1, goes true during data line 28 (L16, L8, L4). VBLNK remains true until scan line 9 (S8 true) of data line 3 (L16\*, L2, L1) goes true.

For 50 HZ devices, VBLNK begins during data line 32 and ends during data line 7.

#### b. Vertical Drive

VDRIVE (Section E-1) is used by the internal monitor and as part of combined sync by the external monitor to initiate the Vertical flyback. It starts with the reset pulse RST1 and ends when L1 returns true 9 scan lines later.

#### c. Memory Module Selection

Since the three sections of the Display Buffer memory are multiplexed at their outputs, the proper section must be selected for input to the one-line Refresh memory. The signals SECT 1 and SECT 2 control this gating and are generated by the flip-flop pair A6 in Section E-4.

VDRIV\* is used to set both flip-flops to zero, which selects Display Buffer module 2. The gating is done on the Memory and Control board. When the first eight data lines have been displayed, A4,12 pulses low (Data line 11 + Scan line 1) setting A5,9 true. This conditions the Memory and Control card to present the next 8 data lines from the second memory module. After 8 more data lines, A4,8 pulses low (Data line 19 + Scan line 1), re-setting A5,9 and setting A5,5 which causes the Memory and Control card to present the last 8 data lines from the third memory module. For 50 HZ, these decodes are all increased by 4 Data lines to center the display in the larger number of scan lines.

#### 4. Character Generation and Video Mixing

##### a. Basic Dot Matrix

As mentioned earlier, the 580 uses a 5 x 7 matrix to generate the displayable characters (see Figure 2-4). The character field is an 8-dot wide by 9-scan line high "window." The character is generated within this field in dot positions 2 through 6 and scan lines 1 through 7. It is evident that the ASCII character information for R and S must be available for at least seven scan lines sequentially in order to generate the two characters or the entire line. Each time a scan line is swept across, a 5-dot portion of the character is generated.

The data line consists of 82 windows, 80 of which are used to display characters. The first and eighty-second windows are always spaces and are used as a margin for the white page. There are 24 such data lines in an entire page for a total of 1920 characters.

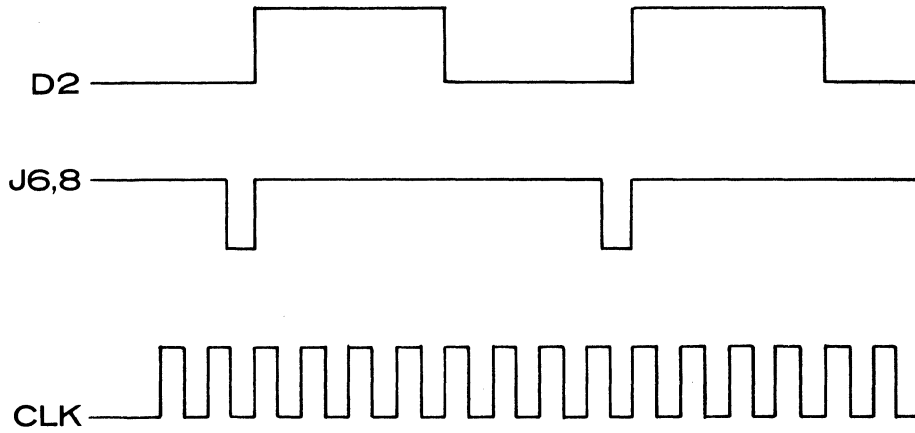
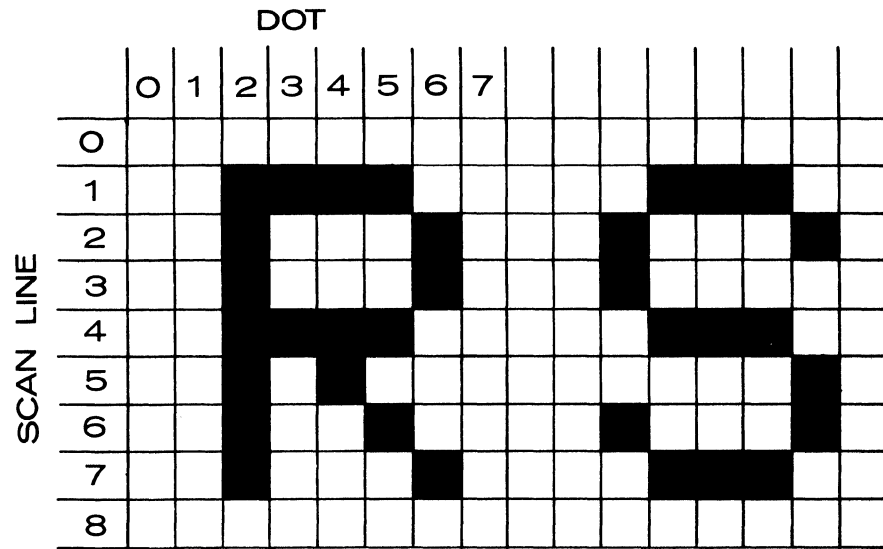
##### b. Read Only Memory (ROM)

A ROM (Section E-6) is used to store the 64 displayable patterns of 5 x 7 dots. Each pattern is broken down into seven 5-dot words or slices.

Each of the patterns or cells is associated with a 6-bit address (0-63). This address is the same as the ASCII code for the character. For example, the ASCII code for an R is 010010 (bit 6 through bit 1). This indicates cell #18 which contains the bit pattern for an R. Each five-dot word is addressed by three bits (0-7). The Scan Line Counter bits S1, S2 and S4 are used to address the proper word within a cell. For example, the third 5-bit word of an R pattern is 10001 and is addressed by S1=1, S2=1 and S4=0, which is the state of the Scan Line Counter during the third scan line. The ROM supplies the 5-bit word in parallel at its outputs that corresponds to the selected word in the selected cell.

# SEQUENTIAL CHARACTER GENERATION

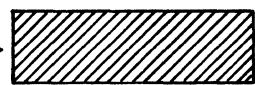
Fig.2.4



ASCII CHARACTER "R" LATCHED IN J6

5 BIT PATTERN FROM ROM FOR ONE SCAN LINE LOADED INTO SHIFT REGISTER L6

5 BIT PATTERN FOR "S" SHIFTED TO VIDEO MIXER



The ROM used is a static design, which means that the word appears at the output as long as the input address remains stable. Upon an Address change, for instance, from the R to the S, that output change is guaranteed to become stable within a maximum of 600 nanoseconds. The character change rate is 639 nanoseconds.

c. Generation of One 5-Bit Character "Slice"

Since the worst case delay through the ROM is 600 nanoseconds, a one-character delay is used to allow time for the first character in a line to set up. Using the S as an example in Figure 2-4, note that the ASCII code for S is latched in the holding register J3 by the signal D2; DATAGT became true on the leading edge of D1, allowing D2 to clock the flip-flops. The 5-bit word for the scan line determined by S1, S2 and S4 is stable at the inputs of L6 prior to the load pulse at J6,8. When J6,8 pulses low, the 5-bit word is transferred to the shift register L6. The next clock pulse (CLK) on L6,2 shifts the bit pattern by one stage and applies the first bit of the word to the output pin 7. A one in the bit pattern will produce a high level in the shift register and a zero will produce a low level. For the fourth scan line, the 5-bit word would be 01110 which would produce the horizontal middle three dots of the "S." As the first dot of the "S" word is shifted into the output stage, the next character to be displayed is latched in the holding register J3.

The output of the shift register is then "ANDed" with a signal that is true for scan lines 1 through 7 and false for 0 and 8. For a black-on-white presentation, the jumper JP1 is installed, which enables AND gate E5,5 when the CURSOR signal is low. The character bits are passed by E5 to C1 which inverts the level. B5,1 then inverts again and drives the base of Q4. For a "one," B5,3 is true which turns Q4 on. This causes a low level (0.7V) at the collector and drives the emitter of Q5 to 0 volts, which is black on the CRT. A zero bit level causes a +4.3V level at the emitter of Q5 which is white on the CRT. The capacitor C13 is to shape the signal suitably for the monitor's input amplifier. At the same time the internal monitor is receiving a 0 or +4.3 volt signal, the external monitor receives a 0.3V to 1V signal through the resistor network R34, R35, and R36. (CMBSN\* is normally high.)

d. Blank Mixing

In Section F-5 the Vertical Blank, VBLNK, and the Horizontal Blank, HBLNK, are applied through the NOR gate C1,11 and C1,13 to one input of the NAND gate B5,2. When either level is high, B5,2 is blocked, causing B5,3

to be high, which in turn causes black on the CRT screen, regardless of the state of the data signal on B5,1.

e. Combined Sync Mixing

The signal CMBSN\* in Section E-2 is normally high. At the end of each scan line it pulses low for 5 microseconds to provide a 0V level signal at the external video output (.3V sync, .7V video). At the bottom of the screen, CMBSN\* goes low for 9 scan lines to generate the vertical interval step for vertical flyback. The diodes D9 and D10 are to protect the external output from a monitor failure.

f. Miscellaneous

The discrete components around the ROM are needed to supply the proper levels to the device. Input levels must be between ground and +13V. The output drives must be sunk to a negative voltage and caught at +5V by diodes D2-D6 to operate properly with TTL circuits.

In the Video amplifier circuit, the Zener Diode D7 is used to establish a stable +5V switching level independent of TTL switching noise.

The signal CURSOR is generated by the Memory and Control P.C. card. It goes true for 639 nanoseconds in Scan Line 8 under the character whose address is held by the Memory Address Register. This causes an inversion in the background which results in a black underline or white underline, depending on the screen background presentation.

5. Address and Tracking Register

The address of the next Display Memory location to be accessed is held by the Memory Address Register consisting of L3, K3, D5 and C6. L3 is an SN74192N, a synchronous up/down decimal counter. This drives K3, and SN74193N, which is a four-stage synchronous up/down binary counter. The two in tandem count from 0 to 79 (only the first 3 stages of K3 are used) or one 80-character line. This portion indicates the horizontal position of the character. The next counter is another SN74193N and is used to indicate which of the eight lines in one memory module contains the character of interest. Finally the two D-type flip-flops of C6 are wired as a synchronous up/down tertiary counter (count of three). This last counter is used to indicate in which of the three memory modules the character location of interest lies.

The Tracking Register is counted by the shift pulse (2) of the Display Memory and indicates which location in any given module is available for access. Its output is stable for one character time and increments at a 1.566 MHz rate. This register is constructed in the same way as the Address Register in that the first stage is a decade counter, followed by a binary counter. Since the three memory modules are shifting together in parallel, only eight lines of 80 characters (one memory module) need be tracked. The last stage of E3 and the two stages of D3 make up the 0-7 counter for the line portion. F3 and the first three stages of E3 made up the character portion.

The three chips F4, E4 and D4 are dual four-bit comparators. These three chips are used to generate a signal that indicates when the memories are at the location held by the Address Counter. This is done by comparing the contents of the character and line portion of the Address Register with the Tracking Register. F4 and E4 compare the character portions and generate a signal named CHCOM, Character Comparison. The output of E4 is gated by COMENB (Comparison Enable) which is true when the memories are not pausing for line end or memory synchronization.

CHCOM is then used with the output of D4 to generate ADDCOM (Address Comparison), the combination of CHCOM and the Line Counter comparison. ADDCOM lasts for 639 nanoseconds and occurs every 510 microseconds, except during the memory synchronization time, during which it occurs every 574 microseconds.

The Address Counter is controlled in two basic ways, incremental control and direct addressing. The incremental control is by use of the cursor position keys. The signals generated by the control keys are CURFR\* (Cursor Forward Not), CURBK\* (Cursor Back Not), CURUP\* (Cursor Up Not), ADV\* (Advance Not, which is cursor down) and HOME. CURFR\* is also automatically pulsed when a memory location is accessed. The signal ADV\* is generated from the Cursor Down key or the Line Feed key. It is also automatically generated when the last character in a line is accessed if the terminal is in the Auto Line Feed mode.

The circuitry around L3 is used to insure that an illegal address (greater than 9) cannot be stable in the decade register. If stages 2 or 3 are true when stage 4 is true, indicating a number greater than 9, H3,1 will go true. After a delay of 300 nanoseconds (R37 and C19) the reset input L3,14 goes true and resets the counter to all zeroes. The reset level lasts for 300 nanoseconds because of the delay.

The circuitry below K3 is used to generate the line up or down signals necessary when the cursor is made to move from one line to another by forward or backward motion. ADV1, H4,8 pulses low when the first three stages of K3 are true (7) and the up count signal, L3,12 pulses low setting the first three stages back to zero (the fourth stage is not used). The two nor-gates H3,10 and H3,13 decode the zero state of the counter and the down count pulse to cause the Line Counter D5 to count down one count. In a like manner, the up and down counts for the tertiary counter, C6, are generated at B2,10 and B2,4.

For the count of three functions, the flip-flops of C6 are wired in toggle mode. The input clocks are pulsed only when that given stage should change state. For example if C6,9 is true and C6,5 is false then both should change for a down count. The gating structure of D6 with its inputs implements the proper pulses to make C6 operate as an up/down synchronous, tertiary counter. Using the previous example, an up count could cause a positive pulse at B2,10. Since B\* is true there will be a clock via D6,1 and 13 to C6,11 which changes C6,9 from a one to a zero. At the same time, since C6,9 was true, A\* (C6,8) was false causing B5,6 to be true. This enables the other half of D6 (pins 4 and 5) and causes a clock at C6,3 changing C6,5 from a zero to a one. Note that if a down count occurred, B2,4 would pulse true and only D6,10 is enabled therefore affecting only C6,5.

The nand gate C4,11 is used to insure that the illegal state of  $A = B = 1$  is not stable. If A and B were both true, C4,11 would go low causing a reset at C6,1 lasting for 300 nanoseconds. The second control mode for the Address Register is by direct addressing. For a horizontal address input XLOAD\* pulses low and the registers L3 and K3 are loaded with an address determined by the levels of B1 through B7. The three most significant bits B5-B7 select which group of 10 locations (0-9, 10-19----70-79) will be addressed. Bits 1 - 4 select which one of the locations within a group is addressed (0 - 9). The vertical address is input when YLOAD\* pulses low. B1 - B3 then indicate which line in a group of 8 is addressed. B4 and B5 indicate which group of 8 or which memory module is addressed.

## 6. Memory to Video Synchronization

To explain why synchronization is necessary, the following explanation is given of the method used to transfer data from the Display Memory to the one-line Refresh Memory.



As mentioned before, the Display Buffer Memory is divided into three modules of 640 characters each (8 lines of 80). These modules are shifting together with their inputs and outputs multiplexed for access and display. At the top of the white page the first memory module must be ready to transfer the first line of 80 characters to the one line Refresh Memory. This indexes the memory by one line of eighty characters. During the next 8 scan lines the Display Memory shifts for 8 more lines. It is then back to the same relative position as when it completed the transfer of the first line (line 0) to the Refresh. The first line was transferred when the Scan Line Counter F7 was at a count of 8. (The characters are generated in lines one through seven.) After the bottom scan of the characters the Display Memory is ready to shift the next line of characters (line 1) to the Refresh Memory. This process continues until all eight lines have been transferred. Now the Display switches to the second memory for 8 more lines of characters and then to the third module for the bottom eight lines.

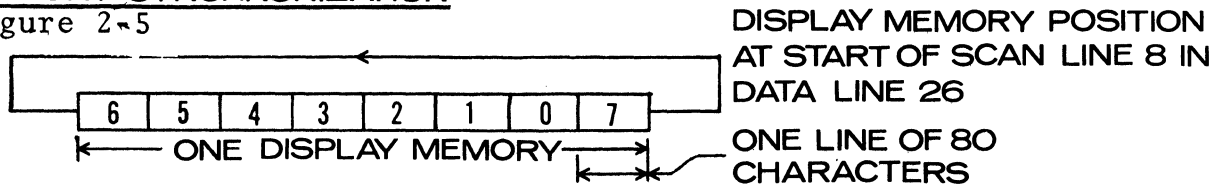
Referring to Figure 2-5, the last line transfers to the Refresh Memory during scan line 8 of data line #26. The memories continue to shift as if they were loading data for two more data lines. At the end of these two data lines the video begins the vertical flyback (RST1 pulses at the end of Data Line 28). When the Video Generator is ready to display the first line on the screen, line 0 of memory module 1 must be ready to transfer to the Refresh Memory. In order to achieve this, the Display memories must be in synchronism with the Scan Line Counter. That is, line 0 in the Display Memory must shift through the output during scan line 0, memory line 1 with scan line 1, etc., in order for memory line 0 to be ready to shift into the Refresh Memory during scan line 8.

When RST1 pulses, the synchronization circuit in sections D1, 2 and 3 begins to lock the memory to the Video Generator. This is done by causing the memories to pause every other scan line until memory line 0 is shifting during scan line zero. The memories are always shifting in groups of 80 shifts in sync with the Video scan line so only the line portion must be brought back into lock.

When the Scan Line Counter outputs S1, S2 and S4 and the Tracking Register outputs TR1, TR2 and TR4 are the same, the memory is in sync with the Video. By not allowing the memories to shift during scan line 8, the memories will remain in sync until the first line is needed, at which time the memories will shift during scan line 8 again.

**MEMORY SYNCHRONIZATION**

Figure 2-5



MEMORY POSITION AT BEGINNING OF SCAN LINE								SCAN LINE	DATA LINE
7	6	5	4	3	2	1	0	0	
0	7	6	5	4	3	2	1	1	LAST DATA LINE DISPLAY
1	0	7	6	5	4	3	2	2	
2	1	0	7	6	5	4	3	3	
3	2	1	0	7	6	5	4	4	
4	3	2	1	0	7	6	5	5	
5	4	3	2	1	0	7	6	6	
6	5	4	3	2	1	0	7	7	
7	6	5	4	3	2	1	0	8	
0	7	6	5	4	3	2	1	0	VERTICAL BLANK BEGINS
1	0	7	6	5	4	3	2	1	
2	1	0	7	6	5	4	3	2	
3	2	1	0	7	6	5	4	3	
4	3	2	1	0	7	6	5	4	
5	4	3	2	1	0	7	6	5	
6	5	4	3	2	1	0	7	6	
7	6	5	4	3	2	1	0	7	
0	7	6	5	4	3	2	1	8	
1	0	7	6	5	4	3	2	0	RST1 PULSES LOW PAUSE IN SHIFTING PAUSE IN SHIFTING MEMORIES IN SYN
2	1	0	7	6	5	4	3	1	
2	1	0	7	6	5	4	3	2	
3	2	1	0	7	6	5	4	3	
3	2	1	0	7	6	5	4	4	
4	3	2	1	0	7	6	5	5	
5	4	3	2	1	0	7	6	6	
6	5	4	3	2	1	0	7	7	
7	6	5	4	3	2	1	0	8	
7	6	5	4	3	2	1	0	0	PAUSE IN SHIFTING
0	7	6	5	4	3	2	1	1	
1	0	7	6	5	4	3	2	1	
2	1	0	7	6	5	4	3	2	PAUSE DURING SCAN LINE 8 OF DATA LINES 1&2
3	2	1	0	7	6	5	4	3	
4	3	2	1	0	7	6	5	4	
5	4	3	2	1	0	7	6	5	VERT BLNK END FIRST LINE OF DISPLAY SHIFTED INTO REFRESH
6	5	4	3	2	1	0	7	6	
7	6	5	4	3	2	1	0	7	
0	7	6	5	4	3	2	1	8	SECOND LINE LOADED
1	0	7	6	5	4	3	2	0	
2	1	0	7	6	5	4	3	1	
3	2	1	0	7	6	5	4	2	
4	3	2	1	0	7	6	5	3	
5	4	3	2	1	0	7	6	4	
6	5	4	3	2	1	0	7	5	
7	6	5	4	3	2	1	0	6	
0	7	6	5	6	5	2	1	7	
								8	

BALANCE OF 1, 2 AND START OF 3

Referring to the schematic drawing, the signal RST1\* pulses low at the vertical flyback time setting the flip-flop B4,9 true. One effect of this is to enable NAND gate A2,2 allowing S8 when true to go high which on the Memory and Control board blocks the clocks that cause the Display memories to shift. DATAGT goes true during the 80 characters shift period and is used to gate the signal MCLKDS (Memory Clock Disable). Since B1,3 is enabled during synchronization, DATAGT is blocked during S1 true and the fact that the memories are not in sync yet (B1,4 true). The result is that the memory clocks are disabled during the time S1 is true until a true comparison is achieved. It takes two pauses to reach sync because the memories were out of sync by 2 lines when RST1\* pulsed low. When synchronization occurs, F6 causes C3,12 to be low which disables B1,6 allowing A2,5 to go true every scan line for 80 shifts. From this point on, the memories pause only during scan line 8 to maintain sync. Vertical Blank goes true at the start of scan line 8 in Data Line 3. This transition is used to set B4,9 back to zero allowing the Display memories to shift during scan line 8.

#### DETAIL DESCRIPTION - MEMORY AND CONTROL

##### Memory and Control Block Diagram Description (Figure 2-6)

#### 1. Display Memory and Refresh Memory

The Display Memory stores the 1920 characters displayed on the CRT screen. Each character position requires 6 bits because the displayable character set consists of 64 different characters. The memory is a group of 9 MOS dynamic shift registers. These registers are arranged in three modules of 640 characters each, with 6 bits for each character. The memories shift at the Video character rate of 1.6 MHz. One module has six 640-bit shift registers running in parallel such that a new 6-bit character appears at the module output every 639 nanoseconds. The outputs from each module are returned to the inputs so that the data renews itself in the memory constantly.

In the block diagram, Data 1 is the 6-bit output of memory module 1 and is returned to the input via the input multiplexer. In order to enter data, the recirculation path of Data 1 is broken for one shift period and new data (INPUT DATA) is gated to the memory input by the input multiplexer and shifted into the memory instead. After the new data has been shifted in, the recirculation path is again closed and the new data remains in memory.

The three memory modules also shift together such that three characters are shifted at a time, one in each module. When data is entered, the input multiplexer breaks the proper recirculation path. The Display Memory clocks are gated in 80-pulse bursts and stopped for 20 character times every scan line such that it takes 8 scan lines to shift 640 times, a complete cycle.

In order for the Video Generator to display a line of characters, it needs the 80 character codes for that line at least 7 times for 7 sequential scan lines. The Refresh memory is used to store the one line of 80 characters for 9 scan lines (7 of which are actually used to generate characters). The Refresh memory consists of six 100-bit shift registers in parallel which shift at the Video character rate of 1.6 MHz. The display select and recirculation control logic transfers one line of 80 characters from the proper Display Memory module to the Refresh memory once every nine scan lines. It does this by breaking the recirculation path of the Refresh memory for one scan line and allowing the data from one of the Display memories to be shifted in. Only the 80 positions filled by the one line of characters are used by the Video Generator. The clocks to the Refresh memory are not gated since the memory is the same length as one scan line (100 characters).

## 2. Access Logic

The access logic controls the input of a character to the Display Memory. The inputs A and B select which module is to be accessed. When the memories are in such a position that the character to be replaced is ready to be shifted from the output back to the input (Address Comparison true), the proper load pulse (LOAD 1, 2 or 3) pulses true. The load pulse causes the recirculation path to break for the one character time necessary to shift in the new data. The signal CLRG is used to force space code into the inputs of the memory modules for an Erase function.

[For units delivered before January 15, 1974, note that the force signals are CLEAR 1, 2, and 3. Also note that space code was forced for Carriage Return as well as for the Erase function.]

## 3. Scroll Logic

This section controls the scrolling of data up the screen. When the Memory Address register indicates the cursor is in the last line (LSTNE true) and the Video Generator indicates that the Address has just gone through the last position

on a line (ADV1\* pulses low), the circuit causes a scroll. At the same time the signal normally causing the Memory Address to change by a line (ADV\*) is not allowed to pulse. Scrolling is accomplished by making the three memories into one memory of 1920 characters for 80 shifts. This is done by gating the output of memory #2 to the input of memory #1, and memory #3 to memory #2. Space code is input to memory #3. Thus all data is shifted up by 80 characters, or one line.

This circuit also blocks the ADV\* signal normally generated by a Carriage Return when the terminal is not in Auto Line Feed mode. The ADV\* then pulses for only cursor down or Line Feed (same code).

#### 4. Cursor Generation

The cursor is generated as follows:  
When Address Comparison is true during Scan Line 8 it means that the character of interest is being loaded into the Refresh memory. The next time Scan Line 8 goes true the cursor must be generated in order to place it under this character. When the signal Character Comparison goes true during the next Scan Line 8 the cursor signal is generated after being delayed by one character time. The delay is necessary because of the one character delay through the ROM character generator. On the Video Generator card the CURSOR pulse inverts the background level causing the underline mark.

### Circuit Description - Schematic #135-152

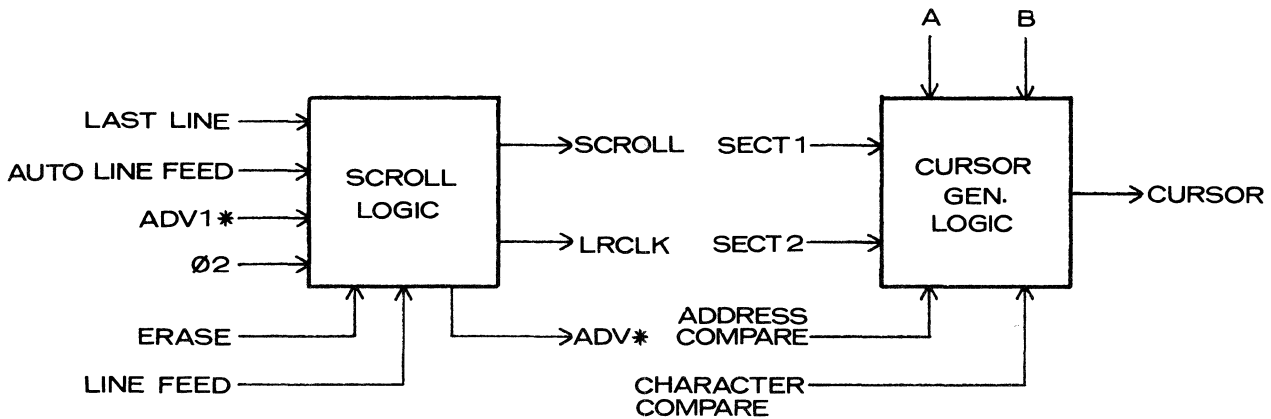
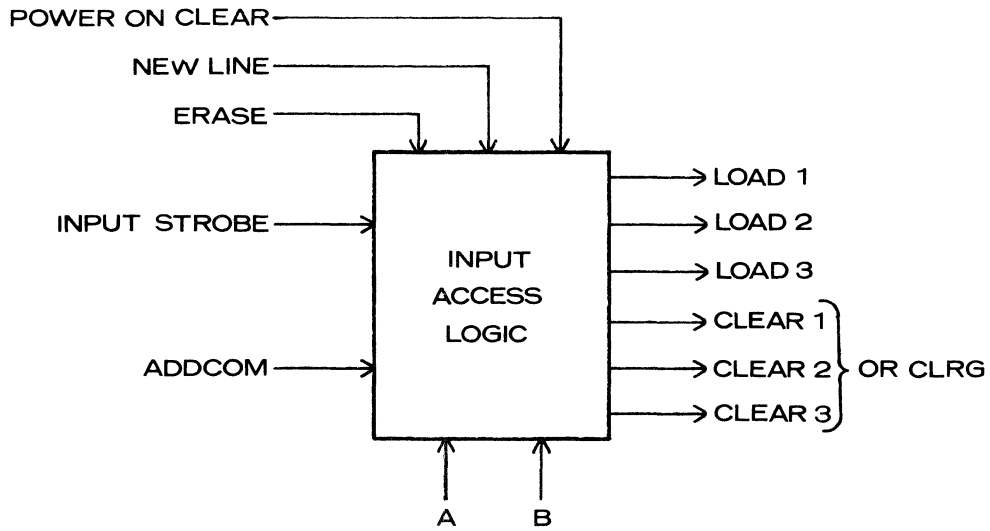
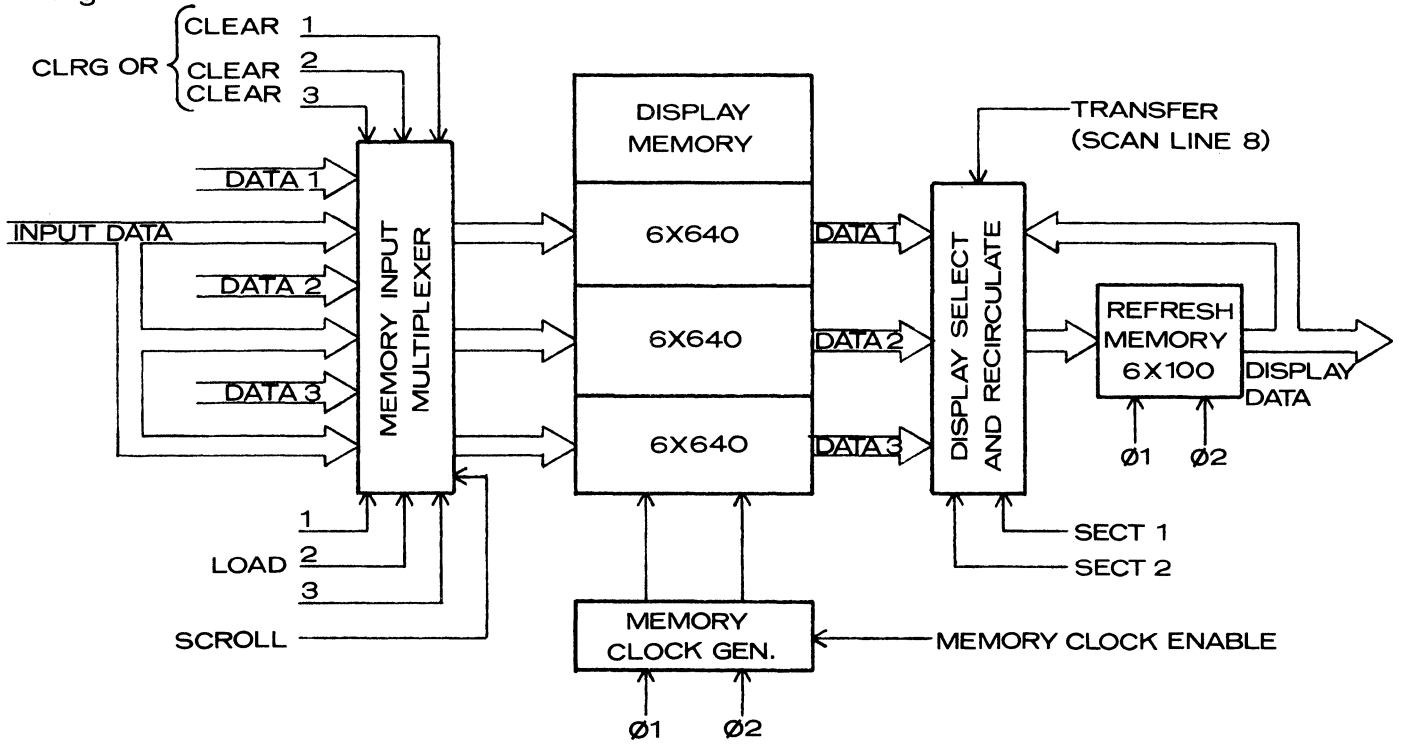
#### 1. Display and Refresh Memory

The Display Memory is a group of shift registers running in parallel and recirculating their contents from output back to print. A single bit is composed of a dynamic shift register 640 bits long. Six such register combinations make up one 6 x 640 bit memory module. Three memory modules make up the entire Display Memory of 1920 6-bit characters.

The dynamic registers are dual 640 bit N-channel MOS devices, MM5869. Memory module #1 consists of K5, L5, and H5. Bit 1 of module #1 will be used to show the recirculation path. The data path around the memory is as follows: The output is K5 pin 5 buffered by the AND gate L6,3 and is named M1. M1 is positive for 1 and zero for a 0. M1 is applied to the input of the dual four-bit multiplexer L7,13. Normally this input is passed on the the output L7,9. L7,9 is tied to the input of K5 completing the recirculation path. (For the 135-081 P.C. boards see the next page a) for the above two paragraphs.

# MEMORY & CONTROL BLOCK DIAGRAM

Fig.2-6



The Refresh memory is made up from three dual 100-bit dynamic shift registers D3, E3, and F3. Referring to Figure 2-7 on the next page, note P1\* and P2\*. These two pulses occurring during one character period are used to generate the clocks to shift the Refresh register C1RR and C2RR. D2 is a dual MOS clock driver which outputs the +5 volt to -12 volt clocks C1RR and C2RR. These clocks are not gated because the length of the register equals the number of character positions in a scan line. The data in the Refresh memory is recirculated by the two quad 2-input multiplexers H4 and F4 which normally pass the buffered outputs B1V-B6V to the inputs of the registers. S8 is true during the ninth scan line and gates the data from the Display Memory to the input of the Refresh memory to update its contents for the generation of the next character line.

The three dual four-line-to-line multiplexers L4, K4 and J4 are used to select which Display Memory module will load the Refresh memory; Module 1 when SECT1 and SECT2 are low, Module 2 for SECT1 = 1 and SECT2 = 0, Module 3 when SECT1 = 0 and SECT2 = 1.

The clocks for the dynamic portion of the memory are PH1 and PH2. These are generated from P1\* and P2\* gated with Memory Clock Disable, MCLKDS, which is low for 80 character times. The transistors are necessary to supply the current for changing the memory clock inputs. The static memory clock is generated from C1LR, (C8,10) by the one-shot J8 is approximately 200 nanoseconds long, SFCLK.

a) Display and Refresh Memory (Schematic #135-081)

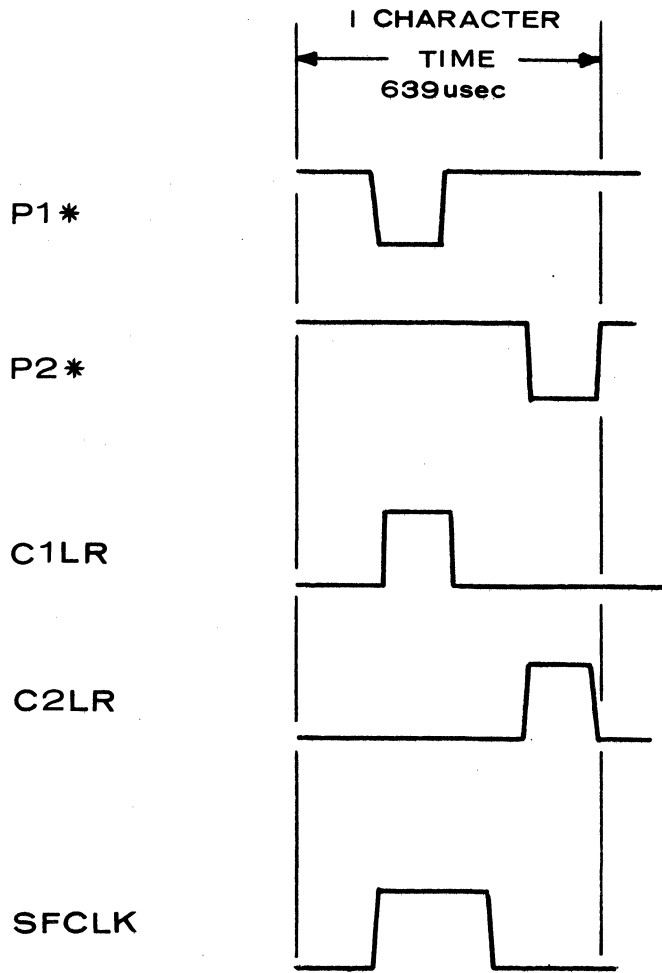
The Display Memory is a group of shift registers running in parallel and recirculating their contents from output back to input. A single bit is composed of a 128-bit static register in series with a 512-bit dynamic register to make a single shift register 640 bits long. Six such register combinations make up one 6 x 640 bit memory module. Three memory modules make up the entire Display Memory of 1920 6-bit characters.

The static registers are quad 128 bit devices, MM5055. The dynamic registers are dual 512 bit devices, MM5017. Memory module #1 consists of K6, 1/2 of H6, K5, L5, and H5. Bit 1 of module #1 will be used to show the recirculation path. The data path around the memory is as follows:

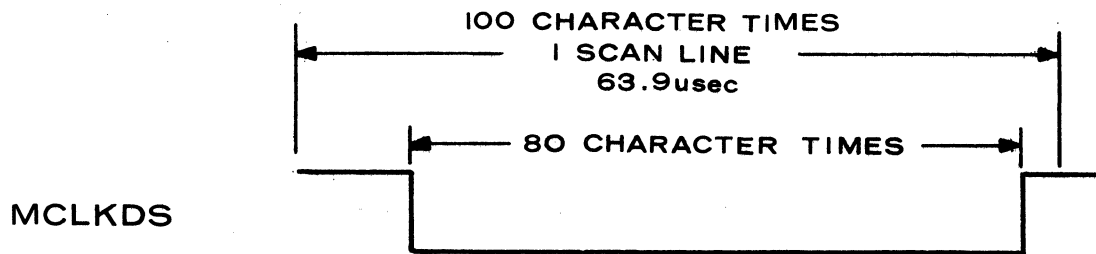
The output is K5 pin 5 buffered by the AND gate L6,3 and is named M1. M1 is positive for 1 and zero for a 0. M1 is applied to the input of the dual four-bit multiplexer L7,13. Normally this input is passed on to the output L7,9. L7,9 is tied to the input of the static register K6,2 whose output K6,14 drives the input of the dynamic register K5,3 completing the recirculation path.

Fig. 2-7

TIMING WITHIN ONE CHARACTER



MEMORY SHIFT TIMING FOR ONE SCAN LINE





## 2. Access Logic

### a) Access for Standard Displayable Characters

When an input to the Display Memory is to be made, the signal ACCESS in section F8 pulses true. This sets the flip-flop A8,9 true, enabling AND gate C4,5 and resetting flip-flop A8,6 true. When ADDCOM is true, indicating that the Display Memory is in the correct position for input, the D input of flip-flop D4,2 is enabled. The clock input to D4 is the inverse of P1\* and sets the flip-flop true at the leading edge of the memory clock C1LR (same time). This releases the clamp on the reset input to D4,13 and causes LOAD\* to go low. LOAD\* strobes the Dual 1-line-to-4-line data selector (F8), causing LOAD1\* LOAD2\* or LOAD3\* to go low depending on which memory module is selected by A and B. This load pulse, assume LOAD1\*, breaks the recirculation path for the memory module and allows the data B1-B7 (B6 not used) to be entered on the trailing edge of C1LR (Memory Input Clock).

Back in the access logic, note that D4,5 also enables NAND gate B3,4. When C2LR pulses (Memory Output Clock) the signal CURCK\* pulses, advancing the cursor one position. At the same time D4,11 is clocked on the trailing edge of C2LR and sets D4,8 false which resets D4,5 low completing the input of one character. As soon as D4,5 returns false it resets D4,8 removing the reset signal on D4,1. When LOAD\* pulsed low the input flip-flop A8,9 returned low blocking the next P1\* from setting D4,5 true again.

### b) Access For CR or FF

For a Carriage Return or Erase function the access is handled somewhat differently. For Carriage Return the signal CR will be true. This causes NOR gate C8,1 to be low enabling AND gate B8,1. When ACS goes true (flip-flop A8,9 goes true upon the ACCESS signal generated by the CR input code) the Q output of flipflop A6,5 goes true. When D4,5 goes true for the first ADDCOM, NAND gate B3,3 goes low clamping D4,5 in the set state. After the first access D4,8 goes low holding the Reset input D4,1 low but since the Preset, pin 4 is also low, output pin 5 of D4 remains high.

If the input code is FF (Erase), the signal CLRG from K8,10 and 13, section G7 is true since CR and CLR\* are both low. This breaks the recirculation path of all three memory modules, and zeros, representing space code, are loaded as long as CLR\* is held low. The flip-flop A8,6 goes false when LOAD3\* returns true after

the third memory module is cleared and then goes true again when LOAD3\* goes low and high a second time which clocks the flip-flop A6,5 back false. The reason for two passes through the memory is to insure the entire screen is erased because the cursor is not returned home by the FF operation before it starts.

If the input code is CR (Carriage Return), CLRG is held low preventing any memory module from erasing any data. The LOAD 1, 2, 3\* signals are inhibited by CLRFF, F8,1 section B3. CLRFF is the inverse of CR. The Preset clamp on D4,4 is released when A6,5 is returned false. The clock input to A6,3 is driven by ADV1, the inverse of ASV1\*, which pulses when the cursor has crossed a line boundary. Since the D input is grounded, the trailing edge of ADV will clock the output back to zero completing the CR function. Keep in mind that the flip-flop A8,6 is true because it was reset with first access and doesn't interfere with the ADV pulse clock.

The signal READY is not used elsewhere in the 580. It is included for possible future use. The READY input to A8,12 is to insure that a second input can not be initiated if the ACCESS logic is busy.

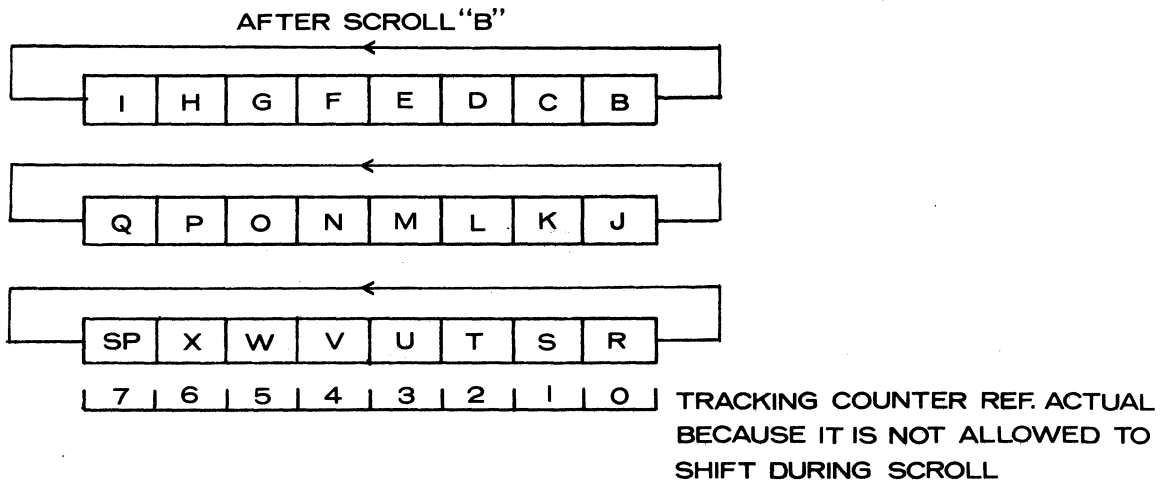
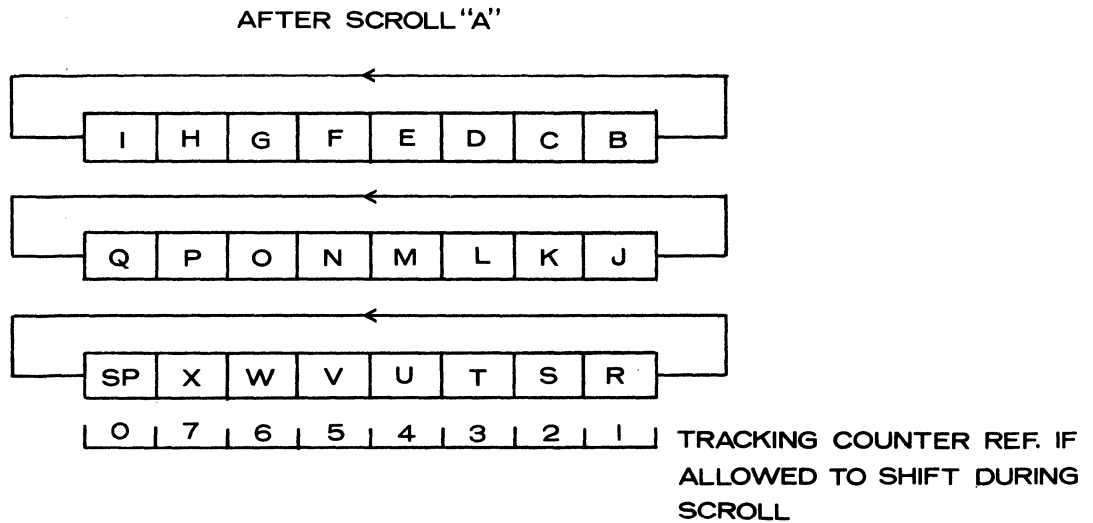
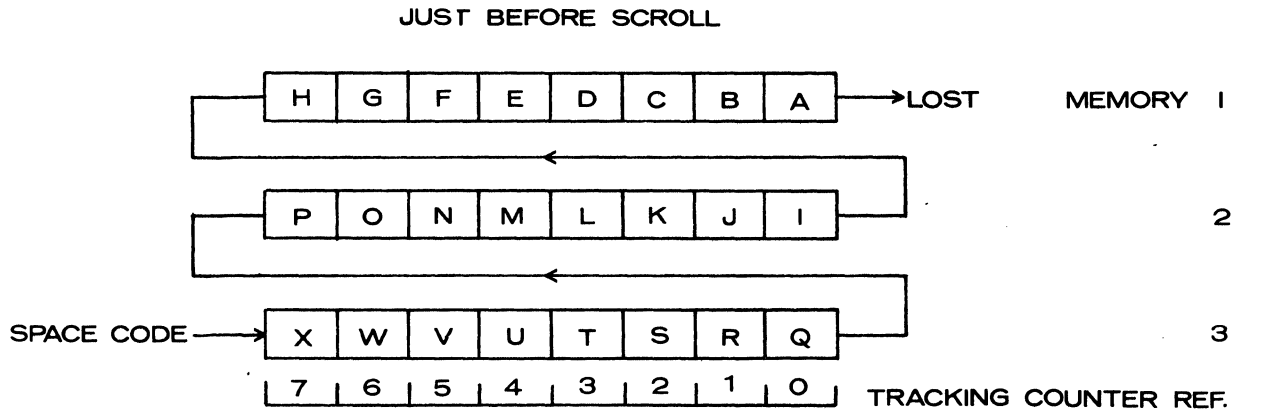
### 3. Scroll Logic

The Scroll circuitry handles two functions, the scrolling of data up the screen and the gating of ADV\* which is the signal from the character portion of the Memory Address register which indicates that the cursor has gone from character position 79 to 0 (crossed the end of a line). If the terminal is in Auto Line Feed, then B3,10 is true which allows ADV1\* to pass on through inverted to the input of NAND gate B4,9. If the terminal is in non-ROLL mode or the cursor is not in the bottom line the other input B4,10 will be enabled allowing ADV1\* to pass as ADV\*. However, if the terminal is not in Auto Line Feed, then ATOLFG is low blocking ADV\* at B3,10. In order for ADV\* to pulse, a Line Feed code or Cursor Down (same code) must be entered, which causes a positive pulse at inverted A2,11 which generates an ADV\* pulse advancing the cursor down one line.

Figure 2-8 illustrates the sequence for scrolling of Memories. At the top, the three memory modules are shown with the output of #3 attached to the input of #2, and the output of #2 attached to the input of #1. The input of #3 is forced to space code while the output of #1 is lost. This occurs when SCROL\* into the dual 4-line-to-1 line multiplexers B7, C7, D7, E7, F7, H7, J7, and K7 goes low. When SCROL\* is low the memories are attached together as one 1920 character shift register.

# RELATIVE MEMORY POSITIONS DURING & AFTER SCROLLING

Fig.2-8



Returning to Figure 2-8, the registers are shifted for 80 counts in the long configuration. After 80 shifts the signal SCROL\* returns true and the memories are returned to the normal configuration as shown in the middle of Figure 2-8. Note that after the scroll, the 80 spaces in memory #3 are in what would be the position of line 0 or the top line of the group of 8 instead of the bottom line where they should be. The same is true of memories #1 and #2. In order to correct this situation, the Tracking Counter must be allowed to go out of sync for the 80 shifts. This is done by not allowing it to count during the time the memories scroll. This reassigns the lines such that the spaces are in line 7. The bottom of Figure 2-8 shows the actual relationship between the data and the Tracking Counter. Note the Tracking Counter hasn't changed from the top reference.

Referring to the schematic, a scroll operation is initiated by ADV1\* pulsing when the cursor is in the last line (LSTNE true), and ROLL is true. ADV\* is blocked and flip-flop A7,5 is set true. This enables the D input of flip-flop A7,12. When ADDCOM is true, P1\* strobes it and clocks flip-flop A7,9 true. This means that the character over the cursor is now at the output of memory #3. When this line (line seven) finishes shifting, the memories are in the position shown in Figure 2-8 at the top. That is, line 0 is ready to shift out. The end of shifting of line 7 is indicated when MCLKDS goes true. Since MCLKDS is inverted, it has no effect on the state of flip-flop A6,9 until it goes negative again indicating the start of the next shift period. At this time A6,9 is inverted by C3,12 to become SCROL\*, which sets up the memories as one shift register when low. A6,8 being low clamps A7,5 and A7,9 low via AND gate A4,6. The signal READY is also held low which blocks any further inputs until the Scroll is completed. The reset input of flip-flop A6,13 is SCRLN (Scroll Enable). This signal is generated on the VG/GT and is always a logical "1." The flip-flop A6,9 resets low, ending the Scroll function when MCLKDS goes negative a second time at the start of another shift period.

#### 4. Cursor Logic

The Cursor circuitry is in section C-2 of the schematic. Below this circuitry is a dual 4-line-to-1 line data selector, D8, with its inputs tied to GND. The two inputs SECT1 and SECT2 indicate which third of memory is being displayed. Pin 7 will be low for memory 1 display pin 6 and 5 low for memory 2 and 3 display. The 74155, F8, has its inputs for the half not used for LOAD\* tied to GND also. The outputs are selected by A and B. E8 is a comparator which has an output, ENABLE, true when A and B equal SECT1 and SECT2. This indicates that the Video Generator is displaying the memory module that is selected by the Memory

Address register which is the third of memory in which the cursor should be displayed. ENABLE enables the D input of flip-flop C1,2. When an ADDCOM (Address Comparison) is true during Scan Line 9 (S8 true) the character under which the cursor should be shown is being loaded into the Refresh. This sets flip-flop C1,5 true indicating that the cursor mark should be generated the next time S8 is true. C1,5 enables the D input C1,12. When S8 goes false C1,9 goes true enabling NAND gate D1,5. The next time S8 is true the second input of NAND gate D1,4 is enabled. Then when CHCOM (Character Comparison) goes true (after the trailing edge of P2\*) B1,2 is enabled. The next P2\* (one character delay later) sets B1,5 true making the cursor mark. Meanwhile, on the trailing edge of P2\*, CHCOM went false allowing the flip-flop to reset on the third P2\*. The cursor mark lasts for 639 nanoseconds or one character time.

#### 5. Reset and Repeat Rate

In the lower left corner of the schematic, a four-stage binary counter is driven by the Video Generator reset signal RST1 (60 HZ). This is divided by 4 to produce the 15HZ signal used for the repeat function on the keyboard. For the blinking cursor option the 4HZ output is used to clamp off the ENABLE signal at E8,3 (if jumper JPl is installed).

When power comes on, the capacitor C10 charges more slowly than the power comes up causing A2,6 to be high and C2,6 to be low for a few milliseconds. This clamps the counter and the flip-flop B1 in the reset state. When C10 charges up, the inverters switch and release the resets. The buffered output of the flip-flop RST is used to cause a power clear of the memories by forcing the access circuitry to the clear function by setting A8,9 and A6,5 true as long as RST remains true. The Front End card also uses RST to condition the UAR/T and all flip-flops to the proper state. B1,9 goes true when the signal 4HZ goes true and returns false (250 milliseconds later) completing the reset function.

#### 6. Miscellaneous

The zeners D1 through D5 (Section C, D, E, F, G H-4) are used to obtain a -5 volt supply by stepping up the -13 volt supply. The -5 volt supplies are required on the N-channel MOS dynamic shift registers, MM5869's.

## DETAILED DESCRIPTION - FRONT END

### Front End Block Diagram Description (Figure 2-9)

#### 1. Serial-to-Parallel Converter

The converter is an MOS device called a UAR/T (Universal Asynchronous Receiver/Transmitter). It accepts parallel data and converts it to 10 or 11 bit serial data. It also accepts 10 or 11 bit serial data and converts it to parallel data. A clock is used to drive the chip and determines at what rate the device will operate. The clock has five switchable rates. The serial input and output is converted from TTL levels to either EIA (+13V) or current loop (20 ma) for operation with standard communication equipment.

#### 2. Decode and Control Logic

Parallel data into the terminal from the UAR/T is checked for validity by the Decode logic. Characters from ASCII columns 2, 3, 4 and 5 are allowed into the memory. Characters from columns 6 and 7 (lower case) with the exception of Rub-out are converted to columns 4 and 5 for input to memory. Control characters from columns 0 and 1 are ignored unless they indicate a terminal control function such as CR, LF cursor controls, etc.

This logic generates the Access strobe and the cursor address control signals.

#### 3. Keyboard Input

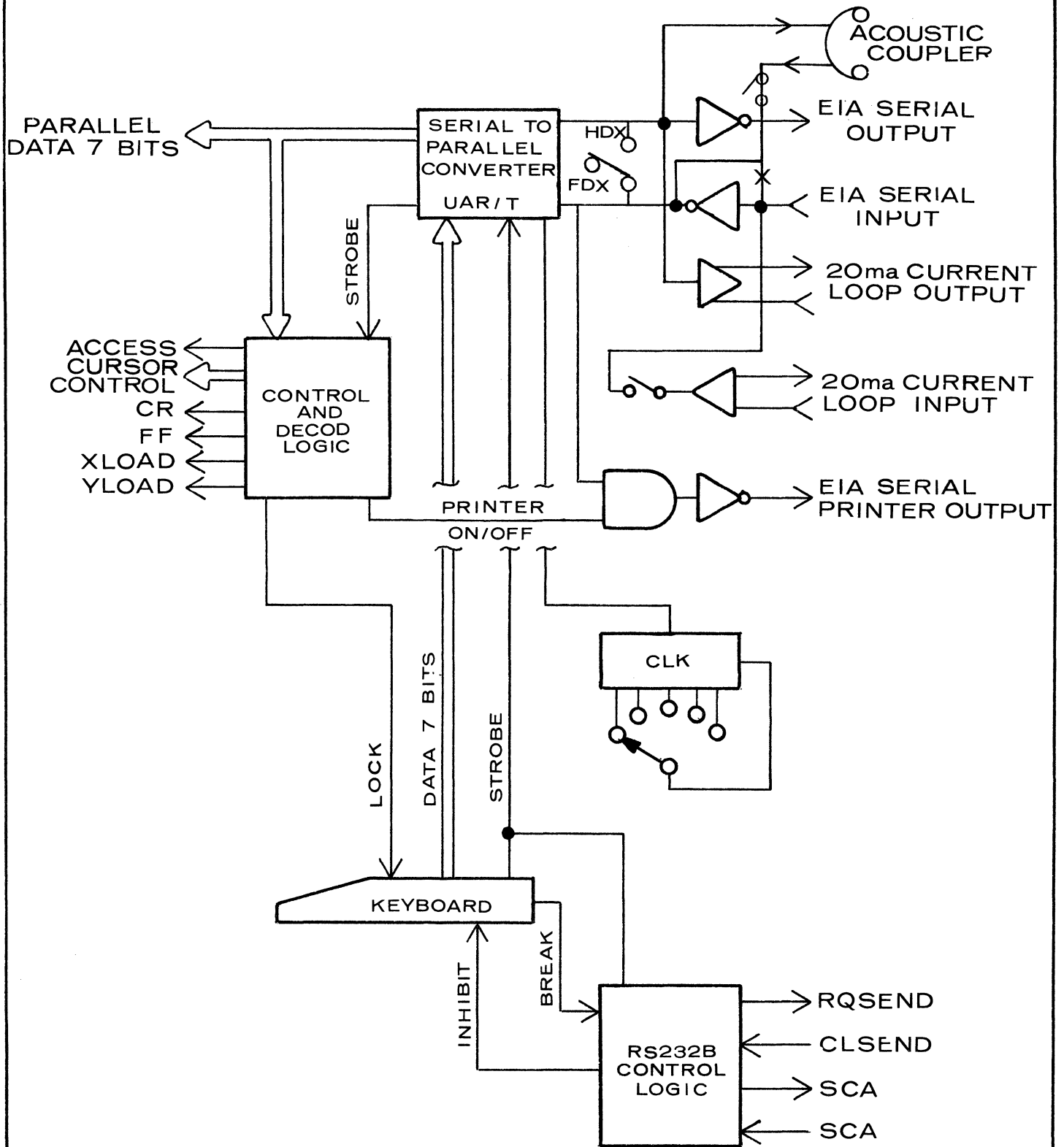
The keyboard supplies the only parallel input to the UAR/T. When a key is depressed, the code along with a strobe is applied to the UAR/T for serialization. When the UAR/T has output the character, another key may be depressed. The only two keys on the keyboard which are not coded are BREAK and REPEAT. BREAK causes a 500 millisecond SPACE on the EIA output and is also used to control the Secondary Channel Request to Send, SCA. REPEAT is used to repetitively output the same code, 15 times per second (10 times per second for 100 baud).

#### 4. RS232C Control Logic

The terminal is capable of operating on any 103-type modem or 202-type modem. For primary channel control, the logic raises Request-to-Send (RQSEND) when the first character of a message is keyed and holds it true until an ETX (End of Text) character is output or a NEW LINE function is performed (CR output in AUTO LF or LF in non-AUTO LF) at which time RQSEND is dropped. The terminal will wait until the modem raises Clear-to-Send before actually outputting the first character.

FRONT END BLOCK DIAGRAM

Fig. 2.9



The Secondary Channel may also be controlled by the terminal. As a switchable option, the keyboard will be locked until the computer allows the terminal to enter the send mode by use of the signals SCA and SCF. If the terminal is in the send mode, the computer may interrupt and force it to the receive mode, locking the keyboard and resetting RQSEND.

#### 5. Printer Output (580/380 only)

There is a serial EIA output port for driving a serial printer. The output is enabled when a Printer-On code is received by the control logic. It is disabled with a Printer-Off code. When on, the printer output copies any serial data that the UAR/T would convert to parallel code. In Half-Duplex, therefore, the printer copies the keyboard data as well as data from the computer. In Full-Duplex, only data from the computer is copied.

#### Circuit Description - Schematic 135-079)

##### Serial to Parallel Conversion

The UAR/T does the conversion from serial to parallel and parallel to serial at TTL levels. The serial data is asynchronous 10 or 11 bit. Normally the data line is at a true or 1 level until a character is sent. The next seven bits are the data bits 1 through 7. The ninth bit is parity and the tenth or both the tenth and eleventh are stop bits, always ones.

The UAR/T is driven by a clock that is 16 times the bit rate. The input is sampled by the clock for the first zero level. If a sample taken 8 clock periods later (center of start bit) is also low, the rest of the bits are detected by center sampling and are stored in a latch. The stop bit (or bits) are checked as well as parity, if set. If all checks good, the UAR/T raises Data Available, DA. If an error were detected, DA is still raised but either Parity Error, PE, or Framing Error, FE, are raised, which results in NOR gate E3,13 being low. The Data out is on pins 6 through 11 of the UAR/T and is buffered for input to the terminal. If an error is detected, E3,13 being low will force an asterisk code on B1 through B7. When DA goes true, AND gate output J8,8 goes true (E6,8 normally true) setting flip-flop E7,9 true. At the same time, E6,12 is enabled so that the next positive edge of SCLK will set E6,8 false, which resets DA. The output data B1-B7 remains stable until just prior to the next DA true level. The edge of SCLK that set E6,8 true also clocked E7,5 true, generating INSTB1 which generates ACCESS. E7,6 going false resets E7,9 so that the next SCLK pulse resets E7,5 low again, completing one input cycle. This same SCLK pulse also sets E6,8 true again because DA has returned false.



In order to output a character the UAR/T must be presented a character in parallel and be given a strobe. When a key is depressed on the keyboard, a 7-bit code is generated and applied to the inputs of the two quad latches A2 and B2. At the same time a strobe is generated called Keyboard Strobe, KBSTB. When KBSTB goes true it sets flip-flop C3,5 true (LOCK\* is normally high and REPEAT is normally low). This enables the D input of flip-flop C3,12 and also strobes the latches to obtain B1L-B7L.

When SCLK goes true C3,9 goes true which, after a delay of 100 nanoseconds (R30, C14), resets C3,5 and removes the strobe from the latches. C3,8 has gone false and returns true on the next SCLK which strobes the UAR/T, causing it to begin the serialization of the character. It is assumed that Clear-to-Send, CLSND, is true. If CLSND is false, DS is delayed until it goes true. The input REPEAT goes true when the Repeat key is held down causing a 15HZ signal at D3,9. If a character key is also held down D3,10 will be enabled and that character will be output at a 15HZ rate. If the character rate is too fast (15HZ at 110 baud for instance) the signal, Transmitter Buffer Empty (TBMT), will be low when the UAR/T is busy which forces C3,5 to be missed. The same will happen if characters are keyed too fast. The signal EOC, End of Character, indicates when the last stop bit for a character has been output.

There are several options concerning the UAR/T which are switch selectable. The Parity may be selected to be even or odd or always 1 or 0. When S6 is closed, the number of data bits is 7, plus one parity bit. The type of parity (odd/even) is selected by S7 which is on for odd and off for even. For no parity, S6 is left off which also selects 8 data bits. The state of the eighth bit is selected by S4 on for a zero, off for a one. The number of stop bits is selected by S5 on for one, off for two.

The clock is a differential comparator operating as a dual ramp integrator. The comparator is A8. The output (bare collector) is pulled up to +13V through 510 $\Omega$ . When on, the output is near zero volts; when off the output is at the reference voltage of Zener diode D4 (5.1V). Assume A8 has switched from zero to +5.1V. This places the positive input pin 2 at +3.3V (note that the positive feedback network is biased at the other side by another Zener diode D3, also 5.1 volts). The output FCOM (Frequency Common) is returned to one of the five inputs FR1-FR5 through the baud rate switch on the rear panel. The capacitor C9 charges towards +5V. When +3.3 volts is reached, the comparator switches low, changing the positive input to +1.65V. Now the capacitor discharges towards ground and again switches high when +1.65 Volts is reached. The inverter A7,2 inverts FCOM to generate SCLK which is the clock used by the UAR/T. The frequency is set by the five Cermet potentiometers R36, R38, R40, R42 and R44. The Baud Rate switch ties FCOM to FR1 for 110 Baud. The other points FR2-FR5, are 300, 1200, 2400 and 9600 baud. The frequencies are 1.76 KHZ, 4.8 KHZ, 19.2 KHZ, 38.4 KHZ and 153.6 KHZ respectively.

## Decode and Control Logic

Input characters are screened by the decode logic to determine whether they are displayable, non-displayable or control functions. Bits four and five (B4 and B5) are decoded into four signals QD0\*, QD1\*, QD2\* and QD3\*. These levels when low indicate in which quadrant of any pair of ASCII columns the character lies. If the character is a control character then CONTROL is true which, when inverted by A7,8, enables the first 8 outputs of the BCD decoder, A5. Its outputs CD0\* through CD7\* each go low for one of the possible combinations of B1, B2 and B3. Thus, a combination of QD0\*-QD3\* and CD0\*CD7\* can select any control character. This is done by use of NOR gates such as B5. For example, B5,1 is the Line Feed code (LF). The ASCII code for LF is 0001010. The first two zeroes are decoded by the NOR Gate D5,4 to enable A5. CD2\* goes low because B3, B2 and B1 equal 010, or 2. QD1\* goes low because bits 5 and 4 are 0 and 1 respectively. Therefore NOR gate inputs B5,2 and B5,3 are both low causing LF to be high. The other control codes used are generated in a similar manner.

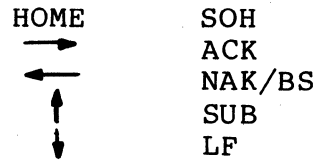
The only exception to the decode method is RUBOUT which is not in columns 0 or 1 and so must be handled differently. In section F-7, the output of NAND gate A3,8 is false when B1, B2 and B3 are true enabling NOR gate K6,2. For a RUBOUT QD3\* is low which causes NOR gate K6,1 to be high enabling A3,3. When B6 and B7 are true then A3,6 is low causing J5,12 to be low blocking ACCESS and INSTB.

For cursor address two codes are used, VT and DLE. VT is used for Vertical positioning and DLE and Horizontal. The two flip-flops (L5) in section E7 and E8 control the addressing. For vertical address VT is true which enables the D input of L5,12 (L5,8 is true allowing AND gate J8,11 to go true with VT). The trailing edge of INSTB\* sets L5,9 true and L5,8 false. L5,8 being false blocks the ACCESS signal by forcing J5,12 low. This also blocks INSTB at E8, 12. The AND gate J4,10 is enabled such that when the next input is made (flip-flop E7,5 pulses true) the signal YLOAD\* pulses low. This in turn loads the least significant five bits of the character following VT into the line portion of the Address Register. The trailing edge of INSTB\* resets L5,9 to false (pin 12 is low because L5,8 block AND gate J8,12) completing the function.

The Horizontal Address is done in the same way when DLE is input to the terminal. L5,5 now sets true generating XLOAD\* causing the character following DLE to be loaded in the character portion of the Address Register.

The signals INSTB and ACCESS are blocked during the X and Y load periods because the address characters may be recognizable control or displayable characters.

The cursors are controlled by 5 codes from the ASCII control columns (0 and 1). These codes are:



These are generated by the decode logic mentioned above. In section G-7 the logic array shown generates the pulses that are used by the Memory and Control board to move the cursor. Note that all five codes are strobed by INSTB to produce a clean signal. The Cursor Forward signal CURFR\* is a combination of the forward code (ACK) and CURCK\*, a signal from the access logic causing a cursor forward when an access to memory is made. The Cursor Up signal, UP\*, is used in a special way. The logic in section H-7 is used to cause the cursor to go home to the bottom left in Roll mode by generating a cursor up after the home code is acted upon. When the code for cursor up is input, UP\* pulses low causing CURUP\* to pulse low via the AND gate H4,5. When a cursor home is done in Roll mode the trailing edge of the pulse HOME sets H5,9 true. The next SCLK pulse sets H5,5 true and H5,6 goes low resetting H5,9 again. H5,5 is combined with ROLL to produce a negative pulse at H5,8 causing CURUP\* to pulse low. This causes the cursor to move from the HOME position (top left) up one line which causes a wraparound to the bottom left. If ROLL is false H4,9 is blocked and the cursor remains in the top left corner.

In the lower left corner of the schematic are two more control functions, Printer Enable and Keyboard Lockout. The signal RST\* resets both J-K flip-flops (C7) upon power up. The Keyboard Lock flip-flop C7,13 (LOCK\*) is optionally reset by the BREAK\* signal or disabled by jumping J8,4 to ground. When enabled, the code EOT causes LOCK\* to go false, blocking the Keyboard Strobe KBSTB at C3,1. STX sets LOCK\* back true allowing the keyboard to operate again. When JP4 is inserted, the Break key may be used to unlock a locked keyboard. The other half of C7 controls the EIA Printer output. DC2 causes C7,9 to be high which enables AND gate D2,13 in section B-3. Any characters following will be output by the EIA driver F4,6. Note the input to D2,12 is the same as the serial input (inverted) to the UAR/T which means that the printer will copy whatever goes to the CRT screen in Full or Half-duplex.

#### RS232C Interface

The voltage range for the EIA standard RS232C interface is +3V to +15V for a Data zero level and -3V to -15V for a Data 1 level. Control signals such as Request-to-Send and Clear-to-Send have the same voltage swing but positive is true and negative is false.

Integrated circuits are available to translate these levels to TTL levels. The driver is a 1488 and the receiver is a 1489.

The EIA output signal, EIAOUT, is generated by F4,11 (1488). The UAR/T output is "AND" with BREAK\* via D3,6 to drive F4,12 and 13. BREAK\* goes false for about 1/2 second when the Break key is depressed, causing a positive level (space) on the EIA output. The output of the UAR/T is normally high and goes low for space bits causing positive levels on EIAOUT. Another section of F4 (pins 4 and 6) is used for the serial EIA printer output described before.

The receiver F5 (pins 4 and 6) is a section of a 1489 and has a TTL level output. EIAIN is converted to TTL and applied to NAND gate B3,5 for input "or-ing" to the UAR/T. If the signal HDX (Half Duplex) is false B3,9 is blocked and output data D3,6 is not gated into the UAR/T. If HDX is true then serial TTL output data is mixed with the input data to provide a local echo path. Either data from the CPU or the keyboard will be input to memory. Switch S1 connecting the output of NAND gate B3,3 to the input of B3,4 blocks the input when Request-to-Send is high in Half-Duplex mode to suppress any echo from the external device (202C modem, for instance).

The Request-to-Send circuitry is just above. When a key is struck, the RQOUT\* goes low (C3,6 in section C-5) which sets E6,5 true and RQSND\* false which via F4 drives RQSND true. The modem raises CLSND which when converted by F5,3 (Section C-5) allows the character to be output. RQSND remains true until an ETX, CR (AUTO LF) or LF (non-AUTO LF) is output. The flip-flop (section D-1) is set when E8,4 is true and EOC (End of Character) returns true. E8,4 is true for three conditions. Assuming JP1 and JP2 are installed, one condition is the output of ETX which when true drives H6,8 false and E8,4 true via D7. When F7,6 goes true (pin 2 grounded, F7 was preset by E6,5 being low before the process began) the signal SCLK/16 (SCLK divided by 16) clocks the flip-flop F7,8 false and then true which clocks E6,5 back low completing a Request-to-Send sequence. If the terminal is in AUTO LF then the CR code enables E8,4. In non-AUTO LF the LF code enables E8,4.

The NOR gate E3, 1, 2 and 3 is used to generate ATOLFG used by the Memory and Control for Erasing in non-AUTO LF mode. This is done by forcing AUTO LF true when CLRFF goes true during an Erase function.

#### Reverse Channel Control

The Reverse Channel (202C) control circuitry is in section F-3. If the reverse channel is to be used for circuit assurance and interrupt, Switch S3 should be closed. Upon power up or after a transmission, flip-flop C8,9 will be true forcing TRANS low

blocking any keyboard input by clamping flip-flop C3,5 reset (Section C-5). At the same time since BREAK is false and C8,8 is false, SCA is true. SCA is the signal that causes a 202C modem to turn on the reverse channel carrier. The CPU monitors SCA for a negative condition and holds SCF normally false. SCF is the received signal detector for the reverse channel. When the user presses the Break key the signal BREAK goes true for approximately 500 milliseconds driving SCA false. The CPU detects the negative level on the reverse channel and responds by raising and dropping carrier or just dropping carrier if already raised. The trailing edge of BREAK sets flip-flop C8,5 true, conditioning the clock input of C8,11 to follow the Carrier Detect signal CARDT1. When the carrier goes false flip-flop C8,9 goes false which enables NOR gate K6,5. When SCF goes true (CPU raises SCA at its end which is SCF at the terminal) K6,6 goes false causing TRANS to go true enabling the keyboard strobe. (Note that the BREAK signal when going true causes a negative pulse of approximately 100 nanoseconds at J5,5 presetting C8,9 true. This allows the transmit mode to be aborted with a Break.) When the transmission is complete, Request-to-Send returns false causing RQSND\* to go true which places a 100 nanosecond negative pulse at J5,4 which presets C8,9 forcing TRANS back false. (H8 is a 74121 one-shot. The time constant is determined by R12 and C10, C11).

### Current Loop

The Current Loop portion is in the lower right hand section. L7 and K8 are opto-isolators (MOC1000). L7 and K8 are opto-isolators (MOC1000). The input stage is K8. When current is present K8,4 and 5 preset a low impedance to -13V. Q5 is turned on holding the EIA input to approximately -11V (S2 is closed for current loop operation). When the loop opens (space) K8,4 and 5 present a high impedance and Q5 turns off allowing the EIA input to go to +13V. The diodes D11 and D10 are used to keep Q5 from saturating insuring that the output stage of K8 is not in an overdrive condition which would reduce the speed because of excess minority carrier storage.

The output stage also uses a opto-isolator (L7). When in the mark condition Q3 is on (because D3,6 is high) which turns on the output stage of L7. Q4 is also on supplying a low impedance to the loop. The diodes D5 and D6 are used to keep Q4 from saturating for the same reason as the input stage. The other two diodes D7 and D8 are to insure some bias voltage for the base of Q4. When a space condition occurs, Q3 turns off (D3,6 low) which in turn causes Q4 to turn off, opening the loop.

The diodes across the input and output, D12 and D9, are to protect the circuits from reverse voltage.

## Miscellaneous

The carrier light is driven by the discrete circuit in section H-4. Normally D2 is not installed. When the Carrier Detect signal goes true (Section E-4) CARDT1 goes true which turns on Q1. Q1 turning on also turns on Q2 and supplies +13V through 300 to the lamp. The other side of the lamp is referenced to -13V.

Units are equipped with alarm circuitry (Section E5 and 6) which activates a "Sonalert" alarm upon receipt of a BEL code producing an audible tone for approximately 1/2 second. The BEL code is decoded by E3,4 from QDO\* and CD7\*. L3 is a one-shot that pulses for a period determined by R50, C15 and C16, starting on the leading edge of INSTB if L3,3 is true. Q6 amplifies the pulse from L3,6 to drive the "Sonalert."

The two signals DATTRY (Data Terminal Ready) and LBIAS (Loop Bias) go to the output connector. DATTRY is needed by a modem when EIA levels are used. DATTRY and LBIAS may be used in a current loop connection to supply the current.

The straight through connections shown in Section D-6 carry I/O signals to the back plane for use by other cards.

## SECTION 3:

## GLOSSARY OF SIGNAL NAMES

SIGNAL NAME	DESCRIPTION	SOURCE
A,B	Select Address for memory module; 2-stage counter tracks memory module for desired address (i.e., cursor position)	C3,VG
ACCESS	Gated INSTB1; inhibited by address advance, all control except FF and CR	D7,FE
ADDCOM	Address Comparison; CHCOM and line counter comparison	B4,VG
ALARM*	Pulses terminal bell equivalent	E5,FE
ADV*	Advances line address counter	B2,MC
ADV1*	Cursor crossed line boundary	C6,VG
ATOFLG	Allows memory and control to erase in non-AUTO LF mode	E3,FE
BREAK	500 ms. pulse derived from BREKEY	F4,FE
BREKEY	Break Key	Keyboard
BX(X=1-7)	Gated out bus of UAR/T; output of UAR/T	D3,FE
BXL(X=1-6)	Output of refresh memories	F1,MC
C1LR,C2LR	P1* and P2* gated with MCLKDS	A5,MC
C1RR,C2RR	Buffered P1* and P2* for driving refresh memories	D1,MC
CARLT	Carrier Light; activates CARRIER light on terminal	G3,FE
CHCOM	Character Comparison	C6,VG
CLK	Main signal clock; 12,528 MHZ	H6,VG

SIGNAL NAME	DESCRIPTION	SOURCE
CLR1,2,3	Load space code (all zeroes) into display memory	H7,MC
CLRG	Load space code (all zeroes) into display memory; used on units after January 15, 1973.	H7,MC
CLSND	Clear to Send; allows terminal to input characters	Modem
CMBSN*	Combined Sync; includes VDRIVE and gated HDRIVE (8 character times after HDRIVE)	F3,VG
COMENB	Comparison Enable; inhibits CHCOM during memory pause and synchronization	E2,VG
CR	Carriage Return; decode from keyboard	G5,FE
CURBK*	Cursor Back; back code (NAK) gated with INSTB	G7,FE
CURCK*	Cursor Clock; advances cursor one position	F6,MC
CURDWN	Cursor Down; down code (LF) gated with INSTB	F7,FE
CURFR*	Cursor Forward; equals CURCK or forward code (ACK)	G7,FE
CURUP*	Cursor Up; equals up code (SUB) or after HOME (Roll Mode) a pulse to position cursor in the bottom left	H6,FE
D4*	One character time (639 nsec)	H5,VG
DA	Data Available; output of UAR/T	D4,FE
DATAGT	Data Gate; 80 character time signal, gates data, set at count 15, reset at 95, starts one character before data is displayed on screen	G4,VG
DS*	Data Strobe for UAR/T; parallel data available to UAR/T	C4,FE



SIGNAL NAME	DESCRIPTION	SOURCE
EIAIN	Input from modem	Modem
EIAOUT	Output to modem	C2,FE
ENABLE	A,B equals SECT1,2	B2,MC
EOC	End of Character; from UAR/T, last stop bit outputted	C4,FE
FCOM	Frequency Common; to common of baud switch	B5,FE
FE	Framing Error from UAR/T	C3,FE
FF	Form Feed; decode from keyboard, same as screen erase	H5,FE
FR1,2,3,4,5	Inputs from baud switch	Baud switch
HBLANK	Horizontal Blank; set at character count 97, reset at 15	G2,VG
HDRIVE	Horizontal Drive; used by internal monitor; set at HBLANK, reset at character count 31	F1,VG
HOME	Home code during INSTB	G7,FE
INSTB1	In strobe; function of selected baud rate	E5,FE
KBSTB	Keyboard Strobe; data available from keyboard	Keyboard
KXKB(X=1-7)	Keyboard Data	Keyboard
LOAD*	Strobe for input to display memories	F6,MC
LOCK*	Keyboard locked signal; from EOT to STX	B7,FE
LRCLK	Advances memory tracking registers; equals C2LR, gated off during scrolling	E6,MC
LSTLNE	Last Line	D5,VG
MCLKDS	Memory Clock Disable; equals COMENB*, allows for sync during video vertical flyback	D2,VG

SIGNAL NAME	DESCRIPTION	SOURCE
MEOL*	Memory End of Line; display memories have shifted 80 counts	B6, VG
P1, P2	Buffered inversion of P1* and P2* for driving display memories; gated with MCLKDS	B4, MC
P1*, P2*	Two-phase clocks for one character position	G5, VG
PE	Parity Error from UAR/T	C3, FE
RDA*	Reset DA in UAR/T	D5, FE
READY	Access logic not busy	E7, .MC
REPEAT	Output of keyboard Repeat key	Keyboard
RQSND	Request-to-Send; signal to modem indicating terminal ready	D2, FE
RST	Power on reset; occurs once per power up sequence	C6, MC
RST1	Half character pulse at line count=29; resets line counter	G2, VG
S8	Ninth scan line	H3, VG
SCA	Secondary Request-to-Send; normally true, low during BREAK, acts as interrupt to modem	E2, FE
SCF	Secondary Received Line Signal Detector; terminal uses to determine permission to transmit	202C Modem
SCLK	16 times UAR/T bit rate; function of selected baud rate	D5, FE
SCRLEN	Scroll Enable; equals DATAGT and sync FF (set RST1, reset end of VBLNK)	D2, VG
SCROL*	Forces display memories to scroll	E6, MC

SIGNAL NAME	DESCRIPTION	SOURCE
SECT1,2	Select Memory Module; 2-stage counter, clocked at data line 11 and SL1, and data line 19 and SL1 (60 HZ)	E4, VG
SFCLK	Static memory clock; pulse stretched CILR	G5, MC
TBMT	Transmit Buffer Empty; from UAR/T, necessary before sending DS	C4, FE
VBLNK	Vertical Blank; set SL1 and data line 28, reset SL9 and data line 3 (60 HZ)	F1, VG
VDRIVE	Vertical Drive; set RST1, reset data line 1, used by internal monitor	E1, VG
XLOAD*	Similar to YLOAD; loads into character portion, provides for cursor character advance	E7, FE
YLOAD*	Loads least significant 5 bits of character following VT into line portion of ad- dress register; provides for cursor line advance.	E7, FE

## SECTION 4:

### UNIT TEST PROCEDURE

The off-line test procedure described in this section provides assurance that the terminal is operating properly. It is assumed before the steps below are followed that no cables are plugged into the Data Connector on the rear panel of the 580 and that the unit is set up for EIA operation (Switch #2 on the FE/GT card placed to the OFF position).

1. Place the POWER switch ON; the red indicator should light and the screen should show a clear white rectangular "display page" after approximately a 30-second warmup, with the cursor at the top left corner of the page.

[If the red indicator does not light, check the line cord. If the cord is properly connected and you have ascertained that the wall receptacle contains power, the fuse on the rear panel should be checked. The fuse is type 3AG, 1.5 Ampere, SLO-BLO.]

2. Place the ROLL and AUTO LF switches in the depressed state. Place the FULL DUP switch in the non-depressed state.

- a. Key [ABDHP (SP)], where (SP) = space

At this point you may wish to readjust the TV picture by using the BRITE and CONT controls on the rear panel. For proper adjustment, first back off both controls fully so that no picture is visible. Bring Brightness up until a raster is visible, then carefully back off Brightness to the point that the raster lines are just not visible. Finally, bring up Contrast to the desired level for a clear picture.

- b. Key [KcK], where Kc = CONTROL-K

The cursor should move vertically down to about the center line.

- c. Key [ABDHP (SP)]

- d. Key [KcW]

The cursor should move vertically down to the bottom line.

- e. Key [ABDHP (SP)]

- f. Key [NEW LINE]

The cursor should go to the bottom left corner and all data should scroll up one line.

- g. Key [PcYs], where Ys = SHIFT-Y

The cursor should go to the bottom right corner.

- h. Key [LF] until the bottom ABDHP is in the top line. A flash of ABDHP elsewhere is normal during a scrolling operation.

- i. Key [PcPcs], where Pcs = CONTROL-SHIFT-P

The cursor should return to the left margin.

3. Place the ROLL switch in the UP position. Key [NEW LINE]. The cursor should go to the top left corner.
4. Place AUTO LF in the UP position. Key in a few characters and then depress CONTROL and SCREEN ERASE. The screen should erase.
5. Depress the FULL DUP switch.
  - a. Key characters; none should go on the screen.
  - b. Return to Half-Duplex (FULL DUP up).
6. Check that all keys on the keyboard work (except PRINT ON and PRINT OFF, unless a serial printer is attached to the Printer port). Note that SCREEN ERASE works only when the CONTROL key is held down.
7. Place the unit in ROLL mode. Check that HOME is bottom left.
8. Place the unit in non-ROLL mode.
  - a. Check that HOME is top left.
  - b. Using the REPEAT key, enter a line of characters and note that the cursor advances to the next line when the current line is completely filled, for units delivered after January 15, 1974. For units delivered prior to that date, the cursor goes back to the beginning of the same line.
9. Return to ROLL mode. Move the cursor down with [↓] and check that the screen scrolls only when the cursor is in the bottom line.
10. Depress the CONTROL-G combination on the keyboard and note that the audible alarm sounds. [NOTE: The alarm is available only on units delivered after January 15, 1974.]
11. To check the printer output, wire a serial EIA printer to the Printer output connector.

- a. Key in characters. They should not go to the printer.
- b. Key [PRINT ON].

All characters keyed should now go to the printer as well.

- c. Key [PRINT OFF].

Characters should no longer go to the printer.

#### NOTE

In place of a printer, an oscilloscope may be used to observe that the output level at the Printer connector (-13V) pulses to +13V when characters are keyed during the Printer On portion of the test procedure.

If all of the above are operative, you are ready to start on-line operation.

Two further tests may also be performed if one wishes to test the EIA driver/receiver circuits and the opto-isolator used for current loop operation.

12. To check the EIA driver/receiver, connect a wire from Pin 2 to Pin 3 of the 25-pin data connector and check that data is keyed to the screen when in Full-Duplex.
13. In order to check current loop, the shroud must be removed, and switch #2 on the FE/GT card placed ON.
  - a. At the data connector, connect a wire from Pin 22 to 24, connect 25 to 17, and connect 18 to 7.
  - b. Key data in Full-Duplex and check that data goes to the screen properly.

#### NOTE

If you wish to operate off-line without jumpers (or EIA), switch #2 on the FE/GT card must be set back to OFF.

## PHYSICAL ACCESS FOR TEST AND REPAIR

## CONTROLS, INDICATORS AND CONNECTORS

A detailed description of the function of all controls and indicators, and of interface connections is given in ADDS publication #511-32900A, Users Manual for the 500 Series Terminals. These components are summarized here.

Controls and Indicators on the Front of the Consul 580

An ON-OFF power switch

A POWER indicator lamp (red). This is in series with a fuse in the primary of the power supply transformer.

A CARRIER indicator lamp (white). This lamp indicates that the signal "Carrier Detect" is high.

Three Mode Select pushbuttons. These switches permit selection of FULL DUP, AUTO LF, or ROLL mode.

Rear Panel (Figure 5-1)

Data connector. This is a 25-pin female Cinch or Cannon type DB 25-S. A mating connector (Cinch or Cannon type DB-25 P) is supplied with terminals.

BNC Video Output connector. This is used to connect 75-ohm coaxial cable (RG 59/U or equivalent) for driving slaved external monitors.

PRINTER 4-pin plug. Used to connect a serial printer.

A 3.0 Ampere "SLO-BLO" Fuse.

A 3-pin power cord connector. The "device" end of the removable Consul power cord plugs into this connector.

## WARNING

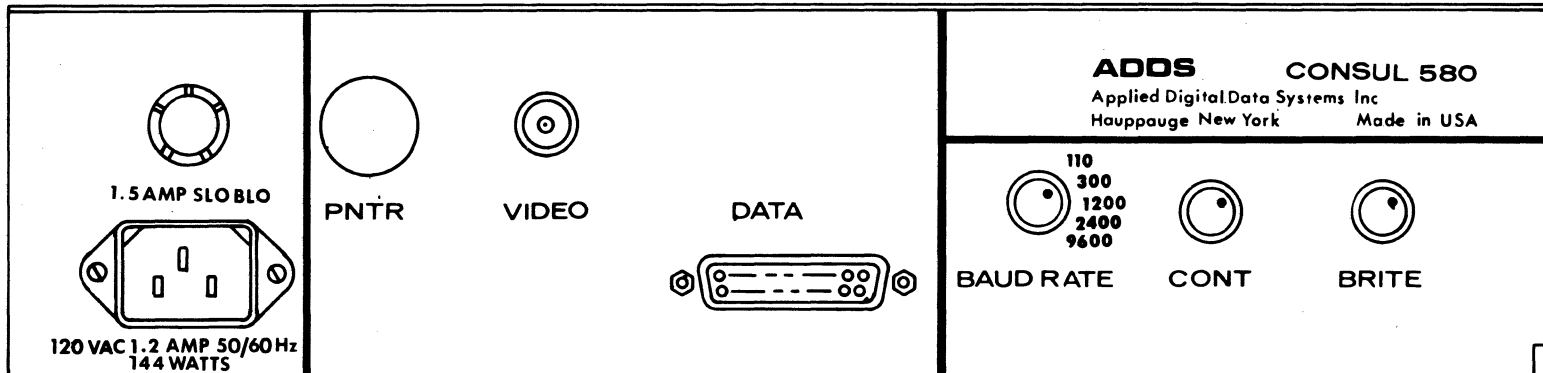
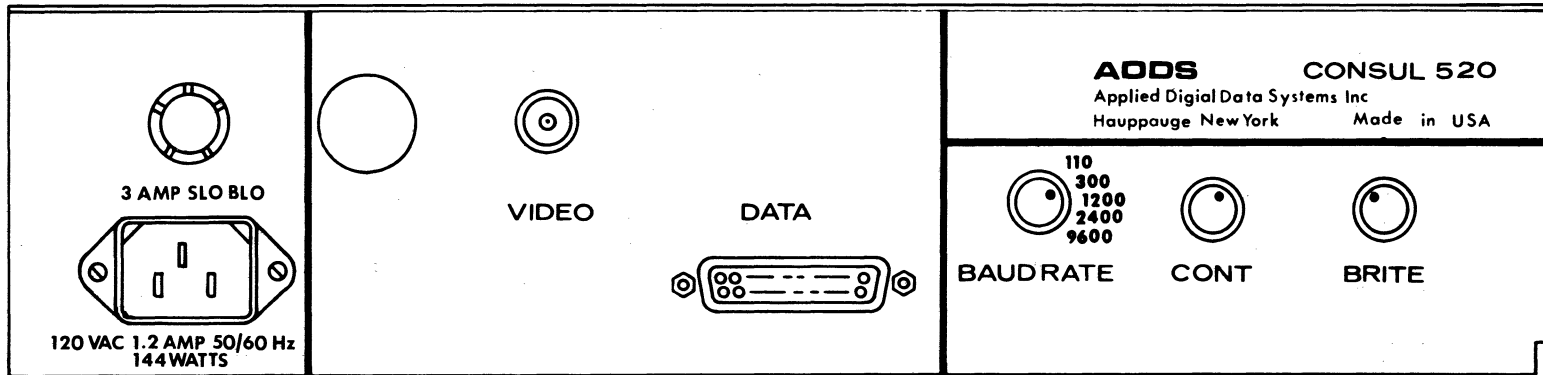
Do not plug 115 volt terminals into a 230 volt outlet.

Consuls may be supplied to operate 230V/50Hz.

A 5-position BAUD RATE switch. This switch is used to select the desired serial baud rate. Speeds of 110, 300, 1200, 2400, and 9600 baud are standard on the Consul. Other baud rates are available on special order.

BRITE control knob. Sets TV screen brightness.

**CONSUL 520/580 REAR PANEL**  
**Fig. 5-1**



**NOTE:**  
 Units set up for 240 Volt operation will have a 1.5 Amp fuse and .6 Amp Power and be marked accordingly.



CONT control knob. Sets TV screen contrast.

#### ACCESS TO PC CARDS AND SUBASSEMBLIES

The top shroud of the Consul is removed to service the PC cards and subassemblies. To take the shroud off, remove four Phillips head screws as shown in Figure 5-2. Then grasp the sides of the shroud and lift up.

Figure 5-3 shows the unit with its shroud removed. The item numbers in Figure 5-3 are referenced in the following paragraphs.

The majority of service problems involve only removal and replacement of PC cards. The layout of PC cards within the card cage (#1) is shown in Figure 5-4. The hold down cover (#2) can be removed by loosening one screw on the front of the cover then lifting it up and to the front. The PC cards can be removed by grasping the end firmly and working the card up and down while exerting a pulling force. For those personnel who must remove cards frequently a "card puller" is recommended. (ADDS service personnel use the "Wire-Grip" puller, part #1733, made by E.H. Titchener and Co., 1 Titchener Place, Binghamton, New York.)

When cards are inserted they should be pushed in until the card shoulder firmly seats against the backplane connector. Cards will not come loose in normal shipment and use since they are firmly seated with long fingers and held in place. However, if the performance of the device is erratic after shipment (or very rough handling is suspected) the cards should be inspected to insure that all are firmly seated.

When the terminal is "unbuttoned" as in Figure 5-3, power may be applied and the device operated if one wishes to check signals in the cabling, the PC card backplane, connector terminations, etc.

If circuitry is to be checked with an oscilloscope as the terminal is operated, an ADDS extender board should be plugged into a card slot and the card plugged into the end of the extender card. The ADDS extender card has a center ground plane to prevent signal pickup and interference between signals on the two sides of the extender. The extender card is almost a necessity if one wishes to diagnose faults to the chip level, rather than the card level. The alternative for chip-level repair is to sequentially replace the suspect chips on a card, if fault isolation is performed only to a card level.

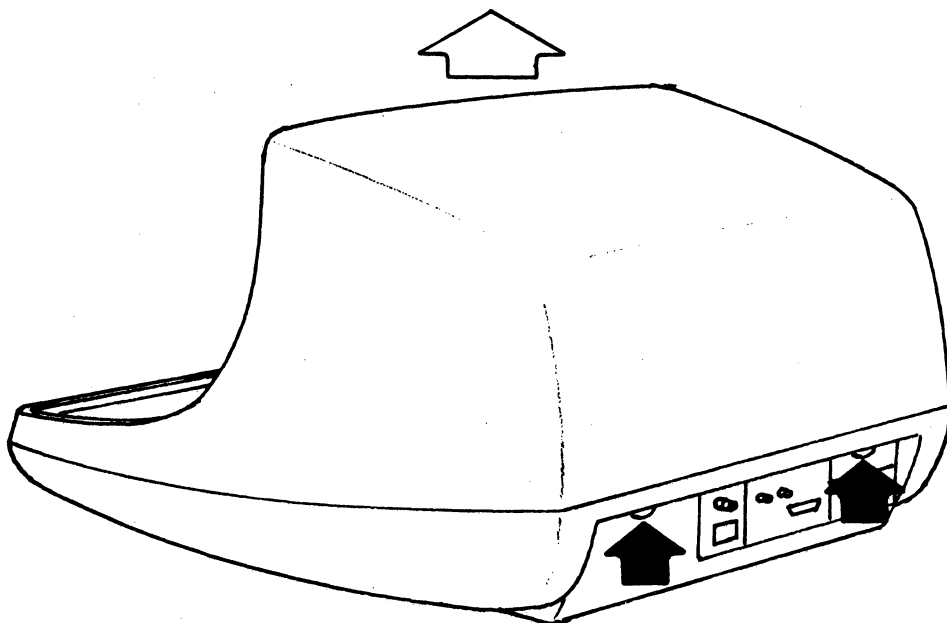
#### CRT Monitor

To remove, undo four mounting screws, then disconnect the 14-pin dip connector on the back edge of the monitor P.C. card, (upper PCB), using the small plastic strap on the connector to extract it. Next, remove the ten-position and six-position Molex type connectors on the power supply P.C. board (lower board) and

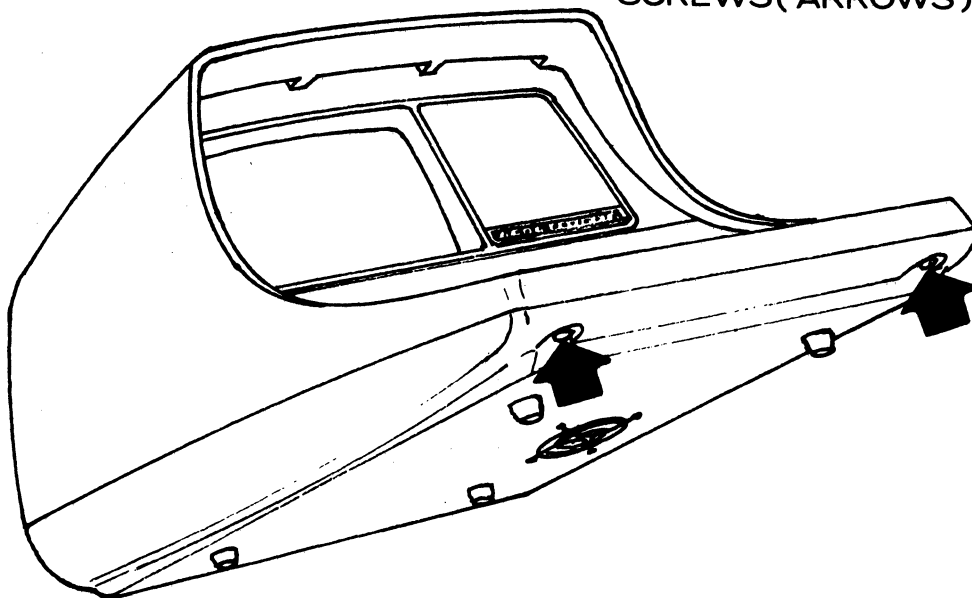
SHROUD REMOVAL

Fig. 5-2

GRASP SIDES OF SHROUD AND LIFT UP

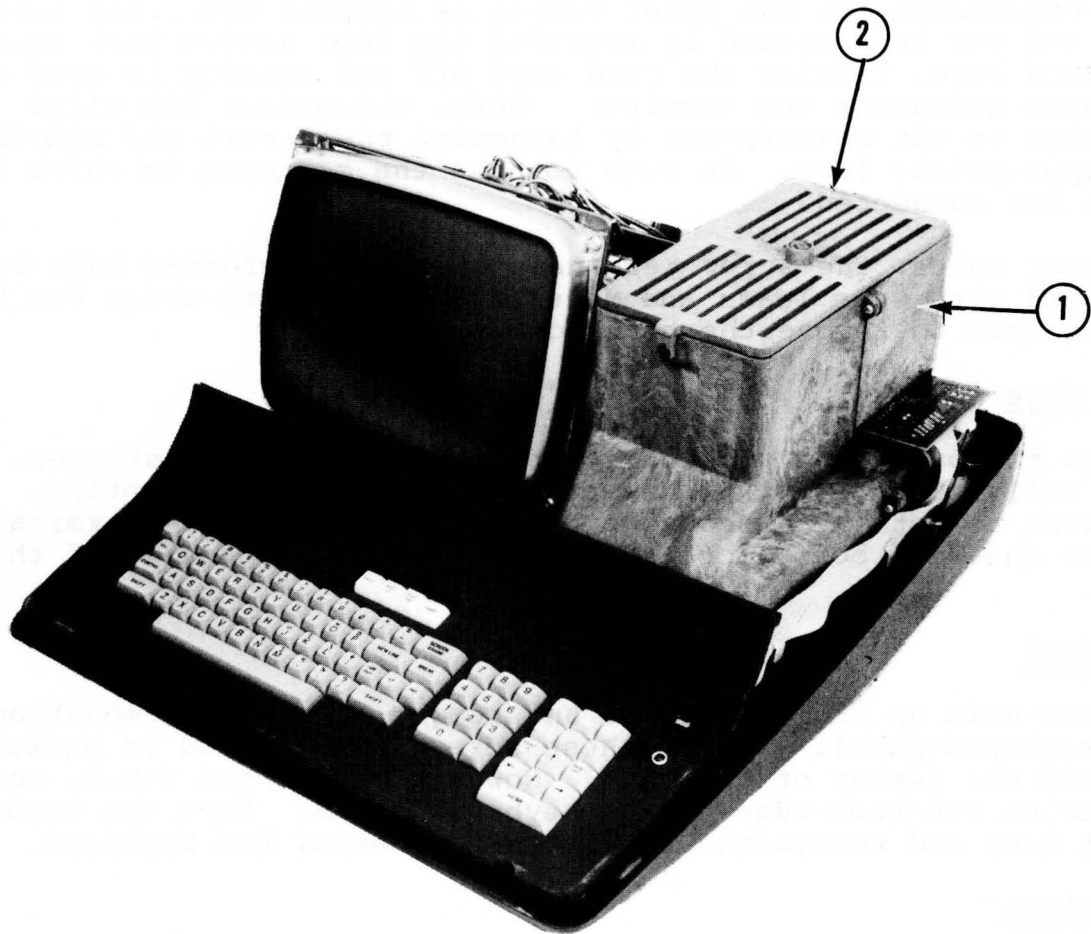


REMOVE 4 PHILLIPS HEAD  
SCREWS (ARROWS)



**CONSUL 580 — WITH COVER REMOVED**

**Fig. 5-3**



disconnect the two-position Molex type connector labeled Sonalert on the rear panel P.C.B. Then loosen the #6 Phillips head screw and disconnect the green ground wire. The monitor with the power supply attached may now be lifted out.

### Power Supply

To remove, first disconnect the three Molex type connectors on the P.C. card. Next remove the two screws located on either side of the heatsink cover, remove the three Molex type connectors and then snap the P.C. board off the two plastic standoffs. The supply may now be removed by sliding it back and rotating it as you lift it out. Care should be taken not to damage the monitor tube when removing the supply.

The transformer for the power supply is located under the card cage and can be accessed by removing the four screws that mount the card cage, lifting the card cage off and setting it down upsid-down alongside the terminal. Next, disconnect the wires attached to the transformer by loosening the screws and removing the appropriate lugs. Be sure to note the sequence in which the wires are connected.

On newer units, the screw terminals on the transformer have been replaced with wire leads and Molex type connectors which can be disconnected to remove the transformer.

### Card Cage

Follow the preceding procedure for accessing the transformer. This will make the backplane accessible for troubleshooting. If you wish to totally disconnect the card cage from the terminal, remove the P.C. board located in the window on the side of the unit.

### Keyboard

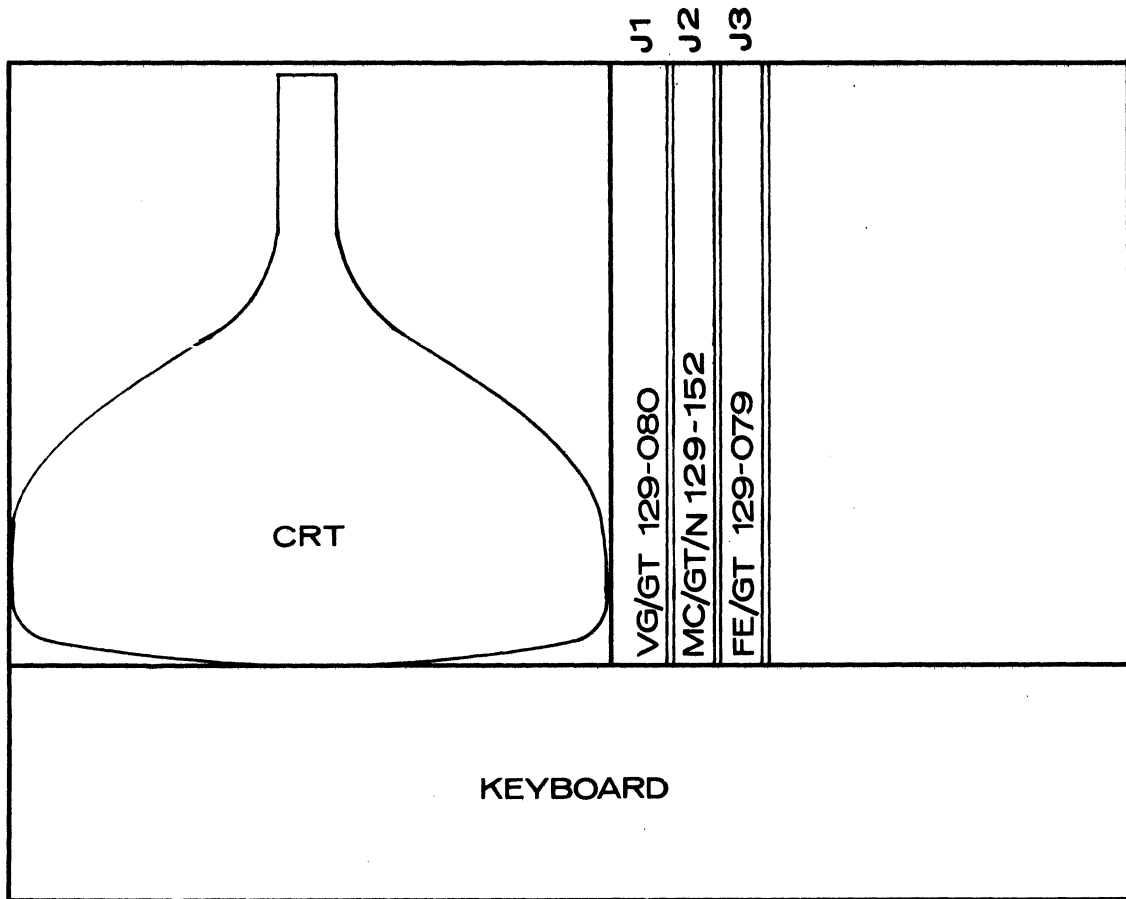
Tip the unit up from the front and remove four screws mounting the keyboard panel. Two of these screws are located in pockets towards the center of the unit. Now disconnect the P.C.B. connector on the back edge of the keyboard P.C.B. Turn the keyboard panel over and remove the four screws mounting the keyboard.

### Backplane

To remove, follow the procedure for removal of the card cage. Once the cage is out you can remove the four screws mounting the backplane, two at the front and two at the rear of card cage. Loosen the P.C. board edge connectors and lift the backplane out of the card cage.

CONSUL 520/580 P. C. CARD LOCATIONS

Figure 5-4



—TOP VIEW—

## CONTROLS, INDICATORS AND CONNECTORS FOR THE MRD-380

### Controls and indicators on the front of the MRD-380 are:

An ON-OFF toggle power switch.

A POWER indicator lamp. (Red) This is in series with a fuse in the primary of the power supply transformer.

A CARRIER indicator lamp. (Yellow) This lamp indicates that the signal "Carrier Detect" is high.

### Located on the rear panel (Figure 5-5) are

Data connector. This is a 25-pin female Cinch or Cannon type DB 25-S. A mating connector (Cinch or Cannon type DB-25 P) is supplied with terminals.

BNC Video Output connector. This is used to connect 75-ohm coaxial cable (RG 59/U or equivalent) for driving external monitors.

Three Mode Select toggle switches. These switches permit selection of FULL DUP, AUTO LF, or ROLL mode.

PRINTER 4-pin plug. Used to connect a serial printer.

A 1.5 Ampere "SLO-BLO" fuse.

A 3-pin power cord connector. The "device" end of the removable Consul power cord plugs into this connector.

#### WARNING

Do not plug 115 volt terminals into a 230 volt outlet.

Consuls may be supplied to operate on 230V/50HZ.

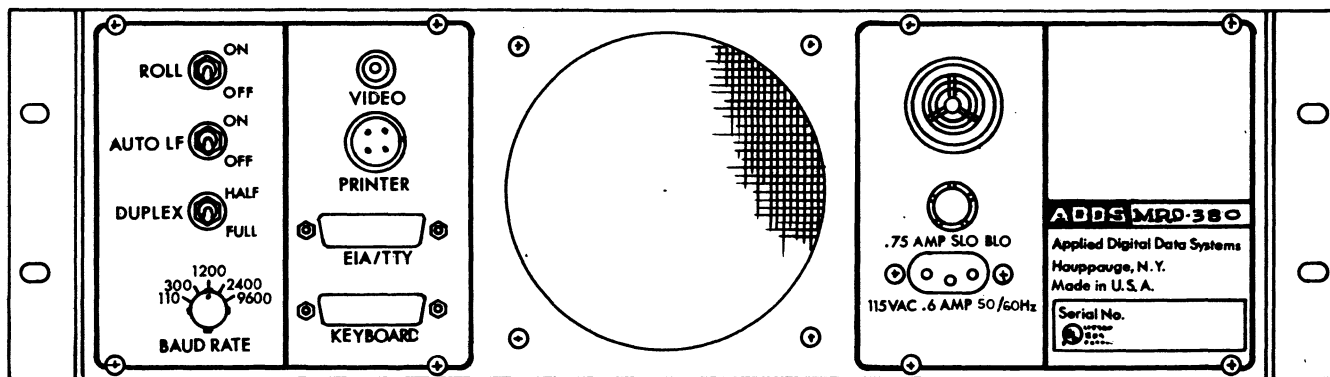
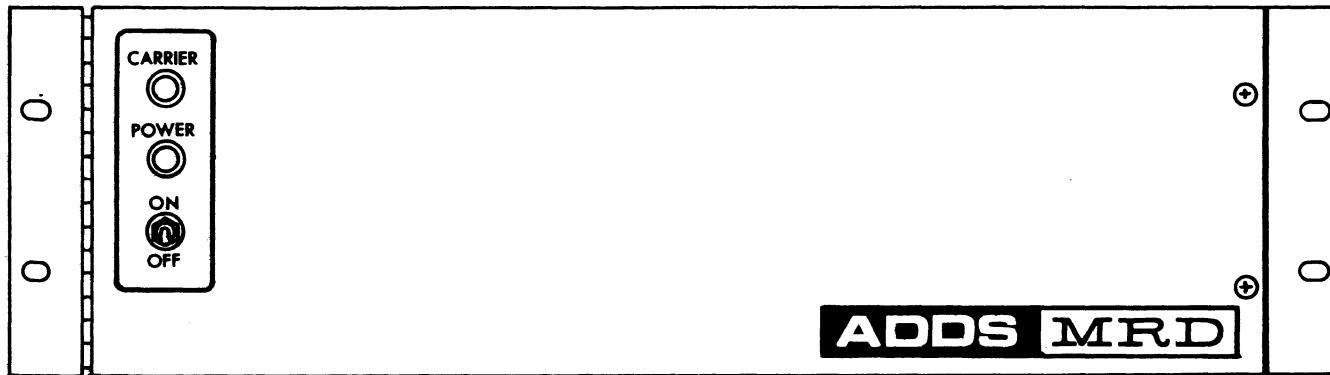
A 5-position BAUD RATE switch. This switch is used to select the desired serial baud rate. Speeds of 110, 300, 1200, 2400, and 9600 baud are standard on the Consul. Other baud rates are available on special order.

### ACCESS TO PC CARDS AND SUBASSEMBLIES

The front door of the MRD is opened to service the PC cards and subassemblies. The majority of service problems involve only removal and replacement of PC cards. The layout of PC cards within the card cage is shown in Figure 5-6. Cards may be removed by grasping the end firmly and working the card up and down while exerting a pulling force. For those personnel who

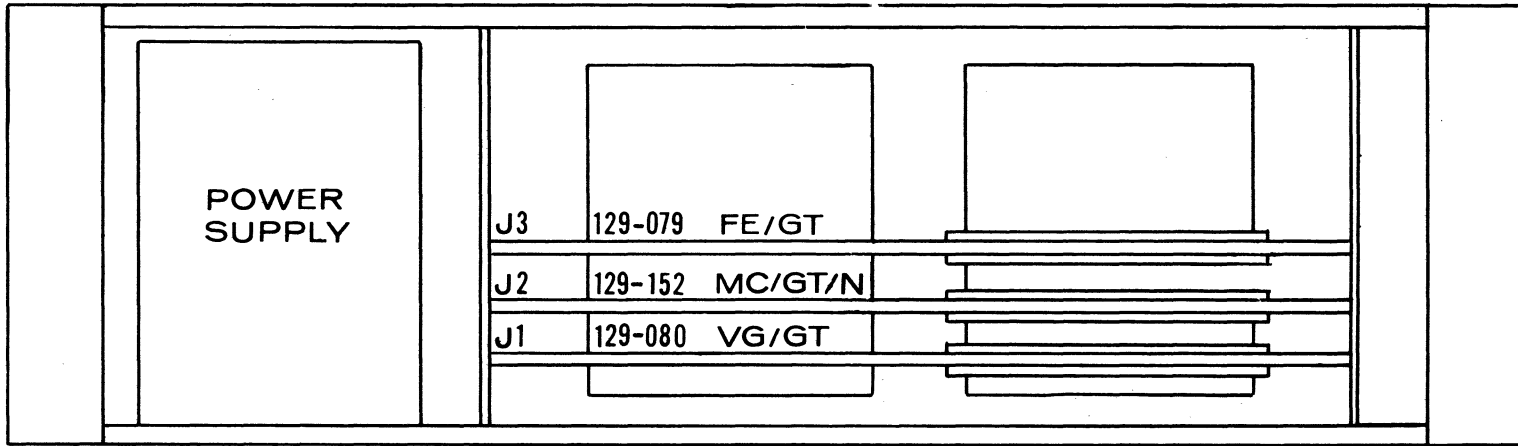
MRD 380 FRONT & REAR PANEL

Fig. 5-5



MRD 380 PC CARD LOCATOR

Fig 5.6



- FRONT VIEW -



must remove cards frequently a "card puller" is recommended. (ADDS service personnel use the "Wire-Grip" puller, part #1733, made by E.H. Titchener and Co., 1 Titchener Place, Binghamton, New York.)

When cards are inserted they should be pushed in until the card shoulder firmly seats against the backplane connector. Cards will not come loose in normal shipment and use since they are firmly seated with long fingers and held in place. However, if the performance of the device is erratic after shipment (or very rough handling is suspected) the cards should be inspected to insure that all are firmly seated.

## SECTION 6:

### TROUBLESHOOTING GUIDE

A troubleshooting chart is presented to the module replacement level. All possible faults can obviously not be listed, but fault diagnosis to the suspect module(s) or subassembly will be facilitated by reference to the chart.

In cases where the cause of a symptom cannot be summarized in a brief phrase the column labeled "Probable Cause" has no entry, but the module(s) or subassembly to be replaced is listed.

#### CAUTION

Turn Power OFF before removing or inserting a Printed Circuit card.

It is essential that, if a defective card has apparently been found, it be reinserted to verify that the symptoms reappear. If the symptoms do not reappear, the fault could have been corrosion on edge connector contacts or a temperature-sensitive I.C. chip. It may be necessary to bring the device back to the operating temperature at which symptoms were first observed to find such chips.

A list of equipment and parts for servicing to both the module replacement level and the chip level is given on page 6-2.

## SERVICE EQUIPMENT AND PARTS

### Minimum and Optional

#### Spare Parts

1. PC Cards (Card complement per Locator Chart in Section 5.)
2. 3 amp SLO-BLO fuse
3. Power Supply - optional
4. Spare chips - optional

#### Tools

1. Phillips head screw driver, medium and small, w/long shank
2. Flat screw driver, medium and small
3. Card extractor
4. Video monitor
5. Extender card - optional
6. Cutters - optional
7. Pliers - optional
8. Soldering iron/solder - optional
9. Solder wick - optional
10. Oscilloscope - optional
11. Trouble lite - optional
12. VOM - optional
13. Frequency counter - optional

## TROUBLESHOOTING CHART

Trouble	Probable Cause	Remedy or Bad Board
Power Light fails to come on when Power On switch pressed	a) AC power	a) check receptacle
	b) fuse	b) replace 1 1/2 amp- ere "SLO-BLO" fuse
	c) faulty switch	c) replace switch
	d) faulty light	d) replace light
Fan fails to come on when Power lamp is ON.	a) faulty fan	a) replace fan
Picture fails to appear after warmup time. Power light and fan OK.	a) poorly adjusted contrast or brightness	a) adjust contrast and/or brightness
	b) poorly seated P.C. cards	b) remove shroud (open MRD-380 panel) and check card seating
	c)	c) VG/GT card
	d) power supply faulty	d) check for shorts or replace supply
Picture fails to appear on screen but does appear on external monitor	a) poorly adjusted contrast or brightness	a) adjust controls
	b)	b) remove shroud (Consul series) and replace P.C. card on internal monitor chassis
	c) faulty Brightness or Contrast pots	c) replace pots
	d) loose connector on monitor	d) remove shroud and check connector on rear of monitor (Consul series)
		e) VG/GT card

<u>Trouble</u>	<u>Probable Cause</u>	<u>Remedy or Bad Board</u>
Screen comes up blank after POWER ON and no characters may be entered, but cursor moves when characters keyed		a) MC/GT card b) FE/GT card c) VG/GT card
Screen comes on full of random characters	a) Power on reset circuitry faulty b) Power down too short	a) replace MC/GT b) cycle power Sw.
Unit gets hot and shuts down	a) blocked fan b) stopped fan c) power supply malfunction or thermal cutoff	a) clear b) clear or replace c) replace power supply
All " " on screen		a) VG/GT card
"?" or "@" on 1/3 or more of screen		a) MC/GT card
Characters distorted by extra dots in character field	b) low +5V supply	a) VG/GT card b) adjust +5V or replace
Characters are not recognizable but may be altered by keying from the keyboard	b) low +5V supply	a) VG/GT card b) adjust +5V or replace
All positions on screen appear black w/narrow white borders		a) VG/GT card

<u>Trouble</u>	<u>Probable Cause</u>	<u>Remedy or Bad Board</u>
Certain groups of characters cannot be entered on screen		a) FE/GT card b) VG/GT card c) Keyboard replacement
Black vertical line appears in middle of screen with data running up screen		a) VG/GT card
Screen torn and distorted	b) faulty monitor c) 50 or 60 cycle operation jumpers incorrect	a) VG/GT card b) replace monitor c) correct as per description on VG/GT schematic
Characters have missing horizontal lines		a) VG/GT card
Characters appear in Right or Left margin		a) VG/GT card
Page on screen wrong in horizontal or vertical size		a) VG/GT card b) adjust TV monitor
Cannot move cursor		a) replace keyboard b) VG/GT card c) MC/GT card

Trouble	Probable Cause	Remedy or Bad Board
Cursor moves erratically	b) noisy keyboard	a) VG/GT keyboard b) keyboard replacement
	c) +5v supply low	c) adjust +5v
	One cursor control fails to work	a) VG/GT card
b) FE/GT card		
c) faulty keyboard		c) check cable, replace keyboard if faulty
REPEAT key fails to operate	a) FE/GT card	
	b) faulty keyboard	b) check cable, replace keyboard if faulty
No cursor visible, but data on screen	a) VG/GT card	
	b) MC/GT card	
Cannot enter data	a) full duplex switch in FDX position	a) switch to HDX (release switch)
	b) modem off line but plugged into EIA connector	c) keyboard replacement
	c) faulty keyboard	
	d) switch 2 on (FE/GT card)	d) turn switch off
		e) FE/GT card
CR or ERASE fills rest of line or whole screen with some characters other than space		a) MC/GT card

Trouble	Probable Cause	Remedy or Bad Board
Data from keyboard is entered in wrong lines sometimes		a) VG/GT card b) MC/GT card
Characters sometimes not entered on screen or missing from words		a) keying in too fast
Characters appear to be entered incorrectly in 1/3 of screen		a) MC/GT card
Characters appear to be entered incorrectly in all of screen		a) MC/GT card b) VG/GT card c) FE/GT card d) keyboard
Cursor Address function fails to operate		a) VG/GT card
Cursor Address operates but cursor goes to wrong location		a) VG/GT card
Line Address function fails to operate		a) VG/GT card
Line Address operates but cursor goes to wrong line		a) VG/GT card



Trouble	Probable Cause	Remedy or Bad Board
Carriage Return fails to operate properly		a) MC/GT card b) FE/GT card
Characters don't scroll up screen		a) MC/GT card
Once data scrolls it doesn't stop; keeps scrolling		a) MC/GT card
Data changes when shifting from bottom 1/3 to middle third or from middle third to top third of screen		a) MC/GT card
Printer fails to operate - power button seems to be ON	a) Power-ON indicator will show "ON" even though Printer is not plugged into AC outlet. Check by pushing LF button b) Not in PRINT ON mode c) not plugged into terminal d) faulty printer	a) plug in and check printer b) press PRINT ON c) plug into terminal d) replace printer
Characters to Printer not the same as on screen		a) FE/GT card b) bad printer
Printer fails to CR after printing only one character on a line when New Line sent from terminal	a) printer out of adjustment	a) refer to Printer Manual

Trouble	Probable Cause	Remedy or Bad Board
Printer returns to next line before the terminal has finished sending a given line	a) printer out of adjustment	a) refer to Printer Manual
EIA output data does not operate	a) bad cable b) wrong baud rate	a) repair cable b) correct setting c) FE/GT card d) "Clear to Send" false
EIA data input does not operate but output operates	a) cable wrong b) wrong baud rate	a) replace cable b) correct setting c) FE/GT card
EIA interface operates but current loop does not	a) cable wrong b) wrong baud rate c) S2 on FE/GT d) loop polarities reversed	a) replace b) correct setting c) FE/GT card S2 on d) reverse polarity
Data to EIA device or from EIA device has high error rate but EIA device check OK	a) baud rate wrong b) frequency of baud rate incorrect	a) correct setting b) replace FE/GT card or adjust frequency
Terminal is hung up and one can not enter anything on screen	a) EIA cable plugged in with no device attached or power off	a) unplug cables

Trouble	Probable Cause	Remedy or Bad Board
CARRIER light fails to come on but EIA appears to function	a) lamp bad	a) replace lamp
	b) EIA cable wrong	b) check Carrier Detect signal
	c) FE/GT card	c) replace FE/GT
"*" written on screen	a) parity error	a) set switches on FE/GT card as per schematic
	b) framing error	b) check EIA device

## POWER SUPPLY SUBASSEMBLY

This section describes the power supplies used in the ADDS Consul series of desktop terminals and the MRD series of rack-mountable equipment. A number of variations exist between the two power supplies.

The variations are:

## 1. Transformer

The power transformer for the Consul is separate from the power supply and located under the card cage. It is also physically different from the power transformer used on the MRD. The MRD transformer is an integral part of the power supply.

## 2. Fan

The fan on the Consul is mounted next to the transformer under the card cage. On the MRD the fan is located on the rear panel. The two power supplies will be described starting with the Consul power supply.

## SPECIFICATIONS

Input - 105-125 VAC/205-250 VAC (strapping option)

Input Frequency - 50-60, 400 Hz

Input Breakout - Below 100/195 VAC

## Outputs

a. +5.2 VDC $\pm 10\%$ Adjustable	9.0A continuous
b. +13.2 VDC	1.5A continuous
c. -13.2 VDC	1.2A continuous

## Regulation

	Specification	
Line Regulation (*)	+5.2V	$\pm 0.5\%$
	+13.2V	$\pm 0.5\%$
	-13.2V	$\pm 0.5\%$
Load Regulation (**)	+5.2V	$\pm 0.5\%$
	+13.2V	$\pm 0.5\%$
	-13.2V	$\pm 0.5\%$

\* Low line to high line for both 115 and 230 VAC

\*\* Full load to no load

Ripple*	Specification	Typical
+5.2V	30mV p/p	6mV p/p
+13.2V output	30mV p/p	6mV p/p
-13.2V output	30mV p/p	6mV p/p

\* At full load

#### Overload protection

All outputs are protected by individual foldback circuits against continuous overloads and short circuits with automatic recovery upon removal of overload condition.

#### Overvoltage Protection

Crowbars for the +5.2 VDC output is present between +6.50 and 7.50 VDC. The +13.2 VDC and -13.2 VDC outputs have a combined crowbar preset between 14.5 and 17.5 V for each output.

#### DC output Adjust

+5.2 VDC output will be adjustable by a Cermet pot 5.2 V  $\pm 10\%$ . The +13.2 VDC and -13.2 VDC will be set by fixed resistors.  $\pm 2\%$ .

#### Temperature Coefficient and Stability

T.C.: 0.02%/°C  
 Stability: 0.1% for any 8 hour period after 30 min. stabilization

#### Operating Temperature

-20° to +55°C

#### Storage Temperature

-55° to +85°C

#### Overtemperature Protection

Thermostat protection provided to turn off AC input in the event ambient temperature goes beyond approximately 70°C. Heatsink temperature protected at 100° to 108°C.

#### Fusing

To protect the power supply from internal faults an input fuse should be used. For 115V input 3.0A SLO-BLO fuse is recommended. A 1.5A fuse must be used for 230V input.

#### Cooling

The power supply is designed for operation with forced air ducted through the power supply cavity.

## THEORY OF OPERATION

### General

The 285-01000 power supply consists of three separate series regulators obtaining their power from a common transformer. Both positive regulators are similar in design and operation. The +5V and +13.2V are positive regulators while the -13.2 is a negative regulator. The sensing, drive and series-pass circuit vary slightly. Each circuit has a full wave rectifier, filter capacitor, complete IC regulator, Darlington pass transistor. An overvoltage crowbar circuit is provided for the +5V circuit and a combined OV circuit for the +13V circuits.

### Circuit Description

115 or 230 VAC is applied to transformer T1 (see schematic for proper jumper connection on transformer for 115 or 230 VAC operation). All input and output connections are made through connectors J1 to J3.

### 5Volt Regulator Circuit

The center tapped transformer winding feeds rectifier, CR1, and the rectified DC is filtered by capacitor C1. The filtered unregulated DC is then fed to the collector of series-pass transistors Q1, Q2 which produce the proper voltage drop to keep the output regulated at the preset voltage. IC regulator U1 consists of voltage reference, error amplifier output transistor and current limit circuit. The output voltage is connected directly to the inverting input Pin 4. The reference voltage is connected to a voltage divider R18, R19, and R20. The reference voltage is divided down to 5.2V with potentiometer R12 and fed to the noninverting input. The regulator will then automatically adjust and maintain the output voltage at the voltage set with potentiometer R19. R19 allows to vary the output voltage at least +10%. The output of the EC regulator feeds driver Q3 which controls passing transistors Q1 and Q2. Overload protection is provided by sensing the voltage drop across emitter resistor R2, R3 plus base emitter voltage of Q1 and Q2. The sense voltage is picked up through voltage divider R4, R5 and fed to the IC regulator in such a manner that drive to Q1 is removed in case excessive current is drawn. In case of a short circuit only a fraction of the nominal output current can be drawn. The input to U1 is fed from the +13.2V output, since the IC regulator requires a voltage several volts greater than its output. Therefore, the +5.2V circuit depends on the presence of the +13.2 volt output.

### +13.2 Regulator Circuit

Transformer secondary winding feeds rectifier bridge CR2. The rectified DC is filtered by capacitors C2. The filtered, unregulated DC is then fed to the collector of the series-pass transistors Q4 which produces the proper voltage drop to keep the output regulated at the preset voltage. Except for the sensing bridge, the 13V circuits operate exactly like the 5.2V described above. The reference voltage from pin 6 of IC U2 is fed directly to the non-inverting input, pin 5. R21, R22 and R23 is the level as the reference voltage (approx 7.15V). This sample of the output voltage is then fed to the inverting pin 4. Jumpers JA and JB across R23 are used to set the output voltage to within +2%. The input to U2 is fed from the bias rectifier circuit (CR3 and C4) which is in series with the +13.2V unregulated DC. This produces an input to U2 several volts greater than its output. Transistor Q4 is a Darlington Transistor.

### -13.2V Circuit

As mentioned above, a negative regulator is employed for the -13V output in order to feed both 13V outputs from a center tapped bridge rectifier circuit. The negative output of CR2 is filtered by C3 and the unregulated voltage is then connected to the -13V Darlington transistor Q5. Q5 and Q6 are connected as a complementary Darlington configuration. The divided reference voltage is connected to the inverting input pin 4 of IC U3 and a sample of the output voltage is fed to the non-inverting input pin 5. Base current for Q6 is supplied through resistor R9 in such a manner that the output current supplied by U3 must increase in order to reduce the regulator output voltage. In case U3 is cut off, the regulator goes into a high output state since maximum Q6 base current can flow through R9. A separate foldback transistor Q7 is utilized for this circuit which works in similar fashion as the 5.2V foldback circuit except that in case of an overload Q7 will supply current into R9 thus reducing Q6 base current. This produces the foldback action and limits the output current in case of an overload.

### Overvoltage Crowbar Circuit

Silicon controlled rectifier Q10 is connected across the +5.2V output. Zener diode VR1, R33, R29, and R30 form a sensing bridge to detect an overvoltage. Q8 is normally not conducting. In case of an overvoltage Q8 will turn on and fire the SCR which causes the output voltage to drop to less than 1.5V. The +13.2V and -13.2V outputs have a combined OV circuit that is identical in operation to the +5.2V circuit except that the anode of SCR Q11 is connected to the +13.2V output and the cathode is connected to the -13.2V output. Zener diode VR2, R35, R31, and R32 form the sensing bridge which in the event of an overvoltage in either output will turn on Q9 and fire Q11 which causes the output to drop to less than 1.4V. CR4 and CR5 protect the outputs from excessive negative voltage.

## Operating Instructions

Connections to the power supply are made through J1, J2, and J3 on the PC board. The transformer is provided with an 18" long cable terminated with a connector which is plugged into J3 on the power supply. The output is connected at J2 and the monitor connection is available at J3. The output voltages have been factory pre-set. The +5V output can be adjusted with potentiometer R19. The power supplies are designed to operate with forced air. Should the fan fail or air-flow be severely restricted, the heatsink will get excessively hot and the thermostat S1 will open, interrupting input power. Operation will continue after power supply has sufficiently cooled off. If this should occur, operation should be discontinued until proper air flow is restored.

## MAINTENANCE

### General

This section describes the trouble analysis routine and test procedures that are useful for servicing the power supply. A chart is provided for troubleshooting. Refer to Specifications for minimum performance standards.

### Trouble Analysis

Whenever a problem develops, systematically check all fuses, primary power connections, input and output connectors J1, J2 and J3, external circuit elements, and external wiring before troubleshooting the equipment. Failures and malfunctions often can be traced to simple causes such as improper jumpers and supply load connections or fuse failure. Use the schematic diagram as an aid to locating trouble causes. The voltage chart contains various circuit voltages that are averages for normal no-load operation. Use measuring probes carefully to avoid causing short circuits and damaging circuit components.

### Checking Transistors and Capacitors

Check transistors with an in-circuit transistor checker. If no checker is available, transistors can be checked with an ohmmeter that has a highly limited current capability. Observe proper polarity for NPN transistors. The forward transistor resistance is low but never zero; backward resistance is always much higher than the forward resistance. When soldering semi-conductor devices, hold the lead being soldered with pliers or a heat sinking device placed between the component and the solder joint.

Note: The leakage resistance obtained from a simple resistance check of a capacitor is not always an indication of a faulty capacitor. In most cases the capacitors are shunted with resistances some of which have low values. Only a dead short is a true indication of a shorted capacitor.



## Printed Circuit Board Maintenance Techniques

Voltage measurements can usually be made from both sides of the board. Use a needle point probe or another suitable measuring probe. Broken or damaged printed wiring is usually the result of an imperfection or strain. To repair small breaks, tin a short piece of hook-up wire to bridge the break and, holding the wire in place, flow solder along the length of wire so that it becomes a part of the circuit. When unsoldering components from the board never pry or force the part loose; use a solder-sucker to remove solder before loosening a component. If a solder-sucker is not available, use tinned copper braid or stranded wire (AWG 14 or 16).

### Trouble Chart

The trouble chart is intended as a guide for locating trouble causes, and is used along with the schematic.

The operating conditions assumed for the trouble chart are as follows:

- a. AC power of proper voltage and frequency is present at input terminals
- b. All loads have been removed

---

<u>Symptoms</u>	<u>Probable Cause</u>	<u>Remedy</u>
No output voltage	S1 open	Replace S1 if it does not reset when cool.
	T1 defective	Check T1 for proper output voltage, replace if necessary
	U1, U2, or U3 defective	Replace if no output on pin 10 or pin 9 on U3 and/or no reference voltage on pin 6
Low output voltage	Q1 to Q6 open	Check and replace
	CR1, 2, or 3 defective	Check and replace
	C1, 2 or 3 shorted	Check and replace

Symptoms	Probable Cause	Remedy
	SCR fired	Rise input voltage slowly and check if OV ckt. crowbars at the right voltage. If yes, check next symptom below. Check for shorted SCR
Output voltage too high	Q1 to Q6 shorted	Check and replace
NOTE: High output may activate OV circuit	U1, U2, or U3 defective	Check and replace
High ripple & unregulated DC	AC input voltage too low	Ck AC line voltage
	Open rectifier CR1, 2, 3	Check and replace
	Excessive Load	Check load current

NOTE: +5.2V output depends on +13.2V output. Check +13.2V output before troubleshooting +5.2V output.

High output may activate OV crowbar. Troubleshoot with reduced input voltage. Use variable transformer to keep output voltage below trip voltage.

### Typical Voltages

Voltage readings taken at 115VAC line input and no load

T1	Blue, Blue -White	10.6 VAC
	Green - White to Green	16.9 VAC
	Green - Yellow to Green	16.9 VAC
	Green - White to Red	
	Green	22.0 VAC
C1		14.2 VDC
C2		23.0 VDC
C3		23.0 VDC
Common to U1-6		6.8-7.5 VDC
Common to U2-6		6.8-7.5 VDC

-13V output to U3-6	6.8-7.5 VDC
VR1	3.3 VDC
VR2	5.6 VDC
Common to Q3 - Base	6.2 VDC
Common to Q4 - Base	14.2 VDC
Common to Q6 - Base	-13.8 VDC
Common to Q2 - Base	5.7 VDC

Note: Voltage readings may vary slightly between units

POWER SUPPLY DRAWINGS AND PHOTOGRAPHS, Consul

Presented on the following pages are:

Figure 7.1 - A photo of the Consul power supply

Figure 7.2 - Diagram of harness connections to power supply

Figure 7.3 - Consul Power Supply Schematic

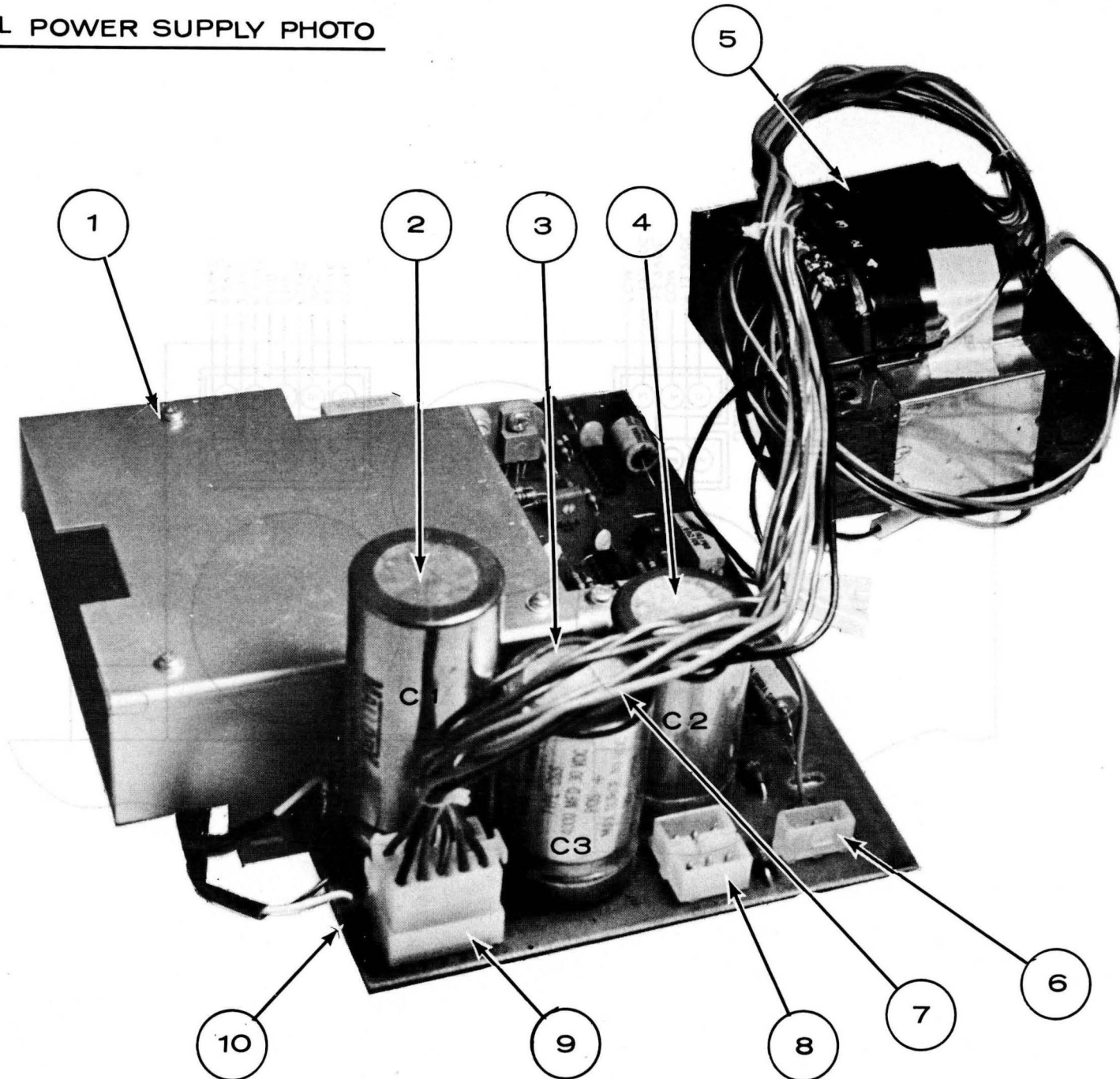
Figure 7.4 - Consul Power Supply Assembly

In Figure 7.1, the major components identified are as follows:

1. Heatsink, mounting bracket
2. Filter capacitor (C1)
3. Filter capacitor (C3)
4. Filter capacitor (C2)
5. Transformer
6. Monitor Molex connector
7. Transformer power harness
8. Card cage power connector
9. Transformer power connector
10. P.C. board power supply

CONSUL POWER SUPPLY PHOTO

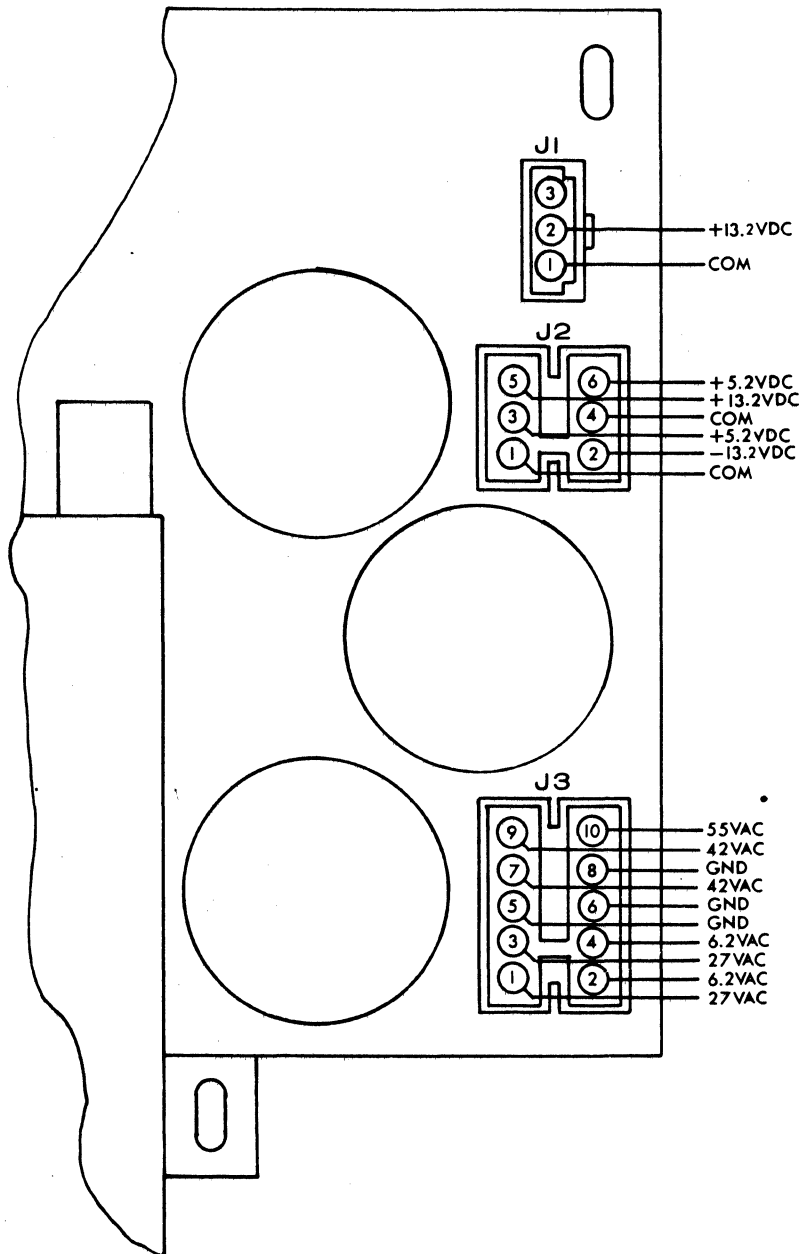
Fig. 7.1



U.S. AIR FORCE  
HEADQUARTERS ELECTRONIC CENTER, BOWLING GREEN, OHIO

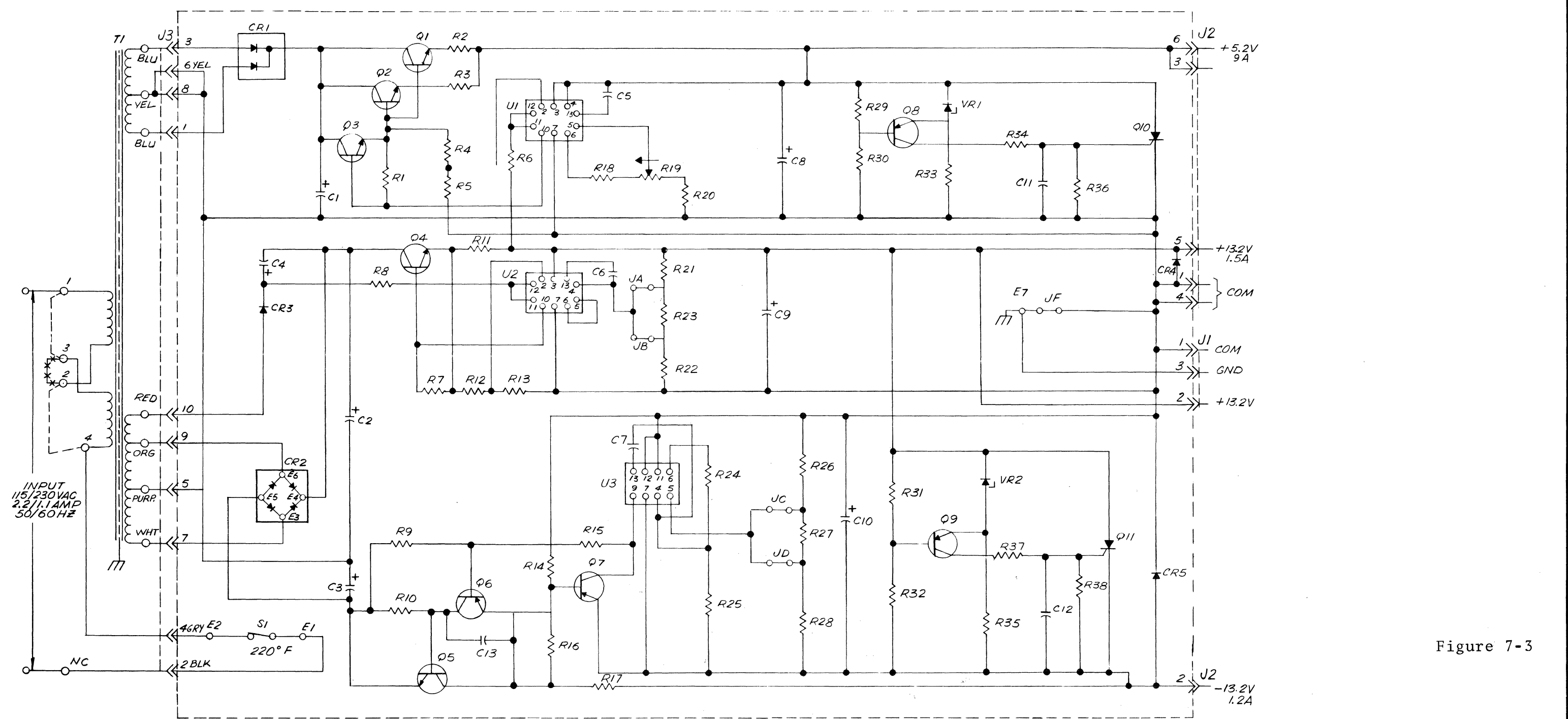
# HARNESS CONNECTIONS, CONSUL POWER SUPPLY

Fig. 7-2



REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	RELEASE FOR PROD.	5-8-76	EB
B	ECO 050-40100	4-12-77	EB
C	ECO 050-40508 (CANCELLED)	7-18-78	
D	ECO 050-40540	3-30-78	CPM

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OUTPUT CONNECTIONS  
 J1-  
 1 COM RET  
 2 +13.2V  
 3 CHASSIS GND  
 J2-  
 1 COM RET 5 +13.2V  
 2 -13.2V 6 +5.2V  
 3 +5.2V  
 4 COM RET

TRANSFORMER INPUT CONN  
 AC INPUT  
 NEUTRAL 1  
 AC HOT NC  
 FAN 1&2  
INPUT JUMPERS:  
 115 VAC 1-3 & 2-4  
 230VAC 2-3

Figure 7-3

7-11/7-12

TOLERANCES:		1/64	.005	1°	<b>ADDIS</b> Applied Digital Data System, Inc. Hauppauge, New York
FRAC DEC ANG					
DO NOT SCALE DWG					
DATE	5/6/76				
CHECKED	1/12/77				
APPROVED	5-19-78				
DATE	5-19-78				
APPROVED	CPM				
NEXT ASSY	USED ON	QTY	5-19-78		
PART NO		285-01000	REV	D	
SCALE		NONE	SHEET	1/41	D







BILL OF MATERIAL

MATRIX

**ADDS** Applied Digital Data System Inc.  
100 Marcus Blvd. Hauppauge, New York

DRAWN BY	N. Brown	5/8/76	TITLE	ASS'Y PWR SUPPLY NEW BASE AND SHROUD		
CHECKED BY		5/19/78	REV.	SHEET 3 OF 3	DWG. NO.	285-010
APPROVED BY	CPM	5-19-78				00

ITEM	ADDS P/N	QTY.	DESCRIPTION	REF. DES.	REV	D								
1														
2	129-17100		PC ASSEMBLY			1								
3	500-03300		CHASSIS (HEATSINK BKT)			1								
4	500-03400		COVER			1								
5	360-34500		HEATSINK			5								
6	360-30900		TRANSISTOR INS. MICA			5								
7	360-31000		TRANSISTOR INS. MICA			1								
8	360-31100		THERMOSTAT 220°F			1								
9	360-31200		NYLON SHOULDER WASHER			10								
10	360-31300		NYLON SHOULDER WASHER			1								
11	360-31400		LUG BURNDY BA16E-6M			5								
12	350-01300		TRANSFORMER ASSEMBLY			1								

**BILL OF MATERIAL**

**MATRIX**

**ADDS** Applied Digital Data System Inc.  
100 Marcus Blvd. Hauppauge, New York

<b>DRAWN BY</b>	BISESTI	7-26-77	<b>TITLE</b>								
<b>CHECKED BY</b>	Ⓢ	7-26-77	ASS'Y PWR SUPPLY P.C. BOARD								
<b>APPROVED BY</b>			<del>REV.</del>	SHEET 2 OF 4	DWG. NO.	129-171	00				
<b>ITEM</b>	<b>ADDS P/N</b>	<b>QTY.</b>	<b>DESCRIPTION</b>			<b>REF. DES. REV.</b>	<b>B</b>				
1	123-17100		PC BOARD PWR SUPPLY				1				
2	140-13300		CAPACITORS 16KUF, 15V			C1	1				
3	140-13400		CAPACITORS 4KUF, 30V			C2 & C3	2				
4	140-13500		CAPACITORS 22UF, 25V			C4	1				
5	140-08400		CAPACITORS .001UF, 500V			C5	1				
6	140-13600		CAPACITORS 390PF, 500V			C6 & C7	2				
7	140-13700		CAPACITORS 220UF, 16V			C8, C9, C10	3				
8	140-13800		CAPACITORS .33UF, 3V			C11 & C12	2				
9	302-00700		RESISTOR 470 OHM, 1/4W			R1, R10, R28, R7	4				
10	310-00200		RESISTOR .15 OHM, 5W			R2 & R3	2				
11	302-00100		RESISTOR 75 OHM, 1/4W			R4	1				
12	302-00400		RESISTOR 220 OHM, 1/4W			R5	1				
13	302-11000		RESISTOR 47 OHM, 1/4W			R6	1				
14	302-11600		RESISTOR 12 OHM, 1/4W			R8	1				
15	302-03100		RESISTOR 3.3K OHM, 1/4W			R9	1				
16	309-00200		RESISTOR .68 OHM, 3W			R11 & R17	2				
17	302-06700		RESISTOR 270 OHM, 1/4W			R12, R16, R29, R37	4				
18	302-02100		RESISTOR 4.7K OHM, 1/4W			R14, R13	2				
19			JUMPER				1				
20	302-04900		RESISTOR 390 OHM, 1/4W			R18	1				
21	313-02000		POTENTIOMETER 500 OHM, 1/2W			R19	1				
22	302-01900		RESISTOR 1.5K OHM, 1/4W			R20	1				
23	302-01000		RESISTOR 820 OHM, 1/4W			R21, R31	2				
24	302-01100		RESISTOR 1K OHM, 1/4W			R22	1				
25	302-11100		RESISTOR 68 OHM, 1/4W			R23	1				

7-17

7-18

## BILL OF MATERIAL

## MATRIX


**ADDS** Applied Digital Data System Inc.  
100 Marcus Blvd. Hauppauge, New York

ITEM	ADDS P/N	QTY.	DESCRIPTION	REF. DES.	REV				
DRAWN BY		BISESTI	7-26-77	TITLE					
CHECKED BY			7-26-77	ASS'Y PWR SUPPLY P.C. BOARD					
APPROVED BY				REV.	SHEET 3 OF 4	DWG. NO.	129-171	00	
								B	
26	302-05800		RESISTOR 2.7K OHM, 1/4W	R24				1	
27	302-05700		RESISTOR 3K OHM, 1/4W	R25, R32				2	
28	302-03400		RESISTOR 1.2K OHM, 1/4W	R26				1	
29	302-03700		RESISTOR 33 OHM, 1/4W	R34				1	
30									
31	302-04600		RESISTOR 180 OHM, 1/4W	R30, R33				2	
32	304-02700		RESISTOR 1.5K OHM, 1/2W	R35				1	
33	302-03000		RESISTOR 680 OHM, 1/4W	R36, R38				2	
34									
35	190-02900		RECTIFIER 1N4001	CR3 & CR6				2	
36	191-00300		RECTIFIER C.T.					1	
37	191-00100		RECTIFIER BRIDGE	CR2				1	
38	191-00200		RECTIFIER 1N5402	CR4 & CR5				2	
39	330-02300		TRANSISTOR RCA 65826	Q1 & Q2				2	
40	330-02400		TRANSISTOR RCA 31	Q3				1	
41	330-02700		TRANSISTOR 2N6055	Q4 & Q5				2	
42	330-02800		TRANSISTOR 2N3645	Q6				1	
43	330-00500		TRANSISTOR 2N3906	Q7, Q8, Q9				3	
44	330-02900		SCR C123F	Q10, Q11				2	
45	200-24800		IC LM723CN	U1, U2, U3				3	
46	190-00200		ZENER 1N746A	VR1				1	
47	190-00100		ZENER 1N752A	VR2				1	
48	170-15900		PCB PIN HEADER	J1				1	
49	170-07700		PCB PIN HEADER	J2				1	
50	170-11000		PCB PIN HEADER	J3				1	

**BILL OF MATERIAL**

**MATRIX**

**ADDS** Applied Digital Data System Inc.  
100 Marcus Blvd. Hauppauge, New York

DRAWN BY	BISESTI	7-26-77	TITLE		
CHECKED BY		7-26-77	ASS'Y PWR SUPPLY P.C. BOARD		
APPROVED BY			REV	SHEET 4 OF 4	DWG. NO. 129-171


ITEM	ADDS P/N	QTY.	DESCRIPTION	REF. DES. REV	B
51					
52	140-13900		CAPACITOR .0022UF, 500V	C13	1
53	302-12200		RESISTOR 1B OHM, 1/4W	R27	1
54			JUMPER		5
55	140-09800		.047UF@100V 10%	C14	1

## MRD POWER SUPPLY SPECIFICATIONS

### Input Voltage

105-125 VAC/210-250 VAC (strapping option)

### Input Frequency

50-60,400 Hz

### Input Breakout

Below 100/195 VAC

### Outputs

- (a) +5.2 VDC +10% @ 6.75 A continuous
- (b) +13.2 VDC @ 0.5 A continuous
- (c) -13.2 VDC @ 1.0 A continuous

### Regulation

Line: +0.5% Low Line to High Line for both 115V and 230 VAC

Load: +0.5% No Load to Full Load

### Ripple

10 mV RMS max.

30 mV Peak to Peak max.

### Overload Protection

All outputs protected by individual foldback circuits against continuous overloads and short circuits. Automatic recovery upon removal of overload condition.

### Overvoltage Protection

Individual crowbars for each output: +5.2 VDC output to be preset between +6.50 and +7.5 VDC. The +13.2 VDC and -13.2 VDC outputs will be preset between 15.0 and 17.0 VDC.

### DC Output Adjust

The 5.2 VDC output is settable by means of a Cermet potentiometer to +10% of nominal. The +13.2 VDC and -13.2 VDC outputs are set by fixed resistors to + 2% of nominal.

### Temperature Coefficient and Stability

T.C.: 0.02%/°C

Stability: 0.1% for any 8 hour period after 30 min. stabilization

### Operating Temperature

-20°C to +55°C

### Storage Temperature

-55° to +85°C

### Overtemperature Protection

Thermostat protection provided to turn off AC input in the event ambient temperature goes beyond 75°C. Heatsink temperature protected at 100° to 108°C.

### Fusing

To protect the power supply from internal faults an input fuse should be used. For 115V input a 1.5 A SLO-BLO fuse is recommended. A 0.75 A SLO-BLO fuse must be used for 230V input.

### P.C. Boards

P.C. boards should be easily field replaceable without desoldering.

### Humidity

The operating range is 0-95% R.H., non-condensing.

## THEORY OF OPERATION

### General Power Supply Description

The power supply consists of three separate series regulators obtaining their power from a common transformer. All three regulators are basically the same in design and operation. Only the sensing, drive and series-pass circuit vary slightly. Each circuit has a full wave rectifier, filter capacitor, complete IC regulator, pass transistor, driver and overvoltage SCR crowbar.

Fold out the power supply schematic drawing, Figure 7.8 on pages 7-31 before proceeding to the circuit description below.

## Circuit Description

### 1. Input Transformer

Input voltage of 115 or 230 VAC is applied to transformer T1; see schematic for proper jumper connection on transformer for 115 or 230 VAC operation. All input and output connections are made through terminal board TB1.

### 2. 5 Volt Regulator Circuit

The center tapped transformer winding feeds rectifiers CR2 and CR3 and the rectified DC is filtered by capacitor C6. The filtered unregulated DC is then fed to the collector of series-pass transistors Q4, Q5 which produce the proper voltage drop to keep the output regulated at the preset voltage. IC regulator A1 consists of voltage reference, error amplifier series-pass transistor and current limit circuit. The output voltage is connected directly to the inverting input. The reference voltage is connected to a voltage divider R7, R8 and R9. The reference voltage is divided down to 5 V with potentiometer R8 and fed to the noninverting input. The regulator will then automatically adjust and maintain the output voltage at the voltage set with potentiometer R8. R8 allows to vary the output voltage at least  $\pm 10\%$ . The output of the IC regulator feeds driver Q1 which controls passing transistors Q4 and Q5. Overload protection is provided by sensing the voltage drop across emitter resistor R18, R19 plus base-emitter voltage of Q4 and Q5. The sense voltage is picked up through voltage divider R5, R6 and is fed to the IC regulator in such a manner that drive to Q1 is removed in case excessive current is drawn. In cases of a short circuit only a fraction of the nominal output current can be drawn. The input to A1 is fed from the +13.2 V output, because the IC regulator requires a voltage several volts greater than its output. Therefore, the +5 V circuit depends on the presence of the +13.2 V output.

### 3. +13 and -13 V Regulator Circuit

Both circuits are identical except for the pass transistor drive circuits. The transformer secondary winding feeds rectifiers CR6 and CR7 and the rectified DC is filtered by capacitor C7. The filtered, unregulated DC is then fed to the collector of series-pass transistor Q6 which produces the proper voltage drop to keep the output regulated at the preset voltage.

Except for the sensing bridge, the 13V circuits operate exactly like the 5V circuit described above. The reference voltage from pin 4 of IC A1 is fed directly at the non-inverting input pin 3. R9, 10 and 11 is a voltage divider, dividing the output voltage down to same level as the reference voltage (approx. 7.15V). This sample of the output voltage is then fed to the inverting input pin 2.

Jumpers J2 and J3 across R11 are used to set the output voltage to within +2%. The -13.2 output has its own rectifier-filter circuit (CR10-CR13, C8). The positive output terminal is connected to the output common.

#### 4. Overvoltage Crowbar Circuit

Silicon controlled rectifiers Q8, Q9 and Q10 are connected across the outputs of each of the three regulators. Zener diode VR2, R14, R15 and R17 form a sensing bridge to detect an overvoltage. Q2 is normally not conducting. In case of an overvoltage Q2 will turn on and fire the SCR which causes the output voltage to drop. All three overvoltage circuits work in the same fashion.

#### OPERATING NOTES

Connections to the power supply are made through the appropriate terminals on the terminal board. The output voltages are factory pre-set. (The +5V output can be adjusted with potentiometer R8.) The power supplies are designed to operate with forced air. Should the fan fail or airflow be severely restricted, the heatsink will get excessively hot and the thermostat K1 will open, interrupting input power. Operation will continue after the power supply has sufficiently cooled off. If this should occur, operation should be discontinued until proper air flow is restored.

Similarly, a short in the terminal backplane wiring could cause the power supply to shut down. If this is suspected, disconnect the output leads (+5.2 VDC, +13 VDC, -13 VDC) from the barrier strip on the power supply and observe whether or not the output voltages at the barrier strip come up to the correct value with the harness to the terminal electronics disconnected. If so, there is a short in the terminal backplane (or P.C. cards) rather than a fault in the power supply itself.

#### MAINTENANCE

##### General

This section describes trouble analysis routines and test procedures that are useful for servicing the power supply. A chart is provided for troubleshooting. Refer to Specifications for minimum performance standards.

##### Trouble Analysis Procedures

Whenever a problem develops, systematically check all fuses, primary power connections, external circuit elements, and external wiring before troubleshooting the equipment. Failures and malfunctions often can be traced to simple causes such as



improper jumpers and supply load connections or fuse failure. Use the schematic diagram as an aid to locating trouble causes. The voltage chart contains various circuit voltages that are averages for normal no-load operation. Use measuring probes carefully to avoid causing short circuits and damaging circuits components.

### Checking Transistors and Capacitors

Check transistors with an in-circuit transistor checker. If no checker is available, transistors can be checked with an ohmmeter that has a highly limited current capability. Observe proper polarity for NPN transistors. The forward transistor resistance is low but never zero; backward resistance is always much higher than the forward resistance.

When soldering semi-conductor devices, hold the lead being soldered with pliers on a heat sinking device placed between the component and the solder joint.

Note: The leakage resistance obtained from a simple resistance check of a capacitor is not always an indication of a faulty capacitor. In most cases the capacitors are shunted with resistance some of which have low values. Only a dead short is a true indication of a shorted capacitor.

### Printed Circuit Board Maintenance Techniques

Voltage measurements can usually be made from both sides of the board. Use a needle point probe or another suitable measuring probe.

Broken or damaged printed wiring is usually the result of an imperfection or strain. To repair small breaks, tin a short piece of hook-up wire to bridge the break and, holding the wire in place, flow solder along the length of wire so that it becomes a part of the circuit.

When unsoldering components from the board never pry or force the part loose; use a solder-sucker to remove solder before loosening a component. If a solder-sucker is not available, use tinned copper braid or stranded wire (AWG 14 or 16).

### Trouble Chart Description

The trouble chart is intended as a guide for locating trouble causes, and is used along with the schematic.

The operating conditions assumed for the trouble chart are as follows:

- (a) AC power of proper voltage and frequency is present at the input terminals.
- (b) All loads have been removed.

## Typical Voltages

Voltage readings taken at nominal AC line voltage and no load.

T1	7-12	18.5 VAC
	5-6, 5-11	10.4 VAC
	8-13	19.2 VAC
C6		14.3 VDC
C7		24.5 VDC
C8		26.2 VDC
C1		-
Com. output	- PC1/A1-4	6.8- 7.5 VDC
"	" PC2/A1-4	6.8 -7.5 VDC
-13V output	- PC3/A1-4	6.8 -7.5 VDC
	PC1/VR2	3.3 VDC
	PC2/VR2	5.6 VDC
	PC3/VR2	5.6 VDC
Com. output	- PC1/Q1 base	6.35VDC
"	" - PC2/Q1 base	14.45VDC
-13V output	- Q7 base	13.8 VDC
Com. output	- Q4 base	5.6 VDC
"	" Q6 base	13.8 VDC

## Trouble Chart

Symptoms	Probable Cause	Remedy
No Output Voltage	K1 open	Replace K1 if it does not reset when cool.
	T1 defective.	Check T1 for proper output voltage; replace.
	A1 defective	Replace if no output on pin 6 or no reference voltage on pin 4.
Low Output Voltage	Q1 open	Check & Replace.
	Q4,5 Q6 Q7 open	Check & Replace.
	CR2,3 CR5,7 (8,9) defective CR10-13	Check & Replace.
	C4 shorted	Check & Replace.
	SCR fired	Raise input voltage slowly and check if OV ckt. crowbars at the right voltage. If yes, check output too high. Check for shorted SCR.
Output Voltage too High.	Q4,5, Q6,Q7 shorted	Check & Replace.
Note: High output may activate OV-circuit	A1 defective.	Check & Replace.
High Ripple & Unregulated DC.	AC input voltage too low.	Check AC line voltage
	Open Rectifier CR2-13	Check & Replace.
	Excessive Load.	Check Load Current.

Notes:

- (a) The +5 Volt output depends on +13 Volt. Check +13V output before troubleshooting +5V output.
- (b) High output may activate OV. crowbar. Troubleshoot with reduced input voltage. (Use variable transformer to keep output voltage below trip voltage.)
- (c) If trouble is suspected to be on PC board, replace entire board if one is available.

POWER SUPPLY DRAWINGS AND PHOTOGRAPHS

Presented on following pages are:

Figure 7.5 - A photo of the MRD power supply.

Figure 7.6 - Photos of the three P.C. boards on the power supply.

Figure 7.7 - Diagram of harness connection to power supply barrier strip.

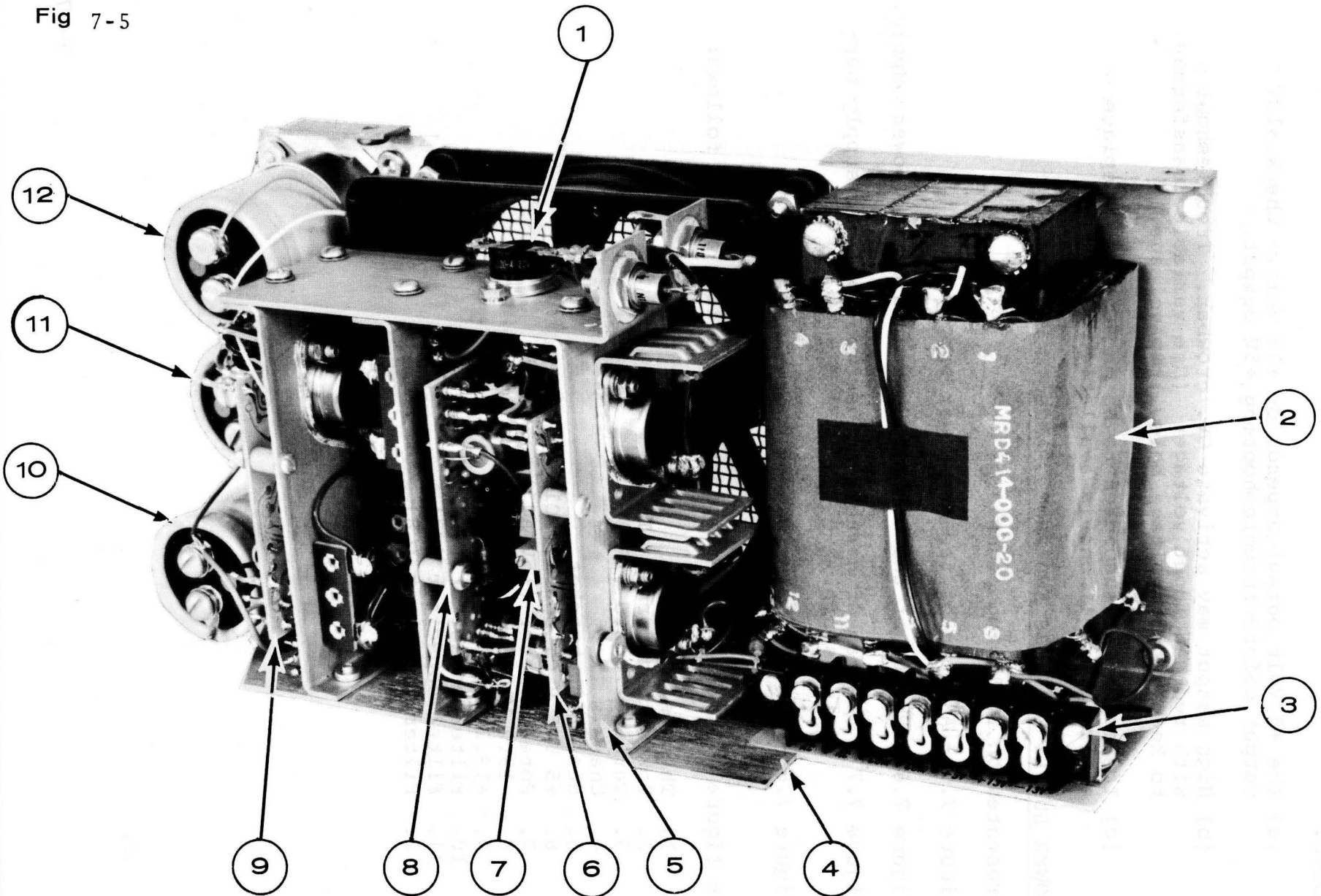
Figure 7.8 - Power Supply schematic drawings.

In figure 7.5, the major components identified are as follows:

1. Thermostat
2. Power transformer (T1)
3. Terminal board (TB1)
4. Chassis
5. Heat sink bracket
6. +5 VDC P.C. Board (PC1)
7. Potentiometer (+5V adj)
8. -13.2 VDC P.C. Board (PC3)
9. +13.2 VDC P.C. Board
10. Filter capacitor (C6)
11. Filter capacitor (C7)
12. Filter capacitor (C8)

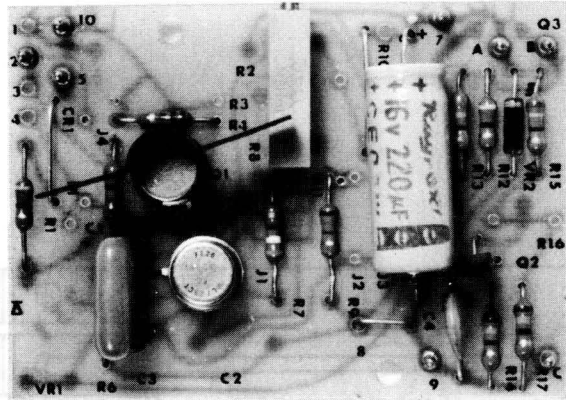
# MRD POWER SUPPLY

Fig 7-5

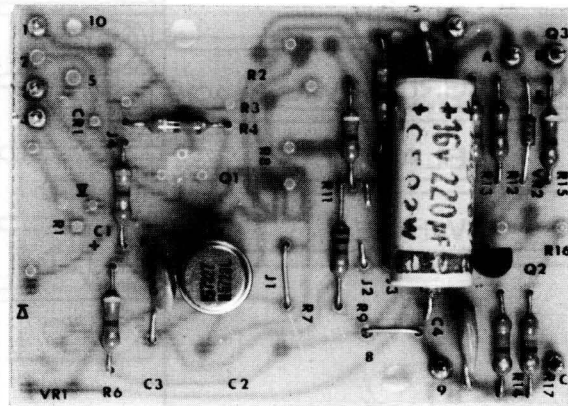


P.C. BOARDS, POWER SUPPLY MRD

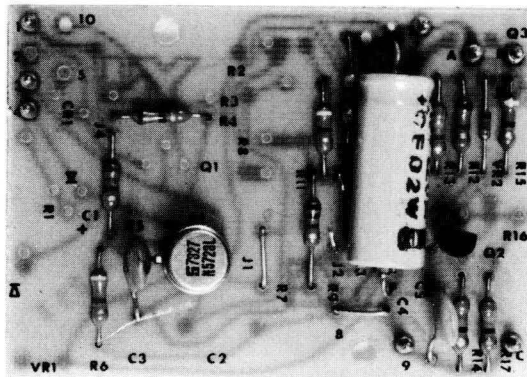
Fig. 7-6



+5VDC PCI 360-110



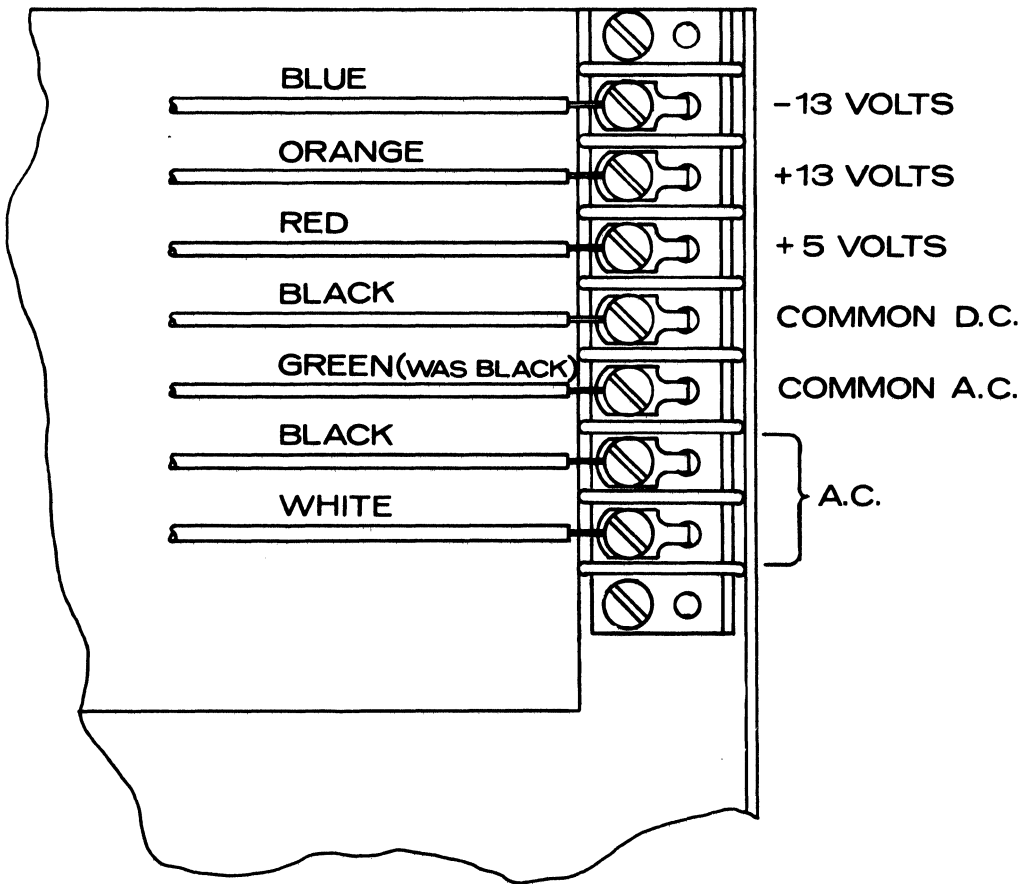
+13.2VDC PC2 360-132



-13.2VDC PC3 360-115

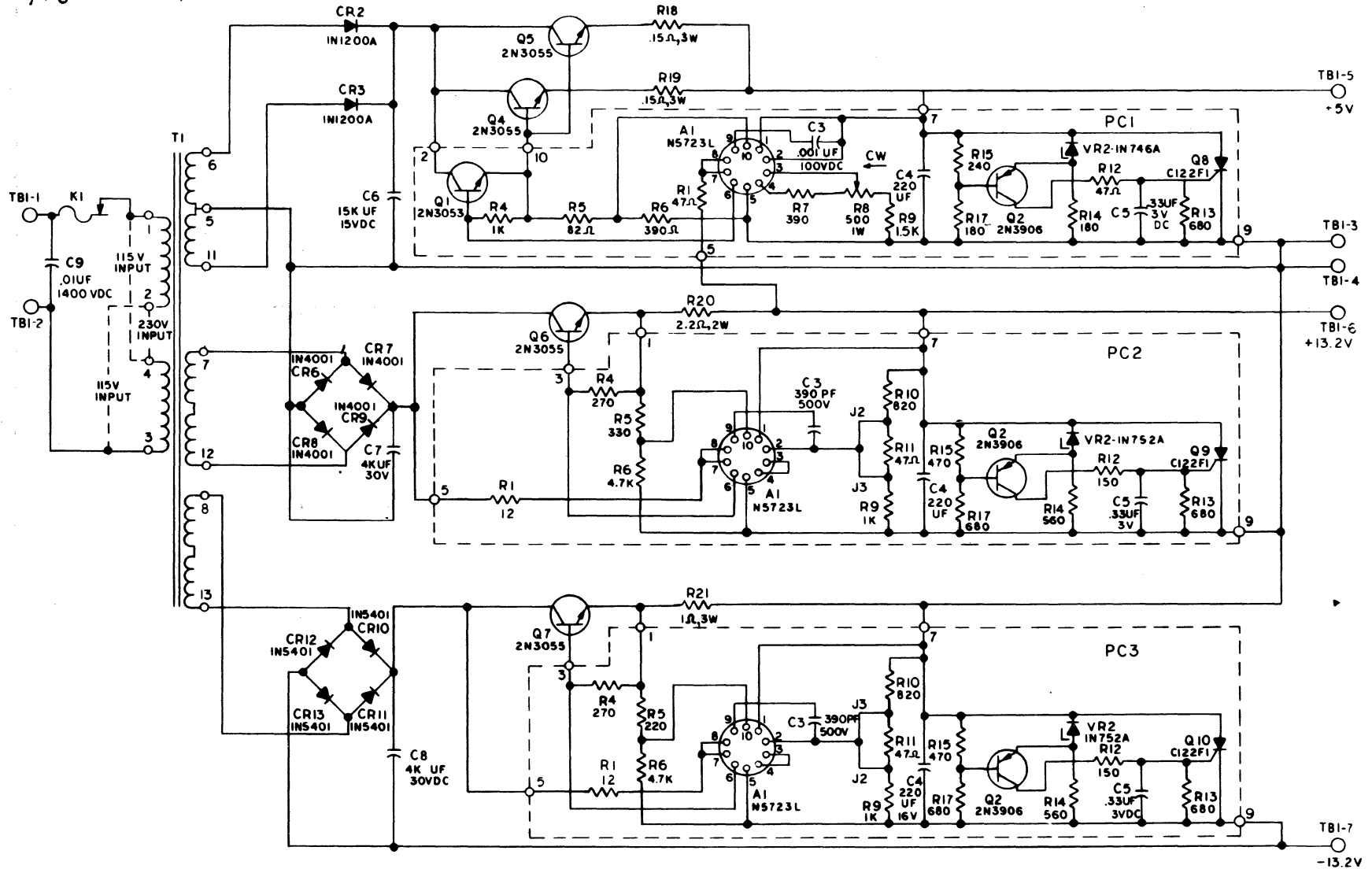
POWER SUPPLY TBI CABLE HOOK-UP

Fig. 7-7



# SCHEMATIC DIAGRAM, POWER SUPPLY, 285-Q04

Fig. 7-8



NOTE  
UNLESS OTHERWISE SPECIFIED  
RESISTORS ARE 1/4 W, 5%



**BILL OF MATERIAL**

**MATRIX**

**ADDS** Applied Digital Data System Inc.  
 100 Marcus Blvd. Hauppauge, New York

7-32

DRAWN BY	R.MEDINA	11-9-77	TITLE <b>POWER SUPPLY ASSEMBLY</b>								
CHECKED BY			REV.	SHEET 2 OF 2	DWG. NO.	504-077					
APPROVED BY							00	01			

120V

240V

ITEM	ADDS P/N	QTY.	DESCRIPTION	REF.DES.					
1	285-00400		POWER SUPPLY		1	1			
2	504-22000		FAN HARNESS ASS'Y.		1	1			
3	618-4230XXX		WIRE BLK. 18 GA. UL1430		1	1			
4	600-00700		PRIMARY WIRING 120V		1	-			
5	600-00800		PRIMARY WIRING 240V		-	1			




7-34

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	502-725	1	CHASSIS		
2	500-035	2	BRACKET-P.C. BOARD		
3	500-036	1	BRACKET-P.C. BOARD		
4	500-037	1	BRACKET RECTIFIER		
5	360-202	2	HEAT SINK - T03	BALL BROS. 1-015-5033	
6	360-318	3	TERMINAL STRIP	CINCH-JONES 52A	
7	360-319	4	TERMINAL STRIP	CINCH-JONES 52	
8	360-320	3	CAPACITOR CLAMP	SPRAGUE 4586-97A	
9	360-321	1	TERMINAL BLOCK	CINCH-JONES 7-140Y	TB1-1
10	350-019	1	TRANSFORMER	PWR. PAC 414-000-20	T1
11	360-322	2	RIGHT ANGLE BKT'S	H.H. SMITH 1446	
12	360-323	6	FIBER STANDOFF	H.H. SMITH 8886	
13	140-087	1	ELECT. CAP 15K uf, 15 VDC	SPRAGUE 36DX153G015AB2	C6
14	140-088	2	ELECT. CAP 4K uf, 30 VDC	SPRAGUE 36DX402G030AA2	C7, C8
15	191-006	2	RECTIFIER-STUD MOUNT	INT. RECT. CORP. 1N1200A	CR2, CR3
16	190-029	4	RECTIFIER-AXIAL LEAD	PWR. COMP. 1N4001	CR6 thru CR9
17	190-034	4	RECTIFIER-AXIAL LEAD	PWR. COMP. 1N5401	CR10 thru CR13
18	360-311	1	THERMOSTAT	KLIXON 20700	K1
19	330-010	4	TRANSISTORS-T03	MOTOROLA 2N3055	Q4 thru Q7
20	140-115	1	CAPACITOR-AC .01 uf, 1400 VDC	DIELECTRON ULR1400DC	C9
21	330-030	3	SCR	G.E. C122F1	Q8 thru Q10
22	309-003	2	RESISTOR W.W. .15ohm 3W	CLAROSTAT CC3L	R18, R19
23	308-011	1	RESISTOR W.W. 2.2 ohm 2W	IRC BWH	R20
24	309-004	1	RESISTOR W.W. 1.0 ohm 3W	CLAROSTAT CC3L	R21
25	360-324	1	MARKING STRIP-VOLTAGE DESIGNATION	H.H. SMITH 8886	
26					

PREPARED	I.C. Serra	11/3/73	TITLE MAIN CHASSIS - POWER SUPPLY		<b>ADDS</b> Applied Digital Data System, Inc. Hauppauge, New York
CHECKED			DWG. NO. 502-725	REV. A	
APPROVED			SHEET 2 OF 5		

————— BILL OF MATERIAL —————

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	360-110	1	PRINTED CIRCUIT BOARD, +5 V	ADDS	PC-1
2	140-117	1	CAPACITOR .001 uf 100VDC	SPRAGUE 225	C3
3	140-137	1	CAPACITOR 220 uf 16VDC	RAYREX RADY 220 PY01605	C4
4	140-138	1	CAPACITOR .33 uf 3VDC	DIELECTRON RT3	C5
5	302-110	2	RESISTOR 47 ohm 1/4 W + 5%	ALLEN BRADLEY EB	R1, R12
6	302-011	1	RESISTOR 1K ohm 1/4W + 5%	ALLEN BRADLEY EB	R4
7	302-117	1	RESISTOR 82 ohm 1/4W + 5%	ALLEN BRADLEY EB	R5
8	302-049	2	RESISTOR 390 ohm 1/4W + 5%	ALLEN BRADLEY EB	R6, R7
9					
10	302-030	1	RESISTOR 680 ohm 1/4W + 5%	ALLEN BRADLEY EB	R13
11	302-046	2	RESISTOR 180 ohm 1/4 W + 5%	ALLEN BRADLEY EB	R14, R17
12					
13	302-005	1	RESISTOR 240 ohm 1/4 W	R-OHM R-25	R15
14					
15	302-019	1	RESISTOR 1.5K ohm 1/4W	R-OHM R-25	R9
16	313-027	1	POT 500 ohm 1 W	AMPHENOL 6034P-501-7310	R8
17	330-018	1	TRANSISTOR T0-5	RCA 2N3053	Q1
18	330-005	1	TRANSISTOR T0-92	NATIONAL 2N3906	Q2
19	190-002	1	ZENER DIODE	MOTOROLA 1N746A	VR2
20	360-316	1	REGULATOR	SIGNETICS N5723L	A1
21	360-317	1	T0-5 HEAT SINK	WAKEFIELD 296-1-AB	

PREPARED	I.C. Serra	11/3/73	TITLE		
CHECKED			CONSUL POWER SUPPLY		
APPROVED			DWG. NO.	REV.	
			360-110	A	SHEET 3 OF 5

Applied Digital Data System, Inc.  
Hauppauge, New York

————— BILL OF MATERIAL —————

7-35

7-36

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	360-132	1	PRINTED CIRCUIT BOARD, +13.2 V	ADDS	PC-2
2	140-136	1	CAPACITOR 390 pf 500V	DIELECTRON X5F	C-3
3	140-137	1	CAPACITOR 220 uf 16V	RAYREX RADY 220PY01605	C-4
4	140-138	1	CAPACITOR .33 uf 3 Volt	DIELECTRON RT3	C5
5	302-067	1	RESISTOR 270 ohm 1/4 W + 5%	ALLEN BRADLEY EB	R4
6	302-110	1	RESISTOR 47 ohm 1/4 W + 5%	ALLEN BRADLEY EB	R11
7	302-039	1	RESISTOR 150 ohm 1/4 W + 5%	ALLEN BRADLEY EB	R12
8	302-030	2	RESISTOR 680 ohm 1/4 W + 5%	ALLEN BRADLEY EB	R13, R17
9	302-047	1	RESISTOR 560 ohm 1/4 W + 5%	ALLEN BRADLEY EB	R14
10	302-021	1	RESISTOR 4.7K ohm 1/4 W + 5%	ALLEN BRADLEY EB	R6
11	302-0 1	1	RESISTOR 3.3 ohm 1/4 W	R-OHM R-25	R5
12	302-011	1	RESISTOR 1.K ohm 1/4 W	R-OHM R-25	R9
13	302-007	1	RESISTOR 470 ohm 1/4 W	R-OHM R-25	R15
14					
15	302-010	1	RESISTOR 820 ohm 1/4 W	R-OHM R-25	R10
16	190-001	1	ZENER DIODE	MOTOROLA 1N752A	VR2
17	360-316	1	REGULATOR	SIGNETICS N5723L	A1
18	330-005	1	TRANSISTOR T0-92	NATIONAL 2N3906	Q2
19	302-116	1	RESISTOR 12 OHM, 1/4 W, ± 5%		R1

PREPARED	I.C. SERDA	11/3/73	TITLE		CONSUL-POWER SUPPLY		<b>ADDS</b> Applied Digital Data System, Inc. Hauppauge, New York
CHECKED			DWG. NO.	360-132	REV.	A	
APPROVED					SHEET	4 OF 5	

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	360-115	1	PRINTED CIRCUIT BOARD -13.2 V	ADDS	PC-3
2	140-136	1	CAPACITOR 390 pf, 500VDC	DIELECTRON X5F	C3
3	140-137	1	CAPACITOR 220 uf, 16 VDC	RAYREX-RADY 220PY01605	C4
4	140-138	1	CAPACITOR .33 uf, 30 VDC	DIELECTRON RT3	C5
5	302-067	1	RESISTOR 270 ohm $\frac{1}{4}$ W $\pm$ 5%	ALLEN BRADLEY EB	R4
6	302-021	1	RESISTOR 4.7K ohm $\frac{1}{4}$ W $\pm$ 5%	ALLEN BRADLEY EB	R6
7	302-110	1	RESISTOR 47 ohm $\frac{1}{4}$ W $\pm$ 5%	ALLEN BRADLEY EB	R11
8	302-039	1	RESISTOR 150 ohm $\frac{1}{4}$ W $\pm$ 5%	ALLEN BRADLEY EB	R12
9	302-030	2	RESISTOR 680 ohm $\frac{1}{4}$ W $\pm$ 5%	ALLEN BRADLEY EB	R13, R17
10	302-047	1	RESISTOR 560 ohm $\frac{1}{4}$ W $\pm$ 5%	ALLEN BRADLEY EB	R14
11	302-004	1	RESISTOR 220 ohm $\frac{1}{4}$ W	R-OHM R-25	R5
12	302-011	1	RESISTOR 1K ohm $\frac{1}{4}$ W	R-OHM R-25	R9
13	302-010	1	RESISTOR 820 ohm $\frac{1}{4}$ W	R-OHM R-25	R10
14	302-007	1	RESISTOR 470 ohm $\frac{1}{4}$ W	R-OHM R-25	R15
15					
16	330-005	1	TRANSISTOR T0-92	NATIONAL 2N3906	Q2
17	190-001	1	ZENER DIODE	MOTOROLA 1N752A	VR2
18	360-316	1	REGULATOR	SIGNETIC N5723L	A1
19	302-116	1	RESISTOR 12 OHM, $\frac{1}{4}$ W, $\pm$ 5%		R1

PREPARED	I.C. Serra	11/3/73	TITLE	CONSUL POWER SUPPLY		<b>ADDS</b>	Applied Digital Data System, Inc. Hauppauge, New York	
CHECKED			DWG. NO.	360-115	REV. A			SHEET 5 OF 5
APPROVED								

7-57

BILL OF MATERIAL

MATRIX

**ADD S** Applied Digital Data System Inc.  
100 Marcus Blvd. Hauppauge, New York

7-38

DRAWN BY **R. MEDINA** **11-9-77**  
 CHECKED BY  
 APPROVED BY

TITLE **FAN HARNESS - MRD 380**  
 REV. **A** SHEET **2 OF 2** DWG. NO. **504-22000**

ITEM	ADD S P/N	QTY.	DESCRIPTION	REF. DES.
------	-----------	------	-------------	-----------

1	170-03600	1	4 POSITION MOLEX	
2	170-05400	2	CONTACT MALE	
3	614-623X0XXX	1	WIRE (BLK) 22 GA.	
4	614-623X9XXX	1	WIRE (WHT) 22 GA.	

## TV MONITOR SUBASSEMBLY

## GENERAL DESCRIPTION

The TV monitor is a solid-state unit intended for use in industrial and commercial installations where reliability and high quality video reproduction are desired.

The monitor subassembly including the power supply can be removed from your terminal by removing the four mounting screws, disconnecting the 14 pin dip connector using the plastic strap to extract the connector, disconnecting the Sonalert Molex type connector on the rear panel P.C. board and disconnecting the 10 pin, 6 pin, and 3 pin Molex type connectors on the power supply P.C. board. Then remove the green ground wire by loosening the Phillips head screw and pulling the lug out. Note that recentering the picture may be necessary when installing a new monitor (see page 8-8). Once the TV monitor is out of the terminal the power supply may be removed by removing the two mounting screws and unsnapping the P.C. board from the two plastic standoffs.

## SPECIFICATIONS

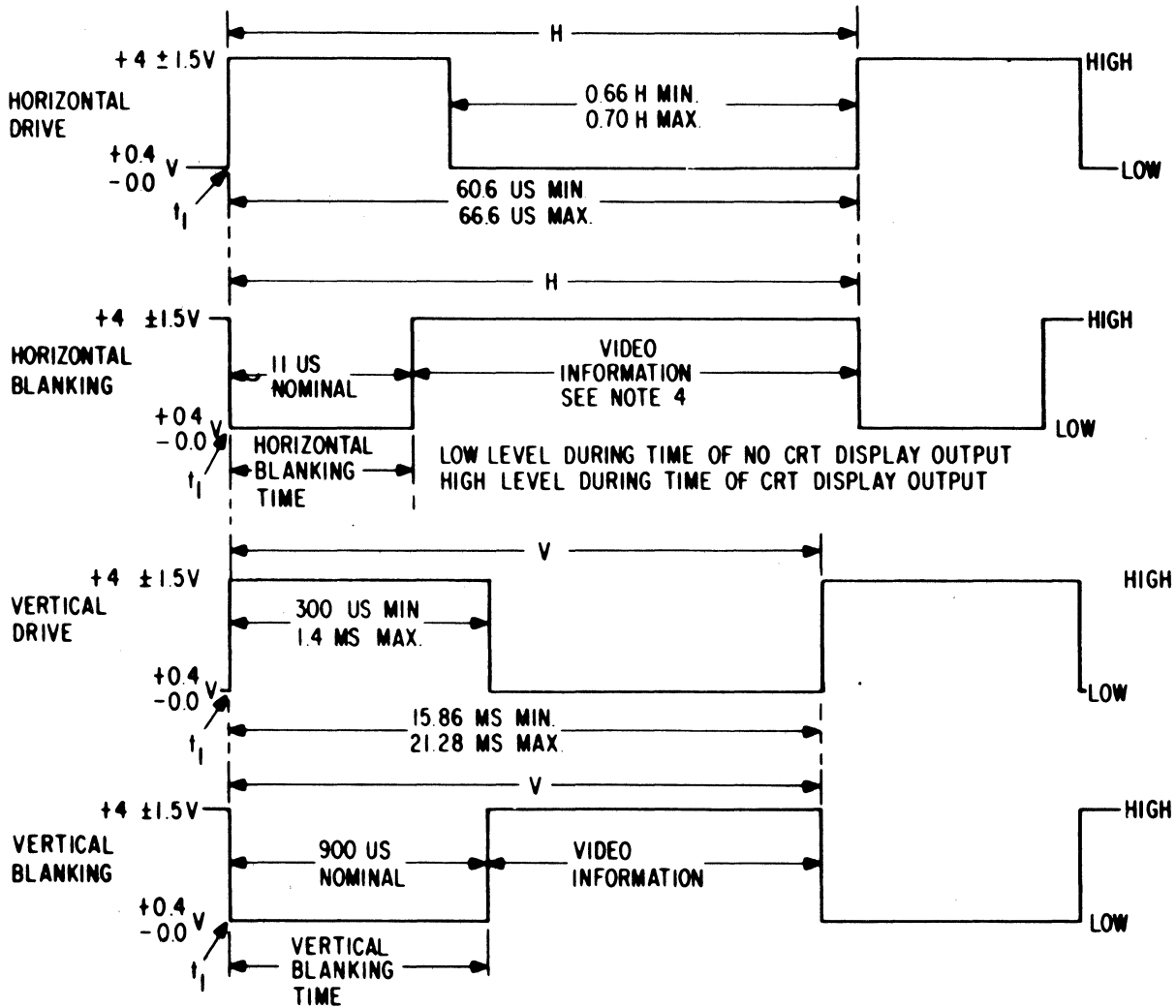
Input Data Specifications

	Video	Vertical Drive Signal	Horizontal Drive Signal
Input Connector	(Necessary Accessory-Available) Printed circuit board card edge connector- Viking #2VK10S/1-2 or Amphenol #225-21031-101		
Pulse Rate or Width	Pulse Width: 100 nsec or greater	Pulse Rate: 50 to 60 pulses per second	Pulse Rate: 15,000 to 16,500 pulses per sec
Amplitude	$+0.4$ Low + Zero $-0.0$ volts High + $4 \pm 1.5$ volts		
Signal Rise & Fall Times (10% to 90% amplitude)	Less than 20 nsec	Less than 100 nsec	Less than 50 nsec
Input Signal Format	See Figure 8-1		



# SYNCHRONIZATION AND BLANKING SIGNALS

Fig 8-1



## NOTES

1. The leading edges of Drive and Blanking waveforms must start at time  $t_1$ . Nominal Blanking times should be observed.
2.  $H$  = time from start of one line to start of next line.
3.  $V$  = time from start of one field to start of next field.
4. Video pulse width should be equal to or greater than 100 nsec.

## Display Specifications

### 1. Cathode Ray Tube

Nominal Diagonal Measurement: 12 inches

Phosphor: P4

\*Resolution (TV Lines): at center - 900 at 40 fL  
at corner - 800 at 40 fL

\*Resolution is measured in accordance with EIA RS-375, except Burst Modulation (or Depth of Modulation) is adjusted for 100 percent.

### 2. Geometric Distortion

The perimeter of a full field of characters shall approach an ideal rectangle to within +1.5% of the rectangle height.

## Power Requirements

Input Connector: Receptacle, Molex #03-06-1041 supplied with unit. Mating plug is Molex #03-06-2041.

Input Voltage: +13.2 VDC

Input Power: 24 Watts (nominal)

Output Voltages: +12v, Kv, DC

## Environmental Specifications

### 1. Temperature

Operating Range: 5°C to 55°C  
Storage Range: -40°C to 65°C

### 2. Humidity

5 to 80 percent R.H. (noncondensing)

### 3. Altitude

Operating Range: Up to 10,000 feet

## X-Ray Radiation

These units comply with DHEW Rules-42-CFR-Part 78.

## Controls

### 1. External Controls

- (a) Contrast, 500 ohm potentiometer carbon composition  $\geq 1/4$  Watt.
- (b) Brightness, 100 kilohm potentiometer  $\geq 1/4$  Watt.

### 2. Internal Set Up Controls

- (a) Height
- (b) Vertical Linearity
- (c) Vertical Hold
- (d) Focus
- (e) Width

## THEORY OF OPERATION

Fold out the monitor schematic drawing, Figure 8-2, before proceeding with the theory of operations. Figure 8-2 is located at the end of this section.

### Video Amplifier

The video amplifier consists of Q101 and its associated circuitry.

The incoming video signal is applied to the monitor through the contrast control through R109 to the base of transistor Q101.

Transistor Q101, operating as a class B amplifier, and its components, comprise the video output driver with a gain of about 17.

The negative going signal at the collector of Q101 is DC-coupled to the cathode of the CRT. The class B biasing of the video driver allows a larger video output signal to modulate the CRT's cathode and results in a maximum available contrast ratio.

### Vertical Deflection

Transistor Q102 is a programmable unijunction transistor, and together with its external circuitry, forms a relaxation oscillator operating at the vertical rate. Resistor R115, variable resistor R116 and capacitors C105 and C106 form an RC network providing proper timing.

R117 and R118 control the voltage at which the diode (anode-to-anode gate) becomes forward biased. This feature "programs" the firing of Q102 and prevents the unijunction from controlling this parameter.

The vertical oscillator is synchronized externally to the vertical interval from the vertical drive pulse at R113.

The sawtooth voltage at the anode of Q102 is directly coupled to the base of Q103. Q103 is a driver amplifier and has two transistors wired as a Darlington pair; their input and output leads exit as a three-terminal device. This device exhibits a high input impedance to Q1-2, and thereby maintains excellent impedance isolation between Q102 and Q104. The sawtooth waveform output at Q103 is coupled through R122, the vertical linearity control R121, and on to C106 where the waveform is shaped into a parabola. This parabolic waveform is then added to the oscillator's waveform and changes its slope.

Q103 supplies base current through R123 and R124 to the vertical output transistor, Q104. Height control R124 varies the amplitude of the sawtooth voltage present at the base of Q104 and, therefore, varies the size of the vertical raster on the CRT.

The vertical output stage, Q104, uses a power transistor which operates as a class A amplifier. C107 is a DC-blocking capacitor which allows only AC voltages to produce yoke current. L1 is a relative high impedance compared to the yoke inductance. During retrace time, a large positive pulse is developed by L1 which reverses the current through the yoke and moves the beam from the bottom of the screen to the top. Resistor R126 prevents oscillations by providing damping across the vertical deflection coils.

### Horizontal Deflection

To obtain a signal appropriate for driving Q106, the horizontal output transistor, a driver stage consisting of Q105 and T101, is used. A positive going pulse is coupled through R127 to the base of Q105.

The driver stage is either cut off or driven into saturation by the base signal. The output signal appears as a rectangular waveform and is transformer-coupled to the base of the horizontal output stage. The polarity of the voltage at the secondary of the driver transformer is chosen such that Q106 is cut off when Q105 conducts and vice versa.

During conduction of the driver transistor, energy is stored in the coupling transformer. The voltage at the secondary is then positive and keeps Q106 cut off. As soon as the primary current

of T101 is interrupted due to the base signal driving Q105 into cutoff, the secondary voltage changes polarity. Q106 starts conducting, and its base current flows. This gradually decreases at a rate determined by the transformer inductance and circuit resistance.

Q106 acts as a switch which is turned on or off by the rectangular waveform on the base. When Q106 is turned on, the supply voltage plus the charge on C113 causes yoke current to increase in a linear manner and moves the beam from near the center of the screen to the right side. At this time, the transistor is turned off by a positive voltage on its base which causes the output circuit to oscillate. A high reactive voltage in the form of a half cycle negative voltage pulse is developed by the yoke's inductance and the primary of T2. The peak magnetic energy which was stored in the yoke during scan time is then transferred to C109 and the yoke's distributed capacity. During this cycle, the beam is returned to the center of the screen.

The distributed capacity now discharges into the yoke and induces a current in a direction opposite to the current of the previous part of the cycle. The magnetic field thus created around the yoke moves the scanning beam to the left of the screen.

After slightly more than half a cycle, the voltage across C109 biases the damper diode CR103 into conduction and prevents the flyback pulse from oscillating. The magnetic energy that was stored in the yoke from the discharge of the distributed capacity is released to provide sweep for the first half of scan and to charge C113 through the rectifying action of the damper diode. The beam is then at the center of the screen. The cycle will repeat as soon as the base voltage of Q106 becomes negative.

L101 is an adjustable width control placed in series with the horizontal deflection coils. The variable inductive reactance allows a greater or lesser amount of the deflection current to flow through the horizontal yoke and, therefore, varies the width of the horizontal scan.

The negative flyback pulse developed during horizontal retrace time is rectified by CR104 and filtered by C110. This produces approximately "D" VDC which is coupled through the brightness control to the cathode of the CRT (V1).

This same pulse is transformer coupled to the secondary of transformer T2 where it is rectified by CR2, CR106, and CR105 to produce rectified voltages of approximately 12kV, "C" VDC, and "B" VDC respectively. 12kV is the anode voltage for the CRT, and "C" VDC serves as the source voltage for grids No. 2 and 4 (focus grid) of the CRT. The "B" VDC potential is the supply voltage for the video output amplifier, Q101.

## ADJUSTMENTS

There is a slight interaction among the vertical frequency, height, and linearity controls. A change in the height of the picture may affect linearity.

1. Set the vertical frequency control, R116, near the mechanical center of its rotation.
2. Adjust the vertical height control, R124, for desired height.
3. Adjust the vertical linearity control, R121, for best vertical linearity.
4. Remove the vertical drive signal from the unit. Alternatively, use a short jumper lead, and short the vertical drive input terminal of the printed circuit card edge connector to ground.
5. Readjust the vertical frequency control, R116, until the picture rolls up slowly.
6. Restore vertical drive to the monitor.
7. Recheck height and linearity.

### Horizontal Adjustments

Raster width is affected by a combination of the low volume supply, width coil L101, and the horizontal linearity sleeve located on the neck of the CRT beneath the yoke.

1. Adjust the horizontal width coil, L101, for the desired width.
2. Adjust the linearity sleeve under the yoke to obtain the best linearity. Although this adjustment will affect the raster width, it should not be used solely for that purpose. The placement of the linearity sleeve should be optimized for the best linearity.
3. Readjust L101 for proper width.
4. Observe final horizontal linearity and width, and touch up either adjustment if needed.

### Focus Adjustment

The focus control, R107, provides an adjustment for maintaining best overall display focus.

## Centering

If the raster is not properly centered, it may be repositioned by rotating the ring magnets behind the deflection yoke.

The ring magnets should not be used to offset the raster from its nominal center position because it would degrade the resolution of the display.

If the picture is tilted, rotate the entire yoke.

## TROUBLESHOOTING AND MAINTENANCE

### List of Symptoms and Remedy

<u>Symptom</u>	<u>Possible Remedy</u>
Screen is dark	<p>If an external monitor is available, plug it into the video connector at the rear of the terminal. If no picture appears on that monitor check the P.C. cards in the terminal bucket which generate horizontal and vertical drive (the VGA and VGB in the 800/700 series; the VG/GT card in the 580/380 series)</p> <p>If external monitor shows picture (or if you cannot check P.C. cards in terminal) proceed to the step below.</p> <p>Check "A" bus Q106, Q105, CR2</p>
Loss of Video	CR105, Q101
Power consumption is too high	Check horizontal drive waveform; check proper placement of horizontal linearity sleeve; Q106, Q105

### Supplementary Drawings

The following four pages show

A schematic drawing

Interconnecting cabling

Important waveforms in the monitor subassembly

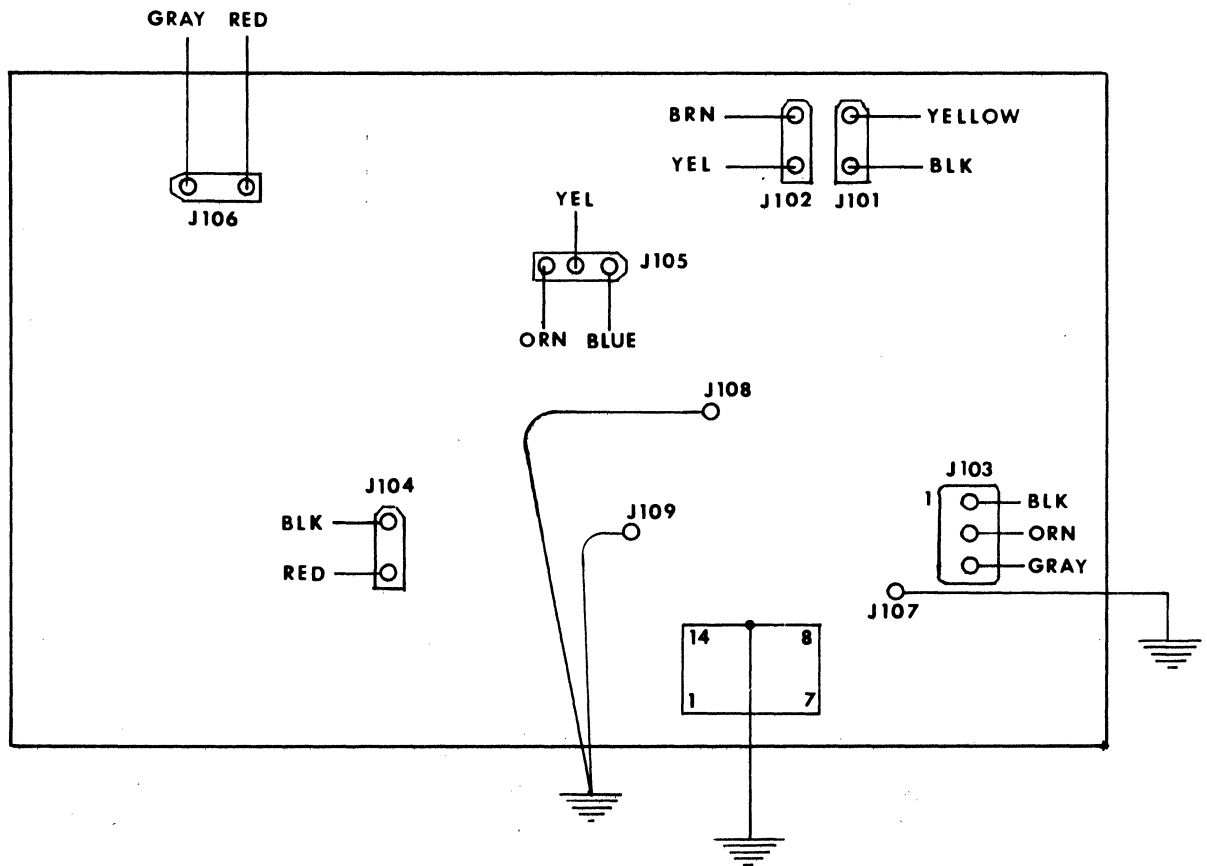
Location of Circuit Board Components





# INTERCONNECTIONS VIDEO BOARD

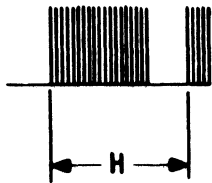
Fig. 8-3



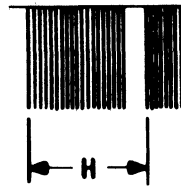
**VOLTAGE WAVEFORMS**

**Fig. 8-4**

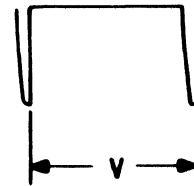
**WAVEFORMS**



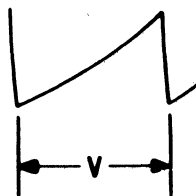
**Q101-B**  
**2.5V P-P**



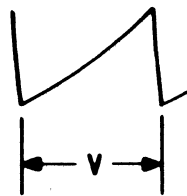
**VI-CATHODE**  
**20V P-P**



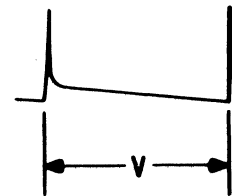
**CR101-ANODE**  
**3V P-P**



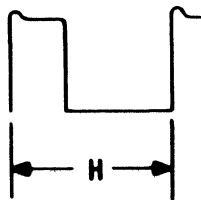
**Q103-B**  
**4.5V P-P**



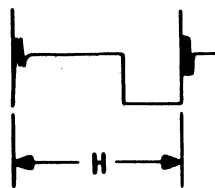
**Q104-B**  
**1.2V P-P**



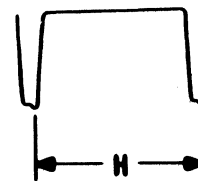
**Q104-C**  
**45V P-P**



**Q105-B**  
**3V P-P**



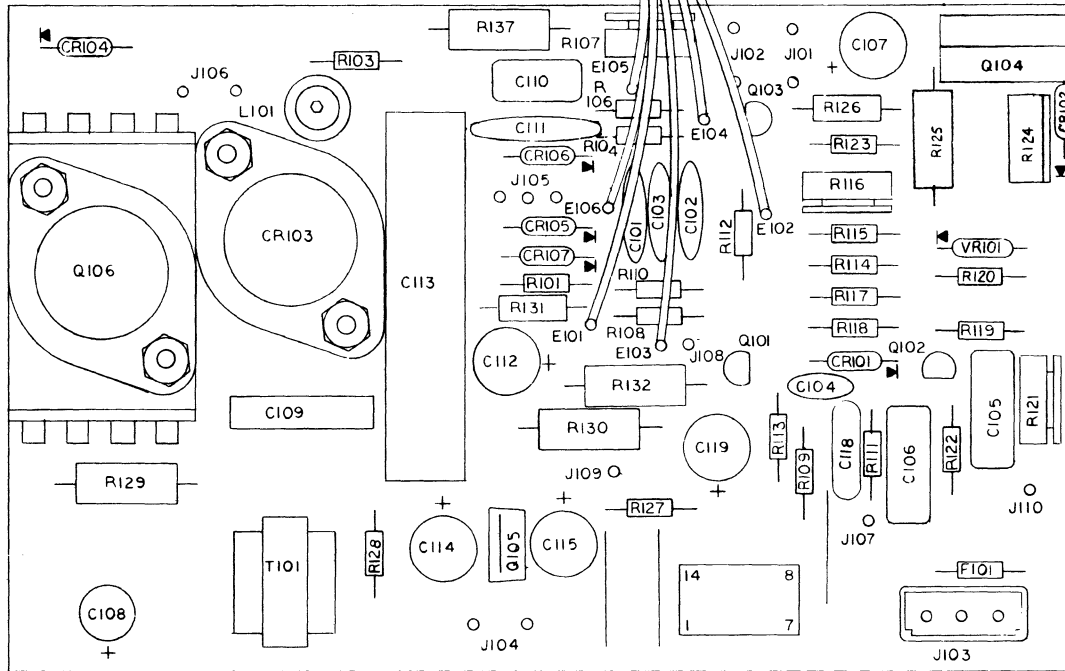
**Q105-C**  
**30V P-P**



**Q106-C**  
**170V P-P**

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REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	REL. FOR PROD, 051-056	4-13-77	FB
B	ECO 050-40196		
C	ECO-050-40184		
D	ECO 050-40199, 40201		
E	ECO 050; 40297, 40275 #40363	9-6-77	FB
F	ECO 050-40409 SK	2-22-78	J.H.
G	ECO 050-40561 & 40546 M	4-11-78	J.H.
H	Added Note 1, ECO 050-40848 RZ	10-17-78	DD RD



NOTE: 1. USE MICA INSULATOR ADDS P/N 360-30900 WHEN MOUNTING CR103. DO NOT USE SILICONE GREASE

8-13/8-14

TOLERANCES			<b>ADDS</b> Applied Digital Data System, Inc. Hauppauge, New York		
1/64	005	1	FRAC	DEC	ANG
DO NOT SCALE DWG					
DRAWN			DATE		
CHECKED			DATE		
ENGR			DATE		
APPROVED			DWG NO		
NEXT ASSY			USED ON		
QTY			REV		
			SCALE 2:1		
			SHEET 1 of 4		
			REV H		

TV MONITOR BILL OF MATERIAL

A complete B.O.M. of the TV Monitor is given in the following pages.

Note that for certain parts, ADDS is the sole supplier. However those parts which are "off the shelf" have a standard manufacturer's part number listed.

91-8

## BILL OF MATERIAL

## MATRIX

**ADDS** Applied Digital Data System Inc.  
100 Marcus Blvd. Hauppauge, New York

DRAWN BY		R. BISESTI		4/11/77		TITLE		ASSEMBLY VIDEO CARD		ADDS STD.	SYS. 70/50								
CHECKED BY		P. BISESTI		9/16/77		REV.		SHEET 2 OF 4								DWG. NO.		129-174	
APPROVED BY																			
ITEM	ADDS P/N	QTY.	DESCRIPTION			REF. DES.			G	A									
1	123-174		VIDEO CARD PCB						1	1									
2	140-16800		CAPACITOR 6.8UF, 25V, ELECTROLYTIC			C117			1	1									
3	140-12100		CAPACITOR .01UF, 1000V CERAMIC			C101-103			3	3									
4	140-11200		CAPACITOR .001UF, 1000V CERAMIC			C104			1	1									
5	140-09800		CAPACITOR .47UF ±10%			C105,106			2	2									
6	140-14700		CAPACITOR 470UF @10V ELECTROLYTIC			C107			1	1									
7	140-12400		CAPACITOR 100UF, 6.3V ELECTROLYTIC			C108			1	1									
8	140-12500		CAPACITOR .022UF ±10%, 400V			C109			1	1									
9	140-10600		CAPACITOR .047UF ±10%, 200V			C110			1	1									
10	140-12600		CAPACITOR .02UF ±20%, 1000V			C111			1	1									
11	140-14900		CAPACITOR 47UF, 50V, ±10%			C112			1	1									
12	140-16300		CAPACITOR 15UF, ±10%, 50V			C113			1	1									
13	140-09900		CAPACITOR 220UF, 25V, ±10%			C114			1	1									
14	140-15100		CAPACITOR 47UF, 25V, 10%			C115			1	1									
15	140-12900		CAPACITOR 820PF, ±5%, 500V			C118			1	1									
16	140-10200		CAPACITOR 22UF, 50V, ±10%			C119			1	1									
17	302-12000		RESISTOR 62K, 1/4W ±5%			R103			1	1									
18	302-05800		RESISTOR 2.7K, 1/4W ±5%			R101, R128			2	2									
19	302-12100		RESISTOR 82K, 1/4W ±5%			R115			1	1									
20	302-02600		RESISTOR 100K, 1/4W ±5%			R104, 106, 119			3	3									
21	313-02300		POT 2.5M, 1/8W, ±20%			R107			1	1									
22	302-10000		RESISTOR 3 OHM, 1/4W, ±5%			R108			1	1									
23	302-11000		RESISTOR 47 OHM, 1/4W, ±5%			R109, 111			2	2									
24	302-01000		RESISTOR 820 OHM, 1/4W, ±5%			R110			1	1									
25	302-00700		RESISTOR 470 OHM, 1/4W, ±5%			R113, 127			2	2									

**BILL OF MATERIAL**

**MATRIX**

**ADDS** Applied Digital Data System Inc.  
100 Marcus Blvd. Hauppauge, New York

DRAWN BY R. RISESTI 4/11/77				TITLE ASSEMBLY VIDEO CARD		ADDS STO	SYS TO/50				
CHECKED BY RBISESTI 9/16/77		REV.		SHEET 3 OF 4							
APPROVED BY						00	01				
ITEM	ADDS P/N	QTY.	DESCRIPTION	REF. DES.	G	A					
26	302-03900		RESISTOR 150 OHM, 1/4W, ±5%	R123, R120	1	2					
27	313-02400		POT 100K, 1/8W, ±20%	R116	1	1					
28	302-02100		RESISTOR 4.7K OHM, 1/4W, ±5%	R117,122	2	1					
29	302-04200		RESISTOR 8.2K OHM, 1/4W, ±5%	R118	1	-					
30	302-04700		RESISTOR 560 OHM, 1/4W, ±5%	R120	1	-					
31	313-02500		POT 10K OHM, 1/8W, ±20%	R121	1	1					
32	313-02600		POT 100 OHM, 1/8W, ±20%	R124	1	1					
33	308-00700		RESISTOR 3.3 OHM, 2W, ±10%	R125	1	1					
34	304-02400		RESISTOR 390 OHM, 1/2W, ±5%	R126	1	1					
35	302-00300		RESISTOR 100 OHM, 1/4W, ±5%	R114	1	1					
36	302-00400		RESISTOR 220 OHM, 1/4W, ±5%	R112	1	1					
37											
38	308-00800		RESISTOR 1.2 OHM, 2W, ±10%	R130,129	2	2					
39	304-02600		RESISTOR 3.3K OHM, 1/2W, ±5%	R131	1	1					
40	308-00500		RESISTOR 82 OHM, 2W, ±10%	R132	1	1					
41	306-01500		RESISTOR 68K OHM, 1W, ±5%	R137	1	1					
42											
43	190-02000		DIODE 1N3605	CR101,102	2	2					
44	190-01700		DIODE 1N4785	CR103	1	1					
45	190-04400		DIODE 1N4005	CR104,105,106,107	4	4					
46											
47	330-00200		TRANSISTOR 2N3904	Q101	1	1					
48	330-01200		TRANSISTOR 2N6027	Q102	1	1					
49	330-01300		TRANSISTOR MPSA14	Q103	1	1					
50	330-01400		TRANSISTOR MJE3055	Q104	1	1					

81-8

## BILL OF MATERIAL

## MATRIX

**ADDS** Applied Digital Data System Inc.  
100 Marcus Blvd. Hauppauge, New York

DRAWN BY R. BISESTI 4/11/77 TITLE ASSEMBLY VIDEO CARD						ADDS STD	S45 70/50				
CHECKED BY		REV.		SHEET 4 OF 4	DWG. NO. 129-174						
APPROVED BY						00	01				
ITEM	ADDS P/N	QTY.	DESCRIPTION	REF. DES.	6	A					
51	330-01500		TRANSISTORS MPS-U05	Q105	1	1					
52	330-02600		TRANSISTORS 2N6031	Q106	1	1					
53											
54	225-01800		FUSE 2A @120V PICO FUSE	F101	1	1					
55	360-24800		COIL WIDTH	L101	1	1					
56	350-01000		TRANSFORMER HORIZONTAL DRIVE	T101	1	1					
57	190-01900		VOLTAGE REG. 1N758	VR101	1	1					
58	175-00400		14 PIN DIP SOCKET		1	1					
59	170-15900		3 POS MATE-N-LOK HEADER	J103	1	1					
60	360-34500		HEAT SINK TO3		1	1					
61	170-17500		CRT CONN. SOCKET HARNESS ASS'Y		1	1					
62	170-17300		MOLEX PINS	J101,102,J104-110	15	15					
63	610-58XXXXXX		JUMPER WIRE		3	3					
64	700-138003		6-32 X 1/2 P/H PHILIPS SCREW		4	4					
65	800-713040		6-32 KEPS NUT		4	4					
66	360-39700		SILICON GREASE		AR	AR					
67	360-03200		TIEWRAP		3	3					
68	190-04800		VOLTAGE REGULATOR VR56	VR102	-	1					
69	360-40028		HEAT SINK (TO-127)		1	1					
70	140-16900		CAPACITOR .005UF, 100V CER	C104	-	1					
71	302-01100		RESISTOR 1K OHM, 1/4W, ±5%	R117	-	1					
72	302-06600		RESISTOR 1.8 K OHM, 1/4W, ±5%	R118	-	1					

## KEYBOARD SUBASSEMBLY

The keyboard is a subassembly which may be simply removed from a 520/580 for repair or replacement.

## KEYBOARD MECHANICAL PACKAGE

Figure 9-1 is a drawing of the 520 keyboard keycap array.  
Figure 9-2 is a drawing of the 580 keyboard keycap array.

Note that the keyboard can be removed from a 520/580 by disconnecting the edge connector at the rear of the keyboard and removing four Phillips head screws at the corners of the keyboard which hold it on the front panel in the terminal. Field maintenance usually consists of removing a defective keyboard and replacing it with a spare unit.

Individual key modules can be replaced by desoldering two connections on the bottom P.C. board, pulling the bad module up through the hole in the mounting frame, and then resoldering the new module to the P.C. board connections. Integrated circuits are located on the keyboard P.C. board such that they can be replaced without further board disassembly.

## KEYBOARD ELECTRONICS

Refer to the schematics and assemblies in this section starting at page 9-5. The heart of the keyboard is an LSI chip that serves the purpose of both an encoder and a ROM. This chip is U1. It is a complete keyboard interface system capable of providing quad mode 90 key keyboard encoding.

A dynamic scanning technique is utilized to detect and pinpoint keyswitch activity on the keyboard. The chip uses two ring counters. A 9-bit X counter monitors the rows  $X_0$  through  $X_8$  of the switch matrix while the 10 columns  $Y_0$  through  $Y_9$  are monitored by a 10-bit Y counter. Since there are  $9 \times 10 = 90$  possible counter states, ninety data switches may be defined by their X-Y coordinates.

Every scan time (90-bit times), all keys are interrogated in turn to determine their status. Each particular key is interrogated every 90-bits or once each keyboard scan cycle. This is implemented by employing the X counter as drivers to drive each row of the switch matrix in turn. The Y counter enables the sensing of each column of the switch matrix. Therefore, if a switch is closed it will be detected if its row is driven and its column is sensed. This corresponds to the particular X-Y time (one of 90 time slots in the scan) defining the closed switch. A key detect pulse at the X-Y time in question is issued, and this is used to define the status of that particular key.



Once it is determined which key is closed, this information is taken and used to provide a coded bit pattern for that key. In addition to scanning the key switch matrix, the X and Y counters are used to scan the contents of a Read Only Memory (ROM) which contains the bit pattern for each key switch. For example, when switch X<sub>1</sub>, Y<sub>1</sub> (letter I) is being interrogated (at X<sub>1</sub>-Y<sub>1</sub> time), the counters are addressing the ROM location which contains the code for switch X<sub>1</sub>-Y<sub>1</sub>. If the key is closed, a key detect pulse is issued. At this time, the ROM contents are strobed into latches which then hold the code pattern D<sub>1</sub> through D<sub>10</sub> for the key X<sub>1</sub> Y<sub>1</sub> (i.e., letter I).

For each keyswitch it is possible to have four modes. These are determined by the status of the SHIFT and CONTROL keys which are inputs to U<sub>1</sub>. There are four possible code patterns for each key as determined by the mode switches.

The code pattern, along with the strobe out of U<sub>1</sub>, is inverted by U<sub>4</sub>, U<sub>5</sub> and U<sub>6</sub> to provide the signals B<sub>1</sub> through B<sub>10</sub> that are active low. The coding information for coded keys is given starting on page 9-5.

All the unencoded keys are generated to the right of the U<sub>1</sub>. These function keys are debounced from a free running oscillator, U<sub>2</sub> triggering the quad latch, U<sub>3</sub>. When a function key is depressed, the corresponding interface pin goes from GND to +5 Volts, and remains at +5 Volts until the key is released.

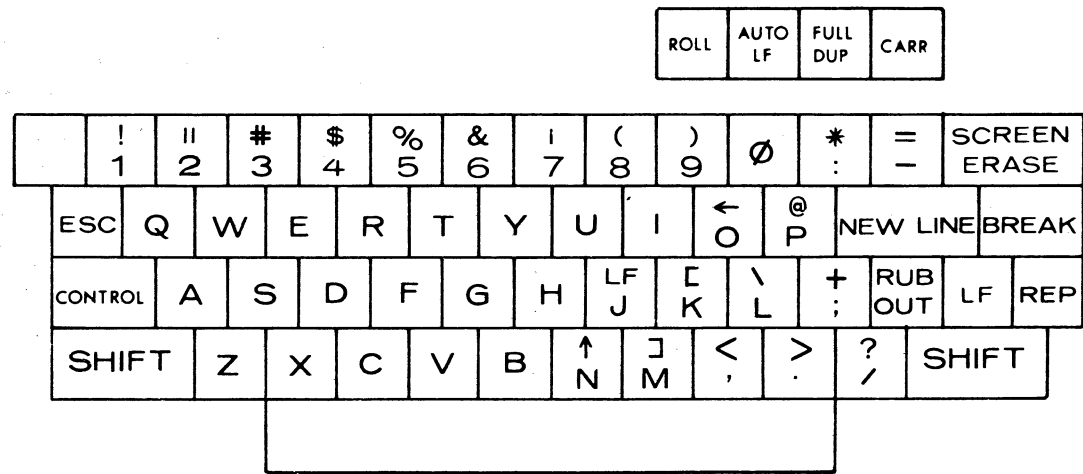
#### KEYBOARD INTERFACE SIGNALS

The amplatch connector on the keyboard is a 26-pin connector. The signals and their pins are listed below.

P-1 GND	P-9 B4	P-17 RPT
P-2 BK1	P-10 B5/8	P-18 CARR
P-3 GND	P-11 B6	P-19 GND
P-4 KBSTB	P-12 B7/9	P-20 -13V
P-5 GND	P-13 B10	P-21 -13V
P-6 B1	P-14 ROLL	P-22 GND
P-7 B2	P-15 AUTO LF	P-23 +5V
P-8 B3	P-16 FULL DUP	P-24 +5V
		P-25 +5V
		P-26 +5V

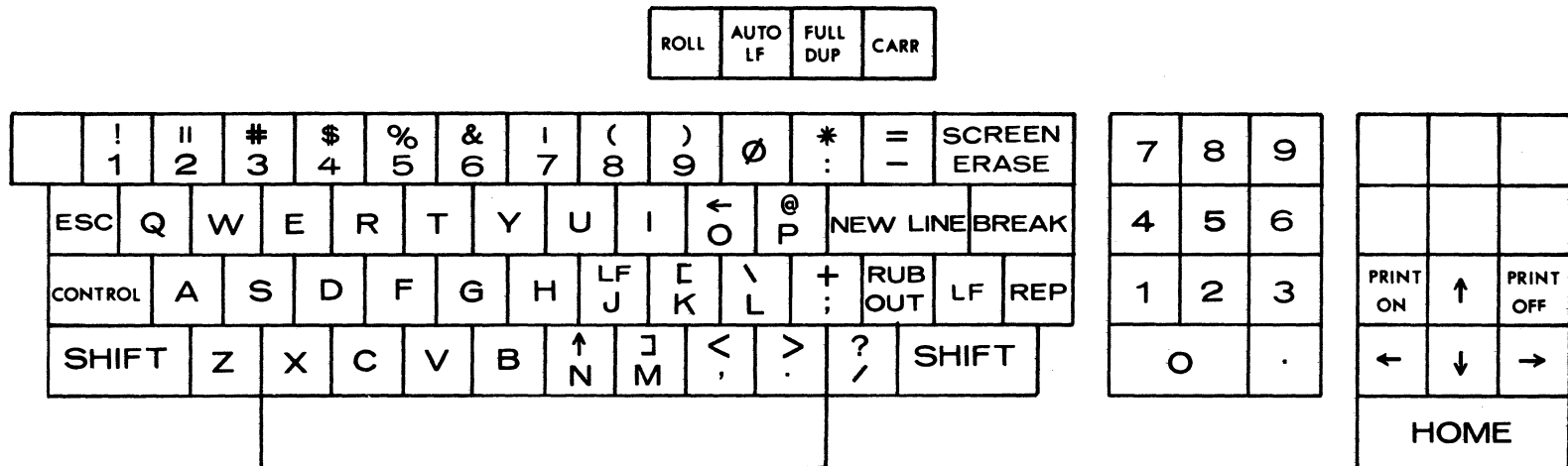
# CONSUL 520 KEYBOARD LAYOUT

Fig. 9-1



CONSUL 580 KEYBOARD LAYOUT

Fig. 9-2



ASCII CODES GENERATED BY THE 580 ROM KEYBOARD  
AND APPLICABLE DETACHABLE 380 KEYBOARD

The tables showing all possible codes which can be generated from the keyboard are arranged as follows:

1. One table for each row in the keyboard (there are five such rows)
2. Within each table, codes appear in the same sequence that keys occur in the row, reading from left to right.

ASCII Codes Generated in Row 1 of Keyboard

KEYTOP LEGEND	UNSHIFTED MODE		SHIFTED MODE		CONTROL MODE		SHIFT & CONTROL MODE	
	BITS 765 4321		BITS 765 4321		BITS 765 4321		BITS 765 4321	
Blank	000	0011	111	0000	110	0000	000	0011
1 !	011	0001	010	0001	011	0001	010	0001
2 "	011	0010	010	0010	011	0010	010	0010
3 #	011	0011	010	0011	011	0011	010	0011
4 \$	011	0100	010	0100	011	0100	010	0100
5 %	011	0101	010	0101	011	0101	010	0101
6 &	011	0110	010	0110	011	0110	010	0110
7 '	011	0111	010	0111	011	0111	010	0111
8 (	011	1000	010	1000	011	1000	010	1000
9 )	011	1001	010	1001	011	1001	010	1001
∅	011	0000	010	0000	111	0000	110	0000
: *	011	1010	010	1010	011	1010	010	1010
- =	010	1101	011	1101	110	1101	111	1101
SCREEN ERASE					000	1100		

TYPING ARRAY

7	011	0111	010	0111	011	0111	010	0111
8	011	1000	010	1000	011	1000	010	1000
9	011	1001	010	1001	011	1001	010	1001

NUMERIC  
PAD

Blank	100	1000	110	1011	110	1111	100	1000
Blank	011	1000	001	1011	001	1111	011	1000
Blank	111	1000	101	1011	101	1111	111	1000

CONTROL  
ARRAY

ASCII Codes Generated in Row 2 of Keyboard

KEYTOP LEGEND	UNSHIFTED MODE		SHIFTED MODE		CONTROL MODE		SHIFT & CONTROL MODE	
	BITS 765 4321		BITS 765 4321		BITS 765 4321		BITS 765 4321	
ESC	001	1011	001	1011	001	1011	001	1011
Q	101	0001	111	0001	001	0001	001	0001
W	101	0111	111	0111	001	0111	001	0111
E	100	0101	110	0101	000	0101	000	0101
R	101	0010	111	0010	001	0010	001	0010
T	101	0100	111	0100	001	0100	001	0100
Y	101	1001	111	1001	001	1001	001	1001
U	101	0101	111	0101	001	0101	001	0101
I	100	1001	110	1001	000	1001	000	1001
O ←	100	1111	101	1111	000	1111	001	1111
P @	101	0000	100	0000	001	0000	000	0000
NEW LINE	000	1101	000	1101	000	1101	001	1101
BREAK	Function Output							

TYPING ARRAY

4	011	0100	010	0100	011	0100	010	0100
5	011	0101	010	0101	011	0101	010	0101
6	011	0110	010	0110	011	0110	010	0110

NUMERIC PAD

Blank	100	0100	011	1011	011	1100	100	0100
Blank	110	0100	111	1011	111	1100	110	0100
Blank	000	1100	101	1100	011	1111	000	1100

CONTROL ARRAY

ASCII Codes Generated in Row 3 of Keyboard

	UNSHIFTED MODE		SHIFTED MODE		CONTROL MODE		SHIFT & CONTROL MODE	
KEYTOP LEGEND	BITS 765 4321		BITS 765 4321		BITS 765 4321		BITS 765 4321	
CONTROL	Internal Function							
A	100	0001	110	0001	000	0001	000	0001
S	101	0011	111	0011	001	0011	001	0011
D	100	0100	110	0100	000	0100	000	0100
F	100	0110	110	0110	000	0110	000	0110
G	100	0111	110	0111	000	0111	000	0111
H	100	1000	110	1000	000	1000	000	1000
J LF	100	1010	110	1010	000	1010	000	1010
K [	100	1011	101	1011	000	1011	001	1011
L \	100	1100	101	1100	000	1100	001	1100
; +	011	1011	010	1011	111	1011	110	1011
RUBOUT	111	1111	111	1111	111	1111	111	1111
LINE FEED	000	1010	000	1010	000	1010	000	1010
REPEAT	Function Output							

TYPING ARRAY

1	011	0001	010	0001	011	0001	010	0001
2	011	0010	010	0010	011	0010	010	0010
3	011	0011	010	0011	011	0011	010	0011

NUMERIC ARRAY

PRINT ON	001	0010	000	0010	001	0010	000	0010
↑	001	1010	000	1010	001	1010	000	1010
PRINT OFF	001	0100	000	0100	001	0100	000	0100

CONTROL ARRAY

ASCII Codes Generated in Row 4 of Keyboard

KEYTOP LEGEND	UNSHIFTED MODE		SHIFTED MODE		CONTROL MODE		SHIFT & CONTROL MODE	
	BITS 765 4321		BITS 765 4321		BITS 765 4321		BITS 765 4321	
SHIFT	Internal Function							
Z	101	1010	111	1010	001	1010	001	1010
X	101	1000	111	1000	001	1000	001	1000
C	100	0011	110	0011	000	0011	000	0011
V	101	0110	111	0110	001	0110	001	0110
B	100	0010	110	0010	000	0010	000	0010
N ↑	100	1110	101	1110	000	1110	001	1110
M ]	100	1101	101	1101	000	1101	001	1101
, <	010	1100	011	1100	110	1100	111	1100
. >	010	1110	011	1110	110	1110	111	1110
/ ?	010	1111	011	1111	110	1111	111	1111
SHIFT	Internal Function							

TYPING  
ARRAY

0	011	0000	010	0000	011	0000	010	0000
.	010	1110	011	1110	010	1110	011	1110

NUMERIC  
PAD

←	001	0101	000	0101	001	0101	000	0101
↓	000	1010	001	1010	000	1010	001	1010
→	000	0110	001	0110	000	0110	001	0110

CONTROL  
ARRAY

ASCII Codes Generated in Row 5 of Keyboard

SPACE	010	0000	011	0000	110	0000	111	0000
HOME	000	0001	001	0001	000	0001	001	0001



## ASCII CODES GENERATED BY THE 520 ROM KEYBOARD

The tables showing all possible codes which can be generated from the keyboard are arranged as follows:

1. One table for each row in the keyboard (there are five such rows)
2. Within each table, codes appear in the same sequence that keys occur in the row, reading from left to right.

ASCII Codes Generated in Row 1 of Keyboard

	UNSHIFTED MODE		SHIFTED MODE		CONTROL MODE		SHIFT & CONTROL MODE	
KEYTOP LEGEND	BITS 765 4321		BITS 765 4321		BITS 765 4321		BITS 765 4321	
Blank	000	0011	111	0000	110	0000	000	0011
1 !	011	0001	010	0001	011	0001	010	0001
2 "	011	0010	010	0010	011	0010	010	0010
3 #	011	0011	010	0011	011	0011	010	0011
4 \$	011	0100	010	0100	011	0100	010	0100
5 %	011	0101	010	0101	011	0101	010	0101
6 &	011	0110	010	0110	011	0110	010	0110
7 ' .	011	0111	010	0111	011	0111	010	0111
8 (	011	1000	010	1000	011	1000	010	1000
9 )	011	1001	010	1001	011	1001	010	1001
∅	011	0000	010	0000	111	0000	110	0000
: *	011	1010	010	1010	011	1010	010	1010
- =	010	1101	011	1101	110	1101	111	1101
SCREEN ERASE					000	1100		

TYPING ARRAY

ASCII Codes Generated in Row 2 of Keyboard

KEYTOP LEGEND	UNSHIFTED MODE		SHIFTED MODE		CONTROL MODE		SHIFT & CONTROL MODE	
	BITS 765 4321		BITS 765 4321		BITS 765 4321		BITS 765 4321	
ESC	001	1011	000	1011	001	1011	000	1011
Q	101	0001	111	0001	001	0001	011	0001
W	101	0111	111	0111	001	0111	011	0111
E	100	0101	110	0101	000	0101	010	0101
R	101	0010	111	0010	001	0010	011	0010
T	101	0100	111	0100	001	0100	011	0100
Y	101	1001	111	1001	001	1001	011	1001
U	101	0101	111	0101	001	0101	011	0101
I	100	1001	110	1001	000	1001	010	1001
O ←	100	1111	101	1111	000	1111	001	1111
P e	101	0000	100	0000	001	0000	000	0000
NEW LINE	000	1101	001	1101	000	1101	001	1101
BREAK	Function Output							

TYPING ARRAY

ASCII Codes Generated in Row 3 of Keyboard

	UNSHIFTED MODE		SHIFTED MODE		CONTROL MODE		SHIFT & CONTROL MODE	
KEYTOP LEGEND	BITS 765 4321		BITS 765 4321		BITS 765 4321		BITS 765 4321	
CONTROL	Internal Function							
A	100	0001	110	0001	000	0001	010	0001
S	101	0011	111	0011	001	0011	011	0011
D	100	0100	110	0100	000	0100	010	0100
F	100	0110	110	0110	000	0110	010	0110
G	100	0111	110	0111	000	0111	010	0111
H	100	1000	110	1000	000	1000	010	1000
J LF	100	1010	110	1010	000	1010	010	1010
K [	100	1011	101	1011	000	1011	001	1011
L \	100	1100	101	1100	000	1100	001	1100
; +	011	1011	010	1011	111	1011	110	1011
RUBOUT	111	1111	110	1111	011	1111	010	1111
LINE FEED	000	1010	001	1010	000	1010	001	1010
REPEAT	Function Output							

TYPING ARRAY

ASCII Codes Generated in Row 4 of Keyboard

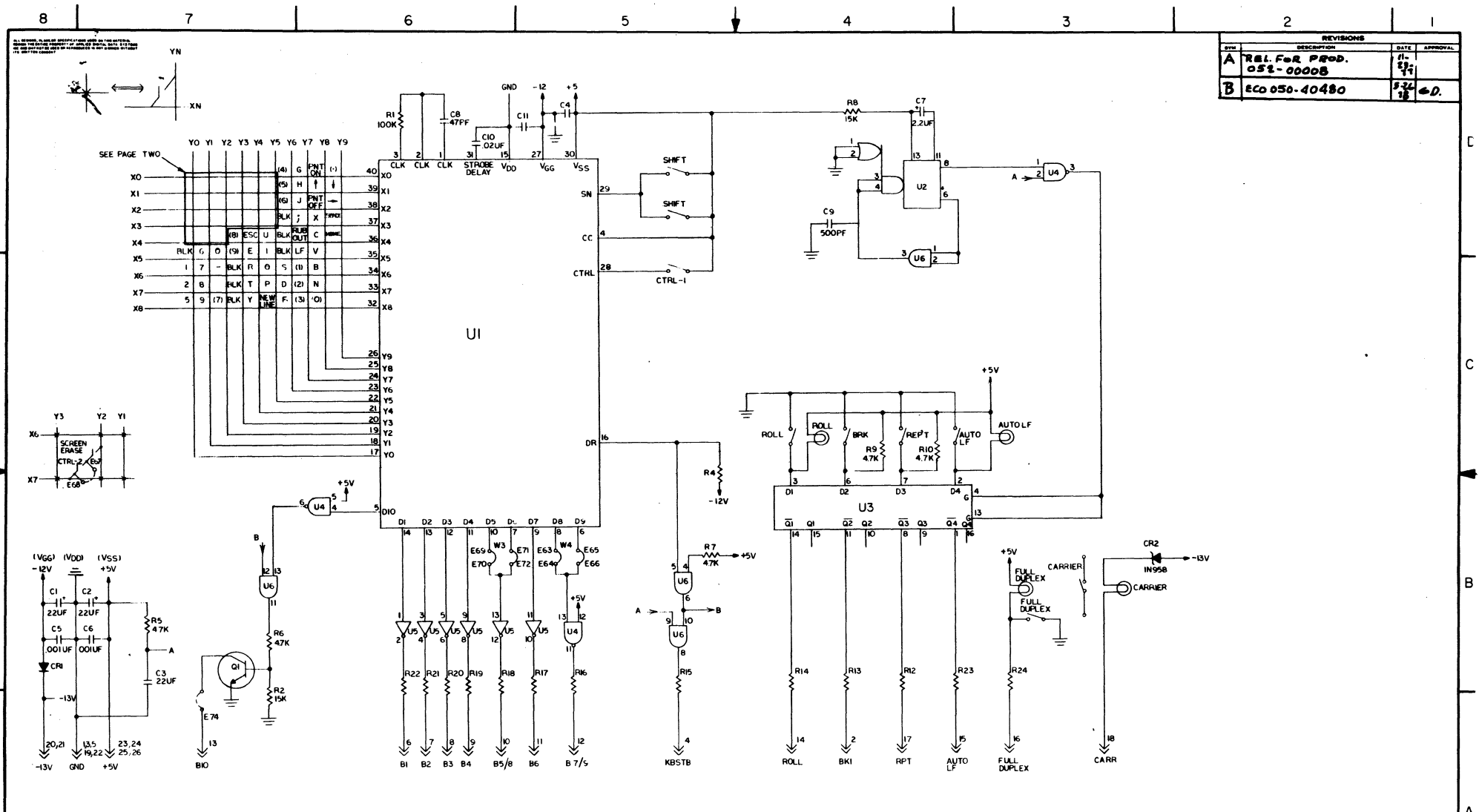
	UNSHIFTED MODE		SHIFTED MODE		CONTROL MODE		SHIFT & CONTROL MODE	
KEYTOP LEGEND	BITS 765 4321		BITS 765 4321		BITS 765 4321		BITS 765 4321	
SHIFT	Internal Function							
Z	101	1010	111	1010	001	1010	011	1010
X	101	1000	111	1000	001	1000	011	1000
C	100	0011	110	0011	000	0011	010	0011
V	101	0110	111	0110	001	0110	011	0110
B	100	0010	110	0010	000	0010	010	0010
N ↑	100	1110	101	1110	000	1110	001	1110
M ]	100	1101	101	1101	000	1101	001	1101
, <	010	1100	011	1100	110	1100	111	1100
. >	010	1110	011	1110	110	1110	111	1110
/ ?	010	1111	011	1111	110	1111	111	1111
SHIFT	Internal Function							

TYPING ARRAY

ASCII Codes Generated in Row 5 of Keyboard

SPACE	010	0000	011	0000	110	0000	111	0000
-------	-----	------	-----	------	-----	------	-----	------

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	REL FOR PROD. 052-0008	5-15-76	
B	Eco 050-40480	5-22-76	ED



NOTES:  
1. SIGNAL GROUND & CHASSIS GROUND TO BE SEPARATE

REF DES	REF TYPE
U1	035-0613
U2	9601
U3	7475
U4	7400
U5	7404
U6	7408
R12 R24	47 OHMS

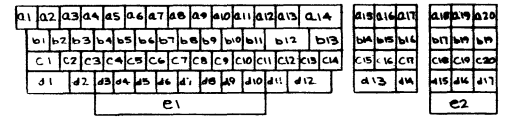
1/8" 200 5/16" 500 1" 1000 DO NOT SCALE DIMS REVISED 6-15-76 7-22-76	<b>ADDS</b> Applied Digital Data System, Inc. Basking Ridge, New York
CHEERY PN B80-29AB NEXT ADPT USED ON RTT	SCHEMATIC DIAGRAM KEYBOARD CONSUL 520 355-02900

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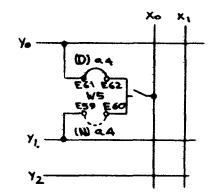
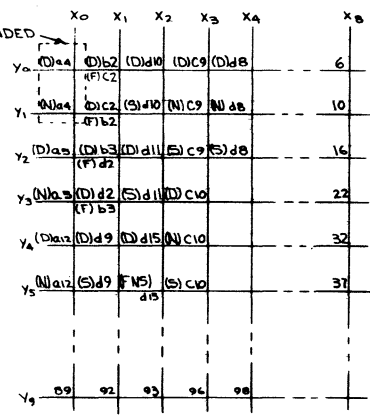
REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL

KEY LOCATION	KEY CAP LEGEND				MATRIX LOCATION		WIRE JUMPER POSITION		WIRE JUMPER NUMBERS
	DOMESTIC	FRENCH	DENMARK-NORWAY	SWEDEN-FINLAND	X <sub>M</sub>	Y <sub>M</sub>	FROM	TO	
Q4	3 #	3 #			0	0	E62	E61	W5
Q4			3 [	3 #	0	1	E60	E59	
A5	4 #	4 #			0	2	E42	E41	W6
A5			4 I		0	3	E40	E39	
Q12	: *	: *			0	4	E7	E8	W7
Q12			] *		0	5	E5	E6	
B2	Q		Q	Q	1	0	E51	E52	W8
B2		A			1	1	E53	E54	
C2	A		A	A	1	1	E47	F48	W9
C2		Q			1	0	E49	E50	
B3	W		W	W	1	2	E55	E56	W10
B3		Z			1	3	E57	E58	
D2	Z		Z	Z	1	3	E43	E44	W11
D2		W			1	2	E45	E46	
D9	> <	> <	> <		1	4	E32	E31	W12
D9				> A (J)	1	5	E30	E29	
D10	. >	. >	. >		2	0	E15	E16	W13
D10				. A (E)	2	1	E13	E14	
D11	/ ?	/ ?	/ ?		2	2	E11	E12	W14
D11				/ 8 (N)	2	3	E9	E10	
D15	← (MAX)				2	4	E1	E2	W15
D15				← (BS)	2	5	E3	E4	
C9	KE	KE			3	0	E28	E27	W16
C9			KE (#)		3	1	E26	E25	
C9				K <	3	2	E24	E23	
C10	L >	L >			3	3	E22	E21	W17
C10			L 8 (#)		3	4	E20	E19	
C10				L >	3	5	E18	E17	
D8	M J	M J			4	0	E38	E37	W18
D8			MA (:)		4	1	E36	E35	
D8				M ?	4	2	E34	E33	

KEY LOCATION



SEE EXTENDED VIEW



EXTENDED VIEW

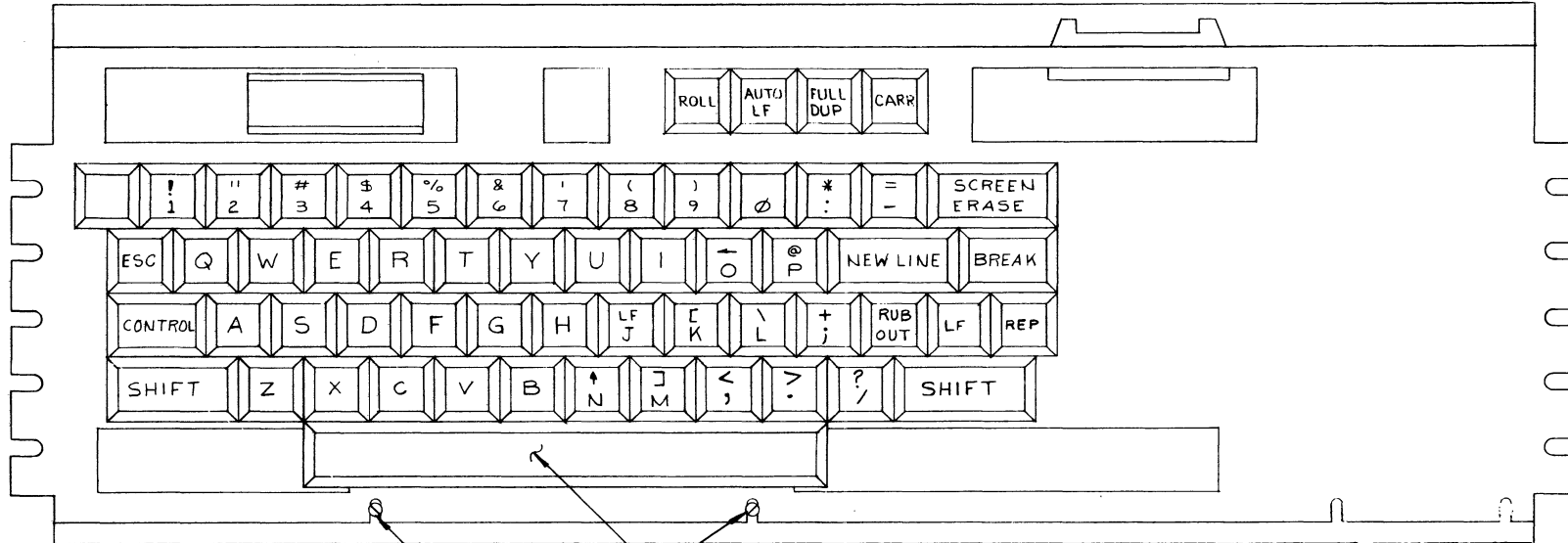
MATRIX

D = DOMESTIC  
 F = FRENCH  
 N = DENMARK-NORWAY  
 S = SWEDEN-FINLAND

TOLERANCES: 1/64 .005 1- FRAC DEC ANG DO NOT SCALE DWG		Applied Digital Data System, Inc. Haverhill, New York
DRAWN R. BISESTI	DATE 11-19-75	
CHECKED  ENGR  APPROVED  CHEERY PM BBO-29 AA CONS 580		SCHEMATIC DIAGRAM KEYBOARD
NEXT ASSY  USED ON  QTY	DWG NO 355-029	

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 REMAIN THE ENTIRE PROPERTY OF APPLIED DIGITAL DATA SYSTEMS  
 INC. AND MAY NOT BE USED OR REPRODUCED IN ANY MANNER WITHOUT  
 ITS WRITTEN CONSENT.

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	REL FOR PROD 052-00008	11-23-77	EB
B	REVISED & REDRAWN ECO 050-40510	2-22-78	



① SPACE BAR H'WARE  
 P/O ITEM 2 #3

②

③

TOLERANCES			<b>ADDS</b> Applied Digital Data System, Inc. Hauppauge, New York		
1/64	.005	1	FRAC	DEC	ANG
DO NOT SCALE DWG					
DRAWN J. MARTINO			DATE 2-22-78		
CHECKED			ENG R		
APPROVED			DWG NO 355-02900		
NEXT ASSY			USED ON		
QTY			SCALE C		
			SHEET 11		
			REV B		

D

C

B

A

9-17

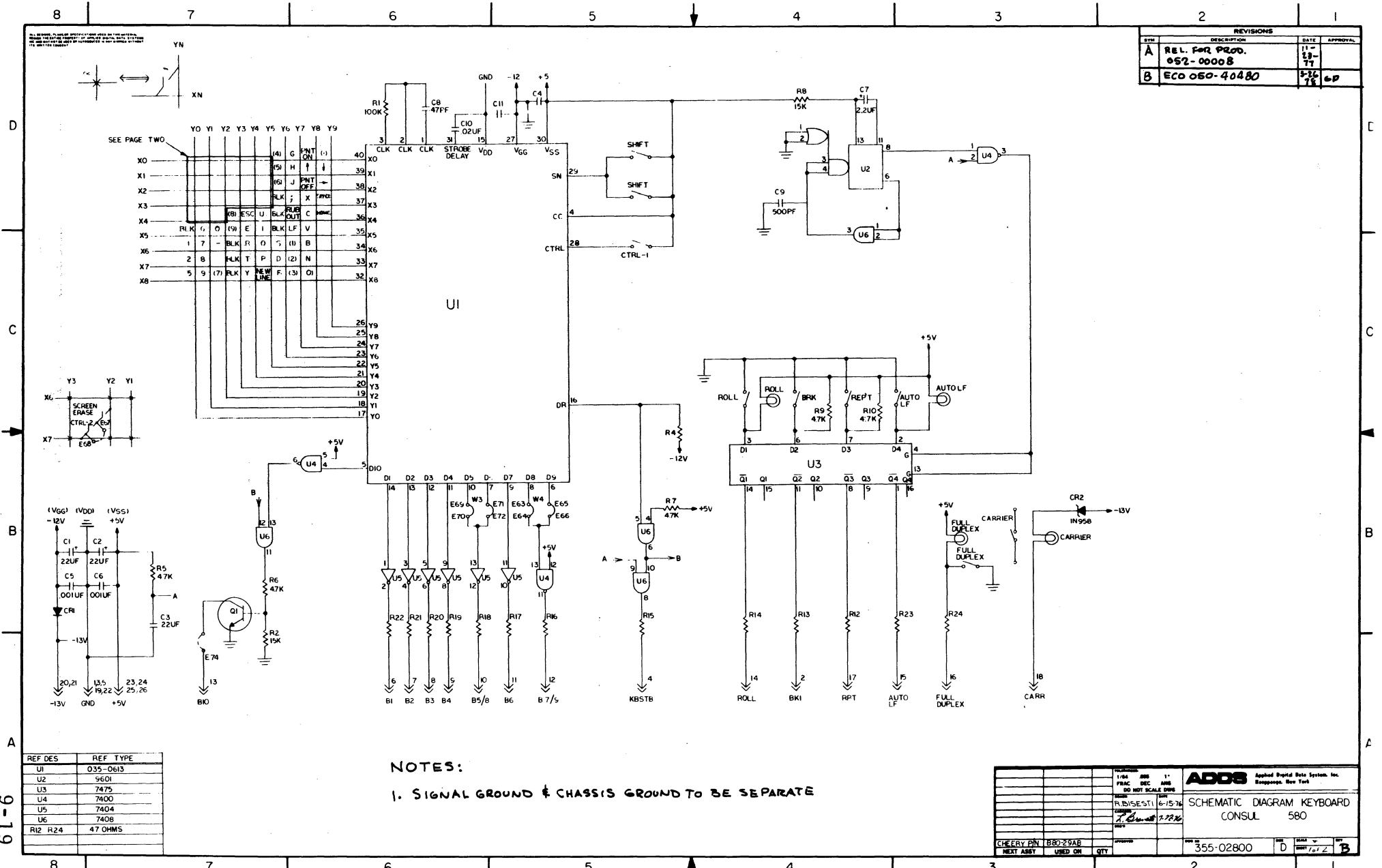
4 3 2 1

4 3 2 1





REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	REL. FOR PROD. 052-0008	11-19-77	
B	ECO 050-40480	3-26-78	ED



61-9

REF DES	REF TYPE
U1	035-0613
U2	5601
U3	7475
U4	7400
U5	7404
U6	7408
R12 R24	47 OHMS

NOTES:  
1. SIGNAL GROUND & CHASSIS GROUND TO BE SEPARATE

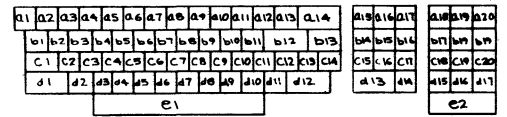
APPROVED		1/84	200	1"	<b>ADDS</b> Applied Digital Data System, Inc. Beverly Hills, New York
NEXT ASSY		FRAC	DEC	ANG	
CHEERY PN	B8029AB	R. B. SESTI 10-15-74			SCHEMATIC DIAGRAM KEYBOARD CONSUL 580
USED ON	QTY	T. B. SESTI 3-22-78			
		355-02800			D

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL

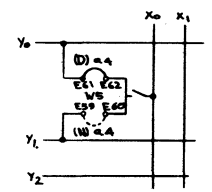
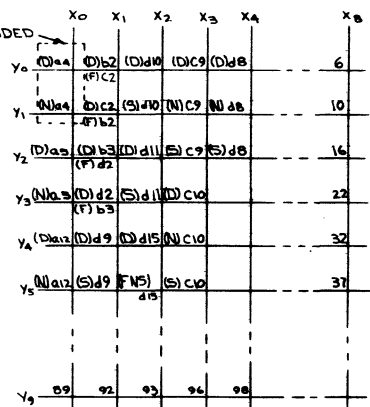
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KEY LOCATION	KEY CAP LEGEND				MATRIX LOCATION		WIRE JUMPER LOCATION		WIRE JUMPER NUMBERS
	DOMESTIC	FRENCH	DENMARK-NORWAY	SWEDEN-FINLAND	X <sub>M</sub>	Y <sub>M</sub>	FROM	TO	
Q4	3 #	3 #			0	0	E62	E61	W5
Q4			3 [		0	1	E60	E59	
Q5	4 #	4 #		4 #	0	2	E42	F41	W6
Q5			4 I		0	3	E40	E39	
Q12	: *	: *		: *	0	4	E7	E8	W7
Q12			1 *		0	5	E5	E6	
b2	Q		Q	Q	1	0	E51	E52	W8
b2		A			1	1	E53	E54	
C2	A		A	A	1	1	E47	F48	W9
C2		Q			1	0	E49	E50	
b3	W		W	W	1	2	E55	E56	W10
b3		Z			1	3	E57	E58	
d2	Z		Z	Z	1	3	E43	E44	W11
d2		W			1	2	E45	E46	
d9	> <	> <	> <		1	4	E32	E31	W12
d9				> A (J)	1	5	E30	E29	
d10	. >	. >	. >		2	0	E15	E16	W13
d10				. A (C)	2	1	E13	E14	
d11	/ ?	/ ?	/ ?		2	2	E11	E12	W14
d11				/ B (N)	2	3	E9	E10	
d15	← (MAX)				2	4	E1	E2	W15
d15				← (BS)	2	5	E3	E4	
C9	KE	KE			3	0	E28	E27	W16
C9			KA (H)		3	1	E26	E25	
C9				KA <	3	2	E24	E23	
C10	L <	L <			3	3	E22	E21	W17
C10			L > (S)		3	4	E20	E19	
C10				L >	3	5	E18	E17	
d8	MJ	MJ			4	0	E38	E37	W18
d8			MA (S)		4	1	E36	E35	
d8				M ?	4	2	E34	E33	

KEY LOCATION



SEE EXTENDED VIEW



EXTENDED VIEW

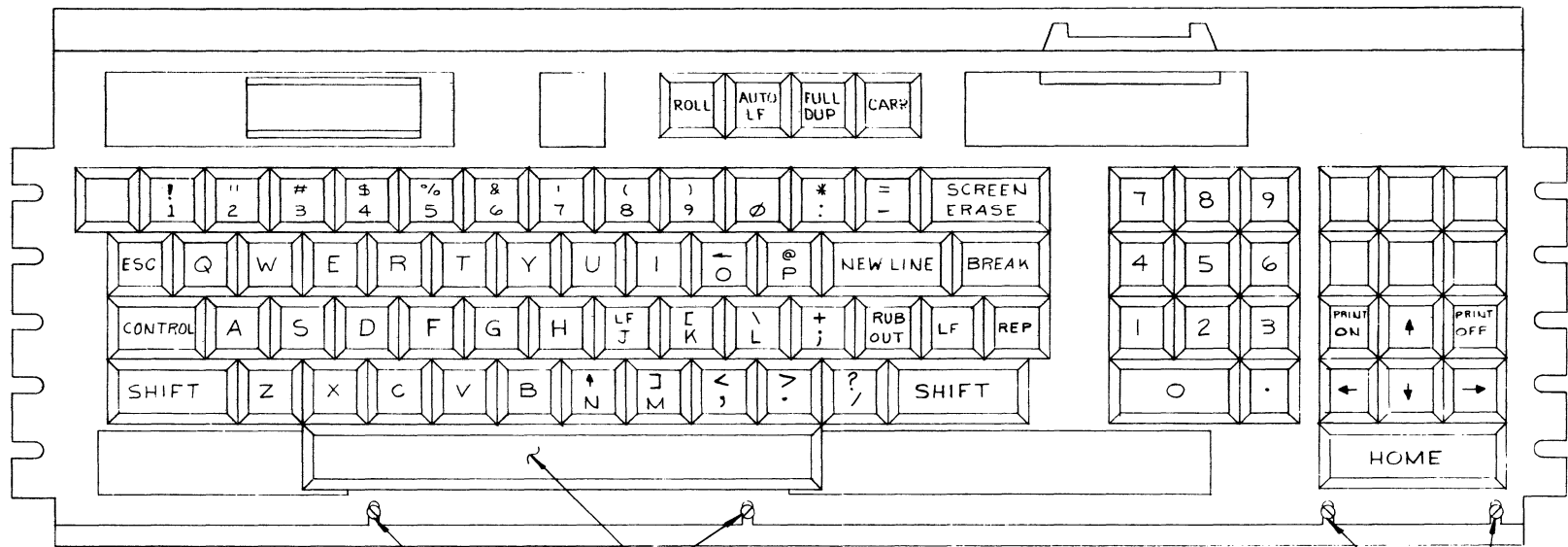
MATRIX

D = DOMESTIC  
 F = FRENCH  
 N = DENMARK-NORWAY  
 S = SWEDEN-FINLAND

TOLERANCES		<b>ADDS</b> Applied Digital Data System, Inc. Hopewagon, New York
1/64	.005 1°	
FRAC	DEC ANG	SCHEMATIC DIAGRAM KEYBOARD
DO NOT SCALE DWG		
DRN	DATE	DWG NO 355-028
R. BISESTI	11-19-75	
CHECKER		REV C
ENGR		
APPROVED		SHEET 2 OF 2
CHEERY PM BBO-20 AA CONSUL 580		
NEXT ASSY	USED ON	QTY

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 ITS WRITTEN CONSENT.

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	REL FOR PROD 052-0000B	11-23-77	ES
B	REVISED & REDRAWN ECO 050-40520	2-22-78	



1

SPACE BAR H'WARE  
P/O ITEM 2

2

HOME BAR H'WARE  
P/O ITEM 2

TOLERANCES			
FRAC	DEC	ANG	DO NOT SCALE DWG
1/64	005	1	
DRAWN: MAF 11/27/77			
CHECKED: [Signature]			
ENG: [Signature]			
APPROVED: [Signature]			
NEXT ASSY	USED ON	QTY	

**ADDS** Applied Digital Data System, Inc.  
 Hauppauge, New York

**ASSEMBLY 580  
 KEYBOARD**

DWG NO	355-02800	SIZE	SCALE	REV
SHEET	10	OF	12	B

D  
C  
B  
A  
9-21

D  
C  
B  
A

4 3 2 1

4 3 2 1





SECTION 10:

SCHMATIC AND ASSEMBLY DRAWINGS

This section includes the schematic and assembly drawings listed below:

FE/GT	135-079H	Schematic
	129-079L	Assembly

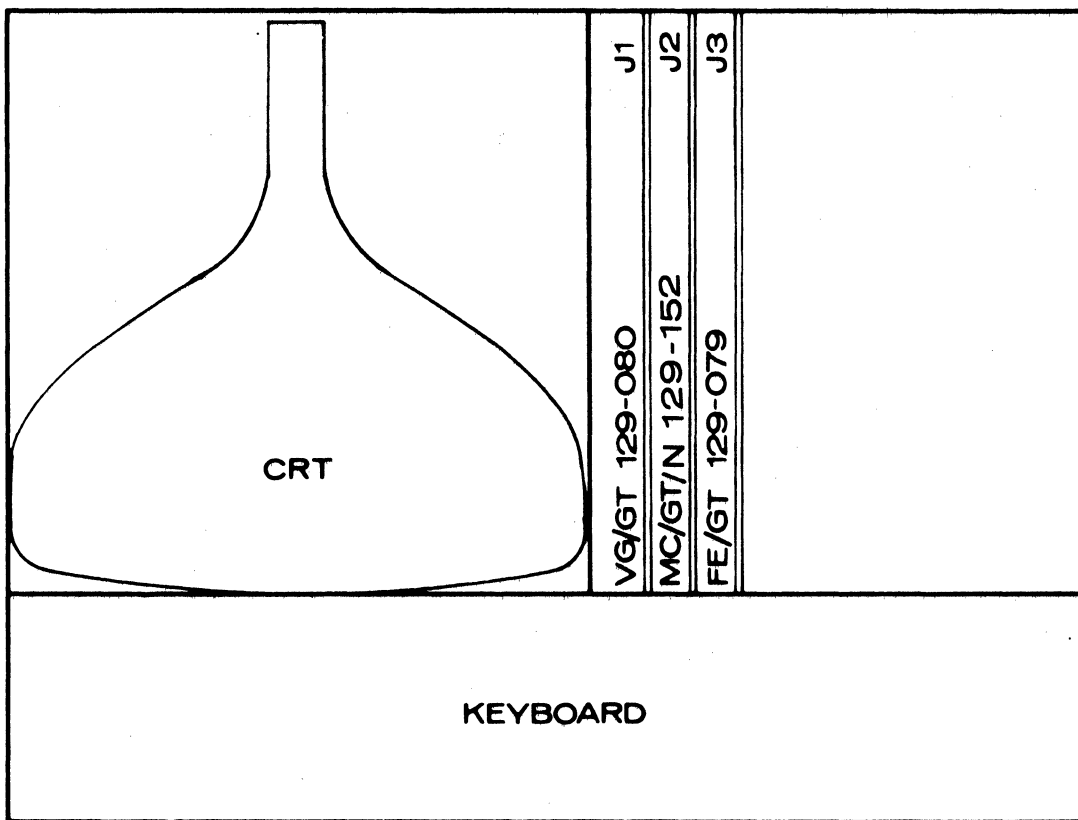
VG/GT	135-080C	Schematic
	129-080F	Assembly

MC/GT/N	135-152A	Schematic
	129-152C	Assembly

A card locator chart for the 580 is presented on page 10-2 showing P.C. board placement in the card cage.

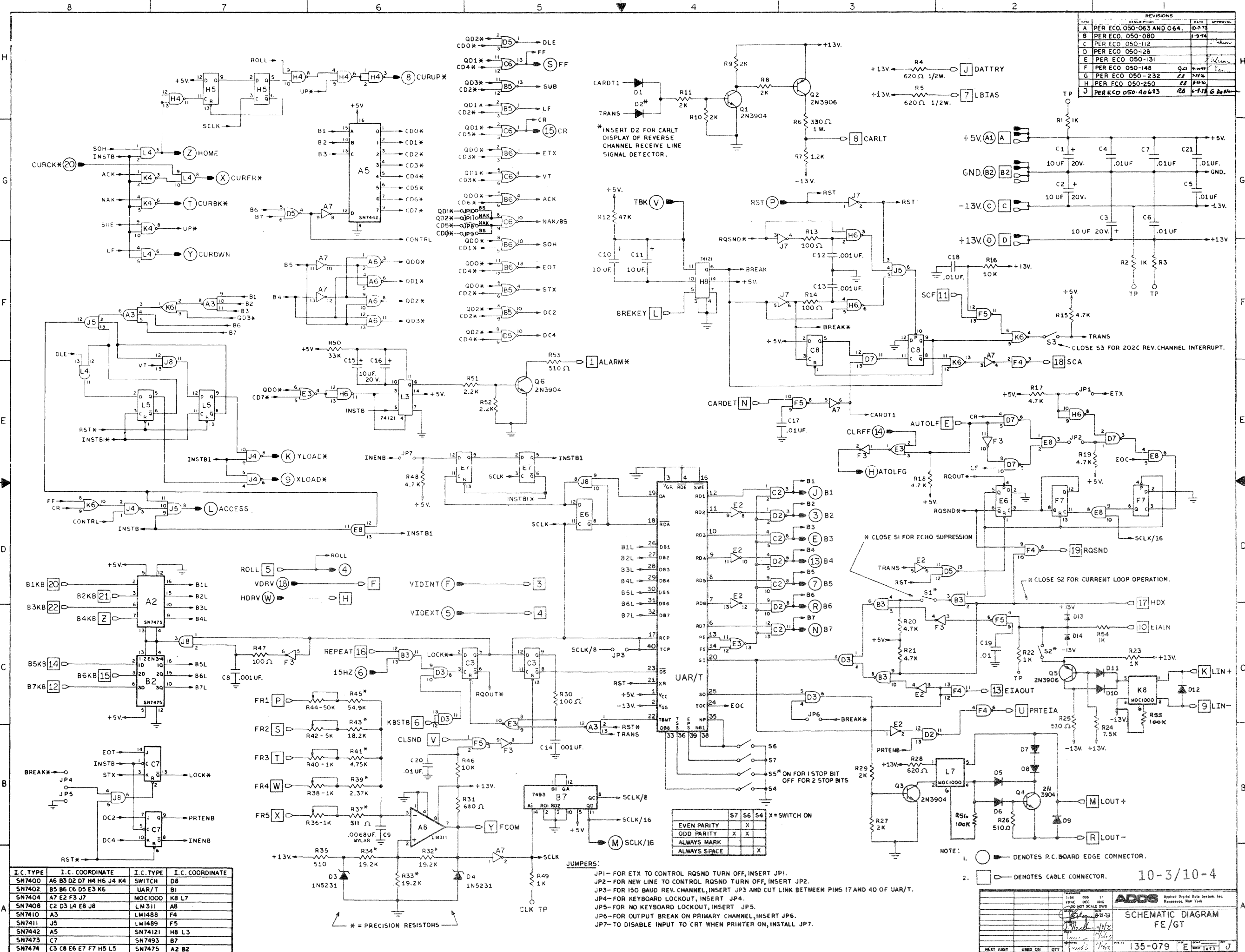
CONSUL 520/580 P.C. CARD LOCATIONS

Fig.10-1



—TOP VIEW—





REV.	DESCRIPTION	DATE	APPROVAL
A	PER ECO 050-063 AND 064.	10-7-73	
B	PER ECO 050-080	1-9-74	
C	PER ECO 050-112		
D	PER ECO 050-128		
E	PER ECO 050-131		
F	PER ECO 050-148	9-22-74	
G	PER ECO 050-232	2-2-75	
H	PER ECO 050-250	1-8-75	
J	PER ECO 050-40613	1-28-78	G. Behr

I.C. TYPE	I.C. COORDINATE	I.C. TYPE	I.C. COORDINATE
SN7400	A6 B3 D2 D7 H4 J4 K4	SWITCH	D8
SN7402	B5 B6 C6 D5 E3 K6	UAR/T	B1
SN7404	A7 E2 F3 J7	MOC1000	K8 L7
SN7408	C2 D3 L4 E8 J8	LM311	A8
SN7410	A3	LM1488	F4
SN7411	J5	LM1489	F5
SN7442	A5	SN74121	H8 L3
SN7473	C7	SN7493	B7
SN7474	C3 C8 E6 E7 F7 H5 L5	SN7475	A2 B2

	S7	S6	S4
EVEN PARITY		X	
ODD PARITY	X	X	
ALWAYS MARK			X
ALWAYS SPACE			X

- JUMPERS:
- JP1 - FOR ETX TO CONTROL RQSDN TURN OFF, INSERT JP1.
  - JP2 - FOR NEW LINE TO CONTROL RQSDN TURN OFF, INSERT JP2.
  - JP3 - FOR 150 BAUD REV. CHANNEL, INSERT JP3 AND CUT LINK BETWEEN PINS 17 AND 40 OF UAR/T.
  - JP4 - FOR KEYBOARD LOCKOUT, INSERT JP4.
  - JP5 - FOR NO KEYBOARD LOCKOUT, INSERT JP5.
  - JP6 - FOR OUTPUT BREAK ON PRIMARY CHANNEL, INSERT JP6.
  - JP7 - TO DISABLE INPUT TO CRT WHEN PRINTER ON, INSTALL JP7.

- NOTE:
- DENOTES P.C. BOARD EDGE CONNECTOR.
  - DENOTES CABLE CONNECTOR.

10-3/10-4

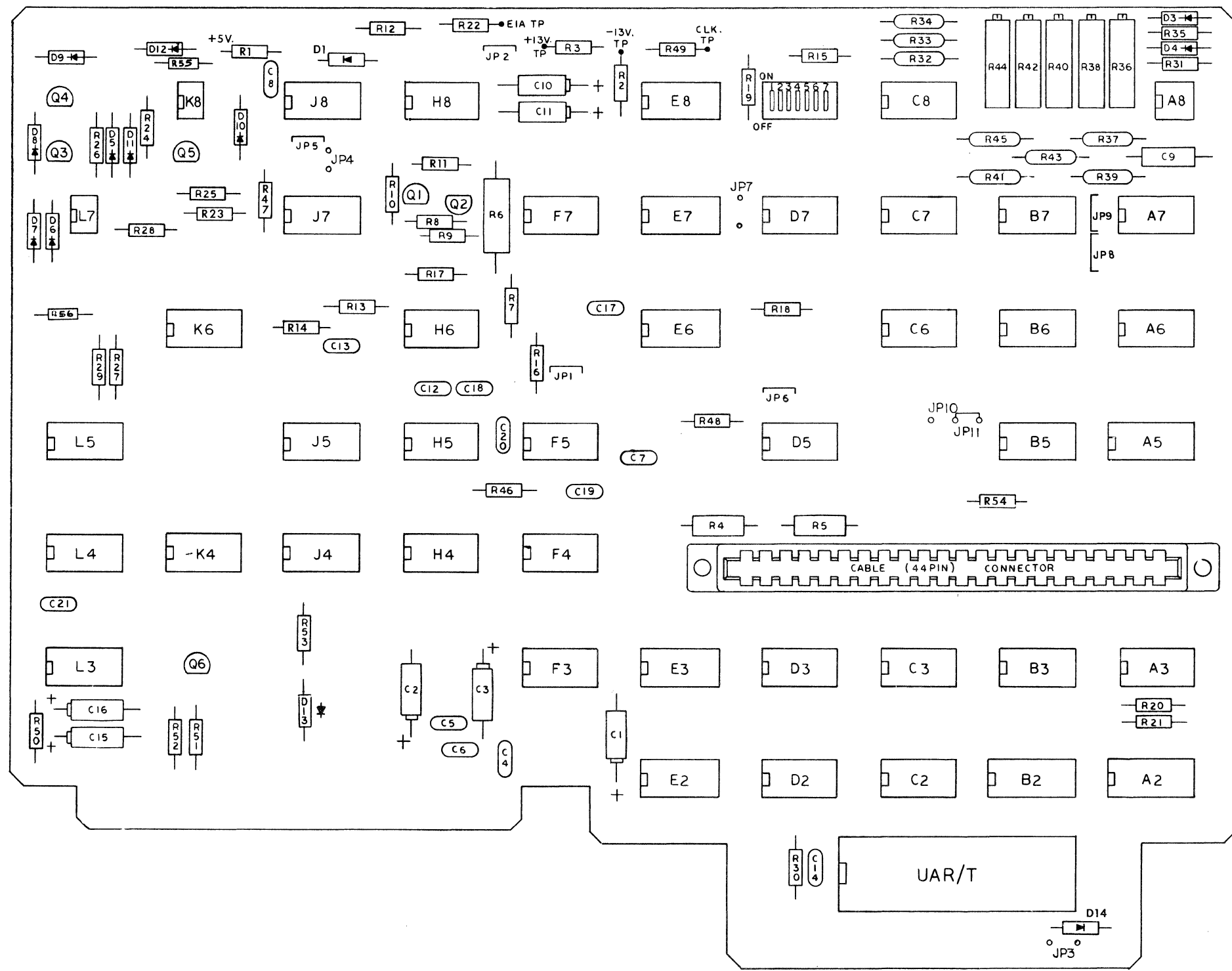
REV.	DESCRIPTION	DATE	APPROVAL
1	10-3-73		
2	10-3-73		
3	10-3-73		
4	10-3-73		
5	10-3-73		
6	10-3-73		
7	10-3-73		
8	10-3-73		
9	10-3-73		
10	10-3-73		

SCHEMATIC DIAGRAM  
FE/GT

135-079

ALL DESIGNS, PLANS OR SPECIFICATIONS USED ON THIS MATERIAL  
 REMAIN THE PROPERTY OF APPLIED DIGITAL DATA SYSTEMS  
 NO AND MAY NOT BE USED OR REPRODUCED IN ANY MANNER WITHOUT  
 ITS WRITTEN CONSENT

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	PER ECO NO. 050 063 AND 064	10/5/73	
B	UPDATE REV LTR TO SCHEM NC		
C	PER ECO 050-112	12-24-74	
D	PER ECO 050-128		
E	PER ECO 050-131	5-20-75	
F	PER ECO 050-148	G.O. 9-9-75	
G	PER ECO 050-158	G.O. 10-20-75	
H	PER ECO 050-179	D.O. 3-4-76	
J	PER ECO 050-210	EB 5-28-76	
K	PER ECO 050-270	10-26-76	Ⓢ
L	PER ECO 050-40226	JB 6-77	
M	PER ECO 050-40455	SK 2-21-78	
N	PER ECO 050-40623	6-12-78	RB JH

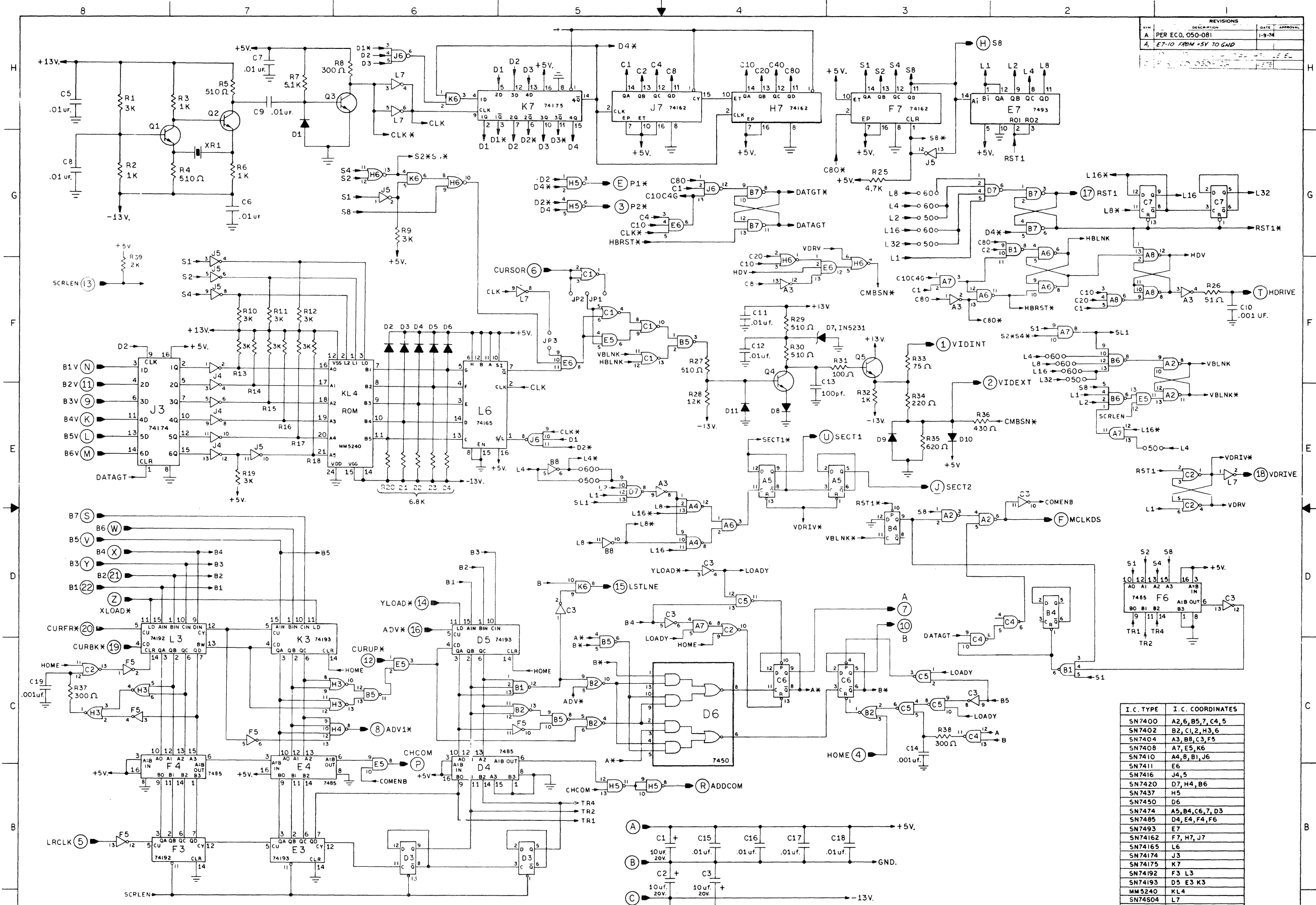


- NOTES:
- JUMPERS:
    - JP1 - FOR ETX TO CONTROL RQSDN TURN OFF, INSERT JP1.
    - JP2 - FOR NEW LINE TO CONTROL RQSDN TURN OFF, INSERT JP2.
    - JP3 - FOR 150 BAUD REV. CHANNEL, INSERT JP3 AND CUT LINK BETWEEN PINS 17 & 40 OF UAR/T.
    - JP4 - FOR KEYBOARD LOCKOUT INSERT JP4.
    - JP5 - FOR NO KEYBOARD LOCKOUT, INSERT JP5.
    - JP6 - FOR OUTPUT BREAK ON PRIMARY CHANNEL, INSERT JP6.
    - JP7 - TO DISABLE INPUT TO CRT WHEN PRINTER ON, INSTALL JP7.
  - SWITCH:
    - S1 - ON FOR ECHO SUPPRESSION.
    - S2 - ON FOR CURRENT LOOP OPERATION.
    - S3 - ON FOR 202-C REVERSE CHANNEL INTERRUPT.
    - S4 - ON FOR ABRAS. L&RT
    - S5 - ON FOR 1 STOP BIT, OFF FOR 2 STOP BITS.
    - S6 - ON FOR PARITY.
    - S7 - ON FOR ...

10-5/10-6

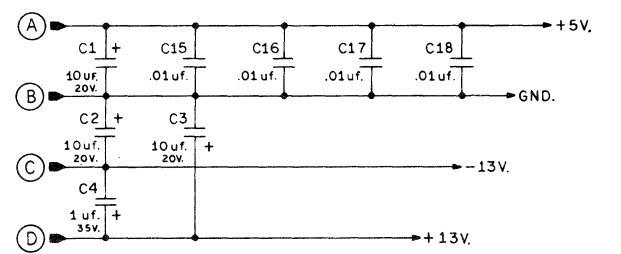
TOLERANCES		1/64 005 1"		<b>ADDS</b> Applied Digital Data System, Inc. Hauppauge, New York
FRAC DEC ANG		DEC ANG		
DO NOT SCALE DWG		DATE		
DATE		DATE		
DESIGNED BY	10/15/73	DATE	11/17/82	ASSEMBLY FE/GT
CHECKED BY	11/17/82	DATE	11/17/82	
APPROVED BY	11/17/82	DATE	11/17/82	
NEXT ASSY	USED ON	QTY	129-07900	SHEET 1 of 4 REV N

REVISIONS		
REV	DESCRIPTION	DATE
A	PER ECO. 050-081	1-9-74
4	E7-10 FROM +5V TO GND	



- NOTES:
1. ALL RESISTORS ARE 1/4W, 5%, UNLESS OTHERWISE NOTED.
  2. ALL DIODES ARE IN914 UNLESS OTHERWISE NOTED.
  3. ALL TRANSISTORS ARE 2N3646 UNLESS OTHERWISE NOTED.
  4. FOR 50 Hz OPERATION, INSTALL ONLY 50 HZ JUMPERS AND 12.6 MHz CRYSTAL.
  5. FOR 60 Hz OPERATION, INSTALL ONLY 60 HZ JUMPERS AND 12.528 MHz CRYSTAL.
  6. FOR BLACK CHARACTERS ON WHITE BACKGROUND, INSTALL JP1.
  7. FOR WHITE CHARACTERS ON BLACK BACKGROUND, INSTALL JP2 AND JP3.

I.C. TYPE	I.C. COORDINATES
SN7400	A2,6,B5,7,C4,5
SN7402	B2,C1,2,H3,6
SN7404	A3,B8,C3,F5
SN7408	A7,E5,K6
SN7410	A4,8,B1,J6
SN7411	E6
SN7416	J4,5
SN7420	D7,H4,B6
SN7437	H5
SN7450	D6
SN7474	A5,B4,C6,7,D3
SN7485	D4,E4,F4,F6
SN7493	E7
SN74162	F7,H7,J7
SN74165	L6
SN74174	J3
SN74175	K7
SN74192	F3,L3
SN74193	D5,E3,K3
MM5240	KL4
SN74504	L7

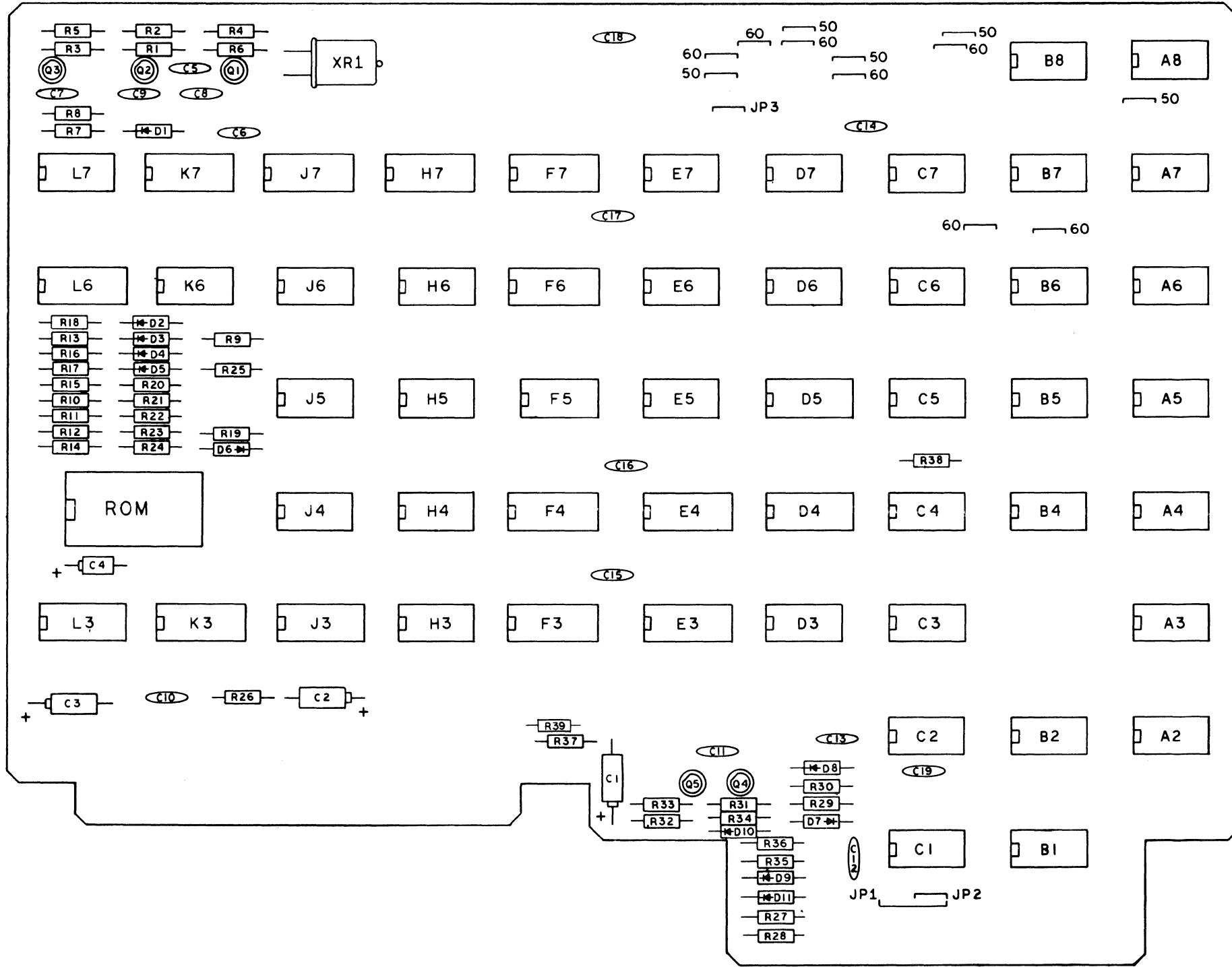


10-7/10-8

REVISED	ISS	ANG	ADD	Applied Digital Data System, Inc.
1-14	008	1	1	Waukegan, New York
FRAC	DEC	ANG	REV	
10	10	1	1	
DO NOT SCALE DWG				
SCHEMATIC DIAGRAM				
VG/GT				
NEXT ASSY	USED ON	QTY	REV	
135-080			REV	
			DATE	
			BY	
			CHECKED	
			DATE	

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REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	UPDATE REV LTR TO SCHEM-NC	1	
B	UPDATE REV LTR TO SCHEM-NC	1/1/74	CB
C	PER ECO 050-126	4-3-75	
D	PER ECO 050-179	8-12-76	
E	PER ECO 050-186, 214	5-14-76	
F	PER ECO 050-268 P/N ITEM#7	10-8-76	
G	PER ECO 050-40621	5-2	JB 84-2



ADDS P/N	SPMD No.	REV
129-08001	ADDS STD.	G
129-08004	117-10068	B
129-08005	117-10042	B
129-08006	117-10041	B
129-08007	117-10058	B
129-08008	117-10070	B
129-08009	117-10067	B
129-08010	117-10033	A
129-08011	117-10034	A

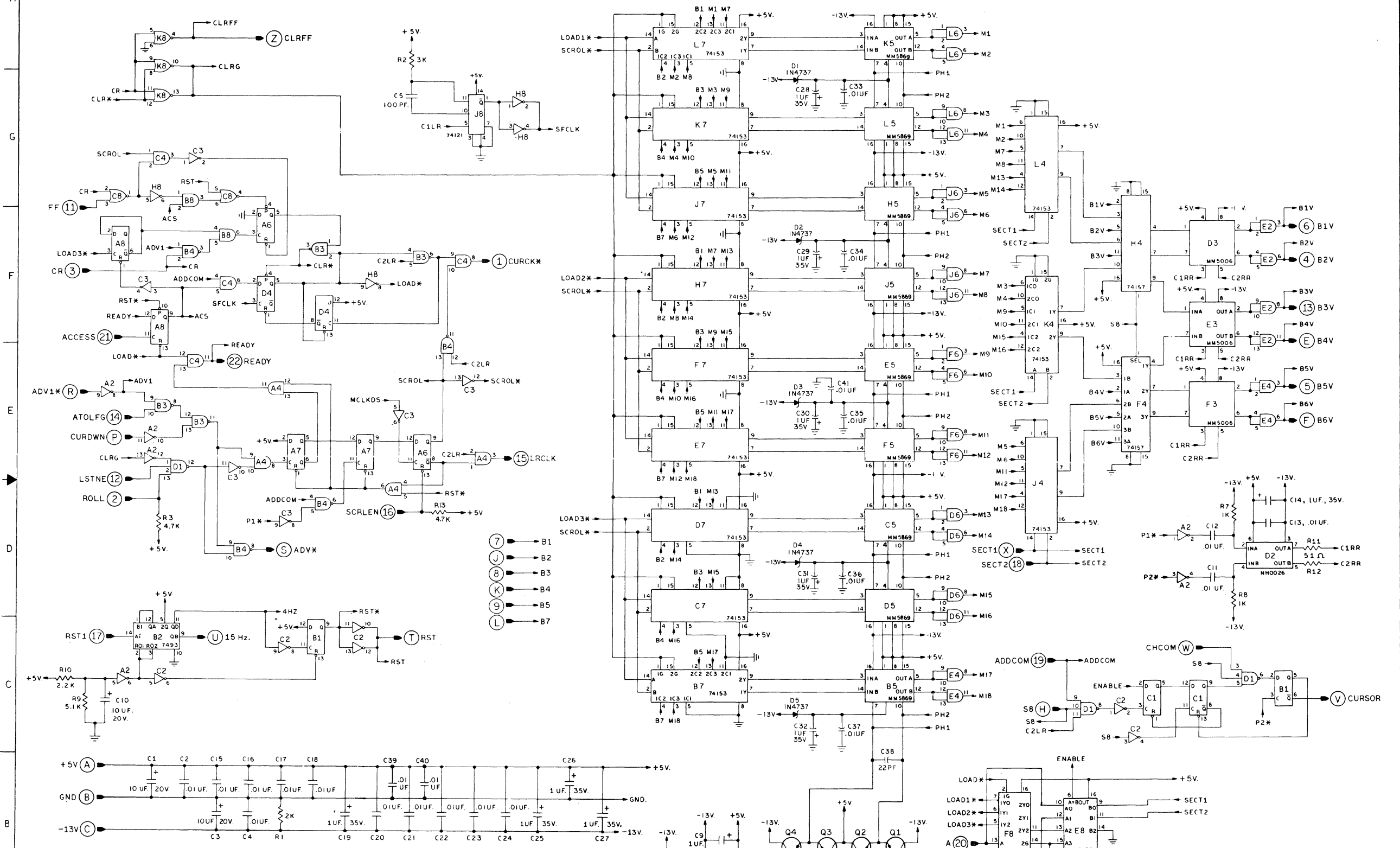
NOTE: SEE SEPARATE B.O.M. TITLE SHEETS FOR CHANGE DESCRIPTIONS.

- NOTES:
- FOR 50 HZ OPERATION, INSTALL ONLY 50 HZ JUMPERS AND 12.6 MHZ CRYSTAL.
  - FOR 60 HZ OPERATION, INSTALL ONLY 60 HZ JUMPERS AND 12.528 MHZ CRYSTAL.
  - FOR BLACK CHARACTERS ON WHITE BACKGROUND, INSTALL JP1.
  - FOR WHITE CHARACTERS ON BLACK BACKGROUND, INSTALL JP2 and JP3.

10-9/10-10

TOLERANCES		1/64	0.05	1		DATE: 10/11/75 TIME: 11:17 AM	APPROVED:	DWG NO: 129-080	SHEET: 1 of 4	REV: G
FRAC DEC ANG										
DO NOT SCALE DWG										
NEXT ASSY		USED ON		QTY	Applied Digital Data System, Inc. Hauppauge, New York <b>ADDS</b> ASSEMBLY VG/GT					

REVISIONS			
STK	DESCRIPTION	DATE	APPROVAL
A	ECO 050-201	8/8	F-H-3
B	ECO 050-40639	4-1-78	



I.C. TYPE	I.C. COORDINATES	I.C. TYPE	I.C. COORDINATES
SN7400	B3, 4	MM5006	D3, E3, F3
SN7402	C8, KB	MM5869	B5, C5, D5, E5, F5, H5, J5, K5, L5
SN7404	A2, C2, 3, H8		
SN7408	A4, B8, C4, D6, E2, 4, F6, J6, L6	NH0026	A5, D2
SN7410	D1		
SN7474	A6, 7, 8, B1, C1, D4		
SN7485	E8		
SN7493	B2		
SN74121	J8		
SN74153	B7, C7, D7, E7, F7, H7, J4, 7, K4, 7, L4, 7		
SN74155	D8, F8		
SN74157	F4, H4		

10-11/10-12

Applied Digital Data System, Inc.  
 SCHEMATIC DIAGRAM  
 MC/GT/N

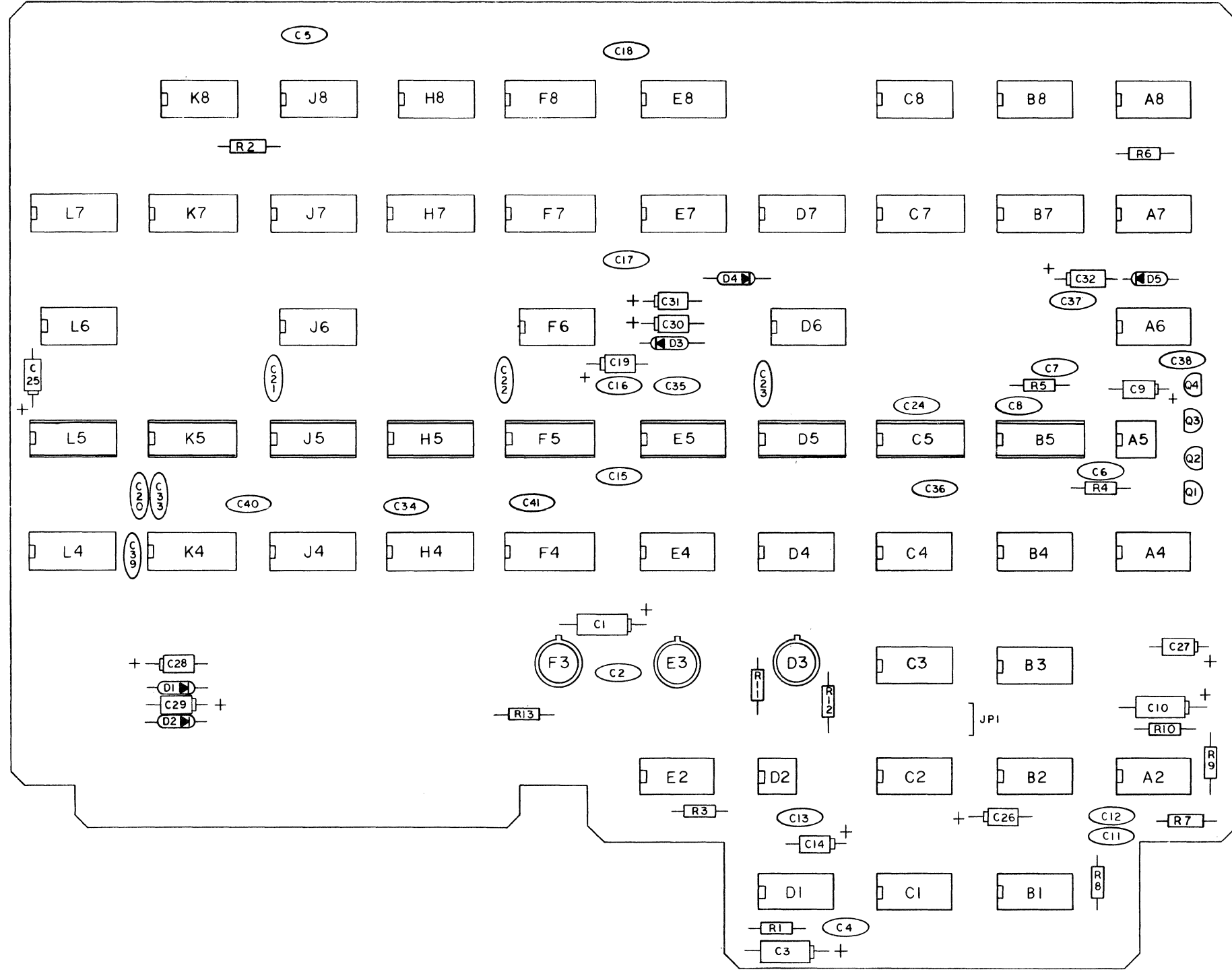
FOR BLINKING CURSOR  
 INSTALL JP1.

APPROVED BY: [Signature]  
 DATE: 10/10/78

135-152 D 101 8

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REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	ECO 050-201	5/20/78	J.B.
B	ECO 050-40226	6/18/77	J.B.
C	ECO 050-40368	10-7-77	M.R.
D	ECO 050-40539	4-3-78	R.P.
E	ECO 050-40736		



NOTE:  
FOR BLINKING CURSOR INSTALL JPI.

10-13/10-14

TOLERANCES		1/64 .005 1-		<b>ADDIS</b> Applied Digital Data System, Inc. Neenauge, New York
FRAC DEC ANG		DO NOT SCALE DWG		
DATE	DATE	DRAWN		ASSEMBLY MC/GT/N
4-1-78		CHECKED		
		ENG'G		
		APPROVED		
NEXT ASSY	USED ON	QTY	REV NO	REV
			129-152	D
			SIZE	1 OF 1
				E

SECTION 11:

WIRELIST AND HARNESS LIST

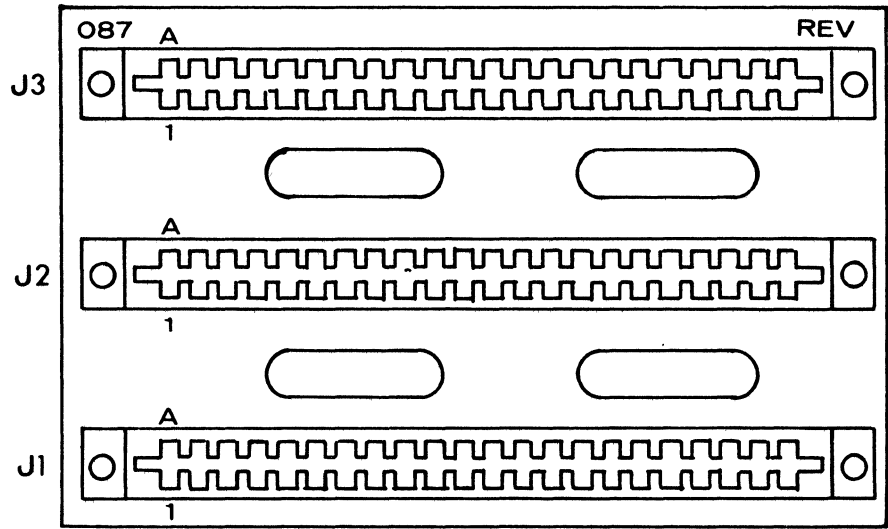
This section contains two types of information:

- a) A point-to-point wire list of the 580 backplane wiring, with signal names.
- b) A point-to-point wire list of the complete 580 harness, with appropriate signal names.

A drawing of the 580 card cage, as seen from the wirewrap side, is given in Figure 11-1 on the next page.

MBI, BACKPLANE MOTHER BOARD

Fig.11-1





WIRE WRAP LIST 520/580/380

VIDINT	J1, 1		J3, F
VIDEXT	J1, 2		J3, 5
P2*	J1, 3		J2, Y
HOME	J1, 4		J3, Z
LRCLK*	J1, 5		J2,15
CURSOR	J1, 6		J2, V
A	J1, 7		J2,20
ADV1*	J1, 8		J2, R
B3V	J1, 9		J2,13
B	J1,10		J2, N
B2V	J1,11		J2, 4
CURUP*	J1,12		J3, 8
SCRLEN	J1,13		J2,16
YLOAD*	J1,14		J3, K
LSTLNE	J1,15		J2,12
ADV*	J1,16		J2, S
RST1	J1,17		J2,17
VDRIVE	J1,18		J3,18
CURBK*	J1,19		J3, T
CURFR*	J1,20		J3, X
B2	J1,21	J2, J	J3, 3
B1	J1,22	J2, 7	J3, J
P1*	J1, E		J2,10
MCLKDS	J1, F		J2, M
S8	J1, H		J2, H
SECT2	J1, J		J2,18
B4V	J1, K		J2, E
B5V	J1, L		J2, 5
B6V	J1, M		J2, F
B1V	J1, N		J2, 6
CHOCM	J1, P		J2, W
ADDCOM	J1, R		J2,19
B7	J1, S	J2, L	J3, N

WIRE WRAP LIST 520/580/380

HDRIVE	J1, T		J3, W
SECT1	J1, U		J2, X
B5	J1, V	J2, 9	J3, 7
B6	J1, W		J3, R
B4	J1, X	J2, K	J3,13
B3	J1, Y	J2, 8	J3, E
XLOAD*	J1, Z		J3, 9
CURCK*	J2, 1		J3,20
ROLL	J2, 2		J3, 4
CR	J2, 3		J3,15
FF	J2,11		J3, S
ACCESS	J2,21		J3, L
CURDWN	J2, P		J3, Y
RST	J2, T		J3, P
15HZ	J2, U		J3, 6
CLRFF	J2, Z		J3,14
ATOLFG	J2,14		J3, H

VIDEO POWER HARNESS ASSEMBLY (511-20000)

<u>From</u>	<u>To</u>	<u>Signal Name</u>
POWER SUPPLY CONNECTOR J1	CRT MOLEX	
1	1	GND
2	2	+13V
GND LUG	3	CHASSIS GND

---

PDL POWER HARNESS ASSEMBLY (511-20100)

POWER SUPPLY CONNECTOR J2	PDL 129-153 POWER CONN.	
1,4	1,4	GND
2	2	-13V
5	5	+13V
3,6	3,6	+5 V

---

VIDEO SIGNAL HARNESS ASSEMBLY (511-20200)

CRT 14 PIN DIP	129-150 MONITOR CONNECTOR	
14	14	HDRV
13	13	VDRV
11,12	11,12	GND
3	3	VIDINT
5	5	-BRT
6	6	WIPER
7	7	+BRT

---

SONALERT HARNESS ASSEMBLY (511-20300)

129-153 SONALERT CONNECTOR	SONALERT LUGS	
1	1	GND
2	2	+13V

---

REAR PANEL HARNESS ASSEMBLY (511-20800)

<u>From</u>	<u>To</u>	<u>Signal Name</u>
129-153 EIA CONNECTOR	129-150 EIA CONNECTOR	
1,3	1,3	GND
2	2	VIDEXT
4	4	PRT EIA
5	5	GND
6	6	VDRV
7	7	GND
8	8	HDRV
9	9	GND
10,12	10,12	GND
11	11	VIDINT
13,15	13,15	GND
14	14	FCOM
16	16	FR1
17	17	FR3
18	18	FR2
19	19	FR4
20	20	FR5
21	21	GND
22	22	EIA OUT
23	23	LINT
24	24	EIA IN
25	25	LIN -
26	26	RQSND
27	27	DATTRY
28	28	CLSND
29	29	LBIAS
30	30	CARDET
31	31	L OUT +
32	32	SCA
33	33	L OUT -
34	34	SCF

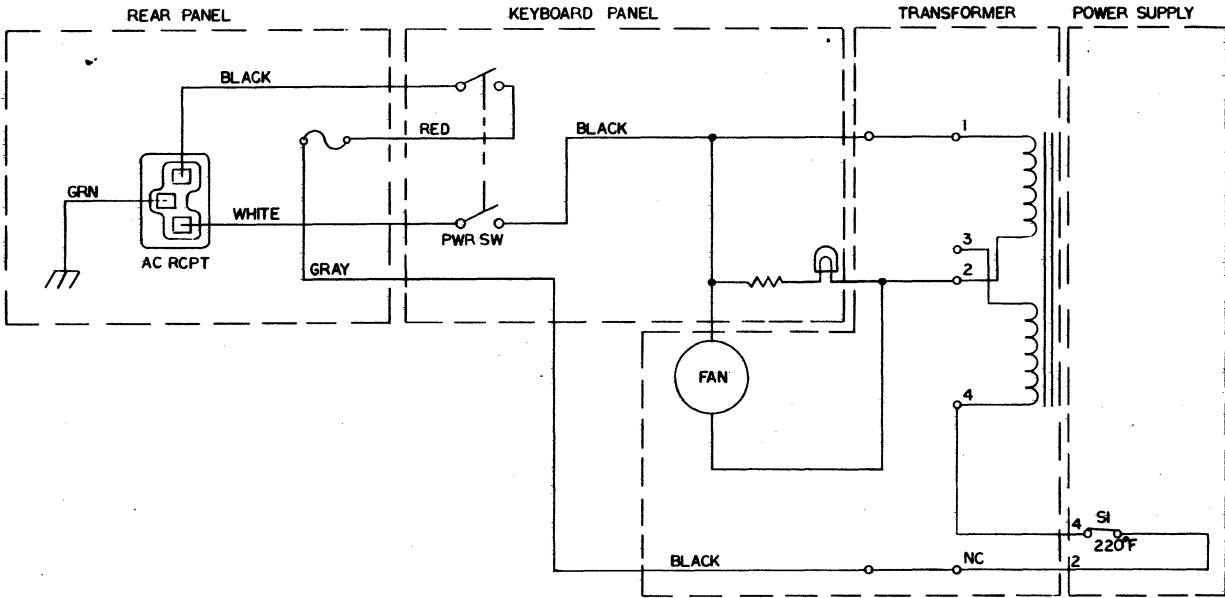
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KEYBOARD HARNESS ASSEMBLY (511-20900)

<u>From</u>	<u>To</u>	<u>Signal Name</u>
129-153		
KEYBOARD CONN.	KEYBOARD	
1	1	GND
2	2	BREAK
3	3	GND
4	4	KBSTB
5	5	GND
6	6	BIT 1
7	7	BIT 2
8	8	BIT 3
9	9	BIT 4
10	10	BIT 5
11	11	BIT 6
12	12	BIT 7
13	13	BIT 10
14	14	ROLL
15	15	AUTO LINE FEED
16	16	FULL DUPLEX
17	17	REPEAT
18	18	CARRIER
19	19	GND
20	20	-13V
21	21	-13V
22	22	+5V
23	23	+5V
24	24	+5V
25	25	+5V
26	26	+5V

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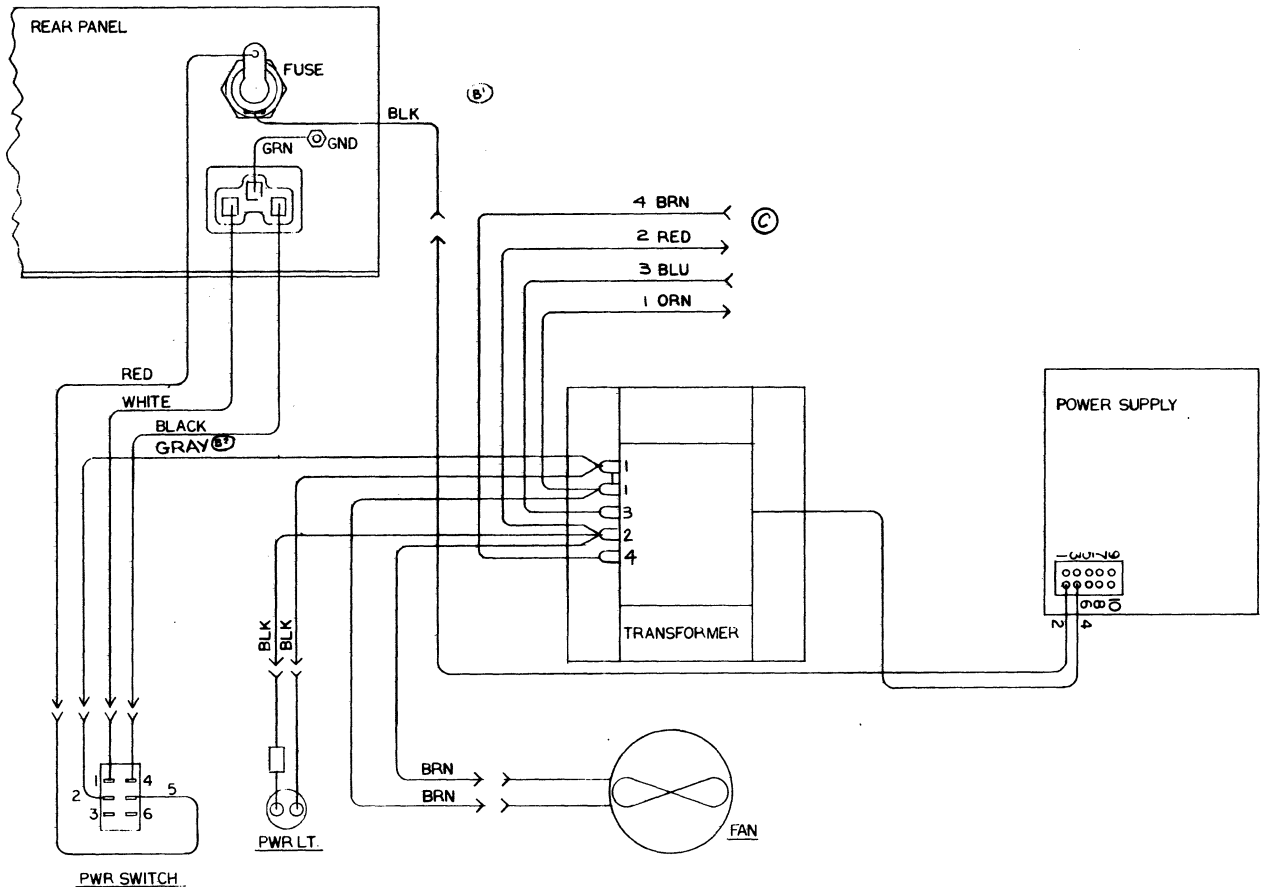
REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL



TOLERANCES: 1/64 .005 1' FRAC DEC ANG DO NOT SCALE DWG			<b>ADDS</b> Applied Digital Data System, Inc. Hempstead, New York	
DRAWN R.BISESTI	DATE 5-3-76	SCHEMATIC DIAGRAM AC WIRING NEW CONSUL SERIES		
CHECKED				
ENG'G				
APPROVED				
NEXT ASSY	USED ON	QTY	PWS NO 600-00900	SIZE C
			SCALE 1/2"	REV A
			SHEET 10F2	

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REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	RELEASE FOR PRODUCTION	5-3-76	[Signature]
B	ECO 050-230 B <sup>1</sup> WAS GRAY B <sup>2</sup> WAS BLACK	6-25-76	[Signature]
C	ADD STRAPPING WIRES ECO 050-33600	10-29-76	[Signature]
D	ECO 050-40059	2-10-77	[Signature]



NOTES:  
 FOR 120 V OPERATION STRAP  
 1 (ORN) TO 3 (BLUE) & 2 (RED) TO  
 4 (BRN).  
 FOR 240 V OPERATION STRAP  
 2 (RED) TO 3 (BLU).

TOLERANCES 1/64 OOS 1- FRAC DEC ANG DO NOT SCALE DWG		<b>ADDS</b> Applied Digital Data System, Inc. Norwango, New York	
DATE 5-3-76	DRW RBIESTI	AC WIRING DIAGRAM NEW CONSUL SERIES	
DATE 6-25-76	CHEK P.GLOVIE		
DATE 6-25-76	ENG [Signature]		
DATE 6-25-76	APP [Signature]		
DATE	APP	DWG NO 600-00900	REV D
DATE	APP	SCALE C	SHEET 2 OF 2
DATE	APP	QTY	
DATE	APP	USED ON	
DATE	APP	NEXT ASSY	

D  
C  
B  
A  
6-II

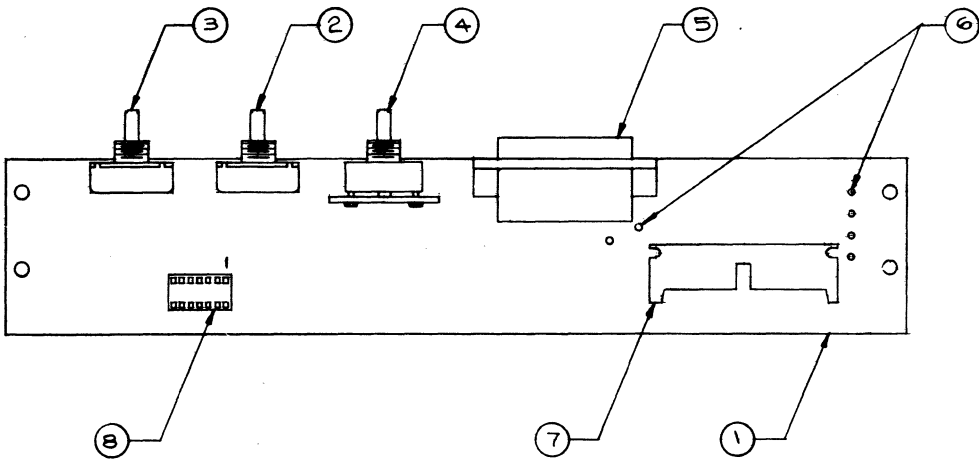
D  
C  
B  
A

4 | 3 | 2 | 1

4 | 3 | 2 | 1

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	RELEASE FOR PRODUCTION	5-4-76	

ALL DIMENSIONS, PLANS OR SPECIFICATIONS USED ON THIS MATERIAL, REGARDLESS OF THE PROPERTY OF APPLIED DIGITAL DATA SYSTEMS, INC. MAY BE USED OR REPRODUCED IN ANY MANNER WITHOUT THE WRITTEN CONSENT.



				TOLERANCES: 1/64 .005 1- FRAC DEC ANG DO NOT SCALE DWG	<b>ADDS</b> Applied Digital Data System, Inc. Hauppauge, New York				
			DRAWN P. BISESTI	DATE 1-16-76					
				CHECKED  ENG'N	REAR PANEL CARD 570/580 ASSY				
				APPROVED 36		DATE 5-4-76			
			NEXT ASSY	USED ON	QTY	DWG NO 129-150	SIZE C	SCALE 1:1 SHEET 1 of 2	REV A

11-11  
D  
C  
B  
A

D  
C  
B  
A

4

3

2

1

4

3

2

1

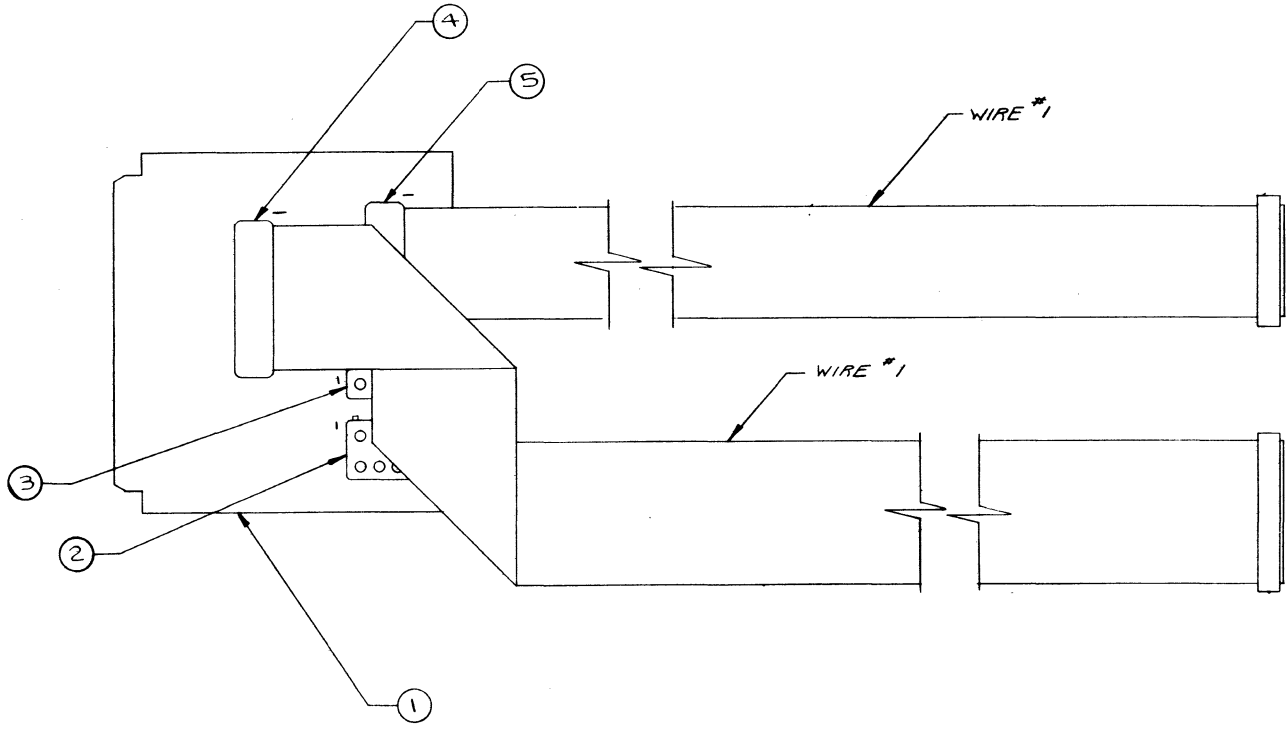




11-12

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REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	RELEASE FOR PRODUCTION	5-4-76	<i>[Signature]</i>
B	ELO 050-40162	5-29-77	<i>[Signature]</i>



C

B

A

D

C

B

A

			TOLERANCES		<b>ADDS</b> Applied Digital Data System, Inc. Hauppauge, New York	
			1/64	.005	1°	
			FRAC	DEC	ANG	
			DO NOT SCALE DWG			
			DRAWN	DATE		
			REBIS	5-27-76		
			CHECKED			
			ENG			
			APPROVED	5-4-76	DWG NO	511-204000
NEXT ASSY	USED ON	QTY	<i>[Signature]</i>	5-4-76	SIZE	C
					SCALE	SHEET 1 OF 2
					REV	B

PDL CARD  
HARNESS ASSY  
520/580

4

3

2

1



COMMENT SHEET

LET US KNOW... if you have any recommendations for improving this publication. After writing your comments, fold, tape and mail this pre-addressed form to us. All comments will be given careful consideration, and become the property of Applied Digital Data Systems Inc.

(from the title page)

PUBLICATION TITLE \_\_\_\_\_ DATE \_\_\_\_\_

PUBLICATION NO. \_\_\_\_\_

YOUR NAME \_\_\_\_\_ TITLE \_\_\_\_\_

COMPANY \_\_\_\_\_

ADDRESS \_\_\_\_\_

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REMARKS:



