MICROSYSTEMS
JUL/AUG 1981
VOL.2/NO.4

16-BIT MICROCOMPUTER SYSTEMS

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Cost effective answers to floppy disk problems.

DMA answers. Standard, accumulator transfer floppy disk controllers can stall your microcomputer system's CPU for as long as 160 milliseconds. Just to access and transfer a sector of data to main memory. If CPU processing speed and system performance are critical, you need something better. That's where Morrow Designs' new intelligent Disk Jockey DMA™ controller comes in. This new breed of peripheral handles both 5¼" and 8" drives and can read almost any format in existence. Speed? Your CPU runs at full tilt while the DMA controller seeks and gathers a sector of data. How? Information transfers to and from main memory occur as "cycle steals" from the system bus. And the missing memory cycles are transparent to the CPU totalling only two milliseconds instead of the usual 80.

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OEM pricing available

*Prices subject to change without notice.

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VB3 is memory mapped for rapid screen updating. But it occupies memory only when activated. So one or more VB3s can be located at the same address with a full 65K of memory still available to the user.

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This month we are highlighting 16-bit microcomputer systems. There has been a great deal of hullabaloo about 16-bit systems of late, particularly the 8086, Z8000 and 68000. But we shouldn’t forget the 16-bit systems that have been operating on the S-100 bus for several years. Marinchip has had the TI-9900 and Alpha-Micro has had their LSI-11-like S-100 CPU’s on the market for well over three years. Seattle Computer Products and TecMar have had their 8086 S-100 CPU’s out for over two years.

These systems have met with a moderate success from systems houses. However, by comparison to 8-bit micros, their acceptance has been distantly disappointing. The lack of greater acceptance, as I see it, is due to two basic causes. First, there is a lack of software for these systems, and secondly these systems are significantly more expensive than 8-bit systems. And let’s face it, 8-bit systems meet the needs of most personal computer users very nicely.

There is no doubt that the new breed of 16-bit microprocessors have a lot to offer in multi-user systems; hence we can expect the 16-bitters to dominate this market. Also, as new applications packages are introduced which capitalize on the greater power of the 16-bit designs, and prices drop, we can also expect to see some single-users switch from 8-bit to 16-bit machines.

The April 1, 1981 issue of EDN magazine (published by Cahners Publishing Co., 221 Columbus Ave., Boston, MA 02116, $30/yr domestic) contained the first extensive benchmark testing of what are currently the four most popular 16-bit microprocessors: the DEC LSI-11/23, the Intel 8086, the Motorola 68000 and the Zilog Z8000. I highly recommend the article to all readers interested in 16-bit micros. The article is 41 pages long and contains all the source code programs for each test, as well as some interesting insights on the comparative features of these processors. I will very briefly summarize the data presented in the article but, again, I strongly recommend reading the article (single copy is $2 domestic).

Benchmark tests are complex and difficult to carry through without prejudice. EDN had each manufacturer conduct seven tests from a group of tests designed by Carnegie-Mellon University, closely supervising to insure a minimum of prejudice. All the source code was published, so readers can check the results on their own systems. I feel that they’ve done an excellent job.

It is apparent from the test results, which I’ve summarized at the end of this column, that each processor has certain strong points and drawbacks, advantages and liabilities.

The tests were conducted by the manufacturers, using the maximum clock speeds available at the time of the tests (late 1980). The following are the clock speeds used (MHz):

- LSI-11/23 3.33
- 8086 10.00
- 68000 10.00
- Z8000 6.00

The benchmark tests use common algorithms that appear frequently in programs. EDN excluded the CM tests dealing with floating point math and virtual-memory handling because most of the micros didn’t directly support such operations. The following are the benchmark tests conducted:

- A: I/O Interrupt Kernel
- B: I/O Kernel with FIFO
- E: Character-string search
- F: Bit set, reset test
- H: Linked-list insertion
- I: Quicksort
- K: Bit-Matrix Transposition

The benchmark results are shown in Table 1. The number of bytes are represented on the left of the slash, the execution time in microseconds appears on the right. Results of test H and I for the 8086 and LSI-11/23 were unavailable at publication date.

"Critical path" network analysis program for scheduling manpower, dollars and time to maximize productivity.

An interactive project management program that runs under CP/M and can relate together different skills, hourly pay rates and projects to maximize efficiency. MILESTONE could be used to track paper flow, build a computer, check a salesman's performance, or build a bridge. MILESTONE can be used by executives, engineers, managers, and small businessmen to:

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Formats: 8, NS, MP, CDOS, SB, TRS2, APPL.


CP/M™ compatible language for 8060/280 CPUs, supports full Pascal & With plus 45 commands to Standard Pascal including Random access files, 4G segment procedures & 16 bit BCD real type. NOW INCLUDES symbolic debugger which features trapping on stores, examining and changing variables and tracing of program execution.

Requires CP/M 2.2 & 56K RAM. Formats: 8, NS, APPL, TRS2.


All features of Pascals/M for the 8086 and 8088 processors running under the 8086/88 version of CP/M.

Requires CP/M-86 & 128K RAM. Format: 8.


8086/88 Translator for existing 8080/280 programs. The new source code can be easily edited and assembled using ACT II to produce hex code which can be executed by 8080/88. Enhances the extensions and features available in the 8080/86.

Requires CP/M & 32K RAM. Formats: 8, NS, APPL.


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Dear Editor:

My first exposure to your magazine was with the January/February issue, and the tip on the CP/M null file for returning to files in RAM was worth the price of the issue.

The evaluation article on double density controllers did your readers an injustice by neglecting the InterSystems product. The board found to be the fastest by the author would have come in second if this one had been included. Before I received my Intersystems FDC-2, I was confused by the advice people gave me about the inherent unreliability of double density and the importance of using this or that brand of premium disk. I have been running double-sided double density exclusively for over a year an a half a dozen different brands of disks, and in that time I have seen one read error message—which I provoked by ignoring the WAIT message while Wordstar was shuffling files. My worst crash required that I hit the reset button after feeding the Intersystems Pascal compiler with a corrupt ASCII file.

While this DMA controller may be a little more expensive than some other boards, the money I saved by using 64K of dynamic vs. static memory was more than the price of the controller.

Please continue with this type of comparative evaluation whenever you can.

Aubrey Soper, III
Virginia Beach, VA

Dear Editor:

Did North Star Topics get left out of the CP/M and S-100 user's journal permanently? I thought that it would provide solutions to problems I didn't know existed. I will now need to find a friendly users group. Could you perhaps rotate North Star Topics with other columns on new, improved, or compatible DOS and languages?

Yours is a great magazine with a wide variety of S-100 products covered. It complements an S-100 (maybe not IEEE compatible) computer well.

One of your new products is a "compliance H," what are other compliances? Do most CP/M programs come in some standard eight inch format?

Ron Masaoka
Gardena, CA

The editor replies:

No, North Star Topics is not out of Microsystems. Regrettably, Randy Reitz has been extremely busy of late on his bread-winning job. He is working on another column which you can expect to see in print soon. Also, we have several other North Star articles scheduled over the next few issues.

Regarding compliance with IEEE S-100 specs, we will have to wait for the final version of the standard. I expect this to be approved soon. Microsystems will carry the full details as soon as they are available.

Regarding CP/M disk format, note that the CP/M and SIG/M user group libraries are currently available in the following formats:

8" single density
5" North Star single or double density
Cromemco 5" and 8" single or double density
Micropolis 5"
DEC RSX-11M
Le Croy 8" Single density
Apple 5"
TRS-80 Model-I 5"
TRS-80 Model-II 8"

The SIG/M Group (Box 97, Iselin, NJ 08830) furnishes these disks to other clubs at $4/disk plus $2 shipping (first disk $1/disk thereafter—U.S. funds only). We hope to publish a list of all clubs who have these disks for copying.

Dear Editor:

I enjoyed Chris Terry's article, "The CP/M Connection" in the July/Aug and Sep/Oct issues of Microsystems, but I really must point out that Chris is mistaken on a technical point he made several times in Part 2.

In describing the allocation bitmap, he says "This map is read in when the drive is logged in, ... and is written back to disk each time a file on that disk is closed." It just isn't true! If Chris would try to show me where that map is stored, he would realize that it is not stored on the disk at all but is calculated from the file allocations in the directory and kept as a bit map only in memory. When CP/M "logs in" a disk, the directory is scanned and the map is created by checking off all extents that are currently in use by a file. This is the whole purpose of the login. This map must be correct for any disk write operation that needs another block allocated, so all CP/M disk write and update operations update this map. That is why CP/M does not like you to change diskettes without "rebooting" the system.

I enjoy Microsystems. Please keep up the good technical articles. But maybe you need a technical wizard to proofread some of their content.

David Mitton
New England Computer Society
CP/M Users Group Chairman
Cambridge, MA

Response from Chris Terry:

Dave is absolutely right. I must have been dreaming when I wrote that—dreaming about the mapping bytes in the FCB & directory entries!
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Dear Editor:

I became a charter subscriber in timely fashion when I bought a Cromemco Z2, to learn about the S-100 Bus. Since then I have devoured each issue, forcing Electronics (which comes four times more often) into a wait state whenever contention arises. The "Conflator," as I call it, set me back a bit so I could afford only a pair of single-sided, single-density 5 1/4" minifloppy disk drives. The problem that many of us face now is how to upgrade to 8" floppy without being left holding the bag when single/single 8" drives become unavailable. The main question I would pose to you, your staff, and to the general readership is: "How long will CP/M-compatible software be available on SS/DD disks, and how quickly will the many software cassettes make their goodies available on DS/DD disks?" Bob Weidemann's article on double-density in the Jan/Feb 1981 issue of Microsystems seems to indicate that a few years will go by before such disks can be used as transfer media. How many readers are faced with this dilemma? Mind you, I'm not against progress, but it is worth considering whether we S-100 junkies should bring back the tape cassette for software exchange and disk backup. The biggest plus, of course, is that Phillips won the battle over physical dimensions and recording format for this medium some time back.

In the April issue of Interface Age is an excellent article entitled "Proposed Cassette Data Storage Format Standard" by Lorin S. Mohler. I don't know if anything came of it, but would like to hear from readers who have, or who have knowledge of any de facto tape standard. Of critical importance in a standard is the method of encoding digital data as analog signals, the baud rate (1) and the resulting reliability of the whole package for sending a set of CP/M files from here to there. With true hindsight and a different purpose for tape in mind, I could suggest a few improvements to Mohler's proposal, which are meant to improve deliverability:

1. Rather than a CRC alone, each physical record (representing a CP/M disk sector) should use an error-correction code, such as the Hamming code.

2. Similarly, tape header information could be written redundantly using a simple 2-for-1 byte minimum-distance code I've discovered, allowing immediate error trapping and recovery.

3. Additional information, not to be included in the disk or file resulting from a transfer, could be included in the header; data written to a transmittal or archive tape.

4. Consideration should be given to those who wish to be compatible with the standard, but do not want or need to take advantage of embellishments.

Walter P. Davis
703rd Place
Brooklyn, NY 11231

Letters, cont'd...

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Visual Technology
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DataSouth DS-180 | 1385 |

MicroPro Int'l.
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| MailMerge | 110 | |
| DataStar | 225 | |
| SuperSort II | 155 | |

Microsoft
| FORTRAN | 349 | |
| COBOL | 574 | |
| BASIC-80 | 294 | |
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Digital Research Reveals Future Plans

Gary Kildall revealed Digital Research's current projects and plans for the future at the CP/M User Group meeting held in April at the West Coast Computer Faire. Gary also reported that DR now has over 200,000 licensed CP/M users on more than 250 different types of systems.

First of all, CP/M Version 3 is in the works and may be released by the end of this year. It will add the following features: time & date, passwords, type ahead, file lockout, record lockout, test and write a record, a screen-oriented editor, much better documentation and (naturally) a smaller TPA.

Also due from DR this year are CP/M Version 2 and MP/M-86. Due in 1982 is XLT-86, an 8080-to-8086 translator, PL/I-86 (full subset-G, with 8087 math processor provisions) and CP/NET-86. DR also expects to have 32-bit software in 1983; I imagine this means that they intend to support the Intel IAPX-432 32-bit micro.

DR sees a future with CP/M, MP/M, CP/NET and MP/NET systems integrated into a sophisticated networking system that uses backplane bus, Ethernet, IEEE-488, RS-232 and high speed parallel communications links between servers, requestors and server/requestors. They see a VAX type host as the node in such a local networking system. It should be noted that DR already has a DEC-VAX machine running at their facility.

IEEE-696/S-100 Standard Status

I have been appointed secretary of the IEEE-696 Standard committee. Although the standard is essentially finalized, committee members and other interested S-100 component suppliers are being given one last opportunity to request changes before the standard is forwarded to the IEEE Standards Group for adoption. I hope to print the final addendum to the standard in the September/October issue of Microsystems. I also expect that the standard will be formally adopted by the IEEE early in 1982.

Most S-100 manufacturers have changed, or are in the process of changing, their products to comply with the standard. It is likely that by mid-1982 all S-100 products will be in conformance with the IEEE-696 standard. Microsystems will attempt, through product reviews, to insure that manufacturers comply with the standard. Although no standard ever completely guarantees compatibility, the frequent incompatibility problems that have plagued the S-100 area should soon be ancient history.

BDS-C & Amethyst User Group News

Bob Ward is the new coordinator of the BDS-C User Group (409 E. Kansas, Yates Center, KS 66783). Membership is now $10. The group has several disks of software available on 8" standard single density format. They also expect to be able to handle Heath H-89 and Micropolis 5-1/4" formats. Included in the library is Adventure in C, 6800 and 1802 assemblers and a new C compiler. Disks are $8 domestic, $12 foreign.

Users of MINCE and SCRIBBLE text editor and formatter (AMETHYST) now have a user group. The main focus of the group is to provide coordination among users developing extensions to MINCE and SCRIBBLE. Membership is $6/yr. For more information write: Barry A. Dobyns, 1633 Royal Crest #1128, Austin, TX 78741, (512) 441-9466.

CP/M-UG & SIG/M Release New Disks

The CP/M-UG and SIG/M have released more volumes of public domain software. The CP/M-UG has released volume 49, containing Fortran material, and is expected to shortly release three more volumes. The disks can be obtained from CP/M-UG, 1651 Third Ave., New York, NY 10028, (212) 722-1700.

The SIG/M has released seven new disks bringing their total up to 25 volumes. The disks can be obtained from SIG/M, Box 97, Iselin, NJ 08830.

A 200 page printed catalog listing the contents of CP/M-UG volumes 1 through 49 and SIG/M volumes 1 through 18 is available for $10 domestic, $13 foreign, from NYACC (New York Amateur Computer Club), Box 106, Church Street Station, New York, NY 10008. NYACC can also furnish a listing for CP/M-UG and SIG/M local groups which furnish copies of these disks. Send a self-addressed, stamped envelope for this listing.

ADA Compiler Being Tested

Telsoftware Inc., of Sorrento Valley, CA (the company Dr. Ken Bowles, of UCSD Pascal fame, founded to develop an ADA compiler) reports that their ADA compiler is now at Beta test sites. The version released for test runs on Motorola 68000-based systems, and contains most, but not all, of the features of the DOD-ADA standard. The price for the compiler package is $2000.

According to certain reports, Western Digital, the Pascal Microengine supplier, had owned 20% of Telesoftware. However, in April WD withdrew and decided to develop its own ADA compiler. However, WD has retained a license for the Telesoftware ADA compiler.
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<thead>
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<th>Kit</th>
<th>A&amp;T</th>
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News & Views, cont'd...

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Patrick Lajico
President, California Digital Engineering
P.O. Box 526
Hollywood, CA 90028

New DOS From BDS-C Author

Ed Ziembas and Leon Zolman, author of the very popular BDS-C compiler, have developed a new “UNIX-like” Disk Operating System for 8080/Z80 based systems called “MARC.” It initially boots under CP/M. They claim that it includes the basic UNIX file system complete with users, groups, protections and the like, as well as much of the UNIX user interface and more. Further, they expect that the system will provide for the transparent running of most existing CP/M programs, as well as programs written for MARC. The expected price is $175, for another $75 you can have either BDS-C or the MINCE editor. We have received an advance copy of MARC and hope to publish a review shortly.

Zilog Announces New 8-Bit Micro

Zilog will soon release a new 8-bit micro that should delight the readers of this magazine. Late this year they will introduce the “Z800” (does that mean it is ten times as good as the Z80 and one-tenth as good as the Z8000?). The Z800 will be an enhanced Z80. Fully compatible with the Z80 instruction set, it will add hardware multiply and divide, and a memory-mapper circuit to access up to four Mbytes of memory. Zilog boasts that it will provide performance three times better than a four MHz Z80.

The Z800 will be offered in a non-multiplexed version like the Z80, and in a multiplexed version that can be used as a Z8000 peripheral. Zilog expects to start sampling the Z800 early this fall.

Incidentally, Zilog reported an $11 million loss on $42 million business in 1980. Zilog has yet to show a profit.

Random Rumors

Several S-100 manufacturers are already in development on CPU cards using the new Intel iAPX-432 32-bit microprocessor. We can expect to see the first such product reach the market late next year....Xerox is rumored to be about to introduce a low-cost (to Xerox $4K-$7K is low cost) microcomputer system using CP/M. They will also furnish WordStar for it. Apparently, this is intended to compete with the Apple.

UNIX Software List Published

A comprehensive directory of UNIX and C software products is being published by InfoPro Systems, Box 33, East Hanover, NJ 07936 ($18/yr domestic, $24 foreign). The first issue I received was nine pages long and listed 29 suppliers along with very interesting comments on the suppliers and their software packages.
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The CP/M Bus

by Anthony Skjellum

If you have questions about CP/M or MP/M we will attempt to answer them in this column. Send your questions to: Anthony Skjellum, 1695 Shenandoah Rd., San Marino, CA 91108.

The major topic of this column will be the continued discussion of possible enhancements for the CP/M operating system. The concept of link files will be introduced. Please refer to the material presented in the May-June "CP/M Bus."

I. More features for CP/M: Part II

It is often convenient for the same data or program to exist in more than one file on a disk. However, in some cases only one copy of the data is actually needed and it becomes a convenience to allow files to link to one another; this permits the programmer to organize data in a sophisticated manner. Link files aren't copies of files, but "point" to other files. Therefore, they only require link records and/or directory entries (depending on the type). Furthermore, when files are changed, any links to them reflect this change automatically.

Two types of link files will be defined here. They are simple and complex links, and will be treated in turn.

Link Files of the First Kind

Sixteen user areas are provided by CP/M2. Each user area requires its own copies of all the files to be used in that area. For example, transients like PIP and STAT are likely to be common to each area in use. However, it seems wasteful to place a copy in each user area, since the information is duplicated. Simple link files will solve this problem.

Simple link files consume no disk space other than a directory entry. They are identified by an attribute bit which we will call b2. These link files will link a file in user area zero. Since a link file requires no directory map, this sixteen byte region (d0...dn is the Digital Research convention) may be used for the name of the actual file in user area zero. See page 14 of CP/M 2.0 Users' Guide for CP/M 1.4 Owners for more information. Link files of this type will be prohibited in user zero.

In order to make simple links useful, a new CCP (console command processor) command is proposed. This is the LN command (standing for link). LN will be used to create simple links and will obviate the need for a special initialization process of new user areas. LN will be used as follows:

LN afn user-number

or

LN ufn user-number new-name

where user-number is a valid user area number greater than zero. When user-number is omitted, the current user area is assumed (provided that we are not in user area zero). Furthermore, "afn" is the ambiguous file

MICROSYSTEMS
specification. However, if we do want to rename the link, an unambiguous specification (ufn) will be needed as will the user-number. Here are two examples of LN in use:

```
USER x
LN *.COM ; change to user x<>0
LN *.* ; link all .COM files to this user area
            ; since user-area was omitted, x was assumed
LN PIP.COM x XFER.COM ; link PIP.COM to user area x and call it
            ; XFER.COM
            ; (we may be in any user area while doing this)
```

A simple link will have all attributes reset except b2'. However, they will be alterable with STAT. For example, we may want a link of a text file in user area x to be SYS even if the actual file in user zero were DIR. Also, remember that deleting a link to a file does not affect the original file in any way. The ERA command will be used to delete simple link files.

Simple link files may not be written to since they are only images of the actual file in user zero. However, reading a link file will be transparent to a transient; it will appear as though the actual file were being read, and no special BDOS commands to access this type of file are needed.

I also believe that simple link files could be included in MP/M without difficulty. Since there is no writing to these files, no problem about conflicts between multiple user access is anticipated.

The type of linking mechanism described above would be quite straightforward to implement and should be quite useful. It would definitely be advantageous in the MP/M environment also. Indeed, this is essentially the type of linking provided by operating systems like UNIX (shell command ln). However, much more ambitious linking mechanisms are possible and complex linking is described below.

**Link Files of the Second Kind**

Complex links continue where simple links leave off. A complex link file may have links to several other files or portions thereof, and may also include data records. Complex link files are indicated with an attribute bit, as are simple links. We will denote this attribute bit as b3'.

Link records consist of information to tell the BDOS what file or part of a file needs to be accessed. The maximum length of a link record entry is sixteen characters, so VLR files used for complex linking will have to have record lengths of at least sixteen. A complete discussion of the internals of link records will be deferred to the next column, when we will discuss them in conjunction with the sub-directory feature.

Complex link files will use normal directory entries since they consist of a number of data and link records which may be mixed as desired. With nested linking, several files will be open at once and each will require an FCB. For example, if file A linked to B which linked to C, three files would need to be open at once. Therefore, the concept of the extended file control block (EFCB) will be introduced.

The EFCB consists of several file control blocks which will be used by CP/M. The first FCB is called the primary FCB and is used for opening the link file. It is followed by six word quantities: nx, nc, a1, a2, a3 and a4. The nx variable tells the BDOS the maximum depth of nesting supported for this file. That means that there must be nx
CP/M Bus, cont’d...

FCB areas provided besides the primary FCB. The nc variable is used by BDOS and contains the current linkage depth. Variables a1, a2, a3 and a4 contain addresses: a1 is the current FCB in use (set by BDOS relative to the address a3), and a2 is the address of the link buffer which must also be provided for the use of CP/M. The link buffer provides storage space for a link record which is being processed. (The buffer is as long as the file record length.) This buffer is necessary since multiple link entries per record are possible. The address a3 points to the start of the first extended FCB. If a3 is zero, the extended FCB’s are assumed to follow directly. Finally, a4 is used by CP/M to keep track of its position within the link buffer.

Note that the primary FCB is assumed to be 36 bytes long and include the a0, r1 and r2 fields added in CP/M release two. However, the extended FCB’s require only 33 byte entries.

Several new BDOS commands will be needed in order to use complex link files. First of all, a create command will be needed. This will work as the standard make file command implemented in CP/M2. However, it will set the bit b’3’ high to indicate that the file is a complex link file. Two versions will be available, one for standard (128 byte record) files and one for VLR files. Second, a generalized open command will be needed. The DE register points to the primary FCB on entry to BDOS; all other necessary information is picked up from the FCB and words which follow it.

Several examples are provided here for clarity:

```
liw d,efcb    ; point to file control block
mvi c,make    ; probably will be the extended block
or a         ; if we plan to do subsequent reads
mvi d,depth   ; max nesting depth (is here)
cvi d,0       ; current depth
mvi a1,dw 0   ; current FCB in use (relative to a3)
a2s d,0 link buffer ; point to link buffer
s2s d,0       ; point to start of EFCB’s. If zero
                ; expect directly after a4.
shl h,5       ; used by CP/M to keep position in
                ; link buffer
if a          ; a1 address word gives the program
                ; capability to inspect the FCB’s of files linked by
                ; the primary file. With this information, these files could
                ; be independently opened and modified.
```

If an overflow of the EFCB occurs on a read, the sign bit of the accumulator is set. This can be detected as in one of the examples above.

Finally, we insist that all files linked by a primary file have the same record length as that primary file.

It will also be useful to manipulate link records directly. Therefore, a read record absolute command will be provided. This command will return the next record of the file even if it is a link record. Similarly, link records can be written by making a ^Y the first character of the record written, as complex link files are always writable when the nesting depth is zero (i.e. writing to the primary file is permitted.) The a1 address word gives the program the capability to inspect the FCB’s of files linked by the primary file. With this information, these files could be independently opened and modified.

Sophisticated indexing schemes are possible through the manipulation (e.g. sorting) of link records and the manipulation of record sub-ranges. Also note that the random access BDOS commands will not expand links (i.e. link records will be returned as read) so that random input-output can be used for creating an indexing method. It is left to the reader to explore these possibilities.

Sub-directories

In this and the last installment of “The CP/M Bus” we have discussed many new features and file modes which could be added to the CP/M operating system. Another extremely useful possibility is the sub-directory. This file type will provide the ability to deal with files outside the sixteen user numbers and allow a flexibility in file maintenance akin to that found on large systems. This will be a primary point of discussion in the next installment.

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DEALER AND OEM INQUIRIES INVITED
The TEC-86 16-Bit Computer System

by Chris Terry

The TEC-86 computer system, manufactured by TecMar Inc., is a general-purpose microcomputer system using the new Intel 8086 16-bit microprocessor. The rugged metal enclosure houses a heavy-duty power supply, an S-100 motherboard with twelve slots, and two Shugart SA800 8" floppy disk drives. The basic system is supplied with:

- CPU board equipped with an Intel 8086 microprocessor running at 5 MHz (4 or 8 MHz options available), an 8259A priority interrupt chip, and power-on jump circuitry;
- 32K of 300nS static RAM on two 16K boards, expandable to 1 Megabyte; available as an option is a single 64K dynamic RAM board at the same price as four 16K boards.
- PROM I/O board equipped with two 8251A serial ports capable of handling synchronous or asynchronous RS-232 data links at transmission speeds of up to 19,200 baud, an 8255 chip that provides 24 lines of parallel I/O, and sockets for 2K x 16 of PROM;
- Microbyte single/dual density disk controller, based on the NEC 765 LSI controller chip and capable of supporting up to four drives.

The price for the basic system is $3990; additional 16K memory boards are available at $395 each.

Hardware Documentation

The manuals supplied by TecMar for each board in the system are very good. They supply complete logic diagrams which, though reduced to half the original size, are clean and readable, as regards both lettering and layout. They are also split into convenient one page chunks, each of which contains one or more complete functions; connections that have to cross page boundaries are brought to the left or right edge of the diagram and are plainly visible. Pin connections and cabling to the outside world are clear and have text clarifications where necessary. On-board jumpers to select options are similar to those found on disk drives—contact pins which are connected together by jumper connectors in plastic covers. The placement of jumpers is both described and illustrated for each option, and the user should have no difficulty in setting up or changing the jumpers correctly. Switch settings are defined as “Open” or “Closed” according to the marking on the switches, and there are clear statements as to whether a switch closure represents a 1 or a 0 on the associated line.

The theory sections contain enough detail to clue in a person who already has a fair amount of hardware experience, and are enhanced by simplified logic diagrams of functions that might otherwise be difficult to understand. This is a most welcome change from so many other manuals where highly detailed and dense descriptions refer to equally dense fold-outs, with no clue as to where in the drawing to look.

TecMar is to be congratulated on these manuals. They have obviously hired professional writers and given them reasonable time and budget to do a first class job. The language is just informal enough to be readable without losing exactness, and clarity has been made a prime goal.

I found only one typographic error (the notorious “intergrated” chips, which conjures up visions of elves diligently grating cheese into the inter-chip spaces). And only one factual error—which in any case is not calamitous—the I/O board manual calls out RS232 signal levels as +5 to +15 volts for a Mark (1) and -5 to -15 volts for a Space (0). In fact, the RS232-C spec defines the signal level limits as 3 volts to 25 volts in either direction relative to signal ground; the positive level is a SPACE (0) for a data line and ON for a control line, whereas the negative level is a MARK (1) for a data line and OFF for a control line.

The Software

Software to support the TEC-86 consists of CP/M-86 from Digital Research, Inc., and Basic-86 from Microsoft, Inc. TecMar also has Pascal/M-86 from Sorcim available as an option. Mention is made in the PROM I/O board manual of a system monitor for which the PROM sockets are intended, but this does not appear on the current price list. The PROM in the evaluation system contains the CP/M-86 bootstrap and disk primitives, but no monitor accessible to the programmer. It would not be necessary,
**16 BIT 8086 MICRO SYSTEM**

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- **Tec-86W** includes a 31 Mbyte Winchester plus memory increase to 256K plus all the Tec-86 features below.
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  - 4-20 mA output - Filters

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Basic 86™ registered tradeMark: Microsoft
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since the CP/M-86 DDT is perfectly adequate for this purpose.

**CP/M-86**

This operating system is functionally equivalent to CP/M Version 2.X for the 8080/Z80 systems. The differences are due mainly to the use of separate memory segments for code, data, and stack, and the addition of function calls—CP/M-86 has 59 function codes, compared to the 36 of CP/M-80 Version 2.X. Page 0 is used for the same purposes as in CP/M-80, but the operating system is usually loaded at 400H, directly above the interrupt locations. You can, however, change this location. Relocatable transient programs load above the operating system, starting at 2A00H. Unlike CP/M-80, CP/M-86 does not use absolute locations for system entry or default variables; instead, entry to BDOS takes place through a software interrupt, and entry to BIOS is by a new function call. Most of the new function calls are related to the allocation or releasing of memory.

Because of the additional BDOS functions and a larger BIOS, CP/M-86 is too large to fit on two single-density tracks, though it fits comfortably on two double-density tracks. If single-density is used, the bootstrap loads only the cold-start loader; this in turn loads CP/M-86 from the file area (not the system tracks). A warm start is somewhat simpler because relocatable code is used. Thus, there is no MOVCPM utility; the only change is to the cold boot, telling it where to start loading the operating system.

The standard system supplied by TecMar is configured to run in a 64Kbyte memory; however, the distribution disk also contains systems to run in 32K or 96K.

**CP/M-86 Documentation**

As the Duke of Gloucester remarked when presented with Volume 4 of *The Decline & Fall of the Roman Empire*: “Another damned thick, square, book! Always scribble, scribble, scribble! Eh Mr. Gibbon?” The TecMar system documentation consists of a six page leaflet describing how to boot up the system (simplicity itself—turn on power, hit RESET, put the disk in the A drive, and close the door!), how to format disks for single or double density, and how to copy the system tracks, for which TecMar has provided utilities to suit the Microbyte controller and formats.

Digital Research has been (necessarily) more lavish. In addition to the *Introduction to CP/M Features and Facilities, The CP/M 2.2 User’s Guide,* and *The Ed User’s Manual,* which are standard for all versions, there is a huge amount of completely new material. The *CP/M-86 Reference Guide* has 138 pages. *The ASM-86 User’s Guide* has 75 pages, and *The DDT-86 User’s Manual* has 19 pages. *The CP/M-86 Reference Guide* is, like most Digital Research manuals, a tough nut to crack. All the required information is there, but it’s not always easy to find. The definitions of BIOS routines and BDOS function calls are easy—they are presented in order, concisely, and reasonably clearly. It’s the mass of other information that causes me trouble. I wish I knew why. I cannot complain that the manuals are badly written or disorganized. Individual sentences are perfectly clear, and there is organization. But it always takes me more time than I like to find what I am looking for. What is frustrating is that I cannot think of just how the manual could be better organized. I suppose you just have to read and read until you know it almost by heart, and then your brain goes “Click!” and the pieces drop into the places in your brain from which you can most easily retrieve them. Perhaps an index would help?

**Performance**

For me, the TecMar system has behaved in an exemplary way. I unpacked it, spent three or four hours with the manuals, plugged it in, connected a Lear-Siegler ADM-3A terminal set for 19,200 baud (as instructed), booted up, and away we went. Operationally, the instructions were clear and simple. Except for copying single-density Basic-80 to a double-density working disk, which gave me a little trouble at first, it’s just like running CP/M 2.2 and Basic-80.

I have not yet found a huge increase in speed, but that is because I have not yet gotten to any real number-crunching in A86. Basic-80, as I understand, is a simple translation of the interpreter from 8080 language to 8086 language, without optimization to make use of the special features of the 8086 CPU and architecture. Thus, when I loaded my Basic program for testing sorting routines, the interpreter (which runs on a 5-MHz clock) executed Bubble, Heap, Shell-Metzner, and Quick sorts in a shade less than half the time it takes on my 2 MHz 8080 machine using Basic-80. For 200 random numbers, the Bubble sort took 148 seconds instead of 310, Heap took 32 instead of 67, Shell-Metzner took 34 instead of 71, and Quick took 17 instead of 34 (average of three runs each). But I suspect that a Z80 running at 4 MHz would have done nearly as well.

However, I am sure that the speed advantages will be seen when there is more software around that is optimized for the 8086. A nice screen editor like Wordmaster, for example. ED is for the birds unless you still have a Teletype, and I am thankful to hear that impending CP/M-80 Version 3.X will have a screen editor. If an 8086 version also appears that uses the magnificent string-handling capability of the 8086, it will probably be a joy to use.

**Conclusions**

The TEC-86 is rugged, easy to get going, has given me no hardware problems and only minor software puzzlement (I didn’t read the manual carefully enough to start with). A price tag of $4600 (which includes 64K of RAM, CP/M-86 and Basic-86) is probably too much for the average hobbyist. But for a small business or a professional user it will be extremely good value, once the software starts being available. And don’t forget that there is much more available right now than you might think—you can run any existing Basic-80 program on the 8086, provided that you save it on a single-density disk as ASCII source code. As you may have gathered, I like TecMar’s product and their hardware manuals. I wish I could afford it for myself!

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Seattle Computer Products’ 8086 System

by Bill Machrone

Considerable attention has been generated by some of the recent entries into the 16-bit arena for the S-100 bus. Some manufacturers are still talking about it, others are doing something about it and a few are already old hands at it. Seattle Computer Products (SCP) has been manufacturing IEEE-696 compatible 8086 processors and 16-bit wide memories for more than two years. Additionally, they offer a system support board and a serial I/O board, all compatible with the 8086 or any other processor that follows the IEEE-696 Standard.

All the well-intentioned hardware in the world is worthless without software to make it go, and Seattle has pioneered here as well. Long before CP/M-86 was released, Seattle’s 86-DOS was a reality. Below, we’ll take a look at the available products and give an evaluation of just how fast it is and how useful it could be in your system.

Hardware

The processor board itself contains an 8 MHz 8086 which can be switch-selected to run at 4 MHz. The board produces or responds to all the standard S-100 signals, including SXTRQ* and SIXTN*. This means that the board can address memories that are either eight or sixteen bits wide and, in accordance with the IEEE-696 Standard, permits intermixing them in the same system. The memory cards must support 24-bit extended addressing. The processor handles memory and I/O references as either eight bit transfers, sixteen bit transfers or “double eight bit transfers” where memory is incapable of a sixteen bit transfer. There is a provision for an IMSAI-style front panel, but a small modification is necessary to make it work. Examine and deposit functions are inoperative with the 8086.

The CPU Support Board has all the goodies necessary to make the system functional, including a monitor/ bootstrap EPROM, two 8259A interrupt controllers, two 16-bit counter/timers, a 24 hour clock (more timers, actually) with provision for battery backup, a serial port, a parallel port and a sense switch input port. Strangely enough, the parallel port is configured as a separate parallel input port and a parallel output port, each with its own cable header on top of the board. This may be advantageous for some applications, but doesn’t permit a full handshaking bidirectional configuration. The bootstrap EPROM has a full 8086 monitor program which allows memory inspection, tracing, debugging and booting the disk controller. At this writing, Seattle does not manufacture a floppy disk controller, so you can request an EPROM which boots one of several popular disk controllers, such as the Tarbell double density controller or the Cromemco 4FDC.

The timers are implemented with the versatile AMD 9513, which provides five timers—one intended as a baud rate generator, two general purpose and two which can be configured as a time of day clock with 0.01 second resolution, or which can also be used as general purpose timers. It has settable alarm registers, which can generate interrupts. Much has already been written about the 8259A interrupt controllers, and their power and versatility is well known. They are configured in a master/slave relationship on the CPU Support Board. Further slave controllers or interrupt sources can be added via the S-100 vectored interrupt lines. Most of the board’s options can be selected by dipswitch, and there are several pin jumpers for other options.

The boards were subjected to all the normal abuses, such as fast clock rates and high ambient temperatures, and performed flawlessly.

The decision to spread the CPU and system management functions over two boards is a sound one. Both are uncluttered, easy to configure and run cool. The two-board approach also gives the user some flexibility in upgrading existing systems. The CPU Support Board could be used by any processor, although it might duplicate one or more of the functions found on the popular 8-bit CPU cards. It’s also possible to use someone else’s support card with the 8086 card, such as Godbout’s new System Support 1.
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16K STANDARD RAM — this fully static RAM is frequently used by OEMs in systems which do not require bank select. High reliability, low noise design. Uses 200 nsec. chips. Addressable to any continuous 16K on 4K boundaries. Any 4K block may be disabled. Prices: 1-9, $265; 10-19, $245.

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SCP Review, cont'd...

Seattle has been producing rock-solid memory boards for as long as they have been in business. The 8/16 RAM follows in that tradition, providing a sixteen bit data path for fastest performance in an 8086 environment. As the name implies, it can be used as an 8-bit memory as well. It appears as either 16K of 8-bit memory or 8K of 16-bit memory. Each card can be addressed anywhere in the 16 Megabyte S-100 address space and can be set to respond to PHANTOM*. They are fully static and use the standard 4044 memory chip.

As with the boards mentioned previously, these boards are models of spacious layout and clean design. The boards provided for the review were subjected to all the normal abuses, such as fast clock rates and high ambient temperatures, and performed flawlessly. The 6 MHz Z-80B actually places more demands on them during instruction fetch cycles than the 8086 does at 8 MHz in any operation mode. They proved to be a match for the worst conditions I could provide in several system environments.

Software

Over the months that I've had the Seattle system for review, the software has been a living, growing thing. I received an early copy of 86-DOS and have received several updates. Then there was a long delay while we waited for Microsoft to modify stand-alone Basic-86 to run under 86-DOS. The conversion was finally done by Seattle Computer Products, with help from Microsoft.

86-DOS is similar enough to CP/M to make you feel at home, but different enough to get you into trouble if you assume that it's really the same. It is conceptually similar, but the differences could be considered departures or enhancements, depending on your point of view. The fact that there are so many good ideas within a framework familiar to the user shows that SCP has some good software people with minicomputer exposure, as well as talented hardware designers.

Typical of the enhancements is the line editor built into the command line interpreter. It uses the DECVT52 function key escape sequences to permit the last line entered to be edited and resubmitted—just the thing when you make dumb typographical errors and you really don't feel like re-entering the entire line. It's also handy when the next command you are going to enter differs by only a few characters from the last command entered. Also, the file copy utility is memory-resident, which saves you the time required to load PIP. The control characters have essentially the same effect except that a control-N is required to un-toggle the printer after a control-P has started it.

The utility software provided includes a resident 8086 assembler, a line-oriented editor, a CP/M to 86-DOS file converter, a Z-80 to 8086 source code converter and a breakpointing debugger. I did not spend much time with the assembler or line editor, but the editor is just as bad as any other line editor I have attempted to use. The Z-80 to 8086 source code converter is interesting. It does a fairly good job until it gets to special Z-80 instructions like block I/O and some of the extra register functions. At this point you have to code by hand. I cannot attest to the relative efficiency of the 8086 code generated because I'm not sufficiently conversant with its instruction set.

The debugger is as good as any of the general-purpose debuggers to be found in the 8-bit world. It loads only object files (no HEX) and, as the manual points out, it will even trace ROM. Every instruction is traced correctly, unlike most 8080 and Z80 debuggers. It doesn't do anything fancy like using a symbol table, but what good is a program like ZSID when the thing misinterprets the object code? The debugger also includes a disk read and write capability.

All of the development tools are important, but the real thing that makes a new processor go is the availability of high level languages. The 8086 languages are coming on strong and Microsoft was there first with Stand-alone Disk Basic-86. With the conversion chronicled above, SCP became the first manufacturer to offer the full hardware, operating system and high level support of an 8086 on the S-100 bus. Virtually anything that is written for the 8080 Microsoft Basic interpreter will run on the 8086 interpreter, but it will go faster because of the higher clock rate and throughput of the 16-bit machine.

The manuals are oriented toward the experienced microcomputerist, particularly one who is graduating from an 8-bit processor in the S-100 world.

Documentation

Before we go on to a comparison of execution times between the 8-bit and 16-bit worlds, a few words are in order about documentation. The folks at SCP have been conscientious in keeping current owners updated with new manuals and releases. Most of the material I received from them had a "Dear User" flavor, giving no indication of preferential status as a reviewer. The manuals are complete, clear and well written, but they are definitely oriented toward the experienced microcomputerist, particularly one who is graduating from a 8-bit processor in the S-100 world. They convey enough information for an experienced person to get the system configured and running, but I think that a relative newcomer or an Apple-wizard would be somewhat bewildered. More examples and pictorials of option switch settings would be helpful.

The one manual in which pictorials are used is the 8/16 RAM manual. Unfortunately, they are a total failure. The artist selected strange trapezoidal directional indicators for the dipswitches which have confused everyone to whom I have shown them.

Comparisons

Aside from those who always have to have the best, newest or fastest computer equipment, there are a limited number of reasons why a user would select a high performance 16-bit system over a high performance 8-bit system. There is no doubt in anyone's mind that the 8086 can move data around faster than even a 6 MHz Z-80, especially when the data path is 16 bits wide. All the standard benchmarks peg the 8 MHz 8086 as having five times the throughput of a 4 MHz Z-80, so all your programs will run five times faster, right?
SCP Review, cont’d…

I wish it was that simple. The real stumbling block is software, not CPU speed. I ran “known quantity” programs that I had written in Microsoft Basic on both machines and found some interesting results. I should point out that I use Basic-80 strictly as a development tool for the Basic Compiler, which represents a plateau of efficiency for 8-bit high level languages, since only PL/I-80 (to the best of my knowledge) produces faster object code. Now, you may object and say that it’s unfair to compare a Compiler and an interpreter even when the CPU is five times faster, but we’re talking about reasons to buy the 16-bit machine. The software state-of-the-art is a major factor.

First, let’s state the facts: Basic-80 is definitely slower than Basic-86. If throughput in executing interpreted Basic programs was the sole criterion, there would be no contest. The second fact is that the Basic Compiler does everything faster than Basic-80, and here again, there is definitely no contest. Its slowest functions, such as string concatenation, are still three or four times faster than the interpreter. Its fastest operations, such as integer arithmetic, are up to twenty times faster than the interpreter.

So when we benchmark the 8086-based interpreter against the compiler, what do we find? We find the compiler still faster in most instances. One exception is string concatenation, which was actually faster than the compiler in the tests I made. This should not be a surprise, because large portions of Basic-86 appear to be translated 8080 code. By no means does this suggest that you shouldn’t consider buying an 8086-based system. Can you imagine how fast a Basic-86 compiler or PL/I-86 will be? Or how much less contention will be experienced in a multi-user environment? Once software becomes available that is well optimized for the 8086, the performance will be remarkable.

By the way, for my fellow hardware freaks, there is a switch on the CPU board which limits it to 8-bit data transfers. It allows you to demonstrate the degree of throughput gain you get with the 16-bit data transfers. What with slogging through all the code in the Basic interpreters, I noticed very little difference between the 8086 in 8-bit mode and a 4 MHz Z-80. For that matter, there was no discernible difference in the operation of Basic-80 with a 4 MHz Z-80 and a 6 MHz Z-80. The 8086 in 16-bit mode was sufficiently faster than 8-bit mode to be noticeable, but the difference was not breathtaking. Again, the quality of the software being executed has a major effect on how efficient the processor will appear.

Conclusions

The conclusion I have drawn from living with the 8086 for a number of months is that the SCP hardware is an excellent foundation upon which to build your entry into the 16-bit world. It is solid, reliable stuff and their software works. (This cannot be said of all manufacturers who create their own operating and utility software.) The availability of Basic-86 is a tremendous convenience, one that bodes well for the future. As an OEM/systems integrator, I’m sure that I will use the 8086 in a commercial system in the not-to-distant future.

First, however, I’ll need WordStar-86, MDBS-86 and all the other “spoilers” which make life in the 8-bit world so enjoyable. The advent of 16-bit high level language compilers will be the crowning touch. Then, look out DEC, Hewlett Packard, et al.
System Product Review

Alpha Micro System Revisited

by Hank Kee

Background

The Alpha Micro system was originally introduced in December of 1976. It has been around for so long that many of us have tended to overlook the system as the first 16-bit system available on the S-100 bus. This system is often used as the benchmark for all other microcomputer systems. It was originally advertised and promoted to the hobbyist in various microcomputer journals. However, they now are no longer selling "direct" to the general public but prefer to sell through dealers. The main thrust of their dealers' selling efforts today is to the "small" commercial business user.

There are well over 5,000 Alpha Micro systems running; last year the company reported sales of over 21 million. There is also a very active Alpha Micro users group called AMUS (c/o Steve Elliot, Front Range Computer, 1966 13th St., Boulder CO 80306).

The system is based on the conceptual architecture of the LSI series designed by Digital Equipment Corporation. The smallest basic configuration (eight systems are available) consists of a two-board CPU (AM-100), a six port serial I/O board (AM-300), and a floppy disk controller (AM-210) interfacing to CDC drives. A hard disk cartridge system (CDC Hawk or Phoenix) could be added for greater disk storage capacities (360 Mbytes maximum). Additional available equipment includes 8.5 Mbyte Winchester and 9 track 1/2" tape peripherals. There are now variations of these boards with different options. Further, both serial and parallel pointers (300, 600 or 900 LPM) with two spoolers are supported. This review is necessarily confined to their original product offerings only because of limited access to their hardware.

Overall Architecture

The AM-100 CPU consists of two boards populated by a five chip set micro-encoded processor manufactured by Western Digital. Western Digital was the original manufacturer of the LSI series for DEC. The AM-100 CPU contains hardware floating-point math. The mnemonic code of the AM-100 is essentially the same as the LSI series, but they differ at the object code level. The Alpha Micro has an improved instruction set compared to the LSI. Assembler source code from the LSI can be easily converted onto the Alpha Micro. A separate 8 to 10 VAC is required to generate the real-time clock pulse. This could be easily tapped off the power supply of the main frame transformer prior to it being rectified into DC.

The AM-210 is the floppy disk controller which has the addition of a Z80 processor. This allows for an interrupt driven operating system. Unlike many other micro based disk systems, interrupts on the Alpha Micro need not be disabled during disk operations. The user can key-in ahead instead of waiting for the system to poll for character input. The original system I worked on interfaced to either Persci 277 or Wangco 76 8" drives. The floppy disk system currently offered by Alpha Micro uses CDC drives and the AM-210 controller. The CDC's are dual-sided double density units. The current floppy disk systems offered by Alpha Micro now has over 2MBytes available to the user.

The functions of I/O are handled by the AM-300 six serial port board. An AM-310 is also sold to those who wish to interface synchronous as well as asynchronous devices to the Alpha Micro.

To complete the basic system, a Pioceon 64K dynamic memory board is available. Up to eight memory boards may be installed for a maximum of 512K of memory. This board has optional parity checking features. I have tried numerous other bank select dynamic memories. Only the Piocion, which was recommended by Alpha Micro, works. An alternative is to use static memories with bank select. Memory boards need not be rated any faster than 460 nanoseconds. Each additional concurrent user requires about 32K of memory. As the number of concurrent users increases, so will the number of memory boards. The use of static memories tend to cause system heat build-up.

Alpha Micro also offers the CDC Hawk cartridge hard disk system on the AM-500 hard disk controller. The drive comes with 5Mbytes of fixed and 5Mbytes of removable storage. Winchester technology without removable media is high risk on small business systems. Alpha Micro does not sell their AM-500 hard disk controller card separate from the CDC Hawk drive. Many owners contract with CDC for monthly service maintenance of
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the Hawk drive, but would prefer owning an extra disk controller card for the purposes of backup. Konan now sells a compatible disk controller (KNX-500). Instead of using the Z80 for data transfer functions, the Konan board uses the 8085. I have found the Konan controller to be an acceptable substitute.

All Alpha Micro manufactured boards, with the exception of the AM-100, can be used with existing S-100 boards for CP/M operation. (Alpha-Micro does not support CP/M on their systems.) BIOS Coding is generally available. The Konan KNX-500 is also supplied with BIOS coding.

Other “foreign” S-100 boards can be successfully included as part of the overall configuration. You will need an Alpha Micro system, though, to initialize other devices. Alpha Micro has included as part of their software, drivers for boards of many other S-100 manufacturers. Non-Alpha Micro boards, however, tend to be non-interrupt driven. The easiest and most efficient configuration is the basic system as offered by Alpha Micro. Originally the Alpha Micro was designed to work with the Tarbell disk controller along with the Imsai SIO or Processor Tech VDM boards.

Alpha Micro has since introduced the AM-100T (about a year and a half ago). This CPU uses a 16-bit address structure, as opposed to 8-bit address architecture. It run substantially faster than the AM-100.

It is possible to interface as many as 22 concurrent users onto the system using their hard disk systems. But I have found degradation of response becomes significant when there are more than a half-dozen or so users on the system. The size of available user storage decreases as the operating system increases to reflect the greater number of concurrent users.

Software Availability

The greatest asset of the Alpha Micro system is that the software is bundled with the purchase of hardware. Many of their software systems are excellent. The AMOS (Alpha Micro Operating System) includes a superb multi-user Alpha Basic in either interpretive or compiler mode. Alpha-Pascal, Alpha-Lisp, and a screen oriented editor (VUE). Rather than dwell on how the operating system works, it suffices to say that it is equivalent to a DEC system running RT-11. For those of you who are familiar with CP/M, it works very much like CP/M. Since CP/M is a variant of RT-11, it might be more equitable to say that AMOS and CP/M are similar to DEC’s RT-11.

AMOS assigns disk space by project ID’s. The operating system ID contains all the system level commands. The user may elect to add customized calls or eliminate others from this space if they are not referenced. This allows for a very small kernel operating system to be resident in memory. Commonly accessed system modules such as the Basic runtime package can be made resident in memory and available to all users. The Basic compiler and runtime modules are reentrant. The typical operating system would use about 32K bytes of memory. Only 64K of memory can be referenced at any one time by the user, including space required by AMOS. AMOS, in its design, permits shared reentrant code. Most of Alpha Micro’s software can be made resident and reentrant. Basic generates reentrant user code.

There is password control on the Alpha Micro for each user of the system. A master account is available for unrestricted access. Instead of comparing this to CP/M, it is really a superset of MP/M.

Basic for the Alpha Micro is very powerful. The compiler can generate reentrant code for access by multi-users. It even tells the user how much time it took to compile a program. Available on this system is the capability to “MAP” variables, very much like COBOL. This allows the programmer to reference overlay areas of the same field with ease. Basic can also be used in interpretive mode. Variable names are not limited to two or three characters. They can be defined to be much more meaningful since up to 31 characters may be used.

Some Alpha Micro dealers have since added the capability to accept data from CP/M or IBM floppy disk formats. Utility programs are provided to perform these functions. Similar routines have been included to transform AMOS oriented formats into CP/M or IBM compatible data structures.

The Alpha Micro system has an excellent method for systems generation. A SYSTEM.INI file is created by the user defining configuration to be generated at dynamic boot-time. It is very easy to modify the operating system to include additional equipment. Having worked with CP/M, AMOS is superior to implement. AMOS also has facilities for running a modified system initialization without affecting the original SYSTEM.INI file.

The Alpha Micro System is the Rolls Royce of S-100 systems.

Alpha-Pascal is an enhanced UCSD Pascal with multi-user, multi-tasking features. Alpha Micro also offers LISP. FORTRAN, COBAL and APL are available from other sources and Alpha Micro dealers. I have not had an opportunity to explore these systems.

If you are interested in running packaged business software, your choices are limited. Alpha Micro offers an Accounting Package which includes the functions of accounts payable/receivable, general ledger, payroll, and inventory and order control.

Almost everyone I know who has implemented this “system” indicates that modifications are very extensive. It is not what one would call an easily adaptable turnkey business application system.

With the exception of the Alpha Micro Accounting System, the abovementioned software comes with the purchase of hardware. A variety of legal, medical, and other type packages are available from Alpha Micro dealers.

The software documentation supplied with the system is very good and quite complete. It is relatively easy to understand. The program reference materials are not tutorial in nature. These were meant to be of assistance to users who have a first-hand working knowledge of programming systems.

Reliability

The system has certain quirks. When running the Alpha Micro in multi-user mode, it is possible for one user to
bring down all other users due to addressing of out-of-bounds memory or hardware “bus” failure. There is no form of hardware protection. In general, running production programs in multi-user mode will be of no problem. But it is advised that application development should not be running concurrent with production processing. During the past two years, I have experienced various board problems with the system. These are typical of past experiences I have had with other microcomputer boards. The only difference is that the repairs require returning the malfunctioning board(s) to an Alpha Micro dealer for servicing. Schematics are not available to the end-user. This arrangement is not always practical in terms of turn-around time. For business environments, it is almost mandatory to configure an overall system with sufficient back-up boards. This is expensive and sometimes not possible.

Conclusion:
The Alpha Micro system is the Rolls Royce of S-100 systems. The manufacturer’s selling and maintenance policies however, are restrictive. Small business systems have been successfully designed around the Alpha Micro, but one must almost duplicate a total system to insure continual processing of business. For high performance, it will compete on its own against typical “minicomputer” suppliers. For the general hobbyist, the Alpha Micro may tend to get a little too rich.

Prices for the system are set by dealers and vary depending the configuration and value added by the dealers. Prices range typically from $10,000 to $15,000.
Well, by now it seems like you've always had that Z80A running at "4 Meg," and the full 64K of high-speed RAM you got to go with it has collected a nice layer of dust since you haven't changed a board in months. Your bank account is finally recuperating from the purchase of that double sided double density disk system you bought a few months back. Right about now, you're congratulating yourself on finally putting together a state-of-the-art system. Guess again! The 16-bit micros have finally come alive, with enough off-the-shelf hardware and software available to make assembling a 16-bit S-100 system a reasonable project for an experienced microcomputerist.

For the past few months I have had the opportunity to install and use Godbout's 8085/8088 Dual Processor Board with Digital Research's new 8086 implementation of the CP/M operating system. The hardware and software were received in their standard, unconfigured form. I was thus able to experience the installation of this new processor and operating system on an existing system. Through this report, I hope to convey to you my impression of these two powerful and exciting new tools.

A Quick Look
The Godbout Dual processor, as the name implies, contains an 8085 microprocessor for the execution of existing 8080-family software, along with an 8088 microprocessor for the execution of the newer 8086-family software. The system powers up with the 8085 active. By means of a software command, the user may then switch back and forth between it and the 8088. This is accomplished by an input command to an I/O port, whose address is switch selectable on the card. An output to the same I/O port sets the value of extended address lines A16 through A23, allowing the 8085 to overcome its normal 64 kilobyte addressing limits and access all 16 megabytes defined by the IEEE-696 standard. Only the upper four bits of this port are used when the 8088 is active, since this processor has built-in addressing for 1 megabyte.

The 8085 chip is basically an enhanced 8080, which eliminates the clock generator chip and negative power supply required for an 8080 system. It also practically eliminates the need for an interrupt controller chip in systems requiring interrupts, since input pins and vectoring hardware are provided on the processor for four new interrupts, in addition to the non-vectorized interrupt carried over from the original 8080. One of these, the Non-Maskable Interrupt, is brought out to the newly-defined NMI pin of the S-100 bus. The remaining three new interrupts, which are maskable in software, may be jumpered to any of the eight S-100 vectored interrupt pins. These new interrupts are referred to as RST 5.5, RST 6.5 and RST 7.5, since they generate calls to addresses 4 bytes above the original 8080's RST 5, RST 6 and RST 7 instructions. The 8085 instruction set is identical to that of the 8080, with the addition of two instructions to enable and disable the three new maskable interrupts. It is important to note that the additional Z80 instruction set is not implemented. A premium version of the 8085 is used on the Godbout board, allowing operation with a 5 MHz clock rate. A switch is provided to drop the 8085's speed to 2 MHz, to accommodate older (and slower) memory boards.

The 8088 contains pipeline logic which will fetch up to the next four memory bytes while the current instruction is being decoded and executed.

The 8088 microprocessor chip represents Intel's recognition of the large number of microprocessor users who would like to upgrade to a 16-bit microprocessor without having to convert all their 8-bit bus hardware and peripherals. The result is an 8086 processor which has been internally modified to convert each 16-bit memory or port access into two sequential 8-bit accesses.
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The 8088 contains pipeline logic which will fetch up to the next four memory bytes while the current instruction is being decoded and executed. Internal operations may therefore proceed at full 16-bit speed, resulting in an overall execution speed almost equivalent to that obtainable on a true 16-bit bus. The bus timing for memory accesses was also made somewhat more liberal, with the result that an 8088 operating a 5 MHz (as on Godbout’s board) will work with most memory designed for 2 or 3 MHz 8-bit systems, without the need to add wait states. Godbout apparently found this to be true, since no means is provided to slow the 8088’s 5 MHz clock.

CP/M-86 is Digital Research’s first venture into the 16-bit micro software market. It implements the same basic file structure, utilities and commands as the current version (2.2) of 8-bit CP/M. Disks written by the two disk systems are fully interchangeable, as long as the same disk definitions are used in the 8- and 16-bit BIOSes. 8086 equivalents of all the standard CP/M utilities such as ASM, PIP, ED and DDT are provided. Those programs necessary to configure the system (such as the 8086 assembler) are also provided in 8080-executable form. This should allow the use of an existing CP/M-80 system to develop and install a CP/M-86 BIOS. All the CP/M-80 version 2.2 BDOS calls are present and use the same function numbers, easing the task of converting existing programs. New BDOS functions have been added to provide controlled access to the 8086 memory management features.

Testing
Two system configurations were used to test the hardware and software. The main one consisted of a non-front panel enclosure, containing a Vector motherboard, an Imsai SIO2-2 serial interface, an iCom 3712 8-inch single density diskette subsystem, and 64K of various brands and speeds of static RAM. It should be pointed out that some of the memory was already known not to operate with a 4 MHz Z80A. The iCom disk system seemed like a good choice for a first attempt at bringing up CP/M-86, since it used a buffered controller and simple parallel interface with no wait state insertion or special timing requirements. The second test system was an Imsai 8080 front-panel type system, containing the original Imsai motherboard, two SSM 104 I/O boards for serial I/O, 64K of fast static RAM and an Industrial Micro Systems 400 diskette controller. This configuration allowed me to test the Godbout board’s operation in the potentially troublesome areas of DMA (on the IMS controller) and front panel operation. Time did not permit installing CP/M-86 on the second system, so the software part of this review is based on operation with the iCom disks only.

Hardware Evaluation
The Godbout board gives a very good first impression as it comes out of its shipping carton. The layout appears clean and open, in spite of the fact that the board contains over 40 IC’s. The two five volt regulators sit on the left side (where the vents are on most S-100 cabinets), balanced by the two 40-pin microprocessor IC’s on the right. In the upper right corner is a 16-pin DIP socket for the optional connection to a front panel. Card ejectors are provided in the upper corners of the board (I wish more manufacturers would provide these, as they prevent skinned knuckles when changing cards in a tight motherboard). The board is solder-masked on both sides, and appears to have been wave-soldered. The silkscreened legends on the component side of the board identify each IC by both its sequential number in the schematic, as well as its generic type number (7400, 8085, etc.). Each option switch (and there are many) has its function clearly marked. One minor annoyance is the absence of metal “fingers” on the unused S-100 connector pins. The high cost of gold plating has caused a lot of manufacturers to omit these, but the result is that the motherboard sockets become dirty sooner, and the user is prevented from making any hardware modifications that might have required the additional pins.

While there are a great many option switches to be set on this board, most are more or less self-explanatory. In either case, the manual explains them in detail and shows the most common initial setup. A large red toggle switch near the upper right corner of the board selects between 2 MHz and 5 MHz operation of the 8085 processor (the 8088 is fixed at 5 MHz). There are three sets of 8 DIP switches. The one in the bottom row selects the I/O port number used to control the processor. An output to this port sets the extended address lines. An input returns meaningless data, but causes control to switch from the current processor to the other one. I set this to the recommended value of OFD hex. The middle set of switches sets the address for the power-on-jump logic to any 256-byte boundary. I used the address of the disk boot PROM in each of my systems. The last set of switches, located near the top of the board, control miscellaneous options. These include: whether to disable the extended address lines during DMA, whether to clear the extended address lines (to all 0’s) at each reset, whether to insert wait states in all I/O operations, whether to reset each processor every time it becomes active or let it continue from where it was, whether to do a jump on reset, whether to do a power-on-jump, and whether to generate the S-100 MWRITE signal. I selected power-on-jump and jump-on-reset in both systems. MWRITE generation was required only in the non-front panel system, since the front panel of my Imsai does its own generation of this signal. I selected the “continue” mode of operation for both processors. However, I did install an additional jumper, described in an addendum to the manual, which allowed the bus reset button to affect both processors, rather than just the 8085. I discovered through experimentation that the I/O wait option was only necessary when operating the 8085 at 5 MHz. All my I/O devices seemed to work fine without wait states when the 8088 was in control.

I was quite pleased with the operation of the board in both systems. Once the correct options were set up, the board performed flawlessly. I have run just about every popular CP/M-based language and package on the 8085 section of the board without any problems. Once potential “catch” concerns operation of the board with DMA devices: due to the manner in which the processor changeover is accomplished, one cannot use the “reset or changeover” option when DMA devices are present, since the DMA is seen as a processor changeover and causes a reset to occur. This should pose no problem in running CP/M-86, since the reset feature is not required.
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Godbout & CP/M-86 Review, cont’d…

By now I’m sure some of you are saying “but why couldn’t they have used a Z80 instead of the 8085?” The reason is simple—there is a great similarity between the timing of the 8085 and 8088 processors. Intel did this to make it easy for their industrial users to adapt existing 8085 designs to the 8088. In the case of the Godbout board, it allows the two processors to share most of the S-100 bus interface logic. Since the timing of the Z80 is vastly different, it probably would have necessitated two totally separate interface circuits, which would not have fit on a single S-100 card. There may be some hope, however, National Semiconductor makes a processor called the NSC800, which they claim has the Z80 instruction set, but timing similar to an 8085. Unfortunately, the NSC800 and the 8085 are not pin-compatible, so some wiring changes would be necessary. Also, the chip seems to be in relatively short supply. Maybe someone at Godbout should be looking into the use of this chip in some future revision to the board (are you listening, Mr. G?).

The first thing that struck me about CP/M-86 was the remarkable degree of similarity to CP/M-80 in both the user and system levels of interface.

There is really only one feature of this board that in my opinion does not live up to expectations. That is the “powerful memory management” alluded to in the company’s advertising. What is actually provided on the board would be more accurately called “centralized bank switching.” There is a single parallel port with its outputs connected to S-100 address lines 16 through 23 (when the 8085 is in control) or 20 through 23 (when the 8088 is in control). The trouble with this simple scheme is that the output instruction which sets the extended address lines must be executed from a memory card that doesn’t recognize the extended address. Otherwise, the program would be knocking its own memory out from under itself! This is not much of a problem when running 8-bit software such as MP/M, which requires some non-banked memory for parts of the operating system anyway. It is also not a serious problem for the 8088, since the CPU directly addresses a megabyte before bank switching is required. The hassle comes when the two processors are used together, if the 8085 needs to access memory above the first 64K to perform some task for the 8088. An example would be the setting up of the 8088’s reset vector (at address 0FFFF0 hex) prior to switching control from 8085 to 8088. The non-extended memory required to perform this operation would require a gap the size of the non-extended card to be left in each 64K of the 8088’s one megabyte space, reducing the maximum size of each 8088 memory segment by the size of the non-extended card. A possible solution to the specific problem of starting up the 8088 is to use a PROM monitor in the extended address space. Alternatively, the extended PROM could simply contain a jump instruction to somewhere in the first 64K, making extended references by the 8085 unnecessary. In any event, I would hope that future processors adopt some true form of address translation or mapping so that practical use may be made of the full addressing capabilities of the S-100 bus.

Software Evaluation

The first thing that struck me about CP/M-86 was the remarkable degree of similarity to CP/M-80 in both the user and system level of interface. This consistency helped me to immediately feel at home, in spite of the fact that I was on a brand new processor and operating system. The software comes on two 6 inch single density floppies. A looseleaf binder contains copies of the CP/M 2.2 Users Guide, the ED Users Manual and An Introduction to CP/M Features and Facilities, all of which are the same manuals supplied with the CP/M-80. Three new manuals provided are the CP/M-86 System Reference Guide, the CP/M-86 Assembler Users Guide, and the DDT-86 Users Guide. The System Reference appears to be the equivalent of both the “Interface Guide” and “Alteration Guide” found in the CP/M-80 documentation package. These manuals seem to be best organized for looking things up rather than reading straight through. All the necessary information is presented in a well organized manner, with several example programs provided both in the appendices and on the release diskettes. There is a great deal of information presented, but it does all fall into place quickly.

CP/M-86 is larger than CP/M-80, and therefore does not fit on the two system tracks of a standard diskette. Instead, it sits in a file called CPM.SYS. An abbreviated version of the system occupies the system tracks, and is used to load the system file during boot-up. Unlike CP/M-80, the system is not reloaded every time a program exits. Control-C issued to a running program simply causes a return to the CCP prompt. Control-C to the CCP causes the disks to be re-logged in. CP/M-86 takes advantage of the inherent relocatability of 8086 object code. The system may be loaded anywhere in memory without the need for a MOVCSPM-like program. The normal procedure is to boot the system into address 00400 hex, just above the 8086 interrupt vector area. This leaves memory from about 02A00 and up free for loading programs.

In CP/M-86, the familiar .COM file type for executable code has been replaced by a new .CMD file type. Besides denoting the presence of 8086 object code rather than 8080, the .CMD file has a header record that describes the program’s space requirements for code, data and stack space. This results in much more compact program storage on disk. A new utility called GENCMD is used to create .CMD files from the extended hex (.H86) files produced by the assembler. This replaces the LOAD program found in a CP/M-80 system. The executable files thus produced may use one of three memory configurations: the “8080 model,” in which code and data are given a single memory area of up to 64K, the “small model,” where two separate areas of up to 64K each are allotted for code and data, or the “compact model,” in which up to eight separate memory areas of up to 64K each may be allocated for code and data. The necessary configuration is determined automatically by the system from the information contained in the .CMD header record.
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David Gerrold is the author of "The Trouble With Tribbles," an episode of Star Trek. He has written almost a dozen novels, including When Harlie Was One and The Man Who Folded Himself. He has been nominated for the Hugo and Nebula Awards a total of seven times.

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The interface between a program and the system has been modified slightly. The page 0 BIOS and BDOS vectors of CP/M-80 have been done away with. Instead, the 8086 software interrupt instruction is used to perform BDOS calls. Since there is no more "warm boot vector" at location 0 for performing direct BIOS calls, a new BIOS function has been added for direct access to all the BIOS routines. The IOBYTE has been moved from location 0003 into the BIOS, with two new calls added to read and set it. Instead of an absolute page 0, the first page of the program's data segment is used by the system to pass the amount of available memory, the default FCB's, and the default I/O buffer. When the "8080 model" configuration is used, this will result in a setup nearly identical to CP/M-80. Due to the absence of a warm boot vector, program termination via "jmp 0" is no longer possible. The program must do a BDOS function 0, or an 8086 "return far" instruction to exit back to the operating system.

CP/M-86 contains added BDOS functions to handle the 8086's memory segmentation features. An added BIOS function allows you specify a table of up to eight non-contiguous areas of memory for programs and data. This allows you to bypass any ROM or other dead blocks in your system. CP/M-86 will then further divide the areas you specify if necessary to provide a total of up to eight separate memory segments. New BDOS calls are provided to allow a program to request additional memory, and to request another program to be loaded. This means that programs may call each other in nested fashion up to eight levels deep.

The CP/M built-in commands remain just about the same as before. DIR, ERA, REN, TYPE and USER operate identically to CP/M-80. The SAVE command has been done away with, however, due to the confusion that it would cause in a segmented memory environment (how would you know which area to save?). Instead of SAVE, a Write command has been added to DDT for saving patched object files. The other noticeable difference at the keyboard is that control-P is no longer canceled when a program terminates or control-C is typed. It will remain in effect indefinitely, until another control-P is typed. This greatly improves your ability to get hardcopy of your console output.

I found installing my first CP/M-86 to be much easier than what I recall of my first few attempts with CP/M-80 back in the days of version 1.3. I simply took a listing of my current CP/M-80 BIOS, hand-translated the disk and console portions into 8086 mnemonics, and edited them into the CP/M-86 BIOS skeleton provided on one of the release diskettes. I then used the thoughtfully-provided ASM86.COM to assemble the new BIOS on the 8085 and CP/M-80. Because of the relocatability of 8086 code, there are no equates in the BIOS for memory size (although there is the aforementioned table of available memory areas), and the whole mess of calculating load offsets for DDT has been eliminated. One simply used PIP to concatenate the provided CPM.H86, which contains the CCP and BDOS, with your just-assembled CBIOS.H86. GENCMD.COM, an 8080-executable version of the CP/M-86 program loader, is used to turn the combined hex file into an 8086 object file. At this point came the big question: "Now that I've got it, how do I boot this thing?"

This is where having both processors on one board really paid off. I simply wrote a short preamble for CPM.SYS in 8085 code, which set the 8086 reset vector to jump to the 8086 BIOS and then switched processors. Voila! A CP/M-86 system that executes as a CP/M-80.COM file. As a finishing touch, I would later make this the embedded command in my CP/M-80 system, so that I could appear to boot straight into CP/M-86.

With the details of starting up the system worked out, it was time to begin testing. I keyed in the command "CPM86" (I had saved the 8086 system with the 8085 preamble as CPM86.COM) and waited. In a few seconds, I was quite tickled to see the message: CP/M-86 Version 1.0

System Generated 03/15/81

and then...

Nothing! The system had printed the signon and then hung up somewhere. Well, let's see. Since the signon printed, the console routines must be working, so the problem must be somewhere in the disk logic, when it goes to log in drive A. The code looks OK, so what am I missing? Wait a minute! Let's have a look at that iCom schematic. Just as I suspected, it's decoding the port number from the upper address bus. This is a common problem on older S-100 boards, where the layout designer took advantage of the fact that the 8080 duplicates the I/O port number on address lines 8 through 15. Most S-100 280 cards have extra logic to perform this function, so there's no problem there, but what do you do on a processor like the 8088 that allows port numbers greater than 255? (In fact, the 8088 uses 16 address bits for port numbers, allowing 64K of I/O ports.) Well, back into CP/M-80, and find a way to make it work. Aha! I can write the 8066 code using 16-bit port numbers that have the same lower and upper byte. That should keep all the old boards happy. The only drawback is that to get the 16-bit port numbers requires loading the CX register with the port number before each I/O instruction, since that's the only means provided on the 8088 for accessing the higher port numbers. Anyway, a few quick edits, reassemble and try it again. This time, the system signs on, and I get the familiar "A " prompt. Fantastic! I type "DIR", and the system responds (a bit more rapidly than CP/M-80, I believe) with a proper directory listing. TYPE also seems to be doing its thing. OK, I know the disk read logic must be working, so the next step is to try to write a file. In this case, I tried to PIP something into another file. No go. After I reboot the system, I can see the new name that was created in the directory, so it must be almost working. Examination of the disk write code showed that I had forgotten to pop a register, so I fixed that and tried again. Still just as bad! At this point, I got an object lesson on the effect of the segment registers. I had changed the data segment register in order to obtain the data to be written from the calling program's data segment. Since I forgot to set it back to my own data segment, all further references to my BIOS variables were coming from somewhere south of Lower Slobbovia! Another well-placed push/pop pair and disk writes started behaving themselves. There I finally was, with a real live and working CP/M-86 system! I then used the working CP/M-86 system to further enhance the CBIOS with a handshaking list driver for my Diablo printer, and various other minor bells and whistles. Once I had set up...
YOUR CHOICE OF OVER 1 OR 2 MBYTES ON-LINE REMOVABLE STORAGE:

<table>
<thead>
<tr>
<th>MODEL</th>
<th>DESCRIPTION</th>
<th>COMPARABLE RETAIL PRICE</th>
<th>DATA COMPASS RETAIL PRICE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-47</td>
<td>Dual-Drive 8&quot; Floppy Disk System featuring &quot;Intelligent&quot;-master and slave drives in compact 13-1/2&quot; wide cabinet with write-protect switches and indicators, built-in power supply, fan and cable. Includes complete technical manual. Fully assembled and tested. (115 VAC, 60Hz Std., 230 VAC, 50 Hz optional.) Total capacity: over 2 Mbytes formatted on-line removable storage.</td>
<td>$3500.</td>
<td>$2395</td>
</tr>
<tr>
<td>1-47 (1)</td>
<td>Same as 1-47 above except with (1) 8&quot; &quot;Intelligent&quot; master drive only. Fully assembled and tested. Total capacity: over 1 Mbyte formatted on-line removable storage. (Model 4820 slave drive can be added later for $733 to double capacity.)</td>
<td>N/A</td>
<td>$1695</td>
</tr>
<tr>
<td>S-100</td>
<td>Industry standard (IEEE 696) S-100 Interface</td>
<td>$225.</td>
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</table>

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Godbout & CP/M-86 Review, cont'd...

CPM86.COM for auto-execute from CP/M-80, I was ready to log some program development time. The difference in speed between the .COM and .CMD versions of ASM86 was immediately noticeable, although not quite as great as I would have expected. GENCMD was drastically improved, with the .COM version seeming to take forever, while the .CMD was about as fast as the CP/M-80 LOAD program. ED, PIP and STAT all seemed slightly faster, while SUBMIT seemed about the same. One can reasonably assume that compute-bound programs will benefit the most, especially if they are partially rewritten to take advantage of the 8088's added instruction set. Disk-bound programs are of course limited by the disk transfer rate and won't show much improvement.

As a final example, I converted my Super Directory program from the SIG/M library into 8086 code. This program contained many opportunities to take advantage of the 8068, since it contains a character-string sort routine and a large number of 16-bit computations. I recoded the sort routine to use the 8086 string-compare routine, thereby eliminating about twenty lines of code. I changed the decimal output routine to use the hardware divide instruction, shortening that code. The ability to store constants directly into memory, as well as the ability to increment and decrement memory directly, without the use of a pointer register, were very useful throughout the program. The index registers and multiple bit shifts were also put to good use. The end result of my work on BIOS and SD appears at the end of this article, and will be available on a SIG/M library diskette at some later date as part of a collection of 8086 programs.

The one program which requires a bit of getting used to is the 8086 assembler, ASM86. As was stated in the manuals, this assembler is mostly faithful to the Intel standard in mnemonics and basic design. The main area of deviation is that inter-segment jumps, calls and returns have unique mnemonics rather than being detected automatically. The tricky part of the Intel standard is that the code generated when a particular identifier is used depends on how that identifier was defined. If it was defined by an EQU, for example, it is treated as a numeric literal and generates an immediate-mode instruction. The label of a DB instruction causes an 8-bit instruction to be generated wherever it is referenced, while DW's cause 16-bit instructions to be generated. Code labels cannot be used in data-reference instructions, and will produce an error message from the assembler. One "feature" which does not seem to be mentioned in the manuals is that code labels must be followed by a colon (:), while data labels must not be, and will cause error messages at every reference to that label. While this is no problem when writing new code, it caused a bit of head-scratching at first when converting existing programs. Also, for some reason the "jump carry" (jc) and "jump not carry" (jnc) opcodes seem to be missing from the assembler. Once again, this is only a problem with existing code, since the synonyms "jump below" (jb) and "jump above or equal" (jae) are present and work properly.

Conclusions

In spite of some of the minor problems mentioned here, both the hardware and software tested appear to be solid, reliable tools which may be had at a very reasonable cost. The dual board makes it possible to step up to 16 bits without sacrificing any existing hardware, or having to swap CPU cards to run 8-bit software. Likewise, CP/M-86 allows a smooth upgrade to 16-bit programming without the need to learn a totally new operating environment. Given the similarity between the 8086/88 and 8080/Z80 architectures, combined with the familiarity of CP/M, most programmers and their software should make the transition with ease. Digital Research is to be congratulated for once again providing a standard-setting product that will provide a consolidated market for the software of the 1980's.

With these products and the others which will now surely follow, 16-bit computing has finally arrived!

Programs begin on page 40.
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title 'Customized Basic I/O System'

* This customized BIOS adapts CP/M-86 to the following hardware configuration:
  * Processor: 8085/8088 Dual Processor
  * Brand: CompuPro (Godbout)
  * Controller: ICom 3712

* Programmer: Bruce R. Ratoff
* Revisions: 04/30/86 20:40

** Bios Jump Vector for Individual Routines **

<table>
<thead>
<tr>
<th>ccpp</th>
<th>org</th>
<th>ccpg offset</th>
<th>org</th>
<th>Bios code</th>
</tr>
</thead>
<tbody>
<tr>
<td>2500</td>
<td>09</td>
<td>3C 00</td>
<td>2501</td>
<td>E9 00</td>
</tr>
<tr>
<td>2506</td>
<td>E9 08</td>
<td>C8 00</td>
<td>2507</td>
<td>E9 CE 00</td>
</tr>
<tr>
<td>250C</td>
<td>E9 D5 00</td>
<td>250F</td>
<td>E9 DD 00</td>
<td></td>
</tr>
<tr>
<td>2512</td>
<td>E9 20 01</td>
<td>2513</td>
<td>E9 1E 01</td>
<td></td>
</tr>
<tr>
<td>2518</td>
<td>E9 54 01</td>
<td>251B</td>
<td>E9 32 01</td>
<td></td>
</tr>
<tr>
<td>251D</td>
<td>E9 51 01</td>
<td>2521</td>
<td>E9 58 01</td>
<td></td>
</tr>
<tr>
<td>2524</td>
<td>E9 61 01</td>
<td>2527</td>
<td>E9 6C 01</td>
<td></td>
</tr>
<tr>
<td>252B</td>
<td>E9 59 01</td>
<td>2532</td>
<td>E9 1E 01</td>
<td></td>
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<tr>
<td>253B</td>
<td>E9 FE 00</td>
<td>253C</td>
<td>E9 FC 00</td>
<td></td>
</tr>
<tr>
<td>2540</td>
<td>E9 3C 00</td>
<td>2541</td>
<td>RC C8</td>
<td></td>
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<tr>
<td>2542</td>
<td>08</td>
<td>DC 00</td>
<td>2545</td>
<td>BE CO</td>
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<td>2546</td>
<td>BE 00 00</td>
<td>2549</td>
<td>BE 29</td>
<td></td>
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<tr>
<td>254A</td>
<td>FC</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>2553</td>
<td>C6 06</td>
<td></td>
<td></td>
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<tr>
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<td>BE 00</td>
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<tr>
<td>2555</td>
<td>BE 08</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2556</td>
<td>BE C0</td>
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** I/O Port Assignments **

<table>
<thead>
<tr>
<th>Port</th>
<th>Assigment</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>Loader BIOS equ false</td>
</tr>
<tr>
<td>08E0</td>
<td>BDOS int equ 224 reserved BDOS interrupt</td>
</tr>
</tbody>
</table>

** Diskette Interface (ICom 3712) **

* Note: Port numbers are "doubled up" because ICom card counts on 880 "address mirror" effect.

<table>
<thead>
<tr>
<th>Port</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0002</td>
<td>Data equ 4 ;data status input port</td>
</tr>
<tr>
<td>0003</td>
<td>Input ready mask</td>
</tr>
<tr>
<td>0004</td>
<td>Output ready mask</td>
</tr>
<tr>
<td>2500</td>
<td>BIOS code equ 2500h</td>
</tr>
<tr>
<td>0806</td>
<td>BDOS offset equ 0806h ;BDOS entry point</td>
</tr>
</tbody>
</table>

** Console Interface (IMSAI SI02-2 port 1) **

<table>
<thead>
<tr>
<th>Port</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0005</td>
<td>Status equ 1 ;status</td>
</tr>
<tr>
<td>0006</td>
<td>Data equ 2 ;data</td>
</tr>
<tr>
<td>0007</td>
<td>Input ready mask</td>
</tr>
<tr>
<td>2508</td>
<td>BDOS offset equ 0806h ;BDOS entry point</td>
</tr>
</tbody>
</table>

** Printer Interface (IMSAI SI02-2 port 2) **

<table>
<thead>
<tr>
<th>Port</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0018</td>
<td>Status equ 1 ;status</td>
</tr>
<tr>
<td>0019</td>
<td>Data equ 2 ;data</td>
</tr>
<tr>
<td>2509</td>
<td>BDOS offset equ 0806h ;BDOS entry point</td>
</tr>
</tbody>
</table>

** BIOS Entry Point, Differs for LDBIOS and BIOS, according to "Loader BIOS" value **

INIT ENTRY POINT:

<table>
<thead>
<tr>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Print signon message and initialize hardware</td>
</tr>
<tr>
<td>Setup all interrupt vectors in low memory to address traps</td>
</tr>
<tr>
<td>Local stack during initialization</td>
</tr>
<tr>
<td>Setup interrupt 0 to address trap routine</td>
</tr>
<tr>
<td>Move into offset, offset int trap</td>
</tr>
<tr>
<td>Move into segment, CS</td>
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<tr>
<td>Move ss,ax</td>
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<tr>
<td>Set ES and DS to zero</td>
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<tr>
<td>Propagate interrupt 0 to address trap routine</td>
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<td>Move ss,ax</td>
</tr>
<tr>
<td>Set ES and DS to zero</td>
</tr>
<tr>
<td>Propagate interrupt 0 to address trap route</td>
</tr>
</tbody>
</table>
PHEX:

CALL PHEX

CONOUT:

; This is a BIOS for the LOADER
mav bx,offset signon
mov ax,0
mov ds,ax
; BDOS interrupt offset
mov bxds offset, bds offset
mov bxds segment,cs
; BDOS interrupt segment

; (additional LOADER initialization)
POP DX
; restore data segment

ENDIF: ; loader bias

IF not loader bias

ENDIF: ; not loader bias

**C P/M Character I/O Interface Routines**

**CP/M Character I/O Interface Routines**

; INT 1A: \texttt{AP} \texttt{CR} \texttt{LF} \texttt{ESC} \texttt{DLE} \texttt{BEL} \texttt{FS} \texttt{GS} \texttt{RS} \texttt{US} \texttt{XOM}

**LISTOUT:**

; list device output

**READER:**

; read character

**PUNCH:**

; write punch device

**SETIOBF:**

; set input character flag

**LISTSTL:**

; list status

**CONOUT:**

; console output

; default to drive A on coldstart

; now print digit

; get high nibble

; print digit into low bits

; block interrupts

; get output data segment

; get status byte

; set status byte

; check input mask

; not ready yet...return al=0, ZF=1

; return al=OFFH, ZF=0

; ret

; ret

**CONIN:**

; console input

**LISTTST:**

; list status

; poll status

; not ready...exit with al=0, zf=1

; move al,active

; set list active flag

**LISTOUT:**

; list device output

**LISTSTL:**

; list status

; poll status

; not ready...exit with al=0, zf=1

; move al,active

; set list active flag

**SETIOBF:**

; set input character flag

**LISTSTL:**

; list status

; poll status

; not ready...exit with al=0, zf=1

; move al,active

; set list active flag

**CONOUT:**

; console output

; default to drive A on coldstart

; now print digit

; get high nibble

; print digit into low bits

; block interrupts

; get output data segment

; get status byte

; set status byte

; check input mask

; not ready yet...return al=0, ZF=1

; return al=OFFH, ZF=0

; ret

; ret

**CONIN:**

; console input

**LISTTST:**

; list status

; poll status

; not ready...exit with al=0, zf=1

; move al,active

; set list active flag

**SETIOBF:**

; set input character flag

**LISTSTL:**

; list status

; poll status

; not ready...exit with al=0, zf=1

; move al,active

; set list active flag

**CONOUT:**

; console output

; default to drive A on coldstart

; now print digit

; get high nibble

; print digit into low bits

; block interrupts

; get output data segment

; get status byte

; set status byte

; check input mask

; not ready yet...return al=0, ZF=1

; return al=OFFH, ZF=0

; ret

; ret
**Disk Input/Output Routines**

READ:

0082
2650 C6 66 6D 27 FF mov cx,0
2655 88 6E 6E 27 FF mov cl,0
2659 BB 60 60 00
265C BB F9 00
265P 73 6D mov cl,0
2661 BB 66 00 mov cl,0
2663 BB 6D 0D mov cl,0
2665 BB 64 64 mov cl,0
2667 BB 63 63 mov cl,0
2669 BB 56 28
266C BB 33 C9
2668 BB 00 00
2669 BB 00 00
266D BB 00 00
266E BB 00 00
266F BB 00 00
2670 BB 00 00
2672 BB 00 00
2673 BB 00 00
2674 BB 00 00
2675 BB 00 00
2676 BB 00 00
2677 BB 00 00
2678 BB 00 00
2679 BB 00 00
267A BB 00 00
267B BB 00 00
267C BB 00 00
267D BB 00 00
267E BB 00 00
267F BB 00 00
2680 BB 00 00
2681 BB 00 00
2682 BB 00 00
2683 BB 00 00
2684 BB 00 00
2685 BB 00 00
2686 BB 00 00
2687 BB 00 00
2688 BB 00 00
2689 BB 00 00
268A BB 00 00
268B BB 00 00
268C BB 00 00
268D BB 00 00
268E BB 00 00
268F BB 00 00
2690 BB 00 00
2691 BB 00 00
2692 BB 00 00
2693 BB 00 00
2694 BB 00 00
2695 BB 00 00
2696 BB 00 00
2697 BB 00 00
2698 BB 00 00
2699 BB 00 00
269A BB 00 00
269B BB 00 00
269C BB 00 00
269D BB 00 00
269E BB 00 00
269F BB 00 00
26A0 BB 00 00
26A1 BB 00 00
26A2 BB 00 00

**Disk Utility Routines**

WRITE:

0272 89 0E 69 27 FF mov cx,0
0276 C6 66 6D 27 FF mov cl,0
027B C3
027C 89 0E 91 27 FF
0280 C3

**Microsystems**
This routine issues a controller command and waits for completion.

DLOOP:
move dx,ctr1
send command

out dx,al

; strobe it off

LOOP1:
in al,ds
get controller status

test ax,al
check ready bit

jnz LOOP1
loop till ready
ret
then exit

This routine issues a "clear" command followed by a "home" command.

RESET:
move al,00h
send "clear"

call DLOOP

mov dl,0
send "home"

jmps DLOOP

; System Memory Segment Table

segtable db 1 ; segment
dw tpa seg ; list seg starts after BIOS
dw tpa len ; and extends to Offh

include singles.lib ; read in disk definitions

; DISKS 2

dbase equ 0

dp0 dw x100,000h ; BASE of Disk Parameter Blocks

dp0 dw x100,000h ; Translate Table

dp0 dw x100,000h ; Scratch Area

dp0 dw x100,000h ; Dir Buff, Parm Block

dp0 dw csv,al ; Check, Alloc Vectors

dp0 dw x100,000h ; Dir Buff, Parm Block

dp0 dw csv,al ; Check, Alloc Vectors

; DISKDEF 0,1,26,6,1024,243,64,64,2

; 1944: 128 Byte Record Capacity

; 243: Kilobyte Drive Capacity
SUPER DIRECTORY PROGRAM

by Bruce R. Ratoff

Displays the directory of a CP/M disk, sorted alphabetically, with the file size in K, rounded to the nearest CP/M block size.

This latest variation on a common theme will automatically adjust itself for any block size and directory length. If the screen fills, the program will pause until a key is struck (see NPL and LPS equates below). Total space used and number of files are printed at end.

Command: SD FILENAME:FILETYPE or just SD

Allows '*' or '?' type specifications. Drive name may also be specified. Ignores 'SYS' files unless SOPT is TRUE and 'S' option is given (i.e., SD *.S will print all files). 05/05/81 Fixed division overflow problem in decimal output routine. 

05/03/81 First 8086 version. (Bruce R. Ratoff)

Based on 'DIRS' by Keith Peterson, W8SDZ

False EQU 0 ;Define logical false

True EQU NOT False ;Define logical true

Opt EQU 05 ;Number of names per line

Delim EQU 1 ;Delimiter character

Wid EQU 128 ;Widest directory entry

Topt EQU 5CH ;Number of sectors per track

Topt EQU 2 ;Number of lines per screen

Win EQU 4 ;Number of names per line

Endif EQU true ;End if

SOPT EQU 1 ;Put true to allow 'DIR . ' or S FORM

Across EQU 4 ;Print all names across if not user

User EQU 16 ;User or 'PY' option

Delim EQU 1 ;Delimiter character

Put EQU 2 ;Put true to allow 4 names across

User EQU 1 ;Print user names for cp/m 2.x also

Tpa EQU 5CH ;Check size

Tpa EQU 105 ;Translate table

Alloc EQU 16 ;Check vector size

Allocation Vector Size

Equivalent Parameters

Same Checksum Vector Size

Same Translate Table

Same Allocation Vector Size

Same Checksum Vector Size

Translations Table

Same Checksum Vector Size

Same Translate Table

Same Allocation Vector Size

Same Checksum Vector Size
NEW! TPM* for TRS-80 Model II
NEW! System/6 Package
Computer Design Labs

Software with Manual/Manual Alone

All of the software below is available on any of the following systems with a 250 CP/M using the CP/M* or similar type disk operating system (such as our own TPM*).

for TRS-80 CP/M (Model I or II)
for 5" CP/M (soft sectored single density)
for 5½" CP/M (soft sectored single density)
for 5½" North Star CP/M (single density)
for 5½" North Star CP/M (double density)

BASIC I

A powerful and fast Z80 Basic interpreter with EDIT, RENUMBER, TRACE, PRINT USING, assembly language subroutine CALL, LOADDO for "chaining", ODPI to modify EXCHG, KILL, LINE INPUT, error inter-cept, sequential file handling in both ASCII and binary formats, and much, much more. It runs in a little over 12 K. An excellent choice for games since the precision was limited to 7 digits in order to make it one of the fastest around. $49.85/$15.

BASIC II

Basic I but with 12 digit precision to make its power available to the business world with only a slight sacrifice in speed. Still runs faster than most other Basics (seven times with most precision). $99.85/$15.

BUSINESS BASIC

The most powerful Basic for business applications. It adds to Basic I with random or sequential files in either fixed or variable record lengths, simultaneous access to multiple disk files, PRIVACY command to prohibit user access to source code, global editing, added math functions, and disk file maintenance capability without leaving Basic (list, rename, or delete). $179.95/$25.

ZEDIT

A character oriented text editor with 26 commands and "macro" capability for stringing multiple commands together. Included are a complete array of character move, add, delete, and display functions. $49.95/$15.

ZTEL

Z80 Text Editing Language - Not just a text editor. Actually a language which allows you to edit text and also write, save, and recall programs which manipulate text. Commands include conditional branching, subroutine calls, iteration, block move, expression evaluation, and much more. Contains 36 value registers and 10 text registers. Be creative! Manipulate text with commands you write using Ztel. $79.95/$25.

TOP

A Z80 Text Output Processor which will do text formatting for manuals, documents, and other word processing jobs. Works with any text editor. Does justification, page numbering, spaced, centered, and much more! $79.95/$25.

MACRO I

A macro assembler which will generate relocatable or absolute code for the 6800 or Z80 using standard Intel mnemonics plus TDL/Z80 extensions. Functions include 14 conditionals, 16 listing controls, 54 pseudo instructions, 11 arithmetic/logical operations, local and global symbols, chaining files, linking capability with optional link and recursive/reiterative macros. This assembler is so powerful you'll think it's doing all the work for you. It actually makes assembly language programming much less of an effort and more creative. $79.95/$20.

MACRO II

Expands upon Macro I's linking capability (which is useful but somewhat limited) thereby being able to take full advantage of the optional Linker. Also a time and date function has been added and the listing capability improved. $99.95/$25.

LINKER

How many times have you written the same subroutine in each new program? Top notch professional programmers compile a library of these subroutines and use a Linker to tie them together at assembly time. Development time is thus drastically reduced and becomes comparable to writing in a high level language but with all the speed of assembly language. So, get the new CDL Linker and start writing programs in a fraction of the time it took before. Linker is compatible with Macro II as well as TDL/Xitan assemblers version 2.0 or later. $79.95/$20.

DEBUG I

Many programmers give up on writing in assembly language even though they know their programs would be faster and more powerful. To them assembly language seems difficult to understand and follow, as well as being a nightmare to debug. Well, not with proper tools like Debug I. With Debug I you can easily follow the flow of any Z80 or 8080 program. Trace the program one step at a time or 10 steps or whatever you like. At each step you will be able to see the instruction executed and what it did. If desired, modifications can then be made before continuing. It's all under your control. You can even skip displaying a subroutine call and up to seven breakpoints can be set during execution. Use of Debug I can pay for itself many times over by saving you valuable debugging time. $79.95/$20.

DEBUG II

This is an expanded debugger which has all of the features of Debug I plus many more. You can "trap" (i.e. trace a program until a set of register, flag, and/or memory conditions occur). Also, instructions may be entered and executed immediately. This makes it easy to learn new instructions by examining registers/memory before and after. And a RADI function allows changing between ASCII, binary, decimal, hex, octal, signed decimal, or split octal. All these features and more are added to give you a very powerful debugging tool. Both Debug I and II must run on a Z80 but will debug both Z80 and 8080 code. $99.85/$20.

APPLE

A Z80 executive and debug monitor. Capable of search, ASCII put and display, and read and write to I/O ports, hex math, breakpoint, execute, move, fill display, read and write in Intel or binary format tape, and more! on disk $34.95/$15.

NEW! TPM now available for TRS-80 Model II

ZAPPLE

A Z80 executive and debug monitor. Capable of search, ASCII put and display, and read and write to I/O ports, hex math, breakpoint, execute, move, fill display, read and write in Intel or binary format tape, and more! on disk $34.95/$15.

SYSTEM MONITOR BOARD (SMB II)

A complete I/O board for TRS·80 systems. 2 serial ports, 2 parallel ports, 1200/2400 baud cassette tape interface, sockets for 2K of RAM, 3-2708/2716 EPROM's or ROM, jump on reset circuity. Bare board $49.95/$20.

ROM FOR SMB II

2K8 masked ROM of Zapple monitor. Includes source listing $34.95/$15.

PAYROLL (source code only)

The Osborne package. Requires C Basic 2. 5½ disks $124.95 (manual not included) 8½ disks $ 99.95 (manual not included) Manual $20.00

ACCOUNTS PAYABLE/RECEIVABLE (source code only)

By Osborne, Requires C Basic 2. 5½ disks $124.95 (manual not included) 8½ disks $ 99.95 (manual not included) Manual $20.00

GENERAL LEDGER (source code only)

By Osborne, Requires C Basic 2. 5½ disks $99.95 (manual not included) 8½ disks $99.95 (manual not included) Manual $20.00

C BASIC 2

Required for Osborne software. $99.95/$20.

SYSTEM/S

TPM with utilities, Basic I interpreter, Basic E compiler, Macro I assembler, Debug I debugger, and ZEDIT text editor.

Above purchased separately costs $339.75 Special introductory offer Only $179.75 with coupon!!

SERVICE INQUIRY INVITED.

Many CDL products are available for licensing to OEMs. Write to Carl Galletti with your requirements.

ORDERING INFORMATION

Visa, Master Charge and C.O.D. OK. To order call or write with the following information.

1. Name of Product (e.g. Macro I)
2. Media (e.g. 8" CP/M)
3. Price and method of payment (e.g. C.O.D.) include credit card info. if applicable.
4. Name, Address and Phone number.
5. For TPM orders only: Indicate if for TRS-80, Tarbell, Xitan DDDC, SD Sales (5½ or 8"), ICOM (5½ or 8"), North Star (single or double density) or Digital (Micro) Systems.
6. N.J. residents add 5% sales tax.

Manual cost applicable against price of subsequent software purchase in any item except for the Osborne software.

For information and tech queries call 609-599-2146
For phone orders ONLY call toll free 1-800-327-9191 Ext. 676

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CARL GALLETTI & ROGER AMIDON, Owners

342 Columbus Avenue
Trenton, N.J. 08629

MICROSYSTEMS

49
16-Bit Microcomputer Disk Operating Systems

by Sol Libes

The following is a compilation of Disk Operating System (DOS) packages currently available for 16-bit microprocessor-based computer systems. While most can be purchased separately from hardware, the XENIX and 9900 Disc Executive packages cannot. These two have been included because they are, or are expected to be, implemented on S-100 based systems. There are many other 16-bit DOS packages currently on the market that I have not included here because they are furnished only as part of turnkey systems which are not S-100 based.

I was amazed to find that there are already fourteen suppliers furnishing 27 different 16-bit DOS packages that range from low cost (typically $450) single-user development DOS, all the way up to a 32 user system capable of handling 256 tasks.

Naturally, the 8086, being the oldest of the current generation of 16-bit microprocessors, has the largest number of available packages, many of which have been in use for well over a year. Most of the Z8000 and 68000 DOS listed were not yet released when my questionnaire was returned by the company.

Reviews of two 8086 DOS packages appear in this issue of Microsystems (CP/M-86 and Seattle Computer Products' DOS). We plan to review some of the Z8000 and 68000 DOS in future issues. Readers interested in writing such reviews should contact me.

16-Bit Microcomputer DOS Suppliers

Seattle Computer Products
1114 Industry Dr.
Seattle, WA 98188

Telecomute Systems, Inc.
251 Spadina Ave.
Toronto, Ont.
Canada M5T 2E2

Industrial Programming, Inc.
100 Jericho Quadrangle
Jericho, NY 11753

Onyx Systems, Inc.
73 East Trimble Rd.
San Jose, CA 75132

Marinchip Systems Ltd.
16 St. Jude Rd.
Mill Valley, CA 94941

Central Data Corp.
713 Edgebrook Dr.
Champaign, IL 61820

Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 95051

Hemenway Associates
101 Tremont St.
Boston, MA 02108

Central Systems, Inc.
1317 Central Ave.
Kansas City, KS 66102

TSC
Box 2570
W. Lafayette, IN 47906

Microsoft
10800 NE 8th St.
Bellevue, WA 98004

Digital Research
801 Lighthouse Rd.
Pacific Grove, CA 93950

Phase One Systems, Inc.
770 Edgewater Dr.
Suite 710
Oakland, CA 94621

Systems & Software, Inc.
2801 Finley Rd.
Donners Grove, IL 60515
### 8086/8088 Disk Operating Systems

<table>
<thead>
<tr>
<th>DOS Name</th>
<th>86-DOS</th>
<th>CP/M-86</th>
<th>MP/M-86</th>
<th>IRMX88</th>
<th>IRMX86</th>
<th>MTOS-86</th>
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<td>Vendor</td>
<td>Seattle Computer</td>
<td>Digital Research</td>
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<td>Intel Corp.</td>
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<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DOS Name</th>
<th>MSP/8086</th>
<th>SP/8086</th>
<th>OASIS-8086</th>
<th>REX-80</th>
<th>XENIX-8086</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vendor</td>
<td>Hemenway</td>
<td>Hemenway</td>
<td>Phase One Sys.</td>
<td>Systems &amp; Software</td>
<td>Microsoft</td>
</tr>
<tr>
<td>Price</td>
<td>$750</td>
<td>$500</td>
<td>$1495</td>
<td>$3750</td>
<td>?</td>
</tr>
<tr>
<td>Size</td>
<td>32K</td>
<td>16K</td>
<td>64K</td>
<td>4K min.</td>
<td>82K min.</td>
</tr>
<tr>
<td>Maximum number of:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Users</td>
<td>1</td>
<td>1</td>
<td>32</td>
<td>User configurable</td>
<td>4 to 20</td>
</tr>
<tr>
<td>CPU's</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Tasks</td>
<td>8 in 32K</td>
<td>1</td>
<td>256</td>
<td>any number</td>
<td>20 to 100</td>
</tr>
<tr>
<td>Network Protocols</td>
<td>yes</td>
<td>yes</td>
<td>none</td>
<td>none</td>
<td>yes</td>
</tr>
<tr>
<td>Real Time Provisions</td>
<td>yes</td>
<td>yes</td>
<td>128 max.</td>
<td>yes</td>
<td>limited</td>
</tr>
<tr>
<td>Memory Size (Max.)</td>
<td>1M</td>
<td>1M</td>
<td>1M</td>
<td>1M</td>
<td>1M min.</td>
</tr>
<tr>
<td>Disk Storage (Max.)</td>
<td>80M</td>
<td>80M</td>
<td>2.8M/Vol. 32 Volumes</td>
<td>User option</td>
<td>2M min.</td>
</tr>
<tr>
<td>Supports: Floppy Disk</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Hard Disk</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>CRT</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Printer</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Line Printer</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Other</td>
<td>paper tape</td>
<td>paper tape</td>
<td>Mag. tape Cartridge tape</td>
<td>A/D &amp; D/A</td>
<td>-</td>
</tr>
<tr>
<td>Comments:</td>
<td>Includes Macro Assembler, Linking Loader, Basic &amp; Pascal</td>
<td>Includes Macro Assembler, Linking Loader, Basic &amp; Pascal</td>
<td>Supports bubble memory</td>
<td>Supports 8087 math processor and PL/M.</td>
<td>Expanded version of Labs UNIX Ver. 7.</td>
</tr>
</tbody>
</table>

Note: K = Kilobytes; M = Megabytes; G = Gigabytes
<table>
<thead>
<tr>
<th>DOS Name</th>
<th>ZMOS</th>
<th>SP/Z8000</th>
<th>XENIX-Z8000</th>
<th>ONIX</th>
<th>OASIS-Z8000</th>
<th>MSP/Z8000</th>
<th>Z8000 Disc Executive</th>
<th>TIS-APL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vendor</td>
<td>Central Data</td>
<td>Hemenway</td>
<td>Microsoft</td>
<td>Onyx Systems</td>
<td>Phase One</td>
<td>Hemenway</td>
<td>Marinchip</td>
<td>Telecompute Sys.</td>
</tr>
<tr>
<td>Price</td>
<td>$450</td>
<td>$500</td>
<td>?</td>
<td>$1500 (4 users)</td>
<td>$1495</td>
<td>$750</td>
<td>$500</td>
<td>$840</td>
</tr>
<tr>
<td>Size</td>
<td>96K</td>
<td>16K</td>
<td>82K min.</td>
<td>80K</td>
<td>64K</td>
<td>32K</td>
<td>9K</td>
<td>30K</td>
</tr>
<tr>
<td>Maximum number of:</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Users</td>
<td>32</td>
<td>1</td>
<td>4 to 20</td>
<td>8</td>
<td>32</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>CPU's</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Tasks</td>
<td>175</td>
<td>1</td>
<td>20 to 100</td>
<td>255</td>
<td>256</td>
<td>8 in 32K</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Network Protocols</td>
<td>none</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>none</td>
<td>yes</td>
</tr>
<tr>
<td>Real Time Provisions</td>
<td>none</td>
<td>yes</td>
<td>limited</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>none</td>
<td>N/A</td>
</tr>
<tr>
<td>Memory Size (Max.)</td>
<td>16M</td>
<td>8M</td>
<td>1M min.</td>
<td>1M</td>
<td>16M</td>
<td>16M</td>
<td>64K</td>
<td>256K</td>
</tr>
<tr>
<td>Disk Storage (Max.)</td>
<td>250M</td>
<td>80M</td>
<td>2M min.</td>
<td>10-40M</td>
<td>2.8M/Vol. 32 Volumes</td>
<td>80M</td>
<td>4M</td>
<td>120M</td>
</tr>
<tr>
<td>Supports:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Floppy Disk</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Hard Disk</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>CRT</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Printer</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Line Printer</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Other</td>
<td>—</td>
<td>Paper Tape</td>
<td>—</td>
<td>—</td>
<td>Mag. Tape</td>
<td>Paper Tape</td>
<td>—</td>
<td>A/D &amp; D/A</td>
</tr>
<tr>
<td>Comments:</td>
<td>Works with CDC memory management hardware.</td>
<td>Includes Macro Assembler, Linking Loader, Basic and Pascal.</td>
<td>Expanded version of Bell Labs UNIX Ver. 7.</td>
<td>Based on Bell Labs UNIX.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:** K = Kilobytes  M = Megabytes  G = Gegabytes
### 68000 Disk Operating Systems

<table>
<thead>
<tr>
<th>DOS Name</th>
<th>MSP/68000</th>
<th>SP/68000</th>
<th>MTOS-68K</th>
<th>UniFLEX</th>
<th>UNIX</th>
<th>XENIX-68000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vendor</td>
<td>Hemenway</td>
<td>Hemenway</td>
<td>Industrial Prog.</td>
<td>TSC</td>
<td>Control Systems</td>
<td>Microsoft</td>
</tr>
<tr>
<td>Price</td>
<td>$750</td>
<td>$500</td>
<td>$9500</td>
<td>$800</td>
<td>not yet set</td>
<td></td>
</tr>
<tr>
<td>Size</td>
<td>32K</td>
<td>16K</td>
<td>8K</td>
<td>32K</td>
<td>128K</td>
<td>82K min.</td>
</tr>
<tr>
<td>Maximum Number of:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Users</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Any number</td>
<td>50</td>
<td>4 to 20</td>
</tr>
<tr>
<td>CPU's</td>
<td>1</td>
<td>1</td>
<td>16</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Tasks</td>
<td>8 in 32 K</td>
<td>1</td>
<td>Any number</td>
<td>Any number</td>
<td>Any number</td>
<td>20 to 100</td>
</tr>
<tr>
<td>Network Protocols</td>
<td>yes</td>
<td>yes</td>
<td>X-25</td>
<td>none</td>
<td>optional</td>
<td>yes</td>
</tr>
<tr>
<td>Real Time Provisions</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>none</td>
<td>60 Hz Interrupt</td>
<td>limited</td>
</tr>
<tr>
<td>Memory Size (Max.)</td>
<td>16M</td>
<td>8M</td>
<td>16M</td>
<td>8M</td>
<td>?</td>
<td>1M min.</td>
</tr>
<tr>
<td>Disk Storage (Max.)</td>
<td>80M</td>
<td>80M</td>
<td>4 single-sided double density floppies</td>
<td>unlimited 8M/drive</td>
<td>?</td>
<td>2M min.</td>
</tr>
<tr>
<td>Supports:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Floppy Disk</td>
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<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Hard Disk</td>
<td>yes</td>
<td>yes</td>
<td>no</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>CRT</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Printer</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Line Printer</td>
<td>yes</td>
<td>yes</td>
<td>paper tape</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Other</td>
<td>paper tape</td>
<td>paper tape</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

**Note:** K = Kilobytes  M = Megabytes  G = Gigabytes

### 9900 Disk Operating System

<table>
<thead>
<tr>
<th>DOS Name</th>
<th>M9900 Disc Executive</th>
<th>NOS/MT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vendor</td>
<td>Marinchip</td>
<td>Marinchip</td>
</tr>
<tr>
<td>Price</td>
<td>included with hardware</td>
<td>$250</td>
</tr>
<tr>
<td>Size</td>
<td>9K</td>
<td>16-36K</td>
</tr>
<tr>
<td>Maximum Number of:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Users</td>
<td>1</td>
<td>any number</td>
</tr>
<tr>
<td>CPU's</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Tasks</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Network Protocols</td>
<td>none</td>
<td>none</td>
</tr>
<tr>
<td>Real Time</td>
<td>user provides</td>
<td>no</td>
</tr>
<tr>
<td>Provisions</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory Size (Max.)</td>
<td>60K</td>
<td>56K/user</td>
</tr>
<tr>
<td>Disk Storage (Max.)</td>
<td>4M</td>
<td>no limit</td>
</tr>
<tr>
<td>Supports:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Floppy Disk</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Hard Disk</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>CRT</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Printer</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Line Printer</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>Other</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Comments:</td>
<td>Requires Marinchip hardware.</td>
<td>Requires Marinchip hardware. I/O drive source supplied. Includes Assembler, Editor, Linker, Basic, Utilities, Output processor. Completely user config-  670.0x670.0urable.</td>
</tr>
</tbody>
</table>

**Note:** K = Kilobytes  M = Megabytes  G = Gigabytes
Input Queuing For North Star Double Density

by Robert T. Armstrong

As a lawyer from 'Down Under' I have been using a North Star system for bookkeeping purposes for over two years. The basic programs I wrote have been annoying because after inputing various values the system took some seconds to process that data, update running balances and write results to disk. Inputing and operating time was wasted.

The problem was aggravated when the delay caused the disk drive to stop; then after inputing the drive had to build up speed again—a minor matter—but seconds add up. I kept taking comfort in the hope that 'shortly' a compiler for North Star Basic would become available.

My interest was aroused by the articles Queueing and Polling in the May 1979 edition of Byte.

The question was how to ensure that the keyboard was checked 'often' while a North Star basic program was running? Two facilities are available:

• First, Basic regularly checks through the 'contc' routine to see whether a control C (to stop the basic program) has been depressed. This is accessed regularly except when a disk access is taking place.

• Second, double density DOS has available an 'often' routine which is called at least once every 40 milliseconds—no doubt incorporated for this very purpose.

The North Star manual gives us warning of the only problem (but, of course I did not read it carefully and had to find out for myself) and this is that 'often' will be called at bootstrap load time, even before the 2900H personalization block is loaded. The answer is to originally patch a 'return' and change this to 'jump' in the initialization routine.

A full listing of alterations to DOS is enclosed, the procedure for double density would be:
1. "LF DOS 5000 {CR}"—put present DOS at 5000H.
2. Bytes 2007H-2018H in my list to be loaded at 5007H-5018H.
3. Bytes 2900H-29FFH in my list to be loaded at 5800H-58FFH.
4. 'SF DOS 5000 {CR}'—get new DOS from 5000H. This technique has cut operator input time considerably, and will hold a maximum of 32 characters in queue, more than enough for bookkeeping purposes.
The character is output twice. Once when put in queue and again when the system (basic) takes it from the queue.

At any time the following keys have special uses:

Control E—jump to bootstrap load at E800H
Control O—jump to DOS
Control B—non destructive jump to basic
Control R—'run' basic program

I still look forward to a compiler. There are no doubt thousands of good working North Star basic programs in the field—all debugged and finalized—but which would welcome the extra speed of a compiler. But in the meanwhile this queueing technique is saving us a lot of time.

Robert T. Armstrong, P.O. Box 263, Toronto, Australia 2283

```
2007 ORG 2007H ;DOS
2007 C9 RET 2007H ;ORIGINALY 'RETURN'
2008 2729 DW OFTEN ;AFTER INIT THEN JUMP TO OFTEN
200A C36220 JMP 2062H
200D C31C29 JMP CONSOOUT
2010 C35F29 JMP CONSin
2013 C30829 JMP INIT
2016 C33329 JMP CONTC

2900 ORG 2900H ;TOP RAM TO HOLD 1ST IN QUEUE
29FF = 1Q IQU 29FFH ;PLACE FOR NEXT IN QUEUE LHLD-SHLD
2900 00 TEMP DB 0
2901 FF29 Q DW 1 ;PLACE FOR NEXT IN QUEUE LHLD-SHLD
2903 AE40AE3700DATA DB 0AEH,40H,0AEH,37H,0

2908 210229 INIT LXI H,DATA-1
290B 23 INIT1 INX H
```

MICROSYSTEMS
LOAD TRS-80 software on your S-100 Z-80 or your money back!!! Of the 501,000 home computers in this country more than 200,000 are TRS-80's. Look through your magazines and you will see that there is more software available for the TRS-80 than all other computers combined. Here is what we offer:

1) An assembled hardware interface and software drive which will enable you to load data from TRS-80 cassette tapes into your S-100 memory.

2) Complete documentation telling you how to relocate the program at its correct address, find the entry point to the program, and link the program to your keyboard input and video output routines.

3) Includes examples of how we interfaced TRS-80 LEVEL II BASIC and SARGON II with our system.

NOTE: Knowledge of Z-80 Machine Code is required or FREE with purchase of Assembled and Tested Compurism or Super Compurism Unit.

ONLY $30.00

PLUS Expandoram (4MHz) MOD. KIT

PLUS 16 A-D 8-D-A

This S-100 board has 16 channels of analog to digital input and 8 channels of digital to analog output. Enough for most burglar alarm or home energy monitoring systems!! It uses National Semiconductor's ADC0816 sixteen channel analog to digital converter, which is available from DIGI KEY and other mail order houses for about thirty dollars. The total cost of construction including the board and parts should not exceed a hundred dollars. All inputs and outputs are 5 volts. Dual or split power supplies are not required. There is a on-board kluge area for construction of custom circuits.

COMPURISM & SUPER COMPURISM COLOR GRAPHICS

Compurism is a color graphics interface for S-100 Systems, with 16K of on-board dynamic memory. Refresh of the dynamic memory is accomplished on board compurism. (super compurism has 32K of on board dynamic memory) The resolution for compurism is 144 horizontal by 192 vertical pixels. (super compurism resolution is 288 horizontal by 192 vertical pixels). Each byte of memory controls only two pixels of the matrix. Four bits of memory are dedicated to the exclusive control of every single pixel. Therefore, every pixel may always be programmed in any one of sixteen colors or sixteen shades of grey, completely independent of all other pixels in the matrix. (Please compare this to any other color graphics interface in our price range.) From the upper left hand corner to the lower right hand corner of the matrix, the pixels are mapped to consecutive memory bytes. This greatly simplifies the programming of compurism.

COMPURISM SOFTWARE PACKAGE

This new board adds complete hardware and software support for FOUR 8" Single or Double sided drives and FOUR 5" Single or Double Sided, 48TP (40 track) or 96TP (80 track) drives, in addition to the three 5" drives supported by the standard Heath/Zenith controller.

Drive               Double Density Size              Capacity
5" Single Sided     162 KBytes 5" Double Sided     343 KBytes
5" 96TPi, Dbl Sided  700 KBytes 8" Single Sided     594 KBytes
8" Double Sided     1210 KBytes

A total added capacity of up to 7.6 Mega-Bytes of on-line storage!

The price of the software package is ONLY $20.00 or FREE with the purchase of an assembled and tested compurism or super compurism unit.

NOTE: Although we are happy to sell compurism as a bare board we strongly urge the novice or person who feels that they do not have a strong hardware background to purchase an assembled and tested unit.

Compurism Bare Board with documentation ONLY $45.00
Kit - $240.00 Assembled and Tested - $380.00
Super Compurism Bare Board with Documentation ONLY $50.00
Kit - $330.00 Assembled and Tested - $395.00

Add $3.00 to bare board price for hard to find I.C.'s / Add $20.00 to assembled and tested price for memory management port. / Add $20.00 to assembled and tested price for 16 level grey scale option.

J.E.S. GRAPHICS Box 2752 Tulsa, Ok. 74101 (918) 742-7104

TRS-80 is a trademark of TANDY CORPORATION *SARGON II is a trademark of HAYDEN BOOK COMPANY (CHESS program written by DAN and KATHER SPACKLEN)

NEW! for the "89 from MAGNOLIA MICROSYSTEMS

DOUBL E DENSITY DISK CONTROLLER $595

including CP/M™2.2

This new board adds complete hardware and software support for FOUR 8" Single or Double sided drives and FOUR 5" Single or Double Sided, 48TP (40 track) or 96TP (80 track) drives, in addition to the three 5" drives supported by the standard Heath/Zenith controller.

Drive               Double Density Size              Capacity
5" Single Sided     162 KBytes 5" Double Sided     343 KBytes
5" 96TPi, Dbl Sided  700 KBytes 8" Single Sided     594 KBytes
8" Double Sided     1210 KBytes

A total added capacity of up to 7.6 Mega-Bytes of on-line storage!

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Input Queuing, cont'd...

290C 7E  MOV A,M
290D D303 OUT 03 ;INIT CONSOLE
290E D305 OUT 05 ;INIT PRINTER
2911 FE37 CPI 0FH ;IS IT LAST
2913 2C029 JNZ INIT
2915 3E3C MOV A,0CH ; JMP INSTRUCTION FOR 'OFTEN' ROUTINE
2918 2D0720 STA 2D0FH ;RETURN

;INSERT PRINTER OUTPUT ROUTINE AS NECESSARY

291C DB03 CONSOUT IN 03
291E E601 ANI 01
2920 CA2C9 JZ CONSOUT
2923 7E MOV A,B
2924 D302 OUT 02 ;OUT TO CONSOLE
2926 C9 RET

;IS IT THE LAST JMP INSTRUCTION FOR 'OFTEN' ROUTINE

2927 DB03 OFTEN IN 03
2929 E602 ANI 02 ;RETURN IF NO KEY HIT
292B CB RET
292C DB02 IN 02
292E E67F ANI 7FH
2930 3C4129 JMP OPT1

;PUT CHAR IN QUEUE

2933 DB03 CONSOUT IN 03
2935 E602 ANI 02 ;RETURN IF NO KEY HIT
2937 CE03 CPI 03 ;IS IF CONTROL 'C'
2939 03 ;IS IT CONTROL 'c'
293B CB RET ;IF SO RETURN

;PRINT CHAR

2941 D9929 OPTI CALL JUMPS
2944 E5 PUSH H
2945 2A0129 LMLD Q ;GET QUEUE LOCATION
2948 77 MOV M,A
2945 7D MOV A,L
2946 08FH CPI 08FH
294A CE9210 JE 2028H ;IF MORE THAN 32 CHAR IN QUEUE THEN TO 'DOS'
294F DB03 IN 03
2951 E601 ANI 01
2953 CA479 JZ CC1 ;PRINT CHAR @ CONSOLE ONLY
2956 7E MOV A,0H
2957 D302 OUT 02
2959 2B BCT 0H
295A 202129 SHLD Q ;SAVE NEXT QUEUE LOCATION
295D 01 POP H
295E C9 RET

;IS THERE A QUEUE

295F E5 CONSI POP H ;GET QUEUE LOCATION
2960 2A0129 LMLD Q ;RETURN WITH CHAR
2963 7D MOV A,L
2964 EE03 CPI 0FFH ;IS THERE A QUEUE
2968 CE9210 JZ CC2 ;GOTO SPECIAL IF A QUEUE
2969 E1 RET
296A R1 R1
296B 01 POP H
296D E602 JZ CC1
296F E6A429 JNP CC2 ;GET CHAR FROM CONSOLE AS NORMAL
2971 DB02 IN 02
2973 E67F ANI 7FH
2975 C9929 JMP JUMPS ;TO RETURN

;GET QUEUE LOCATION

2978 D5 SPECIAL PUSH D ;TO GET CHAR FROM QUEUE
2979 C5 PUSH B
297A 1FF29 LXI 0,01
297C DB03 LDX Q1 ;THIS IS CHAR TO BE SENT
297E 320029 STA TEMP ;SAVE THIS UNTIL SEND
2980 0A DO LDA D ;MOVE THE QUEUE UP
2984 12 STAX D ;IS THIS LAST CHAR IN QUEUE?
2988 DB DEX B ;IS THIS LAST CHAR IN QUEUE?
2989 D8 DEC B ;IF NOT MOVE REST OF QUEUE UP
298A 7B MOV A,E
298B 2D CMP L ;IS THIS LAST CHAR IN QUEUE?
298C 2B26829 JNZ 00 ;IF NOT MOVE REST OF QUEUE UP
298F 25 INX H
2990 220129 SHLD Q ;SAVE NEXT QUEUE LOCATION
2994 00 POP R
2995 E1 POP R
2999 C3 DB02 LDA TEMP ;RETURN WITH CHAR
299B 02 POP H
299E FE05 CPI 0FH ;IS IT 'O'
29A0 CD0089 JZ 0000H ;GOO BOOSTLOAD
29A3 FE02 CPI 02 ;IS IT 'B'
29A5 CA142D JE 216FH ;GO TO BASIC
29A8 FE12 CPI 12H ;IS IT 'R'
29AA CO RPL
29AC 2D0F7D STA 2D0FH ;RETURN
29AF C3002D JMP 2D00H ;RUN BASIC

;GET NEXT QUEUE LOCATION

29B0 3A0029 LDA TEMP ;RETURN WITH CHAR
29B3 00F7D CALL 00FH ;IS IT 'T'
29B6 CA2820 JE 2028H ;GOO 00
29B9 FE05 CPI 05H ;IS IT 'E'
29BE CD0089 JZ 0000H ;GOO BOOSTLOAD
29C3 FE02 CPI 02 ;IS IT 'B'
29C5 CA142D JE 216FH ;GO TO BASIC
29C8 FE12 CPI 12H ;IS IT 'R'
29CA CO RPL
29CE 2D0F7D STA 2D0FH ;RETURN
29FF C3002D JMP 2D00H ;RUN BASIC
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Variable Speed Automatic Slow Step
For the Imsai 8080

by Joseph W. Long

For some time I had been interested in adding an automatic slow step function to the front panel of an Imsai 8080 computer used by the Chemistry Department at Broome Community College. Getting a look at one of the new Intersystems mainframes (the Electrical Department at BCC purchased a number of them) with its slow stepping front panel finally prompted me to see what could be done with the old Imsai. In the August 1977 *Kilobaud* I found one solution. An article by Howard Bendrot illustrated a simple modification for the Imsai front panel which required only one part and cutting a few traces on the front panel. Bendrot's approach, while simple, suffers from the problem that the slow step speed is not variable. That fact, coupled with my desire not to make irreversible modifications to the front panel, led me to develop the variable speed slow step circuit described in this article.

![Complete slow step system. Multiple conductor is used only for +5V and GND. Note uncluttered layout of S-100 board.](image)

Study of the Imsai front panel schematic shows that the only requirement for single stepping the Imsai is to pull pin 1 of U17 to logic low. With the Imsai in the stop mode, I found that connecting a square wave generator to pin 1 produced slow stepping at the square wave frequency. A direct connection is not really practical however, because it interferes with the normal single step operation of the front panel. One solution to this problem is to run the generator through a tristate buffer. Disabling the buffer completely isolates the clock sign from U17. To keep the entire circuit internal to the Imsai, I decided to build a clock, using a 555 timer. The clock circuit is very simple, requiring only a few parts beyond the 555. Figure 2 shows the final circuit.

The range switch is necessary to give a wide range of stepping rates. The range covered by both capacitors is from about one step per ten seconds to over 400 steps per second. C2 on U17 (Figure 1) limits the maximum...
slow step speed to around 400 steps per second. Decreasing its value should allow higher slow step speeds, but I have not tried changing the capacitor. I'm not sure it wouldn't foul up the normal front panel single step function.

Operation of the circuit is very simple. If S2 and S3 are both open, the front panel operates in the normal way. With the front panel in the stop mode, and either S2 or S3 closed, the computer will slow step at a speed depending upon the setting of S1 and R1.

The circuit works well and causes no glitches or problems that I am aware of. While it's more complex than Bendrot's circuit, it is more versatile and requires no modification of the front panel. The circuit even has an advantage over the Intersystems computer—on that machine, you must remove the front panel cover to change the slow step speed.

I gave a lot of thought to where to position the finished circuit. Finally, I decided to mount it inside the IMSAI, since the cover is usually off when I want to single step or slow step. The power transformer is a convenient mounting place—I provided a little breathing space for the transformer by securing the circuit with a couple of strips of a half-inch thick double-sided tape. In order to keep everything modular, I must confess that I set up an entire Vector 8-100 breadboard card to supply the 5V needed by the circuit. No doubt other people could come up with a more reasonable power source.

An experience I had with the circuit may be of some interest. The IMSAI computer runs Cromemo's Control Basic and I thought it would be interesting to slow step through a simple program to see how many machine language steps are really involved. (I had tried this previously, using the single step switch without success.) I used the loop 10 PRINT "HELLO", 20 GOTO 10. This program running in the slow step mode at 100 steps per second took about 45 seconds to loop. That comes out at 4500 machine language steps. I hadn't realized how much interpreting actually goes on in an interpreter! Interesting speed comparisons are possible; the same program run under identical conditions using Northstar Basic required approximately thirty seconds to execute.

I would like to express my appreciation to my brother, David Long, for his advice on the 555 timer portion of this project and to John Young, the Broome Community College photographer for his photographic efforts.
Hardware Product Review

The Televideo 920-C Terminal

by Glenn A. Hart

The Televideo 920-C serial terminal is the flagship in a line of low cost yet highly flexible serial video terminals. While it does have certain problems, the Televideo terminals allow both the microcomputerist on a budget and the professional user requiring multiple terminals to achieve a level of performance previously unattainable at such a reasonable price.

All four Televideo models are based on the same chassis and electronics, differing primarily in the keyboard layout. The 920 models include eleven special function keys, six editing keys and two transmission keys. Each function key can generate two code sequences depending on whether the shift key is depressed, so a total of twenty-two special codes are available. (The physical design does not provide any convenient place above the function keys to indicate the functions assigned to each key, a desirable feature found on some more costly terminals.) The 912 models do not include the special function keys, but all models have 14-key numeric keypads, six cursor movement keys and various other special keys for excellent flexibility. All keys will repeat at a 15 CPS rate when held down.

Both the 912 and the 920 series are available with a choice of keyboard layout, indicated in the model number by either a -B or -C suffix. The B models have a layout loosely based on a Teletype keyboard, while the C models have a Selectric-based layout with oversized RETURN and TAB keys. The location of several characters is completely different (", ', @$, $, etc.). The Selectric layout is easier to use and more familiar to traditional typists, but if you are used to the computer layout it may take a while to make the transition. The C models also cost quite a bit more; the choice is up to you.

The screen displays the traditional 24 lines by 80 characters. The full 96 character ASCII character set is generated in a 7 X 10 matrix with 12 X 10 resolution, resulting in a type font that is elegant and easy to read, with lower case descenders and the ability to underline. No special graphics characters are provided. The clarity of the on-screen characters is reasonably good. While it is definitely far better than many low cost terminals I have used, it is not the equal of some more costly terminals. I have used the unit for six and eight hour stretches without eye fatigue, so the 12-inch black-and-white CRT certainly provides reasonable video performance. Keyboard feel is a bit on the firm side compared to some other terminals, but provides a good level of feedback to the operator.

All Televideo terminals operate at a choice of nine Baud rates from 75 Baud to 9600 Baud. Documentation for earlier units indicated that 19,200 Baud could be used. There is an obvious switch position for this speed, but evidently there were operating problems and the documentation supplied with newer units does not mention 19,200 Baud. Even, odd, mark, space or no parity is available, and the terminals can be used in either normal RS-232 or 20ma current loop modes. An RS-232 printer port is supplied. Both full and half duplex conversational as well as block mode is available.

The 920-C is microprocessor and software driven. Intel's 8035 microprocessor provides much of the operating flexibility of the terminal, with the software routine stored in a ROM. There is a price to pay for this flexibility, but more about that later.

The list of functions available is impressive (see Table 1). Most of the codes are Escape sequences, with few using control characters for compatibility. I am told that the commands resemble those of the ADM-31 terminal. The average user will concentrate his attention on the normal cursor movement commands and few of the special formatting options. Absolute cursor addressing is handled in a normal fashion and the position of the cursor can also be read by a program. Various attractive and useful formats can be designed by combining the half-intensity, reverse video, blinking and underlining features. All these commands can work on a character-by-character basis for careful control. One peculiarity is the extra character position that some of these commands take when they execute; this sometimes requires a bit of juggling in the formatting routines.

Many of the other editing and special features are not available in the normal conversational mode and are intended for block mode use. Since CP/M and other microcomputer operating systems are character oriented, these functions are of little practical use. For the mainframe user, a full spectrum of editing and block mode features is available.

While the editing features would not normally be used in a microcomputer environment, they are often used by applications software. Commands like Erase to End of Line, Insert Line and Erase to End of Screen are often issued by word processors and other programs to speed on-screen activity. The Televideo terminals have problems when such commands are issued by the computer. The terminals were designed to handle keyboard entry of these commands correctly, but the microprocessor/software combination is simply a bit too slow to react correctly. Word-Star, for example, will send several consecutive these commands correctly, but the microprocessor/software combination is simply a bit too slow to react correctly. While the terminals, insert lines, etc., and the TVI will almost always drop at least one character. The Musicraft music entry system uses Erase to End of Line and Insert Line frequently; the terminal will often sound its bell and garbage up the screen with any Basic or other high level languages; presumably they are either slow enough to avoid the problem or don't make use of the troublesome commands at all.

The design engineer at Televideo explained that the 8035 is running at its full designed clock speed. (Some of the terminals using a Z-80 may respond faster.) TVI sent me a new ROM with somewhat faster routines which completely solved the Musicraft problem but still could not totally handle Word-Star. The answer with Word-Star is to disable the use of the special functions by patching the program. This reasonably easy step causes Word-Star to generate the required actions in software instead and results in perfect, although very slightly slower, operation. I don't know TVI's policy on upgrading older units, but I would assume that all new production uses the faster ROM.

I also experienced some reliability problems. Several hours after first powering up the terminal, the power supply module blew a capacitor. I was chagrined to find that TVI warranty covers only in-factory repair, which would have meant sending the unit back to California. TVI's ads indicate that General Electric field service is available. This is true, and service contracts can be purchased to cover the period after the 90-day warranty expires. However, TVI doesn't authorize GE to perform warranty service, so repairs during the warranty period must either be at the factory or at the owner's expense. Some other terminal manufacturers have made field service arrangements similar to TVI's, but they evidently also permit in-warranty repairs at a replacement power module immediately. I don't know if this is something they would do for all customers, but it certainly helped me out tremendously.

All in all, I have been quite happy with the 920-C. It is flexible and easy to use, and has provided many long hours of dependable service once its initial problems were sorted out. Considering the heavy discounts at which the entire Televideo line is commonly sold, TVI terminals offer a very positive cost/performance ratio. The 920-C has more features than many terminals selling for much more, and is a clear winner when compared with terminals selling at or near its price.

### Table One

<table>
<thead>
<tr>
<th>Function</th>
<th>Sequence</th>
<th>Function</th>
<th>Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Beep</td>
<td>Control-G</td>
<td>Read Cursor</td>
<td>Escape ?</td>
</tr>
<tr>
<td>Cursor Left</td>
<td>Control-H</td>
<td>Set Block Mode</td>
<td>Escape B</td>
</tr>
<tr>
<td>Cursor Down</td>
<td>Control-J</td>
<td>Set Conversation Mode</td>
<td>Escape C</td>
</tr>
<tr>
<td>Cursor Up</td>
<td>Control-K</td>
<td>Print Page</td>
<td>Escape D</td>
</tr>
<tr>
<td>Cursor Right</td>
<td>Control-L</td>
<td>Character Insert</td>
<td>Escape F</td>
</tr>
<tr>
<td>Home Cursor</td>
<td>Control-~ or Control-~</td>
<td>Character Delete</td>
<td>Escape G</td>
</tr>
<tr>
<td>Tab</td>
<td>Control-I</td>
<td>Line Insert</td>
<td>Escape H</td>
</tr>
<tr>
<td>New Line</td>
<td>Control_- (underscore)</td>
<td>Line Delete</td>
<td>Escape I</td>
</tr>
<tr>
<td>Protect Mode On</td>
<td>Escape A</td>
<td>Line Erase to Screen</td>
<td>Escape J</td>
</tr>
<tr>
<td>Protect Mode Off</td>
<td>Escape B</td>
<td>Page Erase to Space</td>
<td>Escape K</td>
</tr>
<tr>
<td>Start Half Intensity</td>
<td>Escape C</td>
<td>Page Erase to Space</td>
<td>Escape L</td>
</tr>
<tr>
<td>End Half Intensity</td>
<td>Escape D</td>
<td>Back Tab</td>
<td>Escape M</td>
</tr>
<tr>
<td>Set Column Tab</td>
<td>Escape E</td>
<td>Toggle Page</td>
<td>Escape N</td>
</tr>
<tr>
<td>Clear Tab</td>
<td>Escape F</td>
<td>Start Blink Field</td>
<td>Escape O</td>
</tr>
<tr>
<td>Clear All Tab</td>
<td>Escape G</td>
<td>Start Blank Field</td>
<td>Escape P</td>
</tr>
<tr>
<td>Send Line Unprotect</td>
<td>Escape H</td>
<td>End Blank/Blank</td>
<td>Escape Q</td>
</tr>
<tr>
<td>Send Page Unprotect</td>
<td>Escape I</td>
<td>Tab</td>
<td>Escape R</td>
</tr>
<tr>
<td>Send Line All</td>
<td>Escape J</td>
<td>Start Inverse Video</td>
<td>Escape S</td>
</tr>
<tr>
<td>Send Page All</td>
<td>Escape K</td>
<td>End Inverse Video</td>
<td>Escape T</td>
</tr>
<tr>
<td>Clear All to Space</td>
<td>Escape L</td>
<td>Start Underline</td>
<td>Escape U</td>
</tr>
<tr>
<td>Clear All to Null</td>
<td>Escape M</td>
<td>Line Erase to Null</td>
<td>Escape V</td>
</tr>
<tr>
<td>Clear Foreground to Null</td>
<td>Escape N</td>
<td>Page Erase to Null</td>
<td>Escape W</td>
</tr>
<tr>
<td>Clear Foreground to Space</td>
<td>Escape O</td>
<td>Auto Flip On</td>
<td>Escape X</td>
</tr>
<tr>
<td>Keyboard Enable</td>
<td>Escape P</td>
<td>Auto Flip Off</td>
<td>Escape Y</td>
</tr>
<tr>
<td>Keyboard Disable</td>
<td>Escape Q</td>
<td>Extension Port On</td>
<td>Escape Z</td>
</tr>
<tr>
<td>Load Cursor</td>
<td>Escape R</td>
<td>Page Print Mode On</td>
<td>Escape A</td>
</tr>
</tbody>
</table>

MICROSYSTEMS
An 8086/8088 Reference Book

by Chris Terry

This substantial book is a very good value for the money, and I have a strong feeling that it will become the standard 8086/8088 reference work. As is true of all the books that I have seen from Osborne Associates, it is well organized, cleanly and clearly written, and loaded with diagrams. Good paper, a very readable typeface, and judicious use of boldface enhance the communication, making The 8086 Book a pleasure to use. The book is divided into ten chapters, the first six discussing software and the instruction set, and the last four concerned with the hardware aspects.

Software Aspects

Chapter 1, "Programming," is a crisp, pertinent, and sometimes amusing exposition of the six aspects of the programming task: Specification, Design, Implementation, Testing, Documentation and Maintenance. There's nothing new here, but it's a valuable reminder of what it takes to create a good program.

Chapter 2, "Some Program Examples," discusses the design aspects, at the flow-chart level, of a sort program and associated I/O routines. This is a preparation for chapter 6, "Examples of 8086 Assembly Language Programming," which shows the implementation. Chapter 6 is very valuable; it does not merely supply code, but shows alternative ways of coding certain functions, and discusses their impact on storage space and execution speed.

Chapter 3, "The 8086 Instruction Set," is the longest chapter in the book. After a seventeen-page introduction mainly concerned with design considerations for an I/O driver using the 8251 USART (which I think would have been better placed in chapter 2), we get down to business. First comes a description of the 8086 registers, and how various groups of instructions affect the Status Register flags. Next, there is a detailed description of the six basic addressing options; Immediate, Direct, Direct Indexed, Implied, Base Relative, and Stack. This section includes the mechanisms by which addresses are computed, and the part played by the segment registers. Finally we come to a detailed description of each 8086 instruction, in alphabetical order of mnemonics. Here, the very clear diagrams detail what the instruction does; notes provide clarification and indications of the practical uses of the instruction.

Chapter 4 groups the instructions according to their functions: Data Movement, Arithmetic, Logic, String Primitives, Program Counter Control, I/O, Interrupt, and Rotate and Shift. The information here is mainly tabular, and promotes a better understanding of the instructions by discussing them with a different slant.

Hardware Aspects

Chapter 7 is a clear and detailed description of basic 8086 system concepts and architecture, with particular reference to the use of the data and address buses. Chapter 8 discusses operating modes, interrupts and a timing in single-CPU system. The excellent diagrams include configurations for DMA (Direct Memory Access). Chapter 9 discusses the Intel Multibus, and describes the function of each line. And finally, Chapter 10 discusses multiprocessor configurations.

Of the four appendices, A and B list the instruction set alphabetically by mnemonic, and numerically by hex value of the operation code. Appendix C contains data sheet reprints giving AC and DC signal characteristics and signal waveforms for the 8086, 8088, and support chips of the same family. Appendix D discusses the differences between the 8086 and the 8088; the instruction sets are identical, but the 8088 operates with an 8-bit data bus and therefore uses two bus cycles instead of one to access 16 bits of data.

Comments

The descriptions of how the various addressing modes operate are detailed and as comprehensible as one could expect considering their complexity. The same goes for the use of the segment registers. However, I long for some indications of the purpose behind it all. Although not a professional, I consider myself a moderately competent 8080 programmer, and I can see the point of indexed and relative addressing. But why would anyone want to use base relative, direct, indexed stack addressing? Obviously someone does, or it would not be included. But who—and what for? Similarly, what is the advantage of having a Code segment, a Data segment, a Stack segment, and an Extra segment of memory? For multi-user systems? Maybe, since this element of purpose is something that gets left out of manuals all too often. Without it, the mass of detail on "what" and "how" tends to overwhelm a reader who has no experience with comparable procedures, because he or she is working in an application vacuum. Some guidelines for when
and how to use these features would have been far more valuable than the elementary material that now constitutes chapter 5.

I question the value of the first three pages of chapter 1 (which contains highly simplified remarks about the functions of Assembly Language and assembler programs) and chapter 5 (which contains elementary descriptions of the functions of an editor, an assembler, and a debugger). I have a suspicion that the material was included to appease some editor who complained that terms were being used without being defined. I can only say that anyone who does not have a firm grasp of this material at a much more detailed level is not ready to struggle with the complexities of the 8086. This material cannot possibly prepare a neophyte adequately for the rest of the book, and is just padding for any programmer with more than a few weeks experience with assembly language.

The index is generally useful, although it has a few quirks (e.g., the sort program of chapters 2 and 6 is listed under "Shell sort," not "Sort," and only the chapter 6 reference is listed). I found a few typographical errors and a reference to a non-existent procedural step—but such flaws are few and very minor.

Don't, on any account, let my complaints and wish-list stop you from rushing out to buy this book if you are considering using the 8086, or if you have one already. It's a fine piece of work. And nobody has ever managed to write a book for which someone else (with the benefit of hindsight) could not suggest improvements!
I recently put together a very simple and reliable clock and calendar interface for my IMSAI-8080 system. The board uses a new chip designed by OKI Semiconductor, 1333 Lawrence Expressway, Santa Clara, CA 95051. The IC is called the MSM5832 Microprocessor Real-Time Clock/Calendar. It is oriented to microprocessor use and provides 4-bit data of seconds, minutes, hours, day-of-week, month and year. Data access is controlled by 4-bit addressing. It includes 12/24 hour selection, leap year identification and manual plus or minus 30 second correction. The chip comes in an 18 pin DIP package, designed for crystal control frequency reference, and can use standby battery backup. I bought the IC from Concord Computer Products, 1973 South State College, Anaheim, CA 92806, (714)937-0637. The cost is $8.50 plus tax and shipping.

The following is a sample of the output format from my clock/calendar program:

22:42:45 Tuesday 01-JUL-81
08:31:52 Wednesday 09-JUL-81

I've designed the software to generate a 30 character ASCII string which is displayed in the upper corner of my memory-mapped video terminal, print on my assembler listings, and use anywhere I need to document the time and date.

Hardware

I constructed the clock/calendar circuit on an S-100 prototyping board. The circuit uses only seven IC’s and occupies only a quarter of the board, leaving room for future projects. The interface to the S-100 bus follows a design by Condra, using an 8255 Programmable Peripheral Interface IC in a bi-directional mode to communicate with the clock chip. Two latched output ports and one input port are needed for the interface. The clock/calendar IC also requires a 32.768 KHz crystal for its internal clock circuit to operate. I extracted one from an old LED wristwatch I had lying around. I also used the small trimmer capacitor from the watch for the time adjustment trimmer.

For battery backup I decided not to fool around with an NICAD re-chargeable battery. Instead I selected an alkaline 4.5 Volt photoflash battery I purchased in a local drug store. I used the Mallory PX21. The capacity of this battery is 580 Ma-Hrs; at the measured current drain of the clock chip (20 micro-amperes), the clock should keep on running for 3.3 years!

Once the trimmer is adjusted, the accuracy of the clock is excellent. I have run my board for nearly a year and found it to be accurate to better than five seconds/month. No glitches have been observed during the times I turned the computer power on or off. I can even remove the board from my mainframe without affecting the time of the clock.

Software

The software I use to read the clock circuit is shown in Listing 1. The part of the program specific to the 8255 PPI-IC is the CLKRD subroutine. If you build the circuit with some other interface, this part of the software will have to be altered to fit the IC used. CLOCK is a subroutine which generates a 30 character ASCII string containing the time, day and date (as was shown earlier). On entry, H&L registers are set to point to the location where the ASCII string is to be stored. I use the CLOCK subroutine to display the time and date on my video terminal, and periodically update the time by calling the CLOCK routine while in the keyboard input status wait loop.

Use of the interface is not restricted to assembly language routines. Listing 2 shows a very simple program written in North Star Basic to read and display the clock/calendar data. It would be a very simple task to reformat the output to the needs of a user.

Finally, I've included in Listing 3 the program I used to initialize the clock/calendar IC. I've only used this program a few times because the chip keeps such good time, but it is needed to get your chip going.

Give this simple clock/calendar interface a try. You will be surprised how easy it is to build—and how handy it is to have the time and data available to your S-100 system.

References

Listing 1

RDCLK IS A DUMMY DRIVER PROGRAM USED FOR CALLING THE CLOCK SUBROUTINE.
IT PUTS THE 30 CHARACTER ASCII TIME, DAY AND DATE STRING UP IN THE UPPER
RIGHT HAND CORNER OF THE SCREEN SPLITTER MEMORY MAPPED VIDEO DISPLAY.
STRING .EQU OF032H ;PUT TIME ON CRT DISPLAY
RDCLK: .ORG 01000H
LXI H,STRING
CALL CLOCK
RET ;RETURN BACK TO MONITOR
CLOCK IS A SUBROUTINE TO GENERATE A 30 CHARACTER STRING CONTAINING
THE TIME, DAY-OF-WEEK, DAY, MONTH, AND YEAR IN THE FORMAT
12:34:56 WEDNESDAY 29-JUN-80.
INPUT: HL POINT TO A 30 CHARACTER ASCII STRING OUTPUT BUFFER
ALL REGISTERS ARE USED AND DESTROYED BEFORE RETURNING.
CLOCK: PUSH H ;SAVE CLOCK STRING ADDR
LXI H,CLKTBL ;POINT TO CHIP DATA BUFFER
CALL CLKRD ;READ CLOCK CHIP
LDA CLKTBL+5 ;MASK OFF 24 HR BIT
ANI 3H
STA CLKTBL+5
LDA CLKTBL+8 ;MASK OFF LEAP YR BIT
ANI 3H
STA CLKTBL+8
;CONVERT TIME DATA TO ASCII STRING
LXI B,CLKTBL+5 ;START AT H10
POP H ;GET STRING BUFFER POINTER
LXI D,0302H ;3 GROUPS OF 2 DIGITS
TIME:
LDAX B
ADI 3OH ;CONVERT TO ASCII.
MOV M,A
INX H
DCX B
DCH E
JNZ TIME ;GET UNITS VALUE
DCH D
JI DAY ;DONE WITH TIME, DO DAY

MICROSYSTEMS 65
MVI E,2  ; Put in colon
INX H
JMP TIME

; DAY-OF-WEEK
; THE 7TH BYTE IS THE DAY OF THE WEEK DIGIT
; 0=SUNDAY, 6=SATURDAY

; DAY:
; MVI M,' ',' ; Put 2 spaces in string
INX H
MVI M,' ';
INX H
PUSH H
LDA CLKTBL+6
LXI D,9
19 characters per day
LXI H, DAYTBL

; DAY1:
; DCR A
JMP DAY1
DAD D
JMP DAY0

; POP DAY0
MOV A,M
STAX B
INX H
INX B
DCR E
JNZ DAY2
JMP DATE

; CLKTBL: .RES 13
; CLOCK DATA RAM BUFFER
; .END

; Listing 2

10 REM--THIS IS A NORTH STAR BASIC PROGRAM TO READ THE
20 REM--CLOCK/CALENDAR INTERFACE. THE PROGRAM ASSUMES THAT
30 REM--THE 8255 PPI I/O PORT ASSIGNMENTS ARE AS FOLLOWS.
40 REM-----CLOCK DATA I/O (4 BITS) = PORT 50H (80 DECIMAL)
50 REM-----ADDRESS & CONTROL (7 BITS) = PORT 51H (81 DECIMAL)
60 REM-----8255 MODE CONTROL (8 BITS) = PORT 53H (83 DECIMAL)
65 REM
70 DIM C(13), DS(63), M$(36)
80 OS(1,63) = "SUNDAY MONDAY, TUESDAY
90 M$(1,36) = "JANUARY, FEBRUARY
100 REM--SET 8255 IN MODE8
110 OUT 83,144
120 REM--TURN ON CLOCK CHIP READ AND HOLD LINES
130 AL=48
140 OUT 81, AL
15C
REM--READ THE 13 BYTES OF CLOCK DATA
160 FOR J=1 TO 13
170 C(J)=INP(80)
180 OUT 81, AL+J
190 NEXT J
200 REM--TURN OFF READ AND HOLD LINES
210 OUT 81, 0
220 REM--TAKE OFF THE 24 HOUR BIT (BIT2)
230 C(6)=C(6)-S
240 REM--NOW PRINT OUT THE TIME, DAY AND DATE
250 PRINT %1I,C(6),C(5),":"C(4),C(3),":"C(2),C(1)
260 PRINT D$(91C(7)+1,91C(7)+9)
27011=3l(C(11)l10+C(10»-2
280 PRINT 11$(1'1,1'1+2),"","C(5)+10lC(9),","C(13) ,C(12)
290 PRINT
; System Equates
; COUT .EQU 200DH  ; NORTHSTAR OUTPUT
; CINP .EQU 201OH  ; NORTHSTAR INPUT
; APORT .EQU 50H  ; 8255 PORT A--CLK DATA I/O

; Listing 3

; This is a subroutine to set the MSM5832 clock/calendar interface.

; SYSTEM EQUATES

**SPORT CNTRL NDELY WRHLD HLDBIT WRTBIT**

**RZ**

**ANI**

**OFH**

; MASK LOWER NIBBLE

**MOV**

**H, A**

; DECREMENT DATA POINTER

**DCR**

**H**

; GET MORE INPUT TILL CR

; CLOCK WRITE SUBROUTINE--USED TO INITIALIZE DATA IN CLK CHIP

**XLX**

**HI, TBUFO**

; POINT TO BUFFER

**MVI**

**A, [MODEO]**

; INITIALIZE 8255

**OUT**

**CNTRL**

**MVI**

**A, [HLDBIT]**

; SET HOLD LINE

**OUT**

**SPORT**

**MVI**

**A, [NDELY]**

; WAIT FOR THINGS TO SETTLE

**WAIT**

**DCR**

; GET HOLD LINE + ADDRESS

**DJNZ**

**WAIT**

**MVI**

**B, [HLDBIT]**

; SET HOLD LINE

**WRLOOP**

**CPI**

**HLDBIT+13**

; TEST TO SEE IF DONE

**JZ**

**WRLOOP**

; DONE, TURN OFF HOLD

**OUT**

**SPORT**

; WRITE ADDRESS TO CHIP

**MOV**

**A, B**

; SEND DATA TO CHIP

**ORI**

**40H**

; OR WITH WRITE PULSE

**OUT**

**SPORT**

; WRITE DATA TO CHIP

**OUT**

**SPORT**

; MASK OFF WRITE BIT--KEEP HOLD

**ANI**

**1FH**

; ECHO CHARACTER INPUT

**CIN**

**B, A**

; CHECK FOR RETURN • END

**MSG**

; TERMINAL MESSAGES

**ASCII**

'CLOCK/CALENDAR Initialization Program'

**BYTE**

0D

; CARRIAGE RETURN-LINE FEED SUBROUTINE

**MVI**

**B, 0DH**

; POINT TO BUFFER

**CALL**

**COUT**

; INITIALIZE B2SS

**CALL**

**CNTRL**

**CALL**

**NDELY**

; SET HOLD LINE

**CALL**

**WRHLD**

; WAIT FOR THINGS TO SETTLE

**CALL**

**HLDBIT**

; GET HOLD LINE

**CALL**

**A, B**

; WRITE ADDRESS TO CHIP

**MOV**

**A, B**

; SEND DATA TO CHIP

**ORI**

**40H**

; OR WITH WRITE PULSE

**OUT**

**SPORT**

; WRITE DATA TO CHIP

**OUT**

**SPORT**

; MASK OFF WRITE BIT--KEEP HOLD

**ANI**

**1FH**

; ECHO CHARACTER INPUT

**CIN**

**B, A**

; CHECK FOR RETURN • END

**MSG**

; TERMINAL MESSAGES

**ASCII**

'Input Set Time (HHMM)' 

**BYTE**

0H

; ECHO CHARACTER INPUT

**CIN**

**B, A**

; CHECK FOR RETURN • END

**MSG**

; TERMINAL MESSAGES

**ASCII**

'Input Day of the Week (O=Sunday, 6=Saturday'

**BYTE**

0H

; ECHO CHARACTER INPUT

**CIN**

**B, A**

; CHECK FOR RETURN • END

**MSG**

; TERMINAL MESSAGES

**ASCII**

'Input Year, Month and Day (YYMMDD)' 

**BYTE**

0H

; ECHO CHARACTER INPUT

**CIN**

**B, A**

; CHECK FOR RETURN • END

**MSG**

; TERMINAL MESSAGES

**ASCII**

'~Jh •• n Ready, PRESS RETURN to Initialize CluCK.' 

**BYTE**

0H

; ECHO CHARACTER INPUT

**CIN**

**B, A**

; CHECK FOR RETURN • END
SOFTWARE DIRECTORY

Program Name: Energy Basic
Hardware System: CP/M 2.2 & I.D.S. Modem
Language: Machine Code
Description: Energy Basic is a high level language designed to simplify implementation of energy management systems and similar applications requiring monitoring of time, elapsed time, temperature, kilowatt demand, digital inputs, and control of devices based on such information. It provides the Basic language constructs including FILL, FOR, GOTO, GOSUB, IF, INPUT, LET, LIST, NEXT, OUT, PRINT, RETURN, REM, RUN, STOP, WAIT, ABS, CALL, EXAM, INP, RND
AND SIZE. Special commands and functions include MODE, SET, ANSW, ELAP, ORIG, PSTD, TEMP and TIME. For example, X=TEMP0 sets X to current temperature at sensor 0, T=TIME sets T to current time of day, SET causes current time of day to be set; ANSW places system modem in auto-answer mode; ORIG causes a data communications call to be established to current Originate telephone number; ELAP(A) returns time which has elapsed since A was set equal to TIME; etc. Energy Basic supports a primary system console device, an optional system printer, and an optional originate/answer modem. Energy Basic is available as a development system on 8" or resident on two 2716 type PROMs. The Development System version of Energy Basic also supports the following commands and functions: BYE, LOAD, NEW, SAVE, and SIZE, LOAD and SAVE retrieve and store Energy Basic source programs to and from disk storage.

Release: January 1981
Price: $195. User's manual only $10
Included with price: Either 8" disk (P/N EBO80) or two 2716 EPROMs (P/N EBO10) and user's manual.

Where to purchase it:
International Data Systems, Inc.
P.O. Box 17269
Chicago, IL 60657
(312)327-7666

Program Name: Alpha FORTRAN
Hardware System: Alpha Micro (16-bit)
Minimum Memory Size: 32K user memory
Language: Assembler
Description: A multi-user Fortran 77 implementation that has mainframe features. The compiler produces actual assembly language code, not pseudo code, thus allowing Fortran programs to execute many times faster than Basic. Compilations can be stored into a program library, and later linked with assembler or Pascal programs. In addition, Fortran programs are directly callable from Softwork's AlphaAPL language or from Basic. Floating point hardware provides the user with 11 digit accuracy.

Releases: April 1981
Price: $600
Included with price: Language, documentation, sample programs

Where to purchase it:
Softworks Limited
607 W. Wellington
Chicago, IL 60657
(312)327-7666

Program Name: ACCESS/80 - Information Management System
Hardware System: CP/M Operating System
Minimum Memory Size: 54 K+
Language: Assembly
Description: ACCESS/80 is a high-level, non-programmer oriented system for report generation, data entry, file update, reorganization, and maintenance, statistical tabulation, and applications development. Its high level functionality is comparable to the RAMIS system on IBM mainframes. In addition to functioning as a self-contained system, ACCESS/80 will produce reports from any external file stored in ASCII character format, including Basic and Fortran files.

Price: $795
Included with price: diskette containing program and sample applications; User's Manual, 3 copies of Command Reference Card

Author: Friends Software, Inc.
Where to purchase it:
Friends Software
2020 Milvia Street, Suite 400
P.O. Box 527
Berkeley, CA 94701
(415)540-7282

Program Name: Enhanced I/O Drivers
Hardware System: NorthStar MDS or Horizon
Language: 8080 Machine Code
Description: These enhanced I/O drivers for NorthStar DOS (versions 4 & 5), Lifeboat's NorthStar CP/M (versions 1.4 & 2.2), and UCSD Pascal (version 1.5) are field tested. NorthStar DOS can now echo console output to printer, suspend console output until another key is pressed, and reassign console device. I/O drivers are available for serial devices, IMSAI's VIOC, Malibu's 160 printer, and a modem attached to a serial port with all remote I/O echoed to the local console. CP/M users now have a full implementation of I/O byte, allowing user to reassign console, list, and readdress punch to any of four devices such as CRT, printing terminal, high speed printer and modem. Includes ability to use NorthStar computer as intelligent terminal which can send or receive disk files. Special support is provided for IMSAI VIOC and Malibu 160. UCSD Pascal (from NorthStar) can detect which device is being used as console and can detect if IMSAI VIOC is present.

Release: Available now
Price: $50 per driver
Included with price: CP/M disk

Where to purchase it:
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Author: Allen Ashley

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Author: Allen Ashley

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Program Name: DATABS
Hardware System: CP/M 8
Minimum Memory Size: 40K
Language: Machine Code
Description: DATABS was inspired by CLU (Cornell Lab of Simulation and Programming). The implementation of user-defined types using a dynamic storage mechanism. Data abstractions allow for the programmer to write code that is independent of the actual data structures and memory layout. The implementation of user-defined types using a dynamic storage mechanism. Data abstractions allow for the programmer to write code that is independent of the actual data structures and memory layout.

Release: January 1981
Price: $100-$150 depending on options or special modes. Manual only $30.
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Hardware System: Any 8080/Z80 standard
Minimum Memory Size: 48K
Language: Machine Code
Description: ZAS is an assembly language development tool for Zilog's Z8001 and Z8002 16-bit microprocessors. Includes a relocatable cross-assembler, a linker/task builder, an absolute object file loader, and a Z-8000 run-time module, ZEX, which supports any Z-8000 alternate bus master (such as the Ithaca Intersystems MPU-8000). Using CP/M, ZEX creates an I/O-independent run-time environment for application code with ZAS. The package includes a full integrated software development environment for the Z-8000, while retaining full use of current software and hardware facilities under CP/M.

Release: March 1981
Price: $395, $25 for user manual
Included with price: ZAS Assembler, ZLK Task Builder, ZLD Object Loader, ZEX Runtime Monitor, User Manual. (8" SD CP/M Format Floppy)

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North Star Introduces New I/O Board

North Star Computers Inc. announces a new four-port serial input/output board. The HSIO-4 Board is S-100 bus compatible, and supports asynchronous and synchronous communications with either RS-232 or current loop options. Each port's baud rate is programmable with eight asynchronous or six synchronous speeds. Each port also has four interrupt sources, three of which are maskable, the fourth being enabled/disabled with an on-board jumper.

The HSIO-4 Board supports North Star's new TSS/A multi-user system, and can be easily reconfigured through header changes to support other applications. Price: $349.

For further information, please contact: Elliot Wasserman, Vice President/Marketing, North Star Computers, Inc., 14440 Catalina Street, San Leandro, CA 94577, (415)357-8500.

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Corvus Unveils 5-Megabyte Add-On Winchester Disk Systems

Corvus Systems has announced a family of 5-megabyte Winchester disk systems available to interface to a wide variety of microcomputers—TRS-80 models I and II, Apple II and III, Altos, Alpha Micro, Intertec Superbrain, NEC PC-8001, and Ontel, as well as all S-100 bus-based computers running under CP/M or OASIS; under development are interfaces for the TRS-80 model III, PET, Zenith Z-89, Atari, and HP-85 machines.

A system package consists of the drive (same size as a 5 1/4-inch floppy), and intelligent Z80-based controller card, an intelligent interface card with firmware, software appropriate to the given model of microcomputer and power supply.

Performance specifications include an unformatted data capacity of 6.9 Mbytes (5.8 Mbytes formatted); a minimum seek time of 10 milliseconds; and average seek and latency times of 50 and 8.3 milliseconds, respectively. Power consumption is 120 W.

Further, the drives are fully compatible with Corvus' Mirror™ and Constellation™. The Mirror provides Winchester backup at a 1-Mbyte/minute rate via a standard video cassette recorder and 120-Mbyte capacity cassettes. The Constellation is a backend local network—a host multiplexer that allows up to 64 microcomputers to communicate with each other, share peripherals, and share a common Corvus disk drive.

Price is $3,750; quantity discounts are available. Corvus Systems, 2029 O'Toole Avenue, San Jose, CA 95131. (408)946-7700.

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64K Byte Memory For S-100 Microcomputers

Chrislin Industries' new CI-S100 dynamic RAM memory module requires no wait states at 2 or 4 MHZ and is compatible with most S-100 bus microcomputers.

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S-100 Color Video Processor/Programmable Sound Generator

The Color Video Processor and Programmable Sound Generator allows an S-100 bus computer to display text, graphics and animation along with sound effects or music on a color television set. The board includes 16K bytes of on-card I/O mapped video memory for storing multiple patterns. Two
New Products, cont'd...

New EXPANDER Desktop Computer Introduced

Micro-Expander, Inc. has announced their new entry into the professional microcomputer market. Called the EXPANDER, the S-100 computer requires only a video display and media storage for operation.

Lee Felsenstein, designer of the EXPANDER, is well known for his design of the SOL computer. The computer is built around a single board that contains a Z-80A CPU, keyboard circuitry, interrupt, video circuitry, real time clock, parallel printer interface, RS-232 serial interface, and full color circuitry. The unit also includes a 4-slot S-100 motherboard.

Features include standard 80 x 24 screen format, upper/lower case, 4K ROM monitor, 64K RAM expandable to 512K, video output and color graphics using 256 colors, and a complex tone generator with internal speaker. Keyboard capabilities include calculator keypad, two programmable function keys, and four cursor control keys.

The EXPANDER is sold complete with 24K Microsoft BASIC-80 (disk version) and 10K Microsoft BASIC-80 (cassette tape version). Included is Instant Basic by Gerald Brown, a beginner's manual.

The EXPANDER is available through dealers in the U.S. for under $2,200. A European version, called PAL, will also be available. For more information, contact Mats Ingemanson, president, Micro-Expander Inc., 7835 W. Higgins Ave., Chicago, IL 60656. Telephone (312)792-1196.

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Micro-Magic

AFTER ALL... ALL MODEMS ARE NOT CREATED EQUAL!

Single Board Computer Provides Multi-Processing Capability On The S-100 Bus

Net/80™, a single board microcomputer which operates as a slave processor for data processing networks, is now available from MuSYS Corporation. The device is ideal for use with CP/NET™. Net/80 performs as a Z-80 slave processor loosely coupled to an S-100 bus. Each board comes complete with 64K of RAM, a single level interrupt, a console serial port and a parallel port for communication with the S-100 bus master CPU. Each NET/80 slave operates independently of any others, except for resource queuing in the master. Thus, the entire system appears to be dedicated to each user, unless a large amount of shared resources are being accessed. In addition, NET/80 totally isolates the master CPU from errors in the slave processors.

The master processor has complete control over each slave, and can reset or interrupt a slave at any time. Transfer protocol can be performed with Z-80 block I/O instructions at near DMA speeds, while retaining protection and validation capability for the master. A bootstrap PROM supplied with each slave uses this transfer technique to download the system software into RAM. The PROM is then switched out of the address space so that the entire 64K is available as RAM.

Net/80 permits the customization of each serial port for various applications. Currently, a board configured for RS-232 with the slave appearing as a null modem allows direct connection to most common CRT terminals. Many other configurations are possible, including actual modem operation and RS-449.

A unique expansion bus on each slave gives users with unusual I/O requirements the ability to access additional peripherals. The first board designed for this bus will add a second serial port, Centronics printer or 8-bit bi-directional parallel port, priority interrupt control, real time clock, and the capability to act as the IEEE S-100 permanent bus master. The system is compatible with most CP/M software. Digital Research, the author of CP/M, offers CP.NET and its MP/M operating system for the network master, while Action Computer Enterprises offers OPOS, an operating system for the master, which runs under CP/M.

Price: $1,395.00; complete software also available. For more information, contact Mr. Bill Schultz, MuSYS Corporation, 1451 E. Irvine Blvd., Suite 11, Tustin, CA 92680. (714)730-5692. TWX:910-595-1967. Cable: MUSYSTSTN.
All disks except CS-9004 require 48K and Microsoft Basic. All 8" CP/M disks cost $24.95.

**Basic Games-1, CS-9001**

Includes the Following:
- Acey Ducey
- Amazing
- Animal
- Awari
- Bagels
- Banner
- Basketball
- Batnum
- Battle
- Blackjack
- Bombardment
- Bombs Away
- Bounce
- Bowling
- Boxing
- Bug
- Bullfight
- Bullseye
- Bunny
- Buzzword
- Calendar
- Change
- Checkers
- Chemist
- Chief
- Chomp

**Basic Games-2, CS-9002**

Includes the Following:
- Horserace
- Hawk
- Kinema
- King
- Letter
- Life
- Life For Two
- Literature Quiz
- Love
- Madlib
- Mastermind
- Math Dice
- Mugwump
- Name
- Nicomachus
- Nim
- Number
- One Check
- Orbit
- Pizza
- Poetry
- Poker
- Qubic
- Queen
- Reverse

---

**ADVENTURE**

Spring. You must try to find your way into the underground caverns where you'll meet a giant clam, a nasty little dwarf, and much more. This Adventure is Bi-Lingual—you may play in either English or French—a language learning tool beyond comparison. Runs in 32K CP/M system (48K required to SAVE GAME feature). Even includes SAM76 language in which to run the game. The troll says "Good Luck."

**Two Adventures**

Disk CS-9003 (48K) $24.95

**Adventurenland** (by Scott Adams)—You wander through an enchanted world trying to recover the 13 lost treasures. You'll encounter WILD ANIMALS, BEINGS, and many other perils and puzzles. Can you rescue the BLUE OX from the quicksand? Or find your way out of the maze of pits? Happy Adventuring....

**Pirate Adventure** (by Scott Adams)—"Yo Ho Ho and a bottle of rum..." You'll meet up with the pirate and his daffy birds along with many strange situations you attempt to go from your London flat to Treasure Island. Can you recover LONG JOHN SILVER's lost treasures? Happy sailing matey....

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**Basic Games-3, CS-9005**

Includes the Following:
- Artillery-3
- Baccarat
- Bible Quiz
- Big 6
- Binary
- Blackbox
- Bobstones
- Bocce
- Boga II
- Bombrun
- Bridge-it
- Camel
- Chase
- Chuck-A-Luck
- Close Encounters
- Column
- Concentration
- Condom
- Convoy
- Corral
- Countdown
- Coup
- Dealer's Choice
- Deepspace
- Defuse

**Special Packages**

Standard package: BASIC Computer Games Book and Disks 1 and 2
- CS-9000 $50.00

Special package: More BASIC Computer Games Book and Disks 3 and 4
- CS-9007 $60.00

BASIC Computer Games Book, More BASIC Games Book and All four disks
- CS-9008 $95.00

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**Basic Games-4, CS-9006**

Includes the Following:
- Mastermind
- Masterbaggles
- Mattpuzzle
- Minotaur
- Nomad
- Not One
- Obstacle
- Octrix
- Pasart I
- Pasart II
- Patterns
- Pinball
- Rabbit Chase
- Roadrace
- Rotate
- Safe
- Schmoo
- Seabattle

**Special Packages**

Standard package: BASIC Computer Games Book and Disks 1 and 2
- CS-9000 $50.00

Special package: More BASIC Computer Games Book and Disks 3 and 4
- CS-9007 $60.00

BASIC Computer Games Book, More BASIC Games Book and All four disks
- CS-9008 $95.00

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New Products, cont'd...

Non-Volatile Memory Modules For S-100 Bus
Non-volatile memory boards for S-100 systems are now announced by Dual Systems Control Corporation. The new boards feature high speed CMOS RAM IC's, onboard batteries, and proprietary write-protection circuitry. The result is a degree of data security approaching an EPROM board with the fast access and convenience of high speed RAM.

A software programmable “write-protect window” allows parts of the program, or selected data, to be changed without any risk of accidentally writing over protected data. For further data security, the boards generate a system interrupt when a power drop is detected, enabling the system to store critical data alive before the main power supply fails. When power is restored, the computer can resume operation as if no power failure had occurred.

Access time is 250 nanoseconds. Other features include 8 or 16-bit data transfers, bank select option, and extended memory addressing through 24-bit address lines. The batteries are guaranteed to keep programs and data intact for one year.

Prices: $1,095 for CMEM-32K with 32K bytes of memory, $895 for CMEM-16K and $695 for CMEM-8K. Dual Systems Control Corporation, 1825 Eastshore Highway, Berkeley, CA 94710; (415)549-3854 or (415)549-3890.

BIZCOMP Introduces VersaModem
BIZCOMP Corporation is introducing the Model 1084 Intelligent VersaModem, compatible with the Bell Standard 103 protocol. It uses a patent-pending combination of automatic calling unit (ACU), custom BIZ-080 microcomputer and data modem to enable full automatic dialing and auto-answer capability controlled through a simple RS232 interface.

VersaModem's unique Code-Multiplexed Design allows dialing functions to be easily implemented in high level languages such as Basic or Cobol. The unit itself has a simple command language much like the monitor commands of a minicomputer or microcomputer. Interfacing to RS232-equipped computers, word processors and programmable data equip-
If you are a CP/M user, on any system—S-100, Apple, TRS-80, Heath, Ohio Scientific, Onyx, Durango, Intel MOS, Mostek MOSX, etc.—after all CP/M is the Disk Operating System that has been implemented on more computer systems than any other DOS—then Microsystems magazine is the “only” magazine published specifically for you! Or, if you use an S-100/IEEE-696 based computer—and the most sophisticated microcomputer systems available use the S-100/IEEE-696 hardware bus—then Microsystems magazine is the “only” magazine published specifically for you!

We started publishing Microsystems almost two years ago to fill the void in the microcomputer field. There were magazines catering exclusively to the TRS-80, Apple, Pet, Heath, etc. system users. There were also broad based publications that cover the entire field but no one system in depth. But no magazine existed for CP/M users—or did one exist for S-100 users.

The why and what of a software bus
First of all what is a “bus”? And why do we call CP/M “the software bus”? A “bus” is a technique used to interface many different modules. Examples are the “S-100/IEEE-696 Bus” and the “IEEE-488 Bus.” These are hardware buses that permit a user to plug a bus-compatible device into the bus without having to make any other hardware modifications and expect the device to operate with little or no modification.

CP/M is a Disk Operating System (DOS). It was first introduced in 1974 and is now the oldest and most mature DOS for microcomputer systems. CP/M has now been implemented on over 250 different computer systems. It has been implemented on hard disk systems as well as floppy disk systems.

CP/M software packages and you have the largest applications software base in existence. CP/M is the only DOS for micros that has stood the test of time (seven years) with the highest level of compatibility from version to version. And over the years this compatibility has been maintained as new features have been added.

This is why we say “CP/M is the software bus” and why Microsystems magazine is vital to providing CP/M users with technical information on using CP/M, interfacing to CP/M, new CP/M compatible products and for CP/M users to exchange ideas.

Why support the S-100 bus?
S-100 is currently the most widely used microcomputer hardware bus. It offers advantages not available with any other microcomputer system. Here are a few of the advantages:

- S-100 is processor independent. There are already thirty different S-100 CPU cards that can be plugged into an S-100 bus computer. Nine 8-bit microprocessors are available: 6502, 6800, 6802, 6809, 2650, F8, 8080, 8085 and Z80. Eight 16-bit microprocessors are available: 8086, 8088, 9900, Z8000, 80000, Pascal Microengine, Alpha Micro (similar to LSI-11) and even the AMD2901 bit slice processor. Take your pick from the incredible offerings.

- S-100 has the greatest microcomputer power. What other microcomputer system has direct addressing of up to 16 megabytes of memory, up to 65,536 I/O ports, up to 10 vectored interrupts, up to 16 masters on the bus (with priority) and up to 10 MHz data transfer rate? You will have to go a long way to use up that computing power.

- S-100 is standardized. The S-100 bus has been standardized by the IEEE (Institute of Electrical and Electronic Engineers), assuring the highest degree of compatibility among plug-in boards from different manufacturers. And, Microsystems has published the complete IEEE S-100/696 standard (all 26 pages).

S-100 has the greatest hardware support. There are now over sixty different manufacturers of about 400 different plug-in S-100 boards. Far greater than any other microcomputer system.

With all these advantages is it any wonder that S-100 systems are so popular with microcomputer users who want to do more than just play games?

For the serious computer user.
Each issue of Microsystems brings you the latest in the CP/M and S-100 world. Articles on applications, tutorials, software development, product reviews, and lots more, to keep you on top of the ever changing microcomputer scene.

And if you are an S-100 system user using other operating systems (e.g. North Star) Microsystems also supports you.

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Microsystems – the CP/M* and S-100 User’s Journal

CP/M is the software bus!
S-100 is the hardware bus
for sophisticated microcomputer users!
New Products, cont’d…

operational parameters such as dialing speed, escape code character and number of rings to answer on. Price: $279.00. Hayes Microcomputer Products, Inc., 5835 Peachtree Corners East, Norcross, GA 30092. (404)449-8791.

SSM Introduces New S-100 EPROM Board

SSM Microcomputer Products has introduced the MB8A1K-16K EPROM Board, which provides sockets to support up to sixteen 2708 EPROM's. By removing 8 EPROM's, the board can be disabled in 1K increments. For example, with 8 EPROM's the board will act like and have the capacity of an 8K board. In addition, users can easily add or subtract memory as necessary. The user can overlay RAM and ROM on the same address in any desired increment. This provides increased flexibility when the board is used with RAM boards equipped with Phantom Disable.

SSM Microcomputer Products, 2190 Paragon Drive, San Jose, CA 95131, (408) 946-7400.

Software Vendor Directory

Micro-Serve Inc. has published the fourth edition of the Software Vendor Directory — a directory of microcomputer software companies. This newest edition contains the following features: 1001 software vendors, 4195 products, indexed by 80 hardware categories, and 200 software categories. The price is $100 for the Directory and two updates (which are future new printings at 6-month intervals). The Directory alone is $57.95, and one update to that Directory is $25. A disk version is also available (under CP/M) at $76, which includes a product named “Information Master” from Island Cybernetics of Port Aransas, Texas. The Software Vendor Directory is available from Micro-Serve Inc., at 250 Cedar Hill Avenue, Nyack, New York 10960, telephone (914) 358-1340.

Super Isolator

Electronic Specialists recently announced Model ISO-11 is designed to curb electrical problems. It features two individually dual-PI filtered AC socket banks (6 sockets total). Heavy-duty spike/surge suppression is incorporated in the design. Equipment interactions are eliminated and disruptive/damaging line spikes and hash are controlled. The Model ISO-11 Super Isolator controls power line spikes and hash while providing interaction free microprocessor operation. Price: $94.95.

Electronic Specialists Inc., 171 South Main Street, Natick, MA 01760, Phone: (617) 655-1532.

Software Shops

Software Shops

Software Vendor Directory

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- 6 asynchronous DCE interface channels hook up directly to terminals and printers (no wiring changes required).
- 2 asynchronous or synchronous interface channels (DCE or DTE) are optimized for connection to modems, printers, CRTs, and similar devices.
- Boards may be cascaded for up to 32 channels.
- Includes programmable Baud rates and many other convenience features.

Like our best-selling Interfacer 1 and Interfacer 2 boards, Interfacer 3 meets the most demanding electrical and mechanical specifications, and is built to the same stringent standards that have established our position as the leader in the S-100 field.

Starting in June, multi-user systems will be able to enjoy CompuPro quality interfacing in an extremely convenient format. Interfacer 3 is available at finer computer stores worldwide, or order directly from us.

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