International Product Showcase

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It happened on a freezing Saturday in February.

Joe Reiley, a Hewlett-Packard test and measurement support engineer, was at a wedding in Pottstown, Pennsylvania. The office was the furthest thing from his mind, when suddenly his beeper went off.

In minutes, Joe was on the phone to Travis Field, the support engineer for Smith Corona in Cortland, New York. An HP test system crucial to Smith Corona's production line had gone down. Suddenly, Joe's thoughts turned to figuring out how to get Smith Corona's production line back up. Joe bid the other guests goodbye and ran to his car.

After driving through a blinding snow storm over icy mountain roads, Joe pulled into Smith Corona at 10:30 pm. A thorough analysis of the problem made it clear they needed extra parts, so Joe called another HP support engineer, Pete Nahrgang, in Valley Forge. Working through the early morning, Pete took parts from a back-up HP system, then flew them to Cortland by special courier. By Sunday afternoon, just 24 hours after Joe's beeper first went off, Smith Corona's production line was up again.

True stories like this prove HP's dedication to responsive customer support throughout the world. We'll tailor our hardware, software and education services to your test and measurement needs. With one of the largest support organizations in the industry, we're committed to keeping your production line up and running. For more information, call your local HP sales office or circle the reader service number.

There is a better way.

When Smith Corona's production line went down, HP support was up and running.
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Developing a PC-based test system with standard hardware and software saves valuable development time and produces a higher quality system. That's why National Instruments hardware and software products are built upon industry standards.

Our GPIB boards use the NAT4882™ chip for complete IEEE-488.2 compatibility. And our LabWindows® software combines powerful development tools with standard programming languages.

With LabWindows, you have the software tools you need to integrate all of the hardware in your test system. Use high-level 488.2 routines to simplify system programming or use drivers from the LabWindows Instrument Library to control your GPIB and VXI instruments without programming them at all.

LabWindows has tools for all phases of your development—data acquisition, analysis, and presentation. You can even create a graphical user interface so your test system is easy to operate.

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Our Model 91 will make your pulse race and help you function better.

Introducing the latest member of the 90 Series family: Model 91 Synthesized Pulse Function Generator. It delivers functions and pulses to 20 MHz with five digit frequency accuracy. Out the rear it has pulses to 50 MHz and a 100 MHz clock output. Choose ECL, CMOS or TTL levels, or set your own.

The functions and pulses can be swept or modulated, and there is even GPIB programmability. Plus an external frequency input that lets you use the Model 91 as a frequency counter.

With all these capabilities, Model 91 redefines the concept of an all-purpose benchtop instrument.

About all it doesn’t do is generate arbitrary waveforms, but there’s the Wavetek Model 95 Synthesized Arbitrary Function Generator for that.

Of course if you want even greater pulse generation capability, our four-channel Model 869 is among the most accurate pulse generators in the world.

For more information about our multi-purpose function generators, high performance pulse generators, or test development and arbitrary waveform software, call Wavetek at 1-800-874-4835.
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DESIGN FEATURES

Computer-Aided Engineering

Schematics battle equations for design representation

Debates have raged for years over whether equations or logic schematics are the best design form. Today, that debate is overshadowed by a shift toward synthesis—mapping design representations into silicon.—Ray Weiss, Technical Editor

Instruments

DMM calibration shortcuts pose question of confidence

Simpler methods of calibrating 7.5- and 8.5-digit digital multimeters let you adjust the overall accuracy of an instrument using as few as two external standards—or no standards at all. The methods are innovative but depart from principles the calibration community has cast in stone.—Brian Kerridge, Technical Editor

Components

Delay lines take on timing tasks

As system designs get more complex and operating speeds get faster, timing must be extremely precise. Programmable delay lines offer designers a way to make adjustments in circuit timing and maximize the performance of today's high-speed systems.—Tom Ormond, Senior Technical Editor

Computers and Peripherals

Arm yourself with LAN know-how

Setting up a local-area network is complicated—especially if you've never done it before. A clear idea of what you want to accomplish as well as a basic understanding of your hardware and software alternatives will help you deal with vendors and consultants.—Dan Strassberg, Technical Editor

Continued on page 7
Introducing SCOPEMETER.

There's More Than One Reason to Reach For It.

In fact, there’s every reason to reach for ScopeMeter. Because only ScopeMeter combines the expertise of Fluke and Philips to bring you a dual-channel digital scope along with everything you’ve come to expect from Fluke digital multimeters. The result: an integrated scope-and-multimeter that lets you see a waveform and digital meter display at the same time from the same input. Or switch between dedicated high-performance Scope and Meter functions with the touch of a key. That makes it faster and easier than ever to capture, store and analyze precisely what you’re looking for. At a price that looks good, too.

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- 50 MHz digital storage scope and 3000-count digital multimeter in one handheld package.
- Precision Min Max Record and 40 ns Glitch Capture make it easy to troubleshoot intermittent failures.
- Simultaneous waveform and digital display on a backlit screen you can read across the room.

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- Three-year warranty from Fluke.

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- Autoset automatically sets voltage, time and trigger functions.
- Safety-designed BNC connectors and probes simplify floating measurements.

Go Wherever You Go.
- Runs on rechargeable NiCad batteries, standard C-cells or the included line voltage adapter/battery charger.
- Adjustable tilt-stand comes in handy as a hanger, too.
- Compatible with a wide range of Fluke multimeter accessories.

EDITORS’ CHOICES

Wideband monolithic op amp
Mask-programmable gate arrays

PRODUCT UPDATES

8-bit microcontrollers
Transceiver IC
FPGA software package

PRODUCT REVIEWS

Computer-Aided Engineering
Instruments
Components
Computers and Peripherals

DESIGN IDEAS

Circuit adjusts duty cycle, not frequency
Filter quashes 60-Hz interference

LITERATURE

Hardware and Interconnect Devices
Software
Integrated Circuits
Power Sources

DEPARTMENTS

News Breaks
Signals & Noise
Editorial
Career Opportunities
EDN’s Acronyms & Abbreviations
EDN’s International Advertisers Index

EDN December 19, 1991

ANY WAY YOU SLICE IT,
GENERATION COVERS EVERY

The squeeze is on. Today the PC market is rapidly concentrating into three segments: Notebooks, Desktops and Workstations. And once again, Conner has anticipated these changes.

Which is why we're introducing our newest wave of high-performance 2.5-inch and 3.5-inch drives to meet the needs of each of these evolving market segments.

For the notebook market, take our newest Pancho drive. With 85 Mbytes, it offers the highest capacity available in a light weight, patented 2.5-inch form factor. Low power consumption, rugged packaging and a compact form factor make it the ultimate choice for 386SX and 486SX-based notebook computers.

Then there's our new Jaguar Series for the desktop market — 3.5-inch drives offering 85 and 170 Mbytes. A 17 msec. average seek time and a light weight, patented 1-inch
CONNER'S NEWEST
SEGMENT OF THE MARKET.

high form factor make them ideal for a full range of desk­
top computers.

For workstations, we’re introducing two new 3.5-inch
drives—the 210 Mbyte Cougar and 540 Mbyte Summit. Cougar
is the highest performance low-profile drive on the market
today. While Summit delivers the greatest capacity and
performance of any 3.5-inch drive. Both provide a fast average
seek time of 12 msec., a 2.5 Mbyte per second sustained
transfer rate and a SCSI-2 interface.

It’s all a part of our innovative sell-design-build business
philosophy. To identify our customer’s needs sooner. Then
fill them faster with the most advanced products. In fact,
we’re the technological leader with nine patents issued and
27 pending. Which is why more and more PC users are
asking for systems with Conner drives.

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squeeze on your systems, call us today. We’ll guarantee you
the most refreshing results.
NEW SAMSUNG VI
FOR HIGH PERF
The new Samsung video RAMs will let you take performance to some heights that are—well, dizzying.

And since high performance is the reason for using video RAMs, that’s good news.

In speeds up to 100 nanoseconds, our new 64Kx4 and 256Kx4 parts are industry-standard in every respect. And they’re fabricated with the high level of quality and reliability that has made Samsung a leader in DRAMs, SRAMs, and specialty memories.

### VIDEO RAMs FROM SAMSUNG

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Organization</th>
<th>Package</th>
<th>Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>KM424C64</td>
<td>64Kx4</td>
<td>DIP, ZIP</td>
<td>100, 120 ns</td>
</tr>
<tr>
<td>KM424C256</td>
<td>256Kx4</td>
<td>ZIP, SOJ</td>
<td>100, 120 ns</td>
</tr>
</tbody>
</table>

Additional VRAM organizations and densities are in development now. And as we increase efforts in several product categories, we are in fact rolling out a committed, broad-based Graphics offering—with VRAMs, with our new RAM DACs, and with an upcoming Clock Generator. In all, a whole Graphics line.

In the meantime, our video RAMs will let you put on quite an act.

For data sheets, call 1-800-423-7364, or 408-954-7229 today. Or write to VRAM Marketing, Samsung Semiconductor, 3725 No. First St., San Jose, CA 95134.
IN THE ERA OF MegaChip™ TECHNOLOGIES

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[Image of three men in an office, one on the phone, another writing, and the third observing.]
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The new XGA standard has opened up an era of higher performance for PC graphics. And when IBM licensed their technology to INMOS, a division of SGS-THOMSON Microelectronics, as manufacturer and sole supplier of the IBM XGA chipset, they did it to ensure that the XGA parts got to the market quickly and reliably, setting the stage for XGA to become the next volume standard in PC graphics. Specifically designed for PCs, XGA is already available to support the MicroChannel Architecture bus, and an AT bus-compatible version is under way. The new XGA standard offers significant enhancements over VGA with:

- higher speed
- higher resolution (up to 1024 × 768)
- more colors (256 up to 64K) giving photo-realistic multimedia-style images
- optimized graphics interface for better windowing
- optimization for use with latest generation processors

Fully VGA compatible, XGA performance specs offer a package that is way ahead:

- 132 column text mode
- extended graphics function mode, including hardware sprite and coprocessor hardware drawing assist
- 90% faster than IBM VGA under DOS, 55% faster under OS/2
- 67% faster running Microsoft Windows applications

**TWO CHIPS THAT SET THE STANDARD**

The IBM compatible XGA chipset consists of two advanced VLSI chips, the INMOS IMS G190 XGA Serializer Palette DAC in a 144 pin CQFP and the INMOS IMS G200 XGA Display Controller in a 184 pin PQFP. A major advantage of the IMS G200 is its on-chip coprocessor which offloads tasks from the host processor and allows it to support:
• 1, 2, 4, and 8 bit pixel and bit block transfers
• line draw
• area fill
• logical and arithmetic pixel mixing
• map masking
• scissoring
• X, Y axes addressing

FULL SOFTWARE SUPPORT is offered for the IBM compatible XGA chipset with the following drivers available:

• DOS Application Interface (DOS AI)
• OS/2 Presentation Manager (OS/2 PM)
• Windows 3.0
• Double Byte character set

Plus a programmer's guide so you can develop your own BIOS software.

AVAILABLE NOW
Yes, the standard IBM MicroChannel Architecture-compatible XGA chipset is available right now. Just call or fax one of the SGS-THOMSON locations listed below and get details on delivery and price.

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MICROELECTRONICS
access to technology
WITH TRW'S VIDEO ENCODER, ANYONE CAN PRODUCE PROFESSIONAL VIDEOS WITHOUT HOLLYWOOD BUDGETS.
The monolithic Video Encoder is here. Created by TRW, the film and production industry's leading supplier of high-performance ICs. And the only company ever to be awarded an Emmy for its video IC technology.

Now, TRW brings you the first in its new line of affordable multimedia ICs for desktop video: The TMC22090.

And that means converting RGB, YUV or color-indexed computer images and graphics into studio-quality NTSC, PAL or S-Video signals can now be done with a single, low-cost chip. One fabricated in TRW's Omicron-C™ 1 µ CMOS process. Packaged in an 84 lead PLCC. And, of course, designed with the full-spec performance that is synonymous with TRW standards.

The TMC22090 boasts a 256x8x3 color lookup table, a pixel mask register and compatibility with 171 and 176 RAMDACs. All of which means transparent interface with existing device drivers.

Better still, the high performance Hollywood has come to rely on is provided by 4:4:4 digital encoding, oversampled 10-bit outputs, and built-in test signals. The TMC22090 even gives you a JTAG interface for low cost production testing. So for everything from simply providing an affordable video output for computer display boards, to developing complex desktop video workstations, you can design in confidence. With the video encoder from the leader in video ICs: TRW.

And you can count on TRW to keep you at the forefront of multimedia, too. This Video Encoder, after all, is just our debut. We've got some great sequels in development.

For data sheets, applications and other information on TRW's TMC22090 Video Encoder, as well as to be first in line for coming attractions, call or write today:

TRW LSI Products Inc.,
P.O. Box 2472, La Jolla, CA 92038
(619) 457-1000, FAX (619) 455-6314
(800) TRW-LSIP (800) 879-5747
Oh no. Please, not now. Not with manufacturing release next week.

The Prototype Doesn’t Work.
Six ASICs, fifteen PLDs and the whole thing’s gone south. Maybe I should go south too. Yeah, hop a bus. Head for Mexico.

The Prototype Doesn’t Work.
Software? Could be. Hardware? Might be. So where do I start? At the beginning, of course. And just where is that, smart guy?

The Prototype Doesn’t Work.
And my performance review comes up next month. Maybe they’ll just forget about all this, right? Yeah. Sure.

The Prototype Doesn’t Work.
Wait. What about that glitch in the handshake on the first pass? Couldn’t reproduce it. Maybe it just reproduced itself.

The Prototype Doesn’t Work.

These are just a few of the reasons Tek makes a complete line of scopes, logic analyzers and signal sources. Instrumentation that can quickly get to the core of your prototype’s problems. Whether they’re digital, analog or software. Because even when your prototype doesn’t work, Tek does. Talk To Tek/1-800-426-2200

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Test and Measurement
SECOND ANNUAL INNOVATION AWARDS PRESENTED AT WESCON

On November 19 at a banquet and reception at Wescon/91, the EDN staff presented the second annual Innovation and Innovator of the Year awards. The team of Paul Gullick and Arlie Conner from In Focus Systems were named Innovators of the Year. The team developed a triple super-twisted nematic (TSTN) LCD that furnishes brighter pictures than other LCDs. EDN presented a check for $10,000 in their names to donate to the university of their choice.

Innovation winners were selected in seven product categories. The ISD10xx analog storage ICs from Information Storage Devices (San Jose, CA) won for ICs and semiconductors. The HP54600A 100-MHz digital storage oscilloscope from Hewlett-Packard (Colorado Springs, CO) won for test and measurement. For CAE/CAD, the winner was the Falcon Framework for Concurrent design from Mentor Graphics (Wilsonville, OR). In Focus won again in computers and peripherals with the color LCD technology. The Isocon Interconnection System from Rogers Corp (Tempe, AZ) won for components, hardware, and interconnect. IRMX for Windows from Intel Corp (Hillsboro, OR) won for software. And, last but not least, the Genesis high-power-density battery from Gates Energy Products Inc (Gainesville, FL) won for power sources. For complete product descriptions, see the November 21, 1991, edition of EDN. All winners were selected by votes from EDN readers.—Susan Rose

SINGLE CHIP EMBEDS MS-DOS SYSTEMS

NEC Electronics Inc's DOS engine is a single chip that encompasses an entire IBM PC/XT, except for external memory. Aimed at embedded systems, this chip lets designers build a DOS-compatible system with a minimum number of chips. The DOS engine includes a clock generator, a DMA controller (8273A compatible), an interrupt controller (8259A compatible), a counter/timer (8254 compatible), a speaker interface, a memory controller, an expanded-memory system (EMS) controller, and a programmable PC/XT or PS/2 keyboard and mouse interface. Designed around the NEC V20/30, the DOS Engine is based on an 0.8 μm static process. Future versions will include an ASIC core that you can tailor to your needs. The core will have as many as 20,000 gates for customer-specific circuits that link to an internal 8-bit IBM PC/XT bus. The engine can access as much as 16 Mbytes of virtual memory through its EMS hardware.

The engine operates at 3 to 5V. Running at 8 MHz and 3V, it consumes 5 mA and operates with a minimum instruction-execution time of 250 nsec. Initially, there are two versions of the chip: the V41 μPD70270, based on the V20HL with an 8-bit external bus; and the V51 μPD70280, based on the V30HL with a 16-bit external bus. Both chips are available in a 160-pin plastic quad flatpack (PQFP) with 10-, 12-, and 16-MHz speed grades. The ASIC version comes in a 208-pin PQFP. From $20 (10,000). NEC Electronics Inc, Mountain View, CA, (415) 960-6000.—Ray Weiss
NEWS BREAKS

PROCESS YIELDS FAST AMPS, PIN DRIVERS, AND ASICs

Harris Semiconductor today announced a series of high-speed linear products developed using the company's new complementary bipolar, silicon-on-insulator process. UHF-1 yields npn and pnp transistors with switching speeds greater than 8 and 4 GHz, respectively, and betas of 100 and 60, respectively. The process implements dielectric isolation with trench-isolation and bonded-wafer techniques. The combination of bonded wafers and trenches provides complete isolation between transistors, which results in reduced parasitic capacitance, resistance to latchup, and reduced leakage current at high temperatures. The process's values of beta, breakdown, and early voltage don't compromise the transistors' dc performance to achieve high speed. Size is also a crucial factor. The new process yields faster but smaller devices than were possible with the company's older process—a fact which should let the company offer performance increases without similar cost increases.

The first products built using this high-speed process include op amps, a closed-loop buffer, a pin-driver IC, and ASICs. The HFA1100 family of op amps ($9.95 (100)) features an 850-MHz unity-gain bandwidth, 2500V/µsec slew rates, 11-nsec settling times to 0.1% accuracy, and 0.04-dB gain flatness to 50 MHz. The HFA1110 closed-loop buffer ($9.95 (100)) has a 700-MHz bandwidth, and you can configure the buffer for voltage gains of ±1 or 2 without external components. The buffer's 60 mA of output current makes it appropriate for use as a cable driver and distribution amplifier. The HFA5250 500-MHz pin driver ($48 (1000)) guarantees an output impedance of 50Ω with a maximum variance of ±2Ω. Finally, the company has tied the process parameters into its Fastrack ASIC Design System, offering tile arrays and device-level designs. Designers can optimize the HTA3000 tile array or HDI3000 devices for either high speed or low-power consumption. The tile array consists of 10 device tiles, the elements of which can be op amps, current-feedback amps, comparators, and references. The HDI3000 library includes four npn and pnp transistor types. Typical NRE for the tile and device-level designs is $97,000 and $131,000, respectively. Harris Semiconductor, Melbourne, FL, (407) 724-3704, FAX (407) 724-3937.—Anne Watson Swager

SHAMIR TOUTS BUSINESS OPPORTUNITIES IN ISRAEL

At a dinner for American industrialists in Boston in November, Israeli Prime Minister Yitzhak Shamir encouraged US high-tech companies to come to Israel. The dinner was part of a recent effort to raise interest for increased American investments in Israel. Ambassador Zalman Shoval said that the climate in Israel especially favors high-tech development: Many of the new Russian immigrants are engineers who want to stay in Israel. The country also has favorable trade relations with the US and Europe, Shoval said. Already Digital Equipment Corp, Intel, Motorola, and National Semiconductor have major facilities in Israel. For more information on the business opportunities in Israel, contact the nearest Israeli Consulate.—Susan Rose

ADD FOUR SERIAL PORTS TO YOUR WINDOWS 3.0-BASED PC

The Plus 8 multiport serial board from Star Gate lets you plug more than two serial devices into your Windows-based PC. The board contains hardware drivers that provide full-duplex asynchronous communication for Windows 3.0 in each of its three operating modes—real, standard, and enhanced. As a result, there is no need for your PC to load additional device drivers in order to accommodate a Windows environment. The board plugs into your PC's expansion chassis and uses two 8051 µPs. The RS-232C version costs $570, and the RS-422 model costs $670. Star Gate, Solon, OH, (800) 782-7428, (216) 349-1860, FAX (216) 349-2056.—JD Mosley
No More Constraints!

With MicroSim Corporation's Digital Simulation option for PSpice, the dichotomy between analog and digital simulation vanishes. Here’s why!

Native Mixed Analog and Digital Simulation
You’ll experience true mixed-mode simulation of your circuits including circuits with tightly coupled feedback between analog and digital sections. All of the PSpice analog simulation features with which you’re familiar are at your disposal for mixed-mode simulation.

Outstanding Performance
With our event-driven logic processing algorithm, digital components are processed at logic simulation speeds. Over 10,000 logic gates can be simulated in a circuit along with hundreds of analog components. With Digital Simulation, your circuit’s logic states and propagation delays are computed in a snap.

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That’s what you can count on for all PSpice mixed-mode and analog simulations. With Digital Simulation’s 5 input levels and 64 output strengths, it’s even better.

Full Integration with Schematics
Draw your mixed-mode circuits with our newly introduced Schematics circuit editor. Then simulate and analyze your design with PSpice and Probe directly from the Schematics program. In Probe, your circuit’s analog and digital waveforms can be displayed simultaneously with a common time axis.

Extensive Libraries
In addition to PSpice’s libraries with over 3,500 analog components, Digital Simulation libraries offer over 1,500 TTL and CMOS components. Optional power supply pins are available on all digital components allowing your circuit’s components to run from different power supplies and CMOS device thresholds to change with the power supply voltages.

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SMALL POWER SUPPLIES TARGET PORTABLE PCs

Two new families of switching power supplies from Tamura serve applications ranging from portable data-acquisition equipment to notebook and portable PCs. The company's new products include 1-in.-high, 50W units designed to mount inside a chassis. The FVS and FVM series products include single and triple output models that are smaller than a home-video cassette. The products range in price from $90 to $110, based on configuration and quantity ordered. Meanwhile, the company offers the SWA family products that target external power-supply applications. You can choose from 15, 20, and 30W units that plug directly into wall sockets or 40 and 60W table-top supplies. The external units range in price from $40 to $120. All of the new supplies can handle universal ac inputs that range from 85 to more than 200V. Tamura Corp, Carson, CA, (310) 638-1790, FAX (310) 638-9956.—Maury Wright

DSP CHIP SUITS PARALLEL-PROCESSING APPLICATIONS

The TMS320C40 DSP chip from Texas Instruments provides the processing power necessary for embedded parallel-processing tasks such as computer imaging and vision, 3-D graphics, neural networks, robotics, and speech recognition. The chip has six communication ports, two memory buses, and a 6-channel DMA coprocessor. Operating specs include 275 million operations/sec and 320-Mbyte/sec throughput. Both the manufacturer and third-party vendors offer parallel-processing development tools for the chip. Samples are available now for $560. Texas Instruments, Dallas, TX, (800) 336-5236, ext 700, (214) 995-6111, ext 700.—JD Mosley

DATA-COMPRESSION IC HANDLES 3000 SIMULTANEOUS TASKS

Data-compression ICs currently let you effectively double the capacities of tape and disk drives, but the model 9705 compression chip from Stac Electronics expands that coverage to networks by incorporating support for as many as 1500 simultaneous, full-duplex data streams (3000 tasks). Because of network overhead, the chip provides a typical compression ratio of 4:1 for network data packets. Consequently, you can effectively quadruple a network's available capacity through data compression.

The IC employs the same compression/decompression algorithm as its single-tasking predecessor, the model 9704, and is pin- and software-compatible with the older device. At its maximum clock rate of 50 MHz, the new device compresses 2.5 Mbytes of data/sec and decompresses at 6 Mbytes/sec. For low-power applications, you can also put the chip into a sleep mode that reduces current consumption to 300 µA. Samples of the IC are available; production quantities will be available in the first quarter of 1992. The chip costs $24 (50,000). Stac Electronics, Carlsbad, CA, (619) 431-7474.—Steven H Leibson

X-TERMINAL SOFTWARE SERVES MS-DOS AND WINDOWS

AGE introduced two new software products that let PCs act as X servers in an X-Window application. Xoftware for DOS supports video adapters ranging from monochrome to super VGA to 8514/A. The product include a hot key feature that lets you swap between X-server-DOS and Microsoft-Windows sessions. The product works with MS-DOS 5.0 and costs $395—or $465 when bundled with TCP/IP (transmission control protocol/internet protocol) networking software. Xoftware for Windows, meanwhile, lets you use Microsoft Windows as a local window manager, and still provides the X-server capability. You can cut and paste between Microsoft Windows and X-Window applications. The software can work with any graphics hardware that comes with a Microsoft Windows driver. The Windows software costs $495. AGE, San Diego, CA, (619) 455-8600, FAX (619) 597-6030.—Maury Wright
**PRODUCTS:** Metal film and wirewound resistors.

**OBJECTIVE:** Develop efficient systems for supplying and procuring MIL-style components.

**UNITS INVOLVED:** Raytheon and Dale Electronics, Inc.

For more than two decades, Raytheon and Dale® have developed a strong manufacturer/vendor relationship focused on close communication and a common goal to continually improve quality.

Today, Dale works closely with other Vishay companies (including Angstrohm and Ultronix) in supplying established reliability resistors used in the Patriot, Sparrow and other programs of the Raytheon Missile Division. Military specifications involved include: MIL-R-39005, MIL-R-39007, MIL-R-39009, MIL-R-39017, MIL-R-55182, MIL-R-55342 and MIL-R-83401.

In helping Raytheon meet the exacting requirements of these programs, Dale, in 1984, became the first OEM vendor to Raytheon to install an on-line computer terminal, allowing direct-order capability with several Dale plants.

Since then, this system has been tailored to allow Raytheon purchasing locations to obtain a wide range of information on orders to Dale including everything from price, to production status, to a shipping date.

“In essence,” a Dale spokesperson commented, “Raytheon can access anything we can in relation to any or all of their orders. More recently, Dale helped Raytheon pioneer their first system for electronic data interchange (EDI).”

Quality, also, has played a big part in the relationship. With a history of tens of millions of parts shipped to Raytheon, Dale has maintained exceptionally high quality levels. This is why Raytheon has chosen Dale for several quality and service awards over the last few years.

For more information on how Dale's commitment to effective partnering can benefit your operation, please contact Joe Matejka, Vice President, Quality Assurance, Dale Electronics, Inc., 1122 23rd Street, Columbus, Nebraska 68601-3647. Phone 402-563-6511. Fax 402-563-6418.
dc to 3GHz from $1145

lowpass, highpass, bandpass

- less than 1dB insertion loss
- greater than 40dB stopband rejection
- surface-mount
- BNC, Type N, SMA available
- 5-section, 30dB/octave rolloff
- VSWR less than 1.7 (typ)
- rugged hermetically-sealed pin models
- constant phase
- meets MIL-STD-202 tests
- over 100 off-the-shelf models
- immediate delivery

low pass, Plug-in, dc to 1200MHz

<table>
<thead>
<tr>
<th>Model No.</th>
<th>Passband MHz loss &lt; 1dB</th>
<th>Stopband MHz loss &gt; 20dB</th>
<th>Stopband MHz loss &gt; 40dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLP-4</td>
<td>DC-5 8-10 10-200</td>
<td>DC-25 330-400 400-1200</td>
<td></td>
</tr>
<tr>
<td>PLP-10.7</td>
<td>DC-11 19-24 24-200</td>
<td>DC-370 415-550 550-1200</td>
<td></td>
</tr>
<tr>
<td>PBP-214</td>
<td>24.1 19.2-23.6 23.6-36.5</td>
<td>DC-420 575-800 800-2000</td>
<td></td>
</tr>
<tr>
<td>PBP-314</td>
<td>24.1 19.2-23.6 23.6-36.5</td>
<td>DC-520 750-900 900-2000</td>
<td></td>
</tr>
<tr>
<td>PBP-50</td>
<td>24.1 19.2-23.6 23.6-36.5</td>
<td>DC-620 1150-2000 2000-4000</td>
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</tr>
<tr>
<td>PBP-75</td>
<td>24.1 19.2-23.6 23.6-36.5</td>
<td>DC-750 1350-2000 2000-4000</td>
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<tr>
<td>PBP-100</td>
<td>24.1 19.2-23.6 23.6-36.5</td>
<td>DC-900 1500-2000 2000-4000</td>
<td></td>
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<tr>
<td>PBP-150</td>
<td>24.1 19.2-23.6 23.6-36.5</td>
<td>DC-1050 1750-2000 2000-4000</td>
<td></td>
</tr>
<tr>
<td>PBP-200</td>
<td>24.1 19.2-23.6 23.6-36.5</td>
<td>DC-1200 2000-2100 2100-2500</td>
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</tr>
</tbody>
</table>

Surface-mount, dc to 570MHz

<table>
<thead>
<tr>
<th>Model No.</th>
<th>Passband MHz loss &lt; 1dB</th>
<th>Stopband MHz loss &lt; 40dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLF-21.4</td>
<td>DC-22 32-41 41-200</td>
<td>DC-190 290-380 380-900</td>
</tr>
<tr>
<td>SCLF-45</td>
<td>DC-65 75-90 90-200</td>
<td>DC-340 520-750 750-2000</td>
</tr>
<tr>
<td>SCLF-135</td>
<td>DC-135 210-300 300-600</td>
<td>DC-510 780-1600 1600-2500</td>
</tr>
</tbody>
</table>

Flat Time Delay, dc to 1870MHz

<table>
<thead>
<tr>
<th>Model No.</th>
<th>Passband MHz loss &lt; 1dB</th>
<th>Stopband MHz loss &gt; 20dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>PBP-38</td>
<td>DC-25 78-117 117-150</td>
<td>DC-260 380-500 500-1000</td>
</tr>
<tr>
<td>PBP-117</td>
<td>DC-65 234-312 312-400</td>
<td>DC-540 800-1500 1500-2500</td>
</tr>
<tr>
<td>PBP-170</td>
<td>DC-90 280-360 360-440</td>
<td>DC-720 1100-1750 1750-2000</td>
</tr>
<tr>
<td>PBP-200</td>
<td>DC-120 354-460 460-570</td>
<td>DC-900 1900-2500 2500-3000</td>
</tr>
<tr>
<td>PBP-487</td>
<td>DC-180 460-620 620-800</td>
<td>DC-1200 3000-4000 4000-5000</td>
</tr>
<tr>
<td>PBP-1870</td>
<td>DC-650 3740-6000 6000-9000</td>
<td>DC-2400 7800-14000 14000-20000</td>
</tr>
</tbody>
</table>

high pass, Plug-in, 27.5 to 2200MHz

<table>
<thead>
<tr>
<th>Model No.</th>
<th>Stopband MHz loss &lt; 40dB</th>
<th>Stopband MHz loss &gt; 20dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>PHP-25</td>
<td>DC-13 13-19 19-25</td>
<td>DC-120 210-290 290-400</td>
</tr>
<tr>
<td>PHP-50</td>
<td>DC-25 25-29 29-41</td>
<td>DC-260 380-500 500-6000</td>
</tr>
<tr>
<td>PHP-100</td>
<td>DC-45 45-55 55-70</td>
<td>DC-520 650-800 800-1200</td>
</tr>
<tr>
<td>PHP-150</td>
<td>DC-70 70-95 95-130</td>
<td>DC-750 1000-1500 1500-2500</td>
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<tr>
<td>PHP-175</td>
<td>DC-70 70-95 95-130</td>
<td>DC-850 1100-1600 1600-2200</td>
</tr>
<tr>
<td>PHP-200</td>
<td>DC-90 90-116 116-160</td>
<td>DC-950 1200-1800 1800-2500</td>
</tr>
<tr>
<td>PHP-250</td>
<td>DC-100 100-150 150-220</td>
<td>DC-1100 2000-3000 3000-4500</td>
</tr>
<tr>
<td>PHP-300</td>
<td>DC-145 145-170 170-260</td>
<td>DC-1200 3000-4500 4500-6000</td>
</tr>
</tbody>
</table>

bandpass, Elliptic Response, 10.7 to 70MHz

<table>
<thead>
<tr>
<th>Model No.</th>
<th>Stopbands &gt; 20dB at MHz</th>
<th>Stopbands &gt; 35dB at MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>PBP-10.7</td>
<td>10.7 9.6-11.5 11.5-13.5</td>
<td>DC-220 330-400 400-1200</td>
</tr>
<tr>
<td>PBP-21.4</td>
<td>21.4 19.2-23.6 23.6-36.5</td>
<td>DC-330 440-600 600-1000</td>
</tr>
<tr>
<td>PBP-31.4</td>
<td>31.4 27.5-33.0 33.0-45.0</td>
<td>DC-440 550-800 800-1200</td>
</tr>
<tr>
<td>PBP-50</td>
<td>50.0 45.0-60.0 60.0-80.0</td>
<td>DC-650 900-1300 1300-2000</td>
</tr>
<tr>
<td>PBP-70</td>
<td>70.0 65.0-77.0 77.0-100.0</td>
<td>DC-850 1350-1800 1800-2500</td>
</tr>
</tbody>
</table>

Constant Impedance, 21.4 to 70MHz

<table>
<thead>
<tr>
<th>Model No.</th>
<th>Stopband loss &gt; 1dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>PHP-30</td>
<td>30.0 25.3-35.0 35.0-50.0</td>
</tr>
<tr>
<td>PHP-50</td>
<td>50.0 41.5-60.0 60.0-90.0</td>
</tr>
<tr>
<td>PHP-70</td>
<td>70.0 58.8-74.4 74.4-100.0</td>
</tr>
</tbody>
</table>

Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $39.95

NOTE: All 333 and 1870 only with connectors, at additional $2 above other connector models.

P 0 Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661

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AMP SDL connectors are a cost-effective alternative to crimp-snap type products, whether you do-it-yourself or order custom cables from us in flat, round, or coiled styles. Either way, you benefit from the same ease of application, the same well-thought-out design. And you walk away with the reliability and durability you need.

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AMP Interconnecting ideas
People say boundary in low cost, high quality

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Increasing device complexity. Rising pattern development costs. High density packaging. Disappearing nodal access. These are the board test problems boundary scan was created to solve. Which is fine in theory. Only problem is there hasn't been any way to put boundary scan to the test. Until now.

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Whether you're testing one boundary-scan part or boundary-scan networks, VICTORY software automatically gives you 100% pin-level fault coverage. Using the IEEE 1149.1 and BSDL standards, it takes VICTORY only a minute or two to generate test patterns. It would take a programmer days, even weeks to deliver the same fault coverage for conventional designs.

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scan is a breakthrough board testing.

theory.

feedback you need to eliminate defects where it's most cost-effective—at the source.

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With boundary-scan design and VICTORY software, you won't need bed-of-nails access on nodes where boundary-scan parts are interconnected. That means fewer test pads. Fewer test probes.

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CIRCLE NO. 73

EDN December 19, 1991
Missing information
In the article on FPGA design methods (EDN, August 5, 1991, pg 122), EDN didn’t include Synoptics as a manufacturer of image-processing boards. The company offers boards for the IBM PC/AT and VMEbus based on the ADSP2100 and a proprietary image processor. The boards offer recursive filtering and slow- or variable-scan frame-grabber modes for RS-170 or CCIR formats. Prices range from $1300 to $34,000.

Synoptics
Paragon Towers
233 Needham St
Newton, MA 02164
Phone (617) 527-4461
FAX (617) 527-4084.

EDN’s article on DSP coprocessor boards in the September 16, 1991, issue, pg 108, also omitted a vendor: Mercury Computer Systems
600 Suffolk St
Lowell, MA 01854
Phone (508) 458-3100
FAX (508) 458-9580.

Mercury’s MC family uses the i860 RISC µP. The article noted that although the i860 is not technically a DSP µP, several vendors have found it to be a very powerful DSP engine. EDN called attention to one such firm’s products and indicated that you could expect to see i860-based DSP boards from other companies. Although any i860-based board can perform DSP operations, only a few vendors of such boards emphasize the DSP capabilities.

Engineers more than 40 years old now often cannot even get jobs in engineering. They have to leave engineering for law, or more likely, as common laborers. Yet our educators and government bureaucrats keep singing the refrain, “Shortage of engineers.”

We are now second-class citizens in almost all areas of electronics because engineering leadership has been reduced to a form of rote labor. Our auto-industry products and major appliances are being made overseas, as well as most of our electronics.

Elimination of the exemption from requiring engineering activities to be headed by qualified licensed professional engineers can help, if it isn’t already too late! A measure of the severity of the situation can be drawn from the fact that whereas new law graduates start as clerks with salaries of $70,000 or more a year, young engineering graduates can’t do better than about $30,000 a year if they can even find a job. And many job openings list salaries in the low $20,000s.

How long will there be a market for our professional journals and specialty trade journals, let alone college engineering courses, if this continues? Isn’t it time that a balance be restored that can prevent further erosion of our engineering infrastructure?

Keats A Pullen, Jr
American Association of Concerned Engineers Inc
Kingsville, MD

NEXT WEEK IN EDN
In the January 9, 1992, EDN News Edition, look for
• a Product Watch on emulators vs logic analyzers
• a Career Opportunities article on medical electronics
• the beginning of the Management/Diversity series.
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We're also the originators of the Fast Architecture SCSI (FAS) Series for Fast and Wide SCSI-2 applications, as well as the Triple Embedded Controller (TEC) Series, an ideal single chip SCSI solution for disk applications—which includes a disk formatter, buffer controller, and SCSI controller. So when you're looking for the most effective solutions for your next design project, call Emulex's Micro Devices. And let the best name in SCSI put you in the chips.

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risks associated with new product introductions.

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And breathe new life into your designs.
Anyone looking at the electronics industry will see the momentum. And, they will realize that momentum usually relies on evolution. That momentum, and subsequent evolution, is extending to EDN. Starting with our January 20, 1992 issue, you'll see some of the ways in which EDN is evolving to help you better meet your changing needs for information.

A lot of thought and deliberation have gone into our changes and enhancements. In all cases, the new things you'll see arise from communication with our readers. We've looked at the comments on every reader-service card and we've talked with readers in focus groups. We've also run readers' needs surveys to gauge interest in specific types of articles, types of information, and organization, among other things. We know what you want and what you need.

There weren't any great surprises; readers like what we're doing to help them do their jobs better. Nevertheless, you can always improve a product and that's what we've done. For example, you'll see a new cover style. Many of you scanners or skimmers want more information about articles put on the cover. Thus, you'll find article titles and page numbers on the cover in a consistent place every issue. You'll also find our table of contents is easier to use because we're color coding similar articles. The consistent colored labels will identify article types on the cover and throughout each issue. For example, a red or pink bar denotes new products.

We've also added some new sections to EDN. Many of our Special Reports will include an "Editor's Analysis" box that gives engineers and managers distilled information about cost, design, and management issues. Because the electronics business is so closely tied to microprocessors and microcontrollers, we're dedicating special "Processor Update" pages to introductions of µPs, µCs, and related hardware and software tools. Our editors often get their hands on products and will now bench test them. You'll read their findings and critiques in the new "Hands On!" section. Typically, we'll look at computer boards, instruments, design aids, books, catalogs, and other products that we can give a quick review.

Well, there is still more to come, but I'll save that for my next editorial. In the meantime, all of us at EDN wish you and your family a happy holiday season.

Send me your comments via FAX at (617) 558-4470, or on the EDN Bulletin Board System at (617) 558-4241 300/1200/2400, 8, N, 1.
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This reliable operating system takes full advantage of the protected-mode features of the popular Intel386™ architecture. So it opens new avenues for cost-effective solutions.

Of course, iRMX for Windows also opens some powerful options for software

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real-time applications concurrently.

engineers. Like bringing the huge installed base of DOS applications, tools, and the popular Windows environment to real-time development. What's more, as a developer, you'll receive professional support from Intel engineers.

All of which is important when you're racing to bring your application to market.

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EDN December 19, 1991
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Designing and manufacturing a monolithic op amp that has a gain-bandwidth product greater than 100-MHz may no longer be the challenge that it once was to IC manufacturers. However, combining wide bandwidth with gain flatness, low noise, low distortion, low phase error and the ability to supply 100-mA of output current—all at a cost-effective price—is quite another matter.

The AD811 current-feedback op amp from Analog Devices is optimized for wide bandwidth and gain flatness when operating from a ±15V supply. This device also solves the myriad problems presented by the demands of high-definition television (HDTV), medical imaging, and other video applications.

For example, compared with a bandwidth of 3.58 MHz for NTSC and 4.43 MHz for PAL standards, HDTV requires a gain flatness of 0.1 dB over a bandwidth of 30 MHz. At a gain of two, the AD811 meets this requirement handily while providing a minimum 3-dB bandwidth of 120 MHz. Moreover, differential gain and phase—key specifications for preventing color shifts and image distortion—are 0.01% and 0.01°, respectively. Another significant feature of the op amp is its ability to drive two back-terminated 75Ω cables, an important consideration when using the amplifier as a line driver in video routers or distribution amplifiers.

The AD811 is suited for medical-imaging applications, which require low noise and distortion. At 10 kHz, the op amp has a typical noise of 1.9-nV/√Hz. At 10 MHz, THD is -74 dBc, and third-order intercepts occur at 43 dBm.

The op amp also suits high-speed pulse applications, such as infrared imaging and digital oscilloscopes, where transient response is critical. The device has a typical slew rate of 2500V/µsec; settling times are 25 nsec to 0.1% for a 2V step and 65 nsec to 0.01% for a 10V step.

You can use the op amp as a buffer for ADCs and DACs or as a stand-alone gain stage: With a ±15V supply, it has bandwidth of 140 MHz at unity gain and 100 MHz at a gain of ten. Even with a ±5V supply, the op amp has a bandwidth of 80 MHz at unity gain and 70 MHz at a gain of ten. Full-power bandwidth (defined as a 10V p-p voltage swing) is 32 MHz.

Although there are devices from other manufacturers that can equal the device’s performance for a single specification, none combine the total performance capabilities of this op amp. Also, competing devices that exhibit similar performance can’t match this op amp’s cost.

The device is available in industrial (-40 to +85°C) and military (-55 to +125°C) temperature grades. Packages include 8-pin DIPs, 8-pin ceramic DIPs, 16- and 20-pin SOICs, and 20-pin LCCs. An industrial-grade device in an 8-pin plastic DIP costs $3.35 (100) and $2.85 (1000).—Dave Pryce

Analog Devices, 804 Woburn St, Wilmington, MA 01887. Phone (617) 937-2507.

Circle No. 732
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Mask-programmable gate arrays field
as many as 20k raw gates/chip and 270 I/Os

Only a small proportion of board designers use gate arrays or ASICs; most board designers rely on PLAs, PAL devices, and complex discrete devices. These board designers are turning to FPGAs (field-programmable gate arrays) for higher logic densities and I/Os to fill the gap between ASICs and PLDs. FPGAs appeal to PLD designers because of a PLD heritage with fixed logic cells. Crosspoint Solutions has considered the needs of board designers when modeling its CP20K FPGA series on gate arrays.

CP20K FPGAs have a gate-array-like structure with rows of basic gate and register transistor cells. They offer an almost sea-of-gates, gate-array granularity in an FPGA form. Taking advantage of this similarity, the manufacturer has integrated the array libraries and tools with workstation CAE tools from Mentor Graphics, Viewlogic, and Cadence. Thus, gate-array designers can switch to these FPGAs without changing tools. Even better, they can prototype their designs using a relatively low-cost FPGA, thereby minimizing nonrecurring engineering costs.

The one-time-programmable FPGAs fall below current gate-array densities and speeds. Densities range from 2.2 to 20.6k raw gates and reach clock speeds as high as 40 MHz for a counter and 52 MHz for a flip-flop driving three gate levels (fanout = 3) to another flip-flop. FPGAs are slower because of their programmable interconnections. As many as 7 million programmable interconnections may be in the large 20k-gate array, although the company expects only 3 to 5% to be programmed for a typical design. The FPGAs do, however, approach mainstream gate-array I/O counts, with available I/Os running from 91 to 270 pads.

Each array has rows of diffusion layers. A row of gate pairs overlaid with register cells constitutes a single diffusion layer. The FPGA alternates diffusion-layer rows with horizontal rows of routing resources. Lying vertically across these rows is vertical routing metal for local, as well as long routing.

Unlike most FPGAs, which have complex logic cells, the granularity of the Crosspoint cells is at the basic gate level. This fine logic granularity allows designers to work at the gate level. The array's gate transistors are ordered into transistor pairs called transistor-pair tiles, two of which make up a 2-input NAND gate. Register resources are organized into RAM logic tiles that sit on top of four transistor-pair tiles. You can use RAM-logic tiles for combinatorial logic as well, such as multiplexers, XORs, and NORs.

An innovative feature of these arrays is their structuring for register-intensive designs as well as control logic. Each array has a built-in register grid, linking the RAM-logic-tile resistor resources to a memory structure (Read, Write, Column Se-
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memory mix. The more registers there are, the higher the density should be. A built-in clock-distribution network minimizes skew, holding it to 1.3 nsec/clock.

The manufacturer is also fielding a programmer/tester for its arrays. The device ties into the arrays via a standard JTAG (Joint Test Action Group) port, taking four I/O pins running at 20 MHz. In addition, it provides parts pretests: a simple, 2-minute programming test and a production test. A JTAG boundary scan can test the programmed part. A developmental tool set backends standard CAE tools. It allows engineers to interactively hand-place and route, as well as automatically place and route. The tool set handles engineering change orders, and it allows users to freeze or thaw portions of the design for rework. The set provides a delay calculator and a pin and package editor.

The FPGAs use 3.5V internal logic, mainly to support 10V programming. As a side effect, the arrays consume less power than standard 5V parts. In addition, the transition to 3.3+ voltages for future systems will be easy, eliminating the present level translators at the I/O buffers.

The company uses a 0.75-µm, 2-level metal CMOS process for the arrays. The programmable interconnection is a metal-to-polysilicon antifuse with a native R_{off} of 1 GΩ and a programmed R_{on} of 100Ω. Each connection has low capacitance, measuring 0.65 fF per antifuse.

Each chip has five power and ground planes that have four decoupling capacitors. The devices come in ceramic PGAs (pin grid arrays), ceramic quad flatpacks, and plastic quad flatpacks. The CP20420 4245-gate FPGA will be available next month in a 155-pin ceramic PGA for $277.70 (100). The programmer/tester sells for $4000.—Ray Weiss

Crosspoint Solutions Inc, 5000 Old Ironsides Ave, Santa Clara, CA 95054. Phone (408) 988-1584. FAX (408) 980-9594.

Circle No. 733
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EDN December 19, 1991
8051 family gets second wind; new versions extend life of classic μC

Old 8-bit microcontrollers don’t quietly fade away, they just get more peripherals. And so the venerable 8051 family is quietly expanding as Intel and 8051 licensees continue to pour in additional capabilities.

Today’s 8-bit 8051 carries a lot more muscle than did the early versions introduced in the late 1970s. The 8051’s on-chip memory was initially limited to 128 bytes of RAM and 8 kbytes of ROM. Vendors have pushed beyond those limits to include as much as 2 kbytes of on-chip RAM and 32 kbytes of on-chip EPROM. Peripheral muscle has also been added to the microcontroller: as many as nine 8-bit I/O ports, multiple timers and counter arrays, and even a beefed-up math peripheral with a 32-bit divide and 16-bit multiply.

Processor speeds are up, too. Matra and Phillips Components (Sunnyvale, CA) have pushed clock rates to 30 and 33 MHz, respectively, from the original 12 MHz. Other efforts to speed up the 8051 family are focusing on the core’s 12-clock-stage instruction cycle. Oki Semiconductor’s reworked 8051, the nX 65 K series, executes instructions in four clock cycles, compared with the original 8051’s 12 cycles.

New 8051 versions include

- Oki Semiconductor’s one-time-programmable version of its nX 65K series. The architecture of this series is a superset of the 8051 architecture. The series has a fast core and 4, 8, or 16 kbytes of ROM and 128, 256, or 384 bytes of RAM. Prices start at $6.51 (5000). Oki Semiconductor Inc, 785 N Mary Ave, Sunnyvale, CA 94086; (408) 702-1900. Circle No. 734

- Siemens’s SAB/80C517A/88C517A-5. This 8051 version has an additional 2 kbytes of external RAM and as much as 32 kbytes of ROM. Its clock rate is as fast as 18 MHz. The device also has seven I/O ports, a 10-bit ADC (8 channels), six counters, eight 16-bit data pointers, a 16-bit-multiply and 32-bit-divide unit, and a 21-channel PWM. Prices start at $15 (1000). Siemens Integrated Circuit Div, 2191 Laurelwood Rd, Santa Clara, CA 95054; (408) 980-4500. Circle No. 735

- Signetics’s 83C524/87C58. This 512-byte-RAM version has as much as 32 kbytes of ROM or EPROM and runs as fast as 16 MHz. The chip includes two serial ports, three timer/counters, and the company’s FC (Inter Integrated Circuit Bus) serial interface. Prices start at $7.50 (10,000). Signetics Co, 811 E Arques Ave, Santa Clara, CA 94088; (408) 991-2000. Circle No. 736

- Matra’s high-speed 8051s. Based on a fully static design, the 80C52, 80C32, and 80C154 now come in 25- and 30-MHz versions. The 80C154 also comes in 16- and 32-kbyte-ROM versions. The chips have three counter/timers, a full-duplex serial port, and 256 bytes of RAM. The 80C31Ω-30 costs $6 (10,000). Matra Design Semiconductor, 2895 Northwestern Pkwy, Santa Clara, CA 95051; (408) 986-9000; FAX (408) 748-1038. Circle No. 737
And over the last year, several vendors made some significant extensions to the 8051. Intel introduced its 87C58/80C58, which has as much as 32 kbytes of EPROM, and the 87C51FX, which has a set of programmable counter functions. And Signetics pushed out more microcontroller units with its chip-level serial bus, the FC. This bus is part of Digital Equipment Corp’s proposed Access Bus for low-speed desktop peripherals. It may become a standard.

Vendors continue to modify and extend the 8051 because of the device’s popularity. Many engineers like the 8051 because of its many versions and the wide range of on-chip peripherals available. “With the 8051, if I need more power or different peripherals I can just go to another chip,” says Jim Manley, director of electronic design at Span Instruments Inc (Costa Mesa, CA). Many take advantage of this prolific processor family to move to a higher-level language like C from assembly language. They pay for the additional overhead by moving to a more powerful chip.

The 8051 microcontroller has a rather baroque architecture. On one hand, it provides a complete set of processing operations including complex addressing and bit operations. The architecture provides memory-mapped I/O control.

On the other hand, Intel designers made some design compromises that complicate programming the device. For example, the 8051 has a complex addressing scheme that includes indexed, direct, and indirect addressing. But some addressing capabilities apply to only some areas, thus segregating entities that share the same address space (special-function registers share the same space as external RAM, for example). Also, bit operations are confined to an addressing set of 128 bits in local RAM.

On the positive side, the 8051 has direct bit addressing, four register sets in RAM, and a pseudo-Harvard architecture with as much as 64 kbytes each for program and data memory. On the down side, off-chip memory accesses take an additional instruction cycle, making off-chip access expensive. Competing microcontroller units, such as the Motorola 68HC11, take the same time for on- and off-chip accesses. Also, the 8051 has one 16-bit pointer, which makes off-chip addressing difficult. However, Siemens has added a set of eight pointer registers to its 80C517A.

Many engineers find the 8051 easy to learn and program, but they find its peripherals complex. Intel, for example, has gone beyond the original two counter/timers by adding more counters, a programmable counter array, and an up/down counter. Similarly, other vendors have added their own versions of advanced counter peripherals.

Designing in 8051s can be easy. Dallas Semiconductor Corp (Dallas, TX) offers an 8051 superchip, the DS5000. The device is a hybrid: Inside is an 8051 CPU, 8 or 32 kbytes of RAM, and a battery backup—in other words, a complete system.

—Ray Weiss

Intel Corp, 5000 W Chandler Blvd, Chandler, AZ 85226. Phone (602) 554-2388.

Circle No. 738
Transceiver IC handles both T1 CSU and ISDN primary-rate interfaces

The LXT310 transceiver integrates most of the elements of a T1-rate telephone channel-service unit (CSU) with ISDN primary-rate interface compatibility into one IC. The device allows you to build CSU capability into other customer premise equipment rather than having to add separate units.

The transceiver has separate transmit and receive ports, each capable of either bipolar or unipolar operation. Both ports integrate most of the active components needed for connection to the telephone network, requiring only isolation transformers and impedance-matching resistors to complete the interface. The device complies with relevant industry standards, including ANSI T1.403 and 408, FCC part 68, and AT&T Pub 62411.

The transmit port can drive signals through twisted-pair cable as long as 6000 feet. To handle shorter cables without needing tuned output circuits, the port offers selectable frequency-dependent line build-outs. You can select 7.5, 15, 22.5, or 0 dB of attenuation.

The receive port has a programmable receive equalizer. To increase noise margin in shorter loops, you can limit the maximum equalizer gain to 26 dB; otherwise, you can allow the gain to range to 36 dB. Using a status I/O pin, the receive channel reports on the line insertion loss as indicated by the equalizer gain setting.

The transmit and receive channels both have selectable B8ZS encoder/decoders. In addition, the channels share a low-frequency (3-Hz) jitter-attenuator circuit. You can select which channel uses the attenuator. The attenuator stores incoming data in a FIFO register, then reclocks the data. The output clock adjusts by intervals as small as 1/4 of the clock period.

The transceiver offers several diagnostic features. For example, you can set the transmit section to produce a continuous stream of 1s at the transmit clock frequency to test the cable. You also have a choice of two loopback tests. The local or software methods for controlling the device. The hardware method uses hardwired control pins and coded signals on data pins to select the various operating conditions. If you prefer software control, the device offers a serial communications port for exchanging commands and status information.

The LXT310 operates from a 5V supply and typically consumes 300 mW. It comes in a 28-pin PLCC (plastic leaded chip carrier) and ceramic and plastic 28-pin DIPs. Prices are $30 to $33, respectively (1000).

—Richard A Quinell
Level One Communications Inc, 105 Lake Forest Way, Folsom, CA 95630. (916) 985-3670. FAX (916) 985-3512.

Circle No. 731

EDN December 19, 1991
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CIRCLE NO. 30
Software package lets you postpone selecting of field-programmable parts

Recently released "device-independent" field-programmable gate array (FPGA) tools map your design to any of several specific FPGA architectures, but you still use device-specific place-and-route tools from FPGA vendors to lay out your circuit. FPGA Foundry goes a step further than the recent tools from Data I/O, Exemplar Logic, and Viewlogic Systems because it features place-and-route modules for several FPGA architectures.

The place-and-route modules differ from FPGA-chip-vendor-supplied tools in one key respect: The modules accept timing constraints that enable you to define clock restrictions or path delays. In contrast, vendor-supplied tools are not deterministic; you can place and route 50 iterations and get 50 different layouts—some of which may not meet your timing requirements.

The timing constraints in FPGA Foundry alleviate the necessity of running several place-and-route iterations; the deterministic result will either meet your constraints or fail to complete. (A better implementation would have been to let you choose whether to fail or to complete with warnings.) On failures, you can derate your constraints and try again. One advantage of deterministic software is that it allows incremental modification of the design; small design changes cause small layout changes.

The software provides device-independence by converting your design into low-level-logic intermediate data structures. Although your data is converted, the software still maintains whatever device-specific information you provide as part of the structure. As a result, you can design to a particular FPGA using macrocells and logic geared toward that architecture, yet still experiment with other alternatives.

Similarly, you can use the software to prototype or convert designs between masked semicustom implementations and FPGAs. Create your circuit using your silicon vendor's library, generate an EDIF netlist, map and lay out the netlist in an FPGA, and test the prototype. The final, most important step comes after verifying the function; make sure you check the timing to see that it works.

One hitch in designing a device-independent circuit is that you may use device-dependent functions that may not exist on another device. For example, Actel devices contain on-chip oscillators, Xilinx devices don't. If your design uses an oscillator and you want to place the design in a Xilinx chip, the software won't lay out the circuit.

A timing estimator is part of the software tool kit. This module uses the clock speed and levels of hierarchy to guide the mapping algorithms and place-and-route tools. Tight coupling enables all of these tools to communicate during a run to ensure a placement that meets timing and resource constraints.

An interactive graphic editor offers three modes. The read-only mode lets you view and interrogate the layout. A second mode maintains logic consistency while permitting gate and implementation changes. The third mode is an editor in which you can manually place-and-route the entire design.

The package uses a modular approach that currently includes mapping and place-and-route algorithms for Actel and Xilinx FPGAs. Neocad developed these algorithms.
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CIRCLE NO. 53

UPDATE

without assistance from either company.

Support for devices from other FPGA vendors is under consideration. When available, these algorithms will be delivered as optional modules costing roughly $5000 to $7500 on the PC.

The software currently accepts design data in several formats. EDIF 2.0, LPM (Library of Parameterized Models) standard formats as well as Xilinx- and Actel-specific formats are presently supported. Hooks written into the code will let the tool accept data from CAE- and ASIC-vendor libraries.

Outputs from the software include a cross-reference file, a utilization report, a file containing actual timing delays for back annotation into your simulator, and the output file to program the FPGA. The cross-reference file lets you find buried, replaced, or deleted nodes between schematic and layout. The report generator provides feedback on path and net delays, logic block and I/O utilization, and remaining FPGA resources.

The company is also separately offering its Xilinx place-and-route module. This module does not provide device independence—it only lays out Xilinx FPGAs. The module piggybacks off the Xilinx front-end tools. This software uses the Xilinx intermediate format and, therefore, doesn't support timing. Its cost starts at about $8000.

Written in C++, the software runs under Windows on DOS workstations and on Unix-based workstations running X-Windows and Motif. The company claims the software will be available in January, starting at $18,000.

—Michael C Markowitz

Neocad Inc, 2585 Central Ave, Boulder, CO 80301. Phone (303) 442-9121. FAX (303) 442-9124.

Circle No. 730

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CIRCLE NO. 51

EDN December 19, 1991
Finally, engineering software that clears the way to problem solving without programming.

```c
void service_id(int eid);
{ int stat, byte;
  // serial poll inst
  byte=hpib_spoll(eid);
  if (byte<0) {
    printf("SRQ Prob\n");
    return;
  }
  stat=my_read(eid, DVM);
  if (stat>0) {
    buffy[stat] = '\0';
    printf("Data from instr\n");
  } else printf("I/O read error\n");
  return;
}
main() {
  int busid, stat, MTA, MLA;
  char command[MAXCHARS];
  busid=open("/dev/hpib7", O_RDWR); /* open raw HP-IB for
  MTA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 64;
  MLA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 32;
  stat = BUTTON_BIT;
  sprintf(command, "KM%02o", stat); /* 2 octal digits */
```

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Schematics battle equations for design representation

Debates have raged for years over whether equations or logic schematics are the best design form. Today, that debate is overshadowed by a shift toward synthesis—mapping design representations into silicon.

Ray Weiss, Technical Editor

In the “Good Old Days,” engineers had total control over their designs. Schematics, with gate-level design, ruled. If you drew it, you had it; a gate on a schematic was a gate on the board. Not so today—the designer-to-board connection is not as close, and schematics must compete with equations, as well as truth tables and hardware description languages (HDLs), to represent designs.

Designers no longer have just one universal design representation, but this diversity means they can use the best mechanism for each type of logic. “We use what works. We do PAL [programmable array logic] devices in equations,” says Bob Donaldson, chief engineer at Annapolis Microsystems (Annapolis, MD), “and we use mainly schematics for FPGAs [field-programmable gate arrays]—they let us get close to the configurable-logic-block cell structure for efficient design.” However, opinions of what is best for each type of logic keep shifting.

But more is going on than just a simple competition between schematic-level and equational design methodologies. Engineers are turning to sophisticated tools to optimize and map their designs into silicon. Even with a gate-level schematic, tools may translate and optimize that design into an unrecognizable gate-level implementation.

Design methodologies and tools
are tied closely to the underlying implementation logic. Logic schematics, for example, meshed well with traditional 5400/7400 TTL SSI and MSI ICs. Over the last 30 years, three major logic waves have impacted engineers’ design methods and representation (see box, “Logic waves”).

The shift to equations

Programmable logic is responsible for a large-scale shift in design methodologies from logic schematics to equation-based design. During most of the 1970s and 1980s, programmable logic was largely ignored by mainstream CAE. Today, the majority of board-level designers work with programmable logic.

However, because of its early isolation, programmable logic developed its own brand of representations, including fuse maps and various equational forms. Hardware languages, such as Palasm, Cupl, Abel, and AHDL, evolved during this time for programmable as well as standard logic.

PLDs had fixed logic forms that lent themselves well to easy equational representations. PLAs had a sum-of-products form, with an AND array feeding into a selectable OR array. PAL devices simplified this structure by linking the AND array into a fixed OR array, linking each output to a fixed OR, and having a set number of AND-gate inputs. These PLA and PAL-device structures made it easy for designers to write simple AND/OR equations that mapped directly into the programmable silicon. Not only that, if a design needed changing, designers could simply reprogram a new part, or, with EPLDs, erase the old design and replace it.

PLAs and PAL devices now basically own the board-level design world. “This is the age of PAL-device design,” says Trevor Marshall, president of Yarc Systems Inc (Newbury Park, CA). In achieving dominance, PLDs led design into the world of equations: Most PLD designs are done in equations or a PLD language.

EPLDs and FPGAs have emerged to deal with logic problems beyond the PLD’s grasp. They are large-scale programmable devices with higher pin counts and gate counts than PLDs. Typically, they are built around one or two core logic

You don’t have to use logic schematics or equations to represent logic. Minc’s PLDesigner software lets you use waveforms to represent PLDs. The circuit shown enables a microprocessor to read data from dynamic memory. Inputs appear as (LI) and outputs appear as (O).
FPGAs (field-programmable gate arrays) is that EPLDs use a hierarchical logic structure and fixed routing to combine cells, whereas FPGAs tend to follow the gate-array model, embedding a set of cells in a flat routing structure.

Designing for EPLDs and FPGAs is much more complicated than writing a set of equations for a simpler PLD. Placement and routing become critical for many designs—timing can change drastically depending on placement and signal routing. In general, FPGAs have more flexible routing than PLDs, but they're prone to wider variations in signal delay and skew.

"FPGA-based design is an iterative process," says Billy Beckworth an engineering consultant at Beckworth Enterprises (Mesquite, TX). "I work mainly with schematics. And I do a lot more simulation with them. I try a design and see how well the implementation works and change it as needed." Beckworth works with Actel FPGAs and finds that simulation takes up most of his design cycle.

With EPLDs and FPGAs, designers must map their logic into a collection of cells. This method is somewhat similar to designing with MSI-type logic, but mapping EPLDs and FPGAs into cells only lets designers use one or two MSI functions. However, some EPLD and FPGA cells allow designers to use elements in a cell for different macros or designs. In a Quicklogic (Santa Clara, CA) FPGA, for example, each cell can be treated as three separate elements for design.

Many EPLD and FPGA designers use vendor-supplied macros as design elements. The macros are optimized MSI components made up of cells. These macros serve as logic blocks and lend themselves well to schematic-based design.

ASICs have led large-scale design. But ASIC design levels have been growing slowly. Vendor capabilities have far outstripped mainstream usage. Vendors can deliver usable gate densities of over 200,000 gates. But the typical gate-array design uses far fewer than 20,000 gates.

Many engineers and managers believe the barrier to high-density usage is that few design teams or companies have the capability to define, test, and maintain large-scale gate-level designs. Most ASIC designs have been done the old-fashioned way—with schematics, using primitives and library macro elements.

However, ASIC designers are shifting away from gate-level design and schematics toward higher-level representations. One company shifting its ASIC-design methods is Teradyne Semiconductor Test Division (Agoura Hills, CA), which builds high-performance VLSI testers having hundreds of ASIC chips.

"We're going to VHDL and logic synthesis," says Ben Brown, hardware engineering manager. "We used gate-level design at up to 200 MHz for our J971 tester. We averaged about a man year per ASIC on it. As chip densities go up, we need to up our productivity. HDL-based design offers a way up. There are some things I have some problems with, such as verification at the language level. But we've talked to a lot of users and feel it will work for us."

Almost all the major computer and workstation vendors are working with an HDL and logic synthesis. For example, IBM has designed its mainframes for years using this combination. Similarly, Sun Microsystems uses an HDL for its workstation designs.

HDLs, such as Verilog and VHDL, enable engineers to describe their designs at a behavioral or register-transfer level and to verify the designs through simulation rather than breadboarding. However, until recently the HDL-based design had to be hand translated down to a gate-level design.

Some logic-synthesis tools can overcome that problem. These tools translate the HDL-based design into a silicon implementation. Synthesis tools from Synopsys, Mentor Graphics, Racal Redac, Exemplar, and Viewlogic optimize implementations to meet user-defined speed or area constraints. One of the major benefits to synthesis is a level of independence from the underlying silicon. Engineers can move their designs to different ASIC families, different vendors, or even different silicon technologies.

This new combination of HDLs and synthesis is a major force in the ASIC-design shift from schematic logic to equational forms. Many engineers predict that within five years the bulk of ASIC design for glue and control logic will be in an equational form.

However, all is not perfect yet. Synthesis is still at the logic-chunk level—designers must partition their designs into synthesizable chunks by trial and error. Also, synthesis comes up short in critical areas such as clock distribution and high-speed buffering with latches.

Bucking the trend

Over the last decade, equations have steadily advanced into the schematic world. A key factor has been the engineering shift to equation-based PLD design. Now, however, that invasion shows signs of losing momentum as engineers shift back to schematic based design for the

"Programmable logic is the TTL of the 90s... My advice is to just dive in and start using it."—J Stewart Dunn
**Logic waves**

Design representations (schematics and equations) closely connect to their underlying logic. So as engineers have moved from logic family to logic family, the design representations they’ve used have also shifted. The last 30 years have seen three major waves in mainstream logic design:

- **5400/7400 SSI/MSI (TTL forms)**
- **programmable, packaged logic (PLDs: PLAs and PAL devices)**
- **large-scale logic (EPLDs, FPGAs, and ASICs)**

In the first wave, the logic-design community reached an unparalleled degree of commonality and standards. Designers expressed most logic in standard SSI (small-scale integration) and MSI (medium-scale integration) forms. Engineers could go to any company and be comfortable with their design representations (everybody used the same design templates to draw their logic).

The second logic wave started in the 1970s with the emergence of programmable logic. When traditional schematic forms proved cumbersome, designers shifted to equational representations, which fit the sum-of-products structure of programmable logic. Engineers used simplified hardware languages, such as Abel, Cupl, and Palasm, as well as other forms, such as truth tables and even schematics, to design devices.

The third logic wave has paralleled the first two waves, slowly picking up momentum over time. This third wave, large-scale chip design, includes both ASICs and emerging large programmable logic: EPLDs (erasable programmable logic devices) and FPGAs (field-programmable gate arrays). Larger designs built on more flexible logic components reflect these devices’ greater complexity. Most third-wave design activity is at the schematic logic level; however, ASIC designers, particularly those tackling large designs, are turning to equational forms, using hardware description languages such as VHDL and Verilog.

You can view these three design waves and their underlying silicon as a silicon continuum, ranging from 5400/7400 TTL to gate arrays and standard cells. **Fig A** shows this continuum as one axis, with design mapping as the other axis. At the far extremes—SSI/MSI discretes and high-speed ASICs—most design is at the gate level and has a one-to-one mapping to the raw logic primitives.

However, as design moves from the earlier 5400/7400 components to more modern chips, engineers increasingly rely on design tools to optimize and map their logic into the target circuitry. PLA, PAL-device, and GAL (generic array logic) designers use optimizers and hardware languages. EPLD and FPGA designers rely on optimizers as well as place-and-route tools to map logic to the underlying FPGA cells. And ASIC designers are increasingly turning to synthesis (a software-based logical mapping) and HDLs.
COMPUTER-AIDED ENGINEERING

higher-density EPLDs and FPGAs. EPLD and FPGA vendors provide a path for engineers to stay with schematic-level design using libraries of vendor-supplied macros. Engineers can cobble together their designs using macro building blocks; and they can do so using schematics.

"I use schematic entry for FPGAs," says Highgate's Steve Wasson. "We build our own equivalents to the vendor's macros for efficiency. And we lay out a design in schematics and then tweak it to get high density and efficient routing. Schematics let us see what is happening and serve as a final design medium. We put constraints on the design, such as which pin aligns to what signal. With careful work we can get 75 to 85% gate usage."

"We use equations for PAL devices, and generally schematics for the larger PLDs," says J. Stewart Dunn, vice president of R&D at Datacube (Peabody, MA). "With PAL devices, it was easy to see if a design would fit into a part. With the larger programmable parts, some designs won't fit. And we either redo the design or do hand fitting and routing. In general, equations are much faster—you can change a design in a few hours and have a new part—whereas changing a schematic can take two days. However, for larger PLDs, schematics are the best way now to do design and map into the hardware."

Designers don't have to stay with schematics, they can choose from HDL alternatives. For example, Altera developed its own hardware language, AHDL. The language is basically an extension of the Abellike languages, which feature simple logic equational forms. AHDL, however, supports hardware modules (subdesigns)—designs can be made up of multiple logic modules. Also, Data I/O's Abel now supports a number of EPLDs and FPGAs as well.

The verdict isn't in yet on which design representation is preferable for EPLDs and FPGAs. New tools are emerging that open FPGA de-

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sign to VHDL. Both Mentor and Viewlogic support VHDL representations that can be mapped into FPGAs as well as ASICs. Also, Exemplar Logic Inc (Berkeley, CA) is fielding a VHDL-based synthesis tool for EPLDs (it is the base for Viewlogic's EPLD synthesis). And Synopsys, the pioneering ASIC synthesis company, is now fielding a design compiler for FPGAs that accepts design representations in VHDL or Verilog as well as state tables, equations, or netlists.

Schematics reborn
Schematic capture is becoming more than just an entry tool for logic gates and MSI (medium-scale integration) parts. Instead, schematics are becoming the front end for management of top-down designs. They provide a graphical, hierarchical mechanism to climb down the design tree from a top-level block diagram to detailed logic diagrams and openings to code.

Thus, schematics can serve as the access mechanism for VHDL code as well as for other representations, including truth tables, state-machine diagrams or equations, and waveforms. For example, Mentor Graphics' Design Assistant allows engineers to describe their designs at a block level, with blocks then opening up into VHDL code. Users can define a block, and the system will create a VHDL code stub ready for coding. The schematic interface shows linkage between modules in addition to providing a top-down view.

OrCAD fields a development environment, ESP, that integrates schematic capture, PLD design tools, a simulator, and board-layout packages. You can access PLDs specified in the schematic via the other tools and examine or simulate the underlying source code. Add tionally, the system transforms traditional logic (using special primitives) into PLD equations. The schematic serves as the overall controlling element.

Xilinx's Blox, a new schematic-based FPGA design tool, further encourages using schematics in engineering. Blox enables engineers to work with large parameterized modules. These modules or blocks are chunks of standard logic functions, such as adders, buses, and registers, whose width can be automatically adjusted. You only have to change one parameter on any one of the interconnected blocks to have the design automatically scale to a new size. Blox is an FPGA equivalent to the silicon compiler module generators. It accepts design input from the major schematic entry systems.

No winners
There may be no clear winner in the battle between equations and schematics at all. Instead of a wholesale adoption of hardware description languages or a retreat back to logic schematics, we may end up in a mixed world. Graphics and functional blocks may represent logic subsystems and functions. And those blocks may be in different representational forms, such as truth tables, equations, logic gates, or HDL descriptions for complex control logic.

However, an HDL will probably underlie these representations. And all forms will translate to this HDL for common documentation, simulation, and test.

The future of design holds one sure thing: engineers will be in the same boat as programmers, who live in a world of software mapping. Today, most programmers code in high-level languages, which compile down to executable object code. Similarly, an engineer's designs will pass through a tool-translation layer, which will map them to silicon. Thus, engineers, like programmers, will be increasingly dependent on their tools.

References

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The simulator accepts both C-language user-compiled models and standard Spice models. Among the models included are the Gummel and Poon BJT (bipolar junction transistor) model, five MOSFET models (MOS1, MOS2, MOS3, BSIM1, and BSIM2), a GaAs MESFET model, and standard diode models.

The simulator runs on most workstations and is integrated in the vendor’s Analog Artist design framework. The software costs $30,000 for a single-user license.

Cadence Design Systems Inc, 555 River Oaks Pkwy, San Jose, CA 95134. Phone (408) 943-1234. FAX (408) 943-0513.

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The Design Critiquer compares your design against a set of rules that highlight potential design flaws. Another component of the tool suite is the Parameterized Analog Building Block Generators. The generators use files created by the model builders to generate silicon-level implementations of the functions you need.

Multiplexer cells modeled and characterized for accurate simulation are coupled to each of the analog building blocks. The simulator automatically inserts these blocks into your design, but you have the option of removing any of the multiplexer cells.

The tool suite also includes Mentor Graphics’s schematic-capture software and the Saber/Cadat mixed-signal simulation software. All of the pieces of the tool kit are integrated under an X-Window-compliant graphical user interface. The software is available now; prices start at $75,000.

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Thermal-Analysis Program

Flowtherm is a thermal-analysis CAD program for studying 3-D airflow and heat-transfer in electronic systems. The program accepts data on your hardware design and considers the effects of air viscosity, turbulence, and buoyancy force. The program outputs a picture of the hardware, showing fluid velocities and temperature profiles in all areas of your design. You can apply the program to only a section of pc board or to a complete rack of equipment. The program analyzes natural, forced, or mixed-convecton designs and considers steady-state and transient effects. Version for 386-PC and SPARC-2 workstation, £12,000 and £30,000, respectively. One month trial and two days of tuition, £1100.

Flowmecics Ltd, Kingsgate Business Centre, 12-50 Kingsgate Rd, Kingston-upon-Thames, Surrey KT2 5AA, UK. Phone (81) 547-3373. FAX (81) 547-2682. Circle No. 411

PC-Board CAD Program

Boardmaker-2 is a pc-board CAD program for PCs that accepts netlist inputs, and outputs artwork data in HPLG, or DMPL penplotting language. The program handles through-hole and surface-mount components for as many as ten layers of circuit and silk screen. You can enter a netlist manually, or via a netlist translator, for Mentor, Protel, Racal-Redac, Schema, Tango, and Vutrax formats. The program includes a top-down modification facility for installing modifications to existing designs. Schematic changes automatically modify layout and netlist files and provide automatic time and date stamping. Component renumbering follows through to silk-screen mask, and an update file automatically back-annotates the schematic. A postscript driver lets you import layout files to text processing software, enabling you to generate artwork master drawings on a laser printer or at a typesetting bureau. £295.

Tsien UK Ltd, Cambridge Research Laboratories, 181A Huntingdon Rd, Cambridge CB3 0DJ, UK. Phone (223) 277777. FAX (223) 277747. Circle No. 412

System Simulation Software

Simulab is a simulation and analysis tool for nonlinear dynamic systems. In addition to nonlinear systems, the software also simulates the behavior of linear, continuous, discrete-time, multirate, single-input-single-output, and multivariable input/multivariable output systems. The software models sets of linear and nonlinear differential or difference equations that you can provide as either block-diagram models or in equation form. The software assists in creating block diagrams, and it accepts C, Fortran, or the vendor's own format for the equations. Among the blocks included with the simulator are linear and nonlinear blocks, source and sink blocks, and connection blocks. The tool set allows hierarchical modeling. Analysis tools allow you to solve differential equations, evaluate linear models and determine a system's equilibrium point. The software runs on Apple and IBM PCs and workstations from Apollo, HP, Sun, and DEC. Windows 3.0-based PC version, $3995.

The Mathworks Inc, Cochituate Pl, 24 Prime Park Way, Natick, MA 01760. Phone (508) 653-1415. FAX (508) 653-2997. Circle No. 413
PC-Board Software
ALS-View III Version 6 is a multi-layer pc-board software tool for viewing and editing pc-board layouts. The software, which runs on personal computers with 2 Mbytes of RAM, offers a Motif-like user interface. The software allows viewing and editing of as many as 128 layers; you can edit by window or layer. Resolution of the layers is to one mil. The software generates printer outputs for Postscript and Dot Matrix printers. You can use the software to generate drill files; it also merges multiple Gerber files on a single film. Software, $795; Gerber design-rule-checker option, $495.

ALS Design Corp, 1 Kendall Sq, Suite 2200, Cambridge, MA 02139. Phone (617) 621-7109. FAX (617) 577-1209. Circle No. 414

Fault Simulator
Unlike concurrent fault simulators that simultaneously simulate a good circuit and its evil twin, Adas Fault Simulator uses a differential algorithm that simulates a good circuit and a faulty circuit sequentially. The differential fault simulator only records and tracks the difference between the good and faulty circuits at latches and flip-flops. As a result, the simulator has lower memory requirements than concurrent fault simulators. The algorithm in the difference fault simulator includes dynamic fault grouping to simulate multiple faulted circuits simultaneously. Intelligent fault injection speeds runtimes and reduces the risk of eventless simulation. The software runs on SPARCstations. From $25,000.

Adas Software Inc, 3333 Bowers Ave, Suite 295, Santa Clara, CA 95054. Phone (408) 988-3846. FAX (408) 988-2483. Circle No. 415

Simulation Comparison Program
VCAP is a simulation data comparison-and-analysis program. The software allows you to normalize data to adjust for differences in format, timing, and display modes. The normalization routines include state mapping, timing translation between print-on-change data and cycle data, and data separation on bidirectional pins. The software's analysis routines include reports on output-pin delays and transitions, input-pin timing, and a resource file that checks tester compatibility. You specify which data pins to compare, the allowable timing tolerance, times to mask the comparison, and four comparison algorithms. The software runs on Sun and HP/Apollo workstations. Single user, $3995; server node configuration, $7995.

Source III Inc, 3958 Cambridge Rd, Suite 247, Cameron Park, CA 95682. Phone (916) 676-9329. Circle No. 416

Manufacturability Tool
The Manufacturing Advisor/PCB tool provides information on product cost, quality, and delivery for the analysis of pc-board design alternatives. Built upon the vendor's Falcon Framework, the software evaluates parts lists, board-area consumption, and other considerations that might impact product manufacture. The software monitors and identifies unusual labor requirements, special manufacturing processes, lack of standards compliance, and other issues that lead to high-risk assembly. The software includes a component library containing 800 package styles. Currently available on HP/Apollo workstations, the company plans to run it on Sun and HP Series 700 workstations early in 1992. Software, $16,900 option to Idea Station and Board Station. Additional parts library, $1500.

Mentor Graphics Corp, 8005 SW Boeckman Rd, Wilsonville, OR 97070. Phone (503) 685-7000. Circle No. 417

PC-Board Software
PADS-2000/UX is a design tool for pc-board design. The software includes a push-and-shove auto-router. The design tool offers automatic component placement and rotation of pads and components in 1/10° increments. A 1-µm database provides high resolution and a capability of spacing traces and components closely. The software also features an automatic copper-fill facility. Available on SPARC-stations under OpenLook/X Window. $19,995.

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VHDL Tools
The V-System/SPARC VHDL (VHSIC Hardware Description Language) development and simulation suite works on SPARCstations running Sun OS and Open Windows. The system, which handles designs of 100,000 lines of code, includes a VHDL compiler, an interactive VHDL simulator, and a source-level debugger. The system provides six windows that allow you to view and interrogate the design, display variables and signals, control the simulator, display processes, and list the simulation output. The debugger provides features such as breakpoints, reading and setting signal and variable values, and single-stepping through the source. The software supports the IEEE 1076 standard. The vendor claims initial compilation benchmark results of 15,000 lines per minute and simulation rates of 10,000 RTL statements per second on a Sun IPC. Single-user license, which requires a 15% annual maintenance fee, $4995.

Model Technology Inc, 15455 NW Greenbrier Pkwy, Suite 210, Beaverton, OR 97006. Phone (503) 690-6838. Circle No. 419

Spice Enhancement
The Profile front-end tool works with the Analog Workbench II Spice-based simulation tool. The front-end tool enables both graphi-cal and textual entry of structural- and behavioral-level circuit descriptions. You can build circuit models from block diagrams that include such components as PLLs, differentiators, oscillators, and gain blocks. Although this software also accepts standard Spice netlists, it also permits behavioral-level models containing differential equations, Laplace transforms, and basic arithmetic. The software allows distributed processing of multiple tasks across a network; such tasks don't include simple dc and transient analysis but include statistical and parametric simulation. The software incorporates modeling extensions to Spice to enable such effects as hysteresis, memory, and conditional branching. The models also let you eliminate discontinuities in nonlinear models using piecewise-linear functions. An option to the company’s $12,000 Analog Workbench II simulation and analy-
Computer-Aided Engineering

sis tools, Profile runs on Sun, DEC, and IBM workstations. $15,000.
Valid, 2820 Orchard Pkwy, San Jose, CA 95134. Phone (408) 432-9400.
Circle No. 420

DSP Simulation Software
Hypersignal-Windows Block Diagram software allows you to design and sequence process blocks for DSP applications. Among the functions included with the software are blocks for FFTs, FIR and IIR filters, linear predictive coding, IFFT (inverse FFT), and difference equations. In addition to these blocks, you can create your own. Each block is of the input, output, process, or display type. After stringing each of the blocks together, you can apply a stimulus and simulate the response. You can measure the response using display blocks at your choice of probe points. The software runs on personal computers under Windows. From $1995.
Hyperception Inc, 9550 Skillman, LB 125, Dallas, TX 75243. Phone (214) 343-8525.
Circle No. 421

PC-Board Design Tool
Eagle is a modular PC-based circuit-board design tool that includes a schematics editor, an autorouter, and a layout editor. The tool databases are shared, thereby calling components into the layout editor as you use them in creating your schematic. Alternatively, you can use a utility to convert netlists generated by several other schematic packages into the proper layout database. The software, which runs on PCs, uses expanded memory for large designs. An Electric Rules Checker evaluates the design for shorts, overlapping signals, and continuity. A Design Rules Checker compares trace spacing, wires not in a 45° raster, off-grid objects, and minimum and maximum sizes against user-defined criteria. The autorouter routes two signal layers and unlimited supply layers. Schematic editor, $899; layout editor, $399; autorouter, $699; total system, $1199.

Cadsoft Computer GmbH, Rosenweg 42, W-8261 Pleiskirchen, Germany. Phone 8635-810. FAX 8635-920. Circle No. 423

the JTAG/IEEE 1149.1 testability standard? Let us count the ways.

Texas Instruments was the first electronics company to develop products for implementing the JTAG/IEEE 1149.1 testability standard. Here’s the latest of a fast-growing list of TI products compatible with the 1149.1 standard.

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2. Advanced BiCMOS (ABT) Octals (8)
3. Advanced BiCMOS (ABT) Widebus™ (7)

Support Devices
4. Test Bus Controller
5. Digital Bus Monitor
6. Scan Path Linker
7. Scan Path Selector

Application-Specific Memory
8. Diary
9. TMS320C40
10. TMS320C50
11. TMS320C51

Floating-Point Processor
12. TMS34082

Futurebus+
13. Protocol I/O Controller
14. Arbitration Controller
15. Programmable Arbitrer
16. Data Path Unit
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If you would like to know more about JTAG/IEEE 1149.1 and how it’s being supported by Texas Instruments, please request a copy of our “Testability Q&A Update.”

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<table>
<thead>
<tr>
<th>RFA120 FET Array</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Range: ±5V to ±15V</td>
</tr>
<tr>
<td>Input Offset Voltage: 5 mV typ.</td>
</tr>
<tr>
<td>Input Bias Current: 30 pA typ.</td>
</tr>
<tr>
<td>Gain Bandwidth Product: 3.0 MHz typ.</td>
</tr>
<tr>
<td>Slew Rate (Gain = 1): 8 V/µs</td>
</tr>
</tbody>
</table>

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The requirement for only 2 and 20V dc and 20-kΩ and 1-MΩ standard sources to calibrate Keithley's model 2001 exemplifies the trend toward easier user calibration.

Brian Kerridge, Technical Editor

THE TREND TO SIMPLER methods of maintaining the accuracy of instruments stems from a natural desire to reduce the inconvenience and expense of calibration. Examples of easier ways to calibrate instruments appear on several high-end DMMs. These instruments have many functions and ranges that require regular calibration, and traditionally the cost of ownership is high. Two new methods, “artifact” and “self calibration,” imply you can enjoy substantial cuts in these support costs.

But take care. You might delight in the prospect of lower support costs and more convenience, but calibration diehards frown upon using these methods alone. They argue that traditional methods already represent a minimum procedure for achieving satisfactory calibration. Their argument maintains that the new methods break the all-important traceability chain and are incompatible with established company audit procedures and MIL-STD-45662A (Ref 1).

Artifact calibration is similar to the normal procedure for calibrating an instrument, during which you use external standards to check and adjust key points of a DMM’s performance. The difference with artifact calibration is that the num-

DMM calibration shortcuts pose question of confidence

Simpler methods of calibrating 7.5- and 8.5-digit digital multimeters let you adjust the overall accuracy of an instrument using as few as two external standards—or no standards at all. The methods are innovative but depart from principles the calibration community has cast in stone.
ber of key points you need to check reduces from about 80 to just 2. Consequently, a calibration laboratory needs only two prime standards (the artifacts), instead of a full-compass calibrator, to perform a complete calibration. In practice, the artifacts needed are a 10V dc standard source and one or two resistance standards.

The other new method of calibrating, self-calibration, requires no external equipment at all. DMMs with this facility use standard sources housed within the instrument. At any time you can initiate a self-calibration routine from the instrument’s front panel, and a 10-minute cycle of internal adjustments resets the accuracy on all the unit’s functions and ranges. Of course, the DMM’s internal standards require calibrating at some time, otherwise there would be a complete loss of traceability. Vendors present self calibration primarily as a means of enhancing a DMM’s accuracy and not as a replacement for conventional calibration—an acknowledgment that this method has traceability deficiencies.

Convenience vs confidence

It’s easy to see why both artifact and self calibration offend calibration diehards. The trend among DMM vendors is to reduce most of the cross referencing carried out between external standards and instruments during calibration. DMMs, particularly high-end models, generally find application in critical measurement situations. For example, high-end DMMs are often deployed in ATE systems to provide traceable accuracy for the whole system. Elsewhere, you will find high-end DMMs heading up a company’s in-house system for auditing the accuracy of many other instruments in the plant. In applications such as these, it’s natural to imagine the need for more, rather than fewer, checks in a calibration procedure.

There is no doubt that the easier methods of adjusting accuracy work effectively and are convenient. There’s also no doubt that reconciling these methods with traditional procedures is awkward. The most obvious weakness of the new methods is that they leave you with very little indication that the instrument has in fact been adjusted. It’s this lack of hard records that causes doubts over the traceability of the techniques. If you follow the shortcut methods with a full calibration check, then traceability worries disappear. But you’ll need a full set of calibration sources for that check, which devalues the convenience of the new techniques.

In the short term, it’s unlikely that calibration methods such as artifact and self calibration will ease your calibration costs. In the long term, as the virtue of using the techniques alone becomes evident, you may find it acceptable to extend the regular interval for a full calibration. In the end, your confidence will be the deciding factor.

Laurie Cronin, principal officer

A self-calibrating DMM requires no external standards and offers the easiest way to improve instrument accuracy. For Datron’s model 1281, self calibration provides approximately a 2:1 improvement in both overall long-term accuracy and the effective temperature coefficient over the 15 to 35°C ambient range.
and specialist in dc and low-frequency metrology with the National Physical Laboratory at Teddington, UK, offers advice to reconcile opposing views of artifact and self-calibration. He says if you calibrate an instrument using any new technique, you should still check the instrument’s performance on all its functions and ranges via a full conventional calibration. You should adopt this procedure each time you calibrate the instrument over the first few calibration intervals. As you build up confidence in artifact and self-calibration, you can consider extending the interval between full calibrations.

As an example, you could choose to carry out artifact calibration every 12 months and conduct a full calibration at 24-month intervals.

Simpler methods for adjusting the accuracy of DMMs offer the possibility of extending the period between full calibrations.

Cronin emphasizes that extending the calibration interval is not a recommendation and should be done only when there is evidence to support the change. In his experience, users that have artifact- or self-calibration DMMs have all chosen to check performance fully each time they calibrate the instrument. Cronin suggests that as an overall policy you should treat each instrument on its merits, irrespective of the technique used for adjusting its accuracy.

Table 1 shows which calibration methods today’s 7.5- and 8.5-digit DMMs employ. Artifact calibration appears only on Hewlett-Packard’s 3458A and Keithley’s 2001. HP’s model 3458A needs two standard sources—10V dc and 10 kΩ. For Keithley’s model 2001, you need 2 and 20V dc sources and 20-kΩ and 1-MΩ resistance standards. For both instruments you also need a low-thermal shorting link.

The 3458A also includes a means of self calibration, which the company calls auto calibration, or Acal. Self calibration, or Selfcal, is also a feature of Datron’s model 1271 and 1281 DMMs. Datron’s models also provide a means of conventional calibration against a full set of external standards for those who are not believers in calibration short-

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### Common DMM and calibration terms

**Absolute accuracy**—an accuracy figure that includes all sources of measurement uncertainty. Some standards laboratories calculate this figure as the arithmetic sum of all uncertainty elements. Other laboratories calculate it as the square root of the sum of the squares of the uncertainty contributions to a declared confidence level.

**Accuracy relative to calibration standards**—an accuracy figure that includes only the uncertainty elements contained within an instrument and excludes the uncertainty of the calibration source.

**Artifact calibration**—a calibration method that uses a minimum number of standard calibration sources. The sources for a DMM typically include a 10V dc standard and a standard resistance.

**Calibration**—comparing an instrument of unknown accuracy to a standard of known accuracy, the purpose being to record or adjust the difference.

**Calibration interval**—the period of time over which an instrument maintains its specification without adjustment or verification. Typical calibration intervals for DMMs are 90 days and 12 months.

**Calibration uncertainty**—the arithmetic or statistical total of all uncertainty contributions for a calibration standard.

**Full scale**—the maximum number of counts on a scale; for example, 19,999,999.

**Full range**—the number of counts at the cardinal point on a scale; for example, 10,000,000.

**Linearity error**—the maximum deviation from a straight line between zero and full scale.

**Low-thermal short**—a link used as a zero reference for short circuiting an instrument’s input terminals and producing a minimal thermal EMF.

**National standard**—a standard maintained at a National Standards Laboratory, such as the National Institute of Standards and Technology in Washington, DC.

**Reference standard**—the best, or prime, standard of a hierarchy of standards in a calibration laboratory.

**Traceability**—an unbroken chain of calibration records going back to a national standard.

**Transfer standard**—a standard having no absolute accuracy but having sufficient stability and resolution to allow comparison of two similar devices.

**Working standard**—a standard used for general calibration. Working standards are regularly compared to a reference standard.

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**Acknowledgment**

Thanks go to Peter Crisp, head of standards at Datron Instruments, for helping with this glossary.
In a conventional calibration procedure, you connect 80 inputs in turn to the DMM. At each setting, you initiate a trigger to update a corresponding parameter in the DMM’s calibration memory. This method clearly provides a high degree of confidence that you’ve calibrated most aspects of the DMM’s performance. The drawback is the extensive range of standard sources required to effect the calibration—a single-instrument calibrator to do this job costs approximately $35,000.

Although most DMMs provide a front-panel key to initiate the trigger, usually vendors and calibration laboratories calibrate DMMs remotely using an IEEE-488 system controller and a programmable calibrator. Even so, such an automatic routine could take two hours to calibrate a high-end DMM fully.

Although artifact calibration requires only two or three external standards, the 80 or so accuracy-correction parameters in the instrument still need updating during the process. Clearly, something smart needs to happen inside the instrument to translate two dc and resistance inputs to signals capable of adjusting the overall accuracy of the unit. The overall accuracy adjustment points appear not only on all the dc and resistance ranges of the unit but also on all current and ac voltage ranges.

On Keithley’s 2001 DMM, you use 2 and 20 V dc sources and 20-kΩ and 1-MΩ resistances to calibrate ranges for those inputs directly. To calibrate other dc and resistance ranges, the DMM internally switches its internal gain-defining components to scale up or down from the same standard inputs. When you calibrate the resistance function, you in fact calibrate the currents the unit sources when operating in its normal mode as a resistance meter. The DMM uses these same currents to calibrate its operating current-function ranges.

For ac ranges, the 2001 DMM uses the dc source to calibrate the low-frequency end of the band while

cuts. To add confusion, though, Datron uses the term auto calibration, or Autocal, to describe the company’s conventional method of calibrating the DMMs.

All other high-end-DMM vendors stick rigidly to tradition with their models and provide only a conventional way of calibrating.

Eighty points need adjustment

Table 2 summarizes the merits of the three calibration methods you will find on high-end DMMs. Note that for the majority of DMMs, including even some 4.5-digit handheld units, accuracy control relies solely on correction parameters stored digitally in nonvolatile RAM inside the DMM. It’s partly the function of calibration to adjust these parameters to make the instrument produce accurate readings.

Normally, there is a correction parameter for every function and range combination on a DMM. Some ranges require more than one parameter. For example, the dc function has parameters for zero and both polarities of input, and the ac function has parameters for the low- and high-frequency ends of the band. In total, there could be 80 correction parameters.
Artifact calibration lets you adjust the accuracy of a digital multimeter using one voltage and one resistance standard.

Sanit in a dc-coupled mode. For the high-frequency end, the DMM requires no source at all. The DMM's internal reference voltage generates a step input to each ac range in turn. On each range the DMM stores two samples of the transient response of the input circuits. The magnitude of the samples, in turn, determines the setting of a flatness-compensation amplifier in the ac-measurement signal path.

But there are factors that influence accuracy that artifact calibration doesn't compensate for. These factors include linearity of the main ADC, ac/dc difference in the ac-detection circuit, and self heating on high-voltage and high-current inputs. John Banaska, 2001 project manager at Keithley, explains that you can look at these factors as characterization factors for an individual DMM. He says characterization factors are stable over the life of the product and any change has minimal effect on overall accuracy.

Keithley cancels the effects of these characterization factors at the manufacture stage using an in-house calibration routine. This once-in-a-lifetime routine should need repeating only if the instrument receives a major repair. Banaska says routine user calibration compensates for drifts in the DMM's reference and gain-defining components and that these drifts are the predominant reasons for accuracy drift in a DMM.

In answer to the suggestion that artifact calibration is weak on traceability, Banaska explains that you can output all the accuracy parameters stored in the 2001 DMM. These figures provide a basis for maintaining full records of the stability of the instrument.

A tradeoff of artifact calibration is your loss of flexibility to adjust one area of the instrument's performance or to improve on the published specifications of the product. Conventional calibration lets you optimize one specific range and always make the instrument read nominal value. Artifact calibration gives you no way to do this fine tuning. When the artifact-calibration routine is over, all readings will be within published limits, but not necessarily reset to the center point of the accuracy spread.

Datron's 1271 and 1281 DMMs embody a limited set of calibration sources to let you improve the accuracy of the unit without any external standards. These models also let you perform a conventional external calibration; during that process, the calibration of the internal sources takes place transparently.

Fig 1 shows the salient features of the arrangement. In Datron's instruments, three separate blocks of nonvolatile RAM store different sets of accuracy parameters. The first block sets the accuracy of the DMM following a conventional external calibration. The second block stores parameters relating to the internal calibration sources. The third block sets the DMM's accuracy each time you conduct an internal calibration.

The internal dc voltage sources

Datron's self-calibrating DMMs hold accuracy-correction parameters in three blocks of nonvolatile RAM. The first block sets the accuracy of the DMM following a conventional external calibration. The second block contains parameters relative to the accuracy of internal calibration sources. The third block sets the DMM's accuracy following an internal calibration. In normal operation, the DMM can measure inputs using parameters in blocks one or three.
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and 100 kΩ. A critical feature of the dc sources is their use of a trans­
former multiplier’s fixed turns ratio to determine the 10:1 and 100:1 ra­
tio of the voltages.

The internal process of self cali­
bration follows a path similar to
that of artifact calibration. First, in­
ternal dc sources calibrate the dc
and ac functions; next, the internal
resistance sources calibrate the
drive current on the resistance
function; and last, these drive cur­
rents calibrate the DMM’s current
function.

The real benefit of self calibration
is the cancellation of drift effects in
gain-defining components of the
DMM’s measurement circuits.
These drifts occur when you oper­
ate the DMM at varying ambient
temperatures or as the values of the
components change with time. Self
calibration does not cancel the ef­
fect of drift in the DMM’s main in­
ternal reference.

Not all models make use of self
calibration in the same way. On
Datron’s 1281 model, you use self
calibration as a means of enhancing
the specified accuracy when you de­
cide you need enhanced accuracy.
On other models, you must operate
self calibration at regular intervals
to guarantee that the instrument
meets its accuracy specification.
For Datron’s 1271 and Hewlett­
Packard’s 3458A, these mandatory
self-calibration intervals are 30 days
and 1 day, respectively.

Reference

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The package's user interface includes computer simulations of the front panels of common instruments. Instruments simulated include classic and modern oscilloscopes, a digital recorder, a spectrum analyzer, and a function generator.

The package includes a block-diagram facility with which you can simulate complex DSP algorithms by linking elements from a library of modular DSP functions. Other software functions include graphical analysis and code generation.

Prices range from $1995 to $7995, depending on the bandwidth and resolution of the hardware and the DSP routines you select.

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Circle No. 686

Data-acquisition and -analysis package simulates multiple instruments

Snap-Master for Windows, an icon-based data-acquisition, -analysis, and -display software package, allows you to define custom test instruments. Running on a PC equipped with an A/D card, the software simulates instruments such as a data-acquisition system, digital storage oscilloscope, strip-chart recorder, spectrum analyzer, waveform analyzer, or multimeter. You can also combine simulations of these instruments.

The software’s maximum data-handling rate is 400 ksamples/sec. The software can control sensors, transducers, actuators, and signal conditioners. You can input data from either plug-in A/D cards or A/D cards in separate enclosures as well as IEEE-488 and RS-232C instruments, all from a variety of manufacturers.

To create a custom instrument, you define the flow of data through the virtual test system with a flowchart. You use pipes to connect graphical icons representing each test-instrument element.

Minimal hardware is a 386 or 486 PC with 2 Mbytes of memory (4 Mbytes recommended) and Windows 3.0. The Snap-Master software package costs $995.

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Tel. 617-270-0360
Fax 617-273-2892

**Dallas**
2454 Trade Mart
Dallas, TX 75207
Tel. 214-742-9389
Fax 214-742-9389

**Europe**
Frankfurter Strasse 97-99
6096 Raunheim
F.R. Germany
Tel. 06142-43095/96/97
Fax 06142-22799

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Introducing the biggest thing in slides since ball bearings.

No pinched fingers. Just smooth slide action.
The new Green Button™ release. Only from General Devices.

Stop damaged digits by specifying Chassis Trak® slides with the new Green Button release.
Safe, simple and superior to its spring-clip counterparts, Green Button is standard on our most popular ball bearing slide models. A feature available at no additional cost to you.

Be part of the push. Push these buttons now: 1-800-626-9484.
We'll rush you a copy of our new ball bearing slide catalog and all the info on Green Button...the biggest thing in slides since ball bearings.

General Devices Company, Inc.  P.O. Box 39100, 1410 S. Post Rd., Indianapolis, IN 46239-0100
Heard the news about Keithley's new switching system?

It's on all 80 channels.

Introducing the Keithley Model 7001 High-Density Switching System.

Now, get up to 80 channels of two-wire switching from just one half-rack mainframe and two high-density cards.

Monitor all channels at once, too. The unique vacuum fluorescent display shows the open/close status of all channels simultaneously. Program, modify, or debug your test systems with remarkable ease.

Plus, have the capability to switch a variety of signals. From femtoamps to amps. Nanovolts to kilovolts. And DC to 500MHz. It's the kind of measurement integrity that has made Keithley switches a preferred choice for nearly two decades.

Call 1-800-348-3735. Or return the card. An applications engineer will provide details, arrange a demonstration, even help you design your test system.

Contact Keithley today. We'll be watching for your reply.
6.5-Digit Digital Multimeter
The SI 7063 is a 6.5-digit DMM for measuring dc and ac voltage in the range 100 nV to 1050V, and dc and ac current in the range 1 nA to 2A. The meter also measures resistance from 100 µΩ to 999 MΩ; it measures temperature using a platinum-resistance thermometer, or J, K, R, T type thermocouple sensors. The meter has counter and timer functions to let you measure 1 Hz to 1 MHz, and 1 µsec to 1 sec for analog signals; and measure to 20 MHz and to 100 nsec for TTL signals. IEEE-488 interface programming includes an on-line help facility to provide correct syntax commands. £1810.

Schlumberger Technologies, ATE Systems Div, Victoria Rd, Farnborough GU14 7PW, UK. Phone (252) 544433. FAX (252) 543854. Circle No. 370

Handheld Oscilloscopes
The models 93, 95, and 97 Scopes combine a 50-MHz, 25-Msample/sec, dual-channel storage oscilloscope and an autoranging digital multimeter. The model 97 also includes a signal generator and component tester. The units have an RS-232C interface for calibration. The scopes capture glitches as narrow at 40 nsec and can store eight waveforms and 10 front-panel setups. Metering capabilities include simultaneous display of minimum and maximum readings, relative and percent-relative readings, and dB readings. The units have soft keys and weigh 4 lbs. Batteries power the units. Model 93, $1195; model 95, $1495; model 97, $1795.

John Fluke Mfg Co Inc, Box 9090, Everett, WA 98206. Phone (206) 577-1101. FAX (201) 356-6100. TLX 185102. Circle No. 371

68302 µP Emulator
The Mime-700 in-circuit emulator works with the 68302 microcontroller (μC). You can connect the emulator to the Integrated Services Digital Network as a terminal controller, multiplexer, or concentrator. The 68302 personality module (pod), tracks the μC's pipelined execution to halt when the emulated μC actually executes an instruction, not when the μC first fetches the instruction.

The emulator has 256 kbytes (2 Mbytes max) of emulator memory that you can allocate in 512-byte blocks. The emulator’s trace and trap circuitry features 64k discrete breakpoints as well as 64k breakpoints for 512-byte blocks of memory. The circuitry also has four 80-bit word recognizers, each with its own pass counter. The unit has an 8-ksample x 128-bit trace memory, as well as a digital-waveform generator, a frequency meter, and a digital voltmeter. Emulator with 68302 pod, $14,159.

Pentica Systems Inc, 1 Kendall Square, Bldg 200, Cambridge, MA 02139. Phone (617) 577-1101. FAX (617) 494-9262. Circle No. 372

VXI Chassis
The HP 307X VXI board tester combines a VXIbus chassis with the manufacturer’s existing board tester. You can mount the VXIbus chassis externally or on the tester’s testhead. The VXIbus chassis provides connections to VXIbus and IEEE-488 instruments. The chassis accepts C-sized VXIbus cards. $821,500.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. Circle No. 373

Low-Noise Synthesizer
The PTS 310 broadband signal source covers 0.1 to 310 MHz with a 1-Hz resolution (0.1 Hz optional). Spurious suppression specifies 60 or 65 dB. The instrument offers switching times of 20 µsec or 1 µsec to 20 µsec, depending on band selected. Frequency switching is phase continuous. You have a choice of BCD or IEEE-488 interfaces. PTS 310, approximately $6000. Delivery, six weeks ARO.

Programmed Test Sources Inc, Box 517, Littleton, MA 01460. Phone (508) 486-3008. FAX (508) 486-4495. Circle No. 374
Logic Analyzers

The TA4000 series of logic analyzers includes models with 32, 48, or 80 channels. Asynchronous sampling is at 100 MHz max across all channels or at 400 MHz max across 8 or 16 channels. Memory depth at 100- and 400-MHz sampling is 2k and 8k words, respectively. Its 5-nsec glitch capture operates on eight channels without loss of memory depth.

Synchronous sampling is at 50 MHz max across all channels and includes an 8-level branching-trigger facility that steps as much as 20 nsec. Optional disassemblers cover a range of 8-, 16-, and 32-bit µPs. In addition to internal nonvolatile memory, you can store 512 kbytes of data on a front-panel plug-in memory card. Included as standard are interfaces for IEEE-488, Centronics, RS-232C, and composite video. TA4000-32, £2495; TA4000-48, £2995; TA4000-80, £3995.

Thurlby-Thandar Ltd, Glebe Rd, Huntingdon, Cambs PE18 7DX, UK. Phone (480) 412451. FAX (480) 450409. Circle No. 375

DSP Board

The MacDSP MB/A digital-signal-processing pc board for Macintosh computers runs at 30 Mflops. The board includes a DSP32C DSP µP, a 68000 µP, and data-acquisition modules. The board's two processors run under Apple's A/Ros out of onboard memory. The onboard RAM maps directly into the Mac's Nubus memory space. Board, $3495; expanded-memory version, $4995; data-acquisition daughter boards, $595; C compiler, $1500; array-processor library, $495; signal-analysis package, $495.

Spectral Innovations Inc, 4633 Old Ironsides Dr, Suite 401, Santa Clara, CA 95054. Phone (408) 727-1314. FAX (408) 727-1423. Circle No. 376

Gang Programmer

The MultiTrk-4000 gang programmer programs as many as 32 devices at once using four 8-device plug-ins. It can also impress sequential serial numbers on as many as 32 devices simultaneously. Plug-ins are available for DIPs, plastic
leaded chip carriers, and pin-grid arrays. You can program copies of a single ROM or sets of ROMs for 8-, 16-, and 32-bit-wide designs. The unit handles certain microcontrollers and CMOS PLDs. Other features include a keypad, an LCD, RS-232C and parallel interfaces, and a 3½-in. disk drive. The onboard memory has 256 kbytes, expandable to 16 Mbytes. $4995. Delivery, four to six weeks ARO.

**Bytek, 543 NW 77th St, Boca Raton, FL 33487. Phone (407) 994-3520. Circle No. 377**

**Wooden And Nylon Probers**

This line of wood and nylon probers is safe for use around ESD-sensitive components. The hygroscopic properties of these probing tools mean that they will readily take up and retain static-dissipating moisture from the atmosphere or skin. The probers will not mar or nick component leads. The birchwood spudgers will not melt when holding wires near soldering irons. $0.22 to $1.56.

**Desco Industries Inc, 761 Penarth Ave, Walnut, CA 91789. Phone (714) 598-2753. Circle No. 378**

**PC-Programmable Power Supply**

The model ATEPS-1606 triple-output, programmable power supply plugs into a PC's backplane. It features a single 0 to 6V, 0 to 2A output, and two independent bipolar outputs. The bipolar outputs range from -15.75V to +15.75V at 0 to 200 mA each. Outputs of 0 to 28V and 0 to 125 mA are alternately available. You can vary all outputs in real time and monitor the supply's outputs via an onboard 12-bit A/D converter. You control and monitor the outputs using onboard control registers. The board comes with software. Model ATEPS-16, $995.

**Analyx Systems Inc, Box 14644, Fremont, CA 94539. Phone (415) 656-8017. FAX (415) 657-0927. Circle No. 379**
Integrated schematic and PCB software that was designed that way, not kludged that way.

- Imagine using the same drawing tools for both schematic drawings and PCB artwork.
- Picture the convenience of displaying and editing schematic and PCB drawings simultaneously.
- Visualize being able to create or modify library symbols in seconds using the same commands you use for other drawings.
- Envision a 100% completion rip-up-and-re-route autorouter that costs thousands less than comparable autorouters.
- Suppose you could unleash all this power by spending less than eight hours with the tutorial.
- Now fancy a toll-free number provided for no-charge technical support, and a 30-day, no-hassle, money-back guarantee.

300-MHz Digital Oscilloscopes

The 2-channel model 9310L and the 4-channel model 9314L digital oscilloscopes have 300-MHz analog bandwidth, independent 100-Msample/sec digitizers on all inputs, and 1-Msample/channel memories. You can segment the sample memories for storing multiple events. Trigger events include pass/fail testing, glitches, and windows. The scopes perform signal-processing functions including FFTs. The scopes use credit-card-sized memories for offline storage. Model 9310L, $9900; model 9314L, $14,900. Delivery, six weeks ARO.

LeCroy Corp, 700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977. Phone (800) 553-2769; (914) 425-2000. Circle No. 380

3-GHz Oscilloscope Plug-ins

The model 11A81 3-GHz plug-in for the company’s models 11403A and CSA 404 digitizing scopes has a rise time of ≤130 psec. The plug-in’s external-trigger input’s bandwidth is 2 GHz. Input sensitivity ranges from 10 mV/div to 1V/div in 1-2-5 sequence. Offset range is ±50 divisions. The unit is programmable. Model 11A81, $5495. Delivery, four to six weeks ARO.

Tektronix, Box 19638, Portland, OR 97219. Phone (800) 426-2200; (503) 627-7111. Circle No. 381

68HC16 Emulator

The HMI-200 in-circuit emulator supports the 68HC16 DSP µP. The emulator runs in real time. It has four complex hardware breakpoints and two 4-ksample × 104-bit trace buffers. The unit comes with 256 kbytes of emulation memory. Emulator and software, $16,000; software-performance-analysis unit, $2500; software for Sun or Apollo workstations, $1000.

Huntsville Microsystems Inc, 3322 S Memorial Pkwy, Huntsville, AL 35801. Phone (205) 881-6005. FAX (205) 882-6701. TWX 510-600-8258. Circle No. 383
KEPCO TRIPLE OUTPUT,
LOW PROFILE, OEM a-c TO d-c
SWITCHING MODULES
SERIES MRW/35 AND 50 WATTS

Model MRW 150KV
Model MRW 151KV
35 Watts

Model MRW 160KV
Model MRW 161KV
50 Watts
FEATURES:
- **115/230V a-c operation without user intervention:** Special flyback circuit accepts any input voltage from 90V to 264V a-c.
- **Power-OK logic (TTL compatible) signal** may be used as power fail signal. Logic “1” is given when +5 output is above 4.5V.
- **Current trade-off:** Current may be increased from one of the outputs at the expense of the others, within the limits defined by Figure 1.
- **Adjustable voltage:** Internal trimmer accessible through the case allows manual adjustment of the voltage setting.
- **Overvoltage protection for principal output** shuts down all outputs if output voltage is forced beyond the set limit.
- **Holding time:** Output is sustained by internally stored energy for 30 milliseconds typically, 20 milliseconds minimum.
- **Built-in EMI filter** attenuates conducted noise below the requirements of FCC 20780 for Class B computing devices.
- **Safety:** All models recognized by UL, certified by CSA, and approved by TÜV Rheinland to meet VDE 0806/IEC 380.

### MRW INPUT CHARACTERISTICS

<table>
<thead>
<tr>
<th>SPECIFICATION</th>
<th>MRW 150KV</th>
<th>MRW 151KV</th>
<th>MRW 160KV</th>
<th>MRW 161KV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage range</td>
<td>90 to 264V a-c; 130 to 370V d-c</td>
<td>Maximum load</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Brownout voltage</td>
<td>85V a-c; 120V d-c</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>1.0A</td>
<td>1.3A</td>
<td>Typ load, 115V a-c</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.5A</td>
<td>0.8A</td>
<td>Typ load, 230V a-c</td>
<td></td>
</tr>
<tr>
<td>Fuse value</td>
<td>2.5A</td>
<td>3A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Initial, turn-on surge, first 1/2-cycle.</td>
<td>50A max</td>
<td>115V a-c, typical load 25°C cold start</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td>50/60Hz nominal; range 47-440Hz(1)</td>
<td>Single Phase</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EMI</td>
<td>Meets the conducted noise standard of FCC 20780, Class B and VDE 0871, Class B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Leakage current</td>
<td>0.5mA</td>
<td>115V a-c (UL method) 25°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.75mA</td>
<td>230V a-c (VDE method) 25°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Startup time</td>
<td>400msec (typ)</td>
<td>500msec (typ)</td>
<td>Std.(2)</td>
<td></td>
</tr>
<tr>
<td>Holdup time</td>
<td>20ms</td>
<td>Std.(2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Circuit type</td>
<td>Flyback</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching frequency</td>
<td>~100KHz</td>
<td>80KHz typ</td>
<td>Operating</td>
<td></td>
</tr>
</tbody>
</table>

(1) At 440Hz the leakage current exceeds the UL/VDE safety specification limit.
(2) Std conditions = nominal input, typical load, 25°C

### MRW OUTPUT CHARACTERISTICS

<table>
<thead>
<tr>
<th>SPECIFICATION</th>
<th>MRW 150KV/MRW 151KV</th>
<th>MRW 160KV/MRW 161KV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source effect</td>
<td>1% max</td>
<td>1% max</td>
</tr>
<tr>
<td>Load effect</td>
<td>3% max</td>
<td>5% max</td>
</tr>
<tr>
<td>Temperature effect</td>
<td>2% max</td>
<td>2% max</td>
</tr>
<tr>
<td>Combined effect (source, load, &amp; temperature)</td>
<td>+4%-2% max</td>
<td>+4%-6% max</td>
</tr>
<tr>
<td>Time effect (drift)</td>
<td>0.5% max</td>
<td>0.5-8.5 hr; nom input, rated load, 25°C</td>
</tr>
<tr>
<td>Cross effect</td>
<td>Output #1</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Output #2</td>
<td>1.5% max</td>
</tr>
<tr>
<td></td>
<td>Output #3</td>
<td>0.5% max</td>
</tr>
<tr>
<td>Recovery characteristics:</td>
<td>Excursion</td>
<td>&lt;4.0%</td>
</tr>
<tr>
<td></td>
<td>Recovery (within ±1%)</td>
<td>&lt;2msec</td>
</tr>
</tbody>
</table>
### MRW MODEL TABLE

<table>
<thead>
<tr>
<th>SPECIFICATION</th>
<th>OUTPUT VOLTAGE</th>
<th>OVP SETTING</th>
<th>OUTPUT CURRENT</th>
<th>CURRENT LIMIT</th>
<th>OUTPUT POWER</th>
<th>RIPPLE SOURCE</th>
<th>SWITCHING</th>
<th>NOISE (SPMK)</th>
<th>EFFICIENCY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Units</td>
<td>Volts</td>
<td>Volts</td>
<td>Amps</td>
<td>Watts</td>
<td>mV</td>
<td>mV</td>
<td>Percent</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Condition</td>
<td>Factory set(1)</td>
<td>Adjustment range(2)</td>
<td>Nominal input, 25°C</td>
<td>Nominal input</td>
<td>40°C, 50°C, 60°C, 71°C</td>
<td>Nominal input, typ load</td>
<td>d-c, 1b, 20MHz</td>
<td>Nominal input, rated load</td>
<td>Volts, Watts</td>
</tr>
</tbody>
</table>

#### MRW 150KV (35 WATTS)

- **Output #1** +5 4.75-5.25 5.8-6.9 1.0-2.2 (typ) (4.0 max)
  - Total maximum output power no more than 35.0 35.0 24.5 14.0 30 50 150 70%
- **Output #2** +12 4.75-5.25 5.8-6.9 1.0-2.2 (typ) (4.0 max)
  - Total maximum output power no more than 35.0 35.0 24.5 14.0 30 50 150 70%
- **Output #3** -12 4.75-5.25 5.8-6.9 1.0-2.2 (typ) (4.0 max)
  - Total maximum output power no more than 35.0 35.0 24.5 14.0 30 50 150 70%

#### MRW 151KV (35 WATTS)

- **Output #1** +15 4.75-5.25 5.8-6.9 1.0-2.2 (typ) (4.0 max)
  - Total maximum output power no more than 50 50 35 20 30 50 150 72%
- **Output #2** +12 4.75-5.25 5.8-6.9 1.0-2.2 (typ) (4.0 max)
  - Total maximum output power no more than 50 50 35 20 30 50 150 72%
- **Output #3** -15 4.75-5.25 5.8-6.9 1.0-2.2 (typ) (4.0 max)
  - Total maximum output power no more than 50 50 35 20 30 50 150 72%

#### MRW 160KV (50 WATTS)

- **Output #1** +5 4.75-5.25 5.8-6.9 1.0-5.0 (typ) (6.0 max)
  - Total maximum output power no more than 60 Watts
- **Output #2** +12 4.75-5.25 5.8-6.9 1.0-5.0 (typ) (6.0 max)
  - Total maximum output power no more than 60 Watts
- **Output #3** -12 4.75-5.25 5.8-6.9 1.0-5.0 (typ) (6.0 max)
  - Total maximum output power no more than 60 Watts

#### MRW 161KV (50 WATTS)

- **Output #1** +5 4.75-5.25 5.8-6.9 1.0-5.0 (typ) (6.0 max)
  - Total maximum output power no more than 60 Watts
- **Output #2** +15 4.75-5.25 5.8-6.9 1.0-5.0 (typ) (6.0 max)
  - Total maximum output power no more than 60 Watts
- **Output #3** -15 4.75-5.25 5.8-6.9 1.0-5.0 (typ) (6.0 max)
  - Total maximum output power no more than 60 Watts

(1) Nominal input, typical load, 25°C
(2) All outputs are shut down when OVP is activated
(3) Output #2 follows the adjustment of Output #1

### KEPCO

**TRIPLE OUTPUT, LOW PROFILE, OEM a-c TO d-c SWITCHING MODULES**

**SERIES MRW**

A new series of multi-output PC card switchers featuring a low profile (component height) on the popular 100x160mm footprint. The MRW 150KV and MRW 151KV produce 35W. MRW 160KV and MRW 161KV are rated for 50W continuous duty. All are triple output designs in which output #3 (the "-" rail) is stabilized by a 3-terminal regulator.

### MRW GENERAL SPECIFICATIONS

<table>
<thead>
<tr>
<th>SPECIFICATION</th>
<th>RATING/DESCRIPTION</th>
<th>CONDITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>0-71°C (see model table)</td>
<td>Operating</td>
</tr>
<tr>
<td></td>
<td>-40 to 85°C</td>
<td>Storage</td>
</tr>
<tr>
<td>Humidity</td>
<td>95% RH</td>
<td>Non-condensing; operating &amp; storage</td>
</tr>
<tr>
<td>Shock</td>
<td>20g, 3 axes (11msec ±5msec pulse duration)</td>
<td>Non-operating 3 shocks each axis</td>
</tr>
<tr>
<td>Vibration</td>
<td>5-10Hz; 10mm amplitude</td>
<td>Non-operating 1 hour each axis</td>
</tr>
<tr>
<td>Isolation Output to ground</td>
<td>500V d-c, 100MΩ</td>
<td>Non-operating 1 hour each axis</td>
</tr>
<tr>
<td>Isolation Voltage</td>
<td>3.75KV a-c for 1 minute</td>
<td>Non-operating 1 hour each axis</td>
</tr>
<tr>
<td>Safety</td>
<td>UL 478 recognized, CSA C22.2 certified, VDE 0806/IEC 380 approved by TUV Rheinland</td>
<td>25°C, 65% RH</td>
</tr>
<tr>
<td>Type of construction</td>
<td>PC card</td>
<td>25°C, 65% RH</td>
</tr>
<tr>
<td>Enclosure</td>
<td>Optional metal</td>
<td>Y capacitor removed</td>
</tr>
<tr>
<td>Cooling</td>
<td>Convection</td>
<td>25°C, 65% RH</td>
</tr>
</tbody>
</table>

KEPCO, INC. • 131-38 SANFORD AVE • FLUSHING, NY 11352 USA • TEL: (718) 461-7000 • FAX: (718) 767-1102 • Easylink (TWX): 710-582-2631
A feature of MRW is the ability to draw nearly full power from either of the two "+" rails. The curves reproduced to the right illustrate how the current from one output can be balanced against the other to power your application. Note the effect of the secondary voltage dropping when the primary output's load is reduced below its minimum value (the stabilization of the secondary output is degraded).

**KEPCO TRIPLE OUTPUT, LOW PROFILE, OEM a-c TO d-c SWITCHING MODULES SERIES MRW**

**OUTPUT RATINGS (MRW 150KV)**
- **MAX POWER**: 38.5W

**OUTPUT RATINGS (MRW 151KV)**
- **MAX POWER**: 38.5W

**OUTPUT RATINGS (MRW 160KV)**
- **MAX POWER**: 60W

**OUTPUT RATINGS (MRW 161KV)**
- **MAX POWER**: 60W

**NOTE1:**
- Forced air 20 CFM at 1 atmosphere

**DIMENSIONS**
- MRW 150KV:
  - inches: 1.14 x 3.94 x 6.3
  - mm: 29 x 100 x 160
- MRW 151KV:
  - inches: 1.14 x 3.94 x 6.3
  - mm: 29 x 100 x 160
- MRW 160KV:
  - inches: 1.5 x 3.94 x 6.3
  - mm: 38 x 100 x 160
- MRW 161KV:
  - inches: 1.5 x 3.94 x 6.3
  - mm: 38 x 100 x 160

**NET WEIGHT**
- **MRW 150KV**: 12.35 oz, 350 gm
- **MRW 151KV**: 12.35 oz, 350 gm
- **MRW 160KV**: 17.65 oz, 500 gm
- **MRW 161KV**: 17.65 oz, 500 gm

**OPTIONAL STEEL ENCLOSURES:**
- For MRW 150KV: CA 19
- For MRW 151KV: CA 19
- For MRW 160KV: CA 20
- For MRW 161KV: CA 20

**INPUT-OUTPUT CABLE KITS:**
- For MRW 150KV: 219-0184
- For MRW 151KV: 219-0184
- For MRW 160KV: 219-0184
- For MRW 161KV: 219-0184

**OUTLINE DIMENSIONAL DRAWINGS**
Dimensions in light face type are in inches, dimensions in bold face type are in millimeters.
Omron optical switches keep an eye on innovation. They work by sight rather than touch. Which means they won't wear out like electromechanical switches in tough applications such as duplicating, fax machines and computer peripherals. In fact, our optical switches operate thousands of times faster than electromechanical switches. And, they perform reliably for up to twenty years or more, exceeding the lifetime of the product itself.

Omron's optical switches dramatically improve the reliability of your end product by virtually eliminating switch failure. Take switches. There are over 50 Or ask us about the more than components we produce. You can reach us at 1-800-62-OMRON.

EDN December 19, 1991

CIRCLE NO. 133
If you think DSPs are priced
Our TMS320 family starts at
out of reach, think again.
just $3.

Cost is no longer a barrier to using DSPs. At Texas Instruments, our TMS320 family is well within your reach, thanks in large part to a decade of DSP leadership.

16-bit DSPs as low as $3
Our 16-bit, fixed-point solutions begin at $3. At that, they are on a price par with microcontrollers and are as easy to use, yet give you 10X the performance. These DSPs are extremely well suited to high-volume applications, providing you with opportunities to optimize price/performance ratios. In fact, our 16-bit DSPs are replacing microcontrollers in mainstream applications such as answering machines and disk drives.

32-bit DSPs starting at $25
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Delay lines take on timing tasks

As system designs get more complex and operating speeds get faster, timing must be extremely precise. Programmable delay lines let designers adjust circuit timing and maximize the performance of today’s high-speed systems.

Tom Ormond, Senior Technical Editor

Programmable delay lines allow designers to readily introduce timing corrections in today’s systems. These devices employ control inputs to generate a variable delay between input and output signal transitions. The variable delay lets OEMs stock a single part for a variety of applications requiring delay lines. For one, you can use the variable delay in upgradable PCs to resolve speed mismatches between the upgraded CPU and the system clock.

Most programmable-delay-line applications fall into two categories—de-skewing and timing generation. In the first case, the lines cancel or compensate for the variations generated by system components. Typical de-skew applications would be found in clock-distribution systems, high-speed buses, instrumentation, and test equipment—especially automatic test equipment (ATE). In timing-generation applications, the delay line is used to initiate events at specified times. Typical applications would involve test equipment and other instrumentation.

Programmable delay lines typically employ one of two circuit approaches: selected path or analog variable. In analog-variable delay lines, the designs employ a constant signal path but rely on a variable control level to develop a given propagation delay. The ramp-and-generator design is a popular analog-variable approach because it is flexible and linear. In this design, an input signal transition causes a ramp voltage to start from an initial...
level. The ramp and control voltage levels serve as the inputs of a comparator that switches at a time determined by the value established at the control inputs.

Selected-path devices use digital gates to select one of several fixed-delay paths between the input and the output. Selected-path devices can consist of different elements, including transmission lines, digital gates, and RC delays. All these elements may be configured either in series or in parallel.

While implementations vary from manufacturer to manufacturer, most off-the-shelf programmable delay lines rely on similar operating theory. Hence, examining a single delay line—Analog Devices' AD9501—will give some insight into the internal workings of delay lines in general.

The inside story

As the block diagram in Fig 1a illustrates, the AD9501 consists of three main subcircuits—a linear ramp generator, an 8-bit D/A converter, and a voltage comparator. The rising edge of the input trigger pulse initiates the delay cycle by enabling the ramp generator. The voltage comparator monitors the ramp generator output and switches the delayed output High when the ramp voltage crosses the threshold set by the D/A-converter output voltage. Users program the threshold of the D/A-converter output voltage using digital inputs D₀ through D₇.

The internal timing diagram of the AD9501 (Fig 1b) provides a detailed illustration of how the delay is established. Minimum delay value t₀ equals the sum of trigger-circuit delay, ramp-generator delay, and comparator delay. The trigger-circuit delay and the comparator delay are fixed; ramp-generator delay varies as a function of the rate of change of the linear ramp and, to a lesser degree, the value of the offset voltage. Maximum delay is the sum of minimum delay (t₀₀) and full-scale program delay (tₒ₉₅). Ramp-generator delay is a measure of the time required for the ramp to slew from its reset voltage to the most positive D/A-converter reference voltage (00H). The difference in these two voltages is nominally 18 mV with offset-adjust open or 34 mV with offset-adjust grounded.

These two voltage levels require an offset between them for three reasons. An offset allows the ramp to reset and settle without reenter-
ing the voltage range of the D/A converter. Secondly, the D/A converter may overshoot as it switches to its most positive value (00H); this overshoot could generate false output pulses without the offset between the ramp reset voltage and the upper reference. Overshoot on the ramp could also develop false outputs if there were no offset. Finally, the ramp is slightly nonlinear for a short interval when it first starts. The offset shifts the most positive D/A-converter level below this nonlinear region and maintains ramp linearity for short programmed delay settings. The offset-adjust of the AD9501 allows the user to control the amount of offset separating the initial ramp voltage and the most positive D/A-converter reference. This, in turn, causes the ramp generator delay to vary.

**Buy, don't build**

While some applications might require an application-specific delay line, you can find a number of commercial programmable delay lines that will solve a variety of timing problems. These off-the-shelf components are available in packages that interface directly with standard logic families.

As the information in Table 1 indicates, commercial programmable delay lines offer varied performance attributes. Total programmable delay figures ranging from 2.5 to 10,000 nsec and delay-resolution figures as low as 5 psec illustrate the versatility of today's off-the-shelf devices. Units are available that will interface directly with logic families such as TTL, CMOS, and ECL. The delay lines will also operate at trigger rates as high as 800 MHz. Off-the-shelf delay lines are available for both commercial and military applications.

While the figures in the table illustrate delay-line capability, they don't tell the whole story; today's off-the-shelf units offer other advantages. When you look at printed circuit board real estate considerations, you'll find plenty of packaging options—14-, 16-, and 20-pin DIP, 28-pin PLCC (plastic leaded chip carrier), 32-pin quad flatpack, and gullwing, surface-mount units. All TTL-compatible units operate from one 5V supply, so there's no problem with unique power-supply requirements to consider. The TTL-compatible delay lines also have good driving capabilities—from 10 to 20 gates.

Technitrol and Analog Devices offer products screened to MIL-STD-883, and the PLD-ACT devices from Engineered Components have a standby mode power drain of only 5 nW. Brockettree even makes it easy to familiarize yourself with the information in Table 1.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Model</th>
<th>Total delay (nsec)</th>
<th>Delay steps (psec)</th>
<th>Logic output</th>
<th>Trigger rate (MHz)</th>
<th>Operating range</th>
<th>Package</th>
<th>Circuit type (AV=analog variable, SP=selected path)</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Devices</td>
<td>AD9501</td>
<td>2.5 to 10,000</td>
<td>10</td>
<td>TTL, CMOS</td>
<td>50</td>
<td>0 to 70, -55 to +125°C</td>
<td>20-pin DIP, plastic leaded chip carrier</td>
<td>AV From $8.60 (100)</td>
<td></td>
</tr>
<tr>
<td>Brooktree</td>
<td>B630</td>
<td>25 to 400</td>
<td>NS</td>
<td>TTL</td>
<td>50</td>
<td>-55 to +125°C</td>
<td>14-pin DIP</td>
<td>AV $11.10 (100)</td>
<td></td>
</tr>
<tr>
<td>Dallas Semiconductor</td>
<td>DS1020</td>
<td>74 to 522</td>
<td>250 to 1000</td>
<td>CMOS</td>
<td>0.020</td>
<td>0 to 70°C</td>
<td>16-pin DIP</td>
<td>AV $13 (1000)</td>
<td></td>
</tr>
<tr>
<td>Elmem Technology</td>
<td>PDL 6</td>
<td>3.1 to 31</td>
<td>50 to 500</td>
<td>ECL</td>
<td>80</td>
<td>-10 to +60°C</td>
<td>12-pin single in-line package</td>
<td>SP $63 (1000)</td>
<td></td>
</tr>
<tr>
<td>Engineered Components</td>
<td>PDL-ACT</td>
<td>15 to 358</td>
<td>1000 to 50,000</td>
<td>TTL</td>
<td>To 80</td>
<td>-40 to +85°C</td>
<td>16-pin DIP</td>
<td>SP $15 (100)</td>
<td></td>
</tr>
<tr>
<td>Motorola</td>
<td>MC10E/100E195</td>
<td>2.58</td>
<td>20</td>
<td>ECL</td>
<td>1000</td>
<td>0 to 85°C</td>
<td>28-lead plastic leaded chip carrier</td>
<td>SP $38.07</td>
<td></td>
</tr>
<tr>
<td>Newport</td>
<td>60A</td>
<td>14 to 91</td>
<td>1000 to 12,000</td>
<td>TTL</td>
<td>NS</td>
<td>0 to 70°C</td>
<td>16-pin DIP</td>
<td>NS £3.8</td>
<td></td>
</tr>
<tr>
<td>Sony</td>
<td>CBX1159QY</td>
<td>1.4 to 22</td>
<td>5</td>
<td>ECL</td>
<td>800</td>
<td>-55 to +125°C</td>
<td>32-pin quad flatpack</td>
<td>SP $25 to $40 (100)</td>
<td></td>
</tr>
<tr>
<td>Technitrol</td>
<td>GCTR PC</td>
<td>13 to 111</td>
<td>1000 to 15,000</td>
<td>TTL, CMOS</td>
<td>0.100 to 1</td>
<td>-55 to +125°C</td>
<td>16-pin gullwing surface mount</td>
<td>AV $49 (100)</td>
<td></td>
</tr>
</tbody>
</table>
with standard delay products. They offer a demonstration board that lets you test and evaluate the performance of their BT630 programmable delay lines. The board includes circuitry that can generate a TTL input signal that has user-selectable period and pulse width. The board also includes DIP switches to set the delay range and potentiometers for making fine delay-time adjustments.

Maximizing flexibility

The PDL-ACT devices from Engineered Components have been designed to allow for final delay adjustment during installation or after the lines have been installed in a circuit. These delay lines incorporate all required drive and pick-off circuitry and are self-contained in a 16-pin DIP. Compatible with TTL, advanced CMOS, and FAST (Fairchild Advanced Schottky TTL) logic families, the delay lines feature a hybrid design that includes compensation for propagation delays and incorporates internal termination at the output—no additional external components are required to obtain the required delay. The delay lines are programmed by inputting a logic 1 or 0 at each of the three programming pins. Because only dc levels are involved, you can program the lines using remote switches or you can perma-
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CIRCLE NO. 20

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CIRCLE NO. 50

COMPONENTS

With an 800-MHz max operating frequency, Sony’s ECL-compatible delay lines are designed for high-speed bus, test-equipment, and clock-distribution applications.

Looking down the road
Today's off-the-shelf programmable delay lines offer high performance. However, looking down the road, designers want more. They want more on-board functionality, higher resolutions, and faster programmability. This is particularly true in mixed-signal and VLSI ATE, where programmable-delay networks play an important role in minimizing overall test times without sacrificing precision. Multichannel event-triggered applications require more functionality and easier interfacing to µP/control circuitry.

Article Interest Quotient
(Circle One)
High 512 Medium 513 Low 514
The Series 6600/6700 Thermostats

Now you can ensure the highest level of thermal protection for your P.C. board without compromising its design. Specify an Airpax Series 6600 or 6700 miniature bimetallic snap-action thermostat.

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The 6600 is VDE approved; the 6700 is VDE pending.

A little information goes a long way.

To find out more about Airpax Series 6600/6700 thermostats, call or write us today. You'll see how so little can do so much to increase your P.C. board's reliability. Airpax, Husky Park, Frederick, MD 21701. (301) 663-5141. FAX (301) 698-0624. A North American Philips Company.
The Power in Telecommunications

The squeeze is on

Slimming is an obsession in the electronics industry as engineers face the task of making thinner cards to fit even more functions into standard racks. Once again Ericsson can help.

The new PKE is a 25-30 W DC/DC converter squeezed into a slim package little more than half the height of its predecessor, the internationally acclaimed PKA converter. The PKE is only 10.7 mm (0.42") high and has the same 3"x3" industry-standard footprint and pin out.

Having set the standard for DC/DC converters in 1983, Ericsson's new series represents a remarkable leap forward in power supply technology. The PKE needs no power derating over its entire ambient temperature range of -45 to +85 °C. Quite simply, no one else achieves this in so little space. And you can choose from versions with one, two or three regulated outputs.

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Sealed toggle switch meets severe-environment demands

If your control panel needs a toggle switch that can withstand the rigors of road graders, farm vehicles, or industrial processing equipment, the NT Series from Micro Switch is worth a look. Switches in the series have lever-to-bushing and cover-to-case seals made from a molded elastomer, as well as terminal inserts that are molded into the high-impact thermoplastic case.

This complete sealing of the switching chamber enables the toggle switches to comply with the UL 508, paragraph 13.3 hose-down test. You can use these switches in control panels that are subjected to periodic splashes or wash downs, such as the panels common to food and beverage equipment. The switches can also withstand exposure to heavy accumulations of moisture, such as that experienced by vehicles left outdoors overnight.

Options include 1-, 2-, or 4-pole circuitry; screw, quick-connect, or solder terminals; and momentary or maintained action. The switches are available in 5, 10, and 15A ratings. The toggle levers are 0.68-in. long and have a nonglare nickel finish. In addition to the bat-handle toggle lever, the company can furnish pull-to-unlock and logic-level versions.

NT Series switches have an operating range of -40 to +71°C and are UL recognized and CSA certified. List prices range from $11.59 to $26.44.

Micro Switch, 11 W Spring St, Freeport, IL 61032. Phone (815) 235-6600.

Circle No. 688

Surface-mount RC networks satisfy EMI/RFI filter applications

Advances in digital IC technology are creating stringent demands for the reduction of electromagnetic interference (EMI) and radio-frequency interference (RFI) in electronic equipment. EMI/RFI filters are used in personal computers, data terminals, test equipment, and process controllers to suppress high frequencies. Bourns's 601 Series EMI/RFI lowpass filters are smaller and less expensive than inductive-type filters. The filters come in surface-mount packages and use a resistor-capacitor (RC) network.

Featuring a T-configuration of 16 series resistors and 8 parallel capacitors, the filters can handle filtering for as many as eight lines. The filters are available with resistor values of 10 to 100Ω and capacitor values of 50 to 200 pF. Using 25Ω resistors, a filter's typical 3-dB attenuation point ranges from 20 to 64 MHz, depending on the capacitor value.

The tolerance for component values is ±10% for resistors and ±30% for capacitors. The operating temperature range is 10 to 85°C. In addition to 18- and 20-pin surface-mount packages, the filters are available in 18- and 20-pin plastic DIPs. Prices for the 601 series EMI/RFI filters begin at $2.15 (10,000).

Bourns Networks Inc, 1400 N 1000 W, Logan, UT 84321. Phone (801) 750-7200.

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Magnetic Speed Sensor

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Airpax, Cheshire Industrial Park, Cheshire, CT 06410. Phone (800) 982-0030; (203) 271-6000. Circle No. 392

Picosecond Delay Lines

The PE-23451 to PE-23460 series delay lines help control clock skew and allow users to fine-tune critical clock-distribution circuits. The series comes in delay values from 100 to 1000 psec, in 100-psec increments. The delay lines have an impedance of 50Ω and a maximum dc resistance of 0.5 or 1Ω, depending on part number. The devices meet UL 94V-0 flammability ratings. $2.44 (1000).

Pulse Engineering, 7250 Convoy Ct, San Diego, CA 92111. Phone (619) 268-2400. FAX (619) 268-2515. Circle No. 391

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Aerovox Inc, Electronic Products Group, 742 Belleville Ave, New Bedford, MA 02745. Phone (508) 999-1000. Circle No. 393

Low-Profile Crystal

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NDK Europe Ltd, Tolworth Tower, Ewell Rd, Surbiton KT6 7EL, UK. Phone (81) 390-8344. FAX (81) 390-6926. Circle No. 394

Microwave Transistor

Designed for VHF and UHF applications, the silicon bipolar B12V105 microwave transistor features a typical fT of 10 GHz at a collector current of 10 mA. At that current, the transistor has a gain of 18.1 dB at 1 GHz and 12.6 dB at 2 GHz. At 5 mA, the gain is 16 dB at 1 GHz. At a collector current of 2 mA, the noise figure is typically 1.6 dB at 1 GHz and 2 dB at 2 GHz. Package options include TO-92, SOT-23, SOT-143, 85-mil Micro-X, and hermetic 70-mil stripline. From $0.99 (1000).

Bipolaircs Inc, 5437 Scotts Valley Dr, Scotts Valley, CA 95066. Phone (408) 438-0806. Circle No. 395
Components

10Base-T Filter And Common-Mode Choke
The 1661 filter and isolator and the 1662 common-mode choke meet requirements of IEEE-802.3 10Base-T network systems. The filter and isolator provide 17-MHz lowpass filtering with 2-kV isolation in both transmit and receive lines. The common-mode choke attenuates common-mode noise signals by 20 dB, without differential loss. The 1661 and 1662, in 16- and 8-pin DIPs, respectively, £3.88 and £1.86 (100).

Newport Components Ltd, Tunners Dr, Blakelands North, Milton Keynes MK14 5NA, UK. Phone (908) 615232. Circle No. 396

120

Side-Actuated DIP Switch
The BP series of side-actuated DIP switches consists of 10 spst models having 1 through 8, 10, or 12 positions. Wiping contacts provide reliable switching, and high-temperature materials meet UL 94V-0 requirements. The contacts are rated at 100 mA (max) and have a resistance of <50 mΩ. All terminals are tin plated and epoxy sealed. Models are also available with gold-plated contacts. 8-position switch, $1.08 (1000).

C&K Components Inc, 15 Riverdale Ave, Newton, MA 02158. Phone (617) 964-6400. FAX (617) 527-3062. Circle No. 397

Solid-State Relays
The LH1500 family of solid-state relays features 21 devices that represent the most common relay forms. Included are Form A, Form B, Form A/B,C and dual versions of Form A and B. The relays use a GaAs LED for actuation control and a monolithic silicon chip comprising a photodiode array, control circuitry, and a DMOS output switch. Some of the relays employ current-limiting circuitry, enabling them to pass FCC voltage-surge requirements. The Form A/B relays have a break-before-make action that provides a true Form-C function in a solid-state relay. From $1.25 to $4.75 (1000).

AT&T Microelectronics, Dept 52AL040420, 555 Union Blvd, Allentown, PA 18103. Phone (800) 372-2447, ext 810. In Canada, (800) 553-2448, ext 810. Circle No. 398

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Philips Components, Box 218, Bldg BAF-153, 5600 MD Eindhoven, The Netherlands. Phone (40) 722091. FAX (40) 724825.

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Lumex Opto/Components Inc, 292 E Hellen Rd, Palatine, IL 60067. Phone (708) 359-2790. FAX (708) 359-8904. Circle No. 400

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Circle #99 For Sales Contact, Circle #100 For Literature

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Contact Bob Fryer, at (516)567-5600 ext. 390, for information on the above products.

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Circle #103 For Sales Contact, Circle #104 For Literature

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Spectrum Control Inc, 2185 W 8th St, Erie, PA 16505. Phone (814) 455-0966. Circle No. 402

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Arm yourself with LAN know-how

Setting up a local-area network is complicated—especially if you've never done it before. A clear idea of what you want to accomplish as well as a basic understanding of your hardware and software alternatives will help you deal with vendors and consultants.

Dan Strassberg, Technical Editor

FOR A LONG MOMENT, the phone line was silent. When the consultant spoke, his tone was one of disbelief tinged with exasperation: "You're going to do what in eight pages?" he demanded. "I'm going to write a primer for engineers who have no LAN experience and whose managers want them to set up a local-area network in an engineering department or a manufacturing-test area," I replied, my manner reflecting more humility than it had earlier. "I'm hoping to get these people to the point where they can ask questions of LAN hardware and software vendors without embarrassing themselves," I continued. There was another pregnant pause. "It's clear that you don't understand how enormous this field is," the consultant retorted. "I don't think you can do what you want to do; I'm not sure anyone can. For certain, what you've described would take a LAN expert, and you aren't one." "I know," I said, "but I'm certainly going to try."

At this point, the consultant seemed to change the subject abruptly; he asked if I ever get to New York City. I happened to be going the following week. He recommended that I stop at the McGraw-Hill Bookstore at 1221 Avenue of the Americas in Manhattan. Several other people gave me similar advice, asserting that the store's collection of technical books is unequaled elsewhere. When I arrived at 1221 and descended into the basement store, I asked where I could find LAN books. The salesperson directed me to a section of...
shelving at least four feet wide by
eight feet high, filled from top to
bottom and side to side with books
on networking and LANs. Even af­
ter the warnings I had received, I
gulped; I wasn't prepared for so
much material.

I began to think that perhaps one
of the most important things my tu­
torial could do would be to provide
a reading list. The box “LANs:
Read all about ‘em” names the
books I picked up at the bookstore
and elsewhere, as well as a few
magazine articles. Obviously, it in­
cludes only a small fraction of the
LAN and networking materials
available. However, some of the
materials are particularly useful.

To paraphrase Sophie Tucker, a
good LAN consultant, these days, is
hard to find. The networking field
is so vast and continues to evolve
so rapidly that most consultants
have experience with only a fraction
of the available products. Indeed,
many consultants are familiar with
only a few types of products. More­
over, because of its complexity and
rapid rate of change, the network­
ing field is rife with mythology
and strongly held opinions that, too
often, result from an incomplete
understanding. Unfortunately, the
consulting fraternity is not totally
innocent of disseminating mis­
information.

Still, the situation is not all bad.
If you have no networking experi­
ence, the person you need to guide
you is someone with relevant expe­
rience—somebody who knows prod­
ucts and techniques likely to work
for you, who understands where the
pitfalls lie and how to avoid them.
A consultant need not have experi­
ence with a wide variety of net­
working products and technologies.
The important thing is that your
consultant be familiar with net­
working requirements similar to
your own.

Nearly all modern texts on net­
working begin with a diagram of the
so-called 7-layer cake—the Interna­
tional Standards Organization’s
open-systems-interconnection
model (the ISO/OSI model). In an
attempt to guide you through the
black forest of connectivity, the OSI
model organizes network hardware
and software into seven conceptual
“layers.” The ability to categorize
an item as performing functions as­
associated with one or more layers
can be useful, because if you know
where the product belongs, you will
be less likely to compare it with an­
other product whose function is not
really equivalent.

Instead of digesting this cake,
you may be better off first deter-
mining why you want to have a LAN. LAN projects are important enough to justify a considerable amount of study before you commit to a course of action. Understanding both your immediate and longer-term goals can save you from selecting a seemingly cost-effective approach that you will outgrow rapidly. And careful examination can lead you to products that are less costly than those you had thought necessary. Although you don't want to choose too quickly, you also don't want to waste time trying to absorb everything there is to know about networks.

Once you know what you want to accomplish, you have to avoid jumping to conclusions about the products you must have and being swayed by every input you receive. Keep an open mind while talking to vendors, but remember that claims that seem too good to be true are usually just that. The best immunization against seductive sales pitches is to inoculate yourself with information. If you become confused by conflicting claims as you evaluate products, take time for additional study.

F J Derfler, Jr's PC Magazine Guide to Connectivity (see box) organizes the process of determining your needs and selecting the classes of products most likely to meet them. Bound into the book is a decision tree (flow chart) that asks questions about the types of data you expect to share, how you propose to use the data, and the physical arrangement of the people and equipment you want to connect. Each time the tree leads you to a class of hardware or software, it highlights strong and weak points typical of products in the class. Considering the complexity of the issues it deals with, the simplicity of the diagram is reassuring.

Another strong point of the book is its extensive, though hardly comprehensive, listing of connectivity products and vendors. This 51-pg appendix organizes the products into categories. Unfortunately, the section doesn't present the categories in any obvious order, and the book's index fails to mention the categories. Individual companies and products do appear in the index, however.

Glossaries untangle technobabble

In addition to a directory of connectivity products and services, an item that you'll quickly realize you need is a glossary of networking terms. Several of the source materials in the box contain glossaries, but a full-fledged dictionary wouldn't hurt. LANs are closely related to telecommunications, and the network field has picked up the telephone industry's penchant for technobabble. Many networking acronyms have other acronyms nested within them. Often, the second acronym is built on yet a third one. (An example is 10Base-T—which stands for 10-MHz, baseband-signaling, twisted-pair technology—a network-wiring scheme that forms a part of IEEE standard 802.3. IEEE-802.3 governs a network architecture that began life as Ethernet and is still commonly known by that name. The standard is just one in a family, collectively called IEEE-802.x, whose members cover a variety of LAN technologies.)

Networking glossaries worthy of the name are longer than this article; one that I found useful is in Derfler's guide. Actually, much of his book is equally useful. Chances are, before you're done you'll want to acquire additional texts, but if you have no LAN experience and you can afford only one book on networking, this guide should be it.

While fortifying yourself with some healthy LAN reading, you may find yourself mulling over some of the considerations that follow.

One common reason for wanting a network is to be able to share expensive hardware that no one computer user uses very heavily. A good example of an item you might want to share is a laser printer. If four or five people in a work group each use a printer for an average of a few minutes a day, together they won't use the printer more than an hour a day. If the cost of connecting the computers of all of the work-group members to a single printer is significantly less than the cost of buying four or five printers, the company saves money. The likelihood of any work-group member having to wait very long for a printout is small. If sharing a printer or some other piece of lightly used equipment (a modem, for example) is all you need to do, you can buy hardware (switchboxes) that will do the job. You might not think of several computers connected to one printer via a switchbox as a network, but such a setup is the most elementary form of a computer network.

A switchbox need not have a rotary or pushbutton switch on its front. If you had to walk over and set the switchbox to receive data from your PC every time you wanted to print, you would be losing a major advantage of printer sharing. Some switchboxes automatically connect to the PC of a user requesting printer services. Other users who try to use the printer at the same time receive a "busy" indication. To avoid this annoyance, some switchboxes incorporate a memory buffer. Then all us-
ers can send data to the switchbox at the same time, and the switchbox will buffer the incoming data and queue it up for printing.

Reaping real benefits

Printer-sharing hardware can give you a few networking benefits—most notably equipment-cost savings and perhaps some associated office-space savings. However, to achieve the major benefits of networking (file sharing is the first one that comes to mind), you must choose a more ambitious arrangement; in other words, a real network.

For small networks, an approach that has considerable appeal is "peer-to-peer" resource sharing. The majority of networks—including Unix-based networks—don't provide peer-to-peer capabilities. Most networks (that is, those without peer-to-peer resource sharing) designate the computers either as "clients" or "servers." A client is usually a PC or workstation at which an individual work-group member works. A server is a computer whose resources (printers, mass-storage devices, data files, certain program files) are available to all of the work-group members. Servers are often more powerful than the work-group members' computers. Without peer-to-peer resource sharing, the computer resources of an individual work-group member are available only to that member.

With peer-to-peer resource sharing, all of the networked computers perform both client and server functions. The situation sounds ideal until you consider the drawbacks. A significant drawback of MS-DOS-based peer-to-peer networks is the amount of memory the networking software uses. With DOS's ability to directly address only 640 kbytes, the amount of memory available for running client applications can be so limited that the individual PCs become all but useless. Using extended or expanded memory for portions of the network software and portions of client applications can alleviate these memory problems. Nevertheless, you don't need a great deal of imagination to envisionsoft-
ware-compatibility issues rearing their heads at nearly every turn.

Another approach sometimes used in small networks is to make only one computer both a client and a server. With PCs based on 80386 and i486 CPUs, you can create additional “virtual” 8086-based machines. Virtual machines behave as if they consist of dedicated hardware, whereas in fact, a virtual machine borrows all of its hardware resources from another computer. If you create a virtual machine, it can act as a client while the real machine performs as the server. The two machines can coexist happily—until a client application crashes. Even then, the server will continue working, blissfully unaware of the misfortune that has befallen its virtual-machine client. But to get the client application running again, you must reboot the virtual machine. Whether you like it or not, doing so means bringing down the real machine—in this case, the server. The effects on all of the other clients are potentially disastrous.

Such problems often dictate dedicating a computer as a server. Most networks have dedicated servers. Probably the most important attribute of a server is a fast hard-disk drive with greater capacity than you can imagine ever needing. Though an effective technique on client computers, using a disk cache to improve the access time of a hard disk may not prove very helpful on a server. A group of clients can ask a server to access many widely dispersed files in rapid succession. Caches determine what information they should store by analyzing which files the CPU has recently accessed. In a server, the likelihood is lower than in a client computer that a disk cache will contain information the CPU needs. Therefore, you should be sure the server’s hard drive has fast access even without improvements achieved through disk caching.

You might think that other factors—for example the speed at which messages travel around a network—would have a profound effect on the speed with which clients can access information. To be sure, network speed is affected by many factors. However, several authors report that tests show that with today’s technology, no factor is as important as the server’s hard-disk access speed. So when selecting a server, pick one with the fastest, highest capacity hard disk you can afford.

Many other considerations

Despite the importance of disk access speed, no discussion of LANs should neglect transmission media, physical topologies, logical topologies, and media-access protocols. When you start to deal with these topics, you begin to appreciate just how large and complex a field networking is.

The routes that the LAN signals travel within a building (the network’s physical topology) don’t necessarily bear any relationship to the way the computers that make up the LAN perceive the connection scheme (the network’s logical topology). Physically, a network can be a daisy chain (a bus) or a star. Logically, the network can be a star, a ring, or a bus. But a network that is physically a star can, for example, behave as if it were a ring. Moreover, all other permutations of physical and logical topologies are possible. In general, a physical star will be more reliable than a daisy chain, but the reliability has a price. Despite being easier to install, the physical star costs more than the daisy chain—it uses more cable and requires wiring-hub hardware at its center.

Examples of LAN architectures are Ethernet, Appletalk, Token Ring, and Arcnet (in which ARC is short for attached-resource computing). Although some network architectures are associated with particular physical topologies, when you choose an architecture, you often still have a choice of physical topology. On the other hand, choosing an architecture determines a network’s logical topology.

Similarly, some architectures tie you to a particular transmission medium, whereas others permit choosing among media. Examples of media are fiber-optic cable, coaxial cable, shielded twisted-pair cable, and unshielded twisted-pair cable. None of these descriptions is adequately detailed, however, because each medium has characteristics that depend strongly on its physical properties. Therefore, a specification for coaxial cable might call for type RG-58/AU.

Actually, the situation is a bit more complicated than the previous paragraph implies. For example, the term Ethernet is often changed or modified to tell you something about the medium. “Thick-wire” Ethernet refers to the original Ethernet implementation, which used thick, semi-rigid coaxial cable (a medium known in the trade as “frozen, yellow garden hose”). “Thin-wire” Ethernet (sometimes called “Cheapernet”) uses much thinner, flexible coaxial cable. The thinner medium is not only less expensive than the thick cable, it is easier to work with. However, using it reduces the maximum permissible...
length of the LAN cabling and necessitates placing the network's nodes (the points where you connect computers) closer together. The term 10Base-T Ethernet describes an implementation that uses unshielded twisted-pair cable—similar to that used for telephone wiring. Such cable is less expensive and easier to work with than the thin coax, but using it places still greater restrictions on wiring length.

**Mixing and matching technologies**

Sometimes, a network-architecture specification will let you combine networks having different architectures. For example, through a protocol named Ethertalk, Apple Computer has extended its Appletalk standard to let Appletalk networks take advantage of many attributes of the IEEE-802.3 Ethernet standard. Originally, Appletalk used an unshielded, twisted-pair wiring scheme now called Localtalk. Localtalk, which is still being installed, is an economical medium well suited to small networks. It is limited in speed, however, having a data rate (signaling rate) of 230 kbits/sec. Ethernet, now including twisted-pair implementations, supports a data rate of 10 Mbits/sec. Ethertalk also allows Appletalk networks to incorporate many more nodes than does Localtalk.

You should not confuse running Appletalk over Ethernet with the interconnection of networks. One of the hottest subjects in networking at the moment is "internetworking"—tying networks together; for example, connecting a network in a design department to one in a test-engineering department. Internetworking schemes use hardware systems called bridges, routers, and gateways.

A common misconception about LANs is that using fiber-optic cable will greatly increase a network's speed. Certainly, optical cable can handle much greater signal bandwidths than copper cable can. Nevertheless, in LANs as they exist today, the bandwidth of high-quality coaxial cable isn't what limits data rates. At present, LANs can achieve the same data rates with carefully chosen coax as with optical cable. Therefore other considerations should determine which medium you select. Paramount among these is cost—both the initial cost of the hardware and the installation cost. Other factors include the cable's diameter and flexibility (which affect its ease of installation), the maximum allowable cable length, the network's required degree of immunity to electrical interference (including lightning), the need for keeping the network secure from electronic eavesdropping, and the difficulty of adding nodes to an existing cable run.

A technology that is just emerging is the wireless LAN. Wireless LANs use radio-frequency (RF) or infrared signals as the transmission medium. Several RF schemes use spread-spectrum techniques in which the signals are disbursed over a wide frequency spectrum to improve both data security and the rejection of interference. Proponents of wireless LANs insist that the networks address two major costs of copper-wire (coaxial or twisted-pair) and fiber-optic-cable LANs: the cost of the cable and the cost of installing it. Although that claim is true, wireless-LAN hardware costs sufficiently more than cabled-LAN hardware to make informed consultants suggest that you need some reason besides cost for choosing a wireless LAN. One such reason is that with some wireless LANs, you can walk around your office using a notebook PC, all the while remaining connected to the network—the computer equivalent of using a cordless telephone.

**EDN December 19, 1991**
method of controlling nodes' access to the transmission medium. By definition, networking involves sharing the medium. With sharing comes the likelihood that several nodes will try to talk at once so that nobody can hear. There are several radically different access-control schemes (protocols). The three most important are carrier-sense, multiple-access with collision detection (CSMA/CD), used by Ethernet and defined by IEEE-802.3; token passing, used on IBM token-ring networks and defined by IEEE-802.5; and the scheme, apparently known only as the Arcnet scheme, used by

You have to walk a fine line between jumping to conclusions about the products you must have and being swayed by every input you receive.

The Arcnet protocol is in many ways less sophisticated than the other two. Each Arcnet adapter has a set of switches that you must program with a node number from 1 to 255. (Token-ring and Ethernet adapters require no such address-switch programming.) The lowest numbered node becomes the network controller. It polls all of the nodes for messages. A node that has no message remains silent. Nodes that have messages are granted use of the network for a limited time. Adding a node (for example by applying power to a computer that had been shut down), initiates a reconfiguration process that takes at most 65 msec. Thanks to the address switches, Arcnet adapters are relatively simple—a real advantage, but the scheme imposes a burden on the network manager. When network problems arise, he or she must know which address corresponds to which node. Woe betide the manager who loses (or fails to maintain) a record of the numbers assigned to an Arcnet LAN's nodes.

Although the topologies and protocols may be similar, typical applications of networks in electronic engineering departments are not entirely representative of LAN applications in business. There is probably more similarity between the uses of LANs on college campuses and in electronic-engineering departments in industry than there is with typical LAN applications in manufacturing, commerce, and finance. Design-engineering departments and universities have a significant lead over most nontechnical users in storing and manipulating graphical information. Despite the growing popularity of graphical user interfaces, computers outside engineering departments and universities still deal overwhelmingly with text.

The emphasis on graphics in engi-
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CIRCUIT NO. 48

COMPUTERS AND PERIPHERALS

neering means that your LAN requirements, though almost certainly not unique, probably aren’t run-of-the-mill. Confucius understated the real facts when he said that a picture is worth a thousand words. Without the use of data compression, high-resolution images (especially color images) require megabytes to store and transmit. A screen filled with text encoded in ASCII (American-Standard Code for Information Interchange) represents a mere two kilobytes. The high data content of images can tax networks designed for text.

Despite the differences between engineering LAN applications and many others, most of the areas that customarily concern LAN specialists are also important in engineering LANs. One such area is shared databases or simply shared access to files. A major reason for wanting a LAN is to free yourself from at least part of the nightmare of keeping track of multiple versions of data files. Consider this very simple case: Fred and Joe have a 2-man office—an office without a network. At various times, each of them creates files that the other one works on. When Joe needs to work on a file that Fred created, he asks Fred to copy it from his hard drive onto a floppy disk. Joe then loads the file onto his hard drive. Now there are three copies of the file. If Fred and Joe each work on their own copies, they will soon find it difficult, if not impossible, to figure out whose copy is the “correct” one.

With a LAN, only one copy of the file need exist—on the server’s hard drive. There are still complex issues involved when both Fred and Joe attempt to update the file simultaneously. However, network operating system-software and application-software packages designed to run on networks incorporate mechanisms for dealing with problems of this type. By installing a LAN, Fred and Joe can, in effect, delegate their file-revision-control problem to the authors of the software they use. When they select particular packages, they are opting for certain ways of making the tradeoffs. Chances are, though, that they won't have to give the tradeoffs another thought.

There are many reasons for the huge popularity of networking; you can almost guarantee that your list of reasons for setting up a departmental, facility-wide, or company-wide network aren’t unique. Moreover, once you have a network, you will discover ways to benefit from it that you hadn’t thought of originally. That networks drastically and permanently alter the way people do their jobs is no exaggeration. The effects of adopting networking are nearly as profound as those of adopting computers. Because of this great potential and great effect on people, you should take setting up a network very seriously; doing your homework will pay big dividends. If reading this article is the first research you’ve done on LANs, you have not really even scratched the surface. The references listed in the box will take you much further.

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The drive runs on 5V and can run on batteries. It draws 2W while reading or writing information, 1W when idle, 35 mW in standby mode, and 15 mW in sleep mode. The drive typically spins up in 1.5 sec. During the first second of activation after receiving a data-transfer request, the drive consumes 3.5W. In the next second, the drive consumes 2W while performing the requested data transfer. For the next 5 sec, the drive is in its 1W idle mode.

While in the idle mode, the drive keeps the platter spinning in case another data-transfer request appears. If no requests are made during the 5-sec idle time, the drive drops into its 35-mW standby mode. After another 5 sec of inactivity, the drive goes into its 15-mW sleep mode.

The controller circuitry includes a 32-kbyte data buffer and an IDE (integrated device electronics) disk interface that transfers data in bursts at 4 Mbytes/sec. The average seek time is 20 msec. The disk drive costs $485.


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The board functions as an application-development platform in Sun SPARCstations. You can also develop applications in MS-DOS or Unix using an IBM PC or compatible computer. A proprietary I/O port transfers 16-bit words at 5 MHz. Two full-duplex synchronous serial ports transfer data as 8-, 16-, or 32-bit words at 8.33 Mbps. An optional daughter board contains a dual-channel ADC and dual-channel DAC.

One option provides a 16-bit delta-sigma ADC sampling as fast as 50 kHz. Another option uses an 18-bit successive-approximation ADC sampling as fast as 200 kHz. The DPV DSP board costs £4395; the daughter board costs £600.


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Viewsonic, 12130 Mora Dr, Santa Fe Springs, CA 90670. Phone (800) 888-8583; (213) 946-0711. FAX (213) 946-1618. Circle No. 351

VMEbus Single-Board Computer

The VME201, a single-board computer (SBC) for the VMEbus, has a 16-MHz 68HC000 µP and complete slot-1 controller functions. It features two RS-232C ports, a 16-bit interrupt timer, four 32-pin JEDEC memory sockets for as much as 2 Mbytes of EPROM or 1 Mbyte of static RAM, a calendar clock, and a watchdog timer. An interrupt controller prioritizes interrupts from 12 sources, including the seven VMEbus interrupts, Sysfail, an abort switch, an on-board dual UART, and the watchdog interrupt. A standard version typically draws 700 mA from a 5V supply, and a low-power version draws less than 300 mA. Software options include Microware's OS9 and PDOS VMEPROM operating systems, as well as the company's Microbug debugger and monitor. $350 (100).

Micro-Link, 14602 N US Highway 31, Carmel, IN 46032. Phone (800) 428-6155. Circle No. 352

Sbus DSP Board

The Sbus board is a DSP development board for the Sbus in Sun SPARCstations. The board uses TI's 33-MHz TMS320C30 DSP chip and 128k x 32 bits of zero-wait-state RAM. You can expand the RAM to 512k x 32 bits. You can also add a daughter card, which has dual 16-bit ADCs and DACs. Daughter cards containing either a 200-kHz I/O module or a delta-sigma I/O module are also available. The board contains the company's 16-bit DSP-Link expansion bus for high-speed communication with other Sbus boards. Operating as an Sbus slave, the board has a 2k x 32-bit dual-port static RAM for communicating with the SPARCstation. $4595. Board with TI's assembler and linker, TI's C compiler, and SPOX operating system, $9595.

Computer and Peripherals

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The SDSP/C30D DSP system on a card suits Sbus-compatible workstations. The system hardware consists of a Texas Instruments 33-MHz TMS320C30 processor, 2k x 32-bit-word dual-port static RAM (SRAM), and 128k x 32-bit-word zero-wait-state SRAM (expandable to 512k). The base card accepts plug-in analog-signal I/O daughter boards, and the combination fits an Sbus single-slot space. Options exist for either a proprietary 16-bit parallel I/O port or a SCSI port. Software support includes an interface library of control functions and a device driver. Other software tools include a debug monitor, C compiler, and Spectron Microsystems Spox applications programming interface. System with device driver, debug monitor, and interface library, £2695; analog daughter board, £600.

Loughborough Sound Images, The Technology Centre, Epinal Way, Loughborough LE11 0QE, UK. Phone (509) 231843. FAX (509) 262433. Circle No. 355

STD-32 DSP Board
The ZT 89CT30 DSP board conforms to the STD-32 specification. The board contains a 27-MHz 56001 DSP chip, which executes 24-bit integer arithmetic. The board also contains two synchronous serial channels, a 24-bit Opto-22 interface, a watchdog timer, 2 kbytes of EEPROM; and a configurable DIP switch that lets the board control a variety of I/O operations. As an I/O controller, the board communicates with the STD system's master via dual-port I/O registers and a priority interrupt controller. Motorola’s C compiler and simulator are available for program development. An optional debugger and downloader is also available. The all-CMOS design operates from −40 to +85°C. $1050. Development kit, which includes the board, 12k x 24 bits of RAM, and the debugger and downloader, $1450.

Ziatech Corp., 3433 Roberto Ct, San Luis Obispo, CA 93401. Phone (805) 541-0488. FAX (805) 541-5088. Circle No. 356

STEbus Processor Board
The SCIM88 STEbus processor board combines a 16-MHz 80188 CPU with a user-defined 1-Mbyte memory array. You can populate the memory array with 0.5 Mbytes of EPROM or flash EPROM and 0.5 Mbytes of static RAM (SRAM). Of the SRAM, 16 kbytes are dual-ported, and 256 kbytes can be battery-backed. You can link the processor board to the company’s range of remote signal-conditioning modules via a front-panel ribbon connector. You can expand the function of the processor board with plug-in options, which include a VGA graphics controller, PC-communications ports, analog and digital I/O, and a prototyping module. Software options include DR-DOS and Sourceview, which is a source-level remote debugger for developing DOS-compatible target programs. SCIM88 without memory, £300.

Arcom Control Systems, Units 8-10 Clifton Rd, Cambridge CB1 4WH, UK. Phone (223) 411200. FAX (223) 410457. Circle No. 357

Sbus Graphics Board
The GXTRA 1280 single-slot graphics card works with the Sbus in Sun SPARCstations. It drives 1280 x 1024-pixel displays and has a Sun-4 keyboard and mouse port. The board contains an 8-bit color frame buffer, and it runs on Sun’s Open Windows 2.0 software. Windows executes partially on the board and partially on the host CPU. You can install multiple Sbus boards to service additional users on a single SPARCstation. The board uses a proprietary gate array, which accelerates low-level graphics primitives such as drawing 2-D vectors, solid fills, and characters. $2250.


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Computer Modules Inc, 2348C Walsh Ave, Santa Clara, CA 95051. Phone (408) 496-1881. FAX (408) 496-1886. Circle No. 362

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EDN December 19, 1991
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A 4-Cell Ni-Cad Regulator/Charger for Notebook Computers – Design Note 54

Tim Skovmand

The new LTC1155 Dual Power MOSFET Driver delivers 12V of gate drive to two N-channel power MOSFETs when powered from a 5V supply with no external components required. This ability, coupled with its micropower current demands and protection features, makes it an excellent choice for high side switching applications which previously required more expensive P-channel MOSFETs.

A notebook computer power supply system is a good example of an application which benefits directly from this high side driving scheme. A four cell, Ni-Cad battery pack can be used to power a 5V notebook computer system. Inexpensive N-channel power MOSFETs have very low ON resistance and can be used to switch power with low voltage drop between the battery pack and the 5V logic circuits.

Figure 1 shows how a battery charger and an extremely low voltage drop 5V regulator can be built using the new LTC1155 and three inexpensive power MOSFETs.
Quick Charge Battery Charger

One half of the LTC1155 Dual MOSFET Driver controls the charging of the battery pack. The 9V, 2A current limited wall unit is switched directly into the battery pack through an extremely low resistance MOSFET switch, Q2. The gate drive output, Pin 2, generates about 13V of gate drive to fully enhance Q1 and Q2. The voltage drop across Q2 is only 0.17V at 2A and, therefore, can be surface mounted to save board space.

An inexpensive thermistor, RT1, measures the battery temperature and latches the LTC1155 OFF when the temperature rises to 40°C by pulling low on pin 1, the Drain Sense Input. The window comparator also ensures that battery packs which are very cold (<10°C) are not quick charged.

Q1 drives an indicator lamp during quick charge to let the computer operator know that the battery pack is being charged properly. When the battery temperature rises to 40°C, the LTC1155 latches OFF and the battery charge current flowing through R9 drops to 150mA.

Extremely Low Voltage Drop Regulator

A four-cell Ni-Cad battery pack produces about 6V when fully charged. This voltage will drop to about 4.5V when the batteries are nearly discharged. The second half of the LTC1155 provides gate voltage drive, pin 7, for an extremely low voltage drop MOSFET regulator. The LT1431 controls the gate of Q4 and provides a regulated 5V output when the battery is above 5V. When the battery voltage drops below 5V, Q4 acts as a low resistance switch between the battery and the regulator output.

A second power MOSFET, Q3, connected between the 9V supply and the regulator output "bypasses" the main regulator when the 9V supply is connected. This means that the computer power is taken directly from the AC line while the charger wall unit is connected. The LT1431 provides regulation for both Q3 and Q4 and maintains a constant 5V at the regulator output. The diode string made up of diodes D2-D4 ensure that Q3 conducts all the regulator current when the wall unit is plugged in by separating the two gate voltages by about 2V.

R14 acts as a current sense for the regulator. The regulator latches OFF at 3A when the voltage drop between the second Drain Sense Input, pin 8, and the supply, pin 6, rises above 100mV. R10 and C3 provide a short delay. The µP can restart the regulator by turning the second input, pin 5, OFF and then back ON.

The regulator is switched OFF by the µP when the battery voltage drops below 4.6V. The standby current for the 5V, 2A regulator is less than 10µA. The regulator is switched ON again when the battery voltage rises during charging.

Very Low Power Dissipation

The power dissipation in the notebook computer is very low. The current limited wall unit dissipates the bulk of the power created by quick charging the battery pack. Q2 dissipates less than 0.5W. R9 dissipates about 0.7W. Q4 dissipates about 2W for a very short period of time when the batteries are fully charged and dissipates less than 0.5W as soon as the battery voltage drops to 5V. The three integrated circuits shown are micropower and dissipate virtually no power.

Cost Effective and Efficient Power System

The circuit shown in Figure 1 consumes very little board space. The LTC1155 is available in a 8-pin SO package and the three power MOSFETs can also be housed in SO packaging. Q4 must be heatsinked properly for the short period of time that the battery voltage is above 5.5V. (Consult the MOSFET manufacturer data sheet for SO heatsink recommendations).

The LTC1155 allows the use of inexpensive N-channel MOSFET switches to directly connect power from a 4-cell Ni-Cad battery pack to the charger and the load. This technique is very cost effective and is also very efficient. Nearly all the battery power is delivered directly to the load to ensure maximum operating time from the batteries.

For literature on our MOSFET Drivers, call (800) 637-5545. For applications help, call (408) 432-1900, Ext. 361
Circuit adjusts duty cycle, not frequency

Yongping Xia  
Dept of Electrical and Computer Engineering,  
West Virginia University, Morgantown, WV

The output of Fig 1’s circuit has an adjustable duty cycle that, once set, is constant for inputs that range in frequency from 30 Hz to 1 kHz. The leading edge of the input signal generates a 3-µsec pulse at point A. This pulse closes IC3A and causes the voltage on C4 to equal the output of IC28. The 3-µsec pulse also generates a narrower 1.5-µsec pulse at point B through C2, R2, IC1C. This pulse discharges the integrator after its peak output is stored in the hold capacitor C4. The integrator is composed of IC2B, R3, and C3 and has the following ramping rate:

\[
\text{Rate} = \frac{5V}{(R_a \times C_a)} = 0.106V/msec.
\]

Thus, if the input frequency is 100 Hz, the peak output of the integrator will be 1.06V.

IC2C buffers and R4 divides C1’s peak signal after which it serves as a reference for voltage comparator IC2A. The other comparator input is the output of the integrator at point C. When the signal at point C is lower than the reference, IC2A’s output will be negative. Otherwise, its output will be positive. Since point C is a linear ramp signal and the reference is the peak of that signal, IC2A’s output duty cycle will only depend on the divide ratio of R4. Thus, you can adjust the duty cycle by adjusting R4. The errors of R3 and C3 will not alter the output duty cycle.

The output of IC2A is between ±3.5V. IC1D, D1, and R5 convert this output to a standard TTL signal. With no input signal present, the integrator will reach the highest voltage and the output will stay at zero. Changing the frequency range of the circuit requires changing the values of the hold capacitor and components that make up the integrator and pulse generators.

EDN BBS /DL_SIG #1056

To Vote For This Design, Circle No. 746

Fig 1—Once you adjust and set R4, the output duty cycle of this circuit remains constant over a 30 Hz to 1 kHz range.
Filter quashes 60-Hz interference

Adolfo A Garcia  
*Analog Devices, Santa Clara, CA*

The circuit in Fig 1 filters 60-Hz interference from low-frequency, low-level signals. The filter exhibits 40-dB rejection \((Q = 0.75)\) and draws 95 µA max from a single-sided 5V supply.

Resistors \(R_1\), \(R_2\), and \(R_3\) and capacitors \(C_1\), \(C_2\), and \(C_3\) form a classic twin-T section, and IC1 and IC2 provide local and global feedback. The frequency selectivity \((Q)\) and the rejection performance of this active filter are very sensitive to the relative matching of the capacitors and resistors in the twin-T section. Table 1 shows rejection and \(Q\) as a function of the value of \(R_Q\).

\(R_4\), \(R_5\), \(C_4\), and IC3 form a very-low-impedance reference source to bias IC1 and the twin-T section to half the supply voltage.

To configure the filter to operate at 60 Hz, choose a \(Q\) that will provide enough rejection without excessive loss of desired low-frequency signals that may be close to the filter’s notch frequency. The value of \(R_Q\) is

\[
R_Q = (4Q - 2)R_7.
\]

The gain of the output amplifier is simply that of a conventional noninverting amplifier:

\[
A = 1 + \left( \frac{R_4}{R_7} \right) = 4Q - 1,
\]

and the overall gain of the band-reject filter below and above the notch frequency is

\[
\frac{V_{OUT}}{V_{IN}} = \frac{2A}{1 + A}.
\]

If you need additional rejection, cascade filter sections. Keep in mind that you might have to modify the circuit to account for out-of-band gain multiplication.

**EDN BB S /DL_SIG #1036**

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**Table 1—** \(R_Q\) rejection at 60 Hz, and the filter’s voltage gain as a function of the filter \(Q\)

<table>
<thead>
<tr>
<th>Filter (Q)</th>
<th>(R_Q) (kΩ)</th>
<th>Rejection (dB)</th>
<th>(V_{OUT}/V_{IN})</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.75</td>
<td>1.0</td>
<td>40</td>
<td>1.33</td>
</tr>
<tr>
<td>1.00</td>
<td>2.0</td>
<td>35</td>
<td>1.50</td>
</tr>
<tr>
<td>1.25</td>
<td>3.0</td>
<td>30</td>
<td>1.60</td>
</tr>
<tr>
<td>2.50</td>
<td>8.0</td>
<td>25</td>
<td>1.80</td>
</tr>
<tr>
<td>5.00</td>
<td>18</td>
<td>20</td>
<td>1.90</td>
</tr>
<tr>
<td>10.0</td>
<td>38</td>
<td>15</td>
<td>1.95</td>
</tr>
</tbody>
</table>

---

**Fig 1—** This notch filter suppresses 60-Hz interference in low-frequency signals.
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Take a look at the fresh, innovative, and dynamic graphic and editorial enhancement of EDN in the January 20th Magazine Edition.
EMC/EMI Materials Design Manual
The 24-pg Materials Design Manual contains information on properties of materials used to prevent electromagnetic interference, as well as design tips, formulae, and product applications. In particular, the manual discusses the new EC Directive on EMC, 89/336/EEC, a standard that takes effect in January of 1992. This directive affects European Community business standards as well as businesses that deal internationally and plan to conduct business within the EEC after the first of the year.

Nutwood Publicity Ltd, Marketing Consultants to RFI Shielding Ltd, Boyton End Farmhouse, Baythorne End, Halstead, Essex CO9 4AW, UK.

Plethora Of Connectors And Related Products
This 576-pg catalog, Electronic Interconnection Systems, is a product-ordering guide to connectors and related products. It describes connectors for IC sockets; board-mount and wire-mount sockets; Mix stacking; headers; plugs; DIN standard; pc boards; DIPs; card edge; D-sub; and D-ribbon. Related products include breadboard systems, cable, and assembly equipment. The publication features cross-reference charts for locating the products you want. Three indexes are classified by grid spacing, part number, and product type. Physical, electrical, and environmental specifications are given for each product.

3M, Electronic Products Div Catalog, Box 3064, Cedar Rapids, IA 52406.

Publication Features Adjustable Speed Controls
The 8-pg brochure, Type ABL, presents operating and application information for the Type ABL low-voltage, adjustable speed controls for brushless dc motors. It discusses the three chassis-level PWM models: analog voltage, 8-bit parallel digital, or variable frequency. The publication describes other features, such as dynamic braking, plug-reversible direction control, adjustable acceleration rates, and current limiting. Specifications for the ABL-compatible 34B brushless dc motors and gearmotors as well as optional ABL accessories are included.

Bodine Electric Co, 2500 W Bradley Pl, Chicago, IL 60618.

Catalog Of Components
This 100-pg catalog provides an expansive listing of fuses, fuse holders, ac connectors and plugs, Nema 5-15R outlets, power-entry modules, and voltage selectors. It describes components for ac power-entry products having 1 to 20A IEC 320 inlets and outlets. Also featured are plugs for cold or hot connections, snap-in and chassis-mount filtered power-entry modules, and the Felcom series of modular power-entry modules for custom configurations. It discusses newly introduced products, such as medical-grade fuse holders with captive fuse carriers, filtered and unfiltered power-entry modules, and 250V microfuses with pc-board leads built to IEC standards with UL recognition.

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Instrumentation-Software Demo Package

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Catalog Of PC Tools

This 160-pg catalog describes a comprehensive selection of PC software and hardware products; descriptions include product options and system requirements. Some of the book's 12 sections include Hardware Accessories, IEEE-488 Software & Hardware, Schematic Capture & PCB Layout, Logic Programming & Simulation, Analysis & Design Programs, CAD, Programming Tools & Utilities, and Text Processing. The Product Index helps you find your selections. Discounts for related products are specified in the “Acom-Packs,” which are found throughout the catalog.

App Notes Cover FFTs, LabWindows, And VXI Systems

The first of these six application notes, titled An Introduction to the LabWindows Instrument Driver, describes the components of an instrument driver and the interaction between the driver components. Developing a LabWindows Instrument Driver explains how to use the core driver utility functions to perform error handling. Fast Fourier Transforms and Power Spectra in LabWindows examines the building of a signal-processing application, using the Labwindows Advanced Analysis Library. NI-488.2—What’s New? discusses the functions, routines, user-interface options, and other features added to the driver software. Use of Local Shared RAM on NI-VXI Interfaces, Using VXImemAlloc(), VXImemCopy(), and VXImemFree(), examines special functions for application programs that share local RAM with the VXIbus. Finally, Using NI-VXI Software for VMEbus Systems, explains how to use the NI-VXI software to configure and program a VMEbus system.
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ASIC Design Brochure
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Austria Mikro Systeme International, Schloss Premstatten, A-8141 Unterpremstätten, Austria. Phone (3136) 36660, FAX (3136) 2501-3650. Circle No. 430

Brochure Discusses Custom Mixed-Signal ICs
The 12-pg brochure, Mixed Signal IC Custom Solutions, surveys design approach, computer-aided tools, process technologies, fabrication capability, and assembly operation. Easy-to-read charts compare and contrast design approaches and processes. A flow chart shows how the step-by-step approach allows satisfactory custom solutions.

Silicon Systems, 14351 Myford Rd, Tustin, CA 92680. Circle No. 431

All About Radiation Hard Products
This 700-pg publication contains product information about silicon-on-sapphire ICs. It describes RAMs containing as many as 64k bits, logic, 1553 databus components, 29xx bit slice, and MIL-STD 1750A microprocessors and peripheral devices. Also included are ASICs having as many as 30,000 gates.

GEC Plessey Semiconductors, Cheney Manor, Swindon, Wiltshire SN2 2QW, UK. Circle No. 433

Four Publications Present IC Products
The sixth edition of ASIC & Custom Products Short Form Catalog provides single-page descriptions of devices from the frequency-synthesis, forward-error-correction (FEC), and coding and demodulation product families. The book also outlines the custom design service. The DDS Handbook offers 216 pages of data sheets and application notes on direct-digital-synthesis products, from ASICs through board- and chassis-level products. The Spread Spectrum Handbook is a 189-pg compilation of data sheets and application products. The Forward Error Correction Handbook covers FEC encoding and decoding in its 56 pages of data sheets.

Stanford Telecom, ASIC & Custom Products Div, 2421 Mission College Blvd, Santa Clara, CA 95056. Circle No. 434
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Listing Of Power Supplies And DC/DC Converters

This 16-pg catalog offers a quick glance at the company's products for high-voltage power supplies and dc/dc converters. Proportional PC modules, miniature low-power converters, low-noise PC modules, precision photomultiplier supplies, miniature-rugged, regulated multiple-output, and precision-regulated CRT supplies, as well as custom high-voltage supplies are a few of the products covered in this catalog. For each section, a product photo accompanies specifications and related technology or information.

EMCO, 11126 Ridge Rd, Sutter Creek, CA 95685. Circle No. 440

Power-Conversion Catalog

This 148-pg power-conversion catalog provides specifications, data sheets, an ordering guide, and applications for more than 170 power-conversion products. The range of products includes 57 wide-range input, dc/dc converter modules in industry-standard 2 x 2-in., 2 x 1-in., and 24-pin double DIPs. An extensive overview of the vendor's other products includes data-conversion hybrids, IBM PC/AT and VMEbus board-level products, and panel-mount instruments. A glossary of Power-Supply Terms and a section on Modern Power Supply Principles and Practices details some recent innovations in power-converter design as well as in standard design practices.

Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Circle No. 441

Switch-Mode Rectifier Series

This 23-pg short-form catalog presents electrical specifications, operating characteristics, and design benefits of the Twinpack switch-mode rectifier systems. It outlines the advantages of each component and offers charts and product photos. Describing Twinpack modular power systems, the publication includes the PS/19; system status/control panels; low-voltage disconnect panels; miniload centers; digital-equalize panels; fuse-alarm panels; fuse panels; circuit-breaker panels; battery-disconnect panels; positive or negative-bus bars; battery trays; relay racks; ringing generators; dc/dc converters; dc/ac static converters; and a µP monitor.

Power Conversion Products Inc, Box 380, Crystal Lake, IL 60014. Circle No. 442

Power-Protection Devices

This 46-pg catalog presents power-protection devices for PCs, microcomputers, minicomputers, LANs, workstations, PBXes, and other sensitive equipment. The table of contents lists section titles such as New Technology, How to Solve Power Problems, Choosing the Level of Protection That's Right for You, How to Buy a UPS, The Ferrups Line, Fortress, PLC, Spike-free, Interface Kits, Extended Runtime Options, Installation Options, and Service Plans. Photos and question-and-answer sections complement the product specifications, listings, and technology updates. The catalog's tables supply competitor's prices and comparative product information such as option prices and compatibility requirements.

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I/O—Input-output

ISO—International Standards Organization

LAN—Local-area network

LCA—Logic cell array

MAP—Manufacturing Automation Protocol. A network protocol developed by General Motors Corp to interconnect computers and programmable factory equipment.

MS-DOS—Microsoft disk operating system

MSI—Medium-scale integration

OEM—Original equipment manufacturer

OSI—Open-systems-interconnection

PAL—Programmable Array Logic, trademark of Advanced Micro Devices

PC—Personal computer

PLA—Programmable logic array

PLCC—Plastic leaded chip carrier

PLD—Programmable logic device

PROM—Programmable read-only memory

RAM—Random-access memory

RC—Resistance-capacitance

SSI—Small-scale integration

TCP/IP—Transfer control protocol/internet protocol

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TTL—Transistor-transistor logic

VHDL—VHDL Hardware Description Language

VHSIC—Very-high-speed integrated circuit

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