Special Report:
PC-based software makes board design easy and affordable
pg 126
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SPECIAL REPORT

Low-cost pc-board design tools 126

Low-cost pc-board design software packages that run on personal computers are easy to use and have many of the capabilities of more expensive packages. They are a smart choice for engineers who design their own boards or occasionally design prototype boards.—Doug Conner, Regional Editor

DESIGN FEATURES

RAID 5 architecture provides economical 141
failsafe disk storage

Traditional methods used to back up critical data can be expensive and slow. A parity-based disk-array architecture offers an alternative that attacks these drawbacks.—Michael Anderson, Micropolis Corp

Careful inductor selection optimizes 147
dc/dc converters

Higher output power levels and faster switching speeds have complicated the selection of inductors for small dc/dc converters. However, if you check circuit waveforms for anomalies and review key electrical parameters during the design phase, you can simplify the development of an optimized dc/dc converter.—Bruce D Moore, Maxim Integrated Products

An object-oriented show and tell 161

When it comes time to choose an object-oriented language, you have two options: A pure language that is a complete development system you must learn, or a hybrid language that links with the system you already have.—Chris Terry, Associate Editor

Continued on page 7
High Resolution Digital Meter:
4000 count digital readout; 20,000 count mode (Fluke 87) for 4½ digit resolution

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FROM THE WORLD LEADER IN DIGITAL MULTIMETERS.
Frequency and time-interval analyzers make and store long series of measurements with little or no dead time between readings. The units help spot problems you can't find with conventional counters by letting you visualize the measurements (pg 79).

**Frequency and time-interval analyzers:**

Units provide insights classic counters can't

Time-measurement instruments aren't restricted to counters and timers anymore. Analyzers that let you visualize long series of measurements can help you troubleshoot problems for which you would never dream of using a conventional counter. —Dan Strassberg, Associate Editor

**Learning Ada: Class provides fast track to understanding**

Given enough time and the right motivation, most engineers can learn to use the Ada programming language on their own. However, a training class will hasten language proficiency. —Steven H Leibson, Senior Regional Editor

**PRODUCT UPDATES**

- Dynamic timing analyzer 113
- Modular switching power supply 114
- 68030-based VXIbus controller 116
- SBus-based DSP board 118

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New 512K CMOS PROMs optimize performance.

As embedded control microprocessors shift into high gear, you need memory solutions that won't jam up system performance. With access times as low as 20 ns, our 512K PROMs with fast column access let your microprocessor read right from PROM. For applications from communications and networking to peripherals and avionics, these high-performance, high-density, low-power, CMOS PROMs move embedded control performance into the fast lane.

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Don’t expect much from the Advanced Computing Environment alliance. Such groups do little to further competition or innovation.

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PROFESSIONAL ISSUES 244
Engineering graduate schools face a difficult decade
Enrollments are declining, and a serious faculty shortage may lie ahead. —Jay Fraser, Associate Editor

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For $249 you can plug the Apex 16-MHz math coprocessor board from Second Wave Inc into your Apple Macintosh LC computer's processor-direct slot. The coprocessor accelerates math-intensive tasks such as CAD, graphics, and spreadsheets by five to ten times. Second Wave Inc, Austin, TX, (512) 343-9661, FAX (512) 343-9663. —JD Mosley

CALLING FOR DSP-CONFERENCE PAPERS

DSP Associates has issued a call for papers for its International Digital Signal Processing Applications and Technology Conference and Exhibition. The Conference, which will take place October 28 to 31 in Berlin, Germany, is focused entirely on the development needs and application challenges facing international DSP-product designers. Authors should concentrate on recent DSP-based developments and new products in telecommunications, speech processing, image processing/recognition, control systems, automotive engineering, VLSI and DSP architectures, geophysics, underwater and radar detection, consumer electronics, and other applications. Send (via mail or fax) 100-word abstracts to the company by June 30. Contact the company for more information about display booth space reservations, costs, and other details. DSP Associates, Newton Centre, MA, (617) 964-3817, FAX (617) 969-6689, contact Jim Buhrendorf; Antwerp, Belgium, 32 (3) 237-1677, FAX 32 (3) 248-1694, contact Lina Van Meerbeeck.—Susan Rose

PUBLICATION OPENS PC'S KEYBOARD PORT FOR EXPLOITATION

The keyboard port on IBM PC and compatible computers can provide a handy interface port if you know how to use it. "PC Keyboard Design," a $249 book-and-disk publication, provides detailed information on both the IBM PC/XT and PC/AT keyboard ports with suggestions for possible peripheral devices you might design to use these ports. The accompanying disk includes source code for managing the PC's keyboard controller. Annabooks, San Diego, CA, (619) 271-9526, FAX (619) 592-0061.—Steven H Leibson
MATH COPROCESSORS HIT HIGH AND LOW LIMITS

The $1075 Fasmath 83D87-40 math coprocessor from Cyrix Corp has an operational clock rate of 40 MHz and 5.5M-flops peak performance. For 80286-based computers, you can buy a $238 25-MHz coprocessor, the 82S87-25, that has power-management functions for battery-powered applications. When idle, the 25-MHz coprocessor consumes less than 100 µW of power. By stopping the clock and control input signals you can reduce the power consumption to less than 100 µW. Cyrix Corp, Richardson, TX, (214) 234-8387, FAX (214) 234-8397.—JD Mosley

MACINTOSH OS TIGHTENS APPLICATIONS TIES

Apple Computer Inc is now shipping its System 7 operating system (OS) for the Macintosh personal computer family. The OS supports multitasking as standard procedure, allows the use of virtual memory, and supports 32-bit addressing. The OS also features several tools that simplify interaction between applications packages, including the ability to “publish” data created with one program and “subscribe” to that data with other programs. Published data maintains a link to its source, ensuring that subscribers automatically receive updates when the data changes.

By the end of summer, all new Macintosh computers will come with the new OS factory-installed on the hard disk. Current Macintosh owners on maintenance programs will receive free upgrades. Other users can purchase a personal upgrade kit for $99 or a network upgrade kit, allowing you to update all network nodes simultaneously, for $349. The upgrade kits include the OS, tutorials, manuals, technical support, and a preinstallation tool that checks your programs and data for compatibility with the OS. If the tool finds problems, it provides a telephone number you can call for technical help. Apple Computer Inc, Cupertino, CA, (408) 996-1010.—Richard A Quinnell

ANIMATE CAD DRAWINGS FOR LIVELY DEMONSTRATIONS

Autodesk’s $795 Animator Pro offers a simple way to animate designs. The software can produce and display animations at resolutions as great as 1024 x 768 pixels. It can also read AutoCAD .DXF files and process a 2-D image using any of five different animation techniques. Your audience doesn’t need a copy of the software to play the resulting animation; all they need is an 80386-based computer that runs DOS. Autodesk Inc, Sausalito, CA, (415) 332-2344, FAX (415) 331-8093.—J D Mosley

OPTIMIZE FPGA DESIGNS IN NATIVE ARCHITECTURE

Exemplar’s Release 1.0 software tools combine synthesis, speed and area optimization, and mapping of field-programmable gate arrays (FPGAs) in one package. Most software packages that synthesize and optimize FPGAs don’t work at the architectural level, which slows the design process. The software reads inputs from ABEL, CUPL, Palasm 2 equations, PLA truth tables, and EDIF 2.0.0 netlists. You can also use VHDL (VHSIC hardware description language) RTL (register transfer level) synthesis to create designs. The software outputs a design mapped in the FPGA building blocks, requiring you to use the chip vendor’s tools for place and route. Libraries are available for Xilinx and Actel FPGA families, LSI Logic LCA10000, NEC CMOS6,
A cycle by cycle simulation of switch-mode power supplies is recognized as a difficult simulation task for SPICE-based simulators, which must cope with timings that can span 4 orders of magnitude. This problem invariably results in very long simulation times, but is improved considerably by MicroSim's approach of building the controller macromodel chips so that a significant section is simulated in the digital domain. PSpice's behavioral modeling and mixed analog/digital simulation capability makes this possible.

PSpice is available on the IBM-PC (running DOS or OS/2); Macintosh II; Sun 3, Sun 4, and SPARCstation; DECstation 2100, 3100, and 5000; and the VAX/VMS families. In addition to the PWM macromodels, the PSpice library contains over 3,500 analog and 1,500 digital parts which can be used in a variety of applications. Our technical staff has over 150 years of combined experience in CAD/CAE, and our software is supported by the engineers who wrote it.

For further information about the PSpice family of products, call us at (714) 770-3022, or toll free at (800) 245-3022. Find out for yourself why PSpice has become the standard for circuit simulation.
Toshiba 120g, and VLSI VGT200 gate arrays. The price for the architectural analyzer, one vendor-specific library, and an X-Window graphical user interface is $10,000 per seat for Unix and $6000 for DOS. Options include a $9000 VHDL RTL synthesizer, an $8000 schematic generator for EDIF netlists, and an $8000 library generator. Additional libraries are $5000. Exemplar Logic, Berkeley, CA, (415) 849-0937, FAX (415) 849-9935.—Doug Conner

LOW-COST MASK PROGRAMMING REPLACES FPGAs

Both Xilinx Inc and Altera Corp now have mask-programmable versions of their field-programmable gate arrays (FPGAs). The mask-programmable versions bridge the price gap between programmable gate arrays and ASICs, letting you quickly create a lower-cost pin-compatible replacement for your programmable logic. The field-programmable and mask-programmed versions are interchangeable. However, the mask-programmed versions operate at higher speeds internally because they use metal to replace the programmable interconnect circuitry. You need to verify that the higher speed doesn’t violate setup and hold constraints elsewhere in your design.

The Xilinx devices replace members of the XC3000 FPGA family. The $9 XC3330, $13 XC3342, and $25 (10,000) XC3390 cost 50 to 70% less than the programmable versions. The 100-MHz devices are pin and function compatible with the programmable devices, including emulation of the configuration logic associated with device programming. You can disable the emulation and skip the delay associated with initializing the programmable devices. The NRE charges range from $5000 to $9000, including test program generation, with prototypes available in three weeks.

The Altera devices replace the Max 5000 and EP1810 families. The NRE charge is $15,000, and prototypes can be ready in five weeks. Unit costs vary with package and design sizes. The typical price for an EPM5128 in a 68-lead plastic leaded chip carrier is $10 (5000). Xilinx Inc, San Jose, CA, (408) 559-7778, FAX (408) 559-7114. Altera Corp, San Jose, CA, (408) 984-2800.—Richard A Quinnell

FLASH MEMORY EMBEDS PROGRAM AND ERASE COMMANDS

The Am28F020 2M-bit flash memory from Advanced Micro Devices contains embedded code that automatically erases and programs the memory device. The embedded algorithms save you from writing and debugging the programming routines themselves. When you send the erase command to the chip, the device automatically preprograms, erases, and verifies the entire memory for an all-zero data pattern. The embedded erase algorithm terminates when the chip reaches an adequate erase margin, thereby preventing overerasure. The device doesn’t require any controls or timing during these operations. The device indicates to the system when it’s ready for reprogramming, during which the chip indicates its readiness for new data on a byte-by-byte basis. The devices comes in four speed grades, with access times of 90, 120, 150, and 200 nsec. Organized as 256k × 8 bits, the IC is available in a 32-pin PLCC (plastic leaded chip carrier) and a 32-pin plastic or ceramic DIP. The 200-nsec version in the PLCC package costs $44 (100). Advanced Micro Devices, Sunnyvale, CA, (800) 222-9323, (408) 740-5705, FAX (408) 749-3240.—Anne Watson Swager
There's only one real reason to specify Dale® wirewound resistors: We'll work harder turning something common into something uncommonly valuable. Up front, that means saving you selection time by producing every standard shape and size in the book. Plus, we give you immediate access to design assistance and a wide range of proven special products.

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EDN June 6, 1991
CIRCLE NO. 193
GRIDLESS ROUTER REALLY ELIMINATES GRID

Harris Scientific Calculations’ Freestyle pc-board router is a true gridless router (as opposed to pc-board routers that reduce the size of the grid to seem gridless). Instead of a grid, the device is a shape-based router that starts with routing obstacles placed on a circuit board. These obstacles include the board edges and component pads. Using clearance-driven push-and-shove and ripup-and-retry algorithms, the company claims this gridless router has yet to meet a board it couldn’t route to completion. Among its via editing features, the router allows stacked, staggered, and spiral buried and blind vias, coincident via rules and via tap-in under surface-mount pads. The router performs on-line design-rule checks based on rules that you can set by many characteristics including layer, class, net, and boundaries. Running on both Sun and DEC workstations, the software costs $29,950. Harris Scientific Calculations, Fishers, NY, (716) 924-9303.—Michael C Markowitz

DATA-ANALYSIS SOFTWARE WORKS WITH IEEE-488 DIGITIZER

IOtech’s $1695 Turbolab graphical data display and analysis program calculates a 4096-point FFT in 1.5 sec. The program lets you collect data from as many as 16 analog channels and send it directly to your PC’s memory or disk. The software performs IIR-filter and FFT calculations for as many as 16,384 points and transparently uses your PC’s hard disk as a virtual memory when an operation requires additional RAM. In this way you can acquire, display, and manipulate waveforms of virtually any length. For seamless data acquisition, you can interface the software directly to the manufacturer’s $1795 ADC488 100-kHz, 16-bit IEEE-488 digitizer. The program comes with a module that automatically determines the memory and channel configuration of the ADC488 during startup. IOtech Inc, Cleveland, OH, (216) 439-4091, FAX (216) 439-4093.—J D Mosley

HANDHELD DMMs MEASURE CAPACITANCE AND FREQUENCY

John Fluke Mfg Co’s 70 Series II handheld digital multimeters (DMMs) consists of eight models at list prices ranging from $69 to $185. The flagship models 79 and 29 make all of the basic measurements with 4000-count resolution and 0.3% accuracy for dc volts. They also measure frequency to 20 kHz and capacitance to 9999 µF. John Fluke Mfg Co Inc, Everett, WA, (206) 347-6100.—Dan Strassberg

IC VERIFICATION SOFTWARE DISTRIBUTES TASK

Silvar-Lisco’s suite of IC-design tools, called SL-Verify, operate faster by distributing electrical- and design-rule checks and mask-data preparation across your entire network of available workstations. The software performs layout vs layout, schematic vs schematic, and layout vs schematic consistency checks. To facilitate making runset changes, the software lets you specify rules with variable limits. (The runset is the command file that defines what checks are to be performed and what rules each check shall use.) The $100,000 suite includes four tools: a block-based design-rule checker, an electrical-rule checker that performs parameter extraction, a mask-data preparation tool that includes E-beam and pattern-generation fracturing algorithms, and a manufacturing yield-analysis tool. A rule-set translator lets you use existing Dracula runsets. Silvar-Lisco, Sunnyvale, CA, (408) 991-6000, FAX (408) 737-9979.—Michael C Markowitz
30 MS/s DSO PLUS A TEST BENCH OF FUNCTIONS TIED UP IN ONE PORTABLE PACKAGE.

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- surface-mount • over 100 off-the-shelf models • immediate delivery

**low pass dc to 1200MHz**

<table>
<thead>
<tr>
<th>MODEL NO.</th>
<th>PASSBAND, MHz</th>
<th>center freq, MHz</th>
<th>STOP BAND, MHz</th>
<th>VSWR</th>
<th>PRICE</th>
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**high pass dc to 2500MHz**

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<th>STOP BAND, MHz</th>
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**bandpass 20 to 70MHz**

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<th>PASS BAND, MHz (loss &lt;1dB)</th>
<th>STOP BAND, MHz (loss &gt;10dB)</th>
<th>VSWR</th>
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**narrowband IF**

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<th>PASS BAND, MHz (loss &lt;1dB), STOP BAND, MHz (loss &gt;20dB)</th>
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**PRICE**

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<td>20+</td>
<td>18.95</td>
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Precision op amp guarantees spec
In the Technology Update, "Precision parts demand kid-glove treatment" (EDN, February 18, 1991, pg 99), Bob Dobkin of Linear Technology Corp doubts that anyone can ship a bipolar amplifier with an offset drift of less than 0.1 µV/°C. Because this comment appears immediately following Analog Devices’ (PMI Div) OP-177E TC specification of 0.1 µV/°C, it seems to imply that our product does not meet its published specification.
Bob says “... you can measure performance at this level five times and get five different answers.” True, there is some variation in measured values for all automatic testing; the goal is to refine the testing to a point where all five answers are very close together and then guardband for these test variations. The TC of the OP-177E is tested to a 0.1 µV/°C limit and is typically much better than that.

Derek Bowers
VP Engineering
Steve Sockolov
Linear Marketing Manager
Analog Devices
Santa Clara, CA

This recession’s job market is “less friendly”
Julie Anne Schofield’s article, “The Job Hunting Blues” (EDN, January 21, 1990, pg 230) is right on the mark.
As a 1971 graduate of Cal Tech who has had experience in many areas of electronics and applied physics, I’ve found the present job market much less friendly and much more competitive than when I was last job hunting in 1979. While cleaning out old magazines, I noticed that there were four or five times more job opportunities listed in EDN two or three years ago than in the current issues.
Julie writes, “Don’t even mention the purported engineer shortage to an engineer...” That’s for sure. I’m seriously considering leaving engineering to teach physics and astronomy. (I’m much less seriously considering going into music, but because only 20% of Juilliard graduates have music as their prime source of income, this seems less realistic.)

Craig McCluskey
Colorado Springs, CO

I agree with the Editor’s comment about Apple’s arrogance vis-a-vis an open bus and applications encouragement. I’ll add to this the company’s monopolistic, sole-source pricing philosophy, which has finally come around to bite Apple in the derriere, as witness the recent move to more reasonable prices.

Bill Travis
International Sales & Marketing Manager
Micro Networks
Worcester, MA

Frequency-synthesis technique questioned
The article, “Nonlinear division synthesizes multiple clock frequencies” (EDN, February 18, 1991, pg 169) by Sid Ghosh, is interesting in regard to the resulting phase jitter produced by dithering the divider between d and (d + 1). The tabulated clock frequencies in Table 2 are all related multiples of 8 kHz including the T1 rate of 1544 kHz. A PLL loop can synthesize all these frequencies mentioned in the first paragraph. The conventional analog VCO can be eliminated and a complete digital PLL can be implemented with the Signetics 74HC/HCT297 and a couple of programmable divide-by-N counters such as the 74HC/HCT40103.

Richard L Panosh
President
Vista Medical and Electronic Engineering
Lisle, IL

A promise of more reliability and less noise
Ricardo Rabinovich’s article “State-machine design curbs illegal states and transitions” (EDN, February 4, 1991, pg 95) promises novel ideas that might improve the reliability of the synchronous state machines I design. However, the proposed method of adding next-state-validation logic is likely to decrease,
rather than increase, the reliability of such state machines.

Ricardo discusses several approaches to improved reliability. However, it might be prudent to add another flip-flop at the input stage of the synchronizer so that the exclusive-OR gate input is not taken from the potentially metastable output of the first flip-flop.

The article discusses the implementation of a state machine that includes next-state-validation circuitry. I believe this implementation is less reliable than the equivalent conventional implementation with input synchronization of such state machines shown in the figure below:

---

The remainder of either state machine operates entirely on synchronous signals. In such a machine, errors are due to design error, circuit element failure, or unexpected 1-shot events, such as noise. However, if the next-state-validation logic is derived from the same equations as the next-state-generation logic, then errors in the state-machine specification will be present in both parts of the state machine, and it will do exactly what the designer (wrongly) tells it to do.

Because the proposed circuit has more components than a more conventional implementation, it will experience circuit-element failures more often and be less reliable.

Finally, Ricardo's circuit is supposed to be resistant to illegal transitions caused by noise. I will assume that an error occurs when, due to noise, the present-state register (PSR) is loaded with an inappropriate or illegal value.

If noise is the problem, the conventional state machine will present incorrect values to the PSR only if the noise occurs during setup and hold around the Sysclk edge.

In contrast, noise can affect the article's circuit in other ways:

1. NSD outputs are wrong around the edge of Sysclk. In this case the NSR is loaded with an incorrect value and, if the next-state-validation circuit does its job, the noise-induced error is ignored. This intended benefit eliminates the effect of noise, but only if the noise occurs at the time Sysclk is falling.

2. NSD outputs are wrong around the edge of Sysclk. The multiplexer circuit does not notice the error until after it has been loaded into the PSR and causes an illegal transition. The conventional implementation requires that the NSD include logic to deal with illegal states, but avoids the NSVAL (next-state-validation) burden.

3. NSVAL output is wrong around the edge of Sysclk. The next-state-validation circuit is also subject to noise. Noise causes a valid state transition to be ignored, an invalid state transition to be taken, or worst of all, the multiplexer to take some bits from the present state and some from the next state.

4. Multiplexer output is wrong around the edge of Sysclk. The multiplexer inputs, outputs, and circuits themselves are subject to noise, which may produce an illegal state transition.

Mechanism 2 (above) is the same mechanism that causes illegal transitions in a conventional state machine and would be expected to occur with a similar frequency in both implementations. Mechanisms 3 and 4 are unique to the proposed implementation and would make it less reliable than a conventional implementation.

Ricardo makes many good points about synchronization, decoupling, and timing analysis to ensure the most reliable state machine possible. But by adding more logic to try to detect illegal transition, he has made the circuit more vulnerable to noise.

Allen E Tracht
Principal Engineer
IOTech Inc
Cleveland, OH

(The author's reply: Some of the points that Allen Tracht has raised make sense, but others are debatable. The synchronizer circuit does not require an additional flip-flop because the output of the exclusive-OR gate is connected via the multiplexer to a flip-flop input. All three flip-flops of the input are synchronized by the same clock; therefore, a potential metastable condition in the first flip-flop will not propagate to the last flip-flop unless the metastable condition lasts longer than the clock cycle. An additional flip-flop at the input would be vulnerable to the same problem.

A circuit like the one in my article could require additional parts in a discrete implementation. This addition might be detrimental to system reliability due to the parts count. However, the additional...
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supervisory function could improve the overall reliability of the system. The kinds of techniques presented in my article are oriented toward ASIC implementations where the number of additional gates required for self-checking might not significantly jeopardize the overall reliability of the circuit.

I have not claimed 100% noise immunity for the self-checking circuit; rather, this circuit increases overall circuit-noise immunity.

Illegal states or transitions would be almost unavoidable if this circuit were to operate in a noisy environment. My article focuses on recovering from random noise. Redundant circuitry provides a recovery mechanism when an isolated fault occurs in either circuit, but not in both.

In a conventional state-machine architecture, a noise glitch will almost certainly put the state machine in an undesired state. The self-checking circuit (NSR/NSVAL/MUX) does not let the machine transit to a wrong state. Adding components for the additional circuit increases the possibility of catching more noise. However, noise in the self-checking circuit would not create erroneous state transition, but at worst, a 1-clock delay to a valid one.

A conventional state machine with an input deglitcher is also vulnerable to noise of duration wider than the deglitcher can filter out. The state machine with a self-checking circuit can detect and solve for illegal input combinations, thereby preventing illegal transitions.

This technique will build "forgiveness" in the circuit, but it will not replace good design practices.)

The measure of a solar cell's thickness

Jay Fraser’s article, “Who cares about power?” (Professional Issues, EDN, November 8, 1990, pg 381), is well written, but I question the statement on page 382 that reads: “...solar cells...have to be relatively thick, 25 to 50 mm.” Unless I’m missing something, any solar cell, no matter how transparent, won’t let light penetrate more than a quarter of an inch or so. The intended measurement was probably 25 to 50 mils, which is thick for silicon wafers, but not as thick as the numbers given.

James L Rieger, PE/PTBW
Ridgecrest, CA

(The author’s reply: James Rieger is indeed correct. The measurement of solar cells should be 25 to 50 mils thick.)

Correction

The News Break “A/D converters come in a new package” (EDN, March 14, 1991, pg 18) contains an error. The edited statement, “Missing codes are not guaranteed,” changes the meaning; the statement should read “No missing codes are guaranteed.”

Mea culpa

In the Technology Update on the STD Bus CPU board (EDN, March 28, 1991, pg 51), the Computer Dynamics Sales Inc listing in Table 1 got botched. The entry listed for “Sales Inc” is actually part of the Computer Dynamics Sales Inc data. EDN apologizes for the error.

HAVE YOUR SAY

Send your letters to Signals & Noise Editor, EDN Magazine, 275 Washington St, Newton, MA 02158. Or, send us a message via MCI mail at EDNBOS or via EDN’s bulletin-board system at (617) 558-4241 and leave a letter in the EDITORS Special Interest Group. You’ll need a 2400-bps or less modem and a communications program that is set for 8 data bits, no parity, and one stop bit, or 1200/2400, 8N1 in shorthand.
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FAX (408) 720-1305
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San Gregorio, CA 94074
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FAX (415) 726-3003
Micromint Inc
4 Park St
Vernon, CT 06066
(203) 871-6170
FAX (203) 872-2204

Second sources sought

We would like to find sources for the following parts: the Western Digital WD92C32 phase-locked-loop disk data separator and the NEC µPB9201C floppy-disk interface. The manufacturers no longer make these parts and our buyer has bought all he could find. If you don't know of a source, perhaps you could appeal to the EDN readers.
Margaret Motamed
Principal Member
Engineering Staff
Xerox Corp
El Segundo, CA

Big problem solved

I have a big problem: Who is the manufacturer of the TP3054 chip? Please tell me the company from which I can order this chip.
Joe Müller
Manager of Product Planning
John Lay Electronics
Littau, Switzerland
The CAPS system, which is available from Cahners Technical Information Services, lists two TP3054 manufacturers:
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(408) 721-5000
FAX (408) 730-0764
Texas Instruments Inc
Microprocessor & Microcontroller Products Div
Box 809066
Dallas, TX 75380
(800) 232-3200.

Reader wants to reduce noise of heartbeat signal

I am interested in learning techniques to decouple the noisy IBM power supply from my circuit cards that plug into the bus. Such a technique would let me work with very small signals such as EKG heartbeats and recording-studio-quality signals. Using op amps and trying to process signals in the millivolt and microvolt ranges, I get a lot of common-mode noise and such being fed in by the very noisy IBM power supply. Also, as programs are executed, the noise increases, so I need a way to make the 5, 12, -5, and -12V power supplies clean while the data fly all over the place.

As you've probably guessed, I've tried a wide range of capacitors, resistors, and inductors without success. I suspect that besides the noise I can see on a 20-MHz scope, there is even more outside this band. If someone could provide techniques to work with signals like this, it would open the door for better-quality products. I look forward to any light you can shed on this subject.
John Bereik
Covox Inc
Eugene, OR

No short reply in Ask EDN will solve your problem. Over the years, however, EDN has run a good number of contributed articles on noise reduction.
Also, Analog Devices is conducting a series of DSP seminars at locations around the country. The last hour or so of the seminar covers noise reduction. Associate Editor Dan Straussberg says that the material is very practical but is presented at such a break-neck pace that anyone who wants to carry away much useful information would be well advised to bring a tape recorder.

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<thead>
<tr>
<th>RFA120 FET Array</th>
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<tr>
<td>Operating Range:</td>
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<tr>
<td>Input Offset Voltage:</td>
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<td>Input Bias Current:</td>
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<td>Gain Bandwidth Product:</td>
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<td>Slew Rate (Gain = +1):</td>
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<th>Packaging</th>
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</table>

L = Low  LL = Low,Low  B = 3 Volt  X = Extended Temperature

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Several weeks ago, Compaq Computer Corp announced the Advanced Computing Environment (ACE) consortium, a group established to bring standardized RISC technology to personal computers. If the ACE plan bears fruit, personal computers in the mid-90s will have the power of industry-standard RISC systems, and users will be able to take advantage of standard PC software. To meet these goals, consortium members must develop standard hardware and software based on Mips Computing Systems' RISC microprocessors.

Although the consortium's plans call for each company to build on its own strengths, we're not holding our breath while we wait for advanced-RISC-computing (ARC) hardware and software products to reach users. In fact, the group's ARC specifications won't be available to non-ACE companies until the first ARC systems are sold. So much for an open and competitive market. If you think you've heard a similar story, you may be thinking of the consortium that Compaq led to adopt the Extended Industry Standard Architecture (EISA) several years ago. The member companies laid down grand plans for EISA to challenge IBM's Micro Channel Architecture. Today, you'll have difficulty finding an EISA PC or EISA add-in cards. The invisible hand of the market left EISA behind.

A similar scenario may loom ahead for the ACE companies: Because they're "cooperating," they're not competing. As is typical of such uncompetitive consortia, nothing in the ACE announcement suggests anything innovative in the group's approach to developing hardware or software. If anything, the consortium stifles innovation by adopting a broad plan for a so-called standard computer architecture and for operating systems arrived at by committee decision. I doubt that the ACE companies asked their customers what sort of mediocre committee "standard" they wanted vendors to foist on them.

Whenever a large number of companies forms a consortium to tackle a fast-moving market they let slip by them, mediocrity results. If the ACE members are serious about catching IBM and Sun Microsystems in the workstation and high-performance-PC market, they and we would be better off having the members act as competitors. By forcing each other to do better, they might come up with new products that would leave their rivals behind. After all, it has happened before. Just ask Sun and IBM.
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The lobster’s claw can move quickly and is a real threat in its natural habitat (as shown, it was a threat mostly to our photographer, who reported: Delicious!). Our habitat is an analog “real” world. To model and simulate it, Kepco’s ATE, BOP, BHK and OPS are the fastest analog power tools around. They offer the kind of voltage agility that allows a current stabilizer to recover quickly from the transient of a dynamic load. They provide you with the speed to program test voltages in rapid fire sequence. Tools include power to 1000 Watts, voltage to 5000 Volts and lobster to 5½ lbs. The bipolar models (BOP) operate in 4 quadrants. Conventionally filtered power tools are at home in your laboratory habitat.

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Breaking the Barriers...
MIXED-SIGNAL DESIGNS

Concurrency, circuitry foster testability

Digital circuit designers have a wealth of well-documented design techniques to guide them toward high circuit testability. Unfortunately, as they incorporate more analog circuitry in their ICs, designers sail further into uncharted waters. And these uncharted waters are rough on your budget; mixed-signal vendors estimate testing eats up 25 to 50% of NRE (nonrecurring-engineering-cost) dollars. Worse, test-program development can take from one to three months for a mixed-signal design versus a day or two for a digital design.

Mixed-signal circuits don’t have a checklist of “rules” of testability. “Checklists create too many questions” for you to use them on mixed-signal designs, according to Brice Baker, CAE Manager at Gould AMI. You can’t blindly start adding scan, partitioning, multiplexing, and built-in self-test functions. Blind adherence to added test-logic functions will likely cause your circuit to fall out of specification—though the added circuitry will enable you to measure how far. When you’re designing a mixed-signal circuit, you must carefully take account of the impact of each added function.

In some regards, mixed-signal circuits are like strictly digital designs. The secret to high testability is providing access to internal nodes for control and observation. The two design types differ, though, in the performance cost of such access. Whereas the parasitic effects of extra signal lines on a digital node may degrade performance by hundreds of picoseconds, the effect of extra signal lines on analog circuit components can be devastating.

The difficulty stems from the difference in what you’re trying to measure.

You evaluate digital logic by simply measuring voltage (high/low) and sometimes current. Analog measurements, on the other hand, include circuit response in the time and frequency domain, temperature variations, offset voltages, leakage currents, and stability conditions. And measuring these levels requires such additional tools as Bode plots, according to Randeep Soin, technology specialist at Genrad Ltd.

Solving the mixed-signal test problem

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Mixed-signal designs

isn’t easy. CAE tools for analog and mixed-signal design lag behind those for digital design, and even if the tools were comparable, metrics for measuring the test coverage of analog circuits are imprecise. High fault coverage, the digital benchmark, has little meaning in the analog domain.

The most promising approach to making testable mixed-signal circuits involves concurrent engineering. Standard sequential design styles have you design the part and pass it to the test engineer. The test engineer then writes the test program and hands it to the manufacturing engineer. Manufacturing builds the tooling and uses the test program to test the part. Often in mixed-signal design, this sequential flow is further complicated because different designers create the analog and digital logic.

The flaw in this development flow is that design decisions that cause test escapes and manufacturing difficulties aren’t usually identified until after you’ve finished creating the circuit. As a result, the cost of a redesign is weighed against test and manufacturing kluges. Too often the kluges win.

Using sequential development, even if the analog and digital designers communicate well, there is little feedback from test or manufacturing to design. Concurrent engineering attempts to guarantee feedback between departments and to guarantee that such feedback will come when it will do the most good—before the design is finished. According to Mani Soma, Associate Professor in Electrical Engineering at the University of Washington, test structures can’t be added as an afterthought. Test planning must be an integral part of the design phase of the mixed-signal circuit.

Everyone works together

Concurrent engineering merges all of the distinct development efforts into a joint effort. Not that you, as designers, develop test programs and marketing plans; rather, that you better understand the problems and issues of the other disciplines and weigh their impact on your design. As a result, the test engineer can recommend locations for you to insert test points while you are creating your design rather than asking you to kluge them in after you’ve simulated and debugged your circuit.

The need for concurrent engineering is acute because designers often have limited knowledge of test limitations and capabilities, according to Tom Quan, director of analog IC tools at Cadence Design Systems. Generally, you don’t know enough about such issues as DUT (device under test) boards, tester cabling, load boards, power supplies, and the parasitic capacitance and resistance of the test equipment. This lack of knowledge can translate into testing complications when you begin to use sequential engineering.

Though mixed-signal test development will still take longer than digital, that time will shrink due to the productive interaction of design engineers, test engineers, and manufacturing engineers. Better, development efforts will overlap rather than occur in a progression. So conception to production will...
Mixed-signal designs

take less time in exchange for test and design taking place at once. Not a bad exchange, considering the sacrifice is more of a streamlining than a loss.

While concurrent design is the most promising approach, it may cause cultural upheaval in your company. Changing who works and reports to whom and how product development time is budgeted presents political, social, and economic problems that are beyond the scope of this article. Regardless of these cultural difficulties, talking to your test engineers while you design will help you identify and avoid potential test pitfalls. There are also some tricks that, used judiciously and coupled with careful analysis, can improve the testability of your mixed-signal design.

Partition the design

First, since the digital and analog sub-blocks are often designed separately, partitioning the design and ensuring testability on either side of the interface is important. On the digital side, you can use structured approaches such as scan chains and built-in self-test. On the analog side, ad hoc approaches such as partitioning, providing internal access to individual blocks, and converting analog signals to digital can improve your designs.

The critical part of a mixed-signal design is the interface between the digital and analog circuits, according to Mark Ashton, product marketing manager for scan-based products at Schlumberger Technologies. If you can provide scan-chain access to the interface, you've got control and observation points into and out of both the analog and digital circuits.

Certainly, having easy access to your analog circuitry at the analog-digital boundary is likely to improve testability, but you shouldn't stop there. Internal access to your analog blocks is also important. Frank Binnendyk, product marketing manager at Mentor Graphics’ Simulation and Test Division, suggests that partitioning and providing access to individual analog blocks is also useful as a means of evaluating the entire design.

You can provide this internal access in a number of ways. Analog chip reference. He also notes an extension to this technique that buffers analog circuitry with DACs on the inputs and ADCs on the outputs. Die-size and pin-count considerations might preclude this technique’s practicability. Similarly, you can use voltage-to-frequency and frequency-to-voltage converters to measure digital values from inherently analog circuits.

![Buffering a circuit with a voltage-follower operational amplifier or with an emitter-follower discrete transistor allows you to measure internal signals with minimal impact. (Redrawn from “Testability Practices in the 1990s”)](image)

To maximize silicon utilization, you can share these comparators and converters internally using analog multiplexers and FET switches. These multiplexers and switches must provide access to the right nodes. Picking analog test points is much like picking test points for digital testing—nodes between blocks, at interface points, and at critical points in the design provide the highest efficacy. Unfortunately, since analog circuits are more sensitive than digital circuits, you must consider potential
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loading problems in your choice of test points. If connecting test equipment to particular nodes might disturb your circuit, add buffers between the node and the test point to isolate the node. Consider using impedance-matching networks when testing high-frequency circuits. Finally, as with your digital circuits, feedback loops greatly complicate testing; use analog switches to break automatic gain and frequency control loops wherever possible.

Jon Turino identifies two other important, common-sense considerations for analog testability. First, make sure the voltage or current levels you’re trying to measure are well above the noise of your test equipment. You’ll surely get more accurate and reproducible results measuring the 100-mV output of an operational amplifier rather than the 1-mV input.

Make test circuits testable

The second consideration is to remember that if you add circuitry to make your designs testable, these new circuits must also be testable. Test-logic evidence that your internal circuits are bad is only conclusive if you know the test logic is good.

Although the analog side constitutes the major sticking point in testing mixed-signal circuits, enhancements on the digital side, such as scan chains, can help. Scan chains are shift registers whose storage elements are shared with your sequential logic. Under normal circuit operation, you disable the shifting mechanism and the storage elements function as your design requires. In test mode, the storage elements serially shift data through the design. By alternating test and operating modes, you can preset and capture circuit values at embedded points in your design.

Many different versions of scan testability exist. These versions vary clocking schemes and the types of storage elements they allow. (For a more detailed discussion of how to use scan, see Ref’s 1, 2, and 3.)

Kent Koenig, test manager at NCR, recommends that if your digital circuitry includes a microprocessor bus, you can add an extra register for testing. Using this extra register, you can switch between internal and external references and control the multiplexers and switches.

Concurring with Koenig, Teradyne’s Manager of Test Applications, Randy Kramer, also suggests using a microprocessor bus when available. Because digital sections often have higher pin counts than the analog sections, Kramer also finds multiplexing an analog signal onto a digital pin in test mode a convenient and low-impact means of increasing your analog circuit observability.

On the other hand, many CAE...
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methods for making digital circuits testable require minimal design interference. Such techniques as Crosscheck's embedding test logic; logic-synthesis tools from Dassault Electronique, Racal-Redac, Synopsys, Teradyne EDA, and VLSI Technology/Compass Design Automation inserting scan chains automatically; and Expertest's capacity for creating test patterns for all digital logic almost make digital test a noninvasive operation.

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sections. Just as important, make sure you recheck your circuit's behavior with RC data extracted from the circuit layout.

Of course, one complaint of adding testability to designs is its impact on circuit performance. An effort is underway to help you quantify this impact. A number of vendors, including Genrad, Harris, Sierra, and Valid, are building macro-models of specific pieces of test equipment. Last year, Wavetek introduced its XTM integrated into the Digital Equipment Corp Real-Time Test Integrator—a comprehensive set of models that allows you to emulate a complete test setup. These models allow you to build and simulate a model of your circuit, connect it to the appropriate simulated test equipment, and measure its performance.

If you're looking for testability help from your silicon vendor, be aware that the vendor's expertise and interaction with your design efforts vary widely. At one extreme, Analog Devices takes your specification and returns a piece of silicon; they do the design and ensure its testability using many of the techniques discussed herein.

At the other extreme, Orbit Semiconductor doesn't provide design help. You are responsible for creating the design. Its testability is completely dependent on your skill, creativity, and expertise. Orbit provides you with process parameters that you incorporate into your models. The company offers fast (4- to 8-week turnaround), inexpensive (as low as $1500) foundry service, and they suggest that you prototype functional blocks within the design. During fabrication, the company monitors their process, so if a design fails, they can determine whether their fabrication was within specifications.

Many other companies, among them Gould AMI, NCR, and Sierra, assign and provide you with access to their applications and test engineers. These engineers generally have a good understanding of how their organizations test mixed-signal designs. Therefore, they can tell you what they need to test your circuits. They can often help you weigh the impact of testability on your design.

References

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Time-measurement instruments aren't restricted to counters and timers anymore. Analyzers that let you visualize long series of measurements can help you troubleshoot problems for which you would never dream of using a conventional counter.

Dan Strassberg, Associate Editor

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Units provide insights classic counters can’t

Time-interval analyzers (TIAs) and frequency and time-interval analyzers (or modulation-domain analyzers) make and store large numbers of measurements with little or no dead time between readings. They then present the measurements in numeric or graphics form, either statistically or in the original time-ordered sequence. Such products first appeared more than a decade ago, but only within the last four years have they been widely promoted. Although they may at first seem to be a cure for a nonexistent disease, the analyzers are, in fact, useful—so useful that many engineering departments, even some that don’t own conventional counters, should consider acquiring them.

A related type of product, the time-to-voltage converter (TVC) continuously converts short time intervals to voltage levels that you can monitor on an oscilloscope. The TVC concept is decades old. But, like time-interval analyzers, in the past TVCs were usually specialized devices. For example, some heart-rate monitors used in hospital intensive-care units are based on TVCs. Recently however, Tektronix introduced a TVC designed from the ground up as a general-purpose instrument. This TVC competes with TIAs and frequency-domain analyzers. At $2500, this unit is far and away the low-
est-priced continuous-measurement device (Table 1). It does need a scope for display and a power supply/enclosure, however.

Another instrument, which at first glance appears to be a conventional counter (in concept, if not in packaging), is actually quite unusual. The IBM PC-based GT-2210S Modulation/Time-Interval Analyzer from Guide Technology can make more than 2000 meaningful measurements per sec. This rate is as much as 200 times the maximum rate of classical counter/timers. So, although the Guide product doesn’t make continuous measurements, it makes enough measurements so that you can use it to track rapid changes in frequency or interval duration.

One difficulty that manufacturers of these products have is getting potential users to think about their measurement problems and the instruments’ capabili-

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What you see on the screen of this modulation-domain analyzer from HP is not a voltage ramp; it is the change in output frequency of a synthesizer simulating a step change in frequency as best it can.
ties in appropriate terms. To address that issue, Hewlett-Packard devised the concept of the modulation domain, represented pictorially as follows: Envision a space defined by three axes. Along the X axis is time; along Y is voltage; and along Z is frequency. An oscilloscope is a time-domain instrument; it measures voltage vs time. A spectrum analyzer—a frequency-domain instrument—measures voltage vs frequency. Many TIAs, including HP's frequency and time-interval analyzers, can measure frequency vs time. HP calls the frequency-time (X-Z) plane the modulation domain.

The idea of displaying frequency vs time bothers some people because frequency is defined in terms of time, and you can’t measure frequency in zero time. Even more vexing is the idea of measuring time intervals vs time. In fact, though, when you compare the values of the dependent variables these instruments record (intervals or waveform periods), with those of the independent variable (time), the de-

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**Table 1—Representative frequency and time-interval analyzers and time-to-voltage converters**

| Vendor/Instruments | Model | Maximum | Number of | Timebase stability | Maximum | Maximum | Time-ordered |
|--------------------|-------|---------|-----------|-------------------|---------|---------| readings stored |
|                    |       | frequency | inputs | standard | optional | readings | histogram | readings |
|                    |       | (standard/ | (ppm/ | (ppm/ | (ppm/ | (per sec) | bins | stored |
|                    |       | maximum) | month) | month) | month) | | | |
| Guide Technology  | GT2210S | 100 MHz | 1.3 GHz | 2/2 | 0.2 | 5 | 0.1 | 100 psec | 2300 | Via host-PC software | 30,000 (640k-byte PC) |
| Hewlett-Packard    | 53310A | 200 MHz | 2.5 GHz (see comment) | 2/3 | 0.3 | 8 | 0.005 | 125 psec | 2.5M | 450 | 8000 | 32,000 |
|                    | 5372A | 500 MHz | 2 GHz (see comment) | 2/3 | 0.0005 | 2 | Oven reference standard | None | 150 psec | 13.3M | 2000 | 8191 | N/A |
|                    | 5371A | 500 MHz | See comment | 2/2 | 0.0005 | 2 | Oven reference standard | None | 150 psec | 10M | 125 | 4096 | N/A |
| International Test Instruments | DTA8850 | 200 MHz sampled, 20 MHz direct | | | | | | |
| Odetics            | 2001A | 25 MHz | None | 3/3 | 1 ppm | 1 | None | As little as 50 psec | 1M in 2 sec; 10M in 6 sec | 130,000 | | Double standard memory |
|                    | 3100 | 100 MHz | None | 5/5 | 100/1°C | None | 1.4 nsec | 83k at 10-bit resolution | 1000 | N/A | N/A |
|                    | 4625 | 250 MHz | None | 2 data; 2 control gate; clock | 0.025°C | None | 150 psec | 1.3M at 12 bits | 4000 | N/A | N/A |
| CTime              | 2351 | 250 MHz | None | 2/2 | 0.5 | 0.01°C | None | 88 psec | 30M at 19 bits | 4000 | 16k | 64k (Fall '91) |
| Racal-Dana         | 2351EMD | 250 MHz | None | 2/2 | 1 | 10 | None | 5M with 200-psec resolution | Depends on software | 8191 | N/A |
| Stanford Research Systems | SR620 | 300 MHz | 25 MHz | 2/2 | 100 MHz built-in; 1.3 GHz (DP 901) | | | |
| Tektronix          | TVC 501 | 2.5 MHz | | 2/2 | 25 | 25 | None | 30 nsec | 2.5M | N/A | N/A | N/A |

**Notes:**
- N/A = Not applicable
- 1. All units from HP, International Test Instruments, and Odetics have built-in graphic displays. The others require external displays. The Stanford Research SR620 can operate as a stand-alone counter, however.
- 2. Allan variance: 2 x 10⁻¹² per sec.
- 3. Allan variance: 5 x 10⁻¹² per sec; temperature effects: 0.005 ppm from 0 to 50°C.
pendent-variable values are much smaller. Because of these scale differences, the instruments can legitimately plot frequency and time intervals vs time.

Time-interval analyzers had their beginnings in evaluation of spaceborne magnetic-tape data recorders. TIAs are still used extensively for testing of magnetic recording devices (for example, hard-disk drives). The first TIAs, made in the late 1970s by what was then the Kode Division of Odetics, did not maintain a time-ordered record of measurement results; they kept track only of statistical distributions. By keeping track of just the statistics, a TIA could store the results of many more measurements in much less memory at much lower cost than could an instrument that stored time-ordered measurement sequences. Moreover, the statistics provided all of the information the application demanded.

The nearly unrelenting downward spiral of memory prices has played a major role in the growing popularity of TIAs that retain time-ordered measurements. As you might expect, though, such instruments are not gaining acceptance simply because they have become practical. TIAs that store and display time-ordered measurements have many more potential applications than those that only present statistics.

But a time-ordered display is not essential for testing of magnetic recording devices. When testing a device such as a data tape recorder, you can predict its error rate from the width of the distribution of a large number of measurements of the time from a clock edge to the recovery of a 1 or a 0. If the recorder must maintain low error rates under demanding environmental conditions, you can predict its performance by monitoring how the time-interval distributions shift or widen as you vary the ambient temperature or as you subject the recorder to shock and vibration.

Another point in favor of statistical data recording is that by using it, a TIA can accumulate data for much longer than it can record in the time-ordered mode. When an instrument stores time-ordered readings, it places each reading in a separate memory location. So the analyzer must periodically stop recording to transfer its measurements to a host computer or a mass-storage device. The higher the acquisition rate, the sooner recording must stop.

To store data in histogram form, a TIA needs only one location for
Frequency and time-interval analyzers

each “bucket” or “bin.” Each time a measurement falls in a particular bin, the TIA increments the count in that bin. If the word length of the bins is great enough, a TIA in statistical mode can go on indefinitely making continuous or nearly continuous measurements.

Tektronix emphasizes that because its TVC doesn’t store readings, it can present time-ordered measurement sequences indefinitely. Although that statement is true, the scope on which you view the TVC’s output can display only limited numbers of measurements during its sweep interval; it will miss events that occur during its retrace interval. If you slow the sweep to accommodate more measurements, you will eventually miss transient phenomena of short duration.

Newer TIAs generally have extremely high maximum measurement rates: Odetics specifies its 4625 CTime at 30M measurements/sec, and Hewlett-Packard specifies its 5372A and 5373A at 13.3M. However, when time intervals occur in rapid succession as they do in a magnetic recorder, a TIA may not be able to make continuous measurements.

When the analyzer must leave gaps between measurements, a problem akin to aliasing in more conventional sampled-data systems can arise: the analyzer can lock onto measuring intervals of roughly equal duration and thus give an erroneously optimistic picture of the measurement distribution. To prevent this situation, some analyzers incorporate a randomizer, which de-

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lays the earliest start of successive measurements by a randomly distributed amount.

Word length not the whole story

Most modern TIAs (Odetics' are an exception) show their counter/timer heritage in their long word length. Like nearly all counter/timers, these instruments can make measurements with nominally very high resolution. However, word length is not a good measure of a time-measuring instrument's resolution—especially not its ability to time single-shot events.

Odetics' longest word-length TIA has a 19-bit word, whose least-significant bit is equivalent to 2 ppm of full scale—two counts in the least-significant digit of a 6-digit decimal number. To make up for this relatively short word length, the firm's TIAs have more measurement ranges than most others. Odetics' literature sometimes refers to these ranges as timebases; selecting a different timebase accomplishes much the same thing as changing the sweep speed (timebase) of an oscilloscope. Moreover, just like scopes with a delayed sweep, Odetics analyzers let you delay the start of an interval measurement after a trigger event. The delay can be much longer than the interval represented by a full-scale count.

Don't let the number of digits in a TIA's word length mislead you. When determining the instrument's resolution, the same considerations apply as for counter/timers. The uncertainty in an individual measurement is the result of a rather involved calculation based on various noise sources in the instrument. If

![Image of a TIA](image_url)

You can use a conventional scope to display how time intervals vary as a function of time. Tektronix's TVC 501 time-to-voltage converter makes such displays possible. The small module is part of the firm's TM 500 family.

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you insist on a single number to express the repeatability of a time-measurement instrument's readings, look at the jitter spec. However, you ought to carefully read all of the footnotes in the data sheet and learn how to calculate the uncertainty of real measurements.

The best jitter spec quoted for any instrument in Table 1 is 25 psec, for Stanford Research Systems SR620 counter/timer. (Though the SR620 is not a TIA, it is included because of its built-in ability to produce histograms.)

In fact, jitter in TIA readings can often be more significant than jitter in measurements you make with a counter/timer. The reason is that if a counter/timer's readings aren't repeatable enough, you can usually improve the situation by asking the instrument to average a large number of readings. With a TIA, the variations among readings often represent exactly what you are trying to measure. You'd really like the TIA's own uncertainty to be insignificant compared with the variations attributable to the system under test.

In the eye of the beholder

A TIA's method of presenting its acquired data is an important aspect of its operation. Analyzers from HP, International Test Instruments (ITI), and Odetics are stand-alone instruments that don't require additional equipment. These units incorporate displays—CRTs in the HP products, an electroluminescent (EL) panel in the ITI product, and, depending on the model, either a CRT or an EL panel in the Odetics products. The displays can present data in graphical and numeric form. The stand-alone analyzers can also send data to a host computer via IEEE-488 interfaces, RS-232C ports, or both. The ITI unit offers an additional benefit; you can use the instrument as an 80286-based PC.

The other products require external displays. The Tektronix TVC works with any scope. The Guide Technology unit, which is based on an IBM PC bus I/O board, uses the computer's display. The Racal Dana units are C-size plug-ins for the VXIbus; they use the host computer's display. The Stanford Research unit is a stand-alone counter. It can send its graphics output to a scope, a plotter, or a chart recorder. You need such an external device to take advantage of the instrument's TIA-like qualities,
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though you need no external equipment to use it as a counter.

TIAs, particularly those with a time-ordered presentation, are wonderful general-purpose instruments. Several vendors have compiled stacks of application notes describing the diverse ways in which you can use these products. For example, HP has a 2-in.-thick stack of more than two dozen notes covering applications in fields as varied as disk-drive testing; development of secure-communications, cellular-radio and radar systems; and design of motion-control systems. Tektronix publishes a book (Ref 1) that describes more than a score of uses for its TVC, including several in embedded-system debugging.

TIAs in embedded-system debug

Space limitations don't permit detailed descriptions of many of these applications. Tektronix's embedded-system debugging examples, however, show that the ways in which you can use a TIA are limited mainly by your imagination. As you might expect from the supplier of an instrument that produces a time-ordered display, Tektronix has chosen examples that emphasize the value of such a presentation over a statistical one.

A problem frequently encountered in embedded real-time systems is unpredictable interrupt response time, or interrupt latency. There are many ways to look at interrupt latency, but a TVC or a TIA that produces a time-ordered display allows you to quickly see how interrupt latency varies with time. The instrument measures the time from the falling edge of the processor's interrupt-request (IRQ) line to the appearance on the address bus of the starting address of the interrupt-service routine. A word-recognizer probe generates a trigger when it senses the desired address.

(For even greater rigor, you can further qualify the address with the trailing edge of the memory-read strobe.)

If the interrupt latency sometimes exceeds specifications, you can try to correlate the failures with such events as the line-voltage zero crossing. In this example, you can display the line voltage on an unused scope channel.

Time-interval analyzers and modulation-domain analyzers will ultimately change the way engineers view the measurement of frequency and time. In this ever more digital world, frequency and time are growing in importance as measures of system performance. In an increasingly fast-paced environment, these variables are not static. In a sense, conventional counters and timers have failed to keep pace with the dynamic nature of the quantities they measure. Instruments of the types discussed here have corrected that anachronism. In the months and years ahead, you can expect new and intensified competition among vendors of these units. With it, not surprisingly, will come higher performance and lower prices.

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Given enough time and the right motivation, most engineers can learn to use the Ada programming language on their own. However, a training class will hasten language proficiency.

Steven H Leibson, Senior Regional Editor

LEARNING ADA

Class provides fast track to understanding

If you work on military projects for the Department of Defense, your time has just run out. The US government's fiscal year 1991 budget states that "After June 1, 1991, where cost effective, all Department of Defense software shall be written in the programming language Ada." Thus, you must now prove that another language would be cheaper to use if you wish to avoid using Ada for a military programming project.

Ada's features suit the language for complex programming projects, but its reputation of being hard to learn discourages many engineers from learning it. To find out just how hard learning Ada really is, I attended a 5-day real-time Ada programming class at Alsys in Burlington, MA. (Alsys is not the only compiler vendor to offer classes in Ada programming. I selected this class because its timing suited my needs.) I discovered that learning Ada as a second language isn't as tough as people say. Although Ada is a complex language, it isn't impossibly difficult to learn. In fact, the language actually eases the job of writing programs for multitasking systems.

Although I'd never programmed in Ada before, I have assimilated many other programming languages including Algol 68 (a structured language and a predecessor of Ada that nearly drove me away from computers forever), Basic, HPL (a proprietary Hewlett-Packard programming language for desktop computers), and several microprocessor assembly languages. My familiarity with these programming languages matches the experiences of many engineers who know the general concepts of computer programming but lack specific Ada knowledge.

Dr Benjamin M Brosgol taught the class. His 3-part series on real-time Ada programming appeared in EDN last year (Refs 1, 2, and 3). He was a member of one of the four teams that competed on the original Ada specification.
Learning Ada

unit comprises two parts. The first part, the optional “specification,” declares the elements of the program unit that are visible to other units. The second part is the body code.

Divide and conquer

Ada's definition requires that an Ada compiler be able to compile a program unit consisting of just a specification. Thus, you can write a specification for a program unit in Ada, compile it so that other subprograms can use it, and postpone implementing that module until a later time. You can then write and compile the code that performs the subprogram's real work separately.

This compartmentalization lets you conceal a subprogram's implementation, its “body,” from the other subprograms. This characteristic thus limits the number of details a programmer must remember at any one time by severely restricting access to and from other parts of the program. Restricted access also prevents the conflicting reuse of variables and procedure names—a problem that frequently occurs on projects with a large number of programmers.

In fact, you can separately compile all Ada program units. As a consequence of this feature, Ada compilers include library managers that keep track of the numerous program units, variables (which Ada calls objects), and procedure names that make up a complete program.

Fig 1 gives you a glimpse of the complexity you can expect from even small programs. Ada programs don't have to be so complex. Fig 2 demonstrates that an Ada program can be as short as five lines.

I found the idea of a program comprising tens or hundreds of program units somewhat daunting. All the languages I know well don't allow separate compilation, so this concept was somewhat new to me. As I grew more familiar with Ada, I became accustomed to this programming style and now understand why many vendors stress the abilities of their products' library-management tools. Such tools are essential if you want to take full advantage of Ada's features.

From generalities, the class moved on to the specifics of writing an Ada program. As a first step, you declare all the objects you plan to use. You can declare objects in both the specification and the body of a program. Because Ada has strong typing and constraint checking, you must declare all objects before you use them. Other subprograms can use the objects you declare in the specification unless you declare those objects private. If you declare an object in a subprogram's body, it is private to that unit.
When you declare an object, you must also declare its “type.” For example, if you are going to use an object called DAY to hold the day of the month in your program, you might declare DAY to be an integer. However, the day of the month can never be negative, and if DAY somehow became negative during your program’s execution, that situation would constitute an error. Instead, declare DAY as a “positive,” which is a predefined subset of the integer type that includes the set of integers greater than zero.

Using constraint

To make full use of Ada’s error-checking abilities, you could use Ada’s user-defined subtype declaration to further limit DAY’s value to the integers 1 through 31 inclusive. If you defined DAY as such a subtype, then every time you assigned a value to DAY, Ada would check to make sure that the assigned value fell within the limits of that object’s definition. This continual constraint checking is one of the strongest of Ada’s type-checking abilities because it enhances a program’s reliability.

Further, you cannot use sleazy programming tricks, such as assigning the value of a floating-point number to an integer type, because Ada doesn’t allow such shenanigans. Other languages may allow such “cheating” and their programming styles may sometimes produce more-efficient-looking code, but such languages exact a penalty from anyone trying to maintain your program.

Ada provides explicit ways to convert a floating-point number to an integer. Because the conversion must be explicit, anyone reading your program will be able to see what you are doing. Remember, Ada’s designers were building a language for large projects and big programming teams. They always opted for stylistic clarity and shunned obscurity.

For the remainder of the first day’s lessons, we looked at simple Ada statements such as assignments, if statements, case statements, and loop structures. We also studied the two types of subprograms: functions and procedures. Functions return an explicit value. Procedures do not return a value to the caller but may indirectly return values by changing the value of global objects.

As part of its emphasis on constrained programming, Ada also places limitations on subprograms’ parameters. Parameter modes help you limit vulnerability to inadvertent modification. You can define the mode of a passed parameter as in, out, or in out. A subprogram can read the value of an in parameter but cannot change that parameter’s value. A subprogram can change the value of an out parameter but cannot read its value. And a subprogram can both read and change a parameter you define as in out.

Struggling through day one

I was overwhelmed by the time the instructor turned us loose on our PCs for the first day’s workshop problems. The concepts I had to simultaneously assimilate included Ada terminology, the quirky syntax, several unfamiliar program and data structures, and the language’s stylistic philosophy. I was also learning to use Ada tools, including an editor, verifier, compiler, binder (a linker and librarian rolled into one tool), and a debugger.

Had I realized the sheer volume of information I would need to assimilate that first day of class, I might have studied Ada before class started. The text for the course (Ref 4) would have been a helpful study aid. Of course, if I had the time to read that book, I might not have felt the need to take the course in the first place.

The second day of class was less of a struggle. I began to recognize proper Ada syntax and found reading program listings easier. We started the day by looking at “generics,” Ada’s rough equivalent to programming macros. Generics are templates for creating subprograms. One example of a useful Ada generic is the sort routine.

Suppose you develop an efficient algorithm to sort objects. Instead of writing separate subprograms to sort lists of integers, fixed-point numbers, floating-point numbers, and strings, you can write one generic for that algorithm that sorts objects of an unspecified type. Later, you can specify the object type to be sorted when you instantiate the generic. This Ada feature helps you reuse the code you write.

Next, we studied complex objects: arrays and records. Arrays are homogeneous collections of objects; records are collections of heterogeneous objects. Most programming languages have similar kinds of data structures. Ada allows “dis-
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criminated” records that have variable fields. You can use a record’s discriminator field to determine the number and types of fields in the rest of the record (Fig 3). This feature is a great way to efficiently organize the memory a program uses for records.

Ada’s access types may seem somewhat foreign unless you’re familiar with the C programming language’s pointers. Access types point to objects and thus contain the address of the object to which they point. However, you generally don’t use access types to work directly with machine addresses. Instead, you use an access type to manipulate an object’s component parts by tacking the object’s component names onto the access-type designator.

An example helps clear up the confusing terminology and illustrate the reasons for using access types. Suppose you declare a designator REF as an access type for record R, which has two components: objects VALUE and NEXT. The VALUE component holds a numeric value; NEXT holds a pointer to the next record. If you want to manipulate a linked list of these records using many different Ada subprograms, you could have problems.

Without access types, Ada’s scoping rules (the rules that define which objects a subprogram can use) might cause the Ada runtime system to pass the entire linked list to each relevant subprogram. That operation would create a new copy of the set of records somewhere in memory for every subprogram that uses the records in the list. If the objects you’re working with are large, multiple copies could cause your system to run out of memory and abort the program.

An access designator such as REF lets the subprogram manipulate the original set of objects or, in this case, records. Using Ada’s “dot notation,” the subprogram can manipulate a record’s value component using the designation REF.VALUE. The subprogram finds the next record on the list by reading REF.NEXT.

Note that this scheme preserves Ada’s type-checking feature because REF.VALUE has the same type as VALUE, and REF.NEXT is the same type as NEXT. Access types for complex objects can get pretty involved, and I can’t say that I fully understand them yet, but the class certainly gave me a good start on the subject.

I hit a brick wall during the discussion of recursion in Ada not because of Ada but because I’m just not conversant enough with the basic concepts of recursion. As another class member said, “My mind doesn’t work that way.” I did learn enough to know that if I ever figure out how to effectively use recursion in any programming language, I’ll be able to use Ada to write recursive programs.

At the end of the day’s lecture, we studied storage management, because access types make allocating memory difficult for the runtime system. Temporary objects exist only as long as the tasks using them exist. If you use access types to reference temporary objects, the runtime system may not be able to determine when you no longer need those objects and therefore might be unable to reclaim the memory the objects use. You can explicitly reclaim that memory by using Ada’s “unchecked deallocation” feature. Through unchecked deallocation,
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you can explicitly force the Ada runtime executive to delete an object from memory.
I found the second day's workshop problems on discriminated records and unchecked deallocation to be fairly easy. I skipped the problems that demonstrated recursion.

Making exceptions

We started the third day of class by looking at exception handling. An Ada runtime system can raise several exceptions while your program is running. For example, if an assignment statement attempts to assign an improper value to an object, that operation will cause the runtime system to raise an exception. If you do not write an exception-handling routine for that exception, your program will halt.

Halting may not cause many problems for a program running on a PC or workstation—you can always restart the program. But real-time, embedded programs generally can't afford to halt because some sort of physical damage may result. If your Ada program is managing control surfaces on an aircraft, you don't want that program to halt on its own.

You can generate user-defined exceptions from within a program by using Ada's raise statement. The raise statement causes program execution to jump to the named exception-handling routine. You should not use the raise statement for normal program branching, however, because the program cannot return to the point at which the exception was raised. Exceptions in Ada are just that: exceptional situations. You should use them only when you need to abort one instruction sequence and immediately start another.

The instructor also discussed "exception etiquette," which included tips that help programs stay operational even when exceptions occur.

For example, if a hardware failure or storage exception occurs, your exception handler should close all open files and reclaim storage for objects no longer needed before relinquishing program control. The handler is likely to be closer to the scope of the routine that caused the exception than the subprogram that executes when the exception handler finishes its job would be. Thus, the handler should try to clean things up as much as possible. Helpful hints such as this one differentiate the quality of knowledge you can get in a class from what you can read on your own.

After a more involved look at generics, we moved on to the real-time aspects of Ada. We started with tasks. Until this point, the programs we discussed in class and worked on in workshops were sequential programs. The programs were therefore typical of programs written in nearly any high-level programming language.

One feature that differentiates Ada from many other languages is its inherent parallelism. By labeling a procedure as a task, you tell the compiler that the runtime system can run that procedure concurrently with other tasks on one processor or on multiple processors, if they're available. The ability to run subprograms concurrently resides in the Ada runtime executive supplied with the compiler.

If you're already familiar with multitasking environments, you know that one of the biggest problems to solve in multitasking systems is how to prevent the simultaneous use of shared objects. For example, the CRT screen is an object. If you have two concurrent tasks trying to print characters to the screen at the same time, what actually appears on the screen could be some jumbled mixture of the two character streams.

When using languages not specifically designed to handle concurrent task operation, you will usually create a semaphore to control access to shared objects. Ada has a built-in mechanism called the "rendezvous" to ensure mutually exclusive use of shared objects. The rendezvous uses a simple mechanism to ensure mutual exclusion: It allows only one caller to be served at a time. The server serves all other calling tasks one at a time on a first-come, first-served basis.

A rendezvous is an asymmetric arrangement between the calling and called tasks. The calling (or client) tasks issue a call to the task with which they wish to rendezvous. The called (or server) task has an accept statement that creates an "entry" for the clients. If the client task issues a call before the server task executes its accept statement, the Ada runtime executive suspends the caller until the rendezvous occurs. Similarly, if the server task executes an accept statement first, the runtime executive suspends the server until a client issues a call. Note that accept statements are not caller specific, whereas clients issue server-specific calls.

When at least one client and the server are ready, the rendezvous occurs. A rendezvous situation in which multiple clients call one server causes an implicit semaphore. The semaphore occurs because the server accepts only one call at a time and will not service another client until the server executes another accept statement.

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the server task alone can manipulate a protected object, then all other subprograms (and programmers) must observe the implicit semaphore of the rendezvous. Misused semaphores, a problem in many multitasking programs, are thus rare when using Ada.

The rendezvous does have one potential drawback: execution speed. Depending on the compiler, the µP, and the clock rate, a rendezvous may take tens or hundreds of microseconds to execute—even when both the client and server tasks are ready. A compiler vendor can tell you how long a rendezvous call takes using that company's compiler and a particular hardware configuration. You must then decide if your application can afford that much time. For many real-time applications, even a 100-µsec rendezvous isn't too long. However, some applications can't afford to waste that amount of time.

We investigated Ada tasks during the third day's workshop problems. One problem created two tasks that sent characters to the PC's screen simultaneously. Without using a rendezvous to protect the screen, we did indeed observe jumbled output. By adding a screen-server task to provide mutual exclusion for other tasks, we produced more orderly behavior. Despite Ada's reputation as a verbose language, I found that I could create programs that demonstrated complex Ada concepts with a page or two of code. For example, the three program units for the screen-printing task appear in Fig 4.

On the fourth day, the instructor discussed more-advanced methods for using tasks. For example, conditional, or "guarded," accept statements let you control which rendezvous calls a server task will accept. For example, a guarded accept statement might be available for rendezvous calls only if parameter x equals zero. Server tasks can have multiple accept statements, and you can guard all or just some of them.

When executing, your program will evaluate the guarded statements first and then ignore all accept statements with closed guards.

(a) package LINE_PCKG is
   procedure PUT_UC_LINE (ITEM: in STRING);
   procedure PUT_LC_LINE (ITEM: in STRING);
end LINE_PCKG;

(b) with TEXT_IO;
   use TEXT_IO;
   package body LINE_PCKG is
      task body MONITOR is
         entry PUT_LC_LINE(ITEM: in STRING);
         entry PUT_UC_LINE (ITEM: in STRING);
      end MONITOR;
      task body MONITOR is
         MAX_LENGTH: constant := 80;
         LINE: STRING(MAX_LENGTH);
         INDEX: NATURAL;
         CHAR_CODE, UC_CHAR_CODE, LC_CHAR_CODE: NATURAL;
         procedure MOVE (FROM: in STRING; TO: out STRING; LAST: out NATURAL) is
            LINE: STRING(MAX_LENGTH);
            INDEX: NATURAL;
            for I in 1..200 loop
               if LINE (I) not in 'A'..'Z' then
                  LINE (I) := CHAR_CODE (CHAR_CODE 'POS (LINE (I)));
               end if;
               LAST := LOCAL_LAST;
            end loop;
         end MOVE;
      begin loop
         select
            accept PUT_UC_LINE(ITEM: in STRING) do
               null;
            end PUT_UC_LINE;
            accept PUT_LC_LINE (ITEM: in STRING) do
               null;
            end PUT_LC_LINE;
            for I in LINE'FIRST..INDEX loop
               if LINE (I) not in 'A'..'Z' then
                  LINE (I) := CHAR_CODE (CHAR_CODE 'POS (LINE (I)));
               end if;
            end loop;
         end if;
         end loop;
      end if;
   end MONITOR;

(c) with LINE_PCKG;
   use LINE_PCKG;
   procedure SYNMON is
      task body T1 is
         task body T2 is
         accept PUT_UC_LINE(ITEM: in STRING) do
            null;
         end PUT_UC_LINE;
         accept PUT_LC_LINE (ITEM: in STRING) do
            null;
         end PUT_LC_LINE;
      end SYNMON;

Fig 4—A server task can provide mutually exclusive access to protected objects. The task MONITOR prevents the lines of characters that tasks T1 and T2 generate from intermixing on a display screen.
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The remaining open-guarded and unguarded accept statements are available for rendezvous calls. After one such rendezvous is accepted and completed, the program will reevaluate the guards.

When writing the code for a server task, you need to take care to minimize the amount of suspension time for the calling tasks. You can place a server task's code within the rendezvous, where it is protected, or outside the rendezvous. Placing as much of the server task's code outside the rendezvous as possible minimizes the duration of the rendezvous and thus reduces the amount of time the calling task will be suspended.

Complex structures such as rendezvous calls make Ada seem very much removed from the underlying hardware, but the language also has features that let you directly manipulate the hardware. For example, representation clauses let you specify how the compiler should organize objects at the bit level. If you need to specify the addresses and the exact bit-by-bit definition of a peripheral chip's control and status registers, you use representation clauses.

The fifth and last day of class focused on more hardware-related issues. Ada lets you link hardware interrupts to tasks. The interrupt works like a call to a server task from a client task, but has higher priority than any other Ada task. Because Ada is a high-level language, you may not find Ada-level routines to be the best solution for servicing interrupts, but the facility exists. Ada compilers from different vendors handle interrupts differently, so you need to study the technical specifications to discover how each compiler handles interrupts.

Because Ada handles interrupts as if they were task-entry calls, you can test interrupt-handling tasks without using hardware interrupts. Another task can just as easily rendezvous with the interrupt-handler's entry. You may find this feature handy for testing your interrupt code before you have target hardware or if you do not have enough hardware test beds for all of your programmers.

You can also use interrupts to simulate interrupt situations that may be too difficult or dangerous to test otherwise. For example, if you want to see how your reactor-control software responds to a coolant-leak interrupt, you probably won't want to actually create such a leak for your test during the early stages of software development.

We spent most of the last day discussing rate-monotonic scheduling theory. (Ref 5). This theory, most recently developed by Lui Sha at the Software Engineering Institute (Pittsburgh, PA), lets you create a multitasking system that always meets hard periodic deadlines.

Essentially, rate-monotonic scheduling theory states that if your multitasking system has enough CPU cycles to service all periodic requests, you can assure that the system services all the requests in the time required by assigning the highest priority to the task with the shortest period and the lowest priority to the task with the longest period. Tasks with intermediate periods receive intermediate priorities inversely proportional to their periods.

The discussion of rate-monotonic scheduling concluded the real-time Ada course. Five days of immersion in the language have not made me an expert Ada programmer. However, I did not attend this class to become an expert on Ada's syntax. Instead, I wanted to know why the language incorporated some of its unique features and how to best exploit these features in real-time systems. I now have an excellent foundation to further develop my Ada programming skills.

References

Acknowledgment
For more information about this class, contact Alsys Inc at 67 S Bedford St, Burlington, MA 01803, phone (617) 270-0030, FAX (617) 270-6882.

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The vendor's claim that each member of the tool suite uses the same "simulator engine" is misleading. Each tool uses its own independent event queue and algorithm to perform logic, timing, and fault analysis. Where the tools do converge is in reading the same netlist, eliminating the need for translating data between tools.

The results-file output from the timing analyzer, like the other tools, is also linked to the front-end schematic-capture tools. Rather than sorting through a mountain of confusing error or timing-violation logs, the timing analyzer gives you the option of highlighting errors within your schematic, though this option doesn't extend to VHDL source code. This graphical capability aids debugging. You can also sort the violations by time of occurrence, error type (setup, hold time, pulse width), signal name, or path name.

The simulation suite offers 140 ASIC-vendor-supplied design libraries whose models include all the information for timing analysis. Within Rapidtime, you can scale the timing data in the models to experiment with different design margins. You can also use the LM1000 hardware-modeling system within the simulation runs.

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Modular switching power supply develops an 1100A output

Housed in a package measuring 5 x 8 x 16 in., LFS-52 Series switching power supplies range to 1100A. The units employ a modular design consisting of three full-bridge circuits that switch at 100 kHz. A 1.22-MHz crystal oscillator provides the logic-level timing signals that switch the three modules 120° out of phase. The series includes three models—the LFS-52-2, which has an output of 1.8 to 3.3V at 1100A, the LFS-52-5, which has an output of 4.5 to 6V at 1000A, and the LFS-52-8, which has 5.5 to 8V at 800A output. These output values equate to a power density of 10W/in³.

Each of the modules in the LFS-52 series supplies is wired in a redundant configuration. If one driver fails, the supply will continue to deliver two-thirds of its rated output power indefinitely. To further ensure full internal redundancy, each module has separate fuses; these fuses guarantee that any defective module will be invisible to the remaining modules. The 2V models have a guaranteed minimum efficiency of 70%; minimum efficiency figures for the 5 and 8V models are 75 and 80%, respectively.

Control circuitry in the supplies is referenced to the secondary side of the supply. This design removes the isolation boundary from the feedback loop. The supplies employ an average-current control scheme, allowing for accurate load sharing from supply to supply. A transformer-coupled gate-drive scheme switches the high-power MOSFETs that are incorporated in the inverter modules. Supply input is 3-phase and does not require bulk-storage capacitors. As a result, the units have a 0.9 minimum power factor.

The supplies feature a 2-stage differential filter on the output. Individual module output choke feed into a common capacitor assembly and through a second-stage filter. To address common-mode considerations, the supplies include free-standing input-rectifier and inverter-switch heat sinks to minimize capacitance-to-chassis figures. A shield located between the primary and secondary windings of the main transformer has a low-inductive connection to the input film capacitors, which shorts out the primary-to-secondary interwinding capacitance. The first-stage output-filter choking are located on the negative leg of the output bus structure. This design holds the output bus assembly at a fixed potential relative to ground, thus keeping secondary-to-chassis currents to a minimum.

Supply-line regulation equals 0.1% for line variations of 170 to 265V ac. Load regulation measures 0.1% for 0-to-100% load variations. Transient response time equals 4 msec, and thermal coefficient is 0.03%/°C. The units feature an airflow sensor that provides thermal protection in the event of inadequate air velocity. Fixed-electronic-current limiting clamps output current to 107% of 40°C rated current. Overvoltage protection is standard on all units. When the preset voltage level is exceeded, the protection circuitry removes the inverter drive. A dc-power-good indicator LED goes off to indicate that a power failure has occurred. The LFS-52 Series is priced from $2800.—Tom Ormond

Lambda Electronics Inc, 515 Broad Hollow Rd, Melville, NY 11747. Phone (516) 694-4200. FAX (516) 293-0519.

Circle No. 730
NEW TRANSFORMERS FOR CLASS 2 APPLICATIONS.

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MAXIMUM FUSE VALUE SPECIFIED
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Signal "The American Original" introduces a new family of transformers for 2.5 to 80 VA applications that require low power and a high degree of isolation. These new "Class 2" transformers feature the same dual high-temperature bobbin construction and insulating shroud originally developed for the company's very successful International Series. Available in both PC and chassis mount versions, they offer a choice of inherently limited or non-inherently limited designs and feature 4000 VRMS primary and secondary isolation.

Signal's insulation system results in very high isolation between the primary and the secondary windings, and between either winding and the core. The dual bobbin design reduces capacitance and eliminates the need for an electrostatic shield. The Class 2 dual bobbin series satisfies UL 1585 requirements and CSA safety and performance standards.

Signal transformers are available through Signal's PRONTO 24-Hour Off-the-Shelf shipment program. For additional technical data, contact Signal Transformer, 500 Bayview Avenue, Inwood, N.Y. 11696.

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68030-based VXIbus controller offers real-time, distributed operation

The VXIcpu-030 C-size 68030-based board comes with VXI and IEEE-488 drivers and an integrated Ethernet connector; it's suitable for real-time embedded applications that require VXIbus control. Using this Slot-0 controller board, you can build distributed VXIbus systems that network VXIbus mainframes with workstations, PCs, file servers, and terminals. This single-slot board gives you direct control of VXIbus registers, memory, interrupts, and triggers. You can also configure the board for non-Slot-0 operation.

A SCSI port, an IEEE-488 connector, and two serial ports are standard features on the board. Options include eight additional serial ports, an internal hard-disk drive, and a 68882 floating-point coprocessor. The heart of the controller is a Motorola MVME147 single-board VME computer with a 25-MHz 68030 µP. You can populate the MVME147 with as much as 16M bytes of RAM and 4M bytes of ROM.

The controller is also a fully functioning VXI message-based commander with complete Resource-Manager capability and direct access to all VXI address spaces. You can use it to perform 8-, 16-, and 32-bit data transfers. Onboard RAM is dual-ported to the VXIbus for direct shared-memory communication.

Wind River Systems sells a version of its Vxworks real-time operating system that has been optimized for use with the controller. Using its built-in X-Window server facilities, this operating system lets you use a Unix workstation or a PC as a high-level software development platform; the platform generates real-time code that executes on the controller's target processor.

Development tools that come with Vxworks include libraries for both VXIbus and IEEE-488 instrument control. The VXI driver software includes a resource manager; functions for word serial communications; direct access to the VXI bus; interrupt and signal handling; and trigger handling.

You can edit, compile, link, and debug your real-time application software on your Unix host computer via a local terminal on the controller itself. By downloading portions of your application code to the embedded processor, you can interactively set breakpoints to trace program execution. This software also lets you examine variables, memory, and register locations.

Pricing for the controller board begins at $5995 for a base unit with 2M bytes of RAM. You'll pay an additional $1595 for National Instruments' software-development libraries and $400 for a runtime license. The Vxworks development system for the controller board sells for $20,000; its runtime license costs $600.—JD Mosley

National Instruments, 6504 Bridge Point Pkwy, Austin, TX 78730. Phone in US and Canada, (800) 433-3488; in TX, (512) 794-0100. FAX (512) 794-8411.

Circle No. 733

Wind River Systems Inc, 1010 Atlantic Ave, Alameda, CA 94501. Phone (800) 545-9463; in CA, (415) 748-4100. FAX (415) 814-2011.

Circle No. 734
**Hardware/Software VME SPECTACULAR**

**R3000 SINGLE BOARD COMPUTER**
- 25MHz MIPS R3000 CPU
- 25MHz R3010 PPC
- (4) 25MHz R3020 write buffers
- 128KB (or 32KB) cache
- 25MHz R3020 CPU
- (4) 25MHz PC buffers
- (1) RS232C serial port
- (4) 28-pin EPROM sockets

**SINGLE BOARD COMPUTER**
- 68040 25-33MHz CPU
- (8) 28-pin SRAM sockets (up to 256KB)
- (8) 32-pin ROM sockets (up to 8MB)
- (2) RS232C serial ports
- (16) lines of parallel I/O
- (1) OMNIMODULE socket
- VIC068 VME Controller

**SINGLE BOARD COMPUTER**
- 68020 16.66-33MHz CPU
- (8) 28-pin SRAM sockets (up to 256KB)
- (8) 28-pin ROM sockets (up to 8MB)
- (2) RS232C serial ports
- (16) lines not parallel I/O
- (1) OMNIMODULE socket
- VIC068 VME Controller

**SINGLE BOARD COMPUTER**
- 68000 12.5-16MHz CPU
- 512KB DRAM
- (4) 28-pin ROM sockets
- (3) 16-bit counter/timers
- (2) OMNIMODULE I/O sockets
- DMA controller (optional)
- Optional interrupt generator
- Optional 4 level bus arbiter

**SINGLE BOARD COMPUTER**
- 68000 12.5-16MHz CPU
- (8) pairs of 28-pin sockets for RAM or ROM
- (2) RS232C serial ports
- (2) 8-bit parallel I/O ports
- System controller

**UNIVERSAL I/O BOARD**
- (4) OMNIMODULE I/O sockets for a wide variety of I/O (i.e. 8 serial ports, 80 parallel lines)
- One (1) interrupt per OMNIMODULE (2 optional)

**AVAILABLE SOFTWARE**

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In IL 708-231-6880
CIRCLE NO. 119
PRODUCT UPDATE

SBus-based DSP board performs 33M flops

The TMS320C30-based Spirit-30 DSP board adds 33M-flops math performance to SBus-based computers from Sun Microsystems and other manufacturers. You can use the board in applications such as image processing, communications, and vibration analysis. The board can transfer data to or from the host computer as fast as 25M bytes/sec and can interrupt the host via any one of the seven SBus interrupts.

An SBus-based host computer can reset, interrupt, enable, disable, and read status information from the Spirit-30. The board can accommodate 256k to 2M bytes of zero-wait-state static RAM that is mapped into the host computer's address space. An additional 32k bytes of static RAM connect directly to the expansion bus of the TMS320C30. You can use this private memory to store frequently accessed coefficients.

Dual proprietary parallel ports interface the math board to additional memory and peripheral devices. The first port, dubbed ASM-Peripheral Port, supports 32M-byte/sec transfer rates to data-acquisition devices such as frame grabbers. The second port, the ASM-Main Port, transfers data as fast as 66M bytes/sec. You can use the ASM-Main Port to expand memory to 64M bytes and to link multiple boards in a daisy-chain fashion.

The board also includes two serial ports that can operate as fast as 8M bits/sec. You can connect standard RS-232C devices to the ports. And, the company can supply a number of data-acquisition modules that connect via the serial ports. You can choose from modules with 12- to 16-bit resolution and sampling rates ranging from 8 to 400 kHz. The board also offers compatibility with the industry-standard DT-Connect expansion bus.

You can choose from an array of software-development tools for the board, including an optimizing ANSI-C compiler, assembler, and linker. The company also offers a C-language source-level debugger, a simulator, and a DSPL library of DSP algorithms. You can buy the Spox OS real-time operating system for the board.

A Spirit-30 board configured with 256k bytes of static RAM costs $3995. The SBus board is compatible with Spirit-30 products for other types of computers, such as IBM-compatible PCs. You can port software to any of the boards by recompiling and relinking the source code.—Maury Wright


Image-processing, vibration-analysis, radar, and other DSP application programs execute at 33M flops on Sun SPARCstations and other SBus-based systems equipped with a Spirit-30 board.
The comPAC™ family of high-density DC-input power systems is designed to keep your system running while shrugging off the sags, surges and transients that your input source hands out. So, if meeting Bellcore, British Telecom or IEC standards for input voltage and transient protection is your problem, in applications from 50 to 600 Watts, comPAC is your solution. And comPAC doesn’t talk back . . . it meets Bellcore, British Telecom and FCC/NDE specifications for EMI/RFI.

The low profile package . . . only .99" tall . . . is standard, as is extended input overvoltage capability and reverse polarity protection, output overvoltage and overcurrent protection, trim capability on all outputs, and a master disable. And, every comPAC benefits from the high efficiency and inherently high reliability of our VI-200 family of component-level power converters. So, just tell us what you want . . . 24, 48 or 300 VDC in . . . 1, 2 or 3 outputs, from 2 to 95 Volts . . . output power ratings to 600 Watts . . . we’ll do the rest.

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Fast screen updates

NEC's 80-ns RAM port access speed and fast page operation enable fast frame buffer updates. Block Write and Flash Write fine tune your design by clearing your windows or your full screen, fast. A Split Data Register function simplifies Real Time Data Transfers with relaxed timing.

All standard JEDEC features on our 256K video RAMs are present in our 1 megabit generation. This includes the Maskable Write Function that allows updates of specific bits and eliminates the need for Read Modify Write cycles. The Persistent Write Per Bit feature on the 128K x 8 version realizes compatibility with popular graphics processors.

Intelligent choices

Optimize your frame buffer architecture with the right video RAM configuration. NEC delivers dual port video RAMs at both 256K and 1 megabit densities. Choose from two 1 megabit configurations: 256K x 4 and 128K x 8. Our worldwide manufacturing expertise assures stable supply with the quality you demand.

Call NEC today for high-performance video RAMs—the elegant solution for your sophisticated graphics design.

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<th>Part Number</th>
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Major Characteristics

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### LEADTIME INDEX

Percentage of respondents

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<th>ITEM</th>
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<th>6-10 weeks</th>
<th>11-20 weeks</th>
<th>Over 30 weeks</th>
<th>Last month's average</th>
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**Source:** Electronics Purchasing Magazine's survey of buyers.
Data Acquisition & Control

NEW

TE-158 Telephone Control Card:
Take total control over your telephone communication. Direct telephone line interface gives you control over line connect/disconnect, touch-tone decoding and encoding, and detects call progress. Set your computer to dial out automatically, to keep trying if busy signal, control voice synthesizer, tape recorder with complete in/out capability. FCC approved.

TE-158: $190.00

Relay Card:
8 individually controlled industrial relays. 3A at 120VAC, SPST.
RE-140: $142
8 Bit A to D:
8 Analog inputs, 0-5V.20mV steps. 7500 readings/sec.
AD-142: $142

Temperature Sensor:
Range 0-200°F. 10mV/°C Resolution with AD-142.
TS-111: $12

Digital Input:
8 opto-isolated inputs. Read voltage presence or switch closures.
IN-141: $65

If you have a technical problem, call us!
After 15 years in data acquisition and control, we've come to know a little. We've answered thousands of questions from customers. We'll be happy to answer yours, too. Call our FREE Technical Advice Department at (203) 656-1806, or fax us your question at (203) 656-0756. Let's hear from you!
Kevin Tschudi Engineer, Alpha Products

Latched Digital Input:
8 opto-isolated inputs. Each input individually latched to catch switch closures and alarm loops.
LI-157: $85

Smart Quad Stepper Controller:
On board microprocessor controls four motors simultaneously. Uses simple commands like "MOVE ARM 10.2 (INCHES) LEFT". Set position, ramping speed, units... Many inputs for limit switches etc. Stepper motors available.
SC-149: $299

NEW

FA-154 High Speed 12 Bit A/D Converter:
Blinding speed at low cost! Convert at 10 µS. Eight input channels accepting 0-5V signals. Special onboard variable gain amplifier lets you read signals less than 11SB (1.2mv). For value combined with speed in data acquisition and signal processing, this converter leads the pack!

FA-154: $179.00

12 Bit A to D:
Range: ±4V.
On-board amp. 1mV resolution.
Conversion time 100ns. 1 channel; expand with RE-156 or MX-155
AN-146: $153

Odin Software:
PC compatible. Control relays from analog inputs or time schedules. Logging. Runs in background.
OS-189: $129

Reed Relay Card:
8 Reed relays (20mA at 60VDC, SPST).
RE-156: $109

Digital Output Driver:
8 outputs: 250mA at 12V. For relays, solenoids, stepper motors, lamps.
ST-143: $78


A-Bus Adapters:
IBM PC/XT/AT & compatibles.
AR-133: $69

MicroChannel Adapter:
Parallel adapters also available for Apple II, Commodore 64, 128, TRS-80.
AR-170: $93

Serial Adapter:
Connect A-Bus systems to any RS-232 port. SA-129: $149

Serial Processor:
Built in BASIC for off-line monitoring, logging, decision making.
SP-127: $189

These products work with IBM PC, Apple II, Commodore and Tandy, etc. Our serial interfaces let you use any computer with an RS-232 port.

We back our low prices with great customer service! We're a totally service-driven company. To keep our prices low and volume high, we must rely on your repeat business. Never worry about a problem with Alpha Products. We fix everything. We guarantee everything. No fine print. No excuses. We're here to make you successful.

Kevin Tschudi, Engineer, Alpha Products

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CIRCLE NO. 156

EDN June 6, 1991

303 Linwood Avenue, Fairfield, CT 06430 Phone (203) 259-7713 Fax (203) 254-0169

ALPHA Products 1-800-221-0916
Low-cost pc-board design software packages that run on personal computers are easy to use and have many of the capabilities of more expensive packages. They are a smart choice for engineers who design their own boards or occasionally design prototype boards.

Low-cost pc-board design software has a surprising number of the same capabilities you'll find in software packages costing much more. For less than $5000—often much less—you can obtain software that supports all the steps—design entry, component placement, routing, and design-rule checking—you need to generate artwork for fabricating a board from a schematic design. The ease of use of these packages makes them suitable for both dedicated pc-board designers and engineers needing quick turnaround and tight control over pc boards for prototype and other development applications. Table 1 lists the capabilities of representative low-cost pc-board design software packages.

The first step in using any pc-board design system is having a schematic of the circuit you want to build. Although pc-board design systems let you design from scratch using a schematic drawn on the back of an envelope, you'll save time and avoid errors if the schematic is in an electronic format that the software can read. PC-board design systems are usually compatible with a variety of schematic-entry programs. The system typically needs two lists of information from the schematic: the netlist and the component list. Once the software has this information, you can start designing the board.

In addition to the initial electronic transfer of a design from the schematic to the pc-board design tools, some packages offer forward and back annotation. Both functions help keep the data matched between the pc-board design and the schematic.

Back annotation automatically transfers data back to the schematic after you have designed the pc board. Data typically back annotated are component identifiers and IC pin numbers. After layout, you automatically or interactively assign component identifiers in a logical sequence such as from left to right and top to bottom of the pc board. Back annotation updates the schematic to match the new component identifiers.

During layout, you or your software may have to reassign the logic blocks of ICs such as NAND gates or flip-flops that have multiple logic blocks to improve
the layout and shorten connections. By automatically back annotating these identifier and pin changes to the schematic after you've completed the layout, you'll have a schematic that accurately matches the pc board. Keeping the schematic and pc-board layout consistent is difficult to do if you back annotate interactively or manually.

Forward annotation is most useful when you need to add engineering changes to an existing design. When you need to change a pc board because of errors in the schematic or a change in requirements, you'll often correct the schematic first. Forward annotation makes the component additions or deletions on the layout and adds or removes the corresponding logical connections. You'll still need to place any new components and change the logical connections to physical tracks.

PC-board design software packages sometimes communicate better with the software vendor's own schematic-entry software than with schematic-entry software from another supplier. You should look into this issue if you are trying to match a pc-board design package with another company's schematic-entry software.

To take advantage of the netlist connection information and the parts list from a schematic-entry program, you need to have a component library that has all the components of your design. You have two alternatives: make or buy. Most design packages offer component libraries either as options or standard with the package. Purchasing a large component library can save you considerable work compared with creating your own, but you can't assume that a purchased library will fit your exact requirements.
Design software that uses the netlist's connection information should prevent you from connecting a trace to the wrong component pin.

If your company has developed its own component footprints to match its particular manufacturing methods, you can’t assume the library you buy will match. For example, the lead spacing allowance for a quarter-watt resistor may vary from one company to the next.

Once you’ve obtained component models that include the components’ physical footprints and have created a board outline drawing that includes connectors, the

Table 1—Representative low-cost pc-board design packages

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Product</th>
<th>Price (Basic package)</th>
<th>Back annotation</th>
<th>Gate and pin wrap</th>
<th>Component on both sides for SMT</th>
<th>Connection-length listing</th>
<th>Force vectors</th>
<th>Through-hole and SMT</th>
<th>Blind and buried vias</th>
<th>Design-rule checking, on-line</th>
<th>Minimum grid size for manual routing (mil)</th>
<th>Maximum power and ground layers</th>
<th>Maximum number of nets</th>
<th>Maximum pc-board dimensions (in.)</th>
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Note: NS = Not specified, U = Unlimited, R = Recommended, L = Limited capability.
next step is placing the components on the board. Component placement is one of the most critical steps in board design. Whether you'll be routing the board interactively or using an autorouter, a good component placement will determine how easy routing will be.

Automatic placement tools do exist, but they can't perform the complete placement task. You should expect an automatic placement tool to give you an intelligent initial placement. At that point, you'll have to move components around to get an optimum placement.

Tools exist that can help you with manual component placement, and many of them are available with low-cost pc-board design software. The rat's nest display is a feature of almost all pc-board design packages and is probably the most useful tool. A rat's nest display shows network connections as straight point-to-point connections between component pins. The connections in a rat's nest display are typically rubber banded: When you move a displayed component, the display maintains the point-to-point connection by lengthening or shortening the connection and changing the angle. Using a rat's nest display, you can see immediately how well a particular placement groups interconnecting components.

Because the rat's nest display is sometimes confusing on dense pc boards with many connections, some software packages also offer alternatives. Some let you look at only a portion of the rat's nest at a time. By showing only the connections for a selected component, you can see how well the component is placed relative to the components connected to it.

Force vectors are another tool that aids in component placement. A force vector is an arrow attached to each component. The vector's direction and length indicate the average direction and length of all the connections to a component. Force vectors simplify the display, but they also eliminate connection information.

Another placement aid displays the density of connections on the pc board. By finding where the number of connections is likely to exceed the space available for tracks, placement-evaluation tools can help you avoid a component placement that would be difficult or impossible to route.

**Keep connection lengths short**

A good placement not only makes routing easy, but it should also minimize connection lengths. A measure of a layout's efficiency is the average connection length. The design software usually measures connection lengths by assuming that all tracks must run horizontally or vertically to connect two points. This type of connection length is sometimes called the Manhattan connection length. A layout that reduces connection lengths may be an improvement if it does not create areas where connection densities are too high for you to effectively route the board.
The best autorouters for personal computers typically cost $4000 and more, which pushes the system cost above the $5000 low-cost limit.

One way to minimize connection lengths is to reorder connections on a net after you’ve placed the components. If a net includes more than two nodes, reordering the connections will sometimes result in shorter connection lengths. Some software can reorder nets automatically.

Part of the placement task is making the pin and gate swaps necessary to minimize connection lengths and ease routing. Some software packages perform the function automatically; others offer interactive pin and gate swapping.

Component placement is a highly interactive process. You need to be able to move components quickly and easily. PC boards for surface-mount designs might require placing components on both sides of the pc board.

Component placement is one of the most critical steps in board design. The photo shows placement in progress using the Tango software package from Ace Technologies Inc.

Not all software packages let you do so. When evaluating a pc-board design system, you’ll want to make sure the software and your computer can move and rotate components quickly and pan or zoom quickly.

Count on interactive routing

After developing a good component placement, you’ll move on to routing the pc board. Even if you expect to use an autorouter, you should still count on spending considerable time using the interactive routing tools. You may need to do interactive routing for special analog or digital requirements or for cleaning up areas that the autorouter didn’t do to your liking or wasn’t able to complete. Although most pc-board design tools all perform the same operations in the interactive routing mode, the ease with which they do so varies.

For example, if the design tool takes advantage of the netlist and component information, you won’t need to look for component identifiers and count to the correct pin on an IC. The software will use rubber-banded connections or some other method to show you the track or tracks you need to create for each net. Software that uses the netlist connection information should also prevent you from connecting traces to the wrong component pin.

When routing long traces, you might view a zoomed-in display of the area around the source of a signal and find that the destination is not visible on the screen. You’ll find that having the display indicate the direction of the signal’s destination is a helpful feature. Rubber banding a track as you lay it down from its start to its destination is an easy-to-follow method that works whether the destination is inside or outside the viewing area.

In addition to clearly showing which pads you must connect, the software should make creating the physical connections easy. The pc-board design software should let you quickly add tracks, vias, and change layers. Software that automatically adds a via when you select a different pc-board layer simplifies design. Another timesaver is being able to move a portion of a track from one layer to another.

Interactive routing usually requires some backtracking. You should be able to easily move or delete tracks or track segments. Software that can automatically and simultaneously remove tracks and vias will save you time. Modifying a route rather than removing and rerouting the net is another timesaver.

Satisfy special routing requirements

For complex pc boards, being able to quickly alter a track’s width while you’re routing is important. Track-width changes are sometimes necessary on analog designs and when routing through narrow spaces on surface-mount pc boards.

If you need to create a large irregular copper area on a board, you can do so on just about any system by adding wide traces until you fill the area with copper. Creating an outline of the area and using an area-fill command to create the partial copper plane is an easier method and is available on some systems.

As pc-board density and complexity increase, software support for more-complex manufacturing techniques becomes necessary. For example, you may need to use blind and buried vias, which many low-cost pc-board design packages support. Try an evaluation package before you buy to see whether support means possible but difficult, or easy enough for you to use the tool to quickly perform common functions for your type of design work.
Periodically as you design, you'll need to perform a display redraw to fill in the display in areas where you have deleted objects. A fast display redraw helps keep you from losing your concentration.

To keep screen redraws fast, some software packages display only the centerline of a trace and not its actual width. Some packages leave out other physical details around pads. This display method speeds display redraws, but you also need the option of seeing the true copper shapes of traces and pads.

Many pc boards use power and ground planes, and most design packages let you design these planes. Such software automatically connects power and ground pins to the correct planes. The software also adds clearance areas around vias and pads that do not connect to the plane.

The right autorouter may save time

Interactive routing, even with the most efficient pc-board design tools, can take days or even weeks for large or dense designs. Autorouters are another option. Although you can buy pc-board design software including autorouters for less than $5000, you'll spend more for a package that includes a high-performance autorouter.

Selecting an autorouter is not easy for either low-cost or high-performance design packages. Autorouters use different routing methods and have capabilities that are difficult to quantify. Furthermore, designers use them on a wide variety of pc-board designs.

An autorouter that does an excellent job on TTL designs might not be of any value on ECL designs because it would be unable to put termination resistors near destinations and follow other ECL routing requirements. The presence of analog circuitry in a design provides further challenges to autorouters. You don't want digital tracks crossing sensitive analog areas, and the autorouter would have to follow an endless variety of other special requirements common to analog designs. Surface-mount designs add yet more specialized manufacturing requirements for autorouters, including the directions for traces to enter pads. A through-hole TTL design that has plenty of space between components and a good component placement may be successfully routed by a variety of autorouters. Poor component placement can stump the best autorouter.

Keeping in mind the difficulty of making generalizations about autorouters, a few comments might keep expectations in order and provide some thoughts for evaluating these tools.

The best autorouters for personal computers typi-

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**High-priced pc-board design packages**

Some of the same companies that offer low-cost pc-board design packages also offer higher-cost tools with higher-performance capabilities. Often these tools can accept larger designs and operate more efficiently by taking advantage of the 32-bit mode of 386-and 486-class computers. Also, if you have more than $5000 to spend, you can afford the extra $4000 to $7000 you'll need to buy one of the best autorouters available for personal computers. You can usually upgrade a low-cost system by buying a high-priced autorouter later with little or no price penalty.

As you move up to workstation-based software packages, you'll find capabilities that extend beyond those of today's personal-computer-based products, at least in some areas. For example, you probably can't find a personal-computer-based autorouter that intelligently handles ECL, but you can find such a workstation-based product. ECL autorouters are more common as workstation products not because of any inherent limitations of personal computers, but because workstation-based CAE companies have more customers who need ECL tools.

In fact, personal-computer software for pc-board design is making the jump to 32-bit processing, putting the software limitations of personal computers on a par with the limitations of workstations. Although most of today's pc-board design software is still written in 16-bit code, within the next year you'll probably see many design packages that are written in 32-bit code.

Even though 486-based personal computers offer impressive processing power, high-performance workstation-based systems continue to offer superior processing speed for autorouting large designs.

Workstation-based design systems also offer a robustness that comes from their creators' having worked on pc-board design problems longer. Considerations such as support for military-standard documentation and release control, which prevents you from using the wrong design revision, are common on workstation systems. One thing you probably won't get on workstation-based systems, however, is ease of use.
Low-cost pc-board design tools

cally cost $4000 and more, which pushes the system cost above the arbitrary $5000 low-cost limit. Auto­
routers are often options available with basic pc-board design packages, so you can always add them later.

The best justification for using an autorouter is that the tool will save you money compared with the time you would otherwise spend routing boards. A good autorouter can pay for itself quickly, even if it costs $10,000. Unfortunately, an inexpensive autorouter with limited capability won't be cost effective even if you need to design only a few boards.

An autorouter that completes 85% of the routes on a pc board is probably not going to save you any time because it forces you to move many tracks—probably every single one—to route the remaining 15%. A router that completes more than 95% of the routes might be worth looking into, but you really want a tool that routes more than 98%.

Don't be fooled by an autorouter that achieves a high routing completion by using an excessive number of routing layers. The autorouter has to be routing in the same number of layers you'd use for an interactive design, or it's wasting your money on extra pc-board layers. That waste will continue for the life of the design.

Autorouters require you to set several control pa­
rameters, depending on the complexity of the router. For example, many autorouters let you trade connection length for vias to help reduce the production cost of boards.

Autorouters have variations in what level of interactive use they support. Some autorouters are re-entrant. You can autoroute, stop, make some manual routes or changes to routes, and then resume autorouting the remaining nets. Others tools don't let you inter­rupt and restart them. Sometimes routers that aren't re-entrant let you preroute signals. You can route critical signals yourself before you start the autorouter.

A feature typically found on the more expensive pc-board routers is a push-and-shove capability. When a designer working interactively needs to add a track where there is no space, the autorouter will push tracks over, if possible, and make slight changes to avoid clearance violations. Autorouters with the push-and-shove capability sometimes support interactive operation in a semiautomatic mode. You designate where you want the new track to go, and the router pushes other tracks out of the path.

Editing a pc-board design after an autorouter has finished with it is not an easy task. A designer has a much easier time editing a board he or she has personally designed than a board someone else has designed. Autorouters definitely count as someone else.

Let the software look for violations

Periodically as you route a pc board, you need to verify that you have not created any design-rule viola­
tions. Although autorouters automatically satisfy the design rules, when you work interactively, you might create a design-rule violation. Design-rule checking is a design-software feature that can save considerable time compared with manually checking a layout, and it's more accurate. Design-rule checking can guarantee that the pc-board connections match the schematic and can verify that you've routed the board with proper clearances.

The basic function of design-rule checking is verifying clearances between copper areas. Depending on the software, you may be able to designate different pad-to-pad, pad-to-trace, and trace-to-trace clearances. Some systems allow additional clearance specifications for vias and solid copper areas. Others use the pad clearance for vias.

One concern should be that design-rule checking verifies the spacing between the actual copper areas. For example, if the checker assumes the pads are circular, and they are in fact rectangular, a diagonal trace running close to a rectangular pad might touch it.

Design-rule checking is available on line or in batch mode. You run batch checkers periodically during the design to find and correct errors. Some design tools offer both batch and on-line checkers. On-line checking sounds great in theory because it prevents you from creating a design violation. In practice, it is sometimes a nuisance.

While interactively routing, you'll often want to
Low-cost pc-board design tools

move an existing route to open up space for a new route. In the process, you might temporarily leave a track touching a pad belonging to another net. After entering the new track, you’d go back and clean up the temporary violation. With on-line design-rule checking, you are unable to leave any temporary violations. Designers accustomed to leaving temporary violations will find on-line checking unnatural and inefficient.

When you are routing signals in a design that has different design rules for different signals, the on-line checker is helpful. Rather than keeping track of the design rules for each signal, the on-line checker makes sure you are following the correct design rules for each net. To use design-rule checking in this fashion you need a signal-specific checker, a feature of some pc-board design tools.

Speed is another issue for design-rule checking. Whether the checker is on-line or runs as a batch job, it shouldn’t hinder design. Some systems let you restrict the checker to the area on the screen to boost speed.

Manufacturers of low-cost pc-board design tools

For more information on low-cost pc-board design tools such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN’s Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Satisfying the design rules isn't always the end of the design task. You may need to satisfy special requirements, usually for manufacturing, to finish the job.

If you've designed the pc board interactively, you may have incorporated most of the manufacturing requirements as you routed the board. Some changes, however, are easier to make after you've routed the complete pc board. For example, removing vias when a track doesn't need to change layers is usually easiest to do after you've routed all the nets. Autorouters typically make a manufacturing pass after routing to reduce vias, miter corners, and make other improvements.

After you've completed a pc-board design and are ready to have it fabricated, you'll need to make films. Most pc-board design packages provide standard outputs for photoplotters and drill tapes, although—inevitably—these outputs are sometimes options. Before you make expensive photoplots, you may want to examine a printout of the actual copper areas. Software available with many of the design packages lets you make printouts for visual checks.

System limitations to check

Most low-cost pc-board design systems can accommodate many different design types, but there are some absolute limitations that may prevent you from creating a particular design. Table 1 lists some of these limitations. In most cases, the limitations won't be a problem.

For example, most systems have a minimum grid resolution of 1 mil for manual routing. This minimum shouldn't be a limitation for pc-board design, although it might be an issue for hybrid designs. A few systems have resolutions in the micron range.

Another limitation is the number of board layers the software can handle. A pc-board design package might be limited by the number of signal or power and ground layers. Even most low-cost pc-board design systems can handle boards of eight or more layers, but some software packages are limited to fewer layers.

If you anticipate rotating components in increments other than the standard 90 degrees, you'll find a few packages that support 1-degree or smaller rotation increments. When special pc-board design requirements call for components to be organized in a radial manner, being able to rotate components in small increments is mandatory.

If you design large pc boards, you'll want to verify that a software package can support the number of ICs and networks you'll need. Table 1 lists the maximum number of networks the software packages support. Some packages do not have a strict limit and assign memory as needed, sharing it with other functions. In these cases, the manufacturer may not specify the number of nets the software will let you use.

Another indication of the capacity of a design tool is how much memory it can use. Software packages for IBM and compatible personal-computer systems are sometimes limited to 640k bytes of memory and designs of a few hundred ICs. Those systems that take advantage of extended or expanded memory can accommodate designs of several thousand ICs.

As the size of your design increases, so does the need for computing power. Although you can easily design a pc board with fewer than 100 ICs on an IBM PC/AT or compatible computer, designs of several hundred ICs call for 386- or 486-based systems. The computing power is especially important if you plan to use a high-performance autorouter. Even on a 386 or 486 system, a high-performance autorouter may spend more than 12 hours working on a large board that has many components. Evaluate pc-board design software on a system with the same processing speed and memory you expect to be using.

Given the many low-cost pc-board design packages available, choosing the one that best fits your needs is difficult. Even if only one looks like the right package for you, definitely try the evaluation package that most companies offer.

Evaluation packages are relatively complete and are not canned demonstrations. Usually you can perform all the pc-board design functions the complete system offers, but the evaluation software limits you by not saving or printing your design. Although you might need a few days to exercise an evaluation package completely, when you're done you'll have a good idea of what the system can do, and you'll be more than half trained on the software should you choose to buy it.
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RAID 5 architecture provides economical failsafe disk storage

Traditional methods used to back up critical data can be expensive and slow. A parity-based disk-array architecture offers an alternative that attacks these drawbacks.

Michael Anderson, Micropolis Corp

Redundant Arrays of Inexpensive Disks (RAID) (Ref 1) is a hardware and data architecture for mass data storage. Currently there are six variants, or levels, of the RAID architecture, ranging from RAID 0 to RAID 5. Each level describes an arrangement of data on an array of disk drives that increases your storage capacity and provides data redundancy in the event of a drive failure. RAID 5 is the most versatile of the RAID variants. RAID 5 provides fast data access and an inexpensive means to achieve fault tolerance that challenges traditional backup techniques.

Many of today's top-quality disk drives boast MTBF's greater than 150,000 hours. However, this MTBF translates to a 6% yearly failure rate, which can be catastrophic for many critical applications. Therefore, system designers must provide other assurances that critical data won't be lost. Traditionally, system designers have relied on two approaches to achieve fault-tolerance. The first approach, tape backup, suffers from mechanical limitations; restoring the data onto a high-capacity disk drive can often take hours because of the tape drive's slow access time.

The second approach is to record critical data simultaneously on two separate disk drives—a technique known as disk mirroring. Should one of the disk drives fail, the data on the alternate disk drive is immediately available. Disk mirroring reduces the probability of total data loss to the unlikely probability that the alternate disk drive will fail before you can replace the failed disk and restore the data onto a new disk.

Although disk mirroring is a fast and reliable method for achieving data redundancy, it's expensive. You must employ twice as many disk drives to back up the data completely. RAID 5 provides a less expensive alternative to disk mirroring while maintaining a similar low probability of total data loss.

RAID 5 is mathematically simple

The mathematics supporting the RAID 5 architecture employ the basic algebra postulate that states "If A + B = C, then C - B = A and C - A = B." RAID 5 uses this same postulate but employs modulo-2 addition. In modulo-2 addition, an exclusive-OR (XOR) operation generates the arithmetic sum of the A and B terms, which is also known as odd parity. The postulate lets you reconstruct data on a single drive in the array using data stored on the remaining drives.

A simple example demonstrates how the RAID 5 technique works. Consider an array of three disk drives that store data in single bytes (8 bits). Two of the drives contain actual data, whereas the third drive contains the modulo-2 arithmetic sum of the data on the other two disk drives—odd parity. If one data drive
RAID 5 can employ the host CPU to generate parity or reconstruct data for a failed drive without incurring additional hardware cost.

contains the binary value 00110000, and the other data drive contains 00000011, the parity drive contains 00110011. Table 1 shows how you reconstruct the data on any of the disk drives by generating the XOR function for the data on the remaining drives.

The money you save when you use RAID 5 rather than disk mirroring to achieve fault tolerance increases as the required capacity increases. If an array requires $n$ disk drives to attain the required capacity, disk mirroring requires $2 \times n \times \text{cost/drive}$. In contrast, RAID 5 requires $(n+1) \times \text{cost/drive}$ to achieve the same degree of reliability. For an array containing two data drives, disk mirroring costs $4 \times \text{cost/drive}$ where RAID 5 costs $3 \times \text{cost/drive}$. The extra cost to achieve fault tolerance using RAID 5 asymptotically approaches the cost of an array without backup as the number of drives in the array increases. The additional cost for RAID 5 is $(n+1)/n$ times the cost of an array without backup. If an array has 5 data drives, RAID 5 costs you $(5+1)/5 = 1.2$ times cost/drive to add fault tolerance.

Disk-drive costs don’t quite complete the expenditure necessary to implement RAID 5. However, the additional hardware costs are minimal. Two additional cost factors complete the picture: the cost of the additional hardware required to control redundant data storage and the hardware cost to generate parity.

Disk drives containing a SCSI disk controller are the most efficient building blocks for the RAID 5 architecture. To employ SCSI, the host computer needs a SCSI-to-host adapter board. The board lets the host control as many as seven SCSI disk drives simultaneously. SCSI-to-host adapter boards currently cost from $50$ to $200$.

For most applications, the additional cost to generate parity can be zero. Practically all of today’s file servers contain fast RISC (reduced-instruction-set computer) or CISC (complex-instruction-set computer) CPUs that have 32-bit data paths. These CPUs can execute an XOR instruction, which generates parity, in a shorter time than the time to transfer data to a disc drive. For example, a 33-MHz Intel 80386 µP can generate parity at a rate exceeding 8M bytes/sec, which is four to eight times faster than the typical SCSI transaction rate. Therefore, a basic implementation of RAID 5 can employ the host CPU to generate parity or reconstruct data for a failed drive without additional hardware cost.

### Three strategies manage the data

RAID 5 not only offers fault-tolerance at a lower cost than traditional disk mirroring, but the architecture also efficiently distributes and manages the data on the disk drives. RAID 5 offers three data-management strategies. To write new data to a disk drive using strategy 1, called read-before-write, the host first reads the old data and the old parity bytes from their respective disk drives. The host then removes the effect of the old data on the old parity byte before generating a new parity byte using the new data (Table 2). The host can then write the new data and the new parity to their respective disk drives.

Strategy 2, read-what-you-don’t-have, writes data to a disk drive in a different manner. First, the host reads data from a disk drive whose data isn’t being modified. The host generates a new parity byte by taking the XOR of this data with the new data to be written (Table 3). The host then writes the new data and the new parity byte to their respective disk drives.

RAID 5 employs strategy 3, read-nothing, when modifying all of the data drives simultaneously. For example, in a 3-drive array, when the host must simultaneously modify both data drives, there isn’t a need to read old data or the old parity byte. The host simply generates a new parity byte from the two new data bytes and stores both the data bytes and the new parity byte on their respective disk drives.

RAID 5’s three data-management strategies offer different advantages depending on the number of blocks that you need to modify. If you need to modify

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**Table 1—Reconstructing the data for a failed disk drive**

<table>
<thead>
<tr>
<th>XOR</th>
<th>Drive 1 (data drive)</th>
<th>Drive 2 (data drive)</th>
<th>Drive 3 (parity drive)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00110000</td>
<td>00000011</td>
<td>00110011</td>
<td></td>
</tr>
<tr>
<td>00000011</td>
<td>00110000</td>
<td>00110011</td>
<td></td>
</tr>
<tr>
<td>00110011</td>
<td>00000011</td>
<td>00110000</td>
<td></td>
</tr>
</tbody>
</table>

**Table 2—Calculating new parity using strategy 1**

<table>
<thead>
<tr>
<th>XOR</th>
<th>Drive 1 (old data)</th>
<th>Drive 2 (old data)</th>
<th>(Old parity with old data removed)</th>
<th>New parity</th>
</tr>
</thead>
<tbody>
<tr>
<td>00110011</td>
<td>00110000</td>
<td>00000011</td>
<td>11000000</td>
<td>11000011</td>
</tr>
</tbody>
</table>

**Table 3—Calculating new parity using strategy 2**

<table>
<thead>
<tr>
<th>XOR</th>
<th>Drive 1 (old data)</th>
<th>Drive 2 (old data)</th>
<th>New parity</th>
</tr>
</thead>
<tbody>
<tr>
<td>00110011</td>
<td>00110000</td>
<td>00110000</td>
<td>11000011</td>
</tr>
</tbody>
</table>
only one block of data, strategy 1 is the most effective. If you need to modify data on more than one half of the disk drives, you should employ strategy 2 because there is less data for the host to read before modifying the blocks. If you must modify the data on all of the drives, strategy 3 is the most efficient since it doesn’t require the host to read data from any drive.

**RAID 5 distributes data and parity**

You’ve probably noticed that all three strategies for modifying a data drive also require the host to modify the stored parity byte. If you store parity information on a single disk drive, as some variants of the RAID architecture suggest, each time the host modifies data in the array, it must also access the parity disk drive. Therefore, an array architecture having a single parity disk drive creates a bottleneck because the host can only modify data sequentially.

RAID 5 overcomes this potential bottleneck by distributing the parity information over all of the drives in the array. Because each drive in the RAID 5 architecture contains a mixture of data and parity, the host can issue read and write commands in parallel. Table 4 shows a typical RAID 5 implementation for an array containing 4 disk drives. In this implementation, block 1 data resides on drive 1 and block 6 data resides on drive 2. The parity information for these two blocks is on drives 4 and 3, respectively. Therefore, the host must access drives 1 and 4 to modify block 1 data using strategy 1. Similarly, the host must access drives 2 and 3 to modify block 6 using strategy 1. Because the drives are independent, the host can modify both blocks of data in parallel.

Satisfying multiple disk transfer requests in parallel increases the system’s transaction rate. A high transaction rate is important for image processors and virtual-memory systems that swap large amounts of data in solid-state memory to and from disk. The data distribution shown in Table 4 locates sequential blocks of data on successive disk drives in the array. This arrangement lets the host queue four read requests, for example, from blocks 5, 10, 3, and 12. The queued requests permit the four independent disk drives to access the correct track and sector for the blocks in parallel and thereby proportionally reduce the disk access time.

Many operating systems, including PC-DOS, generate disk requests of varying length. For example, when the operating system loads a program into memory it can generate a large disk request ranging from 64 to 128 blocks of data. On the other hand, when the host accesses a file directory or updates a database, the operating system generates a small disk request ranging from 1 to 4 blocks. The RAID 5 architecture can efficiently handle both types of request and provide inexpensive failsafe storage as well.

**Reference**


**Author’s biography**

Michael Anderson is the director of software engineering for Micropolis Corp. For the past 2 years he has managed an engineering and support staff, participated in market planning, and defined future products. He has also contributed to the development of 360M-, 760M-, and 1.2G-byte disk storage products. Michael majored in computer science at the University of Nebraska and is married with 3 children. He lists parallel arrays, processors, and storage as personal interests.

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Careful inductor selection optimizes dc/dc converters

Higher output power levels and faster switching speeds have complicated the selection of inductors for small dc/dc converters. However, if you check circuit waveforms for anomalies and review key electrical parameters during the design phase, you can simplify the development of an optimized dc/dc converter.

Bruce D. Moore, Maxim Integrated Products

Battery-operated systems and distributed-power-system concepts have greatly increased the use of low-power dc/dc converters and their associated magnetic components. Designers typically use transformers in dc/dc converter designs. However, unless transformer isolation is required, an inductor makes sense for a low-power switching-converter application. This is especially true if the circuit must be more efficient than a capacitor-based charge-pump circuit. Compared with transformers, inductors are easier to specify, procure, and mount. Single-transistor-driver schemes are more effective with inductors than with transformers. Best of all, there's a variety of inductor types available, each in a range of inductance values.

Because standard inductors suit most applications, you can usually avoid expensive custom-magnetics development. Selecting the optimum inductor requires some knowledge of the available inductor geometries and core materials, however. (Note that for some unknown reason, inductor data sheets are often cagey about the product's core-material type.)

In the context of designing dc/dc converters that have an output power capability of 10 watts or less, a boost regulator serves as a general example. The boost regulator used as an example, also called a flyback regulator, features pulse-frequency modulation (PFM) to first establish its L value and then calculate its maximum ratings. By examining the inductor further, you can find certain specifications and characteristics that are a function of its shape and materials.

Fig 1 illustrates the three basic topologies for single-inductor switching regulators—the buck (or step-down), the boost (or step-up), and buck-boost (or inverting) topologies. Low-power regulator applications generally combine one of these topologies with a PFM or PWM (pulse-width-modulation) controller circuit. The different combinations of topology and controller place similar demands on the inductor. However, you must take extra care in calculating the inductance value in pulse skipping controllers.

When selecting an inductor for a simple buck-regulator circuit, you must take several factors into account—inductance value, saturation current, dielectric strength, dc resistance, EMI, and stray capacitance.

The converter's switching frequency and the voltage drop across the inductor determine the correct induc-
Because standard inductors suit most applications, you can usually avoid expensive custom-magnetics development.

tance value. Both factors affect the inductor current's rate of change in any given application. Erroneous inductor values can generate excessive current in the switching transistor or lower the inductor's energy storage performance. Insufficient energy storage, in turn, slows both converter start-up- and transient-response times. In clocked-PFM regulators, insufficient energy storage will also degrade load regulation.

Economic considerations also provide a strong incentive to reduce inductor values: lower values require less wire and smaller cores. As a rule, you should select an inductor whose value is as low as possible, and yet does not introduce excessive-current, inefficiency, component stress, and high-ripple problems.

Pulse-skipping PFM regulators, such as the boost circuit in Fig 2, are a good choice for battery-powered applications because the design draws minimal quiescent current and requires few external components. Here, however, you must be especially careful when selecting the inductor, to avoid load-regulation problems. Studying the regulator's switching waveforms (Fig 3) provides some clues about the factors that influence a PFM regulator's output.

Supply voltage and inductance value determine the slope of an inductors' current waveform. Because the regulators in question operate in a discontinuous-current mode (the current returns to zero on every cycle), the regulator's average load current is directly proportional to the peak inductor current. Peak current depends on slope, and the slope depends on the inductor's value. An inductor with an excessive L value, therefore, cannot transfer adequate energy on each oscillator cycle.

Peak inductor current can be expressed in terms of the voltage boost ratio and the load current as

\[ I_{PK} = (4I_{LOAD})\left(V_{OUT} + V_D - V_IN\right)/(V_IN - V_{SW}), \]

where the factor of 4 is a constant resulting from the 50% duty cycle. Values for \( I_{PK} \) and the switch transistors' on time (\( t_{ON} \)) let you calculate the optimum inductor value as

\[ L = (t_{ON})(V_{IN} - V_{SW})/I_{PK}, \]

where \( V_{OUT} \) equals output voltage, \( V_{IN} \) equals supply voltage, \( V_{SW} \) equals saturation voltage of the switch transistor, and \( V_D \) equals the forward voltage of the rectifier diode.

Coil inductance must not be so low that peak currents saturate the core or overstress the switching transistor. This rule applies to both PFM and PWM regulators. Excessive inductor current causes many odd symptoms, including low efficiency, rattling heat sinks, whining coils, and increased output ripple. Very low inductance can lead to burned windings and shattered, smoking transistors and ICs. The worst-case \( I_{PK} \) in the previous PFM-regulator calculations occurs when load current, supply voltage, and the diode's forward voltage are all maximum values while inductance, switch on-resistance, winding resistance, and switching frequency are all minimum values.

As you strive to extract higher output current from a PFM regulator, the minimum- and maximum-allowable inductor values tend to converge. An actual convergence indicates the need for a power transistor capable of higher currents. But excessive peak currents can result from the discontinuous-current mode in which the inductor operates. This \( I_{PK} \) limitation makes clocked-PFM regulators impractical for power levels exceeding 10W.

The following example uses earlier equations for \( I_{PK} \) and \( L \) to convert an input of 5V (±10%) to an output of 15V using a 1N5817 diode and a MAX641 regulator IC. The IC has a ±10% tolerance on its 50-kHz oscilla-
To regulate the output voltage, the MAX641 boost regulator employs clocked pulse-frequency modulation or pulse-skipping techniques.

The output-current capability must be 15 mA. First, calculate the maximum-allowable inductor value using the equation

\[ I_{PK} = 4(15 \text{ mA})(15\text{ V} + 0.4\text{ V} - 4.5\text{ V})/(4.5 - 0.75) = 174 \text{ mA} \]

\[ L = (9 \mu\text{sec})(4.5\text{ V} - 0.75\text{ V})/174 \text{ mA} = 194 \mu\text{H} \]

Next, you must calculate the minimum-allowable inductor value. Here, let \( I_{PK} \) equal 450 mA—the maximum current rating for the switch transistor in the IC. With those criterion,

\[ L = (11 \mu\text{sec})(5.5\text{ V} - 0.25\text{ V})/450 \text{ mA} = 128 \mu\text{H} \]

From off-the-shelf inductors, you can choose a standard value like 150 \( \mu\text{H} \)—a value which lies between the calculated minimum and maximum values.

**Selecting the inductor for PWM regulators**

Unlike pulse-skipping PFM regulators, most PWM regulators exhibit worst-case peak currents at minimum supply voltages. Because PWM regulators generally operate in a continuous-current mode at high duty cycles, their inductance values are limited only by winding constraints and the need for reasonable startup and transient-response times.

In continuous-current mode, the inductor current fluctuates, but never returns to zero. Because the current may increase in staircase fashion over a period of several cycles, its rate of increase (determined by the inductance value) does not constrain the maximum level attained by the inductor current or the average load current. Thus, PWM regulator designs do not impose a hard limit on the maximum inductance value. The minimum value depends on the inductor's I^2R loss and the switching transistors' current capability.

The exact inductance value is seldom critical for regulation in a PWM circuit, but some control schemes require a particular value for other reasons. The MAX743 dual-output regulator IC, for example, which features current-mode feedback control, achieves ac stability by compensating the inductor current's rate of change, or slope. To ensure ac-stable operation, which is free from subharmonic noise, you must tailor the slope compensation to a given supply voltage and inductance value.

**Don't overlook saturation effects**

In some specialized circuits the design deliberately saturates the magnetic core (for example, Royer-type self-oscillating transformer-drive schemes and saturable magnetic reactors that provide regulation in multiple-output, transformer-based power supplies). In most applications, however, you select the inductance and the core material (using air gaps in the core if necessary) to avoid saturation. For PWM regulators in particular, you must take care to avoid magnetic saturation.
Most pulse-width-modulation regulators exhibit worst-case peak currents at minimum supply-voltage levels.

Saturation-current ratings measure an inductor's ability to handle high concentrations of magnetic flux. Strong magnetizing forces put an inductors' core at risk of saturation when the peak current rises to a high level. When a core saturates, the apparent inductance value falls off and current begins to rise exponentially. IR losses cause a drop in circuit efficiency, and the inductor cannot store additional energy.

High-current spikes resulting from saturation can endanger power transistors and cause noise and efficiency problems. To avoid saturation, the inductors' worst-case peak current must not exceed its peak current or incremental-current rating. Note that inductors lacking a dc-current rating are usually prone to saturation, as are those with an ac amps rating.

Energy stored in an inductor determines the output power available at a given operating frequency. You can calculate energy storage as \( E = LI^2 / 2 \), where \( E \) equals energy in joules, \( L \) equals nominal inductance in henrys, and \( I \) equals peak or incremental current rating in amps. The energy storage requirement for the previous clocked-PFM design example is therefore

\[
E = (194 \, \mu \text{H})(174 \, \text{mA})^2 / 2 = 2.9 \, \mu \text{J}.
\]

Air gaps greatly amplify an inductor's ability to store energy by extending the effective length of the cores' magnetic path. Air can store a tremendous amount of energy. A small air gap, whether built into the material or created by grinding or machining operations, can more than double the power output from a given core by preventing saturation at high current levels.

Ferrite and other highly permeable core materials are very susceptible to saturation, and you must treat them accordingly. The closed magnetic path of a ferrite toroid, for instance, is extremely good for containing EMI. However, the short path combined with the ferrite's high permeability make toroids prone to saturation. Ferrite toroids make good transformer cores, but they are less suited to simple boost regulators featuring large dc-offset currents.

For applications of 5W or lower, powder-type cores with distributed air gaps are often a better choice than ferrite toroids or pot cores. After cutting an air-gap slot in the core of a ferrite toroid, the machining costs and EMI level will be so high that you may have been better off choosing a ferrite bobbin, with its large inherent air gap, in the first place. Pot cores, though self-shielding, are more expensive because they require more manufacturing steps than the other types.

Iron-powder and molypermalloy-powder toroid cores offer the best combination of cost, size, and EMI performance for many low-power applications. These materials have built-in air gaps that allow the core to saturate gradually as the magnetizing force increases. The large number of tiny air gaps are created by the binder material. Each air gap saturates at a slightly different level of magnetizing force.

The cylindrical or bobbin-core geometry, although noisy, is best for low-power ferrite applications because such shapes are easy to wind, and are therefore inexpensive to manufacture. Ferrite pot cores are preferable for applications higher than 5W. The pot core's low EMI emissions are a benefit in applications that involve high levels of current and magnetic field strength.

A look at core-material tradeoffs

There are no clear cut best-choice winners when you look at today's available core materials; each has a distinct advantage in certain areas (Table 1). Ferrites are attractive because they combine low cost with high volumetric resistivity, which minimizes eddy-current losses. Ferrites are the only choice for switching frequencies of 500 kHz and higher. On the other hand, ferrites' high permeability usually calls for an air gap and the associated complications: high EMI for bobbins and extra assembly steps for pot cores.

Molypermalloy powder (MPP), the Porsche of powder core materials, combines good saturation characteristics with low hysteresis losses. MPP is expensive, however; it contains scarce ingredients (nickel) and requires many processing steps. Iron powder and silicon-steel tape, despite their tendencies to sustain eddy-current and hysteresis losses, are inexpensive materials also suited to general-purpose applications.

For small size combined with good EMI performance, it's hard to beat high-flux MPP toroid cores. Standard MPP cores, formulated for RF applications, contain 80% nickel, plus iron and molybdenum. The high-flux variety contains 50% nickel and doesn't work as well for RF applications. However, high-flux MPP cores provide tremendous flux-handling that is useful in switching-regulator circuits.

For comparison, ferrite and standard MPP materials handle flux densities of 4500 and 7500 gauss, and the high-flux MPP material is good for 15,000 gauss. High-flux cores can handle switching frequencies ranging to 300 or 400 kHz before eddy-current losses become excessive. Like all MPP cores, the high-flux types are
Table 1—Common inductors that suit dc/dc converters

<table>
<thead>
<tr>
<th>Type</th>
<th>EMI</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ferrite bobbin</td>
<td>high</td>
<td>Makes compact, low cost, axial-lead (cylindrical) inductors. Low core losses support high efficiency.</td>
</tr>
<tr>
<td>Ferrite bobbin with ferrite shield</td>
<td>low</td>
<td>Efficient but prone to saturation.</td>
</tr>
<tr>
<td>Ferrite pot core</td>
<td>low</td>
<td>Efficient. Easily gapped to the correct value. Best for high-current or high-frequency applications.</td>
</tr>
<tr>
<td>Molded (low cost)</td>
<td>high</td>
<td>OK for light loads. Prone to saturation and often inefficient. Observe current ratings carefully.</td>
</tr>
<tr>
<td>Silicon-steel toroid</td>
<td>low</td>
<td>Tape wound; similar to iron powder. Use thinner tape for higher frequencies.</td>
</tr>
<tr>
<td>Ferrite toroid</td>
<td>low</td>
<td>Prone to saturation.</td>
</tr>
<tr>
<td>Molypermalloy-powder toroid</td>
<td>low</td>
<td>Best available for frequencies less than 400 kHz. Low EMI, low losses, compact, and expensive. Use high-flux type.</td>
</tr>
<tr>
<td>Iron-powder toroid</td>
<td>low</td>
<td>Specify core material carefully to achieve low losses.</td>
</tr>
</tbody>
</table>

For battery-powered and low-voltage applications of 3V or less. In these cases, the inductance values must be low enough to achieve an acceptable slope for the inductor-charging current. Ideally, this slope is determined by the input voltage and the inductance value or \( I(t) = \frac{V_{IN}}{L} \). The peak current is therefore a function of \( t_{ON} \), or \( I_{PK} = \frac{V_{IN}t_{ON}}{L} \). Finally, dc-winding resistance \( (R_{DC}) \) limits inductor current as the inductance value approaches zero, as given by the expression

\[
I_{PK} = \frac{V_{IN}}{R_{DC}} \left( 1 - e^{-R_{DC}t_{ON}/L} \right).
\]

Another current-related topic to consider is temperature rise. Inductor specifications generally include two current ratings—continuous (or rms) and dc saturation, which is sometimes referred to as peak or incremental current. A continuous rating accounts for the temperature rise caused by winding resistance, the inductor’s operating temperature range, and its insulation or potting-material properties. The continuous rating is usually higher than the dc-saturation rating. Often, however, just the opposite is true for higher-valued inductors. As a rule of thumb, make sure that the inductors’ average current is less than its continuous current rating. In high-frequency applications, be sure to include a safety margin for additional temperature rise due to core losses.

High-frequency losses consist of three major components—losses due to hysteresis, losses due to eddy currents in the core, and losses due to eddy currents in the wire. Legg’s equation defines losses within the core as

\[
R_{AC}/L \mu = Xf + YB_m f + Zf^2,
\]

where \( R_{AC} \) equals the equivalent loss resistance in ohms, \( L \) equals inductance in henries, \( \mu \) equals magnetic permeability, \( X \) equals residual-loss coefficient, \( f \) equals frequency, \( Y \) equals hysteresis-loss coefficient, \( B_m \) equals maximum flux level in gauss, and \( Z \) equals eddy-current-loss coefficient.

Magnetic hysteresis, which occurs as flux density nears its saturation point, becomes a problem in iron-powder cores at switching frequencies of 100 kHz or lower. A simple cure for this problem is to enlarge the core volume, which will reduce the peak flux density at high currents. Larger cores, however, exacerbate the eddy-current problem by providing more low-resistance paths for current. Eddy current in the core is a function of \( f \), and rapidly becomes a problem as expensive. For low-power miniaturized applications, however, the high-flux MPP cores are often more cost-effective than ferrite types because they eliminate the need for precision gapping.

Size reduction is possible with high-flux core materials, as can be seen by comparing two prototype boards for the MAX743 switching regulator. Both boards generate 3W at ±15V from a 5V source. However, the surface-mount version uses a high-flux core material to achieve a much higher power density—18W/in.³ vs 2W/in.³.

The core material affects the power level for a given inductor size, but dc resistance in the windings will waste some of that power. In the step-up circuit of Fig 2, the approximate average inductor current is given as

\[
I_{AVG} = I_{LOAD} ((V_{OUT} + V_D - V_{IN})/(V_{IN} - V_{SW}) + 1).
\]

High winding resistance produces an L/R effect in the inductor-current waveform. The resulting \( I_{FR} \) losses degrade circuit efficiency and cause the core temperature to rise.

For pulse-skipping PFM-type regulators, the dc-winding resistance can have the same effect as an overly high inductance value. By limiting \( I_{PK} \), dc resistance limits the available output current. Note that the calculation for maximum inductance value does not account for dc resistance. This dc resistance is significant for battery-powered and low-voltage applications of 3V or less. In these cases, the inductance values must be low enough to achieve an acceptable slope for the inductor-charging current.
Gap spacings in powdered-material cores are so small that EMI is seldom a problem as long as the core is a toroid.

the frequency approaches 300 to 400 kHz. To combat the eddy-current problem, consider switching to another core material rather than changing the core size.

Eddy current in the windings (circularizing currents within the wire) can also be a problem at frequencies of 500 kHz and higher. The solution here is to select a wire thickness equal to the skin depth of copper—a value determined by the switching frequency. Litz wire (ultra-thin, multistranded wire) or windings made from pc-board traces can help reduce eddy current. Positioning these windings within the core as far as possible from the air gap also helps.

Eddy currents appear in cores that have low volumetric resistivity. Low-resistance paths in the core cause the core to behave like a length of metal in a changing magnetic field. Circulating currents in the low-resistance path dissipate power. High switching frequencies (above 100 kHz) can develop significant eddy current in iron-powder and steel-tape cores and these currents generate a core-temperature rise (Table 2). Because the regulator may appear to be operating correctly, the problem can be difficult to detect.

You should settle EMI issues early in the design process, before they can affect the pc layout and component placement. Shielded inductors, for example, tend to be larger, more expensive, and more difficult to mount than unshielded types.

Electronic circuitry can often tolerate moderate levels of EMI. This is particularly true for digital circuits. Even analog circuits, if they involve general-purpose ICs such as the LM324 op amp, can often weather the noise associated with unshielded inductors. In these cases, it’s worth the effort to try an unshielded bobbin-type inductor in place of a pot-core or toroid inductor. The bobbin-type unit will cost half as much and be twice as small as an electrically equivalent pot-core or toroid inductor. Bobbin inductors generate their highest magnetic fields near the ends along the axis, so point them away from sensitive nodes and mount them at 90° angles to other magnetic components.

Another point to consider when selecting inductors is the problem of EMI. The air-gap spacings in powdered-material cores are so small that EMI is seldom a problem as long as the core is a toroid or has a geometry that features a closed magnetic path. Fringe fields are much greater for core geometries that include a cut, or have a large inherent gap such as that between the ends of a bobbin inductor wound on a cylindrical core. Pot cores and other clever mechanical designs make it possible to have air gaps in the ferrite material while keeping the EMI problem minimized.

The final problem area present is the stray interwinding capacitance in inductors with values of several millihenries and larger. This capacitance combines with the coils' inductance to form a tank circuit, which rings at the inductors' self-resonant frequency (SRF). In low-SRF coils, a sudden jump of coil current, which occurs when the power switching transistor turns on, precedes the normal linear ramp of current. Large values of stray capacitance, therefore, cause switching losses that lower the regulator circuits' efficiency.

To avoid this problem, set the SRF at least five to ten times the oscillator frequency, thereby minimizing the interwinding capacitance. You can minimize this capacitance during the toroidal-winding phase by overlapping the ends of the winding somewhat, or by leaving a gap between the winding ends rather than ending the winding with one full layer.

Author's biography
Bruce D Moore is a senior member of the technical staff at Maxim Integrated Products in Sunnyvale, CA and has been with the company for the past year. Bruce defines new product needs, writes application notes, resolves customer problems, and is involved with company seminars. He holds an EET degree from Heald Engineering College (San Francisco, CA). In his spare time, Bruce enjoys chess, skiing, motorcycle road racing, and military history.

Table 2—Frequency limits for standardcore materials

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Core Material</th>
</tr>
</thead>
<tbody>
<tr>
<td>To 100 kHz</td>
<td>Standard iron powders and steel tape</td>
</tr>
<tr>
<td>To 200 kHz</td>
<td>Low-permeability, high-frequency iron powders</td>
</tr>
<tr>
<td>To 400 kHz</td>
<td>High-flux molypermalloy powders</td>
</tr>
<tr>
<td>To 500 kHz</td>
<td>Standard molypermalloy powders</td>
</tr>
<tr>
<td>To 1 MHz</td>
<td>Manganese-zinc ferrite</td>
</tr>
<tr>
<td>To 10 MHz</td>
<td>Nickel-zinc ferrite</td>
</tr>
</tbody>
</table>

Article Interest Quotient (Circle One)
High 485 Medium 486 Low 487
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An object-oriented show and tell

Chris Terry, Associate Editor

“Object oriented” was the marketing buzzword a year ago and The Wall Street Journal dubbed it “the computer industry’s equivalent of oat bran.” The term has moved beyond that to become the description of an approach to software design that is serious, important, and, above all, practical.

Many principles of object-oriented programming (OOP) have been around for a long time. Encapsulation, for example, has for many years meant you can hide the details of how a routine works from other routines that don’t need to know (and should not be able to change) those details. Michel Floyd, manager of CAE product development at Integrated Systems Inc, comments that languages such as Modula-2 permit the encapsulation of procedures but rarely encapsulate data with those procedures, because the data has to be available to many different procedures.

OOP demands a radically different way of thinking, however. Object A can request object B to perform some action (such as drawing itself on the screen) without object A’s knowing anything about how the action will be performed. Further, you can group objects that share all or most of their attributes into a class. Floyd comments that in the fields of simulation and modeling, object-oriented principles make it relatively easy to mimic objects and phenomena of the real world, and that these principles enforce clarity of thought. Floyd cautions, however, that it takes most people six to eight months to learn to think in object-oriented terms.

It’s possible to write object-oriented programs in some of the standard programming languages such as C, which is not particularly easy, or Turbo Pascal 5.5, which has object-oriented extensions for that purpose. However, you won’t be able to make full use of object-oriented features unless the language itself supports them. Purists will recommend that you use a “pure” object-oriented language, such as Smalltalk/V or Eiffel. These complete development systems include an editor, a syntax checker, a browser, and a class library. The class library contains most of the objects and classes that you’re likely to need for general application programs. The editor and syntax checker and, indeed, the nature of the languages themselves, combine to guide you into good OOP practices and signal any gross violations of OOP principles. Thus, they are very helpful to the novice.

These integrated systems have several disadvantages, however. One of them is the need to learn a new programming language; another is the general opinion that Smalltalk is better suited to small projects than to large ones. Further, Smalltalk does not make it particularly easy for you to interface to programs that were written in another language. Eiffel does have some facilities for interfacing to other languages, but they are not as comprehensive as the facilities of C++.

OOP purists tend to sneer at hybrid languages, such as C++ and Turbo Pascal with Objects. Nevertheless, hybrids have the advantage of a relatively simple tran-
Object-oriented programming has become an approach to software design that is serious, important, and above all, practical.

Jeff Kantor, manager of advanced applications development at Iconix Inc, points out that every application needs interfaces to other languages or to programs running on other machines. In cross-development systems, you need to be able to optimize some code for the development system and other code for the target system; often this requires access to the low-level routines that drive the hardware. C and C++ give you these interfaces and links very easily. Smalltalk, on the other hand, deals in higher-level abstractions and therefore encourages isolation from the hardware.

Some vendors of software-development tools for object-oriented software take no stance on the choice of language, but provide tools for both Smalltalk and C++. Parcplace Systems, for example, offers both Objectworks/Smalltalk and Objectworks/C++. Objectworks can help you create color-graphics applications for heterogeneous networks running under standard windowing systems. This integrated development system adheres to the standard conventions of Smalltalk, but has features that make it easier to create larger systems than you could do with the Smalltalk/V development tools. Also, for each version of Objectworks, Parcplace provides a set of class libraries that is available as a separate item.

But the winner is . . .

Just as C is currently the language of choice for programmers who use standard structured-analysis and structured-design methods to design all kinds of systems and application programs, so C++ is well on the way to becoming the language of choice for people who design object-oriented systems and applications.

A few months ago, you might have thought that far more development systems and tools were available for Smalltalk than for C++; this is no longer the case. Table 1 lists almost twice as many compilers, libraries, and add-on tools for C++ as for other object-oriented languages. Although a few items on both sides may have been inadvertently omitted, the 2:1 ratio is likely to change even more heavily toward C++ during the next few months.

The significant change is in the increase of class libraries for C++. Because Smalltalk has been around for nearly 15 years, the class library that comes with Smalltalk/V is huge. However, for C++ there were, until a few months ago, only the somewhat limited AT&T Standard class library and the C++ class library produced by the National Institute of Health.
Manufacturers of object-oriented software-development tools

For more information on object-oriented software-development tools such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN’s Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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<td>$1195</td>
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<td>Comeau Computing</td>
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<td>$250</td>
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<td>CASE tool for Macintosh computers; handles object-oriented analysis in addition to most other CASE methodologies.</td>
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<td>Microway</td>
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<td>evaluate the relationships between various aspects of any project,</td>
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<td>process, or problem. Can also be used as software-design tool.</td>
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<td>Unix</td>
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<td>Development system for embedded systems written in Smalltalk/V. Allows a</td>
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<td>Netware</td>
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<td>project team to work concurrently on different parts of the same projects.</td>
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<td>Library systems track both source and object code and protect completed</td>
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<td>classes and applications from accidental changes.</td>
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<td>Turbo Pascal 5.5 code.</td>
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<td>OS/2</td>
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<td>design tool automatically generates C++ header files and database schemata.</td>
</tr>
<tr>
<td>Oregon Software</td>
<td>Oregon C++</td>
<td>80386, Unix and Sun-3</td>
<td>$895, $1700</td>
<td>Native compiler that compiles directly from C++ source without translation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>to ANSI C. Comes with source-level debugger compatible with C++, ANSI C,</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>and K&amp;R C.</td>
</tr>
<tr>
<td>Parcplace Systems</td>
<td>Objectworks\C++ and Objectworks\Smalltalk</td>
<td>Sun-OS, Windows</td>
<td>$3500, $3500</td>
<td>Integrated development system to help C++ designers. Conforms to AT&amp;T spec</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.1. Comes with a graphical source browser and visual debugger; allows you</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>to use traditional Unix tools as well as the optional Objectworks\C++</td>
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<td>class libraries.</td>
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<td>PMI</td>
<td>Data ++</td>
<td>Windows</td>
<td>$189</td>
<td>Library containing more than 160 classes for development of user interfaces.</td>
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<td>MS-DOS</td>
<td></td>
<td>Works with a variety of C++ compilers.</td>
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<td>Saber Software</td>
<td>Saber C++</td>
<td>Unix</td>
<td>$3995 for single user</td>
<td>Compiler conforms to AT&amp;T spec 2.1. Comes with source-level debugger and</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>class, cross-reference, data, and program browsers, Can be used with IDE's</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>Software through Pictures.</td>
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<td>Facets</td>
<td>Sun-OS</td>
<td>$1000</td>
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<td>of Objectworks/Smalltalk applications. Includes complete source code and</td>
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<td></td>
<td>an on-line, context-sensitive help system. Includes schema designer, forms</td>
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<td>designer, report writer, and menu builder.</td>
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<td>Zinc Interface Library</td>
<td>MS-DOS</td>
<td>$200</td>
<td>Class library for C++ applications. Provides event-manager and window-</td>
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<td></td>
<td></td>
<td>OS/2 Windows</td>
<td></td>
<td>manager classes, together with complete help and error systems.</td>
</tr>
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<td>Zortech C++</td>
<td>MS-DOS</td>
<td>$450</td>
<td>Native compiler for 80386-based computers running MS-DOS or Unix. Conforms</td>
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<td></td>
<td></td>
<td>Unix</td>
<td></td>
<td>to AT&amp;T spec 2.1. Developer's edition includes C and C++ compilers, C++</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>debugger, C++ Tools, and source code for the class library.</td>
</tr>
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</table>
Object-oriented programming demands a radically different way of thinking—it takes most people six to eight months to learn to think in object-oriented terms.

The picture is quite different today because there now are not only C++ class libraries organized along the lines of the Smalltalk library but also some useful specialist class libraries (Ref 1).

The predominance of C++ is further confirmed by the fact that several major CASE tool vendors have announced plans to integrate existing or upcoming C++ development systems into their CASE tool frameworks. For example, Interactive Development Environments is forming an alliance with Saber Software so that Software through Pictures will support not only Saber C but also Saber C++. Cadre, too, is allying itself with Saber so that the Teamwork tools will facilitate the design of object-oriented systems that will be implemented with the aid of the Saber C++ development tools.

Not to be outdone, Hewlett-Packard is offering a C++ version of its Softbench framework that will support object-oriented design and program development on all HP computers that run under HP/UX (HP's version of Unix). The C++ Softbench package consists of Framework LSI (a tool that allows diverse third-party tools to work together on a heterogeneous network), Encapsulator (for adapting individual tools to the Softbench framework), a class and object builder, a browser for finding and examining classes, a static analysis tool, and a graphics editor.

Another indication of the trend toward C++ is that several object-oriented database managers not only provide an interface to related application programs written in C++, but are themselves written in that language. Objectdesign's Objectstore is a typical example of such ODBMS (object-oriented database management system) packages. It can handle persistent data as fast as transient data, and it provides a DML (data manipulation language) preprocessor that is based on the AT&T cfront C++ preprocessor. Objectdesign has signed a strategic alliance with Saber Software to integrate Objectstore with both Saber C and Saber C++.

Objectdesign's DML preprocessor supports parameterized types—that is, a system of templates designed by AT&T's Bjarne Stroustrup for defining container classes. These templates make it easier to design libraries of safe and reusable code—an important step toward wider use of standard software libraries. The ANSI X3J16 subcommittee has decreed that parameterized types will be part of the initial C++ standard. Also, AT&T has announced that it has licensed Objectdesign's implementation of parameterized types for inclusion in C++ Release 3.0. This inclusion of a ready-made mechanism in the compiler will help to accelerate wide distribution of the technology throughout the C++ community.

Another vote for C++ was cast at the OOPSLA
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There seems to be no lack of proposed notations for object-oriented design. The trouble is that few of them agree with each other.

1990 conference, when Objectivity Inc announced that its Objectivity/DB engineering-database management system would support Hewlett-Packard's C++/Softbench for the development of applications to run on HP 9000 workstations.

And finally, Ontologic's Ontos 2.0 ODBMS, which runs on Sun, Apollo, DEC, and high-end 80386-based computers, is written in C++, supports multiple inheritance, and supports data distribution across networks. The package includes a development tool that automatically generates both C++ header files and database schemata, and a graphical browser that allows you to perform interactive inspection and maintenance of the database.

Just in CASE . . .

Although most modern CASE tools let you use a variety of methodologies, each with its own conventions for graphical notation, no standard notation has yet emerged for object-oriented design. You can use one of the standard notations, such as Yourdon/DeMarco, Hatley/Pirbhai structured design for real-time systems, or Chen Entity Relationship diagrams for databases. But these do not always entirely meet your object-oriented needs.

There seems to be no lack of proposed notations for object-oriented design. The trouble is that few of them agree with each other. Fewer still have powerful enough backing to ensure widespread adoption. Meilir Page-Jones began a recent article (Ref 2): "Last week we went to an object-oriented symposium . . . where we met a most unusual software engineer. He didn't have his own object-oriented design notation!"

However, there are two proposals from sources prestigious enough to ensure serious attention: one comes from Meilir Page-Jones, Larry Constantine, and Steven Weiss (Ref 2); the other from Anthony J Wasserman and his colleagues at IDE (Ref 3). It's very doubtful if either of these notations (or any other, for that matter) will become the sole standard. Most likely, several notations will eventually obtain sufficient acceptance to be regarded as de facto standards for particular types of applications. This will duplicate the situation in the structured-analysis/design field, in which engineers and organizations adopt the methodology and notation that best suits their ways of thinking and the kind of work they are doing.

Meanwhile, more and more engineers keep coming up with ideas (some half-baked, others very mature and practical). A good sign for the maturation of object-oriented technology was the formation of the Object Management Group (OMG), quartered in Framingham, MA. This organization now has more than 80 members drawn from systems vendors, software developers, and software users. November 1990 saw the publication of OMG's Object Management Architecture Guide, which provides a complete architectural overview of an object-oriented environment and the major interfaces necessary to facilitate interoperability and extensibility. The guide includes a glossary of the terms used. Because this guide was the collaborative effort of many OMG members, there is hope that OMG will have a screening and stabilizing influence that may lead to the development of common ways of looking at objects and common ways of implementing methods. Until there is wide acceptance of relatively standard approaches, there is little hope of achieving any large body of genuinely machine-independent and reusable code.

References
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Multiplier lowers impedance

Ian Hickman
Ian Hickman Partners, Waterlooville, UK

The Cockcroft-Watson voltage multiplier (Fig 1a) can produce a large negative voltage—hundreds of kilovolts—where the peak voltage across each diode and capacitor equals the p-p input voltage. However, for lower voltage applications—as low as a hundred volts—some disadvantages predominate. Fig 1a’s circuit exhibits a high-output impedance due to the small effective capacitance of the series-connected capacitors, and it exhibits considerable voltage loss due to all of the diode drops. Further, this circuit requires 2n diodes and 2n capacitors to produce a dc output voltage approximately n times the rail voltage.

Fig 1b’s circuit multiplies more effectively using fewer diodes and capacitors. The parallel arrangement of the capacitors lets you use smaller capacitors than those required in Fig 1a. Alternatively, when using the same capacitor values of Fig 1a, the output impedance will be lower. Second, whereas the clock source directly drives only one of the two strings of capacitors in Fig 1a, Fig 1b’s clock drives both strings with opposite phases. This drive scheme doubles the voltage per stage of two diodes. A final diode is necessary to pick off the dc output voltage because both strings of capacitors now carry the p-p ac input-voltage waveform. The ICL7667 dual-FET driver accepts a TTL drive swing and provides a low-impedance push-pull drive to the diode string. This low impedance is particularly helpful when using a long string to raise output voltage to more than 100V starting from a low rail voltage.

Fig 1b requires n + 1 diodes and n + 1 capacitors to output a nominal voltage equal to n times the rail voltage. Using a rail voltage of 5V, Fig 1b requires less than half the number of Fig 1a’s diodes and capacitors because of the improved circuit’s increased output per stage resulting from fewer numbers of diode forward-voltage drops in the circuit. To use Fig 1b to produce a positive output, reverse the polarities of the capacitors and diodes and tie the anode of D1 to the positive rail. Such a positive-output circuit can produce 45V from a 15V input using three capacitors and three diodes—n = 2. (EDN BBS/DI_SIG #966)

EDN

To Vote For This Design, Circle No. 746

Fig 1—The multiplier in b improves upon the conventional circuit in a by exhibiting lower impedance and by requiring fewer capacitors—or alternatively, smaller valued capacitors—and fewer diodes.
Divider splits the divisor

Yongping Zia
Department of Electrical Engineering,
West Virginia University, Morgantown, WV

Fig 1 is yet another variant of a standard digital divider. This circuit, instead of dividing by an integer, divides the input signal by $n + rac{1}{2}$. With the feedback connections exactly as Fig 1 shows, the circuit divides by 3.5. Point C in Fig 1 ultimately controls when the input clocks the 74HC161 4-bit counter. When $C = 0$, the positive edge of the input triggers the counter. If $C = 1$, the negative edge of the input triggers the counter. Each time that point C changes level, the circuit shortens the output pulse width of the counter by half of an input cycle. Thus, the counter’s divisor depends on how many changes occur at point C during one output period.

Although Fig 1 divides by 3.5, feeding back different counter outputs produces different divisors. Generally, an $m$-bit binary counter with pure exclusive-OR (XOR) feedback can form a $n + rac{1}{2}$ counter where $n$ ranges from $2^{m-2} + rac{1}{2}$ to $2^{m-1} - rac{1}{2}$. The divided output is available at the $m-1$ bit of the counter. Table 1 lists the XOR feedback terms necessary to produce various $\frac{1}{2}$ dividers. For example, to divide by 18.5, you need to XOR the following counter outputs together: $Q_0$, $Q_2$, $Q_3$, and $Q_5$. Such a divider requires using a 6-bit binary counter, and the divided output appears at $Q_1$.  

![Figure 1 - Feeding back counter outputs and XORing them with the input produces a counter that divides by $n + \frac{1}{2}$.](image)

<table>
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<th>Divide number</th>
<th>Feedback signal(s)</th>
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<tr>
<td>$N=1.5$</td>
<td>$Q_0$</td>
</tr>
<tr>
<td>$N=2.5$</td>
<td>$Q_0$ $Q_2$</td>
</tr>
<tr>
<td>$N=3.5$</td>
<td>$Q_0$</td>
</tr>
<tr>
<td>$N=4.5$</td>
<td>$Q_0$ $Q_3$</td>
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</tr>
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<td>$N=6.5$</td>
<td>$Q_1$ $Q_2$</td>
</tr>
<tr>
<td>$N=7.5$</td>
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</tr>
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<td>$N=20.5$</td>
<td>$Q_0$ $Q_1$ $Q_2$</td>
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<th>TUF-1</th>
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</tr>
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<td>6.6</td>
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<tr>
<td>ISOLATION (db) typ.</td>
<td>42</td>
<td>47</td>
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<td>$3.95</td>
<td>$4.95</td>
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8051 μC converses with dual-port RAM

Brady Barnes  
*Inter-Tel Inc, Chandler, AZ*

Interfacing an 8051 microcontroller to a dual-port RAM poses some problems that a small amount of glue logic can solve (Fig 1). The main problem has to do with the busy signal, DPR_BZ, that the dual-port RAM generates. When the 8051 attempts to access a location in the RAM that is currently being accessed by another processor, the RAM asserts the DPR_BZ signal to alert the 8051 that it must wait until the other processor’s access is complete. Unfortunately, the 8051 can’t wait because it doesn’t provide for asynchronous bus control. External gating (Fig 1) and some extra software are necessary for proper communication between the two devices. The 8051’s RAM-access code is simple (Listing 1). The 8051 software checks the status of the busy signal, and if the RAM is busy, the software tries again to access the location.

The new circuitry and software must meet two objectives. When the RAM asserts the busy signal, the 8051 must first recognize the busy signal, and then not write to the RAM accidentally. The busy signal generated by the RAM is not a latched signal. Thus, depending on the timing of the two processors that access the RAM, the busy signal can last from ten or

---

**Listing 1—8051 to dual-port RAM interface code**

```assembly
LOOP1 MOVX @DPTR, A   JB P3.1, LOOP1
LOOP2 MOVX A, @DPTR   JB P3.1, LOOP2

Write a byte of data to the DPR. Was the DPR busy? If it was busy, try again.

Read a byte of data from the DPR. Was the DPR busy? If it was busy, try again.
```

---

**Fig 1—Glue logic and software enable an 8051 microcontroller to interface with a dual-port RAM properly.**
Gain Trimming In Instrumentation Amplifier Based Systems – Design Note 51

Jim Williams

Gain trimming is almost always required in instrumentation amplifier based systems. Gain uncertainties, most notable in transducers, necessitate such a trim.

Figure 1, a conceptual system, shows several points as candidates for the trim. In practice, only one of these must actually be used. The appropriate trim location varies with the individual application.

Figure 2 approaches gain trimming by altering transducer excitation. The gain trim adjustment results in changes in the LT1010’s output. The LT1027 reference and LT1097 ensure output stability. Transducer output varies with excitation, making this a viable approach. It is important to consider that gain “lost” by reducing transducer drive translates into reduced signal-to-noise ratio. As such, gain reduction by this method is usually limited to small trims, e.g. 5-10%. Similarly, too much gain introduced by this method can cause excessive transducer drive, degrading accuracy. The transducer manufacturer’s data sheet should list the maximum permissible drive for rated accuracy.

Figure 1. Conceptual Transducer Signal Conditioning Path Showing Gain Trimming Possibilities. In Practice, Only One Adjustment Is Required.

Figure 2. Gain Trimming by Adjustment of Transducer Excitation. This Method is Useable for Small (5-10%) Trims. Large Trims Will Cause Excessive Transducer Power Dissipation or “Starved” Outputs.
Figure 3 adjusts gain in the instrumentation amplifier stage. The fixed gain LT1101 instrumentation amplifier feeds a second amplifier where the trim occurs. As both cases show, the gain trim may be up or down. A secondary benefit of this trim scheme is that it permits optional offset summing and filtering. Note that either the inverter or follower may be set up for gain addition or reduction. The sole limitation is the signal polarity reversal imposed by the inverter case. This may be corrected by reversing the instrumentation amplifiers' inputs.

A final hardware based gain trim is shown in Figure 4. Here, the A→D reference input is scaled to the appropriate voltage by the op amp and associated components. The op amp input is usually the transducer excitation voltage or, in cases where this is not possible, a reference.

One final way to trim gain is in software. If a processor is involved in the system this is a viable alternative. The software trim does a simple code conversion on the A→D output. When using this approach utilize as much of the analog components' dynamic range as possible to avoid signal-to-noise degradation.
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twenty to as long as hundreds of nanoseconds. The busy signal's active time will never be the same for each access contention.

The interface circuit must latch this busy signal. The flip-flop, IC1B, serves this purpose. To simplify the software and make accesses to the RAM as fast as possible for the 8051, the µC must clear IC1B just prior to accessing the RAM. To accomplish this task, the 8051 must fetch an opcode from external memory, which causes the 8051's PSEN to strobe low. (PSEN is equivalent to XPRG_RD in the glue-logic circuit. The mnemonic, XPRG_RD, stands for external program memory read.) Strobing PSEN low clears the flip flop, which is now armed and waiting for the busy signal to assert itself.

Once IC1B clears, the 8051 can access the RAM, which to the controller looks like external data memory. This access causes the address decoder to assert the chip-enable signal, DPR_CS. After DPR_CS goes low, the RAM will assert DPR_BZ within 50 nsec if there is contention for the memory location.

If contention occurs, the busy signal immediately sets IC1B. Because DPR_CS depends solely on address decoding, the time between recognition of a valid address and the busy-signal assertion is 103 + 50 = 153 nsec. Allowing for another 54 nsec for the signal to propagate through the flip flop, the output of that IC1B will then respond within 207 nsec after the RAM's address becomes valid.

The address is valid 43 nsec before the negative edge of ALE. Thus, the output of IC1B when clocked by DPR_BZ will be valid within 164 nsec (207 - 43 nsec) after the negative edge of ALE. The XDAT_WR and XDAT_RDWR signals from the 8051 aren't asserted for at least 200 nsec after the negative edge of ALE. Thus, the output of IC1B will be valid at least 36 nsec before XDT_RDWR or XDAT_RDWR are asserted by the 8051. It is important that IC1B's output be valid before these two XDAT signals become active for two reasons: Together, they form the clock signal that transfers IC1B's state to IC1A, and they work to inhibit a write command to the RAM if the busy signal is active.

The circuit transfers the state of IC1B to IC1A on the negative edge of either XDAT signal. This transfer of the busy status is necessary because XPRG_RD clears IC1B shortly after DPR_CS goes high. The busy status can now be read by the 8051 through one of its ports.

To prevent an accidental write to the RAM, the 8051 must first access the write location without asserting the DPR_WR signal by asserting only the DPR_CS signal. If the RAM asserts the busy signal at this point, the output of IC1B will block the DPR_WR signal via NAND gate IC2C, and thereby prevent a write to the RAM.

If the RAM isn't busy, the DPR_WR signal must not experience a delay of more than 33 nsec in order to meet the data hold time of the RAM. The hold time of the 8051 is 33 nsec, and the required hold time of the RAM is 0 nsec. Thus, the circuit can have up to a 33-nsec delay of XDAT_WR and DPR_WR and still meet the hold time of the RAM. The WR_ signal passes through two levels of NAND gates. The circuit uses ALS logic to meet the write timing requirement. Using HC or HCT logic will not meet the 33-nsec delay requirement. However, either FAST, ACT, or ALS logic is fast enough.

Note that because this interface circuit uses the external-program-read signal from the 8051, the 8051 code that accesses the dual-port RAM must reside in external memory. (EDN BBS/DLS/IG #969)

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**Duty-cycle chopper controls lamp**

Ronald Doctors  
*GM! Inc, Santa Barbara, CA*

Fig 1's high-intensity-lamp dimmer emulates a rheostat; the circuit has only two leads. To maximize the battery-powered circuit's operation time between charges, the circuit employs a PWM system. A system with duty cycles between 20 and 95% provides the necessary brightness range. Fig 1's component values set the maximum duty cycle close to 100% and the minimum around 20%. The circuit is useful for applications in which the minimum duty cycle allows for energy storage, and in which efficiency is important (solar-powered lamps and motors, for example). To maximize efficiency, C1 charges during the off time and stores enough energy to drive Q and keep IC1 operating. Because the dimmer-control circuit is in series with the lamp, all the current passes through the lamp, which improves efficiency.

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some passive components implement the PWM circuit. One half of the TLC556, R₁, R₂, and C₂ form a free-running, 1-kHz oscillator that has a very low duty cycle. This signal triggers a one-shot comprising the other half of the TLC556, R₃, R₄, the 100k potentiometer, and C₃. Q₁ and Q₂ provide the saturated output drive. These transistors can carry 1A with a $V_{CE(SAT)}$ of 0.25V. Thus, no heat sinking is required. D₁ prevents Q₂ from dumping charge onto C₁ when Q₂ is on.

(EDN BBS/DL_SIG #967)

**Current source scrounges parts**

Philip Leong  
*Department of Electrical Engineering, University of Sydney, Sydney, Australia*

Fig 1 uses readily available parts to implement a 0-to 200-nA current source. The circuit borrows a PMOS transistor from the input stage of a CD4007A, a device easier to obtain than a discrete PMOS transistor. The CA3130 op amp operates as a follower so that its positive input sets the current that flows through R₂. The MOSFET input stage of this op amp exhibits low-input current. The op amp must be able to produce an output voltage high enough to turn the CD4007A's internal FET off. Thus, the op amp requires a positive supply voltage of 5V. The circuit presents an output voltage from 0 to 3V, and R₁ controls the amount of output current. (EDN BBS/DL_SIG #970)

(EDN BBS/DL_SIG #970)

To Vote For This Design, Circle No. 749

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**Fig 1—IC₁, a CMOS 555 timer, and associated components form a PWM circuit that adjusts the duty cycle of this lamp dimmer between 20 and 100%.

**Fig 1—This low-drift current source makes use of an input PMOS transistor inside a readily available CD4007A.
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Phase shifter adapts to frequency changes

Ion Constantinescu
B&C Microsystems Inc, Sunnyvale, CA

Fig 1's circuit adds 120 degrees of phase shift to a 50- or 60-Hz input regardless of the frequency and amplitude fluctuations of that input. The circuit configures a 2N4093 JFET as a voltage-controlled resistor whose value is proportional to the phase difference between the input and the output. The values of C1, R1, and rDS determine the amount of phase shift, 120° in Fig 1's case.

A 555 timer implements a phase detector whose two inputs are related to the input and output. The input and output, respectively, drive ICb and ICc, which operate as zero-crossing detectors. D1 and D2 limit the positive-going pulses at the 555 inputs. Thus, the falling edges of ICb and ICc's outputs control the 555 timer. The timer's output signal stays low for a time proportional to the phase shift between the circuit's input and output.

The average value of the timer's output and an off-setting voltage drive IC1o. R2 and C2 filter IC1o's output. The resultant signal controls the JFET. The potentiometer sets the control at a value for which the phase shift between input and output is equal to 120 degrees when the input signal frequency is 50 or 60 Hz. Any differences between the input and output changes the 555 output's average value, thus ultimately modifying the control voltage and the JFET's resistance.

To calibrate the circuit, apply a 50-Hz sine wave with an amplitude less than 1 Vp-p to the input and adjust the potentiometer until the phase shift reads 120° on a digital phase meter. For input frequency variations between 40 and 60 Hz, the phase shift changed by a maximum of ±0.17%, which is equivalent to an offset of only 0.02 °/Hz. The average value at IC1o's noninverting input is 3.864V.

Fig 1—The input and output of this phase shifter drive a 555 timer to maintain a constant 120° of phase shift regardless of input frequency and amplitude.

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Three ICs produce a grand prize

For Bruce Saldinger of Los Angeles, “Three ICs produce pure sine waves” produced the 1990 Design Idea of the Year. Saldinger’s October 25 Design Idea was his first submission. “I’m still in shock” he said, one week after being notified of the $1500 prize.

In Saldinger’s circuit, a TTL counter, an 8-channel analog multiplexer, and a fourth-order lowpass filter generate 1- to 25-kHz sine waves with a THD better than -80 dB. The circuit cascades two second-order, continuous-time Sallen-Key filters to implement the fourth-order lowpass filter. Two resistive dividers provide bipolar dc inputs to the multiplexer. The multiplexer produces an eight-times oversampled staircase approximation of a sine wave. Eight-times oversampling greatly simplifies the smoothing requirements of the lowpass filter by pushing the first significant harmonic out to seven times the fundamental.

The three-IC sine wave idea first came to him when he was a co-op student working at IBM in Manassas, VA. It can also be traced back to all the engineering communications-related classes he took. He says the circuit is an example of a practical solution to a principle learned in school. Saldinger says the three-IC idea also fit in well with his work at Maxim Integrated Products.

Saldinger is currently earning his MBA from UCLA. An MBA will, he says, allow him to “explore other avenues.” Saldinger has a BSEE from UC Berkeley, where he was a member of Eta Kappa Nu, a National honor society for electrical engineers. After graduating, he worked for Monolithic Memories, now Advanced Micro Devices. He wanted to work with a smaller company, so he joined Maxim to design analog ICs. Now he’s back in school full time. Saldinger says he didn’t reach a career plateau, but that he “saw it coming.” This summer he’s off to Tokyo for an internship with Sony. For prospective EE students, he recommends getting a broad background, cautioning that specialization could hold them back.

Saldinger’s main “hobby” is studying for final exams. When not studying for finals or whipping up winning circuit designs, he indulges in wind surfing and squash. —Brian Tobey

ISSUE WINNER

The winning Design Idea for the March 1, 1991 issue is entitled “Amplifier scheme lowers drift and noise,” submitted by Jim Williams of Linear Technology Corp (Milpitas, CA).

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- **EMB** - Electrical Moisture Block Pads seal the grommet area wire harnesses against the penetration of moisture with self-adhesive rubber based mastic.
- **HST** - Heat-Shrinkable Tubing insulates, seals, and provides strain relief for wire splices, in-line components, fusible links and terminals.

The New Ideas Brochure describes recent automotive technologies covering moisture sealing, insulating, interconnects with precision overmolding, flexible magnet material and powder and liquid resins. To obtain a copy, contact a 3M Automotive Trades sales representative, or call 1-800-233-3636.

Vtran is a program that loads the state/time information of simulation stimulus files and reformats the data for use by any of more than 20 widely used simulators. Version 1.5 adds new simulator interfaces for Cadat, Lasar, VLSI Technology, Toshiba, and Lsim, and new “Format String” features enhance the program’s ability to read differently formatted files. You can customize the format descriptors to describe both the input-data format and the output-data format. After loading the data, the program can perform some optional processing on the data before generating the output file. It can change the pin list, pin order, pin timing, and other parameters; the modifications may affect as many as 1024 pins. Vtran is available for Sun, Apollo, Intergraph, and IBM PC/AT computers. Single-node license, $3495.

**Source III Inc**, 4960 Almaden Expressway, Suite 147, San Jose, CA 95118. Phone (408) 997-2575.

**Autorouter For High-Speed Printed-Circuit Boards**

- **Provides table-driven crosstalk controls**
- **Automatically balances pair routing**

Spectra SP50 is an autorouter for the layout of high-speed pc boards. The program lets you construct a table of parallel rules that emulate a curve of gap versus parallel length allowed between two segments; you can use different tables for segments on the same layer and seg-
Here's how to turn a relay with 2 changeover contacts into one with 4.

The MT4, our new relay with 4 changeover contacts, hardly occupies more board space than the MT2, our relay with 2 changeover contacts.

So if you need 6 twin changeover contacts on your board, simply install an MT2 and an MT4. Two relays of virtually identical size.

And the expensive space you formerly needed for a third MT2 is now free for other important functions.

Plus: less testing, less component cost, less assembly effort, greater reliability.

What more can you want?

(The new MT4: Power consumption at 20°C 300 mW. Temperature range −55°C to 85°C. Space occupied per contact 12 M².)

I'm interested in the new MT4 relay. Please send me your literature.

Company ____________________________

Name ______________________________

Address ____________________________

Telephone __________________________

Alcatel STR AG

CH-8055 Zurich/Switzerland, Friesenbergstrasse 75

EDN 6/6/91

EDN June 6, 1991
ments on adjacent layers. This feature helps to achieve high routing completion with little or no crosstalk. For very fast dual-polarity ECL circuits, you normally have to route both polarities as a balanced pair and then fix them in place; this autorouter makes such nets subject to ripup and retry during autorouting, while maintaining conformance to all design rules. Delay considerations may require minimum lengths for some nets and maximum lengths for others. You can specify minimum or maximum lengths for individual connection, nets, or net classes, and the autorouter will observe these constraints. The features reduce the amount of manual editing required during layout and correspondingly reduce the total design time. The program runs on the Sun SPARC family of workstations, the IBM RISC 6000, and the Hewlett-Packard 9000 series 300 and 400 computers. Depending on host configuration, from $45,000.

Cooper & Chyan Technology Inc, 1601 Saratoga-Sunnyvale Rd, Suite 255, Cupertino, CA 94014. Phone (408) 366-6966. FAX (408) 252-9565. Circle No. 357

Layout Editor For Standard-Cell Autorouting
- Provides padframe generation and routing
- Performs all angle editing
L-Edit version 3 is an IC-design tool that runs on IBM PCs and compatibles. New features include built-in standard-cell placement and routing; automatic padframe generation; and padframe routing. The editor now allows you to automatically route a standard-cell ASIC, complete with padframe generation and routing, on your PC. Users of OrCAD, Viewlogic, and Tango systems can use the editor to generate ASICs from their schematic; however, you'll need the Gatesim netlist tool kit and SCMSOscmap to translate and simulate your design in schematic form. When translation and simulation are complete, L-edit uses the standard-cell library SCMSOslib to route the design into a layout-level description. In six to seven weeks, Mosis (Marina del Rey, CA) can fabricate prototypes of chips routed by L-edit for $500; several silicon foundries (including Hewlett-Packard, Orbit, and VLSI Technology) can fabricate intermediate and high-volume quantities. L-edit version 3, $995; SCMSOscmap and SCMSOslib, $295 each; Gatesim, $1295.

Tanner Research Inc, 444 N Altadena Dr, Pasadena, CA 91107. Phone (818) 795-1696. FAX (818) 795-7937. Circle No. 413

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FUSION Developer's Kit also has a flexible C-source code architecture, making it processor- and operating system-independent.

Currently used in hundreds of process control, embedded systems, and end user designs, FUSION Developer's Kit from Network Research comes with full support and porting services.

To receive a FUSION Developer's Kit information package, including data sheet, technical specifications and licensing plans call (800) 541-9508 or write to Network Research, 2380 N. Rose Ave., Oxnard, California 93030, FAX (805) 485-8204.

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Design Kit For Text-Screen Creation

- TSR program reports row/column coordinates
- Screen-design form lets you draw preliminary sketch

Screen Design Kit is a combination of software and accessories that helps you design and maintain text screens for application programs. You can pop up a TSR (terminate-and-stay-resident) program from within any application in order to see the column/row coordinates and attribute byte of any position on the screen; the report shows foreground and background colors in decimal, binary, programming codes, dBase color codes, and English. A color palette displays all of the available color combinations. These reports help you define the characteristics of your screen design very precisely. The accessories include a pad of 50 screen-design forms; these forms let you sketch out your design using exact row/column coordinates; a row/column ruler; a laminated conversion chart showing the ASCII, decimal, hex, octal, and binary codes of every available character or symbol (including box-drawing combinations). $99.95.

Butler Computer Systems, Box 5306, Walnut Creek, CA 94596. Phone (415) 256-8401.

Circle No. 358

Interactive Digital Simulator

- Performs functional simulation and timing analysis
- Runs in protected mode on 80386/486-based systems

Ultisim is an interactive digital simulator that runs in 32-bit protected mode on 80386/486-based systems with a performance comparable to that of simulators running on Unix-based workstations. The 28-state simulator provides save and restore capability, a logic analyzer-like display, and a digital waveform processor. The program comes with model libraries for TTL 54 and 74 series, ECL, CD4000, and PLD devices. The Viewtrace option, developed with Viewlogic Systems (Marlboro, MA), can perform graphical manipulation, Fourier transforms, and analog waveform processing. Three versions are available. Entry System, with a design capacity of 50 14-pin ICs, $1295; Advanced System, with a design capacity of 200 14-pin ICs, $3275; Professional System, with unlimited design capacity, $7375; Viewtrace option, $1995.

Ultimate Technology, 1725 Montgomery St, San Francisco, CA 94111. Phone (415) 391-2433. FAX (415) 391-0669. Circle No. 359

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198 CIRCLE NO. 54 EDN June 6, 1991
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- The RCM-1900—tough 19" color monitor, fits standard rack for rugged graphics anywhere. Brilliant image, resolution to 1,280 x 1,024 pixels.

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KMS Advanced Products, Inc.
700 KMS Place, Ann Arbor MI 48106-1868
CIRCLE NO. 174
RISC Workstations

- Three models use the PA-RISC processor
- Two models deliver 76 MIPS and 72.2 Specmarks

The 9000 Series 700 consists of three models of workstations that use the company’s PA-RISC (Precision-Architecture Reduced-Instruction-Set-Computer) processor. The entry-level desktop Model 720 runs at 50 MHz and delivers 57 MIPS, 55.5 Specmarks, and 17M flops. The desktop Model 730 and the desk-side Model 750 run at 66 MHz and deliver 76 MIPS, 72.2 SPECmarks, and 22M flops. Both desktop models have 128k-byte instruction and 256k-byte data caches and as much as 64M bytes of RAM with error-correction code (ECC). In addition, the desktop models have as much as 840M bytes of internal disk storage and accommodate 10G bytes of disk capacity. The desk-side Model 750 has 512k bytes of cache and as much as 192M bytes of ECC RAM. The Model 750 has as much as 2.6G bytes of internal disk drive and accommodates 40G bytes of disk capacity. The Model 720 and 730 each have one EISA slot, and the Model 750 has four EISA slots. Model 720 with a 400M-byte disk, from $15,990; Model 730 with two 400M-byte disks, from $23,990; Model 750 with 660M-byte disk, from $39,690.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. Circle No. 360

Image Processor

- Three parallel 25-MHz processors achieve 75-MHz rate
- Averages as many as 256 frames in real time

The DT2867 frame grabber and frame processor on a single 16-bit ISA bus board contains three parallel 25-MHz processors, each containing its own ALU and multiplier. The combination achieves a 75-MHz pixel-processing speed. Because the board can process three pixels simultaneously, it performs a 3 × 3 convolution on a 640 × 480-pixel image in less than 1/15 sec. The ALUs have 16-bit accuracy and a 1M-byte processing buffer, which allows the board to average as many as 256 frames in 1/30 sec. In addition, the processor executes histograms in 1/30 sec and can store as many as four separate histograms. The board digitizes images from video cameras and VCRs and stores the images in one of two 512k-byte frame buffers. $6995. A Windows 3.0 software package, called Global Lab Image, will be available in September for $2495.

Data Translation, 100 Locke Dr, Marlboro, MA 01752. Phone (508) 481-3700. Circle No. 361

VGA To Video Board

- Converts VGA output to NTSC or PAL video signals
- Runs independent of the host

The Tapecaster 8-bit ISA bus board converts a VGA output signal to either NTSC or PAL video-formatted signals. A hardware design that doesn’t require software lets you simultaneously view the data on a VGA-compatible monitor while recording data on a videotape. The board uses crystal-controlled frequency sources, which provide a precise NTSC or PAL output frequency. The board also has a Super VHS output. By converting all VGA modes having a maximum resolution of 640 × 480 pixels, the board allows VGA video windows and color to be faithfully reproduced. The video quality is limited only by the NTSC and PAL standards. $750.

Redlake Corp, 15005 Concord Circle, Morgan Hill, CA 95037. Phone (800) 543-6563; in CA, (408) 779-6464. FAX (408) 778-6256. Circle No. 362

EDN June 6, 1991
Smaller. Denier. Faster. This is Super Circuit sophistication at its finest, and is a prime reason you should consider SMT combined with Multiwire® Interconnection Technology. In this day of higher density silicon chip integration and higher speeds, circuit boards need to become an active extension of the component. Multiwire Boards (MWB®) are the next logical step. Using uniform 0.1 mm diameter insulated copper wire for signal interconnection, MWB can routinely accommodate super high wiring densities and high signal speeds. This allows transmission line performance characteristics while offering critical wire length and precisely controlled impedance levels. Concurrent Routing, a uniquely developed wiring technique, permits a high degree of design flexibility while achieving enhanced electrical performance, especially where high signal speeds and crosstalk management are critical.

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So if you need super technology for your applications, turn to Hitachi Chemical, the pioneer of Super Circuit Boards and all of the materials that make them so super!
**80486 EISA Computers**
- Contain 4M bytes of RAM expandable to 32M bytes
- Have one 8-bit ISA and seven EISA slots in AMI’s BIOS

The ME 486-EISA/25 and ME 486-EISA/33 are EISA bus computers containing 25- and 33-MHz 80486 µPs, respectively. Standard configurations include 4M bytes of RAM; 128k bytes of external cache RAM; an extended VGA card and a color monitor capable of 1024 × 768-pixel resolution with 256 colors; a 150M-byte ESDI hard-disk drive; an EISA disk controller with cache; 1.44M-byte, 3½-in. and 1.2M-byte, 5¼-in. floppy-disk drives; one parallel and two serial ports; either DOS 3.3 or DOS 4.01; and a choice of three keyboards. You can expand the memory on the mother board, in 4M-byte increments, to a maximum of 32M bytes. The RAM chips have 70-nsec access times and are arranged in a page mode for zero-wait-state operation. The computers use an AMI BIOS and have one 8-bit and seven EISA expansion slots. ME 486-EISA/25, $4999; ME 486-EISA/33, $5499.

**Micro Express**, 1801 Carnegie Ave, Santa Ana, CA 92705. Phone (714) 852-1400. FAX (714) 852-1225.

**Circle No. 363**

**80386SX Single-Board Computer**
- Executes IBM PC-compatible software on the VMEbus
- Runs at 20 MHz and has 1M, 4M, or 8M bytes of RAM

The XVME-686 PC/AT single-board computer (SBC) for the VMEbus uses a 20-MHz 80386SX µP and 1M, 4M, or 8M bytes of RAM. It executes IBM PC-compatible software. Its operating temperature ranges from 0 to 65°C. The board contains both a VMEbus and an ISA bus hardware interface; an IDE hard-disk controller; a controller for two floppy disks; a 16-bit VGA graphics controller; a socket for an 80387SX coprocessor; two serial ports; a Centronics parallel port; and a watchdog timer. Other features include VMEbus Slot 1 functions and a VME interrupter and interrupt handler. The board can access the short I/O, standard,
or extended address space. The
hardware byte-swapping feature
handles byte-ordering differences
between conventional VMEbus
680xx CPUs and the 80386SX µP.
From $3500.

**Xycom Inc**, 750 N Maple Rd, Sal­
line, MI 48176. Phone (800) 367-
7300; in MI, (313) 429-4971. FAX
(313) 429-1010. Circle No. 364

**Graphics Controller Board**

- **Uses TMS34020 chip and
displays 1024 × 1024 pixels**

- **Provides from 15.7 to 63 kHz**

   The VCF-V graphics controller
   board for the VMEbus uses TI's
   TMS34020 graphics chip to display
   1024 × 1024 pixels; the display has
   a depth of 8 bits. The 6U board also
   provides an overlay of 1024 × 1024
   pixels having a depth of 4 bits. The
   number of addressable pixels is ex­
   pandable to 2048 × 2048 pixels,
   which can produce multiple-page
displays. A write-mask register
write protects individual bit planes.
You can expand the standard dis­
play memory from 1M to 8M bytes,
and you can opt for a TMS34082
floating-point unit. Both the graph­
ics chip and the host processor have
access to the dual-port video RAM ,
which the board uses for display
memory. The board also handles in­
terrupts from the host, an onboard
SCSI controller, and a serial I/O
port. $1900.

**Peritek Corp**, 5550 Redwood Rd,
Oakland, CA 94619. Phone (415)
531-6500. FAX (415) 530-8563.
Circle No. 365

**DSP Evaluation Module**

- **Operates as fast as 40 MHz for
TI's TMS320C51 chip**

- **Lets you develop, debug, and
benchmark algorithms**

   The EVM320C5X DSP evaluation
   module for TI's TMS320C51 chip
   operates at 40 MHz and executes
   20 MIPS. It has 16k bytes of zero-
   wait-state RAM for data and for
   programs, respectively. Both
   RAMs are expandable to 64k bytes.
   A 96-pin DIN expansion connector
   provides access to all of the DSP
   signals. The connector is an inter­
face to a series of companion mod­
ules that aids hardware and soft-
ware development.

---

Our multi-national customers see Ken Talentino as their link to a wide spectrum of connector products. But

they don't see all the people he relies upon for on-time delivery and zero defects. There's

- Chris testing ribbon cable assemblies.
- Tami quoting environmental connectors.
- Cathy watching over filter connectors. And
- Bernie who markets RF connectors. While Bill designs overmolded cable assemblies. These are just some of the key connections that make Amphenol a world class manufacturer, and second to none when it comes to customer service.
ware development. One companion module contains TI's TLC3204X analog interface circuit. In addition, a prototype module lets you develop custom circuitry. The stand-alone evaluation module communicates with an IBM PC-compatible symbolic debugger via an RS-232C port. The PC must have either a 286 or a 386 µP, 512k bytes of available RAM, a hard-disk drive, a 5½-in. floppy-disk drive, a color-monitor adapter, and either PC- or MS-DOS 3.0 or higher. $1495.

Spectrum Digital Inc, Box 1559, Sugar Land, TX 77487. Phone (713) 561-6952. FAX (713) 561-6037.

Circle No. 366

Graphics Controller Board

- Uses a TI TMS34020 chip to draw 4M pixels/sec
- Meets Mil-Specs for military applications

The PMV 68 GDP-1 VMEbus graphics controller board meets Mil-Specs for shipboard, ground mobile, and airborne applications. It uses TI's TMS34020 chip to draw 4M pixels/sec, and it generates fill patterns and vectors. The board comes with as much as 3M bytes of dual-port video RAM for display memory. An additional 1M byte of dual-ported RAM provides the interface between the VMEbus and the TMS34020 chip. The board can display either 768 x 574 or 1280 x 1024 pixels. An 8-bit-deep display buffer provides 256 simultaneous colors from a palette of 16.7M colors. The board also accepts composite-video signals from an external source, such as an FLIR sensor, to overlay the signals on its local graphics and display the superimposed image. $6920. Delivery, eight weeks ARO.

Radstone Technology Corp, 20 Craig Rd, Montvale, NJ 07645. Phone (800) 368-2738; in NJ, (201) 391-2700.

Circle No. 367

DSP Boards

- Use TI TMS320C50 or TMS320C51 DSP chip
- Have 16k x 16-bit RAM

The TMS320C50 system and processor boards are DSP boards for the 16-bit ISA bus; they use either a 40-MHz TMS320C50 or TMS320C51 DSP chip. The boards contain a 16k x 16-bit program and a 16k x 16-
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Korea 82-2-868-0147 (FAX 82-2-868-8600)
Singapore 65-353-8312 (FAX 65-353-8315)

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50-pin connector that permits high-speed 16-bit parallel data transfers. Both boards contain TI’s test bus controller chip, which enables JTAG (Joint Test Action Group) boundary scanning. System board, $3495; processor board, $2495.


Motor Controllers
- Let a host control as many as 31 motors on a network
- Host communicates with multiple drives over an RS-485 link

The TR Node peripheral board controls a servo or variable speed motor. As many as 31 boards operate as nodes on a TR Network that uses a host computer for intelligence. The host computer runs a motion-control program to communicate with the nodes over an RS-485 serial link at a user-selectable rate of 115.2 or 38.4k baud. Each node on the TR network responds to a move-on-demand command set. Each node can interpolate points on a motion profile and synchronize the motor’s speed and position to other motors on the network. The 3.94 x 3-in. control boards accept TTL inputs from an incremental encoder either as a stream of pulses or as quadrature signals. Board and L-bracket mount, $371 (100).

Teknic Inc, 214 Andrews St, Rochester, NY 14604. Phone (716) 546-3212. Circle No. 369
A question for designers who aren't yet using high-performance µPLDs.

Ever feel like your system designs aren't quite up to speed, so to speak? It's probably not your fault. Because PLDs have typically forced designers to sacrifice performance to achieve higher integration.

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In fact, with $t_{PD}$ figures as low as 10ns, Intel's 16-macrocell 85C060 and 24-macrocell 85C090 are, without question, the fastest integrated PLDs in the industry.

So what are you waiting for? Call (800) 548-4725 and ask for Literature Packet #1A81.

We'll send you everything you need to know about how to improve system performance. Without delay.

Why the big delay?

<table>
<thead>
<tr>
<th>PLD Performance</th>
<th>$t_{PD}$</th>
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<tr>
<td>Intel 85C060</td>
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<td>Intel 85C090</td>
<td>15ns</td>
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<td>EP910</td>
<td>33ns</td>
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</tbody>
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COMPONENTS & POWER SUPPLIES

Slide Switches
• Rated for 4A
• Available in single- and double-pole versions
L Series miniature slide switches feature an all-enclosed plastic construction. Power-rated models are UL recognized and CSA certified, and have ratings ranging to 4A at 125V ac. The line also includes versions that are designed for low-level switching applications. Single- and double-pole versions are available in 2-, 3-, and 4-switch configurations. Housing material is 6/6 nylon, which has a 94V-2 UL rating. The switches feature a built-in positive-detent mechanism. They’re available with gold-plated contacts for low-level switching applications and with silver-plated contacts for power service. Electrical life measures 10,000 make-break cycles at full load. Insulation and dielectric strength equal $10^6 \Omega$ min and 1000V rms, respectively. Single-pole models, $0.52; double-pole versions, $0.74 (1000).

VMEbus Backplane
• Accommodates 100-MHz system speeds
• Utilizes 11-layer construction
This J1 backplane is designed to support 16-bit implementations in VMEbus applications. The device can accommodate 100-MHz system operating speeds. Although the unit has only a 3U height, it features all the capabilities normally found on a 6U monolithic backplane. It utilizes 11-layer stripline construction and is designed to be fully backward-compatible with existing VME backplane designs. The device is also fully compliant VMEbus specification IEEE P1014, draft 3.0, revision D. $590.

Bicc-Vero Electronics Inc, 1000 Sherman Ave, Hamden, CT 06514. Phone (203) 288-8001. FAX (203) 287-0062. Circle No. 371

Servoamplifier
• Develops a $\pm 12A$ at $\pm 75V$ peak output
• Has 95% efficiency
The Model 303 PWM servoamplifier is designed for fractional horsepower motion-control applications. It operates from a single-polarity supply (16 to 80V) and develops a 4-quadrant continuous output of $\pm 6A$ at 75V; for applications involving fast motor acceleration, the unit can develop a peak output of $\pm 12A$. The amplifier’s 22-kHz switching frequency puts motor-hum noise beyond the human hearing range. The 3-kHz bandwidth maximizes servo accuracy, and the 95% efficiency simplifies cooling requirements and expands mounting options. The amplifier features a user-configurable gain-bandwidth response; users can tailor the response with a single resistor. The unit can function as a current or voltage source. Measuring 6.7 \times 4 \times 1.1 in., the amplifier can be mounted on pc boards, on equipment bulkheads, or edgewise in bookshelf fashion. The device is also compatible with Eurocard assembly requirements. $275.

Copley Controls Corp, 410 University Ave, Westwood, MA 02090. Phone (617) 329-8200. FAX (617) 329-4055. Circle No. 372
Universal 85-270v Input
AC/DC Power Supplies

SRW SERIES FEATURES:
- Low Profile
- One to Four Outputs
- FCC/VDE Level “B” Input Filter
- All Models UL, CSA and TUV Certified or Under Evaluation
- Optional Chassis & Cover

Compact 3” x 5” x 1.12” size

45 watt

<table>
<thead>
<tr>
<th>Model No.</th>
<th>Output 1</th>
<th>Output 2</th>
<th>Output 3</th>
<th>Output 4</th>
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<td>-5V@2A</td>
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<td>+5V@5A</td>
<td>-5V@2A</td>
<td><a href="mailto:+15V@0.7A">+15V@0.7A</a></td>
<td><a href="mailto:-15V@0.7A">-15V@0.7A</a></td>
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<td>+15V@1A</td>
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<td><a href="mailto:-5V@0.7A">-5V@0.7A</a></td>
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Compact 4” x 6” x 1.12” size

65 watt

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<tr>
<th>Model No.</th>
<th>Output 1</th>
<th>Output 2</th>
<th>Output 3</th>
<th>Output 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRW-65-4001</td>
<td>+5V@5A</td>
<td>-5V@3A</td>
<td>+12V@2A</td>
<td>-12V@2A</td>
</tr>
<tr>
<td>SRW-65-4002</td>
<td>+5V@5A</td>
<td>+12V@1A</td>
<td>+12V@2A</td>
<td>-12V@2A</td>
</tr>
<tr>
<td>SRW-65-4003</td>
<td>+5V@5A</td>
<td>+12V@1A</td>
<td>+15V@2A</td>
<td>-15V@2A</td>
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<tr>
<td>SRW-65-4004</td>
<td>+5V@5A</td>
<td>+24V@1A</td>
<td>+12V@2A</td>
<td>-15V@2A</td>
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<tr>
<td>SRW-65-4005</td>
<td>+5V@5A</td>
<td>+24V@1A</td>
<td>+15V@2A</td>
<td>-15V@2A</td>
</tr>
<tr>
<td>SRW-65-4006</td>
<td>+5V@5A</td>
<td>+24V@1A</td>
<td>+15V@2A</td>
<td>-15V@2A</td>
</tr>
</tbody>
</table>

Compact 4.25” x 7”x 1.25” size

115 watt

<table>
<thead>
<tr>
<th>Model No.</th>
<th>Output 1</th>
<th>Output 2</th>
<th>Output 3</th>
<th>Output 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRW-115-4001</td>
<td>+5V@12A</td>
<td>-5V@4A</td>
<td>+12V@4A</td>
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<td>SRW-115-4002</td>
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<td>SRW-115-4003</td>
<td>+5V@12A</td>
<td>+24V@1A</td>
<td>+15V@3A</td>
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<td>SRW-115-4004</td>
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<td>+24V@1A</td>
<td>+15V@3A</td>
<td>-15V@2A</td>
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<tr>
<td>SRW-115-4005</td>
<td>+5V@12A</td>
<td>+24V@1A</td>
<td>+24V@3A</td>
<td>-12V@1A</td>
</tr>
</tbody>
</table>

Other output combinations available, please consult factory.

Reserved your evaluation units or get additional information on our ready-to-ship universal input switchers.
Fiber-Optic Jumpers
- Available in 3-km lengths
- Have a 0.2-dB insertion loss
These fiber-optic duplex jumpers are designed to fit the company's Escon-compatible transmitter-receiver shell assembly. The units are available in lengths ranging from 3 to 3000m. The terminating connectors have a retractable shroud that provides additional ferrule protection and eases access for cleaning. A typical duplex jumper has a mean insertion loss of 0.2 dB with a standard deviation of 0.09 dB. The jumpers use a cable that features fibers with 62.5-μm cores. The units are designed to withstand pull forces of approximately 67 lbs. 3m jumpers, $250 (1000).

**Siemens Fiber Optic Components, 3846-A First Ave, Evansville, IN 47710. Phone (800) 827-3334; in IN, (812) 422-2322. FAX (812) 422-2339. Circle No. 373**

Bandpass Filter
- Has 4-MHz bandwidth
- Operates over 6 octaves
The Model APS-204 bandpass filter has a constant 4-MHz bandwidth and features continuous electronic tuning over the six octaves from 20 to 1000 MHz. The unit is an active filter and has no insertion loss. The device uses a 4-pole resonant cavity filter, which has a Q of 325, to maintain the passband width at 4 MHz, regardless of center frequency. The filter operates on 12V dc for mobile convenience and consumes just 6W. It is housed in an aluminum case, which includes an on-off switch and a 10-turn potentiometer for selecting the center frequency. Noise figure equals 10 dB max, and the third-order intercept is specified at 15 dB typ. $995.

**Optoelectronics Inc, 5821 NE 14th Ave, Fort Lauderdale, FL 33334. Phone (800) 327-5912; in FL, (305) 771-2050. FAX (305) 771-2052. Circle No. 374**

---

**We've Made A Big Change In**

![Image of an airplane]

**Introducing The MD-11.**

You'll now notice a difference in American's service from San Jose to Tokyo. It's called the MD-11. A roomy new aircraft specifically designed for long-range flights. • American will still offer the only nonstop service to Tokyo from the San Jose/Silicon Valley area. We'll continue to offer nonstops to Tokyo from Dallas/Fort Worth as well. And, along the way, you'll still enjoy our schedules subject to change.

**EDN June 6, 1991**
COMPONENTS & POWER SUPPLIES

Optical Encoders
- Designed for price-sensitive applications
- Feature a GaAlAs light source

Containing only a light source and integral sensor, MOD900 and MOD910 Series optical encoders are designed for highly price-sensitive applications. The units utilize a collimated GaAlAs LED light source and a sensing element that consists of an integrated photodiode—a phased-array optical IC. The encoder requires no interrupter masks normally associated with optical encoders—disk resolution is duplicated in diode-array format on the optical IC. Features include resolutions of 200, 500, 512, 1000, and 1024 pulses/revolution and a 100-kHz frequency response. Operating range spans -40 to +80°C, and MBTF exceeds 100,000 hours. Encoder outputs are TTL and CMOS compatible. An index output is available as an option. $15 (OEM qty).

BEI Motion Systems Co., 1755-B La Costa Meadows Dr, San Marcos, CA 92069. Phone (619) 471-2600. FAX (619) 471-2675.

Circle No. 375

Snap-Acting Switches
- Operate with 15g force
- Rated for 5A

TF-CC and CD Series precision snap-acting switches operate with forces as low as 15g. Designed to meet UL, CSA, and VDE requirements, the units are available in spst and spdt models that are rated to switch 1, 3, or 5A. Units are available with a variety of actuators including standard-pin plungers, wide-pin plungers, levers, lever rollers, and simulated rollers. Termination options include a choice of solder terminals, standard quick-connect, offset quick-connect, screw terminals, and pc-board terminals. From $1 (OEM qty). Delivery, eight weeks ARO.

Unimax, Box 152, Wallingford, CT 06492. Phone (203) 269-8701.

Circle No. 376

DC/DC Converters
- Have 200W output
- Meet military temperature-operating-range requirements

MFL Series dc/dc converters provide a 200W output-power capabil-
Simplicity of design makes Maxtor’s Cheyenne Series inch-high 80MB 7080 disk drive the most reliable in its class. Compare Maxtor’s four-head, two-platter design to Seagate’s six-head, three-platter design. Fewer moving parts make Maxtor’s drives inherently more dependable.

Power consumption is a very low 2.8 watts, making it one of the lowest in the 80MB class. The 7080 is also Novell Labs certified, and is available with either SCSI or AT interface, giving you flexibility for a winning system.

Exceptionally fast 17ms seek time and 32K cache buffer in the new generation inch-high form factor give Maxtor faster data throughput than the competition.

Call and ask about our entire Cheyenne family of disk drives with capacities from 40MB to 130MB. Don’t fall for the off-the-wall claims. Give us a shot and we’ll prove Maxtor specs can’t be matched. Call your nearest Authorized Maxtor Distributor.

<table>
<thead>
<tr>
<th>3.5-inch Disk Drive Spec.</th>
<th>Maxtor 7080A</th>
<th>Seagate 1102A</th>
</tr>
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<tbody>
<tr>
<td>Seek Time</td>
<td>17 Msec.</td>
<td>19 Msec.</td>
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<tr>
<td>Standard Buffer Size</td>
<td>32K</td>
<td>8K</td>
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<tr>
<td>Form Factor</td>
<td>3.5&quot; x 1&quot;</td>
<td>3.5&quot; x 1.6&quot;</td>
</tr>
<tr>
<td>Heads-Diskss</td>
<td>4/2</td>
<td>6/3</td>
</tr>
<tr>
<td>Avg. Power Consumption</td>
<td>2.8 watts</td>
<td>9 watts</td>
</tr>
</tbody>
</table>
Call Your Authorized Maxtor Distributors

A.D.P.I.
1-800-275-2374
301-258-2744
Anheuser Electronics
408-452-2287
Arrow Commercial Systems Group
1-800-323-4373
Arrow/Klerulis
1-800-777-2776
Avnet Computer
1-800-422-7070
B.S.M/Business Solutions in Micro
1-800-888-3475
214-699-8300
Cal Abco
818-704-9100
800-669-2226
Compac Micro Electronics
1-800-426-6722
415-656-2244
Computer Brokers of Canada
416-660-1616
1-800-663-0042
1-800-361-6415
CPC
714-757-0505
800-582-0505
Data Storage Marketing (D.S.M.)
1-800-543-6098
303-442-4747
Firstop Computer
1-800-832-4322
Future Electronics
514-694-7710
Intelect
011-525-255-5325
Marshall Industries
1-800-522-0084
Microwave Distributors
1-800-777-2589
503-646-4492
Mini-Micro Supply Co.
408-456-9500
1-800-628-3656
Pioneer Standard Electronics
1-800-874-6633
Pioneer Technologies
1-800-257-1693
S.E.D.
1-800-444-8962
404-491-8962
Tech Data
1-800-237-8931
813-539-7429
Technology Factory
1-800-848-2073
1-800-227-4712
U.S. Computer
305-477-2288
Wyle Laboratories
1-800-289-9953

COMPONENTS & POWER SUPPLIES

ity in a true military/aerospace grade device. The parts meet the −55 to +125°C military operating-range requirement and are designed to pass constant acceleration, random vibration, thermal shock, and extended high-temperature life tests. The converters operate with either 28 or 270V inputs and provide outputs of 5, 12, 15, 28, ±12, or ±15V at power levels ranging to 65W/unit. As many as three converters can operate in a current-sharing mode. Other converter parameters include an 85% typical efficiency, 50-dB-max audio rejection, and 15-mV line and load regulation figures. Operating with no external components, the converters meet MIL-STD-461C CS01 and CS02 susceptibility requirements. Operating with companion EMI filters, the converters meet MIL-STD-461C CE03 emission limits. $690 (100).

Interpoint Corp., Box 97005, Redmond, WA 98073. Phone (206) 882-3100. FAX (206) 882-1990. Circle No. 377

Surface-Mount Sockets
- Available with tin- or gold-plated contacts
- Feature gull-wing terminals
Diplomate surface-mount DIP sockets are available in dual- and single-leaf versions. They feature gull-wing solder tails and high-temperature-tolerant insulators that can withstand vapor-phase-reflow and infrared-soldering temperatures. Dual-leaf versions feature face-wiping contacts with either tin or gold plating over phosphor bronze. The insulators have a closed-bottom design to prevent solder wicking. Single-leaf sockets come with tin-plated phosphor bronze or beryllium copper contacts. These devices also resist wicking and bridging and have a closed-top design to prevent contact damage. The dual-leaf sockets are available in 16- or 32-position versions; single-leaf units have 28 positions. $1.45 (1000) for the 28-position unit.

AMP Inc., Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752. Circle No. 378

Latch Solenoid
- Requires no power to remain pulled in
- Operates from a single supply
The MS2 solenoid can pull in and latch when power is applied to the coil. A magnet then holds the plunger in the closed position after the power is removed. The unit can operate with only a 50- to 100-msec pulse of power. Once closed, the unit can withstand a force of 76 to 160 oz. A short-duration 1W pulse, applied in reverse polarity, will cancel the permanent magnetic field and release the plunger. The solenoid operates with a supply of 12, 24, or 110V dc. The continuous standard power rating is 7W, and the intermittent-duty power rating is 20W. $13. Delivery, six to eight weeks ARO.

Liberty Controls Inc., 500 Brookforest Ave, Shorewood, IL 60435. Phone (815) 725-2241. FAX (815) 725-6571. Circle No. 379

Connector Kits
- Evaluate epoxyless optical connectors
- Available for single- and multimode fibers
EK100X kits allow users to evaluate XTC Series epoxyless fiber-optic connectors. Each kit contains 25 connectors, a specially designed
crimp tool, a sapphire scribe, and easy-to-follow instructions in a handy carrying case. The kits are available for single- and multimode (50/125 and 62.5/125 µm) fibers. The 2.5-mm connectors in the kit are functionally form- and fit-compatible with the popular ST connector. When terminating a single-mode fiber, the connector demonstrates a 0.16-dB insertion loss over an operating range of -40 to +65°C. EK1001 multimode kit, $444; EK1000 single-mode version, $520.


Circle No. 380

### Prototyping Converter

- **Requires no soldering**
- **Accepts plastic quad flatpack sockets**

The 160QF100-R00-M prototyping socket converter accepts both 160- and 144-pin hinged-lid, ZIF plastic quad flatpack (PQFP) sockets and converts the footprints to a standard 100-mil matrix. You can then mount the converter assembly on standard prototyping boards. The female pins on the top of the converter accept the socket, allowing for easy insertion and removal with no need for soldering. The converter can remain in place on the prototyping board; when any changes are necessary, you simply unplug the socket and replace it with whatever is required for the task at hand. Two converter sizes are available. The minimum-footprint version is only slightly larger than the size of the PQFP socket. The test-pin unit has two rows of test posts/side to facilitate signal monitoring. $166.

**EDI Corp**, Box 366, Patterson, CA 95363. Phone (209) 892-3270.

Circle No. 381
Sensym's 142/163 Series

Features Include:
- Guaranteed precision over temperature: ±1% Max (-18°C to +63°C)
- High level calibrated output: 1.0V ±50mV offset, 5.0V ±50mV span
- Linearity: <0.75% FSO Max

These precision transducers are priced starting at $40 ea / 100's. Stock delivery.

FOR:
- MEDICAL
- INDUSTRIAL
- HVAC

Available parts:
- 163SC01D48 ... - 20 to +120cmH2O
- 142SC series ... 0 to 1 psi up to 0 to 150 psi

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Sensym's new 1990 Sensor Handbook gives complete product specifications plus over 200 pages of application notes and ideas.

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NEW PRODUCTS

INTEGRATED CIRCUITS

14-Bit Hybrid ADC
- Contains T/H circuit
- Conversion speed is 5 MHz

Packaged in a hermetic 40-pin TDIP, the ADC-00145 contains a 14-bit A/D converter, a 200-nsec track/hold circuit, 3-state output buffers, and timing circuits. Capable of converting at a 5-MHz rate, the device uses a 2-step conversion algorithm. A pulse input to the encode-command pin initiates the conversion cycle. After the T/H circuit samples and stores the analog input, a flash ADC generates a coarse encode of the sampled voltage and stores its 8 bits in the MSB register. At the same time, a high-speed DAC converts the 8 bits to an analog voltage, which is subtracted from the original input. The flash ADC then generates a fine encode of the subtracted voltage and stores these 8 bits in the LSB register. Digital error correction combines the coarse and fine data to yield a 14-bit output. The ADC-00145 operates over -55 to 125°C. From $1200. Delivery, 8 to 12 weeks ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600, ext 419. FAX (516) 567-7358. Circle No. 383

High-Speed S/H Amplifier
- Delivers 16-bit accuracy
- Acquisition time is 500 nsec

The SHM-945 is a high-speed S/H amplifier characterized for both 16-bit and 14-bit applications. At 16-bit resolution, the hybrid circuit features a maximum acquisition time of 500 nsec to ±0.00076% (±1/2 LSB) for a 10V full-scale step. At 14-bits, the device has a maximum acquisition time of 350 nsec to ±0.003% (±1/2 LSB). The amplifier features a differential input, which provides rejection of common-mode noise. Other specifications include feedthrough rejection of 100 dB, hold-mode rms noise of only 60 µV, aperture uncertainty of 10 psec, and a bandwidth of 16 MHz. The device operates from 5 and ±15V supplies. Packaged in a 24-pin DDIP, the SHM-945, in commercial and military temperature ranges, $79 and $87, respectively (OEM qty).

Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. FAX (508) 339-6356. TLX 174388. Circle No. 383

Sampling A/D Converter
- 12-bit resolution
- 333-kHz throughput

The SP7800 sampling A/D converter features a 333-kHz throughput at 12-bit accuracy and resolution. In addition to a 12-bit ADC, the monolithic device contains an internal S/H circuit, a reference, a clock, a microprocessor interface, and 3-state outputs. Dynamic performance includes a S/N ratio of 72 dB, a spurious-free dynamic range of 80 dB, and THD of -80 dB. The device supports standard input ranges of ±5 and ±10V. The SP7800 is available in a 28-pin plastic DIP, 28-pin side-brazed ceramic DIP, and 24-pin SOIC packages. Commercial grade parts, from $23 (100).

Sipex Corp, 6 Fortune Dr, Billerica, MA 01821. Phone (508) 663-9691. Circle No. 384

BiCMOS Decoder PLDs
- Have 6- or 7-nsec propagation delay
- Support system clock rates to 50 MHz

Optimized for address-decoder ap-
In the technological jungle, the new Samsung graphic LCD is an entirely different animal. Larger screens, High Contrast in paper white, green, blue and gray, and multi-angle viewing, make Samsung LCDs among the best on the market. Add our reputation for on-time delivery, and you're ensured a high-quality, stable supply. And if that doesn't convince you, we'll put it in black and white: Your customers will go wild for them.
applications, the 12-input, 8-output fuse-programmable BiCMOS PLDs feature propagation delays of 6 or 7 nsec. The 336 and 337 models of this series have registered inputs; the 338 and 339 have output latches. The 336 and 338 have two product terms per output; the 337 and 339 have four product terms per output. The chips with registered inputs accommodate most RISC (reduced-instruction-set computer) processors, including SPARC and MIPS, which assert addresses for only a short period around the clock edges. The chips with output latches accommodate processors that do not issue an address within every clock cycle and that remove addresses and data before the end of the clock cycle, a behavior that is typical of CISC (complex-instruction-set-computer) processors such as the 80486 and 680x0. The decoder PLDs come in a variety of packages including DIP, SOJ, LCC, and PLCC (plastic leaded chip carrier) types. $14.30 to $16.35 (100).

Cypress Semiconductor, 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600.

Circle No. 385

Color-Palette D/A Converters
- Compatible with RS-170
- Data rates from 35 to 110 MHz

The TMC0171 and TMC0176 color-palette D/A converters contain three 6-bit DACs, a 256-word × 18-bit RAM look-up table, and a standard MPU interface for writing and reading the RAM. An 8-bit data input addresses the RAM, selecting one of the 256 18-bit words that determine the specific 6-bit levels of red, green, and blue colors. The devices, which cover data (pixel) rates from 35 to 110 MHz, are compatible with the RS-170A standard and directly drive the red, green, and blue analog inputs to CRT monitors. The TMC0171 is available in speed grades of 35 and 40 MHz. The TMC0176, which includes a power-down control for use in battery-operated systems, is available in speed grades of 40, 50, 66, 80 and 110 MHz. Package options include 28-pin DIPs and 44-lead PLCC’s (plastic leaded chip carrier). Depending on type and speed grade, $3.38 to $6.82 (100).

TRW LSI Products Inc, Box 2472, La Jolla, CA 92038. Phone (619) 457-1000. FAX (619) 455-6314.

Circle No. 386

Resolver-To-Digital Converter
- Replaces optical encoder
- Has 1.3 arc-minute accuracy

Designed to replace optical encod-
Announcing the New Ultimate in Driving

Power Convertibles™

The premiere vehicle in power conversion. These DC/DC Converters allow you to maintain a unique balance between price and performance.

The hottest economy model on the road is the HPR1XX. It is compact and affordably priced to drive your system. The Single-In-Line body styling conserves board level parking, taking up less than 0.2 inch² board space. A low profile is achieved through Surface Mount Manufacturing.

Precision performance comes with the HPR1XX's 750mW of output power. This Power Convertible has exceptional roadhandling with a high efficiency rating of 80%. You can "rev" up your designs with our isolation voltage of 750VDC.

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Write P.O. Box 11400 - Tucson, AZ 85734

CIRCLE NO. 210

Power Convertibles is a registered trademark of Power Convertibles Corporation, an affiliate of Burr-Brown Corporation.

Your Partner in Quality
ers in high-resolution military applications, the 16-bit HRD1416 resolver-to-digital converter comes in a 1-in.-square, hermetically sealed, 32-pin package. The Type-II tracking converter operates from a single 5V supply and consumes only 75 mW of power. Compatible with both 8- and 16-bit microprocessors, the converter features an accuracy of 1.3 arc-minutes. An anti-180° false-lock-up feature provides a logic "1" when the tracking error exceeds ±1°. The HRD1416 is built using MIL-STD-883B processing. From $525. Delivery, 16 weeks ARO.


Circle No. 387

Analog Multiplier/Divider

- **Bandwidth** is 10 MHz
- **Slew rate** is 450V/µsec

Operating with a full-power bandwidth of 10 MHz, the ADT34 multiplier/divider offers a slew rate of 450V/µsec, a S/N ratio of 94 dB, and a guaranteed conversion accuracy of 0.25%. The device performs the mathematical function W = XY/U, where X, Y and U are fully differential analog-input signals. Connected as a four-quadrant multiplier, the device can function as an oscillator, filter, or voltage-controlled amplifier. Connected as a 2-quadrant divider, the device can function as an automatic-gain-control (AGC) amplifier or an rms-to-de converter. A direct-divide mode allows users to optimize the dynamic range for varying input-signal spans. Because of its 40-MHz input bandwidth, you can also use the device as a demodulator or mixer in heterodyne receivers. The third-order intercept point is 43 dBm, and the 1-dB compression point is 18.6 dBm for an 8.46V signal across 1 kΩ. Third-order intermodulation distortion (IMD) is -75 dB. The

---

**INNOVATIVE SOLUTIONS from RAD**

**RJ-002** SYNCHRONOUS CDP MODEM

Operates at data rates up to 256 kbps

Performing all the functions of a sync short range modem, the RJ-002 operates at data rates up to 256 kbps. Utilizing conditional diphase modulations, it requires only interfaces to the phone line and user circuits for complete modem. Transmit clock is derived from either the attached crystal or externally. The carrier can be controlled by the RTS signal or setup for continuous operation. An external circuit programs the delay between RTS and CTS. The receive circuit recovers the clock from the line signal and decodes the data into NRZ format. A carrier detect circuit indicates the presence of the carrier on the line. The part suits the design of built-in short range modems into data PBXs, high-speed multiplexers, voice PBXs, terminals, telemetry control and diagnostic systems, computers, workstations, etc.

Based on 3 µm CMOS technology, the device comes in a 22-pin plastic package.

**RJ-009** ASYNCHRONOUS/SYNCHRONOUS CONVERTER

RJ-009, asynchronous to synchronous converter provides the interface between an asynchronous DTE and a synchronous DCE, allowing the DTE to operate within the timing control of the DCE. While converting from asynchronous to synchronous, the chip inserts or removes STOP bits from the Data to compensate for frequency differences between the DTE and DCE. In the event of stop bits being removed, the remote RJ-009 detects the missing stop bits and generates shorter stop bits according to CCITT V.22 bis. The RJ-009 contains an AUTO-BAUD detector which makes manual programming of the bit rate unnecessary, by automatically measuring the modem's clock frequency. Other features include: data rates up to 38.4 kbps async, character length of 8, 9, 10 or 11 bits, low power consumption and single 3-5.5V power supply. Based on 1.5 micron CMOS technology, this 24 pin RJ-009, 0.3 inch wide is offered in a plastic package.

---

**U.S. HEADQUARTERS**

U.S. EAST: 151 West Passaic Street, Rochelle Park, NJ 07662. Tel: (201)587-8822, Fax: (201)587-8847.

U.S. WEST: 771 Center Avenue #400, Huntington Beach, CA 92647. Tel: (714) 991-1994, Fax: (714) 987-7788.

INTERNATIONAL HEADQUARTERS

8 Hanechoshet Street, Tel Aviv 69710, Israel. Tel: 972-3-492820, 5447851.

CIRCLE NO. 60

EDN June 6, 1991
Go ahead ... add 5 psec

Picoseconds are no problem for the DG535 Precision Pulse & Delay Generator.

The DG535 provides 4 edge (delay) and 2 pulse (delay and width) outputs, all with 5 ps resolution, 1000 sec range, 50 ps rms jitter, and adjustable output levels. The outputs drive 50 Ohms or high impedances to 4 Volts with a slew rate of 1 V/ns - just right for driving TTL or ECL or even high speed analog circuits. Throw in the 35 Volt output option and you can trigger almost anything. For even greater accuracy and stability, add the 1 ppm optional timebase.

Top it off with the intelligent menu-based front panel and standard GPIB interface, and the DG535 is probably the most versatile timing generator you can find.

On the bench or in a test environment, the DG535 has the accuracy, stability, precision, and reliability you need to solve your tough timing problems - all at a price you can afford. Call SRS for more information on the DG535, even if you don't need picosecond resolution.

---

**DG535**

- 4 delay, 2 pulse channels
- 5 ps delay resolution
- 50 ps rms jitter from trigger
- Adjustable output levels to 4 Volts
- 0 to 1000 sec delay range
- Internal/external trigger to 1 MHz
- Internal/external timebase
- 9 location set-up memory
- GPIB interface standard
- ±35 Volt output option
- 1 ppm timebase option
- 100 ps rise/fall time option

---

SRS 
STANFORD RESEARCH SYSTEMS

1290 D Reamwood Avenue, Sunnyvale, CA 94089 TEL (408) 744-9040 FAX 4087449049 TLX 706891 SRS UD

EDN June 6, 1991  CIRCLE NO. 211  221
AD734 is available in a 14-pin ceramic package, two temperature grades, and three accuracy grades. AD734AQ, with 0.1% accuracy, $10.55 (100).

Analog Devices Inc, 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428.

Circle No. 388

**Bus Driver/Receiver IC**
- For analog multiplex-bus networks
- Designed for automotive applications

The CS-8425 bus-driver/receiver IC interfaces with the system's µP and the sensors and control elements needed to provide the system with specific information or functions. Designed for class-A multiplexed bus networks such as those used in automotive applications, the IC provides protection against short circuits, thermal overload, voltage transients, and reverse-battery voltages. The IC also contains a watchdog feature that you can use to disable the power-output stage. Two operating modes are available. The polling mode provides synchronous access to each of 30 possible sensors on the bus. The command mode allows random access to any of 32 control elements on the bus. Each mode relies on the IC to interpret digital input information and then communicate with the system by placing analog signals on the bus. CS-8425, in 16-pin DIP and 20-pin SOIC packages, $1.60 and $1.70 (1000), respectively.

Cherry Semiconductor Corp, 2000 South County Trail, East Greenwich, RI 02818. Phone (401) 885-3600. Circle No. 389

**64k-Bit Nonvolatile Smart RAM**
- Includes real-time clock
- Organized 8k × 8 bits

The MK48T08 and MK48T18 Smart RAMs each contain a low-power 8k × 8-bit CMOS static RAM (SRAM), a CMOS clock and power-fail detection circuits, a crystal, and a lithium battery. The devices, which provide time and data retention without need of external power, have access times of 100 and 150 nsec. The devices operate with a standard SRAM memory access, without need for any special write-timing requirements and without limitations on the number of write cycles. Integral power-fail circuitry automatically provides chip deselect and write protection whenever \( V_{cc} \) falls below 4.75V (MK48T08) or 4.5V (MK48T18). Both devices also provide two chip-enable inputs and a power-fail output signal. Using a 24-hour BCD format, the clock func-
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EDN June 6, 1991 CIRCLE NO. 212

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CIRCLE NO. 212

223
tions include year, month, date, day, hour, minute, and second. A control register lets you set, stop, restart, or calibrate the clock. They come in 28-pin plastic DIPs. From $22.50 (1000).

SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. FAX (602) 867-6290. Circle No. 390

**Dual-Port Memory Module**

- **Features 512k-bit density**
- **Has 16k x 32-bit organization**

Designed for high-performance applications employing 32-bit CISC (complex-instruction-set computer) or RISC (reduced-instruction-set computer) processors, the IDT7M1002 memory module features 512k-bit density and a 16k x 32-bit organization. The module, which mounts four IDT7006 16k x 8-bit dual-port devices on a 121-pin PGA package, is 1.8 in². To meet varying customer requirements, the dual-port module is available in access-time ratings of 40, 45, 50, 55, 65, 80, and 100 nsec. The vendor tests each module at the pin level as if it were a single monolithic component, using guardbanded ac and dc parametric tests over the operating temperature range. IDT7M1002, from $447.50 (100).

Integrated Device Technology, Box 58015, Santa Clara, CA 95052. Phone (408) 727-6116. FAX (408) 492-8674. Circle No. 391

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**The Ultimate VMEbus Tool Set**

Based on the VBT-321 Advanced VMEbus Analyzer, VMETRO's Modular VMEbus Analyzer System offers piggyback modules for all kinds of VMEbus development, verification and tuning purposes.

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**Instrumentation Amplifier**

- **Noise is 1 nV/√Hz**
- **THD+N is 0.0009% at 1 kHz**

Designed primarily for use with low-source-impedance transducers, the INA103 instrumentation amplifier features a noise specification of only 1 nV/√Hz. The monolithic device incorporates a distortion-canceling input stage, which reduces THD+N to 0.0009% at 1 kHz. The device also includes gain-setting resistors for gains of 1 and 1000; external resistors can set the gain anywhere in the 1 to 1000 range. At a gain of 1000, offset voltage is 52 µV max, and drift is 1.25 µV/°C max. The INA103 comes in a 16-pin DIP and is available in commercial and military temperature grades. From $4.85 (1000).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; in AZ, (602) 746-1111. FAX (602) 889-1510. Circle No. 392
HARTING is a hallmark of innovation and reliability worldwide – throughout the electronics industry and in the switchgear sector.

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LAN Support For µP Development System

• Consists of card cage, interface, and EPROM card
• Supports 8, 16, and 32-bit µPs
The 67400A card cage, 67401A LAN interface card, and a companion EPROM card let you interface the vendor’s µP development systems to local-area networks. Hence, you can upload and download code and control the operation of hardware development tools, such as in-circuit emulators, from networked workstations. Tools for 8, 16, and 32-bit µPs are supported, so that on a single network, you can debug systems based on several types of target processors. The hardware connects with different types of LANs either directly or via an attachment interface unit. Some of these LANs are thick- and thin-wire Ethernet, and StarLAN. Card cage, $6000; LAN card, $2500; flash EPROM card, $500.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 393

MS Windows-Based Data-Acquisition Drivers

• Provide more than 70 services for creating tasks
• Let you take advantage of your hardware’s speed
The Driverlinx series family of language-independent dynamic-link libraries supports several vendors’ data-acquisition boards under MS Windows V3.0’s real, standard, and enhanced modes. Supported boards come from Keithley Metrabyte, Computer Boards, Soltec, and Advantech. The libraries provide developers with more than 70 services for creating foreground and background data-acquisition tasks. Such tasks include analog and digital I/O; frequency, period, and time measurement; and event and pulse counting. Applications communicate with the drivers by passing service requests that contain the specifications of the required task. Speed of operation is usually that of the hardware. C source code for the libraries’ interactive demonstration program is included. $400.


Differential Probe Set

• Have 250-MHz bandwidth
• Permit adjustment of resistance and ac response
The MD12F differential probe set lets you precisely match oscilloscope channels for accurate differential measurements. The probes work with signals from dc to 250 MHz. One of the probes in the pair lets you precisely adjust its attenuation at dc. Coarse and fine controls let you adjust the frequency response. The probe set has an attenuation of 10:1 and a rise time of 1.4 nsec. The probe set works with scopes whose input capacitance is from 10 to 60 pF. $340.

Test Probes Inc, 9178 Brown Deer Rd, San Diego, CA 92121. Phone (800) 368-5719.

Circle No. 395

80386SX Preprocessor For HP Logic Analyzers

• Includes clip for contacting PQFP IC
• Also includes disassembly and configuration software
The 386SX preprocessor works with HP 1650A/B, HP 1652A/B, HP 1654A/B, and HP 16510A/B logic analyzers. It has a software disassembler, configuration software, and a passive clip that facilitates connect-
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SUPERPRO is a software controlled 40-pin universal device programming workstation designed to meet all of your programming needs for different types of programmable devices.

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- Package includes software, program ming module, high speed interface card, & cable

Circle # 221

JEDEC files
- PLA verification using test vector
- GAL electronic signature recognition

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- ADAPTOrs for PLCC, LCC, SOIC, FLATPAK-type ICs
- A Socket Adaptor for E2PROM
- Socket Adaptors for Micro Controllers.

Circle # 222

3 1/2 Digit LCD Display of Voltage and Current
- Triple Output
  - Output # 1: 0~50V, 0.5% max
  - Output # 2: 15V, 1A(Fixed)
  - Output # 3: 5V, 2A(Fixed)
- Ripple
  - Output # 1: 1mV max
  - Output # 2: 5mV max

Load Regulation
- Output # 1: 0.01%+5mV
- Output # 2: 5% Less than 35mV

ADVANCED DATA ACQUISITION CARD

The MCP - 550 is the ideal single board solution for many data acquisition and control applications.

It is a high performance data acquisition card for IBM PC/XT/AT, integrated with A/D, D/A, D/I, D/C, and Timer/Counter functions. A built in Direct Memory Access circuit makes it possible to transfer data in high speed.

The MCP - 550 is supported by a variety of vendor softwares which makes it ideal for wide range of industrial and laboratory applications, such as Process Control, Automatic testing, Factory Automation, and Data Acquisition. Furthermore, it can be in tegrated with a PC and softwares to emulate many electronic devices. For example, Digital Oscilloscope, X-Y Recorder, Data

Circle # 224

- Multi functions in one card: A/D, D/A, D/I, D/O
- 16 single ended or 8 differential analog input channels
- A/D Sample Rate: 60KHz normal or 100KHz max.
- 24 TTL compatible D/I & D/O channels
- Two 12-bit monolithic multiplying D/A channel

LOW - COST DATA ACQUISITION CARD

The MCP - 520 is a cost effective single board solution for many data acquisition and control applications.

It is a multi-function card for IBM PC/XT/AT or compatible computers, integrated with A/D, D/I, D/O functions on a single board.

In order for users to minimize their efforts for developing application softwares, a utility softwares diskette is provided, which includes drivers and sample programs.

- Multifunctions in one card: A/D, D/I, D/O
- Eight single ended analog input channels
- Industry standard 12 bit resolution with

Circle # 225

successive approximation
- 24 TTL compatible Digital input/Digital output channels
- High speed analog to digital conversion with 60,000 samples/sec(15 sec)
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- Monitoring and Controlling process
- Programmable signal generator
- Industrial Off/On control
- Contact closure monitoring

IEEE - 488 INTERFACE CARD

The MCP - 488 interface card complies with IEEE - 488 standards, which is the most popular international standard for transferring information between electronic devices.

Communication between PC and IEEE bus devices is possible because the MCP - 488 interface card provides hardware and software. The firmware manifests its competence and handness with programming languages or operating systems.

Interfaces ought to deal with hardware book - keeping and timing while maintaining compatibility between a computer and peripherals. The MCP - 488 handles IEEE - 488 interface standards smoothly.

Circle # 226

- Complete compliance with IEEE - 488 standards
- The software provides flexible and handy IEEE - 488 language extenstions for high level languages and operating systems
- The printer port of IBM PC/XT/AT can be programed to a port for IEEE - 488 devices
- Direct memory access for high speed data transmission
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EDN June 6, 1991 CIRCLE NO. 170
TEST & MEASUREMENT INSTRUMENTS

Handheld DMMs
- Include eight models
- Some measure capacitance to 9999 µF
The 70 Series II consists of eight handheld digital multimeters; three of them are in bright yellow safety cases. The flagship models 79 and 29 make basic measurements with a resolution of 4000 counts and an accuracy of 0.3% for dc volts. They also measure frequency to 20 kHz and capacitance to 9999 µF. Convenience features, such as Touch Hold, simplify use. With this feature actuated, when you touch a probe to a voltage, the meter will hold its reading until you tell it to make another measurement. Therefore, you can watch where you’re probing instead of watching the meter. $69 to $185.

John Fluke Mfg Co Inc, Box 9090, Everett, WA 98206. Phone (206) 347-6100. FAX (206) 345-5116. TLX 185102. Circle No. 397

High-Speed Pattern Generator
- Provides eight channels at 680 MHz; four at 1.36 GHz
- Stores 16k or 32k states/channel
The PG-1400 high-speed pattern generator can produce an 8-channel output at 680 MHz or a 4-channel output at 1.36 GHz. In the 8-channel mode, it stores patterns 16k-states deep; in the 4-channel mode, it stores 32k-state patterns. You can connect as many as eight units together to produce 64-channel patterns at 680 MHz or 32-channel patterns at 1.36 GHz. As its host, the
Finally, engineering software that clears the way to problem solving without programming.

```c
void service(void)
int eid;
{ int stat, byte;
/* serial poll int
byte = hpi b_spoll(eid);
if (byte<0) { if (byte<0) { if (byte<0) {
    printf("SRQ Problem\n
    return; }
    stat = my_read(eid, DVM;
if (stat>0) {
    buffy[stat] = '\0';
    printf("Data from instrument\n    return; }
else printf("I/O read error\n
return; }
main() {
  int busid, stat, MTA, MLA;
  char command[MAXCHARS];
  busid = open("/dev/hpi b", O_RDWR); /* open raw HP-IB */
  MTA = hpi b_bus_status(busid, CURRENT_BUS_ADDRESS) + 64;
  MLA = hpi b_bus_status(busid, CURRENT_BUS_ADDRESS) + 32;
  stat = BUTTON_BIT;
  sprintf(command, "KM%02o", stat); /* 2 octal digits */
}
```

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So, if programming is keeping you from finding solutions, call 1-800-752-0900. Ask for Ext. 2380, and find out how HP VEE clears the way.

* U.S. list prices.

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TEST & MEASUREMENT INSTRUMENTS

generator requires an IBM PC/AT or equivalent computer with a high-resolution color display and 10M bytes of free space on its hard disk. $38,500. Delivery, six weeks ARO.

**Outlook Technology Inc, 200 E Hacienda Ave, Campbell, CA 95008. Phone (408) 374-2990. TLX 350479. Circle No. 398**

**PC-Based DSO With Deep Memory**

- Acquires 40M samples/sec
- Stores 1M sample

The Compuscope 220-1M is a digital storage oscilloscope on a pair of IBM PC bus I/O cards. It samples two channels with 8-bit resolution—one at a maximum rate of 40M samples/sec and the other at 20M samples/sec. The minimum rate is 1 sample/sec. The scope can store 1M sample. You can devote all the memory to either channel, or you can divide the memory equally between the channels. The inputs have a resistance of 1 Ω shunted by 20 pF and have seven gains that you can program from 0.1 to 10 in 1-2-5 steps. The external-trigger input has ac and dc coupling and gains of 0.1 and 1. The scope triggers on either positive or negative slopes. The software included with the boards lets you store, analyze, print, and communicate data. $3900.

**Gage Applied Sciences Inc, 5465 Vanden Abeele, Montreal, PQ Canada H4S 1S1. Phone (514) 337-6893. FAX (514) 337-8411. Circle No. 399**

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CIRCLE NO. 64

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- Queries you about your application
- Creates analog, digital, and counter/timer I/O routines

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CIRCLE NO. 101

TEST & MEASUREMENT INSTRUMENTS

Handheld 2- to 8-GHz Signal Generator
- Provides at least 10 dBm
- Accepts TTL remote programming

The Model 8001 signal generator produces an output of at least 10 dBm over the range of 2 to 8 GHz. The 2.52 x 5.57 x 7.45-in. handheld unit uses less than 10W of ac power and is programmable via a TTL interface. Frequency resolution is 1 MHz; accuracy is ±15 MHz. In normal mode, the generator can switch frequencies across the full band in less than 350 msec; in fast mode, switching takes less than 20 msec.

At 20 kHz from the carrier, single-sideband phase noise is 80 dB below carrier level (-80 dBc). Second-harmonic output is at least -8 dBc, third-harmonic output is typically -14 dBc, and spurious outputs are -50 dBc. You can frequency-modulate the unit (40-MHz carrier deviation) with dc to 200-kHz signals. $3750. Delivery, three to five weeks ARO.

April Instrument, Box 62046, Sunnyvale, CA 94088. Phone (415) 964-8379. FAX (415) 965-3711.

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Near Plethora Of Products For 1991
The 1991 product handbook provides a comprehensive listing of data-acquisition, industrial-control and monitoring, signal-conditioning, personal instrumentation and communications products for IBM PCs, PS/2s, and Apple Macintosh microcomputers and compatibles. The 272-pg book also describes the Workhorse and Metrabus families of high-speed industrial control and monitoring products. Selection guides can help you find products you need to locate.
Keithley Metrabyte, 440 Myles Standish Blvd, Taunton, MA 02780.
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Brochure Surveys Applications For DSP
The subject of this 8-pg brochure is DSP-based solutions for high-end signal-analysis applications in military/SIGINT (signal intelligence), research physics, and satellite communications. Application notes explain pulsed radar, FSK, and other measurements. A description of the VMEbus-based analysis system includes comparing amplitude and frequency; spectrogram; and phase and view limits of color displays.
Tektronix Federal Systems Inc, Box 4545, MS 38-386, Beaverton, OR 97076. Circle No. 406

App Notes Discuss Embedded Systems
The Basics of High Speed Design explains how to design a reliable and functional high-speed digital system, delving into ground bounce, crosstalk, transmission lines, ground planes, and pc-board stack-up. Networked Embedded Design Development Systems discusses how to develop well-designed networks. Transparent Connections for Embedded Microprocessor Systems Design Tools deals with five types of transparency. It explains how you can build the five types of transparency (communications, execution, logical, electrical and mechanical) into an emulation system. Event Monitor System for ES 1800 Emulators covers the benefits and features of such a system. Programming the 8018X/80C18X Peripheral Control Block gives examples of how to set the
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**Noting Remote-Terminal Memory Management**

Application Note AN/B-18, A MIL-STD-1553B Notice 2 Solution For Bulk-Data Transfers, explains the need for improved remote-terminal memory management in bulk data transfers. It discusses the use of the MIL-STD-1553 bus for transferring large blocks of data or program code between intelligent subsystems. Listing useful attributes for improved memory management, the note mentions the processing of multiple messages to the same transmit/receive subaddress without host-processor intervention; capacity for at least 64k words; receiving and transmitting bulk data blocks; storage for mailbox data blocks; and the option of complying with MIL-STD-1553B notice 2. The publication introduces Bus-61559 Aim Hy'er hybrids for implementing multimessage transfers.

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Literature Dept, 105 Wilbur Pl, Bohemia, NY 11716. Circle No. 408

**Journal Reports On Circuits And Systems**

The quarterly journal, *Analog Dialogue*, focuses on circuits, systems, and software for real-world signal processing. The 28-pg Volume 24, No. 3 features three RAM D/A converters that enhance VGA graphics. It also covers a monolithic current transmitter, enhancements for DSP (IC processors and development tools), and two precision dual op-amp families. The regular feature, Ask the Applications Engineer, continues a discussion on op amps; the Worth Reading column provides a listing of app notes.

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PROFESSIONAL ISSUES

Engineering graduate schools

Jay Fraser, Associate Editor

Enrollments are declining, and a serious faculty shortage may lie ahead.

Americans make up approximately 95% of all students who receive bachelor’s degrees in engineering from US schools, but less than 50% of those who go on to earn a PhD. Today more than half of the teaching assistants, research assistants, and faculty under 35 years old in our engineering schools are foreign nationals. Behind those statistics from the National Science Foundation lies a complex of interlocking factors—financial, psychological, academic, even ethnic—that may mean serious problems in the future for graduate-level engineering education and the engineering profession in this country.

The most overpowering reason why the majority of American students don’t go on to graduate school is financial. More than half of all undergraduates now need some sort of financial assistance to pay for their educations. Because of current federal policy, they usually receive this assistance in the form of student loans. So going to graduate school would only sink them further into debt. In addition, some students, as soon as they graduate, are expected to help support their families or to help put a younger brother or sister through college. The pressure is very strong on many people to leave school after earning their
face a difficult decade

BS degree and start earning money as soon as possible.

This situation isn't helped by the low stipends that many schools pay their teaching and research assistants. A full professor with tenure may earn as much as an engineer of equal age and experience working in industry. Teaching and research assistants, on the other hand, usually receive only one-third to one-fourth the salary of someone with a BS and an entry-level job at a high-tech company.

Another reason for the low number of Americans who go on for a master's degree or a PhD is that many students simply become tired of going to school. After grinding away for four or five years, a large number of students want to get out of academia and do something practical. They think of advanced degrees as being important for a career in teaching, but not really necessary for a career in industry, where they will gain knowledge through hands-on experience.

J Ray Bowen, Dean of Engineering at the University of Washington (Seattle, WA), points out that in graduate schools the courses too often aren't aimed at students who are seeking practical knowledge. "Some of those educational experiences that are designed to prepare students for advanced degrees are not necessarily applicable [to industry]," he says. "We have to enhance the design training in the advanced degree programs. We also need to introduce some courses related to engineering management and the management of technologies. We need to get more into the design of complex systems."

Educators believe that one way to raise the number of Americans enrolled in graduate engineering programs is to put more effort into recruiting people from those groups that have been traditionally under-represented in the profession—women and minorities. In recent years engineering schools have worked to attract and retain women and minority students through increasing the number of scholarships available, setting up support groups, and providing academic counseling.

These efforts have shown positive but small results so far. According to the National Action Council for Minorities in Engineering, the number of African-American, American-Indian, and Hispanic freshmen has risen in the last five years. Members of these groups now make up 6.5% of all engineering graduates. However, only about 1% of the faculty of engineering schools are members of minorities.
Although the number of women enrolled in engineering programs has leveled off in recent years at approximately 15%, it too rose during the last decade. Women currently make up about 3% of engineering faculty members.

Women and minority students are, of course, subject to the same financial pressures and the same desire to leave school for industry as other students, but educators point to an additional reason why many women and minorities have not become faculty members until now. The fact that there have been so few women and minority instructors and professors in engineering schools means that students have lacked role models and mentors.

Another reason for low student interest in an academic career may underlie all the others. As Bowen puts it, “There’s been a sort of malaise in many institutions about the attractiveness of a faculty career, and that has been reflected perhaps in a poor marketing job on the part of university faculty for their profession.”

At many colleges and universities, the road to tenure is through research and writing, not teaching. This emphasis discourages students who are interested in teaching, and hinders teachers from working more closely with students. Some professors only teach the bare minimum—one course per semester—so they can devote themselves to their research. Students perceive that a desire to teach could actually be dangerous to a faculty career. On many campuses you can still hear the old joke: “He was the best teacher I ever had. Don’t tell the tenure committee.”

All these reasons conspire to prevent American students from pursuing advanced degrees. According to the American Society for Engineering Education (ASEE), the number of Americans who received PhDs in engineering last year was about half of what it was in 1970. A much higher percentage of foreign-born students go on to graduate schools, not because they have a more pronounced taste for the academic life, but because many of the pressures American students live under don’t affect them.

Some foreign graduate students don’t feel the same financial pinch that Americans do because they’re supported by their governments while they go to school. Many European countries pay their students a wage equivalent to what an engineer starting out in industry would receive.

In much of the world only students who pass grueling tests are allowed to go to college. Honor and pride, in addition to financial considerations, compel them to go as far as they can in the higher education system. Plus, an advanced degree from an American university will help them command more prestige and a larger salary if they decide to return home.

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But many students will want to stay in the US. The new US immigration law that took effect last year gives foreign students an additional incentive to earn an advanced degree. The law gives preference to skilled and educated individuals. A PhD greatly increases a student’s chances of becoming a permanent resident or a US citizen.

The result of this combination of factors is that foreign nationals now make up more than half of all recipients of PhDs and more than half of all the faculty members under 35 years old in American engineering schools.

Some people see this as a cause for alarm, and some don’t. Richard Ellis, Director of Manpower Studies for the American Association of Engineering Societies, says, “Essentially, we should be proud that we offer an educational system that appeals to people from all over the world. Our schools are clearly leaders internationally. It’s one of the few places where Americans are still in a position of technological mastery and leadership.”

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PROFESSIONAL ISSUES

cerns language. Many foreign nationals speak less than perfect English, and this can make communication difficult. "There's some truth to that," says Ellis. "But at the same time, we caution people to be very careful about stereotypes. There are many foreign nationals in the schools whose English is better than yours or mine."

Another problem is cultural differences. Some foreign-born teachers come from countries where women are not treated as first-class citizens. In a survey of female graduate students conducted at MIT in 1987, the respondents indicated that they faced difficulties ranging from being left out of classroom discussions to being assigned less challenging assistantships. However, the women also said that it was not always foreign-born instructors who caused these problems.

Looming on the horizon may be another problem that has far-reaching implications for US graduate schools and high-tech firms: The number of foreign-born engineering students and faculty members could decrease sharply at any time. Recent events in the People's Republic of China are a good example of what might happen elsewhere. After the massacre in Tiananmen Square in June of 1989, the Chinese government cut back severely on the number of students allowed to study abroad and made it much more difficult for those who were permitted to leave. Now, before Chinese students travel overseas they must, in effect, post bond for themselves.

The number of foreign graduate students and faculty members may also decrease if the American economy continues to weaken. If foreign nationals feel there are better opportunities for them in their native countries, then more and more of them will return home. That will leave gaps in the student and faculty populations of US engineering schools as well as in high-tech companies.

A potential faculty shortage

Another problem is fast approaching that will exacerbate all the others. A 1989 report by the ASEE Task Force on the Engineering Pipeline estimates that by 1995, 25% of the engineering faculty in this country will reach retirement age. A large number of students enrolled in engineering programs in the late 1950s during the defense buildup of those years and the beginning of the space race, and consequently joined engineering faculties. As these people retire over the next decade, engineering schools will have to increase their efforts to fill faculty positions just to maintain their current levels of staffing.

Maintaining the quality of graduate schools of engineering in this country is extremely important, and the US can't depend on a constant number of foreign nationals to fill its teaching positions. It must assure itself of a reliable supply of first-rate American students who want to pursue advanced degrees in engineering and go on to faculty careers. Educators and professional organizations have analyzed the problems besetting US engineering schools and have come up with a number of recommendations.

The first place many people look for help is the federal government. It could aid graduate schools by creating more fellowships and increasing the amount of money it distributes as research grants. In addition, when government agencies are evaluating research proposals they should take into account not just the technical goals of the projects, but also the number of students who would be involved in them. However, with the trend these days toward cutting government spending, more federal funding may be hard to come by.

Industry can help in some of the same ways government can—providing more fellowships and sponsoring more research on campus. Many companies already have tuition reimbursement plans, and many engineers are willing to go back to school for an advanced degree if their companies will pay for it. However, they're put off by how long it will take if they have to go part time. Companies should try to make it possible for their employees to attend graduate school full time.

But engineering schools can't count on outside institutions to solve their problems for them. First of all, they should take steps to ease the financial burden on students by increasing stipends for teaching and research assistants so that they equal the average starting salary in industry for someone with a BS.
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<tr>
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<th>Gate Count</th>
<th>System Frequency</th>
<th>Pins</th>
<th>Availability</th>
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<td>50MHz</td>
<td>68</td>
<td>NOW</td>
</tr>
</tbody>
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PROFESSIONAL ISSUES

Educators should do more to encourage students to consider an academic career. Faculty members enjoy benefits, such as flexible schedules, the freedom to choose their own research projects, and tenure, that simply don’t exist in industry. Teachers also get the personal satisfaction that comes from working with students. More students might choose a faculty career if they understood its rewards better.

For those students not interested in academic careers, but who want more thorough preparation to work in industry, graduate schools should include more courses that offer practical information and deal with real-world problems. Students won’t go to graduate school if they believe it’s only for those who want to pursue abstract research.

Engineering schools must do a better job of recruiting women and minority students and convincing them to continue on for advanced degrees. This is necessary not just to keep educating a sufficient number of engineers, but also to provide role models for younger students. With more role models visible, more women and minority students may enroll in engineering programs, and this problem might eventually solve itself.

In brief, if engineering graduate schools want to head off the problems they’ll face in the decade ahead, they must make it much more attractive for students to go after advanced degrees. They’re going to have to recruit students for faculty careers more aggressively as high tech firms recruit them for industry.

EDN

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EDN June 6, 1991
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- 68010
- 68020
- 68320
- 68332
- 68332

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<th>YSW-2-50DR</th>
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<tr>
<td></td>
<td>500MHz</td>
<td>2000MHz</td>
</tr>
<tr>
<td>Insertion loss, typ (dB)</td>
<td>0.9</td>
<td>1.3</td>
</tr>
<tr>
<td>Isolation, typ (dB)*</td>
<td>50</td>
<td>40</td>
</tr>
<tr>
<td>1dB compression, typ</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>(dBm @ in port)</td>
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<tr>
<td>RF input, max dBm</td>
<td>22</td>
<td>22</td>
</tr>
<tr>
<td>(no damage)</td>
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<tr>
<td>VSWR (on), typ</td>
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<tr>
<td>Video breakthrough</td>
<td></td>
<td></td>
</tr>
<tr>
<td>to RF, typ (mV p-p)</td>
<td></td>
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</tr>
<tr>
<td>Rise / Fall time, max (nsec)</td>
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**PRICE**

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<th>YSW-2-50DR</th>
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<td>19.95</td>
<td>59.95</td>
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*typ isolation at 5MHz is 80dB and decreases 5dB/octave from 5-1000 MHz*

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