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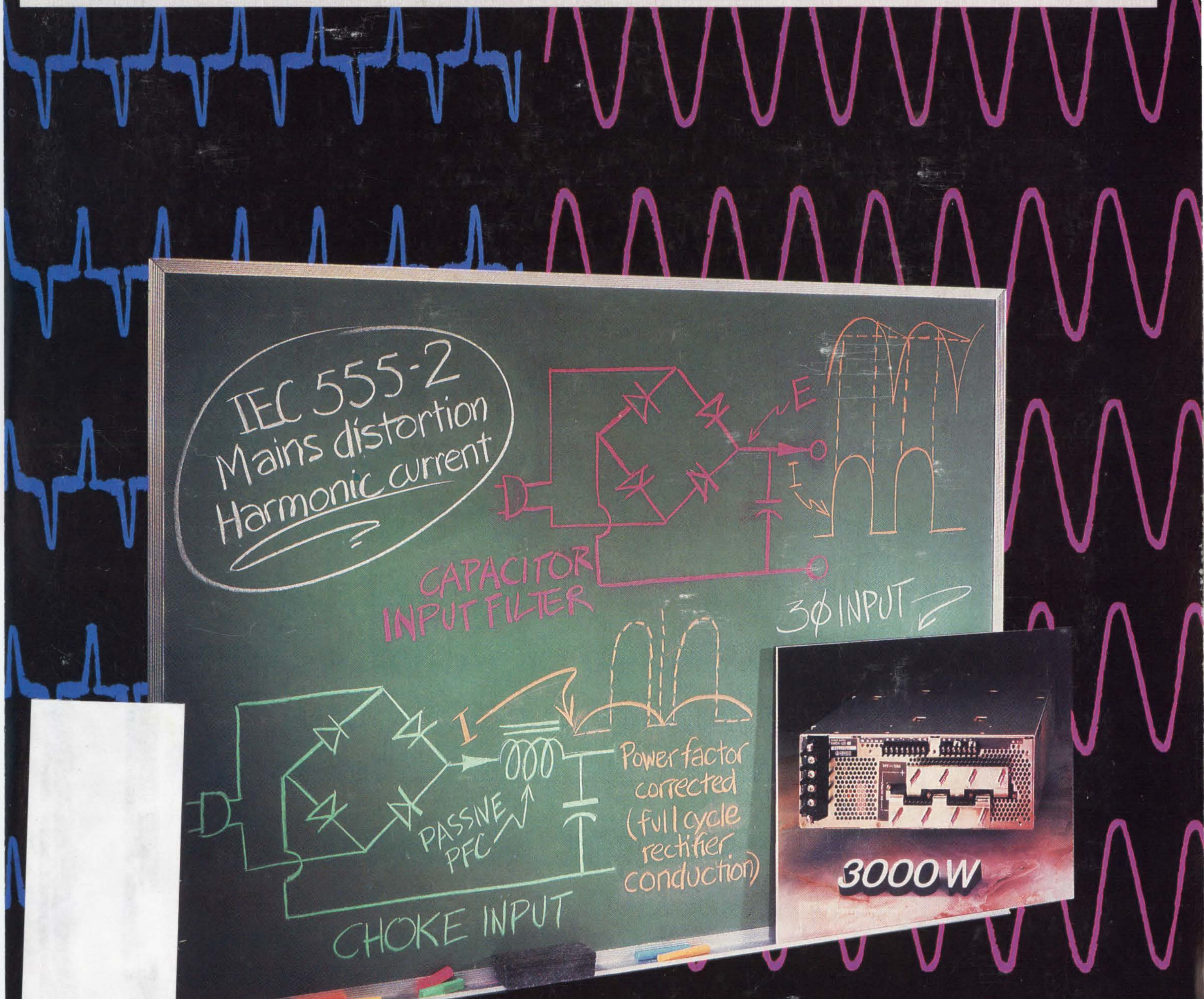
APRIL 11, 1991

EDN®

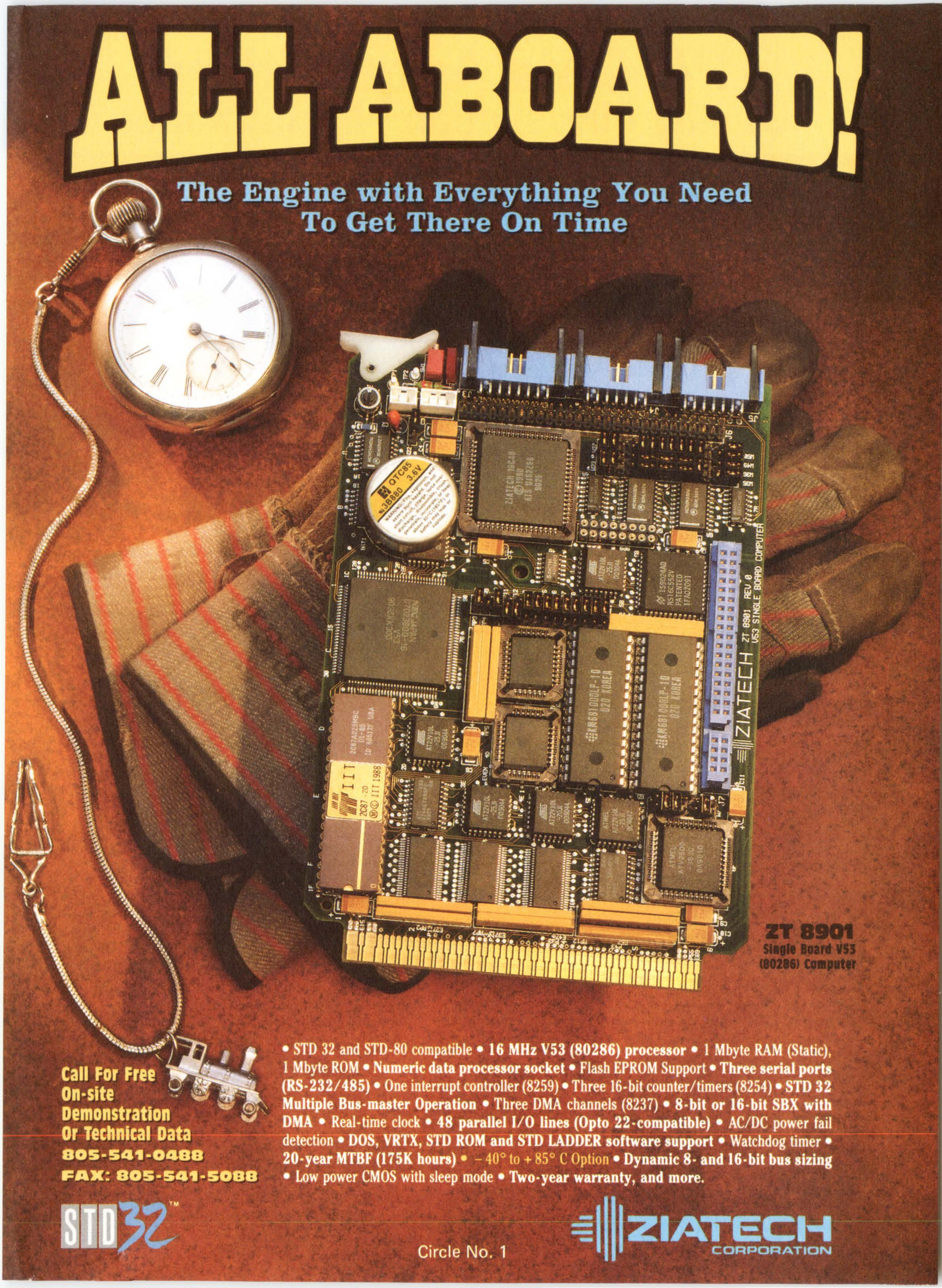
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



Special Report:

Switching supplies use chips and chokes to correct power factor

pg 90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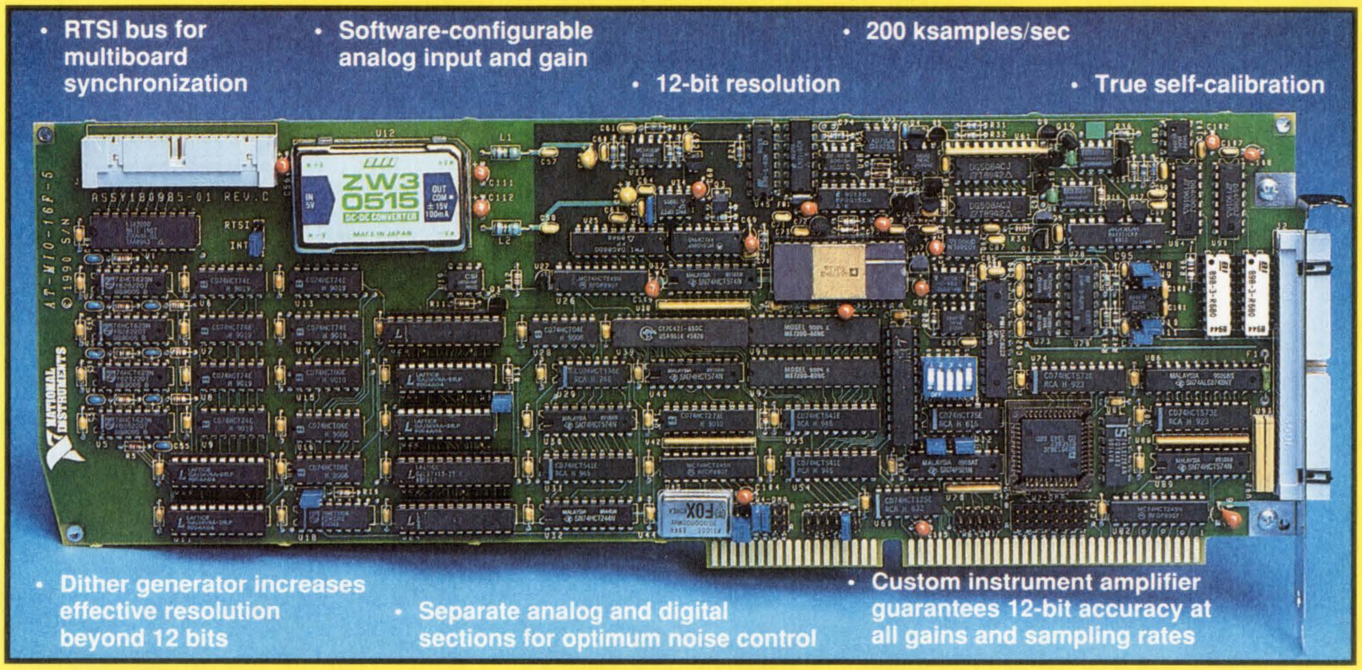

The National Instruments AT-MIO-16F-5 Sets the New Standard

It takes a serious commitment to quality to deliver data acquisition boards that reliably meet the most demanding specifications. Our new AT-MIO-16F-5 creates a new standard in excellence with several firsts, including a proprietary ultra high-performance instrumentation amplifier, a dither generator for extended resolution, and self-calibration that eliminates the need for external signals required by other "self-calibrating" boards. The quality, innovation, and performance of our AT-MIO-16F-5 sets the new standard in PC data acquisition. As the table below shows, the rest of our extensive PC product line surpasses industry standards. Each board undergoes a 48-hour burn-in, and passes a thorough system test to guarantee linearity, fast analog input settling, high common-mode rejection, and low noise. At National Instruments, we're serious about data acquisition.

Data Acquisition Board	Computer Bus	Channels*	Analog Input: Max Sampling Rate (samples/sec)	Analog Input: Resolution (bits)	Analog Input: Ranges (V)	Analog Input: Gains	Analog Output: Channels	Analog Output: Resolution (bits)	Digital I/O Channels	Counter/Timers	Software: LabWindows	Software: DOS LabDriver	Software: PC LabDriver	Software: Measure	Software: VisionScope	Software: Third Party
AT-MIO-16F-5	AT	16 SE 8 DI	200,000	12	±5, 0 to 10	0.5, 1, 2, 5, 10, 20, 50, 100	2	12	8	3	√	√				
AT-MIO-16H-9 AT-MIO-16H-15 AT-MIO-16H-25	AT	16 SE 8 DI	100,000	12	±10, ±5, 0 to 10	1, 2, 4, 8	2	12	8	3	√ √ √	√ √ √		√ √ √		√ √ √
AT-MIO-16L-9 AT-MIO-16L-15 AT-MIO-16L-25	AT	16 SE 8 DI	100,000	12	±10, ±5, 0 to 10	1, 10, 100, 500	2	12	8	3	√ √ √	√ √ √		√ √ √		√ √ √
Lab-PC	XT	8 SE	62,500	12	±5, 0 to 10	1, 2, 5, 10, 20, 50, 100	2	12	24	3	√	√	√	√		√
PC-LPM-16	XT	16 SE	50,000	12	±5, 0 to 10 ±2.5, 0 to 5	1	–	–	16†	3	√	√	√			
AT-DIO-32F PC-DIO-96 PC-DIO-24	AT XT XT	– – –	– – –	– – –	– – –	– – –	– – –	– – –	32 96 24	– – –	√ √ √	√ √ √	 √ √			√ √
PC-TIO-10	XT	–	–	–	–	–	–	–	16	10	√	√	√			
EISA-A2000	EISA	4 SE SS	1,000,000	12	±5	1	–	–	–	–	√	√			√	

Featured Product

* SE – Single-Ended, DI – Differential, SS – Simultaneous Sampling   † 8 Channels In, 8 Channels Out

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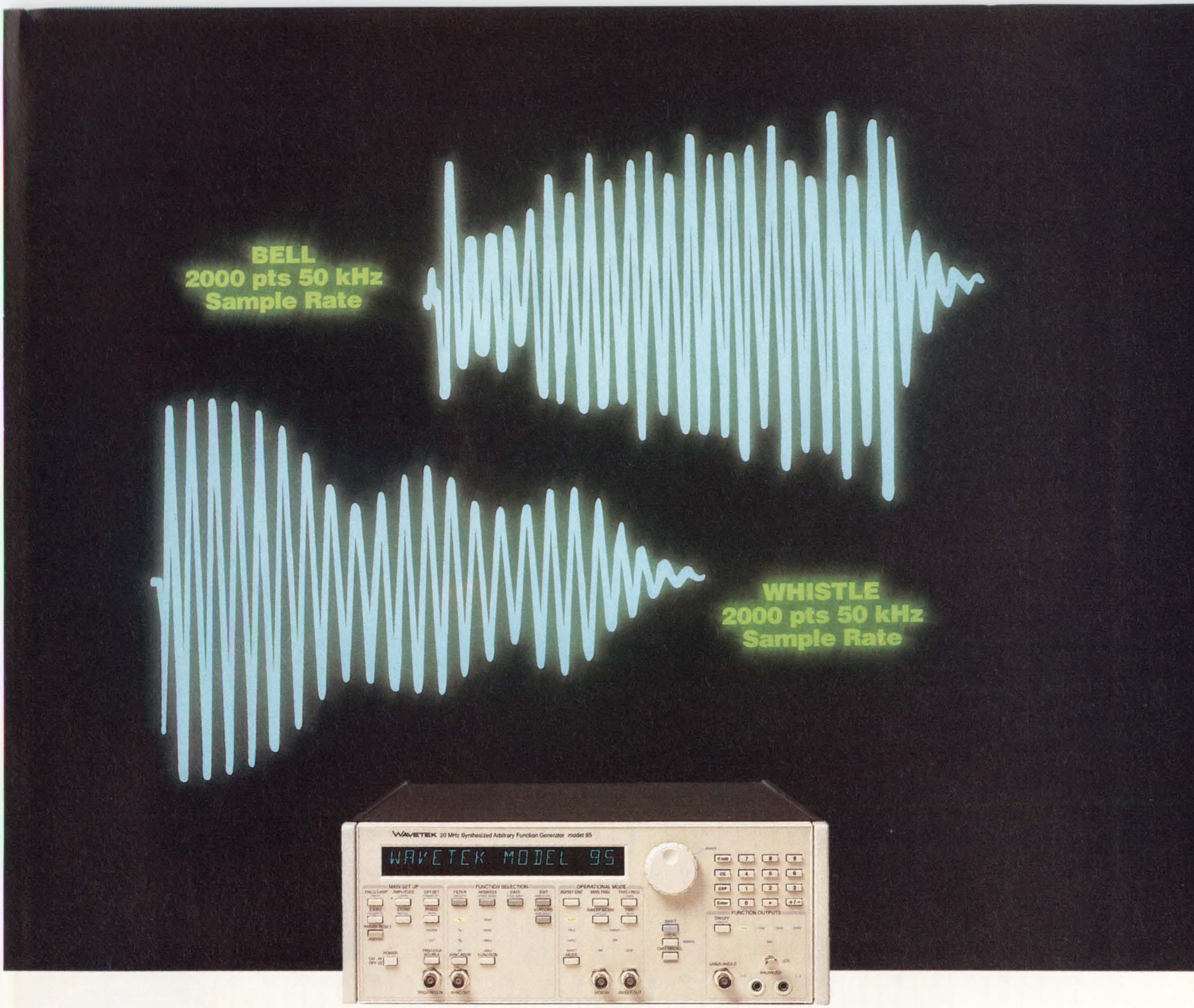

Our new function generator has all the bells and whistles.

In fact, it has any kind of waveform you can imagine. Because the Model 95 combines a high performance function generator with a powerful arbitrary generator.

As a function generator, Model 95 produces remarkably pure square waves, triangles and sines, from 1 mHz to 20 MHz with synthesized accuracy up to 0.001%. It has the power to output 15 Vp-p into 50Ω, and includes sweep, pulse and modulation modes plus four user-selectable output impedances. There's even an internal trigger generator for trigger, gate and burst.

If you'd rather be arbitrary, Model 95 gives you up to 128k of waveform memory to work with, and a sample rate of 20 MHz. Four different editing modes help you produce even the most complicated wave shapes quickly and accurately, while analog and digital filters allow you to create the purest output possible.

For information about all the other bells and whistles you'll find on the Model 95, call Wavetek San Diego, Toll Free at **1-800-874-4835** today.

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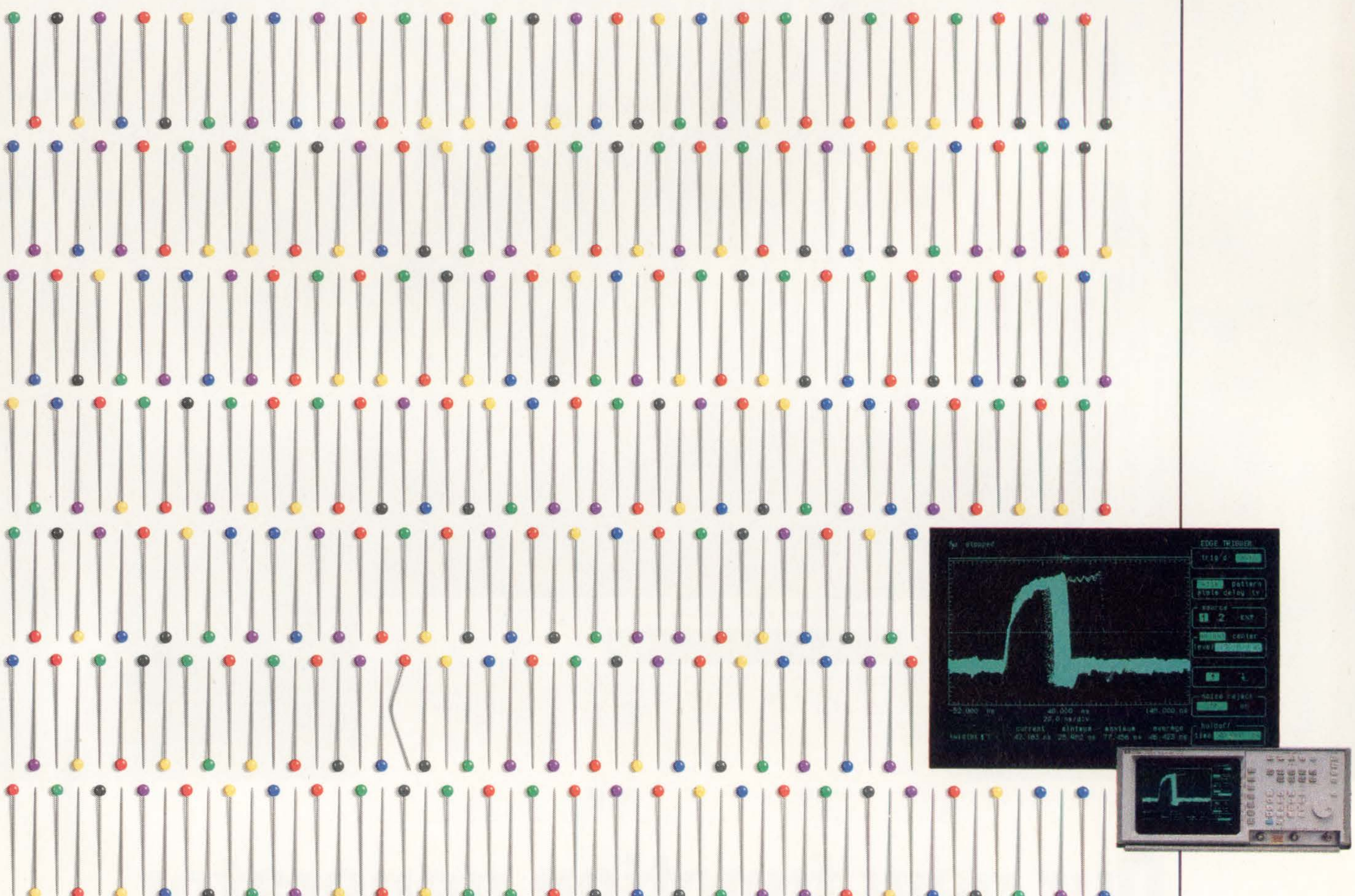

At $10,950*, you won't find a better value in a digitizing scope.

When you need to troubleshoot and debug digital designs fast, you can't afford to miss a thing. And now, you don't have to. The HP 54510A looks at a billion samples a second with a time-qualified pattern triggering and an infinite persistence display to pinpoint rare events and elusive glitches the instant they happen.

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So, if you're looking for a solution to high-speed trouble-shooting, call **1-800-752-0900****. Ask for **Ext. 1902**, and we'll send you an application note on the HP 54510A that shows you how to find faults fast.

*U.S. price only.
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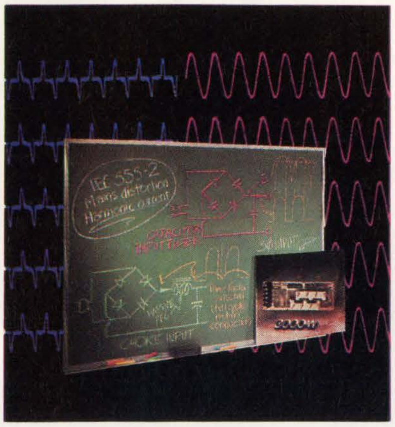
CIRCLE NO. 157

Volume 36, Number 8

EDN Magazine Edition

April 11, 1991

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *If you think your off-line switching power supply draws only sinusoidal current, you may be underestimating the incoming ac line current by as much as 40%. Supplies corrected for the input current's power factor—the result of the nonsinusoidal current waveshape—are better equipped to meet the needs of many ac-powered products. See our Special Report on pg 90. (Photo courtesy Kepco Inc)*

Continued on page 7

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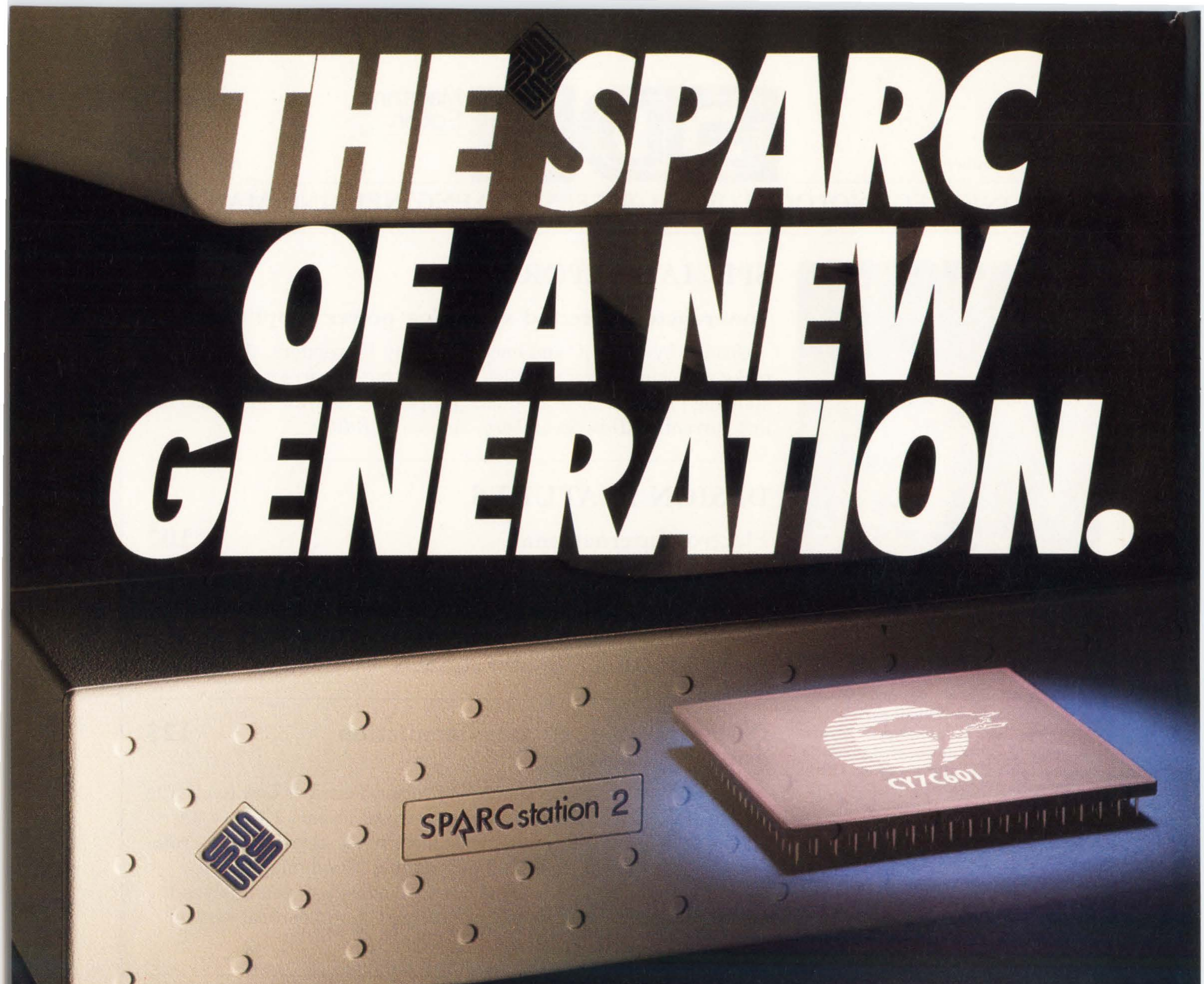
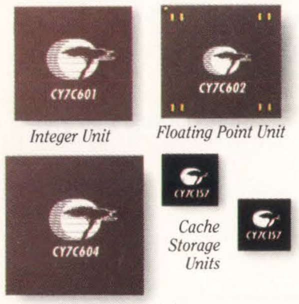
BPA ABP



A new generation of performance.

The new SPARCstation™2 from Sun Microsystems delivers almost twice the CPU performance of previous generations – the highest performance in its class.



Integer Unit

Floating Point Unit

Cache Storage Units

Cache Controller and Memory Management Unit

The complete SPARC chipset, designed by our ROSS Technology subsidiary, is now available for high-volume applications.

The reason for this blazing speed: The highest-performance CMOS SPARC® available. The CY7C601, 32-bit SPARC microprocessor and CY7C157 16K x 16 Cache Storage Units from Cypress Semiconductor. Cypress 0.8 micron CMOS gives the CY7C601 SPARC RISC microprocessor 40 MHz clock rates and a sustained throughput of 29 MIPS.

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Because they're SPARC chips, they're completely compatible with over 2100 SPARCware™ products. They offer true scalability into a wide spectrum of applications. And a growth path for future high-performance products.

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CYPRESS SEMICONDUCTOR

Continued from page 5

EDN Magazine Edition®

April 11, 1991

TECHNOLOGY UPDATES

PRODUCT UPDATES

NEW PRODUCTS

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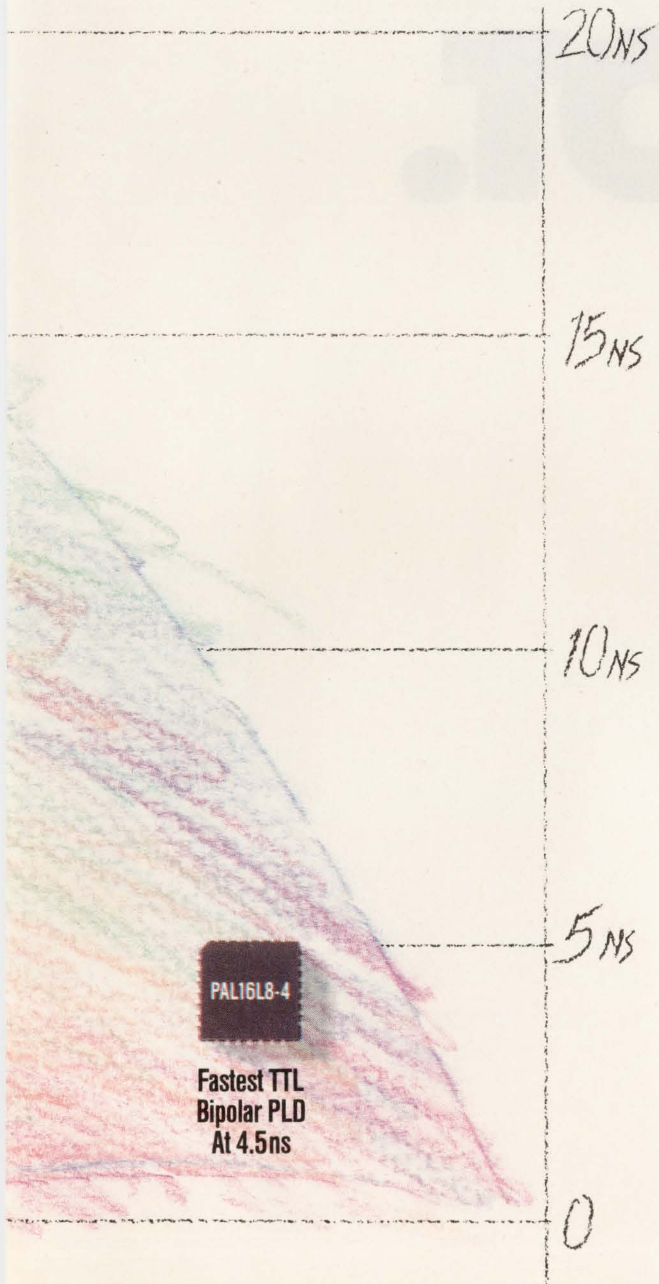

Whatever kind of PLD you need, the fastest comes from AMD.

We'd love it if all our work amounted to "zero." As in zero delay. And we're not far off.

Not surprising—because AMD invented the PAL® device. That's why we know programmables better. And offer you the most choices of the best devices.

Say you want speed, but can't sacrifice density. Don't. Use our new MACH™ products (Macro Array CMOS High-density) that give you up to 3600 gates and 15ns performance. They're two to three times faster than the competition and cost 40% less.

For more speed, along with low power consumption, try our new 10- and 15-nanosecond CMOS PLDs. Use our 16V8-10s and 20V8-10s anywhere you'd use a GAL® device. Or choose the ever-popular AMD-invented 22V10, at 15ns.

Faster still are our seventh generation bipolar PAL devices. Complete families of 16L8-5s, 20L8-5s, and the 22V10-10s. And for real speed freaks, we're now shipping a 4.5ns bipolar PAL device—the world's fastest TTL programmable logic.

Along with all this speed, we're providing equally fast delivery. In quantity. In fact, we deliver more programmable logic devices than all our competitors combined.

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"The world runs on infor silicon breakthroughs to right to the desktop."

HOW NATIONAL SEMICONDUCTOR IS HELPING YOU MEET THE CHALLENGES OF TODAY'S – AND TOMORROW'S – DATACOM AND TELECOM SYSTEMS.

John Jorgensen, National's Director, Advanced Communications Business Group, talks about applying advanced VLSI technology to next-generation communications systems.

Setting the stage for connectivity.

"National has a definitive strategy for providing voice- and data-communications solutions in silicon.

"We have solutions for Ethernet, FDDI, and integrated-digital networks. And we're working on next-generation solutions for ultra-high-speed network applications.

"The key to building devices this sophisticated is our experience with advanced analog+digital integration. We have all the enabling technologies. BiCMOS, CMOS, and ECL processes. Powerful design tools. Experienced analog +digital designers.

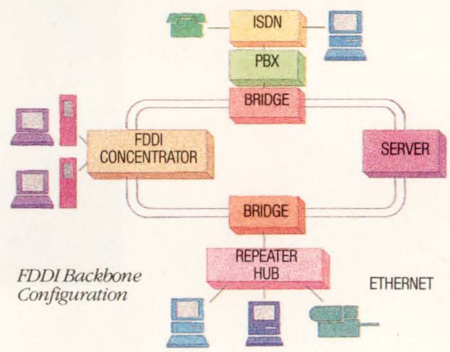
"It isn't easy. But we're doing it."

Linking LANs with FDDI.

"Our FDDI chipset provides the backbone that links Ethernet LANs at the workgroup level with integrated-digital networks, such as ISDN and SONET– and it provides the high-speed datapipe that links workstations directly.

"We're the first manufacturer to introduce a fully-integrated FDDI solution. It offers more network management features and consumes less power than any other solution.

"Our latest device, called the BSI, provides the system interface between our core FDDI chips and the host-system bus, such as VME,



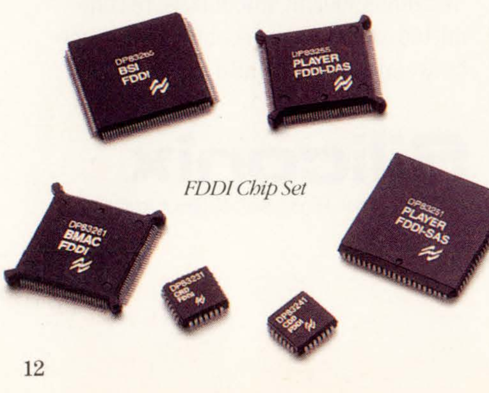
FDDI Backbone Configuration

AT, Microchannel, or EISA. It gives you the maximum available system bandwidth, with burst-mode transfers of 800Mbits/second through a 32-bit-wide data interface – without the need for an external processor.

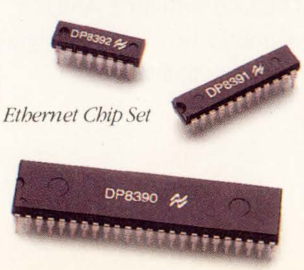
"So now you can develop products for highly-integrated FDDI networks, such as bridges, routers, and concentrators, or you can develop adapter cards for high-performance workstations and PCs – all from one supplier. National."

Linking the workgroup with Ethernet.

"Our SONIC – Systems Oriented Network Interface Controller – integrates, for the first time, a digital controller with a 10Mbit/second analog encoder/decoder.



FDDI Chip Set

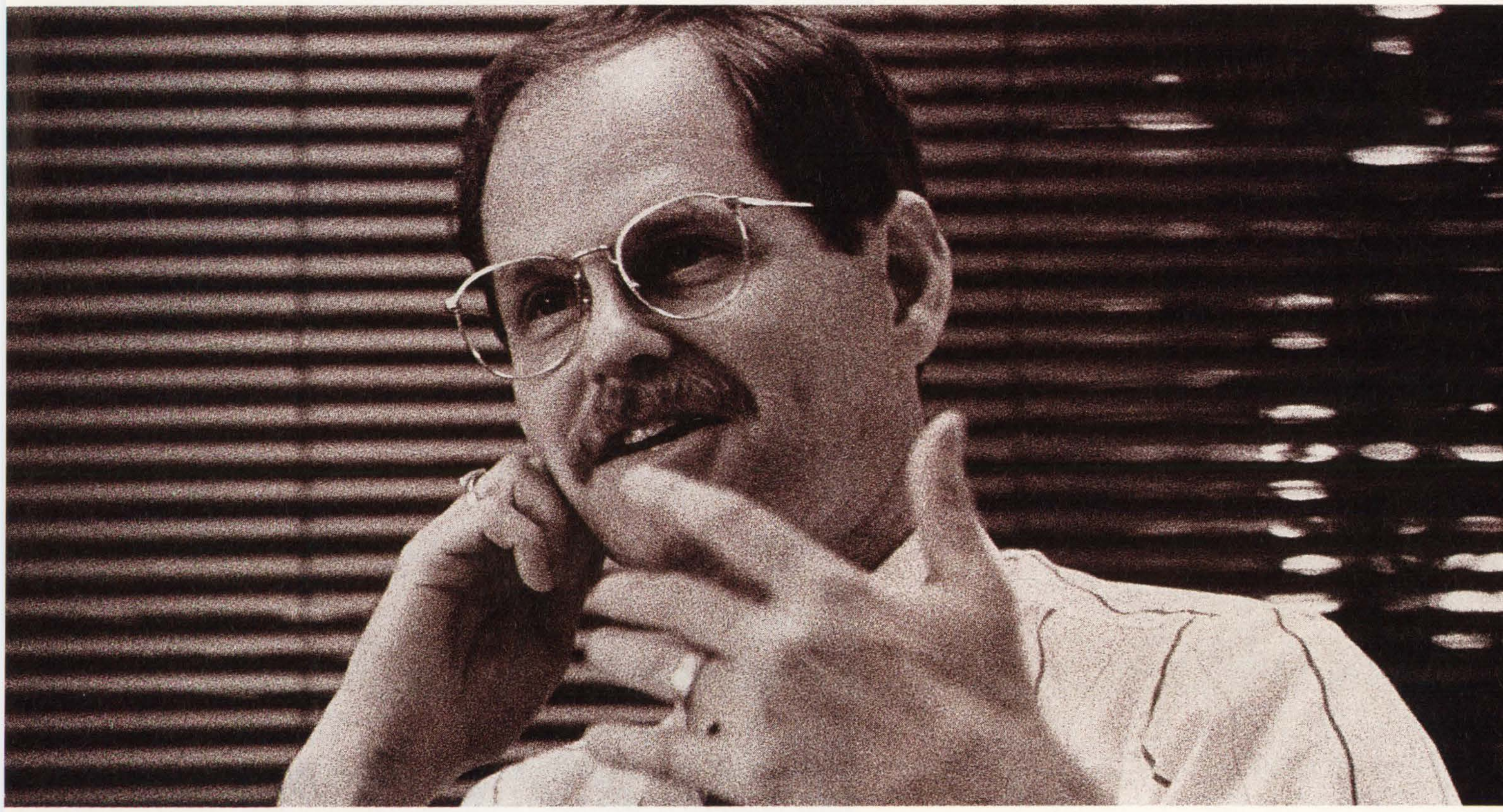


Ethernet Chip Set

SONIC

ISDN U Interface

mation, and we're making bring that information



"It supports all IEEE 802.3 functionality in a single chip that goes right on the motherboard in 16- and 32-bit systems, providing full network management functions in hardware.

"And with a transfer rate of 50 Mbytes/second, it's 20 times faster than most other solutions, and cuts bus occupancy by up to 80%.

"The workgroup is linking itself with Ethernet. And we're making it happen faster, smaller, and more cost effectively. That's the standard, and we're setting it."

Linking voice and data with ISDN.

"Our U interface breaks the ISDN logjam. It allows the simultaneous transmission of voice and high-speed data over the existing twisted-pair telephone network, providing the missing link between the subscriber and the central office.

"It may be the most technically complex mixed analog+digital device ever designed. The receiving front-end is analog, but the back-end signal processing is all VLSI digital. And this had never been done before. Until we did it."

Putting it all to work for you.

"The communications revolution is accelerating. As a datacom or telecom systems designer, I'd feel the need for advanced solutions to tomorrow's problems *today*. That's why I'd call National. Because we have those solutions. Today."

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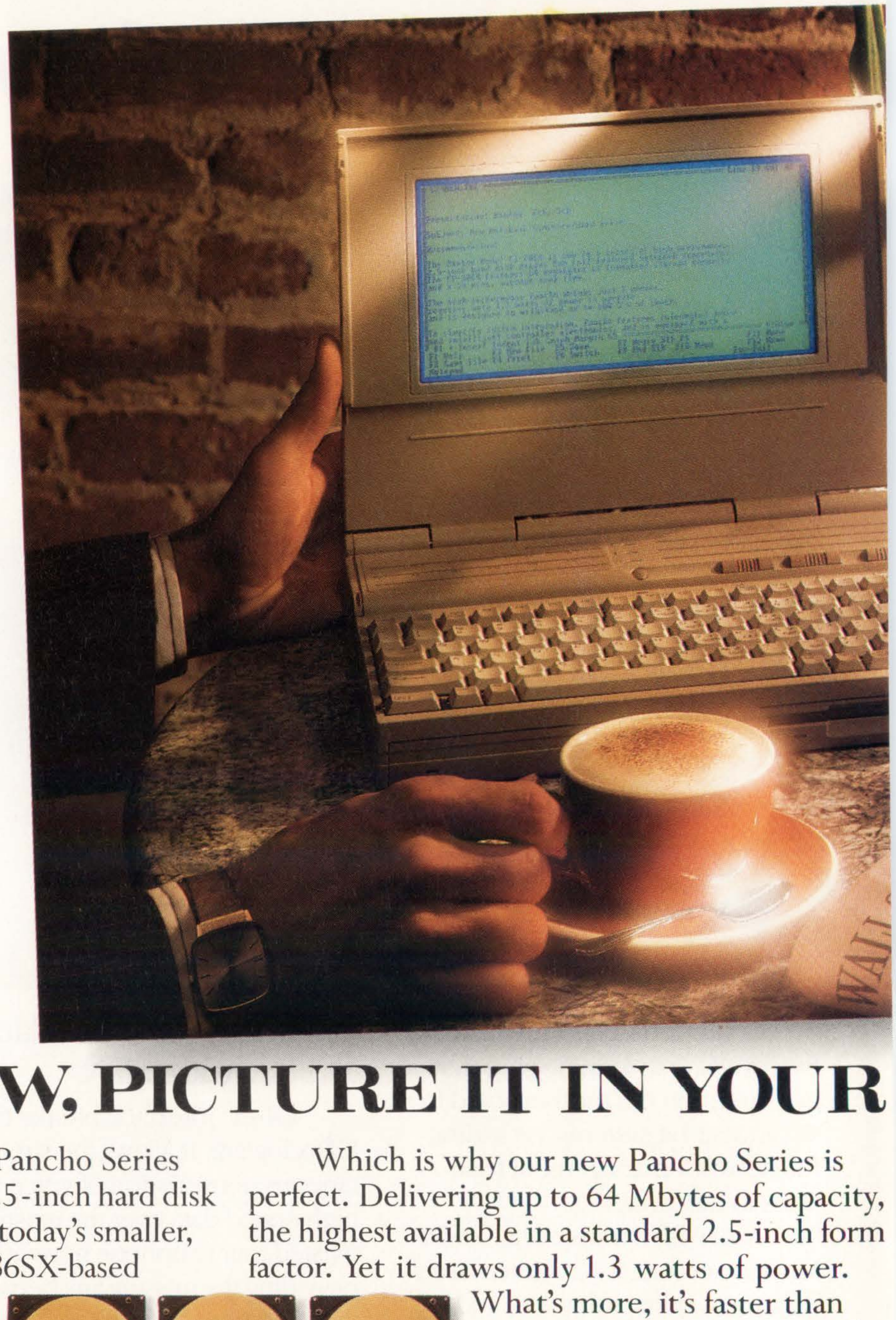
PICTURE A SMALLER,

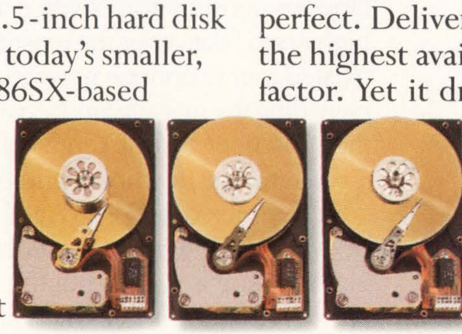
PICTURE IT WITH HIGHER



NOW, PICTURE IT IN YOUR

You've just pictured the Pancho Series from Conner. A new wave of 2.5-inch hard disk drives designed specifically for today's smaller, high performance 386- and 386SX-based notebook computers.

Advanced systems that need to run storage-intensive spread sheets, data base and graphics-oriented programs without sacrificing light weight or battery life.



The Pancho Series: 32MB, 42MB and 64MB of formatted storage.

Which is why our new Pancho Series is perfect. Delivering up to 64 Mbytes of capacity, the highest available in a standard 2.5-inch form factor. Yet it draws only 1.3 watts of power. What's more, it's faster than ever, with an access time of 19 msec.

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It's all a part of our innovative sell-design-build business philosophy. Even before we design or build a product, our engineers work closely with major systems manufacturers. To identify their specific needs sooner. Then fill them faster. As a result, we consistently design the exact disk drives our customers need.

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CIRCLE NO. 133

It's one thing to set the standard for an entire industry, as HP helped to do with FDDI. But it's quite another to follow it up with products that set the standard for performance and quality. Of course, that's just the HP way.

Case in point, our new integrated FDDI transceiver with integral MIC receptacle makes the most of its HP heritage. Engineered to meet and beat FDDI standards, this single-piece solution provides consistent performance over a wide range of operating temperatures and voltages. The bottom line is a 14.5dB power budget that exceeds the 11dB FDDI PMD standard, resulting in a comfortable 3.5dB design margin.

Attributes that stem directly from HP's role as a vertically integrated supplier. Which means we have direct control over all the active elements of our FDDI designs, ensuring you a consistently high quality product—and a constant high volume supply.

What's more, our new FDDI transceiver is just one part of a growing family of 1300nm products. Like our individual transmitter/receiver pair—for FDDI and general-purpose applications—that offer data speeds up to 200MBd. With more new and innovative products on the way.

So, if you're in the process of building a name in fiber optic networks, remember this—there's only one supplier of FDDI products worthy of the HP name. For more information, call HP today at **1-800-752-0900, ext. 1960**. We'll make it worthy of your time.

There is a better way.

HEWLETT PACKARD

CG08001

CIRCLE NO. 182

NEWS BREAKS

EDITED BY SUSAN ROSE

VMEBUS BOARD HAS KEYBOARD, DISPLAY, AND MOUSE

The GESVIG-4WVME interface card from Gespac Inc provides a user interface for your VMEbus system. The $1695 board incorporates a display controller that employs the Hitachi ACRTC video-controller chip, a keyboard interface that accepts IBM PC-style keyboards, and a serial interface port for a mouse. The board's video output can display 720 × 540 pixels using 256 colors. The board makes the video signals available on a front-panel DB-9 connector in the pin configuration used by IBM PC systems. Therefore, you can use any common PC CRT monitors. You can also buy a companion software package for the board: The $250 G-Windows Desktop Manager lets you implement a windowed user interface for Microware's (Albany, NY) OS-9 operating system. Gespac Inc, Mesa, AZ, (602) 962-5559, FAX (602) 962-5750, contact Don Bizios.—Steven H Leibson

SCOPES HIT STREET AT PRICES LOWER THAN PREDICTED

When Hewlett-Packard first announced its 2-channel 54600A and 4-channel 54601A 100-MHz digital scopes with "analog feel," the company expected them to cost $3000 and $3500, respectively (EDN, March 1, 1991, pg 76). Now that HP has actually started shipping the scopes, it has changed the prices to $2395 and $2895. Moreover, on orders of four units or more, a 10% discount applies. Hewlett-Packard, Colorado Springs, CO, (800) 752-0900.—Dan Strassberg

SPICE-MODEL LIBRARIES ADD SIMULATION ABILITIES

Analog Devices Inc and Burr-Brown Corp are the latest linear-IC companies to offer free disks of Spice models for their amplifiers. The disk from Analog Devices includes 176 models, some of which correspond to different performance grades of each of the company's amplifiers. This list includes all of the op amps from the company's newly acquired Precision Monolithics Div (formerly PMI). The library also includes current- and voltage-noise models for 26 of the devices, letting your Spice simulation predict system noise performance. The company's modeling technique lets the models use as many poles and zeros as needed to simulate each amplifier's frequency response accurately.

The 75 models in Burr-Brown's library include nearly all of the company's op amps, difference amplifiers, and instrumentation amplifiers. Three types of models are available: a standard macromodel, an enhanced macromodel, and a simplified circuit model. The company derived its macromodels using PSpice's (Microsim Corp, Irvine, CA) Parts and Enhanced Parts simulation software. The circuit model is a simplified transistor-level model that produces more accurate simulations but lengthens simulation time. The transistor-level models are available for some high-speed op amps; current-feedback op amps have simplified circuit models only. Analog Devices Inc, Norwood, MA, (617) 329-4700, FAX (617) 326-8703. Burr-Brown Corp, Tucson, AZ, (800) 548-6132, FAX (602) 889-1510.—Anne Watson Swager

QUARTZ-CRYSTAL OSCILLATOR MEETS MIL-883C

The QC6111 from Salford Electrical Industries Ltd is a quartz-crystal oscillator in an industry-standard 40-lead ceramic chip carrier. You can choose frequencies of 375 kHz to 30 MHz and frequency stability depending on the operating temperature range. For -40 to $+85°C$, the stability selection is either ± 35 or ± 60 ppm. For extended temperature operation from -55 to $+125°C$, the choice is ± 60 or ± 100 ppm. The module operates from a 5V supply, consumes 90 mW of power, and drives two standard TTL gates. The oscillator is designed in accordance with MIL-883C. Prices are £25 to £30 (1000), depending upon specification. Salford Electrical Industries Ltd, Heywood, UK, (706) 67501, FAX (706) 64394.—Brian Kerridge

EMULATOR CONNECTS TO SIMULATORS

Using the RPM Emulation System (starting at $70,000 for a 10,000-gate, 272-I/O configuration), you can prototype and emulate an ASIC in a system before you have working silicon. The Rapid Vector Evaluator (starting at $35,000) lets you drive the emulator from your simulator. The evaluator includes a cascadable 416-bit-wide port to Sun workstations and driver software that enables you to transfer test vectors and capture responses from the emulator. Simulation can then proceed as fast as your simulator can process vectors. You can also use the evaluator as a functional tester and for collecting vectors from operating hardware for driving your simulations. Quickturn Systems Inc, Mountain View, CA, (415) 967-3300, FAX (415) 967-3199.—Michael C Markowitz

GRAPHICS CHIPS ENHANCE DISPLAYS

Three graphics chips from Chips and Technologies enhance VGA, flat-panel, and 8514/A display systems.

The 82C453 ultra VGA controller has 1024×768-pixel resolution with 256 simultaneous colors. It interfaces to video RAMs for image storage, thus speeding the image transfer rate. The controller also uses a single-cycle read-modify-write operation to enhance windowing operations. It comes in a 160-pin plastic flat pack and costs $30 (1000). The 82C457 flat-panel controller supports a variety of color-panel technologies, including gas-plasma panels and supertwist-pneumatic, active-matrix thin-film transistor, and metal-insulator-metal color LCDs. It will also simultaneously drive a CRT with the flat panel. The controller uses techniques such as dithering to increase the number of colors beyond those provided by the panel alone, producing several thousand colors on a panel normally limited to a palette of 512. The $86.90 (1000) device comes with a flat-panel color palette/DAC and a clock synthesizer.

The 82C480 has a resolution of 1280×1024 pixels with 256 simultaneous colors. It conforms to the 8514/A graphics standard and supports as much as 4M bytes of video RAM. The company provides software-driver support for Windows 3.0 and AutoCAD 11.0, and BIOS and complete register specifications for applications software developers. The part costs $75 (1000). Chips and Technologies, San Jose, CA, (408) 434-0600, FAX (408) 434-0147.—Richard A Quinnell

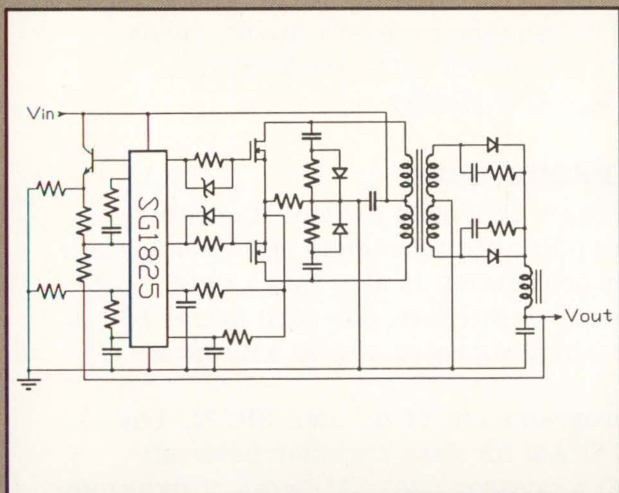
PERFORM REAL-TIME DATA ACQUISITION IN WINDOWS 3.0

Driverlinx from Scientific Software Tools gives you more than 70 command services for creating foreground and background I/O and measurement tasks. This tool provides language- and hardware-independent dynamic link libraries that port your data-acquisition applications to Windows 3.0. Applications communicate with the software by passing a "service request" that contains the specifications for a data-acquisition task. The software acknowledges the service request and notifies the application upon completion of each stage of the task. The package lets you operate

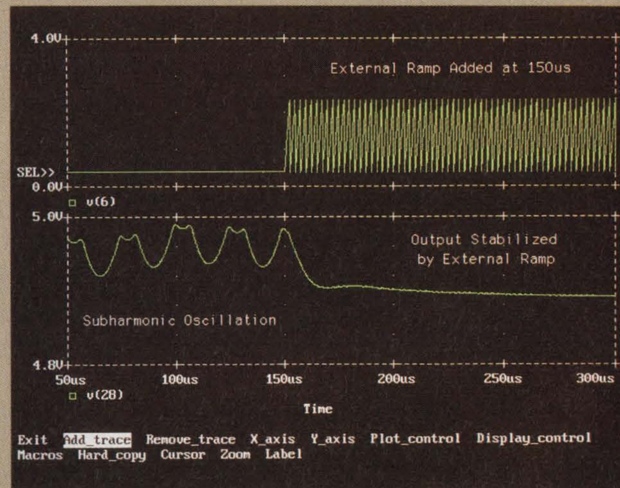
PSpice

MicroSim Corporation

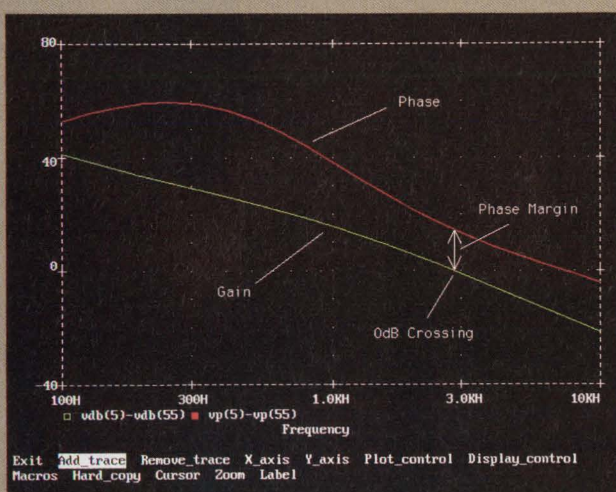
The Standard for Circuit Simulation Switch-Mode Power Supply Design



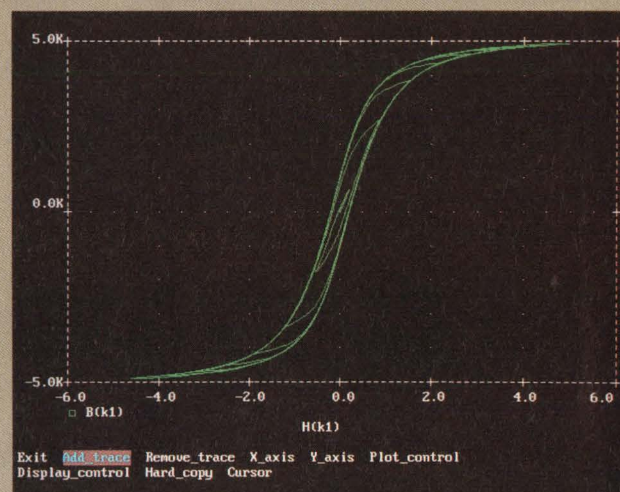
Current mode power supply schematic.



Power supply simulated using mixed analog/digital simulation. Plot shows subharmonic oscillation being suppressed by external ramp.



Simulation using the Vorperian switch model to examine the stability of a power supply.



Hysteresis curve of transformer.

A cycle by cycle simulation of switch-mode power supplies is recognized as a difficult simulation task for SPICE-based simulators, which must cope with timings that can span 4 orders of magnitude. This problem invariably results in very long simulation times, but is improved considerably by MicroSim's approach of building the controller macromodel chips so that a significant section is simulated in the digital domain. PSpice's behavioral modeling and mixed analog/digital simulation capability makes this possible.

PSpice is available on the IBM-PC (running DOS or OS/2); Macintosh II; Sun 3, Sun 4, and SPARCstation; DECstation 2100, 3100, and 5000; and the VAX/VMS families. In addition to the PWM macromodels, the PSpice library contains over 3,500 analog and 1,500 digital parts which can be used in a variety of applications. Our technical staff has over 150 years of combined experience in CAD/CAE, and our software is supported by the engineers who wrote it.

For further information about the PSpice family of products, call us at (714) 770-3022, or toll free at (800) 245-3022. Find out for yourself why PSpice has become the standard for circuit simulation.

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CIRCLE NO. 163

Keithley/Metrabyte, Advantech, Computer Boards, and Soltec data-acquisition boards within the real, standard, and enhanced modes of Windows 3.0. Adding multitasking and multiuser capabilities, the software can manage as many as six data-acquisition boards and 10 concurrent tasks. Multiple copies of one application or multiple applications can access this program without interfering with ongoing tasks. The $400 package conducts analog I/O, digital I/O, time and frequency measurement, event counting, pulse output, and period measurement. Scientific Software Tools Inc, Malvern, PA, (215) 889-1354, FAX (215) 889-1334.—J D Mosley

DSP CARD FOR MACINTOSH USES DUAL PROCESSORS

Spectral Innovations' MacDSPII is a dual-processor DSP card for the Macintosh Nubus. The card uses two AT&T DSP32C floating-point digital signal processors, each with 1M byte of static RAM (SRAM), for number crunching. It also has a 68000 μP to run Apple's Real-Time Operating System Executive. Further, the card offers 16-bit, dual-channel A/D and D/A converters that have sampling rates of 250 kHz max.

The DSPs run concurrently, each executing programs out of its own SRAM. The two processors share an additional 8M bytes of SRAM for data transfer between processors at a rate of 50M bytes/sec. The 68000 processor uses 2M bytes of dynamic RAM (DRAM), which is also part of the Nubus address space. Each DSP can access the DRAM and data converters via a parallel DMA port. Support for the $7995 card includes a C language compiler, assembler, and simulator, and a library of signal-processing and graphics subroutines. Spectral Innovations, Santa Clara, CA, (408) 727-1314, FAX (408) 727-1423.—Richard A Quinnell

SERIAL DATA-COMMUNICATIONS ICs GAIN SPEED

Zilog's 20-MHz version of the Z85230 enhanced serial communications controller (ESCC) and 16-MHz version of the Z16C35 integrated serial communications controller (ISCC) are general-purpose, multiprotocol, serial-controller ICs. They are 20 and 50% faster, respectively, than previous versions. The ESCC handles serial data rates to 5M bps, and the ISCC handles 4M bps when its on-chip DMA controllers manage the data transfers. The ESCC and ISCC cost $17.50 and $22.50 (1000), respectively. Zilog, Campbell, CA, (408) 370-8000, FAX (408) 370-8056.—Steven H Leibson

HIGH-DENSITY PLD HAS WIDE INPUT STRUCTURE

The PML2552 CMOS PLD from Signetics has the equivalent of 2500 gates and an unusual interconnect structure. You can connect the output lines from any of the device's 96 gates and 20 buried JK flip-flops to the input lines of any other gate and flip-flop, including folding the signal back on itself. To accommodate this plethora of signals, each product-term gate has 258 input lines. You can implement any combinatorial logic function with as few as two gate delays. Gate delays are 12 nsec, and the flip-flop toggle rate is 50 MHz.

The PLD also has both a low-power mode and a test mode. When you activate its low-power mode, the device freezes in its current state and drops power consumption from 525 to 52 mW. When in test mode, the device links its internal registers into a serial test loop, letting you monitor the registers' status using scan test techniques. The PLD comes in either a 68-pin J-leaded, windowed, ceramic quad flat pack for $60 or a 1-time programmable plastic leaded chip carrier for $20. Signetics, Sunnyvale, CA, (408) 991-3266, FAX (408) 991-2268, contact Khanh Le.—Richard A Quinnell


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Raju Joshi,
Project Manager
Sun Microsystems, Inc.

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Project Manager
Litton Systems Canada Ltd.

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Director, R&D and Custom Products
Dassault Electronique

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Sandy Hirschhorn,
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"The MultiSim Interactive Designer is excellent – it's the first CAE tool that works well with a top down design approach. It's set up so you can build and simulate block by block, and its speed makes it easy to find your mistakes, make changes, and try again without a lot of time spent recompiling."
Steve DeLong,
Technical Team Leader
Jim Walsh,
Technical Staff Member
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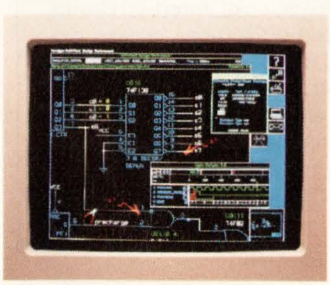

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SIGNALS & NOISE

More serious threat to US than Japanese competition

In Jon Titus's editorial (EDN, January 3, 1991, pg 35), he identifies a much more serious threat to US industry than Japanese competition. As long as I can remember, telephone operators (and many secretaries) seemed to be much more interested in getting rid of the caller than helping the caller reach the right person.

Answering machines have compounded the problem. Only the rare corporate species of "self-starters" muster the energy to even look for messages, never mind answer them. (After all, a body at rest wants to stay there.)

Once I had to clarify a spec within a half hour—the typical turnaround time for the copy desk— and spent the time listening to messages and menus from the company's voice-mail system. Finally, on my third try for Jim Neverin, assistant marketing manager, I did leave a message: "Jim, since no real people seem to work for your company, I'm placing my order with XYZ Corp."

The next time I needed Jim, his secretary answered and put me right through. Of course, that was sheer coincidence.

Max Schindler
Boonton, NJ

Accommodating the little guy

Scott B Rosenthal of Microsol Corp recently wrote concerning his problems in getting small quantities of parts. At our consulting and contract-engineering company, we face similar problems. We don't manufacture anything, but we often need small numbers of parts to build prototypes. I concur that in recent years it has become increasingly difficult to obtain small quantities.

I sometimes request samples. But I don't like doing this, because it leaves us entirely at the mercy of manufacturer's reps who don't always appreciate the time constraints we are under.

To the Hamilton Avnets and others who don't really want to be distributors except to the big guys, I have this to say: Not all little companies stay little, and some remember who served them and who didn't.

Stephen D Anderson, President
Ansco
Minneapolis, MN

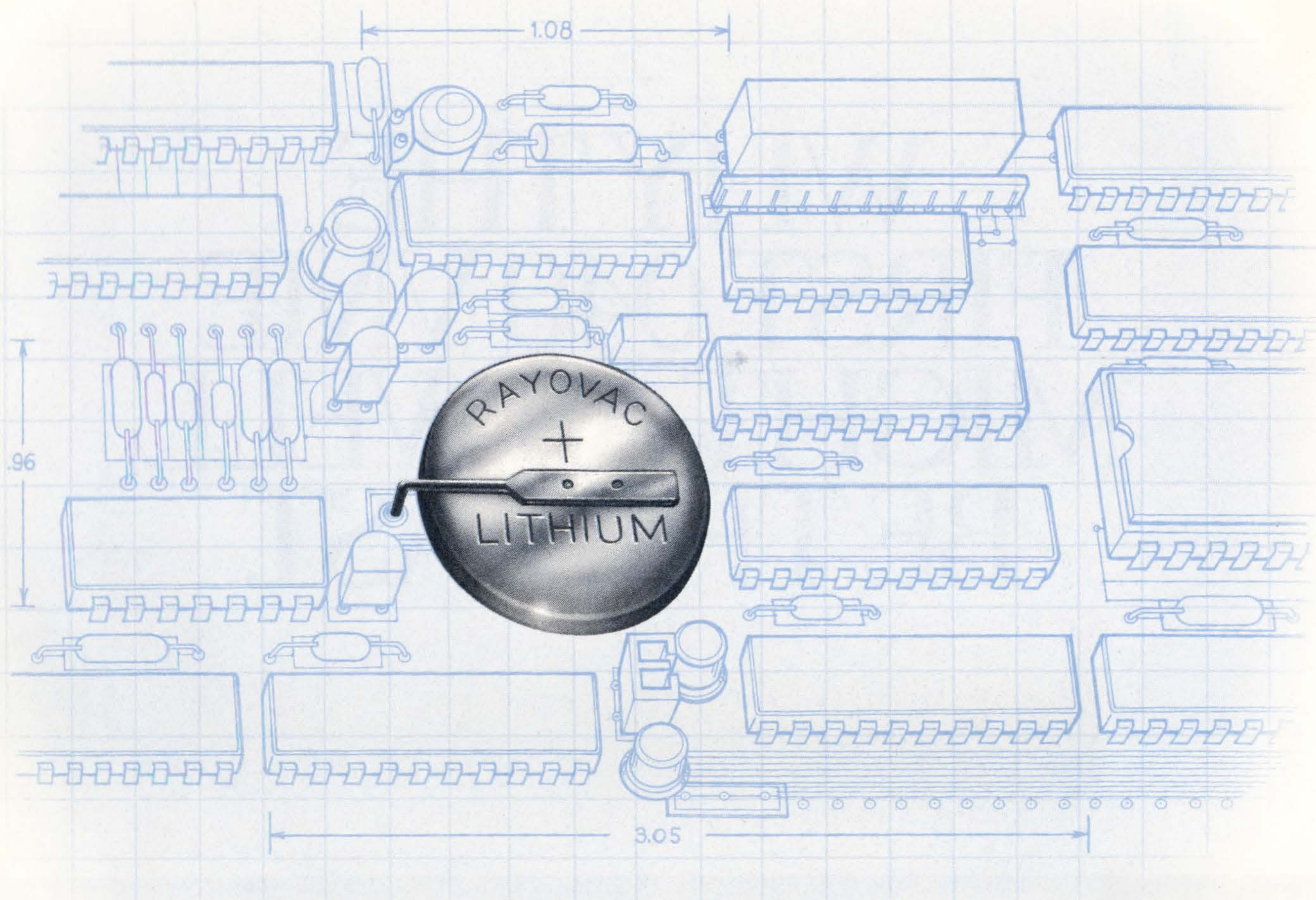
Correction for µP Directory

EDN's 17th Annual Microprocessor Directory (November 22, 1990, pg 115) lists the SGS Thomson ST9 µP chip as a derivative of the Zilog Z8. SGS Thomson reminds us that, although the company is licensed by Zilog to produce the Z8 µP, members of the ST9 µP family use a separate and distinct computer architecture, as well as an instruction set that's incompatible with the Z8. Thus, the ST9 is not a derivative or an enhancement of the basic Z8 µP.

IT'S EASY TO HAVE YOUR SAY

EDN's Signals & Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. You can use one of several easy ways to reach us. First, there's always the mail. Send your letters to Signals & Noise Editor, EDN Magazine, 275 Washington St, Newton, MA 02158. Or, send us a message via MCI mail at EDNBOS. Finally, EDN's bulletin-board system is ready for use—and it's free (except for the phone call). You can reach us at (617) 558-4241 and leave a letter in the EDITORS Special Interest Group. You'll need a 2400-bps or less modem and a communications program that is set for eight data bits, no parity, and one stop bit, or 1200/2400, 8N1 in shorthand.

EDN



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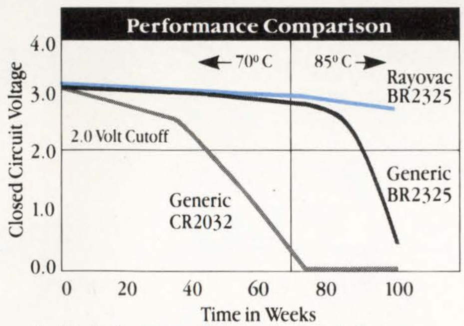

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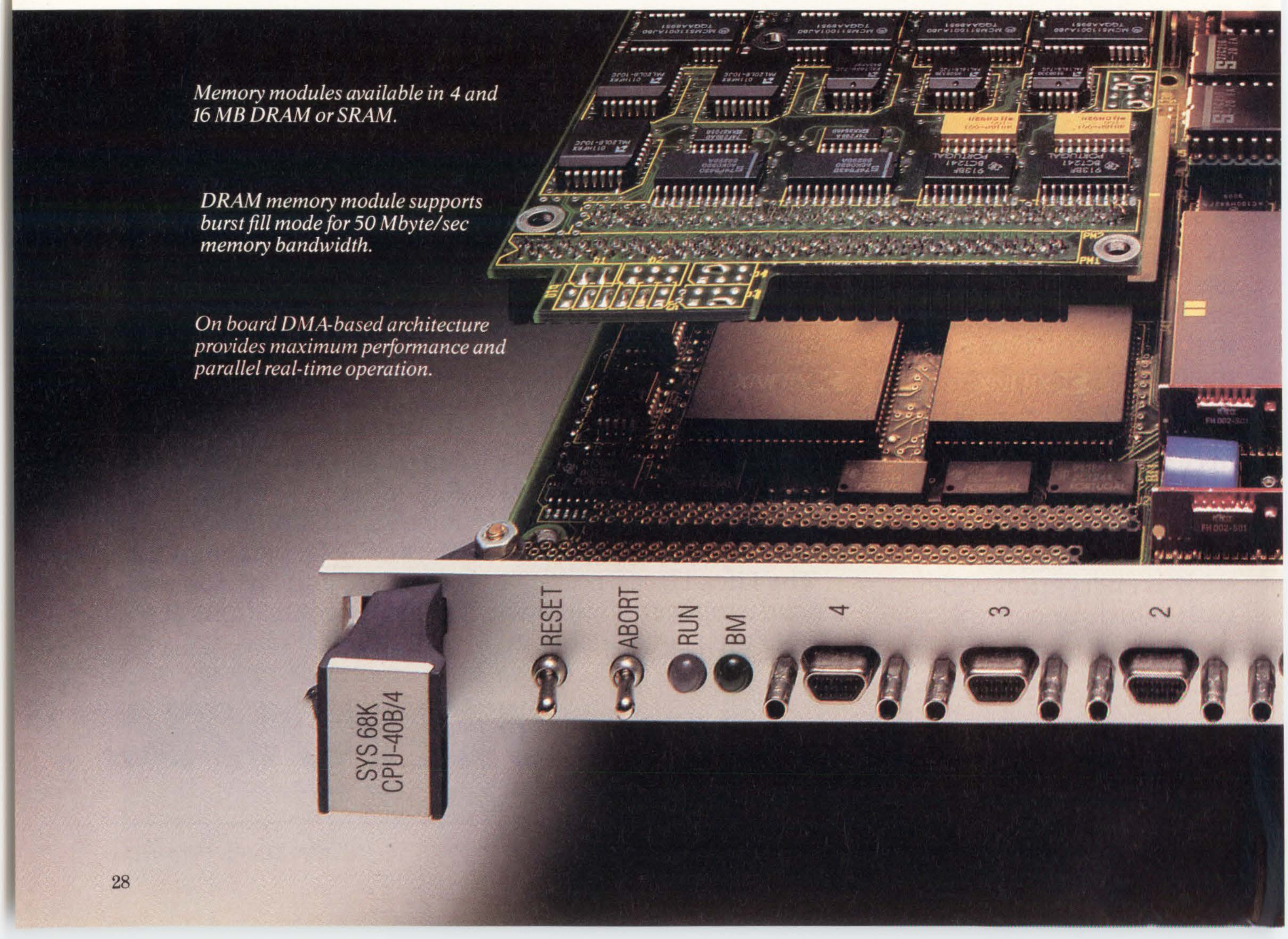
CIRCLE NO. 172

WHY THE FIRST 040 VME MIGHT AS WELL BE THE LAST.



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CPU-40 PERFORMANCE CHARACTERISTICS

Data from	CPU	CPU	CPU	CPU	VMEbus	SCSI*	Floppy Disk*	Ethernet*	Shared RAM*	VMEbus*
Transfer to	Shared RAM	EPROM	Serial I/O Timers	SCSI, Ethernet Controller, Floppy Disk	Shared RAM	Shared RAM	Buffer RAM	Dual-port RAM	VMEbus	VMEbus
Transfer Speed	53.7 MB/sec	16 MB/sec	2 MB/sec	2 MB/sec	5 MB/sec	4 MB/sec	500 KBit/sec	10 MBit/sec	15 MB/sec	15 MB/sec
Local 68040 CPU Operation	100%	100%	100%	100%	70%	80%	100%	100%	75%	100%

*DMA x FPS

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*Actual dhrystone results may vary depending on compiler used. **Computer Design News, March 12, 1990.

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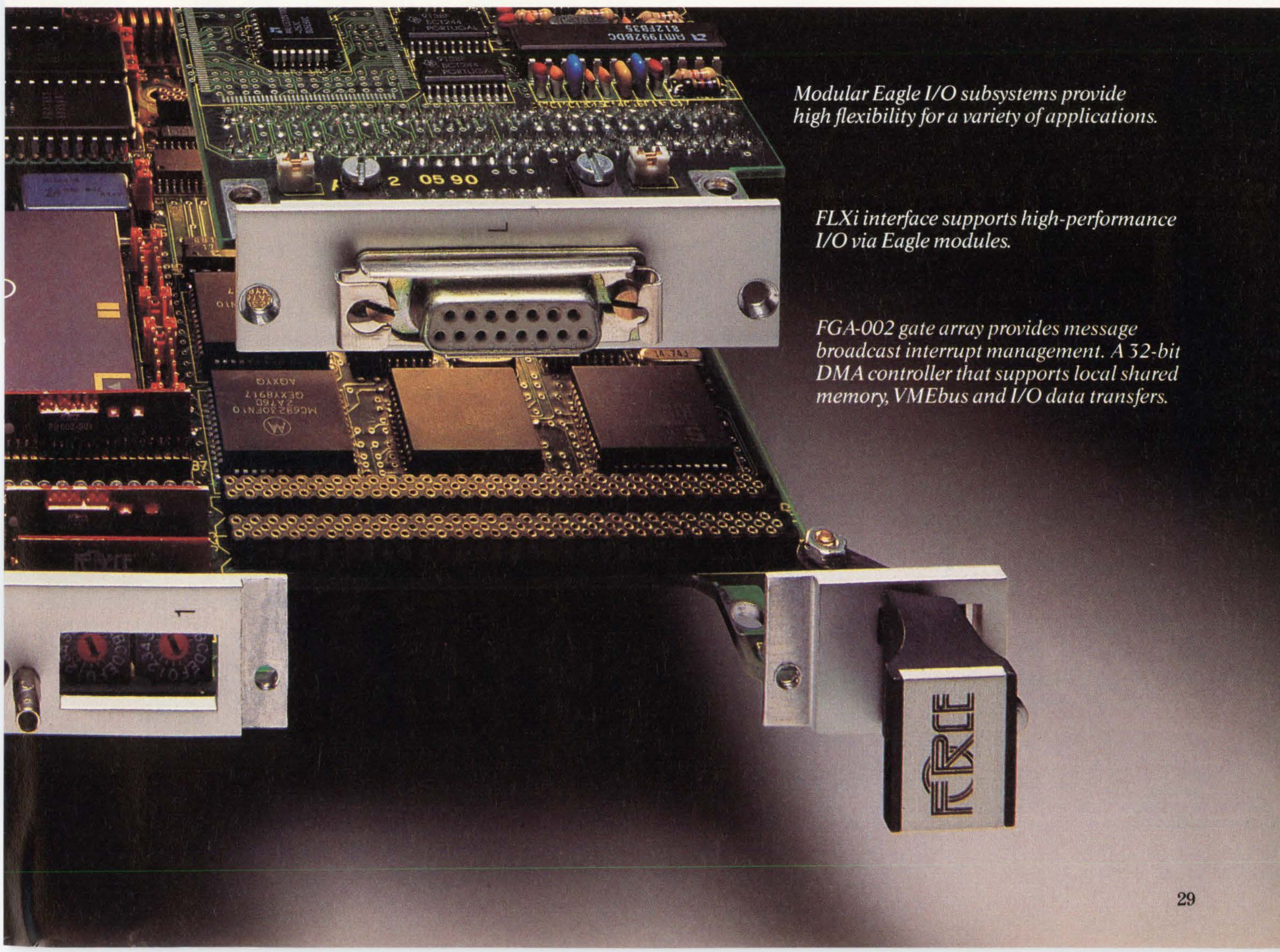

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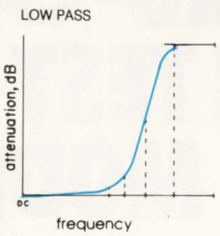
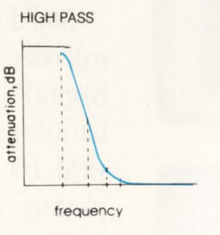


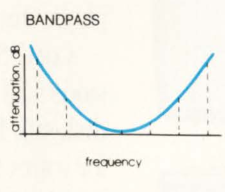
MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	(loss>40dB) Max.	Min.	VSWR pass-band typ.	stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

high pass dc to 2500MHz



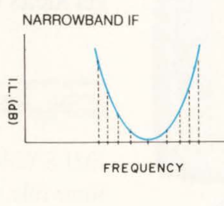
MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	(loss>40dB) Min.	VSWR pass-band typ.	stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

bandpass 20 to 70MHz



MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	Max. F4	(loss > 20 dB) Min. F5	Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

narrowband IF



MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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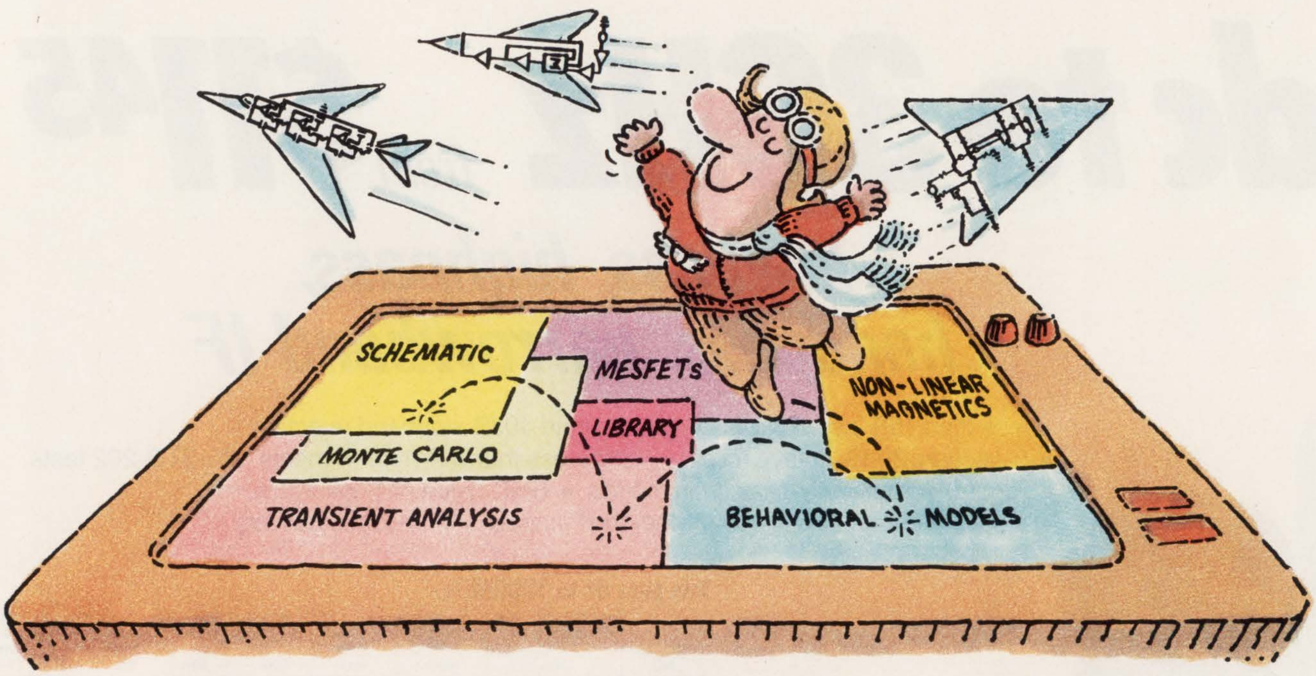

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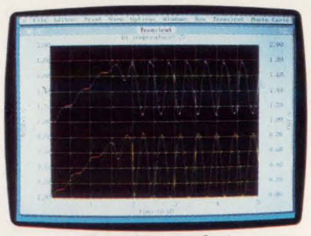
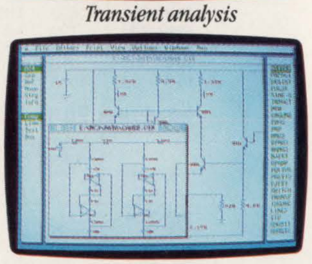
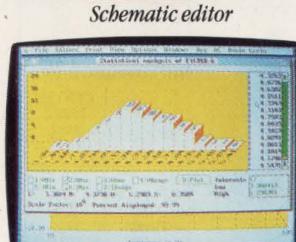


Transient analysis



Schematic editor



Monte Carlo analysis

And don't forget MICRO-CAP III's extended routine list—from impedance, Nyquist diagrams and BH plots to Monte Carlo for statistical analysis of production yield. The algebraic formula parsers for plotting virtually any function. The support for Hercules, CGA, MCGA, EGA and VGA displays. Output for plotters and laser printers.

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CIRCLE NO. 176

ASK EDN

EDITED BY JULIE ANNE SCHOFIELD

Have you been stumped by a design problem so long that you don't know who to turn to? Are you having trouble locating parts? Finding companies? Can't interpret a spec sheet? Ask EDN.

This department will serve as a forum to solve nagging problems and answer difficult questions. EDN's editors will provide the solutions. If we can't solve a problem, we'll find an expert who can, or we'll print your letter and ask your peers for help. We can't answer every question, but we'll try to publish the ones that will help you most in your job.

Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS. Or, send us a letter on EDN's bulletin-board system. You can reach us at (617) 558-4241 and leave a letter in the /ask_edn Special Interest Group.

Gas-sensor circuit found

I'm looking for a circuit diagram of a gas and smoke alarm, gas monitor, gas sentinel, electronic gas detector, or gas analyzer that uses the Figaro (Wilmette, IL, (312) 256-3546) 813 or 822 gas sensor. Green, yellow, and red LEDs should indicate low, medium, and high gas concentrations, respectively. Such a system could also be a fire alarm because the sensor detects smoke also. Thank you for your help.

Dilip S Poudwal
Ocean Star CHS/G-5
Bombay, India

Linear Technology Corp's Application Note 11, "Designing Linear Circuits for 5V Operation," (September 1985) describes a circuit for a linearized methane transducer signal conditioner that uses the Figaro 813 sensor. You can contact the company at 1630 McCarthy Blvd, Milpitas, CA 95035. (408) 432-1900. FAX (408) 434-0507.

Alternate source located

We are using DM2502 successive approximation registers made by National Semiconductor. This device has been obsoleted by National Semiconductor. Please let us know of alternate sources or devices.

V Ramasubramaniam
R&D Manager
Systronics
Naroda, India

According to Brent Rowe, marketing manager for digital memory products at National Semiconductor, Rochester Electronics Inc now manufactures DM2502s. You can contact the company at

Rochester Electronics Inc
10 Malcolm Hoyt Dr
Newburyport, MA 01950
(508) 462-9332
FAX (508) 462-9512.

Readers and sources linked

In the January 21, 1991, issue of EDN, Mr Christer Berg requested a source for National Semiconductor's NS405-A12N microprocessor. We have a supply of 234 used NS405B12N microprocessors that may be of use to him.

The A12 uses a 5×7 type font, whereas the B12 uses a 7×9 type font, but both operate at a 12-MHz video rate. These parts were used for less than one year in a video board; we are unlikely to use the board design in the future. While awaiting our management's permission to release or sell these parts, it would be useful to know if they are of any value to Mr Berg. Please pass our phone number along to Mr Berg or relay his number to us.

Mark Foan
Manager of Technical Services
British Columbia Lottery Corp
Kamloops, BC, Canada

In the January 21, 1991, issue, someone was looking for National Semiconductor part number NS405-A12. We have some available. Have persons contact me.

Roland Levin
Videomedia
Sunnyvale, CA

We also are in need of National Semiconductor part NS405-A12; therefore, we would appreciate a source for these chips.

Forest C Sprague
Adaptrol Inc
Pontiac, MI

The appropriate parties have been put in contact with each other.

Reader seeks piggyback plug

Can you find out who manufactures piggyback plugs? A piggyback plug is a service cord with an in-line series 3-prong plug.

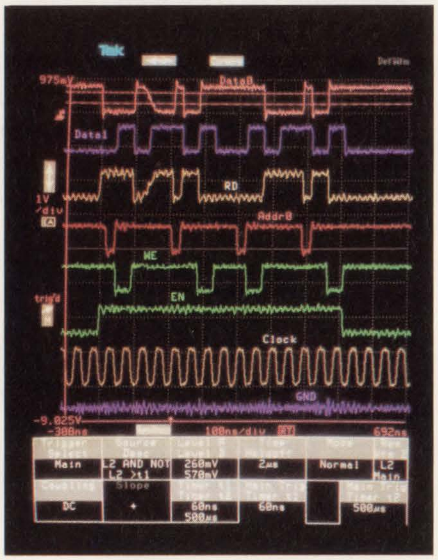
Larry Shields
Custom Switches Inc
Manvel, TX

Belden Wire & Cable has a standard product #17666 that has a male and female connector on the same end of the cord. You can contact the company at

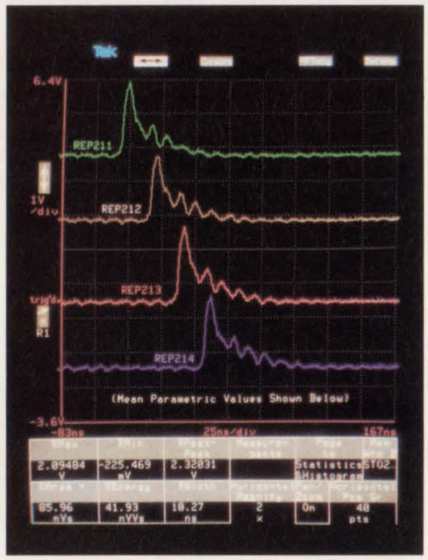
Belden Wire & Cable
Box 1980
Richmond, IN 47375
(800) 235-3364;
in IN, (317) 983-5200
FAX (317) 983-5294.

EDN

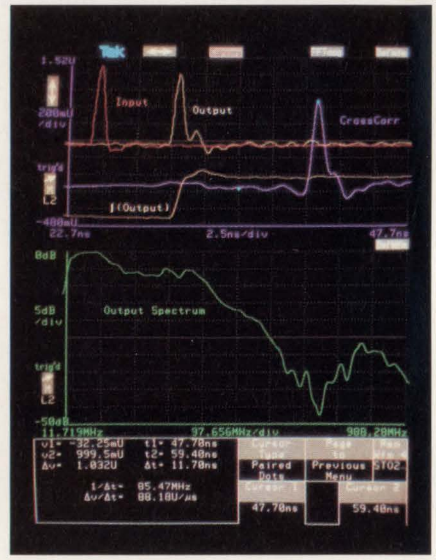
Get S



Extended triggering. Sophisticated triggering in the DSA600A reliably discriminates glitches, transition slew-rates, runt pulses and timing violations. Long memory and pre-trigger help reveal the cause.



Transient capture, analysis and storage. Capture a series of transient events with automatic labeling and parametric analysis. Examine statistics of each measured parameter over the ensemble. Transport results using built-in (DOS-compatible) floppy disk.



Advanced signal processing. Transform and combine acquired waveforms at visual real-time speeds to reveal key phenomena. FFT, correlation, convolution and calculus functions provide multiple views of critical events.

When you need serious measurement, serious analysis, serious accuracy, nothing—but nothing—delivers it like Tek DSA 602A and 11403A oscilloscopes.

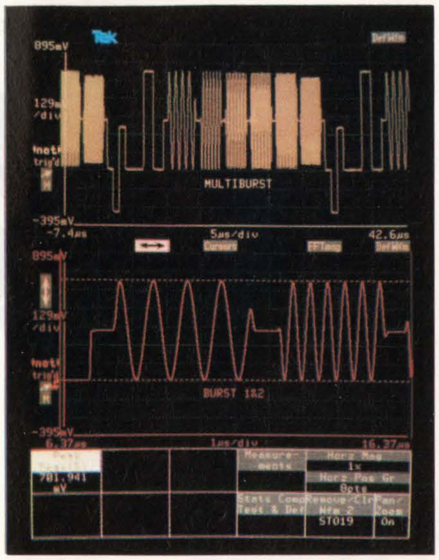
When you expect your instruments to be as serious about the truth as you are, only the DSA602/11403A, with their superb new amplifiers and probes, their unrivaled accuracy, plug-in flexibility, and their powerful new set of waveform analysis and measurement functions, come through with results like you see above.

Serious numbers? Try the new 2 GS/s, 1 GHz bandwidth Tek DSA 602A. No other scope combines DSP hardware for live displays of FFTs, correlation or convolution, plus high signal fidelity and powerfully selective triggering modes. There's even a new disk drive in this latest DSA version to save setups and data.

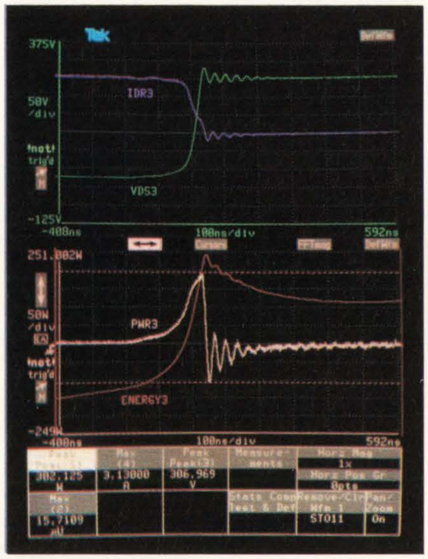
Pit the new 11403A Digitizing Oscilloscope, with 1 GHz bandwidth and 10-bit vertical resolution, against the toughest repetitive signals. Get more than 30 pushbutton measurements, with statistical analysis and built-in pass/fail decisions from the most accurate scope of all. Put its new FFT features to work measuring total harmonic distortion, or use the statistical data base to characterize jitter.

Configure and reconfigure your scope with new plug-ins like Tek's programmable 50 MHz current amplifier, four-channel 75Ω video amplifier and high-resolution video trigger. Choose from our true differential amplifier and voltage comparator, our 50Ω and high-impedance amplifiers. Take advantage of their unequaled overdrive recovery and wide dynamic

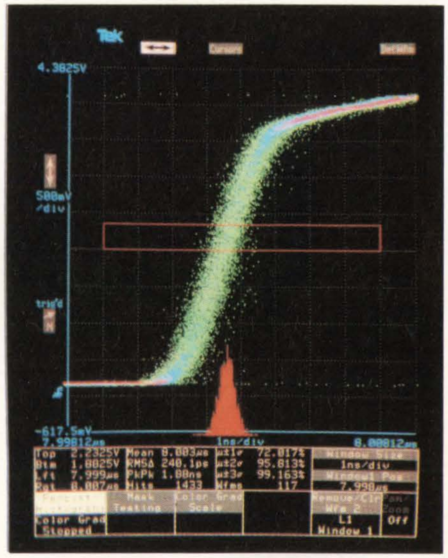
erious!



Video and HDTV. Analyze video waveforms, including HDTV. Line and field select on up to 1280 lines with the new 11T5H Video Trigger Unit. New 4-channel 11A34V 75Ω Video Amplifier provides excellent signal fidelity up to 300 MHz.



Current and power. Make accurate, high-bandwidth power measurements and energy calculations with our new 11A16 Programmable Current Amplifier. Current and voltage maintain their proper phase relationship to 50 MHz.



Jitter and noise analysis. Analyze jitter and noise with Tek's exclusive statistical data base. Color grading, statistic readout and histograms clearly show the distribution of the edge jitter.

range, while you mix and match to the capabilities, channels and bandwidths you need.

Finally, choose from our high-impedance, high-bandwidth probes for fast logic devices . . . high-voltage and current probes for power conversion analysis . . . optical-to-electrical converters for direct measurements on lightwaves . . . and more, from the best probing resource around.

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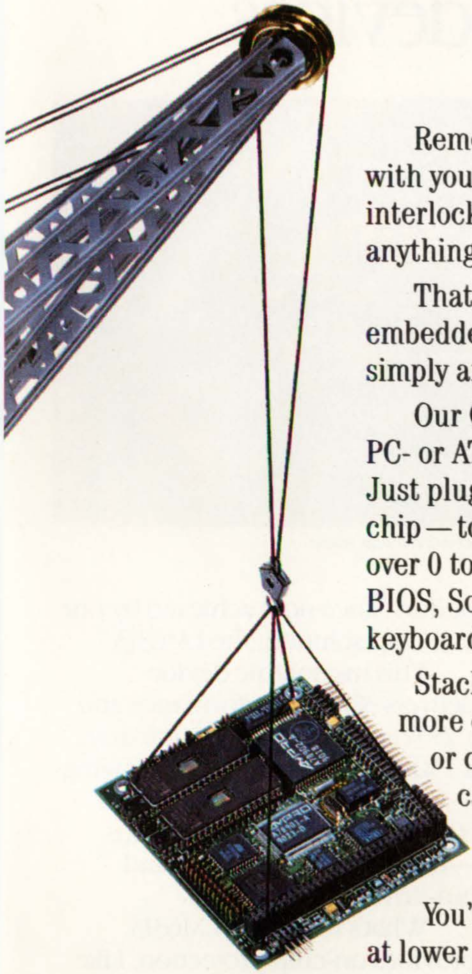

Remember the challenge of constructing "engineering marvels" with your Erector® set? That red metal box held a complete set of interlocking pieces—all that was needed to assemble just about anything. Your imagination was the only limitation.

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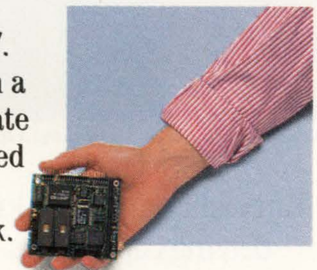

Our CoreModule™ family packs ready-made full PC- or AT-compatible intelligence into 3.6″ x 3.8″ x 0.6″. Just plug one into your circuit board—like plugging in a chip—to easily interface to your own logic. They operate over 0 to 70°C, and include a CMOS CPU, RAM, extended BIOS, Solid State Disk, serial and parallel I/O ports, keyboard and speaker interfaces, and a real-time clock.

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You'll get your product to market faster, with less risk, and at lower cost, because the CoreModule family is based on the most economical industry standard architecture. Now you can focus on the more challenging part of your system—the application itself.

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National Semiconductor

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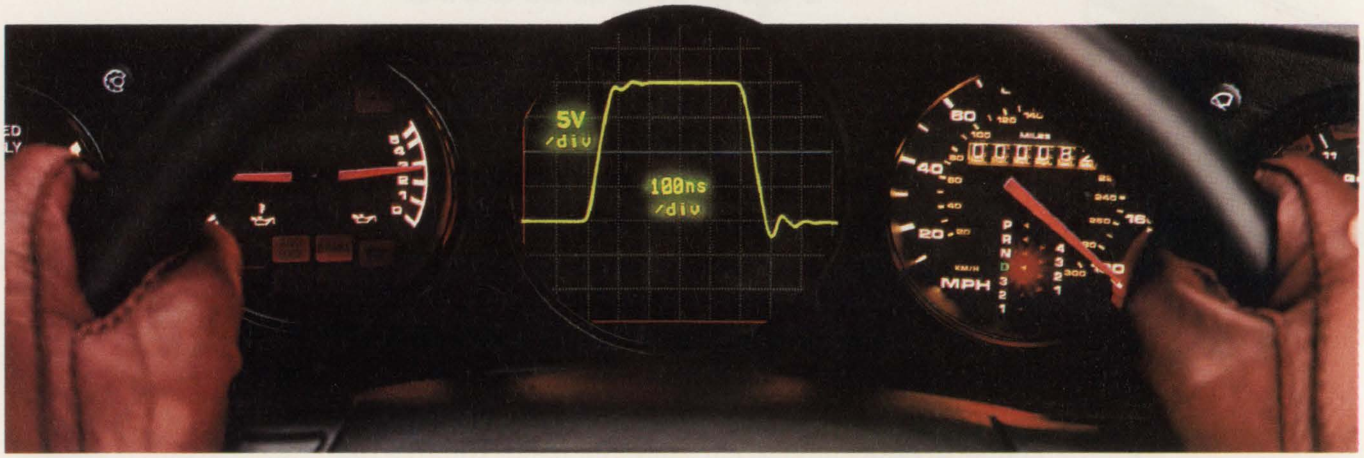
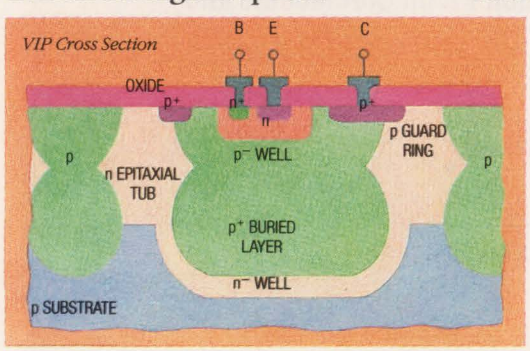


Driving a 1,000pF C_L and slewing at 250V/μs, the LM6313 delivers 250mA into the load and still remains stable.

Turbocharging your load-driving capabilities.

Our new VIP op amps are built to drive... and at very high speeds. Which makes a great deal of high-performance sense when you consider they're designed with an innovative bipolar technology called "Vertically Integrated PNP" or VIP.

With a ±15V power supply, our VIP op amps offer a higher signal-to-noise ratio, a higher dynamic range, *and* higher drive capability (none of which you can get from other high-speed ±5V amps). In fact, they'll drive capacitive loads without oscillating. Which means they're easy-to-use and very stable. Even at the highest speeds.



Packing precision and speed in the same op amp.

The LM6218, a dual op amp, is not only extremely precise, it's extremely fast. Which is why it provides a low offset voltage of 3mV (1mV max for the LM6218A), a bandwidth of 17MHz, and a slew rate of 140V/μs.

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Delivering the world's first high-speed, high-power monolithic op amp.

Until recently, you needed multi-chip solutions to match the world-class performance now achieved by our one-chip solution, the LM6313.

This monolithic device delivers 35MHz performance and a 250V/μs slew rate. Plus, it'll drive a 75Ω cable to a ±11V output swing—with a peak output current of 300mA and 220mA continuous—making it ideal for ATE and pin-driver applications.

What's more, the LM6313 provides on-chip protection. Like overcurrent and thermal shutdown protection with early-warning error flags.

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For your design package, call or write us today. And let our high-speed VIP op amps put your designs into overdrive.

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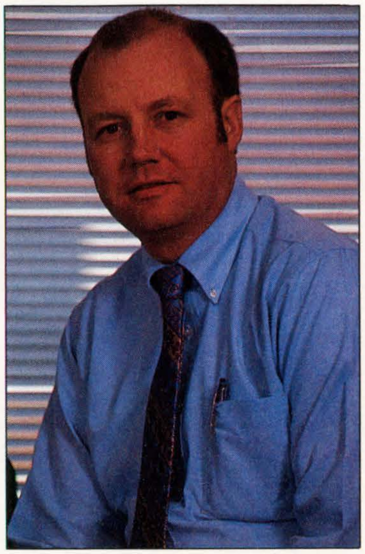
Teach children to think about math



I am amazed at the way we introduce our children to the wonders of higher mathematics. Instead of teaching them how to think about solving problems, we dull their interest with drill sheets of unchallenging problems. It seems that many teachers learned by-the-book methods and that is how they teach. Some of those techniques baffle me. My 13-year-old daughter had a difficult time with percentages in math class. The tough part for her was deciding which way to move a decimal point. I explained that a percentage is just a fraction that always has 100 in the denominator. Once you know that, you can keep track of what you're doing without guessing. Instead, her teacher moved decimal points *without discussing the techniques* involved in setting up the problems.

In my 16-year-old son's math class they studied logarithms. I was dismayed to see that they were writing down logs in an archaic way—3.6789-7, for example. Surely there are better ways to introduce children to the subject of logs. Unfortunately, the children cannot use calculators to find logs and antilogs. Neither can they use them to interpolate between log-table values. My son found it difficult to understand the interpolation method taught in school. I explained it to him by graphing a straight line between two points, which clarifies what interpolation is all about. He said they never showed him that in school.

I'm surprised by the prohibition of calculators. Some teachers and parents think that calculators encourage laziness and undermine basic math skills. Nothing could be further from the truth. Poor teaching techniques and long columns of dull exercises undermine anyone's interest in math. If school systems and teachers would concentrate on the basic skills of thinking about math, explaining how to approach problems, and applying these skills in different ways to solve realistic problems, the controversy about calculators would subside. Educators would find that many children really can enjoy math.

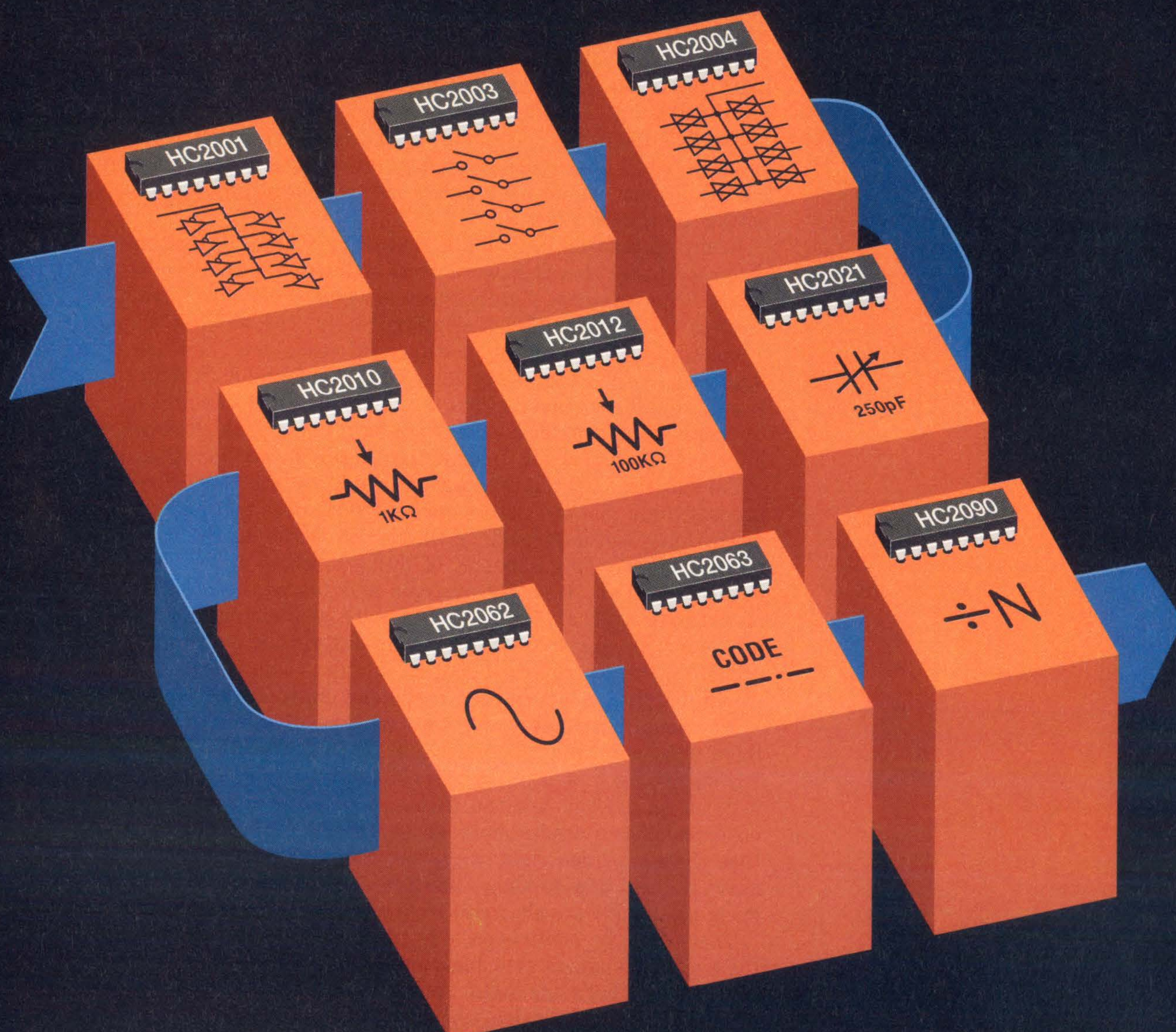
We should challenge youngsters with realistic problems that show them what percentages, logarithms, and interpolations are all about. It's surprising how a class' interest blossoms when you explain logs in terms of decibels and the Richter scale. We must also concentrate on explaining alternate methods of solving problems and explaining that there's no one right way, but many wrong ways, to arrive at answers—and how to know the difference. By using calculators, children can quickly try alternate routes to solving problems.

There may be some hope. I'm pleased to read that people taking the College Board math achievement test in June will be able to use calculators. That's the right approach—let the students concentrate on evaluating and setting up problems. The calculators can do the routine computations. I hope we'll see more and more calculators, computers, and other tools push their way into classrooms. I hear other parents say, "Calculators just let children get sloppy and avoid the hard math. They need more drill and work sheets on the basics." Maybe they're right. Perhaps modern tools have no place in school. But what if your daughter says she is having trouble in wood shop because it's difficult to drive a nail straight when banging it with a rock? Isn't it time for a hammer?

Jon Titus
Editor

Send me your comments via FAX at (617) 558-4470, or on the EDN Bulletin Board System at (617) 558-4241 300/1200/2400, 8, N, 1.

Jesse H Neal
Editorial Achievement Awards
1987, 1981 (2), 1978 (2), 1977, 1976, 1975
American Society of Business Press Editors Award
1988, 1983, 1981



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SERIALLY PROGRAMMABLE
DEVICES

NSP

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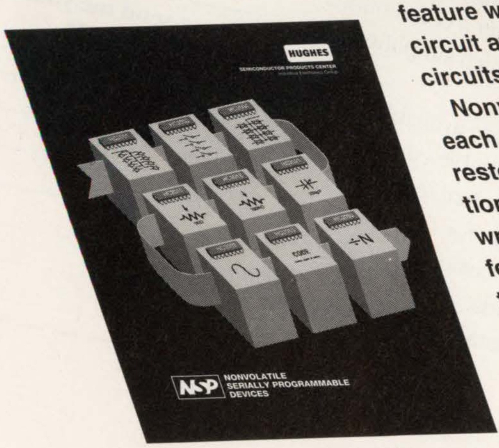
Here are nine players that can work together in any order. Won't forget their plays. And can take new instructions anytime from homeplate.

From the Semiconductor Products Center of Hughes Aircraft Company comes another major development in semiconductor integrated circuits.

Hughes' new NSP family of Nonvolatile Serially Programmable devices gives circuit designers new freedom and flexibility in their work....saving time, money and labor while improving overall system performance and reliability.

With these nine general purpose devices, PC boards or hybrids can be trimmed or configured electronically. Instead of using a slow, laborious, and often difficult mechanical trimming procedure, it's all done remotely through a personal computer or test station.

That's because these NSP components have a serial interface feature which permits accessing the nonvolatile memory of the circuit at the system level, also enabling many configurable circuits to be cascaded.



Nonvolatile data latches retain the last programmed state in each device when power is removed, then automatically restore the correct state when power is resumed. In addition, a standard serial interface provides both read and write access to the nonvolatile memory. All NSP devices feature low power consumption and redundant circuit techniques to assure reliable operation and long life.

For a complete information packet, contact Hughes Semiconductor Products Center, PO Box H, Newport Beach, CA 92658; or call (714) 759-2665 or FAX (714) 759-2913.

CIRCLE NO. 64

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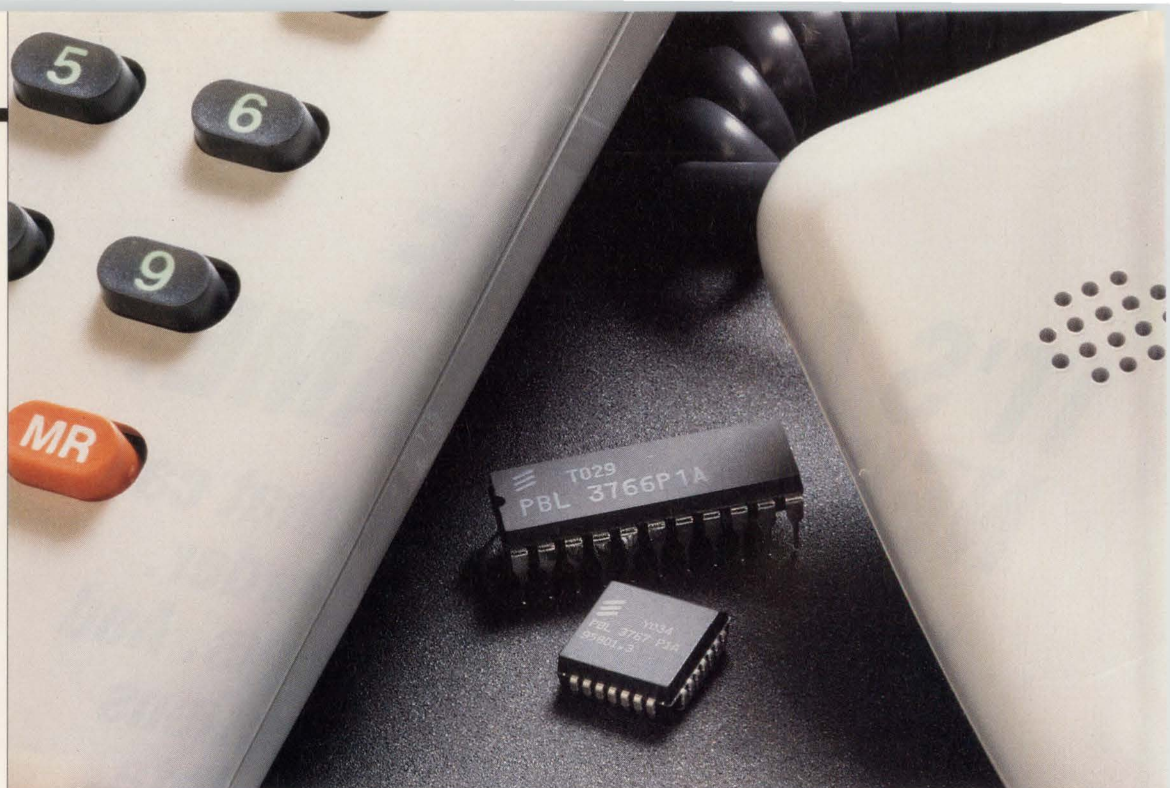


New SLICs cut the cost of on-premises/PBX subscriber lines

Lower cost chips that need fewer external components are the latest Subscriber Line Interface Circuit offerings from Ericsson.

Designed for cost sensitive applications such as general purpose PBX/Key systems, they give you three other major advantages over alternative solutions: wide supply voltage operation from -24 V to -58 V dc, on-hook transmission and a very low on-hook power dissipation of just 35 mW with -48 V dc supply or 20 mW when running from a -24 V dc supply.

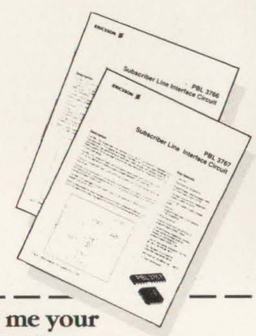
So you can reduce the cost of your power supply circuit too!

Each SLIC includes loop current and ring trip detection, together with a ring relay driver. And they work with either a conventional or programmable CODEC/filter, all of which simplifies design.

Equally important, the new circuits are available in two versions: the PBL 3766 with a programmable constant loop current, and the PBL 3767 with programmable resistive battery feed and loop current limitation for short lines.

Both come in a choice of 22-pin plastic DIP or 28-pin PLCC packages with compliant 'j' leads.

Simply call us for full technical data or clip the coupon.



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ERICSSON

SENSITIVE SCOPE MEASUREMENTS

Scopes pluck waveforms from the signal swamps

Oscilloscopes do far more than simply display a signal level versus time. Now they can dig through noise and sift out interference to make sensitive measurements accurately.

Charles H Small,
Senior Editor

In the past, engineers performed many of their most sensitive measurements with instruments other than oscilloscopes. Sensitive measurements were the domain of band-limited, special-purpose instruments such as distortion meters, spectrum analyzers, phase meters, and network analyzers. But now you can make many of these sensitive measurements with your oscilloscope, backing up a digital oscilloscope with digital signal processing.

A word of caution: As Jim Williams, at Linear Technology, says, "High-performance circuits can work only if you negotiate compromises with nature. Ignorance of, or contempt for, physical law is a direct route to frustration." Physically, your probe and scope become part of your system under test when you hook the scope to your circuit.

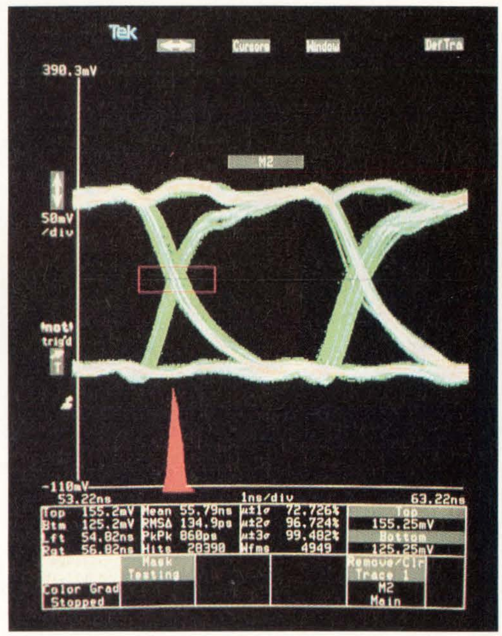
Scope and probe concerns

What do you need to know about your scope and probes? For starters, become very familiar with your particular scope's input impedance, rise times, ac coupling, probe compensation, noise performance, overdrive recovery, sweep nonlinearity, triggering, and channel-to-channel feedthrough.

Without knowing your scope's limitations, you can easily fall prey to the most common mistake in oscillography. You may unwittingly measure the performance of your scope instead of the performance of your circuit.

The GIGO (garbage-in/garbage-out) principle applies to oscillography with a vengeance. Informally surveying high-performance analog-IC makers and oscilloscope vendors reveals that most problems designers have with their high-performance circuits are actually probing problems. In short, to take advantage of modern scopes' processing power, you must first comprehend the mysteries of probing.

You have many different kinds of probes to choose from. Each type has



You can characterize complex signals using digital post processing *such as that offered by Tektronix Tek CDA 803.*

its own proper sphere of application. FET probes, for example, have high input resistance and low input capacitance. But they also have substantially more delay than passive probes. FET probes' common-mode-range limitations can lead to erroneous displays if you accidentally exceed them. Not all FET probes have extremely high input resis-

tance—some types are as low as 100 kΩ.

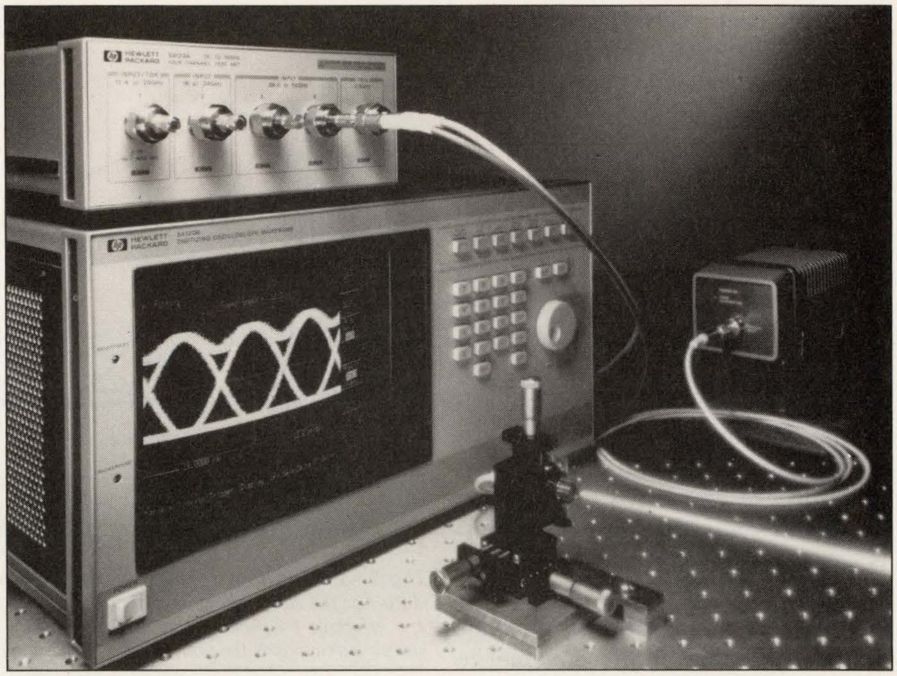
Current probes come in two types. The passive, transformer types are fast and have less delay than the Hall-effect versions. The Hall types, however, respond at dc and low frequencies; the transformer types typically roll off below a certain frequency limit, usually 100 Hz to 1 kHz. You can easily saturate both types of current probes, resulting in misleading displays.

Study each type of probe that you use. Different probes have different impedances and delay times. You must account for these impedances so you can hook the probes to your circuit without inducing spurious responses. Your probes' differing delays influence how you interpret your scope's displays.

A probe's resistive loading can cause amplitude distortion and alter the dc bias of your circuit. Capacitive loading can cause timing changes by introducing an RC time constant or by slew-rate limiting. Capacitive loading also causes nasty bandwidth-limiting effects. Under certain conditions, the probes parasitic effects can even cause an otherwise stable circuit to resonate.

Probing's greatest source of error is grounding. The parasitic inductance in a probe's ground connection can cause ripples and discontinuities in a displayed waveform. Probes' ground wires have about 25 nH/in. of inductance. In some cases the grounding at one channel will affect waveforms on another channel. In the worst case, connecting the probe's ground wire will shut your circuit down.

Common-mode noise wreaks havoc with sensitive measurements. Luckily, you have several ways to attack this noise. Which scheme you use to measure signals in the presence of high common-mode interference depends on frequency. Use differential plug-ins for low-speed, differential probes at frequencies as high as 200 MHz, and the familiar A − B scope setting (with your A and B probes carefully zeroed out) for higher-frequency signals such as differential ECL signals. Digital scopes make probe zeroing a snap because they let you take care of differing probe delays by shifting memory points in software rather than trying to make up for phase differences in hardware.



The segmented memories in digital oscilloscopes, *such as the Hewlett-Packard HP 54124A, can capture bursts of signals.*

Now consider your oscilloscope

Proceeding down the signal chain from probe to scope, consider a scope with a differential-amplifier front end or plug-in. Most engineers think of differential amplifiers as measuring signals not referred to ground, such as across a current shunt. However, differential amplifiers provide two not-so-obvious advantages in noisy environments as well.

At low signal levels, the ground potential at the signal source is often not exactly equal to the ground potential at your scope. Ground loops and high ground-return currents conspire to make your signal ground very noisy compared with low-level signals. Many ground-loop problems would disappear if scopes were double insulated. But industry standards require everything to be grounded—both systems under test and scopes.

To verify how noisy a ground can be, try putting a scope probe on your circuit's "ground" sometime. You will almost always see substantial noise and perhaps a small dc offset. The scope probe faithfully picks up and reproduces this noise. But a differential measurement cancels out the grounding differences, restoring true fidelity.

A second and related benefit of the differential amplifier is RF/EMI reduction. As is obvious, any electromagnetic flux cutting across a scope probe's cable induces a small voltage across the cable's shield.

Sensitive scope measurements

Thus the scope sees the actual signal plus the noise voltage induced on its ground shield **(Fig 1a)**. A differential amplifier cancels the spurious signal, passing only the differential signal **(Fig 1b)**. This effect explains why telephone, audio, and data communications use balanced line transmission.

Assuming you are adept enough at oscillography to capture an accurate representation of a signal, digital postprocessing of that signal can transform your general-purpose oscilloscope into a band-limited, special-purpose, sensitive instrument. Whether you do your postprocessing with your scope's built-in routines (if any) or export the raw data files to a computer for analysis is mostly a matter of convenience and throughput. In both cases, the postprocessing principles are the same. For example, the Nicolet Series 400 oscilloscope has a built-in version of Basic that can call the scope's routines. You can use this interpreter to compose and execute a suite of signal-processing routines.

Capture multiple records

In some cases, the throughput—from capture, to dumping the captured data into off-line memory, to re-arming the scope—is especially important. In pulsed-laser and data-communication applications, for example, the device under test often produces a short burst of data followed by a relatively long interval of dead time. In most cases, you are interested in only the pulsed data, not the dead time between pulses. In these cases, the digital scope must have very fast throughput or a segmented memory.

With a segmented memory, such as that in the Hewlett-Packard HP 54510A, the digital scope can capture several high-speed bursts before exhausting its high-speed memory. Thus you can capture several records without pausing to dump your captured data to off-line memory.

After capturing a record, or records, digital scopes can further manipulate the captured data with post-capture processing. Digital scopes, such as LeCroy's 9400 series, commonly perform postprocessing such as averaging, filtering, phase shifting, rise- and fall-time derivation, and FFTs **(Fig 2)**.

A feature unique to digital scopes is their ability to digitally filter al-

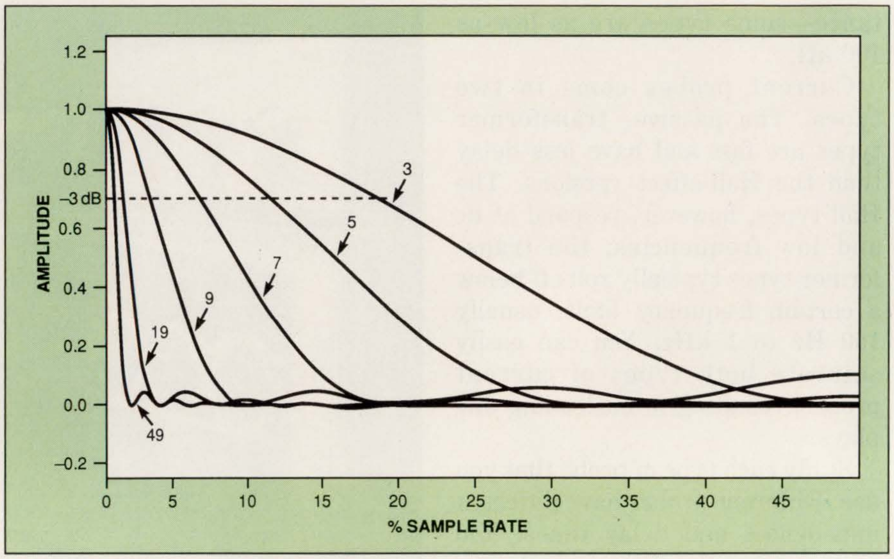


Fig 2—Performing a "sliding average," or "smoothing function," *on a set of digitized data has the same effect as a lowpass filter: removing high-frequency noise. This graph shows the effective frequency response of various numbers of points in the sliding average. The graph normalizes frequency as a percentage of the digital scope's sample rate.*

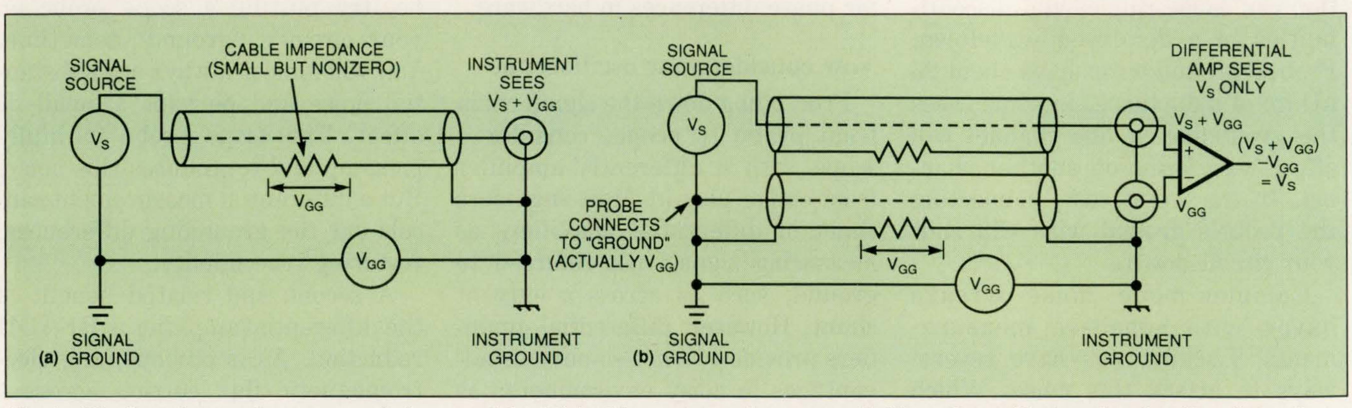


Fig 1—The impedance of a scope probe's ground lead (a) *adds a minute, but not negligible, voltage (V_{GG}) to the signal's voltage that a single-ended scope sees. In* ***b****, a scope having a differential probe or differential front-end cancels out the ground lead's spurious voltage.*

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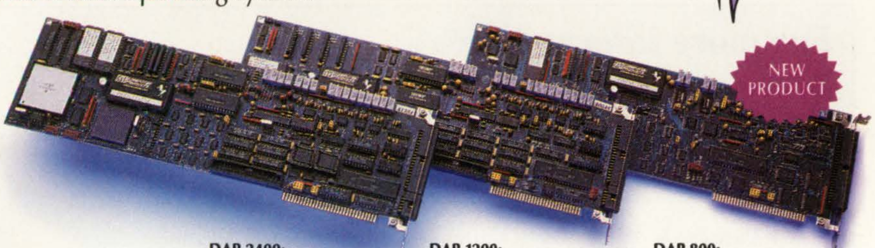

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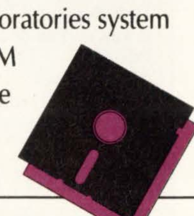

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ready-acquired waveforms, including one-shot transients. By properly selecting the cutoff frequency, you can reduce noise without distorting the desired signal. Filtering also improves the resolution of the digitized signal in proportion to the reduction in bandwidth. Unlike working with an analog scope's inflexible, fixed front-end filtering, trying several different digital filters on a captured signal to determine which gives the best results is quite simple. In effect, you can adjust bandwidth after capturing the signal.

Leave your eyeballs out of it

Digital scopes can also perform statistical analyses on sets of captured data. Such analyses provide more accurate and reproducible characterizations of random processes than eyeballed analyses of analog-scope displays.

For example, postprocessing allows you to measure jitter, a random process that often exhibits a normal distribution. Jitter has the same effect on a signal as does a lowpass filter, obscuring potentially valuable high-frequency information. With analog scopes, you can only look at jitter, not measure it. With a standard analog oscilloscope, you see jitter as an illuminated band, the brightest section corresponding to the location where the jittery edge occurs most often. A blot of lower intensities shows where the edge occurs less frequently.

With an analog oscilloscope, you typically would increase your CRT intensity until just before blooming occurs and record the limits of jitter as a peak-to-peak jitter measurement. This jitter measurement depends on how each engineer sets a scope's intensity. Consequently, such jitter measurements are not reproducible. And the intensity may not be enough to illuminate the actual extremes of the jitter's range, yielding something less than the true peak-to-peak jitter.

Furthermore, you need to separate the scope's trigger jitter and time-base jitter from the signal's jitter. Digital postprocessing allows correcting for the scope's jitter contribution.

For example, the Tektronix DSA 600 series scopes remove jitter by sliding records backwards and forwards in time trying to make them fit over one another. The company's CSA 803 digitizing signal analyzer offers a false-color display. This display mode is analogous to a monochrome, Z-axis variable-intensity display, but shows different colors corresponding to the density of overlapped traces at each point in the display.

Now with certain digital scopes you can measure and characterize jitter. These digital scopes display a histogram of the jitter's time distribution. From the histogram you can see if you have a normal distribution—which is ordinary noise—or if there are some peaks indicating other sources for the jitter. Using these scopes, you can get figures for your jitter and noise margins that you couldn't get before.

Digital scopes also excel over their analog siblings in triggering capability. Enhanced triggering makes capturing the one waveform you want out of a stream of similar waveforms easier. In addition to triggering on the occurrence of a signal, digital scopes can trigger on the non-occurrence of a signal, a "dropout." Modern scopes, such as the Philips/Fluke PM 3340 digital oscilloscope, now have "envelope" functions that allow you to see only out-of-bounds excursions.

Digital oscilloscopes offer an amazing array of sophisticated features, yet still rely on compara-

For more information . . .

For more information on the oscilloscopes and probes discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Sensitive scope measurements

tively primitive probes to acquire their information. However, you can learn how to utilize these features and compensate for probe shortfalls. Instrument and IC vendors have a wealth of free applications information to help you master oscillography. The **references** section following this article provides a list of some of the material available. EDN

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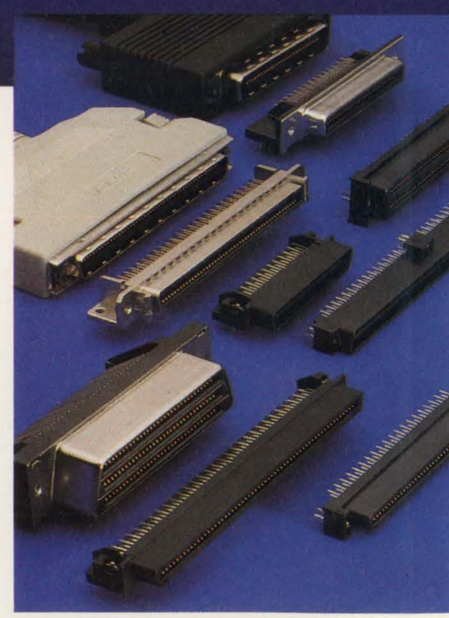

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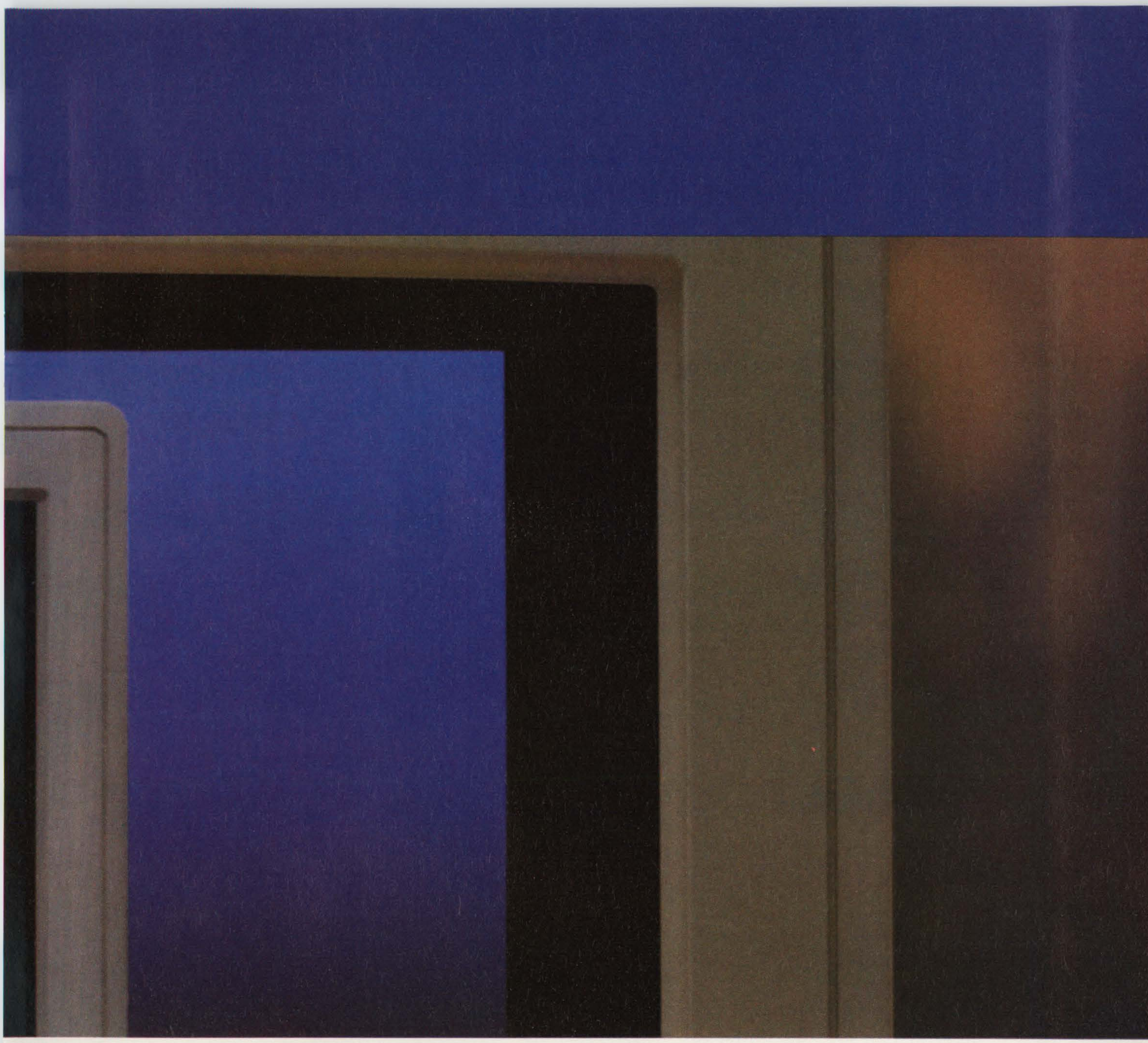

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KM28C17	2Kx8	Parallel	150	*Data polling, ready/busy*
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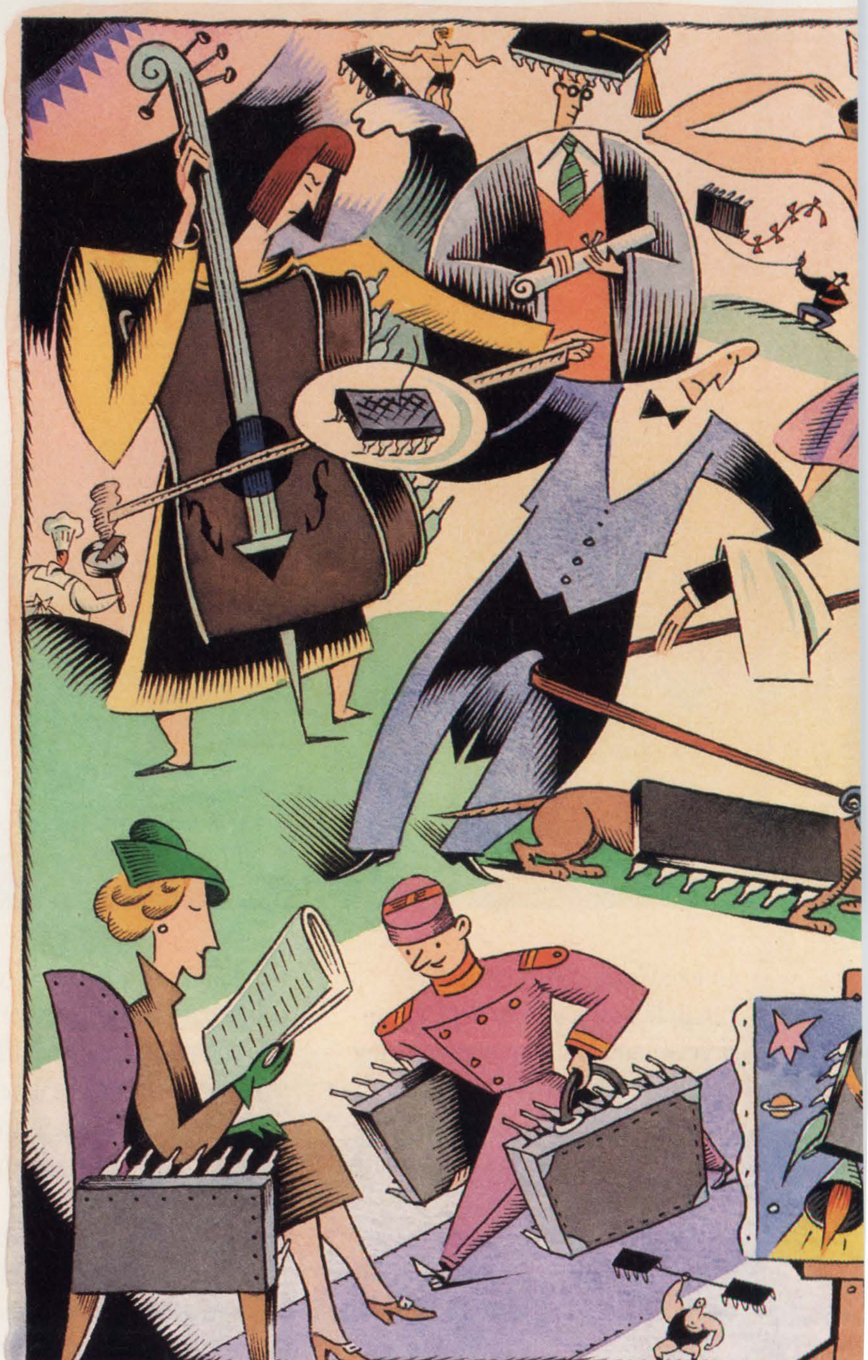

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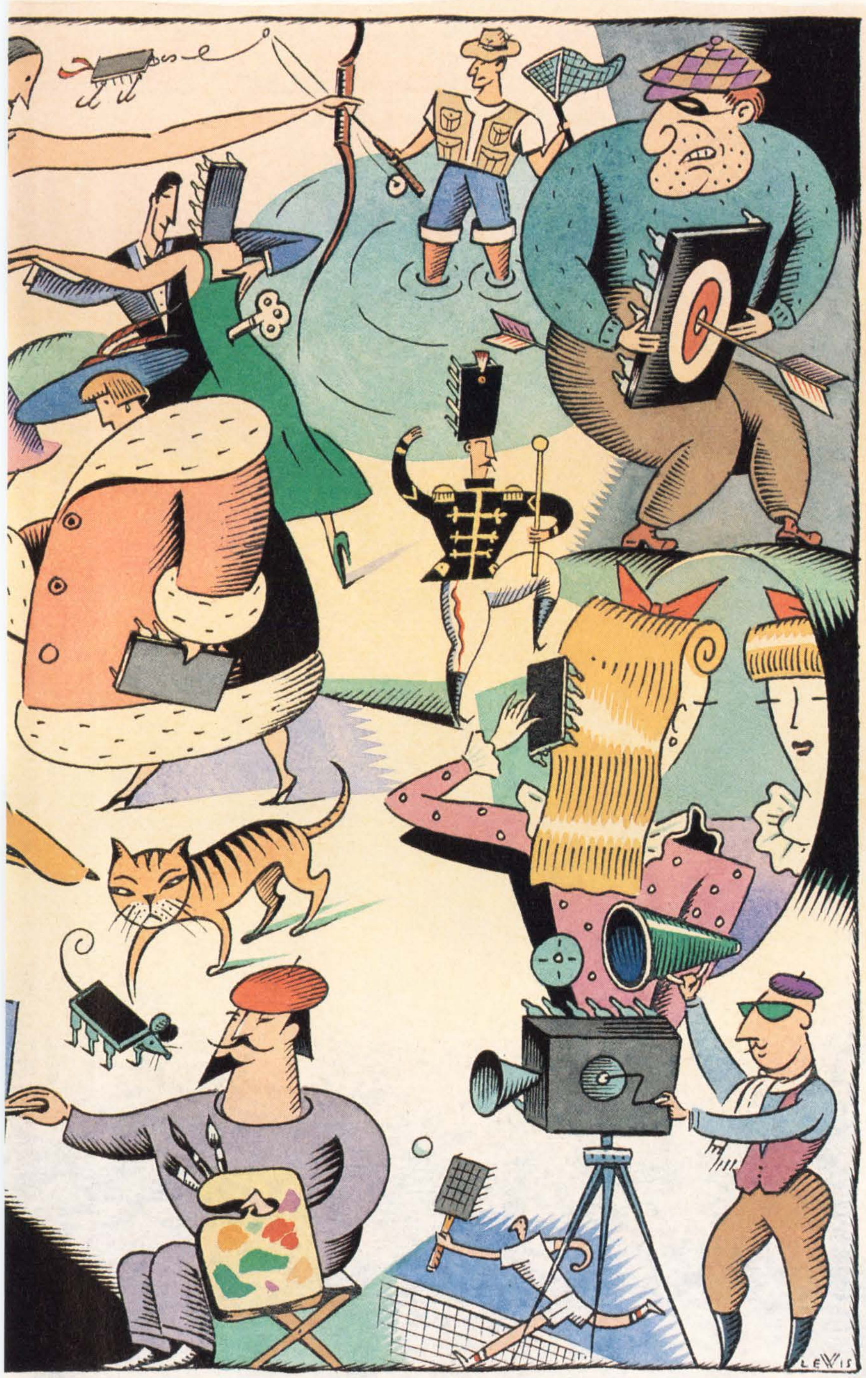

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FIBER-OPTIC PRESENCE SENSORS

Devices survive harsh environments

Because fiber-optic sensors are mainly passive devices, they are more reliable than traditional mechanical or electronic sensing devices—especially in the hostile world of industrial electronics.

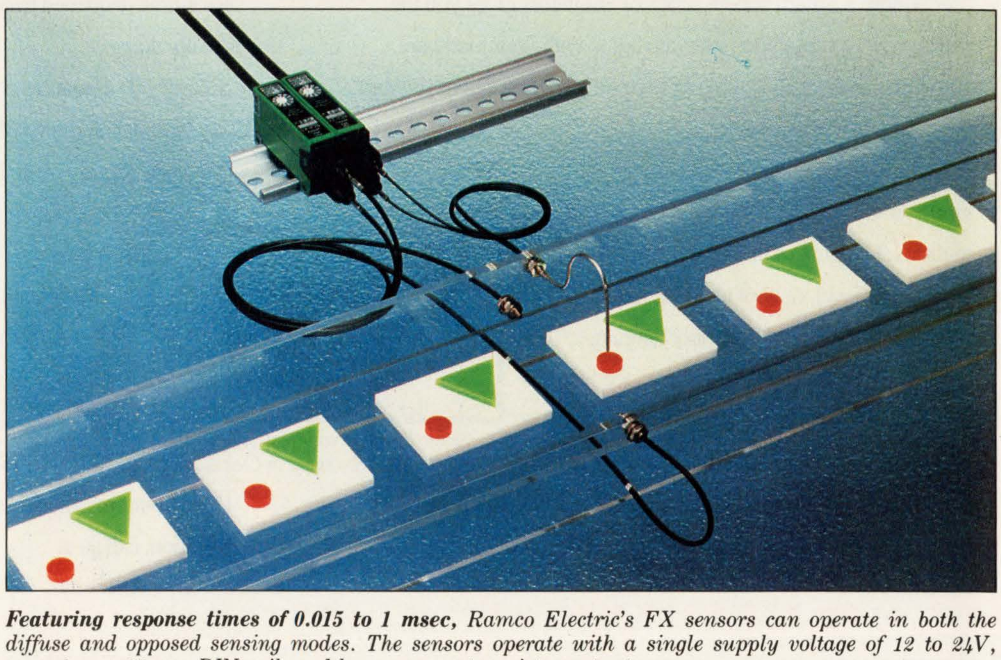
Tom Ormond, *Senior Editor*

Fiber-optic presence and color sensors have sensor tips as narrow as a human hair and can withstand hostile environments including extreme shock and vibration, moisture, heat, and chemicals. They have no moving parts, which can wear out, and so are more reliable and more flexible than traditional copper-wire sensors. In addition, fiber-optic sensors can function in all standard photoelectric sensing configurations (see **box,** "A primer on fiber-optic sensing modes").

Optical fibers have bandwidths in the megahertz range. As a result, you can multiplex many sensing elements onto a single fiber to form a sensor network distributed in space. This capability lets you use a single fiber to simultaneously measure several hundred points. To match the information-carrying capacity of a single fiber, a cable with copper wire would have to be more than 200 times as thick.

Signal attenuation over distance is much lower in an optical fiber than it is in a copper wire. Lower attenuation increases the distortion-free transmission distance for an optical-based sensing system. Optical fiber is a dielectric, so it is not susceptible to electromagnetic waves. Fibers do not transmit electrical signals, so you don't have to worry about sparking.

Glass fibers can handle temperature extremes ranging from subzero to several hundred degrees Celsius with no problem. Glass fibers also resist attack from corrosive or toxic atmospheres that



Featuring response times of 0.015 to 1 msec, *Ramco Electric's FX sensors can operate in both the diffuse and opposed sensing modes. The sensors operate with a single supply voltage of 12 to 24V, mount on a 35-mm DIN rail, and have an npn transistor output.*

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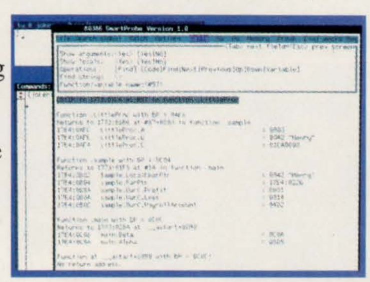

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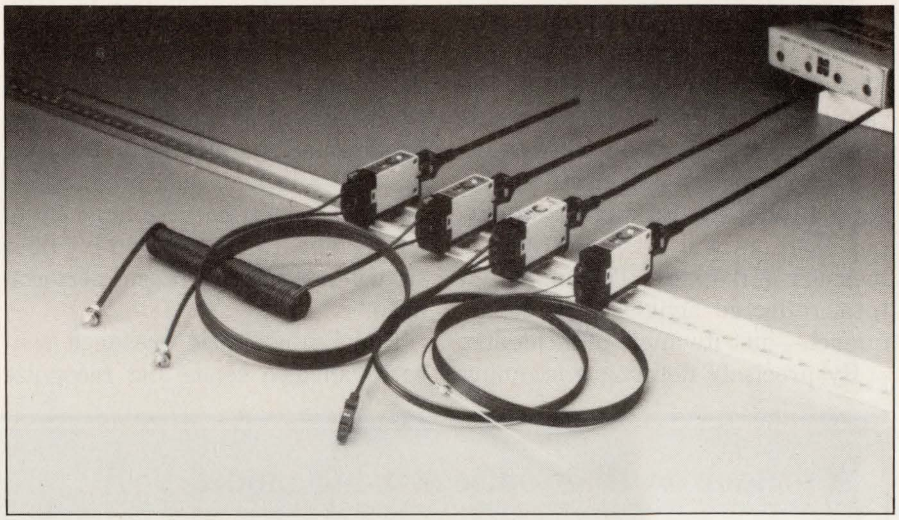
would devastate metals. (Plastic fibers would have the same problems as metals in the aforementioned environments.) Fiber-optic sensors can interface with remotely located control electronics via a fiber-optic data link.

The numbers tell the story

Table 1 lists parameters for a sampling of fiber-optic presence sensors. The slowest sensor response time is 10 msec. Aromat's MQ-F sensors can detect targets as small as 0.0020 in. All the units in the **table** function with plastic fiber, which is less expensive than glass fiber and easier to terminate. In fact, Aromat supplies a plastic-fiber cutter with each of its MQ-F sensors.

Fiber-optic sensors operate from a single supply voltage and produce dc outputs that can interface directly with logic circuitry, relays, or programmable controllers. The sensors from Aromat, Omron, and Opcon can function in light- or dark-detection modes, so they can serve as either presence or absence sensors. Omron offers separate presence and absence sensors; Aromat and Opcon sensors have an integral switch that lets users configure a single sensor for either presence or absence detection.



A speed of 1000 operations/sec *suits Aromat's MQ-F sensors for high-speed, small-piece part-detection applications. The sensors can detect objects as small as 0.002-in. wide and can mount in a panel or on a DIN rail.*

Industrial environments can be rough on optical sensors whose operation is based on light intensity. A change in target color or reflectivity, a dirty lens, or movement in the target background can degrade sensor performance. To circumvent such problems, Aromat employs triple-beam technology in its MQ-F fiber-optic sensors to accurately define a scanning-distance window.

The sensor employs three fibers. One fiber operates as a transmitter; the other two function as receivers. The transmit fiber sends the LED's beam to the prospective target. The two receiver fibers capture the light reflecting back from the target to the sensor. The fibers guide the reflected light to two PIN photodiodes. These diodes generate a current that is a function of the received light. The MQ-F sensors use the diode output current ratio to determine the target's distance.

The receiver optical system comprises an aspherical lens and the two fibers. The system reacts to the angle of the incoming light rather than the intensity of the light. The angle at which the reflected light exits the receiver fibers varies as a function of target distance. Thus, the light will be hitting each of the

Table 1—Representative fiber-optic sensors

Manufacturer	Model	Detection modes	Detection range (cm)	Fiber type	Response time (msec)	Minimum target size	Operating range (°C)	Price
Aromat Corp	MQ-F	Diffuse, reflective	1.5 to 12.0	Plastic	0.5	0.002 in.	−40 to +70	$75 (100)
Omron Electronics Inc	EE-SPZ	Retroreflective	0.8*	Plastic	10.0	0.59×0.59 in.	−10 to +55	$46
Opcon Inc	Comet 100	Proximity	0.76	Plastic	2 to 8	0.020 in.	−40 to +70	$80 to $110
		Opposed	2.95					
Ramco Electric Co	FX	Diffuse	5	Plastic, glass	0.015	15μm	−40 to +70 (plastic)	$30 to $394
		Opposed	350				−20 to +300 (glass)	

* Nominal value for a 60-cm length of fiber.

PIN diodes at a different spot, causing the diode output to vary. For example, for a distant target, the first diode will receive most of the reflected light; when the target is close, the second diode will receive the major portion of reflected light. As a result, the ratio of diode output currents will vary strictly as a measure of distance. The amount of total reflected light is of no consequence—just its angle of incidence.

By precisely defining a scanning window, triple-beam technology takes away all target-color, reflectivity, and shape considerations. And because MQ-F sensors let you predetermine the sensing window, background movements and objects have no effect on measurement accuracy. In fact, because light intensity is immaterial, even a dirty fiber tip will not degrade sensor performance.

Some fiber-optic presence sensors can also sense and recognize color. These devices suit such applications as label differentiation and sorting color-coded parts, bottles, cans, or foods and can be a cost-effective alternative to an off-line color lab. CRS 300/301 Series sensors ($8000) from Micro Switch can be programmed to recognize as many as eight colors and use the 400- to 800-nm visible light spectrum to characterize colors.

CRS sensors use a halogen light source to illuminate the target. This

A primer on fiber-optic sensing modes

Photoelectric sensors operate in one of three modes—opposed, retroreflective, or proximity. The proximity mode includes several submodes: diffuse, divergent-beam, convergent-beam, and background suppression.

Opposed-mode, or through-beam, sensors have the emitter and receiver opposite each other. The emitter aims its optical beam directly at the receiver. The sensor detects an object when the object interrupts the beam between the two components.

In retroreflective sensors, the emitter and receiver are adjacent to each other. The emitter sends out a light beam at a reflector, and the receiver detects the reflected light. Retroreflective sensors detect an object when the object interrupts the light beam.

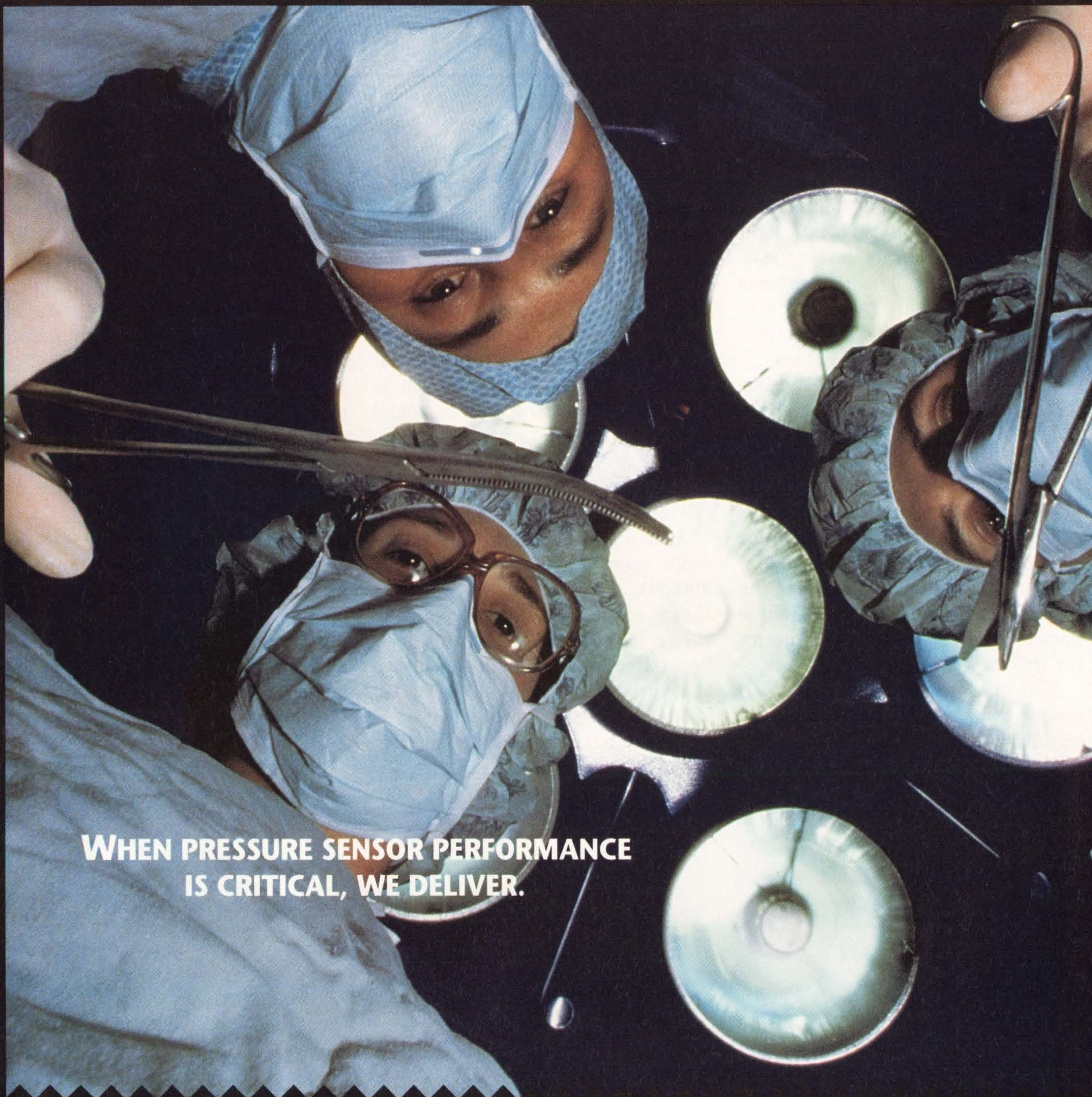
A proximity sensor detects objects by sensing the amount of its own transmitted energy that reflects back from the surface of the target object. Both the emitter and receiver are on the same side of the target object and are usually located in a single housing. An object, when present, establishes the beam.

Diffuse-mode sensors are probably the most popular type of proximity sensor. In these sensors, the light from the emitter strikes the target surface at an arbitrary angle and diffuses off the surface at many angles. This operating mode is not very efficient because the receiver looks for only a small amount of the light reflecting back from the target. Also, diffuse-mode sensors (as well as all other types of proximity sensors) are heavily influenced by the reflectivity of the target's surface. A diffuse-mode proximity sensor will have a greater sensing range for a target with a bright white surface than it will have for a target with a dull black surface.

Short-range unlensed divergent-beam proximity sensors suit applications in which you have to avoid the effects of signal loss from shiny objects. The lack of a lens shortens the usable sensing range, but these sensors are much less dependent than diffuse-mode sensors on the incident angle at which their light beam strikes the target that is within range. Target size also influences the performance of divergent-beam sensors—more energy will return from large targets. However, divergent-beam sensors respond better than diffuse-mode sensors to objects that are very close to the sensing tip.

Convergent-beam proximity sensors use a lens system that focuses the emitted light at an exact point in front of the sensor. These units focus the receiver element at the same point. This design establishes an intense, well-defined sensing area at a fixed distance from the sensor lens. The technique is quite efficient. Convergent-beam sensors can readily sense small targets. They can also sense materials that have reflectivity levels too low to be detected by diffuse-mode or divergent-beam sensors.

The background-suppression sensor rounds out the list of proximity sensor types. These devices simply ignore objects that lie beyond their sensing range. The background-suppression sensor compares the amount of reflected light that each of its two optoelements receives. These sensors recognize a target if the light level reaching the base receiver equals or exceeds the light level reaching the other receiver. The sensor does not develop an output when the light arriving at the second receiver exceeds the light level reaching the base receiver.


WHEN PRESSURE SENSOR PERFORMANCE
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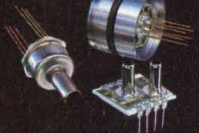

source light travels over the emitter portion of the fiber-optic cable and provides a uniform white light that permits accurate and repeatable color sensing. The light reflects off the target and travels back to the sensor through the receiver portion of the fiber-optic cable.

The light returning from the target then reflects off an internal diffraction grating. The grating breaks the light into a color spectrum, which shines onto an array of 128 photodiodes. These diodes sense the intensity of the light for the different colors in the spectrum. The array, in essence, converts the light-intensity pattern into a unique data set that represents a signature for the target color.

The microprocessor in the CRS sensor compares the incoming color signature data to signatures it has stored in memory. When it detects a match, the processor turns on the appropriate output. The standard CRS unit has a 0.1- to 2-in. sensing distance range. It has eight digital outputs, one for each of its color channels. These outputs can be either current sinking or current sourcing and can drive as much as 600 mA. You can use onboard switches or menu-driven software to configure the outputs. The sensor can also transfer data over its RS-232C or RS-485 serial ports.

A 10.5 to 30V, 47W supply provides operating power for the CRS 300/301. Reverse-polarity protection is standard, and the operating range is 0 to 40°C. The sensor is housed in an aluminum enclosure that provides NEMA 1, 3, 4, 12, 13, IP65, and IP67 protection.

In addition to accurately monitoring the performance of an industrial processing system, fiber-optic sensors can simplify the task of actually controlling the flow of a process. Photoelectric sensors with analog outputs are especially useful in process-control and similar applications in which monitoring an object's relative position or size is necessary to produce a continuously variable voltage output. You can also use analog-output sensors to monitor the optical reflectivity or optical clarity of materials.

Banner Engineering's Omni-Beam sensors ($187 to $300) are an example of analog-output fiber-optic sensors. By properly designing the sensing-end tip of the plastic or glass fiber, you can maximize the analog response. You can monitor the linear or angular displacement between two surfaces by operating the sensors in the opposed mode. You can also use this mode to measure the width of an object as a percentage of the beam blocked by the object. Opposed-mode sensors can look through a transparent or translucent material to monitor optical clarity. You can monitor the reflective characteristics of a material by using the vendor's bifurcated fiber assemblies. Custom-designed fiber assemblies can yield distance measurements as precise as a thousandth of an inch.

The sensors provide a variable dc voltage output that is directly related (noninverting output) or inversely related (inverting output) to the strength of the light signal the sensor receives. When you properly adjust the sensor, the two analog outputs are mirror images of each other and the output-voltage

For more information . . .

For more information on the fiber-optic sensors discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Everett, WA 98203
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waveforms intersect at 5V. Each sensor has multiturn null and span controls that set the minimum and maximum limits of the sensor's sourcing-voltage outputs. Proprietary circuitry lets you make null and span adjustments without encountering interaction problems. A 10-element moving-dot LED array provides a visual indication of the relative light-signal change and power-block voltage output to within the nearest volt.

Omni-Beam sensors consist of two basic building blocks: a sensor head and a power block. The sensor heads contain optical components, an analog amplifier, the null and span adjustment controls, and LED-indicator-array circuitry. The fiber-optic sensor heads are available in versions for both diffuse and opposed sensing applications. Sensor-head types include infrared- and visible-light glass-fiber models as well as a visible-light, plastic-fiber model. The power block contains power-supply and analog-voltage-output circuitry. These blocks are available in three models: OBPT3 for 15 to 30V dc, OPBA3 for 105 to 130V ac, and OBBB3 for 210 to 250V ac.

As factory and process-automation requirements become more demanding, the need for reliable sensors will increase. Fiber-optic sensors will be able to satisfy these sensing needs. They can handle a large amount of data, transmit data over longer distances than traditional copper-wire sensors, overcome EMI/RFI problems, and handle the harshest industrial environments. EDN

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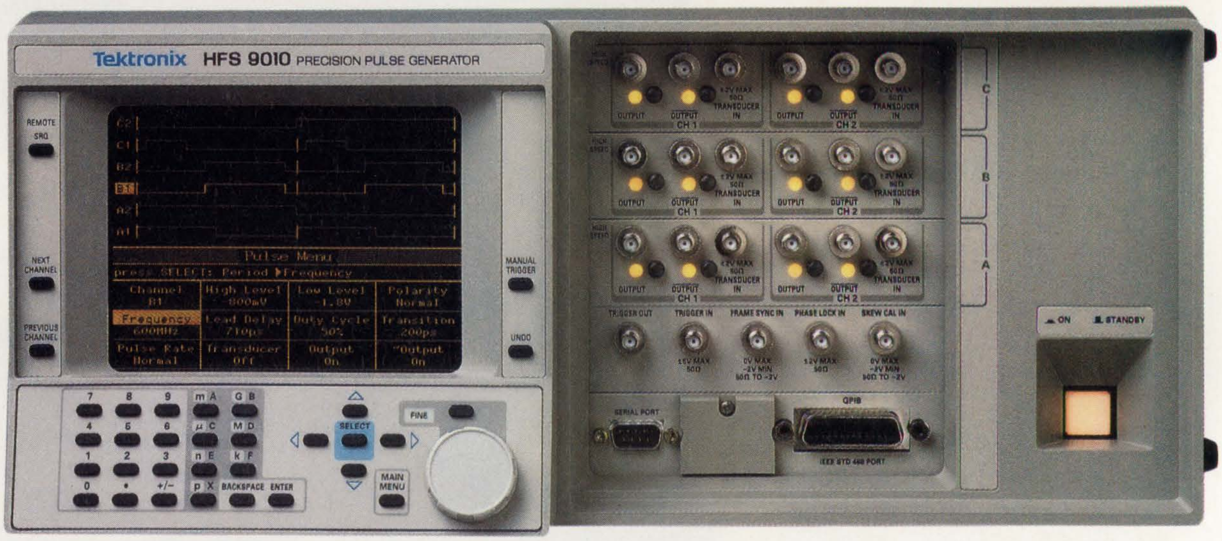

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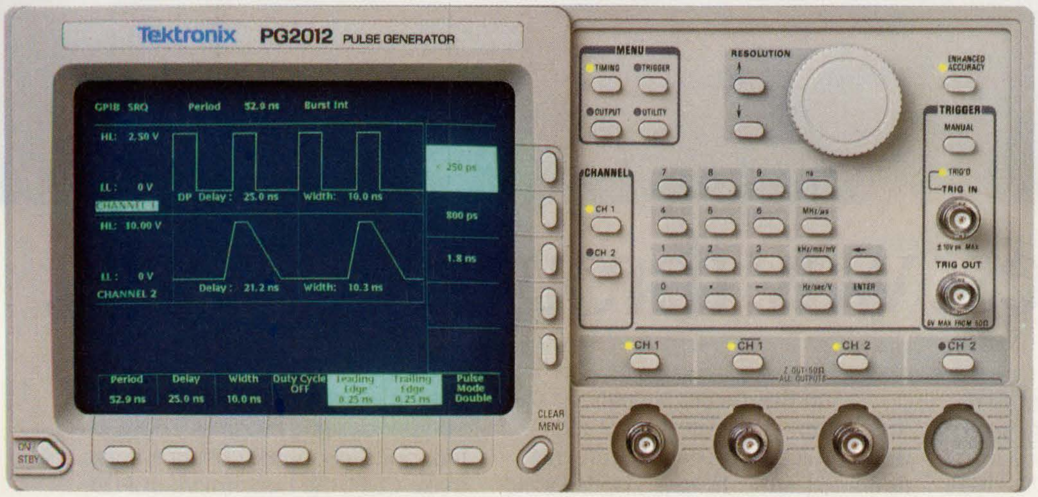

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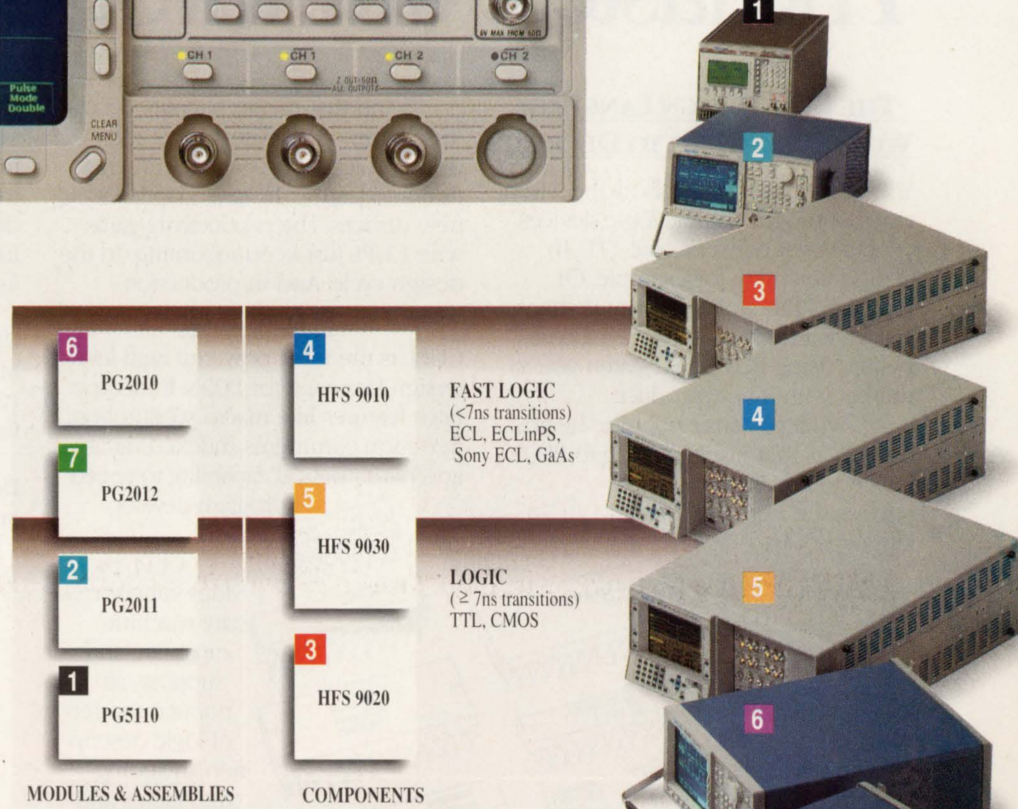

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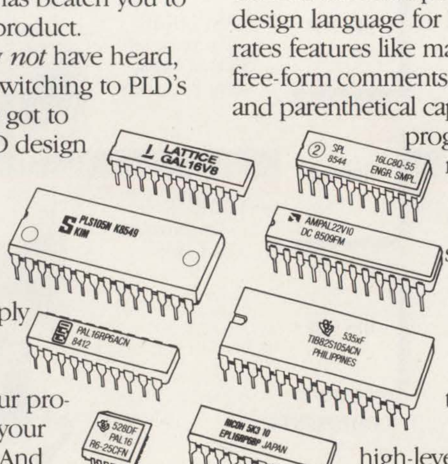

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CIRCLE NO. 113

Synthesis tools speed PLD design efforts

PLD design tools have moved beyond the compiler approach to offer design synthesis capability. You provide a high-level design description, and the tool does the rest.

Richard A Quinnell,
Regional Editor

As time-to-market pressure increases, designers' need for productivity aids is growing. Logic synthesis tools for PLDs are meeting that need. First introduced three years ago, the tools are still evolving, increasing their efficiency and expanding beyond PLDs to encompass FPGAs (field-programmable gate arrays) and other gate arrays. These tools now allow you to describe your design using whatever form is most convenient for you. They then optimize your design and automatically offer you a selection of the best parts for implementing that design.

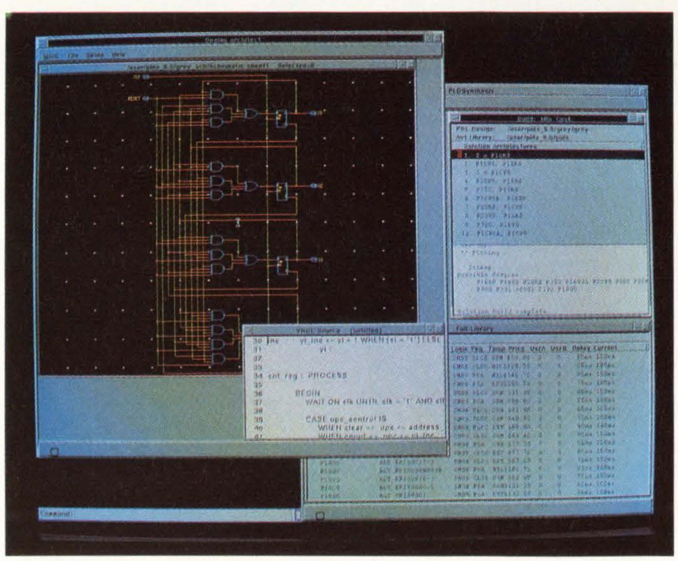
As logic synthesis tools have evolved, vendors have shown that they differ in what they mean by logic synthesis. The simplest definition, following the model developed by Gajski and Kuhn (**Ref 1**), is that logic synthesis translates a behavioral design description to a structural one. In the case of simple PLDs, the translation would convert Boolean equations to fusemaps.

While some vendors still use that definition, most consider synthesis to include refining higher-level design descriptions and optimizing circuits. Some stretch the definition of logic synthesis to include automatic partitioning of a design into multiple devices.

PLD synthesis tools' ability to optimize logic carries many advantages. The foremost advantage for today's accelerated engineering schedules is reduction of time to market. Once you've defined the function, the tools perform the tedious and error-prone optimization process orders of magnitude faster than humanly possible. Though the tools are by no means perfect, (see **box**, PLD synthesis: not a push-button solution) the time they save outweighs their limitations for most applications.

Finding the best solution

PLD synthesis tools also help you reach a good design quickly by allowing you to avoid making early decisions about implementation details. Using these tools, you can quickly adapt your high-level design to a variety of parts and technologies, then you can evaluate the results. Thus, you choose the best part for your application after your design is complete, instead of having to guess what's best (perhaps wrongly) be-



Offering design entry techniques from VHDL to schematic, *tools such as Mentor Graphic's PLDSynthesis allow you to focus on function, not implementation.*

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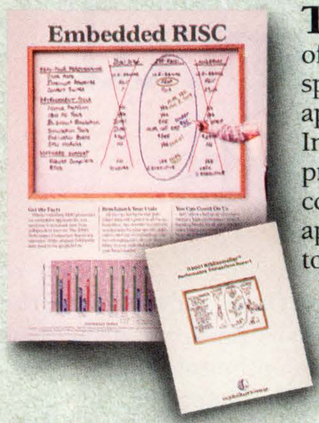

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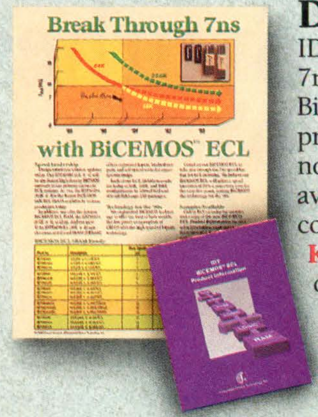

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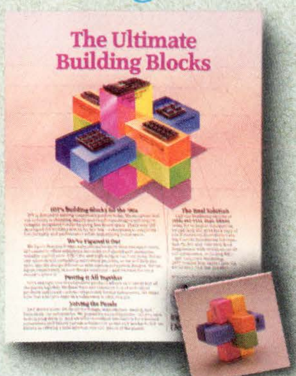

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fore beginning. A list of representative tools appears in **Table 1.**

Working with synthesis tools requires a design methodology that's different from methodologies used with earlier PLD tools. Early PLD tools operated like assembly-language compilers, taking your design description and converting it to a device-specific programming file. As with assembly language, you had to choose the target device before beginning design.

Choose parts last, not first

Today's synthesis tools invert the process, leaving the choosing-parts phase until close to the end of the design effort. Now you begin by describing your design in whatever form is most convenient for you. With most tools, you can choose from Boolean equations, truth tables, schematics, state-machine algorithms, and hardware description languages (HDLs) for the description. Tools based on Minc's technology also let you describe your design in terms of its waveforms.

Next, the tools allow you to verify that your design functions as you expected. The functional verification uses unit delays for timing, so you won't find any timing problems at this stage. You can, however, make sure that sequencing is correct.

Stand-alone synthesis tools, such as Data I/O's Abel, Isdata's Log/IC, and Minc's PLDesigner, verify only your PLD designs. When you use tools that have been integrated with a complete CAD package, however, you can extend verification to include simulated interaction with the rest of your circuit board. Cadence, Dazix/Intergraph, Mentor, and Valid have all incorporated one or more of the stand-alone tools into their systems.

Once you confirm that your design is functionally correct, the synthesis tools pick up steam. They can automatically perform a series of operations designed to reduce your design to its essentials. These operations include expanding negated compound equations into simple terms using DeMorgan's rules, eliminating redundant terms in each output signal, and combining terms common to a group of signals.

The circuit optimization techniques provided were once distinguishing features among the various synthesis tools. Revisions issued during the last six months have all but erased the distinctions. Two features that used to differentiate the tools, and that are included now in most of the revisions, are automatic output polarity selection and the use of "don't care" states in truth tables. These features allow the tools to reduce circuit com-

PLD synthesis: not a push-button solution

Despite the improvements made in PLD synthesis tools during the last three years, you cannot simply set them to work and accept the results. The tools still require a designer's insight to yield the best circuit.

For example, the tools won't produce as compact and fast a design as a knowledgeable engineer can. Synthesis tool vendors consider a synthesized design that achieves 80 to 90% of human performance to be standard. Even then, the efficiency of the tools varies with the type of design.

Algorithms that optimize state-machine designs, for example, are well developed, nearly matching human skills. When dealing with complex designs, the tools may find solutions even the experts miss. Designs that are unstructured or are register-intensive, on the other hand, are hard for synthesis tools to fit into PLDs. Logic with multiple levels is equally difficult, and asynchronous designs (if anybody wants them) are even worse. Even when the tools optimize well, you still must direct the process to achieve a tradeoff between a compact design and high-speed circuit operation.

The tools also force you to consider the PLDs separately from the rest of your design. With stand-alone tools, you have to import your partitioned PLD design to the CAD tool containing the rest of your schematics. Then you can test the PLDs as they interact with the other circuits. If the design is incorrect, you have to ping-pong between the two tools to solve the problem.

Even PLD tools integrated with a full CAD package segregate the PLD design portion. When using this integrated software, you have to collect the PLDs in their own block of schematic pages so that the PLD tool can find them.

An exception is Valid's System PLD. Valid's tool allows you to specify your programmable logic elements throughout the schematic at any level of the design description hierarchy. It will automatically collect and merge the PLD functions for optimization and partitioning, then back-annotate your schematic after you've selected the devices.

plexity substantially by eliminating unnecessary constraints. Without these features, you would have to try different polarities and truth table values manually until you found which attributes yielded the smallest design.

Partitioning methods vary

Still distinguishing the various tools are their methods for partitioning large designs into multiple devices. Some, like Minc's PLDesigner, offer automatic partitioning. All you have to do is specify constraints for the final design, such as number of devices used, device types that you allow, cost, or grouping of key signals. These tools try to fit your design into all combinations of allowed parts, then they report your best options, letting you make the final choice.

Data I/O's Abel-4 and Isdata's Log/IC take a different approach—their tools are interactive. You decide where to place each signal, then the tools advise you as to which additional signals must or should be included in the same device. The interaction may inspire you to make design changes—such as burying a node—that can substantially improve device utilization.

The best approach for you depends on which has more value—your time or your silicon budget. In the hands of a knowledgeable designer, an interactive tool can yield greater device utilization than an automatic one. The automatic tool, on the other hand, can work on solving your problem while you work on another project. It may even come up with designs you wouldn't think of because you're unfamiliar with some of the parts it can choose.

Synthesis tools that have optimizing and partitioning capabilities free you from having to understand the myriad architectures of simple PLDs. You're not off the hook altogether, however. You still need to understand the architectures of the more complex PLDs and of field-programmable gate arrays (FPGAs). The advent of these complex PLDs and FPGAs is stretching the capacity of automatic tools, and their par-

Table 1—Representative PLD synthesis tools

		Additional design-entry methods							
Company	Product	Waveform	EDIF	Hardware-description language	Partitioning	Library size (architectures/ devices/ device families)	Operating platforms	Base cost	Comments
Cadence Design Systems	Amadeus PLD			Verilog	Interactive	/4000/	SPARC, DEC, Apollo/HP	$12,000	Board-level CAD using Data I/O's technology.
Data I/O	Abel-4		x	Abel-HDL	Interactive	250/6000/	PC, Sun-3, SPARC, Apollo/HP, Integraph, DEC, Macintosh	$1995	
	Abel-FPGA			Abel-HDL	Interactive	//Xilinx, Actel, Plus Logic, Altera, AMD	PC, Sun-3, SPARC, Intergraph	$7995	Can include Abel-4.
Dazix/ Intergraph	PLD Master with Abel			Abel-HDL	Interactive	275/3400/	Intergraph, Sun	$8000	Board-level CAD using Data I/O's technology.
	PLD Master with Log/IC				Interactive		Sun	$11,000	Board-level CAD using Isdata's technology.
	PLDesigner Plus	x		Proprietary	Automatic	180/3000/	Intergraph	$14,000	Board-level CAD using Minc's technology.
	PGADesigner Plus	x		Proprietary	Automatic	//Actel, Altera, AMD, Xilinx	Intergraph	$19,000	Board-level CAD using Minc's technology.
Isdata	Log/IC		x	VHDL	Interactive	380//	PC, Apollo/HP, DEC, Sun	$1480 to $6700	Offers graphical state-machine design (flowcharting).
Logical Devices	CUPL, with PLPartition			Cupl	Interactive	240/3000/	PC, DEC, Sun, Apollo/HP	$695 to $2295	
Mentor Graphics	PLDSynthesis			Proprietary	Automatic	140/3000/	Apollo/HP	$14,900	Board-level CAD using Minc's technology.
Minc	PLDesigner	x	x	Proprietary	Automatic	/3200/	any DOS or Unix	$1950	
	PGADesigner				Automatic	//Actel, AMD, Xilinx		$2500	
Valid Logic Systems	System PLD	x	x	Proprietary	Automatic	/3000/	DECstation, Sun, RS/6000	$13,500	Board-level CAD using Minc's technology.
	System PGA					//Actel, Xilinx			

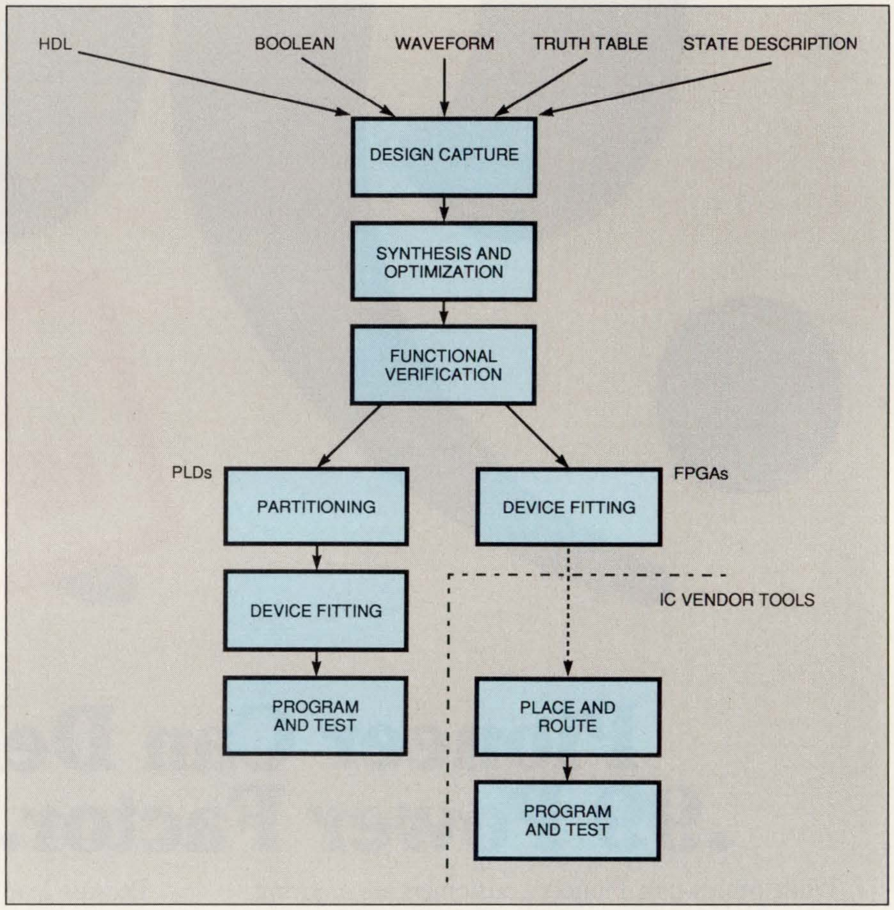
Note: All tools offer schematic, Boolean, truth-table, and state-machine design entry.

PLD logic synthesis tools

titioning software has not yet caught up. When dealing with such complexity, you'll have to select the target device based on your own knowledge.

The tool vendors are responding to the demands these complex devices place on their software by creating a separate design path for them, as shown in **Fig 1.** This design path includes a detour to tools outside of their own tools. Acknowledging that device vendors have the greatest insight into device architectures, the PLD synthesis tool vendors are forging links to the device vendors' design tools instead of creating their own.

This may seem like a step backward in design methodology. Instead of having a single tool handle your design from description through implementation, as with PLDs, you have to send your design to a second, device-specific tool. And if you're going to design predominantly in FPGAs, the prospect of moving from one tool to another may tempt you to use just the device vendor's tool. However, if you use the PLD synthesis tool as a



Parts selection is the final design step *when using today's PLD synthesis tools, as this work-flow diagram shows. Earlier PLD design tools required that you select the part before beginning design.*

For more information . . .

For more information on the PLD synthesis products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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FAX (408) 943-0513
Circle No. 700

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Redmond, WA 98053
(206) 881-6444
FAX (206) 881-6856
Circle No. 701

Dazix
An Intergraph Co
1 Madison Industrial Park
Huntsville, AL 35894
(205) 730-2000
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Isdata Inc
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Monterey, CA 93940
(408) 373-7539
FAX (408) 373-3622
Circle No. 703

Logical Devices Inc
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(305) 974-0975
FAX (305) 974-8351
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Wilsonville, CA 97070
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in CA, (503) 685-8000
FAX (503) 685-8001
Circle No. 705

Minc Inc
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(719) 590-1155
FAX (719) 590-7330
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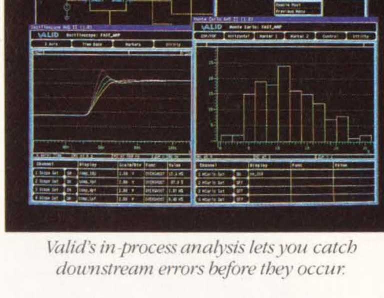

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front end, you keep the advantage of being able to choose the target technology after you create the design, instead of before.

If you use a PLD synthesis tool for FPGA design, the tool will optimize your design for the target device, then produce an output file that the device vendor's tool accepts. The format of that output file varies with the synthesis tool vendor. Isdata and Minc provide vendor-specific formats, matching the native format of each device-vendor's tool to take maximum advantage of the part's architecture. Data I/O takes a more open-architecture approach; its output files are in PDS or Abel-PLA format, allowing a variety of FPGA and ASIC design tools to accept the same file.

Adapting to encompass FPGAs is only one way that PLD synthesis tools are evolving. Another is their inclusion of industry standard interfaces. Electronic Data Interchange Format (EDIF) and VHSIC Hardware Description Language (VHDL) interfaces, for example, are under development at most of the PLD synthesis tool vendors. You will probably see these interfaces become widely available during the next six to nine months; some are ready now. Isdata, for example, has translators that accept VHDL and EDIF design descriptions for its Log/IC tool. In addition, Isdata, Logical Devices, and Mentor Graphics offer EDIF output files.

The continuing evolution of PLD synthesis tools isn't stopping with programmable devices. Vendors have already taken steps toward encompassing gate arrays. Data I/O's output file format, along with the other vendors' EDIF output format, makes it possible for your design to migrate from PLD and FPGA to ASIC tools. Furthermore, Isdata offers a tool called Hint that flattens a PLD design so you can implement it in a gate array. And there is no telling how far along the path to ASICs the PLD vendors can take their tools, allowing you to design while having access to the entire range of user-defined logic.

EDN

Reference

1. Markowitz, Michael C, "Logic synthesis prepares for VHDL," *EDN*, March 30, 1989, pg 51.

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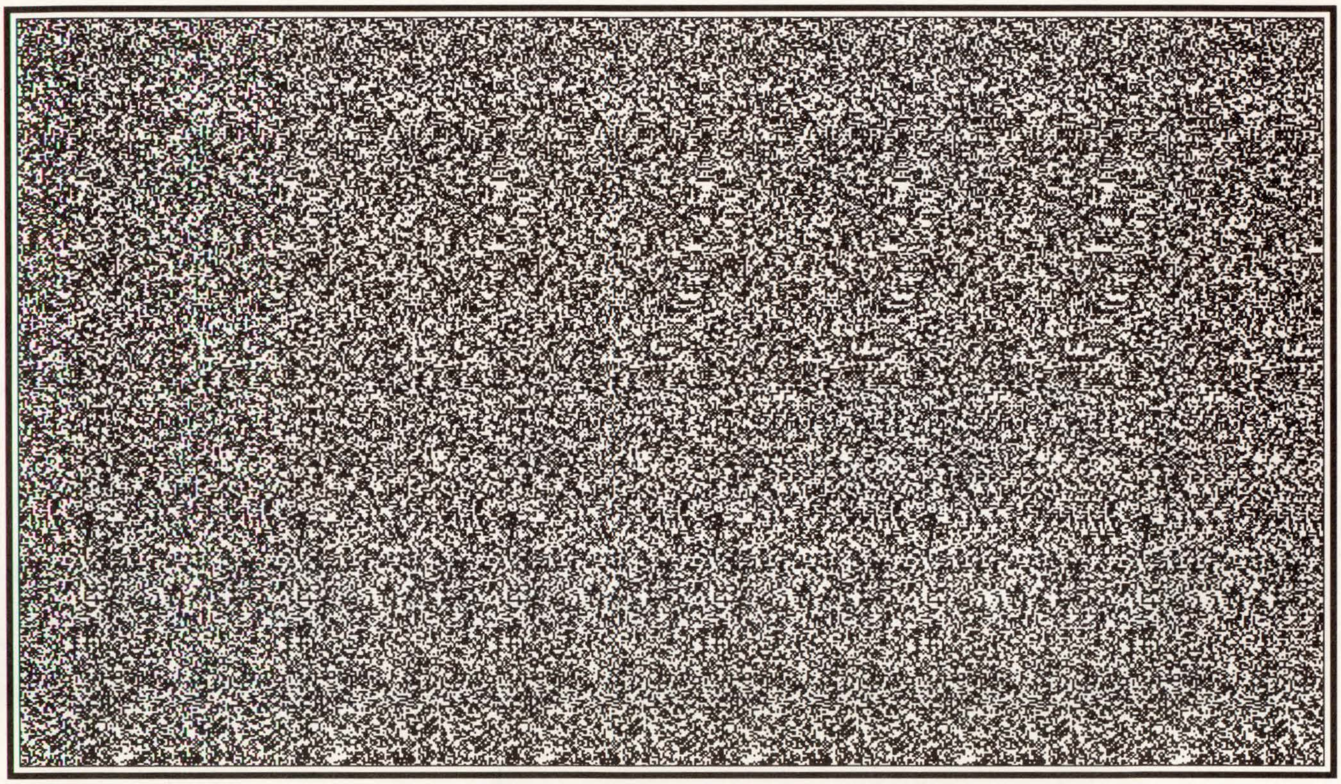

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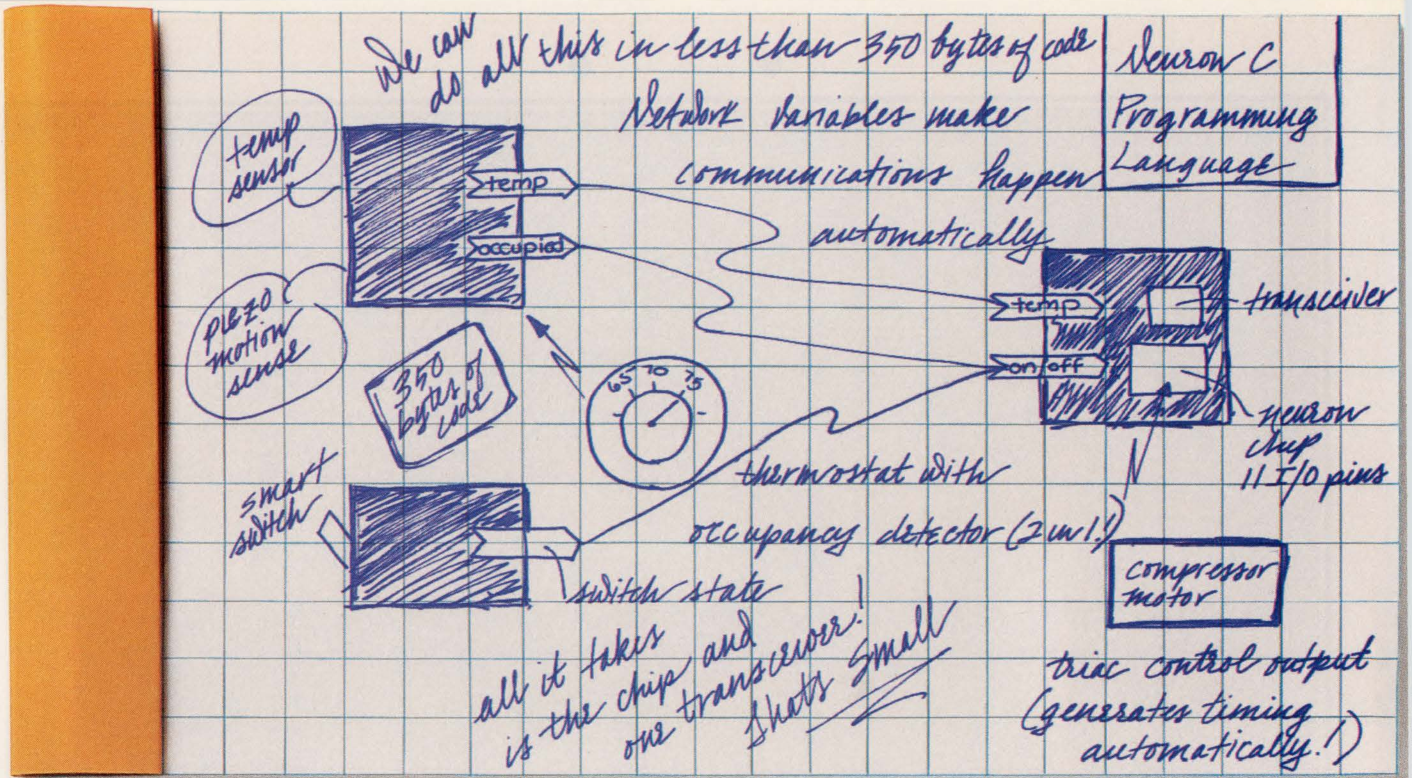
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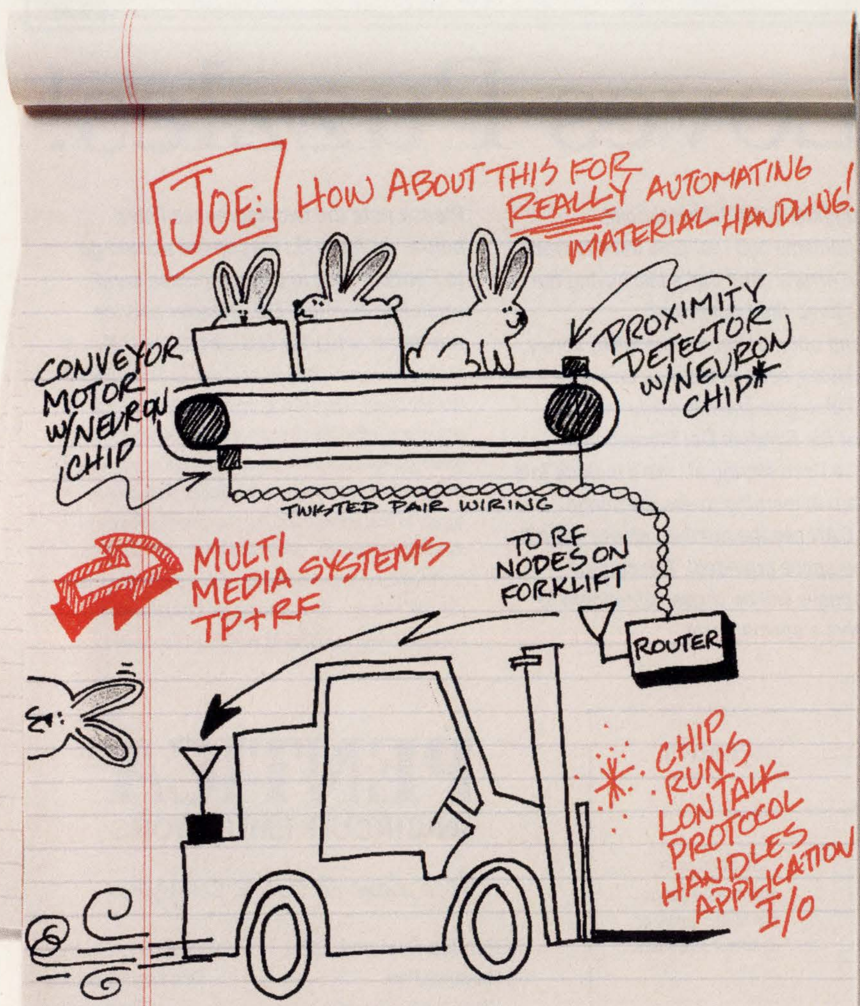
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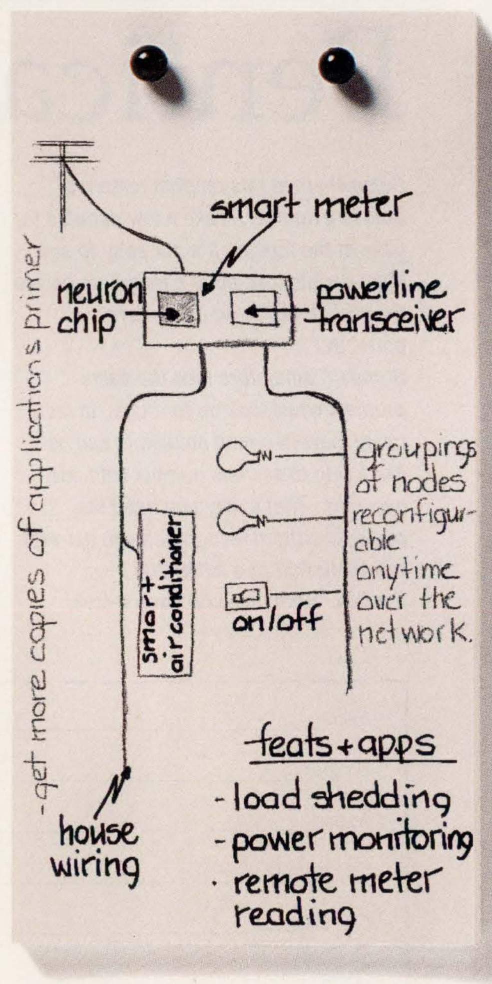
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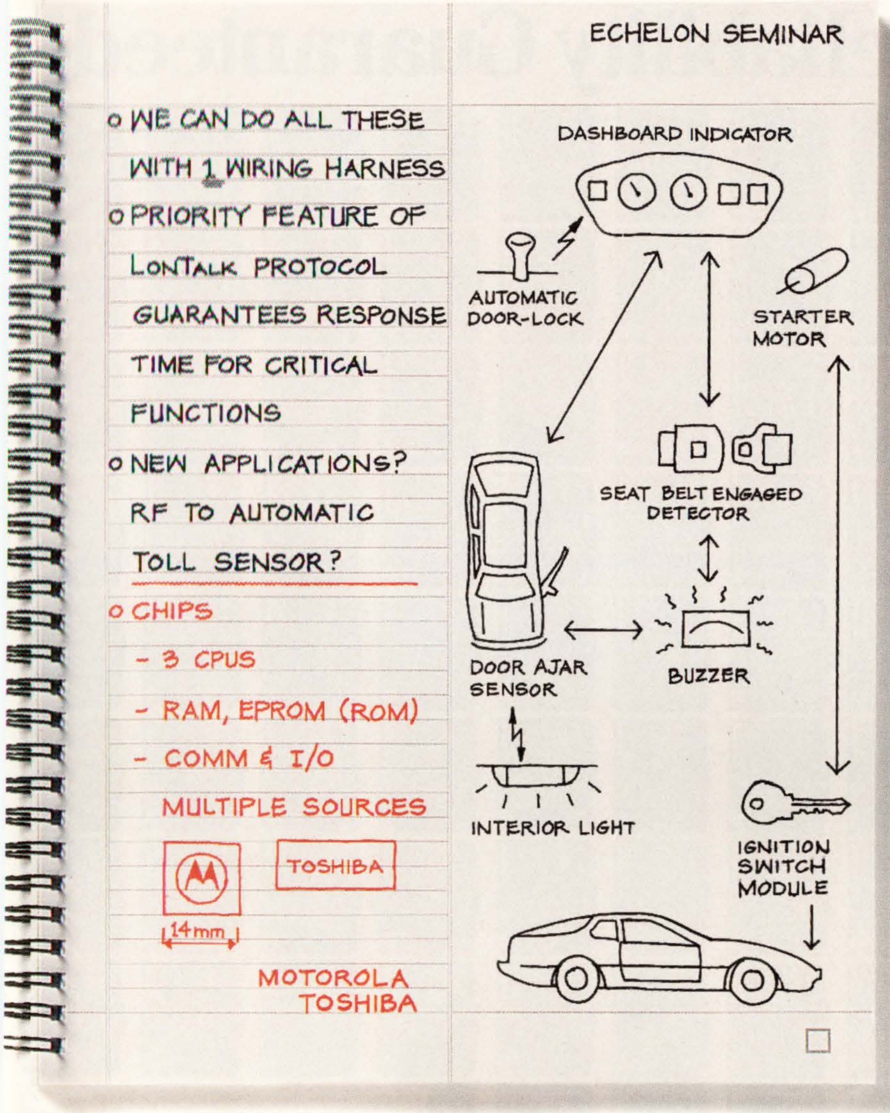

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Without GaAs, RISC workstation family breaks 55-MIPS speed limit

Just as IBM made its re-entry into the workstation field with its RS6000 last summer, Hewlett-Packard/Apollo has declared that it shouldn't be counted out. The HP/Apollo 9000 Series 700 workstations run at 57 and 76 MIPS, or at 55.5 and 72.2 SPECmarks using a CMOS CPU. Spec integer performance ranges from 39 to 51 VAX MIPS, and floating-point performance is 70.2 to 91 VAX MIPS.

The Precision-RISC-based computers are available in three models. The base model 720 starts at $11,990 and, like its two siblings, comes standard with 16M bytes of RAM.

The memory in the two lower-end machines is expandable to 64M bytes. Although the 720 base unit is diskless, you can add as much as 840M bytes of internal storage or as much as 10G bytes of external disk capacity via its standard SCSI-2 port. The 50-MHz Precision CPU uses a 256k-byte data cache and a 128k-byte instruction cache.

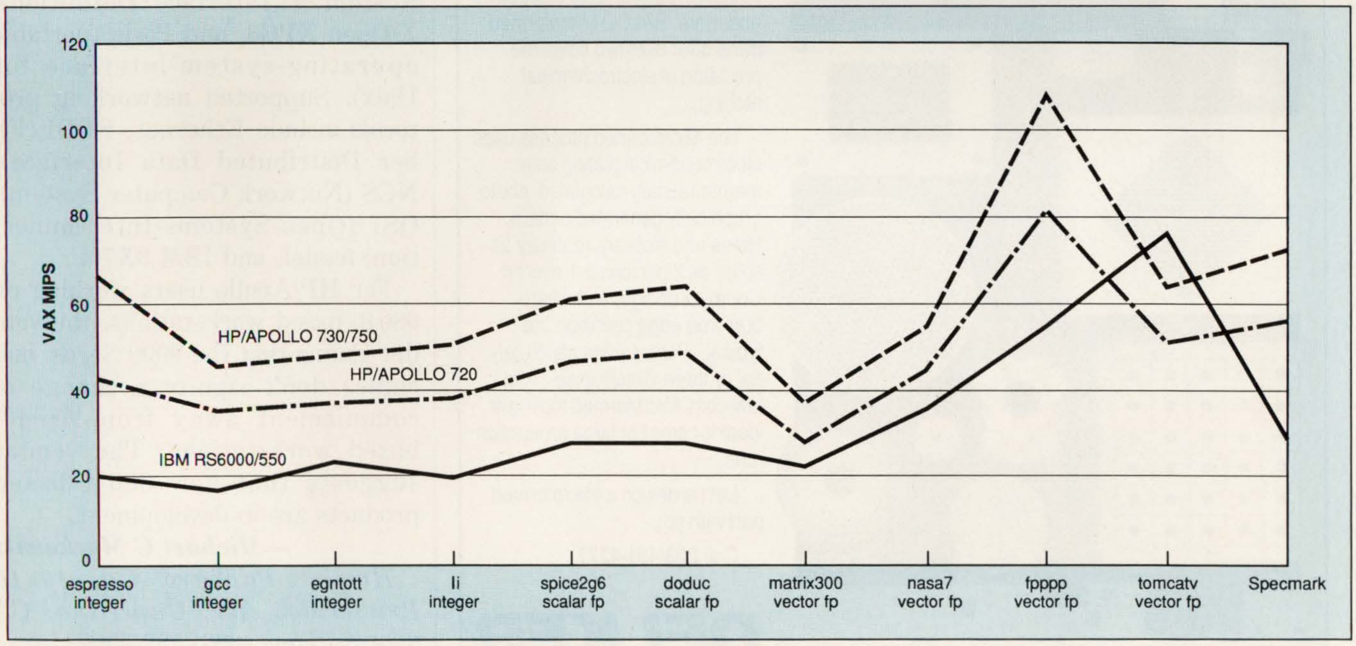
The mid-level machine, the $19,990 Model 730, uses a test-selected 66-MHz CPU to improve its throughput. The workstation also adds a 200M-byte hard disk. Like its 50-MHz sibling, this workstation accepts as much as 10G bytes of disk capacity. The EISA (extended-industry-standard architecture) slot is optional in the low-end machine, but it comes standard in this machine.

The $43,190 Model 750 rounds out the family. This desk-side workstation/server offers a 660M-byte hard disk. Although it too comes equipped with 16M bytes of RAM, you can furnish the system with as much as 192M bytes of 2-way interleaved RAM. To improve instruction-cache (I-cache) hit rates, this workstation doubles its I-cache to 256k bytes.

All of the workstations feature Ethernet, RS-232C, Centronics, and HP-HIL ports for network and peripheral-device connections. And where the 720 has an optional EISA slot and the 730 has one EISA slot, the 750 has four EISA slots. All of the machines offer optional CD-ROM and 4-mm digital audio-tape capabilities. The CD-ROMs can provide operating-system, application, and documentation access.

Four levels of graphics performance are available on the Series 700. The starting gray-scale GRX is available on the basic 720 and 730 workstations. The CRX is the entry-level color system and is included with the 750. The GRX and CRX graphics subsystems provide 1.15M 2-D vectors/sec and 8044 X11 vectors/sec performance. The two high-end graphics systems use one to four i860 dedicated graphics processors to provide as much as 1.3M 3-D vectors/sec and 195,000 lighted and shaded polygons/sec.

For workstation users committed to some of their DOS applications, the 66-MHz CPU provides 20- to 25-MHz DOS emulation via a $700 Insignia emulator license. The



Benchmark results give an indication *of the type of performance you might expect from the HP Series 700 workstations.*

workstation uses HP/Apollo's 9000 Series 800-level binary code so you won't need to recompile Series 800 applications that don't use or need the graphics or floating-point capability of the Series 700.

Although the vendor claims that more than 2000 software applications run on Precision-based workstations, the 9000 Series workstations don't yet have a significant base of electronic-design-automation (EDA) applications. However, a few EDA vendors, among them Mentor Graphics, Cadence Design Systems, Racal-Redac, and Zuken say they will port their software. Racal's software will be released this summer. Mentor's port should be available before the end of the year, but Cadence didn't offer a release schedule. Other EDA vendors, such as Synopsys, Valid, Vantage, and Viewlogic, are waiting for user demand to grow before committing to a port.

The workstations use the HP Vue user interface, a refinement of the OSF/Motif GUI (graphical user interface). The 9000 Series machines run the OSF/1 version of Unix and are compatible with SVID (Unix System V Interface Definition), X/Open XPG3, and Posix (portable operating-system-interface for Unix). Supported networking protocols include Ethernet, FDDI (Fiber Distributed Data Interface), NCS (Network Computer System), OSI (Open-Systems-Interconnection) model, and IBM 3X70.

For HP/Apollo users working on 68040-based workstations, the vendor claims that the 9000 Series machines don't signify a change of commitment away from 68040-based workstations. The vendor suggests that new 68040-based products are in development.

—Michael C Markowitz

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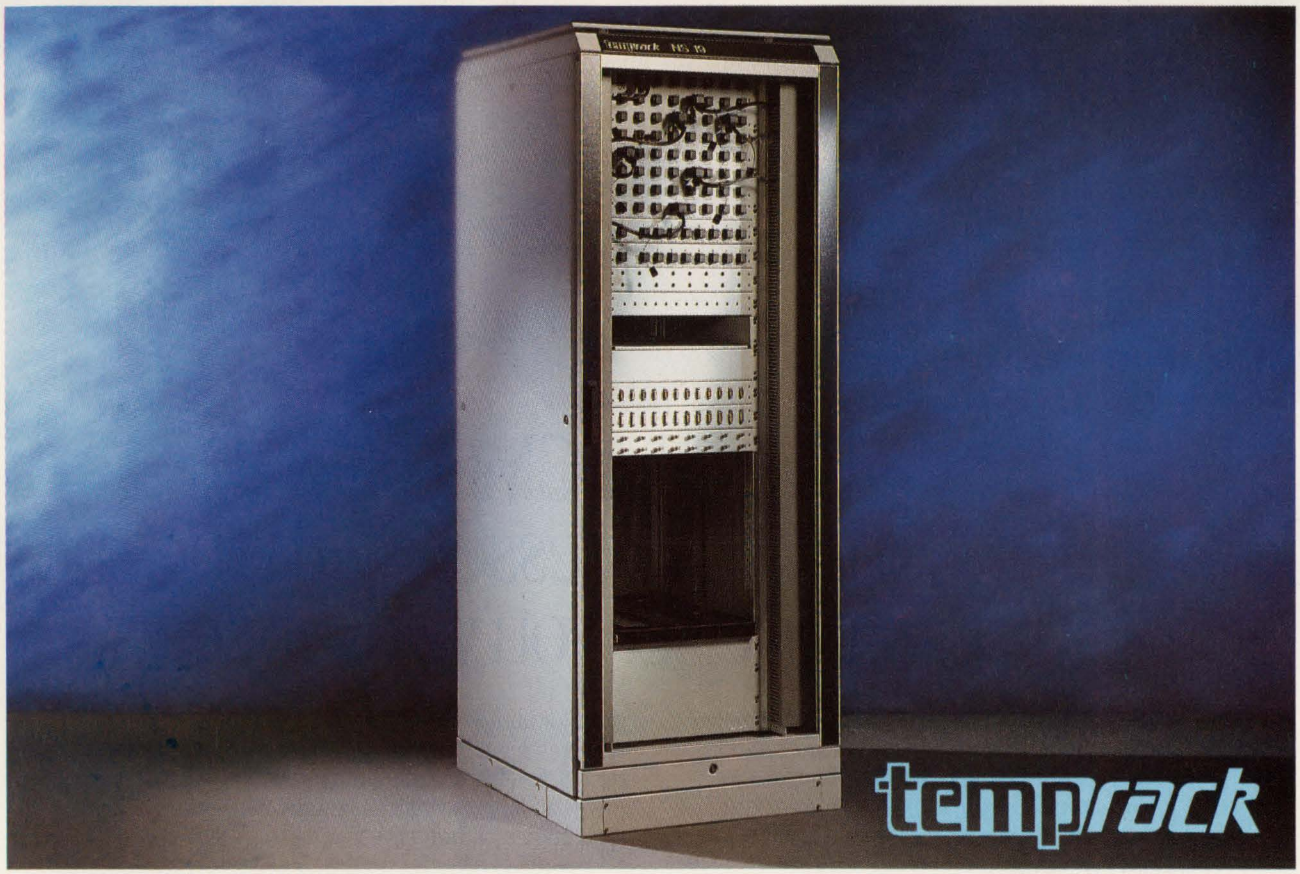

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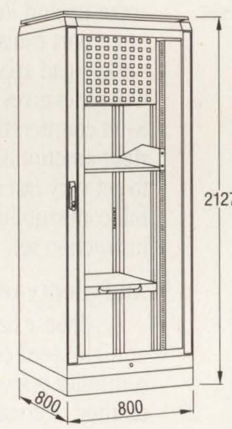

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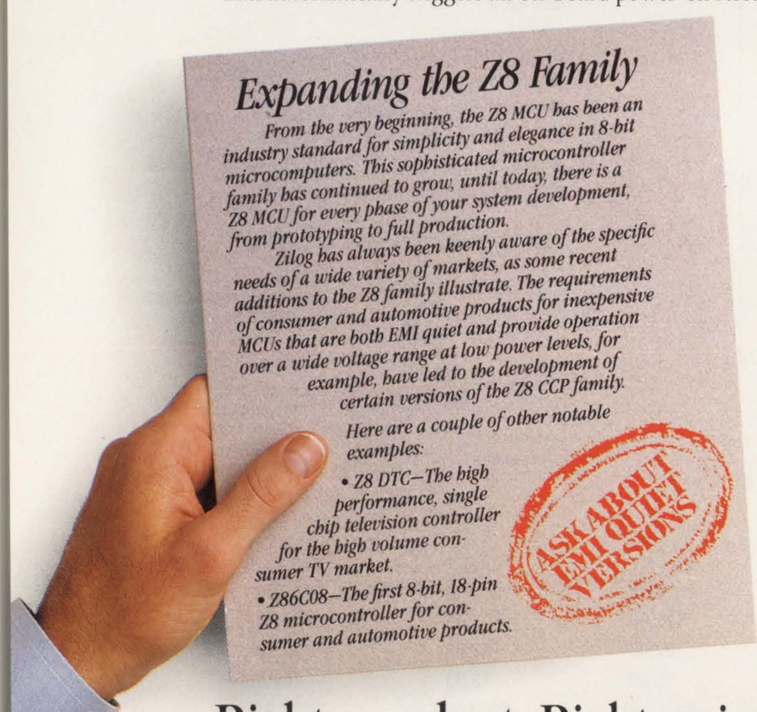

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Low-cost ac instruments offer high accuracy

Keithley is entering the ac-instrumentation field with five products: two LCZ meters and three multifunction synthesizers. These products simplify the process of testing your circuit or device by automating setup procedures and measurement parameters. The prices for these instruments are as little as one-third the prices of comparable instruments sold by other manufacturers.

The Model 3321 and 3322 LCZ meters are 4½-digit, IEEE-compatible units that offer 0.1% accuracy for inductance, capacitance, and impedance measurements. Dissipation and quality measurements display with 0.0001 resolution; phase resolution is 0.01°. You can select ac test voltages of 1V or 50 mV. To operate either meter, just connect the device you're testing and take a reading—both units automatically identify the type of circuit and display all applicable outputs. Both meters also come with an internal 2V bias source, but you can supply an alternate external bias source as large as 35V.

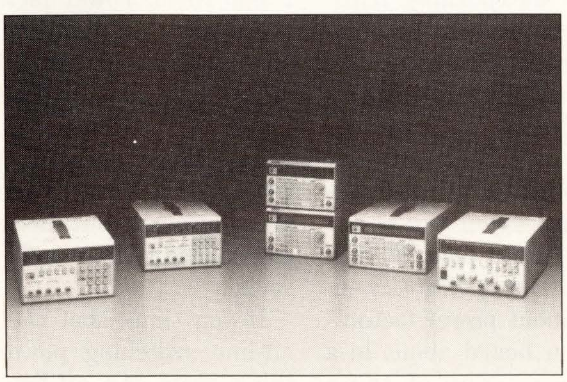
The $3490 Model 3321 has 150-msec and 480-msec trigger-reading rates and offers test frequencies of 120 Hz, 1 kHz, 10 kHz, and 100 kHz. The Model 3322 costs $3990, has eleven test frequencies, and adds a 64-msec trigger-reading rate. The 3320 can also read percent deviation from a preset value and identify what kind of device it's testing.

The three multifunction synthesizers use Direct Digital Synthesis (DDS) to ensure phase-continuous waveforms. Using DDS allows the units to change frequencies without taking several cycles to stabilize. The units are accurate to 5 ppm and have five built-in waveforms, trigger/burst/gate functions, and on/off oscillation control.

The $3590 Model 3930A offers 11-digit output resolution, a range of 0 Hz to 1.2 MHz with 0.1-mHz resolution, and a 30V p-p output voltage. The $5390 Model 3930 has 12-digit output resolution, a range of 0 Hz to 20 MHz, a 20V p-p output, and two built-in synthesizers that can act as a 2-phase oscillator or a harmonic generator. Both models have a built-in IEEE-488 interface and sweep capability over the entire range. The 3930 also has burst capability over its range. If your application doesn't require such accuracy, the $1695 Model 3910 is accurate to 30 ppm over a range of 0 Hz to 1 MHz.—***J D Mosley***

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (216) 248-0400. FAX (216) 248-6168.

Circle No. 730



Offering improved price/performance ratios, *Keithley enters the ac instrumentation market with two LCZ meters priced less than $4000 and three multifunction synthesizers priced less than $5400.*

Power-factor-corrected switching power supplies

Goaded by the IEC and encouraged by IC vendors, firms that make switching power supplies are starting to correct a long-standing problem: their products' propensity to draw nonsinusoidal line currents.

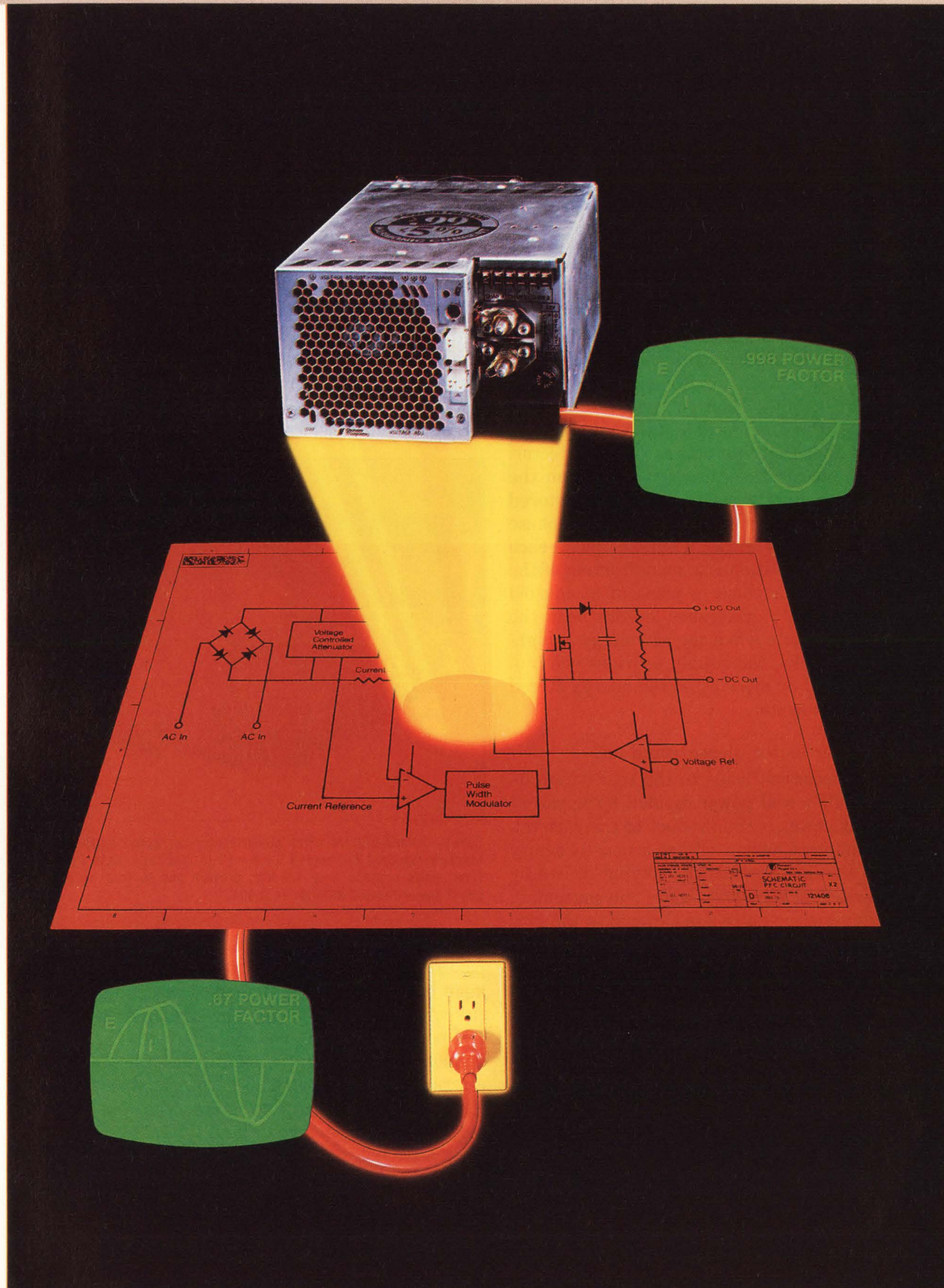
Dan Strassberg, Associate Editor

You designed your system conservatively. You know that the power supplies can handle their loads. When you figured out what the worst-case ac line current would be, you took the supplies' maximum dc output power, divided it by the supplies' efficiency, and then divided the result by the lowest line voltage at which you said the equipment would operate. But when the supplies are heavily loaded, every now and then the circuit breaker inexplicably trips. You tell yourself that the problem must be transient surges—that you just need a clean ac line or a circuit breaker that has a higher rating or a less aggressive current-vs-time trip characteristic.

If the preceding scenario sounds a bit too familiar, you should start to wonder about the power factor of the incoming ac. "Power factor?" you ask, somewhat incredulously. "But *electronics* engineers don't need to worry about power factor!" Power factor is something you heard about in a course on electrical machinery—one of those courses your adviser made you take because the EE faculty thought all EEs ought to know something about machines. Neither you nor any of your friends could see the relationship between electrical machinery and the kind of work you wanted to do after graduation, so none of you paid much attention.

You remember, though: Power, $P=EI\cdot\cos\Theta$. E and I are the rms values of sinusoidal voltage and current waveforms; Θ is the phase angle between them. Power factor, $PF=\cos\Theta$. And then there was that dumb mnemonic they taught you about Eli the ice man. E (voltage) leads I (current) in an inductive circuit—one where inductance, L, predominates; I leads E in a circuit where capacitance, C, predominates. The preceding applies only when the voltage and current are sinusoidal. But, heck, back in that machinery course, the voltage and current were always sinusoidal.

If you think that the current drawn by most off-line switching power supplies is sinusoidal, think again. An off-line supply is one that first creates a high dc voltage by directly rectifying



By using power-factor correction, a switching power supply can transform a harmonic-laden current into a safely consumable sinusoidal current. (Photo courtesy Pioneer Magnetics)

If you think that the current drawn by most off-line switching power supplies is sinusoidal, think again.

and filtering the incoming ac, without first passing the ac through a transformer. The high dc voltage is converted to high-frequency ac, transformed (usually to a lower voltage), rectified, and filtered. In the initial stage of directly rectifying and filtering the ac line, most off-line switchers use capacitor-input filters.

"So," you say, "it's the capacitor-input filter that makes the power supply's input current lead the line voltage." Hardly—the *combination* of the supply's rectifiers and input filter capacitor acts as a peak detector; current flows to charge the capacitor only when the instantaneous ac voltage exceeds the voltage stored on the capacitor. In other words, in a single-phase system an off-line supply draws a current pulse each half cycle. The pulse duration is a small fraction of the half-cycle duration. The pulse, a piece of a sinusoid whose shape is called a haversine, occurs near the midpoint of the half cycle when the ac voltage is highest. Between the peaks, the supply provides continuous power to the load by drawing on the energy stored in the input filter capacitor.

Will the real power factor please stand up?

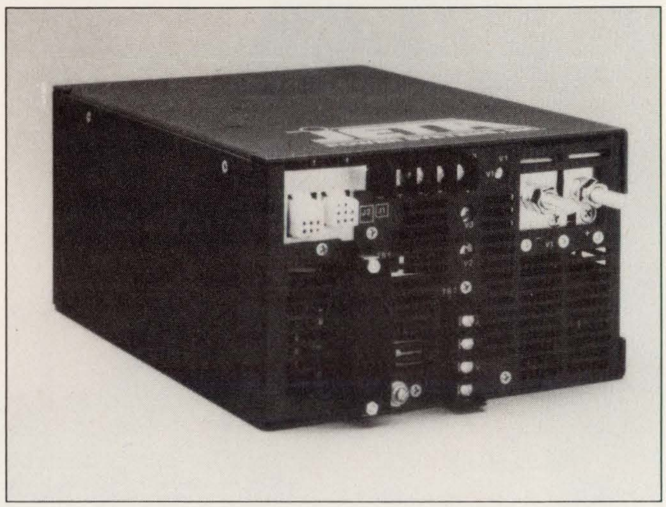
The previous discussion leads to the real definition of power factor: PF = real power divided by apparent power. Apparent power is the product of the rms values of the line voltage (the line voltage is usually nearly sinusoidal) and the line current (the current drawn by most off-line switching supplies is quite nonsinusoidal). In such a supply you actually don't calculate the rms input current by dividing the supply's output power by its efficiency and dividing the quotient by the rms input voltage. The result of such a calculation would significantly understate the rms input current.

If you think about the problem in the frequency domain, you will remember that you can consider any periodic waveform to consist of a summation of sinusoids. If you integrate the product,

$$E_1 \cdot \sin(\omega t) \cdot I_n \sin(n\omega t + \Theta),$$

where n is the harmonic number, over one cycle of the fundamental, only when $n = 1$ is the result not zero. (E_1 is the amplitude of the fundamental-frequency component of the line voltage. I_n is the amplitude of the *nth* harmonic component of the current.) Because the line voltage is essentially sinusoidal, but the current is nonsinusoidal, only the current's fundamental-frequency component will affect the power. However, the harmonics present in the current waveform can have a profound effect on the rms value of the current.

The reason that the harmonics affect the rms current is that I_{rms} is the average over the waveform period of the integral of the *square* of the current. Every harmonic term is multiplied by itself. The integral of a sinusoid squared over one or more periods is always greater than zero. Therefore, although the harmonics in the nonsinusoidal current waveform contribute nothing to the power consumed by the supply, they can make the supply's rms input current considerably greater than the rms value of the fundamental-frequency component.



Several manufacturers offer power-factor-corrected supplies in the industry-standard fan-cooled 5×8×11-in. package. Jeta Power Systems' units produce 1 or 1.2 kW, provide one to four outputs, and boast power factors as high as 0.998.

The real power delivered to the supply is the output power divided by the efficiency. To obtain the rms input current, you must do one of two things: measure the current with a wideband ac ammeter or divide the real power by the line voltage and divide the resulting quotient by the power factor. Because the power factor can never be greater than 1, the supply's rms input current will almost always exceed the real power divided by the rms line voltage. A typical off-line switching supply will have a power factor of approximately 0.7, so the line current will be about 40% greater than you would calculate if you ignored power factor.

Supplies that have extra long "holdup" time—the time that they will continue to supply power to a load after the incoming ac power fails—can have even lower power factors. Off-line switchers with full-load power factors as low as 0.6 are common. At any given value of load, a switching supply will exhibit the lowest power factor when its input line voltage is highest.

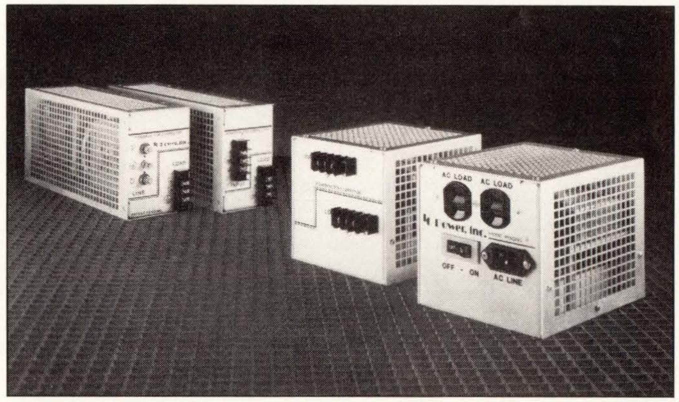
The harmonics' effect in inflating the rms current can cause other mischief besides the nuisance of tripping circuit breakers mentioned earlier. Suppose your system uses 900W of dc power and that you intend it to operate from an ordinary 120V, 15A branch circuit. According to Underwriters' Laboratories (UL), equipment connected to a "15A" circuit should draw no more than 12A for sustained periods. If your power supply is 75% efficient, its input power will be 1200W. If you specify your system to operate normally when the line voltage drops to 100V, it will draw a maximum current of 12A—provided the power factor is 1.

If the power factor is 0.7, the current will exceed 17A rms. That value is not merely greater than the derated value of 12A that is considered safe on a sustained basis in "15A" circuits; it is greater than the circuit's 15A rating. If a system with a supply having a 0.7 power factor and 75% efficiency is to operate for long periods with a line voltage of 100V on a (nominally) 120V, 15A branch circuit in the US, it must consume no more than 630W of dc power.

Three-phase, 4-wire "wye-connected" power systems can have an even more insidious problem. In such systems, loads are connected from each phase to neutral. If the load currents are sinusoidal, equal, and in phase with the phase voltages, the current in the neutral wire will be zero. But if the loads consist of switching power supplies that draw nonsinusoidal currents, even if the fundamental-frequency components are equal and are in phase with the phase voltages, the harmonic currents that flow in the neutral wire are unlikely to cancel.

In fact they can add in such a way that the rms value of the neutral current exceeds the current in any phase. It is customary for the neutral wire to be of the same gauge (diameter) as the phase wires. For a 3-phase system's neutral wire, choosing a wire gauge that equals the gauge of the phase wires is thought to be a conservative practice. After all, under ideal conditions, the neutral wire carries no current. But because of harmonics, the neutral wire can, in some cases, carry a current larger than the currents in the phase wires, and so should be of a larger gauge.

The situation described in the previous paragraph reveals the possibility that circuit breakers could fail to protect a building's wiring. For safety reasons, circuit breakers do not interrupt the neutral leg of 3-phase power systems. If the neutral conductor carries an rms current that is, say, 25% higher than the current in any phase conductor, there is a possibility of excessive temperature rise in the neutral conductor and, over time, damage to the wiring insulation. (Remember, the temperature rise is proportional to the square of the current.) In existing buildings, changing the wiring to correct this potential problem is an expensive proposition. Eliminating the source of the problem—the harmonic currents—is a better solution.



If you don't want to switch to a new power-supply model or a new vendor, you may be able to add a PFC module between the ac line and your existing supply. These ac-in/ac-out units from HC Power offer power factors of 0.98 with 98% efficiency. Power ratings range from 500 to 4000W.

IEC 555-2, a power-factor standard

The preceding discussion demonstrates that the growing use of switching power supplies in electronic equipment is making power factor increasingly important. The problem is becoming so significant that the International Electrotechnical Commission (IEC) has drafted a standard for power-factor correction (PFC). The standard, IEC 555-2, applies to equipment that operates from 220V (nominal) ac lines. Unless there is an unforeseen delay, beginning in 1992, equipment covered by the standard and sold in Europe will have to comply. More about IEC 555-2 later.

Ever since the invention of the off-line switching power supply, a technique has existed for increasing the supplies' power factor considerably beyond 0.7. That technique, which really predates the invention of the off-line switcher, is the use of LC (inductive-capacitive) input filters. The problem with LC input filters is that they use inductors (chokes) that are large, heavy, and somewhat expensive. Hence, using inductors in an off-line switcher's input filter network does away with at least part of the advantage of switching technology over linear power-supply technology. Even so, because of the technique's inherent simplicity and reliability, several manufacturers continue to introduce new supplies that use LC filters for power-factor correction.

Filter inductors that operate at line frequency (or

Table 1—Representative power-factor-corrected switching power supplies[1]

Vendor	Product	When introduced	US price[2]	Added cost for PFC[3]	Maximum output power	Has own fan(s)?	Dimensions (inches)	Number of outputs	Input voltage and frequency
Abbot	AW and AM	11/90	$900 (1)	20%	75W	No	2×2×0.85	Multiple	103.5 to 126.5
Astec	JF201	1990	$991 (1)	NA[5]	2 kW	Yes	5×8×10	1	180 to 264V 1 or 3 phase
Computer Products	Special	1986	Varies[6]	$100 (OEM qty)	1500W	Varies[6]	Varies[6]	Varies[6]	90 to 130V 180 to 260V 47 to 63 Hz
Deltron	FM Series	Q2 '91	$705 to $827 1 kW (OEM qty) 2 kW $1131 to $1358	$325 1 kW $410 2 kW	1 kW 2 kW	Option (1 kW) Yes (2 kW)	1 kW: 12×6.5×2.5 2 kW: 5×12×6.5	1 kW: 1 to 7 2 kW: 1 to 8	1 kW: 90 to 264V 2 kW: 180 to 264V Both: 47 to 63 Hz
HC Power	Power-miser	1988	$300 Stand-alone PFC	Not applicable	250W to 4 kW	3 kW and 4 kW only	5×3.5×11.25 to 1 kW	1: ac to ac to dc supply	90 to 132 V or 180 to 246V
	HC1010	4/91	$1450 (1)	$300	1 kW	Yes	5×8×11.25	1 to 4	90 to 264V 47 to 63 Hz
	HC1501	4/91	$1500	$300	1.5 kW	Yes	5×8×11.25	1	90 to 264V 47 to 63 Hz
Jeta	N100x	3/90	Under $900 (OEM qty)	Under $100	1 kW	Yes	5×8×11	As many as 4	90 to 264V
	N120x	3/90	Under $1000 (OEM qty)	NS	1.2 kW	Yes	5×8×11	As many as 4	90 to 264V
Kepco	Ray Series	11/90	$2395	NA[5]	3 kW	Yet (3)	4.3×13.4×12.7	1	170 to 264V 3 phase
Lambda	SMS-1500 SMM-1500	8/89	SMM: $1479 to $1698 (100)	NA[5]	1.5 kW	Yes	5×8×11	SMS: 1 SMM: 1 to 5	176 to 264V 48 to 65 Hz
LH	PSMA line	1989	750W: $1055 (1) 2 kW: from $1700 (1)	$350 to $400	0.75, 1, 1.25, 1.5, 2 kW	Yes	5×8 Depth 10 to 14[8]	1 to 4	85 to 264V
NCR Power	680W 4 output	Q2 '91	$500	10%	680W	No. You pro- vide 100 cfm	11.25×15.35×3.82	4	180 to 257 V 49 to 60.6 Hz
Pioneer Magnetics	PM3187A	11/90	$1485 (1)	$250	1344W	Yes	5×8×12.25	2 to 5	96 to 264V 47 to 63 Hz
Power One	SPF4 Series	12/90	1250W: $1403 (1), $1091 (OEM qty)	$260 (1) $204 (OEM qty)	1.35 kW (120V) 1.5 kW (240V)	Yes	5×11 Width: 3 to 8[9]	1 to 12	85 to 264V 47 to 63 Hz
Puls	PS 1000	1989	Under $3000 (OEM qty)	NA[5]	4 kW	Yes	16.8×16.9×6.9	4	230V 1 phase 115V 3 phase 230V 3 phase
Sorensen	DCS Series	Q3 '91	$3500 (1)	NA[5]	3 kW	Yes	3.5×19×18	1 variable	190 to 253V 47 to 63 Hz
Todd Products	Max-1000 line	4/91	$1150 (1), $800 (OEM qty)	$80 to $100 1 kW (OEM qty)	1 kW	Option[10]	8×12×3.4 with fan	4	90 to 264V 47 to 63 Hz
Transistor Devices	MPS Series	12/90	$1096 to $1750 (100)	NA[5]	1 kW/module; 3 kW/5.25 in.	Yes	Modules: 5.22×5.3×18.1	1 to 5	88 to 264V 47 to 63 Hz
	BCE Series	1984	$4000 (100)	NA[5]	3450W	Yes	6.75×8.25×15.88	1	103 to 264V 47 to 63 Hz 1 phase
Unipower	F Series	4/90	$808 (1 output) $920 (multiple output) (100)	$158	1.5 kW	Yes	4×5×12	1 to 7	90 to 132 V 180 to 264V autoranging 47 to 63 Hz

Notes: NS=Not specified.

[1]Power-factor correction is sometimes abbreviated as PFC.

[2]The figure in parentheses indicates the approximate quantity at which the price applies. "OEM qty" refers to large quantities that, for competitive reasons, the vendor does not wish to describe completely. Prices shown include the added cost for PFC.

[3]At quantity indicated in the Price column (compared with vendor's closest equivalent supply without PFC).

[4]At full load and maximum line voltage.

[5]PFC not available as an add-on option.

Minimum[4] Efficiency (%)	Power factor	Comments
65%	0.9	MIL spec; 47 to 440 Hz.
80% typ	0.95 3 phase	
70%	Not specified	Auto switching between input-voltage ranges.
70 to 80% Depends on output voltage	0.99	5W/in.[3]; modular construction allows quick delivery of custom units.
98%	0.98 (50% load)	Stands between ac line and supply that lacks PFC.
70%	0.99	Can directly replace supplies lacking PFC.
70%	0.99	
70%	0.998	Supplies 1 kW while drawing 12A at 115V.
70%	0.998	Meets IEC 555-2.
80% typ	0.92 typ	Meets FCC class A EMI requirements.[7]
80%	0.95	Meets VDE 0871 level B.
72 to 73%	0.99	
65%	0.99 (low line)	All outputs battery-backed by external 48V battery.
70%	0.99	Meets IEC 555-2 and VDE 0871 level A.
77% typ	0.95	Meets UL1950(D3); meets VDE 0871 level A at 230V.
90%	0.7 0.9 0.9	Meets VDE 0871 level B; for mobile use in high RF environment.
85%	0.99	Output ranges: 0 to 8V to 0 to 600V.
75%	0.99	Takes less than half 5×8×11 unit's volume.
72% (5V) 80% (higher voltage)	0.95	Modular system for 19-in.-rack mounting; "hot" switching with isolation diodes.
83 to 87%	0.95	Options include battery charger and military components.
70 to 80% (Depends on outputs)	0.98	Designed to meet IEC 555-2; meets UL1950, CSA22.2 number 220, TUV/IEC 950 and VDE0806.

[6]PFC is offered in custom products. Price depends on requirements.
[7]EMI stands for electromagnetic interference.
[8]Depth depends on power and number of outputs.
[9]Width depends on power and number of outputs.
[10]Unit without fan needs user-supplied air. Size: 8×10.5×3.38 in.

twice line frequency, as does an inductor that follows a full-wave rectifier in a single-phase system) must often be larger than transformers that handle the same amount of power at the same frequency. Although the inductors usually have only one winding, whereas transformers, except for autotransformers, have two or more, the inductor windings must carry dc, which tends to saturate the inductor cores. To prevent saturation, the cores often include air gaps. Even though air gaps help to stabilize a choke's inductance, they lower its inductance and frequently necessitate the use of larger cores.

Correcting an off-line switching supply's power factor by using inductors in its input filter is called passive power-factor correction. Power-factor-correction (PFC) schemes that use active circuits can overcome many of the drawbacks of passive PFC. Within the last two years or so, semiconductor vendors have introduced ICs that make possible power factors very close to 1 (**Table 1**). Although PFC circuits based on special-purpose ICs are more complex than those based on passive approaches, they require the addition of fewer components than were used by earlier discrete active PFC circuits.

Moreover, some active PFC techniques improve more than just power factor. For example, some PFC circuits furnish a supply with an input voltage that, regardless of the line voltage, always corresponds to the high end of the supply's input range. As a result, the supply's holdup time—its ability to "ride through" brown outs or short-duration outages—increases. The energy stored in a capacitor (in this case, the input filter) is proportional to the square of the voltage across the capacitor, so a 30% increase in voltage yields a nearly 70% increase in holdup time. Such an increase is quite significant. Because PFC circuits can attenuate input-voltage fluctuations, incorporating PFC can improve a supply's line regulation. But as should already be clear, including PFC does raise a supply's cost.

Active correction uses preregulator

The basic technique used by most active PFC schemes is to precede the supply with a high-frequency switching preregulator that, over the course of an ac-line cycle, draws current from the line approximately in inverse proportion to the instantaneous line voltage. If the preregulator operates at 100 kHz, it completes 833 switching cycles in ½ cycle of a 60-Hz line.

Near the line-voltage zero crossing, the preregulator draws line current most of the time. As the instantaneous voltage increases, the percentage of time that the preregulator draws current decreases. The result is a

You don't calculate the rms input current by dividing the supply's output power by its efficiency and dividing the quotient by the rms input voltage.

current waveform that, when filtered, nearly mimics the line-voltage waveshape. If the current and voltage waveforms are exactly alike and coincide in phase, the power factor will equal 1. In practice, vendors readily achieve power factors of 0.95. Some companies claim that their supplies exhibit power factors greater than 0.99.

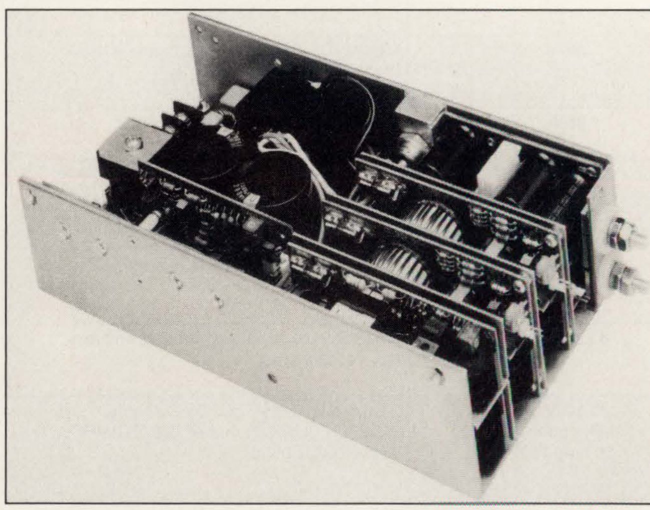
Power-factor-correcting switching preregulators use inductors to store energy. But like the magnetic components in switching power supplies themselves, these inductors operate at high frequencies. Therefore, they can be smaller, lighter, and less expensive than magnetic components that operate at line frequencies. Furthermore, a preregulator can act as an ac-to-dc converter, subsuming the functions of a conventional rectifier and filter and furnishing the high-voltage dc that switching supplies use internally. Combining the PFC and ac-to-dc-conversion functions in a single circuit eliminates some redundancy and thereby reduces the incremental cost of power-factor correction.

Adding the PFC function usually exacts a small penalty in a supply's efficiency. Where a vendor furnishes both power-factor-corrected and uncorrected versions of a supply, it might specify typical efficiencies of, say, 70% for the PFC version and 72% for the uncorrected version. Such a decrease in efficiency is equivalent to a 7% increase in the supply's internal power dissipation and temperature rise. That increase, however, has a minimal effect on the line current the supply draws, especially when you compare the size of the increase to the large decrease brought about by PFC.

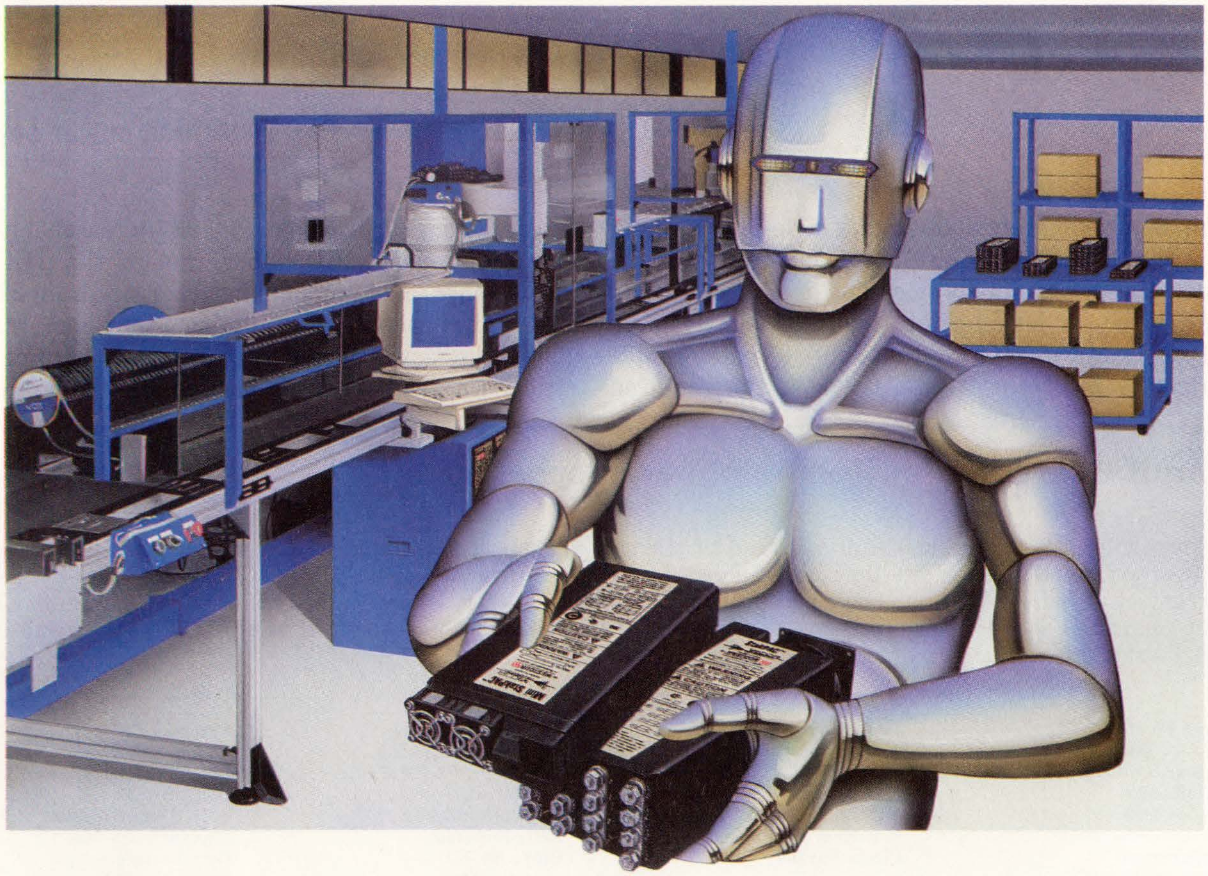
"But," you say, "I don't design equipment that draws kilowatts, and I certainly don't design equipment that uses 3-phase power. So I don't have to concern myself with power-factor correction." You may be surprised to discover that PFC is likely to affect you anyhow. If you design equipment that operates from 220V ac lines and will be sold in Europe beginning in 1992, it will probably have to conform to IEC 555-2. IEC 555-2 imposes limits on line-current waveshapes and harmonic content that will require many products that use off-line switching power supplies to incorporate PFC. As for your product not using 3-phase power, remember that in most factory and office buildings the single-phase ac lines are derived from 3-phase service.

"OK," you concede, "but what of it? I can just go to my power-supply vendor and get him to substitute a PFC supply for one that lacks the feature." In many cases, you may indeed be able to do just that. But, at present, the number of situations where that approach won't work probably exceeds the number where it will. In some cases, you will be able to obtain an accessory PFC module that you can place between the incoming ac line and your existing power supply or supplies. You may even be able to selectively install the PFC module—for example, only on units going to Europe. Nevertheless, blindly applying PFC, even on a fraction of the units you produce, can unnecessarily increase the cost of your product. You'd be better off understanding when you really need PFC and designing it in intelligently.

IEC 555-2 defines four classes of equipment, A through D. Electronic equipment falls into classes A and D. Class A equipment requires 3-phase ac service. The majority of electronic products use single-phase power and hence fall in class D. Class D distinguishes between equipment that consumes less than 300W of ac power and equipment that uses 300W or more. In the less than 300W category, permissible harmonic currents are proportional to the equipment's power level. And at more than 300W, the limits become absolute; they permit the equipment to draw a number of amperes that depends on the harmonic number but is independent of the power consumed. By writing the specification in this manner, the IEC essentially forced higher power-factor requirements on equipment that uses higher levels of power.



Specifying a PFC supply doesn't mean you necessarily have to choose a look-alike product. Deltron's Moduflex series uses modular construction to accomplish twin objectives: The power density is very high—as high as 5W/in.^{3}—and the firm quotes rapid delivery on custom multiple-output units.



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STAKPAC STANDARDS 1200 WATT MODELS

Model	Output Voltage (VDC) and Maximum Current (amperes) per Channel #1	#2	#3	#4	#5
Single Output					
SP1-1801	2 @ 240				
SP1-1802	5 @ 240				
SP1-1603	12 @ 100				
SP1-1604	15 @ 80				
SP1-1605	24 @ 50				
SP1-1606	28 @ 42				
SP1-1607	48 @ 25				
Dual Output					
SP2-1801	2 @ 120	5 @ 120			
SP2-1802	5 @ 120	5 @ 120			
SP2-1803	5 @ 120	12 @ 66			
SP2-1804	12 @ 66	12 @ 66			
SP2-1805	15 @ 53	15 @ 53			
Triple Output					
SP3-1801	5 @ 180	12 @ 16	12 @ 16		
SP3-1802	5 @ 150	12 @ 33	12 @ 16		
SP3-1803	5 @ 180	15 @ 13	15 @ 13		
SP3-1804	5 @ 150	15 @ 26	15 @ 13		
Quad Output					
SP4-1801	5 @ 150	12 @ 16	12 @ 16	5 @ 30	
SP4-1802	5 @ 150	15 @ 13	15 @ 13	5 @ 30	
SP4-1803	5 @ 150	12 @ 16	12 @ 16	24 @ 8	
SP4-1804	5 @ 150	15 @ 13	15 @ 13	24 @ 8	
Five Output					
SP5-1801	5 @ 120	12 @ 16	12 @ 16	5 @ 30	24 @ 8
SP5-1802	5 @ 120	15 @ 13	15 @ 13	5 @ 30	24 @ 8
Seven Output					
SP7-1801	5 @ 60	12 @ 16	12 @ 16	24 @ 8	24 @ 8
	#6	#7			
	5.2 @ 28	2 @ 30			

Total output power may not exceed 1200* watts for any model, single or multiple output. Lower power StakPAC models and many other configurations are available.
*Standard models supply 1100 watts; high-powered version 1200 watts. Please contact the factory.

MINI STAKPAC STANDARDS 600 WATT MODELS

Model	Output Voltage (VDC) and Maximum Current (amperes) per Channel #1	#2	#3	#4	#5
Single Output					
ST1-1401	2 @ 120				
ST1-1402	5 @ 120				
ST1-1301	12 @ 50				
ST1-1302	15 @ 40				
ST1-1303	24 @ 25				
ST1-1304	28 @ 21				
ST1-1305	48 @ 13				
Dual Output					
ST2-1401	2 @ 60	5 @ 60			
ST2-1402	5 @ 60	5 @ 60			
ST2-1403	5 @ 60	12 @ 33			
ST2-1404	12 @ 33	12 @ 33			
ST2-1405	15 @ 26	15 @ 26			
Triple Output					
ST3-1401	5 @ 60	12 @ 16	12 @ 16		
ST3-1402	5 @ 60	15 @ 13	15 @ 13		
ST3-1501	5 @ 90	12 @ 8	12 @ 8		
Quad Output					
ST4-1401	5 @ 30	12 @ 16	12 @ 16	5 @ 30	
ST4-1402	5 @ 30	15 @ 13	15 @ 13	5 @ 30	
ST4-1403	5 @ 30	12 @ 16	12 @ 16	24 @ 8	
ST4-1501	5 @ 30	15 @ 13	15 @ 13	24 @ 8	
ST4-1502	5 @ 60	12 @ 16	12 @ 8	5 @ 15	
ST4-1503	5 @ 60	15 @ 13	15 @ 7	5 @ 15	
ST4-1504	5 @ 60	12 @ 16	12 @ 8	24 @ 4	
ST4-1505	5 @ 60	15 @ 13	15 @ 7	24 @ 4	
Five Output					
ST5-1501	5 @ 30	12 @ 16	12 @ 16	5 @ 15	24 @ 4
ST5-1502	5 @ 30	15 @ 13	15 @ 13	5 @ 15	24 @ 4

Total output power may not exceed 600 watts for any model, single or multiple output. Lower power Mini StakPAC models and many other configurations are available. Please contact the factory.

For ordering information call Vicor Express at 1-800-735-6200 or (508) 470-2900 at ext. 265.

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Below approximately 350 watts, single-phase equipment will not usually require power-factor correction, provided the power supply does not exhibit especially high efficiency or long holdup time. At slightly more than 1 kW, passive PFC will probably no longer enable a product to meet the spec. At 2 kW, the required power factor is approximately 0.98—a reasonably stringent requirement. Remember, though, that IEC 555-2 applies only to equipment that operates from 220V. If you apply its limits to equipment that operates from 120V, the power-factor requirements become more stringent. There is no indication, however, that the

Manufacturers of switching power supplies with PFC

For more information on power-factor-corrected switching power supplies such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN. Some companies have provided the name of a person to contact should you need more information than you find in their literature.

Abbott Electronics
2727 La Cienega Blvd
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(213) 202-8820
(213) 936-8185
FAX (213) 939-1995
Hamid Emami
FAX (213) 836-1027
Circle No. 650

Astec America
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Oceanside, CA 92054
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FAX (619) 439-4243
Ron Sutton
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Cherokee International
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Tustin, CA 92680
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FAX (714) 838-4742
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Computer Products/ Power Conversion
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in PA, (215) 699-9261
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Circle No. 654

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Some PFC circuits furnish a supply with an input voltage that, regardless of the line voltage, always corresponds to the high end of the supply's input range.

IEC intends these limits to apply to 120V equipment. **Table 2** shows the IEC 555-2 Class D current limits as a function of harmonic number.

Given the information in the paragraph above, it is not surprising that most of the power supplies listed in **Table 1** are units that produce 500W or more. Note that the power figures given in **Table 1** are supply output powers; to obtain the input power (**Table 2** refers to input power), divide the output power by the efficiency. Remember, too, that if you draw less than a supply's full-rated power, its efficiency will be less than the value shown in **Table 1**. With no load, all supplies have zero efficiency!

Yet another fact to bear in mind is that, without PFC, as a supply's load decreases, so does its power factor. (Long holdup times indicate low power factors; lightly loaded supplies can have very long holdup times. Suppose you choose a supply that, at full load, requires PFC to meet IEC 555-2, but you never operate the supply at more than 50% of full load—a conservative practice that can greatly increase the supply's reliability. From this discussion, you can probably conclude that the supply should still incorporate PFC.

Universal operation can be a PFC bonus

Many of the listed supplies have so-called universal input ranges. That is, you can vary the input voltage from, say, 90 to 264V without resetting any switches or changing any jumpers. Moreover, the supply vendors often indicate that you can protect the supply over this entire range with a fuse or circuit breaker of a single rating. In some cases, this universal operation is a direct consequence of PFC. As noted earlier, the preregulators in some PFC supplies produce a constant, high-output voltage over a wide input-voltage range.

For products that you will ship to customers in Europe and Asia as well as in North America, such universal operation can greatly simplify configuration, testing, and packaging. Frequently, if your product uses a universal-input supply, the only item you need change as a function of its destination is the power cord. Rather than including a cord appropriate to a specific location, some equipment vendors actually package sets of cords with their products. Other firms have their foreign distributors provide suitable cords when they install the equipment.

Power-factor correction is not for every product. Although most ac-powered products would actually benefit from using PFC supplies, the incremental cost of PFC will prevent the technique from being adopted universally. Nevertheless, under the impetus of IEC 555-2, and with the encouragement of the IC vendors whose chips are simplifying the job of incorporating PFC in power supplies, its use will spread. As PFC's use spreads, its cost will come down. As its cost comes down, its use will spread further. There can be little doubt that PFC is a technique whose importance is destined to grow in the years ahead. **EDN**

Table 2—IEC 555-2 Class D harmonic-current limits

Harmonic order (n)	Equipment that draws less than 300W of ac power: Relative limits (mA/W)	Equipment that draws 300W or more of ac power: Absolute limits (A)
Odd harmonics		
1[1]	4.55	Power/Voltage
3	3.6	1.08
5	2.0	0.60
7	1.5	0.45
9	1.0	0.30
11 through 39	0.6* (11/n)	0.18* (11/n)
Even harmonics		
2	1.0	0.3
4	0.5	0.15

Note: [1]IEC 555-2 does not specify the limits on the fundamental-frequency component of current. The values shown were obtained by dividing the applicable power by the nominal line voltage specified (220V). The equipment would draw a current of this magnitude if the phase angle between the line voltage and the fundamental component were zero.

Acknowledgment

In addition to the power-supply manufacturers, several firms provided assistance in preparing this article: Venture Development Corp, a market-research organization in Natick, MA; and the following manufacturers of PFC ICs: Ixys Corp, San Jose, CA; Micro Linear, San Jose, CA; and Unitrode Integrated Circuits Corp, Merrimack, NH.

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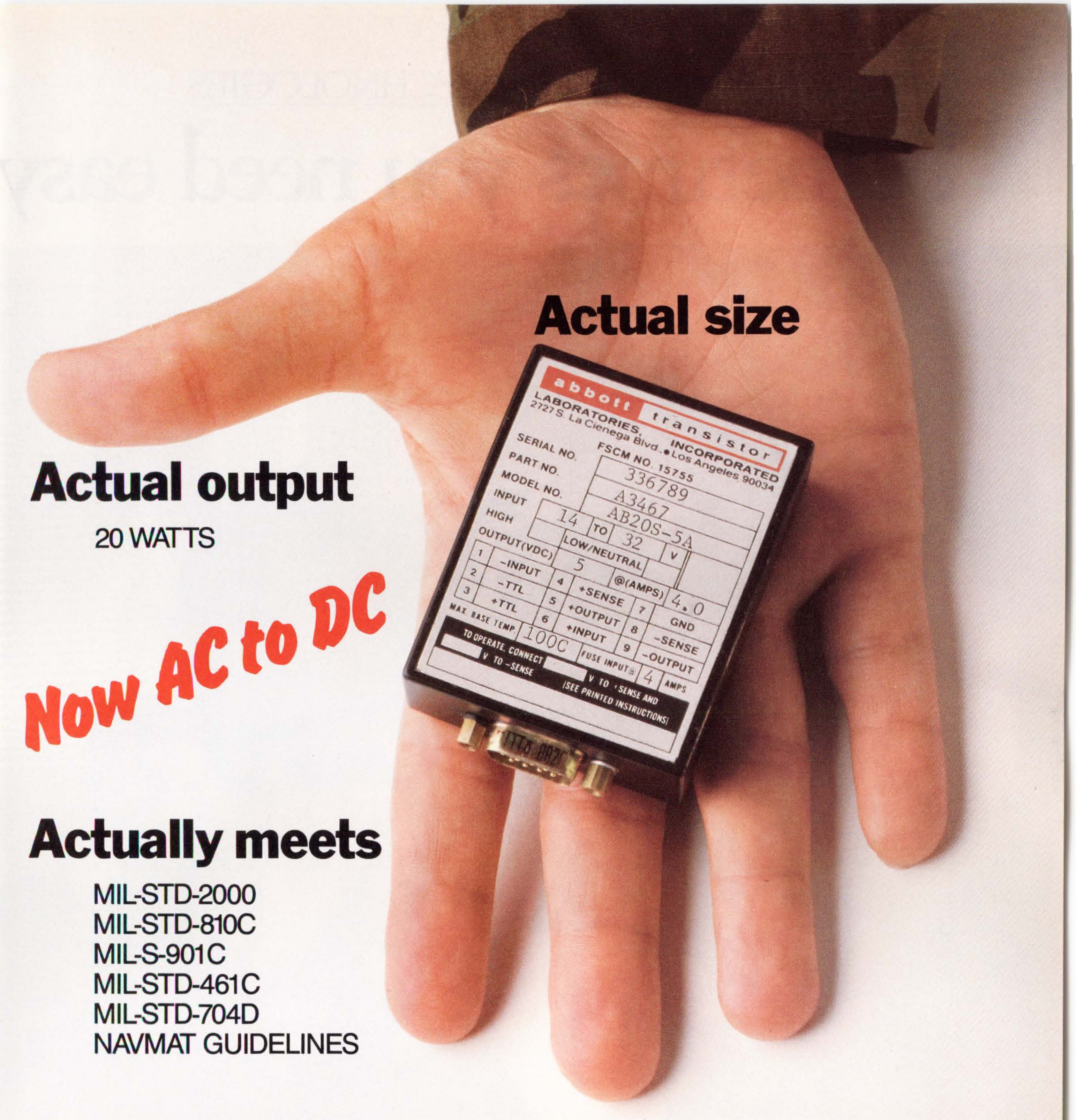

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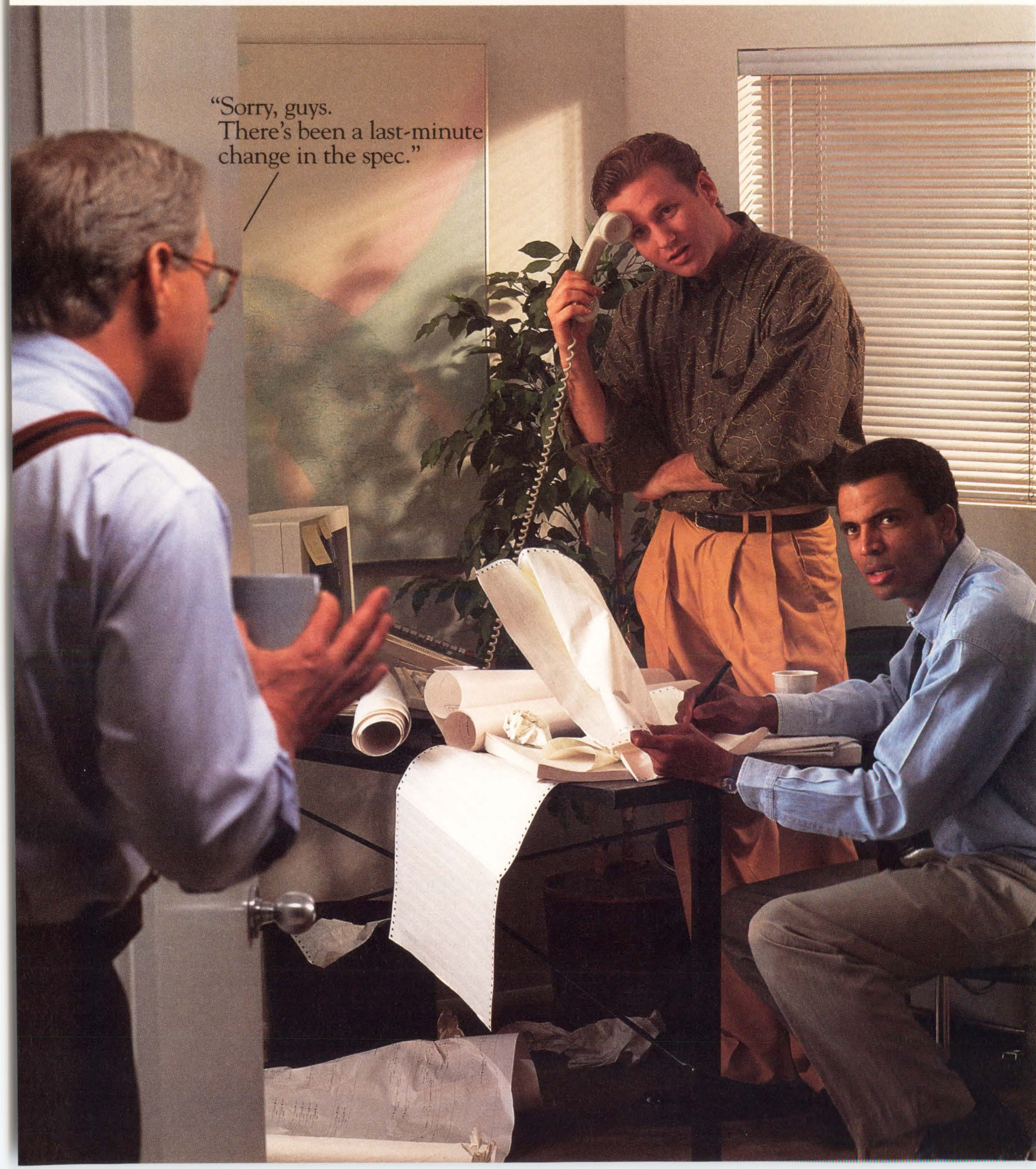

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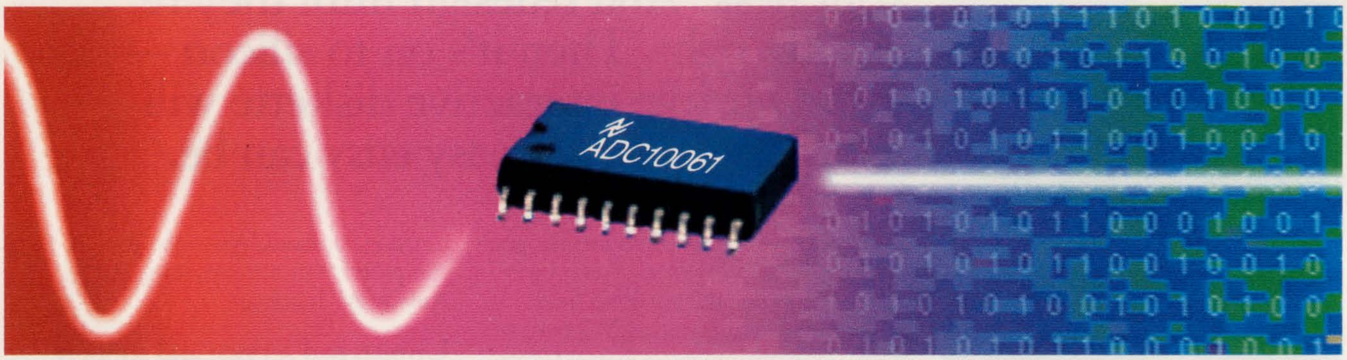

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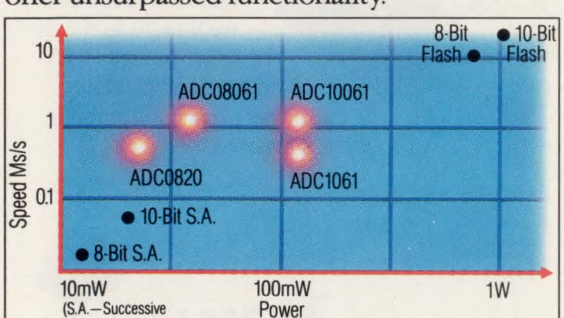

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Electro/ International

No matter what your interests are, Electro/International will provide you with the latest information on new products, technologies, and professional career issues.

John Gallant, Associate Editor

This year it's New York City's turn. The Electro/International show, which alternates between Boston and New York City on successive years, will take place at the Jacob K Javits Convention Center from April 16 through the 18. This year, the East Coast's largest electronic trade show will feature more than 450 companies exhibiting their electronic products. Electro/ International will also offer 43 technical sessions and 11 short courses devoted to keeping the engineer and manager abreast of the current trends in electronic design and manufacturing.

The ceremonies begin at 8:30 am on Tuesday, April 16, when Congressman Don Ritter (R-PA) will deliver the keynote address on "Meeting the Challenges of the 21st Century." The Congressman will discuss how government and industry strategies, along with intense international competition, have made many electronic business sectors unprofitable for American companies. He will also discuss how high-resolution imaging systems in general, and HDTV (high-definition television) in particular, can reverse this trend and revive US consumer electronics. All Electro/International registrants may attend the address at no extra charge.

In keeping with the theme of the keynote address, a number of the sessions deal with the issue of competition in today's tightening global economy (see **table**). Professionals from different parts of the world describe global marketing and communications techniques in Session 5. Session 10 discusses strategies for competing in worldwide markets, especially in Japan, the Pacific Rim, and western Europe. Session 15 gives an overview of the quality-control procedures used in the world today—essential knowledge for selling products across international boundaries. Session 20 deals with global opportunities and how education must be improved here and abroad.

The changing economic structure and the present downturn in job opportunities are topics discussed in Session 43. While companies downsize their technical and engineering staffs, many individuals are becoming certified-professional engineers. If you're considering a career change to consulting, sit in on Session 29, which weighs some of the pros and cons of this career move.

Gladly, not all of the Electro/International sessions focus on the current economic conditions. There will be plenty of old-fashioned technical discussion on emerging technologies as well. Tutorial 3 reviews the

Table 1—Electro/International sessions, tutorials, and short courses

Tuesday April 16, 1991	**Medical electronics**	**Communicatons**	**IC technology**	**IC technology**	**Global electronics business colloquium**	**Short courses**
10:00 am to 12:00 noon	**Tutorial 1** Medical electronics	**Tutorial 2** Lightwave technology: fundamentals and fiber in the loop	**Tutorial 3** Solid-state image sensors	**Session 4** Memory and I/O solutions for today's microcontrollers	**Session 5** International public relations, marketing, and sales promotion for the electronics industry	8:30 am to 11:30 am **(1A)** Advanced design techniques for surface-mount technology—Part I
12:30 pm to 2:30 pm	**Session 6** Medical electronics	**Session 7** Lightwave technology	**Session 8** Integrated micro-engineered sensors and actuators	**Session 9** New innovative specialty memory architectures speed up systems and simplify their design	**Session 10** The global marketing imperative	1:30 pm to 4:30 pm **(1B)** CAD/CAM tooling/manufacturing for surface-mount technology—Part II
3:00 pm to 5:00 pm	**Session 11** Health effects of low-frequency electromagnetic fields	**Session 12** Photonic switching	**Session 13** Programmable logic—the software side	**Session 14** Evolving solid-state memory technology and device architectures promote new cost-effective memory system designs	**Session 15** Quality-profiting in the global marketing	8:30 am to 4:30 pm **(1C)** Surface-mount technology—Parts I and II 8:30 am to 5:00 pm **(2)** Grounding and shielding of electronic systems
Wednesday April 17, 1991	**Manufacturing and test**	**Communications**	**Computers, digital systems, and software**	**Career**	**Global electronics business colloquium**	**Short courses**
9:30 am to 11:30 am	**Session 16** Advances in electronic packaging	**Session 17** New technologies for microwave systems	**Session 18** Cache memories for today's systems	**Session 19** Diversity in the workplace: the emerging majorities	**Session 20** Global opportunities	8:30 am to 12:30 pm **(3A)** The 8086 family of microprocessors: software, hardware, and system applications—Part I
12:30 pm to 2:30 pm	**Session 21** Applications of statistics to manufacturing and design	**Session 22** Commercial applications for microwave technology	**Session 23** New architectures in high-density/high-performance programmable logic devices	**Session 24** Continuing education: a lifetime professional commitment	**Session 25** Canceled	1:30 pm to 5:30 pm **(3B)** 16/32 bit microprocessors: 68000/68010/68020 software, hardware, and design applications—Part II
3:00 pm to 5:00 pm	**Session 26** A case study of computer-integrated manufacturing	**Tutorial 27** Direct digital synthesis	**Tutorial 28** Object-oriented databases: a new enabling technology for electronic design applications	**Session 29** Consulting as a career path for engineers		8:30 am to 5:30 pm **(3C)** 16/32 bit microprocessors—Parts I and II 8:30 am to 12:30 pm **(4)** Talking tech: tips for technical talks
Thursday April 18, 1991	**Manufacturing and test**	**Communications**	**Computers, digital systems, and software**	**Career**	**General**	**Short courses**
9:30 am to 11:30 am	**Session 30** Commercial and industrial ATE	**Session 31** Premises distribution systems	**Session 32** Neural networks	**Session 33** Employing professionals with disabilities: an untapped resource	**Session 34** Public safety communications and transportation	8:30 am to 12:30 pm **(5A)** Intelligent pattern recognition and applications—Part I
12:30 pm to 2:30 pm	**Session 35** New testing protocols for SMT-IEEE boundary scan	**General** **Session 36** Superconductor applications	**Session 37** Artificial neural networks	**Tutorial 38** Giving us the tools: a packaged training program on employing individuals with disabilities	**Session 39** Status of magnetically levitated high-speed transportation in the US today	1:30 pm to 5:30 pm **(5B)** Pattern recognition and image processing—Part II 8:30 am to 5:30 pm **(5C)** Image recognition—Parts I and II
3:00 pm to 5:00 pm	**Session 40** Techniques for automatic testing	**Session 41** OEM sensor technologies for the 90s	**General** **Session 42** Photovoltaic solar cells and systems	**Session 43** Career problems and opportunities	**Session 44** Speech synthesizers and speech-recognition technology: clinical and commercial applications	12:30 pm to 5:00 pm Supplier quality and electronic data interchange

basic concepts and discusses progress in the field of visible and infrared image sensors with an emphasis on VLSI sensors for HDTV. Session 7 presents four papers on new application areas for lightwave technology. High-speed cache design and a look at tomorrow's cache systems are the subjects of Session 18. Session 27 is a tutorial on direct digital synthesizers. You'll learn how to expand synthesizers' bandwidths, and suppress spurious signals.

Sessions 32 and 37 will present papers on neural networks—a topic that always stirs up interest. Session 32 will look into the effectiveness of neural-network models for speech recognition, image processing, and fuzzy logic. The papers presented in Session 37 emphasize why artificial neural networks are among the top three research activities at the Defense Advanced Research Projects Agency (DARPA). Session 44 looks at how speech synthesizers are overcoming the inability of the blind to read text and numbers on a computer screen. The session will review commercially available devices and computer methods for synthesizing understandable speech.

In addition to the professional sessions, Electro/International offers 11 short courses, on the Tuesday and Wednesday show days, covering a variety of topics. A schedule and a brief course outline for the short courses offered appears in the **table** on the right side. The courses are not covered by the registration fee, however. Tuitions range from $200 to $355.

In addition, there will be a 2-part purchasing conference at the Javits Convention Center on Wednesday, April 17, from 12:30 pm to 5:00 pm. In part 1, a distinguished group of panelists will discuss how purchasers can establish a partnership with suppliers to obtain consistent quality. Part 2 will focus on the savings Electronic Data Interchange means to purchasing. There is a $20 registration fee for the conference.

Don't forget to explore the exhibitor's booths on the convention's main floor. The exhibition floor opens at 10:00 am all three days and closes at 6:00 pm on Tuesday, 7:00 pm on Wednesday, and 4:00 pm on Thursday. Whatever your interests, there are plenty of booths to attract your attention. Moreover, there's lots to see and do in New York, and the attractions continue into the late evening hours. As the Broadway tune goes, "New York, New York, it's a hell of a town." EDN

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Finding your way to the show

The Jacob Javits Convention Center is located on 11th Ave between W 34th St and W 39th St—on the west side. It is easily accessible, and both public transportation and a free Electro shuttle bus have stops at the center. The 42nd St crosstown bus (M42) and the 34th St crosstown bus (M34) both serve the Javits Center. These buses run east to west and stop on every block to connect with most north to south bus routes by a free transfer. Fare is $1.15 in coins or tokens. Buses serving the center have Javits Center signs.

The closest subway line to the Javits Center is the 8th Ave IND line (A, E, C, and K trains) at either the 34th St or 42nd St exits. Other convenient subway lines on 34th and 42nd St are 7th Ave IRT (Nos. 1, 2, and 3); Flushing Line IRT (No. 7); 6th Ave IND (B, D, F, and JFK Express); Broadway BMT (N, Q, R); and the Grand Central to Times Square Shuttle (S). Fare is $1.15, and connections to public buses can be made at street level.

If you're trying to get to Electro/International by car, forget it. There is no parking available at the Jacob Javits Center. However, if there are no scheduled baseball games, Electro/International attendees can park and ride from either Yankee Stadium or Shea Stadium. Both parks are adjacent to New York's subway system. You can also park at the Meadowlands Sports Complex No. 13 parking lot. An express bus, No. 322, runs between the parking lot and the downtown Port Authority Bus Terminal. Parking is $2.75, and the trip takes approximately 15 minutes. Round-trip fare is $5.50.

If you're flying into Kennedy or LaGuardia airports, you'll save yourself some cash if you use the Carey bus service to get downtown. The buses run every 30 minutes between 7:15 am and 11:00 pm and connect you with either the downtown Hilton, Marriott Marquis, or the Sheraton City Squire hotels. The service also stops at the downtown Port Authority Bus Terminal, which is on 42nd St between 8th and 9th Ave. The fare is $7.50 from LaGuardia to the bus terminal and $9.50 from Kennedy to the bus terminal. You can catch a crosstown bus from the bus terminal to the Javits Center or your hotel. The Port Authority Trans-Hudson Corp furnishes an alternative way to get to NYC from New Jersey and the Newark Airport. Call (201) 963-2558 for transportation information.

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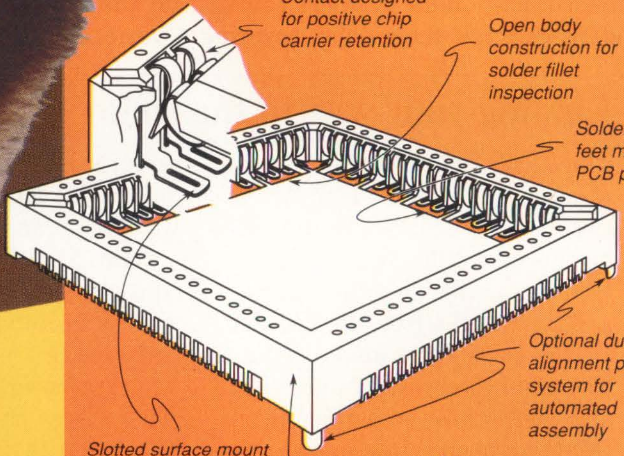

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ACL Inc, 1960 E Devon Ave, Elk Grove Village, IL 60007. Phone (800) 782-8420; in IL, (708) 981-9212. FAX (708) 981-9278. TLX 4330251. Booth No. 2551.
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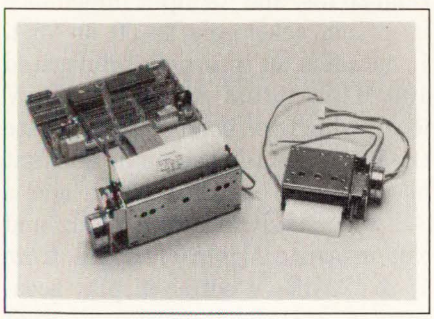

Thermal Printers

The PL2040 and PL4080 are thermal printers and controllers for the OEM designs. The PL2040 has a print width of 20 or 40 columns and accepts a paper width of 60 mm. The PL4080 has a print width of 40 or 80 columns and accepts a paper width of 114 mm. Both units print at a 152-dpi resolution and have horizontal and vertical dot pitches of 0.007 in. The minimum character size is 6×9 dots, which is expandable $15\times$. In addition, the printers can print 12 lines/sec, and they have bar-code-printing software built in. The printers also have bit-image and dot plot modes. PL2040, $301; PL4080, $328 (100).

Telpar Inc, Box 796, Addison, TX 75001. Phone (214) 233-6631. FAX (214) 233-8947. TLX 732561. Booth No. 2226. **Circle No. 352**

Reset-Delay Relay

The C Series is a family of reset-delay relays. The units consist of spst or spdt switches that delay for a fixed or adjustable time before being energized or de-energized after you activate the trigger terminal. You can use the units on a pc board or panel mount to prevent circuit operation for a set period of time. The units consist of solid-state circuitry that drives a relay. Standard units have five male terminals spaced at intervals of 0.11 in. You can also opt for terminals spaced at 0.25-in. intervals or screw terminals. The relays come with preset tie delays of 0.10 to 600 sec. You can also purchase units with screwdriver-adjustable potentiometers that set the time delays between 4 and 165 sec, 150 and 300 sec, or 300 and 600 sec. Contacts have 0.5A ratings at 115V ac. You can specify the input voltage from 5 to 140V ac or 6 to 30V dc. $22.50.

Amperite Co Inc, 600 Palisade Ave, Union City, NJ 07087. Phone (800) 752-2329; in NJ, (201) 864-9503. FAX (201) 864-3955. Booth No. 2452. **Circle No. 353**

Vacuum-Fluorescent Display

The model 3601-30-040 vacuum-fluorescent display shows two lines of 11.3-mm-high characters. Each line can have 20 characters; each character comprises a 5×7 dot matrix. The module measures $10.8 \times 2.75 \times 1.3$ in. It communicates with a host via an RS-232C or an RS-422 port at 1200 or 9600 baud. All characters and control codes are in 7-bit ASCII format. The module comes with a standard ASCII 96-character set and alternate General European, Scandinavian, German, and scientific characters. The characters are flicker free, and you can filter them to achieve a variety of colors. The unit can detect errors in transmission, and a test mode displays all characters. $228 (100).

Industrial Electronic Engineers Inc, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. FAX (818) 902-3723. TLX 4720556. Booth Nos. 2621, 2623.
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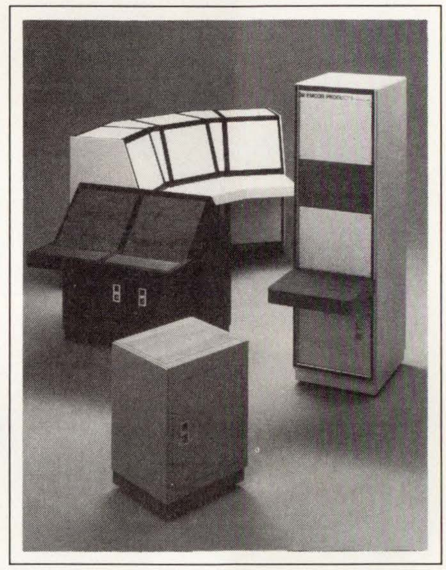

Modular Enclosures

The ESQ family of modular enclosures comes in 19- and 24-in. panel widths and vertical, desk- and counter-height, slope-front, low-silhouette, wedge-unit, turret, or writing-top frames. The enclosures are fabricated from cold-rolled steel, and electronically controlled resistance welders ensure uniform welds. Their construction employs speed nuts and hardened Phillips-head sheet-metal screws for fastening panels. The enclosures come in 16 standard colors, and the company can match your paint chip or any Federal-Standard-595 color using a color-matching computer system. The enclosures have a static load capacity estimated at 800 lbs of equipment evenly distributed in the frame. Desk-top units without accessories, \$252 to \$520.

Emcor Products, 1600 4th Ave NW, Rochester, MN 55901. Phone (507) 289-3371. FAX (507) 287-3405. Booth Nos. 2321, 2323.

Circle No. 355

Sealed Lead-Acid Battery

The Model PS-12120 is a rechargeable, sealed, lead-acid 12V battery. The 5.95×3.86×3.70-in. unit delivers 12.0 Ahrs at a 20-hour rate. This capacity results in an energy density of 1.69 Whrs/in. The maintenance-free battery weighs 8.8 lbs and can deliver as much as 120A of discharge current. You can use the battery in any position, and it has a life expectancy of more than 5 years or 200 to 500 recharges (depending on the average depth of the discharge). The battery operates at temperatures from −20 to +50°C; withstands a vibration of 2000 cycles/minute, having a 0.10-in. excursion for 2 hours; and has a 3-month shelf life with 91% of nominal capacity at 20°C. \$33.80 (500).

Power-Sonic, Box 5242, Redwood City, CA 94063. Phone (415) 364-5001. FAX (415) 366-3662. TLX 348400. Booth No. 2733.

Circle No. 356

Portable Spectrum Analyzer

The model PL 5610 portable spectrum analyzer has a 1-GHz frequency range. It operates from multiple ac line voltages, an external 12 to 15V dc supply, or its internal 12V dc rechargeable battery. The battery operates for approximately 1 hour after being recharged for 2 hours. The analyzer weighs less than 20 lbs, and its input impedance is switch selectable to 50 or 75Ω. It contains an internally generated 100-MHz signal at an 80-dBμV level, which you can use to calibrate the instrument in the field. The unit has a 70-dB dynamic range and a 3-dB IF bandwidth of 10 kHz and can measure signals ranging from 15 to 123 dBμV with a display accuracy of ±2 dB. It uses a 3½-digit LCD display to indicate the center frequency with an accuracy of ±3 MHz. \$2995.

B&K Precision, Maxtec International Corp, 6470 W Cortland St, Chicago, IL 60635. Phone (312) 889-1448. FAX (312) 794-9740. TLX 210017. Booth Nos. 2033, 2035.

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The Model 182 6½-digit digital voltmeter offers a 1-nV sensitivity. The instrument has a special low-tem-

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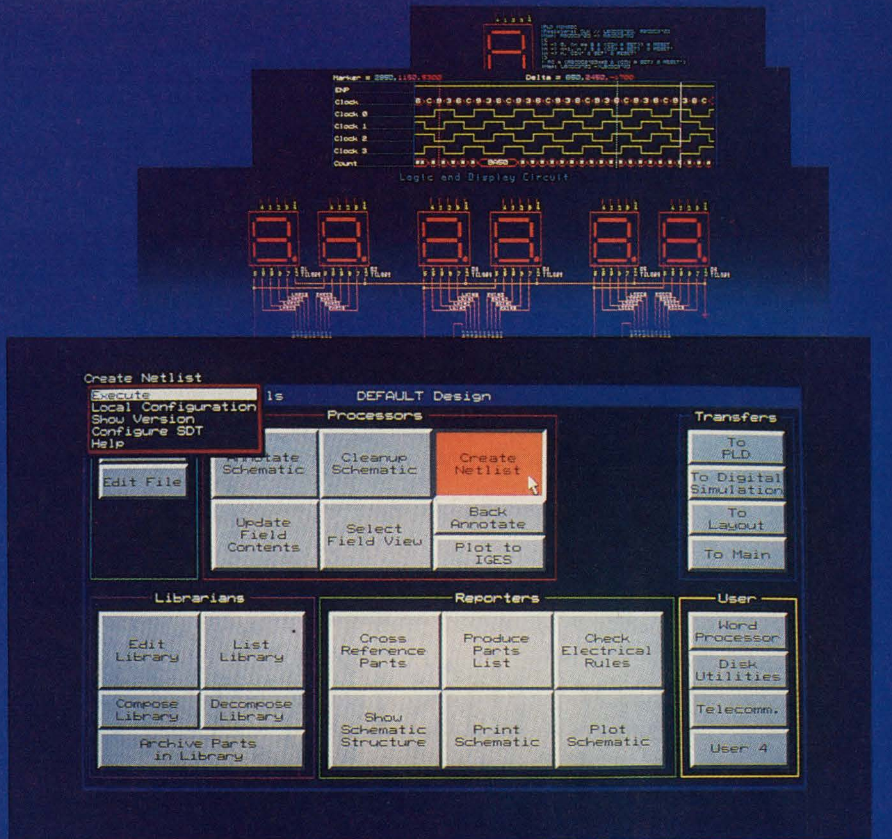

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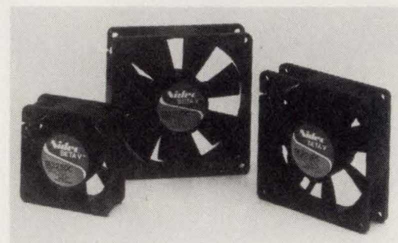
or write to OrCAD Sales Department, 3175 N.W. Aloclek Drive, Hillsboro, Oregon, 97124 perature input connector and cable that reduces noise for low-voltage measurements. The model maintains an input noise level of 15 nV p-p. In addition, the instrument has an input impedance greater than 10 GΩ on all voltage ranges. It has a FET input design that provides 160 dB of common-mode rejection when making differential measurements using both the positive and negative inputs. The unit has analog and digital filters that operate on the data in the unit's buffer memory. The filters reduce noise when transferring data to a host computer via its IEEE-488 bus. The model can also achieve more than 50 readings/sec. You can program the voltmeter via the IEEE-488 bus, and an autoranging function automatically switches between 5 voltage ranges—3 mV, 30 mV, 300 mV, 3V, and 30V. $3695. Delivery is four weeks ARO.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (800) 552-1115; in OH, (216) 248-0400. FAX (216) 248-6168. Booth No. 2040. **Circle No. 358**



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Nidec Corp, 318 Industrial Ln, Torrington, CT 06790. Phone (203) 482-4422, ext 400. FAX (203) 489-7201. Booth Nos. 2315, 2317.

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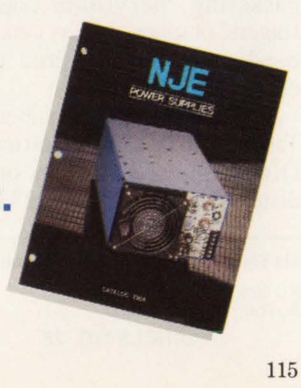

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achieve over 90% coverage using either wave-flow or infrared and vapor-phase-reflow soldering. The series comprises 25 models covering an inductance range from 10.0 to 330.0 μH. The units come in either carrier or reel packaging. $0.41 (1000).

Sprague-Goodman Electronics Inc, 134 Fulton Ave, Garden City Park, NY 11040. Phone (516) 746-1385. FAX (516) 746-1396. TLX 144533. Booth No. 2056.

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Micro-Strip high-speed interconnected connectors maintain a 50-Ω transmission line impedance within a ±10% tolerance. They have contacts on 0.05×0.10-in. centerline spacing and a design that can fit 40 signal lines and their associated ground lines into a linear inch. The receptacle contacts present a flat metal surface that faces the ground plane. An interconnected unit limits crosstalk to less than 4% when signals have rise times of 1 nsec. Board-to-board connectors are available as right-angle and vertical stacking units. Vertical stacking units are available in 0.43- or 0.738-in. stack heights. Cable-to-board connectors are compatible with transmission-line cables that feature precision-controlled mass-soldering terminations. The connector costs $0.15 per mated pair for stacking configurations and approximately $0.21 for right-angle board configurations (OEM qty).

AMP Inc, Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752. Booth No. 2322. **Circle No. 361**

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The 9414 digital oscilloscope captures and analyzes signals having frequencies as high as 150 MHz. Each of the scope's four channels employs a flash A/D converter that can digitize transient events as fast as 100M samples/sec and periodic signals as fast as 4G samples/sec. A ±0.002% timebase simultaneously drives each A/D converter to ensure timing accuracy for measurements between channels. In addition, the scope contains 10k bytes of memory/channel, letting you analyze waveforms by expanding them to 200 times. An optional card reader allows you to store waveforms and setups on 128k- or 256k-byte memory cards. The scope also lets you automatically measure rise time, fall time, RMS voltage, and other signal characteristics using the IEEE-181 pulse-measurement standard. $12,990. Delivery is six weeks ARO.

LeCroy Corp, 700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977. Phone (914) 425-2000. FAX (914) 425-8967. TWX 710-577-2832. Booth Nos. 1934, 1936.

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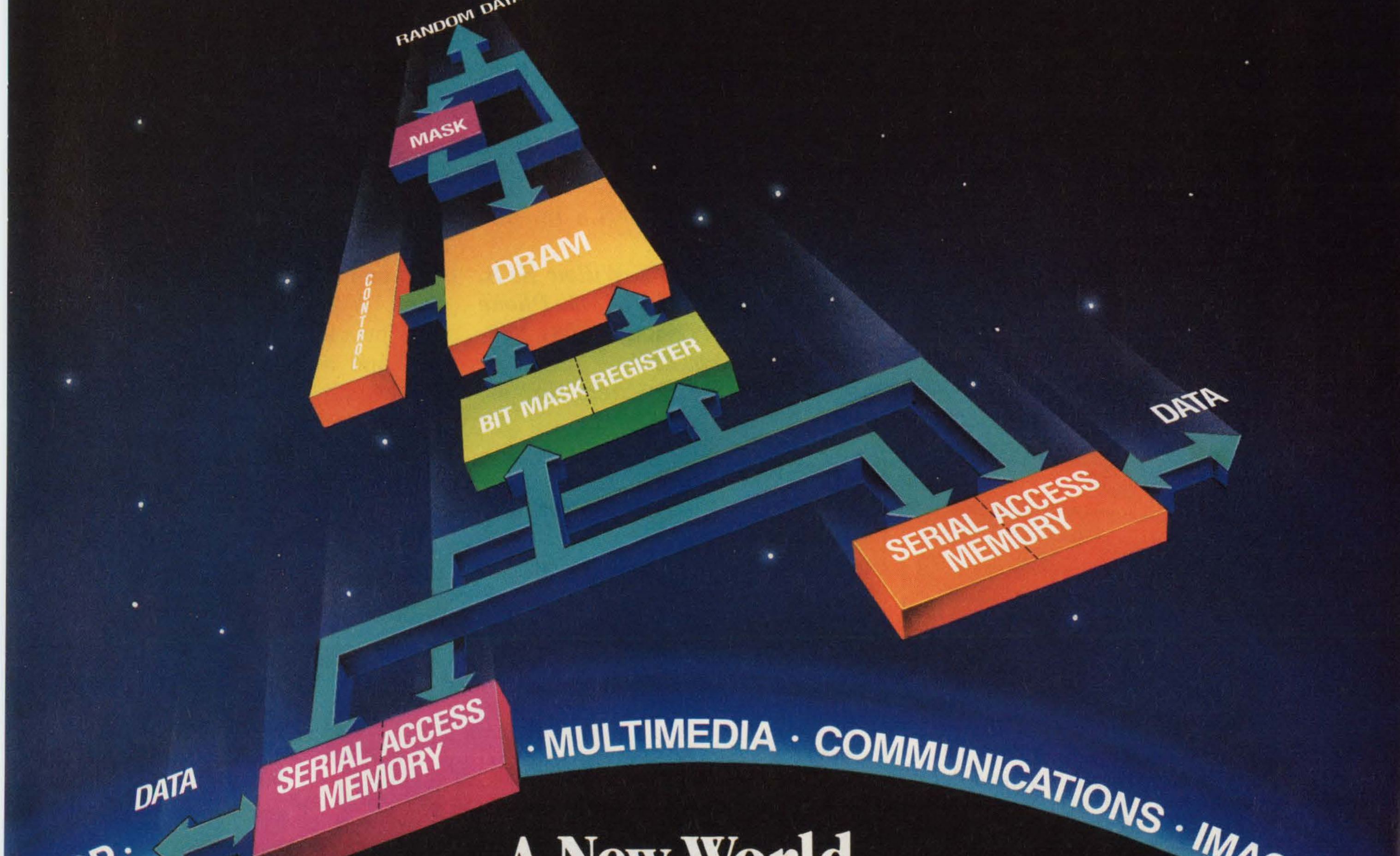
LAN Tester

The Cable Scanner tool for testing LANs operates on Ethernet, Arcnet, StarLAN, Token-Ring, and Twisted-Pair networks. The tool lets you determine if cabling is the cause of a malfunction. If the problem is cabling, the tester helps you pinpoint the location of a fault or break. The tester also provides cable resistance measurements, noise-level measurements, and audible continuity checks. You can attach a line printer to the unit to record activity. After the scanner helps

Triple Port DRAMs



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*Provides SAM stop address input **Call for military availability

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you locate the faulty cable or connection, a tracer lets you know the cable's exact location in the ceiling or wall. The tracer locates the fault by detecting a signal injected into the cable by the main unit. The unit comes with adapters for Ethernet, Arcnet, and Twisted-Pair networks; a printer cable; IBM PC-compatible software on floppy disk; and six AA NiCd batteries. The unit measures 1×4×7.5 in. and weighs 2 lbs. $1495.

Contact East, 335 Willow St S, North Andover, MA 01845. Phone (508) 682-9844. FAX (508) 688-7829. Booth No. 2221.

Circle No. 363

68332 Emulator

The HMI-200 emulator for Motorola's 68332 µP provides real-time emulation; four complex break and trigger points; and two 4k×104-bit trace buffers, which include 16 external trace bits and 32 bits of time-tag data. It has a standard 256k bytes of memory and an option for 1, 2, or 4M bytes. The emulator comes with a window-driven high-level-language debugger called Sourcegate. The debugger supports C, Pascal, PL/M, and Ada compilers. Sourcegate displays source code only, assembly code only, or source and assembly code. You can display windows to monitor specified memory locations and variables. A performance analysis option provides real-time software test and analysis. Emulator and Sourcegate, $16,000; performance analysis option, $2500.

Huntsville Microsystems Inc, 3322 S Memorial Pkwy, Huntsville, AL 35801. Phone (205) 881-6005. FAX (205) 882-6701. TWX 510-600-8258. Booth No. 2755.

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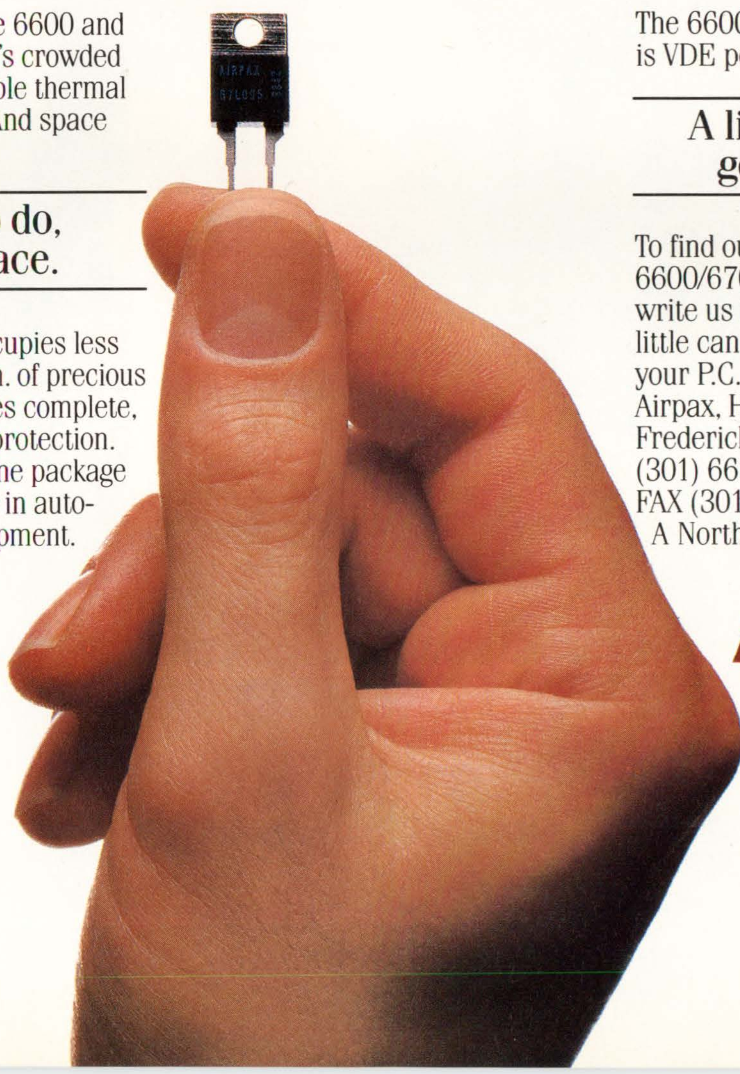
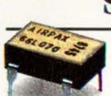


So much to do, so little space.



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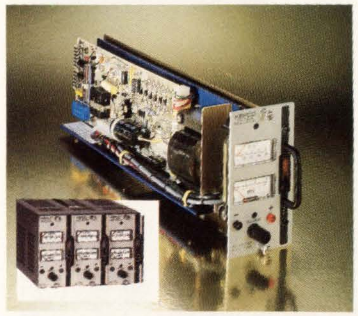

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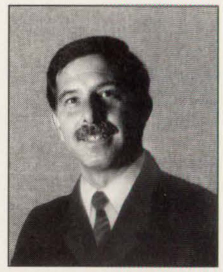

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EDN DESIGNERS' GUIDE TO

servo simulation using PSpice part 2

Servo analysis gets a boost from parametric models

Part 2 of this 2-part series describes how to use the basic mechanical models presented in part 1 to create more complex mechanical subsystems, such as rotational loads, gear trains, and dc motors. Combining these models with standard electrical circuit models allows you to analyze the dc, ac, and transient response of an entire servo-control system.

Dr Vincent G Bello, *Norden Systems*

Modeling and then interconnecting important subsystems simplifies the analysis of complex electromechanical servo systems. With a library of mechanical and electrical subcircuits at your disposal, you can easily simulate a servo system comprising any number of nested subcircuits. You can simulate each block or subcircuit by itself and compare the model's accuracy to measurements or data-sheet specifications. For designers of electromechanical systems, mechanical models are an important part of that library. The following sections present PSpice models for main mechanical subsystems such as rotational loads, gear trains, and dc motors.

The first of these subcircuit models is a rotational load (**Fig 1**). This model includes elements for moment of inertia, viscous damping, coulomb friction, shaft stiffness, and mass unbalance. A constant torque approximates the mass unbalance, which is a valid approximation if the shaft-angle variations are small. **Listing 1** gives the code for the subcircuit named ROTLD. The equivalent circuit and code follow directly from the analogous circuits for simple mechanical elements developed in part 1.

The first line of **Listing 1** assigns negligible default values to the parameters the **listing** defines as J, B, KS, BKS, FC, and MU. The program uses these defaults if the main circuit's sub circuit call statement doesn't assign alternate values. The external nodes are node 1—the shaft speed in rad/sec relative to space—and node 2—the platform

The software listings in this article are available on EDN's computer bulletin board system (BBS). Phone (617) 558-4241 with modem settings 300/1200/2400,8,N,1. Access */freeware* SIG and specify *(r)ead* option followed by *(k)eyword* search for "MS #181".

In some gear trains, backlash is an important parameter. If the amount of backlash is too large, the servo system can oscillate.

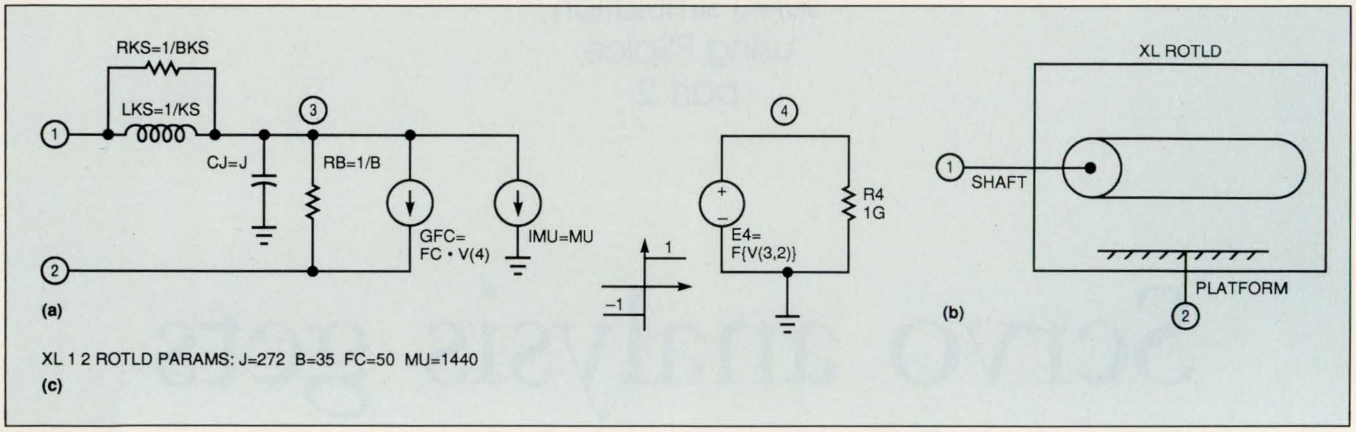

***Fig 1—This equivalent circuit for a rotational load (a) includes** elements that simulate moment of inertia, viscous damping, coulomb friction, stiffness, and mass unbalance, whose values you define in the subcircuit call statement (**c**). The subcircuit block has two external connections, as **b** shows.*

speed in rad/sec relative to space. Note that the torque delivered to the shaft will not equal the torque returned to the platform because the returns from the moment of inertia and mass unbalance connect directly to space or ground. The platform connection allows an independent platform velocity input. You might need to use such an input in the case of an airborne application in which the airframe can undergo rapid velocity changes.

This rotational-load model contains coulomb friction, so be sure to set this parameter to zero for ac small-signal analysis, or bias the solution away from the transition regions. Part 1 discussed the potential problems that can occur at these regions.

Gear train meets its electrical match

The gear train is another mechanical subsystem and is analogous to an electrical transformer (**Ref 1**). The output torque or current is equal to the input torque times the gear ratio. The output shaft velocity or voltage is equal to the input shaft velocity divided by the gear ratio. For an ideal gear train or transformer, the output power equals the input power. **Fig 2**'s equivalent circuit of a gear train includes input and output inertia, friction, and stiffness. The sources EB1 and GT2 model the ideal portion of the gear. Source VT1 is used to measure the input torque. The remaining elements model inertia, friction, and stiffness of the input and output gears. The parameters N1 and N2 are the number of teeth on the input and output gears, respectively, and define the gear ratio, N, which equals N2/N1.

Listing 2 gives the code for the gear-train subcircuit named GEAR. The comments at the beginning of the code define the parameters. The external nodes 1 to 4 define the connection of the gear train to the system. There are two independent platform connections, nodes 2 and 4, allowing for movement between an input platform and an output platform. Generally, you would tie these together to a single platform.

The gear-train model is linear except for the two coulomb-friction parameters, F1 and F2. For ac small-signal analysis, set $F1 = F2 = 0$ (the default values), or bias the solution away from the transition region.

The previous gear-train model ignores backlash. However, in some gear trains, backlash is an important parameter. If the amount of backlash is too large, the servo system can oscillate (**Ref 2**). Backlash occurs when the input and output gears do not mesh, which stops the transmission of power.

Listing 1—PSpice code for simple rotational load

```
.SUBCKT ROTLD 1 2 PARAMS:J=1P B=1N KS=1G BKS=1N FC=0 MU=0
* ROTATIONAL LOAD MODEL INCLUDING INERTIA, VISCOUS FRICTION,
* SHAFT SPRING CONSTANT, COULOMB FRICTION, AND MASS UNBALANCE
* NODE 1 IS SHAFT SPEED IN RAD/SEC RELATIVE TO SPACE
* NODE 2 IS PLATFORM SPEED IN RAD/SEC RELATIVE TO SPACE
* NODE 0 IS SPACE REFERENCE
* CURRENT INTO NODE 1 IS TORQUE DELIVERED IN OZ-IN
* UNITS : OZ,IN,RAD/SEC
* J IS INERTIA OF LOAD IN OZ-IN-SEC/RAD/SEC
* B IS VISCOUS FRICTION OF LOAD IN OZ-IN/RAD/SEC
* KS IS SHAFT SPRING CONSTANT IN OZ-IN/RAD
* BKS IS SHAFT SPRING DAMPING IN OZ-IN/RAD/SEC
* FC IS COULOMB FRICTION IN OZ-IN
* MU IS MASS UNBALANCE IN OZ-IN
LKS 1 3 {1/KS}
RKS 1 3 {1/BKS}
CJ 3 0 {J}
RB 3 2 {1/B}
* CIRCUIT TO MODEL COULOMB FRICTION
E4 4 0 TABLE {V(3,2)} = (-.1M,-1) (.1M,1)
R4 4 0 1G
GFC 3 2 VALUE = {FC*V(4)}
* CONSTANT MASS UNBALANCE
IMU 3 0 {MU}
.ENDS ROTLD
```

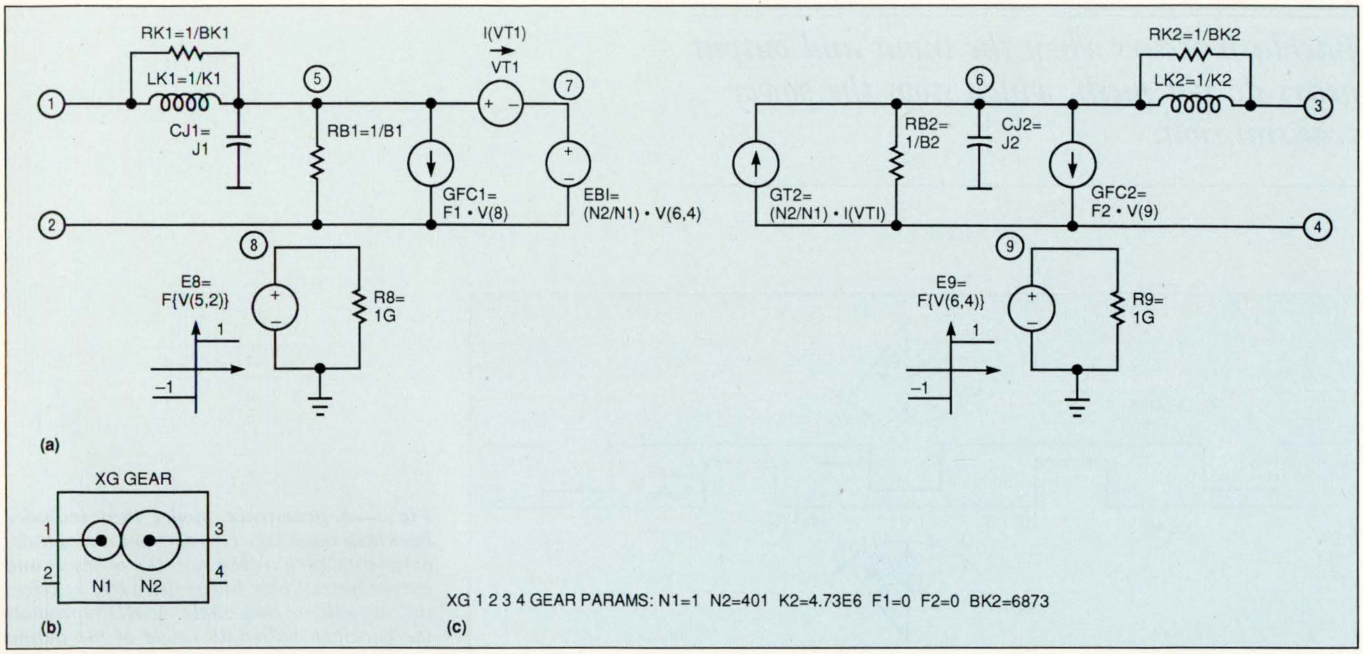

***Fig 2—The sources EB1 and GT2 of this gear train's equivalent circuit (a) simulate** ideal characteristics. Other elements model inertia, friction, and stiffness of the input and output gears. The subcircuit symbol (**b**) displays the four external connections. The parameters N1 and N2 in the corresponding call statement (**c**) define the gear ratio.*

To derive the equations for backlash, first define the following variables for **Fig 3**:

ω_1 = input-gear speed in rad/sec
θ_1 = input-gear angle in radians
N_1 = number of input-gear teeth
R_1 = input-gear radius
v_1 = input-gear linear velocity
x_1 = input-gear linear distance
ω_2 = output-gear speed in rad/sec
θ_2 = output-gear angle in radians
N_2 = number of output-gear teeth
R_2 = output-gear radius
v_2 = output-gear linear velocity
x_2 = output-gear linear distance
N = the gear ratio, N_2/N_1
HD = backlash halfwidth angle at output gear in radians.

When the two gears are in contact, the tangential velocities, v_1 and v_2, are equal. Thus,

$$\omega_1 R_1 = \omega_2 R_2.$$

Because $R_2 = NR_1$, it follows that

$$\omega_1 = N\omega_2.$$

In order for the two gears to contact, the linear distance traveled by the first gear relative to the second gear starting from the center position must be

$$x_1 - x_2 = HD \cdot R_2.$$

Dividing this entire equation by R_1, substituting NR_1

Listing 2—PSpice code for gear train

```
.SUBCKT GEAR 1 2 3 4 PARAMS: N1=1 J1=1P B1=1P F1=0 K1=1G BK1=1N
+                            N2=1 J2=1P B2=1P F2=0 K2=1G BK2=1N
* NODE 1 IS INPUT SHAFT SPEED IN RAD/SEC RELATIVE TO SPACE
* NODE 2 IS INPUT PLATFORM SHAFT SPEED IN RAD/SEC RELATIVE TO SPACE
* NODE 3 IS OUTPUT SHAFT SPEED IN RAD/SEC RELATIVE TO SPACE
* NODE 4 IS OUTPUT PLATFORM SHAFT SPEED IN RAD/SEC RELATIVE TO SPACE
* NODE 0 IS SPACE REFERENCE
* CURRENT INTO NODE 1 IS TORQUE DELIVERED IN OZ-IN
* CURRENT OUT OF NODE 3 IS TORQUE DELIVERED IN OZ-IN
* UNITS: OZ,IN,RAD/SEC
* N1 IS NUMBER OF TEETH ON INPUT GEAR
* J1 IS INPUT GEAR INERTIA IN OZ-IN-SEC/RAD/SEC
* B1 IS INPUT GEAR VISCOUS FRICTION IN OZ-IN/RAD/SEC
* F1 IS INPUT GEAR COULOMB FRICTION IN OZ-IN
* K1 IS INPUT GEAR SHAFT SPRING CONSTANT IN OZ-IN/RAD
* BK1 IS INPUT GEAR SHAFT DAMPING IN OZ-IN/RAD/SEC
* N2 IS NUMBER OF TEETH ON OUTPUT GEAR
* J2 IS OUTPUT GEAR INERTIA IN OZ-IN-SEC/RAD/SEC
* B2 IS OUTPUT GEAR VISCOUS FRICTION IN OZ-IN/RAD/SEC
* F2 IS OUTPUT GEAR COULOMB FRICTION IN OZ-IN
* K2 IS OUTPUT GEAR SHAFT SPRING CONSTANT IN OZ-IN/RAD
* BK2 IS OUTPUT GEAR SHAFT DAMPING IN OZ-IN/RAD/SEC
LK1 1 5 (1/K1)
RK1 1 5 (1/BK1)
CJ1 5 0 (J1)
RB1 5 2 (1/B1)
E8 8 0 TABLE (V(5,2)) = (-.1M,-1) (.1M,1)
R8 8 0 1G
GFC1 5 2 VALUE = (F1*V(8))
VT1 5 7
EB1 7 2 VALUE = ((N2/N1)*V(6,4))
GT2 4 6 VALUE = ((N2/N1)*I(VT1))
CJ2 6 0 (J2)
RB2 6 4 (1/B2)
E9 9 0 TABLE (V(6,4)) = (-.1M,-1) (.1M,1)
R9 9 0 1G
GFC2 6 4 VALUE = (F2*V(9))
LK2 6 3 (1/K2)
RK2 6 3 (1/BK2)
.ENDS GEAR
```

for R_2, and using small-angle approximations yields the following condition for gear contact in the positive direction:

$$\Theta_1 - N\Theta_2 = N \cdot HD. \tag{1}$$

If contact is to occur in the positive direction, v_1 must be greater than v_2 prior to contact. If, after contact occurs, v_1 falls below v_2, the gears will separate until contact is made in the negative direction when the following condition exists:

$$\Theta_1 - N\Theta_2 = -N \cdot HD. \tag{2}$$

This equation is the condition for gear contact in the

Backlash occurs when the input and output gears do not mesh, which stops the power transmission.

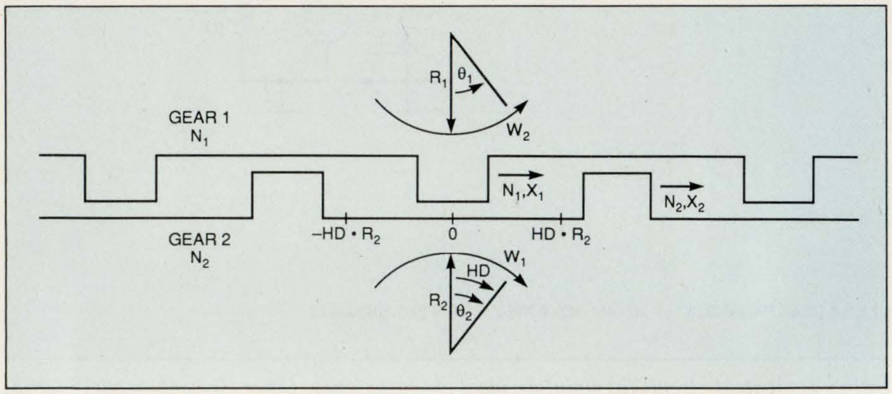

Fig 3—A gear-train model that includes backlash *must take into account many characteristics such as the number of input and output gears; their linear distance, x; velocity, v; radii; x; and angle, θ. HD represents the backlash halfwidth angle at the output gear.*

negative direction. If contact is to occur in the negative direction, v_1 must be less than v_2 just before contact.

By dividing the differential linear velocity Δv, which equals $v_1 - v_2$, by the radius R_1, you can derive the differential angular velocity at the input gear as follows:

$$\Delta\omega_{IN} = \omega_1 - N\omega_2.$$

The differential angle at the input gear is

$$\Delta\Theta_{IN} = \Theta_1 - N\Theta_2 = \int \Delta\omega_{IN} dt.$$

The differential angle at the output gear is

$$\Delta\Theta_{OUT} = \Delta\Theta_{IN}/N.$$

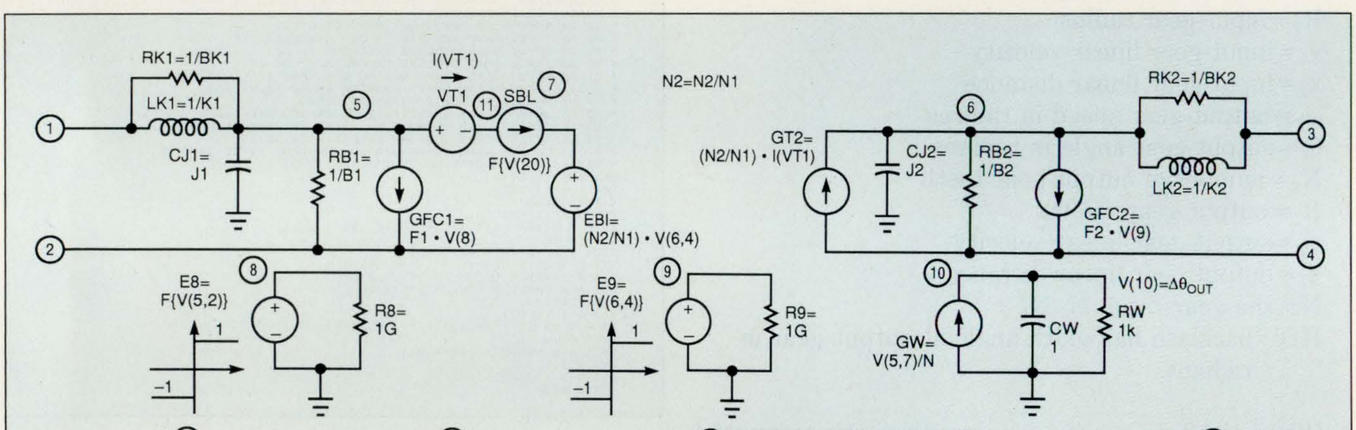

Fig 4—The equivalent circuit for a gear train with backlash (a) includes *a controlled source, SBL, which acts as a switch. SBL is an open circuit when the gears are in backlash and a short when the gears mesh. The subcircuit symbol (**b**) is identical to the gear train without backlash; the call statement in **c** defines backlash parameters such as HD.*

Listing 3—PSpice code for gear train with backlash

```
.SUBCKT GEARBL 1 2 3 4 PARAMS: N1=1 J1=1P B1=1P F1=0 K1=1G BK1=1N
+                              N2=1 J2=1P B2=1P F2=0 K2=1G BK2=1N
+                              HD=1U
* NODE 1 IS INPUT SHAFT SPEED IN RAD/SEC RELATIVE TO SPACE
* NODE 2 IS INPUT PLATFORM SHAFT SPEED IN RAD/SEC RELATIVE TO SPACE
* NODE 3 IS OUTPUT SHAFT SPEED IN RAD/SEC RELATIVE TO SPACE
* NODE 4 IS OUTPUT PLATFORM SHAFT SPEED IN RAD/SEC RELATIVE TO SPACE
* NODE 0 IS SPACE REFERENCE
* CURRENT INTO NODE 1 IS TORQUE DELIVERED IN OZ-IN
* CURRENT OUT OF NODE 3 IS TORQUE DELIVERED IN OZ-IN
* UNITS: OZ,IN,RAD/SEC
* N1 IS NUMBER OF TEETH ON INPUT GEAR
* J1 IS INPUT GEAR INERTIA IN OZ-IN-SEC/RAD/SEC
* B1 IS INPUT GEAR VISCOUS FRICTION IN OZ-IN/RAD/SEC
* F1 IS INPUT GEAR COULOMB FRICTION IN OZ-IN
* K1 IS INPUT GEAR SHAFT SPRING CONSTANT IN OZ-IN/RAD
* BK1 IS INPUT GEAR SHAFT DAMPING IN OZ-IN/RAD/SEC
* N2 IS NUMBER OF TEETH ON OUTPUT GEAR
* J2 IS OUTPUT GEAR INERTIA
* B2 IS OUTPUT GEAR VISCOUS FRICTION
* F2 IS OUTPUT GEAR COULOMB FRICTION
* K2 IS OUTPUT GEAR SHAFT SPRING CONSTANT
* BK2 IS OUTPUT GEAR SHAFT DAMPING IN OZ-IN/RAD/SEC
* HD IS BACKLASH HALF WIDTH IN RAD REFERRED TO OUTPUT GEAR
LK1 1 5 (1/K1)
RK1 1 5 (1/BK1)
CJ1 5 0 (J1)
RB1 5 2 (1/B1)
E8 8 0 TABLE (V(5,2)) = (-.1M,-1) (.1M,1)
R8 8 0 1G
GFC1 5 2 VALUE = (F1*V(8))
VT1 5 11
EB1 7 2 VALUE = ((N2/N1)*V(6,4))
GT2 4 6 VALUE = ((N2/N1)*I(VT1))
CJ2 6 0 (J2)
RB2 6 4 (1/B2)
E9 9 0 TABLE (V(6,4)) = (-.1M,-1) (.1M,1)
R9 9 0 1G
GFC2 6 4 VALUE = (F2*V(9))
LK2 6 3 (1/K2)
RK2 6 3 (1/BK2)
*
* CIRCUIT TO CALCULATE BACKLASH HALF WIDTH
*
* V(10) = GEAR OFFSET ANGLE IN RADS REFERRED TO OUTPUT GEAR
* V(10) = INTEGRAL[(W1-N*W2)/N]=(THETA1-N*THETA2)/N=THETA1/N-THETA2
GW 0 10 VALUE = (V(5,7)/(N2/N1))
CW 10 0 1
RW 10 0 1K
* CALCULATE POSITIVE BACKLASH SWITCH CLOSURE = V(12)
* V(12) = 0 WHEN V(10) < HD
* V(12) = 1 WHEN V(10) > 1.01*HD
ESP 12 0 TABLE (V(10)/HD) = (.99,0) (1,0) (1.01,1) (1.02,1)
RSP 12 0 1G
* CALCULATE NEGATIVE BACKLASH SWITCH CLOSURE = V(13)
* V(13) = 0 WHEN V(10) > -HD
* V(13) = 1 WHEN V(10) < -1.01*HD
ESN 13 0 TABLE (V(10)/HD) = (-1.02,1) (-1.01,1) (-1,0) (-.99,0)
RSN 13 0 1G
* INPUT TORQUE DIRECTION SENSORS
* IF TORQUE < 0 OR V(5,7) < 0 THEN SET V(15)=0 ,
* OPEN POSITIVE BACKLASH SWITCH FOR NEGATIVE TORQUE OR ROTATION
ETSP 15 0 TABLE (V(5,7)+I(VT1)) = (-10M,0) (0,0) (10M,1) (20M,1)
RTSP 15 0 1G
* IF TORQUE > 0 OR V(5,7) > 0 THEN SET V(16)=0 ,
* OPEN NEGATIVE BACKLASH SWITCH FOR POSITIVE TORQUE OR ROTATION
ETSN 16 0 TABLE (V(5,7)+I(VT1)) = (-20M,1) (-10M,1) (0,0) (10M,0)
RTSN 16 0 1G
* BACKLASH SWITCH TO DISCONNECT INPUT GEAR FROM OUTPUT GEAR
GC 0 20 VALUE = (V(12)*V(15)+V(13)*V(16))
RC 20 0 1
CC 20 0 10UF
SBL 11 7 20 0 RBL
.MODEL RBL VSWITCH (RON=1M ROFF=1MEG VON=1 VOFF=0)
.ENDS GEARBL
```

From **Eqs** **1** and **2**, the gears mesh when either

$$\Delta\Theta_{OUT} \geqslant HD \text{ and } \Delta\omega_{IN} > 0, \qquad (3)$$

or

$$\Delta\Theta_{OUT} \leqslant -HD \text{ and } \Delta\omega_{IN} < 0. \qquad (4)$$

Alternately, the gears are in the backlash region when the absolute value of $\Delta\Theta_{OUT}$ is less than HD; that is, when the relative angle of the gears is less than the backlash halfwidth angle.

Backlash circuit uses a switch

Fig 4 shows the equivalent circuit for a gear train with backlash. The main difference between **Fig 4** and **Fig 2** is **Fig 4**'s controlled source, SBL, which acts as a switch. In the backlash region, SBL is an open circuit, disconnecting the input gear from the output gear. When the gears mesh, SBL acts as a short, connecting the input and output gears. Controlled current source GW and capacitor CW together determine $\Delta\Theta_{OUT}$ at node 10, because the voltage drop from node 5 to 7—V(5,7) in Spice nomenclature—is

$$V(5,7) = \omega_1 - N\omega_2 = \Delta\omega_{IN},$$

and the voltage at node 10—V(10) in Spice nomenclature—equals

$$V(10) = \int (V(5,7)/N)dt = \Delta\Theta_{OUT}.$$

Listing 3 is the code for the gear train with backlash subcircuit (GEARBL). The source ESP uses the table function to set V(12) equal to 1 when V(10)>HD and to set V(12)=0 when V(10)<HD. Similarly, the source ETSP uses the table function to set V(15)=1 when V(5,7)>0 or I(VT1)>0 and to set V(15)=0 when V(5,7)<0 or I(VT1)<0. When both V(12) and V(15) are high, the condition in either **Eq 3** or **4** is satisfied, and the resistance of voltage-controlled resistor SBL is set low, connecting nodes 11 and 7 through a low resistance. The control voltage, V(20), and the following parameters determine the resistance of source SBL: RON=1M, ROFF=1MEG, VON=1, VOFF=0.

The control voltage V(20) is equal to the quantity (V(12)×V(15))+(V(13)×V(16)). If both V(12) and V(15) are high or V(13) and V(16) are high, then the switch resistance is low and nodes 11 and 7 are connected. If any of the nodes 12, 13, 15, or 16 equal 0, then the switch resistance is high, nodes 11 and 7 are disconnected, and the gear train is in the backlash region. Sources ESN and ETSN determine the backlash region for negative offset angles. Elements CC and RC slow the switch transition times, which helps improve transient convergence.

Although the equivalent circuit for the gear train with backlash is fairly complex, using the circuit isn't. You simply define the input and output node connections and give the relevant parameter values, as **Fig 4** shows. In the main-system description, one line describes each subcircuit. As in all simulations, the models should be only as complex as required. If backlash is negligible, use **Fig 2**'s model for a gear train, which

The gear-train-with-backlash model includes a controlled source that operates as a switch.

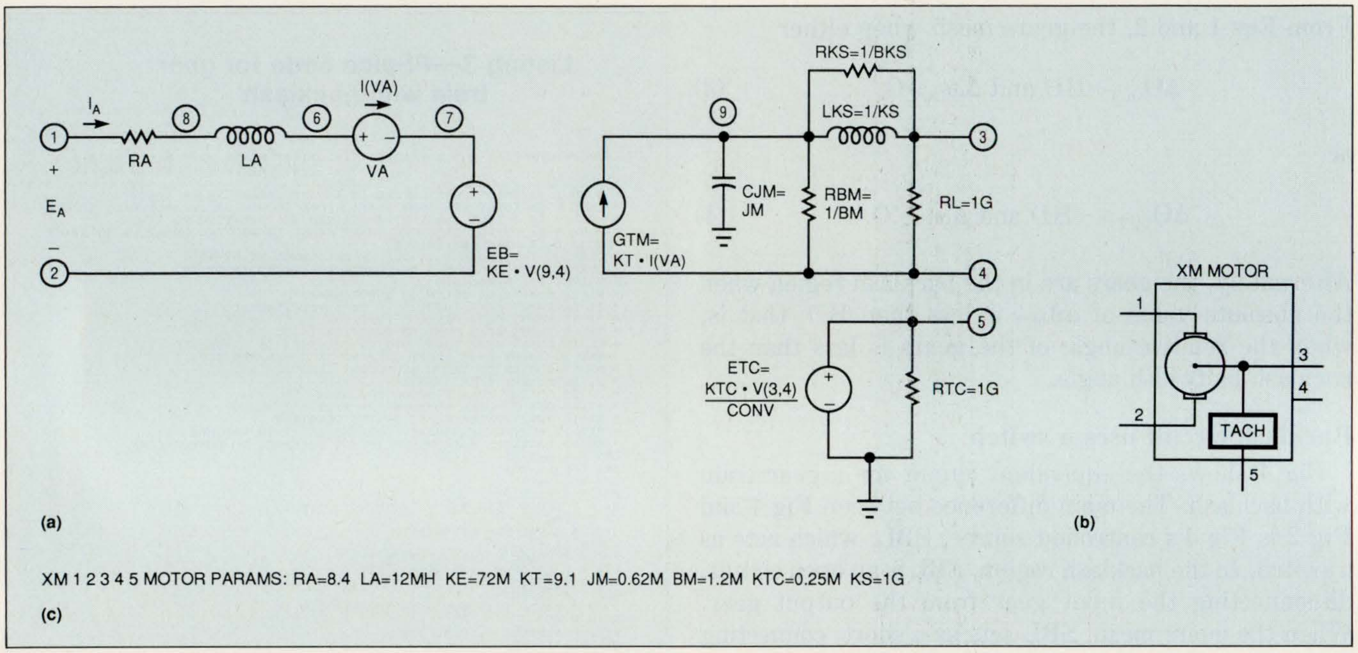

Fig 5—RA and LA model the armature resistance and inductance, respectively, *of this dc motor equivalent circuit (**a**). The subcircuit has five external connections, as **b** shows, two inputs, two outputs, and one tachometer output. Again, the call statement (**c**) requires you to define a number of parameters.*

is much simpler. The backlash model can greatly lengthen the simulation time because fast transients occur whenever the gear hits the backlash region, an event that can occur many times during a simulation. Backlash also causes a problem for ac small-signal analysis because the backlash condition prevents signals from transmitting through the gear train. For ac analysis, either bias the gear out of the backlash region or use the **Fig 2** gear model, which has no backlash.

The servo motor connects the electrical and mechanical parts of a servo system. The motor's input is electrical, and its output is mechanical. The dc motor with armature control and the permanent-magnet motor are analogous to an electrical transformer. The input's electrical power is equal to the output's mechanical power. The torque is proportional to the armature current, I_A, and equals

$$T=K_TI_A$$

where K_T is the motor's torque constant. The back EMF, E_B, produced in the armature circuit is proportional to the motor speed, ω_M, as follows:

$$E_B=K_E\omega_M.$$

K_E is the back EMF constant. For an ideal dc motor,

$$I_AE_B=T\omega_M \text{ (watts).}$$

Fig 5 shows the analogous equivalent circuit for the dc motor (**Refs 1, 2, and 3**). **Listing 4** presents the

Listing 4—PSpice code for dc motor with armature control

```
.SUBCKT MOTOR 1 2 3 4 5 PARAMS:RA=1M LA=1NH KE=7.06M KT=1 JM=1P
+                              BM=1N KTC=1M KS=1G BKS=1N
+                              CONV=.10472
* DC MOTOR WITH ARMATURE CONTROL
* NODE 1 IS POSITIVE MOTOR ARMATURE VOLTAGE
* NODE 2 IS NEGATIVE MOTOR ARMATURE VOLTAGE
* NODE 3 IS MOTOR SHAFT SPEED IN RAD/SEC RELATIVE TO SPACE
* NODE 4 IS MOTOR PLATFORM SPEED IN RAD/SEC RELATIVE TO SPACE
* NODE 0 IS SPACE REFERENCE
* NODE 5 IS TACH OUTPUT IN VOLTS OF MOTOR SPEED RELATIVE TO PLATFORM
* CURRENT OUT OF NODE 3 IS TORQUE DELIVERED IN OZ-IN
* UNITS : OZ,IN,RAD/SEC
* RA IS ARMATURE RESISTANCE IN OHMS
* LA IS ARMATURE INDUCTANCE IN HENRIES
* KE IS MOTOR BACK EMF CONSTANT IN VOLTS/RAD/SEC
* KT IS MOTOR TORQUE CONSTANT IN OZ-IN/AMP
* JM IS MOTOR INERTIA IN OZ-IN-SEC/RAD/SEC
* BM IS MOTOR VISCOUS FRICTION IN OZ-IN/RAD/SEC
* KS IS MOTOR SPRING CONSTANT IN OZ-IN/RAD
* BKS IS SHAFT SPRING DAMPING IN OZ-IN/RAD/SEC
* KTC IS TACHOMETER GAIN CONSTANT IN VOLTS/RPM
* CONV IS RPM TO RAD/SEC CONVERSION CONSTANT = 2PI/60
RA 1 8 (RA)
LA 8 6 (LA)
VA 6 7
EB 7 2 VALUE = (KE*V(9,4))
GTM 4 9 VALUE = (KT*I(VA))
CJM 9 0 (JM)
RBM 9 4 (1/BM)
LKS 9 3 (1/KS)
RKS 9 3 (1/BKS)
ETC 5 0 VALUE = (KTC*V(3,4)/CONV)
RTC 5 0 1G
RL 3 4 1G
.ENDS MOTOR
```

Simulation models should be only as complex as necessary. If certain conditions, such as gear-train backlash, are negligible, use the simplest model.

code for the subcircuit named MOTOR. RA is the armature resistance, and LA is the armature inductance. Additional parameters define the motor inertia, viscous friction, and shaft stiffness. In addition, a tachometer output is provided at node 5. The armature voltage connects across nodes 1 and 2. Node 3 represents the motor shaft speed. Node 4 represents the motor platform speed. **Fig 5**'s model is linear and fairly simple. The models for the dc motor with field control and the ac motor are even simpler.

Note that although individual parameters are provided for the back EMF constant (KE) and the motor's torque constant (KT), these parameters are not independent (**Refs 2** and **3**), even though they are often specified independently. KE equals KT in the SI system of units (Newton, meter, radian, second). In the system of units used here (ounce, inch, radian, second), KE equals $7.06 \times 10^{-3} \times$ KT. These relationships come from setting the input electrical power equal to the output mechanical power for an ideal motor. Measurements of KE and KT may differ due to parasitic losses, which are not accounted for.

The following example combines these mechanical models with standard electrical components to simulate the inner-most loop of the roll axis of a complex airborne antenna-positioning servo system. **Fig 6** is a block diagram of the tachometer feedback loop for the dc motor with armature control. The power amplifier uses current feedback to control the motor armature current, thereby controlling the motor torque. The demodulator provides a feedback signal from the motor tachometer output, allowing control of the motor shaft speed. The op amp acts as a summer, closing the loop.

Open the loop

Listing 5 presents the PSpice code for an ac open-loop analysis of the tachometer feedback loop. The components LOL, COL, and VOL, along with their assigned values of 1 kH, 1 kF, and 1V ac, respectively, serve to open the loop for ac analysis while maintaining

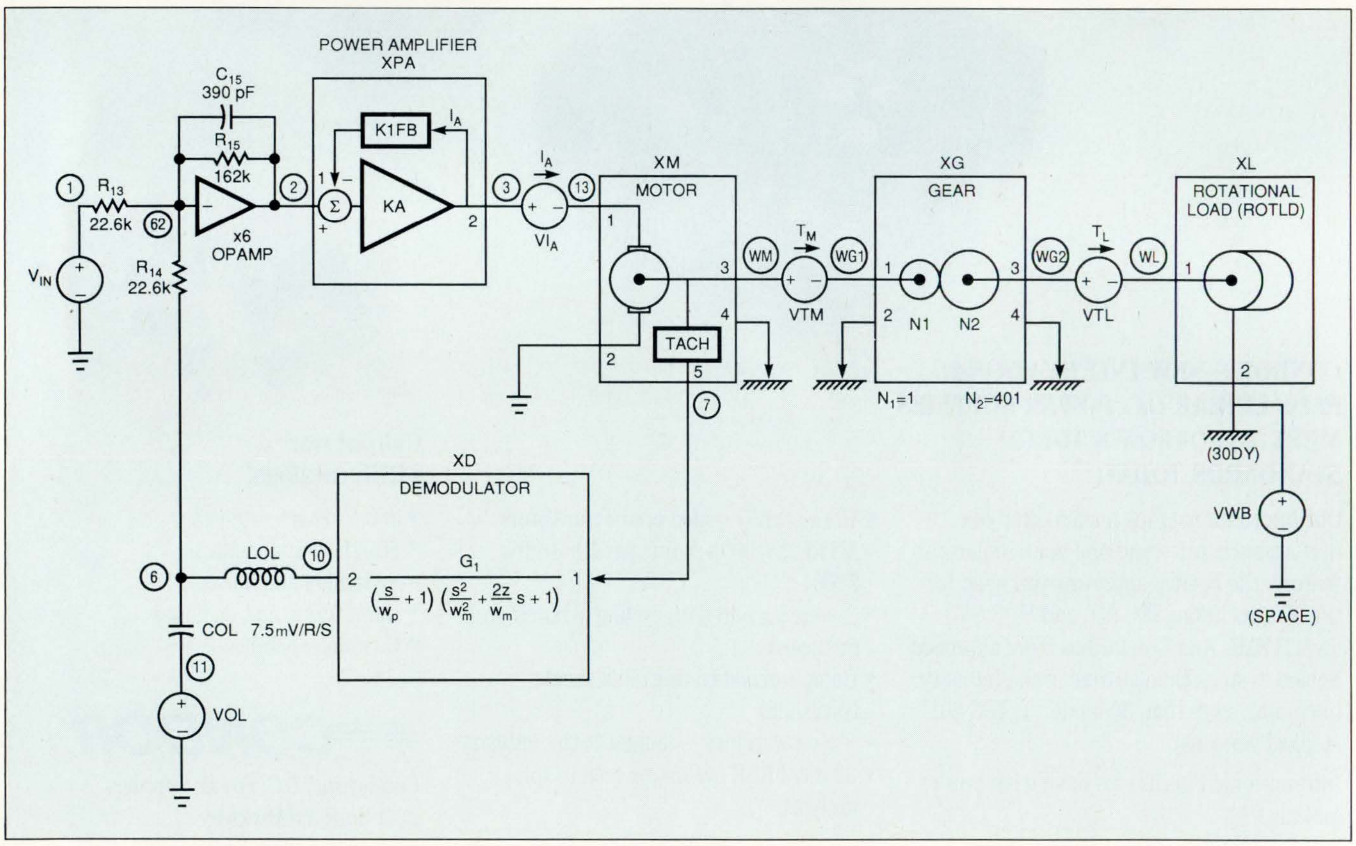

Fig 6—This servo loop models a dc motor with tachometer-feedback control. The power amplifier uses current feedback to control the motor armature current thereby controlling the motor torque. The demodulator provides feedback from the motor, allowing the loop to control the motor shaft speed.

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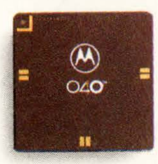

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Don't be surprised if certain parameters, especially nonlinear ones such as backlash, greatly increase the simulation time.

the correct dc operating point. VOL injects a 1V ac signal at node 6, COL is a short at ac, and LOL is an open at ac. Under these conditions, and with VIN equal to zero, the voltage at node 10 equals the loop gain.

To perform meaningful ac analysis, the models must not include step-type nonlinearities or you must bias the circuit outside the nonlinear regions. Thus, use a power-amplifier model without deadzone, the gear model without backlash, and a simple rotational load model. **Fig 7a** shows the ac open-loop gain and phase of the tachometer feedback loop. The open-loop crossover frequency is 9.5 Hz, and the phase margin is 90°. The notch at 21 Hz and peak at 40 Hz are due to the gear-stiffness parameter K2 resonating with the load inertia and motor inertia. The gear-shaft damping parameter BK2 determines the Q of this resonance. The values for K2 and BK2 match the measured data. The gain margin for the tachometer loop is 12 dB at 190 Hz.

You can obtain the ac closed-loop response by setting LOL = 1 nH, COL = 1 pF, VOL = 0V ac, and VIN to 1V ac. WM, the motor-shaft-speed node, now repre-

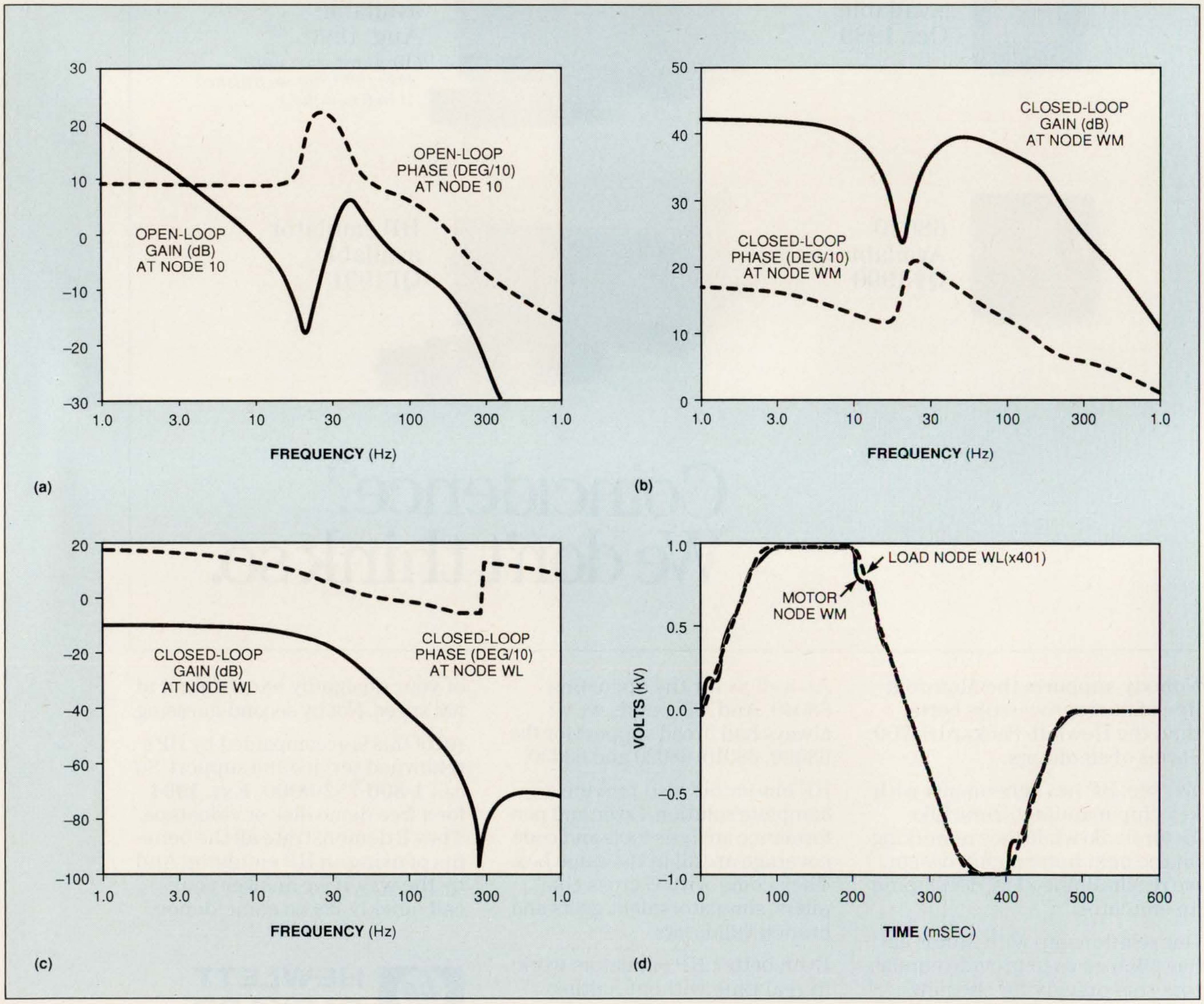
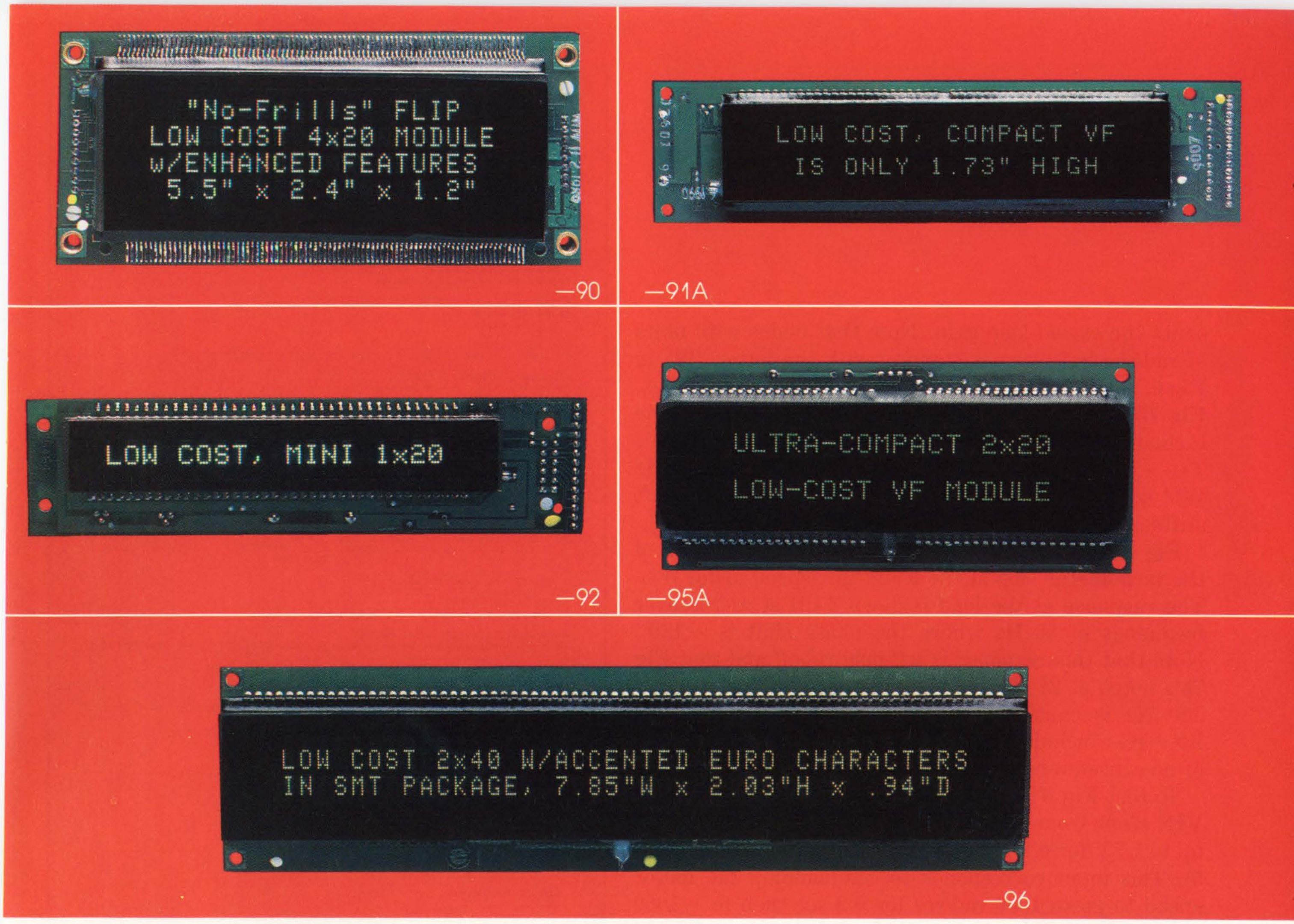


Fig 7—Using a combination of electrical and mechanical models, *you can simulate* ***Fig 6***'s *tachometer loop and investigate the open-loop gain and phase (**a**), the closed-loop gain and phase at both the motor (**b**) and the load (**c**), and the transient response of the motor and load (**d**) to a square-wave input.*



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sents the closed-loop gain. Note that nodes with units of rad/sec have names starting with the letter "W" in **Fig 6**, which helps identify the mechanical speed nodes. **Fig 7b** shows the ac closed-loop gain and phase of the tachometer loop at the motor-shaft-speed node, WM. The −3-dB bandwidth of the tachometer loop at node WM is 10 Hz. The notch resulting from the gear-shaft stiffness is clearly seen at 21 Hz.

Fig 7c shows the ac closed-loop gain and phase of the tachometer loop at the load-shaft-speed node, WL. The response at the load is down 3 dB at a crossover frequency of 30 Hz where the phase shift is −120°. Note that this response is a 2-pole rolloff and that **Fig 7b**'s notch at 21 Hz is no longer present. The notch at 300 Hz is caused by the high parasitic stiffness—KS = 1G—included in the rotational load model and is of no consequence at such a high frequency.

To test **Fig 6**'s transient response, the input voltage VIN steps from 0 to −7.5V for 0.2 sec, and then steps up to 7.5V for 0.2 sec before returning to zero (**Listing 5**). This input corresponds to commanding the motor speed to go to 1000 rad/sec for 0.2 sec then to −1000 rad/sec for 0.2 sec before returning to zero. **Fig 7d** shows the motor-speed response and the load-speed response. There is significant slewing because of the power amplifier's 3.5A current limit. The load torque showed some ringing because of the gear-shaft stiffness, but the load-speed response was smooth. These responses were obtained with no dead zone and no backlash.

The PSpice program is particularly efficient for ac analysis. Frequency sweeps with 150 data points typically took 20 seconds to run on a Compaq 386/33 with a 80387/33 coprocessor. Transient runs took several minutes to run. Including gear backlash in the model greatly increases the transient runtime, depending on how many times the simulation traverses the backlash region. In this example, adding backlash to the tachometer loop circuit caused very little difference in the output. However, the simulation crossed the backlash region three times, causing the CPU time to triple. When running worst-case analysis, remember that the runtime is proportional to the number of cases.

As enhanced versions of Spice continue to improve, they will become even more useful for the simulation of servo systems. Areas of possible improvement include the ability to assign mechanical unit labels, the ability to directly assign tolerances to subcircuit parameters, and faster execution of behavioral models during transient analysis. EDN

Listing 5—PSpice code for tachometer loop simulation

```
ANTENNA SERVO - TACH LOOP SIMULATION
* TACHLOOP.CIR
* NODE NAMES STARTING WITH W ARE SPEED IN RAD/SEC
* CURRENT AT SPEED NODES IS TORQUE IN OZ-IN
*
* PARAMETERS
.PARAM PI2=6.2831853
*
* INPUT TACH VELOCITY COMMAND IN VOLTS : 7.5V=1000R/S AT MOTOR
VIN 1 0 AC 0 PWL(0S 0V 1MS -7.5V .2S -7.5V .201S 7.5V .4S 7.5V .401S 0)
*
* BODY TO SPACE SPEED INPUT IN RAD/SEC
VWB WB 0 AC 0 PWL(0 0 1MS 0)
*
* TACHOMETER LOOP FEEDBACK AMPLIFIER
R13 1 62 22.6K
R14 6 62 22.6K
R15 62 2 162K
C15 62 2 390PF
X6 0 62 2 OPAMP PARAMS: G1=200K WP=(5HZ*PI2) VLIM=13.5V
*
* MOTOR POWER AMPLIFIER
* FOR AC DO NOT USE DEADZONE
* XPA 2 3 POWAMPDZ PARAMS: KA=120 K1FB=3 ILIM=3.5A VLIM=130V DZ=.2V
* +                        RO=1 WP=(100KHZ*PI2)
XPA 2 3 POWAMP PARAMS: KA=120 K1FB=3 ILIM=3.5A VLIM=130V RO=1
+                      WP=(100KHZ*PI2)
*
* MOTOR MODEL
VIA 3 13
XM 13 0 WM WB 7 MOTOR PARAMS: RA=8.4 LA=12MH KE=72M KT=9.1 JM=.62M
+                             BM=1.2M KTC=.25M
VTM WM WG1
*
* GEAR MODEL
* FOR AC SET F1=F2=0
XG WG1 WB WG2 WB GEAR PARAMS: N1=1 N2=401 K2=4.73MEG BK2=6873
* XG WG1 WB WG2 WB GEARBL PARAMS: N1=1 N2=401 K2=4.73MEG BK2=6873
* +                               HD=1.2M
*
* ROTATIONAL LOAD MODEL
VTL WG2 WL
* FOR AC SET FC=0
XL WL WB ROTLD PARAMS: J=272 B=35
*
* TACHOMETER DEMODULATOR MODEL
XD 7 10 DEMOD PARAMS: G1=3.14 WP=(19.5KHZ*PI2) Z=.47 WN=(202HZ*PI2)
*
* SET LOL=1KH , COL=1KF , VOL=1VAC FOR AC OPEN LOOP
* LOOP GAIN = VDB(10) VP(10)
LOL 10 6 1KH
COL 6 11 1KF
VOL 11 0 AC 1
*
* ANALYSIS COMMANDS
*
* .AC DEC 50 1HZ 100HZ
.AC DEC 50 1HZ 1KHZ
.PRINT AC VDB(10) VP(10) VDB(2) VDB(3) VDB(7) VDB([WM]) VDB([WL])
+          VP([WL])
* .TRAN 5MS 600MS 0MS 5MS
.PRINT TRAN V(1) V(6) V(2) V(3) V([WM]) V([WL]) V(7)
.PRINT TRAN I(VIA) I(VTM) I(VTL)
.OP
.PROBE
.OPTIONS ACCT LIST NODE
.OPTIONS RELTOL=1M ABSTOL=1U VNTOL=1U
.OPTIONS ITL1=100 ITL2=20 ITL5=10000 CHGTOL=1C
*
.LIB SERVO.LIB
.END
```

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2. Kuo, B, *Automatic Control Systems*, Prentice Hall, NJ, 1987.

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Author's biography

Dr Vincent G Bello is a senior member of the technical staff at the Norden Systems (Norwalk, CT) division of United Technologies and has been with the company for 21 years. He specializes in the analysis and design of analog circuits and has used Spice extensively. He developed widely used Spice models for switching regulators. Dr Bello has written one book, fourteen papers, and holds four patents. He has a bachelor's degree from Manhattan College and a masters and PhD from New York University.

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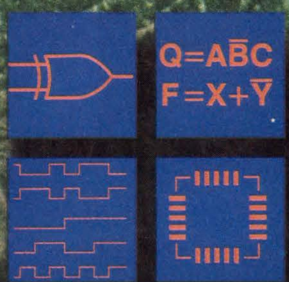

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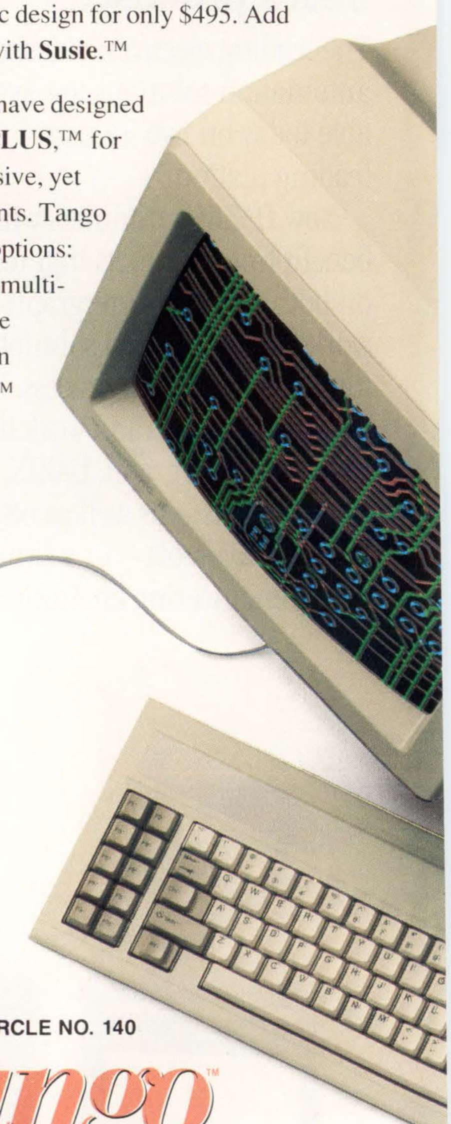

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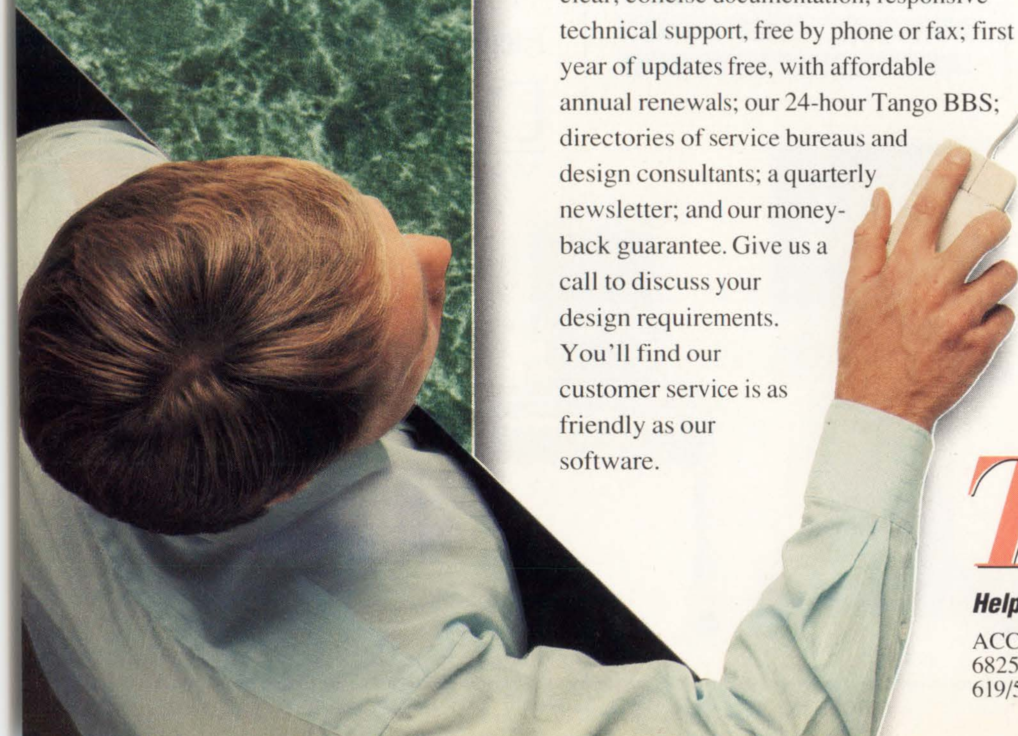

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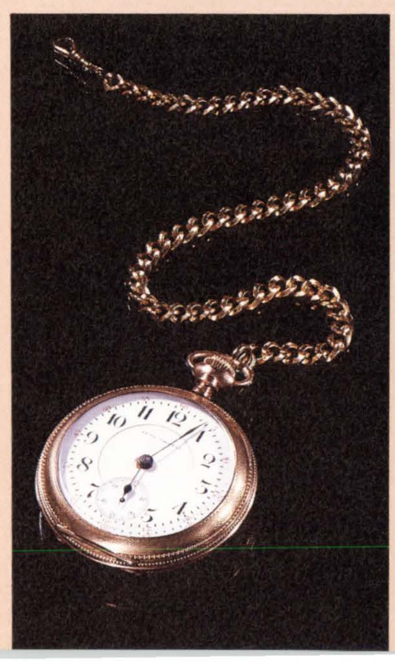

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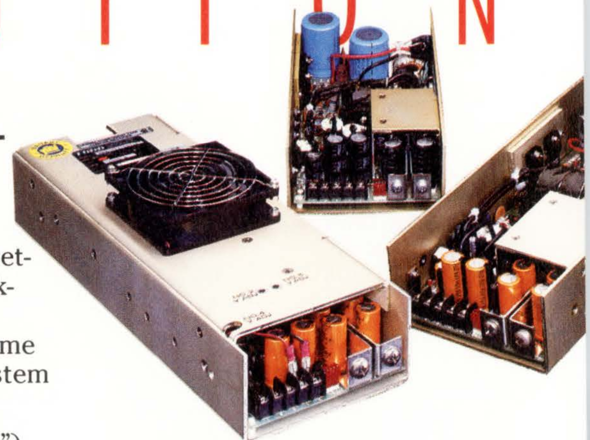

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MAX-354-1205	+5V @ 50A	+12V @ 8/12Apk	-12V @ 4.0A	-5.2 @ 2.0A
MAX-354-1212	+5V @ 50A	+12V @ 8/12Apk	-12V @ 4.0A	12V @ 2.0A
MAX-354-1224	+5V @ 50A	+12V @ 8/12Apk	-12V @ 4.0A	+24V @ 1.5A
Model	**400,500 WATTS: 2.5"x5"x11.5"***			
MSC-402-0512	+5V @ 20A	+12V @ 25/36Apk	—	—
MAX-503-0512	+5V @ 80A	+12V @ 10/16Apk	-12V @ 10.0A	—
MAX-504-1252	+5V @ 80A	+12V @ 10/16Apk	-5.2V @ 10.0A	12V @ 2.0A
MAX-504-1205	+5V @ 80A	+12V @ 10/16Apk	-12V @ 10.0A	5.2V @ 2.0A
MAX-504-1212	+5V @ 80A	+12V @ 10/16Apk	-12V @ 10.0A	12V @ 2.0A
MAX-504-1224	+5V @ 80A	+12V @ 10/16Apk	-12V @ 10.0A	+24V @ 2.0A
MAX-504-1552	+5V @ 80A	+15V @ 10/16Apk	-5V @ 10.0A	15V @ 2.0A
Model	**700,750 WATTS: 2.5"x5"x13.6"***			
MAX-704-1205	+5V @ 100A	+12V @ 12/20Apk	-12V @ 10.0A	5.2V @ 2.0A
MAX-704-1212	+5V @ 100A	+12V @ 12/20Apk	-12V @ 10.0A	12V @ 2.0A
MAX-753-0512	+5V @ 120A	+12V @ 12/20Apk	-12V @ 10.0A	—
MSC-753-0512	+5V @ 120A	+12V @ 20/27Apk	-12V @ 6.0A	—
MAX-754-1252	+5V @ 120A	+12V @ 12/20Apk	-5.2V @ 10.0A	12V @ 2.0A
MAX-754-1205	+5V @ 120A	+12V @ 12/20Apk	-12V @ 10.0A	5.2V @ 2.0A
MAX-754-1212	+5V @ 120A	+12V @ 12/20Apk	-12V @ 10.0A	12V @ 2.0A
MAX-754-1224	+5V @ 120A	+12V @ 12/20Apk	-12V @ 10.0A	+24V @ 2.0A

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EDN DESIGNERS' GUIDE TO

subranging ADCs
part I

Subranging ADCs operate at high speed with high resolution

Subranging A/D converters offer performance levels difficult to obtain with successive-approximation or flash converters. They can deliver higher conversion speed and resolution and suit such applications as digital signal processing. Part 1 of this 3-part series explores the architecture and operation of these devices. Part 2 will cover subranging-ADC parameters and specifications. Part 3 will conclude the series with test and measurement principles.

Ray K Ushani, *Datel Inc*

The subranging, or multipass, A/D converter has become increasingly popular in the last few years. A major reason for this popularity is digital signal processing, which demands high conversion speeds and resolution. The traditional successive-approximation converter has reached its speed-resolution limit (about 1 μsec for 12 bits) and can't meet the demands of many applications. Although flash converters offer high speeds, a practical limit exists to the resolution they can provide because the number of comparators rises exponentially with the number of bits. A 12-bit flash converter, for example, does not exist.

A flash converter, however, is an essential part of the subranging-ADC architecture. Designers have a wider choice of flash converters than they did a few years ago, and today's devices have significantly better performance and lower prices (approximately $10 for an 8-bit flash converter in OEM quantities). Semicustom design has also helped spur subranging-ADC manufacturing because the devices inherently require more components than successive-approximation converters. Integrating the timing and correction logic on a single chip greatly reduces cost, the number of active components, and assembly and reliability problems.

The three types of subranging-ADC architectures are conventional, pipelined, and intermeshed; each type best suits certain applications. All subranging ADCs—whether the device is a hybrid IC or ICs and discrete components on a pc board—contain at least a sample-and-hold (S/H) circuit, a D/A converter, a scaling network, and timing and digital-correction logic.

The conventional subranging architecture **(Fig 1)** is a 2-stage A/D converter. With S_1 closed and S_2 open, the S/H circuit switches to the hold mode. The flash converter then quantizes the input signal, V_{IN}. After proper scaling, the D/A converter converts the digitized and latched signal back into an equivalent voltage. This voltage is subtracted from the original input signal at the summing junction, yielding the difference between the first conversion and the input signal. The closing of S_2 and the opening of S_1 feeds the difference signal back to the flash converter, which amplifies and digitizes the signal. After latching, the result of this conversion goes through the digital-correction logic to produce the output.

The three different types of subranging-ADC architectures are conventional, pipelined, and intermeshed.

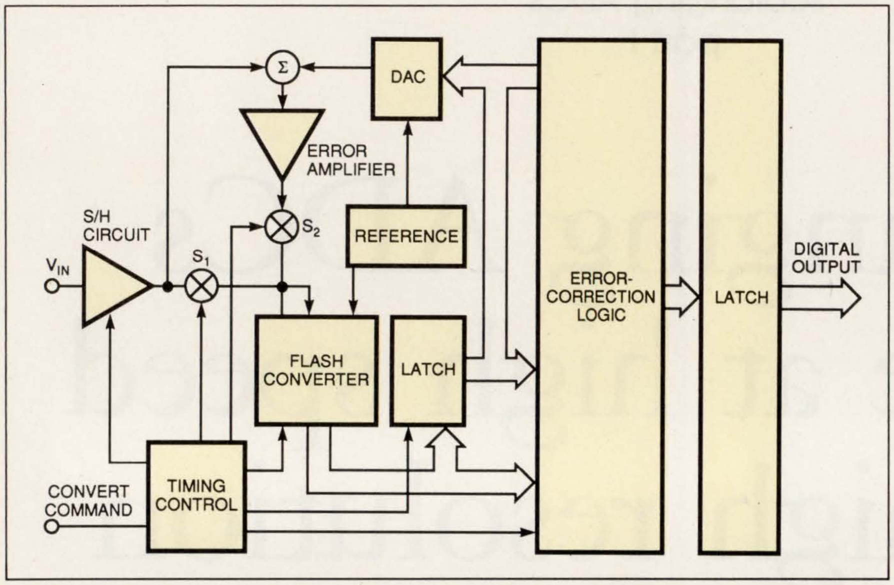


Fig 1—A conventional subranging ADC *uses an S/H circuit, a flash converter, and a D/A converter.*

Designing and fabricating a good high-resolution flash converter is a major task. Therefore, in monolithic subranging ADCs, using a lower-resolution (3- to 4-bit) flash converter is preferable. Of course, the lower resolution means more passes through the flash converter, making the subranging ADC seem like a successive-approximation converter with a reduced number of trials. This variation of the conventional architecture, which combines flash and successive-approximation features, is the recursive subranging architecture.

The second type of subranging converter has a pipelined architecture. Compared with the other subranging-ADC types, the pipelined architecture offers a faster throughput rate because the circuit can initiate a new conversion before the previous conversion is finished. However, the conversion time is not significantly improved, and the digital output data corresponding to the present conversion is always delayed by at least one clock.

The 2-stage pipelined converter has an extra S/H circuit and an extra flash converter (**Fig 2**). In operation, the first S/H circuit switches to the hold mode after acquiring the input signal, V_{IN}. The first flash converter then quantizes the input signal, while the

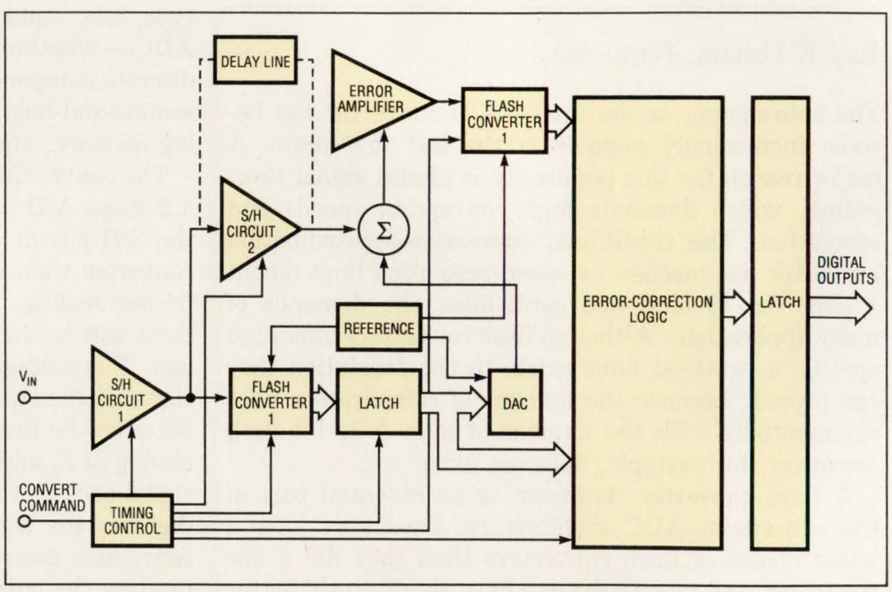


Fig 2—A pipelined subranging ADC *uses two S/H circuits, two flash converters, and a D/A converter.*

second S/H circuit goes to the hold mode. The D/A converter latches and converts the digitized signal into an equivalent voltage. This voltage is then subtracted from the held output voltage of the second S/H circuit, which represents the input voltage at the time the first flash converter made its conversion. The second flash converter amplifies and digitizes the difference between the first conversion and the input voltage. After latching, the result of this conversion goes through the digital correction logic to produce the output.

Immediately after the second S/H circuit switches to the hold mode, the input S/H circuit can acquire a new signal, effectively increasing the throughput rate (the rate at which the converter can accept new convert commands). Another advantage of pipelining is that you can time the outputs of the S/H circuit and the A/D converter to change simultaneously. Thus, the outputs don't overdrive the error amplifier, resulting in only a very short transient switching glitch.

In place of the S/H circuit, you could also use a delay line. For the optimum throughput rate, the delay should not exceed the conversion time of the first flash converter plus the settling time of the D/A converter. The delay line itself must be of high fidelity and have a large bandwidth.

The third type of subranging converter uses an intermeshed architecture. **Fig 3** shows a block diagram of this type of converter, which operates as follows: After the S/H circuit acquires the signal, the MSB flash converter decides the range of the input. This input lies between two resistors in the ladder and determines the most significant bits. These two points on the resistor ladder then switch to the reference top and reference bottom of the second flash converter (the higher

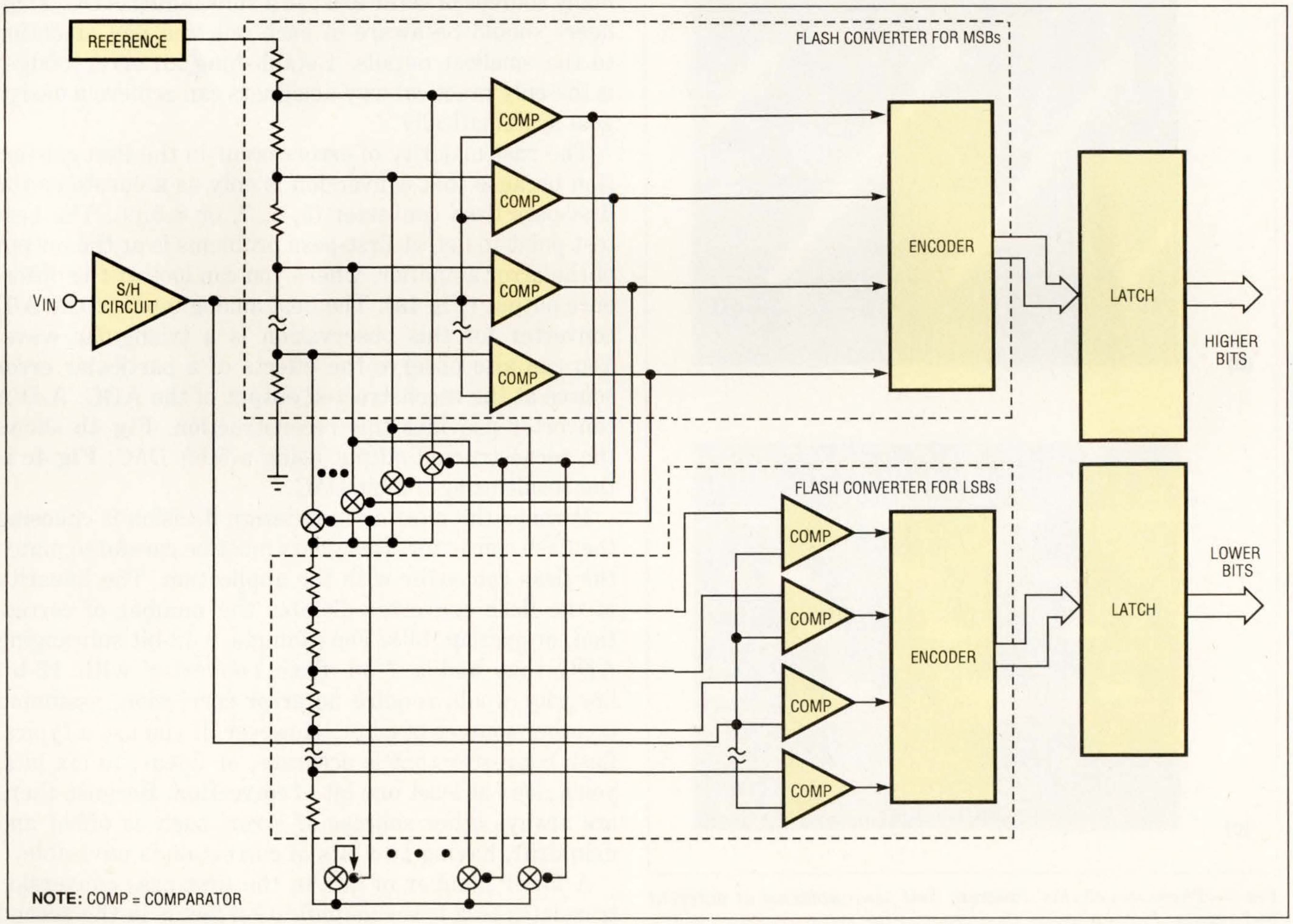
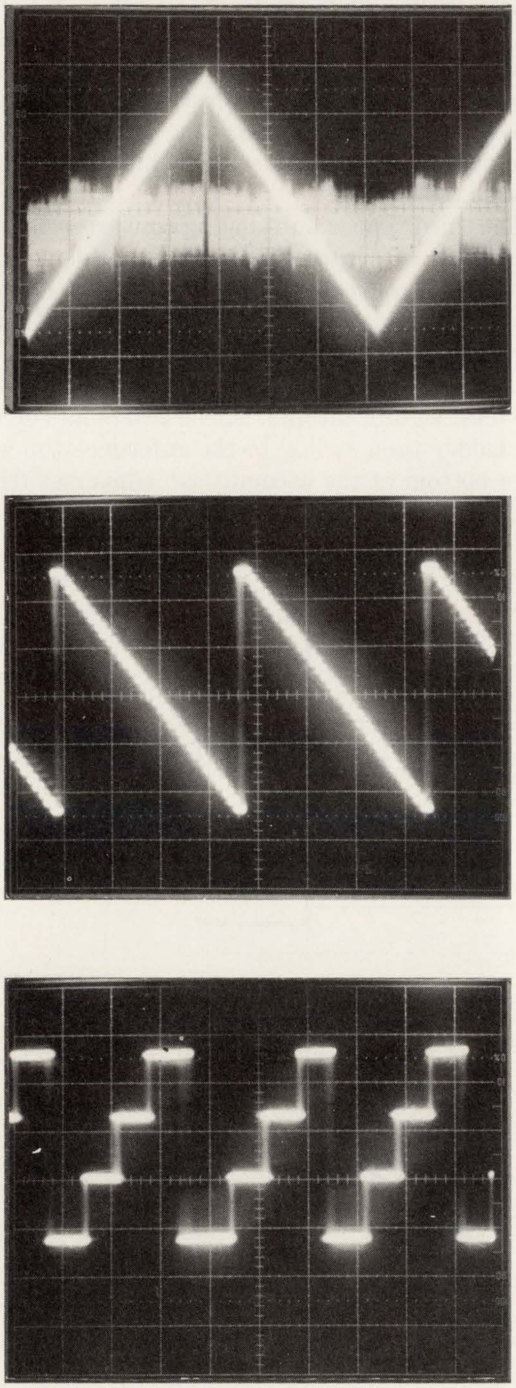


Fig 3—An intermeshed subranging ADC *uses separate flash converters for the MSBs and LSBs. Note the absence of the D/A converter, the error amplifier, and the correction logic.*

Perhaps the most critical design decision is choosing the flash converter.



(a)

(b)

(c)

Fig 4—These waveforms illustrate first-pass problems at different test points. *Photo **a** shows the output of the error amplifier with a triangle-wave input. Photos **b** and **c** show the reconstructed output of the ADC using a 5-bit DAC **(b)** and a 2-bit DAC **(c)**.*

voltage on the ladder will be the reference top and the lower voltage will be the reference bottom). Upon a convert command, the LSB flash converter digitizes the original input to produce the least significant bits.

Because this architecture has no correction logic, the MSB flash converter must be as linear as the intended linearity of the overall A/D converter. Note the absence of the D/A converter, the error amplifier, and the correction logic in the block diagram. This relative simplicity, plus the fact that the circuitry is repetitive, suits the intermeshed architecture for monolithic applications.

To the uninitiated, the block diagram of a subranging A/D converter can appear to be deceptively simple, consisting merely of a few building blocks. On the contrary, subranging A/D converters are the most challenging ADCs to design and manufacture. Because many sources of error exist in a subranging ADC, engineers should be aware of each one and pay attention to the smallest details. Establishing an error budget is the only practical way designers can achieve a design goal systematically.

The vast majority of errors occur in the first conversion because that conversion is only as accurate as the first-pass flash converter (5, 6, 7, or 8 bits). The best test point to detect first-pass problems is at the output of the error amplifier, where you can look at the difference output (**Fig 4a**). The best analog input to the A/D converter for this observation is a triangular wave. You can also observe the effects of a particular error source at the reconstructed output of the ADC. A D/A converter provides this reconstruction. **Fig 4b** shows the reconstructed output using a 5-bit DAC; **Fig 4c** is the result using a 2-bit DAC.

Perhaps the most critical design decision is choosing the flash converter. Designers must be careful to match the flash converter with the application. The linearity of the flash converter dictates the number of correction, or overlap, bits. For example, a 12-bit subranging ADC that had a 7-bit flash converter with 12-bit linearity would require no error correction, assuming no other sources of error. However, if you use a typical flash converter that is accurate, or linear, to six bits, you'll need at least one bit of correction. Because there are always other sources of error, such as offset and gain drift, having two bits of correction is advisable.

A lower number of bits in the first-pass conversion translates to a lower amplification factor in the second pass. As a result, the amplifier settles faster, and you can get by with a lower-resolution D/A converter, which is easier to design. However, this lower-resolution DAC mandates a higher-resolution flash converter in the second pass, which is more expensive than a lower-resolution converter.

CMOS flash converters are attractive because of their low power consumption. Converters that operate from a single supply have especially low power consumption. However, because most CMOS flash converters use a design scheme in which the comparators switch back and forth between the reference ladder and the input depending on the clock level (**Fig 5**), large glitches that are synchronized to the convert command appear at the converters' inputs. As a result, CMOS converters distort the input signal, making the devices hard to drive. To overcome this problem, use a high-speed, wide-bandwidth buffer with low output impedance.

CMOS flash converters cause large spikes on the power lines, which not only degrade the performance of the converter, but also create problems for the overall system. Heavily bypassing the reference voltages and power lines right at the flash converter helps lessen, or prevent, spikes. Also, avoid external HCMOS logic when the ADC's sampling rate is greater than 5 MHz. Because of its high-speed switching, HCMOS logic also creates large spikes on the power lines.

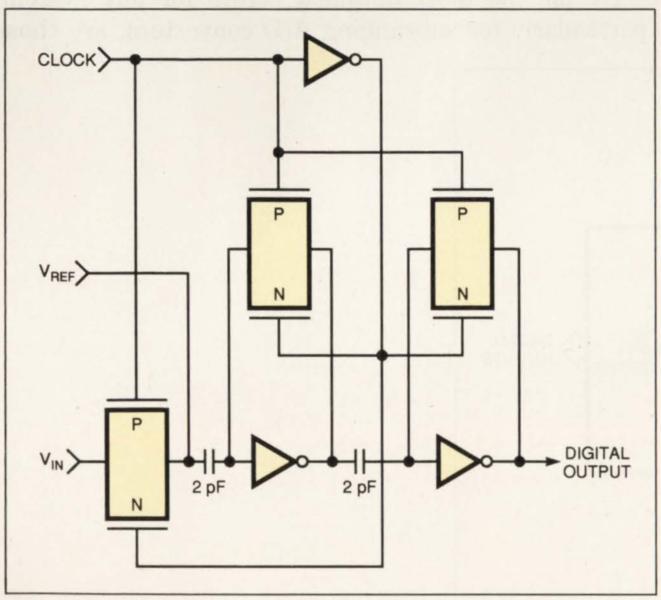


Fig 5—Most CMOS flash converters use a design scheme *in which the comparators switch back and forth between the reference ladder and the input. This switching can cause undesirable glitches synchronized to the convert command.*

Compared with CMOS types, bipolar flash converters, have fewer problems. However, most bipolar flash ADCs require dual supplies (often +5 and −5.2V) and usually consume more power than CMOS converters.

In a subranging A/D converter, the bit resolution of the D/A converter does not need to be more than the resolution of the flash converter used in the first-pass conversion. However, the DAC's differential and integral linearity must be considerably better than the desired differential and integral linearity of the A/D converter. The integral nonlinearity of the DAC not only causes integral nonlinearities but creates nonmonotonicity and differential nonlinearities every time the input of the DAC changes. This effect is called overlap; **Fig 6** illustrates overlap at the ADC's reconstructed output. The DAC should have an accuracy

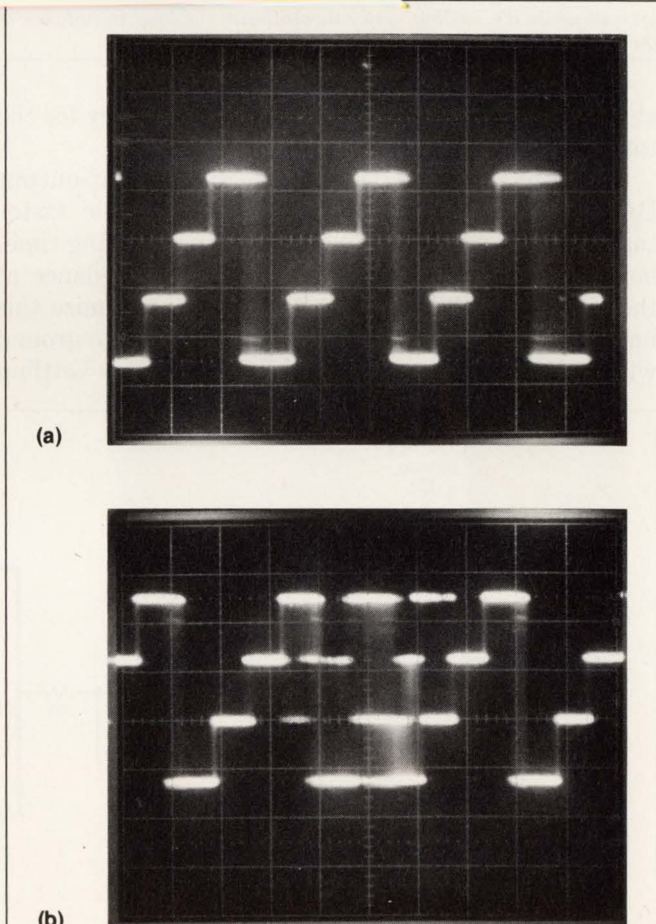


Fig 6—These scope photos compare *the reconstructed output of the D/A converter in the typical case **(a)** and when the DAC has integral error **(b)**. This error is called overlap.*

The resolution of the DAC in a subranging A/D converter does not need to be greater than that of the first-pass flash converter.

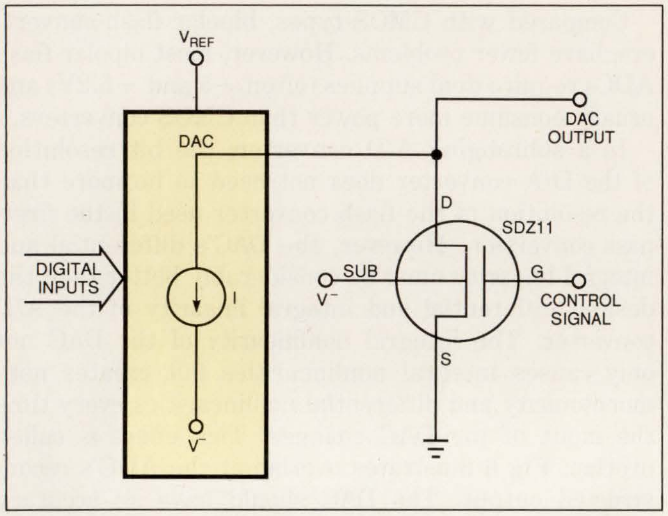


Fig 7—By using a MOSFET to switch *the output of the DAC to ground while it's settling, you can minimize the load impedance at the output of the DAC and optimize its settling time.*

at least 1-bit greater than the desired accuracy for the total converter.

For subranging A/D converters, current-output DACs are a good choice because they settle faster than voltage-output DACs. For optimum settling time, however, you should minimize the load impedance at the output of the DAC. The best way to minimize this impedance is to switch the output of the DAC to ground with a MOSFET transistor while the DAC is settling **(Fig 7)**. Most current-output DACs have application resistors you can use to set the best gain and gain-drift performance. If the DAC does not have such resistors you must design them into the same resistor network that sets the reference current of the DAC.

The error amplifier

The error amplifier scales the difference between the first-conversion output and the input signal. The characteristics of the first-pass flash converter determine the gain of this amplifier. This amplifier does not have to settle to better than the accuracy of the second flash converter; therefore, most commercially available monolithic high-speed op amps will do. However, because the amplifier's closed-loop gain requirements are normally high, the device is subject to saturation while the error signal is settling. To eliminate this problem, make sure the error signal settles before it switches to the amplifier, as **Fig 8** shows.

Another problem to watch for is overvoltage-recovery time. If the input of the A/D converter exceeds the analog input range even slightly, an undesirable overvoltage recovery time will occur. Usually the input capacitance of the flash converter increases the amplifier's overshoot and, as a result, increases the settling time. In this case, a small-value resistor in series with the output of the amplifier can help.

By far the most untamed errors for any system, particularly for subranging A/D converters, are those

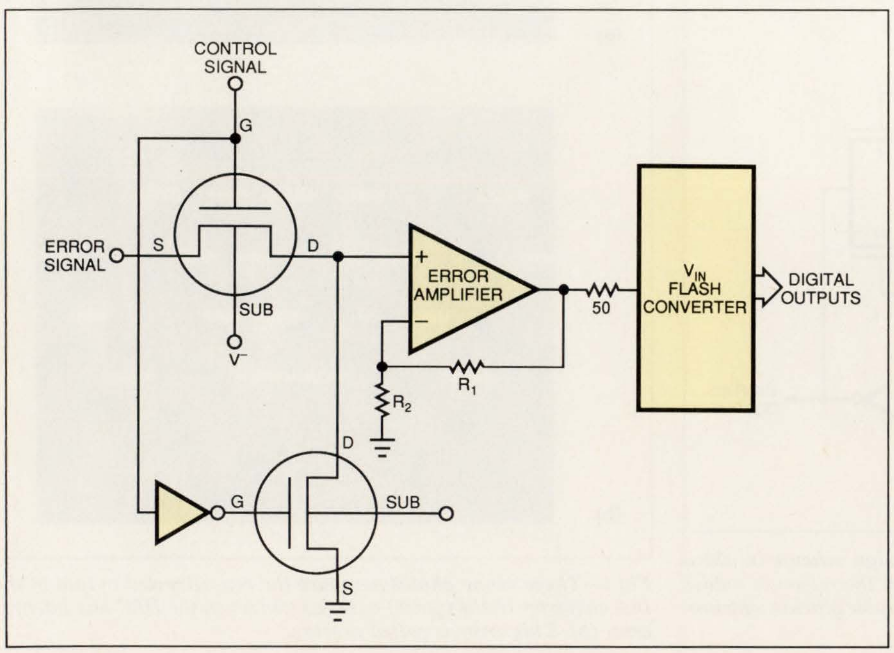
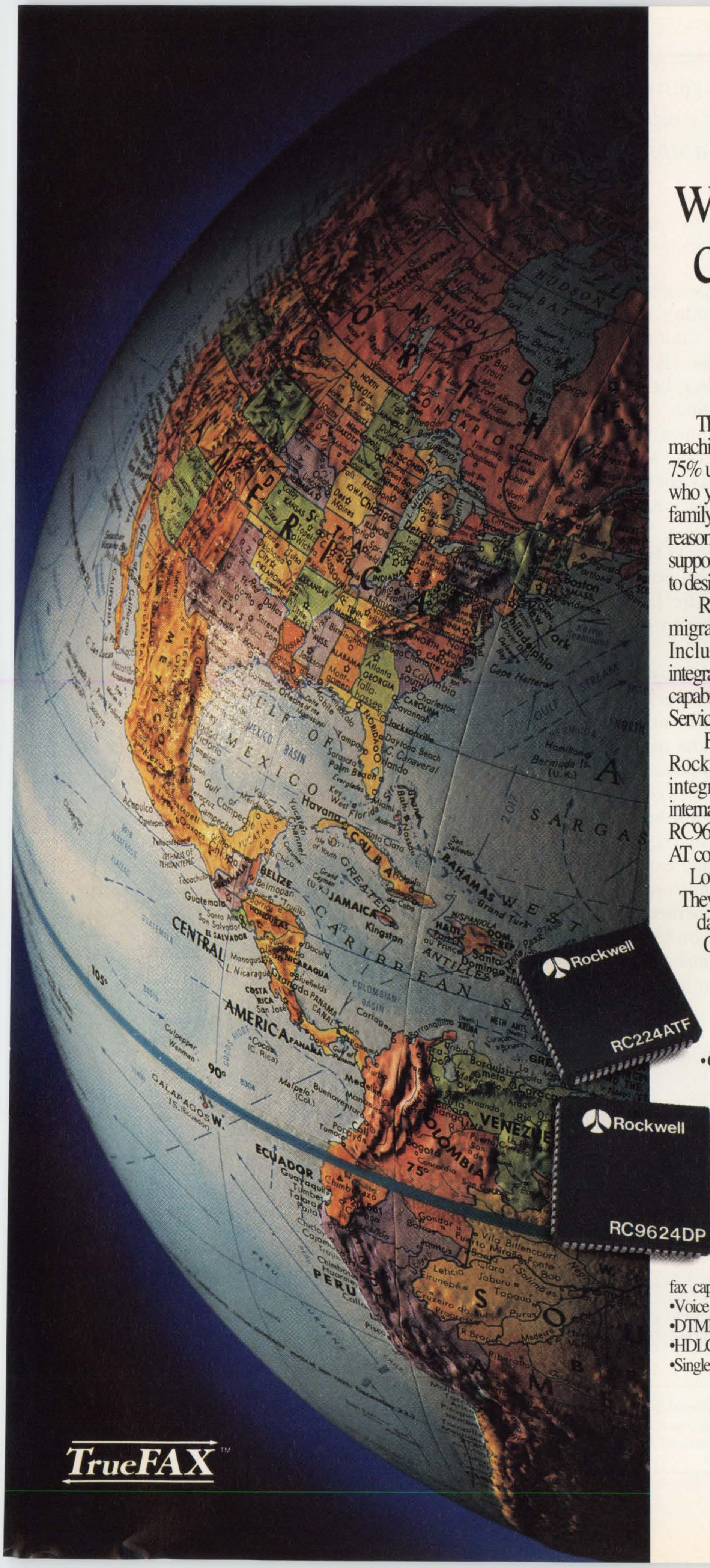


Fig 8—Switching the input of the error amplifier *to ground while the error is settling can prevent the amplifier from saturating.*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The characteristics of the flash converter determine the gain of the error amplifier. Most monolithic high-speed op amps are suitable.

that improper grounding introduces. Designers often think that their breadboard is functioning properly, but when they change the setup or the timing (repetition rate, duty cycle, or the fall and rise times of the convert command), major errors occur because of ground loops or poor grounding. In some cases, the breadboard stops functioning. **Fig 9** shows the transients on the ground of a subranging ADC with poor grounding. You can see the effects of this poor grounding by looking at the error-amplifier output and the ADC's reconstructed output.

Because the number of overlap bits limits the digital correction, poor grounding could cause an error in the first pass that exceeds the digital-correction limit. This first-pass error can cause the remainder to go out of the correction window **(Fig 10)**.

You can solve most grounding problems by separating the analog and digital grounds and connecting them only to heavy ground planes underneath or close to the flash converter. Making ground runs as wide as possible and decoupling the power supplies will also help. Note that CMOS logic and CMOS flash converters tend to magnify any grounding problems because of the large transients they cause whenever they switch. In such cases, you need to take additional care.

A major factor in the proper functioning of a subranging A/D converter is the error-correction logic, which is the Boolean algebra performed on the outputs of the first- and second-pass conversions to produce the ADC's output. This logic corrects for any first-pass

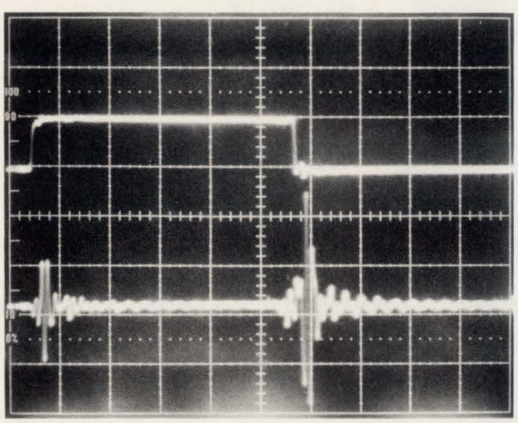

Fig 9—This photo shows the transients *on the ground of a subranging ADC that has poor grounding. The upper trace shows the signal; the bottom trace shows the analog ground with respect to the same ground at a different physical location.*

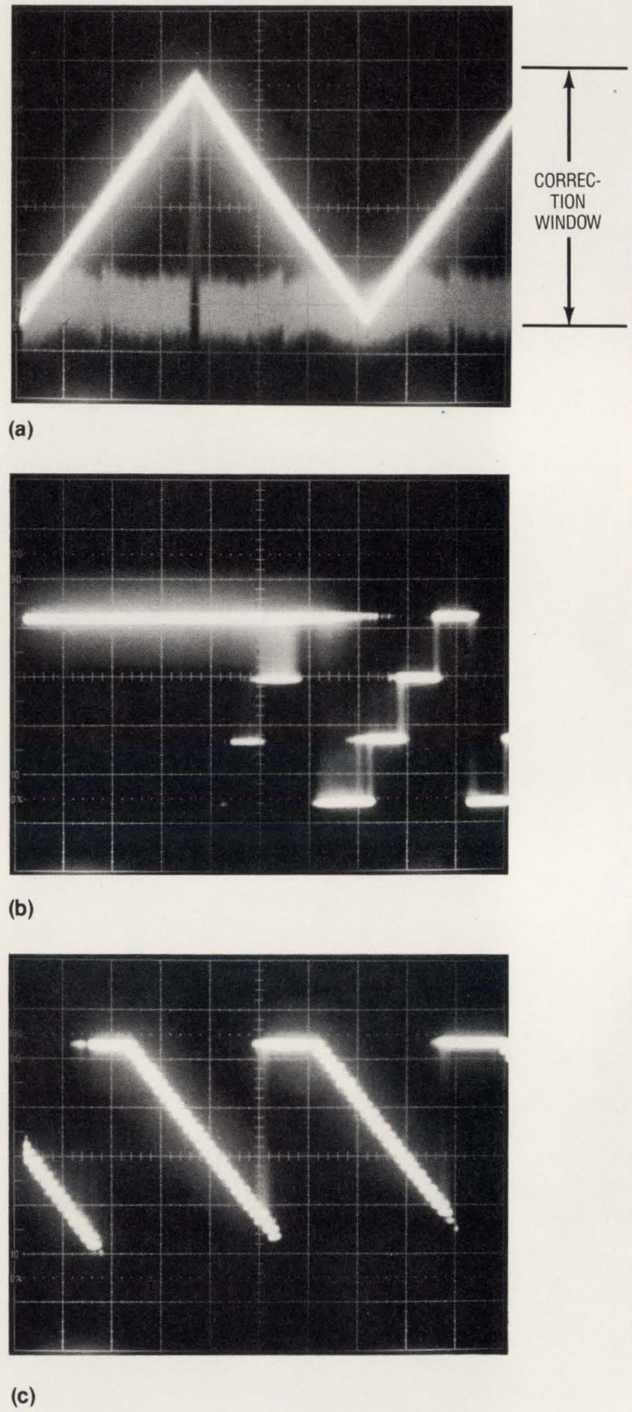

Fig 10—In this ADC, a slight change in the start-convert pulse width *caused the remainder to go out of the correction window **(a)**. Traces **b** and **c** show the resultant missing codes at the reconstructed output for a 2-bit DAC and a 5-bit DAC, respectively.*

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You can solve most grounding problems by separating the analog and digital grounds and connecting them to heavy ground planes underneath or close to the flash converter.

errors that create remainders that stay within the correction window (**Fig 11**).

Generally, the device's biasing offsets the input negatively in the first-pass conversion to ensure that the error, or remainder, is positive. A positive remainder simplifies the correction logic to an addition, which means the outputs of the first and second conversion are added to get the final output of the ADC. The way these outputs are added depends on the number of correction bits, or overlaps. For example, in the case of a 7-bit flash converter with 1 bit of correction, the ADC's output is

First-pass data:	D1	D2	D3	D4	D5	D6	D7 → overlap bit						
Second-pass data:	+						D1	D2	D3	D4	D5	D6	D7
The ADC output:	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13.

D7 in the first pass and D1 in the second pass must have the same weights to be added. If you use a 7-bit flash converter with 2 bits of correction, the ADC's output is

First-pass data:	D1	D2	D3	D4	D5	D6	D7 → overlap bits				
Second-pass data:	+					D1	D2	D3	D4	D5	D6 D7
The ADC output:	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11 B12.

In this case, D6 and D7 in the first pass must have the same respective weight as D1 and D2 in the second pass. To make sure the overlap bits have the same weight, the gain of the error amplifier must be $K=G\times2^{N-M}$, where G is the first-pass gain, N is the resolution of the first-pass flash converter, and M is the number of correction bits. In the first example, $K=G\times2^{7-1}=$

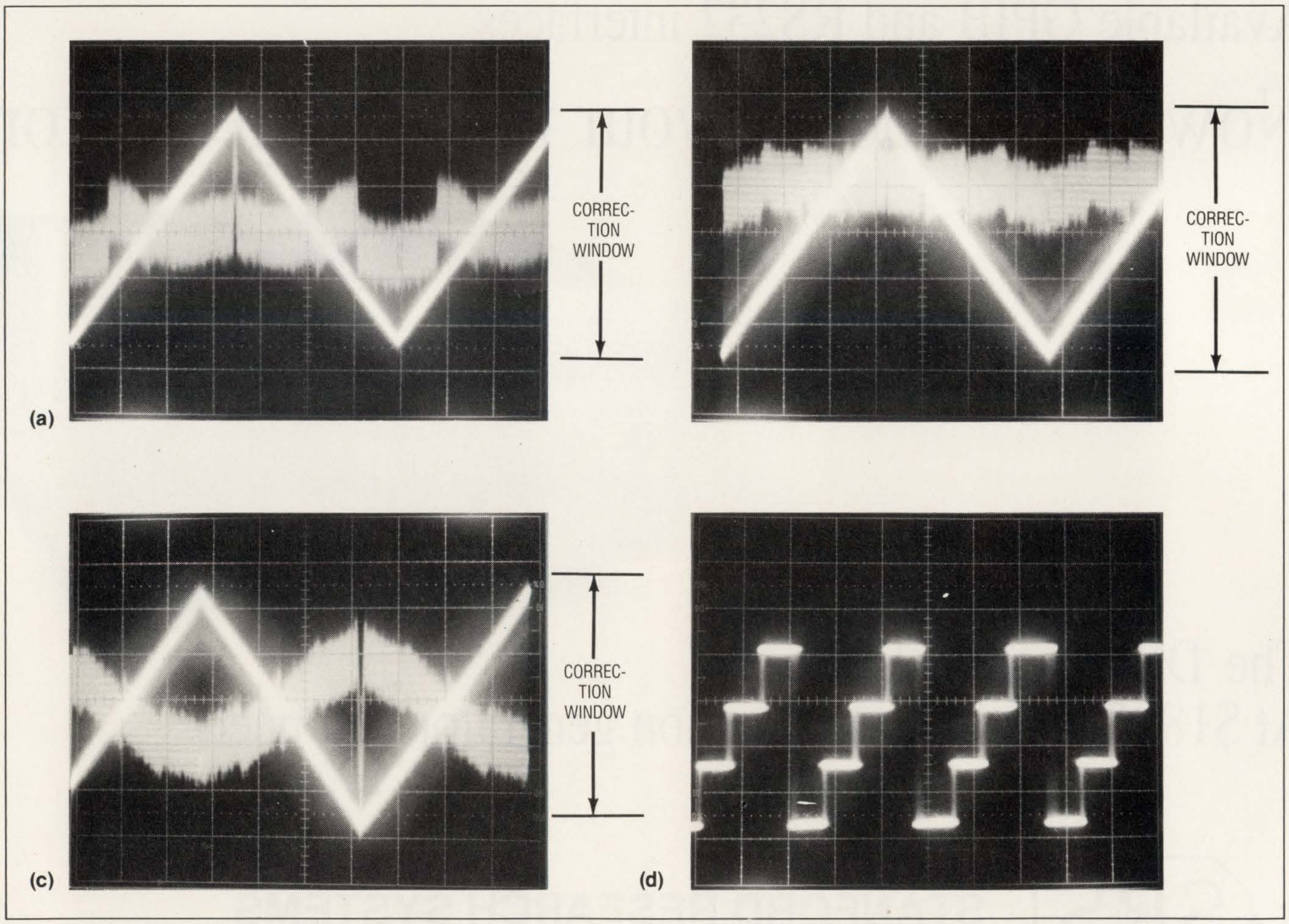
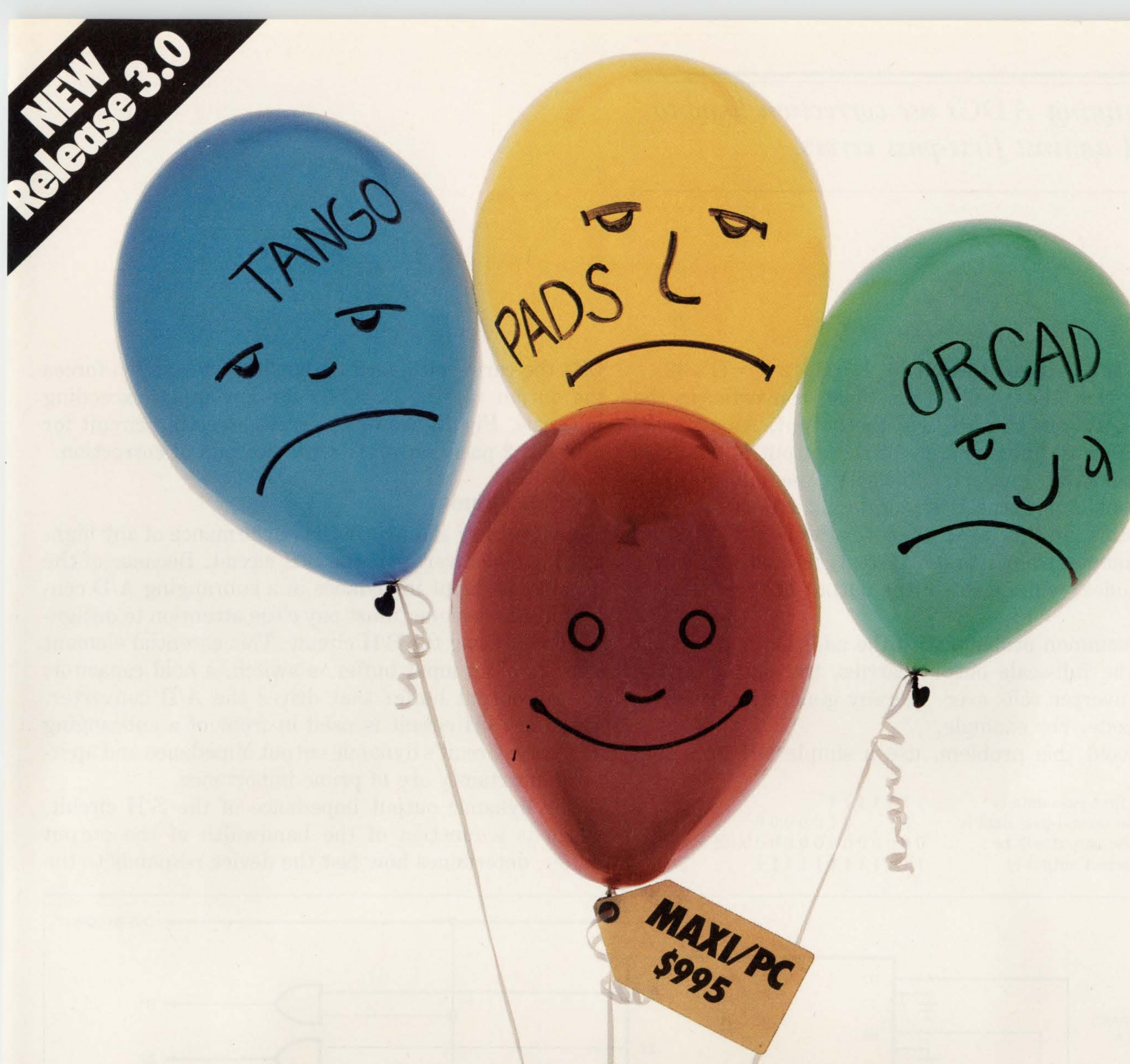


*Fig 11—**Correction logic in a subranging ADC** corrects for first-pass errors that stay within the correction window. Photos **a**, **b**, and **c** show the effects of first-pass nonlinearity, offset, and gain errors, respectively. Photo **d** shows that these errors have no effect on the reconstructed output.*



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Subranging ADCs use correction logic to guard against first-pass errors.

$G \times 64$. In the second example, $K = G \times 2^{7-2} = G \times 32$.

Note that the LSBs of the flash converter in the second pass are the LSBs of the output. As a result, the differential nonlinearity of the output is the flash converter's differential nonlinearity. The only time this statement is not true is if you do not adjust K to the right value. In this case, whenever the LSB of the first pass changes from 1 to 0 or 0 to 1, discontinuities, or noisy codes, will appear in the output of the A/D converter.

One common problem with the addition logic is that when the full-scale output carries, the output of the A/D converter rolls over, thereby generating an erroneous code. For example,

If the first-pass data is	1 1 1 1 1 1 1
and the second-pass data is	0 1 0 0 0 0 0,
then the output will be	0 0 0 0 0 0 0 0 0 0 0 0 with a carry.
The correct output is	1 1 1 1 1 1 1 1 1 1 1 1.

To avoid this problem, use a simple OR gate that ORs the carry with each output bit. This action forces the output to stay at all 1s for any input exceeding full scale. **Fig 12** shows an error-correcting circuit for a 12-bit, 2-pass converter with two bits of correction.

The S/H circuit

Another key element in the performance of any high-speed A/D converter is the S/H circuit. Because of the usually low input impedance in a subranging A/D converter, the designer must pay close attention to designing or selecting the S/H circuit. This essential element consists of an input buffer, a switch, a hold capacitor, and an output buffer that drives the A/D converter. When an S/H circuit is used in front of a subranging ADC, the circuit's dynamic output impedance and aperture uncertainty are of prime importance.

The dynamic output impedance of the S/H circuit, which is a function of the bandwidth of the output buffer, determines how fast the device responds to the

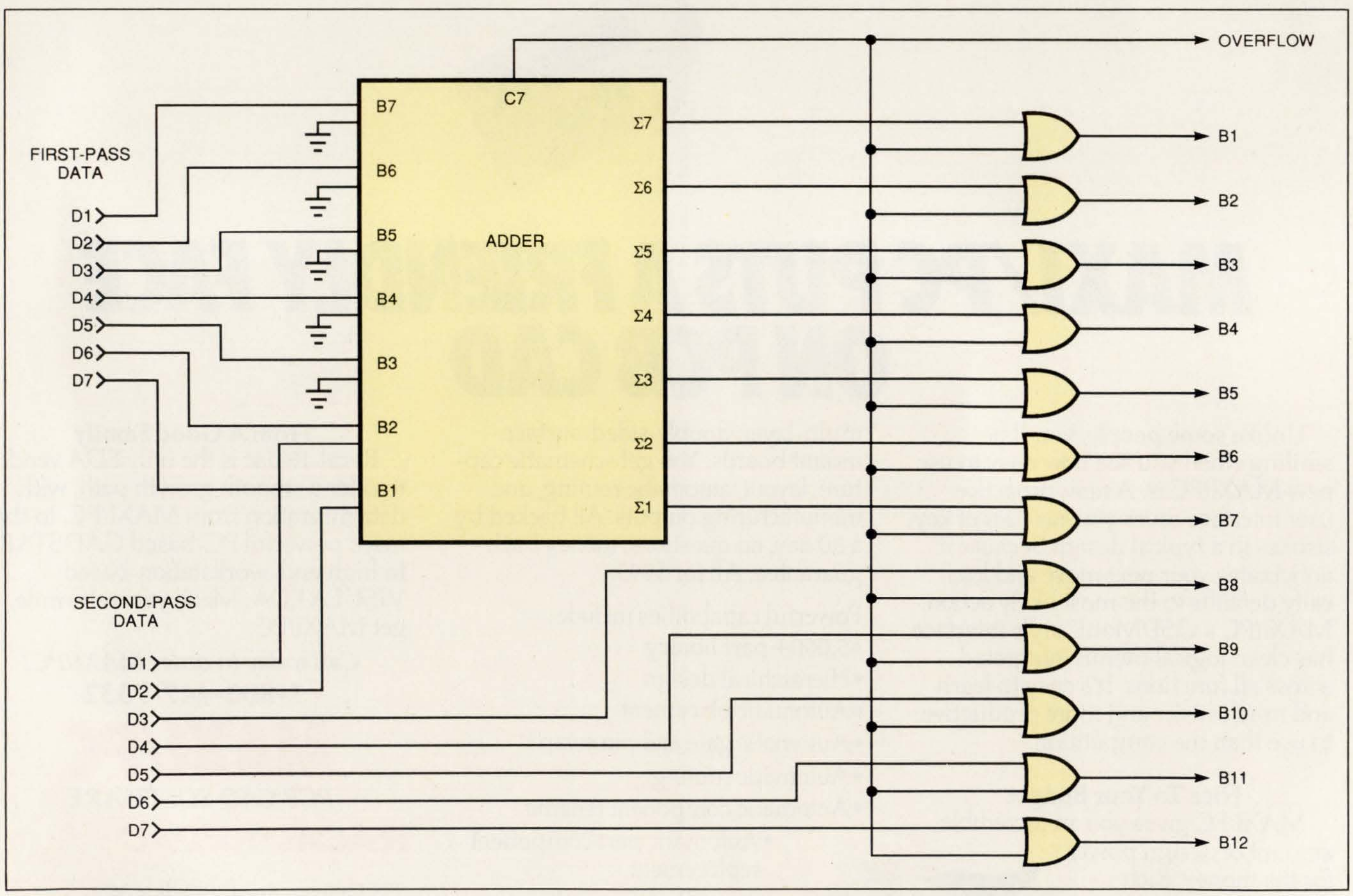
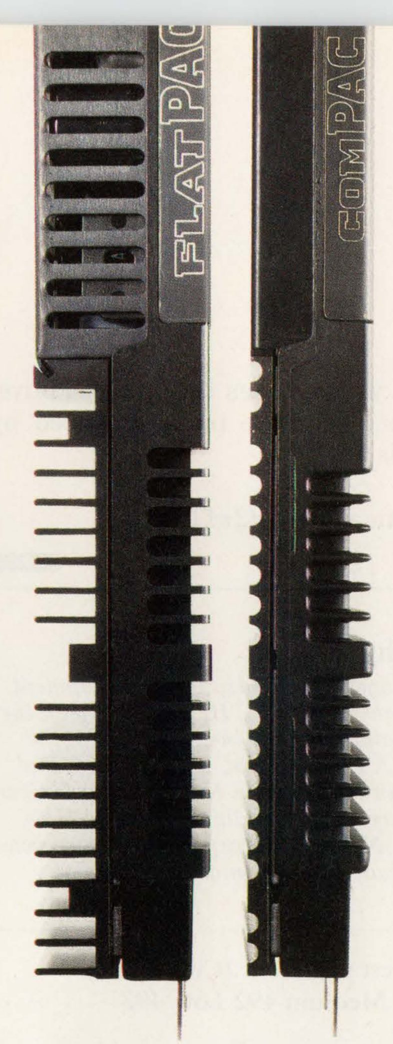


Fig 12—This diagram shows the error-correction logic *for a 12-bit, 2-pass converter with two bits of correction.*



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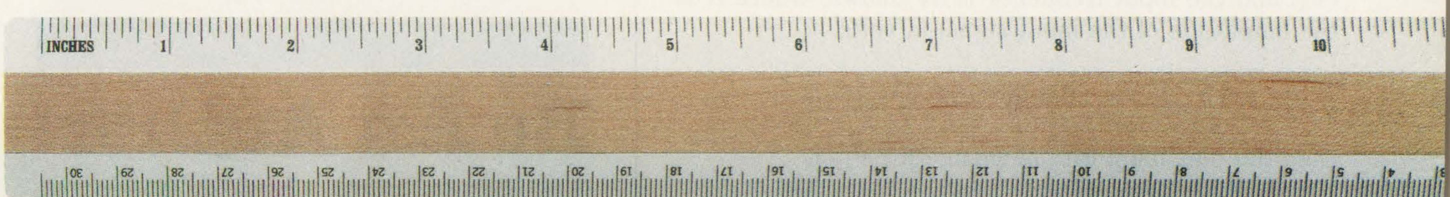

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Subranging ADCs are the most challenging ADCs to design and manufacture.

dynamic load it drives. Because of subranging ADCs' low input impedance and the switching that takes place on the input, the devices require a S/H circuit with a low dynamic output impedance to attain an optimal conversion time.

For precision A/D converters, try to avoid open-loop S/H circuits. The gain of open-loop S/H circuits changes drastically with input frequency and amplitude, and most noticeably with the output load. Any of these factors can cause large static and dynamic errors.

Another error source is the aperture uncertainty, which is the uncertainty period associated with the closing of a switch. Many factors contribute to this error source. The most common are timing jitter caused by random noise, 60-Hz line frequency or other frequencies modulating the power lines, and the uncertainty of the sample command. The ADC's output takes on the spectral characteristics of the error source. The aperture uncertainty also limits the input frequency that the circuit can sample within the specified error budget. The relationship between aperture uncertainty (T_A) and the input frequency is as follows, where A is the amplitude of the input signal in volts:

$$\text{If } V_{IN}=A\cdot\sin(\omega t)=A\cdot\sin(2\pi f_t),$$

then the maximum rate of change for V_{IN} is

$$\frac{dV_{IN}}{dt}=\frac{dA\ \sin(2\pi f_t)}{dt}\Bigg|_{t=0}=2A\pi f\cos(2\pi f_t)\Bigg|_{t=0}$$

$$\left(\frac{dV_{IN}}{dt}\right)_{MAX}=2A\pi f.$$

Aperture-uncertainty noise generally follows a Gaussian distribution similar to white noise, which means that the rms aperture uncertainty corresponds to the distribution's σ value. The distribution's 2σ point thus becomes the proper choice for the maximum value. The maximum aperture uncertainty equals $2T_A$. To determine the maximum full-scale sine-wave frequency (f_{MAX}) that produces ½-LSB error, first calculate the error arising from $2T_A$:

$$2T_A\ \text{error}=2(T_A)_{MAX}(dV_{IN}/dt)=2T_AA2\pi f_{MAX}.$$

Thus,

$$f_{MAX}=1/T_A\pi 2^{n+2}.$$

The error resulting from the aperture uncertainty is primarily random, which makes the noise additive. The general expression for the noise produced by Gaussian time jitter is

$$\text{S/N ratio}=-20\log(2\pi fT_A).$$

EDN

Author's biography

Ray Ushani is the manager of the Advanced Development Group at Datel Inc (Mansfield, MA). He has been with the company for six years and has been instrumental in the development of several A/D converters, multiplexers, and S/H circuits. Ray has an MSEE from Northeastern University (Boston, MA) and is a PhD candidate at Tufts University (Medford, MA). Not one to stray far from his vocation, Ray's hobbies include RF and microwave design.

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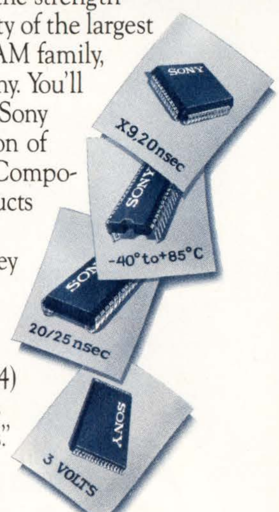
	Model	Speed (ns)	Packaging	Data Retention Current	Special Features	Availability
128Kx8	CXK581000P	100/120/150	DIP 600mil	L/LL	B/X	Now
	CXK581000M	100/120/150	SOP 525mil	L/LL	B/X	Now
	CXK581100TM	100/120/150	TSOP	L/LL	B/X	Now
	CXK581100YM	100/120/150	TSOP (reverse)	L/LL	B/X	Now
	CXK581001P	70/85	DIP 600mil	L/LL		Now
	CXK581001M	70/85	SOP 525mil	L/LL		Now
	CXK581020SP	35/45/55	SDIP 400mil			Now
	CXK581020J	35/45/55	SOJ 400mil			Now
128Kx9	CXK77910J	20	SOJ 400mil		Sync ASM	2H '91
256Kx4	CXK541000J	25/30/35	SOJ 400mil			2H '91

L = Low LL = Low, Low B = 3 Volt X = Extended Temperature



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LINEAR TECHNOLOGY DESIGN NOTES

Current Feedback Amplifier "Do's and Don'ts" – 46

William H. Gross

Introduction

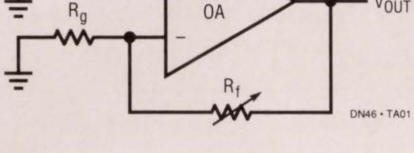
The introduction of current feedback amplifiers, such as the LT1223, has significantly increased the designer's ability to solve difficult high speed amplifier problems. The current feedback architecture has very high slew rate and the small signal bandwidth is fairly constant for all gains. Current feedback amplifiers are used in broadcast video systems, radar systems, IF and RF stages, RGB distribution systems and many other high speed circuits.

As with any new circuit, there are several new rules that must be kept in mind to prevent problems. Because current feedback amplifiers act very much the same as regular op amps, it is important to note the differences and show how some standard op amp circuits should be implemented.

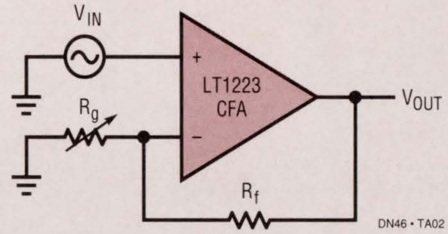
The most important thing to remember about current feedback amplifiers is that the impedance at the inverting (negative) input sets the bandwidth and therefore the stability of the amplifier. It should be resistive, not capacitive. To slow the amplifier down, increase the resistance driving the inverting input. If the amplifier peaks too much due to capacitive loading, or anything else, increase the value of the feedback resistors.

The best way to demonstrate how to use current feedback amplifiers is to show some example circuits. To make it as painless as possible, I will show the traditional op amp implementation next to the current feedback amplifier version.

Op Amp Adjustable Gain Amp

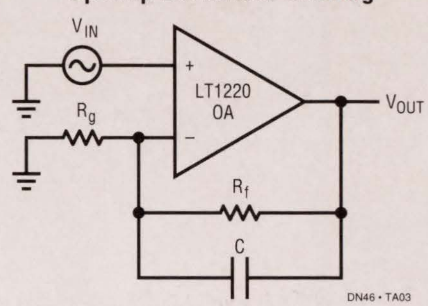


Current Feedback Amp Adjustable Gain Amp

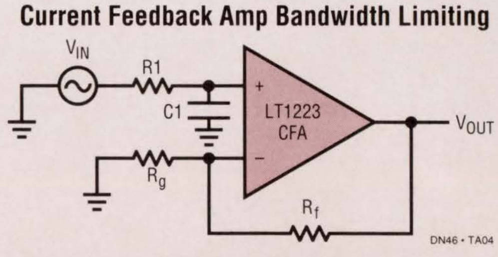


With a standard op amp you can vary the gain of the amplifier with either R_f or R_g. The only real restriction on the values is the loading affect the resistors have on the amplifier output. With a current feedback amplifier the value of R_f should not be varied. If R_f is a pot, then the bandwidth will be reduced at minimum gain and the circuit will oscillate when R_f is very small.

Op Amp Bandwidth Limiting

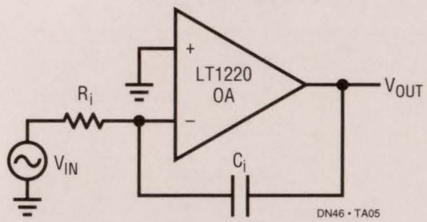


Current Feedback Amp Bandwidth Limiting

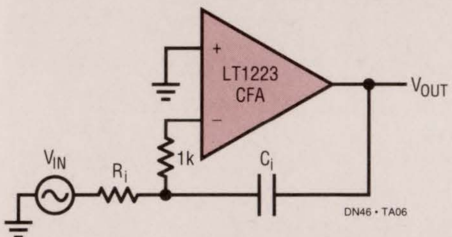


It is very common to limit the bandwidth of an op amp by putting a small capacitor in parallel with R_f. This works with all unity gain stable op amps; DO NOT PUT A SMALL CAPACITOR FROM THE INVERTING INPUT OF A CURRENT FEEDBACK AMPLIFIER TO ANYWHERE, ESPECIALLY NOT TO THE OUTPUT. The capacitor on the inverting input will cause peaking or oscillations. If you need to limit the bandwidth of a current feedback amplifier, use a resistor and capacitor at the non-inverting input (R1 and C1). This technique will also cancel (to a degree) the peaking caused by stray capacitance at the inverting input. Unfortunately, this will not limit the output noise the way it does for the op amp.

Op Amp Integrator

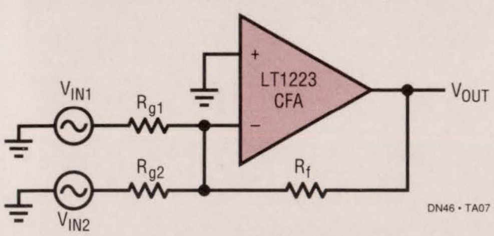


Current Feedback Amplifier Integrator



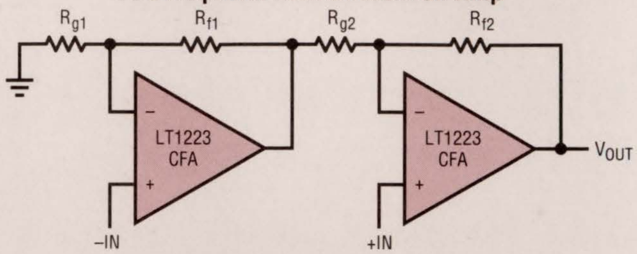
The integrator is one of the easiest circuits to make with an op amp. However, the circuit must be modified before a current feedback amplifier can be used. Since we remember that the inverting input wants to see a resistor, we can add one to the standard circuit. This generates a new summing node where we can apply capacitive feedback. The new current feedback amplifier compatible integrator works just like you would expect; it has excellent large signal capability and accurate phase shift at high frequencies.

Current Feedback Amplifier Summer (DC Accurate)



There is no I_{OS} spec on current feedback amplifiers because there is no correlation between the two input bias currents. Therefore we will not improve the DC accuracy of the inverting amplifier by putting an extra resistor in the non-inverting input. This is also true of input bias current canceled op amps where the I_{OS} spec is the same as the I_B spec, such as the LT1220.

Two Amplifier Instrumentation Amp



TRIM R_{g2} FOR GAIN, THEN TRIM R_{g1} FOR CMRR. VOLTAGE GAIN, G, IS V_{OUT} DIVIDED BY DIFFERENCE BETWEEN +IN AND –IN.

OP AMP DESIGN EQUATIONS:

$R_{f1} = R_{g2}$; $R_{f2} = (G-1)\,R_{g2}$; $R_{g1} = R_{f2}$

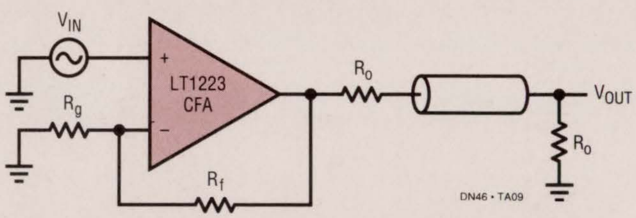
CURRENT FEEDBACK AMP DESIGN EQUATIONS:

$R_{f1} = R_{f2}$; $R_{g1} = (G-1)\,R_{f2}$; $R_{g2} = \frac{R_{f2}}{G-1}$

DN46 • TA08

The two amplifier instrumentation amp is easily modified for current feedback amplifiers. The only necessary change is to make the feedback resistor of each amplifier the same and therefore make the gain setting resistors different. This way the bandwidth of both amps is the same and the common mode rejection at high frequencies is better than that of the op amp circuit. In the op amp circuit one amplifier has maximum bandwidth, since it runs at about unity gain, while the other is limited to its gain bandwidth product divided by the gain.

Cable Driver



The cable driver circuit is the same for both types of amplifiers. But because most op amps do not have enough output drive current, they are not often used for heavy loads like cables. When driving a cable it is important to properly terminate both ends if even modest high frequency performance is required. The additional advantage of this is that it isolates the capacitive load of the cable from the amplifier so it can operate at maximum bandwidth.

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8051 converts 16-bit integer to BCD

Jeremy Ottenstein
Allied Signal Aerospace Corp, Teterboro, NJ

For an 8051 μP, converting a 16-bit binary integer to decimal form is considerably more complicated than converting an 8-bit integer. The most straightforward method uses a 16-bit-divide routine. **Listing 1**'s alternative method takes advantage of the 8051's BCD commands. Using the BCD commands results in simple and clean code.

The **listing** is for the Boston Systems Office (Waltham, MA) 8051 macro assembler. Its macro definitions differ somewhat from Intel's. The **listing** uses (r0, r1) and (r2, r3, r4) for the input and output, respectively; but you can use any five 8051 registers or any five internal-direct memory locations. You can obtain the **listing** from the EDN BBS. Phone (617) 558-4241 with modern settings 300/1200/2400, 8, N, 1. From the main menu, enter (s)ig, <s/di_sig>, rk946).
(EDN BBS /DI_SIG #946) **EDN**

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Listing 1—8051 Radix-conversion routine

```
        title   cnvbcd


; Listing controls
$  nocond
$  genonly


rlc16   macro   %x1, %x2
; Performs a 16-bit rotate left through the Carry flag.
        mov     a, %x2
        rlc     a
        mov     %x2, a
        mov     a, %x1
        rlc     a
        mov     %x1, a
        endm


clrbcd  macro   %x1, %x2, %x3
; Initializes the packed bcd digits.
        mov     %x3, #0
        mov     %x2, #0
        mov     %x1, #0
        endm


incbcd  macro   %x1, %x2, %x3
; Increments the packed bcd digits by 1, if the carry is set.
        mov     a, %x3
        addc    a, #0
        da      a
        mov     %x3, a

        mov     a, %x2
        addc    a, #0
        da      a
        mov     %x2, a

        mov     a, %x1
        addc    a, #0
        da      a
        mov     %x1, a
        endm


dblbcd  macro   %x1, %x2, %x3
; Doubles the packed bcd digits.
        mov     a, %x3
        add     a, %x3
        da      a
        mov     %x3, a

        mov     a, %x2
        addc    a, %x2
        da      a
        mov     %x2, a

        mov     a, %x1
        addc    a, %x1
        da      a
        mov     %x1, a
        endm


cnvbcd:

; CNVBCD accepts a 16-bit unsigned binary integer and converts it into
; 5 packed bcd digits.

; The input is passed in (r0,r1).
; The output is returned in (r2,r3,r4).

; Note : The contents of R0 & R1 are destroyed at the end of this routine.

;* The following algorithm is used.
;* See Knuth, "The Art of Computer Programming", Vol 2, 1981
;* Section 4.4, Radix Conversion.

;* y := 0 ;
;* for i := 1 to 15 do
;*   y := y + x[16-i] ;
;*   y := y * 2 ;
;* end do ;
;* y := y + x[0] ;


        mov     r7, #15
        clrbcd  r2, r3, r4

1$:     rlc16   r0, r1
        incbcd  r2, r3, r4
        dblbcd  r2, r3, r4
        djnz    r7, 1$

        rlc16   r0, r1
        incbcd  r2, r3, r4

        ret

        end
```

Pause detector adapts to signal

Tibor Szep and Andras Pomozi
Technical University of Budapest, Budapest, Hungary

You can increase the throughput of a LAN's data transmission if you transmit only during the talk-spurt period. If your detector is sensitive enough, even the pause among the words can be utilized for data transmission. The circuit in **Fig 1** distinguishes between the signal and pause states in a speech signal coming from the microphone of a telephone handset. The circuit is adaptive because the threshold level of the comparator depends on the long-time average of the speech signal's power. The detector can also accommodate background noise. Even in cases of massive continuous background noise, the detector can distinguish the signal state from the nonsignal state.

Fig 1 consists of four major parts: a 2-way precision rectifier, an integrator with two time constants, a long-time integrator, and a comparator. The rectifier produces the absolute value of the incoming speech signal. R_1 controls the gain. The rectifier's output drives the integrator. The integrator's rise is determined by τ_1 which is approximately equal to $R_2 \times C_1$. τ_2 which is approximately equal to $R_3 \times C_1$ determines the fall time. R_5 and R_6 eliminate the op amp's offset. Two time constants are necessary because the requirements for defining the beginning and the end of a speech period are different. The circuit must be able to detect quickly the beginning of a speech period; determining the end of an active period isn't as critical. Also, making the fall time somewhat longer than necessary avoids biting off the end of a word.

The long-time integrator's time constant (τ_3) equals $R_4 \times C_2$. A potentiometer controls the threshold level of the comparator. Speech quality depends on the values of all three time constants. **(EDN BBS /DI_SIG #937)**

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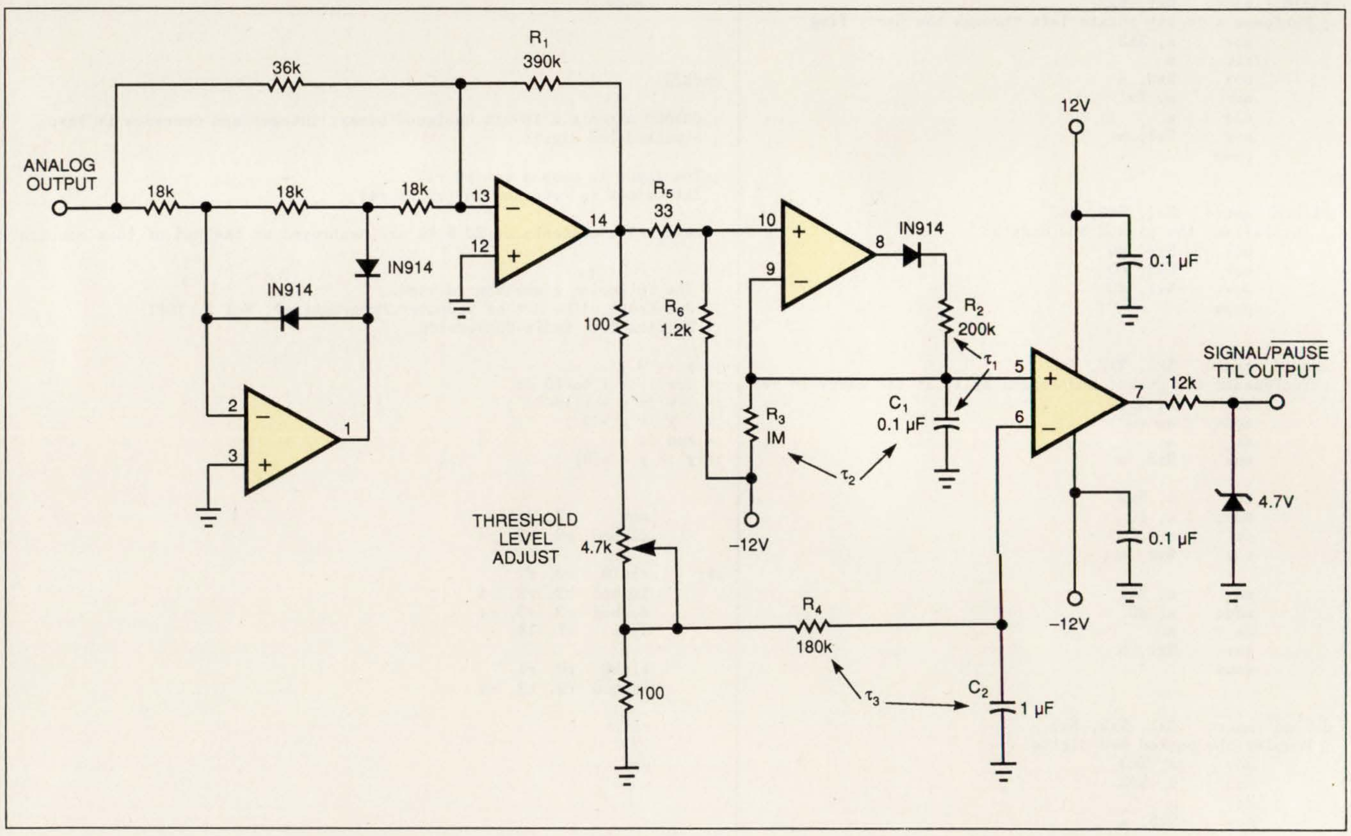
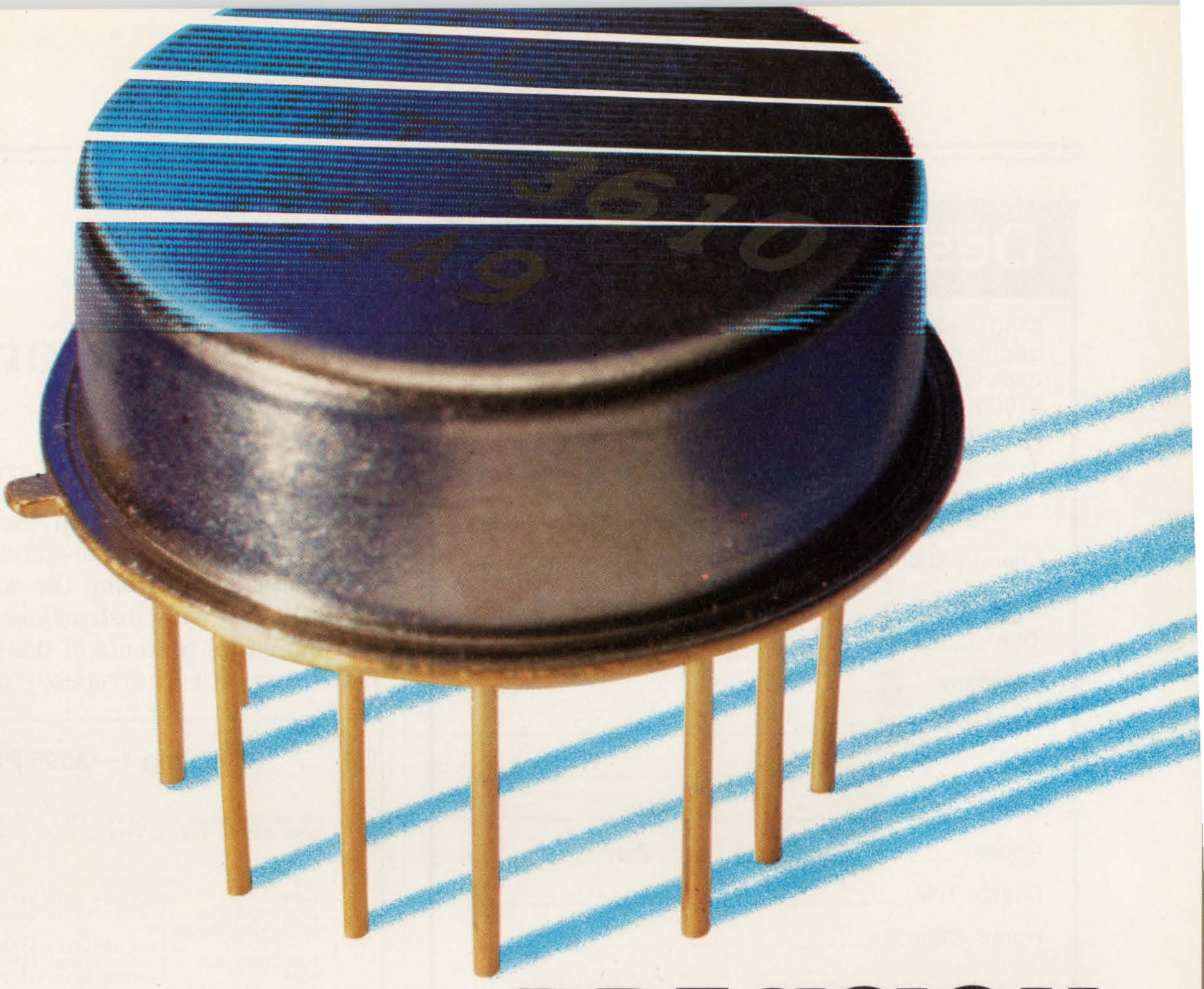


Fig 1—Three independently adjustable time constants, *τ_1, τ_2, and τ_3, allow this pause detector to define the beginning and end of a speech period and allow it to adapt to speech signal levels.*



ISSUE WINNER

The winning Design Idea for the January 21, 1991 issue is entitled "Digital recorder speeds sampling rate," submitted by Lin Jun of Changchun University of Earth Sciences (Changchun, Jilin, Peoples Republic of China).

Your vote determines this issue's winner. All designs published win $100 cash. All issue winners receive an additional $100 and become eligible for the annual $1500 Grand Prize. **Vote now**, by circling the appropriate number on the reader inquiry card.

Macro fixes 8096 shortcoming

John N Liddy
Simplex Time Recorder, Gardner, MA

An obvious shortcoming of the 8096 μP is that you cannot save the program-status word (PSW) on the stack without disturbing the working copy stored in the PSW. The only instructions available that can access the entire contents of the PSW are PUSHF and POPF; these two instructions push and pop the contents of the PSW. However, the PUSHF instruction not only pushes the contents of the PSW onto the stack, it also clears the entire PSW. Clearing the PSW causes several undesirable events, including disabling interrupts and clearing all the flags. This idiosyncrasy can be quite annoying when all you want is to save the contents of the carry flag for future use.

Listing 1—8096 PSW macro

```
;
;     SP is the word register (18H) which contains the stack address
;     WORD_REG is any general purpose word register (20H - 0FFH)
;

PUSH_PSW  MACRO      WORD_REG
      PUSHF          ;push psw onto stack (clears working psw)
      PUSH WORD_REG  ;save contents of word register on stack
      LD   WORD_REG,2[SP]
                     ;load register with original PSW contents
      PUSH WORD_REG  ;push original PSW contents onto stack again
      POPF           ;restore original PSW contents
      POP  WORD_REG  ;restore word register from stack
```

The macro in **Listing 1** will save the PSW on the stack without altering the PSW's working value. If you use this macro in a time-critical, interrupt-driven application, be aware that for 93 clock cycles, this macro will disable interrupts. For a 12-MHz clock, interrupts will be off for 7.75 μsec. You could lower this interval by not saving the general-purpose-word register, thereby lowering interrupt latency to 5.75 μsec. **(EDN BBS /DI_SIG #949)** EDN

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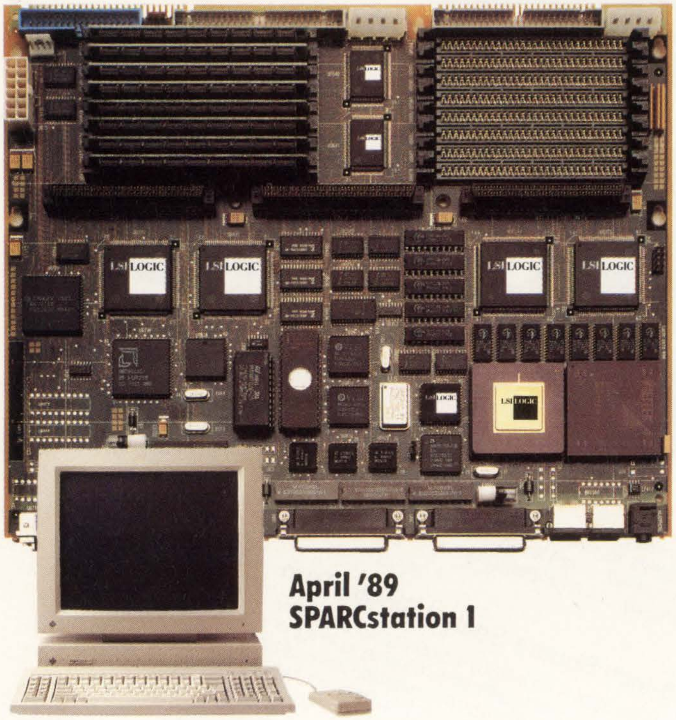

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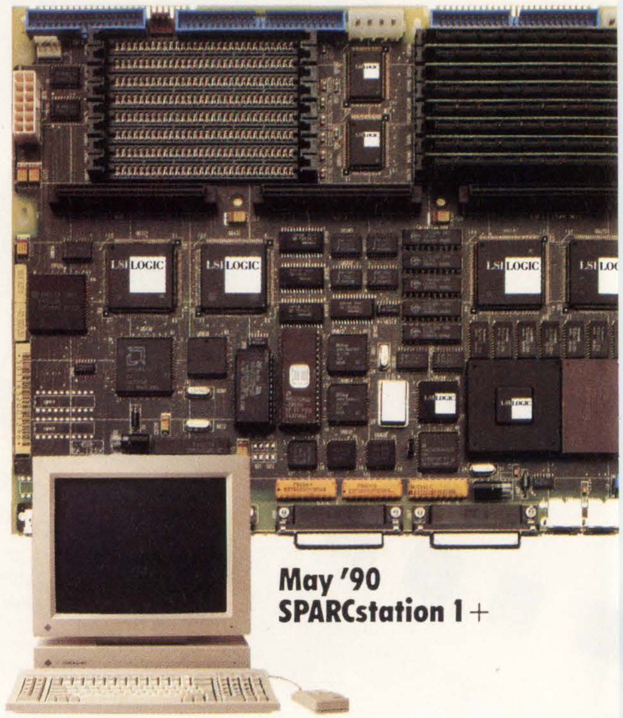
SPARCstation 1



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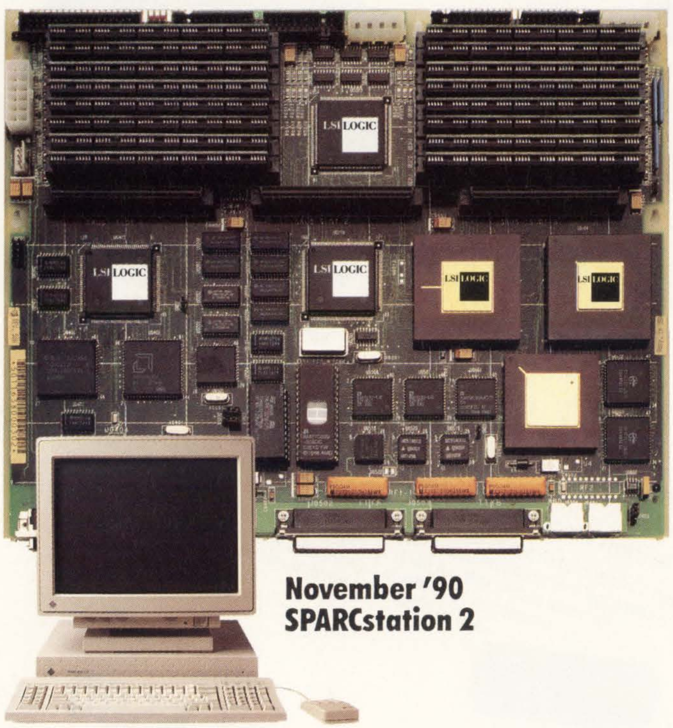

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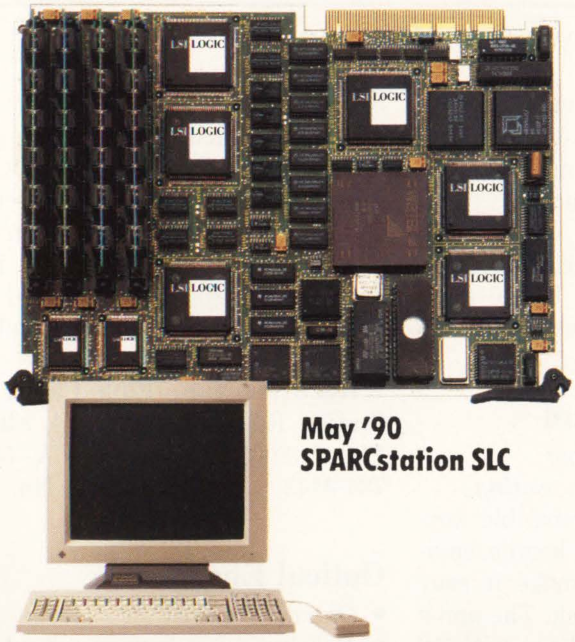

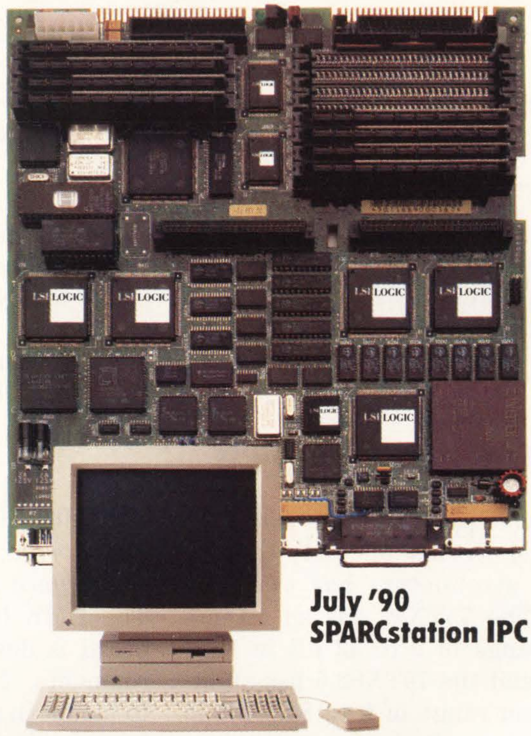

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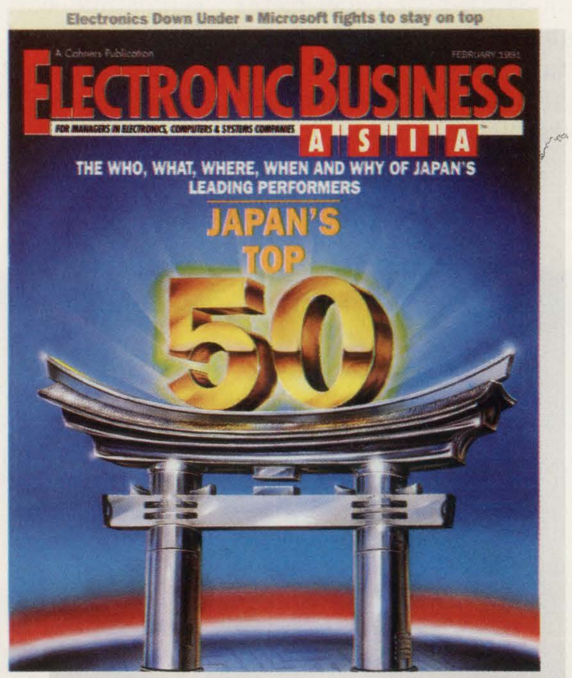

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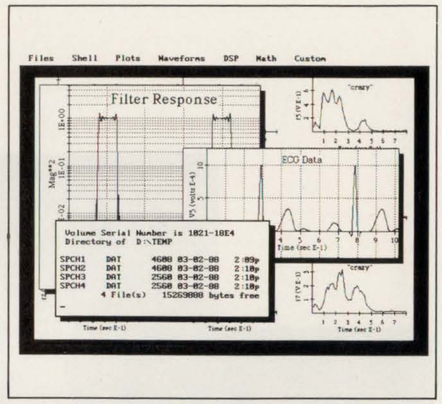

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CIRCLE NO. 155

with either a mouse or the keyboard. You can create multiple graphics windows for data display. Binary data pipes link processing modules implemented as executable (.EXE) files; you can add any number of your own modules, which can be written in any language that supports the standard DOS file system I/O. DSP utility modules included with the software are forward and inverse FFT routines; convolution; correlation; window generation; FIR and IIR filter design and implementation; derivatives and integrals; test-data generation (sinusoidal, rectangular, impulse, triangular, uniform-random, and Gaussian-random data); and real and complex math functions. Multistage transformations such as Cepstrum and Hilbert transforms are available by combining basic operations in data pipes. The software includes data-acquisition routines but does not allow continuous real-time processing. $185; demo disk, $10.

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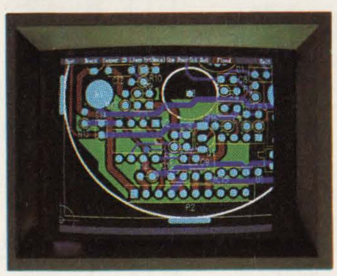

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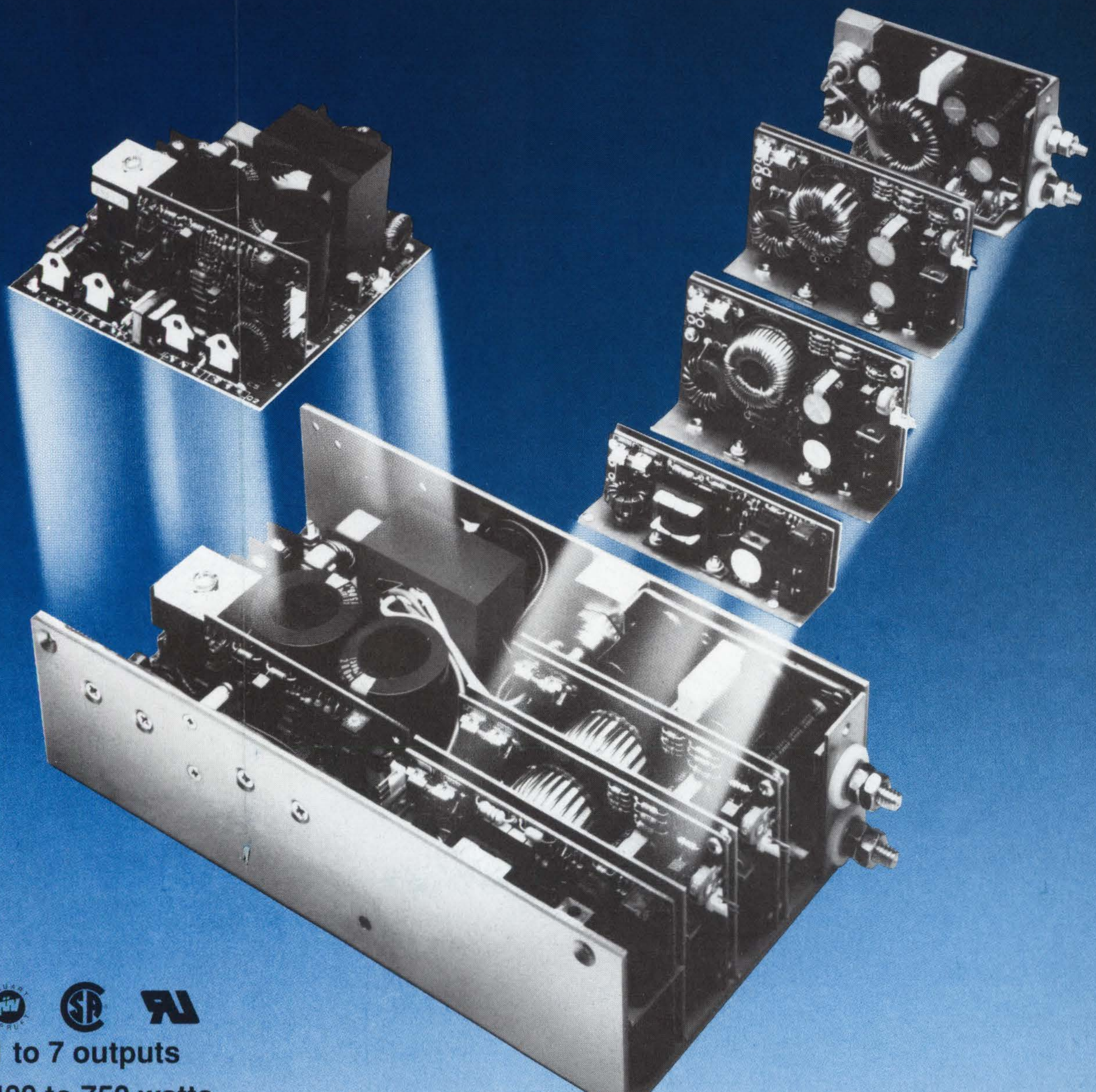

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N	Super Main

M Type Main Module Ratings		
Power Rating	Current Multiplier	
	Single	Multiple
400W	0.8	0.6
500W	1.0	0.8
600W	1.2	1.0
750W	N/A	1.2

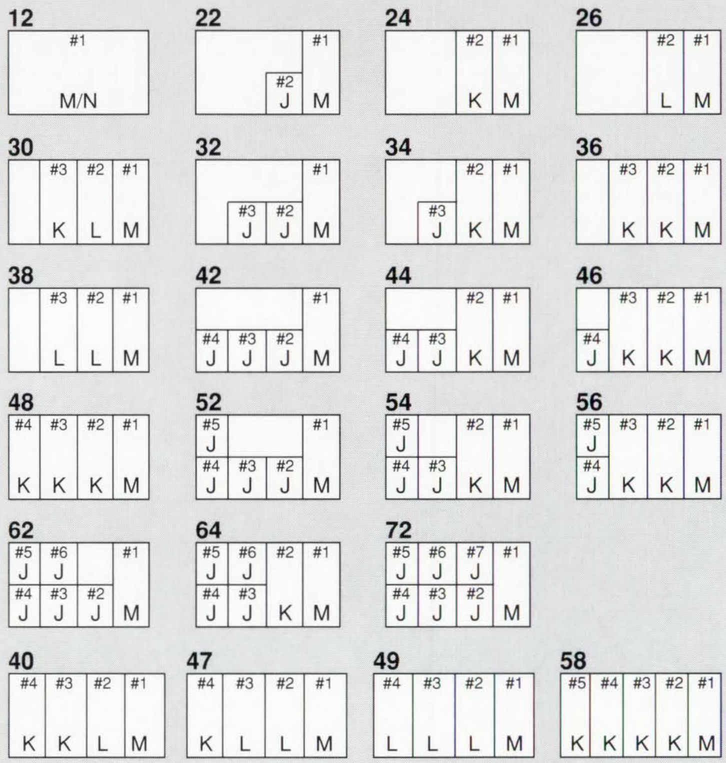
Options	
Option Code	Function
01	Power Fail Monitor
02	Auto Ranger
04	Pilot Bias
08	Active Surge Limit
16	Redundant
32	Cover
64	Fan Cover

Options 02, 04, 08 mutually exclusive.

Output Modules							
Output		Type					
Code	Volts	J Amps	K Amps	L Amps	R Amps	M Amps	N Amps
0	2	10	20	30	40	100	150
1	3.3	10	20	30	40	100	150
2	5	10	20	30	40	100	150
3	12	6	12	24	17	42	62
4	15	5	10	20	13	33	50
5	18	4	8	16	11	28	42
6	24	3	6	12	9	21	31
7	28	2.5	5	10	7	18	27
8	36	2	4	8	6	14	21
9	48	1.5	3	6	4	10	16
A	2.2	10	20	30	40	100	150
B	2.4	10	20	30	40	100	150
C	2.7	10	20	30	40	100	150
D	3	10	20	30	40	100	150
E	3.6	10	20	30	40	100	150
F	4	10	20	30	40	100	150
G	4.5	10	20	30	40	100	150
H	5.7	10	20	30	36	90	135
J	6.3	10	20	30	32	80	120
K	7	9	18	30	28	70	105
L	8	8	16	30	25	62	93
M	9	8	15	30	22	56	84
N	10	7	14	30	20	50	75
P	11	7	13	27	18	45	68
Q	13.5	6	11	22	15	37	56
R	17	5	9	18	12	30	45
S	19	4	8	16	11	26	39
T	21	4	7	14	10	24	36
U	23	4	7	13	9	22	33
V	26	3	6	12	8	19	29
W	29	3	5	10	7	17	26
X	32	2	5	9	6	16	24
Y	40	2	4	8	5	13	20
Z	44	2	4	7	5	12	18

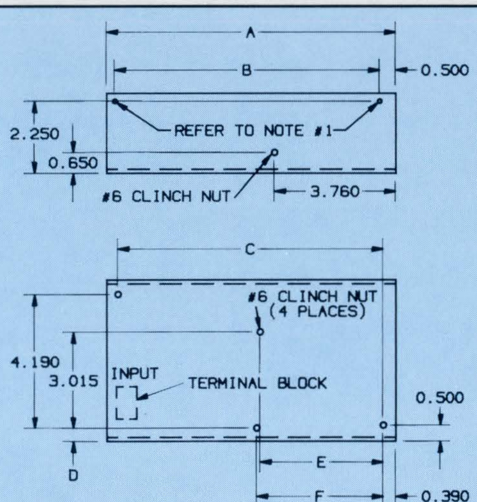
For multiple output modules of a given type, voltages are arranged in ascending order by magnitude in the same sense as the output number sequence. Shaded ratings are stock, others available on special order.

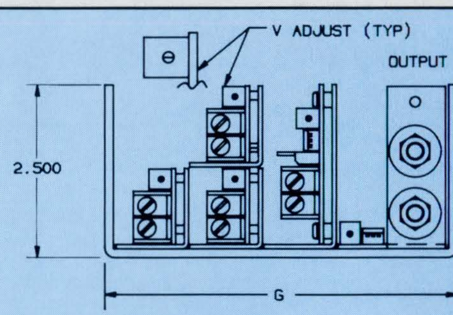
Output Configurations
Output #1 can be Type K, L, R, M. For singles, M or N only.



The boxes above are diagramatic representations of the power supplies as viewed from the output end. The two digit numbers above the boxes are the configuration codes. Configurations 40,47, 49 and 58 – Power Code D, Case 3. Configurations 26, 30 and 38 – Power Codes C and D, Case 2. Remaining configurations – Power Codes A, B, C and D, Cases 1 and 2.

M/DM SERIES DIMENSIONS





(1) With cover (#6-32), W/O cover (.150 dia.)
(2) W/fan cover unit height (4.100)
(3) Terminal Blocks (#6-32)
(4) Studs (1/4-20)

	Case 1	Case 2	Case 3
	400/500 W	600/750 W	600/750 W
A	9.000	9.630	9.630
B	8.25	8.880	8.880
C	8.260	8.890	8.890
D	.410	.425	1.725
E	3.820	4.450	4.450
F	3.930	4.560	4.560
G	5.050	5.200	6.500

DESCRIPTION

Moduflex switchers form a comprehensive line of open frame power supplies assembled from standard "off the shelf" modules. These subunits and assembly hardware are pre-approved by safety agencies so that certifications can automatically apply to custom models. Additional advantages include first piece delivery within two weeks and the elimination of engineering costs for qualified "OEM" requirements using stock modules.

The M and DM Series offers the highest power density available in the industry, delivering 6 watts per cubic inch at an ambient temperature of 50°C. The design features "State of the Art" topology, a meticulous thermal structure and the use of high efficiency circuits and components to attain the desired power density.

The modular system concept reduces manufacturing to simple submodules, capable of high volume production with a superior quality level.

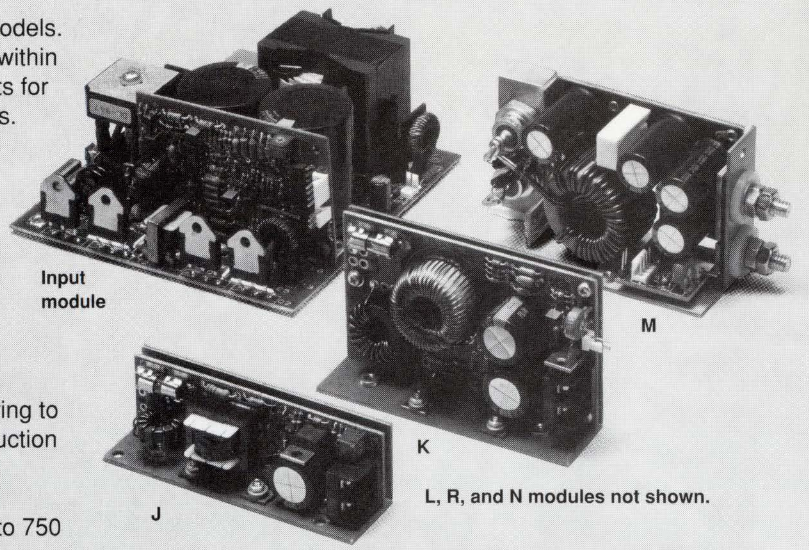
M Series are available in power ratings from 400 to 750 watts with only a slight size increase. This power versatility permits system expansion without the need for extra power supply space. DM Series available in power ratings of 400 or 600 watts.

FEATURES

- TUV, UL, CSA.
- 6 watts per cubic inch.
- 400-750 watts output.
- 120 kilohertz MOSFET design.
- Current mode control.
- All outputs:
  - *Adjustable*
  - *Fully regulated*
  - *Floating*
  - *Overload and short circuit proof*
  - *Overvoltage protected*
- Standard features include:
  - *System inhibit*
  - *Load proportional DC fan output*
- Options include:
  - *Auto ranger for continuous input operation*
  - *Power fail monitor*
  - *Independent pilot bias*
  - *Cover*
  - *Fan cover*
  - *Active surge limit*
  - *Redundant operation*

MODEL SELECTION

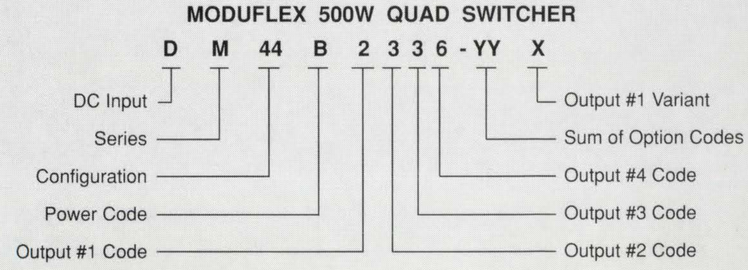
Input modules are available in ratings of 400, 500, 600, and 750 watts with corresponding code letters A through D. See Power Codes chart opposite.



Output modules are available in six types J, K, L, R, M and N in nominal power outputs of 75, 150, 300, 200, 500 and 750 watts respectively. Type M or main output modules are variable power rated depending upon the power level of the input module. This is reflected in the rating table opposite which shows the corresponding multiplier applicable to the output current ratings of the M module as a function of the power rating of the input module. For example, a 750 watt multiple will have its M type module configured to produce 600 watts of output. The ratings of output modules are given in the table of output types. Ratings in shaded areas are stocked for fast delivery.

HOW TO ORDER

To form the proper model number defining a custom requirement, select the letter M to designate the series, then choose the desired configuration of output modules and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Add a suffix letter K, L or R to designate the substitution of one of these module types for the type normally specified for output #1. See example below. For DC input add a prefix D to the model number.



SPECIFICATIONS

INPUT
90-132 VAC or 180-264 VAC, 47-440 Hz. Strappable.
40-60 VDC for DM Series.

INPUT SURGE
Less than 68 Amps peak from cold start.

HOLDUP TIME
20 milliseconds from loss of nominal AC power.
3 milliseconds for DM Series.

OUTPUTS
See model selection table.

ADJUSTABILITY
±5% trim adjustment.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries.

REMOTE SENSING
On all outputs except type J modules.

RIPPLE & NOISE
1% or 100mV pk-pk, 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 10 LFS cooling air directed over the units for full rating. Two test locations on chassis rated for max. temperature of 90°C.

TEMPERATURE COEFFICIENT
±0.02%/°C.

EFFICIENCY
80% typical.

SAFETY
Units meet UL 1950, CSA 22.2 No. 220, CSA bulletin 1402C, IEC 950, VDE 0804, VDE 0806, VDE 0805 (proposed). Certifications in process.

DIELECTRIC WITHSTAND
3750 VRMS input to ground.
3750 VRMS input to output.
700 VDC output to ground.

SPACING
8 mm primary to secondary.
4 mm to grounded circuits.

LEAKAGE CURRENT
0.75 mA at 115 VAC 60Hz. input. Not applicable to DM Series.

EMISSIONS
Units meet FCC 20780 Part 15 Class A and VDE 0871/6.78 Class A for conducted emissions. Compliance with Class B limits by use of additional external filter. DM Series also meet Bellcore TR-TSY-000515.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%.
R, M and N modules – 200 microseconds.
J, K, and L modules – 500 microseconds.

UNDERVOLTAGE
Protects against damage for undervoltage operation.

OVERVOLTAGE PROTECTION
Standard on all outputs.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Auxiliaries have additional backup fuse protection.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

SOFT START
Units have soft start feature to protect critical components.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided.

SHOCK
MIL-STD 810-D Method 516.3, Procedure III.

VIBRATION
MIL-STD 810-D Method 514.3, Category 1, Procedure I.

MECHANICAL
400 W/500 W – 2.5" H x 5.05" W x 9.00" L. Case 1.
600 W/750 W – 2.5" H x 5.20" W x 9.63" L. Case 2.
600 W/750 W – 2.5" H x 6.5" W x 9.63" L. Case 3.

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME compatible power fail signal providing 4 milliseconds warning before main output drops by 5% after an input failure.

AUTO RANGER
Optional circuit provides automatic operation at specified input ranges without strapping. Not applicable to DM Series.

PILOT BIAS
Optional circuit provides SELV output of 5 volts at 75 milliamps independent of the main power converter. Output isolation compliant to safety specifications referenced above.

ACTIVE SURGE LIMIT
Limits input surge to less than 18 Amps, and provides rapid reset.

COVER
Optional flat cover recommended when customer supplied fan cooling is directed through the length of the unit.

FAN COVER
Optional cover with brushless DC fan which provides the required air flow for full rating of Moduflex power supplies.

REDUNDANT
This option is specified when two or more like M units are to be used in an N + 1 redundant hookup using external isolating diodes. Cable assemblies are provided that interconnect the remote sensing leads and the single redundant wire which provides current sharing. This option not available for M units containing J modules.

POWER FACTOR CORRECTION
Refer to Bulletin FM-101 for M Series units with 0.99 power factor and harmonic currents compliant to IEC 555-2.

Deltron inc.
290 WISSAHICKON AVENUE, P.O. BOX 1369, NORTH WALES, PA 19454
PHONE: 215/699-9261 • FAX: 215/699-2310

Int'l. Units: Delaire • Sallynoggin Road, Dun Laoghaire, Co. Dublin, Ireland. Tel: (01) 851411 Prefixes – from U.K. – (0001)–Int'l. + 353–(1) Telex: 30442DEL EI
Delinc • Padre Mier y Dr. Mina, Reynosa, Tamps., Mexico 08866. Tel.: (892) 38723 Prefix – from USA – (01152) FAX (892) 38776

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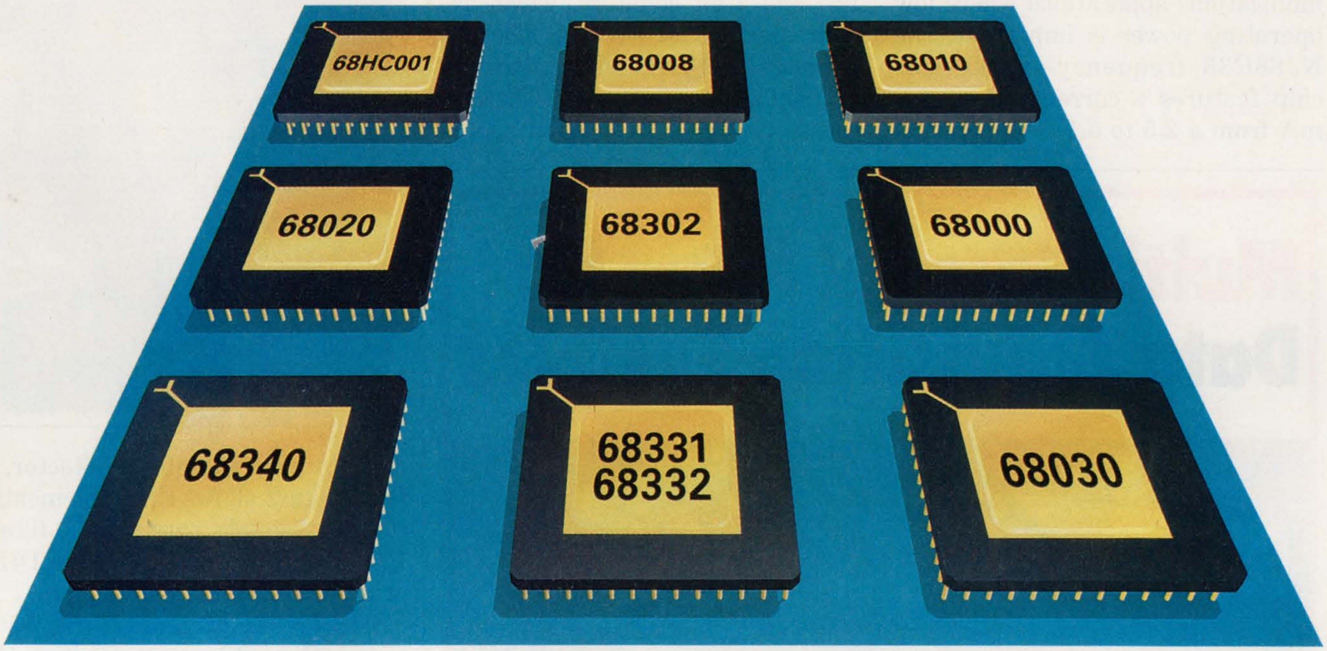
Designing with Motorola's



Microprocessors?

Then you need HMI's development systems, we support the entire 68000 family. As Motorola enhances and increases integration of its microprocessors, you can count on HMI to be there with high-quality development products to support your projects. HMI believes in supporting the entire family of products for the Motorola family. Ease of use and familiarity are common in all the emulators.

Features of HMI's development systems includes:

- Run at real-time with no wait states.
- Window driven source level debugging—SourceGate®
- C, Pascal and ADA compiler source level support for all major compiler companies.
- Real-time hardware performance analyzer.
- Works with IBM PC family and UNIX based machines including Sun and Apollo.
- RS232 Interface up to 115.2K.
- Parallel Interface for high-speed code downloading.
- Complex events and sequences for break and trigger conditions.
- Two independent 4K deep trace buffers.
- 1 μsec resolution interval timer.
- 100 nsec resolution Time-stamp in trace buffer.
- Logic state analyzer capabilities built into the emulator.
- 16 External Trace bits.
- Overlay memory up to 4 Mbytes.

If you are looking for one emulator company that provides support for the entire Motorola family, then look to HMI for total support.

Motorola Devices Supported Include:

68000	68030	68340
68008	6809	68HC001
68010	68302	68HC11 including
68020	68332/331	F1 and D3

IBM is Reg. T.M. International Business Machines, Inc. Unix is Reg. T.M., Bell Laboratories, Inc.

HMI

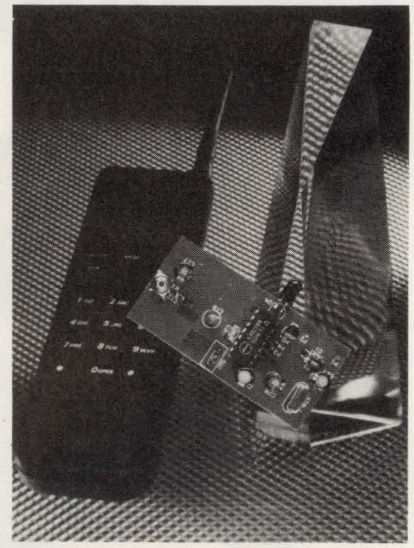
Huntsville Microsystems, Inc.
3322 South Memorial Parkway
Huntsville, AL 35801
Tel.: (205) 881-6005
FAX: (205) 882-6701

CIRCLE NO. 159

Frequency Synthesizer

- *Operates to 120 MHz*
- *Current drain is 3 mA*

Designed for use in personal communications applications where low operating power is important, the NJ88C33 frequency-synthesizer chip features a current drain of 3 mA from a 2.5 to 5.5V supply. You can use the IC as a single-chip 120-MHz device or with an external prescaler for operation to 2 GHz. The IC contains programmable 16-, 12-, and 7-bit counters, which are addressed by an I^2C bus. The bus operates to 2 MHz and can achieve channel loading in 20 μsec. The synthesizer chip uses current-source



outputs from the phase detector, a feature that allows the implementation of a simple passive loop-filter. The NJ88C33 comes in 14-pin DIPs or SOIC packages. $7.87 (100).

Plessey Semiconductors, 1500 Green Hills Rd, Scotts Valley, CA 95066. Phone (408) 438-2900. FAX (408) 438-5576. TLX 494-0840.

Circle No. 386

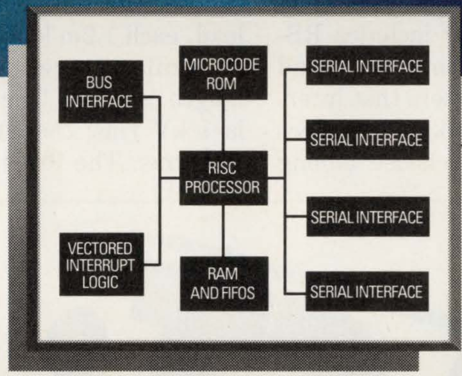
Dual 14-Bit DAC

- *Saves board space*
- *Includes a 3V zener reference*

The AD7244 dual 14-bit DAC includes a 3V buried-zener reference, output amplifiers, and high-speed serial interface logic. A pin-compatible 12-bit version, the AD7242, provides an upgrade path for applications that don't currently need 14-bit performance. Housed in a 24-pin DIP or 28-lead SOIC, these dual DACs save cost and board space compared with separate devices. The devices typically consume 130 mW from ±5V supplies. The 14-bit dual DAC settles to ±½ LSB in less than 4 μsec; the 12-bit device settles in 3 μsec. Both devices have a nominal output span of ±3V. The 14-bit AD7244, from $17.95; 12-bit AD7242, from $14 (100).

Analog Devices, 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428. **Circle No. 387**

UXART
The Wait Is Over.
Now there's a serial I/O chip designed for UNIX.



For years, dumb UARTs have been the standard datacom solution. Now there's something better for today's multi-user, multi-protocol datacom environment. Our single-chip solution gives you multiple channels — each capable of full-duplex operation at 115.2 kbps — and replaces up to 10 chips.

Cirrus Logic introduces the UXART — the first and only UART with specific features to simplify and speed up serial I/O efficiency by a factor of ten or more. So your UNIX® system can support more users, with better response time — and less waiting.

The CL-CD1400 UXART™ gives you 4 fully independent datacom channels, each capable of full-duplex operation at 115.2 kbps. Each channel has two 12 byte FIFOs, one for transmit and one for receive. Separate vectored interrupts allow quick entry to the correct service routine.

A number of features reduce the load on the host system. Automatic expansion of Newline to CRNL, plus other CR and NL options. User-definable flow control characters for automatic flow control. All five types of UNIX-specified parity and error handling. And more.

For high-line-count, cost-effective applications, there's the CL-CD180. It offers performance gains similar to the CL-CD1400, plus the advantage of 8 channels in a single 84-pin package.

The CL-CD2400 adds synchronous capabilities. It offers 4 independent, multi-protocol channels, plus an on-chip DMA controller for fast, efficient I/O.

For all your multi-protocol, multi-user datacom needs, the Cirrus Logic family of intelligent, high-performance data communications controllers gives you superior throughput in less space — with less waiting.

Don't wait. Call today for *free* product information and benchmark report on the CL-CD1400.
Call 1-800-952-6300. Ask for dept. LD25

An on-chip 10 MIPS RISC-based processor handles transmit and receive functions, buffer management, flow control, and all special character processing. On-chip FIFOs reduce host interrupts to give you more efficient interrupt handling. The result: faster system throughput, lower host overhead, and less waiting.

CIRRUS LOGIC
C L O S I N G T H E G A P

TEST & MEASUREMENT INSTRUMENTS

191-MHz FFT Spectrum Analyzer

- *Has 90-dB dynamic range*
- *Includes MS-DOS-compatible $3^1/_2$-in. floppy-disk drive*

The SR760 is an FFT spectrum analyzer that covers frequency spans of 100 kHz to 191 MHz with a dynamic range of 90 dB. Line widths range from 476 μHz to 250 Hz. Real-time bandwidth is 50 kHz. In dual-trace mode, you can view a time record and a spectrum simultaneously. The unit incorporates a 16-bit A/D converter and a $3^1/_2$-in. floppy-disk drive that stores 720k bytes of data and setups in MS-DOS format. The analyzer includes RS-232C and IEEE-488 interfaces, and it directly drives plotters that interpret the Hewlett-Packard Graphics Language. You can choose among the following windowing functions: Blackmun-Harris, flat-top, Hanning, and force exponential. $4350.

Stanford Research Systems Inc, 1290 D Reamwood Ave, Sunnyvale, CA 94089. Phone (408) 744-9040. FAX (408) 744-9049. TLX 706891.

Circle No. 388

Silicone-Rubber Multimeter Lead Set

- *Rated for 1 kV and 10A rms*
- *Accepts push-on probes and accessories*

The STLS 2000 lead set for multimeters includes a red and a black lead, each 1.2m long. The TLS 2000 is similar, except that the lead length is 1.5m. The voltage rating is 1 kV rms; the current rating is 10A rms. The leads are supple because the wire in each lead consists of more than 700 strands; moreover, the insulation is soft silicone rubber. The leads have banana plugs at each end. The plugs, which accept push-on probes and accessories, incorporate spring-loaded, retractable shields. $19.95.

Test Probes Inc, 9178 Brown Deer Rd, San Diego, CA 92121. Phone (800) 368-5719.

Circle No. 389

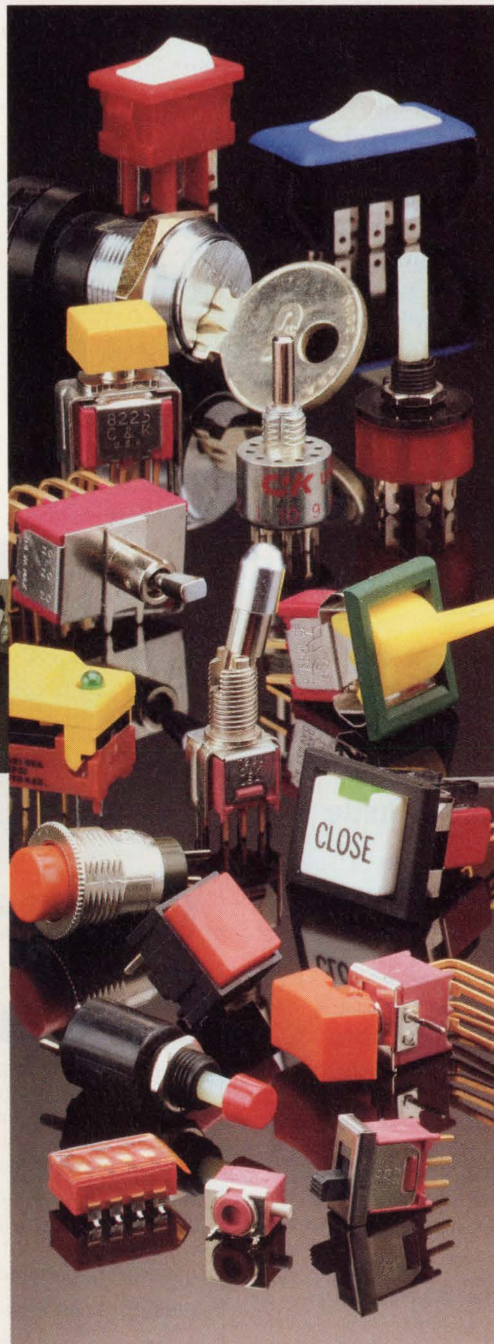
RS-232C-Interfaced Device Programmer

- *Works with computers of any type*
- *For PROMs, EPROMS, μCs, EEPROMs, PLDs, and EPLDs*

The Allpro-S device programmer works with any computer that

CIRCLE NO. 39

CONSISTENT QUALITY. TECHNICAL EXCELLENCE. AVAILABILITY.



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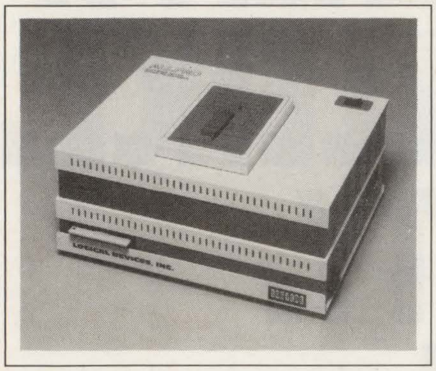


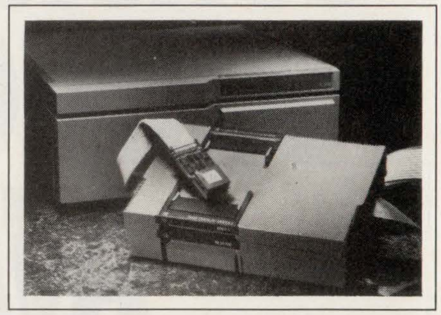
has an RS-232C port. The instrument handles PROMs, EPROMs, EEPROMs, PLDs, EPLDs, and single-chip microcomputers. It adapts to all devices via software; there are no plug-in adapters. Users of the vendor's IBM PC-based programmers can turn those units into the equivalent of the new programmer by adding a chassis that includes an RS-232C port, a 3½-in. floppy-disk drive, and a processor based on an 8088 μP with 256k bytes of memory. Upgrades to 640k bytes are possible. $5995.

Logical Devices Inc, 1201 NW 65th Pl, Fort Lauderdale, FL 33309. Phone (800) 331-7766; in FL, (305) 974-0967. FAX (305) 974-8531. **Circle No. 390**

In-Circuit Emulator For MC68EC030

- *Displays coprocessor registers in floating-point format*
- *Can include event-triggering system*

The EL 3200 in-circuit emulation system now supports the MC68EC030 μP. Features include support of cache-burst and single-cycle modes; symbolic and source-level debugging; and 33-MHz, zero-wait-state, high-speed overlay memory for normal bus cycles. The trace and event system includes access breakpoints; software and



hardware execution breakpoints; complex-event comparators; trigger inputs and outputs; counters; timers; and flags. The emulator communicates with its host via Ethernet using TCP/IP. Hosts are IBM PCs, Sun 3s, SPARCstations, DECstation 3100s, and VAX/VMS systems. From $30,000; trace and event system from $10,000. Delivery, eight weeks ARO.

Applied Microsystems Corp, Box 97002, Redmond, WA 98073. Phone (800) 426-3925; in WA, (206) 882-2000. **Circle No. 391**

CIRCLE NO. 154

NEW PRODUCTS

COMPUTERS & PERIPHERALS

Process Controller Board

- *Displays control parameters on computer screen*
- *For programs having as many as 96 segments*

The SMT-01 single-loop process controller board is a PID (proportional-integral-differential) controller. It plugs into a 16-bit ISA bus expansion slot. The board is programmable for any number of programs having as many as 96 segments each. You can display the process variable vs time along with setpoint, high and low alarms, PID parameters, and autotuning. You can store these parameters in a battery-backed RAM. A ROM-based algorithm provides thermocouple linearization. The controller accepts inputs from a thermocouple, a resistance temperature detector, a 4- to 20-mA source, a pressure transducer, and other specified inputs. Dual 4-to 20-mA control outputs are selectable from the keyboard. The board's two alarm outputs drive solid-state relays. Board, including software on a 5¼-or 3½-in. disk, $395.

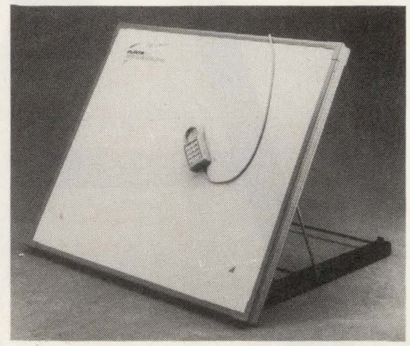
Temp Inc, Box 929, Fairmont, WV 26554. Phone (304) 366-4088.

Circle No. 392

Portable Digitizer

- *Features an 18×24-in. tablet*
- *Components fit inside the surface of the tablet*

You can use the XLC/1824 portable digitizing tablet for CAD, drafting, and construction estimating. The 18×24-in. tablet lets you place components inside its surface, making it flat instead of sloped. The digitizer works with Timberline and Promation construction estimating software as well as popular CAD programs. The unit connects to an IBM PC or a compatible computer, and you can transport it from office to office. The vendor offers a choice



of either a corded 2-switch pen or a corded 16-key cursor with a window cross hair. The digitizer can also emulate GTCO's L Series, Calcomp 9500, Summagraphics Microgrid, and Numonics 2200 digitizing tablets. The software driver supports Microsoft mouse and Windows-compatible programs. Tablet with ±0.01-in. accuracy, $2195; tablet with ±0.005-in. accuracy, $3695.

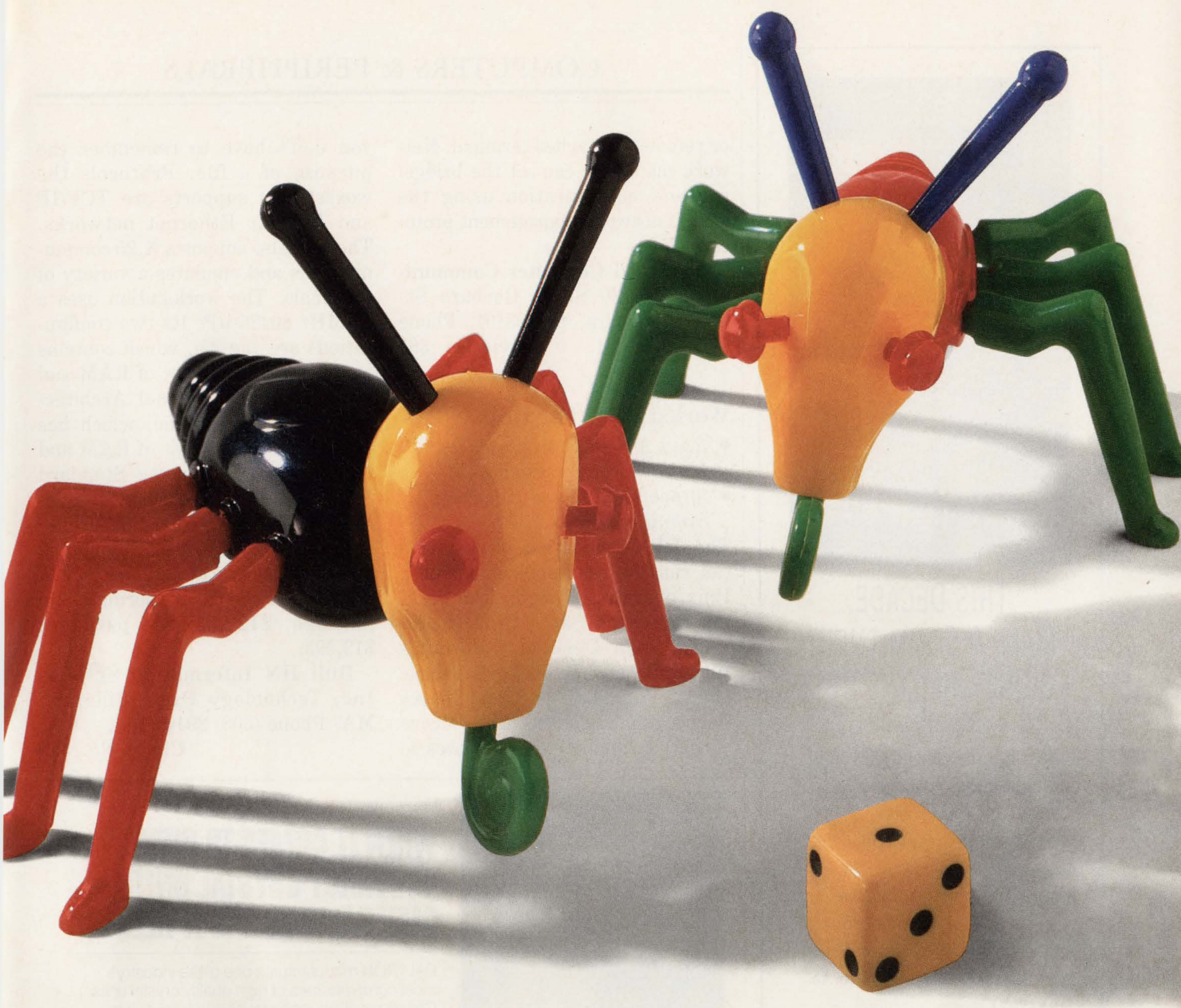
Kurta Corp, 3007 E Chambers St, Phoenix, AZ 85040. Phone (602) 276-5533. FAX (602) 276-7823.

Circle No. 393

T1 Bridge/Router

- *Links remote networks together as fast as 2.048M bps*
- *Software features IEEE-802.1 spanning-tree protocol*

The ACS 4200 T1 bridge/router links remote networks together as fast as 2.048M bps. The unit operates on the company's Series 4000 multiprotocol bridge/routing software. The software routes TCP/IP, DECnet, XNS, and IPX protocols while providing a bridge to all other network protocols. The software also features the IEEE-802.1 spanning-tree protocol, automatic address learning, and dynamic and static routing. Each of the unit's two wide-area-network ports can operate at different speeds and physical connections, such as X.25 networks or T1 leased lines. You can configure the unit from a locally



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or remotely attached terminal. Network managers can set the bridge/router's configuration using the simple network-management protocol. $8500.

Advanced Computer Communications, 720 Santa Barbara St, Santa Barbara, CA 93101. Phone (805) 963-9431. **Circle No. 394**

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- *Runs MS-DOS programs on Unix operating systems*
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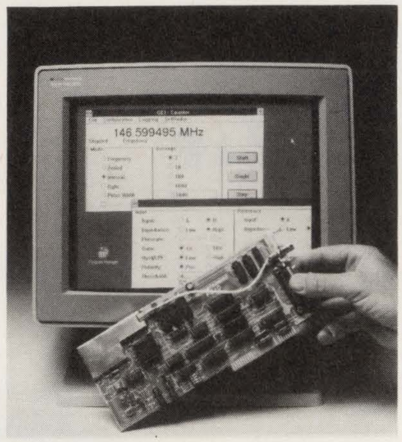
The DPX/Prostation workstation can run MS-DOS applications on a Unix operating system. The desktop unit runs Santa Cruz Operation's Open Desktop, Informix's WingZ, Frame Technology's Framemaker, Alfalfa's Poste, and Ingres Corp's application software. Icons connect to an array of templates so you don't have to remember the purpose of a file. Protocols the workstation supports are TCP/IP and ISO for Ethernet networks. The unit also supports X.25 communications and emulates a variety of terminals. The workstation uses a 25-MHz 80486 µP. Its two configurations are the 25i, which contains as much as 32M bytes of RAM and a single Micro Channel Architecture slot; and the 25e, which has as much as 64M bytes of RAM and two Extended Industry Standard Architecture slots. Each system includes a 213M-byte hard-disk drive and a 144M-byte, 3½-in. floppy-disk drive that can read and write IBM PC/AT and compatible formats. 25i package, $12,995; 25e package, $13,495.

Bull HN Information Systems Inc, Technology Park, Billerica, MA. Phone (508) 294-6616.
Circle No. 395

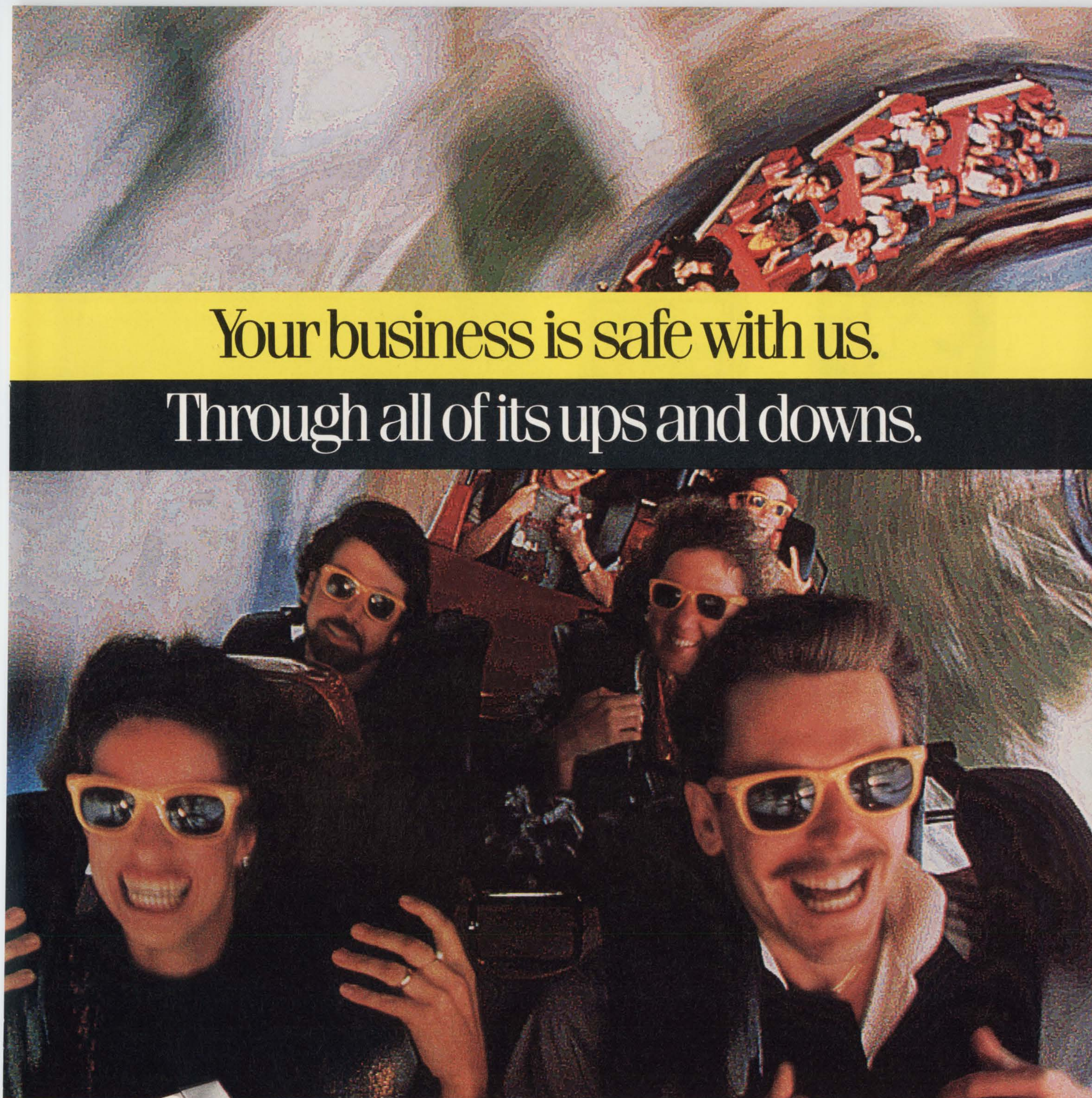


Universal Counter/Timer Card

- *Uses Windows 3.0 as a control panel and display window*
- *Operates from 10 Hz to 2.4 GHz*

The Model PC-10 universal frequency counter/timer operates from 10 Hz to 2.4 GHz. The IBM PC-compatible plug-in card uses Windows 3.0 as a control panel and display window. The unit captures and analyzes discrete and average frequency readings, pulse widths, time intervals, and the ratio between two frequencies. The card's 200-MHz CMOS ASIC and three bipolar monolithic microwave ICs reduce the parts count to 23 ICs. The unit operates as a self-tuning radio, and when the frequency scanning is too slow, it can tune a companion receiver. The card's minimum sensitivity is 10 mV. The unit displays the frequency with 10-digit resolution. The unit's input-gate is continuously variable from 1 msec to 28 sec for optimum balance between time and resolution. The temperature-compensated crystal oscillator has a ±1-ppm resolution. $335.

Optoelectronics Inc, 5821 NE 14th Ave, Fort Lauderdale, FL 33334. Phone (800) 327-5912; in FL, (305) 771-2050. FAX (305) 771-2052. **Circle No. 396**



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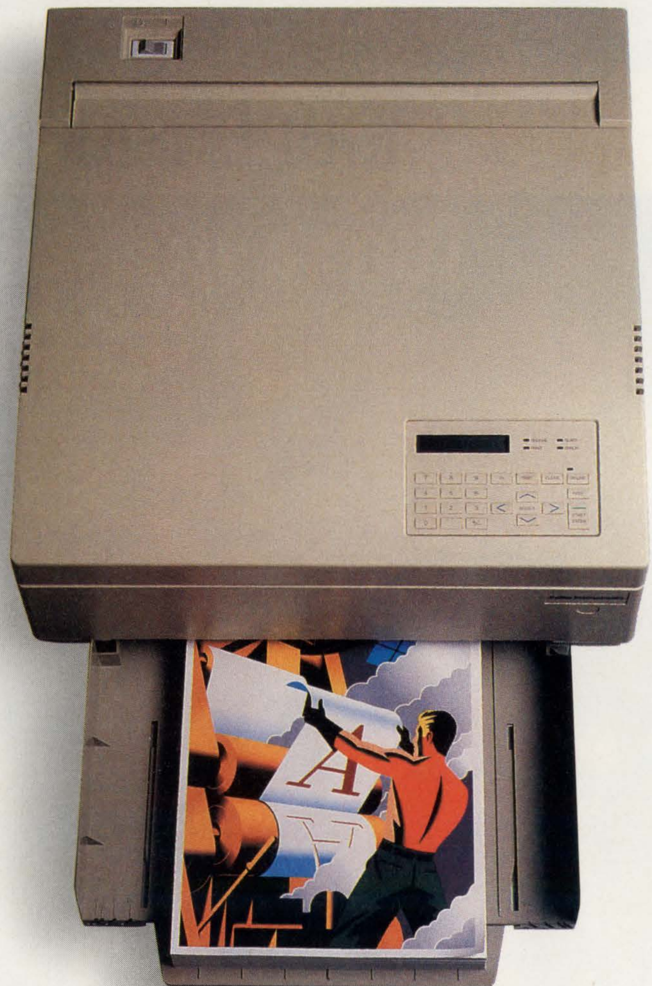

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Listing Of Scientific Software Programs

The 1991 Cosmic Software Catalog provides a comprehensive listing of program abstracts for approximately 1200 scientific programs that are available in the US. It also lists more than 900 programs for limited distribution. Each abstract explains the program's capabilities and presents the programming language, machine requirements, size, and price of the source code and supporting documentation. The printed and microfiche catalogs provide a keyword index, and the disk versions have a search menu. NASA's Technology Utilization Program makes these computer programs available for re-use by domestic industries, governmental agencies, and universities. $25 to $60.

Cosmic, University of Georgia, 382 E Broad St, Athens, GA 30602.

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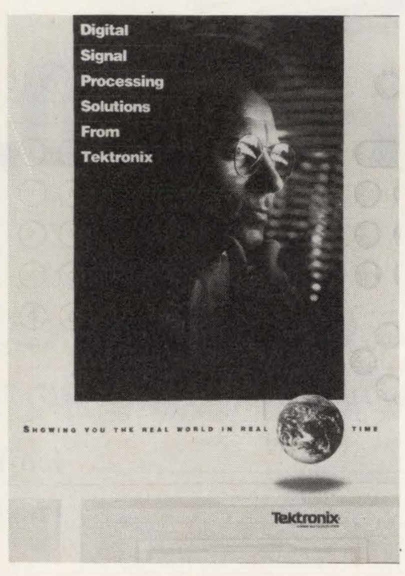

Brochure About Digital-Signal Processing

This 8-pg pamphlet presents DSP-based solutions for high-end signal-analysis applications in military/signal intelligence, research physics, and satellite communications. It contains application notes and ex-

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Military: P.O. Box 47 • Joplin, MO 64802 • (417) 623-8000 • Commercial: P.O. Box 130 • Seneca, MO 64865 • (417) 776-2256 planations on pulsed radar, frequency-shift keying, and other measurements. The publication describes the VMEbus-based analysis systems that have amplitude-vs-frequency; spectrogram; and phase- and view-limits color displays.

Tektronix Federal Systems Inc, Box 4495, MS 38-386, Beaverton, OR 97076. **Circle No. 397**

Guide To Components For Signal Processing

The 116-pg *1991 Short Form Designer's Guide* covers data converters; amplifiers; analog signal-processing devices; transducers; disk-drive components; voltage references; and data-acquisition subsystems. Inside the front cover you'll find instructions on how to use the book, followed by an example of the selection-guide organization. The New Products section contains nu-

merous additions to the vendor's line of products.

Analog Devices, Box 9106, Norwood, MA 02062. **Circle No. 398**

Booklet Highlights VXIbus

This 32-pg brochure, *Feeling Comfortable with VXIbus*, introduces you to VXIbus, its features, and advantages. The publication explains how you can integrate VXIbus products in current test systems, and it discusses the tradeoffs in selecting various VXIbus devices. The publication is an overview of VXIbus technology rather than a manual for a particular VXIbus instrument. For more detailed technical information, the brochure provides a recommended-reading list.

Hewlett-Packard Co, Box 10301, Palo Alto, CA 94303.

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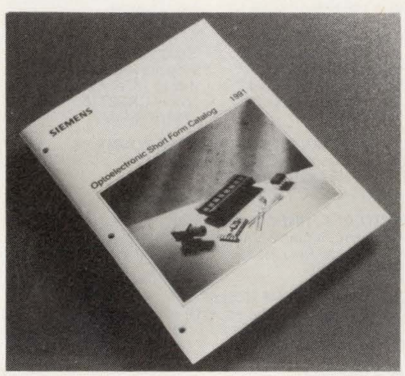

Publication Catalogs Optoelectronic Products

This 48-pg catalog talks about product-quality programs such as intelligent display devices; numeric displays; and military high-reliability displays. Other devices discussed are optocouplers, LED lamps, IR emitters, photodetectors, and plastic fiber-optic emitter and detector components.

Siemens Components Inc, Optoelectronics Div, 19000 Homestead Rd, Cupertino, CA 95014.

Circle No. 400

EDN's CHARTER

EDN is written for professionals in the worldwide electronics industry who design, or manage the design of, products ranging from circuits to systems.

EDN provides accurate, detailed, and useful information about new technologies, products, design techniques, and careers.

EDN covers new and developing technologies to inform its readers of practical design matters that will be of concern to them at once or in the near future.

EDN covers new products
- that are immediately or imminently available for purchase
- that have technical data specified in enough detail to permit practical application
- for which accurate price information is available.

EDN's Magazine Edition also provides specific "how to" design information that its readers can use immediately. From time to time, EDN's technical editors undertake special "hands on" engineering projects that demonstrate EDN's commitment to readers' needs for useful design information.

EDN's News Edition also provides comprehensive analysis and news of technology, products, careers, and distribution.

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For Most People, It Was Just Another Warm September Day.

For design engineers, it was the day mixed analog/digital design came of age.
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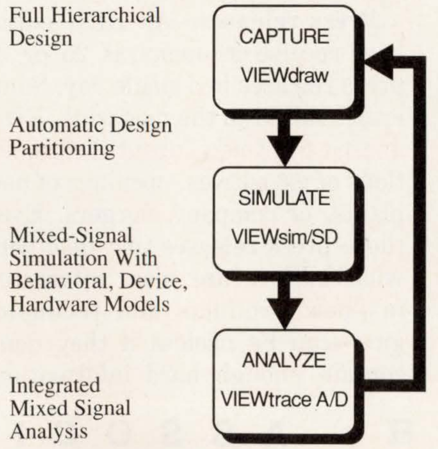

Our white paper "Mixed-Signal Simulation Benchmark Report" proves the point. **Call us at 1-800-422-4660, Ext. 102.** You'll like the climate we're creating for mixed-signal design.

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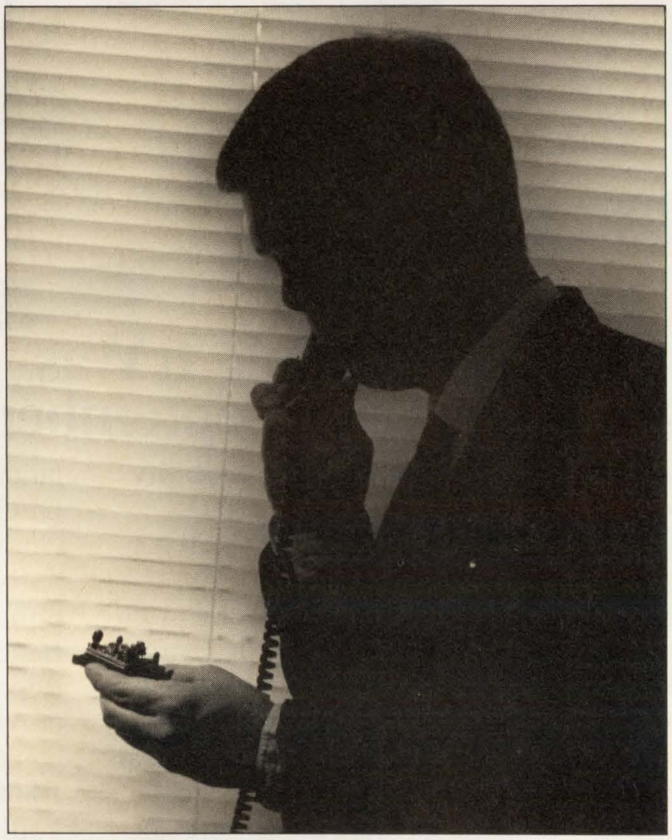
There's a lot more to being an EDITOR than editing



An EDN editor is a writer, a talent scout, a tutor, a researcher, a reporter, a critic, a trend spotter, a production coordinator, a consultant, and a troubleshooter. On any given day, he or she may watch a new-product presentation, give some guidance to a free-lance writer, brainstorm ideas for articles with other editors, advise an engineer about a design problem, answer readers' inquiries, attend a conference, hunt down some information, or write an article. The days are sometimes long, but seldom dull.

The raw material EDN editors deal with every day is information—information about companies, information about industry trends, and, most of all, information about new products and designs. All EDN technical editors have engineering degrees and extensive hands-on experience as working engineers. Their knowledge of what engineering in the real world is like guides them as they gather, process, and present the information that goes into the magazine.

The information comes to them from a variety of sources:

Press releases—An EDN editor may receive as many as 25 or 30 press releases in a single day. Some aren't suited to the magazine. EDN doesn't print news about the promotions of executives, openings of new plants, or company mergers. Even those press releases that deal with what editors are most interested in—new products and technologies—can be useless if they don't contain enough hard information, such as availability dates and prices. Perhaps one-fifth of the press releases that come in have information that will eventually find its way into the pages of the magazine.

Books, magazines, and newspapers—EDN editors read widely. They scan everything from prepublication copies of engineering textbooks to the newsletters of local computer societies. Some editors make a point of reading periodicals that deal with technologies outside their areas of expertise to give themselves additional perspective. It isn't just the articles that editors read: advertisements can also contain valuable information.

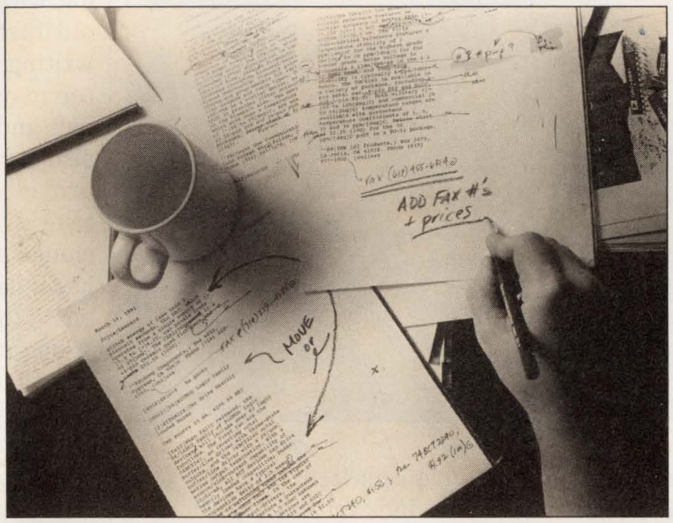
Marketing and public relations people—EDN editors are in constant contact with marketing and PR people. The people who do their jobs best know the magazine and understand what its needs are. They sometimes call an editor to announce a new product if they think he or she might be interested in it. PR people haven't always enjoyed a lofty reputation, but the real professionals can be an invaluable source of information.

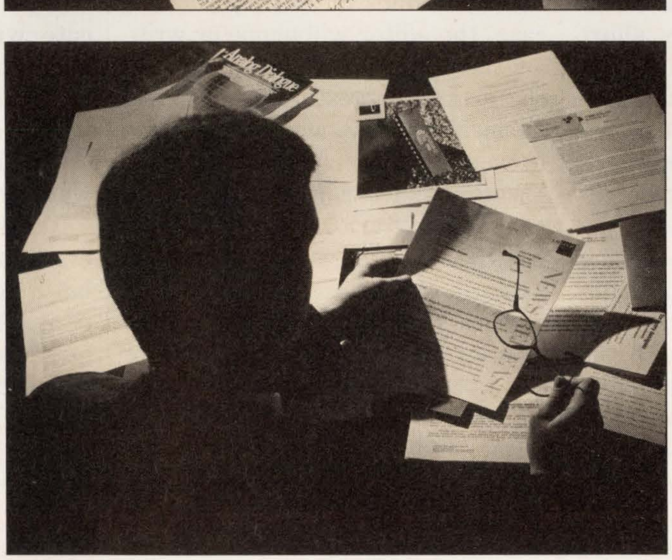
Company visits—Some compa-

JAY FRASER, ASSOCIATE EDITOR

nies send representatives to EDN's offices to announce new products. Sometimes they bring the products with them and demonstrate them. After an editor attends one of these meetings, he or she writes up a report and circulates it to the other editors in the office on E-mail. He or she also sends it to the regional editors on MCI mail.

Exhibitions and conferences—Exhibitions and conferences are valuable because they give editors a chance to see a great many new products at one time and provide a snapshot of where an industry is and where it is heading. But exhibitions and conferences are also important because they give editors a chance to meet and talk to people—marketing people, executives, engineers, and EDN readers. There's no substitute for talking with someone face to face.





Other editors—EDN editors are constantly passing information among themselves. Editors also confer with each other to determine how to focus an article and how to best present information.

EDN has six regional editors in the USA and one in Europe. Every week they write up reports about the companies they visit, the people they talk to, and the things they see, and send them into the home office. Regional editors are consulted about story ideas just as technical editors are.

Drawing on all these sources of information, every August and February EDN editors make up a list of topics for the articles they want to write in the coming year. They submit their lists to the editor, who then sits down with two senior editors and works out a detailed schedule. The schedules are only six months long because the high-tech industry changes so rapidly and predicting trends is difficult.

Once a topic is approved and an article scheduled, the first thing an editor usually does is send out editorial call letters. The letters go to firms that manufacture the products the editor will discuss in the article. The editor asks for detailed information—specs, part numbers, prices, applications, and the advantages and disadvantages of the products. The editor also asks for photographs or drawings and the name and phone number of someone he or she can contact for more information.

Then an editor begins to phone his or her industry contacts to find out about the newest products that have been introduced, or are about to be introduced, and the latest technology advances. Contacts aren't necessarily public-relations people. An editor also talks with engineers, managers, and people who have used a product.

The editor also turns to his or her files and digs out all the press releases, clips from magazines and newspapers, and faxes that might pertain to the article. In addition, the editor checks back issues of EDN to see what has been previously written about the subject.

After the replies to the editorial call letters have come in and the rest of the information has been assembled, the editor begins to write the article.

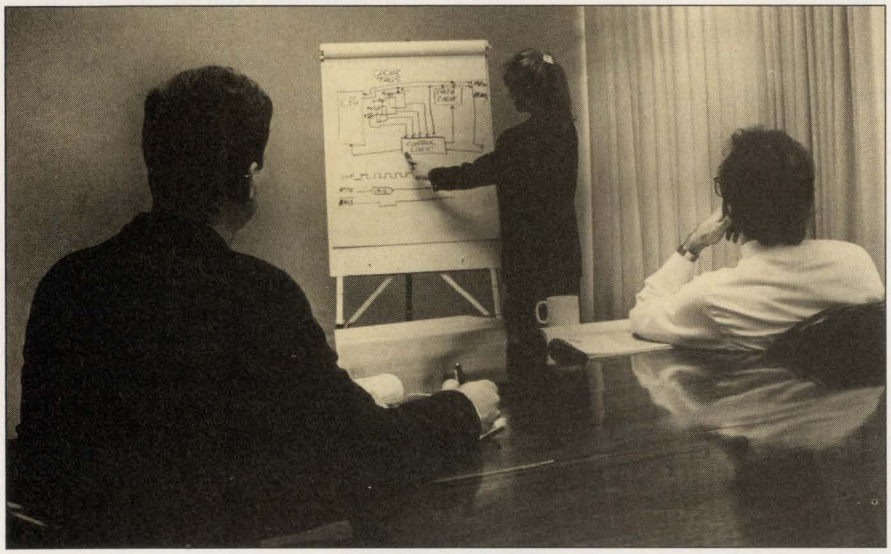
Writing is part craft and part art. The craft is extracting from the mass of information what is most important, putting it in the proper order, and making sure that it's complete and that all the pieces fit together into a smooth whole. Editors add their insight and analysis to the material, interpret what is going on in the industry, and look for trends. The art of writing lies in adding that indefinable spark that will bring the entire article to life and catch and hold the reader's attention.

Part of writing an article is also the painstaking compilation of ta-

Photography by Kevin Bryan

bles or graphs and the checking and rechecking of names, addresses, and telephone and fax numbers to make sure they're accurate.

Every EDN technical editor has a varied schedule of writing assignments. He or she is responsible for Special Reports, Technology Updates, Product Updates, Design Features, and News Breaks each



year, as well as a small number of miscellaneous pieces. Each editor also contributes numerous short write-ups to the New Products section. The information for these write-ups comes from press releases, visits by company representatives, and editors' visits to high-tech firms.

Writing articles for the magazine is an editor's primary responsibility, but it's only part of the job. Editors also have to deal with the many proposals and manuscripts that are sent to the magazine. EDN receives hundreds of these each year. Unfortunately, most of them are unusable.

Too many people who want to write for EDN don't read the magazine carefully to understand the kind of articles it does and doesn't print. They send in proposals for articles dealing with a single product, or case histories, or Horatio Alger stories. The editors reject these proposals out of hand.

Other people start by sending in complete articles they have slaved over. That's almost always a waste of time and postage. Even if the article happens to be on a subject of interest to EDN's readers, it would almost certainly have to be rewritten to conform to the length, structure, and style EDN requires.

Occasionally an editor will receive an unsolicited proposal that he or she finds interesting. In that case, the editor will phone or write a letter to the person who proposed the article suggesting what should be included in it and requesting a detailed outline and a sample lead paragraph. The editor will also send a copy of "Writing for EDN," a booklet that describes what the magazine requires in a contributed article. The editor and the writer may go through a great deal of give and take and more than one rewrite to mold the article into its final form.

Some editors have additional, specialized duties. Two of them handle the Design Ideas section. They choose among the designs sent in by readers and edit the descriptions and schematics. Because they receive many more ideas than the magazine has room to print, the choices they have to make are sometimes difficult. In this situation, too, the editors' real-world engineering experience helps them make their decisions.

After the information is distilled into a story, it is presented to the readers in the magazine. EDN is published 26 times per year, and each issue is read by approximately 160,000 working engineers. The magazine is the primary way editors have to convey information, but it isn't the only way.

Editors always welcome feedback from readers, and readers have a number of options for communicating with them. Readers can use the old-fashioned method of simply writing a letter to the editor. A letter may end up printed in the Signals and Noise section. Readers can also write comments in the space provided on the Information Retrieval Service cards that are included in every issue. If a reader has a design problem, he or she can write to the Ask EDN department. If the editors can't solve the problem themselves, they'll get in touch with experts who can.

Last October, EDN started a computer bulletin board system that enables readers to communicate with the magazine's editors and with other readers. The bulletin board offers many other services, such as providing free utility, scientific, and engineering shareware programs.

This brief summary doesn't cover every detail of an EDN editor's job, but it does touch on the many facets of it. An EDN editor does much more than simply edit manuscripts. An editor reads, listens, observes, thinks, and then conveys the information he or she has gathered. Most readers never notice the names on the masthead or on bylines, but the work the editors do is important, satisfying, and usually enjoyable. EDN

Article Interest Quotient
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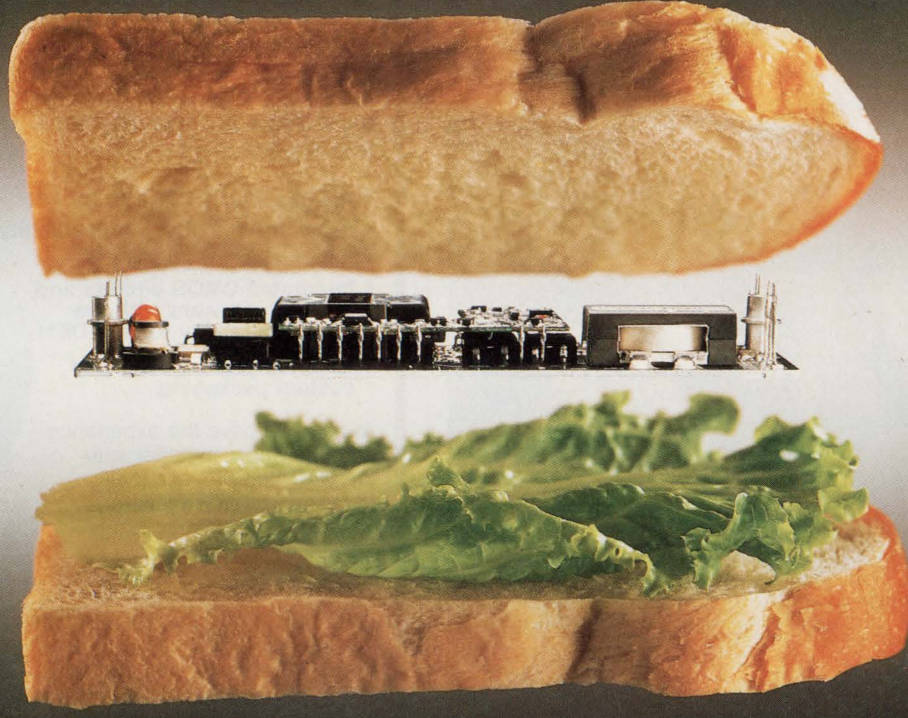

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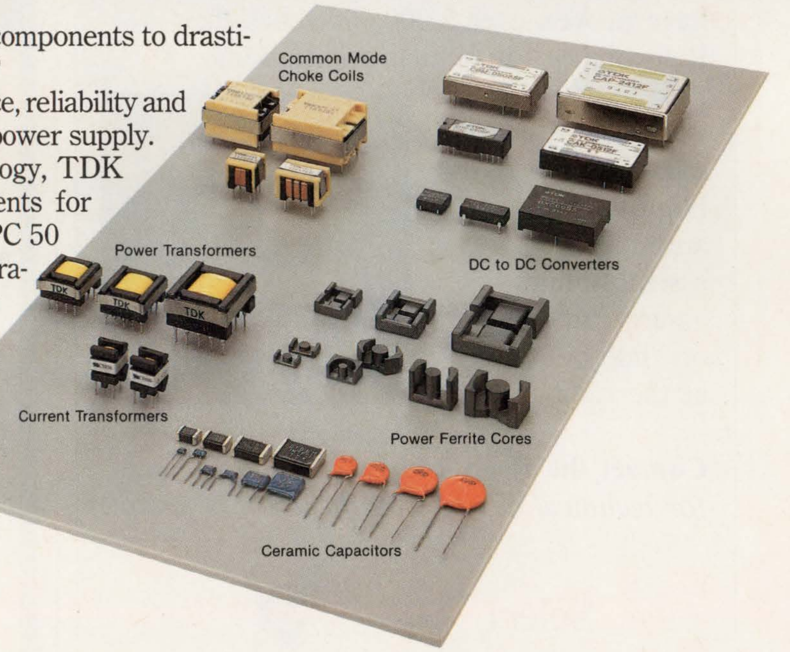

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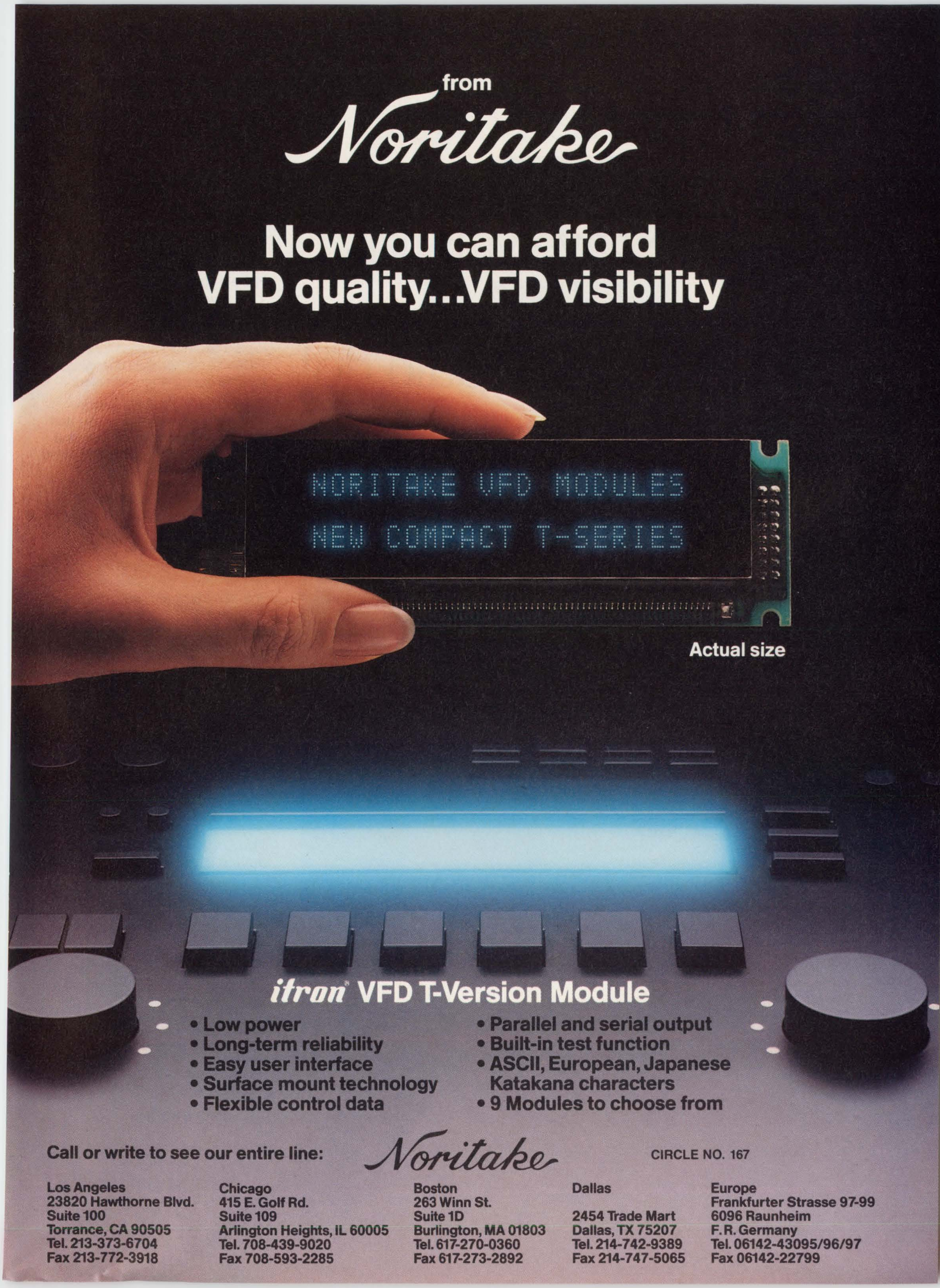

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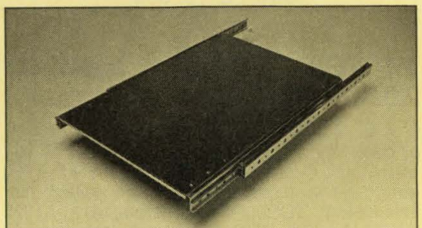

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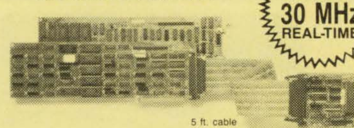

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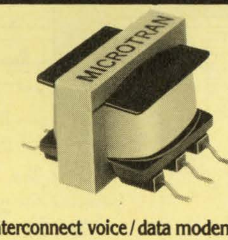

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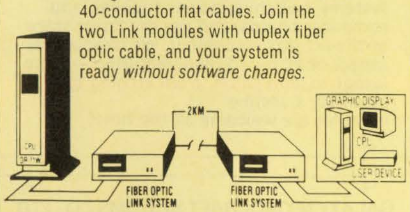

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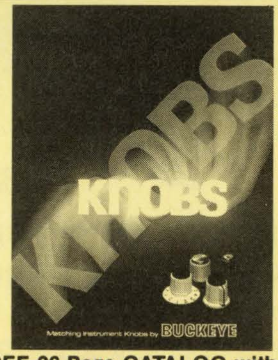

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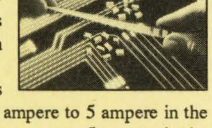

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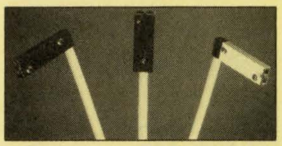

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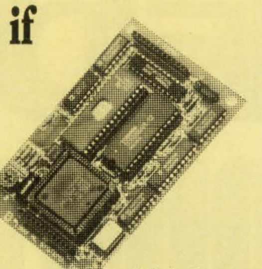

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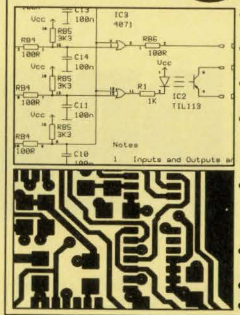

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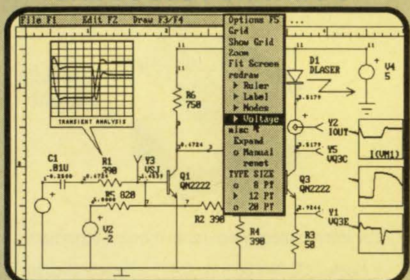

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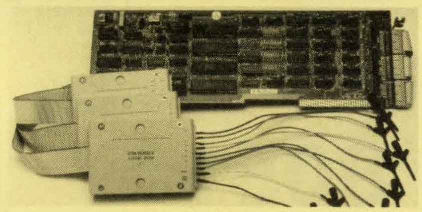

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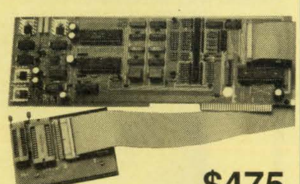

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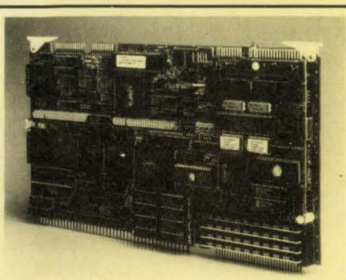

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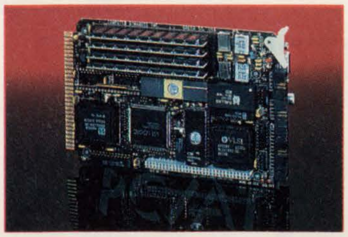

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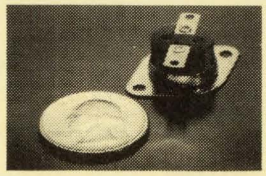

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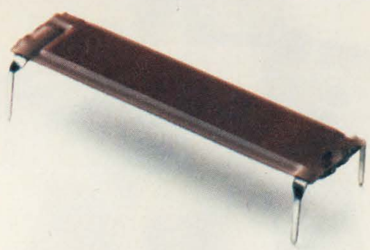

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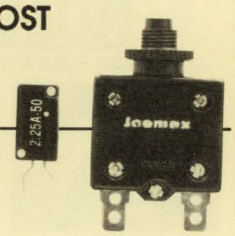

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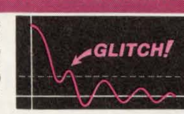

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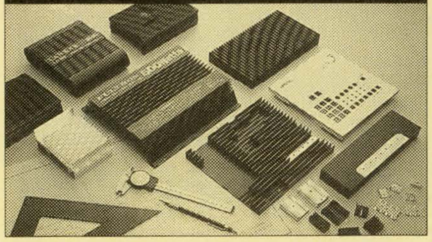

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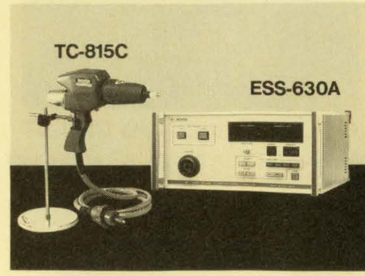

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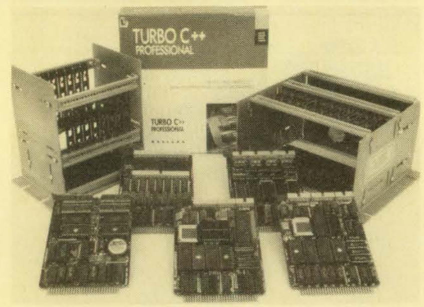

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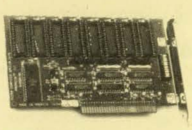

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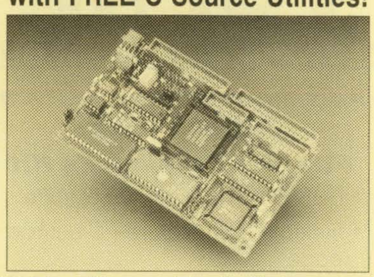

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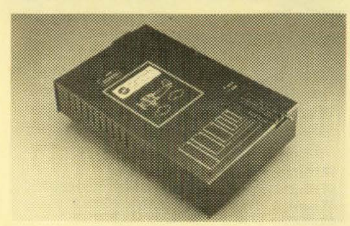

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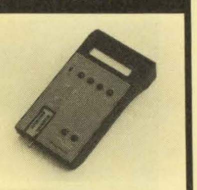

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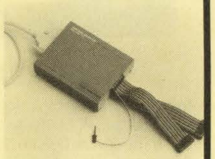

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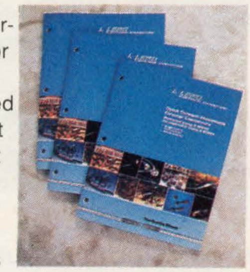

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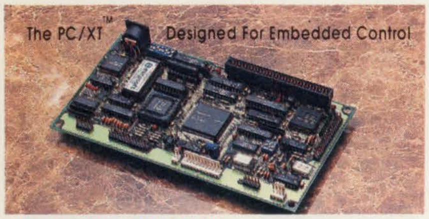

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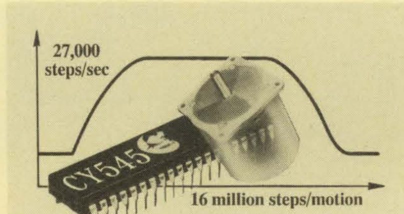

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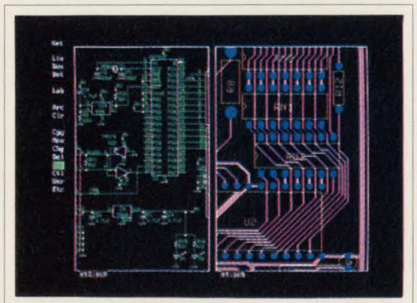

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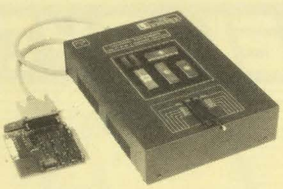

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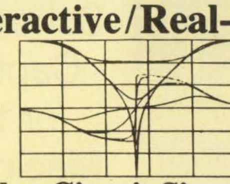

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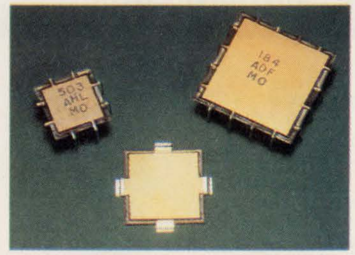

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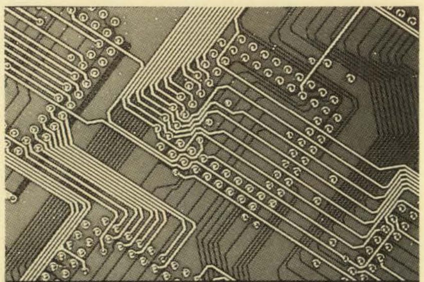

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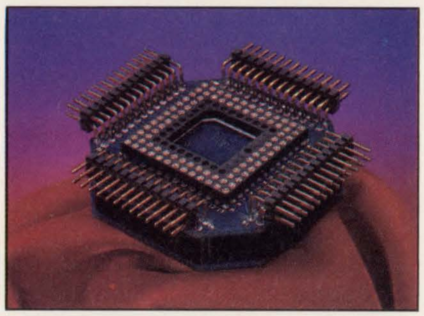

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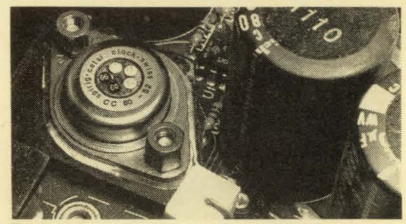

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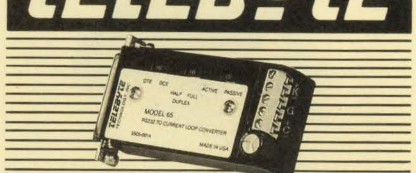

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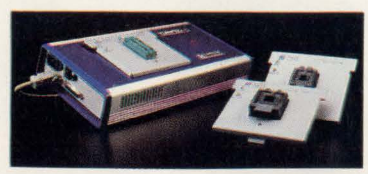

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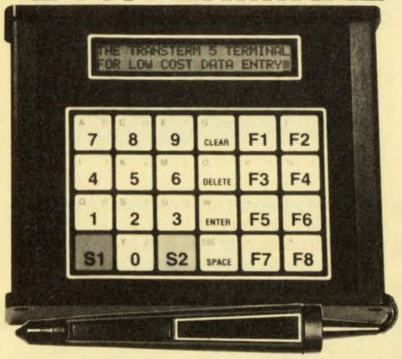

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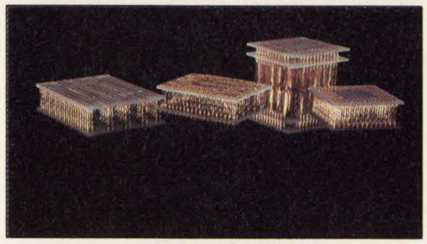

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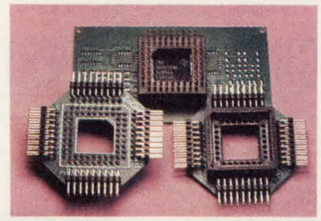

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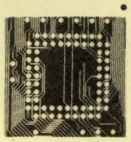

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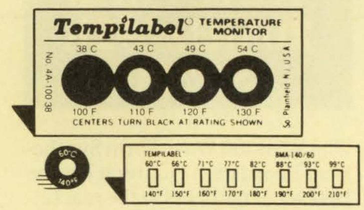

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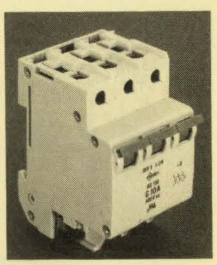

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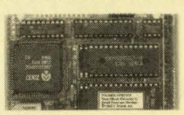

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Issue	Issue Date	Ad Deadline	Editorial Emphasis
Magazine Edition	June 20	May 30	Software, ICs & Semiconductors, High Speed Memory Technology • Computer Bus Boards
News Edition	June 27	June 7	ICs & Semiconductors, RISC**, Regional Profile: So. California**
Magazine Edition	July 4	June 13	Product Showcase—Volume I • Interconnects, ICs & Semiconductors • Neural Networks • Power Sources, Software
Magazine Edition	July 18	June 26	Product Showcase—Volume II • Test & Measurement, Computer Peripherals • Components, CAE/ASICs •
News Edition	July 25	July 5	ICs & Semiconductors, Peripherals**, Regional Profile: Massachusetts**
Magazine Edition	Aug. 5	July 11	CAE • ASICs, Test & Measurement • Computers & Peripherals • Technical Article Database
News Edition	Aug. 8	July 19	CAE, Datacom**
Magazine Edition	Aug. 19	July 25	Military Electronics Special Issue, Image Processing • Ultra High Speed ICs/ASICs • Computer Peripherals, Software •
News Edition	Aug. 22	Aug. 2	Peripherals/Components, Test & Measurement**, Regional Profile: Idaho, Colorado, Utah**
Magazine Edition	Sept. 2	Aug. 8	ASICs Special Issue, Semicustom ICs • CAE, Packaging • ICs & Semiconductors Data Converters
News Edition	Sept. 5	Aug. 16	Military Electronics Special Issue, Computer Architectures, Defense Electronics**
Magazine Edition	Sept. 16	Aug. 21	DSP/Microprocessors, ICs & Semiconductors, CAE/ASICs, Environmental Engineering • Software
News Edition	Sept. 19	Aug. 29	RISC/ICs, Computers**, Regional Profile: Florida**
Magazine Edition	Oct. 1	Sept. 5	Computers & Peripherals/Networks, DSP Chip Directory • ICs & Semiconductors/Memory Technology, Instrumentation
News Edition	Oct. 3	Sept. 13	ICs & Semiconductors, Multimedia**
Magazine Edition	Oct. 10	Sept. 19	Test & Measurement Special Issue, Oscilloscopes, VXI Board Directory • CAE/ASICs, Sensors & Transducers •
News Edition	Oct. 17	Sept. 27	ATE/Board & IC Testing, Artificial Intelligence**, Regional Profile: New Mexico & Arizona**
Magazine Edition	Oct. 24	Oct. 3	Telecommunications ICs, Graphics & Video Circuits, Computers & Peripherals, Software, Wescon Preview Issue

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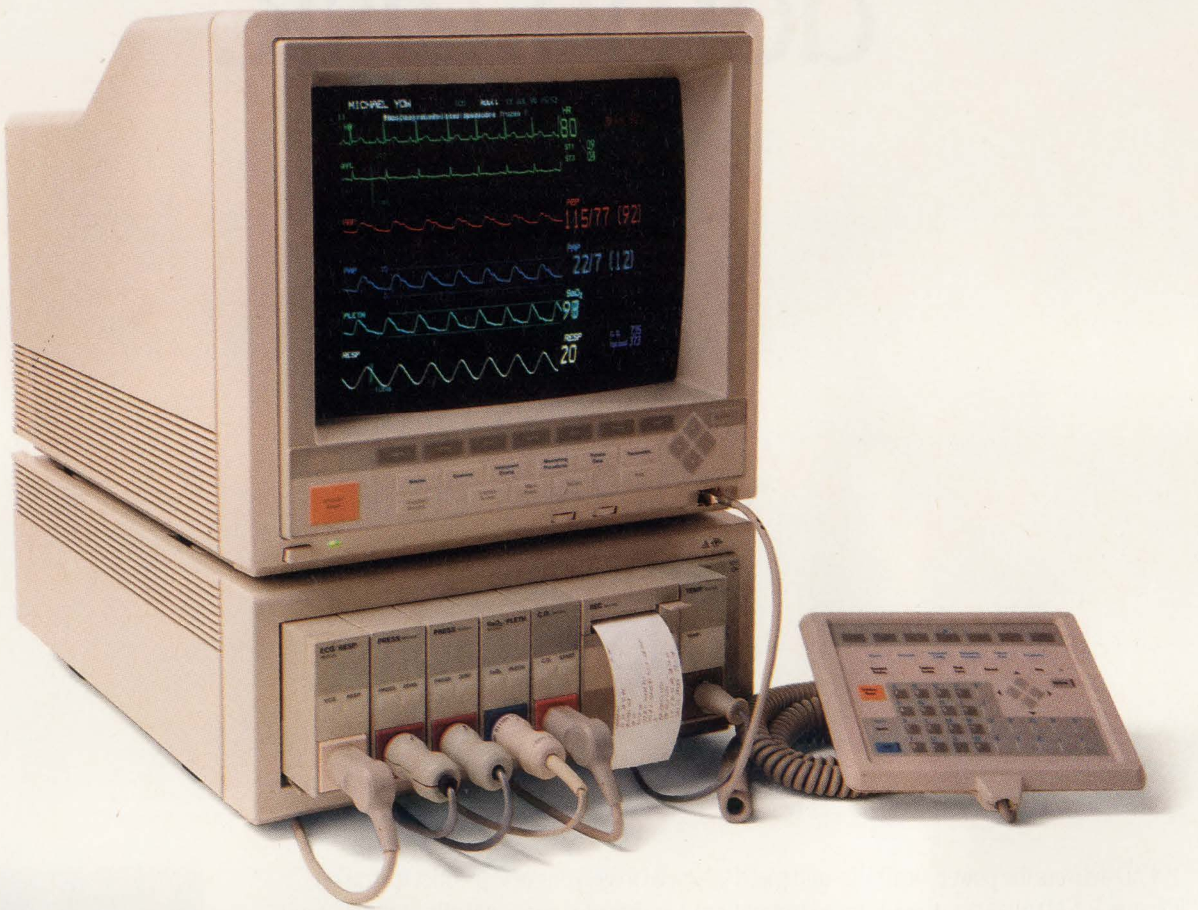

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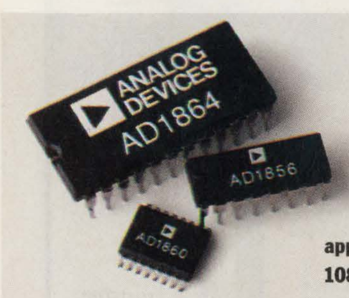

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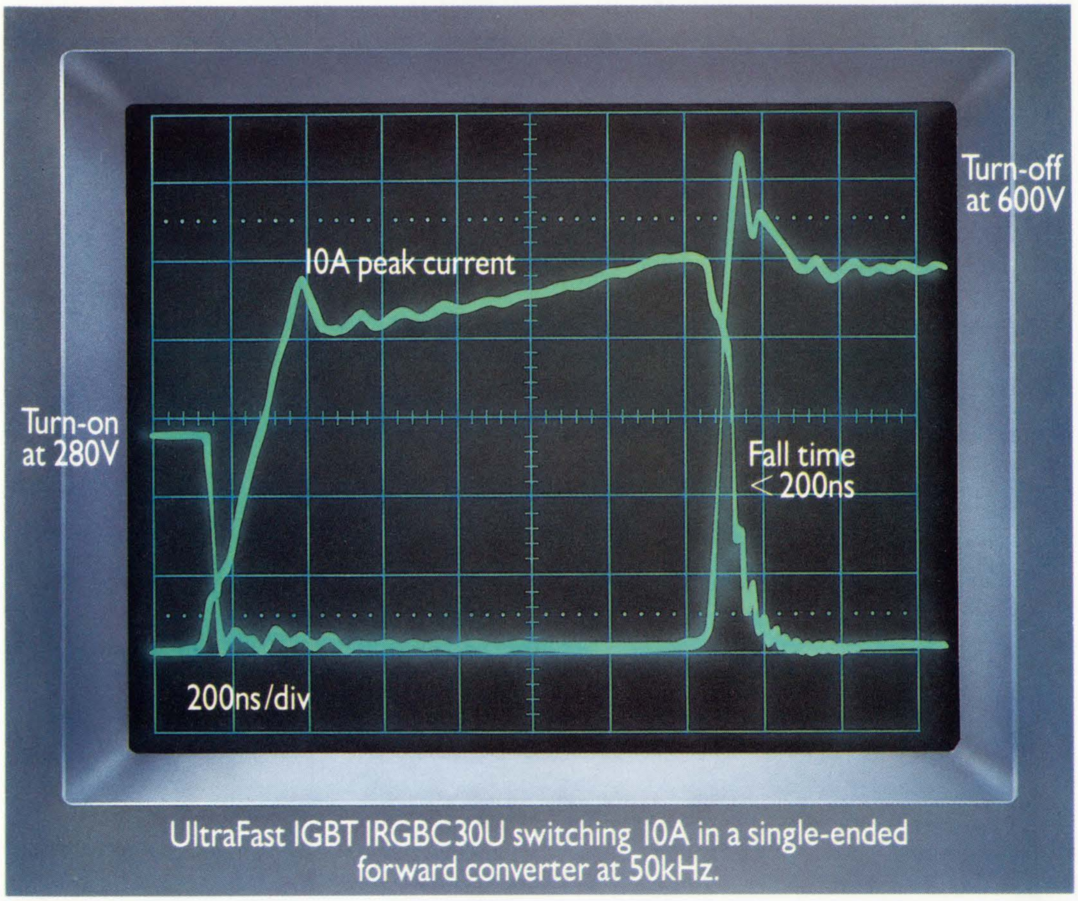

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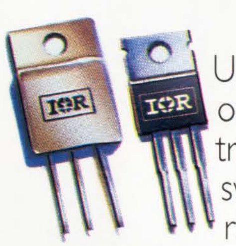

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