Special Report:
Competitive 3½-in. hard-disk drives erode demand for larger units  pg 72
Burr-Brown offers one of the industry's most complete line of high performance digital-to-analog converters. High quality and reliability are assured by our 35+ years of microcircuit design and manufacturing experience. Key features include:

- wide selection of 12-bit, 16-bit, and 18-bit resolution DACs with many performance options
- µprocessor-compatible DACs with double-buffered latches
- zero-chip interface DACs for digital signal processing and digital audio applications
- low cost, low power, CMOS DACs
- variety of package options

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**Complete 12-Bit**

- DAC813
  - ±1/2LSB linearity error
  - µprocessor interface
  - 270mW max power dissipation
  - compact 0.3" wide DIP SOIC
  - from $11.90*

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  - 8-bit, 12-bit, serial port interface
  - single +5V supply
  - 4 quadrant multiplying
  - 0.3" wide DIP, SOIC
  - From $12.35*

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- DSP201/202
  - zero-chip interface to most popular DSP ICs
  - 500kHz update rate
  - 90dB Signal-to-Noise + Distortion
  - -92dB THD
  - from $24.95*

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  - drop-in AD667 replacement
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  - fast 60ns digital interface
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Tucson, Az 85734
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**PRECISION TTL-CONTROLLED ATTENUATORS**

**up to 35dB**

10 to 1000MHz

**only $5995**

<table>
<thead>
<tr>
<th>TOAT 512</th>
<th>TOAT 124</th>
<th>TOAT 3610</th>
<th>TOAT 5020</th>
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<td>0.7</td>
<td>35.0</td>
<td>1.0</td>
</tr>
</tbody>
</table>

**Bold faced values are individual elements in the units**

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**SPECIFICATIONS**

<table>
<thead>
<tr>
<th>YSW-2-50DR</th>
<th>dc-500MHz</th>
<th>500-2000MHz</th>
<th>2000-5000MHz</th>
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</thead>
<tbody>
<tr>
<td>Insertion loss, typ (dB)</td>
<td>0.9</td>
<td>1.3</td>
<td>1.4</td>
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<tr>
<td>Isolation, typ (dB)</td>
<td>50</td>
<td>40</td>
<td>28</td>
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<tr>
<td>1dB compression, typ (dBm @ in port)</td>
<td>20</td>
<td>20</td>
<td>24</td>
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<tr>
<td>RF input, max dBm (no damage)</td>
<td>22</td>
<td>22</td>
<td>26</td>
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<tr>
<td>VSWR (on), typ</td>
<td>1.4</td>
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<tr>
<td>Video breakthrough to RF, typ (mV p-p)</td>
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<tr>
<td>Rise/Fall time, typ (nsec)</td>
<td></td>
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</tr>
</tbody>
</table>

*typ isolation at 5MHz is 80dB and decreases 5dB/octave from 5-1000 MHz

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SPECIAL REPORT

High-capacity 3½-in. hard-disk drives

New 3½-in. hard-disk drives have capacities exceeding 500M bytes and perform as well as high-end 5¼-in. units. The small drives are as reliable as 5¼- and even 8-in. drives and can be found in workstations, file servers, and drive arrays.—Maury Wright, Regional Editor

DESIGN FEATURES

Real-time programming—Part 9

The discussion of task coordination methods continues in Part 9 of this series with an overview of how semaphores and controlled shared variables coordinate tasks in real-time applications. Part 10 will discuss task coordination and communication via signals.—David L Ripps, Industrial Programming Inc

State-machine design curbs illegal states and transitions

You can learn theoretical state-machine design from myriad sources, but most neglect to tell you how to design state machines that work reliably. Such neglect is unfortunate—and unnecessary—because reliability is fairly easy to come by.—Ricardo Rabinovich, Librascope Corp

TECHNOLOGY UPDATES

Semicustom analog ASICs: 35

Design methods resist generalization

Designing an analog ASIC requires a tremendous amount of communication between system and IC designers.—Anne Watson Swagger, Regional Editor

PC-based logic simulators: 47

Device capabilities are growing

Improvements in hardware and software are making PC-based logic simulation an alternative to workstations and mainframes for small- and medium-sized designs.—Doug Conner, Regional Editor

Continued on page 7
Each StakPAC output is factory configured utilizing Vicor's robotically manufactured power converters...VI-200 series modules. Consider the advantages of a StakPAC customized for your system needs with automated power modules:

**USER DEFINABLE OUTPUTS**—The use of proven standard catalog modules offers the features of a custom without the associated risk or investment.

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For technical information contact Westcor at (408) 395-7050 or FAX (408) 395-1518 or call Vicor.

---

### STAKPAC STANDARDS

**1200 WATT MODELS**

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<thead>
<tr>
<th>Model</th>
<th>Output Voltage (VDC) and Maximum Current (amperes) per Channel</th>
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<tbody>
<tr>
<td>Single Output</td>
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<tr>
<td>SP1-1801</td>
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<td>SP1-1802</td>
<td>12 @ 100</td>
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<tr>
<td>SP1-1805</td>
<td>45 @ 25</td>
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<td>Dual Output</td>
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<tr>
<td>SP2-1801</td>
<td>2 @ 120</td>
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<tr>
<td>SP2-1802</td>
<td>5 @ 120</td>
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<td>12 @ 66</td>
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<tr>
<td>SP2-1804</td>
<td>15 @ 33</td>
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<td>Triple Output</td>
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</tr>
<tr>
<td>SP3-1801</td>
<td>5 @ 180</td>
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<tr>
<td>SP3-1802</td>
<td>12 @ 15</td>
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### MINI STAKPAC STANDARDS

**600 WATT MODELS**

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<tr>
<td>SEPT-1802</td>
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</table>
Timing-diagram design tools: Front-end tools reduce schematic drudgery

You can't draw a schematic until you find which timing requirements are critical. A new breed of computer tools takes the pain (and the pencil) out of this task. —Chris Terry, Associate Editor

EDITORS' CHOICE

32-bit µP chip for embedded computers

PRODUCT UPDATE

BiCMOS 20-copy clock-driver IC

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Buffers stabilize oscillator
Current loop controls SCRs
Regulator measures battery voltage
Programmable source operates precisely
Clamps provide self-test
Feedback and amplification

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Battery/float-chargers.

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—Anne Watson Swager

CAHNERS 1991 ECONOMIC FORECAST AVAILABLE TO READERS

Every year, Cahners Economics, the research and forecasting group at Cahners Publishing, compiles a list of trends and predictions for the coming year. The Cahners 1991 Economic Outlook reviews the economy in general, demographics, financial markets, and international markets. In addition, it has analyses of industries covered by Cahners publications, including electronics (semiconductors and components, computers and telecommunications, instruments and controls, military, and consumer). For EDN readers, the 57-pg book costs $11 (list price is $75). Cahners Economics, attn: Wendy Chambers, 275 Washington St, Newton, MA, (617) 630-2124, FAX (617) 630-2100.—Susan Rose

CMOS µP INCREASES SPEED

Zilog's Z280 16-bit µP now comes in a 12.5-MHz version that is 25% faster than the company's 10-MHz version. The µP has a 3-stage pipelined architecture, and an optional 8- or 16-bit data bus; it is code compatible with the company's 8-bit Z80 CPU. The µP's on-chip memory-management unit can address 16M bytes of memory and a 256-byte instruction and data cache. Other on-chip functions include three 16-bit counter/timers and a full-duplex UART. The $28 (1000) µP comes in a 68-pin plastic leaded chip carrier. Zilog, Campbell, CA, (408) 370-8000, FAX (408) 370-8056.—Dave Pryce

FUTUREBUS+ CHIPSET COMPLIES WITH IEEE STANDARDS

National Semiconductor Corp recently announced a Futurebus+ chip set that complies with the IEEE P896.1 and P896.2 specifications. The set consists of five ICs that use the company's backplane transceiver logic (BTL). The devices come in either plastic quad flatpacks or plastic leaded chip carriers. (Prices listed are for the flatpacks.)

The $7.70 (100) bipolar DS3883 is a 9-bit data transceiver that transmits and receives address, data, parity, command, and status signals. A 64-bit system requires 10 of these ICs. The IC has filters that eliminate glitches due to wire-ORed connections. The $28.75 (100) CMOS DS3875 arbitration controller supports the Futurebus+ distributed protocol and message passing in the central arbitration scheme. The
$13.90 (100) BiCMOS DS3885 is a 9-bit arbitration transceiver that communicates with the bus and the arbitration controller. The transceiver implements the arbitration-competition logic and performs parity checks. The $9.90 (100) BiCMOS DS3886 is a 9-bit latched-data transceiver, and the $13.90 (100) BiCMOS DS3884 is a handshake transceiver. National Semiconductor Corp, Santa Clara, CA, (408) 721-5000, FAX (408) 749-9071.—John Gallant

QUADRUPLE CMOS COMM DEVICE SAVES BOARD SPACE

VLSI Technology Inc's VL16C554 combines the abilities of four ICs in a single chip. The chip has four VL16C550 UARTs, each with its own 16-byte data FIFO circuit, and suits applications that involve intensive data communication in PCs, terminal cluster controllers, or statistical multiplexers. The chip's four CMOS asynchronous communications elements act as serial data I/O interfaces that perform serial-to-parallel conversion on data characters received from peripheral devices, such as modems. The VL16C554 comes in an 84-lead plastic leaded chip carrier and costs $63 (1) or $32 (1000). VLSI Technology Inc, Tempe, AZ, (602) 752-8574, FAX (602) 752-6000.—J D Mosley

WINDOWS-BASED DSP DEVELOPMENT SOFTWARE SUPPORTS OOP

Signal Technology Inc's NiPower 1.0 is an object-oriented Windows-based development framework for digital-signal-processing applications. It lets you prototype your application rapidly because it treats individual data files and software modules as objects. You string together the data, algorithms, and hardware control functions drawn from both the framework library and third-party software using a Lisp-based symbolic language to define the procedures. The framework runs on a Sun SPARC or VAX workstation and costs $6000. The framework package supplies the X-Window interface, an object-oriented high-level application language, 2- and 3-D graphics capability, and a library of signal- and data-analysis functions. You can add modules to the framework, including a library of DSP algorithms, DSP-chip code generators, and control for selected A/D and D/A devices. You can also acquire a module that lets you add third-party software to the framework. Modules cost from $250 to $3750. Signal Technology Inc, Goleta, CA, (805) 968-3000, FAX (805) 968-2620.—Richard A Quinnell

MEMORY-CELL STRUCTURE LIMITS LEAKAGE IN DRAMs

Toshiba America Electronic Components is researching a memory cell that provides 0.6 µm of separation between the crucial regions of trench cells in dynamic RAMs (DRAMs), even with 0.4-µm design rules. The company is developing the cell because conventional methods of building trench cells for DRAMs won't scale to 64M-bit densities. Because of their proximity to each other, leakage between adjacent trench cells, and from active areas to the storage capacitors within cells, results when IC geometries shrink. The memory cell uses a thin insulating layer of oxide on the surface of each trench capacitor to prevent leakage. In addition, the memory cell uses an asymmetric and offset trench, rather than the parallel alignment of conventional trenches. Toshiba America Electronic Components, Irvine, CA, (714) 455-2000, FAX (714) 859-3963.—Michael C Markowitz
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low pass dc to 1200MHz

<table>
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<th>MODEL NO.</th>
<th>PASSBAND, MHz (loss &lt;1dB)</th>
<th>fco, MHz (loss 3dB)</th>
<th>STOPBAND, MHz (loss&gt;10dB)</th>
<th>VSWR</th>
<th>PRICE</th>
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high pass dc to 2500MHz

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bandpass 20 to 70MHz

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narrowband IF

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<th>Vendor</th>
<th>Platform</th>
<th>O.S. &amp; Application</th>
<th>Design Kits</th>
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EDN February 4, 1991
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Reader notes competent reporting on neural networks
Maury Wright's article, "Neural networks tackle real-world problems" (EDN, November 8, 1990, pg 79), is the sort of in-depth reporting that should stimulate more designers to investigate the benefits of neural networks. Many companies are using this technology to reduce costs and improve quality.

Maury referred to our C25 accelerator board as having a price range of $2500 to $4150. The company now offers only the high-end zero-wait-state board at $1995.

Mark Lawrence
President
California Scientific Software
Grass Valley, CA

Price of optical-disk drive
The price of the RMD-5100-S 3½-in. rewritable optical-disk drive from Most Inc did not appear in the New Product write-up (EDN, December 20, 1990, pg 118) because it was not available when this issue went to press. The RMD-5100-S drive costs $2450; the price of $120 is for the cartridges only.

Phone-number correction
Two digits in the phone number for Xitron Technologies Corp (EDN, December 20, 1990, pg 149) were inadvertently transposed. The correct number is (619) 458-9852.

Software correction file available on EDN BBS
The correction file for the software in Fred Salvatti's article, MS152 (EDN, August 20, 1990, pg 141) is available on EDN's Bulletin Board Service (BBS), /freeware SIG, (617) 558-4241 (2400,8,N,1).

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EDN's Signals & Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. You can use one of several easy ways to reach us. First, there's always the mail. Send your letters to Signals & Noise Editor, EDN Magazine, 275 Washington St, Newton, MA 02158. Or, send us a message via MCI mail at EDNBOS. Finally, EDN's bulletin-board system is ready for use—and it's free (except for the phone call). You can reach us at (617) 558-4241 and leave a letter in the EDITORS Special Interest Group. You'll need a 2400-bps or less modem and a communications program that is set for eight data bits, no parity, and one stop bit, or 2400, 8N1 in shorthand.

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EDN February 4, 1991
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EDITORIAL

Where are the experimenters?

Electronics used to be a fun hobby. I remember my first experiments with electricity. My grandfather, an electrician, wired up a selection of switches, bulbs, buzzers, and bells on small wooden blocks so I could connect them and try out various circuits. Those first circuits led me to explore crystal radios, a 1-tube receiver, plug-board experimenter kits, and, later, kits from Heathkit, Lafayette Radio, and Allied Radio. I tried out a lot of ideas and circuits—even though I didn’t always know what I was doing. I recall a particularly neat breadboard that supplied components on yellow plastic mounts that fit into a large sheet of perforated wooden board. Special jumper clips connected the components. The explanations in the accompanying manual told me how the circuit worked and what each component did.

New York City held a special lure for teenagers like me growing up on Long Island. Many of us wanted to “go to the city” to sample nightlife, see a play, or visit a museum or library. Instead, at 15, my first solo trip to New York took me to Canal Street, an experimenter’s paradise where electronic-surplus stores lined a quarter-mile stretch of this downtown street. The stores offered relays, switches, surplus computer boards, military radios, and even old teletypewriters. When you needed a part, you found it on Canal Street.

Much of Canal Street is now history, and I’m afraid that much of the hobby of electronics is, too. I’m always surprised at this time of year by the lack of “101-electronic experiment” kits, chemistry sets, and microscopes in the toy stores. It seemed not long ago that kids enjoyed technical toys. These days, many toys and games use electronic components, but the kids don’t know it and don’t appreciate what electronics does for them. (Maybe they just haven’t had the chance—safety concerns with some of these sets seem to have cleared the shelves of nearly all experimenting toys.)

Most of the hard-core electronics hobbyists and experimenters I knew in high school went on to become talented engineers or scientists. I’m convinced that their early hands-on experience with electronics further advanced their learning and their careers. Perhaps they succeeded because they had developed a feel for things electronic, a love for the technology, and a deep enthusiasm for new possibilities.

The engineering profession is poorer for not giving youngsters the opportunities to experience electronics firsthand, particularly when they’re open-minded and awed by technical things. Yet, it’s difficult to give them that opportunity. For example, few of the young people I know are interested in amateur radio. With cellular phones, fax machines, and computers and modems, who’s thrilled by 2-way Morse-code communication with a person in New Zealand? Likewise, small, inexpensive radios and stereos are easy to buy on most kids’ allowances. That makes it completely unattractive to build a short-wave receiver. Why bother?

On the other hand, we don’t have legal or medical hobbyists, yet our colleges and universities turn out many fine lawyers and physicians who get almost all of their experience in formal surroundings. Maybe the lack of electronics as a hobby or avocation doesn’t harm the engineering profession after all. It’s possible, though, that we might have even better doctors, lawyers, and engineers if they got some realistic exposure to medicine, legal matters, and electronics before they chose a profession.

Jon Titus
Editor

Jesse H Neal
Editorial Achievement Awards
American Society of Business Press Editors Award
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CIRCLE NO. 71
Designing an analog ASIC requires a tremendous amount of communication between system and IC designers.

Anne Watson Swager, Regional Editor

Design methods resist generalization

Choosing the appropriate design method for your analog ASIC can reduce much of the design risk currently associated with these ICs (see box, "Recognize risks to reap rewards"). Making this choice is not trivial because many variations of each basic method exist. Regardless of whether you, the vendor, or an independent designer or fabless design house do the majority of the designing, a close working relationship among all concerned parties is the only way to ensure design success.

Analog-ASIC design methods fall into two general categories: full custom and semicustom. Full-custom ASICs are completely handcrafted from bare silicon, generally by an experienced IC designer.

Semicustom analog ASICs split into array-based and standard-cell designs. Traditional component arrays consist of a slate of transistors, resistors, and capacitors on a piece of prefabricated silicon. Tile arrays comprise fixed circuit blocks. Each block contains a fixed number and type of active and passive components. For both types of arrays, the designer's job is to connect the elements by defining one or sometimes two final metallization layers.

Standard-cell designs start out as a blank slate. By defining the functions you want from the vendor's library—or by specifying some new cells of your own—you create the entire mask set for the chip. The vendor has already designed and characterized the cells' corresponding mask sets. Most vendors of cells and arrays have some capacity to place digital gates on their ICs. These vendors still consider themselves analog vendors, despite the mixing of analog and digital circuitry.

Full-custom ICs clearly make the best use of their die area, but they incur the longest design times and highest NRE costs. Standard cells place second on the silicon-efficiency scale. You choose only the exact circuit elements you need. However, standard-cell designs are only half a step from full custom. Rarely does a vendor's library contain all the cells you need; the vendor must often create new "custom" cells.

Arrays trade a standard-cell design's
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Semicustom analog ASICs

efficient use of silicon for lower NRE costs and faster turnaround times. Tile arrays constrain a design if that design calls for an element or number of elements not on the array. Also, tile arrays may waste silicon by leaving some passive or active components unused.

Volume will also influence your design-method choice. For example, if you’re planning to build a small number of ICs, a tile array will get you started with less NRE costs. Also, many vendor’s fabrication processes and design methods may only be viable for high-volume customers (many vendors define high volume as 100,000 to 250,000 units per year). Unless a vendor has a substantial business interest in your particular application area, you may not be able to find a company to build your chip in small volumes.

Now, the exceptions

Unfortunately, these generalizations about design methodologies make choosing a design approach sound cut and dried. It’s not. For one thing, analog-ASIC design capabilities are changing fast. Table 1 can serve as a guide, but tables tend to oversimplify the design choices. The equivalent of the digital gate array does not exist in the analog world. There’s no consensus or well-accepted standard approach to designing analog ASICs.

For example, making assumptions about the process technology you need may be risky. Analog ASICs can be CMOS, bipolar, or BiCMOS. You might assume that you have to use a bipolar process to build a function with a particular performance level, but even the vendors themselves are surprised at what they can accomplish with CMOS processes. Don Bartlett, an analog-design project leader at NCR Microelectronics, says his company now has a 10-bit ADC as a standard cell—a goal engineers didn’t think they could achieve a year ago.

Both standard cells and arrays are changing in ways that either minimize or remove their previous limitations. Tools continue to become available to system designers. Large and well-established semiconductor companies such as Texas Instruments, Motorola, National

Recognize risks to reap rewards

Analog ASICs are laden with many design risks and tool shortcomings that digital ASICs have long since overcome. Common design problems include isolating noise, isolating the substrate, interfacing the chip with external electronics, and keeping NRE costs low and all schedules short. Designers measure the “first-time silicon success” of analog ASICs functionally. Many analog ICs work on the first pass, but they often require some form of tweaking to perform exactly as you want.

Inadequate tools and the lack of test methods are the two big stumbling blocks for analog and mixed-mode ASICs. Spice and its derivatives serve many pure analog designs well, but capable mixed-mode simulation tools are just beginning to become available. Worst-case modeling is difficult, and vendors don’t guarantee a part will work based on simulation results alone.

No systematic or widely accepted test method for analog ASICs exists. Vendors don’t have much to say about test except that they’re working on it. They do say that testing a highly embedded function requires early planning on how the testing equipment will access the chip.

The good news is that you don’t necessarily need expensive tools to design analog ASICs. Many vendors have made IBM PCs and compatibles their hardware of choice. Other design methods don’t even require that you simulate the ASIC because you’re combining proven building blocks. Micro Linear’s semistandard ICs let you specify a combination of proven circuits. Advanced Linear Devices provides building blocks identical to those of the final IC. You can connect these blocks and troubleshoot them on a pc board.
Semicustom analog ASICs

Semicustom analog ASICs have much experience designing analog and mixed-signal ASICs. These companies will design semicustom ICs for you, as will other companies listed in Table 1, using their proprietary tools and standard cells. They generally work with very-high-volume customers and only make their tools available to special customers. However, these companies envision a time when tools will be available to all their customers. Within the next couple of years, TI will make parts of its

Table 1—Representative semicustom analog ASIC design methods

<table>
<thead>
<tr>
<th>Manufacturer/Corporation</th>
<th>Product Type/Design</th>
<th>Design Method</th>
<th>Vendor/customer relationship</th>
<th>Process/Technology</th>
<th>Typical NRE Costs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advanced Linear Devices</td>
<td>Function specific linear ICs</td>
<td>Cell based with standard products</td>
<td>Customer designs</td>
<td>CMOS</td>
<td>$20,000 to $50,000</td>
</tr>
<tr>
<td>Analog Devices</td>
<td>Mixed-signal ASICs</td>
<td>Cell based</td>
<td>Turnkey supplier only</td>
<td>BiCMOS</td>
<td>$50,000 to $100,000</td>
</tr>
<tr>
<td>AT&amp;T Microelectronics</td>
<td>CBIC process</td>
<td>Array based</td>
<td>Customer/vendor designs</td>
<td>Bipolar</td>
<td>$30,000 to $50,000</td>
</tr>
<tr>
<td>Cherry Semiconductor</td>
<td>Genesis</td>
<td>Array based</td>
<td>Customer designs</td>
<td>Bipolar</td>
<td>$10,000</td>
</tr>
<tr>
<td>Custom Arrays Corp</td>
<td>MM/MV</td>
<td>Array based</td>
<td>Customer designs</td>
<td>Bipolar</td>
<td>$5000 to $15,000</td>
</tr>
<tr>
<td>Exar</td>
<td>Flexar</td>
<td>Array based</td>
<td>Customer designs</td>
<td>Bipolar</td>
<td>$2500 to $9500</td>
</tr>
<tr>
<td>Gould AMI</td>
<td>Mixed-signal design solution</td>
<td>Cell based</td>
<td>Customer designs</td>
<td>CMOS</td>
<td>$50,000 to $70,000</td>
</tr>
<tr>
<td>Harris Semiconductor</td>
<td>Mixed-signal, analog and power ASICs</td>
<td>Cell based</td>
<td>Customer designs</td>
<td>Bipolar, CMOS, BiCMOS</td>
<td>From $40,000</td>
</tr>
<tr>
<td>ICS</td>
<td>Mixed-signal ASICs</td>
<td>Cell based</td>
<td>Turnkey supplier only</td>
<td>CMOS</td>
<td>$30,000 to $70,000</td>
</tr>
<tr>
<td>International Microelectronic Products</td>
<td>Mixed-signal ASICs</td>
<td>Cell based</td>
<td>Turnkey or joint designs</td>
<td>CMOS, NMOS</td>
<td>$90,000</td>
</tr>
<tr>
<td>Micro Linear Corp</td>
<td>Semistandard ICs</td>
<td>Array and cell based</td>
<td>Turnkey supplier only</td>
<td>Bipolar, CMOS</td>
<td>$5000 to $50,000</td>
</tr>
<tr>
<td>Motorola</td>
<td>Mixed-signal ASICs</td>
<td>Cell based</td>
<td>Turnkey or joint designs</td>
<td>CMOS bipolar</td>
<td>$30,000 to $55,000</td>
</tr>
<tr>
<td>National Semiconductor</td>
<td>Classic</td>
<td>Cell based</td>
<td>Turnkey or joint designs</td>
<td>Bipolar, CMOS, BiCMOS</td>
<td>$45,000 to $65,000</td>
</tr>
<tr>
<td>NCR Microelectronics</td>
<td>Mixed-signal ASICs</td>
<td>Cell based</td>
<td>Turnkey or joint designs</td>
<td>CMOS</td>
<td>$40,000 to $50,000</td>
</tr>
<tr>
<td>Plessey Semiconductor Corp</td>
<td>ULA mixed-signal ICs</td>
<td>Array based</td>
<td>Turnkey or joint designs</td>
<td>Bipolar</td>
<td>$5000 to $6500 (customer designs) from $18,500 (turnkey designs)</td>
</tr>
<tr>
<td>Raytheon Semiconductor</td>
<td>RLA, RFA</td>
<td>Array based</td>
<td>Customer designs</td>
<td>Bipolar</td>
<td>From $21,000</td>
</tr>
<tr>
<td>SGS-Thomson Microelectronics</td>
<td>ANACA mixed-signal and linear ASICs</td>
<td>Array and cell based</td>
<td>From turnkey to customer designs</td>
<td>Bipolar, CMOS, BiCMOS</td>
<td>$30,000 to $75,000 (standard cell) $25,000 to $40,000 (arrays)</td>
</tr>
<tr>
<td>Sierra Semiconductor</td>
<td>Mixed-signal ASICs</td>
<td>Cell based</td>
<td>Turnkey or joint designs</td>
<td>CMOS</td>
<td>$20,000 to $120,000</td>
</tr>
<tr>
<td>Tektronix</td>
<td>QuickFile</td>
<td>Array based</td>
<td>Customer designs</td>
<td>Bipolar</td>
<td>$85,000 to $91,000</td>
</tr>
<tr>
<td>Texas Instruments</td>
<td>LinASIC</td>
<td>Cell based</td>
<td>Primarily turnkey</td>
<td>Bipolar, CMOS, BiCMOS</td>
<td>$50,000 to $150,000</td>
</tr>
</tbody>
</table>

Note: The mixed analog/digital methods included in this table have the ability to integrate large amounts of analog circuitry. Vendors that offer primarily digital ASICs with only a small analog portion are not included here.
tools compatible with Mentor Graphics' Falcon framework. Gould AMI is announcing the final version of its Mixed-Signal Design Solution system this quarter. The system will include model-building software that lets you create cells in house.

Categorizing array-based methods is difficult. Array-based methods range from AT&T's high-speed, high-performance CBIC process to Advanced Linear Devices' standard IC building-block approach. Many arrays now have features that minimize their previous limitations, too.

First of all, designing with tile arrays doesn't require designing exclusively with discrete transistors, capacitors, and resistors. Instead of transistors, for example, Raytheon Semiconductor uses gain blocks as the basic element in its arrays. Most tile-array vendors feature macrocells and defined tiles. In most cases, these tiles are located at specific locations on the tile array.

For example, Cherry Semiconductor's Genesis 5200 high-frequency array features a programmable bandgap voltage reference on the lower-left edge of the array. You can program the reference's voltage between 1.25 and $V_{CC} - 2V$. By using a fuse-link trim option, you can achieve a voltage deviation of $\pm 3.5\%$. You can internally structure the tile in four configurations.

SGS-Thomson's TSFJ series of mixed bipolar arrays also have built-in bandgap references in addition to tiles for oscillators, voltage regulators, and R-2R ladders for a 6-bit DAC. Raytheon's RLA ICs consist of op-amp cells, comparator cells, and thin-film resistors. Plessey's ULA DA family of analog/digital arrays include a bandgap reference, voltage regulators, low-offset transistors, matched precision resistors, capacitors, and 120-mA transistors.

Tile arrays suit many applications, including military ones. Late last year, Harris Semiconductor announced the dielectrically isolated HTA2000 analog tile array. The two versions of the array meet class S and class B reliability requirements. The dielectric isolation lets the arrays use both vertical npn and pnp transistors. The arrays' library features:

<table>
<thead>
<tr>
<th>Typical turnaround times (weeks)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 to 16</td>
<td>User designs and breadboards the ASIC with completely specified, standard ICs provided by the vendor. Specializes in low-power designs.</td>
</tr>
<tr>
<td>24 to 52 from signed specification</td>
<td>NRE charge includes all design and fabrication to deliver final packaged and tested silicon. Specializes in high-performance (12-bit accuracy) circuits.</td>
</tr>
<tr>
<td>6 to 8</td>
<td>High-speed and high-performance process. Some arrays are laser trimmable. Building block kits are available. Vertical npn and pnp transistors.</td>
</tr>
<tr>
<td>8 to 12</td>
<td>Company maintains BBS for users to transfer design information (1-800-272-2447).</td>
</tr>
<tr>
<td>4 to 8 from layout</td>
<td>Macrocell library contains amplifiers, comparators, timers, regulators, buffers, flip-flops, S/H amplifiers, and Schmitt triggers. Kit parts available. Company sells design software for 386-based IBM PC.</td>
</tr>
<tr>
<td>3 to 6</td>
<td>Designer can move tiles to different locations and can create either an npn or a pnp transistor in a given location. Macro library of proven circuits.</td>
</tr>
<tr>
<td>From 20</td>
<td>Model-building software lets designers create models in house.</td>
</tr>
<tr>
<td>6 from final design</td>
<td>Tile arrays and standard cells part of FastTrack design system. Runs on Unix workstations.</td>
</tr>
<tr>
<td>16 to 20 from first specification</td>
<td>Design services include &quot;free-look&quot; prototyping. Vendor can make changes at this stage without scrapping masks and prototype wafers. Specializes in low-power designs, not locked into 5V process.</td>
</tr>
<tr>
<td>22 to 24</td>
<td>Also offers manufacturing services for customer designs.</td>
</tr>
<tr>
<td>6 to 14 (bipolar) 12 to 24 (BiCMOS) after design verification</td>
<td>You create a semistandard IC by modifying an existing standard product.</td>
</tr>
<tr>
<td>6 from simulation</td>
<td>Company provides engineering design assistance for $3000/week. NRE and lead times are quoted for company's MOS products.</td>
</tr>
<tr>
<td>12 to 16 (conception to first prototype)</td>
<td>1-week training course is free to customers and $1000 for others. Dense bipolar process yields high integration.</td>
</tr>
<tr>
<td>10.5 from design review</td>
<td>Accurate cell models have timing information from silicon built in. Turnaround time includes customer-performed post-simulation layout. High-performance CMOS.</td>
</tr>
<tr>
<td>4 to 12</td>
<td>Library of analog and digital macro functions. Special cells located at chip corners. 5-mask process keeps costs down.</td>
</tr>
<tr>
<td>6 to 8 from design verification</td>
<td>Macrocell op amps and comparators. Dual-layer metal. Thin-film resistors. Kit parts available.</td>
</tr>
<tr>
<td>6 to 9 (standard cell) 3 to 4 (arrays)</td>
<td>Tiles have kit parts. Macrocell library includes op amps, comparators, timer/oscillator, video amplifier, bandgap reference, transconductance amp Schmitt trigger, NOR, NAND, flip-flop, and DAC.</td>
</tr>
<tr>
<td>9</td>
<td>Company has large library of cells. Process technology combines analog and digital circuitry and EEPROM.</td>
</tr>
<tr>
<td>10</td>
<td>Startup package with software and training course costs $15,000. Software runs on Sun workstation. High-speed designs, accurate models.</td>
</tr>
<tr>
<td>16 to 52</td>
<td>Specializes in high-performance, high-integration designs.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>NRE and lead times</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specializes in high-performance designs.</td>
<td></td>
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<td></td>
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</tr>
</tbody>
</table>

EDN February 4, 1991
Semicustom analog ASICs

of cells includes op amps, comparators, S/H amplifiers, buffers, references, and differential video circuits.

**Tile arrays get more flexible**

Possibly the biggest design deterrent to using tile arrays is their inflexibility, but vendors are coming up with ways to make tile arrays more flexible. Tektronix's QuickTiles, relatives of the company's QuickChip family of ICs, combine full-custom fabrication with a tile-like design method. Designers define the circuit by snapping together standard tiles at any desired location on a coarse grid. Because the location of the devices in the arrays varies, all mask levels must be generated and the wafers must be fabricated from bare stock. The grid eliminates the risk of violating layout rules.

Both Exar and Custom Arrays Corp (formerly Interdesign) have tile arrays from which you can create either pnp or npn transistors. Exar's Flexar array lets you select either an npn or a pnp transistor from the same location using a single layer of metal. Custom Arrays' MV array has what the company calls a pnpn structure. The pnpn elements can serve either as lateral pnp or normal npn transistors. The arrays have a modular structure of cells that repeats throughout the chip. Thus, you can place macro functions anywhere on the array. Flexar's arrays come with a soft-macro library of proven circuits as well as kit parts and Spice device models.

**References**


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TECHNOLOGY UPDATE

PC-BASED LOGIC SIMULATORS

Device capabilities are growing

If you're already using a personal computer for CAD/CAE applications, you will find that you can use it for logic simulation as well. Before examining the details of PC-based simulation, it's worth looking at what simulation can offer you. Logic simulation software typically provides three types of simulation: functional, timing, and fault.

Functional simulation, normally the first step in verifying a design, checks the circuit's logic to see that it works the way you expect it to. Functional simulation typically uses unit timing delays instead of accurate timing models for component behavior. At the functional simulation level, you can find problems, such as inverted signals and improper sequential or combinatorial logic.

Once you've determined that the circuit executes the proper functions, you can concentrate on the timing simulation. Timing simulation makes more detailed demands of the simulator and the models used in the simulation. Therefore, accurate results require accurate models of the hardware.

Timing simulations often use gate-level representations. To simulate a circuit's operation more accurately, however, some designers use a switch-level representation, especially in IC design. Switch-level models represent the circuit at the transistor level, giving a more accurate simulation of the electrical characteristics. However, not every simulator supports switch-level modeling (see Table 1).

Fault simulation is useful for test operations where you want to find stuck-at-one and stuck-at-zero faults. A fault simulation uses a set of test or stimulus inputs to check out a design, finding the percentage of cases where stuck-at-one and stuck-at-zero faults are detected. Fault simulations are often useful when developing IC test programs.

Before you can reap the benefits of logic simulation, you have to go through three steps: entering the design, obtaining models for the components, and generating a set of stimulus or test vectors.

The usual method for entering a design into a logic simulator is via a netlist that describes how the components in the circuit are connected. Simulators

Improvements in hardware and software are making PC-based logic simulation an alternative to workstations and mainframes for small-and medium-sized designs.

Doug Conner, Regional Editor
MEGA MEMORY.

<table>
<thead>
<tr>
<th>MODEL</th>
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<td>CXK581000P*</td>
<td>128K x 8</td>
<td>100/120</td>
<td>DIP 600 mil</td>
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<tr>
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<td>100/120</td>
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<tr>
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<td>SOP 525 mil</td>
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<td>128K x 8</td>
<td>35/45/55</td>
<td>SOJ 400 mil</td>
<td>L</td>
</tr>
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</table>

*Extended temperature range available.

L = Low power.
LL = Low, low power.

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PC-based logic simulators

typically accept netlists from various schematic-capture software packages.

The simulator also needs component models to simulate what each component does, both functionally from a logic standpoint, and for timing characteristics if you are performing a timing simulation.

You need either to purchase model libraries that cover the devices you are simulating or develop your own models. Simulation vendors usually provide model libraries or offer them as an option. If they don't, you can often buy the libraries from third-party vendors.

Don't assume all the models that you need are available. When shopping for a logic simulator, check out the available model libraries carefully, unless you are planning to develop your own models. Although the functional characteristics of models are usually straightforward, timing characteristics can vary considerably in their accuracy.

The model may measure only average timing characteristics, or be able to measure minimum, maximum, and average timings. In addition, the model may or may not have accurate data concerning correct setup, hold, reset, and clock intervals.

Even if you plan to use models from existing libraries, you should be aware of the methods available for generating models yourself. Undoubtedly you'll run into cases where you cannot find a model, or perhaps you need to modify a model to look at special behavior.

Developing your own models

To build logic models, you typically use the logic-primitive models provided with the simulator. These primitives include basic logic functions, such as AND gates, OR gates, and storage functions. High-level primitives, such as D and JK flip-flops, latches, RAM, and ROM may also be available. In addition to the logic functions, you need to know what timing constraints are included with the logic primitives.

For example, OrCAD's primitives have minimum and maximum gate delays. The storage primitives have setup and hold times and minimum clock-width parameters.

Building models up from primitives isn't the only way to develop your simulation. Behavioral or hardware description languages (HDLs) are another option on some simulators. For example, Viewlogic has an optional VHDL (VHSIC hardware description language) for modeling and simulation. Aldec's Mobic/T is a high-level IC modeling language for the company's Susie (standard universal simulation for improved engineering) series of logic simulators.

SimuCAD supplies the Silos behavioral modeling language for the company's Silos II logic simulator. You can use the modeling language to develop behavioral models that

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Product</th>
<th>Libraries available</th>
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<td>Aldec Susie 4</td>
<td>TTL2, CMOS, ECL, memory, ( \mu P, ) PLD, FPGA</td>
<td>Gate, behavioral</td>
<td>IBM PC/XT, PC/AT, PIC/CS</td>
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<td>Timing option $1495</td>
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<td>Timing option $2495</td>
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<td>Gate, behavioral</td>
<td>IBM, 386/486, compatible</td>
<td>$1995</td>
<td>Timing option $3995</td>
<td></td>
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<tr>
<td>OrCAD</td>
<td>VST</td>
<td>TTL2, CMOS2, ECL2, memory2</td>
<td>IBM PC/XT, PC/AT, PIC/CS</td>
<td>$995</td>
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<tr>
<td>SimuCAD</td>
<td>Silos II/386</td>
<td>7400 series2</td>
<td>Switch, gate, behavioral</td>
<td>IBM, 386, compatible</td>
<td>$2500</td>
<td>Fault simulation</td>
</tr>
<tr>
<td>MacSim IIs</td>
<td>7400 series2</td>
<td>Switch, gate, behavioral</td>
<td>Apple Macintosh II</td>
<td>$2500</td>
<td>Fault simulation</td>
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<td>P/C Silos</td>
<td>7400 series2</td>
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<td>$1000</td>
<td>Limited version $400</td>
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<tr>
<td>Tanner</td>
<td>Gatesim</td>
<td>ASIC, FPGA, custom IC</td>
<td>Gate</td>
<td>IBM PC/XT, PC/AT compatible</td>
<td>$1295</td>
<td>Fault simulation</td>
</tr>
<tr>
<td>Viewlogic</td>
<td>Viewsim/SD</td>
<td>ASIC, TTL, ECL, CMOS, memory, FPGA, PLD, ( \mu P )</td>
<td>Switch, gate, behavioral</td>
<td>IBM, 386, P3/2 compatible</td>
<td>$7500 to $19,000</td>
<td>Virtual memory supported</td>
</tr>
</tbody>
</table>

Notes: 1. Optional unless otherwise noted.
2. Included in package.
3. Only available from third-party vendors.
PC-based logic simulators replace devices or blocks of devices in your simulation.

Behavioral or high-level description models let you design your circuit from the top down. The higher-level descriptions have faster simulation speeds than low-level descriptions, which can save development time.

Stimulus for the simulation

After you've entered the circuit's netlist and models for the components, the only remaining task is generating a set of stimulus or test vectors.

Developing stimulus vectors, and subsequently the correct response for them, is an important and potentially time-consuming part of the simulation process. The simulator can only help you verify whether a circuit design works properly by exercising the circuit simulation with input stimulus and knowing how the circuit should respond.

When developing test vectors, you typically need to concentrate on two different concerns. The first concern is making sure the circuit does everything it should do so that the design meets its specifications.

The second concern is to make sure the design doesn't do anything it should not do. For this you need to verify that the circuit behaves correctly with any legal input, and possibly with illegal inputs.

For example, if you are simulating a design for a circuit that receives its inputs from a bus, then you can test only the legal bus-cycle inputs and ignore what happens with illegal bus cycles. If you think illegal bus cycles will occasionally occur, you should test the circuit design for them. Although your design may not need to function properly with illegal bus cycles, you want to avoid a locked-up condition requiring a system reset. Therefore, you need to generate the test vectors to check out potential problems.

Simulators typically let you generate test vectors using equations, tables, or a mouse. Aldec's Susie series lets you draw test vectors manually, using a mouse, or create them using equations. OrCAD's VST includes a pop-up editor for generating stimulus vectors that lets you define as many as 200 signals. You can generate clock signals in relative or absolute formats.

When you enter your design into the stimulus vectors, you are ready to run the simulation and see the results.

The usual format for simulator output is similar to a logic-analyzer timing display. The simulator presents the signal's state vs time or, in a bused format, it presents data states shown in binary, octal, decimal, or hex.

Simulators don't just leave you to hunt through these outputs for problems. They provide a variety of tools to help you zero in on problems. For example, breakpoints are available on some of the simulators, such as VST and the Susie series. Breakpoints let you look for specific logic conditions occurring when you run a simulation.

Simulators can also look for certain errors automatically. Most will flag setup and hold time violations, minimum pulse-width violations, or bus-contention cases where two devices attempt to drive a bus simultaneously. Some simulators detect race conditions, oscillations, and spikes.

Help for finding bugs

When you run a simulation and see incorrect results, you need to find the source of the problem and fix the error. Something as simple as an inverted output won't take a master sleuth to find and correct. Other errors start much further back in the logic cycle and will take some careful backtracking to get from the point where you observed
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PC-based logic simulators

the error to where it originated. Tracking problems and debugging a design at the simulation level can take a considerable amount of time. Therefore, tools offered by the simulation vendor to speed the debug process should be carefully considered.

For example, Silos II has a 2-dimensional interactive debug capability (time and topology). When you discover that a node has made a transition to an incorrect state, you can interactively trace the cause backward in time and look at the inputs that drive the node. You can continue to work your way back in time and device inputs until you reach the source of the problem. You can also trace node outputs to forward destinations.

Silos II also supports spike simulation. A spike occurs when two or more edge transitions arrive at a device's input and the edges are spaced closer to each other in time than the propagation delay of the device, causing a state change in the device. Instead of swallowing the spikes, the simulator makes them visible, allowing you to trace them to their source. You can also track the influence of the spike on subsequent logic by following the spike state.

The spike state is a special signal state added to the ordinary twelve states covered by simulators. The 12 states are typically made up of a combination of three logic levels (high, low, and unknown) and four strengths (supply voltage, driving, resistive, and high impedance). Some simulation vendors add to these 12 states in order to cover spike states and add other improvements.

Debug tools that give you speed are important, but so are features that let you incorporate your changes and resimulate quickly. A simulator that is well integrated with a particular schematic-capture software package allows you to change the schematic representation and immediately resimulate with the changes in the design. You also save time if, after making changes, you don't have to recompile the entire simulation before running it. Aldec's Susie series has an incremental compiler that allows you to recompile only the portion of the design affected by the change.

Silos II has a feature that lets you save and restart the simulation from any point in time. If you need to make multiple simulation runs from one point, you need not spend the time going through simulations from the beginning; you can start at the point where you are altering the simulation.

Trust your own benchmark

You should run your own benchmark to find out how fast these products actually simulate, rather than depend on events per second or other numbers from simulation vendors. The events per second quoted by simulation vendors are not all equivalent. Furthermore, some vendors quote simulation speed by stating a design with X gates and Y stimulus vectors will run in a given amount of time, but that speed depends on how the gates are connected and how the simulation vectors exercise the design. If you run your own simulation benchmarks on simulation soft-

Should you simulate on a PC or a workstation?

Designers sometimes want to know how simulation on personal computers compares with simulation on workstations and mainframes. First, you should note that two of the companies with PC-based simulation (SimuCAD and Viewlogic) also offer simulation products for workstations and mainframes. The software is essentially unchanged, regardless of the computer.

High-end PCs, such as 386- and 486-based computers and Apple Macintosh IIs, are approaching low-end workstation performance. Provided the systems have equivalent amounts of memory, you should get logic-simulation performance close to a low-end workstation.

If you're performing a timing simulation on a 50,000+ gate circuit, you'll probably find a PC-based simulator slow, even if the circuit fits. However, you shouldn't let that discourage you from using a PC-based simulator on smaller designs.

EDN February 4, 1991
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TECHNOLOGY UPDATE

PC-based logic simulators

ware you are considering, you'll have meaningful results and you'll know more about what the simulator can do.

Simulation speed issues and the debug process should be considered together for the overall efficiency of a simulator. A measure of the simulator's speed, however, is not necessarily how fast the simulation runs after you've compiled the code and started the simulation. What you really need to know is how long it will take to simulate, find problems, correct them, and verify that the simulated design works properly.

The best measure for determining whether a particular logic simulator will work in your application is to try some circuit examples that gave you trouble in the past. If the simulator can find problems that you didn't discover until you had hardware, then the simulator shows promise of saving you time and money.

Some of the problems designers typically have to look for are setup and hold-time violations and clock setup violations, such as the end of a reset pulse to the beginning of a clock cycle on a flip-flop. You might also be trying to detect glitches on components and their effects.

Depending on the type of design work you do, you will have special demands for a simulator. For example, in IC design you need different timing for each instance of a gate. You also need to transfer routing delays back to the simulator after physical layout to verify that the timing still works.

Most PC-based simulation software vendors have free or nominal-cost demo software that you can obtain to try out simulation. The packages have limitations either in design size or other features, but they will give you a start in evaluating the products for your applications.

EDN

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High 515 Medium 516 Low 517

For more information...

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Meet NCR's SCSI development team. In 1983, they gave the computer industry its first SCSI device. By providing easy connectability and significantly reducing time to market, a new product era was born. Since then needs have changed. By combining our system skills, high-performance standard cell methodology, and in-house manufacturing, NCR has maintained its leadership role with innovative new ideas like the 53C700 product family. And the joint development of LADDR — a new architecture aimed at cutting the development time of OS/2 device drivers by 90%. Today SCSI is becoming the leading I/O standard — adopted by industry giants like Apple, IBM, HP, and DEC. And no one is selling more SCSI chip level products than NCR. In fact, no one even comes close.

Part of the NCR SCSI Development Team: (left to right) Jerry Armstrong, Sr. Software Engineer; Harry Mason, Strategic Marketing Manager; John Lohmeyer, NCR Sr. Consulting Engineer and Chairman of the ANSI X3T9.2 Committee and Dave Skinner, SCSI Product Manager.
Here's another.

The NCR 53C700 SCSI I/O Processor…
So good, Electronic Design named it the product of the year.

"You can't tell a good SCSI chip just by looking at it…" and according to Electronic Design, NCR's 53C700 is the best there is.

The only third generation SCSI device on the market today, it concentrates all the functions of an intelligent SCSI adapter board on a single, smart and extremely fast, chip… for about 15% of the cost.

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Those are just a few of the reasons Electronic Design's "Best of the Digital IC's" award went to NCR's 53C700 last year.

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EDN February 4, 1991
TECHNOLOGY UPDATE

TIMING-DIAGRAM DESIGN TOOLS

Front-end tools reduce schematic drudgery

Digital logic designers constantly live on the edge. They are on the edge of a critical waveform until they know it will satisfy complex timing requirements; on the leading edge of technology if their design works correctly; on the trailing edge of disaster if they miscalculate by a few crucial nanoseconds and the product has to be recalled. Engineers spend many hours (as much as 75% of the design phase) drawing timing diagrams, analyzing the circuits these diagrams represent, and calculating the potential effect of component changes at point A on timing tolerances at point B many gates downstream.

You may draw a skeletal schematic while you're working out the timing, but until you know the mutual dependencies of the waveforms, you're in no position to specify the component and IC part numbers that a schematic-capture tool will demand of you. So you take your colored pencils and you draw... and you draw... and you redraw... until the schematic comes out right. It's a repetitious, tedious, and frustrating task. If you make a nasty mess with the eraser, the documentation people may displace a signal edge by a significant amount. If you're tempted not to follow a dependency all the way through the many sheets of the diagram, the components' manufacturing tolerances may combine to make your design unreliable. Creating the final timing diagram is dogwork that often makes you wonder why you ever wanted to be an engineer.

In these days of computer-aided this and computer-aided that, why can't the computer do the dogwork? After all, that's what computers are for, isn't it?

The trouble is that CAE tool designers have so far been busy with the back end of the design. Many board-design tools include a timing simulator that will analyze your captured schematic and use the device characteristics of the automatically placed components to run checks against your design rules. For high-speed boards, some simulators will analyze the schematic and the layout to check for undesirable transmission-line effects.

However, these simulators all require
Many said it was impossible. Create a truly programmable filter that lets you skip over do-it-yourself passive-filter design and do away with many external components.

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Whether you’re designing hard disk drives, LANs, cellular telephone systems, radar systems or whatever, your next mission is to contact your nearest Silicon Systems representative or distributor. Or call us for literature package SPD-4.

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Timing-diagram design tools

that the schematic-capture, layout, and routing phases be complete. They can only verify your work on the waveform diagrams—they’re not a substitute for that original work. They will flag timing violations—but then what? You have to go back to the start, either changing device types or modifying the schematic to correct the error. Then you run the simulation over again and hope that your changes have not caused more or different timing violations. These computerized iterations can take as much time and cause as much frustration as manual methods. You may find yourself drawing and redrawing timing diagrams by hand before you draw the schematic just so the simulator will give your design a clean bill of health the first time around.

Cavalry to the rescue

Two companies have turned their attention to the front end of the design phase and offer timing-diagram design tools that will help you solve your timing problems (with paper and pencils). Chronology Corp’s Timingdesigner costs $1495 and runs on IBM PC/ATs and compatibles under Microsoft Windows 3.0. Doctor Design Inc’s dV/dt Plus also runs on IBM PC/ATs and compatibles—with at least 1M byte of extended memory and DOS version 3.0 or higher—and costs $795. Doctor Design also offers a Macintosh version of dV/dt for $695.

Doctor Design Inc has—perhaps too boldly—trademarked a commonly used expression, “dV/dt,” so you can expect another spate of physicist/mathematician jokes at the expense of engineers. Engineers have always been stuck at the bottom of the academic totem pole. Witness the mathematician’s definition: “An engineer’s a guy who uses a slide rule to multiply 2 by 2, gets the answer to 3.95, and then decides to approximate and call it 4.”

And a physicist was recently overheard saying about dV/dt: “It’s a real nifty program, but if that’s the best they can do for a name, maybe they should have stuck to designing doctors.”

Dismissing quibbles about naming, both of these programs are valuable tools that can save you hours of drudgery. Indeed, they constitute an innovative breakthrough in a CAE world, which for several years has been refining known techniques rather than developing anything really new.

The programs offer similar facilities. You can enter duty-cycle, duration, phase, and jitter parameters for the clock. The clock generator then automatically generates clock signals throughout the diagram. You can also enter IC constraints such as setup, hold, or minimum pulse width, and the built-in ana-

For more information ...

For more information on the timing-diagram editors discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN’s Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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(206) 869-4227
FAX (206) 869-4229
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  - Internal Protection Features

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  - 500 mW Power Rating
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**UPDATE**

Timing-diagram design tools

lyzer will highlight any violation of these constraints. You can display signal edges with minimum/maximum uncertainty, computed either on the basis of the known characteristics of standard library parts, or on the basis of variables such as temperature or voltage.

Both programs let you save, retrieve, and print timing-diagram files, so now you can provide accurate diagrams in a form suitable for incorporating into your design documentation. You won't have to risk the potential errors of redrawing rough sketches. The Macintosh version of dV/dt can output the diagrams to any "chooser-selectable" Mac printers, and dV/dt Plus works with all Epson MX series and HP LaserJet series printers. Timingdesigner will work with hundreds of printer, plotters, graphics cards, and monitors through Windows' device drivers.

If you're a Macintosh user, dV/dt is currently your only choice. If you're a PC/AT user running Windows 3.0, Timingdesigner will probably give you the best performance. But if you don't run Windows 3.0, then dV/dt Plus in the DOS environment will still let you jettison those pencils, scrap sheets, and napkins.

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**READ ON IN EDN**

To find out why more and more engineers are eschewing 5%- and 8-in. drives in favor of 3½-in. units, turn to this issue's Special Report.
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A true leader

The UNIX based DECstation™ 5000 Workstation
Example #1: Performance
No matter how you measure it, Digital’s DECstation 5000 workstation leads all others in performance. Whether it’s raw CPU performance, 2D or 3D graphics speed, or price/performance, the DECstation 5000 workstation comes out ahead. In fact, for overall performance, nothing else is close. And we’ve got the numbers to prove it.

<table>
<thead>
<tr>
<th>PERFORMANCE COMPARISON CHART (1)</th>
<th>SUN SPARCstation 1+</th>
<th>IBM 320/520</th>
<th>DECstation 5000 cx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Graphics &amp; Windowing (2)</td>
<td>0.24</td>
<td>0.71</td>
<td>1.59</td>
</tr>
<tr>
<td>Integer</td>
<td>1.04 (3)</td>
<td>1.34</td>
<td>1.61</td>
</tr>
<tr>
<td>Floating Point</td>
<td>1.10 (3)</td>
<td>2.6</td>
<td>1.7</td>
</tr>
<tr>
<td>Overall Performance</td>
<td>0.65</td>
<td>1.35</td>
<td>1.63</td>
</tr>
</tbody>
</table>

(1) All data normalized to DECstation 3100. Comparable configurations tested. Geometric mean used to combine results. Performance will vary depending on applications and environment. (2) Graphics and windowing data measured using X11perf benchmark. CPU Integer and Floating Point performance measured from running SPEC V1.0 workload. (3) SPEC performance estimate based on SUN 4/330 results published by Sun Microsystems, Inc.

Example #2: UNIX based Applications
When you run with the leader, you know you’re in good company. The DECstation 5000 workstation runs more than 1,500 UNIX based applications, including the industry’s most popular MCAD and EDA applications.

Example #3: PowerFrame™ for Design Integration.
With Digital’s PowerFrame design framework, you can easily integrate the DECstation 5000 workstation with your existing UNIX based EDA and MCAD systems. PowerFrame is the most widely used framework for heterogeneous design management.

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For your copy of benchmark test results and a list of available applications, call 1-800-343-4040, ext. 970. These are filled with examples of what you expect from a leader.
Specs for Hard Drivers.

Maxtor 7080

Simplicity of design makes Maxtor's Cheyenne Series inch-high 80MB 7080 disk drive the most reliable in its class. Compare Maxtor's four-head, two-platter design to Seagate's six-head, three-platter design. Fewer moving parts make Maxtor's drives inherently more dependable.

Power consumption is a very low 2.8 watts, making it one of the lowest in the 80MB class. The 7080 is also Novell Labs certified, and is available with either SCSI or AT interface, giving you flexibility for a winning system.

Exceptionally fast 17ms seek time and 32K cache buffer in the new generation inch-high form factor give Maxtor faster data throughput than the competition.

Call and ask about our entire Cheyenne family of disk drives with capacities from 40MB to 130MB. Don't fall for the off-the-wall claims. Give us a shot and we'll prove Maxtor specs can't be matched. Call your nearest Authorized Maxtor Distributor.

<table>
<thead>
<tr>
<th>3.5-inch Disk Drive Spec.</th>
<th>Maxtor 7080A</th>
<th>Seagate 1102A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Seek Time</td>
<td>17 Msec.</td>
<td>19 Msec.</td>
</tr>
<tr>
<td>Standard Buffer Size</td>
<td>32K</td>
<td>8K</td>
</tr>
<tr>
<td>Form Factor</td>
<td>3.5&quot; x 1&quot;</td>
<td>3.5&quot; x 1.6&quot;</td>
</tr>
<tr>
<td>Heads-Disks</td>
<td>4/2</td>
<td>6/3</td>
</tr>
<tr>
<td>Avg. Power Consumption</td>
<td>2.8 watts</td>
<td>9 watts</td>
</tr>
</tbody>
</table>
Inexpensive 32-bit µP chip seeks embedded systems

While giant semiconductor companies are making 32-bit µP design look so formidable that few start-up companies even dream of developing competitive 32-bit designs, a small German company is ready to do battle. The battleground is the crowded embedded-computer market, where 10-person Hyperstone Electronics is determined to gain a beachhead in its campaign for embedded-system customers. Named the Hyperstone E1, the 85,000-transistor chip operates at a burst rate of 25 MIPS at 25 MHz. The µP requires no external cache, and it operates with external dynamic RAM (DRAM) chips, which it controls directly.

The E1 chip offers an address space of 4G bytes, and it has separate memory and I/O addresses. The chip supplies 19 global and 64 local registers, each of which has 32 bits. Programs can directly address as many as 16 global and 16 local registers. You can also reconfigure the registers in a variable-length stack, using from 2 to 16 frames. Most of the chip's instructions are 16 bits long, although complex instructions can consume as many as 48 bits. Benchmarks yield 38,000 Dhrystones. The throughput results from a combination of pipelined load instructions, an internal 2-stage decode/execute pipeline, and a look-ahead instruction cache.

This chip is not the quixotic dream of an eccentric engineer. Hyperstone's founder and leader is Otto Müller, a computer engineer who is known in Europe for designing computers for Telefunken, Nixdorf, and Triumph-Adler. After designing computers for these large companies, Müller founded his own company, CTM, which produced computers for businesses. Müller's new company, Hyperstone, is 2½ years old and is already producing µP chips.

Although the company does not fabricate its own devices, it has a foundry in the USA that furnishes them. It has also licensed nonexclusive rights to the chip to Zilog, which currently has working silicon and expects to offer chips in March. Zilog will also offer the chip as a core in its Superintegration ASIC program.

You can purchase the E1 µP chip directly from Hyperstone for $150. However, the company expects the price to drop to less than $50 (10,000) by the end of 1991. A development board, which provides an E1 CPU, 1M byte of DRAM, 256k bytes of EPROM, and an RS-232C I/O port, is available for $1699. An assembler and a debugger cost $350 and $400, respectively. They run on an IBM PC or a compatible computer. You can load instructions and data into the development board through the computer's serial I/O port.

—Jon Titus

Hyperstone Electronics, GmbH, Robert-Bosch-Strasse 11, D-7750 Konstanz, Germany. Phone 07531-67789. FAX 07531-51725.

Circle No. 730

Zilog Inc, 210 Hacienda Ave, Campbell, CA 95008. Phone (408) 370-8000. FAX (408) 370-8056.

Circle No. 731
PRODUCT UPDATE

Driver IC distributes 20 clock copies and offers a primary output of 80 MHz max

You can use the SC3501 BiCMOS 20-copy clock-driver IC to handle clock distribution throughout an entire high-speed-CPU board. The IC outputs TTL-compatible signals with frequencies as fast as 80 MHz. Less than 500 psec of skew characterizes the 20 leading-edge synchronized outputs.

As input, the clock-driver IC requires a signal of double the desired output frequency. A differential ECL input signal from a crystal-controlled oscillator, operating between 5V and ground, provides a high-precision output signal. Optionally, you can drive the IC with TTL signals for low-frequency applications.

The SC3501 IC offers three groups of outputs. The first set of 10 outputs operate at the primary clock frequency of the chip (one-half the input frequency). You can set the second group of five outputs to be identical to the primary output frequency or to operate at one-half the primary output frequency. Likewise, you can set the third group of five outputs to a choice of one-half or one-fourth of the primary output frequency.

All 20 outputs provide waveforms with 50% high/low duty-factor symmetry centered around a threshold of 1.5V. You can adjust the clock-width timing symmetry in ±0.34-nsec increments via strappable input pins.

The outputs include complementary 24-mA-pk source and sink drivers. The outputs also feature internal source termination that minimizes signal overshoot or undershoot without requiring external termination networks. A maximum output slew rate of 2V/nsec minimizes simultaneous output switching noise and distortion. You can also connect the outputs in parallel to drive capacitance loads of 40 pF and higher.

The SC3501, in a 52-pin quad flatpack, costs $17 (1000).
—Maury Wright
Silicon Connections Corp, 6160 Lusk Blvd, Suite C-204, San Diego, CA 92121. Phone (619) 535-0442. FAX (619) 535-1635.

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EDN February 4, 1991
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WHAT GOOD IS A BRAIN
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To hear most people in the computer business talk, you’d think the only valuable part of a system is its microprocessor. Maybe they haven’t lost their minds. But they’ve certainly forgotten about the hard drive. And the critical data it stores. Data which can’t be easily replaced like a microprocessor.

So it’s no surprise that many OEMs are reducing their risk of system failure with disk drives from Conner. Using proven technologies, our high performance drives consistently set the standards for form factor, reliability, and innovation.

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All of which makes choosing Conner disk drives a low risk decision.

So call Conner today. The results should be quite memorable.

CONNER
THE THIRD WAVE
Diminutive disk drives cram more and more data onto standard-size 3½-in. media. (Photo courtesy Quantum Corp)
HIGH-CAPACITY

3½-IN.

HARD-DISK

DRIVES

New 3½-in. hard-disk drives have capacities exceeding 500M bytes and perform as well as high-end 5¼-in. units. The small drives are as reliable as 5¼- and even 8-in. drives and can be found in workstations, file servers, and drive arrays.

Maury Wright, Regional Editor

Most hard-disk-drive trends stay the same: higher capacities, smaller units, faster performance, and cheaper prices. This year is no exception. The latest round of 3½-in. drives includes units that have capacities exceeding 500M bytes. You can now buy 100M-byte 3½-in. drives that stand only 0.75-in. high. Some manufacturers offer drives whose spindle motor speeds exceed 3600 rpm. These drives have low rotational-latency specs and fast read-channel data rates. And many 3½-in. drives are now cheaper than comparable 5¼-in. drives and have MTBF specs as high as 200,000 hours.

In fact, the widespread availability and competitive pricing of 3½-in. disk drives has completely eroded demand for 5¼-in. units with capacities of 200M bytes and less. A year to 18 months ago, you paid a premium for a 3½-in. unit—even in a low capacity such as 30M bytes. Now you can buy 3½-in. units for less than what you’d pay for 5¼-in. drives at capacities of 200M bytes and less—with the exception of sporadic fire sales by manufacturers of 5¼-in. inventory. The discounted street prices of 100M-byte 3½-in. drives have reached $450, and some of the newer drives should drive that price lower within the next quarter.

The newly announced 400M- and 500M-byte 3½-in. drives will soon become the primary choice of designers of workstations and network file servers—applications currently dominated by 5¼-in. drives. The size of the smaller drives also suits them for arrays.

So chances are you’ll be looking at 3½-in. disk drives this year unless your upcoming designs require fea-

A cache that adapts to ongoing operations optimizes the performance of Western Digital’s WDSP4200 200M-byte 3½-in. drive. The on-drive controller chooses the cache algorithm number of segments and the segment size.
The emergence of 500M-byte 3½-in. drives will erode demand for 5¼-in. drives, especially for workstations and LAN servers.

tures that other form factors can better provide. For example, laptop and notebook designs will most likely take advantage of the smaller size of 2½-in. drives. (For more information on advances in 2½-in. drives see box, “Capacities of 2½-in. drives approach 100M bytes”).

And a few reasons do remain to consider 5¼-in. drives. You can buy the larger drives in higher capacities—currently as high as 1.6M bytes. Some 5¼-in. drives offer features previously associated only with 8-in. drives. One such feature is split data channels, which doubles the raw data rate a drive can sustain. You can also buy 5¼-in. drives with a greater choice of interfaces, notably ESDI and IPI-2 (Intelligent Peripheral Interface), both of which are device-level interfaces. Drives with this type of interface require a host-resident controller board.

The new generation of 3½-in. drives seemingly marks the end of device-level interfaces in disk drives. All the recently announced drives feature either SCSI or IDE (Integrated Device Electronics—also called the AT interface) intelligent interfaces. Drives with intelligent interfaces have embedded controllers, which make technological advances such as multiple-zone recording and on-drive caches and error handling possible. Advances in disk-control and -interface ICs have made the overhead previously associated with intelligent interfaces virtually negligible.

**Few drives support ESDI**

You must consider drive interface as a key system-design issue. Only a few companies offer device-level interfaces on 3½-in. drives. Some older units have ST-506 device-level interfaces. Microscience International ships 110M- and 123M-byte members of its 5100 family of drives with ESDI interfaces. NCL America Computer Products also offers 3½-in. drives with ESDI interfaces.

Dave Tovey, Toshiba’s marketing vice president, says array designers will demand 3½-in. drives with some type of device-level interface. Tovey thinks a simplified version of the ESDI interface—possibly with

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**Capacities of 2¹/₂-in. drives approach 100M bytes**

You can now buy 60M-byte 2½-in. disk drives from several sources, and 80M- and 100M-byte units will soon follow. The drives suit traditional applications such as portable, laptop, and notebook computers. But expect the tiny drives to also find use in applications such as fax machines, laser printers, and even automobiles.

Prairietek leads the 2½-in.-drive field. The company offers the PT-120 20M-byte drives for $432 (100) and the PT-240 40M-byte drives for $534 (100). The drives employ one and two platters, respectively. Along with Prairietek, Conner Peripherals and JVC have supplied most of the 2½-in. drives shipped to date. Most of these units have been 20M-byte drives.

Several other companies have recently announced 2½-in. drives, and more will soon follow. The 40M-byte drives are now main-
no signal drivers because the cable runs would be short—might suit such applications. Neither Toshiba nor any other company currently offers a 3½-in. drive with such an interface, however, and no standard for such an interface exists. Most of the new IDE and SCSI drives do have some features, such as spindle synchronization, that support array designs.

The IDE and SCSI offerings should suit your needs for traditional system designs. Intelligent drives typically add less than one millisecond of overhead to I/O operations. The IDE units work only in IBM PC/AT bus systems and offer plug-and-play compatibility with the original IBM PC/AT ST-506 disk controller. In fact, newer IBM PC/AT-compatible mother-board chip sets from companies such as Chips and Technologies (San Jose, CA) and VLSI Technology (Tempe, AZ) regularly include the simple IDE host interface. A single header connector on the motherboard provides the primary I/O capability. IBM has developed a similar interface for its Micro Channel-based systems and, along with Conner Peripherals, manufactures compatible disk drives.

SCSI drives require nonstandard operating-system drivers or BIOS additions for use on IBM-compatible personal computers. The drives offer performance advantages for multitasking operating systems such as Unix or Novell's NetWare that overlap I/O requests. SCSI drives are compatible with many other peripherals. You can use a single SCSI host adapter to connect tape drives, CD-ROM drives, scanners, and printers, as well as disk drives. Outside the world of IBM-compatible personal computers, the computer industry has endorsed SCSI as the interface of choice for most systems with less-than-mainframe power.

These high-capacity drives all support the SCSI-2 standard. Less than a year old, SCSI-2 formally defines a common command set for disk drives and other peripherals. The standard adds error-recovery features and command tags that facilitate command queuing. SCSI-2 also defines optional wide and fast data transfers. The wide transfer option defines the expansion of the interface from an 8-bit to a 16- or 32-bit bus. The fast option doubles the bus speed during synchronous transfers to 10 MHz, which results in a 10M-byte/sec rate on an 8-bit implementation.

The SCSI-2 drives available now don't support the optional wide or fast data transfers. Virtually all manufacturers of high-capacity 3½-in. drives plan to support

stream products, and higher-capacity drives are now emerging. Toshiba, for example, entered the market with the 40M-byte MK-1122FC drive that weighs 6.3 oz. The single-platter drive costs $425 (100), includes a 32k-byte cache, and has an average seek time of 23 msec. The company also offers a 20M-byte version of the product. Quantum announced a single-platter 40M-byte drive, and Seagate offers a single-platter 20M-byte unit and a dual-platter 40M-byte drive.

Areal Technology, Conner Peripherals, and Western Digital have announced 60M-byte products. Western Digital's $325 (100) 30M-byte WDAB130 and $495 (100) 60M-byte WDAH260 drives include one and two platters, respectively. When combined with the company's 7600 Core Logic family of mother-board chip sets, the drives offer eight power-saving modes for battery-powered notebook computer operation. The combination also yields zero-wait-state memory access between the host CPU and the IDE controller. Typically, systems with IDE drives insert one or two wait states when accessing the controller.

Conner Peripherals includes 30M, 40M, and 60M-byte drives in its Pancho series of drives. The drives' prices range from $395 to $495. The CP-2064 60M-byte product employs two platters and features a 19-msec average seek time. The drive requires 1.3W and can withstand shocks of 100g.

Areal Technology's MD-2060 uses a single platter to store 60M bytes. The drives use glass-substrate media—a holdover from Areal's previous attempts to enter the 3½-in. drive market with a 1-in.-high 100M-byte drive. Areal now has a manufacturing agreement with Sanyo (Tottori City, Japan), and Sanyo holds an equity position in Areal. Evaluation units of the drive cost $995, and Kirby says production units will be available in the first quarter.

Around midyear, expect to see 80M-byte 2½-in. drives. Prairietek has announced plans to build a 2-platter 80M-byte unit. Conner Peripherals offers a 0.75-in.-high, 85M-byte 3½-in. drive. If Areal succeeds in producing its 60M-byte unit on schedule, you may also see a 120M-byte, 2-platter offering from the company in the second half of the year. Finally, expect Maxtor to enter the market during the first half of the year with a drive designed at its Colorado division (formerly Miniscribe). Given Maxtor's reputation, expect the drive's capacity to exceed that of currently announced products.
New 3½-in. drives eschew device-level interfaces such as ESDI completely and instead offer the choice of SCSI or IDE interfaces. Fast transfers, at least as an option. Vendors of disk-controller ICs are busy adding the capability, so expect widespread availability of drives with the feature after midyear. The wide SCSI-2 data-transfer option should be more popular on 5½- and 8-in. drives.

Choosing a disk-drive supplier will prove to be a much less exact science than choosing an interface. In the 400M- to 500M-byte product category, the list of suppliers reads like a who's who of the disk-drive industry. (See Table 1 for suppliers and drive specifications.) Hewlett-Packard, Hitachi, IBM, NEC, Quantum, Seagate, and Western Digital all offer 3½-in. drives with capacities exceeding 400M bytes. IBM and Western Digital sell the same drive. IBM designed and builds the drive and handles sales to large customers. Western Digital sells the drives to smaller OEMs and through distribution.

Conner Peripherals, Fujitsu, Maxtor, and Rodime all offer drives with capacities exceeding 500M bytes. The companies offer depopulated versions of the drives (versions with one or more disk platters removed) that have capacities of 200M to 400M bytes. The 400M- and 500M-byte drives all have similar performance specs, but you should evaluate the actual performance of the drives in your application. Be aware that manufacturers measure performance in different ways, so comparing specified seek times or data rates is not necessarily like comparing apples and apples.

**Fast spindle speed reduces latency**

The Fujitsu M262XSA/T and Seagate ST1480 drives deserve note in the performance area. The drives feature a state-of-the-art average seek time of 12 msec. They have rotational speeds of 4400 rpm; most other drives have rotational speeds of 3600 rpm. The faster spin rate results in an average rotational latency spec (the time required for the platters to rotate half a turn) of 6.8 msec, compared with 8.3 msec for most competing products. The faster rotation also results in a faster raw data rate—approximately 3M bytes/sec.

**Table 1—Representative high-capacity 3½-in hard-disk drives**

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Model</th>
<th>Formatted capacity (M bytes)</th>
<th>Price</th>
<th>Number of disks</th>
<th>Track density (rpi)</th>
<th>Bit density (bpi)</th>
<th>Data encoding scheme</th>
<th>Spindle speed (rpm)</th>
<th>Average seek time (msec)</th>
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</thead>
<tbody>
<tr>
<td>Conner Peripherals Inc</td>
<td>CP-3200</td>
<td>212</td>
<td>$660</td>
<td>4</td>
<td>1700</td>
<td>31,800</td>
<td>2,7RLL</td>
<td>3485</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td>CP-3500</td>
<td>510</td>
<td>$1295</td>
<td>6</td>
<td>2100</td>
<td>42,763</td>
<td>2,7RLL</td>
<td>3609</td>
<td>12</td>
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<td></td>
<td>CP-4200</td>
<td>422</td>
<td>$1225</td>
<td>5</td>
<td>1850</td>
<td>44,383</td>
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<td>3600</td>
<td>13</td>
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<tr>
<td></td>
<td>CP-510</td>
<td>520</td>
<td>$1570</td>
<td>5</td>
<td>1650</td>
<td>44,100</td>
<td>2,7RLL</td>
<td>3600</td>
<td>13</td>
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<tr>
<td></td>
<td>CP-600</td>
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<td>$1890</td>
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<td>1450</td>
<td>45,000</td>
<td>2,7RLL</td>
<td>3600</td>
<td>13</td>
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<tr>
<td>Fujitsu America Inc</td>
<td>M262XSA/T</td>
<td>520, 425, 330</td>
<td>$1750, $1500, $1250</td>
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<tr>
<td>Hewlett-Packard Co</td>
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<td>419</td>
<td>$1780 (100)</td>
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<td>320</td>
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<td>1,7RLL</td>
<td>4316</td>
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<td></td>
<td>*0661-467</td>
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<td></td>
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<td>213</td>
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<td></td>
<td>LXT535, 437</td>
<td>535, 437</td>
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<td>38,427</td>
<td>1,7RLL</td>
<td>4316</td>
<td>11.5</td>
</tr>
</tbody>
</table>

Key: N/A = Not applicable. N/S = Not specified. *IBM and Western Digital both sell these drives; IBM sells them only in large OEM quantities.
The features of intelligent controllers can sometimes improve the performance of disk drives beyond the capabilities of the drive hardware. Quantum has offered a multisegment cache on its drives for years. Its newest Prodrive 330 and 425 products include a 256k-byte cache. The controller continues to read sequential data after an I/O request completes. The drive can service subsequent requests with no seek time or rotational latency (typically close to 20 msec) on cache hits.

Drives with this cache implementation can continue to prefetch data and service incoming I/O requests simultaneously with no extra command overhead. Thus, a new I/O request never interrupts a prefetch operation that might be retrieving the requested data. On cache hits, the controller can continue a prefetch operation and transfer the requested data from the cache at the same time.

**Stigma remains on write caches**

You can also specify a write cache as an option on Quantum's drives. Product Marketing Manager John Klonick says that 50% of all I/O requests write data; a cache speeds such operations by holding data tempo-

<table>
<thead>
<tr>
<th>Track-to-track seek time (msec)</th>
<th>Disk data rate (M bits/sec)</th>
<th>Recording zones</th>
<th>MTBF (hours)</th>
<th>Cache size (k bytes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>12</td>
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<td>50,000</td>
<td>64</td>
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<tr>
<td>4</td>
<td>16</td>
<td>N/A</td>
<td>100,000</td>
<td>256</td>
</tr>
<tr>
<td>3</td>
<td>19 to 24</td>
<td>4</td>
<td>200,000</td>
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<td>141 to 20.6</td>
<td>3</td>
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<td>64</td>
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<tr>
<td>7</td>
<td>14</td>
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<td>150,000</td>
<td>64</td>
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<tr>
<td>7</td>
<td>16</td>
<td>N/A</td>
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<tr>
<td>5</td>
<td>12</td>
<td>N/A</td>
<td>45,000</td>
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</tr>
<tr>
<td>4</td>
<td>16</td>
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<td>150,000</td>
<td>64</td>
</tr>
<tr>
<td>3</td>
<td>16</td>
<td>N/A</td>
<td>150,000</td>
<td>128</td>
</tr>
<tr>
<td>3</td>
<td>9 to 15.7</td>
<td>6</td>
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</tr>
<tr>
<td>3</td>
<td>133 to 20.5</td>
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<td>128</td>
</tr>
<tr>
<td>3</td>
<td>133 to 20.5</td>
<td>8</td>
<td>150,000</td>
<td>128</td>
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<tr>
<td>4</td>
<td>12.5</td>
<td>N/A</td>
<td>60,000</td>
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<td>64</td>
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<td>32</td>
</tr>
<tr>
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<td>10.8 to 16.3</td>
<td>8</td>
<td>50,000</td>
<td>64</td>
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<tr>
<td>4</td>
<td>12.2 to 21.7</td>
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<td>150,000</td>
<td>256</td>
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<td>136 to 21.6</td>
<td>8</td>
<td>100,000</td>
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<tr>
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<td>10</td>
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<td>150,000</td>
<td>64</td>
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<tr>
<td>2.5</td>
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<td>16</td>
<td>N/A</td>
<td>150,000</td>
<td>64</td>
</tr>
<tr>
<td>3</td>
<td>16</td>
<td>N/A</td>
<td>150,000</td>
<td>128</td>
</tr>
</tbody>
</table>

The 4400-rpm spindle speed of Seagate's ST1400 family of drives results in an average rotational latency of 6.8 msec and disk data-transfer rates as fast as 3M bytes/sec.

Traditionally, system designers resist write caches because a system or power failure could result in lost data. Klonick points out that the typical Unix system has 8M bytes of data in main memory that disappear when failures occur, but only a few kilobytes are lost on the drive.

Other companies have become serious about caching as well. For 400M- and 500M-byte 3½-in. drives, a 256k-byte cache is the rule rather than the exception. Conner Peripherals includes a 4-segment, 256k-byte cache on its CP-3500 drive. Previously, the company offered a simple 1-segment read-ahead buffer.

Quantum offers a controller feature called read on arrival. The drives can attempt to read data immediately upon arriving at the desired track without waiting for the heads to settle for a specified period. When the read is successful, the drive sometimes eliminates the latency caused by a full rotation of the disk. Of course, the technique can increase seek errors, so you can disable the feature with software.

In addition to performance, consider reliability and cost when choosing a 3½-in. drive. Manufacturers of disk drives have raised the MTBF spec of their products across the board in the last year. Hewlett-Packard started the trend by specifying an MTBF of 150,000 hours and a warranty of five years on all its drives. Fujitsu followed with a 200,000-hour spec on its products. Both companies have also published papers detailing the derivation of their published MTBF specs.

Other manufacturers have been less forthcoming with detailed information on drive MTBF specs. Manufacturers should explain the theoretical basis for a MTBF spec. Accelerated life testing should back up the theory. And field data along with ongoing life testing should further substantiate the spec.
Consider overall drive design, also, as an indicator of how producible and reliable a drive might be. A drive’s design can also subtly indicate how reliable the company’s next-generation product might be. Most manufacturers have specific technological strongholds that influence their drive design and how they achieve high disk-drive capacities. You can always increase a drive’s capacity yourself by adding platters or increasing the bit or track density. Multiple-zone recording can boost a drive’s capacity by as much as 50% and is virtually free once designed in. Also called zone-bit recording (a Seagate trademark), multiple-zone recording requires that the drive surface be divided into concentric zones. The outer tracks have more sectors than inner tracks and store more data than the inner tracks store.

Try to judge which drive-design parameters a manufacturer drives to the edge to achieve high capacities. Maxtor, for example, uses six platters, 1,7 RLL data encoding, and 8-zone multiple-zone recording to achieve the 535M-byte capacity of its LXT-535 drive. Conner Peripherals chose not to use multiple-zone recording in its 510M-byte CP-3500. The company achieved the capacity of that drive by pushing the track density to 2100 tpi; Maxtor’s product has a track density of 1600 tpi.

**RLL boosts capacity and tightens margins**

Michael Gluck, senior vice president of Fujitsu’s Computer Products Group, warns that you should watch out for the data-encoding scheme drive manufacturers use. Gluck points out that 2,7 RLL data encoding offers a 50% capacity boost compared with MFM encoding; 1,7 RLL offers a 33% relative increase. Gluck says 2,7 encoding results in tighter read-channel window margins and a potentially less-reliable drive. Fujitsu’s M262XSA/T uses 1,7 RLL coding, six platters, and 4-zone multiple-zone recording. In practice, manufacturers have proven that 2,7 RLL encoding will work reliably. However, soft read errors that don’t show up as drive failures cause retries and hurt drive performance.

Hewlett-Packard, NEC, Quantum, and Seagate have not announced 6-platter drives yet and, therefore, have no 500M byte products. However, you can expect such products in the future. IBM and Hitachi use more than six platters in their 400M-byte products. IBM’s Model 467 has eight platters, and Hitachi’s DK314 has seven.

IBM and Hitachi chose to face stiffer packaging requirements and the associated head spacing and aerodynamic problems rather than push bit or track density to achieve high-capacity drives. Neither company currently employs multiple-zone recording. Thus, they have the potential to double the present capacities of their drives without adding more disks. For now, more heads and disks translate into higher cost.

Choosing a drive with a capacity of 100M- to 200M bytes typically requires more attention to cost than to any other detail. Conner Peripherals’ CP-3100 family of drives has been among the most popular 100M-byte drives, and mail-order houses sell the product for less than $500. Several Seagate drives in the 100M-byte range have suggested list prices of approximately $500. Kalok just introduced the KL3100 100M-byte 3½-in. drive. You can expect discounted street prices to near $400 after midyear.

**Synchronous 10M-byte/sec SCSI-2 data transfers suit the 540M-byte Rodime 3004T drives for use in workstations and file servers. The drives also feature spindle synchronization for array applications.**

You also have various sizes of 3½-in. drives to choose from in the 100M-byte range. Most of the drives are 1.625 in. high—the standard full height for a 3½-in. product—but over the last two years, several manufacturers have introduced 1-in.-high drives.

Conner Peripherals, Fujitsu, Maxtor, Quantum, Rodime, Seagate, Teac, Toshiba, and Western Digital have introduced 1-in.-high 3½-in. drives that store more than 100M bytes. You will find differentiating the drives’ performance specs tough, so be sure to test the drives in your system if performance is a prime concern. Other key parameters include power consumption, noise level, and environmental specs.

The 1-in.-high drives assume many of the features present in full-height drives from the same manufacturers. MTBF averages 100,000 hours, and the products include caches—albeit smaller ones than the full-height
NAT4882
The Only Way to Reach Full 488.2 Compatibility

- Industry Standard
- 7210/9914 Compatible

PC AT #31

- The New Industry Standard
- 16-bit speed

Sun SPARCstation SBus #32

DECstation TURBOchannel #33

Macintosh NuBus #34

Macintosh SE/30 #37

VXI Embedded Controllers #35

IBM Micro Channel #36

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3½-in. hard-disk drives

Drives. Western Digital, for example, includes an adaptive 64k-byte cache on its 125M-byte AC2120. The controller monitors drive activity and adjusts the cache configuration during operation. For example, the controller can increase segment size while decreasing the number of segments available and vice versa.

You can buy a 0.75-in.-high, 85M-byte drive from Conner Peripherals, the $495 CP-4084. You can fit two of the drives into the space a single full-high 3½-in. drive requires. Thus, products should succeed in mid-life system redesigns and updates and in the upgrade aftermarket.

Looking ahead, you can expect to see 1G-byte 3½-in. drives by this time next year. Fujitsu's Michael Gluck predicts that by 1998 the technology will exist for drives with areal densities of 1G bit/in.²—10 times the density of the newest 500M-byte 3½-in. drives. The downsizing trend will not stop soon. Sherri Besser, Western Digital's marketing manager of 2½-in. drives, says these drives will cost less to manufacture than 3½-in. drives in two years. And some industry insiders have started talking about a new form factor that uses 1.8-in. media.

Manufacturers of disk drives

For more information on disk drives such as those discussed in this article, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Address</th>
<th>City, State, ZIP</th>
<th>Phone</th>
<th>Fax</th>
<th>Circle No.</th>
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<td>FAX (408) 436-6844</td>
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<td>(507) 253-1997</td>
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<td>FAX (408) 432-0457</td>
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<td>FAX (714) 583-3133</td>
<td>No. 665</td>
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<tr>
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<td>Irvine, CA 92618</td>
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It's a smart move.
Semaphores and controlled shared variables

The discussion of task coordination methods continues in Part 9 of this series with an overview of how semaphores and controlled shared variables coordinate tasks in real-time applications. Part 10 will discuss task coordination and communication via signals.

David L Ripps, Industrial Programming Inc

In most applications, tasks must share sets of data, such as a table that is read by one task and updated by another. A second example of shared data are the global variables within a non-reentrant procedure that could be called by different tasks.

A segment of code in which a task is accessing some shared resource is often called a "critical region" with respect to that resource. Not every reference to shared data forms a critical region, however. Accessing a fixed data table would not qualify. A region is critical only if there could be harmful interactions because of the sharing of the resource. For data, this means that the variables are both shared and alterable. More general resources, such as a printer or console, engender critical regions only when it is undesirable to intermix the output from different tasks on the same page or screen.

Shared resources must be protected against potentially harmful interactions by permitting only one task at a time to enter a critical region. In the first example, while the data is being read, the update task must be blocked; while the data is being updated, the reader task must be blocked.

In real-time applications, a critical region can be so small that its existence is easily overlooked. Suppose that a certain memory-mapped byte (call it lamps) is used to control eight lights: a 1 in bit i turns the ith light on; a 0 turns it off. Initially all lights are off. At some point task TskA turns light 7 on by OR-ing with 0x80. A higher-priority task, TskB, turns light 0 on by OR-ing with 0x01. Most of the time this works. But occasionally, because of an ill-timed task switch, the two tasks are in the critical region for lamps at the same time:

<table>
<thead>
<tr>
<th>TskA</th>
<th>lamps</th>
<th>TskB</th>
</tr>
</thead>
<tbody>
<tr>
<td>lamps=/&gt;reg</td>
<td>0x00</td>
<td>blocked</td>
</tr>
<tr>
<td>OR reg with 0x80</td>
<td>0x00</td>
<td>blocked</td>
</tr>
<tr>
<td>preempted by TskB</td>
<td>0x00</td>
<td>lamps=/&gt;reg</td>
</tr>
<tr>
<td>preempted by TskB</td>
<td>0x00</td>
<td>OR reg with 0x01</td>
</tr>
<tr>
<td>preempted by TskB</td>
<td>0x00</td>
<td>reg=/&gt;lamps</td>
</tr>
<tr>
<td>preempted by TskB</td>
<td>0x01</td>
<td>...</td>
</tr>
<tr>
<td>reg=/&gt;lamps</td>
<td>0x01</td>
<td>blocked</td>
</tr>
<tr>
<td>...</td>
<td>0x80</td>
<td>blocked</td>
</tr>
</tbody>
</table>

Shared resources must be protected against harm by permitting only one task at a time to enter a critical region of code.

In this case, the final value is $0 \times 80$ instead of $0 \times 81$. Problems such as these are insidious since they arise from subtle timing relationships.

Critical regions must be protected by guaranteeing one-task-at-a-time access. The MTOS-UX operating system provides two different facilities to achieve such mutual exclusion: the semaphore (SF) and the controlled shared variable (CSV), the SF being the simpler of the two.

A semaphore is an operating system object that is created by task request. In most applications, a separate SF is created for each critical region. (You could utilize a single SF to protect several regions, but this usually leads to excessive contention delays.) Prior to entering a critical region, every task must invoke \textit{waisem} to wait for the corresponding SF to be free. If another task already has taken that SF, the new task waits. Queuing is based on the current priority of the waiting tasks. Upon exiting a critical region, a task must relinquish control to the next waiting task:

\begin{verbatim}
  task A: request SF, enter critical region, ..., release SF
        ---- time ---->
  task B: request SF, <blocked for SF> enter critical region, ..., release SF
\end{verbatim}

A simple way to protect critical procedures is to make the first statement a wait-for-SF and the last statement before returning a release-SF. This method places all control aspects completely within the procedure. As a result, a caller does not have to know that the procedure is critical.

Creating a semaphore

A typical call to create a semaphore is

\begin{verbatim}
#define SF34 0x53463334
long int s34id; /* sample semaphore*/
s34id=crsem (SF34);
\end{verbatim}

The argument is the external name associated with the semaphore. If a semaphore with the given key already exists, the function just returns the identifier. Otherwise, the OS creates the SF and returns the identifier. Only in the unlikely case of not having any internal resources remaining does \textit{crsem} fail. The value returned upon failure is \textit{QUEFUL}.

Waiting for a semaphore

Every task that wishes to enter a critical region protected by semaphore \textit{SF34} must first issue a wait-for-semaphore-to-be-free request. In most cases, the call would specify wait-forever (\textit{WAIFIN}) coordination.

\begin{verbatim}
  long int result; /*result of request*/
  waisem (s34id,&result,WAIFIN);
\end{verbatim}

The first argument must be the identifier of an existing SF, as provided by \textit{crsem}. Otherwise, the function returns a failure value of \textit{BADPRM}. Failure values are also stored within the results buffer addressed by the second argument. As usual, a maximum wait time can be added to the coordination mode. Thus,

\begin{verbatim}
  waisem (s34id,&result,WAIFIN+10+SEC);
\end{verbatim}

waits up to 10 sec for the SF, while

\begin{verbatim}
  waisem (s34id,&result,CLEF2+1+MIN);
\end{verbatim}

waits no more than 1 minute for that SF and sets local event flag 2 as a completion indicator. The variable \textit{result} receives the final status when the request is completed: \textit{NOERR}, for success; \textit{BADPRM}, \textit{TIMOUT}, or \textit{QUEFUL} for failure.

Each SF either is free or is “owned” by a task that issued a \textit{waisem} without a corresponding release. Ownership is not permanent; once the release is given, the SF becomes free again to be owned by another task.

With some operating systems, the SF has just two states: free and in use. (In use means owned by some task, but the identity of the owner is not necessarily retained.) These are called binary semaphores. With a binary SF, any task, including the current SF owner, must wait if it issues a wait-for-semaphore request and the target SF is already in use.

MTOS-UX provides counting, not binary, semaphores. The difference between the two is that a task does not wait if it issues \textit{waisem} targeted to a semaphore that it currently owns. The SF has an internal use-count that is incremented by 1 each time the owner issues a wait request and is decremented by 1 each
time the owner issues a release. Note that the use-count is 0 when the SF is first created and when the SF is free.

There is value in providing counting semaphores, as opposed to just binary ones. In a complex application, it may be necessary for a task to make nested entries into critical regions for the same variables, say, in the main body of the code, and in some utility procedures. Each region separately needs the protection of the SF. With only a binary SF, it would be necessary for the task to know if it already has reserved the SF, and when it is safe to release it. With a counting SF, each critical region is bracketed by `waistem` and `rlsem` (release semaphore). Upon exiting from the last of these nested brackets, the SF count returns to 0, and the SF is automatically freed.

There is an essential difference between event flags and semaphores, even though both are used to achieve coordination between concurrent tasks. If several tasks are waiting for the same EF and it is set, then all those tasks continue simultaneously. If several tasks are waiting for the same SF and it is released, only one task (the one with the highest priority) continues; the others continue to wait.

The semaphore provided by MTOS-UX is similar to, but not exactly the same as, the semaphore proposed by Dijkstra (Refs 1 and 2). MTOS’s `waistem` is close to Dijkstra’s `P` or `wait`; MTOS’s `rlsem` is close to Dijkstra’s `V` or `signal`. The difference is that when a Dijkstra semaphore is created, a non-negative number (s) is assigned to the SF. Thereafter, s can increase or decrease (down to 0) via `P` and `V`. The action of `P` is

```
if (s > 0) then --s else block task on SF
```

The action of `V` is

```
if (any tasks are blocked on SF) then release 1 task else ++s
```

A Dijkstra SF need maintain only the use-count, s, and the list of tasks waiting for the SF; it need not record the current owner of the SF. Furthermore, the release `V` may precede the wait `P`, and the task that issues the release need not be the one that performed the wait. A Dijkstra semaphore permits s tasks to proceed into a critical region. These could be s different tasks, the same task s times, or any other combination that sums to s. MTOS-UX permits the same task to proceed any number of times, but blocks all other tasks.

Possession of a semaphore does not guarantee that a task cannot be interrupted by a task of equal or greater priority. Pre-emption is always permitted. However, having the SF does guarantee that a pre-empting task will not be allowed past a `waistem` for that SF.

**Deadly embrace**

There is no limit to the number of semaphores that a task can reserve and the number of `waistem` requests it can have outstanding. Thus, a task may wait for one SF while it has reserved another. But beware the deadly embrace. To illustrate this phenomenon, suppose that task D has reserved SF SFN1 and seeks SF SFN2. Task E already has SF SFN2 and seeks SF SFN1. Deadlock.

In principle, the solution is easy: Have all tasks that seek multiple semaphores always seek them in the same order. In complex cases, this may not be easy to arrange.

Deadly embraces can also arise from other combinations of limited resources. For example, a task that has a semaphore and is seeking a memory pool allocation can deadlock with a task that has a large portion of the memory and is waiting for that SF.

To reduce the effects of a deadly embrace, avoid unlimited waits. Use `WAIFIN + 10 MS`, rather than just `WAIFIN`. And when you fail to obtain one of the needed resources, relinquish other limited resources and then try again. Furthermore, you should use different time limits in different tasks to make it unlikely that the same deadly embrace will reappear on each cycle of retry.

**Releasing a semaphore**

The request

```
result = rlsem (s34id);
```

decreases the use-count of the given semaphore and releases it to the next user if the count becomes 0. If the argument is not a semaphore currently held by the calling task, the function returns a failure value of `BADPRM`. Two values represent success: `NOERR` means that the SF was released and is now free; `NOTFRE` means that the SF is still held since the count has not been reduced to 0.

For best overall performance, a semaphore should be released immediately upon exit from the critical region.

**Deleting a semaphore**

In a dedicated real-time application it is likely that control objects, such as semaphores, would be created.
Beware the "deadly embrace." Two tasks are blocked, because each needs a semaphore that the other has reserved for itself.

by an initialization task and then remain "forever." In contrast, the semaphores created by transient (temporary) tasks are not likely to be permanent. Thus, the OS provides a mechanism to delete a semaphore once it is no longer needed.

result = dlsem (s34id);

If the argument is not the identifier of a semaphore, the function returns a failure value of BADPRM. The function returns NOERR for success.

Usually, the SF is not in use when it is deleted. If it is in use, the delete request is discarded, and the function returns the warning value NOTFRE. Each task that accesses a nonpermanent SF should delete the SF before it exits.

Controlled shared variables

As already noted, it is common in real-time applications for a set of tasks to share a group of alterable variables. The semaphore facility permits the OS to grant each task exclusive access to the variables to prevent possibly harmful interference.

In some cases, however, a task does not simply want exclusive access to the variables; it wants that exclusivity only after a certain relation exists among variables in the group. Until then the task must be blocked. For example, suppose the group contains 32 binary variables akin to event flags. The task might have to be blocked until a given set of these variables are all equal to 1. Thus, the task might have to leave the critical region so that other tasks can access and change the variables, but then re-enter the critical region when the desired relation is true (Ref 3). MTOS-UX includes five service calls that make it efficient to handle this type of coordination.

cresv create a group of controlled shared variables
usecsv wait for exclusive access to a group of controlled shared variables
waicsv wait for given function of controlled shared variables to be TRUE
rlscsv release exclusive access to a group of controlled shared variables
dlcsv delete a group of controlled shared variables

Creating a group of CSVs

The first step toward establishing a group of controlled shared variables is defining their structure. To illustrate the creation and use of CSVs, assume that you are interested in maintaining multiple windows on a CRT screen. The supporting data is

```
#define NW 4 /* maximum number of windows*/
struct mw {
  long wid[NW]; /*width*/
  long len[NW]; /*length*/
  short avl[NW]; /*0=available*/
  /*position and other data*/
};
```

You can create a set of controlled shared variables having this structure via the sequence

```
#define WNDO
#define MWSIZ
struct mw * wndgid; /*identifier of group=addr of first variable*/
wndgid=(struct mw *) cresv (WNDO, (long ) MWSIZ );
```

The first argument (WNDO) is the usual key associated with the group of variables. The second argument (MWSIZ) is the overall size of the variables, in bytes. If a group with the given key already exists, the group identifier is returned as the value of the function when the current and original lengths match. When they do not match, BADPRM is returned. For a new key, the OS attempts to create the group. If successful, again the identifier is returned. If there is not enough internal memory currently available for creation, the function returns the error code QUEFUL.

The group identifier is also the address of the first variable. The group is created with all variables initialized to 0.

Waiting for exclusive access to CSVs

For tasks to share the variables successfully, all users must wait until the OS grants exclusive access. (This is the implication of the term controlled.) If the task needs exclusive access with no preconditions having to be met, it would invoke the unconditional form of the wait request. For example,

```
usecsv (wndgid,NOEND);
```

provides a wait without limit, while

```
usecsv (wndgid,100+MS);
```

sets a maximum of 100 msec to the wait. If the group does not exist, usecsv returns BADPRM. If the requesting task already has exclusive access to the
group, the return value is DUPTSK (duplicate task request). If the group is available or becomes so during the specified interval, the return value is NOERR. Finally, if the group remains unavailable during the given interval, the request is canceled and the return value is TIMOUT.

Once exclusive access is granted, the task may freely and safely read and write the group variables. Recall that the group identifier is also the address of the first of the variables. Continuing the example just introduced,

```c
if (usecsv (wndgid,100+MS)==NOERR)
{
    printf ("Size of window #1 is %lx by %lx\n", wndgid->wid[0], wndgid->len[0]);
    ...
    }
```

Releasing CSVs

When a task no longer needs its exclusive access to a group of CSVs, it must issue a release request.

```c
rlscsv (wndgid);
```

The argument identifies the group. Once the group is released, the task must not alter any of the group variables, even though the OS does not have the ability to enforce this rule.

Calls to waicsv and rlcserv mark the entry into and exit from the critical region for the group, in a way analogous to waisem and rlssem.

Waiting for the function of CSVs to be true

If only unconditional waits for access are needed, it is easier and faster to implement the variables as a task-level, public structure and protect the structure with an ordinary semaphore. The strength of CSVs arises when a task wishes to enter a critical region only when a certain condition is met among the variables. Alternatively, a task already within a critical region may wish to leave it until a condition is met.

The C function to wait for a certain relation among CSVs to be true is formally defined as

```c
int waicsv (gid,bfun,interval)
    long int gid,interval;
    int (*bfun) ();
```

The first argument identifies the variables group, the second argument supplies the address of the evaluation function, and the third argument indicates the maximum time to wait before returning from waicsv. If the interval is NOEND, the service can never time out. Possible return values are NOERR (for success), TIMEOUT (if bfun is never TRUE during the specified interval), QUEFUL (if the timer cannot be allocated), and BADPRM (if the group does not exist).

When it is called, bfun is presented with a pointer to the group variables as its only argument. The function must return an integer value of TRUE (nonzero) if the task is to be blocked or FALSE (zero) if the task is to be continued. No task-level service calls are permitted within bfun.

The wait service call may be made either as a way into the critical region or as a way to exit the region until bfun is TRUE. In either case, waicsv does not return successfully until both bfun is TRUE and the task has been given exclusive access to the variables.

The bfun evaluation function is called immediately after waicsv is invoked if the requesting task already has exclusive access to the variables or the variables are free. If the task is to be blocked, bfun will be called again each time a task leaves the critical region via rlcserv or waicsv. Whenever more than one task could be unblocked because its evaluation function is TRUE, only the highest priority task will be continued at that point. The others will have to wait until the variables are available again.

To complete the example already started,

```c
static int idx;    /* index of available window */
static int mwid;  /* min width of available window */
static int mlen;  /* min length of available window */
int testw ();     /* test value function */

waicsv (wndgid,testw, 5+MIN); /* wait for testw to be TRUE*/

testw (data)
    struct mw *data;
    {
        register int i;
        /* search index */
        for (i=3;i>=0;i--)
            {
                if (((data->avl[i])>0)&&(data->wid[i]>=mwid)&&(data->len[i]>=mlen))
                    {
                        data->avl[i]=1; /* take window */
                        idx=i; /* note which one */
                        return (1); /* end wait */
                    }
                data->avl[i]=0; /* keep waiting */
            }
        return (0); /* keep waiting */
    }
```

Whether or not a task had exclusive access to the group originally, it loses this privilege while it is blocked and regains it when the task becomes unblocked because its evaluation function was satisfied. However, it does not have access upon a time out or
other unsuccessful return. Thus, the application must have the following overall structure

```c
if (waicsv (wndgid, testw, 5+ MIN) == NOERR)
{
    
    ricssv (wndgid);
}
```

Deleting a group of CSVs

When a group of controlled shared variables is no longer needed by any task, it may be deleted by invoking

```c
result = dicsv (wndgid);
```

The function returns NOERR for success and BADPRM for failure.

The same problem arises in deleting a group of CSVs as in deleting a group of public event flags: how to know when the last task is finished with the group so that it can be removed. The same solution is used. Thus, dicsv does not immediately delete the group if there are any tasks waiting because of waicsv. If there are, the group is internally marked "deletion requested." Actual removal does not occur until there are no more tasks waiting. In the interim, all CSV functions may be applied in their normal manner.

Priority inversion

Once the OS grants task LP a semaphore, a group of controlled shared variables, or any other exclusive-access object, the OS is not free to take the object back and give it to another task. (That would defeat the whole purpose of providing exclusive-access objects.) As a result, if a higher-priority task (HP) seeks the same object, it must wait until LP releases the object. But, because LP is a low-priority task, it may take a very long time for LP to execute. Thus, a low-priority task can block a higher-priority one for an indefinite period. This is known as priority inversion.

Equivalent forms of priority inversion can occur when a task
- is blocked waiting to restart another task that is executing at a low priority,
- is blocked waiting to communicate with a partner that is executing at a low priority,
- or needs memory or another shared resource that is held by a low-priority task,

among other cases. This is not the same as a deadly embrace since in principle the high-priority task does get to run eventually.

In very simple cases, it is tempting to have the OS temporarily raise the priority of task LP to that of HP to break the inversion. However, because of the many and subtle ways in which priority inversions can occur, and the complexity of nested blockages, there is no easy way to avoid inversions completely. These problems are actively being investigated at the Software Engineering Institute of Carnegie-Mellon University (Ref 4) and other places.

To sum up, a critical region is a segment of code in which alterable variables or some other resource is being shared by two or more tasks. The resource must be protected against potentially harmful interactions by enforcing one-task-at-a-time entry into any critical region for that resource. Semaphores and controlled shared variables can provide the required mutual exclusion.

A semaphore is sufficient to protect a set of shared alterable variables when all entries into their critical regions are unconditional, that is, do not depend upon the current values stored in the variables. A semaphore is created for the set of variables. Before every task enters a critical region, it requests temporary ownership of that SF by issuing waicsv. The OS allows only one task to proceed; it blocks all others. When a task leaves the critical region, it releases the SF by issuing ricssv. If there are no tasks waiting for the SF, the SF is set free. Otherwise, only the highest priority task is unblocked.

Controlled shared variables are a further refinement of the idea of semaphore protection. The request to enter a critical region can contain a condition function. Now the task may be blocked until both exclusive access can be granted and the function (evaluated with respect to the variables) returns TRUE. The same service also permits a task that is already in a critical region to exit until the same two criteria are met.

Part 10 of this series will discuss task coordination and communication via signals.

References


Article Interest Quotient (Circle One)
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You can learn theoretical state-machine design from myriad sources, but most neglect to tell you how to design state machines that work reliably. Such neglect is unfortunate—and unnecessary—because reliability is fairly easy to come by.

Ricardo Rabinovich, Librascope Corp

Different design enhancements can decrease the likelihood that your state machine will reach an illegal state or illegally reach a legal state. Synchronizing or deglitching the inputs and filtering or decoupling the supply and ground rails are among the less obtrusive techniques you can use.

Unless the number of valid states in your state machine is a power of 2, the machine will have illegal states. An illegal state is a state that the machine cannot reach during its normal operation. The machine reaches an illegal state as a result of electrical noise, a power glitch, transient illegal input combinations, or other unfavorable conditions.

Another functional concern in designing state machines is the problem of the machine's reaching a legal state via an illegal transition. Most textbooks recommend that you explicitly specify a legal transition from illegal states to an initial idle state to recover from illegal state assignments. However, they generally do not address illegal transitions to legal states.

Unfortunately, in practical situations, defining an idle state is often difficult. Many state-machine designs have more than one idle state. Even when only a single idle state exists, changing to that state could hang-up the machine or system by leaving the system waiting for some output that doesn't occur.

Synchronizing and deglitching inputs require a simple circuit. Fig 1 shows a circuit that synchronizes an input with the system clock regardless of the input signal's normal polarity. This circuit consists of three D-type flip-flops, one of which has a multiplexed input and an exclusive-OR gate. The same clock-edge clocks all three flip-flops. The exclusive-OR gate validates the input-level change before that input change is transmitted to the rest of the state machine. If both inputs of the exclusive-OR gate are the same, the multiplexed input is selected.

Fig 1—A synchronizer circuit, such as this one, improves state-machine reliability by aligning asynchronous inputs to the clock while removing input glitches.
State machines aren’t supposed to reach illegal states, but because they occasionally do, you should design conservatively.

A multiplexer selects the state machine’s input signal. If the input levels are different, the multiplexer refreshes the existing signal. Therefore, the input signal must remain stable for at least one clock cycle before the state machine acknowledges it. In addition to synchronizing and degrading inputs, this pipeline arrangement prevents a metastable condition from propagating through the state machine.

The second step toward freedom from illegal states is to filter and decouple the power and ground rails. Usually all you have to do is connect a 0.1-µF capacitor between the two. Be sure to connect the decoupling capacitor as close as possible to each component. Decoupling is especially important when using high-speed logic, such as FAST or FCT parts.

Even with these precautions, building a highly reliable state machine demands that your design include logic that specifically prevents unwanted states and illegal transitions to valid states. An effective technique for detecting and suppressing illegal transitions is to sample the value of the next state in the middle of the system clock cycle and compare it with the value of the present state. If the transition is legal, the next state becomes the present state at the beginning of the next clock cycle. If the transition is not legal, the clock latches the present state again, ignoring the next state.

**Is the potential transition legal?**

The block diagram in Fig 2 demonstrates this technique. (For clarity, logic blocks have been labeled in all upper case, and signals have been labeled in lower case with an initial capital.) This circuit uses the SYNC block from Fig 1. Insync is the output signal of the SYNC block and is an input to the NSD (next-state decoder) block. The NSD is a combinatorial circuit that generates the next-state signal, Uns. Uns is strictly a function of Insync and the present state, Prst, of the state machine, and does not indicate the legality of the transition. The falling edge of the system clock latches Uns into the NSR (next-state register) in the middle of the clock cycle. The output of NSR and the Prst signal are inputs into the NSVAL (next-state validation) block of combinatorial logic, which evaluates the legality of the transition between states. The output of NSVAL controls a multiplexer. If the transition is illegal, then the NSVAL output is low, and the multiplexer feeds the state machine’s present state back to

---

**Fig 2—Adding logic that checks the legality of all state transitions before the machine executes them reduces the risk that your machine might enter states illegally.**
the PSR (present-state register). If the transition is legal, the NSVAL output goes high and the rising clock latches Uns into the PSR.

The NSVAL block checks whether a transition is legal on the rising edge of Sysclk. The OD (output decoder) block drives the output signal, Out, as a function of the present state only, regardless of changes that occur at the input of the state machine. By definition, then, the state machine in Fig 2 is a Moore machine, and its outputs are solely a function of the present state. A state machine whose outputs are a function of both the inputs and the machine's present state is a Mealy machine. You can use similar logic to design reliable Mealy machines. However, please note that Mealy machines are more prone to output glitches because the inputs and the system clock are asynchronous.

Designing a simple state machine will help clarify these reliability-ensuring techniques. Assume you must create a firing mechanism for a rocket launcher. To minimize the risk of false launches, the operation of the firing system requires the sequential assertion of two toggle switches. The wrong toggle-switch sequence invalidates the entry. The state diagram in Fig 3 describes the machine.

Calculating how fast the machine will run

After you have designed your state machine, you often want to know its maximum operating frequency: \( f_{\text{MAX}} = 1/T_{\text{MIN}} \). To simplify the calculations, you can assume the inverter delay is negligible. The worst-case delay among four circuit paths limits the maximum operational frequency. First, the delay through the SYNC circuit in Fig 1 is

\[
T_{\text{MIN1}} = T_{\text{MET}} + T_{\text{XORD}} + T_{\text{FFMXS}}
\]

and

\[
T_{\text{MIN2}} = T_{\text{dtd}} + T_{\text{XORD}} + T_{\text{FFMXS}}^2
\]

where \( T_{\text{dtd}} \) is the duration of metastability for a given MTBF,

\( T_{\text{XORD}} \) is the exclusive-OR gate delay, \( T_{\text{FFMXS}} \) is the MUX and flip-flop data setup time, and \( T_{\text{dtd}} \) is the flip-flop clock-to-output delay.

Then, the half-cycle delay through the SYNC circuit and the next-state register in the state machine of Fig 2 is

\[
T_{\text{MIN3}} = T_{\text{SYNC}} + T_{\text{NSDD}} + T_{\text{NSRS}}
\]

where \( T_{\text{SYNC}} \) is the clock-to-output delay of the SYNC block, \( T_{\text{NSDD}} \) is the NSD (Next State Decoder) block delay, and \( T_{\text{NSRS}} \) is the NSR (Next State Register) data set up time.

Lastly, the half-cycle delay from the NSR block through the present-state register in Fig 2 is

\[
T_{\text{MIN4}} = T_{\text{NSRD}} + T_{\text{NSVALD}} + T_{\text{MUXD}} + T_{\text{PSRS}}
\]

where \( T_{\text{NSRD}} \) is the NSR (Next State Register) clock-to-output delay, \( T_{\text{NSVALD}} \) is the NSVAL (Next State Validation) block delay, \( T_{\text{MUXD}} \) is the MUX block delay, and \( T_{\text{PSRS}} \) is the PSR (Present State Register) data set up time.

The longest of the above four delays determines your state machine's operating frequency:

\[
f_{\text{MAX}} = 1/T_{\text{MIN}}.
\]

where \( T_{\text{MIN}} = \text{MAX}(T_{\text{MIN1}}, T_{\text{MIN2}}, 2\cdot T_{\text{MIN3}}, 2\cdot T_{\text{MIN4}}) \).

Fig 3—This state machine, controlled by inputs X1S and X2S, launches a rocket from State 3.
A state machine should test all transitions to determine whether they are legal before the machine executes them.

State 0 is the idle state. As long as \( X_1 \) is 0, the machine ignores the value of \( X_2 \) and \( Y \) remains 0. When only \( X_1 \) is activated, the state machine goes to state 1 while \( Y \) remains 0. If \( X_1 \) is released while the state machine is at state 1, the state machine returns to idle State 0. If \( X_2 \) is activated while \( X_1 \) is active, then the state machine moves to State 2. Upon reaching this state, \( Y \) becomes 1, causing the missile launch. A launch returns the machine to State 0 and clears output \( Y \).

The state table (Table 1), which corresponds to the state diagram, supplies the Boolean equations for the next-state variables and the output of the machine.

Where \( G_1 \) and \( G_2 \) constitute a binary representation of the machine’s four states, \( P \) is the present state, \( N \) is the next state, and \( S \) is a synchronous input:

\[
G_2 N = G_2 P \cdot G_1 P \cdot X_2 S \cdot X_1 S,
\]

\[
G_1 N = G_2 P \cdot G_1 P \cdot X_2 S \cdot X_1 S + G_2 P \cdot G_1 P \cdot X_2 S \cdot X_1 S,
\]

and \( Y = G_2 P \cdot G_1 P \).

A Karnaugh map can help you simplify \( G_1 N \):

\[
G_1 N = G_2 P \cdot X_2 S \cdot X_1 S.
\]

The logic in the equations for \( G_1 N \) and \( G_2 N \) constitutes the NSD block. The equation for \( Y \) defines the logic for the OD block. The next-state validation circuit, NSVAL, is a combinatorial circuit that analyzes each next-state transition for all possible present states and determines whether the transition is legal. If the transition is legal, output variable \( M \) is 1. Conversely, \( M \) is 0 for all illegal transitions. The output of this circuit controls the multiplexer block.

The diagram shows legal transitions

Inspecting Fig 3 allows you to determine the legal transitions. These transitions are:

- From State 0, the state machine can go to State 0 or 1.
- From State 1, the state machine can go to States 0, 1, or 2.
- From State 2, the state machine will go to State 0.
- From State 3, the state machine will go to State 0.

The output variable, \( M \), is a function of both the
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present- and the next-state inputs (Table 2). A Karnaugh map helps simplify the Boolean equation for M:

\[ M = G_2N \cdot G_1N + G_2N \cdot G_2P + G_1N \cdot G_2P \cdot G_3P. \]

The equations for \(G_2N, G_1N, Y,\) and \(M\) provide the information you will need to build a simple state machine that is better protected against illegal states and illegal transitions.

Techniques such as synchronizing the inputs, preventing illegal transactions, and providing for the safe transition to an idle state from illegal states can increase the reliability of state machines. The requirements for your particular state machine will determine the most appropriate method to resolve illegal states or transitions. Design techniques that build forgiveness into your circuits are only part of your design arsenal. The best way to avoid state-machine hang-ups is to prevent noise from reaching the system and ensure clean input signals.

Acknowledgment

The author would like to thank L Prater for his collaboration in the development of some of the concepts presented in this article.

Author's biography

Ricardo Rabinovich is a staff engineer with Librascope Corp (Glendale, CA). A graduate of an electronic-engineering program at Buenos Aires University, Ricardo is a computer design engineer. He has worked with 68020-based microcomputer designs and recently helped design an ASIC containing a VMEbus interface.

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Buffers stabilize oscillator

Maxwell Strange
Goddard Space Flight Center, Greenbelt, MD

Adding a CMOS buffer to a classic op-amp oscillator dramatically improves its performance, while preserving its low cost and low power consumption.

The overriding source of frequency drift in Fig 1a is the nonsymmetry and variability of the op amp's output-saturation voltages. These effects produce output-amplitude variations, which, when fed to the inputs via $R_1$ and $R_2$, produce switching-threshold changes. Supply voltage, temperature, loading, and op-amp selection also affect these saturation voltages. You can clamp the op amp's output with reference diodes, but these diodes are expensive and power hungry.

The circuit of Fig 1b overcomes these problems and has other advantages as well. Gates A and B produce a rail-to-rail voltage swing to feed back to the circuit's input, eliminating the saturation-voltage drops of the op amp. If you select the proper op amp, only the circuit's passive components will affect its frequency stability. The circuit's output symmetry is near perfect over a wide range of supply voltages. Further, the buffers' output transitions are much faster than the op amp's slew-rate-limited transitions, allowing you to use a micropower op amp.

The circuits' output frequency is

$$f_0 = \frac{\log e}{2 \log \left(1 - \frac{2R_1}{2R_s} = \frac{R_1}{R_1 + R_2}\right) RC},$$

if $R_2 = 3R_1$, $f_0 = \frac{0.979}{RC}$

(EDN BBS DI #933)

To Vote For This Design, Circle No. 746

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**Fig 1**—Adding CMOS buffers to a classic op-amp oscillator (a) improves the oscillator's performance without significant increases in power consumption or cost (b).
Current loop controls SCRs

Robert Diffenderfer
*Gordos, Rogers, AR*

The circuit in Fig 1 allows a 4- to 20-mA loop to control an isolated (4000V) SCR drive. The SCR drive can, in turn, control lighting intensity or motor speed. With a 4-mA control input, the SCRs will turn on at 90 and 270° with respect to the power input. By increasing the control input to 20 mA, the SCRs will turn on at 0 and 180°.

The current loop develops a control voltage across R1, D1 and associated components clamp this voltage to 5V max to power 1-shots IC₁a and IC₁b.

Optoisolator Q₂ detects the zero crossings of the 120V ac input, providing a low-to-high transition that triggers 1-shot IC₁b. R₃ and R₄ affect the transition’s timing. You can adjust these components to compensate for propagation delays. When triggered, 1-shot IC₁b produces a 0.1-msec pulse. The pulse turns on Q₁, discharging capacitor C₂.

When Q₁ turns off, C₂ begins charging. The voltage across R₁ and the value of R₂ set the rate at which C₂ charges. IC₁₈ will produce a 0.1-msec pulse when the voltage on C₂ reaches approximately 2.5V. This pulse turns on either SCR₁ or SCR₂ via optoisolator Q₃. C₂’s charge time is

\[ t = -R_{02} \times C_2 \times \ln \left(1 - \frac{V_c - V_1}{V_F}\right) \]

where

- \( V_c \) = the input-logic threshold voltage (voltage across C₂),
- \( V_F \) = the voltage across R₁ (a function of the input current), and
- \( V_1 \) = the voltage to which C₂ was discharged (≈0.3V).

You may want to adjust the values of R₂ and C₂ to compensate for highly inductive loads.

(EDN BBS DI #935)

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*Fig 1—A couple of 1-shots and optoisolators let a 4- to 20-mA current loop control lighting intensity or motor speed.*
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CIRCLE NO. 112 C118 REV. E
Regulator measures battery voltage

Mark Freeman
Stratos Product Development, Seattle, WA

If your low-power μP system is battery powered, the μP can use a precision regulator to monitor its own battery voltage. The circuit in Fig 1 uses no precision passive components and requires no trimming. Error is less than ±3%, and linearity error is less than ±1%. You must write a short control and voltage-calculation routine for your μP.

The heart of the circuit is a Texas Instruments TL431 precision shunt regulator functioning as both a voltage reference ($V_{REF} = 2.5V$) and as an integrator/amplifier.

In operation, the μP first sets an output buffer high for a programmed interval. Then the μP sets the buffer low and waits for a trigger signal back from the monitor circuit. The ratio of the two time intervals yields the supply voltage.

While the output buffer is high, effectively connecting $R_1$ to the positive rail, capacitor $C_1$ discharges at the rate of $(V_{CC} - V_{REF})/(R_1C_1)$. When the μP's output buffer goes low, connecting $R_1$ to ground, $C_1$ begins charging at the rate $(V_{REF})/(R_1C_1)$. When $C_1$'s voltage reaches the turn-off voltage of $Q_1$, $Q_1$ turns off, developing the TRIGGER signal for the μP.

The μP fixes the discharge time $\tau_{DIS}$. $V_{CC}$ determines the charge time, $\tau_{CHG}$. Battery voltage is

$$V_{CC} = V_{REF}[(\tau_{CHG}/\tau_{DIS}) + 1].$$

The components in Fig 1 yield a 16.7-msec $\tau_{DIS}$, which will integrate out 60-Hz interference. $V_{CC}$ may vary between 3.5 and 6.0V.

Component values are not critical, and your μP's clock need not be accurate, as long as it does not drift during a conversion cycle. Choose $C_1$ such that at the highest value of $V_{CC}$, $C_1$'s voltage never goes lower than $V_{REF}$, because at that point the regulator will quit operating. Use a low-leakage, solid-tantalum capacitor for $C_1$.

If you want to measure some voltage other than the supply voltage, you can use an external CMOS switch or buffer to handle the switching chores. The only restriction is that the voltage to be measured must be greater than $V_{REF}$. (EDN BBS DI #932)

To Vote For This Design, Circle No. 748

Programmable source operates precisely

Jim Williams
Linear Technology Co, Milpitas, CA

Precise, voltage-programmable, ground-referenced current sources are usually complex and require trimming. Fig 1's simple configuration produces output current in strict accordance to the sign and magnitude of the control voltage, $V_{IN}$. The circuit's dynamic response is well controlled, and the circuit requires no trimming; the circuit's accuracy and stability depend almost entirely upon resistor $R$.

$IC_1$, biased by $V_{IN}$, drives current through $R$ (in this case, 10Ω and the load). Instrumentation amplifier, $IC_2$, operating at a gain of 100, senses the voltage across
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R. IC2’s output closes the loop back to IC1. Because IC1’s loop forces a fixed voltage across R, the current through the load is constant. The 10-kΩ/0.05 μF combination sets IC1’s roll-off, making the circuit stable.

Fig 1—This programmable current source’s dynamic response is well controlled, and the circuit requires no trimming.

Fig 2—For a full-scale input step, Fig 1’s response is clean with no slew residue or aberrations. Trace A is the voltage-control input, and Trace B shows the output current.

Assuming an errorless component for R, IC2’s 0.05% gain specification and its 5-ppm/°C temperature coefficient dominate the circuit’s initial error. High-grade film or wirewound resistors will not degrade this level of performance.

Fig 2 shows the circuit’s dynamic response for a full-scale input step. Trace A is the voltage-control input, and Trace B is the output current. Response is clean, with no slew residue or aberrations.

(EDN BBS /DL_SIG #931)

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EDN February 4, 1991
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FEEDBACK AND AMPLIFICATION

PLD is really a PROM

We did some checking for an interested reader and found out that a part an author (and company) called a PLD was really a PROM. The Design Idea “PLD adds flexibility to motor controller” on pg 177 of EDN’s March 1, 1990 (DI #808) issue contains a part labeled PLE5P8. This part number is an obsolete Monolithic Memories Inc designation for a simple 32×8-bit PROM.

Anne Watson Swager and Charles H Small Design Ideas Editors

EDN’s bulletin board is on line

Call EDN’s free bulletin board service (BBS) at (617) 558-4241 (1200/2400,8,N,1) and select /DI_SIG to get additional information or to comment on these Design Ideas.

Maxim Jay Skender
Microrobotics, St Charles, IL

You can get double duty from your clamping diodes if you tie them to the output of a D/A converter (or an op amp configured as a converter). In this fashion (Fig 1), you can use the clamping diodes as a controllable input during self-tests. (EDN BBS DI #934)
The recent alliance of Elco and AVX with Kyocera forms a solid business relationship that gives us even stronger connections to today's exciting world of technology.

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How To Avoid Losing Face On Your Color LCD Display.

Face it. The first thing everybody notices about your newest laptop is the display quality. Is it bright? Are the images clear and well modeled? Are the colors vivid?

With Cirrus Logic LCD VGA controllers, your answer is yes. Which is why we’re the leading supplier of display controller chips in the laptop and notebook market.

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Our monochrome solutions give you displays that PC Magazine called “the stars of our VGA color-mapping tests”** with up to 64 shades of gray. And with a lower dot clock rate, your power consumption is lower than other solutions for longer battery operation.

Cirrus Logic LCD controllers are fully compatible with the popular PC video standards and will work with LCD, plasma, or electroluminescent displays.

Simplify your design job. A higher level of integration gives you all this in the smallest form factor available. We also supply software and hardware design notes and full design support. You get the results you want quickly and easily.

Design a more competitive product. One that looks better — and makes you look better. That lasts longer on a battery. Use the display solutions from a proven technology leader in laptop and motherboard VGA: LCD controller chips from Cirrus Logic.

Get the picture. Get more information on LCD controllers. Call 1-800-952-6300, ask for dept. LL24

Cirrus Logic monochrome LCD controllers will also make everything from realistic scanned images to business charts look tastier.
NEW PRODUCTS

INTEGRATED CIRCUITS

2.5-GHz-Bandwidth, Variable-Gain Amplifier

- Provides 20-dB gain control
- Comes in surface-mount SO-8 package

The HPVA-0810 is a monolithic variable-gain amplifier that features 20 dB of gain and gain control over its entire dc-to-2.5-GHz bandwidth. Operating from a single 6V supply, the amplifier dissipates only 250 mW. Designed for use in VHF/UHF receivers, RF data links and broadband local-area networks, the amplifier can replace more expensive hybrid devices, which typically have narrower bandwidths. The device is available in a surface-mount SO-8 package. HPVA-0810, $13.25 (100).

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 351

1M-Bit CMOS DRAMs

- Feature 60-ns speed
- Support µPs with speeds to 16 MHz

With Read/Write cycle times as low as 110 nsec, the AAA1M300 series of CMOS DRAMs (dynamic RAMs) allows designers to implement zero-wait systems utilizing 16-MHz µPs. Complex interleaving or caching schemes are not necessary. The high-speed DRAM is also available in enhanced-page-mode versions with Read/Write cycle times of 25 nsec. The devices work over a supply range of 4.5 to 5.5V and a temperature range of 0 to 70°C. The DRAMs are available in DIPs, ZIPS, and SOJ packages with industry-standard interfaces and pinouts. $5 (10,000).

NMB Technologies, 9730 Independence Ave, Chatsworth, CA 91311. Phone (818) 341-3355. FAX (818) 341-8207. TLX 651340.

Circle No. 352

Transconductance Op Amp

- Has 700-MHz bandwidth
- Slew rate is 3000V/µsec

Called an operational transconductance amplifier (OTA), the OPA660 combines a voltage-controlled current source with a separate buffer amplifier. By programming the quiescent current using a single external resistor, users can optimize gain- and bandwidth-tradeoffs. The complementary emitter-follower buffer section provides a 700-MHz bandwidth, a 3000V/µsec slew rate, 0.06% differential gain error, and 0.02% differential phase error. Transconductance for the OTA section is 125 mA/V. You can connect the OTA and buffer sections to create a current-feedback amplifier. The OPA660 comes in 16-pin DIPs and SO packages, $4.35 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. FAX (602) 889-1510. TWX 910-952-1111.

Circle No. 353

Quad SPST Analog Switch

- Operates from a 5 to 30V supply
- Needs no V_ref supply

The HI-201 monolithic quad spst analog switch operates from a single 5V to 30V supply. The IC eliminates the need for a V_ref supply, which is normally required for operation with power supplies other than ±15V to maintain TTL compatibility without pull-up resistors.
A plug-in upgrade for the Harris HI-201, the IC typically consumes only 4 mW of power while operating over a supply range of ±4.5V to ±18V. Each switch is independently selectable and features an on-time of 260 nsec and an off-time of 100 nsec. On-resistance is typically 45Ω. The device is available in 16-pin DIPs, ceramic DIPs, SO, and 20-pin LCC packages in commercial, industrial and military temperature ranges. From $2.06 (1000).

Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No. 354

Automotive Smart Sensor
- Operates from a 9 to 30V supply
- Temperature range is −40 to +125°C

Operating from an automotive battery supply of 9 to 30V, the AD22001 5-channel comparator automatically detects the failure of headlamps, indicators, and other lights. The comparators operate by detecting a small threshold voltage, nominally only 1.75 mV, across a low-value shunt resistor, which can be a length of copper track on the circuit board. Compatible with automotive applications, all input pins on the sensor will withstand a continuous dc voltage from −34 to +36V, and a 60V transient for 40 msec. The five comparators are arranged as two pairs, each with a common output, and one comparator with a dedicated output. The comparator pairs test any two related lights in either the on or off condition, indicating a failure of one or both. The single comparator is intended for brake-light testing. The AD22001, which comes in a 20-pin plastic DIP, is specified for operation of a −40 to 125°C temperature range. $2 (OEM qty).

Analog Devices Inc, 804 Woburn St, Wilmington, MA 01887. Phone (617) 937-2381. Circle No. 355

Motor Controller
- Needs no Hall sensor
- Compatible with Delta/Y/Star motors

The first of the company’s Hall-sensorless ICs, the SSI-32M595 provides motor speed control for both 5V and 12V Delta/Y/Star motors. The µP’s starting the motor...
initiates the drive control, which activates EMF-induced self-commutation in the SSI-32M595. The controller’s EMF circuitry typically detects motion within the first revolution of the motor. Speed control, which is implemented through a control loop, is maintainable over a range of speeds to an accuracy of ±0.017%. The controller operates from a single 5V supply and comes in a variety of packages, including a 28-pin SO package. $5 (1000).

**Silicon Systems**, 14351 Myford Rd, Tustin, CA 92680. Phone (714) 731-7110. FAX (714) 669-8814.

_Circle No. 356_

**High-Speed, 6-Bit Flash A/D Converter**

- Conversion speed of 75 MHz
- 140-MHz full-power bandwidth

A pin-compatible upgrade to the AD9000, the MN5903 offers improved S/N ratios and a wider bandwidth. At 540 kHz, the S/N ratio is 38 dB; at 35 MHz, it remains high, at 36 dB. Full-power bandwidth is 140 MHz. The converter is available in two logic configurations. You can also use the MN5903A as a standalone 6-bit ADC or as a terminating device for 7- or 8-bit applications. The MN5903 is for use as a cascading device with the MN5903A for 7- or 8-bit applications. The parts differ only in their output coding for signals greater than V_ref. In the overrange, the MN5903’s outputs are set to a logic “0;” the MN5903A’s outputs are set to a logic “1.” The converters come in a 16-pin, hermetically sealed DIP. Commercial devices, from $39; extended-temperature-range devices, from $85 (100).

**Micro Networks**, 324 Clark St, Worcester, MA 01606. Phone (508) 852-5400. FAX (508) 853-8296.

_Circle No. 357_

But all you really need to know is that they’re made by NEC, a 24-billion-dollar company, and the fourth largest manufacturer of disk drives in the world. For more information, call 1-800-NEC-INFO.

EDN February 4, 1991

_CIRCLE NO. 11_
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5225 Verona Road, Madison, WI USA 53711-4495, Tel. 608-273-5008
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NEW PRODUCTS
TEST & MEASUREMENT INSTRUMENTS

1-GHz-Bandwidth Telecomm And General-Purpose DSOs
- Automatically make eye-pattern measurements
- Make statistical measurements
With appropriate plug-ins, the CSA 404 and 11403A DSOs have a 1-GHz repetitive-signal bandwidth. Both units have color displays. The CSA 404 makes measurements that are useful in communications work. For example, as it acquires signals, the DSO constructs a statistical database, allowing it to measure jitter and noise without user intervention. The same database enables the unit to make direct, automatic eye-pattern pulse measurements. To determine whether a device under test meets specs, the scope can make mask tests; it stores ten masks in nonvolatile memory. The 11403A, a general-purpose scope with DSP capabilities and as many as eight channels, also makes pass/fail tests. It can display six such measurements simultaneously.

CSA 404, $22,000; 11403A, $18,950.
Tektronix Inc, Box 19638, Portland, OR 97129. Phone (800) 426-2200. Circle No. 360

Real-Time ICE For 33-MHz i960CA RISC µP
- Interfaces with MS Windows 3.0
- Performs nonintrusive monitoring and control
The Express Plus is an IBM PC/AT-hosted real-time in-circuit emulator that nonintrusively monitors and controls the 33-MHz version of the i960CA RISC (reduced-instruction-set computer) µP. The unit’s software runs under MS Windows 3.0. The target processor remains in the target system, reducing the likelihood that connecting the emulator will interfere with proper target operation. Besides passively monitoring the µP’s bus, the instrument uses all of the control information available from the µP to reconstruct programs executing from cache memory. It lets you halt the processor, execute single instructions, set software and hardware breakpoints, examine registers, and trace program execution. The unit is compatible with C-language tools from Intel and Microtec Research. You can obtain interfaces to the SGDB960 and Xray source-level debuggers. $28,750. Delivery, 60 days ARO.
Step Engineering Inc, Box 3166, Sunnyvale, CA 94088. Phone (800) 538-1750; in CA, (408) 733-7837. FAX (408) 733-1073. TWX 910-339-9506. Circle No. 361

Programmable Power Supply
- Has three outputs—6V at 2A and dual 28.1V at 125 mA
- Uses 12-bit ADC to read back voltages
The PPS-2806 is a triple-output programmable power supply on a card that plugs into the IBM PC bus. The unit contains one supply rated at 6V and 2A, and a pair of supplies that can produce 28.1V at 125 mA. Besides furnishing constant voltage, the last two supplies can produce or absorb constant current. You can also connect them in series or ground their positive or negative terminals. In addition to the supplies, the board contains a 12-bit ADC that can monitor voltage, current, or resistance. The board comes with menu-driven software that displays the outputs and ADC readings in numerical and graphic form. You can also control and monitor the board by reading from, and writing to, its registers. $1296.
Analyx Inc, Box 14644, Fremont, CA 94539. Phone (415) 656-8017. FAX (415) 657-0927. Circle No. 362

RTD Simulators
- Produce errors as low as ±0.005%
- Use Waidner-Wolf shunt circuits to minimize errors
The RTD-100, RTD-100X, RTD-200, and RTD-500/1000 simulate resistance-temperature detectors (RTDs), sometimes called platinum resistance thermometers. The RTD-100X is accurate to ±0.005% over its range of 10 to 1111.11. To minimize errors caused by contact resistance, the units use Waidner-Wolf shunt circuits on their three most sensitive ranges. With
this technique, a contact resistance of 1.5 mΩ affects the measured resistance by 4 µΩ, a value that represents a 0.4% error in a 1-mΩ step, the smallest step. $600 to $1795.

**General Resistance**, Box 155, North Branford, CT 06471. Phone (203) 481-5721. FAX (203) 481-8937.

Circle No. 363

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**VMEbus-Based Simulators For MIL-STD-1553 Bus**

- Test and simulate MIL-STD-1553 Bus
- Operate as bus controller, remote terminal, or bus monitor

The EXC-1553VME/E and EXC-1553VXI/E are intelligent interfaces between the VME- and VXIbus systems and the MIL-STD-1553 bus. The modules can also simulate and test the MIL-STD-1553 bus. The vendor furnishes the modules in B and C sizes. They can operate as bus controllers, remote terminals, or bus monitors. In all of these modes, they can detect errors; in the controller and terminal modes, they can inject errors under program control. The units have a memory-mapped interface. Options include sinusoidal and variable-amplitude transceivers. From $6995.

**Excalibur Systems Inc.,** Box 6839, Fresh Meadows, NY 11356. Phone (718) 357-3500. FAX (718) 357-3544. TWX 650-347-3609.

Circle No. 364

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**SPARCstation Interfaces To VXI and VME Buses**

- Plugs into workstation’s Sbus
- Interfaces to 6U VME systems and B- and C-size VXI systems

The VXI-SB2020 and VME-SB2020 kits allow you to control VXI and VME systems from Sun Microsystems’ SPARCstation workstations. Each kit includes a card that plugs into the workstation’s Sbus and generates the MXI (multisystem extensions interface) bus. A 2m MXI cable is included. Also in each kit is a module that receives the MXI bus and plugs into the VXI or VME bus. The VXI kit includes a C-size slot-0 board. The VME kit contains a 6U VME card that works in VME systems and in B-size VXI systems. Both kits include software tools that run under the SunOS operating system. These tools allow you to configure system resources and to control and transfer data to
A picture is worth a thousand points in a time interval measurement.

The SR620 brings graphic statistical analysis to time interval and frequency measurements. The SR620 shows you more than just the mean and standard deviation - multimode frequency distributions or systematic drift for example. Histograms or time variation plots are displayed on any X-Y oscilloscope, complete with Autoscale, Zoom, and Cursor functions. Hardcopy to plotters or printers is as easy as pushing a button.

Of course, the SR620 does everything else you'd expect from a high resolution universal counter, such as frequency, period, time interval, pulse width, rise / falltime, and phase measurements. The SR620 offers 25 ps single-shot time and 11 digit frequency resolution and complete statistical analysis, all for a fraction of the cost of comparable instruments.

For the whole picture, call SRS and ask about the SR620.

SR620 $4500
- 4 ps single shot least significant digit
- 25 ps rms single shot resolution
- 1.3 GHz maximum frequency
- $10^9$ Hz frequency resolution
- Sample size from 1 to 1 million
- Frequency, period, time interval, phase, pulse width, rise and fall time
- Statistics - mean, standard deviation, min max, and Allan variance
- Analyzer display on any X-Y oscilloscope
- Hardcopy to printer or plotter
- GPIB and RS232 interfaces
- Optional oven timebase
VXI and VME modules. C-size VXI kit, $3700; VME/B-size VXI kit, $3300.

National Instruments Corp, 6504 Bridge Point Pkwy, Austin, TX 78730. Phone (800) 433-3488 (US and Canada); in TX, (512) 794-0100. FAX (512) 794-8411.

Pocket-Size ESD Tester
- Checks static-protective items
- Shows discharges produced by touching conductors
- Can also show when a discharge occurs as a result of touching high conductivity areas of objects charged to different potentials—for example, an IC pin and a circuit board trace. You can use it to test static-protective devices, such as wrist straps and antistatic mats. It

Pocket-Size ESD Tester

National Instruments Corp, 6504 Bridge Point Pkwy, Austin, TX 78730. Phone (800) 433-3488 (US and Canada); in TX, (512) 794-0100. FAX (512) 794-8411.

Circle No. 365

EDN February 4, 1991
Position-Sensitive/ Ranging Components

Hamamatsu offers a variety of auto-focus and position detectors especially designed for proximity switching, displacement sensing and optical distance measurements. They are smaller, faster, require less power and feature more stable performance than comparable types.

Applications include auto-focus cameras, computer disc drives, linear motion detection in industrial equipment, beverage dispensers, robotic controls and automated car wash equipment.

CIRCLE NO. 79

Hamamatsu Photocouplers

Don't miss our newest catalog. It covers the complete line of Hamamatsu photocouplers including CdS Cell, Photo IC and Phototransistor output types. Also included are photointerrupters and photoreflectors.

Many can be used in surface-mount applications for non-mechanical position sensing and high voltage isolation of circuits.

Applications include color video signal interface for TV, high speed I/O computer interface, line receiver interface, electronic motor control and switching regulators.

CIRCLE NO. 79

Hamamatsu CdS Photoconductive Cells

This catalog is a must for every electronics designer. Hamamatsu CdS cells are available in plastic-coated, metal-case and glass-bulb type assemblies for a wide variety of applications.

Applications include exposure meters, light dimmers, musical equipment, flame monitors, street light controls and many others.

CIRCLE NO. 79

Hamamatsu Photodiodes

Did you know that Hamamatsu offers a complete line of photodiodes? From UV to IR, GaAsP, SI, PIN, APD and GaP, they're all here in our latest catalog. Send for it today.

Applications include high speed light sensors, CAT scanners, X-ray monitors, illuminance meters, light absorption meters, light-to-logarithmic voltage conversion circuits and more.

CIRCLE NO. 79

P2288 and P2613 Pyroelectric Detectors

These competitively priced devices feature a large sensitive area and offer optimal spectral response in the near IR. Built-in impedance converting circuitry makes them easy to design into equipment.

Applications include intrusion and fire detectors, industrial robots and other electronic sensing devices.

CIRCLE NO. 79

Hamamatsu UVtron R2868 Flame Sensor

The UVtron flame sensor can detect the ultraviolet radiation of a match from distances greater than 15 feet. Quick detection, wide directivity and compact design make it easy to integrate the R2868 into your products.

Applications include flame detectors for industrial, automotive and petroleum plant environments; also in horse or livestock stables.

CIRCLE NO. 79

ADVERTISEMENTS

P2288 and P2613 Pyroelectric Detectors

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Applications include intrusion and fire detectors, industrial robots and other electronic sensing devices.

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CIRCLE NO. 79
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NEW PRODUCTS

Source-Level C Debugger For Motorola’s 68000 µP family

• Includes cable to connect a target ROM socket to a PC host
• Provides six display windows for program I/O and debugging data

The Quickfix C-language source-level debugger complements the vendor’s cross-compiler for 68000-based embedded applications. The debugger makes use of a cable that connects the ROM socket of a target system to a parallel port on the host IBM PC or compatible. To configure the ROM socket driver, you need only specify the ROM socket base address, the socket width (8, 16, or 32 bits), and the ROM size. You can use host RAM in place of the ROM, or you can piggy-back the displaced ROM onto the cable so that both the ROM and the debugger operate simultaneously through the common socket. The debugger provides six windows: The source window displays the C or assembly-language execution context whenever the debugger stops; the register window displays the contents of the processor registers; the command window accepts your commands and displays their results; a data-display window shows the current values of specified C expressions; a terminal window emulates a terminal connected to the target and displays output from the program under test; and a help window provides on-line, context-sensitive debugger command and usage information. Quickfix, $1750; Quickfix with the Sierra C compiler, $1500.

Sierra Systems, 6728 Evergreen Ave, Oakland, CA 94611. Phone (415) 339-8200. FAX (415) 339-3844.

Circle No. 358

Printed-Circuit-Board Design System

• All modules share the same database and user interface
• Symbol library includes IBM PC expansion-board symbols

Eagle (Easily Applicable Graphics Layout Editor) handles all phases of pc-board design, from net-list input through layout to autorouting. All modules share the same database and menu-driven user-interface, so moving from one module to another is fast and easy. You can issue commands from a mouse, a keyboard, or a combination of both; the macro facility lets you assign frequently used command sequences to a function key; the total number of macros is limited only by the amount of available memory. The symbol library includes DIP and SMT devices, Zilog, Intel, and PAL devices, passive components, and standard IBM PC expansion boards. You can edit any of the library symbols and create your own symbols for inclusion in the library. The Undo/Redo feature backs up all command sequences in an unlimited history file, thereby allowing you to recover from errors or unsuccessful design steps. The system can work with both EGA and VGA graphics (color or monochrome) and can output to dot-matrix and laser printers, or to a Gerber photoplotter. To run the program, you need an IBM PC or compatible with at least 640k bytes of RAM and a hard disk; the program will use a mouse or a math coprocessor if these are present. Schematics editor, $495; Eagle alone, $399, or $699 with autorouter; complete system with schematics editor, layout editor, autorouter, and Gerber driver, $1199.

American Small Business Computers Inc, 327 S Mill St, Pryor, OK 74361. Phone (918) 825-4844. FAX (918) 825-6359.

Circle No. 359
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NEW PRODUCTS
COMPONENTS & POWER SUPPLIES

Low-Power Switches
- Available in multiunit versions
- Have switch life of 100,000 operations min

KS Series switches are available in individual (KSM) and multiunit (KSR) versions. The spst KSM units handle loads as high as 24V at 50 mA. Contact resistance measures 100 mΩ max, and switch life is 100,000 operations at rated load. Insulation resistance and dielectric strength equal 100V dc and 250V ac, respectively. KSR devices are available in 4-, 6-, and 14-switch blocks. Offered in spst and dpst configurations, the multiswitch units are rated for loads of 20V at 2 mA max. Insulation resistance and dielectric strength for these devices measure 100V dc and 150V ac, respectively. With a 5V/1A load, switch life for KSR devices equals 200,000 operations. Contact resistance measures 500 mΩ max. KSM versions, from $0.04 (OEM qty).

Lighted Pushbutton Switches
- Offer a choice of light sources
- Available with spdt or dpdt contact configurations

A3G LPB switches feature a snaplock, socket-mount design that allows you to connect the actuator to the base easily. The units mount in 16-mm panel cutouts, have a 100,000-operation lifetime, and are available with spdt or dpdt contacts in momentary, alternating, or indicator versions. Pushbuttons and indicators are available in round, square, or rectangular styles with a choice of LED, incandescent, or neon light sources. General-purpose contacts are rated for 3A at 250V ac, 5A at 125V ac, or 3A at 30V dc. Ratings for low-level applications are 100 mA at 125V ac or 30V dc. The switches feature oil-resistant (IP65) service ratings. The line also includes nonlighted, selector switch, and key-type versions. Lighted switches, from $7.80; nonlighted models, from $5.90 (500).

IDC Sockets/Headers
- Offer as many as 100 positions
- Rated for 5A at 30V

The sockets in this line of IDC (insulation displacement connector) devices accept 0.025-in. pitch cable. The sockets and headers are available in sizes ranging from 10 to 100 positions and come with either straight or right-angle leads. The units accept #30 AWG pitch planar cable and mate with 0.016-in. square pins. The socket and header combination is rated for 30V at 0.5A. The socket features a double-beam contact design. Contacts are phosphor bronze with 30 µin. of gold plating over 100 µin. tin. The glass-filled polyester insulators carry a 94V-0 UL flammability rating. $0.045 to $0.050 (1000) per position for sockets; $0.03 per pin for headers. Delivery, stock to six weeks ARO.
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- Frequency Stability: ±50 ppm (−55°C to +105°C)

**SURFACE MOUNT CRYSTAL UNITS**
- Frequency Range: 3.5 MHz-360 MHz
- Mode of Oscillation: Fundamental to 9th O.T.
- Frequency Tolerance: @ 25°C: ±2.5 ppm to ±100 ppm
- Frequency Stability: ±100 ppm (−10°C to +70°C)

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CIRCLE NO. 14

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Micro Switch, 11 W Spring St, Freeport, IL 61032. Phone (815) 235-6600. Circle No. 371

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- Features a 640×400-pixel display area
- Has an 18-.cd brightness

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Toshiba America Inc, 1 Pkwy N, Suite 500, Deerfield, IL 60015. Phone (708) 945-1500.

Circle No. 372

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- Features automatic speed control
- Reduces noise by 15 dB

Smart Fan’s self-contained electronics automatically controls its speed to regulate temperature in equipment enclosures against changes in room temperature, system power dissipation, flow resistance, and altitude. A self-contained thermistor senses the temperature changes, and proprietary control electronics adjusts the airflow to maintain a constant temperature once the system temperature exceeds a preset minimum level. This scheme protects critical components against temperature-related failure and reduces the overall noise by 15 dBA. The fans are available with an internal alarm, which activates when temperatures exceed the norm by 10°C, or when there is a loss of cooling-system power. The fans are offered in a variety of popular sizes including 4.7 × 4.7 × 1.5, 3.6 × 3.6 × 1, and 4.7 × 4.7 × 1 in. $15 (5000).

NMB Technologies Inc, 9730 Independence Ave, Chatsworth, CA 91311. Phone (818) 341-3355. FAX (818) 341-8207. TLX 651340.

Circle No. 373
The Analog Behavioral Modeling option for the PSpice Circuit Analysis package allows you to describe analog components, or entire circuit blocks, using a formula or look-up table. Linear blocks can be described using either a Laplace transform or a frequency response table. Once defined, you can use these blocks in all PSpice analyses, including DC, AC, and transient.

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- **Digital Simulation**: simulation of mixed analog/digital circuits with feedback between the analog and digital sections.
- **Monte Carlo Analysis**: calculates the variations in a circuit's performance allowing for component tolerances. This option performs statistical analyses: Monte Carlo, Sensitivity, and Worst Case.
- **Probe**: acts as a "software oscilloscope" to provide an interactive viewing and processing environment for simulation results (see photo).
- **Parts**: is a parameter extraction program allowing the extraction of device model parameters from data sheet information.

PSpice is available on the PC (running DOS, Protected Mode DOS, or OS/2), Macintosh II, Sun 3, Sun 4, and SPARCstation, DECstation 2100, 3100, and 5000, and the VAX/VMS families.

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Adtron Corp, Box 1848, Gilbert, AZ 85234. Phone (602) 961-7511. Circle No. 374

Sbus Expansion Boards
• Consist of a SCSI host adapter and communication board
• Communications board has one parallel and eight serial ports
Two Sbus expansion boards are available for the company's desktop SPARC workstations. The serial parallel controller, a communications board, has eight serial ports and one parallel port. You can install three boards in a SPARCstation 1/1+ to connect as many as 18 asynchronous devices such as modems, printers, and terminals. Each port on the card can transfer data at 38.4k baud. A SCSI host adapter connects as many as seven SCSI devices to the workstation. The board can transfer data at 5M bytes/sec and divides heavy disk traffic between two SCSI channels. It supports disk drives with as much as 2.6G bytes of storage. Serial parallel controller, $1095; SCSI host adapter, $495.

Sun Microsystems Inc, 2550 Garcia Ave, Mountain View, CA 94043. Phone (415) 960-1300. FAX (415) 969-9131. Circle No. 375
Modem Board
- Has as many as eight modems on one ISA bus board
- Operates at 2400 bps and uses the Hayes AT command set

The Digichannel Modem/X board for the ISA bus has four or eight modems. It can operate at 2400 bps and utilizes the Hayes AT command set. The modem conforms to the Bell 103, Bell 212A, CCITT V.22, and CCITT V.22 bis specifications. Besides providing autoanswering and tone or pulse dialing, the board also meets FCC Part 68 and FCC Class B requirements. Because the board is compatible with the company's PC/X board, the board works with Santa Cruz Operation's Unix and Xenix serial drivers. As many as four modem boards can be installed in a single computer to support as many as 32 users simultaneously. You can also configure the board's address and interrupt requests in software. 4-modem board, $1195; 8-modem board, $1995.

SPARC Workstation
- Runs at 40 MHz and has 16M bytes of RAM
- Has three Sbus slots and Ethernet port

The SPARCstation 2 family of workstations uses a 40-MHz CMOS SPARC integer and floating-point processor. The system's CPU board also contains a SCSI controller; an Ethernet controller; 16M bytes of memory expandable to 96M bytes; an audio port; and two serial ports. The system achieves 21 Specmarks, which is a figure that represents the geometric mean of 10 benchmark tests. The system runs the SunOS operating system and supports the following network protocols: NFS, TCP/IP, PC-NFS, and TOPS. Features include three Sbus expansion slots; a 3½-in., 1.44M-byte floppy-disk drive; and support for an internal 414M-byte drive. You can also attach an external drive for a total capacity of 7.6G bytes. A GS and a GT model has 3D color graphics. $14,995.
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Image-Compression Board
- Compresses frame-buffer images
- Can achieve compression ratios as high as 40:1

The ZR73660 image-compression and decompression board for the 16-bit ISA bus can compress an image from a frame buffer to a disk or decompress an image from a disk to a frame buffer in approximately 3 sec. It accepts data from frame buffers that have 512 x 480-pixel, 24-bit Targa-24 color images. Compression ratios are as high as 40:1. The company's ZR34161 vector µP calculates algorithms and mathematical transforms, using single instructions that operate on the entire data set. The board has an 80286 µP and occupies a single slot in the host computer. The Development Environment includes three software packages and the company's Imagineering DSP board. Board and software, $875; Development Environment, $4500.

Zoran, 1705 Wyatt Dr, Santa Clara, CA 95054. Phone (408) 986-1314. Circle No. 379

Synchronous Communications Board
- Has 80376 µP and DMA
- Two 16C30 multiprotocol chips control four serial ports

A synchronous communications board is available for the 16-bit ISA bus. It uses Intel's 80376 µP, a member of the 80386 µP family for embedded control. The 16-MHz µP relieves the host of synchronous-protocol overhead and communications tasks. The µP has use of 256k bytes of dual-ported RAM, 512k or 2M bytes of local RAM, and from 32k to 128k bytes of EPROM. An Intel 82370 chip provides DMA for the serial communications channels. Two Zilog 16C30 multiprotocol controller chips control full-duplex data transfers at 10M bps for each of the four synchronous serial ports. An X.25 software package, which allows a Unix system to operate as a LAN server, is also available. Board, $1800; board and X.25 software, $2495.

Star Gate Technologies Inc, 29300 Aurora Rd, Solon, OH 44139. Phone (800) 782-7428; in OH, (216) 349-1860. FAX (216) 349-2056. Circle No. 380
Zilog's integrated universal serial communication controller (Z16C31) combines two 32-bit full duplex DMA channels with a powerful single-channel USC cell. And that means efficient bus access, sophisticated buffer management, higher throughput, a greatly reduced CPU workload, and considerably lower cost for complex data communications applications.

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Integrated buffer management.
The IUSC's two 32-bit DMA channels provide for 32-bit addresses and 16-bit data word transfers... and they allow full duplex operation at 10 Mb/s. The two simple DMA modes, normal and buffered, mean your design can be tailored to common buffer management schemes. The two chained DMA modes, array chained and link array chained, reduce CPU overhead in advanced buffer management schemes. The daisy-chain DMA priority structure makes it easy to design multiple IUSC systems.

Versatility and reliability.
The IUSC's flexible, multi-protocol design lets you adapt your system to a variety of networks as interconnect standards evolve. The IUSC supports ten protocols and eight data encoding formats, including asynchronous, bit and byte synchronous, HDLC, isochronous, Ethernet and MIL-STD-1553B. And it all comes to you off the shelf, backed by Zilog's proven quality and reliability. To find out more about the IUSC or any of Zilog's growing family of Superintegration products, contact your local Zilog sales office or your authorized distributor today. Zilog, Inc., 210 Hacienda Ave., Campbell, CA 95008, (408) 370-8000.
Data Book And Designer’s Guide For GaAs ICs

The 1991 GaAs IC Data Book and Designer’s Guide describes GaAs ICs, including the Picologic, Nano-RAM, and NanoROM families, fiber-optic communications products, and standard cell arrays. The 496-pg publication highlights seven new devices, making a total offering of 46 IC products. Other featured products include chip sets for direct digital synthesis, PLL frequency synthesis, and an 800-MHz pin drive for automatic-test-equipment pin electronics applications. The Designer’s Guide contains 14 application notes.

Gigabit Logic, 1908 Oak Terrace Lane, Newbury Park, CA 91320. Circle No. 381

Real-Time Data-Acquisition Products

This 30-pg catalog describes real-time IBM PC-based instrumentation. It provides product specifications, comparisons with competitive products, and advice for buying a data-acquisition system. The publication features application notes and a guide to the Codas product line, a PC-based waveform recorder.

Dataq Instruments Inc, 825 Sweitzer Ave, Akron, OH 44311. Circle No. 382

Booklet Discusses Servo Analyzer

This 22-pg brochure focuses on the RF9211C FFT servo analyzer. It describes the instrument step by step and provides illustrations of sample screens. The publication mentions several added functions, including analysis of low-frequency noise in semiconductor devices or sensors; a zoom function for high-resolution measurement in steps of 100 mHz at any frequency range; and synchronous octave analysis through DSP techniques.

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The indicating triangle of the CelsiClock™ labels turns permanently black when the surface reaches the specific "switch" temperature level of that triangle. Highly visible labels are available as single temperature spots or in multiple sequenced temperature increments. Labels are self-adhesive and quickly placed on any dry surface. Temperature ranges from 10°F (−12°C) to 550°F (288°C). FREE SAMPLE on all inquiries.

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To advertise in Product Mart, call Joanne Dorian, 212/463-6415
EDN February 4, 1991
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Try SCHEMA III for free, and see how easy schematic capture can be. SCHEMA III performs many functions on the drawing sheet level and is compatible with workstation formats. Call Ovation for your FREE demo disk today!

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**MFI-421**

Multi Functions in One Instrument

- Frequency counter * Range: 1 Hz - 100 Mhz
  * Sensitivity: 1 Hz - 60 Mhz (15mV) 60 - 100 Mhz (25mV)
  * Accuracy: ± (f Hz + 1 digit + Time base error) * Display: 8 digits LED w/ units annunciator
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R.L.C.'s large selection of 8 and 16-Bit STD Bus Single Board Computers offer on Intel 80C186/188 CPU and 80C187/8087 Numeric Co-Processor at true bus speeds up to 16 MHz. On-board functions include MEMORY, SERIAL PORTS, REAL TIME CLOCK, TIMERS, DMA, INTERRUPT CONTROLLER, and BATTERY BACK-UP, WATCHDOG TIMER and much more. R.L.C. also offers 16-bit support cards, card cages and complete software support using the award winning TURBO-DEBUGGER. For more information and technical assistance please call Robert Coomer.

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TekTouch™, our analog capacitive touch screen, has six UL certifications. Its rugged construction allows it to stand up to harsh environments and heavy-use applications, but its exceptional optics make it ideal for more delicate uses, such as medical equipment.

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C for the 8051

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CIRCLE NO. 768

CIRCLE NO. 769

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Reliability and Maintainability Prediction and FMECA Analysis Software

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(415)726-3000 Tlx: 910-350-5842

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CIRCLE NO. 774

CIRCLE NO. 775

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The power of a consistent and colorful campaign can be yours with EDN's Product Mart Section.
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NEPCON West '91 makes Design For Manufacturability a reality. It is the largest event that brings together all aspects of electronic manufacturing. You'll see leading design companies including Mentor Graphics, Intergraph, Valid Logic, Dazix, and Data I/O—in EPCAD our special design center devoted to the newest methods in design automation software, imaging and photoplotting techniques.

Find the newest advancements in design techniques when you attend our conference program which has an entire track devoted to CAE/CAD/CAM/CIM. Learn from industry experts including Robert Myers, the President of Omnimation, as he speaks about Open CAM Systems and the use of CAD Data in PCB Manufacturing. Discover the latest developments in concurrent engineering and Design For Manufacturability in sessions presented by Dr. Sam Shina of The University of Lowell.

NEPCON West '91 is the best, most important industry event for design solutions. It is the one event where you will find the design products that you need as well as the packaging, production and test products your manufacturing team needs. All in one place. All at one time.

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Who’s into disk drives for the long haul? One look around the industry shows you that no one’s doing disk drives — or planning for long-term growth — better than Quantum.

That’s because we realize that success comes easier when you’re surrounded by good, dependable people. And you’re linked with some of Silicon Valley’s hottest companies.

The results so far? Unprecedented third quarter sales of $231.6 million, an increase of 108% over the same period in 1990. That growth and a penchant for continuous innovation has created opportunities for you to get in on some great development work at Quantum.

Our location in the San Francisco Bay Area also gives you a year-round Mediterranean climate, blue skies and weather that enables you to enjoy recreational activities that range from hiking and sky-diving to skiing and surfing. Find out more about joining Quantum in one of these positions.

**Disk Drive Engineers**
- Servo Engineer, Dept. 618EDNM
- High-Speed Digital Design Engineer, Dept. 641EDNM
- Test Equipment Design Engineer, Dept. 633EDNM
- Software Test Engineer, Dept. 621EDNM
- Firmware Engineer, Dept. 609EDNM
- ASIC Design Engineer, Dept. 630EDNM
- Mechanical Design Engineer, Dept. 614EDNM
- Read/Write Engineer, Dept. 617EDNM
- PCB Electrical Engineer, Dept. 629EDNM

**Manufacturing Engineering**
- Manufacturing Engineer-Test Equipment, Dept. 633MEEDNM
- Commodity Engineering Manager, Dept. 466EDNM

**Quality**
- Failure Analysis Engineer, Dept. 553EDNM
- Reliability Engineer, Dept. 552EDNM
- Field Product Assurance Engineer, Dept. 558EDNM

Still up in the air?

Maybe you should know about the great benefits at Quantum. Like profit sharing and stock options. Plus friendly, supportive people and new facilities currently under construction. To find out more, send your resume, indicating the appropriate department code, to: Quantum Corporation, Human Resources, 1804 McCarthy Blvd., Milpitas, CA 95035; or fax it to (408) 922-0611. We are an equal opportunity employer. Principals only, please.

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**CAREER OPPORTUNITIES**

**1991 Recruitment Editorial Calendar**

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<tr>
<td>Edition</td>
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<td>Computer Peripherals • Fiber Optics</td>
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<td>CAE • Software • Digital/Analog CAE • Time Analysis, ASICs</td>
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<td>Apr. 11</td>
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<tr>
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<td>Analog Technology Special Issue, ICs &amp; Semiconductors, Test &amp; Measurement, CAE, Power Sources</td>
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<tr>
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<td>Software, ICs &amp; Semiconductors, High Speed Memory Technology • Computer Bus Boards</td>
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</tbody>
</table>

Call today for information on Recruitment Advertising:

East Coast: Janet O. Penn (201) 228-8610
West Coast: Nancy Olbers (603) 436-7565
National: Roberta Renard (201) 228-8602

[EDN logo]

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EDN February 4, 1991
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Honeywell in Phoenix offers a variety of career opportunities in our Commercial Flight Systems Group. Our continuing growth has created the following positions:

Systems Design Engineer — In this area, you will be involved in guidance and control systems analysis and hardware/software design trade-offs. Specification designs, including guidance, navigation and control algorithm development, as well as systems integration and installation, flight test and customer liaison activity, are a part of these positions.

System Software Development — This area involves development of flight software for advanced guidance and control systems for aircraft using modular and structured programming techniques. You will be involved with algorithms and development of real-time programs in both assembly (8086 family Z8002, 68000) and high order languages such as Pascal, "C," Ada and PLM/86, with subsequent hardware integration.

Electronics Engineering — These positions involve the development of new processor/bus architectures and specifications to support fault tolerant/redundant airborne applications.

Display Systems — These positions offer systems, software and hardware opportunities with CRT/LCD display technology. You should be familiar with digital hardware design and/or real-time programming. Systems functions include overall system definition, design and customer interaction.

To qualify for the positions listed above, you should have a BSEE or a BSCS degree and at least three years of experience.

Quality Engineering — To qualify for this position, you should have a BS degree in an engineering curriculum. A minimum of two to five years of experience in quality engineering/assurance, reliability and/or product engineering is required. You should have computer applications experience. Customer interface experience is preferred.

Additional opportunities are available in:
- CRT/LCD Display Technology
- Avionics Systems Simulation
- CAE Engineering (Apollo Mentor Systems)
- Artificial Intelligence
- VAX Systems Administration
- Fiber Optic Pressure Sensors
- EMI/HERF
- Software Tools Development

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U.S. citizenship required for some positions
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- Controller firmware
- SCSI experience preferred

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- BSME
- 3-5 years experience in electromagnetic/electromechanical devices
- Disk drive industry experience preferred

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- 3 years experience in the disk drive industry
- Prefer digital signal processing, adaptive servo, and feedforward servo background

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- Conduct special projects and studies for R&D and provide analyses and reports

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- West Coast: Nancy Olbers (603) 436-7565
- National: Roberta Renard (201) 228-8602

EDN February 4, 1991
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Mike Paradis  
Personnel Manager  
HTS

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EDN Magazine Edition  
News Edition  
A Partnership in Power and Prestige Worldwide.
EDN Databank

Professional Profile

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- Service is nationwide. You'll be considered for openings across the U.S. by PSL and its affiliated offices.
- Your identity is protected. Your resume is carefully screened to be sure it will not be sent to your company or parent organization.
- Your background and career objectives will periodically be reviewed with you by a PSL professional placement person.

We hope you're happy in your current position. At the same time, chances are there is an ideal job you'd prefer if you knew about it. That's why it makes sense for you to register with the EDN Databank. To do so, just mail the completed form below, along with a copy of your resume, to: Placement Services, Ltd., Inc.

| IDENTITY |
| Present or Most Recent Employer |

<table>
<thead>
<tr>
<th>Name</th>
<th>Parent Company</th>
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<tr>
<th>Home Address</th>
<th>Parent Company</th>
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<table>
<thead>
<tr>
<th>City</th>
<th>State</th>
<th>Zip</th>
<th>Location (City, State)</th>
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<tr>
<th>Home Phone (include area code)</th>
<th>Business Phone if O.K. to use</th>
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<tr>
<th>EDUCATION</th>
<th>Major Field</th>
<th>GPA</th>
<th>Year Degree Earned</th>
<th>College or University</th>
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<td>Degrees (List)</td>
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<th>POSITION DESIRED</th>
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| PRESENT OR MOST RECENT EMPLOYER |

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<th>Present or Most Recent Position</th>
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<th>Title</th>
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Duties and Accomplishments: Industry of Current Employer:

Reason for Change:

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<th>PREVIOUS POSITION:</th>
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<table>
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<tr>
<th>Job Title</th>
<th>Employer</th>
<th>From</th>
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<th>City</th>
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Division: Type of Industry: Salary:

Duties and Accomplishments:

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<tr>
<th>COMPENSATION / PERSONAL INFORMATION</th>
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<tr>
<th>Years Experience</th>
<th>Base Salary</th>
<th>Commission</th>
<th>Bonus</th>
<th>Total Compensation</th>
<th>Asking Compensation</th>
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<tr>
<th>Date Available</th>
<th>I Will Travel</th>
<th>Light</th>
<th>Moderate</th>
<th>Heavy</th>
<th>I own my home. How long?</th>
<th>Rent my home/apt.</th>
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<th>Employment Status</th>
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<th>Unemployed</th>
<th>Married</th>
<th>Single</th>
<th>Height</th>
<th>Weight</th>
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Level of Security Clearance:

<table>
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<tr>
<th>U.S. Citizen</th>
<th>Non-U.S. Citizen</th>
<th>My Identity may be released to:</th>
<th>Any employer</th>
<th>All but present employer</th>
</tr>
</thead>
<tbody>
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WILL RELOCATE: WILL NOT RELOCATE: OTHER:
Shocking news? We don’t think so. All right, maybe the White Sox won’t win the World Series. But U.S. industry can maintain its world leadership.

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Jacob Javits Convention Center
New York, N.Y.

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