Design and test engineers alter roles to facilitate test

IC vendors integrate PC telecommunication services

Mezzanine buses gain respect, find new uses
You’ll find Synergy products built into the world’s most demanding applications.

The Goal:
Design the world’s only multi-frequency Radar Target Generator System able to simulate hostile threats on the military’s diverse radar systems.

The Problem:
To get the needed horsepower, sixteen 68040 CPU boards were required. However, with this many boards, VMEbus bandwidth limits would severely degrade system performance making the project unfeasible.

The Solution:
Synergy’s V420 dual 68040 SBC. After evaluating several products, KOR Electronics selected eight V420s which could deliver 320 MIPS without VMEbus bandwidth degradation.

“Not only did we meet our project performance goals, we were able to reduce our costs by 40%.”

Unexpected Benefits:
Synergy’s dual ’040 solution cut KOR’s hardware requirements by 50% while vastly increasing system reliability. These unexpected benefits reduced system costs by 40%.

In Synergy, KOR also found a design partner with strong integration expertise and dependable customer support.

“I recommend you call Synergy today.”

Next time you need high performance SBCs, do as KOR Electronics did. Call Synergy Microsystems. You’ll be as satisfied as they are.

SYNERGY MICROSYSTEMS, Inc. 179 Calle Magdalena, Encinitas, CA 92024, 619-753-2191, Fax 619-753-0903
It's the innovative application of cutting-edge technology to your specific requirements. It's what we do at Electronic Solutions.

There was a time when a backplane was little more than a few connectors mounted to a simple pc board. But today's higher performance systems require higher performance multilayer backplanes. Someone has to resolve the difficult issues faced in designing a backplane that will handle your high-speed system—a balancing act between design parameters that affect crosstalk, reflections, impedance, ground shift, and power distribution.

That's where Electronic Solutions can make your job easier! You can rely on our experience and expertise to resolve the design issues you're facing quickly—at a price that even your bean counters will be pleased with.

For industry standard backplanes such as VME, Multibus I or II, Sun, VXI, or Futurebus+ we have a line of high performance backplanes available off the shelf. Our backplanes have been independently tested and ranked as the "Best Balanced" backplanes available.

For proprietary backplanes, no matter how exotic or unusual, we'll apply the same design expertise exemplified by our standard products and build you a backplane tailored to your specific requirements.

Let us prove it to you! Just call and request information on our backplane design capabilities and we'll FAX the FACTS right to you. Or ask to talk to one of our Applications Engineers who will help you translate your requirements into a backplane spec.

For standard or proprietary applications, there's only one way to get a backplane that's just right for your system. That's to call Electronic Solutions and put our experience to work for you.

One example of our design innovation is our patented Active Automatic Daisy Chaining, which eliminates the number one field service problem—improperly placed Bus Grant Jumpers. It's superior to the passive auto-daisy chaining touted by other vendors, and it's available free of charge on our new VME backplanes.

One example of our design innovation is our patented Active Automatic Daisy Chaining, which eliminates the number one field service problem—improperly placed Bus Grant Jumpers. It's superior to the passive auto-daisy chaining touted by other vendors, and it's available free of charge on our new VME backplanes.
The New Dual '040 VME SBC: Faster, More Efficient and Lower Cost Than Any Multi-board Solution

Get on-board multiprocessing and an astounding 40 MIPS throughput, when you power your system with Synergy’s new SV420 single-slot SBC. The SV420’s dual-CPU design means you’ll need fewer boards in your VME chassis, with no VMEbus bandwidth bottlenecks between the '040s, and system-wide cost saving of more than 40%.

And even if you don’t need multiprocessing right now, the SV420 still puts you out front. Use the second '040 as a super-smart DMA controller. When combined with the SV420's 66 MByte/sec VME64® circuitry, nothing communicates faster over the VMEbus.

Add even more on-board power by selecting from Synergy’s big list of high-performance, intelligent plug-on I/O modules – such as our latest Super-VSB module offering 40+ MB/sec over the VSB bus.

Or choose another module, from a T1/E1 controller to a super-fast graphics engine, that plugs onto any Synergy SBC.

Better yet, just tell us what you need. We’re the company you can talk to about your VME system design problems. You’ll find that we listen and deliver (every Synergy I/O module on our list started as a customer request). We mean business when we say customer support is our most important mission.

So if you want to be out front in system performance, just be up front with Synergy. Call us today.
Designers are assuming new roles to facilitate test just as Mozart's young rogues changed roles to test the steadfastness of their "true" loves.

Illustration by Bill Morrison

Editorial 14
Advertiser Index 127

WITH THIS ISSUE

Computer Design's new OEM Integration supplement debuts this month and is being mailed with this issue. If someone has walked off with it, call (508) 392-2124 for another copy.

NEWS BRIEFS

TECHNOLOGY DIRECTIONS

CAE/CAD Tools
EDA and test vendors forge alliances to promote standards.

Computers & Subsystems
2,000-Mips PC rescues high-end applications.

Software & Development Tools
Integrated tool environment targets real-time development.

Integrated Circuits
Powerline spread-spectrum modulation saves copper in LANs and control systems.

ASICs & ASIC Design Tools
Vendors vying for FPGA market try different strategies.

NEW PRODUCT DEVELOPMENTS

Software & Development Tools
Programming tool integrates functions of UNIX utilities.
Lite emulator does heavy duty.

CAE/CAD Design Tools
Mixed-signal simulator features high speed, capacity and convergence.

Integrated Circuits
Disk drive controllers automate SCSI and AT interfaces.
12-bit A-D converter outputs RS-232.

ASICs & ASIC Design Tools
Prototyping system emulates up to six million gates.

CONTINUED ON PAGE 5
Introducing HMI Lite, the brilliant breakthrough in high-performance, highly affordable development tools.

Our new Lite quietly begins a whole new era in emulation and debugging tools. Because at under $5,000, the Lite delivers more capabilities than you ever imagined possible in its price range.

First, the price includes a complete, full-featured, real-time emulator integrated with HMI’s popular SourceGate emulator control and debugging software.

Now, check these features: multiple hardware and software breakpoints, full trace capability including show cycles and dequeuing of prefetched pipelined instructions, and support for all Port-E configurations.

And, the 256K emulator RAM features complete mapping control including all chip select signals and dynamic bus sizing for 8/16 bit operations. In addition, dual ported RAM is provided for real-time monitoring of critical memory variables.

Oh yes, and this is all packaged in a single 4.5 x 1.5 inch direct-plug pod enclosure.

Write or call for details on the Lite, it supports all industry C, PASCAL and Ada compilers and is ready for use with IBM PC family and UNIX based host computers. The new Lite is the best of our emulation technology—for less. Brilliant!

HUNTSVILLE MICROSYSTEMS, INC.
3322 South Memorial Parkway
Huntsville, AL 35801 USA.
Tel: (205) 881-6005
Fax: (205) 882-6701

IBM is reg. T.M. International Business Machines, Inc.
UNIX is reg. T.M., Bell Laboratories, Inc.
IC vendors integrate PC telecommunication services
First came fax-modem combo chips. Now IC manufacturers are attempting to integrate voice messaging and caller ID. They’re thinking about color fax and video conferencing. Are there limits beyond which the technology envelope can’t be stretched? — Stephan Ohr

Mezzanine buses gain respect, find new uses
High-density chips and chip sets are bringing more and more functionality to a single board, often reducing system bus requirements. This opens the way for mezzanine boards, not only to increase available board real estate, but to become an integral part of the system architecture—in some cases to the exclusion of system buses. — Warren Andrews

Design and test engineers alter roles to facilitate test
Time is running out for silicon, circuit board and system houses who haven’t taken design-for-test seriously. Old test methods are fast becoming inadequate, while the next generation of systems is waiting in the wings. — Mike Donlin

Event-driven strategy wins for robot test handler
Engineers at Taltec, working with a customer to develop a robotic pick-and-place machine, saw an opportunity to craft their own system platform, and ended up in the tester/handler business.— Jeffrey Child

Trace issues drive 32-bit emulator choice
For integrating hardware with software, as well as hunting down the nastiest bugs in your real-time microprocessor-based design, there’s no more effective tool than an emulator. — Jeffrey Child

MIXED-SIGNAL DESIGN — Stephan Ohr
Are automobiles the proving ground for the next generation of electronics?
No logic analyzer is, for that matter.

Because at speeds above 25 MHz, even the best designer needs a scope to handle nightmares like race conditions, ground bounce, and crosstalk. And not just any scope, but one tailored specifically for high-speed digital design.

At Tektronix, we understand this need all too well. As proof, we’ve not only designed and built a great logic analyzer — our powerful new GPX — but also a perfect companion. The TDS 640 digitizing oscilloscope.

To get you started, the GPX provides more channels than cable TV. Up to 160, for instance, of 80 MHz state analysis, and 32 channels of 1 GHz timing or 160 channels of 200 MHz transitional timing.

In short, enough to handle the world’s fastest microprocessors. And with that kind of performance, you can easily track your system at clock rates well beyond 50 MHz, which allows you to locate complex coding errors quickly and accurately.
Enter the TDS 640.

With a 500 MHz bandwidth and 2 GS/s real-time sampling on four channels, the TDS displays logic and timing errors with absolute accuracy. And because it was created with the digital designer in mind, the TDS lets you trigger directly on common digital circuit events like glitches, runt pulses, and excessive clock jitter or skew. Put all that together with the power of the GPX and you have a remarkably effective solution.

Cost effective, too. In fact, the GPX and TDS together sell for less than competing scope/logic analyzer combinations. And if you buy the pair between now and February 28, 1993, we’ll take an additional 10% off the retail price.

Enough, already.

Analyzer Is Great For It’s Not Nearly Enough.

For more information on the very best high-speed digital design tools available, call Tektronix today at 800-426-2200.
This is your chance to get the full power of embedded
SPARC. Don’t let it slip away.

This is one of those times when you just have to seize the day. Because opportunities like this are rare indeed.

You see, FORCE is the only company licensed by Sun to put SPARCstation 2 technology on VME.

So we’re the only ones who can give you validated hardware and software compatibility. Allowing you to run SunOS™ with any of your SPARCstation 2 applications and peripherals. Without a hitch.

We also have a whole new family of SPARC 2 products. With everything from our CPU-2CE (6U) board to the microforce single-slot system.

We even have 20-slot systems that allow you to customize I/O. Giving you the perfect combination of real-time and UNIX.

And our SPARC products provide the broadest software offering of any RISC architecture. Including SunOS, real-time operating systems and a host of application software.

So if you want a better grasp of embedded SPARC, call for a free brochure. 800-237-8863, ext.5. Or in Europe, 49.89.608-14-0.

Because there’s no reason to let all this power slip through your fingers.
HP joins open-standards revolution

Last month Hewlett-Packard (Fort Collins, CO) jumped into the real-time, open-bus business with a vengeance when it introduced the 742m. This full-featured CPU carries HP's 50-MHz PA-RISC 7100 processor with floating-point coprocessor. The new board is designed to run the HP-RT 1.0 real-time POSIX-based operating system, and is closing in on 60 SPECmarks.

The board, however, is but one of HP's forays into the open-systems, real-time arena. It's also introducing an entire family of industrial workstations based on VMEbus. The family will be part of the HP Apollo 9000 Series 700 workstations, targeted at the manufacturing, aerospace, telecommunications, and medical and laboratory industries.

The new products are designed to let OEMs, system integrators and users increase performance with HP's PA-RISC architecture and software development tools. Board products are compatible with the company's other workstations. In making its announcement, HP becomes the second major maker of minicomputers to jump on the VMEbus bandwagon for real-time applications. Last year, Digital Equipment Corporation (Maynard, MA) announced that it would focus on the real-time market, using VMEbus with its Alpha processor architecture. At the time, it announced an agreement with Wind River Systems (Alameda, CA), in which that company would port its VxWorks to Digital's new family of products and integrate Alpha into its existing real-time OS.

Both HP and Digital have traditionally had heavy stakes in the real-time business—HP with its 1000-series minicomputers and Digital with its PDP machines. Both, however, were in jeopardy of losing out to more flexible, standard-bus-based machines. Despite rumors to the contrary, Digital's project leader, Maureen Johnson, reports that the company's VMEbus-based project is on schedule.

Antsy for ANSI

VITA (VME International Trade Association—Scottsdale, AZ) has submitted an application to ANSI to become a standards sponsoring group. The group's objective is to provide a more comprehensive vehicle for the VMEbus specification.

VITA's application is currently going through the approval process at ANSI, a process that's expected to be completed early next year. It's expected that once VITA achieves sponsorship status, it will write a revised VMEbus specification divorced from the present 1014 Revision C, and probably also from the proposed Revision D, which adds VME64 to Revision C.

A new VMEbus specification is expected to emerge in place of these documents, one with SBBLT and all the new timing parameters it mandates. It will also include most of the features discussed for Revision D but not included in that document. In addition, it may include similar features for both 3U and 6U, as well as multiplexed P1 signals to give 3U VME 32-bit SBBLT performance.

VITA's ANSI application has a few people in the IEEE upset. "Most of the rock throwing is over now," says Ray Alderman, VITA's technical director. "It's now down to a few substantive issues, which we hope will be resolved soon." But it's an open question as to whether or not VITA's move will result in an exodus of standards from the IEEE. At this time, VITA, which represents both Futurebus+ and VME, isn't planning to move the Futurebus+ specification to ANSI.

Mentor Graphics opens six top-down design centers

To reduce the risk to users of transitioning from gate-level to top-down design, Mentor Graphics (Wilsonville, OR) has just opened half a dozen design centers, staffed with its own senior ASIC designers and equipped with Sun SPARC workstations. The centers are located in Boston, Dallas, Denver, Munich, San Jose, and Tokyo. Later this month Mentor will begin a worldwide training program called SmartStart, which covers software, hardware, silicon fabrication, and support services.

To make vendor support available to SmartStart participants, Mentor has initially teamed up with Sun Microsystems and ASIC vendors Fujitsu, LSI Logic, Mitsubishi, and VLSI Technology, as well as FPGA vendor Xilinx. "Mentor Graphics wants to partner with companies that are doing the most difficult, leading-edge ASIC designs," says Dan Ganousis, manager of Mentor's ASIC Design Center program.

Training for SmartStart participants will include seminars, workshops, VHDL language training, and on-site consulting services. During the training, customers will actively participate in taking a design from VHDL to layout through actual hands-on experience.

Continued on page 12
46% BOARD SAVINGS
IDT's new 16-, 18-, and 20-bit Double-Density FCT-T Logic family offers the performance of two octal logic devices in one flow-through 48- or 56-pin high-density, JEDEC-standard, shrink small outline package (SSOP) or Cerpack, for twice the functionality in half the board space.

A WIDEBUS™ UPGRADE
IDT's Double-Density logic family is more than twice as fast as ACT, uses 35% less power than ABT, and it's form-, fit-, and function-compatible with both of TI's Widebus families. The Double-Density family also offers typical pin-to-pin skew of 250ps and quiescent supply current at 0.05mA (typ.).

3 APPLICATION CHOICES
5V High Output Drive
Ideal for low-impedance bus and backplane applications.

5V Balanced Drive (Low Noise)
Contains on-chip, source-terminating resistors to minimize signal noise. These devices are ideal for driving point-to-point transmission lines and highly capacitive loads, such as a bank of DRAMS or SRAMS.

3.3V Low-Power Logic
Designed for regulated or unregulated 3.3V power supplies, these devices use less power than 5V parts, without sacrificing high speed. 5V-to-3.3V unidirectional and bidirectional translators are also available.

FREE SAMPLES
Call today for free samples and a copy of the new High-Performance Logic Data Book and start your Double-Density logic design today!

(800) 345-7015 • FAX: 408-492-8674
ASK FOR KIT CODE 3071

CIRCLE NO. 7
Alfa fab registered for ISO 9000

Digital Equipment Corporation (Hudson, MA) has announced that its semiconductor fab there has been registered to the International Organization for Standardization (ISO) standard 9002. The Hudson site is one of two Digital facilities manufacturing the 200-MHz Alpha AXP family of RISC microprocessors, the world’s fastest 64-bit chips.

The ISO-9000 series of quality assurance standards is becoming a prerequisite for conducting business in Europe and other parts of the world. In contrast to the Malcolm Baldrige Award for Quality, ISO 9000 is an ongoing certification rather than a one-time award. ISO-9000 registration requires adherence to strict guidelines and comprehensive auditing by a qualified outside agency. The accredited agency that registered the Digital facility is the Quality Management Institute. With the Hudson registration, all four of Digital’s semiconductor fabs are ISO-9002 qualified. The ISO 9002 is the second-highest level of ISO-9000 qualification. Digital is among a small group of IC manufacturers that’s registered for ISO 9000.

More manufacturers are expected to follow in Digital’s footsteps now that companies such as AT&T, Hewlett-Packard and IBM are requiring their suppliers to move toward ISO-9000 certification.

Dual use the watchword as defense pares down

With military budgets feeling the pinch due to recession and relaxing world tensions, defense contractors are looking to develop products that can be used in both the military and civilian sectors. They’re also more actively marketing products developed for the military into civilian applications. A case in point is Loral Defense Systems (Akron, OH), which is offering a high-speed parallel/associative computer, originally developed for use in airborne warning and control systems (AWACS), for use in VME-based workstations.

The ASPRO-VME is a single-instruction, multiple-data (SIMD) associative computer that finds data by content, not address. It can be built up in modules of 512 processors to a total of 8,192 processors, and can perform between 150 Mflops and 2.4 GFlops. The military uses the ASPRO-VME primarily for target correlation and tracking, image processing and tactical decision support. More general civilian applications include image processing, signal processing, associative database management, artificial intelligence, and neural networks.

—Tom Williams

Pact to provide real-time UNIX for Intel computers

The Santa Cruz Operation (SCO—Santa Cruz, CA), a leading supplier of UNIX for PC's, has joined forces with Chorus Systems (Paris, France) to produce a real-time version of UNIX for Intel-based computers. The real-time aspects of the system will leverage off Chorus microkernel technology, which it embodies in its Chorus MII product. SCO will contribute its 386/486-based SCO UNIX and its SCO Open Desktop X-Window-based GUI.

Initial plans call for the new product to be targeted at real-time applications in telecommunications, point-of-sale, and process and manufacturing control, as well as testing and simulation. Given the compact size of the Chorus microkernel, the system should be easily portable to smaller, single-board embedded systems as well. SCO’s alliance with Chorus could also be a counter to the threat posed by Sun Microsystems, whose Solaris version of UNIX is poised to invade the Intel-based arena now dominated by SCO. To date, Solaris does not have real-time capabilities.

—Tom Williams

MCMs still waiting in the wings

At the recent International Electronic Packaging Society Conference (Austin, TX), multichip modules (MCMs) attracted the usual group of curiosity seekers, but didn’t prove they can garner design wins. Despite predictions that the fledgling technology is poised to become a dominant component of next-generation systems, many designers deem MCMs as either too expensive or too risky to become anything but fodder for technical papers. But AT&T Bell Laboratories (Murray Hill, NJ) hopes to extricate MCMs from this quagmire by incorporating them into its next-generation of telephone products.

AT&T is predicting that volume could run up to 500,000 MCMs per year—a figure that may be greater than the sum total of MCMs produced this year. Although AT&T hasn’t committed to volume production of MCMs as yet, the company is currently doing feasibility studies of the technology at its manufacturing plants in Kansas City, MO and Shreveport, LA.

—Mike Donlin

Neural network uses 3-D stacking technology

Irvine Semiconductor (Costa Mesa, CA) is using its 3-D chip-stacking technology and flip-chip bonding methods to develop a multiple-layered neural network device. Dubbed the neural conditioning module (NCM), the device will be able to recognize and abstract features from a focal plane array. According to Irvine, the module’s highly parallel architecture and processing power could be combined with next-generation artificial intelligence software to produce a system that could truly emulate the human brain, when prototypes are completed in about two years.

The module hosts a 128 x 128 detector array that is bump-bonded to a laminated cube using flip-chip technology. Another chip, the lateral resistive layer, is bump-bonded to the NCM, and contains an array of addressable and variable resistances. Signals processed by the device are sent through a crossbar switch that effectively connects the 128 inputs through seven layers of processing nodes to 128 outputs. Irvine spokesmen say the module will result in a new class of smart sensors that can operate on a real-time basis for military and commercial applications.

—Mike Donlin
Open up to Mercury's embedded realtime multicomputer solutions. Because of a balanced architecture, our multicomputers deliver scalable performance into the tens of GFLOPS, with GBytes of I/O to match. With interboard and interchassis communications, you can build a solution to satisfy even the most demanding applications within your constraints of cost, space, and power consumption.

Mercury's commercial and ruggedized multicomputers are supported by our standards-based realtime operating system software, including advanced multicomputing development tools that enable you to harness the power of hundreds of processors.

For more information on our commercial off-the-shelf (COTS) products and to receive our White Paper: Balancing I/O and Computation, call Mercury toll free today at 1-800-229-2006 or (508) 458-3100.
Keeping track of change

Many technical articles today are peppered with phrases such as “top-down design,” “designing for testability,” “over-the-wall methodologies,” and “concurrent engineering.” The use of this verbal shorthand is often justifiable, because the topics under discussion are complex, but overuse can water down these terms and diminish their effect. This is unfortunate, because the concepts behind them are all valid.

We hear from many sources that the way the electronics industry operates must change. Engineers in the insulated worlds of design, test and manufacturing are discovering that precious time is lost and quality is sacrificed when each group must modify the work of the others to get a product out the door. We’re told that engineers from each of these disciplines must work concurrently on a project, with the needs of all considered as early as possible in the design cycle. Still, we have to wonder, are these changes really taking place, or is everyone just giving lip service to change while staying stubbornly bound to the old ways? Are semiconductor, circuit board and system houses really trying to design their products with testability and manufacturability in mind? Are the walls that have separated different departments really crumbling? Will engineers and managers accept the ramifications that these changes portend?

Here at Computer Design, we’re as anxious to know the answers to these questions as you are. It’s senseless for us to churn out articles about trends that don’t exist, but it’s equally senseless for us to ignore real trends because we’ve become cynical about the electronics industry’s ability to embrace teamwork concepts. So, starting in January, we’ll be featuring a column called “Tools and Techniques,” which will try to answer these and other questions about the changing face of our industry. I’ll be spearheading the effort, and my fellow editors will be stepping in from time to time to examine the same trends in their respective beats—buses and boards, integrated circuits, ASICs, and software. But we need your help.

We’re looking for input from our readers, vendors and users alike, to help us keep the column in focus. We’d like to hear your opinions about the changes taking place in design, test and manufacturing. We want to track the transition of the designer from rugged individualist to team player. We need to know if those of you in management support these trends, or if you’re leery of changes that could poison morale and derail productivity. So give me a call at (508) 392-2123, and let me hear your side of the story. With your help, Computer Design can chart what promises to be an interesting journey for us all.
SERIAL EEPROMs:
ALL SHAPES, ALL SIZES,
ALL 1.8 VOLTS

Atmel makes every key serial-interface EEPROM in the market today. And, we'll make tomorrow's. That's every configuration, every density, every package. We're the world's broadest supplier.

Our 1.8-volt serials will cut your power needs by 80 percent. They're perfect for anything portable or anything that uses batteries. (We make 5-volt serials too.)

We don't wear out easily. We guarantee 100,000 write cycles, tenfold more than most. And for just a little more we'll guarantee one million.

Because of our manufacturing expertise, we are price competitive. Really competitive. We own a state-of-the-art U. S. fab, and are the industry leader in EEPROMs. We know what we're doing and pass it on in a form that every purchasing agent loves.

So, if you're using serial EEPROMs, think about Atmel—we make them all. And, if you give us a call, we'll send you a few to try.
LIVE LONGER AND PROSPER

With more run time, the new HYDRITECH™ nickel hydride battery is significantly increasing the lives of portable computers and their consumer appeal. HYDRITECH offers 25% more power than the best nickel cadmium battery. It gives users hours more work time without recharging. Plus, HYDRITECH's enhanced performance also allows you to add more features and design a lighter, smaller product. All with one hour charge capability. And it's environmentally preferred. Gates Energy Products is the only company that has a full line of nickel hydride batteries and unparalleled assistance to apply this new technology to your designs. So, if you're interested in portable computers with more run time and more sales potential, live longer and prosper with HYDRITECH. Call Gates Energy at 1-800-67-POWER today.

THE NEW HYDRITECH™ BATTERY FROM Gates Energy Products
As the demand for advanced low-power portable systems—cellular telephones and laptop, palm-size and pen-based computers—increases, the electronics and computer industries are shifting to lower-voltage ICS and ASICs. The relentless shrink in chip geometries is also a driving force, because devices made with 0.5-µm-and-under design rules will require reduced supply voltages.

Some of the larger, next-generation desktop commercial and industrial systems are also moving in this direction, but they will first be based on hybrid 3-V/5-V designs. This is an interim step designed to cope with the higher power dissipation associated with geometries that go below 1 µm—and with tomorrow's 0.5-µm geometries and their higher clock rates.

As this technology unfolds, chip vendors are bringing to market 3-V microprocessors, RAM, discrete logic, and ASIC libraries. Third-party CAE/CAD suppliers are scurrying to develop tools to handle these mixed 3-V/5-V and 3-V designs, coming in both digital and mixed-signal flavors.

Prudent designers must be wary in approaching 3-V technology. To avoid the problems they experienced at 5 V, they must be careful to check out 3-V ASIC libraries, and to look for difficulties with low-voltage ASIC designs. The predictability of low-voltage designs is directly related to ASIC cell characterization and how it's performed. The right way is to fully characterize each and every cell in a library; the wrong way involves the careless application of global derating factors.

I The right way vs the wrong way

The proper characterization of cells in a library involves two major steps. First, you select the appropriate power-supply limits so the devices in the library will operate effectively. It's within these voltage limits that the models in a cell library are expected to provide accurate simulation results. Second, each individual cell is completely characterized for delay behavior over a selected range of $V_{DD}$, input, slew rate, capacitive load, temperature, and wafer-process variations. Engineers designing with a 3-V or 5-V library can then calculate delays using a gate-level simulator and get the delay values they're expecting.

Unfortunately, silicon vendors can publish incorrect methods in order to move product quickly to eager but naive electronic systems manufacturers. One such method involves lowering the power of existing 5-V silicon to 3 V and hoping the ASIC will operate as intended. This is risky because silicon powered down to a lower voltage may exhibit different temperature characteristics or other anomalous behavior due to the change.

With limited characterization data, how can chip-level evaluations be performed accurately? And how can all the circuits in an ASIC and their critical paths be simulated or tested under all worst-case conditions?

A second incorrect approach isn't as risky, but it still doesn't work well in efficient, high-performance 3-V design. This approach uses derating factors, or the estimated average percentage by which device characteristics will change for most, or all, cells in a library. The odds of attaining favorable results aren't good with this method, because each cell derates in a slightly different way, depending on the mix of P- and N-channel devices in it.

Derating is also inaccurate because of increased gate delay, which results from a decrease in transistor gain as the operating voltage is reduced. And differences in how P- and N-channel devices are structured in different gate types cause them to derate differently and to exhibit different gate delay-vs-voltage characterizations.
teristics. In a NAND gate, for example, P-channel devices are in series and N-channel devices are in parallel. NOR gates, on the other hand, have P-channel transistors in parallel and N-channel devices in series. This variation can result in setup-time errors for different types of flip-flops or in variations in rise and fall times for different gate structures.

Such inaccuracies aren’t what systems houses expect as they start to develop new product engineering plans. Aside from wishing to deploy fully characterized libraries, they’ll want to keep virtually the same design routines they’ve used in the past, so the same terms and conditions that exist for 5-V ASIC design must be maintained for 3-V design.

Welcome, analog

The same holds true for analog functions, but with an additional challenge—many digital designers view analog design as an arcane art form characterized by its complexity and unpredictability. It’s clear that the challenge is to make analog features and functions as robust and predictable as the digital features and functions with which designers are familiar.

Full characterization of 3-V analog cells must, therefore, be based on procedures similar to those used for 3-V digital cells. But unlike improperly recharacterized or derated digital cells, which can still function, improperly characterized analog cells won’t work at all. This is because analog cells require precise accuracy; there’s no middle ground, no compromise and certainly no room for estimates.

Analog cell performance springs from three processes: transistor modeling, simulation and post-silicon design tolerance evaluation. First, you need state-of-the-art MOSFET modeling to get the best representation of the performance of an analog circuit via simulation. It’s particularly important to base a model on a single equation for the triode region, saturation and subthreshold regions of a transistor. Other models use separate equations for each of these regions, but, as a consequence, accuracy of simulation suffers.

There are linear equations for the triode region; other equations cover saturation; and a third group of exponential equations applies to the subthreshold region. As a result, adverse effects known as kinks and glitches occur in the transistor source drain current, transconductance and output conductances at the boundaries between regions. Distortion is created as a consequence. These kinks and glitches also lead to reduced predictability in a model and in the real analog circuitry, so the device might not perform as expected and possibly will fail completely.

An important step in building the accurate models needed for proper analog cell characterization and simulation is extraction of detailed parasitic information from the physical transistor layout and the use of this information in transistor-level analysis to ensure accurate simulation. This information includes transistor sizes, routing capacitances, internode coupling capacitances, and sizes of the parasitic diodes.

The third and final step in producing a high-performance analog cell is taken during the silicon fabrication process. Design tolerance evaluation (DTE) is an integral part of that process; it involves analyzing large groups of finished silicon wafers that represent best-case (fast-device), nominal and worst-case (slow-device) scenarios with various parasitic loadings. DTE is accomplished by controlling the variation of such parameters as channel length, channel width, gate oxide, and dielectric thicknesses. After the devices are fabricated, samples from different process categories are characterized to generate an accurate set of specifications covering extremes of processing, voltage and temperature.

Architecture, signal level, specs

Gaining a good understanding of performance and accuracy criteria for analog circuitry gives designers a basis for dealing with other analog cell issues. Architectures, signal levels and specmanship, for example, have to be confronted in designing low-voltage ASICs. In a world of analog CMOS, the 5-V chip structures and circuitry that vendors have long relied upon won’t necessarily work when implemented at 3 V. Designers will also have to be cautious with signal-level specs and input ranges. There’s ample headroom on input values at 5 V, but it won’t be available at 3 V.

Specifications dealing with such parameters as linearity, resolution, operating voltage range, and temperature, moreover, will be an open question as the industry picks up speed in the 3-V mixed-signal ASIC area. We’re only now crossing the low-voltage analog threshold, but within a year specs will be coming from several directions. The questions to be asked are: Is the operating range to be 3.3 V ± 5 percent? Or ± 10 percent? Or will operating ranges be specified even lower than the de facto 3.3-V standard?

It’s important that designers understand the ways in which 3-V mixed-signal ASIC vendors specify 3-V analog blocks. They usually establish a tighter operating range for analog than for digital circuitry at the lower voltage. Some analog cells will require off-chip components to achieve higher performance, and these support devices will also need tighter specifications. A more tightly specified, and more expensive crystal, for example, will be necessary to achieve higher fre-
The right way vs the wrong way

Mixed 3-V/5-V design

One of the big pluses of mixed 3-V and 5-V design is flexibility. Traditionally, designers have had little latitude in changing a design in midstream. Once a design was begun, the best option involved selecting the most appropriate CMOS cell or macro for a specific function. Now designers can tap into both 3-V and 5-V cell libraries and use either CMOS or BiCMOS cells, depending on circuit requirements. Special CMOS cells can be dialed up and mixed and matched, even after the design is well under way. And BiCMOS drivers and buffers are especially valuable for surmounting high capacitance drive barriers.

It's a good idea, then, to abandon earlier engineering thinking and try to understand the nuances of current design practices, particularly in the areas that design managers have long taken for granted, such as layout. Historically, designers have confidently turned over their 5-V designs to silicon vendors for placement-and-routing and the subsequent steps leading to finished silicon. Mixed 3-V and 5-V design, however, introduces fresh concerns at the layout stage, such as getting optimal placement in an ASIC chip of 3-V and 5-V analog and digital cells and macros to attain a targeted performance. Other concerns include verifying on-chip 3-V/5-V interfaces; circuit partitioning to ensure that 3-V/5-V analog and digital chip portions are segmented according to a specific ASIC design and having single-pass timing calculation as part of layout to comply with time-to-market schedules. Systems houses will have to take a greater interest in this part of the cycle, since it can create new problems concerning performance and the design schedule.

To avoid such pitfalls, it's best that floorplanning tools automatically assign separate circuit sections to specific locales within the logic core. Many cell-area possibilities can quickly be checked to reveal the best topology for a given design. Floorplanning tools perform other functions as well, such as clustering similar cells to keep the number of power-supply lines to a minimum. But their most significant capability comes with layout software that can concurrently place all 3-V and 5-V cells for optimized designs. Without these tools, multiple independent placements are necessary.

Silicon vendors can help here by providing expert direction in targeting separate power-supply functions, including specifying the arrangement of power buses to 5-V and 3-V rails. Those vendors can also point out design restrictions—whether or not a group of 3-V or 5-V cells is best placed in a certain corner of the chip, for example. Layout accuracy becomes more important here, because masked inefficiencies lead to lower performance.

Inefficient layout also adversely affects the customer's design schedule, because it can create the added burden of troubleshooting. And layout problems in mixed 3-V and 5-V ASIC designs will be more difficult to track and resolve than those at traditional voltage levels, because mixed-power supply/mixed-signal layout entails more tasks and covers diverse areas where more mistakes can occur. That's especially true if silicon vendors use conventional layout tools that require much manual intervention. Unfortunately, when new problems crop up, they translate directly into time-to-market losses and aggravate the risk that latent problems will turn up at the system designer's location.

Outlook for the future

The move to 3 V will yield many system benefits, some of which remain to be discovered. For the present, we can expect extended battery life, increased reliability, reduced electromechanical interference, tighter packing densities, and—one of the biggest advantages—continuing use of low-cost plastic packaging.

The applications most readily moving to low-voltage designs are in the areas of mass storage and mobile computing, with workstation not far behind. In portable PCs, full conversion to 3-V systems will probably be accomplished by the end of next year, with traditional 5-V system implementations phased out of all portables by 1994.

Wireless communications and multimedia represent two emerging applications that will propel 3-V ASIC technology into true systems-level ICs. This will probably involve large-function DSP and communications macros, operating in tandem with other memory and logic structures in the same ASIC chip, all operating at 3 V in both digital and analog circuitry.
Increased 386 Perform

AMD's 3-Volt 386 Microprocessors Deliver
The Longest Battery Life For Portable Computing.

The power struggle continues. While you can get a 386 microprocessor that goes fast, you’ll still burn through a battery charge in a hurry. Low-voltage 386 CPUs from AMD are the answer—the Am386"SXLV and Am386DXLV microprocessors.

Here are two CPUs made not only to go fast, but to go the distance with portable computer users. Unlike common power-hungry 386s, these low-voltage CPUs run on 3 volts. And they automatically slip into a static “sleep” mode to save power whenever the processor is idle. So users depend less on recharge units—and get the longest operational battery life.

Both Am386 CPUs were designed to fit as comfortably in your budget as they do your portable computers. But you won't compromise on performance because the Am386SXLV and Am386DXLV 3-volt microprocessors both run at 25MHz. So
they're plenty powerful for running Windows."

Now there's nothing stopping you from charging forth with more efficient 3-volt laptops, notebooks, and palmtops. AMD also has your memory needs covered with our 3-volt EPROMs. And now that the industry at large has welcomed low-voltage portable computing, you'll find the rest of your components equally easy to come by.

For more information on low-voltage 386 microprocessors and support logic, call 1-800-222-9323 and ask for Literature Pack 15F. And become the current leader in portable computing.

Advanced Micro Devices
Microprocessors For The Masses.

trademark of Advanced Micro Devices. All other brand or product names are trademarks or registered trademarks of their respective holders.
AP Labs VMestation™

REAL-TIME
Integrated VME Workstation

TESTED TO MIL-STD-810E

Fully integrated systems for seamless real-time computing
- SPARC, 680X0; 860; MIPS architecture
- UNIX, Solaris/SunOS and VxWorks; C, Fortran, Ada
- Low-latency, high-performance asynchronous I/O
- Fully integrated VME I/O real-time device driver support
- Data Acquisition; Signal Processing; Telemetry; Simulation

AP Labs
6215 Ferris Square
San Diego, CA 92121
(619) 346-8626
Fax:(619) 346-0278

CIRCLE NO. 12

AVOCET SYSTEMS, INC.

<table>
<thead>
<tr>
<th>Intel</th>
<th>Motorola</th>
</tr>
</thead>
<tbody>
<tr>
<td>8051</td>
<td>680X0</td>
</tr>
<tr>
<td>8048</td>
<td>68300</td>
</tr>
<tr>
<td>8085</td>
<td>68HC11</td>
</tr>
<tr>
<td>8096</td>
<td>6800</td>
</tr>
<tr>
<td>Hitachi</td>
<td>6801</td>
</tr>
<tr>
<td>64180</td>
<td>6802</td>
</tr>
<tr>
<td>18H</td>
<td>6803</td>
</tr>
<tr>
<td>Western</td>
<td>6804</td>
</tr>
<tr>
<td>65816</td>
<td>6805</td>
</tr>
<tr>
<td>Rockwell</td>
<td>6809</td>
</tr>
<tr>
<td>6500</td>
<td>Zilog</td>
</tr>
<tr>
<td>6502</td>
<td>Z8</td>
</tr>
<tr>
<td>RCA</td>
<td>Z80</td>
</tr>
<tr>
<td>1802</td>
<td>Z180</td>
</tr>
</tbody>
</table>

C and Pascal Compilers
Simulators
Assemblers
In-Circuit Emulators
EPROM Programmers

The Source For Quality Embedded-System Tools
120 Union Street, P.O. Box 490, Rockport, ME 04856
In Maine, or outside U.S., call (207) 236-9055
TLX: 467210 Avocet Cl • FAX: (207) 236-6713
Call today:
1-800-448-8500

CIRCLE NO. 13

COMPUTER DESIGN

EDITOR-IN-CHIEF/ASSOCIATE PUBLISHER
John C. Miklosz, Ph.D., (508) 392-2114

SENIOR EDITORS
Warren Andrews, Computers & Subsystems
(508) 283-2102
Barbara Tuck, ASICs & ASIC Dicgn Tools
(516) 473-1661
Michael G. Donlin, CAE/CAD Tools
(508) 392-2123
Tom Williams, Software & Development Tools
(408) 335-5514
Don Tutte, Integrated Circuits
(415) 365-5656
Jeffrey Child, New Product Developments
(508) 392-2126

CONTRIBUTING EDITOR
Stephen Oeh, Analog & Mixed-Signal
(908) 232-1389

OEM INTEGRATION
Senior Editors
John Mayer, Technology & Product News
(617) 484-5804
Frank Caruthers, Special Reports
(215) 993-9595

MANAGING EDITOR:
Alyn S. Powell, Jr.

CHIEF COPY EDITOR:
Annette M. Storr-Wilson

COPY EDITOR:
Kym Wilson Gilhooly

PRESENTATION MANAGER:
Richard Sarno

EDITORIAL ASSISTANT:
Clare Ellis

ART DIRECTOR: Ian Horner

AD TRAFFIC MANAGER:
Kelly Rice, (508) 392-2198

CIRCULATION DIRECTOR:
Robert P. Dromgoole, (918) 832-9213

CIRCULATION MANAGER:
Paul Westervelt, (918) 832-9287

PUBLISHER
David I. Allen, (508) 392-2111

ASSOCIATE PUBLISHER/NATIONAL SALES MANAGER:
Tim L. Tobeck, (508) 392-2116

PennWell PUBLISHING COMPANY

Advanced Technology Group
Dr. Morris R. Levitt, Senior Vice-President
Leslie P. Cypret, Vice-President, Administration
One Technology Park Drive
P.O. Box 990, Westford, MA 01886
Tel: (508) 692-0700 • Fax: (508) 692-0525
Postmaster: Send change of address form 3579 to COMPUTER DESIGN Circulation Department,
Box 3466, Tulsa, OK 74101

ATTENTION RETAILERS: To carry Computer Design
in your store, contact International Periodical
s Distributors at 1-800-999-1170, ext. 447 (dealer calls only).

CIRCLE NO. 12
When the other guys claim they have DSP for multimedia, shoot a few questions at them.
Can I differentiate my product?

Is it affordable?

Is it available?
The other guys call it DSP for multimedia, and say it's on the way. We call it Signal Computing, and it's here and now. In fact, leading companies like Olivetti and Siemens have already incorporated Signal Computing components into their latest products.

Signal Computing integrates three interchangeable and extensible silicon and software capabilities: a multi-purpose signal processor, sigma-delta signal port ICs, and algorithm software from Independent Algorithm Vendors (IAVs) who provide expertise in real-world media like sound, video, speech, music and communications.

Signal Computing provides an open architecture that allows you to create value-added differentiation for your computer, communications or consumer products. Toolkits allow you to easily customize Signal Computing solutions. Multiple data types can be mixed and matched on the same low cost platform. And because Signal Computing has attracted algorithm and hardware specialists worldwide, your options will not be constrained by proprietary solutions developed or supported by a small set of vendors.

Signal Computing is affordable for both coprocessing and embedded applications.

A complete V.32bis fax/data modem solution has already been introduced, priced at just $25. Perfect for mass market applications. And IAVs are already delivering algorithms for speech recognition, text-to-speech conversion, music synthesis, still image compression, audio compression and Dolby® AC-2 digital audio.

In today's market, you have to be quick on the draw. We can help you differentiate your product right now. So check out the other guys' claims. The more you know, the more you'll understand why Signal Computing is the right solution. To learn more, call 617-461-3771, or write us at the address below.
All TME products come with Two Serial ports, One Bidirectional Parallel port, Floppy & IDE Hard Disk Interfaces.

- HQP486
  - 20/25/33/50Mhz, 80486/SX/DX
  - Up to 48Mbytes on-board memory
  - Optional 256K write back cache memory

- HQP386C
  - 25/33/40Mhz, 80386SX
  - Up to 32Mbytes on-board memory, 128K write back cache memory

- HQP386SX
  - 16/20/25Mhz, 80386SX
  - Up to 16Mbytes on-board memory, 64K cache memory
  - Up to 1.5Mbytes FLASH EPROM on-board

- RTMX/BN
- RTMX/XX
  - Based on Sun OS Library
  - Complete POSIX
  - SVID 3.0 Compliant
  - Full Networking with TCP/IP and OSI Support
  - BSD4.3 Socket Library

TME
Toronto MicroElectronics Inc.
1848 Bonhill Rd. #1 Mississauga, Ontario, L5T-1C4
CANADA
Tel: 416 564-4833 • Fax: 416 564-4768

CIRCLE NO. 16

RealTime, Multi-platform POSIX Operating System

- Realtime fixed priority tasking
- Derived from Berkeley BSD NET/2
- POSIX 1003.1 Compliant
- Source Compatible with Sun OS

RTMX is standardized. POSIX compliance assures consistent, portable code for now and for the future. X Windows provides you, the developer and user, with the most powerful graphical user interface available. Runs on Intel, Motorola, MIPS, and SPARC processors.

Realtime tasking gives you, finally, what we have all wanted...a real system -- and realtime performance!

CIRCLE NO. 17

Calendared

November 16 - 20
Comdex/Fall '92
Las Vegas, NV. Comdex/Fall, one of the largest trade shows in the country for computer and communications products, returns for its 14th year. The show focuses on the strategies and technologies of enterprise computing in the 1990s with five programs: corporate computing, new media, connectivity, the channel network, and international business and marketing. Also featured are four technology showcases, covering network computing, multimedia, imaging, and OEM business. Contact: The Interface Group, 300 First Ave, Needham, MA 02194-2722, (617) 449-6600, Fax (617) 449-2674.

CIRCLE 267

November 17 - 19
Wescon '92
Anaheim Convention Center, Anaheim, CA. The Wescon International Electronics Conference and Exhibition expects to draw more than 45,000 professionals to sunny California. Featuring more than 1,400 exhibitors, Wescon '92 presents five separate shows, highlighting such products as semiconductors, ICs, ASICs, EDA tools, and test and measurement equipment. Each show is complemented by dedicated technical sessions, covering topics relating to programmable architectures FPGAs, computer-integrated manufacturing, VXIbus modular instrumentation, and microelectronics packaging. Contact: Patti Masters, Wescon '92, 8110 Airport Blvd, Los Angeles, CA 90045-3194, (310) 215-3976, Fax (310) 641-5117.

CIRCLE 268

December 1 - 3
AFCEA Hawaii '92
Sheraton Waikiki Hotel, Honolulu, HI. The seventh annual Hawaii Pacific International Electronics Conference & Exposition provides a discussion forum for military, government and industry professionals from the U.S. and the Pacific Rim nations. The technical program will address such topics as electronic security, force downsizing, software reusability, and opportunities for U.S. industry in the Pacific Rim region. Contact: J. Spargo & Associates, 4400 Fair Lakes Ct, Fairfax, VA 22033, (800) 336-4583, ext. 6200, Fax (703) 818-9177.

CIRCLE 269

December 1 - 3
Technology 2002
Baltimore Convention Center, Baltimore, MD. Technology 2002, the third national technology transfer conference and exposition, features presentations by federal laboratories and contractors on the latest advances in computer, science, electronics, and manufacturing technologies. Sponsored by NASA, NASA Tech Briefs and the Technology Utilization Foundation, the conference offers more than 120 symposia and 60,000 ft² of exhibits. Contact: Wendy Janiel, Technology Utilization Foundation, 41 E 42nd St, New York, NY 10017, (800) 944-6272, Fax (212) 986-7864.

CIRCLE 270

Continued on page 28
Power seekers demanded it. We delivered. Presenting the 486 TEK-AT4 single board computer.

The first half-size 486 PC/AT to offer a cornucopia of essential features and Teknor’s unique approach to modularity: the interchangeable microprocessor.

Here’s how it works: start with a low cost 486SX configuration. Then, when you’re ready to upgrade, sink your teeth into the more powerful DX computing environment or the ultimate 66Mhz 486DX2. Simply by changing the microprocessor.

And since they are all 100% compatible, the cost of upgrading won’t cause you heartburn.

So call us today at 1-800-387-4222 to find out how you can sample the TEK-AT4. We’re certain it’ll satisfy even your most power-hungry applications.

P.O. Box 455, Sainte-Therese (Quebec) Canada J7E 4J8
Tel: (514) 437-5682 • Fax: (514) 437-8053
Contact-free soldering and de-soldering

with the new Leister Hot-Jet "S"

- For SMD and through board components
- Very rapid and ESD protected
- Hot-air temperature with stepless electronic control
- Air-volume with stepless electronic adjustment
- Power output 460 W, air volume 10-60 l/min
- Range of 700 desoldering nozzles available

NEW: Desoldering nozzle with temperature gauge

NEW: Desoldering nozzle with suction tube

PLEAS Ask FOR FREE BROCHURE UW 218 AND THE ADDRESSES OF SALES AND SERVICE OFFICES NEAR YOU.

Karl Leister, Elektro-Geratebau, CH-6056 Kagiswil/Switzerland
TEL. (041) 66 00 77, Fax (041) 66 78 15, Telex: 866 404

CIRCLE NO. 20

CIRCLe NO. 19

The SPARC™ CPUengine - 40MHz™

Indistinguishable.

With two exceptions.

First, Pinnacle’s
SPARC CPUengine-40MHz
has FAST SCSI-2.
10 MB/sec to be exact.

Second, the board comes with
a one year warranty.

Pinnacle Data Systems.
We manufacture solutions.

CIRCLE NO. 76

CIRCLE NO. 271

January 3 - 6, 1993
VLSI Design '93
Taj Intercontinental Hotel, Bombay, India. The Sixth International Conference on VLSI Design, with the theme Chip, Board and Systems Design in the 90s, brings researchers and designers to the west coast of India. The four-day program consists of paper sessions, posters, tutorials, and industrial CAD exhibits, covering such topics as CAE/CAD systems, logic synthesis, design for testability, circuit simulation, and economic issues. Contact: Rochit Rajsuman, Dept. of Computer Engineering & Science, Case Western Reserve University, Cleveland, OH 44106, (216) 368-5510, Fax (216) 368-2801.

CIRCLE NO. 272

The SPARC™ CPUengine - 40MHz™
The new SPARC®-2SE has serious crunch power. 30 MIPS and 5 MFLOPS change the definition of single board computer performance. Workstation features? This board is loaded.

If you need I/O, try 10Base-T, Ethernet, AUI, SCSI, and VME. Parallel, serial, keyboard, mouse and audio ports get you connected.

Choose SunOS or VxWorks to tackle embedded and critical real time applications. Our MBus architecture is the high speed path for VME data and the only way to track Sun's hot new product moves.

Need more? Two SBus slots turn on a world of graphics and communications options. With 128 Kbyte cache and up to 128 Mbytes of DRAM on-board, no job is too big.

It's simple: When it comes to crunch, the 2SE eats the competition's lunch.

 SPAAC! is a registered trademark of SPARC International licensed exclusively to Themis Computer. All others are trademarks of their respective companies.
His perception transformed the world. Leonardo da Vinci brought a new dimension, a different and extraordinary vision to the world of art and science. And in the process, he defined the concept of perspective and pictured nature as it really looked.

In the world of PC Compatible products, Micro Industries brings a new dimension to the market: a new perspective on the functional requirements of OEM applications that can support your needs now and into the future.

Micro Industries provides PC Compatible Technology that will satisfy even the most demanding OEM applications. Our products are available in a variety of configurations and can be easily modified to support your unique requirements, without sacrificing long-term compatibility with evolving technology.

You should be able to develop your products without the fear of future compatibility problems or even worse—obsolescence. Our commitment to quality and service ensures you of success, today and in the years to come, with a partner that understands the needs of the market.
Micro Industries creates a solution with the needs of the OEM in mind:

We provide the engineering support you need to configure the optimal price/performance solution for your application.

We offer a variety of hardware platforms to accommodate future performance requirements into your design without paying a premium today.

We have a proven history of maintaining compatibility of our products from generation to generation and supporting products over the life of the application.

We can isolate your applications software from the constant evolution of PC component technology.

Achieving Tomorrow's Ideas Today.

We're Micro Industries. We provide electronic solutions that help you bring ideas to market... faster, more cost-effectively, and with higher quality end products. You supply the ideas, and we can provide the electronics solution. Micro-processor based board-level solutions. In your choice of standard, semi-custom, or full custom boards. In low, medium, or high volumes.
EDA and test vendors forge alliances to promote standards

Mike Donlin, Senior Editor

The recent International Test Conference (ITC—Baltimore, MD) marked a shift in testability's role in system design. A spate of alliances and joint technology/marketing agreements heralded what many analysts and engineers alike agree will be a new relationship between design, test and manufacturing departments.

Perhaps the most significant of these announcements was the official launching of the Design & Test Alliance (DTA), a confederation of automatic test equipment (ATE) vendors, electronic design automation (EDA) software suppliers, system houses, and semiconductor companies. Although the Alliance is still in its infancy, initial meetings provided encouraging signs that participating companies would unplug the test bottleneck plaguing the production cycles of today's complex ICs and systems.

The DTA's primary objectives are to spur cooperative efforts between vendors and users of design and test technologies and to raise management's awareness of the importance of integrating these technologies with operations. Through ongoing research programs and projects, the Alliance will try to provide quantitative data and analysis on this integration. Another major goal of the group is to accelerate the integration process by sharing the results of its analysis with the electronics industry.

The Alliance is presently composed of nine companies: Cadence Design Systems (San Jose, CA), GenRad (Concord, MA), Hughes Aircraft (Los Angeles, CA), LTX (Westwood, MA), Mentor Graphics (Wilsonville, OR), Racal-Redac (Mahwah, NJ), Synopsys (Mountain View, CA), Teradyne (Boston, MA), and Texas Instruments (Dallas, TX). These companies will pool resources to create a board of directors, administrative personnel, a steering committee, a research committee, and working groups.

The working groups are currently being formed. They'll address integration issues at a technical level and report to the steering committee. The steering committee will be composed of four categories of members, representing EDA, test, support, and end-product manufacturers, with members from academia involved in the appropriate categories based on their technical focus. These member categories will permit the engineering problems of each group to be represented and addressed adequately at the management level of the alliance.

The DTA is scheduled to present its initial research findings in the first quarter of 1993. The Alliance hopes that, by bringing a managerial as well as a technical focus to the effort, it will be able to convince the computer industry of the importance of bringing test issues forward in the design cycle. "The way the industry approaches test is fundamentally changing," says Jeff Hotchkiss, vice-president of Teradyne. "Today, there's a broader set of issues that has to do with the integration between silicon vendors, EDA tool suppliers and ATE companies. It affects how designers test their systems."

Although the need for such integration has existed for some time, the increasing complexity of both silicon and systems, and the resulting lack of accessibility for mechanical testing devices, is bringing the design-for-testability issue to a head. "We realize that there have been pockets of design-for-test activity through the years," says Jim Solomon, president of the analog division at Cadence. "And we aren't here to become a standards body. But the time has come to instill in the minds of the design and test communities the need to address product development in conjunction with a synergistic design/test philosophy. DTA aims to educate both camps toward the common goal of productive product development."

I Partners for standards

In addition to the announcement of the DTA, the ITC saw the formation of other alliances portending the integration of design and test as well as the acceptance of standards such as IEEE 1149.1 for boundary-scan design methodologies. Tektronix (Beaverton, OR), Teradyne and Tex-

Members of the Design & Test Alliance conducted a press conference to kick off the consortium's efforts. Press conference speakers, from left to right, are: Doug Kostlan, TI marketing manager; Vin Ratford, Mentor Graphics marketing manager; Jim Solomon, president of the analog division at Cadence; and Jeff Hotchkiss, vice-president of Teradyne.
So you think you can design a better embedded computer than we can?

Of course you can. And we'll even help you. With the new MVME162 Embedded Computer.

The MVME162 is modular. Adaptable. So that you can select the exact functionality you want, without paying for features you don't need.

Now, would you like your MVME162 with a 68040 CPU (with floating point) or a 68LC040 CPU (no floating point)? VME bus or no bus? One, two, three, or four IndustryPack™ modules? Synchronous or Asynchronous serial ports? Ethernet or SCSI? 1MB DRAM or 4MB? 512K or 2MB of SRAM? And what other functions would you like with that?

Decisions, decisions. And they're all yours.

About the only thing that's not optional is Motorola's unmatched single board computer expertise, breakthrough engineering, outstanding performance and unwavering commitment to quality.

That's standard with every board.

With all that the MVME162 offers you, the easiest decision to make is to call the number below for a free information pack.

1-800-234-4VME
Teradyne’s Virtual Interconnect Test module (left screen) generates test patterns that provide 100-percent pin-level fault coverage for boundary-scan devices. The module can link to Teradyne’s board testers as well as TI’s ASSET PC-based boundary-scan design debug tool (right screen). ASSET’s scan analyzer supports logic analyzer-type features such as waveform displays (upper window) and state-table displays (lower window).

as Instruments, for example, announced an agreement on a joint development and marketing effort to support 1149.1. The new relationship is an extension of an agreement that TI and Teradyne announced at last year’s ITC. In it, the two companies joined forces to promote links between Teradyne’s Victory boundary-scan test module and TI’s Advanced Support System for Emulation and Test (ASSET) via Teradyne’s Virtual Interconnect Test (VIT) software.

Tektronix will join in these efforts, as well as incorporate boundary-scan diagnostic capabilities into its laboratory rack-and-stack equipment during 1993. “We’re pooling our efforts to reach four major goals,” says David Fink, market segment manager at Tektronix. “First, we’re committed to the development and integration of products supporting the 1149.1 family of buses. Second, we’re going to promote industry standards to take full advantage of 1149.1 features. Third, we’re going to develop cooperative programs to serve the specific needs of customers through our combined expertise. Finally, we’ll be cooperating in joint training, sales and marketing.”

Texas Instruments also used the ITC forum to announce a revamped version of its ASSET boundary-scan development suite—Version 2.0. “The new release is based on input from customers over the last four years,” says Glenn Woppman, ASSET product manager at TI. “We used that information to define the new release and rewrote the code for the entire product family using C++ object-oriented methodologies. We’re convinced that boundary scan’s acceptance depends on products that make it easier for designers to include it in their designs.”

According to TI, ASSET simplifies scan-path management and increases scan speed via a test-bus controller. Through its object-oriented database and controller-based architecture, the system assumes the burden of counting test clocks and managing test access port state transitions. ASSET also includes an interactive debugger and scan analyzer. By interacting at a functional level, you can scan instructions or data into device test registers and view results.

Another test vector development method that ASSET supports is 100-percent boundary-scan interconnect automatic test pattern generation (ATPG). “Customers told us that ATPG for boundary-scan interconnects is a key concern,” says Woppman. “The ASSET VIT product, based on Teradyne’s Victory technology, addresses that.”

Workbench boundary scan
By adding Tektronix to the JTAG team, TI and Teradyne are hoping to make boundary scan an integral part of the design/test environment by bringing it into the engineer’s laboratory. If boundary scan is available as a design verification and debug tool, they reason, then designers might be inclined to choose devices that incorporate 1149.1. This in turn will pressure silicon vendors to incorporate the standard into their off-the-shelf products.

Tektronix hopes that, by offering boundary-scan diagnostic capabilities to its customers, the company may woo them over to buying racks of test equipment from a single source. “People are getting tired of mix-and-match laboratory facilities where they have to try to connect incompatible equipment from different vendors,” says Tektronix’s Fink. “We’re also hoping that the new equipment, which is based on the VXIbus, will let them downsize their equipment racks while increasing the bandwidth of their test systems. The older GPIB standard reaches its limits at around 200 kHz, while VXI
Pick up the number one real-time operating system.

And run with it.

In today's competitive market, it's important to run with the best. And when it comes to real time, the iRMX® operating system is the clear favorite.

You see, iRMX has a 13-year track record for proven reliability. In fact, only DOS runs on more X86 systems. Now, iRMX for Windows provides the first real-time operating system with guaranteed response time that runs DOS and standard-mode Windows on the i386™ and i486™ architecture. That's right, true real time on a PC!

iRMX for Windows brings more than just affordable hardware to real time. It also gives you a head start on development with access to the huge installed base of DOS applications and tools. In fact, you even have the option to run Windows® (including Windows 3.1).

So take the first step, call (800) GET-iRMX (800-438-4769)¹ and ask for Lit. Pack. #2B. And start running real time with your favorite DOS and Windows software.

¹Outside the U.S.A. and Canada, FAX (503) 696-4633. © 1992 Intel Corporation. iRMX is a registered trademark and i386 and i486 are trademarks of Intel Corporation. 
¹iRMX runs on IBM and Compaq compatible i386 and i486 based PCs. ᶾAll other products shown or mentioned are trademarks or registered trademarks of their respective owners.
We want to hear from you!

So, what do you think of Computer Design? What do you like best, the Technology Viewpoint pieces? The Technology Directions articles? The Special Reports? The Product Focus articles and specification tables? New Product Developments? Steve Oh's column on Mixed-Signal Design? What is there about Computer Design that you don't like? What would you like to see us cover more extensively?

The only way we can know what you like or don't like, or what you want to see more of or less of, is if you'll write us. There's about 11.25 in.² of space on the Reader Inquiry Card for your comments, but if that's not enough, you can write directly to John Miklosz, Editor-in-Chief, Computer Design magazine, 1 Technology Park Dr, Westford, MA 01886.
Radstone reveals an ancient technique for designing an ultra high performance VME system...now.

Lurking right there in the VMEbus designer's bag of powerful tricks is the over-looked, under-utilized and very potent VSB with all of its board and system enhancing features. There's even a complete range of VME/VSB boards just waiting to be designed into a superfast, super-flexible system...right now.

A multiple systems-within-a-system architecture forming tightly coupled sub-systems capable of independent and parallel operation.

The VME Sub-system Bus gives you:
- A proven system solution that's multi-vendor sourced and industry accepted.
- Highly flexible multiple bus capability today.
- Multiple systems within a system.
- Wide range of products: CPUs, I/O and memory.
- Freeflow+ architecture that eliminates system bottlenecks.
- Increased system efficiency: VSB for data/VME for message passing.

If you're looking for a way to get next generation bus architecture performance right now, look at VSB. Radstone will support your efforts with the world's most complete line of VME/VSB processor, I/O and memory boards and the world's only line of Freeflow+ architecture boards. Call us to take advantage of the ancient wisdom of VSB...now.
2,000-Mips PC rescues high-end applications

Warren Andrews, Senior Editor

The Intel personal computer architecture and PC/MS-DOS operating system are now ubiquitous, and have made steady inroads into many commercial and industrial applications. Once rooted, this technology hasn’t always been able to deliver practical solutions, but based on a hardware/software cost ratio of between 1:10 and 1:20, OEMs have been jumping through hoops—and putting their suppliers through ordeals—to make up for any inadequacies while maintaining software compatibility.

PCs have fallen down on the job for a variety of reasons. One is that PCs were intended for a relatively gentle office environment and can’t handle harsh physical and electrical conditions. Many PC makers interested in industrial solutions have evolved environmentally hardened, passive-backplane systems, ruggedized motherboards, PCs embedded in other form factors (such as STD, Multibus and VME), and even totally new pin and connector configurations.

These solutions have solved many problems, but new ones have continued to appear—mainly in the areas of form factor, power dissipation and performance.

**Form factor, power, performance**

Responses to the form-factor problem have come from a variety of manufacturers, from the compact boards of Ampro Computers (Sunnyvale, CA) and the PC/104 consortium, to ESP designs from Dover Electronics (Longmont, CO), to the latest compact industrial PC from RadiSys (Beaverton, OR). Some of these solutions also address the low-power needs of portable and remote instrumentation.

When higher performance was required, OEMs have traditionally had to wait for the next generation of processor to emerge, hoping it will provide the needed performance enhancement.

This need for more and faster processing spawned the RISC revolution, unleashing a new type of processor with less baggage so that new generations can be implemented faster.

And then along comes the need for multiprocessing. Although multiprocessing technology is just starting to reach the marketplace in the form of new workstations, it provides little relief for those committed to the PC/MS-DOS environment. Promised multiprocessing configurations for MS-DOS-based machines haven’t yet materialized.

Until now, that is. The Multibus Manufacturers’ Group (MMG—Aloha, OR) has just come up with a solution to the problem that theoretically lets PC applications run in Multibus II multiprocessing environments at speeds of 2,000 Mips and beyond. The solution can be implemented today because it uses standard off-the-shelf boards.

The technology, demonstrated at Buscon East (Boston, MA, September 14-18), comes in two systems: a 33-MHz, 486-based laptop PC and a PC-based Multibus II system. In single-CPU configurations, both systems operate at 27 Mips. But the Multibus II system includes six boards operating together that produce more than a tenfold improvement.

And, according to MMG executive director Len Schu/witz, the technology is fully scalable to a full 20-slot Multibus system, providing more than 2,300 Mips.

Schulwitz says the Multibus II message-passing capability acts as a fast LAN, which operates at 40 Mbytes/s. "The MMG Technical Committee developed high-speed communications among Multibus II boards and PC-based Multibus II boards which support DOS BOS," says Schulwitz. "Known as the Multibus II Transport, the most recent release provides backplane communication between MMG boards and any DOS-based PC board on Multibus II."

For the demonstration at Buscon East, the MMG used boards from three vendors: a 120-Mips i860 board from Mentec Computer Sys-
DOS, Windows and real time. At the same time.

The most widely-used application software runs on DOS and Windows. But they can't provide real-time capabilities for demanding industrial applications.

Microware’s OS-9000 Real-Time Operating System with Virtual PC (VPC) lets you run DOS and Windows as tasks under OS-9000. Data and I/O devices can be shared between the two environments. DOS or Windows applications can be used to monitor and control real-time processes running under OS-9000. And VPC is included FREE with the OS-9000 Real-Time Operating System.

OS-9000 provides complete real-time development and run-time environments for hard real-time applications, including Microware’s Ultra C advanced, high-technology ANSI C compiler. OS-9000 also offers extensive options for networking and graphics.

Do you want DOS, Windows and real time at the same time? Call our toll-free number to order your complete “plug-and-play” OS-9000 386/486 package for only $995. Or ask for your free copy of Questions & Answers for Serious 386/486 PC Users.

Call Microware Today!

1-800-475-9000
One of the top performers in the MMG demonstration of high-performance O/S-based machines is Mentec’s i860-based accelerator card. The board adds 120 Mips to the processing power of the Multibus II system.

To support these dramatically higher levels of PC performance, says Jack Blevins, MMG technical director, “PC systems must be scalable in both hardware and software. Hardware scalability lets you easily add processor boards to support multiprocessing without upsetting the existing system. More important, software which runs on a single-processor system must now be distributed to run on two or more processors.”

“To solve the software problems,” Blevins continues, “you have to scale PC software over multiple processors. To do this you have to overcome two obstacles. The first is task-to-task communications, which lets two or more CPUs share the load. The

The Powerful Combination!

DX2 and DTI

A Powerful Combination!

50/66MHz 486 EISA
Engine Only

Product names are trademarks or registered trademarks of their respective companies.
second is sharing system I/O resources. A significant effort is needed to accomplish the seemingly mundane task of sharing disk, terminals and peripherals, and this is true from the exclusive ownership of a single processor, such as in standard PC systems, to coping with multiple processors that must access I/O.

I Multiprocessing solution

The idea of using a number of PC-based CPUs in a multiprocessing environment has been tossed around for several years. Former Multibus wizard John Hyde frequently used such a multiprocessing paradigm to describe his view of the future of multiprocessing systems. Hyde left Intel's Multibus group to join the company's advanced processor group, where it's expected he will apply the same model to multiprocessing at the processor-chip level.

While we wait for this higher chip-level performance to emerge, perhaps some of Hyde's legacy remains,

"To support dramatically higher levels of PC performance, PC systems must be scalable in both hardware and software."

—Jack Blevins
MMG technical director

since board-level technology that's now available can show significant advances over single-processor approaches in DOS-based systems. It may well even be possible to exceed the current speculations of MMG members.

For example, using the new MMG approach to double the speed of the Multibus II backplane to almost 80 Mbytes/s, intertask communication can take place with even greater ease than is currently the case. Further, Micro Industries recently introduced a DSP board sporting four AT&T DSP32C chips. "Putting 19 such boards to work in a system with an 80486 host could result in dramatically greater performance, solving the right kind of problem," says Micro Industries president Michael Curran. "It's possible to achieve more than 20,000 Mips on a DOS application using such an approach."

The MMG solution might not be for everyone, but it does allow OEMs now married to a PC-based solution to easily jump an order of magnitude in performance without waiting for individual processor chips to reach that level. Costs are high compared
320 MFLOPS

SuperCard i860-based vector processors deliver. With our Quad 860 multiprocessor and our SC-3XL ultimate performance models, CSPI continues to offer you the greatest range of vector processing power. Look what you can get on a 6U board with VME64:

- 320 MFLOPS Performance
- 64 MBytes Memory
- 200 MBytes per second I/O
- Intel's 50 MHz i860 XP chips
- 200 usec 1024 complex FPT
- VME64 and VSB
- MIL Spec
- GFLOPS Multiprocessors
- 200 usec 1024 complex FPT

CSPI's SuperKit and Integration Toolkit software cut development time to the bone with:

- Industry-leading Libraries
- DataFlo Visual Programming
- pSOS+ Real-time Kernel
- C, Fortran, and Ada
- UNIX compatibility

Call or write CSPI and learn more about our new Quad-860 and SC-3XL SuperCard family members: CSPI, 40 Linnell Circle, Billerica, MA 01821, 1-800-325-3110, Fax: 508-663-0150. In Europe, CSPI, Creteil, France, 33-1-43774577, Fax: 33-1-43994508.

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Intel (408) 765-8080 ... Circle 263
Multibus Manufacturer's Group (503) 696-7155 ... Circle 264
Mentec Computer Systems 353 1 2851444 .... Circle 265
Micro Industries (614) 548-7878 .................... Circle 266

A pricey approach

The Multibus II approach provides dramatic scalability for those users requiring ultimate performance and willing to accept the increased cost of hardware and software development. Even compared with a pricey 50-MHz 486 (at well under $3,000), the Multibus solution is costly; each of the CPU boards used in the system is priced between $3,000 and $6,000. Then add to this the cost of a backplane, card cage and power supply.

Single-processor solutions aren't likely to reach the 2,000+-Mips performance level in the near future, but the migration from a single-processor PC to a multiprocessor Multibus II system won't be as seamless as going from one generation of CPU to the next. Someone has to tell which task to go where, and the MMG's software doesn't do that yet.
Looking for maximum performance in VME-based X Windows applications? Your search is over.

1. **More Processing Power**
   While most X servers rely on a single processor, the IGC uses two. A 40 MHz TMS34020 handles the X server code and graphics, while a 20 MHz MC68020 takes care of the TCP network communications and user interface. By dividing computing tasks and off-loading X Window server routines from the host, our dual-processor design significantly improves overall system performance.

2. **High-Resolution Performance**
   When your application demands high-speed, high-resolution color graphics, the IGC delivers. It runs 37,000 X Stones with 1280 x 1024 non-interlaced resolution — while displaying 256 colors from a palette of 16.7 million.

3. **More Configuration Flexibility**
   No other VME-based X server offers you the configuration flexibility of the IGC. It can communicate with X clients over the VME backplane, through Ethernet™ or both — making it ideal for a wide range of VMEbus X applications. You can even install several IGCs in the same VME system.

   The IGC is compatible with Tadpole’s extensive line of high-performance RISC and CISC single-board computers running VxWorks™ or TP-IX, Tadpole’s implementation of UNIX® System V3.2.

4. **More On-Board Software**
   On-board EPROM contains the complete X11R4 server code, which is optimized for the IGC’s dual processors. The IGC also offers the convenience of built-in VT100/200 terminal emulation, diagnostics and a user-friendly firmware monitor.

5. **Just Plug And Play**
   The IGC comes complete with a mouse and keyboard interface. Just add power. We’ve taken care of everything else.

   So what should you look for in high-performance X? You’re looking at it: Tadpole’s new TP-IGC6V.

For information in the U.S. call: 800-232-6656

Cambridge, England 0223 250030
Paris, France (1) 60 86 27 92
All trademarks belong to their respective companies.
Integrated tool environment targets real-time development

Tom Williams, Senior Editor

Software tool integration isn’t waiting for standards. Increasingly, tool vendors are setting up environments that address the way programmers develop code in the real world, which often doesn’t conform to theories about how such development should be done. Answering the growing needs of real-time and embedded systems programmers for integrated development environments is Microtec Research (Santa Clara, CA), which has introduced a system based on its proven and popular XRay debugger technology.

XRay MasterWorks provides an integrated C and C++ software development environment for embedded systems engineers. Significantly, the environment doesn’t include the front-end structured design and analysis CASE tools that have received so much publicity recently. Rather, XRay MasterWorks concentrates on tools for building programs, generating and debugging code, navigating through source files, and managing projects that are oriented toward enhancing the efficiency of the edit-compile-debug process, which is the way most developers are working today.

Message server at center

The hub of XRay MasterWorks is a message server that ties together the current suite of tools and provides for the integration of future tools. The server provides point-to-point communication between tools rather than broadcasting to all tools on the system. “For example,” says product marketing manager Arubindo Tripathy, “under the file menu, I have a button that says ‘re-make and reload.’ Any time someone clicks that, we have to establish communication between the XRay Make tool and the debugger.” The Make tool already knows what needs to be rebuilt, so the message only needs to tell the debugger what particular target is to be rebuilt. The debugger can then instantly be aware of all the files making up the program under development.

In the future, Tripathy says, Microtec is planning to open the messaging scheme so that you can integrate other tools.

At present, Microtec is working with certain value-added resellers, giving them the messaging protocol to help them integrate their products. Applied Microsystems (Redmond, WA), for example, is working on integrating its in-circuit emulation tools into the MasterWorks environment.

You interact with the system via the XRay control panel, which lets you set up a project and working environment. The control panel is more than a graphical user interface; it lets you select tools, working directories, project-specific source files, and make files to establish the context in which you’ll be working. It’s possible, for example, to bring frequently used commands that may normally be hidden in a menu onto an on-screen button for easy access. It’s also possible to save different contexts for different projects.

The control panel doesn’t currently support version control, however. The level of project control provided involves setting up which files are associated with a given project, launching tools and setting up directories, so eliminating many repetitive steps when starting a session.

Microtec has integrated its widely used XRay source- and assembler-level debugger into MasterWorks, along with its relatively new Source Explorer navigation tool. Source Explorer graphically displays a program’s calling structure, its function definitions and specific function calls. Integrating Source Explorer with the XRay debugger lets you graphically control program execution at the function level via the graphical program structure display.

Each box in the call tree represents a function and contains information on whether that function is global or local; clicking on a box with the mouse brings up this information. It’s possible to display the
DISTRIBUTED PROCESSING
WITH THE QNX® FLEET™ NETWORK.

Because computers were meant to run together.

Maybe it's not natural to expect a network of microcomputers to perform like a supercomputer.

With the QNX operating system, it's not natural to expect anything less.

POSIX AND MORE
Thousands of VARs and OEMs choose QNX for mission-critical applications – from POS to manufacturing to medical instrumentation. And with good reasons.

Like POSIX compliance. And real-time performance. And true microkernel architecture. And message-passing IPC. Not to mention our technical support and customer services.

Now add “FLEET” to the list.

FAULT-TOlERANT NETWORKING
With most networks, a hardware failure spells disaster. But not with QNX.

If a card or cable fails on a dual-net FLEET setup, QNX will automatically re-route data through the other network before you – or your application – can even blink.

EOFICIENT PERFORMANCE
FLEET uses network hardware to full advantage for maximum throughput. Whether you’re running Ethernet for speed (application-level throughput at just under 1 Mbyte per second) or Arcnet for deterministic transactions – or both network cards in the same machine – you can count on FLEET for optimum efficiency.

Extensible Architecture
You can support new networks simply by adding new drivers. And you can start and stop drivers dynamically, without even rebooting.

TRANSPARENT DISTRIBUTED PROCESSING
In QNX there’s no difference between local execution and network-remote execution. Which means you don’t need to modify your applications in order to distribute them across the FLEET network.

To sum up: networking with QNX is fault-tolerant, load-balancing, efficient, extensible, and transparent. But it’s a lot easier to just say “FLEET.”

Go with the QNX FLEET network. Nothing runs like it.

To find out how your applications can thrive in the QNX environment, call 1-800-363-9001 (ext. 103).
XRay MasterWorks integrates functions to aid the edit-compile-debug process and to automate the tedious tasks of program building. Control of a project takes place through a window panel that defines tools to be launched, modules in the project, files, and directories. Tools communicate point-to-point to let you easily find your place in large volumes of code.

VMEbus 486DX2 -66MHz

- New generation single slot 486DX2-50 & 66MHz -100% PC/AT compatible (A32/D32)
- No platforms, no piggy-backs, just clean streamlined low-cost one-side SMD technology
- Up to 16M of on-board DRAM
- 1024x768 SuperVGA w/512K Video DRAM
- 2 Serial Ports, 1 Parallel Port and Real Time Clock w/Battery
- AT style keyboard Controller and Connector
- Floppy and Hard Drive IDE Controllers on-board -4 ways to connect to Disk Drives
- Three-way Byte/Word Swapping Hardware for interfacing to 68000 type CPUs
- Access VMEbus through Real Mode Window or Protected Mode
- Custom Gate Array technology provides -Interrupter, Interrupt Handler, System Controller, all SW configured
- Reset Switch and Speaker
- Choice of SCSI or PC/AT Bus on P2

INTERGON INC.
3000 Wilcrest
Houston, Texas 77042

Tel: (713) 780-7003 Fax: (713) 974-6059 1-800 - 68VME-AT

Automated program building

Program building is automated by the XRay Make tool, which is based on UNIX's make(1). This compatibility lets you use existing make(1) files under MasterWorks without modification. Make also identifies build errors and displays the offending source code lines in a window for quick editing.

XRay MasterWorks gathers a suite of cross-development tools for a range of different CPUs and MPUs. These include ANSI C and C++ cross-compilers, assemblers and linkers. There's also a set of C++ class libraries. In addition, the environment supports instruction-set simulators that can be used with the debugger and Source Explorer before target hardware is ready; they can yield information down to the detail of cycle counts.

Finally, there's an object format converter that can convert the output of the Microtec tools and compilers into forms usable by logic analyzers, emulators and PROM programming devices. These include IEEE-695, common object file format and Intel OMF-86.
Learn the Only Embedded Debugger You Will Ever Need Without Turning the Page

TARGETS:
68xxx, 386/486, R2000/R3000/R4000, Sparc, 88000/88110, Gmicro, V810, more...

C • C++ • Fortran • Pascal

Double click on a variable to create a window that displays its value whenever the program stops.

Click on a variable to print its value.

Click on a green dot to set a breakpoint. Click on the stop sign to clear the breakpoint.

The program is currently stopped here.

Click on a function name to display its source code.

Attach to a target with the "remote" command.

Set a conditional breakpoint at the current line.

Click "go" to continue (or start the program).

Click "reg" to display a register view window.

Click "help" to learn the rest of MULTI.

Monitor calls
ret struct bar {  
41 struct bar {  
42 struct bar *next;  
43 enum color {red,orange,yellow,green,blue}color;  
44 float d[10];  
45 int count;  
46 }*Bar;  
47  
48 struct bar *NewBar(count,color)  
49 enum color color;  
50 {  
51 int i = 0;  
52 struct bar *ret;  
53  
54 if (count == 0)  
55 return 0;
56 ret = (struct bar *)malloc(sizeof(struct bar));  
57 ret->next = NewBar(count-1,color);  
58 ret->color = color;  
59 ret->count = count;
60 for (i = 0; i < count; i++)  
61 if (count)  
62 return ret;
63  
64  
65 main()  
66 {  
67 Bar = NewBar(10,orange);
68 Rest();

STOPPED

remote monserv /dev/ttya
Remote cpu: M68020
Remote coprocessor: M68882
count: 10
stopif i=9

It's worth learning MULTI to fix one bug.

Hosts: Microsoft Windows, Sparc, Sun-3, DECstation, Unix/386, Motorola Delta, more...

Green Hills

© SOFTWARE INC.
510 Castillo, Santa Barbara, CA 93101
Tel: (805) 965-6044 • FAX: (805) 965-6343

Oasys

1 Cranberry Hill, Lexington, MA 02173
Tel: (617) 862-2002 • FAX: (617) 863-2633

Copyright 1992 Green Hills Software, Inc. MULTI and Green Hills Software are trademarks of Green Hills Software, Inc. All other trademarks are trademarks of their respective owners.
Can Your Current MCUs Meet These Specs?
Your designs demand more from existing MCUs. As the leader in MCU technology, Mitsubishi offers you a breadth of 8- and 16-bit microcontrollers with the functions you want.

**Highest Integration**
Get the highest levels of on-chip functionality with a host of features you need most, including synchronous I/O, UARTs, programmable I/Os, A-D/D-A converters, LCD and VFD drivers, PWM, special timers and more.

**Lowest Power Dissipation**
We offer the lowest power dissipation available today—4mA at 3.0V at 8MHz, for our most highly integrated 16-bit MCUs.

**Low Voltage**
For low voltage, our MCUs operate in the 2.7 to 5.5 volt range at 8MHz. For higher performance up to 25MHz, we offer 4.5 to 5.5 volt operation without paying the high power penalty.

**Largest On-Chip Memory**
Utilize up to 2 Kbytes RAM and 32 Kbytes ROM or OTP with our 16-bit MCUs, and up to 1 Kbyte RAM and 32 Kbytes ROM in our 8-bit MCUs, with expanded memory planned for the future. EPROM and ROMless versions are also available.

**Smallest Packages**
Get all these advantages in the smallest packages on the market. Mitsubishi offers a wide range of packaging options including 64- to 160-pin surface mount packages, with 0.50mm, 0.65mm and 0.80mm lead pitch. Shrink DIPs are available in 32- to 64-pin configurations.

For faster time to market, Mitsubishi provides development support tools for each phase of your product design.

For your best system solution, call Mitsubishi today at (408) 522-7498. For Eastern U.S. and Canada, call (408) 522-7499.
Powerline spread-spectrum modulation saves copper in LANs and control systems

Don Tuite, Senior Editor

A building's electrical power wiring is an attractive medium for data communication. This is because such wiring, unlike dedicated runs of coaxial or twisted-pair cable, is already in place, so that if the network is ever reconfigured, it won't be necessary to lay more cable. It's even more attractive for industrial control than it is for office LANs, because it connects to most of the devices that have to be controlled, such as lights, chillers and motors.

Unfortunately, those same lights and motors make power wiring a difficult transmission medium for either office or industrial communication. Signals above a few hundred kHz are attenuated by tens of dB, changing loads cause ground bounce in the neutral wire, and fluorescent ballasts and thyristor-based controllers create severe noise.

In the past, attempts have been made to run data at low baud rates over powerlines, with the best-known efforts focusing on remote meter reading. None of these attempts has resulted in widespread commercial success, but a new approach is being pioneered by a pair of companies using spread-spectrum techniques so that narrow-band noise can't interfere with data transmission.

Two companies, two approaches

The two companies currently shipping products for spread-spectrum powerline communications are Echelon Corporation (Palo Alto, CA) and Adaptive Networks (Cambridge, MA). Echelon's modules are new elements in its established product line—a complete, distributed-intelligence industrial control system.

Spread-spectrum modulation is usually thought of as an RF data-transmission technique. To date, the most celebrated use of such modulation has been in the U.S. global positioning system (GPS) satellite network. The same techniques, however, that communicate the ephemerides of navigation satellites to a tank commander in Iraq can be used to access a file server on an office LAN.

Spread-spectrum is essentially immune to narrow-band interference, and the effective sensitivity of spread-spectrum detectors is extremely high. To apply spread-spectrum modulation, you use a known pseudo-random bit sequence to frequency- or phase-shift-modulate a carrier. The data is encoded on the pseudo-random sequence by either shifting or not shifting the phase each time the sequence repeats, using an NRZ (non-return-to-zero) format. A correlator at the receiving end detects the pseudo-random sequence and extracts the data from the phase information.

Chipping away at data

Adaptive Networks' strategy is more broadly based, encompassing LANs and WANS in addition to industrial controls. Of the two companies, Echelon is more willing to talk about the physical layer of its protocol, while Adaptive Networks tends to treat its modulation techniques as proprietary, preferring to talk about its flexible token-passing data protocol.

Echelon's transceiver communicates at an effective data rate of 10 kbits/s. According to the company's director of engineering, Tom Tormey, the transmission technique used is direct-sequence spread-spectrum, at 31 chips per bit. (A chip is the narrowest pulse width in the encoding pulse sequence that can be used to represent a bit. The number of chips per bit used in a spread-spectrum encoding scheme represents a trade-off between the degree of spectrum spreading and the bit rate.)

If the modulating pseudo-random sequence consists of a simple series of square pulses, the distribution of harmonics in the frequency domain is a $|\sin x/x|$ pattern. Echelon's engineers have trimmed the modulating signal to provide an essentially flat distribution within the required frequency band, with a rapid rolloff at the upper end.

This was necessary because, in the United States, the spread-spectrum signal must fit between 100 and 450 kHz. The 100-kHz limit is set by practical considerations, because powerline noise increases dramatically below that. The upper limit reflects an FCC require-
### Memory Configuration

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Features</th>
<th>Part Number</th>
<th>Access Time (ns)</th>
<th>Packaging Options</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Triple Port DRAMs</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>256K x 4</td>
<td>Fast Page Mode/Block Write</td>
<td>MT43CA257/8</td>
<td>80,100</td>
<td>SOJ</td>
<td>Now</td>
</tr>
<tr>
<td>128K x 8</td>
<td>Fast Page Mode/Block Write</td>
<td>MT43G8128/9</td>
<td>80,100</td>
<td>SOJ</td>
<td>Now</td>
</tr>
<tr>
<td><strong>Dual Port DRAMs (VRAMs)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>256K x 4</td>
<td>Fast Page Mode/Block Write</td>
<td>MT42C4256*</td>
<td>70,80,100</td>
<td>ZIP, SOJ</td>
<td>Now</td>
</tr>
<tr>
<td>128K x 8</td>
<td>Fast Page Mode/Block Write</td>
<td>MT42C8128*</td>
<td>70,80,100</td>
<td>SOJ, TSOP</td>
<td>Now</td>
</tr>
<tr>
<td>256K x 8</td>
<td>Extended Data Out/Block Write/Programmable Split</td>
<td>MT42C8256</td>
<td>70,80</td>
<td>SOJ, TSOP</td>
<td>Now</td>
</tr>
<tr>
<td>256K x 8</td>
<td>Fast Page Mode/Block Write/ Dual Write Enable</td>
<td>MT42C8255</td>
<td>70,80</td>
<td>SOJ, TSOP</td>
<td>Now</td>
</tr>
<tr>
<td>256K x 8</td>
<td>Fast Page Mode/Block Write/ Dual Write Enable</td>
<td>MT42C8254</td>
<td>70,80</td>
<td>SOJ, TSOP</td>
<td>Now</td>
</tr>
<tr>
<td><strong>Specialty DRAMs</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>256K x 16</td>
<td>Fast Page Mode</td>
<td>MT416256/7/8/9*</td>
<td>70,80</td>
<td>ZIP, SOJ, TSOP</td>
<td>4Q92</td>
</tr>
</tbody>
</table>

*Low power versions also available.

**Windows** is a trademark of Microsoft Corporation.
The utility of spread-spectrum communications lies in its immunity to much stronger interfering signals. This representation of an oscilloscope’s time-domain display shows the voltage amplitude of a fluorescent light ballast’s noise burst as it apparently obliterates a received signal.

In a practical system, each of Echelon’s Neuron Chips (one per node) delivers 55 to 60 packets per second. To deal with dynamic variations in the condition of the powerline, the transceiver module incorporates an oversampling correlation filter and an adaptive bit timing recovery algorithm to synchronize instantaneously to incoming packets.

If an error occurs, packet reconstruction is faster than packet retransmission. Classical methods for

**Features Include:**

- Supports any 386SX/486 processor up to a true 50 MHz.
- Flash EPROM for users upgradeable BIOS and storage of custom information such as serial numbers or company name.
- Frequency synthesizer – replaces crystals and oscillators for improved reliability.
- Guard banding of clock signals for highest functional reliability and improved EMI characteristics.
- Secondary cache for top performance.
- Diagnostic LED’s – useful for systems with no video controller.
- Up to 64Mb of main memory.
- All connectors accessible internally.
- Shrouded gold plated connectors.
- Highly integrated – includes standard storage and communications controllers.
error correction add more bits than Echelon's proprietary error-correction method, which requires only 6 percent overhead.

Another approach
Adaptive Networks, pursuing its goal of a full data communications network running over powerlines, achieves a 19.2-kbit/s data rate with an error rate of $10^{-9}$. The system supports a range of network options and can address over 64,000 nodes. Maximum range is 4 km.

In its data link layer, Adaptive Networks decomposes messages into short frames with error correction. It uses forward error correction, as well as error detection; each frame must be acknowledged before the next is sent.

Where Echelon employs a contention-based protocol, Adaptive Networks uses token passing. Marketing manager Eric Hughes says, “This technique avoids problems that can occur when nodes fail to detect collisions, provides deterministic access to the network under heavy loads, and makes it easier to verify that a destination node is on the network.”

Because Adaptive Networks sees a market in industrial control, as well as in workstation-based WANS and LANs, it's interesting to compare its data-layer protocol approach to Echelon's. In contrast to PC-based LANs, industrial control networks can have a large population of nodes with light data loading. In such cases, passing tokens to nodes that have nothing to say wastes time. Adaptive Networks' solution is to switch between static token passing and a dynamic scheme.

The decision to switch between schemes depends on network utilization. In the dynamic phase, which is used when utilization is light, nodes join and leave the logical ring based on whether or not they have anything further to transmit. There's a randomized start-time delay to prevent several new nodes from trying to join the ring at once.

Echelon offers complete control modules, including its distributed-intelligence Neuron Chips, as well as bare transceiver modules. The data interface is optimized for the company's proprietary Lonworks architecture, which includes a control-oriented development environment.

Adaptive Networks' powerline communications module has a more conventional RS-232-style data interface. The two-chip ASIC set is also available by itself.

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Adaptive Networks
(617) 497-5150 . . . . . . . . . . .Circle 261

Echelon
(415 ) 855-7400 ........... Circle 262
The use of FPGAs is growing explosively, forcing veteran programmable logic vendors to enhance performance with new-generation products. At the same time, semiconductor giants are being tempted to enter the field.

Only Xilinx (San Jose, CA), however, is backing its boasts with production silicon. This month the company debuts all five members of its SRAM-based, 0.8-µm CMOS XC3100 FPGA family. The new devices take aim at the current speed leaders, antifuse-based pASICs from QuickLogic (Santa Clara, CA), themselves due to be ported to the Cypress Semiconductor (San Jose, CA) 0.65-µm CMOS process. At the same time, Altera (San Jose, CA) is selectively sampling the first members of its new SRAM-based, 0.8-µm CMOS FLEX 8000 family. And Actel (Sunnyvale, CA) is revealing additional performance numbers as its antifuse-based ACT 3 family goes through process characterization in Hewlett-Packard's 0.8-µm CMOS process.

Intel (Santa Clara, CA), meanwhile, will officially enter the FPGA market next year when it samples its 0.8-µm CMOS EPROM FLEX logic family with SRAM option, and Motorola (Phoenix, AZ) announced a few days ago that it has concluded a licensing agreement with UK-based Pilkington Microelectronics Ltd. for its fine-grained, dynamically programmable logic device technology. In so doing, Motorola has followed the lead of GEC Plessey Semiconductors and Toshiba.

With a process more performance- than density-oriented, Xilinx has doubled the speed of its earlier devices without burdening users with a new architecture or software changes. By making its XC3100 family pin- and software-compatible with 1,300- to 5,000-gate XC3000 devices, the company makes it possible for users such as Howard Goetz to make direct plug-in replacements for higher speed. Goetz, hardware design manager at the Graphics, Printing and Imaging Division of Tektronix (Wilsonville, OR), was using a Xilinx 3090 for memory management in a printer product and was a long accumulator that stretched through seven configurable logic blocks. "I can operate with one wait state now rather than two," he reports.

With the introduction of its new parts, Xilinx also claims to have unseated QuickLogic as the FPGA speed leader. System speeds of 50 to 80 MHz prove, says Xilinx, that you don't have to go to exotic antifuse-based processes for high performance. FPGA architectures that use antifuse elements as programming switches are much more difficult to scale, according to Xilinx, than SRAM-based FPGAs that use transistors as switches. In going from 1 µm for its 3000 devices to 0.8 µm for its 3100 devices, Xilinx says it's cut interconnect element parasitics in half. And while today's antifuse architectures have limited buffering, resulting in significant variations in delay depending on fanout, Xilinx logic blocks have large output buffers that eliminate most fanout dependency.

To prove its point about variation in delays due to fanout, Xilinx gives path-delay elements from pin to pin for 3100 parts as compared to QuickLogic pASICs. The figures show that the 3100 family can achieve 9- to 11-ns pin-to-pin delays, almost independently of internal fanout, whereas QuickLogic delays increase substantially with high fanout. QuickLogic president and CEO David Laws counters this by noting that with the asymptotic waveform evaluation (AWE) technique, you can use QuickLogic's pASIC toolkit to selectively program heavily loaded paths to be 20 to 25 percent faster than indicated by the high fanout figures given by Xilinx.

Xilinx also uses JEDEC benchmarks to illustrate a speed advantage over QuickLogic. Pin-to-pin delay for a 9-bit parity circuit implemented in a...
Now You Can See True Colors
Without Getting Soaked.

New full-featured RAMDACs from Brooktree deliver 24-bit true color for cost-conscious PC designers. Introducing four new RAMDACs that span the spectrum of PC applications, from 640x480 VGA systems to 1280x1024 workstation-quality graphics. They've got the right features, the right prices and are available right now.

True Color in a VGA Environment
Unplug Sierra. Plug in our totally compatible Bt481 or Bt482. You'll get 24-bit performance at 16-bit prices.

These new RAMDACs support 15-bit TARGA, 16-bit 5:6:5 and 24-bit true-color formats. They even allow you to switch between VGA and true color on a pixel-by-pixel basis.

Choose the Bt481 if you prefer an external hardware cursor. Or pick the Bt482 for its on-board 32x32x2 cursor — ideal for faster windowing environments.

Workstation Graphics at PC Prices
Introducing the Bt484 and Bt485, our newest mouth-watering RAMDACs. They combine true color with higher resolutions for higher performance graphics subsystems. And they're economical, too.

Bt485 operates at up to 135 MHz to drive pseudo color to 1280x1024 resolutions and gamma correct true color to 1024x768. It has a 64x64x2 cursor and all the serialization and timing to directly interface to a VRAM frame buffer.

Bt484 provides maximum flexibility with its programmable pixel port to provide 256 to 16.8 million colors, on-board 32x32x2 cursor and supports both interlaced and non-interlaced monitors.

<table>
<thead>
<tr>
<th>Resolution</th>
<th>Bt481/Bt482</th>
<th>Workstation RAMDACs</th>
</tr>
</thead>
<tbody>
<tr>
<td>640x480</td>
<td></td>
<td></td>
</tr>
<tr>
<td>800x600</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1024x768</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1280x1024</td>
<td>Bt485</td>
<td></td>
</tr>
</tbody>
</table>

Call Brooktree at 1-800-VIDEO-IC for technical details and pricing today.
Brooktree Corp., 9950 Barnes Canyon Road, San Diego, CA 92121, (619) 452-7580, FAX (619) 597-0673.

©1992 Brooktree Corporation. Brand names or product names mentioned herein may be trademarks or registered trademarks of their respective companies.
With its XC3100 family, Xilinx claims to have unseated Quicklogic pASICs as FPGA speed leader, giving as proof these comparative path-delay figures, which show significant variations in QuickLogic delays depending on fanout. With the application of the asymptotic waveform evaluation technique to selectively program heavily loaded nets, pASICs will run 20 to 25 percent faster than these figures indicate, according to QuickLogic president David Laws. (Interconnect delays for typical paths are estimated at an additional 3 ns for both manufacturers.)

3100, for example, is 12.9 ns, a 39 percent improvement over a pASIC's 21-ns delay. Specific benchmarks can be selected to prove a competitive point, responds Laws. "QuickLogic did the 9-bit parity plus other JEDEC benchmarks to illustrate density, not performance, in response to a specific user's request. For demonstrating performance, the PREP benchmarks, when they're available, will be much better," he adds.

In the meantime, the semiconductor benchmark group called PREP, for Programmable Electronics Performance, is due to have its first ballot on a list of proposed benchmarks that will help you compare various FPGA architectures. After review, the benchmarks will go through a check-and-balance process among FPGA makers before approval and endorsement by the PREP group. A proposed datapath benchmark standard, prepared by QuickLogic and issued by PREP as an example of the

---

**We Build 100% Of Our Memory Cards.**

You never have to wait when Mitsubishi makes your memory cards.

Memory card manufacturing and delivery schedules are directly proportional to availability of the ICs that go inside. At Mitsubishi, we produce 100% of our own DRAMs, SRAMs, flash memory, EEPROMs, OTPROMs, MROMs and peripheral circuitry in our own fully automated manufacturing facilities.

Ranked among the world's top ten semiconductor suppliers, Mitsubishi is always a front-runner in next-generation memory densities and technologies. So, we consistently offer our cards in the highest memory densities and in the current versions of PCMCIA, JEIDA and JEDEC standards. As a technology leader in ASICs, Mitsubishi also supports custom card requirements.

Since we don't have to wait for our ICs, you won't have to wait for your cards.

Call (408) 730-5900, ext. 2214.
The backplane is the single most critical element of a packaging system. Augat offers the broadest selection of quality backplanes available, many in stock.

Our VME prototyping tools continue our long-standing tradition of assisting the development engineer; high performance extender boards speed up critical debugging process and wire-wrap panels provide high-quality prototyping panels for designs using in high-speed devices. VME powered chassis make it easy to test new designs.

We offer a line of high performance VME and VXI backplanes equipped with an innovative 96 pin DIN connector with internal switching. The "Auto Bus Grant" connector provides jumpering between the bus grant daisy chain and the bus arbiter when a card is removed from the VMEbus or VXIbus.

Send us your specifications and we'll quote your requirements on stock, custom or semi-custom product.

We encourage you to get complete technical and delivery information on these or any other Augat components that you require. Call today for your free VME VXI Engineering Design Guide.
data reporting format under consideration, shows a QL12X16 pASIC fitting 12 benchmark units and performing the required function at a worst-case speed of 143 MHz. To illustrate the speed of its 3100 devices, Xilinx has published its own preliminary benchmark results, not yet approved or endorsed by PREP. For a 16-bit prescaled counter implemented in an XC3190, for example, results show the Xilinx part fitting 13 benchmark units and performing at 99 MHz. According to Laws, QuickLogic retains its position of speed leader.

“We’re still in a 1.2-µm process,” he says, adding that he anticipates a speed improvement of 20 to 25 percent for QuickLogic pASICs when ported to Cypress Semiconductor’s 0.65-µm process. Under the QuickLogic/Cypress agreement, Cypress will be a source for QuickLogic pASICs, spanning densities from 1,000 to 20,000 usable gates and beyond. The first product available will be a 4,000-gate pASIC in a high-pin-count package. Laws expects die size to decrease dramatically—perhaps by as much as half—to make pASICs cost-competitive. Samples will be available the first half of next year.

Interconnect impedance
What about Xilinx’s claim that the RC delay in antifuse-based processes doesn’t consistently decrease when a process migrates to finer device geometries—and that the resistance and capacitance in the antifuse-based Actel devices haven’t budged since Actel introduced its very first device? QuickLogic’s Laws counters that when pASICs are scaled to 0.65 µm, the resistance (determined by the impedance of the antifuse) will be about the same, but capacitance should go down significantly. In addition, with AWE techniques, the resistance of ViaLink interconnects in the most heavily loaded nets can be reduced to less than 50 Ω.

Warren Miller, Actel’s product planning and applications manager, says that his company has indeed improved interconnect impedance in each product generation. In fact, for the forthcoming 0.8-µm, 1,000- to 10,000-plus-gate ACT 3 devices, the interconnect impedance is 200 Ω and 6 fF, vs 500 Ω and 16 fF for the 2-µm ACT 1 devices.

Another delay factor is the number of antifuses or switches a signal must travel through to get from source to destination. By making architectural changes, Miller says Actel has reduced clock-to-output time from 30 ns in the ACT 1 family to 10 ns for the ACT 3 family. And still another indication of performance improvement is logic module speed, which Miller claims has been reduced from 5.4 ns in ACT 1 to 3 ns for ACT 3.

Deterministic delays
For the interconnects in its new SRAM-based, register-intensive Flexible Logic Element Matrix, or FLEX,
Think Performance.

400,000 gates

Think Mitsubishi Gate Arrays.

Before you design your next gate array, or even your first, you've got to think about performance. Your very next thought ought to be: Mitsubishi Gate Arrays.

Mitsubishi's triple-layer metal, 0.8µm gate arrays offer 400,000 gates with over 60% utilization, and a typical loaded delay as fast as 215 picoseconds. We also give you up to 512 I/OS and pin counts as high as 576 in our exclusive µPitch TAB™ packaging.

We also offer design kits for the industry's most popular workstations, from logic synthesis, to simulation, to automatic test pattern generation (ATPG). So you can design on your own workstation or ours.

Mitsubishi offers both local design support and the global resources of a stable, well-capitalized company. As one of the world's top 10 semiconductor suppliers, we've been in the ASIC business over 15 years and we're continuing to invest in technologies for the next decade.

When you think gate arrays, think performance. Then think Mitsubishi. You'll be glad you did.

Phone (408) 730-5900 ext. 2106
I TECHNOLOGY DIRECTIONS

8000 family of parts with 4,000 to 24,000 usable gates, Altera is using what it calls the FastTrack interconnect scheme. FastTrack consists of dedicated metal lines that traverse the entire device in both horizontal and vertical directions, providing a predictable across-the-chip interconnect delay of 9 ns. With 70-MHz in-system performance, the first of the new devices, the 12,000 usable-gate EPF81188 (with 1,188 flip-flops) will sample next quarter, with production quantities expected by the second quarter of next year.

Intel is readying the first of its EPROM-based family with SRAM option for first-quarter sampling. With deterministic 10-ns pin-to-pin delays and 80-MHz system clock frequencies, the iFX780 consists of eight configurable function blocks linked by a 100-percent-connectable matrix. According to Intel, each block can be defined either as a 24V10 logic block or as a 128 x 10 SRAM, providing approximately 5,000 gates of logic. SRAM bits are initialized by on-chip, non-volatile configuration cells during power-up.

Intel's FlexLogic family supports JTAG and provides in-circuit reconfiguration and programming through the use of the four-pin JTAG test port. When a final version of the design is confirmed, it can be programmed into the non-volatile cells so the configuration won't be lost even when power is turned off.

According to Motorola, its version of Pilkington's fourth-generation architecture will include enhanced speed and performance, increased flexibility to reprogram all or part of a chip very quickly and a very high registers-to-logic ratio, especially useful for sequential operations. The architectural similarity between Pilkington's fine-grained FPGAs and Motorola's metal-programmed gate arrays is expected to facilitate migration from FPGAs to gate arrays. Initial sampling of Motorola's 0.8-µm FPGAs, likely at the 5,000 and 10,000 usable-gate level, is expected in the fall of next year.

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Actel (408) 739-1010 Circle 253
Altera (408) 984-2800 Circle 254
Cypress Semiconductor (408) 943-2600 Circle 255
Intel (408) 987-7953 Circle 256
Motorola (602) 821-4000 Circle 257
QuickLogic (408) 987-2000 Circle 258
Xilinx (408) 559-7778 Circle 259

Real-Time DSP.

A ffordable real-time Digital Signal Processing becomes a reality with Vigra's high-performance digital audio boards for VME and SBus. You'll find exclusive features such as programmable coding and sampling rates from high-fidelity DAT or CD performance down to telephone bandwidths (16-bit linear to 4-bit ADPCM).

Each board has a 56001 DSP for each audio channel, plus multi-ported store-and-forward RAM, on-board firmware in EPROM, and direct audio inputs and outputs. Vigra's unique DSP expansion bus provides an easy method for adding multiple channels and customized analog front ends.

For post-acquisition processing, use Vigra's Audio Editing Toolkit to make seamless splices and dazzling dubs — ideal for preparing interactive audio such as flight simulation, voice synthesis and communication response systems. Vigra's board audio/DSP product line and custom capability assure you just the right match for your application. Call us today, and discover why Vigra is the leader in board-level audio.

4901 Morena Blvd., Bldg. 502, San Diego, CA 92117 (619) 483-1197 FAX (619) 483-7551

CIRCLE NO. 39

60 NOVEMBER 1992 COMPUTER DESIGN
Introducing the real-time development system that won't drive you to drink.

Thanks to Spectra, you no longer need to rely on caffeine or those gooey simple carbohydrates to get your job done. That's because Spectra was designed to speed up software development. Not your heart rate.

Spectra is a bona fide breakthrough in real-time technology. With cross-development features that have never existed before. The Spectra tools work for all real-time applications. From bare machines to complex systems. From device drivers to multithreaded applications. And from microcontrollers to high-end microprocessors. So now, even lightweight targets can have heavyweight tools.

What's more, Spectra's Virtual Target lets you debug your application on the host before your hardware is ready. All of which makes Spectra ideal for custom designs.

And because the Spectra system is truly open, it supports our tools, your tools and third party tools. Finally, Spectra offers a 100% VRTX compatible, scalable run-time that can be tailored to your application.

So if you're ready to kick the caffeine habit, call 800-321-2636. Now, if we could just figure out a way to get you to lay off the Twinkies.
CALL FOR PAPERS:

APPLICATIONS MAKE THE DIFFERENCE AT ECC

THE ATTENDEES

ECC differs from other industry events because it focuses on providing solutions for a variety of embedded computer applications rather than focusing on technology alone or products alone. Developing these applications and finding the best solutions brings into play single-chip microprocessor and microcontroller implementations; custom and semicustom board designs; standard bus-based single-board computers and peripheral boards; operating systems, real-time kernels and compilers; development systems and debugging tools; embedded PCs, embedded workstations and even embedded microcomputers.

ECC attendees are intimately involved in the design, development and integration of a broad range of products and systems based on embedded computers.

ECC attendees are working in all major industries, where they are designing, developing and building a full spectrum of products and systems:

- In the computer industry, developing workstations and larger computers and making decisions about proprietary buses, open architecture buses or bus-less approaches.
- In process control and automation, developing systems for motor control, process measurement and control, machine vision, robotics and manufacturing automation, traffic control, etc.
- In communications, developing systems for use in cellular communications, PBXs, multiplexers, local area networks and wide area networks, etc.
- In the military/aerospace and avionics industries, building equipment and systems for communications, command and control (C3), weapons guidance and control, simulation, airborne and ground-based flight-control systems, etc.
- In the test, measurement and instrumentation industry, where equipment and systems are being built for product testing, maintenance and service applications, diagnostics (including medical), resource exploration, etc.
- Research and development, where scientists and engineers are designing equipment and systems for data acquisition, analysis and simulation that range from benchtop systems to space stations.

THE PROGRAM

ECC's technical program has been designed to provide attendees with the practical information they need to incorporate embedded computers in an end product or subsystem. These embedded computers can take the form of dedicated microcontrollers; sophisticated 32-bit CISC or RISC processors; off-the-shelf or customized SBCs; standalone SBCs; standard bus-based subsystems; or OEM workstation, desktop or industrial computer platforms.

While the Technical Program Committee will entertain proposals for presentations covering a broad range of embedded computer approaches, special consideration will be given to proposals dealing with the following major areas of concern:

SYSTEM ARCHITECTURES

Presentations in this category will deal with interprocessor and memory architectures, custom and semicustom system implementations, and loosely and tightly coupled software and hardware models. This section will include a discussion of chip sets for "standard-architecture" machines such as the X86-, SPARC- or MIPS-based workstations and the features that make them suited, or unsuited, to embedded applications. Some other areas of interest are:

- PCs (80X86, P5) in embedded applications
- RISC architectures (Alpha, HP-PA, MIPS, SPARC, 88K) in embedded applications
- Integrating processor, memory and I/O on stand alone SBCs
- Memory architectures with or without cache
- Symmetrical and asymmetrical multiprocessing
- Live-insertion, fault-tolerant, high-availability computing

INTERFACES AND STANDARDS

This track will deal with local on-board interfaces, addressing issues such as architectural considerations, transceiver considerations (cost, power, space, time-to-market) and implementations, current and emerging standards such as PCI and PCMCIA as well as more conventional mezzanine-I/O buses such as IndustryPacks, SBus, MX bus and others. Particular areas of concern include:

- Standard mezzanine/daughter boards
- SBus, TURBOchannel and other workstation I/O buses
- 80X86 (P5) peripheral interfaces
- Networking interfaces such as Ethernet, ATM and SONET
- Peripheral interfaces such as SCSI, HiPPI, and FiberChannel
- MCM standards and interprocessor module buses
A FOCUS ON SOLUTIONS

INTERCONNECT ARCHITECTURES

The approaches to interconnecting board-level subsystems are undergoing a revolution, including the development of new standards such as PCI/104, SCI (Scalable Computer Interface) and Futurebus+, as well as major changes and enhancements to such well-established standards such as VME and Multibus II. In addition, there are many other approaches vying for the embedded market such as ESP (Extra Small Package), various STD approaches, G64 and others. Rapidly changing semiconductor technology is forcing changes in bus and interface technology which are reflected in:
• VMEbus, Multibus, Futurebus+, STD/STD32
• Custom and semicustom implementations
• High-performance backplanes
• Bridges and intercrate communications

SOFTWARE AND DEVELOPMENT TOOLS

Because embedded computer applications involve real-time processing, the major software focus of ECC will be real-time issues. Special emphasis will be given to multiprocessing in real-time using both traditional and Windows-based operating systems. Also of interest to attendees are:
• Real-time OS and kernels
• Real-time DOS
• Windows for embedded and real-time applications
• Multiprocessing with DOS and other real-time OSs
• High-performance optimized compilation
• POSIX and POSIX compatibility
• Communications protocols/standards
• Ada in military and nonmilitary applications

Proposals will be considered for presentations on any of the above topics, as well as on any other topics related to the design, programming and application of embedded computer products, subsystems or systems.

HOW YOU CAN PARTICIPATE

You may participate in the ECC Technical Program by submitting a proposal for either a one-hour lecture-type presentation, a 20-minute application-focused paper, or a longer tutorial. Please submit your proposal no later than November 20, 1992. The proposal should be no longer than one page and consist of a short abstract that summarizes the content and goals of the presentation, and a brief outline of the major topics covered by the presentation. Presenters must be technically qualified and able to answer questions from attendees. A short biography of the presenter, detailing his or her technical background and accomplishments must accompany the proposal.

Acceptance of proposed presentations will be made by December 2, 1992. A complete copy of the presentation, including all visuals and graphics, for publication in the Conference Proceedings must be provided by March 1, 1993. Presentations given at ECC will be published in the Proceedings and copyright shall be assigned to Computer Design/PennWell Publishing Company.

THE FORMAT

A combination of one-hour presentations, application-focused multi-paper sessions and tutorials will address a broad range of topics of importance to engineers and engineering managers designing both the hardware and software for embedded computers and subsystems.
• Tutorials are extended presentations intended to provide attendees with an in-depth understanding of core technologies used in embedded computers.
• Individual presentations are focused on various aspects of applying new or emerging technologies and products to solving specific problems in designing products or subsystems using embedded computers. Special consideration will be given to presentations that emphasize make-or-buy trade-offs in specific applications.
• Multipaper sessions consist of several shorter papers that focus on the implementation of embedded computing in specific application areas, including:
  • Medical instrumentation
  • Vehicular traffic control
  • Signal processing/data acquisition/DSP
  • Automated vehicles
  • Machine control
  • Graphics
  • Low-power and portable applications
  • Imaging
  • Visual inspection
  • Virtual reality
  • Military C3I
  • Communications
  • Peripheral interface and control
  • Process control
  • Laboratory automation
  • Multimedia
  • Networking

COMPUTER DESIGN • One Technology Park Drive • P.O. Box 990 • Westford, MA 01886
Tel: 508-392-2124 • 800-223-4259 • Fax: 508-692-7780

CIRCLE NO. 41
All the makings of a masterpiece.

Before your name goes on it, you've got to depend on what goes in it. That's why you should know IBM has the quality parts, products, technology, software and services you need for all your greatest creations.

With our manufacturing sites around the world, you can count on IBM for just about whatever you need, whenever and wherever you need it. We can supply OEM versions of just about everything in our product line—at competitive prices. All backed with a range of services and support unmatched in the business. OEM versions of everything from 1.2GB disk drives, Optical Link Cards and Token-Ring MINI cards, to OS/2® 2.0 and ESCON™ products, all the way to OEM versions of complete systems like the PS/2® Model 95 and various RISC System/6000™ models, and more. And everything carries IBM's reputation for quality that's earned all kinds of recognition, including the prestigious Malcolm Baldrige National Quality Award for the manufacturing process of the IBM AS/400®.

With IBM as your OEM supplier, you can create your own masterpiece. For a free OEM product reference guide or to have an IBM OEM marketing representative contact you, call 1 800 486-0974, send the attached reply card by mail, or fax it to 1 800 394-0974.

When you think OEM, think IBM.

- A wide range of OEM offerings.
- Award-winning technology and quality.
- Competitive pricing and responsiveness.
- Worldwide availability.
IC vendors integrate PC telecommunication services

First came fax-modem combo chips. Now IC manufacturers are attempting to integrate voice messaging and caller ID. They’re thinking about color fax and video conferencing. Are there limits beyond which the technology envelope can’t be stretched?

Stephan Ohr, Contributing Editor

There’s little doubt that the desktop PC of the very near future will be a communications center as well as a data-gathering and document-publishing center. Business users will set up their PCs to send and receive not just modem data and faxes, but voice messages as well.

In certain parts of the United States, it’s now possible to automatically identify the person who calls you. With the aid of Windows-based software, you can pull a file on the caller and put all relevant information (including the caller’s picture) on your computer screen—even before you pick up the phone.

Data-compression techniques are on the horizon that will let PCs send and receive color images of photographic quality. In the more distant but still foreseeable future, these same techniques will bring moving video images to the desktop PC for video conferences.

What isn’t clear at this point is which telecommunications media will be used to carry multiple communications services. The standard analog telephone line is optimized for a voice-frequency signal with a bandwidth of 3 kHz. With the help of wave shaping, echo cancellation and other digital signal-processing techniques, you can transmit facsimile or modem data at 14,400 bits/s—or almost five times the bandwidth of the phone line. In fact, modem manufacturers are currently developing a standard for 28.8-kbit/s data rates. In addition, it’s possible for a receiver to automatically distinguish between voice, modem and facsimile calls. The receiver can also capture a dual-tone multifrequency (DTMF) signal that communicates the phone number of the call originator.

But at this point the PC-as-communications-center idea begins to break down. The call-recognition service known as caller ID is legal in only a few states in this country. Analog phone lines, moreover, don’t have the band-
**Technology Focus: Integrated Telecoms**

Fax-modem architectures are composed of three major building blocks: an analog-digital front end (transceiver) which interfaces with the telephone line, a waveshaper or DSP controller and a controller that interfaces the modem to the PC or host computer. Voice-compression algorithms and protocols distinguishing fax, modem and voice calls, as well as a number of other functions, are all embedded in the firmware attached to the control processor. An isolation transformer, using a direct access arrangement (DAA), ensures that faulty telephone equipment won’t damage the phone line.

**Software is the issue**

“Much of this is a software issue,” insists Greg Lang, product manager for Satisfaxtion fax-modem boards from Intel (Santa Clara, CA). “Two years ago, the software supporting fax-modem boards was just a ‘viewer.’ Every page you sent or received was big, fat, slow, and required a ton of horsepower to process. Now the software is much more efficient. There’s even software with OCR [optical character recognition] which converts a fax image to ASCII text for editing.”

According to Lang, as far as the user’s concerned, the value of a fax-modem board isn’t in the silicon, but in the software. Integrated fax-modem chips have little to do with page formatting and printing, so a higher telecom data rate doesn’t result in faster printouts. From the point of view of the board builder, semiconductor manufacturers have made it easier for them to offer competitive products by providing devices with greater integration of functions, higher modem transmission speed and lower cost. “The current generation of fax-modem data pumps,” says Lang, “is approximately 30 percent as expensive as a board, down from 60 percent just two years ago.”

Integration of voice-messaging functions is something that Lang believes users will demand in years to come. Fred Kamp, director of communication products marketing at Sierra Semiconductor (San Jose, CA), agrees, pointing out that such integration will let small, home-based businesses provide the same kind of voice mail services now used by larger companies. In addition to digital answering machine services, the extra storage space and horsepower of the PC can be used to supply a menu of services to the caller, including a send-fax capability where the caller uses the telephone keypad to identify fax pages to be received.

**Chip sets pull it together**

Sierra’s SQ3214, a four-chip set introduced last month, combines high-speed modem and fax data transceivers and voice messaging with caller ID. The XR-29V00 from Exar (San Jose, CA) is a two-chip set introduced in April that offers a complete data-pump function for Group III fax, 2.400-bit/s data, voice coding with 4:1 compression, and caller ID. During the summer, Phylon (Fremont, CA) introduced two sets of two-chip fax-modem devices, one a low-power chip set optimized for laptop computers and the other equipped for normal desktop operation. Both sets offer V.17 fax and V.32 bis modem capabilities, with data rates up to 14.4 kbit/s, along with adaptive differential pulse code modulation (ADPCM) voice compression and caller-id functions. With a firmware change, says Phylon vice-president of marketing Sid Bagwe, PHY1001/1002 chips can support the new V.34 standard of 28.8 kbit/s, due for ratification by the Consultative Committee for In...
The path to top-down design can be anything but straight and narrow. And once you get off track, you can get into all sorts of trouble. The ASIC wilderness is littered with good point tools that somehow fail to provide an integrated solution.

COMPASS Design Automation knows all about the rules of the road. That's because we've been down it more than any other EDA company. We've developed the most integrated top-down ASIC solution in the industry, from first concept to first silicon. Supporting even the largest and most complex designs that require a million gates and more.

Simply put, we save you time. Starting with an easy-to-use integrated graphical HDL and synthesis environment through comprehensive cell-based and gate array libraries. And all the automated tools you need to move on down the design road.

So chart your course today. For more information, please circle the reader number, call (800) 433-4880, ext. 7097 or fax your request to (408) 434-7977.

© 1992 COMPASS Design Automation, Inc. COMPASS and the COMPASS logo are registered trademarks of COMPASS Design Automation, Inc.
INTERNATIONAL TELEPHONE AND TELEGRAPHY (CCITT) NEXT YEAR.

Phylog has been particularly successful at developing front-end analog interface chips for modem and voice communications. Users include Shiva (Cambridge, MA), with its NetModem/E, and Hayes Microcomputer Products (Norcross, GA), with Ultra 144, a 14.4-kbit/s modem. Helios Systems (San Jose, CA) incorporated the Phylog chip set into the first fax-modem combo its NetModem/E, and Hayes incorporated the Phylon chip set for Sun Microsystems' SBus.

The processing power of a Sun workstation all but eliminates page formatting delays that continue to exist in the PC environment.

Other highly integrated chip sets are available from Rockwell International (Newport Beach, CA) and Cirrus Logic (Fremont, CA). Rockwell's two-chip RC144ACL and Cirrus' two-chip CL-MD1424AT provide fax, modem and voice coding and compression, although not caller ID.

THREE-WAY SPLIT

These chip sets are composed of three major building blocks: an analog front end (transceiver) interfacing with the telephone line, a waveshaper or DSP controller, and a modem. Cirrus Logic (Fremont, CA) incorporated the Phylog chip set into the first fax-modem combo board for Sun Microsystems' SBus. The processing power of a Sun workstation all but eliminates page formatting delays that continue to exist in the PC environment.

Other highly integrated chip sets are available from Rockwell International (Newport Beach, CA) and Cirrus Logic (Fremont, CA). Rockwell's two-chip RC144ACL and Cirrus' two-chip CL-MD1424AT provide fax, modem and voice coding and compression, although not caller ID.

THREE-WAY SPLIT

These chip sets are composed of three major building blocks: an analog front end (transceiver) interfacing with the telephone line, a waveshaper or DSP controller, and a controller that interfaces the modem to the PC or host computer. The four chips introduced by Sierra include an analog front end, DSP waveshaper, dedicated controller, and interface logic. Cirrus claims full integration of all functions with just two chips—three, if you add error-correction and data-compression functions. Exar, Phylog and Rockwell's two-chip sets partition modem functions between a DSP chip and an analog-digital front end. To interface properly to the host, a separate microcontroller may or may not be required.

For voice coding, a fourth element, a voice encoder/decoder converter, is required. This device converts telephone voice frequencies into data patterns that can be stored on a hard disk; it also converts digitized messages back into voice output that can be played back over the telephone line. With most chip sets, this capability is incorporated into the analog front end. ADPCM compression algorithms are applied to the digitized voice patterns to minimize the amount of disk space required; these algorithms, along with protocols to distinguish, fax, modem and voice calls, caller ID, DTMF dialing, Hayes-type AT commands from the host computer, Microcom Networking Protocols (MNPs), and V.42 bis error correction, are all embedded in the firmware attached to the control processor.

PUMPING DATA

A modem's analog-digital front end, typically called a data pump, is a transmitter/receiver combination that puts a basic carrier frequency onto the telephone line and varies its amplitude, frequency or phase up or down to signify changes in the serial data pattern. Modems that transmit data at rates below the 3,000-Hz bandwidth of the telephone line (at 2,400 bits/s, for example) use either frequency-shift keying (FSK) or differential phase-shift keying (DPSK) to indicate changes in logic state. Modems that transmit data at rates above the 3-kHz bandwidth use DSP techniques to shape the waveform of an 1,800-Hz carrier frequency. A single

MODÉM STANDARDS

<table>
<thead>
<tr>
<th>Standard</th>
<th>Fax/Data</th>
<th>Bits/s</th>
<th>Modulation</th>
<th>Baud rate (symbols/s)</th>
<th>Carrier frequency originate-M/S</th>
<th>Constellation points</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bell</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>103/108/113</td>
<td>D</td>
<td>300</td>
<td>FSK</td>
<td>300</td>
<td>1270/1070</td>
<td>2225/2025</td>
</tr>
<tr>
<td>202</td>
<td>D</td>
<td>1200</td>
<td>FSK</td>
<td>1200</td>
<td>1200/2400</td>
<td></td>
</tr>
<tr>
<td>212A</td>
<td>D</td>
<td>1200</td>
<td>DPSK</td>
<td>600</td>
<td>1200</td>
<td>2400</td>
</tr>
<tr>
<td>201</td>
<td>D</td>
<td>2400</td>
<td>DPSK</td>
<td>1200</td>
<td>1800</td>
<td></td>
</tr>
<tr>
<td>208</td>
<td>D</td>
<td>4800</td>
<td>QAM</td>
<td>1600</td>
<td>1600</td>
<td>1800</td>
</tr>
<tr>
<td><strong>CCITT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V.17</td>
<td>F</td>
<td>14400</td>
<td>TCM</td>
<td>2400</td>
<td>1800</td>
<td>128</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12000</td>
<td>TCM</td>
<td>2400</td>
<td>1800</td>
<td>64</td>
</tr>
<tr>
<td></td>
<td></td>
<td>9600</td>
<td>TCM</td>
<td>2400</td>
<td>1800</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7200</td>
<td>TCM</td>
<td>2400</td>
<td>1800</td>
<td>16</td>
</tr>
<tr>
<td>V.21</td>
<td>D</td>
<td>300</td>
<td>FSK</td>
<td>300</td>
<td>980/1180</td>
<td>1650/1850</td>
</tr>
<tr>
<td>V.21 ch2</td>
<td>F</td>
<td>300</td>
<td>FSK</td>
<td>300</td>
<td>1650/1850</td>
<td></td>
</tr>
<tr>
<td>V.22</td>
<td>D</td>
<td>1200</td>
<td>DPSK</td>
<td>600</td>
<td>1200</td>
<td>2400</td>
</tr>
<tr>
<td>V.22 bs</td>
<td>D</td>
<td>2400</td>
<td>QAM</td>
<td>600</td>
<td>1200</td>
<td>2400</td>
</tr>
<tr>
<td>V.23</td>
<td>D</td>
<td>1200</td>
<td>fsw</td>
<td>FSK</td>
<td>300</td>
<td>75</td>
</tr>
<tr>
<td></td>
<td></td>
<td>75 rev</td>
<td>FSK</td>
<td>75</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V.26</td>
<td>D</td>
<td>2400</td>
<td>DPSK</td>
<td>1200</td>
<td>1800</td>
<td>4</td>
</tr>
<tr>
<td>V.27 ter</td>
<td>F</td>
<td>4800</td>
<td>DPSK</td>
<td>1600</td>
<td>1800</td>
<td>8</td>
</tr>
<tr>
<td>V.29</td>
<td>F</td>
<td>9600</td>
<td>QAM</td>
<td>2400</td>
<td>1800</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>9600</td>
<td>QAM</td>
<td>2400</td>
<td>1800</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4800</td>
<td>QAM</td>
<td>2400</td>
<td>1800</td>
<td>4</td>
</tr>
<tr>
<td>V.32</td>
<td>D</td>
<td>9600</td>
<td>QAM</td>
<td>2400</td>
<td>1800</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4800</td>
<td>QAM</td>
<td>2400</td>
<td>1800</td>
<td>4</td>
</tr>
<tr>
<td>V.32 bis</td>
<td>D</td>
<td>14400</td>
<td>TCM</td>
<td>2400</td>
<td>1800</td>
<td>128</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12000</td>
<td>TCM</td>
<td>2400</td>
<td>1800</td>
<td>64</td>
</tr>
<tr>
<td></td>
<td></td>
<td>9600</td>
<td>TCM</td>
<td>2400</td>
<td>1800</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7200</td>
<td>TCM</td>
<td>2400</td>
<td>1800</td>
<td>16</td>
</tr>
</tbody>
</table>

Chart courtesy of Cirrus Logic, "Modem/Fax Technology Guide" (November 1991)
Just What Your Customers Need, Another Outlet For Their Creativity.

What’s in? Video Out. Putting video to a VCR and displaying video on a composite monitor are the newest capabilities every computer will need to compete in the Multimedia Age.

Now you’re just a single chip away from adding Video Out to your very next computer design. Introducing Bt858, a monolithic digital device that packs in a board full of analog circuitry and puts out studio quality composite video.

Bt858 is a tweakless all-digital chip that bridges the video gap between RGB computers and composite or S-VHS outputs in the NTSC/PAL formats. It accepts multi-format digital inputs from 24, 16 or 15-bit RGB, 24 and 16-bit YCrCb and 8-bit VGA.

And because it has a programmable clock rate it adjusts for the 1:1 square pixels in computers and 4:3 rectangular pixels on TV without distortion.

Bt858 gives your system an image quality advantage, too. Studio quality output is a step above tape decks and TV monitors so images always look “first generation.”

You’ve read the book. Now see the picture. Call 1-800-VIDEO IC and we’ll send you “The Ins and Outs of Video Out,” a revealing presentation of Bt858’s capabilities.

That’s all folks.

Brooktree Corporation, 9950 Barnes Canyon Road, San Diego, CA 92121, (619) 452-7580, FAX (619) 452-7294

There are several modem-resident protocols that, like trellis coding, improve transmission over a noisy signal line but also raise the data-transmission rate. The most commonly used are the MNP protocols, developed by Microcom (San Jose, CA) for V.22 bis fax modems, MNP 3 protocol, for example, is used for synchronous bit-oriented, full-duplex data exchanges. By eliminating the start and stop bits in a block data transmission, the protocol obtains a throughput of approximately 108 percent. MNP 4 is similar to MNP 3, but also has adaptive block sizing and data phase optimization; its throughput efficiency is approximately 120 percent. MNP 5, the most commonly used protocol, adds data-dependent compression to MNP 4. Its throughput is approximately 200 percent—4,800 bits/s—at a 1.6:1 compression ratio.

The V.42 bis is a CCITT error-correction scheme that adds Lempel-Ziv data compression to the link access protocol modem, for a 4:1 data-compression ratio. (The Rockwell RC144AACL, in addition, will support MNP 10, a protocol useful for data transmission over cellular telephone lines or under other adverse conditions.)

The ability to shape the phase of the carrier signal in response to multiple protocols depends on a DSP. This can be an add-on device. Zilog (Campbell, CA), for example, manufacturers a mixed-signal processor with modem, fax and voice firmware. The Z89120 integrates a 16-bit DSP, an 8-bit microcontroller, an A/D converter, and a pulse width modulation D/A converter on a single chip. The firmware permits host interface and control using the AT command set, with voice and fax extensions for the Z8 controller. The modulation and demodulation algorithms performed by the DSP provide firmware support for full-duplex V.22 bis modems with operating speeds of 9,600 bits/s. Voice compression is performed at 7 kbits/s using the DSP and data converters. Motorola (Austin, TX) also offers the 68000-based 68302 as a multiprotocol communications controller.

The caller ID controversy

Caller ID, on the other hand, is a firmware function. “It’s relatively simple to implement,” says George Urbani, communications business unit manager for Cirrus Logic, which doesn’t offer caller ID functions at this time. “You simply capture the V.21 demodulation scheme between the first and second ring.” The phone number of the call initiator, in other words, is embedded in a signal from the local telephone company’s central switch.

The problem, as Urbani explains, is that the right to offer caller ID functions—the legality of caller ID, to put it another way—is restricted in many states, including California. There are many professional groups that believe caller ID constitutes a violation of privacy. The argument goes that the identity of obscene callers and unwanted solicitors should be protected. These groups lobby against the proliferation of the service.

This means that if you subscribe to the caller ID service in New Jersey,
We Like to Illustrate How Well We Adapt

Link Your Sun Sparc, DEC, IBM, PC-AT, ISA or EISA Bus to VMEbus Computers.

VMIC's new family of VMEbus adapters gives you the ability to easily connect your workstation to your VMEbus. VMIC's new adapter family links Sun Sparc Stations, DEC 5000 Workstations, IBM 6000 Series Workstations, and machines based on PC-AT, ISA or EISA bus to VMEbus computers.

The product line supports master(s) and slave(s) in the VMEbus chassis and features a software-controlled dynamic address mapping mode. A software transparent mode is supported at power-up and requires no additional initialization.

VMIC also offers a Reflective Memory product line. Call VMIC toll-free and let us illustrate how easy it is to connect you.

1-800-322-3616

VMIC
VME Microsystems
International Corporation
12090 South Memorial Parkway
Huntsville, AL 35803-3308
(205)880-0444 FAX (205)882-0859

CIRCLE NO. 44
TECHNOLOGY FOCUS: INTEGRATED TELECOMICS

The WindowsPhone hardware/software kit is one of the first to take advantage of caller ID services. The system identifies the caller by telephone number, pulls up relevant information about the caller and displays it on the screen, even before you pick up the phone. But, caller ID services aren't legal in every state.

where it's legal, you won't be able to identify a caller from California. Where the service is restricted, "With such restrictions," says Urbani, "caller ID won't live up to its potential."

The IC manufacturers, such as Exar and Sierra, who currently offer call-recognition firmware with their chip sets, are banking that caller ID will be legalized in most business localities and that the regional Bell Operating Companies will provide the necessary identifying tones in the signals that come from their central offices. Exar's marketing manager of communications products, Richard Reifner, for example, believes that caller ID subscriptions will grow at a rate of 12 million per year over the next three years.

Manufacturers of PC insert cards and software are also betting that caller ID will become a vital business service. Data-Cal (Chandler, AZ), for example, has developed a Windows-based hardware/software system which tracks both incoming and outgoing calls to and from a PC host. For outgoing calls, you select a phone number and related files from your database. The computer places the call and automatically records the time spent online. For incoming calls, the WindowsPhone system uses caller ID information to compare the number of the originating caller with numbers in your database. Where there's a match, relevant information on the caller can be brought to the screen, even before you pick up the phone.

Technical restrictions

While caller ID service may be withheld for legal and jurisdictional reasons, there are other telecommunication services that may trip over technical limitations. Armando Geday, Rockwell's director of worldwide marketing, foresees that a number of communications functions will be impeded by the analog phone line. Color fax, for example, currently isn't possible with telephone communications. Apart from a lack of transmission and reception standards, the major difficulty centers on the inability to print a color hard copy. Color fax won't proliferate until inexpensive color printers become available.

The major problem with analog phone service is its bandwidth; it's too narrow to accommodate moving video images or teleconferencing services. The amount of compression needed to transmit video images over existing phone lines would be far too costly. Even V.Fast, at 28.8 kbits/s, is much too slow. The need for video conference services may even dampen the trend toward putting multiple data communications services on standard phone lines.

Local phone company service, almost everyone agrees, doesn't have the bandwidth for video services such as video conferencing. The ISDN (Integrated Services Digital Network) will provide higher transmission bandwidth, while reducing some of the compression requirements for video transmission. While there's currently a movement afoot to make ISDN national, so as to link services between the regions serviced by local Bell Operating Companies, implementation has been slow. Some semiconductor manufacturers, such as National Semiconductor (Santa Clara, CA) and SGS-Thomson (Phoenix, AZ), have made substantial investments in ISDN; others such as Exar are concentrating on the primary-rate trunk lines. Exar has formed an alliance with AT&T Microelectronics (Berkeley Heights, NJ), in fact, to create T-1 trunk-line products that will operate at 1.544 Mbits/s. But with support so divided, few analysts foresee ISDN reaching large numbers of business PC users anytime soon.

Cirrus Logic's Urbani voices a colorful personal opinion about all this: "The phone company runs its equipment until it dies. They'll use vacuum tubes if you let them," he says. "As a consequence, ISDN was never fully implemented, and much of the technology it was supposed to embody has passed. Perhaps the phone company's new interest in the data and TV businesses will speed up implementation of ISDN."

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

<table>
<thead>
<tr>
<th>Company</th>
<th>Number</th>
<th>Circle</th>
</tr>
</thead>
<tbody>
<tr>
<td>AT&amp;T Microelectronics</td>
<td>(908) 771-3291</td>
<td>230</td>
</tr>
<tr>
<td>Cirrus Logic</td>
<td>(510) 623-8300</td>
<td>231</td>
</tr>
<tr>
<td>Exar</td>
<td>(408) 434-6400</td>
<td>232</td>
</tr>
<tr>
<td>Motorola</td>
<td>(512) 891-3434</td>
<td>233</td>
</tr>
<tr>
<td>National Semiconductor</td>
<td>(408) 721-3289</td>
<td>234</td>
</tr>
<tr>
<td>PhyPhon</td>
<td>(510) 656-2606</td>
<td>235</td>
</tr>
<tr>
<td>Rockwell International</td>
<td>(800) 854-8099</td>
<td>236</td>
</tr>
<tr>
<td>SGS-Thomson Microelectronics</td>
<td>(602) 867-6100</td>
<td>237</td>
</tr>
<tr>
<td>Sierra Semiconductor</td>
<td>(408) 263-9300</td>
<td>238</td>
</tr>
<tr>
<td>Zilog</td>
<td>(408) 370-8000</td>
<td>239</td>
</tr>
</tbody>
</table>

72 NOVEMBER 1992 COMPUTER DESIGN
Windows Power Debugging ... for Real-Time Targets

WATCHPOINT® is a Microsoft® Windows®-based high-level language debugger for real-time embedded systems. In real time you can watch:

- Multiple source windows with user-controlled focus!
- Multiple data windows for variables, expressions, registers, memory, the stack, and trace data — with time-interval updating!
- Trace data, and you can examine and set memory, breakpoints, and triggers, all while your program runs!

Watchpoint gives you one-click navigation to routines, variables, and structures. The configuration tool bar puts the tools you need one click away. And accelerator keys give you one-keystroke access to all common commands.

Breakpoint buttons appear on eligible lines. Set, delete, or switch between hardware and software breakpoints with one click.

Automate testing with unique full command capture and replay. Optional command sequence at break and trigger.

Watchpoint’s Help system is the most advanced anywhere. Point to reduced screen images for instant help.

Complex triggers become simple with Watchpoint’s Trigger Setup window. The informative Trace Display window differentiates reads, writes, source, trigger, etc., so you can quickly and easily find what you need.

Watchpoint takes full advantage of Microsoft Windows so you have easy-to-learn direct control over Sophia’s powerful in-circuit emulators.

Call for more information.

Sophia Systems and Technology, 777 California Ave., Palo Alto, CA 94304, TEL: (415) 493-6700 FAX: (415) 493-4648
Sophia Systems Co., Ltd., Shinjuku NS Bldg. 8F, 2-4-1 Nishishinjuku, Shinjuku-ku, Tokyo 163-08, Japan, TEL: (03) 3348-7000 FAX: (03) 3348-2446

Microsoft is a registered trademark and Windows is a trademark of Microsoft Corporation.

Watchpoint is a registered trademark of Sophia Systems and Technology.

©1992 Sophia Systems and Technology.
Your application is first in line with the MVC 16-line Async Commux. It's got processing capacity to spare, thanks to a 16 MIPS RISC, so system power goes to your users—not I/O.

Character processing and buffering is managed on-board by our RISC, so driver calls and host overhead are kept to a minimum. All 16 lines can operate at 38.4 Kbaud. That's over 61,000 characters per second throughput, double the rate of other VMEbus async controllers.

The MVC's advanced features benefit both the integrator and programmer. Port and VMEbus parameters are soft-configured and set line-by-line. Modem control is standard. Full software support is also included, along with diagnostics and a Streams driver.

Advanced memory architecture and high-speed buffering eliminate overruns and port domination. Memory is expandable from 128KB to 1MB, so the MVC handles today's requirements and future application needs.

With over 11 years experience producing advanced storage, communications and memory products, Macrolink delivers the powerful and flexible MVC in 8 and 16 line configurations. Call us today. We won't keep you waiting.

Macrolink Inc., 1500 North Kellogg Drive, Anaheim, California 92807. Phone (714) 777-8800, FAX (714) 777-8807.

Mix & match I/O panels feature DB25 or RJ-45 connectors.
Mezzanine buses gain respect, find new uses

High-density chips and chip sets are bringing more and more functionality to a single board, often reducing system bus requirements. This opens the way for mezzanine boards, not only to increase available board real estate, but to become an integral part of the system architecture—in some cases to the exclusion of system buses.

Warren Andrews, Senior Editor

Once seen as a not-so-reputable fix to system problems, the mezzanine bus is fast becoming a major architectural feature in system design. On one hand, mezzanine buses provide a good way to personalize I/O on standard-bus boards. There's also a growing trend toward a local or mezzanine bus replacing the system bus. This has resulted in a rash of single-board computers (SBCs) with no main system bus, with I/O residing on a number of mezzanine tiles.

Early mezzanine or daughter boards were thought of as kludges, fixes forced by poor initial design. They were necessary but frowned upon—like the soldered-in jumper wires and cut circuit board traces. Such boards were usually ridden with problems related to thermal management and a clean interface to the motherboard.

Mezzanine approaches were also criticized because of questionable reliability. Early connectors and edge-card fingers were suspect and failure-prone. So unreliable were some of these connectors that a critical tool in the serviceperson's kit was a pencil eraser used to burnish plated edge-card contacts.

That period's now behind us, however, because a number of factors have combined to add respectability to daughter board approaches. These include dramatic improvements in connector technology, the availability of modular computers and the growing adherence to hardware and software standards.

Among the factors that have contributed to the growing acceptance and popularity of mezzanine approaches, the most commonly mentioned by users is that mezzanines offer increased circuit density and more efficient use of board real estate. This gives board vendors the ability to customize standard boards for special applications.

Pete Yeatman, president of Radstone Technology (Montvale, NJ), empha-
sires that his company's aim for mezzanine board technology is to provide enhanced functionality with a device that's an integral part of a system. "Mezzanine boards aren't simply something you add on at some future date to increase basic system function," he says. "Mezzanine board functions are a significant part of the system architecture, both in hardware and software."

Radstone's marketing director, Joel Silverman, concurs, commenting that not only do mezzanine buses offer added functionality in terms of additional I/O, they can also off-load the system bus through a separate channel—a local or mezzanine bus. "In many configurations," says Silverman, "a single board's processing power is so great it can call for a number of I/O options beyond the basic system bus. This has resulted in what Radstone calls its Free-Flow system architecture, where VME cards take advantage of the VME system bus, the VSB (VME subsystem bus), one or more SCSI channels, communications channels such as Ethernet, and a local or mezzanine bus channel."

## Gaining respectability

While mezzanine boards may have acquired a bad reputation early on, they seem to have come around to respectability—even with one of the industry's toughest customers, the U.S. military. Radstone modified its PEX and APEX buses to meet military muster, resulting in the company's MXbus. "The philosophy behind MXbus is the same as for the PEX and APEX buses," says Silverman, "only the mechanicals had to be changed. These changes include allowing for conduction cooling and permitting connections to the P2 connector rather than to the front of the board." As is the case with other standard boards adapted to military service, the Radstone concept is to provide standard hardware fitting COTS (commercial off-the-shelf) and NDI (nondevelopmental item) military specifications, and so lower-cost.

In addition to being used for basic I/O, specialized mezzanine buses perform other functions, including serving as coprocessor modules. While the most obvious such modules are the SPARC and Motorola 88000 M bus implementations for multiprocessor, others have been used to compress hundreds of MFlops of performance onto a single VME-sized board.

To increase processor density in very-high-performance multiprocessor systems, for example, Cy-clone Microsystems (New Haven, CT) puts an i960 processor on one of its Squall mezzanine boards, which gives way to other approaches promising more robust I/O.

Intel's (Hillsboro, OR) ilBX, coming after iSBX, had emerged as the next-generation local bus, aimed at providing high-speed memory to CPU boards without the problems associated with system bus latency. Although widely used, ilBX suffered from being applied to problems that were too highly focused and specialized for Multibus II. Intel also introduced the Mix bus a few years ago. This clever attachment scheme for Multibus II lets mount-on modules essentially share the processor bus of a host CPU board. Intel and others have developed a number of Mix modules, yet the cost per module has tended to keep them out of high-volume I/O applications.

## Off the bus

While mezzanine buses have largely been viewed as a board maker's standard bus fix to provide wide-ranging I/O capabilities without changing the basic board, an entirely new architectural approach to embedded computers using them has recently emerged. This approach looks at the system from the viewpoint of the CPU, and uses a local bus rather than a system bus for I/O. This approach differs somewhat from more traditional standard-bus approaches, in that it's more likely to result in general-purpose computer engines steered to particular applications through the I/O.

"More traditional approaches, such as those used by Radstone," says Silverman, "use a board optimized for a specific application, such as high-performance multiprocessor. But while boards may be optimized for an application, it's still only possible to include perhaps 80 percent of what any given customer wants. The remainder can be accommodated with either manufacturer- or customer-built mezzanines."

Over the past several months, several examples of the general-purpose, single-board approach have surfaced. While many system makers have in the past used an SBC with a mezzanine board as I/O or as a personality module, these boards have usually been proprietary, de-
The Fire Control Processor for the M1A2 Abrams Main Battle Tank: one example of Vista Controls' fully mil-qualified RISC-based board-level systems solutions for fire control and gun stabilization. Being manufactured today.

A Cost-Effective Solution...Now
If your system requires NDI (non-developmental item) MIL-SPEC VME/SAVA/1553 boards and chassis, then Vista Controls can supply your needs. Our RISC-based products typically take the place of two to three CISC-based boards, resulting in significant system cost savings. Vista’s NDI hardware and software shorten your leadtime, lower your costs, and reduce your risk—let our RISC lower your risk™

Validated ADA and C
SAVA and 1553
Radiation Hardness
Control Systems
Real-time Kernel
IFTE Test Interface
ATR Chassis
Real-time Communications

With Quality and Support Built-in
Vista Controls' engineering and software expertise in fire control, real-time communications, and control systems will provide you with complete turn-key systems solutions all the way from concept and systems integration to full production.

Whether your system operates on land, in the air, or on the ocean, Vista Controls stands ready to supply you with the highest performance VME cards available for fire control, communication, and control systems.

Ready to go under the gun...for you.

VISTA CONTROLS®
HIGH PERFORMANCE MILITARY CONTROL SYSTEMS
Valencia, CA 91355 • (805) 257-4430
Total Systems Integration™
TECHNOLOGY FOCUS: MEZZANINE BUSES

dveloped for a single application. One of the first manufacturers to offer such a board as a standard industrial product was Sun Microsystems Computer Corporation (Mountain View, CA), with single-board versions of its SPARCstation 1, 2 and now 10, called SPARCengines. Each of these SBCs includes at least two slots for SBus I/O modules. You can select from among more than 100 Sun and third-party SBus cards.

Others have also jumped on the mezzanine-bus bandwagon. PEP Modular Computers (Pittsburgh, PA), for example, has developed a bus/busless strategy designed for industrial applications. At the heart of PEP's approach is the company's controlling applications. The approach lets any combination of VME and CXM boards be used.

PEP presently offers a pair of host carrier boards, and already includes about 20 CXM modules covering a wide range of industrial applications. PEP president Josef Kreidl says, moreover, that there are currently at least 20 customer designs either in use or under development. PEP also makes 22 piggyback boards providing digital, analog and miscellaneous functions.

Toward a mezzanine standard

Most recently, Force Computers (Campbell, CA) and Motorola (Tempe, AZ) have joined the flock of controller extension module (CXM). CXM was developed to provide a flexible technology that could carry PEP piggyback boards, as well as provide a relatively large mezzanine platform—about 2½ times the size of 3U VME.

CXM uses a straightforward connection scheme with a 96-pin DIN header connector and a simple addressing scheme that lets you stack up to seven CXM modules on a single base module. In its simplest configuration, a system can be built up without a backplane bus and can interconnect via similar systems using simple field-bus connections. (PEP uses Profibus for this purpose.)

In more complex configurations, however, multiple 3U VME modular and controller boards can be used in a standard 3U VMEbus rack to increase processor power for demand-

mezzanine believers. Force has sided with Sun and provides a VMEbus-based version of Sun's SPARCengines 1 and 2. In addition, the company provides a connectorless 6U-form-factor version of the 2E board without the VMEbus interface. Both boards sport a pair of SBus slots. Force is expected to announce a SPARCengine 10 version shortly.

For its part, Motorola saw a need for broad I/O functionality on a single board and came up with its 162 SBC, which is available with and without a VMEbus interface. For I/O, Motorola has adopted GreenSpring Computers' (Menlo Park, CA) IndustryPack technology. "The IndustryPack," says GreenSpring vice-president X. Kim Rubin, "was designed to be the ideal module for the VME form factor. It's been designed such that two modules fit comfortably on a 3U board, and four on a 6U card. This provides users with a broad variety of options from a single platform."

GreenSpring also offers a single-board product with four Industry-Pack sites that's based on the Motorola 68332 communications processor.

In the interest of fostering the IndustryPack technology, GreenSpring has submitted it to VITA (VME International Trade Association) for possible adoption as a formal industry standard. But the idea hasn't met with much success. First, because just about every VMEbus manufacturer offers its own mezzanine standard, with many offering two or more; and second, because mezzanine bus technology is often tailored to specific requirements and isn't likely to produce a single standard to satisfy diverse applications.

"Mezzanine technology," says PEP's Kreidl, "must offer rapid product development and differentiation for added product functionality. It makes sense to avoid mezzanine standardization, because many useful existing functions would be made obsolete. PEP's CXM technology, for example, specifically preserves the company's existing bank of smaller I/O piggyback functions while offering a simple, cost-effective bus/busless expansion capability."

Proponents of SBus experienced similar resistance when they tried to introduce that technology as a standard mezzanine for Futurebus+. For the same reason that Kreidl mentioned, companies such as Heurikon (Madison, WI) wanted to leverage their current mezzanine technology for the next-generation standard board. Heurikon's CoreBus approach is designed to provide transfer rates in the 200-Mbyte/s range; the company expects to use its mezzanine on Futurebus+ as well as VMEbus products.

MCMs as mezzanine "boards"

While most mezzanine bus approaches are meant to provide flexible I/O solutions, a family of mezzanine buses is emerging that's aimed at higher performance and higher-density packaging. Although these mezzanine boards are usually referred to as multichip modules (MCMs), the approach and technology are basically the same as those used for conventional I/O modules. While there's discussion of even higher-density approaches, such as silicon-
Creating Real Time

**CREATIVITY** translates ideas into action. Ideas are not enough.

**CREATIVITY** is control. It changes chaos into order.

**CREATIVITY** is visualizing the outcome of a design soon enough and clearly enough to improve the plan before action.

**CREATIVITY** is the extra ten percent that makes all the difference.

pSOSystem.
Giving You the Freedom to Create.

The real-time operating system you choose for your next project can make or break it. You need a system that's bullet-proof and fast, integrated and complete. You want a system that gives you the freedom to focus on your application, to develop ideas into reality.

Give yourself that creative edge with pSOSystem, the benchmark real-time operating system. Scalable. Modular. One that's embedded and proven in thousands of products large and small, from telecom switches to video phones, from CT scanners to handheld terminals. And pSOSystem brings you the latest features you need:

- Open system networking, from NFS, RPC, to X11.
- Broad host support, from workstations, PC to VMS.
- Complete language support, from C, C++ to Ada.
- Integrated source and system-level debug tools.
- Transparent multiprocessing.
- Quick-start framework for custom or off-the-shelf hardware.

Discover creative freedom. Call us today at 800-543-pSOS, 408-980-0400 (fax), or at scg_sales@isi.com (e-mail).

CIRCLE NO. 48
on-silicon modules, most of the currently implemented and discussed approaches use standard PC-board or older hybrid circuit technology.

Leading the parade in the commercial implementation of such approaches are the SPARC-based processor modules offered by both Cypress Semiconductor (San Jose, CA) and Texas Instruments (Dallas, TX). These modules include a common cache-coherent interface so that other modules can be added to the system without additional changes.

Both the TI and Cypress modules use the SPARC M bus as a standard interface, with an alternate packet version, XBUS, also available. The modules comprise the CPU, cache memory, cache memory controller, and interface circuitry. The first commercial use of the approach was in Sun's SPARCstation 10, which is available with up to four TI SuperSPARC modules.

Similarly, Motorola offers its hypermodule, based on its own 88000 M bus technology. Systems are available that accept up to four such modules. Outside of some server implementations, however, the 88000 approach has met with only limited commercial success.

MCUs are currently in their infancy, though, and a variety of modules will probably emerge in coming months. One initiative, offered by the Modular Open System Architecture Standard (MOSAS) council, comprising some 20 major defense contractors, proposes a standard module and board interface to cut across both military and commercial applications.

MOSAS is calling for systems based on Futurebus++ protocols, with a standard module form factor, pin-out and module/local interface specification. Initially, four modules are intended to fit on a single SEM-E form-factor board (slightly smaller than 6U in size), with one of them being a Futurebus++-interface module. Others tentatively defined include RISC-based processor, DSP and communications modules.

While the MOSAS concept has merit in attempting to define a universal set of standards, it's come under attack by a number of companies. Some complain that the MOSAS group is exclusionary; others that military applications aren't broad enough to drive the commercial market; and others still that there's no need to introduce yet another format (SEM-E), since there are others already in wide use in the commercial sector; and a single standard such as Harvardbus ++ on SEM-E with MOSAS modules won't satisfy all applications—not even all land-based, shipboard and avionic military applications, not to mention the myriad commercial and industrial uses.

An option from the PC world
Despite controversy at the high end of the market, the embedded per

Motorola's board group broke tradition when it offered its first 6U SBC without a VME interface. The board, also offered with a full VME interface, is aimed at cost-sensitive OEM applications. I/O is handled with four sites for GreenSpring IndustryPack mezzanine boards. A marketing agreement between GreenSpring and Motorola lets the latter company resell IndustryPacks.

the past few months. From a humble beginning only one year ago, the PC/104 consortium, a trade group formed around the emerging standard, has grown to almost 50 members, with more joining almost daily.

PC/104 backers are working to make their specification an IEEE standard—or, more accurately, a subchapter of the IEEE 996 ISA standard. Thus far the consortium has been accepted as a working group and has its own PAR, P996.1. "The project is going ahead with the standard for compact embedded PC modules designation at this time," says Ampre's vice-president of strategic development, Rick Lehrbaum, "just in case there are any changes between the completed IEEE specification and the current PC/104 specification. But I don't anticipate any problems along the way." With or without IEEE approval, PC/104 is well on its way to the critical mass required to become a market standard.

Package, power, price
The small form-factor PC/104 approach has found wide utility; in SBCs using it as a mezzanine bus, in PC/104-form-factor CPUs and in other standard buses such as VME and STD that use PC/104 as a mezzanine. The advantages of PC/104 are that it provides small, inexpensive, reliable, low-power I/O for PC-based designs.

One of the first vendors to see PC/104 as a mezzanine bus for VME was industrial board and system maker Xycom (San Jose, CA). The company includes a PC/104 site on its 386-based VME board, permitting fast, easy and low-cost addition of PC-type functions to a VME system. Others in the VME community are reportedly looking at the approach and will probably be making announcements within months.

While VME makers are taking advantage of small, low-cost, low-power PC/104 technology, the idea. STD Bus has long been regarded as the foremost I/O bus because of the broad range of I/O boards available for it. The idea, then, of using a mezzanine for anything but the simplest function was slow in coming to this community.
The Taurus is a dual-processor, dual-bus, single slot VME board. Its dual-bus architecture allows the 68040 to execute code uninterrupted, while the '030 processes on-board I/O. This optimizes the 68040's performance. Using the '030 as an I/O processor simplifies writing your code. You only need to write high level code to the 68040. The '030 handles the device level code. You also can use the '030 as a DMA controller, while the 68040 directly controls all on-board I/O devices. The '030 uses the SRAM with the 128KB of EPROM code provided by Omnibyte.

The Taurus extensively uses intelligent, on-chip DMA devices for Ethernet, SCSI and serial I/O. This helps reduce processor intervention. Up to 2 stackable modules contain the DRAM. This allows upgradeable options from 4-128MB.

Advanced Omnimodules provide additional custom I/O. You can stack Advanced Omnimodules up to 3 high. The Taurus can accept 1 memory module and 1 Advanced Omnimodule and still fit into a single slot.

To learn more contact Larry Snow:
800-638-5022

© 1992 Omnibyte Corp.
Our New Dual 68030 + '030 I/O Bus Streamlines Writing Your Code

Omnibyte's ARIES™ VME SBC

Aries Architecture
The Aries features 2 68030's. You can use the 2nd '030 as an I/O processor or DMA controller. Using the 2nd '030 as an I/O processor simplifies writing your code. You only need to write high level code to the main '030. The 2nd '030 handles the device level code.

Intelligent I/O
Ethernet: 82596CA¹, SCSI: NCR53C710¹, 4 RS232D: CD401

Standard I/O
2 RS232D: 68C681 DUART, 32 Lines Parallel I/O, or 16 w/ Centronics Printer Port

Memory
4MB to 128MB¹ DRAM, 512KB SRAM, 8KB NVRAM, 1MB PROM, 4MB EPROM

Other
VSB¹, VME64³, Watchdog, Calendar Clock, Mailbox, 68882², (6) 16-bit Timers, Snooping, Advanced Omnimodule Socket

Software
VxWorks¹, UNIX², OS-9³, CrossCodeC, FreeForm⁴

¹ Denotes optional features.

A gate and I/O bus allow the main '030 to execute code while the 2nd '030 processes its extensive I/O. This optimizes the Aries' overall performance (20 MIPS total).

For less I/O intensive applications, you can get the Aries in a single processor version.

Up to 2 stackable modules contain the DRAM. Up to 3 stackable Advanced Omnimodules™ provide additional high performance I/O. The Aries with 1 module each will fit into a single slot.

To learn more contact Larry Snow:
800-638-5022

CIRCLE NO. 119

© 1989 Omnibyte Corp. Celestial Art © Dave Archer Studios, San Rafael, CA

OMNIBYTE™ Corporation, 245 W. Roosevelt Rd., West Chicago, IL 60185
Individual modules or combinations of modules can be connected via a field bus. We've done iSBX modules before, but what we discovered was that, with the power of PC-based chip sets, it was possible to squeeze all the functions of a powerful PC onto the standard STD form factor. Many of our customers have been using our STD board as a stand-alone SBC with the system bus connectors waging in the wind.

Burckle relates, however, that it became clear that there was almost always some function that a customer wanted that's not included on a card, regardless of how comprehensive it may be. And yet users are increasingly intolerant of the cost of a separate card cage and second STD board—both in terms of dollars and real estate. “PC/104,” says Burckle, “because of its widespread following, relatively low cost, straightforward ISA-based interface, and variety of I/O functions available, is the natural choice. There are already 20 or 30 different peripheral functions available and a handful of CPUs. In addition, the form factor makes a nice fit with that of STD.”

The first to see the need for something such as PC/104 was STD board maker WinSystems (Arlington, TX). “We've done iSBX modules before, but they were only for simple, character-based I/O,” says vice-president Robert Burckle. “What we discovered was that, with the power of PC-based chip sets, it was possible to squeeze all the functions of a powerful PC onto the standard STD form factor. Many of our customers have been using our STD board as a stand-alone SBC with the system bus connectors waging in the wind.”

Burckle relates, however, that it became clear that there was almost always some function that a customer wanted that's not included on a card, regardless of how comprehensive it may be. And yet users are increasingly intolerant of the cost of a separate card cage and second STD board—both in terms of dollars and real estate. “PC/104,” says Burckle, “because of its widespread following, relatively low cost, straightforward ISA-based interface, and variety of I/O functions available, is the natural choice. There are already 20 or 30 different peripheral functions available and a handful of CPUs. In addition, the form factor makes a nice fit with that of STD.”

The latest WinSystems product family has a full-featured 80486 board with four options. The first is a low-cost, stand-alone SBC; the second is the same board with an STD connector and interface; the third option includes a PC/104 interface as well as the STD interface; and the last option has a cable connector for a standard passive ISA backplane. “All options, including the STD-based boards, include mounting holes for stand-alone mounting of the board,” says Burckle.

WinSystems apparently isn't the only STD board maker to realize the value of PC/104 technology. Ken Finster, vice-president of MicroSys (Glendale, CA), reports that his company is looking closely at the approach and will probably go in that direction. Like WinSystems, MicroSys provides iSBX connectors and has realized that there are many users don't want or need the baggage of a full card cage and system bus. But they do need the flexibility to provide different functions without modifying the main SBC.

More alternatives

While PC/104 offers an inexpensive interconnect for a mezzanine, alternatives are fast becoming available, and may supply price advantages, leveraged by the high-volume PC market. One such approach that's largely targeted at memory is PCMCIA. This compact form-factor approach, backed by the leading consumer manufacturers in Japan as well as the U.S., provides high-density flash memory at prices well below those of discrete parts. Users of Industry-Pack and PC/104 technologies can already take advantage of this approach through adapters available from Ampro and Green Spring. Whether or not PCMCIA can become a major general-purpose I/O technology—as opposed to simply a memory technology—remains to be seen. It isn't likely to become a mainstream I/O technology for industrial applications in the near future, however, because the need for functions such as data acquisition isn't high enough to attract vendors who'll design specialized parts to fit the exacting form factor.

As PCMCIA is making its commercial debut, Intel's latest 80386/486/P5 local bus, PCI (for peripheral component interconnect), is also coming on the scene. Sometimes billed as a local bus, sometimes as a mezzanine bus, PCI has a defined specification and Intel has reportedly developed interface chips. As initially previewed, however, the bus is intended as a solder-in connection for standard peripheral chips handling such functions as graphics, high-speed communications and other peripheral components.

The advantage of PCI—indeed, its reason for being—is that it handles transfer rates far beyond the capacity of conventional ISA and even EISA configurations. Billed as handling rates of up to 160 Mbytes/s, PCI should be well-suited for the more taxing requirements of multimedia applications.

Only a small leap in technology is required to replace the solder-in approach of PCI with a standard signal pin-out and connector, making it a true mezzanine bus. Should this come to pass, PCI will probably displace ISA for most of the common I/O functions. It might not be a shoehin in the industrial market, however, because once again, relatively low volumes may make implementation...
TRENDS FOR THE FUTURE

Such mezzanine-bus approaches are fast becoming an integral part of system architectures. And it's apparent that the trend will continue well into the future. VITA technical director Ray Alderman predicts that "It's possible that standard-bus products of the future will comprise nothing more than a mezzanine carrier board with standard bus interface circuitry. A board function will be built up by selecting from a variety of processor, communications and I/O mezzanine boards."

The Futurebus+ Desktop Committee (Profile D) already has taken the lead in that direction. It's eliminating the carrier board by using a stack technology, not unlike PC/104 in concept, but with different physical and electrical parameters. While the profile is still far from becoming part of the Futurebus+ specification, visionaries on the committee have identified a tile approach that would provide a stackable array of credit-card-sized tiles. The individual tiles could also be used as standard mezzanine cards on other standard and proprietary boards.

Although nothing has been finalized yet, the Futurebus+ specifiers are looking at a low-power, high-speed interface technology (such as CMOS transistor logic or Gunning transistor logic) and a high-density connector (such as elastomeric connectors currently used in products such as watch displays). Bus traffic is expected to be fast enough to handle real-time video as well as other high-speed applications.

From the work done so far, it looks as if the framers of Profile D are looking to create the ultimate standard mezzanine bus. But as is the case with Futurebus+ itself, it's as yet unclear whether or not one standard bus will be able to solve all problems—that is, to address both low-cost and high-performance requirements in the commercial, industrial and military markets.
Finally, a smart SIO board that puts the intelligence where it really counts: on the serial communications controllers. *A full 40 MIPS worth!*

The result? *Processor power to spare!* The on-board 68030 is free because each channel has its own DMA and 16 byte FIFO controlled by a RISC core. With all 32 channels operating simultaneously at 64-Kbits/second, over 95% of the main CPU's bandwidth is still available. Now that's intelligent!

The Ironies IV-3234 is not only smart, it's flexible. Standard features include synchronous and asynchronous modes, 1 or 4 MBytes of fast DRAM, and the most powerful VME interface in the industry. SCSI/Ethernet, VSB, and additional higher speed SIO ports (up to T1 rates) are optional. Choose from among the best development environments and real-time kernels.

So make the smartest choice for intelligent SIO...the Ironies IV-3234.

...and now, *more SIO in less space with no hassles!* Ironies' new Modular SIO system fits 16 ports, with 8-signals and modem controls on every port—*in just one VMEbus slot!*

*Call our VME Product Hotline Today.*

1-800-334-4812

IRONICS INCORPORATED • 798 Cascadilla Street Ithaca, New York 14850 USA • 607-277-4060 Fax 607-272-5787

IRONICS MODULAR SIO—the most elegant, comprehensive Serial I/O protocol conversion and signal distribution system in the world

IV-3234 and Very Intelligent SIO Controller are trademarks of Ironies, Inc. All other brands or products are trademarks of their respective holders.
Introducing the IXD7232 ...

150MFLOPs of DSP Power!

- **Power by Design:**
  Two IEEE 32-bit floating point ADSP21020s combine to make the IXD7232 the most powerful 6U DSP board available.

- **High Data Throughput:**
  Each DSP has its own independent data paths allowing sustained data transfer rates of 100MBytes/sec with peaks of 200MBytes/sec.

- **I/O Flexibility:**
  Each IXD7232 holds two IXI I/O mezzanines within a single-slot 6U. A wide variety of IXI options, Analog and/or Digital, are available.

- **Reconfigurable Global Memory:**
  SRAM (0ws) and DRAM (1-2ws) mezzanines allow global memory to be optimized for a wide variety of algorithms and applications.

- **Versatile Parallel Pipelining:**
  In addition to global memory, DSPs can pass data via FIFOs (0ws); full bandwidth pipelining between boards is achieved via the IXI ports.

- **Comprehensive Software Support:**
  Development tools include Assembler, Linker, Librarian, Simulator, C Compiler, RunTime Library, Debugger, Debug Monitor and ICE.

Call us at (301)572-6700 for more information.
Design and test engineers alter roles to facilitate test

Time is running out for silicon, circuit board and system houses who haven't taken design-for-test seriously. Old test methods are fast becoming inadequate, while the next generation of systems is waiting in the wings.

Electronics corporations have been singing the praises of designing for testability (DFT) for years. Unfortunately, their arias have been falling on deaf ears and few companies have really embraced true DFT; that is, few are bringing test requirements forward into the design cycle. As components and the systems they drive become more complex and as time-to-market windows close, many companies are, in fact, finding their DFT strategies woefully inadequate. There are myriad reasons for this, but the biggest is simple—unless there is absolutely no way out, people don't like to change the way that they do things.

"Getting design engineers to embrace DFT is a real challenge," says Frank Binnendyk, director of marketing for TSSI (Beaverton, OR). "But right now we have testability problems that are reaching crisis proportions. Packaging and technology trends are producing PCBs and systems that are almost untestable by conventional means, and we can't"

Mike Donlin, Senior Editor
**SPECIAL REPORT: DESIGN FOR TESTABILITY**

simply put a Band-Aid on the problem. But reluctance to change is understandable. Designers still have to worry about everything they always have, and now they’re being told that their designs have to be testable as well.”

Until recently, design issues were the concern of design engineers, and test issues were the concern of test engineers. Each group was managed differently, and although the gap between the two camps was bridged by the system under development, the two didn’t have to deal with each other a lot. If a designer produced a PCB prototype that worked, the board went on to the test engineer, who would more or less start from scratch.

This approach no longer works for many PCB designs, because the smaller traces and surface-mount components of today’s PCBs make accessibility by traditional bed-of-nails testers difficult. This means that test points must be placed intelligently on a complex board to make the most of the limited access it provides. Test, then, must be part of the design of a board right from the outset, and there lies the rub.

**Maturing differently**

The EDA and test industries grew up separately, so the concerns of EDA vendors were different from those of automatic test equipment (ATE) vendors. As a result, the tools that each provided to their prospective users weren’t able to communicate very well. This was unfortunate because much of the information the designer needed to complete a PCB could be useful to the test department, but the necessary links between the two databases simply weren’t there.

To complicate matters, as EDA and test evolved, the technologies that they were helping to create were getting more complex. A prime example is the emergence of multipich modules (MCMS), complex silicon-on-substrate devices that are a test engineer’s nightmare. “With traditional PCBs you could take measurements by putting down two probes and analyzing the path between them,” says Stephen Taft, CAE product manager at Harris EDA (Fishers, NY). “With MCMS, the traces are much finer, so you really can’t inject current or you’ll cause problems in the substrate. So people are looking for more passive methods. That means that EDA vendors have to expand their databases to approximate what a capacitance value might be and evaluate problems along a net. The time is ripe for a melding of the two technologies, EDA and test.”

As technical advances and market pressures force these two camps to cooperate, both design and test engineers are concerned that they’ll have to become experts in the other’s discipline. “But it’s not really so much becoming an expert in someone else’s field as it is getting the appropriate information from one group to the next,” says Pete Lwin, marketing manager at Schlumberger (San Jose, CA). “It’s really an information management problem. But not many design engineers are willing to implement test strategies simply because another department requests it. So the ATE and EDA vendors have to work to make this transition as painless as possible.”

There’s tremendous pressure to make these interdepartmental linkages. Corporations embracing DFT strategies have impressive results to crow about, and these results involve the driving forces behind any product’s success—cost, quality and time-to-market.

“We’re designing 6 x 9-in. VME boards with up to 200 components on them,” says Paul Wittenburg, test engineering manager for the Motorola Computer Group (Tempe, AZ). “To make sure that we get the high yield that our six-sigma quality program demands, we use a combination of in-circuit, cluster, functional, and scan testing. We use this test data to weed out manufacturing faults and unreliable component vendors. We are also bridging the gap between EDA and test and are working with companies such as TSSI to make bidirectional links between our testers and simulators. The program is working. Three years ago, it took 12 weeks to develop PCB tests with 65- to 70-percent fault coverage. Today we can develop 95-percent fault coverage in a four-week time frame, and we can envision even better results in the future.”

**Getting support**

Stories such as Motorola’s are sure to get the attention of design management and will speed up the development of the necessary links between design and test, but the transition is far from painless. It will undoubtedly take the authority of upper management to drive the effort.

“In many companies, senior management doesn’t believe that test, reliability and manufacturability should be the concerns of the design engineer,” says Vin Ratford, marketing manager for test products at Mentor Graphics (Wilsonville, OR). “So even if a designer wanted to take the time to incorporate DFT strategies, chances are that he or she would still be evaluated on how fast a prototype was developed. Only when senior management changes the way that it evaluates design engineers’ performance—to actually producing a testable, manufacturable product—will DFT take hold.”

Undoubtedly, as senior management realizes the benefits of adopting DFT and the consequences of failing to do so, the links between design and test will be mandated. But even when they are, what spe-
FUTUREBUS+ BECOMES A REALITY.

FUTUREBUS+ PICKS UP WHERE VME LEAVES OFF.

CCT is proud to be the first to deliver a significant family of Futurebus+ products. A family that's built on industry standards!

With Futurebus+, OAS (open architecture systems), CCT has taken a giant step forward in computer technology. We can deliver OAS systems or boards based on industry standard micro-processors & operating systems, all in an environment that allows more speed, capacity and intelligent communications.

Our product line includes, standard CPU's, global memory, array processors and specialized interfaces that address the demands of many applications. Including:

- Telecommunications bridges and routers
- Tactical computers and displays
- Manufacturing process monitoring & control

Today's processing power is cramped on yesterday's bus. Release the power of your application with Futurebus+ data movement capacity.

Don't invest in yesterday's technology — Futurebus+ is here today!

FEATURES:

- Scaleable up to 256-bit
- 64-bit compatible
- Multi-processing and Cache coherent environment
- Standard software paradigm through CSR's
- Fault tolerant
- Distributed and Central arbitration
- 68030-33 CISC CPU
- 29000 RISC CPU
- i860 64-bit RISC CPU

Call or Fax CCT today for more information on our Futurebus+ product line!

Phone 1-800-CCT-7902
Fax 1-714-937-1225

Cable & Computer Technology, Inc.
1555 S. Sinclair St.
Anaheim, CA 92806
(714) 937-1341
specific products are available to help bridge the gap? One company that's been developing these links is TSSI, whose Wavemaker software accepts data from a variety of EDA sources and generates an intermediate waveform database. The TSSI Waveform Database (WDB) contains behavioral data, independent of simulation and test environments. The database stores unstructured data in a Standard Events Format (SEF) file and structured data in WDB data sets. It permits unrestricted movement throughout the TSSI software system and can be displayed, analyzed, modified, and used in a variety of outputs, including the generation of ATE-specific test programs. The database can also perform both simulation and tester rules checks.

**Forging a link**

Bridging the gap between simulation and test is an important consideration in a successful DFT strategy; otherwise, incorrect and costly assumptions can be made by both the design and test departments. "In a typical test environment, you first run a fault simulation to make sure you have a complete set of test patterns to verify a board's functions," explains TSSI's Binnendyk. "Then, if you're doing functional testing, you create a fault dictionary and set up guided probe diagnostics, which means setting up the right databases to accomplish your testing goals. You take that information and migrate it to the tester and debug the test programs so that they pass a known good board. But when you do this, you change the base level of patterns that were verified by the simulator, so you don't have proof that you have the same coverage. To close the loop, you need to go out of the tester environment and resimulate."

Although products such as TSSI's take advantage of the natural synergy that should exist between design and test data, true DFT needs to migrate up the design cycle, not simply get tacked on at the end. And even though many PCB designs are partially tested through software simulation, the board that comes out of manufacturing can have serious problems if DFT hasn't been implemented. "Not many people are doing full board simulation," says Schlumberger's Lwin. "Even if you simulate functional blocks, it's hard to see how they interact when you get everything put together. There are always a lot of unknowns when you get into asynchronous processes, bus mastering and interrupts. In the past, when you had a lot of test points for observability and many boards were synchronous, testing was easy. But today's asynchronous designs, where you have a microprocessor handling interrupts from peripherals such as keyboards, are much harder to simulate and test. For many companies, it's easier just to make a prototype and debug it."

**Boundary scan to the rescue?**

If designers are going to be persuaded to change their "prototype and debug" habits, an easy-to-use, low-penalty technology must emerge. Fortunately, boundary scan seems poised to assume that role. Also known as the Joint Test Action Group (JTAG) standard, boundary scan was officially adopted as an IEEE standard—1149.1—in 1990. It's a technique that gives you access to the I/O pins of digital circuits on a PCB by means of a test bus consisting of four wires. (A fifth wire is optional.) In a typical boundary-scan IC, a shift register is placed between the core logic and the buffers adjacent to each I/O pin. Each shift register stage lets you control and observe what happens at each I/O pin of the IC.

On a PCB assembled with boundary-scan ICs, the registers for each component can be connected in series to form a path through the design to test each component and diagnose failures. Unfortunately, because few commercially available ICs use boundary scan, it's nearly impossible to populate a board solely with boundary-scan devices. Still, designers see it as one of the few avenues open to them to implement DFT.

"Boundary scan is a powerful remedy for today's test problems, but it's not a panacea," says Chi Yau, supervisor of the boundary-scan technology group at the AT&T Bell Laboratories Engineering Research Center (Princeton, NJ). "PCBs will always have analog parts and jellybean components that don't have boundary scan, but at least boundary scan eases the pinch we're feeling in trying to test PCBs. With boundary scan we can use less test pads and reduce node count. The high node counts in circuit test fixtures are hard to maintain. The small pins are delicate and easily bent, which decreases yield. Bound-
The ultimate design-for-testability technique: 1149.1 boundary scan

Over the years, design-for-testability (DFT) techniques for board test have evolved to respond to changes in device, assembly and test technologies. In the early days of in-circuit test, for example, the basic DFT techniques were published design guidelines specifying the use of test pads on nets without throughhole components, the size and placement of test pads and the like. Later developments include internal scan patterns for the board-test library, tools for in-circuit testability review prior to artwork and simulation of design vectors to be used in test.

Today, however, new technologies are driving electronic manufacturers to embrace the ultimate DFT technique: the IEEE 1149.1 1990 boundary-scan standard. Here the tester hardware is a scan cell designed into the silicon. In the two years since the standard received the IEEE's blessing, dozens of systems houses have started down the boundary-scan path. Teradyne alone has more than 40 customers who are using our software to implement boundary scan.

Three trends

Three major trends are behind the rapid adoption of 1149.1 boundary scan. First, DFT is emerging from the shadows to stand in the spotlight on the concurrent engineering stage. Test and manufacturing engineers have always struggled with testability issues, but other people in the organization, including design engineers, are now thinking about it too.

A second trend is the explosion in device complexity. Typical vlsi device designs today have tens of thousands to hundreds of thousands of gates, resulting in dramatically longer development times for in-circuit test patterns. For a device such as the Intel 80386, for example, it might take seven weeks to develop pin-level fault coverage patterns for in-circuit testing. Custom ASIC devices have similar development times.

Third force behind boundary scan's rise is the lack of physical test access. Nodal access is disappearing because of high-density boards, fine-lead components, surface-mount assembly, TAB, and MCMs. Without physical access, conventional tools simply can't be used. The designer can't access the assembly for prototype debug and verification, nor can manufacturing gain access for board-level in-circuit testing. These impediments can be so great as to render a product strategically unfit.

Boundary scan solves the problems of pattern generation and test access. Serial test vectors can be generated automatically using ATPG software from ATE vendors, cutting test programming times from months to minutes. And boundary scan provides virtual access through the boundary-scan path, which is a board tester or debug accesses from the board's edge-connector.

Despite these advantages for manufacturing and test, device design engineers are quick to point out the drawbacks of boundary scan. Typical objections include the performance decrease from adding the boundary-scan cell's multiplexer in the datapath, the sacrifice of precious silicon to test circuitry and the extra design time that could delay getting the product to market.

These problems are not insurmountable. The typical 1-ns propagation delay can be reduced through intelligent implementation. Designing the boundary-scan cells into the output buffer, for example, can reduce the propagation delay to hundreds of picoseconds or less. The percentage of silicon devoted to the test circuitry declines as device size increases, and large parts are the ones most likely to be designed with boundary scan. On a medium-sized part, for example, 1149.1 circuitry might take up only 2 to 3 percent of the silicon. On a large part such as the 80486, it might be 1 percent. Furthermore, designers can often find ways to employ unused parts of the die, such as the output buffer circuits, as locations for the boundary-scan cells. Finally, to ease the design burden, design tools are becoming available that insert 1149.1 circuitry into ASICs automatically, verify 1149.1 circuitry prior to first silicon and verify BSDL models automatically. Board designers can also benefit from automatic testability analysis software and prototype debug/verification tools already on the market.

Although adoption of the 1149.1 standard may contribute to some increases in design time and costs, the manufacturing group will typically gain far more benefit in terms of reduced time and costs. Compare, for example, the time it takes to develop test programs for Intel's 386 chip without boundary scan to the time it takes for the 486 chip designed with boundary-scan test circuitry. We estimate it takes seven weeks to develop conventional in-circuit test programs for the 386 that deliver 100-percent pin fault coverage. The cost, assuming $50/hour for labor, is $14,000. By comparison, producing boundary-scan test programs for 100-percent fault coverage using ATPG software takes 10 hours and costs $500. If the BSDL is provided by the semiconductor vendor, as is the case with most commercial parts, the time and cost shrink to two hours and $100.

Other benefits

In addition to the savings during manufacturing, 1149.1 offers the potential for faster service response and shorter time-to-market. Strategically, boundary scan opens up an entirely new approach to troubleshooting down systems. Shorter time-to-market comes from time savings in two areas that typically act as gates to new product introduction: prototype debug time and test program development time. Since boundary-scan software and the 1149.1 standard can help shorten both of these activities, they can speed time-to-market. Faster test programming results from the automated programming that can be achieved with boundary-scan designs. Depending on the board design, a lower-cost tester may be able to deliver the same test quality as a much higher-performance, more expensive tester.

Ultimately, electronics manufacturers will adopt 1149.1 design and test because of the overwhelming economic and competitive benefits. These advantages make boundary scan much more than just a testability technique. It promises to be the most significant factor driving board test economics in the 1990s. And it may well be the third major wave in the history of board test, following functional board testing in the 1970s and the rise of in-circuit testing in the 1980s.

Mark Myers, product manager, Assembly Test Division, Teradyne, Boston, MA
Boundary-scan PCB architecture

Within a PCB assembled from several ics, the boundary-scan registers for the individual components can be connected in series to form a single path through the complete design. The path, which surrounds the core logic, provides test data input (TDI) and test data output (TDO) connections, and appropriate clock (TCK) and control signals (TMS). In such an arrangement, test data can be shifted through the boundary-scan path from TDI to TDO to achieve node testability. Each boundary-scan cell can capture data on its parallel input, update data onto its parallel output, and serially shift data to its neighbor.

Scan strategies can potentially shave valuable time off design and test cycles, making the technology worth the investment.

"Let's say you want to write test vectors for a 386 to see if you have opens, shorts or stuck-at faults," says Brian Miller, product manager at Teradyne (Boston, MA). "The average time that our test services people would quote to do that is about eight weeks, at a cost of $15,000. But if you took a more complex chip, such as the 486, and it had boundary scan, you could use our test pattern generation software and get the same level of fault coverage in about eight hours. If the silicon vendor gave us the boundary-scan description language (BSDL) files, it would take less than two hours. If someday you could have a board with 100-percent boundary-scan components on it, it's not unreasonable to think about an order of magnitude of difference in the test-development cycle."

Automated pattern generation

If such time-to-market rewards are to be realized, boundary scan must be embraced by board design and test engineers, who in turn will pressure silicon vendors to implement it. To entice designers to use boundary-scan components, companies such as Teradyne are automating the test pattern generation portion of the design cycle for boundary-scan parts. The company's Victory software, for example, automatically generates in-circuit test patterns for boundary-scan devices. For networks of boundary-scan parts, Victory generates interconnect test patterns that deliver 100-percent pin-level fault coverage. The tool also lets you use the scan path to test the internal logic of boundary-scan devices, and to test non-boundary-scan devices by using the scan cells connected to the boundary-scan inputs and outputs as virtual channels.

Tools such as Victory get their knowledge of a device's boundary-scan circuitry from a model written in BSDL, a subset of VHDL that's tailored to the 1149.1 standard. It offers a standard syntax for defining the topology of the test access port (TAP) and boundary-scan register, including which boundary-scan cell corresponds to which physical device pin.

In a complex device such as a microprocessor, the correlation of the BSDL description to the actual implementation in silicon must be documented correctly, or the resulting BSDL file can do more harm than good. Intel (Santa Clara, CA) recently enlisted support from Hewlett-Packard (Loveland, CO) to help debug BSDL files for the company's 486 microprocessor. Intel plans to publish these files on public bulletin boards such as CompuServe, but first needed assurance that they would be as accurate as possible. HP was chosen for the task because the company was responsible for developing the BSDL standard.

"When you create a boundary-scan test, you create thousands of test vectors," says Stig Oresjo, applications engineer at HP. "It's of prime importance that your BSDL file describes how the boundary-scan chain has been implemented in the component. Because it's a map between the cells and the I/O pins, and there are large vector sets in a complex component, it's important to verify the correct description."

Although the BSDL files for complex devices must be written and debugged with care, one thing is certain. When silicon giants such as Intel start making their BSDL files public and begin implementing boundary scan in their devices, widespread acceptance of the boundary-scan standard is imminent.

Limited use, but useful

For the present, most designers and test engineers are content to use boundary scan to check for open solder connections, shorted solder bridges and devices whose pins are stuck at one or zero due to grounding or shorting to power pins. This rather limited use of the technique might seem like a lot of work for little return, but board manufacturers are convinced that it's worth the effort. "When you're designing boards for military and aerospace applications like we are, fault cover-
The main strategies for printed circuit board (PCB) test and fault diagnosis are functional test, in-circuit test and boundary scan. Any design-for-test (DFT) considerations must be based on the test strategy that's to be used.

Functional testers make use of the board's edge connectors to drive the circuit's inputs and monitor its outputs. With this method one is obliged to create a unique set of test vectors for each board. Creating these vectors may become excessively expensive as the complexity of the board increases.

In-circuit testers verify the functions of components in situ, on an individual or cluster basis. Creating in-circuit test fixtures for boards with lead-through-hole components mounted on a single side is relatively easy. Circuit boards using surface-mount technology (SMT), however, may create problems for in-circuit test, especially when the components are mounted on both sides of the board. In-circuit DFT considerations include providing sufficient and accessible test points and ensuring that each component can be isolated and tested independently. A component can be isolated by forcing any devices driving it into a tri-state condition.

Boundary scan to the fore

The increasing complexity of components and the introduction of SMT, with its limitations in testability access, have proved to be major driving forces behind the use of boundary scan. All types of scan technology have benefited from being incorporated into logic synthesis, but typically this has only found application in ASICs.

Until recently, the support tools needed to successfully use boundary scan in the PCB realm haven't been available. There's a world of difference between a prepackaged demonstration and the real-world application of a tool.

Although there are some powerful in-house tools, it's only recently that commercial boundary-scan tools have become sufficiently mature for use in the PCB arena. In addition, there's a scarcity of off-the-shelf devices that contain support for boundary scan.

Intergraph, a manufacturer of workstations and associated software, and Intergraph Electronics work together to produce Intergraph systems. These workstations are based on the latest technology, which mandates DFT strategies. As an example of this technology level, consider an 11 x 14 in., multilayer, ultra-high-density, double-sided SMT assembly with over 1,000 devices (102 of which are GaAs), more than 10,000 soldered joints and over 16,000 vias. The via and pad dimensions are 0.016 and 0.030 in., respectively, for through-vias, and 0.010 and 0.020 in., respectively, for blind and buried vias. The board runs at 75 MHz on fiberglass.

Beginning with the concept

At Intergraph, DFT begins at the conceptual stage of the design. The appropriate test strategy is determined by the test engineering team in conjunction with the design team. The test strategy selected then determines the DFT requirements.

Although individual components may be supplied with extensive specifications, there are few published industry specifications that cover the fitness and suitability of materials and components for specific SMT assembly processes. The component engineering team selects component packages for manufacturing process compatibility, including such factors as lead form, package type, leadplating thickness and materials, and operating temperature tolerances. This level of up-front specification provides the receiving department with the data needed to make decisions as to whether or not to accept or reject components and materials.

The component engineering team also specifies the preferred presentation format—that is, the packaging in which the components are to be delivered to the manufacturing group. This ensures that all parts are in a format compatible with the automated manufacturing process, as well as the automated component test process.

It isn't sufficient to develop test procedures that work only with boards that have just been populated. The test procedures must also be appropriate for field returns which have, for example, heat sinks attached to the components.

Multilayer, double-sided, ultra-high-density SMT boards typically have major problems providing access points for in-circuit tester pins. While boundary scan certainly offers some advantages, the scarcity of off-the-shelf boundary-scan devices, and the accompanying overheads of increased gate count and propagation delays, often prove to be deciding factors. Also, in-circuit test is a known and mature technology and provides the advantages of instant and accurate diagnostics, 100-percent short fault detection and the ability to test analog components.

Since in-circuit is currently Intergraph's test strategy of choice, Intergraph Electronics provides Intergraph with an in-house tool. The PCB-Engineer post-layout database contains all necessary information pertaining to the locations of components on both sides of the board. The database also has information about those components with heat sinks, and about required test-point clearances for components both with and without heat sinks. By examining the PCB-Engineer database, the in-house tool automatically extracts test-point locations for in-circuit test. The tool takes into account component locations, test pads, through-hole vias, and blind vias on both sides of the board. Also, in conjunction with PCB-Engineer, the tool is used to ensure that the positioning of any hand-wires won't affect test-point access.

The test engineering team provides the design team with DFT guidelines; it's also involved in all aspects of the design process to ensure that nothing slips through the net. An example of in-circuit DFT guidelines is the ability to take control of the clock distribution network. With respect to the clock, design guidelines ensure that multiple pipeline stages aren't driven from the same clock branch. ASICs are designed with one pin tied to a soft pull-up. By controlling the single pin, the in-circuit tester can cause all of the ASIC's outputs to go tri-state. Similarly, in the case of PLDs, either an extra pin or an unused state is utilized to cause all the PLD outputs to go tri-state.

With the growing use of MCMS, both Intergraph companies are actively pursuing hybrid solutions combining in-circuit test and boundary scan.

Clive Maxfield, a member of the technical staff, Intergraph Electronics, Huntsville, AL
SPECIAL REPORT: DESIGN FOR TESTABILITY

age has to be very high," says Mike Howard, staff engineer at the Hughes Radar Systems Group (El Segundo, CA). "By using boundary scan whenever possible, we can test for manufacturing defects which account for a significant portion of board failures. Boundary scan lets us know whether the problem is in the design or in the manufacturing process of the PCB."

This ability to separate manufacturing defects from design faults is currently boundary scan's chief selling point. Some companies, such as John Fluke Manufacturing (Everett, WA), are banking on boundary scan's acceptance at the bench or field service level. Fluke has been bundling boundary-scan diagnosis capabilities with the PM 3580 logic analyzer from Phillips (Eindhoven, the Netherlands). By connecting the logic analyzer to the boundary-scan ports on a PCB, you can check for shorts, opens or missing components on a prototype. The latest release of boundary-scan software, the PM 3705 BST Explorer, works in conjunction with either a notebook PC or the Phillips logic analyzer to debug boundary-scan boards.

By emphasizing the use of boundary scan to find manufacturing faults, Fluke and Phillips are hoping to convince designers that boundary scan doesn't have to be used only for sophisticated diagnostics. "We envision using boundary-scan analyzers in field repair," says Bob Roth, product marketing manager at Fluke. "This will let field engineers quickly test and swap out defective boards or make simple field repairs. It can also help the people in the repair lab isolate and correct faults on boards returned from the field."

As attractive as boundary scan appears when it's presented in such a flattering light, some engineers are concerned about the trade-offs, either in device and board real estate or in performance. Although boundary scan isn't exactly free, many EDA and silicon vendors are assuring the design community that the penalties are slight when compared to the gains in testability and overall design quality. "On a typical device, you're only talking about a 300-to-500-gate penalty in the logic and about eight to ten gates per I/O pin," says Kelly Gomes, product marketing manager at Synopsys (Mountain View, CA). "Some ASIC vendors have come up with ways to reduce this even further, but in terms of overall percentage of silicon sacrificed, it's not much. By using boundary-scan devices, you can concentrate on debugging the functional side of your design because you've eliminated manufacturing faults as a cause of failure."

For its part, Synopsys has released the Test Compiler Plus, which includes boundary-scan synthesis in its automatic test-pattern generation (ATPG) capabilities. Using this feature, you can synthesize the TAP controller, control circuitry and I/O pads, and can automatically connect JTAG to your design.

Synopsys has also developed synthesis for partial scan into IC designs. Partial scan is an approach to IC testability that turns some of the sequential elements in an IC design into scan registers or elements that are controllable and observable. This is a variation of full scan, where all of the sequential elements are scannable. According to Gomes, "Partial scan is attractive for design applications that are tightly constrained by performance and area requirements—for example, a CPU that can't afford any performance impact on a critical path."

Stumbling blocks may crumble

Through the efforts of EDA vendors such as Synopsys, the stumbling blocks to DFT may eventually crumble, but not without concerted effort on the part of silicon vendors and ATE manufacturers as well. Cadence Design Systems, for example, has joined the ranks of EDA vendors providing test synthesis tools. At last month's International Test Conference (Baltimore, MD), Cadence unveiled three tools, the Test Synthesizer, Test Simulator and Test Generator. Although these tools target ASIC designs, the increased availability of ATPG software will ultimately make circuit boards more testable, since both custom and off-the-shelf ICs routinely sport scanchain testability features.

Until the day comes when most components offer boundary-scan capabilities (which is, at best, a way off), designers will have to get creative about using what test access they have. Analog components, for example, aren't generally amenable to boundary-scan techniques, so their networks will require physical access if analog in-circuit testing is necessary. These complications require that designers and test engineers alike communicate their test needs to layout engineers, so that all or most of the PCB can be tested. By designing for access, the needs of test can be met without dramati-
New test strategy needed for complex PCBs

How does an engineering department design a PCB for testability when it contains 24 layers, 100 208-pin quad flat packs ICs, 8,000 nets, 1.5 miles of wire, 20,000 holes, and a 6-mil trace pitch?

That was the challenge facing Quickturn Systems in designing the new Enterprise Emulation System, a very complex hardware emulation system in which testability and reliability are paramount. The Enterprise Emulation System contains up to eleven PCBs ( emulation modules), each with more than 100 ICs interconnected through a programmable backplane. A fully populated system contains more than 1,200 complex ICs, which must all be tested and proven to function correctly to provide the reliability demanded by users. One criterion of the board design, then, was to come as close as possible to 100-percent testability.

Team approach

Quickturn determined that the testability problem could only be solved by developing a new set of test strategies. The first thing the company did was form an interdisciplinary team consisting of company engineering and manufacturing groups and key vendors, the latter being: the layout specialist (Shared Resources, San Jose, CA), the board fabricators (AcSist Associates, St. Louis Park, MN; Ambitech, Chatsworth, CA; and Multek, Irvine, CA); and the assembly contractor (Ceridian, formerly part of Control Data, Bloomington, MN). This group was charged with making the emulation modules manufacturable at a very high quality level; it also facilitated a team approach in solving any problems that might crop up.

The team determined very early in the design cycle that testability would be a key success factor. Since faults are more complex and difficult to clear if they’re found late in the test sequence, it made sense to concentrate on early error detection. The first goal, then, was to find errors and problems as early in the test process as possible, resulting in easier fixes that would save valuable time and effort.

Since most faults are manufacturing defects—interconnect problems, shorts and opens, and the occasional bad component—the first portion of the test strategy concentrated on developing a strong bare-board test. Testing to the actual netlist instead of using the more common golden board method verified that the design’s netlist was correctly implemented and that systematic errors were found. Much care was taken with layout to assure that in-circuit test pins could contact all 8,000 nets on the board. And obviously, it was necessary that large enough commercial test systems were available to handle the design.

Special considerations were also incorporated into the design. For example, except for power and ground, no pins (such as enable pins) are tied directly to the VCC and GND planes in the board. Vias are used on all traces to make sure the tester can reach all signals from the bottom of the board. And surface-mount pads are routed to via holes arranged on a regular 50-mil grid to allow contact with the bed-of-nails tester and provide access to all pins.

In-circuit test

The next step was to develop an in-circuit test for the assembled board. A major problem was encountered, however. There was no commercial in-circuit test system with enough pins to test the fully wired board using standard techniques. The solution to this problem was in the design of the board itself.

The Enterprise board design consists of large numbers of full-custom ICs designed by Quickturn and of Xilinx FPGAs. The custom chips were designed with a fully functional JTAG implementation, and the FPGAs were also loaded with JTAG circuitry. Special care was taken with the circuitry to allow parallel functional testing of the custom chips and FPGAs. Since a complete system may have thousands of chips, it’s impractical to test them all individually. By injecting test vectors to all ICs in parallel and monitoring the TDO pins while running an internal test, the chips could be verified very quickly. The TDO pins should behave in the same way for all chips on a clock-for-clock basis.

If any chip is different, an internal error is indicated. Many of these test vectors are the same as those developed by chip vendors for testing fabricated chips on their IC testers.

The pin limitation problem was also solved thanks to JTAG. Ceridian test engineers exploited the JTAG boundary-scan features of the design and invented a clever signature analysis-based in-circuit test strategy that reduced by two-thirds the number of test pins required to test the board and isolate its faults.

As part of this strategy (and prior to chip availability), Quickturn did a dry run with dummy boards to give all vendors process experience. This let many process problems and mechanical fixturing issues be solved before the prototype boards were even built.

Verification of the emulation modules in the finished system was the next concern. The Enterprise Emulation System is designed to take any circuit netlist and implement it in reprogrammable hardware. The system includes an internal pattern generator and logic analyzer to assist in debugging the user’s design. Using these features, the test engineers had the emulator test itself. Test circuits were loaded into the system, exercised with the pattern generator, and, using the logic analyzer, the actual results were compared with the expected results.

Reliability issues were addressed simultaneously with test issues. The exchange of ideas and information between Quickturn and Ceridian test and diagnostic engineers allowed exploitation of a number of strategies, and the team test effort produced excellent results. JTAG simplified the diagnostic routines, and Quickturn added a suite of built-in diagnostic tests that can be run to test the system before starting the emulation process. The system test diagnostics take less time to run than on an earlier version of the product, even though the new product is an order of magnitude more complex.

Dug Stewart, vice-president of manufacturing, Quickturn Systems, Mountain View, CA
I S P E C I A L R E P O R T: DESIGN FOR TESTABILITY

Synopsys' JTAG synthesis tool automates 1149.1-compatible synthesis and insertion into ASIC designs (left). It synthesizes the test access port (TAP) controller, control circuitry and boundary-scan register (right) based on parameters defined in a menu-driven user interface.

Engineers at TI (Plano, TX) used boundary scan for design verification as well as in-circuit test on the Aladdin 32-bit parallel processor. Shown here is an Aladdin Basic Processing Module (BPM), which hosts four multichip modules. Each BPM provides a peak throughput of 100 Mips, simultaneously with 400 MFlops of vector processing. The Aladdin system, which includes five BPMs, will fit within a 45-in. cylinder that's approximately 3-in. high and 4-in. in diameter. It will be used primarily for automatic target recognition systems for intelligent weapons and avionics.

...interconnects...

Aladdin, is a 100-MHz, high-density parallel processing computer. It employs silicon-on-silicon packaging and three-dimensional memory packaging to achieve 500-Mips of scalar processing performance and two GFlops of floating-point processing performance, all packaged in a 4.5-in. (diameter) cylinder less than 6-in. high. TI used its Asset tool to generate scan tests to verify test bus operation, scan path integrity, internal register access, core logic operation, and IC-to-IC interconnects.

"We were able to find some problems in the design that never showed up during simulation," says Wayne Daniel, an applications engineer at TI. "We also had some catastrophic failures on ASICs that were caused by hardware scan errors. Occasionally, one or more bits caused bad instructions or data to be scanned into the unit under test. A scan error had placed the ASIC in test mode and enabled a boundary-scan IO direction control cell. This condition caused the device to back-drive a memory port, which quickly led to overheating and caused a power-to-ground short. One painful lesson we learned was about the lack of fault tolerance and fail-safe procedures in 1149.1. While absolute control is required for boundary-scan tests, the standard test bus could be enhanced to reduce the probability of scan errors that could cause physical damage."

While TI's experience certainly shows the limits beyond which the IEEE standard can't be pushed, it will undoubtedly be a while before the average design team uses JTAG so exhaustively. Most designers are taking a wait-and-see approach while innovations such as TI's are published and more devices host JTAG ports. Until boundary scan comes of age, these design and test engineers will rely on standard methods of software simulation for portions of their designs, as well as debugging of the prototype and in-circuit testing.

"Right now there are two camps," says Dan Caldwell, manager of test technology at Plexus (Neenah, WI), a contract electronics manufacturer. "There are people who embrace boundary scan as much as they can, and there are people such as us who feel we can get our product to market faster using other DFT methodologies, along with exhaustive simulation and debug. About 90 percent of the VLSI devices out there don't have boundary scan, and we don't think it makes sense to design ASICs with it if nothing...
Today's system solutions call for an integrated approach to hardware and software. That's why we've put BUSCON and SOFTCON together.

BUSCON, the leading trade show and conference for bus boards and other elements of systems architecture, now runs concurrently with SOFTCON, the national software conference for system engineers. The combined focus of BUSCON and SOFTCON bridges the gap for system integrators, engineers, and their managers seeking total solutions.

Coordinated by Electronic Design, BUSCON and SOFTCON offer the hardware and software solutions you need now. Our flexible format allows you to mix and match sessions from either program. And both conferences offer entry to the combined BUSCON/SOFTCON exhibit hall.

If you're looking for system solutions you can use now, then plan to attend BUSCON '93 West and SOFTCON '93 West, February 9-11, 1993 at the San Jose Convention Center, San Jose, CA. For more information, just return the coupon or call (800) 243-3238 or fax (203) 857-4075.
else on the board has JTAG. We're positioned to use boundary scan when it's more accessible, but right now our methods work fine.”

Finding other ways

In addition to traditional design methods of ensuring PCB quality, some design and test engineers are pursuing alternative techniques to test their boards. One such method uses FPGAs to get to inaccessible areas on complex PCBs. Lattice Semiconductor (Hillsboro, OR) has introduced a family of non-volatile, in-system, programmable, LSI (ispLSI) devices that it uses to improve PCB testability. The devices use TTL-level signals for programming, and a simple five-wire interface for programming control. The programming circuitry is embedded in the ispLSI device, which reduces the amount of dedicated circuitry required for testability.

“One of our customers used our devices on a 15-layer, 23 x 28-in. board with surface-mount devices on both sides,” says Jock Tomlinson, field applications engineering manager at Lattice. “They used seven of our devices on the board, but instead of programming them for their intended logic functions, they programmed a digital pattern into the FPGA to test sections of the board. One of these is a DRAM controller, which they use to force test vectors into the DRAM bank. They can program it for its normal function after the test.”

Tomlinson also says that customers use the parts to isolate devices on the board. By setting the ispLSI enable pin low, all pins on the device are tri-stated, effectively shutting it off for diagnostic purposes.

Even with such innovative ways of implementing DFT strategies, the core problem is still getting design engineers to accept new responsibilities. Certainly, the success stories of companies that have implemented such strategies are bound to get management's attention. But some

---

Look at the 3V experience of AT&T Bell Laboratories. Look at the success of our sub-3V cordless phone. You can see why no one can match AT&T's problem-free, worry-free 3V system design development.

The chart tells you why we're a 3-volt leader. But, beyond that, you get the design-in power of our flex-

**3-Volt ASIC Checklist**

1. Experienced 3V ASIC Supplier
2. > 70 MHz 3V Operation Achievable
3. Fully Characterized Library of Cells (Voltage/Temp/Process)
5. 3V Industry-Standard Macrocells
6. 3V Analog Cells (OSC., A/D, D/A, etc.)

AT&T
vendors caution against making grandiose claims for DIT methods, or technologies such as boundary scan will end up on the garbage heap of buzzwords and broken promises. “My big worry is that upper management will invest in boundary-scan parts and methodologies and expect miracles,” says Mark Myers, product manager at Teradyne. “They might start looking for test times to immediately be reduced by one-third or one-half. But in mixed technology boards, the testing problems can get difficult in a hurry, particularly if everyone is just learning how to use the new methods. If there’s too much pressure on design and test departments to shorten design cycles because someone upstairs thinks boundary scan or some other DIT strategy is a panacea, then there will be a backlash from engineers, who are admittedly reluctant converts to begin with.”

Postscript

Until recently, bringing up the topic of DFT was a sure-fire way to make a design engineer’s eyes glaze over. Nowadays, however, the subject often starts intense debates about overworked designers, untestable systems and shifting management roles. The fact is, testability has been playing catch-up with technology innovations for years, but most companies were willing to let the test department scramble for solutions at the back end of the design cycle. But recent developments in IC packaging and MCM technology, as well as increased demands for wringing more performance from smaller systems, are sounding the death knell for the old way of doing things.

At September’s International Test Conference in Baltimore, the commitment to DFT was evident. EDA vendors were touting the latest in ATPG software, ATE vendors were displaying links to design tools, and papers were presented that were aimed at the new breed of design engineer who incorporates testability into a design. These developments are all welcome, but a key ingredient is missing—the commitment of upper management to implementing DFT strategies as part of a corporate philosophy. Until design engineers are convinced that they’re part of a team whose goal is to get a reliable, manufacturable product out the door, then the “over the wall” ways of the past will stay with us.

---

AT&T Microelectronics

CIRCLE NO. 54
WHAT IS RISC '93: RISC '93 is the premier annual gathering of hardware designers and software developers involved with RISC system architectures; RISC processors, ASIC cores and peripheral ICs; RISC programming and debugging; and the design of RISC-based systems for general-purpose computing, embedded and realtime applications.

THE ATTENDEES: RISC '93 is a down-to-earth conference aimed at both hardware and software engineers and engineering managers responsible for the design and development of products based on RISC processors. Specifically, RISC '93 is targeted at individuals with a solid background in electronic/computer system design and development (both hardware and software), as well as applications programming, who are looking for the most up-to-date information on the design of RISC-based computers, the design of embedded and realtime RISC systems, programming RISC-based systems, designing ASICs with RISC cores, and specifying and integrating RISC development tools into the overall product development environment.

THE FORMAT: TOTAL IMMERSION
RISC '93 has been designed as an intensive 3-day program that will place all participants in a total immersion environment where they'll have the opportunity to attend:

- Half-day tutorials that will help clarify the intricacies of the major RISC processor architectures.
- A variety of one-hour lectures that focus on specific aspects of RISC architectures, RISC-based hardware design, programming techniques, compilers, and development tools.
- Multipaper, application-focused sessions consisting of 20-minute presentations by system designers and software developers who've already implemented RISC designs in applications ranging from workstations, graphics, image processing, communications, signal processing and embedded control.
- A luncheon on each day of the conference that will be highlighted by an address from a recognized authority on RISC architecture or RISC-based designs.
- Demonstration workshops where attendees will be able to get hands-on exposure and detailed information about the latest RISC processors, compilers and development tools offered by leading hardware and software vendors.
- Free-wheeling "rap" sessions, led by RISC experts, on the first two evenings of the conference. Conference participants will have the chance to explore and exchange ideas about any aspect of RISC and RISC-based system design in an informal atmosphere of shirt sleeves, beer and pizza.

RISC '93 Conference is sponsored by COMPUTER DESIGN • One Technology Park Drive, Westford, MA 01886
TEL: 508-392-2124 • 800-223-4259 • FAX: 508-692-7780 • Contact: Patti Kenney, RISC '93 Conference Coordinator
PARTICIPATION: Suppliers of RISC processors, ASICs, peripheral ICs and memory, compilers, and development tools, as well as system designers and programers working on RISC-based designs and applications, are invited to participate in RISC '93 by presenting tutorials, lectures, 20-minute application-focused papers or leading one of several evening "rap" sessions. A variety of topics that would be of interest to attendees is suggested in the Call for Papers for RISC '93. All presenters receive free admission of all tutorials, lectures, applications sessions, luncheons, rap sessions and a copy of the proceedings.

Suppliers of RISC hardware/software or development tools may also participate in RISC '93 by sponsoring a demonstration workshop. These workshops will be two hours in length and will be the last formal sessions of the day. They're intended to provide attendees with an intimate, hands-on exposure to a supplier's product or service. The cost of sponsoring these sessions is $1500 for one two-hour workshop, $2700 for two workshops on successive days and $3500 for a workshop on each of the three days of the conference. One complimentary admission to RISC '93 for each workshop sponsored is included in the fee.

RISC '93 is open to all system designers and software developers and the tuition fee covers admission to any tutorial, lecture, application session, demonstration workshop, evening rap session, and the three conference luncheons.

TUITION:
$495. Early Bird—Register by Dec. 3, 1992
$595. If registered between Dec 4, 1992 - Jan 21, 1993
$695. After Jan 22, 1993

(Tuition includes lunch on all three days as well as snacks and refreshments during the rap sessions.)
Company group discounts available.

HOTEL ROOMS:
The single room rate at the Hyatt Regency is $108. Call the hotel directly at 415-347-1234 Be sure to tell them that you are attending RISC '93.
DESIGN STRATEGIES: ROBOTICS AND AUTOMATION

Event-driven strategy wins for robot test handler

In 1988, engineers at Taltec (Goleta, CA) worked with a customer to develop a robotic pick-and-place machine, one that could place surface-mount devices—from very small chips to large devices with hundreds of 25-mil pitch leads—on a very large PCB. Originally a consulting firm, Taltec saw this project as an opportunity to craft its own system platform, one it could migrate to other projects in the future. Taltec's designers created a general system architecture for robotics based on a distributed control scheme. To this core technology, custom features could be added as required. After building several machines for different customers, Taltec found an opportunity to use its technology in the tester/handler business.

At the heart of this architecture is what Taltec calls a WorkCell Controller (WCC), a PC/AT-based computer from which Taltec's software controls the various hardware subsystems of the robotic system. These subsystems include a robot controller to control the robot in real time and a vision processor to control the vision functions in real time. Taltec's strategy was to use standard off-the-shelf I/O hardware while investing its development efforts in the software architecture needed to glue it all together.

No simple task
"We enhanced the software to make it more flexible for tester/handler needs," recalls Tom La Rovere, president of Taltec. "The job of the test handler robot is simple: pick up an untested part from the tray, put it into a test socket, communicate with the

Jeffrey Child, Senior Editor
Your success depends on having a firm grasp on today's performance choices. Technology, however, is only the beginning. Effectively integrating those choices demands performance from hardware and software alike. You should have the flexibility to select from standard or custom configurations.

Heurikon provides you with total solutions. Whether you use VME, Multibus or a proprietary platform we deliver you the real-time performance for your application. With Heurikon you have more than a grasp on the problem, you've got a handle on the solution!
The major functional blocks of the THS-120 are a robot controller, the WorkCell Controller (WCC) and various I/O modules. The WCC is a 33-MHz 386 PC/AT that Taltec builds from off-the-shelf parts which fit into a 19-in. rack. A parallel multiplexed interface (PAMUX) connects the WCC to the I/O modules. Those modules provide opto-isolated analog and digital I/O over which the WCC communicates with the robot and the touch screen operator console. Because as many as eight RS-232 lines are connected to the WCC controller in a typical system, an intelligent I/O card resides in the WCC to handle interrupts.

THS-120 in action
A typical sequence begins when the WCC sends a start signal to the customer's test equipment. The test equipment runs its test and returns with a "bin" signal and a test signal. The THS-120 latches up to the signals, making them available to the robot, which determines where it should put the part. As soon as the end-of-test signal returns from the customer's tester, the test press is retracted, permitting the robot to unload the part from the test socket and load the next part.

Once that sequence starts, the robot handles these functions locally, and the WCC, for the most part, sits back as a monitor, waiting for some event such as a bin going empty or an output bin becoming full. When such events occur, the robot informs the workstation controller and the WCC is programed to take effective recourses.

THS-120 in action

Three-part software
The THS-120's software consists of three major elements: the WCC software, robot control software and vision processor software. On the WCC resides the QNX real-time operating system and Taltec's Event Action Software (EASE).

A table-driven approach is used. When a customer selects a particular test protocol and part to be tested, for example, that data is held on file by the WCC. The robot receives this data and uses it to set up the appropriate conditions for robot control.

While the EASE software is written in C, code for robot control is in a BASIC-like language providing typical robot commands such as "Move to Point." Such commands control the trajectory and type of motions performed by the robot. Logic expressions such as WAIT and IF are also used in this software.

The vision system is programmed in a Pascal-like language. Again, a table-driven approach is used. Tabular data is sent to the WCC, which forwards it on to the vision processor. The vision processor then runs its own program. It sends back predefined messages to the WCC, such as error codes or information about where the center of the part is.

Customer input crucial
Taltec's most recent version of its test-handler machine was greatly influenced by input from its latest customer, Vitesse Semiconductor (Camarillo, CA). Specializing in

customer's test equipment, receive from that equipment a sorting signal, and then place the part into an appropriate sorting tray.

"Very straightforward and simple, or so we thought," La Rovere laughs. "Unfortunately—or, I guess, fortunately for us—it's not that simple. With this type of robotic system, and in this type of application, it's not the task that's difficult. It's the recourses that must be dealt with. By recourses I mean the unexpected events coming from the environment that you have to decide how to respond to. The operator, for example, does something you can't predict. That's where the simple structure decomposes into something much more difficult. That has driven us to orient our software to deal with those kinds of issues and we developed a flexible software architecture."
high-performance GaAs ASICs, Vitesse wanted to boost its manufacturing efficiency by automating the process of testing its ICs. The Taltec machine also had to handle Vitesse's wide variety of custom packages, as well as the special power requirements of its GaAs chips.

After rating the available test handlers on the market, Vitesse had difficulty finding a machine that fit all its requirements. "We wanted a machine that could deal with various packages, a lot of which weren't defined at the time," says Marc Van Dyke of the technical staff at Vitesse. "We test very high-speed parts with high pin counts, so the test equipment we buy is some of the most expensive on the market. As a result, our test floor operations are very costly. So we wanted to keep the setup cost and the changeover time between package types as small as possible."

According to La Rovere, "As an ASIC vendor, Vitesse builds a variety of different products. They needed to be able to handle different packages in the system with a lot of different mechanical fixtures. We were also incorporating a vision system programmed to look at the different devices, and place them accurately into the test socket."

One of the initial design decisions Taltec made was in the choice of QNX from Quantum Software Systems (Kanata, Ontario) as its operating system. Jeffrey Schaffer, a consultant to Taltec, played a major role in OS-related software design. He considers QNX to be an excellent choice. "Message passing is the key," he says. "Using a multitasking operating system lets us write individual tasks to model the sections of the machine, so the natural modular structure of the software falls out from designing the machine that way.

"Earlier, Tom [La Rovere] mentioned error recourse as motivating the event-driven philosophy for design of the system. It turns out that we handled almost every interaction based on this event-driven philosophy. Even in the software we designed ourselves, the Event Action Software (EASE), events that occur are modeled as messages," adds Schaffer. The advantage of this approach was brought home when the team started to draw block diagrams describing hardware and software. "We saw that the hardware and software really mirror one another very closely," he says.

While other choices for an OS might have sufficed, and Ready Systems' VRTX and Integrated Systems' psos+ were considered, those operating systems weren't as high-level as QNX. "QNX is a full, high-level system, much like an early UNIX, yet much more refined," says Schaffer. "Our event-driven control scheme fits very well with the message-passing capabilities of QNX."

For the THS-120's touch screen, Taltec designers chose to implement the graphical user interface software in their own script language. This makes it easy to adjust to the user interface; it can be done by simply changing a few lines of script language, rather than rewriting C code.

Just as Taltec bought an off-the-shelf OS, it also could have bought an off-the-shelf control software. But commercially available software packages were between $25,000 and $50,000, too much for this project. And it wasn't clear that a third-party software package would suit the project's needs anyway. That led to the decision by the Taltec team to develop its own director scheme to run the test floor.
YOU ARE CORDIALLY INVITED TO THE... 

Computer Peripherals Invitational Computer Conference

featuring new technology presentations and product displays

Request your Complimentary Invitation and Agenda

OEMs, Systems Integrators, VARs — If you are involved in the purchasing, design, or specification of peripheral products... you should be here!

Indicate your conference selection below and return this section by FAX or mail.

- Newton, MA Sep 09 '92
- Dallas, TX Sep 22 '92
- Portland, OR Oct 22 '92
- Irvine, CA Jan 07 '93
- San Jose, CA Feb 09 '93
- Minneapolis, MN Mar 04 '93
- Austin, TX Mar 25 '93
- Denver, CO Apr 08 '93
- Nashua, NH Apr 20 '93

Copy your business card here
FAX to: (714) 476-9969

Dataquest

3990 Westerly Place, Suite 100, Newport Beach, CA 92660 Tel: (714) 476-9117 Fax: (714) 476-9969

CIRCLE NO. 59
I DESIGN STRATEGIES: ROBOTICS AND AUTOMATION

The challenge was to create a scheme that was simple for the user, and yet that was still complex enough to let the you work at a high level. For Taltec's earlier pick-and-place machines, that meant finding a way to sequence the os, and to respond to events and generate recourses.

I Director controls system

At the heart of the entire software system—and, therefore, of the entire system—is the Director. The Director controls systemwide behavior. This control is critical in cases where an error occurs that involves more than one subprocess. If the part doesn't get placed right, that error involves the robot, for example, but it also involves the vision system, which has to reinspect the part.

Each hardware subsystem of the machine has its own software program. There's a program that deals with the PAMUX, the digital I/O control points. Similarly, the robot has its own program, which passes event messages over the serial port. “We think of all these messages as events,” says Dan Eliason, software engineer at Taltec. “These programs are all capable of generating messages. The PAMUX, for example, watches its input ports; if a certain state change happens, it generates an event.”

Besides responding to events from the subprograms, the Director is also responsible for reading a special script language. If you need to make changes in system configuration, you don't have to write any C code. Instead, you rewrite the script. The Director reads the script language, compiles it on the fly, then executes the reaction accordingly. “If a user wanted a light to turn on, for example, when the light curtain was broken, he could just change one line in the script language and it’s done,” says Eliason. “The customer has the flexibility to make changes, or we can make the change for him.”

One change made for the Vitesse product was to replace the ASCII terminal touch screen with a color touch screen. “We had a decision at that point about whether to use the QNX window function calls to do the graphics for the touch screen in a C program,” says Eliason. “Instead, we thought we’d try something more flexible, so that if we needed to use a different machine, we could easily do that just by rewriting the actions instead of sections of C code.” This led the Taltec team to craft a script language for its user interface as well.

QNX already provides an interface editor that lets you create windows using a mouse, but you still have to write a program to use those windows. “We decided to write a user handler or server that would use a similar script language to the one we use with our Director,” says Eliason. “So when the user does something with a window, like pushing a button, that becomes an event just for this user interface. And it has a script language to tie that event to the opening of further windows or generating events from the Director.” With this approach, Taltec could keep to its event-driven philosophy.

I Lessons learned

As the design progressed, Eliason had some insights about control software structure, and the prospect of using new technologies in future projects. “During this project, we talked a lot about the issue of expert systems,” he says. “We surmised that we could use an expert system as a Director. It could determine systemwide things that need to happen based on events that occurred. An expert system operates by scanning lists of conditions; when the conditions are met, it fires the rule or does the list of activities. Our system is structured so that each server is responsible for recognizing things that need systemwide attention.

“One of the things I’d like to explore for the future,” contemplates Eliason, “is a sort of event-posting architecture.” If an event's important, it gets posted to the Director. But the Director, rather than taking immediate action on the event, can scan its rule list. It could combine the event with other events from other servers to recognize important systemwide conditions.

Would the use of an expert system make any difference in performance? “It’s really a philosophical point, because I haven’t yet run into an event that we couldn’t address with our current architecture,” concludes Eliason.
<table>
<thead>
<tr>
<th>ISSUE</th>
<th>SPECIAL REPORT</th>
<th>TECHNOLOGY FOCUS</th>
<th>PRODUCT FOCUS</th>
<th>DESIGN STRATEGIES</th>
<th>OEM INTEGRATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>JANUARY</td>
<td>Verilog and VHDL</td>
<td>• DSP development tools</td>
<td>C cross compilers</td>
<td>Networking</td>
<td>• Secondary &amp; mezzanine buses</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Disk drive controllers and associated ICs</td>
<td></td>
<td></td>
<td>• Backplanes &amp; enclosures</td>
</tr>
<tr>
<td>FEBRUARY</td>
<td>Bridging the buses</td>
<td>• Software tool integration</td>
<td>Flash EEPROMs</td>
<td>Process control</td>
<td></td>
</tr>
<tr>
<td>*</td>
<td>* Buscon West, EDAC/EuroASIC</td>
<td>• ICs for desktop video</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MARCH</td>
<td>Memory architectures</td>
<td>• Multithreaded operating systems</td>
<td>SCSI host adapter boards</td>
<td>Data acquisition</td>
<td></td>
</tr>
<tr>
<td>*</td>
<td>* RISC '93, PCB Design</td>
<td>• PC-Based CAE/CAD Tools</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>APRIL</td>
<td>Embedded Computer Conference</td>
<td>• PC/AT architectures in embedded applications</td>
<td>Device programmers</td>
<td>Peripherals</td>
<td></td>
</tr>
<tr>
<td>*</td>
<td>* EMBEDDED COMPUTER CONFERENCE (ECC) SHOWGUIDE*</td>
<td>• Developments in 3-V ICs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MAY</td>
<td>CICC</td>
<td>• Evaluating simulation strategies</td>
<td>Video D-A converters</td>
<td>Portable computers</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Benchmarking programmable devices</td>
<td></td>
<td></td>
<td>• Networking interfaces,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Bus standards</td>
<td></td>
<td></td>
<td>standards &amp; components</td>
</tr>
<tr>
<td>JUNE</td>
<td>High-level synthesis and architectural design</td>
<td>• Small form factor VME</td>
<td>Ultra-fast SRAMs</td>
<td>Graphics</td>
<td></td>
</tr>
<tr>
<td>*</td>
<td>* DAC</td>
<td>• Data compression standards and ICs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JULY</td>
<td>Advances in IC packaging</td>
<td>• Interfaces for DSP</td>
<td>Real-time kernels and operating systems</td>
<td>Imaging</td>
<td></td>
</tr>
<tr>
<td></td>
<td>* Fuzzy Logic '93</td>
<td>• Fuzzy/neural update</td>
<td></td>
<td></td>
<td>• Display devices &amp; monitors</td>
</tr>
<tr>
<td>AUGUST</td>
<td>Trade-offs in programmable devices architectures</td>
<td>• RISC in real time</td>
<td>Emulators</td>
<td>Robotics</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Integrating testability into the ASIC design process</td>
<td></td>
<td></td>
<td>• Power sources</td>
</tr>
<tr>
<td>SEPTEMBER</td>
<td>Software testing and quality</td>
<td>• Futurebus+</td>
<td>Low-power DRAMs</td>
<td>Instrumentation</td>
<td>• Interconnects</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Integrating testability into the ASIC design process</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Futurebus+</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OCTOBER</td>
<td>Analog &amp; Mixed-Signal Design Konference SHOWGUIDE**</td>
<td>• Hardware/software trade-offs in multiprocesssing</td>
<td>Logic analyzers</td>
<td>Simulation</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Network interfaces and interface ICs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NOVEMBER</td>
<td>Conex</td>
<td>• PLD design tools</td>
<td>High-resolution A-D converters</td>
<td>Communications</td>
<td>• Mass storage</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Mezzanine buses</td>
<td></td>
<td></td>
<td>(disk, tape, CD-ROM, memory cards)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Full-system simulation</td>
<td>VME CPU Boards</td>
<td>Supercomputers</td>
<td></td>
</tr>
<tr>
<td>DECEMBER</td>
<td>Designing the next generation of portable computers</td>
<td>• FAX/modern ICs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>*</td>
<td></td>
<td>• Mass storage (disk, tape, CD-ROM, memory cards)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Contact Computer Design for circulation, rates and closing dates

For more information, contact any of us:
- PUBLISHER: David L. Allen, 508-392-2113
- ASSOCIATE PUBLISHER: Tim L. Tobock, 508-392-2116
- NATIONAL ACCOUNTS MANAGERS: WESTFORD, MA, Tim Pritchard, 508-392-2217
- SPRING, TX, Eric Jever, 713-353-0309 Fax 713-288-8503
- SAN JUAN, CA, Diane Palermo, 408-371-7551 Fax 408-371-6209
- STRATEGIC ACCOUNTS REPRESENTATIVES:
  - WESTFORD, MA, Sue Nafzick, 508-392-2118 Fax 508-392-2259
  - David Singer, 508-392-2319
  - INTERNATIONAL SALES OFFICES:
    - SURREY, ENGLAND, David Randle, 81-770-1109 Fax 81-770-9779
    - PARIS, FRANCE, Daniel R. Bernard, 3-38-14-6780 Fax 01-38-14-7114
    - MUNICH, GERMANY, Andreas Braune, 89-90-30-008 Fax 89-90-30-008
    - MILAN, ITALY, Luigi Rancati, 2-70-30-008 Fax 2-70-30-008
    - TOKYO, JAPAN, Toshio Egusa, 81-33-536-5404 Fax 03-336-5400
- ASIA, AUSTRALIA, NEW ZEALAND, Tom Gormley, 852-833-281 Fax 834-582

CIRCLE NO. 61
**I RISC needs more channels**

RISC processors, with their pipelined architectures and high pin counts, make life challenging for emulator vendors. The Am29000 RISC processor from Advanced Micro Devices (Austin, TX), for example, has a three-bus architecture that requires from 200 to 250 channels of trace to provide a view of what's happening. More channels are needed than the processor has pins, so an emulator can view not only what's going on inside the chip but everything that's going on around it. "Some emulators force you to switch back and forth between looking at control signals and two buses and looking at three buses and no control signals," remarks Norbert Laengrich, president of Embedded Performance (Santa...
<table>
<thead>
<tr>
<th>Model</th>
<th>Speed (MHz)</th>
<th>Processor(s) supported</th>
<th>Overlaid memory (bytes)</th>
<th>No. of hardware breakpoints</th>
<th>No. of break point locations</th>
<th>Trace buffer depth (bits)</th>
<th>Performance analysis</th>
<th>Price</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Applied Microsystems</td>
<td>16, 25</td>
<td>68330, 68340, 68333</td>
<td>—</td>
<td>4</td>
<td>2</td>
<td>—</td>
<td>no</td>
<td>$7,500</td>
<td>Plugs directly into target device.</td>
</tr>
<tr>
<td>CodeTAP CPU32</td>
<td>33</td>
<td>#80C0A, CF</td>
<td>—</td>
<td>4</td>
<td>2</td>
<td>8k</td>
<td>no</td>
<td>$4,995</td>
<td>Plugs directly into target device.</td>
</tr>
<tr>
<td>CodeTAP 386</td>
<td>33, 44</td>
<td>Am3960DX/DXL, 686DX</td>
<td>—</td>
<td>4</td>
<td>2</td>
<td>8k</td>
<td>yes</td>
<td>$16,000</td>
<td>Supports dynamic bus sizing, real-time pin reprogramming. Correlates instructions with registers and bus cycles.</td>
</tr>
<tr>
<td>EL3200 CPU32</td>
<td>16, 25</td>
<td>68330, 68340, 68333</td>
<td>4M</td>
<td>16</td>
<td>4</td>
<td>8/32k x 144</td>
<td>yes</td>
<td>$28,575</td>
<td>Supports pipelining, data and instruction cache, burst mode, multiple bus widths.</td>
</tr>
<tr>
<td>EL3200 960</td>
<td>33</td>
<td>#80C0A, CF</td>
<td>4M</td>
<td>16</td>
<td>4</td>
<td>16k x 139</td>
<td>no</td>
<td>$24,050</td>
<td>Runs on Sun, PC, VAX; can be accessed via Ethernet.</td>
</tr>
<tr>
<td>EL3200 68020/030</td>
<td>33</td>
<td>68020/030</td>
<td>2M</td>
<td>6</td>
<td>4</td>
<td>16k x 144</td>
<td>yes</td>
<td>$20,000</td>
<td>Same as above.</td>
</tr>
</tbody>
</table>

| Embedded Performance       |            |                        |                         |                              |                            |                          |                     |                  |                                               |
|----------------------------|            |                        |                         |                              |                            |                          |                     |                  |                                               |
| SYS29K                     | 25         | Am29000, Am29005, Am29050 | 256k - 2M              | 50                           | 16                         | 2096                     | yes                 | $14,995 - $25,000 | Hosted to PC, Sun-3, Sun-4, VAX-VMS, HP9000, Ethernet option. |
| SYS29K-LYNX                | 25         | Am290000/05, Am29050   | 256k - 4M              | 50                           | 16                         | 2048                     | yes                 | $20,000 - $30,000 | Hosted on PC, Sun-3, Sun-4, HP9000, VAX-VMS via Ethernet and high-speed serial interface. |
| SYS29K-PUMA                | 25         | Am29000, Am29005, Am29050 | 256k - 4M              | 50                           | 16                         | 2096                     | yes                 | $20,000 - $35,000 | Same as above.                                |
| SYS29K-TURBO               | 33, 40     | Am29000, Am29005, Am29050 | 256k - 4M              | 50                           | 16                         | 8k - 32k                 | yes                 | $25,000 - $40,000 | Same as above.                                |
| SYS33K                     | 25         | LR33000, LR33050       | 256k - 4M              | 50                           | 16                         | 8k - 32k                 | optional            | $27,000 - $40,000 | Same as above.                                |
| SYS-R3000                  | 25         | R3000, R3000A, R3001   | 256k - 4M              | 50                           | 16                         | 8k - 32k                 | optional            | $25,000 - $40,000 | Same as above.                                |
| SYS-R3051                  | 25         | R3051, R3052, R3081    | 256k - 4M              | 50                           | 16                         | 8k - 32k                 | optional            | $25,000 - $40,000 | Hosted to PC, Sun-4, MIPS via Ethernet or high-speed serial interface. |
| SYS-SPARCl                 | 25         | CY7C611                | —                      | 50                           | 16                         | 8k - 32k                 | optional            | $25,000 - $45,000 | Same as above.                                |

| Hewlett-Packard            |            |                        |                         |                              |                            |                          |                     |                  |                                               |
|----------------------------|            |                        |                         |                              |                            |                          |                     |                  |                                               |
| HP64747B                   | 40         | 68030, 68EC030         | 0 - 2M                  | 8                            | 8                           | 1k                       | yes                 | $9,000 - $24,700 | X11/motif-based graphical interface, available high-level debug, real-time software performance analysis. Same as above. |
| HP64748A                   | 33         | 68020, 68EC020         | 0 - 2M                  | 8                            | 8                           | 1k                       | yes                 | $6,000 - $21,700 | Same as above.                                |
| HP64750A                   | 25         | 68040, 68EC040         | 512k                   | 8                            | 8                           | 1k                       | no                  | $33,900 - $44,600 | Same as above.                                |
| HP64751A                   | 16         | 68340                  | —                      | 8                            | 8                           | 1k                       | yes                 | $6,000 - $21,700 | X11/motif-based graphical interface, available high-level debug, real-time software performance analysis. Available on HP9000s, Sun workstations, PCs. |
| HP64760A/701               | 25, 33     | 680KA/K8, 686SA/38     | 2M - 4M                | 16                           | 32                         | 1024                     | yes                 | $24,000 - $26,000 | Same as above.                                |
| HP64772A                   | 50         | AT&T DSP23C            | 64k                    | 8                            | 8                           | 1k                       | no                  | $42,000          | —                                             |
| HP64774J                   | 25         | Am290000/05            | 0 - 4M                 | 8                            | 8                           | 1k                       | no                  | $38,000          | —                                             |
| HP64774K                   | 25         | Am29050                | 0 - 4M                 | 8                            | 8                           | 1k                       | no                  | $38,000          | —                                             |

<p>| Huntsville Microsystems    |            |                        |                         |                              |                            |                          |                     |                  |                                               |
|----------------------------|            |                        |                         |                              |                            |                          |                     |                  |                                               |
| HMI-200-68020              | 16 - 33    | 68020, 68EC020         | 256k - 2M              | 4                            | 4                           | 8k x 104                 | yes                 | $12,000 - $20,000 | Includes SourceGate emulator control and debugger software. Same as above. |
| HMI-200-68030              | 16 - 33    | 68020, 68EC030         | 256k - 2M              | 4                            | 4                           | 8k x 104                 | yes                 | $12,000 - $20,000 | Same as above.                                |
| HMI-200-68040              | 25         | 68040, 68EC040, 68LC040 | 256k - 2M              | 4                            | 4                           | 8k x 104                 | yes                 | $25,000          | Same as above.                                |</p>
<table>
<thead>
<tr>
<th>Model</th>
<th>Speed (MHz)</th>
<th>Processors supported</th>
<th>On-chip memory (bytes)</th>
<th>No. of hardware breakpoints</th>
<th>No. of breakpoints per function</th>
<th>Trace buffer depth (bits)</th>
<th>Performance analysis</th>
<th>Price</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Microtek International</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Circle 305</td>
<td></td>
</tr>
<tr>
<td>MICE-III</td>
<td>25</td>
<td>68020/30, 68EC020/30</td>
<td>1M</td>
<td>5</td>
<td>Up to 8</td>
<td>2k x 96 or 32k x 96</td>
<td>optional</td>
<td>$14,000 - $16,000</td>
<td>High-level language debug support optional.</td>
</tr>
<tr>
<td>MICE-V</td>
<td>33</td>
<td>256, 386, 386SX, 486, 486SX</td>
<td>128k x 1M</td>
<td>8</td>
<td>4</td>
<td>8k x 141</td>
<td>no</td>
<td>$15,000 - $32,000</td>
<td>Same as above.</td>
</tr>
<tr>
<td>PowerPack</td>
<td>40</td>
<td>68330, 68331, 68332, 68333, 68334</td>
<td>256k x 1M</td>
<td>8</td>
<td>4</td>
<td>128k x 96 or 256k x 96</td>
<td>optional</td>
<td>$9,995 - $15,000</td>
<td>Trace collected at MPU clock level.</td>
</tr>
<tr>
<td><strong>Nohau Corporation</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Circle 306</td>
<td></td>
</tr>
<tr>
<td>EMUL16/300-PC</td>
<td>16</td>
<td>68331, 68332, 68340</td>
<td>4M</td>
<td>1</td>
<td>3</td>
<td>512k</td>
<td>yes</td>
<td>$4,000 - $8,000</td>
<td>High-level debugger.</td>
</tr>
<tr>
<td><strong>Orion Instruments</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Circle 307</td>
<td></td>
</tr>
<tr>
<td>8800</td>
<td>40</td>
<td>68330, 68331, 68332, 68334</td>
<td>12k x 2M</td>
<td>65K</td>
<td>4</td>
<td>128k x 512</td>
<td>—</td>
<td>$8,800</td>
<td>DOS extender on 386 PC host, high-speed parallel interface to host.</td>
</tr>
<tr>
<td><strong>Sophia Systems and Technology</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Circle 308</td>
<td></td>
</tr>
<tr>
<td>MultiSTAC</td>
<td>25</td>
<td>386/386SX</td>
<td>16M</td>
<td>22</td>
<td>8</td>
<td>8k x 154 or 32k x 154</td>
<td>yes</td>
<td>$15,000 - $17,000</td>
<td>Source-level debugger, fast download.</td>
</tr>
<tr>
<td>MultiSTAC</td>
<td>25</td>
<td>487SX/DX</td>
<td>Up to 16M</td>
<td>22</td>
<td>8</td>
<td>154 bits x 8k or 32k bus cycle</td>
<td>yes</td>
<td>$17,000 - $30,000</td>
<td>Microsoft windows-based source level debugger, 9 x 6 x 1-in. module, download speed of 1 Mbyte/s, eight-level trigger.</td>
</tr>
<tr>
<td>MultiSTAC</td>
<td>25, 50</td>
<td>68EC020/30, 487SX</td>
<td>16M</td>
<td>22</td>
<td>8</td>
<td>8k x 154 or 32k x 154</td>
<td>yes</td>
<td>$15,000 - $19,000</td>
<td>Same as above.</td>
</tr>
<tr>
<td>MultiSTAC</td>
<td>33</td>
<td>486DX/DX2</td>
<td>16M</td>
<td>22</td>
<td>8</td>
<td>8k x 154 or 32k x 154</td>
<td>yes</td>
<td>$19,000</td>
<td>Same as above.</td>
</tr>
<tr>
<td>MultiSTAC</td>
<td>33</td>
<td>68020/30</td>
<td>16M</td>
<td>22</td>
<td>8</td>
<td>8k x 154 or 32k x 154</td>
<td>yes</td>
<td>$15,000 - $17,000</td>
<td>Same as above.</td>
</tr>
<tr>
<td>MultiSTAC</td>
<td>40</td>
<td>68EC030</td>
<td>16M</td>
<td>22</td>
<td>8</td>
<td>8k x 154 or 32k x 154</td>
<td>yes</td>
<td>$28,000</td>
<td>Same as above.</td>
</tr>
<tr>
<td>MultiSTAC</td>
<td>50</td>
<td>68030</td>
<td>16M</td>
<td>22</td>
<td>8</td>
<td>8k x 154 or 32k x 154</td>
<td>yes</td>
<td>$28,000</td>
<td>Same as above.</td>
</tr>
<tr>
<td><strong>Step Engineering</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Circle 309</td>
<td></td>
</tr>
<tr>
<td>Eclipse JTAG</td>
<td>16</td>
<td>Am29200, Am29205</td>
<td>515k - 6M</td>
<td>—</td>
<td>1k x 256</td>
<td>no</td>
<td></td>
<td>$7,995</td>
<td>Integrated SDBGUXDBGUG debugger environment.</td>
</tr>
<tr>
<td>Eclipse/LX</td>
<td>up to 25 MHz</td>
<td>Am29000, Am29003, Am29003, Am29005, Am29200, Am29205</td>
<td>512k - 6M</td>
<td>3</td>
<td>16</td>
<td>32k x 256 bits</td>
<td>yes</td>
<td>$14,950</td>
<td>Universal support for all 29K family integrated SDBGUXDBGUG debugger environment.</td>
</tr>
<tr>
<td>Eclipse 29K</td>
<td>up to 40 MHz</td>
<td>Am29000, Am290030, Am290030, Am29200, Am29205</td>
<td>512k - 6M</td>
<td>63</td>
<td>16</td>
<td>32k x 256 bits</td>
<td>yes</td>
<td>$16,675</td>
<td>Universal support for all 29K family, integrated SDBGUXDBGUG debugger environment.</td>
</tr>
<tr>
<td>Excel II 900/901/932</td>
<td>up to 50 MHz</td>
<td>M866730/31/32</td>
<td>512k - 6M</td>
<td>5</td>
<td>1</td>
<td>32k x 256 bits</td>
<td>no</td>
<td>$15,875</td>
<td>Integrated to XDBG, X-RAY debugger.</td>
</tr>
<tr>
<td>Express I</td>
<td>25</td>
<td>960CA/CF</td>
<td>512k - 6M</td>
<td>9</td>
<td>1</td>
<td>8k x 256</td>
<td>no</td>
<td>$17,950</td>
<td>Integrated SDBGUXDBGUG debugger environment, cache-on support, executes reconstruction breakpoints. Same as above.</td>
</tr>
<tr>
<td>Express II</td>
<td>33</td>
<td>960CA/CF</td>
<td>512k - 6M</td>
<td>9</td>
<td>1</td>
<td>8k x 256</td>
<td>no</td>
<td>$23,450</td>
<td>Integrated SDBGUXDBGUG debugger environment, range breakpoint (match-words) with qualifiers, cache-on support.</td>
</tr>
<tr>
<td>Express III</td>
<td>40</td>
<td>960CA/CF</td>
<td>512k - 6M</td>
<td>68</td>
<td>16</td>
<td>32k x 256</td>
<td>yes</td>
<td>$36,950</td>
<td>Integrated SDBGUXDBGUG debugger environment, range breakpoint (match-words) with qualifiers, cache-on support.</td>
</tr>
</tbody>
</table>
Hewlett-Packard has added real-time operating system measurement capability to its 64700 series of emulators. This new tool lets you trace the flow of OS activity through your system. The software displays this trace activity in the actual native service call mnemonics of your OS (middle window). Users can trace all OS service calls, including input parameters and return values.

Looking for the best in a real-time multitasking kernel?

Since 1978, KADAK has provided products, documentation and technical support to those who absolutely insist on the best. It's one reason why more than 1,000 developers have come to count on KADAK for our AMX real-time multitasking kernel and more.

You'll marvel at the comprehensive, simple-to-follow AMX manual that will assist you in the development of virtually any application. You'll also appreciate the prompt, courteous service you'll receive from KADAK product support people if you should ever need assistance.

All this, plus you will be given source code and automatic software updates for a full year after purchase. And, with AMX, there are no royalties to pay.

For further information on the KADAK AMX Real-time Multitasking Kernel contact us at our offices. Phone: (604) 734-2796 Fax: (604) 734-8114

Count on KADAK.

KADAK Products Ltd. Setting real-time standards since 1978. 206-1847 West Broadway, Vancouver, BC, Canada, V6J 1Y5

AMX is a trademark of KADAK Products Ltd. All trademarked names are the property of their respective owners.

Clara, CA). “That can be frustrating to designers when they're trying to debug because they really want to look at everything.”

In general, RISC chips, especially those based on MIPS, SPARC, 29000, and 88000 architectures, need more channels of trace than there are pins on the chip. “That’s something that’s often overlooked,” says Laengrich. “Each of the RISC microprocessors needs extra channels for its own reasons.” SPARC chips, for example, have two buses—a data/instruction bus and an address bus—and these buses are multiplexed. According to Laengrich, “[In the SPARC chip,] on every cycle you get two values on the bus. To really see what’s going on in that case, the emulator needs to demultiplex those addresses—or data values as data instructions—and present them in parallel to the trace control.” By demultiplexing the buses, you take a 32-bit bus and turn it into two 32-bit buses. Again, that demands more channels of trace.

Embedded Performance supports several families of RISC chips with its Turbo emulator architecture. Each emulator provides from 200 to 256 channels of trace. The Turbo emulator architecture supports 33- and 40-MHz clock rates and offers 8-kbyte trace buffers as standard, with 32 kbytes as an option.

Emulators from Sophia Systems (Palo Alto, CA) offer a feature called fetch triggering that addresses one of the subtleties of trace. Of the emulator’s 16 triggers, up to four may be set up as fetch triggers. You may, for example, want to trigger a trace if there’s a read from a particular address, but only if you’re executing in a certain area of the program. Sophia’s emulator lets you specify the address and value of the instruction that was fetched to cause a certain data value. As a result, you can trigger if a particular variable is set by one subroutine but not by others. “There isn’t anybody who’s yet figured out how, in real time, to trigger on a variable that’s on the subroutine stack,” claims Robert E. Hoffman, executive vice-president at Sophia Systems. “If you’re willing to stop when you get to the entry point of the function, and quickly record the address of the stack, then you can set up a trigger on the variable at that point. But nobody’s do-
ing it in full real time yet. With the fetch trigger you can do that.”

- **Tracing OS activity**

The way that trace is displayed by user interface software can also be a critical issue. Designers are accustomed to looking at software at the same level of abstraction at which they’re working. People designing in source code, for example, want to see trace information displayed in source-level code.

Hewlett-Packard (Colorado Springs, CO) has taken this concept a step further by outfitting its 64700 series of emulators to perform measurements for embedded designs that use real-time operating systems (RTOS). Don Logelin, an HP systems design engineer involved in the 64700 project, explains the usefulness of this capability. “When designers have a multitasking operating system,” he says, “they want to be able to view that information the same way they are used to dealing with it. Designers using RTOSs are used to dealing with the task names. They know what messages get passed between their tasks, and what semaphores they use. Unless you can display it at that level, they have to go through a very tough translation process.”

To perform the required OS measurements, HP uses a sophisticated sequencing and windowing mechanism. “If you have a shared OS task or a shared OS utility that’s called by a number of different tasks, for example,” says Logelin, “but you’re only interested in dealing with it when it gets called by a particular task, you can set up our emulator to trigger and set the storage qualifications to only pick up the data when that particular task is active and when that operating system routine is called. Without that type of sophistication in the emulator, a lot of measurements wouldn’t be possible.”

At present, HP provides measurements in the 65700 emulator for RTOSs such as Integrated Systems’ PSS5+ and Ready Systems’ VRTX32. This measurement capability, coupled with the emulator’s graphical user interface, helps you understand the flow of OS activity, track dynamic memory usage, isolate defects based on OS level-task qualifications, and perform time profiling of task durations.

**Why Settle For Second Best When You Can Have the Realtime, Real UNIX®?**

VenturCom provides VENIX™ operating systems for realtime and embedded realtime solutions on popular low-cost Intel® 386 and 486 processors. VENIX software is the enhanced, USL licensed, UNIX operating system—not a look-alike or a clone.

**VENIX System Software**
- Full Kernel Preemption
- Deterministic
- Priority Scheduling
- ROMable/Embeddable
- Contiguous File System
- 27 µs Interrupt Response

Call for our Realtime Technical Overview.

**VenturCom**

Industrial Strength UNIX
215 First Street, Cambridge, MA 02142
TEL 617-661-1230  FAX 617-577-1607

**THANK YOU!**

More and more of you have been rating *Computer Design* Number One in our readership studies. Thanks for the vote of confidence, and we’ll continue to live up to your expectations.
**NEW PRODUCT DEVELOPMENTS**

**SOFTWARE & DEVELOPMENT TOOLS**

**Programming tool integrates functions of UNIX utilities**

Recognizing that the majority of C programmers aren't currently using software engineering environments or, for that matter, CASE tools, ProCase has introduced a low-cost tool designed to make life easier for them.

Most programmers still handcraft code in a highly iterative "edit-compile-debug" cycle, and the tools they use are mostly utilities supplied with UNIX.

**Single-window functionality**

C/Spot/Run is a tool that integrates the functionality of such UNIX utilities as Grep, Lint and cscope within a single window so you can interactively select utility functions without shutting one utility down or changing windows. Grep is used to search a file or files for a pattern or string of characters and show file name and line reference for each occurrence. Lint is a C-program verifier that searches files for likely bugs. cscope is a cross-reference tool used to navigate within specified C-source files. C/Spot/Run combines semantic analysis, syntax checking, dependency analysis, and source code filtering, along with the ability to navigate through graphical representations of function calls.

While the UNIX utilities are file-oriented, C/Spot/Run looks at the code from a program/module perspective. Before code is linked and compiled, C/Spot/Run can parse all included code modules and establish a picture of the ones that will make up the compiled program. In parsing, C/Spot/Run also logs all semantic errors, which are listed in an exception report in a separate window. You can click on a listed error and be taken to the line of code in which the error occurs, and then expand your view to see lines of code preceding and following the line of interest.

**Maneuvering techniques**

To navigate quickly through a calling sequence, you click on a function and see the calling and called functions in a small window. You can then follow that path in a graphical representation and view the code of any function with a mouse click. C/Spot/Run supports dependency analysis so you can specify the language-dependent context in searching for a string. In this way, the system doesn't return every reference to each "i" or "j" in the program.

C/Spot/Run's program-wide cross-referencing lets you follow the impact of changes. The tool filters code to show only the source lines relevant to the task at hand, and can also filter the references to an identifier to give a quick view of dependencies.

The tool runs on Sparcstation workstations under SunOS 4.0 with Open Windows or on Hewlett-Packard 9000/700 systems under HP-UX 8.0 with HPVUE. Priced at $995, it will be distributed through UNIX Central.

---

Tom Williams

---

**C/Spot/Run at a glance**

- Single tool integrates functions of several UNIX utilities
- Automatically parses code before compilation
- Logs semantic errors and allows instant access to relevant code
- Shows calling sequences in graphical form with mouse-click navigation
- Filters code to show only references relevant to user's task
- Supports commonly used "edit-compile-debug" programming cycle

---

ProCase
3130 De La Cruz Blvd, Ste 100
Santa Clara, CA 95054
(408) 727-0714
Circle 352
Until now, there was just one thing missing from CPU32 development solutions.
The solution.

Introducing our newest development systems for the 68330, 68340 and 68F333 microcontrollers: emulators, CodeTAPs®, debuggers, simulators, language tools, and support services. Now you have a range of tools to match your needs throughout the development cycle. Only from Applied.

Smarter than your average tools.

Because these new 32-bit controllers are far more complex than their predecessors, you need a smarter solution. One that saves you weeks of development time.

For example, since you can reconfigure CPU pins, you have to be able to track the changes. Ours is the only system that can determine the correct function of each pin, transparently, and in real-time.

And our new intelligent trace disassembler provides the only accurate picture of register values correlated with instructions. It also gives you detailed timing data for performance analysis.

Applied's system solves one of your most critical productivity issues. Instead of mismatched tools that don't speak the same language, you can now work with integrated tools that share a common user interface.

A real solution costs less than you think.

Just because our CPU32 development tools are the best in their class doesn't mean you have to pay more for top performance. You'll be pleasantly surprised at how affordable these tools are.

Want to learn more?

We'll send you free product information and our latest Application Note on working with the complexities of the CPU32 controllers.

Just call Applied at 1-800-343-3659 (in WA, 206-882-2000) or return the card below.

And ask for your solution.

Send for FREE technical information.

Or call us at 1-800-343-3659 (in WA, 206-882-2000)

☐ Please send me product information about Applied's new development solutions for the following microcontrollers: ☐ 68330 ☐ 68340 ☐ 68F333

☐ Please send me your latest Application Note about the Motorola CPU32 microcontroller family.

☐ Please call me to arrange a demonstration.

Phone number ____________________________ Title ____________________________

Name ____________________________

Company ____________________________

Address ____________________________ Mail Stop ____________________________

City ____________________________ State __________ Zip ____________________________

Lite emulator does heavy duty

Huntsville Microsystems (HMI) has released its Lite series of emulators for the Motorola 68300 series of microcontrollers. The unit is the company's answer to the problem of emulation cost. While other emulator vendors have addressed the cost issue by offering emulation substitutes that lack trace capability, the Lite can do everything that makes an emulator an emulator. This includes 4k cycle trace, hardware breakpoints and complete emulation of the 68300-series chips. HMI's goal with the Lite is to make emulation technology available to users with limited funds.

Looking inside

The Lite offers thorough emulation of 68300 chips, including the proper tracing of show cycles—internal transfers which occur inside rather than outside the chip. To trace these cycles, the Lite takes advantage of special features on the chip that put the show cycles onto the bus where they can be accessed.

The problem of pipeline queues provides another example of the Lite's sophisticated tracing. On 68300 chips, instructions are prefetched and queued in a pipeline. The problem is that look-ahead logic on the chip may bypass instructions when a JUMP is encountered. So that these instructions aren't lost to the trace, the Lite emulator uses the same look-ahead logic. It dequeues the trace so that what actually gets executed is what's seen in the trace buffer.

Pesky Port E

A key issue in emulation is the ability to emulate a processor exactly without limiting its use. The 68300 chips have a port called Port E which is frequently used by emulator makers for this purpose. Port E has data-strobe and address-strobe acknowledge signals that normally can be used for emulation, but the port is also reconfigurable by the user for something else, such as I/O. If that's done, the data strobes and other signals are tied up and can't be used for emulation. The Lite emulator gets around the problem by using the chip select signals to access memory and exercise control, while bypassing Port E.

Integrated on the Lite is HMI's SourceGate debugger. It provides full emulator control integrated with source-level debugging and support for all major C and Ada compilers. You can host SourceGate on IBM PC-compatible or UNIX-based platforms. Communications are supported through a high-speed serial port (115.2-kbaud) and a parallel port for downloading code.

The emulator is configured with 256 kbytes of overlay RAM. It supports mapping of all chip select signals with dynamic bus sizing for 8- and 16-bit operations. In addition, two kbytes of dual-port RAM are provided to monitor critical variables in real time.

The unit supports up to four hardware events for triggering breakpoints or traces. There are, in addition, multiple software breakpoints. A 4k x 63-bit trace buffer permits direct viewing of source code. This trace buffer can also record full address, data bus, chip select, and control signal information.

The initial release of the Lite emulator supports Motorola's 68330/1/2/3 microcontrollers. Support for the 68040 and the HC16 family are planned. Offered with HMI's SourceGate debugger, the unit is priced at $4,995.

—Jeff Child

Lite emulator at a glance

- Supports 68330/1/2/3; support for 68040, HC16 planned
- Full tracing of show cycles, pipeline dequeuing, Port E support
- 256-kbyte overlay RAM
- Two kbytes of dual-port RAM
- 115.2-kbaud serial interface to host

Huntsville Microsystems
PO Box 12415
Huntsville, AL 35815
(205) 881-6005
Circle 354
Mixed-signal simulator features high speed, capacity and convergence

GenRad's Design Automation Group has just introduced Shado, a mixed-signal simulator that combines the digital capabilities of HSIM, from the company's System HILO 4 suite, with Eldo, an analog simulator from AnaCAD, a German company that recently opened an office in Fremont, CA. According to GenRad, the Eldo simulator provides an order of magnitude improvement in capacity, up to two orders of magnitude improvement in speed, and better convergence than other simulators.

The Eldo analog engine uses both second- and third-generation equation-solving methods. The second-generation algorithms are Spice-like, and use matrix manipulation and Newton-Raphson (NR) iteration techniques to solve the circuit's differential equations. Although these techniques provide solutions for all types of technology, they sometimes sacrifice performance. For circuit sections with loose couplings (such as MOS transistors), faster third-generation algorithms, such as one-step relaxation (OSR) methods, are used.

Balancing algorithms

A key feature of Eldo is that it can apply both NR and OSR techniques to a solution. The simulator uses a patented balancing technique to select the best equation-solving algorithm for a particular section of the analog circuit. Moreover, the NR and OSR algorithms are applied simultaneously to the whole circuit. This can be automatic, with no user intervention.

The aim of the balancing algorithm is to partition the circuit into blocks, each identified as appropriate to NR or OSR. This technique assigns the appropriate algorithms to targeted blocks. In the case of the NR algorithm, the technique manipulates several smaller matrices instead of one large matrix (as is the case with Spice algorithms).

For circuits with severe convergence problems, techniques such as simulated annealing are used. The circuit can also be repartitioned when non-convergence is detected until successful DC convergence is achieved. NR and OSR algorithms are then used for transient analysis, block by block.

The digital side of the simulator, HSIM, supports VHDL 1076, RTL logic and test synthesis. Libraries are common between the simulator and the synthesis tool, which makes for faster design iterations and more accurate synthesis.

Shado uses a lock-step algorithm for synchronization between the analog and digital simulation engines. This approach is different from some other mixed-signal solutions, such as the Calaveras algorithm from Analogy (Beaverton, OR), which lets one simulator run ahead of the other. GenRad defends its approach by pointing out that leapfrog algorithms such as Analogy's waste CPU time because they make a simulator backtrack in time. GenRad does admit, however, that leapfrog algorithms may have an advantage in simulations that are mostly digital.

Shado is available now on Sun SPARC stations and Hewlett-Packard 700 systems. Prices start at $30,000.

— Mike Donlin

Shado at a glance

- Mixed-signal simulator combines HSIM digital with Eldo analog simulation
- Uses second-generation Newton-Raphson algorithms and third-generation one-step relaxation techniques
- Has lock-step algorithm for efficient use of CPU time
40 MB/SEC DUAL-PORT VME/VSB MEMORY

The CI-VME40 is the ultimate high-speed, high-capacity DRAM memory board with a dual-port interface to the VME and VSB Busses. The CI-VME40 is optimized for Block Transfer Cycles yielding a bus transfer rate up to forty megabytes per second. Chrislin is the only memory supplier to offer such an advanced and versatile dual-ported VME/VSB memory!

THE CI-VME40 FEATURES:
- 20ns write/20ns read ACCESS TIMES in BLOCK CYCLE
- 90ns write/140ns read ACCESS TIMES in SINGLE CYCLE
- 63ns write/83ns read CYCLE TIMES in BLOCK CYCLE
- 195ns write/195ns read CYCLE TIMES in SINGLE CYCLE
- 4MB, 8MB, 16MB, 32MB, 64MB in one VMEbus/VSB slot

ALSO AVAILABLE FOR THE VMEBUS ARE...

THE CI-VME memory FEATURES:
- Low-cost high-power VME memory with 4, 8, or 16MB
- VME Revision C.1 compatibility
- Lower and upper memory addresses independently selectable in 64K byte increments
- Byte Parity Error Detection with selectable trap on Parity Error
- On-board Control Status Register

THE CI-VSB-EDC FEATURES:
- Low-cost high-power dual-ported VMEbus/VSB EDC (Error Detection and Correction) memory
- 4, 8, 16, 32 or 64MB in one VMEbus/VSB slot
- VME Revision C.1 compatibility, VSB Revision C
- Lower and upper memory addresses independently selectable on 256K byte boundaries
- Single-Bit Error Detect and Correct, Double-Bit Detect

Chrislin Industries, Inc.
31312 Via Colinas, Suite #108, Westlake Village, CA 91362
TEL: (818) 991-2254 FAX: (818) 991-3490

Providing Top Quality Memory for Over 16 years!

CALL TOLL FREE: (800) 468-0736 (PST)
CIRCLE NO. 64
Disk drive controllers automate SCSI and AT interfaces

Computer users want their disk drives big, fast and inexpensive. They usually get two out of those three characteristics. Two new controllers in Adaptec’s AIC8000 family, however, help drive manufacturers come closer to delivering all three.

Adaptec’s approach is to integrate data-flow automation into the disk controller, increasing I/O performance and freeing the microcontroller for servo and mechanical operations.

Even with these two new microcontrollers, disk manufacturers have run into limits of capacity and performance. Adaptec’s new chips, however, support disk NRZ (non-return-to-zero) rates of 40 Mbits/s for the AT bus and 40 to 48 Mbits/s for SCSI, plus host data transfers to 10 Mbytes/s, with bandwidth for error correction.

Adaptec calls its approach Automatic Data Flow Management (ADFM). In the SCSI interface, ADFM permits automatic management of single or multiple SCSI phases and automated handling of the SCSI control and data signals. In the AT interface, ADFM supports full AT command execution and automatic update of the AT Task File. ADFM provides for automated data flow between host and disk and automated full-track data access from disk for Adaptec’s AIC8110 and 8160 controllers.

Adaptec’s AIC8110 and 8160 disk drive controllers are similar chips with different host interfaces for AT and SCSI-2 buses. By automating the control functions for the host, drive and buffer interfaces, they unload the disk drive microcontroller and speed the flow of data. Their high degree of integration also lowers the cost of drive systems and speeds time-to-market.

Adaptec’s SCSI chip, the AIC8110, can handle 10-Mbyte/s synchronous SCSI-2 Fast transfers, or 5-Mbyte/s synchronous or asynchronous SCSI-1 transfers, in either single-ended or differential modes.

On the other side of the drive, the disk controller essentially takes over from the microcontroller after power-up initialization. It contains a 48-word disk format/read/write sequencer RAM.

Between the host and the disk, the buffer controller is the final element in the automated datapath, controlling data flow into and out of the buffer RAM while the host and disk ports are operating. It interfaces to the disk controller through a 16-byte FIFO and to the host interface manager through a 16-byte (SCSI) or 24-byte (AT) FIFO.

Error detection and correction (EDC) can use standard 32- and 56-bit computer-generated codes or an 88-bit non-interleaved Reed-Solomon code. The latter can correct a single-burst error of up to 14 bits.

The local microcontroller interface handles most 8-bit microcontrollers with either multiplexed or non-multiplexed address/data buses.

For portable applications, a power manager provides for idle, standby and sleep modes. Adaptec estimates a 30-percent power savings over a controller with no power management.

Both controllers are available in 100-pin thin and standard quad flat packs. In quantities of 10,000, the unit price of the AIC8110 is $18.95, and the AIC8160 is $15.95.

—Don Tuite
Thanks for the memories...

At this time, we wish to extend our good wishes for the season and a happy and healthy New Year, on a personal as well as a business level. You — our readers and advertisers — our friends helped make 1992 a spectacular and memorable year for all of us at Computer Design and Military & Aerospace Electronics. Thanks — and best wishes for a terrific, memorable and profitable 1993.
12-bit A-D converter outputs RS-232

A single A-D converter chip with two-wire, unbalanced RS-232 serial output can replace the customary chain of five or more chips used for remote data gathering in monitoring and control systems. Micro Linear's ML2223 contains a 13-bit (12-bit plus sign) analog-to-digital converter, sample-and-hold, voltage reference, UART, and baud rate generator. You can place the 16-pin DIP right at your sensor and eliminate analog noise problems.

The range of the differential input is -5 to +5 V, and the chip is self-calibrating. Maximum non-linearity over temperature is 0.018 percent. Conversion time, including sample-and-hold, is 45.6 µs maximum.

Although the RS-232C specification calls for shorter cable lengths, Micro Linear claims that it's practical to run signals as far as 200 ft from its chip. Long-range remote sensing can be accomplished using modems or LANs. The data rate isn't limited to the RS-232's 19.2-kbits/s maximum, but may go as high as 200 kbits/s.

Data is output in two 9-bit bytes (including parity). Each byte is framed by one start bit and two stop bits, so a burst of output data is 24 bits long. To help the system controller identify bytes, the least significant is sent with even parity, while the most significant is sent with odd parity.

Of the two data output modes, the current mode outputs data immediately after the analog-to-digital conversion is complete, but at the price of longer intervals between conversions. The previous data mode overlaps conversion and data output for a higher conversion rate, but introduces a longer delay between conversion and output.

To achieve 12-bit resolution on a small die, the chip's A-D circuits use an algorithmic approach to successive approximation conversion, rather than the more common technique that involves feedback from a DAC. For positive inputs, the input sample, multiplied by two, is compared to the voltage reference. If it's greater than the reference, the MSB is set to one, and the reference is subtracted from the 2x input voltage, with the remainder stored in the sample-and-hold. If it's less, the MSB is set to zero and the 2x input voltage itself is stored in the sample-and-hold. The process is repeated for successive bits, except that twice the value currently in the sample-and-hold is compared to the voltage reference each time. Negative inputs are handled similarly.

In quantities of 1,000, the unit price of the ML2223 is $14.50.

---Don Tuite

ML2223 at a glance

- Differential ±5-V input
- 12-bit (plus sign bit) resolution
- Serial RS-232 output, at up to 200 kbits/s
- 16-pin 300-mil DIP
- ±5-V supplies

Micro Linear
2092 Concours Dr
San Jose, CA 95131
(408) 433-5200
Circle 355

"FUZZY LOGIC" REPRINTS

Last year our March special report on Fuzzy Logic generated over 4,100 reader inquiries and the April 1992 Fuzzy Logic report is already poised to generate an even higher number of inquiries! Reprints of the April article are available now—quantities of 100 or less are $1.00 each, quantities over 100 are .75 each. To order, call Patti Kenney at (508) 392-2124.

CIRCLE NO. 14
Prototyping system emulates up to six million gates

For pre-silicon prototyping, the Enterprise Emulation System from Quickturn Systems (Mountain View, CA) is based on a multiplexed architecture that's separated into logic emulation modules and a reprogrammable backplane. You can plug up to eleven modules, each with the capacity to emulate 30,000 gates, into the Enterprise backplane. By using an Interconnect Module, moreover, you can cluster as many as 22 systems, for a total emulation capacity of six million gates.

The key to the Enterprise architecture is a full-custom, 168 x 168 crossbar switch, dubbed the Multiplexed Interconnect Chip (MIC), that Quickturn developed for both the Enterprise logic emulation modules and its reprogrammable backplane. Each module has 42 Xilinx 3090 FPGAs to accommodate logic and 42 MICs to implement interconnects. By alleviating the need to use FPGAs for interconnect purposes, Quickturn has made it possible to pack the FPGAs much more densely with logic. Each of the Enterprise's 3090s can accommodate up to three times as many gates as identical parts in earlier Quickturn hardware emulators.

Separating logic from interconnect also shortens routing delays, resulting in typical emulation speeds of from 4 to 8 MHz, and simplifies the process of mapping your design into the emulation system. In addition, putting interconnects into MICs rather than into more costly FPGAs lowers overall system cost. On a per-gate basis for a fully configured system, Enterprise costs 25 percent less than Quickturn's previous hardware emulator.

Automatic partitioning
In the past, Quickturn users have had to manually partition very large designs into manageable logic blocks, but Enterprise users can now assign that difficult task to the Automatic Design Partitioner. This software partitions logic into netlists fitting within a single emulation system and also automates the clustering of multiple Enterprise systems.

Also new with Enterprise are Memory Emulation Modules that automatically map memory elements from a netlist to the emulation system. These programmable plug-in boards eliminate the need to rely on emulation board resources. You can model multiport RAMs with up to 32 ports and single-port RAMs of up to 2 Mbytes on a single board. Precision Emulation Software, embedded in Enterprise, automatically maps synchronous and asynchronous designs into the emulation system. For debug, the software has a timing analysis tool that supports asynchronous designs. Quickturn claims that its Timing Sensitive Partitioning and Precision Prototype Synthesis algorithms guarantee a violation-free configuration.

For future expansion, Quickturn has reserved interconnect capacity on the Enterprise's backplane to ensure the opportunity to introduce increased-gate-count logic emulation modules when higher-capacity FPGAs replace the 3090s.

The Enterprise Emulation System, available now, is priced at $388,000 for a 120,000-gate system and $798,000 for a 330,000-gate system.

—Barbara Tuck

Enterprise at a glance

- Logic separated from interconnects
- Shorter delays, simplified mapping
- Emulation speeds from 4 to 8 MHz
- Automated design partitioning
- Plug-in boards for emulating memories

Quickturn Systems
325 E Middlefield Rd
Mountain View, CA 94043
(415) 967-3300
Circle 351

Trademark Information

UNIX is a registered trademark of AT&T Bell Laboratories.

PAL is a registered trademark of Advanced Micro Devices, Inc.

SMART-POWER is a registered trademark of Nartron Corp.

CDA and BurstRAM are trademarks of Motorola, Inc.

SCOPE and ASSET are trademarks of Texas Instruments, Inc.

IRIS POWERVISION is a trademark of Silicon Graphics, Inc.

RealTimeX is a trademark of Concurrent Computer Corp.

Zone Bit Recording is a registered trademark of Seagate Technology, Inc.
Are automobiles the proving ground for the next generation of electronics?

Art Fury, the charismatic vice-president of Semitech (Newbury Park, CA), tells a story about convincing automakers to make better use of semiconductors. As an applications engineer for General Electric in the 1960s, he got a design win for power switches by equipping an old car with three-step sequential directionals and driving it to Detroit. His ideas were incorporated into the early versions of the Mercury Cougar, but he reports that until Ford engineers could see the technology in action, they were extremely reluctant to incorporate the electronics into their cars.

Changing situation
Although it tends to shy away from publicity, the automotive industry has become one of the most powerful drivers of mixed-signal technology—for CAE tools as well as smart-power devices. Jean-Philippe Dauvin, the keynote speaker at last month’s Computer Design/Miller Freeman Analog and Mixed-Signal Design Conference, highlighted the importance of the automotive sector. Dauvin, the market research manager for SGS-Thomson Microelectronics (Paris) and president of WSTS Europe (the independent reporting agency for semiconductor industry statistics), said that over the next five years, automotive electronics will grow faster than any industry segment, including computers, consumer electronics and telecommunications. Auto industry electronic devices account for the smallest percentage of the $710 billion in electronic systems manufactured in 1991—4.3 percent compared to 14.2 percent each for military and consumer electronics and 37.5 percent for computer systems. By 1997, automotive electronics will be 6.1 percent of a $1.065 trillion market, while the proportions of consumer and military electronic systems will decrease. Automotive electronics, said Dauvin, will grow at an 11-percent compound annual growth rate (CAGR) between 1991 and 1997, while computers, with the next largest growth rate, will only grow at an 8-percent CAGR.

Automotive customers now consume only 6 percent of the $54.6 billion in semiconductors sold worldwide, but, once again, this area will give the industry its highest growth rate (14 percent) between 1992 and 1997. By then, automotive semiconductors will be 7 percent of a $92.7 billion market. Of particular IC types, semicustom devices will show the highest CAGR (15 percent) during that period.

Use of electronics expanding
Part of the reason for this growth is that the auto industry is beginning to see the potential of electronics. Whereas the industry once considered electronic controls suitable only for passenger compartment climate control or audio consoles, it now sees semiconductors as vital for automobile braking systems, air bag deployment and engine controls. Some of this has been in response to regulatory pressures. Delco Electronics (Kokomo, IN), the automotive systems arm of General Motors, freely admits that it adopted the Motorola 68332 for engine controls in response to the severe emission standards set by the California Air Resources Board (CARB). But if one looks closely, it’s clear that the responses of Delco and General Motors have been significantly above and beyond the need established by CARB. Automotive engineers, for instance, are among the best consumers and enhancers of mixed-signal modeling tools.

There’s also a vision of the future driving automakers such as Germany’s Daimler-Benz AG, manufacturer of the Mercedes Benz. In the future, for example, satellite warning and navigation systems will guide drivers and regulate traffic patterns, according to Daimler’s chairman, Edzard Reuter, in comments he made about his company’s acquisition of AEG Electronics (Frankfurt, Germany) in 1989. Electronic components, currently representing about 5 percent of the value of a Mercedes-Benz, will rise to 25 percent by the year 2000. (The electronics content of automobiles will be much higher, in fact, if automakers are successful in perfecting a low-cost quick-
10 FUNCTION
μP SUPERVISOR
HAS 6ns CHIP ENABLE

Automatic Backup-Battery Switching With Low-Battery Monitor

Supervising memory and power supplies in complex μP-based systems requires both time and real estate. Avoid complicated multi-chip solutions, use Maxim’s new MAX791 – the Ultimate μP Supervisor. The new MAX791 features the fastest CE gate delay available, allowing you to protect the data integrity of the fastest SRAMs without degrading memory access times.

♦ 10 Functions in One IC:
  - Power OK – 200ms Delay
  - Backup-Battery Switching
  - Precision Voltage Monitor
  - No External Timing Capacitor
  - 6ns Chip-Enable Gate Delay
  - 2-Stage Power-Fail Warning
  - Backup-Battery Monitor
  - Memory Write Cycle Completion
  - Separate Watchdog and Reset Outputs
  - Manual-Reset Input

♦ 60μA Operating Supply Current
♦ 1μA Backup Supply Current
♦ Space-Saving 16-Pin Narrow SOIC

FREE μP Supervisory Design Guide – Sent Within 24 Hrs!
Includes: Data Sheets and Cards for Free Samples

CALL TOLL FREE 1-800-998-8800
For a Design Guide or Free Sample

MasterCard® and Visa® are accepted for Evaluation Kits or small quantity orders.

Maxim Integrated Products, 120 San Gabriel, Sunnyvale, CA 94086, (408) 737-7600, FAX (408) 737-7194.

Distributed by Arrow, Bell-Graham, Elmo, Hall-Mark, Nu Horizons, and Pioneer. Authorized Maxim Representatives: AL, M2i Montgomery Marketing, Inc. AZ, Techni-Source Inc.; CA, Mesa Pro Associates, Inc.; Centaur Corporation; CO, Component Sales; CT, NRG Limited; DE, TAI Corporation; FL, Sales Engineering Concepts; GA, M2i Montgomery Marketing, Inc.; ID, E.S./Chase; IL, Heartland Technical Marketing Inc.; IN, Technology Marketing Group; IA, JR Sales Engineering, Inc.; KS, Delltron; LA, BP Sales; MD, Micro-Comp, Inc.; MA, Comp Rep Associates; MN, Mcl Foster Technical Sales, Inc.; MS, M2i Montgomery Marketing, Inc.; MO, Delltron; MT, E.S. Chase; NE, Delltron; NV (Renno, Tahoe area only) Pro Associates, Inc.; NJ, Emtec Sales, Inc.; TAI Corporation; NM, Techni Source Inc.; NY, Parallax, Relazioni; NC, M2i Montgomery Marketing, Inc.; OH, Lyons Corporation; OK, BP Sales; OR, E.S. Chase; PA (Pittsburgh area) Lyons Corporation; (Philadelphia area) TAI Corporation; SC, M2i Montgomery Marketing, Inc.; TN, M2i Montgomery Marketing, Inc.; TX, BP Sales; UT, Utah Component Sales, Inc.; VA, Micro-Comp, Inc.; WA, E.S. Chase.

Distributed in Canada by Arrow and Future. Authorized Maxim Representative in Canada: Tech Trek.

Maxim is a registered trademark of Maxim Integrated Products. © 1992 Maxim Integrated Products.
While driven by automotive concerns, Daimler's push into electronics has repercussions for other consumers of mixed-signal technology. Under the Daimler umbrella, AEG and Deutsche Aerospace (Munich, Germany) have formed four microelectronics groups—semiconductors, microsystems, automotive systems, and special technologies. Companies in the semiconductor group include not only Telefunken (Heilbronn, Germany) and Eurosil (Munich, Germany), but also Britain's Dialog Semiconductor (Swindon, England), Matra Micro (Nantes, France), and American-based Siliconix (Santa Clara, CA). Mixed-signal products of the group include smart-power ICs, power transistors and discretes, ASICs and application-specific standard products, as well as microprocessors and microcontrollers.

Matra, in fact, was one of the first companies to introduce a 3-V microcontroller chip, according to Irving Gold, the U.S. marketing manager for the company, which now shares facilities with Siliconix. Based on the popular 80C51 architecture, a favorite for automobile consoles, the new controllers were announced in August and will function from a positive rail that can vary from 2.7 to 5.5 V. Siliconix, which made Art Fury famous in the early 1980s as an evangelist for smart-power technology, was among the first companies to successfully package DMOS power-driver transistors in reduced footprint SO packages—a technology the company calls “little foot.” Matra’s sister company, Siliconix, is now 80-percent owned by AEG. The semiconductor group expects to benefit from Daimler expertise in engine control anti-skid braking systems and display technologies, as well as developments in microwave technology and high-energy batteries.

**Sensors and actuators**

Current-generation auto system controllers rely on two mixed-signal systems—front-end signal conditioners and back-end amplifiers—which correspond roughly to sensors and actuators. On the front end, a sensor converts engine temperature or brake pressure into a voltage, amplifies it and converts it into a digital number. A microprocessor typically compares this measurement with a reference voltage in ROM-based look-up and issues a corrective response. In some cases, a D-A converter transforms the digital number into a voltage; in others, the digital output of the microcontroller can be used directly to open or close a big mechanical switch—power door locks, for example. In either case, a power transistor must be harnessed to raise the current level high enough to magnetize the coil that turns the motor, activates the relay or squeezes the brake pads. While sensor signal conditioning, with typically low-frequency requirements, is relatively mature, much development work needs to be done in reducing the size and packaging weight of power transistors, and in obtaining tighter integration with control logic, the essence of smart-power technology.

One example of smart-power technology developed for automotive electronics users is Prism, recently introduced by Texas Instruments (Dallas, TX). The Prism technology is composed of a standard-cell ASIC that permits the integration of VLSI logic elements such as microprocessors and memories with linear and power devices. The two keys to Prism are reusable engineering—based on a multipurpose standard-cell library—and a process technology that combines 1-µm CMOS, analog and high-voltage CMOS, and bipolar and power DMOS transistors all on one chip. The technology is said to produce smart-power chips smaller than those coming from the updrain DMOS process of Motorola Semiconductor (Phoenix, AZ) or the BCD-2 process of SGS-Thomson Microelectronics (Phoenix, AZ and Agrate Brianza, Italy). It was developed to impress the automotive system designers at Delco.

More than 100 engineers were involved in the Prism project, according to Delbert Whitaker, TI's vice-president in charge of product development. Prism includes six or more mixed-signal and linear cell libraries. The key to its success, however, is a lateral DMOS transistor structure that drastically reduces the real estate required by DMOS power transistors. One advantage of smaller chip real estate is the ability to replace cumbersome SIP and TO-220 power packages with smaller, less expensive and more manufacturable DIP and SO packaging. Apart from actuators developed for Delco, the first standard TI products to use the technology will be power transistor arrays, data bus latches and transceivers.

### Driving CAE tool development

In addition to device technology, automotive equipment makers will be instrumental in the development of analog and mixed-signal CAE tools. They are already among the best customers for Analogy’s behavioral modeling tools. A consortium of European auto equipment manufacturers, in fact, is attempting to develop a framework for hardware development and simulation tools. Fueled by engineers at Daimler-Benz and the Bavarian Motor Works (BMW), the consortium’s focus is simulating the operation of new systems, even while they’re in the conceptual phase. The goal is to test out control system concepts and compare alternatives before the detailed design work is begun.

Key to the success of this initiative is the availability of abstract system-level models, especially those that depict mechanical and electromechanical devices, such as relays, motors, actuators, and switches. These are also among the key concerns of the groups actively tracking the development of an analog hardware description language (AHDL). Gauging by attendance at the Analog and Mixed-Signal Design Conference last month, automotive system builders will be among the first users of an AHDL.

Stephan Ohr is president of Indian Forest Research and editor of the monthly newsletter, Mixed Signals.
8051 IN-CIRCUIT EMULATOR

$995.00

- 8031/32/51/52 support
- 64K Memory/64K breakpoints
- Source Level C and Assy debugging
- Trace Buffer
- Programmers
- Money Back Guarantee

VAIL SILICON TOOLS
305 570 5580
CIRCLE NO. 166

QUICK-TURN PC BOARDS
INSTANT QUOTES
1-800-234-1556
(Flush Hours (602) 377-7319)
Single/Double Sided/Multi-Layer
Gerber Input/ Floppy or Modem
MIL Approved U.L. Listed
AVANTI CIRCUITS, INC.
17650 North 25th Avenue
Phoenix, Arizona 85023
(602) 863-7729 & 234-1556
1-800-234-1556
BBS (602) 234-1737
CIRCLE NO. 169

8051/68HC11/Z80
Integrated Debugging System
Software & Hardware
$2495 Includes:
- Borland Turbo C Like interface
- Multi-windowed editor
- Symbolic source or assembly debugging with 16 breakpoints
- CPU register, PSW, SFR memory, watch, output displays
- Target Interface Unit (TTU) connects PC to target PROM socket
- One TU supports all µPs
- Control program execution with Run, Step, Stop to Cursor. Reset, Step to Trace
- 128K ROM emulator built-in
- 8051, 68HC11 or Z80 target board included
- Supports many compilers

CIRCLE NO. 171

System Showcase
COMPUTER DESIGN NOVEMBER 1992 123
New Tools ...... to Support Your New Designs!

For over 17 years, Elan Systems has been designing device programmers that enhance the application of the latest in IC technology. The task today is even greater, - but Elan continues to meet the challenge by providing you with 3 new models to match your specific design requirements:

**Model 6000**
The ultimate in Pin-Driver Programmers. Total device support today ... and tomorrow!

Elan Systems, Inc.
365-700 Woodview Ave.
Morgan Hill, CA 95037
Tel (408) 778-7267 FAX (408) 778-2597

**Model 5000 Turbo**
Stand-alone, universal programmer with today’s fastest approved programming times - 2700 < 30 secs

**Model 5-J08**
PCMCIA card Programmers for development or production. Reader/Writer also available.

CALL (800) 541-ELAN for a FREE Cross-Reference Wall Chart.

See us at WESCON - Booth #2749

---

**Half size ECL Clock Oscillator**

Connor-Winfield Corp. introduces its new 8-pin DIP ECL clock oscillators. The E500 Series is available in frequencies from 24 MHz - 180 MHz. Options available include industrial temp range of -40C to +85C, complimentary output, enable/disable function, and surface mount header. Frequency stabilities are available to +/-25 ppm over temperature.

These models are available with supply voltage of either 5.2 V dc (10K equivalent) or 4.5 Vdc (100K equivalent) or +5Vdc. Prototype quantity pricing at 120 MHz is $43.90 each. Delivery is stock to 7 weeks A.R.O. Contact Barney Hill at: Connor-Winfield Corporation 1865 Selmarion Road, Aurora, IL 60505 PH: (708) 851-4722 FAX: (708) 851-5040

---

**State Machine Design**

For Complex & High Density PLDs

The most powerful PLD/FPGA CAE design software from $495.00

**CUPL™ 4.2**

1-800-331-7766

LOGICAL DEVICES, INC.

See us at Wesccon Booth 3526 Hall A

---

**CapFast Schematic Capture and Interface Tools**

Price Starts at $595.00

Available on both DOS, Windows and UNIX (SPARC, DEC, HP, IBM)

CapFast is an advanced hierarchical schematic design and interface tool for PCB, PLD/FPGA, as well as ASIC designs.

The optional EDIF 200 tools allow the designer to translate CapFast schematics to and from other EDA systems, such as Mentor Graphics and Cadence. For further information, please call (503) 645-0313.

---

**WHY??**

**BURN EPROMS?**

when

Quality, FAST-LOADING

EPROM EMULATORS

start at ONLY

$129

**SYSTEM SHOWCASE**

Reach over 100,000 qualified engineers and engineering managers with SYSTEM SHOWCASE advertising.

Rates start at $940

For more information call Sue Shorrock at 800-225-0556 or 508-392-2185
S Y S T E M S H O W C A S E

OEM AIR PUMPS/COMPRESSORS
• Only one moving part • Oilless
• Low power • Low vibration
• AC & DC models

Call us to discuss your application
TEL: 708-860-0500
FAX: 708-860-9473
MEDICAL-SURGICAL • LEAK TESTING
BUSINESS MACHINES
AERATION SOURCES
VENDING MACHINES
ENVIRONMENTAL
GRAPHIC ARTS
Send for FREE catalog

M E D O USA, I N C.
700 S. Central Ave
Wood Dale, IL 60191

CIRCLE NO. 184

Emcor Introduces Product Guide for Electronic Enclosures

"A Guide to Emcor Enclosures" describes design, construction, and component features of all the Emcor enclosure systems—ESQ, 10 Series, Emcor L, EMRF shielded cabinets—plus CompuDesk, enclosure cooling accessories, Instant Emcor ship-from-stock program, and Emcor's modification and custom design capabilities. Free catalog available.

Emcor Products
1600 W. 4th Avenue NW
Rochester, MN 55901
507-289-3371, FAX 507-287-3405

CIRCLE NO. 185

SCSI-2
Low-cost, PC-Based Testers

For all SCSI Devices
With solutions for every testing situation...
Design, manufacturing, field service
Transfer data at 10 MB/second. They feature:
• SCSI-2 Command Queuing
• SCSI-2 Message System Support
• High-level Multi-threading Support
• Initiator and Target Emulation

We offer complete development systems, low-cost manufacturing platforms and portable turn-key systems, all available with integrated bus analysis.

For information or prompt quotation, call, write or FAX us:

6975 Washington Ave. So., Suite 220 • Edina, MN 55439
612/941-5505 • FAX 612/941-2386

CIRCLE NO. 186

FIN ALL
One tool to satisfy all your firmware development needs

PROMICE is a universal system.
 • Develops code for any microprocessor
 • Complete, real-time, source level debugging
 • Host software for DOS, Unix, Mac, VMS
 • Non intrusive on your target system
 • Simply plugs into any ROM socket

PROMICE also supports Turbo Debugger, C thru ROM, FreeForm, GDB, and more.

PROMICE...the affordable solution.

Grammar Systems
TEL: (614) 899-7878
West: (614)752-0219
FAX: (614) 899-7888

CIRCLE NO. 187

Multibus II Parallel System Bus Analyzer

PSBA-100 A productivity enhancement tool for the system integrator, field service engineer, software, and hardware engineer.

• Stand-alone, single board computer
• 64 bit format, installs in a single slot
• Built-in, terminal-based user interface
• Supports all four address spaces
• Data capture based on Multibus II protocol
• Fully programmable filter logic uses templates based on Multibus II protocol
• Filter logic supports 16 trigger levels

Multibus II is a trademark of Intel Corp.

PRC
PPC Inc.
1410 West Street
Bellevue, NE 68005
(402) 203-3900

CIRCLE NO. 188

HIGH PERFORMANCE GRAPHICS CARDS

• 32/40 MHz TMS34020 GSP
• Optional FPP w/512K local SRAM
• For ISA Bus & STD 32® systems
• 1 MB DRAM, 1 MB VRAM standard
• On board memory expandable to:
  • 4 MB DRAM
  • 4 MB VRAM
  • 512K EPROM
• 640x480 thru 1600x1200 pixels
• 24-bit True Color mode
• 256 colors from 16.7 million
• Free TIGA® & Windows® drivers

$1,495 up

ZWICK SYSTEMS INC.
Tel 613-726-1377, Fax 613-726-1902

CIRCLE NO. 191

Conner-Winfield Corporation
1865 Selmaart Road
Aurora, IL 60505
PH: (708) 851-4722 FAX: (708) 851-5400

CIRCLE NO. 189

386/486
Bolt-in Computers for embedded applications

High performance CPUs for aggressive applications. From full blown VGA flat panel, 8MB RAM, 512 MB IDE systems. To number crunching high throughput ROM-based systems.

• 16/25 MHz 386SX/486SLC
• 8MB RAM, 16 MB ROM
• Solid state or IDE disk for DOS 5.0, Windows 3.1
• Multi-tasking, multichip, comm./P/D control
• multi-CPU software
• Optional STD BUS expansion

From $995

CIRCLE NO. 192
POSITION WANTED ADS

Free 1" ad to subscribers seeking full-time employment. Just include 50 words of copy and your subscription label. We'll run your ad in 2 consecutive issues. Available to non-subscribers or consultants/companies at $125 per column inch. Mail your position wanted ad to: COMPUTER DESIGN Positions Wanted, One Technology Park Drive, PO Box 990, Westford, MA 01886

SEASONED PR/ADVERTISING/MARCOM MANAGER, 26 years experience with many awards, seeks sr. level corporate or agency position. Heavy magazine PR experience, plus advertising, collateral, trade shows, videos, newsletter. Former radio/TV reporter. Experienced at planning, managing, executing. Exceptionally good at developing and managing individual contributors. Live Northeast, will relocate. Call Jeff, (508) 746-7898.


PROJECT MANAGER: Highly versatile professional with over 15 years of broad-based experience in Project Management, Economic Analysis and Engineering gained with blue chip firms (GTE, PacBell, FHP, etc.). Technically oriented, MBA, BS, and BA degrees with strong functional skills embracing all areas of research, applications engineering and business analysis. Call Bob Mazzola, (714) 841-8878.

Product Development: Hardware, Firmware, Software. Developed and owns complete rights to market-ready Data Acquisition/Voice/Phone/Instrumentation products. Experience in Embedded Controlers, Assembly language, PC interface and programming. Schematics Design, PCB layout, prototype development, troubleshooting, Brochure, advertising and manual write-up. Excellent communications skills. Contact Nidal at (719) 260-6834.

TECHNICAL WRITER. Eight years publications experience. Documentation and promotions including copy and scripting. Knowledge of popular PC packages. Clients include CAD, robotics, software developers, design. Offer free diagnosis of your publications needs. Samples. Call Jay at (617) 523-4217.


POSITIONS WANTED

ENGINEERING/APPLICATION/CUSTOMER ENGINEERING. BSEE with 20 years of hands-on management of design from concept to delivery. Customer/vendor contact, Analog/Digital/Package & use of CAD, Peripheral/Small system exp. Kayvon Kiamanesh, 21811 Saticoy St #21, Canoga Park, CA 91304.

Q.A. Manager seeks position with a company desiring to improve its performance, i.e., quality & productivity. I have excellent related experience that includes quality program audits, proposals, plans, procedures, TQM, SPC, SQA, QE, MRB, Config. Mgt, and ISO programs for aircraft & aerospace products & services. Please call (818) 365-2200 if no answer please leave message.

PROJECT MANAGER: Highly versatile professional with over 15 years of broad-based experience in Project Management, Economic Analysis and Engineering gained with blue chip firms (GTE, PacBell, FHP, etc.). Technically oriented, MBA, BS, and BA degrees with strong functional skills embracing all areas of research, applications engineering and business analysis. Call Bob Mazzola, (714) 841-8878.


QUALITY ASSURANCE, SOFTWARE engineering. BSEE, 11 years experience in the design and development of large scale data acquisition and control systems. Managed and performed real-time software & hardware systems design in instrumentation, control, data acquisition, signal conditioning, transducers etc. Mooror, 1000 Mira Vista Dr, Huntsville, AL 35802 (205) 881-8444.
## ADVERTISERS INDEX

Computer Design's
INSTANT DATA ACCESS
ADVERTISERS

To receive data sheets instantly from these advertisers via FAX, dial (617) 494-8338 and when prompted, enter the 4 digit document number shown here.

<table>
<thead>
<tr>
<th>ADVERTISER</th>
<th>PAGE</th>
<th>CIRCLE</th>
<th>**IDA</th>
<th>NO.</th>
<th>NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advanced Micro Devices</td>
<td>20-21</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Alacron</td>
<td>58</td>
<td></td>
<td>36</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog Devices</td>
<td>23-25</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AP Labs</td>
<td>22</td>
<td></td>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Applied Microsystems</td>
<td>112A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AT&amp;T Microelectronics</td>
<td>96-97</td>
<td></td>
<td>54</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ATML Corporation</td>
<td>15</td>
<td></td>
<td>9</td>
<td>1050</td>
<td></td>
</tr>
<tr>
<td>Augat, Inc.</td>
<td>57</td>
<td></td>
<td>37</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Avanti Circuits, Inc.</td>
<td>124</td>
<td></td>
<td>159</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Avotec Systems, Inc.</td>
<td>22</td>
<td></td>
<td>13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>W.H. Brady</td>
<td>28</td>
<td></td>
<td>19</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Brooktree Corporation</td>
<td>55</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>69</td>
<td></td>
<td>1026</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BUSCON '93 West</td>
<td>95</td>
<td></td>
<td>53</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cactus Logic</td>
<td>123</td>
<td></td>
<td>172</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cable and Computer Technology</td>
<td>87</td>
<td></td>
<td>52</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Christin Industries, Inc.</td>
<td>115</td>
<td></td>
<td>64</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Compass Design</td>
<td>67</td>
<td></td>
<td>43</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Computer Design</td>
<td>106</td>
<td></td>
<td>61</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Computer Design</td>
<td>117</td>
<td></td>
<td>65</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Computer Design</td>
<td>110</td>
<td></td>
<td>14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Computer Design</td>
<td>128</td>
<td></td>
<td>74</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conner-Winfield Corp.</td>
<td>124</td>
<td></td>
<td>178</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conner-Winfield Corp.</td>
<td>125</td>
<td></td>
<td>189</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CSR</td>
<td>42</td>
<td></td>
<td>28</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cypress Semiconductor</td>
<td>CV4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t ConferenceProceedings96-97</td>
<td>55</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Diversified Technology</td>
<td>40-41</td>
<td></td>
<td>27</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dynatem, Inc.</td>
<td>CV3</td>
<td></td>
<td>75</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>Elen Systems, Inc.</td>
<td>124</td>
<td></td>
<td>176</td>
<td></td>
</tr>
<tr>
<td>Electronic Solutions</td>
<td>1</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Embedded Computer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conference</td>
<td>62-63</td>
<td></td>
<td>41</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Error Products/Crieno</td>
<td>125</td>
<td></td>
<td>185</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Force Computers</td>
<td>8-9</td>
<td></td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>G</td>
<td>Gates Energy Products</td>
<td>16</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Globe Manufacturing</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sales Inc.</td>
<td>82</td>
<td></td>
<td>49</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grammar Engine, Inc.</td>
<td>125</td>
<td></td>
<td>187</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>HM Systems</td>
<td>52-53</td>
<td></td>
<td>35</td>
<td></td>
</tr>
<tr>
<td>Heurikon Corporation</td>
<td>101</td>
<td></td>
<td>57</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Heurikon Corporation</td>
<td>103</td>
<td></td>
<td>58</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Heurikon Corporation</td>
<td>105</td>
<td></td>
<td>60</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Huntsville Microsystem</td>
<td></td>
<td></td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I</td>
<td>I-TECH Corp.</td>
<td>125</td>
<td></td>
<td>186</td>
<td></td>
</tr>
<tr>
<td>Innovative Integration</td>
<td>123</td>
<td></td>
<td>173</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IBM Corporation</td>
<td>64</td>
<td></td>
<td>42</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Imagine That</td>
<td>123</td>
<td></td>
<td>171</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Integrated Device Technology</td>
<td>11</td>
<td></td>
<td>7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Integrated Systems</td>
<td>79</td>
<td></td>
<td>48</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Intel Corporation</td>
<td>127</td>
<td></td>
<td>72</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Intel Corporation</td>
<td>35</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Intergen</td>
<td>46</td>
<td></td>
<td>31</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Intersational Computer Conference</td>
<td>104</td>
<td></td>
<td>59</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### ADVERTISER INDEX

<table>
<thead>
<tr>
<th>ADVERTISER</th>
<th>PAGE</th>
<th>CIRCLE</th>
<th>**IDA</th>
<th>NO.</th>
<th>NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ironics, Inc.</td>
<td>83</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Itelabs</td>
<td>84</td>
<td></td>
<td>51</td>
<td></td>
<td></td>
</tr>
<tr>
<td>KADAK</td>
<td>110</td>
<td></td>
<td>62</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logical Devices, Inc.</td>
<td>124</td>
<td></td>
<td>180</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M</td>
<td>Macroink, Inc.</td>
<td>74</td>
<td></td>
<td>46</td>
<td>1037</td>
</tr>
<tr>
<td>Maxim Integrated Products</td>
<td>121</td>
<td></td>
<td>70</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEDO USA</td>
<td>125</td>
<td></td>
<td>184</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mercury Computer Systems</td>
<td>13</td>
<td></td>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Micro Industries</td>
<td>30-31</td>
<td></td>
<td>22</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Micro-Sys</td>
<td>125</td>
<td></td>
<td>192</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Micron Semiconductor</td>
<td>51</td>
<td></td>
<td>34</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Microwave Systems Inc.</td>
<td>39</td>
<td></td>
<td>26</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mitsubishi Electronics/EDG</td>
<td>48-49</td>
<td></td>
<td>33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mitsubishi Electronics</td>
<td>EDG</td>
<td>56</td>
<td>66</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Motorola TSD Group</td>
<td>33</td>
<td></td>
<td>23</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Needham's Electronics</td>
<td>124</td>
<td></td>
<td>179</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nohau Corporation</td>
<td>123</td>
<td></td>
<td>167</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nohau Corporation</td>
<td>123</td>
<td></td>
<td>168</td>
<td></td>
<td></td>
</tr>
<tr>
<td>O</td>
<td>Qsys, Inc.</td>
<td>47</td>
<td></td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>Omnibyte Corporation</td>
<td>80A</td>
<td></td>
<td>119,120</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OrCAD Systems</td>
<td>123</td>
<td></td>
<td>170</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Phase Three Logic</td>
<td>124</td>
<td></td>
<td>181</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pinnacle Data Systems</td>
<td>28</td>
<td></td>
<td>76</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PRC, Inc.</td>
<td>125</td>
<td></td>
<td>188</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quantum Software Systems</td>
<td>45</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R</td>
<td>Radstone Technology Corp.</td>
<td>37</td>
<td></td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>Ready Systems</td>
<td>61</td>
<td></td>
<td>40</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RISC '93 Overview</td>
<td>98-99</td>
<td></td>
<td>56</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Robotrol Corporation</td>
<td>125</td>
<td></td>
<td>190</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RTM, Inc.</td>
<td>26</td>
<td></td>
<td>17</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S</td>
<td>Sophia Systems &amp; Technology</td>
<td>73</td>
<td></td>
<td>45</td>
<td></td>
</tr>
<tr>
<td>Synergy Microsystems</td>
<td>2</td>
<td></td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Synergy Microsystems</td>
<td>CV2</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T</td>
<td>Tadpole Technology</td>
<td>43</td>
<td></td>
<td>29</td>
<td></td>
</tr>
<tr>
<td>Technical Solutions</td>
<td>124</td>
<td></td>
<td>182</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Teknor Microsystems, Inc.</td>
<td>27</td>
<td></td>
<td>18</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tektronix, Inc.</td>
<td>6-7</td>
<td></td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thersis Computer</td>
<td>29</td>
<td></td>
<td>21</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Toronto MicroElectronics</td>
<td>26</td>
<td></td>
<td>16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V</td>
<td>Venturicom</td>
<td>111</td>
<td></td>
<td>63</td>
<td></td>
</tr>
<tr>
<td>Vigra, Inc.</td>
<td>60</td>
<td></td>
<td>39</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vida Controls</td>
<td>77</td>
<td></td>
<td>47</td>
<td>1052</td>
<td></td>
</tr>
<tr>
<td>VME Microsystems Inc.</td>
<td>71</td>
<td></td>
<td>44</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VMetro, Inc.</td>
<td>51</td>
<td></td>
<td>24</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vail Silicon Tools, Inc.</td>
<td>123</td>
<td></td>
<td>166</td>
<td></td>
<td></td>
</tr>
<tr>
<td>W</td>
<td>Brian R. White Company</td>
<td>28</td>
<td></td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>Z</td>
<td>Z-World Engineering</td>
<td>123</td>
<td></td>
<td>174</td>
<td></td>
</tr>
<tr>
<td>Zwick Systems, Inc.</td>
<td>125</td>
<td></td>
<td>191</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Domestic only
t International only
** These advertisers have made arrangements to provide you with instant product data via Computer Design's Instant Data Access (IDA) System.

The Advertisers Index is published as a service. The publisher does not assume liability for errors or omissions.

When your product advertising demands that you reach the key decision makers in the microprocessor based electronics OEM, COMPUTER DESIGN delivers!

Only COMPUTER DESIGN:

• serves today's $570 billion microprocessor based electronics OEM
• provides design directions, options and choices-with exclusive "why-to" editorial
• delivers over 100,000 engineering managers and engineers-100% design and development qualified!
• reaches over 71,000 design and development engineering managers-more than any other design publication in the market
• is the fastest growing publication in the field

For more information on how to subscribe or advertise, please contact: Tim Toback, National Sales Manager/Associate Publisher at (508)392-2116.
When your product advertising demands that you reach the key decision makers in the microprocessor based electronics OEM, COMPUTER DESIGN delivers!

Only COMPUTER DESIGN:

• serves today’s $570 billion microprocessor based electronics OEM

• provides design directions, options and choices with exclusive "why-to" editorial

• delivers over 100,000 engineering managers and engineers-100% design and development qualified!

• reaches over 71,000 design and development engineering managers more than any other design publication in the market

• is the fastest growing publication in the field

For more information on how to subscribe or advertise, please contact: Tim Tobeck, National Sales Manager/Associate Publisher at (508)392-2116.

COMPUTER DESIGN (ISSN-0010-4566) is published monthly by PennWell Publishing Company, 1421 S Sheridan, Tulsa, OK 74112. Second-class postage paid at Tulsa, OK 74112 and additional mailing offices. Editorial offices are located at One Technology Park Dr, PO Box 990, Westford, MA 01886. Subscription Prices: Free to design and development qualified engineers and engineering managers in the U.S. and Canada. Paid to all others. Qualified engineers and engineering managers outside the U.S. and Canada - air shipped - $85 one year. For non-qualified recipients in the U.S. - $88 one year; in all other countries - air shipped - $154 one year. Call (918) 832-9263 for subscription information. Microfilm copies of COMPUTER DESIGN may be purchased from University Microfilms, a Xerox Company, 300 N Zeeb Rd, Ann Arbor, MI 48106. POSTMASTER: Send change of address form to COMPUTER DESIGN, Circulation Department, PO Box 3466, Tulsa, OK 74101. ©1992 COMPUTER DESIGN by PennWell Publishing Company. All rights reserved. No material may be reprinted without permission from the publisher. Officers of PennWell Publishing Company: Frank T. Laulinger, Chairman and Chief Executive; Joseph A. Walking, President and Chief Executive Officer; John Ford, Senior Vice-President; Carl J. Lawrence, Senior Vice-President; V. John Maney, Vice-President/Finance; W. Steve Zimmerman, Vice-President/Corporate Services.
Small in Size – Great in Performance
or's 3U boards offer more CPU power and functionality on less than half of a 6U board.

Low Power CMOS
The 100% CMOS design guarantees lowest power consumption: e.g. our 68030 CPU board requires only +5 V, 0.85 A at 32 MHz!

-55° to +105° C
The cold CMOS design combined with conduction cooling assures operation at the extreme of +105° C.

100 G Shock
or's stiffened 3U boards are almost completely shock and vibration proof. Jumpers and sockets have been replaced.

Highest MTBF
or's ruggedized boards have set marks in VME: e.g. our 68030 CPU boards has an MTBF of 740,000 hours! (MIL-HDBK-217, 20° C).

Broad Product Range
68040 CPU, 68030 CPU, dual 68302 communication contr., graphics, MIL-STD-1553B, ARINC-429, SCSI, ethernet, flash-disk, synchro-resolver, digital I/O, analog I/O,.... VRTX-32, PSOS®, OS-9, ADA, C,....

4 Styles – Low Cost
Four software-compatible styles from economy to MIL-883/B cover all environmental needs at best prices.

Controlled Quality
or's quality assurance complies with AQAP-4 and MIL-1-45208.
CYPRESS MEMORY AND SILICON GRAPHICS WORKSTATIONS COMBINE TO CREATE SOME SEXY GRAPHIC EFFECTS. If you're like most, you loved the stunning special effects in "The Lawnmower Man." They gave you an imaginative preview of what Virtual Reality might look like in the near future. To design and create those effects, Angel Studios relied heavily on cutting-edge Silicon Graphics® workstations, spurred on by lightning-fast Cypress memory.

Cypress offers a full range of high-performance products, including SRAM and PROM memories, PLDs, SPARC microprocessors, logic products, BiCMOS ECL memories, and multichip modules. Products that can make your designs highly attractive. If you're ready to embrace top line performance, call for the Cypress Data Book.

FOR A FREE DATA BOOK AND POSTER OF THIS AD CALL OUR HOTLINE: 1-800-858-1810* Ask for Dept C116.

*In Europe, fax your request to the above dept. at (32) 2-652-1504 or call (32) 2-652-0270. In Asia, fax to the above dept. at (415) 961-4201.
© 1992 Cypress Semiconductor, 3901 North First Street, San Jose, CA 95134. Phone 1 (408) 943-2000, Telex 92102 CYPRESS SNJ LTO, TWX: 910-997-0753. "The Lawnmower Man" image was created by Angel Studios, Carlsbad, California. © 1992 Allied Vision Lane Pringle Productions. All rights reserved. Silicon Graphics is a registered trademark of Silicon Graphics, Inc.