

A PENNWELL PUBLICATION

COMPUTER DESIGN[®]

OCTOBER 15, 1988

THE FIRST MAGAZINE OF SYSTEM DESIGN,
DEVELOPMENT AND INTEGRATION

Sharing design data
through networking



■ AI techniques
enter the realm of
conventional languages
Page 45

■ Caching options
eliminate wait states
to relieve bottlenecks
Page 65

■ Higher speeds,
CMOS designs drive
flash A-D converters
Page 74

WANT TO TALK SCSI? CALL CIPRICO AT 1-800-SCSI-NOW.

Why talk SCSI with Ciprico? To start with, we're the only vendor with a complete line of high-performance SCSI host bus adapters for Multibus® I, VMEbus, and Multibus II. Each board was designed to optimize performance with its system bus. And consider our experience. Ciprico has over 50,000 boards installed world-wide. Our design expertise provides you with the highest possible performance at the lowest possible price.

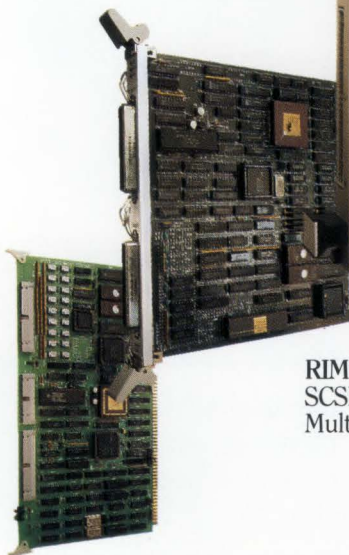
But that's not all. Ciprico has *responsibility*. We have the largest staff of customer support engineers in the industry to help you resolve any integration problems. Plus software drivers for all major operating systems.

Our SCSI adapters are all based on an 80186 microprocessor, providing a command queuing, pass-through SCSI command software interface. Each board supports SCSI disconnect/reconnect and asynchronous and synchronous transfer rates of 2MB/s and 5MB/s respectively. And a floppy port is optional for cost effective system design.

So if you're currently designing a system based on Multibus I, VMEbus, or Multibus II, give us a call to talk SCSI.

**CIPRICO**
2955 Xenium Lane
Plymouth, MN 55441
CIPRICO LISTENS. AND RESPONDS.

RIMFIRE 1500
SCSI Adapter for
Multibus® I

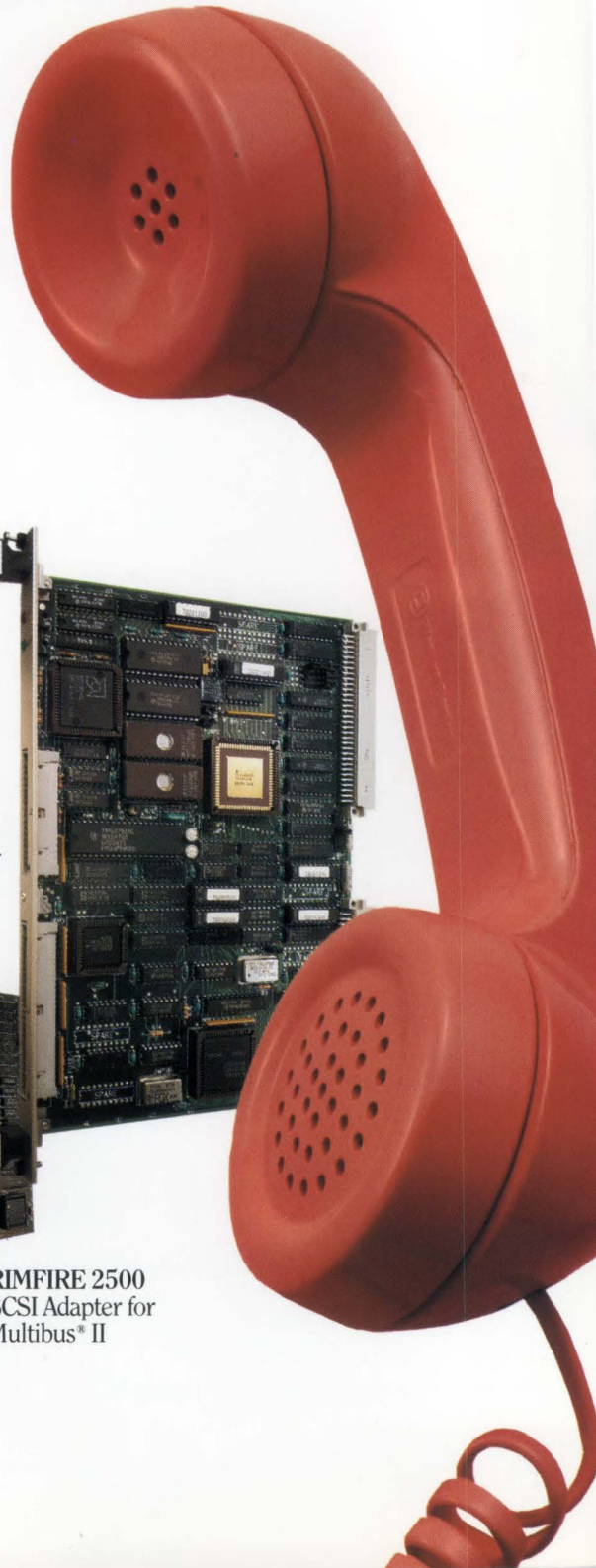


RIMFIRE 3510
SCSI Adapter for
VMEbus

RIMFIRE 2500
SCSI Adapter for
Multibus® II

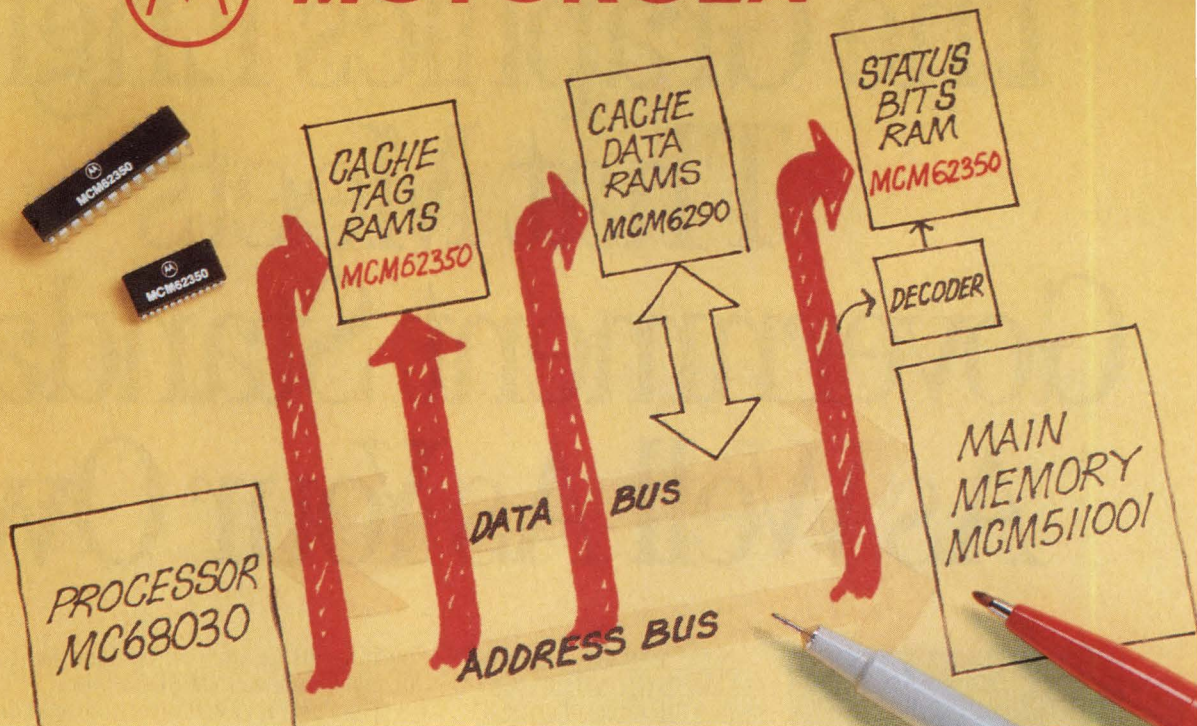
Multibus is a registered trademark of Intel Corporation.

CIRCLE NO. 1





MOTOROLA



Extra cache helps.

New Cache Tag RAMs from Motorola enhance any 32-bit MPU's performance.

Motorola's new MCM62350 and MCM62351 4Kx4 Cache Tag RAMs give you the chance to maximize performance with any 32-bit microprocessor.

Even MPUs with Motorola-pioneered on-chip cache can be enhanced. This new Cache Tag RAM line offers the best solution.

Only from Motorola.

Now, address four times as much cache. And only Motorola's Cache Tag RAMs can double as Status Bit RAMs. This exclusive innovation lets you set, clear, read, write and compare individual status bits.

It's possible, using the '62350-51, to duplicate the MC68030 cache architecture in which internal caches store four 32-bit long words for each tag and still maintain a status bit for each long word.

Both new types feature Exclusive NOR (XNOR) and AND-OR-Invert (AOI) comparison modes, and address valid to match valid times of 25 and 30 ns.

Still, performance is only part of the story. We're the first to make Cache Tag RAMs available in the popular SOJ package as well as the plastic DIP. In addition, Motorola offers the industry's first multi-sourced Cache Tag RAM, the MCM4180. And there's more.

Soon more new fast SRAMs will be available to boost performance in other system cache memory sockets.

For additional information, call us toll

free any weekday, 8:00 a.m. to 4:30 p.m.,


1-800-521-6274

MST, from anywhere in the US or Canada. Or write or send the completed coupon to Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036.

**We're
on your
design-in
team.**



MOTOROLA



To: Motorola Semiconductor Products, Inc.,
P.O. Box 20912, Phoenix, AZ 85036
Please send more information on Motorola Cache Tag RAMs. 365CD101588

Name _____

Title _____

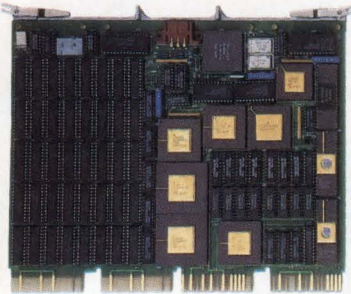
Company _____

Address _____

City _____ State _____ Zip _____

Call me (_____) _____

The Graphics Engine That Meets Government Standards As Well As Your Own.



Now—your DEC MicroVAX or VME-based systems can meet a full range of critical government standards for high performance graphic workstations, thanks to three new versions of CalComp's hot Formula 1 graphics engine.

These single card Formula 1 solutions are engineered with the same "four on the

floor" custom VLSI technology that runs up to four workstations from a single platform. With graphics superiority you can see at a glance.

Zoom, pan and update with turbo-charged speed and high-visibility 1280 x 1024 resolution. With on-board 32-bit floating point processor, 68020 command processor, display list and six custom VLSI gate arrays as standard equipment. Whatever your software interface is, CalComp has the solution ... graphic interfaces from CGI to GKS and language bindings—Ada, C and Fortran.

The powerful Q-bus Subsystem is designed both for the DEC MicroVAX and the new 3000 series. You get a full subsystem package including the Formula 1 card, enhanced for VMS and ULTRIX.

The VME Subsystem starts with an industry standard 6U160 VME card that supports X-Windows and UNIX. CalComp can supply you with VME modules or a total subsystem for integration into your system.

The Formula 1 meets your TEMPEST requirements, too. Choose a subsystem designed for DEC's TEMPEST MicroVAX II, or combine the graphics engine with CalComp's TEMPEST

peripherals for your own unique solution. All are designed to meet NACSIM 5100A.

The Formula 1 will meet your standards for price and performance—without sticker shock. You can drive away with an entire Formula 1 Subsystem—card, high-resolution color monitor, keyboard and mouse—starting at \$6995. Or choose the card alone, for as low as \$3995. Attractive OEM discounts are available.

For more information, call: 1-800-CALCOMP. Or write: P.O. Box 3250, Anaheim, CA 92803.



We draw on
your imagination.™

 **CalComp**

A Lockheed Company

CIRCLE NO. 3

DEC and MICROVAX are registered trademarks of Digital Equipment Corporation. UNIX is a registered trademark of Bell Laboratories. Formula 1 is a trademark of CalComp Inc. © 1988 CALCOMP Inc.

THE FIRST MAGAZINE OF SYSTEM DESIGN, DEVELOPMENT AND INTEGRATION



Page 21

TECHNOLOGY UPDATES

Integrated Circuits

Chip set tackles laptop design issues, offers flat-panel VGA control21

DSP-based microcontrollers blaze new trails into real-time computing23

Software

Unix gains edge over OS/2 by running DOS applications26

Design and Development Tools

Development tools enhance real-time Ada support31

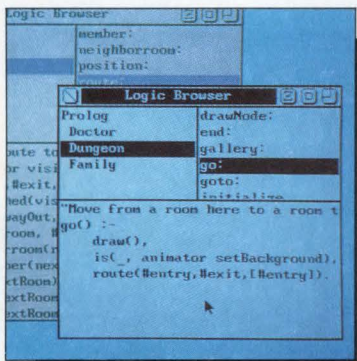
Off-the-shelf in-circuit programmers cut costs, ease firmware updates32

Printed circuit board component libraries deliver consistency and accuracy33

Computers and Subsystems

Multiprocessing cache bus turns to AT bus for I/O36

Hybrid board scheme bridges optical and electrical circuitry38



Page 45

TECHNOLOGY AND DESIGN FEATURES

AI techniques enter the realm of conventional languages

AI techniques become practical and accessible by linking AI modules written in languages such as Lisp or Prolog into conventionally coded systems.45

Clear-cut than the implementation as they work to link diverse sets of computing resources.50

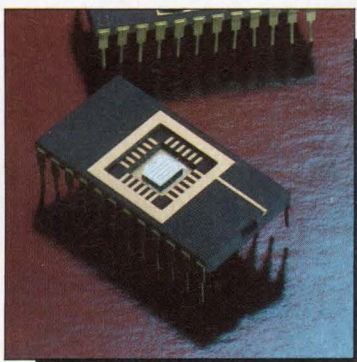
Caching designs eliminate wait states to relieve bottlenecks

Alternative approaches to cache architectures present a range of trade-offs in cost, performance and complexity.65

COVER STORY

Sharing design data through networking

Engineering managers find that the benefits of CAE/CAD networks are more



Page 74

NEW PRODUCT HIGHLIGHTS

PRODUCT FOCUS

Higher speeds, CMOS designs drive flash A-D converter developments74

Computers and Subsystems

Macintosh II floating-point coprocessor performs 20 MFlops82

Data Acquisition and Control

Analog-to-digital I/O board speeds to 1 Msamples84

Design and Development Tools

Emulator boasts zero wait states at 16 MHz85

Integrated Circuits

Twelve-bit multiplying D-A converter hosts on-chip amplifier86

Major System Components

VMEbus monolithic backplane features low-capacitive loading88

Software

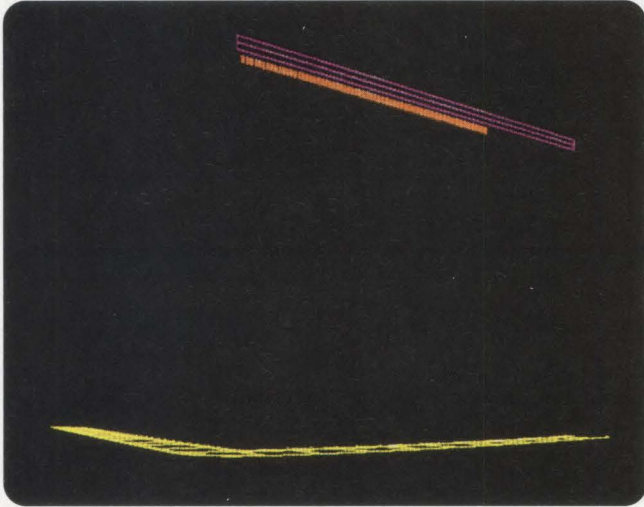
Software package brings parallel processing to Ada89

Product Briefs90

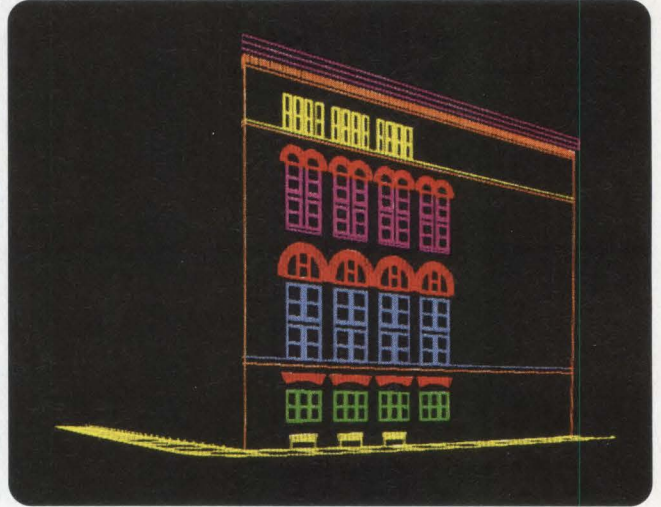
DEPARTMENTS/COLUMNS

News Briefs	9
Editorial	14
New Products Index	90
Advertisers Index	94
Last Bits	96

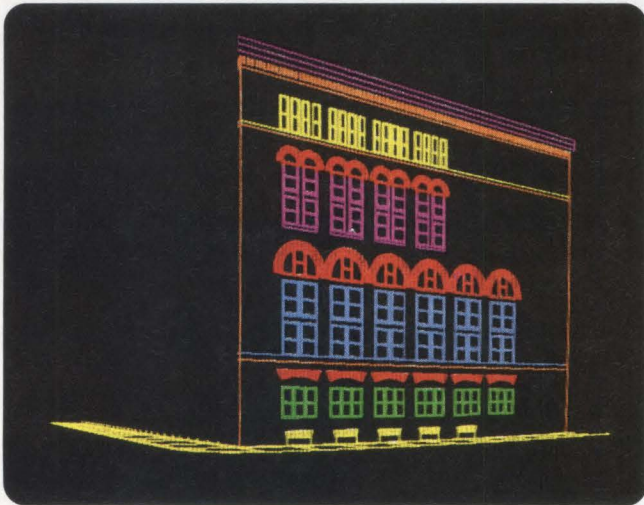
In the time it takes other graphics engines to draw a few lines...



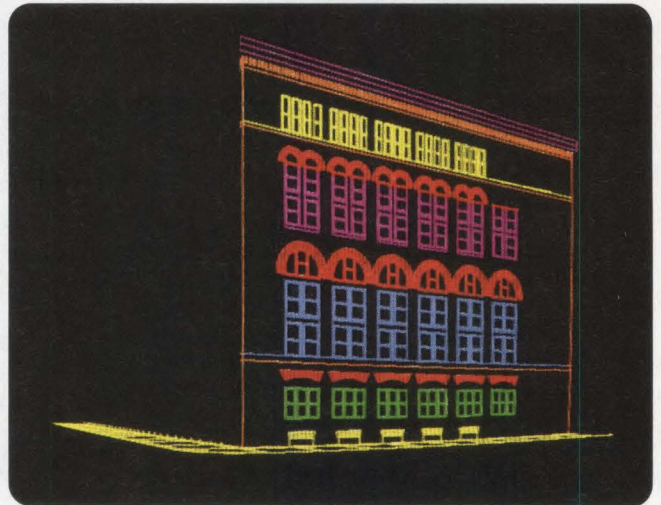
Texas Instruments TMS 34010 (2%)



AMD Am95C60 (17%)



Hitachi HD63484 (20%)



Intel 82786 (25%)

*GeoCad® perspective drawing courtesy of Rudolph Horowitz and Associates, Architects.
Simulated performance based on maximum patterned line-drawing rates in an eight-bit color system with a resolution of 1024 by 768.
Of course, performance ultimately depends on system elements like memory speed.*

ours gives you the whole picture.

THE FIRST FULLY PROGRAMMABLE GRAPHICS PROCESSOR WITH ON-CHIP ACCELERATION

You can have the fastest calculations in the world but if your system's graphics are slow, your system is slow. National's latest addition to its Advanced Graphics Chip Set—the DP8500 Raster Graphics Processor (RGP)—is the fastest graphics engine on the market.

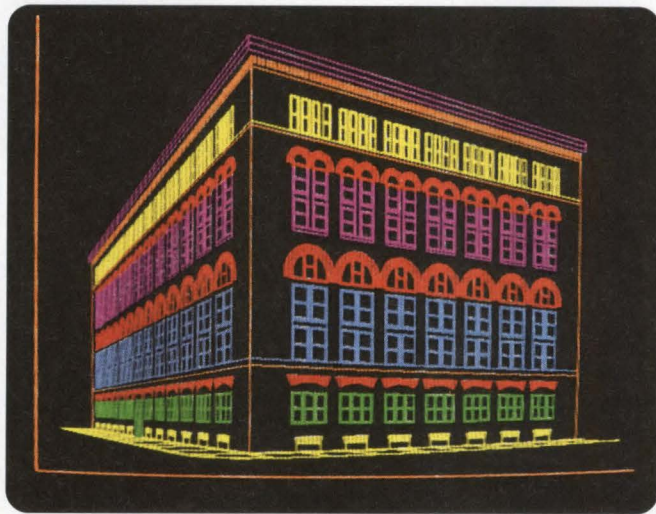
This 20-Mhz CMOS chip features a bus cycle time of 100 nanoseconds on back-to-back vector and block operations.

It gives you blazing speed in line drawing, BitBLT, fills, polygons, character drawing, and windowing—regardless of the number of bit planes. It also controls screen refresh.

COMPLETE FLEXIBILITY

The RGP gives you the programmability of a general-purpose processor, so you can optimize your system for specific applications. Or differentiate it from your competitors through proprietary algorithms.

The RGP, with our DP8511 BitBLT processing unit, is also the only



National DP8500 Raster Graphics Processor

graphics solution that effectively allows you to select either planar or pixel-oriented operation on-the-fly. So you no longer have to lock yourself into one architecture or the other.

The RGP handles the very highest-resolution CRTs and printers, including laser printers. And it supports any type of memory.

It also gives you the right "hooks" and the right architecture for moving into 3D and solids modeling applications.

A COMPLETE SET OF CHIPS

Our Advanced Graphics Chip Set also includes

- two BitBLT processing units
- four video clock generators
- four video shift registers
- three video RAM controllers
- a growing list of video DACs

They're all part of National's unique modular approach—the only approach that addresses the complete graphics pipeline. And the only one with the performance and flexibility you need to carry you into the 1990s.

COMPLETE SUPPORT

We offer a wide range of software tools—including assembler, debugger, librarian, linker, software

utilities, graphics kernel packages, and a C compiler package.

Nova Graphics International is providing full support for graphics software standards, including GKS and CGI.

Check it all out for yourself with the DP850EB demo/evaluation board for only \$1495. Buy the board and we'll include a coupon good for ten free RGPs on your first order of 100 or more.

To order today, call National Semiconductor at (408) 721-5404. Or for a copy of our system-level comparison brochure, circle the reader service number.

 **National Semiconductor**

CIRCLE NO. 4

©1988 National Semiconductor Corporation

**Advanced
Peripherals**

SHIPPING NOW

A 386 μ P.
155 supporting chips.
And no time
to breadboard.



A80386-16
S40344
I649202R
© © i '85-'86

Mentor Graphics lets you simulate an 80386-based motherboard in only 4.3 minutes.

You're designing a complete 32-bit PC motherboard. And you're running out of time.

Your only hope is to bypass the time-consuming breadboard phase and debug directly through simulation. Which means simulating 32 I/O write cycles that program the board's peripheral chips for normal operation — 27,942ns of execution time, including a memory refresh.

So you turn to Mentor Graphics' QuickSim™ logic simulator and run the design file—21 sheets in all, including an Intel 80386 microprocessor and 155 other IC packages, each represented by a SmartModel™ from Logic Automation, Inc.

The result? Simulation completed in just 4.3 minutes.

Introducing the soft breadboard.

With Mentor Graphics, you have a production-proven way to create and debug systems designs—in software. During simulation, design schematics can be displayed, probed, modified, and resimulated. And to complement your simulation, QuickPath™ rapidly checks your design for critical path timing problems. All in a single, interactive work environment.

Your debug operations stay right on your Mentor Graphics workstation, where engineering changes are fast, simple and inexpensive.

Modeling is the key.

Systems simulation requires a wide range of

modeling technologies. And that's precisely what we deliver. Like Behavioral Language Models (BLMs), which transcend basic functionality and deliver features such as automatic error detection and reporting. And QuickParts™, which combine maximum speed with minimum memory requirements—and produce timing behavior identical to the data book.

There's also our Hardware Modeling Library™, which provides modeling for VLSI parts, including the latest microprocessors. Plus unparalleled support for ASIC libraries, so you can include your ASIC directly in your board simulation.

Once design and analysis is complete, other Mentor Graphics tools follow your design through PCB layout, mechanical packaging, thermal analysis and documentation.

To be continued.

So much for the present. We're already developing new EDA tools for systems design that will extend to every dimension of electronic product development. From high-level systems descriptions to CASE.

It's all part of a vision unique to Mentor Graphics, the leader in electronic design automation. Let us show you where this vision can take you.

Call us toll-free for an overview brochure and the number of your nearest sales office.

Phone 1-800-547-7390

(in Oregon call 284-7357).



Mentor Graphics®

SmartModel is a trademark of Logic Automation, Inc.

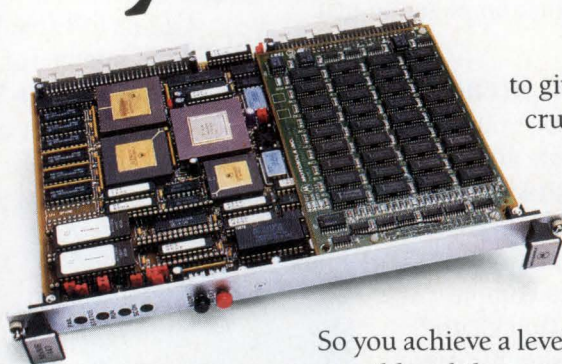
Your ideas. Our experience.

“Their new 030 board isn't really a single-board computer. It's a single-board system.”

OEMs weren't prepared for the level of *functionality* our new MVME147 processor module delivers. On one standard VME card, it packs virtually all the functions you need to build a small, multi-user system.

How? Mainly through ASICs like the single-chip VMEbus interface and Peripheral Channel Controller. Plus high-density on-board DRAM (4 or 8 Mbytes), SCSI interface and Ethernet chip set. To even come close in functionality, it would take as many as *five* conventional modules.

Besides which, the 147 outperforms everything in sight. It takes maximum advantage of Motorola's new 32-bit MPU—the MC68030—coupled with a floating-point coprocessor. Both running at up to 25 MHz,



to give you outstanding number-crunching power.

And since the 147 features both UNIX® and real-time operating system support, you can plug it into your existing 020-based architecture and software base.

So you achieve a level of integration never before possible, while protecting your existing investment. All of which gives you unprecedented price/performance advantages for just \$3747 in OEM quantities of 100.

To get an idea of what the future of VME looks like, call us today—toll free: 1-800-556-1234, Ext. 230; in California, 1-800-441-2345, Ext. 230. Or write: Motorola Microcomputer Division, 2900 Diablo Way, Tempe, AZ 85282.

UNIX is a registered trademark of AT&T.



MOTOROLA Microcomputer Division

Approaching our technology from your point of view.

Sparc wins and loses

Although endorsements for the popular Sparc RISC chip from Sun Microsystems (Mountain View, CA) continue to be announced, the chip may also be about to lose some significant support.

Rumors are circulating that AT&T (Morristown, NJ) is reconsidering its earlier commitment to Sparc and will turn instead to Motorola's 88000 as its core processor for future Unix System V-based computers. The Sun/AT&T agreement, signed last January, created a furor among Unix licensees that eventually resulted in the formation of the Open Software Foundation (OSF). Apparently, the agreement was also viewed within AT&T as a threat to the company's longstanding relationship with Motorola. AT&T uses Motorola's 68000 family of processors in its 3B line of minicomputers.

Meanwhile, Sun's plans to establish a group of highly competitive vendors for Sparc has taken several more steps forward. Following the announcement in August of a second-source agreement between previous Sparc licensee Cypress Semiconductor (San Jose, CA) and Texas Instruments (Dallas, TX), Fujitsu Microelectronics (San Jose, CA) and Prisma (Colorado Springs, CO) have made announcements of their own. Fujitsu has announced production release of its 15-Mips, second-generation S-25 Sparc CPU. Implemented in the company's 1.2-micron CMOS process, the chip will run at 25 MHz.

Separately, supercomputer design house Prisma announced plans to implement Sparc in gallium-arsenide MSI. The company reportedly plans to use logic chips from Gigabit Logic (Newbury Park, CA) to build a Sparc CPU system capable of 250-MHz operation and a peak execution speed of 250 Mips. Shipment is scheduled for late 1989.—*John Mayer and Ron Wilson*

A RISC solution takes wing

At the Buscon/88-East show earlier this month, a group of vendors unveiled what's touted to be the first complete real-time and general-purpose development system and

execution environment for a RISC processor: namely, Sparc from Sun Microsystems (Mountain View, CA). Cooperative development efforts among Fujitsu Microelectronics (Santa Clara, CA), Mizar (Carrollton, TX), Sun Microsystems (Mountain View, CA) and Wind River Systems (Emeryville, CA) have yielded their first fruit. The real-time compute server and a hybrid development system combines a Sun Unix environment and a Sparc real-time subsystem within a single enclosure. "Anyone who wants to do a real-time application with Sparc will now have all the hardware, software, development tools, and other support he needs," says Joe Ramunni, Mizar president and CEO.

—*David Lieberman*

Digital paper drives poised to boost optical storage

Mass storage peripherals using inexpensive, flexible "digital paper"—actually a Mylar substrate coated with photoactive polymer dye—are set to compete heavily in the optical storage arena. According to a report by Venture Development Corp (Natick, MA), Bernoulli Optical Systems (Boulder, CO), a subsidiary of Iomega (Roy, UT), is readying disk drives using digital paper, and Creo Products (Burnaby, BC, Canada) will use the paper in tape drives.

Digital paper disks can be accessed in around 40 ms, according to Robert Perera, director of research and development for Bernoulli. This access time, faster than that of rigid optical disks, is possible because the flexible media can be stabilized at the focal point of the laser head. Because the head needs no focusing mechanism and can be lighter than other optical heads, they can be positioned faster. Storage capacities on the order of 1 Gbyte on a 5¼-in. disk are expected.

The digital-paper-based tape drive under development by Creo is expected to boast 1,000 Gbytes per reel. Fabio Arcuri, market research analyst at VDC, calculates that a 2,900-ft reel of digital paper tape would have the capacity of a 20-ft optical disk—with sequential access, of course.—*Tom Williams*

DEC to purchase new RISC chip for Unix workstation

Digital Equipment Corp (Maynard, MA) has finally gone public with its long-rumored agreement to purchase RISC microprocessors from MIPS Computer (Sunnyvale, CA). DEC will use the MIPS processor in a line of Unix workstations. The move is apparently a counterstroke against the success of Sun Microsystems (Mountain View, CA) in penetrating the decade-old VAX/VMS hegemony over engineering computing. Previous DEC attempts to fight against Sun and Apollo workstations with its proprietary MicroVAX architecture have seen only limited success. Under the agreement, DEC will take an equity position in closely held MIPS that could reach as much as 20 percent of the company.—*Ron Wilson*

The PS/2 clone countdown

There are 30 days left until Comdex '88 convenes in Las Vegas, and the odds are excellent, according to well-placed sources, that somewhere between a half and a full dozen computer vendors will introduce their first PS/2 clones at the show, joining the three vendors who have already taken the plunge.

Even more board, system and peripheral vendors may use the show to preannounce PS/2-compatible products, unless the recent announcement of the EISA (Extended Industry Standard Architecture) alternative to IBM's Micro Channel architecture moves them to continue to keep their PS/2-compatible prototypes under wraps. Should the EISA indeed contribute to the already widespread uncertainty about the advisability of supporting the PS/2, expect to see a slew of "EISA-compatible" banners gracing the wealth of new AT-compatible products certain to appear at the show. Then, of course, there will be those who hedge their bets by supporting both the Micro Channel and the EISA.—*David Lieberman*

(continued on page 10)

OEM superminis tackle real-time applications

Thanks to a cell-based application-specific IC processor, a new family of high-performance computers from Modcomp (Fort Lauderdale, FL) can tackle real-time applications without the need for additional front-end processors. The ASIC processor provides over 10 Mips to give the series the ability to address the computational speed requirements of real-time systems. Additional computational power is available using an optional hardware floating-point accelerator.

The company uses an advanced 299-lead ceramic pin grid array to handle the main processor chip, which packs over 220,000 transistors (54,000 gates) and was developed in conjunction with VLSI Technology (San Jose, CA). Cache and memory-management handling for the machines is provided through ASICs, while interrupt handling and I/O throughput are managed with additional ASIC components as well as standard ICs. Introduction of this yet-to-be-named series of computers is slated for Autofact next month.—*Sydney Shapiro*

DEC submits XUI user interface tools to OSF

Digital Equipment Corp (Maynard, MA) has formally submitted its XUI user interface technology in response to the Open Software Foundation's request for graphical user interface technology. All technologies submitted must conform to the X Window System, Version 11, which was developed at the Massachusetts Institute of Technology (Cambridge, MA).

Designed to run on any hardware platform, the XUI programming environment consists of a toolkit, a style guide, a window manager, a session property manager and associated documentation. With XUI, programmers can design a graphical user interface with icons, scroll bars, and pull-down menus for their programs. DEC designed the technology to provide a single applica-

tion program interface for systems supporting the X Window standard and to eliminate the problems associated with multiple operating system environments.—*Mike Donlin*

PC-based system uses CD-ROMs to automate component selection

A PC-based system gives engineers access to technical specifications and manufacturer's data sheets for ICs and discrete semiconductors. Called Cahners CAPS (Computer Aided Product Selection) by Cahners Information Services (Newton, MA), the system stores text and graphics images of over 400,000 devices from more than 250 companies worldwide on a set of CD-ROMs.

CAPS installs on a subscriber-provided IBM PC AT or compatible and consists of a four-disc CD-ROM reader, a high-resolution full-page monitor and a mouse. Data base updates are issued to subscribers at 90-day intervals and include information on new components, manufacturers' revisions and cross-reference part numbers. A one-year subscription, including hardware, costs \$7,950.—*Mike Donlin*

Whither the Micro Channel?

Is IBM slowly abandoning the Micro Channel? Just a few weeks after introducing a new PC based on the older AT bus, and just one week after IBM's major PC rivals banded together to endorse an extended version of the older bus architecture, reports are circulating that IBM is working on yet another PC not built around the Micro Channel. The new system reportedly uses Intel's new 80386SX processor, a stripped-down version of the popular 80386 with a 16-bit data path. If not indicative of any erosion of IBM's support for the Micro Channel, the "new/old" PCs just may reflect the company's reassessment of its decision to quickly abandon the older AT architecture after introducing the Micro Channel-based products.—*John Mayer*

Quarter-inch tape vendors fight back against DAT

For those tempted to exchange their familiar ¼-in. cartridge tape drives for one of the latest wrinkles in magnetic storage—the computer-oriented variety of digital audio tape (DAT)—the ¼-in. industry suggests another solution: stick with what you have. Since many designers have become enamored of the very high capacities possible with DAT, the Quarter-Inch Cartridge (QIC) standards committee will push its products beyond the current 320-Mbyte frontier into the 1.3-Gbyte capacity range by 1990 and to as much as 4 Gbytes by 1993. "This natural migration path will all be based on the use of reliable, widely accepted DC600-class cartridges," says Sam Thompson, committee chairman, "and the resultant product class will have capacities equal to new, competing technologies such as DAT, while achieving faster transfer rates."

—*David Lieberman*

EDIF interface boosts CAE system independence

Designers can now transfer schematics and net lists between multivendor application-specific IC design-automation tools by using a software interface from Synopsys (Mountain View, CA). The interface allows automatic EDIF (Electronic Design Interchange Format) net list-to-schematic translation in either direction between the company's Design Compiler and standard EDIF-compatible files available from most major CAE vendors. Although EDIF has been around since 1983, true compatibility between systems has been hindered by differences in each system's design data. The Synopsys interface tackles that problem by extracting the design from its source representation and then regenerating it into an EDIF description in the context of the target system.—*John Mayer*

TRY
THE 212 FOR
15 DAYS
at no obligation.



A NEW PROGRAMMER FOR BIG IDEAS AND SMALL BUDGETS.

THE NEW 212 REDUCES THE COST OF HIGH PERFORMANCE. Now it doesn't take a large budget to get all the support you need for memory devices, plus the performance of a Data I/O® programmer. The new 212 Multi Programmer offers broad device support today, and the ability to upgrade and expand tomorrow. It makes programming big ideas easy.

SUPPORT FOR MEGABIT PARTS AND MICROCONTROLLERS. The 212 programs more than 350 MOS and CMOS PROMs, EPROMs and EEPROMs in 24-, 28-, 32- and 40-pin packages. With the optional micro module, the 212 can also handle single-chip microcontrollers.

HIGH-SPEED DATA TRANSFER. A two-in-one bi-directional parallel and serial port allows fast, easy transfer of large files. It also makes the 212 flexible enough to interface to a handler.

Use the RS232C capability for simple interfacing to a host computer, PC or printer. Add PROMlink Interface and File Management Software and you can edit, program, and even customize menus from your PC.

FAST PROGRAMMING ALGORITHMS.

The 212 uses the fastest available programming algorithms such as Intel's Quick Pulse™ and Flash™, AMD's Flashrite™ and Texas Instruments' Snap™. And with serial set programming, 8-, 16- and 32-bit data is fast and easy to program.

RAM EXPANDABLE TO EIGHT MEGABITS. The standard two megabits of RAM is upgradeable to eight megabits, giving you extra capacity for larger devices.

MEMORY CARD PROVIDES EASY UPDATES. The 212's memory card lets you update algorithms without firmware changes. Just slip in a new card.

QUALITY AND RELIABILITY BUILT IN.

The 212 offers the speed, reliability and accuracy you'd expect from a Data I/O programmer. It's built to last and is fully supported by our worldwide sales and service network.

TRY THE 212 FOR 15 DAYS WITH NO OBLIGATION. If your design ideas are bigger than your budget, the 212 is the programmer for you. Call us today and we'll give you 15 days to prove it.



Visa and MasterCard accepted.

1-800-247-5700
Ext. 846

Data I/O Corporation 10525 Willows Road N.E., P.O. Box 97046, Redmond, WA 98073-9746, U.S.A. (206) 867-6899/Telex 15-2167
Data I/O Canada 6725 Airport Road, Suite 302, Mississauga, Ontario L4V 1V2 (416) 678-0761
Data I/O Europe World Trade Center, Strawinskylaan 633, 1077 XX Amsterdam, The Netherlands +31 (0)20-6622866/Telex 16616 DATIO NL
Data I/O Japan Sumitomoseimei Higashishinbashi Bldg., 8F, 2-1-7, Higashi-Shinbashi, Minato-ku, Tokyo 105, Japan
(03) 432-6991/Telex 2522685 DATAIO J

How the fa

Our new 75ns PAL[®] device is fast enough to prove that standard logic shouldn't set the standard anymore.

It's also fast enough to finally let today's new microprocessors run at the speeds for which they were designed—breathtaking.

Raising your standard.

How fast would you like your standard logic?

How about faster than any TTL logic around? Even FAST[™] or AS? You've got it with the 75ns PAL device.

And the fact that you can config-

ure it yourself means you can get exactly what you want.

If you want to redesign something, you change the PAL device. Not the board.

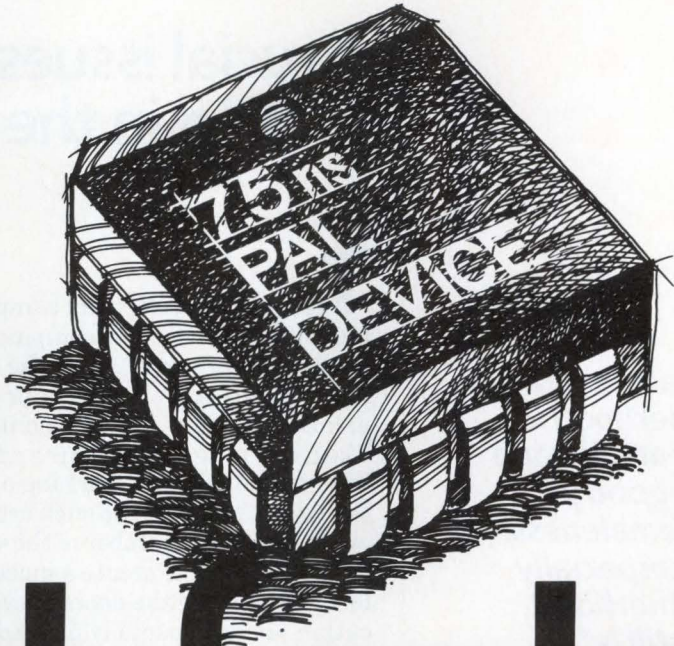
Not only is this the fastest way to get high speed logic, it's also the most practical. One 75ns PAL device replaces two to six standard TTL devices.

Which cuts down on board size.

And cuts down chances for a device failure.

75ns PAL Device vs. FAST & AS

SSI/MSI		FAST	AS	75ns PAL Device
Combinatorial				
74138	tPD	8.0	10.0	7.5
Decoder				
74151	tPD	11.0	15.0	7.5
Mux				
Register/Latch				
74374	tCO	10.0	9.0	6.5
Octal Register				
74373	tPD	8.0	6.0	7.5
Octal Latch	tLEO	13.0	11.5	7.5
Counters				
74161	tS	5.5	8.0	7.0
Four bit Ctr	tCO	11.0	13.5	6.5
74269/869	tS	2.5	5.0	7.0
Eight bit Ctr	tCO	10.0	11.0	6.5



st get faster.

What to give the microprocessor that has everything.

We suggest the first PAL device that can keep up with it.

The 75ns PAL device runs at 74 Mhz. It can deliver the speed the new high performance microprocessors need.

Processors like the 29K, the 386 and the 68030.

This PAL device delivers 25% more speed than any other PAL device.

We even have the fastest 22V10.

Our 15ns 22V10 runs at 50Mhz. That's 10ns faster than anyone else on the market. And it lets you run at twice the rate of the new 25Mhz microprocessors.

We've been shipping 20 pin 10ns

PAL devices for eighteen months. And now you can get the new 24 pin 10ns PAL device as well.

There's plenty of service and support to get and keep your project moving. And all our fast PAL devices are available in volume when you need them. Now, for example.

For all the facts about our fast PAL devices, drop us a line. Or call us at (800) 222-9323.

Because you can never be too fast.

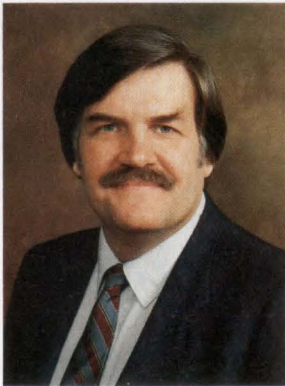
Advanced Micro Devices 
Monolithic Memories 

901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088.

PAL is a registered trademark of Advanced Micro Devices, Inc. FAST is a trademark of National Semiconductor Corporation. ©1988 Advanced Micro Devices, Inc.

CIRCLE NO. 32

"Maleness or fatherhood is never an obstacle to a good job, but femaleness, and especially motherhood, still is."



John C. Miklosz
Associate Publisher/
Editor-in-Chief

Crucial issues buried in the noise

This year's presidential campaign has been marked by so much mudslinging, negative campaigning and evasion that even the few positive proposals made by the campaigners have been lost in the noise. Bush's day-care plan, for example, was ridiculed into oblivion, and Dukakis's college-financing proposal seems to have evaporated like a morning fog. At a time when the United States is challenged by determined, hard-working and ruthless competitors throughout the world, how can two such crucial issues—one, our ability to utilize every potential member of the work force who wants to work, and two, our ability to create a more knowledgeable and skilled work force by opening the doors to everyone who wants a college education—be so brusquely pushed aside? It boggles the mind, to use a tired, but true, cliché.

The United States has an enormously underutilized resource in its female population. Despite all of the gains that have been made over the last 20 years or so, there's still a long way to go before women have a fair shot at all of the jobs—and everything that goes with them—that are open to men. You only have to look at the number of women in science and engineering to see that this is so. Maleness or fatherhood is never an obstacle to a good job, or good pay, or rapid advancement or a rewarding career, but femaleness, and especially motherhood, still is. The time has long since passed for us to remove this last barrier. Many of our competitors, even those in which women are still second-class citizens in every way, provide better day care than the United States does. The options are many, and a tax credit is only one of those that should be—no, must be—explored.

Male or female, the route to a good job, good pay, rapid advancement or a rewarding career is a dead end for most without a college education. But getting a college education today means having parents who are well-off—nothing short of wealthy, it seems—or who are self-sacrificing, or who are poor enough to have their children qualify for assistance in one form or another. A lot of youngsters who are smart, hard-working and deserving of an education are simply left out. A simple solution to this vexing problem is to have the individuals who will benefit from a college education over their lifetimes pay for that education over their lifetimes. According to Dukakis's proposal (which was nothing new, by the way), an eighth of a percent tax for every thousand dollars borrowed for a college education—maybe we should say “invested” in a college education—would do the trick. What's that, compared to the extra quarter of a million dollars, more or less, that a college education is worth over a lifetime?

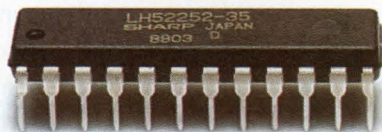
A handwritten signature in black ink that reads "John Miklosz". The signature is written in a cursive style with a large, prominent 'J'.



IN VANCOUVER, WASHINGTON, WE'VE JUST ISSUED PERMITS TO BREAK SPEED LIMITS.

How do you keep ninety of the country's hottest design engineers happy? First, give them permission to pull out all the stops. Then give them a place to do it.

That's exactly what we've done at our new Sharp Microelectronics Technology Center in Vancouver, Washington. There we've provided our outstanding staff with the most advanced CAD systems available. And we've backed them with a world-class 1.2 micron production facility in Japan, along with a national network of salespeople and distributors.



Sharp's new LH52252 64k x 4 SRAM

The purpose of all this? To aggressively carve a niche for ourselves by creating a select line of high-speed chips. Like the new Sharp LH52252, our 64k x 4 SRAM that operates at 35 ns cycle time and consumes just 100 microamps in standby mode. It's the first of many high performance products you can expect from our new design center. And it's available right

now at Marshall, Milgray, Western Microtechnology, Space Electronics, and Added Value.

If you have specific questions, we invite you to call Sharp at (201) 529-8757. Especially if moving at 35 ns or faster

sounds appealing. Because if you like breaking speed limits, Sharp has just the ticket.

SHARP'S NEW HIGH-SPEED CMOS SRAMS			
DEVICE #	ORGANIZATION	ACCESS TIME	AVAILABILITY
LH52252	64k x 4	35 ns/45 ns/55 ns	Immediate
LH52259	32k x 9	35 ns/45 ns/55 ns	3Q 1988
LH52251	256k x 1	35 ns/45 ns/55 ns	3Q 1988
LH52256	32k x 8	70 ns/90 ns/120 ns	Immediate
LH5261	64k x 1	25 ns/35 ns	1Q 1989
LH5262	16k x 4	25 ns/35 ns	4Q 1988

SHARP
ELECTRONIC COMPONENTS DIVISION

IF IT'S SHARP, IT'S CUTTING EDGE.™

PERFORMANCE

NOW WITH
C SOURCE
LEVEL DEBUGGER

It's what you expect from a finely-tuned machine. It's what you get from our 68HC11 cross development toolkit. The toolkit consists of a highly optimized C cross compiler and powerful support tools, a macro assembler and a microprocessor simulator. In short, everything you need for developing C language programs for your Motorola 68HC11 processor. Each product can be used separately, but together they deliver optimized performance that will improve your productivity. That's because all the components of the toolkit have been specifically



designed to work together. You don't waste time and effort reformatting files and shifting among diverse tools. And if you are interested in developing and debugging 68HC11 embedded programs in real-time, you can use our toolkit with an emulator from one of today's leading vendors. To experience the performance of our 68HC11 toolkit, and to receive an up-to-date list of compatible emulators, call our toll-free number, 800-225-1030. Within Massachusetts, call 508-692-7800.



WHITESMITHS, LTD.

CIRCLE NO. 8

This issue's cover. . .



Cover design by Sergio Roffo

As the complexity of a design project grows, more and more people must have ready access to the design data. And as the number of people involved in a design grows, so do the demands for access to specialized, usually expensive, resources such as hardware accelerators. When you add to this the potentially explosive proliferation of CAE/CAD workstations as hardware prices continue to fall, it's clear that everyone responsible for the design strategy must be equally involved in the networking strategy. For only through networking can all of the grasping, covetous hands reaching for a piece of the data be kept occupied.

COMPUTER DESIGN

THE FIRST MAGAZINE OF SYSTEM DESIGN, DEVELOPMENT AND INTEGRATION

PUBLISHER
David L. Allen

ASSOCIATE PUBLISHER/EDITOR-IN-CHIEF:
John C. Miklosz

TECHNOLOGY EDITORS:
Ron Wilson, *Integrated Circuits* (Portland)
Warren Andrews, *Integrated Circuits*
David Lieberman, *Computers & Subsystems*
Tom Williams, *Graphics & Imaging*
John H. Mayer, *Computers & Subsystems*
Sydney F. Shapiro, *Data Acquisition & Control*

CONTRIBUTING EDITORS:
S. Louis Martin, *Integrated Circuits*
Bill Harding, *Design & Development*
Howard Falk, *Software*
Art DeSena, *Testing & Manufacturing*

RESEARCH/SPECIAL PROJECTS MANAGER:
Sydney F. Shapiro

SECTION/SPECIAL PROJECT EDITORS:
Ron Wilson, *Technology Updates*
David Lieberman, *Contributed Articles*
Michael G. Donlin, *New Products*
Patti Kenney, *Directories*

MANAGING EDITOR: Susan R. Nykamp

ASSISTANT EDITOR: Kerstin L. Rosenquist

COPY EDITORS: Richard Dagley, Barbara-Ann Scofidio

EDITORIAL ASSISTANTS: Claire Coupal, Claire Ellis

WEST COAST EDITORIAL OFFICES
MANAGING EDITOR: Tom Williams

75 Mount Heman Rd, Suite E-180
Scotts Valley CA 95066, Tel: (408) 335-5514

1111 S.W. Gaines, No. 8
Portland, OR 97201, Tel: (503) 224-9396

ART DIRECTOR: Jan Horner
ILLUSTRATOR: Christopher Hipp

PRODUCTION DIRECTOR: Jan M. Lopez
PRODUCTION MANAGER: Mari Rodriguez
ADVERTISING COORDINATOR: Adrienne Adler
COMPOSITION MANAGER: Holly Kersey
COVER ART: Sergio Roffo

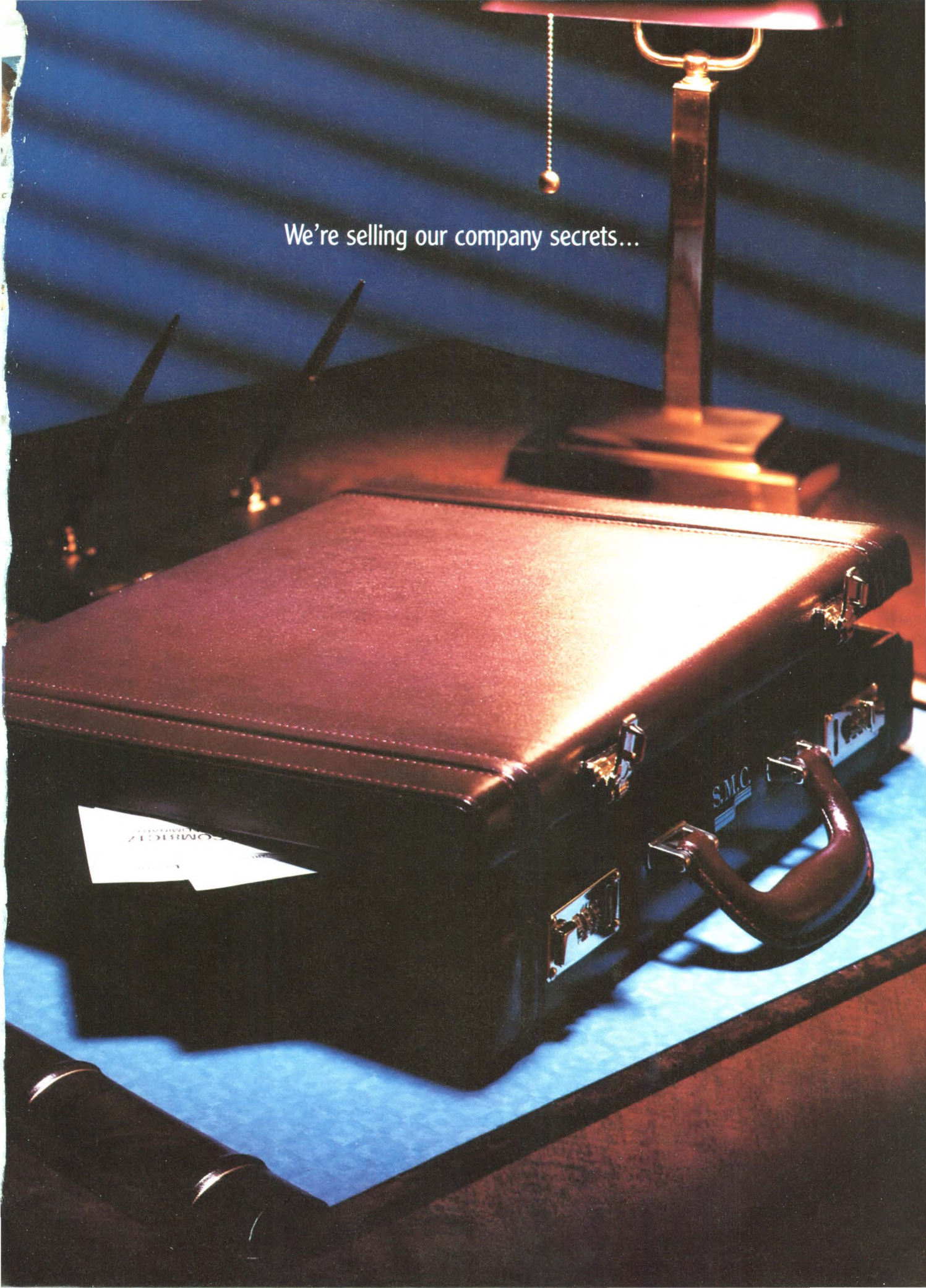
CIRCULATION DIRECTOR: Robert P. Dromgoole

PennWell
PUBLISHING COMPANY

Advanced Technology Group
L. John Ford, Senior Vice-President
Leslie P. Cypret, Vice-President, Administration
P.O. Box 417
119 Russell St, Littleton, MA 01460
Tel: (508) 486-9501
Fax: (508) 486-9397

Postmaster: Send change of address form 3579
to COMPUTER DESIGN, Circulation Department,
Box 3466, Tulsa, OK 74101

We're selling our company secrets...

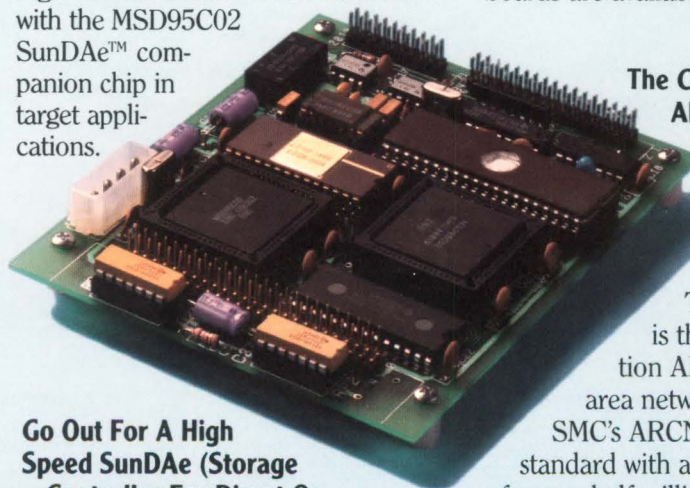


...AND SMC'S 17 YEARS OF CAN BE THE SECRET OF

For nearly two decades SMC® has focused its technological expertise on the design and manufacture of application specific integrated circuits for the microperipheral industry. Our CMOS solutions for display, storage, data communications and local area networks begin with Standard Components such as:

Big Performance In A SCSI (Small Computer System Interface Controller)—SMC's MSD95C00.

This design features automatic arbitration for data transfer on an ANSI SCSI compatible computer bus. It also offers selection and reselection of devices, allowing simultaneous processor operation and transfer of entire commands from an initiator with minimal host processor intervention. This is due to the internal twelve byte buffer, which supports 5 MBytes/sec. synchronous and 3 MBytes/sec. asynchronous data transfer modes. It also features on-chip 48 mA high current drivers. It can be used with the MSD95C02 SunDAe™ companion chip in target applications.



Go Out For A High Speed SunDAe (Storage μ-Controller For Direct Or Serial Access Devices) Drive—SMC's MSD95C02.

This is the next generation high speed micro-programmable mass storage controller ideal for embedded hard disk, QIC24 tape and

optical drives as well as PS/2, ESDI and SMD disk controllers. It allows the user complete flexibility in design via the internal 32×32 writeable control store. A powerful on-chip 3 channel DMA controller arbitrates cache transfers without microprocessor intervention. This product is organized in a modular fashion, based on SuperCells™, for easy adaptation to special purpose applications.

Make IBM® Micro Channel™ Bus Interface Adapter Boards Spectacularly Simple—SMC's MCI94C18.

This CMOS device is fully compatible with the Micro Channel bus specification. It features support for 2 DMA channels with on-chip arbitration, shared local memory arbitration with the peripheral, a programmable wait state generator, as well as an on-chip timer. The MCI94C18 also provides a very flexible interrupt interface to the peripheral. Evaluation boards are available now.

The Complete ARCNET® Controller On A Single Chip—SMC's COM90C62.

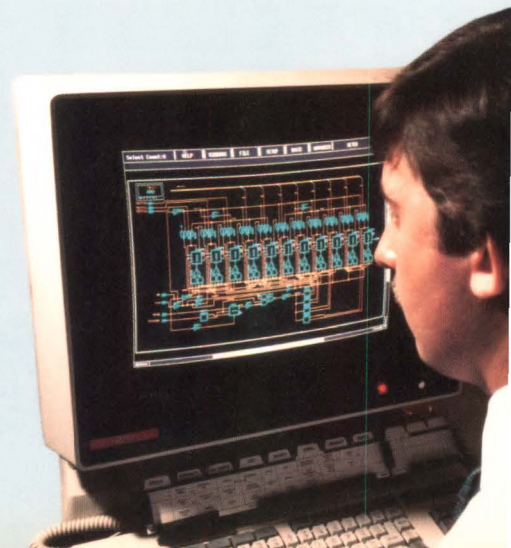
The COM90C62 is the next generation ARCNET local area network controller. SMC's ARCNET, a defacto standard with an installed base of over a half-million nodes, has earned PC Magazine Editor's Choice Award for its high throughput, deterministic access and simple installation. Combining the functions of the COM90C26, COM90C32, and a crystal



oscillator, this highly integrated IC contains all the logic necessary to control a token-passing ARCNET interface across standard coax, twisted pair or fiber optic cable. The COM90C62's high level of integration allows inclusion of a LAN interface directly on a PC mother board.

The Logical Choice For An ATLC (Advanced Terminal Logic Controller)—SMC's CRT92C07.

The CRT92C07 is a fully integrated CRT/attributes controller allowing implementation of VT220/320 terminals with less than 10 ICs. It features a 42 MHz video shift register, 80/132 column capability, a fully register programmable format and a writeable character font. The CRT92C07 can create multiple horizontal split screens capable of being smooth scrolled independently.



F ASIC EXPERTISE F YOUR SUCCESS.

What's An SMC SuperCell?

Its foundation is the proven architecture of an existing SMC ASIC. Its agenda is the customization of capabilities to fulfill specifically defined application and performance objectives. Its methodology is a synergistic development process involving both user and SMC engineers. Its results are dramatically decreased developmental costs, reduced board space and a significantly accelerated production schedule. And we process our 2-micron SuperCell products with epitaxial silicon for greater latch-up resistance. It's SuperCell—another unique way SMC can meet your IC needs. Here are some examples:

Tune Into Expandable Micro Channel Capabilities—SMC's SuperCell MCI94C18.

Building on the MCI94C18 Bus Interface Adapter's capabilities (see above), a designer can integrate additional functions to enhance a specific component's performance. Yet, it is all achieved with a single, board-space-reducing, chip.

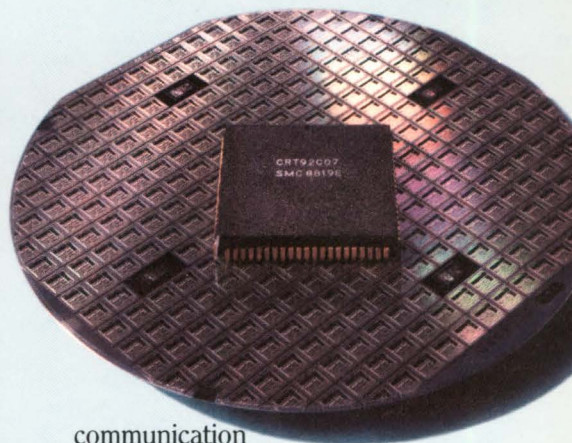
Two Ways To Customize Solutions In IBM Connectivity— SMC's SuperCell COM9064 And SuperCell COM52C50 (Twinax)

Our two popular IBM network controllers are now available as modular designs (SuperCell) for your specific adaptations. The COM9064 SuperCell is an MOS/LSI circuit used to facilitate high speed data transmission. It can implement an interface between IBM 3274/3276 compatible control units and 3278/3287/3289 compatible terminal units. Receiver and transmitter sections may be used

independently of each other. With the COM52C50 Twinax SuperCell, communications interface to an IBM 5250 Twinaxial Bus can be combined with additional functions for connection to IBM's System 36 and 38 or to IBM's new Application System/400 Silverlake family.

Ace Design Problems With Our Asynchronous Communications Element (ACE)— SMC's SuperCell 82C50

The SuperCell ACE is ideal for integration within complex



communication controller ASICs. Its soft-macro architecture can be modified for specific applications, with circuit features added or deleted as required.

Start With Six Storage μ -Controller Access Subfunctions In One IC And Build From There— SMC's MSD95C02 (SunDAe)

Create a proprietary device from what is already the next generation of intelligent programmable storage controllers for direct access and serial access devices. Composed of six peripheral controller subfunction SuperCells—Microsequencer, DMA Controller, ECC Generator/Checker and Processor, Disk and Host Interfaces—the MSD95C02 can be modified or interchanged with other SuperCell modules to increase functionality. This allows you to include proprietary circuitry for product differentiation and cost effectiveness.



STANDARD MICROSYSTEMS CORPORATION

35 Marcus Blvd., Hauppauge, NY 11788

Yes, I'd like to know more.

Please send me your Data Sheet on: _____

Please send me your most recent Short Form Product Catalog.

NAME _____

TITLE _____

COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP _____

SMC™ is a registered trademark; SunDAe™ and SuperCell™ are trademarks of Standard Microsystems Corporation. ARCNET™ is a registered trademark of Datapoint Corp.; IBM™ is a registered trademark; Micro Channel™ is a trademark of International Business Machines Corporation.

THE SECRET OF SMC'S SUCCESS.

From our first ASIC design-win in 1971 to our latest solutions for tomorrow's demands, SMC has consistently been the source for microperipheral innovations in the fields of mass storage, data communications and display control.

Our strong leadership presence in the marketplace is backed by a unique combination of technological expertise and a keen awareness of our customer's needs. Because we maintain and control our own New York-based 2-micron wafer fabrication facility, we can tightly monitor our products from design through final silicon—assuring you a quality product.

SMC's global acceptance is substantiated by our worldwide field sales and applications offices, and guaranteed by our multi-corporation patent/cross licensing agreements.

Today's devices are shrinking in size, while increasing in functionality and sophistication. Specifying SMC ASICs and SuperCells in your designs virtually ensures they'll be around—and relevant—for a long time to come.

With SMC's products working for you...your products will be on the leading edge of technology.

STANDARD MICROSYSTEMS CORPORATION

35 Marcus Blvd., Hauppauge, NY 11788
(516) 273-3100



NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 536 SMITHTOWN, N.Y.

Postage will be paid by addressee

Standard Microsystems Corporation
Department CD
35 Marcus Boulevard
Hauppauge, NY 11788



INTEGRATED CIRCUITS

Chip set tackles laptop design issues, offers flat-panel VGA control

Tom Williams, Western Managing Editor

Declaring laptop computer systems as "the wave of the future," Chips and Technologies (San Jose, CA) has developed a core logic chip set specially tailored to laptop computers' needs for power savings, tight integration and design flexibility. Called Leap (for Low-Power, Enhanced AT Portable), the chip set is accompanied by a single-chip flat-panel Video Graphics Array (VGA) graphics display controller. The chips are designed to provide the basis for systems built around the Intel 80286 at 12, 16 and 20 MHz, and around the 80386SX at 16 or 20 MHz. The 80386SX, a full 32-bit 80386 that uses a 16-bit external bus, allows considerable interconnect and board space savings in portable systems.

Chips and Technologies designed the Leap chip set with the assumption that the distinction between desktop and laptop systems will blur in terms of functionality. "In order for laptop systems to really take off, there will have to be a lot of the desktop features embedded that you can take with you," says Ahmet Alpdemir, systems logic product manager. In addition, customers are demanding other features—such as security, power savings and the ability to interface to ROM cartridges—that are unique to laptops.

The Leap chip set, also designated the CS8223 chip set, consists of a bus and memory controller, an address/data buffer chip with bus conversion logic, an 82C206 integrated peripheral chip, an 82C636 power control unit, an 82C609 multifunction controller/data separator and an 82C455 VGA/LCD controller.

Many of Leap's features are programmable—and these are the ones that OEM system designers will use to make cost/performance trade-off decisions and to customize designs. One of the main avenues for product differentiation, according to Alpdemir, will be by means of the basic I/O system (BIOS). "Every mother board is going to be different from OEM to OEM," he says. An OEM

system designer may decide, for instance, to program in different wait states based on the selected memory speed, or he may want even more security features than are already implemented by the chip set. Or the designer may choose to give the user control over setting certain para-



The Leap chip set was designed around the need to embed desktop features into laptops, according to Ahmet Alpdemir, Chips and Technologies systems logic product manager (left). By pairing Leap with a single-chip flat-panel VGA display controller, the company offers the first controller chip with VGA support for LCD, plasma, EL and CRT displays, according to Keith Angelo, product manager of graphics operations (right).

meters, such as the time-out for shutting down a power-hungry device to save the battery.

The Leap chip set provides the option to support the BIOS in either 8-bit-wide EPROM or 16-bit-wide double EPROMs. Since executing the BIOS from EPROM may be considered too slow for many systems, the

chip set provides a shadow RAM capability, which lets the BIOS be loaded into system RAM from the EPROM on boot-up. The BIOS is then executed from the faster system RAM. The designer also has the option of storing system and display BIOS in the same EPROM.

■ Meeting needs of laptop users

Since laptops contain sensitive information, users want them made safe from unauthorized access. Chips and Technologies dealt with the security issue by building in an interface to EEPROM that allows storage of two passwords. The user enters one of the passwords, and the factory preprograms the other. The preprogrammed password overrides the user password; therefore, a user who forgets his or her password can take the machine back to the dealer to regain access to it.

Users also want a laptop that can run on battery for eight to 10 hours, according to Alpdemir. Power-saving features of the Leap chip set concentrate on two main areas: shutting or slowing down the CPU clock, and monitoring peripherals that consume large amounts of power and shutting them down if no activity is detected in a given time period. For the 80C286, the 82C241 system controller provides a sleep mode that stops the CPU clock while the application is waiting for an external event. While the system is in sleep mode, interrupts are still processed normally. Each time an interrupt is serviced, the sleep mode checks to see if some specified event has occurred. If it has, the application takes over; if not, the system goes back to sleep.

For CMOS processors that can't be completely shut down, their operating frequency can be slowed down to one-sixteenth the operating frequency of the processor clock. This can be combined with the use of slow-refresh dynamic RAMs, for which the refresh cycle can be expanded from 4 to 64 ms for added power savings.

Slow-refresh DRAMs come into play when using the Leap suspend/resume capability. The designer can configure a BIOS to set the machine into standby mode when the power is turned off. In standby mode, operation is suspended and the contents of registers are saved either to battery-

INTEGRATED CIRCUITS

backed CMOS RAM or to disk—again at the designer's option. Battery-backed slow-refresh DRAMs can be used to keep the application alive while consuming less power. When power is turned on, the contents of the machine's registers are restored to the CPU and configuration registers, and the application resumes.

One big consumer of power in any system is the disk drive. Several peripheral manufacturers, seeing the potential in the laptop market, are designing devices with power moni-

set by the OEM in the BIOS, and/or a range of time-out options can be made available to the user.

The advent of ROM cards and modules that can be plugged in or removed by the user has made customizing systems and applications easy and affordable and is a natural for laptops. "All of our customers asked for direct access to ROM modules," says Alpdemir. ROM modules can come in many forms, such as chips that plug into the mother board, or as credit card-sized modules such as the

num multitasking of the kind that will be required to support OS/2, at least 64 registers are needed.

Flat-panel VGA control

Probably the biggest barrier to a wide acceptance of laptop computers is the quality of their displays. While there have been steady improvements in readability, until now there hasn't been a large-format LCD display that's truly readable in a wide range of viewing angles and lighting conditions.

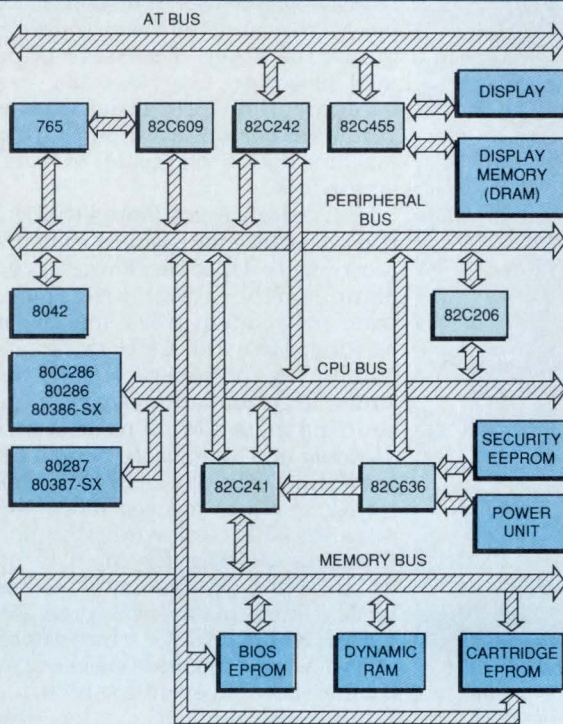
This year, however, all the major Japanese LCD manufacturers will be presenting neutralized twisted nematic (NTN) displays that will finally have "page white" display quality. And they'll be capable of up to 16 levels of gray scale and will have a screen resolution of 640x480 pixels, making them compatible with the VGA standard from IBM.

"What we're seeing is the confluence of increasing display resolution coinciding with the software standard," says Keith Angelo, product manager of graphics operations at Chips and Technologies. The company claims that the pairing of the 82C455 flat-panel VGA controller with the Leap chip set creates the first controller chip to offer VGA support for LCD, plasma, electroluminescent and CRT displays.

Since even the NTN LCD displays are monochrome, the chip must be able to map the 16 gray-scale levels of an NTN panel to the 16 colors specified by VGA. This is done by an on-chip algorithm called Smartmap that ensures a minimum user-selectable contrast between any adjacent gray scales on the screen. Thus, no matter how the initial gray-level-to-color map is set up, the actual display will be automatically adjusted so that it's readable.

Chips and Technologies' goal in developing the Leap chip set, according to Alpdemir, was to offer OEMs a wide range of possibilities for configuring systems and targeting price/performance levels and options using a common silicon platform. Although a great deal of this will be done in hardware, an even greater degree of product differentiation will probably come through innovations in the BIOS that will take advantage of Leap's programmable options. □

LEAP-BASED LAPTOP SYSTEM



Chips and Technologies' Leap chip set is helping create a new generation of true laptops that are small, power-saving and highly functional. The chip set integrates CPU, AT bus control functions, memory control logic and specific laptop features into six VLSI CMOS devices.

toring and conservation features. The 3½-in. CP-3022 20-Mbyte Winchester drive from Conner Peripherals (San Jose, CA), for example, can be programmed to shut down the spindle motor and put its electronics into a sleep mode if it hasn't been accessed in a certain amount of time. The 82C636 power monitor chip, however, has been designed to monitor the operation of disk drives and other power-hungry devices—especially backlit LCD displays—in the system and shut them down after a predetermined time-out. Here again, time-outs for certain devices can be

Melcard from Mitsubishi (Tokyo, Japan) or the Star Card offered by ITT Cannon (Fountain Valley, CA). Accordingly, Chips and Technologies has provided the ability to directly access ROM cartridge address space through extended memory specification (EMS) page registers.

The Leap control logic supports EMS 4.0 with four 1-Mbyte on-chip page registers, and Chips and Technologies also supplies a software driver to use the extended memory option to accommodate ROM modules or system memory beyond the 640-kbyte DOS limit. But for opti-

DSP-based microcontrollers blaze new trails into real-time computing

Warren Andrews, Contributing Editor

The traditional role of the microcontroller is changing from performing relatively slow, stand-alone functions to handling high-speed, real-time, or close-to-real-time activities. And while semiconductor manufacturers are scrambling to boost the performance and bus width of more conventional controllers, industry demands—particularly in terms of algorithm complexity—are outstripping their efforts. In response, a new breed of microcontroller is emerging that's replacing the conventional processor core with a high-performance digital signal processor. And while such parts may take sockets from traditional microcontrollers, their speed and flexibility will undoubtedly let them replace analog subsystems as well as unearth entirely new applications.

The first of this new-generation device comes from Microchip Technol-

ogy (Chandler, AZ), the wholly owned spin-off of General Instrument's semiconductor group (Hicksville, NY). The chip was designed by Microchip under a license from Texas Instruments (Houston, TX) and is being manufactured and marketed by both companies. The DSC320C14 is a single-chip device in which the core of a TI 320C10 DSP is surrounded with I/O and peripheral circuits. The new controller offers a 160-ns instruction time that, when combined with its ability to execute multiplication operations in one instruction cycle, results in a peak performance of 6.4 Mips—five to 10 times that of conventional 16-bit microcontrollers.

The new architecture represents a revolutionary change in the way engineers look at control functions—many of whom continue to use analog circuitry because the DSP horsepower hasn't been available, accord-

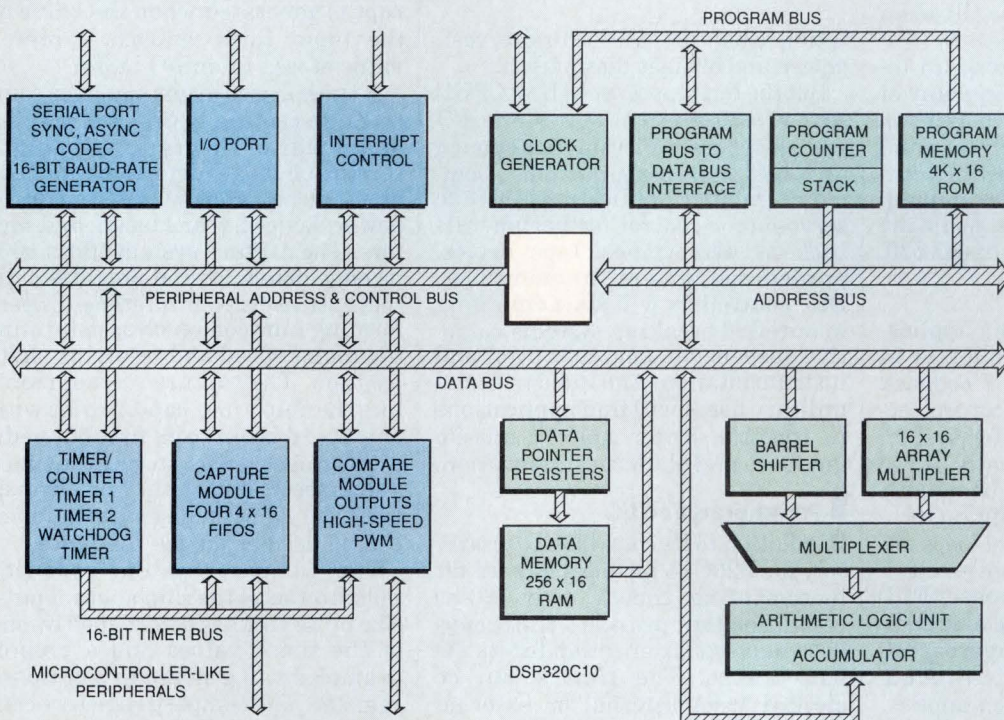
ing to Rahul Sud, vice-president of marketing for Microchip. Because the 320C14 can execute single-cycle multiplications, it can perform many advanced control algorithms, such as adaptive control, Kalman filtering and those for state controllers in real time, says Ajay Padgaonkar, design engineering manager.

Other DSP makers follow suit

Though the Microchip/TI DSP controller is the first of its kind to hit the market, expect to see a host of similar products surface in coming months. Fujitsu Microelectronics (Santa Clara, CA), for example, recently introduced a 24-bit floating-point DSP chip aimed at cost-sensitive applications. Fujitsu is positioning the device as a DSP microcontroller even though it lacks most of the peripheral and I/O functions of the 320C14, according to John Reimer, the company's manager of microcomputer and communications products.

Because the company positions the chip as a controller, Reimer hopes that designers will begin to consider using DSPs rather than more conventional microcontrollers such as

THE DSC320C14 ARCHITECTURE



Microchip Technology's 320C14 single-chip digital signal processor controller includes a TI 320C10 core DSP and a number of I/O and peripheral functions. These include 16 bidirectional I/O ports; four 16-bit incrementing timers; a capture module including four 4-x16-bit first-in, first-outs; a compare module with six pulse-width modulation output channels; a serial port that operates either synchronously or asynchronously and offers a codec (coder-decoder) mode to support standard digital telephone rates; and an interrupt controller.

INTEGRATED CIRCUITS

the 80196 from Intel (Folsom, CA) or the HDC 1600 from National Semiconductor (Santa Clara, CA). In addition, many forthcoming applications will require customized versions of DSP products, according to Reimer. "It's easy to add some timers, I/O and other peripheral functions to the basic chip for custom applications," he says. "We've already developed some customized versions for low-end applications."

Similarly, other DSP makers may soon be looking to jump on the microcontroller bandwagon. Analog Devices (Norwood, MA) has taken a step in that direction by including some additional on-chip memory in its ADSP 2101/2102 high-end, floating-point DSP. But Analog Devices will probably continue to look at integrating more functions that will appeal to high-end applications.

Like TI, Motorola (Phoenix, AZ) has a heavy investment in the microcontroller area and also offers DSP devices. But the company's microcontroller and DSP groups are making no comment at this time. Oki Semiconductor (Sunnyvale, CA) and NEC (Mountain View, CA) have an interest in both the microcontroller and DSP camps, but if they have any plans, they're not discussing them.

DSP chips have traditionally been relatively expensive. In the new DSP controllers, cost will become an increasingly critical factor in many of the target applications, such as in automobiles, disk drives, printers and consumer products. Microchip's controller is expected to sell for well under \$10 in OEM quantities, while the Fujitsu device will sell for under \$30.

■ Closed-loop control

One of the more promising applications for the DSP controller is in closed-loop control, where a feedback loop is used to improve control accuracy by compensating for system characteristics. Traditionally, these compensation loops have been built using analog circuitry. If digital techniques are used, the control loops are generally implemented using second-order finite impulse response (FIR) and infinite impulse response (IIR) filters. These digital approaches bring higher reliability, noise immunity and flexibility to such applications. But these complex digital

filters require computationally intensive sum-of-products calculations and traditionally have been poor performers, too expensive, or both.

Conventional microcontrollers lack the hardware arithmetic capability and are unable to compute such filter algorithms in anywhere near real time. Instead, they rely on approximate values obtained by accessing lookup tables, which results in an inflexible system that often lacks the necessary accuracy. DSP chips have the computational capability but, until now, have lacked the I/O and peripheral functionality for cost-effective implementation. Systems built from conventional single-chip DSPs are burdened with so much extra glue logic that their implemen-

The combination of a DSP CPU's power with a microcontroller's I/O and peripheral functions has opened up a host of new applications.



tation is impractical due to size, cost, power and/or heat dissipation.

But the combination of a DSP CPU's power with a microcontroller's I/O and peripheral functions has opened up a host of new applications. Common computer applications include servo-motor control for peripherals such as disk drives, tape drives, printers and plotters. In automobiles, DSP controllers will start emerging in antiskid breaking systems, adaptive suspension, engine control and instrumentation. And industrial and military users will find applications in robotics, motor control, missile guidance and platform stabilization.

■ Peripherals and I/O

In addition to its core 320C10 processor, the 320C14 includes four 16-bit incrementing timers with 160-ns resolution that provide a time reference and synchronization for its I/O subsystems. The timers can be clocked from internal or external sources and are driven by program-

mable prescalers to divide the clock by 1, 4 or 16. Included are a watchdog timer with programmable time-out; a pair of general-purpose timers that can be configured to produce one 40-bit timer with a resolution of 160 ns and a maximum duration to two days; and a baud-rate generator.

The watchdog timer provides a number of functions. To prevent accidental resetting of the timer, it's nonwritable. To assure glitch-free operation, the programmable time-out period is stored in a double-buffered period register, and to simplify the creation of an independent "warm restart" mechanism, the timer makes its overflow signal available on one of the chip's pins, which can also be tied directly to the reset input.

Direct control over external actuators such as valves, relays and indicators is managed by the 320C14's 16 software-configurable latched I/O lines. A data-direction register determines whether a given line is used as an input or output. A second 16-bit register stores the status of each line. Individual bits can be set or reset using bit-set or bit-clear functions without having to use read-modify-write operations. In addition, the input lines can be grouped so that an interrupt is generated when the value of the input lines matches a preset value stored in an I/O buffer.

A timer-based event manager comprising a capture system, comparator and a pair of timers handles high-resolution edge detection and enables direct, continuous control of power devices, transducers and motors. The capture system offers 160-ns edge detection and provides a direct optical encoder interface for performing functions such as determining motor speed and resolving shaft position. The capture system monitors the chip's four capture pins with one 4- \times 16-bit first-in, first-out dedicated to each pin for storing the timer value associated with a pin transition. The event manager's two timers can be used as a time reference.

The compare system produces pulses on six of the chip's output pins. The pulse width is determined by one of the timer values and a preprogrammed value stored in a compare register. The compare registers constantly compare their value with the



"We should have used Hitachi Drives."

The meeting that should never have happened.

When a disk drive crashes, you're in trouble. To an irate customer, it doesn't matter that you purchased the drive from someone else. *Your* logo is on the system.

This means you need a disk drive supplier who is also a partner... a company who understands what it's like to compete in today's tough computer systems marketplaces. That company is Hitachi.

An intimate knowledge of the disk drive business.

When you decide to do business with Hitachi, you get more than just a high quality, incredibly reliable disk drive. You also get the support, resources, and expertise of a \$40 billion dollar company who's one of the largest OEM computer systems manufacturers in the world. We use disk drives in our own systems, and risk losing customers if drives fail. Just like you.

This means we know what it takes to make the best. We design and build our own motors, heads, microprocessors, and custom LSIs to our own stringent specs—all checked by the most stringent Quality Assurance program in the industry.

We have over 1,500 engineers who work on nothing but disk drives. They're supported by nearly two decades of

experience manufacturing disk drives, and over 16,000 employees in R&D throughout the company.

A serious commitment to the disk drive business.

Hitachi continues to advance storage technology, through the ongoing development and manufacturing of new 5.25," 8," and 8.8" Winchester, magnetic tape subsystems and ultra-high density optical disk subsystems. We plan on being in this business for a long time... making sure your customers call with orders, not complaints. Next time, specify Hitachi.

Fast Action: To get information or product literature immediately, CALL TOLL FREE 1-800-538-8157, Ext. 877. In California, 1-800-672-3470, Ext. 877. Ask for literature number APB-002.

Regional Sales Offices: Waltham, MA 617/890-0804, Dallas, TX 214/991-7983, Brea, CA 714/993-1610, San Bruno, CA 415/872-1902.



Hitachi offers a complete line of Winchester, magnetic tape, and optical storage products with speeds, capacities and interfaces for virtually any application.

Hitachi America, Ltd.
Computer Division
950 Elm Avenue, Suite 100
San Bruno, CA 94066

See Us at Comdex Booth #1258



CIRCLE NO. 10

INTEGRATED CIRCUITS

timer value and hold data until it's rewritten with a different value. When the value in a compare register matches the timer, the compare subsystem generates a pulse and feeds it to a set of six action registers. Bits in the action registers determine if the compare pulses will set, reset or toggle the compare pin, or generate compare interrupts.

The compare system's six outputs can be converted to high-speed pulse-width modulation outputs by setting

a control bit. The outputs produce pulses as small as 40 ns at a frequency of up to 3 MHz, thus providing a 10-bit resolution at 25 kHz or 8-bit resolution at 100 kHz.

The future of DSP controllers

Looking a step or so ahead, it seems natural evolution for DSP cores to become cells in many semicustom vendors' libraries, just as the 6502, COPS800, 8051 and other microcontroller architectures have been

merged into cell libraries. At least for this generation and maybe the next, however, this may not prove to be a practical solution because of the die area occupied by the DSP function. The DSP function measures about 110 mils on a side—considerably larger than most conventional library cells. But with rapidly shrinking geometries and process refinements, the DSP core's size may cease to be an obstacle to its semicustom status. □

SOFTWARE

Unix gains edge over OS/2 by running DOS applications

Tom Williams, Western Managing Editor

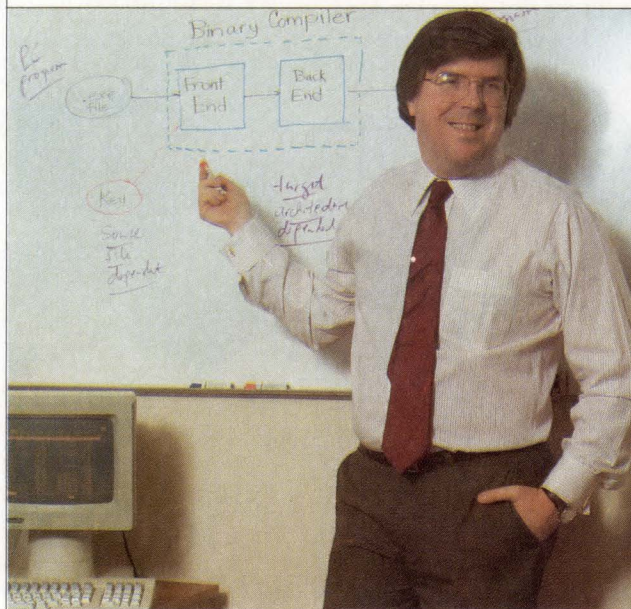
The race is on between Unix and OS/2, and Unix has a head start. Why? As OS/2 and Unix start to compete side by side for acceptance in the commercial, business sector, Unix stands ready at the starting gate with a rich multitask environment and established applications. And now, Unix is gaining an extra boost as the capability emerges to easily run DOS applications from a Unix environment on a wide variety of hardware platforms. In addition, Unix may pull a clear distance ahead of OS/2 with the added push from recent developments aimed at improving the user interface via the X Window standard, combined with the efforts of the Open Software Foundation (OSF) to provide a common operating environment spanning many major hardware vendors.

Unix will likely move from its traditionally perceived role as an operating system for engineers and scientists into a new role as an operating system for the business environment that can support single- and multiuser productivity applications. And that's precisely the environment for which OS/2 has been targeted. This migration of Unix into the office will become possible when and if a commonly understood user interface emerges to shield the nontechnical user from having to deal directly with the actual workings of the operating system.

Although Unix hasn't yet achieved an acceptable level of user comfort, it still has a leg up over the yet-to-be-fully-real OS/2: there's a larger number of applications than currently exist for OS/2, and now with the ability to run existing DOS applications from a Unix environment, that advantage will take a quantum leap. Efforts to provide access to DOS applications from the Unix environment have been spurred by the emergence of workstations based on high-performance, 20- to 25-MHz versions

of the Intel 80386 32-bit CPU. Such workstations are in a performance class with Motorola 68000-based workstations running Unix that are now used for CAE/CAD/CAM and scientific work.

The 80386 also brings a link into a universe of applications that have become widely accepted in the business community. What has heretofore been lacking, however, is an operating system that can fully utilize the 80386's potential. What users have really needed—and what DOS doesn't provide—is a truly multitasking operating system that can directly address large memory arrays. But at the same time, users also need access to the vast number of quality application programs and the civilized user interface they have come to ex-



"The last thing a software vendor wants is to have his 'pride and joy' run in Unix and run terribly," says Colin Hunter, president of Hunter Systems. To ease the translation of DOS programs so that they run efficiently under Unix, Hunter Systems has developed a set of tools for both software vendors and hardware OEMs.

SOFTWARE

pect under DOS.

The development of OS/2 was ostensibly aimed at that goal. But with OS/2 lagging and genuine standards efforts afoot in the Unix community, software developers are taking a wait-and-see attitude before investing in developing OS/2 applications. Meanwhile, some companies have developed ways to bring existing DOS applications into the Unix environment, thus making Unix an even more attractive option as a powerful, multitasking operating system.

■ Bringing DOS into the fold

There are basically two ways to get applications written for DOS to run under Unix: emulate a DOS environment under Unix and run the applications unmodified, or translate each program so that it runs efficiently in the Unix milieu. Both of these approaches are being pursued. Insignia Solutions (Sunnyvale, CA) and The Santa Cruz Operation (Santa Cruz, CA) are taking different tacks at emulating a DOS environment, while Hunter Systems (Mountain View, CA) has developed a set of tools to ease the task of translating DOS programs to run like "well-behaved" Unix applications.

Insignia Solutions has created a complete software emulation of a PC. Called SoftPC, it's "a total emulation of a PC, including 8088, peripheral chips, DMA, timers and graphics," according to Henry Nash, vice-president of engineering. Versions of SoftPC are available for the 68000 family, MIPS Computer Systems' reduced-instruction-set processors, the Motorola 88000, and the Intergraph Clipper processor. SoftPC is also available for manufacturers to bundle with their systems.

A similar approach is used by The Santa Cruz Operation (SCO) with its VP/ix product, which runs under the company's Xenix version of Unix on the 80386. VP/ix is limited to the 80386 because it takes advantage of the 80386's ability to support a mode that will run a hardware version of the 8088 instruction set. So VP/ix supports an emulation of the PC DOS environment under Unix but, unlike SoftPC, doesn't have to emulate the instruction set. VP/ix, however, doesn't have SoftPC's portability to other processors. Both SoftPC and

VP/ix can share files with Unix.

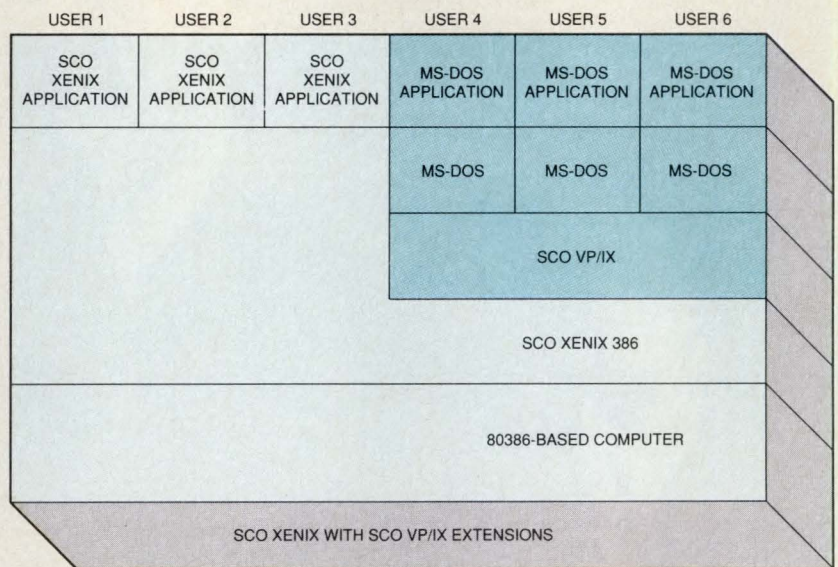
Emulating an entire machine's logic as well as an operating system requires a certain amount of overhead. And in a multiuser environment, each user running a DOS application has his or her own DOS machine emulation. Nash estimates that a SoftPC emulation requires about 1 Mbyte of memory plus 640 kbytes for the DOS system memory.

get close to the performance of an AT." In addition, he says, as code is refined and made more efficient, performance will improve.

■ Easing the translation task

"The last thing a software vendor wants is to have his 'pride and joy' run in Unix and run terribly," says Colin Hunter, president of Hunter Systems. "Most DOS software ven-

SCO XENIX WITH VP/IX EXTENSION



The Santa Cruz Operation's solution to emulating a DOS environment under Unix, VP/ix runs under the company's Xenix version of Unix and uses the 80386's support of the 8088 instruction set to set up multiple virtual DOS environments. Users can load and run DOS applications without modification, but can also share DOS and Xenix data files.

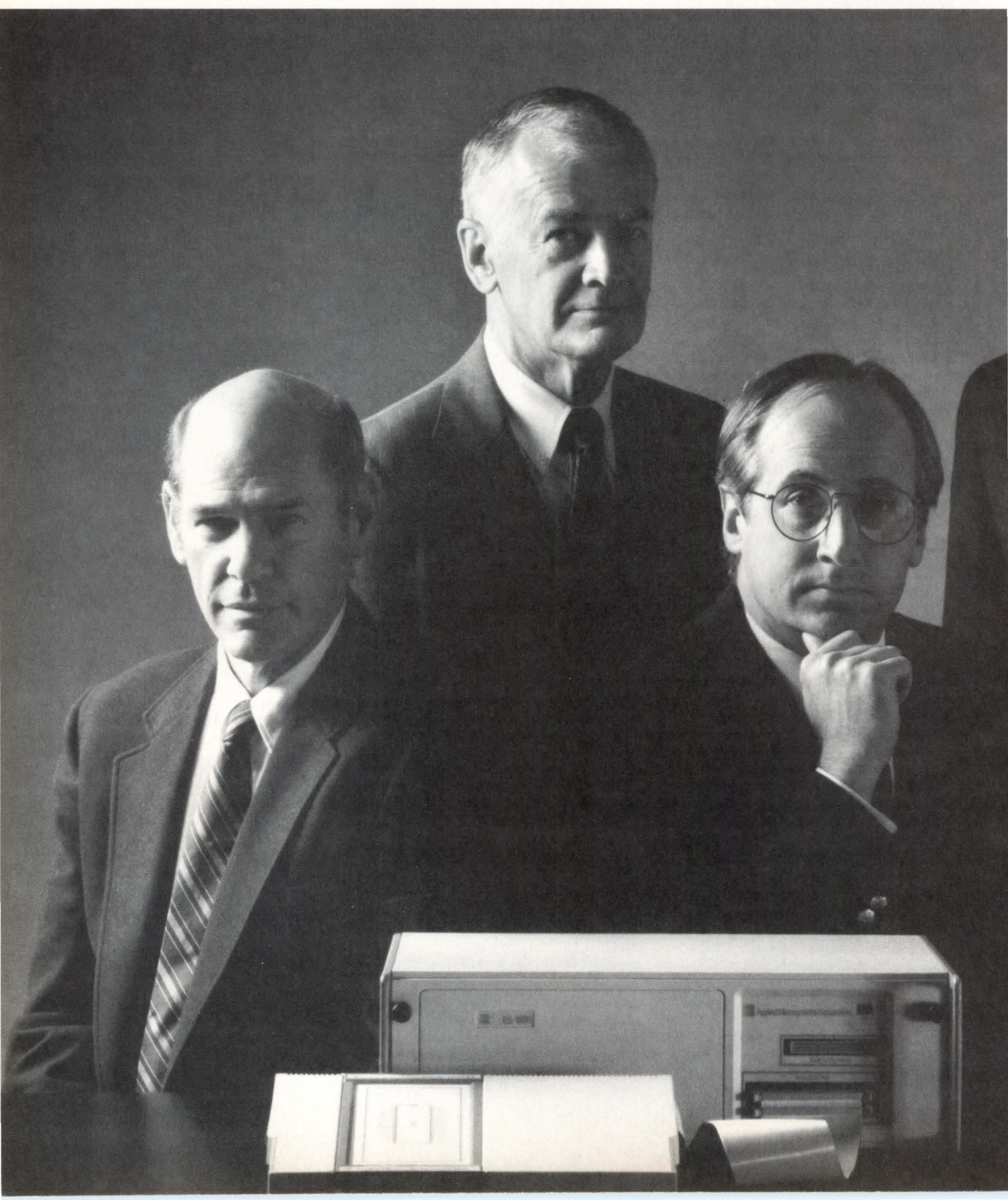
SCO's approach requires somewhat less memory because the instruction set is in hardware and, therefore, SCO doesn't have to emulate the machine instructions in software.

The performance of VP/ix is tied directly to the speed of the 80386 processor being used. For SoftPC, performance is also tied to the processor, but will vary greatly depending on the particular processor, architecture and the number of users and/or tasks on a multiuser system. A single-user 68020 running at 16 MHz, for example, will yield a SoftPC performance roughly equivalent to that of a basic IBM PC XT, according to Insignia's Nash. With higher performance systems, he says, "You can

dors have competitors that already run under Unix." This concern led Hunter Systems to develop a set of tools that will help the software developer get popular DOS applications to easily run under Unix—and to run at the performance levels expected by users of Unix workstations. Hunter stresses that it isn't DOS that a user is interested in, but rather the functionality of the DOS applications. It's the job of the system integrator to provide that functionality.

Hunter Systems provides two tools—a global analyzer primarily for use by software vendors and a binary compiler primarily targeted at hardware OEMs—both under the name of XDOS. The binary compiler consists

THE NIT PIC



PICKER'S PICK.



Many of the world's most demanding engineers are already sold on the ES-1800 microprocessor development system from Applied Microsystems.

Because it's the only closely coupled system that includes emulators, debuggers, SCSI, two megabytes of overlay memory and transparency at operational speeds.

And because we've kept it state-of-the-art by constantly expanding and upgrading the system.

Now the ES-1800 supports most every popular processor, including 68020 at 25 MHz, 80C186 at 16.0 MHz and 68000 at 16.7 MHz. As a result, you don't need to replace your development system every time you select a new microprocessor.

There just isn't a more comprehensive, effective, efficient or experienced development system around. Not Intel ICE. Not Hewlett Packard.

Nearly 10,000 units out there continue to debug embedded systems more reliably than any of the others. By doing more. Faster, easier and more accurately. After all, thousands of nit pickers can't be wrong.

For a demonstration, write Applied Microsystems Corporation, P.O. Box 97002, Redmond, Washington, USA 98073-9702. Or call (800) 426-3925, in WA call (206) 882-2000.



Applied
Microsystems
Corporation

CIRCLE NO. 11

SOFTWARE

of a front-end that reads an executable DOS program—directly as supplied by the manufacturer—and a back-end that generates instructions for the target processor. The resulting code is then linked to a run-time package to run under Unix. Thus, the user doesn't need access to source code to perform the translation.

The front-end of the binary compiler reads the DOS program and a .KEY file that has been generated by the global analyzer. The .KEY file contains information needed by the compiler to help it regenerate the application in a form that will make it run efficiently under Unix. The .KEY file contains a complete analysis of the program, including flow graphs, information on registers and flags needed by the XDOS compiler.

In the course of generating the .KEY file, the analyzer may encounter sections of code it can't handle automatically. Anomalies may include sections of code that alter themselves or I/O routines that aren't efficient in a Unix environment. In the case of such ambiguous code, an engineer is needed to interactively input data to complete the .KEY file.

One example cited by Hunter where an interactive input would be useful is in a keyboard input routine. Many DOS programs are written for single-user, single-task machines. Thus, a program might go into a tight loop, polling the keyboard and looking for character input. In a multitasking, multiuser system, this represents a waste of CPU resources. A keyboard interrupt routine is more appropriate, because it simply waits

for an interrupt to tell it that it has input rather than tying up the CPU.

Hunter Systems' strategy is to make the analyzer portion of XDOS primarily available to software manufacturers. They could then produce .KEY files to go with the Unix versions of their DOS software products. The binary compiler would mainly be used by hardware OEMs to bundle with their systems.

Dealing with graphics

Lest the situation sound too rosy, none of the three companies mentioned has come up with a totally satisfactory way to transform the IBM standard graphics operations into something that looks like the DOS application's graphics output on the myriad of display devices used by Unix-based systems—including dumb terminals. The reason is that graphics and user interface standards in the Unix world are still in a state of flux.

Of the three products, Insignia's SoftPC comes the closest to "DOS-like" graphics because the PC emulation also emulates the graphics silicon. The present graphics emulation is limited to the Color Graphics Adapter hardware, which has a resolution of only 320x200 pixels, but emulations are in the works for emulation of the Enhanced Graphics Adapter (EGA) with 640x350 pixels and the Video Graphics Array (VGA) at 640x480 pixels. The output of the SoftPC graphics emulation must, of course, then be adapted to whatever Unix drivers and display hardware are being used on the target system.

Insignia also has a standard X Window version 11 implementation of SoftPC for Unix machines that standardize on the X Window system.

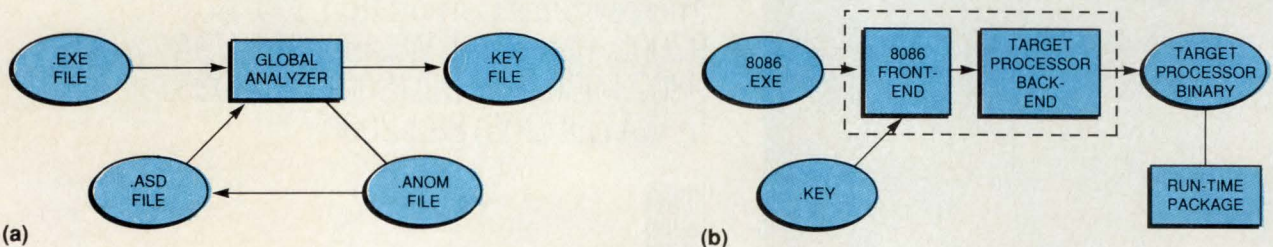
DOS graphics output from a VP/ix has an advantage in that many 80386-based systems use IBM-type graphics controllers—primarily EGA and VGA—and therefore can handle the graphics directly. Since VP/ix isn't specific only to the 80386, but also to Xenix, DOS graphics output can run in full-screen mode in SCO's Xenix window environment.

XDOS comes in two versions: a "vanilla" character mode version and a graphics-oriented version. Porting the graphics version requires more effort, and the hardware integrator must pay attention to all the details of a given display environment to be able to adapt it. Hunter says he is encouraged, however, by the growing popularity of window-oriented user interface systems, both in the DOS and in the Unix worlds. "We can easily map a Microsoft Windows application onto X Window," Hunter says.

Given the fact that Unix appears to be getting its act together, proponents of Unix as an alternative to OS/2 have been becoming bolder in their pronouncements. Not least among these are the suppliers of bridges to DOS applications.

What if one should be tempted to ask the heretical question, Does the world even need OS/2? "That's a good question," says Insignia's Nash. "We're taking a wait-and-see attitude." Hunter Systems' Hunter is more definite. His answer: "No." □

HUNTER SYSTEMS' XDOS SYSTEM



A global analyzer and a binary compiler are the two major components of Hunter Systems' XDOS system. The global analyzer (a) reads an application .EXE file and generates a .KEY file containing the parameters needed to convert the program structure to work with Unix. Any items the analyzer can't deal with automatically are stored in the .ANOM file. An engineer then resolves those problems and enters any customization input via the .ASD file. The XDOS binary compiler (b) runs on the target hardware. It reads the software vendor's standard .EXE file along with the final version of the .KEY file, and the target processor-specific back-end produces a native binary file that's linked to the target machine's run-time package.

Development tools enhance real-time Ada support

Richard Goering, Senior Editor

Developers of embedded software for military systems have two critical needs—real-time programming support and the Ada programming language. To provide the best of both, Ready Systems (Sunnyvale, CA) this month is introducing a target-environment Ada simulator, a complete Ada operating system, and various Ada-specific enhancements to its Computer Aided Real-Time Development tools (CARDtools).

Of these, the most significant introduction appears to be RTAda-Sim, which Ready Systems claims to be the first run-time Ada simulator. This software simulator lets users test Ada programs written for 68020 targets without having to use an actual target or I/O devices. Available on VAX/VMS and Sun/Unix hosts, RTAda-Sim provides a re-creation of the target environment, simulating the I/O devices, clock, run-time system and operating system.

Of the many existing software simulators, few provide a run-time simulation of target I/O devices. In RTAda-Sim, these devices are described through a simple form that specifies the I/O behavior in terms of direction (input or output), timing and data.

"The real bottom line is that RTAda-Sim lets you run Ada code unchanged," says Rich Blomseth, Ready Systems product manager. To test Ada code on a host today, users normally have to change any code dealing with the target I/O devices. Yet the complexity of I/O is one of the most difficult aspects of real-time programming, and I/O code may be the part of the program that needs testing the most. Simulating the target environment lets this I/O code be tested without modification.

RTAda-Sim includes a source-level debugger that displays the source code, allows breakpoints on the Ada source line and permits single stepping by Ada source statements. The source code displayed and executed by the debugger is the same code that will run on the target system, includ-

ing operating system calls and I/O device handlers. When users are ready to move to the target, they can use Ready Systems' Artscope, a multi-tasking debugger that lets the target system run at full speed.

Building an operating system

RTAda-Sim works with RTAda/OS, an extensible real-time operating system introduced this month by Ready Systems. RTAda/OS includes ARTX, a real-time Ada kernel based on Ready Systems' VRTX kernel. "We added three additional products to build the kernel into a full operating system," explains Blomseth. These modular products include RTAda-I/O, which provides a file system; RTAda-MP, which supports shared-memory multiprocessing; and RTAda-Net, which supports LAN multiprocessing.

"The big deal with RTAda-I/O is that it provides a complete, hierarchical file system for the run-time target," says Blomseth. "Typically you have only a very simple file system for the target." In addition, RTAda-I/O supports disk and stream I/O in the target environment. RTAda-MP supports architectures that plug multiple processors into one

bus, while RTAda-Net provides networking between processors using TCP/IP (Transmission Control Protocol/Internet Protocol).

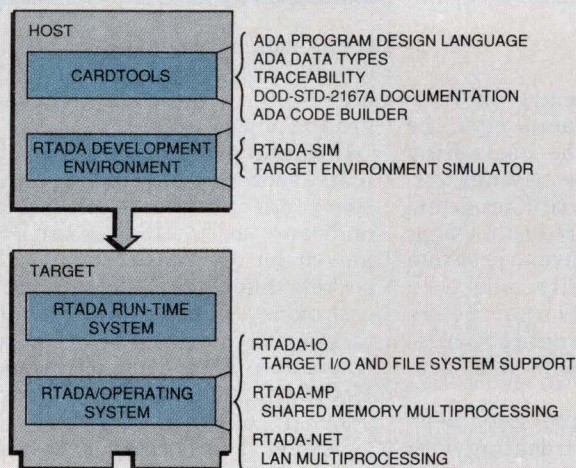
New CARDtools

To round out its offerings, Ready Systems has added several Ada enhancements to its CARDtools, including structured analysis, structured design and real-time performance verification. One addition is an Ada Program Design Language (PDL). The Ada PDL includes Ada-specific keywords and structured support for Ada tasking constructs.

The Ada Code Builder generates Ada code frames from PDL descriptions. A code frame is an Ada package declaration that can be automatically compiled into Ada source code. It includes a header, and procedure and type declarations.

To support the documentation that's required from government contractors, Ready Systems has released a DOD-STD-2167A document generator. This standard, updated from the previous 2167 standard, defines the types of documentation that must be included with embedded software. Ready Systems has also announced a requirements traceability tool that lets users keep track of contractual obligations and ensure that these requirements are met when the software design is complete. The traceability tool also ensures that changes to the design don't violate the original specification. □

SUPPORT FOR REAL-TIME ADA DEVELOPMENT



Ready Systems has enhanced its support for real-time Ada development with a number of capabilities. Areas of enhancement include CARDtools, which provide structured analysis and design; the RTAda development environment, which now provides a target-environment simulator; and RTAda/OS, a new operating system that builds on Ready Systems' ARTX kernel.

Off-the-shelf in-circuit programmers cut costs, ease firmware updates

Richard Goering, Senior Editor

By programming devices such as EPROMs after they're loaded onto printed circuit boards, in-circuit programming tools can save production costs and ease firmware updates. But in-circuit programming is both customized and expensive. And, until now, it has been used almost exclusively in certain high-reliability military applications. This month, however, Data I/O (Redmond, WA) is taking first aim at the commercial marketplace by introducing what it claims to be the industry's first off-the-shelf in-circuit programmer.

The company's Boardsite 4100 and 4400 programmers are portable units hosted by the IBM PC. They include a do-it-yourself interface kit that lets users connect their printed circuit boards to the programmer by constructing a simple wire-wrap board. The Boardsite units also provide software that lets users define a board profile, which describes the printed circuit board's characteristics to the programmer.

A traditional custom-built system, in contrast to a portable unit, includes a physical interface and a board profile that's developed by the programmer vendor. Costs are typically \$40,000 to \$50,000, and a new cost is incurred every time the board is changed. The Boardsite programmers start at \$9,500.

Multiple benefits

In Data I/O's missionary effort to bring in-circuit programming to the commercial world, the big selling point is going to be cost savings during production. In-circuit programming involves fewer production steps because users don't have to program each device individually, label each part, and then store each part before assembly. Instead, the entire board is assembled, and then it's programmed as a unit.

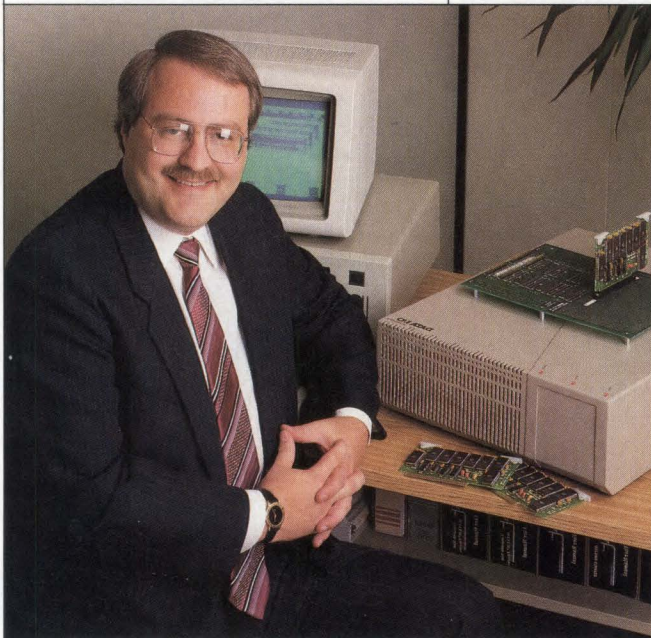
"Not only have some steps been eliminated, but you're dealing with whole boards rather than parts,"

says Randall Lutz, product manager at Data I/O.

In addition, inventory control is simpler with in-circuit programming because it isn't necessary to maintain separate supplies of individually programmed parts. Firmware updates are also much easier because users won't have to remove devices from the board, erase and reprogram each part individually, and load

types of programmable devices or all kinds of designs. It's primarily beneficial for MOS EPROMs and EEPROMs. The Boardsite programmers can support certain other MOS devices as well, such as microprocessors, microcontrollers and programmable logic devices. Bipolar PROMs generally aren't programmed in-circuit because they require that voltages be raised to levels that could possibly damage adjacent TTL circuitry.

In-circuit programming is seldom practical for complex PLDs because it would complicate logic verification. "You can't verify the test vectors very easily unless you've done some fancy footwork in order to get the sig-



The Boardsite programmer from Data I/O is the first off-the-shelf programmer for in-circuit programming. According to product marketing manager Randall Lutz, board manufacturers can save production costs and simplify firmware updates by programming devices such as EPROMs after they're loaded into boards.

them back onto the board. With in-circuit programming, the entire board can be erased and then reprogrammed as a unit.

In-circuit programming also eliminates sockets, which is a big plus for some users. Sockets are often placed on boards so that devices can be removed for firmware updates. But sockets take up real estate, and they cost money. "For example, if you're talking 15 parts to a board, at anywhere from 50¢ to \$1 for a socket, and 10,000 to 20,000 boards a year, it adds up," explains Lutz.

Despite its advantages, in-circuit programming isn't the answer for all

nals back out to the programmer," according to Lutz. Moreover, some PLDs require high voltages on one of the address lines. It's difficult to get that voltage to the device, and TTL devices on the same bus would have to be isolated.

To implement in-circuit programming, designers must avoid mixing devices with different programming algorithms. They must also separate V_{cc} from V_{pp} lines and separate PROM V_{cc} from TTL device V_{cc} when using fast algorithms. In addition, designers have to allow full programmer control over bus, address, data and programming lines.

Placing decoupling capacitors on the V_{cc} and V_{pp} lines is recommended.

■ Creating a board profile

In-circuit programming requires that the designer describe the board's characteristics to the programmer. This is done with a piece of software called the board profile, and in the past it's been created from an assembly language program. The Boardsite programmers let users create a board profile by answering questions in a menu format. Users provide such data as bus width, device architecture, address and data assignments, and types of MOS devices mounted on the board.

Building a physical interface to the board that's being programmed is

"It used to be hard to build an interface, but we put a lot of the logic you need inside the programmer."

—Randall Lutz, Data I/O



much like constructing a simple breadboard. The Boardsite programmers come with a do-it-yourself kit that includes some prepunched boards. "It used to be hard to build an interface, but we put a lot of the logic you need inside the programmer," says Lutz. "Eighty to 90 percent of the applications need only wires and connectors. You don't need to put active components on the interface."

Because Boardsite lets users program several boards simultaneously, it includes isolation circuitry. This buffer circuitry isolates the boards from one another, so that, in the case of a catastrophic failure, only one board will be affected.

The Boardsite 4100 is a single-board programmer that can be expanded to program up to eight boards. The Boardsite 4400 programs from four to 32 boards at a time. Both are now available as benchtop or portable models, and both connect to any IBM PC or compatible over a high-speed expansion bus. □

Printed circuit board component libraries deliver consistency and accuracy

Richard Goering, Senior Editor

One aspect of printed circuit board CAE/CAD that most engineers despise is the creation and maintenance of component libraries. Those library headaches might soon be eliminated, however, by a new company formed to provide component libraries, Sedco (Scotts Valley, CA), which is now forging agreements with printed circuit board CAD vendors.

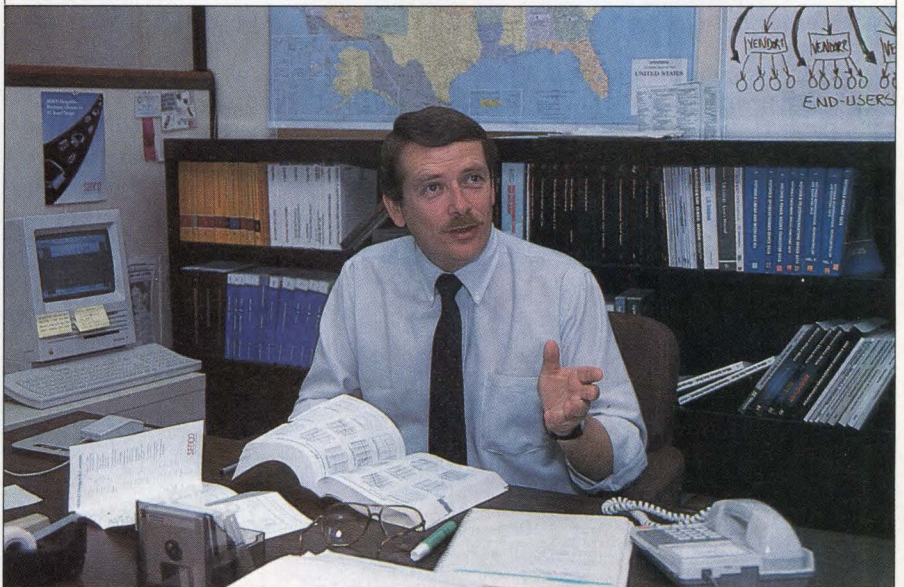
Sedco provides component libraries representing 28 data books with over 20,000 components. Each of Sedco's DesignLib libraries includes a schematic symbol for every component in a single data book, along with a physical outline of every package type in the data book. The libraries also include all the gate- and pin-swapping information necessary for automatic placement and routing. So far, DesignLib libraries are available for design systems from Computervi-

sion, Mentor Graphics, Orcad, Personal CAD Systems, Racal-Redac, Zuken and IBM.

Following an OEM agreement with Zuken (San Jose, CA), Sedco signed an OEM agreement this month in which DesignLib will be sold with IBM's CBDS printed circuit board CAD system. About six more OEM agreements are in the works, according to Sedco president Frank Summers. Also this month, Systems Effectiveness Associates (Norwood, MA) signed a joint marketing agreement in which Sedco will provide component libraries for SEA's thermal- and reliability-analysis programs. Until now, the absence of libraries has prevented many designers from using these programs.

■ Will users pay?

Printed circuit board CAE/CAD vendors already provide component



Creating and maintaining component libraries can be a big problem for printed circuit board CAD users, according to Frank Summers, president of Sedco. "Some users we've talked to say creating and maintaining libraries takes one-third to one-half of their time," he says. To help ease the engineer's task, Sedco provides component libraries that include complete data books and implement a number of accuracy checks.

DESIGN AND DEVELOPMENT TOOLS

libraries as part of their product lines, but these libraries are far from complete. Rather, vendors select the most common components and then group them by technology. A given vendor might offer, for example, 500 of the most widely used TTL parts from Texas Instruments (Austin, TX). One DesignLib, in comparison, covers the entire TI TTL volume 2 data book and can be updated along with the data book.

Accuracy is another selling point for the Sedco approach. Not only is data entry from a data book error-prone, but the data books themselves are often found to be inaccurate. Sedco implements an exhaustive series of checks to ensure library accuracy. "We will not knowingly pass along an error to a customer," vows Summers. "We fixed 600 errors in the Texas Instruments TTL volume 2 data book alone."

The question now facing Sedco is whether users are willing to pay for this accuracy and completeness. After all, printed circuit board CAD vendors don't charge an additional fee for libraries, so they're essentially free. For IBM PC-based systems, Sedco leases its DesignLib libraries for \$125 per seat per year for schematic or layout. For workstation-based systems, a complete schematic and layout library leases for \$1,000 per seat per year.

If CAD users need to manually create even a small number of symbols per year, the cost may be worth it. It takes several hours of an engineer's time just to create a simple compo-

nent definition, exclusive of test and documentation costs, according to Summers. "Some users we've talked to say creating and maintaining libraries takes one-third to one-half of their time," he says.

■ Schematics and layout

The schematic symbols provided by Sedco can be displayed in either the ANSI Y32.14 or IEEE-91 standards. But all of the libraries are compliant with the IEEE-91 standard, which is mandatory for defense contractors.

"There can't be a vanilla file that handles all data structures from all vendors."

—Frank Summers, Sedco



To guarantee consistency between the two different types of symbols, Sedco has developed a symbology that ensures all connection points are the same. Either ANSI or IEEE symbols can thus be plotted from the same library.

The layout symbol includes all pin numbers and names that are in the schematic view. Because there may be small variations in package size, it also includes minimum, maximum

and nominal dimensions for each package. Finally, component height information is included in the layout symbol, letting the libraries be used for the design of three-dimensional mechanical tools that check for clearance and fit inside enclosures.

Sedco libraries also identify functionally equivalent pins, allowing automatic placement and routing programs to swap pins. This information may be included with schematic or layout views, depending on the system. In the future, Sedco intends to add parameters for such characteristics as pin-to-pin timing, thermal properties, weight and mass, and power dissipation. These parameters will be used in SEA's thermal analysis, in addition to stress and vibration analysis.

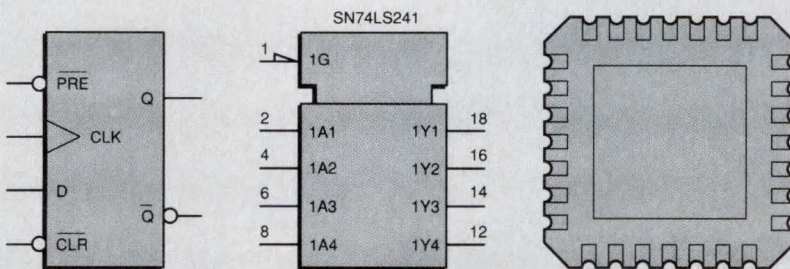
To get the library into a printed circuit board CAE/CAD system, Sedco compiles ASCII files according to the CAD vendor's format requirements. If the vendor uses a binary data format, for example, the library data is then compiled into that format. Once read into the system, the Sedco libraries appear exactly like any other library that comes with the system, and users can modify symbols and add part numbers if permitted by the system.

■ Making EDIF work

Users should remember that each Sedco library is targeted to a specific printed circuit board CAD system. "There can't be a vanilla file that handles all data structures from all vendors," explains Summers. Issuing a library in the Electronic Design Interchange Format (EDIF) won't help, according to Summers, because EDIF is aimed at file transfers between systems. EDIF doesn't let Sedco take advantage of those data structures that might be specific to one vendor.

But Sedco's approach could let EDIF translation take place at a higher level. If two systems have Sedco libraries, a component can be translated by simply referencing its name, orientation and location. One of the big problems with EDIF today is that it's difficult to move library data from one system to another. If Sedco libraries someday become common, then library portability will also become less of a problem. □

INFORMATION PROVIDED BY DESIGNLIB



Sedco's printed circuit board component libraries provide three types of information. Schematic symbols (left) are compliant with the IEEE-91 specification. Gate and pin swapping information (center) notates functionally equivalent pins for automatic placement and routing. Package size and configuration (right) is provided for printed circuit board layout.

CONTROL DATA JUST CHANGED THE DISK DRIVE INDUSTRY FOR GOOD.

Control Data has just created a new, separate subsidiary called Imprimis Technology Incorporated. But you can just call us Imprimis. It means "in the first place." We think it fits—because we are. And we intend to remain there. First in high-performance, high-capacity disk drives. First in quality. First in service and

customer satisfaction.

We introduced the world's first 200 megabyte disk drive in a 3½ inch form factor: the SWIFT™ WREN™ 5¼ inch disk drives were the first to break the sub-20 millisecond seek time barrier and they're still the fastest 5¼ inch drives in the world. The SABRE™ 8 inch disk drive was the first drive of its size to

offer over 1,200 megabytes of storage. And in survey after survey of the OEM drive business, we ranked first in customer service.

So, just because we changed the name doesn't mean we're going to change our ways. We're going to stay the world's leading supplier of OEM data storage products.

**IMPRIMIS**

A Subsidiary of Control Data

Multiprocessing cache bus turns to AT bus for I/O

David Lieberman, Senior Editor

Perhaps the most interesting sidelights on IBM's AT bus are the clever ways designers work around its inadequacies, especially those involved in 80386-based AT-compatible systems—such as 16-bit transfers, relatively low bandwidth, relatively inefficient DMA, and clumsy multimastering capabilities. A new multiuser computer architecture called ATtack, developed by Corollary (Irvine, CA), gets around these inadequacies by relegating the AT bus to the position of I/O bus for a main system bus. The main bus of the ATtack architecture—the C (for cache) bus—has all the facilities that the AT bus lacks for building high-performance multiprocessor systems—and it even has some facilities that are lacking in the more powerful industrial buses.

Using an industry-standard bus as an I/O channel is fairly common in some workstations and larger computers. For such systems and for ATtack, the standard I/O bus gives the system access to a wealth of I/O and peripheral boards available from multiple vendors on the open market. Typically, however, the I/O

channel is linked to a proprietary system bus whose specifics are closely guarded secrets. Corollary, in contrast, is working on cooperative ventures to bring the architecture to market and won't be building its own ATtack machine. "We're going out of our way to be the first computer company to resist the temptation to actually build a computer," says company president George White.

Flexibility key to system

Simultaneous with the ATtack announcement, Zenith Data Systems (Glenview, IL) announced that its ATtack-based prototype workgroup and networking platform has been at beta sites since April. "This architecture is an ideal platform for Xenix/Unix applications, which can best tap the multiuser, multitasking capabilities of this new technology," explains John Frank, Zenith president. "The key to the system is flexibility. By using industry-standard components, operating systems and an open architecture, it allows expansion and upgrading as workgroup needs evolve and microcomputer technology advances."

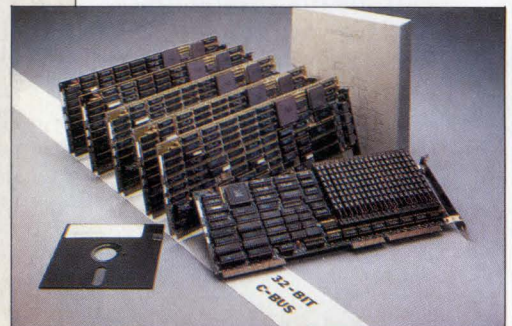
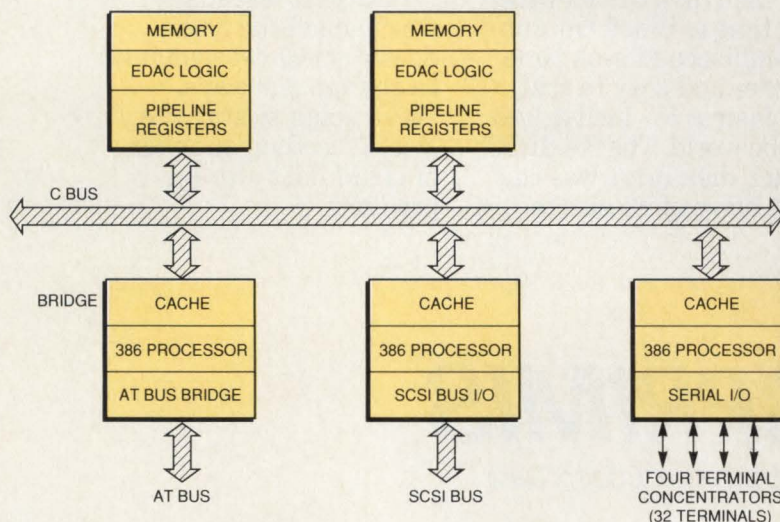
Corollary is having "serious discussions" with three other vendors of personal computer systems, according to White.

The base components

The base components of an ATtack system are two to six 80386-based CPU boards, each with a healthy 64 kbytes of cache and support for an 80387 coprocessor; a SVID-compliant (Unix System V Interface Definition), binary-compatible extension of the Xenix 386 operating system from The Santa Cruz Operation (Santa Cruz, CA); up to four memory boards, each with from 4 to 16 Mbytes of memory for a potential maximum of 64 Mbytes of pipelined, error-corrected memory; the 32-bit, 64-Mbyte/s synchronous C bus; a "bridge" board that links the C and AT buses; and the AT I/O bus with whatever boards the system requires. The ATtack CPUs and memory boards reside only on the C bus, and the AT boards only on the AT bus, while the bridge CPU board resides on both buses, linking the two. The C bus owes its speed in part to a 16-MHz clock rate, compared to the 10-MHz clock rate of NuBus and Multibus II. "Parts have gotten faster since these two buses were first defined," White explains. "We're also willing to live with a 12-in. bus, instead of the 20-in. bus that might be specified for a Multibus II or NuBus system."

The speed and efficiency of the C bus also depend on a block-transfer

THE ATTACK SYSTEM



Corollary's ATtack system includes a main bus—the C (cache) bus—that has all the facilities necessary to build high-performance multiprocessor systems. C bus accommodates up to six 80386 CPU boards, up to 64 Mbytes of pipelined, error-corrected memory, and an AT I/O bus. Bus traffic runs at up to 64 Mbytes/s.

mode that, while optional on several other buses, is the only mode of transfer on the C bus, except for certain utility operations. "There's no such thing as going out to read a byte out of C bus memory," says Corollary's White. "Every transfer is of four sequential 32-bit words." The C bus, CPU caches and system memory are all geared toward this mode of operation. The C bus also has built-in cache coherency protocols, a feature shared by only the Futurebus among the industry-standard buses. For the sake of bus efficiency, a copyback caching scheme is used.

The new bus also features a fair arbitration scheme to prevent bus hogging and overlapped arbitration to

"C bus was built specifically to be a multiprocessing bus, and it's not particularly good at anything else."

—George White, Corollary



avoid unnecessary idling. "Everybody says their buses are 'optimized for multiprocessing,' but C bus was built specifically to be a multiprocessing bus, and it's not particularly good at anything else," White says.

The ATtack caching scheme yields an overall 96 percent hit rate, according to White. "We've used a diagnostic program that attempts to pathologically cause the cache to miss a lot," he says. "When we run it on a five-CPU system, we wind up using about half the bus bandwidth. With a real benchmark running spreadsheets, data bases and a large variety of other application programs, the traffic is between 17 and 20 percent of bandwidth."

This suggests, of course, that the ATtack scheme could be expanded beyond its stated six-CPU limit, which White confirms. "We designed the system for 10 CPUs, although we've only built one with six CPUs so far," he says. "But we're looking at a midrange multiuser platform and aren't trying to compete with Se-

quent Computer Systems."

In an ATtack system, the C bus can be implemented on the same backplane as the AT bus, on a separate backplane or, conceivably, on a ribbon cable across the top of the boards.

As far as running application code

is concerned, ATtack is a completely symmetrical multiprocessor system, although its multiprocessing architecture is invisible to the application. Each CPU runs an identical copy of the extended Xenix kernel, and the system work load is transparently

WIN/TCP™ for 386 STREAMS. The thrill of UNIX® connectivity.

True open systems communication. That's the excitement of WIN/TCP for 386 STREAMS software from Wollongong.

WIN/TCP for 386 STREAMS connects your 80386-based systems running popular versions of UNIX System V Release 3 to other computers supporting the TCP/IP suite of protocols.

Log on to remote systems, transfer files, exchange mail, and integrate Network Management functions. WIN/TCP for 386 STREAMS also supports the Remote File System (RFS), Network File System (NFS), and the R-Series of remote commands.

Ride the current of true UNIX connectivity. Call 800-872-8649 or 800-962-8649 (in California), or write The Wollongong Group, Inc., 1129 San Antonio Road, Palo Alto, CA 94303.

WOLLONGONG

We are the standard.™

WIN/TCP AND WINS ARE TRADEMARKS OF THE WOLLONGONG GROUP, INC.
ALL OTHER PRODUCT NAMES ARE TRADEMARKS OF THEIR RESPECTIVE MANUFACTURERS.

CIRCLE NO. 13

COMPUTERS AND SUBSYSTEMS

distributed among system CPUs as they fetch jobs from a common run list residing in system memory. But since the bridge CPU is the only CPU with direct access to the AT bus, it's the only C bus CPU able to run certain system code, such as the driver routines for an AT disk controller board. The bridge board also contains a memory-mapping function that gives AT boards a 16-Mbyte window on system memory that may, nevertheless, reside virtually anywhere in C bus memory space.

For connection to the outside world, ATack has four 230-kbaud synchronous serial ports that link to a Corollary eight-port terminal con-

centrator. In this configuration, each ATack CPU can link to 32 external serial devices. Other configurations are possible as well. White cites one interested vendor that considered replacing the ports with a small computer system interface (SCSI) chip set in order to bring disk data directly into the C bus without first going through the AT bus. "There's no hard technical information on what the benefit of this might be," explains White, "but perhaps disk traffic can create an AT bus bottleneck in some systems."

The ATack architecture seems to have both the power and flexibility to help carry the AT bus standard well

into the future. Zenith's platform, which is the first announced system to be built around the architecture, demonstrates some of the possible variations. Built around a passive backplane, the as-yet-unnamed Zenith machine implements a combination 8-/16-/32-bit I/O bus called the Superset bus instead of an AT bus. This permits the use of both 8-bit XT and 16-bit AT boards, as well as boards with a full 32-bit interface. The machine also features a fault-tolerant power supply—complementing the fault-tolerance capabilities of a multiprocessor system—and removable disk drives that satisfy archival or security requirements. □

Hybrid board scheme bridges optical and electrical circuitry

David Lieberman, Senior Editor

Someday, prognosticators say, as the increasing speed and density of computer circuitry forces electrical technology to give way to the optical alternative, photons will replace electrons as the data carriers of necessity. In these days of pre-optical computing, however, two electrical engineers have developed a method for bringing the benefits of optical interconnection to electronic circuitry: the Optobuss electrical/optical interconnection system.

Developed and patented by William Batina, president, and Lamar Gipson, vice-president, of Optobuss Technology (Miami, FL), the Optobuss system consists of an optical network embedded within a printed circuit board, an edge-card connector that accommodates both electrical and optical media, and a unique chip-carrier design that bridges the electrical and optical worlds. Although no Optobuss components or systems have actually been built, nor have its basic concepts been tested, the Optobuss system suggests some interesting possibilities for designers who are finding themselves at a dead end with conventional printed circuit board technology.

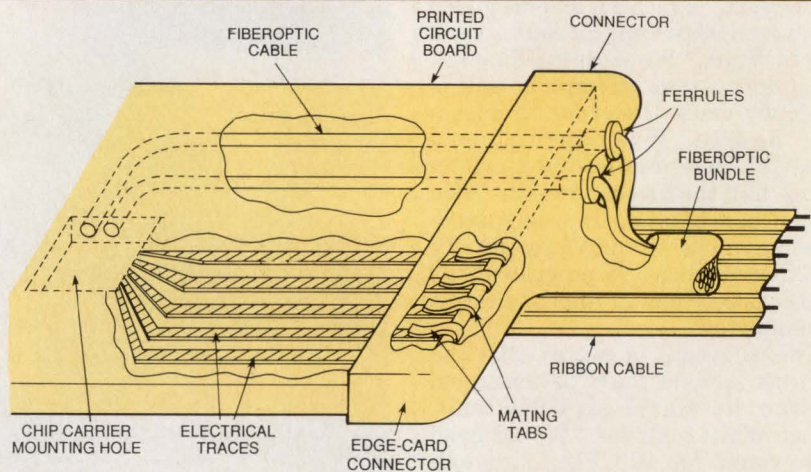
"The Optobuss system was devel-

oped as an offshoot of our research into starting a contract manufacturing company for circuit board assembly," says Batina. "We observed many industry problems with interconnecting high-speed, high-pin-count chips by means of increasingly finer printed circuit board traces

with smaller spaces in between. With finer lines and closer spacing, the capacitance goes way up, which slows transmission down, and there's a greater potential for crosstalk between signal lines." Accomplishing reliable inspection of very dense boards is also a dilemma, according to Batina.

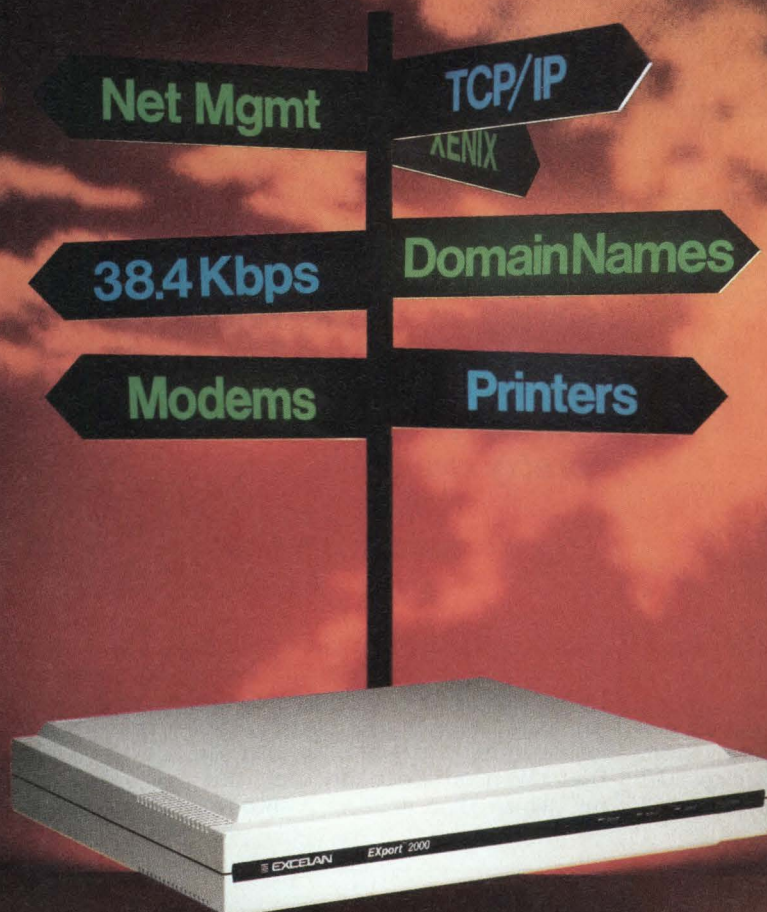
In the Optobuss scheme, a board's data bus(es), address bus(es) and control lines are all implemented via optical fibers, rather than traditional copper traces, within a printed circuit board. Electrical traces are provided on or within the printed cir-

THE OPTOBUSS EDGE-CARD CONNECTOR



The Optobuss edge-card connector secures both electrical and optical media to a printed circuit board for distribution of optical and electrical signals as the application requires. Internal and external optical fibers mate within the connector body. Tensioned finger tabs connected to the ribbon cable mate with electrical traces on the printed circuit board.

Unlimited Service.



Now there's a server that does much more than connect terminals to your network. With Excelan's EXport™ 2000, you can communicate in a variety of directions. Modems and printers can be shared, as can incoming connections to hosts. With unparalleled flexibility, power, and convenience.

The EXport 2000 server connects all types of RS-232 asynchronous serial devices to Ethernet. And with Network Management Station™ (NMS) software that runs on VMS, UNIX or DOS, you can configure and control all communications servers on your network, no matter where they are located.

Moreover, Excelan's EXport 2000 communications server supports other industry-standard protocols such as TCP/IP, RS-423, and Domain Name Service.

Find out how the EXport 2000 extends Excelan's complete, high-speed LAN solutions for heterogeneous environments. Call today: **1-800-2-GET-LAN.**

CIRCLE NO. 14



2180 Fortune Drive San Jose, California 95131 800-2-GET-LAN FAX 408-434-2310 Telex 176610
Excelan Europe, Ltd. Intec 2, Suite 17, Wade Road Basingstoke, Hampshire, RG24 0NE England, UK
Tel: (44)256-842296 FAX (44)256-842298

COMPUTERS AND SUBSYSTEMS

cuit board basically for power and ground, and wire is used for communications within each chip carrier. It's also possible to install additional electrical highways for other functions.

Because of the inherently greater speed and bandwidth of optical transmission, says Batina, "One optical fiber may be able to substitute for an entire 16- or 32-bit data bus. In an address bus, the lower-order bits move very rapidly and the higher-order bits sometimes move more slowly, so you might want to use an individual fiber for each lower-order bit but multiplex all the higher-order bits into a single fiber." Fiberoptic transmission also offers the familiar benefits of immunity to electromagnetic interference, electromagnetic pulses and electronic countermeasures.

The Optobuss configuration

The Optobuss solderless chip carrier, pressfit into a printed circuit board mating hole, consists of an opaque, molded ceramic substrate, transparent plastic side walls and an integral beam splitter. Three dice—a phototransistor, a function chip (such as a microprocessor or a memory chip) and a phototransmitter—are epoxied to the substrate and interconnected

via wire bonding. Batina predicts that future ICs will incorporate the functions of all three dice into a single die.

In operation, a light pulse traveling down an optical fiber enters the Optobuss carrier through one side and hits the beam splitter, which deflects some portion of the light to the phototransistor. The phototransistor then converts the optical signal to an

"I wonder about the yield and the cost of Optobuss, considering the difficulties we have now with PC board houses dealing with pretty straightforward things."

—Chuck Richardson, Micro Industries



electrical signal that's conducted to the function chip. Electrical signals that are output by the function IC are conducted to the phototransmitter for conversion to an optical signal that's transmitted to the beam splitter, which then deflects it into the

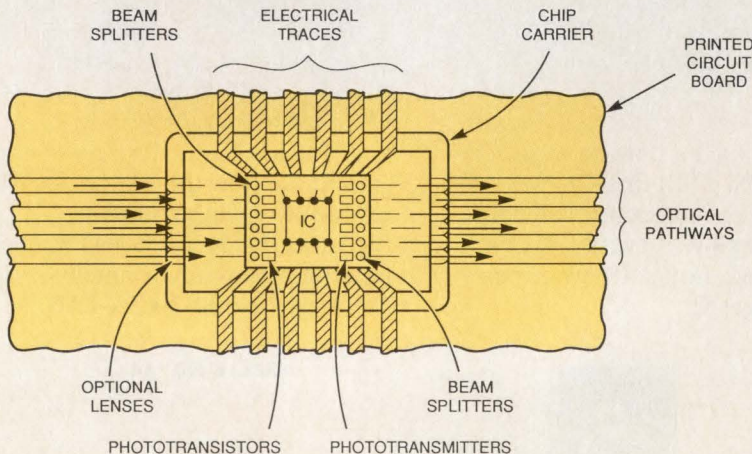
optical pathway.

Electrical signals output by the phototransistor can also be conducted directly to the phototransmitter for optical conversion and transmission, if so required. As an option, optical lenses can be used to focus and project the light entering or exiting the chip carrier. In addition, a pair of carriers can be sandwiched around a single beam splitter to create a bidirectional optical network.

A variation on the basic Optobuss interconnect scheme provides a novel approach to multiboard computer design: the vertical optical interconnect. Built with a transparent top and bottom, the chip carrier could be used to transmit signals perpendicular to the plane of a printed circuit board to communicate with other boards stacked above or below it. According to the intent of the Optobuss scheme, the multiple stacked printed circuit boards would be separated by thermally conductive plates that act as heat sinks, and holes would be drilled through the plates to let optical signals be projected from board to board throughout the stack.

By offering both thermal management and a very high-speed board-to-board interconnect, the Optobuss stacked printed circuit board scheme is a perfect medium for developing gallium arsenide-based systems today, says Batina. A stacked printed circuit board system also would result in an extremely rugged design.

AN OPTOBUSS PRINTED CIRCUIT BOARD



An Optobuss printed circuit board can have multiple electrical and optical pathways to the chip carrier. Electrical traces exist primarily to provide power and ground, and the function IC is wire bonded to the photodie. Many signals can be multiplexed onto a single optical fiber.

From concept to finished product

Right now, Optobuss is only a concept. Transforming it into a real-world product means problems and expense. It's uncertain, for one thing, whether common optical fiber could withstand the high-temperature, high-pressure processing used with common printed circuit board materials. Molded printed circuit boards made of plastic or some other material would probably be most appropriate for the Optobuss scheme, according to Batina. Also, since the optical fibers must be bent to route an optical pathway wherever one is needed, he says, "The glass optical fibers we're all familiar with aren't necessarily the right transmission media for Optobuss."

The Optobuss system also would require extremely tight manufactur-

COMPUTERS AND SUBSYSTEMS

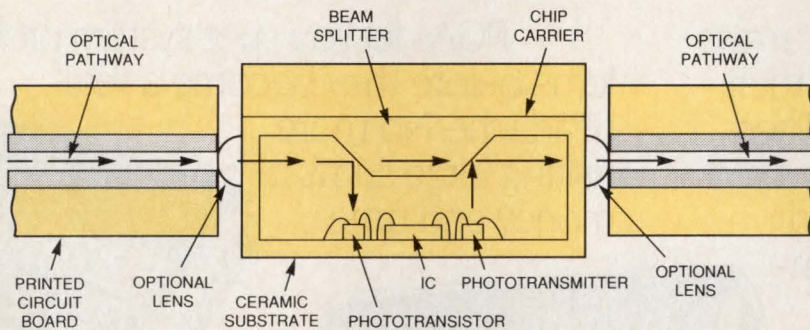
ing tolerances. One reason for this would be to ensure proper alignment between the deflecting surfaces of the beam splitter and the optical fibers on either side, and between the splitter and photodice. Also, the Optobuss system's potential for using dual electrical/optical highways, optional lenses in various locations, both sin-

Nonetheless, Batina views Optobuss as a relatively simple system. "You've got to take a close look at some recent high-performance boards," he says. "They've got 24 layers these days. That in itself creates an absolute layout nightmare, not to mention what happens in debug, test and inspection."

some appeal in the scheme. "We've been hearing about all kinds of wild things being done with printed circuit boards lately, including a scheme to place components in pre-cut grooves," he says. Like the mating holes for Optobuss chip carriers, these grooves are intended to simplify the placement and alignment of fine-pitch devices, a procedure that, according to Richardson, tends to be "very critical, difficult and expensive. I wonder about the yield and, hence, the cost associated with Optobuss boards, considering the difficulties we now have with printed circuit board houses dealing with pretty straightforward things."

Michael Hayward, president of Hybricon (Ayer, MA), thinks the notion of an optical interconnect between boards is somewhat premature, although he mentions that some companies have successfully used optical transmission to interconnect backplanes in different chassis. "The market for optical transmission of signals was supposed to take off for about 15 to 18 years now, but it hasn't," he says. "It may make sense for very specific applications where it would allow the size of the equipment to be materially reduced, but otherwise it would require deviation from existing bus standards, so there would be no open-market boards available for it. Even if it offers significant advantages, such a scheme will take a long time to take off." □

THE OPTOBUSS CHIP CARRIER



The Optobuss chip carrier has transparent side walls that let light pulses enter and exit. A phototransistor die converts the optical signal to an electrical signal for the chip; a phototransmitter die translates the chip's electrical output into an optical signal. If fashioned with transparent top and/or bottom walls, the carrier would also allow the implementation of interboard optical pathways.

gle and multimode fibers, uni- and bi-directional pathways, and a range of other possibilities could quickly tempt the designer into unnecessarily complex implementations. Then, too, the more complex the Optobuss design, the less tolerance it might have to minor imperfections in the actual implementation. On the other hand, however, if properly done, an Optobuss design could conceivably exploit complexity to create an implementation that's very tolerant of system faults.

Managing signal timing in Optobuss wouldn't be an easy feat either, because of its built-in redundancy. Since a light pulse entering the chip carrier is only partially deflected by the beam splitter, an attenuated version of the signal passes through to the next chip in the optical pathway, creating the potential for contention problems. Then, too, if the electrical signal output by the phototransistor is conducted to the phototransmitter as well as to the function chip, another version of the signal enters the optical pathway.

Another potential problem with Optobuss is that optical-to-electrical and electrical-to-optical conversions within the chip carrier would introduce a certain amount of delay, albeit trivial compared to the overall speedup. Also, if parallel data is serialized for transmission over a single fiber, this would inject a degree of delay. Furthermore, the light lost because of this partial deflection could become a problem. "It might become significant if you're trying to communicate over several kilometers," Batina admits, "but for several inches or centimeters, it probably won't be a problem." It's also possible, he adds, to construct a half-silver-type mirror splitter that would deflect virtually all the light that hits it.

■ Mixed response to Optobuss

Industry spokespersons have expressed mixed reactions regarding the Optobuss scheme. Chuck Richardson, director of the Surface Mount Technology Association and vice-president of manufacturing at Micro Industries (Westerville, OH), sees



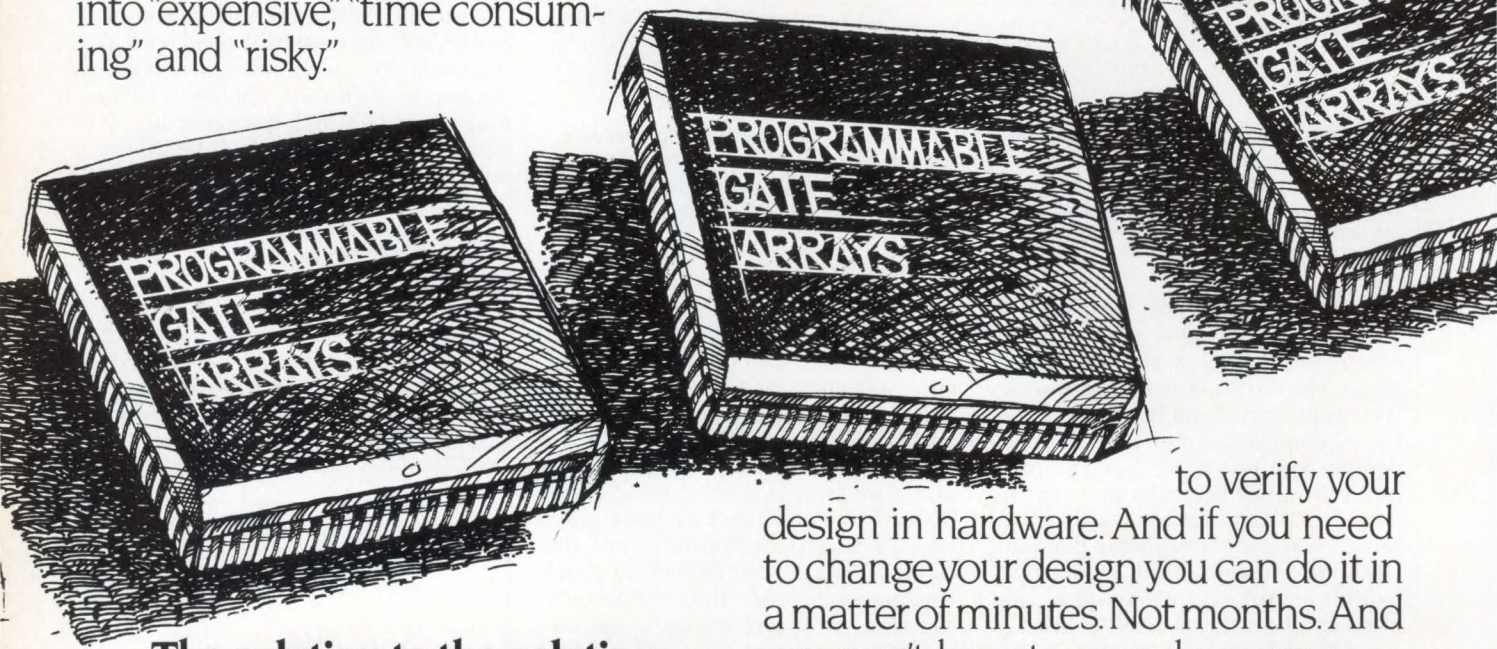
Trying to find the right ICs?

Turn to the Integrated Circuits section in New Product Highlights. You might find just what you need.

No one can solve but we solve

Everyone thought gate arrays would be a great solution to their semi-custom design needs. Then they designed one and discovered that "semi-custom" translated into "expensive," "time consuming" and "risky."

PGAs let you spot system problems before they become a real headache. No more risking large sums of money and time



The solution to the solution.

Meet the Logic Cell™ Array—the first Programmable Gate Array. It's a high density CMOS chip of unmatched technology that's user programmable where it's easiest for you to program—in software.

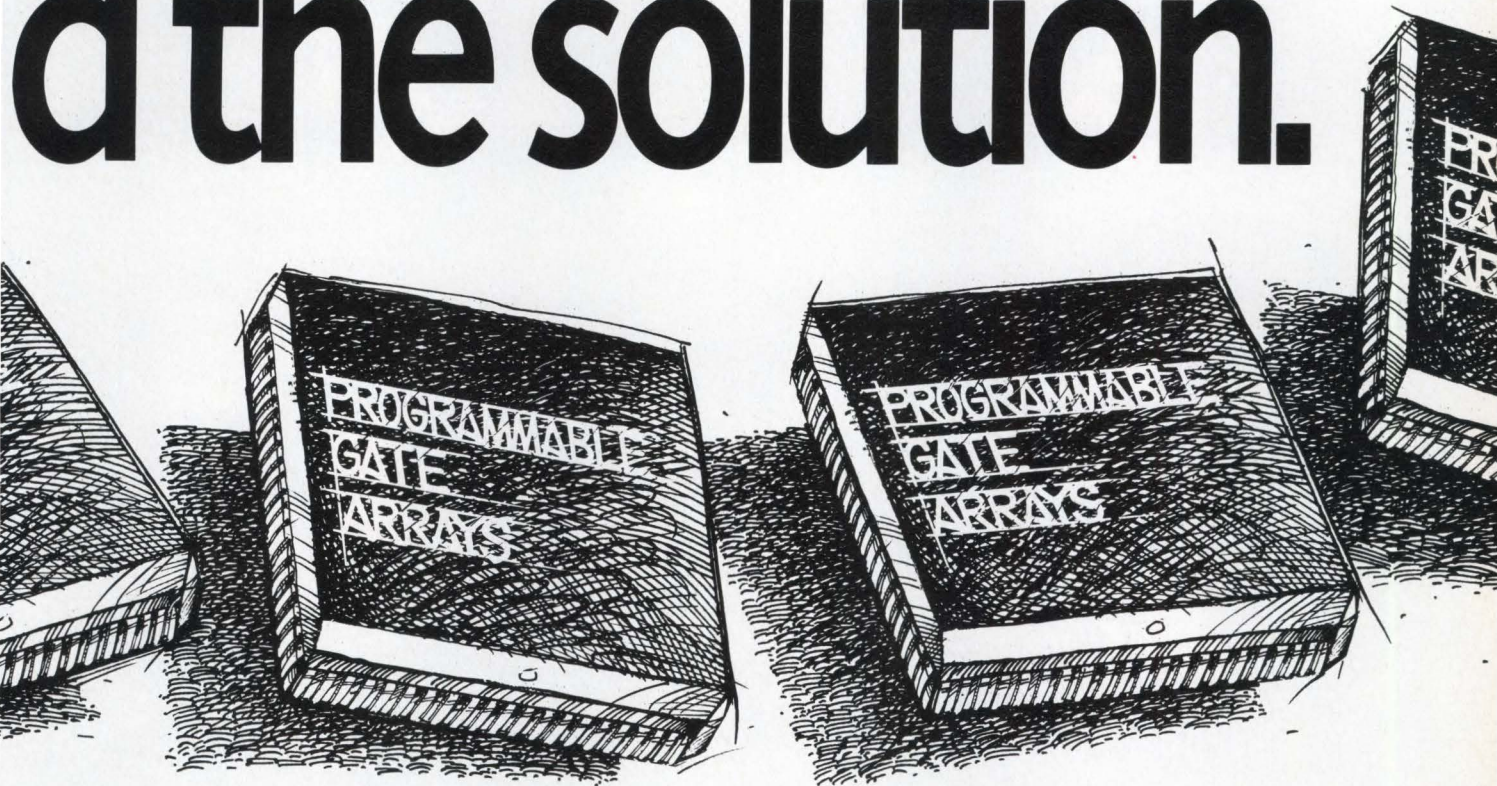
Your development cycle is cut to a week or two instead of six months. So you can get your product to market that much sooner.

to verify your design in hardware. And if you need to change your design you can do it in a matter of minutes. Not months. And you won't have to spend any more money.

9000 ways to get ahead of schedule.

The Am2000 series has densities from 1000 to 2000 usable gates and the Am3000 series has densities from 2000 to 9000 usable gates. With those densities (we'll have even higher densities later), you need fewer parts to get the same functions as

ve the problem, d the solution.



EPLDs or discrete logic.

There is no other PGA technology available today. And over 5000 designers are already using it.

Even getting started is easy.

Your investment is minimal. You don't have to finance months of NRE. You can get started for the price of a PC (which you probably already have) and some software.

PGAs are the epitome of the just-in-time product. They are the only gate arrays stocked in production quantities at your distributor. And they're programmable instantly. Which means you can go from design to production as fast as you need to.

Even overnight.

See for yourself.

Contact us for a free diskette that gives you a detailed product overview, an interactive session where you can plug in your own design criteria and find out how PGAs can help your design. Part of the PGA development software is included so you can get started saving time and money right away.

Just call (800) 222-9323. Or drop us a line.

Advanced Micro Devices 

901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088.

© 1988 Advanced Micro Devices, Inc. Logic Cell is a trademark of Xilinx, Inc.

CIRCLE NO. 15

Doorways to DSP



High performance A/D and D/A converters for digital signal processing and other dynamic applications.

Now you can transfer signals between the turbulent analog world and the ordered digital world simply and accurately.

Burr-Brown offers the industry's most complete line of precision data converters specifically designed and tested for dynamic signal processing applications. Use them to obtain peak

performance from waveform generators, FFT-based spectrum analyzers, and other designs requiring superior dynamic range and spectral purity.

Millions of units of experience.

Our PCMs are already the converters of choice for compact disc systems, music and speech synthesizers, and professional audio equipment

throughout the world. They provide exceptional performance and are backed by millions of units of design and manufacturing experience. Contact your Burr-Brown technical rep for complete information, or call Applications Engineering, 602/746-1111. Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734.

MODEL	PCM53P	PCM54/55	PCM56P	PCM64	PCM78P
Type	D/A Converter	D/A Converter	D/A Converter	D/A Converter	A/D Converter
Resolution	16-Bits	16-Bits	16-Bits	18-Bits	16-Bits
Dynamic Range	96dB	96dB	96dB	108dB	90dB
Total Harmonic Distortion + Noise	-94dB	-92dB	-92dB	-100dB	-88dB
Conversion/Settling Time	350ns (I_{out}) 3 μ s (V_{out})	350ns (I_{out}) 3 μ s (V_{out})	350ns (I_{out}) 1.5 μ s (V_{out})	200ns (I_{out})	4 μ s
Packages	Plastic DIP	Plastic DIP, SOIC	Plastic DIP	Plastic DIP	Plastic DIP
Price*	\$12.15	\$10.90	\$12.00	\$31.80	\$39.90

*U.S. prices only, in 100s.

BURR-BROWN®



CIRCLE NO. 21

AI techniques enter the realm of conventional languages

AI techniques become practical and accessible by linking AI modules written in languages such as Lisp or Prolog into conventionally coded systems.

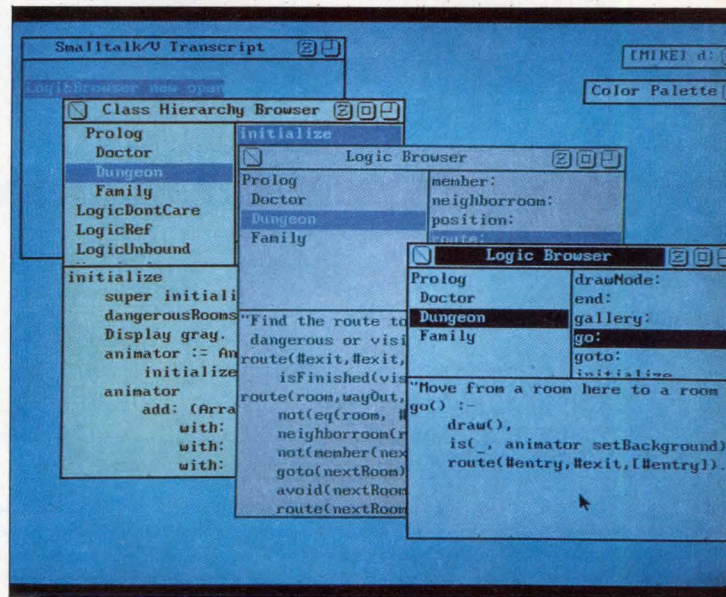
Howard Falk
Contributing Editor

Artificial intelligence techniques promise to provide the built-in cleverness needed to run the complex systems of the future. But most system developers have been frustrated by the difficulties of implementing these techniques. Coding AI in conventional languages such as C or Ada is, to say the least, arduous. Although AI-oriented languages, of which the best known are Lisp and Prolog, offer much simpler programming for AI functions, they also have discouraging faults. Code execution is slow with these languages, and demands for memory are extensive.

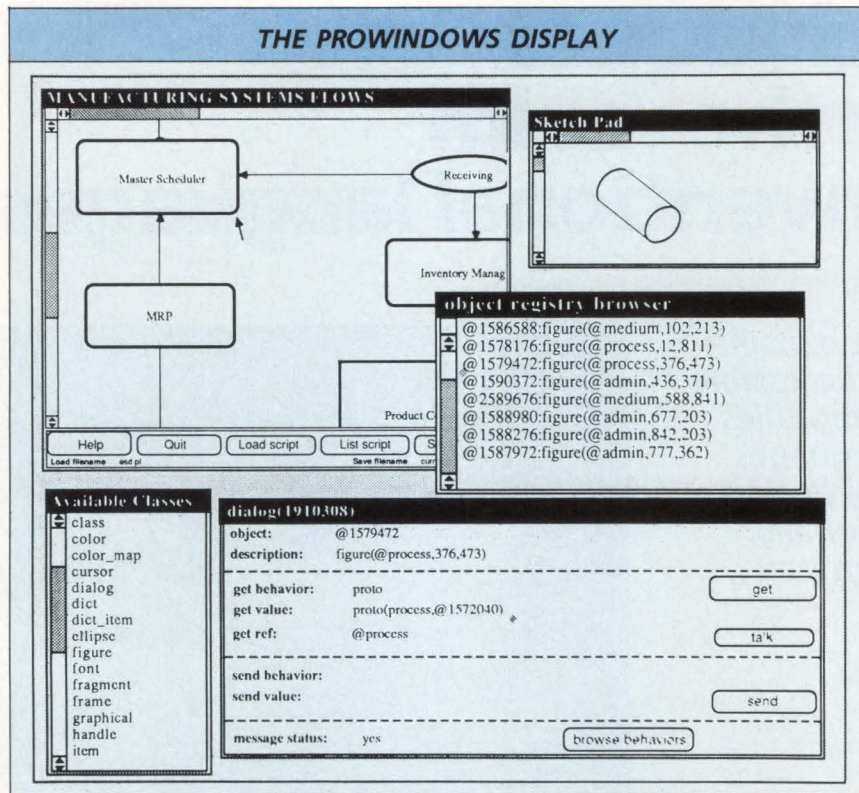
Although Lisp and Prolog vendors initially considered their products to be superior replacements for conventional languages, users haven't been drawn to these languages as vehicles for developing complete software systems for large applications. Instead, most Lisp and Prolog vendors and users now stress the ability to embed intelligent modules, developed in these languages, within conventionally coded systems. Restriction of Lisp and Prolog to narrower use has been further defined by developers of AI tools, who have discovered that, despite the difficulties, it can often be worth the effort to use conventional languages to implement AI functions.

If a workable strategy to extend the use of Lisp and Prolog beyond the present limited group of devotees exists, it probably lies in encouraging the development of AI modules, written in these AI-oriented languages, which can be linked into conventionally coded systems. "We recognize that Prolog isn't a universal language. It won't solve all applications problems, but Prolog-coded routines can be useful in many applications systems," says Johnathan Grayson, a member of the technical staff at Expert Systems International (Philadelphia, PA).

In the future, according to David Bowen, manager of Prolog technology at Quintus Computer Systems (Mountain View, CA), the Prolog language will have to synchronize more closely with conventional software tools because users are becoming more interested in adding Prolog subroutines to conventional language programs than in doing complete applications in Prolog. At present, C can be called from Quintus Prolog, and there's an interprocess library package that lets a running Prolog process be called by a separate C process. There's still no general mechanism for calling Quintus Prolog



Prolog/V is an AI-oriented language designed by Digitalk for use with its object-oriented language, Smalltalk/V 286. Users can connect the two languages through this window display. Code for the object class Dungeon, for example, is displayed in the three windows: two Logic Browser windows and a Class Hierarchy Browser window. Collapsed windows (top right) are for disk browsing (MIKE) and color selection.



The ProWindows display from Quintus aids users of Quintus Prolog during software development. The application flow diagram (upper left) can be altered by using display buttons that call for help information, load new diagram scripts, add nodes and change connections between them. The Object Registry Browser window displays defined lists of existing objects, while the Available Classes window displays a scrollable list of available classes. Users can both send and receive messages about these objects through the Dialog window (lower right).

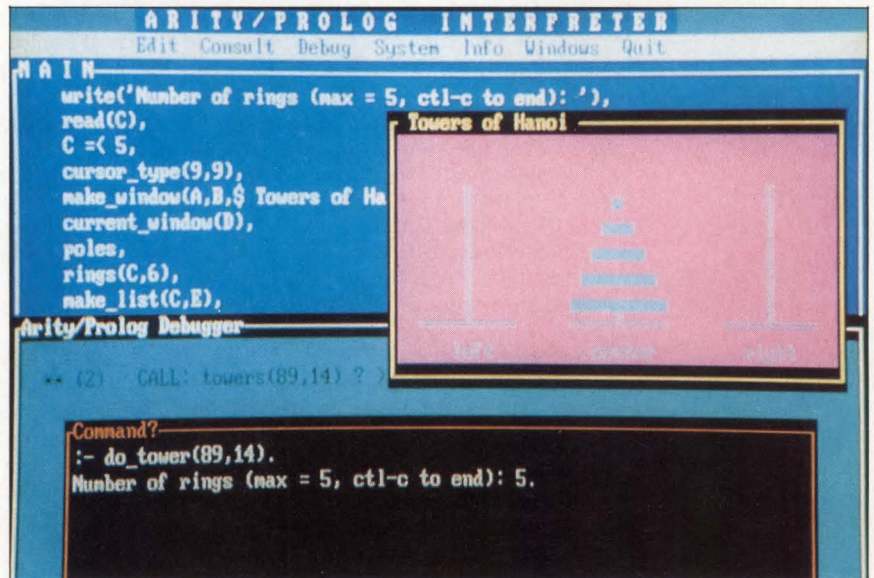
code from a C program, but Quintus plans to add this capability.

In the traditional Prolog development environment, the compiler is always present, and users go through a compile, test, modify cycle with a compiler to add functions to an application. In contrast, the Quintus Run Time Generator takes Prolog source code as the input and produces standalone executable files, such as Unix .O or VMS .OBJ files, for distribution. This lets applications that combine Prolog with C be constructed using standard system linkers. The compiled code can be shared, so that one copy in memory can be used by multiple processes. Individual source files can be separately compiled, allowing use of library files and rapid modification of applications.

Recent versions of Arity Prolog from Arity (Concord, MA) let programmers call C code. With the latest version, Prolog can be called from C. In addition, this latest version of Arity Prolog accepts all C language declarations. At the beginning of a C

file, for example, there can be INCLUDE statements that define C data structures and functions. These and other C expressions can be embedded directly in the Prolog code, without the need for special calling routines to translate data formats. In turn, Arity Prolog users have direct access to various conventional language libraries. To use a C function such as PRINTF, a C-style INCLUDE declaration is placed at the beginning of the file, and the print function then becomes available through Prolog.

Expert Systems International provides interfaces between its Prolog-2 and other languages such as C, Fortran, Pascal and assembly. The interfaces are bidirectional, letting either a Prolog pattern-matching routine or a theorem-proving routine be called from C code, or C modules be called from Prolog code. Prolog-2 is modular, and independent pieces of code can be developed in Prolog or in conventional languages, then tied together using the Prolog interpreter. The modules can contain compiled Prolog code, Prolog data bases stored in heap format (so they can be loaded quickly), assembler routines and compiled conventional language code. Modules having conventional language are called just as if they were Prolog predicate modules, but they execute as conventional code.



The Main window of this development display from Arity lists a game program written in Prolog. (Output can also be displayed through this window.) Execution of the program is shown in the box labeled Towers of Hanoi. Working on a line of code in the Debugger window, the user has popped up a command box through which that portion of the code is being re-executed. From the menu bar below the screen title, users can select function keys to pull down additional windows for editing, reading in files, adjusting the size of existing windows or working with DOS.

"Interfaces to other languages are becoming increasingly important," says Richard Gabriel, chief technical officer at Lucid (Menlo Park, CA). Gabriel notes that C, Pascal and Fortran are all being used in conjunction with Lisp, and that many Lucid Common Lisp users are now embedding AI functions within conventional software. To make this worthwhile, users must be able to call into and out of Lisp to the other language with little or no penalty in time and effort.

"Initially, Lucid provided inadequate means for interfacing to other languages," admits Gabriel. The company then developed a data-structure description language that describes foreign data structures in a declarative way. This lets Lucid Common Lisp construct and recognize such data structures. These structures are known to the Lisp garbage collector, which is a routine that makes memory available by clearing out infrequently used material.

The interface between the languages doesn't create objects that will be discarded by the garbage collector. C and other procedural languages have stack frame formats that are radically different from that of Lisp. Lucid's approach lets Lisp and foreign language stack formats coexist. Lucid software also ensures that Lisp-style interrupts can be correctly processed by C code. Since C and Lisp must share the same address space, Lucid Common Lisp understands malloc and other C procedures for allocating storage.

The ability to move easily between a declarative AI language such as Prolog or Lisp and conventional procedural languages, combined with the ability to prepare linkable AI language modules, is the wave of the future, according to Gabriel. This approach lets developers use AI techniques in conventional software systems without making a large commitment to AI technology, since AI segments can be imported into existing or planned systems.

■ Effective prototyping tools

If Lisp and Prolog can extend their usefulness by serving as tools for developing embedded AI, system developers will become more familiar with these languages and may discover that they also have virtues as prototyping tools.

One of the problems with development of large systems is that conventional software preparation, and

Space station system troubleshoots with embedded AI

A good example of embedded intelligence is the Mission Information Data Analysis System (Midas) for a planned U.S. space station, according to Ronald Citrenbaum, chairman of Abacus Programming (Van Nuys, CA). Midas takes in telemetry data and monitors for fault summary messages coming from space. The system's objective is to let users identify, locate and solve problems as they arise.

When an expert system like the one in Midas interfaces with traditional data-retrieval facilities, it's possible for users to make their queries in terms of their problems, without having to know where or how the stored data is organized. In response to a query about a malfunctioning subsystem, for example, Midas might reply that there are three probable areas of trouble. The user could then choose one of those areas, and Midas would display any data from that area that wasn't within normal ranges. Midas would also comment on the current behavior of the system, compared to its expected behavior, and on related problems that had been encountered in the past. This kind of interactive troubleshooting based on a large data base is comparable to discussing problems with another person, according to Citrenbaum.

In a conventional data base configuration, there might be an operating system, a data-management system such as R-Base and application programs written in C. The application programs would call material from the data base and, if outside expertise was needed, a user interface would handle the interaction. With embedded intelligence, expert system software emulates the human expert in guiding the work of the overall system. A protocol interface is used to link the expert system to the applications code and the data-management system.

The Abacus Programming expert software for Midas resides on personal computers and is written in Pascal. Information on components and black boxes is stored in a 30,000-record data-tape data base. The Pascal programs interface with an R-Base relational data base, which controls the data-tape data base. Associated with the R-Base is a large program, written in Arity Prolog, which provides information about the meaning of the data. Midas users key in questions directed to mission problems. The AI embedded in the system translates this user input into a query through R-Base to find relevant data, and then displays the results through the Pascal software.

modification to meet changing requirements, can take a very long time. To speed the process, many developers now write a preliminary prototype program as soon as the basic requirements for the software are known. The prototype can then be examined by prospective users, the added requirements formulated, and another prototype produced. If the prototype programming process is both simple and fast enough, it can be repeated as needed until a satisfactory design is attained. If necessary, when a sound design has been attained, the software can be recoded in another language to attain faster execution speed.

Often a program that takes 100 lines of C code can be written in 50 lines of Lisp. Lisp programs are simpler to modify than those written in C or Ada, according to Ronald Citrenbaum, chairman of Abacus Programming (Van Nuys, CA). Citrenbaum believes that Lisp and Prolog are ex-

cellent tools for fast prototyping because they let developers quickly write new code.

■ AI languages lack speed

Although Lisp and Prolog haven't become popular with system developers, they're fairly well known as the fundamental languages used to develop expert system tools. But amid the excessive growth of expert systems technology, and the less-optimistic recent expectations, there's been a subtle but broad move away from AI written in Lisp toward the more conventional languages, such as C and Pascal.

As Citrenbaum sees it, this trend is based on the fact that the AI user community is moving out of the research labs and into real-world applications. He points out that most conventional languages have recursive functionality and other basic features needed for expert system development. Whether the language

■ AI LANGUAGES

is Lisp, Prolog, C, Pascal or Ada, it can be used to develop reusable AI subroutines. During the next few years, Citrenbaum expects to see many Ada-based tools developed for AI applications.

Nexpert Object, an expert system development tool from Digital Equipment Corp (Marlboro, MA), for example, is written in C for VAX systems. Other similar expert system development tools, including the S.1 from Teknowledge (Palo Alto, CA), KES from Software Architecture and Engineering (Arlington, VA) and Rulemaster from Radian (Austin, TX), are also written in conventional code. Now that expert system techniques have become well defined, the needed modules can be readily coded in conventional languages. While it's true that such modules can be built more rapidly in Lisp or Prolog, they will run more slowly.

In fact, vendors of AI-oriented languages make no bones about their slowness and even willingly offer speed estimates. Allegro Common Lisp from Coral Software (Cambridge, MA) is about half as fast as C,

according to Andrew Shalit, software engineer. Shalit says that Lisp slowness can be particularly evident when run-time libraries are used, since storage paging tends to be inefficient. Quintus' Bowen estimates that a typical Quintus Prolog application will run about four times slower than the same application written in C. He notes that execution speed

"We recognize that Prolog isn't a universal language."

—Johnathan Grayson,
Expert Systems International



of Prolog code, when symbolic information is being manipulated, now runs about half as fast as C. This fourfold slowdown is due to the fact that Prolog is even slower for arithmetic computations.

Lisp or Prolog vendors seem unable to predict when, if ever, Lisp and Pro-

log code will run as fast as equivalent C code. Meanwhile, since user choices of one version versus another of these AI-oriented languages is still mainly influenced by speed, vendors are striving to improve these codes to optimize their speeds.

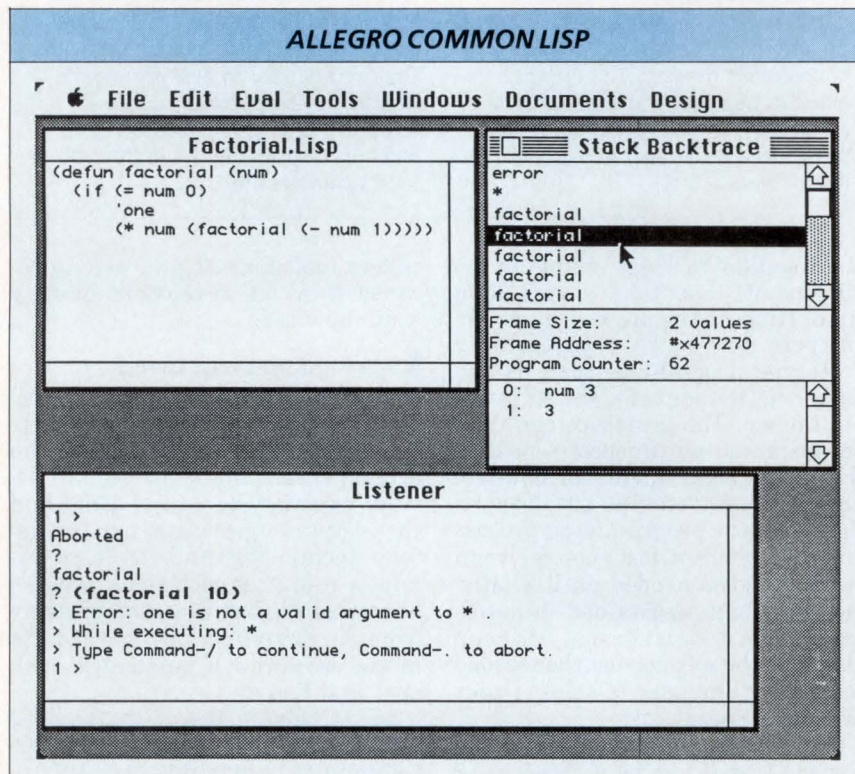
■ Optimizing AI speeds

About a year ago, Arity found some mistakes in the traditional model it had used for Prolog compilation, known as a Warren abstract machine. Since then, a new Arity compilation model has been developed that analyzes Prolog code in unique ways. Arity Prolog is much faster in execution than competitive versions of Prolog, according to Gabriel.

Prolog code consists of clauses within predicates (procedures). During compilation, indexing is performed to find the desired clause. Traditionally, when a clause is compiled, a lot of time is spent optimizing the head of the clause, or the material before the "if" in the clause. The body of the clause is then compiled as a series of calls. The new Arity compilers take a more powerful approach, which considers the entire clause and the entire predicate when making optimization decisions. Arity also uses optimizations that deal with calls to predicates. With this broader view, additional worthwhile optimizations come into play.

New optimization techniques developed for Allegro Common Lisp RISC versions, from Franz (Alameda, CA), also take a broader view of the source code. The intermediate code form used in the RISC compilers lets optimizations be performed based on data-flow analysis. Instruction scheduling implements optimizations that take advantage of delays after branch instructions. When users declare that numbers are floating-point, special floating-point optimizations are invoked by the compiler.

AI vendors are also offering users added control over optimization. For example, in GC Lisp from Gold Hill (Cambridge, MA), there's a proclamation statement that lets users specify degrees (one to four) of speed and code-size optimization, as well as optimization safety. Typically, when code is first being developed, safety is set high, so errors will be readily caught for debugging. Once the code is developed and debugged, optimization safety can be set lower to generate faster, more efficient code. Users can hope that no added bugs will be



Editing, debugging and dialog with Coral Software's Allegro Common Lisp are conducted via this screen. The upper left window displays and provides editing for a disk file called Factorial.Lisp. The top of the Stack Backtrace window displays a series of function calls that led to an error; the middle gives details on the highlighted function; and the bottom displays the local variables of highlighted functions. The Listener window provides a means for accessing Allegro Common Lisp.

introduced by this setting. Users of Allegro Common Lisp can set the compiler for maximum run-time error checking and for speed, with settings from one to three for each. Users can also decide which compiler functions will be invoked or bypassed by different settings.

If the user throws the right switch, the Lucid Common Lisp compiler can report on which optimizations could and could not be done. Such information can be valuable to developers seeking to improve their code. Lucid is working to further improve this capability, according to Gabriel.

Vendors are also striving to find ways to limit Lisp's appetite for memory, mostly by reducing the number of Lisp language functions kept in memory. The undesirable side effect, however, is sometimes slower execution. Another approach to limiting this need for memory is to use shared dynamic libraries of Lisp software, similar to those provided by Unix. Techniques are being developed at Lucid to link together Lisp and conventional code segments for

these libraries. Since few libraries for Lucid Common Lisp have been produced, the development process includes recoding Lisp code segments into library-usable formats.

If Lisp and Prolog can capture the allegiance of a large number of developers who wish to incorporate AI modules in larger, conventionally coded systems, these languages have a promising future. Programming and maintenance of existing pro-

grams in these languages seem to call for less effort than do conventional languages. Undoubtedly, Lisp and Prolog seem to be superior vehicles for developing AI implementations. But until the drawbacks of sluggish execution and significant memory demands are overcome, prospective users will continue to be diverted from investing in these AI-oriented languages and will postpone their use of AI techniques. □

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Abacus Programming (818) 785-8000, ext 209	Circle 248
Arity (508) 371-1243	Circle 249
Coral Software (617) 868-7440	Circle 250
Digital Equipment Corp (508) 490-8004	Circle 251
Expert Systems International (215) 735-8510	Circle 252
Franz (415) 548-3600	Circle 253
Gold Hill (617) 621-3300	Circle 254

Lucid (415) 329-8400	Circle 255
Quintus Computer Systems (415) 965-7700, ext 354	Circle 256
Radian (512) 454-4797, ext 5523	Circle 257
Software Architecture and Engineering (703) 276-7910	Circle 258
Teknowledge (415) 424-0500, ext 453	Circle 259

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 500 Average 501 Low 502

AP LABS I/O SUBSYSTEM



THE GATEWAY TO FAST, AFFORDABLE REAL TIME APPLICATIONS

The AP Labs IOS is a programmable I/O Subsystem enabling many general purpose and scientific host computers to perform data acquisition, storage and data routing tasks in real time environments. The IOS interfaces with Gould, DEC-VAX, Sun Microsystems, UNIX and NTDS Host computers, VMEbus computers and Aptec and FPS Processors.

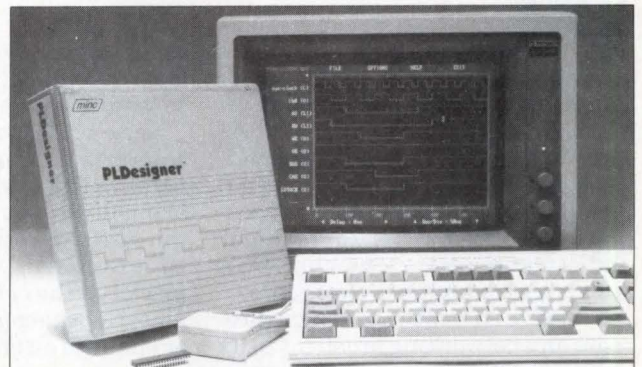
The AP Labs IOS provides:

- ▶ LOW COST INTERFACE
- ▶ LARGE SELECTION OF PERIPHERALS—with drivers

- ▶ OFF LOADING OF THE HOST COMPUTER
 - ▶ HIGH LEVEL SOFTWARE CONTROL
 - ▶ TEST AND DEBUG PROGRAMS
- AP Labs IOS supports Real Time Data Routing, Hardware In-The-Loop Simulation, Signal/Image Processing, Process Control, Data Acquisition, Data Switching and Real Time Graphics. Call today.

AP Labs
ADVANCED PROCESSING
LABORATORIES, INC.
4411 Morena Blvd. Ste. 150, San Diego,
CA 92117 (619) 272-8890

CIRCLE NO. 24



Introducing PLDesigner™ from Minc

Now—Design Synthesis For PLD Designs

This universal next generation tool separates design from device selection and provides:

- High level behavioral language
- Algorithmic design entry for state machine
- Waveform design entry for interface logic
- Simulation with automatic test vector generation
- Partitioning across multiple device architectures
- Automatic selection of devices
- Device library of over 2,000 devices

PLDesigner runs on IBM and compatibles. Call and ask for our demo disk showing PLDesigner in action on several logic examples. Now, speed your design time and get your product to market faster.

MA, CT, RI, ME, NH, VT (617) 935-3001 • NY, NJ (201) 692-0200 • IL, IN, WI, MI, IA (312) 298-2290 • TX, OK, LA, AR (214) 661-0300 • WA, OR, MT, ID, AK (206) 746-7970 • Northern CA, Reno NV (408) 980-8868
Southern CA (714) 897-0319

Minc Incorporated
1575 York Road, Colorado Springs, CO 80918 (719) 590-1155



CIRCLE NO. 25

Sharing design data through networking

Bill Harding, Contributing Editor

Engineering managers find that the benefits of CAE/CAD networks are more clear-cut than the implementation as they work to link diverse sets of computing resources.

With engineering work groups communicating via yellow Ethernet cables, twisted-pair phone lines, fiber-optic cables, satellite links and floppy disk "walknets," engineering networks occupy a position equal to engineering computers. A network populated with compatible workstations and compute servers supplied by a single vendor and that runs compatible CAE/CAD software seldom presents any networking problems to its users. The problems arise when incompatible computing machines running incompatible CAE/CAD software from a number of vendors attempt to coexist on the same network. Of course, such a situation would be avoided if the network were planned before workstations or software were acquired.

But no network, it seems, has ever been planned. Virtually all network users and all CAE, workstation and network vendors share the same opinion: networks evolve. And they evolve using a wide variety of computing resources—from mainframes to minicomputers to personal computers to engineering workstations to special-purpose computers. A network grows by adding to existing resources, not by discarding anything that's already in place. Although

starting over would be much easier from a technical point of view, doing so would be impractical.

Since engineering managers constantly face the question of how to expand existing resources or how to bring divergent resources together, the status of networking today must be examined, with special focus placed on the options open to the engineering manager who must expand or enhance an engineering network.

■ The evolution of networks

The evolution of computer capability and the plunging prices of computing power are major influences on today's networks, reversing the computer-to-user ratio that existed in the late 1970s and early 1980s. The earliest networks could be characterized as one computer with many users; a single mainframe or large minicomputer served a number of users who accessed the system via interactive terminals. The arrival of low-cost PCs and powerful engineering workstations resulted in a trend toward one computer with one user. Today, with special-purpose computers and compute servers on the network, the typical network has many computers for each user.

As networks moved from one stage

to the next, however, users weren't willing to give up what they already had in place. The one-computer/many-users environment of the early 1980s usually consisted of time-shared, interactive applications running on IBM mainframes or DEC VAX computers, accessed through individual user terminals. Sometimes the network would contain both IBM and DEC computers, with occasional large Crays, loosely coupled via remote job entry or SNA.

When powerful engineering workstations came onto the scene in the mid-1980s, the tendency of the engineering community was to add workstations and PCs to the existing time-share environment. But engineers weren't willing to give up their mainframe capability. They knew how it worked, they trusted it, and all of their applications were there. New applications could go on the workstations and old ones could eventually migrate there, but the mainframes would stay in place.

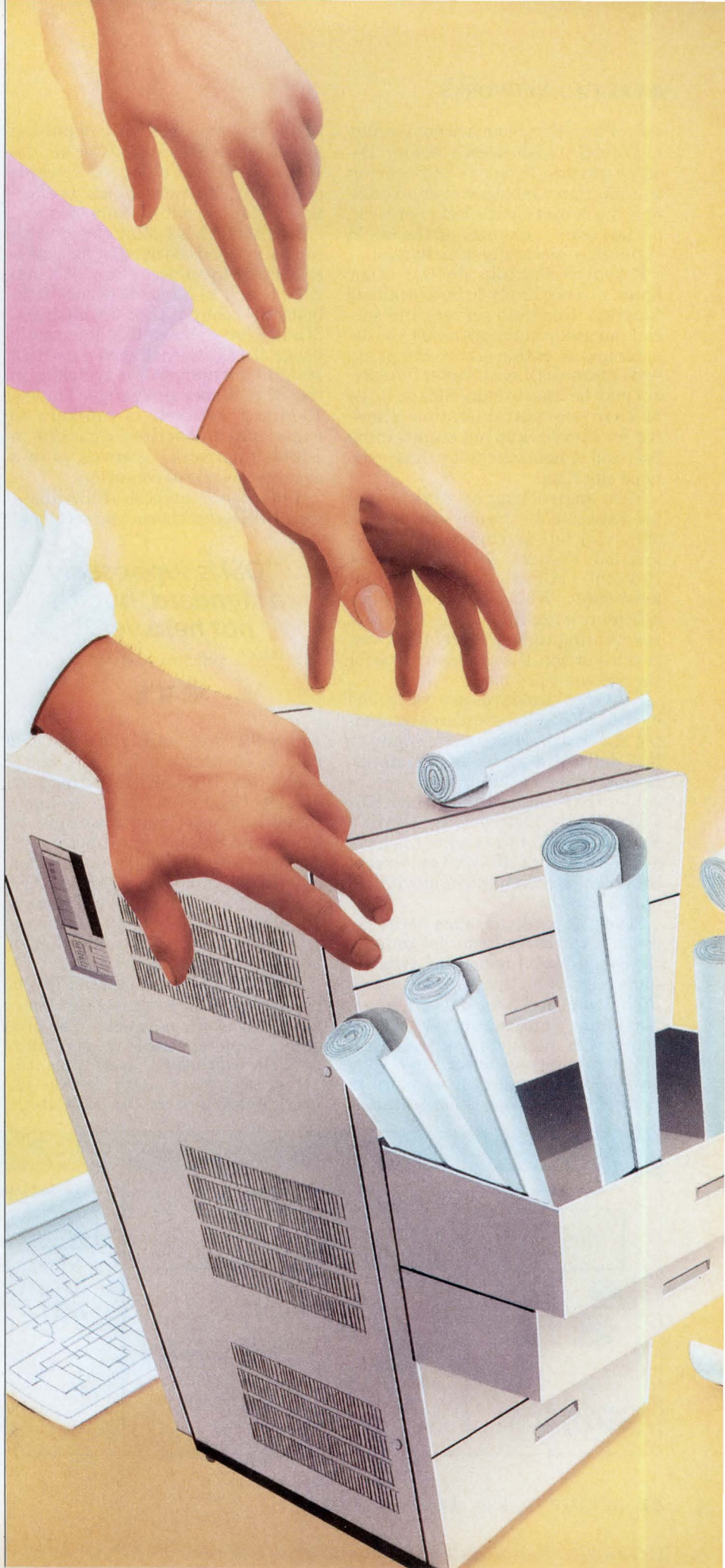
To paraphrase Parkinson's Law, designs will grow to fill the capacity allocated to their creation. Today's huge designs have taxed the capacity of engineering workstations, which has led to the introduction of special-purpose computers and very power-

ful compute servers. But these compute servers and special-purpose computers probably come from different vendors; thus, the software tools aren't compatible. In addition, more engineers must work on the same design and access the same data, which creates a need for better communication between systems. So networks filled with mainframes, workstations, PCs, compute servers and special-purpose computers bring us to the one-user/many-computers ratio that we see today.

■ Deciding on functions

When faced with networking options, you must ask yourself what you want from your network. Do you want that great design team in Europe to work with your local team on some new projects? Do you want to send fully simulated designs to a plant in Asia for fabrication? Do you want all the engineers in your local design group to have access to the engineering department's new simulation accelerator and file servers? Whatever your reasons, they probably boil down to two things: communications and resource sharing.

Communications involves everything from passing a message via electronic mail to transmitting a cus-



■ CAE/CAD NETWORKS

tom chip design from a design center to a foundry's fabrication facility. Designs can pass from one engineering workstation to another over an engineering department's local network, or they can be sent around the world through a hierarchy of networks.

Resource sharing, on the other hand, is more likely to be a localized function. Compute servers and special-purpose computers tend to be departmental rather than company-wide resources. Local cluster file servers may be used to store files on large disks in one central location, allowing for easy backup but maintaining fast and simple access for those who need the files.

Most engineering networks today use Ethernet for the physical process of moving bits and bytes, and Transmission Control Protocol/Internet Protocol (TCP/IP) to control that movement. While Ethernet's capabilities are improving and Ethernet is retaining compatibility from version to version, the same isn't true for the software protocols.

Ethernet standards are controlled by the IEEE 802.3 standards committee. Over the years, that committee has defined a series of standards, ranging from the ubiquitous yellow cable that implements 10BASE5 Thick Cable Ethernet, to 1BASE5 StarLAN. All of the standards have a bandwidth of 10 Mbits/s, except StarLAN, which has a bandwidth of only 1 Mbit/s.

StarLAN received much notice because it can carry Ethernet communications over unshielded twisted-pair telephone lines, according to Rich Brand and Balu Balakrishnan, National Semiconductor (Santa Clara, CA) delegates on the IEEE 802.3 committee. Since most companies have extra twisted pairs in their phone systems, Ethernet can be

run over phone lines without pulling expensive yellow cable. After all, the 10BASE5 Thick Cable costs upwards of \$1.50/ft, but twisted pair is effectively free since it already exists.

But StarLAN's 1-Mbit/s bandwidth limitation, and the need for an expensive bridge to connect a StarLAN network to any 10-Mbit/s Ethernet backbone, is cooling that enthusiasm. Studies have shown that maximum usage of an Ethernet network with a 10-Mbit/s bandwidth is typically in the 30 to 40 percent range. Thus, a 10-Mbit/s network is unlikely to experience an overload condition; a 1-Mbit/s network, however, is in a constant overload condition.

A proposed standard—10BASET—for a 10-Mbit/s Ethernet protocol that

"OSI is supposedly a standard, but it's not here yet."

—Bob Davis, Excelan



will work over unshielded twisted pair is currently before the 802.3 committee. 10BASET is getting a lot of attention, even in preliminary committee meetings, according to Brand and Balakrishnan, because it can run over the same unshielded twisted-pair phone lines as StarLAN, but at a 10-Mbit/s rate. And, with a 10-Mbit/s bandwidth, it requires a much less expensive connection to 10BASE5 backbone networks.

Another standard—10BASEF—is being proposed for connecting Ethernet to fiberoptic networks. The proposed implementation of the standard, for which IEEE approval is still about two years away, would let users upgrade it to the 100-Mbit/s

Fiber Distributed Data Interface (FDDI) methodology. However, since the controller board at each node costs about \$20,000, FDDI can be quite expensive.

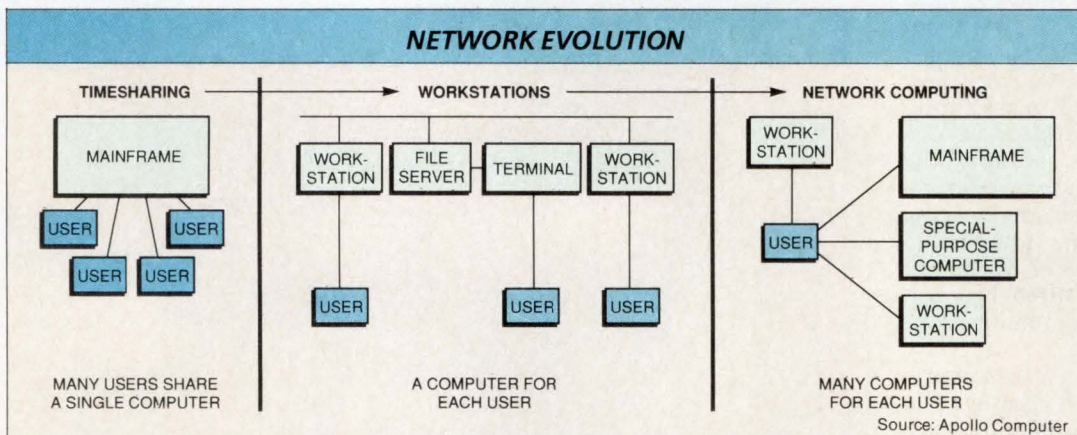
■ Ethernet vs. token ring

Ethernet, however, isn't the only game in town. IBM offers Token Ring, and Apollo Computer (Chelmsford, MA) offers Domain, also a ring network. Rings offer advantages over Ethernet, particularly when network usage gets very high.

Ethernet is a contention-based network: every node has equal access to the network at all times, according to Wes Hilton, manager of integration products at Computervision (Bedford, MA). If two nodes try to transmit at the same time, a collision results, causing both nodes to terminate transmissions, go through a randomizing routine to get out of sync, and try again. This can cause problems, notes Hilton, but only when network usage exceeds about 75 percent, and most engineering applications don't reach that level.

Collisions can't occur on token-ring networks, since only one node can ever attempt to transmit at one time. In this type of network, a token is passed around the ring. If a node wants to transmit, it takes the token, thereby preventing other nodes from also transmitting. If it doesn't want to transmit, the node passes the token to the next node.

Response times are more predictable in a token-ring network than in an Ethernet network, making the token ring adaptable to applications where response time is critical. A token-ring network, however, is more sensitive to system failures within the network, since the failure of one system could break the ring. Ethernet networks, on the other



Early networks grouped users around a single computer in a timeshare environment. Workstations and personal computers brought engineering power to the individual engineer's desk. Networking today lets a single user have access to a wide range of computers.

Networking: a glossary of terms

The networking world has a language all its own, with heavy use of acronyms and abbreviations. The following are some of the more common terms.

Backbone The primary organizational network that ties systems and other networks together.

BSD Berkeley Software Distribution. Networking protocols developed at the University of California at Berkeley for use with Unix.

Bridge A hardware link that connects two similar networks, such as two Ethernet networks.

Ethernet Defines the Physical (Layer 1) and Data Link (Layer 2) levels of the OSI Reference Model (see OSI Reference Model).

FDDI Fiber Distributed Data Interface. Fiberoptics LAN standard that operates at 100 Mbits/s.

Frame The Ethernet communications "packet" that moves information across the physical link from one Ethernet node to another.

FTAM File Transfer, Access and Management. The OSI standard for multivendor file access and transfer. It competes with NFS (Sun's Network File System), which is the equivalent de facto standard under TCP/IP.

Gateway A hardware link that connects two dissimilar networks, such as connecting Ethernet to IBM's SNA.

ISO International Standards Organization. The international organization that's defining the OSI standards for multivendor networking.

GOSIP Government OSI Profile. A subset of the OSI Reference Model protocols adopted for U.S. government network standards.

MAP Manufacturing Automation Protocol. Specifies networking protocols for manufacturing; a subset of OSI protocols.

Network The physical link and control software that lets data be transferred between systems.

WAN Wide area network. A network that connects systems over long distances. Distances can be a few miles or thousands of miles. With satellite links, WANs frequently provide worldwide communications.

LAN Local area network. A network that operates over relatively short distances (typically no more than two or three miles), linking systems within the same building or in nearby buildings.

SAN Small area network. Generally limited to short-range (tens of meters) special-purpose communications functions, such as process-control systems and real-time applications.

Network manager A "traffic cop" that handles the flow of data within a network.

NFS Network File System. A method developed by Sun Microsystems for organizing and managing file transfer over a network. Currently adopted by well over 100 computer vendors.

OSI Reference Model A seven-layer communications protocol model proposed by the ISO; sometimes referred to as the ISO/OSI Reference Model (OSI stands for open system interconnection).

Layer 7: Applications Layer Provides the interface between applications programs and the network.

Layer 6: Presentation Layer A translation function that converts messages from a native format to an international standard format for transmission, and from the international standard to the native format upon reception.

Layer 5: Session Layer Establishes communications paths between systems and terminates them upon completion of transmissions.

Layer 4: Transport Layer Provides reliable data flow between sender and receiver. This layer corresponds to the Transmission Control Protocol (TCP) function in the TCP/IP methodology.

Layer 3: Network Layer Accepts packets (or frames) of data from the Transport Layer and routes them to their destination over all necessary links and intermediate systems as necessary. In the receiving system, this layer simply passes packets to the Transport Layer. Layer 3 corresponds to the Internet Protocol (IP) level in the TCP/IP methodology.

Layer 2: Data Link Layer The interface between hardware and software layers. This is a hardware layer that formats packets for transmission and ensures that they're properly received at the other end. In the receiving node, the Data Link checks packet address fields to see if the local node should receive the packet.

Layer 1: Physical Layer The actual connection to the transmission medium, handling the transmission and reception of raw bits across the medium.

RJE Remote Job Entry (or Execution).

SNA Systems Network Architecture. IBM's proprietary networking format.

TCP/IP Transmission Control Protocol/Internet Protocol. The de facto standard for communicating via Ethernet, corresponding to Layers 3 and 4 of the OSI Reference Model.

Token Ring Endorsed by IBM, it's emerging as the de facto standard for networking PCs.

TOP Technical/Office Protocol. A subset of OSI protocols, similar to MAP, for engineering and office applications.

UUCP Unix-to-Unix Communications Protocol. Commonly used for electronic mail within the Unix community, including universities on public networks.

X.25 A standard adopted by the ISO for wide area networking, as opposed to local area networking. It involves layers 1, 2 and 3 of the OSI model.

X.400 A standard adopted by the ISO for electronic mail handling over a multivendor network.

IEEE 802.3 Ethernet physical standards

The IEEE 802.3 standards committee has defined the following four Ethernet standards:

10BASE5 Known as Thick Cable Ethernet. 10 Mbits/s, baseband, 500-m range. Can be identified by the yellow Ethernet cable.

10BASE2 Known as Thin Cable Ethernet (or Cheapernet). 10 Mbits/s, baseband, 200 m. Runs on a 50-Ω shielded cable. Its major attraction is its lower-cost cable, about 10¢/ft (compared to about \$1.50/ft for Thick Cable).

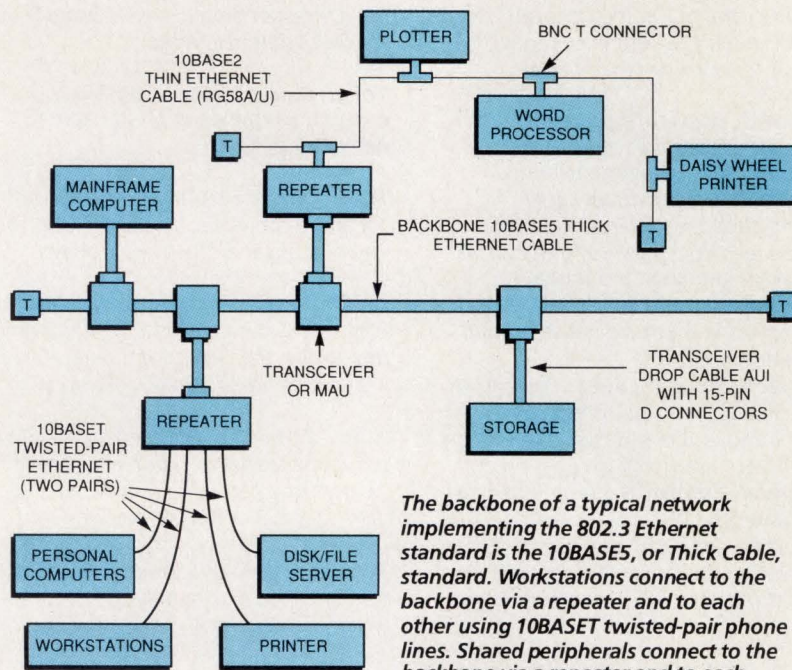
10BROAD36 10 Mbits/s, broadband, 3,600 m. Provides much longer range than both 10BASE5 and 10BASE2 and will run on any broadband cable plan.

1BASE5 Known as StarLAN. 1 Mbit/s, baseband, 500 m. Twisted pair. Networking 10-Mbit/s Ethernet with 1-Mbit/s StarLAN requires an expensive bridge. StarLAN is losing its luster with the pending approval of the 10BASE5 standard.

The following aren't yet IEEE 802.3 standards but are under development by the IEEE 802.3 standards committee:

10BASET 10 Mbits/s, baseband, twisted pair. The majority of the 802.3 committee work is going on here. This standard, once developed, will allow 10-Mbit/s Ethernet over existing telephone wires. Since it's 10 Mbit/s, it can work with a 10BASE5 backbone without an expensive bridge. It should be ready for design in six to nine months, with the official IEEE stamp of approval in 18 months.

10BASEF 10 Mbits/s, baseband, fiberoptics. This proposed standard is in the early stages of development, and it will be about 12 to 18 months before design efforts can be started, and over two years before IEEE approval. There's some controversy revolving around passive hub architecture vs. active hub architecture. The cable plan for 10BASEF could be used for the higher performance Fiber Distributed Data Interface so that users who need even higher performance could upgrade in the future.



The backbone of a typical network implementing the 802.3 Ethernet standard is the 10BASE5, or Thick Cable, standard. Workstations connect to the backbone via a repeater and to each other using 10BASET twisted-pair phone lines. Shared peripherals connect to the backbone via a repeater and to each other via 10BASE2 Thin Ethernet.

Source: National Semiconductor

hand, are generally insensitive to node failures, since there's no inter-node communication other than the passing of applications data.

■ OSI or TCP/IP?

The whole purpose of networking is to let systems communicate and share resources. At the physical level, systems can be connected to form networks, similar networks can be connected by bridges, and significantly different networks can be joined by gateways.

Since the early 1980s, TCP/IP has been the de facto standard for communicating over heterogeneous Ethernet networks. First introduced in the 1970s by the Department of Defense, TCP/IP gained commercial acceptance when it was incorporated into the Unix 4.2 BSD kernel in 1982, and later when 4.2 BSD linked TCP/IP with Ethernet. Since then, TCP/IP has grown in strength.

In 1984, before TCP/IP became popular, the International Standards Organization (ISO) proposed a seven-layer protocol called the ISO/OSI (open systems interconnection) Reference Model. The OSI model addressed many of the issues that plagued networks at the time of its early definition. A hot issue in the networking community today concerns the migration to the OSI standard from TCP/IP.

Bob Davis, product-line manager at Excelan (San Jose, CA), for one, questions such a migration. "OSI is supposedly a standard, but it's not here yet," he says. "TCP/IP is the least common denominator when tying heterogeneous networks together; it's a de facto standard; it's here now; it's mature; and it's rapidly filling all of the gaps that OSI supposedly addresses."

One OSI strength is its File Transfer, Access and Management (FTAM) facility, through which it addresses file access across a network. FTAM has specifications that are better, particularly in the area of electronic mail, than those of the Network File System (NFS), the equivalent de facto standard in the TCP/IP and Unix worlds. NFS was developed by Sun Microsystems (Mountain View, CA), has been around for several years, however, and is constantly being improved.

So, while some of OSI's features appear to be somewhat better than those of TCP/IP, it's unlikely that OSI will soon replace TCP/IP, if ever.

**INTEL'S 80960
ARCHITECTURE
IS THE
SUPERHIGHWAY
FOR EMBEDDED
CONTROL.**

AND IN 1989
WE'RE RAISING
THE SPEED LIMIT.



66* MIPS by 1989. Over 100 MIPS in the 1990's.

At those speeds, Intel's new 80960 architecture is going to be miles ahead of other embedded control solutions. By enabling the execution of multiple instructions per clock, the 80960 architecture goes beyond simple RISC. Thus raising both the speed limit and your expectations.

But you don't have to wait to get on this virtual superhighway for embedded control. Because Intel offers a family of processors that you can drive away with today. All based on the 80960 architecture.

Starting with the 80960KB. The only 32-bit embedded control processor with a complete Floating-Point coprocessor. All on a single chip.

Then there's the 80960KA. A single chip 32-bit embedded control processor with a direct upgrade path to 66 MIPS in 1989. Available in more economical versions, without Floating-Point,

at 16-, 20- and 25 MHz.

And for military applications, Intel offers the 80960MC. The only 32-bit embedded control processor with hardware multiprocessing capabilities on a single chip.

We also supply all the development support you need. Including high-level languages for a variety of industry-standard hosts, and the ICE™ 80960 development tool.

The result is the world's first fully supported 32-bit architecture designed exclusively for embedded control.

So why wait any longer? Our comprehensive 80960 brochure gives you the complete story. To receive it, just call (800) 548-4725 today and ask for Lit. Dept. #W475. With one phone call, your project can be on the road to 32-bit embedded control.

And ready to accelerate.



intel®

© 1988 Intel Corporation

*Sustainable MIPS on-chip.

CIRCLE NO. 16

■ CAE/CAD NETWORKS

The question, according to Davis, shouldn't be one of replacing TCP/IP with OSI, but of running both at the same time on the same network.

Excelan's strategy is to run both on the same network by providing controllers that automatically and transparently determine whether a command or message uses the OSI protocol or the TCP/IP protocol. Excelan customers can replace TCP/IP with OSI, or both protocols can continue to run on the same network.

■ "The network is the computer"

Network vendors and workstation vendors have recognized the movement to heterogeneous networks and have developed their networking strategies and products accordingly.

"The network is the computer," states Sun Microsystems in a trademarked phrase. To support this contention, Sun developed the Open Systems Network (OSN) philosophy, designed not only to let diverse systems work together in a single net-

work, but to also make the entire network look like a single computer to the user. OSN is made up of two parts: open network computing (ONC) and a network/extensible window system called X.11/NeWS, which is a merging of Sun's NeWS windowing system and Version 11 of the X Window System.

ONC is designed to address three networking problems: resource access, application design and development, and network administration. Through a layered process, ONC lets users access any network resources, from simple files to special-purpose computers, as if the resources were resident on the user's local computer.

At the top of the ONC hierarchy is the applications level. One such application is Sun's NFS, which is rapidly becoming a standard in its own right. NFS provides the ability to access files anywhere in the system and to let different computers share files. Vendors also may develop applications at this level.

Just below the application level is a remote procedure call (RPC) facility, which accesses remote resources and executes portions of an application on another network system.

Below the RPC level is a parameter translation level called XDR (external data representation). At this level, data can be passed between machines that use different data representation formats.

The second part of OSN, X.11/NeWS, can be distributed anywhere on the network, since it's independent of operating systems, hardware and screen resolution. Sun's aim is to make X.11/NeWS a network resource, just like a piece of network hardware.

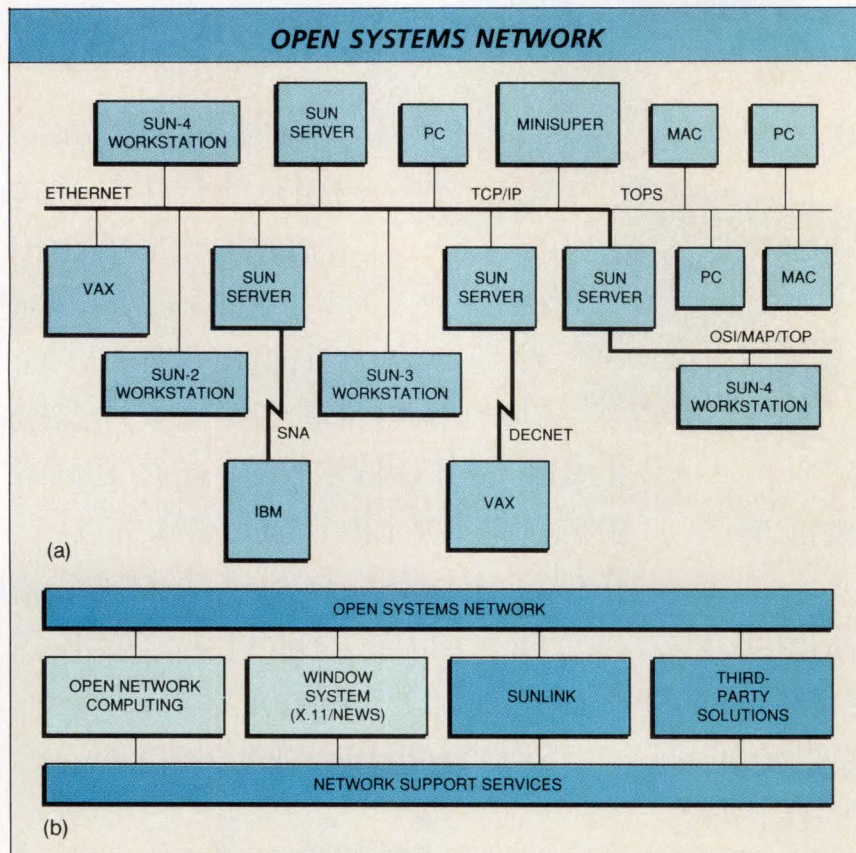
■ The last piece of the puzzle

Hewlett-Packard's Colorado Networks Division (Fort Collins, CO) bases its Advancenet on the idea that a network starts with a mainframe, possibly a minicomputer, and some PCs in place. "When you add engineering workstations to the network, you must first ensure that the existing network is still functional," says Dave Morse, HP's engineering solutions manager. "You must provide file-transfer capability to move files back and forth, and you must provide a terminal emulation mode to maintain access to the applications on the mainframe."

One motivation for moving out of the time-share environment, according to Morse, is to take advantage of the competition in the computer market. Adopting a networking scheme that's vendor-specific defeats that purpose, he says, so users should stick to standards that let them take advantage of the most cost-effective engineering solutions available.

Advancenet supports what HP considers to be the dominant standards in networking: the OSI Reference Model and IBM's SNA. It supports both the original Ethernet and the more recent IEEE 802.3 specification at Layers 1 and 2 of the OSI Reference Model. Advancenet also includes HP StarLAN and HP StarLAN 10 for LANs; IEEE 802.4 for ARPA (the Department of Defense's Advanced Research Projects Agency) and MAP (Manufacturing Automation Protocol) networks; and the HP Private Packet Network, which is based on the X.25 standard.

Like HP, Apollo focuses on the fact that networking is considered only after all the other pieces are in place. "Networking is the last frontier of



Sun Microsystems' Open Systems Network (OSN) supports a heterogeneous network (a). It works on the premise that a network must build on any existing installation and be compatible with future installations. Major components of OSN (b) include Sun's open network computing (ONC) and a window system, X.11/NeWS, which is a merging of X Window System Version 11 and Sun's NeWS.

Distributed fault simulation elicits supercomputer performance from CAE network



Networks of CAE workstations aren't limited to the tasks originally envisioned for them. They can also be used as loosely coupled parallel processors

that can cost effectively reduce the run time of compute-intensive operations.

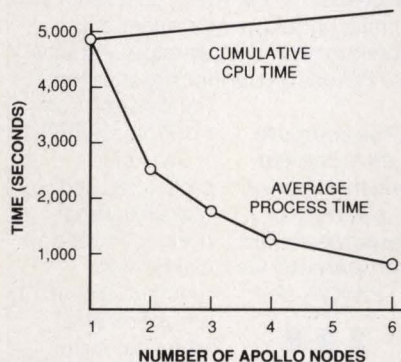
Accurate fault simulation is one operation that can benefit from such parallel-processing schemes and is therefore contributing to an industry trend toward more effective use of network resources. Verifault-XL, the latest fault-simulation product from Gateway Design Automation (Westford, MA), for example, can run on networks of standard workstations, achieving an almost linear reduction in processing time as network workstations are added.

Designers use fault simulation to determine the efficacy of sets of test patterns that they've developed using a logic simulator. The test patterns, if proven adequate, can then be used in manufacturing and field-service test equipment. Unfortunately, large numbers of circuit nodes (and hence potential faults) coupled with the large numbers of test patterns necessary to exercise the nodes can make fault-simulation execution quite slow.

■ Random fault sampling

Statistical fault-simulation schemes can quickly provide a rough indication of the effectiveness of a set of test patterns. Verifault-XL, for instance, includes a random fault-sampling feature that lets users simulate only a small percentage of the total number of possible faults. Obtaining full confidence in a test-pattern set, however, requires an accurate, deterministic fault simulation.

To perform such a simulation, a fault simulator must be able to simulate a stuck fault (that is, a permanent logic 1, 0, or for MOS circuits, open condition) at each circuit node. The total time required for fault simulation is dominated by the " $F \times T \times P$ " time, where F is the total number of faults to be simulated, P is the total number of patterns, and T is the average time required to simulate a



Doubling the number of Apollo workstation nodes available for parallel processing nearly halves the time required for fault simulation. The results of a 6,600-gate circuit running at 100 percent fault set show a slight rise in the cumulative CPU time, which is caused by interprocessor communication and is limited to 5 to 10 s per processor.

faulty machine for each pattern.

For circuits of even moderate gate count, fault simulation, therefore, is computationally intensive. One 6,600-gate circuit evaluated by Gateway exhibited 23,741 faults. Achieving 68 percent fault coverage of this circuit required 104 test patterns.

Hardware accelerators have provided one means of speeding up accurate, deterministic fault simulation, but to use them, you must buy expensive, dedi-

cated equipment. In contrast, if you use an existing network of general-purpose workstations to run a distributed fault-simulation package, the hardware is essentially free because fault simulation can run on the network at night.

■ Parallel-processing tasks

The operation of Verifault-XL illustrates how networked workstations can accomplish parallel-processing tasks. Verifault-XL lets multiple workstations work in parallel on a single simulation. For logic circuits of 1,000 gates or more, adding additional workstations results in a nearly linear reduction in run time despite the overhead associated with interprocessor communication.

To run Verifault-XL on a network, the user interfaces with a parent processor, which serves as the user's single point of entry and exit. The parent processor (which may be any workstation in the network) accesses the circuit model and stimulus vectors for the circuit to be simulated. Next, the parent passes circuit information on to several children processors, designated by the user.

Each processor (including the parent) then performs fault simulation on the entire circuit for a unique, nonoverlapping subset of the total fault set. This step essentially divides the dominant $F \times T \times P$ time by the number of workstations available for distributed processing. The time spent modeling and post-processing and the total time spent simulating a good machine for each pattern also add to the total fault-simulation time.

When each processor finishes its simulation, it returns summary information to the parent, which merges the simulation data from all processors into a results file. The user gets supercomputer performance from a network of standard workstations.

Prabhu Goel, PhD, president, Gateway Design Automation

computing," says Bob Chiras, networking marketing manager at Apollo. "We get to the user last, after most of the computing decisions that have made, so we have the least influence on the user's environment. The networking vendor's job is to coexist with the decisions already made and to make the user's investments in con-

nectivity correct."

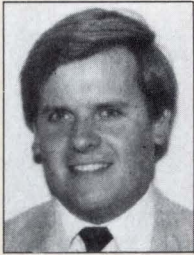
Apollo's networking offerings span the full range of commonly used protocols and network configurations, including Ethernet 802.3 and the Apollo Domain ring.

For application development, Apollo's Network Computing System considers the engineering workstation

the integration point, or unifying technology, for network computing. It provides the foundation for a heterogeneous network that supports distributed applications and services across one network or a group of interconnected networks.

The networking goal of Digital Equipment Corp (Maynard, MA) is to

Networking innovations maximize CAE/CAD performance



The growing need to proliferate CAE/CAD resources among as many engineers as possible has driven the demand for affordable desktop workstations. At the same time, CAE/CAD applications' hunger for computer performance is greater than that of almost any other class of software, and the graphics- and compute-intensive nature of CAE/CAD is continuing to increase. These factors have pushed computer hardware to its performance limits. Through networking innovations, however, the CAE/CAD environment can reach effective performance levels at the right price.

"Networking innovations" refers to the creation of a cost-effective CAE/CAD environment that satisfies the computer-performance requirements of the different stages of the design cycle. Digital simulation requires the highest CPU (or Mips) performance. Design capture and CAD applications require the maximum level of graphics performance. And analog simulation and printed circuit board routing require very high floating-point performance (Flops). Because no one affordable workstation can meet all of these CAE/CAD requirements, the compute environment must consist of a variety of resources linked transparently via a network.

One method on which to model a networked CAE/CAD environment is the desktop/server approach—the approach taken by Daisy Systems (Mountain View, CA). Graphics-intensive activities such as schematic capture, simulation analysis and printed circuit board design are supported on the desktop computer. CPU-intensive and floating-point-intensive activities are allocated to specialized resources shared over the network, such as hardware accelerators and high-Mips servers, respectively. This approach provides the individual engineer with low-cost, dedicated computer power on the desktop as well as access to more expensive computer resources that are shared with other design team members.

To give the engineer the ability to in-

teract with the accelerator or server as if the applications were running on the desktop workstation, Daisy has developed a specialized communication protocol called Inter-Process Communication (IPC). Because it's optimized for the CAE/CAD environment, IPC provides a high level of functionality.

IPC is a Session Layer protocol (Layer 5 in the OSI model), optimized to establish cooperation between applications running on Daisy workstations and those running on accelerators and servers. IPC runs on the industry-standard

The compute environment must consist of a variety of resources linked transparently via a network.



Transmission Control Protocol (TCP). Daisy's IPC protocol is used typically by engineers sitting at a workstation running a digital simulation on a Megalogician or Gigalogician accelerator. The accelerator implements the actual simulation algorithm in micro-code at speeds greater than those of general-purpose computers. With the IPC protocol establishing and maintaining a link between the accelerator and the desktop workstation, the engineer can interact with the simulation in real time with little thought that the simulation is being carried out elsewhere.

IPC also supports Daisy's analog simulation engine, DSpice, which requires strong floating-point performance. DSpice performs best on the Sun-4-based XL Server or on a VAX. For engineers running DSpice on a VAX, IPC maintains the link between the engine and the graphics interface running on the engineer's desktop.

Because of its transparency, many of the engineers who use IPC may not even realize it. But the benefits of such a communications protocol are evident. It offloads CPU-intensive tasks such as analog or digital simulations to powerful network resources, yet maintains interactivity. This reduces the CPU load on the local workstations, which minimizes cost per seat. Powerful resources are easily accessible to the entire network, which maximizes their availability and cost effectiveness.

move everyone to OSI. As a means to this end, the company announced in August its enterprise-wide networking product line. These products are designed to help integrate networks and computers throughout an organization. DEC recommends that networks be organized with local VAX clusters serving individual engineering groups, with the local cluster connected to a backbone Ethernet cable for company-wide networking, an approach DEC's enterprise-wide products support.

The new product line includes communications servers, networking software and gateways that connect dissimilar networks. The DEC MicroServer is a MicroVAX II-based server that provides four times the performance of DEC's previous server. The DECrouter 2000 software connects DECnet users to high-speed telephone lines. The X25router 2000 software gives DECnet users access to wide area networks using the X.25 protocol. And the SDV11 is a high-speed synchronous interface that provides two lines that run different applications, as well as providing access to networks using the DECnet, X.25 or SNA protocols.

Supporting OSI is DEC's VAX FTAM software, which complies with ISO/OSI Reference Model specifications. Since OSI isn't yet an industry standard, DEC also supports numerous de facto standards, including TCP/IP and Ethernet.

■ CAE vendors provide support

Most CAE vendors prefer to let their workstation vendors or independent networking vendors provide networking hardware and software, while they develop applications that will run on those networks.

Daisy Systems (Mountain View, CA) believes that networking has three functions in the engineering environment: meeting engineering performance needs, tying members of a design team together, and tying the engineering environment to the corporate environment.

Performance needs refer to those tasks that can't be handled on the engineer's PC or engineering workstation. Such tasks would include long simulation runs, IC or printed circuit board layout, centralized file storage, and shared peripherals such as plotters and printers. Daisy's applications tend to support interactive design on the engineer's desk and batch-mode applications on servers.

Kevin Woods, BSEE, product manager, workstation marketing, Daisy Systems

Why more companies choose high-speed channel interfaces from KMW Systems' Auscom line.

The Auscom line of channel interfaces from KMW Systems has been outselling the competition for more than 12 years. In fact, we now have an installed base of more than 4,000 units. And for good reason: KMW Systems offers the broadest range of IBM and compatible mainframe channel connections available anywhere, backed by a dedication to service and support that's unsurpassed.

An unlimited variety of applications.

KMW board-level and system-level channel interfaces can connect your IBM or compatible mainframe to Ethernet, X.25, T-1, IEEE-488, high-speed printers, non-IBM computers, custom networks, other mainframes, high-resolution graphics devices, and optical disks.

Our interfaces appear to the mainframe as standard control units, so no modification to host software is required. And our channel interfaces can emulate multiple controllers and support different devices and protocols simultaneously for maximum productivity.

Channel connections for virtually any configuration.

KMW Systems' channel interfaces are offered on popular, industry-standard bus structures — VME, Multibus, and Q-bus. Additionally, KMW Systems offers a board-level channel interface that uses a programmable parallel interface instead of a bus connection. This product depth ensures that OEMs can find the board-level product that best suits their system integration needs. Every Auscom channel interface allows attachment to an IBM or

compatible channel, with data transfer rates of up to two megabytes per second.

Reliability no one else can match.

KMW Systems' channel interfaces have a history of reliability, with field-tested MTBFs as high as 19 years.

Our engineers are ready to work with you to ensure proper installation and operation of your channel interface. We also offer training classes, consulting services, and a free technical support hotline. That's the kind of service that's made us number one.

For complete information on KMW channel interfaces, protocol converters and graphics processors, call the toll-free number below. Or write KMW Systems, 6034 W. Courtyard Drive, Austin, TX 78730.



 **KMW
SYSTEMS
CORPORATION**

(800) 531-5167
In Texas, (512) 338-3000

Diverse circumstances influence individual networking decisions

How do networks get started? The answers are as varied as the companies that use them. The examination of three networking examples illustrates the influences on network decisions. The first example involves a start-up that's designing its first product, a supermicrocomputer. The second involves the application-specific IC division of a very large semiconductor manufacturer. This division was faced with merging two product lines. The third example involves a giant manufacturing company that must manage the design efforts of some 90,000 subcontractors.

■ The start-up

Clustrix (Santa Clara, CA) started out as a consulting company, but gave up consulting to pursue the design and manufacture of supermicrocomputers. The company's engineering network consists of six Apple Macintosh computers, six IBM PC ATs, a Sun workstation and an Apollo workstation. As one might surmise, the network evolved rather than was planned, but it gets the job done.

"As a consulting company, our objective was to produce thorough reports for our clients," says Douglas McTavish, vice-president and one of the founders of Clustrix. "We chose the Apple Macintosh for its text processing, spreadsheet and graphics capabilities."

When Clustrix undertook the design of its first product, it had to select design tools and the computers to run them, since few such tools run on the Macintosh. The Clustrix design philosophy, based on mainframe computer design techniques, played a major part in how those selections were made. Among these is the company's method for creating and entering designs into the design data base.

"We develop our ASIC designs as a set of equations that we enter directly into the design data base," says McTavish. "ASICs constitute about 90 percent of our design effort."

Since the ASIC design files are equations that are created and edited using commercially available text editors rather than graphics editors, it wasn't necessary to have a large number of graphics workstations. Clustrix added ATs as individual engineering stations because of their greater compatibility with available engineering tools. The company chose a suite of design auto-

mation tools from Silvar-Lisco (Menlo Park, CA), thus dictating that workstations capable of running simulators and printed circuit board design tools be part of the design environment. A Sun workstation was added to run the simulators, and an Apollo workstation was added for printed circuit board design.

The Macintoshes are connected by Apple Talk; all other machines are connected by Ethernet, with a bridge between the two. Designers can run simulations by logging onto the Sun workstation via the network and run the simulations from either a Macintosh or a PC. When it's time to move an ASIC design from the local environment to a foundry for final simulation and fabrication, the move is accomplished via magnetic tape rather than by a network link.

■ Networking the networks

The network at National Semiconductor (Santa Clara, CA) is what one would expect: individual engineering groups using a variety of engineering workstations are networked together within their own groups and may be supported by local NAS mainframes (National Advanced Systems' IBM-compatible computers) or VAX minicomputers. Protocols such as TCP/IP (Transmission Control Protocol/Internet Protocol) and DECnet are used to link various computers.

Local clusters are connected to the company's backbone network, which links various National facilities throughout the world. In addition, gateways provide links from the backbone into public networks.

When National acquired Fairchild Semiconductor last year, Roy McGuffin, director of design automation at National's ASIC Division, was faced with a problem: National's ASIC design network had to be merged with Fairchild's network. In addition, National's customers, using a variety of design automation tools, had to be able to work with the National foundry for the production of their ASIC designs.

National's system was based on NAS mainframes, and the Fairchild system, FairCAD, was based on VAX VMS. Both systems worked but were somewhat inflexible in how they interfaced to customers' design tools. So National decided not to simply merge the two networks. Instead the company developed DA4, a design environment that's

more compatible with customer design environments and that takes advantage of existing workstation and networking standards.

According to McGuffin, the most important thing that National did was to base DA4 on existing standards, in particular on the Electronic Data Interchange Format (EDIF) standard. An EDIF "backplane" is the key to integrating diverse systems and design tools. All of the customer design tools and National design center tools plug into one side of the EDIF backplane, and the National foundry tools plug into the other side.

A design may be created and a net list generated on any CAE workstation, as long as it can produce a net list in EDIF 2.0 format. The EDIF net list then becomes the universal language for accessing all National simulation, layout and verification functions.

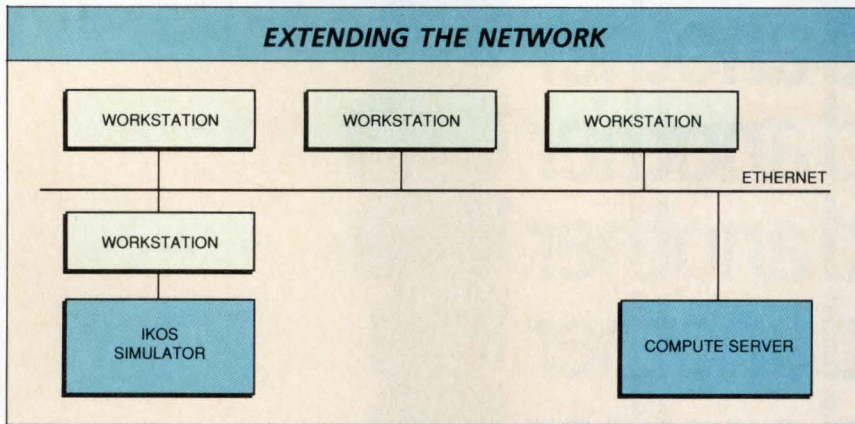
■ The giant influence

General Motors has a somewhat different problem: standardizing the way outside contractors work for GM. GM has approximately 90,000 approved subcontractors, and they produce about 80 percent of every new GM automotive design.

GM's problem is one that every engineering manager faces: compatibility of information. GM decided, therefore, to implement a program, called the C-3 Data Pipeline, that will provide "art to part" consistency of data generation, data transmission and data interpretation. When implemented, outside contractors will be required to provide their design inputs in an electronic format that's compatible with the C-3 Data Pipeline and therefore compatible with other design and fabrication tools. GM estimates that it will spend hundreds of millions of dollars implementing this program over the next five years.

The C-3 Pipeline is both a very large design network and a design philosophy. Cadam (Burbank, CA), a major supplier of mechanical and printed circuit board design software to GM, was selected as a strategic partner to help implement the program.

"The C-3 Data Pipeline doesn't mandate anything that we hadn't already planned," says David Brazier, director of CIM marketing at Cadam. "The whole philosophy is to apply standards that already exist in order to achieve greater compatibility and portability."



Special-purpose and general-purpose compute servers extend the capabilities of an engineering network. In some cases, the compute server connects directly to the network. Some special-purpose computers, such as the Ikos simulator, attach to the network through an intermediate workstation.

The latter two network functions relate to communications: communications among design team members working on elements of the same task, and communications between design teams and other departments such as MIS and manufacturing.

Cadnetix (Boulder, CO), like most vendors, usually integrates its CAE/CAD tools with existing customer engineering environments. But the company believes that customers have to change how they do their job. The mere act of integrating CAE/CAD tools into an engineering department should cause changes. The problem is getting both the customer and the CAE vendor to understand what those changes are.

When integrating into an existing environment, Cadnetix usually deals with the MIS department, since new computers will be hooking into the companywide network. Cadnetix provides turnkey systems with its software on Sun workstations and incorporates Sun networking tools, including NFS for file access and XDR for data compatibility.

Cadnetix has found that integrating the engineering environment into the overall corporate network runs into more political resistance than technical problems. Companies demand that paper be moved when a design is handed to manufacturing.

Electronic mail may be a first step to corporatwide networking. But MIS managers are reluctant to give nonprofessionals—that is, non-MIS professionals—access to the corporate mainframes. The managers wonder, “Will those engineers do weird things with my systems?”

But political resistance isn't the

only problem. There are ample technical problems within the engineering network itself, according to William Loesch, president of Ikos Systems (Sunnyvale, CA). Ikos provides high-performance simulators, including hardware simulation accelerators, for incorporation as a special-purpose computer on a client's engineering network. The Ikos system must integrate into the client's network because Ikos doesn't offer the front-end products.

The physical process of moving bits and bytes around in a network isn't a problem, according to Loesch. Ethernet does that quite well. The problem is being able to do something with the information once it arrives at its destination.

The difficulty is caused by the way different computer architectures handle data internally, Loesch explains. A “byte-swapping” problem results, not from data in pure binary or pure ASCII, but from mixed binary and ASCII files. Since a schematic is often a mixed ASCII/binary file, with graphics information in binary and text in ASCII, a schematic started on one workstation may cause problems if edited on a different architecture, even though the applications software is from the same vendor.

■ Where to from here?

It looks like networks will be with us for quite some time, although the transmission media may change. Ten-Mbit/s twisted-pair Ethernet networks are probably less than two years away. Fiberoptic networks, while expensive today, will probably follow the path of all other technological advances and come down in

price. And perhaps a future network will consist of portable workstations connected by cellular telephones or even satellites.

Will we solve the problems of moving information between diverse systems in a meaningful manner? The answer may lie in the recent movements toward cooperation among electronic CAE/CAD companies. The Electronic Design Interchange Format (EDIF) finally works and is being supported by several CAE vendors. And the CAD Framework Initiative (CFI) announced at the 1988 Design Automation Conference could solve many data-interchange problems.

The best advice to the engineering manager, however, is stick with the standards that exist today. You can always find a networking technology that may be somewhat better than the one everyone else is using, but what happens when you can't expand your network because no one supports the technology you've chosen? As one network user puts it, “Beware of the vendor who wants to control the universe!” Like it or not, networking is one area where it pays to follow the crowd. □

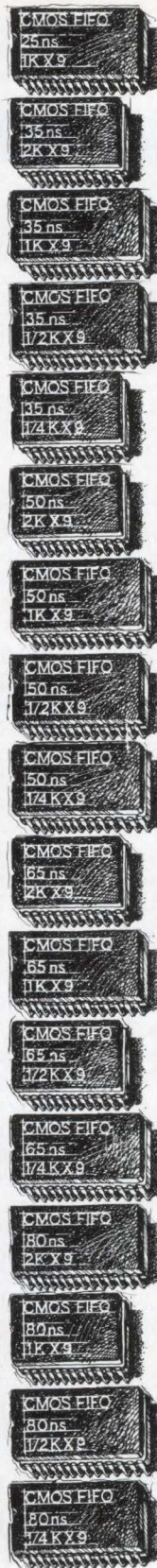
For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Apollo Computer	
(508) 256-6600, ext 4191.....	Circle 260
Cadnam	
(818) 841-9470, ext 372.....	Circle 261
Cadnetix	
(303) 444-8075.....	Circle 262
Clustrix	
(408) 970-0270, ext 16.....	Circle 263
Computervision	
(508) 275-1800, ext 6407.....	Circle 264
Daisy Systems	
(415) 960-6388.....	Circle 265
Digital Equipment Corp	
(603) 881-2934.....	Circle 266
Excelan	
(408) 434-2313, ext 120.....	Circle 267
Gateway Design Automation	
(508) 692-9400.....	Circle 268
Hewlett-Packard	
(303) 229-3800, ext 2220.....	Circle 269
Ikos Systems	
(408) 245-1900, ext 541.....	Circle 270
National Semiconductor	
(408) 749-7406.....	Circle 271
Silver-Lisco	
(415) 853-6396.....	Circle 272
Sun Microsystems	
(415) 960-1300.....	Circle 273

Please rate the value of this article to you by circling the appropriate number in the “Editorial Score Box” on the Inquiry Card.

High 503 Average 504 Low 505

Announcing another
and another
and another
and another
and another
and another
and another
and another
and another
and another
and another
and another
and another
and another
and another
and another
and another
and another
and another.



AMD is introducing 17 low power CMOS FIFOs.

They come in a broad range of speeds and densities. Even architectures for specialized applications.

And they're all available now.

Call us at (800) 222-9323. Ask for the Specialty Memory Data Book and find out about your favorite FIFO. And another and another and another.

Advanced Micro Devices 

901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088.

© 1988 Advanced Micro Devices, Inc.

Caching designs eliminate wait states to relieve bottlenecks

Alternative approaches to cache architectures present a range of trade-offs in cost, performance and complexity.

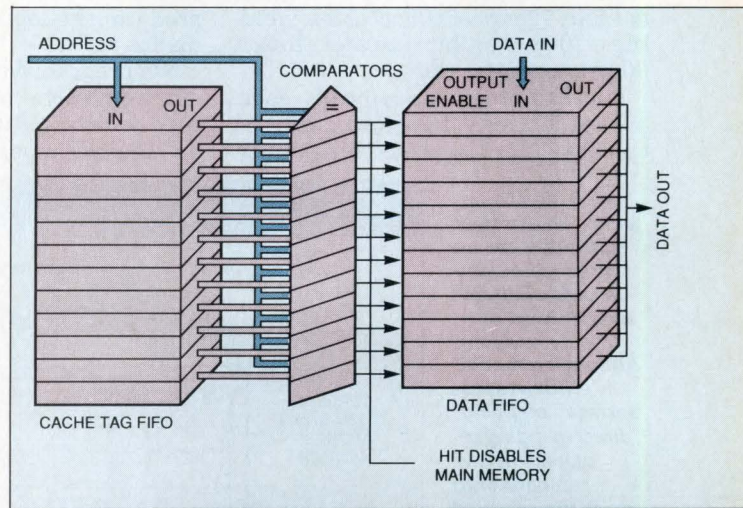
Richard Gregory, BScEE

The demands that today's high-speed processors place on main memory can't be economically met without severe price/performance trade-offs. Designers have had to either use dynamic memory and insert wait states in CPU memory accesses or use high-performance static memory and pay a premium price. There is, however, a third alternative: A relatively small static memory cache can be added to dynamic memory to allow high average read-access bandwidth with relatively little extra cost.

By exploiting the repetitive and sequential nature of software execution and data base manipulation, caching enables a small amount of very fast static memory to improve the perceived performance of sluggish dynamic memory. Memory systems incorporating cache devices can eliminate wait states for over 90 percent of all accesses and can do so at a fraction of the cost of equivalent high-speed static memory. The resulting increase in memory access bandwidth is particularly important in real-time systems, multiuser/multitasking systems, data base manipulation, multiprocessor systems and any application that's memory-intensive and time-critical.

Because cache systems increase bandwidth so efficiently, they've become very much in vogue. Various manufacturers provide processors with on-chip caches, chip sets to implement full off-chip caches, and cache boards that "turbo boost" existing memory systems. And one standardized bus, Futurebus, includes provision to exploit all cache features. Each variation on the cache

Richard Gregory is technical director at Ovation Systems (Great Milton, Oxfordshire, UK).



One common form of caching uses associative mapping, in which a FIFO-like cache-tag memory stacks records of memory locations in order of access.

■ CACHING DESIGNS

theme presents its own cost, performance and complexity trade-offs.

Cache systems increase the effective speed of main memory by providing the CPU with a copy of the most frequently used data more quickly than the memory the cache supports. If more data is prefetched than requested, cache memory can be further enhanced and can provide a very high hit rate to sequential accesses.

Cache systems consist of a cache-tag RAM and an associated data RAM. The cache-tag RAM contains records of addresses accessed on previous cycles together with validation bits indicating that a valid cache entry has been made. The data RAM contains the corresponding data associated with those addresses. When subsequent addresses match a validated cache-tag entry, a cache hit is indicated. The main memory is then bypassed and the corresponding data retrieved from the cache data RAM.

■ Software properties

Because most software routines spend considerable time in loops repeatedly executed from the same memory location, it's very likely that program data will be found in the cache from previous passes through the loop. Cache systems exploit this property to provide high hit rates for program data accesses. A 32-kbyte cache will typically contain program data for 70 percent of accesses, yielding a 70 percent hit rate and, thus, a 30 percent miss rate.

Because programs typically operate sequentially, the cache miss rate can be reduced by prefetching multi-

ple data words from main memory and entering them into cache. Also, by expanding the data width—or line length—of prefetched data, the miss rate is reduced in almost direct relation. Memory systems designed with a wide line length thus give very high hit rates.

Since most software loops and subroutines typically reside within less than 1 or 2 kbytes of memory, cache memory doesn't have to be particularly large to produce noticeable improvements. The 68020/68030 CPUs from Motorola (Tempe, AZ), for example, have only 256 bytes of cache memory yet achieve significant per-

**Address and data
storage methods
differ in how
the cache-tag entries
relate, or map,
to the address space
they serve.**



formance enhancements over similar CPUs without caches. Increasing the cache size will improve the hit rate, but for most applications a cache size of around 16 to 32 kbytes will produce the optimum cost/performance ratio.

Nonprogram data fetches also benefit from cache memory. Variables used within software routines may be accessed repeatedly with a high

probability of being provided from cache. Similarly, data base manipulation will typically concentrate on relatively small parts of a data base, and these will mostly be contained in the cache. But a simple cache memory is unlikely to dramatically benefit systems in which large amounts of data must be written into main memory without being read back, or if the memory accesses are unlikely to be sequential or repeated locations.

■ Direct vs. associative mapping

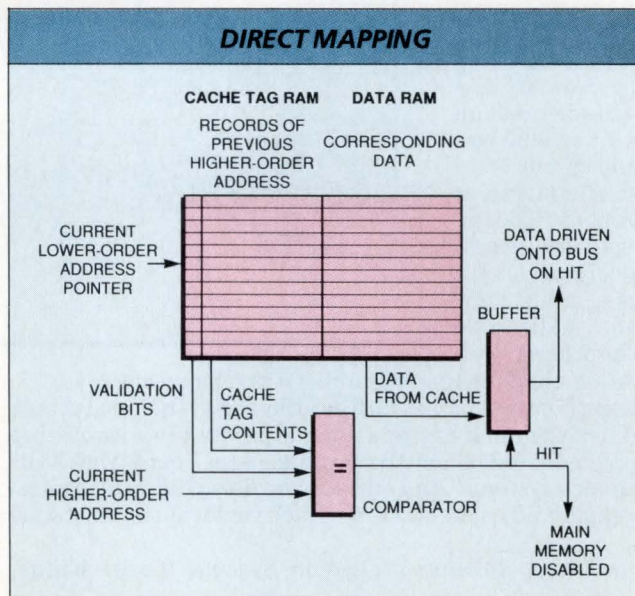
There are a number of ways in which a cache can maintain a store of the addresses and corresponding data of the most commonly used memory locations. Each storage method differs in how the cache-tag entries relate, or map, to the address space that they serve.

Associative mapping stores cache-tag entries in the order in which they last occurred, with the records stacked in a specialized first-in, first-out (FIFO) memory. This method provides very efficient mapping since it maintains a complete record of all the most recently accessed memory locations. It's difficult, however, to implement on a large scale because all the cache-tag entries in the FIFO must be checked to determine whether they match any subsequent cycles. This checking can be done in VLSI circuitry, but it can't provide for many entries because a dedicated comparator must be attached to every cache-tag location to determine whether any of the cache-tag locations have hit.

Unlike associative mapping, direct mapping allows the use of static RAM devices to hold the records of the addresses that are most commonly accessed. Direct mapping is thus easier to implement. The records aren't stored strictly in order of occurrence, but in locations that have a direct relationship to the address in main memory.

With direct mapping, lower-order address lines are used to retrieve a record of the higher-order addresses of previous cycles from high-speed static memory. If this record matches the present higher-order addresses and the validation bit is asserted, the cache tag indicates a cache hit. Data is then retrieved from the cache data RAM in preference to the main memory. If the addresses don't match or the validation bit isn't set, a cache miss is indicated and a new cache entry is made, consisting of the present

With direct mapping, conventional static RAM can be used to hold the records of the addresses most commonly accessed. Although not quite as efficient as associative mapping, direct mapping requires just one comparator to check the retrieved cache tag.



Evaluating cache performance

Of the many factors that affect the performance increase attained by attaching a cache to a system, the most important are the characteristics of the actual application. Nevertheless, it's possible to perform a theoretical analysis of different caching techniques in a few simple steps.

First, look at the cache miss rate for various cache sizes and prefetched data-line lengths for a direct-mapped system. Note that the miss rate drops dramatically with an increase in line length. A line length that's wider than the processor bus will provide enhanced cache hit rates because of the sequential nature of most CPU activity. In fact, read hit rates approaching 95 percent can be

achieved through line lengths of eight times the CPU bus width.

Next, compare the cache miss rates of the various mapping methods, here expressed as a ratio of the direct-mapped method. To determine the actual miss rate of a nondirect-mapped system, find the miss rate (from first table) for a direct-mapped system and multiply it by the relevant cache-mapping-type ratio (from second table).

The resulting miss rate applies to read cycles only. If the cache uses a copyback

scheme or includes a write-cycle buffer, all write cycles may be regarded as cache hits. Assuming that 80 percent of memory cycles are read cycles, the overall miss rate may be reduced by 0.8. If the system is a writethrough cache, all write cycles are analogous to a cache miss in that the cache has to go to main memory, so 0.20 should be subtracted from the hit rate.

The miss rate of a particular cache implementation may be translated into a figure for total system improvement by determining the resultant hit rate, which equals 1 minus the miss rate, and considering the improvement in cycle time on a cache hit compared to a cache miss (see equation above). A cache hit will normally provide the minimum cycle period from the CPU. The cache miss cycle period depends on the main memory used.

A direct-mapped, writethrough caching system with 8-kbyte entries and a 4-byte line length removes three wait

$$\begin{aligned} \text{Total Hit Rate} &= 1 - (0.12 \times 1.00) - 0.20 \\ &= 0.68 \end{aligned}$$

$$\begin{aligned} \text{Performance Improvement} &= \frac{(6 \times 0.32) + (3 \times 0.68)}{6} \\ &= 1.52 \end{aligned}$$

states for a cache hit in a 68020-based system. (The 68020 has a minimum memory access cycle length of three clock periods. Any further clock periods required to meet the memory access time are referred to as wait states.) The system, therefore, provides a 52 percent increase in total performance.

$$\text{Performance Improvement} = \frac{\left(\frac{\text{Cache Miss Cycle Period}}{\text{Miss Rate}} \times \text{Miss Rate} \right) + \left(\frac{\text{Cache Hit Cycle Period}}{\text{Hit Rate}} \times \text{Hit Rate} \right)}{\text{Cache Miss Cycle Period}}$$

CACHE SIZE AND LINE LENGTH

Number of Entries	Miss Rate for Various Line Lengths			
	2 bytes	4 bytes	8 bytes	16 bytes
2k	0.57	0.23	0.10	0.04
4k	0.40	0.18	0.07	<0.04
8k	0.32	0.12	0.05	<0.04
16k	0.22	0.09	<0.04	<0.04

CACHE TYPE ADJUSTMENTS

Cache Types	Ratio of Miss Rate to Direct Mapping
direct-mapped	1.00
two-way set-associative	0.78
four-way set-associative	0.70
eight-way set-associative	0.67
fully associative	0.66

higher-order addresses, an asserted validation bit and the current data.

Direct mapping replaces cache entries on accesses to addresses that are multiples of the lower-order address range. This isn't quite as efficient as associative mapping, which replaces entries as on a least recently used basis. However, since most software operates serially, direct-mapped systems perform almost as well as associative systems. What's more, direct mapping has the considerable advantages of requiring just one com-

parator to check the retrieved cache-tag record and of using conventional SRAM. Direct-mapped caches of larger capacity thus may be constructed without extra cost or complexity.

■ A hybrid approach

Set-associative mapping is a hybrid of the direct-mapped and associative methods and is normally used as an efficient way of expanding a direct-mapped system. Set-associative systems contain multiple banks of direct-mapped caches that are dynam-

ically allocated on a least recently used basis, effectively providing a stack of direct-mapped caches.

A set-associative cache that has n banks of direct-mapped caches is referred to as n-way set-associative. Increasing the cache size by set-associative mapping gives greater hit rates than increasing the depth of a direct-mapped system. For this reason, many high-performance caching devices and systems adopt set-associative caching as a compromise between complexity and performance.

■ CACHING DESIGNS

All of these cache-tag methods need a mechanism for invalidating cache records either on power up or when it's clear that the cache entry is no longer a valid copy of the main memory. This mechanism is implemented as a validation bit attached to the cache-tag RAM and is included in the address comparison when determining whether a hit has occurred. Also, since many locations in a system address map may be uncacheable—including status latches, I/O devices and devices that require regular access—cache systems must provide mechanisms to exclude these locations from being entered in the cache.

■ Dealing with write cycles

In addition to the various mapping methods, cache systems may deal with write cycles by adopting one of two schemes: writethrough or copyback. Writethrough systems provide the simpler method in that write data is always passed straight through to the main memory, thus maintaining valid, up-to-date data in main memory. Writethrough caches don't affect the performance of write cycles, but since processors typically spend only 20 percent of their time performing write cycles, writethrough systems provide the best balance of performance and economy.

Copyback systems are the more complex of the two alternatives, providing a cache for write cycles as well as for read cycles. The copyback cache accumulates write cycles, transferring the data through to the main memory either when space is required in the cache for new entries, or to ensure that cache coherency is maintained when the cache has the only valid copy of data that another processor requires. Copyback systems will thus make the main memory appear to contain only valid data; the actual data in main memory will be incomplete until all the cache data has been copied back into it.

Copyback systems offer optimum performance, but they're highly complex. Copyback systems are most valuable when multiprocessors communicate via shared memory over a common bus. A copyback cache lets each processor maintain its own local copy of the global data, considerably reducing the traffic over the common bus. Protocols must be established for guaranteeing that data modified by any processor and retained within its cache is redistributed when other processors access the same location.

■ A bus solution

Futurebus, which was designed to let powerful cache systems be imple-

mented within a standard bus structure, provides protocols that guarantee the redistribution of this data. The only fully standardized system to offer these facilities, Futurebus lets simple writethrough systems coexist with full copyback systems.

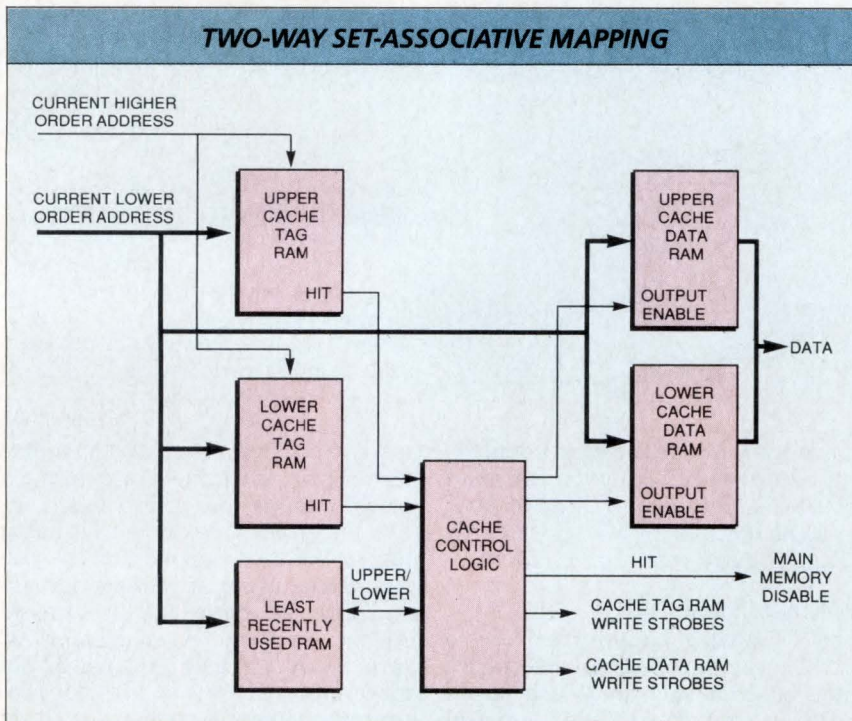
The Futurebus caching scheme adds a new dimension to multiprocessor cache systems. Multiple CPU cards, each with its own cache, may access shared global memory over Futurebus. Each cache may retain the only valid copy of pieces of data or one of multiple copies. Subsequent accesses to that data from any other processor will access the relevant cache and not necessarily the main memory. The global memory map thus becomes physically distributed among the separate cache systems, yet always appears as linear centralized global memory to all participating processors. Futurebus need only transfer data for write cycles and cache misses—a fraction of the data traffic otherwise required.

To allow full, coherent copyback operation, Futurebus defines states that are attached to every cache entry to indicate whether that entry is modified, owned, exclusive, shared or invalid. Futurebus further defines the rules that manipulate these states to maintain coherency. Once suitable VLSI devices become available, the Futurebus caching scheme will hold great promise for multiprocessor systems operating on a common data base.

■ Keeping the cache coherent

A cache system works by providing a local image of part of main memory. That image must be accurately maintained: It must be kept coherent. A caching system must operate within a set of rules that ensures that all entries are updated to reflect the true state of main memory. This procedure is straightforward when all accesses to the main memory share a common access port and, hence, share the cache facilities. This happens in single-processor designs in which only one device is using the memory. It is also true of multiprocessor systems in which the cache is positioned between the common global bus and the memory.

Cache coherency proves difficult when the main memory may be updated independently of the cache from a secondary port or independent bus. Although the main memory could be updated, the cache would



Using banks of direct-mapped caches that are dynamically allocated on a least recently used basis, two-way set-associative mapping produces greater hit rates than does increasing the depth of a direct-mapped system.



GE Plastics

There's
a New
Global Leader
in ABS
Resins...



It's Also the World's Leading Source

With the recent acquisition of Borg-Warner Chemicals, GE Plastics can now supply worldwide markets with the broadest line of ABS resins in the industry. Combined with our total resources in high-performance engineering polymers, this expansion forms a global product offering that is unmatched in its scope and versatility—a product range totally supported by the technologies which made these ABS resins and engineering polymers the world leaders in sales.

GE Plastics

Now designers and manufacturers all over the world have one source for a wider choice of products and properties to fit specific application needs—products that provide a new dimension of design possibilities and manufacturing efficiencies. LEXAN® resin, NORYL® resin, VALOX® resin, XENOY® thermoplastic alloys, CYCOLAC® ABS,

® LEXAN, NORYL, VALOX, XENOY, CYCOLAC, PREVEX, ULTEM and GELOY are registered trademarks of General Electric Company or affiliates.

™ SUPEC is a trademark of General Electric Company.



Source of Engineering Polymers.

PREVEX[®] polymer, ULTEM[®], SUPEC[™] and GELOY[®] resins, and many more.

With a network of technical, R&D and manufacturing facilities and sales offices spanning the globe, GE Plastics customers get fast response, dependable supply and delivery, and hands-on support from the industry's largest technical staff and market development team.

GE Plastics: creating more options, more opportunities—all over the world.

For information on LEXAN, NORYL, VALOX, ULTEM, SUPEC and GELOY resins and XENOY thermo-plastic alloys, call (800) 845-0600.

For information on CYCOLAC ABS and alloys and PREVEX polymer, call (800) 624-2611 (In Canada, call 416/372-6801).



GE Plastics

For information on LEXAN,
NORYL, VALOX, ULTEM, SUPEC and
GELOY resins and XENOY thermo-
plastic alloys, call (800) 845-0600.

For information on CYCOLAC ABS
and alloys and PREVEX polymer, call
(800) 624-2611 (In Canada, call
416/372-6801).



GE Plastics

■ CACHING DESIGNS

Micro Devices (Austin, TX) uses its cache to fill its instruction pipeline when a branch is made out of a sequential program flow.

Off-chip caches, on the other hand, allow even greater performance increases. With an off-chip cache, the cache system can be more precisely tailored to specific applications, but at the expense of extra chip count and complexity.

These external caches range enormously in their degree of integration. All contain a cache-tag RAM of varying mapping types, some contain the logic to control a separate off-chip data RAM, some provide an on-chip data RAM, and some include bus-snooping circuitry, parity protection or even memory-management units. Generally, the more highly integrated devices are targeted at specific processors and offer very high hit rates.

The current use of cache systems bridges the gap between high-performance processors and low-cost memory, allowing the transmutation of lumbering DRAM into nimble SRAM. With the present trend toward parallel processing, caching schemes relieve the shared memory access bottleneck and so let conventional processor elements operate efficiently in multiprocessor systems. □

ON-CHIP CACHING

Processor	Manufacturer	Cache Size (Bytes)	Mapping Type	Notes
68020	Motorola	256 program	direct-mapped	
68030	Motorola	256 program 256 data	direct-mapped	on-chip MMU
29000	Advanced Micro Devices	512 program	two-way set-associative	cache branches out of sequential program flow
32532	National Semiconductor	512 program 1,024 data	two-way set-associative	on-chip MMU
Clipper	Intergraph	4k program 4k data	two-way set-associative	chip set

Microprocessors that have their own on-chip caches improve system performance significantly. Some use pipelined architectures to overlap data fetches from internal cache with accesses to off-chip devices.

still contain the old, now invalid, data. This could be the case when each processor in a multiprocessor system has its own cache independent of the global bus where the shared memory resides, or when the main memory is actively dual-ported between two independent buses.

One solution to ensure cache coherency is to provide a mechanism to update or invalidate individual cache entries when the corresponding main memory locations are modified by a second processor or from another port. This is called bus watching, or snooping.

As an alternative, cache coherency through dual-ported memory may be maintained by suitable software handshaking. The processors sharing memory would arrange that no block of memory would be used while a device is actively modifying that block. When a processor needs to use a new memory block, it would clear all previous cache entries to guarantee that no stale data remains.

■ On-chip caches

Processors with on-chip caches create potential cache coherency problems if the main memory is dual-ported to other devices. When the on-chip cache is used solely for program data fetches, the dual-ported memory isn't usually a problem because program data isn't normally dynamically altered. It becomes a problem, however, when dynamically changing data is shared between two devices.

Multiple processors with on-chip caches will have difficulty communicating and coordinating actions when they don't recognize all of the changes in shared memory. Most processors with on-chip cache rely on the software handshaking solution to this problem, but some processors provide hardware hooks that let off-chip bus-watching hardware invalidate internal cache entries. Processors could conceivably also be designed with bus-watching hardware on-chip.

On-chip caches improve system performance significantly, but they're hungry for silicon real estate. These caches are, therefore, typically quite small: 256 bytes for the 68020/68030 and 512 bytes for the NS32532 from National Semiconductor (Santa Clara, CA), for example. Some high-performance processors use pipelined architectures that let a data fetch from an internal cache overlap accesses to off-chip devices. On-chip caching thus allows concurrency of data fetching, reducing the bottleneck of getting data on- and off-chip.

The NS32532, for example, provides hardware hooks to let an off-chip bus watcher invalidate on-chip cache. The 68030 allows burst filling of its cache, exploiting the relatively high access bandwidth of DRAM page and nibble modes, with which sequential data may be retrieved within a single, extended memory cycle. And the 29000 from Advanced

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Advanced Micro Devices (512) 462-5226	Circle 275
Motorola (602) 438-3715	Circle 276
National Semiconductor (408) 749-7431	Circle 277
Ovation Systems (44) 08446 638	Circle 278

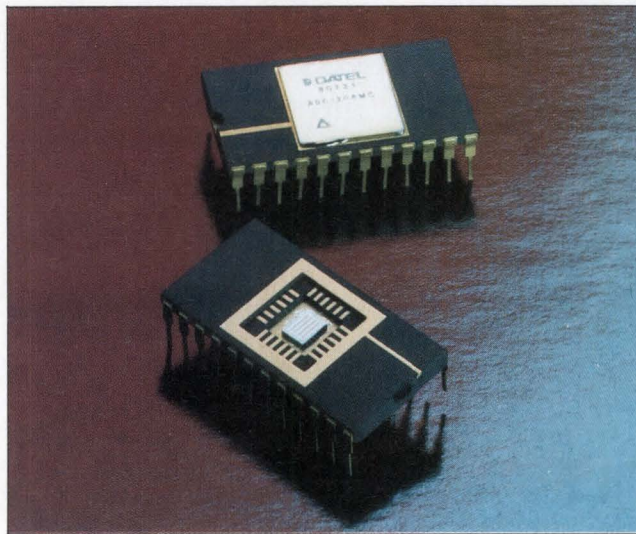
Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 506 Average 507 Low 508

INTEGRATED CIRCUITS

Higher speeds, CMOS designs drive flash A-D converter developments

John H. Mayer, Senior Associate Editor



CMOS flash analog-to-digital converters demonstrate increasing levels of performance. Designed in a 1.2-micron CMOS process, Datel's 8-bit, 20-MHz A-D converter-208 delivers $\pm 1/2$ least significant bit linearity over its full temperature range. An overflow pin lets designers achieve 9 bits of resolution by cascading two devices.

As digital signal processing systems move beyond strictly military applications and into the imaging and consumer markets, the demand is building for high-performance flash analog-to-digital converters capable of digitizing analog signals at increasingly faster rates. Vendors of high-performance DSPs are finding that the success of their processors is as dependent on the availability and cost of comparable high-performance front-ends as it is on processor performance.

"We're finally getting to the point where the whole DSP arena is getting out of the military domain," says John Hull, marketing manager for data-conversion products at Integrated Device Technology (Santa Clara, CA). "There's finally enough of a base of knowledge, the components are understood well enough, and the prices have come down to where it's really worthwhile to use these DSPs in consumer applications."

The market is responding with a growing array of monolithic and hybrid bipolar flash A-D converters capable of delivering sampling rates of up to 300 Msamples/s at 8 bits and 50 Msamples/s at 10 bits. In addition, vendors such as GE (Santa Clara, CA), IDT, Micro Power (Santa Clara, CA) and Datel (Mansfield, MA) are delivering CMOS parts boasting power consumption a fraction of their higher speed bipolar cousins. Continual improvements in CMOS processes are pushing these 8-bit devices

up to 30 MHz and higher. At the same time, data-converter designers are finding ways to add support functions ranging from references and drivers to clamping circuits and sampling amplifiers.

Business prospects for the flash A-D converter market look attractive enough to support a growing number of manufacturers. A few years ago, TRW (La Jolla, CA) led the industry as the sole major supplier. Its multi-sourced TDC1048 set the industry standard for 8-bit flash A-D converters. But with market analysts such as Venture Development (Natick, MA) projecting average annual growth rates in the 15 percent range over the next five years, the flash A-D converter market is becoming increasingly crowded. As the accompanying table demonstrates, about 20 vendors (some didn't respond to our survey) offer significant product lines ranging in resolution from 4 to 10 bits.

■ Ten-bit flash A-D converters

TRW still leads the industry in the race for the highest resolution flash A-D converter. The company's TDC-1020 is the only 10-bit monolithic flash design in volume production. Packed into a 64-pin dual in-line package, the TDC1020 offers a significantly more compact and less power-hungry solution than board-level alternatives. A commercial version of the TDC1020 is available, with a military model to be introduced later this year.

The other company to announce a 10-bit flash A-D converter is Honeywell (Colorado Springs, CO). The 50-MHz HADC77600 has already been designed into one military system, according to a spokesperson from the company's Signal Processing Technologies Group. Like many high-resolution flash A-D converters, the device adds a sparkel code detection circuit to prevent erroneous outputs.

Announced over a year ago and not yet available in production quantities, the HADC77600 has already gone through one redesign. The initial version of the part added a linear preamplifier with differential inputs and outputs placed between each pair of input-signal lines to the chip's comparators. Honeywell added the preamp because there weren't any buffer amplifiers capable of driving the converter's input, according to a company spokesperson. The revised, simplified design will eliminate the preamp in favor of an off-chip track-and-hold amp recently developed by Addacon (Greensboro, NC). Addacon offers the track-and-hold separately, but will eventually bundle the 30-MHz circuit in a module with the converter.

■ Video applications dominate

The product lines of most suppliers center around 8-bit parts targeted for TV video systems—by far the largest application for flash A-D converters. Determining the speed leader is a difficult, almost futile task. Specsman-

Device	Resolution (bits)	Sample Rate (Msamples/s)	Power Dissipation (mW)	Input Bandwidth (MHz)	Packaging	Price (100s)	Comments
Analog Devices PO Box 9106, Norwood, MA 02062 (617) 329-4700							Circle 100
AD9002	8	150	750	115	DIP, LCC	\$90	single supply, ECL output
AD9000	6	77	675	20	DIP, LCC	\$40	overflow bit, bipolar input
AD9011	8	100	1,500	80	metal DIP	\$180	built-in programmable gain
AD9012	8	100	955	180	DIP, LCC	\$70	TTL comp.
AD9688	4	200	700	100	DIP	\$20	bipolar input
AD770	8	200	2,000	250	DIP	\$175	wide bandwidth, bipolar input
Brooktree 9950 Barnes Canyon Rd, San Diego, CA 92121 (619) 452-7580							Circle 101
8-bit CMOS	8	20	500	6	DIP, PLCC	\$26	input clamping circuit, on-chip reference
Datel 11 Cabot Blvd, Mansfield, MA 02048 (508) 339-3000							Circle 102
ADC-207	7	35	250	10	DIP, LCC	\$30	CMOS, single 5-V supply, mid-point tap, 883 comp.
ADC-208	8	20	500	10	DIP, LCC	\$50	same as above
ADC-300	8	20	1,470	5.5	DIP	\$27	±1/2 LSB, -5-V supply, ECL comp.
ADC-301	8	30	420	15	DIP	\$65	±1/2 LSB linearity
ADC-302	8	50	550	25	DIP	\$125	±1/2 LSB linearity
ADC-303	8	100	1,200	40	DIP	\$286	±1/2 LSB linearity
ADC-304	8	20	360	8	DIP	\$28	±1/2 LSB linearity, TTL comp.
ADC-310	10	20	360	10	DIP	\$472	bipolar monolithic, ECL comp.
Fujitsu Microelectronics 3545 N First St, San Jose, CA 95134 (408) 922-9000							Circle 103
MB40547-7	8	20	900	—	24-pin DIP	\$64	±1 LSB accuracy, ECL output
MB40547-8	8	20	900	—	24-pin DIP	\$74	±1/2 LSB accuracy, ECL output
MB40576	6	20	270	—	16-pin DIP, SO	\$5.21	TTL output
MB40578	8	20	480	—	22-pin DIP	\$23.15	0.2% linearity, TTL output
GE Solid State/Intersil 2450 Walsh Ave, Santa Clara, CA 95051 (408) 996-5000							Circle 104
CA3304A	4	25	35	12.5	18-pin C, P DIP	\$5.94	CMOS/SOS
CA3306A	6	15	70	7.5	18-pin C, P DIP, 20-pin SO	\$15	CMOS/SOS
CA3318	8	15	150	5	24-pin C, P DIP	\$31	CMOS/SOS
Hitachi America 2210 O'Toole Ave, San Jose, CA 95131 (408) 435-8300							Circle 105
HD49303	8	20	200	5	DIP	\$16.15	CMOS, half flash
HA19217	8	40	600	7	SM (MSP)	—	bipolar, dual-input multiplexer, internal ref.
HA19216	6	30	250	5	DIP, SM (MSP)	\$5.90	bipolar, three-state output w/latch
HA19213	7	30	250	5	DIP, SM(MSP)	\$9.70	bipolar, TTL or CMOS comp.
Key: * single piece price; C= ceramic; comp.= compatible; DIP= dual in-line package; DNL= differential nonlinearity; EDC= error detection and correction; INL= integral nonlinearity; LSB= least significant bit; LCC=leadless chip carrier; MSP= mini square pack; P=plastic; PLCC=plastic leaded chip carrier; S/H= sample and hold; SM= surface mount; SO= small outline; SOS=sapphire-on-silicon; T & H=track and hold							

■ PRODUCT FOCUS/Flash A-D Converters

Device	Resolution (bits)	Sample Rate (Msamples/s)	Power Dissipation (mW)	Input Bandwidth (MHz)	Packaging	Price (100s)	Comments
Hitachi America 2210 O'Toole Ave, San Jose, CA 95131 (408) 435-8300							Circle 105
HA19211A	8	40	250	7	DIP, SM (MSP)	—	enhanced HA19211, wide bandwidth
HA19211	8	30	250	5	DIP, SM (MSP)	\$15	bipolar, HA19209 with added output latch
HA19209	8	30	250	5	P & C DIP, SM (MSP)	\$15	bipolar, TTL or CMOS comp.
HA19203	4	15	200	—	SM (MSP)	\$3.05	bipolar
HA19202	4	15	200	—	DIP	\$4.25	bipolar
Integrated Device Technology 3236 Scott Blvd, PO Box 58015, Santa Clara, CA 95052 (408) 727-6116							Circle 106
IDT75C48	8	30	500	15	28-pin CDIP, LCC, SO	\$21.50	CMOS, comp. w/TRW 1048, includes EDC
IDT75C58	8	30	500	15	28-pin C DIP, LCC, SO	\$21.50	CMOS, tristate output, overflow output
Maxim Integrated Products 120 San Gabriel Dr, Sunnyvale CA 94086 (408) 737-7600							Circle 107
ADC0820	8	—	25	12.7 kHz	DIP, SO, PLCC	\$8.95	CMOS, half-flash, w/ T & H, 1.4- μ s conversion
AD7820	8	—	25	12.7 kHz	DIP, SO, PLCC	\$9.95	same as above, 1.34- μ s conversion
AD7824	8	—	25	10 kHz	DIP, SO, PLCC	\$10.45	four-channel input, T & H, 1.6- μ s conversion
AD7828	8	—	25	10 kHz	DIP, SO, PLCC	\$10.95	eight-channel input, T & H, 1.6- μ s conversion
MAX150	8	—	25	12.7 kHz	DIP, SO, PLCC	\$9.95	+2.5-V _{ref} , T & H, 1.34- μ s conversion
MAX154	8	—	25	10 kHz	DIP, SO, PLCC	\$10.45	+2.5-V _{ref} , T & H, four input channels
MAX158	8	—	25	10 kHz	DIP, SO, PLCC	\$10.95	+2.5-V _{ref} , T & H, eight input channels
Micro Power Systems 3151 Jay St, Santa Clara, CA 95054 (408) 727-5350							Circle 108
MP7690	8	10	400	50	24-pin C DIP	\$95	no S/H, $\pm 1/2$ LSB
MP7783	8	2.5	100	—	P, C DIP, SO, LCC	\$8	same as above
MP7684	8	10	400	50	P, C DIP, SO, LCC	\$13.65	monolithic, no S/H, ± 2 LSB DNL
MP7685	11	1	100	—	P, C DIP	\$23.65	same as above
MP7682	6	15	120	50	DIP, LCC	\$5.85	monolithic, no S/H, $\pm 1/2$ LSB
MP7683	8	3	100	—	P, C DIP, SO, LCC	\$18.45	$\pm 1/2$ LSB DNL/INL
MP7686	6	35	200	—	SO, P, C DIP	\$8	monolithic, latch up free, no S/H, $\pm 1/4$ LSB DNL
MP7688	8	25	500	50	SO, P, C DIP	\$16.40	monolithic, latch up free, no S/H, $\pm 1/2$ LSB DNL/INL
Motorola Semiconductor Products 7402 S Price Rd, PR360, Tempe, AZ 85282 (602) 897-3872							Circle 109
MC10319	8	25	618	—	24-pin C DIP	—	monolithic, int. Grey code structure
MC10321	7	25	459	—	P DIP, SM	—	monolithic, int. Grey code structure
National Semiconductor 2900 Semiconductor Dr, PO Box 58090, Santa Clara, CA 95051 (408) 721-5000							Circle 110
ADC0820	8	0.5	75	7,000	20-pin DIP, 20-pin PLCC	\$8.95	half flash, built-in T & H

Device	Resolution (bits)	Sample Rate (Msamples/s)	Power Dissipation (mW)	Input Bandwidth (MHz)	Packaging	Price (100s)	Comments
NEC Electronics 401 Ellis St, Mountain View, CA 94039 (415) 960-6000							Circle 111
μ PP6950	8	15	400	—	DIP	—	CMOS, monolithic, for video applications
μ PD6951	6	20	125	—	DIP	—	same as above
Plessey Semiconductors 1500 Green Hills Rd, Scotts Valley, CA 95066 (408) 438-2900							Circle 112
SP97308E	8	30	450	—	18-pin C, P DIP	—	ECL output
SP97508	8	110	1,200	120	DIP	—	ECL output
SP9756	6	110	1,200	250	28-pin C DIP	—	ECL, $\pm 1/2$ or $\pm 1/8$ LSB
SP973T8	8	30	550	70	18-pin C, P DIP	—	latched TTL/CMOS output
SP97504	4	110	935	100	18-pin C DIP	—	ECL output, on-chip encoding
Samsung Semiconductor 3725 N First St, San Jose, CA 95134 (408) 434-5400							Circle 113
KSV3100AN-7/8	8	20	1,200	50	40-pin DIP	\$18.40/\$24	flash A-D & D-A, D-A 7 or 8 bits, on-chip V_{ref} gen., input preamp
KSV3110N-7	8	20	1,200	50	40-pin DIP	\$18.40	same as above
KSV3110AN-8/9/10	8	20	1,200	50	40-pin DIP	\$24/\$32/\$48	flash A-D & D-A; D-A 8, 9 or 10 bits, on-chip V_{ref} gen., input preamp, input clamping circuit
KSV3208AN	8	20	900	50	28-pin DIP	\$18.40	A-D only, on-chip V_{ref} gen., input preamp, input clamping circuit
Siemens Semiconductor Group, IC Div 2191 Laurelwood Rd, Santa Clara, CA 95054 (408) 980-4577							Circle 114
SDA8010	8	100	1,300	80	24-pin C DIP	\$100	complements SDA8020, SDA8800 data-acquisition components
SDA8200	6	300	1,500	250	40-pin C DIP	\$168	five effective bits at 150-MHz full-scale input, output demultiplexer
Signal Processing Technologies 1150 E Cheyenne Mtn Blvd, Colorado Spgs, CO 80906 (719) 540-3900							Circle 115
HADC77200	8	150	2,200	100	DIP	\$86	monolithic, preamp comparator design, quarter-point ref. ladder taps
HADC77600	10	50	4,700	70	PGA	\$795*	monolithic, preamp, eighth-point ref. ladder taps
Signetics 811 E Arques Ave, Sunnyvale, CA 94088 (408) 991-2000							Circle 116
TDA8703	8	40	300	19.5	24-pin DIP	\$15	low power, input buffer amp, +5V only
Sipex, Hybrid Systems Div 22 Linnell Cir, Billerica, MA 01821 (508) 667-8700							Circle 117
HS1068	8	20	1,750	13	24-pin metal DIP	\$295	hybrid, includes input buffer amp, V_{ref} , output register
SP1070	8	25	965	6	28-pin metal DIP	\$260	hybrid, includes dc stabilized input buffer amp, V_{ref} .
SP1072	8	25	1,400	7	hermetic 42-pin pkg	—	dual-channel hybrid; two 8-bit A-Ds, two buffer amps/channel, V_{ref} .

■ PRODUCT FOCUS/Flash A-D Converters

Device	Resolution (bits)	Sample Rate (Msamples/s)	Power Dissipation (mW)	Input Bandwidth (MHz)	Packaging	Price (100s)	Comments
Sony 10833 Valley View St, Cypress, CA 90630 (714) 229-4197							Circle 118
CXD1172P/M	6	20	70	40	DIP, SM	\$8.90/\$9.50	—
CXD1175P/M	8	20	90	40	DIP, SM	\$19/\$21	—
CXA1096P/M	8	20	350	8	DIP, SM	\$17.20/\$19	—
CXA1016P	8	30	420	15	DIP	\$39	—
CXA1056P	8	50	550	25	DIP	\$75.60	—
CX20116	8	110	1,200	90	DIP	\$89	—
CXA1076K	8	200	720	180	LCC	\$270	wide input bandwidth, low power
CXA1176K	8	300	1,300	200	LCC	\$175	same as above
Tektronix PO Box 500, Beaverton, OR 97077 (800) 835-9433							Circle 119
TKAD20C	8	250	5,000	125	84-pin ceramic	\$850	on-board T & H, selectable demultiplexed output
TRW LSI Products PO Box 2472, La Jolla, CA 92038 (619) 457-1000							Circle 120
TDC1044	4	25	350	12.5	16-pin C, P DIP	\$9	monolithic, comm. or 883 comp., TTL output
TDC1046	6	25	625	12.5	18-pin C DIP	\$13	monolithic, low-power, comm., hi-rel. or 883 comp., TTL output
TDC1047	7	20	1,000	7	24-pin C DIP	\$20	monolithic, comm., hi-rel. or 883, TTL output
TDC1048	8	20	1,600	7	28-pin DIP, LCC, PLCC	\$23	monolithic, comm., hi-rel. or 883, TTL output
TDC1038	8	20	500	10	28-pin DIP, LCC, PLCC	\$20	monolithic, low-power upgrade for TDC1048 & CXA1096
TDC1058	8	20	500	10	28-pin DIP, LCC, PLCC	\$20	monolithic, +5-V supply, upgrade for CXA1096
TDC1049	9	30	3,000	15	64-pin DIP, 68-lead LCC	\$202	monolithic, comm., 883 or std mil drawing testing, ECL output
TDC1020	10	20	3,500	5	64-pin C DIP	\$395	monolithic, comm. or 883 test, TTL output
THC1068	8	20	1,600	10	24-pin metal DIP	\$73	hybrid, complete flash A-D system, TTL output
THC1069	9	30	3,500	15	32-pin metal DIP	\$279	same as above with ECL output
THC1070	10	20	4,000	10	32-pin metal DIP	\$540	hybrid, complete flash A-D system, TTL output
TDC1029	6	100	2,400	50	24-pin C DIP	\$78	monolithic, comm. test, ECL output
THC1200	12	10	8,500	5	46-pin metal DIP	\$1,390	hybrid, half flash, complete A-D system, TTL output
THC1201	12	10	5,500	5	46-pin metal DIP	\$1,300	same as above
TDC1025	8	50	2,900	12.5	68-contact CC	\$290	monolithic, comm. or hi-rel. test, ECL output

ship, as always, is a problem. Also, newer, faster parts emerge every few months. But if one had to select the speed leaders among 8-bit flash A-D converters, they would no doubt include the AD770 from Analog Devices (Norwood, MA), the TKAD20C from Tektronix (Portland, OR), the

SDA8200 from Siemens (Santa Clara, CA), and the CXA1076 and CXA1176 from Sony (Cypress, CA).

For pure 8-bit accuracy, the TKAD20C from Tektronix offers the best, albeit one of the most expensive, solutions. At high speeds, A-D converters are typically limited by their

ability to track and capture the incoming signal. Many designers handle this problem by placing a separate track-and-hold amplifier in front of the device. The TKAD20C, however, was the first commercial A-D converter to include an on-board track-and-hold circuit.

INTEGRATED CIRCUITS

Unlike many competitors, the TK-AD20C was designed from the ground up as a two-chip device. The resulting tight interface between the A-D converter and the track-and-hold amplifier helps the part achieve a 250-M-sample/s conversion rate and an impressive accuracy of 7 effective bits at 125 MHz. Selectable demultiplexed outputs let designers easily conform the part to a variety of applications.

Though the AD770 from Analog Devices can't quite match the performance of the Tektronix part, it delivers an 8-bit output at 200 Msamples/s with a 250-MHz full-power bandwidth. The converter also sells at roughly one-quarter the price of the Tektronix part. For radio frequency applications, the analog input range can be unipolar or bipolar and can be set any to any span within ± 2 V.

An interesting price/performance trade-off is offered by the Siemens SDA8200. The 6-bit, 300-MHz A-D converter is the first monolithic flash signal converter to digitize a 150-MHz input signal with an effective resolution of 5 bits. In addition, the 6-bit part only requires 63 comparators to reach its performance level, in contrast to the 255 comparators required for an 8-bit part. Chip size is small, and power dissipation is a scant 1,800 mW. Like its competitors, the SDA8200 adds overflow outputs so designers can cascade two or more parts to achieve 7-bit resolution. A user-selectable demultiplexer splits the output signal through two parallel output streams at half the sampling rate.

■ CMOS speeds accelerate

Although bipolar flash A-D converters still provide the highest performing solutions, CMOS devices continue to edge closer to their bipolar competitors. If a designer doesn't require flash A-D converters at top speeds, CMOS parts offer compact, precise solutions at significant power savings. "For the 20-MHz and under region, there's very little argument in favor of bipolar, and most of it in favor of CMOS," says Walter Borlase, Micro Power Systems' director of standard products.

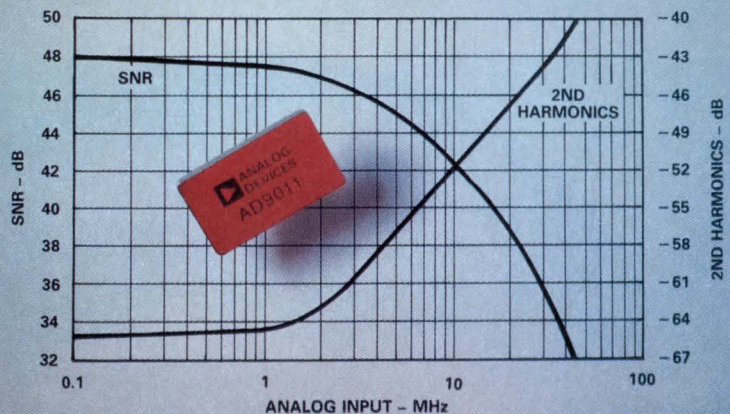
Micro Power Systems offers monolithic CMOS A-D converters up to 20 MHz with full-power bandwidths in excess of 50 MHz. The Micro Power parts operate from a single supply

and provide a reference voltage of 0 to 2 V_{dd} . "Most of the devices on the market right now are built almost strictly for television, so you get a 2- V_{pp} ," says Borlase. "We'll actually give you 0 to 5 V."

Other vendors are pushing CMOS parts beyond 20 MHz. This summer, IDT unveiled its IDT75C58, a 30-MHz 8-bit CMOS chip. The device features a unique on-chip error detection and correction (EDC) circuit that guarantees no missing codes over all temperature and voltage extremes. "A lot of our competitors' converters

will get so hot you might not be able to put it into a normal package," he says. "It would be well-nigh-impossible to put the amount of added circuitry that we included on this EDC on a bipolar flash A-to-D."

Despite these apparent advantages, most vendors agree that as CMOS parts move to bipolar speeds, the dividends CMOS offers evaporate. Bipolar converters dissipate the same power whether running at 1 or 20 MHz, while CMOS power usage increases with speed. "It's a myth that CMOS parts are low-power,"



Complete analog-to-digital systems such as Analog Devices' AD9011 save board space by combining a monolithic flash converter with a wideband op amp and voltage reference in a single, 24-pin metal dual in-line package. The 8-bit, 100-Msample/s part is targeted for applications in radar, digital radio, ATE systems and digital oscilloscopes.

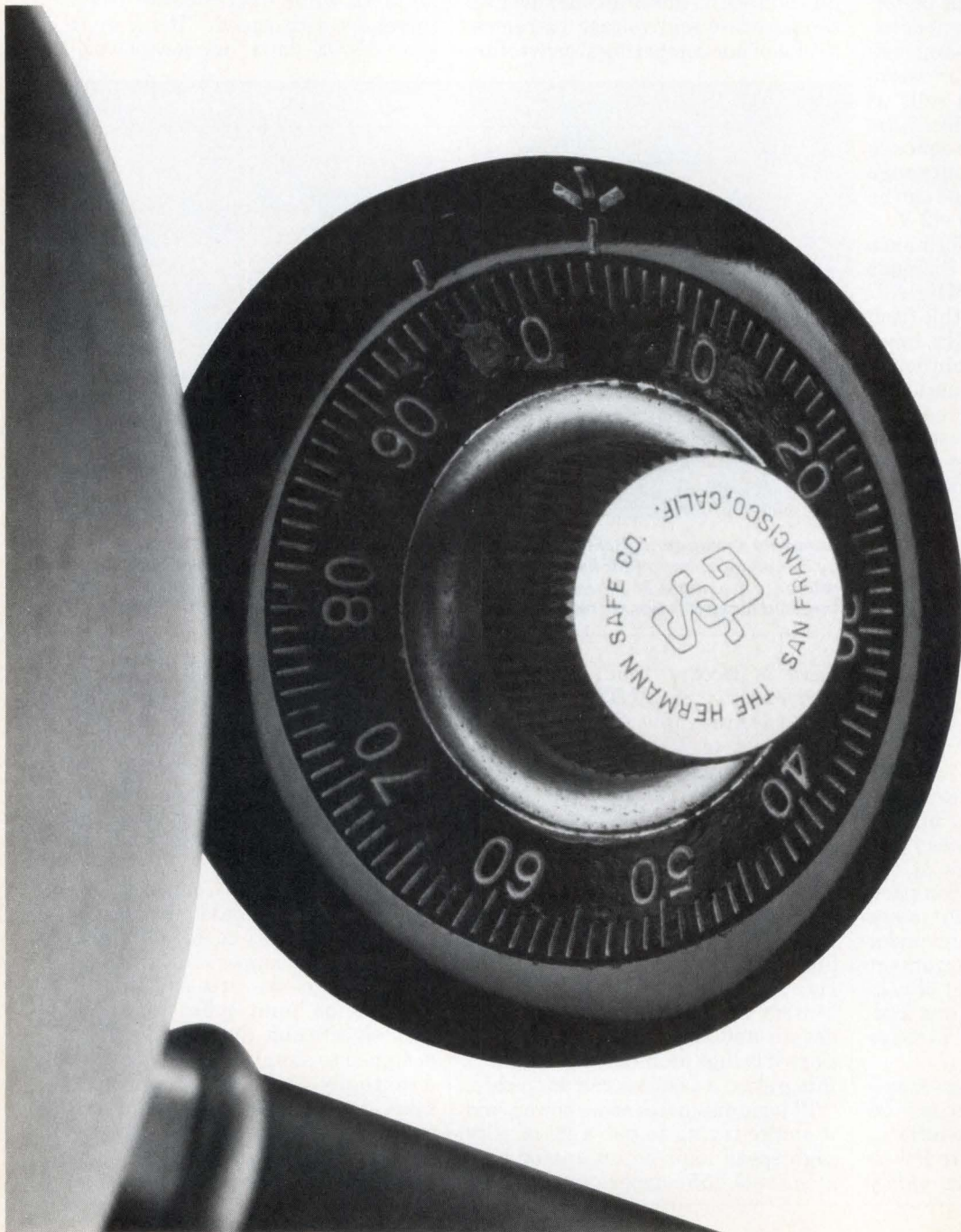
have a decoder that's similar to either a two-input AND gate or sometimes a three-input AND gate to detect the 1 to 0 second transition," explains Jim Brubaker, senior staff design engineer at IDT. "We've gone beyond that by detecting an illegal state and suppressing the false binary code that you get out."

The ability to add support functions such as EDC to a chip reflects a major advantage of CMOS over bipolar designs, according to IDT's Hull. He claims that the power-hungry characteristics of a bipolar design and the thermal considerations it brings prohibit the amount of integration a designer can do on-chip. "All logic dissipates some power, and if you're trying to put a lot of very high speed logic on an analog chip along with 255 comparators, the chip

says Karlak. "The reality is that at higher speeds, they're going to approach bipolar power." Micro Power's Borlase agrees. "If you take a CMOS machine and start to run it at very high clock rates, you suddenly find that the power consumption goes up as well because you have all the capacitance to charge."

Still, CMOS designs, or perhaps Bi-CMOS designs, should offer designers an opportunity to add a number of interesting support functions on-chip. Some of the first add-ons will probably be input buffer amplifiers and significant digital interfaces designed to simplify use of the part. Eventually, the flash A-D converter market will most likely see increasingly application-specific products with inputs and outputs designed to meet specific application needs. □

E²/DIGITAL/ANALOG. COMBINATION Y



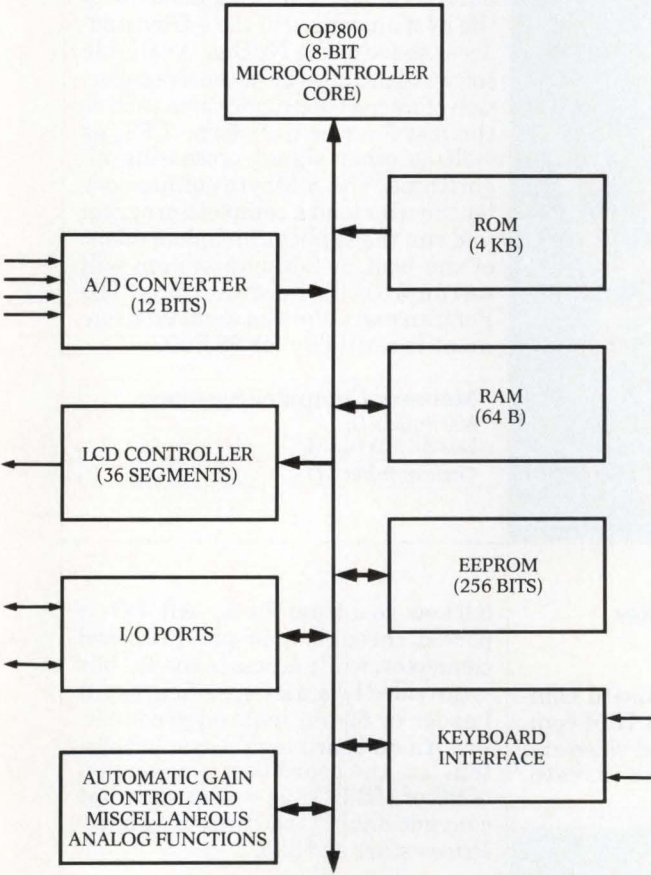
THE TECHNOLOGY YOU CAN BANK ON.

To be perfectly honest, we didn't invent the concept that says high integration equals high profit. But as you can see from the application diagram on this page, we definitely perfected it. With our Triple Technology,[™] a process that allows you to combine E², digital, and analog functions on the same chip. And, create higher levels of integration than ever before.

In this case, our customer's last product was a medical instrument the size of a paperback, with 70 different components. By combining a sophisticated 8-bit controller, RAM, ROM, A/D converter, and 256 bytes of EEPROM on the same chip, we helped them shrink the same instrument to the size of a matchbox. And cut the costs just as dramatically.

As a result, they have a product that sets new standards for the industry. And for their shareholders. And by working closely with their designers, we were able to create this one-chip solution with standard cells from our library. In fact, our customer only had to design about 200 gates of logic using our standard digital cells.

Turnaround time from code to first silicon was only 18 weeks. And because of our development tools and mixed-mode simulation (MIXsim[™]), the first prototypes worked.



Single chip measurement and control system, integrating several EEPROM, analog, and digital functions.

Of course, this is only one example. With 250 digital, 50 analog, and over 20 EEPROM cells in our library, we can create literally thousands of combinations. Including Analog/E², E²/Digital, Analog/Digital, and E²/Analog/Digital. For every application you can imagine. And we can execute them all in high performance CMOS.

So, no matter what you're designing, call or write for our complete library card. And we'll show you a combination you can always bank on. Your ideas and our technology.



Sierra Semiconductor
Triple Technology.[™] In CMOS.

2075 North Capitol Avenue, San Jose, California 95132. Telephone (408) 263-9300

CIRCLE NO. 20

COMPUTERS AND SUBSYSTEMS

Macintosh II floating-point coprocessor performs 20 MFlops

The MC3200NU single-slot processor card for the Macintosh II is aimed at 32-bit floating-point-intensive applications. The board, which can be

master or slave in the system, is a 20-MFlops, 10-Mips coprocessor that executes computation-intensive vector and scalar operations for applications such as simulation, modeling, signal processing, image processing and postscript. Programmable in C, Fortran, assembler and microcode,

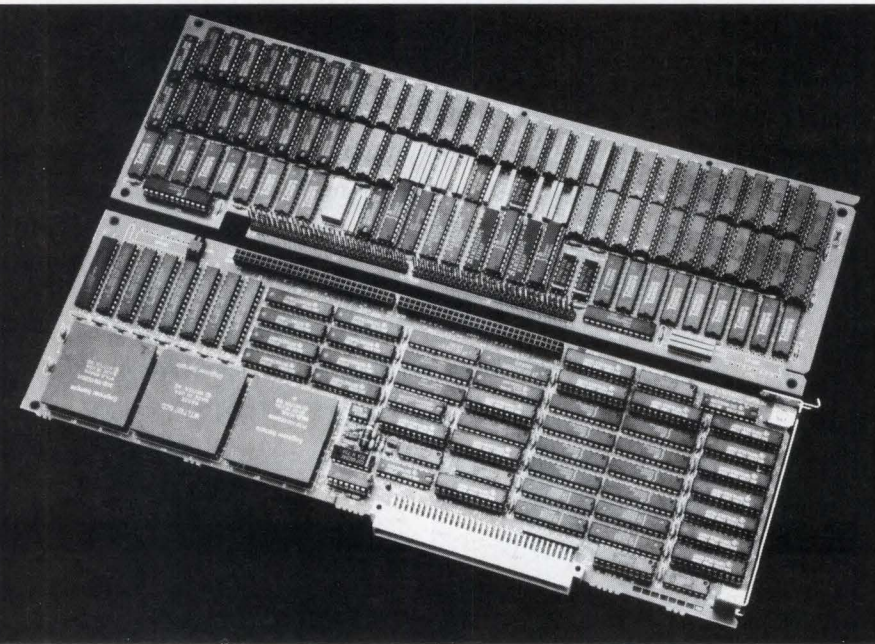
the coprocessor is supported by the Macintosh Programmer's Workshop, which provides the development environment.

The board is based on Weitek's XL-8032 reduced-instruction-set processor chip set, which includes the WTL-3132 32-bit floating-point unit. The three-chip set is supported by up to 8 Mbytes of two-way interleaved memory on a 40-Mbyte/s internal bus. Mastership capability lets the board transfer data independent of the host anywhere in the 4-Gbyte address space of the NuBus. Available software includes an extensive collection of microcoded algorithms such as the fast Fourier transform (FFT) as well as other signal processing algorithms. The 8 Mbytes of memory let the user load a complete program and run the application independent of the host. A 2-Mbyte system will sell for \$10,000, hardware only. The Fortran and C development environment is available for \$8,500.

Mercury Computer Systems

600 Suffolk St
Lowell, MA 01854

Circle number 121

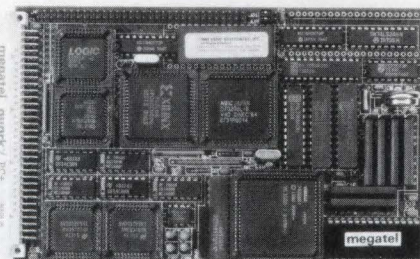


Z280 STD Bus board expands to 128 kbytes

Featuring the speed and architectural improvements of the Zilog Z280, the H280STD is a single-board computer for the STD Bus. It will run all current Z80 applications, including CP/M. On-board cache is incorporated by the microprocessor, as well as 24-bit address space, memory management and protection, and hardware multiply/divide. Up to 128 kbytes of ROM or battery-backed RAM can be included in any mix on the board, which comes with 20 bits of parallel I/O standard and three RS-232 ports. A total of eight counter/timers are included for real-time, multitasking process control applications. Price for the single-board computer is \$395.

Single-board computer consumes 3 W

The Quark/PC+ single-board computer boasts a complete IBM-compatible CPU with on-board video and disk controllers on a 4-x6-in. card,



and consumes 3 W. Up to 768 kbytes of dynamic RAM is available on the board, as well as a small computer system interface host adapter, a floppy disk controller, a video/LCD controller, three serial ports, a parallel port, a reset switch and a battery-

backed real-time clock. All I/O is ported through a 96-pin Eurocard connector, while access to the PC bus is provided by a user-specified 64-pin header or 62-pin male edge connector. An on-board legal basic I/O system lets the board boot any version of PC or MS-DOS as well as run most conventional PC software packages. Prices start at \$325.

Megatek Computer

174 Turbine Dr
Weston, ON M9L 2S2, Canada

Circle number 123

Controller functions reside on AT-class mother board

A small-footprint, IBM PC AT-compatible computer, the ARC Turbo uses VLSI chips for I/O, video and disk controller functions. The system runs under either the MS-DOS or OS/2 operating system, with keyboard- or software-selectable

Computer Design Solutions

PO Box 127
Statesville, NC 28677

Circle number 122

COMPUTERS AND SUBSYSTEMS

clock speeds of 8 or 12 MHz. Basic configuration includes 1 Mbyte of RAM expandable to 16 Mbytes, a 1.2-Mbyte 5¼-in. floppy disk drive, a keyboard and a 150-W power supply. System expansion is provided through five full-sized expansion slots, four of them 16 bits and one 8 bits. An 80287 numeric coprocessor is optional. The basic system is priced at \$1,995.

American Research
1101 Monterey Pass Rd
Monterey Park, CA 91754

Circle number 124

68020 VMEbus SBCs use mezzanines for expansion

A pair of VMEbus controller/single-board computer products are specifically designed to allow user expansions via plug-in mezzanine modules. The 68020-based boards are identical except in the area of on-board memory. The PT-VME118 provides 1 Mbyte of dual-ported RAM, expandable to 2 Mbytes, without parity. The PT-VME120 offers a fixed 1 Mbyte of dual-ported dynamic RAM with parity protection. Both models' memory runs at 16-MHz zero-wait-state clock speeds. Other features include a seven-level VMEbus interrupt handler, two 32 JEDEC sockets for local RAM/ROM and an optimized VME interface. Most options on the modules are configured via a software menu through an RS-232C terminal with all software-defined user information stored in a dedicated 1-kbit EEPROM. The PT-VME118 is priced at \$1,600, while the PT-VME120 costs \$1,840.

Performance Technologies
435 W Commercial St
Rochester, NY 14445

Circle number 125

80386 mother board doubles AT's speed

Based on the Intel 80386 microprocessor, the 386 Motherboard/AT improves the performance of an IBM PC AT by 2½ times by upgrading a 6- or 8-MHz AT to 16-MHz 386 speed. The board, which will also work with AT compatibles, uses the Award 386

basic I/O system, comes with four 16-bit and four 8-bit I/O slots, has a 32-bit RAM extension connector, and can be expanded with up to 12 Mbytes of RAM. A 16-MHz 387 math coprocessor is available for math-intensive applications. With 1 Mbyte

of memory, the board is priced at \$1,595.

Hauppauge Computer Works
175 Commerce Dr
Hauppauge, NY 11788
Circle number 126



2.5 Gigabytes Unattended Backup

Digi-Data's GIGASTORE™ provides 2.5 Gigabytes of data storage on a single T-120 VHS video cartridge. That permits backup of your largest disk drive on off-hours without an operator.

Utilizing true read-after-write coupled with very powerful error correction, GIGASTORE gives you an unsurpassed error rate of 1 in 10²³ bits. In addition, you get a high speed search capability not available in most 9-track drives.

GIGASTORE can be provided with an interface for DEC computers, such as VAX and Micro Vax, for operation under VMS. It is also available with an IBM PC interface, operating under MS/DOS.

Call Digi-Data, an organization with a 25 year history of manufacturing quality tape drives, at (301) 498-0200.

™GIGASTORE is a trademark of Digi-Data Corporation.



DIGI-DATA CORPORATION
8580 Dorsey Run Road
Jessup, MD 20794-9990
(301) 498-0200
Telex 87-580

... First In Value

In Europe contact: Digi-Data Ltd. • Unit 4 • Kings Grove • Maidenhead, Berkshire
England SL6 4DP • Telephone No. 0628 29555/6 • Telex 847720

**DEALER
INQUIRIES
INVITED**

CIRCLE NO. 22

COMPUTER DESIGN OCTOBER 15, 1988 83

DATA ACQUISITION AND CONTROL

Analog-to-digital I/O board speeds to 1 Msample/s

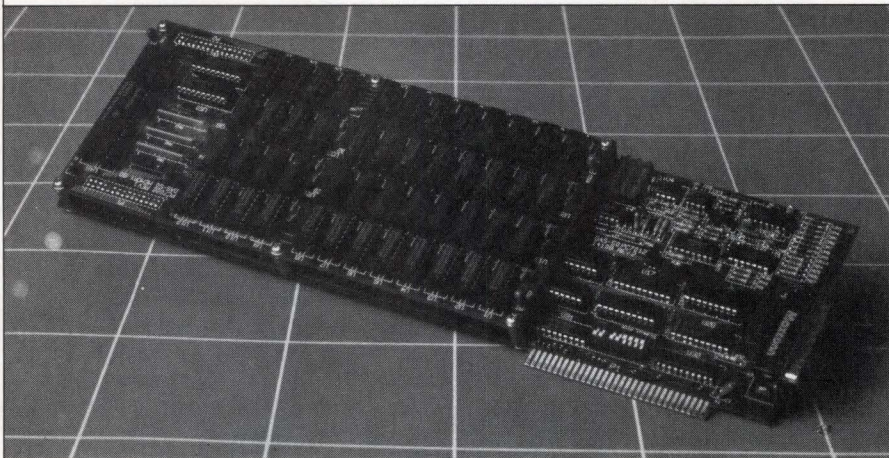
Featuring an on-board 12-bit analog-to-digital converter with a maximum sampling rate of 1 Msample/s, the DAS-50 is a four-channel I/O board for IBM PCs, PC XTs, PC ATs and

compatibles. A series of samples (or Trace) may be triggered via software commands, an external trigger or a voltage-level input.

Since direct memory access isn't possible at 1 million conversions/s, local on-board data storage is provided. Up to 1 Mword of memory may be configured by using up to four banks

of 256k x 1-bit dynamic RAMs. By using 16 consecutive locations in I/O address space that can be set to start at any base I/O address, the board takes up no memory address space, requires no on-board initializing basic I/O system and can be installed regardless of the I/O address usage of other peripherals.

Five software programmable, unipolar or bipolar input ranges are available, and maximum linearity error is only 1 least-significant bit guaranteed over the full input range. The selection and control of all features are accomplished through the computer keyboard or a mouse, with utility software provided as a device driver, letting programs be written in any upper-level language. Prices start at \$1,999.



Metabyte

440 Myles Standish Blvd
Taunton, MA 02780

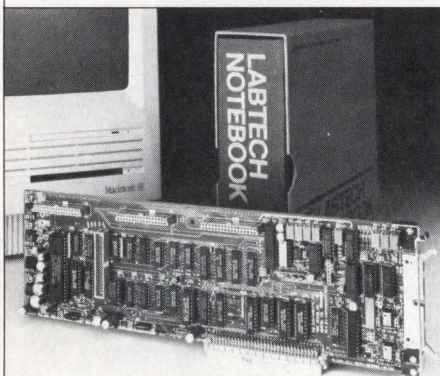
Circle number 127

Data-acquisition products target Macintosh II and SE

The MacAdios II Data Acquisition System consists of a multifunction analog and digital I/O board set that plugs into one of the Macintosh II or

functions; and data replay. The software transfers acquired and reduced data to spreadsheets, scientific graphics worksheets and other Macintosh programs for further data analysis and display.

tional set-up commands include data logging, real-time operator interfaces and on-line analysis. The package is priced at \$2,995.



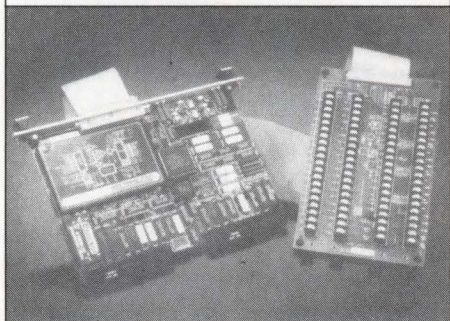
GW Instruments

35 Medford St
Somerville, MA 02143

Circle number 128

Industrial process control software runs on PCs

A factory automation software package for industrial process control, the L/T Control System is designed for use on IBM PCs or compatibles equipped with the manufacturer's data acquisition and control hardware. The boards plug into PC expansion slots; have software-selectable ranges or autorange; are self-calibrating with diagnostics available on command; and feature a low-noise integrating converter that can take up to 10,000 samples/s. Graphical real-time animated data displays are offered, as well as high-resolution plots, on/off control, and alarm loops. Addi-



Strawberry Tree Computers

160 S Wolfe Rd
Sunnyvale, CA 94086

Circle number 129

Controller allows data acquisition on Bitbus

The RTP7411/70 serial controller provides an interface between Bitbus and the manufacturer's RTP family of analog, digital and special-function I/O data-acquisition hardware and software products. The board

SE expansion slots, a variety of signal-conditioning daughter boards, and software for data acquisition and control. Optional Labtech Notebook software provides user-definable control and display setups and parameters; real-time mathematical, statistical and signal-processing calculations; triggering; monitoring; control

DATA ACQUISITION AND CONTROL

consists of a standard Bitbus core, a hardware interface to the RTP bus, an RS-232 serial channel and a firmware package that converts Bitbus to RTP signals. All programs and data are stored in a 32-kbyte, battery-backed CMOS RAM. Rates of up to 375 kbits/s are supported.

Computer Products

2900 Gateway Dr
Pompano Beach, FL 33069

Circle number 130

VMEbus boards feature 16-bit A-D resolution

The DT1492 series of analog and digital I/O boards features single-board operation with up to 16 bits of analog-to-digital resolution and 16 lines of digital I/O. High-speed simultaneous analog input and output operations are supported via 512 kbytes of memory, allowing A-D throughput speeds of up to 750 kHz. Gap-free continuous performance operation assures data

integrity, while automatic sampling of any input or output sequence is possible at any gain. Optional simultaneous sample-and-hold A-D can acquire up to four channels within 10 ns. The series consists of nine models with a variety of options. Prices start at \$2,195.

Data Translation

100 Locke Dr
Marlboro, MA 01752

Circle number 131

DESIGN AND DEVELOPMENT TOOLS

Emulator boasts zero wait states at 16 MHz

An in-circuit emulator for Intel's 80C186/80C188, the ES 1800 runs with zero wait states at 16 MHz. An I/O overlay capability is featured that lets the emulator exercise I/O service routines without target hardware. The device also lets the user see the entire peripheral control block on one screen and make register changes without the large number of register dumps and writes normally required.

Complementing the emulator is the Validate/Soft-Scope source-level debugger. It features a powerful command set, real-time trace displayed in source-level statements, machine

instructions and bus cycles with easy access to high-level language data structures and arrays. The Event Monitor System is included, providing state-machine capabilities for triggering, breakpoint and emulation control. The system lets an engineer control emulation by breaking on any combination of address, data status, pass counter and logic state fields. An event or combination of events, defined by logic statements, can be used to break emulation, trace software sequences and count or trigger outputs. Prices start at \$11,000.

Applied Microsystems

5020 148th Ave, NE
Redmond, WA 98073

Circle number 132

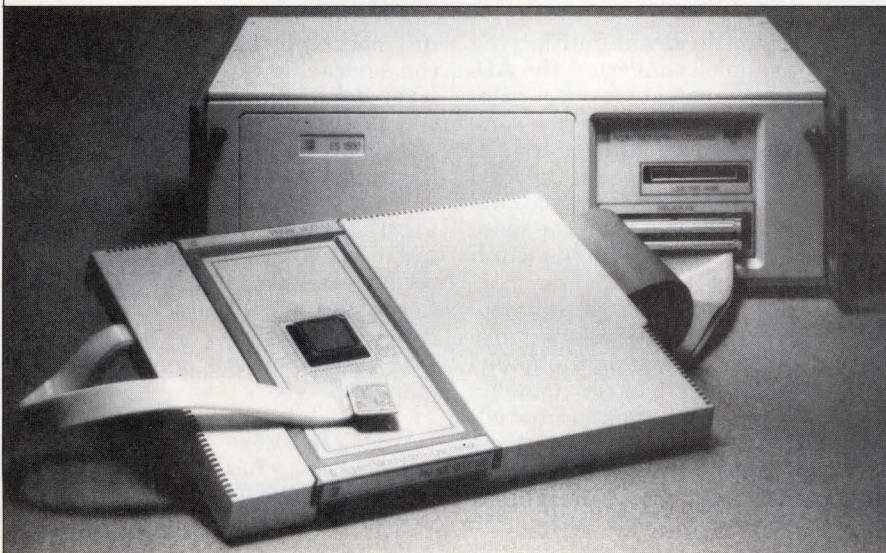
X Window System coupled to DOS, Unix workstations

The X Window System Version 11 (X11) lets Hewlett-Packard's MS-DOS and Unix workstations access X-based applications in a multivendor, networked environment. Based on a client/server architecture, the system lets clients, or X-based applications, make requests for resources (display, keyboard, mouse or other input devices) from the server. Software developers have the choice of building a user interface for their applications based on HP's X Widgets, designing their own widgets, or using a combination of the two. With these tools, developers can use pop-up menus, panels, scroll bars and a variety of other widgets to construct the desired user interface. Prices range from \$495 to \$4,500 depending on the host system.

Hewlett-Packard

19310 Pruneridge Ave
Cupertino, CA 95014

Circle number 133



FULLY APPROVED UNIVERSITY DEGREES Economical home study for Bachelor's, Master's, Ph.D., fully approved by California State Department of Education, not accredited. Prestigious faculty counsels for independent study and life experience credits (5000 enrolled students, 400 faculty). Free information—Richard Crews, M.D. (Harvard), President, Columbia Pacific University, Department 3E50, 1415 Third Street, San Rafael, CA 94901. Toll free: (800) 227-0119; California: (800) 552-5522; or (415) 459-1650.

DESIGN AND DEVELOPMENT TOOLS

Logic analyzer increases debugging performance

A logic analyzer that can rapidly identify problem areas in microprocessor and logic designs, the K115 offers the power of two independent analyzers in one package. The general-purpose state/timing section provides 64 input channels and eight levels of trace control triggering at resolutions of 50 ns. The high-resolution section provides eight additional channels with resolution to 10 ns, with four channels user configurable to 5 ns. Other features include noise margin analysis to identify signals not making full logic-level swings, histogram analysis for program execution overviews, disassembly for detailed program tracking and mixed radix display formats.

Gould
3631 Perkins Ave
Cleveland, OH 44114
Circle number 134

Floppy disk controllers support XTs, ATs and PS/2s

The ACC 3200 series of single-chip floppy disk controllers for IBM PC XT, PC AT and Personal System/2 Models 30, 50, 60, 80 and compatible systems directly controls up to four diskette drives. Each VLSI device is manufactured with 1.5-micron CMOS technology and incorporates all functions of a floppy disk controller in one 68-pin plastic leaded chip carrier to save space in system designs. Prices are from \$10 to \$20.

ACC Microelectronics
3333 Bowers Ave
Santa Clara, CA 95054
Circle number 135

Routing program designs surface-mount devices

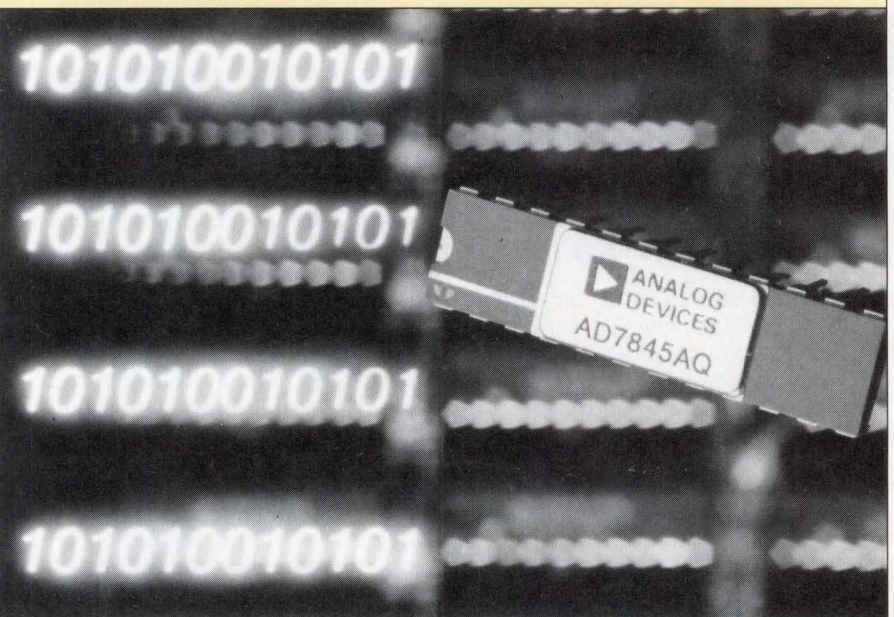
A gridless software program for automatically routing ultra-high-density circuits, the Flex Router is based on algorithms designed for surface-mount technology. The software runs on the manufacturer's CR 3000 electrical CAE/CAD/CAM system and al-

lows exact routing from the center of the surface-mount device pad or off-grid routing between pads. Capabilities for bus routing, general signal routing and ground routing are also provided. The design tool allows special routing of connectors, including autorouting of edge connectors, and

features user-selectable routing angles as well as rip-up and reroute capabilities.

Zuken
24 New England Executive Park
Burlington, MA 01803
Circle number 136

INTEGRATED CIRCUITS



Twelve-bit multiplying D-A converter hosts on-chip amplifier

A 12-bit, four-quadrant multiplying digital-to-analog converter, the AD-7845 includes an on-chip output amplifier. The monolithic device combines high-speed digital logic and linear circuitry in a 0.3-in. Skinny dual in-line package (DIP) to reduce chip count while displacing half the space of traditional 24-pin double-width DIP devices.

External connections permit configuration for either unipolar or bipolar operation, as a programmable-gain amplifier or a programmable current source. Gain ranging and offsetting are provided via three matched internal application resistors, while TTL- or CMOS-compatible inputs drive the 12-bit latch, con-

trolled by standard signals, allowing connection to the 16-bit bus interface through direct unbuffered operation.

Guaranteed monotonic over the full operating temperature range, the device allows a maximum of ± 1 least-significant bit (LSB) differential nonlinearity and ± 2 -mV zero-code offset error. The on-chip amplifier and feedback resistor perform current-to-voltage conversion with accuracy within ± 1 LSB. Delivering a ± 10 -V swing into a $2\text{-}\Omega$ load, the internally compensated output amplifier settles to 0.01 percent full-scale range in under $5\ \mu\text{s}$. In quantities of 100, prices for the D-A converter start at \$7.40.

Analog Devices
One Technology Way
Norwood, MA 02062
Circle number 137

INTEGRATED CIRCUITS

EDC circuit detects memory errors in 16 ns

The Am29C660 error detection and correction (EDC) circuit, a high-speed CMOS device, detects all single-, double- and some triple-bit errors in each single memory word. The 32-bit circuit corrects all single-bit errors, including hard errors caused by permanent physical device failure as well as soft transient errors by using a modified Hamming Code algorithm and generated check bits. The highest performance version has a 16-ns maximum delay for error detection and a 24-ns maximum delay for error correction. In 5,000-piece quantities, the chip is available in a 68-pin plastic leaded chip carrier for \$42 and in a 68-pin grid array the chip is priced at \$44.

Advanced Micro Devices

901 Thompson Pl
Sunnyvale, CA 94088

Circle number 138

64-kbit SRAM yields 10-ns access time

Arranged as 64k×1 bit, the IDT-10490 is a BiCMOS ECL I/O static RAM with a 10-ns access time. The chip consumes only 120 mA of power and offers ECL-100K compatibility, which keeps logic levels constant through temperature and power-supply fluctuations. The device is available in 22-pin, 300-mil wide cerdip as well as in plastic dual in-line packages. In 100-unit quantities, the chip is priced at \$88.50.

Integrated Device Technology

3236 Scott Blvd
Santa Clara, CA 95052

Circle number 139

Chip set emulates PS/2

A chip set is available that lets users emulate the IBM Personal System/2 Model 30, reduces non-memory chip count and improves system speed by 25 percent, according to the manufacturer. The three-chip set consists of the VL82C031 System Controller, the VL82C032 I/O Controller and the

VL82C033 Disk Controller and Data Separator. In conjunction with the set, a Video Graphics Array (VGA) device is available that provides high-resolution graphics normally reserved for PS/2 Model 50 and higher. In quantities of 1,000, the

three-chip set is priced at \$92.60, while the VGA chip is \$38.60.

VLSI Technology

8375 S River Pkwy
Tempe, AZ 85284

Circle number 140

When it comes to choosing a Network Analyzer, this disk is all you need.

LAN Watch™

Network Analyzer

Demo Disk



One good look at our demo disk will convince you that LANWatch is the only network analyzer software you'll ever need. Indeed, you'll quickly see why *PC Magazine* designated it their Editor's Choice.

View the comprehensive screen displays, conveniently color-coded by protocol. Zoom in on individual packets for all the information you need to locate and diagnose transmission problems. Experiment with the powerful filters.

For all its abilities, LANWatch is inexpensive. There's no need to purchase a dedicated hardware system. Simply tap into your

existing network anytime you like, for a quick glance or a detailed look. LANWatch fully supports Ethernet, Token Ring and StarLAN networks running TCP/IP, XNS, DECnet and VINES. You can even add your own protocol recognition...the code's included.

So, use this publication's bingo card to send for your free demo disk of the only network analyzer you'll ever need: LANWatch.



P.O. Box 150, Kendall Square Branch
Boston, MA 02142 (617) 868-4878
Telex 981970
FAX (617) 864-3943

Runs on IBM PCs, PS/2s and compatibles under DOS 2.0 or later, with Western Digital, 3Com, MICOM-Interlan, Proteon and other interfaces.

CIRCLE NO. 23

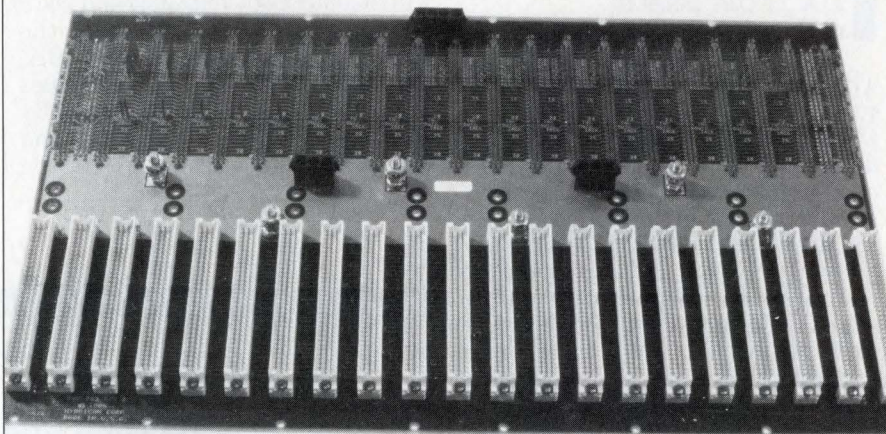
COMPUTER DESIGN OCTOBER 15, 1988 87

MAJOR SYSTEM COMPONENTS

VMEbus monolithic backplane features low-capacitive loading

Two 21-slot monolithic backplanes, the 024-139 and the 024-239, are designed for critical 32-bit applications and VMEbus speed. The six-layer design of the backplanes, with 3-oz power and ground planes, keeps ground shifts and noise potentials to a minimum. In addition, in-board termination contributes to reduced propagation times for the forward and reflected signals.

The optimized geometry design achieves clean transmission of bus signals with low crosstalk and features low-capacitive loading to ensure minimum propagation delays on VME interface circuits. The 024-239 differs from the 024-139 in that the J2 section has extra rows of ground pins to provide shielding between signal lines in I/O cables, which are con-



nected to the A and C rows of each J2 connector.

Each backplane comes in three versions (designated -01, -02 and -03), differing in the types of connectors by which power is brought into the backplane. Customized models are also

available. The price of the backplane is \$1,150.

Hybricon
12 Willows Rd
Ayer, MA 01432
Circle number 141

Industrial terminals comply with NEMA 4X specifications

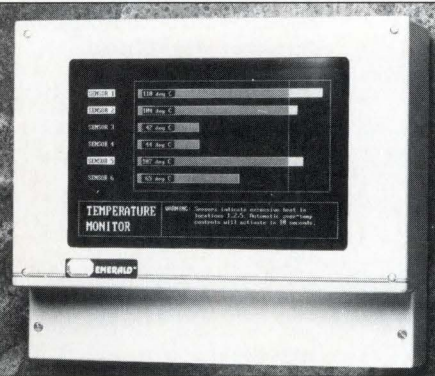
Based on a high-resolution, 640×400-pixel electroluminescent display, the Model CV-10 solid-state terminal is built to the National Electrical Manufacturers Association 4X specification. The display is less than 4 in. in depth, weighs less than 6 lb and can withstand water, dust and dirt

its own text and graphics support, which can produce 80-character×25-line text, 40-character×12-line double high/wide text and complete bit-mapped graphics. A touch-screen feature is optional. In 100-piece quantities, the unit is priced at \$1,795.

Emerald Computers
7324 SW Durham Rd
Portland, OR 97224
Circle number 142

noise feedback onto the power line, reverse voltage protection, and over-current protection on the +5-V main output. Prices start at \$60.

Sola
1717 Busse Rd
Elk Grove Village, IL 60007
Circle number 143



found in harsh industrial environments. Enclosed in polystyrene, the device can also tolerate electrical noise, magnetic fields and vibration, but doesn't require any cooling fans or filters. The terminal comes with

Switcher series ranges from 40 to 150 W

Intended for low-power applications such as personal and mainframe computers and other microprocessor-based environments, the Gold Line series of switching power supplies offers outputs ranging from 40 to 150 W. These open-frame, dual-input units offer minimum efficiencies of 60 percent and are designed to meet MIL-STD-801D vibration/shock specifications. The switchers are capable of operating on dual-input voltages of either 90 to 132 V or 180 to 264 V ac, user-selectable through a jumper-wire adjustment. All models feature built-in EMI filtering to prevent

Power supplies plug to VMEbus systems

A family of plug-in dedicated power supplies for systems using VMEbus architecture, the NCR series features a TTL-compatible open-collector signal that verifies in-spec performance within 500 ms after power-on. Remote control is accomplished by using a 2.4-Vdc TTL signal as the ENABLE, and an open-collector signal as the DISABLE. While the standard models are usually adequate, factory customization is available to comply with special conditions. Three dc outputs are standard.

NCR Power Systems
3200 Lake Emma Rd
Lake Mary, FL 32746
Circle number 144

SOFTWARE

Software package brings parallel processing to Ada

An implementation of Ada designed to run on the manufacturer's multiprocessor system, the Encore Parallel Ada Software Package allows multiple servicing of run-time requests in parallel. The software emphasizes the locking of data structures in the run-time rather than in critical code sections, allowing concurrent access to run-time services by multiple Ada tasks.

Multiple processes are preforked at execution start and are then dynamically available during program execution. Re-using these processes by assigning them to queued Ada tasks awaiting execution reduces the overhead involved in concurrent processing of these tasks.

The number of processes assigned to Ada task execution may be matched to the number of available processors and to the computational needs of others on the system. These optimizations, as well as the process scheduling strategy, are selectable by run-time parameters and don't require recompilation or relinking of the application.

A complete set of tools for compilation, program generation, library management, debugging and source code control are included. Prices for the package start at \$20,000 for commercial users and \$7,500 for educational users.

Encore Computer

257 Cedar Hill St
Marlboro, MA 01752

Circle number 145

Ada compiler offers C performance

The Tartan Ada compiler boasts benchmark performance competitive with optimizing C compilers. Code generated with the software for the Hennessy benchmark programs executed faster than the equivalent code generated by the Sun-3 C compiler in seven out of 10 programs. Tested both internally and at external beta sights, the compiler has completed the required government on-site testing for validation under

ACVC version 1.9. The productline includes VAX-VMS and Sun-3 Ada compilers, and a VMS-hosted cross compiler to the MIL-STD-1750A.

Tartan Laboratories

461 Melwood Ave
Pittsburgh, PA 15213

Circle number 146

68000 C compiler targets ROMable applications

An optimizing C compiler for Motorola 68000 family systems, Crosscode C generates ROMable code for all 68000 family members, including the 68020 and the 68881 floating-point processor. Compiler output code is split into five independent memory sections that can be assigned into ROM or RAM as the user requires. Position-independent code can also be selected. Small and large models



can be chosen for any target processor, with small models using 16-bit offsets for tighter code, while large models allow unlimited code and data sizes. Special facilities on the compiler let users locate their C code in memory. Prices start at \$1,595.

Software Development Systems

3110 Woodcreek Dr
Downers Grove, IL 60515

Circle number 147

68000/20 cross-development software interfaces to PC AT

A software monitor residing in a G-64 bus 68000 or 68020 target board, the Probe Developer and De-

bugger interfaces to an IBM PC or PC AT through an RS-232 serial link. Multiple-trace and single-step modes are supported, as well as 16 breakpoints and a menu-driven user interface. The software lets 10 disk files be displayed concurrently while debugging, so programmers can define their own set of debug commands tailored to the application. The package, which is compatible with C compilers from Microtec, Unix System V, Sun Microsystems and Greenhills, is priced at \$995.

Gespac

50 W Hoover Ave
Mesa, AZ 85210

Circle number 148

FFT library addresses 80386 protected mode

A library of one- and two-dimensional fast Fourier transform (FFT) and digital signal processing (DSP) algorithms, the NDP/FFT library is callable from the manufacturer's 80386 protected mode C and Fortran compilers, NDP C-386 and NDP Fortran-386. The library automatically detects which coprocessors (Weitek mW1167, Intel 80387 or 80287) are present at run time. If more than one is available, the math chip that will optimize performance is selected. The software supports arrays of up to 4 Gbytes and can access the entire protected mode address space of the 80386. The practical limit on array sizes is determined by the physical memory available in the computer. The price is \$250.

Micro Way

PO Box 79
Kingston, MA 02364

Circle number 149

Trademark Information

UNIX is a registered trademark of AT&T Bell Laboratories.

PAL and PALASM are registered trademarks of Monolithic Memories Inc.

GEOMETRY ENGINE is a trademark of Silicon Graphics Inc.

386, 386SX, 376, Intel386, iRMK, iRMX, and ICE are trademarks of Intel.

PRODUCT BRIEFS

Fast-settling FET-input op amp

The AD845 FET-input op amp features a typical settling time of 350 ns to 0.01 percent (for a 10-V step) into a 500- Ω /100-pF load. Starts at \$9.50.
Analog Devices **Circle 150**

Workstation for harsh environments

The RT-60 Unix workstation is designed for military and harsh industrial environments and provides approximately 5 Mips. Starts at \$46,000.
RTG **Circle 151**

Monolithic SRAMs

Using a four-transistor CMOS design, the DPS92256 32k \times 8-bit SRAM features low-operating power (50 mA max), TTL compatibility and access times as fast as 85 ns. Starts at \$30.
Dense-Pac Microsystems **Circle 152**

21-in. gray-scale monitor for Mac II

Designed for use with the Macintosh II, the Silverview is a 21-in. gray-scale monitor capable of displaying from 2 to 256 shades of gray. Starts at \$1,999.
Sigma Designs **Circle 153**

12-bit A-D converter

The ADC12B is a 12-bit dual-slope integrating A-D converter. The cell offers a nonlinearity specification of ± 1 count as well as common-mode rejection ratio of 80 dB.
Sierra Semiconductor **Circle 154**

PAL chip eases timing problems

The PAL22IP6 allows communication between two system components that aren't synchronized to a common clock. It has six edge-activated programmable flip-flops. Starts at \$13.95.
Advanced Micro Devices **Circle 155**

Disk subsystems for Sun

Designed for new and existing VME-bus Sun workstations, the CoDisk series of disk subsystems offers capacities from 330 Mbytes to 1.2 Gbytes in stand-alone cabinets. The disks are controlled by a proprietary 32-bit disk controller that takes a single slot in the Sun system.
CoSystems **Circle 156**

Monochrome monitor

The Greyscale Bundle model RS9503 for PS/2s consists of a 14-in. flat-screen monitor and an Orchid VGA card. \$545.
Relisys **Circle 157**

Parallel/serial converter

The Mali Card matches parallel and serial data transmissions. Parameters can be set dynamically or with DIP switches.
Cartronic **Circle 158**

PRODUCT INDEX

COMPANY, PRODUCT	CIRCLE NO.	COMPANY, PRODUCT	CIRCLE NO.	COMPANY, PRODUCT	CIRCLE NO.
ACC Microelectronics		GW Instruments		Performance Technologies	
<i>XT/AT/PS/2 floppy controllers</i>	135	<i>Macintosh data-acquisition PCB</i>	128	<i>68020 VMEbus single-board computers</i>	125
Advanced Micro Devices		Hauppauge Computer Works		Plessey Semiconductor	
<i>EDC circuit</i>	138	<i>80386 AT mother board</i>	126	<i>flash A-D converters</i>	112
American Research		Hewlett-Packard		Samsung Semiconductor	
<i>small footprint AT-compatible</i>	124	<i>X Windows for DOS/Unix</i>	133	<i>flash A-D converters</i>	113
Analog Devices		Hitachi America		Siemens Semiconductor Group, IC Div	
<i>flash A-D converters</i>	100	<i>flash A-D converters</i>	105	<i>flash A-D converters</i>	114
Analog Devices		Hybricon		Signal Processing Technologies	
<i>12-bit multiplying D-A converter</i>	137	<i>VMEbus backplane</i>	141	<i>flash A-D converters</i>	115
Applied Microsystems		Integrated Device Technology		Signetics	
<i>in-circuit emulator</i>	132	<i>64-kbit static RAM</i>	139	<i>flash A-D converters</i>	116
Brooktree		Integrated Device Technology		Sipex, Hybrid Systems Div	
<i>flash A-D converters</i>	101	<i>flash A-D converters</i>	106	<i>flash A-D converters</i>	117
Computer Design Solutions		Maxim Integrated Products		Software Development Systems	
<i>STD Bus single-board computer</i>	122	<i>flash A-D converters</i>	107	<i>C compiler</i>	147
Computer Products		Megatel Computer		Sola	
<i>data-acquisition board for Bitbus</i>	130	<i>3-W single-board computer</i>	123	<i>40- to 150-W switchers</i>	143
Data Translation		Mercury Computer Systems		Sony	
<i>VMEbus A-D I/O boards</i>	131	<i>floating-point coprocessor</i>	121	<i>flash A-D converters</i>	118
Datel		Metrabyte		Strawberry Tree Computers	
<i>flash A-D converters</i>	102	<i>1-Msample/s A-D I/O board</i>	127	<i>industrial control software</i>	129
Emerald Computers		Micro Power Systems		Tartan Laboratories	
<i>industrial terminals</i>	142	<i>flash A-D converters</i>	108	<i>Ada compiler</i>	146
Encore Computer		Micro Way		Tektronix	
<i>parallel processing for Ada</i>	145	<i>FFT library for 80386</i>	149	<i>flash A-D converters</i>	119
Fujitsu Microelectronics		Motorola Semiconductor Products		TRW LSI Products	
<i>flash A-D converters</i>	103	<i>flash A-D converters</i>	109	<i>flash A-D converters</i>	120
GE Solid State/Intersil		National Semiconductor		VLSI Technology	
<i>flash A-D converters</i>	104	<i>flash A-D converters</i>	110	<i>PS/2 chip set</i>	140
Gespac		NCR Power Systems		Zuken	
<i>68000 development tool</i>	148	<i>VMEbus power supplies</i>	144	<i>routing program for SMDs</i>	136
Gould		NEC Electronics			
<i>logic analyzer</i>	134	<i>flash A-D converters</i>	111		

SAFECON

The Software and Firmware Engineering Conference



Writing Code for High-End Microprocessors

February 7-9, 1989 Fairmont Hotel, San Jose, CA

WHY SAFECON?

Competition in the electronic device market is so intense that design turnaround time is becoming a major factor in the success or failure of a product. Thus, the popularity of ASICs (application specific integrated circuits) and design strategies that promise fast turn times for nearly-custom logic.

At the same time, the newest chips are increasingly complex and their performance depends more and more on efficient firmware. The information provided by vendors on how to use their chips is spotty and not always accurate. As end products become more sophisticated, firmware programming has become an increasingly large portion of the product development cycle.

Software components can provide a piece of the firmware solution. In some cases, these provide a leap forward in the development cycle. Standard software components provide continuity from project to project. But they must be well understood or they just add to the confusion.

The same difficulty lies in the use of high-level languages. Certainly, a programmer writes more code, faster, when using LISP, Pascal, or ADA, but compilers distance the programmer from the hardware--a serious limitation that must also be understood, especially for real-time applications.

Thus **SAFECON**, the new Software and Firmware Engineering Conference. **SAFECON** is the first forum to address these problem areas and provide applications knowledge on a highly-focused basis.

WHO WILL ATTEND?

The **SAFECON** attendee is a software engineer who generally selects the software and tools with little or no input from management.

At **SAFECON**, the attendee will get an in-depth education in the latest programming techniques, tools, and ways to use them in daily work. We call this "next-day education"--what is taught at **SAFECON** today can be used tomorrow. The emphasis is on practical knowledge, not abstract theory. Moreover, **SAFECON** gives the attendee enough information to make an intelligent selection of processors, support chips, software and development tools for his or her specific application.

Attendees will be drawn from Original Equipment Manufacturers (OEMs) that manufacture board and system-level products based on high-performance microprocessor technology.

Similarly, designers of peripheral devices, such as input/output devices, storage systems, communication products and consumer products ranging from blenders to televisions, will find **SAFECON** an ideal refresher on the latest real-time programming methods and the application of the latest controller technology.

WHO SHOULD EXHIBIT AND WHY?

The **SAFECON** exhibition and technical conference is an ideal forum for chip manufacturers and vendors of software-development tools (such as compilers, assemblers, CASE systems, software components and in-circuit emulation equipment).

SAFECON, with its technical program tightly coupled to the equipment exhibited, provides a unique one-on-one, in-person forum to meet quality attendees in an unhurried atmosphere. You'll meet developers specifically interested in software/firmware programming requirements related to high-end microprocessors.

-
- **Seminar/Session Topics:** Understanding the new chips (Intel, Motorola, National, AMD, etc.), including bus structures, instruction sets, memory management, interrupt structure; Leveraging processor performance (registers, burst-made read/write operations to reduce band width); Maintaining software quality (change control, testing); Multi-processing, peer processors) and more . . .

For more information, simply write, FAX, or call: Multidynamics, Inc., 13762 Newport, Ste. 204, Tustin, CA 92680
Phone: (714) 669-1201, FAX: (714) 669-9105, MCI-ID: MULTIDYNAMICS

**Going
fast.**

Introducing ultra high-speed ECL logic packaged to meet your needs.

If the race belongs to the swift, then you're in fast company with Fujitsu Microelectronics. Because we'll give you all the high-speed ECL logic you need to win.

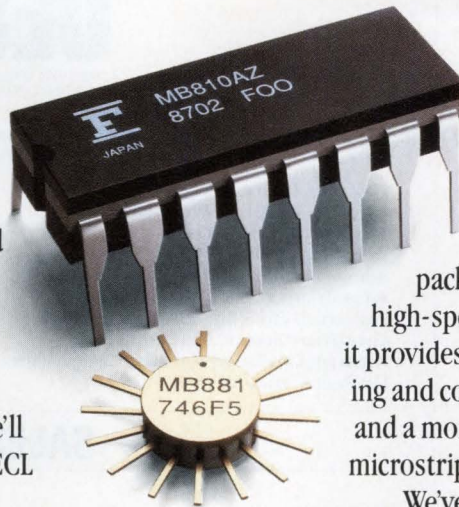
Whether you choose the 3GHz MB880 series, the 1.5GHz MB810 series, or our complementary 1-2.5GHz master slice series, the MB1600, MB1700 and MB1800, you get the fastest UHECL logic available. And you get it packaged to go. Because it's on the shelf now.

You can even mix and match the MB880 and MB810 discrete logic series with the MB1600, MB1700 and MB1800 master slice series for optimum system performance and cost.

Take the 3GHz MB880 discrete logic series and associated 2.5GHz MB1800 UHECL master slice array, for example. They were designed for ultra high-performance systems where speed is an absolute must.

Which makes them ideal for fiber-optics, telecommunications, video-graphics processing and high-speed computing applications.

When it comes to packaging for ultra-speed performance, we've got the MB880 and the master slice series all wrapped up in a compact, circular, ceramic flat package with radial leads.



This unique package is designed for ultra high-speed applications. And it provides you with easier mounting and cooling, lower crosstalk and a more efficient interface to microstrip transmission lines.

We've even made it easy for you to check out our incredibly fast ECL process speeds for yourself. Our optional ECL test kit provides you with hardware to check out the performance of the circular ceramic flat package devices.

The 1.5GHz MB810 discrete logic series and 1.0GHz MB1600 and MB1700 master slice series are designed for use in high-speed test equipment, instrumentation and general logic applications. And they're conventionally packaged in 16-pin cerdip and ceramic flat-packs to provide performance at a lower cost.

What's more, you don't have to worry about compatibility, either. Because the MB880 and MB810 discrete logic series, and the MB1600, MB1700 and MB1800 master slice array series are logic-level compatible with ECL 10K and 10KH series.

Best of all, they're from Fujitsu Microelectronics. The partner you can count on. Now and in the future. Providing you with the edge you need to always stay ahead.

If you'd like to know more about the UHECL series, call 800/642-7616. We'll show you how to fall in with a fast crowd.

FUJITSU

FUJITSU MICROELECTRONICS, INC.
INTEGRATED CIRCUITS DIVISION
The edge you need in a changing world.

Integrated Circuits Division • 3545 North First Street • San Jose, CA 95134-1804

CIRCLE NO. 28

ADVERTISERS INDEX

ADVERTISER	PAGENO.	CIRCLE NO.
Accel Technologies.....	95	228
Advanced Micro Devices, Inc.....	42, 43	32
Advanced Processing Labs.....	49	24
Aldia Systems, Inc.....	95	227
Applied Microsystems.....	28, 29	11
Bo-Sherrel Co.....	95	222
Bo-Sherrel Co.....	95	221
Burr-Brown Corporation.....	44	21
CAD Software, Inc.....	CV3	29
CalComp.....	2	3
Ciprico.....	CV2	1
Control Data Corp.....	35	12
Data I/O.....	11	6
Digi-Data Corp.....	35	22
Excelan, Inc.....	39	14
FTP Software.....	87	23
*Fujitsu.....	92, 93	28
GE Plastics.....	69, 70, 71, 72	19
Hitachi America, Ltd.....	25	10
Hybricon Corp.....	95	225
Intel Corp.....	55, 56, 57	16
KMW Systems Corp.....	61	17
Mentor Graphics Corp.....	6, 7	17
Micro Computer Control.....	95	226
Minc, Inc.....	49	25
Motorola.....	1	
Motorola.....	8	5
*MultiDynamics, Inc.....	91	*
National Instruments.....	95	229
National Semiconductor Corp.....	4, 5	4
†Philips.....	92, 93	31
Sharp Electronics.....	15	7
Sierra Semiconductor Corp.....	80, 81	20
Standard Microsystems.....	17, 18, 19, 20	9
†Themis 29.....	89, 91	27
Triad Semiconductors.....	95	223
Versitron Inc.....	CV4	30
Wave Mate Inc.....	95	224
Whitesmiths, Ltd.....	16	8
The Wollongong Group.....	37	13

*Domestic Issues Only †International Issues Only

The Advertisers' Index is published as a service. The publisher does not assume liability for errors or omission.

COMPUTER DESIGN

THE FIRST MAGAZINE OF SYSTEM DESIGN, DEVELOPMENT AND INTEGRATION

Executive Office: P.O. Box 417, 119 Russell St, Littleton, MA 01460-0417

(508) 486-9501 (800) 225-0556 Telex: 883436 ELN: 62649490 FAX: (508) 486-9397

Publisher, David L. Allen

Associate Publisher, John C. Miklosz

Marketing Services Manager, Mary M. Gregory

Sales Promotion and Research Manager, Judy Leger

Administrative Assistant, Tina LePage

Advertising Coordinator, Adrienne Adler

Postcards/System Showcase/Recruitment, Shirley Athorn, Barbara Kovalchek

Circulation Director, Bob Dromgoole

Assistant Circulation Manager, George Andrew

List Rental, Bruce McCarthy

SALES OFFICES

New England/Upstate New York/ Florida/E. Canada

Kevin Callahan
P.O. Box 605
North Scituate, MA 02060
Tel: (617) 545-6603

New York/New Jersey/ Pennsylvania/Delaware/Maryland/ North-South Carolina/Georgia

Neil Versen
Park 80 West, Plaza Two
Saddle Brook, NJ 07662
Tel: (201) 845-0800
Fax: (201) 845-6275

Midwest/Ontario, Canada

Robert D. Wentz
9501 West Devon, Suite 203
Rosemont, IL 60018
Tel: (312) 518-9191
Fax: (312) 698-2675

Southwest

Eric Jeter
3050 Post Oak Blvd., Suite 200
Houston, TX 77056
Tel: (713) 621-9720
Fax: (713) 963-6285

Southern California/Colorado

Tom Boris, Greg Cruse
2082 SE Bristol, Suite 216
Santa Ana, CA 92707
Tel: (714) 756-0681
Fax: (714) 756-0621

Northern California

Tom Boris, John Sly, Bill Cooper
1000 Elwell Court, Suite 234
Palo Alto, CA 94303
Tel: (415) 965-4334
Fax: (415) 965-0255

Oregon

Tom Boris
2082 SE Bristol, Suite 216
Santa Ana, CA 92707
Tel: (714) 756-0681
Fax: (714) 756-0621

Washington

John Sly
1000 Elwell Court, Suite 234
Palo Alto, CA 94303
Tel: (415) 965-4334
Fax: (415) 965-0255

U.K./Scandinavia

David Round
69 Imperial Way
Croydon
Surrey CR0 4RR, England
Tel: 01 686 7655 Telex: 938420
Fax: 01 688 2134

France/Belgium/S. Switzerland/ Spain/The Netherlands

Daniel R. Bernard
247, Rue Saint Jacques
75005 Paris France
Tel: (1) 43 54 55 35
Telex: 214235F MISIVZ
Attn: Missitex: PENNWELL
Fax (1) 4707 59 01

W. Germany/Austria/ N. Switzerland/Eastern Europe

Johann Bylek
Verlagsbuero Johann Bylek
Stockaekerring 63
D-8011 Kirchheim/Muenchen
Federal Republic of Germany
Tel: 089 903 88 06
Telex: 529355 vbb d

Italy

Luigi Rancati
Rancati Advertising
Milano San Felice Torre 5
20090 Segrate Italy
Tel: 2 7531445
Telex: 328601 RANCAD I
Fax: 02 7532354

Japan

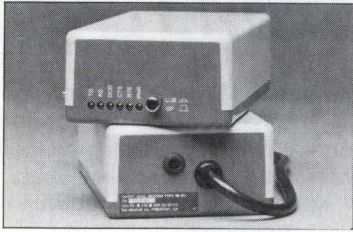
Sumio Oka
International Media Representatives, Ltd.
2-29 Toranomom 1-chome
Minato-ku, Tokyo 105 Japan
Tel: 03-502-0656
Telex: J22633 MEDIAREP
Fax: 03-591-2530

Southeast Asia

Anne Goh-Taylor
Seavex, Ltd.
400 Orchard Rd.
10-01, Orchard Towers
Singapore 0923
Republic of Singapore
Tel: 734-9790
Telex: 35539 SEAVEX RS
Fax: 732-5129

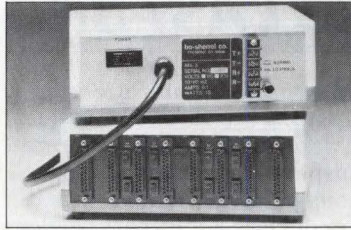
Jay G. Seo
Yong-Jin Park
Doobee International, Ltd.
Center Building (Byulgan)
1-11 Jeong-dong, Choong-ku
CPO Box 4557
Seoul, Korea
Tel: 776-2096
Telex: K27117 DOOBEEES
Fax: 755-9860

SYSTEM SHOWCASE



M-5S Synchronous Short Haul Modem \$219.00. Features include: EIA RS232 or CCITT/V .24 interface—speeds up to 38400 bps—internal or external clocking—clear to send delays—optical isolation—operating distance up to 10 miles—DTE/DCE switch selectable—LED indicators—screw terminal or RJ11—two year warranty. For more information: Bo-Sherrel Company, Inc., 36133 Niles Blvd., Fremont, CA 94536 or phone (415) 792-0354.

CIRCLE NO. 221



MX-3 8 Channel TDM Multiplexer \$389.95. Features include: EIA RS-232 or CCITT/V .24 interface—speeds up to 19200 bps—no modem needed up to 5000 ft.—completely transparent to data format—DTE/DCE switch selectable on each channel—composite link test for diagnostic—built-in lightning protection. Bo-Sherrel Co., Inc., 36133 Niles Blvd., Fremont, CA 94536 or phone (415) 792-0354.

CIRCLE NO. 222



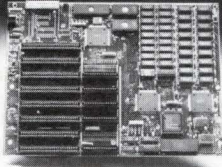
TRIAD'S GRAPHICS COLOR PALETTE OFFERS ENHANCED COLOR CAPABILITY!

THE TR9C1710 IS VGA STANDARD PIN/FUNCTION COMPATIBLE. SUPERIOR PERFORMANCE: INTEGRATED COLOR LOOK-UP TABLE, TRIPLE VIDEO DAC, LOGIC & ANALOG INTERFACE ON 1 CHIP REDUCES SYSTEM COST. ENHANCED (256) COLORS. UNLIMITED ACCESS TO LOOK-UP TABLE. 66 MHZ CLOCK RATE. FOR A BETTER SYSTEM SOLUTION, CALL 800-288-1874.

5575 Tech Center Dr., Colorado Springs, CO 80919

CIRCLE NO. 223

BULLET-286AT THE UNBEATABLE VALUE

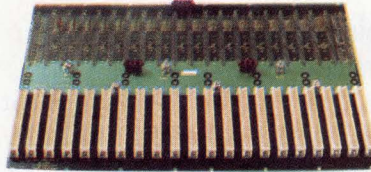


- 10, 12.5, and 16 MHz operation
- 80286 PC/AT compatible
- Wave Mate proprietary BIOS
- State-of-the-art VLSI design
- Disk cache software included
- PC/XT (Baby AT) form factor
- 0 wait state RAM (512K to 4MB)
- EMS RAM supported
- Optional 80287 with ext. clock
- Made in USA, 2 year warranty
- No risk -- money back guarantee

WAVE MATE INC. 2341 205th Street, #110, Torrance, CA 90501
Tel: (213)533-8190 Fax: (213)533-5940

80286 MOTHERBOARDS CIRCLE NO. 224

!!NEW!!



21-SLOT VME MONOLITHIC BACKPLANES

Send for FREE Product Data:
21-Slot and other sizes

Hybricon

12 Willow Road, Ayer, MA 01432
EAST COAST WEST COAST
(508) 772-5422 (602) 921-1824

CIRCLE NO. 225

8051

C COMPILER ASSEMBLER SIMULATOR SUPPORT LIBRARY

• Call today for a FREE technical bulletin •

MICRO COMPUTER CONTROL
P.O. Box 275 - Hopewell, NJ 08525 USA
Telex 9102404881 MICRO UG

FOR IMMEDIATE ACTION CALL:
(609) 466-1751

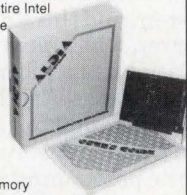
CIRCLE NO. 226

IT'S EASY TO LOCATE ROM SOFTWARE SUPPORT

PC-LOCATE: Produce ROM-able code from your "exe" files. PC-LOCATE assigns physical addresses to the re-locatable image based on user inputs. PC-LOCATE supports the entire Intel processor family including the 8086, 8088, 80186, 80188 and 80286.

PC-PROMPAK: A PROM/ROM expansion board for IBM and IBM-compatible computers. PC-PROMPAK provides up to 384 Kbytes of expansion memory and supports most 28-pin JEDEC compatible devices.

PC-ROMDRIVE: Create a "Diskless PC" that can include MS-DOS and your application program. Program execution can be automatically invoked through the use of an "autoexec.bat" file.



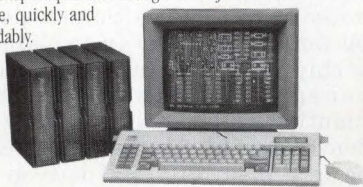
ALDIA
SYSTEMS INC.

P.O. BOX 37634 PHOENIX, AZ. 85069
(602) 866-1786

CIRCLE NO. 227

Tango™ Sets The Pace!

Tango's ease-of-use, rich functionality and crisp output have brought *tens of thousands* of boards to life, quickly and affordably.



Start-to-finish design tools include:

Tango-Schematic With Library Manager.	\$495
Tango-PCB 1 mil Grid, 9 Layers, Gerber Output.	\$495
Tango-Route Autoroutes 90+% . Fast!	\$495
Tango-Tools 8 Money-Saving Utilities.	\$295

Let's discuss *your* design needs Toll-Free, or order a full function Evaluation Pkg, just \$10. VISA/MC.

800 433-7801 619/695-2000 Satisfaction guaranteed.

ACCEL Technologies, 7358 Trade St., San Diego, CA 92121

CIRCLE NO. 228

IEEE-488 for VMEbus & MULTIBUS



Hardware Options — High-speed DMA or low cost programmed I/O
Software Support — UNIX, PDOS, MTOS, VERSAdos, Aegis



Call for FREE Catalog
512/250-9119 or 800/531-4742

CIRCLE NO. 229

LAST BITS LAST BITS LAST BITS LAST BITS LAST B

Control Data establishes separate disk drive group

In an effort to improve its marketing flexibility and ability to respond to customer needs, Control Data (Minneapolis, MN) is establishing its highly successful Data Storage Products Group as a stand-alone subsidiary operating under the moniker Imprimis Technology. Lawrence Perlman, Data Storage Group vice-president, will head Imprimis.

After a difficult few years in the mid-1980s, the Data Storage Group under Perlman has assumed a strong position in the disk drive industry with an array of high-capacity, fast-access 8-, 5¼- and 3½-in. Winchester drives. With its independent status, the new subsidiary will be free to seek strategic alliances, joint ventures and partnerships in the fast-moving disk drive industry and to sell a minority interest of its stock to the public.

Motorola and Cherry agree to exchange bipolar technologies

Motorola Semiconductor Products Sector (Phoenix, AZ) and Cherry Semiconductor (East Greenwich, RI) have agreed to collaborate to achieve compatibility in manufacturing processes for selected high-volume, bipolar linear ICs. Each company will have the technical capability to alternate source certain bipolar ICs designed by the other. The agreement will effectively offer better service to customers who require alternate supply sources for bipolar devices.

PC communications made simple

Intel's Personal Computer Enhancement Operation (Hillsboro, OR) and Digital Communications Associates (Alpharetta, GA) have unveiled and put into public domain

a standard communications programming interface that will let software developers incorporate transparent communications among personal computers and other devices. Third-party endorsements have come from a number of software houses, including Lotus Development, Microsoft, Borland International and Novell. The specification, called the DCA/Intel Communicating Applications Specification (CAS) Version 1.0, is the result of a combined effort to provide a seamless standard for PC and non-PC users to share PC-generated information, including documents, spreadsheets, graphics, data bases and electronic mail.

Joint venture produces CAE tools

An agreement for the development and marketing of an advanced set of electronic CAE tools has been struck between Silvar-Lisco (Menlo Park, CA) and N.V. Philips (Eindhoven, the Netherlands). The products will be used in a variety of application-specific IC applications and are targeted for use by a number of the product groups within the Philips organization. In addition, Silvar-Lisco will commercialize the resulting tools and market them to other potential users.

Mathematical application tools made for RISC

Customers wanting floating-point capabilities for the Am29000 32-bit RISC microprocessor from Advanced Micro Devices (Sunnyvale, CA) won't have to buy an accelerator chip or write extra code, thanks to an agreement between AMD and Quantitative Technology Corp (Beaverton, OR). Under the terms of the agreement, QTC will develop trap handlers to implement IEEE standard instructions that emulate all the functions of a floating-point processor chip in software. The trap

handlers are best suited for systems with limited floating-point requirements, such as various embedded controller designs, spreadsheets, low-end workstations or simple statistics programs.

Space station contract targets gate arrays

International Microcircuits (Santa Clara, CA) has been awarded \$2.75 million in production contracts for military-standard applications in defense, outer space and other high-reliability environments. Production quantities of the manufacturer's mil-spec screened gate arrays are being delivered to Rockwell International's Avionics Division (Cedar Rapids, IA) for use in the Navstar Global Positioning Satellite. In addition, Canadian Marconi (Montreal, Quebec), Singer's Kearfott Division (Wayne, NJ) and Magnavox Marine Division (Fort Wayne, IN) are receiving the gate arrays for use in NASA's space station project as well as other defense applications.

Apollo announces Portable Software Group

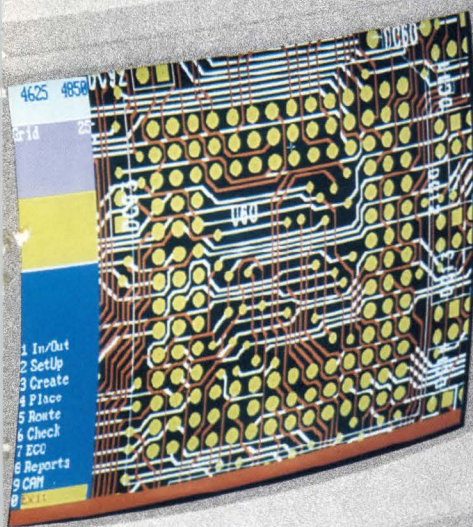
In what seems to be an industry first, Apollo Computer (Chelmsford, MA) has announced that it will offer object-code versions of its software to competing vendors. The newly formed Portable Software Group will open up three Apollo products to other users and vendors: the industry-standard Network Computing System, the Open Dialogue object-oriented interface creation system and the Network License Server, which provides for the concurrent usage licensing of software applications. Apollo's move seems to be an attempt to gain strength in the Open Software Foundation while positioning its software products as industry standards.

COMPUTER DESIGN (ISSN-0010-4566) is published twice monthly, except in July and December, by the Advanced Technology Group of PennWell Publishing Company, PO Box 417, 119 Russell St., Littleton, MA 01460. Second class postage paid at Tulsa, OK 74112. COMPUTER DESIGN is distributed worldwide to qualified subscribers free of charge. Annual subscription price for non-qualified subscribers: \$70 in the U.S.A., \$110 elsewhere. Call (918) 831-9401 for a subscription application. Microfilm copies of COMPUTER DESIGN may be purchased from University Microfilms, a Xerox Company, 300 North Zeeb Rd., Ann Arbor, MI 48106. POSTMASTER: Send change of address form to COMPUTER DESIGN, Circulation Department, PO Box 3466, Tulsa, OK 74101.

© 1988 COMPUTER DESIGN by PennWell Publishing Company. All rights reserved. No material may be reprinted without permission from the publisher. Officers of PennWell Publishing Company: Philip C. Lainger, Jr., Chairman and Chief Executive; Joseph A. Wolking, President; John Ford, Senior Vice-President; Carl J. Lawrence, Senior Vice-President; John Maney, Vice-President/Finance.

PADS SUPERSTATION™

Completely Integrated CAE/CAD



The Integrated PADS-Superstation™ is a new and powerful PC-Based Design Station that allows the Engineer or Circuit Designer to perform the entire design sequence from cradle-to-grave. Every decision required in the design effort, from Logic Capture to Printed Circuit Design, to 100% Connection Routing, to Checking, to generating Manufacturing Aids is made by the responsible engineer and implemented on a single, fully integrated CAE/CAD SUPERSTATION!

LOGIC CAPTURE

The PADS-CAE system maximizes Logic Capture automation, while allowing the engineer to concentrate on the design task. This high degree of automation results from the use of a new type of database: A Design-Oriented-Database. All drawing sheets of the design are simultaneously available - not merely a single sheet, as with most other Logic Capture systems.

Among the many advantages of this new database are Automatic (hands-off) entry of Reference Designation, gate and pin data, on-line real time

data checking across all drawing sheets, rapid paging from sheet-to-sheet, and instantly available (no batching) Annotation Lists to both PADS-PCB and other board CAD systems using FUTURE NET™

The most tedious and error-prone phase of Engineering Documentation, i.e., Engineering Change Order (ECO), is easy with PADS. ECOs generated in either the Schematic, or the Board database are used to automatically (hands-off) update the corresponding database.

BOARD DESIGN

PADS-PCB is today's most popular board CAD System and is the heart of the Superstation. PADS-PCB has revolutionized Printed Circuit Board CAD expectations by demonstrating an alternative to today's \$100,000 Work Stations. Thousands of designers, engineers, and Board Design Centers use PADS-PCB - and for good reasons: 1 mil resolution, 30 layers, large board (over 400 14 pin ICs per board), complete SMD support, fine line (1, 2 & 3 tracks between IC pins), both Analog & Digital capability, fast Air Gap & Data checking, Gate & Pin swapping, dynamic rubber banding, rats' nest display, interactive and auto placement, interactive & auto routing, and all required Manufacturing Aids (CAM).

PADS-PCB is tightly coupled, both to and from PADS-CAE, and from other Logic Capture systems using FutureNet™

100% COMPLETION AUTOROUTING

The most demanding phase of board design is routing the connections; approximately 70% of the board design effort is spent in this time consuming, labor-intensive task. Every Designer and Engineer's dream is to have a 100% completion autorouter, and PADS-Superrouter™ brings this capability to the Superstation™

Here's how it works: the Designer places the components on the board, selects the "Route"

command, and the SUPERROUTER takes over, routing around the clock, hour after hour, performing this tedious task to completion, or near completion, while the Designer is involved in other tasks. It's that easy! PADS-Superrouter allows the designer to set up a routing strategy based upon the requirements of each board. A costed Maze Search algorithm, using obstacle hugging on a 10, 20, 25 or 50 mil grid, and up to 12 simultaneous layers attempts to achieve 100% completion. A Rip-up-and-Retry Algorithm is used to obtain this objective.

Following routing, an Ease-of-Manufacturing Optimizer prepares the board for maximizing the manufacturing yield. Bends and curves put in by obstacle hugging are removed, closely spaced tracks are unpacked, corners are made at 45°, and all possible Vias are removed. The results equal or exceed that of the most experienced board designer.

LOW PRICE

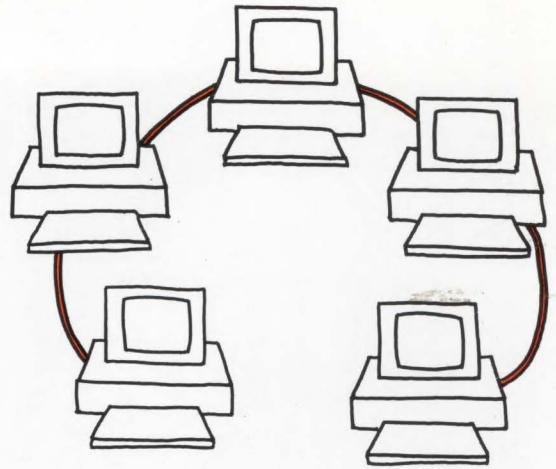
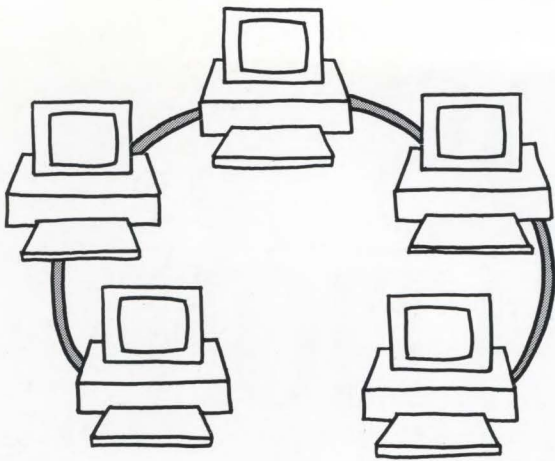
While the performance and functionality of the PADS-SUPERROUTER is equal to any Workstation at any price, its price is competitive with the very low cost PC-based CAD systems. The price has been structured to allow every engineer in the organization to have his/her own personal SUPERSTATION™

EVALUATION PACKAGE

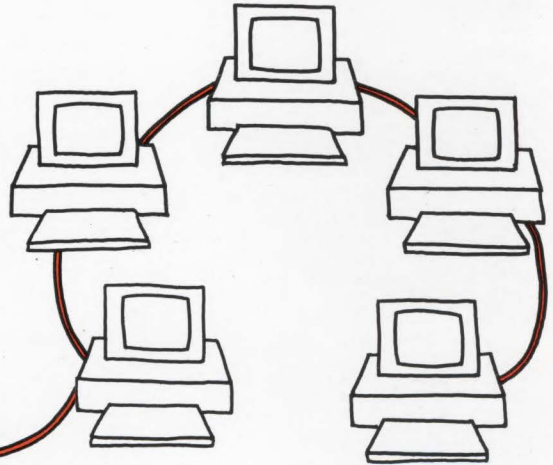
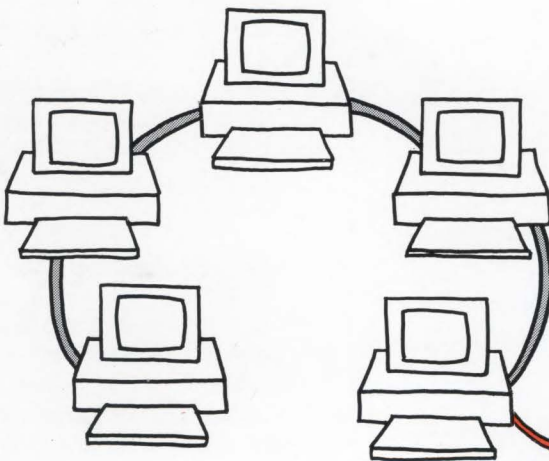
So that you can appreciate the impact the PADS-Superstation™ will have in your organization, we have created a Superstation Evaluation Package. It is available at no cost to qualified engineers and designers. Please call our Sales Department at (800) 255-7814; Inside Mass. (508) 486-9521.



CAD Software, Inc.
Suite #6
119 Russell Street
Littleton, MA 01460



This LAN is your LAN, this LAN is our LAN,



this LAN was made from yours and ours.

Your Ethernet LAN probably uses a copper medium, either coax or twisted pair.

Our Ethernet LAN uses fiber optic cable.

If you connect them with a Versitron Coax/Fiber Tap, our part of the LAN will have all the advantages of fiber without replacing your part. Fiber gives you longer cable runs and you can run it where there's just no room for Coax. Fiber is impervious to power-line surges, lightning and ground potential differences between nodes. And fiber

media is more secure than copper.

Our LAN uses industry standard Network Interface Controllers just like yours. And it works under the same software that yours does.

It's easy to try fiber. For less than \$1,000, our Coax to Fiber Starter Kit will let you add workstations to a coax Ethernet LAN using fiber optic media. Call (800) 537-2296 to order it.



9005-8 Junction Drive Annapolis Junction, MD 20701 (800) 537-2296 (301) 497-8600 Telex 4972387

CIRCLE NO. 30