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COMPUTER DESIGN

DECEMBER 1986

THE MAGAZINE OF SYSTEM DESIGN AND INTEGRATION

TECHNOLOGY/PRODUCT TRENDS '86/'87

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CIRCLE NO. 2

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THE MAGAZINE OF SYSTEM DESIGN AND INTEGRATION

SYSTEM TECHNOLOGY

Integrated Circuits

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55 **RISCs and parallel processors drive multiprocessing innovations**
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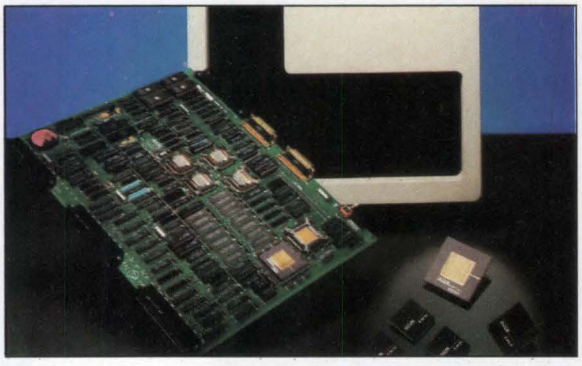

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81 **Advances in CMOS and ECL process technology yield powerhouse ICs**
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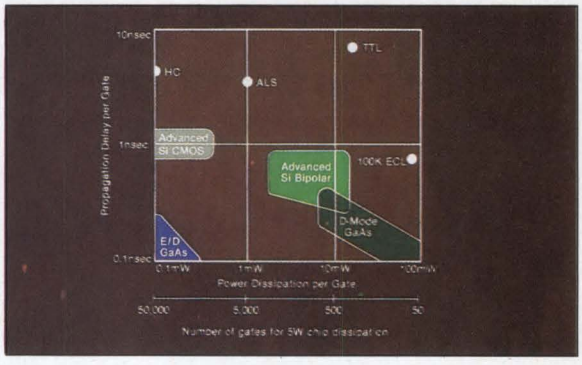

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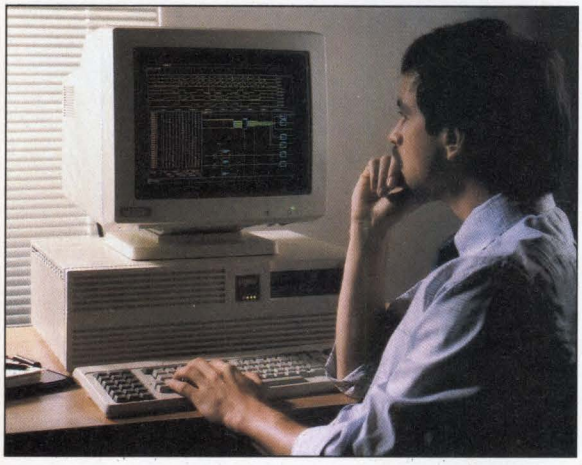
Design and Development Tools

105 Price and performance improvements drive design tool market
Competitive pressures and technological advances have combined to make CAE/CAD systems, development systems, and test and measurement tools more accessible to the average system designer.



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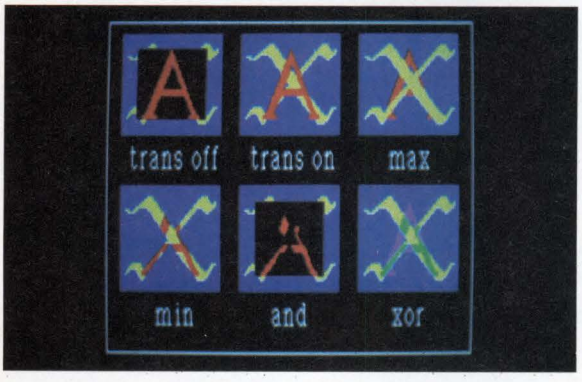
127 Graphics developments geared toward speed and capacity
Advances in graphics technology provide far-reaching cost/performance improvements.



PRODUCT TRENDS '86/'87

Computers and Data Communications

66 Expandable parallel processor serves supermini to low-end supermicro market...Family of data acquisition and control boards serves VMEbus...Two mid-range processors improve performance using innovative VLSI CMOS architecture...Apollo expands DN570/580 workstations with turbo package ...Communications controller supplies high-speed connection.

Integrated Circuits

94 68000 family is expanded with second generation 32-bit MPU...New process generates fast 16-×16-bit multiplier-accumulators...D-A converter chip offers 3-D graphics for PC applications...32-bit chip set offers 30-MHz performance for multiuser systems...80386 logic support implemented in seven-chip set.

Design and Development Tools

116 Desktop workstations challenge minicomputers...PC-based workstations tackle IC and printed circuit board layout...Analog circuit simulator targets system-level designs...Tool set completes CAE software environment...Software tool gives expert know-how to novice designers...Logic analyzer provides unique measurement capabilities.

Peripherals, Graphics and Imaging

138 520-Mbyte disk drive cuts response time...32-bit graphics processor features on-chip display control...Tektronix extends 41000 line while lowering prices...Software and boards deliver high-speed image processing to IBM PC AT...Low-cost VMEbus board overlays graphics on live images.

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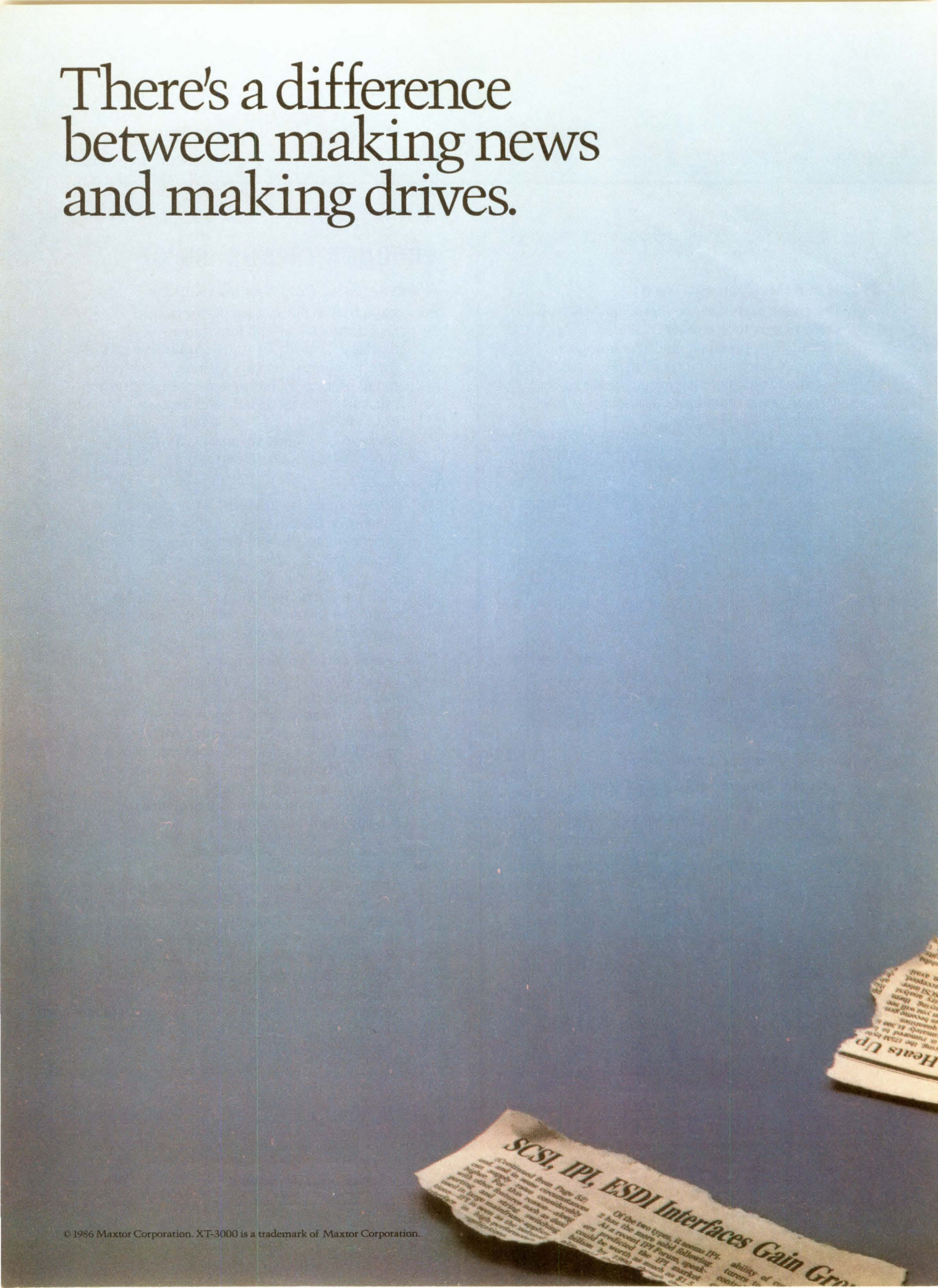
There's a difference between making news and making drives.



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While others are announcing high-capacity SCSI drives, Maxtor is shipping them.

That should come as no surprise. Because our new SCSI drives are based on the same proven technology as the tens of thousands of ST506/412 and ESDI drives we've already shipped.

They're called the XT-3000™ Series. The difference is they feature an embedded SCSI controller with an extensive command set.

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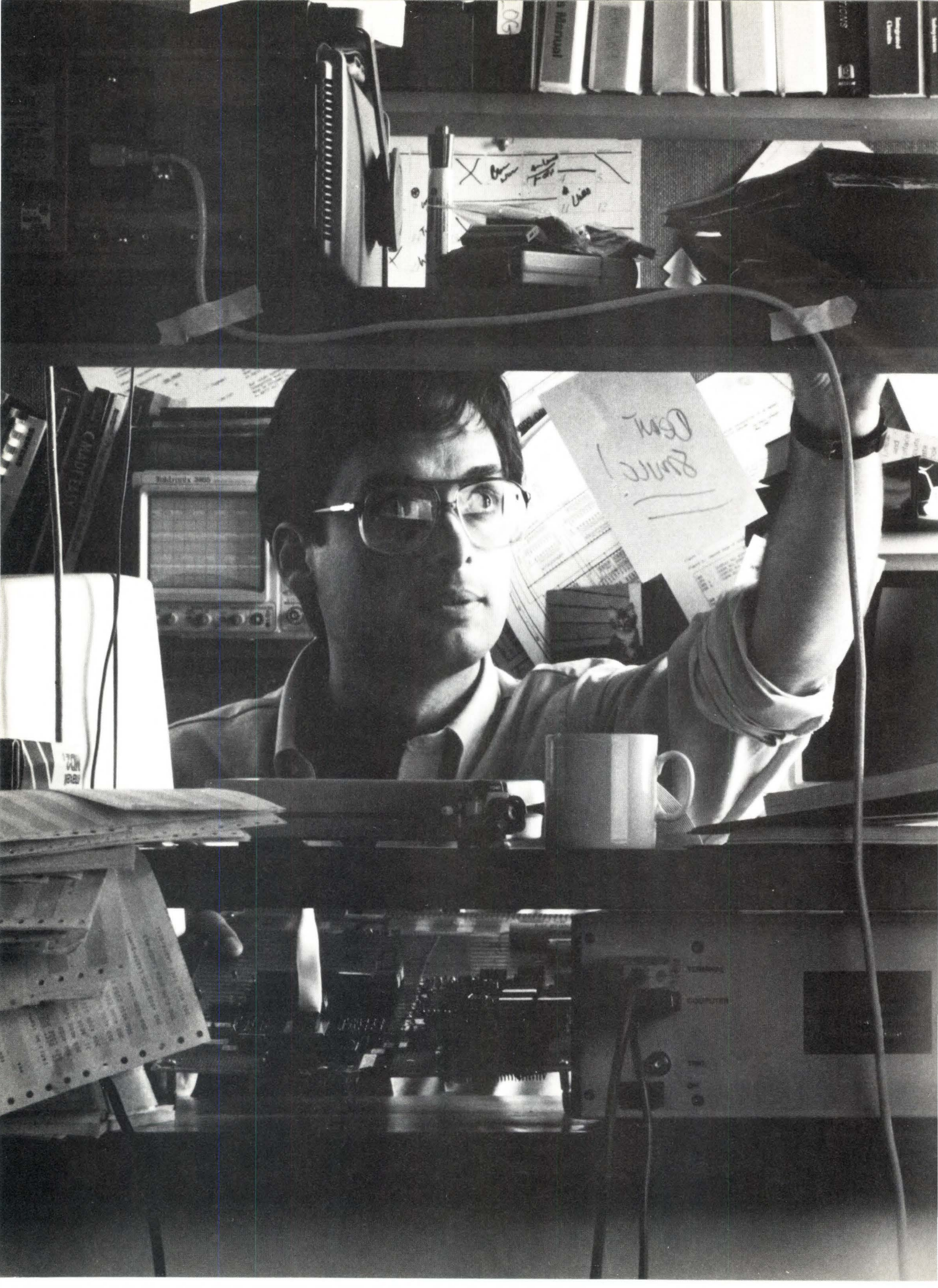

The difference between a few more tweaks and a few more weeks.

Introducing the CIDS method from Applied Microsystems. The first painless way to assemble the debug environment you really need.

You could spend weeks looking for the right tools, plus months trying to make them work together, and still not have a system that was truly integrated. That's why Applied Microsystems has developed the CIDS method.

CIDS stands for Customer Integrated Development Systems and the concept is simple. You choose your hardware and software tools. Applied Microsystems makes sure they work together seamlessly.

HOSTS	OPERATING SYSTEMS	TARGETS	LANGUAGES	TOOLS
VAX MicroVAX UNIX-oriented workstations · Apollo · Sun · IBM AT MS-DOS workstations · PC · PC XT · PC AT	VMS ULTRIX UNIX XENIX MS-DOS	8048 family 8080, 8085, 8086/88, 80186/188 and 80286 68HC11, 6800/2/8, 6809/9E, 68000/8/10 and 68020 Z80, MK3880/4 and Z8001/2/3 NSC-800	C Pascal FORTRAN PL/M Assembler	Assemblers Linkers Locaters Compilers Symbolic debuggers Source-level debuggers Emulators

A stand-alone or host-control system of fully integrated debug tools built on high performance emulation.

An overview of Customer Integrated Development Systems.

Whether you're working on an 8-bit, 16-bit or even a 32-bit design, we let you tailor the emulation and debug tools you need. Everything from symbolic and source-level debuggers to assemblers, cross-compilers and utilities. The chart gives you some idea of the power and convenience of the CIDS method, but it can only hint at the control and visibility you will enjoy.

Validate™ links emulation with source-level debugging.

When your software engineers only speak C and your emulator only speaks assembler, your tools are worthless. Or if your function is in assembler and your debugger only speaks C, it's the same dead end.

The power of the Validate environment is that it works equally in high level languages and in assembler. You don't sacrifice any power or comfort.

Real-time emulation for the 68020 and 80286.

Applied Microsystems lets you emulate high performance targets at top speed. Up to 16.6 MHz for the 68020. And 12.5 MHz for our new 80286 with full function implementation. Free access to the virtual protect mode makes transparent emulation possible using logical or physical addresses.

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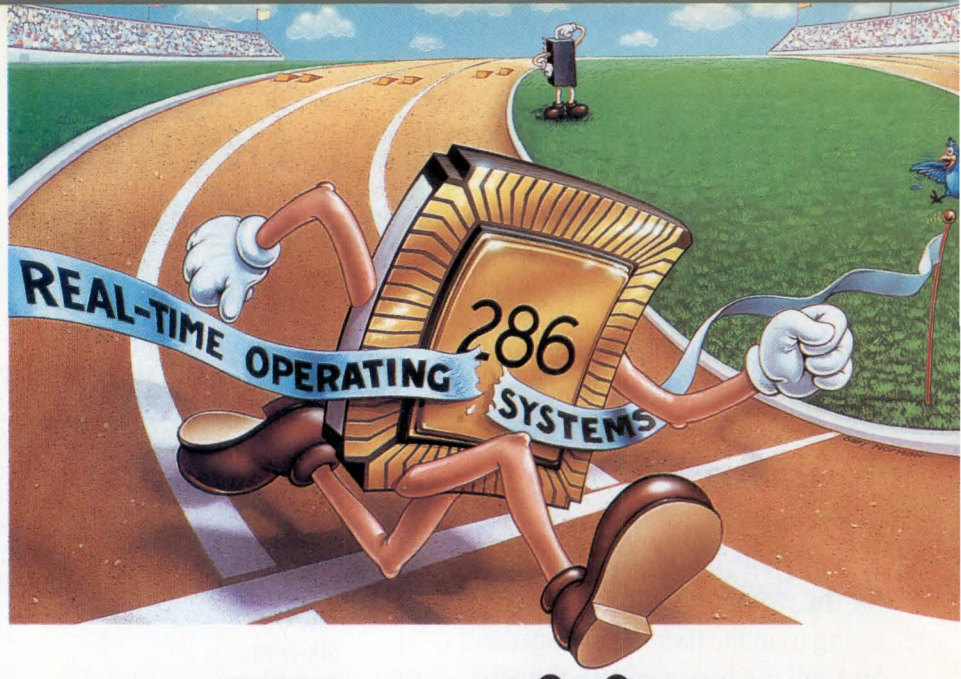

WHO WE ARE.

We're RTCS, Real-Time Computer Science Corporation. Giving it all we've got so that you can get the most from what you have. It's our philosophy. And by constantly extending our lead, we can extend your capabilities. Like the capabilities of IBM and compatible personal computers to complete more sophisticated and complex tasks.

We have no competition so we have to top ourselves. Introducing RTX/286.

We got good by specializing. For example, our specialized configurations of Intel's iRMX86 and iRMX286 to run on IBM PC's and compatibles. By the way, Intel's iRMX86 was chosen because of its maturity. Since its introduction in 1980 it has become the de facto standard for real-time multitasking operating systems. iRMX is supported by an active and aggressive international users group.

RTX286 AND WHAT WE'RE DOING NOW.

It took hard work to make the IBM AT work harder. By configuring RTX286 in, you're able to get more out, like minicomputer power. 16MB addressability. Protected memory. Plus the same real-time multitasking capability of other RTCS operating systems.

Moving farther ahead, we'll soon be adding support for some "almost compatibles" like the HP Vectra, the ITT XTRA and many more. Compaq's 286 Portable, Portable II and 286 Deskpro as well as Sperry IT and Honeywell PC are already supported.

WHAT WE'VE DONE.

1982 *RTCS/UDI runs Intel MDS software on IBM PC*

1983 *PC/RTX real-time multitasking OS for IBM PC*

1984 *PC/RTX real-time multitasking OS for IBM XT*

1985 *AT/RTX real-time multitasking OS for IBM AT*
PC/RTX-C configurable OS for IBM XT
AT/RTX-C configurable OS for IBM AT

1986 *RTX286 real-time multitasking OS for IBM AT*
RTX286-C configurable OS for IBM AT

1987 *RTX386 real-time multitasking OS for future IBM developments*
RTX386-C configurable OS for future IBM developments

Nearing the finish line is Open Net local area network for RTX and a new, powerful RTX debugger. As for RTX386, we're making great strides forward.

WHO WE'LL BE.

We've been the leader, and we'll continue to be. Our real-time multitasking operating systems for IBM and compatible personal computers can give you the lead, too. Call RTCS today, **(805) 987-9781** or write 1390 Flynn Road, Camarillo, CA 93010. Telex: 467897 RTCS CI. Who knows, it may put you so far ahead, there won't be a competitor in sight.

RTCS

Getting the most from what you have.

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CIRCLE NO. 5

UP FRONT

150-MFlops GaAs minisupercomputer planned

Vitesse (Camarillo, CA) plans to apply its enhancement/depletion mode LSI technology to produce the first GaAs minisupercomputer. The initial product, which has been out for about two years, will use ECL technology and deliver 150 MFlops. Product marketing manager Tom Duggan expects the computer to deliver 20 times the performance of a VAX 8600 at the same cost. The GaAs version, due out between 1988 and 1989, should attain twice the performance advantage of the ECL version.—*K.M.*

Modeling effort may clarify design exchange standards

Two standard-setting committees are developing a reference-modeling technology to clarify the confusion among the different design interchange standards that, in some cases, compete. The committees will compare and evaluate the Electronic Design Interchange Format, the VHSIC Hardware Description Language and the Initial Graphics and Exchange Specification, and form a vehicle to communicate among these evolving standards. This clarification of the standards is a joint effort by the IEEE Computer Society's Design Automation Standards Subcommittee and the IGES Electrical Application Committee.—*R.G.*

VMEbus tracer to cover 32 bits

Small startup VMetro A/S (Oslo, Norway) will display a tracer board at Buscon West (Anaheim, CA) next month that will accommodate 32 bits. The board is completely passive, providing all the features of a logic state analyzer configured specifically for the VMEbus. Without signals driven on the bus by the board, the module saves up to 30 hrs/engineer-year in debugging system configurations based on VMEbus, according to the company. Both software and hardware errors can be traced. The module contains its own 68008 processor and accommodates 1 kbit of real-time trace for data, address and control signals on the bus.—*N.M.*

MAP 3.0 demo delayed to assure full functionality

The demonstration of MAP Version 3.0 scheduled for the November 1987 Autofact conference has been postponed until the second quarter of 1988. "Even though the 3.0 specification will be ready, the lack of quality testing procedures to assure operational devices will delay the presentation," says Tony Durham, a member of the General Motors staff at the GM Tech Center (Warren, MI) and MAP committee coordinator of the 3.0 demo. The MAP/TOP Users Group and the Corporation for Open Interface (COS) steering committee will determine where and when the official 3.0 demo will take place. Individual companies, however, may show some 3.0 functionality at Autofact '87.—*S.F.S.*

(continued on page 10)

(continued from page 9)

First 25-MHz single-board computer with zero wait state

Force Computers (Los Gatos, CA) will introduce the first zero-wait-state, 25-MHz single-board computer this month. The SBC uses 1 Mbyte of 25-ns static RAM and is targeted at real-time industrial and imbedded applications. According to Wayne Fischer, director of marketing, the board uses static RAM instead of cache memory because real-time applications can't withstand the worst-case performance penalty of repeated cache misses.—*K.M.*

U.S. industry must adopt CIM or join third-rate economy

Financial analysts at the Design and Manufacturing Automation Conference (Detroit, MI), organized by Prudential-Bache Securities (New York, NY), were told that the American industry could be saved only by further development of computer-integrated manufacturing and that nothing less than a total reorganization of business methods must be adopted. "If we fail to address key integration issues, we can anticipate the continuing loss of manufacturing capacity to overseas competitors, and we can expect to see the U.S. deteriorate into a second- or even third-rate manufacturing economy," warned George F. Meister, senior vice-president and general manager of McDonnell Douglas Manufacturing Industry Systems (St. Louis, MO). —*S.F.S.*

ASIC size and speed boosted by 1.5-micron technology

Soaring gate counts and sub-nanosecond gate delays are the result of a move by LSI Logic (Milpitas, CA) into 1.5-micron CMOS technology. LSI Logic's structured cells, a mixture of standard cells and customized megacells, have gone from a maximum of 12,000 to 60,000 gates and offer up to 36 kbits of RAM and 512 kbits of ROM. The company's structured arrays, a mixture of gate arrays and megacells, can now provide up to 38,000 gates. With gate speeds improved from 1.4 ns to 650 ps, these new ASICs provide clock rates approaching 100 MHz, putting them in the same league as ECL technology.—*R.G.*

TI issues a challenge on graphics benchmarks

Graphics technology is now feeling the need for a way to benchmark performance. A proposed set of benchmarks from Texas Instruments (Dallas, TX) will compare graphics chips for desktop CAD and office systems. A set of six benchmarks covers simple text that emulates the IBM Color Graphics Adapter format and many other capabilities. TI is generating a document along with an MS-DOS floppy disk containing display list and font data that will be available to graphics chip manufacturers.—*T.R.W.*

Sub 2-ns GaAs static RAMs expected

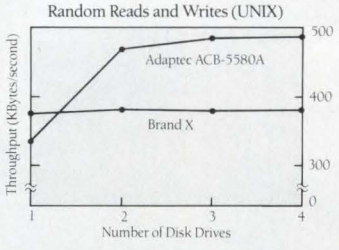
Ford Microelectronics (Colorado Springs, CO) and Vitesse (Camarillo, CA) plan to introduce the industry's fastest static RAMs in 1987. Ford expects to have a sub 2-ns, 1-kbit ECL compatible SRAM and Vitesse plans to introduce a 2- to 3-ns, 4-kbit device. Both will be about twice as fast as the fastest equivalent ECL parts.—*K.M.*

SCSI, the Small Computer Systems Interface, is far more powerful than the name implies.

To prove it, we asked an independent consultant to compare the throughput of our SCSI to SMD controller (with our MULTIBUS® host adapter) to one of the fastest MULTIBUS SMD controllers around. So he ran a series of UNIX™ benchmarks doing random reads and writes.

The outcome? With two drives connected, we beat them. With four drives and more than a gigabyte on line, we hung them out to dry.

How did we do it? Adaptec's multithreading, that's how. It let us execute tasks on each drive at the same time. Of course features like 1:1 Interleave and Disconnect/Reconnect didn't hurt.



What's more, our SCSI controllers bring the same kind of performance to ST506, ESDI or even 15MHz ESMD drives. So now, whatever your application, you can get a faster controller with the added flexibility of SCSI, for a lot less money.

For complete benchmark results and more about our line of high-performance SCSI controllers, call us at **408-432-8600**, ext. 400. Or write Adaptec, Marketing Department (TH), 580 Cottonwood Drive, Milpitas, California 95035-7403.

And start thinking big.

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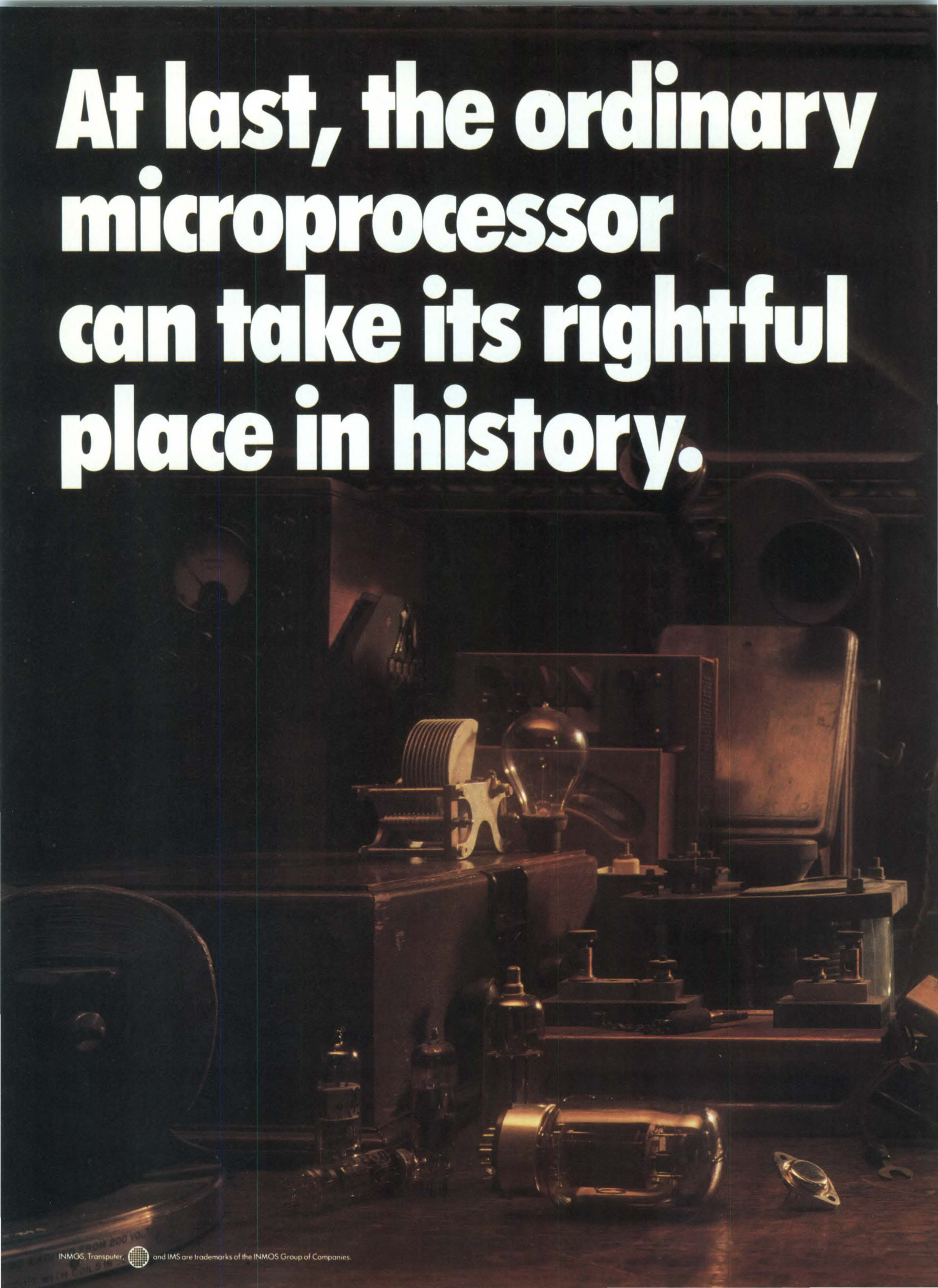
CIRCLE NO. 6

At last, the ordinary microprocessor can take its rightful place in history.



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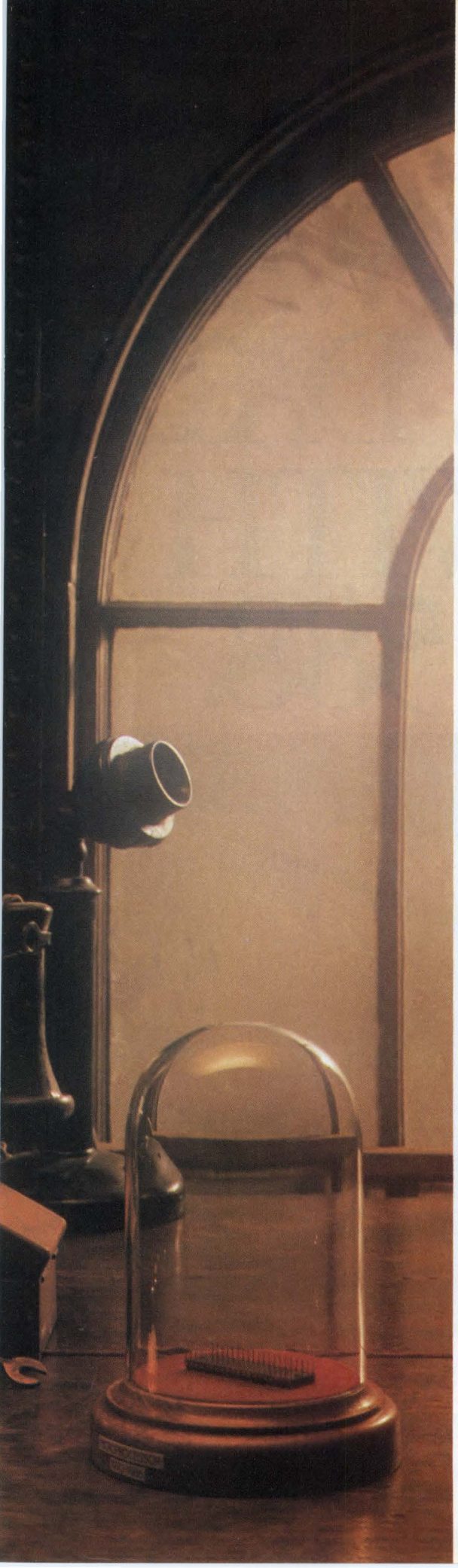

It had to happen—the conventional microprocessor has had its day. Relegated to the ranks of yesterday's devices by the new transputer family from INMOS. It's history in the making.

The IMS T414 transputer is a fast, easy-to-use VLSI component, integrating a 32-bit processor, four inter-transputer communication links, 2K bytes Static RAM, 32-bit memory interface and DRAM controller. All on a single CMOS chip—offering execution rates up to 10 MIPs.

While transputers excel in single-processor systems, their real power can be unleashed by connecting any number of transputers together via the high-speed serial links. Multi-transputer systems can deliver the performance you need today, and can be easily expanded in the future as your processing requirements increase.

And there's more. Programming multiprocessor systems has never been easier. The Transputer Development System (TDS) supports C, Fortran, Pascal and OCCAM, providing a complete software development environment, and is available for a number of popular hosts. Software developed on the TDS can be executed on one or more transputers, enabling cost-performance tradeoffs to be made.

INMOS transputers are available now and have already found their way into companies who are evaluating, prototyping and manufacturing transputer-based systems. Applications include supercomputers, DSP, graphics, robotics, AI, distributed control systems, PC's, engineering workstations and many others.

Write or phone for more information on the transputer family and start making history yourself.

TRANSPUTER PRODUCTS	
IMS T414	32 bit Transputer–2Kbyte —4 links
IMS T212	16 bit Transputer–2Kbyte —4 links
IMS M212	16 bit Disc Processor–1Kbyte—2 links
DEVELOPMENT TOOLS	
IMS D701-2	IBM PC—Transputer Development System.
IMS D600	VAX/VMS—Transputer Development System.
EVALUATION BOARDS	
IMS B002-2	Double Eurocard + IMS T414 + 2Mbyte DRAM + 2 x RS232.
IMS B003-1	Double Eurocard + 4 x IMS T414 + 4 x 256Kbyte DRAM.
IMS B004-2	IBM PC Format + IMS T414 + 2Mbyte DRAM.
IMS B006-2	Double Eurocard + 9 x IMS T212 + 128Kbyte SRAM.
IMS B007-1	Double Eurocard + IMS T414 + 0.5Mbyte DRAM + 0.5Mbyte Video RAM.
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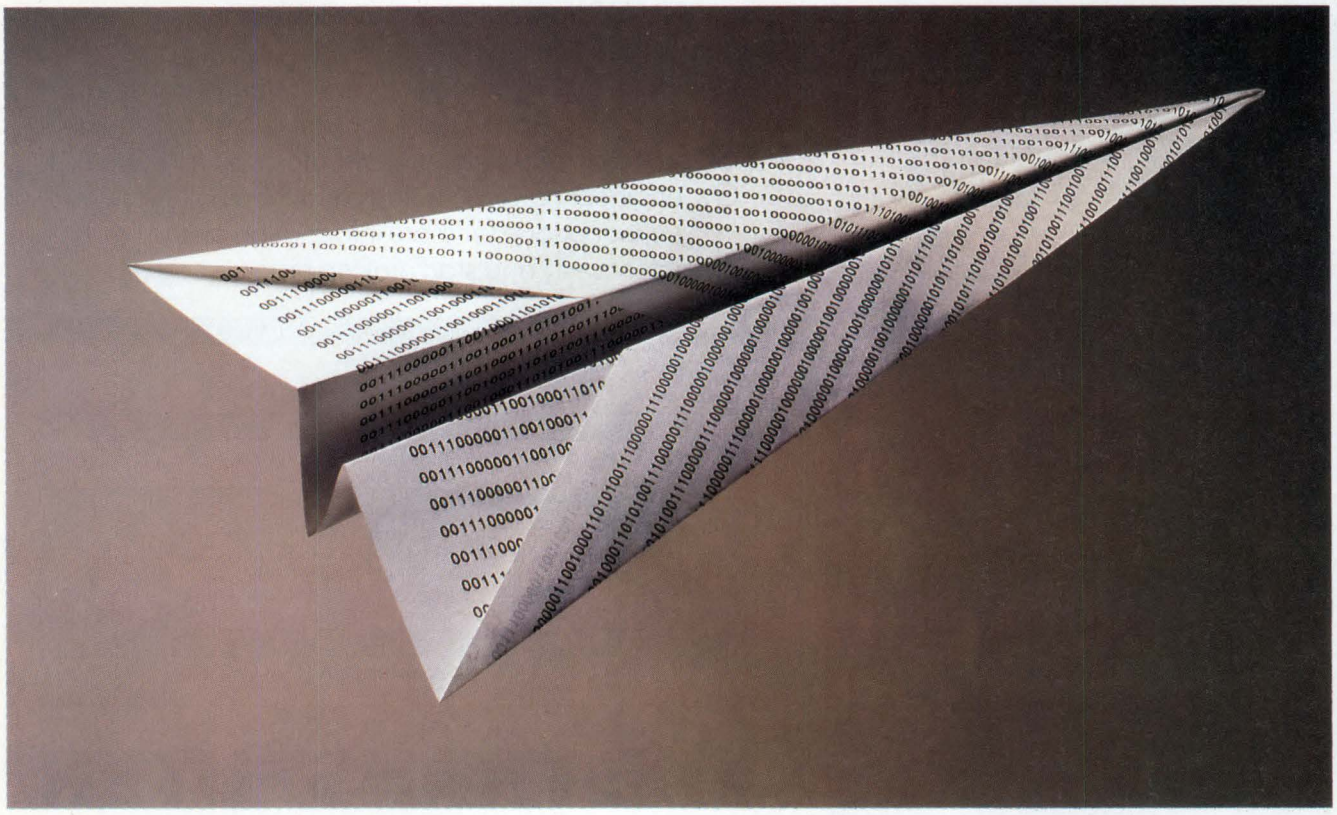
CIRCLE NO. 7

THERE ARE CHEAPER WAYS TO MOVE DATA THAN WITH INTEL'S 588.



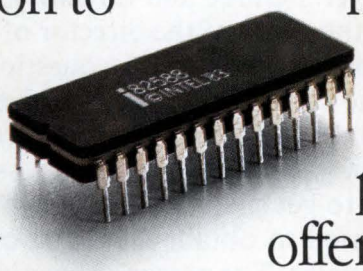
Now you can cut the cost of a PC LAN dramatically with our new 82588 LAN controller.

It's the most integrated networking solution in the 1-2 Mbps range.

And it's optimized to run with standard phone wiring.

Which means that low-cost PC LANs can finally get off the ground. And that's exciting. Especially when you consider that 10 million PCs out there could use an inexpensive way to connect.

That's a great reason to start designing now with the 82588. It's the LAN controller that reduces cost by cutting your board space in half. Saving you the bucks and bother of installing extra chips.



We put timing recovery, data encoding/decoding, collision detection and transmit clock generation all on a single chip. To lower your component count.

Which adds up to even more savings in areas like assembly, testing and reliability.

And we made sure that the 82588 supports emerging LAN standards like StarLAN. It also supports the IBM® PC Network. Plus many other specialized baseband and broadband LANs.

And because it snaps together with Intel's world standard 186 and 188 microprocessors, you eliminate TTL glue and save even more money. While speeding up your design.

To help your LAN products take off, we're offering an easy-to-use design kit. Included are two 82588s plus all the essential hardware, software and documentation needed to tie two PCs together. And all for just $65.

For information on how to get your kit, call Intel toll-free at (800) 548-4725 and ask for Lit. Dept. W-334.

Then see how high your profits can soar.

intel®

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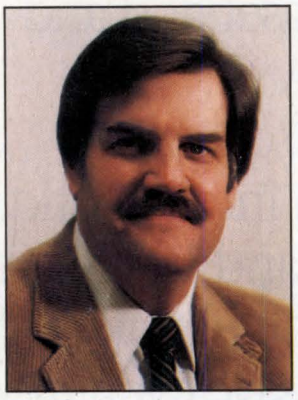

Is this any way to do business?

A major portion of the Feb. 15, 1987 issue of *Computer Design* will consist of a Buyer's Guide of single-board computers and a directory of vendors of VMEbus, Multibus I and II, Q-bus and STD Bus board-level products. As part of the effort to gather the mountains of information needed for the Buyer's Guide and directory, we first assembled a list of manufacturers. We then obtained the name of the director of marketing communications or the director of marketing to whom we would send a questionnaire, mailed the questionnaire, and followed up with phone calls if we didn't receive a completed questionnaire after a couple of weeks. We didn't foresee any major problems. After all, we were offering a free listing in *Computer Design*. With business the way it is today, who wouldn't jump at the opportunity to get some free exposure? Were we in for a surprise.

Our troubles started when we tried to obtain the name of the appropriate person to whom we should send the questionnaire. The person answering the telephone often didn't know who the director of marketing was or refused to give out a name. In a couple of cases, we got routed through the personnel department. And a few times, the female editor making the calls was treated to a variety of condescending comments including "honey" and "sweetheart." Despite these hurdles, we got most of the names we needed.

The cover letter we sent along with the questionnaire clearly detailed the editorial nature of the questionnaire and the value of the listing to our readers. You would think that the responses would come flooding in. Again, were we in for a surprise.

With the questionnaires only trickling in, we started the follow-up calls. The responses here were even more amazing than the responses to our initial phone contacts. Some didn't even bother to read the first paragraph of the cover letter. Some didn't know, or couldn't remember, if they had received the questionnaire. Some didn't "see that there was anything in it" for them. And some just didn't "care to participate."

But there were some bright spots. And they demonstrate what running a good business is all about. Quite a few individuals jumped at the opportunity to get a free listing for their companies. They took great pains to get our questionnaire to the right person and to complete it accurately and carefully and to send backup materials. One in particular stood out.

A distributor had inadvertently been included in the mailing, but he completed the questionnaire for all of the manufacturers he represented. One of those manufacturers was the one who didn't "see that there was anything in it" for his company.

With the electronics/computer industry facing hard times, we all tend to look for explanations in the tax laws, trade restrictions, foreign competition or unproductive workers. But maybe we're having a hard time surviving in a tough competitive world because there are just too many who've forgotten how to do business.

John C. Miklosz
Executive Editor

HOW FAR DOES YOUR DRIVE SUPPLIER GO TO GIVE YOU AN EDGE?

9″ Drives: 800 MB, or 520 MB sized for today's smaller superminis.

NEC goes all the way to 800 MB.

NEC continues to expand the edges of disk drive technology farther and farther. So your computer systems can be more competitive.

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CIRCLE NO. 9

NEC keeps going for more.

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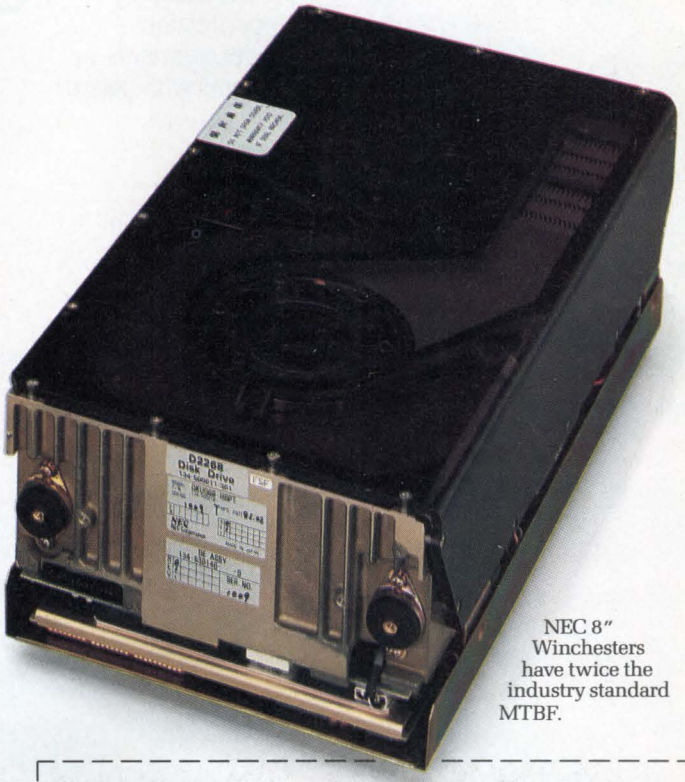

NEC 8″ Winchesters have twice the industry standard MTBF.

☐ Please send me more information on NEC disk drives.

☐ Please have a salesperson call.

Name _____

Title _____

Company _____

Address _____

City _____

State _____ Zip _____

Tel ( ) _____

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CIRCLE NO. 10

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ON-CHIP VIRTUAL CACHE CONTROL	YES	NO
AVAILABLE FOR 16-BIT 68010 AS WELL AS 32-BIT 68020	YES	NO
VIRTUAL MEMORY: PAGES, SEGMENTS, PAGED SEGMENTS	ALL THREE	PAGES ONLY
MEMORY MANAGEMENT: CACHE, LOCAL, MAIN MEMORY	ALL THREE	MAIN MEMORY ONLY
REGION SUPPORT FOR SHARING LIBRARIES	YES	NO
WAIT STATES	NONE ON CACHE HITS	ON EVERY ACCESS
AVAILABILITY	NOW	?

Yes, I'd like more information on BMAC.

☐ Please have a salesman swing by with a BMAC sample pack.

☐ Save yourselves the trip for now. Just send me some product info. I'm primarily interested in:

☐ 68905 for the 68010 ☐ 68906 for the 68020

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Name_____

Position_____

Company_____

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Phone_____

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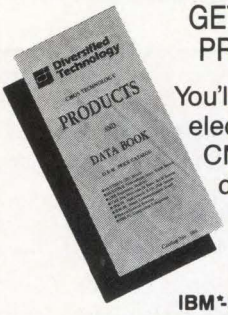

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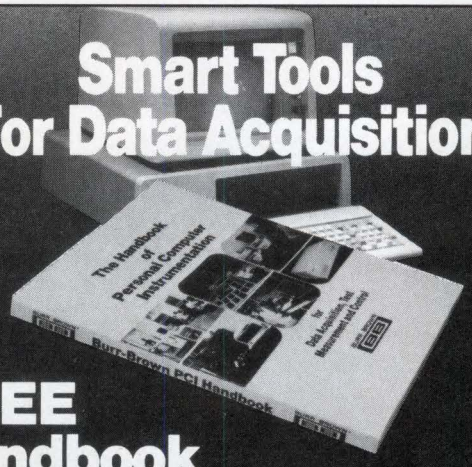

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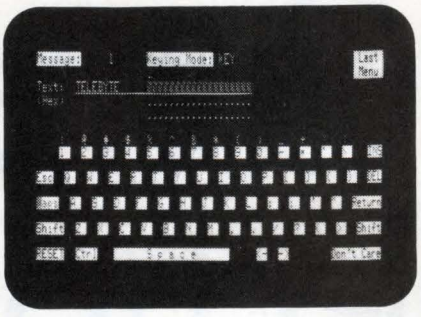

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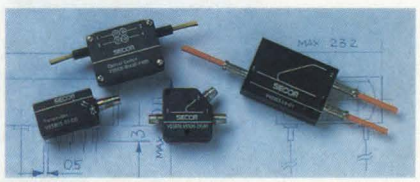


Left to right: 200 MBaud transmitter, fiber optic switch, WDM, T-coupler with pigtail.

SIECOR

CIRCLE NO. 14

LETTERS

The debate goes on

Your July editorial, "Must We Shut Up or Quit?," fails to address the crucial issue in the "Star Wars" ethical debates or in any other Luddite argument. The historical fact is that every estimation of the real impact of any idea or invention has been wrong. The critics and the supporters simply lack real information and invariably project their wishes and fears into their prediction of future harm or benefit. Therefore, it is a waste of time and energy to debate any idea or invention that can't be put to immediate tests to determine the real side effects. I believe that small-scale testing of bad ideas would prevent the allocation of resources in undesirable projects. Putting each idea to a test would prevent managers or other decision makers from killing ideas for political or personal reasons.

The initial focus of the SDI program was on death rays and super rockets. A more mature examination of the tasks in SDI acknowledges that sensing and timely action is important but is totally dependent on knowing when to act and how to respond to incremental threats.

I believe that many of the operational problems would be resolved in SDI if research were focused on a top-level control facility that would predict the next move of all actors in each region by analysis and reevaluation of past patterns. It is more useful to predict a launch than to be ready for any launch at any time from any place. The pattern-recognition ability of some existing computers is adequate to form a knowledge sieve of behavior patterns for each actor. This approach would allow low-level information gathered under uncertain conditions to be evaluated and assigned a probability weight.

It is correct and proper to discuss ethical values when there is factual evidence about the effects and costs of projects. However, idle speculation and endless debate are the signs of a mob mentality. Who will benefit by this diversion of time and energy?

Dannie Davis
Scientist
Asteroid Mining
Elmore, Alabama

A question of origin

In "Hypercube Architecture Leads the Way for Commercial Supercomputers in Scientific Applications" (May 1, pp 28-30), Nicolas Mokhoff stated that "This architecture, known as the hypercube or binary n-cube, was conceived at the California Institute of Technology several years ago." This is incorrect.

The first reference in computer science literature to the binary n-cube as an interconnection network for multiple computing elements was in the paper "Programming and Design Considerations of a Highly Parallel Computer," by J.S. Squire and S.M. Palais, which appeared in the AFIPS Conference Proceedings, Vol 23, 1963 Spring Joint Computer Conference. The next reference was in the paper, "A Large Scale, Homogeneous, Fully Distributed Parallel Machine, I," by Herbert Sullivan and me, published in the Proceedings of the 4th Annual Symposium on Computer Architecture, March 1977.

The latter paper gives an extensive analysis of various interconnection schemes. We concluded that the Boolean or binary n-cube network has advantageous behavior over many performance parameters, such as full access, delay time, mean queue length for packets, number of connections and so forth. In fact, Charles Seitz of Caltech, who is quoted in the article, not only referenced our paper in "The Cosmic Cube," Communications of the ACM, January 1985, but stated that Caltech's hardware ideas were very much influenced by our paper and that Caltech even calls the Cosmic Cube a "homogeneous machine" from our usage of the term.

Since 1977, however, we have learned that a clever interconnection scheme itself is not sufficient to achieve high speed with multiple computing elements. We are not using an n-cube network in our current development of the Chopp supercomputer because it does better simulation results than the latest Cray machines on the Lawrence Livermore Laboratory benchmark programs.

T.R. Bashkow
Professor, Dept of Computer Science
Columbia University
New York, NY

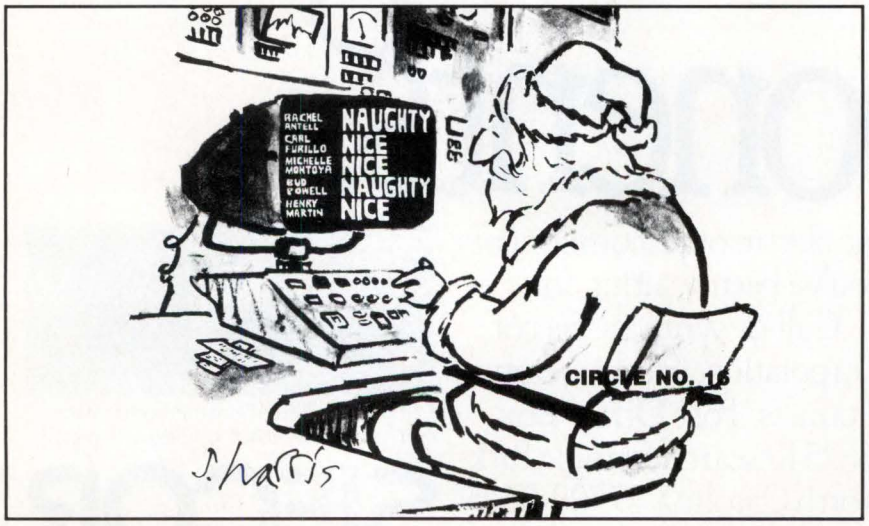
Setting the record straight

Thank you for your Up Front report about Siemens' launch of Multibus II boards as first European manufacturer (May 1, p 9). It contains two mistakes, however.

The last sentence "Siemens now sells Multibus II boards as well as VMEbus boards to the European market" is incorrect. Siemens sells neither Multibus I nor VMEbus boards, but sells the AMSbus, which is a European variation of Multibus I.

R. Gopfert
Marketing Microcomputer Systems
Siemens AG
Munich, Germany

The information included in that Up Front item was based on an English translation of a statement released in Germany by Siemens. We contacted Siemens public relations representatives in New Jersey for verification of the statements. They provided additional information after contacting personnel in their European facilities. We regret that the wording of the item conveys an incorrect meaning.—Ed.



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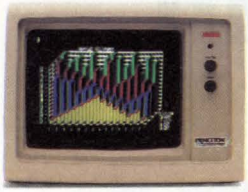
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CIRCLE NO. 15

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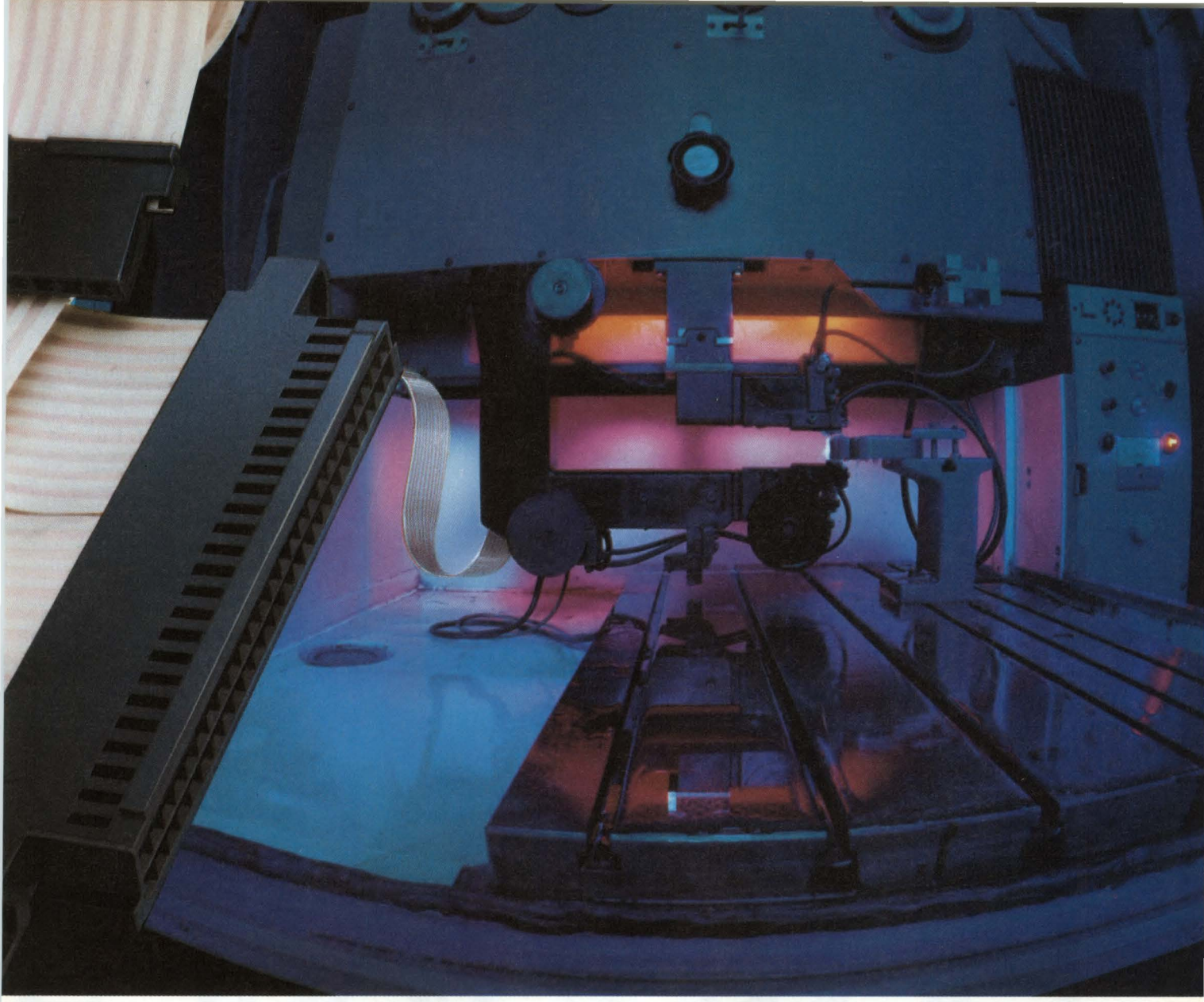

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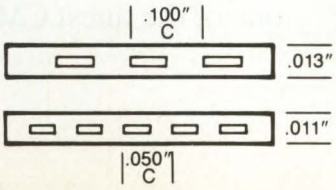
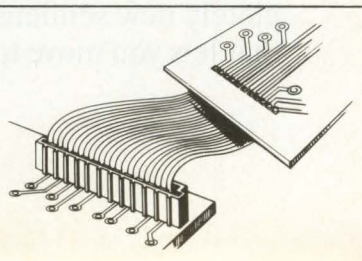
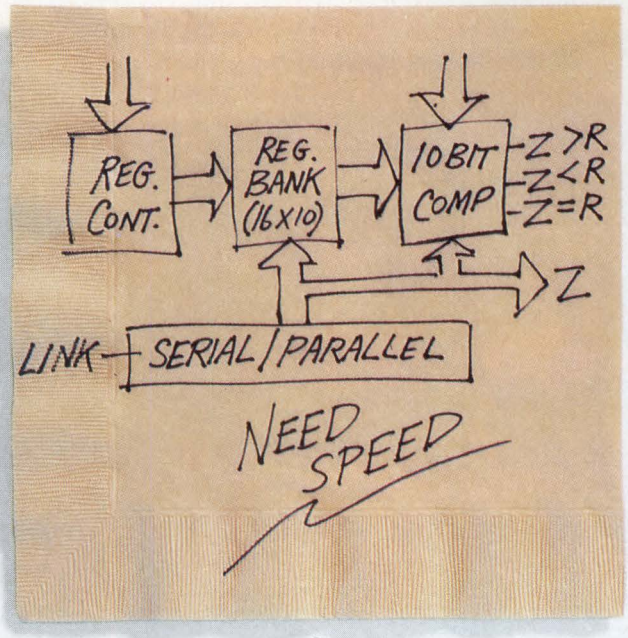
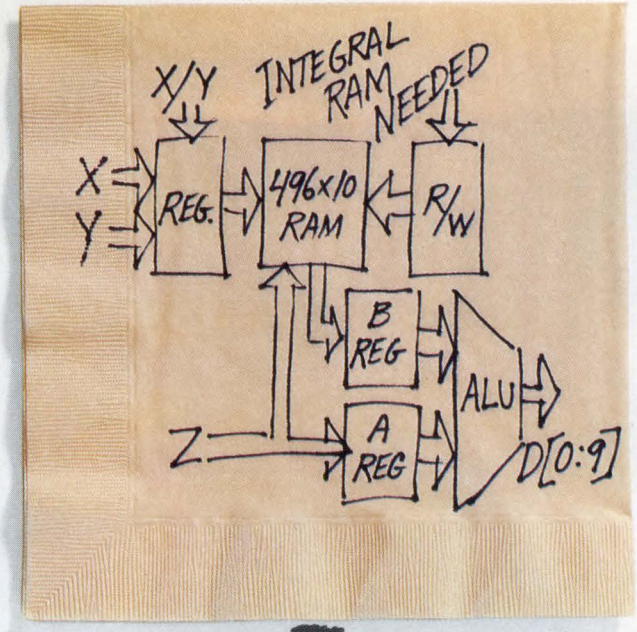


AMP Trio-Mate connectors for flat flex cable .004" to .015" thick. Staggered contacts reduce insertion force, wiping action assures reliable contact. Horizontal and vertical styles, 2-22 positions.







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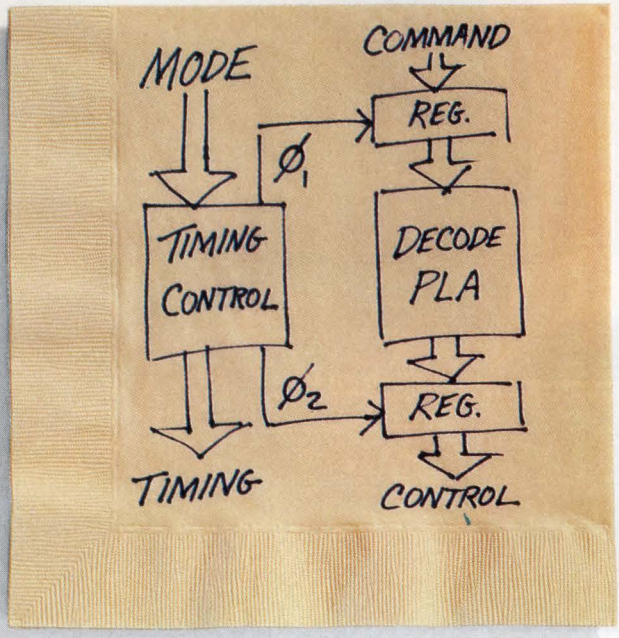

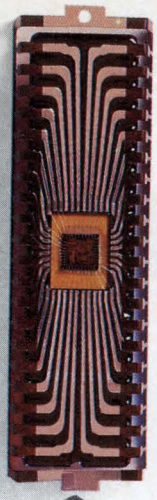

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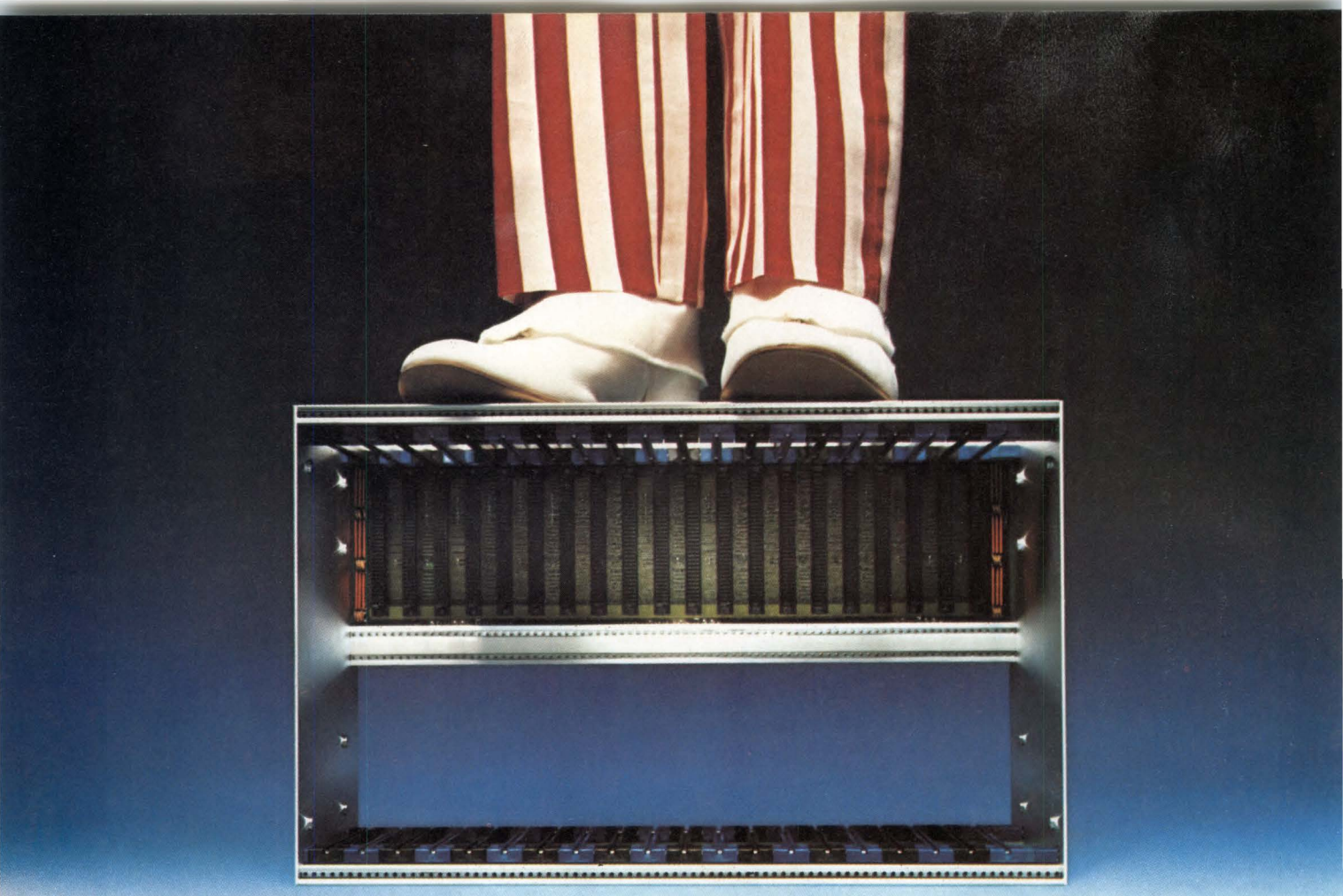
CIRCLE NO. 17



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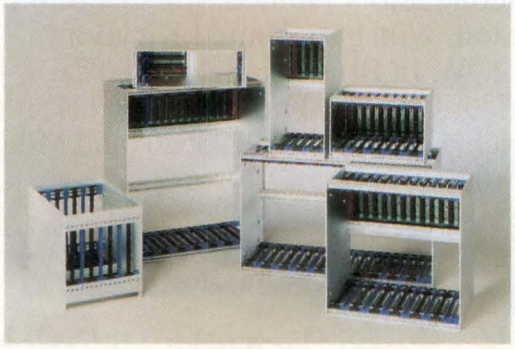

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CIRCLE NO. 18

Integrated MMU and data cache supports 30-MHz zero-wait-state accesses

With 32-bit microprocessor speeds approaching 30 MHz, system designers are finding it increasingly difficult to design cost-effective memory subsystems that can keep pace. To obtain zero-wait-state performance at 20 MHz, designers must use the fastest, most expensive dynamic RAM (60 ns) available. At 25 MHz, designers must turn to static RAM cache memory. And at 30 MHz, even caches can't keep up.

To provide designers with cost-effective memory subsystems for 30-MHz performance, AT&T (Holmdel, NJ) has combined a memory management unit (MMU) and a 4-kbyte, two-way set-associative, physical data cache on the same chip. Known as the WE32201, the MMU/cache supports the 32-bit WE32200 microprocessor with zero-wait-state cache accesses at speeds as high as 30 MHz. (AT&T plans to provide a 30-MHz version of the 32200, along with a 30-MHz coprocessor, a 32-bit DMA controller, and a DRAM controller within the next year.) The data cache offers an 85 percent hit rate, and by ganging four MMUs, a designer can increase the hit rate to as much as 95 percent. Also on-chip is a fully associative, 64-entry descriptor cache that provides a 99.8 percent hit rate.

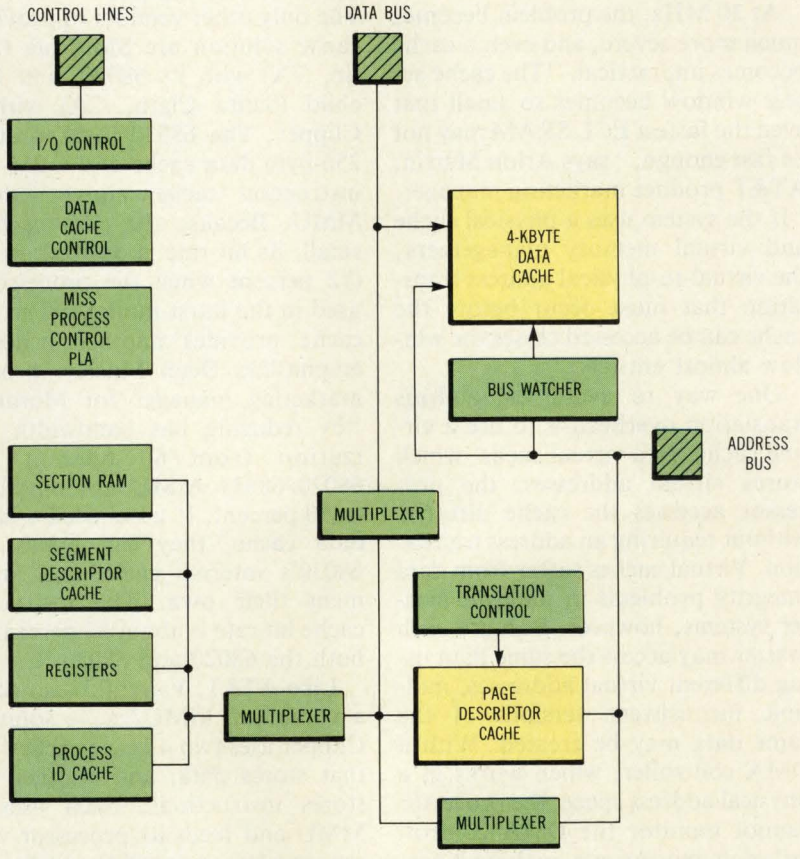
Though no vendor is currently shipping production microprocessors that are faster than 20 MHz, system designers are already grappling with the problem of designing cost-effective memory subsystems. Although 60-ns DRAM can provide zero-wait-state operation at 20 MHz, it makes the memory boards expensive. "To keep their costs down," explains Tom Powell, product marketing manager at Synergy (Encinitas, CA), "system vendors are using slower memory and adding a wait state. With 100-ns memory, for example, a processor can run at 20 MHz with one wait state. The wait state degrades performance by about 13 percent, but cuts memory costs by 75 percent—60-ns DRAM costs about $2,100/Mbyte, versus $570/Mbyte for 100-ns DRAM."

Ken Marrin
Senior Editor

To cache or not to cache

A cache can be used instead of wait states to reduce memory cost. But at only 20 MHz, there's not much improvement in overall memory access speed. "The cache runs at zero wait states for hits," explains Powell, "but on misses, the hit/miss calculation costs an extra wait state. The improvement the cache offers depends on the code that's being executed, but generally speaking, the improvement isn't significant."

At 20 MHz, the cache doesn't provide much improvement in cost either. Typically, a cache reduces system cost because relatively slow main memory can be used. Instead of using one-wait-state main memory, for example, the designer might



Incorporating a 4-kbyte, two-way set-associative physical data cache with an 85 percent hit rate, AT&T's WE32201 MMU supports zero-wait-state cache accesses at speeds as high as 30 MHz. The MMU also includes a fully associative, 64-entry descriptor cache, which provides a 99.8 percent hit rate. Four MMUs can be ganged together for a fourfold increase in the size of the data and descriptor caches.

be able to reduce cost and maintain the same performance by using two-wait-state memory and a small zero-wait-state cache. At 20 MHz, however, two-wait-state memory costs about the same as one-wait-state memory, so using a cache provides no cost savings.

But the picture changes at 25 MHz. To run at zero wait state, a processor would require 30- to 35-ns DRAM, which doesn't exist. Even at one wait state, the system must have 60-ns memory. Using a fast CMOS SRAM cache lets the designer use considerably less expensive two-wait-state DRAM. The SRAM cache is expensive, but because the two-wait-state main memory is less expensive than the one-wait-state main memory, the total cost of the cache-based system will be less.

At 30 MHz, the problem becomes much more severe, and even a cache becomes impractical. "The cache access window becomes so small that even the fastest ECL SRAM may not be fast enough," says Arlon Martin, AT&T product marketing manager. "If the system uses a physical cache and virtual memory management, the virtual-to-physical address translation that must occur before the cache can be accessed closes the window almost entirely."

One way to avoid the address translation overhead is to use a virtual cache. In a virtual cache, which stores virtual addresses, the processor accesses the cache directly, without requiring an address translation. Virtual caches suffer from data integrity problems in multiple-master systems, however. Because each master may access the same data using different virtual addresses, multiple inconsistent versions of the same data may be created. With a DMA controller, which works in a physical address space, the processor cannot monitor the DMA controller's data movements, making it possible for the data stored in the cache to disagree with the corresponding data stored in main memory.

AT&T has eliminated the need to use a virtual cache, or even to design a separate cache, by integrating a cache with the MMU. Because the cache is included with the MMU, the delay associated with accessing an external cache is eliminated. The faster access time lets AT&T provide a 4-kbyte, two-way set-associative physical cache that supports zero-wait-state accesses at 30 MHz. "The hit rate is about 85 to 90 percent," claims Martin, "and is equivalent to an 8-kbyte direct-mapped cache."

If a larger cache is needed, up to four MMUs can be ganged with virtually no glue logic. The MMUs can store user data, user instructions, kernel data, or kernel instructions. In addition to a fourfold increase in the data cache size, the ganged MMUs quadruple the size of the MMU's descriptor cache.

Other cache strategies

The only other vendors to provide a cache solution are Motorola (Austin, TX) with its 68030, and Fairchild (Santa Clara, CA) with its Clipper. The 68030 incorporates a 256-byte data cache and a 256-byte instruction cache, along with an MMU. Because the data cache is small, its hit rate is only 60 percent (72 percent when the processor is used in the burst mode). "The data cache provides another benefit," emphasizes Dean Mosley, product marketing manager for Motorola, "by reducing bus bandwidth utilization from 60 percent [for 68020/68851 MMU combinations] to 50 percent. If users need a larger data cache, they can bypass the 68030's internal cache and implement their own. The instruction cache hit rate is about 82 percent for both the 68020 and 68030."

Like AT&T, Fairchild also offers a combined MMU/cache solution. Clipper uses two 4-kbyte caches: one that stores data, and another that stores instructions. Each uses an MMU and feeds its processor via a separate bus. According to Clipper's product manager, Gary Baum, the two-way set-associative data cache provides a 90 percent hit rate, while the instruction cache provides a 96 percent hit rate.

Unlike the AT&T MMU/cache, however, Clipper's cache looks more like a hierarchical cache, providing zero-wait-state accesses only within 16-byte lines. When the processor accesses the cache, an entire 16-byte line is loaded into a high-speed buffer. The initial cache access requires 120 ns, but as long as the processor accesses data within that 16-byte line, it can do so at 30 ns, or zero wait states. AT&T's MMU/data cache, by contrast, runs at zero wait states for accesses anywhere within the cache.

Expanded MMU capability

Along with a data cache, AT&T's 32201 will provide one of the most powerful MMUs on the market, particularly in multiuser applications. Most notable is a 64-entry, fully associative descriptor cache, which provides a 99.8 percent hit rate. High hit rates are even more critical in descriptor caches than in data or instruction caches, as further processing can't continue until multiple descriptors are fetched from main memory and loaded into the cache. If the MMU includes hardware miss processing (the MMU, not the CPU, fetches the descriptors), the delay may only be 10 to 30 clock cycles. If the MMU relies on software miss processing, however, a trap to the operating system will be required, delaying further processing for several hundred clock cycles.

Like the WE32201, Motorola's 68851 MMU (which supports the 68020) also provides a 64-entry fully associative cache and hardware miss processing. And Fairchild has the largest descriptor caches of all, providing 128 entries for both instructions and data. As a two-way set-associative cache, it provides a 98 to 99 percent hit rate.

The 68030's MMU, which is included on-chip, takes a step back from the 68851. The cache is still fully associative, but it contains only 22 descriptors. For small numbers of users and small programs, where reducing the number of descriptors doesn't have a major impact on the 68030's hit rate, Mosley claims a 98.9 percent hit rate. **CD**

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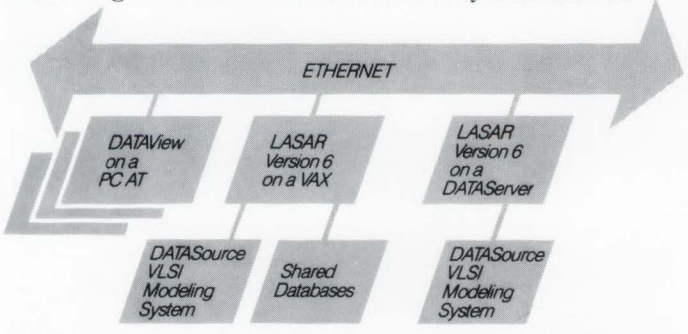

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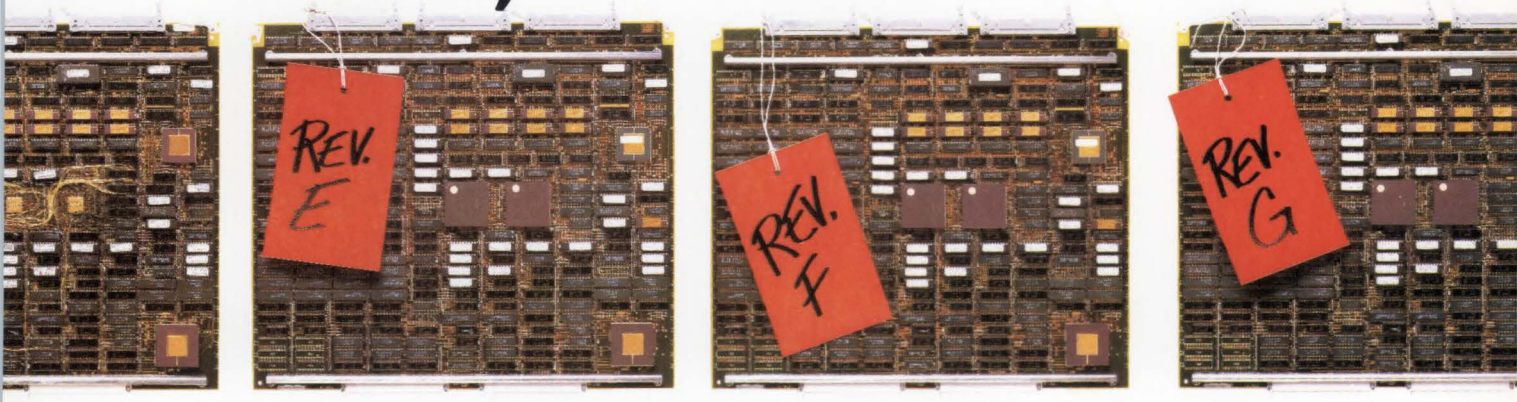

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Microprogram sequencers depart from classic architectures

For those applications where speed is the name of the game, single-chip microprocessors rarely make the grade, and in those cases usually a building block approach must be taken. The heart of a building block system is a sequencer that generates control signals via addresses to the microprogram memory for the various blocks or components that make up the system. Innovative sequencers have recently come to the forefront to control the new building block families that are also emerging.

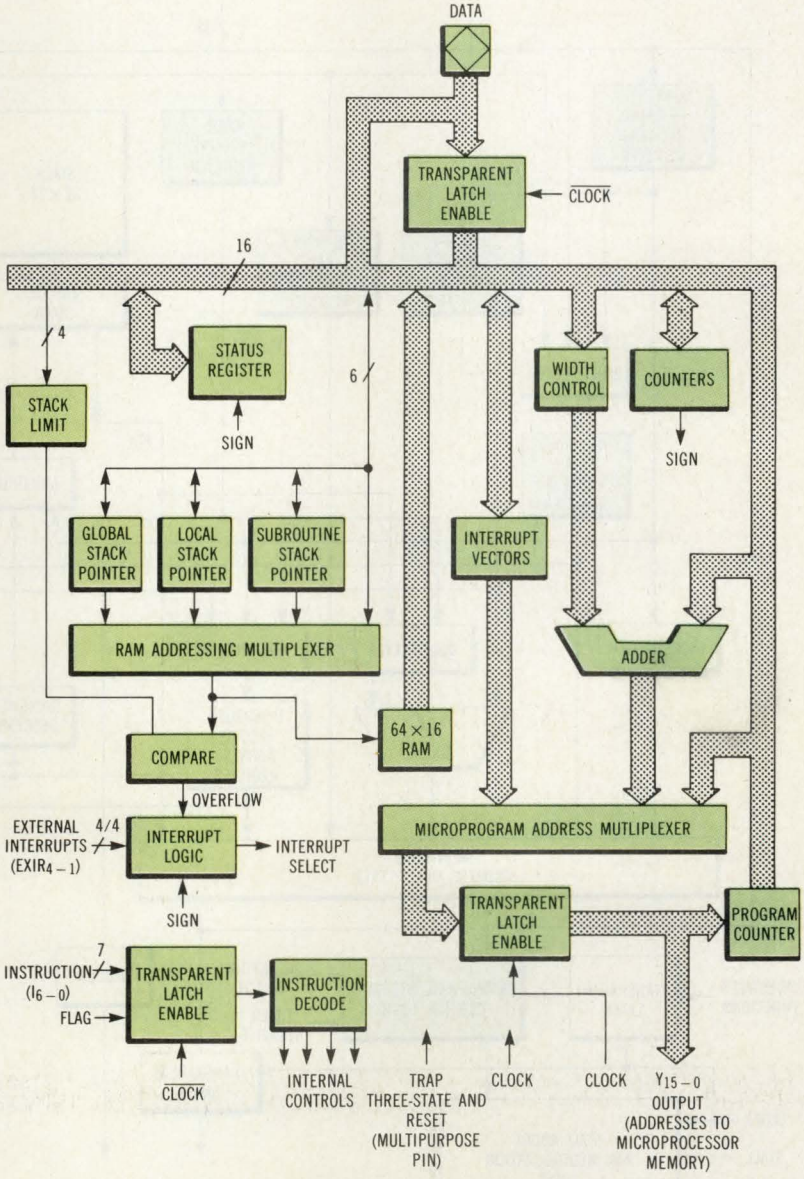
Analog Devices (Norwood, MA) and Weitek (Sunnyvale, CA) have made significant architectural departures from the classic 2910 sequencer developed by Advanced Micro Devices (Sunnyvale, CA). These sequencers incorporate an on-chip interrupt capability, larger and more flexible stacks and pipelining of address, data and instruction buses. In addition, the new part from Weitek features 32-bit output address, data and instruction buses along with a large pin count.

A one-chip solution

Distinguishing the new generation of sequencers from the old, David Fair, strategic marketing specialist at Analog Devices, says, "What I see Analog Devices and Weitek doing for the first time is really giving you a one-chip solution to the task of microprogram sequencing. That is the point of departure." The two most salient points of that departure, according to Fair, are interrupt capability and stack extension.

One perceived shortcoming of the 2910 is the shallowness of its stack—it's only nine words deep, which limits the nesting of subroutines. AMD has increased the depth of the stack in subsequent parts. Consequently, Analog Devices and Weitek have increased the depth of the stack in their new parts. And Analog Devices has increased the flexibility of the stack as well.

The new sequencer from Analog Devices—the ADSP-1401—has an internal RAM that serves as the stack. This RAM is 64 words deep × 16 bits wide, and any of the 64 words in the RAM may be output onto the address port. There are four distinct sources of access to the RAM: the subroutine stack pointer, the global and local register stack pointers, and data port bits 0

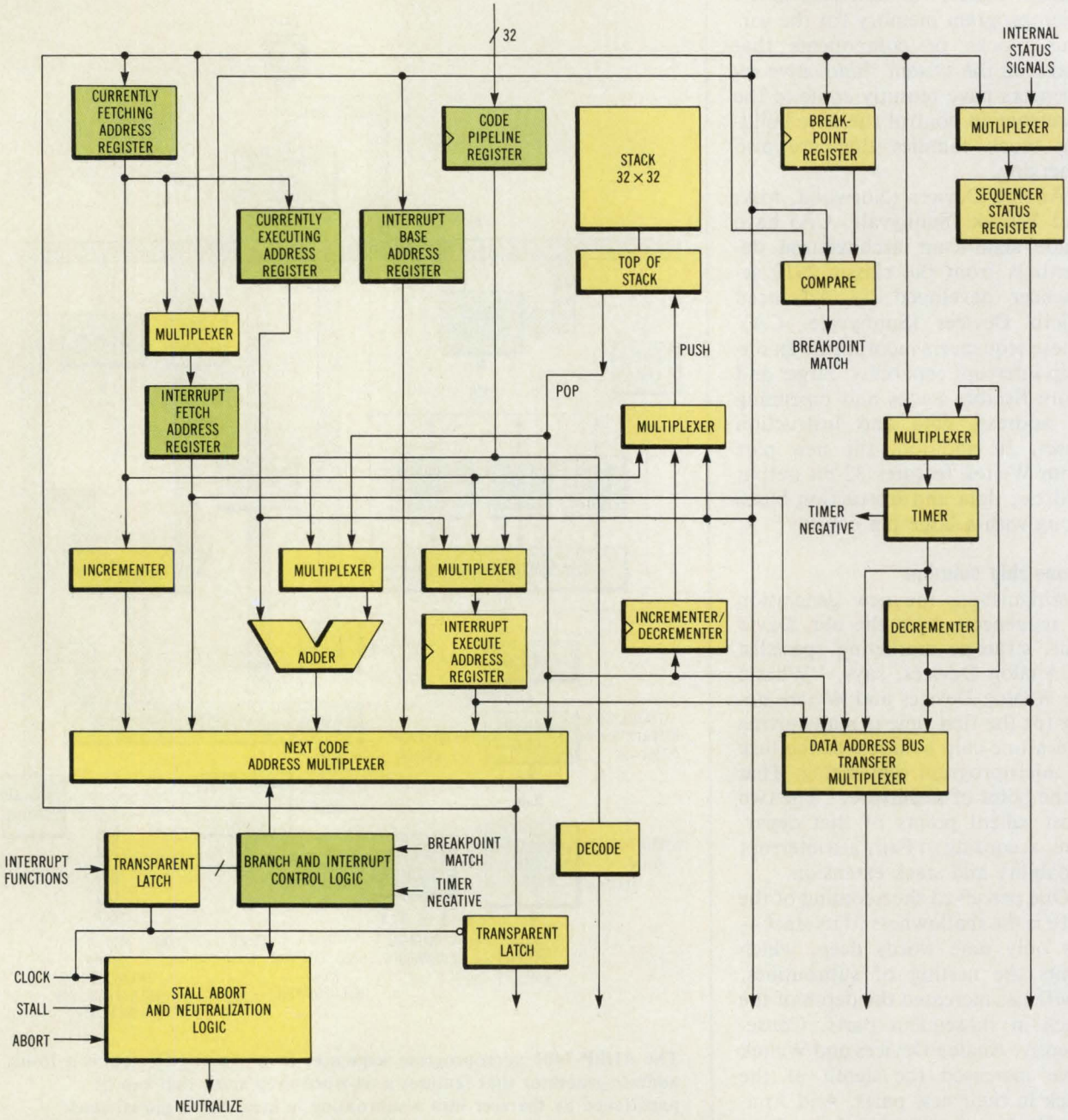


The ADSP-1401 microprogram sequencer from Analog Devices is a 16-bit address generator that features a 64-word-deep stack that can be partitioned by the user into a subroutine, a local and a global stack pointer. It features interrupt capability and transparent I/O latches that operate in a complementary fashion so that fetched addresses, even in a branch situation, are always correct.

Steven L. Martin
Contributing Editor

CIRCLE NO. 19

through 5 for indirect addressing. The subroutine stack and the register stack are implemented on the RAM. The subroutine stack is accessed via the subroutine stack pointer (SSP), while the register stack is accessed via two pointers, the global stack pointer (GSP) and the local stack pointer (LSP). The subroutine stack is used for storing return addresses, counters and status bits for return purposes. The register stack is available as an additional convenience. The GSP is used for addressing of common registers between different routines, while the LSP is used for local purposes. The subroutine stack and the register stack are separated by a stack limit register (SLR), which is preloaded by the user. This lets the user divide the RAM between the two types of stacks. The SLR then warns the user of an impending overflow.



The WTL7136 from Weitek is a 32-bit address generator (sequencer) that can be used with main memory as well as microcode control stores. It also features four external and seven internal interrupts as well as a split pipeline.

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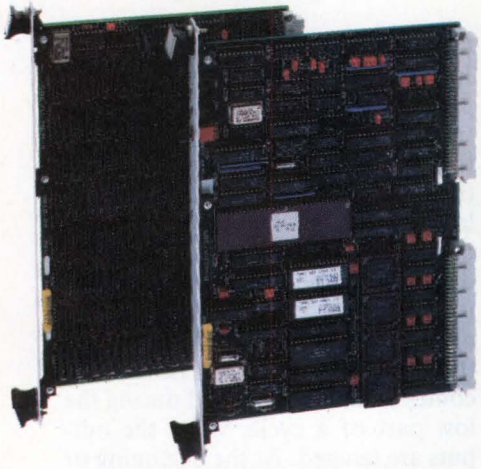

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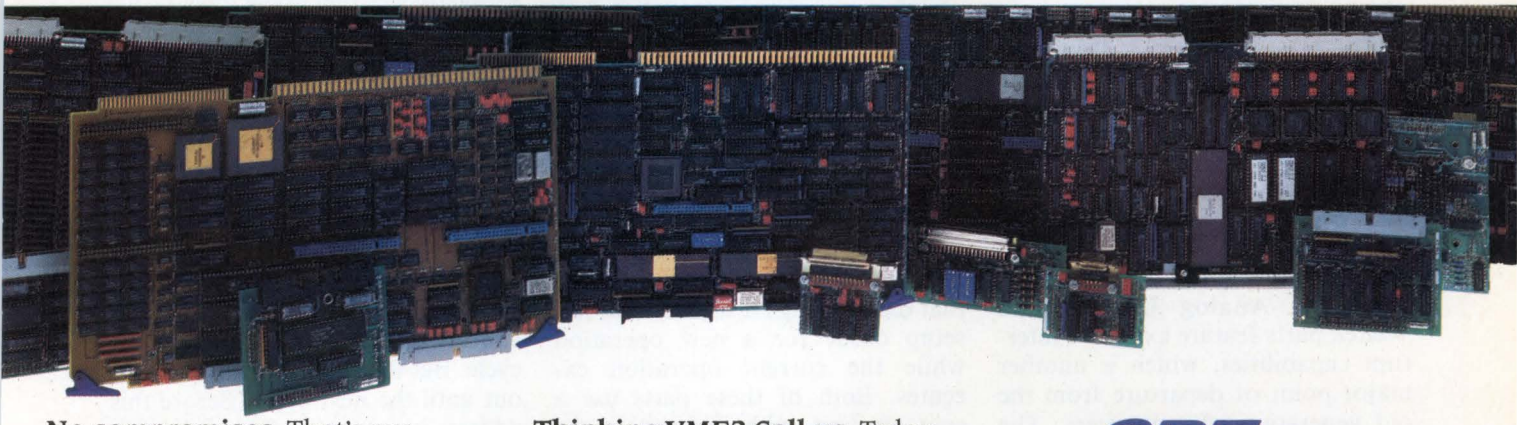

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CIRCLE NO. 20

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The WTL7136 sequencer from Weitek contains a traditional stack whose depth has been increased to 33 words. At 32 bits, however, its width is greater than any traditional stack. The sequencer has a single subroutine stack pointer, which is adequate for most applications, according to Leon Torban, Weitek's product marketing manager for integer products.

Analog Devices' Fair compares his company's stack with those of Weitek and other companies: "The word is out that you need more than what the 2910 had to offer. Sixty-four words for a stack is a lot. That's important because it means that you can do some very sophisticated sequencing without having to page the stack." Commenting on the added features of the ADSP-1401 stack, Fair says, "Other companies give you a traditional stack with a single point of access—pushes and pops. What is helpful is a frame pointer that lets you point at some position on the stack, or save specific things in a separate place without pushing or popping."

The local and global register stacks are also valuable, Fair says. "The global stack pointer lets you save the addresses of several routines that could be used in many subroutines, and is accessible to any subroutine. The local stack pointer is used within a particular subroutine. We've let users set what we call a stack limit register, and at their discretion, they can divide the RAM in any way they choose."

Interrupt capabilities

Both the Analog Devices and Weitek parts feature extensive interrupt capabilities, which is another major point of departure from the old generation of sequencers. The WTL7136 generates interrupts for four external, user-defined conditions and seven internal conditions. Interrupts may be individually masked or group masked, a characteristic shared with the part from Analog Devices. Masking or unmasking is easily done via the status register in both devices. Because Weitek intends to tightly couple its sequencer with other members of its family, the external interrupts are targeted at specific functions.

By contrast, Analog Devices' interrupts are general. The ADSP-1401 offers eight external interrupts but only two internal ones. The external interrupts may be used for any purpose, but since only four external interrupt lines are available, they must be multiplexed in two groups of four onto the sequencer. Interrupts IR8-5 are latched on the first half cycle (HI), and interrupts IR4-1 are latched on the second half of the cycle (LO). An external multiplexer is required if a user wants to use eight external interrupts.

The ADSP-1401 provides only two interrupts for internal exception conditions—one for the stack limit register and overflow and one for stack overflow. It contains an on-chip interrupt vector file, whereas the Weitek WTL7136 services interrupts by determining an interrupt vector address from an interrupt base address and an offset.

"The unique thing about the interrupts is that the whole file is on the chip itself," Fair says. "When the interrupt condition occurs, that address is immediately available to access microcode memory. The 7136 has an interrupt vector, but it's a pointer to an interrupt table in memory, which adds another cycle to interrupt servicing."

Both Analog Devices' and Weitek's parts are pipelined, but differences between the two are worth noting. Pipelining usually means a process involving data flow and timing of that data through a register that lets setup occur for a new operation while the current operation executes. Both of these parts use a split pipeline, with registers at the input and registers at the output. Processing occurs between these registers, so that what goes in is not what comes out. The input is data from the microcode memory; the output is an address to the microcode memory. For Analog Devices, the input registers are for the input data bus and instruction port, for Weitek, they are for the 32-bit microcode bus, an input bus that contains the 32-bit instruction word. In both cases, this allows the fetching of an instruction and its setup at the inputs to the device while an instruction is currently executing.

Areas of difference

In Analog Devices' look-ahead pipeline register the sequencer has transparent latches on the registers that let data flow through on the active part of the cycle and be latched on the inactive part of the cycle. For the instruction and the data port, the latches are active (transparent) low; for the address output port the latches are active (transparent) high. An instruction comes in and is processed during the low part of a cycle, while the outputs are latched. At the beginning of the new cycle (clock high), the output register becomes transparent, and the newly computed address comes out valid and is latched during the second half of the cycle. Then, during the second half of the cycle, with the address output valid and latched, the next instruction flows in and computes. This next instruction is computed on the basis of microcode that is fed back to the sequencer, based upon the previous address. Because the new address is computed after the old address has been used to access microcode memory, and returns the next real instruction to the sequencer, an address never has to be cancelled.

The operation of Weitek's pipeline differs significantly. An instruction (code) comes in on the high or first part of the cycle, and the new address is computed during the first cycle. But the address does not come out until the next cycle. Before this address is output, however, the new instruction begins to compute. Since it does this before the previous address is output and before code is returned from the microcode memory, it may be computing the wrong address if branching is involved. It assumes that any operation is sequential. So a neutralization instruction is required to

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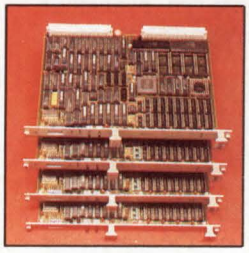

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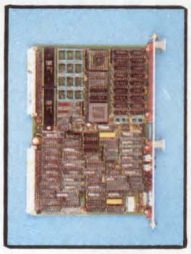

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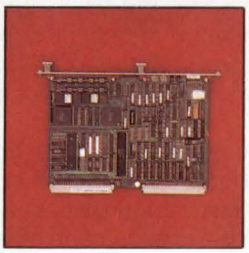
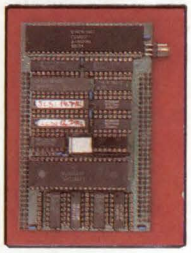


CPU-2PB

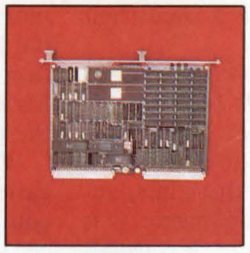


PIGGY BACK BOARDS

68020
@ 12.5 MHz,
16.5 MHz, or
20 MHz,
DRAM ¼ Mb,
1 Mb, or 4 Mb

CPU-4RT

STAND ALONE HOST



CPU-1

CPU-3

	STAND ALONE HOST		REAL-TIME MASTER/SLAVE			
	CPU-1	CPU-3	CPU-2RT	CPU-2SC	CPU-2PB	CPU-4RT
MICROPROCESSOR	68000/68010	68010	68000/68010	68000/68010	68000/68010	68020
FREQUENCY	8MHz	12.5 MHz	12.5 MHz	12.5 MHz	12.5 MHz	12.5 - 20 MHz
MEMORY MANAGEMENT	68451	68451 (2nd as option)				
DMA	LOGIC		68450 option	68450 option	68450 option	
FLOATING POINT PROCESSOR		68881 (option)			68881 (option)	68881 (option)
RAM (DUAL PORTED)	256 Kb	2 Mb	128/512 Kb	128/512 Kb	512 Kb	1/4, 1, 4 Mb
EPROM		2 Sockets (128 Kb)	2 Sockets (128 Kb)	2 Sockets (128 Kb)	2 Sockets (128 Kb)	2 Sockets (128 Kb)
EEPROM			2 Sockets (16 Kb)	2 Sockets (16 Kb)		
SIO	1 PORT	1 PORT	2 PORTS	4 PORTS	• I/O ON PIGGYBACK BOARDS • PB-SCSI1 SCSI/DMA • PROTO BD	3 PORTS
PIO	1 PORT		1 PORT			
TIMERS	1	4/ 8 bit	3/ 16 bit			1/ 32 bit
ADDITIONAL FEATURES	1K PROM FLOPPY DISK CONTROLLER	Translation Cache	R/T CLOCK 58274	R/T CLOCK 58274		
SOFTWARE	UNIX* SYS V	UNIX* SYS V pSOS**	pSOS** PDOS***	pSOS**	pSOS**	pSOS** PDOS***

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cancel the instruction being processed when a branch is detected.

When branching occurs, the cancelling of a newly generated address costs a cycle. This is not a problem for applications that are largely sequential. For applications that involve much decision making and branching, however, this may prove costly.

"Any time you do a branch, you waste the instruction immediately following the branch" says Fair. "When the branch address comes out of the part, it's already working on the next instruction in the next sequential structure. So Weitek needs procedures like stall, abort and neutralize."

Adding convenience

A convenience feature of the WTL7136 is the Breakpoint/Watchpoint register, which makes debugging easier. Either a data address or a code address can be loaded, which then halts execution (via an interrupt) when an attempt is made to access data at the data address or execute code at the code address.

The Op bus is a unique feature of the WTL7136. The Op bus is a five-bit output bus for the control of external devices. It indicates the type of operation that is currently taking place in the sequencer. For example, says Torban, "if you wanted to control a cache memory controller based on what instruction is being executed in the sequencer, the sequencer puts out a code that your external hardware decodes and performs the required function."

Both parts feature traps, which are mainly used for system calls, especially in the case of cache memory misses where system servicing is required. The trap is essentially an interrupt for that purpose. Analog Devices invokes a trap via a dedicated pin (TTR). When TTR is detected by the ADSP-1401, the highest level of interrupt occurs, and the system can then download to the cache or do whatever else may be necessary.

Weitek, on the other hand, implements traps in software. Three software trap instructions have slightly different effects. One system trap simply interrupts the processor. One system trap with backup interrupts the processor and backs up one cycle, and another system trap pushes the contents of the WTL7137 integer processor register onto the stack.

Although Weitek has three trap instructions, Analog Devices has a related instruction that Weitek does not have—a write-control-store instruction used for downloading memory to the cache when a cache miss occurs. This feature provides sequential addressing during microcode downloads to a RAM-based microcode store and is a significant convenience.

Bus size is another major point of difference. The ADSP-1401 has 16-bit data and output address buses and a 7-bit instruction bus. As a result of the 16-bit address bus, addressing of microcode memory is limited to 64 kbytes, which is usually considered sufficient. The WTL7136, on the other hand, has three 32-bit buses: the output code address bus, the data address bus, and the code bus. These buses contribute to a hefty pin count of 144 pins. By contrast, the ADSP-1401 is a 48-pin device.

More address space

Because of the large address bus, the WTL7136 addresses up to 4 Gbytes of memory. Why is there so much address space in systems that have traditionally gotten by on much less? "With microprogrammable devices, it's very difficult to program more than 16 kbytes of microcode words, not to mention 64 kbytes," Weitek's Torban says. "We chose to provide 32 bits of code address space, and that gives you 4 Gwords. Obviously, we didn't think that anybody was going to write microcode of that depth. We did it because we intended the family to work with main memory systems."

This, perhaps more than anything else, differentiates the two parts. While the Analog Devices part is a high-performance, full-feature device with a 70-ns cycle time (compared with the 80- and 100-ns cycle times for the Weitek part), the Weitek device must be evaluated from Weitek's perception of how it will be used.

Weitek anticipates that the sequencer will be used primarily with other Weitek components; therefore, the system is tightly coupled. Torban points out that in microprogrammed systems of the past, the main emphasis has been on flexibility for the designer. But programming these devices has been difficult.

"Weitek has decided to take a more integrated approach to the hardware," says Torban. "Integration requires partial freezing of the hardware. What we have retained is the performance."

Weitek is trying to make things easier for the designer, and a major component of its strategy is the Accel software development tools for the new sequencer and its related hardware family members, the WTL7137 integer processor and the WTL313/332 floating-point processor. The Accel software includes compilers for Pascal, Fortran and C to allow rapid software development with large main-memory programs. Key to Weitek's thinking is the idea that noncritical code can be compiled from high-level sources, while critical code can be hand-coded for performance.

Commenting on the approach chosen by Weitek, Fair says, "Weitek seems to have in mind a RISC-type architecture that attempts to do away with the distinction between microcode memory and program memory." Stating that 16 bits is fine for a microprogram control store but not enough for a RISC-type processor, Fair says that it seems as if Weitek is trying to cover several bases. "If I were a designer building a microcoded machine, and if everything else were equal, I'd go with the small part that did the job—a 48-pin DIP or 52-pin PLCC. Why do I need 32-bit ports?" The answer, says Weitek, is Accel. **CD**

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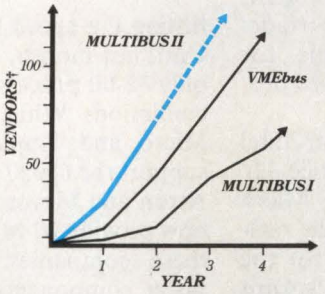

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ICE makers grapple with 32-bit microprocessors

With the introduction of two in-circuit emulators for the Intel 80386 and the announcement of two 20-MHz emulation systems for the Motorola 68020, emulation for 32-bit microprocessors took a big step forward at the end of 1986. But emulator manufacturers face difficult challenges and painful tradeoffs as they develop tools for increasingly fast and complex processors.

The ICE-386 system from Intel (Hillsboro, OR) and the Mice-32/80386 emulator from New Micro (Gardena, CA) both provide real-time emulation at 16 MHz for the 80386. Meanwhile, Hewlett-Packard (Colorado Springs, CO) has brought out a 20-MHz 68020 emulator for its HP 64000 development system, and Atron (Saratoga, CA) has announced a PC-hosted 20-MHz 68020 emulator for less than $10,000. With the 68020 now available at 25 MHz, however, emulator vendors are still playing catch-up to the chip's expanding capabilities.

At 20 MHz, an emulator has just 50 ns to read, write and access overlay memory. While high-speed memories and new cabling schemes have pushed emulation up to 20 MHz, it's unclear whether 25 MHz can be achieved without rethinking the design of emulators or compromising performance. Such features as an on-chip memory management unit (MMU), cache and prefetch queueing also pose severe challenges for emulation, and make it difficult for the user to determine what's going on inside the chip.

Independent emulator manufacturers such as Zax, Sophia, Arium and Microcosm all plan to support 32-bit microprocessors, but have delayed their plans until 1987. While Sophia (Santa Clara, CA) has close ties to Japanese chip makers, the other manufacturers will probably start with Intel or Motorola microprocessors. National Semiconductor (Santa Clara, CA) sells an emulator for its 32032 processor, and AT&T Technologies (Berkeley Heights, NJ) provides emulation for its WE 32100 processor. Nobody has even tried to emulate the 33-MHz Clipper from Fairchild (Mountain View, CA).

Richard Goering
Senior Editor

Hitting the speed limit

Until last month, the 68020 was the only 32-bit processor supported with emulation. While Tektronix, New Micro and Applied Microsystems support the 68020 at 16.6 MHz, HP, Atron and Motorola (Phoenix, AZ) now provide 20-MHz emulation. All these companies have turned to faster components and have found ways to save a few nanoseconds by shortening cables. The HP 64416 A/B emulator, for example, puts emulation memory in the microprocessor pod itself and uses 25-ns static RAMs for overlay memory. But product marketing engineer Jim Ting concedes more must be done to get HP emulators up to 25 MHz.

To reach speeds as high as 25 MHz it will be necessary to turn to unbuffered emulation, according to Richard Jensen, vice-president at Applied Microsystems (Redmond, WA). That means the emulator won't provide switching circuits to protect itself against power surges or inconsistencies in the target. "The tool will become more vulnerable at higher speeds," says Jensen. But Motorola staff engineer Jay Hartvigsen predicts his company will be able to emulate at 25 MHz by providing still faster parts for its HDS-300 emulator.

The MultiV 68020 emulator from Tektronix (Beaverton, OR), the ES-1800 emulator from Applied Microsystems and the Mice-32/68020 emulator from New Micro insert wait states at 16.6 MHz when emulator memory is used. Opting for less expensive memories, these emulators run in real time at 16.6 MHz only in the target memory. Atron's 68020 Probe/3 emulator uses 40-ns SRAMs, but inserts one wait state at 20 MHz when running out of emulator memory. By using 25-ns SRAMs, HP and Motorola can operate out of emulator memory in real time at any speed.

All 68020 emulators are subject to the extremely tight timing relationships presented by the microprocessor itself. At 16.6 MHz, a user-generated signal named DSACK must be returned from the negative-going edge of the address strobe within 25 ns. Since the emulator itself will eat up much of this time in signal transmission, wait states will be inserted unless the user returns DSACK without delay. Real-time emulation without wait states is thus prototype-dependent and may not be possible in practice.

Looking inside the chip

The new 80386 emulators from Intel and New Micro support real-time emulation up to 16 MHz, the maximum rated speed of the 80386. Like most 68020 emulators, these emulators insert wait states at 16 MHz when emulation memory is used. "To get full-speed emulation with no wait states, you need static RAMs," says Gordon Reid, marketing manager for Intel Development Systems (Hillsboro, OR). "We use dynamic RAMs, and we look to the user's target to provide no-wait-state emulation."

Both the 80286 and the 80386 support a real-address mode and a protected virtual-address mode. Reid says that protected mode cannot be emulated without a bond-out chip, a proprietary version of the microprocessor with key signal lines brought out to external pins. Intel uses bond-out chips in its own emulators but doesn't make them available to outside suppliers. Applied Microsystems emulates the protected mode of the 80286, but Jensen declines to say how. HP emulates the protected mode of the 80286 by using its own custom bond-out replacements.

New Micro emulates the protected mode of the 80286 by interrogating the instruction descriptor table base

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The PC-hosted Mice 32/80386 emulator from New Micro provides real-time emulation of the 80386 up to 16 MHz. New Micro plans to emulate the protected virtual-address mode of the 80386 by interrogating internal registers in software.

register in software, and plans to use the same technique in a later release for the 80386 emulator. The descriptor table allows the emulator to trace the sequence of instructions through the microprocessor. But Intel's Reid believes this trace won't be fully accurate without a bond-out chip. "You might have a fair idea of what's going on inside the chip, but when you get to a critical decision point, you're not quite sure what happened," says Reid.

The 80286 and 80386 also have an on-chip MMU, which means that an emulator looking at a microprocessor's address lines can't determine which address in real memory is being accessed. This isn't normally a problem for symbolic software debugging, because users set breakpoints on symbols rather than on addresses. But if users need to know a physical address, most 80286 emulators require that they figure it out by hand. It's possible to determine physical addressing without bond-out chips, and New Micro provides physical addressing by accessing the instruction descriptor table.

The 68020 doesn't have an on-chip MMU, but its on-chip cache causes a similar problem. When the cache is in operation, the address bus is quiet and the user doesn't know what's going on inside the chip. Motorola provides an instruction that disables the cache, and 68020 emulator vendors suggest that the cache be disabled for most debugging modes. "Ideally, you'd like to be able to emulate the cache, to set breakpoints and throw it up on the screen," says Dave Blakemore, vice-president of Arium (Anaheim, CA).

Microprocessors such as the 80286, 80386 and 68020 use prefetch queueing, which means the processor fetches instructions that might not be executed. This makes it difficult to determine program control from the emulator's trace display. To make debugging easier, HP's 80286 emulator dequeues the executed-instruction flow in real time. Intel uses its bond-out chips to look at the end of the execution stream after the fetch has taken place.

Emulating other chips

Independent emulator manufacturers pursue the 68020 and 80386 because they're perceived to be mass-market chips. For emulation support for National Semiconductor or AT&T 32-bit microprocessors, users must turn to the chip makers themselves. National's ISE32 in-circuit emulator can emulate not only the 32032 CPU, but also the 32082 MMU and 32201 timing control unit. Although the 32032 can run at 15 MHz, ISE32 supports real-time emulation up to 10 MHz only.

AT&T Technologies provides an emulator for its 32100 chip set, including the CPU and MMU. While the emulator runs up to 14 MHz with no wait states, the 32100 now goes up to 18 MHz. Instead of pushing emulation to that speed, AT&T plans to release a "footprint monitor" to handle faster versions of the 32100. This tool can observe the CPU but can't control program execution. "It's less intrusive into the target system than an emulator," says AT&T hardware designer Bob Rango.

The Fairchild Clipper is beyond today's emulation technology not only because of its 33-MHz speed, but also because it uses a modified Harvard architecture with separate buses for data and instructions. Emulator vendors would thus have to emulate two buses and keep them synchronized. "We've found a decreasing demand for emulation and an increase in the demand for performance tuning tools," says Gary Baum, strategic marketing manager for the Clipper. **CD**

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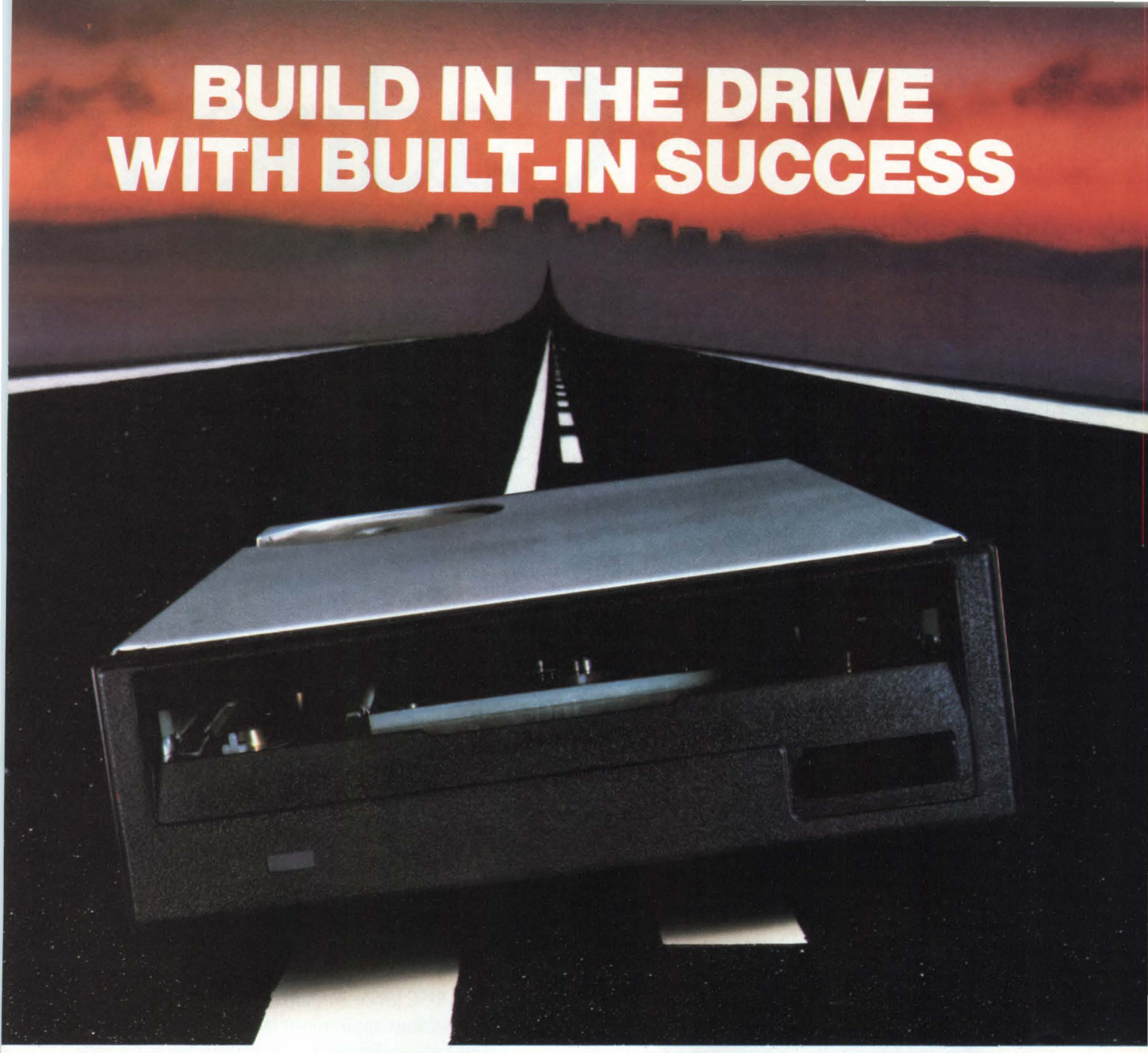

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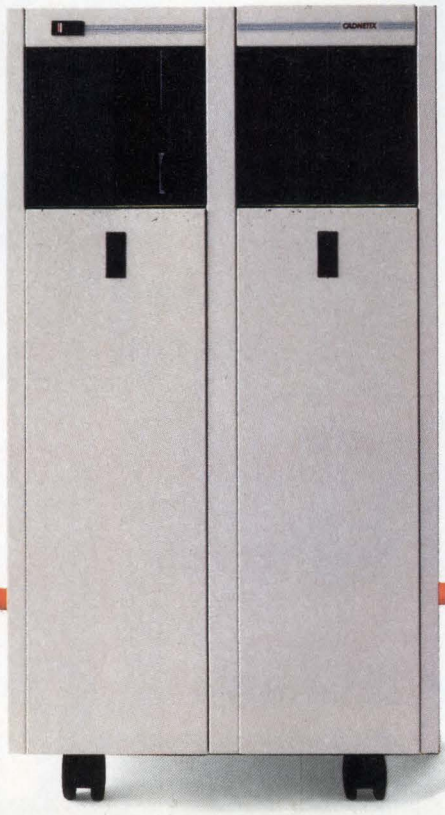

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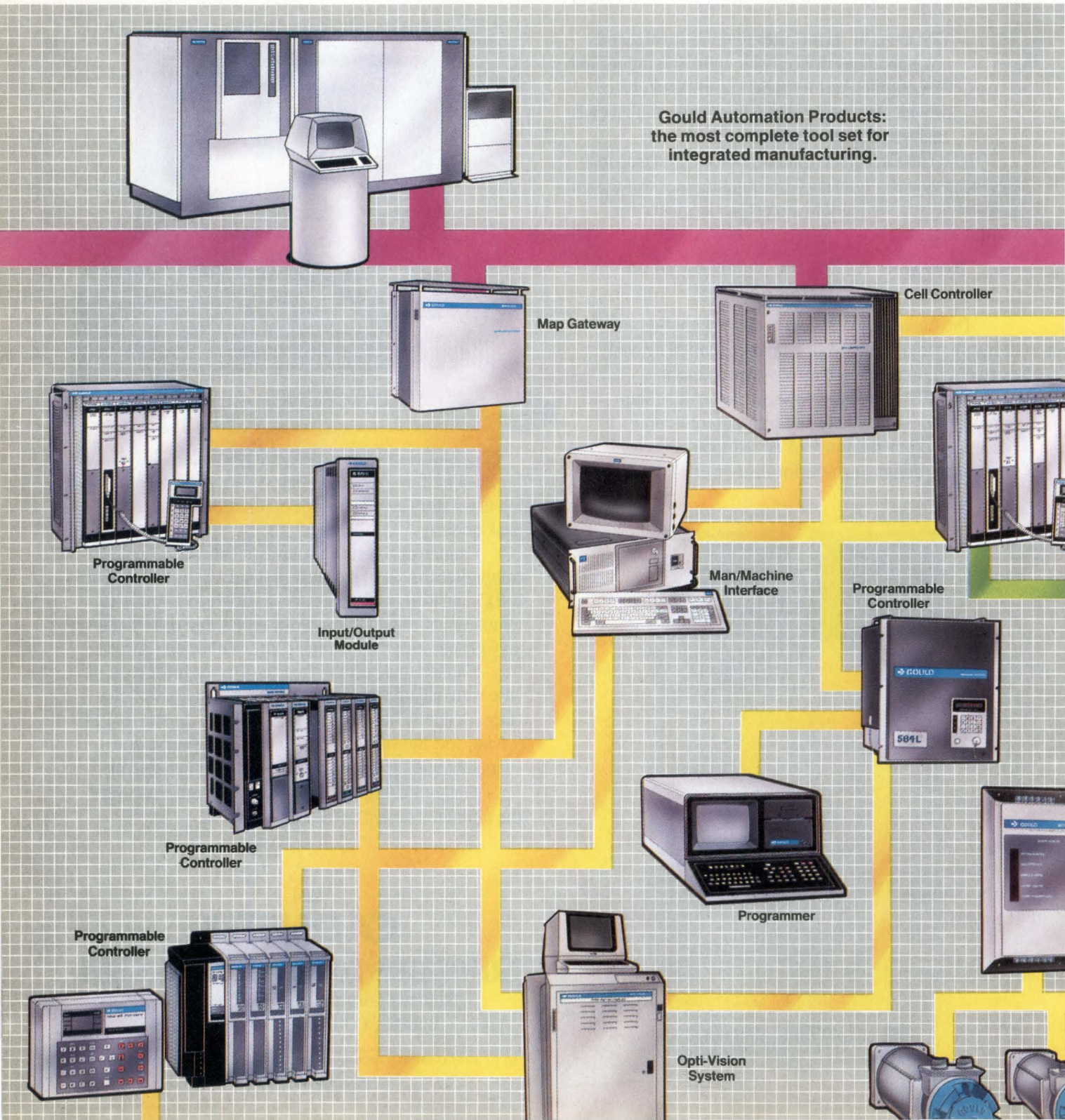

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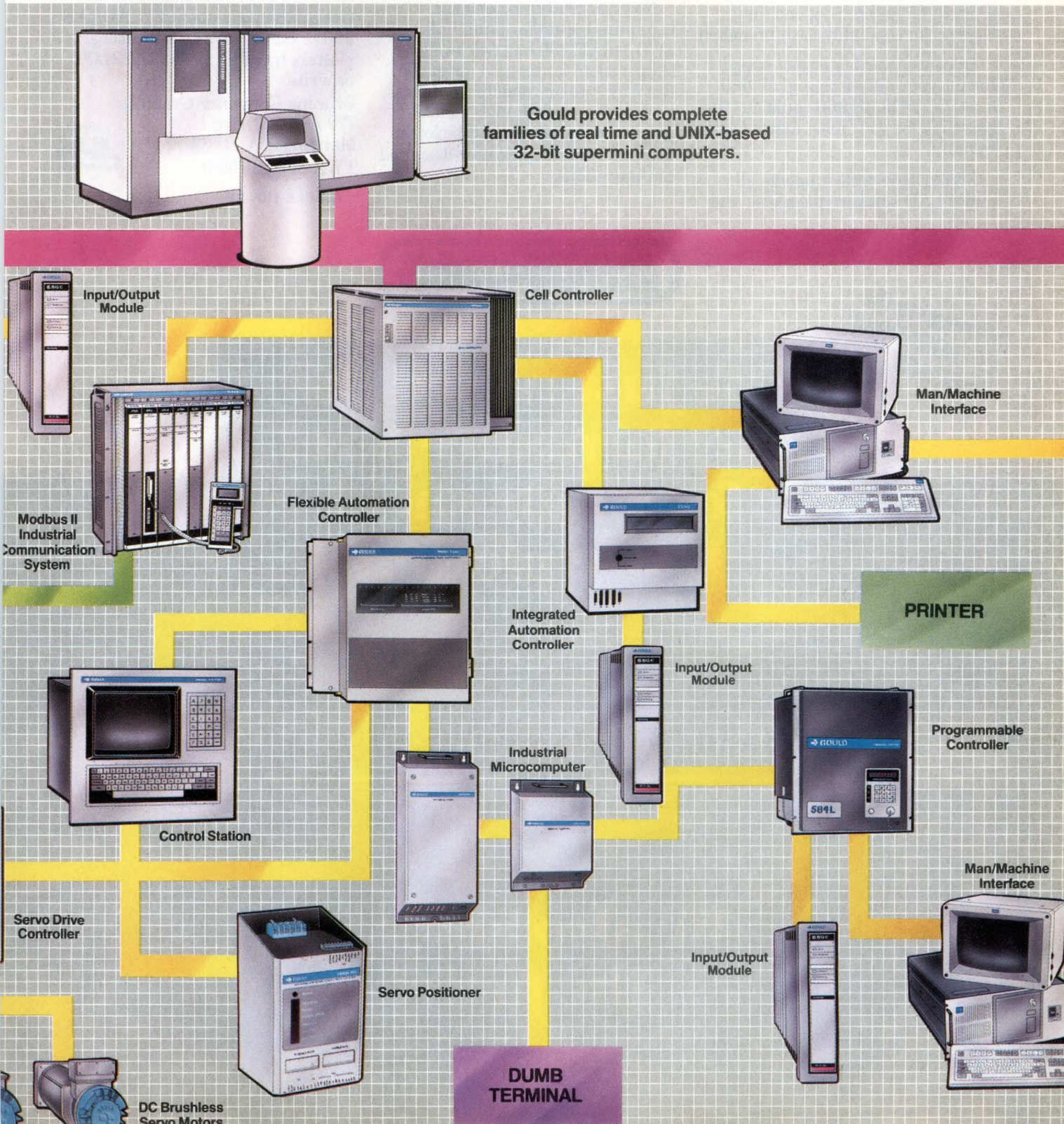

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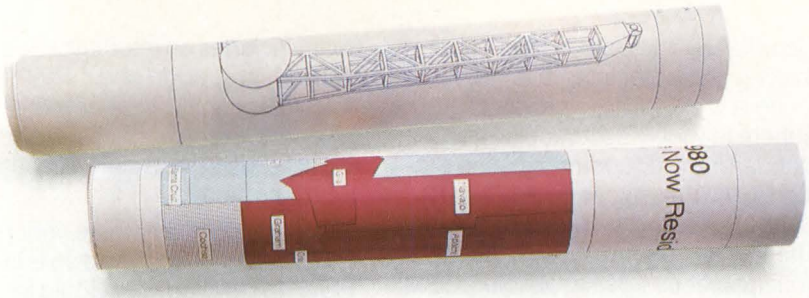

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RISCs and parallel processors drive multiprocessing innovations

Multiprocessing and distributed processing come to life as novel computer architectures hike performance and lower cost.

Nicolas Mokhoff
Senior Editor

The onslaught of novel computer architectures ranging from parallel processing to reduced-instruction-set computers (RISC) continued unabated this past year. Because of the possibilities offered by VLSI chips, more computer manufacturers took the plunge into innovative designs. Computers, from mainframes to fully functional boards, have brought the concepts of multiprocessing and distributed processing to life.

In terms of computer architecture, 1986 was the year of RISC. Besides the much heralded entry of IBM's RT PC, Hewlett-Packard and startup MIPS Computer Systems introduced RISC products. MIPS Computer (Sunnyvale, CA) made a splash in the early part of the year by announcing that it would supply, on an OEM basis, high-performance system building blocks based on its proprietary RISC architecture. Nearly 20 computer manufacturers, system integrators and government system suppliers are already designing products based on MIPS Computer technology. According to the company, the RISC products bridge the gap between superminicomputer performance and microprocessor cost by achieving performance levels two to five times that of traditional 32-bit microprocessors—and at competitive prices.

MIPS Computer's R2000 series of products offer sustained performance of 3, 5, 8 and 10 Mips and are an outgrowth of the Stanford RISC research project, called the Microprocessor without Interlocking Pipeline Stages—MIPS. The project combined IBM's study of optimizing compilers with Berkeley's development of a VLSI RISC chip. The R2000 products include component kits, CPU boards, a development system, a memory option, optimizing compilers for C, Pascal and Fortran and two versions of the Umips operating system (a Unix derivative). The R2065 component kit includes a 12.5- or 16.7-MHz CPU chip capable of 8 or 10 Mips,

respectively, a MIPS Computer floating-point accelerator chip, a write buffer consisting of four gate array chips and a binary copy of the Umips operating system, utilities and C compiler. The MIPS Computer CPU boards feature the basic building blocks contained in the component kits, preconfigured and manufactured with either a standard VMEbus or Multibus II.

Hewlett-Packard (Palo Alto, CA) made the decision several years ago to base its next generation of computers on RISC technology. Its Spectrum family of RISC-based minicomputers, introduced this year, maintain compatibility with the company's installed base of complex-instruction-set computers (CISC), which are members of the HP 3000 family. According to HP, many current applications could be easily moved to the new Series 930 and 950 computers because the new systems run the existing HP 3000 object code without modification, recompilation or data conversion.

Pyramid Technology (Mountain View, CA) was one of the first to implement RISC as a means of enhancing the multiuser, multitasking performance of Unix. Introduced by Pyramid in the last year, the Workcenter acts as a communications gateway to corporate data centers, and as a departmental hub interconnecting workstations and PCs. Recently the company introduced its Series 9000—two Unix-based 32-bit superminicomputer platforms for multiuser, multitasking applications, such as data base systems, networking and software development. Pyramid has also started offering its machines domestically on an OEM basis.

High-performance system building blocks incorporating RISC principles include component kits, CPU boards, and development systems for design and software engineers. The products are intended to establish a new price/performance standard for systems in the 3- to 10-Mips performance range.

Another early producer of RISC-type machines, Ridge Computers (Santa Clara, CA), unveiled its 3200 Model 90 system for computationally intensive scientific and engineering applications. The machine is the high end of the company's line with computational performance rivaling that of DEC's VAX 8600. It processes single-precision calculations at 4.3 MWhetstones/s and runs double-precision calculations at 2.4 MWhetstones/s. It features a microprocessor-based service processor that manages all remote diagnostics. The 3200 has a peak I/O transfer rate of 18.3 Mbytes/s in burst mode with a typical rate of 10.7 Mbytes/s. Configured for maximum performance, the system has a 600-Mbyte hard disk, 16 Mbytes of main memory and 16 RS-232 ports, expandable to 32.

The past year was also marked by a few entries in the minisupercomputer market. There are three architectural approaches to scientific and engineering computing: vector, parallel and RISC. Vector architectures, such as in the SCS-40 from Scientific Computer Systems (San Diego, CA), offer high performance by using single-machine instructions that operate on multiple data elements, or vectors. When introduced early this year, Scientific claimed that the machine delivers 25 percent the performance of the Cray X-MP/1 supercomputer for about 10 percent of the cost. An entry-level system costing $595,000 executes up to 44 MFlops. Scalar performance is equally impressive at 18 Mips.

Parallel processing technology also made a major attempt to move into the mainstream of computer architecture during the past year with products differentiated by price/performance trade-offs. The hypercube was one of the more innovative parallel processing architectures introduced last year because its power grows in proportion to the number of processors that are connected in the array. Use of the most powerful mass-produced microprocessor chips may facilitate the construction of hypercube computers many times more powerful—but less costly—than today's fastest supercomputers.

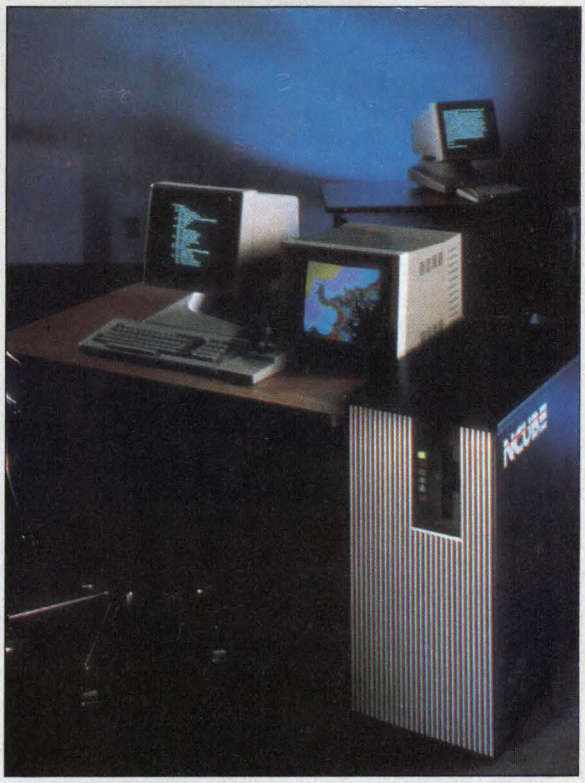
Intel Scientific, Ncube and Floating Point

Systems, (all Beaverton, OR), introduced hypercube machines (see "Hypercube architecture leads the way for commercial supercomputers in scientific applications" *Computer Design,* May 1, 1986, p 28). Meanwhile, Ametek (Arcadia, CA) has been working on its next-generation hypercube machine—the Mark III. Its supernodes will consist of MC68020-based boards, each of which will rival or exceed the performance of a typical superminicomputer. According to Ametek, a concurrent computer assembled from 32 supernodes would have the performance of the fastest current supercomputers at less than one-twentieth the cost.

Clearly, the most significant parallel processing architecture introduced in 1986 was that in the Connection Machine, a 64,000-node parallel processor implementing data-level parallelism. Individual processors assigned to individual elements of data attack the entire problem at once, allowing operations on all data elements to proceed in parallel. If there are fewer than 64,000 data elements in the problem, the system assigns a complete processor to each one. If there are more than 64,000, the system operates in virtual processor mode on data sets with as many as a million elements. The Machine's developer, Thinking Machines (Cambridge, MA), claims that the power of 64,000 processors operating in parallel yields performance above 1,000 Mips in a wide range of applications areas. By contrast, the biggest conventional large-scale machines operate at less than 40 Mips.

Key to the success of parallel processors is the ability to add more processors without substantially increasing the time devoted to interprocessor communications. Ideally, total system power should approach or equal the sum of the power of each individual processor. For most applications, this is posssible only with an internal network that eliminates bottlenecks that impair performance. BBN Advanced Computers (Cambridge, MA), believes its Butterfly machine comes closest to bottleneck-free operation. In fact, BBN's 256-processor version, made commercially available this year, has achieved a computational speed of more than 230 times that of a single component processor using a variety of standard benchmarks.

BBN attributes its success to an internal communications method different from that of the hypercube or the bus. In the hypercube design, each node connects to several immediate neighbors and supports systems with a large number of processors. This method, however, can be inefficient if communications with nonadjacent nodes is desired. The number of processors that can be added to bus architectures is limited. BBN applies its packet-switched networking techniques to interprocessor communications. This interconnection method directly connects multiple processors without requiring numerous point-to-point connections.



Ncube/seven is a desk-height parallel processor that can support up to 16 users on a maximum of 128 processing nodes. Its hypercube architecture is distributed among boards that house 64 processing nodes each. When two boards are inserted, the wiring in the backplane creates an order-7 hypercube.

Central to the Butterfly computer's communications method is a proprietary switch containing custom VLSI switch chips. The switch uses packet addresses to route data to and from processor nodes. Since processors are relieved from the responsibility of routing, interruptions and delays are eliminated. Using both local and shared memory, the Butterfly doesn't use messages to retrieve data. Instead, it directly references memory located anywhere in the system.

Another form of parallel processing that made an appearance in 1986 was dataflow parallel processing computing. The LDF 100 dataflow machine from Loral Instrumentation (San Diego, CA)

Chan Russell
Vice-president of product development
BBN Advanced Computers

The need for parallel processing

Continuous-process industries, such as the oil, chemical, power and paper industries, could use complex simulation and modeling for planning and designing a new plant, developing control algorithms, training operators with a real-time model, monitoring the plant's operation and detecting and repairing problems. For tasks as diverse as general-circulation weather modeling, resolution of numerous algebraic and partial differential equations in the design of bridges or three-dimensional modeling of oil fields, parallel processing offers more computing power than conventional computers at a better price/performance ratio. With such complex environments, simulation provides a more economical and, in some cases, a more realistic model than is possible with physical experimentation. Both complex simulation and modeling make significant demands on computer systems—demands that parallel processing is uniquely qualified to satisfy.

The greatest of these requirements is the ability to manage complexity in real time. Matrices used to construct real-life models of a system can contain hundreds of thousands of elements. A minicomputer able to quickly solve a 100-×100-element matrix is at a loss when the matrix's dimensions are 1,000,000×1,000,000. For example, today's most powerful minicomputers can only effectively simulate circuits with a hundred or so transistors. The ability to accurately detect errors in circuits containing hundreds to thousands of transistors prior to chip fabrication is possible through parallel processing, and it offers great ecomonic benefit. Similarly, simulating a single combustion cycle in an automobile engine today takes up to 80 hours on a conventional mainframe. Increasing the simulation speed by 1,000 percent through parallel processing has obvious positive consequences.

Clearly, the ability to solve complex tasks quickly is essential. Although parallel processing has the potential for effectively solving such problems, this potential is only realized if the commercial parallel processor has general-purpose features that adapt well to these applications. Parallel processors with a large number of homogeneous processors and a fast interconnection network are particularly effective for complex simulations. Each component of the simulation can be mapped to a processor that interacts with individual components. Because the simulations will increase in complexity over time, it is also important that the parallel processor be incrementally expandable. Finally, in order to meet real-time requirements, parallel processors must have fast I/O to match their high processing capabilities.

Image processing is also an important applications area for parallel processing. High-level vision is critical to robotics and manufacturing as well as being a key element in inspection, automated assembly, welding and sorting operations. Parallel processing permits the reconstruction of 3-D surfaces from visual inputs for the inspection of multidimensional parts, the recognition of partially obscured parts or the analysis of complex images of a moving scene.

Images of a scene are recorded by several cameras and stored in a parallel processor as a collection of pixels. The digitized image is then processed to gain information about a scene. A scene with a 3-D object typically only registers as a 2-D image on a conventional computer. Information is therefore lost and the image analysis is inaccurate. The ability to produce a multidimensional image, simultaneously accounting for numerous variables such as shading, texture, movement and obstruction, is an inherently parallel task. Parallel processing provides the computing power needed for high-level vision, greatly improving image analysis accuracy. This additional processing power offers great economic benefit in manufacturing, where today's mechanical systems—expensive to maintain and relatively slow in operation—could be replaced by fast, efficient optical systems powered by parallel processors.

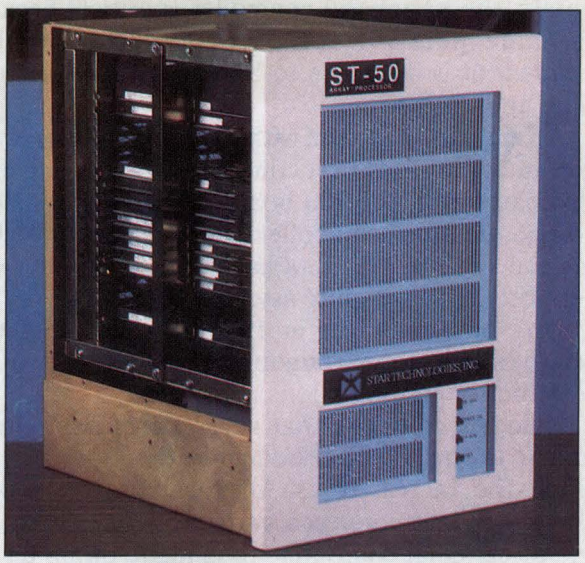
Shared-memory parallel processors are especially useful in high-level vision applications. In a shared-memory, tightly coupled parallel processor, all processors have equal access to all memories within the system, as opposed to loosely coupled, private-memory parallel processors where processors can't read one another's memories and must pass messages across communications links. High-level vision is well suited to a shared-memory architecture because it is most efficient when a single, shared view of an image can be analyzed from several perspectives—rather than having a duplicate of this information for each processor.

epitomizes this technique. The LDF 100 fills the void between the fastest generation of superminicomputers, typified by the 4-Mips VAX 8600 and low-end supercomputers that have speeds of approximately 60 Mips. Offering configurations between 5 and 256 Mips, the LDF 100 is data-driven, as opposed to the usual instruction-driven machines. Processors wait until they receive the data instead of continually processing instructions.

Dataflow architectures are categorized by their granularity—the amount of processing occurring at any processor—and by their static or dynamic capability. Granularity is referred to as either small- or large-grain. The granularity of the Loral dataflow machine is medium- to large-grain with a static distribution of functions. Functions can be individually programmed in C, Fortran and Ada, with the description of the dataflow graph written in Loral's Datagraph Language.

Another entry in the parallel arena this year was the Balance 21000 from Sequent Computer Systems (Beaverton, OR). This latest entry in the Balance family of computers can be configured with up to 30 32-bit processors, compared to the previous Balance 8000, which accommodated two to 12 processors. The 21000 enlarges the simultaneous user base to 256. Balance computers incorporate an innovative parallel computing architecture that supports traditional sequential applications and parallel applications at the same time. Parallel programming, which allows appropriately structured applications for improved performance, is supported by shared memory and fast synchronization between hardware and Sequent's high-level language software libraries.

In another category of computer technology—array processors—the trend is toward more embedded functionally and smaller-size systems. By incorporating CMOS VLSI chips, Star Technologies (McLean, VA) was able to squeeze 50 MFlops into its ST-50—a 19-×26-in. package. Star's first product, the ST-100, included multiprocessor architecture combined with emitter-coupled logic chips that yielded 100-MFlops operation. This year's addition to Star's stable is a compact version of the ST-100 adapted from its architecture using high-density CMOS technology. These CMOS logic chips incorporate at least five times more gates per chip, enabling Star to physically reduce the size of the ST-50 to approximately 3 ft^3. Consuming less power and costing less than ECL versions, the CMOS-based machine can nevertheless achieve 50 to 60 percent of the computational speed of the ST-100. Principal applications of the ST-50 are in medical imaging, nondestructive testing systems and digital signal processing systems.



A compact CMOS-based array processor operates at 50 MFlops in compute-intensive applications such as siesmic data processing, modeling and simulation and medical imaging. The ST-50 from Star Technologies uses multiple processors for I/O, storage movement, arithmetic operations and control.

In the commercial computer market, a significant introduction was an internal bus for a new VAX line of machines—the 8200, 8300 and 8800 from Digital Equipment Corp (Maynard, MA). DEC decided to incorporate a 32-bit bus called BI-bus that can transfer data at 13.3 Mbytes/s. After its introduction, 13 vendors announced their support for the new synchronous bus. Events occur on the BI-bus at fixed 200-ns intervals, with all address, arbitration and data transmission time-multiplexed over its 32 data lines. The physical address space is 1 Gbyte. The bus is supposedly an interface only for DEC's high-end computers and not intended to be competitive with either Multibus II or VMEbus third-party boards.

While the board market for 32-bit systems experienced healthy growth during 1986, a discernible trend is that of more specialty boards for both the Multibus and VMEbus. The special niches that have recently sprung up include analog I/O, disk controllers, communications and high-performance boards. According to Xylogics (Burlington, MA), the peripheral controller is the secret ingredient behind high-level computer system performance. Unlike many other board-level products that play a nominal role in supermicrocomputer,

workstation, parallel and multiprocessing computers, the peripheral controller is critical because the more quickly data is transferred, the more bus bandwidth is available to handle demanding real-time applications.

After scoring success with disk controllers, Xylogics introduced its first communications controller this past year. The 780 board is the first VMEbus communications controller to feature a full 32-bit, instead of a 16-bit, data path. The controller can support 16 full-duplex asynchronous ports at 9.6 kbits/s or eight ports at 19.2 kbits/s on a single board, improving throughput 70 percent over other VMEbus communications controllers.

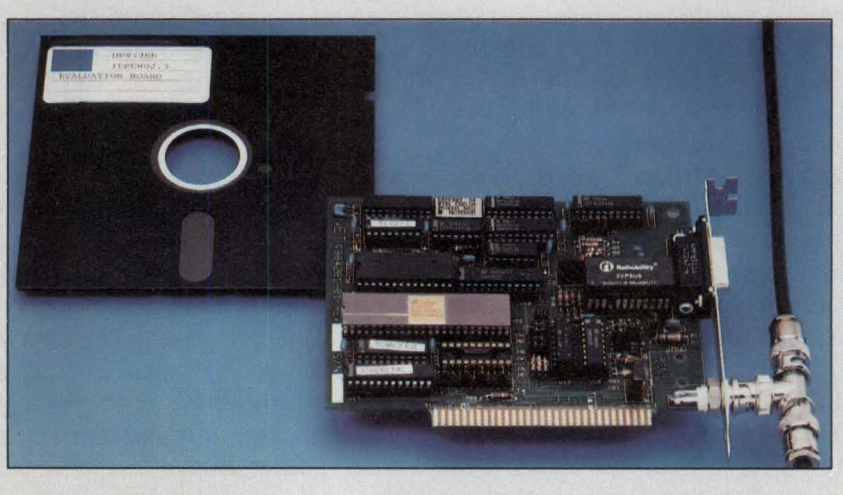
Xylogics contends that several factors contributed to the need for a product like the 780. These include the increased use of local area networks (LANs) to interconnect a variety of computers, the use of personal computers to emulate dumb terminals and the broadening implementation of Unix multiuser computers for commercial applications. The result has been a reduction in the need for synchronous communications between computers and an increasing number of asynchronous lines and trafficon Unix machines.

The WE321SB from AT&T Information Systems (Holmdel, NJ) is one of the most recent examples of an open-system single-board computer. With the Unix V/VME operating system, the board provides an OEM with the fundamental hardware and software tools to produce a system product that can exploit the existing hardware of the VMEbus as well as existing Unix applications packages. The processor board executes programs out of on-board local memory in a 5-cycle zero wait state at 18 MHz. Using Berkeley benchmarks, the processor board provides performance equivalent to 3 VAX-11/780 Mips on the average. The single-precision Whetstone benchmark executes at 1.2 MWhetstones/s.

Future enhancements to the WE321SB include real-time and 4-Mbyte local memory versions. The WE32200 processor chip set, a planned third generation of 32-bit chips, is projected to double the performance of the current WE32100 chip set. An upgrade to Unix Release 3.1 with remote file sharing and the Streams mechanism will also be included in the upgrade.

Development boards from IC vendors that offer data communications chips were also on the agenda for 1986. With the IEEE standards for LAN interfaces 802.3, 802.4 and 802.5 reaching the final acceptance stage, IC vendors are confident enough to offer LAN chips on a large-volume basis. Many of these same vendors are including evaluation boards and kits with the chips. The kits and evaluation boards help designers alleviate system-level interface problems. National Semiconductor (Santa Clara, CA) offered a three-chip set that can be used in any of the three 802.3-based LANs—Ethernet, Cheapernet, and StarLAN—and includes an evaluation board. The DP839EB board contains the three-chip set that includes the DP8390 network interface controller, the DP8391 serial network interface and the DP8392 coaxial transceiver interface. Plugged into an IBM PC or equivalent, it gives the system designer a complete diagnostic environment for evaluating the chips.

A similar arrangement has been provided this year by Advanced Micro Devices (Sunnyvale, CA). Hardware and software support for AMD's Am7990 three-chip set comes in the form of three evaluation boards: the Multibus Ethernet/Cheapernet, the Am7990 stand-alone and the IBM PC Ethernet/Cheapernet board package. The IBM



Evaluating LAN chips can become more efficient when boards that house the chips are used. The evaluation board and accompanying software for National Semiconductor's Ethernet/Cheapernet/StarLAN chip set lets system designers evaluate a LAN interface with an IBM PC.

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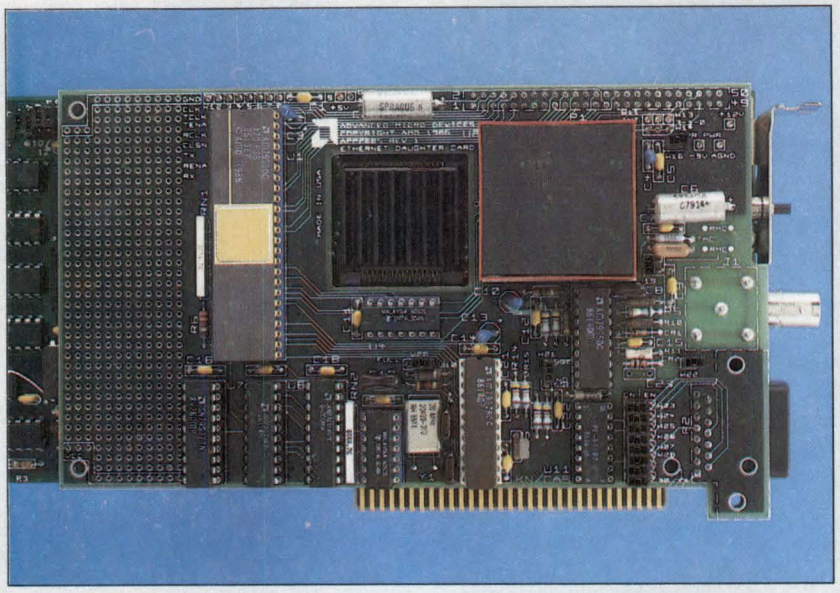

In a mother- and daughter-board combination, an on-board 80186 is used as a node processor for the three-chip LAN combination on the daughter board. The stand-alone 80186-based board speeds applications programs running on the IBM PC and supplies 16-bit bus memory for the three-chip interface set.

board consists of a mother board actually developed by Orchid Technology (Fremont, CA), under its label of PCTurbo-186. A daughter card from AMD integrates the three chips and connects them to the 80186 microprocessor via a 50-pin connector.

Texas Instruments (Dallas, TX), came up with its own network adapter subsystem that lets designers evaluate the company's TMS380 five-chip set for 802.5-based token-ring LANs. TI also offers the designer a TMS380 application-specific IC tool kit. The kit lets designers reduce the adapter subsystem housed on a full-length board to a half-length board.

TI is so bullish about its token-ring chips that it predicts that the next generation of professional workstations will all sport the token-ring networking interface. The company's bases its confidence on the fact that the IEEE 802.5 standard allows individual packets to contain over 2.5 times as many bytes as 802.3 collision-based protocols, improving the token-ring's capacity for handling large file transfers. The guaranteed access of token-passing protocols, coupled with a larger packet size, yields a 95 percent utilization of the token-ring data rate. This represents a significant advantage over collision-detection protocols. By comparison, collision-based technologies begin losing performance when 30 percent of the maximum number of users are hooked into the network. At best, they deliver less than 60 percent of the bus data rate, says TI.

The third LAN standard, the 802.4 bus-oriented, token-passing interface, received a large boost in 1986 from continuing interest in the Manufacturing Automation Protocol. Specified and promoted by General Motors to tie together computers from various vendors on the factory floor, MAP will eventually encompass all seven layers of the Open Systems Interconnect (OSI) protocols.

So far, chips and boards and some modules adhering to the standard have appeared. For example, Industrial Networking (Santa Clara, CA) introduced a MAP interface and host-resident networking software program for connecting IBM PC XTs and PC ATs to a MAP LAN system. The two-board interface includes an 80186-based controller board and a 10-Mbit/s token-bus modem board. The MP-500, when equipped with Industrial Networking software downloaded over the network, implements the entire seven-layer communications architecture specified by MAP 2.1.

Vendors that have designed products to the 2.1 version of MAP may get stung, however. Version 3.0, to be completed early next year, will affect the Applications Layer of the OSI protocols. Although products designed to Version 3.0 will be compatible with products designed for Versions 2.1 and 2.2, the opposite will not be true. Very few designs have been aired that incorporate the Applications-Layer requirements. Developing these products for the factory environment should be a boon for third-party vendors. **CD**

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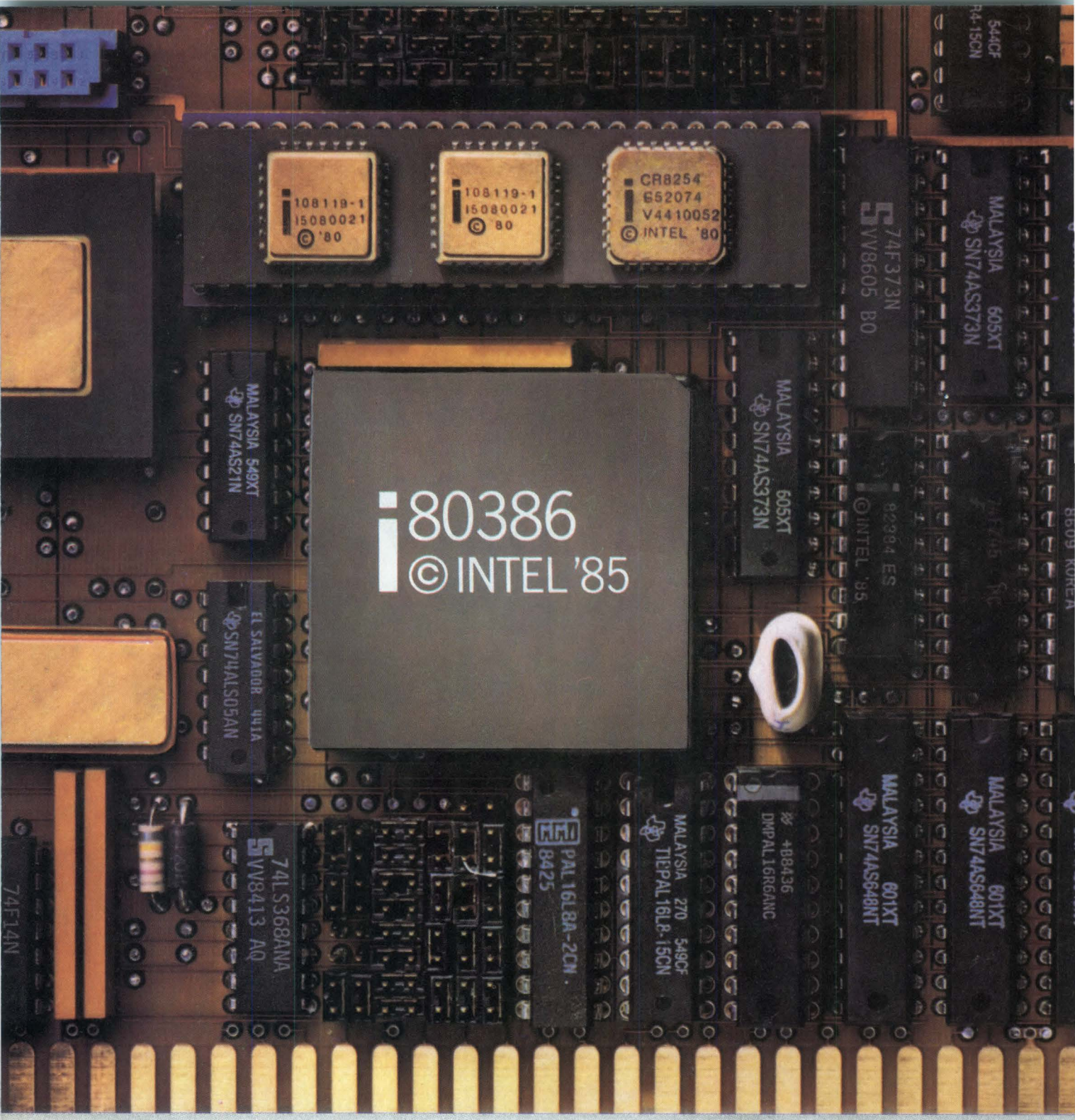

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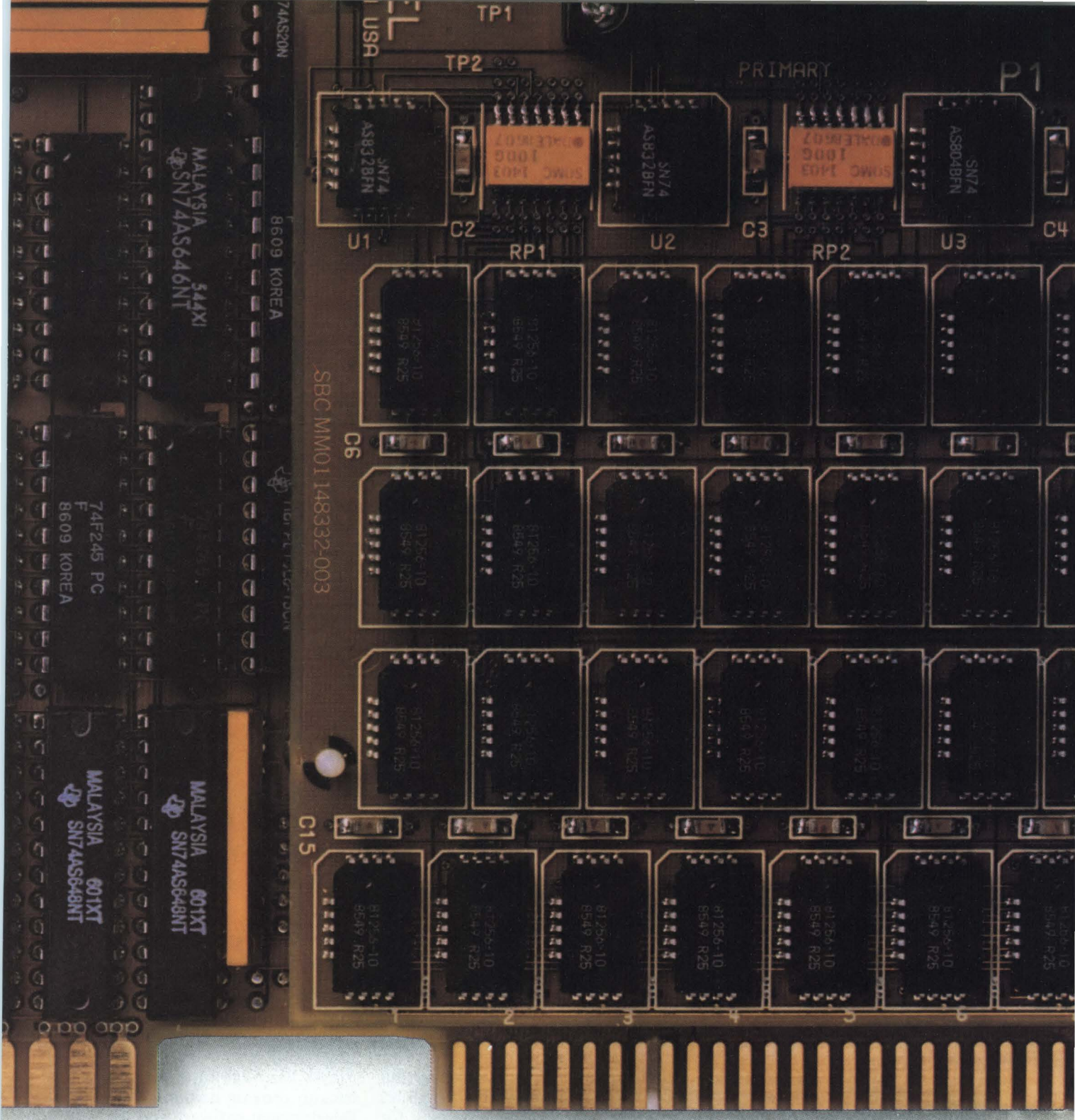

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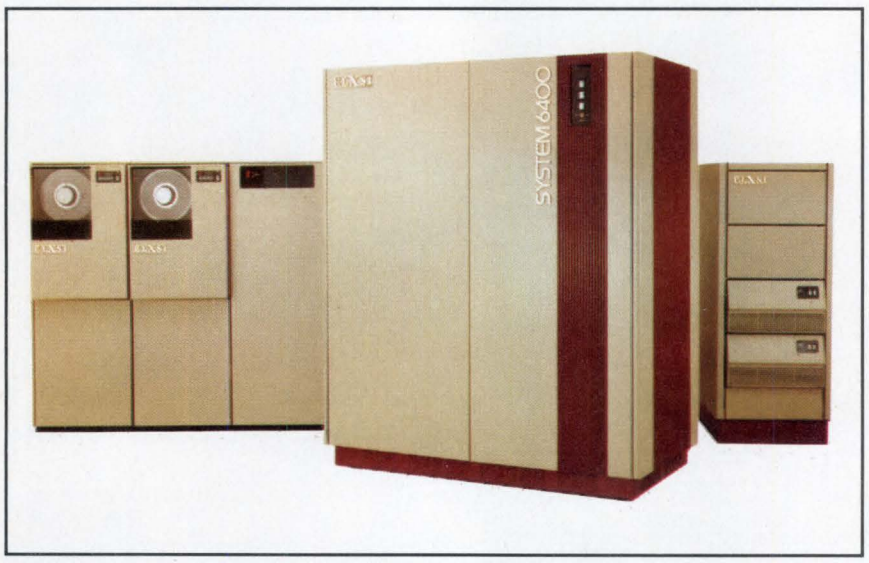
CIRCLE NO. 29

Expandable parallel processor serves supermini to low-end supermicro market

A 12-processor computer using a parallel processing architecture offers 12 times the performance of a VAX 8600 and performs at up to 72 Mips. Elxsi's computer systems fill the gap between large minicomputers and supercomputers that traditional mainframe vendors don't serve.

The expanded version of Elxsi's System 6400 offers complex problem-solving skills requiring fast, interactive processing. It can operate in time-sharing, real-time or batch-processing environments, and by incorporating one to 12 CPUs, it provides between 6 and 72 Mips. Its ability to perform equally well in both parallel processing and multiprocessing modes offers a high degree of flexibility.

Main memory for the system is expandable to 192 Mbytes. It features up to 4 Gbytes of virtual addressing space per process. A synchronous 64-bit-wide channel system bus, called the Gigabus, provides a system bandwidth of 320 Mbytes/s.



Using a tightly coupled multiprocessor architecture and advanced semiconductor technology, the System 6400's power comes in a compact package. The system packs a single 6-Mips CPU on three circuit boards using ECL and LSI proprietary gate arrays.

This message-based architecture permits the addition of CPUs without modification to user software or the operating system. The design of the Gigabus ensures expandability to accommodate new technologies and prevent system obsolescence.

Three multiuser, multiprocess operating systems—Embos, Unix BSD 4.3 and Unix System V.2—run on the system concurrently. A variety of programming languages are supported, including Fortran, C, Pascal, Cobol and Mainsail.

Housed in two 32- × 59-in. cabinets, a fully configured 12-CPU system is priced at approximately $3 million.

Elxsi, 2334 Lundy Pl, San Jose, CA 95131. **Circle 100**

Stand-alone vector processors deliver high-speed array processing and offer extensive expansion options

Two budget vector processors, the Maxim/32 and Maxim/64, offer scientific researchers high levels of multiprocessing power and multifunctionality in stand-alone packages. They combine the VMS-based MicroVAX II with the MAP (Modern Array Processors) 32- and 64-bit array processors supported by MAP Fortran cross compilers from CSPI.

Both vector processors are easily expandable to accommodate both single-user and multiuser environments. Their flexible architecture supports expandable memory and disk storage devices. A single-stream compiler automatically compiles Fortran source code programs for high-speed execution in the array-processing module.

The Maxim/32 is based on CSPI's Mini-MAP family. It couples a MicroVAX II general-purpose module with an array-processing module that computers with 32-bit single-precision accuracy. The basic configuration offers a 5-Mbyte physical CPU memory and an internal 1 Mbyte of data memory. A 71-Mbyte high-performance disk and a 91-Mbyte cartridge tape for program backup provide additional storage. Development software and the Fortran compiler is included. Up to four array processor modules can be combined for multitasking environments.

The Maxim/64 computes with 64-bit double-precision accuracy. Its basic configuration consists of a 5-Mbyte memory for the 32-bit CPU and a 16-Mbyte internal data memory for the 64-bit array processor. Disk and cartridge tape storage are the same as for the Maxim/32.

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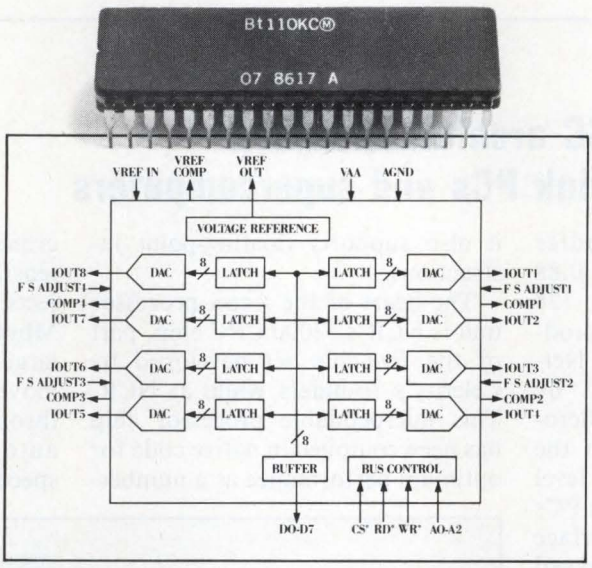

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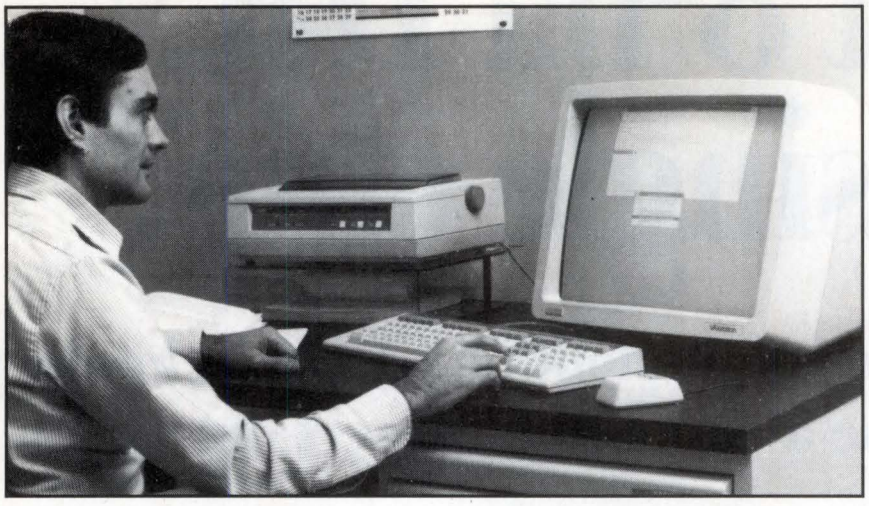


Both systems provide extensive expansion options for CPU and array processor memory. CPU memory expands to 9 Mbytes on both units. The Maxim/32 array processor data memory can be extended up to 12 Mbytes and the Maxim/64 up to 64 Mbytes. Disk capacities for both units range up to 1 Gbyte. A scientific software subroutine library and extensive networking capabilities are also available.

Prices for the systems start at $65,000 for the Maxim/32 and at $165,000 for the Maxim/64.

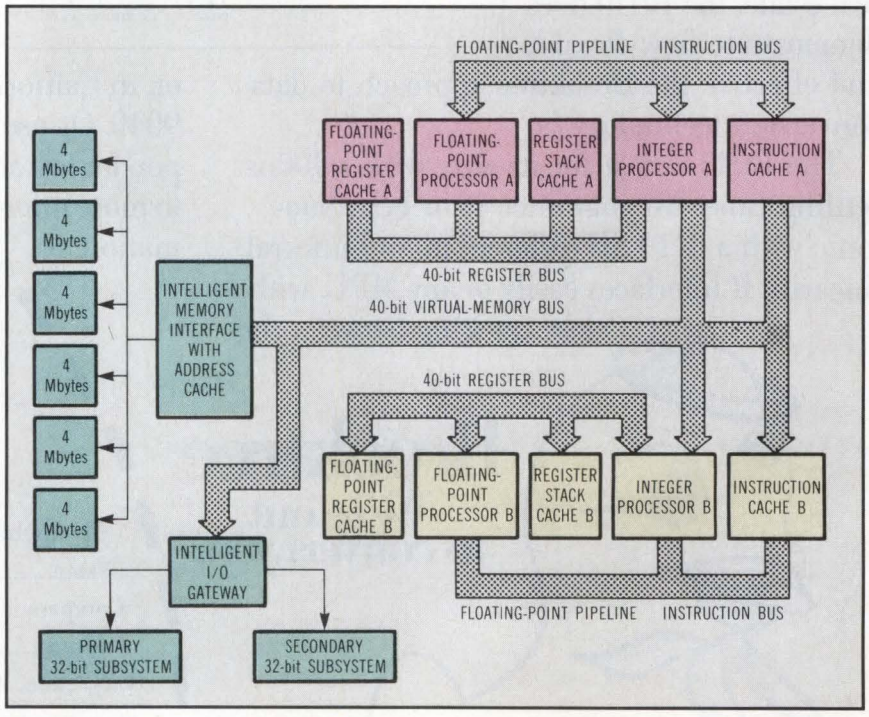
CSPI, 40 Linnell Circle, Billerica, MA 01821. **Circle 101**

Unix-based CAE RISC architectures and software products link PCs and supercomputers

The C1260 superminicomputer boasts an execution rate of 0.88 MFlops and supports up to 128 users. Using two software products—PC-Interface and the Network File System developed by Locus Computing and Sun Microsystems, respectively—users of the C1260, C1230 and the lower level C1200 can share data with both PCs and supercomputers. PC-Interface enables Celerity's Unix-based systems to communicate with IBM PCs, while the Network File System exchanges files in a distributed environment between different vendors' equipment.

Celerity's RISC-based architecture is geared to CAE and scientific-modeling applications and all of the models feature a proprietary 32-bit Accel processor unit and floating-point coprocessor. With more than 150 commands, as compared to the 30 to 35 found in some RISC-based systems, the computer can maintain the enhanced execution speeds of a reduced instruction set without limiting the processor to too few commands and thus sacrificing function. A three-stage pipeline architecture with delayed jumps provides a basic system time as low as 100 ns. Unlike other RISC machines, it also supports floating-point instructions.

The heart of the Accel processor unit is NCR's 32000 CPC chip, part of the five-chip set developed by Celerity's founders while at NCR. This microcodable processor chip has been compiled in native code for optimum performance as a number-crunching engine for compute-intensive design and research projects. The architecture and the 24 Mbytes of physical memory support large applications programs. The movement of data and instructions through four or more separate and autonomous 32-bit data paths speeds computation.



All Celerity models support I/O-intensive applications, such as those requiring frequent access to a large data base. The C1230 has 23 I/O slots on two I/O buses and can support 64 simultaneous on-line users, with up to 4,096 Unix processes.

Interfaces include Centronics parallel, IEEE 488 and DR-11/W for use with high-performance graphics stations, laser printers and electrostatic plotters.

In addition, 4260 and 4230 disk drives allow system configuration with as much as 44 Gbytes of on-line disk storage.

The Accel floating-point extended arithmetic unit, a 64-bit coprocessor that handles mathematically complex portions of programs to speed execution, supports all floating-point operations. The model C1260 system features two independent Accel processors and two floating-point processors.

Celerity uses a native and complete implementation of Unix 4.2 BSD for all of its systems.

Functional system configurations for these superminicomputer design systems are priced at $75,000 for the C1230 and $110,000 for the dual-processing C1260. The PC-Interface (initial 32-user license) and the Network File System are priced at $2,500 per installation.

Celerity Computing, 9692 Via Excelencia, San Diego, CA 92126

Circle 102

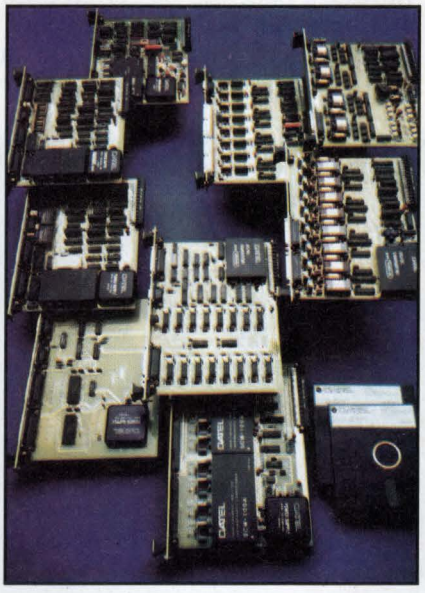
Family of data acquisition and control boards serves VMEbus

Entering the VMEbus arena for the first time, Datel has introduced a complete line of compatible analog and digital I/O boards. The DMVE line is intended to provide complete data-acquisition solutions for VMEbus-based systems through standard and semicustom board-level products that cover a wide range of functions and include industrial-grade A-D, D-A, digital I/O and analog multiplexer boards with software support.

Two of the A-D models, designated the DVME-611 and DVME-612, support 32 single-ended or 16 differential analog inputs. Both boards feature an expansion connector providing up to 256 channels using the DVME-64x series of multiplexer boards. Product-line versatility is increased using Functional Data Acquisition Cells. These replaceable cells provide four versions of each model with A-D resolution and conversion rate pairs of 12 bits/20 μs, 12 bits/4 μs, 14 bits/35 μs and 16 bits/400 ms.

To generate interrupts at the end of conversion and at the end of scans, A-D conversions are programmable in single-channel, single-channel continuous, sequential and externally triggered sequential modes. With the 4-μs conversion rate A-D version, the DVME-611/612 can reach throughput rates of of greater than 160 kHz.

Besides its versatility, the DVME family offers high-voltage isolation.



Representative of this capability is the DVME-602. Serving industrial applications demanding isolated inputs for dc or slowly varying signals, this board provides 1,000-V peak isolation as well as signal conditioning of thermocouples and low- or high-level signals. Isolated analog input signals are converted to 12-bit plus sign data at conversion rates of 30 samples/s. On-board electronics provide thermocouple linearization of J-, K-, T-, S-, B-, E- and R-type thermocouples, watchdog timer and local cold junction compensation.

On the D-A side, the DVME-624 is a fully isolated, four-channel D-A converter board with 12 bits of resolution. Each channel output can be configured as 0 to 5 V, 0 to 10 V, $\pm$2.5 V, $\pm$5 V, or $\pm$10 V dc and can support a 4- to 20-mA current-loop option. Channel-to-channel and channel-to-bus isolation is guaranteed up to 300 vrms. The four versions of the board provide settling times of either 6 μs or 30 μs.

For eight-channel operation, the DVME-628 also provides 12-bit resolution and a 6-μs settling time. It can be configured for the same five voltage outputs as the DVME-624.

In digital I/O, the DVME-660 features 48 software programmable TTL-level channels to VMEbus systems and is plug-compatible to Opto-22 and Gordos I/O modules.

Three multiplexer boards complete the Datel family. The DVME-641 is a high-level analog multiplexer board with 32 single-ended or 16 differential input channels. It features an on-board dc-to-dc converter that provides $\pm$15 V dc from the VMEbus +5-V dc power supply. An eight-channel analog multiplexer board, the DVME-643 delivers 1,000-V peak, isolation and signal conditioning for thermocouple, low- or high-level signals. The third multiplexer board, the DVME-645, consists of 16 single-ended or eight differential analog input channels, with input data acquired simultaneously by 10 sample-hold amplifiers.

Prices range from $695 to $1,595.

Datel, 11 Cabot Blvd, Mansfield, MA 02048. **Circle 103**

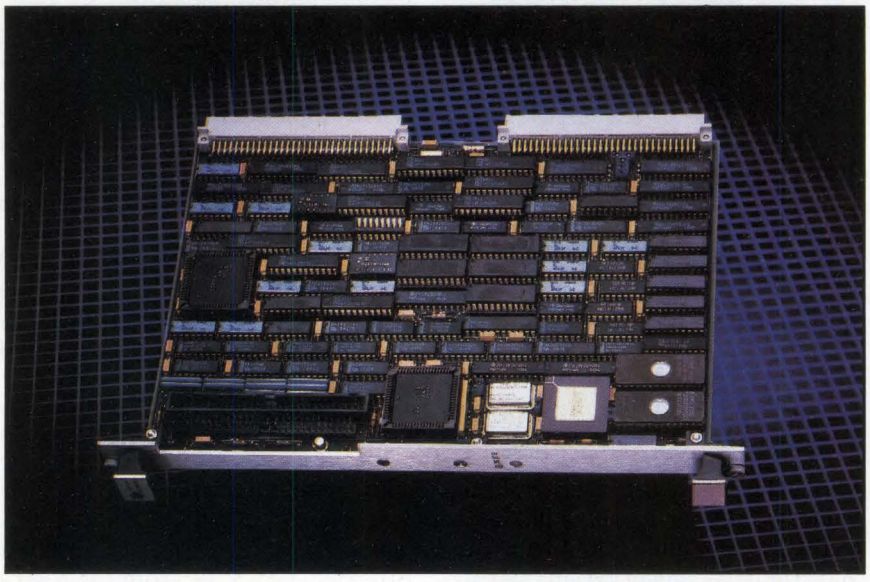
Disk controller pushes VMEbus throughput close to speed limit

Cheetah, a high-performance storage module device (SMD) disk controller from Interphase increases all existing VMEbus throughput by a factor of three. Interphase director of marketing Tom Kent says that Cheetah boosts DMA throughput to 30 Mbytes/s, while present VMEbus controllers have been limited to between 5 and 10 Mbytes/s.

This drastic rise in throughput capability approaches the theoretical VMEbus bandwidth of 40 Mbytes and results from development of the proprietary Buspacket interface, a VMEbus architecture used for the first time on Cheetah. Buspacket decouples bus activity from other on-board controller activity through the use of high-speed, 256-word, bus first-in, first-out (FIFO) buffers and an asynchronous state machine that connects to the VME address bus and controls VMEbus signaling.

Additionally, Cheetah uses a 128-kbyte pool of dynamically allocated RAM buffers instead of the 16-kbyte buffer used in the company's earlier model controllers. This expanded buffer permits multiple data track storage and improved use of the company's intelligent caching capability.

The interface preformats packets of data in the FIFOs before the bus is accessed. These 15-ns FIFOs, located between the RAM buffer and VME data bus, are emptied at 30 Mbytes/s once the bus is accessed and released for other activities. A Busmaster interface for CPU data and a Busslave interface for buffer data connect to the VME data bus.



Multitasking virtual buffer architecture, controlled by a 68000 microprocessor, provides zero latency read/write operation. It permits simultaneous data movement between Cheetah and the bus and between Cheetah and system peripherals. The microprocessor also manages the pool of data buffers by allocating and deallocating those buffers for various system processes. This eliminates both read overruns and write underruns.

Unlike traditional controllers, Cheetah begins reading data as soon as the head lands on the track. It then immediately transfers all sectors of interest regardless of their order on the disk. The controller thereby never needs more than one disk revolution to transfer an entire data track.

Even after requested sectors of the disk are read and transferred, the controller continues to read and cache sectors. Then, if the host later requests that data, the controller can transfer the data from cache without accessing the disk and without block interleaving by the operating system.

Technically designated the V/SMD 4200, Cheetah operates with many system variables and programmable system parameters. These incude burst rates and multiple interrupt vectors as well as all variable bus configurations. Price for the single VME double-height V/SMD controller is $2,350.

Interphase, 2925 Merrell Rd, Dallas, TX 75229. **Circle 104**

RISC architecture cuts overhead and boosts throughput

Serving both business and technical applications, two reduced-instruction-set computers (RISC) mark the beginning of a new line from Hewlett-Packard. Called the HP 3000 Series 930 and 950, the computers are fully compatible with earlier HP 3000 models, yet offer system throughput up to three times greater.

The source of this performance enhancement is the company's HP Precision Architecture, based upon a RISC design. Implementing computer instructions directly in the hardware, HP Precision Architecture eliminates the system overhead associated with the microcoded instructions of conventional computers. The architecture can be implemented in a number of technol-

ogies (initially TTL and NMOS-III) and supports VLSI design.

The first unit in the line, the Series 930, is a 4.5-Mips processor that supports up to 24 Mbytes of main memory. An optional floating-point coprocessor extends system performance for computation-intensive operations. Housed in a compact, two-bay cabinet, the unit requires minimal power and cooling.

For higher performance operation, the Series 950 is designed around a 6.7-Mips VLSI processor. It supports 64 Mbytes of main memory and delivers approximately three times the throughput of the older Series 68. The company has achieved this performance level by integrating a 1-micron NMOS-III process into a dense VLSI technology developed for processor designs. The entire processor is contained on a single chip.

Both systems employ HP Advancenet, the company's networking architecture that is compatible with IBM systems and the International Standards Organization's Open Systems Interconnection standards.

A basic Series 930 system with 16 Mbytes of memory, two I/O channels, LAN channel, dual-access data base, system dictionary and operating software sells for $225,000.

The Series 950, available in 1987, will cost between $300,000 and $350,000.

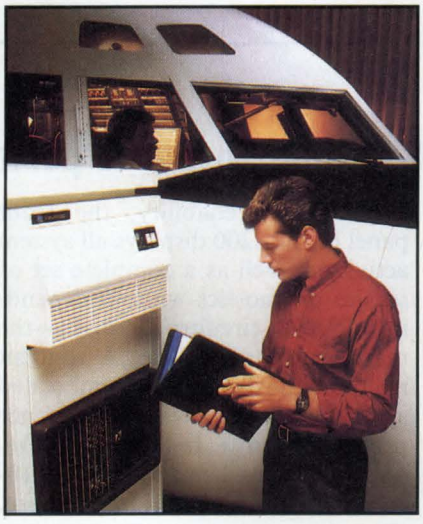
Hewlett-Packard, 1820 Embarcadero Rd, Palo Alto, CA 94303. **Circle 105**

Expandable supermicro family serves wide range of applications

Bringing an easily expandable design to Unix-based, 32-bit computer systems, the MCX family of supermicrocomputers serves applications ranging from CAD to aerospace projects to scientific labs. The computer family includes four models based on the 16.7-MHz MC68020 processor with multiprocessing options.

The line is built around the Harris Supermicrocomputer Unix (HX-/UX), which is based on both AT&T System V and Berkeley 4.2 BSD versions. The line incorporates an enhanced Multibus I/O system, which doubles the traditional Multibus I/O bandwidth to up to 6 Mbytes/s. By separating the memory bus from Multibus communications through a hardware adapter specially designed for DMA transfers, I/O doesn't inhibit CPU activity.

The microcomputers include 32 Mbytes of main memory, 256 Mbytes of physical address space and 4 Gbytes of virtual address space. An 8-kbyte cache memory is added along with three separate buses for memory, I/O and real-time data acquisition, and an integrated MC68881 floating-point coprocessor. For extensive arithmetic calculations, an optional custom-designed floating-point accelerator boosts each processor's performance to 3.6 Mips.



The MCX-3 Model 40 is an entry-level unit that supports 12 users and offers four expansion slots. The MCX-3 Model 60 can operate as a multiprocessor with two processors and has 12 expansion slots. For more computational-intensive operations, the MCX-5 Model 60 can be configured with two processors and a range of peripherals. The top of the line, the MCX-5 Model 70, supports up to 64 users and accommodates up to four processors. Prices range from $18,700 to $73,000.

Harris, Computer Systems Div, 2101 W Cypress Creek Rd, Ft Lauderdale, FL 33309. **Circle 106**

Two mid-range processors improve performance using innovative VLSI CMOS architecture

Designated Models 3620 and 3650, two mid-range systems complement the entry-level 3610AE. Together, they replace all but the high-end Symbolics Model 3675. The 3620 offers a 20 percent increase in processing power over the older 3640 while occupying one-quarter the space.

Measuring just 17.5 × 8.5 × 25 in., this entry-level software development system contains a processor, I/O controllers, a 190-Mbyte disk and 4 Mbytes of main memory. An Ethernet interface, expansion slots for three additional memory boards and a monochrome console with keyboard and mouse are also included. Options include 16 Mbytes of main memory, an additional 190-Mbyte disk, floating-point accelerator and varied peripherals.

The second mid-range unit, the 3650, adds a 40 percent performance punch to the capability of the older 3670. Standard equipment includes a 368-Mbyte disk, an Ethernet interface and up to 32 Mbytes of main memory as well as a second 368-Mbyte disk. For color graphics applications, the computer offers an optional high-resolution

color console with keyboard and mouse and 8- and 24-bit color capabilities with CAD buffer and frame grabber graphics systems.

Both the 3620 and 3650 use an innovative 36-bit tagged architecture that, unlike the 32-bit design commonly seen, uses an extra 4 bits to provide information about the data to be processed. This architecture optimizes performance in Lisp applications by providing run-time data typing, dynamic storage allocation, dynamic linking, multitasking in a single address space and object-oriented programming.

The systems also come stocked with the company's Geneva software environment that provides common Lisp language plus extension, utilities and additional components required for large-scale software development projects. Users are able to write programs that are extensions of the environment itself, while easing the reallocation of activities such as editing, debugging and evaluating Lisp forms.

Price with console for a basic 3620 is $49,900; a standard-configuration 3650 is $65,900.

Symbolics, 4 New England Tech Ctr, 555 Virginia Rd, Concord, MA 01742. **Circle 107**

Supermini borrows RISC design to boost performance

In what purports to be third-generation reduced-instruction-set computer (RISC) technology, Ridge Computers offers the 3200 Model 90 system performing at levels equivalent to or better than VAX 8600 superminicomputer for one-tenth to one-fifth the cost. Anchoring the high end of the company's product line, the Model 90 offers this strong computational performance while incorporating additional reliability features such as a microprocessor-based service processor to manage all remote diagnostics. With remote diagnostics, every service function can be provided off-site.

To enhance reliability, the front panel of the 3200 displays all system activity as well as a complete set of service diagnostics without depending on I/O circuitry or disks—the major cause of failure. A resident microdiagnostic self-test embedded as part of the power-on sequence protects against failures that frequently occur when a system is turned on or off. An additional feature, the system boot software that resides in an on-board erasable programmable read-only memory, further reduces reliance on I/O or disk.

The 3200 can support more than 100 users of workstations from Sun Microsystems, Digital Equipment Corp and Apollo Computer as well as more than 100 users of IBM PC ATs and RT PCs and users of Apple MacIntoshes running on the Appletalk network. Primarily slated as a server in engineering and scientific work groups, this computer processes single-precision calculations at 4.3 MWhetstones/s. Integer applications, such as compilation, run in excess of 5 million instructions/s. System I/O transfer rate reaches 18.3 Mbytes/s in burst mode. With 128 Mbytes of main memory, I/O speeds of up to 2.4 Mbytes/s per disk can be achieved using the

embedded SMD I/O interface protocol.

Applications software compatible with Ridge's other systems is available on the 3200. This includes packages for mechanical and electrical engineering such as Swanson Analysis Systems' Ansys program and MacNeal-Schwendler's MSC/Nastran for finite-element analysis.

A basic system with 4 Mbytes of main memory, a 78-Mbyte hard disk, eight RS-232 ports and ¼-in. tape cartridge backup, is priced at $36,650.

Ridge Computers, 2451 Mission College Blvd, Santa Clara, CA 95054. **Circle 108**

Apollo expands DN570/580 workstations with turbo package

The mid-range DN570 Turbo workstation for computational-intensive two-dimensional graphics applications and the high-end DN580 Turbo workstation for real-time three-dimensional graphics applications extend the performance of the Apollo DN5xxx series of color graphics workstations. For existing DN570/580 workstation users, an add-on Turbo package is offered.

The new Turbo workstations incorporate an optimized 68020 32-bit microprocessor with 16 kbytes of physical cache memory and a 68881 floating-point coprocessor. In addition, the workstations support up to 16 Mbytes of error-checking and correcting memory and 2 Gbytes of virtual address space for each concurrent process.

A high-performance floating-point accelerator option complementing the 68881-based system improves performance by two to six times over the standard 68881 floating-point coprocessor, according to the company.

The Turbo workstations outperform conventional workstations because of their ability to transform and clip 2-D vectors by 50 percent to 150,000 vectors/s and 3-D vectors by 30 percent to 130,000 vectors/s. Overall, the higher performance Turbo workstations run graphics-intensive applications up to 2.2 times faster than the original DN570/580 workstations. Apollo boldly claims the Turbo workstations are eight times faster than DEC's VAXstation II/GPX workstation and 2.2 to three times faster than the 2-D and 3-D performance of Sun's 3/200 workstation series.

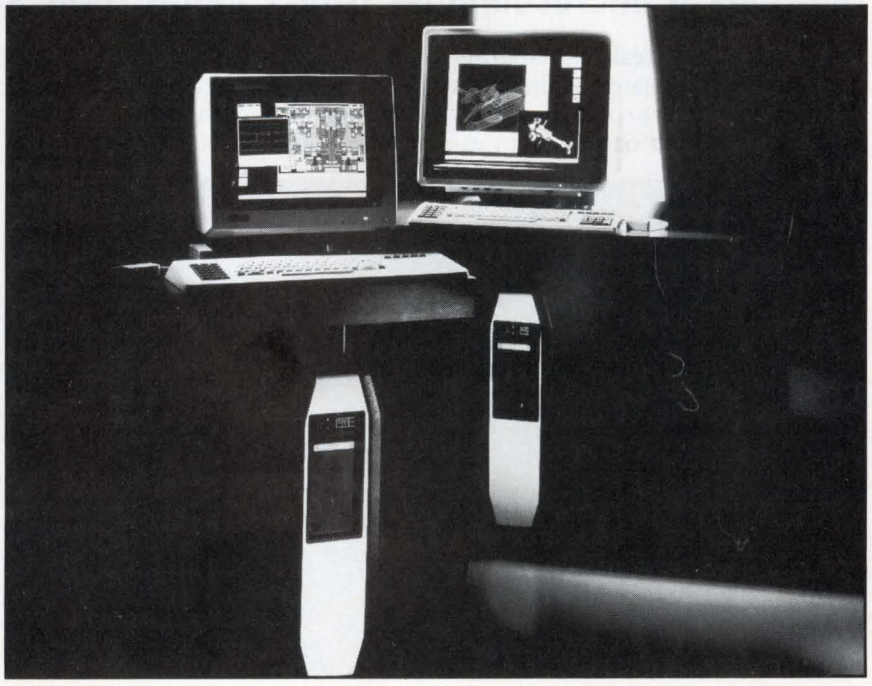
The Turbo 580 has a high-resolution display with a 19-in., 60-Hz noninterlaced 1,024- × 800-pixel, bit-mapped color monitor. Its drawing processor delivers 150,000 2-D transformed and clipped vectors/s and eight planes of display memory. The Turbo 570 features either a 15-in. nonglare or a 19-in. flicker-free display, both at 60 Hz noninterlaced, 1,024- × 800-pixel bit-mapped. Its drawing capability is 40,000 2-D transformed and clipped vectors/s and eight planes of display memory.

A floating-point accelerator option uses the Weitek 1164/1165 floating-point chip set in a heavily microcoded environment. This hikes performance to 2,200 single-precision Whetstones and over 1,800 double-precision Whetstones. For applications that include vector arithmetic, such as finite-element analysis and modeling, its instruction set includes vector mode instructions resulting in close to a sevenfold gain in performance.

The Turbo 570/580 workstations are compatible with other DN5xxx workstations and run more than 700 applications software packages currently available on Apollo's Domain system product family.

Both workstations are available with 8, 12 or 16 Mbytes of main memory. Price range from $43,900 for the DN570 Turbo with 8 Mybtes of main memory to $66,900 for the DN580 Turbo with 16 Mbytes of main memory. The Turbo performance package is available with 8, 12 and 16 Mbytes of main memory at prices starting at $12,500. The floating-point accelerator option is priced at $5,900.

Apollo Computer, 330 Billerica Rd, Chelmsford, MA 01824. **Circle 109**



Supermini computer packs power onto single board

The Eclipse MV/7800 is built around a six-chip set. Using VLSI technology, it manages to pack its CPU, floating-point processor, remote diagnostics processor, time-of-day clock, 2 to 4 Mbytes of error-checking memory, writable control store, and support for data channel and burst multiplexer channel buses onto a single 15- × 15-in. board.

The chip set consists of four NMOS circuits, a CMOS gate array and an ECL gate array. Its standard floating-point unit speeds single- and double-precision arithmetic operations to a rate of 1,067 single-precision Whetstones and 756 double-precision kWhetstones.

If needed, the system can accommodate up to 14 Mbytes of main memory. With 14 I/O slots, it supports up to 9.4 Gbytes of disk storage and up to 128 peripherals.

Compatible with the rest of Data General's 32-bit line and its 16-bit models, the MV/7800 offers three different operating systems—the Advanced Operating System/Virtual Storage (AOS/VS) for time-sharing applications, AOS/Distributed Virtual Storage (AOS/DVS) for distributed systems and DG/US for Unix environments.

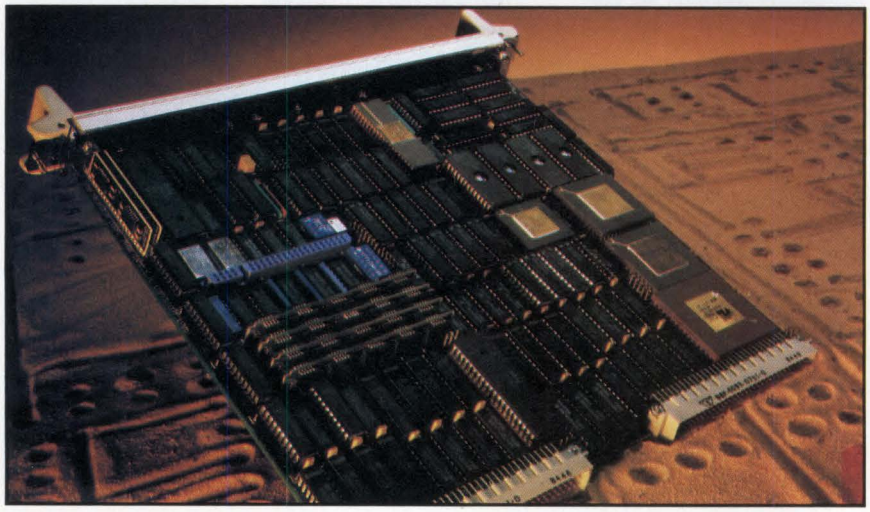
A 2-Mbyte rack-mount Eclipse MV/7800 model with power supply, 16-slot chassis and AOS/VS is priced at $19,050.

Data General, 4400 Computer Dr, Westboro, MA 01580. **Circle 110**

Multibus II microcomputer offers 32-bit DMA at high speed

Designed for both real-time environments and sophisticated applications demanding interprocessor communications and broad memory expansion, a multiprocessing engine from Heurikon serves high-speed Multibus II applications.

The HK68/M220 delivers its performance through a 25-MHz 68020 MPU coupled with 4-Mbyte on-board dynamic RAM with parity, 256-kbyte EPROM and 128-byte nonvolatile RAM for user functions. Two RS-232 serial ports and an ANSI-compatible SCSI handle communcations.



Other features include a 16-bit iSBX connector, iLBX II memory-expansion bus, on-card 4-channel DMA with 32-bit data path clocked at CPU speed and three 16-bit counter/timers. An optional 68851 paged memory-management unit aids Unix operation, and an optional on-board 68881 floating-point coprocessor improves performance in research applications.

The board's 32-bit data path, 32-bit addressing and full message passing provide complete compatibility

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with a broad range of peripheral boards for varied applications.

Operating system support includes Unisoft's Uniplus+, Unix V.2 compatibility, Hunter & Ready's VRTX Real-Time Executive and Microware's OS-9.

Heurikon also offers a Unix-to-VRTX development system called Link/X for real-time development and test. A 4-Mbyte board with a 12.5-MHz processor is priced at $4,195.

Heurikon, 3201 Latham Dr, Madison, WI 53713. **Circle 111**

LAN controller converts PC to industrial workstation

The MAPware Series 1200 conforms to the requirements of all seven layers of the Manufacturing Automation Protocol (MAP) Version 2.1 specification. And when MAP 3.0 becomes effective, the board will also support that version.

The board lets an IBM PC, PC XT, PC AT or ruggedized PC enter a MAP network and either exchange information or control a small workcell. Up to eight simultaneous connections can be maintained. The controller can call any of eight nodes with eight different types of equipment, put that node on hold and make a connection somewhere else.

Hardware for the Series 1200 is based on the Intel 80186 running at 10 MHz. The board contains 512 kbytes of dynamic RAM and 64 kbytes (upgradable to 256 kbytes) of "boot" PROM. Configuration parameters are stored in 2 kbytes of nonvolatile RAM. A Motorola MC68824 token-bus controller chip executes the MAP media access control function.

Because this board functions with an external modem rather than an internal card, only one slot in the PC case is now needed to maintain the MAP function instead of one slot for the controller and one for the modem. The Series 1200 can be connected to either of two external MAP modems at a distance of up to 16 ft from the PC via standard 37 conductor cable. The modem can be table-top or wall-mounted. One of the modems, a 10-Mbit/s broadband modem, adheres to the IEEE 802.4 standard and operates over a mid-split CATV cable.

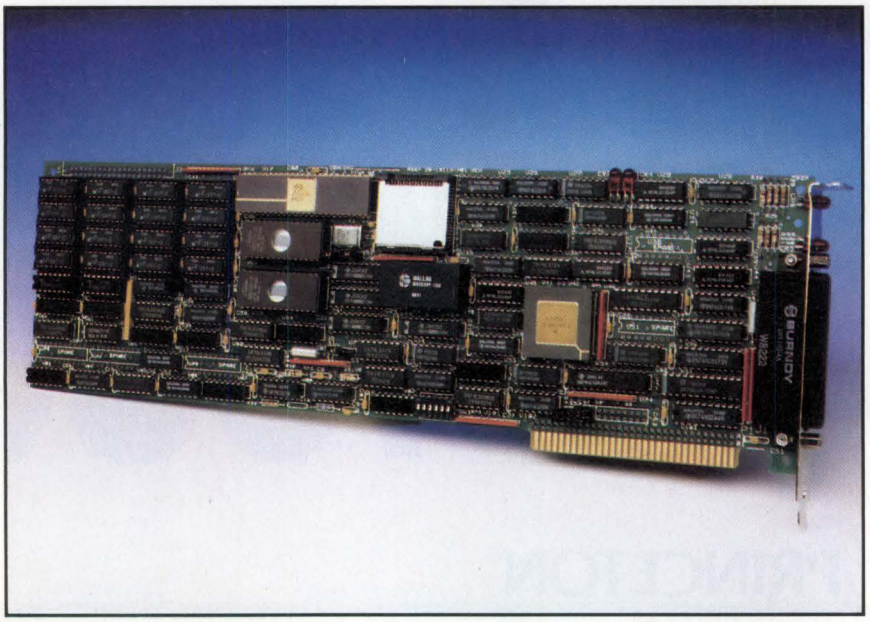
Both frequency agility and modem transmit power levels are software-adjustable. Frequency agility enables the board to set to any of three broadband channels. Addressable power levels are particularly valuable in a factory application. If a signal isn't strong enough or if the environment is exceptionally noisy, the power can be raised.

The controller board can be software-configured as a full MAP node, executing MAP Layers 1 through 7. In particular, applications developers can interface to the Common Application Service Element at Layer 7, to Session at Layer 5, to Transport at Layer 4 and to Data Link at Layer 2. The software is maintained on a 5¼-in. disk and downloaded from the PC executing PC-DOS 3.1 or above. All or part of the software can be used at any of the layers.

The PC bus interface provides 8-bit DMA or program-controlled data transfers. It includes one 8-bit I/O port control register and one 8-bit port status register. The I/O port base address is set by six straps. A 37-pin differential modem interface is IEEE 802.4-compliant for data circuit-terminating equipment and data terminal equipment.

The Series 1200 board sells for $2,695. Deliveries will begin in the first quarter of 1987.

Concord Communications, 397 Williams St, Marlboro, MA 01752. **Circle 112**



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Communications controller supplies high-speed connection

The Xylogics 780 controller, a 16-port asynchronous I/O, serial I/O processor, handles 16 ports transmitting data simultaneously at 9.6 kbits/s or eight ports transmitting simultaneously at 19.2 kbits/s. The controller doubles the number of ports available on a single board, while providing the highest possible transfer speed. On-board intelligence off-loads character-oriented processing from the host.

To achieve these functions within the space constraints of a standard 160- × 233-mm VMEboard, Xylogics merged proprietary chips from its disk/tape controller products for the VMEbus with standard off-the-shelf components. Use of custom large-scale integration makes room for a powerful iAPX-186 processor and 512 kbytes of RAM within the VMEboard.

High performance is obtained by combining the 186 microprocessor with the DMA82258, a 32-channel DMA controller from Intel. This controller off-loads the on-board processor from data input work coming from the 16 ports, leaving it free to handle some of the work previously done in the Unix driver. Because the DMA chip manages the relatively involved translations required by the Unix generic TTY protocol, the system CPU is free to concentrate on the application.

Working under the XyCE realtime multitasking executive, the 10-MHz iAPX-186 controls all board activity and moves data quickly. The Intel DMA chip takes each character from a staging buffer, performs the necessary conversions and returns the data to another part of memory. Xylogics' DMA chip picks the converted data out of memory and puts it onto the VMEbus at transfer data rates of 10 Mbytes/s.

Communications between the host and controller are accomplished by asynchronously passing message packets via a message pipe (a set of separate input and output buffers). This mechanism supports efficient transfer of either single characters or character blocks. Since messages are placed and taken from message queues asynchronously, the host is not required to spin on any hardware bits as part of the host-to-controller communications protocol.

The 780 I/O processor is designed on a single dual-height VME Eurocard that contains drivers and receivers from the RS-232C port. Connection to the host is via two 60-pin ribbon cables. Board price in single quantities is $2,495.

Xylogics, 144 Middlesex Tpk, Burlington, MA 01803. **Circle 113**

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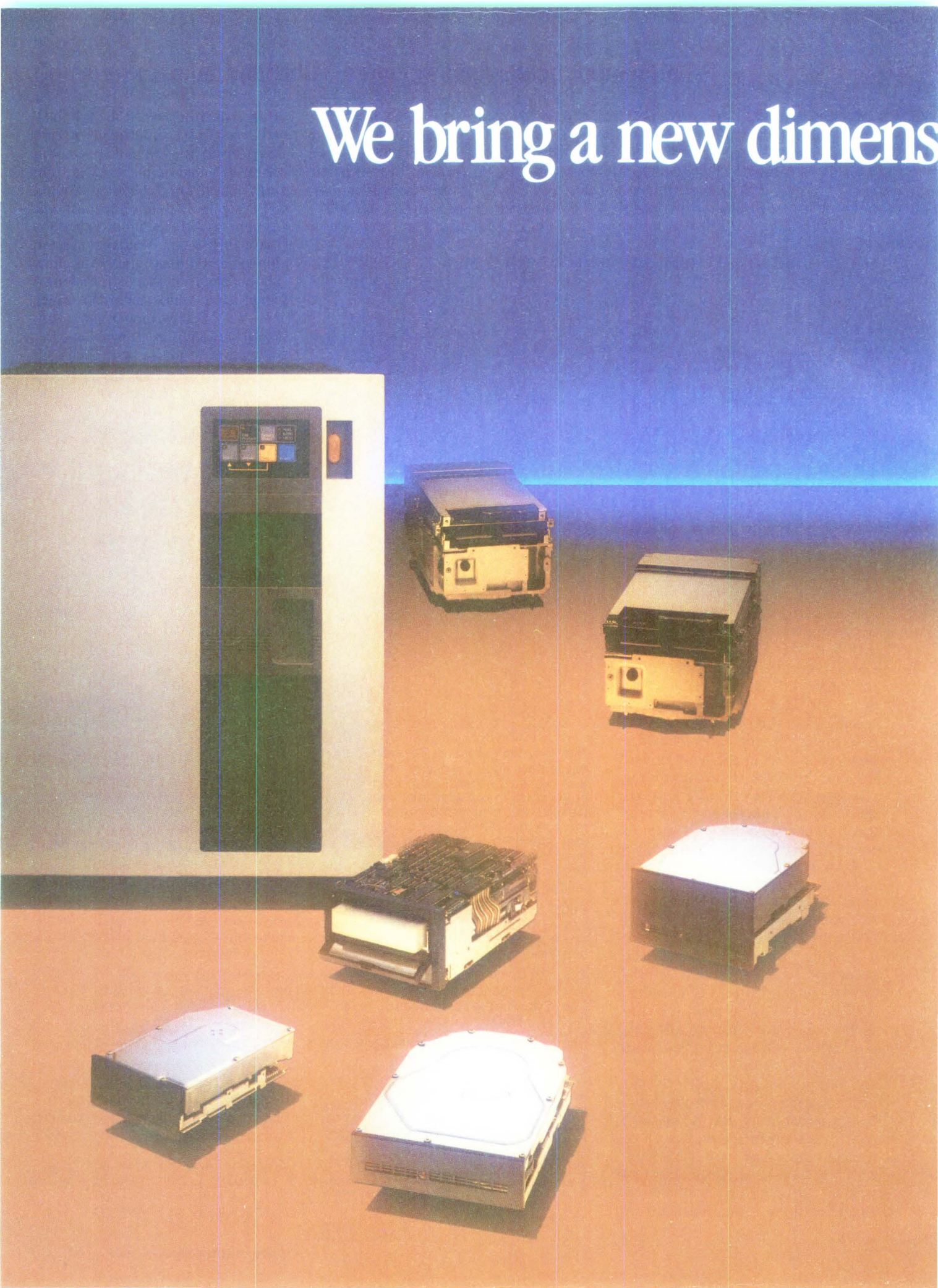

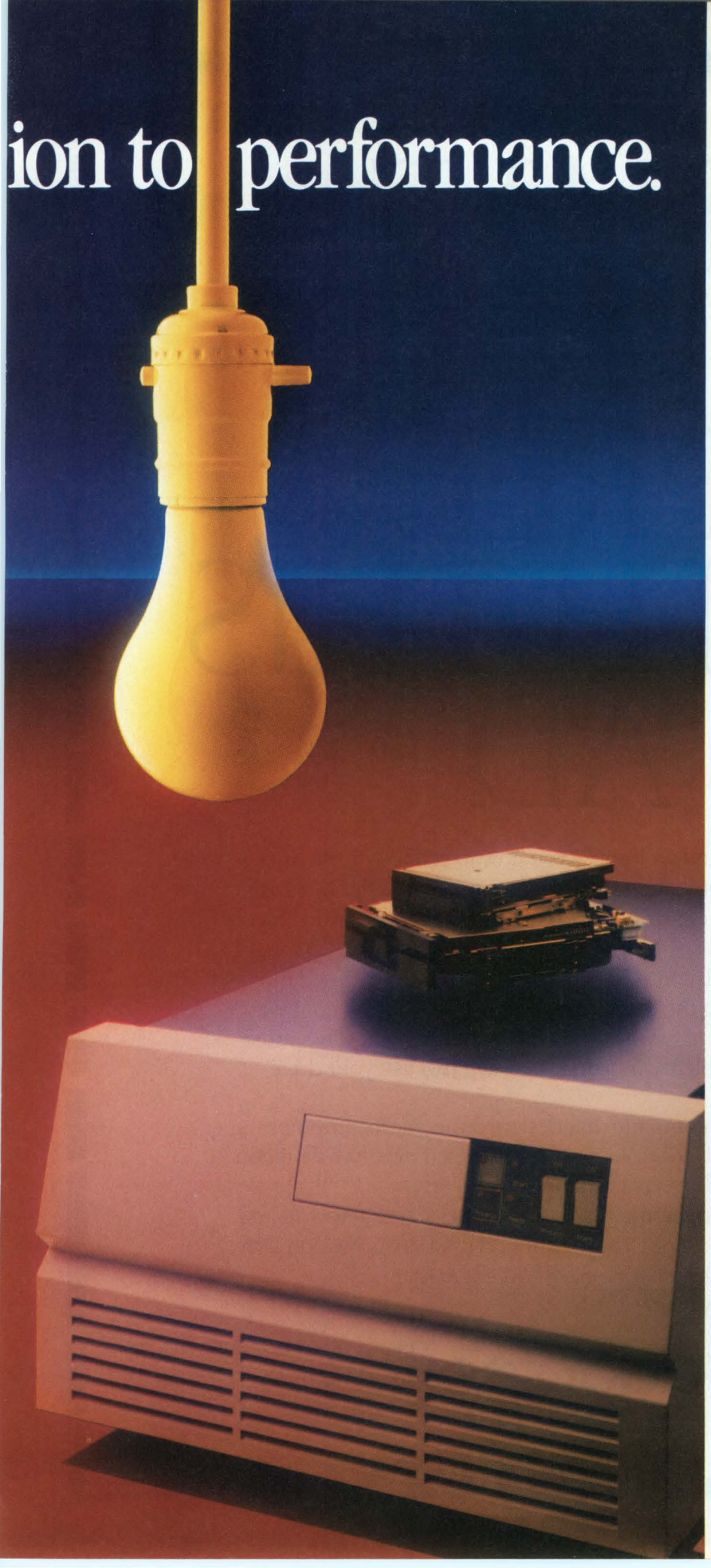

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CIRCLE NO. 39

Advances in CMOS and ECL process technology yield powerhouse ICs

Microprocessors, digital signal processors and programmable logic devices have all gained from progress in CMOS and ECL technology.

Ken Marrin
Senior Editor

The IC industry was reshaped in 1986 by the departure of U.S. semiconductor vendors from the dynamic RAM business and by advances in both CMOS and ECL technology. Japanese competition has forced U.S. semiconductor vendors to refocus their memory efforts on the static RAM area. Advances in CMOS technology have led to the emergence of a robust digital signal processing (DSP) industry, and CMOS has also surpassed TTL and Schottky technologies in several key IC areas.

Advances in CMOS have also allowed vendors of 32-bit microprocessors to break the 20- and even 30-MHz speed barrier, greatly expanding the demand for support ICs. Vendors of semicustom, memory, logic and programmable logic devices are all scrambling to develop CMOS components that can keep up with the higher performance microprocessors.

While CMOS process technology is surpassing bipolar and Schottky technology, improvements in emitter-coupled logic technology are raining on the GaAs parade. Although GaAs technology is still winning hands-down in the laboratory, GaAs process technology is still immature and lags behind silicon technology by about eight years. GaAs should enjoy some success at the SSI/MSI level in emerging industries such as fiberoptics and ISDN, but commercial GaAs LSI viability may be as much as five to 10 years away.

Probably the most dramatic occurrence in the IC industry in 1986 has been the virtual elimination of U.S. vendors from the DRAM market. For the most part, U.S. vendors simply can't compete in commodity markets. DRAM prices are currently protected and artificially inflated in the United States. But in Japan, where the real price is set, the 256-kbit DRAMs are commodity items, and the price of 1-Mbit DRAMs is less than half of their U.S. price.

In January, Motorola (Austin, TX) was still reporting that it would maintain a high-end DRAM effort to drive the process technology for other product lines. Not long thereafter, though, low profitability forced Motorola to abandon that effort. Texas Instruments (Houston, TX) still plans to market a 1-Mbit DRAM, but its introduction has been delayed until 1987. Because of the delay, TI doesn't expect its 1-Mbit DRAM to be a big moneymaker. Like Motorola, TI plans to use its 1-Mbit process to drive the process technology for other product lines. But since TI moved its manufacturing to Japan, the company doesn't legitimately qualify as a U.S. 1-Mbit DRAM supplier.

Major technological issues in the DRAM market have also been resolved in 1986. At the start of the year, vendors were still split on whether NMOS or CMOS technology would dominate and whether planar or trench capacitors would be used.

By mid-1986, however, both issues had been resolved. Although all vendors agreed that CMOS would be the technology of choice for 4-Mbit DRAMs, some initially thought that NMOS DRAMS would be cheaper to produce at the 1-Mbit level because of their smaller die size. But CMOS operating margins have proven to be better than NMOS margins, according to Mark Ellsbury, product marketing manager at Toshiba (Tustin, CA). "Because its margins are better, CMOS is cheaper to produce in spite of its larger die size," says Ellsbury. For that reason, Toshiba, which at first marketed both an NMOS and a CMOS 1-Mbit DRAM, has discontinued its NMOS line. Virtually every other NMOS producer has done the same.

The advantage of CMOS in the long run is lower power, a wider range of operating modes and a lower soft error rate. "In the active mode," explains Ellsbury, "NMOS and CMOS draw comparable power. When in standby, however, because CMOS uses transistors rather than polysilicon resistors as loads, CMOS draws five times less power. Because NMOS has such high standby power consumption, page mode is impractical to implement." CMOS also gives a greater immunity to alpha particles. Where NMOS designs typically spec 1,000 failures per 10^9 hours, Toshiba's CMOS DRAMs spec 10 failures per 10^9 hours.

The other major unresolved issue at the beginning of 1986 was whether planar or trench capacitors would be used. Vendors agreed that the trench design, because it supports a smaller die size, would dominate the 4-Mbit market because it supports a smaller die size. But several vendors were concerned that the trench technology would be difficult to bring to market in time. Their concerns proved to be valid, and vendors such as TI and NEC that used the trench design had to delay their introduction. Because DRAMs using planar capacitors were introduced first, the planar designs will dominate at the 1-Mbit levels. Trench designs will probably win out at the 1-Mbit level, where the higher density makes the smaller die size more critical.

Another major development in the IC industry in 1986 was the advance of CMOS technology at the expense of bipolar TTL and Advanced Schottky technology. No longer a technology that sacrifices speed for low power and high integration, CMOS has displaced bipolar technology in some areas and is about to displace it in others.

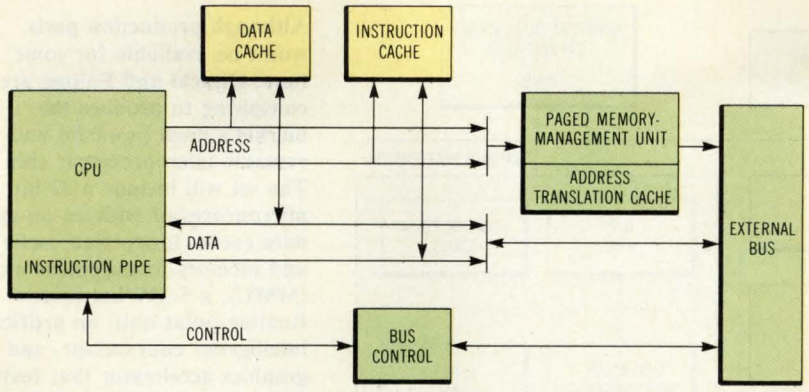
Because of its low power and high density, CMOS has been displacing bipolar technologies in new processor designs for some time, but in 1986 CMOS surpassed even TTL/Schottky logic in both speed and power. According to Ralph Cognac, product marketing manager for Integrated Device Technology (Santa Clara, CA), IDT's CMOS FCTA family is 40 percent faster and uses one-fourth the power of the Fast Advanced Schottky line from Fairchild (Puyallup, WA), and is three times faster than Fairchild's CMOS Fact line. TI's ACL (Advanced CMOS Logic) family, due out in early 1987, will offer comparable speed.

CMOS is even overcoming its traditional drive limitations. One of the primary drawbacks to CMOS logic was its inability to drive long metal line and multiple loads. IDT's FCTA family, however, will be able to supply up to 64 mA, comparable to that supplied by bipolar logic.

Despite the superior performance of CMOS, the majority of designs are still using Fast parts. "That's because IDT's CMOS family's part selection can't yet match Schottky's," says Cognac. While Fast sports over 100 SSI and MSI functions, IDT's FCTA line supplies only 40. Bob Liggett, Motorola's logic product marketing manager, agrees with Cognac. "Although CMOS is the technology of the future, parts selection is just as important as performance, and CMOS has a way to go in that area."

Fueling the demand for the bulk of the new IC markets in 1986 was the emergence of 20- to 30-MHz CMOS microprocessors, and vendors of CMOS products are scrambling to keep pace with the rapidly escalating speeds of microprocessors.

The highest performance production 32-bit microprocessor announced in 1986 was Motorola's 25-MHz 68020. The Clipper from Fairchild (Palo Alto, CA) is faster at 33 MHz, but strictly speaking,



A cross between a Harvard and a von Neumann microprocessor, the 68030 from Motorola combines three internal buses with a data and instruction cache that optimally allows two operands and an op code to reach the execution unit in parallel. This arrangement provides as much as 80 Mbytes/s of internal bandwidth, and helps the 68030 double the 68020's performance for the same clock speed.

it qualifies as a board-level processor. AT&T (Holmdel, NJ) will be in production in 1987 with a 30-MHz chip set. National Semiconductor (Santa Clara, CA) will follow in late 1987 with a 30-MHz family of its own, and Motorola will follow soon thereafter with the 68030 (production October 1987), which will outperform the 68020 by two to three times for the same clock speed.

Motorola, with its 68030, and AT&T, with its WE 32200, will each try to capitalize at the chip level on some of the innovation that Fairchild has implemented with Clipper at the board level. The 68030 will be the first conventional chip-level microprocessor to implement a Harvard-style architecture. AT&T's WE 32200 will feature the first memory-management unit (MMU) to also include a 4-kbyte, two-way set-associative data cache and a 64-entry fully associative descriptor cache. Both products are software-compatible with their previous generation parts.

The architectural standard for microprocessor-based systems was set last year by Fairchild with its board-level Clipper, which offers high performance by using a modified Harvard-style architecture. In a von Neumann architecture (such as that used by the 68020 and 80386), instructions (op codes) and data (operands) are stored serially in the same address space. Thus, if the combined op code and operand fields consume more than 32 bits of data, the microprocessor makes multiple serial fetches to execute an instruction.

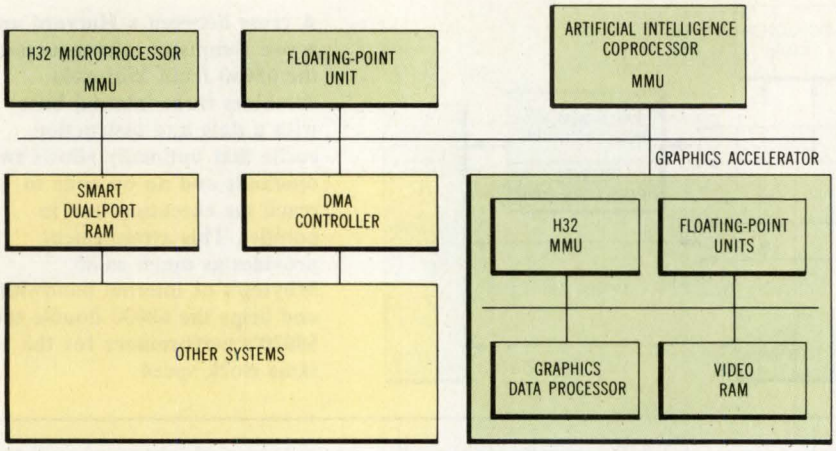
Harvard architectures avoid this bottleneck by storing instructions and data in separate address spaces and providing separate buses for each address space, each of which feeds the execution unit in parallel. Some Harvard architectures, such as those used in DSP applications, may even support two separate data spaces. By supporting separate data and instruction spaces, a Harvard architecture supports simultaneous data and instruction fetches.

Clipper provides a mix between a Harvard and a von Neumann architecture. Program data and instructions are stored in the same main memory space, but once they're fetched from main memory, instructions are stored in Clipper's 4-kbyte instruction cache, and data is stored in the 4-kbyte data cache. Because each cache has a separate path to the CPU, as long as a hit occurs in each cache, data and instructions can be fetched simultaneously. "The two-way set-associative data cache provides a 90 percent hit rate, while the instruction cache provides a 96 percent hit rate," says Gary Baum, Fairchild's Clipper product manager.

The 68030 uses a similar architecture, providing two 256-byte caches and a common MMU. To programs, the 68030 looks like a von Neumann processor, providing a single 32-bit nonmultiplexed bus with access to a single, external, virtual or physical address space. Internally, however, the 68030 uses three separate nonmultiplexed buses and two caches. One cache stores data, while the other stores instructions. A separate bus connects each cache with the execution unit, and a third bus connects the off-chip data/instruction space with the execution unit and instruction pipe. As a result, the 68030 can theoretically fetch two operands and an instruction simultaneously.

Because the data cache is small, its hit rate is only 60 percent (72 percent when the processor is used in the burst mode). But the data cache provides an additional benefit, reducing bus bandwidth utilization from 60 percent (for 68020/68851 MMU combinations) to 50 percent, according to Dean Mosley, Motorola product marketing manager. "If you need a larger data cache, you can bypass the 68030's internal cache and implement your own," says Mosley. "The instruction cache hit rate is about 82 percent for both the 68020 and 68030."

AT&T's WE 32200 chip set is also a take-off on



Although production parts won't be available for some time, Hitachi and Fujitsu are conspiring to produce the market's most powerful and versatile microprocessor chip set. The set will include a 32-bit microprocessor with an on-chip data cache, instruction cache and memory-management unit (MMU), a 5-MWhetstone/s floating-point unit, an artificial intelligence coprocessor, and a graphics accelerator that features the fastest graphics processor on the market.

Fairchild's Clipper, combining a data cache with an MMU. In addition to the microprocessor and the MMU/cache, the AT&T chip set will include a 3.3-MWhetstone/s floating-point unit and the industry's only 32-bit DMA controller. The most significant part is the MMU/data cache, which supports zero-wait-state physical data cache accesses at 30 MHz. The data cache offers an 85 percent hit rate, and the MMU provides a 99.8 percent hit rate. To obtain higher hit rates in both the MMU and data cache, users can gang up to four 32201s.

The 32201 solves one of the most significant problems that system designers will face in the next few years—that of implementing a cost-effective memory subsystem. Current microprocessors support no cache, forcing designers to either accept wait states, use expensive main memory, or use expensive caches. To obtain zero-wait-state performance at 20 MHz, designers must use the fastest, most expensive DRAM (60 ns) available. At 25 MHz, designers must turn to external SRAM cache memory, and at 30 MHz, external caches can't keep up at all.

External caches can't keep pace because bus protocol consumes so much of the access window. If the processor uses a three-clock bus cycle, over two-thirds of the three clock cycles are required to drive the bus, leaving less than one clock cycle to access the cache. If the processor is running at 20 MHz, the designer will have to use the fastest CMOS SRAM. At 30 MHz, the window may be too small for even an ECL SRAM to keep up. "By keeping the cache on-board the MMU, AT&T is able to hide the MMU translation time and implement cache memory that's fast enough to be accessed at 30 MHz," explains Arlon Martin, AT&T product marketing manager.

The newest vendor in the 32-bit microprocessor market is Hitachi (San Jose, CA), which is working with Fujitsu (San Jose, CA) to produce a complete chip set. A 20-MHz version will be available for sampling in late 1987, and a 24-MHz version will be released in 1988. In addition to a microprocessor that includes an on-chip MMU, thirty-two 32-bit registers, and a data and instruction cache, the chip set features a 32-bit DMA controller, a 4- to 5-MWhetstone/s coprocessor and a graphics processor. The graphics controller will provide 10 times the performance of Hitachi's ACRTC graphics controller and display processor (30 ns/pixel drawing vs. 400 to 600 ns/pixel drawing).

The H32 microprocessor will be optimized to run the Tron (The Real Time Operating Nucleus) operating system, which is a full-featured, real-time system that rivals Unix in functionality, says Jim Fleurry, Hitachi product marketing manager. The processor will also run Unix.

The Hitachi/Fujitsu chip set will provide the most comprehensive solution of any chip set. Unless Hitachi is prepared to back its part with better support than Japanese vendors typically provide, however, its chip set won't make much headway in the United States. Like NEC's V Series microprocessors, Hitachi's parts, with the exception of the graphics processor, will probably be used primarily inside the company and in Japan.

Improvements in high-end microprocessor speed have had a significant impact in the programmable logic device market, where vendors have increased their speed significantly to keep pace. PLDs provide the decoder, arbitration, timing control and interface logic necessary to integrate microprocessors into real systems. Presently, there is a gap between the fastest CMOS PLDs and the fastest CMOS microprocessors and logic. CMOS PLDs aren't yet fast enough to replace either CMOS logic or to keep

up with high-speed microprocessors.

"Even at 12 MHz, systems require 15-ns PLDs," says Art Swift, product planning manager for programmable products at Fairchild. "At 20 MHz, systems demand 10-ns PLDs, requiring the fastest Schottky parts, and at 30 MHz, systems require 7 ns, currently available only from ECL PLDs." Fairchild (Portland, ME) plans to introduce 7-ns Schottky PLDs within 12 to 18 months, Swift says. Meanwhile, CMOS PLDs are still laboring at 25 ns.

The same dilemma exists in ECL systems. The fastest available ECL PLDs are presently 6 ns, adequate for low-end ECL applications, but 10K ECL logic offers 1-ns delays and 100K ECL logic offers 750- to 900-ps delays. To match ECL logic, PLD speeds will have to drop to the 3- to 4-ns region. Monolithic Memories Inc (Santa Clara, CA), TI and Fairchild all plan to address the high-end market with 3- to 4-ns ECL PALs within the year.

While CMOS seems destined to replace TTL and Schottky technologies in the logic market, it will have a tougher time in the PLD arena. Bipolar TTL and Advanced Schottky PALs are maintaining a 50 percent speed advantage over the best CMOS, and bipolar speeds are continuing to fall. "By the first half of 1987," says Bob Bailey, TI's product marketing manager, "TTL PALs will reach 10 ns."

"By the time CMOS gets to 10 ns," says Steve Grossman, product marketing manager for Advanced Micro Devices (Sunnyvale, CA), "TTL PALs will be well down the learning curve, and vendors will be able to offer half-power versions that provide the same speed, equivalent power consumption, and lower cost." And bipolar TTL PLDs, says Bailey, will continue to cost half that of CMOS PLDs at the same speed.

One of the most significant trends in the PLD market in 1986 has been an increase in PLD functionality. Having squeezed the highest speed possible out of their devices, vendors are applying their process technology to extending their device's gate equivalence. Some vendors, such as Altera, Cypress and Xilinx, are even looking at the low-end gate array market.

PLD vendors face the problem of extending the device's usable density within the constraints of a rigid AND/OR array that inherently limits flexibility in many applications. Improvements in process technology let vendors pack more product terms (gate equivalents) on a chip, but the rigidity of the architecture often limits how many of those product terms a user can access.

Although the programmable AND/fixed OR architecture used by PLDs works well in decoder and control applications, in many applications it lacks the flexibility needed to efficiently implement random logic. As the density of the AND and OR arrays is increased, the range of functions that can take advantage of that added density decreases. In random logic applications, a PLD's usable gate equivalence may be only a fraction of its theoretical gate equivalence.

To extend the capacity of output cells, vendors are using silicon rather than increasing the array size. Features such as programmable output polarity, registered outputs, buried registers, product sharing, register preload, synchronous reset and asynchronous preset extend a PLD's usable gate equivalence without increasing the array size.

Vendors are also experimenting with different PLD architectures. One of the most popular architectures is actually a variation on the field programmable logic array (FPLA) architecture from Signetics (Sunnyvale, CA), which features both programmable AND arrays and programmable OR arrays. Programmability in the OR array allows product terms (outputs from the AND array) to be shared among outputs.

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Until recently, FPLA architectures have been unpopular because the additional programmable array incurred a performance penalty and made them difficult to understand. However, software tools like Cupl from Data I/O (Redmond, WA) and Abel from the Assisted Technology Division of PCAD (Los Gatos, CA) have made FPLAs as easy to use as PAL-like devices, and improvements in process technology have made their speed competitive.

A compromise between the PAL-like architecture and the FPLA architecture is a product steering architecture, which uses a programmable AND and a fixed OR array. Rather than fixing the number of product terms that are available to each output, however, it allows outputs to access product terms from a common pool.

In spite of the fundamental limitations that the rigid AND/OR architecture imposes on PLDs, several vendors are targeting the low-end gate array market. Altera produces a 2,100-gate equivalent array, MMI and Xilinx (San Jose, CA) have teamed to produce a RAM-based, 1,800-gate equivalent array, and Cypress plans to introduce a 1,200-gate equivalent PLD within the year.

According to David Laws, vice-president of marketing for Altera Semiconductor (Santa Clara, CA), PLD vendors will win designs from low-end gate arrays not only because of their shorter time to market, but also because of their lower cost. "Vendors deemphasize their lower-performance/lower density gate arrays, driving up their cost per gate relative to their higher density arrays."

Altera (second-sourced by Intel) and Xilinx (second-sourced by MMI) have taken different approaches in attacking the low-end gate array market. Altera takes a more conventional approach with its EP1800. Each EP1800 is divided into four quadrants, each of which contains 12 macrocells. Each macrocell, in turn, contains a logic array, selectable register element, and a tri-state I/O buffer. CMOS EPROMs are used to configure logic functions within the device.

Xilinx has taken a more radical approach, employing RAM-based cells that let users change their function on the fly. According to Joel Rosenburg, MMI's strategic marketing manager for logic cell arrays, Xilinx has taken more of a gate array approach. The array consists of 64 configurable PAL-like building blocks, surrounded by 64 configurable I/O blocks. Twelve-thousand bits of RAM are distributed throughout the array in order to provide reconfigurability.

Using RAM gives the Xilinx array more flexibility than a PLD, but when power is removed, the device loses its function. Consequently, the function must be booted during power-up. "A better approach would be to use EEPROM cells in place of RAM," says Steve Grossman, AMD's product manager. "EEPROM memory allows the device to be reconfigured on the fly, but maintain its function on power down."

Another market that's being driven by high-speed microprocessors is the SRAM market. As microprocessor word widths and speeds increase, so does the demand for the high-speed cache, control stores and buffers needed to support them. DSP microprocessors, floating-point processors, bit-slice processors and custom processors will all be heavy users of cache. Randy Chapman, Hitachi product marketing manager, expects most 32-bit microprocessor-based systems to use a minimum of 4 kwords of cache and 64 kwords. Bit-slice systems will use SRAM for their control stores. Dane Elliot, Cypress applications manager, expects bit-slice control stores to range from 2k to 32k words deep and from 30 to 150 bits wide.

The result of an increased focus on the SRAM market has been a rapid reduction in SRAM access times. CMOS SRAM access times for 64-kbit devices have dipped to 25 ns, and Performance Semiconductor (Sunnyvale, CA) claims to be close on a 20-ns, 64-kbit part. IDT plans to be first in production with a high-speed 256-kbit SRAM and expects to have 25-ns parts out in January. Inmos (Colorado Springs, CO) also expects to announce a 256-kbit, 25-ns part by the end of the year. ECL memories are maintaining their speed advantage at 5 to 10 ns, but they offer limited density of between 0.5 and 4 kbits. Hitachi plans to release a 10-ns, 16-kbit part in 1987.

Because of the stiff competition and the fast rate at which the technology is evolving, price erosion is becoming a serious problem in the SRAM market, just as it did in the DRAM market. The result is that slower SRAMs are becoming commodities faster than many vendors had expected. Vendors can demand a premium if they offer the highest speed product, but products only marginally slower (5 to 10 ns), fall off dramatically in price. For example, Vitelic's (San Jose, CA) 8k × 9-bit parts cost $11 for the 35-ns speed grade, but drop to $7.50 for the 45-ns version, $6.50 for the 55-ns version, and $6 for the 70-ns version.

Another way that vendors are carving a niche for themselves is through application-specific RAMs. Several startups have indicated that their initial product offerings serve merely to establish their credibility in the market. Once they've established

credibility with a customer, they work with that customer to identify and develop application-specific parts. The most common application-specific parts include dual-port RAMs for multiprocessor and synchronization applications, ×9 configurations for parity, cache-tag RAMs with fast reset for cache applications, and output enable and separate I/O to relieve bus contention.

Nowhere in the IC industry has the evolution of CMOS process technology had more of an effect in 1986 than in the DSP industry. Hardware signal processing solutions have been available for some time, but they consisted mainly of expensive and difficult-to-configure bit-slice building blocks. High integration and speed has let several vendors implement building block systems on a single chip, though, and inexpensive DSP is now at hand.

In the last year, a dozen DSP microprocessors have been introduced, along with a bevy of bit-slice processors, floating-point processors and application-specific processors. Competition will be stiff, but the availability of easy-to-use inexpensive hardware is opening a wide range of applications.

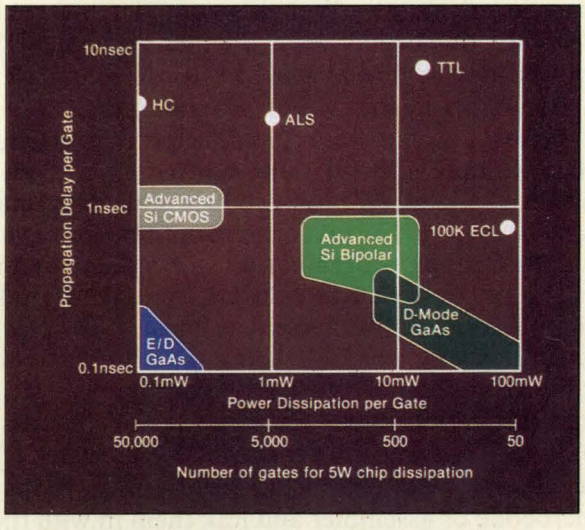
The mainstay of DSP hardware is its ability to perform addition and multiplication in a single clock cycle. This capability is essential in processing analog signals in the digital domain, as the algorithms for doing so (Fast Fourier transforms and various filter algorithms) consist primarily of a repetitive sequence of multiplication and addition operations.

System designers are finding that they can apply this fast math capability to applications other than the processing of analog signals, however. Graphics algorithms, image-processing algorithms, and control algorithms all rely heavily on math operations. In such applications, DSP processors can outperform conventional microprocessors and their math coprocessors by 10 times.

The performance of DSP microprocessors has improved dramatically within the last year. While systems configured from discrete building blocks such as sequencers, multipliers and register files once enjoyed a greater than 10 times performance advantage over DSP microprocessors, that advantage has now been cut to two to three times. Microprocessors such as Motorola's DSP 56000 (not yet available), AT&T's DSP16, Analog Devices' ADSP 2100, and TI's TMS 320C25 can execute core DSP algorithms such as 1,024-pt FFTs in 5 to 7 ms, and specialized processors such as Zoran's VSP can execute the algorithm in 2 to 3 ms. The fastest building block solutions execute the algorithm in 1 ms, but many are much slower.

Building block processors give greater flexibility than microprocessors. Designers can design custom instruction sets and architectures that directly suit their application. However, they're also much harder to use, requiring the designer to program in microcode. Tools such as metassemblers and metasimulators remove some of the programming burden, but DSP microprocessors provide assemblers and even compilers. Datacube (Peabody, MA) has designed a C compiler for the ADSP 2100, Sky Computer (Lowell, MA) has designed a C compiler for the TMS 32010, and most of the major microprocessor vendors have internal compiler efforts.

Even with the improvements that DSP microprocessors have made, however, high cost may still limit their penetration. Though the range of applications is expanding rapidly, the bulk of the applications are still in low-end telecom applications, where low cost is critical. "These applications will demand $5 to $20 parts, and will not be open to the new crop of $100-plus processors," says John Scarisbrick, TI product marketing manager. "The new processors will find some applications in high-end applications such as image processing and graphics, but until they move down the learning curve, they will find high-volume applications scarce." The next high-volume market, predicts Scarisbrick, will be in the consumer, control, and automotive markets, where DSP microprocessors will replace



Although production GaAs hasn't yet fullfilled its potential, as larger production wafers become available, GaAs will eventually offer the highest speed and lowest power of any logic family on the market. That benefit should extend to LSI parts as well within the next five to 10 years.

conventional 8- and 16-bit microprocessors. Again, though, low cost will be the dominant issue.

Another high-interest market for DSP vendors is the high-end floating-point market. Scientific computing, workstation, array processing, image processing, and high-end signal processing applications all benefit from floating point's higher accuracy and dynamic range.

Newcomers to the floating-point market in 1987 will be TI and Bipolar Integrated Technology (Beaverton, OR), which should surpass the performance of existing vendors. TI's 1-micron CMOS parts will include a 40-ns, 32-bit integer registered ALU (74AS8832), a 20-ns, 16-bit expandable sequencer (74AS8835), a 15-ns, 64-word-deep three-port register file (74AS8834), a 50-ns 32 × 32 integer multiplier (74ACT8836), and a 70-ns floating-point, double-precision multiplier (74ACT8837).

The most impressive of the TI parts will be a floating-point multiplier, which will provide 70-ns, double-precision multiplication without requiring pipelining. BIT expects to achieve even higher performance with its floating-point multipliers, which they will fabricate with their high-performance bipolar technology.

While floating-point speed has doubled during the past year, probably the most significant event has been the introduction of C, Pascal and Fortran compilers from Weitek (Sunnyvale, CA) for its floating-point building blocks. For the first time, building block designers don't have to program in microcode. Weitek's compiler has rekindled the controversy over whether high-end DSP applications will be willing to tolerate a compiler's inefficiency to gain ease of programming.

"Most compilers are 20 to 30 percent efficient when compared with hand-crafted microcode," says Julie Cates, Weitek product marketing manager. "However, by performing optimizations such as decomposing programs and storing data and instructions in separate address spaces, Weitek's compilers obtain 40 percent efficiency. By taking advantage of a parallelizing scheduler, which minimizes memory fetches by combining instructions into 64-bit words, efficiency can be increased to 80 to 90 percent." To obtain even greater efficiency, users can code their speed-critical loops in microcode or assembler and link them in with their high-level programs.

Providing higher performance than either building blocks or DSP microprocessors are application-specific chips. By exploiting the inherent parallelism of particular algorithms, and combining multiple arithmetic units on a single chip, application-specific chips can surpass building block performance by 10 times.

By combining eight multipler/accumulators on the same chip, for example, Zoran's FIR (finite impulse response) filter chip is able to process 512- × 512-pixel images in real time.

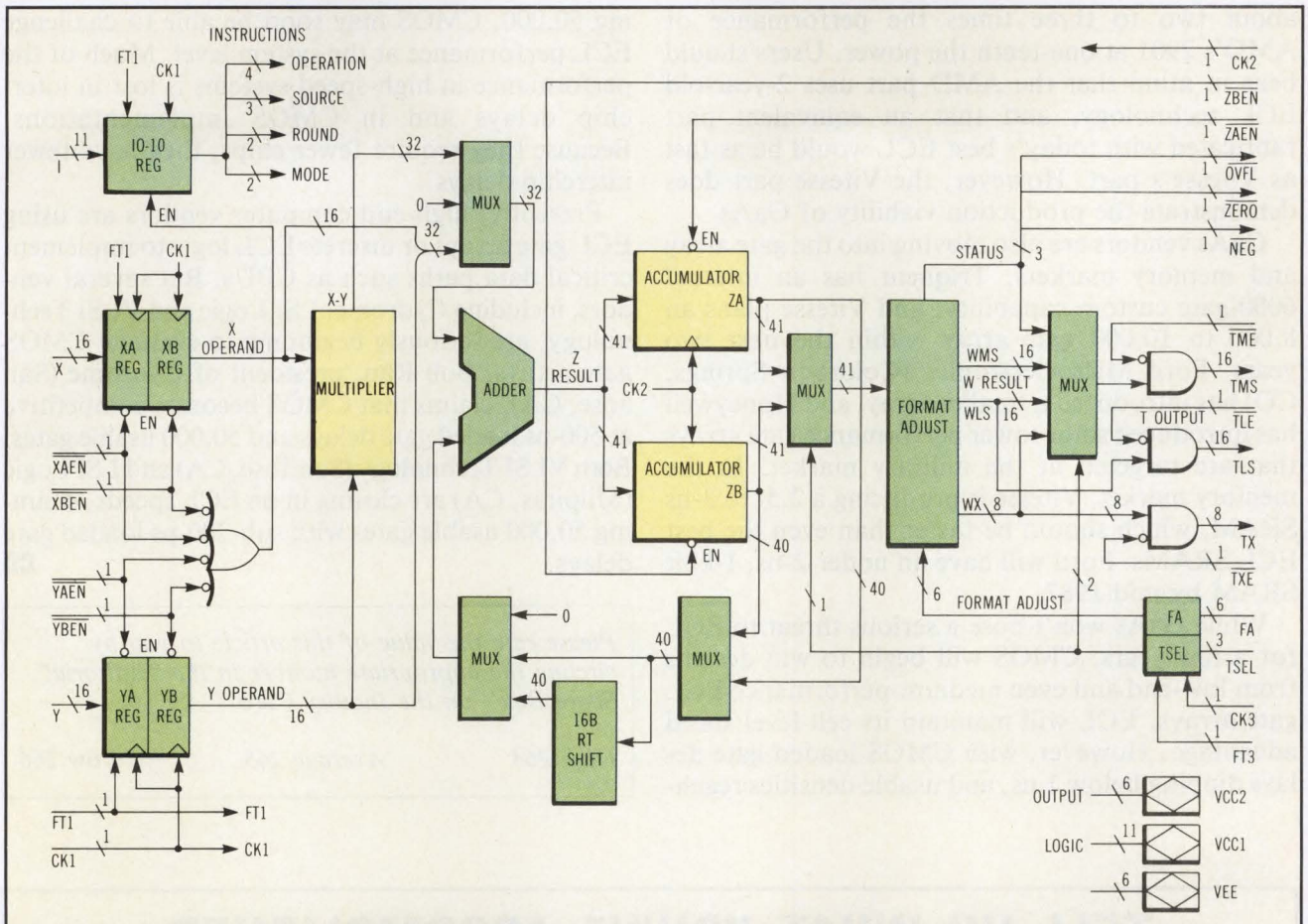
"The highest performance solution of all," explains Pat Narendra, director of DSP products at Honeywell (Colorado Springs, CA) "exloits semi-custom and full custom technology. By using a custom approach, designers can put as many arithmetic units as they like on a chip, and configure the architecture precisely to handle a particular algorithm. Custom chips, as well as algorithm-specific chips, will give DSP microprocessors and building blocks a run for their money."

While CMOS technology made great strides in 1986, bipolar ECL technology didn't stand still. As CMOS exerts more pressure from the low end, vendors of minicomputers, superminicomputers and even workstations are turning to ECL technology to keep pace. Some ECL vendors have responded by supplying densities as high as 10,000 gates and loaded gate delays in the 250-ps region.

The most significant ECL gate array introductions in 1986 came from Motorola (Phoenix, AZ), with its MCA 10000 and BIT, with its CGA70E1H. While the MCA 10000 set new performance and density standards, the BIT array had the best speed/power performance of any array. Offering CMOS-like power dissipation at near-ECL speeds, the BIT process represents the state of the art today in bipolar process technology. Fujitsu and Fairchild are also revamping their processes, and plan to increase their speed/power by four and eight times, respectively, within a year.

In addition to keeping a step ahead of CMOS, ECL advances are delaying the commercial emergence of GaAs. GaAs SSI/MSI logic is two to three times faster, but GaAs LSI performance is poor. In the laboratory, GaAs ICs are demonstrating an advantage of five times the performance and 10 times the power savings over ECL technologies, but GaAs production technology still lags behind silicon technology by about eight years. Three-inch GaAs wafers are only now becoming commercially viable, with 4-in. wafers still two years away.

According to Tom Reeder, product marketing manager for Triquent (Beaverton, OR), GaAs LSI loaded gate delays are approximately 500 ps (for fanouts of 4 and metal loads of 3 mm), with power consumption at about 1 mW per gate. While the power consumption is about two times better than the best ECL gate arrays, the speed is comparable



By providing ECL-level performance at a fraction of the power dissipation, Bipolar Integrated Technology has been able to produce the market's first ECL-class 16×16 multiplier. By far the fastest 16×16 fixed-point multiplier on the market, BIT's 11-ns B3011 provides a full 40-bit parallel output port, dual 40-bit accumulators, 10K ECL compatibility, and consumes only 5.5 W.

at best. Motorola's MCA10000, which specs loaded gate delays at 250 ps, is about twice as fast.

The problem is that GaAs performance falls off dramatically under heavy loading. While unloaded GaAs delays may be well under 100 ps, long metal lines can increase the delays to as much as 1 ns. Like CMOS gates, GaAs gates are inherently drive-limited because they use FETs. GaAs transistors have about four times the drive of CMOS, but because their drive is proportional to the difference between the gate-to-source and threshold voltage, and bipolar drive is an exponential function of collector current, GaAs transistors have much lower drive than bipolar transistors.

CMOS gate arrays compensate for their lack of drive at the system level with their higher density. Because CMOS arrays are so dense, gates within the array drive fewer loads and drive smaller amounts of metal on average. Consequently, even though CMOS transistors can't match bipolar transistors in drive because they don't require as much drive, the performance doesn't degrade appreciably in gate array applications.

The low power of GaAs will ultimately give it the same high density as CMOS. Because GaAs process technology is so far behind, however, its density is currently limited to a few thousand gates. Consequently, GaAs gates have to drive the same number of loads and the same amount of metal as ECL gates. This causes GaAs gate array performance to degrade dramatically. "By using high-drive buffers at cell outputs," explains Reeder, "gate delays can be kept to under 500 ps. However, in the long run, larger GaAs wafers will have to become available before GaAs can compete seriously with ECL at the LSI level."

While GaAs LSI still has a way to go, several vendors are demonstrating that commercial GaAs LSI is feasible. Probably the most significant GaAs product introduction this year was the GaAs version of AMD's ECL 2901 bit-slice processor from Vitesse (Camarillo, CA). Vitesse's 2901 offers

about two to three times the performance of AMD's 2901 at one-tenth the power. Users should bear in mind that the AMD part uses 2-year-old ECL technology, and that an equivalent part fabricated with today's best ECL would be as fast as Vitesse's part. However, the Vitesse part does demonstrate the production viability of GaAs.

GaAs vendors are also moving into the gate array and memory markets. Triquent has an internal 6000-gate custom capability, and Vitesse plans an 8,000 to 10,000 gate array within the next two years. Ford Microelectronics (Colorado Springs, CO) has introduced a smaller array, and Honeywell has introduced some lower performance gate arrays that are targeted at the military market. In the memory market, Vitesse is producing a 2.5- to 3-ns SRAM, which should be faster than even the best ECL SRAMs. Ford will have an under-2-ns, 1-kbit SRAM by mid-1987.

While GaAs won't pose a serious threat to ECL for a few years, CMOS will begin to win designs from low-end and even medium-performance ECL gate arrays. ECL will maintain its cell-level speed advantage. However, with CMOS loaded gate delays dipping below 1 ns, and usable densities reaching 50,000, CMOS may soon be able to challenge ECL performance at the system level. Much of the performance in high-speed systems is lost in interchip delays and in CMOS implementations. Because they require fewer chips, they have fewer interchip delays.

Presently, high-end computer vendors are using ECL gate arrays or discrete ECL logic to implement critical data paths such as CPUs. But several vendors, including Cydrome, LSI Logic and VLSI Technology, are seriously beginning to evaluate CMOS gate arrays. Bob Rau, president of Cydrome (San Jose, CA), claims that CMOS becomes competitive at 500-ps loaded gate delays and 50,000 usable gates. Both VLSI Technology (San Jose, CA) and LSI Logic (Milpitas, CA) are closing in on ECL speeds, claiming 50,000 usable gates with sub-700-ps loaded gate delays. **CD**

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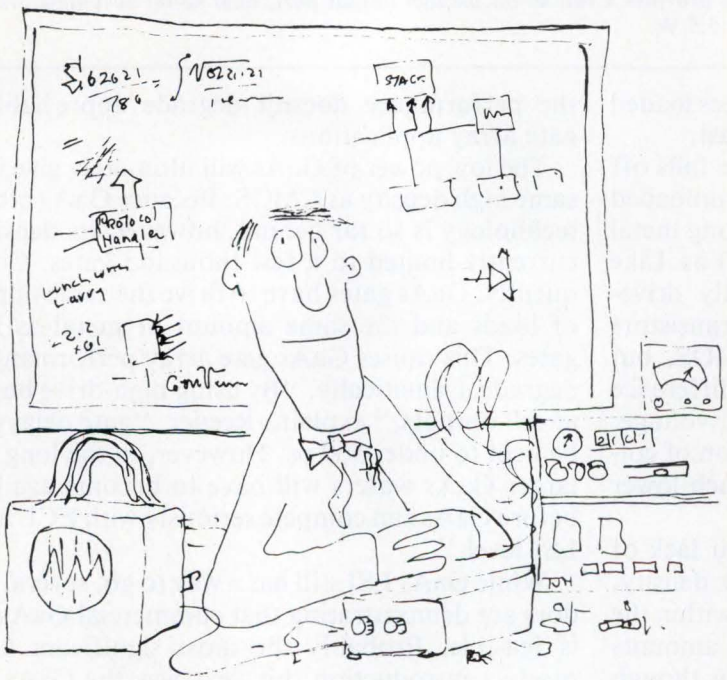

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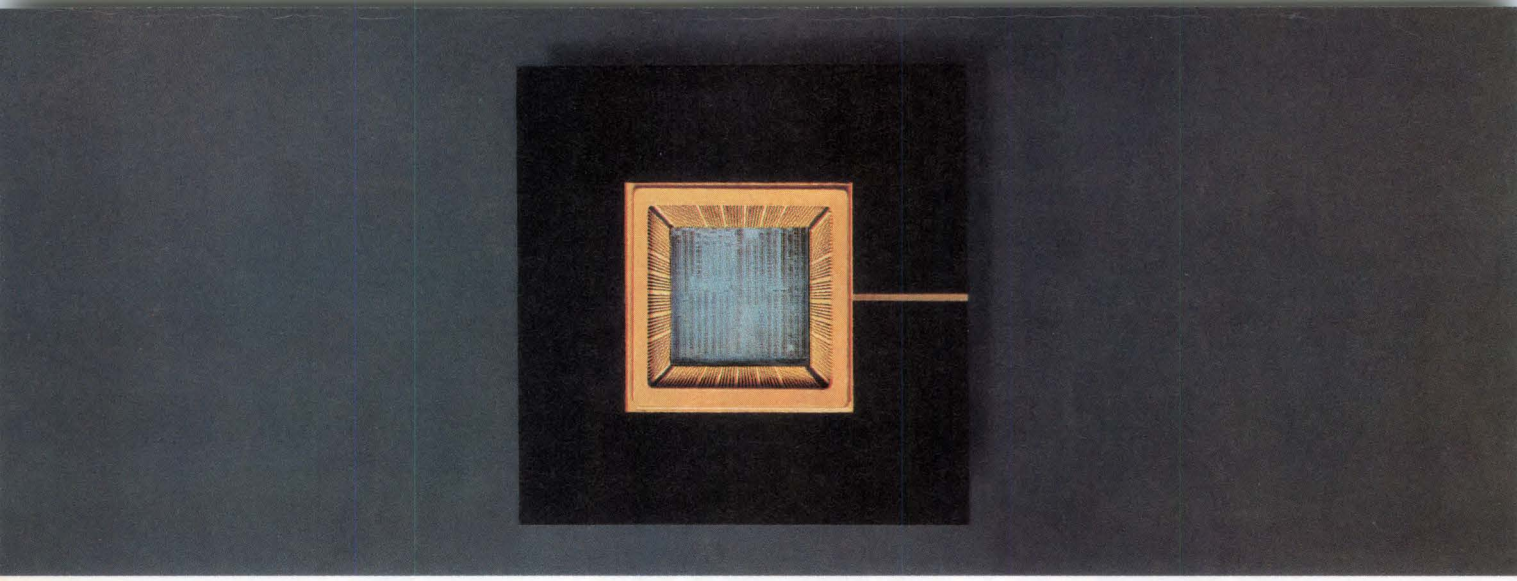

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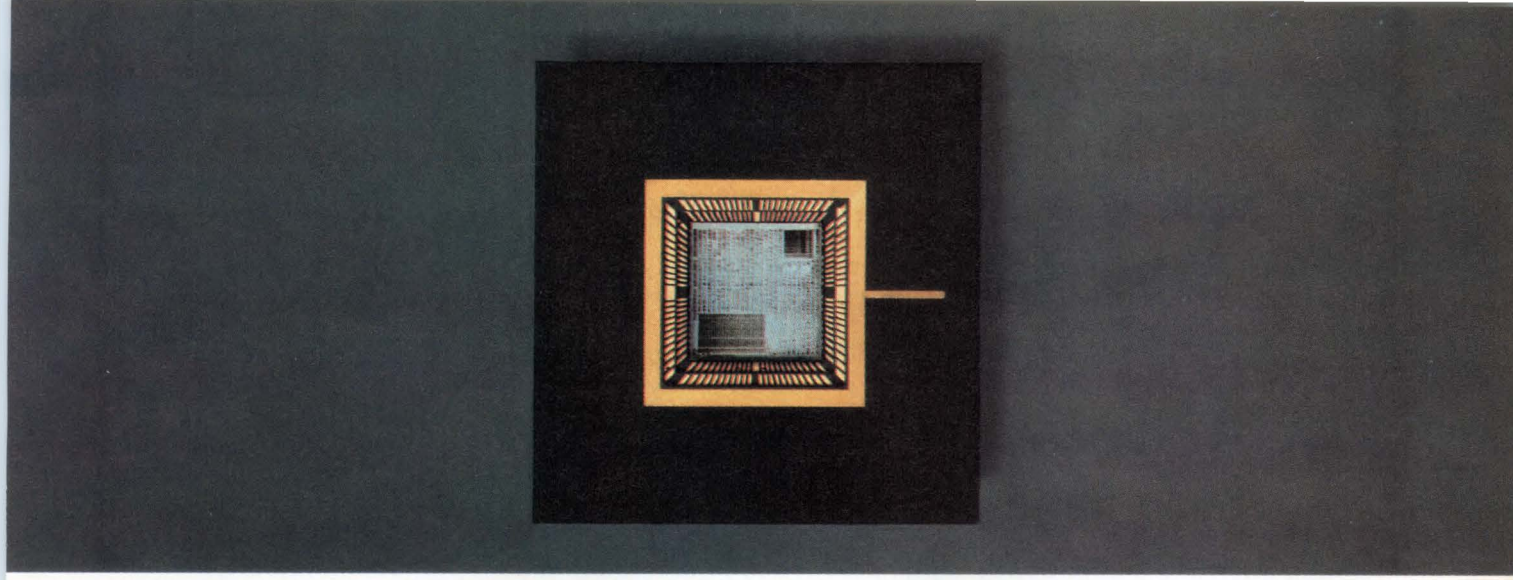

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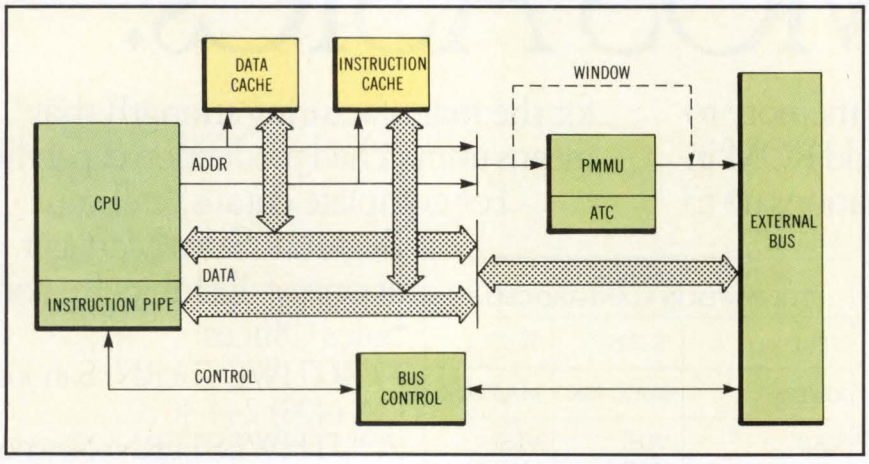
CIRCLE NO. 35

68000 family is expanded with second generation 32-bit MPU

Retaining 100 percent software code compatibility with the entire 68000 family, the MC68030 from Motorola is based on the 68020 core. This second generation 32-bit MPU offers twice the performance of its predecessor and several additional enhanced features.

Departing from the traditional von Neumann architecture used in most 32-bit microprocessors, the MC68030 employs a modified Harvard architecture to attain this increased performance while maintaining backward compatibility. The architecture uses three internal, nonmultiplexed buses and independent on-chip data and instruction caches to let the CPU, caches, paged memory management unit and bus controller operate in parallel. This enhanced internal parallelism provides the processor with an internal bus bandwidth of greater than 80 Mbytes/s. With the ability to simultaneously access from the instruction cache, data cache and external memory, the MC68030 can attack a microprocessor's major performance bottleneck—data flow to the CPU—and significantly improve performance. To keep bus access time low, a burst fillable cache mode permits high-speed data fills at both the data and instruction caches.

Unlike the 68020, which uses an external management unit, the 68030 makes additional gains in performance by incorporating the memory-management function on-chip. Besides reducing system size and cost, in some cases this implementation reduces the virtual-to-physical address translation time to zero by performing translation for the next address during the current bus cycle. The resulting reduced translation time lets designers use physical data caches with slower, denser and less expensive static RAM.



The chip also supports the flexible coprocessor interface first introduced in the MC68020 and adds additional pins to support burst mode, synchronous mode, dual cache support and emulation. A dynamically configurable bus interface supports both a synchronous bus interface (with at least two clock accesses), allowing maximum access time to a cache subsystem, and an asynchronous interface (as on the 68020) for slower memories, peripherals and other subsystems. The interface supports synchronous or asynchronous accesses on a cycle-by-cycle basis as determined by the memory subsystem requested. Compatibility is maintained by supporting the existing aynchronous dynamic bus sizing feature which allows interfaces to 8-, 16-, or 32-bit devices.

General samples will be available in July 1987.

Motorola, PO Box 3600, Austin, TX 78764. **Circle 114**

Single-chip interface available for Multibus II

To further improve processor use and data transfer efficiency in systems based upon the Multibus II architecture, two companies, Intel and VLSI Technology, have jointly introduced the Message Passing Coprocessor (MPC). MPC is a single-chip bus interface component that implements the message-passing protocol, thus relieving the main CPU from communications tasks.

MPC communicates with other boards across Multibus II Parallel System Bus (iPSB) by requesting information (requester mode) or by responding to requests in the system. In requester mode, MPC performs all arbitration functions, transmits message packets, monitors and reports error during data transfers and generates parity. As a replier, it receives message packets, checks parity and supports access to interconnect space from both on- and off-board requesters.

The device is processor-independent and maximizes bus use by transferring all data at maximum bandwidth and speed of the bus. In the Multibus II environment, it's compatible with the 186/286/386 and 68000 families of processors. It supports the coexistence of dual-port and message-passing architectures.

The coprocessor offers three interfaces: one to the on-board CPU, one to the Parallel System Bus and one to interconnect space for identifying, configuring and diagnosing boards in the system. Because message-passing schemes don't use shared memory, full memory protection is supported. With individual CPUs managing only their memory and operating systems in a local environ-

ment that's invisible to other system boards, multiple operating systems can function in a single system.

Besides enhancing throughput, the device has other economic advantages. It reduces the amount of board space required to implement the bus interface, freeing space for a designer to add additional functionality. As a VLSI device, it provides cost, manufacturing and reliability advantages over discrete interfaces. And MPC manages the bus interconnect activity through interconnect space and geographic addressing, significantly reducing system design time and cost by allowing configuration in software and eliminating the use of jumpers.

Using a 2-micron, double-metal CMOS process, this 70,000 transistor device comes packaged in a 149-pin grid array. Price is $200.

Intel, 5200 NE Elam Young Pkwy, Hillsboro, OR 97123. **Circle 115**

VLSI Technology, Application Specific Logic Products, 10220 S 51st St, Phoenix, AZ 85044. **Circle 116**

Family of numeric processors eases software development

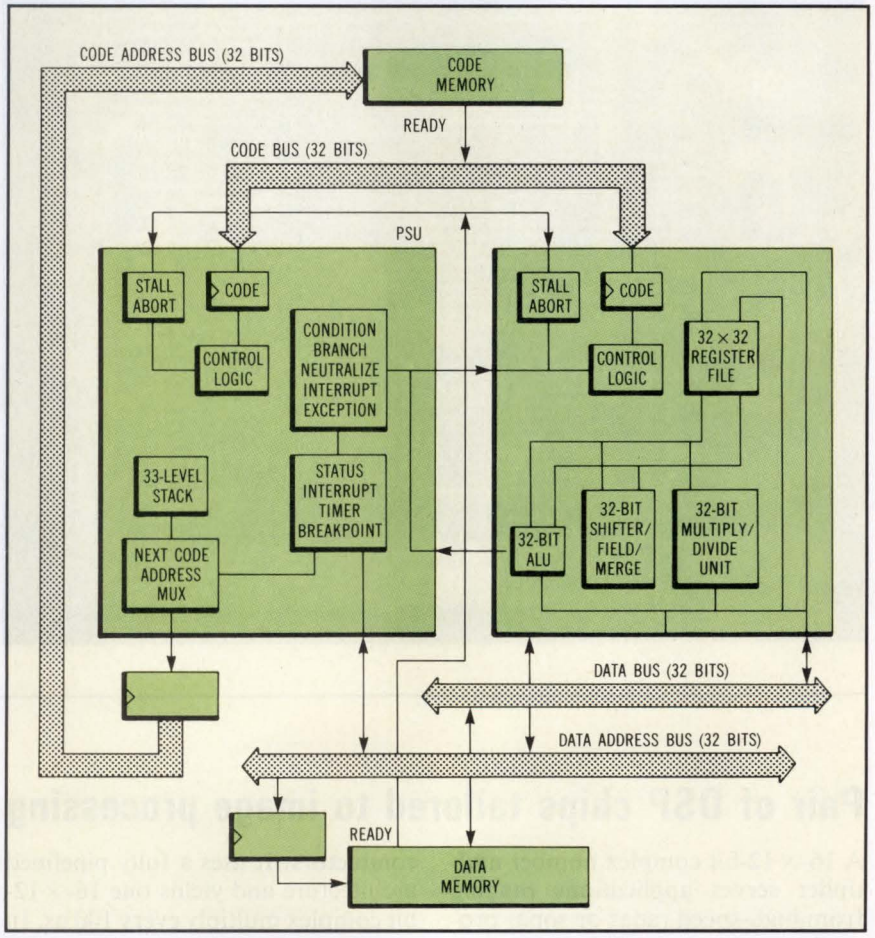
Filling the gap between compiler-supported arithmetic processors and microcoded bit-slice design, the Accel family of numeric processors can process up to 25 Mflops. These highly integrated CMOS devices from Weitek combine bit-slice performance with the ease of microprocessor development systems.

Capable of a sustained performance of 5 Mips and 5 Mflops, with peak rates hitting as high as 12.5 Mips and 25 Mflops, the Accel 8000, 8032, and 8064 speed throughput by paralleling hardware, pipelining and widening data paths. Separate code and data memories permit code and data access every clock cycle. The processors also boast an on-chip register file and stack to minimize the number of off-chip fetches.

Combining an Integer Processing Unit and a Program Sequencing Unit, the 32-bit Accel 8000 processor targets two-dimensional graphics, logic simulation and general-purpose computing. The 8032 adds a 32-bit floating-point unit to address digital signal processing and three-dimensional graphics applications as well. A third member of the family, the 8064, is identical to the 8032 but replaces the 32-bit unit with a 64-bit double-precision FPU. It serves high-speed double-precision floating-point math processing for applications such as CAE- and CAD-related three-dimensional graphics, or Fortran and C acceleration.

Software includes C, Fortran and Pascal optimizing compilers. To reduce the number of instruction cycles, these compilers eliminate redundant load/store operations, constant folding, and induction variables. The code is then loaded into a parallelizing instruction scheduler where it is examined and fitted to the execution patterns of the hardware.

Run on an IBM PC AT/Xenix or VAX/Unix host, the Accel development system consists of two boards, a software monitor, and a debugger.



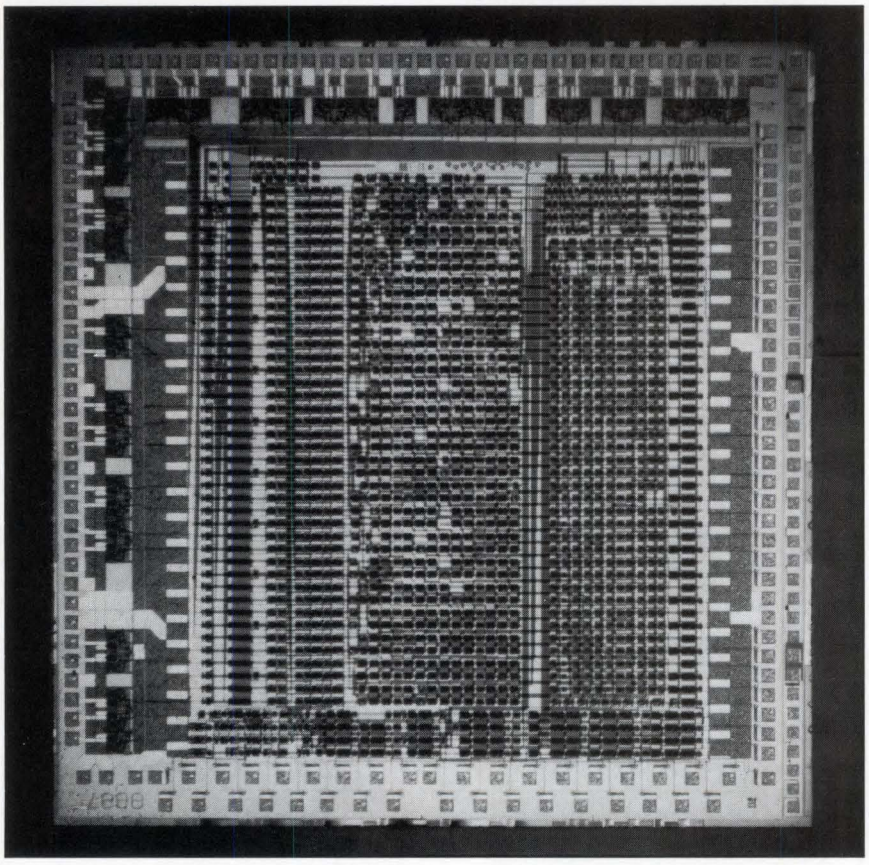
The 8000 and 8032 processing units and the Fortran and C compilers should be available in volume in January. The 8064 and Pascal compiler are due out during the second quarter of 1987. In quantities, the 8000, 8032 and 8064 cost $600, $1,000 and $1,500, respectively.

Weitek, 1060 E Arques Ave, Sunnyvale, CA 94086. **Circle 117**

New process generates fast 16- × 16-bit multiplier-accumulators

Using a new bipolar VLSI manufacturing process, Bipolar Integrated Technology has introduced an ECL 16- × 16-bit multiplier-accumulator that delivers a typical multiply-accumulate time of 11 ns. Typical power dissipation for the B3011 is 5.5 W. The company has developed a TTL version (B2011) of the multiplier-accumulator that's also clocked at 11 ns, but with only 4.5 W power dissipation.

For complex number and double precision computations, both chips provide 40-bit accumulation with dual input registers and 40-bit output. Packaging is a 132-pin grid array. Both units offer parallel loading of full accumulator from input ports and add or subtract the input value from the accumulator. A choice of registered or transparent inputs is available. They also feature single, double or triple clock operation and separate negative sign, overflow and zero status flags.



The bipolar VLSI technique used in these products is capable of 200-MHz input clock rates, according to the company. It improves power delay over traditional ECL processes by a factor of five and achieves densities comparable to 1.5 micron CMOS.

Minimum mask feature size is 2 microns and typical gate propagation delay is 300 ps. Individual gate power dissipation is 0.3 mW. The chips have two metal layers with a metal pitch of 4 microns (2-micron line width and 2-micron spacing) on both layers. Overall transistor area is 14 microns^2.

Prototypes are available now, and production quantities will be available in early 1987. The B3011 sells for $340, and the TTL B2011 is priced at $265.

Bipolar Integrated Technology, 1050 NW Compton Dr, Beaverton, OR 97006. **Circle 118**

Pair of DSP chips tailored to image processing

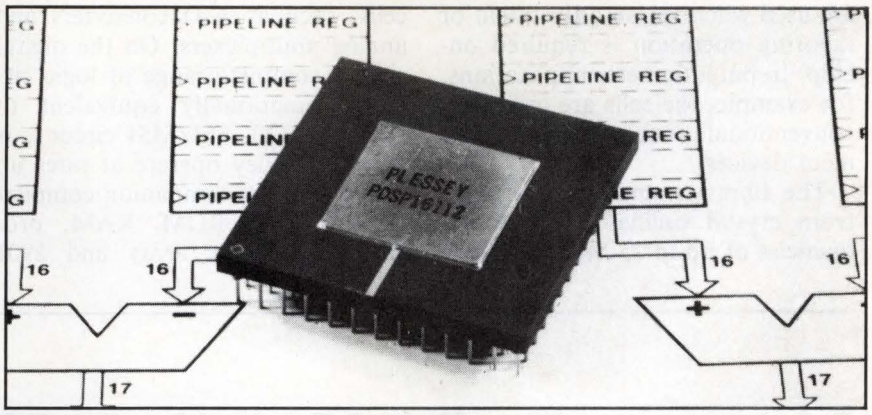
A 16- × 12-bit complex number multiplier serves applications ranging from high-speed radar or sonar processing systems to digital filtering, Fast Fourier Transforms, graphics image processing and instrumentation. This single chip operates at 10 MHz and replaces four multipliers and two adders.

The first of a family of 2-micron CMOS digital signal processing devices, the PDSP16112 chip was designed using the Megacell semicustom technique from Plessey Semiconductors. It uses a fully pipelined architecture and yields one 16- × 12-bit complex multiply every 100 ns. In addition to offering complete TTL compatibility, the chip features a test control pin that permits execution of a self-test at 1 million vectors/0.1s. It's composed of a three-row × six-column array of full adders and combines four real/imaginary parts of the products in two pipeline 16-bit adders. Available in an 84-pin grid array, the PDSP16112 chip is priced at $283 in 1,000-piece quantities.

A second chip developed using the Megacell process is the first 2-micron CMOS digital single-chip processor designed for image edge detection that measures the presence, size and direction of edges within a video frame. Called the PDSP16401, it operates at 20 MHz and performs 22 (13-bit) additions and three comparisons in 50 ns. The device features four independent 3 × 3 filters and an on-chip threshold detector. Power consumption is less than 500 mW across a −40 °C to +85 °C range.

As a dedicated single-chip signal processor, the PDSP16401 can replace a complete logic board in applications such as robotics and machine vision. It detects edges by performing a concurrent convolution of a frame consisting of three adjacent pixels in each of three input lines with four 3 × 3 masks. The chip sells for $320 in an 88-pin grid array and $296 in an 88-pin leadless chip carrier.

Plessey Semiconductors, 3 Whatney, Irvine, CA 92718. **Circle 119**



Cell library uses EEPROMs to speed VLSI circuit design

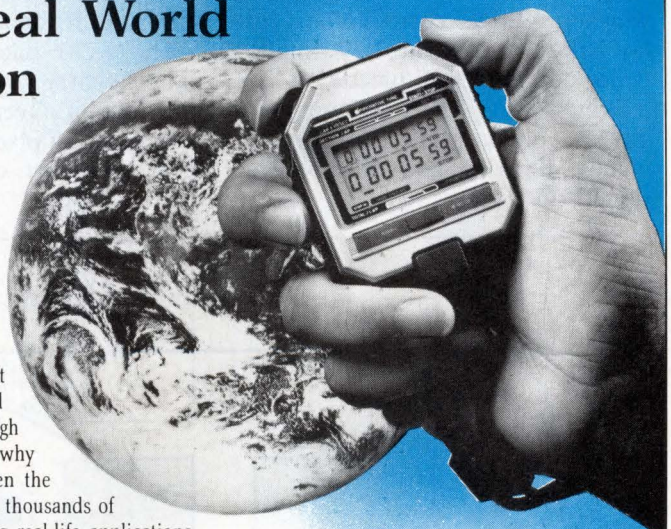
Improving system integration while reducing cost, Sierra Semiconductor has introduced the first standard-cell library with electrically erasable memory cells that let users calibrate and tailor systems without manual adjustments. The library includes a range of analog and digital cells and a full set of computer-aided design tools. Using this product, a system designer can easily design a VLSI chip to replace all conventional linear integrated circuits and digital integrated circuits and to adjust components on an existing printed circuit board assembly.

Called the Triple Technology Library, it's based on a 2-micron CMOS technology that allows extensive analog, digital and memory-function integration in a single VLSI circuit without loss of performance or reliability. The EEPROMs ease integration by providing on-chip, nonvolatile storage of calibration parameters and access codes or other tailoring data. They also provide low-cost, nonvolatile on-chip replacements for potentiometers, switches and jumper wires, as well as offering other means of calibrating, adjusting and programming system functions. By eliminating the manual adjustments, operations such as system test, calibration and maintenance can be automated.

These advances in integration are accomplished using a rugged single-bit EEPROM cell. The EEPROM circuitry is embedded in digital flip-flop and latch cells, which make the details of the EEPROM operation completely transparent to the circuit designer. The cells are programmed on the chip using a high-voltage interface cell and the optional EEPROM 5- to 18-V power supply generation cell.

Registers and other simple circuits

The Real World Runs on Real Time.



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CIRCLE NO. 36

are used wherever an adjustment or tailoring operation is required on-chip. In potentiometer applications, for example, the cells are used with conventional on-chip analog adjustment devices.

The library's analog cells range from crystal oscillators, with frequencies of up to 25 MHz, to super cells, such as A-D converters and analog multiplexers. On the digital side, a complete range of logic circuits, functionally equivalent to standard TTL SSI/MSI circuits, is included. They operate at rates up to 80 MHz. A companion compiler library offers ROM, RAM, programmable logic array and 2901 data path cells of any size.

A CAD system, with tools for schematic entry, circuit simulation and verification, circuit layout, interconnection routing and test programming, supports VLSI design.

Sierra Semiconductor, 2075 N Capitol Ave, San Jose, CA 95132.

Circle 120

D-A converter chip offers 3-D graphics for PC applications

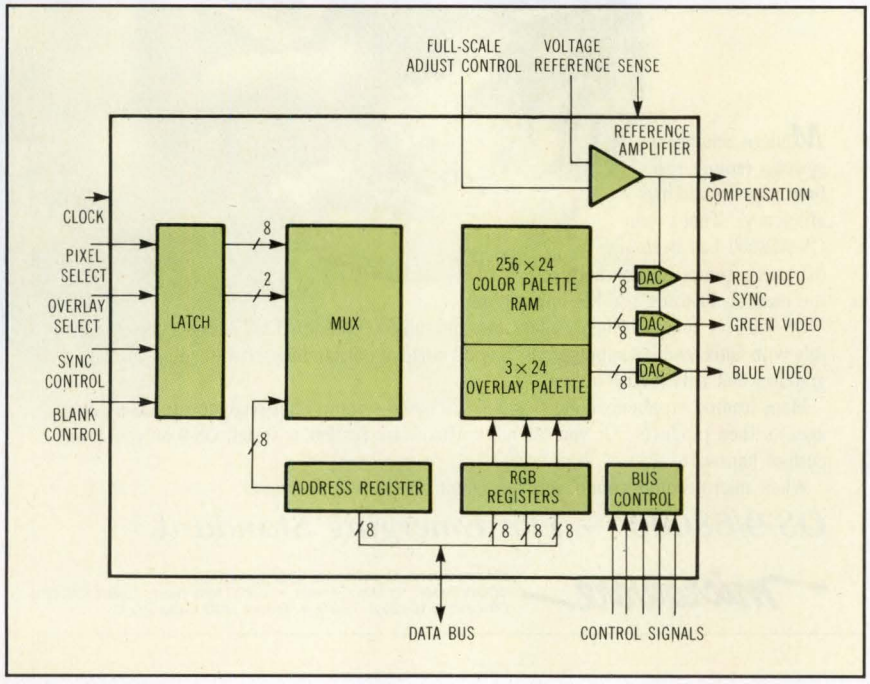
The Bt453 is a 40-MHz, TTL-compatible, monolithic CMOS IC designed for producing high-resolution three-dimensional color graphics for personal computer applications. The Bt453 combines three 8-bit video D-A converters with color palettes, overlay registers, a multiplexer, a latch and other elements on a single chip.

A dual-ported 256-color × 24-bit palette RAM combines with the company's exclusive Sidecar RAM, which is a three-color × 24-bit overlay palette, to provide 259 simultaneous colors from a palette of 16.8 million colors. The overlay palette stores colors used for cursors, menus, blinking and other operational functions.

A separate bus interface provides direct access for an external microprocessor controller to internal control registers and color and overlay palettes. Control signal inputs specify whether the MPU is accessing the address register, color palette RAM or overlay registers.

The address register's upper eight bits increment following reading or writing of blue color information and specify which color palette is accessed. The two least significant bits specify RGB data.

The RGB data specifies which palette entry will provide color information. Overlay inputs may be controlled by pixel timing or by external character, cursor or grid generation logic.



Red and green values, of eight bits each, are temporarily stored in registers when writing to the palettes. They combine with the eight bits from the blue value during the blue value write cycle, so that all 24 bits are written to the palettes at one time. During the period in which the microprocessor is writing or reading RGB data, pixel- and overlay-select inputs to the latch are forced to a reference black level.

The latch serves as a digital buffer to synchronize pixel timing. At the beginning of a clock cycle, eight bits of pixel select information and two bits of overlay select information are latched into the Bt453. The selected 24 bits of color information, eight bits for each color, are input to the three video D-A converters on every clock cycle.

Sync and blank control inputs are sampled at the beginning of each clock cycle and are pipelined to maintain synchronization with the pixel and overlay select data. Each video D-A converter converts the digital information to analog signals for the color guns of the CRT monitor. The varying output current from each video D-A converter generates a corresponding RS-343-A compatible red, green or blue video signal as a voltage that drives a doubly-terminated 75-Ω coax directly. A typical output load is 37.5Ω. No external buffering to the CRT is necessary. A separate current output provides a composite sync signal for horizontal and vertical synchronization. Typically, only the green video signal contains sync information.

The video D-A converters have a

segmented architecture that eliminates the need for precision component ratios. Monotonicity and low glitch result from the use of identical current sources.

The Bt453 is available as a 40-pin CERDIP in sample quantities for $58 each.

Brooktree, 9950 Barnes Canyon Rd, San Diego, CA 92121 **Circle 121**

Monolithic programmable timing chip controls digital system performance

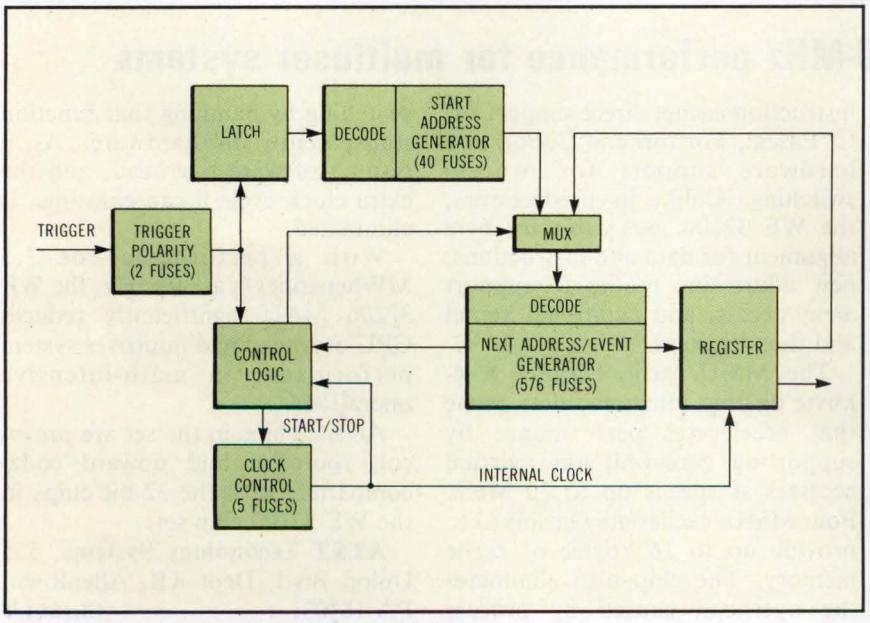
Replacing counters, analog delay lines and resistor/capacitor networks, the Am 2971 Programmable Event Generator (PEG) from Advanced Micro Devices is the first monolithic digital timing circuit to allow high-precision system timing. Offering timing control applications for a broad range of digital systems, this chip can reach a resolution as low as 10 ns between events.

Key to the PEG chip's performance is a new architecture that incorporates a 10- to 100-MHz multiplying phase-locked-loop crystal oscillator for improved timing accuracy. It can be clocked from an existing external system clock or from an on-board crystal oscillator. The chip's 12 programmable registered output waveforms define 12 independent timing signals. Operators can select one of eight user-programmable start addresses to calibrate the timing sequence and to program all stop functions.

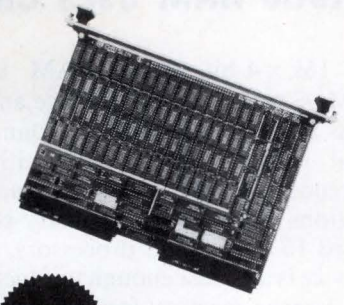
Since every digital system requires timing control, the device can serve many applications. A typical use is as a digital substitute for analog delay lines when generating accurate clock signals demanded by address-multiplexed dynamic RAMs. Its programmability and large number of outputs let it replace several delay lines simultaneously. Other applications include bus timing or peripheral control in such areas as disk drive control or timing control for bit-mapped graphics.

Available in a 24-pin ceramic DIP, the chip is priced at $17.75 each in 100-unit quantities.

Advanced Micro Devices, 901 Thompson Pl, PO Box 3453, Sunnyvale, CA 94088. **Circle 122**



VME



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CIRCLE NO. 71

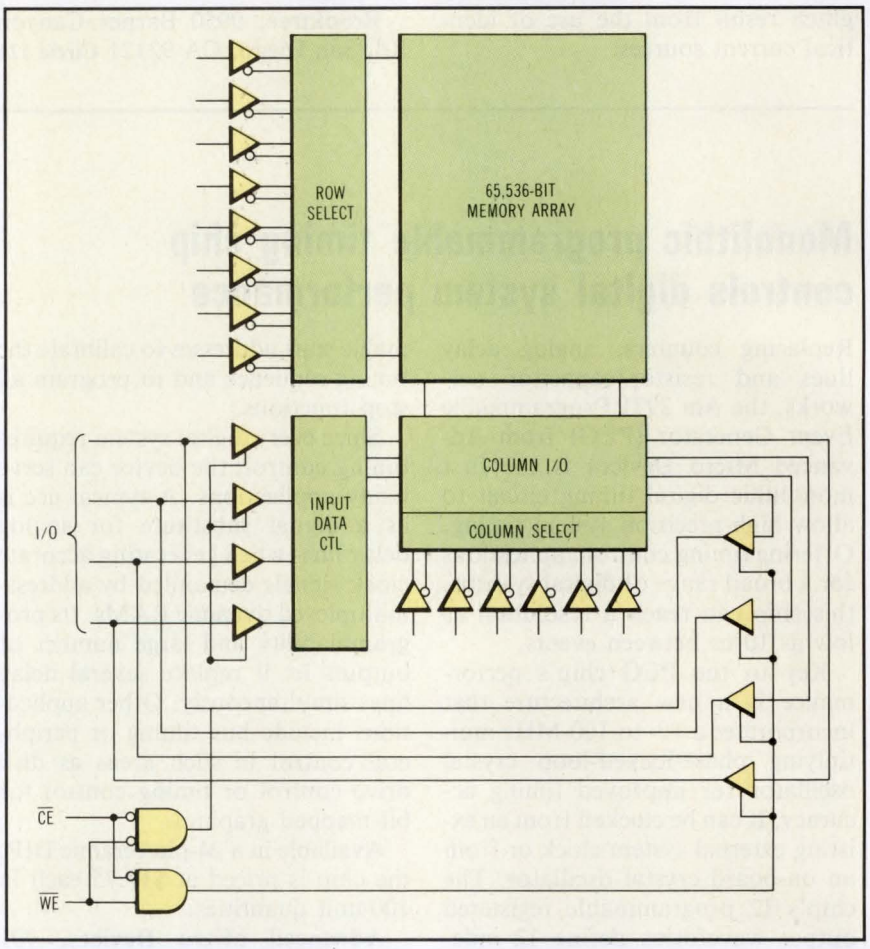
Static RAM uses CMOS to break speed barrier

A 16k × 4-bit static RAM uses CMOS technology to achieve an access time of 20 ns over the commercial temperature range. Initially intended for a broad range of applications supporting industry-standard 16- and 32-bit processors, this device is also fast enough to function as a cache memory for mini, supermini and mid-range general-purpose computers or high-performance scientific workstations.

The first memory product from Performance Semiconductor, the P4C188 integrates over 400,000 transistors on-chip. All parts are completely CMOS and are designed with six-transistor cells, providing better electrical margins and single-event upset protection than conventional four-transistor cells.

The static RAM attains higher performance levels yet retains its small size through a proprietary technique called Pace. The CMOS memory needs no clocks or refreshing, and all inputs are TTL-compatible. Power consumption is a low 550 mW active and 193 mW standby.

Performance Semiconductor, 610 E Weddell Dr, Sunnyvale, CA 94089. **Circle 123**



32-bit chip set offers 30-MHz performance for multiuser systems

Claiming to be the first chip set to offer system-level performance in the 20- to 30-MHz range, the WE 32200 chip family is a third generation 32-bit product optimized for Unix systems. The chips are implemented in the same 1-micron CMOS technology used by AT&T in its 1-Mbit DRAM.

The set includes three chips: the WE 32200 microprocessor, the WE 32201 Integrated Memory Management and Data Cache (MMU/cache) and the WE 32206 Math Acceleration Unit (MAU). All three are offered in speeds from 20 to 30 MHz.

The CPU chip offers a 256-byte instruction cache, direct support for C, Pascal, Fortran and Cobol, and hardware support for process switching. Unlike its predecessors, the WE 32206 uses arbitrary byte alignment for data and instructions, new addressing modes to support array access, and additional kernel and user registers.

The MMU/cache features a 4-kbyte on-chip integrated data cache that accelerates performance by supporting zero-wait-state virtual accesses at speeds up to 30 MHz. Four MMU/caches may be linked to provide up to 16 kbytes of cache memory. The chip also eliminates the overhead caused by process switching by handling that function transparently in hardware. As a result, software overhead, and the extra clock cycle it can consume, is eliminated.

With a performance of 3.5 MWhetstones/s at 30 MHz, the WE 32206 MAU significantly reduces CPU overhead and improves system performance in math-intensive operations.

All the chips in the set are protocol, footprint and upward code-compatible with the 32-bit chips in the WE 32100 chip set.

AT&T Technology Systems, 555 Union Blvd, Dept KB, Allentown, PA 18103. **Circle 155**

PAL device broadens functional capabilities

A 20-pin programmable array logic device from Advanced Micro Devices—called the AmPAL18P8—simplifies device programming and makes it easier to optimize logic functions. The unit features programmable output polarity so that designers can select active high or active low on each of the eight outputs, which allows the handling of both outputs on the same device. In addition to the eight output pins, the device offers a total of 18 input pins—two more than other 20-pin PAL devices—which extend its functional capabilities.

Each of the chip's inputs is connected to a programmable AND array containing 72 logical product terms. Using eight product terms and one three-state control term for each output, the AmPAL18P8 can be programmed with complex logic equations, providing extra logic power and design flexibility.

High-speed versions of the device boast an input-to-output propagation delay of 15 ns. To obtain this speed, the chip takes advantage of the company's Imox oxide-isolation process. With the Imox process, density increases while internal capacitance decreases. The PALs are fabricated with a platinum-silicide fuse technique that gives a controllable melt rate and large non-conductive gaps that increase reliability.

Each fuse of the PAL is programmed with a simple sequence of voltages that are applied to the output being programmed. To address the fuse array, TTL and V_{HH} levels are set on eight input pins (five select the input line number and three select the product term number). V_{CC} is maintained at a normal level throughout programming and verification cycles.

After programming has been completed, the array can be reverified at V_{CCL} and V_{CCH}. Reverification is accomplished by reading all eight outputs in parallel, instead of one at a time. The verification cycle for array fuses checks that the correct array fuses have been blown and can be sensed by the outputs.

In quantities, the chip sells for $3.55 each for the 25-ns version.

Advanced Micro Devices, 901 Thompson Pl, Sunnyvale, CA 94088. **Circle 124**

80386 logic support implemented in seven-chip set

When Chips and Technologies introduced its 80286 chip set last year, vendors found it offered a simplified method to create IBM PC AT-compatible products. The company is now entering the 32-bit arena with a seven-chip set for the 80386. When used in conjunction with the company's recently unveiled Integrated Peripherals Chip (IPC), users can configure an 80386-based system board with only 40 components plus memory devices. The board produced is one-half the size, consumes one-third the power and delivers more than twice the performance of an 8-MHz 80286 AT.

The seven-chip set manages both address and data functions for the 80386, as well as memory and bus control. It combines one bus controller chip (82C301), a page/interleave memory controller chip (82C302), two address buffer chips (82A303 and 82A304), two data buffer chips (both designated 82A305), and one miscellaneous control logic chip (82A306). The standard architecture of the set supports a local CPU bus, a 32-bit memory bus and AT buses. AT-bus compatibility is provided by an independent clock that compensates for the built-in timing assumptions inherent in many add-on boards. It achieves the full 16-MHz, zero-wait-state operation of the 80386 and supports from 1 to 16 Mbytes of memory.

As a completely AT-compatible solution, the CS 8230 chip set runs the billions of dollars of applications software that can run on the AT, XT and PC. This software compatibility, combined with the processing power of the 80386, direct the chip set toward the compute-intensive CAD/CAE, industrial automation and transaction processing applications traditionally associated with 32-bit microprocessors. "CAD/CAE applications demand the horsepower of 32-bit, 80386-based machines," claims company president Gordon Campbell. "With the CS 8230 chip set, users have a cost-effective solution for a system with that power, yet the system is completely compatible with the IBM PC AT."

Supporting the set is a development kit, the DK 8230, to assist users in their design efforts. The kit offers a development board, data sheet, user's guide and data book for the chip set.

The CS 8230 AT/386 seven-chip set sells for $196.40 in quantities of 100, while the development kit is $2,995.

Chips and Technologies, 521 Cottonwood Dr, Milpitas, CA 95035. **Circle 125**

Coming January 1

Watch for the System Design article on digital control of linear circuits by John Nemec of Signetics

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- ☑ Three Drivers, Three Receivers
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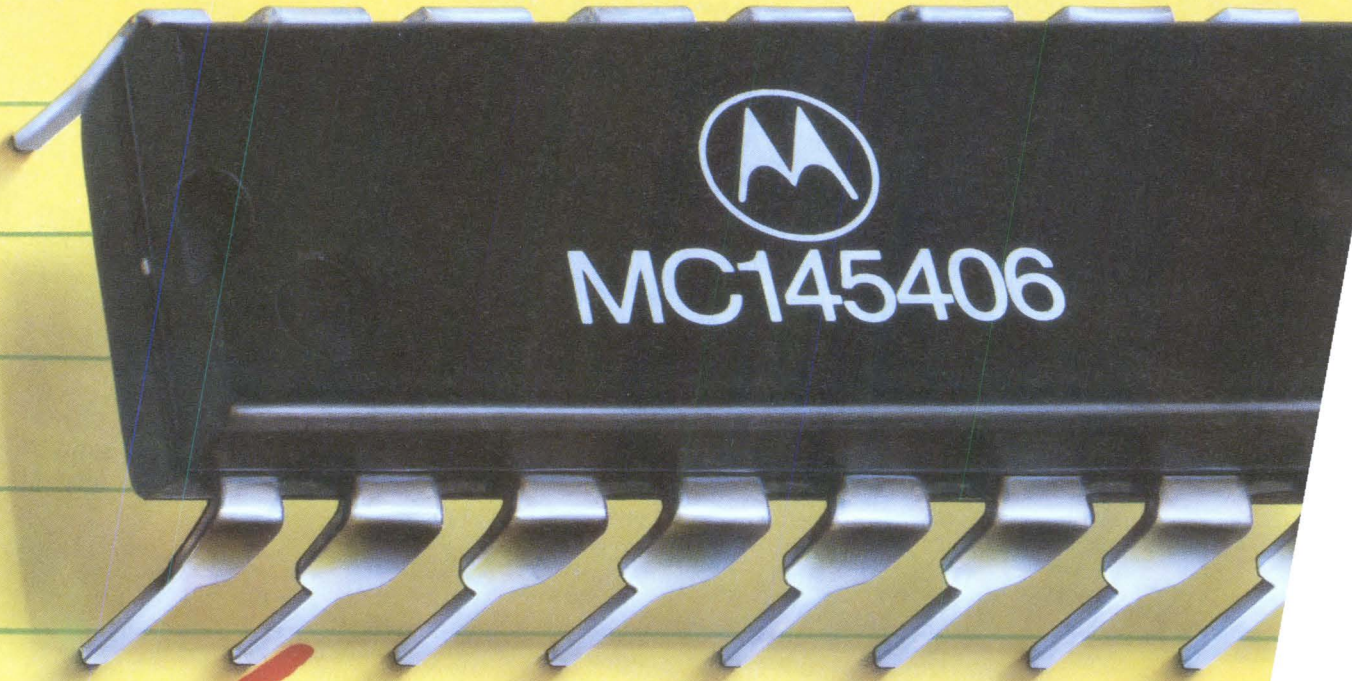


- ☑ 15 mW P_D
- ☑ ±5V–±13V Operation
- ☑ TTL Digital Interface

Space and power efficiency.

RS-232-C IC combines 3 drivers and 3 receivers in a single CMOS chip. Try the MC145406, free.

Motorola's new MC145406 silicon-gate CMOS Driver/Receiver IC for the first time combines 3 drivers and 3 receivers on a small single chip to meet the electrical specs of EIA RS-232-C and CCITT V.28.

Anyone designing communications equipment where low power and space savings are important, such as digital telephones, portable computers or line-powered modems, will discover nothing can do the job better.

Free MC145406 samples.

We want everyone to know just how outstanding the MC145406 is, so we've arranged for you to have two evaluation samples without charge. To receive your samples, simply attach your business card to the completed coupon from this ad when you send it in. We'll send you the parts, the data sheet and our Telecomm Data book, absolutely free. Offer expires March 30, 1987 and requests must be postmarked by April 1, 1987.

Low power: 15 mW CMOS vs. 706 mW bipolar.

It's the low-power CMOS technology of the MC145406 that requires a maximum of only 15 mW compared to the 706 mW required by a common bipolar pair previously used to accomplish the same job.

There's no comparable choice for new low-power designs, and you reduce package requirements at the same time.

Space-saving package alternative.

Original availability of the MC145406 was in the traditional 16-pin dual in-line package, and that's the package the free samples are in.

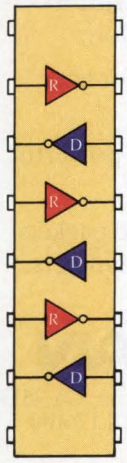
Now, for even greater space savings, this low-power CMOS IC is also available in the 16-pin SOIC package.

Drivers.

MC145406 drivers offer true TTL input compatibility, a slew-rate-limited (30 V/μs max.) output circuit that requires no external capacitors and a 300 ohm power-off source impedance.

Receivers.

The on-chip receivers can handle up to the EIA-required 15 volts, while presenting impedance over a 3-to-7 kilohm range.



They will level-shift voltages between -15 and +15 volts down to TTL logic levels from 0 to +5 volts: also from TTL levels to voltage levels proportioned to the high-voltage supplies applied to the device. Input switchpoint hysteresis gives the receivers a significant assist in reception of noisy signals.

No better DCE interface device.

This incomparable driver/receiver provides all the necessary level-shifting between the TTL logic levels of your product and the high voltage levels of RS-232-C equipment. It's finding new applications from PABX to remote telebanking and from key systems to multiplexers, limited-distance modems and computer networks.

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Someone has.

The someone is Excelan.

We took all the features of our Nutcracker, the most powerful Ethernet network analyzer there is, added even more new features, and put them all onto a single plug-in board. Our new creation is called the LANalyzer EX 5000E. It comes with complete system software that runs on MS-DOS. And it slips right into your IBM PC, XT, AT, or compatible.

The LANalyzer VLSI components and high performance software help you monitor, analyze, and troubleshoot your Ethernet network as nothing else can. And its extensive graphic displays make it easy to use, too.

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- Capture Ethernet packets at a sustained rate of 1000 packets per second.
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The EX 5000E functions independently of any vendor's Ethernet hardware or software. And it's compatible with Ethernet V1.0, V2.0 and IEEE 802.3.

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In either form, the EX 5000E is the most powerful, versatile, cost-effective tool there is for handling an unsurpassed range of LAN analyzer applications — everything from development to maintenance, even in complex multivendor environments.

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CIRCLE NO. 34

Price and performance improvements drive design tool market

Competitive pressures and technological advances have combined to make CAE/CAD systems, development systems, and test and measurement tools more accessible to the average system designer.

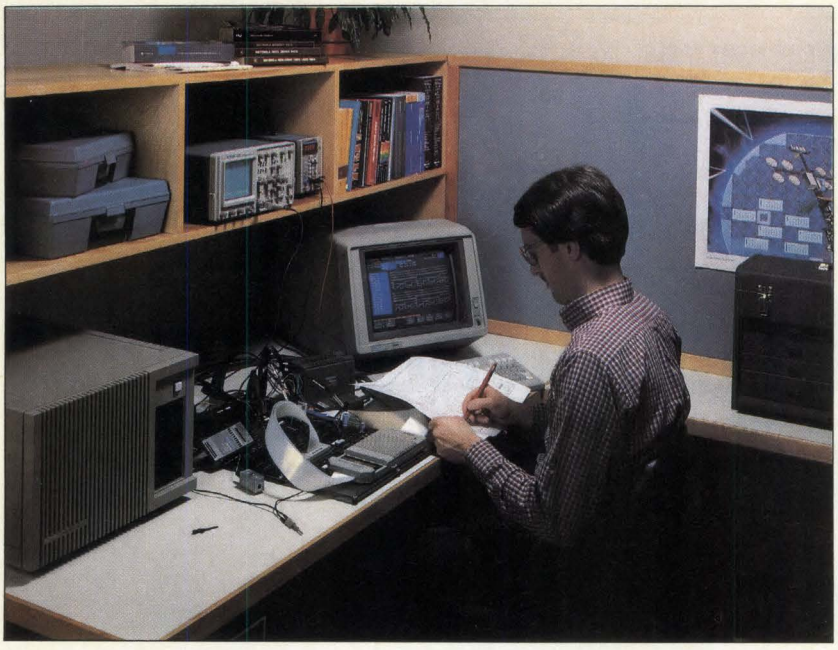
Richard Goering
Senior Editor

For users and prospective buyers of design tools, 1986 has been a good year. Sharp price drops in computing platforms and innovations in technology have made many tools more affordable and powerful. As the electronic CAE/CAD industry becomes more mature, there have been fewer premature product announcements and unsubstantiated claims than in previous years.

It hasn't been such a good year for vendors, however, particularly in the beleaguered CAE/CAD sector. As the industry goes from an exponential growth rate to something approaching normality, too many companies are fighting for an increasingly selective group of customers. And CAE tools are still used mostly for application-specific ICs, while many board- and system-level designers remain skeptical. Growth has also been disappointing for vendors of microprocessor development systems and test instrumentation.

Few technological breakthroughs have emerged in CAE/CAD software, microprocessor development tools or test instrumentation. In fact, the biggest news in CAE/CAD didn't come directly from CAE/CAD vendors, but concerned such items as price drops in 32-bit workstations, add-on capabilities for the IBM PC and developments in acceleration, parallel processing and networking.

Although design tools are becoming less expensive, the integration of tools is a largely unsolved problem that will continue to plague users and vendors in 1987. Design tool vendors are continuing their move to industry-standard computing platforms and operating systems. But many development labs are still hobbled by proprietary data formats, incompatible operating systems and platforms that can't be networked. Standardization efforts such as the Electronic Design Interchange Format are making progress, but implementation is very slow.



The Apollo DN3000 allows Mentor Graphics to offer a turnkey workstation with schematic capture, logic simulation and timing verification for $34,000. Both hardware and software provide more functionality than the $100,000 workstations of a few years ago.

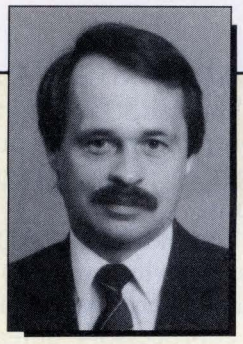
The falling cost of 32-bit workstations has made electronic CAE/CAD affordable for thousands of system designers. That trend was underscored early this year when Apollo (Chelmsford, MA) announced the Apollo DN3000, a 68020-based workstation in the $10,000 to $25,000 price range. This desktop workstation boasts a 1.2- to 1.5-Mips performance, and enhancements introduced this fall provide up to 8 Mbytes of memory, up to 348 Mbytes of disk storage and a 19-in., 1,024- × 800-pixel color display. Used exclusively by the current CAE industry leader Mentor Graphics (Beaverton, OR), Apollo also serves as a platform for Tektronix CAE Systems, Analog Design Tools, Calma and Aida.

The recent enhancements from Apollo are part of its ongoing struggle with Sun Microsystems (Mountain View, CA), which introduced a 68020-based 2-Mips workstation this summer. Priced competitively with the Apollo DN3000, the Sun 3/100 provides 4 Mbytes of memory and can support from 71 to 142 Mbytes of disk storage. It's equipped with a 15-in., 1,152- × 900-pixel color monitor. Both the Apollo and Sun workstations can serve as diskless nodes on a network. Sun is strong in electronic CAD, where it has agreements with Computervision, Applicon and Telesis, and Sun is making a concerted effort in electronic CAE.

IBM made a considerable splash in February with its RISC-based RT PC, a 32-bit workstation that falls into the $10,000 to $25,000 range. Although IBM sells Silvar-Lisco's (Menlo Park, CA) schematic capture system on the RT, few CAE/CAD vendors have embraced this platform. The RT has been widely criticized for its lack of networking and graphics capabilities. Despite IBM's claim of a 2-Mips performance, the RT runs approximately twice as fast as the IBM PC AT, generally a 0.3- or 0.4-Mips machine. It now appears that IBM will be more successful in CAE/CAD with an 80386-based workstation, expected by many observers early next year.

Digital Equipment Corp (Maynard, MA) retains a huge installed base in the engineering community, and both Valid Logic (San Jose, CA) and Daisy Systems (Mountain View, CA) are pinning their hopes on DEC. Valid this year ported many of its CAE tools to the monochrome VAXstation II and the color VAXstation II/GPX under the VMS operating system. A VAXstation II/GPX with 5 Mbytes of RAM, a 71-Mbyte disk and a 19-in., 1,024- × 864-pixel display costs around $26,000. Daisy's delay in porting its software to the MicroVAX is widely cited as one reason for that company's financial setback in 1986.

Intergraph (Huntsville, AL) broke a dollar-per-Mip record this year with its Interpro 32C, a 5-Mips workstation based on Fairchild's 33-MHz Clipper microprocessor. With 6 Mbytes of memory, up to an 80-Mbyte disk and a 15-in., 1,184- × 884-pixel color monitor, this workstation carries a base price of just $25,000. Intergraph will run its own CAE/CAD software on the machine. Sun Microsystems' 3/200 series workstations, with prices



Lutz Henckels
President
HHB Systems

CAE must address PCB market to grow

During 1984 and early 1985, the CAE industry achieved enormous growth. In the last 18 months, however, the industry's performance has fallen significantly. This downturn is reflected in the tumbling of share prices over the last year by a factor of two, or even three, of the publicly traded CAE companies. What will it take to get the CAE industry moving again? The answer requires a look at the initial success of the CAE industry.

Early success was based primarily on penetrating the IC design market with tools focused on application-specific IC design. These tools include schematic capture, simulation and layout capabilities. However, as reported by the Technology Research Group (Boston, MA), this market is now well saturated. By the end of 1986, 39,000 engineering workstations will have been sold, with most of them used for IC design applications and less than 13,000 ASIC designs performed per year. The conclusion is that any growth will have to come from CAE tools that address printed circuit board and system design applications—a market roughly three to four times larger than that for IC applications.

The question remains as to why the CAE industry is stalled, given that all major CAE vendors are now offering printed circuit board CAE tools. There are two answers to this question. First, the CAE industry has in the past promised more than it could deliver, a factor that has made CAE users more cautious about purchasing new tools. This is particularly true for printed circuit board applications, most of which could benefit greatly from CAE tools but which currently do not absolutely require them. Because of this, only proven technologies are finding their way into printed circuit board applications: namely, schematic capture and printed circuit board layout tools. Design analysis tools, such as behavioral and logic simulators, and test programming tools, such as fault simulators and automated test generators are still being used only by early adopters of the new technology. Large discretionary purchases of these CAE tools are being postponed subject to the evaluations and results achieved by the early adopters.

The second reason—and the one most responsible for the slow printed circuit board/CAE market expansion—is that CAE tools for printed circuit board design and test are still largely inadequate. From this perspective, the cautious buying patterns exhibited in printed circuit board market are warranted. Perhaps the best way to understand the nature of the problem confronting the printed circuit board market is to analyze a typical printed circuit board design situation.

Consider the design of a complex system consisting of five boards. The user first needs a good behavioral simulation capability to perform a top-down design of the circuit. The designer may start with a behavioral model for the system, then develop five models for each of the boards. The final stage might involve building six to 10 behavioral models for each section of each board. The design team then provides the details of the design by substituting the behavioral models with actual circuits of structural models. This might involve several ASIC chips, microprocessors, VLSI support chips, ROMs, RAMs and other logic. After verifying such a complex design, the user may further want to develop a test program with high fault coverage for functional testing.

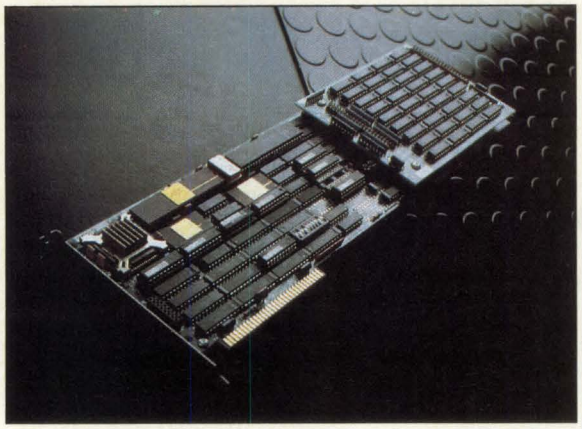
Given the above requirements, the closest and best design analysis capabilities to date exist among companies specializing in simulation technology. These companies provide both design and test simulation tools for complex printed circuit board requirements, including hardware chip modeling and compute engines/accelerators. The solutions provided by most other CAE vendors are inadequate for printed circuit board design/test applications.

Additional growth of the CAE industry will have to be spurred by the printed circuit board market. Until real working solutions for printed applications are clearly available and deliverable, purchases of CAE tools for printed circuit board applications will continue to be light and the CAE industry will remain stalled.

starting at $33,900, boast a 4-Mips performance with a 25-MHz 68020-based CPU.

While 32-bit workstations have declined in price, the power of the IBM PC has been growing. One reason is the prevalence of the AT, which is now available with an 8-MHz 80286 processor and a 30-Mbyte hard disk. A more important reason is the growing use of coprocessor boards that bring 32-bit power to the PC. But even with coprocessors, PCs lag behind 32-bit workstations in networking and graphics capabilities.

Futurenet (Canoga Park, CA) sells the Cadat



Thirty two-bit coprocessor boards from Opus Systems add power to a variety of IBM PC-based CAE/CAD systems. At an OEM price of around $3,000, these 32016- or 32032-based boards run Unix System V and provide 2 to 4 Mbytes of RAM.

logic and fault simulator from HHB Systems (Mahwah, NJ) on a plain AT or on an AT with a Unix coprocessor board. Users can select a 32016- or 32032-based board from Opus Systems (Cupertino, CA). In a recent Futurenet benchmark, the 32032-based coprocessor ran a 5,000-gate simulation slightly faster than a VAX-11/750 and three times faster than the plain AT. While 5,000 gates is pushing memory capacity for an unassisted AT, Futurenet claims that a 4-Mbyte 32032-based coprocessor can handle a simulation of 30,000 gates.

Coprocessors have shown up in a variety of applications this year. Analog Design Tools (Menlo Park, CA) and Valid Logic now run their respective versions of the Spice circuit simulator on the Opus board. Factron EDA (Scotts Valley, CA) runs full-custom IC layout on an AT using the 32032-based Opus system. Lattice Logic (Santa Clara, CA) runs its Chipsmith silicon compiler on a 32032-based coprocessor board from Definicon (Westlake Village, CA). While Opus runs Unix System V, Definicon provides a virtual memory capability for MS-DOS by supplying a virtual DOS interface to the 32032.

Although Hewlett-Packard (Palo Alto, CA) and Valid Logic run all their PC-based applications on coprocessor boards, Mentor Graphics avoids them entirely. While offering schematic capture under DOS, Mentor representatives argue that a fully-loaded PC with a coprocessor board, graphics and networking can exceed the cost of a low-end 32-bit workstation. Daisy also avoids coprocessors, but ports its own version of Unix directly to the AT processor and adds 3.25 Mbytes of RAM and a high-resolution monitor. This fall, Daisy ported its printed circuit board layout, gate array layout and custom IC layout packages to its PC-based Personal Logician workstations.

PC-based suppliers such as Personal CAD (San Jose, CA) and Viewlogic (Marlboro, MA) have decided to avoid coprocessor boards and stick with MS-DOS. Arguing that coprocessors defeat the purpose of the PC, these companies are waiting for Microsoft (Bellevue, WA) to release its long-awaited virtual-memory DOS. This development will remove the current memory limitation of 640 kbytes, the primary restriction for CAE/CAD tools on the PC. Meanwhile, Viewlogic runs its tools in the VAX/VMS environment and recently announced support for DEC's new VAXmate personal computer.

One problem with PCs is the lack of networking capabilities comparable to those of Apollo or DEC. While Apollo or DEC workstations can access files without copying them, PCs must copy files to local memory first. The PC/Network File System from Sun Microsystems now offers an alternative by providing transparent file access under DOS to any platform that uses NFS. Using PC/NFS over Ethernet, a Cadnetix (Boulder, CO) user can sit at a PC and open a Unix window into the Cadnetix Analysis Engine, which provides simulation and printed circuit board routing acceleration as well as hardware modeling.

Until this year, the low end in electronic CAE was defined by PC-based schematic capture packages costing $5,000 or more. Now, schematic capture packages from OrCAD (Hillsboro, OR) and Omation (Richardson, TX) sell for $495 and claim most of the capabilities of the $5,000 systems. Both companies provide mouse-driven packages with pop-up windows and menus, and OrCAD supports color. Capabilities such as design rule checking, net-list generation, printer/plotter output and interfaces to printed circuit board CAD systems are also included.

These new introductions prompted Aptos Systems (Scotts Valley, CA) to offer a $1,000 schematic capture package for the PC. Since Aptos also supports logic simulation and both printed circuit board and IC CAD, this low-cost schematic capture is part of a comprehensive CAE/CAD system. Altera (Santa Clara, CA) has introduced a $975 schematic capture package on the PC for its erasable programmable logic devices.

Low-end packages aren't restricted to schematic capture. Visionics (Santa Clara, CA) sells its EE

Designer package with schematic capture, gate-level logic simulation and interactive printed circuit board layout for just $975. An $895 artwork editor from Wintek (Lafayette, IN) can be used to lay out printed circuit boards, but this product provides no connection with schematic capture or simulation. Such tools may appeal to some board-level designers who hadn't considered CAE.

While the new low-end suppliers have found a market niche, they haven't posed a serious threat to the $5,000 schematic capture products from such companies as Futurenet and Personal CAD. One reason is that $500 schematic capture packages lack extensive library support and connections to industry-standard simulation tools. Another reason is that companies such as OrCAD and Omation are mail-order businesses, while Futurenet and Personal CAD offer extensive service and support as part of their product. Even so, the new low end will put more price pressure on the market and will make life difficult for vendors who want $10,000 or more for a basic schematic capture program.

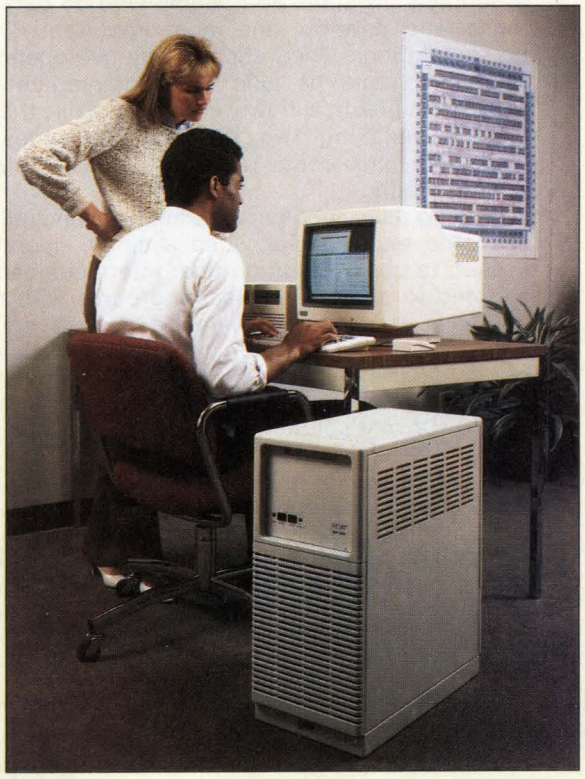
The low-end market has been strengthened in simulation acceleration, where several new suppliers and new introductions have heated up competition. As 1986 began, the third-party acceleration market was held almost exclusively by Zycad (St. Paul, MN) and Silicon Solutions (Menlo Park, CA). While Zycad dominated the high end, the Silicon Solutions Mach 100 engine provided simulation at 250,000 events/s at a base price of $25,000. Now that machine is receiving competition from several simulation products in the $25,000 to $100,000 range.

One new entry is the Ikos 800 accelerator from Ikos (Sunnyvale, CA), which provides speeds ranging from 500,000 to 2 million events/s for a base price of $40,000. This PC-hosted accelerator can run in unit-delay mode at 10 times that speed. Ikos also offers a stimulus-processing accelerator that can generate and store up to 10 million I/O events in local memory. Aida (Santa Clara, CA) offers a Cosimulator Processor for $85,000 that handles up to 1 million gates at 5 million events/s. Part of Aida's Apollo-based CAE system, this accelerator runs Aida's compiled-code simulator.

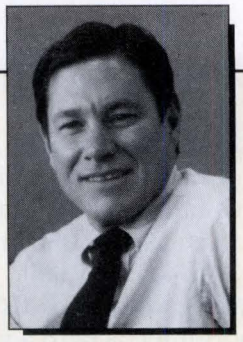
A selection of accelerators ranging from $49,000 to $295,000 was introduced this summer by Xcat (Hopkins, MN). With capacities from 32,000 to 256,000 gates, these accelerators provide up to 2 million events/s. Xcat this fall introduced its MXT-25, a logic and fault simulator that handles 16,000 modeling elements at 2 million events/s. Equating this performance to 1,000 Mips, Xcat claims a price of $39 per Mip with a base price of $39,000 for the machine.

In response to competition at the low end, Zycad brought out a family of low-cost logic and fault simulation accelerators this fall. Zycad's Magnum line offers performance from 25 to 100 Mips at prices ranging from $38,000 to $115,000. These machines are fully compatible with Zycad's high-end accelerators and support interfaces to a variety of CAE workstation and simulation vendors. By specifying speed in Mips, Zycad hopes to avoid confusion over events/s as opposed to evaluations/s, two different measurements of simulation speed.

Special-purpose accelerators aren't the only option for boosting simulation and other computationally intensive tasks. The Dataserver, for example, from Teradyne (Boston, MA) is a parallel-processing system based on the Balance 2100 from Sequent (Portland, OR). With Teradyne proprietary accelerator boards, Dataserver runs Teradyne's Lasar logic and fault simulator 10 to 15 times faster than a VAX-11/780. That's much slower than a dedicated accelerator, but the Se-



The Xcat MXT-25 runs logic and fault simulation at 2 million events/s, equivalent to 1,000 Mips, and is priced at $39,000. Xcat is one of several new companies to join the accelerator market in 1986.



William G. Parzybok, Jr.
Group Vice President and General Manager
Design Systems Group
Hewlett-Packard

Common operating systems will unite design tools

If you assign two talented engineers to a design project, and each speaks a different language, the job will probably get done—but it will cost more, take longer, and be of inferior quality than the same task undertaken by two similarly talented engineers speaking the same language.

Modern companies trying to realize the full potential of linking CAD, CAE and CAM face a challenge just as vexing as the one above. Solutions currently in the marketplace are difficult to link to new products, and new products from different vendors speak in markedly different dialects and languages. AT&T's Unix operating system provides an opportunity to break down the barriers to efficient and effective communication and to link dissimilar products and applications.

Design engineers generally don't care what operating system they use. Well-crafted applications software should make the operating system essentially invisible. The people who do care are those who develop, and more importantly, link these solutions. Theoretically, any two operating systems should be able to accommodate one another. In practice, however, it's more like the engineers speaking two different languages—it takes too long, costs too much, and results in poorer quality.

Serving user needs across multiple disciplines becomes much easier when a single operating system is used. Common user interfaces can be adopted to shorten the learning curve with new software. A common operating system greatly simplifies implementation of industry standards in networking, data base management and other crucial areas to help get fully automated CAE/CAD/CAM solutions to users sooner, and at a lower cost.

But why a Unix operating system rather than some other? Unix operating systems stress backward compatibility with other computers already installed to protect the investment of users. This allows vendors that have adopted it to communicate with a growing installed base in the industry. The flexibility of these systems allows users to add improvements into an existing system without giving up their hardware or software investments. In addition, because Unix operating systems are used by an increasing number of vendors as well as by colleges and universities, the rate of innovation for products using it will continue to be rapid.

Unlike Unix operating systems, proprietary operating systems lock users into a more limited set of hardware and software choices. New solutions will often not be available as soon, if at all. A commitment to Unix is a commitment to the competitive marketplace.

Most leading computer vendors have introduced some form of Unix on at least one of their computers. As it becomes more of a de facto standard, however, vendors must either provide Unix operating systems across the breadth of their product line, or provide only partial and nonintegrated solutions. That would present a serious competitive disadvantage.

Are all Unix operating systems alike? No, they are not. In order to meet the standard, all implementations should use the full System V Interface Definition Issue 1. This definition is supported by the IEEE P1003 Standards Committee, which is working on a single Unix operating system standard for use worldwide. In some cases, like HP-UX, the operating system is in fact a superset, meeting all requirements of the Interface Definition while adding specialized features for those users who are able to take advantage of them.

Today, the two engineers still speak different languages through much of their design task. But the picture is steadily improving. In some areas, they can now communicate effectively. And with further development and adoption of an industry-wide Unix operating system standard, we may soon clear away one of the biggest obstacles blocking our path to the development of the factory of the future.

quent system also accelerates other Unix-based tasks.

A combination of general- and special-purpose acceleration appears in the Cadnetix Analysis Engine. Based on the R2000 series chip set from Mips Computer Systems (Sunnyvale, CA), the CDX-760 GP is a general-purpose accelerator in the Analysis Engine that lets users run net-list compilation or the Spice circuit simulator. The Analysis Engine also includes dedicated bit-slice accelerators for simulation and printed circuit board routing. As an integrated processing node, it includes 40 Mbytes of disk storage and a 68020 processor.

By providing more computing horsepower at a lower cost, simulation and acceleration vendors are making logic and fault simulation more practical

for system designers. Since most simulation products are still used on the chip level, opening the simulation market for board-level applications is one of the greatest challenges for the CAE industry. To that end, virtually every CAE vendor now provides hardware modeling, a tool that allows designers to use physical chips in place of complex, hard-to-obtain software models.

But software modeling has become a more viable alternative with the behavioral models now available from Quadtree (Bridgewater, NJ) and Logic Automation (Beaverton, OR). These models include debugging features that help identify timing errors and cost from $300 to $2,000 each, much less than the cost of hardware modeling. Logic Automation supports the Intel 80386 and Motorola 68000, 68010 and 68020 microprocessors. Quadtree recently announced what it calls the first full-function 68000 and 68010 models, which include a full instruction set implementation and pin-level timing.

Analog system-level simulation took a step forward this year with the introduction of the Saber simulator from Analogy (Beaverton, OR). This simulator runs faster than the Spice circuit simulator and shows a linear increase in CPU time as circuit complexity grows. Moreover, Saber can simulate anything that can be mathematically modeled, including behavioral components of electronic systems. Working toward mixed analog-digital simulation, Sierra Semiconductor (San Jose, CA) extended the VTIsim simulator from VLSI Technology (San Jose, CA) to handle behavioral analog models of Sierra's ASIC products.

The link between simulation and production test was strengthened with the Test Development Series from Test System Strategies (Beaverton, OR), a software package that takes tester limitations into account. The TDS package provides modules for a variety of simulators and testers. Trying to make test generation more feasible, Zycad and HHB Systems this fall introduced automatic test generation programs that can handle sequential logic.

Prototype test systems that compare simulation results to actual response became more abundant in 1986 as several new suppliers joined the market. The ASIC prototype test market is still dominated by the Logic Master from Integrated Measurement Systems (Beaverton, OR), which was recently expanded to handle dc parametrics. But IMS now has competition from the Delta VLSI verification system from Tektronix (Beaverton, OR), the Topaz system from Hilevel (Irvine, CA) and the STM 5100 from Cadic (Beaverton, OR). And Tektronix provides an ASIC verification software package for its new DAS 9200 logic analyzer.

While CAE tools focus on designing and verifying hardware, they generally don't help with the massive amounts of software that goes into today's computer-based systems. Nor can they simulate or test actual software running in a system. One possible exception is Valid Logic's Realmodel, a 500,000-event/s accelerator that comes with a hardware modeling system. Realmodel has enough horsepower to run 100,000 assembly-level instructions in a single simulation.

Hewlett-Packard ported its 64000 software development system to the HP 9000 series 300 workstation this year, the same platform that runs HP's CAE/CAD tools. HP and Tektronix both provide links between their microprocessor development systems and logic simulators. But logic simulation is much too slow for most software designers, and relatively little connection between software and hardware development exists in most design environments. The HP and Tektronix interfaces are used mostly to initialize RAM and ROM modules in logic simulation.

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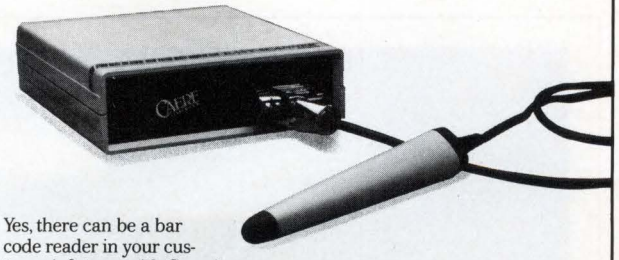

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CIRCLE NO. 40

Hewlett-Packard ported its 64000 software development system to the HP 9000 series 300 workstation this year, the same platform that runs HP's CAE/CAD tools. HP and Tektronix both provide links between their microprocessor development systems and logic simulators. But logic simulation is much too slow for most software designers, and relatively little connection between software and hardware development exists in most design environments. The HP and Tektronix interfaces are used mostly to initialize RAM and ROM modules in logic simulation.

To cope with software-intensive projects, production-quality compilers and source-level debuggers are becoming prerequisites in microprocessor development environments. Thanks to third-party agreements, vendors of PC-based emulators such as Zax (Irvine, CA) and Applied Microsystems (Redmond, WA) now offer such support. Structured analysis and design tools from suppliers such as Cadre (Providence, RI) and Tektronix help designers graphically plan software projects. Performance analysis tools such as the Softanalyst from Northwest Instruments (Beaverton, OR) and iPAT from Intel (Hillsboro, OR) are pointing the way to a new generation of software testing tools.

Driven by price/performance pressure, several products that offer some of the features of in-circuit emulation at a lower cost have become available. The Tektronix Software Executor, for example, allows software debugging with a target microprocessor but isn't hooked up to the target system. Intel's Targetscope doesn't provide hardware breakpoints or logic analysis, but costs less than half of that company's I²ICE emulator. Price/performance is also a motivation for the Echo, a 68000-based development system that provides compilers, source-level debuggers and emulators for less than $10,000 from Arium (Irvine, CA).

The Arium Echo is a self-contained, 68000-based development system that provides compilers, source-level debuggers and in-circuit emulation for less than $10,000. The Echo runs under Regulus, a Unix-compatible operating system.

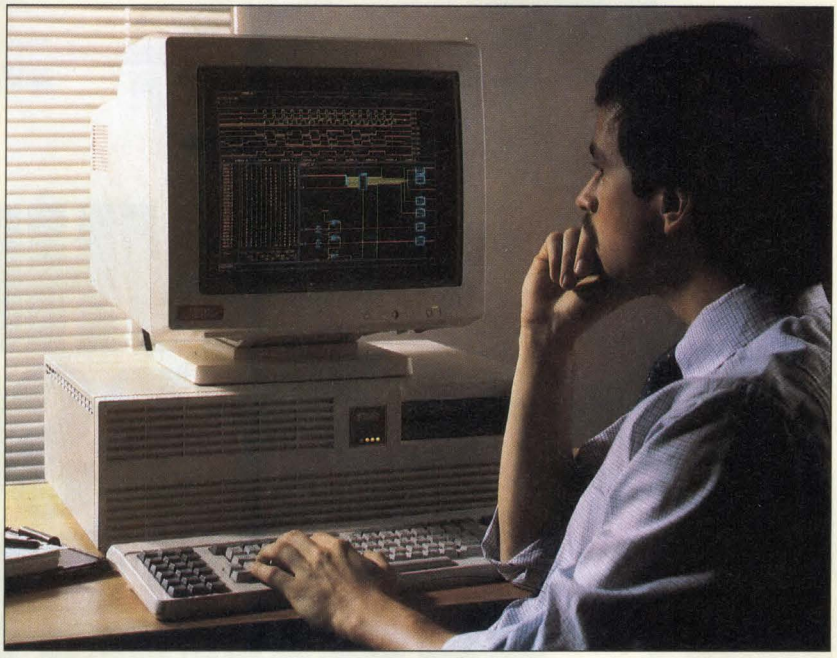
Basic laboratory instructions such as logic analyzers and oscilloscopes are sometimes lost in the limelight of CAE, but are no less important to the system designer. Price/performance was critical in the tough instrumentation market of the past year. The Tektronix DAS 9200 hit a new high in logic analyzer performance, supplying up to 540 channels at 20 MHz, 432 channels at 200 MHz or 160 channels at 2 GHz. But the DAS 9200 isn't cheap—a high-end system can cost over $100,000.

The new T-100 from Outlook (Campbell, CA) supports eight 2-GHz channels and provides up to 250-MHz pattern generation. At prices ranging from $27,500 to $39,000, this PC-hosted analyzer offers up to 100-ps timing resolution and provides several measurement capabilities. These capabilities allow the T-100 to sample within a clock cycle at precisely known locations and to monitor setup and hold violations on every channel. Gould Design and Test Systems (Santa Clara, CA) sells a $5,000 module that provides a 150-ps resolution by taking multiple recordings.

Low-cost logic analyzers from companies such as Arium and Breeze (Broomfield, CO) are offering expanded capabilities and have become major shareholders in the logic analyzer market. Going one step further, new analyzers in the $5,000 to $10,000 range from suppliers such as Philips Test and Measurement (Mahwah, NJ) and Panasonic (Seacaucus, NJ) can offer a considerable amount of power. The Philips PM3570, for example, provides up to 32 channels at 100 MHz, 16 channels at 200 MHz or 8 channels at 400 MHz.

Two powerful digitizing oscilloscopes appeared in November. The HP 54111D oscilloscope boasts a 1-Gsample/s digitizing rate and has a 500-MHz repetitive bandwidth and an 8-kbyte deep memory. Signalling the importance of digital scopes, HP closed out its analog scope line in 1986. The Tektronix 11400 series includes a 500-MHz and 1-GHz oscilloscope with a 10-ps horizontal resolution. These menu-driven oscilloscopes use a touch screen for command entry.

The affordability and power of today's design tools make it even more important to provide an integrated development environment. Buyers want to



The Tektronix DAS 9200 can provide up to 540 channels and speeds up to 2 GHz. This modular system includes a color terminal, ASCII keyboard, hard disk drive and multitasking operating system.

pick and choose the best tools, but the tools must communicate with each other. The move to standard computing platforms by most vendors of CAE, CAD and microprocessor development systems should help. While proprietary hardware can still be purchased from such suppliers as Daisy, Valid and Computervision, most automated design tools now run on workstations from IBM, DEC, Apollo or Sun.

But standard computing platforms aren't the entire story. Apollo's Domain network, for example, is a relatively closed system that makes communications with other vendors' workstations difficult. Taking a different approach, Sun licenses its Network File System protocols to other workstation vendors, including DEC and HP. A standardized operating system is also important. While most CAE/CAD and workstation vendors now offer some version of Unix, VMS still has a large installed base, and suppliers such as Valid and Viewlogic are staying with VMS.

To facilitate the exchange of data among CAE/CAD tools, many users are hoping for continued progress with the Electronic Design Interchange Format. Initiated by semiconductor and CAE vendors, EDIF provides a neutral interchange format for the transmission of design data. EDIF this year was expanded to include printed circuit board data, and the EDIF committee is working toward standardization with the Electronics Institute of America. But few EDIF implementations have appeared in the marketplace.

The integration of CAE/CAD with microprocessor development systems, mechanical CAD/CAM and test and measurement equipment is an even broader goal than communications among CAE/CAD tools themselves. Yet that's the goal that HP has articulated in announcing its CAE/CAD strategy. By adopting schematic capture, simulation and printed circuit board layout tools from third-party vendors, HP has shown itself to be an integrator rather than an originator of design tools. HP representatives believe integration can be achieved through a common operating system and a data base management system.

Most design tool vendors will end up with multivendor systems, and that's where integration and data base management are the biggest problems. To help manage data produced by different vendors' tools, Sherpa (San Jose, CA) provides a VAX/VMS-based system that serves as a central repository for files and provides such features as access control and status checking. The communications problem is addressed by DA Systems (Campbell, CA), which offers a neutral interchange format for CAE systems, CAD tools, manufacturing equipment and automatic test equipment. **CD**

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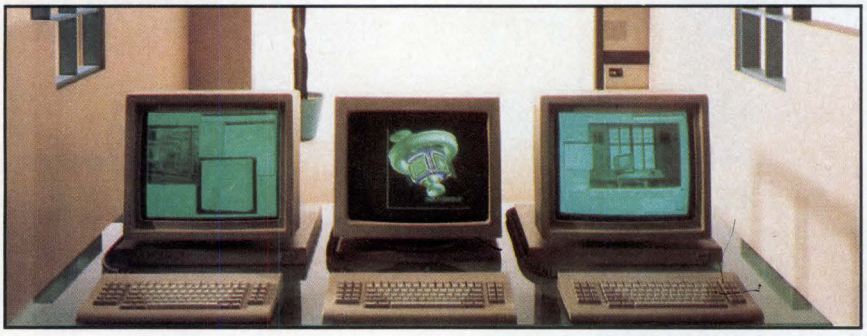
CIRCLE NO. 41

Desktop workstations challenge minicomputers

Claiming performance levels in the same league as the VAX 8600, a new workstation from Sun Microsystems delivers 4-Mips performance and twice the graphics resolution of comparable systems. A low-cost color system featuring a 2-Mips performance rate complements this addition to Sun's workstation line.

Sun's high-end 3/200 series workstations handle compute-intensive tasks with a 25-MHz MC68020-based CPU. By pairing the CPU with a 20-MHz MC68881 floating-point coprocessor, 64 kbytes of virtual address memory cache and a 64-bit processor-to-memory bus, the workstation achieves a 4-Mips, 125-kflops performance level. Basic memory is 8 Mbytes with error checking and correction, but it can be expanded to 32 Mbytes.



Doubling the resolution of existing Sun workstations, a 19-in., two million-pixel monochrome monitor, arranged in 1,600 columns × 1,280 rows, rounds out the system. A 19-in., 1,152- × 900-pixel color or gray-scale monitor is optional.

The 3/200 can be configured in two ways: in stand-alone mode with 280 Mbytes to 1.1 Gbytes of local storage, or without a disk subsystem as a network node that shares file and printer resources via Ethernet. Price for a diskless monochrome version starts at $33,900. When fitted with a 280-Mbyte disk and backup tape drive, the price is $51,500.

Sun's second introduction, the 3/110LC, uses newer technologies such as 1-Mbit dynamic RAM and high-speed video RAMs to mount a color workstation on a single board. Built around a 16.67-MHz MC68020 CPU and a 16.67-MHz MC68881 floating-point coprocessor, the workstation has a capability of 2 Mips. Standard features include a 10-plane color or monochrome frame buffer, 4 Mbytes of memory, an Ethernet interface, two RS-423 ports and the VMEbus interface.

Accompanying this workstation is a standard 15-in. color monitor delivering 1,152- × 900-pixel resolution. A 19-in. color or gray-scale monitor with the same resolution is available as an option.

Similar to the 3/200, this low-end system operates in either stand-alone mode or as a diskless network node. Local storage is configurable from 71 to 142 Mbytes with backup from an optional 60-Mbyte, ¼-in. tape cartridge. Without a disk, the 3/110LC's price starts at $15,900. The same system with a 71-Mbyte disk and backup tape drive costs $21,900.

Sun Microsystems, 2550 Garcia Ave, Mountain View, CA 94043.

Circle 127

Low-cost 32-bit graphics workstations deliver 5-Mips instruction execution

Intergraph's 32C family of graphics workstations operate at a 30-ns instruction cycle time, delivering five times the performance of a DEC VAX-11/780. Instruction execution averages 5 Mips. Built around the 32-bit Clipper microprocessor from Fairchild, these systems are designed for scientific and professional computing applications running in a Unix environment.

For production environments, the Interact 32C features dual screens, an ergonomic design and a built-in digitizing tablet. In contrast, the Interpro 32C comes in a compact desktop configuration for office environments. Both workstations offer 1,184- × 884-pixel resolution on 60-Hz, noninterlaced monitors that can simultaneously display 32 active colors from a palette of 4,096.

Main memory on both systems is 6 Mbytes, with an 80-Mbyte hard disk drive and a 1.2-Mbyte floppy disk drive. Additional features include the basic Unix System V operating system, DEC VT100/220 terminal emulation, and screen management software. Options include compilers for C, Pascal and Fortran.

The Clipper microprocessor provides a full 32-bit internal and external architecture. It actually contains three chips: a CPU with on-chip floating-point execution unit, and two combination cache/memory-management chips (one for instructions and one for data). A dual-bus architecture, with one bus dedicated to instructions and the other to data, links the two cache chips to the CPU.

Network connection components and software permit operation in a network environment.

The Interact 32C is priced starting at $40,000, while the Interpro 32C begins at $25,000.

Intergraph, One Madison Industrial Park, Huntsville, AL 35807.

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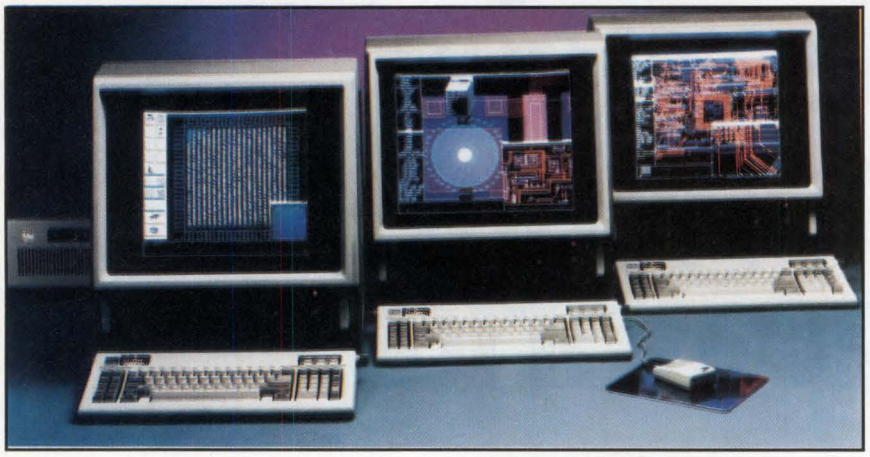
CIRCLE NO. 42

PC-based workstations tackle IC and printed circuit board layout

Although IBM PC-based workstations can handle a variety of CAE tasks, few have ventured into IC or printed circuit board layout. Now, a trio of PC-based workstations handles both design and layout: the Personal Gatemaster for gate arrays, the Personal Chipmaster for custom ICs and the Personal Boardmaster for printed circuit boards.

These turnkey packages run on the Personal Logician, an IBM PC AT-compatible computer that runs the DNIX operating system from Daisy Systems. This proprietary operating system is based on Berkeley Unix Version 4.2. The Personal Logician includes 3.25 Mbytes of RAM, up to 140 Mbytes of memory on hard disk and a Daisy graphics controller. Display options available include a 17-in., 1,024- × 826-pixel monochrome display and a 19-in., 1,024- × 823-pixel color display.

The Personal Gatemaster offers the same tools as Daisy's accelerated Megagatemaster, including schematic entry, pre- and post-layout simulation, timing and test analysis and gate array placement and routing. Included with the Personal Gatemaster is the new Autolayout interface, which automates the complete layout procedure from placement through routing. Designers can execute a layout run by simply typing a Run command.



The Personal Chipmaster offers the same functionality as Daisy's high-end Chipmaster workstation, bringing full-custom IC layout to a desktop workstation. The Personal Boardmaster provides the same features as Boardmaster, Daisy's high-end printed circuit board design station. Tools include schematic capture, printed circuit board layout and verification, and computer-aided manufacturing output.

Complete hardware and software prices range from $40,000 to $55,000 for all three workstations.

Daisy Systems, 700 Middlefield Rd, Mountain View, CA 94039 **Circle 128**

System accelerates logic and fault simulation in software

Using parallel processing techniques, the Dataserver simulation server from Teradyne accelerates the company's popular Lasar Version 6 simulations. The company claims the system provides 10 to 15 times the performance of a DEC VAX-11/780. Every simulation available in Lasar can be accelerated, including good-circuit logic simulation, worst-case timing analysis and concurrent fault simulation. Dataserver also supports any mix of structural, behavioral and hardware models in simulation.

In contrast to hardware accelerators, which encode simulation algorithms on custom ICs, Dataserver operates in software and thereby permits relatively simplified modification and upgrade of Lasar algorithms. In addition, instead of limiting itself to simulation activities, the system includes general-purpose, Unix-based processors to run non-simulation tasks.

Dataserver combines Sequent Computer System's Balance 21000 parallel computer system with hardware optimized for simulation operations. Custom software enables any Lasar simulation job to be executed in parallel.

A base system features two general-purpose and four optimized simulation processors, 16 Mbytes of main memory, a 330-Mbyte storage disk, tape drive, and 16 terminal ports. It can be operated as a standalone host or networked using an Ethernet interface.

The system is easily expanded to accommodate more optimized processors for heavier simulation loads, more memory for simulations of larger circuits, or more general-purpose processors for larger non-simulation loads. Maximum disk capacity per cabinet is 2.4 Gbytes. Depending upon configuration, prices can range from $300,000 to $700,000.

Teradyne, 321 Harrison Ave, Boston, MA 02118. **Circle 129**

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Schematic package sets price/performance standard for PC-based CAD

Creating a new price/performance standard for PC-based CAD, OrCAD/SDT is a complete schematic capture program selling for $495. The package is developed to run on the IBM PC and compatibles. OrCAD/SDT supports most popular graphics boards and printers. Menu-driven operation simplifies the placement of wires, text and graphics symbols. Users select parts by entering the part name from the keyboard or by choosing the part from a pop-up directory where, once it's selected, the part may be easily moved or rotated for placement on the worksheet.

For the repetitive tasks involved in schematic capture, OrCAD/SDT stores over 100 commands and executes them with a single keystroke. Worksheets may be partitioned into manageable parts and then hierarchically organized for easy recall. The system supports worksheets in media sizes from A to E.

A component library with more than 1,200 parts offers all parts used in industry. Devices from TTL and CMOS families, microprocessors, peripherals, memories, and discrete components as well as newly introduced parts are included. A text editor and Symbol Description Language permit simple creation of new symbols or custom libraries.

The OrCAD/SDT system also features real-time rubberbanding of wires and buses, multilevel intelligent zoom, auto panning of worksheet at screen boundary, string searching, and on-line part browsing. The package provides utility programs for schematic output, net listing of signal and part connections, design checking for unconnected pins and signal-line conflicts, and a parts list for the design.

OrCAD Systems, 23315 W Baseline Rd, Hillsboro, OR 97123. **Circle 130**

Simulation engine tailored to small- and medium-size designs

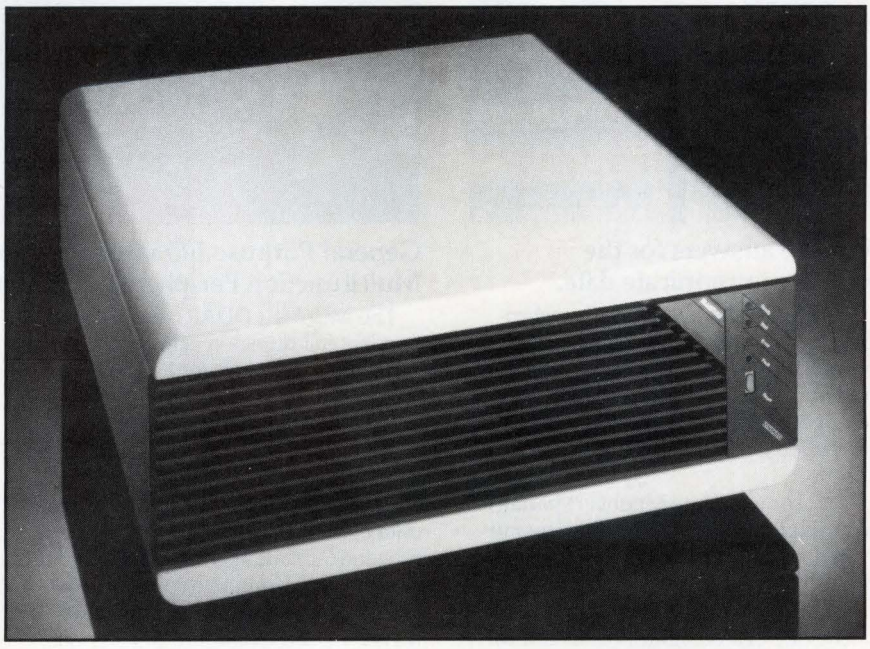
Engineers working on small designs usually cannot justify the cost of a high-end and very expensive logic (or fault) simulation accelerator, yet there is a need for the product. Zycad is trying to meet that need with a low-cost, base model simulation engine specifically intended for designs in the 10,000- to 64,000-gate range. Called Magnum, the engine is available in four different models offering performance at speeds ranging between 25 and 100 Mips for prices dipping as low as $38,000. All four systems interface to a range of CAE systems.

All products in the line are fully compatible with other Zycad product families, ensuring a complete upward migration path. At the entry level, the Model 40 provides a capacity for 16,000 modeling elements at a speed greater than 25 Mips for $38,000. Models 60, 80, and 120 feature capacities of 32,000, 48,000 and 64,000 modeling elements, respectively, at increasing performance increments of 25 Mips each. At the top-of-the-line, the Model 120 provides 64,000-gate capacity at greater than 100-Mips performance for $115,000.

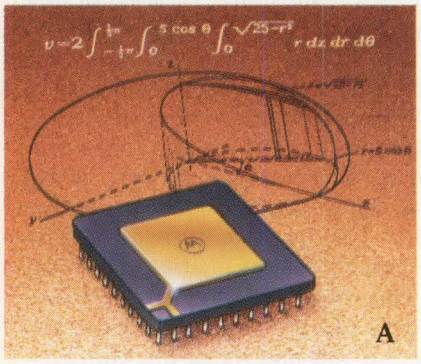
The Magnum family is composed of small units, designed for an office environment and capable of fitting either on top of or beside a desk or workstation. None of the units demand special cooling or power environments. Among the products' features are an optimized, event-driven algorithm, 12-state simulation, delay modeling, accurate timing, unidirectional and wired gate functions, user-definable truth tables, and selectable reporting.

For users with needs beyond basic logic simulation, options for bidirectional switch-level simulation, the Eventlink data exchange package and use of Zilos front-end software are available. Magnum products will offer behavioral and physical modeling options in early 1987.

Zycad, 3500 Zycad Dr, St. Paul, MN 55109. **Circle 131**



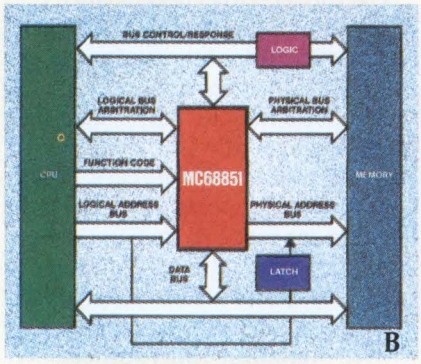
Motorola M68000



Floating point coprocessor has it all.

The MC68881 Floating Point Coprocessor serves M68000 Family and non-Motorola processors with a blend of complete conformance to the IEEE binary floating point standard (754), the four basic arithmetic functions, plus over 40 transcendental and non-transcendental functions including root values, trig functions, logs, exponentials and hyperbolics.

All functions are worked to 80 bits of precision in hardware, and it can break the million Whetstone performance mark.



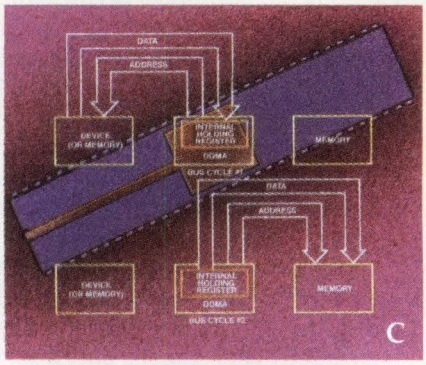
Memory management support for virtual memory environments.

Memory management for M68000 Family processors is performed by the MC68851 Paged Memory Management Unit and MC68451 MMU.

The MC68851 supports a demand-paged virtual memory environment with the high-performance 32-bit MC68020 MPU.

On-chip address translation minimizes translation delays and maximizes system performance.

The MC68451 provides address translation, write protection and task access protection for MC68010-based systems.



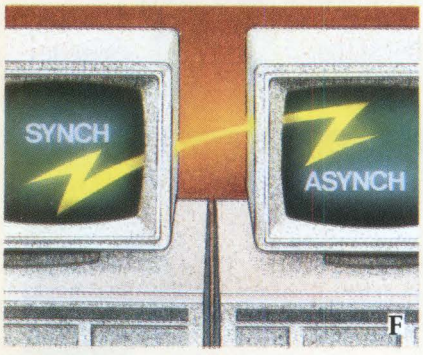
DMA moves and manipulates data on multiple channels.

Three DMA Controllers of varied functionality serve the M68000 Family.

The MC68450 performs high-speed data movement and sophisticated data manipulation in complex systems. It's pin compatible with the MC68440 and '442.

The MC68440 moves blocks of data quickly and efficiently on two independent DMA channels. Channel switching and set up is also very fast.

The MC68442, with extra addressing for 32-bit MPUs, is an expanded version of the '68440.

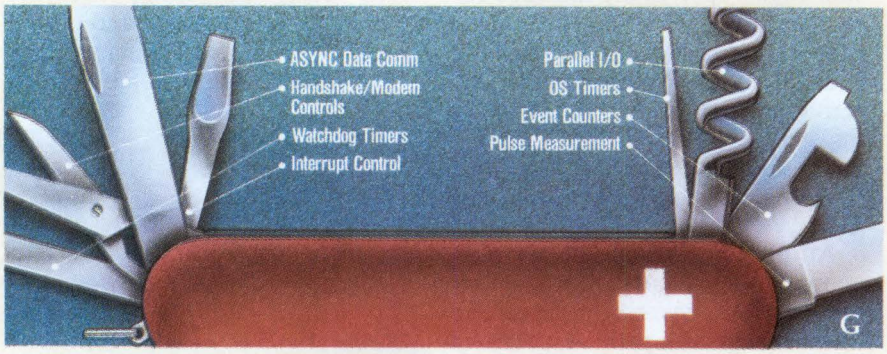


Versatile answers for the need to communicate data.

The MC68661 is a universal synchronous/asynchronous communications controller for M68000 and most other 8- and 16-bit MPUs. Receiver and transmitter are double-buffered for efficient full- and half-duplex operation. No system clock is used.

It can simultaneously convert parallel data from the MPU data bus to transmit-serial data and receive-serial data to parallel characters for MPU input.

The MC68652 is a single-channel serial data device that recognizes byte-control and bit-oriented protocols. It can operate at 2 Mbit/sec.



General Purpose I/O interface supreme, with DUART, Multifunction Peripheral and Interface/Timer circuits.

The MC68681 DUART has two independent full-duplex synchronous receiver/transmitter channels for direct M68000 MPU bus interface.

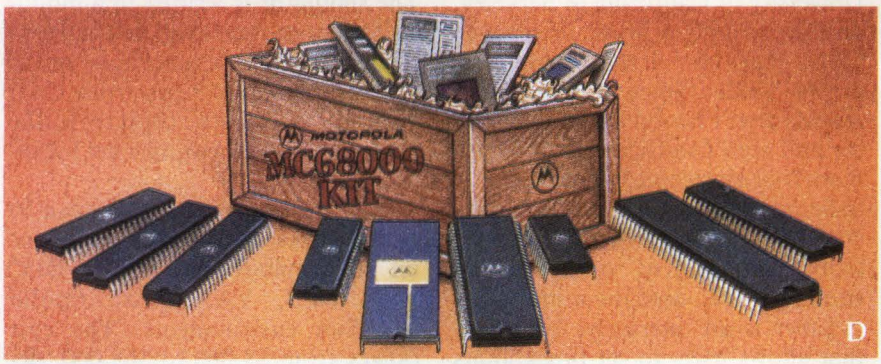
Receiver data registers are quadruple buffered, and transmitter data registers are double buffered to assure minimum MPU intervention. Power for complex data communications is from multi-function 6-bit input and 8-bit output ports, a 16-bit programmable counter/timer, interrupt handling ability and a one-megabyte/sec. maximum transfer rate.

Our MC2681 is otherwise identical, but is without the M68000 bus interface.

The MC68901 multifunction circuit serves microcomputer requirements, via M68000 bus interface, with a single-channel UART for data communications. It has an 8-source interrupt controller, four 8-bit timers and eight parallel I/O lines.

The MC68230 is a programmable interface/timer with versatile double-buffered, unidirectional or bidirectional, parallel interfaces and an M68000 system timer. It also has the full M68000 bus interface.

Peripherals Today



$98 kit demonstrates the performance and versatility of the M68000 Family.

We put together the MC68000KIT and gave it the irresistibly low price of only $98 to make it easy and inexpensive for you to experience the performance and flexibility of the M68000 Family.

It has just what you need to create three basic M68000-based systems.

You get: Three MPUs • MC68000, the general-purpose standard for performance-intensive applications • MC68010 high-performance virtual memory MPU • MC68008, a cost effective 8-bit MPU with the 32-bit architecture of the '68000.

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X.25 Protocol Controller.

Motorola's MC68605 implements level 2 of the 1984 CCITT X.25 Recommendation Link Access Procedure Balanced LAPB.

It independently supports full-duplex point-to-point serial communications up to 10 Mbps generating link level commands and responses. In transparent operation (monitor mode), frames are user-generated with the MC68605 providing HDLC framing and CRC checking/generation.

One-on-one design-in help.

Get an engineer-to-engineer update on designing in Motorola's M68000 Family.

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Call toll-free any weekday, 8:00 a.m. to 4:30 p.m., MST. If the call can't cover your needs, we'll have a local applications engineer contact you.

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MOTOROLA

Chips for MAP Communications.

Motorola's MC68824 is the only single-chip implementation of the IEEE 802.4 Media Access Control sublayer of the ISO Data Link Layer specified by MAP, the GM Manufacturing Automation Protocol.

It supports serial data rates of 1, 5 and 10 Mbps, and relieves the host processor of frame-formatting and token-management functions.

The MC68184 Broadband Interface Controller completely implements the digital functions necessary for an IEEE 802.4 broadband modem as specified in MAP.

Special literature packs supply product and application facts.

M68000 Family product literature has been assembled into three special assortments including brochures, technical summaries and data sheets, benchmark reports, application notes, technical articles, etc.

The M68KPAK is an M68000 Family overview, from chips and software to board- and system-level products.

The M32BITPAK focuses on our 32-bit products featuring the MC68020, with material specific to the subject.

The M68KCOMPAK is oriented to communications, including MAP, X.25, Bisynch, Asynch, etc.

To: Motorola Semiconductor Products, Inc.
P.O. Box 20912, Phoenix, AZ 85036

Please send me the following information on the M68000 Family.

A ☐ Floating Point Coprocessor
B ☐ Memory Management
C ☐ DMA Control
D ☐ Kit Brochure. Kits available from authorized Motorola distributors only. Contact yours.
E ☐ X.25 Protocol Control
F ☐ Communications Peripherals
G ☐ General Purpose I/O
H ☐ Manufacturing Automation Protocol (MAP)
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303CD120186

Analog circuit simulator targets system-level designs

Analog circuit simulation is so slow and difficult to use that it's typically restricted to small pieces of electronic designs. A new simulator announced by Analogy challenges the slow speed, CPU time and modeling problems that have plagued users of analog circuit simulation. Called Saber, this product can simulate anything that can be mathematically modeled, including mechanical components such as sensors, actuators, and motors.

Without sacrificing accuracy, the company claims Saber runs many times faster than Spice, the popular circuit simulation program from the University of California at Berkeley, and shows only a linear increase in CPU time as circuit complexity grows. Unlike Spice models, Saber models aren't bound into the simulator and aren't restricted to low-level models of electronic components. A Saber model, for example, could include a behavioral view of an electronic component or a set of equations that describe a motor.

Saber is an interactive simulator that allows users to set breakpoints and stop and restart simulation. A postprocessor provides a graphical user interface and displays waveforms on the host computer CRT. The simulator is written in a modular format so that it will link easily to schematic capture packages or to graphics postprocessors from CAE vendors. Schematic capture is the preferred way of getting a net list into a simulator.

Saber is designed so that it can be easily accelerated. Saber now runs on IBM mainframes and in DEC VAX/VMS, VAX/Unix, Apollo and Sun environments. The cost ranges from $9,000 to $65,000, depending on the host selected.

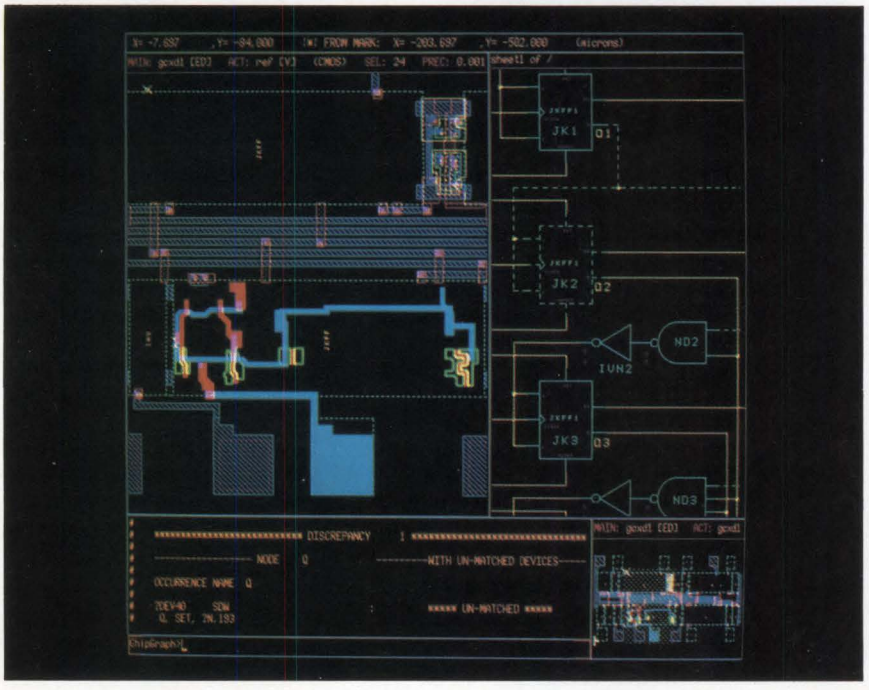
Analogy, 8605 SW Creekside Pl, Suite D, Beaverton, OR 97005.

Circle 132

Debugging program unites schematics, layout and verification

Verifying IC layouts against schematics is a time-consuming, error-prone process that usually requires a lengthy search through a textual listing. A debug program from Mentor Graphics simplifies the verification process by providing a single graphics environment that unifies the output of the schematic editor, layout editor and layout verification system. By introducing Remedi, Mentor Graphics has taken one of the first steps toward integrating the logical design environment with physical IC layout.

Remedi lets users select portions of the layout and see the corresponding sections of the schematic for cross-referencing. Users can also select a portion of the schematic and view related sections of the layout and the error listing, or they can select errors from the listing and display corresponding sections of the schematic and layout. By alleviating the need to shuffle through schematic pages, error listings and layout plots, the program greatly shortens debugging time.



As a visual aid, the program can emphasize the corresponding area of a layout when a schematic net or transistor is selected. If a logic gate or functional block is selected from the schematic, for example, the corresponding layout transistors and nets are highlighted. Remedi opens the door for back annotation of IC designs by letting users view the extracted parasitics and transistors from the layout. These can be viewed as a function of their parameters.

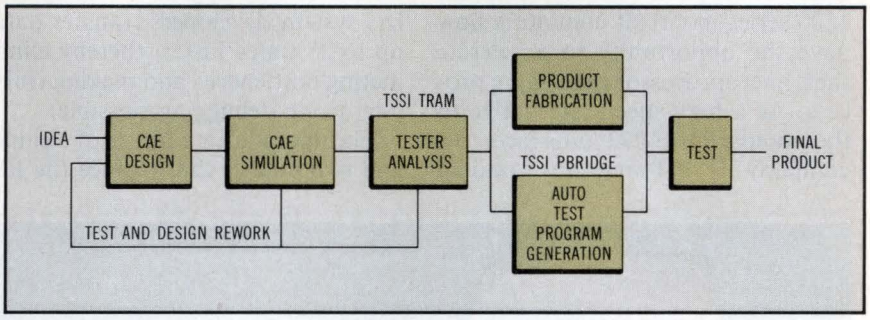
Remedi is primarily geared to the Chipgraph custom IC environment and the Dracula layout verification system from Ecad. Remedi is available for approximately $15,000.

Mentor Graphics, 8500 SW Creekside Rd, Beaverton, OR 97005.

Circle 133

Software shortens design-to-test process

Moving test considerations to an earlier stage in the design process when modifications are easier and less expensive, a software package from Test Systems Strategies ties the simulation data files of CAE systems and test programs to produce test-compatible diagnostics. The test programs generated will run on any targeted tester.



Test Development Series (TDS) software introduces a systems approach to the design-to-test problem by linking the functional verification data provided by CAE workstations with the functional and format requirements of ATE systems. A TDS system contains three modules. Each module supports specific software tools and test equipment in the user's environment.

The first module, Converter, is a first-step conversion program that facilitates translation from CAE-specific waveform files to the TDS standard format. Different Converter modules support a variety of major CAE simulation data formats. These modules can be added to the TDS software whenever data from a new CAE environment must be addressed.

Test Resource Allocation Manager analyzes simulation waveform data to determine compatibility with test equipment. The program creates a report that indicates to the design engineer which areas in the simulation test requirement will not match the selected tester characteristics. Suggested corrections are also provided. This analysis tells engineers whether their design can be tested successfully on the available tester during the design process.

P-Bridge rounds out the TDS series. This software module generates functional test programs for the ATE hardware specified using waveform files from the CAE simulator. The programs that are created include statements to generate a real-time stimulus and to verify the response of the device under test. As a result, a programming task that usually takes weeks can be completed in hours.

Test Systems Strategies, 8285 SW Nimbus Ave, Beaverton, OR 97005. **Circle 134**

Tool set completes CAE software environment

Providing the missing piece to its integrated tool set for software development, Tektronix has created Structured Design (SD) Tools. This set of graphics-oriented software development tools automates the overall design of a software system. By combining these tools with the company's existing Structured Analysis (SA) Tools, users can configure a complete package of automated software development tools covering every phase from requirements analysis to software/hardware integration and testing.

SD Tools encourages design creativity by allowing rapid changes within the software structure without requiring tedious drafting revisions. By offering a systematic graphics method to diagram the overall design of a software system, the package graphically partitions software modules in a hierarchical structure that displays their communications interfaces and controlling relationships. Functions such as transforming and drawing diagrams, organizing documents and making copies are automated.

The data source for SD Tools is SA Tools. Transformation tools, built into the SD Tools process, automatically convert data-flow diagrams created with SA Tools to a structure chart. A special-purpose interactive graphics editor lets designers create and modify structure charts on-line. Using this editor, designers can create, label, move and delete each type of symbol in the structure chart.

The SD Toolkit includes software tools, installations, an interface to the Tektronix Colorkey+, on-line documentation, a keyboard overlay, a user's manual, and a reference book. The system runs on VAX and MicroVAX computers running under VMS and Unix/Ultrix operating systems. SA Tools will soon be available on Apollo Domain and IBM PC-DOS and can be used in an integrated environment with VAX computers and workstations.

Tektronix, PO Box 500, Beaverton, OR 97077. **Circle 135**

Coming January 1
Watch for Bill Suydam's Special Report on computer-aided software engineering

SCSI option enhances interactive potential of emulator family

Users of Applied Microsystems' ES 1800 series in-circuit emulators now have the opportunity to accelerate their microprocessor debugging process. As a high-speed alternative to the standard RS-232 interface, the company is offering an optional SCSI interface upgrade. This option lets system developers transfer data up to 35 times faster, thereby eliminating bottlenecks and making truly interactive debugging possible.

The upgrade kit consists of a cable and two boards that replace the ES 1800's controller and main controller boards. Accommodating a variety of hosts including the IBM PC family and Sun Microsystems, Digital Equipment Corporation, and Apollo platforms, the SCSI interface opens up a range of design applications.

Potential applications include any situation requiring real-time visibility and control for designing and debugging complex systems. The increased data-transfer speed permits interactive debugging, even with high-performance 32-bit microprocessors. Debugging performance is typically enhanced by 10 percent.

Additionally, when used as an instrumentation bus, the interface connects to several devices for multiuser configurations. In a multiuser setup, any of eight units can act as initiators, with either an emulator or a host acting as the controller.

Pricing for the two-board option, with a revised host software package, starts at $3,995 per set.

Applied Microsystems, PO Box 97002, Redmond, WA 98073. **Circle 136**

Software tool gives expert know-how to novice designers

Using a rule-based, expert system to improve completion rates on the first board layout, the Insight router from Telesis is targeted at printed circuit board designers who aren't familiar with automated routing techniques. According to Joseph Prang, marketing support manager for the company, first-time users can deliver the same results promised in benchmarks and product demonstrations. Using Insight, users need only input the board's physical characteristics, such as the board's dimensions, the minimum spacing permitted between lines and the number of signal layers desired.

Routing has been optimized through the adjustment of approximately 30 costing factors in the product's maze and line probe algorithms. Insight automatically sets such costing factors as grid size, with specification down to 1 mil; via grid, which reserves specific grid locations for placement of vias; and pin keep-away, which leaves routing channels open to facilitate the automatic placement of etch and future engineering change orders.

Standard features include automatic 45° routing, fine-line routing features, variable grid capability and up to 14 signal layers available for automatic routing.

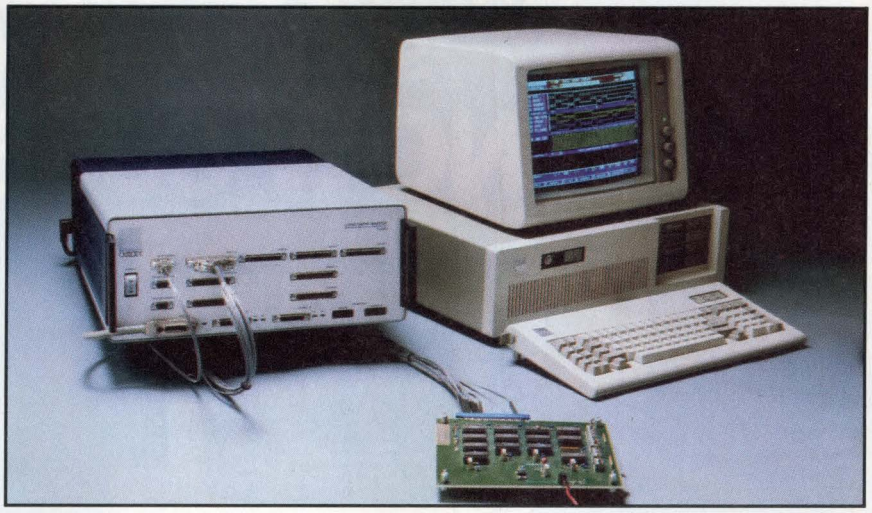
The system also aids the novice by preplanning the design so that the final product offers the same patterning and aesthetic quality found on designs from skilled users. One way this is accomplished is through the independent handling of horizontal and vertical connections, which enables the completion of over 50 percent of all connections without using any vias. Unlike traditional rip-up routers, which arbitrarily destroy and then place connections until a solution is found, Insight avoids potential blockages and designates legal via sites early in the design process.

All routing algorithms were developed using Prolog, a programming language used extensively in artificial intelligence applications. The router complements Telesis' EDA-3000 Design Application software and will be available as part of the entire turnkey PCB Design Workstation package.

Telesis Systems, Two Omni Way, Chelmsford, MA 01824. **Circle 137**

Logic analyzer provides unique measurement capabilities

A new approach to logic analysis provides a 100-ps timing resolution, up to 2-GHz acquisition speeds, 250-MHz pattern generation, and several new measurement capabilities. While most logic analyzers provide extensive features for software analysis, the Outlook T-100 is claimed to be the first logic analyzer aimed specifically at high-performance hardware design.



One unique feature of the T-100 is its ability to monitor setup-and-hold violations on every channel. This lets users detect a problem that won't necessarily cause a test to fail, but may cause hidden problems in device operation. The T-100 can trigger on a setup-and-hold violation within a −5-ns to +15-ns window in 100-ps increments.

The T-100 provides synchronous recording with an external clock that can run up to 250 MHz. If the external clock provides a square wave instead of pulses, the T-100 can handle synchronous recording up to 350 MHz. While most analyzers only run synchronous channels up to 25 or 50 MHz, Outlook's synchronous recording lets the user synchronize the analyzer with the clock in a high-speed system. The T-100 also introduces three new modes of synchronous recording: synchronous harmonic clocking, phase-shifted harmonic clocking and equivalent time recording.

In the equivalent time recording mode, the analyzer makes multiple recordings of repetitive data, shifting the sampling clock by 100 ps for each recording. The samples are then assembled in the analyzer's memory, giving a composite recording that's equivalent in resolution to a 10-GHz sampling rate. But this mode won't catch single shots because it requires multiple recordings. Nonrepetitive data can still be sampled at 500 ns with the T-100's 2-GHz asynchronous recording.

The T-100 can provide four asynchronous channels at 2 GHz with 32-kbit deep memory, eight channels at 1 GHz with 16-kbit memory, 16 channels at 500 MHz with 8-kbit memory, or 32 channels at 250 MHz with 4-kbit memory. Users can change the input configuration by typing a command from the host computer keyboard. When the analyzer is set up for 32 channels, a transition timing mode can store inputs that have changed since the last transition and display a timing diagram using time tag information.

The T-100 uses an IBM PC host to provide a user interface to the logic analyzer. Its minimum requirements are an IBM PC XT with 640 kbytes of RAM, an Enhanced Graphics Adapter card, and a high-resolution color display. Price, excluding host, is from $27,500 to $39,000, depending on the probe sets ordered.

Outlook Technology, 200 E. Hacienda, Campbell, CA 95008.

Circle 138

Digitizing scope attains 1-Gsample/s rate

Intended as a digital alternative to analog-storage scopes in the 250-MHz bandwidth range, a digitizing oscilloscope from Hewlett-Packard, with a 500-MHz repetitive bandwidth and 8 kbytes of memory, boasts a 1-Gsample/s digitizing rate. Similar to the previously introduced HP 54110D, the new unit—the HP 54111D—combines a digital architecture with a crystal-controlled time base.

The 54111D attains its high digitizing rate by incorporating five new parts. These include a GaAs track-and-hold circuit, a high-speed bipolar A-D converter, an NMOS timebase chip, an NMOS 2k-×8-bit memory, and a 1-GHz saw oscillator. Its 1-Gsample/s digitizing rate translates into a 250-MHz single-shot bandwidth, letting it capture glitches as narrow as 1 ns wide. A variety of analysis features combined with its 8-kbyte memory let scope users compress, expand and measure waveforms or position the window in positive or negative time with respect to the trigger.

Additional features include a color display with 4,096 colors, variable-to-infinite persistence displays for worst-case analysis, pre-trigger viewing, instant hard copy output and a variety of setup aids to simplify time-domain measurements. The price of the scope is $23,900.

Hewlett-Packard, 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 139

MICROTEK DOES IT AGAIN

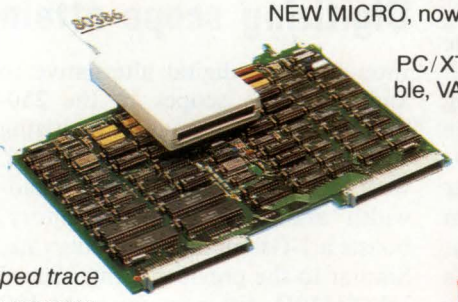
...AT THE LEADING EDGE

SUPER 8, 68020,

NOW 80386!

The Intel 32-bit 80386 microprocessor has arrived, and is set to play an important role in high-end, high-performance products. Due to wider buses and higher clock speeds, complex 80386 target systems now require more powerful developing and debugging tools. Selection of a good development system and emulator will be critical in determining whether or not 80386-based products are completed on schedule and within budget.

MICROTEK'S U.S. service, sales and marketing arm, NEW MICRO, now has the MICE-32/80386, a portable emulator that can run with any IBM-PC/XT/AT personal computer or compatible, VAX, and MicroVAX through parallel or serial interface. Or can stand alone with a terminal.



Look at these features:

- *Completely self-contained standalone emulator*
- *User-friendly command structure*
- *Emulation to 32 MHz*
- *"Snapshot" conditional, time-stamped trace*
- *256K Bytes soft mapped emulation memory*
- *Powerful symbolic debugger with user definable procedures under PC/MSDOS, VMS and ULTRIX.*

Other processors supported by Microtek

80286, 80186, 80188, 8086, 8088, 68000, 68010, 68008, Z80, NSC800, 8085, 6809, 6809E, 6502 (40 and 28 PIN) 8032, 8051, 8031, 8344, 8048, 8049, 8050, Z8, SUPER 8

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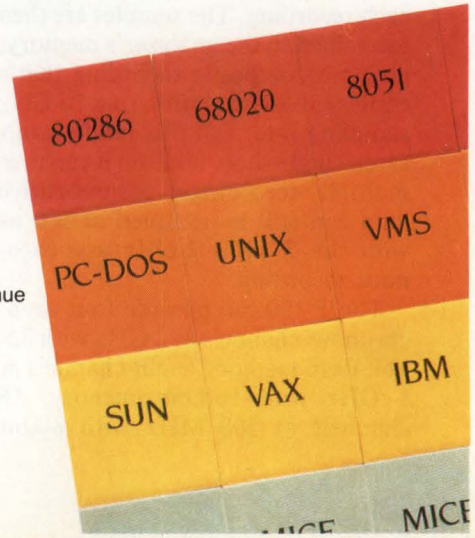

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Graphics developments geared toward speed and capacity

Advances in graphics technology provide far-reaching cost/performance improvements.

Tom Williams
Western Managing Editor

As with computers themselves, the quest for increased speed and capacity was the overriding concern this past year in all areas of peripherals, including output devices such as printers and plotters, mass storage systems such as hard and optical disks, and tape drives. Speed and capacity concerns also have dominated the main mode of user/system interaction—graphics technology. The goal has been to obtain higher resolution, more color, and real-time interactivity, including the compute- and display-intensive modeling of solid objects.

In 1986, there was a dramatic series of developments in graphics technology that will have far-reaching impact on the cost/performance ratio, and thus the accessibility to users, of a vast range of computer systems. These systems include general business and office systems, personal workstations, in both electrical and mechanical CAD/CAM/CAE and a wide range of other more specialized systems, including factory automation and military command and control.

Although these advances have taken place in both hardware and software, the basis for the rapid development has been silicon. Major semiconductor manufacturers have created a new generation of graphics display processors, but hasten to assure everyone that even these advanced chips are not the last word.

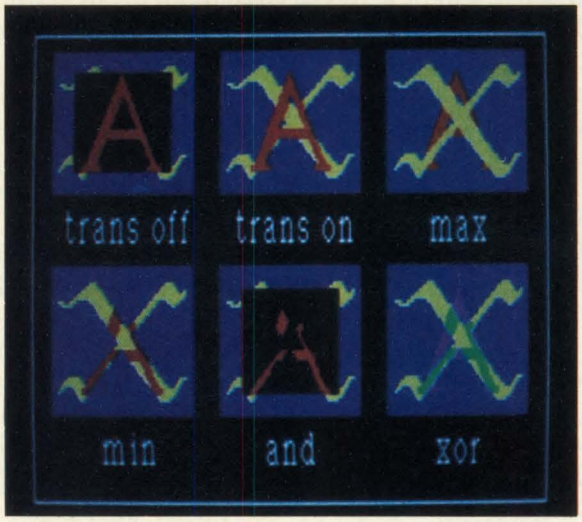
Graphics technology depends on two types of processing power for its performance. First, it requires high-speed floating-point computing to calculate the scale, rotation, clipping and perspective of an object. Second, it requires powerful integer processing to write the data into the pixel positions in the frame buffer and to manipulate it within the frame buffer.

The demand that graphics places on math-intensive processing power has been lessened by more general-purpose processors, math

coprocessors, floating-point accelerators and digital-signal processing chips. These parts are needed to supply the large amounts of data to support the virtually insatiable demands of high-speed, high-resolution graphics. On the display end, a new generation of display controllers has emerged. Several of the newer devices are processors in the sense that they fetch and execute their own instructions. These devices include the TMS34010 from Texas Instruments (Dallas, TX) and the 8500 raster graphics processor and support chips from National Semiconductor (Santa Clara,CA).

While one kind of display processor exhibits a high degree of software programmability, another group relies on a relatively small number of high-level macro commands to perform graphics functions. These include the HD 63484 advanced CRT controller by Hitachi (Tokyo, Japan), the 95C60 quad-pixel dataflow manager (QPDM) by Advanced Micro Devices (Sunnyvale, CA) and the 82786 by Intel (Santa Clara, CA). These devices depend on receiving their instruction stream from a host processor. But, the small number of instructions needed to perform high-level graphics functions gives a speed boost that, to some degree, compensates for their dependence on a host.

Whatever their level of programmability, the new generation of display processors represents a consensus on the types of drawing and display functions expected of today's graphics systems. These include line, arc, polyline, polygon and area fill functions and, perhaps most significantly, the use of bit boundary block transfer (bitblt) operations for both text and graphics operations. Since bitblt involves moving $n \times m$ matrices of pixels to arbitrary positions in the frame buffer it requires access to individual pixels and must cross memory word boundaries. Bitblt text involves copying characters from a font stored in a nondisplayed area of the frame buffer to a displayed area, while often coloring, scaling and/or rotating the characters in the process.



Pixblt operations allow various image combinations, including (clockwise from upper left) replacement with transparency on or off, maximum or minimum, and AND or exclusive OR.

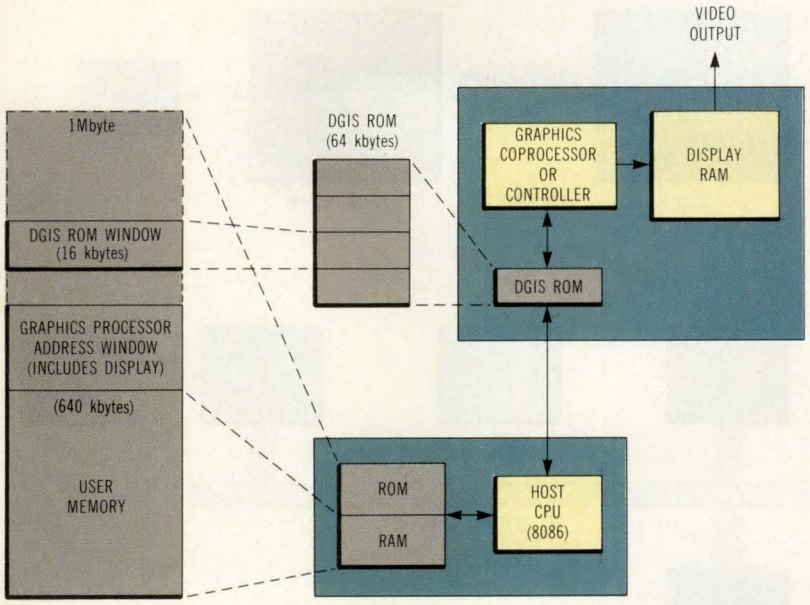
The chips mentioned differ widely in their programmability, the number of bit-planes they can control, their approach to windows, the way they address the bit-map (as pixel planes or as a single-linear address space) and their implementation of bitblt. There are also a number of cost/performance choices for the system designer in terms of the need for a host processor, the number of support chips needed, and so forth. Despite this wide differentiation that forces graphics system designers and graphics software designers to make a host of choices, the display processors make their jobs much easier.

When board-level graphics products are finally based on a small number of display processor ICs, the system designer's task will be to determine how the chips can be used to create a different value-added product. One way will be the development of innovative software. With a limited number of highly functional display control ICs, board makers will have less trouble providing device drivers for their products, implementing the drivers mainly in terms of the chip's instruction set. Third-party software developers will also be able to address a large part of the market by making sure that their products can communicate with this potentially large subset of hardware.

One example of such a development is the Direct Graphics Interface Specification (DGIS) developed by Graphic Software Systems (Beaverton, OR). The applications program can talk to a standard set of commands provided by DGIS. This command set is similar to that specified in the proposed Computer Graphics Interface (CGI) standard. DGIS is a ROM-able software package for MS-DOS that translates this standard command set into the instructions for the particular hardware for which it is adapted—usually a display controller IC. As a result, any application that has a DGIS driver can talk to any hardware for which DGIS has been adapted.

Similar steps are being taken to ease the writing and maintaining of device drivers in Unix. A product called Terminal Graphcap by Visual Engineer-

The host communicates with a typical PC-based graphics controller via a 16-kbyte portion of its DGIS ROM that is mapped into system ROM space. The rest of the 64 kbytes of DGIS are outside system address space. Both the applications software and the controller communicate with DGIS and with each other via this ROM window.

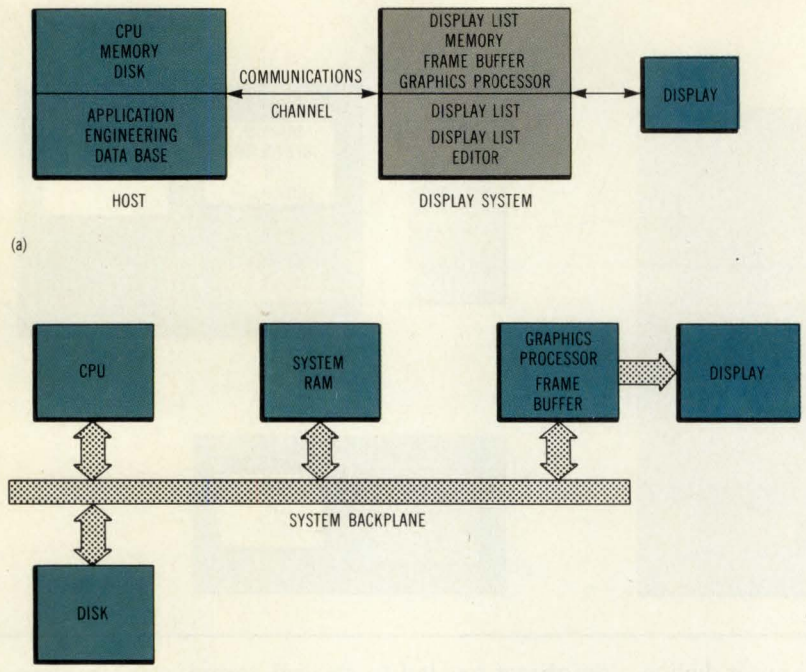


ing (San Jose, CA) lets the programmer enter device characteristics and parameters via a text menu. The resulting text file is then compiled to a binary personality file. The application accesses a standard driver, which then calls the personality file (containing the specific device parameters) to "fill in the blanks" for the particular device being accessed. Personality files for new but similar devices, such as models with enhanced features, can be created by editing the old text file and recompiling it under the new device name. Precision Visuals (Boulder, CO) has a similar method for creating device drivers but keeps it in house. Precision Visuals develops and supports drivers to enable a wide range of graphics hardware to run its graphics software products.

Developments in hardware—silicon as well as workstation architecture—are influencing the ongoing efforts to establish graphics software standards. Having settled on at least one standard for two-dimensional graphics—the Graphical Kernel System (GKS)—the industry is now grappling with the need for a three-dimensional standard. So far the options have been to create 3-D extensions to GKS or to go to a different standard altogether—the Programmer's Hierarchical Interactive Graphics Standard (Phigs). While both options have their proponents and are being actively pursued, Phigs has a ready-made compatibility between the display list used to draw objects on the screen and the data base used to represent the computer model of the actual object.

The need for an interactive link between a hierarchical data base and the hierarchical display list of an object has led to several commercial implementations of Phigs although no official national or international standard has yet been adopted. These implementations include the Figaro product from the Template Division of Megatek (San Diego, CA), the Gbase system from Genisco Computers (Costa Mesa, CA) and the DI-3000-XPM package from Precision Visuals. The attraction of linking data and display with a Phigs-like model has also forced some manufacturers to add accellerators or hardware tree traversers to speed up traversal of both display list and data base structures. The DN 580 workstation from Apollo Computer (Chelmsford, MA) not only has hardware support for tree-like display lists, but also lets the display list spill out into virtual memory, so theoretically, display commands and data could coexist in the same file.

Advances in workstation architecture, such as Apollo's, are causing some workstation manufacturers to question the idea of a graphics standard that generates a separate display list. The need to generate such a list comes from the days when a display device was connected to the host via a serial channel. Today's workstations have integrated the host processor and display subsystem in one box, and they communicate over a high-speed system backplane. Manufacturers of high-end systems, such as Silicon Graphics (Mountain View, CA), believe that all that's really required are drawing primitives that can be integrated with the application and data base to display the computer model of an object in the data base, with the user modifying



Remote display systems (a), even those with the ability to edit graphics locally, required the compilation of a separate display list because the data to be displayed had to be sent over a slow channel. A modern workstation architecture (b) contains all programs—engineering data base, applications, graphics routines and graphics editor—locally. All transfers take place across the system bus or via even faster private buses for graphics, eliminating most of the need for a separate display list.

it by interaction with the display in real time.

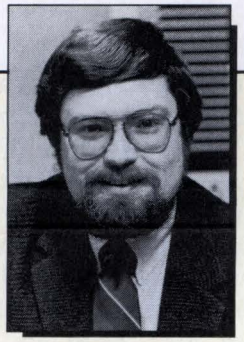
Advances in silicon, particularly in math processors and digital signal processing (DSP) chips, have also helped bring image processing out of the research lab and into the realm of affordable applications. These applications, which include systems for machine vision and undersea exploration and reconnaisance, require the ability to do contrast and edge enhancement, which need spatial filtering. Spatial filtering relies on the ability of the image processor to perform eight or more multiply-accumulate operations, called convolutions, on every pixel in the display or on every pixel in an area of interest of the display.

Board-level products for the IBM PC AT and compatibles and for the DEC MicroVAX demonstrate the ability to perform for image acquisition and spatial filtering on images of 512- × 521- × 8-bit pixels in less than 1/30th of a second—essentially in real time. Manufacturers such as Datacube (Peabody, MA), Imaging Technology (Woburn, MA) and Data Translation (Marlboro, MA) not only have shrunk image processing down to board sets, but also have produced boards that represent modular functions. These boards allow a system designer to make cost/performance tradeoffs and to include a subset of image-processing functions (such as image capture, histogram generation and convolutions) that are important to the specific applications needs.

Regarding storage, Winchester disk drives continued their push for increased capacity and lower cost per Mbyte. The disk that currently has the largest capacity in a 5¼-in. form factor is the 760-Mbyte XT-8760E from Maxtor (San Jose, CA). On the lower end of hard disk capacities—disks with a capacity of 40 Mbytes and below—the 3½-in. form factor appeared to be offering a stiff price/performance challenge to the 5¼-in. drives that had dominated that capacity range. Even floppy disk technology managed to advance into the 10- and 12-Mbyte arena that was formerly the domain of Winchesters. A drive introduced by Eastman Kodak (Rochester, NY) used a 5¼-in. cartridge similar to that used in 3½-in. floppies to achieve 12 Mbytes of storage.

Refinements in media and servo technology have been one reason for the increased capacity. Another factor has been the advances made in controller electronics. Controllers that use run length limited (RLL) encoding can increase a drive's capacity by 50 percent without any change in track density or flux reversals per inch on the medium. RLL controllers are being supplied as separate products by companies such as Adaptec (San Jose, CA), but are also being embedded directly in drives along with the drive electronics.

Economies of scale, coupled with increased inte-



Thomas B. Clarkson, III
Chairman
Graphic Software Systems

The impact of high-performance graphics technology

Analysts speculated a year ago that graphics processor chips would lead to dramatic performance improvements in desktop computer graphics. Now, graphics processor chips are here, and board designers are incorporating them into a new generation of powerful graphics display boards and printers for desktop computers. By the middle of 1987, end-users will have graphics hardware and applications software packages that provide several times the graphics price/performance found in current desktop products.

Graphics have grown into an integral part of desktop computing, and silicon companies are investing substantial resources in making graphics processors part of the overall computer system architecture. These graphics processor chips are regarded by many as the solution to the graphics performance problem. Performance is the key issue in desktop computer graphics and will remain so because applications developers will always want to do more with graphics.

Today, three graphics-based applications areas are generating a great deal of excitement: visual user interfaces, desktop publishing and PC-based CAD. Each application is stifled by the graphics performance provided by today's desktop computer systems.

Currently, the PC industry has decided on the IBM Enhanced Graphics Adapter (EGA) as a de facto standard hardware model for graphics applications compatibility, even though the EGA is inadequate to meet the graphics-intensive needs of visual user interfaces, desktop publishing and PC-based CAD. The resolution is marginal, the number of colors is limited and the performance is unacceptable for software that relies heavily on interactive graphics.

Graphics processors improve graphics performance because applications can off-load graphics tasks to the intelligent board. Graphics processors become increasingly important as applications developers take advantage of increased resolution and number of colors. But because raw CPU power increases so much more slowly than the demand made by increases in resolution and the number of colors, users are no longer satisfied with those devices where the CPU does all the graphics operations. For example, a 1,280-×1,024-×8-pixel display board has 82 times as many disks as a 640-×240-×1-pixel display board, so it's unrealistic to expect the 80386 to do graphics operations 82 times as fast as an 80286.

The industry is converging on three significant graphics processor chips: the Intel 82786, the Hitachi ACRTC and the Texas Instruments TMS-34010. These chips represent two major design approaches for graphics silicon: fixed-function (the Intel and Hitachi chips) and programmable controllers (the TI chip).

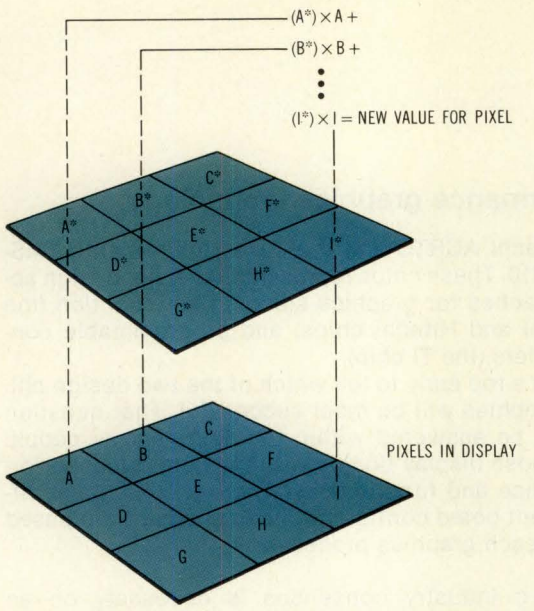
It's too early to tell which of the two design philosophies will be most successful. That question will be answered within the next year as people choose display boards with the best price, performance and functionality. There will be many different board configurations to choose from based on each graphics processor.

An industry consensus is necessary on an extended, high-performance compatibility model because the growth of graphics processors is as important to desktop systems today as the growth of microprocessors was 10 years ago. A recent step toward such a consensus is the Direct Graphics Interface Specification.

DGIS offers applications program developers a consistent way to deal with graphics boards incorporating graphics processors. Any board with DGIS firmware will support any application with a DGIS driver. Even future boards with graphics processors will support today's DGIS-compatible applications. DGIS device drivers are also being developed for most of the leading PC applications packages as well as for Microsoft Windows (and all software operating with Windows) and for the computer graphics interface-based Graphics Development Toolkit packages (and applications developed with them).

Board design and integration with the PC are major determinants in achieving high performance with graphics processors. There are two main board-design considerations that pertain to maximizing graphics performance through graphics processors: bandwidth to the graphics processor, and true coprocessing vs. lockstep operation. The width of the communications path, number of wait states, shared memory design, and memory contention affect bandwidth, thus, affecting performance and board design. It's important that the hardware and interface design exploit the parallel architecture of separate graphics processors. Each processor shouldn't spend too much time waiting for the other.

As the compatibility model and board configuration issues are resolved, the new graphics technology promises to transform desktop computing. The industry can look forward to more graphics-based applications, greater ease of use and richer expression of computer-based information for the future.



To perform a 3×3 convolution for a spatial-filtering operation on pixel E, a mask or kernel is applied to the pixels surrounding it. Each pixel in the neighboring array is then multiplied by the value in the corresponding position of the kernel. The results are summed and become the new value of pixel E.

gration of functions on silicon, have also made it possible to embed the disk controller on the drive. Controllers that use the Small Computer Systems Interface (SCSI) have, as a result, become "standard" disk drives that can essentially plug directly into any system incorporating a SCSI bus interface. In addition to the cost savings that have been made on board space, embedded controllers have let drive manufacturers pursue value-adding enhancements to their products behind the anonymity of a standard interface due to backplane slots and faster integration of drive products.

For example, embedded controllers allow elimination of transciever ICs used to communicate between drive and controller electronics and allow use of a single microprocessor for both drive and controller. They also allow the manufacturer to pursue innovative approaches to error correction and defect mapping without impacting the host system and software.

Of course, with SCSI currently limited to a transfer rate of about 1.25 Mbytes/s in its asynchronous mode, it's less attractive for the needs of systems requiring more than 300 Mbytes of storage. Systems with high-performance buses, such as the VMEbus or Multibus II, tend to use 5¼-in. drives in the higher capacity ranges. In this case, it makes sense to find a better performance match with the Enhanced Small Device Interface (ESDI) or the Intelligent Peripherals Interface (IPI), both of which can run about 10 Mbytes/s. While integrating ESDI or IPI isn't as straightforward as integrating SCSI, the performance bought with the higher speed ESDI and the added intelligence of IPI will give those interfaces dominance over SCSI in high-performance systems.

IPI seems to hold promise, especially for system designers who wish to match high-capacity disk and tape devices to high-performance system buses. Defined in three levels, the IPI-2 device-level interface is expected to show up in commercial systems in 1987. IPI-3 combines the physical interface definition and logical command protocol needed to run storage devices without much intervention from the host CPU. IPI-3 will allow the host to move a queue of commands and format parameters to the peripheral and let it run without intervention. It also allows more formatting functionality to be done off-line for high-end tape backup systems than the more disk-oriented ESDI.

Although no one has yet invented a controller tailored to the specific needs of optical storage devices, that hasn't stopped the idea from entering into the plans of system designers or kept them from using available controller technology such as SCSI. And the fact that read/write technology for optical drives hasn't been perfected hasn't slowed anyone from finding applications, either. Optical media is finding applications both as read-only (as in the CD ROM) and as write-once, read-mostly (WORM) technology. In fact, the vast capacities offered by optical drives are causing some people to find applications for computer systems that were not previously possible.

CD ROMs are being used, for example, to store chemical and electrical engineering abstracts and articles, an entire encyclopedia set along with an index to each word in the 20-volume set, and a data base of poisons and antidotes for emergency treatment centers. WORM drives are very useful in applications where data doesn't change often and where audit trails are needed to trace data updates, such as in banking and insurance operations. A WORM application would generally flag the system to read the latest update, but pointers are available to lead back through all changes. One factor hindering writable optical storage technology is that it's difficult to increase the data rate beyond the rotational speed of 1,800 rpm—the time needed for a laser pulse to deliver enough energy to burn a

spot in the media.

While all these alternative applications for optical drives may be very useful, everybody is really waiting for the erasable read/write drive. Most forecasters believe the technology can be perfected and should be available in commercial products within four to five years. Until then, the market will be kept alive by finding innovative and useful applications for the present technology.

Despite all the interest in optical storage, the cartridge tape remains the backup system of choice for Winchester disks. Although there is a genuine effort to establish format and interface standards for cartridge tapes, manufacturers are competing to cram more storage into a smaller space at a lower price.

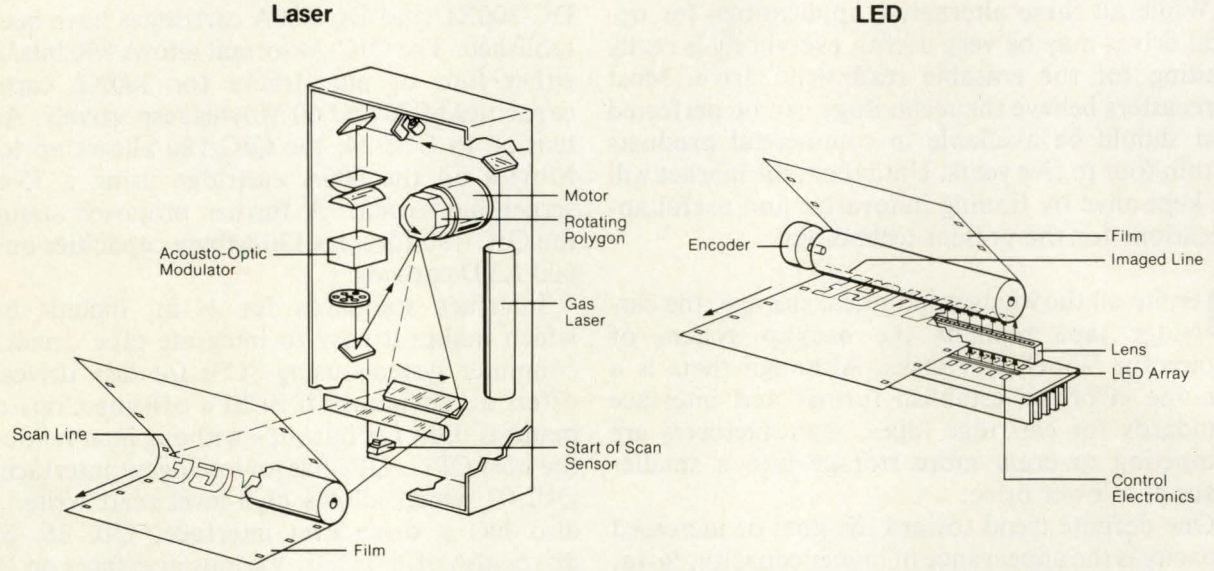
One definite trend toward the goal of increased capacity is the appearance of higher capacity, ¼-in. cartridge drives in the 5¼-in. form factor. Quarter-inch cartridges with storage capacities from 10 to 125 Mbytes are needed as backup devices on microcomputers with hard disk capacities covering the same range. As the distinction between desktop microcomputer workstation and minicomputer continues to blur, ¼-in. drives will push into areas formerly held by ½-in. cartridge drives.

Higher capacity drives have been made possible by better mechanical design that allows 24-track recording and high-capacity tape cartridges, mostly from 3M (St. Paul, MN) and its licensees. Tape format standards are being worked out by the Working Group for Quarter-inch Tape Compatibility (QIC), which is also trying to establish interface standards for drives. Two format standards for 3M DC-300XL and DC-600A cartridges have been established. The QIC-24 format allows 800 bits/in. in either four or nine tracks for 300XL cartridge capacities of 20 and 60 Mbytes respectively. An extension to QIC-24, the QIC-120 allows up to 125 Mbytes on the 600A cartridge using a 15-track serpentine format. A further proposed standard, the QIC-150 foresees 130-Mbyte capacities on DC-600 XTD cartridges.

Interface standards for ¼-in. include SCSI, which makes it easy to integrate tape drives into computer systems using SCSI for disk drives and offers an advantage if SCSI's off-line Copy command is used for backups without intervention by the host CPU. QIC has an intelligent interface, the QIC-02 which allows high-level read/write. QIC also has a drive-level interface, QIC-36. Some drives also offer ESDI. Various interfaces on ¼-in. products are needed to fit a range of systems from personal microcomputers to mainframes. Although mainframes have no direct use for a ¼-in. drive, data is often passed from micros to mainframes via tape cartridges.

By the same token, smaller computers need to put data on ½-in. drives that are more frequently used by mainframes. For ½-in. drives, there is the IBM 3480 system with a 200-Mbyte formatted capacity that was designed for mainframes but considered by some to be too bulky and expensive for smaller systems. The efforts of a Working Group for Half-Inch Tape Compatibility (HI/TC) have produced two formats that specify the 3480 tape

Archive's Super Scorpion with a 125-Mbyte formatted capacity in a 5¼-in. form factor is one of the few ¼-in. cartridge tape drives that conform to the QIC-120 standard. The standard, an extension of QIC-24, lets data be written on 3M DC-600A cartridges using a 15-track serpentine scheme.



If costs can be lowered, LED-based electrophotographic printers will be inherently more reliable than laser printers because the latter rely on moving mirrors and precisely aligned optics, while the former use a fixed array of LEDs.

cartridge but not the drive. They are HI/TC-1 with 240 Mbytes formatted and HI/TC-2 with 480 Mbytes. Drives that will use these formats will most likely use ESDI and SCSI to fit into small systems and to bridge the gap to larger ones.

In printer technology, the daisy wheel, once the answer to letter-quality output, seems to have lost its competitive edge when compared to both the dot-matrix and laser technologies. Dot-matrix impact printers offer low cost and high speed for general-data, draft-copy and letter-quality output. In addition, dot-matrix printers also offer programmable fonts and monochrome graphics under software control for those applications in which the resolution provided by these printers is acceptable. The real movement, however, has been in nonimpact printer technology, with laser printers leading the way. Other contenders are thermal-transfer and ink-jet printers, as well as those using ion-deposition.

For applications that require color, however, laser technology hasn't arrived. But, thermal-transfer devices from Seiko (Torrance, CA), Okidata (Mount Laurel, NJ), and Hitachi (Tokyo, Japan), offer 100-dot/in. resolution color for less than $200. On a higher level, color screen copiers from Hitachi and Seiko achieve 400 dots/in. in reproducing color CRT displays.

Laser printers are essentially raster devices, and can be controlled by the same kind of graphics controller ICs used in CRT diplays. This makes transferring text and graphics between CRT and printer more a matter of resolving the differences in dot density than that of elaborate recoding and reformatting or raster to vector conversion.

This flexibility of nonimpact printers means that there is a considerable need for high-quality software to bring out their potential. Page-description languages, such as Postscript from Adobe systems (Palo Alto, CA), allow a page to be stored in a printer's memory in the form of higher level descriptions of text and formatting commands. The printer's intelligence converts these commands to the raster scan, thus, requiring less memory in the printer and reducing the time needed to transfer a page from host to printer.

Currently, all low-cost electrophotographic-type printers are laser-based, but LED-based printers are presenting a challenge. The laser printer uses a system of optics and a rotating mirror to scan its beam on a photosensitive drum or belt. These are moving, mechanical parts that require alignment and are subject to wear and tear. LED printers use a fixed horizontal array of LEDs to sensitize the drum or belt. If volume production and engineering decrease costs enough to compete with lasers, the LED approach appears to offer a more effective and reliable design. **CD**

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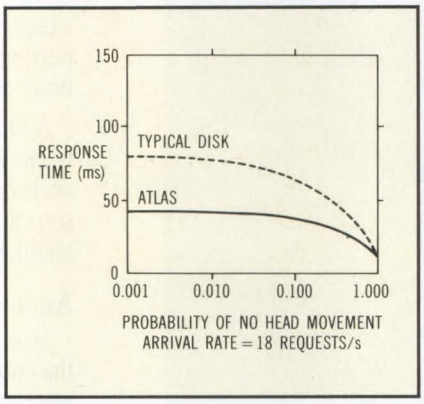
CIRCLE NO. 48

520-Mbyte disk drive shortens response time

Flying 76 read/write heads over four 14-in. diameter platters, the 520-Mbyte capacity Atlas 520 fixed-disk drive offers virtually instant access to the 2.25 Mbytes of data that lie under the heads. Because disk-intensive programs run with substantially fewer seeks, the drive yields average access times below 18 ms even in high-demand network environments.

While most conventional disk drives mount one head per slider and one or two heads per surface, this design mounts multiple heads per surface. One head is allocated to each track in a cylinder. The heads read each recording surface in the four-platter stack and can access an



Entire 2.25-Mbyte cylinder of data without movement. This design reaches the data's location faster.

Many heads and few seeks provide rapid access to data. Overall, multi-user systems benefit from the faster response to I/O requests because the shorter access time cuts the amount of time that any request spends in the request queue.

The Atlas 520 drive attaches to the host using available controllers that support transfers at rates to 1.8 Mbytes/s. Two drives can be linked to supply a total of 1,040 Mbytes of on-line capacity. A dual-port option allows two or more host systems to connect to the drive.

Drives, complete with cabling and power supply, sell for $10,850. OEM discounts are available. Delivery takes 10 to 12 weeks.

Alpha Data, 20750 Marilla St, Chatsworth, CA 91311. **Circle 142**

5¼-in. Winchester disk drive line features highest capacity available

Claiming the highest storage capacity of any disk drive in its category, the XT-8760E from Maxtor has a capacity of up to 760 Mbytes. The unit is the top-of-the-line of the company's new XT-8000E product family. A second drive, the XT-8380E, which stores 380 Mbytes, is also available.

Drives are designed with either an Enhanced Small Device Interface or a Small Computer System Interface. Maxtor drives support hard or soft sector formats. Access time on the new units is 18 ms for the XT-8760E and below 16 ms for the XT-8380E.

The capacity increase stems from a revised architecture that, in the high-capacity model, packs over 50 Mbytes of data onto each of 15 disk surfaces. The drive design allows eight thin-film disks per side with one dedicated to servo information. Each system uses Whitney read/write suspension heads, which feature low mass and low load force.

Prices for the drives in OEM quantities are approximately $4 to $5/Mbyte—the lowest cost per Mbyte in the industry.

Maxtor, 150 River Oaks Pkwy, San Jose, CA 95134. **Circle 143**

Internal storage systems provide affordable backup

A line of three internal mass storage subsystems deliver simplified, automatic tape backup to microcomputer users. The TG-1020i is an internally mounted, half-height, 5¼-in. tape drive for the IBM PC, PC AT, PC XT and compatibles. It backs up 20 Mbytes of data on a DC-2000 tape cartridge.

The TG-2025i, which is also compatible with the XT, is an internally mounted, full-height, 5¼-in., 25-Mbyte hard disk with a 20-Mbyte tape drive. It also backs up data on a DC-2000 tape cartridge.

The third drive, the TG-1425i, is an internal, 3½-in., 25-Mbyte hard disk that mounts inside the PX with a half-height, 5¼-in. tape drive storing 20 Mbytes of data on a DC-2000 tape cartridge.

All the tape drives come with the company's software Version 2.0, controller, cables and mounting hardware. In addition, the entire subsystem line employs PC/T, the industry-standard tape format.

Backtrack, a hard disk backup program, backs up files from hard disk to tape, to another disk or to a floppy diskette. XTree is a flexible file and directory management program that simplifies the use of DOS commands and reduces the number of keystrokes required for DOS operations.

The three internal drives—TG-1020i, TG-2025i and TG-1425i—sell for $995, $1,995, and $2,095, respectively.

Tallgrass Technologies, 11100 W 82nd St, Overland Park, KS 66214. **Circle 144**

Low-cost, high-capacity disk drives grab workstation attention

Model 6000E disk drives from Miniscribe can store 80 to 170 Mbytes of data and can access that data in less than 30 ms. These devices combine drive control electronics on a single board with an Enhanced Small Device Interface to lower power requirements. Using a head/disk assembly like those used on lower capacity 6000 drives, the 6000E cuts manufacturing costs.

By replacing the ST412 interface of the 6000 with an ESDI, the manufacturer has doubled both the capacity and the data transfer rate of the drive to meet the more aggressive performance goals of the workstation market.

The change in interface, coupled with a move to thin-film disks, increases the capacity to 20,832 Mbytes/track. Use of the ESDI also permits data transfer speeds up to 10 Mbits/s as opposed to the 5-Mbits/s limitation of the ST412. Besides doubling the capacity and transfer rate, ESDI lets customers control the drive themselves. Unlike SCSI drives, which handle management functions within the interface, ESDI drives offer users the ability to increase the throughput of their operating systems by using custom formats.

Prices for the drives are from $1,000 to $1,300.

Miniscribe, 1861 Lefthand Circle, Longmont, CO 80501. **Circle 145**

OWNERSHIP STATEMENT
Statement of the Ownership, Management Etc. of
COMPUTER DESIGN
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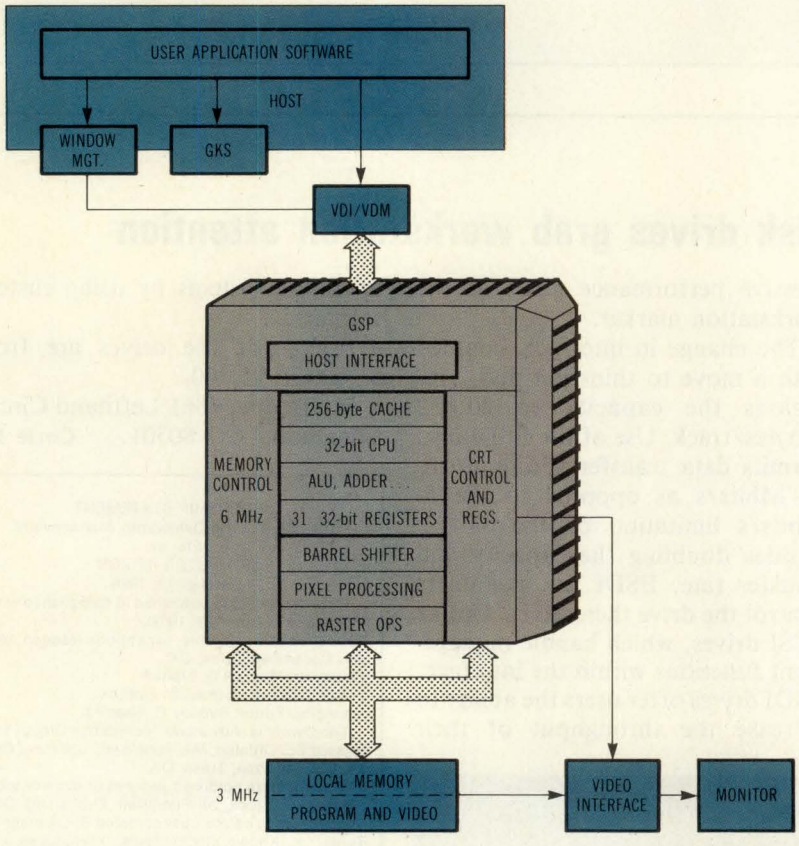
Michael S. Elphick
Publisher

32-bit graphics processor features on-chip display control

A 32-bit graphics system processor (GSP) from Texas Instruments—the TMS34010—integrates the functions of a graphics controller with a 32-bit microprocessor whose architecture is specifically designed for graphics operations. Included on the chip is a video system controller (VSC).

The TMS34010 consists of a 32-bit CPU with 31 registers and a 256-byte instruction cache. Since instructions are executed from the cache, the processor can perform calculations internally while its on-chip memory-control unit accesses memory. At the same time, the VSC can execute its commands and control display timing and dynamic RAM refresh. The GSP's internal processor executes at a 6-Mips rate and consumes 0.25 W. External cycle time is 320 ns for accessing memory and the video interface.



The memory's bit-addressable nature permits the processor to perform "field management" and to define groups of bits of arbitrary size without worrying about the alignment of memory operations on word boundaries.

Bit-addressable memory allows display memory configurations in any desired combination of screen resolution and pixel depth (number of bits per pixel). The 320-ns cycle time makes a 1,280-×1,024-pixel resolution practical. The GSP can store its own instructions and display list data in its own memory space along with multiple screens. If needed, multiple GSPs can be associated with a bit map for even larger array sizes.

The GSP's high-level language programmability provides for adaptation via software to any of the existing or emerging graphics standards. Since the actual display control is embedded in the processor, the programmer need only worry about high-level functionality and not the details of display. Texas Instruments supplies a series of development software for the TMS-4010, including an assembler, a C compiler and a linker.

Texas Instruments, Semiconductor Group, Box 809066, Dallas, TX 75380. **Circle 146**

Graphics device drivers compiled from menus "while you wait"

To write device drivers that make Computer Graphics Interface (CGI) commands understandable to specific devices, Visual Engineering has developed an extension to its Visual GKS product. Graphcap converts a text file of user-readable device protocol commands into control modules that can be assessed by the application at run time.

Graphcap defines a device by its capabilities and control. Capabilities are described by flags (yes/no answers about device capabilities) or by integers to describe functionality. Control is defined by strings or by substitution parameters.

Graphcap has input possibilities to include almost any graphics device description, including complex parameter substitution. This feature lets Graphcap handle encrypted protocols that can combine a code for a control function with numeric parameters. It handles floating-point numbers for fractional positioning.

(continued on page 145)

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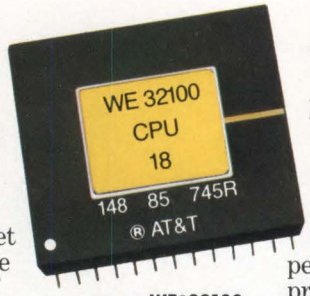

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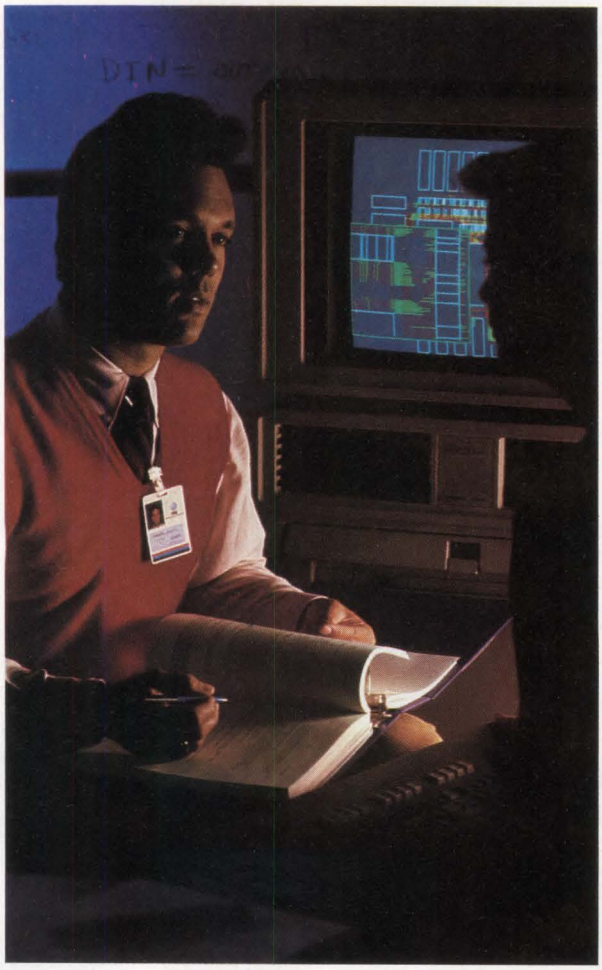

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Right now, for example, AT&T is the only company in volume production of a microprocessor-controllable, single-package modem that can handle up to 2400 bits per second.

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Few remember James Mollison, the second man to fly solo across the Atlantic, because 'Lindy' did it first.

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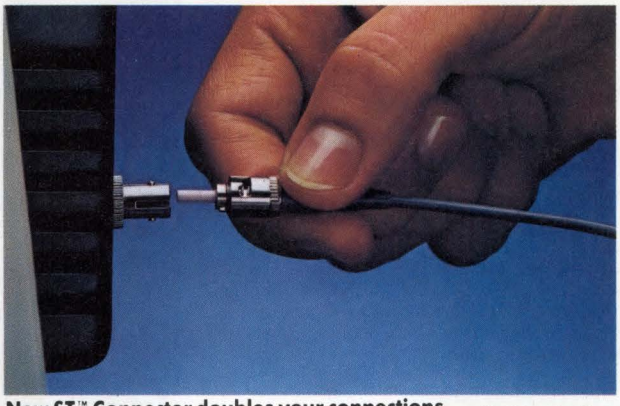
encryption processor available.

And our X.25 Protocol Controllers offer the widest range of applications, from PCs to satellites.

In memory, not only are we currently delivering an American-made 256K DRAM, but we offer a range of leading-edge specialty memories.



New ST™ Connector doubles your connections.

Count on AT&T's advanced technology to help you move your product out the door on schedule.

Advanced custom design capability.

Nobody knows better than you—moving to market first, and staying there, can require custom designed components.

At AT&T, we'll get involved at any stage of your product design—from layout to prototype to production. We'll support you with the industry's most advanced CAD/CAM software, rapid prototype turnaround, and unsurpassed volume manufacturing capability. Everything you need to ensure the success of your product—on your manufacturing line and in the market.

Your specialized interconnection needs will be quickly taken care of—with multilayer printed wiring boards and hybrid ICs produced to the highest standards of quality and reliability.

We'll meet your application-specific IC needs with expert design and engineering personnel. And with powerful CAD software that helps make sure your devices work the first time. The commitment and resources to deliver solutions—that's what makes AT&T, AT&T.

It all takes power.

AT&T's board-mounted power products cut design time with unmatched flexibility. Our low profile power converters are modular in design and about one quarter the size of conventional DC/DC circuit board converters. So they can be mounted in more places. And in the tightest situations.

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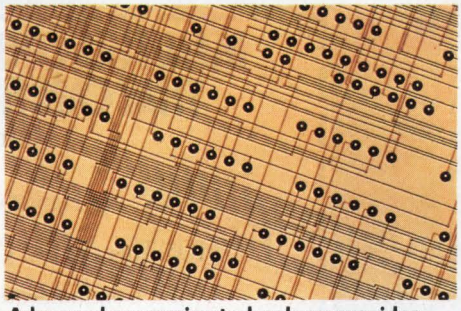
Networking products that lock-in the future.

For local or long-haul transmission, AT&T offers a complete family of fiber optic products and apparatus.

In local area networks, our new ST™ Connector can actually double your network connections—or double the distance between connections—without affecting the fiber optic cable or electronics.

And for high performance data transfer, AT&T's ODL® 50 and ODL® 200 Lightwave Data Links, with bit rates up to 200 Mb/s, incorporate the latest optical and integrated circuit technology. These products, as well as our ODL RS232-1 Fiber Optic Modem, a high performance data interface, readily mate with the ST Connector.

Our newest addition to the AT&T lightwave family—the ASTROTEC™ ceramic laser module—is a reduced-size, long-wavelength laser that offers highly reliable, low cost performance.



Advanced processing technology provides superior buried microvias in multilayer printed wiring boards.

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For more information, phone AT&T at 1 800 372-2447. We'll help you put wings on your concept, and "first" on your product.

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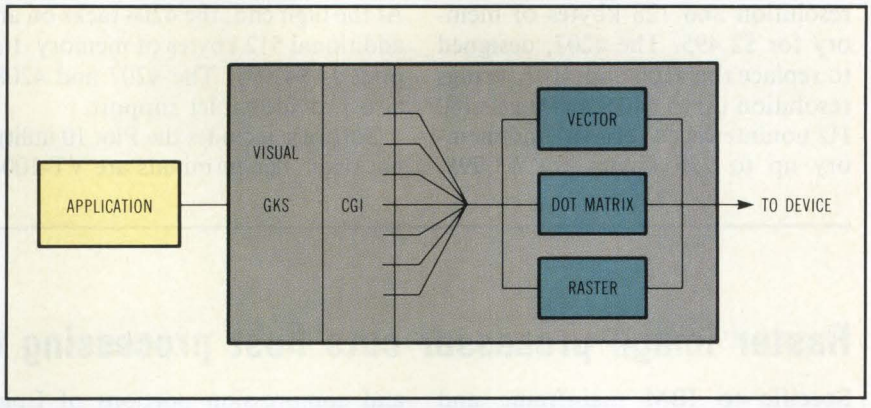
Graphics device drivers...
(continued from page 140)
Plotter width might be described as 0 to 1, for example, so the pen must be positioned in decimal fractions.

A Graphcap definition can also include a previously defined file. For example, if a system designer wishes to upgrade a six-open to an eight-open plotter from the same manufacturer, most of the definition for the new device will be identical to the old one. The new driver would be given a new designation or name and instructed to include the file for the old plotter. Next, the new device would be instructed to reflect any changes in the number of pens and other enhancements. Graphcap's compiler renders drivers as two compact binary files.

One of these files is a personality file that describes the device's characteristics, such as the number of colors or screen resolution. The second file is the device-protocol file, which tells the system how to perform the functions—the actual escape sequences required to move a cursor, enter graphics mode and so forth. These compact files are the actual definitions for an individual device driver.



Only one interface is needed between CGI and any device driver. The pair of files created by Graphcap personalizes a copy of a single master device driver for any device. When starting up Visual GKS, users instruct it to open the primary graphics device.

Visual GKS is already linked through CGI to the driver. It invokes an interpreter that's invisible to users. After reading the binary files that define the device, the interpreter reads the personality file to determine which functions can be performed by protocols in the protocol file and which must be implemented by GKS.

Visual Engineering, 2680 N First St, San Jose, CA 95134. **Circle 147**

Tektronix extends 4100 line while lowering prices

Building upon the industry-standard feature set established by its 4100 line, Tektronix has introduced a new family of graphics terminals offering a broader array of functions to CAD, two-dimensional drafting and data analysis users.

Like the 4100 series, the 4200 graphics terminals offer local graphics segments, true local zoom and pan, multiple views, surfaces, graphtext, and graphics input. To differentiate complex graphs and drawings, 16 colors are displayable from a palette of 64. Custom characters let users define character fonts, such as chemical and mathematical symbols or timing diagram characters. These can be permanently saved on the host and downloaded when needed.

The product line has three models. At the entry level, the 4205 provides the basic features found in the 4104 and 4105, such as segments, zoom and pan, with 480- × 360-pixel

resolution and 128 kbytes of memory for $2,495. The 4207, designed to replace the 4106 and 4107, brings resolution up to 640 × 480 pixels (60 Hz noninterlaced refresh) and memory up to 256 kbytes for $3,995. At the high end, the 4208 tacks on an additional 512 kbytes of memory. Its price is $4,995. The 4207 and 4208 also provide tablet support.

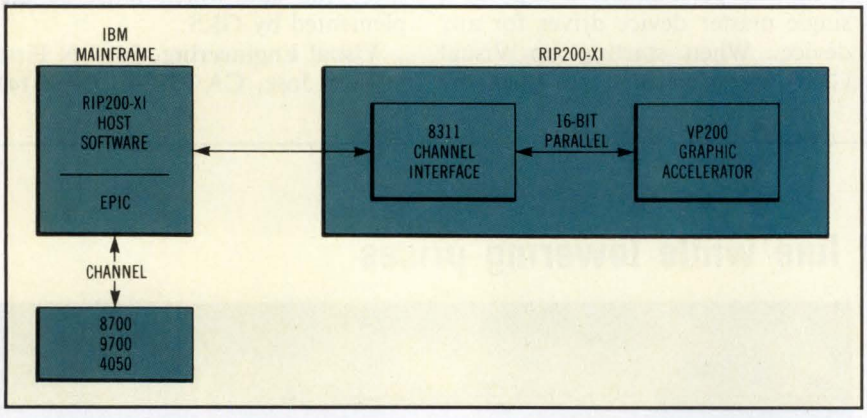
Software includes the Plot 10 utility package. The terminals are VT-100-compatible, and a CX option is available for IBM 3270 environments that provide IBM 3179 alphanumeric emulation.

Tektronix, PO Box 1700, Beaverton, OR 97075. **Circle 148**

Raster image processor cuts host processing overhead

Specific to IBM mainframe and Xerox printer use, the KMW RIP-200XI graphics image processor is a specialized graphics system designed to replace the rasterization phase of the Xerox Electronic Printer Image Construction (Epic) software. RIP-200XI reduces host rasterization processing by an average of 60 to 80 percent by replacing rasterization and compression portions of Epic software.

Graphics elements are rasterized by the image processor at speeds of up to 46 ns/pixel and stored in an internal bit map. The bit-map image is compressed and transferred back to the IBM mainframe as a binary image file. This file can then be merged with textual information stored on the Xerox laser printer to create a complete page.



The image processor is compatible with IBM MVS and DOS-VSE operating systems as well as Xerox Epic and Graphics Handling Option graphics packages. All hardware is connected through an IBM channel to the RIP-200XI. In operation, Phase I of the Epic software builds a vector plot file on the IBM computer. The vector plot file is then automatically sent through the IBM channel to the image processor. On the RIP-200XI, Phase II of the Epic software rasterizes and compresses the graphics elements in the file into a bit map. The bit map, or image file, is sent through the IBM channel back to the IBM mainframe, where it can be merged with text if desired. The job is then sent to the Xerox laser printer.

KMW Systems, 8307 Highway 71 W, Austin, TX 78735. **Circle 149**

3-D graphics board set leaves real-time impression

Real-time three-dimensional graphics and imaging with 3-D solids, smooth shading and hidden surface removal is now available on a three-board VMEbus-compatible set or as a desktop workstation product from IGS Technologies. The 3DFX provides up to 80 Mips of graphics processing through up to 16 digital signal processor (DSP) chips for transformation operations and includes a 10-MHz National Semiconductor 32016 CPU, a 32081 floating-point processor, and a 32082 memory-management unit (MMU).

The set consists of a CPU board, a graphics-processor unit (GPU) board and a frame buffer board. The CPU is called the control and communications processor and contains the three National 32000 family of processors mentioned above, plus 4 Mbytes of on-board RAM. In addition to handling most computing tasks for the applications program, which involves creating the display list, the CPU controls communications and peripheral interfaces. It may also directly address up to 8 Mbytes of additional physical RAM over the VMEbus. Virtual memory up to 4 Gbytes is provided by the MMU.

Rendering throughput can be increased with an expansion card that supports the addition of up to 12 more DSP chips. Each DSP chip runs at 5 Mips and is provided with 16 kbytes of local program and variable storage.

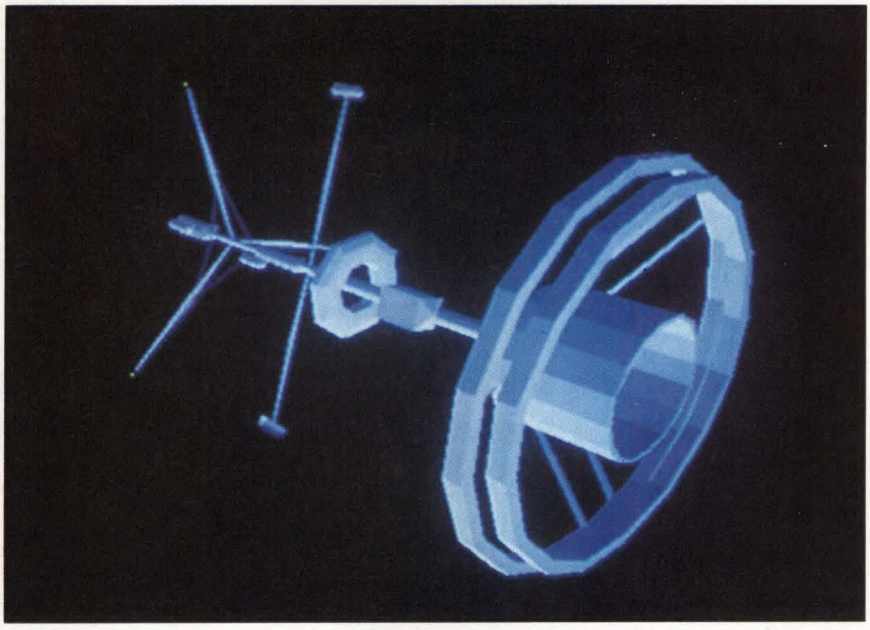
The frame buffer board accommodates two 512- × 512- × 8-bit pixel buffers, each expandable to 1,024 × 1,024 × 8 bits. This allows double buffering of images for smooth

changing of imagery and a greater real-time animation effect. The 8-bit pixel information goes to a 24-color lookup table, and 256 simultaneous colors can be displayed of a possible 16.7 million. Frame buffer formats are software selectable from 30 Hz interlaced to 60 Hz noninterlaced.

The 3DFX is also supplied as a workstation in a floor-standing tower configuration with power supply and fans.

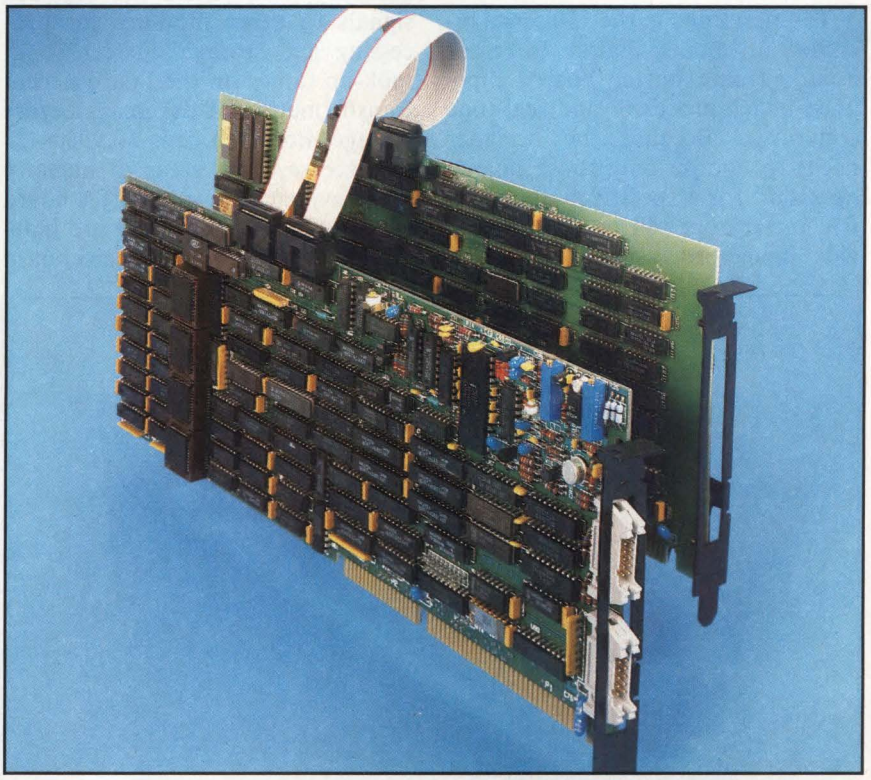
OEM prices are $18,000 to $24,000 for the board set, depending on the number of transform processors included. Prices for the workstation configuration range from $40,000 to $50,000.

IGS Technologies, 145 Cityview Dr, Toronto, Ont. M9W 5A5, Canada. **Circle 150**



Software and boards deliver high-speed image processing to IBM PC AT

Using a proprietary CMOS memory architecture, three products introduced by Data Translation accelerate image processing on the IBM PC AT to minicomputer throughput speeds. The basic system is built around a single board, the DT2851 High Resolution Frame Grabber, which digitizes, stores, processes in real time, and displays video images. Complementing the Frame Grabber, the DT2858 Auxiliary Frame Processor is a 16-bit pipelined processor that speeds completion of lengthy image-processing calculations. The DT-Iris Image Processing Software directs the processing of algorithms to the two boards rather than to the slower PC AT. The system is up to 250 times faster than the PC AT processor alone.



Two 256-kbyte memory buffers offer enough on-board storage for two complete image frames. By transferring images captured in one buffer to the DT2858 Auxiliary Frame Processor, the architecture permits parallel processing of multiple images. Images sent to the DT2858, for example, can be convolved or histogrammed while other images are averaged, offset or overlayed with graphics in real time on the other buffer.

Using an on-board RAM conversion table and a 16-bit arithmetic logic unit, the DT2858 Auxiliary Frame Processor speeds arithmetic-intensive operations. The board attaches to the DT2851 Frame Grabber via external I/O ports,

allowing the transferral of entire image frames at very high speeds.

The software supplies application and subroutine support. Processing routines such as windowing, frame averaging, histogram, logic operations, and N×M convolution serve applications in machine-vision inspection, medical imaging, scientific research and robot vision. Unlike other software packages, however, the DT-Iris implements its routines on the Frame Grabber/Processor hardware, rather than on the slower PC AT processor.

The DT2851 Frame Grabber lists for $2,995, while the DT2858 Auxiliary Frame Processor is priced at $1,495. The software costs $995.

Data Translation, 100 Locke Dr, Marlboro, MA 01752. **Circle 151**

High-performance VMEbus boards deliver modular real-time image processing to industrial environment

Four board-level image-processing modules, initial introductions in the Imaging Technology Series 150 family, are designed specifically for use with VMEbus-compatible computers in rugged industrial environments. Aimed at machine-vision applications, in which high-level performance is a necessity, the boards offer a price/performance ratio that's suitable for a variety of applications.

The first units in the 150 series include an analog-digital interface board, frame buffer board, pipelined image processor and real-time convolver. Because the designer needs to choose only those boards necessary for a specific system, system integrators will be able to provide image-processing systems for less than $10,000. To lower system costs, vendors that are building their own boards will soon be offered a proprietary chip that implements the video bus interface to this series of boards.

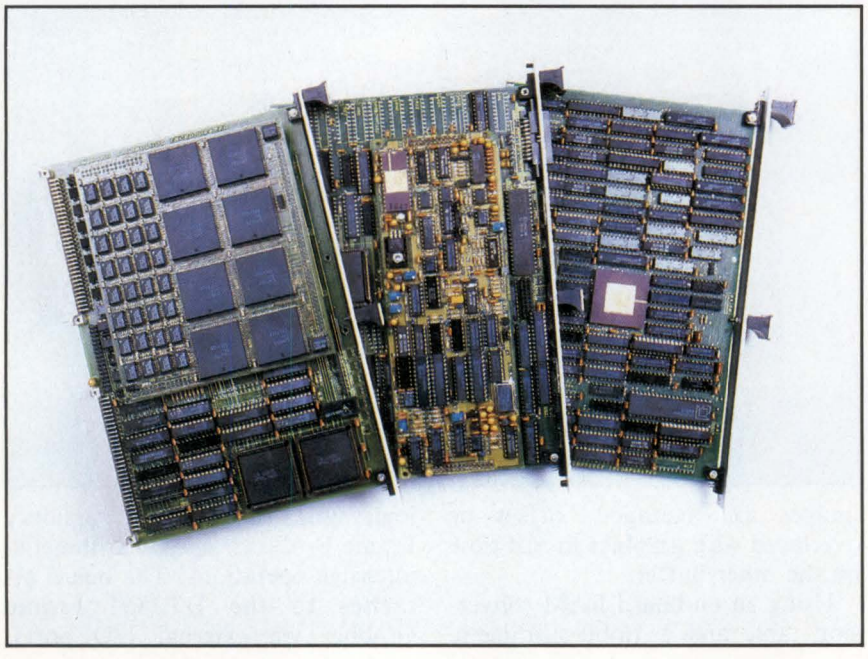
Analog-digital interface board ADI-150 accepts analog inputs from as many as four devices, such as cameras or videocassette recorders, digitizes the input signal to 8 bits of accuracy, and passes the digitized signals to other modules for processing and storage. Sixteen input look-up tables on the board permit transformation of the image before storage. Board price is $2,995.

Three separate areas of memory are provided by frame buffer board FB-150. Because all areas are independently controllable, this board can simultaneously hold multiple processes and/or unprocessed images. In addition, the FB-150 supports pan, scroll and zoom. It's priced at $2,995.

The 16-bit ALU-150 pipelined image processor performs summation, subtraction and averaging arithmetic functions as well as AND, OR, and XOR logic operations on a full frame of pixels in 1/30 s. The ALU-150 also can execute complex convolution algorithms such as those required in machine-vision inspection systems. The image processor costs $1,995.

Real-time convolver board RTC-150 performs 4×4 convolutions—the computation of a weighted average of each pixel in an image that's based on the values of the pixels in the immediate area—at video rates. This board sells for $3,995. Software—including diagnostics for testing and verification of the boards—is provided.

Imaging Technology, 600 W Cummings Park, Woburn, MA 01801. **Circle 152**



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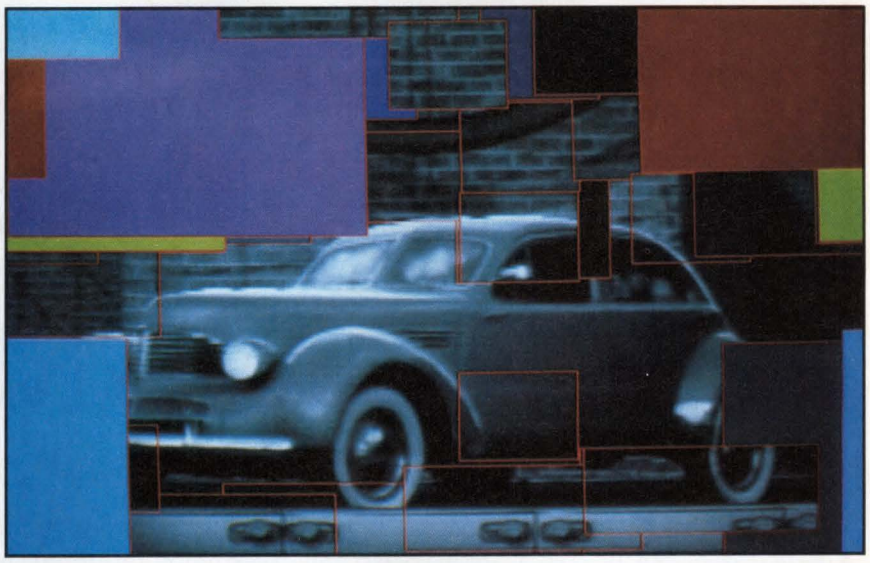
Low-cost VMEbus board overlays graphics on live images

Many image-processing applications require not only a clear image, but demand user-generated elements as well. A reference grid to the display, for example, can simplify imaging applications significantly. A graphics controller from Datacube offers the capability to overlay graphics on live digital video signals.

Maxgraph features separate red, green and blue outputs for the simultaneous display of 256 colors from a palette of 16.8 million. Delivering 512 × 1,024 × 8 bits of total graphics memory, Maxgraph's 512 lines of displayable memory can be scrolled anywhere within the 1,024-line space. Memory can also be reconfigured as two 512- × 512-pixel image buffers.



Built around the Hitachi HD 63484 Advanced CRT controller chip, the board can operate as a stand-alone graphics generator or as a video processing module with overlay capabilities. As a graphics board, it offers 38 commands including circle, line, polygon, arc, ellipse and rectangle draw. For both monochrome and color environments, it completes fill operations at rates up to 2 million logical pixels/s. The board is capable of running as many as four graphics windows simultaneously, with each window's size and position completely programmable.

Maxgraph-10 offers 512- × 512-pixel capability running at 10 MHz for $1,495. For users of less sensitive sensors, such as those found in factory environments, Maxgraph-7 will deliver 384- × 512-pixel resolution at 7.16 MHz.

Datacube, 4 Dearborn Rd, Peabody, MA 01960. **Circle 153**

32-bit graphics co-computer promises AT a rest

A three-board graphics OEM subsystem for the IBM AT and compatibles off-loads graphics-intensive tasks from the host 80286 CPU. The Graflex system from New Media Graphics has a range of options for program memory, display memory and graphics controller integrated circuits to match system needs.

The basic system consists of three boards. One board houses the co-computer and contains the 68020 and 68881, two serial ports and a shared memory interface to the host. A display buffer delivering 1 or 2 Mbytes of dual-port video RAM and a Hitachi 63484 advanced CRT controller occupy the second board. The third is a video output board that features timing circuits, color lookup tables, and D-A converters for outputting the RGB video signal.

The 68020 can address from 32 kbytes to 32 Mbytes of program memory, independent of the host 80286, letting OEM system suppliers port 68020 CAD software directly. The Graflex system supports the Computer Graphics Interface (CGI) from Computer Software Systems (Beaverton, OR) and can easily link to the ANSI-standard Graphical Kernel System. In addition, it's supplied with a standard C subroutine library and a Unix-compatible C compiler that runs as a cross-compiler under MS-DOS on the AT. A linker, a relocating loader and a graphics subroutine library are also provided.

The three-board configuration is modular. Each 63484-based display buffer board can have 1 or 2 Mbytes of picture memory for a display of 1,272- × 824- × 8-bit pixels, but up to four such boards can be configured in different ways. They can be configured as horizontal bands for a picture memory of 4,096 × 4,096 × 4 bits or overlapped for 1,448- × 1,448- × 32-bit pixels. The video RAM outputs pixel data via its on-chip shift registers, leaving a maximum amount of time for writes from the 63484 or direct access from the 68020.

The present video output board supports screen resolutions of 720 × 512 (60 Hz noninterlaced) or 1,152 × 800 pixels (30 Hz interlaced).

Three boards and software are available in OEM quantities for $2,500.

New Media Graphics, 279 Cambridge St, Burlington, MA 01803. **Circle 154**

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On the following pages you'll find the winners of our August "Best in Issue" ad contest. All of these advertisers and their agencies thank you for the time you spent making your choices and for your constructive comments on the ads. Listed on this page are the top ten winners in rank order, plus winners in five special categories.

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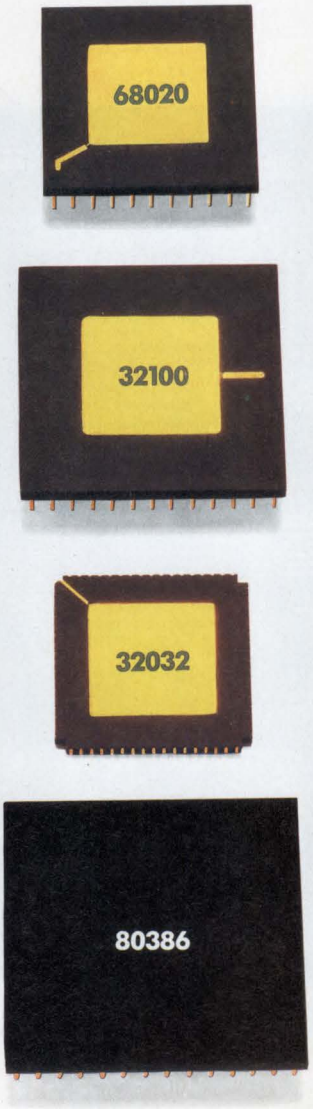
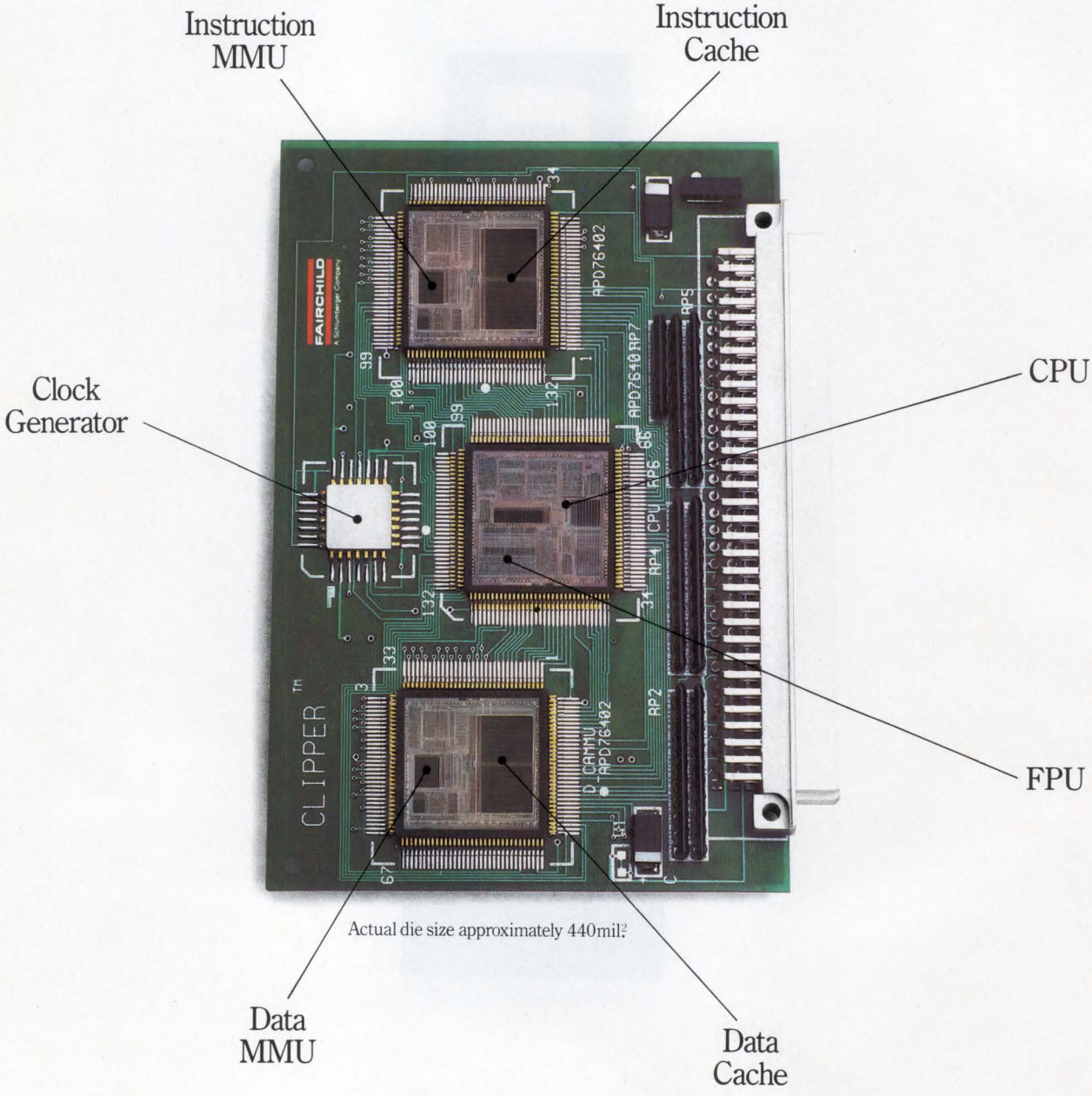
If they had it to do all over again,



this is how they'd do it.



Actual die size approximately 440mil²

Fairchild's CLIPPER.™ 33 MHz performance. Today.

Those microprocessors on the first page all talk a lot about being "the most complete," or "ultra-fast," or even "the next industry standard."

Contrary to those claims about being state-of-the-art, however, most of them are actually state-of-the-past. They're all based on architectures developed way back at the dawn of the microprocessor era, and their performance has reached a practical limit. They simply can't bridge the gap to true supercomputer performance.

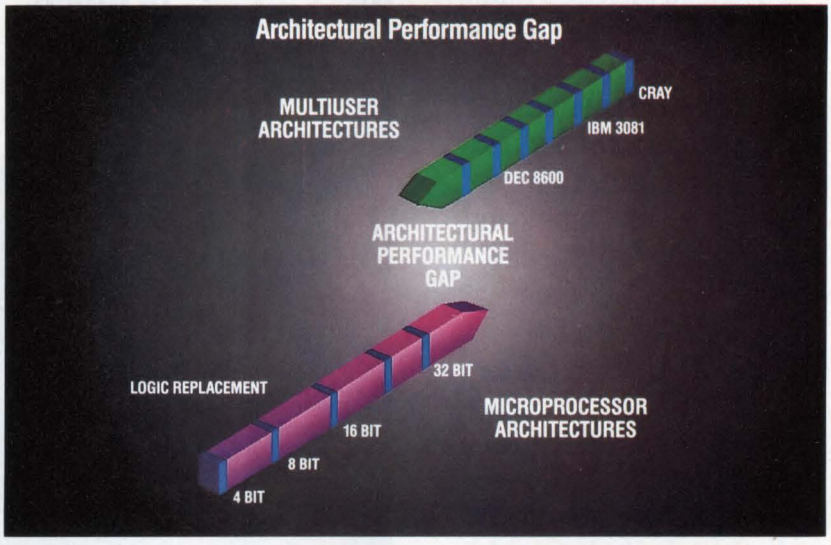
It's high time someone offered something more. Like a microprocessor built from the ground up with a brand new architecture. Able not only to replace those ICs of yesteryear, but to make them obsolete.

Now there's a microprocessor that does just that.

It's called CLIPPER. And it's from Fairchild.

CLIPPER. What everyone else will think of next.

CLIPPER is the biggest single advance in microprocessors since the microprocessor itself. It combines VLSI design with mainframe and supercomputer techniques to create the new standard in 32-bit microprocessor performance. Our CLIPPER port based on the UNIX® System V operating system gives unprecedented software power, speed and portability to any application. And in today's RISC-oriented world, CLIPPER does RISC one better – its unique Streamlined Instruction Set offers all the advantages of a RISC, the advantages of a CISC, and then some.



Just by looking at it, you can tell CLIPPER is a different breed of microprocessor. In a unique three-chip set, you get an architecturally advanced, very high-performance, CMOS 32-bit compute engine, optimized for scientific and professional computing applications. In fact, you get everything in the three CLIPPER chips that it takes the competition's entire CPU board to give you.

The bottom line? CLIPPER is incredibly fast. It's optimized for speed, and designed for high bandwidth and true concurrent execution of instructions. It also runs at 33 MHz which, until CLIPPER proved otherwise, was considered impossible. CLIPPER achieves a peak execution rate of 33 MIPS, with average performance greater than a VAX™ 8600 – twice as fast as any other microprocessor in existence, five *times* as fast as a VAX 11/780. Floating-point performance exceeds 2 MFLOPS, while simple instructions execute in a scant 30 nanoseconds.

Think of it as a very small supercomputer.

Unlike any other microprocessor architecture, CLIPPER uses proven supercomputer and mainframe architectural concepts.

Pipelining, for example. Not only do we overlap fetch, decode and execute processing phases, but we've gone one step further to pipeline the integer execution unit, processing up to three instructions at the same time during the execute phase.

Concurrent processing units are also built in: the CLIPPER FPU is on-chip, for faster processing in parallel to integer operations.

We also included mainframe-style caching. The two large 4K-byte caches, combined with mainframe-style set associativity and 16-byte line size, reduce memory access times and significantly improve hit ratios. When it comes to bus bandwidth, the CLIPPER CPU features two 32-bit buses to cache memory. Bus bandwidth to the CPU is 133M bytes per second, far greater than ordinary, single-bus architectures. We enhanced bus bandwidth even further by using an additional 32-bit CLIPPER synchronous bus that provides quad-word updating of the caches, in addition to its flexible byte, half-word and word transfers.

Then there is the distinctive CLIPPER Streamlined Instruction Set. 101 instructions are hardwired instead of microcoded to deliver the performance of a reduced instruction set computer. We balanced the RISC architecture by adding a macro-instruction unit. Which provides 67 high-level instructions and functions such as floating conversions, task switch, trap and interrupt handling. And the CLIPPER resource manager provides instruction pipeline management in hardware, where you want it, instead of in your software tools. The result? You get all the advantages of a RISC with the robustness of a complex instruction set.

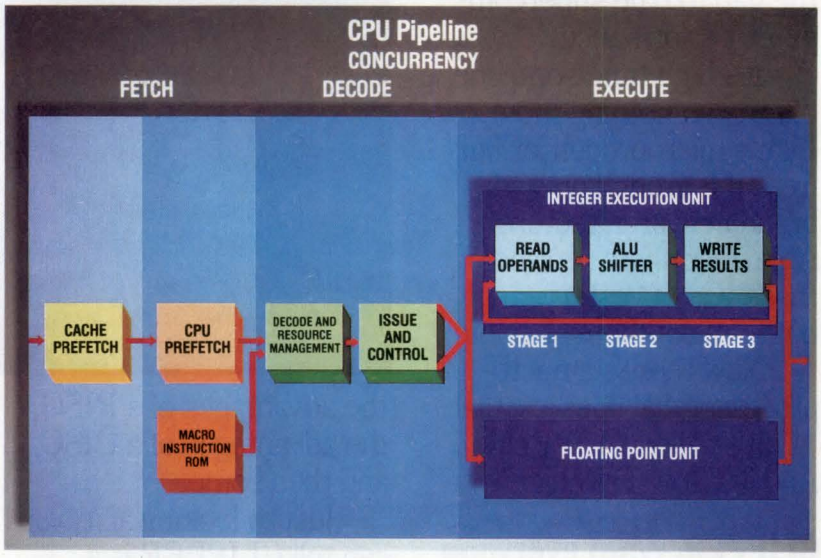
What got into CLIPPER.

The revolutionary CLIPPER three-chip module resides on a 3.0 x 4.5-inch printed circuit card which interfaces to your system with a standard 96-pin connector. You'll find a pipelined CPU with a three-stage integer execution unit, plus an on-chip, IEEE-standard floating point unit. For packaging, we put the chips in state-of-the-art 132-pin ceramic leaded chip carriers.

Next you'll find two 4K-byte combination cache/memory-management chips. A clock generator completes the package, for a staggering total of 846,000 transistors. That's practically as dense as all the competition put together.

Lastly, you'll find switching speeds up to the rest of the fast CLIPPER standards. Like Fairchild's FACT logic family and other advanced products, CLIPPER is fabricated with a high-speed, double-metal advanced CMOS process that achieves transistor switching at speeds of up to 500 ps.

If you're having trouble keeping up with speeds like this, just think how the competition feels.



Our cache is right on the money.

In keeping with our goal of bringing supercomputer technology to the chip level, we linked the CLIPPER cache chips via a dual-bus architecture, with one 32-bit

bus dedicated to instructions, the other to data.

The two cache chips are identical. The instruction cache is distinguished from the data cache only by the activation of an on-board program counter that allows prefetch activities into cache memory.

The fast caches provide hit rates greater than 90%. And the instruction cache hit rate with prefetch enabled is greater than 96%.

Contributing to this phenomenal access speed is the combination on the same chip of the cache and demand-paged MMU, which reduces bus loading and eliminates chip-to-chip delays. In addition, virtual addresses are translated concurrent with cache access, eliminating the performance bottleneck of virtual memory translation. Separate caches called Translation Lookaside Buffers (TLBs) store 256 recent page translations. These large TLBs improve overall system performance up to 20% over systems with smaller TLBs.

And your program won't be cramped by an insufficient address space.

Each user process enjoys a full 4G bytes of virtual memory, which may be separate from the operating system's 4G-byte virtual address space. Virtual addresses are translated to a 4G-byte real memory space with a separate 4G bytes for each I/0 and boot memory.

More CLIPPER support. Inside and out.

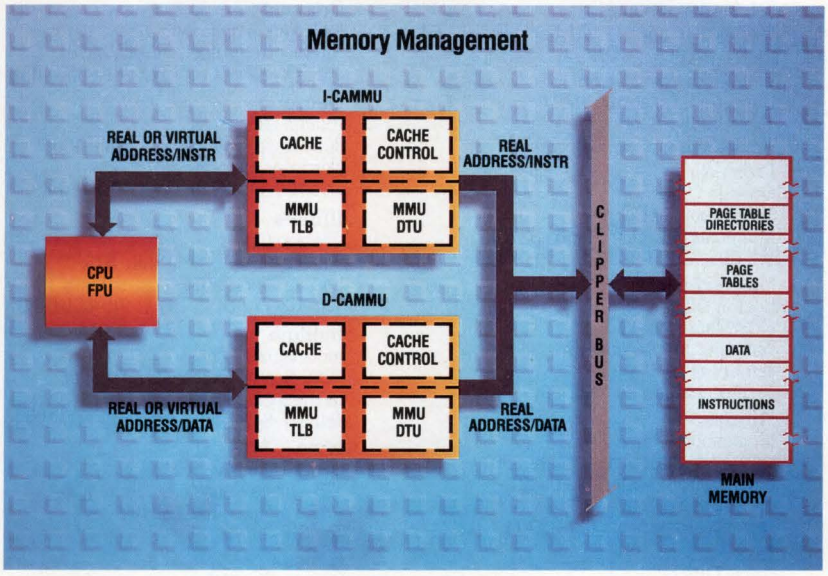
As befits a breakthrough in microprocessor technology, CLIPPER is supported by a powerful software environment. After all, you don't want to spend your time developing software tools. So we give you everything you need, ready-made. Including a CLIPPER port based on the UNIX System V operating system. Optimized FORTRAN, C and Pascal compilers. Plus an assembler.

Or you can choose a VAX cross-support package. Which includes an assembler, C compiler, processor simulator, performance analyzer, debugger, and various other utilities.

There's one more important ingredient in the CLIPPER package: expert advice, care of our application engineers and systems designers. Each one of them, in every sales office and FAIRTECH™ Design Center, thoroughly trained in helping you get everything out of CLIPPER that we put into it. And each one of them ready to help.

CLIPPER. The future got here sooner than you expected.

So there you have it. Simply the most advanced 32-bit microprocessor since the advent of microprocessors themselves.



Offering superior performance advantages in literally every system area: speed, technology, integration, and architecture.

For more information, just give us a call. CLIPPER

You'll find us at The Fairchild Customer Information Center by dialing 1-800-554-4443.

CLIPPER from Fairchild. It's what the competition wishes they'd built in the first place.

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We're taking the high ground.

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CIRCLE NO. 51

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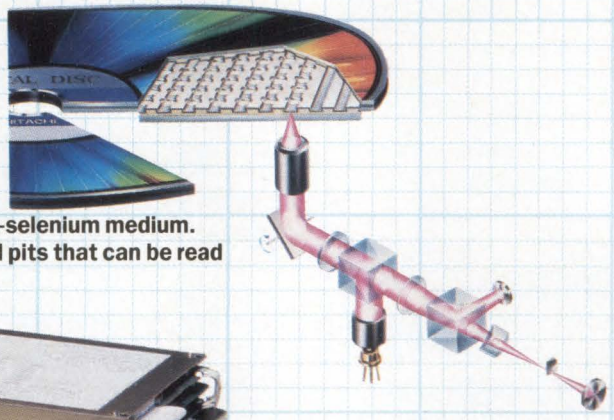
CIRCLE NO. 52

SPEEDING INFORMATION ACCESS THROUGH OPTICAL DISK TECHNOLOGY

THE 301 SERIES OPTICAL DISK SUBSYSTEM

Hitachi's 301 Series optical disk subsystem enables a computer to access as much as 5.2 gigabytes of on-line information. The 301 Series optical disk subsystem consists of a formatter/controller that handles as many as four disk drives, each having a write-once storage capacity of 2.6 gigabytes. The drives record data by employing a semiconductor laser to score microscopic pits on a 12-inch disk coated with a photosensitive tellurium-selenium medium. This proprietary technique produces sharply defined pits that can be read back with high accuracy and reliability.



Disk Drive OD301A-1

The 301 Series drive automatically checks each data bit after it is written and also records error-correcting bits. The combined use of read-after-write checking and error-correction codes reduces expected read errors to 10^{-12}, allowing storage of both image and encoded data.

Disk Cartridge OC301

To assure data retention, the 301's disks are sealed in a glass envelope and then encased in an easy-to-handle plastic cartridge. The predicted data life of the doubly sealed disk is more than 10 years.

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How Hitachi's 301 Series Facilitate Information Storage and Retrieval

With the introduction of its 301 Series optical disk system, Hitachi has taken a giant step forward in speeding information access. Unlike conventional disk units, which record information magnetically, the model 301 stores data optically—by using a laser to inscribe microscopic pits on a specially coated disk surface and subsequently read them.

The results: a big leap in storage capacity per disk. A 301 Series system can store 2.6 gigabytes of information on a 12-inch disk. The 301 Series library unit, which combines an automatic disk changer with one or two drives, can store and retrieve 83 gigabytes of information—yet occupies no more space in an office than would a large filing cabinet.

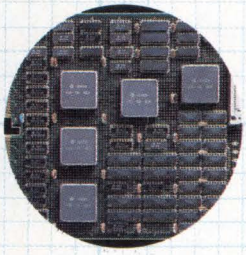
The ability to record so much information so compactly opens vast new applications for on-line information storage and retrieval. For example, with the 301 Series, it becomes economically feasible to create extremely compact electronic archives for storing and retireving copies of medical records, engineering drawings, and other documents, much faster than with conventional microfilm or magnetic tape storage. Other applications include electronic publishing and backup of volatile databases in large-scale information processing systems. For more information, contact:

Hitachi America, Ltd.

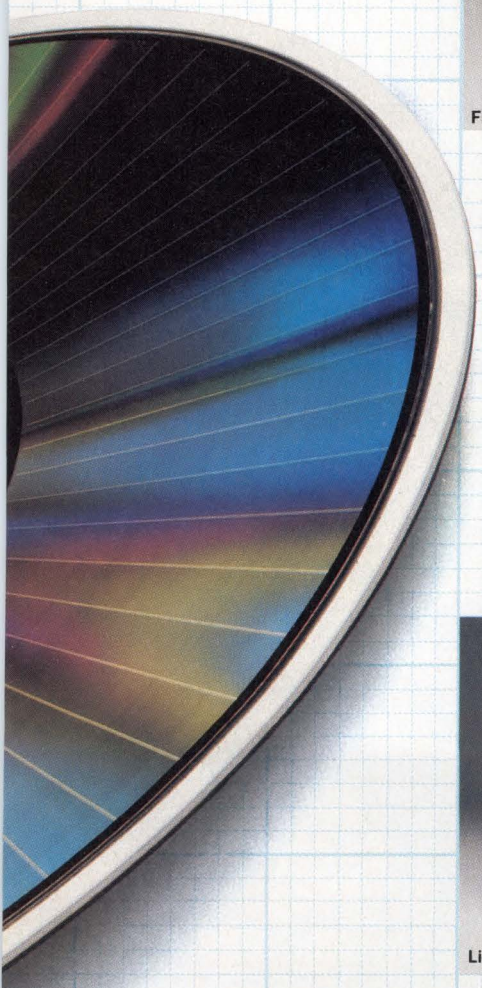
Computer Division
Peripheral Systems Marketing Department
950 Elm Avenue, San Bruno, CA 94066
Tel: 415/872-1902
or: 313 Speen Street, Natick, MA 01760
Tel: 617/655-5501

The 301's formatter/controller implements either the industry-standard SCSI interface or a GP-IB (IEEE-488) interface, which enables the disk subsystem to be used with a wide range of computers. The unit includes its own memory buffer to speed data transfer between a host computer and the disk drive, which has a 250 millisecond average access time.

Formatter Controller OF301S-1/2



Hitachi Developed
6000 Gate LS1



This 12-inch optical disk can store 2.6 gigabytes of images or encoded data.

Library Unit OL301S-11

The 301 Series library unit provides as much as 83 gigabytes of on-line storage capacity. It incorporates a formatter/controller, one or two disk units, and an automatic changer for as many as 32 disk cartridges.

HITACHI®

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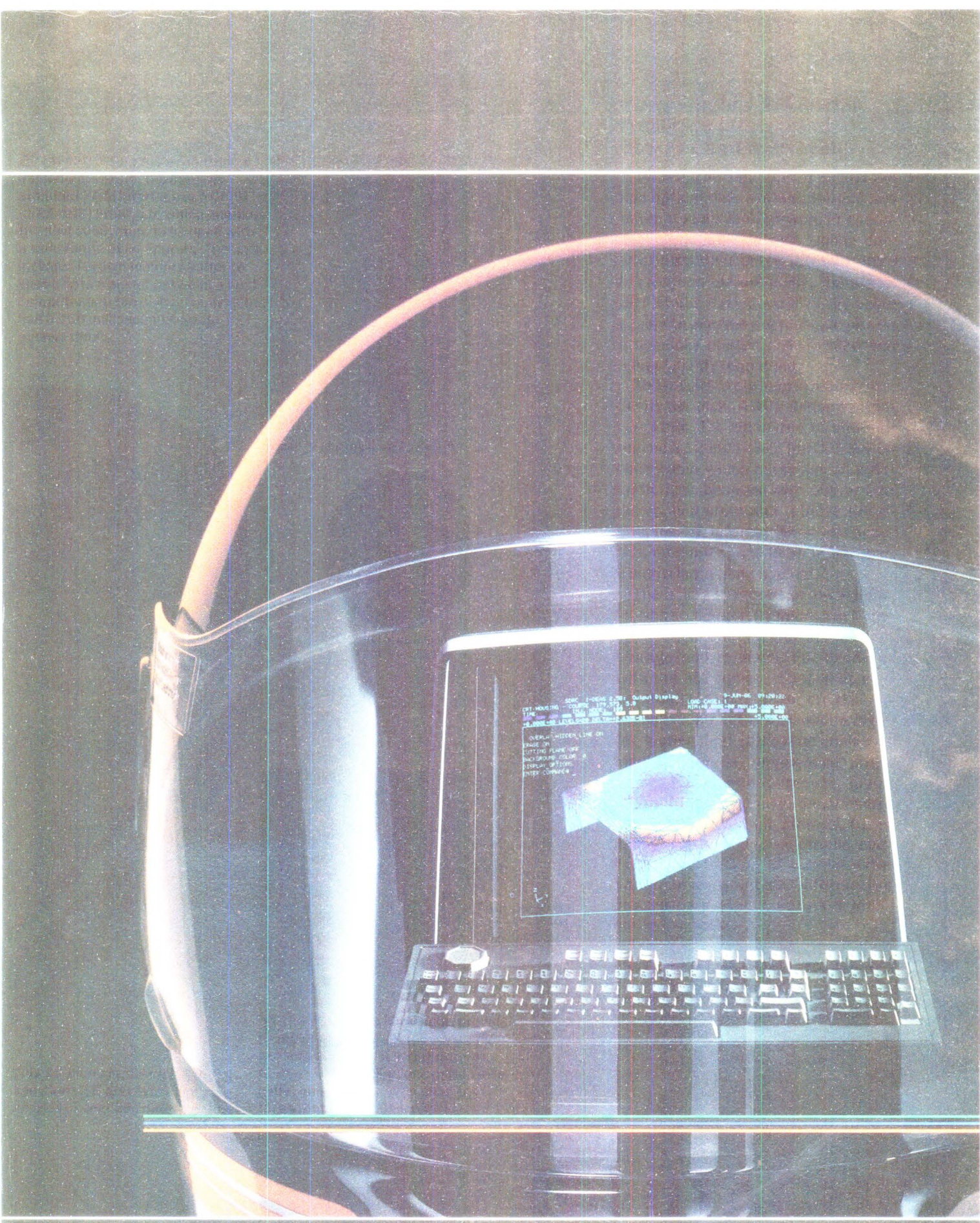

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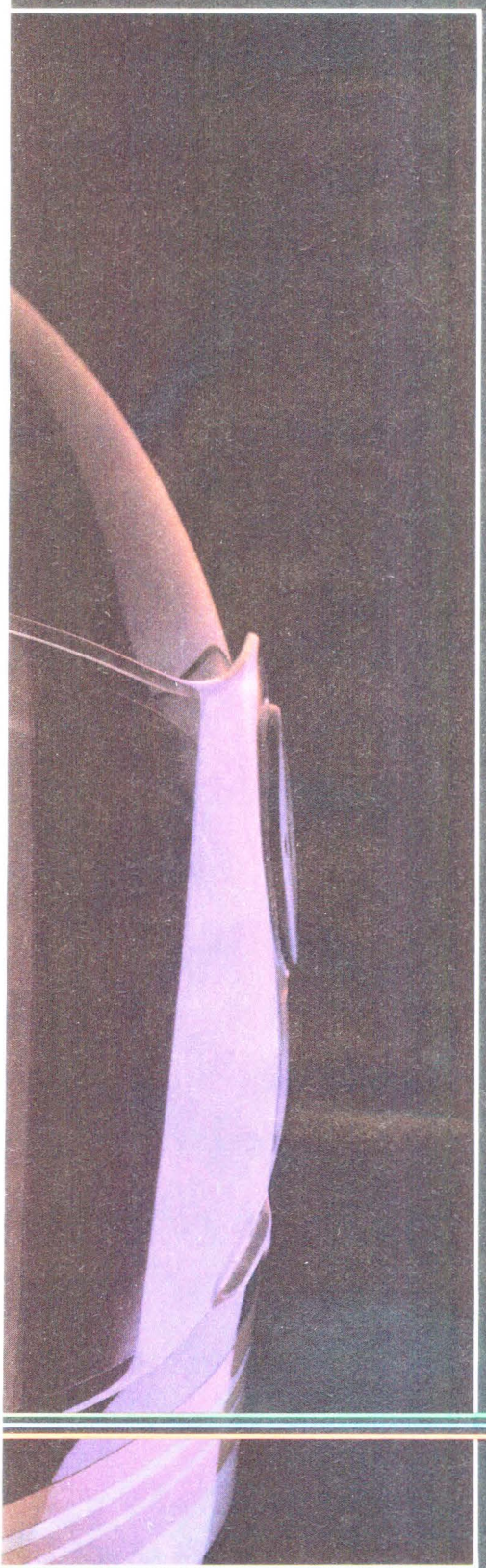

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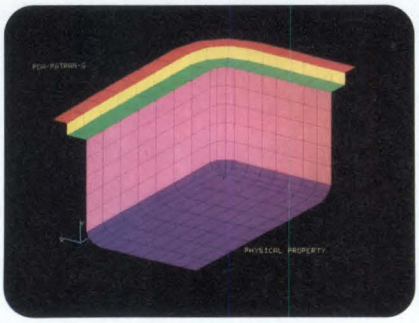

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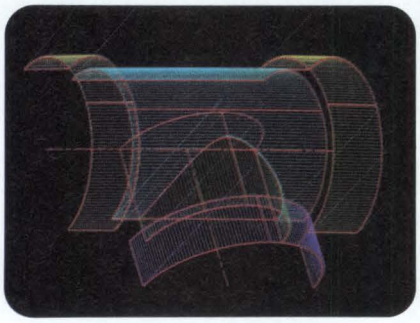

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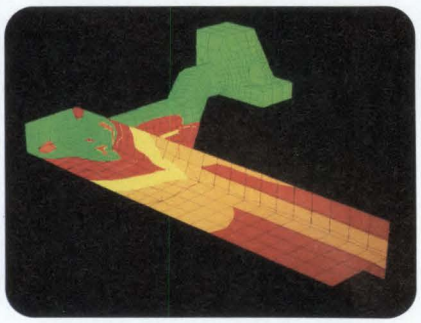

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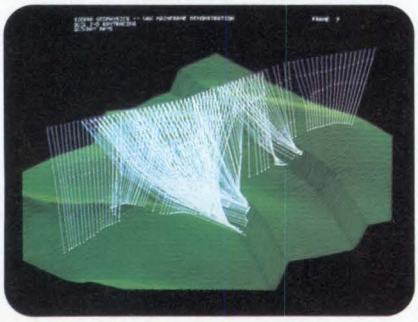

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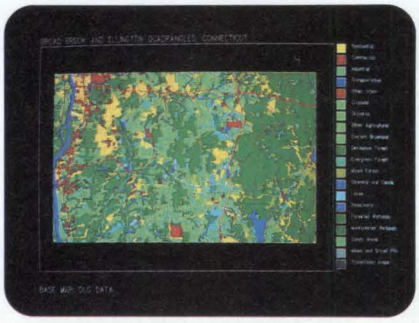

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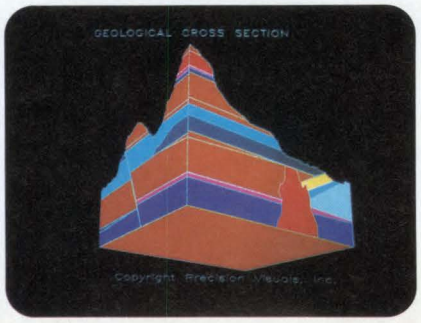

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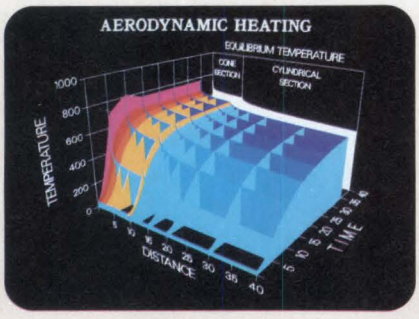

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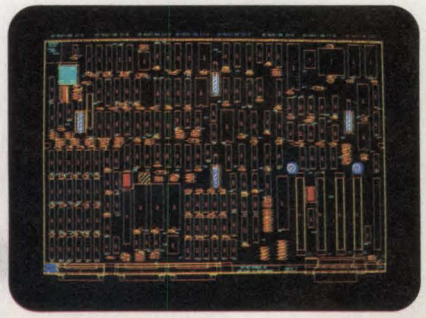

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Now, the high-speed, high-resolution 4111 desktop terminal is supported by more application software packages than ever.

Combine these new solutions with the 4111's new optional IBM 3270 compatibility, and you have an even more powerful tool for CAD/CAM, mechanical drafting, technical data analysis, mapping, cartography and business graphics applications.

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Contact your local representative for more information about the versatile 4111, or circle the reader reply number below.

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CIRCLE NO. 55

A no-nonsense message for your workstation selection committee...

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Wide range of graphics solutions.

The choice is yours...from low-cost monochrome to high-resolution color monitors...from simple report

run UNIX* systems and environment, talk to HP.

graphics to 3D solids modeling. There are industry standards like GKS and ANSI Computer Graphics Virtual Device Interface (CG-VDI), to protect your investment by making your existing software portable. HP's accelerated graphics solutions are highly modular, so you can upgrade whenever you choose.

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CIRCLE NO. 56

HOW FAST CAN THE 80386 MAKE YOUR WORKSTATION GO?

Faster than any other 32-bit microprocessor can.

In technical terms that's 4 MIPS. 4 MegaWhetstones. With 4 Gigabytes.

Fast enough to have a sudden and lethal impact on your competition.

To achieve its blazing speed, the 80386 has six-stage pipelining, which allows the standard 16 MHz part to deliver over 6100 Dhrystones per second.

That's nearly four times the Dhrystone performance of a VAX* 11/780, or 4 VAX MIPS.

And with the 80386 you don't sacrifice all that performance for demand-paged virtual memory. Because of its on-chip paging unit and transparent paging cache, the 80386 can do a full virtual to physical address translation without the performance penalty of non-pipelined, off-chip designs. Giving you 4 MIPS of deliverable UNIX** performance.

Of course, to achieve performance like that, you need a bus that's faster than a speeding bullet.

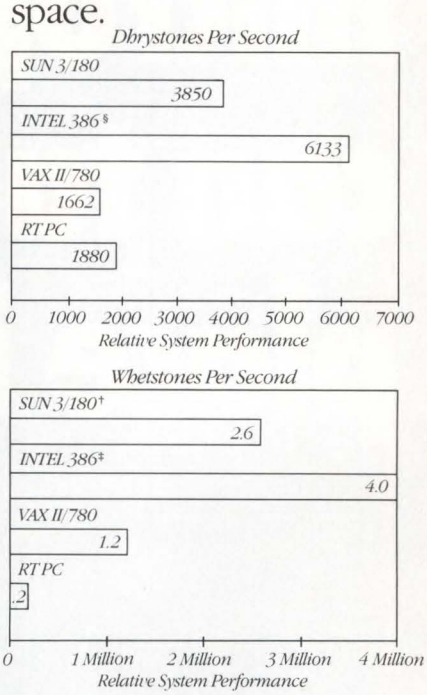
Like our 2 clock bus that provides a 32 Megabytes per second transfer rate.

That's the highest performance of any microprocessor bus.

So what more could advanced system designers ask for?

Blistering 4 MegaWhetstones per second performance for superb graphics and number crunching. Only the 80386 uniquely teams with Weitek's 1167 floating point coprocessor to deliver the highest numerics performance on the market.

And of course all this comes in a 64 Terabyte virtual address space with a 4 Gigabyte linear address space.



§ *Intel 386 MULTIBUS* I 16 MHz Starter Kit.*
† *With Weitek 1164, 1165 floating point chip set.*
‡ *With Weitek 1167 floating point coprocessor.*
Source: Refer to Intel 80386 Benchmark Report.

Finally, for your silver bullet, add to all this $6 billion worth of DOS software. And watch how fast it runs on your 4 MIPS, 4 MegaWhetstones UNIX machine.

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Or call (800) 548-4725 for complete technical information.

Get all the ammunition you need to make your next system a success.

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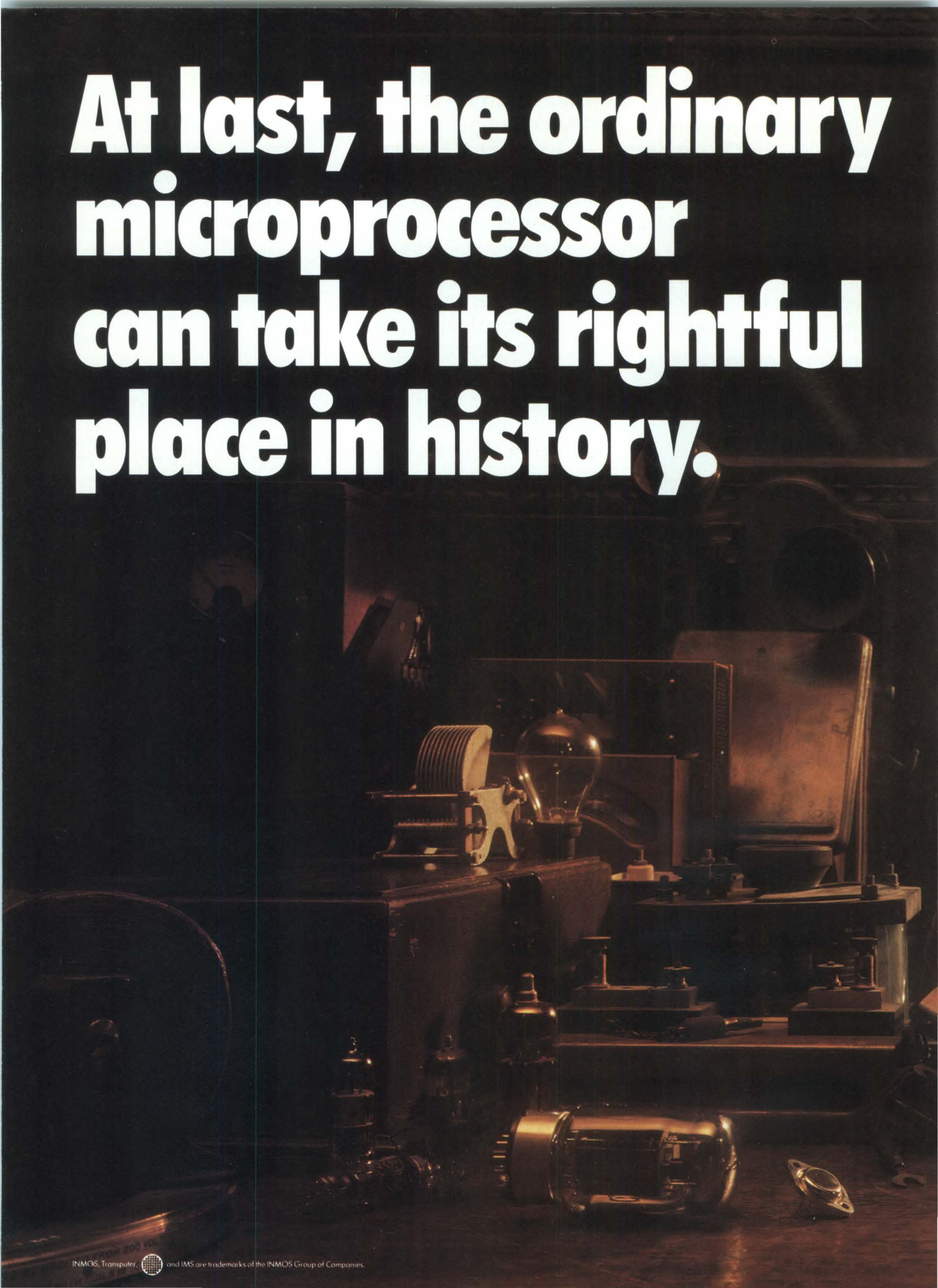
CIRCLE NO. 57

At last, the ordinary microprocessor can take its rightful place in history.



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It had to happen—the conventional microprocessor has had its day. Relegated to the ranks of yesterday's devices by the new transputer family from INMOS. It's history in the making.

The IMS T414 transputer is a fast, easy-to-use VLSI component, integrating a 32-bit processor, four inter-transputer communication links, 2K bytes Static RAM, 32-bit memory interface and DRAM controller. All on a single CMOS chip—offering execution rates up to 10 MIPs.

While transputers excel in single-processor systems, their real power can be unleashed by connecting any number of transputers together via the high-speed serial links. Multi-transputer systems can deliver the performance you need today, and can be easily expanded in the future as your processing requirements increase.

And there's more. Programming multiprocessor systems has never been easier. The Transputer Development System (TDS) supports C, Fortran, Pascal and OCCAM, providing a complete software development environment, and is available for a number of popular hosts. Software developed on the TDS can be executed on one or more transputers, enabling cost-performance tradeoffs to be made.

INMOS transputers are available now and have already found their way into companies who are evaluating, prototyping and manufacturing transputer-based systems. Applications include supercomputers, DSP, graphics, robotics, AI, distributed control systems, PC's, engineering workstations and many others.

Write or phone for more information on the transputer family and start making history yourself.

TRANSPUTER PRODUCTS	
IMS T414	32 bit Transputer–2Kbyte —4 links
IMS T212	16 bit Transputer–2Kbyte —4 links
IMS M212	16 bit Disc Processor–1Kbyte—2 links
DEVELOPMENT TOOLS	
IMS D701-2	IBM PC—Transputer Development System.
IMS D600	VAX/VMS—Transputer Development System.
EVALUATION BOARDS	
IMS B002-2	Double Eurocard + IMS T414 + 2Mbyte DRAM + 2 x RS232.
IMS B003-1	Double Eurocard + 4 x IMS T414 + 4 x 256Kbyte DRAM.
IMS B004-2	IBM PC Format + IMS T414 + 2Mbyte DRAM.
IMS B006-2	Double Eurocard + 9 x IMS T212 + 128Kbyte SRAM.
IMS B007-1	Double Eurocard + IMS T414 + 0.5Mbyte DRAM + 0.5Mbyte Video RAM.
HIGH PERFORMANCE VLSI MEMORIES	
	16K CMOS SRAM, 25-45ns, 64K CMOS SRAM, 35-70ns 256K CMOS DRAM, 60-100ns

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CIRCLE NO. 58

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OBSOLESCENCE

WITH MAINFRAME PERFORMANCE TOOLS FOR YOUR IBM PC.

MAINFRAME CAPABILITY FOR A FRACTION OF THE COST. The FutureNet® family of PC-based CAE tools gives you the high performance you demand, at a price you can afford. From the DASH™ Schematic Designer, DASH™-CADAT PLUS to the DASH™-PCB, our products let you take even the most complex designs through schematic capture, simulation, and printed circuit board layout—faster and easier than you ever thought possible.

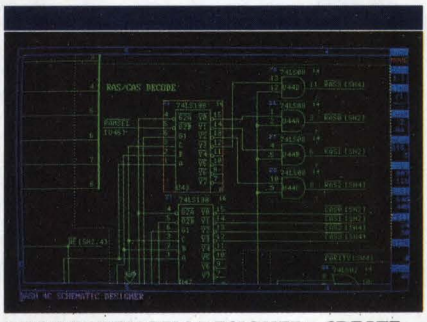
And our Personal Silicon Foundry™ gives you rapid design, testing and programming capabilities for programmable logic devices.

FUTURENET TALKS TO THE WORLD OF CAE/CAD. An open architecture and IBM® PC platform let you easily integrate our CAE system into your engineering environment. FutureNet offers many post processors to translate schematics into files compatible with your in-house CAD system. Complete database description and source software for net lists and drawing translators are also available.

And because DASH is an accepted CAE standard, it gives you immediate access to more than two dozen gate array foundries, as well as a wide variety of engineering service bureaus.

FUTURENET PROTECTS YOUR CAE INVESTMENT. We are committed to continually enhancing our CAE product line. Each new software version is compatible with the last, so you can always use your existing drawing files.

And you'll never have to worry about outgrowing your system. Our 32-bit co-processor gives you the power to add high performance logic simulation and PCB layout capability within the same platform. This flexible hardware design will also let you easily take advantage of tomorrow's new and more powerful processing capabilities.



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- Most widely used schematic designer
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- Help menus and on-line documentation
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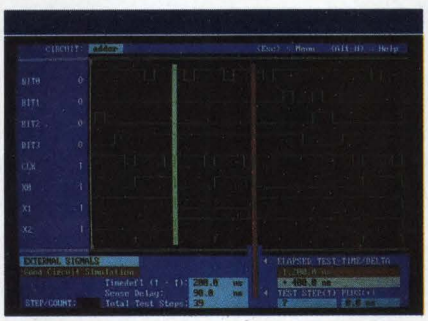

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- Rivals mainframe performance
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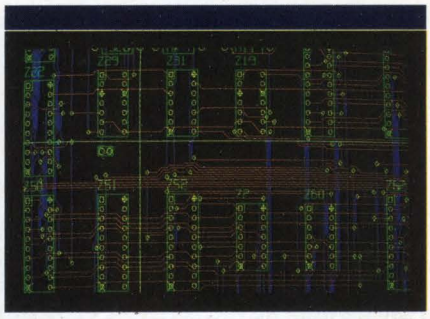
- Stimulus language simplifies test vector generation
- Simulates at transistor, gate, functional or behavioral level
- ASIC libraries and optional hardware modeler



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- Board capacity up to 32" X 32"
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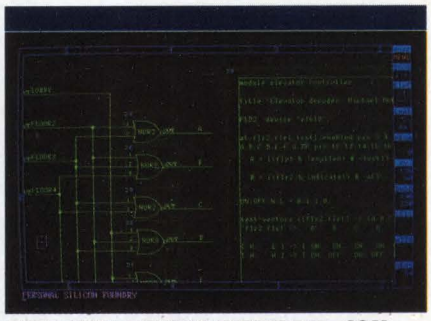

PERSONAL SILICON FOUNDRY: CONCEPT TO SILICON IN THREE HOURS.

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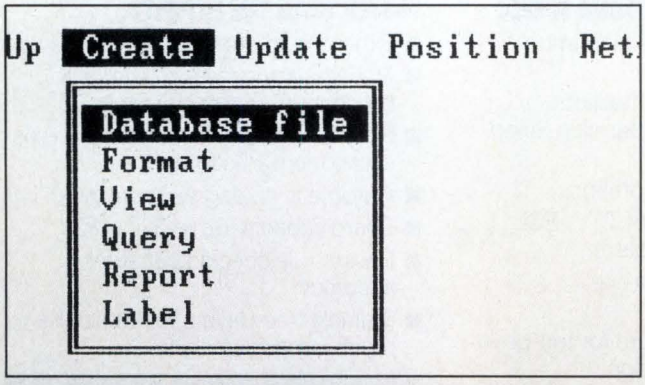
The database used now be used

Introducing dBASE III PLUS.™

The PLUS stands for all the improvements we've made to the world's number one selling database management software.



The Assistant helps beginning users accomplish day-to-day data management tasks without programming.

Mind you, dBASE III PLUS still has the powerful dBASE programming language, dot prompt, and all the features that have made dBASE III the standard of the industry.

We've simply raised the standard.

And just as dBASE III introduced more power to the people, our new dBASE III PLUS introduces more people to the power.

People who aren't all that crazy about programming, for example.

The Assistant feature in dBASE III PLUS now provides them with new easy-to-use pull-down menus for creating, using and modifying multiple databases.

So now anyone who can manage a simple cursor can manage day-to-day data management tasks. Without programming.

And by using our new Screen Painter, anyone can create custom screens. Without programming.

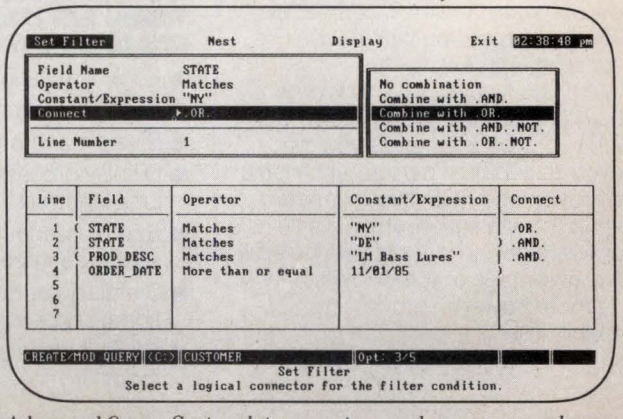
Or using View, access related information in several databases at one time. Without programming.

With Advanced Query System, another new non-programming feature, any user can build complex queries just by selecting from the dBASE III PLUS pull-down menus.

For rapidly creating entire programs, there's even a new Applications Generator.

And for all those who wish to learn to program, the Assistant can be of further assistance. By teaching you programming commands as you go along. Without disrupting your work flow.

These are only a few of the dBASE III PLUS features that can help new users quickly get up to speed. And experienced users quickly increase their speed. (Sorting, for example, is up to two times faster and indexing up to ten times faster than dBASE III.)



Advanced Query System lets you set up and answer complex queries without programming.

by more people can by more people.

And it's the fastest way to network those users, too. Because now, true multi-user capabilities for local area networking are built right in.

dBASE III PLUS can also help put developers in the fast lane. With a new Data Catalog and more than 50 new commands and functions. Plus code encryption and linking, improved debugging aids, assembly language calls and much more.

For the name of the Ashton-Tate® dealer nearest you,* call 800-437-4329, Extension 2861.**

And get your hands on dBASE III PLUS.

It's the software more people can look forward to using.

*Upgrades are available to all dBASE III owners. **In Colorado call (303) 799-4900, Extension 2861. Requires IBM® PC or 100% compatible. Trademarks/owners: Ashton-Tate, dBASE III PLUS/Ashton-Tate; IBM/International Business Machines Corp.
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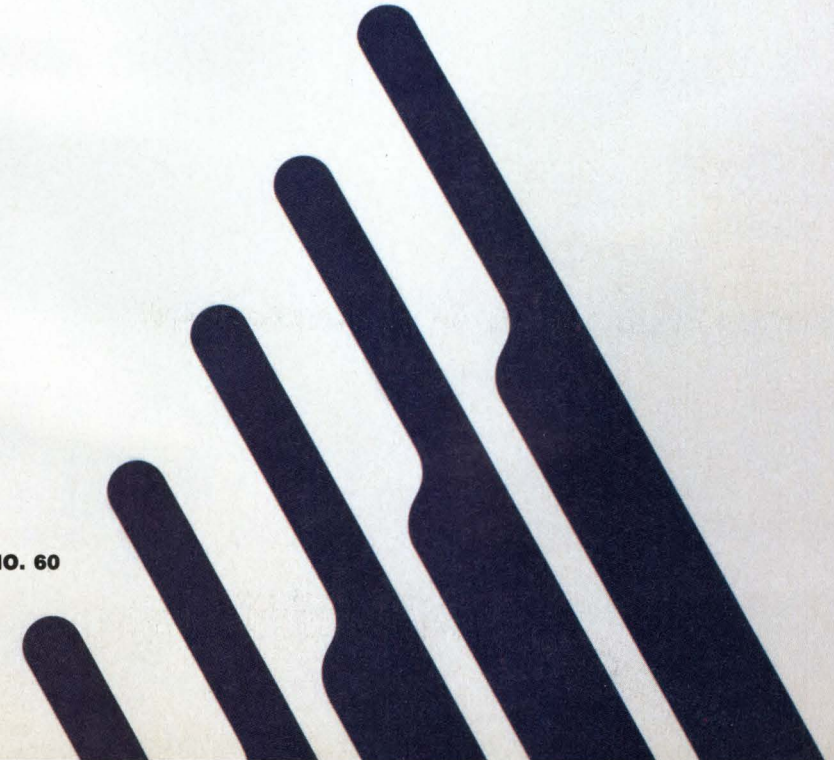
dBASE III PLUS

The data management standard.



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The world's most advanced

CMOS macrocells have arrived.

Introducing a state-of-the-art selection of standard cells, including a 32-bit slice μP.

You can now design ASIC systems-on-a-chip using a library of CMOS LSI standard cells. Included are the world's first 16-bit and 32-bit bit-slice processor cells, EPROMs and peripherals. All manufactured using a 1.2 micron channel length CMOS process.

The LSI cells were developed by WaferScale Integration Inc. (WSI) and will be alternate sourced by RCA. WSI will also offer RCA's CMOS standard cell library.

First 32-bit bit-slice processor cell.

The 32-bit CMOS CPU cell replaces eleven discrete bipolar ICs. It beats the performance of the 2901C bit-sliced-based system by 20% and saves 97% of the power, yet it is software compatible.

The 16-bit μP slice cell runs faster than bipolar speed, and replaces five off-the-shelf bipolar devices. Without rewriting microcode. Without adding glue parts.

The 4-bit μP slice cell is functionally identical to the bipolar 2901 4-bit slice, yet runs 25% faster. You can replace the bipolar part directly for instant improvement in system performance and power consumption.

Each μP is available as a cell in the library or as a standard IC.

CMOS EPROMs.

Another new LSI cell is a 1K x 16 CMOS UV EPROM with 55ns access time. Providing on-chip microcoding capability, this cell interfaces with 8-bit, 16-bit or 32-bit buses. An intelligent algorithm allows fast programming, achieved within 4 seconds. The EPROM cell uses only 20 μA in the standby mode and only 15mA in the active mode.

And it's also available as a 70ns 8K x 8 standard EPROM in 28-pin ceramic DIP or 24-pin bipolar PROM footprint...at very competitive prices.

Complete standard cell library.

The WSI cell library has been combined with the RCA library of over 300 verified cells to give you a very broad choice of LSI, MSI and SSI standard cells. Our CAD tools are extremely advanced and user-friendly. Our software supports all of the major workstations: Daisy,™ Mentor,™ Valid,™ even the IBM PC.

With our small geometry CMOS technology, you can reduce an entire PC board of capability onto a single ASIC chip. You benefit with smaller power supplies, lower system cost, smaller system-level boards and higher system reliability.

Working through one of our design centers, you get fast, accurate service. Simulation and testability steps built into the design flow allow us to achieve almost 100% first time success.

Data base scaling upgrades without redesign.

Your design can take advantage of next generation l-micron CMOS geometries without redesign. So you'll sit back and watch your ASIC get faster all the time.

High Rel, too.

These standard cells are also characterized over the full military temperature range.

Choose your source and call today.

For more information, or to get started on your design, call your RCA or WSI sales office or design center today.

WaferScale INTEGRATION, INC.

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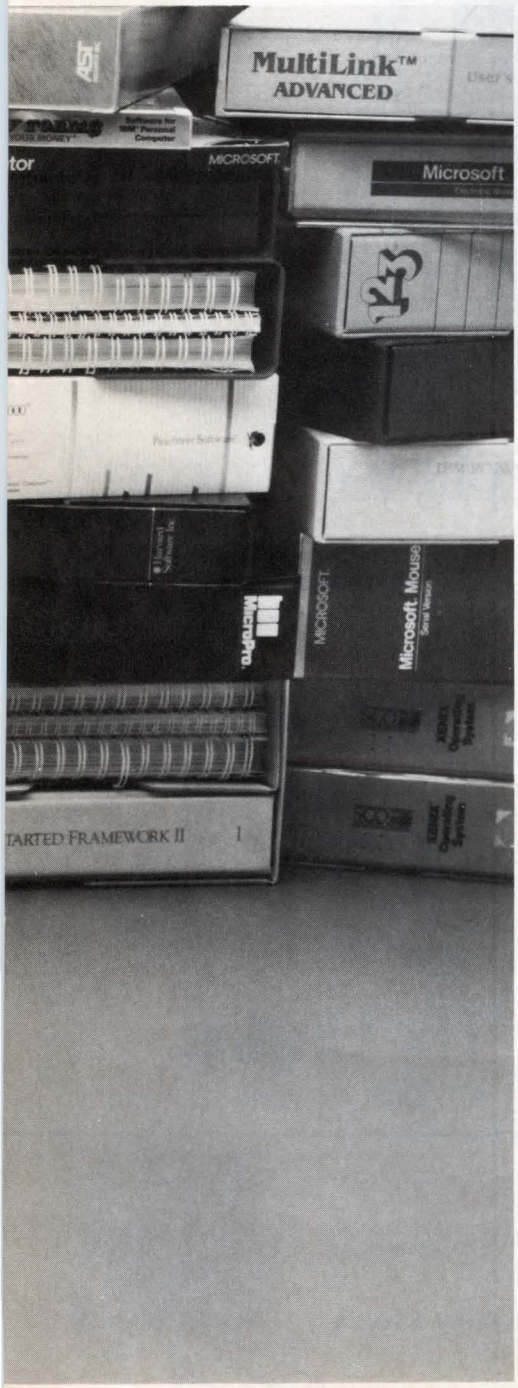
CIRCLE NO. 61

The WYSEpc. It but expensive.

runs everything



For this incredibly low price, you get everything but bulk. The WYSEpc runs virtually every popular IBM-compatible software package.

And $1499 *includes* dual floppy drives, 14″ tilt/swivel monitor, height-adjustable keyboard, 256K RAM, two serial ports, one parallel port, MS-DOS with GW-BASIC, manuals, the works.

How can we do it for $1499? We leave out the ugly and don't charge you for it. That's how we got to be the world's leading independent manufacturer of terminals, shipping more than anybody but IBM.*

The WYSEpc is also available in an IBM PC/XT compatible model with a 10-Megabyte or 20-Megabyte Winchester disk, and a color graphics option.

For more information about the WYSEpc or our full line of computer display products, write or call toll-free, today.

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*Dataquest 1985 mid-year terminal update.

WYSE

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Call 1-800-GET-WYSE

☐ **Yes, please send me detailed information on the WYSEpc.**
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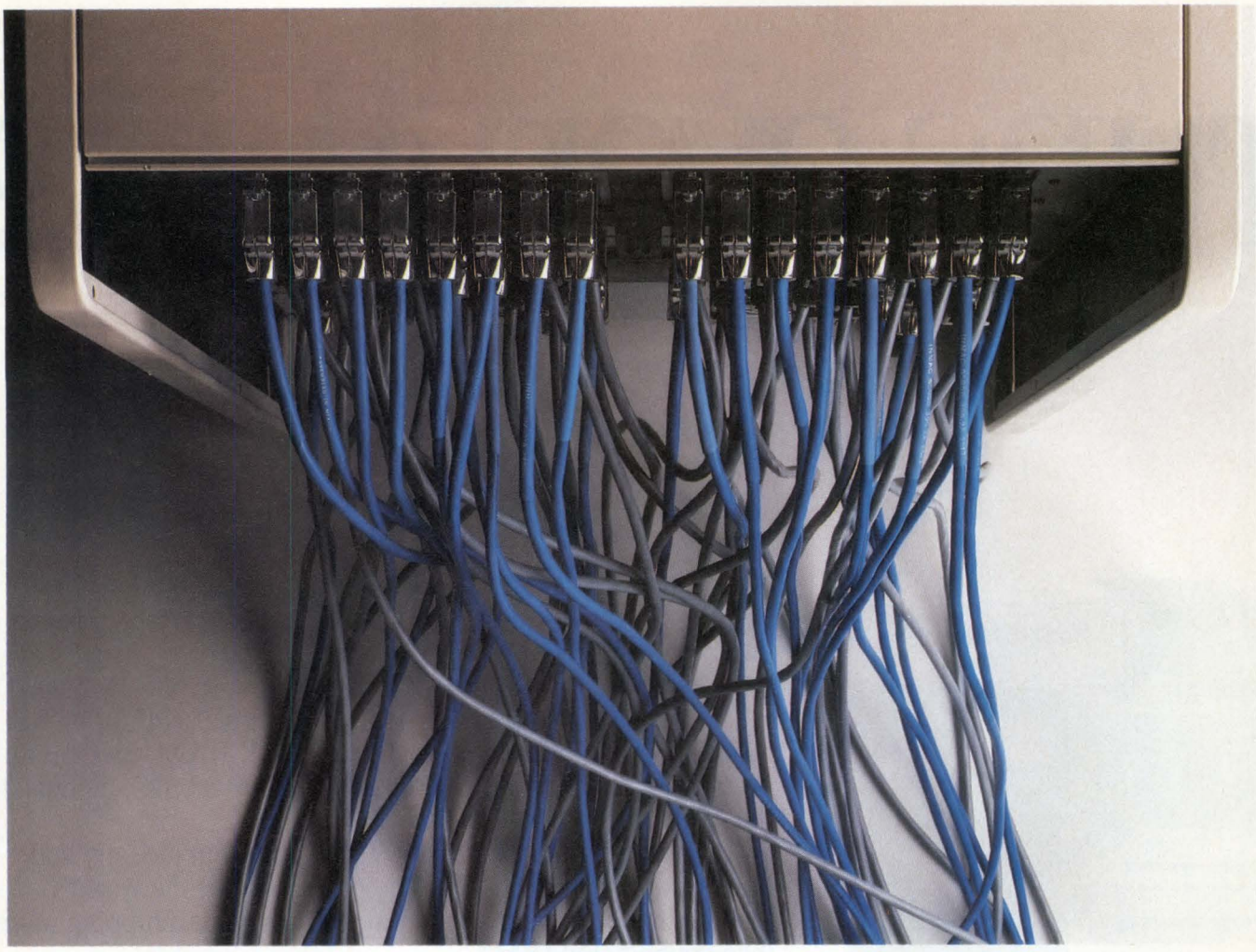


How many more reasons do you need to Unplug your computer?

Until now, connecting 128 terminals to your computer meant one thing. A myriad of cards taking up precious space on the backplane. And accomplishing nothing but communications. All of which could frustrate almost any self-respecting system designer into hanging up his calculator.

Well, at Systech, we understand the serial communications problems of a multi-user system. So we developed The Unplug™ asynchronous distributed multiplexer that can be used with any Multibus,® VMEbus or Multibus® II system.

The Unplug can take those 128 connections off the back of the computer and turn them into just one. And presto, you've got all the expansion slots you need for more important things. Like disks. Streaming tapes. More CPU power. A synchronous communications processor. And your imagination.

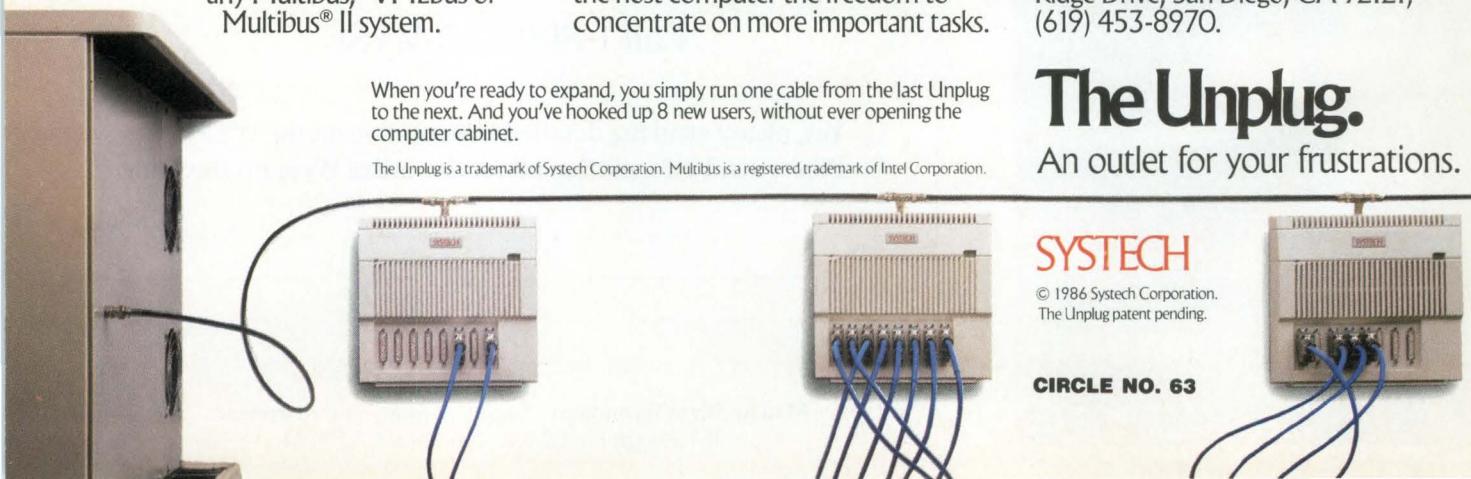
You see, what we did was move part of the computer's operating system—the part devoted to managing traffic to and from the terminals—out of the computer and into The Unplug. Giving the host computer the freedom to concentrate on more important tasks.

We know it sounds simple. And the truth is, it is. In fact, you might wonder why no one thought of it before. Then again, no one else has our commitment to make your job easier. And a lot more gratifying.

Just give us a call at Systech to hook up with The Unplug. Then you can start figuring out what you want to add on next.

Instead of trying to figure out how to untangle all those wires.

Systech Corporation, 6465 Nancy Ridge Drive, San Diego, CA 92121, (619) 453-8970.



When you're ready to expand, you simply run one cable from the last Unplug to the next. And you've hooked up 8 new users, without ever opening the computer cabinet.

The Unplug is a trademark of Systech Corporation. Multibus is a registered trademark of Intel Corporation.

The Unplug.

An outlet for your frustrations.

SYSTECH

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The Unplug patent pending.

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Let Lab Boss™ turn your IBM PC into a powerful instrument controller.

You can spend thousands of dollars for a dedicated instrument controller. Or a few hundred for a controller that's dedicated to you and your IBM PC.

Lab Boss™ from National Instruments puts you and your IBM PC (or compatible) firmly in charge of GPIB instruments. From sophisticated laboratory equipment, like digitizing oscilloscopes and spectrometers, to standard printers, plotters, tape drives and more. At data transfer speeds that are the highest in the industry.

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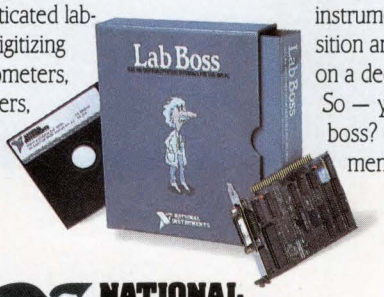

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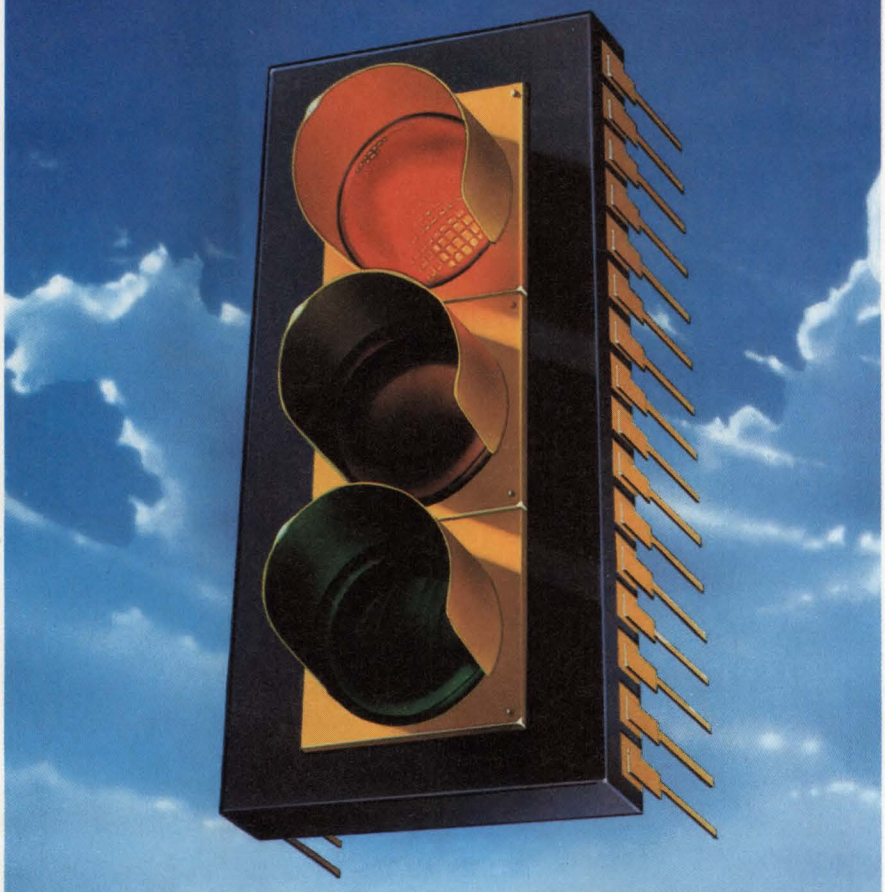
GREATER CONTROL

THE AT&T X.25 PROTOCOL CONTROLLERS.

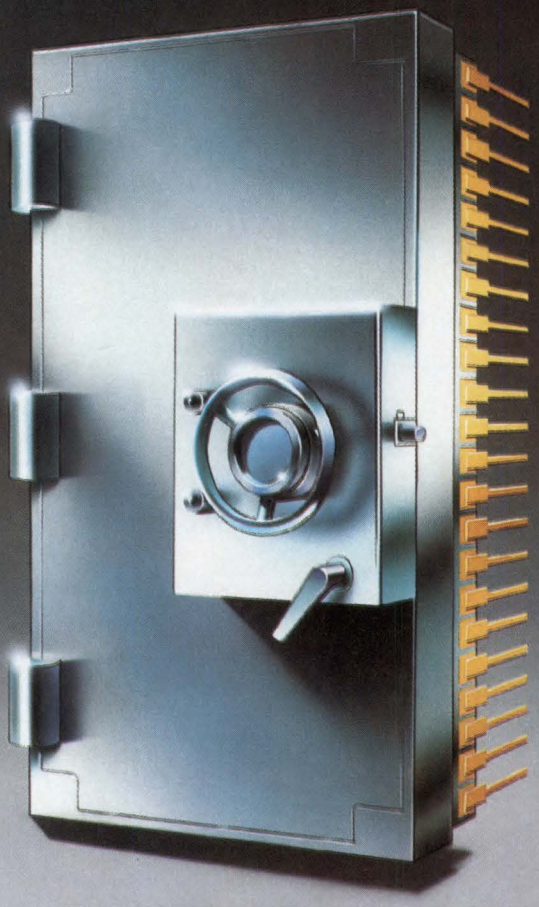


Some protocol devices need a lot of control from the microprocessor and software. Not AT&T's T7100 and T7102 X.25 Protocol Controllers. They feature a large set of programmable registers. And, because almost all the control functions are handled on-chip, level 2 protocol software can be reduced by more than 90%.

Programmable timers allow our X.25 Protocol Controllers to function in a wide range of applications from PCs to satellites. For the best way to get your X.25 protocol under control, call **1 800 372-2447**, or write to AT&T, Dept. KB, 555 Union Blvd., Allentown, PA 18103.

MAXIMUM SECURITY

THE AT&T DIGITAL ENCRYPTION PROCESSOR AND RANDOM NUMBER GENERATOR.

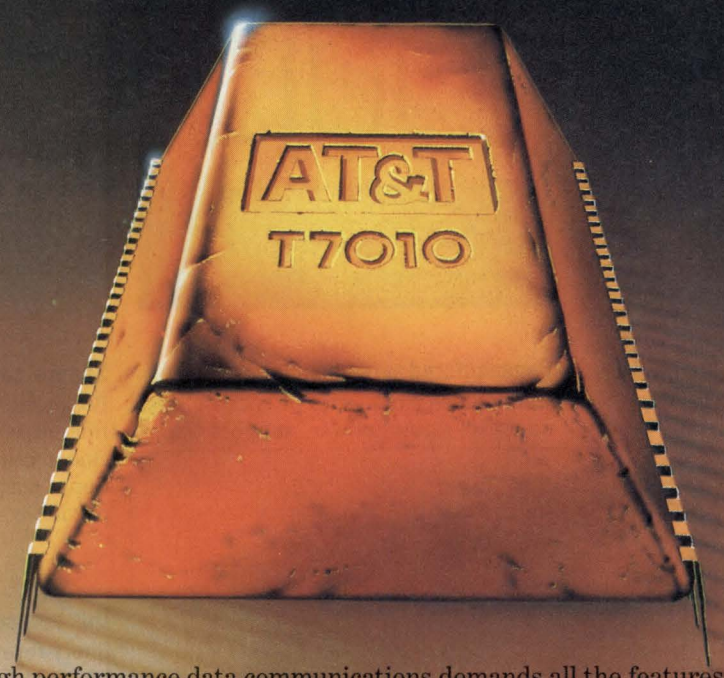


Only our T7000A Digital Encryption Processor offers all four modes of DES encryption, including 1,8 or 64-bit cipher feedback. Four on-chip keys and initial value registers allow a single data stream to be encrypted up to four times, for maximum security. Or, if you prefer, up to four data streams can be encrypted at the same time and then multiplexed.

The T7000A has a high, 1.8 Mb/s throughput with low-power CMOS technology. AT&T also offers the T7001, the only random number generator in chip form with a free-running oscillator for true random number generation. To lock up DES security, call **1 800 372-2447**, or write to AT&T, Dept. KB, 555 Union Blvd., Allentown, PA 18103.

FEATURE RICH

THE AT&T T7010 SWITCHED CAPACITOR MODEM.



High performance data communications demands all the features of the T7010 Switched Capacitor Modem. This compact, 40-pin package has speeds up to 1200 bps, which can be doubled with the use of a digital signal processor.

The T7010 Modem exceeds Bell 212A and CCITT V.22 standards, handles synchronous and asynchronous transmissions, performs self-diagnosis, and minimizes error rates and noise levels. For feature-packed performance, call 1 800 372-2447, or write to AT&T, Dept. KB, 555 Union Blvd., Allentown, PA 18103.

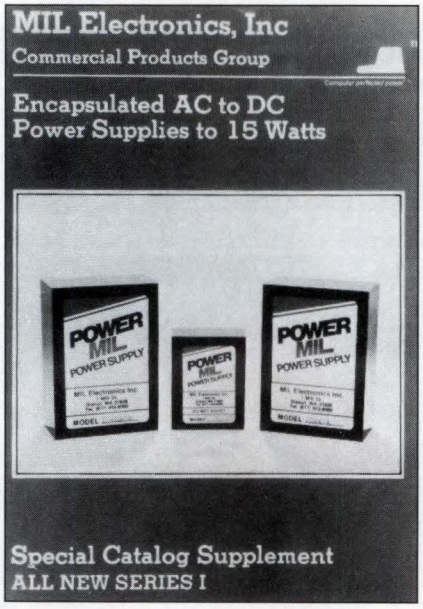
AT&T
The right choice.

LITERATURE

Networking connections
Over 2,000 products for networking and wiring of voice and data systems, such as fiberoptic, coaxial and multiconductor copper interconnection products, are included in an 84-page catalog. **AMP**, Harrisburg, PA. **Circle 156**

Add-in memory
Twenty-page full-color catalog and selection guide presents data to aid design engineer on range of add-in memory products for Versabus, VME, DEC, IBM RT PC and Sun Microsystems 3 buses. **Clearpoint**, Hopkinton, MA. **Circle 157**

Signal-to-noise analysis
Four-page application note presents advantages of Fast Fourier Transform speeds for determining signal-to-noise analysis of analog-to-digital converters. **ILC Data Device**, Bohemia, NY. **Circle 158**



Encapsulated power supplies
Catalog describes series of encapsulated ac-to-dc linear power supplies from microminiature up to 15 W that provide over 50,000-h MTBF under continuous extreme conditions. **MIL Electronics**, Dracut, MA. **Circle 159**

Micromotors
Catalog contains 52 pages of comparison data on disk and dc ironless motor technologies as well as product data, specs, dimensions and drawings of stepper motors, drive circuits and dc motors. **Portescap U.S.**, Valley Forge, PA. **Circle 160**

VMEbus guides
Series of application and configuration guides aid system integrators in selection of VMEbus subsystems. **VME Microsystems Int'l**, Huntsville, AL. **Circle 161**

Secure communications
Brochure on full line of stand-alone fiberoptic communication modules includes primer on Tempest communications networks for secure data applications. **Versitron**, Washington, DC. **Circle 162**

Bus-compatible peripherals
Short-form brochure contains specs on board-level microcomputer products for IBM PC, VMEbus and Multibus compatible systems used in automation, process control and scientific research. **Anasco**, Danvers, MA. **Circle 163**

Surface mount technology
Issues involved in designing connectors for surface mounting are described in a tutorial contained in a 24-page handbook. Illustrations, definitions and tables are included. **Molex**, Lisle, IL. **Circle 164**

Data communications products
Line of data communications products described in 24-page catalog includes hand-held test sets, data traps, printers, modems, data switches and test equipment. **International Data Sciences**, Lincoln, RI. **Circle 165**

Power-op amps
Handbook contains 120 pages of application notes describing how to achieve

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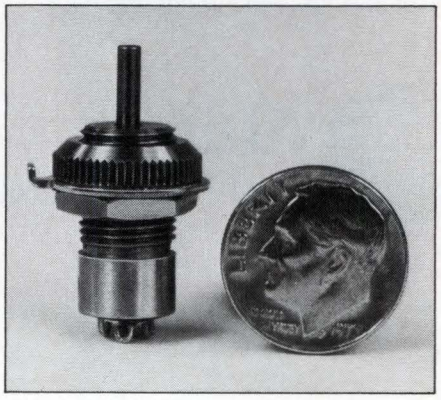

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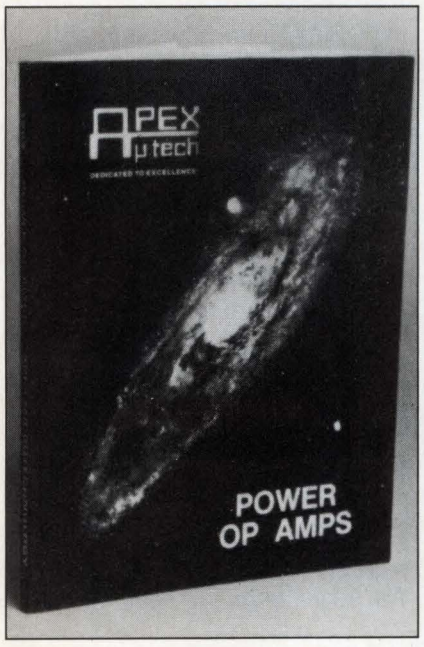

high performance from power op amps, as well as data sheets for a wide selection of the devices. **Apex Technology**, Tucson, AZ. **Circle 166**

Test environment

Integration of a design and test environment based on Lasar Version 6 system for logic and fault simulation in circuit board and gate array development detailed in 12-page brochure. **Teradyne**, Boston, MA. **Circle 167**

Computer cables

Catalog describes cables and accessories for installing and expanding computer systems, LANs and data communications systems. **Support Systems International**, Richmond, CA. **Circle 168**

ISDN device testing solutions

Solutions for testing integrated services digital network devices and information on dc parametric, microprocessor interface, transmitter and receiver functionality, and device features are described in brochure. **Teradyne**, Boston, MA. **Circle 169**

Indicator lights

Source book and user's guide contains 208 pages of technical and selection data on electronic, industrial and commercial applications for LED, incandescent and neon indicator lights. **Industrial Devices**, Edgewater, NJ. **Circle 170**

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JAN 20-21—Buscon/87 West and **Syscon**, Los Angeles Int'l Airport Hilton Hotel, Los Angeles, CA.
INFORMATION: Edward Grazda, 17100 Norwalk Bldg, Suite 116, Cerritos, CA 90701.
Tel: 213/402-1610

JAN 20-23—UniForum 1987, Washington Convention Center, Washington, DC.
INFORMATION: Robert Linke, 2400 E Devon Ave, Suite 205, Des Plaines, IL 60018.
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JAN 28-30—Computer Graphics New York '87, Jacob K. Javits Convention Center, New York, NY.
INFORMATION: Justin Webb, Exhibition Marketing & Management, 8300 Greensboro Dr, Suite 690, McLean, VA 22102.
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FEB 3 & 5—Bustop Conferences, Hotel Europa, Raleigh, NC (FEB 3) and Radisson Orlando, Orlando, FL (FEB 5).
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FEB 9-12—Communications Networks '87, Washington Convention Center, Washington, DC.
INFORMATION: Nancy Thayer, CW/Conference Management Group, Box 9171, Framingham, MA 01701.
Tel: 617/879-0700

FEB 10-12—Systems Design & Integration Conference, Santa Clara Convention Center, San Jose, CA.
INFORMATION: Alexes Razevich, 8110 Airport Blvd, Los Angeles, CA 90045.
Tel: 213/772-2965

FEB 10 & 24—Invitational Computer Conferences, San Jose, CA (FEB 10) and Dallas, TX (FEB 24).
INFORMATION: Suzanne Hubner, B.J. Johnson & Associates, 3151 Airway Ave, C-2, Costa Mesa, CA 92626.
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FEB 16-19—Electronic Imaging West, Anaheim Convention Center, Anaheim, CA.
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FEB 23-26—Compcon Spring '87, Cathedral Hill Hotel, San Francisco, CA.
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MAR 17 & 19—Bustop Conferences, Adams Mark Hotel, Philadelphia, PA (MAR 17) and Sheraton National, Arlington, VA (MAR 19).
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MAR 24-26—Southcon, Georgia World Congress Center, Atlanta, GA.
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MAR 22-26—Computer Graphics '87, Philadelphia Civic Center, Philadelphia, PA.
INFORMATION: National Computer Graphics Association, 2722 Merrilee Dr, Suite 200, Fairfax, VA 22031.
Tel: 703/698-9600

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SHORT COURSES

JAN 22-23—Micro-Mainframe Links, San Diego, CA.
INFORMATION: Yolande Amundson, Integrated Computer Systems, Box 3614, Culver City, CA 90231.
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JAN-APR—MAP/TOP: Networking in Industrial Environments, various locations and dates.
INFORMATION: Yolande Amundson, Integrated Computer Systems, Box 3614, Culver City, CA 90231.
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FEB 23-27—Microcomputers in Control Systems, Washington, DC.
INFORMATION: Merril Ann Farber, Continuing Engineering Education Program, The George Washington Univ, Washington, DC 20052.
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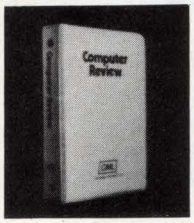

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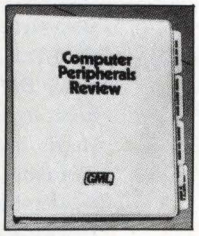

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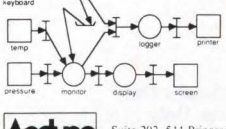

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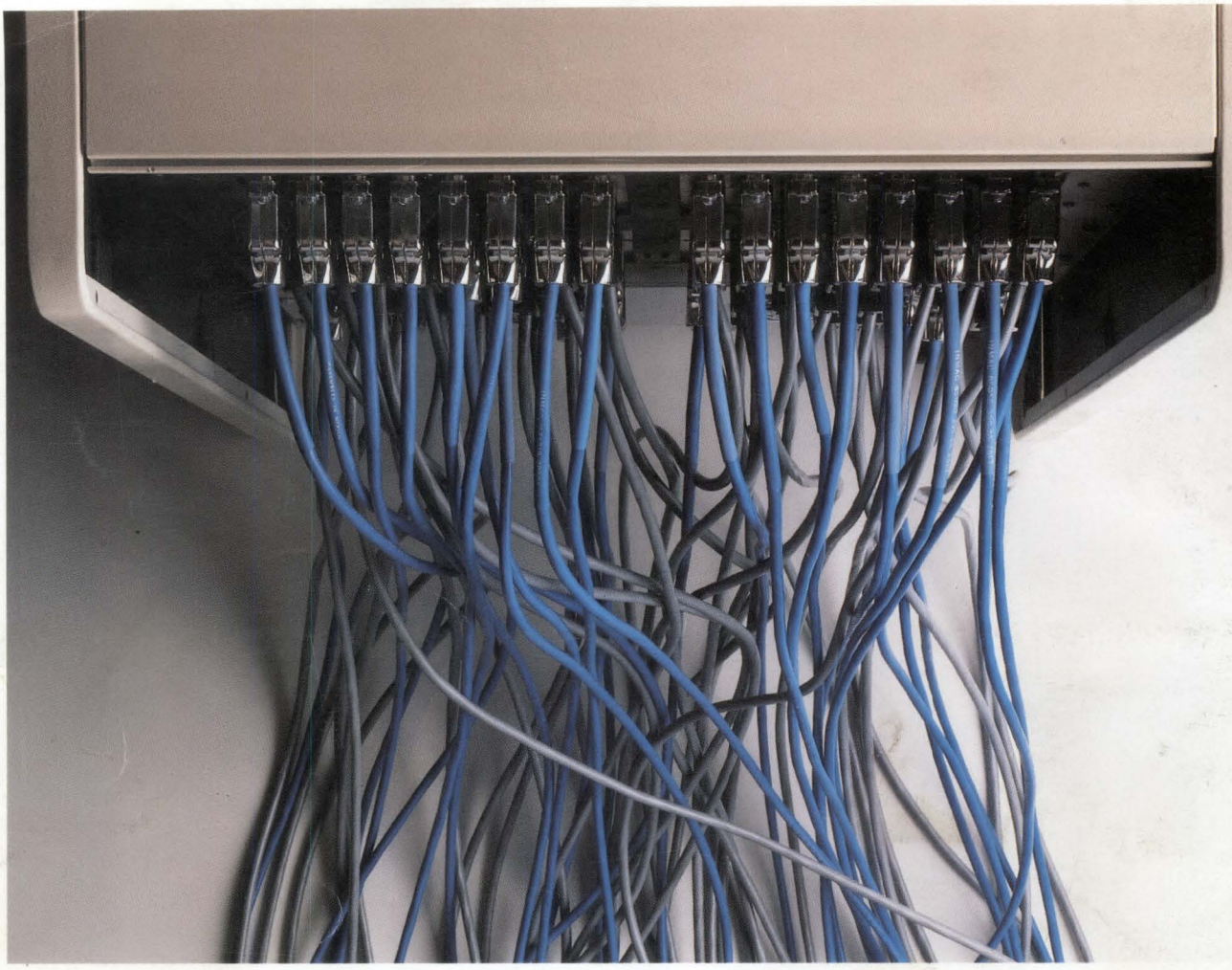

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Until now, connecting 128 terminals to your computer meant one thing. A myriad of cards taking up precious space on the backplane. And accomplishing nothing but communications. All of which could frustrate almost any self-respecting system designer into hanging up his calculator.

Well, at Systech, we understand the serial communications problems of a multi-user system. So we developed The Unplug™ asynchronous distributed multiplexer that can be used with any Multibus,® VMEbus or Multibus® II system.

The Unplug can take those 128 connections off the back of the computer and turn them into just one. And presto, you've got all the expansion slots you need for more important things. Like disks. Streaming tapes. More CPU power. A synchronous communications processor. And your imagination.

You see, what we did was move part of the computer's operating system—the part devoted to managing traffic to and from the terminals—out of the computer and into The Unplug. Giving the host computer the freedom to concentrate on more important tasks.

We know it sounds simple. And the truth is, it is. In fact, you might wonder why no one thought of it before. Then again, no one else has our commitment to make your job easier. And a lot more gratifying.

Just give us a call at Systech to hook up with The Unplug. Then you can start figuring out what you want to add on next.

Instead of trying to figure out how to untangle all those wires.

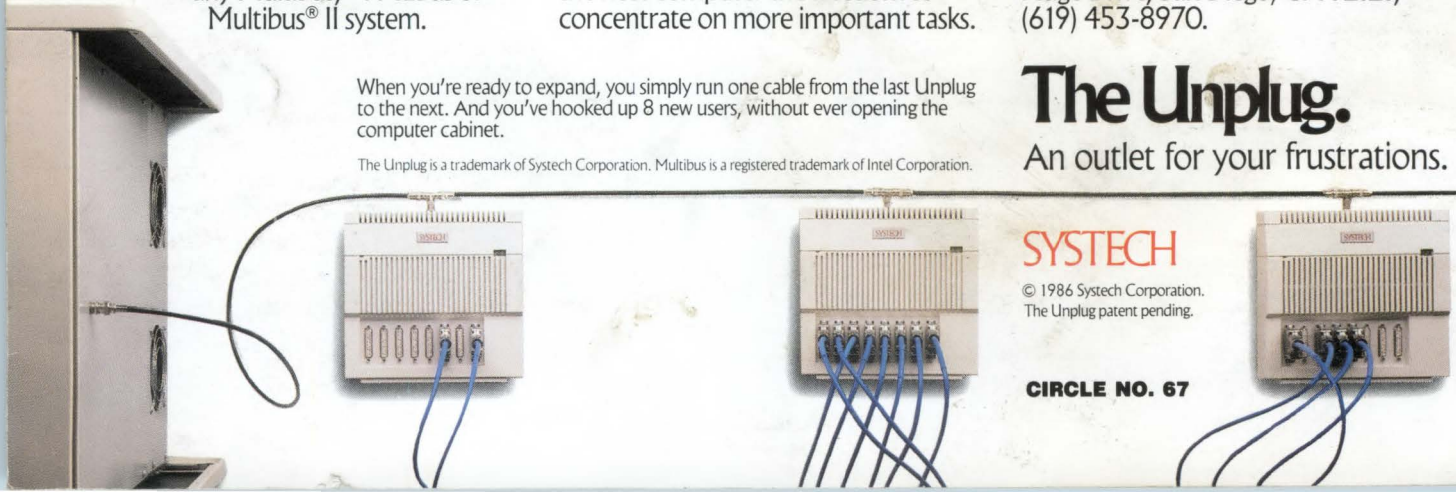
Systech Corporation, 6465 Nancy Ridge Drive, San Diego, CA 92121, (619) 453-8970.

When you're ready to expand, you simply run one cable from the last Unplug to the next. And you've hooked up 8 new users, without ever opening the computer cabinet.

The Unplug is a trademark of Systech Corporation. Multibus is a registered trademark of Intel Corporation.

The Unplug.

An outlet for your frustrations.



SYSTECH

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The Unplug patent pending.

CIRCLE NO. 67