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COMPUTER DESIGN

THE MAGAZINE OF SYSTEM DESIGN AND INTEGRATION

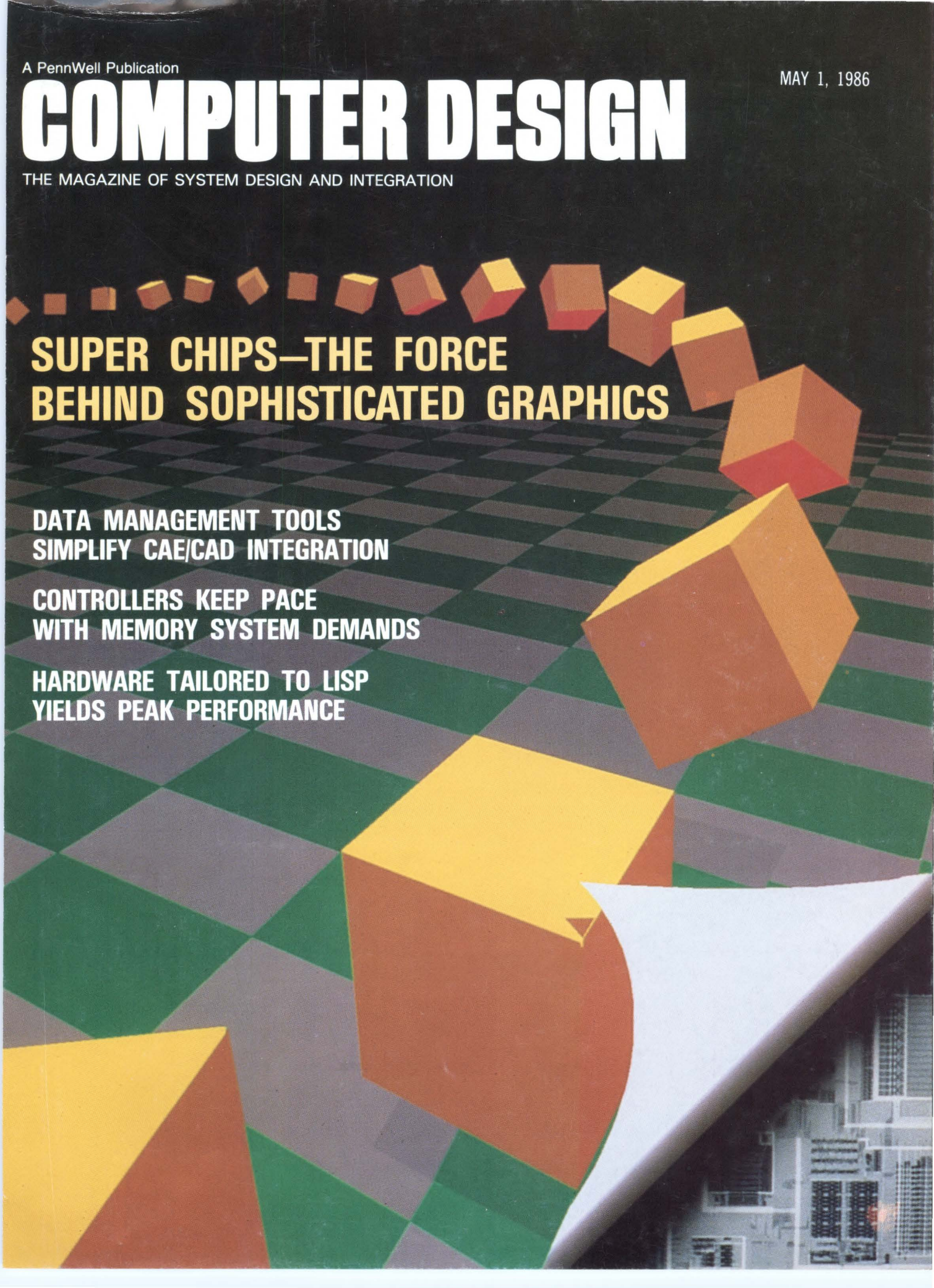
MAY 1, 1986

SUPER CHIPS—THE FORCE BEHIND SOPHISTICATED GRAPHICS

DATA MANAGEMENT TOOLS SIMPLIFY CAE/CAD INTEGRATION

CONTROLLERS KEEP PACE WITH MEMORY SYSTEM DEMANDS

HARDWARE TAILORED TO LISP YIELDS PEAK PERFORMANCE



PROMISE YOU JUST THE FASTEST AN IDEA FLY.

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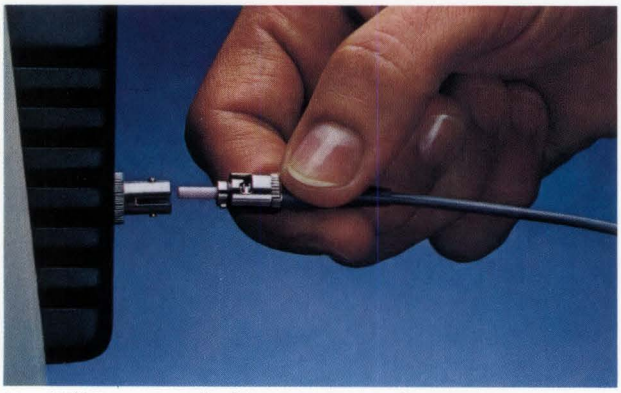
And our third-generation, single-chip Digital Signal Processor gives you the edge you need to design-in superior system performance at a competitive price.



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For local or long-haul transmission, AT&T offers a complete family of fiber optic products and apparatus.

In local area networks, our new ST™ Connector can actually double your network connections—or double the distance between connections—without affecting the fiber optic cable or electronics.

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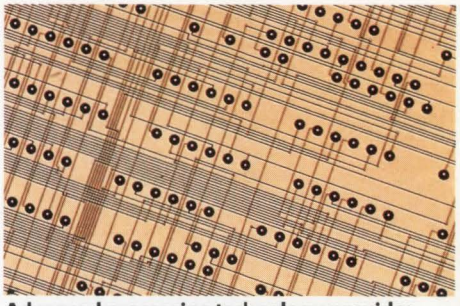
Our newest addition to the AT&T lightwave family—the ASTROTEC™ ceramic laser module—is a reduced-size, long-wavelength laser that offers highly reliable, low cost performance.



Advanced processing technology provides superior buried microvias in multilayer printed wiring boards.

News in ac plasma.

AT&T has just introduced a new lightweight, compact ac plasma display for alphanumeric and graphic images. It offers excellent visual characteristics in virtually unlimited applications.

We'll work with you, all the way.

Call us right from Day One, and we'll put our expertise at your disposal. Call us when you hit a snag, and we'll work out a solution together. After all, we've got the world's greatest problem-solvers on call—the men and women of AT&T Bell Laboratories.

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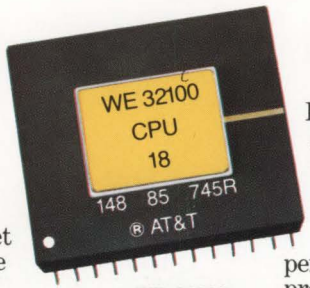
CIRCLE 1

AT&T DOESN'T IMMORTALITY... WAY TO MAKE

Today, the product that's first in the market is likely to win the biggest share of market.

So when you're racing to get a great idea off the ground—ahead of your competitors—you need more than just a "supplier."



WE®32100, heart of the first full 32-bit chip set.

You need a company with a broad line of high-performance components and electronic systems. A company with a networking point-of-view, an end-to-end capability, and the people and resources to assure all-out technical support.

AT&T.

Ready now to offer you the total commitment to quality and reliability that we've always insisted on in the systems and products we develop for ourselves.

Ready now to deliver solutions.

We'll keep you on the leading edge.

Because that's where AT&T Bell Laboratories keeps us.

Our new 32-Bit UNIX™ Microsystem, for example, delivers performance others only promise. It's a chip set that's 100% complete, 100% CMOS, and 100% TTL-compatible—fully able to reduce your design time by as much as 50 percent.

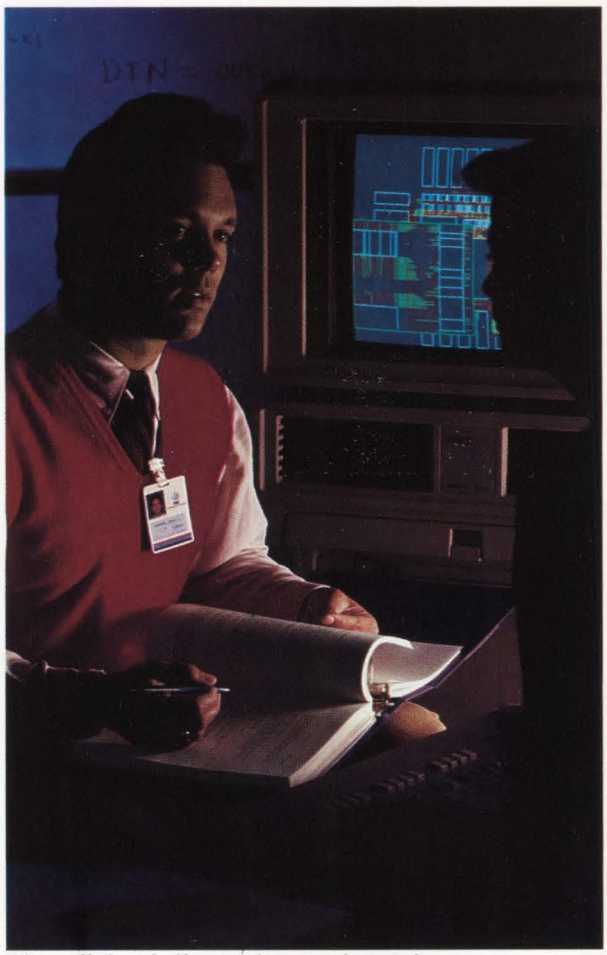
In data communications devices, we're state-of-the-art every step of the way. (As you might expect from the company that developed the world's biggest, most reliable communications network.)

Right now, for example, AT&T is the only company in volume production of a microprocessor-controllable, single-package modem that can handle up to 2400 bits per second.

Our Digital Encryption Processor is the only software-programmable, encryption processor available.

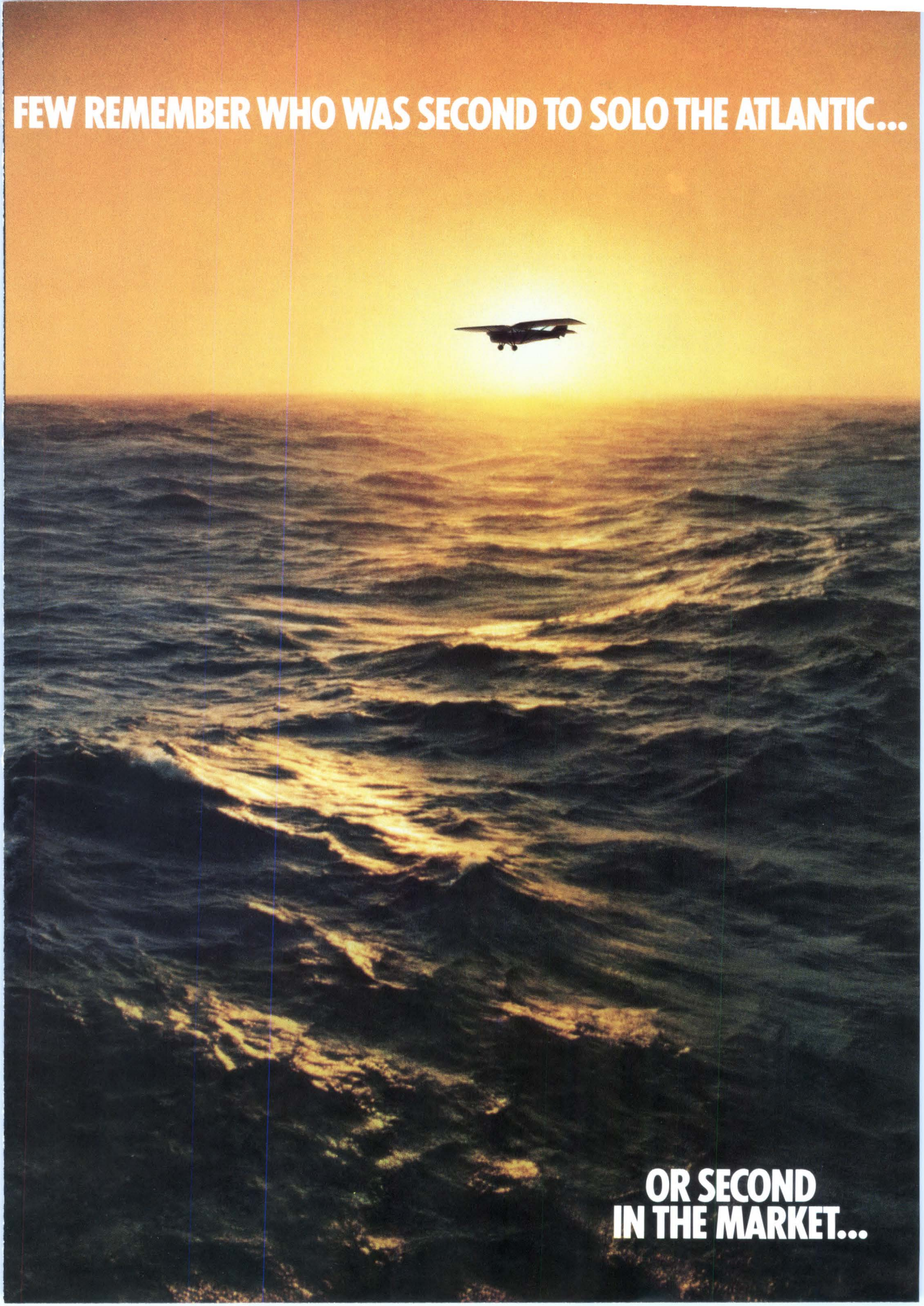
And our X.25 Protocol Controllers offer the widest range of applications, from PCs to satellites.

In memory, not only are we currently delivering an American-made 256K DRAM, but we offer a range of



When off-the-shelf won't do, our advanced custom design gives you the edge.

Few remember James Mollison, the second man to fly solo across the Atlantic, because 'Lindy' did it first.


FEW REMEMBER WHO WAS SECOND TO SOLO THE ATLANTIC...
OR SECOND
IN THE MARKET...

Model 6500 Streaming Cartridge Recorder

WE'RE DELIVERING!

It's true — the 'Handful' is going out the back door by the truckload. More and more people are discovering the superior features of Model 6500 — features such as it's non-moving hard coated head tape loading system; it's direct drive motor; it's faster speed — the large data buffer has a reposition time of 600ms, allowing Model 6500 to maintain streaming longer than any other drive. And Model 6500 is available in QIC-36 (half-high) QIC-02 and SCSI.

Finally, Model 6500 is elegantly simple in mechanical design — designed for long, dependable service.

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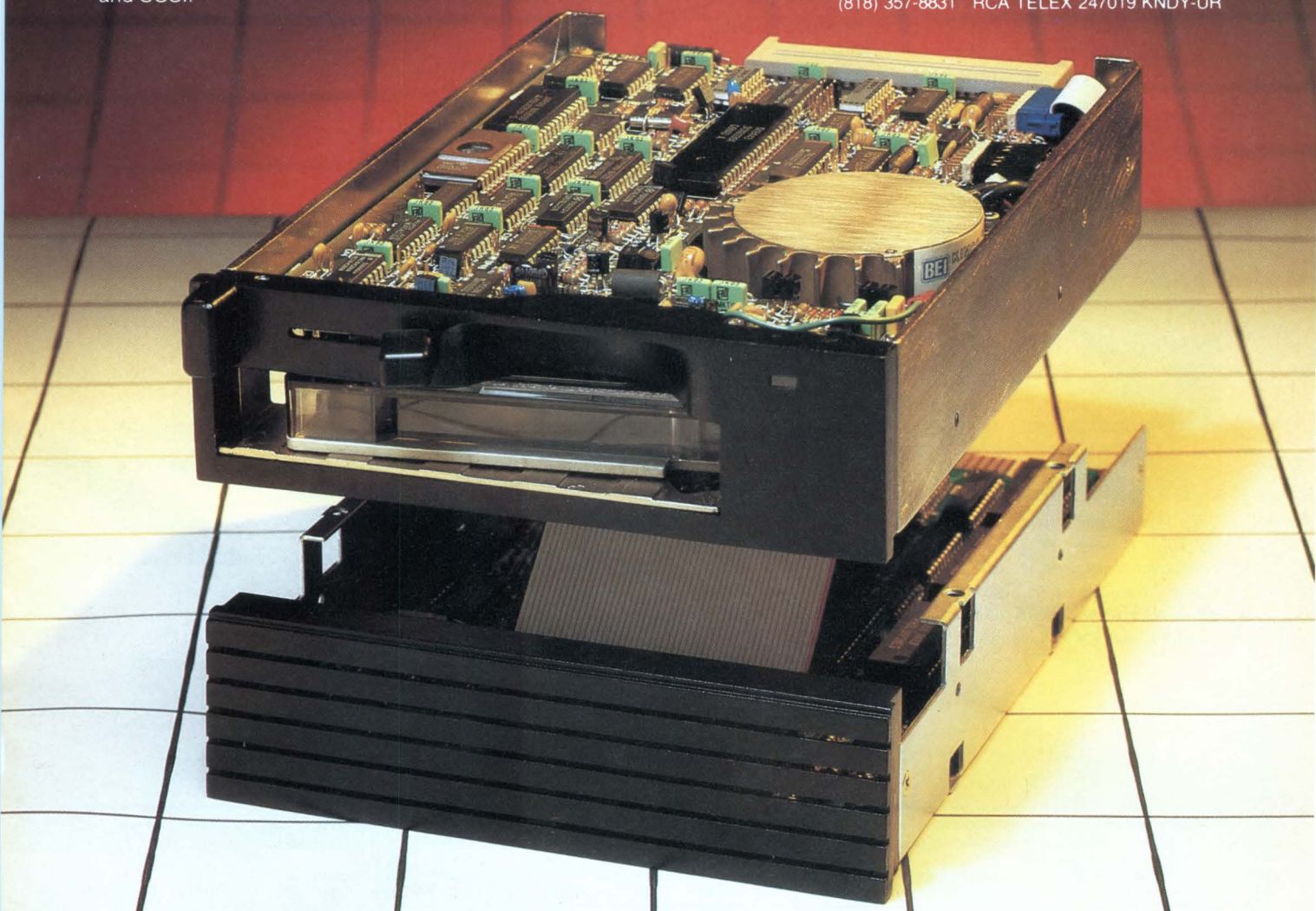

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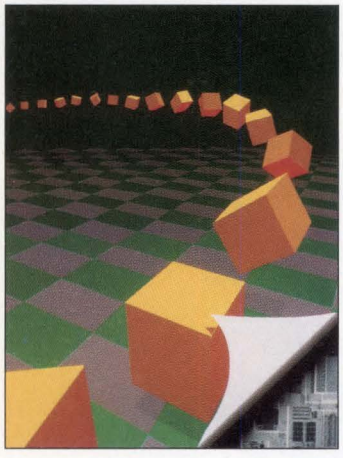
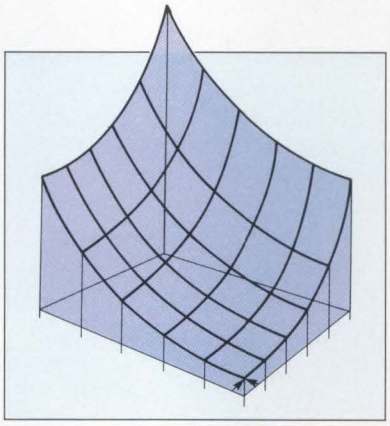
SPECIAL REPORT ON GRAPHICS TECHNOLOGY



This issue's cover was designed by John Bonner. It was computer-drawn at Visual Conspiracy (Boston). The chip photo is Advanced Micro Devices' Am95C60.

SYSTEM TECHNOLOGY



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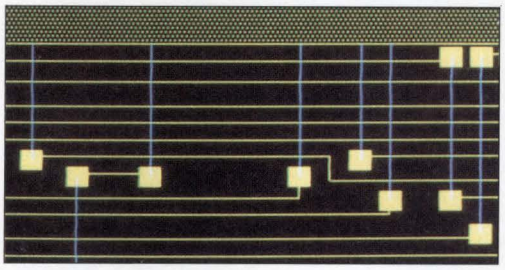
SYSTEM DESIGN

SYSTEM PRODUCTS



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Electro/86 / Mini/Micro Northeast

DEPARTMENTS

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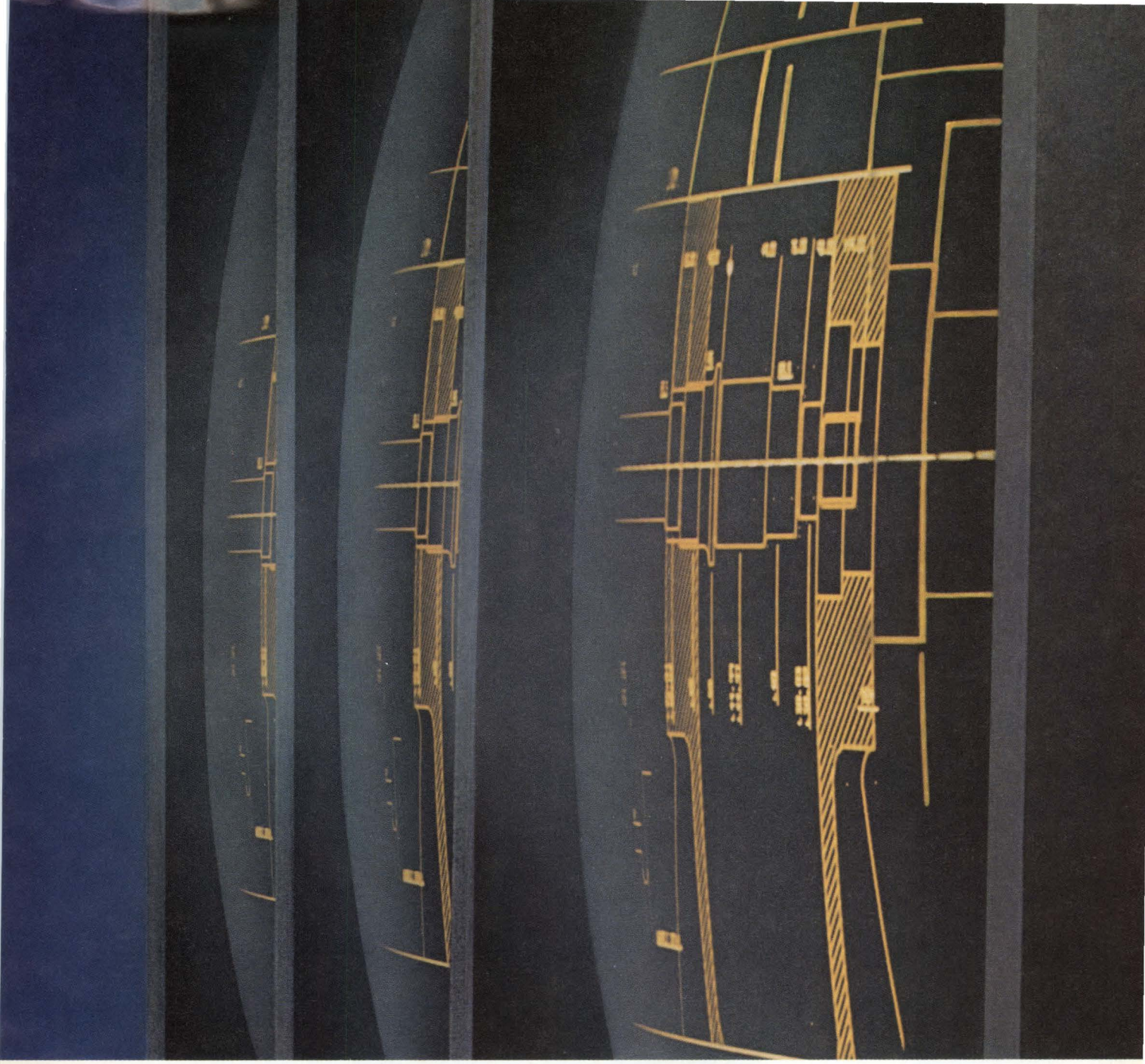

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The Siemens design team investigated a range of 32-bit solutions, and found only one that met all their needs: National's Series 32000 family.

Unlike other 8- and 16-bit processors being extended upward, the Series 32000 has no programmer-visible changes in architecture—throughout the entire family. So Siemens could develop any application the market demanded, now or in the future, without depreciating its existing software investment.

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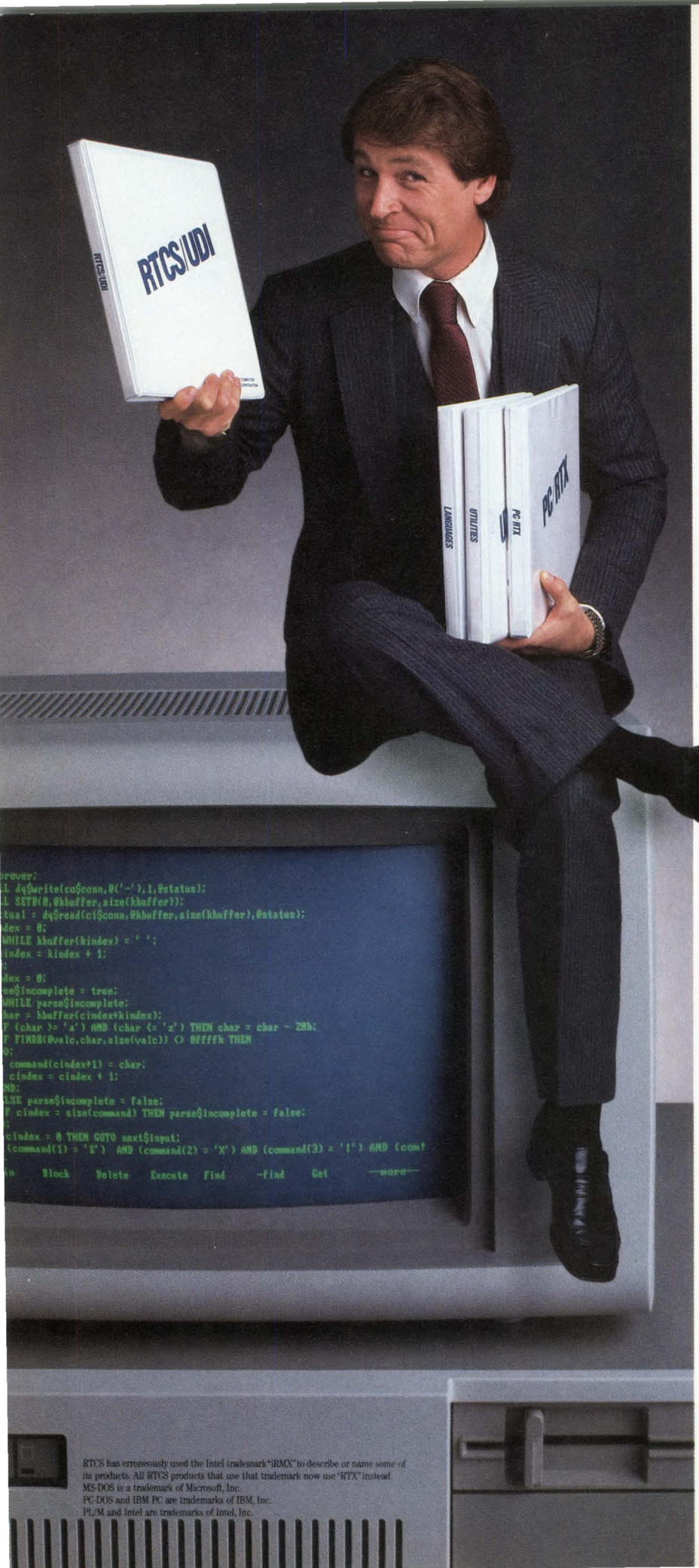
CIRCLE 4



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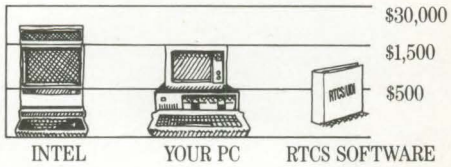

Also available from RTCS is PC/RTX, Real-Time, Multi-user Multi-tasking Operating System for IBM PC and others; Intel languages such as Pascal, Fortran, PL/M,™ and C Compilers; Utilities such as high level software debuggers, as well as a wide range of software support supplied with the RTCS/UDI at no additional cost.

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CIRCLE 5

UP FRONT

Emulation replaces simulation for programmable ICs

By offering an in-circuit emulator for design verification of its programmable Logic Cell Arrays, Xilinx (San Jose, CA) is challenging the industry axiom that simulation is the only way to verify random logic. The Xilinx Xactor emulator works exactly like in-circuit emulators built for microprocessors, but it downloads and executes a bit stream derived from the logic description of the chip rather than compiled code. This allows the user to plug in a logic cell array, verify its operation in the system and reprogram it if necessary. The Xactor emulator also allows users to probe the status of internal latches in the IC. Unlike simulation, emulation runs in real-time and can test more than just a few microseconds of system operation. —*R.G.*

First HI/TC tape cartridge drive appears with 5¼-in. form factor

IBM's 3480 half-inch tape cartridge now serves as the media basis for three different cartridge drives. In addition to the IBM-compatible drive offered by Aspen Peripherals (Longmont, CO) as an alternative to the 3480, and a Quarter-Inch Tape Cartridge format drive anticipated from Cipher Data (San Diego, CA), which uses a half-inch cartridge, there is now a half-inch cartridge drive bearing the specifications of the ad hoc HI/TC (Half-Inch Tape Cartridge) group. The Patriot drive by Computer Peripherals (Valley Forge, PA) adheres to the HI/TC standards for 240-Mbyte capacity, 250-kbyte/s transfer rate and serial serpentine recording, as well as ESDI/SCSI interface. But it packs it all into a 5¼-in. form factor using the same physical cartridge by means of an innovative tape path design. —*P.K.*

European electronics giant enters Multibus II arena

Siemens announced its first eight Multibus II boards for the European market at the Hannover Fair. The company, based in Munich, West Germany, joins Intel in the competition for the 32-bit microcomputer board market. Memory, controller and 80186 and 80286 CPU boards for Multibus II are now available. Karl Herschel, director of marketing for the Siemens board group, says that an 80386 CPU board will be announced later this month. A graphics controller board is expected to follow. Herschel notes that the company's goal is to gain at least 10 percent of the European market for Multibus II applications. Siemens estimates that market is increasing an average of 25 percent per year and will reach 460 DM ($184 million) by 1992. Siemens now sells Multibus I boards as well as VMEbus boards to the European market. —*S.F.S.*

15-ns PLA line complements high-speed logic family

Programmable logic arrays from Fairchild Semiconductor (Cupertino, CA) boast clock speeds up to 50 MHz and propagation delays as low as 15 ns. The devices complement the Fairchild Advanced Schottky TTL (Fast) logic family. Only the beginning, the PLA series is expected to extend Fairchild's family

(continued on page 10)

(continued from page 9)

of programmable logic to include ECL. All devices in the PLA line have a power-up reset capability. This feature holds down current consumption by keeping outputs in tri-state until dc power conditions are met. To improve programming yield, the devices blow fuses by shorting an emitter-base junction of a vertical npn transistor. —*T.R.W.*

PC card boasts speaker-independent voice recognition

In what may be the beginning of larger, speaker-independent recognition systems, a voice board for the IBM PC recognizes digits and the words "yes" and "no." The card by Votan (Fremont, CA) also includes a speaker-dependent mode. In this mode, the board recognizes a wide user-selected vocabulary. According to James Rogano, Votan president, recognizing words with one syllable is harder than recognizing words with multisyllables because there is less information on which to base a discrimination. The Votan card discriminates background noise, gender and accent without artificial intelligence. —*T.R.W.*

Single board offers SNA link from Multibus to IBM mainframe

Residing on a single board, a new Systems network architecture/3270 product by Systems Strategies (New York, NY) lets a Multibus host exchange data with an IBM mainframe. All major emulations of IBM functions, including synchronous data link control, cluster control and device emulation, have been ported to the DCP-8804 Multibus data communications processor by Systech (San Diego, CA). This architecture-independent approach frees the Multibus host from almost all communications software by placing it on a separate communications processor board. The company also offers SNA/LU6.2, which is a full implementation of IBM's Logical Unit 6.2 enhancement to SNA. This allows peer-to-peer connectivity and program-to-program communications over an SNA network. An implementation of SNA/LU6.2 on a VMEbus controller by Motorola is expected next month. —*N.M.*

Timing verifier attacks reconvergent fanout problem

Most timing verifiers generate false errors when reconvergent fanout is present because the program doesn't know where input signals came from. A new version of the Daisy Timing Verifier from Daisy Systems (Mountain View, CA), which is now undergoing beta site testing, claims to solve the reconvergent fanout problem by keeping track of the history of transitions between nodes. If signals branch out and then reconverge on a gate, the program can go back in time to determine whether the signals came from a common source. But nothing comes for free, and the new Daisy Timing Verifier runs from 20 percent to five times more slowly than the previous version, depending on how much reconvergent fanout is in the circuit. —*R.G*

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CIRCLE 6

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Awning over bridge, R.M.S. Titanic. Courtesy of Woods Hole Oceanographic Inst.

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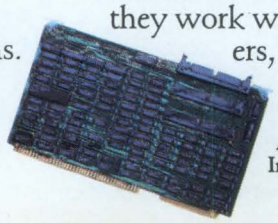
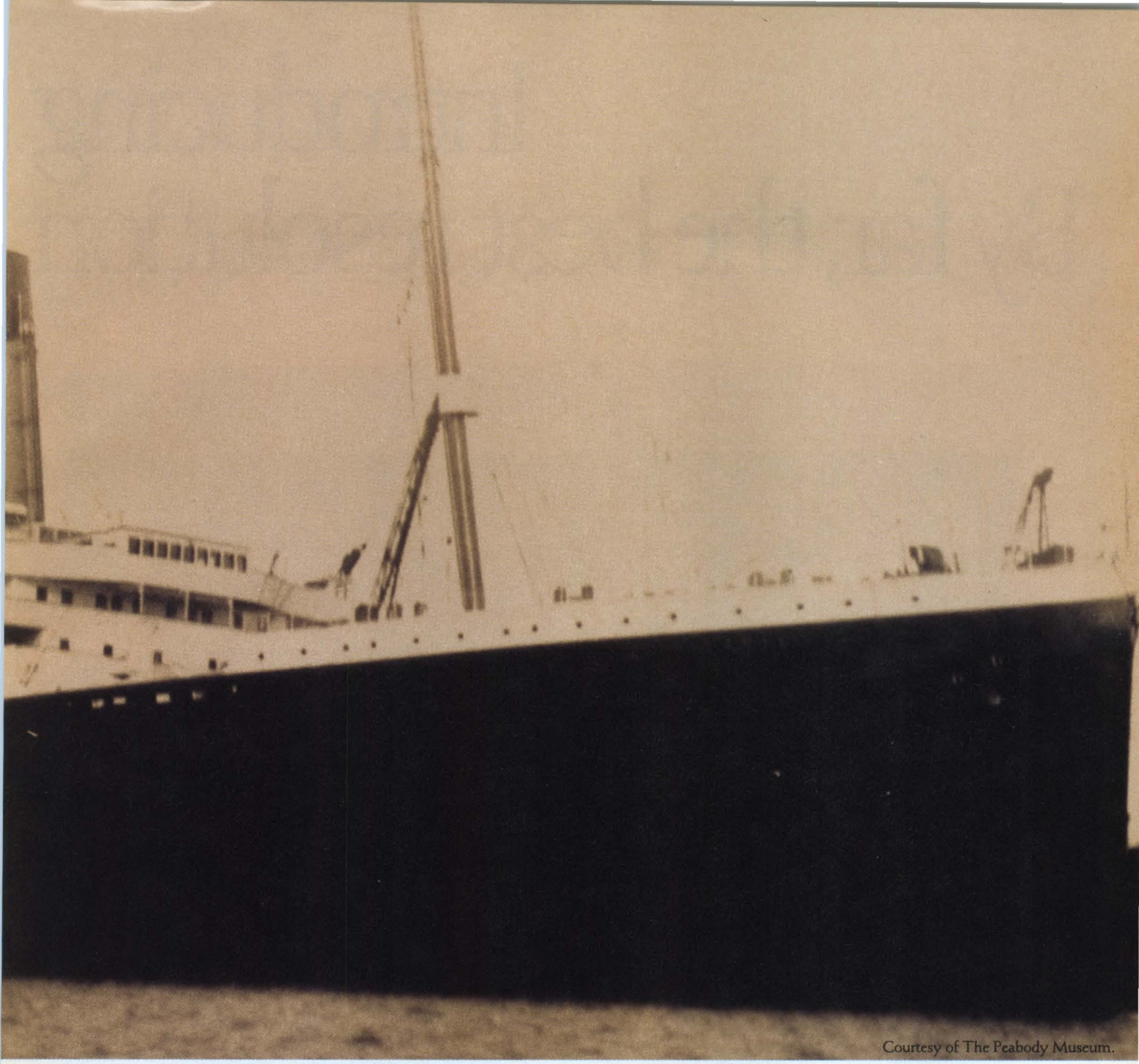


ALU-512 Image Processor



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CIRCLE 7

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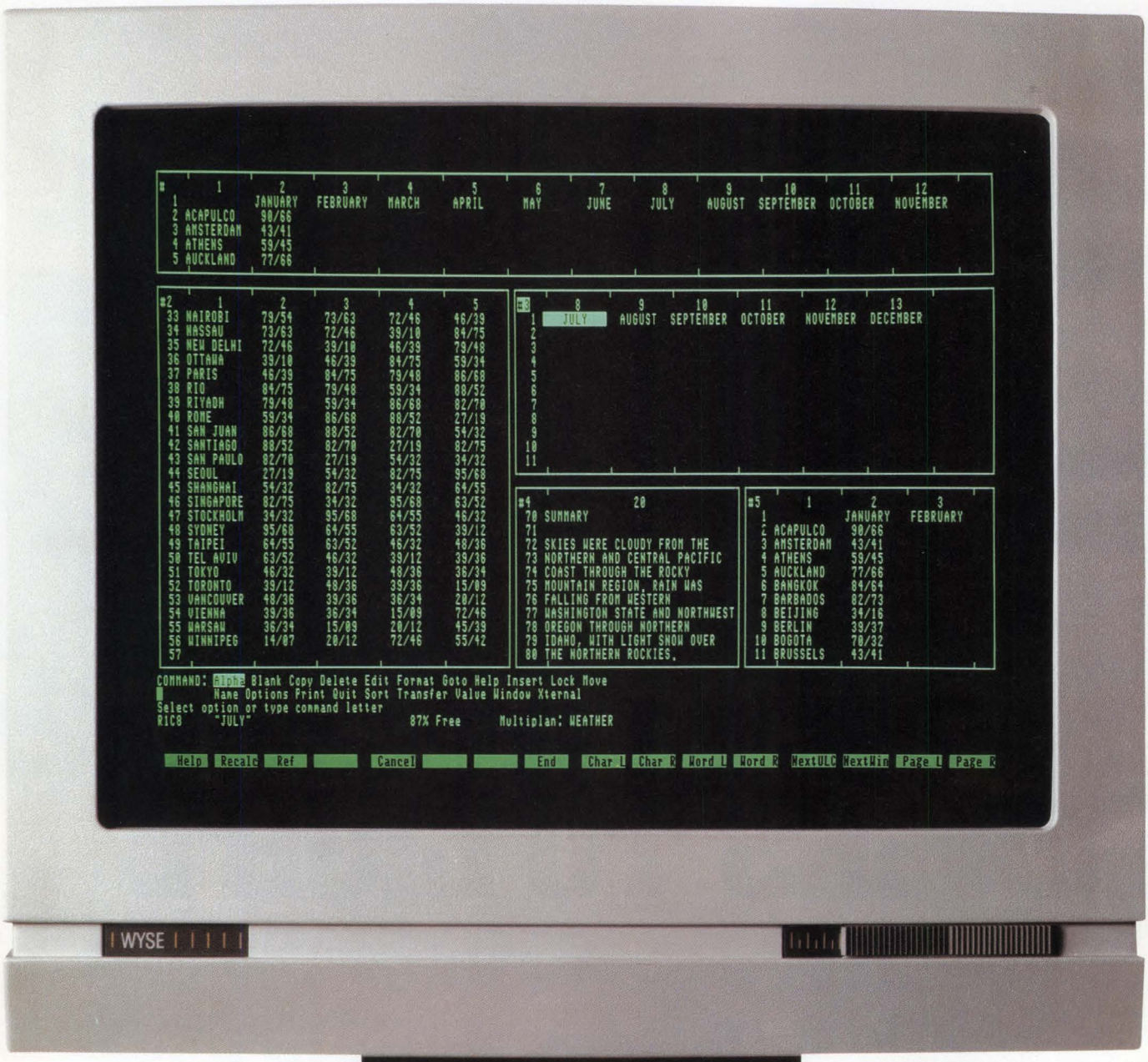

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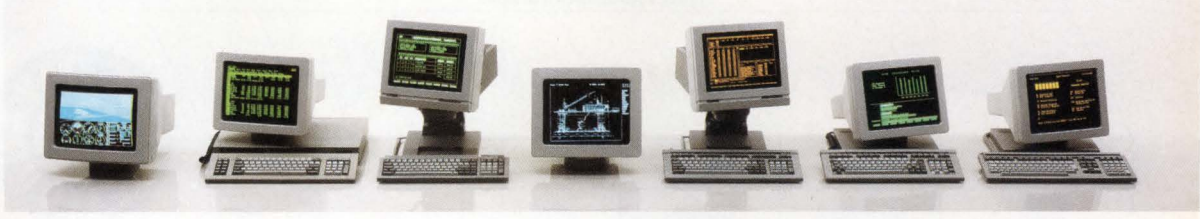

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CIRCLE 8

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CIRCLE 9

Swallowing a bitter pill

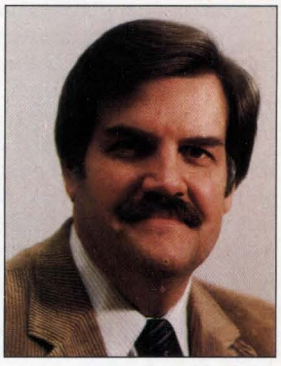
With the Libyan crisis dominating the front page of every newspaper and network news program in the U.S., the recent visit by Prime Minister Nakasone of Japan for another round of high-level trade talks with the Reagan Administration was pushed into the background. As with other visits and other talks, this one was to focus on the need for the Japanese to open their markets to U.S. products and move their economy closer to one that's consumption-oriented rather than production- and export-oriented. Unfortunately, this focus for U.S./Japanese trade discussions pushes more fundamental problems—that are mostly ours and ours alone—into the background.

For a long time now, U.S. manufacturers of both low-tech and high-tech products have complained about the difficulties associated with penetrating Japanese markets. There's no question that a number of barriers, both formal and informal, have blocked the movement of products from the U.S. to Japan during the past 25 years. In the very early days of Japan's economic recovery, the barriers were substantive ones imposed by the government, including direct tariffs and tight restrictions on foreign investment. In recent years, the barriers have become less official and more subtle, and are often attributed to differences in language (difficult to master), culture (a predisposition to long, drawn-out formalities and red tape), history (foreigners are barbarians) and a keen sense of national purpose (buy Japanese to maintain growth and prosperity).

But debates on the validity and significance of these barriers to U.S. success in Japan obscure a far more important point; major segments of U.S. manufacturing didn't lose their competitive battles in Japanese markets, they lost them in domestic markets and in world markets. Beyond that, it's hard to see how access to Japanese markets at this point in time will help those industries that have suffered major losses regain market share or prevent further loss. If you can't win on your own home court, do you really stand a chance to win on somebody else's?

That the game's been lost in many manufacturing segments, and that the point spread's widening in many others, is all too clear. Losing is a bitter pill to swallow for any nation, and especially for a business community that's always prided itself on its prowess for innovation, efficiency, resourcefulness, shrewdness and competitive spirit. It's a lot easier to blame our losses on somebody else. We can cite the mystique of Far Eastern management techniques or some cultural predisposition to hard work and group harmony. We can also look for government, industrial and banking conspiracies. Or perhaps we could swallow the pill.

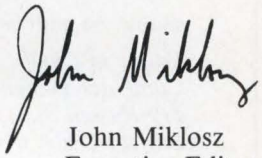
Admitting we're losing is unpleasant, especially when it's on four counts. The first, and most important one, is that we simply haven't competed as aggressively as the Japanese in both domestic and world markets. The Japanese dominance of consumer electronics, for example, could have been checked when we still had the advantages of brand recognition, in-place distribution channels and economies of scale. And despite protection, the steel industry failed to apply the differentials between Japanese and U.S. steel prices to the modernization of their plants.



Second, we've failed to develop relationships among government, industry, the banking and investment community, and labor that would support a more aggressive competitive position and a dynamic, rapidly changing industrial system. Government policy, for example, has put U.S industry at a disadvantage with rigid antitrust laws. These laws seem to have been elevated to an end in themselves. What's needed is an interpretation of antitrust that's pragmatic and flexible enough to address the problems of international competition. As for banking and investment circles, their preoccupation with quarterly earnings, share price and debt-to-equity ratios inhibits rapid growth. And while U.S. executives may claim that their employees are their most important asset, who believes it?

Third, we completely underestimated the potential for the Japanese to become world-class competitors, and we're continuing to underestimate their abilities, especially in technological innovation. In the last analysis, no one took the Japanese moves into electronics, automobiles or cameras seriously—until it was too late. And the current view that the Japanese are great at adaptation and poor at innovation is the height of arrogance and folly. The creative prowess of a society is directly related to its educational level and the amount spent on research, and the Japanese are passing us in both areas.

Fourth, we joyfully sold them the technology they needed to get under way in the first place. Underestimating the Japanese led to nearly run-away licensing of technology in the 1960s and some welcome profits for many U.S. firms. The profits may have been welcome then, but we're paying for them now.



John Miklosz
Executive Editor

LETTERS TO THE EDITOR

Getting the facts straight

The February 1 issue of *Computer Design* featured the Special Report "PLDs Slow Advance of Gate Arrays in Low-End Designs" (p 43). Taken in perspective, this article was an ambitious undertaking for your magazine. You are to be commended for attempting to present the scope of this rapidly evolving segment of the electronics industry to your readers.

As part of that Special Report, I submitted a panel on programmable logic/gate array evolution and relative utilization trade-offs (p 49). In several instances, I believe the readers were misinformed as a result of the editing process. For example:

- The panel said that "second-generation PLDs such as Altera's CMOS EP300...provided features such as programmable-output I/O [and] 2000-gate densities." The EP300 actually has both programmable input and output, and it has approximately 300 gate equivalents.
- The panel said that PLDs cost "typically less than a penny a piece in high volume." The correct statement is a penny per gate. This makes quite a difference for a 2000-gate equivalent device such as Altera's recently introduced EP1800.

Stan Kopec
Manager, Product Planning
Altera
Santa Clara, CA

Opting for clarification

I knew that the March 1 issue of *Computer Design* would contain an article featuring high-speed graphics controller boards. Not only was I interested in reading about the competition, I was also eager to read about my company's product, the Omni 2000 GDS (graphics display subsystem). Marketing a product involves hard work, dedication and, sometimes, sleepless nights. When you know you're listed in a key publication, you feel another step closer and that's exciting. I was disappointed to see the misspelling of my company, and I would like to clarify this for the benefit of those interested.

The correct name is Omnicomp Graphics (not Opticomp as published on p 47).

Bernadette Platis
Marketing Communications
Representative
Omnicomp Graphics
Houston, TX

Criticism from an IEEE life fellow

I am a little surprised that Jerry Suran (see letter from Bruno O. Weinschel, "Letters to the Editor" *Computer Design,* Mar 15, p 18) set up such a controversial policy as one that "safeguarded editors from the membership." This has led to censorship of ideas that have badly needed airing. I'm not talking of political ideas, but new technology. This philosophy has permeated all of the management hierarchy of the Societies as well as the parent organization.

Needless to say, I am further surprised that no one in the top management of IEEE is able to recognize the consequences of what has been done. If others having a modicum of creative instincts have been treated the way I have (and apparently they have), we can understand why the Japanese and others are catching up and overtaking us.

Those of you who for one reason or another haven't been able to get into the various "clubs" have received rejection notices on fundamental electronics with the usual "So many good papers" and so on. I have published eight books, at least seven of which contained important technical information that I haven't been able to get into IEEE journals in any form, except in letters long after the information should have been made available.

As long as we had AIEE and IRE, we had a little competition, and new technology usually could get out to the profession. Now all that gets out is what interests the particular publication hierarchy. And they have no qualms about censoring the existence of objections to this kind of censorship. The censorship imposed by IEEE editors could be more severe than that encountered at the hands of the Department of Defense. At least, there would appear to be a sounder reason for the latter than there is for some of that practiced by IEEE societies.

Keats A. Pullen, Jr
Life Fellow IEEE
Kingsville, MD

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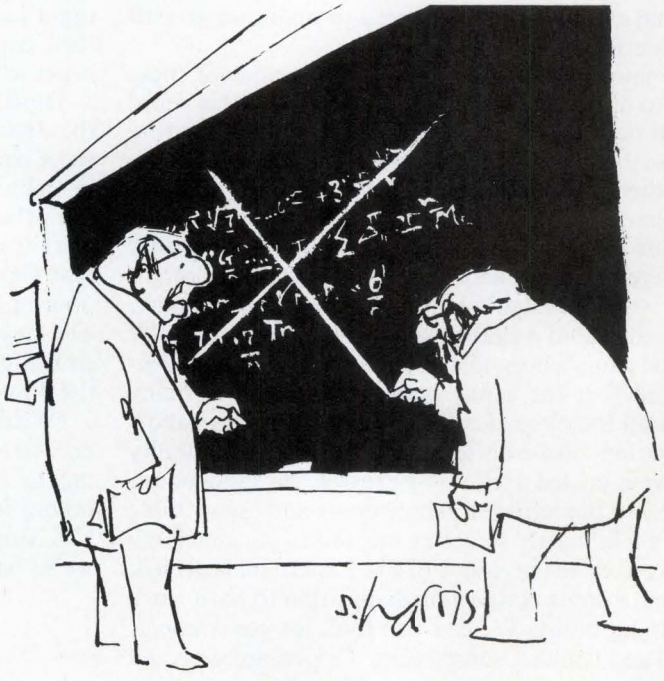

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CIRCLE 12

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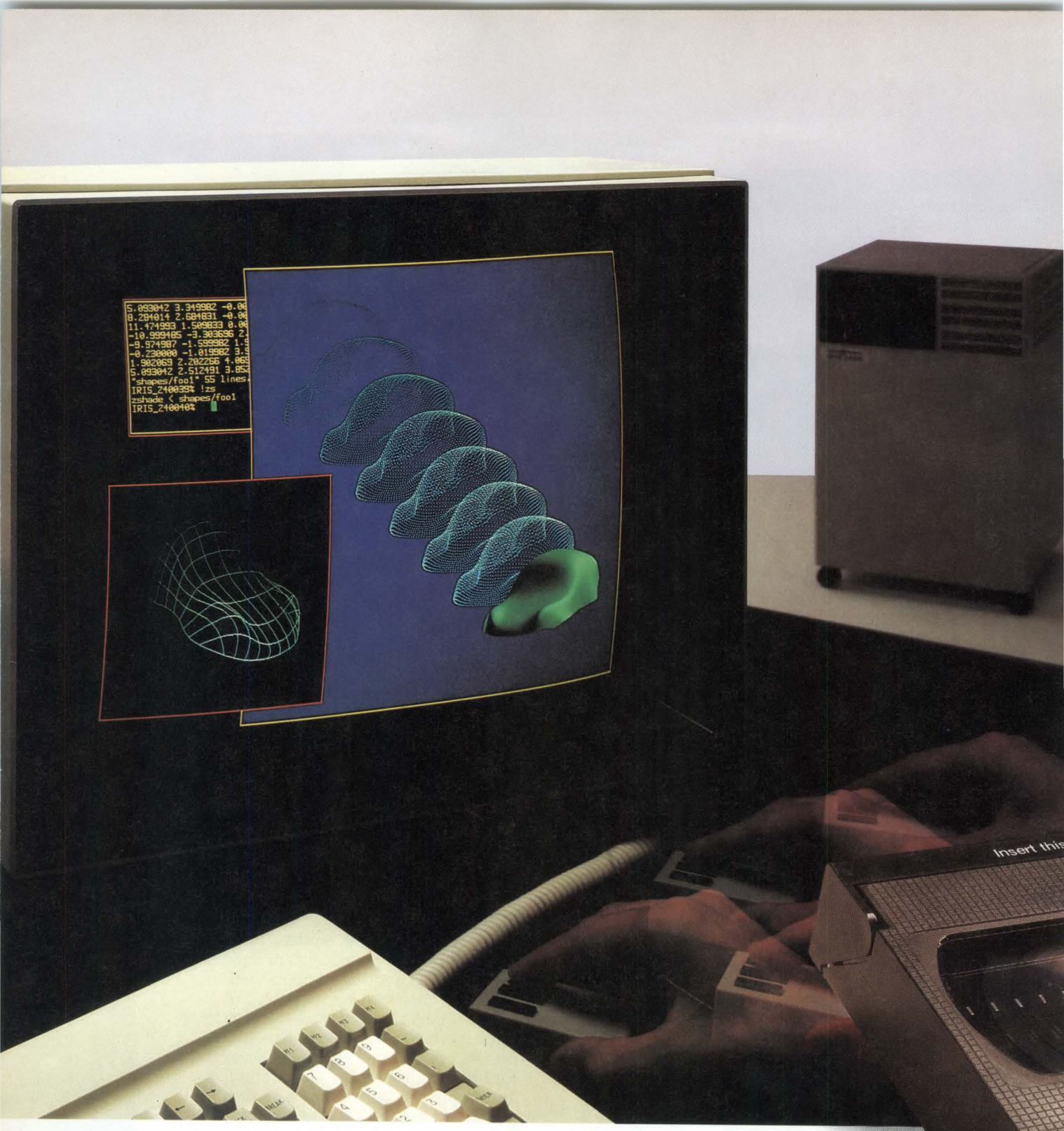

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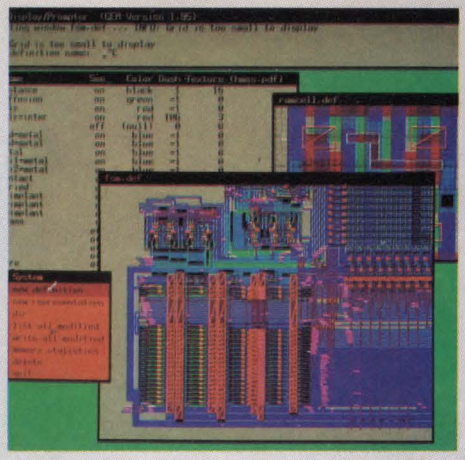

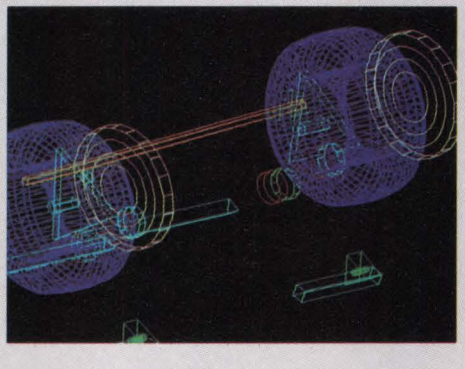

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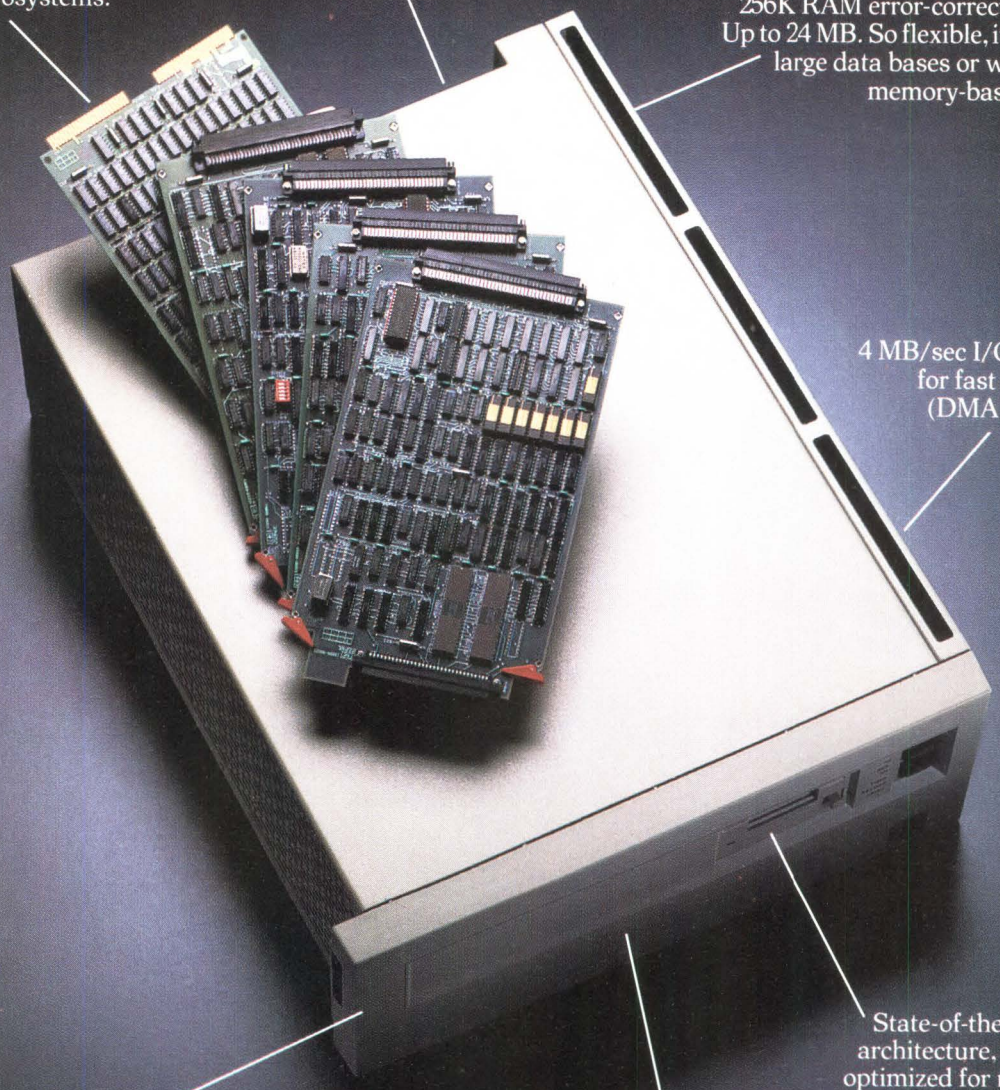

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CIRCLE 14

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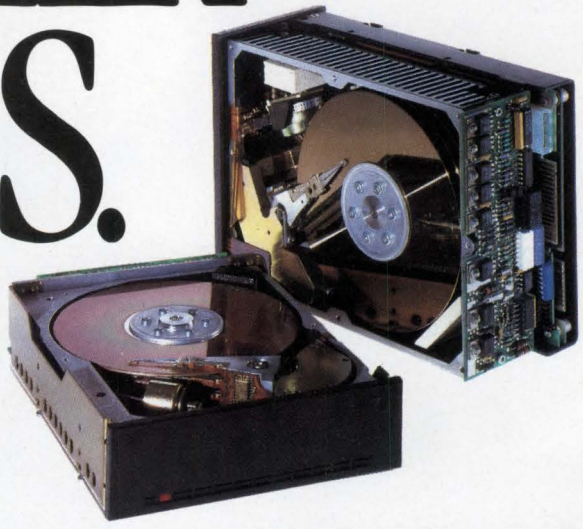

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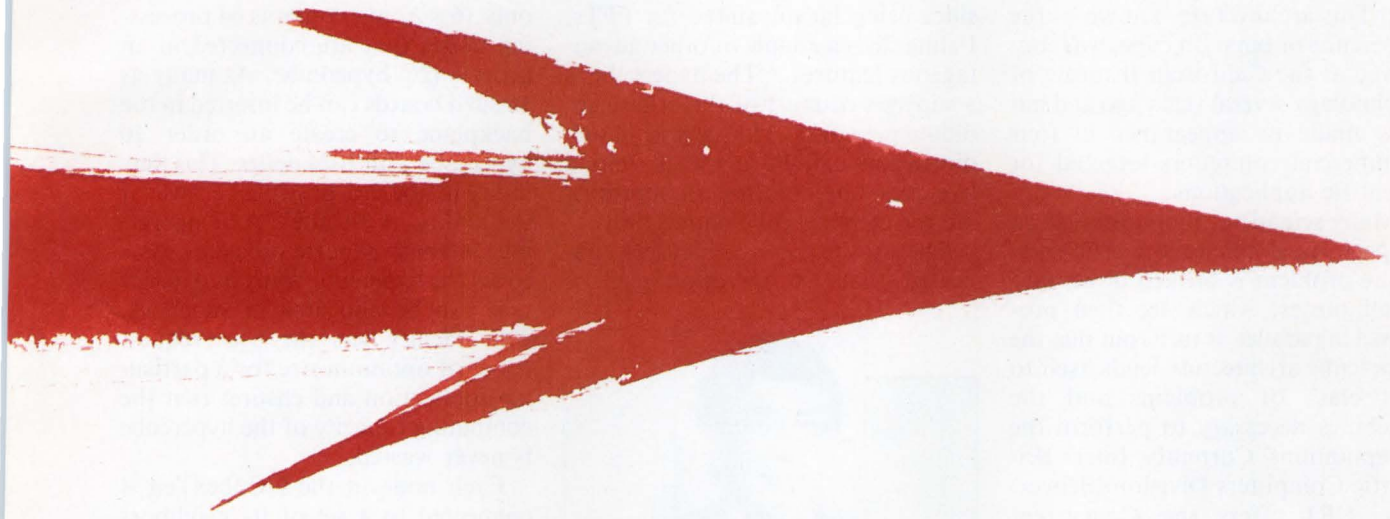

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CIRCLE 15

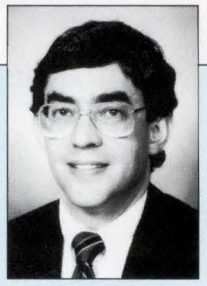
Hypercube architecture leads the way for commercial supercomputers in scientific applications

With parallel processors becoming a commercial reality, one architecture seems to be emerging as a favorite for achieving efficient parallel computing. This architecture, known as the hypercube or binary-n cube, was conceived at the California Institute of Technology several years ago and has now made its appearance in four commercial computers targeted for scientific applications.

Many scientific computations can be performed much more efficiently if the problem is broken down into small pieces, which are then processed in parallel. It turns out that the hypercube architecture lends itself to this class of problems and the machines necessary to perform the computations. Currently, Intel's Scientific Computers Division (Beaverton, OR) offers the Concurrent computer, with a vectorized hypercube architecture, which yields a maximum raw performance of 424 Mflops. NCube (Beaverton, OR) has stretched its NCube/Ten to a maximum performance of 500 Mflops. And the latest offering from the Oregon woodlands comes from Floating Point Systems (Portland, OR) in the form of the T series. When fully configured, a T series computer could clip along at an unprecedented 262 Gflops. Finally, this month, Thinking Machines (Cambridge, MA) is unveiling its Connection Machine, a 64,000-node hypercube that's expected to yield a performance of 2 billion 32-bit integer additions per second.

All four vendors exhalt the hypercube architecture for its performance and its suitability for solving highly parallel scientific problems. Says John Palmer, chairman and one of the founders of NCube, "The hypercube is the perfect network for one of the most important of all computational algorithms, the Fast Fourier transform (FFT), which is used in all areas of scientific computation. We chose the hypercube because it has a set of properties that can't be matched by any other network." Besides being ideally suited for FFTs, Palmer lists a couple of other advantageous features. "The hypercube is a superset of most of the other candidate networks. Thus a grid of any dimension can be mapped onto a hypercube by ignoring an appropriate set of hypercube connections."

The hypercube is so densely connected that its operation can be approximated by considering every node to be connected to every other node—an important approximation for parallel computations because the pattern of communication isn't predictable. "The hypercube is the most densely connected network that's also scalable to thousands of processors," says Palmer. To double the number of processors in a system, it's only necessary to add one communications channel to each node.



"Concurrent processing yields high performance by distributing a large problem among many processing nodes, while vector processing increases each node's arithmetic capability."
—Paul Wiley
Intel

The NCube/Ten has been built around a set of processor boards and a backplane. Each board, measuring only 16 × 22 in., contains 64 processing nodes that are connected in an order 6 (2^6) hypercube. As many as 16 such boards can be inserted in the backplane to create an order 10 hypercube with 1024 nodes. This flexibility in nodes is possible because of the ability of NCube's Axis operating system to allocate subcubes. Axis treats the hypercube array as a device that can be allocated in subcubes. This facility lets the user request cubes of optimum size for a particular application and ensures that the computing capacity of the hypercube is never wasted.

Each node in the NCube/Ten is connected to a set of its neighbors through DMA communications channels that are controlled by the processor. The NCube/Ten has eight I/O channels, each of which can move data at 90 Mbytes/s in each direction. The I/O channels are implemented in a powerful configuration of DMA channels. Each node has 22 DMA channels, with 20 of these paired into 10 bidirectional communications links for connecting neighbors in the hypercube and two used for system I/O. A system I/O channel consists of one pair of communications links from each of 128 nodes bundled together and brought through the backplane to one of the I/O slots. With all backplane slots occupied, each of the 1024 nodes has a direct connection to an I/O board through one of the system I/O channels.

Currently, NCube offers four I/O options: a host/user interface board that supports all standard peripherals via three Intel iSBX interface connectors, a graphics board, an intersystem board and an open system board. The intersystem board is used for communicating between two NCube/Ten systems, and the open system board is used for interfacing to

Nicolas Mokhoff
Senior Editor

special-purpose devices or proprietary systems.

"The key to both high performance and high reliability in the NCube/Ten," says Palmer, "is the individual processing nodes. Each node is an independent 32-bit processor with its own local memory and communications links to other nodes in the system." As opposed to hundreds of chips being used to implement the nodes in other parallel processors, NCube's node consists of one custom VLSI chip and six memory chips surrounding it. All of the node's logic is integrated into the 160,000-transistor custom chip. Because of this tight integration, NCube can place four nodes on an IBM AT card, at $10,000 each, and four of these can be loaded into the AT. In effect, a 16-node hypercube boosts the floating-point processing performance of a PC AT with an 80287 coprocessor by about 20 times.

While Intel's Scientific Computers Division also uses the hypercube architecture, its implementation is based on off-the-shelf parts mounted on a board that encompasses the node processor. Based on the 80286, associated memory, communications control and a complementary vector processor board, the iPSC-VX system can be expanded in groups of 16, 32 or 64 nodes. The processing nodes in a system are interconnected using a hypercube topology with the connected nodes supported with point-to-point message delivery service. The 16, 32 or 64 multiple nodes may be housed in one, two or four computational units, respectively, with a Cube Manager, which includes a separate Intel System 310 supermicrocomputer, providing a gateway to the system and serving as a software-development station.

Paul Wiley, market segment manager for the iPSC family, emphasizes that the Intel iPSC-VX vector concurrent supercomputers combine the low-level parallelism of vector processing with the high-level parallelism of concurrent processing. "Concurrent processing yields high performance by dividing a large problem into smaller problems, and distributing them among many processing nodes," Wiley points out, "while vector processing increases each node's arithmetic capability by allowing data to be processed in a rapid assembly line fashion."

The concepts of vector and concurrent processing are separate but complementary forms of parallel processing. According to Wiley, the performance improvements from vector and concurrent processing are multiplicative, so that solutions to large-scale scientific computing problems which lend themselves to both forms of parallelism are dramatically speeded-up by the capabilities of a vector concurrent computer.

The iPSC-VX system contains an

What is a hypercube?

A hypercube is a network of small computers, or nodes, that send messages through bidirectional, asynchronous communications channels. The nodes are connected in a binary-n, or 2^n, cube configuration. In a binary-6 cube system, for example, each node is connected to six other nodes to form a communications network that follows the plan of a six-dimensional hypercube. A hypercube can be defined inductively as well. A hypercube of order 0 is a single node. A hypercube of order n + 1 is constructed by taking a hypercube of order n, duplicating it and connecting the duplicated nodes together.

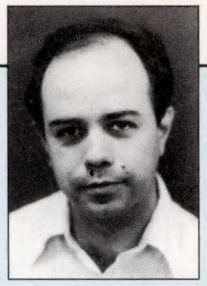
A significant difference between the hypercube and most other parallel processors is that this multiple-instruction, multiple-data machine uses message passing instead of shared variables for communications between concurrent processes. As professor Charles Seitz of the Caltech Computer Science Department points out, "The hardware structure of a message-passing machine like a hypercube differs from a shared-storage multiprocessor in that it employs no switching network between processors and storage. The advantage of this architecture is that one can separate the engineering concerns into processor-storage communication and interprocess communication." As a result, the so-called von Neumann bottleneck—the critical path in communications between an instruction processor and its random-access storage—can be engineered to exhibit a much smaller latency when the processor and storage are physically localized.

Since the hypercube can be defined inductively, all hypercubes are logically equivalent. According to NCube's chairman, John Palmer, this property yields two advantages. "One is that the programs can be written so that the dimension of the hypercube within which they will operate is a run-time parameter. Second, the full hypercube can be treated as a resource that can be allocated in subcubes." Because of this, programs can be written so that only their performance changes as they are run on different size hypercubes. This is extremely important, says Palmer, because every program increases in performance only until some maximum number of processors is reached. Beyond that, more processors represent only wasted computing power.

Subcube allocation ensures that a program doesn't waste resources. The user simply requests subcubes whose orders are below the point on the efficiency curve that represents the maximum number of processors suited to the particular computational problem and leaves the rest of the processors for other users. The granularity of the problem is always kept near the optimum point with large cubes used on large problems and small cubes used on small problems.

ensemble of node processors interconnected by a hypercube network. Each node processor is supported by a high-performance vector coprocessor board that occupies the adjacent card slot in the system. A private iLBX bus connects these two boards in a tightly coupled, shared-memory interface that maximizes system efficiency, while imposing no additional burden on the programmer. According to Wiley, each vector coprocessor boosts the floating-point performance of its companion node processor by up to 100 times for 64-bit vector operations and by as much as 10 times for 64-bit scalar operations.

The Connection Machine's unique contribution to parallel processing is that it uses the hypercube architecture for artificial intelligence applications. The system is front-ended either by a VAX or a Symbolics processor which provide the operating system environment in either VMS or Lisp. The 64,000-node system is implemented in gate array technology and is said to operate at a performance level that exceeds 1000 times the logical inference capabilities of current Lisp workstations. Applications for the Connection Machine are expected to be in VLSI circuit design, fluid dynamic analysis, real image analysis and free text data base search.

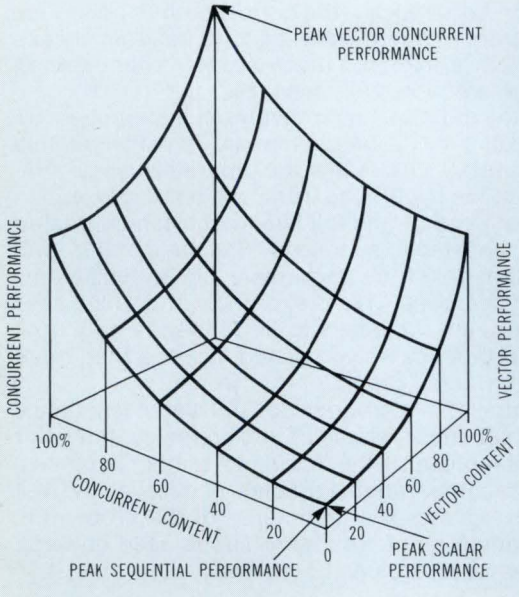


"The hypercube is the most densely connected network that's also scalable to thousands of processors."
—John Palmer
NCube

Floating Point Systems is using a unique VLSI processor and its accompanying software language. FPS has combined the hypercube architecture with the Inmos transputer and Occam software language to come up with an extremely modular computer that can accommodate from eight to 16,384 nodes. "We went with the transputer and Occam because of its inherent parallel-processing features," says John Gustafson, senior staff scientist. "Occam provides all of the facilities for reprogramming any set of communicating processors in a simple and staightforward manner."

Each node in the T series is a complete scientific computer, roughly equivalent in computing power to an FPS-364 front-ended by a superminicomputer. The peak arithmetic speed of a single node is 16 Mflops, 128 Mflops for an eight-node T/10 system and as much as 1 Gflops for a 64-node T/100 system. The largest model that could be configured, the T/40000, could have 16 Gbytes of primary memory, up to 4 Tbytes of disk storage and a peak arithmetic speed of 262 Gflops. But Lloyd Turner, FPS' president and CEO, emphasizes that power, cooling and footprint for the T/40000 are within the practical range of a small office building, adding, "If the customer has an application for a T/40000, we'll provide the building."

While Intel's iPSC-VX and NCube's NCube/Ten will run applications written in most of the common languages, such as Fortran and C, the programs for FPS' T series machines must be written in Occam. While very enthusiastic about the T series machines, Kenneth Wilson, director of Cornell University's Center for Theory and Simulation in Science and Engineering, is realistic about the chore of porting current applications programs to Occam. "The idea of using parallel processing to solve the problems that cannot be solved with current architectures is not to try to fit a program that has been written for von Neumann-type machines into a hypercube, but to break the problem into chunks that can then be written into a parallel-processing language such as Occam," says Wilson. "Unfortunately we are far away from having everybody think in those terms and thus we need to port currently available programs from a Unix environment into the Occam environment." Nevertheless, Wilson is elated that the processing power of a one-quarter-Tflops machine is finally at hand to tackle some of the theoretical physics and engineering problems that only a machine of this speed can solve. **CD**



How effectively a supercomputer handles the combination of vector and scalar operations is the key to its performance, and the synergistic relationship that exists between the two can result in dramatic performance improvements. The performance boosts resulting from vector and concurrent processing are multiplicative, so that solutions to large-scale scientific computing problems which demonstrate both forms of parallelism are dramatically speeded-up.

Microprocessor brings floating-point capability to 32-bit market

In the face of a seemingly saturated 32-bit microprocessor market, NEC has announced a general-purpose 32-bit microprocessor, dubbed the V70, that's aimed at stealing design-ins away from Motorola, Intel and National Semiconductor. NEC is banking its hopes on the demand-paged memory-management unit that it's packed onto the chip, along with a barrel shifter that gives the V70 a floating-point performance equal to that of many coprocessors.

Using a 1.5-micron CMOS process, NEC (Natick, MA) has squeezed 375,000 transistors onto the V70 chip. But the next-generation V71 will take advantage of the 1-micron process now used in NEC's memory chips to boost the transistor count to 700,000. Available sometime in 1987, the V71 will incorporate a 4k × 8-bit data and instruction cache. By the early 1990s, NEC claims that it will be running its 32-bit microprocessors at 10 Mips, an increase of almost 70 percent over the V70's current peak performance of 6 Mips (typically 3 to 4 Mips at 16 MHz).

A full 32-bit microprocessor (with 32 external nonmultiplexed address and data lines), the V70 has a 32/16-bit cousin, the V60 (32 address lines and 16 data lines), that's intended for low-cost applications. Internally, the V60 and V70 are identical, each containing (32) 32-bit general-purpose registers, executing 119 different types of instructions (273 total instructions), and providing an emulation mode that lets them run V20 and V30 code. The V20 and V30 are 16-bit microprocessors that provide a superset of the Intel 80186 and 80286 instruction sets, respectively.

Fast floating point

The V70 joins AT&T's WE32100 as one of only two general-purpose microprocessors that provide on-chip floating-point capability and perform both 32- and 64-bit IEEE 754 floating-point arithmetic. An on-chip 64-bit barrel shifter improves the floating-point performance by supporting fast scaling and normalization.

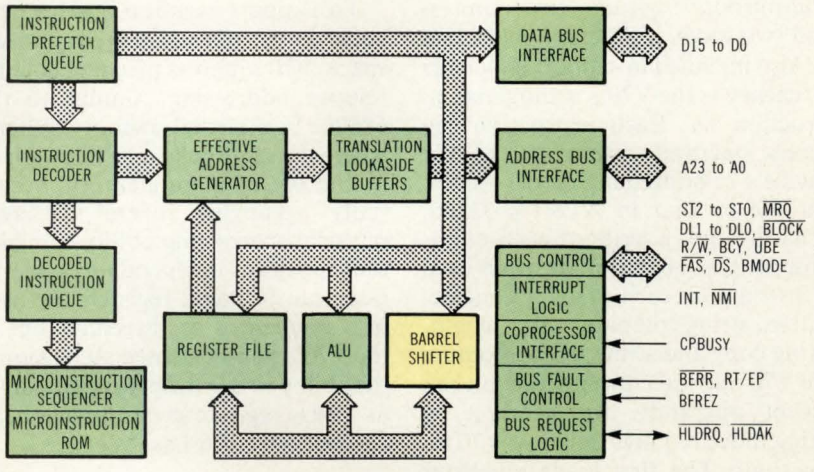
According to Rick Naro, engineering manager for NEC's V series microprocessors, the V70's microcoded floating-point performance is comparable to that of dedicated coprocessors that use a hardware multiplier and ALU. "The V70," claims Naro, "can perform 32-bit floating-point arithmetic twice as fast as an Intel 80287 coprocessor—five μs for 32-bit floating-point addition, subtraction and multiplication and 10 μs for 64-bit arithmetic."

Naro admits that the V70 can't match a coprocessor's internal precision (the 80287, for example, provides 80 bits, compared with the V70's 32 bits). But, he emphasizes, "Because the V70 performs math operations on chip, it doesn't suffer the performance degradations that result from cumbersome external coprocessor interface schemes. Where a microprocessor that uses an external coprocessor must move data off chip, the V70 contains a coprocessor interface and data paths on chip."

The 80387 coprocessor, which is still not available, will outperform the V70, but Naro says that a coprocessor could also be used with the V70 if higher math throughput is needed. NEC plans to have a V70-compatible coprocessor available sometime in 1987. The on-chip floating-point capability, however, gives users the option to save space and cost in less demanding applications.

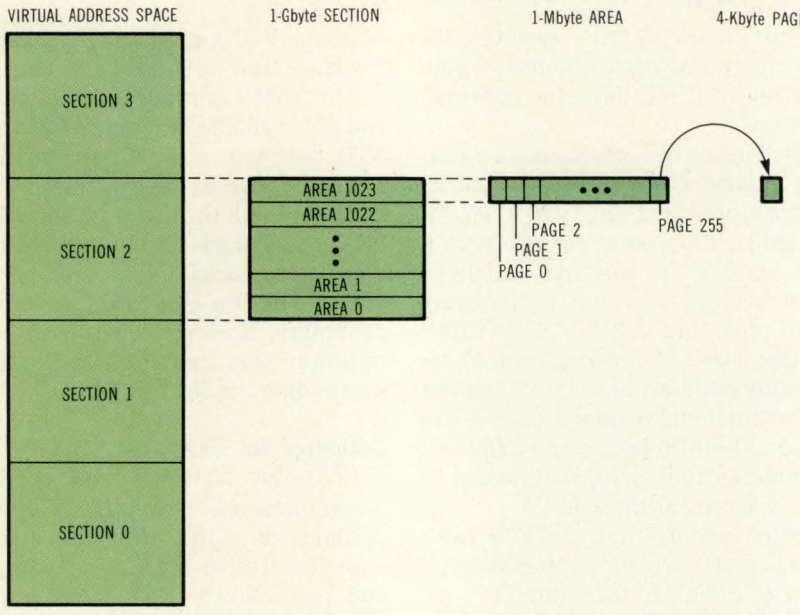
Optimized for Unix

Like the National and AT&T 32-bit microprocessors, the V70 was designed as a fast Unix processor, with features in both the hardware and instruction set to help programmers as well as optimizing compilers achieve speed. Heading this list of features is a set of (32) 32-bit general-purpose registers, matched only by those of AT&T's 32200 processor. This large register set gives compilers and assembly programmers more flexibility in optimizing their Unix code. The next closest competitor,



One of two 32-bit general-purpose microprocessors which support 32-bit and 64-bit floating-point mathematics, the V70 features a barrel shifter and microcoded instructions that deliver a floating-point throughput that's equivalent to many coprocessors. Other significant features are on-chip memory management, specialized graphics and Unix instructions, and an orthogonal instruction set.

Ken Marrin
Senior Editor



V70 uses a four-stage translation process to convert virtual and physical addresses. Bits 31 and 32 in the virtual address access one of 4 1-Gbyte sections. Bits 20 through 30 select one of 1024 areas, each of which contains 256 pages. Bits 13 through 19 select one of these pages, each of which contains 4096 bytes. Bits 0 through 12 select one of these bytes.

National's 32032, has only 16 registers. Motorola provides eight data and seven address registers in its 68020 and Intel provides four general-purpose registers, two pointers and two index registers in its 80386.

Also intended to support high Unix efficiency is the V70's orthogonal instruction set. Each instruction can access operands using any of the device's 21 addressing modes—comparable to that in AT&T's 32200. What's more, a series of instructions support fast execution of often-used C instructions such as string concatenation, string compare, string length, string copy and string move. Because the V70's string move instruction can accept operands, for example, a string move requires only two V70 instructions. The first loads a register with the string's stop character (which helps determine the string's length), and the second moves the string from the source to the destination location. The equivalent Intel 80386 instruction, by contrast, can't accept operands and requires three additional instructions to load the source and destination addresses into registers and compute the string length.

To support position-independant code in a nonsegmented address space, V70 supports program counter relative addressing, similar to the 68020. In a virtual memory system, where the same code may be swapped in and out of main memory, potentially occupying several different physical spaces, the ability to maintain position-independant code is essential. Segment registers are used in a segmented architecture, but in the V70's nonsegmented architecture, the ability to use the program counter as a base register saves the overhead of configuring a base register.

Fast graphics

In addition to providing high Unix throughput, the V70 offers several instructions that are ideal for graphics applications. Most notable is a bit-addressing instruction, which makes it possible for the processor to access any bit in its 4-Gbyte space using a single instruction. With a 35-bit address field, the first 32 bits specify one byte of 4 Gbytes and the last three bits of this address field specify a particular bit in the byte.

Other processors require at least two instructions to access a single bit. The 68020, for example, can access a single bit with one instruction if the bit is a constant and can be identified at compile time. In most applications, however, where a program manipulates a bit map, individual bits in the map are variables and require two instructions.

"Because of its bit-manipulation capabilities," says Naro, "the V70 can efficiently perform graphics operations such as Bitblt." Also improving the V70's graphics capabilities are extended logic operations, which let the V70 perform logic operations on words as large as 512 kbytes with a single instruction.

On-chip memory management

To support its 4-Gbyte demand-paged virtual memory space efficiently, the V70 uses an on-chip memory-management unit that's part of the instruction pipeline. This MMU can translate a 32-bit logical address to a physical address in 1 μs (worst case). If the location of the page that's being accessed can be found in the chip's translation look-aside buffer (an on-chip cache that maintains the location of the 16 most recently accessed pages), memory locations can be accessed without incurring wait states.

The V70 uses a four-stage translation process to sequentially access a section of the virtual address space, an area within a section, a page within an area and finally a byte within a page. Section and page tables are stored in main memory, but the translation look-aside buffer cache speeds address translation. Whenever the MMU makes a translation, the bits defining the area and page, the page frame number and protection and history information are stored in the look-aside buffer. When the V70 makes a memory ref-

(continued on page 38)

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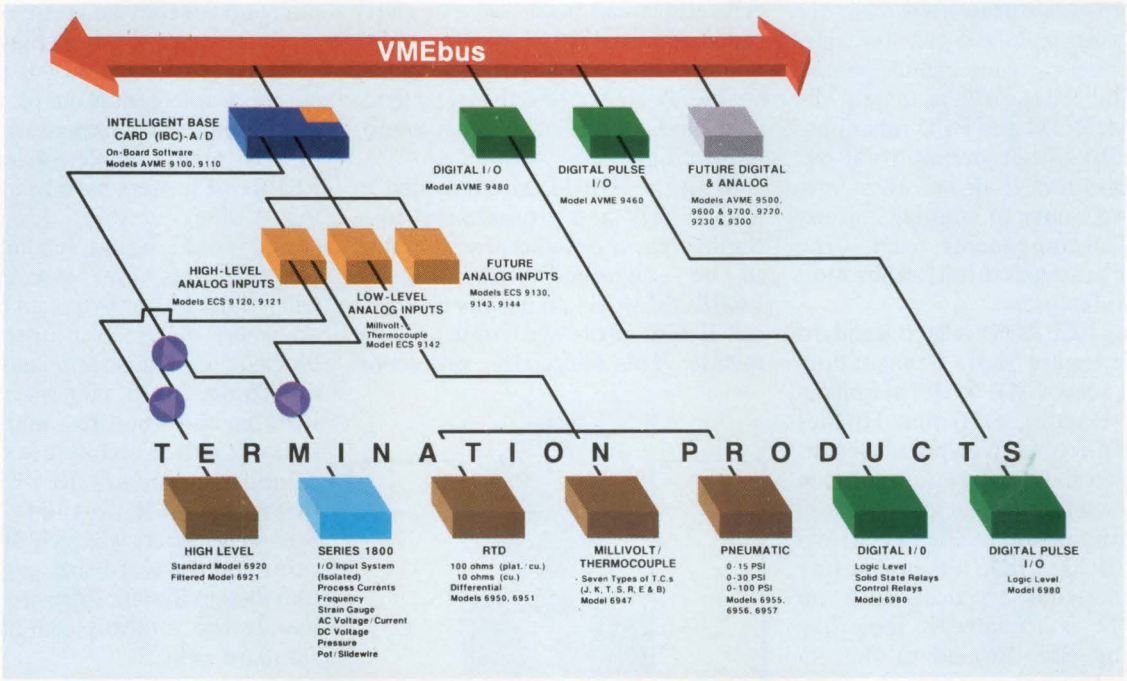

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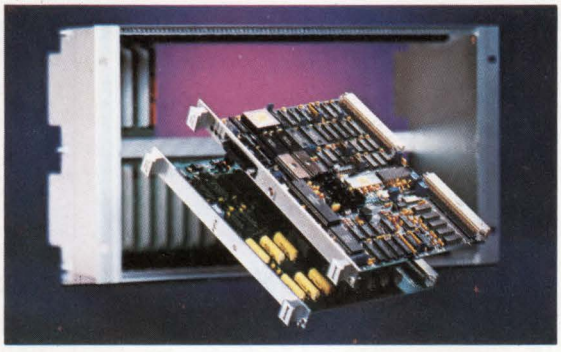

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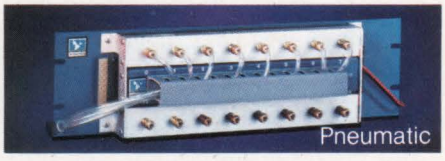
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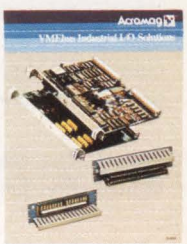


CIRCLE 16

EEPROMs move into standard cell libraries

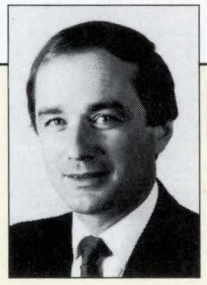
Electrically erasable PROM cells and the nonvolatile storage they offer are moving into standard cell libraries. Most libraries already include analog and digital cells as well as macrocells for RAM, ROM and PLD functions. This variety of cells permits total system integration. It also means someone doesn't have to manually adjust mechanical components, opening the door for automated test, calibration and maintenance.

Adding EEPROM cells to standard cell libraries are Sierra Semiconductor (San Jose, CA), NCR Microelectronics (Dayton, OH) and Hughes Semiconductor (Newport Beach, CA). Each has a different approach to implementing systems that use nonvolatile memory. Sierra, for example, decided that the easiest way for a designer to deal with an EEPROM is to have it look like something else. Instead of the designer learning the intricacies of the EEPROM, Sierra has configured its nonvolatile memory to look similar to more traditional logic parts, such as a D flip-flop. At the same time, Sierra has addressed the problem of testing an embedded EEPROM in a standard cell environment.

Dropping a conventional EEPROM structure into a standard cell requires dedicated testing paths and a test protocol for the cell. This places restrictions on the designer. Sierra, however, designed its EEPROM cell to eliminate these tests. Its cells model a D flip-flop, SR flip-flop and transparent latch. Testing is the same as for a flip-flop or RAM cell; designers simply write a 1 or 0.

Externally, the D flip-flop cell looks just like any conventional D flip-flop with the addition of V_{PP} and program/erase lines. The programming voltage and timing to these lines is supplied on the chip for all EEPROM cells by either a high-voltage source or high-voltage interface cell. The source cell accepts a 5-V input and supplies properly timed 18-V programming signals. The interface cell accepts and passes on a properly timed external 18-V programming voltage while supplying the timed enable. A user need only apply data, clock and a write/erase signal to program a bit.

With the EEPROM embedded in a logic shell and programmed by a timing cell, a designer doesn't have to be concerned with how an EEPROM works to use the cell. The cell is also protected from possible misuse. This simplicity, protection and freedom from specialized testing comes at the price of silicon real estate, however. Relative to the size of a conventional EEPROM cell, the Sierra cell is more than eight times as large. And the programming cells are many times larger than that. "But most designs don't require large blocks of nonvolatile memory," points out Don MacLennan, Sierra's director of custom marketing, "only a few bits or bytes to accomplish the functions of, say, a potentiometer or a DIP switch cost-effectively. We think greater reliability and less testing make up for the real estate penalty."



"Most designers don't require large blocks of nonvolatile memory. We think greater reliability and less testing more than make up for the real estate penalty [of a larger cell.]"
—Don MacLennon
Sierra Semiconductor

MacLennan contends that the cost of discrete EEPROMs has prohibited the implementation of the self-modifying, self-compensating or remotely maintainable systems that EEPROM makers have been predicting. "Many of these designs," he says, "could be implemented with very few bytes of memory, especially when those bits or bytes can be placed anywhere on the chip instead of in blocks." For those applications that do require more memory, Sierra is working on multibit implementations. It will probably use the same compiler approach for EEPROM that it uses for RAM and ROM cells. System designers will pick the dimensions and the word size. Sierra Custom Design System software will then handle the multibit cell like other standard cells.

A more conventional EEPROM

NCR takes a more conventional approach with its EEPROM supercell, offering the features and functions of a stand-alone EEPROM in a 32- to 256-bit cell. Width is variable from one to eight bits with a constant 32-word depth. The cell also includes many of the latest discrete device features: 5-V operation, three-line control, latched address and data inputs, auto-timed write cycle, false write protection, low-power sleep mode, 200-ns access time and 10-ms write time.

Designers familiar with commodity EEPROMs will feel right at home designing with NCR's supercell, particularly those acquainted with the firm's standard cell design base. So that the supercell doesn't affect the rest of the design, NCR developed a single-poly capacitor for its EEPROM, matching the EEPROM processing to the processing used for the rest of the chip. One extra masking step for the tunnel oxide is all that is needed. A result of that process allows writing of a bit without first erasing, making the EEPROM look like a RAM when it's writing.

William Twaddell
Contributing Editor

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CIRCLE 17

As with the Sierra cell, the supercell can accept an external programming voltage (15 V) and external write timing. Unlike the Sierra cell, however, NCR's EEPROM must be tested in the same way as a conventional EEPROM. Designers must, therefore, provide access to address, data and control lines, including the three lines used for cell margining. This may seem like a lot of lines, but according to NCR, many may be multiplexed with other chip functions. To make the testing easier, the cell incorporates block write capability.

Fully supported by NCR's CAD system, the EEPROM supercell is implemented in the same manner as the firm's other supercells. A symbol representing array size and cell orientation is used and all sizes are autoroutable and completely compatible with NCR's other standard cell libraries.

Another company entering this market, Hughes Semiconductor, has been combining analog, digital and EEPROM circuitry on custom chips for several years. An early pioneer in CMOS EEPROM technology, Hughes has developed what it calls "knitter" cells that use silicon-gate CMOS technology for its library of 2-micron

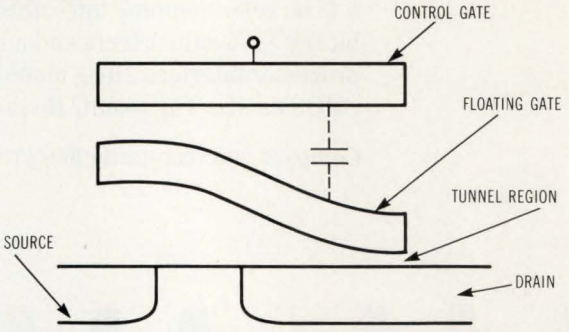
How to make an EEPROM look like a flip-flop

When Sierra Semiconductor set out to build EEPROM cells, it first looked at the problems of a conventional EEPROM memory cell," recalls Joe Nolan, chief architect of the cell and program manager for electrically erasable custom designs.

A two-transistor cell with the tunnel region in the drain of the EEPROM transistor, it has electrons that pass up and down and to and from the floating gate through the tunnel oxide. The control gate acts as a large capacitor that controls the floating gate. Programming occurs when the control gate is driven to a voltage that's very high with respect to the drain, creating an electric field across the tunnel oxide. Electrons from the drain tunnel through the thin oxide to the floating gate, charging it negatively and holding the transistor OFF when it's read. If the field is reversed and the electrons tunnel away from the floating gate, however, the charge is positive. The transistor is held ON when it's read.

Some of the standard tests applied to an EEPROM cell include cycling and margining. These tests are done at the factory to check for cells that aren't dead yet but would not make the endurance requirements. Cycling usually involves 100 to 1000 write/erase cycles after which the part should be good for 10,000 cycles. Margining is a method of checking the cell's written and erased voltage thresholds to ensure that logic levels can be reliably written and read. Over time, charge gets trapped in the tunnel oxide, preventing a full charge from tunneling to or from the floating gate. If too much charge is kept from tunneling, the transistor will not reliably turn ON or OFF during a read. Margining attempts to predict how many times the cell can be cycled before it becomes unreliable.

EEPROM cells also experience a problem called read disturb. When the cell is read, current flows through the channel. Sometimes this current produces enough energetic electrons to produce a hot electron effect, in which the electrons jump over to the floating gate, reducing the charge on the gate. Another form of read disturb stems from the field that forms across the tunnel oxide when the cell is biased for reading. Though much smaller than the field generated during programming, it's large enough to cause some leakage across the tunnel oxide, again lowering the charge on the gate. Both effects alter the retention (long-term readability) of stored data.



To avoid the difficulties of testing and the problem of read disturb, Sierra completely redesigned the EEPROM cell. The first step was to move the tunnel oxide out of the gate-drain path and give it its own terminal, separating the programming path from the read path. Next, Sierra added an identical transistor and cross-coupled the gate and tunnel terminals so that writing to one transistor erases the other. Then came a pair of sense amps, completing a full complementary cross-coupled latch which draws no power during a read. To this basic cell, the designers added a front end that makes it look like a D flip-flop and some back-end output buffering. Whenever power is applied to the cell, it looks like a D flip-flop that always comes up in the right state.

By splitting off the tunnel oxide from the drain, both read disturb problems are eliminated. In addition, by using two transistors, the thresholds for write and erase states are referenced between the two instead of to some center threshold voltage, effectively doubling the cell's margin and greatly extending cell endurance. This tends to relieve the need for margining.

But what if a bit fails during programming? Cycling would have caught it, but because cycling is undesirable, Sierra instead implemented 100 percent redundancy for every bit. If the tunnel oxide on one transistor ruptures, the transistor in parallel automatically and transparently takes over.

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CIRCLE 18

standard cells. A knitter cell is a complete, fully functional EEPROM that is knitted together with a basic EEPROM, EEPROM latch and a capacitive charge pump.

The EEPROM bit may be configured with others to form a memory array. An on-circuit dip switch can be configured with the latch cell. In addition, the charge pump cell generates high voltages (usually 16 to 17 V) on chip. Sophisticated features of the cell include autotiming and, like the Sierra and NCR versions, Hughes' EEPROM device calls for a single 5-V supply for all operating modes.

Admittedly, the latch cell and charge pump cell adds to the real estate demands of the knitter EEPROM. But according to Jerry Goetsch, Hughes' manager of applications engineering of semiconductor products, "The real estate penalty of on-chip charge pumps is offset by the cell's benefits. It's a convenience."

Hughes bases its knitter cells on some of its custom chips and is transferring these designs to standard cell form. Although the knitters are complete laid out, they're not yet extracted as stand-alone cells.

"The real estate penalty of on-chip charge pumps is offset by the cell's benefits. Its a convenience."
—Jerry Goetsch
Hughes Semiconductor

National Semiconductor (Santa Clara, CA) also plans to add EEPROM cells to its analog and digital standard cell offerings, looking at a time frame of about one year.

A CMOS EPROM alternative

There's at least one other way to get nonvolatile memory into a semicustom chip. Waferscale Integration (Fremont, CA) offers a family of three 2-micron double-metal CMOS EPROM cells in its Modular cell library. The first is a 1k × 16-bit cell that features a 45-ns maximum access time. The cell is stackable in X and Y dimensions and is compatible with the company's bit-slice processor and peripheral cells.

A second cell is nonstackable and features a more traditional 8k × 8-bit cell. This chip has an access time of 200 ns. Last in the family is a stackable 1k × 16-bit cell that has an access time of 40 ns.

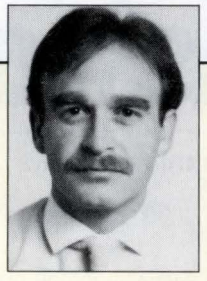
Waferscale family members program with a 13.5-V V_{PP} at a speed of 1 ms per word. Chips that include these arrays can be packaged with or without a window. The cells are self-contained and require no additional wave-shaping or timing circuitry.

Other logic blocks available in the firm's library include 32-bit CPUs, I/O logic and RAM and PLA cells. Although not offering in-system reprogrammability, an EPROM-based design is a viable alternative for many systems. Waferscale is currently investigating ideas for an EEPROM cell to add to its library. **CD**

Microprocessor brings floating...
(continued from page 32)
erence to a virtual address in any of the 16 most recently referenced pages, it can find the page location in the cache. It doesn't have to access the page and area tables in main memory.

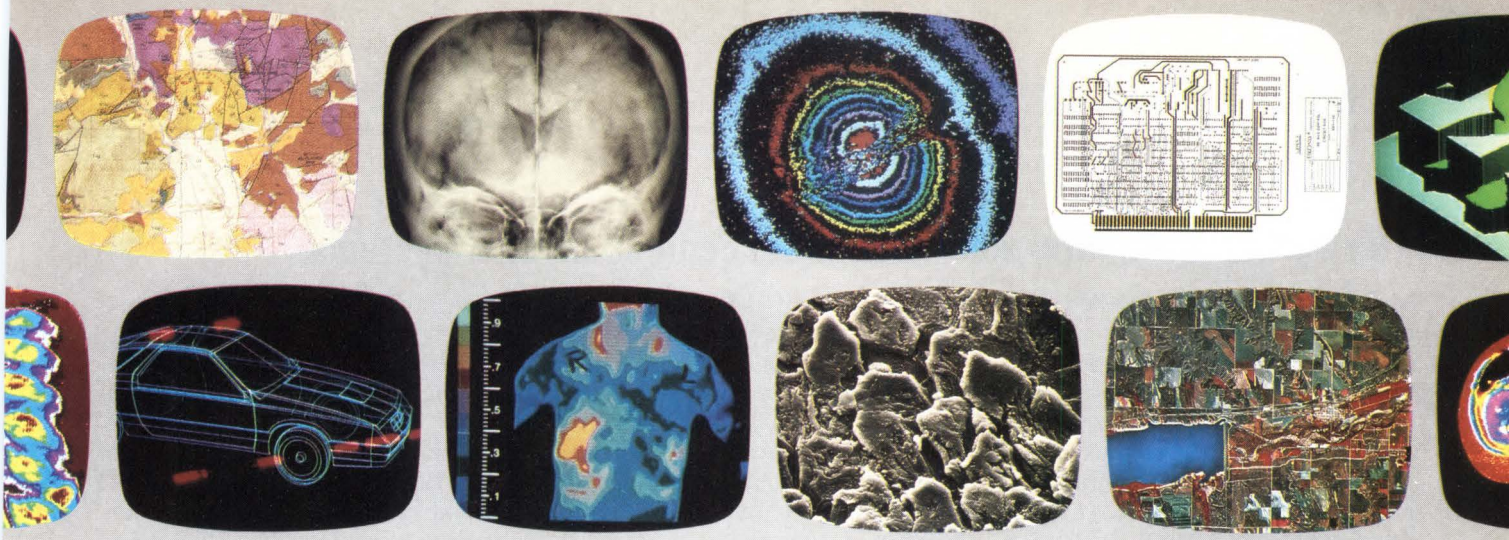
With demand paging, the V70 can run programs that require more memory than is available in main memory. As in other demand-paged virtual-memory-management strategies, when a virtual address translates to a physical address that isn't housed in main memory, the MMU generates an interrupt to a fault handler, which brings the page from disk into main memory. The fault handler then updates the look-aside buffer to reflect the most recent access.

The advantage of incorporating the memory-management function on chip is that it reduces translation time. Because the V70 doesn't have to move data between itself and an external MMU, it can reference main memory in three clock cycles, even when a virtual-to-physical-address translation is required. An off-chip MMU, by contrast, would require at least four clock cycles.



"The V70 can perform 32-bit floating-point arithmetic twice as fast as an Intel 80287 coprocessor."
—Rick Naro
NEC

A possible disadvantage of the on-chip MMU is degraded performance in a multimaster system. When a DMA controller acts as a bus master, for example, and requires a virtual memory capability, it must use the V70's MMU. If the MMU is housed on a seperate chip, then the DMA controller doesn't have to interrupt the processor. "To address this problem," says Naro, "NEC will add an MMU capability to its DMA controller. Instead of using the microprocessor's MMU, the DMA controller uses a virtual address and pointer to the task's translation tables to calculate the physical address." **CD**



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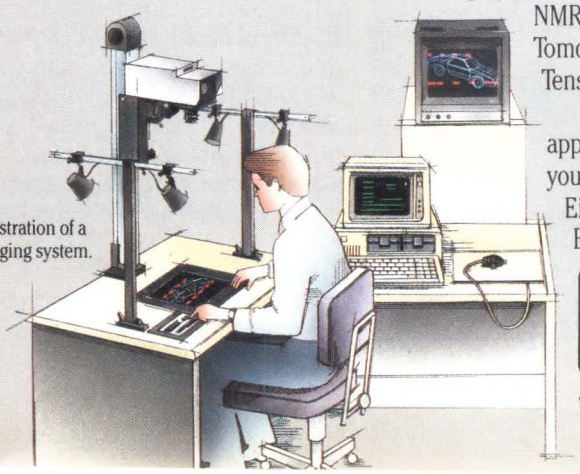

Illustration of a typical imaging system.

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CIRCLE 19

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Third-party software aids data management in CAE systems

Many users of computer-aided engineering and design face the problem of managing volumes of data from tools provided by different vendors. Translating data from one tool to another, or from the engineering to the manufacturing environment, is also a difficult challenge. To address these problems, several third-party software vendors are now providing data-management tools for multivendor engineering and manufacturing environments.

To bring file-management and project-management capabilities to the engineering environment, Sherpa (San Jose, CA) will introduce a software system called Sherpa Data Management System (DMS) this spring. This VAX/VMS-based system serves as a central repository for files and provides such features as access control and status checking. Sherpa DMS lets users define release procedures and track organized sets of files through an orderly development cycle.

Computer-Integrated Manufacturing (CIM) software from DA Systems (Campbell, CA) also provides some file-management capabilities, but focuses on data translation from one tool to another. DA Systems' neutral interchange format provides data translations for CAE systems, CAD tools, manufacturing equipment and automatic test equipment. Running on an IBM PC-based network, CIM provides a common user interface among the various CAE/CAD tools and host computers attached to the network.

Richard Goering
Senior Editor

Management problems

Sherpa DMS can be envisioned as a management layer that sits on top of the engineering data bases provided by various vendors. Sherpa DMS performs such functions as keeping track of files, making sure engineers use the correct files, checking the status of files and maintaining access privileges. "These are management problems, not engineering problems," says William Johnson, a director of Sherpa. "If you're going to solve these problems, you have to model the management organization and its policies."

Johnson observes that many CAE vendors have file-management systems, but adds, "None that I know of have project management, with release procedures and an ability to track deliverables." A deliverable can be a single file, such as a schematic diagram, or a set of files related to a particular design. Sherpa DMS provides a flexible capability for defining deliverables and allows deliverables to be nested hierarchically within other deliverables.

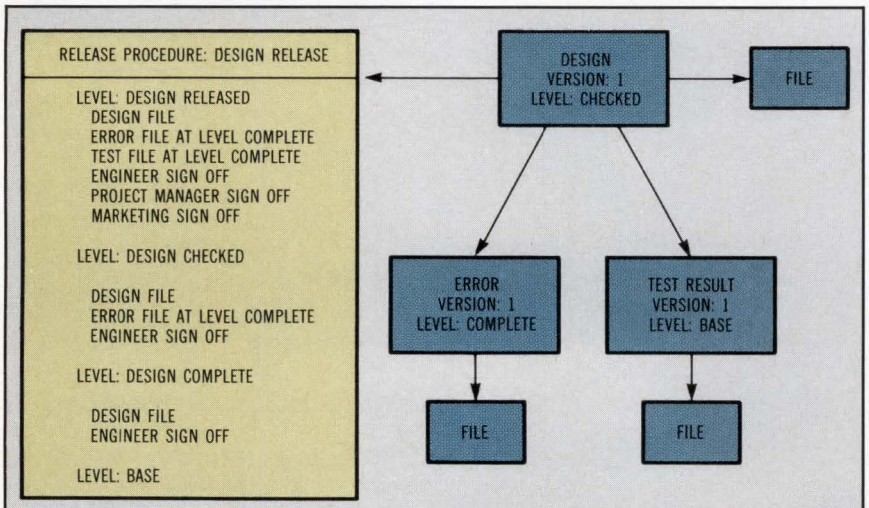
Deliverables can be advanced through the release process through a predefined set of promotion levels. Common examples of such promotion levels include the completion of conceptual design, the completion of a detailed design, release of a design for use and the retirement of a design from active use. Each promotion level carries a set of rules, or checks, that must be fulfilled for the deliverable to be promoted to the next level. One form of a check is a sign-off approval.

Sherpa DMS also controls access privileges for every deliverable and lets users define separate access privileges for each promotion level in a release procedure. As an example, an IC cell at the "detailed design complete" stage might provide update access to the design engineer for editing, but provide no access to individuals outside the project. When the cell is promoted to "released for use," engineering management could eliminate update access and provide read-only access.

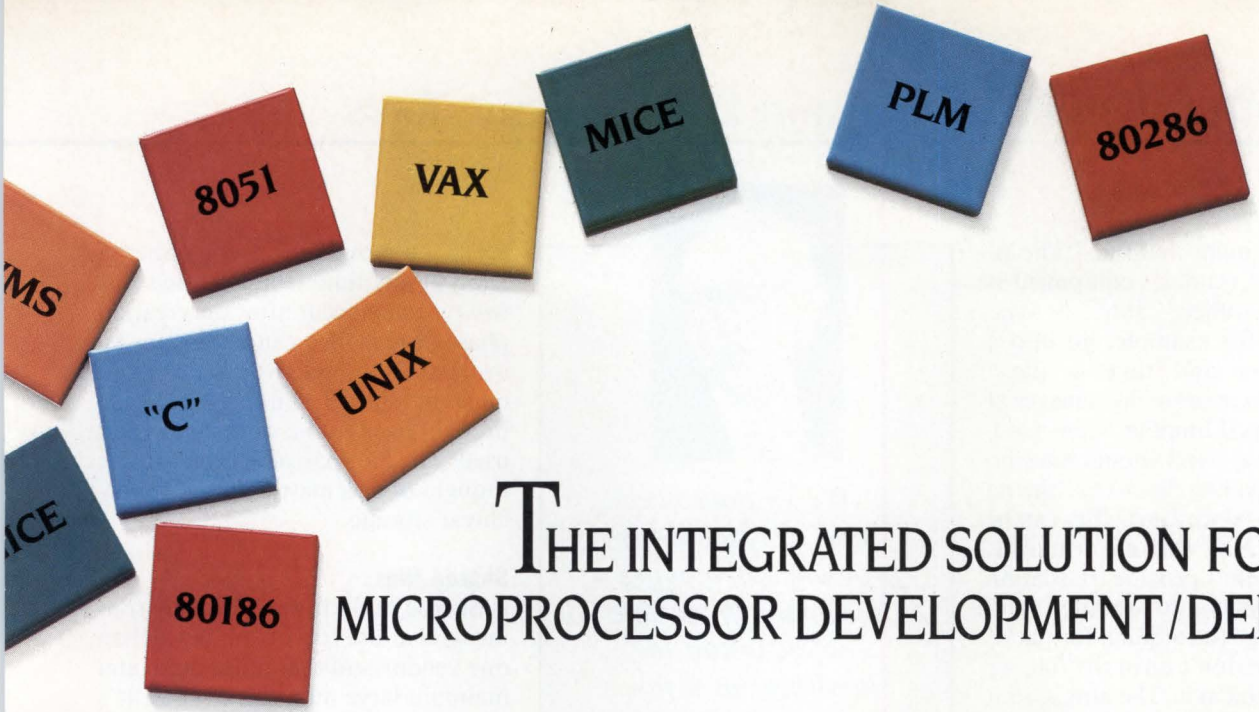
From the user's point of view, Sherpa DMS provides an object-oriented data base, with objects such as "project" and "release procedure" that are familiar in a project-management environment. On an implementation level, Sherpa DMS uses a relational data base model. "It's flexible, it lets users make changes, and it's good for ad hoc queries," Johnson says. Relational data bases are typically slow, but Sherpa DMS avoids that problem because it doesn't break up individual files.

Transporting files

While Sherpa DMS can accept a file from any CAE/CAD system, the



The Sherpa DMS system provides file management and project management for engineering data. The system allows users to advance files through a coordinated release procedure and to control access at each level of the release.



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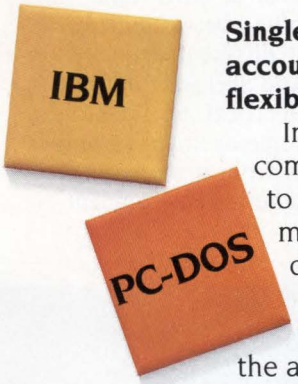

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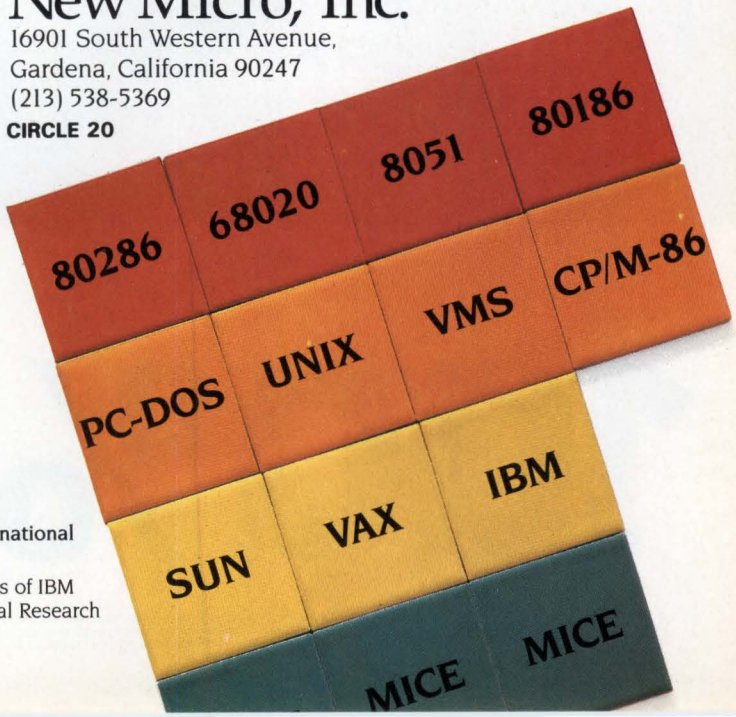

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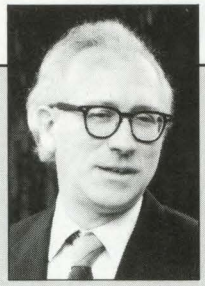
user has to provide that file. "The interface to the vendor's equipment is up to the customer," Johnson says. "We can't, for example, go into a Daisy system and take a file." Jayaram Bhat, marketing manager at Daisy Systems (Mountian View, CA), comments that users should have no problem uploading files to the Sherpa DMS system, since Daisy files can be stored in a VAX/VMS environment.

Sherpa doesn't provide translation from one system to another, and doesn't change the original format of the file. "We don't open the file, we don't even look at it. The atomic unit we track is the file itself," Johnson says. But he adds that Sherpa DMS offers a good service for people who have to store translated files, because the software can track both versions of a file simultaneously.

Because Sherpa DMS works independently from the workstation,



"We've only been able to resolve the problem [of moving a schematic from one workstation to another] in a few special cases where people have done a lot of work to create compatible libraries."
—Russ Briggs
DA Systems

users can move files over to Sherpa DMS at any time. Johnson says this will typically occur after the creation phase, when files can no longer be isolated on a single workstation and must be shared. Files can still be brought back to the workstation and used. The Sherpa system can thus be thought of as a master library for archival storage.

Shared files

Sherpa DMS is geared to environments that use tools from more than one vendor and that must share and maintain large numbers of files. It's particularly useful in environments where data is shared between different locations or different divisions, Johnson says. And Sherpa DMS isn't restricted to electrical engineering files—the same management system can handle files from a mechanical CAD or manufacturing environment.

Rather than providing a central repository for files, CIM software from DA Systems allows data translation and control within a distributed, PC-based network. By providing a neutral interchange format, DA Systems helps users avoid the multitude of one-to-one interfaces that are usually necessary as projects go through various phases of engineering, manufacturing, and testing. Only one interface needs to be written for each tool, and DA Systems will provide interface for the most common tools in each area.

DA Systems now provides interfaces for the PC Design Automation System from RDS/Automate (Palo Alto, CA); in-circuit testers from Zehntel (Walnut Creek, CA) and Genrad (Concord, MA); and automatic insertion equipment from Dyna/Pert (Beverly, MA). Russ Briggs, president of DA Systems, believes the company will have no problem providing interfaces to commonly used CAE systems. This will generally be accomplished through the export formats that many vendors publish. In addition, most vendors provide a language or a set of access routines that let users write net list interfaces.

While DA Systems can help users move from CAE to manufacturing and testing, it generally can't help users dump data from one CAE system to another. This is because most CAE vendors zealously guard their libraries from competitors. "If you tried to take a schematic from a Valid workstation to a Daisy system, that would be really touchy," Briggs says. "We've only been able to resolve that type of problem in a few special cases where people have done a lot of work to create compatible libraries."

But DA Systems could take a Valid schematic to an in-house simulator or a third-party layout system. By the time the schematic is levelized and compiled, it has all the information it needs to go on to the next process, including information extracted from libraries. This doesn't mean the user can draw a schematic and forget about the rest of the process, however. "It's important that people produce schematics that are convertible and usable by the simulator and the printed circuit board design system," Briggs says.

In addition to providing an interchange format, CIM supplies a common user interface for transferring design and engineering data among various types of systems. The software package coordinates the release of jobs, revisions and engineering changes using a menu-driven interface. Back annotation from CAD to CAE is also provided. **CD**

Comprehensive analyzers ease the pain of LAN performance testing

Just a few years ago, instruments designed to comprehensively test local area networks existed only in the imaginations of a few frustrated systems engineers. But with the number of LAN installations exploding, two companies have responded with multifunction LAN testers to provide development and maintenance support for the most popular Ethernet IEEE 802.3 standards.

The LANalyzer from Excelan (San Jose, CA) and the HP 4971S from Hewlett Packard's Telecommunications Division (Colorado Springs, CO) bring a new dimension to LAN testing. Besides monitoring, capturing and analyzing data frames in the network, these units give the systems engineer extensive ability to define and generate data frames to test other nodes on the LAN and to measure network load. Network traffic can be viewed, performance analyzed and problem areas narrowly defined. User-defined performance tests can measure bad frame rates and collect specified frames for analysis. And by measuring the distribution of the size of data frames and estimating peak usage, the overall performance of a network can be optimized.

John H. Mayer
Associate Editor

Excelan's LANalyzer is the first hardware/software package to deliver network-analysis capabilities to the IBM PC and compatibles. It succeeds the Nutcracker, an Excelan product primarily directed toward protocol development. It is PC-based, adds network management and support to the Nutcracker's development functions and accommodates test criteria independent of protocols such as TCP/IP, DECnet, XNS and ISO.

To verify protocols or debug problems on the LAN, systems developers using the LANalyzer can define test criteria for up to eight receive channels and capture specific information based on byte address, byte patterns, character strings or node addresses. It accommodates up to 200 nodes. A 700-kbyte trace buffer holds bursts of data when the user seeks to analyze a precise data packet. Available in two configurations, a LANalyzer kit with a plug-in PC controller board, software package and transceiver costs $9500. A portable version that bundles the board and software with a Compaq Portable 286 for field service applications sells for $19,500.

The HP 4971S troubleshoots and maintains LANs employing Ethernet IEEE 802.3 implementations. A softkey-guided programming language lets users define diagnostic tests.

Like Excelan's LANalyzer, Hewlett-Packard's 4971S helps solve multivendor problems by allowing data capture with the upper-layer protocol information labeled. Systems developers can write their own applications programs using a softkey-guided programming language for statistics gathering, problem diagnosis or stimulus/response testing. Unlike the LANalyzer, HP's unit is a $30,000 piece of stand-alone hardware with an analyzer, a display, keyboard and dual 3½-in. floppy disks.

According to Subhash Bal, vice president of marketing for Excelan, that's the fundamental distinction between the two instruments. "The basic advantage we found after comparing the two products was our flexibility because we're based on the PC. We are telling people they don't have to buy a new instrument as such. All they do is buy our hardware and software, plug it in, and they can convert their PC into a very useful tool."

And because the LANalyzer is PC-based, trace and statistics files are standard DOS files. Bal admits that the instrument as presently configured doesn't provide for every testing contingency, but he points out that users can manipulate acquired data to serve their applications using the vast amount of available third-party DOS-based software. Hewlett-Packard's 4971S will communicate with other instruments capable of running third-party software, but because it uses a proprietary operating system, it doesn't offer as much flexibility as the LANalyzer.

The HP 4971S, although less flexible in its application, offers a higher level approach to LAN testing. It's designed for the larger network that combines mainframes and PCs in a dispersed environment or one with a large number of nodes.

(continued on page 48)

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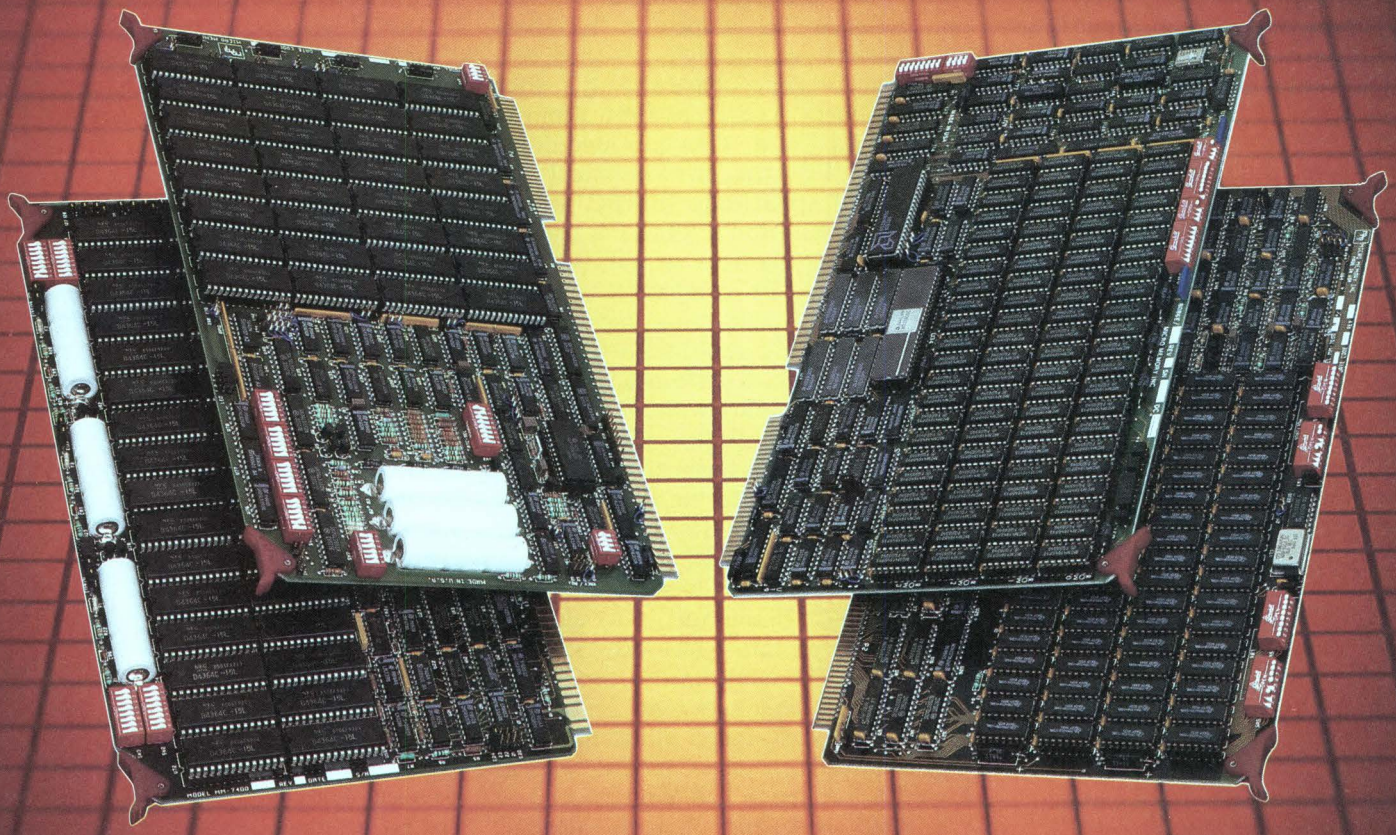

Micro Memory Inc. gives you a choice of either type of Multibus memory board... CMOS or DRAM, with capacities up to 4 Mbytes on a single board. On DRAM boards you can pick parity, Error Detection and Correction (EDC), or dual-port with LBX. CMOS boards have the ability to mix EPROMs with the RAM. Micro Memory Inc. offers you the widest choice of Multibus memory boards, which are completely compatible with systems employing 80286, 80186, 8086, or 68000 microprocessors.

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MM-7200D	256K, 512K, 1M, 2M	LBX (Parity)	330/220	64K or 256K DRAM
MM-8086E	256K, 512K, 1.5M, 2M	EDC	500/300	64K or 256K DRAM
MM-9000D	512K, 1M, 2M, 4M	Parity	350/240	64K or 256K DRAM
MM-8500C	64K, 128K, 256K	Non-Volatile	200/200	CMOS (Calendar)
MM-8550C	512K, 1M	Non-Volatile	150/150	CMOS (Calendar)
MM-8800C	**64K, 128K, 256K, 384K, 512K, 1M, 1.5M**	**Non-Volatile**	**150/150**	**64K or 256K CMOS**

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CIRCLE 22

Terminals add PC features to fulfill multiuser system demands

To fill what many observers believe will be a skyrocketing demand for terminals in multiuser systems, a new breed is emerging known as the PC terminal. An ASCII terminal with IBM PC-style keyboard, screen attributes and characters, the PC terminal is designed specifically for use in multiuser environments, many of which will be based on PC ATs. But beyond these PC-like features, the PC terminal will provide higher resolution characters, extended length and width displays, multiple-page display memory and more.

Market researchers predict this year will be an explosive one, claiming that multiuser system vendors moved far down the learning curve in 1985 with the PC AT. Dataquest (San Jose, CA), for example, projects that 183,000 terminals will be required for multiuser personal computer systems in 1986. Of these, half are estimated to be traditional dumb ASCII terminals and half the new breed of PC terminals.

Peg Killmon
Senior Editor

Although the terminal features necessary to compete in this arena haven't been firmly established, several contenders have already fielded products. As early as 1984, Kimtron (Santa Clara, CA) introduced the KT-7/PC—the first terminal designed specifically for PC attachment. Kimtron's KT-7/PC uses an IBM PC character set and has nonembedded PC-compatible video attributes. While minicomputer-style terminals use embedded or hidden attributes, which perform a bold or underline function without occupying space on the display, the PC's nonembedded attributes display the control codes used to perform these functions on the screen. The KT-7/PC is priced at $695.

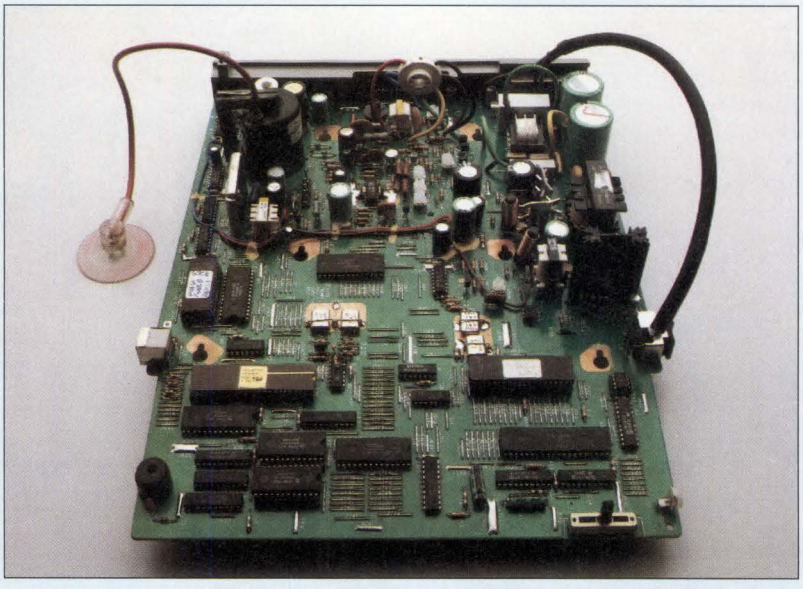
The following year, Falco Data Products (Sunnyvale, CA) unveiled the Falco 500, which now sells for $795. The latest entries come from Wyse Technology (San Jose, CA), which boasts that it will set new price and performance standards with its "full-function" WY-60, priced at $695, and Esprit Systems (Melville, NY), which is pursuing a goal of being a price leader with its ATerm that lists at $479.

Acknowledging that basic terminals will remain the mainstay of data-entry applications, Steve Holtzman, Wyse Technology's director of product marketing, believes that a wide range of features is extremely important in the multiuser world. "The market is willing to pay a premium for functionality that makes the terminal infinitely more useful, and increased attention will be paid to high-end, full-function terminals that meet future and emerging needs."

Responding to this belief, Wyse offers terminals with features that go beyond those of most of today's full-function terminals. Wyse's WY-60, for example, adds a 10-×16-pixel character, 44-line display capability, seven-page display memory and desktop accessories, such as a built-in calendar, alarm clock, calculator and ASCII reference tables. Three keyboard styles also are supported—the IBM 3161, IBM PC AT and WY-50, a typical ASCII keyboard with a special set of editing keys used in data entry applications.

The Wyse WY-60 is built around a highly integrated design in which the two or three boards normally required to achieve full functionality have been reduced to a single board. While the board design has three key elements—the logic circuitry, analog power supply circuitry and monitor circuitry—they've been designed as a single entity. This allows the sharing of components common to two or more elements.

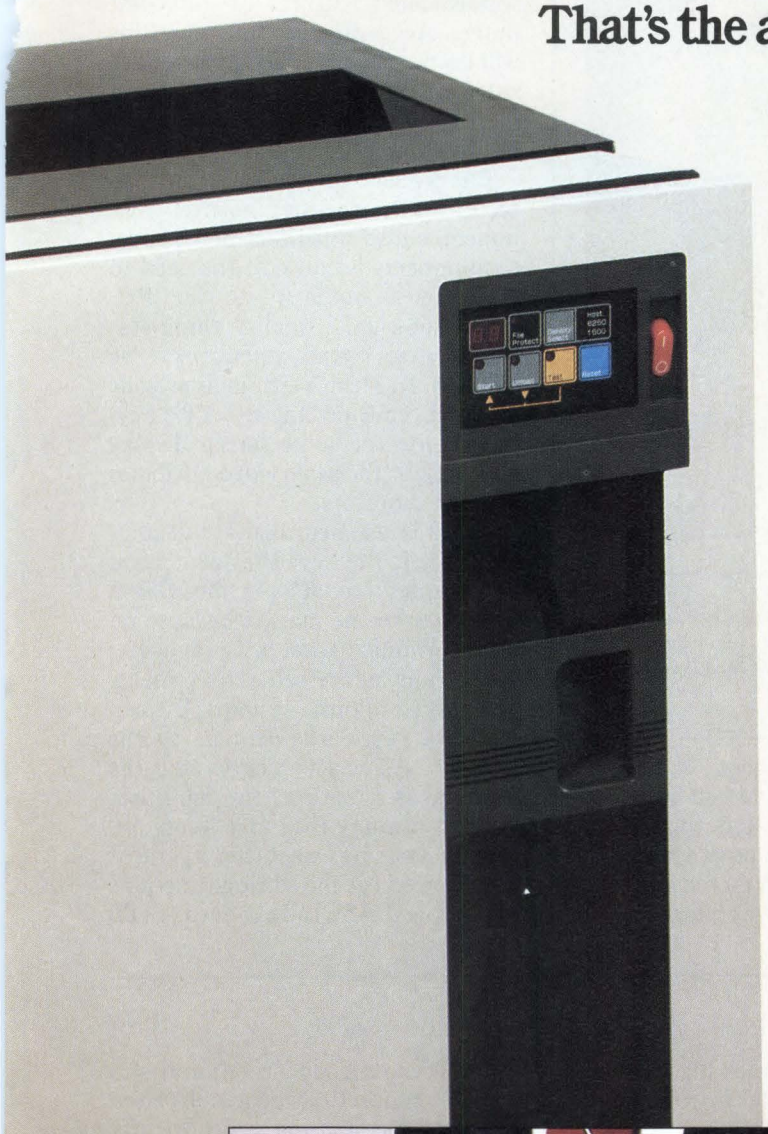
Increasing the screen's legibility with the crisply defined characters afforded by the 10×16-pixel character, both Falco and Wyse have addressed user demands for better character resolution. But the Falco 500 terminal takes this one step farther by using a flat screen coated with P-167 phosphor to provide a soft white background. "This background closely resembles the paper from which the operator reads," says Tom Sullivan, Falco's director of marketing, "and greatly reduces fatigue and



The single-circuit board design used in the Wyse WY-60 combines logic circuitry, monitor circuitry and power supply in one assembly.

With this high-performance GCR Streamer, the benefits begin with reliability and end with cache.

That's the advantage you get with a leader.



At Fujitsu America we want our back-up devices to be second-to-none in price, performance and reliability.

That's why we developed the M244X series ½" GCR tape drive with an intelligent 256KB cache buffer. The buffer means you get all the versatility of our start/stop drive, plus the speed and reliability of our streamer technology. Parameters such as transfer rate, block size and ramp times are all switch-selectable so you can easily optimize the drive for your system.

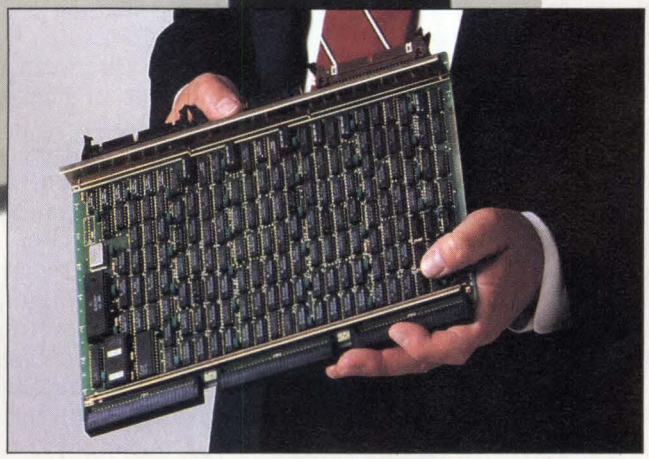
But the cache buffer is just the finishing touch on a tape drive that already outperforms the competition.

By incorporating Fujitsu's advanced LSI electronics, we have eliminated the high-cost, high-failure mechanics found in other low-cost GCR tape drives. As a result, you get a high-performance GCR Streamer with the best reliability rating—and the best price—in its class.

Throughout this drive's design, we have found ways to keep your cost of ownership to a minimum. The drive performs its own internal monitoring and self-adjustment, eliminating costly preventative maintenance. And the sophisticated diagnostics make it possible to isolate system faults without special test equipment.

For information on this or any other Fujitsu tape drive, call (408) 946-8777. Or write Fujitsu America, Inc., Storage Products Division, 3055 Orchard Drive, San Jose, CA 95134-2017.

The Fujitsu M244XAC GCR Streamer, with cache buffer. From price, to performance, to reliability—it's the best tape drive in its class.



Fujitsu Cache Adapter provides a 256KB intelligent memory buffer, increasing system performance.

MODEL	M2442AC	M2444AC
Tape Speed (ips)		
Streaming	100	75
Start/Stop	12.5	25
Recording Density (bpi)	6250/1600	
MTBF	8,000 hours	
Cache Buffer	256 KB	
Transfer Rate	Selectable from 60 KB/sec to 1 MB/sec	
Compatibility	IBM,® ECMA and ANSI	
Interface	Cipher,® Pertec compatible	

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CIRCLE 23

While supplying a PC AT-like keyboard that allows individuals to move easily between the console terminal and other terminals in the system, Esprit's ATerm maintains the 14-in. screen and tilt-and-swivel housing common to the ASCII terminal world.

eye strain, resulting in greater productivity."

In combination with improved legibility comes extended display. Supporting both 80 and 132 columns, the displays on both Wyse and Falco terminals have been extended to accommodate 44- and 40-line screens, respectively. This lets the terminals accommodate the large spreadsheets that are becoming increasingly common in multiuser applications.

Hidden, or embedded, attributes also let multiuser systems provide the sophisticated features of minicomputers. According to Holtzman, this will become increasingly important as software developers bring more and more sophisticated applications to the multiuser microcomputer world.

But Robert David, Kimtron's director of marketing, believes that nonembedded attributes better meet requirements because of the need to maintain a similarity to the PC. "This look-alike quality eliminates the need to retrain operators," he explains. Kimtron's terminals provide an exact replica of the PC AT's keyboard, use the same screen display and support the same video attributes as IBM monitors.

Esprit is also betting that full compatibility is the key. President John Sacco states that, at $479, the ATerm fills a gap in the market because no other terminal in that price range has specifically addressed requirements of PC AT multiuser systems. By providing a keyboard identical to the IBM PC AT, Sacco claims that the terminal is a natural for multiuser systems running Pick and Xenix operating systems, since the operator has no need for the editing functions of a typical ASCII keyboard. **CD**

Comprehensive analyzers ease...
(continued from page 44)

As a very high-performance troubleshooting tool, the 4971S can handle any network environment, says Dave Couch, product manager for HP's Telecommunications Division. "What we attempted to do is build a device that, regardless of the traffic rate on the network, will receive all data and not miss any frames. We haven't encountered a condition yet with which we can't keep up."

The key to this high performance is a sophisticated filtering mechanism implemented in the tester's hardware. The LANalyzer, in contrast, performs its filtering in software. As users define more complex filters, the ability of a tester with software-defined filters to track high data rates declines. But Linda Stewart, product marketing manager for Excelan, claims that the LANalyzer's ability to capture 1000 packets/s, coupled with its 700-kbyte trace buffer will handle "90 to 95 percent of the LAN environments that are out there."

But Couch has reservations. "The point is, when problems start to occur, they occur when you get bursts of traffic that the nodes on the network can't handle. To diagnose and troubleshoot those situations, you have to have a device that can keep up with the data rates and provide reliable and good data integrity regardless of network rates."

The 4971S also offers the flexibility to format incoming data as well as the ability to decode the various fields on all common LAN protocols. Even if a designer is using a proprietary protocol, the formatting capability of the 4971S' 16 filters can be used to define the protocol breakout and decode the protocols.

Despite their differences, both instruments can claim a common achievement. They dramatically simplify LAN testing. For many engineers, this should signal an end to tedious hours of configuring homegrown, ad-libbed LAN logging devices that provide—at best—a vague notion of LAN conditions. Comparing these devices with the new LAN testers, Couch says, "It's like someone all of a sudden turned the lights on." **CD**

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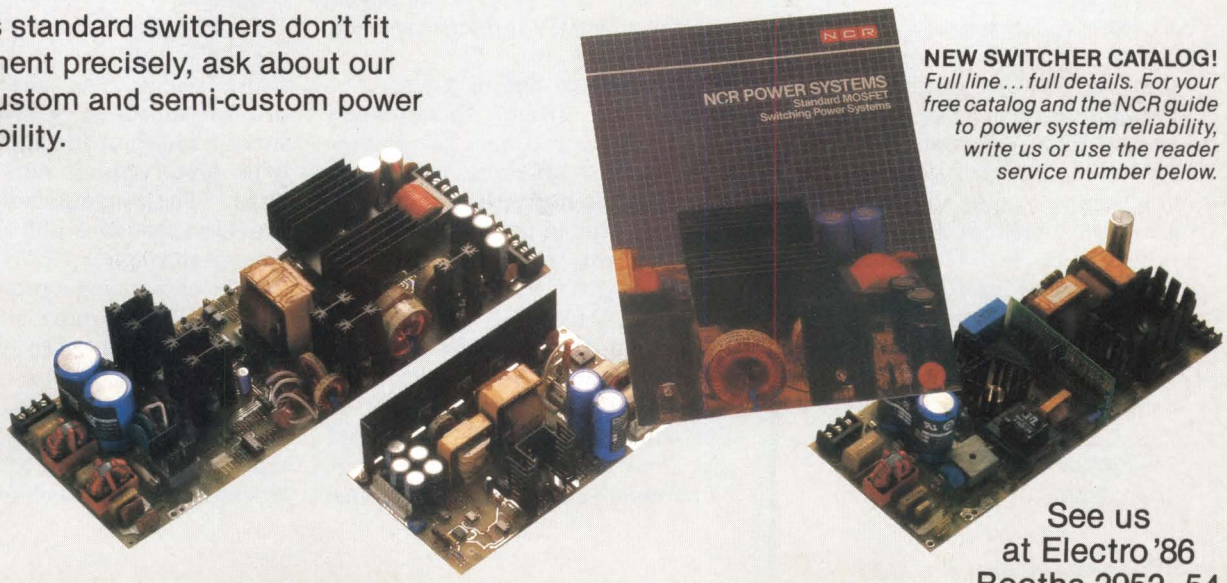

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Controllers drive performance up to meet system demands

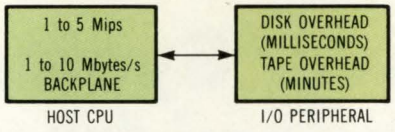
The link between peripheral storage devices and the CPU, controllers hold the key to improved system performance. As peripheral storage devices increase in capacity and speed, more intelligent controllers are being developed to provide the most efficient and cost-effective path to the CPU. Efficiency and cost-effectiveness also demand that the controller maintain compatibility with as many drives as possible so that peripheral storage capacity and performance can be tailored to specific needs.

To meet this combination of objectives, controllers must match the performance of the peripheral devices to that of the computer system bus. They must also balance the performance provided by the peripheral/controller combination with the system's throughput objectives.

The problem of performance relates both to the interface implemented on the peripheral end of the controller and to the methods used within the controller to move data between the peripheral and the system bus. As a result, controller manufacturers are struggling with the question of intelligent versus system-level interfaces as well as which functions to supply in the controller and which are better left to the host.

Systems with capacity requirements in the 300-Mbyte range are no longer limited to an 8- or 14-in. drive that operates on the Storage Module Drive (SMD) interface. Current choices are between 5¼- and 8-in. drives, and interface possibilities include the 10-Mbit/s Enhanced Small Device Interface (ESDI) or 1.2-, 1.8- or 2.4-Mbyte/s versions of the standard SMD. As increasing numbers of drives move to take advantage of the growing capabilities of protocol chips providing the intelligent Small Computer Systems Interface (SCSI), still more choices will open up. For users with capacity requirements beyond 300 Mbytes, the interface of choice is currently limited to SMD or one of its higher performance variants. But the increasing availability of drives using the Intelligent Peripheral Interface (IPI) will remove many of the capacity and performance restrictions for drives in this range.

Choices in tape drives are almost as wide. While Quarter-Inch Tape Cartridge Compatibility (QIC) standards form the device-level interface for most ¼-in. cartridge tape drives, the more intelligent ESDI promises to increase its hold. As disk drives sporting this interface become available, tapes will make the move to ESDI. Tapes will also feel the influence of the intelligent embedded SCSI, which will make its mark as SCSI controllers become more common. Tape drives will also acquire intelligent interfaces as IPI's influence spreads.



A basic performance mismatch found between the processor and the inherently slower peripheral device is the target of controller technology. To minimize the differences in performance between the two, the controller can overlap operations of several peripherals to provide more efficient access to data.

Interface choice tied to goals

While it's difficult to say where each interface will have the greatest impact, most observers are betting that SCSI, no matter how smart, will find only limited use in high-performance systems. According to Richard Tam, director of marketing at Sysgen (Fremont, CA), SCSI will be slow to have an impact in the IBM PC market because of the development effort that has already been invested in QIC-36 tape controllers and ST506 disk controllers. Sam Miller, director of hardware engineering for Tecmar (Solon, OH), on the other hand, sees SCSI being used more widely in PCs, although it still hasn't gained much acceptance. "With a system like that," Miller says, "you can throw a very large drive in and it will be totally transparent to the system."

Despite the pessimistic bets of some, there are several advocates of SCSI for high-performance applications. Adaptec (Milpitas, CA), for example, supplies a link between Enhanced SMD drives and SCSI with its ACB-5585, a 15-Mbit/s ESMD controller, and between ESDI and SCSI with the ACB-4520, a 10-Mbit/s ESDI-to-SCSI controller. Adaptec sees workstations and multiuser systems as potential applications for SCSI. The 5585 can control four disk drives simultaneously, enabling concurrent execution of tasks on all attached drives. "This can supply double the I/O performance of other boards," says Jeff Miller, vice president of marketing. The 4520 maximizes I/O performance by supporting noninterleaved operations with an 8-kbyte on-board buffer.

"The primary impetus for embedded controllers will come in the SCSI arena," says Harry Laslow, product marketing manager for peripheral controllers at Intel (Santa Clara, CA). He already sees rapid movement away from bridge adapters and ST506-to-SCSI controller boards toward embedded controller products.

Bryan Fifield, director of marketing for storage products at Emulex (Costa Mesa, CA), sees the move toward embedded SCSI picking up speed because of the number of systems manufacturers now looking at SCSI. "These manufacturers hope to provide a standard I/O link to their systems through SCSI," says Fifield, "while maintaining a proprietary system bus." This move should make embedded SCSI more meaningful. "On top of that," he emphasizes, "SCSI performance is increasing. While transfers over SCSI are currently limited to about 1.25 Mbytes/s by chips in use, new chips will move

Peg Killmon
Senior Editor

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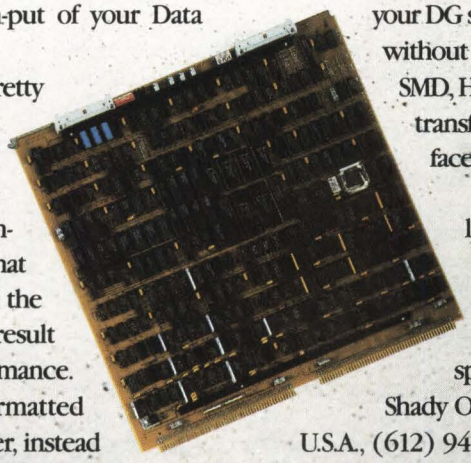
Now you can make a high performance system even faster: Zetaco's Argus-emulating disk controller, Model ARZ-1, will improve the through-put of your Data General Eclipse/MV.

ARZ-1 isn't just another pretty interface. It is the most intelligent controller ever designed for the DG world. It acts as a co-processor, off-loading the data command functions from the CPU so that your MV can do other tasks while the controller manages the disk. The result is significantly faster system performance.



ARZ-1 offers greater formatted storage capacity, too. The controller, instead of the software driver, maps the disk, thereby obtaining maximum use of the available capacity. No longer does the drive need to fit a specific head/cylinder/sector configuration to work with your DG system. The ARZ-1 does the work – without patching, without hassle. Any four SMD, HSMD or SMDE disk drives, with data transfer rates up to 3 MB/sec, can interface the ARZ-1 via the high-speed BMC.

The ARZ-1 Disk Controller. Fast. Efficient. Designed to reach new horizons of higher performance.

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ZETACO

The Link To Tomorrow.

CIRCLE 26

that performance up considerably, and should also make it more attractive."

Emulex, for one, is producing its own SCSI protocol chip. This chip will be able to operate at rates of better than 4 Mbytes/s in synchronous mode; asynchronous performance will be at 3 Mbytes/s. Using such a chip in conjunction with buffer controllers and formatters, drive manufacturers will be assured of the best possible performance. Systems manufacturers can use the chip in conjunction with a buffer controller to build host ports into their processors or to build their own host adapters.

While the disk drives that embed SCSI interfaces typically have a 20-Mbyte capacity, this may change if the move by systems manufacturers to supply SCSI as their I/O bus takes hold. There seems to be general agreement, however, that this interface will appeal primarily to those who want to attach several different devices to their systems, rather than attach several like devices. Users who must attach many devices to achieve the on-line storage they need are also looking for higher performance than is generally associated with SCSI devices. "Backup storage media," explains Chappell Cory, Xylogics vice president of research and development, "tend to have more formatted functionality in them than is found in system disks." Because of this, Cory believes that there will be far more embedded SCSI in backup peripherals than in system disk drives, even though SCSI can be used on either.

When it comes to tape, it seems unlikely that users of ¼-in. cartridges will pay the price to embed the SCSI interface. In spite of this, SCSI will play an important role in the ¼-in. tape cartridge market. Here, Fifield believes that SCSI will act as the bridge between ¼-in. cartridge products and ½-in. cartridge products using IBM 3480 technology.

Dick Rausch, vice president of marketing at North Atlantic Industries' Qantex Division (Hauppage, NY), predicts that ESDI will become a dominant interface when the ½-in. tape cartridges appear. With ESDI as the native interface, these higher capacity cartridges will use serpentine recording techniques with the IBM 3480-type cartridge to supply capacity beyond the currently perceived limits of ¼-in. cartridges.

ESDI is also seen as essential in the 5¼-in., form-factor high-capacity disk drive arena. Intel's Laslow points to ESDI as having a place in engineering workstations and high-end desktop computers that demand high performance and high storage capacity. As ESDI disk drives become available from Hitachi, Maxtor, Micropolis and Siemens, demands for capacities of 140 to 300 Mbytes can be met with 5¼-in. form-factor disk drives. Controller products an-

Intelligent interfaces create test problems

The emergence of intelligent interfaces along with the use of higher levels of integration is moving many functions into the controller. Since these signal-processing and buffering functions are intended to present clean data to the system, they mask the real performance of the drive and make it almost impossible for the end user to test the drive.

"With the increasing recording densities of devices, the ability to produce flawless media decreases exponentially," notes Frank Meijers, president of Luctor (Phoenix, AZ), a manufacturer of disk drive test equipment. "Marginal conditions in headers, sync bytes and other critical areas will go unnoticed if testing is restricted to what is available through the interface controller, and these may ultimately lead to catastrophic failure. What's more, it's naive to regard self test and error correction as a panacea for all the drive's potential ills.

"The extra circuitry increases costs, error correction degrades the performance and the number of errors continues to go up exponentially with the increases in recording density. In addition, unexpected errors in areas such as headers could prove to be fatal," says Meijers.

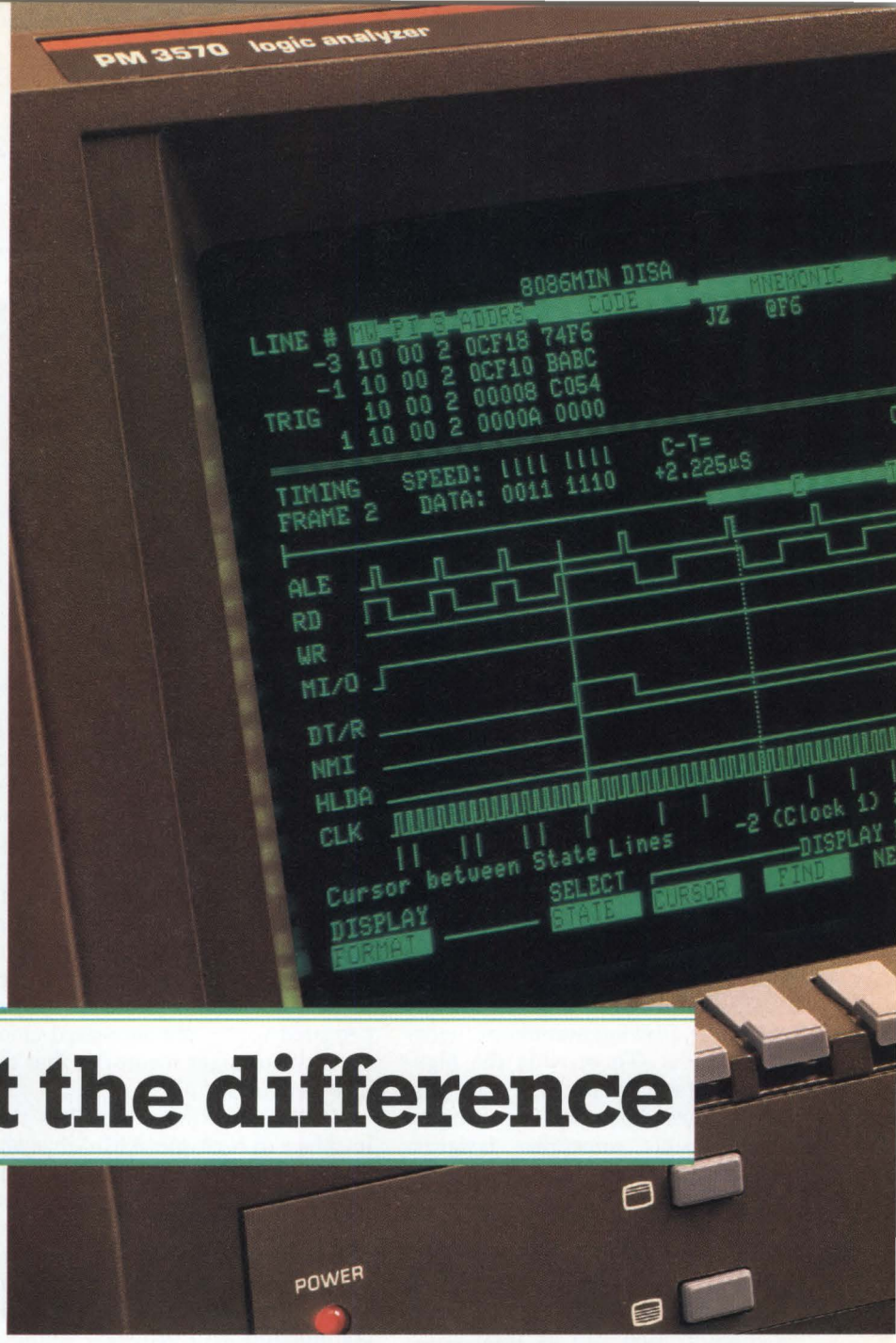
To provide adequate testing in all situations, Meijers believes that the test equipment must be able to take real-time control of the drive without interference from the controller. While ESDI and SMD interfaces contain features that are suitable for test applications with minor modifications, thorough testing of drive and media through these interfaces requires several additional signals to allow access to analog signals and to pulse write/read data. SCSI and IPI interfaces, however, compound these problems with their intelligent features and pose some particularly difficult problems with VLSI and LSI implementations. To remedy this situation, Meijers advocates implementing intelligent interfaces in such a way that the controller can be bypassed and the drive's vital signals made accessible in real time.

To enable a drive with an SCSI interface to be tested, for example, a special access mode should be added to the command protocol to allow direct addressing of cylinders and heads. The buffered data channel of SCSI drives should be bypassed by supplying access to real-time signals and a command that disables the data controller access and prevents faults generated by the disabled data controller from getting to the command controller.

Unfortunately, current interface standards do not go far enough to ensure testability, frequently defining irrelevant values and omitting the definition of methods and conditions necessary to measure critical values. To ensure testability, standards must define not the specific kinds of disks and a set of values, but rather the test methods to be used, nomenclature and equipment and procedures.

To address the requirements that Meijers feels are essential to effective testing, the Ansi X3B7.1 Disk Test Methods Committee has extended its charter to include standards for test interfacing and may ultimately provide a set of recommendations for each type of disk drive by interface.

Double your logic analysis capability!



The new PM 3570 Logic Analyzer featuring the dual-screen mode allows you to perform time-correlated state and timing analysis with no less than 115 channels simultaneously. Built-in performance analysis permits system optimization. Other special features include:

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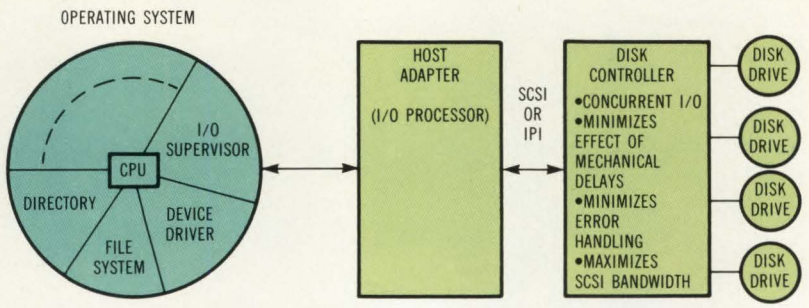

An intelligent I/O controller significantly increases the performance at the system level by handling many functions previously relegated to the host operating system.

nounced to date put this interface on the VMEbus and the Multibus and have joined it to the SCSI bus.

Fast buses drive technology

The factors that have driven the growing desire to shift from ST506 to ESDI interfaces—not an easy switch from a system designer's standpoint—include cries for higher capacity disk drives and demands to fully utilize the growing number of higher speed buses. To provide the high-speed data path necessary to pass data to these buses at the maximum rates possible, controller designers feel that it's necessary to maintain a device-level interface to the drive itself.

While consideration of the system bus—whether PC or mainframe—to some extent constrains the amount of technology that can be used effectively, considerable value remains to be added through controller technology. At issue here is where to put the intelligence—use a device-level interface or an intelligent interface at the controller? There are three basic choices: the first puts enough intelligence in the device to allow high-level language communications between disk and computer; the second is semi-intelligent, putting some control functions in the device but leaving others to be performed by the host; and the third, a strictly nonintelligent approach, simply lets all device control reside in the host.

Dave Friesen, vice president of marketing for Alloy Computer (Framingham, MA), says that using host resources is cheaper than building that resource into the controller. Concentrating on disk capacities of 50 Mbytes and above, Alloy's approach is to use host-resident software and main memory cache to obtain maximum performance from the peripheral/controller combination. "The overhead incurred by the processor," claims Friesen, "is compensated for by the increased clock speeds and larger memories that the host provides."

Vendors making controllers that interface to high-speed Multibus and VMEbus have taken similar tacks. In its 712 ESDI-to-VMEbus controller, Xylogics meets the high-performance demands of multiuser Unix systems by incorporating an 8-kbyte first-in, first-out buffer in the controller. In conjunction with firmware supporting elevator seeks, scatter/gather reads and writes, and command chaining, the buffer lets data be taken off the disk at its 2.4-Mbyte/s rate and transferred directly to system memory via DMA at a 10-Mbyte/s rate. Unlike other FIFO implementations, the buffer can be filled and emptied simultaneously, eliminating data overflow and rotational latency problems.

The approach that Interphase (Dallas, TX) has taken to supplying the highest possible performance is to move intelligence to the controller, and put a lot of buffering on board using deferred write and read-ahead commands to take advantage of the buffer and the bus speed. "By playing sophisticated games at the controller level," says Ed Gross, manager of disk/tape controllers, "significant increases in system performance can be achieved."

Interphase sees a lot of activity in the VMEbus arena for ½-in. tape controllers. In demand are fast, intelligent controllers that squeeze as much performance as possible from the tape drive. One way to accomplish this is to use intelligent caching. Rather than handling commands sequentially, they can be stored in a circular command queue so that the controller can perform look-ahead fetches for the next block of data.

Even more important in achieving the greatest gain in system performance, according to Tom Thawley, Interphase's executive vice president, is close coupling. Gains in performance can be achieved by interconnecting disk and tape controllers so that data can pass back and forth without going through the system memory. This can reduce bus bandwidth requirements by as much as 50 percent.

"As disk drives have progressed, making good on their promises, controller technology has moved ahead to utilize these advances."
—Lynn Speaker
Zetaco

While Interphase currently doesn't supply a controller for ESDI tape drives, Gross says that the company's V/ESDI 3201 disk controller contains

Does A True ESDI Controller Really Exist?

If today's claims and counterclaims leave you unsure of just what constitutes a true ESDI controller, you are not alone. Still, from all the confusion one fact is clearly emerging: simply put—*"a fully effective ESDI controller has to be one that allows your system to take maximum advantage of the SCSI bus."*

To achieve this, the controller must offer these performance features: A 64-Kbyte continuous circular buffer. Burst rates of 1.5 to 1.85 megabytes per second. Full through-parity, connector to connector. Capability to format while off the bus. Programmable sector sizes. Full support of write/verify commands. 48-bit ECC. And the ability to format the drive with redundant ID fields to increase error recoverability.

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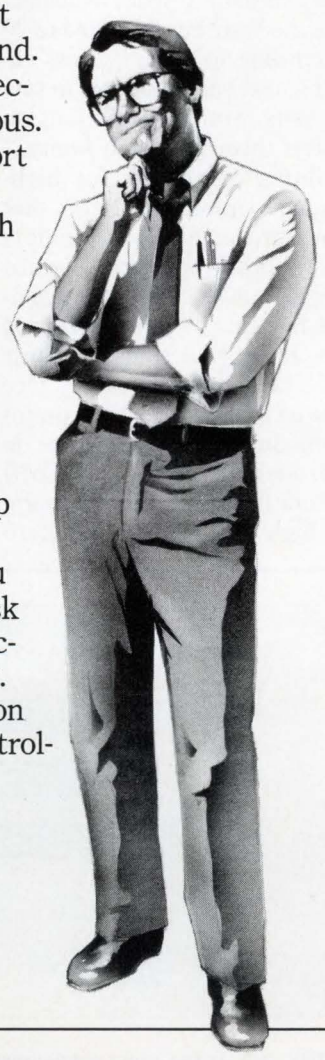
So next time someone talks to you about an ESDI controller, be sure to ask about its speed, data integrity and functionality. Or better still, ask ADSI first. Call 714-594-5858 for full information on the D200 and all our disk and tape controllers and VLSI custom chip sets.



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CIRCLE 28

all the necessary hardware. Firmware containing the commands and software interface needed for use with tape drives is under development and will be available late this year.

Multibus and VMEbus controller vendors also maintain that multifunction controllers have potential. Intel's Laslow sees the move in the Multibus area as being stimulated by the form factor of the board as well as by the desire to minimize total system board count; it's possible to implement a hard disk controller and still have room left. With the smaller VMEbus board, the move is propelled more by the limited amount of space available. "Because the VMEbus is limited to 20 slots, according to spec," Gross explains, "big users are interested in saving card slots. Multiple functions on a card offer them this opportunity."

In building controllers for high-performance minicomputers that maintain a proprietary bus, vendors encounter similar problems. Zetaco (Eden Prairie, MN), for one, counters these handicaps by concentrating on zero latency designs. "These designs," says Lynn Speaker, vice president of marketing, "rely on independent dual microprocessors on the controller to handle tasks offloaded from the the CPU while maintaining high performance." Zero latency results from the use of two-sector buffers that operate in a ping pong or alternating fashion. "The performance advantage is that overflows and underflows are eliminated along with housekeeping overhead."

Key to high performance

The key to keeping performance high while adding the ability to perform such functions as proximity seeks and command queueing, says Speaker, is to replace previously used bit-slice processors with higher speed processors such as Advanced Micro Devices' 29186 and 29286. Along with the faster micros, larger RAMs and EEPROMs bring additional benefits. Also, because functions such as error checking and corrction code are implemented in a parallel fashion, they can occur without interrupting the data flow.

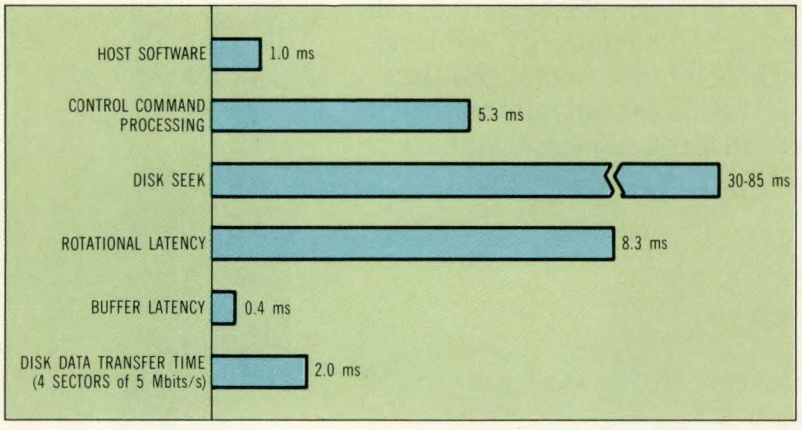
Those building controllers for the Multibus and VMEbus market are also excited about the prospects of IPI. Interphase's Gross comments that IPI's potential performance blends in very well with the performance of the VMEbus. And Xylogics' Cory sees IPI-2 as a natural progression from SMD. "It's about time that IPI-2 started taking over for SMD," says Cory, "and 1986-87 is the year that the transition will begin, as IPI-2 takes off as a device-level interface."

A lot of effort is now going into the IPI-3, a high-level intelligent superset of IPI-2, which Cory maintains is more "mainframish" in terms of applications. "Since backup storage devices tend to have more formatted functionality in them than system disks do," he observes, "they are better suited to IPI-3."

Bill Martin of Control Data Corp's OEM marketing group (Minneapolis, MN) describes IPI-3's benefits as relating both to the increased transfer rate and the intelligence that's provided. The intelligence supplied gives the ability to move the queue of work from the CPU to the controller. "This will cut the traffic back and forth to the CPU significantly."

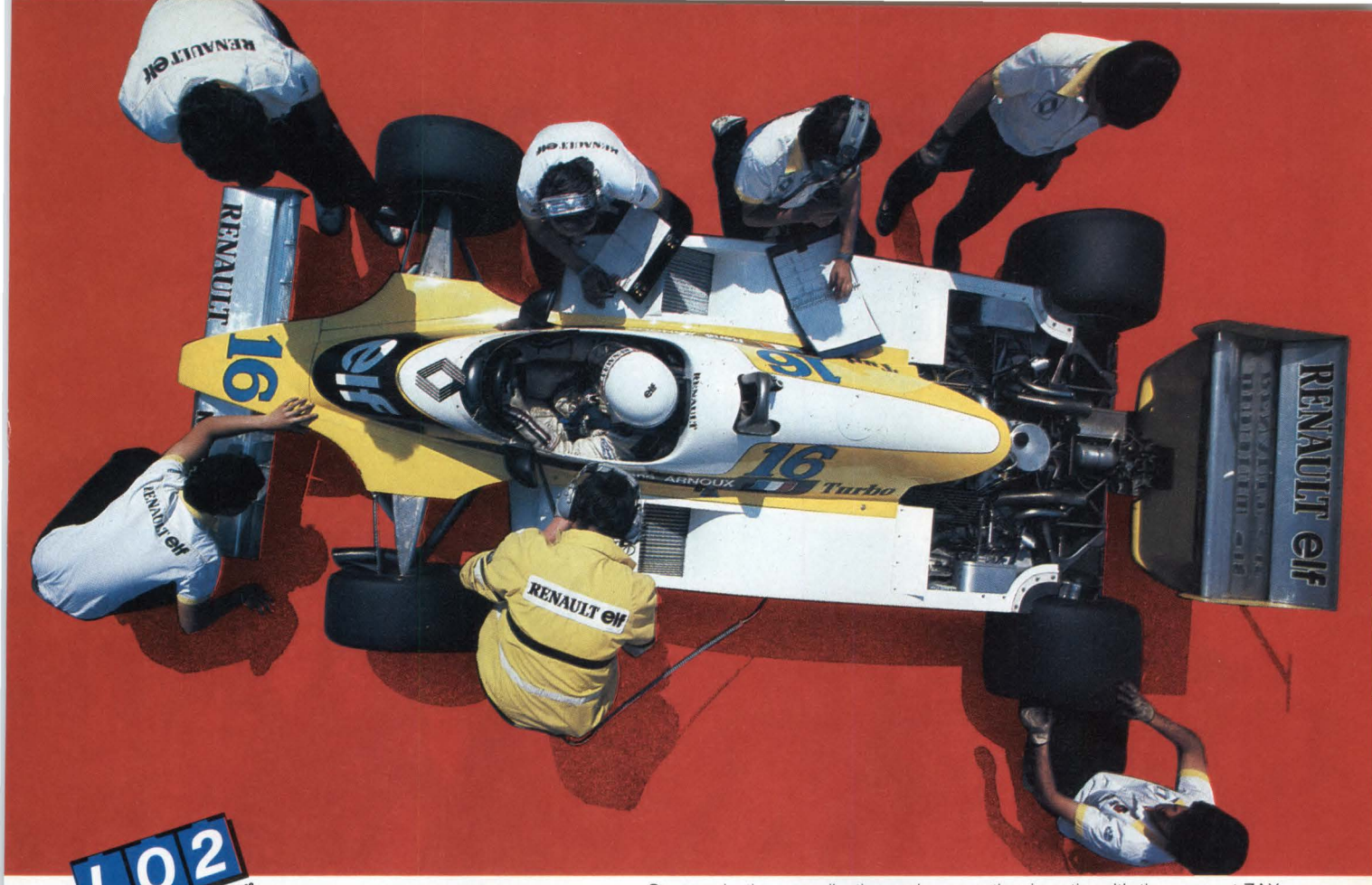
Describing simulation studies performed on the CM3 controller, an unannounced CDC product that puts IPI-2 to work on the device side and implements IPI-3 on the host side, Martin says that in one situation, bus utilization was cut from 30 percent to 10 percent. "This is significant because the CPU's workload goes down, and the bus, because it is less heavily utilized, can handle more devices without degrading system response time," Martin points out.

More important, however, than which interface at what speed will be used on tomorrow's disk or tape drives is the fact that technological advances are becoming solid and reliable. "As disk drives have progressed, making good on their promises, controller technology has moved ahead to utilize these advances," observes Zetaco's Speaker. The move to offload burdensome tasks from the CPU to the controller will continue at an even more rapid pace, allowing controllers to make an even more significant contribution to the performance equation. **CD**



The disk seek is the most time-consuming aspect of a typical disk access operation, and cache memory in the controller can significantly speed data transfer. Such on-controller cache keeps one or more tracks of information accessible. This reduces the need to seek to disk since the next data requested can frequently be found in the controller's cache.

Look for Mike Bloom's technology report on simulation accelerators in the May 15 issue.



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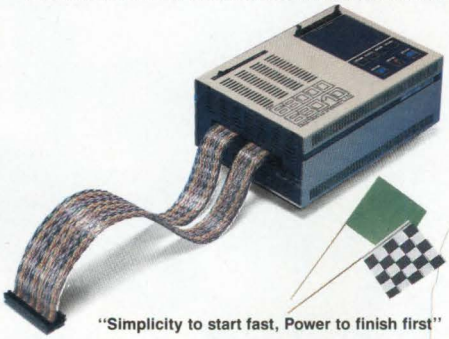

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CIRCLE 29

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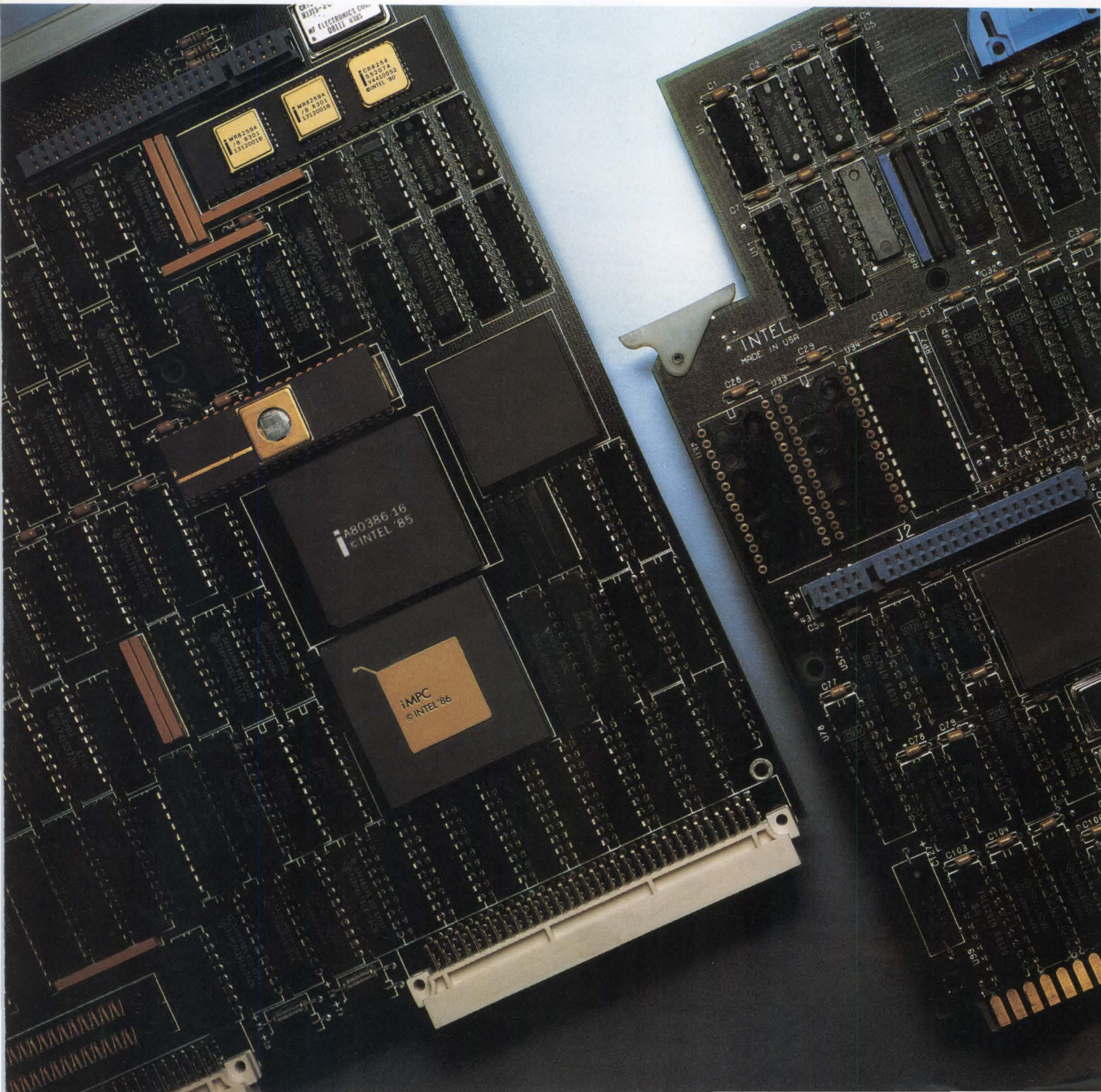

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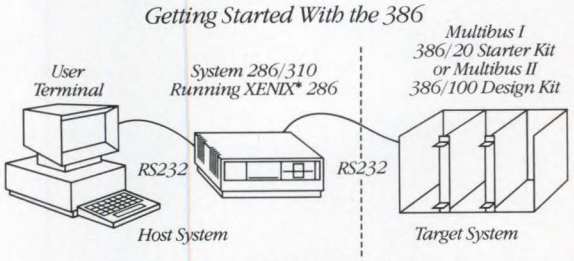

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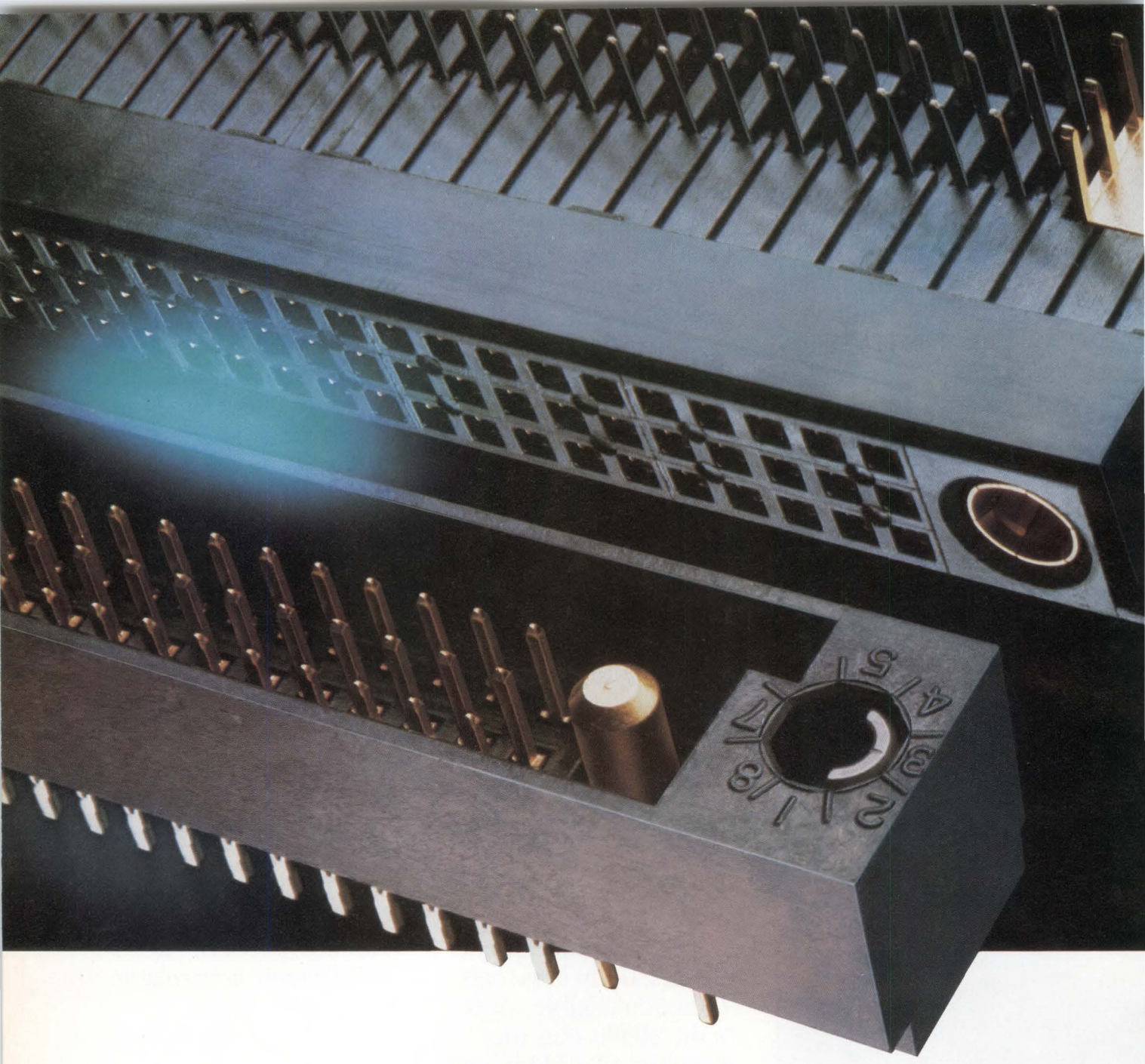
CIRCLE 30



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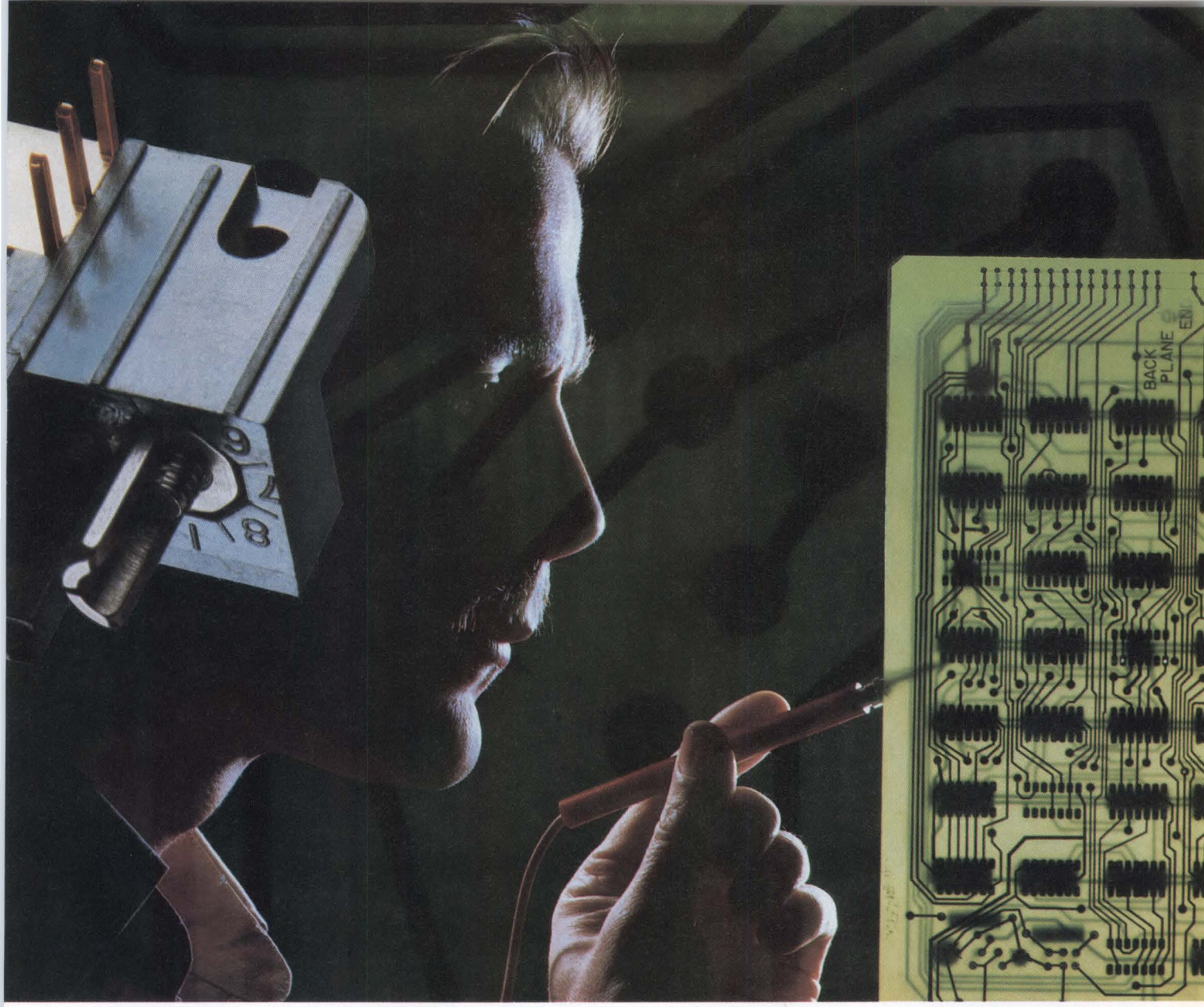

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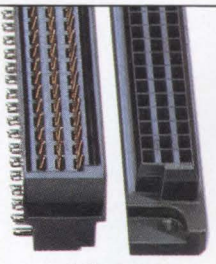

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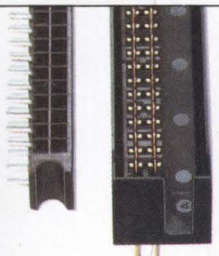

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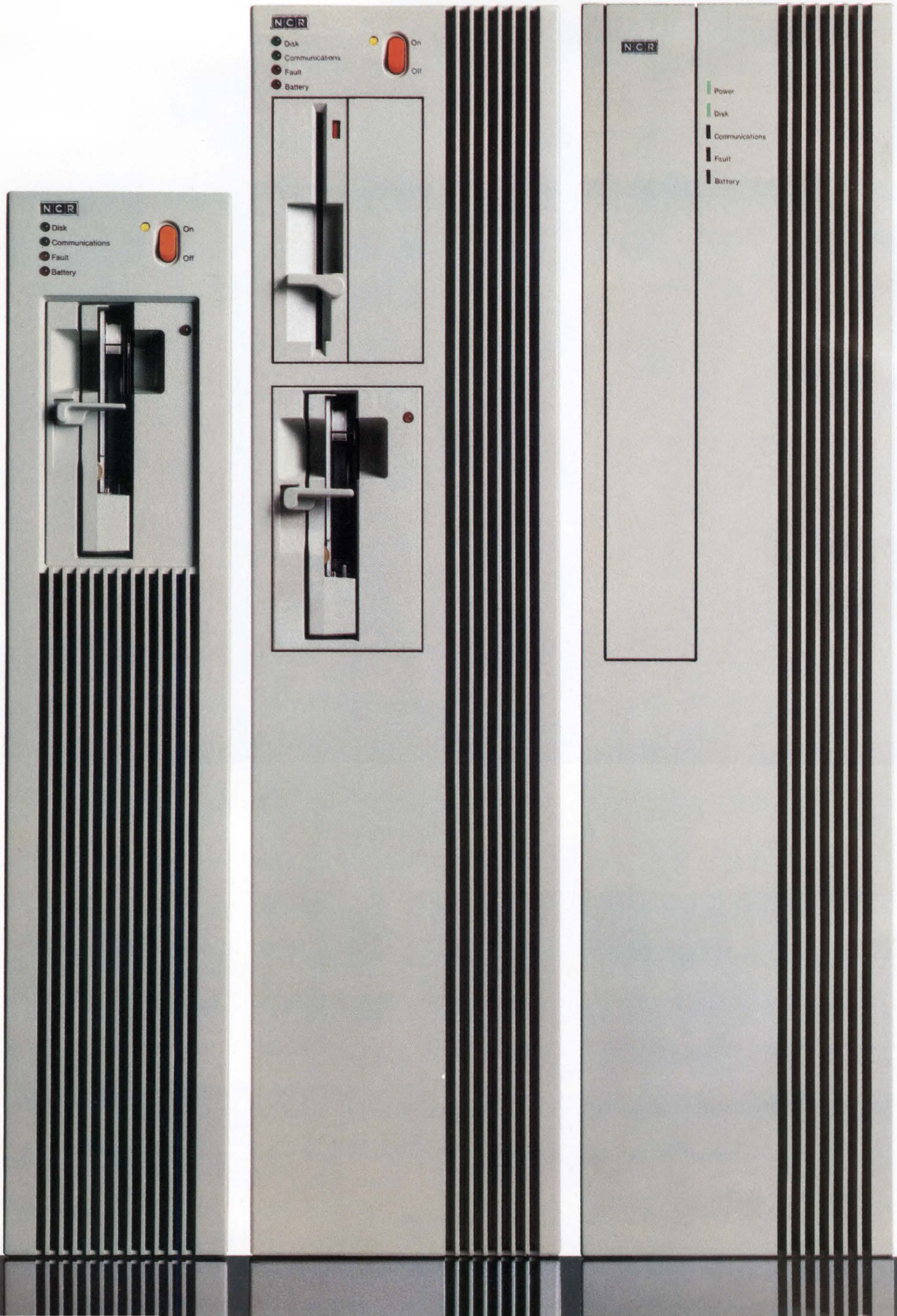
CIRCLE 31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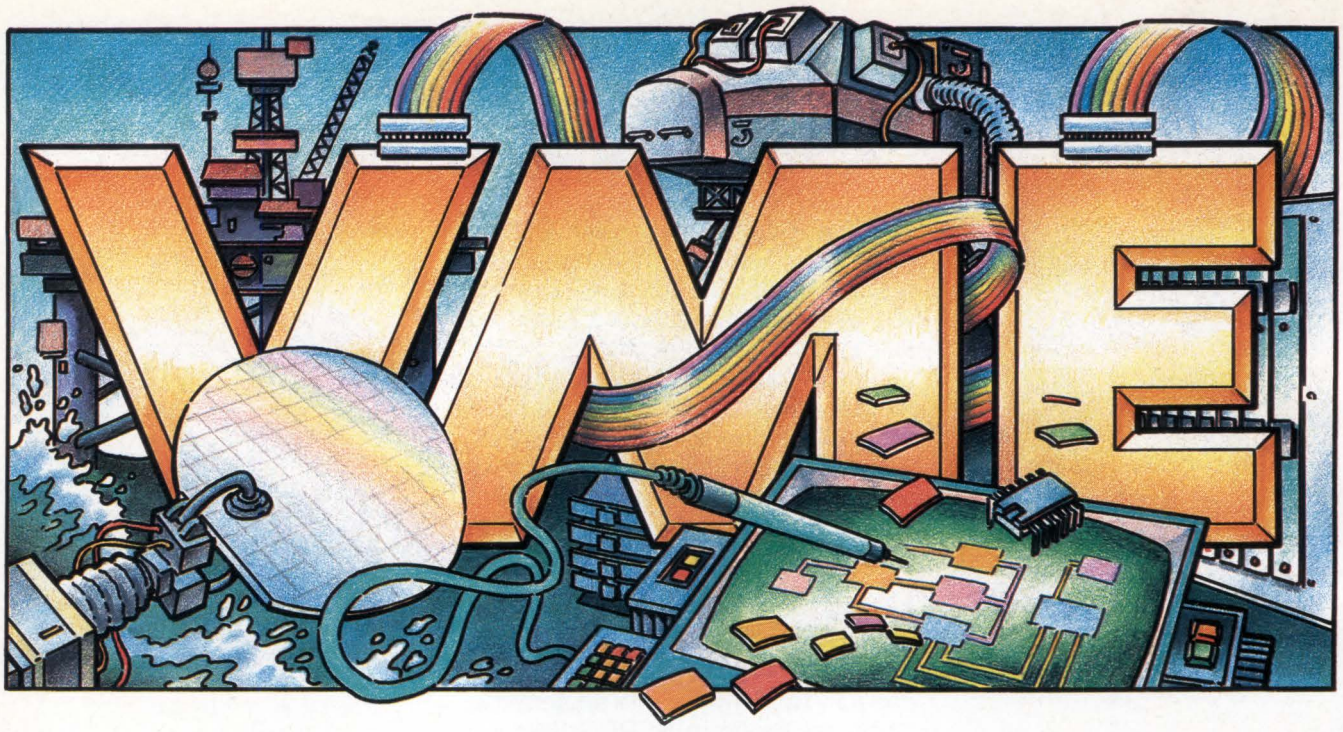

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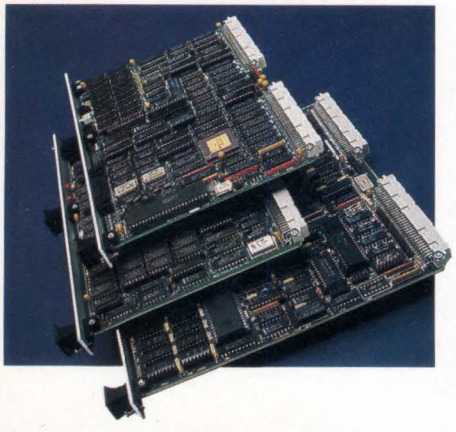

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CIRCLE 33

Super chips bring unprecedented power to graphics display control

The speed, resolution and text/graphics integration requirements of today's color graphics displays are being met by a new generation of display controllers that incorporate dedicated microprocessor functions.

by Tom Williams
Western Managing Editor

For the foreseeable future, graphics will consume all of the processing power we can throw at it." This is how Mark Olson, product marketing manager for Intel's graphics component division, sums up the efforts of major semiconductor manufacturers to produce engines that can keep up with user demands for graphics systems, but at prices that will make them practical in a broad range of applications, especially in desktop office/engineering workstations.

Over the past several months, these efforts have yielded a crop of graphics processors that go beyond the capabilities traditionally associated with graphics controller ICs. These new chips are characterized, in varying degrees, by microprocessor functions incorporated on the chip with display memory control, and in some cases, display control circuitry as well. Their instruction sets are tailored to their roles as graphics coprocessors and these chips can fetch and execute their own instructions without the constant attention of a host CPU. But beyond these similarities, each member of this new generation of ICs represents a design philosophy with its own unique trade-offs, advantages and limitations. These chips offer great power, but the question for the system designer is, "How much power at what cost?"

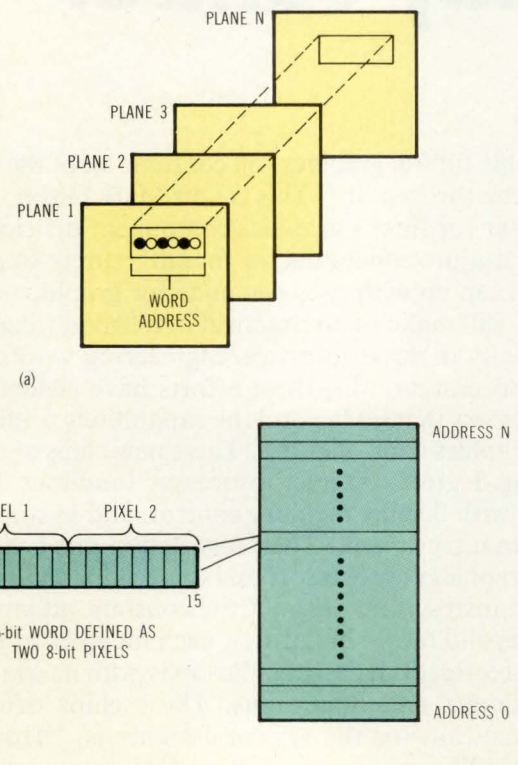
Graphics systems place two different demands on computation power. The first, and the most math-intensive, is the generation of the display list. A processor, usually the host CPU or a special display list processor, translates program instructions into instructions for lines, arcs, polygons and similar drawing primitives. This display list processor, sometimes called a geometry engine, usually requires floating-point calculations, especially when it's working with three-dimensional objects. The output of this processor is a display list—a series of drawing commands for the display processor that represent a specific frame or picture.

In essence, an object may exist as a software model somewhere in the computer and the display list processor translates that abstract model into a display list specification for a particular view of that object. The display processor then executes the display list by writing pixels into a display memory. Appropriate video control circuits then shift the pixel data serially out of the display memory and send them to the CRT for display.

Changes that must be made to the display are increasingly being done by moving blocks of pixel data around in the display rather than redrawing the entire display. Such moves require processing power in the form of address generation and read/modify/ write operations that would bog down the host. To avoid this problem, processing power is being incorporated in dedicated display-control silicon.

The new generation of processors are testimony to the emergence of bit boundary block transfer (Bitblt) as the acknowledged method of handling text and graphics elements in a display system. The extensive use of Bitblt, also known as raster operations (raster ops), requires that processors operate in terms of the bit boundaries, or number of bits per pixel, in addition to the word boundaries common to microprocessors. In addition to clock speed, these processors need architectural features tailored to the rapid movement of blocks of display memory (also called frame buffers or bit maps) of varying sizes from place to place in the display memory.

The primary requirement for the graphics display processor is speed. Speed is a product of raw clock speed, efficiency of the processor design, a balance between the hardware and software implementation of certain functions, and the overall architectural design of the display system, especially those elements related to the organization and management of the display memory.



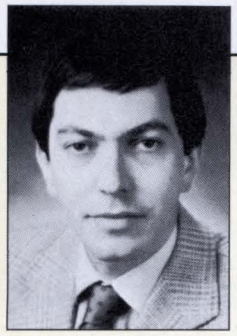
A bit map can be configured in basically two ways. In a plane architecture (a), the processor addresses a word in each plane. Corresponding bits in each plane define the color or gray values of a pixel. To modify multiple bits in a pixel, the processor must address each plane in succession or have some scheme for addressing planes in parallel. In a packed pixel architecture (b), the bit map is a single linear address space and pixels are defined as fields within a word up to the size of the word. All bits in a pixel can be modified with a single access.

Managing the bit map

The overall approach to the management of display memory is the primary distinguishing characteristic among display processors. Display memory, or more properly, displayable memory, refers to the entire range of memory the display processor is capable of addressing. Because the address ranges of these processors is often as large as 4 Mbytes, all of the display memory can't be displayed at once. The frame buffer, or bit map, is that portion of display memory currently being used to furnish data output to the CRT.

In a single-plane system (one bit per pixel) each bit maps directly to a corresponding pixel (picture element) that's either turned off or on in a monochrome display. In color systems or monochrome systems with gray scale, there may be more than one bit defining each pixel, but each such cluster of bits, be they arranged in memory planes or in a linear address space, maps to a specific pixel on the screen.

In systems with display memories larger than the bit map used for the current display, the display processor can change the display in basically three ways. It can write new data into the bit map from instructions it receives from the host, it can redefine different areas of display memory as the current bit map or it can transfer blocks of pixel data into the current bit map from other portions of display memory. In addition, some processors can use display memory to hold nongraphics elements such as commands, tables and other data needed to manage the display. These elements, while not pixel data, are also contained within display memory although they will never be output to the CRT.



Steve Dines
Director of Strategic Marketing
Advanced Micro Devices

Bitblt—a new measure of performance in display systems

The rapid drop in semiconductor prices during the last decade has fueled the acceptance of the bit-mapped raster scan display. Because the bit map can be considered from two different perspectives, this newer technology is essentially a bridge between two older technologies—the alphanumeric and the random vector (stroke writer) display. The traditional alphanumeric market sees bit-mapped technology as a way to bring both text and graphics to the office and home environments. The traditional random scan market, however, sees bit-mapped technology as a vehicle for cost reduction with little sacrifice in features. This dual perspective is neatly encapsulated in the benchmark performance figures that can be calculated for bit map update. The vectors-per-second measurement is an important benchmark for the traditional vector-based application. It indicates how fast a multivectored image can be recreated on the screen.

The newer benchmark is the speed with which pixels can be moved either within the bit map or between the bit map and the system bus. This pixel movement is known as bit boundary block transfer (Bitblt). The true significance of this benchmark, however, is subtle, and has particular relevance to the operation of a modern workstation. The two major areas that are affected by this benchmark are text location and windowing.

Early attempts to produce combined text and graphics bit-mapped displays resulted in alphanumeric text superimposed over a bit-mapped image. The question that arises is, "Why bother with alphanumeric text overlays even in the presence of a bit map?" The answer lies in the difficulty of supporting bit-mapped text. While the modern alphanumeric terminal imposes relatively minor demands on the computational element, the bit-mapped textual approach demands a much more powerful computational element for the same degree of interactivity. This is due to the way in which the text is manipulated by the CPU. Alphanumeric text is stored as byte or word strings. The insertion or deletion of text comes down to byte or word moves in memory—actions that are speedily handled by most off-the-shelf DMA controllers and CPUs.

The insertion or deletion of text in a bit map, however, demands the movement of actual character patterns. Moving the character in this form (compared with moving its byte representation in the alphanumeric situation) is computationally intensive for two reasons. First, at least 100 bits must be moved for a 10- × 10-pixel, black-and-white character, and even more than this if color is used. Second, the alignment scheme of the character pattern with respect to memory word boundaries may necessitate barrel shift and merge operations. To achieve any reasonable degree of interactivity (usually defined as a 0.1-s or better screen update), computation power far beyond the capabilities of a single-chip microprocessor is required.

Today the creation of a bit-mapped character on the screen is simply the movement of the set of pixels that represent the character from the font area to the screen area of the bit map. In the monochromatic single-plane implementation, the font is clearly stored in the plane, and treated as a Bitblt source as required. In a multiplane color environment, font storage is a more subtle issue. Color text can be generated from single-plane fonts by using the stored character pattern as an activity mask. In addition, foreground and background colors are separately specified. This scheme supports color text, without requiring an area for font storage on each plane. In this situation, it's the responsibility of the graphics engine to perform the necessary background/foreground processing.

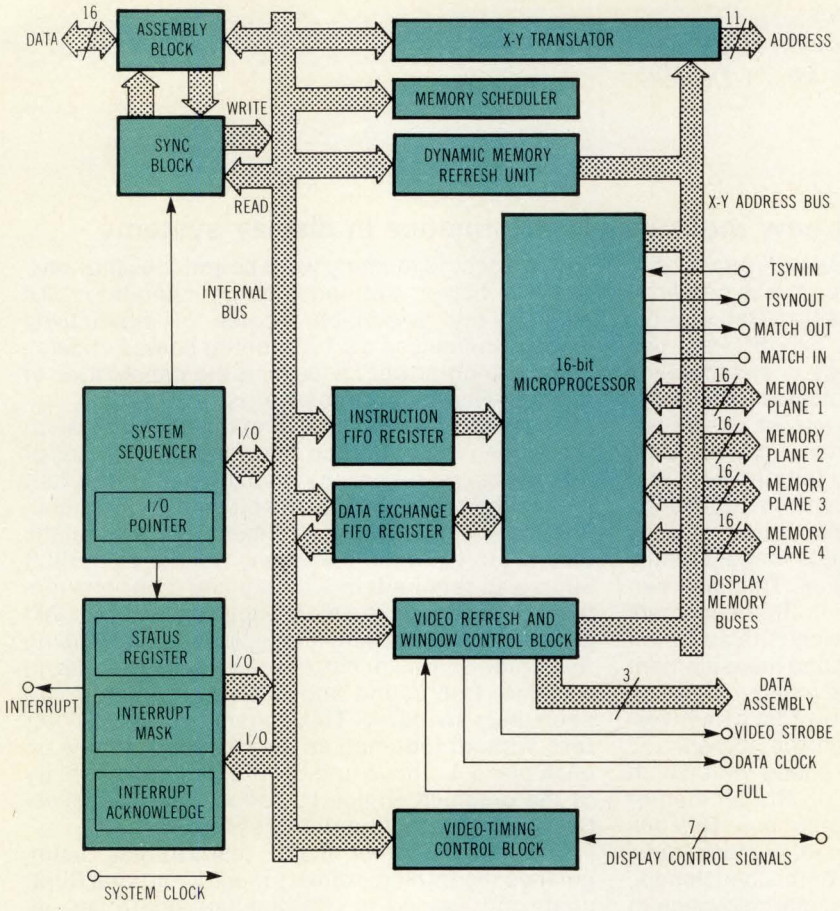
There's one other major feature that distinguishes the Bitblt primitive for text. A normal Bitblt command, issued to the graphics controller, requires many words of parameters, including source, destination and Bitblt size. This rapidly blows up the size of the text file with respect to the size of an alphanumeric text file (only 1 byte per character).

A more compact solution is to embed the Bitblt commands in a table, adjacent to the font patterns. This table is then indexed by the value of a single-word text command supplied to the controller. Using a table-driven structure such as this provides all the advantages of bit-mapped text with the compactness of an alphanumeric representation.

The other major generic use of a Bitblt function is windows—the latter being defined as a set of separate processes all viewed in a single display system. In the hardware window approach, the display processor, which selects areas of the bit map for display on the screen, jumps around in the bit map and displays noncontiguous memory areas, or windows, overlayed on the bit map.

The software window approach actually transfers the noncontiguous areas into a 1:1 bit-mapped representation of the screen. The display processor then outputs the bit map to the screen as one contiguous array of pixels.

The availability of a fast Bitblt today allows the user to implement unrestricted windows in Bitblt via software. As a result, a tremendous growth in the popularity of software Bitblt windows is predicted as the silicon horsepower becomes available.



Each AMD Am95C60 Quad Pixel Dataflow Manager (QPDM) is equipped with four 16-bit buses to address four display memory planes in parallel. Each also incorporates control circuitry for dual-port video RAMs and video control signals. The match-in and match-out signals allow multiple QPDMs to work together.

Problems in managing bit-mapped display memories arise when each pixel is defined by multiple bits to specify color or gray values in a monochrome display. The traditional approach has been to organize such memories in planes where each plane corresponds to a bit in the mapped pixel. Architecturally, this approach is at odds with the design of a microprocessor which accesses bits as part of a word, and a graphics system which often needs to access and change a single bit in a pixel. To handle these pixel bit changes, a conventional processor must first select a plane corresponding to the bit to be changed, access the word (either 8 or 16 bits within that plane) and perform a read/modify/write. If two bits within that pixel need to be changed, two such operations are necessary. If the processor can't perform these operations within the time constraints of the video refresh rate, an intermediate color will appear as an artifact on the screen.

The increased resolution of graphics displays and the increasing number of colors, however, has made it impossible for processors to modify multiple bits in a pixel by sequentially accessing each memory plane within the time needed for flicker-free display. Higher resolution means more pixels to process but less time in which to do the processing. One way around this limitation, adopted by National Semiconductor (Santa Clara, CA) and Advanced Micro Devices (Sunnyvale, CA), is to process bit planes in parallel. Such parallel processing, however, means that hardware must be dedicated to the task. This approach imposes a cost penalty in terms of chip count, pin count, board real estate and power consumption, but the payoff is a constant pixel-processing rate for any selected pixel depth.

The Am95C60 Quad Pixel Dataflow Manager (QPDM) from Advanced Micro Devices is oriented toward accessing four bit planes in parallel. As a processor, the QPDM is designed to address a 16-bit word. But it's equipped with four 16-bit buses (64 pins) so that it addresses four 16-bit words in parallel, which corresponds to 16 4-bit pixels, on each memory access. Multiple QPDMs can be cascaded to handle 8-, 12- and 16-bit pixels, and beyond.

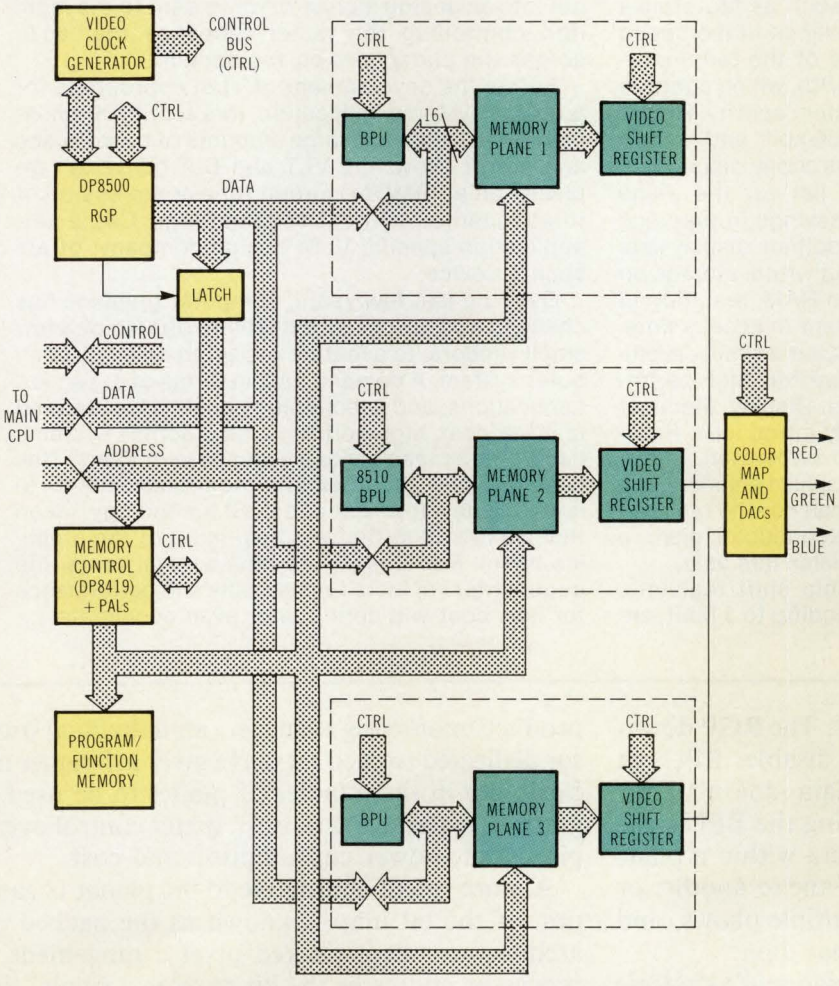
With this architecture, a bit map-update function, such as a block move, is tied directly to the access-

ing and processing speed of the QPDM and not to the pixel bit depth. A particular read/modify/write operation might require 800 ns for a 16-bit word, or 50 ns per pixel, no matter how many bits per pixel are involved in the operation.

Masking and other logical operations are done within each QPDM but are coordinated among multiple QPDMs by a pair of synch lines on each device. If two QPDMs are programmed to search for an edge color in a fill operation, each would have four bits of that 8-bit color definition in corresponding registers. Even if one of the QPDMs finds its 4-bit match, it doesn't mean that the actual 8-bit edge color has been found. Two synch pins, however, TSYNOUT and TSYNIN, let multiple QPDMs stray slightly and then reach a breakpoint in their microcode where they synchronize and compare match flags, MATOUT and MATIN.

In this color search operation, one QPDM might find its four bits, set its match flag and check to see if the second QPDM has a match at the same location. If not, the two set off again. When they are both at the same location, and both match flags agree, the edge color has been found. According to Steve Dines, director of strategic marketing for AMD's logic products division, loops and routines have been built into the microcode so that multiple QPDMs, which would be operating independently on different sets of four bit planes, could stray apart slightly in their timing and then reach a point where they would synchronize again.

The DP8500 Raster Graphics Processor (RGP) from National Semiconductor is also designed to access pixels in parallel. Unlike AMD, however, National has dedicated a separate subprocessor, the DP8510 Bitblt Processing Unit (BPU) to each bit plane. A DP8510 BPU can act as a slave to either the DP8500 RGP or to a general-purpose microprocessor. The BPU includes a control register for storing commands, a barrel shifter for aligning pixels on bit boundaries and a logic unit for Bitblt operations. A single RGP can directly control up to eight BPUs. Buffers are needed to control a larger number of BPUs, but if they're added, any number of BPUs



In a high-end system using the National Semiconductor DP8500 family, the DP8500 Raster Graphics Processor (RGP) would coordinate the operation of a Bitblt processing unit (BPU) for each memory plane. Since the BPUs are oriented toward 16-bit words, each access can perform operations on 16 pixels simultaneously.

Jack McCarthy
Vice President of Marketing
Genisco Computers

The impact of VLSI on the graphics industry

Perhaps no industry has seen more rapid growth over the last few years than that of computer graphics and computing systems using graphics. The fuel for this growth has been provided by a convergence of trends in hardware and software technology and user requirements.

The classical graphics system consists of five major components: the host (where the application program is resident), display list processor (which commands what is drawn), graphics engine (a special-purpose drawing processor), bit planes (for storage of the image to be drawn) and video processor (to display the image on a monitor). Each of these components has experienced major changes over the last few years which should continue in the foreseeable future. These changes have affected the design process, resulting in more powerful graphics systems, on less board space, at lower cost.

The 32-bit microprocessor, such as Motorola's 68000, marked a significant advance in the speed and versatility of the front end of the terminal—the graphics processing unit (GPU), which controls and supervises the graphics system activity. Higher density dynamic RAMs of 256-kbit and 1-Mbit capacities have resulted in a less costly display list, or (in practice) more display list for the same amount of money, along with savings in precious printed circuit board space. In addition, display lists of a size which formerly required virtual storage on disk can now be held entirely in RAM, resulting in orders-of-magnitude improvement in access time.

Graphics engines have witnessed a similar evolution. For example, a new powerful, high-performance device, the Quad Pixel Display Manager (QPDM) from AMD, was recently introduced. Previously, much microcode had to be written, implemented and debugged for the graphics engine. From a third to a half of that function can now be replaced with the QPDM. National Semiconductor plans a similarly powerful component later this year.

Dual-port VRAMs with on-chip shift registers, from 64 kbits to 256 kbits, expanding to 1 Mbit, are being used to store the large amounts of data that results in highly sophisticated graphics manipulations. For example, a 64-kbit VRAM, which requires three passes for orienting three-dimensional movements can now be replaced with a 256-kbit VRAM which performs the same function in one pass. With devices such as the TI TMS4161 64-kbit VRAM, vector drawing speeds of under 350 ns per pixel (effectively the raw access speed of the memory circuit) are possible. Conventional RAM devices, which are design-intensive, could require twice the time.

The video processor, or back end of the system, contains the video lookup table (VLT) and digital-to-analog converter. The bit patterns from the bit plane section enter the VLT for determination of the color for a specific pixel location on the monitor screen. The D-A comverter converts the digital output into an analog signal, which is sent to the monitor, controlling the raster refreshes that scan across the phosphors on the screen.

Before the development of VLSI appropriate for graphics systems application, this section required extensive design and large amounts of board space and power. Now, the VLT and D-A converter are placed on a RAMDAC circuit for a compression of three to tenfold. Brooktree (San Diego, CA), a new application-specific VLSI design company, offers such a device.

Over the last few years, computer graphics has changed from a specialized feature offered by a few small vendors, to a feature expected on every computer system. A demand pull, in terms of expanded applications, and a technology push, have resulted in lower cost, high-performance graphics systems becoming accessible to a wider base of users. This push and pull, together with the broader trends in software development and VLSI technology, mean that we're still at the very beginning of the graphics boom. For at least the next several years, the current trend of more functionality and performance for less cost will continue or even accelerate.

can be controlled by a single RGP. The RGP downloads commands and enables or disables BPUs as needed, but the actual pixel data doesn't flow through the RGP. By commanding the BPUs, the RGP can cause them to move data within a plane or planes, move data from one plane to another or move data from one plane to multiple planes, and perform logical operations on that data.

According to Lauren Schlicht, National's strategic products marketing manager, an individual processor dedicated to each bit plane gives a designer more flexibility in the number of planes to be used in a graphics system, and in turn, better control over the pin count, power consumption and cost.

A more recent alternative to the planar organization of the bit map is known as the packed pixel architecture. In a packed pixel arrangement, the processor addresses the bit map as a single, linear

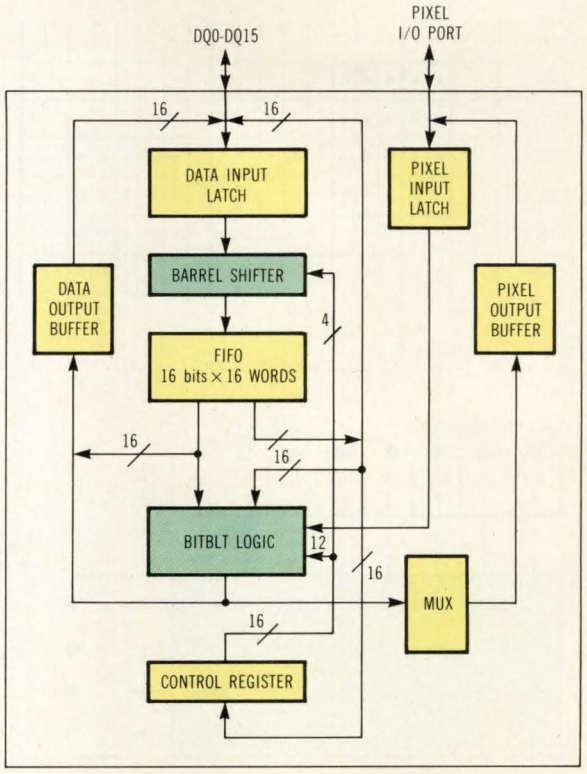
address space, rather than as an address space multiplied by some number of bit planes. The number of possible bits per pixel is essentially limited to the number of bits in the processor's data word size. A 16-bit processor, therefore, could be programmed to address a bit map with 16 bits/pixel. Any combination of bits in a pixel could be changed with one read/modify/write operation. The 16-bit data word could be set to contain two 8-bit pixels, four 4-bit pixels and so on. The rate at which read/modify/write operations could be performed on pixel data would vary with the number of bits defined per pixel, but would have a practical limit determined by the size of the data word. The packed pixel approach is especially attractive in 32-bit architectures because it offers fast pixel processing for a specific pixel depth along with a much lower pin and package count than a parallel approach.

The two principal players in the packed pixel arena are Texas Instruments (Dallas, TX) and Motorola (Phoenix, AZ). TI recently introduced the TMS34010 graphics system processor (GSP), a full 32-bit microprocessor specifically tailored for graphics that includes display memory and video control circuitry. Motorola claims that customer feedback indicates that sufficient graphics performance (at least for Motorola's targeted markets) can be obtained from the 16.67- and 20-MHz versions of the 68020 now becoming available and from faster versions expected in the near future. Intel (Santa Clara, CA) is reportedly close to announcing a graphics processor, the 82786, that also will use a packed pixel approach.

TI and Motorola rely on the 32-bit word size and high clock speed (the TMS34010 runs at an equivalent of about 25 MHz) to handle the pixel data. Motorola's advanced components product manager, Jim Lovegrove, says that some users of the 68020 are still configuring their display memory as planes using dual-port video RAMs and interface logic. "The processor must then address words in different planes sequentially, but in present applications, it seems fast enough to do this without creating color artifacts on the screen," he claims.

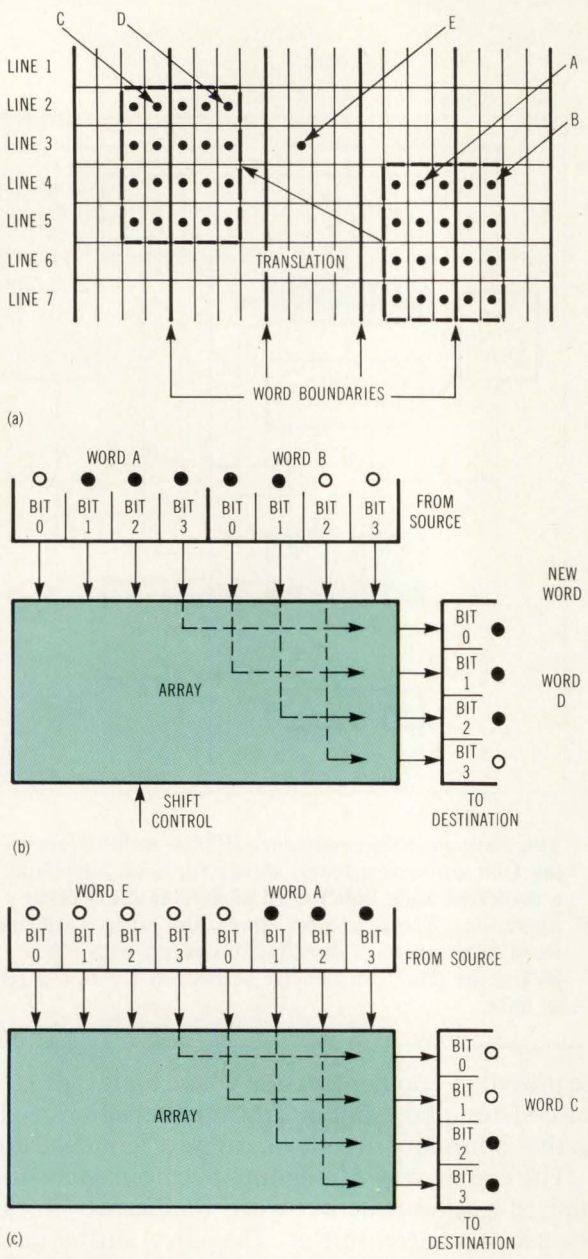
Bitblt—a yardstick for performance

Whatever memory organization, internal architecture or speed that a graphics processor has, it must be able to move patterns of bits rapidly around within the bit map and perform logical operations on them. Schemes have been developed to shift bits both within words and across the word boundaries generally recognized by microprocessors with a minimum of overhead. This is especially important when a pattern of bits that spans a word boundary must be moved to another location where it may also cross a word boundary, but in a different position relative to that boundary than it was in its original location.



The National Semiconductor DP8510 Bitblt Processing Unit contains a barrel shifter for each plane and a dedicated logic unit for all 16 conventional raster operations. The pixel port allows any bit in a selected word to be accessed directly. In concert with other BPUs, the RGP can directly access any random pixel as data.

The classic way of aligning pixel bits is to fit the desired positions across word boundaries through the use of a barrel shifter. The barrel shifter can input two words that contain a pattern spanning their boundary and output a single word containing the partial but properly positioned bit pattern for the destination word. To complete the pattern transfer, additional shifts are performed by inputting a single additional source word per shift and always shifting by the same amount. The AMD Am95C60 and TI TMS34010, for example, contain internal barrel shifters. National has placed the barrel shifter in its DP8510 BPU, dedicating a barrel shifter to each memory plane. Although the Motorola 68020 doesn't contain a specifically dedicated barrel shifter, it accomplishes the necessary operations through a set of bit field instructions that allow the extraction and insertion of any field of bits within a 32-bit word.



Moving an array of bits from one position spanning a word boundary to another which crosses a word boundary but leaves the bits in different positions in the destination words, is a common problem in Bitblt operations (a). Using 4-bit words as an example (b), source words A and B are input to the barrel shifter and shifted left one bit position. The resulting word is written to D. Next, words E and A are input to the shifter (c) using the same shift increment to produce the output word written to C. After repeating such operations for each line in the array, the array is transferred using word-oriented read/modify/writes, but can be placed at any bit position. It's also necessary to mask off the bits in the word that are not part of the array so as not to overwrite existing data in the destination word.

The bit-level manipulations of the 68020 and the TMS34010 don't require the explicit specification of a shift, and the calculations involved in working across word boundaries are done by the processor, which lets the programmer work with any desired block size. In fact, the TI GSP presents the programmer with a 32-bit, bit-addressable address scheme. In reality, the processor's memory is organized as 16-bit words. The on-chip memory controller fetches a full word and shifts to correspond with the specified bit address, but this operation is transparent to the programmer.

The National DP8510 BPU is dedicated to bit boundary alignment and logical operations and has a 16-word first-in/first-out buffer. In addition to accessing pixels as 16-bit words in a plane, the BPU has a pixel port that allows the system to pull out any particular bit within a word. When multiple BPUs are used, this allows instant access to the bits in each plane. These bits, which constitute a pixel at the specific depth of the system, can then be used as data words by the DP8500 RGP or the host processor. This feature is useful for image-processing tasks that must perform a large number of very fast operations on pixel data. The FIFO buffer is used to stage data for such things as a three-operand Bitblt, in which data might be brought in, modified with a masking word and fed back to the FIFO buffer before being written back out to the new location in the bit map.

Bitblt for text and windows

Handling text places special demands on Bitblt. The system must be able to move character arrays rapidly from the font area of the bit map to the cursor location in the display portion of the bit map and it must do so with the least possible instruction overhead for each move. At a minimum, each move requires that the processor know the source location, the offset from the last character, the block size and the destination location.

For efficiency, designers of color graphics systems like to store the character definition in only one bit plane and assign a color during the Bitblt operation. With this scheme, multiple fonts can be stored in the same general X-Y area of the bit map, but with each font in a separate bit plane. In the case of larger character sets, such as Japanese Kanji or Chinese, a very large number of characters—around 8000—can be placed in memory if their patterns are stored in only one plane per character.

For applications involving publication-quality text and graphics, Bitblt operations need to handle character cells that represent proportionally spaced characters, in which different widths are assigned

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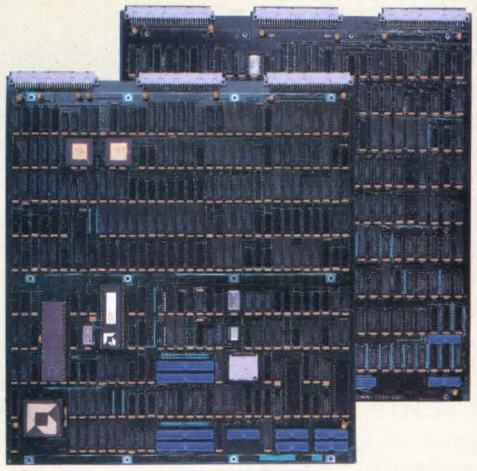

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Description: Ultra high performance, modular, multi-configurable graphics display subsystem offering an entry level workstation upgradable to fit specific application needs via the addition of MULTIBUS II circuit board modules.
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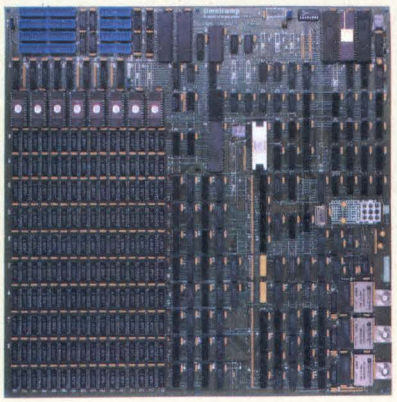


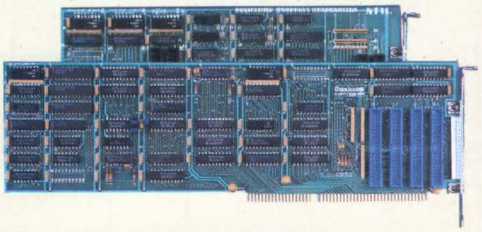
OMNI AT 1000

Description: Inexpensive, high resolution graphics plug-in board for the IBM PC/AT, supports popular application software packages such as AutoCAD, upwardly compatible to the OMNI 1000 GDC and OMNI 2000 GDS series.
Features: Dual ported video memory, display resolution is 1024 x 1024 x 8, 256 simultaneous colors from a palette of 256K, GKS compatible in C or FORTRAN libraries, and requires 2 slots in the IBM PC/AT.

See on exhibit at Computer Graphics '86 in Anaheim Booth No. 1948.

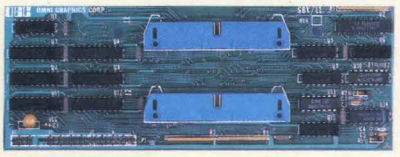
PARALLEL INTERFACE MODULES FOR IBM PC/XT/AT

Description: A 16-bit parallel interface board that provides communication between the PC or AT buses and DEC standard parallel interfaces.
Features: Parallel programmed I/O or DMA interface conforming to the following DEC interface specifications: DRVII, DRII-C, DRVII-WA, and DRII-W, transfer rates are up to 100 KByte/second on a PC/XT or up to 1.2 MByte/second on a PC/AT. Requires 1 slot in the IBM PC/XT/AT.



PARALLEL INTERFACE MODULE FOR MULTIBUS SYSTEMS

Description: A module used on any host board that supports 16-bit SBX connections as per the Intel iSBX Bus specification.
Features: Provides parallel programmed I/O interface conforming to the DEC DRVII interface specification and communicates at data rates of 100 KByte/second.



PARALLEL INTERFACE MODULE FOR VME SYSTEMS

Description: A 16-bit parallel interface board for VME systems will soon be available. Provides DEC standard parallel interfaces for VME systems.
Features: Parallel DMA interface conforming to a DRII-W and DRVII-WA interface specifications for the VME bus.

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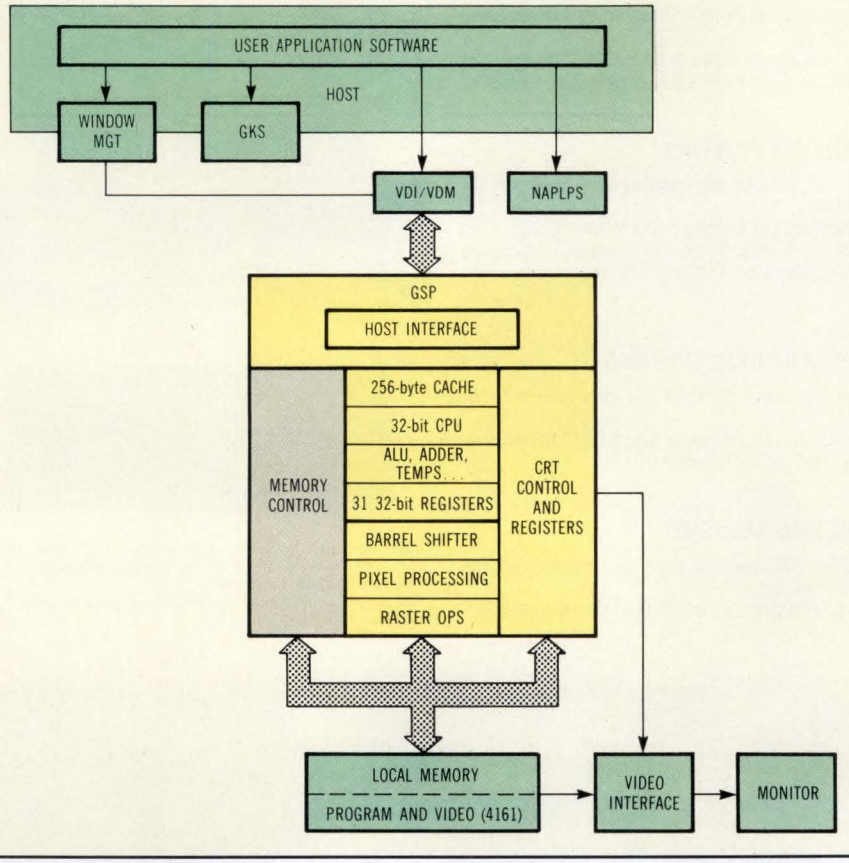
to the cell depending on the character, the character's type style and kerning. Kerning requires the definition of variable offsets and transparency so that a letter that intrudes into its neighbor's cell can "show through" the white space pixels that are written over it. As a result, the system needs to store and perform logical operations on a number of attributes for each character.

When manipulating text, it's important that the graphics processor continue to view the system as if it were an alphanumeric controller. This allows character codes (ASCII or other) to initiate the Bitblt operations that transfer text to the screen. The AMD Am95C60 QPDM, for example, recognizes that there are at least six words, plus the instruction word, for each Bitblt: the X and Y calls for the character, the X and Y sizes, and the X and Y destinations. The latter are usually the cursor locations. Rather than have the QPDM fetch and execute each instruction and its parameters from program memory, and rather than force the user to handle text with explicit Bitblt commands, the QPDM stores them in a table in the bit map. This command table is associated with the type font and is downloaded along with it when that font is selected by the system. In string mode, the processor uses character codes to point to the command table and move the text.

The National DP8500 family uses a similar scheme with an attribute table of four words per character. In addition to height and width, the table specifies an X and Y offset from the previous character. This avoids storing white space along with the character font. The offset can be proportional, or even negative in one or both axes for kerning, superscripting and subscripting. With the QPDM, the character data flows through the QPDM for barrel shifting and color assignment; with the 8500 family, it flows only through the BPU which does the shifting and can "broadcast" to other BPUs to set bits in their planes to define color.

The TI TMS34010 GSP doesn't specify a format for text handling, since it's much more of a general-purpose processor and therefore more software-oriented. It does, however, have a pixel block transfer (Pixblt) command as part of its instruction set. Its integral memory controller automatically handles X-Y-to-linear-address translation and word alignment. "The GSP's large register file [31 (32-bit) registers] allows 15 registers to be used for default parameters for commands, thus making the lookup table technique even more efficient," says Kurt Guttag, TI's graphics strategy manager. "With the internal bar-



The Texas Instruments TMS34010 graphics system processor (GSP) includes a general-purpose 32-bit microprocessor with a rich register set to run high-level languages. Instructions are tailored for Bitblt operations, and video control circuitry is included on-chip. The inclusion of a dedicated memory control unit allows address operations and computation to be done in parallel with data movement and logical operations.

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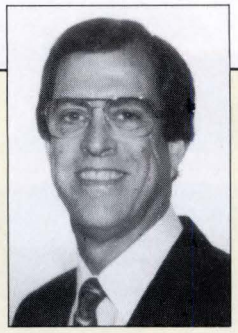

Garth Wilson
General Manager of Graphics Component Operation
Intel

Today's graphics: improving worker productivity

The ultimate goal of nearly all VLSI technology is to improve or enhance productivity of machines and workers. The automated tools used on today's factory floor depend on devices with faster processing power, higher tolerance to harsh extremes, and reliable equipment. A similar picture can be painted for the personal computer or workstation that sits atop a desk in an office. Faster microprocessors, higher resolution screens and software functions implemented in hardware have vastly impacted an office worker's productivity. Though improvements in all functions of the desktop computer continue to be made, the graphics function probably remains the area in which the most significant gains may yet be made.

One aspect of office productivity is individual productivity, which is supported by two VLSI functions. Microprocessors such as the Intel 80286 and 80386 have contributed speed and processing capabilities, which let an individual attack bigger problems with the computer system. In so doing, the implementation of application software is more rapid, or in real time, and serves to enhance worker efficiency. But without an equivalent improvement in the performance of the user interface to the application, some of the potential productivity can't be realized. As a result, a new demand is being placed on the improvement of graphics processing power to support the user interface.

Another area of office productivity combines the productivity of multiple individuals by tying islands together via a network, resulting in organizational productivity that yields a sharing of resources and communications support. With local area network products such as the Intel 82586 and 82588, the next level of productivity expands to a department, further increasing worker productivity.

A study, published in 1985, by James T. Brady of IBM analyzed the relationship between a worker's think time, entry time and the response time of the system. With entry time remaining constant and system response time cut in half by increasing speed and power, an average worker's think time would also be reduced by a factor of two. By greatly improving system response time through high-performance microprocessors and graphics coprocessors, the average worker's productivity might be increased by as much as threefold.

Improvements in hardware capabilities don't necessarily correspond to an equivalent improvement in worker ability levels, however. The more sophisticated the machine, the higher the demands for interactive tools become, mainly in the processing power of the graphics engine so that it can support the software. Applications software for such things as windowing, therefore, would best be implemented on a dedicated graphics processor to off-load the CPU from pixel-intensive operations. Visually, the performance of the graphics display on-screen will see dramatic improvement, both in display quality (colors, resolution and depth) and in display response. A key consideration for choosing a graphics device for such an application is cost. To penetrate the large, cost-conscious office systems market, a graphics IC must be cost-effective as a part of a system while still providing appropriate functions. Graphics devices that meet the needs of high-end engineering workstations, for example, would certainly provide more than the office needs—and at too-high a cost.

A second consideration is a graphics device's software compatibility within the existing applications base. To bring a new device to market cost-effectively and quickly, the product should immediately take advantage of current applications software. The software upgrade that the graphics device provides enhances the system output, and ultimately, the user's productivity.

rel shifter and microprogammed memory manager, each Pixblt is really a field-extract/field-insert operation like those of the 68020, but programmers don't need to be explicit about it. They merely specify pixel addresses and the processor does the rest."

A vast number of applications demanded a solution to the problem of mixing text and graphics. That demand was answered with Bitblt. Similarly, a consensus is arising regarding user interfaces implemented via a window environment—a consensus that may also be addressed via Bitblt techniques. Both Bitblt and the idea of accessing multiple tasks from a single screen via virtual windows into each task originated at Xerox's Palo Alto Research Center (Parc). A window interface was introduced on the Xerox Star system and has become a part of the Apple Macintosh. Window software environments have recently been produced by Microsoft (Bellevue, WA) and Digital Research (Pacific Grove, CA).

All of today's popular window environments use windows implemented by software routines, and most processor manufacturers appear to have de-

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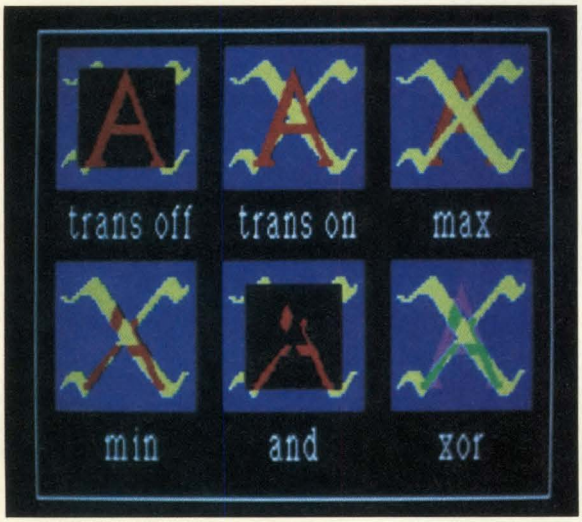
CIRCLE 36

cided that software windows will take precedence over windows supported by hardware. But software windows place heavy demands on graphics processors, namely the need for a good deal of Bitblt horsepower. Software windows simply do a Bitblt transfer of the needed window from a nondisplayed portion of the bit map into the display portion.

With hardware windows, on the other hand, the starting address of a window in the bit map is stored in the processor. When the processor comes to the point in the display area where the window starts, it jumps to a location indicated by pointers and begins shifting the data into the indicated window area. From the screen, it appears as if the window were simply a part of the displayed memory.

"Although software windows do require Bitblt power," notes AMD's Dines, "they allow greater flexibility as to position and shape and are easier to keep track of when the system is using multiple windows. But there are constraints on size and position as well as on the number of windows the software can handle without becoming unmanageable." AMD appears to have hedged its bets just a little with QPDM providing support for one hardware window.

Hardware windows are intrinsically faster since there's no need to actually move pixel data around. Hardware windows could be organized as sort of a linked list of pointers. Although details aren't yet available, only Intel appears to be planning full support of hardware windows by including a silicon window manager in its 82786 graphics processor. "You have to design well to support hardware windows." says Intel's Olson.



Pixblt operations allow various image combinations, including (clockwise from upper left) replacement with transparency on or off, maximum or minimum, and AND or exclusive OR.

One of the fundamental differences between graphics processors concerns their design philosophy: some functions should be implemented in silicon and other functions should be left to the user to program in software. It's the classic dilemma of speed versus flexibility. In each case, the processor relies on a stream of instructions from a host CPU or a specific geometry engine. These instructions (the display list) are written in terms of the processor's instruction set and once they're supplied, the processor can run the display list independently.

The instruction set for AMD's QPDM seems to be the most specifically oriented toward graphics processing, and sets of its registers are specifically oriented for video control, display configuration and window control. It's also the most dependent on an external processor. The instructions themselves execute microcoded algorithms for drawing functions such as line, arc and circle, and fill operations. Clipping, antialiasing, color search and even line style are all covered in the instruction set.

National's DP8500 RGP, on the other hand, appears to straddle the fence between the very hardware-oriented instruction set of the QPDM and the very software-oriented approach of TI's GSP. The RGP incorporates many hardware draw instructions including polygon, curve and the most widely used line drawing algorithm, the Bresenham algorithm. But the 8500 also supports moves and arithmetic functions (except divide) and uses a conventional stack in memory. It supports four addressing modes: register, immediate, absolute and stack.

The MC68020 and the TI GSP, being architecturally the most like general-purpose microprocessors, rely on software algorithms to perform their graphics functions. One architectural feature that distinguishes both processors is a 256-word on-chip instruction cache. Since a great many graphics algorithms are highly iterative and consist of relatively short loops, even so few instructions cached on-chip can contribute a great deal to speed and efficiency.

"According to Motorola's research," says Lovegrove, "20 percent of the applications involving the MC68020 are graphics applications. Recognizing that fact, the company is beginning to develop a series of development support tools to aid in graphics design tasks." The fact that compilers and general software tools already exist for the 68020 should ease the job of supplying libraries of graphics routines for the chip.

In the area of graphics-specific development support, however, TI appears to be way out in front. Software and hardware development and debugging tools now available include a full C compiler for the TMS34010, an assembler/linker, and the GSP/SIM

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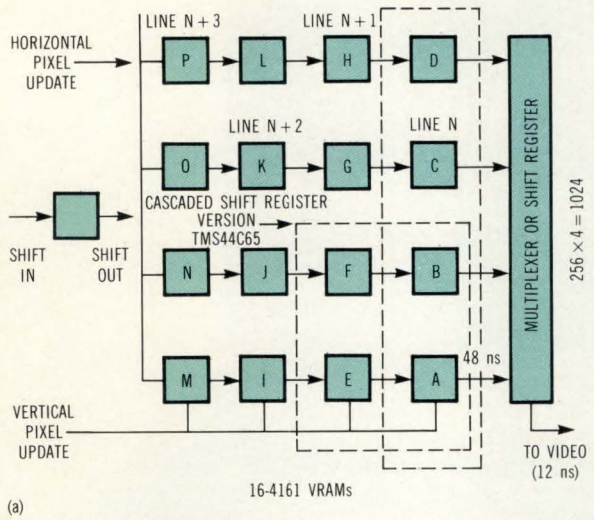

(a)

A	B	C	D	A	B	C	D	A	B	C	D
E	F	G	H	E	F	G	H	E	F	G	H
I	J	K	L	I	J	K	L	I	J	K	L
M	N	O	P	M	N	O	P	M	N	O	P
A	B	C	D	A	B	C	D	A	B	C	D
E	F	G	H	E	F	G	H	E	F	G	H
I	J	K	L	I	J	K	L	I	J	K	L
M	N	O	P	M	N	O	P	M	N	O	P

(b)

One plane of a 1024-×1024-pixel display (a) can be defined by 16 64-kbit TMS4161s (or four 256-bit TMS44C65s). Pixels, however, can be addressed in blocks of 16 (b). Each block represents 64 kbits with four 256-bit shift registers connected in series to form four 1024-bit shift registers, which correspond to four scan lines. Each time data is transferred to the serial shift registers, four complete lines are transferred in a single cycle, leaving the rest of the time for random access by the processor. If the memory is set up such that the CPU addresses one bit in each of the 16 blocks, the data it will be writing will correspond to one of the 16-×16-pixel tiles (b). Thus the letter R can be transferred to the proper location with four memory accesses instead of the eight that would be needed if memory were addressed according to horizontal lines.

PC-based software-debugging environment. In addition, TI supplies hardware-development support in the form of a debugger and PC board that allows real-time execution, breakpoints, variable video timing and the ability to select screen resolution and pixel depth. The software supplies a screen-oriented state machine presentation of linked GSP executable code, modifications of registers and memory, trace-on instruction acquisition and an on-line help utility.

TI also offers the source rights to a graphics function and font library to help systems developers start designing with the TMS34010. The function library is a set of C-callable routines including math functions, 3-D matrix operations, geometric primitives, text output and attribute functions, and viewport and rendering functions. With these, the user can build the supplied subroutine calls into an application and write any algorithms needed for proprietary applications or to optimize performance.

The system picture

The Am95C60 QPDM can execute instructions that have been stored in a nondisplayed portion of the bit map. Otherwise, it acts as a slave peripheral to the host processor and is optimized to work with the Intel iAPX family of processors, such as the 8086 and the 80286. Since multiple QPDMs would have no master/slave relationship among them, they need the CPU to control and coordinate their activities.

The host CPU can place instructions in the bit map, or the CPU can feed instructions directly to the QPDM's instruction FIFO buffer. To avoid tying up the CPU for too long, AMD recommends use of a universal DMA controller, especially when multiple QPDMs are used. The DMA controller can keep a steady stream of instructions, which have been placed in a memory area by the CPU, flowing to the QPDMs while servicing requests for one or more controllers. To read and modify contents of the bit planes, controllers must be addressed separately via chip selection logic. Instructions, however, are broadcast to all QPDMs simultaneously.

The National 8500 family uses a scheme that's similar conceptually, except that the 8500 RGP is itself the master in terms of graphics system control. Specific graphics operations, as well as general processor functionality, are concentrated in the RGP with specific control for each individual bit plane allotted to the 8510 BPUs. National's Schlicht points out that this arrangement allows a wide range of flexibility for configuring systems at different price/performance levels. Members of the 8500 family are scheduled to be introduced over the next nine months beginning with the 8515 video shift register, the 8512 clock generator and the 8510 BPU. The 8500 RGP will follow in 1987.

On the high end, one RGP can control many bit planes via individual BPUs, which can be used without the RGP but with a general-purpose microprocessor. For low-end applications, it's possible to use a microprocessor controlling one BPU that can be multiplexed between a small number of bit planes.

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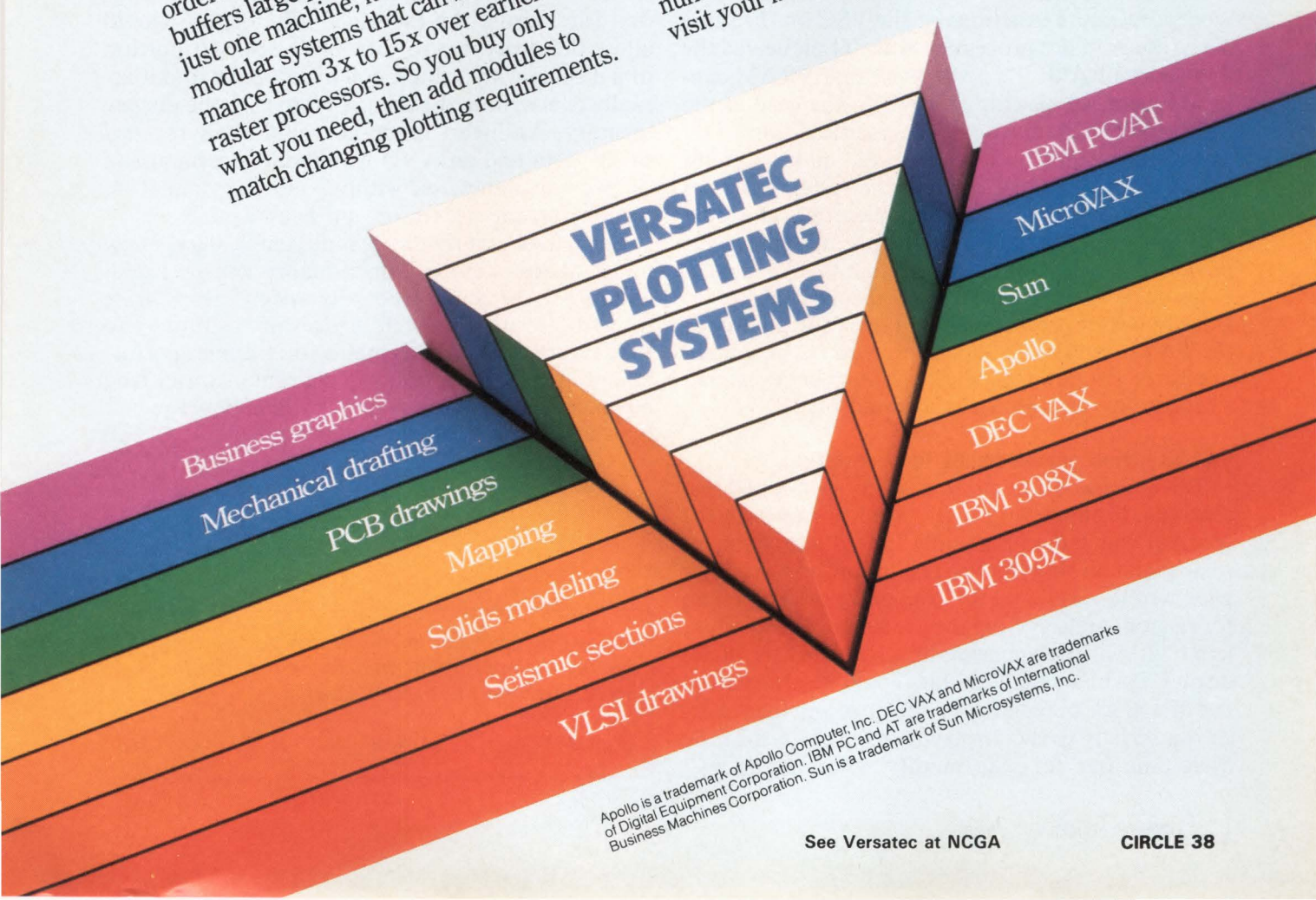

In the case of the Motorola 68020 and the TI 34010, there's no question of independence from a host CPU. While a system design may designate a master system CPU, both of these chips are full processors in their own right and can address system memory as directly as their bit map memories and, conversely, the host CPU can directly address the bit map.

The trend in graphics processors is also to integrate the video control functions, such as display timing and display memory control. The AMD Am95C60 has seven video display signals, including horizontal and vertical synch and reset, blank and a vertical odd/even pin for synchronizing interlaced display with an external device.

The National 8500 family has left both the video-timing and memory-control functions off the RGP in the interest of flexibility. As a part of the 8500 family, however, National does supply the DP8512 video clock generator (VCG). The VCG orchestrates the timing between the RGP, the frame buffer memory and a video shift register for outputting pixel data to the display. The VCG takes a a 20-MHz input signal and can multiply it internally up to 200 MHz for the pixel clock.

TI previously announced a video system controller (VSC) chip called the TMS34061. The TMS34010 incorporates the functions of the VSC on the same die as the graphics processor. Since TI pioneered the dual-port VRAM, it's no surprise that VRAM control is included on-chip as well. In the case of the Motorola 68020, although no specific display control circuits are included, Motorola makes a number of display control ICs and the system designer is free to choose from them or implement some other display-timing and control interface. In light of the power of the 68020 and the availability of support chips such as Motorola's 6845 display controller, Isaac Shearson, co-founder and scientific advisor to the TAT Graphics Group (Sunnyvale, CA), a manufacturer of desktop workstations, believes that "Motorola's decision was a sound one."

VRAMs—from enhancement to necessity

The amount of memory used in bit-mapped systems has brought with it the need to optimize the speed at which data is serially shifted out of the bit map to the display (higher resolutions mean higher pixel-writing rates) and the availability of the bit map for random updates from the processor. The solution, from TI, was the inclusion of a shift register in the display RAM so that 256 bits could be transferred out of a block of memory in one cycle and then shifted out serially to the display, leaving the rest of the cycle time free for read/modify/write operations.

As video memory densities increase, architectural techniques are being used to match the RAMs to the needs of the graphics system. For instance, the present generation of 256-kbit VRAMs from TI (TMS44C65), AMD (Am90C64), Fujitsu (MB81461) and Hitachi (HM53462) are organized as 64k × 4 bits. Each 64-kbit block has an associated 256-bit shift register. In addition, the RAMs have a serial-in capability so that blocks can be cascaded. This not only allows a longer shift register and thus a greater percentage of time available for random access, but it allows more efficient mapping or tiling of memory accesses for common operations such as Bitblt. Tiling would mean that the processor could address memory for read/modify/writes in terms of blocks that correspond more to adjacent pixel locations than linear addresses that correspond more to the scan lines.

The Hitachi HM53462, which like others of its class is organized as four 64-kbit blocks with 256-bit shift registers, is capable of performing certain logic functions formerly assigned to the graphics processor. During the falling edge of row address strobe, the processor can set a logic function in the VRAM's on-chip logic unit by accessing the first four address lines. This allows automatic logic operation on external data and data already contained in the memory cells. Using the exclusive OR function would allow the processor to turn off a selected portion of a display with a single command and without actually overwriting the data contained in the display memory. An invert function would allow reversal of the data and an AND would allow comparison of two bit planes, all without moving data from memory to the processor and back again.

The design community will ultimately decide how much of this kind of functionality will be useful within VRAM chips, especially as densities migrate toward 1 Mbit. But such devices are testimony to the fact that the large demand for graphics performance at acceptable cost will spur innovation. And advances in VLSI for graphics will encourage better and more productive applications. **CD**

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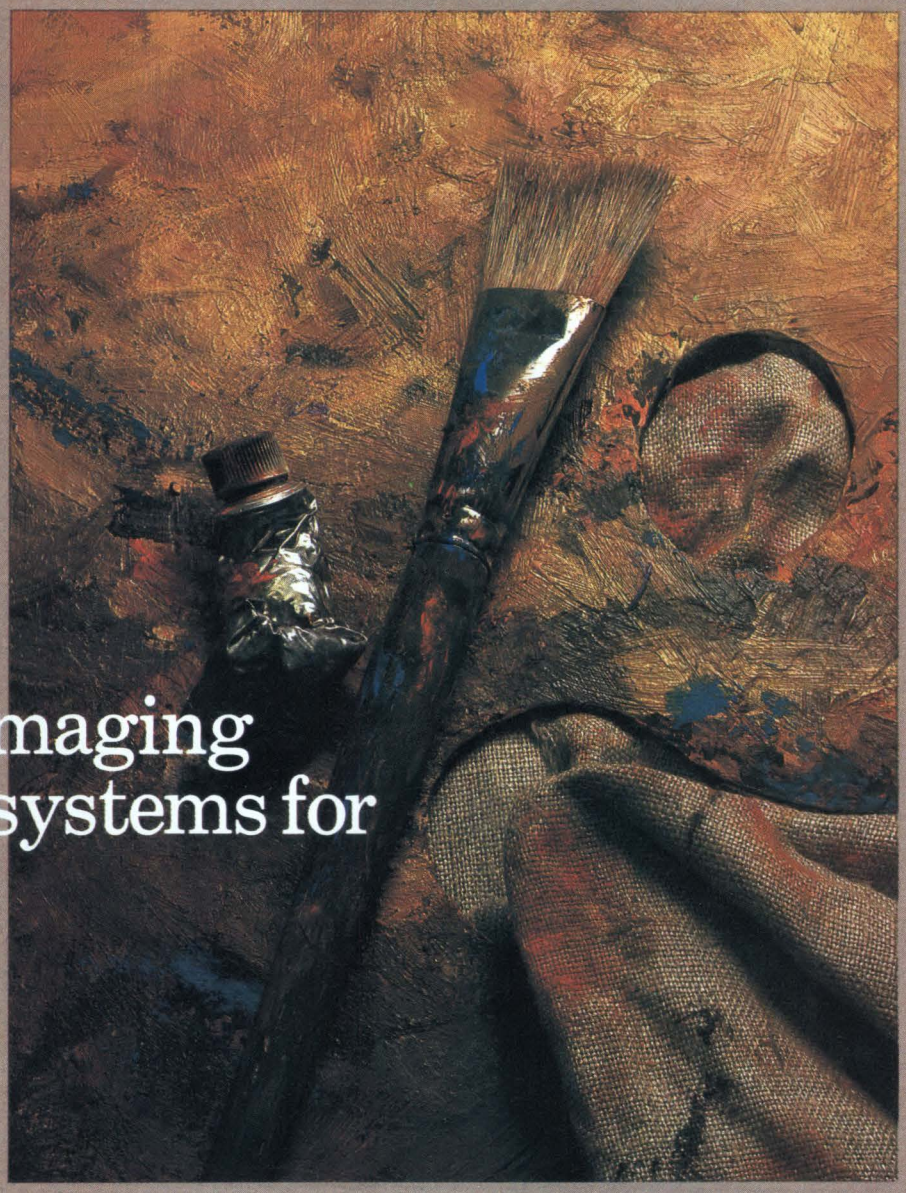

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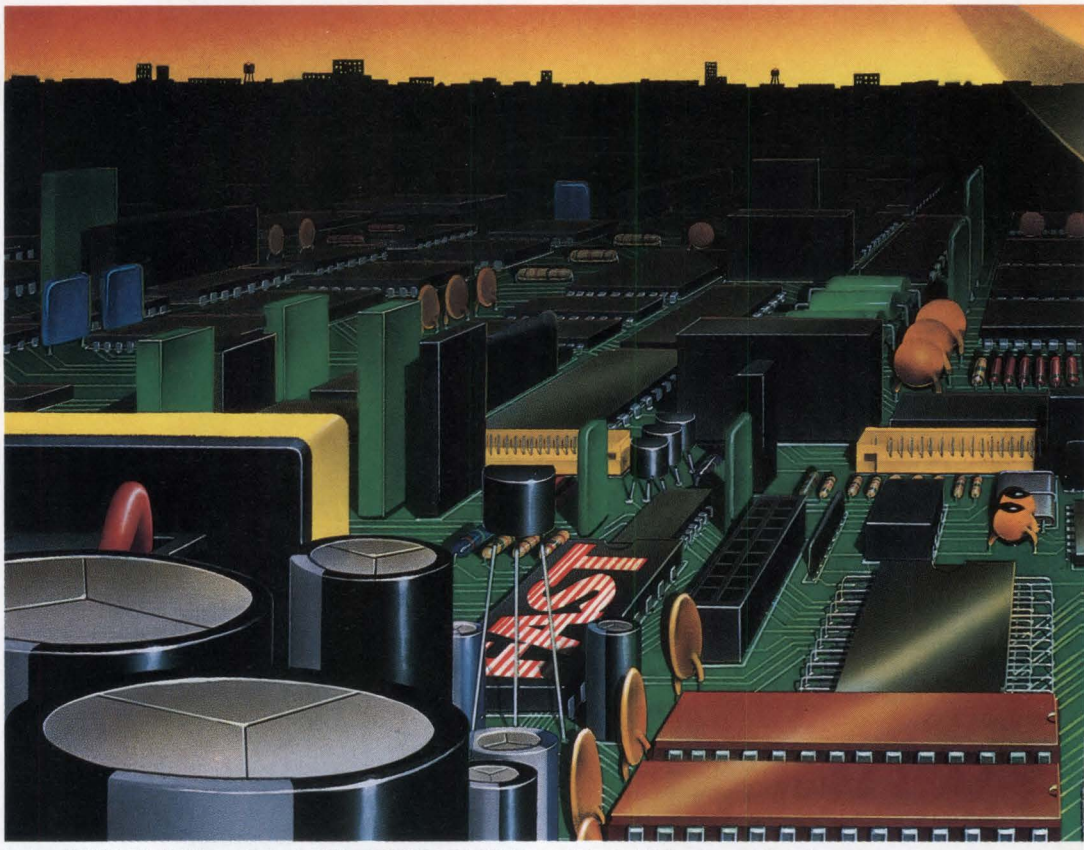

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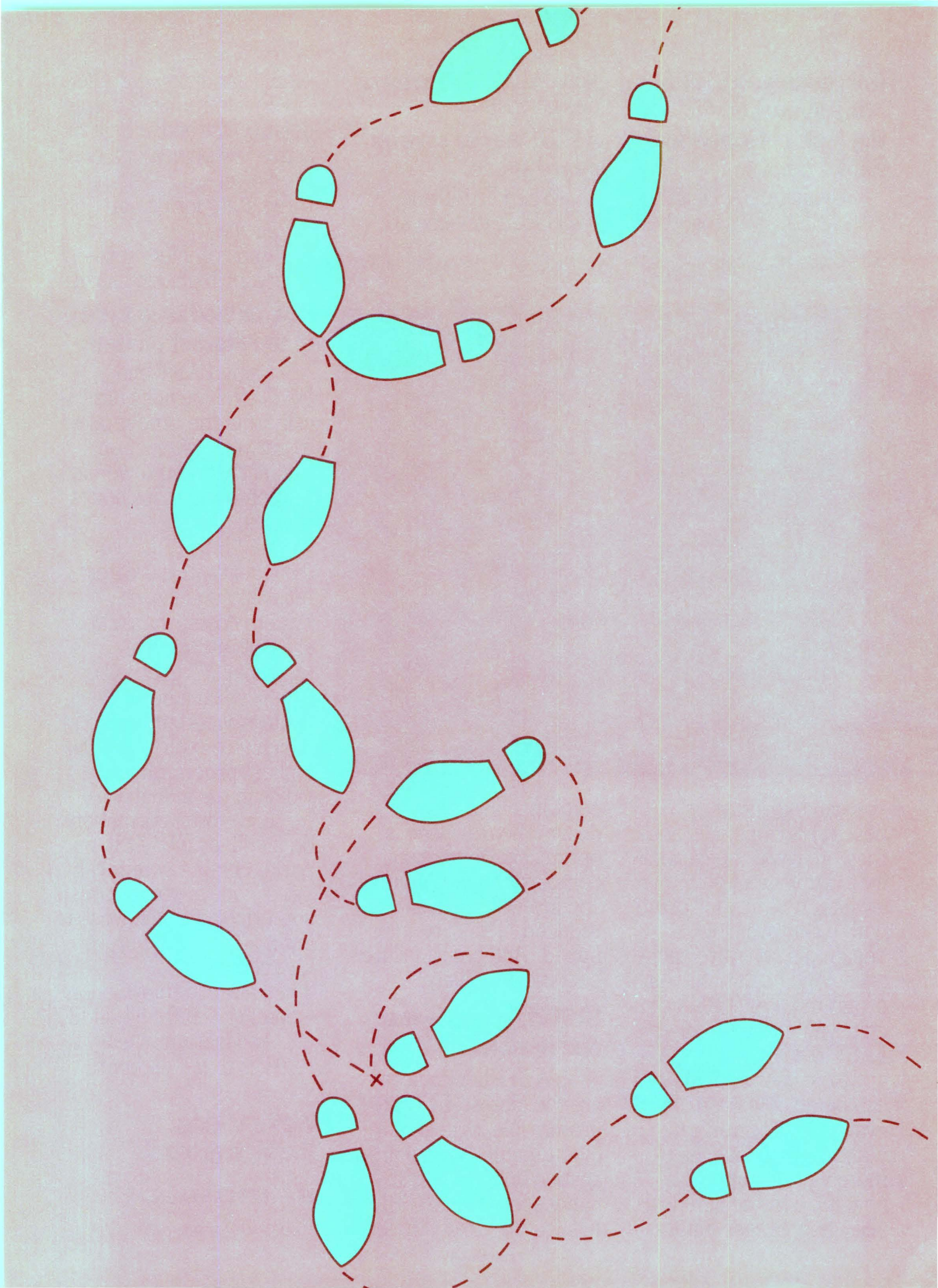

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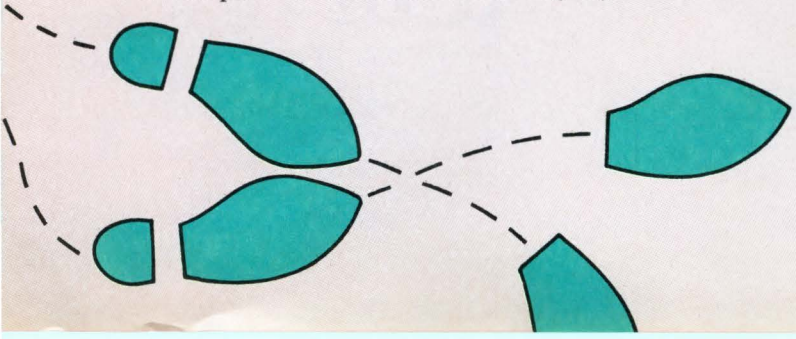

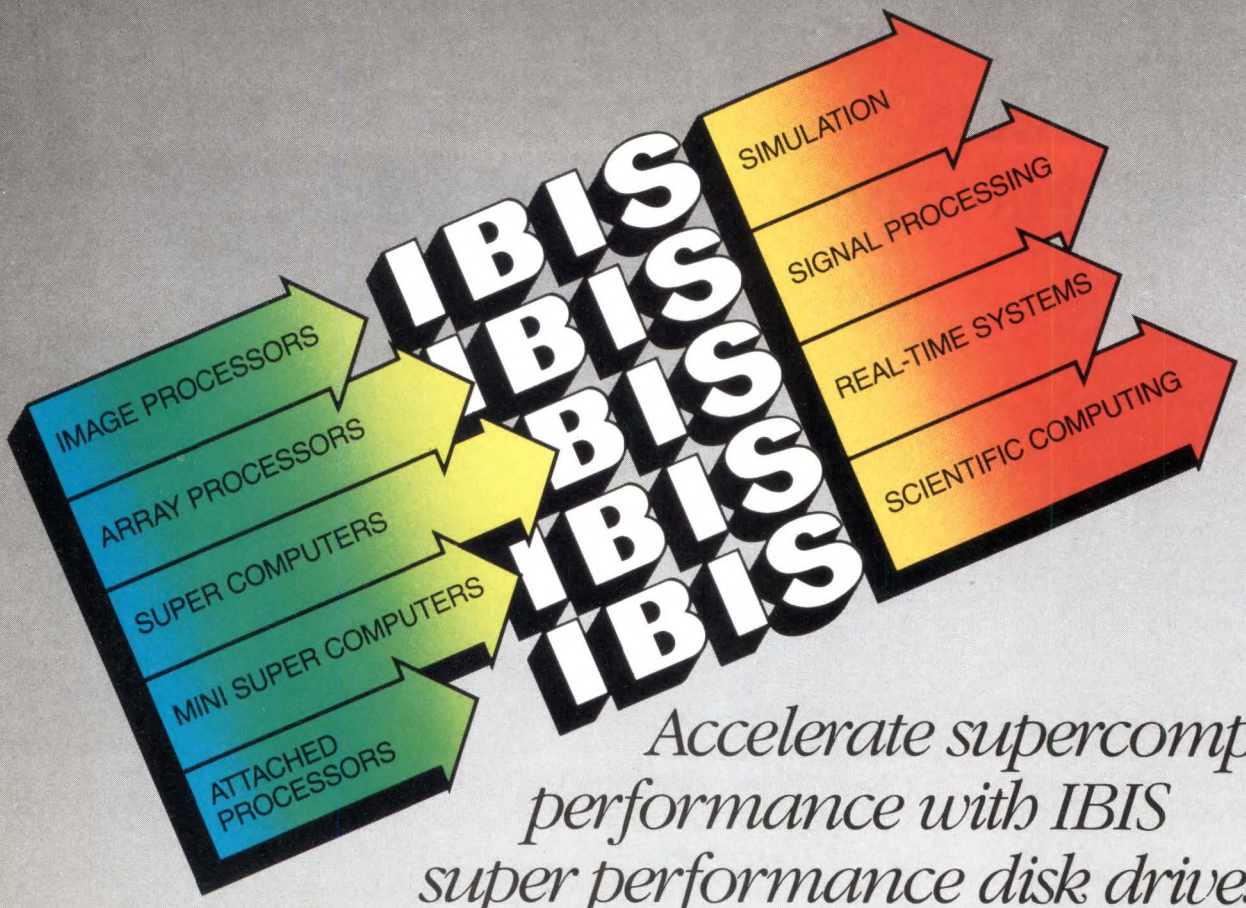

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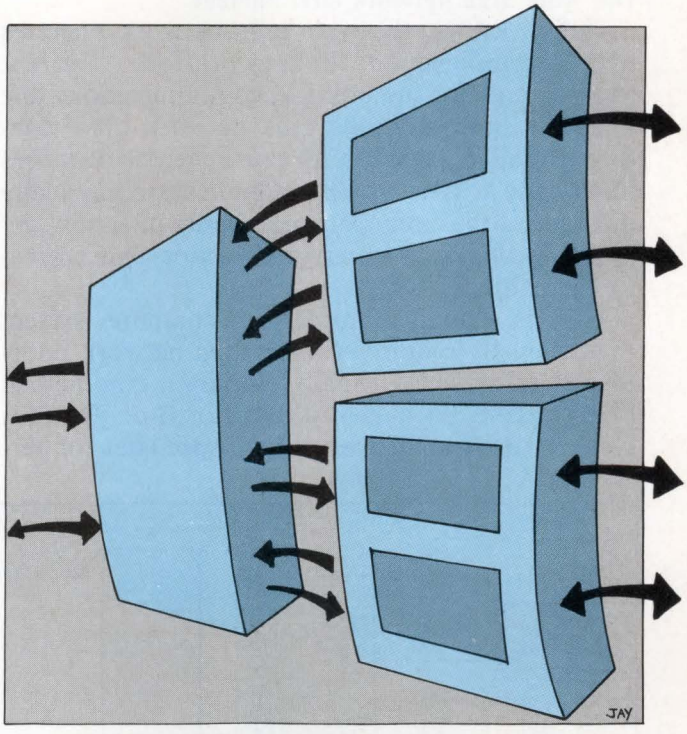
CIRCLE 42

Communications board speeds network integration

To interface a wide area network to a host computer quickly, a communications board should distribute intelligence among several devices and have an embedded software platform to reduce software development time.

Growing portions of the high-end microcomputer and minicomputer markets demand wide-area communications capability. A few years ago, only dedicated minicomputers and mainframes needed such capabilities. But the ability to meet the protocol and speed requirements for various wide area networks has become increasingly important to computer users. Today, users must connect a variety of smaller systems to wide area networks, including personal computers, multiuser office computers, CAE/CAD workstations and supermicrocomputers. This implementation of a large variety of small systems has also brought about the need for a single computer to be compatible with multiple wide area networks.

The fastest way to integrate a wide area network interface to a host computer is to add a board with communications capabilities and an embedded software platform to reduce software development time. Using a specialized communications board helps designers avoid the pitfalls of throwing general-purpose microprocessor boards at wide area network communications problems. The communications section of a computer requires excellent data communications capabilities, not just data processing capabilities. The role of the communications board is to alleviate the host CPU from time-consuming data movement tasks. One way for the communications board to meet these requirements is to distribute intelligence among specialized peripheral processors.



The Systech DCP-8804 is a good example of a board that provides both the necessary distributed intelligence and the embedded software platform. This board splits the wide area network interface

Bernard Lafreniere

Lafreniere is vice president of engineering at Systech (San Diego, CA). He received an AS in computer science from the San Diego College of Engineering.

among three intelligent devices—the serial communications controller, a DMA controller and a general-purpose microprocessor. This distributed intelligence scheme lets the communications processor interface with a wide area network with minimum impact on host performance. And the embedded software platform lets the OEM develop software to interface to a specific communications application.

Like their local area network cousins, wide area networks require strictly defined protocols for data transfer. Layers of hardware and software are used to define the network protocol conceptually. The physical data transmissions medium is considered the lowest layer. The next layers control the data bit-passing and the conversion to useful bytes of data. The top layers include application programs and operating systems. Wide area network controllers address the layers associated with the telecommunications line interface and the layers where meaning is attached to data.

The wide area network environment

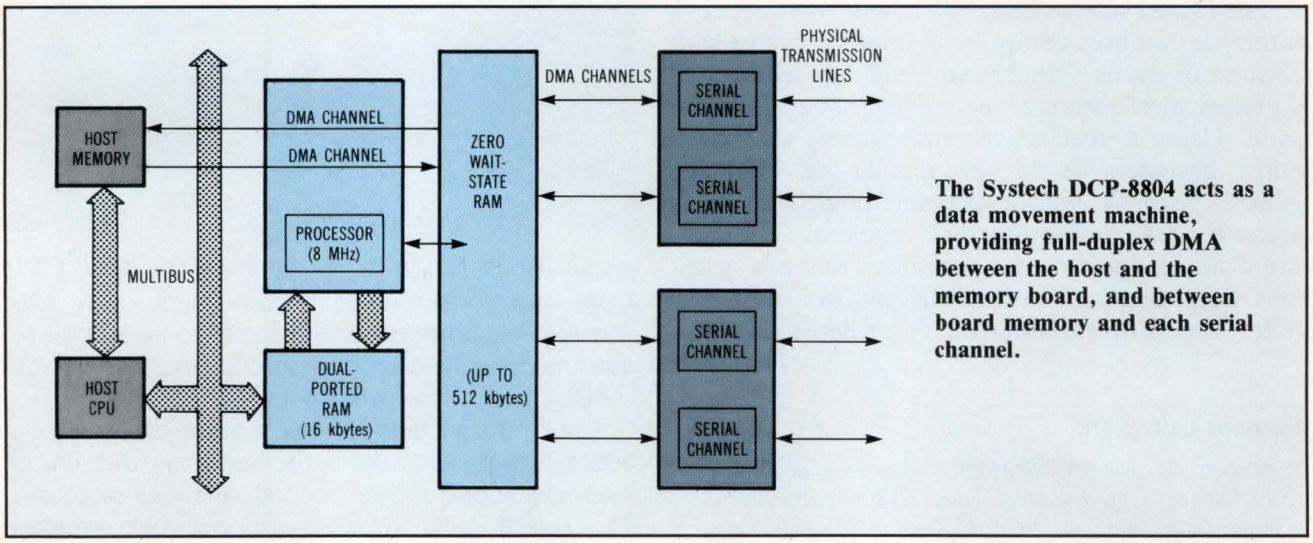
Unlike LANs, the wide area network operates over communications links worldwide. Current technologies for the physical communications line limit the practical wide area network data rates to well under 1 Mbit/s. Because greater distances make wide area network communication physically difficult, wide area network communication demands protocols with error detection and correction capabilities.

Unix is a good example of a computer system that typically requires a wide area network interface. Unix systems usually employ a commercial bus structure, such as Multibus I or II or VMEbus (with the occasional use of a high-speed bus for performance improvement). For simple low-speed, low-volume inquiries or information exchange, Unix systems can use standard RS-232C serial communications channels to provide dial-up access to remote systems. Most applications, however, require computers at remote sites to share large files and pass megabytes of information. The wide area network is the most effective way for remote computers to interchange large amounts of data.

Defining the requirements

For these large data exchanges, a specialized communications processor board must have a variety of features, including multiple communications channels and the ability to support both standard and custom protocols. The board should also support a wide range of communications speeds. It should have a straightforward architecture with distributed intelligence that satisfies wide area network requirements with minimal impact on host performance. Ideally, the sole communications duties of the host should be to complete DMA file transfers between the host's semiconductor or disk memory and the local memory of the communications processor.

In the Systech DCP-8804, the intelligence for the wide area network interface is distributed among the serial communication controller (SCC), a DMA controller and a general-purpose microprocessor. Either the SCC or the processor IC is used to interface to the wide area network. In the DCP-8804, two Zilog 8530 ICs are used as dual-channel SCCs for a board capacity of four full-duplex channels. The DCP-8804 offers DMA operation on all channels and can operate in interrupt-driven or polled operation for low-speed applications. Each 8530 channel returns unique interrupts based on user-



The Systech DCP-8804 acts as a data movement machine, providing full-duplex DMA between the host and the memory board, and between board memory and each serial channel.

defined conditions. In addition, the SCC can be programmed to modify interrupt vectors based on the status of the bits in its UART buffers.

In most wide area network applications, the SCC must operate in DMA mode. This makes a programmable DMA controller necessary to provide the link between the SCC and the memory of the local communication processor. In fact, two individual DMA channels are required for each full-duplex communication channel. The Intel 8237 (two are used in the Systech DCP-8804) provides a good example of a programmable DMA controller. It has four independent DMA channels with independent initialization of each channel.

The communications board also requires a subsystem controller to provide the host interface and act as a traffic cop. A general-purpose microprocessor usually serves as the subsystem controller. Typically, a DMA channel is required for the host interface. Processors such as the 80188 or 80186 provide both a suitable DMA link and the ability to act as system controller.

Implementing SNA

As an example of how this distributed intelligence scheme works, consider an implementation of the IBM SNA/SDLC (Systems Network Architecture/Synchronous Data Link Control) protocol for data transfer. The SDLC standard specifies the low-layer methods of interchanging raw bytes of data. The SNA portion of the protocol defines the data transfer at higher layers and associates specific meanings with the data. The communication processor handles the two portions of the data transfer protocol differently.

The intelligent SCCs provide an interface between the communication processor's DMA channels and the physical telecommunications lines. The SCC performs data conversion between the parallel data of the communications board and the serial data of the telecommunications line. In addition, the SCC interprets low-level data-transfer protocols, such as SDLC.

While the DMA controller simply serves to move data, the system-controller processor interfaces between the host and the communications hardware. The microprocessor transforms data into the required SNA transmission protocol and then formats the received data so that it can be used by the whole system.

Upper layer requirements

While the lower levels of most communications protocols have similar specifications, the higher layers vary widely from one protocol to another. The adaptability requirements vary for each intelligent device in the distributed intelligence network. For instance, because of the low-layer similarities in wide area networks, and because it merely provides a serial interface (with no meaning attached to data), the SCC may be programmed for use in any wide area network environment.

The system controller and the microprocessor, however, must be able to adapt to a wide range of wide area network environments. The system controller must have a more flexible programming environment to handle the variations in the upper level of wide area networks.

To get an idea of the microprocessor requirements, consider the example of a PDN (packet data network) wide area network environment. A PDN operates by sharing its network of leased lines and microwave links among many customers. The PDN scheme allows the costs of the communication facilities to be shared among many customers, and also provides customers with access to dissimilar remote sites. Data transfers occur in packets, and data flow is controlled by different physical transmission channels. The network has the potential to transmit some packets via leased lines and other packets via satellite.

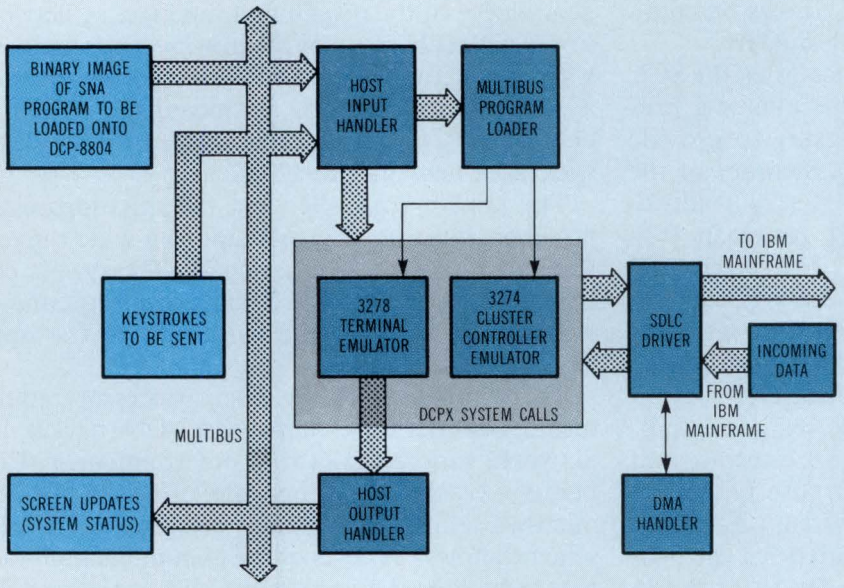
According to the protocol of a given PDN, the CPU performs a variety of duties. In most cases, the CPU must perform some type of error checking. In addition, the data packets must be assembled for transmission, and disassembled after reception. The CPU provides the interface between files for the host and the data packets for the net.

Ideally, the CPU manipulates a small amount of data. For example, since DMA channels handle the data movement, the CPU may deal solely with packet addressing information. In other cases, the processor may perform some type of protocol conversion, such as EBCDIC to ASCII.

Dynamic adaptability

In addition to compatibility with different protocols, the communication processor can function at the various speeds required by different wide area networks. The DCP-8804 implementation, using an SCC and a DMA controller, will support programmable data transmission speeds of up to 1 Mbit/s. This speed will support physical communications line limits for years to come, and can also support other standard protocols, such as 3270 or X.25 or custom protocols.

The easiest way to attain protocol adaptability is to have the host download the code required for a given wide area network interface. For example, each of the four full-duplex channels of the DCP-



The DCPX multitasking operating system provides task scheduling, message-handling, and a run-time environment for the board-level application, in this case a 3270 SNA emulator. The Host Input Handler accepts keystrokes from the host and routes them to the Terminal Emulator. DCPX also routes outbound data to the SDLC driver. Incoming data from the remote mainframe follows a similar path to the Host Output Handler, which deposits the data in host memory. DCPX provides an environment where multiple emulations and protocols can execute simultaneously.

8804 can interface with a different wide area network, and each can be dynamically reprogrammed. The key to meeting the needs of the communications processor is the software platform, which can consist of custom code or an operating system with added extensions.

The starting point for the software platform is a real-time, multitasking operating system, which provides the starting base for software development. Multitasking supports the ability to adapt to different wide area network environments and eases the implementation of different functions, such as running a separate task on each communications channel of the communications board CPU. On the DCP-8804, the DCPX real-time, multitasking operating system makes it easier to develop the code to address the communications board to a specific communications protocol. This software platform reduces development cost and saves development time.

An X.25 application

The X.25 communications environment provides a good example of a potential application for the DCP-8804. X.25 allows OEMs to provide users with the opportunity to connect to PDNs, and it defines three levels of protocols:

- X.25 L3, packet level (virtual call procedures)
- X.25 L2, frame level (link access procedures)
- X.25 L1, physical level (electrical interface)

The packet level defines procedures for handling virtual calls. The frame level specifies procedures for controlling the flow of information over the access link. The frame-level procedures include the ability to detect and correct transmission and procedural errors. The physical level defines the electrical interface between the subscriber and the network—the operation of the synchronous circuit.

The DCP-8804 X.25 package implements all three levels of the X.25 protocol on the communication processor board. The board-level software supports access to X.25 networks at line speeds of up to 64 kbaud. In addition, the software platform allows the board to support additional communications protocols simultaneously. The DCPX operating system and its extensions provide the base for software development and program execution. The operating system provides task and memory management, scheduling and intertask communication. The DCPX extensions control the serial channels, DMA channels, downloading of executable code, access to the Multibus and the host/communications processor interface.

Two built-in tasks, the host port and request completion handlers, provide the mechanism for communications between the processor-resident task and the host. The Multibus program loader task lets the host download new tasks to the board and start task execution. This task supports downloading of the executable code and configuration tables to the DCP-8804 upon power-up or reset and also during run time.

The X.25 task receives commands from the host via I/O control blocks (IOCBs). To execute the X.25 task, the host downloads and starts the task on the communication processor. When execution

starts, the X.25 task requests that the host port handler route X.25 IOCBs to the task. When the host interrupts the DCP-8804 to send it an IOCB, the host port handler analyzes the IOCB and routes it to the appropriate executing task.

Typically, the host commands result in data being interchanged between the dedicated memory of the communications board and Multibus memory that the host can access. Upon completion of the requested operation, the X.25 task sends a completion message back to the host via the request completion handler.

This handler coordinates the request completions generated by the on-board tasks with the host activities. When the host is ready, the request completion handler interrupts the host to indicate which IOCB has been completed.

The DCP-8804 X.25 package is divided into a packet-level segment and a frame-level segment. The packet-level segment of the X.25 package establishes X.25 "virtual circuits," interfacing to the host via IOCBs. This segment of the package can also place calls, accept or reject incoming calls, send and receive packets and monitor the status of the requested services.

The frame-level segment provides a means of transmitting and receiving packets on the network using defined link access procedures. In addition, the frame-level code adds address and control information to outgoing packets and analyzes that same information on incoming packets. For synchronous serial transmit or receive operations, the frame-level task must set up the DMA controllers and SCC chips. The physical level actually performs the packet transfers to and from the X.25 network. The SCC and serial line driver chips support the physical-level operations. **CD**

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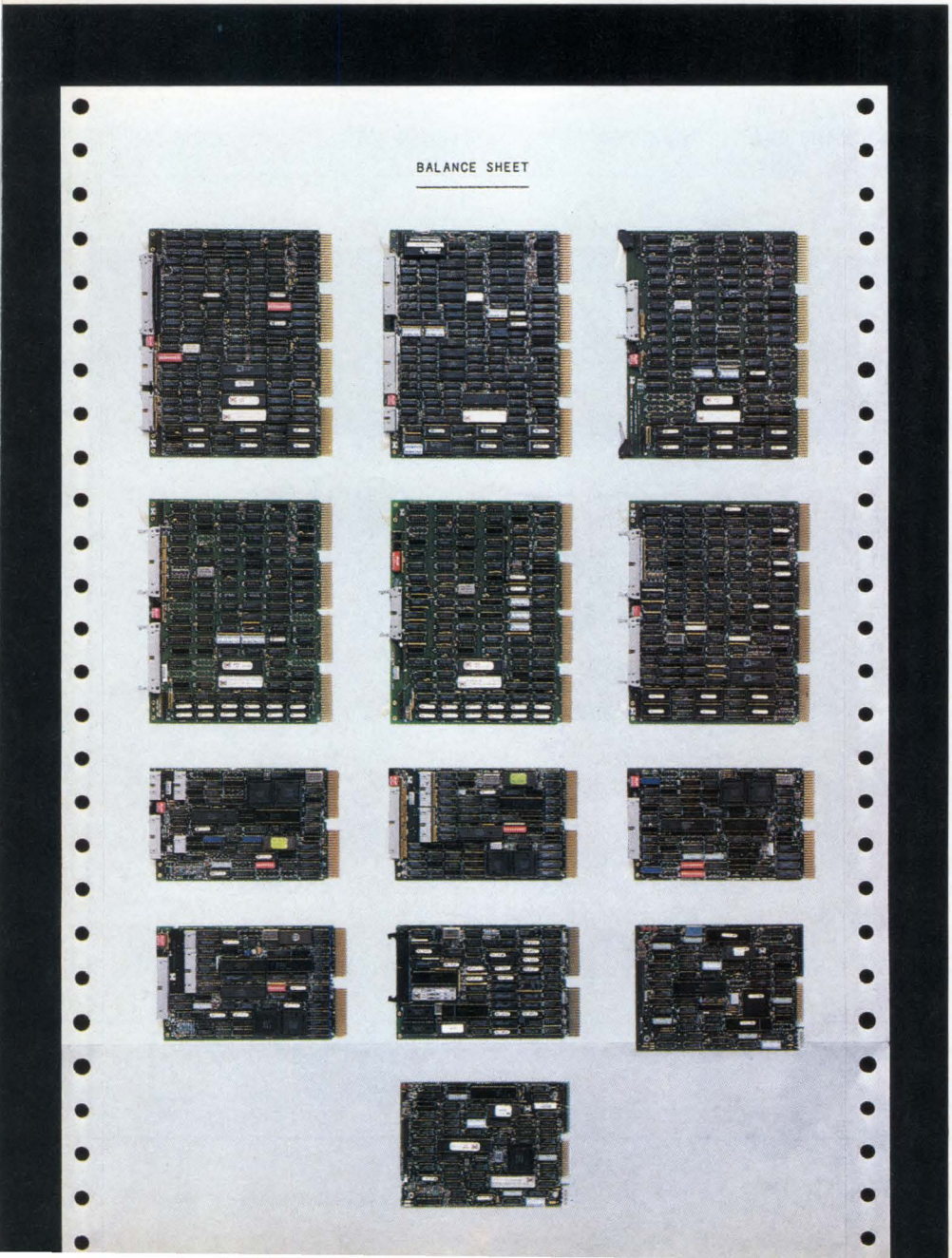

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CIRCLE 44

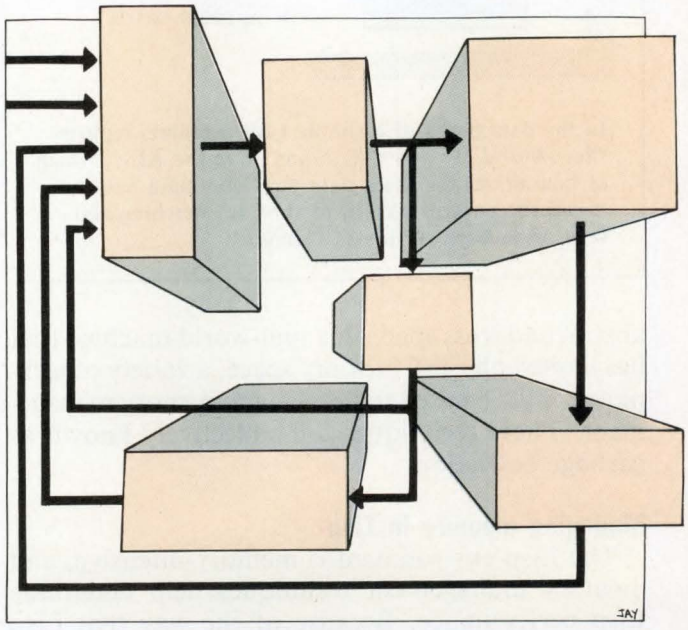
Matching hardware to Lisp yields peak performance

The Lisp environment differs significantly from conventional computing. Understanding how the software features of Lisp affect the operation of Lisp machines, gives designers an edge in choosing a high-performance workstation.

The system designer or software developer moving into symbolic processing soon finds that choosing an intelligent workstation requires a knowledge of the unique features of Lisp architecture. These features include the extensive use of multiple variables and data types, the use of garbage collectors to control data traffic, a linear address space that uses a large number of data structures, and an extended data-tagging system field.

A Lisp machine that effectively implements these features in hardware takes advantage of the idiosyncrasies of the Lisp environment. To implement the internal Lisp features, the Lisp machine must have a very large microcode memory. It must also have a variety of extra internal registers to take care of data tagging. Finally, the machine must have a dual-pointer stack to track data movement within the large abstract address.

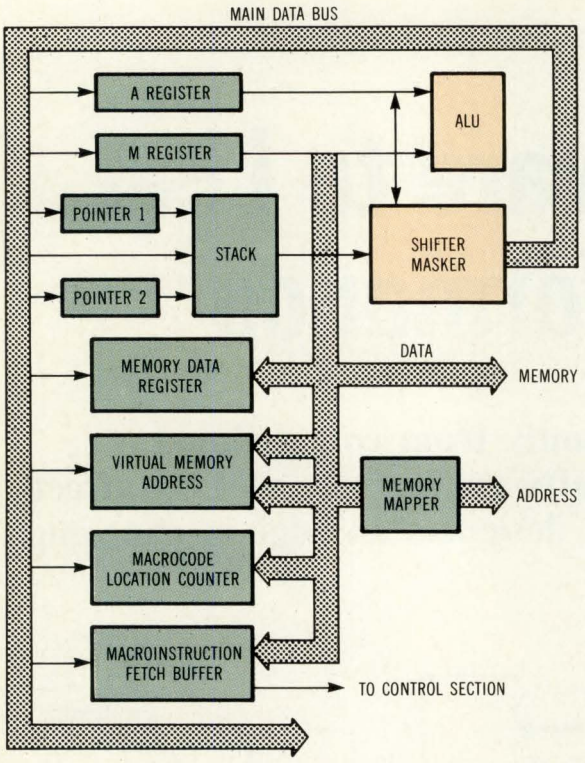
In Fortran or Pascal, a variable can hold only a single data type. In Lisp, many basic operations work for several types of data, and any variable can hold any type of data. For example, there is only one add operation in Lisp (called "PLUS" or "+"), which works for all valid numerical representations, such as fixed and floating point. Attempts to operate on invalid data types are detected and aborted with an error message. One example of an invalid operation is adding a list to an integer. Since this operation is done at run time, rather than during compilation, the hardware architecture must provide a method of carrying the data type along with the data value. This provision is not necessary for conventional architectures.



Because the programmer works symbolically in a large address space, there is less inherent concern for memory management issues in the Lisp environment. But since memory management is still required to implement the programmer's large

Gene Matthews, Glenn Manuel and Steven Krueger

Matthews is director of the Symbolic Computing Lab for Texas Instruments (Dallas, TX). Manuel is a technical contributer also for TI. Krueger is a senior member of TI's technical staff.



In the data paths of a simple Lisp machine, register files (A and M) and a data bus drive the ALU, which in turn drives the main data bus. The main data bus drives the control section of the Lisp machine and feeds data back to the ALU inputs.

abstract address space in a real-world machine that has limited physical memory space, a variety of techniques must be used to implement memory management. These techniques are collectively known as garbage collection.

Managing memory in Lisp

The Lisp environment is memory-intensive, and memory management techniques help determine Lisp performance. Because of the way that Lisp manipulates lists, for example, many small chunks of memory are used for short periods of time. A large amount of list handling can quickly fragment the Lisp machine's memory and exhaust its memory space.

To ease the handling of large lists, a Lisp system has a built-in garbage collector. Periodically, the garbage collector reclaims chunks of memory that are no longer used. In addition, most garbage collectors perform compaction. This process rearranges the blocks of data in memory, removes fragmentation and restores memory to a linear, contiguous order.

To maintain the integrity of the data structures during the compaction process, garbage collectors need to keep track of data movement so that pointers to the data can be updated. One method of tracking data is to place a pointer's new location in its old location when the pointer is moved. The old location is marked as a forwarding pointer, rather than a normal pointer. As a protective feature, any attempt to use the old location is automatically redirected to the location to which the data has been moved.

Tracking the data

When this technique is used, the pointer must be identified as a normal or forwarding pointer. In addition, the presence of forwarding pointers complicates memory access. Each time a pointer is accessed, it must be checked to see if it is a normal or forwarding pointer. Since the pointer can be either a forwarding or normal pointer, the checking process must be repeated.

If it is a forwarding pointer, the pointer must be followed to where it points. When the end of the forwarding pointer chain is reached, the original pointer which started the memory access must be updated with the final pointer value. This enables subsequent memory access to go directly to the new location, instead of going through the chain of forwarding pointers.

Since the process of checking for forwarding pointers adds to the overhead of each memory access, it must be as efficient as possible. A Lisp hardware architecture must provide support for forwarding pointers.

A linear address space is the critical feature of an efficient Lisp architecture. To provide the best possible implementation of the Lisp address space, logical memory should be as large, linear and uniform as possible. Memory address spaces with partitions imposed by logical address limitations (such as base registers and segments) complicate efficient memory management for a variety of reasons.

Overcoming management obstacles

First, because Lisp pointers are actually memory addresses, they must be extended to include the memory partition. Unfortunately, this procedure uses memory inefficiently, since pointers are longer. It also slows execution because of a more complex pointer format. The base register, for example, must be checked. It may even have to be changed for every access.

Second, symbolic processing programs tend to use large numbers of data structures. If the size of

a data structure exceeds the size of a memory partition, the data structure access will be very inefficient. Finally, since garbage collection must be done on the entire address space, the garbage collector itself can add significant overhead to program execution (depending upon the algorithm used). This problem is also aggravated by the base register changes that are required as the garbage collector moves through memory.

Tagging the data

Because of the need to reorganize memory via garbage collection, and because Lisp contains both pointers and data, data must be tagged. In a tagged data architecture, each memory word contains both the data and a tag which indicates the data type. In addition to indicating the data type, tags differentiate between pointers and actual data. Special bits in the tag may also be required for memory management to provide forwarding pointers and garbage collector status bits. These status bits indicate whether or not a word can be reclaimed.

Another requirement for Lisp implementation is a flexible architecture. Since Lisp is an interactive and dynamic language, the architecture must be easy to modify, so that it can track and support changes and extensions in the language. The key to this flexible architecture is effectively modifying the architecture in accordance with the microcode and microprogramming.

A simple Lisp machine

A Lisp machine has a very large microcode memory (typically 16 kbytes × 50 to 60 bits). In such a machine, Lisp source code is not executed directly, but is compiled down to a virtual machine code (macrocode). The microcode then interprets the macrocode. To allow interpreted execution of Lisp source code, a compiled Lisp interpreter program is always resident in the system. Many of the internal Lisp features, such as the virtual memory management and garbage collection, are implemented in microcode. Since the microcode is resident in the system, changes, extensions and modifications can be easily made.

In the data paths of a simple Lisp machine, a register file drives one input of the ALU, and the other ALU input is driven by a bus. On this bus is a second register file, stack cache, virtual memory address register, memory data register, Lisp macrocode location counter and macrocode instruction buffer. The ALU output drives the machine's main data bus. This bus feeds data back to the data path sources and to parts of the control section.

In parallel with the ALU is a shifter/masker which also drives the main data bus. Each machine instruction uses the ALU or the shifter/masker to perform its operation. To eliminate a separate tag processor, tags are implemented as the top few bits of the data word and the normal data paths are used for tag processing. The shifter/masker is added to make tag processing, which involves many bit manipulations, more efficient.

The shifter/masker consists of a barrel shifter and a full-width programmable AND gate. The barrel shifter shifts a data word any number of bits in one operation, and the masker allows any number of bits in the shifted word to be masked off. It then combines the masked word with a back-

Real world implementations

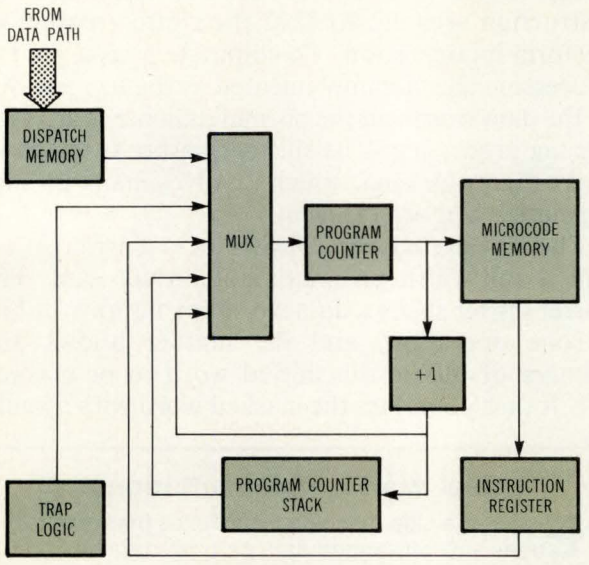
Explorer, a Lisp machine from Texas Instruments, uses a 32-bit tagged data path (25 data bits and 7 tag bits). The 25-bit pointers provide a 128-Mbyte virtual address space. Memory accesses, however, can bypass the virtual address mapping hardware, which allows full use of the 32-bit (4-Gbyte) logical address space.

The Explorer data paths use two register files, an ALU, a shifter/masker and 1-kbyte words of stack cache that include two pointers, the Lisp macrocode location counter, the memory data register, the virtual memory address register and the macrocode instruction buffer. Additional hardware improves tag processing. A tag comparator across the inputs of the ALU implements a tag equal check on the two operands of an instruction. In addition, a tag classifier RAM (instead of a dispatch memory) handles generic tag checking.

The control section features a 16-kbyte × 56-bit microcode memory, a program counter stack with a depth of 64 bits and a 4-kword dispatch memory. A 2-kword microcode PROM is used for booting and self-test. Circuitry is included to modify the instruction register of the next instruction. This design provides for dynamic instruction modification, such as one-instruction calculation and the ability to set up the shifter/masker control bits for the next instruction.

Designers investigating Lisp machines for symbolic processing will see a Lisp architecture in VLSI. Texas Instruments is developing a 2-micron CMOS generic Lisp processor architecture called Compact Lisp Machine. Although this chip will not implement the microcode memory and the memory mapper, it will include some features not in the generic architecture, such as a normalizer that improves floating-point performance.

Since Compact Lisp Machine is too fast (40-MHz clock) to be supported by standard DRAM, the data cache is accessed in parallel with the mapper. In this design, for a cache hit, the data is returned immediately, with the memory operation aborted. For a miss, the memory operation in progress is completed and memory is accessed over the Lisp machine system bus (NuBus).



The decoded outputs of the instruction register are the control signals that bring about the execution of each instruction. The program counter is selected from the previous counter (incremented), a field of the instruction register, a program counter stack, trap logic or an output of dispatch memory.

ground word. The shifter and masker perform the load byte operation, the deposit byte operation and the selective deposit operation. Load byte, which is useful for extracting a tag from a data word, replaces a specific number of the lowest bits of a word with a field of the same length. (This field can be located anywhere within another word.) Deposit byte uses this same number of lowest bits to replace the same number of bits in another word. This is useful for storing a tag with a data word.

Selective deposit replaces a field of length n in one word with the bits in the same location of another word. This is useful for copying tags from one word to another. Finally, the shifter/masker is useful in processing the data portion of the word. The result is greatly improved performance for many data operations, especially the extensive bit manipulations needed for bit-mapped graphics.

Stack aids performance

The Lisp machine is a stack machine—each call to a function causes a frame to be added to the stack. The frame contains information and storage space for that invocation of the function, including storage of local variables. When a function is executed, its frame is removed from the stack and replaced by the frame of the next function. To improve the performance of stack operations, a hardware stack cache is provided.

Two pointers are used to index the stack. One always points to the top of the stack for conventional push and pop operations. The other can point anywhere, and is useful for accessing local variables within the stack. This hardware stack is used as the top of a large memory-resident stack that is managed by the microcode.

The abstract address space of the Lisp machine is implemented as demand-paged virtual memory. Memory mapping hardware translates the CPU's virtual addresses into the memory's physical addresses. Memory access is performed independent of the CPU. This independent operation lets the CPU start a read request before it actually needs the data, nearly eliminating wait states. Lisp macrocode is contained in the virtual address space.

Maintaining control

In the control section of the basic Lisp machine, microcode memory is addressed by the program counter, and its output is latched in the instruction register. The decoded outputs of the instruction register are the control signals, which cause execution of each instruction. The program counter is selected from either the previous counter, a field of the instruction register (for jump instructions), a program counter stack (for subroutine calls or returns), a trap address generator or the output of dispatch memory.

Dispatch memory is used for macroinstruction decoding and generic operations. It contains the starting addresses of specific microcode routines. The dispatch memory address is selected from one of two sources. For example, using the macrocode instruction buffer as the source, the next macroinstruction is decoded by jumping to the microcode routine which implements it. Using the shifter/masker output as the source, the tag can cause a jump to the microcode routine for handling a particular data type (this function is used for generic operations). The shifter/masker output can also be used for other more specialized applications. **CD**

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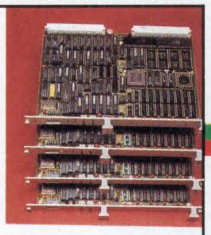

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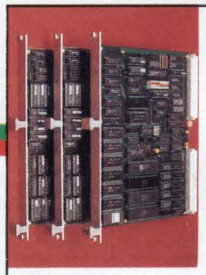

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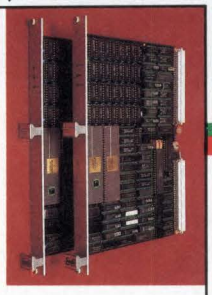

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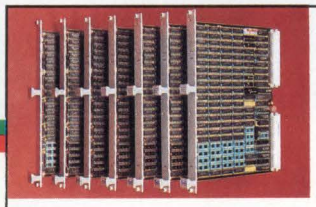
MEMORY BOARDS



MEM-3 2MB
2 Mbytes RAM
Parity
32 bit data, and address

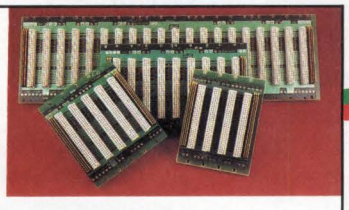
MEM-3 4MB
4 Mbytes RAM

MEM-3 6MB
6 Mbytes RAM

MEM-1
512 Kbytes RAM
Parity or Error Correction
16 bit Data, 24 bit Address

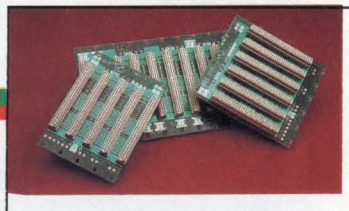
MEM-2
2 Mbytes RAM
Parity or Error Correction
16 bit Data, 24 bit Address

BACKPANELS – "A" SERIES



"A" SERIES-ON BOARD TERMINATION
Std. Product: Immediate Delivery
P1-4, 5, 9 & 20 Slots
P2-5, 9 & 20 Slots

BACK PANELS – "R" SERIES



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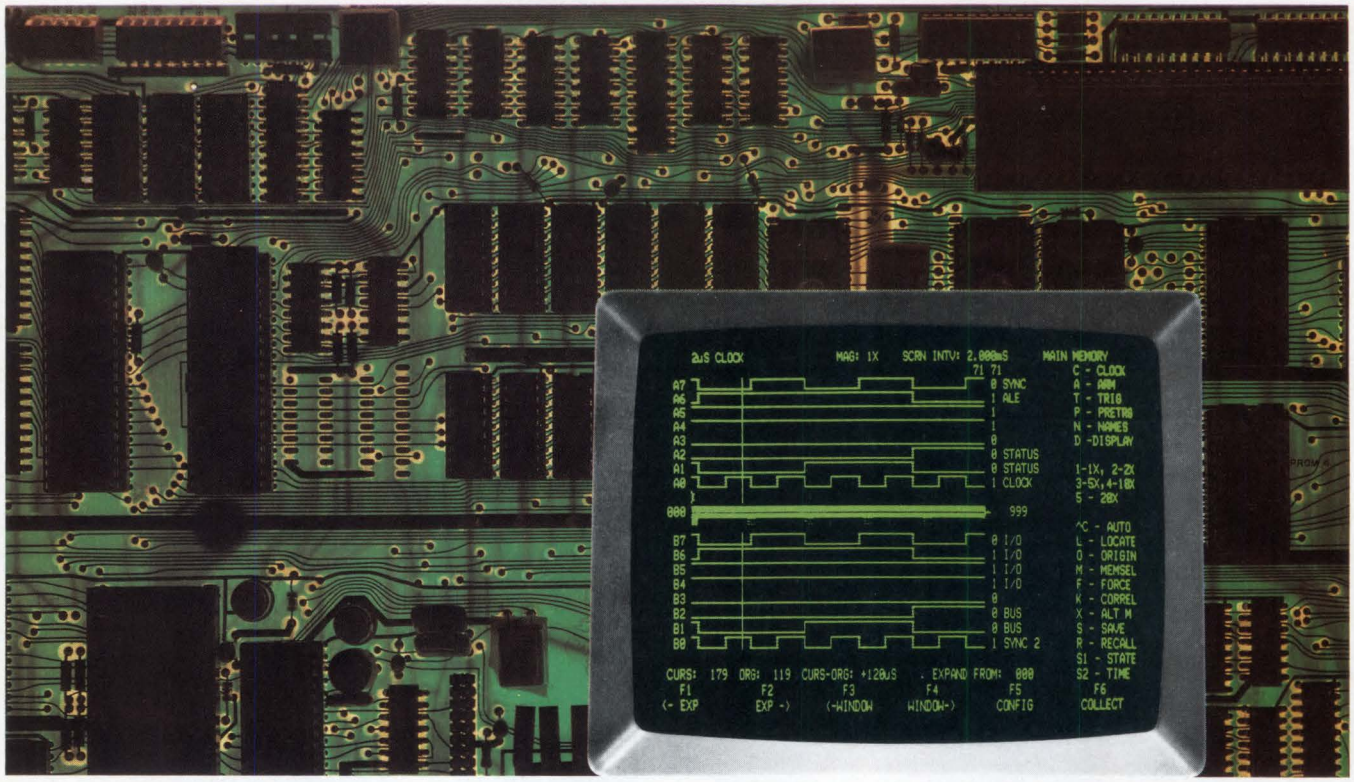

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CIRCLE 46

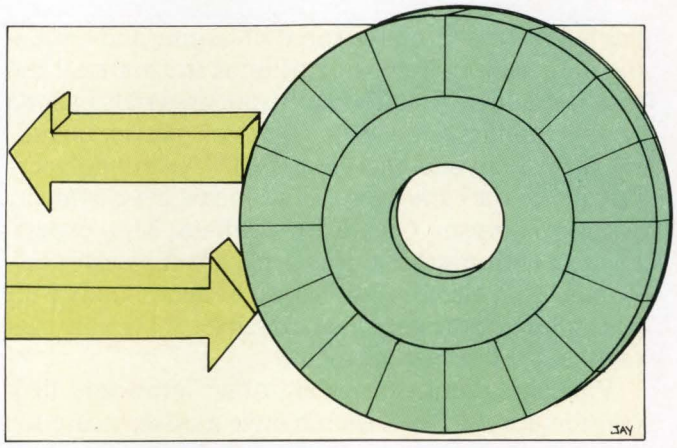
Optical systems erode mass storage barriers

Digital optical disks incorporate laser and video disk technologies to supplement conventional magnetic storage with low-cost, permanent and higher capacity storage.

In an increasing number of applications, such as scientific and medical research, health care, office automation and national defense, traditional magnetic tape and magnetic disk drive systems are becoming increasingly hard-pressed to manage today's heavier archival storage and electronic filing tasks. A supplement to conventional magnetic storage systems recently introduced in the electronic data processing marketplace incorporates the latest advancements in laser and video disk technologies to produce a rugged yet simple storage system possessing a long storage life and substantial storage capacity.

The digital optical disk resembles magnetic disk drives in its use of spindle and servo motor drives, and read/write and interface electronics. But unlike magnetic peripherals, optical storage systems use a laser to write data onto a preformatted disk that's designed to provide end users with low-cost permanent storage. This technology also provides easy replication of storage disks by using a physiochemical process.

In terms of value, a unit that provides 1 Gbyte of storage per 12-in. disk currently represents the best investment. The media cost in this evaluation is a fraction of a cent per kbyte, compared with the 1 cent-per-kbyte cost of a standard (erasable) floppy disk. As the technology evolves and new ways are found to achieve the desired results using more efficient or less expensive components, optical storage systems are expected to cost less.



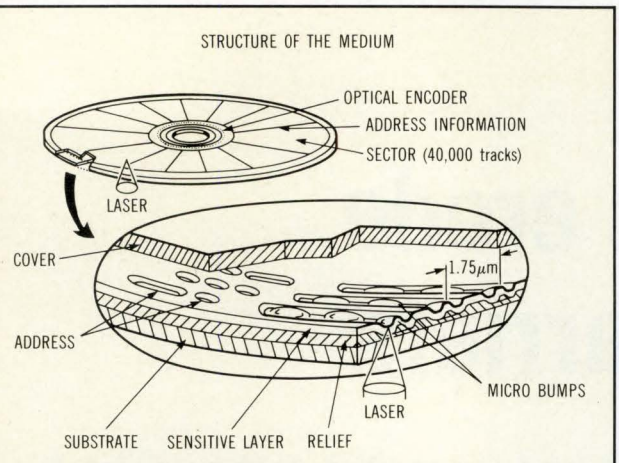
Given the large number of potential applications for optical storage, systems designers should seriously consider using optical storage for products that will reach full production within the next two to three years. Optical storage systems can now provide specific advantages over magnetic tape and disk peripherals. But the marketplace is a keenly competitive one, where a large number of drive developers are vying for position. There are many issues concerning both the technology and the vendors that must be carefully examined to make the correct decision concerning the use of optical storage systems.

John Robinson

Robinson is a vice president of sales at Image Management Systems (Providence, RI). He holds a BS in mechanical engineering from Pennsylvania State University.

Evaluating the optical disk

The focal point of optical storage technology is the disk itself. The disk should have direct access to any sector in the read/write mode; this capability



A side of a typical 12-in. optical storage disk is pregrooved with more than 40,000 spiral tracks. Each of these tracks is divided into 25 sectors and has a 1-kbyte capacity. Data is easily accessed according to its logical address.

has a direct effect on the speed of writing and retrieving data. Another consideration is the material the disk is made of. Possible substrate materials include tempered glass and various types of plastic, including polymethylmethacrylate (PMMA) and polycarbonate. In the early stages of its media development, Alcatel Thomson Gigadisc (Waltham, MA) experimented with a more durable plastic substrate. Existing plastic materials, however, became cloudy with age and made the data less accessible. ATG now uses tempered glass for all media.

Packaging and storage are other important disk considerations. Disks should have a cassette case for easy handling, storage, loading and unloading, and complete protection against pollutants or changes in the workplace environment. The cassette should be sturdy enough to withstand the rigor and shock of manual loading and unloading.

Most vendors of optical disk systems now guarantee data storage for up to 10 years. While tests for longer storage haven't yet been performed, 10 years will hopefully become the minimum figure. Unfortunately, there are many factors that might interfere with this goal. For example, with certain tellurium-based disks, the laser writes data by etching it on the disk platter. This is essentially a rapid oxidation process, which may continue long after the write process has been completed. The long-term effects of this continued oxidation aren't yet known. The integrity of the physical seals on the media can also be a factor in the longevity of the stored data. Tellurium disks are very susceptible to moisture damage, and any environmental incursion will result in data loss over a prolonged time period.

Another issue that applies specifically to optical disks is the quality of construction and packaging of any optical storage unit. Since a well-built system must ensure protection against environmental changes, special attention must be given to the materials used and the fit and finish of the product.

Consider the vendor

Vendors are frequently neglected players in the decision process involved in purchasing a new technology or system. There are some vendor issues that apply specifically to optical disk purchase. For example, vendors who can maintain strict control over the entire technology and development process without relying on outside suppliers of media (some of whom may not subscribe to similar standards) can ensure continuity in existing and future product development. And vendors who implement a field-testing program are able to ferret out design flaws before their products reach the production stage, greatly reducing the potential risk to the customer.

Other desirable vendor characteristics include systems that are manufactured to exacting standards (because they require few if any adjustments following the replacement of a part or subassembly) and systems that don't require hard-to-find custom-made parts. In addition, vendors who offer maintenance service schedules, factory-trained service technicians and training sessions for OEM customers deserve more favorable consideration.

Features to look for

Despite the seeming paradox, sophisticated, well-designed systems are the easiest to operate. For the disk system, the paramount question is whether the controller, error-correction scheme and servo mechanism work to give users an accurate flow of information and quick access to any record. There are a number of features to look for in attaining this goal. One is an optical system that features a capable solid-state laser diode module and photodetector. This is important because a laser that's constantly used at near full power will have an extremely short functional life span. A module that operates at 60 percent of full power is preferable.

Other desirable features include an optical head designed for "fine" accessing via radial and vertical positioning of the laser beam. A multiple accessing system (one that allows both coarse and fine access positioning) allows rapid track-to-track search. The advantage of this system is that the processor is much more accurate and doesn't "work" as hard in the actual tracking process. Another feature to look for is a sturdy linear coil mechanism that positions the optical head within the target track area.

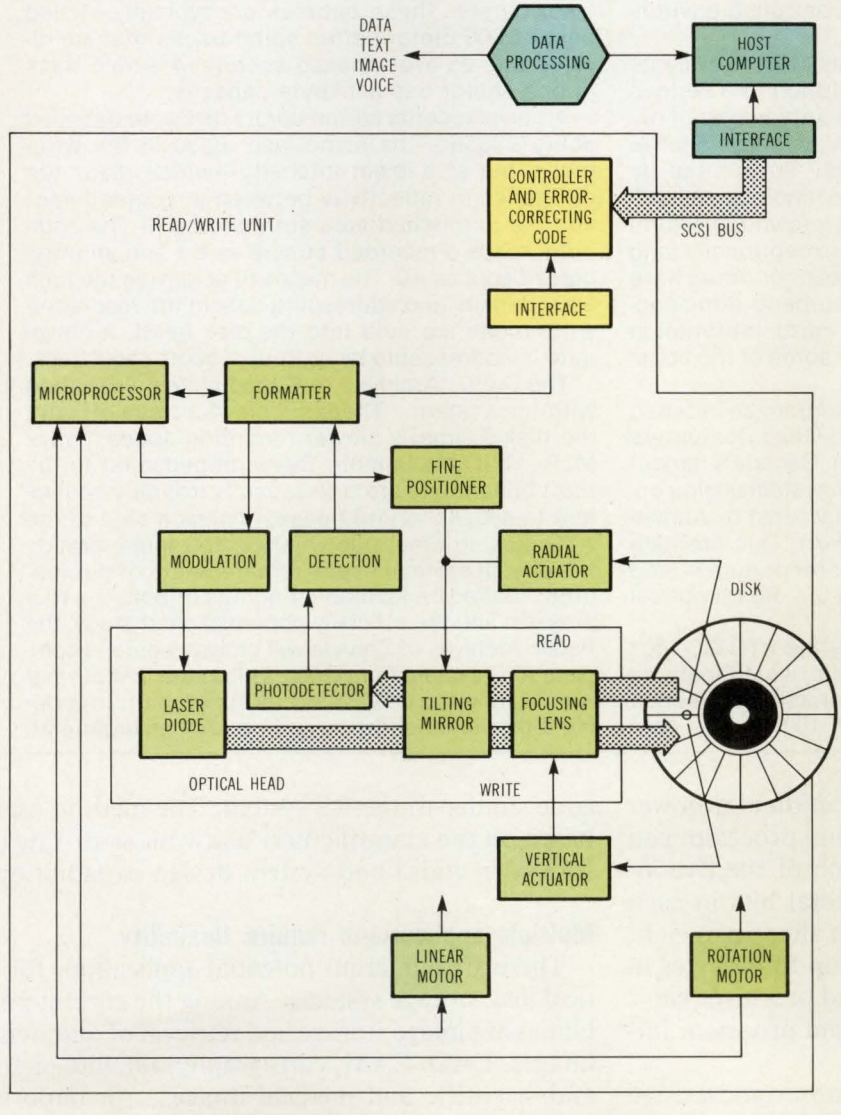
In the coarse access position, the optical head moves very quickly to all points on the target track area. Since the optical head is a heavy block assembly, the linear coil motor and guide rail must be capable of handling this heavy use. Thus, the performance rating of the motor should be comfortably above the demands placed upon it at peak usage. A good rule of thumb is that the demands placed on the motor shouldn't exceed 80 percent of rated power during normal operation.

In addition, the disk system should have a dedicated microprocessor that controls the power output of the laser, the servo mechanism and the disk access. This is necessary because extensive optical activity is required, and if the same processor that performs the servo mechanism activity also performs internal communications, the effectiveness of that processor is impaired.

Finally, the rotational drive motor should be securely clamped to the center spindle. Durability is essential—the motor shouldn't operate at more than 80 percent of the rated torque capacity.

Maintaining data integrity during the recording process is of paramount importance to the user. Several system vendors, including ATG, have developed powerful, real-time error-detection/correction circuitry that's simple, reliable and inexpensive. These systems feature an error rate of 10^{-12} after correction for normal data reliability in the data processing environment.

The high-speed Reed-Solomon (RS) burst error system used by ATG includes a back-end processor



The read/write unit of Alcatel Thomson Gigadisc's GD 1001 is designed to provide an accurate flow of information and quick access to records. It features a solid-state laser diode module and photodetector, fine accessing of the optical head and a dedicated microprocessor to control power output for the laser, servo mechanism and disk access.

Optical storage system resolves overcrowding of archives

The Public Archives of Canada had a problem—storage space. Thousands of public records, generated by every agency of the Canadian government—and, by law, written in both French and English—are delivered daily to 13 overcrowded government archive buildings in the capitol city of Ottawa and to five regional centers across Canada. When the prospect of a huge record avalanche began to alarm many high-ranking Canadian officials, a departmental optical disk committee was formed to examine various storage alternatives.

The committee felt that magnetic tape, while simple to use and store, didn't provide the storage capacity that could effectively stem the expansion of the burgeoning archives. Tape needed to be refreshed after two years, and it could be erased accidentally—an eventuality that no one in the public archives, especially those handling priceless manuscripts, was favorably disposed toward. Further, tape must be stored in a controlled environment to assure its longevity.

The committee selected Dennis Mole to evaluate the use of optical disks as a solution to a serious problem. Mole was recently appointed chief of optical disk systems for the public archives, a move which acknowledged his already substantial involvement in this relatively new technology. According to Mole, "Optical disks were known to perform well in applications where their exceptionally long storage lives (most last for 10 years or more) have helped to ease the day-to-day burdens of managing frequently unmanageable mass information flow. Libraries and hospitals are some of the beneficiaries of this technology."

Mole suggested that a pilot program be initiated between the public archives and Geac Computers International (Markham, Ontario), Canada's largest computer firm and a developer of systems using optical disk storage devices manufactured by Alcatel Thomson Gigadisc (Waltham, MA). This program called for the experimental transfer of data stored on existing magnetic tape to ATG's digital optical disk and back again.

The pilot program incorporates the ATG GD 1001 digital optical disk storage system, which features an SCSI interface and an error-detection/correction mode with a reliability rate of 10^{-12}. The data transferred to the disk from textual, numerical and cartographic tape is an exact image of the information stored on the tape. The Geac system accommodates documents in both ASCII and EBCDIC code, and will accommodate tapes in both the 1600-bit/in. and 6250-bit/in. formats.

The ATG optical disk used in the study offers a higher density than magnetic memory, with more bits and tracks per inch. The optical disk is easily removable and can be electronically accessed without rewinding. Since the optical disk is a nonerasable medium, archivists can't inadvertently erase or write over optically stored data once it's been recorded on the disk. The 12-in. disk consists of three layers: a substrate, a polymer layer and a heat-sensitive nobelium film sandwiched between two protective outer layers of plastic. Information is stored on the heat-sensitive middle layer in the form of minute bubbles raised on the disk surface by laser bursts. These bubbles are typically etched onto 40,000 preformatted spiral tracks that are divided into 25 even-spaced sectors. A single track in one sector has a 1-kbyte capacity.

Archival records stored on the disks are decoded using a laser—the same laser used in the write mode, but at a lower intensity—which reads the difference in reflectivity between a recorded spot and the untouched area surrounding it. The computer reads a recorded bubble as a 1 and an unrecorded spot as a 0. The means of achieving the high areal density and addressing data in the read-after-write mode are built into the disk itself. Archival data is addressable by both disk sector and track.

The Public Archives of Canada seems satisfied with the system. "There's a bit of a trade-off with the disk's slightly slower recording speed," says Mole, "but this is more than compensated for by the 1 billion-byte storage capacity (roughly equivalent to 400,000 printed pages) on each side of the ATG disk. In time, this will help to reduce greatly the overall storage space requirements of our records." Based on favorable findings of both the trial program and the officially commissioned study, the Public Archives of Canada will probably order a complete ATG system from Geac. This is the first of what is envisioned to be as many as six systems, operating either independently or in a LAN environment.

with the ability to do full RS correction at a slower speed when necessary. The front-end processor can correct up to a 1-byte burst in each of the five interleaved RS codes or up to 40 total bits in each block. The back-end processor can alter up to eight byte errors in each code word or up to 40 bytes in each block. Whenever the front-end processor can't repair an error pattern, the back-end processor initiates the correction.

To guarantee error rate limits, most optical drive manufacturers use mathematical interleaving of data code similar to the RS system. The method used is based on the manufacturer's raw bit error rate (before correction) and system design capabilities.

Multiple applications require flexibility

There are numerous potential applications for optical disk storage systems. Among the current possibilities are image storage and retrieval of audiovisual images, CAD/CAM, cartography, satellite pictures and scientific and medical images. An important criterion in selecting an optical storage system for

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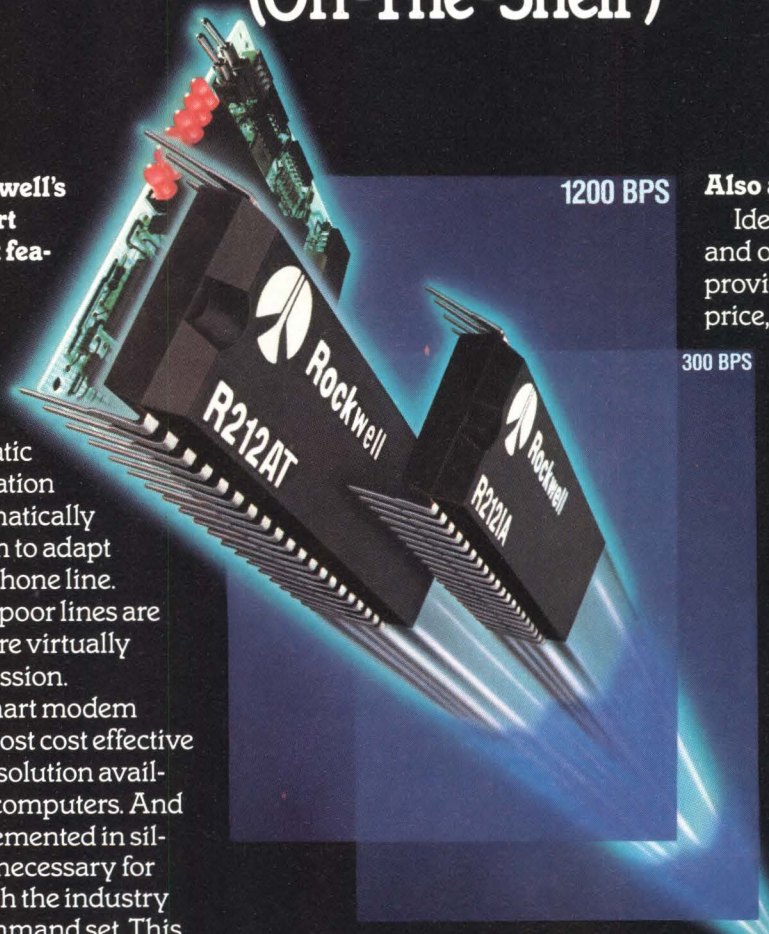


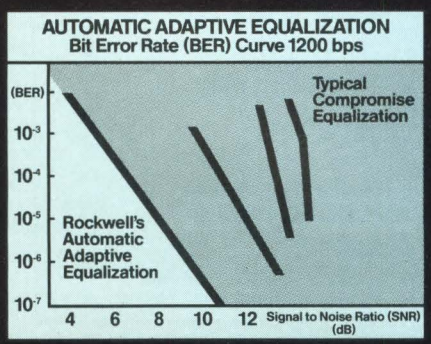
Introducing Rockwell's new R212AT smart modem device set featuring Automatic Adaptive Equalization.

Rockwell International's exclusive Automatic Adaptive Equalization Algorithms automatically enable the modem to adapt to any quality of phone line. Even signals over poor lines are enhanced to ensure virtually error-free transmission.

The R212AT smart modem device set is the most cost effective communications solution available for personal computers. And R212AT has implemented in silicon the software necessary for compatability with the industry standard "AT" command set. This allows quick design-in because we've presolved all the "AT" dialing functions. It incorporates auto dial, auto answer and can dial DTMF tones or pulses.

The R212AT smart modem offers lower system cost because it incorporates the controller and analog filter circuitry required for modem communications in the device set itself. This reduces parts count, enhances total system reliability and meets low power requirements for portable applications.

As well as operating asynchronously, the R212AT has synchronous mode operation for higher transmission throughput.



Also available: Rockwell's R212DP.

Ideal for remote diagnostics and other integral applications, it provides specific advantages in price, performance and system cost savings.

The R212DP, like the R212AT, has automatic fall back to slower speeds and an RS232C interface. Both these Bell 212A and 103 compatible device sets are available at any level of integration from devices to boards or customized private label systems.

For ease of evaluation, Rockwell provides a board level evaluation modem for laboratory analysis to assure the performance and quality of R212AT and R212DP.

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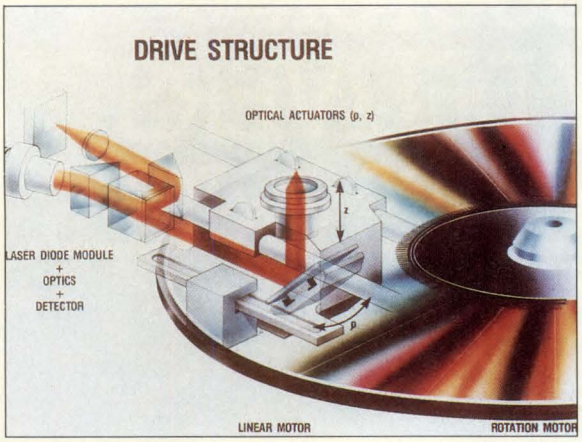
CIRCLE 47



A low-power laser routed through a succession of optics is used to detect variations in reflectivity between a recorded spot and the unrecorded surface. A sophisticated photodetector registers the difference as a 1 or a 0.

these applications is the compatibility of the system with host computers. The read/write optical disk should be compatible with the Small Computer System Interface because SCSI is projected as the general-purpose I/O interface of the future for small computers. SCSI is already in use for floppy disk and 5¼-in. Winchester drives and is rapidly developing into a popular standard for optical drive interfaces. SCSI compatibility provides a wide range of adaptability to both micro- and minicomputers.

Most manufacturers are already quite familiar with SCSI's counterpart, SASI (Shugart Associates Systems Interface). SCSI, which is an ANSI standard, is an enhanced version of the SASI system. Although the SMD (Storage Module Drive) interface was considered, existing optical drive performance was far below the high-performance capability of SMD. In addition, optical drives are not ideally suited for the range of applications typically targeted for SMD-compatible peripherals. **CD**

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

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Your back-up shouldn't leave you behind.

Meet the MT-2st. Teac's breakthrough half-height digital cassette tape streamer—based on the Philips cassette format. With its 90 ips performance you can store twenty megabytes of back-up in an incredibly quick four minutes.

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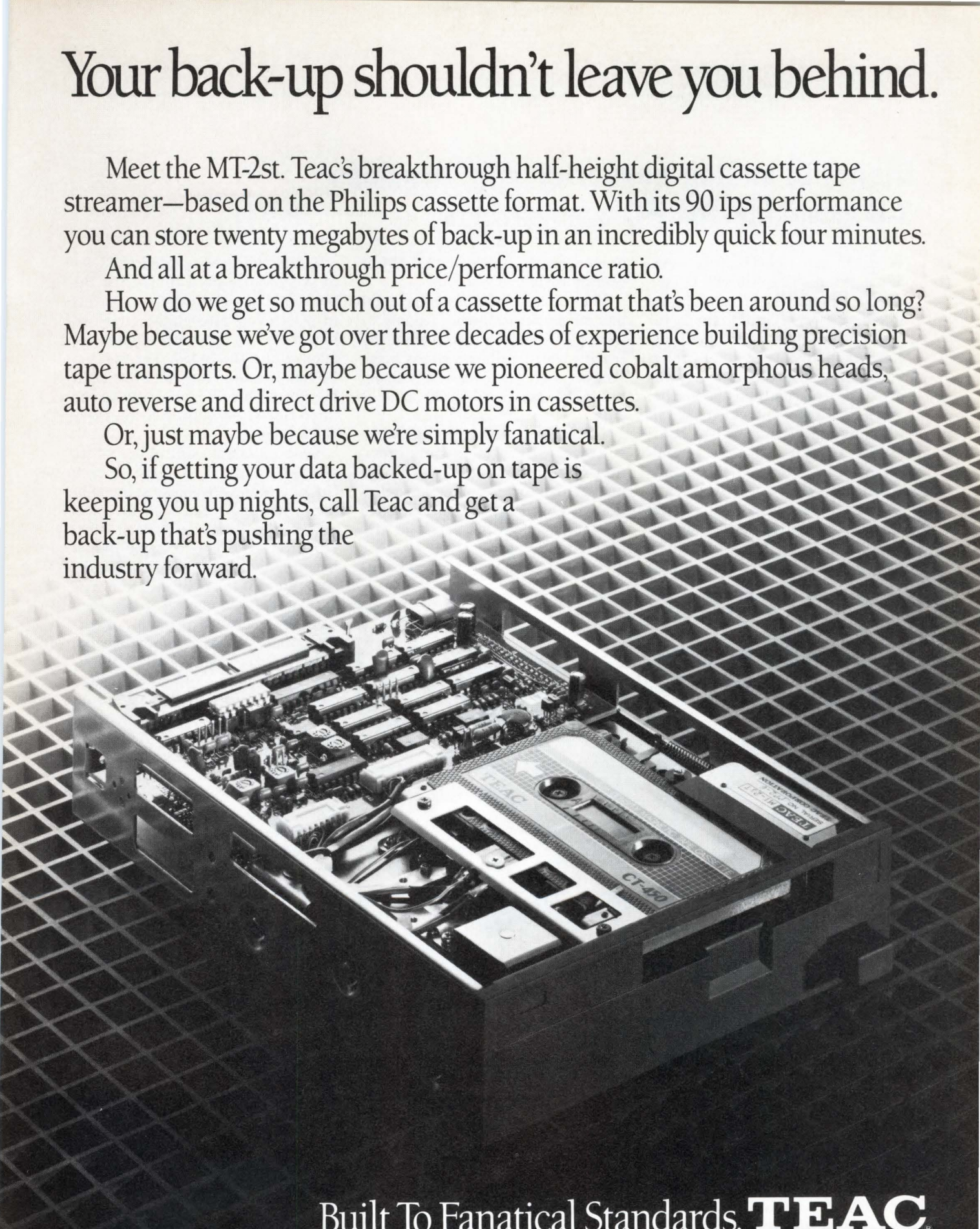

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CIRCLE 50

Digital-to-analog converter chip provides 3-D graphics for PC applications

The Bt453 is a 40-MHz, TTL-compatible, monolithic CMOS IC designed for producing high-resolution three-dimensional color graphics for personal computer applications. James A. Bixby, president of Brooktree, claims that the Bt453 is the only device presently available that combines three 8-bit video digital-to-analog converters with color palettes, overlay registers, a multiplexer, a latch and other elements on a single chip.

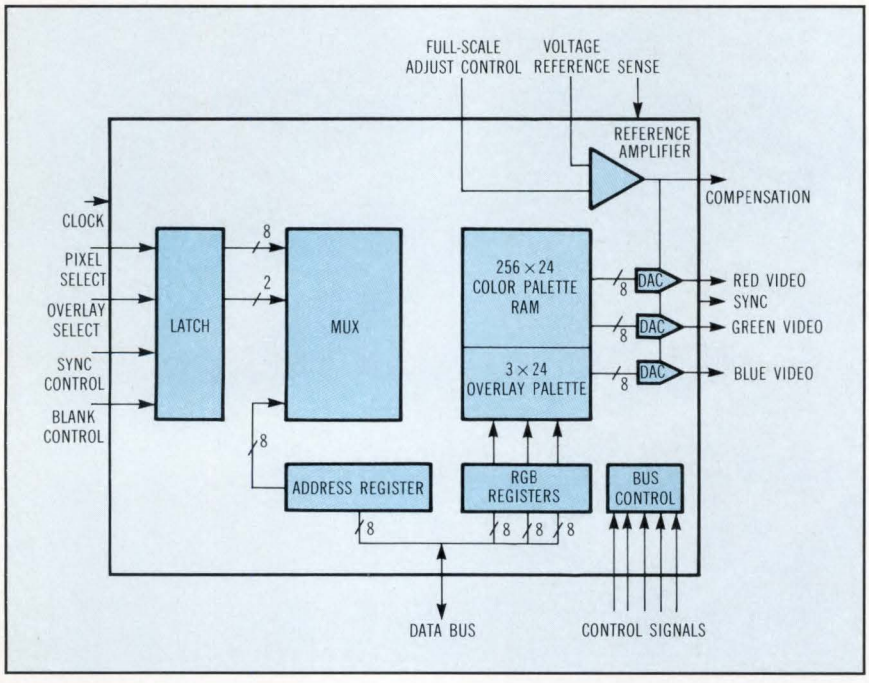
A dual-ported 256-color × 24-bit palette RAM combines with the company's exclusive Sidecar RAM, a three-color × 24-bit overlay palette, to provide 259 simultaneous colors from a palette of 16.8 million colors. The overlay palette RAM stores colors for cursors, menus, blinking and other operational functions.

A separate bus interface provides direct access for an external microprocessor controller to internal control registers and color and overlay palettes. Control signal inputs specify whether the MPU is accessing the address register, color palette RAM or overlay registers.

The address register's upper eight bits increment following reading or writing of blue color information and specify which color palette is being accessed. The two least significant bits (LSB) specify red, green and blue data.

This RGB data specifies which palette entry will provide color information. Overlay inputs may either have pixel timing to control overlay selection on a pixel basis or be controlled by external character, cursor or grid generation logic.

Red and green values, of eight bits each, are temporarily stored in registers when writing to the palettes. Then they combine with the eight bits from the blue value during the blue value write cycle, so that all 24 bits are written to the palettes at one time. During the period that the microprocessor is writing or reading RGB data, pixel and overlay select inputs to the latch are forced to a reference black level.



The latch serves as a digital buffer to synchronize pixel timing. At the beginning of a clock cycle, eight bits of pixel select information and two bits of overlay select information are latched into the Bt453. The selected 24 bits of color information, eight bits for each color, are input to the three video D-A converters on every clock cycle.

Sync and blank control inputs are sampled at the beginning of each clock cycle and are pipelined to maintain synchronization with the pixel and overlay select data. Each video D-A converter converts the digital information to analog signals for the color guns of the CRT monitor. The varying output current from each video D-A converter generates a corresponding RS-343A-compatible red, green or blue video signal as a voltage that drives a doubly-terminated 75-Ω coax directly. A typical output load is 37.5 Ω. No external buffering to the CRT is necessary. A separate current output provides a composite sync signal for horizontal and vertical synchronization. Typically, only the green video signal contains sync information.

The video D-A converters have a segmented architecture that eliminates the need for precision component ratios. Monotonicity and low glitch result from the use of identical current sources.

A 1.2-V external voltage reference is required for the chip and a single external resistor controls full-scale output current. Power dissipation is typically 500 mW and 1.0 W maximum. Differential and integral linearity errors of the D-A converters are less that ±1 LSB. All specifications are guaranteed over a full 0 to 70 °C temperature range.

The Bt453 is available as a 40-pin CERDIP in sample quantities for $58 each.

Brooktree, 9950 Barnes Canyon Rd, San Diego, CA 92121. **Circle 100**

—Sydney F. Shapiro

Personal computer for CAD/CAM users outperforms IBM PC AT

The APC IV, aimed at CAD/CAM users, delivers high-resolution graphics via a multisync color monitor that automatically adjusts to the scan points of all major graphics boards. The PC is completely compatible with the IBM PC AT.

The APC IV is available with either of two display monitors. The standard Advanced Color Monitor offers text and graphics resolution of 800 × 560 pixels. This 14-in. monitor automatically scans and adjusts to horizontal frequencies between 15.75 and 35 kHz. Covering the same scan rate and available as an option, the Elite Color Monitor supports 1120- × 750-pixel resolution.

The PC's extensive graphics capability is available in three options. Using the Color Graphics Board, the computer supports 640- × 200-pixel resolution and is compatible with IBM's CGA card. The Advanced Graphics Board features 140- × 350- and 640- × 200-pixel resolutions and is compatible with the IBM EGA card. It also supports software for the Hercules board. For the highest resolution environments, the Power Graphics Board provides 1120- × 750-pixel resolution, 16 colors and four planes of 128-kbyte video RAM. As opposed to the first two boards which occupy one expansion slot each, this board occupies two slots. A total of eight expansion slots are available.

Driven by the Intel 80286 microprocessor that drives the AT, the machine delivers user-switchable clock speeds of 6 and 8 MHz and supports 16- and 24-bit memory addressing. An optional 80287-3 math coprocessor is available. Each computer is bundled with MS-DOS 3.1 and runs most business and productivity software written for the AT.

A basic unit has 640 kbytes of RAM, expandable to 10.5 Mbytes. Five internal storage peripheral slots serve such potential options as 360-kbyte and 1.2-Mbyte floppy drives, and 20- and 40-Mbyte 5¼-in. half-height Winchester drives. Both Winchester drives supply 5-Mbit/s data transfer rates and a 40-ms average access time. A calendar/clock with battery backup, two RS-232C serial ports supporting data rates of 50 to 9600 baud and a parallel printer port are other standard features.

The PC comes in three configurations: the Model APC-H400 features a standard CPU with a 1.2-Mbyte floppy disk drive, the Model APC-H401 adds a 40-Mbyte hard disk drive to that configuration, and the APC-H402 replaces the 40-Mbyte drive with a 20-Mbyte drive. The IBM PC AT-like H401 sells for $5045.

NEC Information Systems, 1414 Massachusetts Ave, Boxboro, MA 01719. **Circle 101**

—J.H.M.

Design and Development Tools

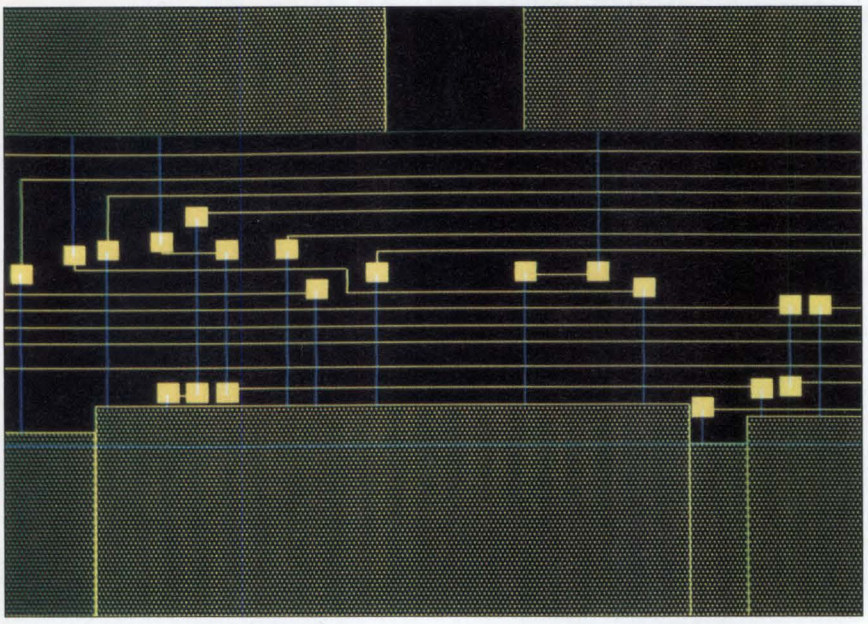
Cell-based layout system provides flexibility

A layout system for cell-based IC design helps minimize die size and lets the user forego most limits on block size and placement. Users can import blocks from other systems and place blocks anywhere without restrictions on gridding or cell height.

The Cellmaster layout system uses the same proprietary hardware as Daisy's 80286-based Chipmaster. It claims to solve the most prevalent problems in cell-based layout systems, including large die size, poor block support and lack of interactivity.

To optimize cell placement, the system uses simulated annealing, a technique that can provide a 10 to 20 percent area reduction over traditional tools.

The system's automatic tools are under user control at all times, with



capabilities to interrupt, modify and restart any process. All results can be edited interactively. On-line design rule and connectivity checks are provided for all manual operations.

Large blocks can be mixed with row-based cells. Within the rows, cells can have varying heights, and the routing can take advantage of the valleys left by the lower cells. Power and signal routing is provided to all cells.

Cellmaster is fully integrated with other Daisy systems for schematic capture, simulation, testability analysis and fault grading. Shipments are expected in July 1986. Cost of a turnkey system is $125,000.

Daisy Systems, 700 Middlefield Rd, Mountain View, CA 94039.

Circle 102

—R.G.

Memory Systems

3480-compatible cartridge tape drive cuts size and cost

Compatible at both tape format and tape cartridge levels with IBM's 3480 half-inch cartridge tape drive, Aspen Peripherals' I480 provides competitive performance in a smaller, less expensive package. A direct replacement for the IBM 3480-B22, which is rapidly gaining acceptance as the new industry standard for magnetic tape technology, the I480 supplies compatibility along with a simplified mechanical design.

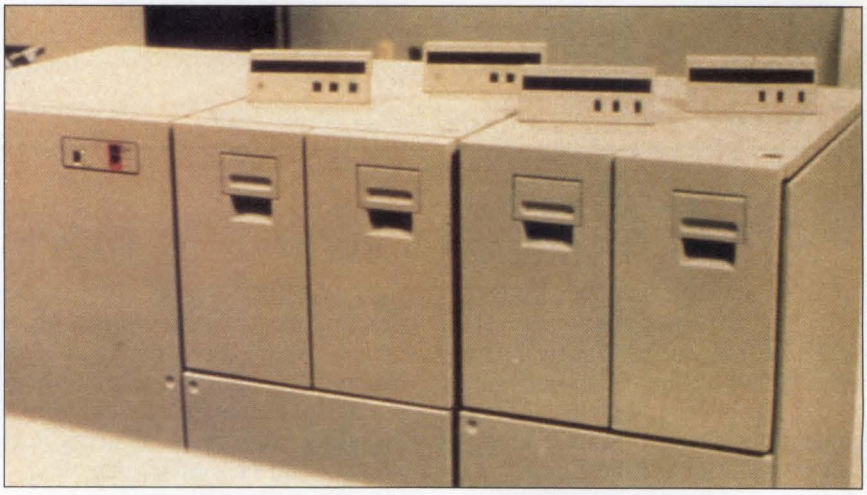
The 4-×5-×1-in. enclosed cartridge stores 218 Mbytes of formatted data, recording at a useful density of 24,689 flux changes per inch, using a double-density NRZI code, in an 18-track parallel format. The 18-track thin-film recording head allows data transfers to occur at 2.98 Mbytes/s. Reading and writing at a tape speed of 78.74 in./s, the drive can conduct searches at a 157.48-in./s rate. Rewind also occurs at 157.48 in./s, allowing a nominal rewind time of 41 s. The automatic tape load process requires 4 s.

The unit's design cuts the parts count by 15 percent over the 3480 drive and reduces space requirements by 75 percent. The I480 provides separate power and air supplies for each drive. This allows one drive to remain operable even if a pump fails.

Preventive maintenance consists simply of loading a cleaning cartridge that removes residue from the head. Built-in diagnostics can run at the drive level. Because the drive is functionally packaged with the read/write and device interface on one card and servo and reel drives on another, problems can quickly be isolated to one card or the other. A CE key pad allows drives to be taken off-line so that isolation and problem repair can occur without system interruption.

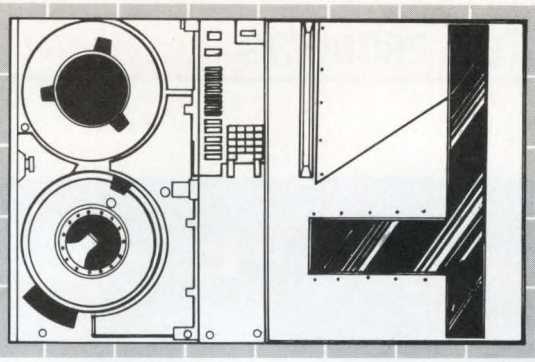
Aspen Peripherals, 1860 Lefthand Cir, Longmont, CO 80501.**Circle 103**

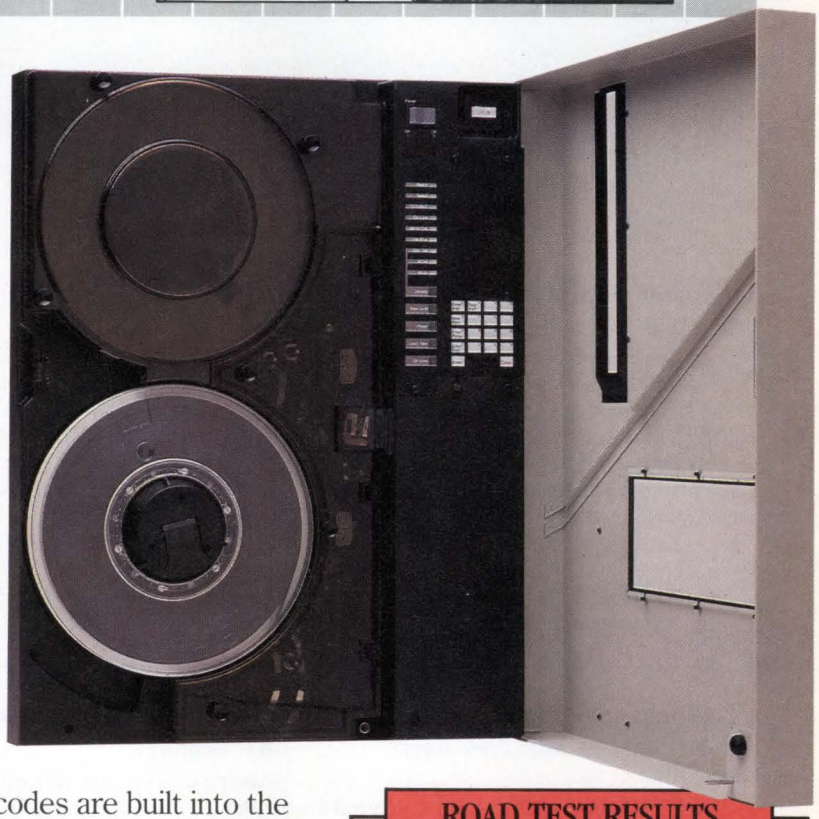
—P.K.



Storage Technology's New 2925 Tape Accelerator.

It goes with unsurpassed speed.
It comes with unsurpassed features.





TAKE THE PERFORMANCE DRIVE.

StorageTek's Model 2925 gives you the speed you need, and the features your customers demand. The 2925's Accelerator (Cache) feature dynamically adapts to system requirements and the host's capability ...at transfer rates ranging from 100 kilobytes per second up to 1.25 megabytes per second. The 2925 goes with speed indeed; but what it *comes with* is even more remarkable.

AT A GLANCE

Series Standard Features

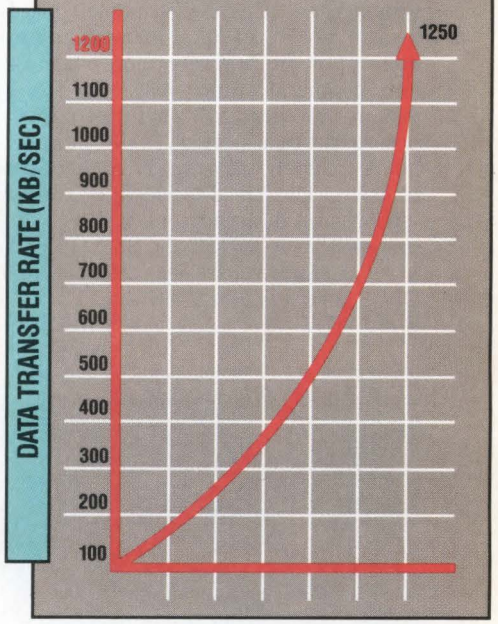
- *Dual-speed 50 ips Start/Stop and 100 ips Streaming with Buffered or Synchronous mode*
- *ANSI Standard 1600 bpi/6250 bpi formats*
- *Convenient Auto-Threading*
- *Integrated Formatter/Controller*
- *Service Panel with Alpha/Numeric Display*
- *Resident Diagnostics*
- *Host-optimized Data Transfer Rates*

Error correction codes are built into the cache's 256k of multi-record memory; so your data is checked both as it enters cache and as it is written onto tape. Data can be retrieved directly from cache–should defective media be encountered. The 2925 allows OEM systems integrators to attach ANSI-compatible 1600/6250 bpi capability to systems ranging from micros to minis...without software modification. For ease of integration, the 2925 is available with either StorageTek- or Pertec-compatible interfaces.

That's still only the beginning–be sure to read the accompanying list of features. You'll understand at a glance that 2925 performance is not only *speed...but reliability, flexibility and ease of operation.* StorageTek's experience with GCR 6250 bpi technology includes a full 11 years of pioneering, proving and perfecting. Our 2920 Series includes the 2921 (50 ips start/stop), the 2922 (50 ips start/stop with 100 ips streaming) in addition to the 2925 subsystem.

Take a drive in our 2920 Series...
and experience performance you'll be proud to call your own.

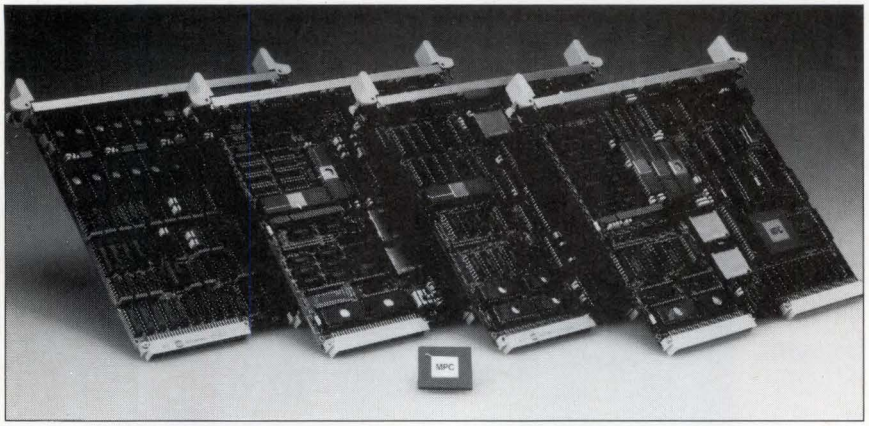
ROAD TEST RESULTS



StorageTek

Storage Technology. It's More Than Our Name...It's Our Commitment.

CIRCLE 51 **OEM MARKETING**/3N, Louisville, Colorado 80028-0001 USA (303) 673-4066



Multibus boards use message passing coprocessor

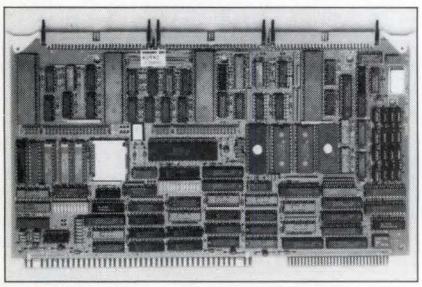
Four single-board computer products expand Multibus II system functionality. The group includes an Ethernet controller board, a central processor board, a serial communications board and a universal-site memory expansion board. All but the memory board use the Intel 16-bit 80186 microprocessor and the Message Passing Coprocessor single-chip bus interface. The iSBC 186/530 works as a communications engine and bundles an Intel 82586 Ethernet controller with 256 kbytes of dynamic RAM (expandable to 512 kbytes), and an RS-232C port. For industrial automation operations, the iSBC 186/100 CPU board features 512 kbytes of DRAM, four EPROM sites, two programmable serial interfaces and 24 programmable I/O lines. The memory board, designated iSBC MEM/601, supports up to 1 Mbyte. Units have self-test firmware. **Intel,** 5200 N E Elam Young Pkwy, Hillsboro, OR 97123.

Booth 2803/05, 2902/04 **Circle 104**

Eight-channel communications board serves Multibus users

Functioning as a master or a slave, the CD21/3518 intelligent communications controller board implements a wide variety of serial line protocols for Multibus system users. The eight-channel board uses an 8-MHz 80186 processor and optional on-board firmware to offload most host communications tasks. On-board memory provides 512 kbytes of parity-protected, dual-ported RAM and six DMA channels offer high baud rate data transfers. The RS-232 serial ports can be synchronous or asynchronous. Protocols supported include X.25 and SNA. Price is $1555. **Central Data Corp,** 1602 Newton Dr, Champaign, IL 61821.

Booth 2716/18 **Circle 105**



Converter serves vector-stroke CRT displays

Boasting a low-glitch performance rate of 10 mV, the DAC-02310 D-A converter features input storage registers, a 14-bit D-A converter, a track/hold deglitcher and precision reference and timing circuits. A 10-MHz update rate supports small changes. Available in 13- and 14-bit linearity grades with 14-bit resolution, the converter offers a settling time of up to ± ½ LSB for a full-scale ± 2.5-V step change in 600 ns. Output current is 5 mA max. Typical applications include vector-stroke CRTs and precision waveform generators. For military and industrial applications, the unit is packaged in a 32-pin hermetic TDIP. The cost is $245 for commercial (0° to +70°C range) and $269 for military (-55° to +125°C) temperature ranges. **ILC Data Device,** 105 Wilbur Pl, Bohemia, NY 11716.

Booth 1527/29 **Circle 106**

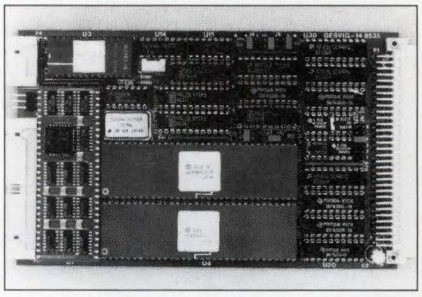
Development system links Unix with multiprocessing boards

Serving single or multiprocessor environments, the Performer 32/D is a VMEbus, Unix V.2 development/target system. Two VMEbus boards, the IV-3201 68020 CPU and the IV-3273 System Control and Console I/O, form the core of each unit. The CPU board features a 16-MHz 68020 microprocessor running with no wait states from a 1-Mbyte dual-port dynamic RAM. Other features include memory management and coprocessor facilities, parallel and serial I/O interfaces. Mass storage is provided by floppy and Winchester disks, removable cartridge tape and optional nine-track tape. The system runs Unix V.2 with Unisoft and Berkeley enhancements. **Ironics,** 798 Cascadilla St, Ithaca, NY 14850.

Booth 2505, 2507 **Circle 107**

Graphics controller displays 16 simultaneous colors

Built on two single-height Eurocards, a graphics controller for the G-64 bus runs on CAD workstations, industrial data terminals and displays for navigation computers. The set includes a controller board



and memory plane. The GESVIG-14 graphics controller board displays up to 16 simultaneous colors. Resolution ranges up to 800 × 600 pixels in a noninterlaced display. Features include zooming, drawing complex figures and pattern fill at speeds in excess of 2 million pixels/s. An on-board DMA controller exchanges large blocks of display memory with the system memory via the G-64/G-96 bus. The second board, designated the GESVIE-14, offers 2 Mbytes of memory and storage room for 4 million pixels. Particularly complementary to CAD applications, it provides fast scrolling and panning throughout the display memory. Both devices are mounted on standard 100- × 160-mm Eurocards. A two-board set sells for $3950. **Gespac,** 100 W Hoover Ave, Mesa, AZ 85202.

Booth 2616 **Circle 108**

Industrial CRTs provide shock and vibration resistance

The 1020 series touch-control screens are ready-to-install subsystems supporting manufacturing applications. Each unit comprises a touch-sensitive front panel, CRT, logic board, power supply and mounting hardware. A free-standing unit is also available. Sealed from moisture, dirt and contamination, the screens operate across a 0 to 60 °C range and are shock and vibration resistant. An RS-232 interface serves screen-to-host links. The price is under $1500. **John Fluke Mfg Co,** PO Box C9090, Everett, WA 98206.

Booth 2402-08 **Circle 109**

Connector solves electromagnetic compatibility requirements

Measuring only .375 in height, the Compu-Shield Assembly connector terminates round or flat-shielded, or unshielded cable with a wide range of wire guages. The connector comes in 6, 8, 10, 15 and 25 pins and exceeds FCC 20780 requirements while replacing DIN and Sub-D connectors. It is also field-installable. **Stewart Stamping,** 630 Central Park Ave, Yonkers, NY 10704.

Booth 1511 **Circle 110**

Low-power 12-bit A-D converter performs in 500 ns

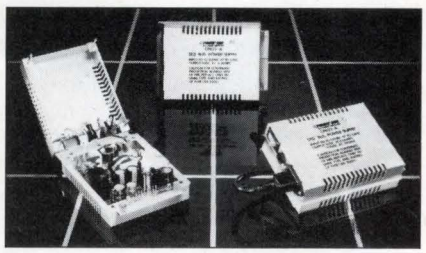
With a maximum power dissipation of 1.5 W, the ADC-500 A-D converter accomplishes a 12-bit conversion in a maximum 500 ns. A second unit, the ADC-505, is designed to serve military temperature ranges and offers a slightly slower 550-ns conversion speed. Both converters employ a digitally corrected subranging architecture that is built around a proprietary custom chip and laser trimming scheme. Features include initial errors of 3 least significant bits max for offset and gain errors, CMOS/TTL compatibility and three-state outputs. Spectrum, transient, vibration and waveform analysis are typical applications. Hundred-piece prices are $397 (0 to 70 °C), $346 (-55 to +125 °C) and $450 (-55 to +125 °C). **Datel,** 11 Cabot Blvd, Mansfield, MA 02048.

Booth 2620 **Circle 111**

UPS protects small micros and minis

The mini-UPS is a 750-VA miniature uninterruptible power supply (UPS) featuring automatic inverter restart and power alarm circuitry. Built for small micros and minicomputers requiring high start-up power for disk drives, it is engineered to deliver six times the rated current for very short durations. During blackouts the unit remains on-line with up to 10 minutes of regulated power to the computer from its own self-contained backup battery. Auxiliary packs can provide an additional 250 minutes of emergency power. **Sola,** 1717 Busse Rd, Elk Grove Village, IL 60007.

Booth 2820/22/24 **Circle 112**



STD Bus power supplies support card rack or motherboard units

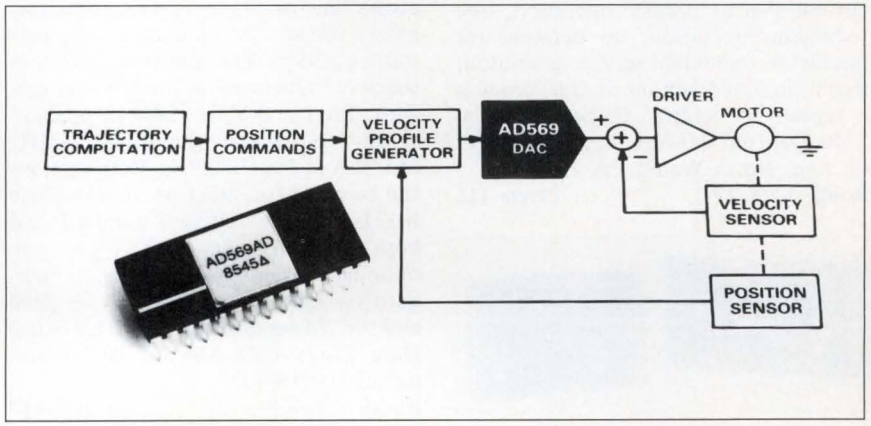
Delivering up to 74 W of dc output power, three STD Bus power supplies come in stand-alone or in rack-mounted configurations. All three units are available in compact efficient STD Bus-compatible packages designed to specifications of the STD Manufacturers Group. Three power levels serve most STD Bus system applications: the Model BP622 has a dc output of +5 V at 6.5 A; the Model BP632 provides +5 V at 4.5 A; and the Model BP635 offers +5 V at 10A. Prices are from $210 to $245. **Power One,** 740 Calle Plano, Camarillo, CA 93010.

Booth 2351/53 **Circle 113**

D-A converter features double-buffered chip interface

Guaranteeing 16 bits of monotonicity over its operating range, the AD569 is a double-buffered, 16-bit D-A converter that interfaces directly to either an 8- or 16-bit data bus. The device integrates CMOS logic with bipolar components to deliver a 200-mW typical power consumption with a 5-μs maximum voltage settling time to $\pm$0.001 percent for a full-scale step. Using the company's proprietary BiMOS II process, the converter features a voltage segmented design that combines three op amps, two 256-switch segment decode sections and two high-precision resistor strings to deliver $\pm$0.0004 percent differential nonlinearity. A double-buffered microprocessor interface permits sequential loading and simultaneous updating of data in a multiple D-A converter design. Packaged in a 28-pin ceramic or 28-pin plastic DIP, the converter costs $19, $24, $28, $37 and $88.50 for JN, KN, AD, BD and SD grades, respectively. **Analog Devices,** Two Technology Way, Norwood, MA 02062.

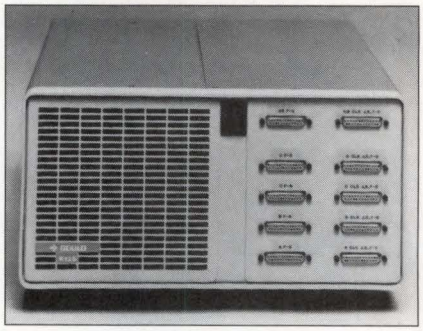
Booth 206/08, 307/09 **Circle 114**



Chip developer offers low-cost option to stand-alone systems

UniLab II Universal Development Laboratory supports more than 120 microprocessor types and runs command and control functions through the IBM PC. The product is actually four instruments in one. It combines a 48-channel bus-state analyzer with an in-circuit emulator, a stimulus generator and an EPROM programmer in a single package. Using a nonintrusive analysis technique, the system lets users run hardware and software at full speed. Trigger points can be specified by observing symptoms. Personality Paks provide all cables and software required for specific popular microprocessors. The learning curve on the system is appreciably shortened by a windowed display featuring menu-prompted commands executed through function keys. Multiple windows are manipulated for debugger and disassembler displays and pop-up panels indicate mode status. It sells for $2995. **Orion Instruments,** 702 Marshall St, Redwood, CA 94063.

Booth 4076, 4708 **Circle 115**



Test-verification unit targets CAD/CAM and ATE

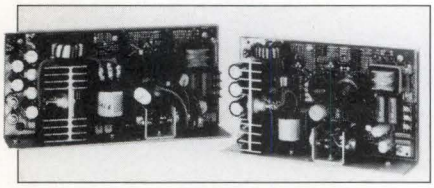
The K125 digital engineering design and test-verification unit operates as a CAE, CAD or ATE system peripheral or as an IBM PC, XT or AT intelligent peripheral. This analyzer uploads signals from the system under test as test vectors, permitting design simulation to use actual input signals for operational simulation. The unit then compares these results with actual system outputs for system verification. A 500-kbyte memory is programmable for pass/fail output from the unit to the main system. Configurable from eight to 80 channels, the main channel cards offer 32 channels of 20-MHz clocking. What's more, high-speed cards deliver eight channels at 100 MHz or four channels at 200 MHz. **Gould,** Design and Test Systems Div, 19050 Pruneridge Ave, Cupertino, CA 95014.

Booth 150 **Circle 118**

Power supplies offer true redundant operation

Meeting VDE, IEC, UL, BP, ECMA and CEE safety requirements, the V series 270- and 360-W switching power supplies provide 3750-Vac isolation and 8-mm safety spacing. These products feature current sharing parallel operation, true redundant operation, no derating for parallel or redundant service and output signals in redundant mode. Efficiency is a typical 80 percent. Pricing starts at $140. **Deltron,** PO Box 1369, Wissahickon Ave, North Wales, PA 19454.

Booth 1325/27 **Circle 116**



Dynamic RAM board features fast Multibus memory

Adding up to 2 Mbytes dynamic RAM to any Multibus system, the LBX 512K-2M dual-port, parity-checking dynamic RAM board delivers a typical LBX read data access time of 145 ns in its high-performance version. A standard version performs at 195 ns. The board runs zero-wait states in asynchronous mode in systems with Intel's 6-MHz 286/10 and in synchronous mode with Intel's 8-MHz 286/10A or 286/12 CPUs. Both versions can be fitted for either 64- or 256-kbyte RAMs. Parity checking is standard, and both Multibus and LBX cycles can optionally generate interrupts. The standard version of the board sells for $890 and the 2M version costs $1150. **Central Data Corp,** 1602 Newton Dr, Champaign, IL 61821.

Booth 2716/18 **Circle 117**

Data-acquisition subsystem designed for industrial operation

Expanding mainframe, controller and PC versatility, the Helios I Computer Front End is a data-acquisition and control subsystem. It communicates to any host using standard RS-232 and RS-422 interfaces. Configuration and programming instructions are included for the IBM PC, Tandy TRS-80, DEC PDP-11 and MicroVAX, and Apple IIe. A ruggedized design supports industrial applications, while a microcomputer in the subsystem drives measurement and control hardware and sends appropriate responses to the host. For plant-monitoring operations with large computer systems, a single unit is extendable to 1500 channels with a distributed extender chassis. The price is $1995. **John Fluke Mfg Co,** PO Box C9090, Everett, WA 98206.

Booth 2303-09 **Circle 119**

Multiple-output power supplies come in low profile packages

The RMV and RMC series open frame, multiple-output switching power supplies support instrumentation, communications, industrial and medical applications. Covering the 200- to 400-W power range, the RMV 22X is a 220-W convection-cooled unit. A 300-W convection-cooled unit, the RMV 30X, reaches 400 W as the fan-cooled RMC 40X. Both product families use MOSFET devices on the primary channel and magnetic amplifiers on secondary channels. Amplifiers provide post-regulation on all channels and high peak current capability on auxiliary channels. Prices range from $237 to $363 each. **ACDC Electronics,** 401 Jones Rd, Oceanside, CA 92054.
Booth 2557, 2559 **Circle 120**

Ethernet front-end processor handles X.25 wide area networks

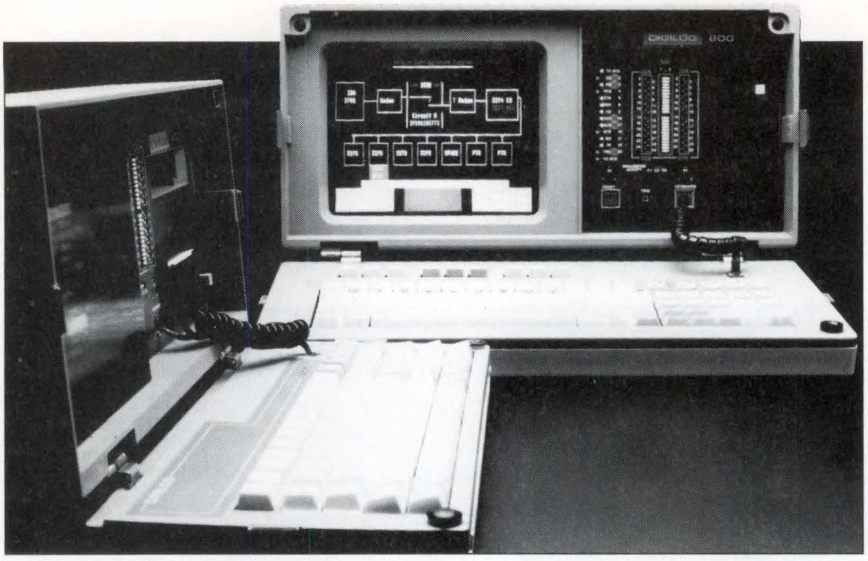
Offering a plug-in solution to Ethernet LAN interfaces, the SBE/MLAN-11 is a front-end processor for Multibus systems. This board operates as a typical Ethernet node processor when functioning as a slave controller or comes with its own power supply to run as a stand-alone serial/parallel/Small Computer Systems Interface gate to the Ethernet LAN. It combines a 10-MHz 68000 microprocessor with a Lance chip set to provide a transfer rate of 10 Mbits/s. Serial/parallel and iSBX channels use an on-board programmable 68450 DMA controller for full-duplex operations. Protocols supported include X.25, SDLC, HDLC, bisync and async. Price is $1495. **SBE,** 2400 Bisso Ln, Concord, CA 94520.
Booth 2521 **Circle 121**

Low-power ICs reduce system cost

The CD54/74AC/ACT family of advanced CMOS Logic (ACL) ICs are intended as high-speed, low-power replacements to advanced bipolar TTL families. Propagation delay in these devices is typically 3 ns and output drive current is specified at 24 mA. Ten IC types are available, including a quad 2-input NAND gate, a dual D-type flip-flop and a variety of octal device types. Using CMOS logic, these ICs consume only one-fourth the power of corresponding bipolar TTL families when operating at 5-MHz clock rates. **RCA Solid State,** Rt 202, Somerville, NJ 08876.
Booth 315/17/19 **Circle 122**

Digital plotter boasts 70-cm/s performance

Using an optical positioning system, the SE 293 digital plotter boasts a repeatability of better than 0.1 mm and a plotting speed in excess of 70 cm/s. The plotter is driven by a digital servosystem that uses dc motors. A 16-bit microprocessor controls advanced functions including circle generation, business graphics, coordinate transformation, hatching of areas and interpolation of higher order. Users can program maximum speed, contact force and acceleration. **BBC-Metrawatt/Goerz,** 2150 W 6th Ave, Broomfield, CO 80020.
Booth 2110/12 **Circle 123**



System analyzes SDLC/SNA links

Using turnkey applications software, the Digilog 600 and Digilog 800 data analyzers perform automatic Synchronous Data Link Control/Systems Network Architecture (SDLC/SNA) protocol activity monitoring. Tracking protocol communications and record performance statistics, SDLC/SNA message traffic errors are counted, categorized and interpreted in English. A diagnostic mode permits the user to review Level 2 SDLC and Level 3 SNA communications between devices. When an error occurs, a message appears on-screen and an audible alarm sounds. Protocol violations detected and/or counted include invalid number of frames received/sent, SNA sense data messages, time-outs, frame rejects, frame check sequence errors, aborted frames, short frames and invalid SNA response. **Digilog,** 1370 Welsh Rd, Montgomeryville, PA 18936. **Circle 124**

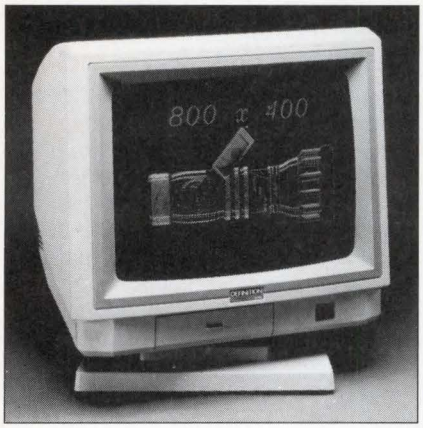
Vector network analyzer supports communications characterization

The 8753A vector network analyzer, while covering a 300-kHz to 3-GHz range, measures the magnitude and phase of transmission and reflection characteristics of components and devices with resolutions of 0.001 dB and 0.01 degrees over a 100-dB dynamic range. A built-in synthesized signal source provides 100-mW

swept-frequency test signals with 1-Hz frequency resolution. For the characterization of communications systems components, the unit measures delays as long as 1 s and offers a group delay resolution of better than 1 ps. It costs $23,500. **Hewlett Packard,** 1820 Embarcadero Rd, Palo Alto, CA 94303. **Circle 125**

Storage oscilloscope serves signal analysis

DSS 5040 is a 40-MHz portable A-D storage oscilloscope featuring 10-MHz single-occurrence capture. Function selection controls are identical to those found on most analog scopes but with the addition of a push-button selector for sine or pulse interpolation and push-button controls for store, erase and reference memory. A level-lock circuit controls trigger signals and automatically adjusts the trigger level. Other features include autofocus, roll mode, 1-kbyte memory on both channels, a channel one (50 mV/div) output and recorder output. The unit sells for $2995. **Kikusui International,** 17819 S Figueroa St, Gardena, CA 90248. **Circle 126**



Monitor and card provide flicker-free graphics

A color graphics monitor and graphics card, developed in a joint venture between two manufacturers, offer flicker-free graphics for business software. Microvitec's Definition 895 DU and Ultragraphic's Ultragraph 800 run on the IBM PC or AT and provide flicker-free resolution of 800 × 400 pixels in 16 colors. The graphics monitor features a horizontal scan frequency of 15.75 to 17.1 kHz. An antiglare screen plus brightness and contrast controls are included. The graphics card runs PC-compatible software and generates enhanced text. Prices are $895 for the monitor and $995 for the card. **Microvitec,** 1943 Providence Ct, College Park, GA 30337. **Ultragraphics,** 37 S Franklin St, Chagrin Fall, OH 44022.

Circle 127

Interfaces link digital cameras with computers

An interface package links IBM PC-compatible computers to Eikonix Series 78/99, Series 850 and E-Z Scan digital cameras. Based on the IEEE-488 protocol, the package consists of two interface cards: one in the electronic support unit of the digital camera and the other in a card slot of the host computer. The interfaces run with PC-DOS or MS-DOS on hosts with an IEEE-488 communications port, a minimum 256 kbytes of memory and disk or tape storage. By linking digital cameras with low-cost PCs and compatibles, users can obtain a high-performance digital imaging system for one-half the cost of using a minicomputer host. **Eikonix,** 23 Crosby Dr, Bedford, MA 01730. **Circle 129**

Controllers offer enhanced graphics to VMEbus

The VG-640 graphics display controller provides enhanced graphics to the VMEbus. The controller is a dual-height VMEbus card that drives a 60-Hz noninterlaced display of 640 × 480 pixels. As many as 256 colors can be displayed. Drawing up to 35,000 vectors/s (30-pixel vectors) and 5000 characters/s, the VG-640 controller can draw a complete screen in less than a second. A two- or three-dimensional command set is executed on board with a 32- or 16-bit CPU. The high-level command set includes line, circle, ellipse, polygon, fill, LUT and text commands. The VG-640 graphics controller is priced at $2995. **Matrox,** 1055 St Regis Blvd, Dorval, Que, Canada H9P 2T4.

Circle 130

Emulator provides desktop control over VAX CAE programs

A graphics terminal emulator provides circuit designers with the ability to access DEC's VAX/VMS or MicroVAX computers on an IBM PC, XT or AT. The G Term/E Term emulation software uses a personal computer as a graphics window to VAX or MicroVAX-based systems, allowing users to take advantage of the full computational power of mainframes. Engineers can perform design compilation, simulation and autorouting, viewing these operations from the desktop unit. Drawing files can be sent to the target host for compilation and simulation, speeding the communication of design data from distributed CAE workstations to host-based CAE/CAD applications. Designs or drawings can be stored on the VAX or MicroVAX for archival storage or control. These designs are accessible using the PC as a remote graphics terminal under the VMS time-sharing system. To run on PC hardware, the emulator requires a graphics board that is compatible with the Enhanced Graphics Adapter or Hercules Graphics Adapter standards. To interface to the VAX, a serial communications port is also necessary. The graphics terminal emulator costs $2500. **Case Technology,** 633 Menlo Ave, Menlo Park, CA 94025.

Circle 131

Single-slot card incorporates IBM PC graphics standards

Delivering four IBM PC graphics standards in a single-slot card, the SigmaEGA high-resolution graphics board uses a software emulation technique to support the IBM Enhanced Graphics Adapter (EGA), the Color Graphics Adapter, the Monochrome Display Adapter and the Hercules Graphics Adapter. Users can run all EGA graphics modules with 256 kbytes of on-board standard memory. The board is compatible with the IBM PC, XT, AT and compatible computers, and interfaces with the IBM Monochrome Monitor, Color Display Monitor and Enhanced Color Display Monitor. With the PC Paintbrush software package, the price is $595. **Sigma Designs,** 2023 O'Toole Ave, San Jose, CA 95131.

Circle 128

1-Mbit CMOS EPROM targets high-performance systems

A 200-ns access time, high-speed programming and 16-kword × 16-bit organization are features of a 1-Mbit CMOS EPROM. The Am27C1024 1.5-micron device can be programmed in less than 2 minutes, using an AMD interactive algorithm. The 16-bit-wide chip architecture interfaces directly with 16- and 32-bit systems. In active mode, the device consumes 250 mV; in standby mode, it uses only 5 mV; and when the chip-enable input is deselected and the device powers down, it dissipates only 1 mV. The EPROM is currently available in a 40-pin side-brazed package, and a leadless chip carrier package will be offered later this year. A version for operation in the commercial temperature range costs $199 in 100-unit quantities. **Advanced Micro Devices,** Box 3453, Sunnyvale, CA 94088.

Circle 132

10-MHz numeric coprocessor doubles speed of 80287

A 10-MHz version of the high-performance 80287 numeric coprocessor, fabricated with an HMOS-111 1.5-micron process, operates at twice the speed of earlier models. This process also cuts die size by 50 percent. Containing 80-bit registers, the 80287-10 is compatible with the object code of the 80287 numeric coprocessor. Software designed for earlier versions can be upgraded to systems based on 80286 and 80386 microprocessors. The numeric coprocessor adds single- and double-precision floating-point, trigonometric, logarithmic and exponential instructions and conforms to the IEEE Floating-Point Standard 754. In 40-pin ceramic DIP, the 80287-10 costs $350 in quantities of 100. A 5- or 8-MHz version is also available. **Intel,** 3065 Bowers Ave, Santa Clara, CA 95051.

Circle 133

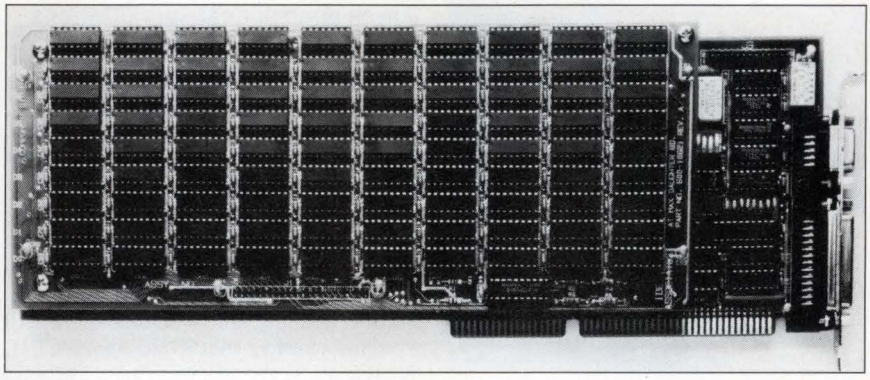
CMOS floating-point DSP boasts 13.4-Mflops performance

Manufactured with a 1.5-micron CMOS double-layer metal process, the μPDP77230 digital signal processor (DSP) features a 32-bit floating-point architecture on chip. The device includes a 55-bit floating-point multiplier that executes in a 150-ns instruction cycle. It completes a 512-point complex floating-point Fast Fourier transform in 4.7 ms and provides 13.4-Mflops performance. Unlike other digital signal processors, it addresses external memory for both data and instructions. Two 512- × 32-bit, separately addressable RAM blocks feed operands to the multiplier. Available in a 68-pin grid array, the device uses a 5-V power supply and dissipates 1.7 W. In 100-unit quantities, the μPDP77230 DSP is priced at $260. **NEC Electronics,** 401 Ellis St, Mountain View, CA 94039.

Circle 134

Half-slot accelerator speeds IBM PC, XT

Reaching processing speeds three times faster than the IBM PC or PC XT, the TinyTurbo 286 is a half-slot accelerator board that uses an 80286 CPU. It plugs into the host's 8088 processor socket, while the 8088 is plugged into a socket on the board. By operating independently of, but in tandem with the PC, the board's processor with 16-bit on-board bus and 8-kbyte static RAM cache accesses all system memory. Retail price is $695. **Orchid Technology,** 47790 Westinghouse Dr, Fremont, CA 94539. **Circle 135**



AT multifunction board meets variety of software applications

Supermax/EMS is an IBM AT multifunction board that combines expanded and extended memory, two serial ports and one parallel port. Memory capacity is 4 Mbytes. The board supports all types of PC software applications, including those using the Lotus/Intel/Microsoft specification as well as applications using conventional memory. Print spooling software accompanies the board, which uses expanded memory to print large files without tying up the PC. **Ideassociates,** 35 Dunham Rd, Billerica, MA 01821. **Circle 137**

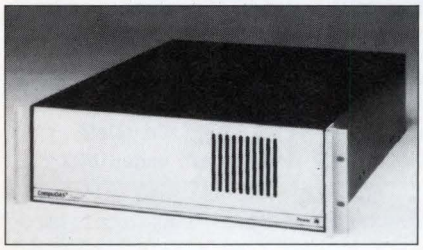
Single-board computer with CMOS serves industrial applications

Designed for products serving industrial applications, the CMOS Micro PC is the first PC bus single-board computer with full CMOS processing. Only one-fifth the size of a typical PC motherboard, the single-board computer plugs into a passive backplane and is form-factor compatible with IBM PC expansion cards. The board's compact size comes from its use of the company's proprietary FE2010 VLSI integrated circuit. In addition to the CPU, the board features an 8087 processor socket, keyboard port, 256 kbytes of CMOS RAM and the company's PC-compatible ROM Bios. Single-quantity price is $550. **Faraday Electronics,** 743 Pastoria Ave, Sunnyvale, CA 94086. **Circle 136**

Hardware/software platform enables user-defined systems

Providing extreme flexibility and broad expansion paths, the System 19 family computer systems are based on the Advanced System Platform (ASP). The ASP is a fundamental system architecture offering an interchangeable set of processors, displays, mass storage, system interfaces and software elements. Three basic configurations serve graphics systems, multiuser systems and servers (database, file or compute). All designs are based on the Unix System V operating system and the Motorola 68020 microprocessor. Up to eight 68020 VLSI microprocessors can be combined with up to 40 Mbytes of RAM and between 50 and 560 Mbytes of Winchester disk storage. A dual-bus architecture using a 12-Mbyte/s System Composition Bus and a 33-Mbyte/s Interprocessor Bus supports both low-cost single-processor and high-performance multiprocessor configurations. System prices start at $17,200. **Counterpoint Computers,** 2127 Ringwood Ave, San Jose, CA 95131. **Circle 138**

Control and Automation

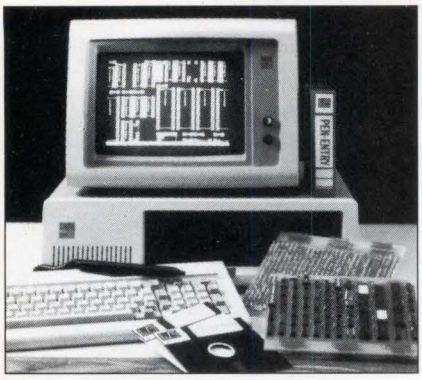


Single-board controller optimized for process control

Sentinel is a 16-bit Intel 80186/8087-based, single-board intelligent controller for industrial control operations. The computer integrates analog and digital I/O, pulse accumulation and frequency inputs through a PROM-based real-time operating system and an enhanced Basic language called Dabil. Supporting RS-232, RS-422, RS-423 and a 250-kbit/s standard LAN, the board offers systems integrators the opportunity to build applications software simply by plugging into a CRT. On-board diagnostics monitor system performance and flash error messages on an LED display. Features include a dual floppy disk controller, a real-time clock, four serial ports and data-acquisition rates to 10,000 samples/s. In single quantities, the price is $4500. **Compudas,** 61 Brown Rd, Ithaca, NY 14852. **Circle 139**

Process controller offers extensive memory

Designed for distributed control systems or stand-alone control requiring up to 48 bits of digital I/O, the Z80A CPU Process Control Computer offers a 16-kbyte EPROM and 8-kbyte battery-backed RAM. Eight optically isolated digital inputs and 16 digital outputs can operate up to 50 V at 500 mA. Additional features of the Process Control Computer include 24 bits of Opto 22-compatible, programmable digital I/O, a watchdog timer and a Z80 counter timer chip. **Gaston County Controls,** Box 927, Mount Holly, NC 28120. **Circle 140**



Wire-wrap design package uses files created by other CAD stations

Pen-Entry PC is an add-on interactive graphics CAD/CAM package running on the IBM PC family that speeds development of wire-wrap or discrete wired prototypes. The package offers a precursor hardware debugging opportunity, while compiling a data base for improved integration of later printed circuit board or Multiwire board production. Consisting of a graphics card, light pen and software, the package lets users develop the wire-wrap board directly from schematic or through optional links for downloading and data base exchange between schematic net files created by other IBM packages. Once a graphics facsimile of the panel has been created, users can lay out components and interconnections with special capabilities for handling gate arrays, surface-mount devices, restricted area or via routing and twisted pairs. The price is $5999. **Wire Graphics,** 95 Sherwood Ave, Farmingdale, NY 11735.

Circle 141

Three-dimensional workstations speed graphics by 44 percent

Serving graphics-intensive applications such as solids modeling, simulation, molecular modeling, seismic and fluid dynamics functions and animation, the Iris Series 3000 are real-time 3-D workstations. The product line consists of the 3010 terminal featuring a 20-Mbyte disk drive, the 3020 workstation with a 72-Mbyte disk drive and the 3030 workstation with a 170-Mbyte disk drive. All systems employ the 68020-based CPU, 8-MHz VLSI geometry engines, 2 Mbytes of memory expandable to 16 Mbytes, eight bit planes expandable to 32 with a Z buffer, optional floating-point processor board and a 20-slot chassis. Graphics transformations are accelerated to 86,300/s, a 44 percent increase over 68010-based systems, using a set of specialized VLSI processors. An Extent File System speeds disk I/O without wasting disk space. The Model 3010 sells for $34,900, the 3020 for $42,900 and the 3030 for $54,900. **Silicon Graphics,** 2011 Stierlin Rd, Mountain View, CA 94043.

Circle 142

Grayscale workstation fills niche between monochrome and color

Designed for applications requiring high graphics clarity but not full color, the Sun 3/160G workstation is an eight-plane system that can simultaneously display up to 256 shades of gray. Main memory is 4 Mbytes standard, expandable to 16 Mbytes. A 12-slot pedestal accommodates a graphics processor, floating-point accelerator and third-party boards. The workstation combines a 16.67-MHz MC68020 processor with a 12.5-MHz MC68881 floating-point coprocessor and a full VME-based architecture. Features include high-resolution, bit-mapped graphics, Ethernet networking, a 66-Hz, noninterlaced display refresh rate and the company's version of the Unix operating system. A basic workstation lists for $29,900. **Sun Microsystems,** 2550 Garcia Ave, Mountain View, CA 94043.

Circle 143

Printed circuit board design supports surface-mount uses

The V04 CAD system enhances printed circuit board designer productivity by specifying critical component placement while automatically routing a printed circuit board with high-quality routing patterns. It handles analog and digital boards as well as multilayer boards, and offers special capabilities for surface mount technology. The user can override the automatic router at any time using a data tablet. Graphics features include hard pan and zoom and rubberbanding. The system also accommodates military specifications. Running on a DEC VAX-11/73 with a specially designed accelerator, a two-station system with an off-line autorouter processor is priced under $200,000. **Calay Systems,** 2698 White Rd, Irvine, CA 92714.

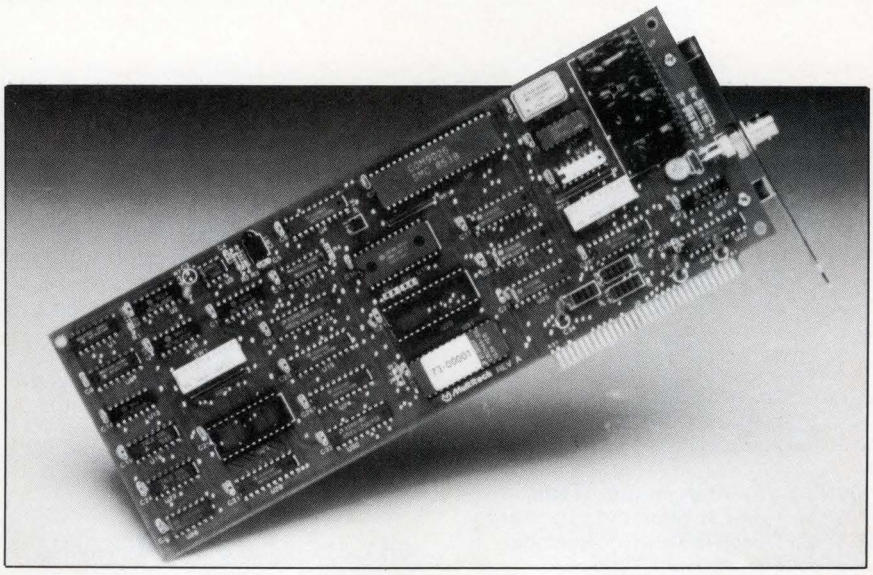
Circle 144

Controller offers Ethernet features to military users

The first intelligent Ethernet controller for military computers, Linc is a single-card communications device that coordinates the movement of data onto and off of any IEEE 802.3/Ethernet-compliant network. The card accommodates both Ethernet and IEEE 802.3 hardware protocols to provide half-duplex, synchronous serial transmission at 10 Mbits/s. An on-board, 16-bit MicroEclipse microprocessor provides intelligence and thereby increases system throughput. This controller performs all data link and physical layer functions on a single I/O card, which can be installed in any 16-bit computer chassis or I/O expansion chassis. Besides the dedicated microprocessor, the board contains 256 kbytes of RAM, up to 5 kbytes of PROM and built-in test capabilities. **Rolm Mil-Spec Computers,** One River Oaks Place, San Jose, CA 95134. **Circle 145**

Data repeater links broadband and baseband Ethernet

The Ethermodem Repeater links Ethernet networks running on standard or thin-coax cable to broadband Ethernet networks. Supporting a 10-Mbit/s data rate, the repeater contains an integral Broadband Ethernet modem and serves single- or dual-cable networks. The repeater retimes, amplifies and repeats all receiving signals from one coax cable segment and passes the signal to the next. To the user, an extended network appears as a single network. The price is $6250. **Chipcom,** 31 Thorpe Rd, Needham, MA 02194. **Circle 147**



LAN offers network-wide file sharing

The ComcoLAN local area network boasts an operating system that allows every workstation in the network to function as a shared file server. Based on Datapoint's Arcnet token-passing architecture, this product links workstations with either passive four-connector hubs or active eight-connector hubs. The LAN uses coax cable with BNC connectors between workstations. Data transfer rate is 2.5 Mbits/s using interrupt-driven memory-mapped buffers. Three levels of security are available. A high-performance disk cache, optimized disk scheduling and the ability to boot directly from the network are also provided. **Multitech,** 9FL 266, Sung Chiang Rd, Taipei, Taiwan. **Circle 146**

Software

Software products link networked PCs and dissimilar hosts

Running on the TCP/IP protocol, the Exos 8052-01 NetBios-TCP/IP software package allows users to run any DOS 3.1 personal computer networking application compatible with IBM's NetBios standard interface across an Ethernet network. Typical network applications include the IBM PC Network Program, Novell Advanced Netware, Ashton-Tate dBase III Plus and Microrim R:base 5000. A complementary program, the Exos 8051-02 TCP/IP, includes a socket library that provides a set of routines to allow programmers to write PC-to-host networking applications that use the TCP/IP protocol. It is based on the Unix 4.2 socket interface standard and permits communications between PCs and a variety of Unix-based micros and host computers. Both packages operate on DOS and run on the company's Exos 205 intelligent Ethernet controller board. The 8052-01 software sells for $95 and the 8051-02 socket library costs $595. **Excelan,** 2180 Fortune Dr, San Jose, CA 95131. **Circle 148**

IBM XT, AT design software supports PC version of Spice

Linear CAD II, a second-generation linear design software program, transforms an IBM XT or AT into a design workstation. Simplifying custom and semicustom linear integrated circuit design, the program features an expanded library of macro cells and device models for Micro Linear's 12-V linear bipolar process. It supports schematic capture, net list output and Pspice (a PC version of the Spice circuit simulation program). Special component interconnection requirements demanded by linear LSI design can be automatically included in the simulation models. The price is $10,000. **Micro Linear,** 2092 Concourse Dr, San Jose, CA 95131. **Circle 149**

CALENDAR

CONFERENCES

JUNE 2-5—Vision '86, Cobo Hall, Detroit, MI. INFORMATION: Vision '86 Public Relations, PO Box 930, Dearborn, MI 48121. Tel: 313/271-0777

JUNE 5-6—Robexs '86 (Robotics and Expert Systems), Gilruth Center NASA/Johnson Space Center, Houston, TX. INFORMATION: Deborah Poor, Instrument Society of America, 67 Alexander Dr, PO Box 12277, Research Triangle Park, NC 27709. Tel: 919/549-8411

JUNE 8-10—AI in an IBM World, Westin Hotel at Stamford, Stamford, CT. INFORMATION: New Science Associates, 46 Hunt Terrace, Greenwich, CT 06831. Tel: 203/531-0050

JUNE 9-13—IEEE Computer Society Tutorial Week, Quality Inn Pentagon, Arlington, VA. INFORMATION: Martez A. Camilleri, Dir of Tutorials, IEEE Computer Society, 1730 Massachusetts Ave, NW, Washington, DC 20036. Tel: 202/371-0101

JUNE 10-12—Comdex International, Nice Congress and Exhibition Centre, Nice, France. INFORMATION: The Interface Group, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600

JUNE 10-12—NEPCON East, Bayside Exposition Center, Boston, MA. INFORMATION: Show Manager, NEPCON East 86, Cahners Exposition Group, 1350 East Touhy Ave, PO Box 5060, Des Plaines, IL 60017. Tel: 312/299-9311

JUNE 16-19—NCC '86 (National Computer Conference) Las Vegas Convention Center, Las Vegas, NV. INFORMATION: NCC '86, AFIPS, 1899 Preston White Dr, Reston, VA 22091. Tel: 800/NCC-1986

JUNE 22-25—IEEE Int'l Conference on Communications, Sheraton Centre, Toronto, Canada. INFORMATION: Douglas Peck, IEEE Communications Society, 1450 Don Mills Rd, Don Mills, Ontario, Canada M3B 2X7. Tel: 416/581-4251

JUNE 22-26—Computer Vision and Pattern Recognition, Fontainebleau Hotel, Miami Beach, FL. INFORMATION: IEEE Computer Society, 1730 Massachusetts Ave, NW, Washington, DC 20036. Tel: 202/371-0101

JUNE 23-26—ATE East, World Trade Center, Boston, MA. INFORMATION: Registrar, Morgan-Grampian Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-3976

JUNE 29-JULY 2—Design Automation Conference, Las Vegas Hilton, Las Vegas, NV. INFORMATION: PO Pistilli, 23rd Design Automation Conference, 7366 Old Mill Trail, Boulder, CO 80301. Tel: 303/530-4333

JULY 1-3—IEEE Symposium on Fault-Tolerant Computing, Vienna, Austria. INFORMATION: H. Kopetz, Interconvention Hofburg, Box 80, A-1107 Vienna, Austria. Tel: 43/222-520293

JULY 7-11—IEEE Optical Computing Conference, Shoresh, Jerusalem, Israel. INFORMATION: Prof Joseph Shamir, Dept of Electrical Engineers Technion, Haifa 32000, Israel. Tel: 04-293273

JULY 20-24—ASME Conference on Computers in Engineering, Hyatt Regency Hotel, Chicago, IL. INFORMATION: Charles E. Butler & Assoc, 60 E 42nd St, Suite 541, New York, NY 10165. Tel: 212/687-2481

JULY 28-30—SCSC '86 (Society for Computer Simulation), MGM Grand Hotel, Reno, NV. INFORMATION: Rosemary Whiteside, Marketing Manager, PO Box 17900, San Diego, CA 92117. Tel: 619/277-3888

AUG 4-6—ACM Conference on Lisp and Functional Programming, Massachusetts Institute of Technology, Cambridge, MA. INFORMATION: Richard P. Gabriel, Lucid, Inc, 707 Laurel St, Menlo Park, CA 94025. Tel: 415/329-8400

AUG 18-22—ACM Siggraph, Dallas Convention Center, Dallas, TX. INFORMATION: Ellen Frisbie, Smith, Bucklin & Assoc, 111 E Wacker Dr, Chicago, IL 60601. Tel: 312/644-6610

AUG 18-22—IEEE Computer Society Tutorial Week, Marina Beach Hotel, Marina Del Rey, CA. INFORMATION: Martez A. Camilleri, IEEE Computer Society, 1730 Massachusetts Ave, NW, Washington, DC 20036. Tel: 202/371-0101

AUG 19-22—IEEE Computer Society/ACM Conference on Parallel Processing, Pheasant Run Resort, St Charles, IL. INFORMATION: IEEE Computer Society, 1730 Massachusetts Ave, NW, Washington, DC 20036. Tel: 202/371-0101

AUG 24-28—SPSE Congress on Advances in Non-Impact Printing Technologies, The Fairmont Hotel, San Francisco, CA. INFORMATION: Conference Management Corp, 17 Washington St, Norwalk, CT 06854. Tel: 203/852-0500

Announcements intended for publication in this department of *Computer Design* must be received at least three months prior to the date of the event. To ensure proper timely coverage of major events, material should be received six months in advance. Programs and dates are subject to last-minute changes.

SHORT COURSES

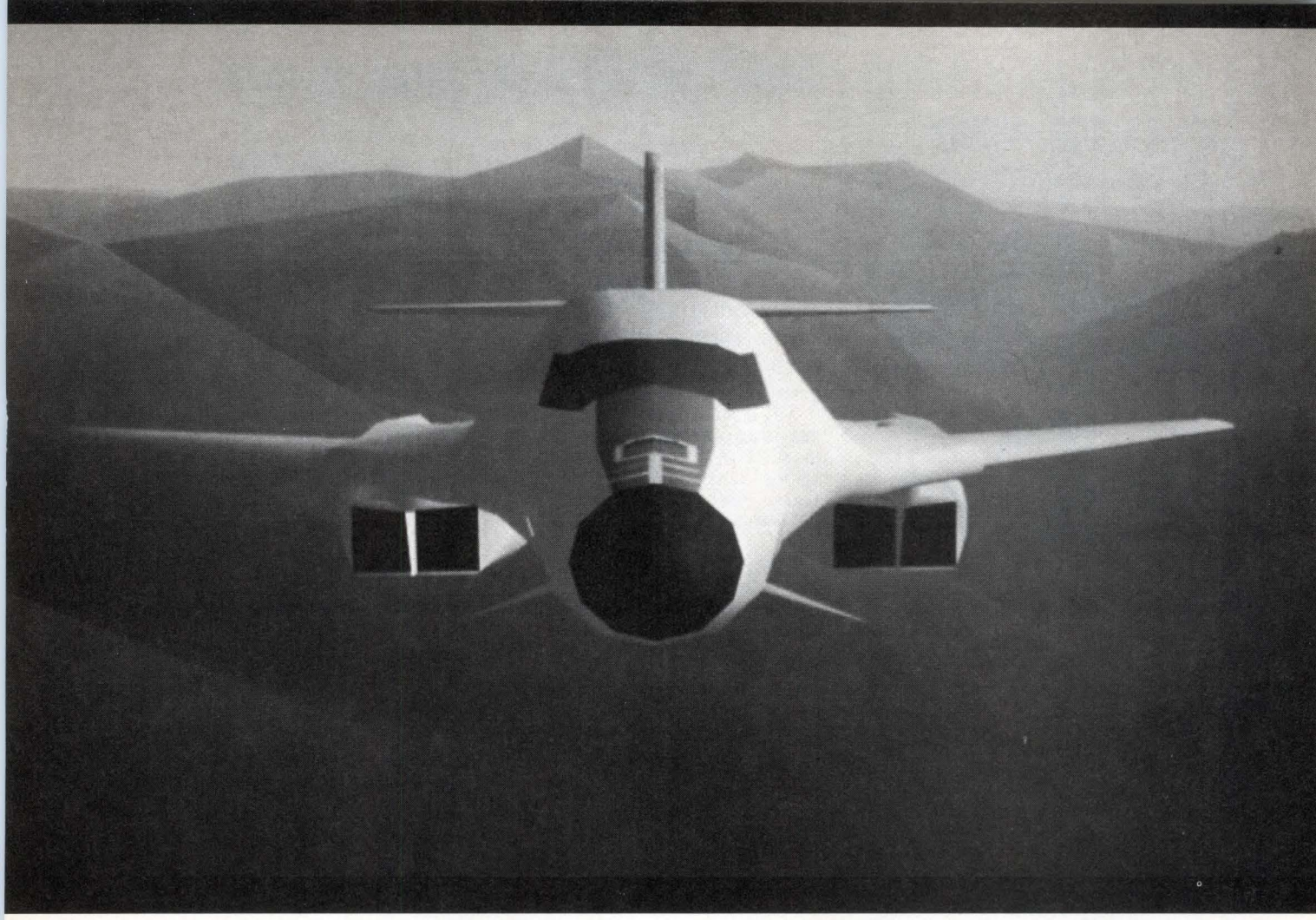
MAY 22-23—Seminar on MAP, TOP and OSI, Airport Hilton, Philadelphia, PA, **JUNE 16-17,** Back Bay Hilton, Boston, MA; **MAY 29—MiniMAP,** Airport Hilton, Philadelphia, PA. INFORMATION: Ship Star Assoc, 36 Woodhill Dr, Newark, DE 19711. Tel: 302/738-7782

JUNE 6—Briefing on Computer Integrated Manufacturing, The Marriott, Worcester, MA; **JUNE 16—Briefing on Machine Vision,** The Loews Summit, New York, NY. INFORMATION: Office of Continuing Education, Worcester Polytechnic Institute, Worcester, MA 01609. Tel: 617/793-5517

JULY 16—Seminar on Networking PCs, The Sheraton, Lexington, MA, **AUG 19,** The Charles Hotel, Cambridge, MA. INFORMATION: Joan Merrick, Boston Univ Seminar Coordination Office, Suite 415, 850 Boylston St, Chestnut Hill, MA 02167. Tel: 617/738-5020

JULY 21-25—Microcomputers in Control Systems; JULY 28-AUG 1—Internet Systems and Protocols, Washington, DC. INFORMATION: Merril Ann Ferber, Continuing Engineering Education Program, The George Washington Univ, Washington, DC 20052. Tel: 202/676-8522

AUG 20-22 and 25-27—SME Workshop on Applying Machine Vision to Your Manufacturing Process, Cambridge, MA. INFORMATION: Joanne Rogers, Society of Manufacturing Engineers, Box 930, Dearborn, MI 48121. Tel: 313/271-0039



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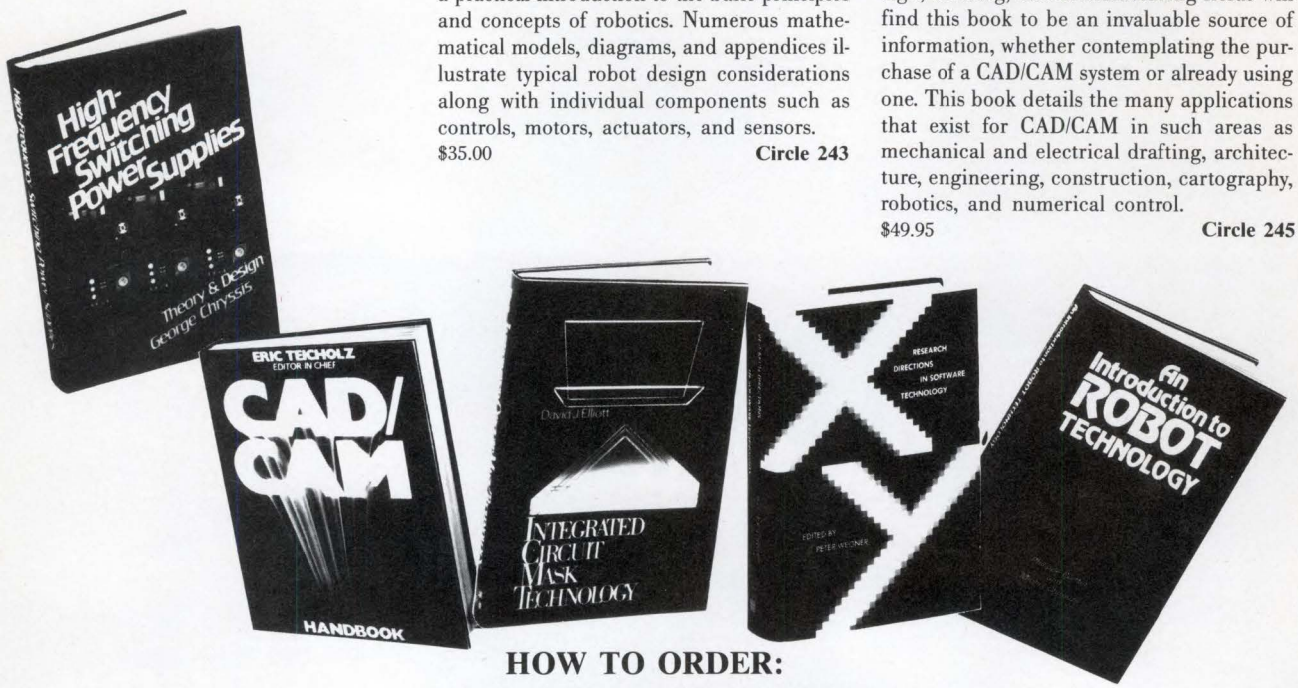

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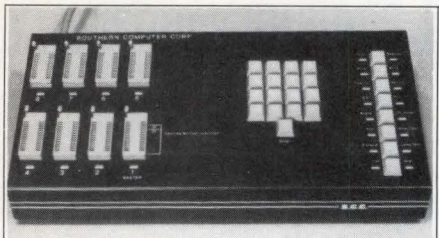

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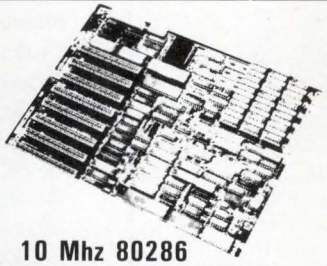

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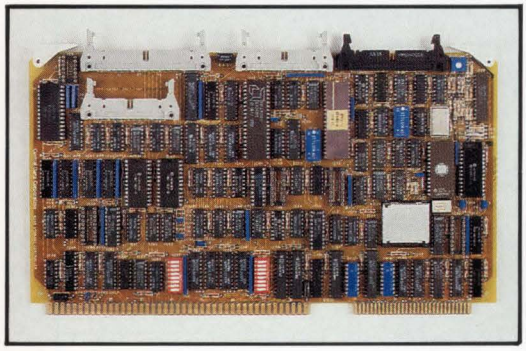

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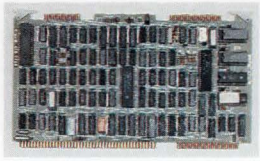

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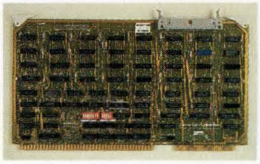

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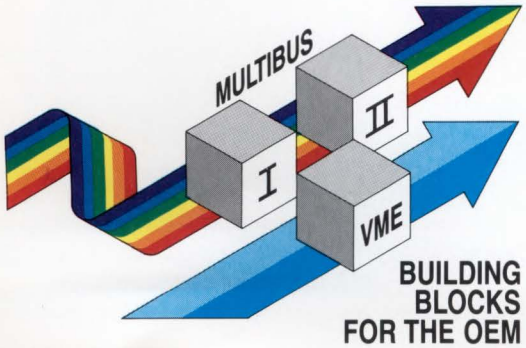

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