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FEBRUARY 1985

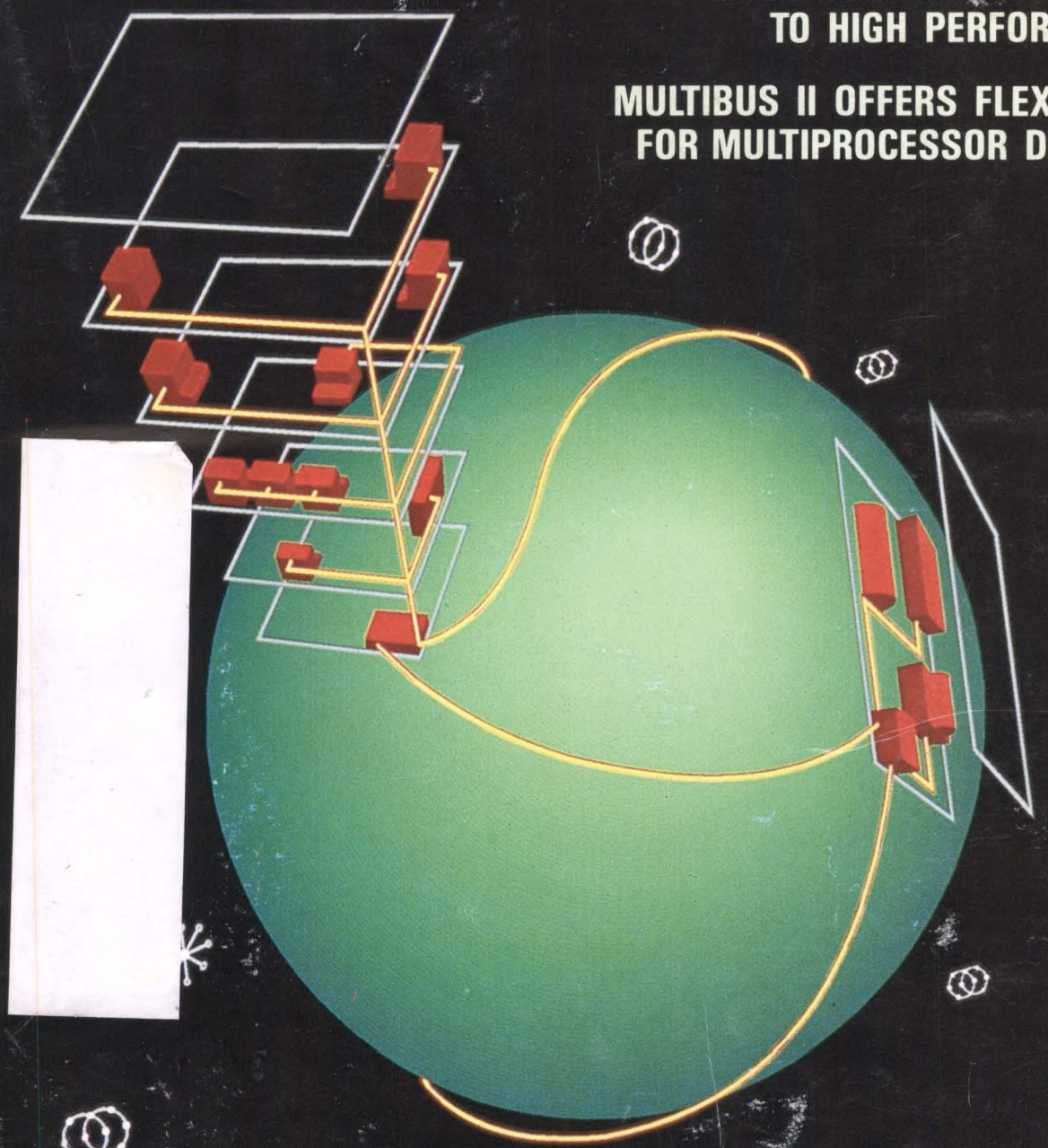
COMPUTER DESIGN

DATA COMMUNICATIONS

LASER PAGE PRINTERS FACE NEW COMPETITION

BIPOLAR BLOCKS STACK UP TO HIGH PERFORMANCE

MULTIBUS II OFFERS FLEXIBILITY FOR MULTIPROCESSOR DESIGNS



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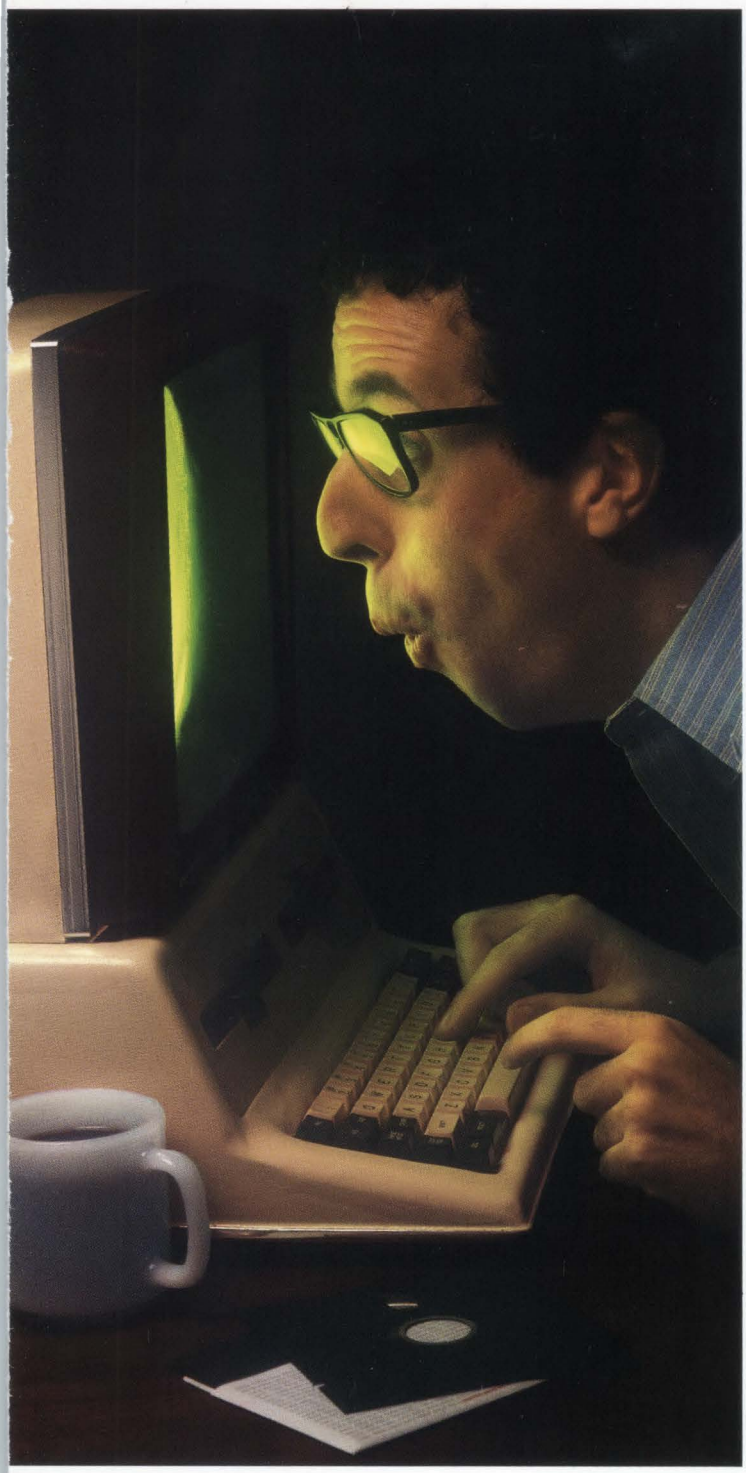

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CIRCLE 1

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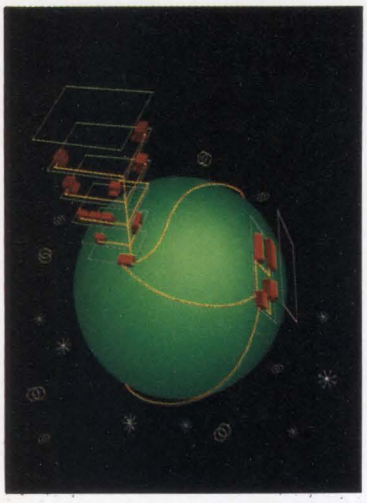


This month's cover was designed and illustrated at Coddbarrett Associates using a DICOMED D-38 design station and a D-48 high resolution film recorder.

SPECIAL REPORT ON
DATA COMMUNICATIONS

97 Network interconnection has become a software-intensive activity in data communications. As more local area networks are created, more opportunities arise for software solutions that tie LANs to wide area networks. Each new opportunity, in turn, presents a new challenge for the network designer. This special report explores the latest frontiers in network design.

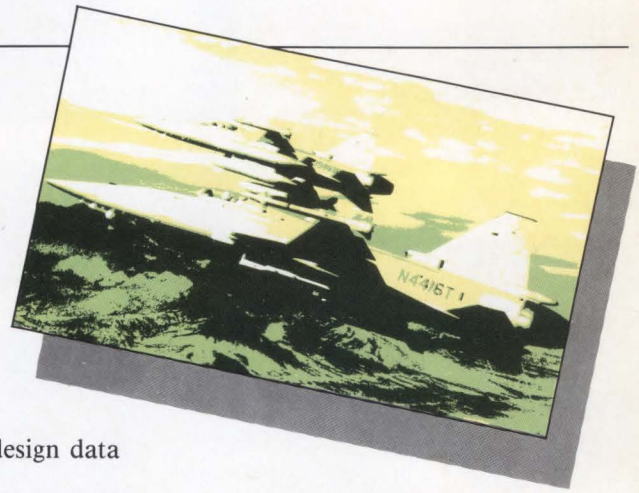
99 **LANs team up to widen the network connection**
The next step in creating a global network is developing protocols to match those of different local area networks.

125 **Gateways link assorted networks**
Connecting identical networks is straightforward, but handling different types of networks with multiple protocols, priorities, and multiplexing calls for gateways.

137 **X.25 standard simplifies linking of different LANs**
Interconnecting with the X.25 protocol allows networks to encompass different local area network configurations in wide area, packet-switching systems.

143 **Choosing the best local area network for any application**
Regardless of the application, a LAN that adheres to some standard provides the most cost-effective, long-term approach to networking.

151 **Controller IC contends with multiple protocols**
The most widely used data communication protocols are now supported by a single-chip controller that requires minimum external hardware.



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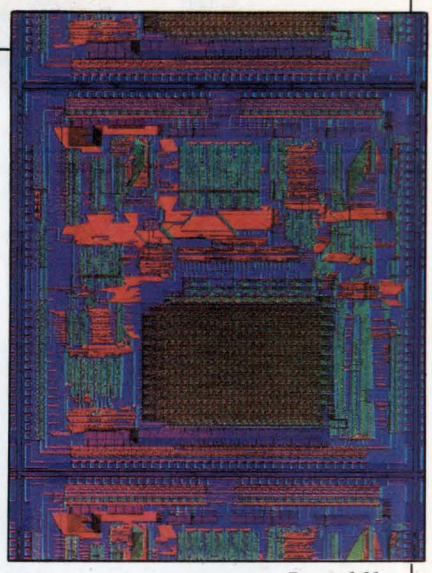

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SYSTEM DESIGN

161 Integrated circuits: **Building blocks stack up to high performance**
Designed using concepts of functional partitioning, three-bus architectures, and fault detection, a family of 32-bit building blocks can satisfy the needs of both general-purpose computing and signal processing.

171 Interface: **Multibus II designs exploit advanced bus concepts**
With several bus architectures available, designers face the problem of choosing one that provides the features and flexibility needed for new multiprocessor designs.

181 Computers: **Computers tailored to efficient expansion**
Sharing utilities and applications as well as automatic code and data segmentation can give today's user needed power. Future computing, however, requires virtual machines that can handle multistate architectures.

SYSTEM COMPONENTS

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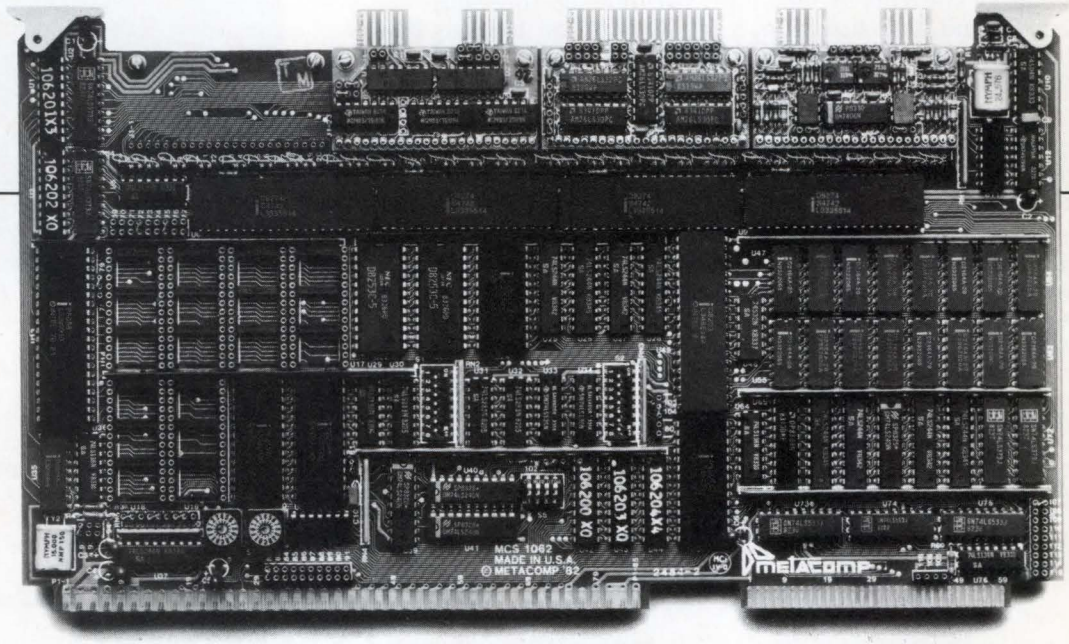
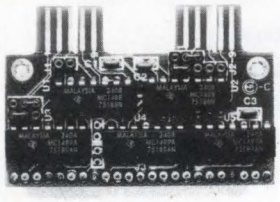


Get eight channels of intelligent slave serial I/O with this new wave Multibus controller



The versatile California Serfboard, MCS-1062, is the first serial I/O controller with eight intelligent slave channels. Plus all the features highlighted below. That's double the typical capacity in a single cardslot. And the on-board CPU means performance and programmable flexibility that leaves the competition treading water.

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CIRCLE 3

UP FRONT

Silicon Graphics predicts an end to current graphics standards

New workstations may render existing graphics standards obsolete, according to Silicon Graphics founder and chairman James H. Clark. "The problems normally addressed by graphics standards like CORE," the former Stanford University computer science professor pointed out, "involve communication between a graphics terminal and a host." But Clark said he expects that kind of system to be replaced by workstations such as Silicon Graphics' new Iris 2000 series. Built around VLSI "geometry engine" chips, the Iris workstations avoid using bit-mapped graphics in favor of a parallel pipelined architecture that calculates as many as 100,000 vertices/s. As such computation-intensive workstations become more common, Clark said he thinks the current tendency to treat graphics protocols as common data structures will give way to lower level graphics primitives. Essentially geometric, these primitives will execute directly on future graphics hardware, such as Silicon Graphics' geometry engine.—*W.E.S.*

Microprocessor operating system standard makes the draft

The much-debated microprocessor operating systems interface standard may finally become official—at least in its basic form. Draft 6.2A will be considered by the IEEE's Standards Board next month. Work continues on language bindings for Pascal, Ada, C, Fortran, Cobol, and PL/M as well as an extension of the standard to handle memory management and device I/O. Computer designers who want to take part or comment on the standard should call MOSI chairman Don L. Jackson at 602/438-3163.—*H.H.*

"Hackers' Mac" promises open architecture

Hobbyists and professionals in Palo Alto, Calif are developing a Macintosh-like computer with an open architecture. They hope it will encourage the manufacture of compatible products. The machine, appropriately called the "Hackers' Mac," will not be plug-compatible with the Macintosh, nor will its operating system be identical. It will, however, feature a multichannel DMA port and onboard expansion. The designers intend the architecture and operating system to be sufficiently compatible to allow porting applications from the "Hackers' Mac" to the Macintosh, with only a slight loss of features.—*T.R.W.*

Semiconductor startup offers nonvolatile RAM cartridges

A new company with a new idea, Dallas Semiconductor (Dallas, Tex), is offering nonvolatile RAM cartridges that plug into computer memory boards. These cartridges—compatible with JEDEC-standard, 25-pin DIP sockets—can be used for software updates, system configuration, or secondary storage. The first cartridges available will provide 64 Kbytes, 128 Kbytes, or 256 Kbytes of RAM. They will use embedded lithium cells in DIPs to retain memory contents for up to 10 years, according to the company.—*R.G.*

UP FRONT

Superminis battle for supremacy

To maintain their niches in the processing hierarchy, manufacturers of 32-bit computers are tweaking and tuning their machines for higher performance. Data General (Westboro, Mass) plans to push its MV/10000 to 3.5 million instructions per second, while Prime Computer (Natick, Mass) will squeeze 4 MIPS from its model 9955. Not to be outdone, Perkin-Elmer's Computer Systems Div (Oceanport, NJ) just dropped a price/performance bombshell: a 32-bit system based on the 3200 series processor for under $17,000. At the high end of the series is the 3260 MPS, a tightly coupled 10-processor configuration that adds I/O processors to the CPU/multiple-APU array to gain performance. Another Perkin-Elmer machine, code-named "Cruncher," promises further competition for Digital Equipment Corp's VAX 8600 next month.—*P.K.*

Portable applications targeted by 8-bit CMOS CPU

A new CMOS microprocessor from Hitachi America (San Bruno, Calif) aims at powering portable, low power CP/M systems while reducing chip counts and addressing larger memories than current 8-bit CPUs. The 6-MHz HD64180 will incorporate a memory management unit as well as a two-channel DMA controller. The onchip MMU will give the HD64180 direct access to 512 Kbytes of RAM, which can be refreshed by an onchip dynamic refresh circuit. The processor retains object code compatibility with the 8080 and Z80. Twelve additional instructions will provide a sleep mode, an 8-bit multiply with 16-bit result, immediate I/O address-to-register transfers, and block address increment and decrement.—*T.R.W.*

MS-DOS fever hits minicomputers

It used to be that minicomputer programs were scaled down to run on microcomputers. Now, the reverse is also true. The MS-DOS microcomputer operating system has such an extensive array of application software written for it that new coprocessor systems run MS-DOS software on Digital Equipment Corp's Q-bus and Unibus-based minicomputers. Among the firms providing PDP-11 or VAX hardware to perform this chore are Logicraft (Nashua, NH), Decmation (Santa Clara, Calif), and Virtual Microsystems (Berkeley, Calif). The hardware uses Intel 8086/8088 microprocessors and DOS emulation while running under various DEC operating systems.—*H.H.*

Odd sample sizes no problem for new FFT algorithm

Whitman Engineering of Maitland, Fla has announced a fast Fourier transform algorithm that runs on the IBM PC, Texas Instruments Professional, Apple II, and other personal computers. The algorithm is incorporated in a software package called MADCAP (modular access design, computer aided processing) that includes a synthesizer/signal generator and special-function generators. Company president Joanne Smith describes the MADCAP package as "a signal processing laboratory in software." A special version of the MADCAP

(continued on page 8)

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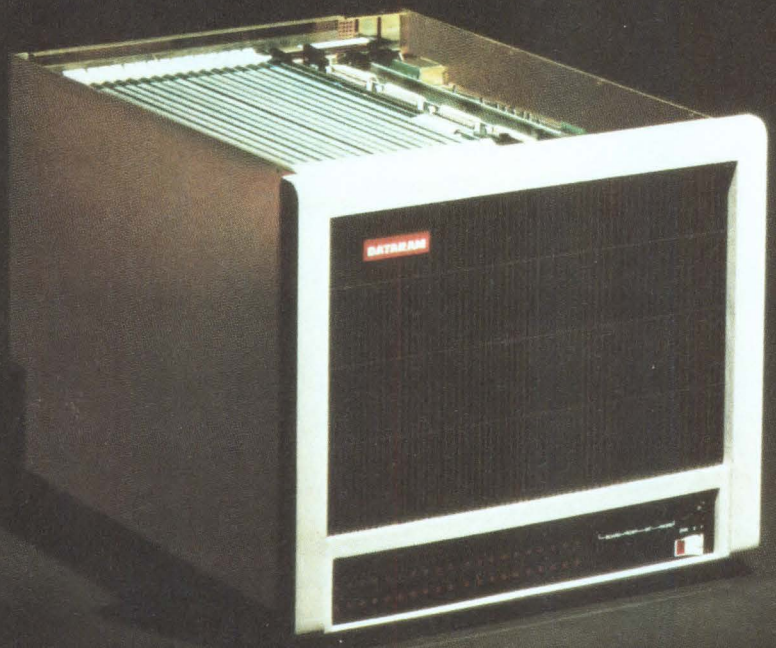

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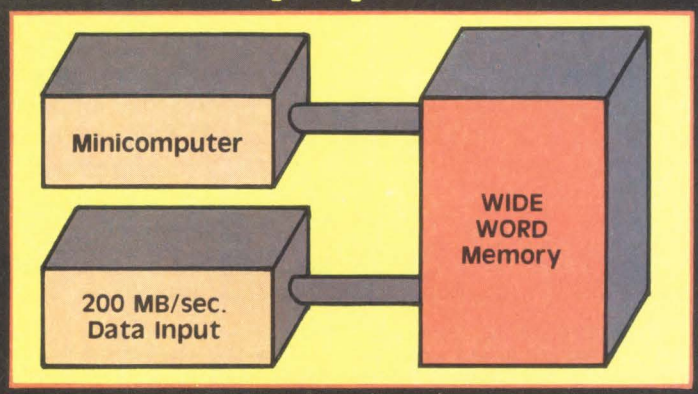

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(continued from page 6)

package serves as a product development system for TI's TMS320 signal processing chip. The new algorithm's main advantage is its ability to process a wide range of sample sizes without distortion. The algorithm also processes a given odd sample size more quickly than other FFTs. Further, the smaller samples reduce memory requirements.—*W.E.S.*

Automation veteran forms CAE firm for mechanical design

Philippe Villers has done it again. The cofounder of Computervision (a manufacturer of computer aided design equipment) and of Automatix (a robotics company) now has created Cognition Corp. This company, temporarily quartered in Burlington, Mass, will develop and produce mechanical computer aided engineering equipment. After September, the company will move to Billerica, Mass, "close enough to Automatix to permit me to get to board meetings," says Villers, who remains chairman of the board of that company. By Villers' definition, CAE is "the preliminary or conceptual design stage, basically analysis and synthesis. It precedes CAD, which is the execution stage. CAE is for engineers, CAD is for designers and draftsmen." Villers says electrical CAE is only about three years old, grosses approximately $200 million, and is growing at a rate of 70 percent annually. "Mechanical CAE needs to be born," he says, "and it eventually will be even bigger than electrical."—*S.F.S.*

Digital Research forsakes Unix as 80286 port is validated

AT&T and Intel have validated Digital Research's (Pacific Grove, Calif) port of Unix System V, version 2, for the Intel 80286 microprocessor. The Digital Research version will be marketed by Microport Systems, Inc (Pacific Grove, Calif), a recent spin-off from Digital Research, as well as by Unisoft Systems (Berkeley, Calif) and Interactive Systems (Santa Monica, Calif). The spin-off marks Digital Research's disinvolvement with Unix. The firm reportedly wants to concentrate on the Graphics Environment Manager and its Concurrent DOS series of operating systems.—*H.H.*

Custom chip set to back up MAP standard

Two original supporters of General Motors' Manufacturing Automation Protocol are jointly developing a three-chip set that will implement the IEEE 802.4 token-passing network standard. Concord Data Systems of Waltham, Mass and Gould's AMI Semiconductors (Santa Clara, Calif) say the three-chip set will interface with major 8- and 16-bit microprocessors. The set comprises a data chip with baseband or broadband modem interface, a DMA interface chip, and a protocol controller chip linked by a private bus.—*S.F.S.*

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CIRCLE 5

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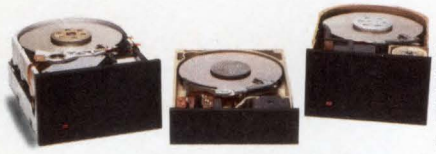

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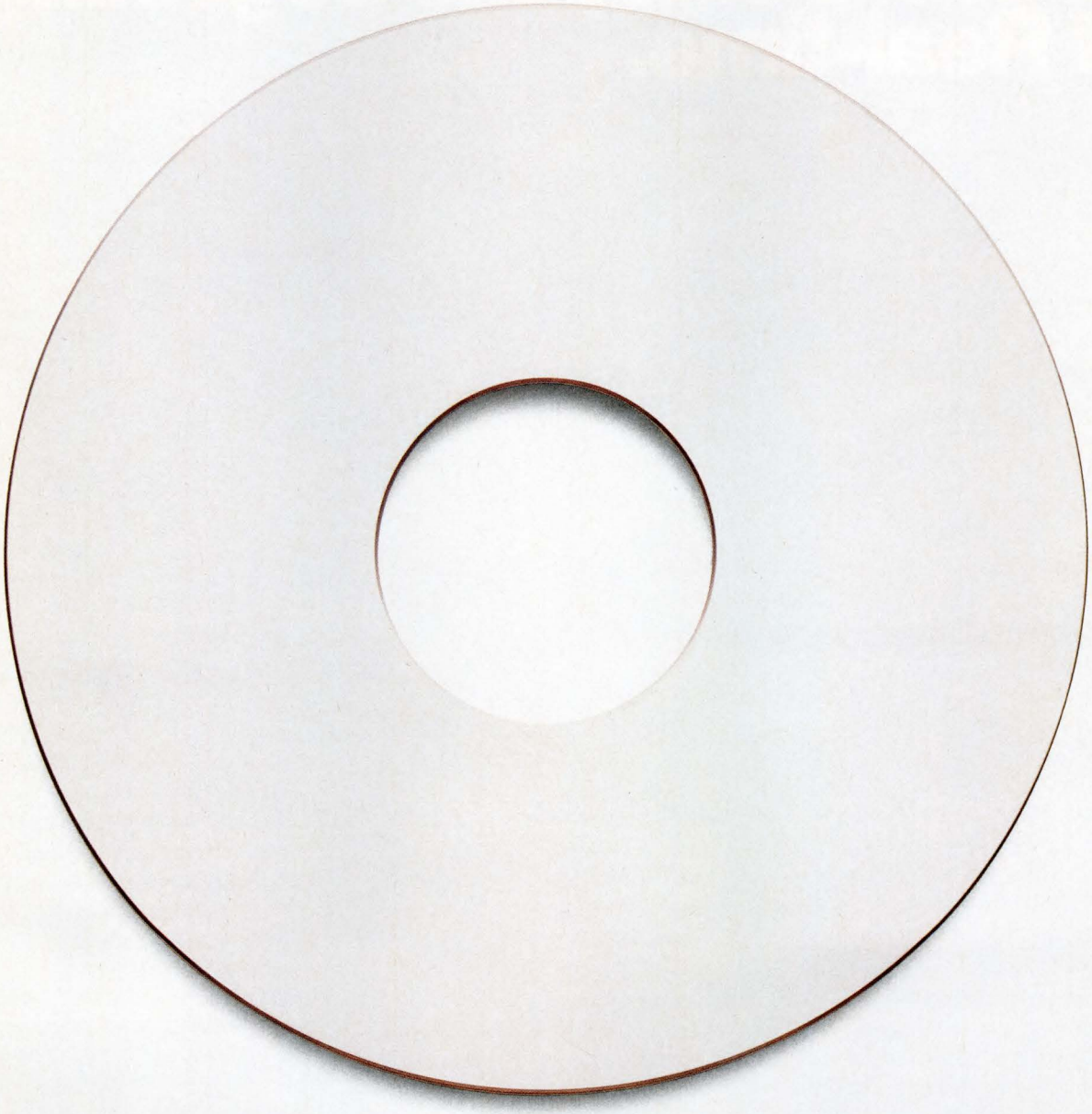

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CIRCLE 7

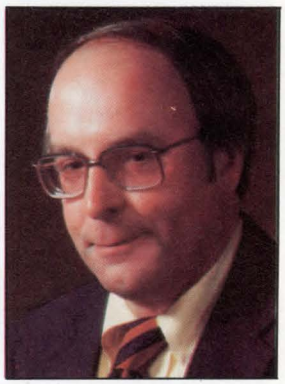
FAREWELL TO AN OLD FRIEND

Those of you with a keen eye for detail may have noticed a change on the cover of *Computer Design*. At the beginning of the year, we removed the tag line, "The Magazine of Computer Based Systems," from beneath the magazine's logo. Unfortunately, our old friend who served us faithfully for many years became yet another victim of progress. We can assure you, though, the disappearance of the tag line does not signal any change in the magazine's role. Rather, it is an indication that, while our charter has stayed essentially the same, both the computer and magazine industries have undergone dramatic changes. We shall continue to do what we have always tried to do during 22 years of publication—provide the essential information you need to design better computer systems.

If you are reading your own copy of this magazine and not somebody else's, then you must be either an engineer or engineering manager involved in the design of computer systems. This role for readers of *Computer Design* never changed. Two things did change, however: the types of computer systems you design and the types of magazines that compete for your attention. Subsystems forming the nucleus of larger computer systems now exist at the chip, board, and box levels. And computer systems are designed and integrated not only by original equipment manufacturers, but also in many other types of organizations such as system houses and sophisticated end users. Furthermore, today's computer systems require both hardware and software design at all stages of the development. Moreover, most systems involve communications, information display, and storage in addition to digital processing.

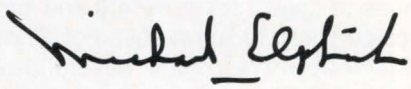
One fact remains amid all this potential for confusion: wherever real design work must be done, design engineers will be doing it. Hence, the central role of *Computer Design*. While other magazines serve, say, software designers but not hardware designers, or value added resellers but not OEMs we continue to serve the design engineers and their managers wherever and however they design computer systems.

So why was our tag line added and why was it removed? Back in the days when the only processors were mainframes and minicomputers, people sometimes wondered whether *Computer Design* served people who designed computers or people who designed *with* computers. The answer then, as today, was "both." But, in a sense, the magazine was ahead of its time. Obviously, there was a vast difference between the information needs of engineers who designed circuits at the device level and those who designed complete systems. Therefore, the tag line was added to show that *Computer Design* was aimed at the senior engineers and project managers who designed at the system level. The development of the microprocessor and related chip-level subsystems, of course, blurred the distinction between system design and design at the component level. More recently, design automation of custom chip-level systems has obliterated any remaining distinctions between digital circuits and digital systems. So, we decided to bid farewell to our old friend the tag line.

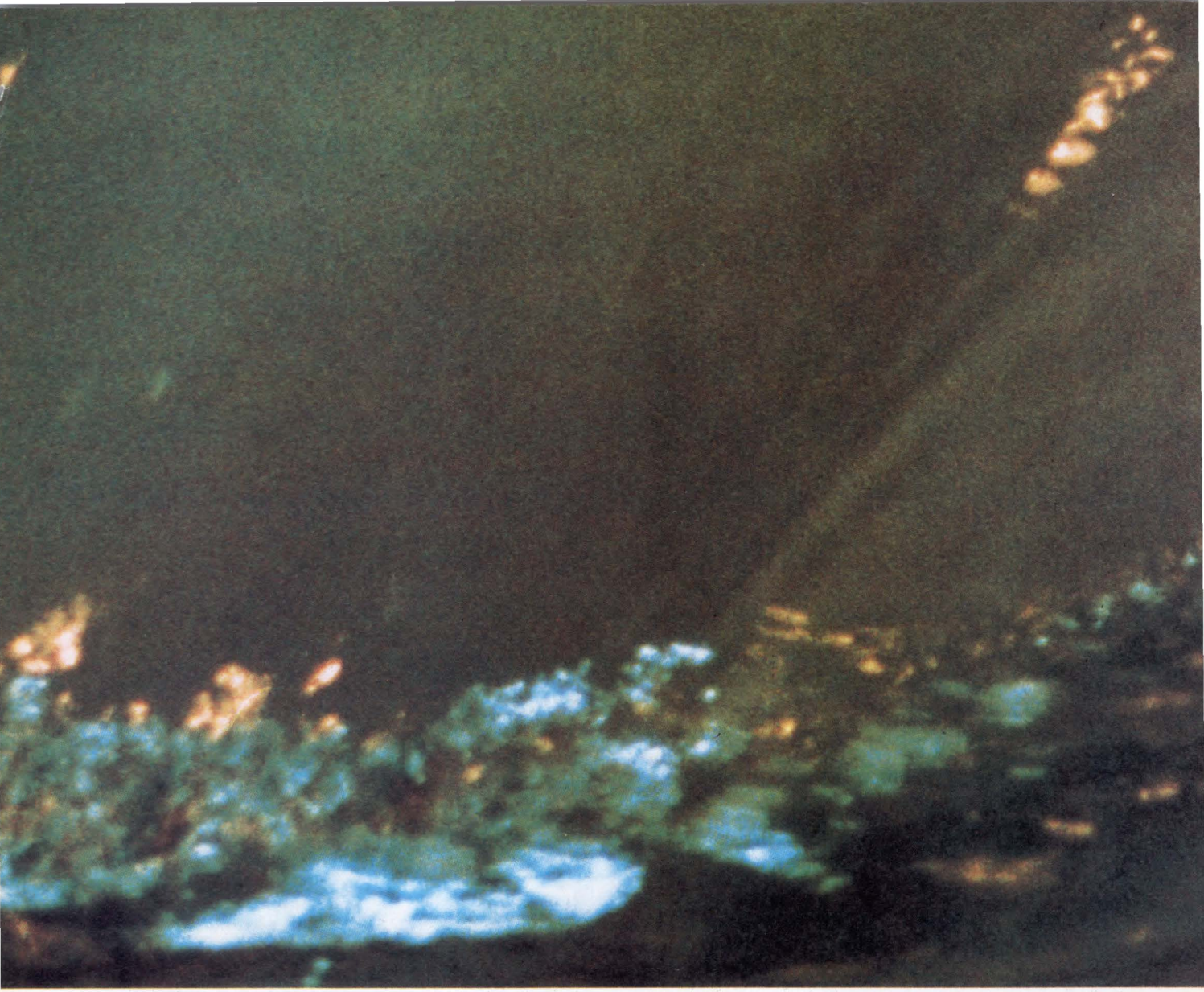


Industry trends had conspired to make our tag line both misleading and seemingly arrogant. The line implied that the magazine was devoted only to system integration and not to system design. Also, it implied that it was the *only* magazine serving system integrators. However, during recent years, other magazines have emerged to compete with *Computer Design* in that area—though not in all areas. We think the magazine is unique in other ways, but we can no longer claim to be the only one serving system integrators. We think our uniqueness was better expressed in a longer tag line we have used in promotion pieces aimed at potential advertisers: "The only computer magazine that concentrates on design; the only design magazine that concentrates on computer systems."

Perhaps a new tag line—one that succinctly summarizes our purpose—will replace our old friend. But, for now, we believe that *Computer Design* says it all.



Michael S. Elphick



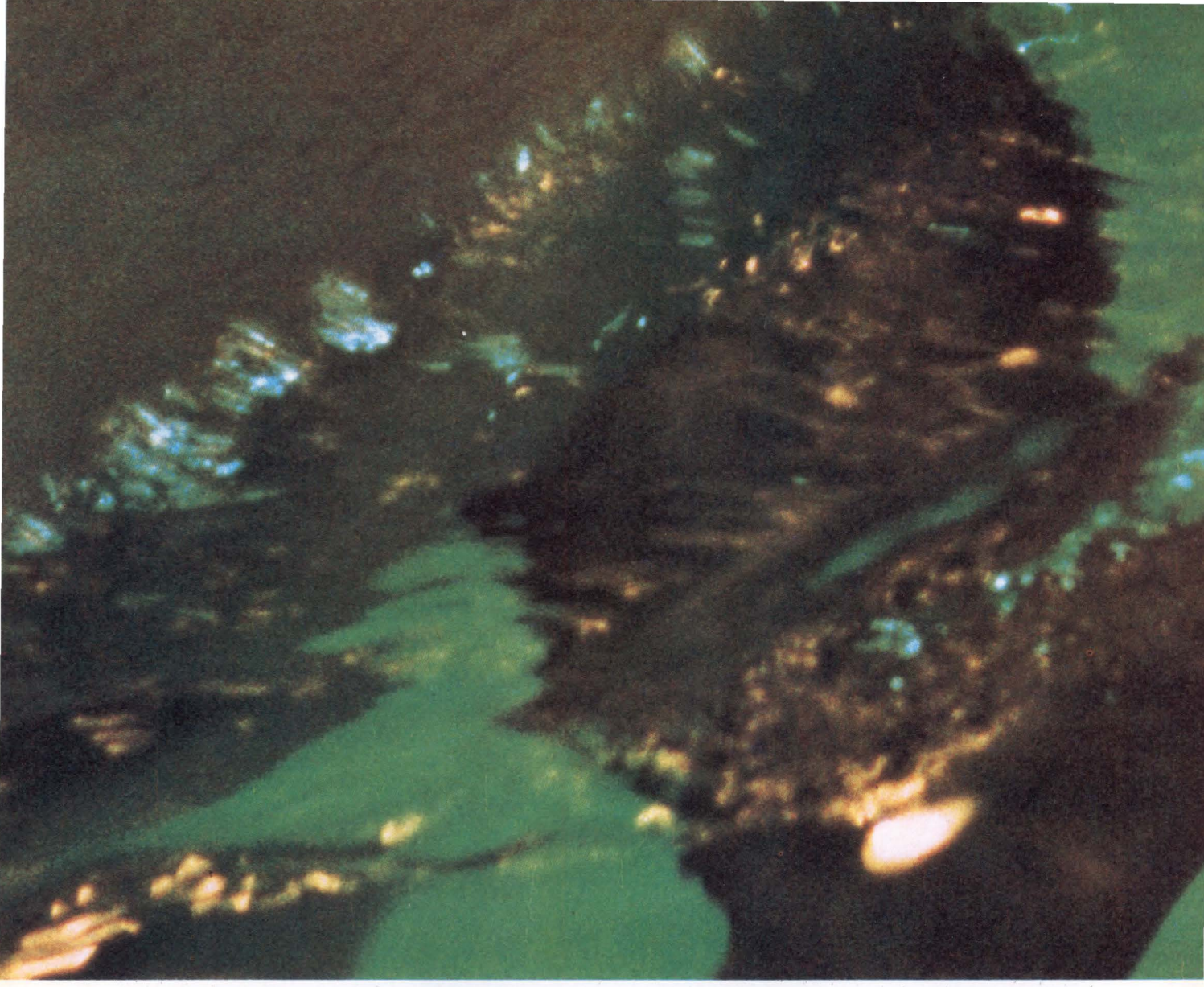
INMOS has natural answers

High-volume production of our new 80ns how we accelerate your designs.

Some creatures are in their natural element when it comes to speed. It's breeding and conditioning that have enabled them to jump ahead of all other species. Speed is inherent in their sleek, natural design that surfaces with sudden bursts of energy, in play or in flight.

In keeping with the natural design for speed, our new 80ns 64K x 1 DRAM has evolved as the fastest member of our entire high-performance DRAM family. This new DRAM chip is available with 80ns, 100ns or 120ns $\overline{RAS}$ access times and 130, 160 and 190 cycle times. The part also offers other exceptional features that are common only to the INMOS DRAM line. $\overline{CAS}$-before-$\overline{RAS}$ refresh, for example, as well as nibble mode are delivered as standard features and at no extra cost. We also furnish a military version of our new 64K DRAM that's qualified to MIL-STD-883C.

Our 16K x 4 DRAM is another outstanding chip in our DRAM selection. You can choose 100ns, 120ns or 150ns access time and count on exceptionally high memory bandwidth. In addition, we offer you our 8K x 8 DRAM with 120ns, 150ns or 200ns access time and pin-1 refresh. Its byte-wide organization can boost the performance of the latest microprocessor system.



on speed.

64K DRAM is just one example of

You'll also get the flexibility in packaging you expect from our capable DRAM family. Anything from low-cost plastic DIPs to ceramic side-brazed editions, including leadless chip carriers.

The point is, it pays to go to the leader where DRAM development, production and delivery are simply faster by nature. To the company that can give you the world's broadest DRAM family line with more choices of speeds and organizations.

If you have questions on which member of our DRAM field can help you win your design race, just ask us.

We'll be quick with in-depth answers that will fill you in on the rest of our picture.

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CIRCLE 8

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CIRCLE 11

Microprocessor programming made simple.

"Keep it simple" was the principle of the 14th Century English philosopher William of Occam and it has even more validity today. Faced with the problems of sophisticated computer systems, designers have found that ever more complex programming languages are further complicating their tasks. Until now.

Occam. Created for system design and implementation.

When we started designing our new VLSI family of 10-MIP transputers, we built on William's simple philosophy. To take advantage of the possibilities opened up by the transputer, we needed to create a language capable of properly addressing parallelism and multiprocessor systems.

With the ability to describe concurrency (whether timeshared or real) and to handle message-passing at the lowest level of the language, all aspects of a system can be described, designed and implemented in occam. From interrupt handling through signal processing to screen editors to artificial intelligence. And on.

But occam is not limited to our transputer family. It provides an efficient, responsive implementation language for systems built on today's microprocessors. It also opens up future possibilities with its performance-enhancing multiprocessor capabilities. And INMOS now offers a product to let you exploit occam's total capability in your system.

Simplify your job with the Occam Programming System.

The Occam Programming System (OPS) gives you the tools for complete VAX / VMS software development. This package includes an integrated editor / checker, an optimizing VAX compiler and full documentation. This gives you a supportive environment for the development of occam programs for execution on the VAX. Cross-compilers for 68000 and 8086-based systems will also be available.

What's more, the occam programs developed and proven on the OPS will give you a head start for work with the INMOS transputer. Extensions to the OPS will be available which will allow occam programs to run on the transputer.

And if you have a requirement to program the transputer in other popular high-level languages, other extensions will include compilers for C, Fortran, and Pascal.

Get started today.

Contact us for our information pack on occam, the Occam Programming System and the transputer. You'll be surprised how simple your life can be.

For quick response, call us at (303) 630-4000 or write: Occam, P.O. Box 16000, Colorado Springs, CO 80935.

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WE COULDN'T OVERPOWER THE 8051. SO WE UNDERPOWERED IT.

The Intel 80C51 8-bit microcontroller. Featuring the powerful performance of the world standard 8051, but needing only one-tenth the energy.

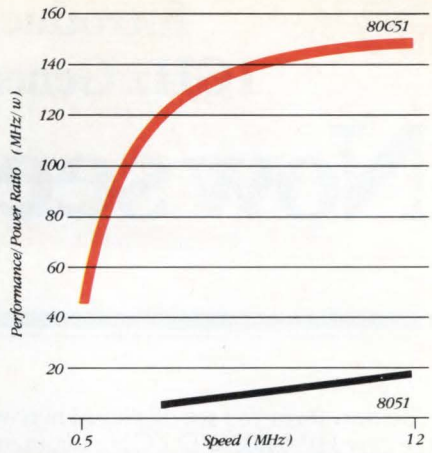
The 80C51 is based on Intel's revolutionary CHMOS technology. Achieving the high performance and high integration of HMOS, with the low power advantages of CMOS.

The result is an 8051 pin-compatible microcontroller with the most powerful eight-bit CPU and the highest level of integration available. The 80C51 runs on an incredible 11mA at 8MHz clock frequency. Average power dissipation can be lowered into microamp range, by using one of two new software programmable power control modes. In the power down mode, current drain is 50 microamps.

On the performance side, the 80C51 has a maximum clock rate of 12MHz.The fastest data throughput of any CMOS microcontroller.

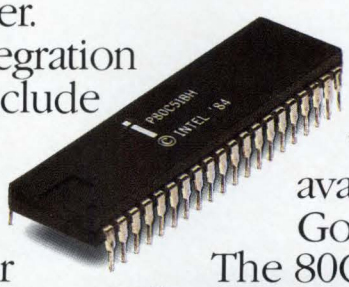
Its high integration capabilities include 4K byte ROM and 128 byte RAM, a Boolean Processor able to manipulate 256 individually addressable bits, a versatile serial port and a pair of 16-bit counter/timers.

All this helps to make the 80C51 ideal for high end eight-bit applications ranging from hand-held instruments to factory line powered controllers, to portable communications systems. A military version of the 80C51 will be available soon.



The 80C51 microcontroller delivers the highest performance per watt over the broadest frequency range in the industry. Giving you control over speed and power.

The 80C51 also boasts the world standard in development tools. Like the Series II/ICE™-51 emulator and the iPDS™ system/EMV-51. As well as a relocatable assembler and high level languages. MCS-51 workshops are available, too.



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Because now, running with the very best requires very little energy.

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CIRCLE 13

Introducing the HP 54100A/D 1 GHz General Purpose Digitizing Oscilloscope.

Now see waveforms you've

The waveform you see displayed here was captured by the new HP 54100A/D 1 GHz Digitizing Oscilloscope. It shows an intermittent extra pulse at the Q output of a D flip-flop. Plus, it automatically positions the event of interest in the center of the display and shows the events in negative time that led up to the trigger. The new HP 54100A/D can easily capture rare events like this and hold them for you to analyze with no blooming or fading. What's more, you get this with 10 psec resolution and 1 GHz bandwidth necessary to capture sub-nanosecond transistions in today's high speed logic designs. And it does all this at the touch of a button.

The first truly general-purpose digitizing scope for dc to ECL.

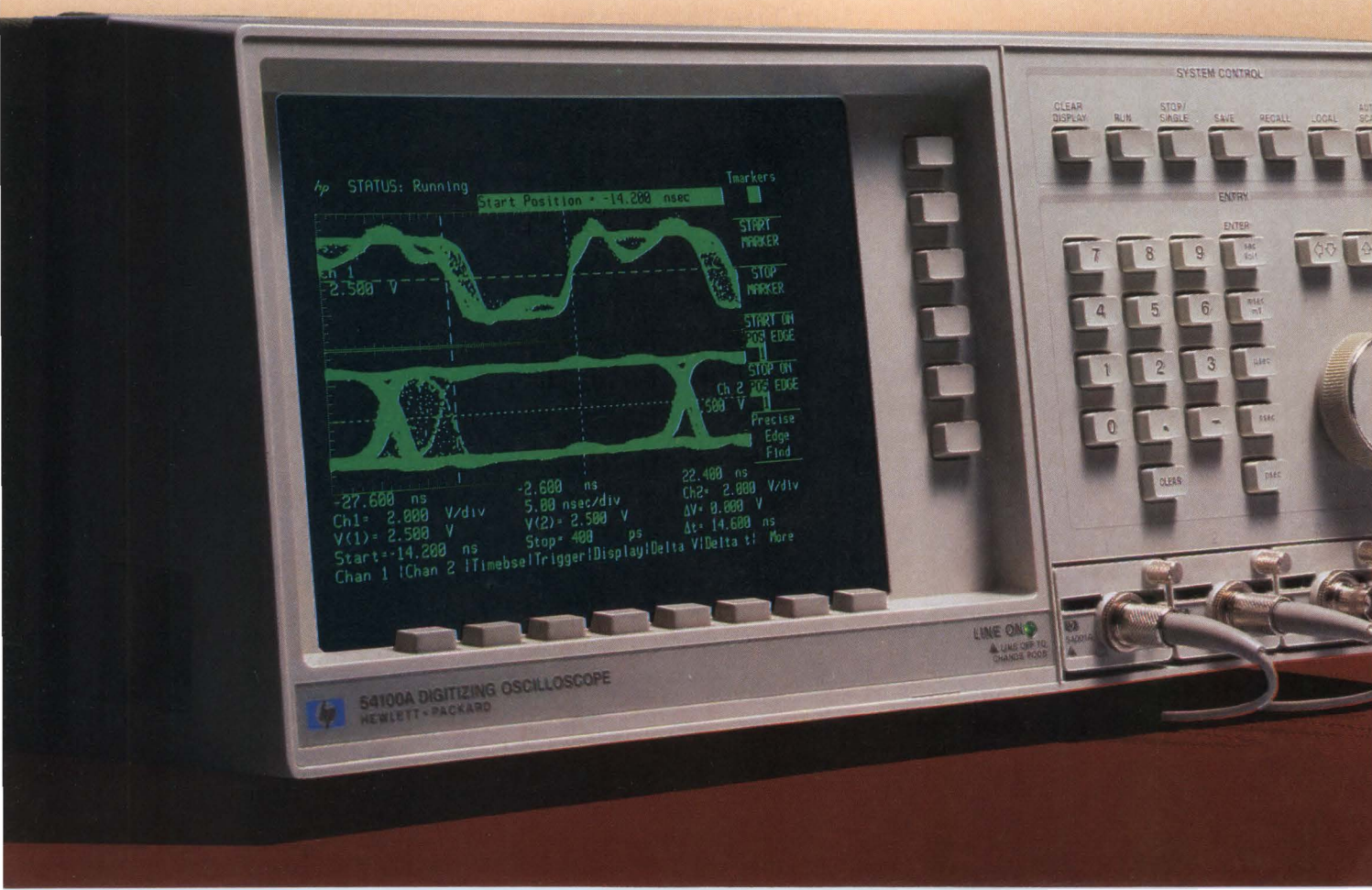
With logic speeds pushing faster all the time, you need a scope that can deliver reliable measurement results from dc all the way to ECL. The new HP 54100A/D 1 GHz Digitizing Oscilloscope gives you that versatility. It combines a fast 350 psec rise time with a crystal-controlled timebase, sophisticated on-board analysis firmware, and easily re-configured inputs. It lets you see low duty-cycle signals with clarity and brightness not previously possible. You can even take it out of the lab into production. Make it a vital part of your computer-based ATE test system for even greater productivity and usefulness through HP-IB.

Complete one-button characterization of your high-speed waveforms.

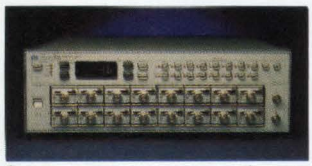
With the HP 54100A/D Digitizing Oscilloscope, you can be productive as soon as you sit down in front of it. Simple keystroke sequences give you automatic pulse parameter measurements, automatic signal scaling and instrument setup, automatic hardcopy output (over HP-IB) and more. You can trigger on logic patterns,

DESIGNED FOR HP-IB SYSTEMS

HP-IB: Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a measurement system.



never seen before.



time-qualified patterns or state, or you can delay the trigger by edge count or absolute time. The HP 54100A/D unloads much of the setup and test burden from you so you can devote your time to designing.

Expanded probing capability and convenience.

Designed as a companion product to the HP 54100A/D, the new HP 54300A Dual 8:1 Probe Multiplexer expands your scope's two inputs to a total of 16. Use it as a front-end interface for your production ATE test system or as a bench test system for design characterization in your R&D lab.

High frequency, high impedance probing.

Whether you're in R&D or production engineering, you know the need for better, more flexible probing schemes. With the HP 54100A/D or the HP 54300A Probe Multiplexer, you can choose from 1 GHz miniature probes, 50 ohm BNC inputs, or high-impedance 1 Mohm/300 MHz probes. Automatically setup and recall up to 100 test sequences of up to 99 steps each (3700 steps maximum), either from the front panel or under HP-IB control.

Call HP today.

For more information on the HP 54100A/D 1 GHz Digitizing Oscilloscope or the HP 54300A Probe Multiplexer, contact your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

HEWLETT PACKARD

0801507

CIRCLE 14

Kontron Logic Analyzers:

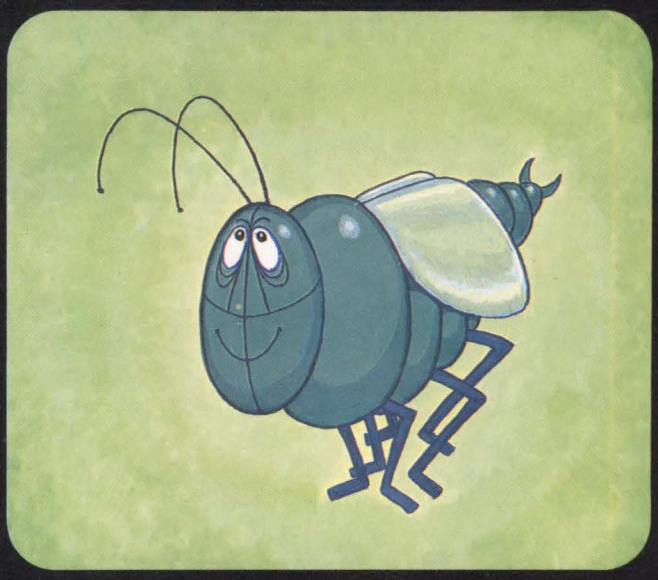
Kontron's new Series III Logic Analyzer is the ideal tool for debugging digital products, taking you into the deepest forest, up the tallest trees, in pursuit of the rarest leaves bearing the most exotic bugs.

Survey more of the "forest"
With memory depth of 8K, and up to 64 inputs, the Series III captures *4 times* as many samples per recording as any major competitor. Capturing more samples means a better overview of the target system's operation, and clearer insights into the cause of system faults.

Choose your "trees"
Kontron's advanced triggering scheme doesn't force you to go through complicated routines for simple measurements. And, for more complex requirements, the Series III makes the most sophisticated measurements of any logic analyzer *ever.*

Clutching leaves in the wind
Sampling rates to 100 MHz (standard) and 500 MHz (optional) are fast enough for capturing the briefest intermittents. Grab more data and multiply effective recording time with *transitional* recording and high resolution time measurement.

A better bug trap.
Every bug is different, and many can only be caught by combining advanced recording features. Kontron's Series III is *modular* and configurable to cover the broadest range of applications possible; from mainframe to microprocessor system development, and from high-speed custom IC design to GPIB and RS232 communications analysis.



Locate Bugs Efficiently.

Have it your way.
The Kontron Series III is available in stand-alone configurations, as an integral part of our Kontron Modular Workstations, or for maximum economy, as *the* Personal Logic Analyzer hosted on your IBM PC.

For more information, contact
KONTRON ELECTRONICS INC.
630 Price Ave.,
Redwood City, CA 94063,
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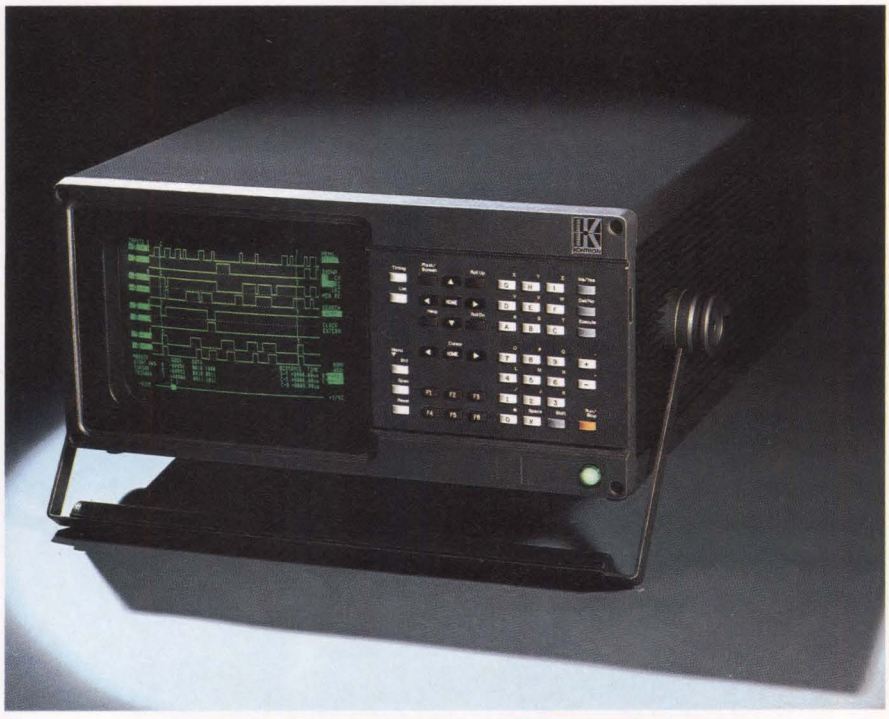
We'll get you out of the woods.



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CIRCLE 15

This New Fiber Optic Modem will Extend a DCE Interface to Any Point in Your Local Area Network.

Plus a whole lot more.

- **Can also be used for standard modem applications**
- **Automatically accepts or supplies DCE/DTE clocks**
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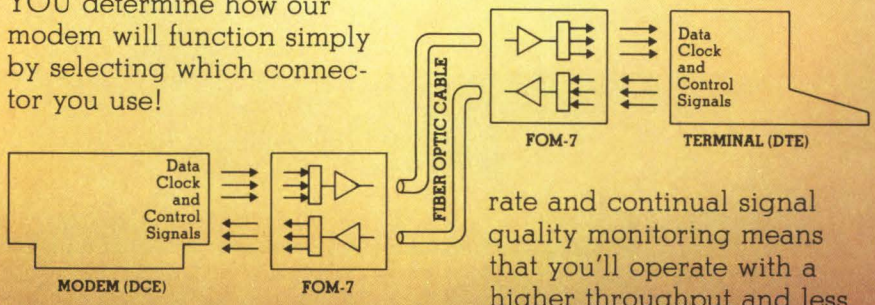
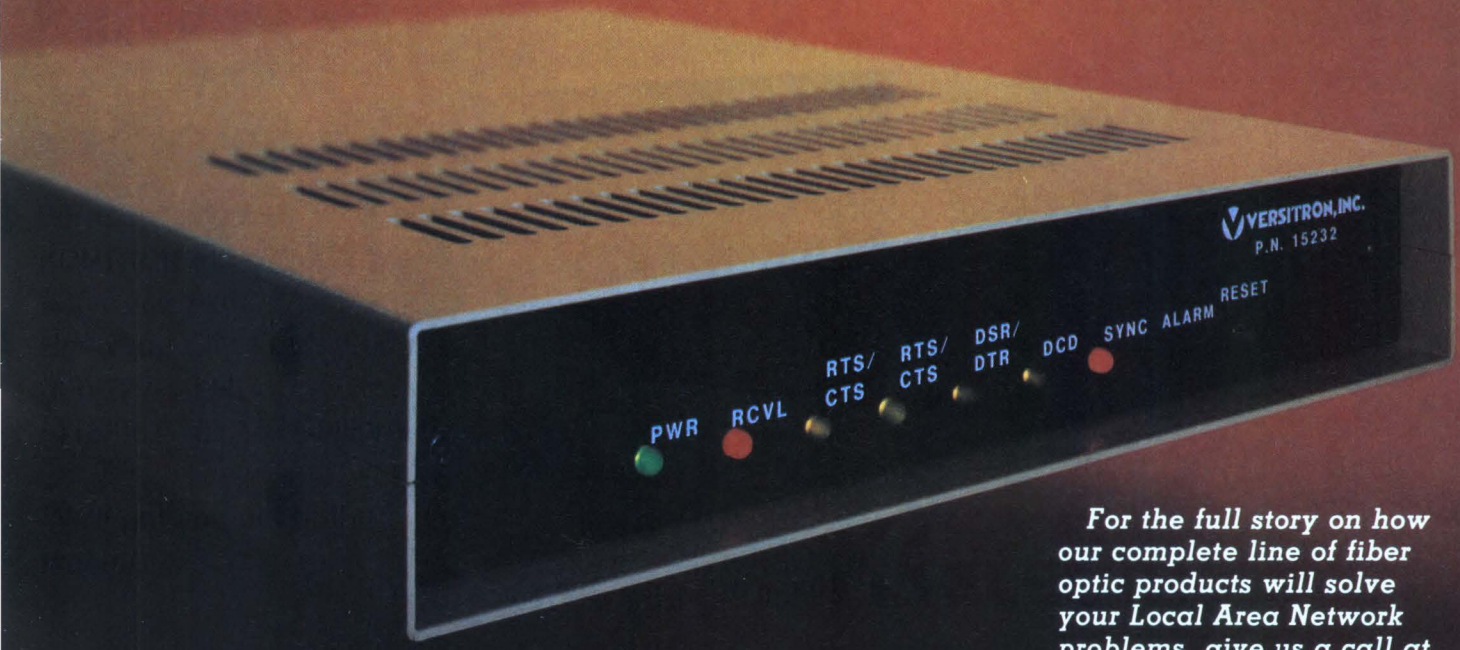
- **Provides secondary data channel**

In short, you can use our new fiber optic modem between *any* two plug compatible units in your local area network. And it won't require any jury-rigging or looping clock and interface signals. That's because, from an operating standpoint, our fiber optic modem looks just like an EIA cable; whether you're going from a long-haul modem to a remote terminal or from a CPU port to a printer. And it's just about as easy to install as a cable — we even provide two separate connectors (DTE and DCE) on each modem. YOU determine how our modem will function simply by selecting which connector you use!



Once our fiber optic modem is installed and operating it'll really begin to shine. You'll benefit not only from the advantages inherent with fiber optics (traffic security plus noise immunity) but also from the exceptional operating performance. Our very low error rate and continual signal quality monitoring means that you'll operate with a higher throughput and less downtime than ever before.

Versitron manufactures a complete line of fiber optic products for Local Area Networks. Our 20 years' experience in fiber optic is reflected in the performance capabilities of our products.



For the full story on how our complete line of fiber optic products will solve your Local Area Network problems, give us a call at (202) 882-8464. Or write:

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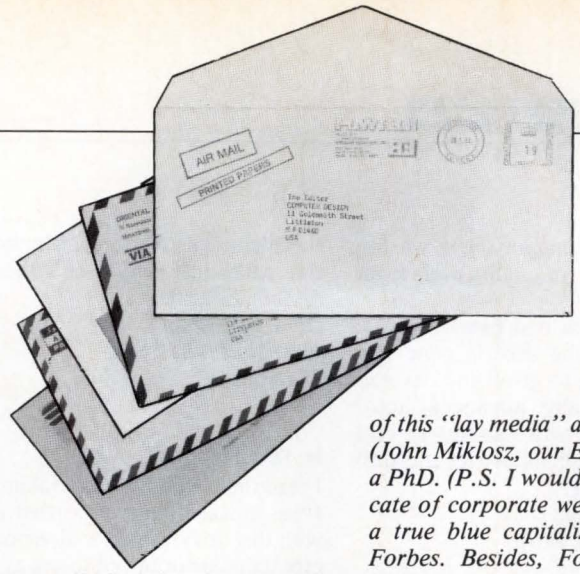
CIRCLE 16

LETTERS TO THE EDITOR



Checking the facts

I was pleased to see that *Computer Design* is interested in covering new developments in symbolic processing—a technology that is coming of age and certainly has vast ramifications for our industry. In the November issue (p 45), John Bond introduced our new Explorer system as a significant new entry into this market.

Unfortunately, in comparing it to other dedicated Lisp machines on the market, he made a few factual errors. On the basis of these errors, he positioned the Explorer exclusively as a low cost delivery vehicle for artificial intelligence applications. As Bond pointed out, the Explorer is certainly smaller and less expensive than some of its competitors, making it an ideal delivery system. However, Explorer was designed to be a powerful development tool as well.

Bond refers to the Explorer's disk capacity as 112 Mbytes several times when, in fact, its capacity is significantly greater. The disk system for Explorer can consist of four tabletop or stackable enclosures, each of which can contain two 5¼-in., 112-Mbyte drives for a total of 896 Mbytes of formatted disk storage. In addition, he states that while a full Zetalisp implementation is preferable for program development, TI chose Common Lisp instead because of the 112-Mbyte disk capacity.

Explorer does support a full Zetalisp implementation. Common Lisp, however, was chosen as the default Lisp dialect because it is an emerging industry standard. In addition, TI has added a more consistent and user-friendly interface to the MIT-based system software. And, as Bond very accurately reported, TI has provided several "toolkits," including natural language and relational table management systems, to enhance the development environment.

Joe Watson
Texas Instruments
PO Box 2909
Austin, TX 78769

Engineering shortage myth

In response to Mr Feerst's letter in the December issue, in my experience, the "engineering shortage" myth does not lie in the number of technically trained people turned out by the universities, but the use of these people after graduation.

Because management often believes in the "mass" approach to problem solving, it must keep salary costs down. Accordingly, the ranks are filled with young or underqualified people.

Those who have reached a level of competence as a result of years of experience, eventually find that they are at the top of the all-powerful "salary bracket." They are then often forced to leave what they know and do best, and go into management or sales, or leave the technical field entirely.

On a national level, using masses of low priced technical people instead of rewarding individual achievement is self-defeating. Fathers who have been forced out of a career in design and development by artificially depressed salaries are not going to recommend a technical career to their sons. Eventually, certainly not now considering the waste of talent, a *real* shortage of engineers could be forced upon us.

The "solution" in Mr Young's letter is another of the many solutions proposed by management in attempts to maintain the status quo in which it can blame the lack of imagination and ability on the chimera of "engineering shortage." Until management is convinced it the waste of technical talent is a disgrace instead of "good business," it will continue to cry shortage to the future detriment of our country.

C.W. Spindler, Jr
PO Box 11220
Elkins Park, PA 19117

What's in a name?

Who is this insignificant whelp, Michael S. Elphick? He doesn't have the stature or qualifications to review the merits of Mr. Iacocca! His comments about Professor Shannon's works are the epitome of the lay media's gall! (P.S. There is a much more esteemed member of the press with first initials M.S.—maybe you have heard of him, but I doubt it.)

(Unsigned)
Phoenix, Ariz

Unlike the author of this letter, the insignificant whelp has the courage to sign his comments. Fortunately, even in 1984, low status people were still able to criticize high status people. However, like Mr Iacocca, I am a graduate engineer with design experience. Several other editors of this "lay media" are engineers and one (John Miklosz, our Executive Editor) has a PhD. (P.S. I would not expect an advocate of corporate welfare to be a fan of a true blue capitalist like Malcolm S. Forbes. Besides, Forbes is even more opinionated than I am.)
Michael S. Elphick
Editor in Chief

Quality is the issue

In response to the December editorial on Mr Iacocca, I feel that Mr Elphick's comments were completely out of line. First of all, Mr Iacocca had no other choice than to go to the federal government for a loan guarantee because if he had not, we would all be paying for the welfare that the unemployed Chrysler workers would be collecting. Time was an issue and to negotiate with private banks would have taken too long. It was the government's responsibility to provide Chrysler with the guarantees it needed in order to prevent the economy from becoming worse than it already was. I would like to see someone from the computer industry save Evotek the way Mr Iacocca saved Chrysler.

The automotive industry has more influencing it than does the computer industry. Labor is a more important issue due to the unions that keep crippling the industry's efforts to solve quality problems. I wonder where the computer industry will be in 70 years? The automotive industry is also a heavy industry, the computer industry is not. Automobile manufacturers deal with more safety issues than computer markets.

To sight Mr Iacocca for your problems with the Pinto is like me blaming Ken Olson because my RL02 drive crashed. What does a Colt have to do with Chrysler? All they do is sell the car, not manufacture it! In fact, the car is made by Mitsubishi (a Japanese company of all things). Mr Iacocca is also responsible for the Mustang, one of the most renowned cars of all time.

I am aware of the problems that major industries in the United States are facing, and it appears that these problems are now surfacing in electronic and high-tech companies. Quality is a problem for many industries in this country. I know, I work in the storage products division of a

major computer company and we are constantly fighting for quality parts from our vendors.

Sure, Mr Iacocca had help from the government, but the debt is gone and Chrysler continues to grow and develop new and technically advanced automobiles. Why not write about the real issue of quality in US industries and stop the finger pointing?

W. Dale Robertson
Digital Equipment Corp
333 South St
Shrewsbury, MA 01545-4112

Surprisingly, I find myself agreeing with Mr Robertson on many of the points he makes. But perhaps I am old-fashioned in believing a chief executive should be held accountable for the quality of the products he sells. Though Iacocca was demonstrably better than the managers who preceded him at Chrysler, I still believe that Mr Robertson treats him too kindly. Perhaps if Mr Iacocca had mentioned somewhere in his self-serving autobiography that he too was "constantly fighting for quality parts from our vendors," I might have as much respect for him as I do for Mr Robertson and other engineers at companies like DEC. Instead, Iacocca merely brags about how he superficially restyled the bodywork of marginally profitable cars so that he could jack up the price. Also, has Mr Robertson considered who pays the welfare for the 33 vice presidents and thousands of other workers fired by Iacocca after he joined Chrysler?
Michael S. Elphick
Editor in Chief

Right man, wrong category

I have two comments regarding your editorial in the December issue of *Computer Design*. I regret your awkward experience with "Who's Who of American Women." I hope you advise Marquis of their error, as I don't believe the company intends to perpetrate such faux pas. Secondly, as for Lee Iacocca's award, I would have to agree that "entrepreneurship" is probably not the right category. I don't think the loan guarantee to Chrysler was fair to other struggling businesses either. However, I think that Iacocca may deserve some sort of award or recognition. A lot of people seem to think so. And he can hardly be blamed personally for design or construction defects in Chrysler's cars.

I myself am listed in "Who's Who in the West." I know what I did to get there, and think I deserve to be there. If I've any complaint with Marquis, it's about some fine colleagues who aren't there who I think should be.

Dave Fafarman
4330 Jana Vista St
El Sobrante, CA 94803

Is this for real?

I read the December editorial in disbelief. I was amazed that you wasted your time with this obvious personal vendetta. Several thoughts occurred to me as I read it:

1) Who really cares whether or not you approve of the selections by "Who's Who?"

2) Do you really believe that Claude Shannon cared that you didn't attend?

3) I had a 1973 Pinto (of the alleged exploding vintage) which I loved. It was one of the most reliable and economical cars I have ever owned. Does that make the Pinto one of the most reliable cars made? Of course not! A sample of one from a population of millions cannot lead to any general conclusion. You state that you would call these cars lemons "except that the word suggests an isolated bad car rather than a typical product in the line." What evidence, *except* the isolated car incidents you give, support this comment? The same arguments apply to your Dodge. I could easily conclude from your article that you don't take care of your cars ("...after a water hose fell off and the engine overheated").

4) Your criticism of Marquis for sending you a letter for Who's Who of American Women is totally absurd. I can't imagine how many women in the industry have probably received letters addressed to "Mr so-and-so." In fact, I would bet your own magazine has been guilty of this same thing—multiple times.

Let me make it clear that I am not affiliated with Marquis, Ford, Chrysler or anyone else mentioned in your article. I simply do not care for sloppy journalism which uses isolated examples and totally unsubstantiated arguments. Whether you are writing an article or an editorial, your readers deserve substantiated facts—not your wife's opinion.

I don't know exactly what your gripe is against Who's Who, except that you don't like Iacocca. Regardless, *Computer Design* is not the place for this crap.

Mark Forbes
140 Carlton Ave
Los Gatos, CA 95030

Like Mr Forbes, I am skeptical of mother-in-law (or wife) surveys. That was why I quoted an independent survey of consumer satisfaction in the editorial. Also, Ford was forced by the federal government to recall the car twice, and it is not likely that this was done on the basis of a few isolated incidents. The whole point of my argument was that I spent an excessive amount of time and money repairing the car because of inadequate design. Incidentally, I hope Mr Forbes was careful to check all of his hose clamps before leaving for work this morning.
Michael S. Elphick
Editor in Chief

Thanks for getting it right

Thank you for taking the time to get it right in the December editorial covering "Who's Who" and Mr Iacocca. Your choices of Alan Shugart and Claude Shannon (and apologies) are certainly more understandable than those of the Who's Who committee.

Although Mr Iacocca's efforts were in a business arena, and a very large arena at that, his performance is primarily a management and finance endeavor. The automobile industry certainly does need saving. (Even the US auto worker tends to purchase foreign automobiles.)

It is encouraging to find other people who do not attend events. I hope that you find some events worth attending and pass those results on to the rest of us who are often not in a position to attend or not attend.

Ronald C. Edwards
2156 Sierra Ventura Dr
Los Altos, CA 94022

Letters to the Editor
should be addressed to:
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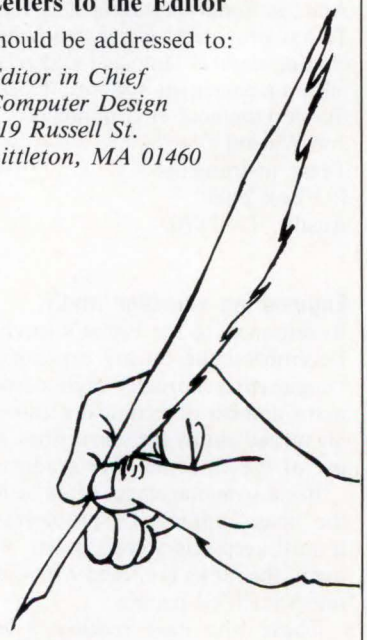

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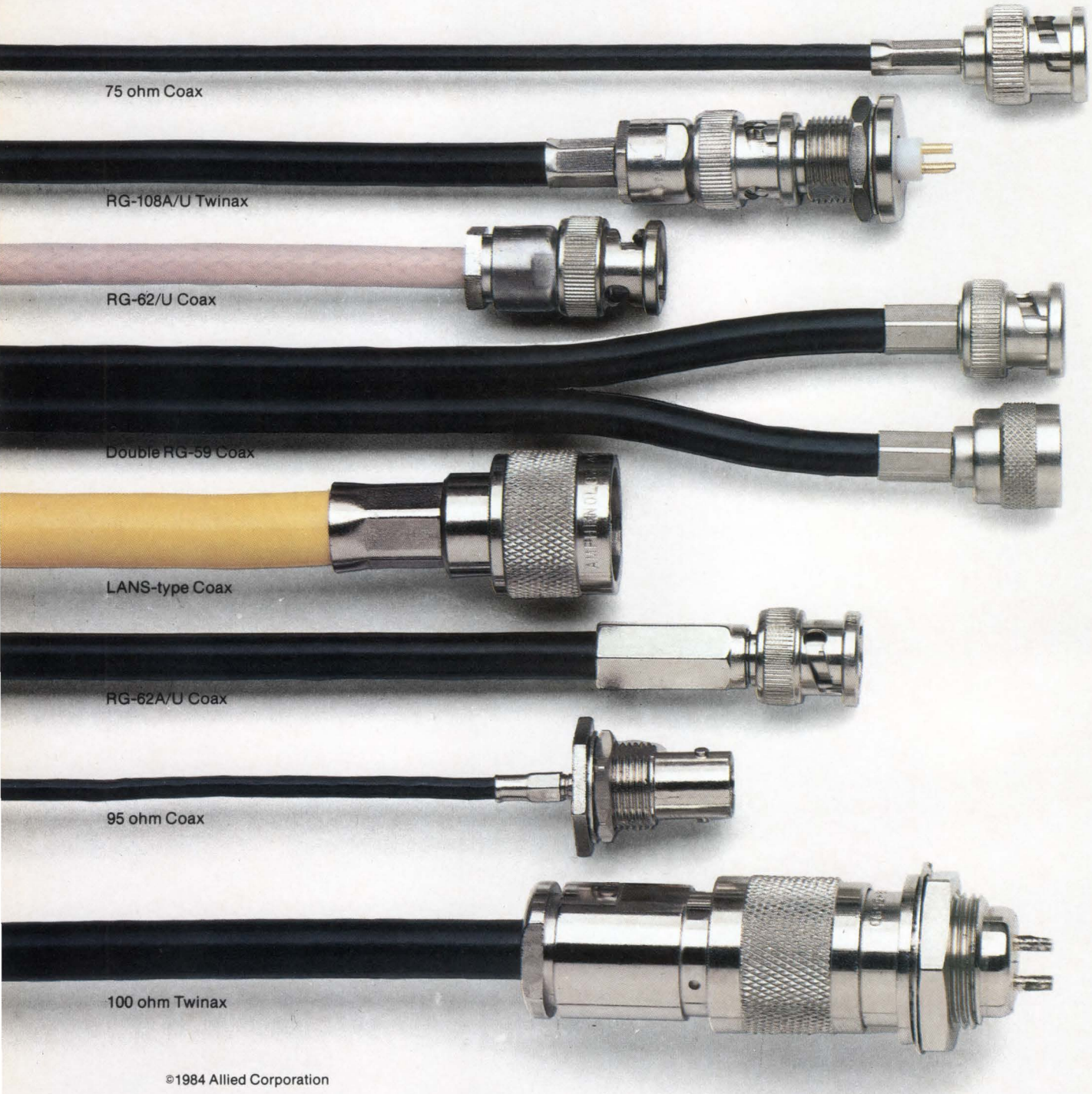

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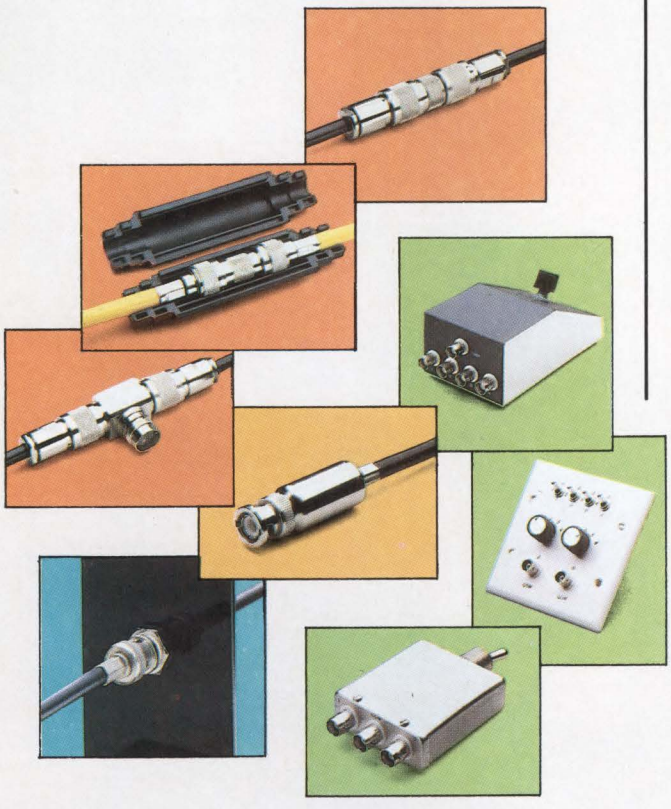

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CIRCLE 17

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CIRCLE 18

Options multiply for nonimpact page printers

While the laser printer is experiencing a drop in cost and a surge in popularity, alternative technologies for nonimpact page printers are emerging. They will offer stiff competition and drive costs even lower. Foremost among the laser's competitors are magnetic and electro-optical printers. As in laser printing, these technologies are based on a modified electrophotographic technique, originally developed for copiers. With this technique, an image is formed on a photosensitive surface by electrical charges that can attract a toner. A printed image is produced when the toner is transferred to paper and fused under heat.

These nonimpact page printers differ from other nonimpact printers (such as those using ink jet and thermal technologies) because they use a photosensitive surface to transfer an image. This makes them best suited for printing a single page. In addition, since they have evolved from copier technology, they already incorporate automatic paper sheet handling. This is an option on other printers, hence, an added expense.

By combining the copier with a laser, mirrors, and lenses, it is possible to scan the laser in time with a video signal from a computer display. This forms a kind of screen printer. The resulting basic print engine is more properly called a marking engine since it marks the paper according to the signal it receives. To print actual data, such as an ASCII text stream, a controller must be added. The controller requires memory to buffer the data and intelligence to convert the ASCII code into dot arrays. The laser needs dot arrays to scan across the drum to form characters.

Most manufacturers of low cost laser printers buy the marking engine from a manufacturer of copiers and add their own controller and interface. With this approach, there is opportunity for many additional functions and features. These include ROM-based and downloadable fonts, bit-mapped graphics, and emulations of other standard letter quality printers.

Since the basic task that the laser accomplishes is getting the electrically charged dot pattern from the computer onto the photosensitive surface (usually a drum), other technologies might be cheaper and better for marking engines. The critical factors are dot size (resolution), accuracy of dot placement, overall cost of the system, and reliability.

Variety in marking engines

In discussing nonimpact page printers, it is important to distinguish between the various marking engines with their different capabilities, and the controllers and interface electronics added by the different printer manufacturers. In the case of laser printers, there are three major suppliers of marking engines—Xerox, Canon, and Ricoh—but manufacturers have added a wide range of price/performance capabilities to these engines in the attempt to satisfy user needs. Although helium-neon or semiconductor lasers are commonly used in laser printers because of their speed, accuracy, and low power consumption, it is not altogether necessary that a laser be used to sensitize the drum surface. First, materials other than the selenium are being developed as drum surfaces. Second, coherency of the light is not as critical as the intensity and the ability to precisely focus dots on the drum. The light source must also be turned on and off fast enough to provide sufficient printing speed. When the laser is scanned across a photosensitive drum by the rotating mirror, it acts much like a raster monitor.

For all these reasons the laser is a natural choice. But there are alternatives. Optical techniques based on liquid crystal shutters, LEDs, and beam scanning on a CRT can be used to project light onto the drum.

The cost of laser marking engines has been coming down with technological improvements to such alternatives as the selenium drum. One of

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The Hewlett-Packard Laserjet printer is a desktop unit based on a marking engine by Canon. It has enough memory and intelligence to combine text and graphics with a 300-dot/in. resolution.

Nonimpact page printers

(continued from page 33)

these developments is the organic photoconductor material placed on a flexible belt instead of on a hard metal drum. A belt is used in the Ricoh (West Caldwell, NJ) LP4120 and is changed easily by the user. In another, stamped octagonal mirrors are used in laser printers, instead of precision machined ones. Sometimes the controller is added externally, and sometimes it is built into the printer package. The most basic function of the controller is to accept ASCII, bit-mapped, or graphic data from the computer and convert the data into a form that turns the laser beam on and off as the laser beam is scanned across the rotating drum. Moving mechanical parts, such as a mirror, require precise optical alignment to keep exact dot placement.

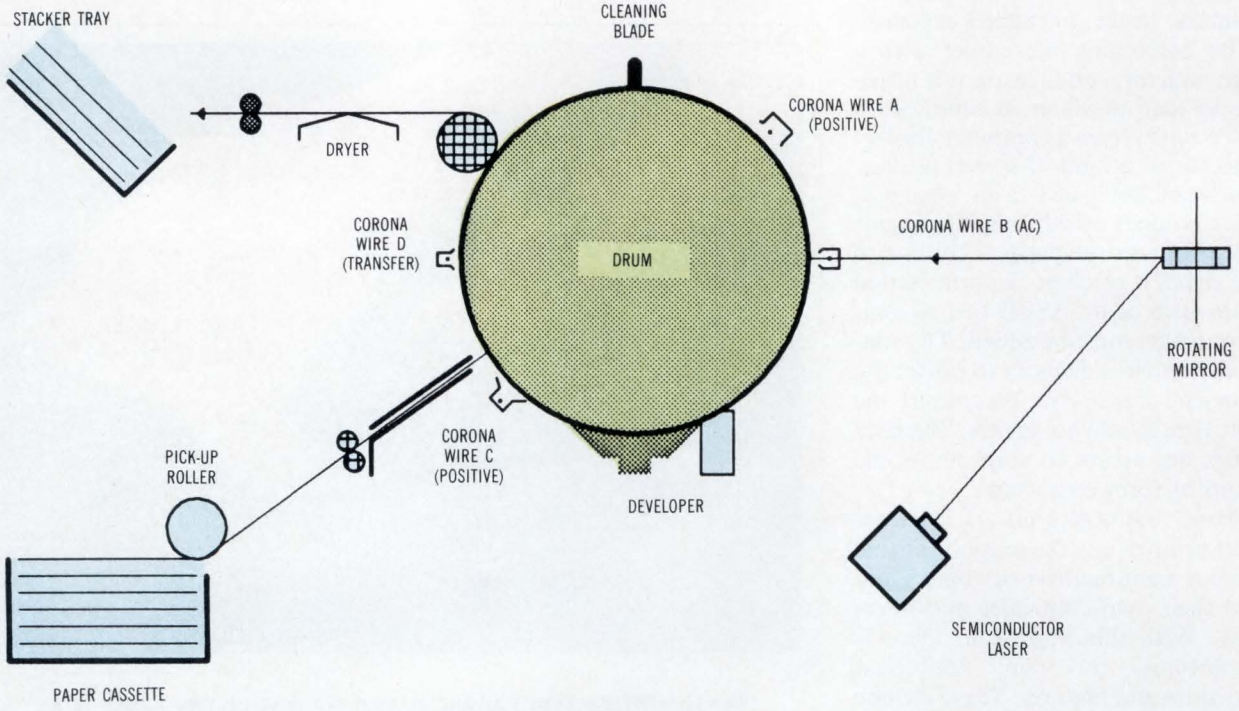
Dot placement is as important a factor in print quality as dot density or resolution. There is, however, some disagreement about where the optimal dot density lies. Many contend that at about 240 to 300 dots/in., the human eye loses the ability to distinguish between the dots. On the other hand, typesetters claim that the blackness of printer's ink is approached at about 700 to 800 dots/in. Serving the needs of the very high density user, of course, will increase the price paid for additional buffer memory and for more accurate optics.

The important aspect of dot placement is the ability to place four adjacent dots so that they are tangent to one another. This seems to leave the largest possible gap between the edges of the dots and leads to the belief that better resolution might be attained by slightly overlapping the dots. But, in both electrophotographic and magnetic printing, flux lines between adjacent dots (with the same charge or polarity) pick up toner and tend to fill in the gaps and smooth the edges between dots.

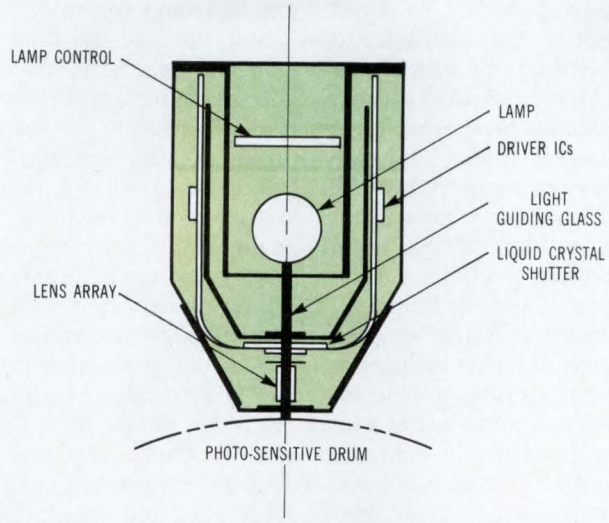
Another important factor in the quality of laser marking engines is the writing method used: scan-to-write or scan-to-erase. In scan-to-write, the laser places a charged dot at every point that should pick up toner—it is essentially writing with a black dot. Scan-to-erase starts with a fully charged surface and removes a charge at every point that should not pick up toner—essentially writing with a white dot. In both cases, low frequency noise can cause a scan line to vary somewhat from being perfectly straight across the page. In scan-to-erase, this variation in the two lines on either side of the line to be left black would cause the width of that line to vary. Scan-to-erase, thus, cannot produce lines exactly one pixel wide and scan-to-write is inherently more accurate.

Lights and magnets

Alternative electrophotographic marking engines are addressing the laser's need for precisely aligned optics and a moving part (in the form of a rotating mirror). The liquid crystal shutter technology recently introduced by Epson retains the selenium drum and toner system of the laser



The rotating mirror in a laser marking engine is timed to sweep the beam of the laser across the drum. The drum rotates at a speed defined by the dot density.



In the Epson GQ-3000 printer, light from a lamp passes through a guiding glass to the liquid crystal shutter. Dots in the liquid crystal panel turn on and off to admit light as the drum rotates beneath it.

printer, but uses an incandescent light source behind a stationary liquid crystal shutter with an array of over 2000 dots. The dots are turned on and off as the data is fed to the array scan line by scan line. As the polarity of the liquid crystal changes, light to the drum is either admitted or blocked. According to Masahiko Mori, general manager of design for Epson's printer division in Kamisuwa, Japan, this method significantly reduces the number of moving parts and the cost, and increases reliability. But, he cautions, dot resolution has a practical limit of about 300 dots/in. Epson's introductory model, the GQ-3000, has a resolution of 240 dots/in.

Two other approaches are the K-2 intelligent printer by Kentek (Allendale, NJ) and the Elpho 20 by Philips Peripherals (San Francisco, Calif). The K-2 uses a fixed array of 2084 LEDs focused on the drum through fiber optic lenses. In the Elpho 20, a CRT projection technique focuses the beam scanning across a monoline CRT onto the moving drum. Philips has achieved a dot density of 600 dots/in. with the Elpho 20, placing it close to the resolution demanded in phototypesetting applications.

Although magnetic printing uses a method for sensitizing the drum different from that used in electrophotographic systems, the engine works in essentially the same way. Magnetized dots on the drum pick up toner and transfer the image to paper.

Two manufacturers currently producing magnetic printers are Honeywell-Bull, represented in the United States by Cynthia Peripherals (Sunnyvale, Calif), and Ferix Corp (Fremont, Calif). The Cynthia 6000 series uses a hard steel drum with a proprietary surface alloy that picks up magnetic impulses from a stationary array of magnetic cores. The core array is manufactured in sections that are assembled inline and precisely aligned.

The Ferix new thin-film head technology is the basis for another magnetic printer technique. The head, a thin strip of metal manufactured by a wet chemistry process, consists of a 16 x 8 array of magnetic elements. Since the head is flexible, it is compliant to the drum, making critical alignment unnecessary. The magnetic elements are toroidal and focus the magnetic flux through the surface of the head strip onto the drum. The drum is coated with the mylar ferric oxide material used in a floppy disk.

In the current Ferix printer Model 800, the head array is moved back and forth across the drum like a dot matrix printer. The technology can provide a higher dot density than currently achievable, and can eventually be implemented within a stationary array.

Magnetic printing brings with it a couple of inherent advantages. First, once the drum is magnetized, it stays that way until erased or written over. This means that once the image has been transferred, multiple copies of that page can be printed offline without tying up the computer. In addition, it is possible to write the page in two or more passes—once for text and then around again to add bit-mapped graphics.

The controller difference

If the function of the marking engine can be compared to that of a raster monitor, the task of the controller is essentially image processing. The controller also handles host and application interfacing, protocols, and in some cases performs job management tasks (eg, formatting, integrating text with graphics, font changes, and higher level graphics primitives).

Perhaps the most basic function provided by low cost electrophotographic and magnetic printer controllers is emulation of daisy wheel and high quality dot matrix printers. This is a feature needed to preserve the software investment and provide upward compatibility.

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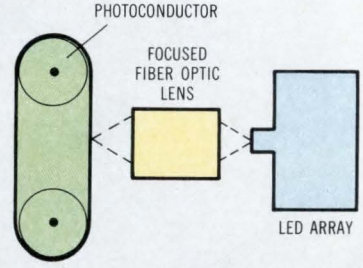

Like the Ricoh LP4120 laser printer, the Kentek K-2 LED printer uses a belt of organic photoconductor. Light is supplied by a 2084-fixed LED array across the drum and focused through fiber optics.

Nonimpact page printers

(continued from page 35)

The next most common function is to provide multiple fonts, which are most often supplied in plug-in ROM cartridges. Even at this level the printer will require control codes from the host that differ from those used in present printer driver software.

As the features and functions of the controller multiply, the requirement for software grows. In some cases, such as the 12/300 laser printer by Imagen (Sunnyvale, Calif), even fonts are no longer considered dot arrays, but are made up of high level graphic primitives.

One thing that laser/electrophotographic and magnetic printers have in common is that they are synchronous devices. Once they have started to print a page, they cannot be interrupted without ruining the scan. To work properly, they must print a page at a time, stopping only on an end-of-page code. The computer must therefore supply enough data for a complete page description on one data transfer, and the printer must be able to buffer that data.

A full 8½- x 11-in. page printed at 240 dots/in. is equivalent to about 8.3 million pixels. This translates to a little over 1 Mbyte of memory to buffer a full bit map. Add to this the memory needed for program storage and ROM-based fonts, and the amount of memory can exceed the address space handling of some 16-bit microprocessors. Nevertheless, some manufacturers supply a full megabyte of memory space, such as Kentek in its K-2. Hewlett-Packard supplies varying amounts of buffer memory in the Laserjet for storing graphic bit maps. But few attempt to buffer a bit map of an entire page. The data rate of a common RS-232 or parallel interface would make this unacceptable.

In the Kentek K-2, the large amount of RAM is provided because fonts and emulation software are supplied on a floppy disk instead of in ROM cartridges. The files needed are called off-disk by the page description sent to the printer from the host. Depending on the capabilities of the printer, a page description can consist of simple text with a code for emulation and a few font changes, or a complex file combining text, graphics, and forms definition.

Still, for the marking engine to scan, it must refer to a bit map buffered in memory. However, if the page description is stored in the printer in code form, the bit map can be created on-the-fly, then buffered and scanned in segments. The host, having transferred the page description, can do other things until the printer signals that it is ready for another page description.

Since a page description that results in a printed page of some 8 million pixels can be complex, the software used to create and interpret page descriptions plays a key role in the acceptance and integration of these printers. Software is needed to adapt such widely used applications as spreadsheets, word processing software, and database management programs to the printers. It is also necessary to give the ordinary user the ability to select options that satisfy the need to have a "what you see is what you get" transition from display terminal to printed page.

Hewlett-Packard's 2688A text and graphics page printer, for example, can be driven by a number of software packages that run on HP 3000 computers. An interactive formatting system, IFS/3000, allows the user to specify fonts, electronic forms, and page configurations from a menu of predefined forms or to develop customized formats. Graphics may be designed from existing Hewlett-Packard graphics software, such as HPDRAW, that is able to drive the 2688A; individual characters may be designed using an interactive design system. Such characters are defined as any dot pattern within a specified area. All this software must be run on the HP 3000, using specific graphics terminals to provide the "what you see is what you get" experience.

Page printer manufacturers that are addressing the OEM market on a wider basis have a tougher row to hoe. They must make their page-definition software flexible enough to adapt not only to a wide range of application packages, but also to different terminals. Such software does

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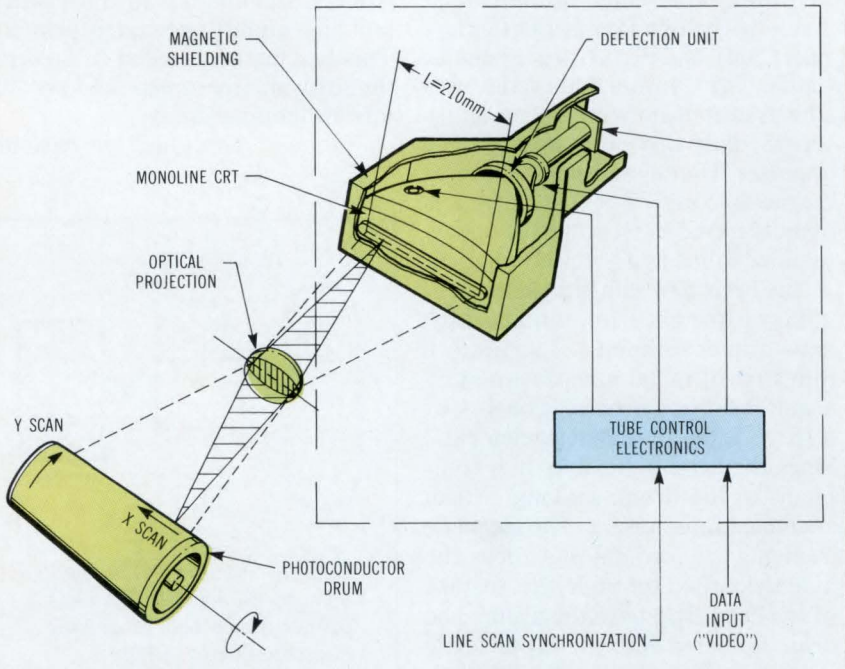
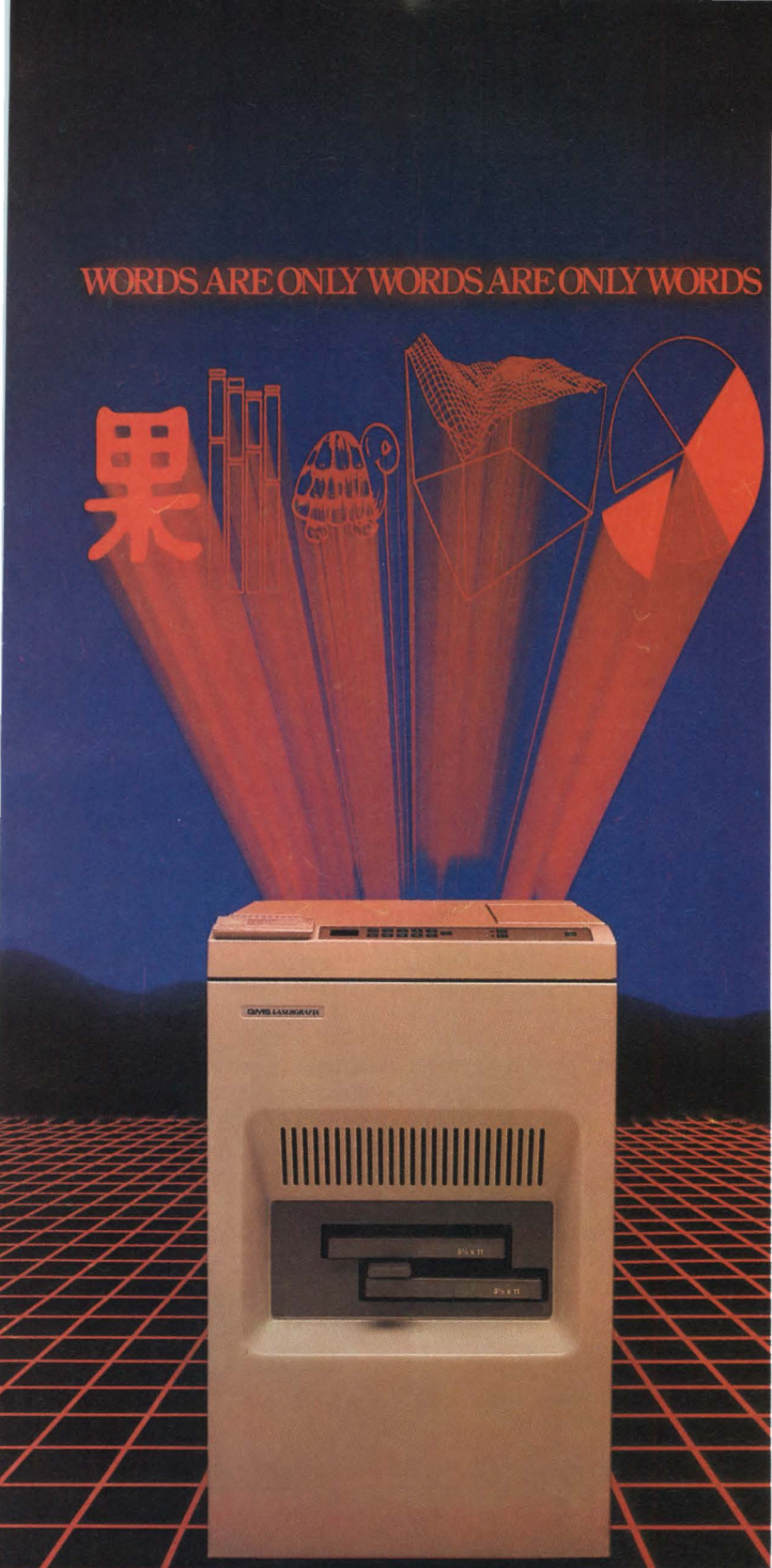


The Philips Elpho 20 achieves very high dot resolution (600 dots/in.) by focusing the light from a CRT beam onto the selenium drum.



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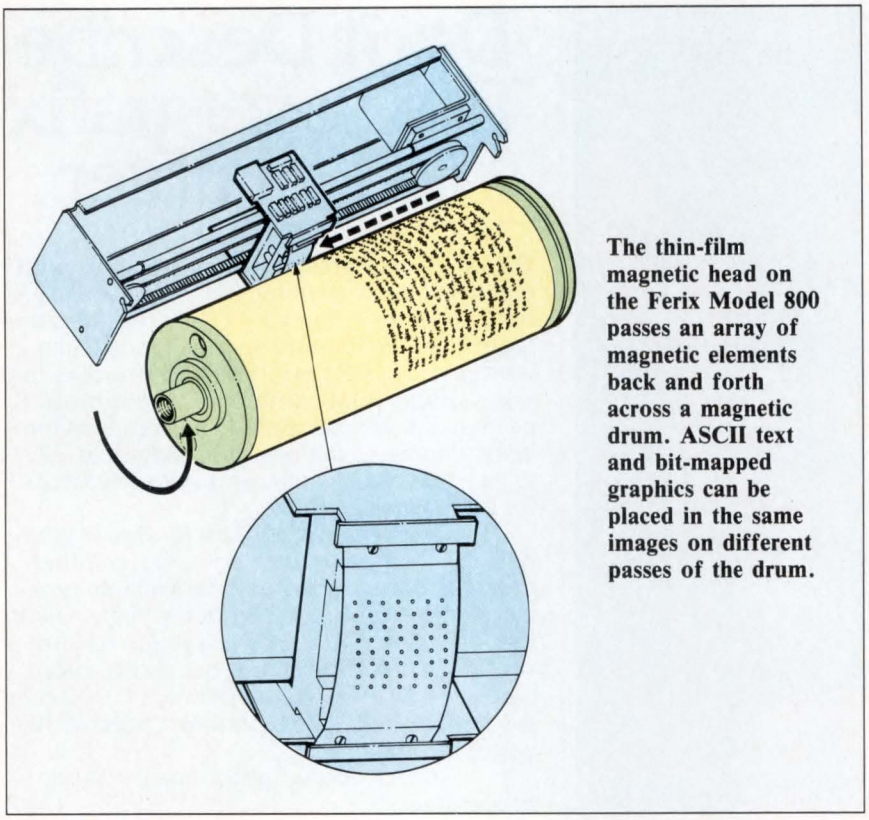
CIRCLE 19



The thin-film magnetic head on the Ferix Model 800 passes an array of magnetic elements back and forth across a magnetic drum. ASCII text and bit-mapped graphics can be placed in the same images on different passes of the drum.

Nonimpact page printers

(continued from page 36)

not really exist as programs that can be compiled and executed in the normal sense; rather, it is embedded in a text stream that is sent to the printer to control the printer's functions.

Two companies that provide software to drive their controllers are Imagen (Sunnyvale, Calif) and Quality Micro Systems (Mobile, Ala). The imPRESS package by Imagen sends codes to the printer to control text, graphics, and orientation. The codes are entered as binary numbers.

An imPRESS page description will typically consist of 8 to 10 Kbytes of text, font changes, and vectors. The page description is then compiled into a page object of about 20 to 30 Kbytes. This page object resides in the printer's memory and converts to raster information on-the-fly as the Imagen 12/300 laser printer scans the drum. Robert Wallace, vice president of marketing at Imagen, stresses that the Imagen controller is not tied to laser technology. However, it can be adapted to other types of electrophotographic or magnetic systems by adding a different personality board.

A software package such as imPRESS is really an OEM tool that lets application or system designers adapt existing software or lets them design user interfaces to create page descriptions interactively on a CRT with a mouse or another input device. The program will generate a page description that contains the proper imPRESS binary codes. With this package, it would be possible, for example, to have a program that would take input data from a mouse and output imPRESS code to drive the printer.

The Quality Micro Systems' QUIC language is similar in concept to imPRESS. Instead of entering binary numeric codes for the command, however, mnemonics allow a user to write the page description with an editor. A lot of numeric strings still exist and the QUIC code is not readily decipherable in its source form. But that is not the main purpose of QUIC or imPRESS; they are meant to form a bridge between applications and the printer's capabilities. Both are specific to their own controller or controller family. QUIC runs on the Quality Micro Systems line of Lasergraphix machines, which use Canon or Xerox marking engines.

Quality Micro Systems also supports a text and graphics integration software package supplied by Adobe Systems (Palo Alto, Calif). Called Postscript, the package is a page description language that uses a device independent imaging model that supports a raster image. Fonts, for example, are defined as outlines that can then be given attributes, such as point size, fill, and orientation. The user writes the page description in terms of standard Postscript commands. This description is sent to the printer controller where it is interpreted by a controller-specific interpreter stored in ROM. Using Postscript, the user can specify text and graphics using the same model.

Nonimpact page printers, be they laser, electro-optical, or magnetic, appear to have a definite future. They are, in reality, low cost, high resolution graphics output devices with embedded image processing capabilities. As such, the key to unlocking their potential lies in the software that is developed to drive them and to mate existing applications with their capabilities.

—Tom Williams,
West Coast Managing Editor
SYSTEM TECHNOLOGY

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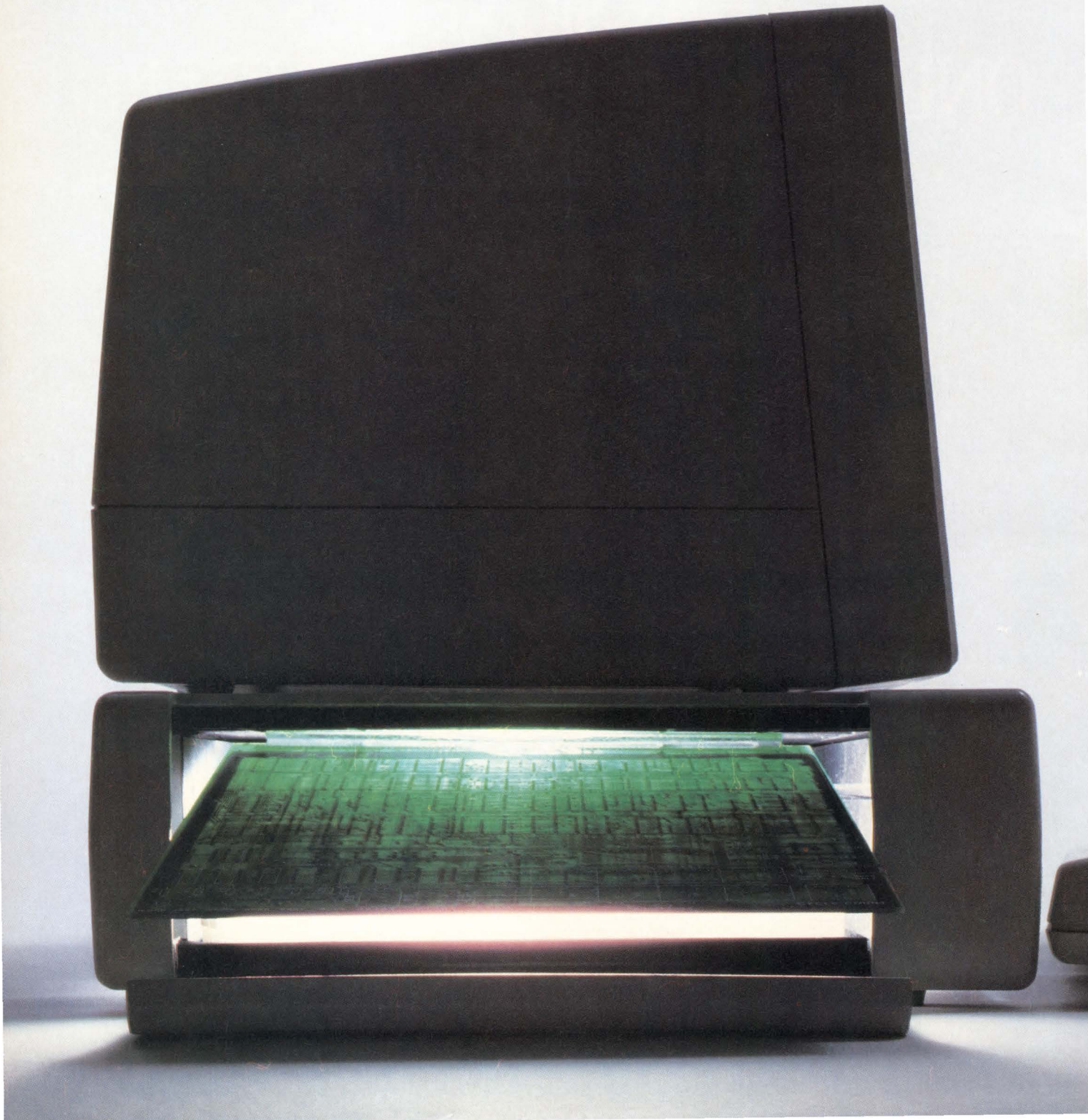

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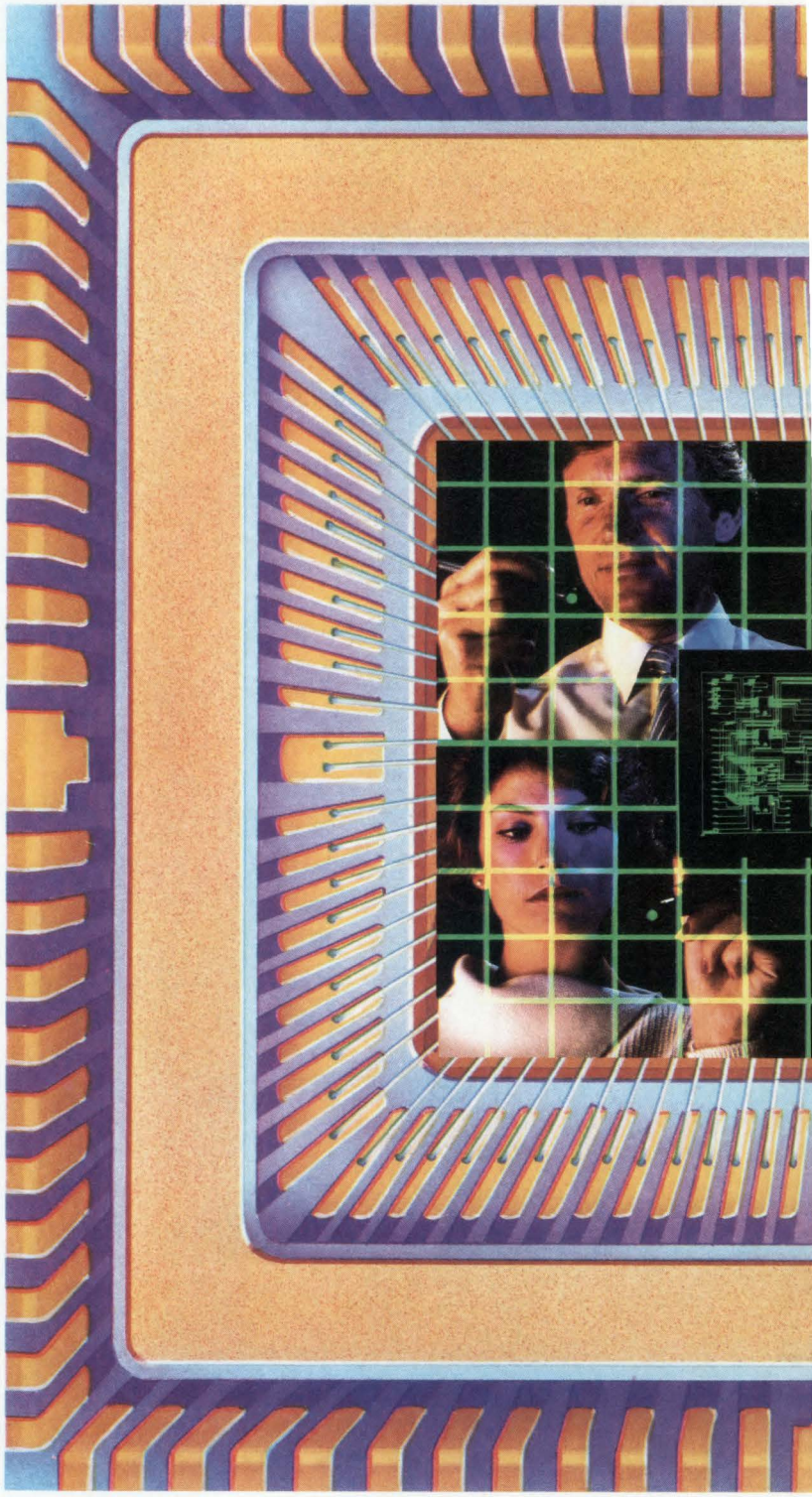
H CMOS	2.8 μ	5.0 ns	440-3900
VH CMOS	2.3 μ	2.5 ns	2600-8000

*2-Input NAND Gate, F/O = 2

BIPOLAR

TECHNOLOGY	PROP DELAY TIME*	GATE COUNT	POWER DISSIPATION PER GATE
LSTTL	1.8 ns	500	2.3 mW
LSTTL	1.9 ns	240-1100	0.8 mW
LSTTL	0.95 ns	2000	0.65 mW

*3-Input NAND Gate, F/O = 1



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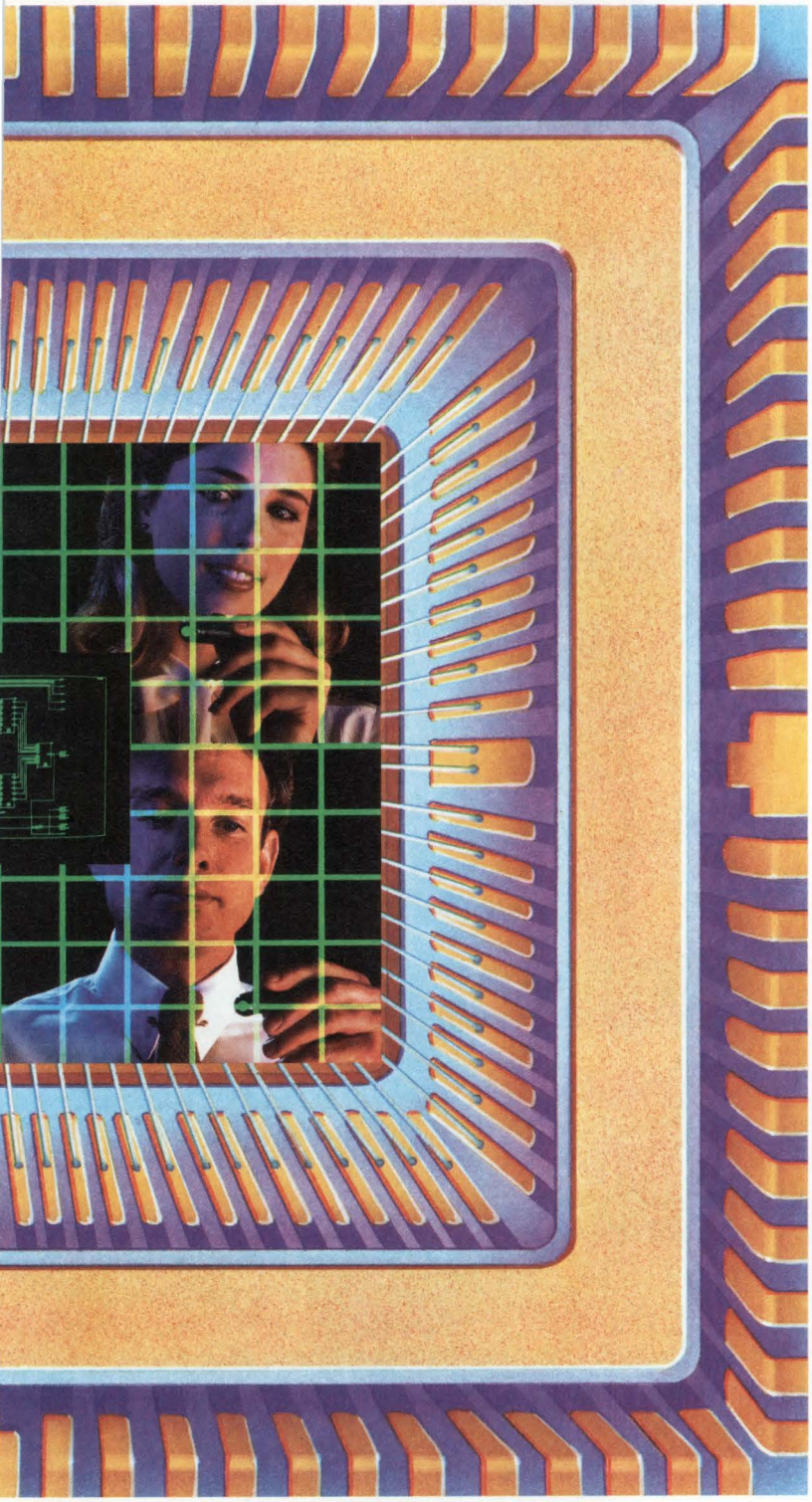

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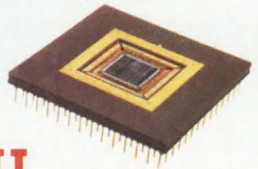

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CIRCLE 20

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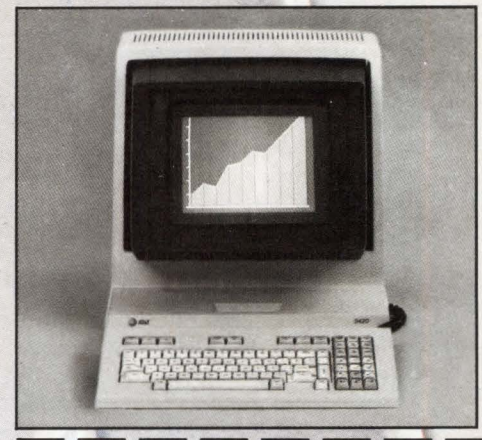

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DoD struggles to balance IC reliability and price

The Department of Defense wants higher reliability in the ICs it buys. Suppliers say that the methods requested by the United States government will cost more money.

This is only one of several disagreements over new testing requirements, spelled out in revisions to MIL-STD-883. This document is used by the military to define and control tests for the reliability levels of semiconductors parts it buys. No one wants to say it openly, but there is deep animosity and suspicion among the government, many of its major contractors, and the companies supplying semiconductors for government programs. Some semiconductor suppliers are saying they will not sell parts meeting the new standard. And some federal inspectors are telling anyone who will listen that the manufacturers are supplying parts with inadequate testing.

"I could tell immediately, based upon the price-quote, whether a company planned to test the parts to an acceptable level," said one government inspector. Unfortunately, he says, he doesn't even see those price quotes. He is called in after the contract has been awarded and parts are being produced.

The government is making no bones about its desires; it wants its suppliers to use only Joint Army-Navy qualified parts. Darrell Hill, chief of the microcircuit qualification branch at the Defense Electronics Supply Center in Dayton, Ohio, is one who recommends the use of JAN parts wherever possible.

Unlike parts previously procured under 883, the JAN parts are produced and tested to MIL-M-38510. "It allows no exceptions, no waivers," says Hill. MIL-M-38510 is the standard document used by the military to define the conditions under which microcircuits will be manufactured in order to attain JAN designation. Parts manufactured under this method are tested to both the requirements of 38510 and those of 883.

On the other hand, major contractors maintain that the cost of JAN parts is so high that they cannot make competitive bids if they are forced to use those ICs exclusively. The limited number of suppliers who manufacture JAN parts (nearly three times as many sources exists for non-JAN parts), confines buyers to a list of fewer than 20 manufacturers. This can result in lengthy delivery times and cause program delays.

Prices will escalate

Costs for a "newly qualified" JAN microprocessor range from $600 if JAN parts are specified, $60 for MIL-STD-883 level B parts, and $15 for industrial-grade ceramic parts. While some of the markup for the JAN-qualified parts represents the initial certification costs, the price can never fall to the level of 883 parts because the documentation required by the government is so great.

Even such "mature" products as an 8080 still cost in excess of $150 each, with JAN certification. The reasons are that manufacturers must impose controls on the process lines, implementing a layer of management and bureaucracy that is beyond standard industry practices. The government insists, for example, that materials used for manufacturing JAN parts be traceable by lot number back to the original manufacturer. In addition, the testing records required are far more detailed than for other programs. According to DESC's Hill, ICs are tested to one of

(continued on page 48)

Can the military shift to all-JAN?

Widely touted by the general press as "built to best commercial standards," the Northrop F-20 Tigershark program has drawn a great deal of attention, due mainly to the high performance it offers at a relatively low price. Since the F-20 was designed for sale to third-world countries, its design was not regulated by the same review and control processes that is ordinarily imposed on a U.S. fighter development project.

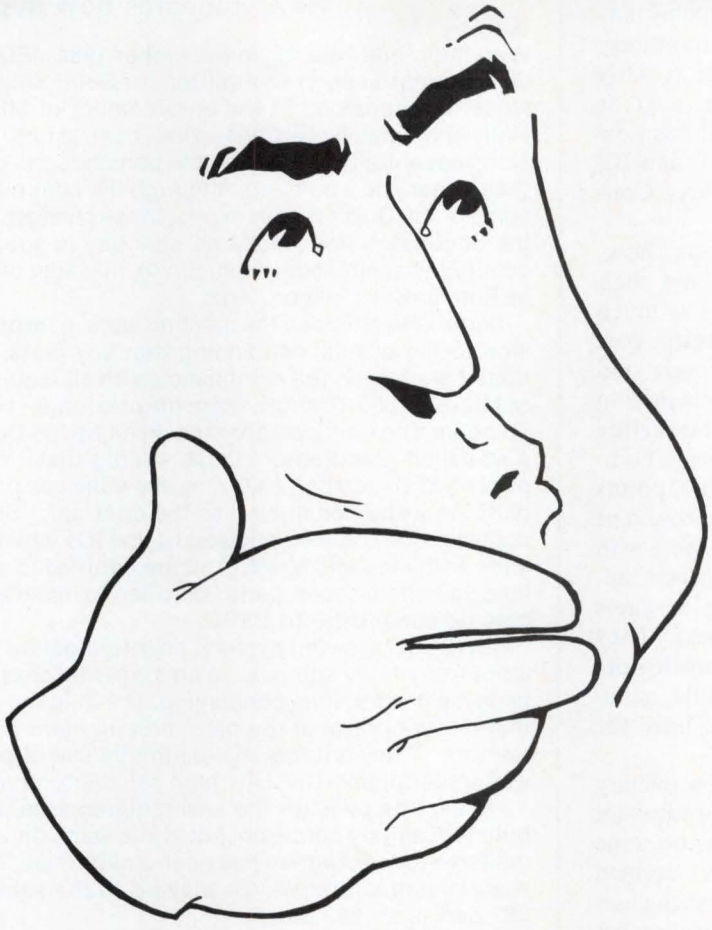
According to Northrop (Hawthorne, Calif) design manager Herb Stark, the avionics were built with military ICs. "In no case was any component allowed in the project unless it was tested to the full requirements of MIL-STD-883, level B," he says.

Honeywell, who provided the inertial navigation system (INS), revealed that only Joint Army-Navy level components were used. In fact, the INS for the F-20 is a standard Honeywell military product and is manufactured on the same assembly line as those destined for use in U.S. military aircraft.

But at Teledyne Systems (Northridge, Calif), Alan Smeyne, program manager for the avionics control computer used in the F-20, says he feels that a push toward full JAN parts is a mistake. "First, 38510 can get you into a sole-source situation where only one company is authorized to make a particular part," he explains. According to Smeyne, JAN approval takes too long. "The newest technology isn't there [on the QPL], and the JAN parts cost more," he says. MIL-STD-883 parts are not only adequately tested, he feels, but also a step ahead of JAN parts because of the time that it takes to obtain 38510 approval.

This opinion is reinforced by Mike Campbell, reliability and quality manager at Inmos (Colorado Springs, Colo). Campbell says, "I've seen it take as long a year and a half to get JAN approval on a 64-K DRAM."

SOS or SOS?



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The Midnight Sun Rises in the West.

CIRCLE 22

DoD struggles

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three different levels of reliability currently authorized for use in military systems. The highest level is JAN MIL-M-38510 parts, the next is MIL-STD-883 (which itself has now only two levels of testing: S and B), and the lowest level is Source Control Drawing.

Military systems designers, however, feel that SCD parts are their "ace in the hole." It takes as much as two years to get a specific part through the JAN approval cycle, and two years is a whole new world in ICs. As Ralph Cognac, marketing manager for Integrated Device Technologies (Santa Clara, Calif), points out, "It precludes the latest round of technology. Rather than dealing with two year old technology, the best military designers are trying to guess what will be available next. They have to be excellent prognosticators because in the electronic battle, nanoseconds count. They must have the very latest technology."

SCDs were devised to allow military contractors to use parts that were not JAN qualified but, in view of some technological edge, were deemed essential for a program. In such cases contractors submit a justification for using such parts. They also create a specification and drawing for that part, including test requirements that are used as the purchasing specification. "Our first preference is that our suppliers procure JAN M-38510 microcircuits. That gives them the high reliability that we're all looking for. That's what we want," says Hill.

But Al Jonas, military sales manager at TRW Semiconductor (La Jolla, Calif), predicts not only will prices have to go up to meet this change in DoD policy, but the new policy will cause production and delivery disruptions. "How will that help the government?" Jonas asks.

Despite the high cost of the components, the military claims it could save money by using the parts. But there may be other reasons for using them.

First, most government buyers simply do not like MIL-STD-883 parts, which they call JAN look-alikes. Although they may be screened to the same reliability standards as JAN parts, suppliers of these parts are not required to have the same government inspections and approval of their production lines. This line certification process is expensive and the approval cycle is lengthy. A company actually gives up a great deal of control over its own line. Second, SCD parts can be used in DoD equipment only through a series of waivers, whereby the contractor must justify the use of unapproved parts. Originally, the DoD intended for the provision to allow the use of parts which had not yet received JAN approval so DoD contractors could keep up with the state of the art. The DoD now believes that this avenue has been abused by contractors.

DoD representatives condemn the use of SCDs. Some, off the record, accused their prime contractors of

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New standards now in place

With their final meeting in December 1984, JEDEC Committee J13, the Government Liaison Committee for Solid State Products, settled the issue of extensions to the enforcement of MIL-STD-883, Revision C. Hotly contested by all sides—DoD, contractors, and suppliers—the revisions essentially support all the demands the government made more than a year and a half ago. Although the committee managed to rewrite some of the DoD's requirements, those changes were intended to clarify the document, and "made no changes in substance or intent," says committee chairperson, Herb Smith, manager of international marketing at Burr-Brown (Tuscon, Ariz).

Some who attended the meeting were in favor of a three-month extension to the clause, demanding that any parts offered for sale as 883 tested must be in full compliance with all requirements and provisions of MIL-STD-883. In short, there may no longer be any exceptions to the standard.The only compromise given by the DoD was the inclusion of a so-called grandfather clause stating that, "contracts which issued prior to 31 December, 1984 may allow the use of 883-B or SCD procured parts until the conclusion of the contract." Smith explains that new contracts will only be allowed to use ICs which are produced, tested, and certified to MIL-M-38510, or are certified to comply with DESC drawings. In certain cases, parts "certified to manufacturers specifications" may be acceptable to DESC.

The DESC drawing system, an intermediate step on the path to full Joint Army-Navy approval, is no longer favored by military contractors because it is too time consuming. The military, on the other hand, feels that it lost control of the parts procurement process used by its contractors. "They felt that the continued use of source control drawings was undermining the JAN high reliability program," says Smith.

He says he believes the new requirements will increase the cost of building military hardware, but at the same time he sees benefits. "The military spares program has been a nightmare," he says. "Now, at least every manufacturer will be playing to the same set of rules. Now an 883 part is an 883 part."

Dick Lambert, quality manager at Signetics (Sacramento, Calif), chairs the J13.2 subcommittee for micro-electronic devices. He feels it was the grandfather clause that subdued the expected debate over immediate compliance. Lambert thinks this is shortsighted, because "sooner or later the current contracts will run out, and then everyone who wants to stay in this business will have no option other than full compliance." Given this situation, Lambert says his company will assume that all requests for quotes received pertain to new contracts, and will respond and bid appropriately. "There simply is no other way to play it. We receive thousands of requests for quotes, and there is no time to investigate whether they are for new contracts or not, because we have to respond within one week."

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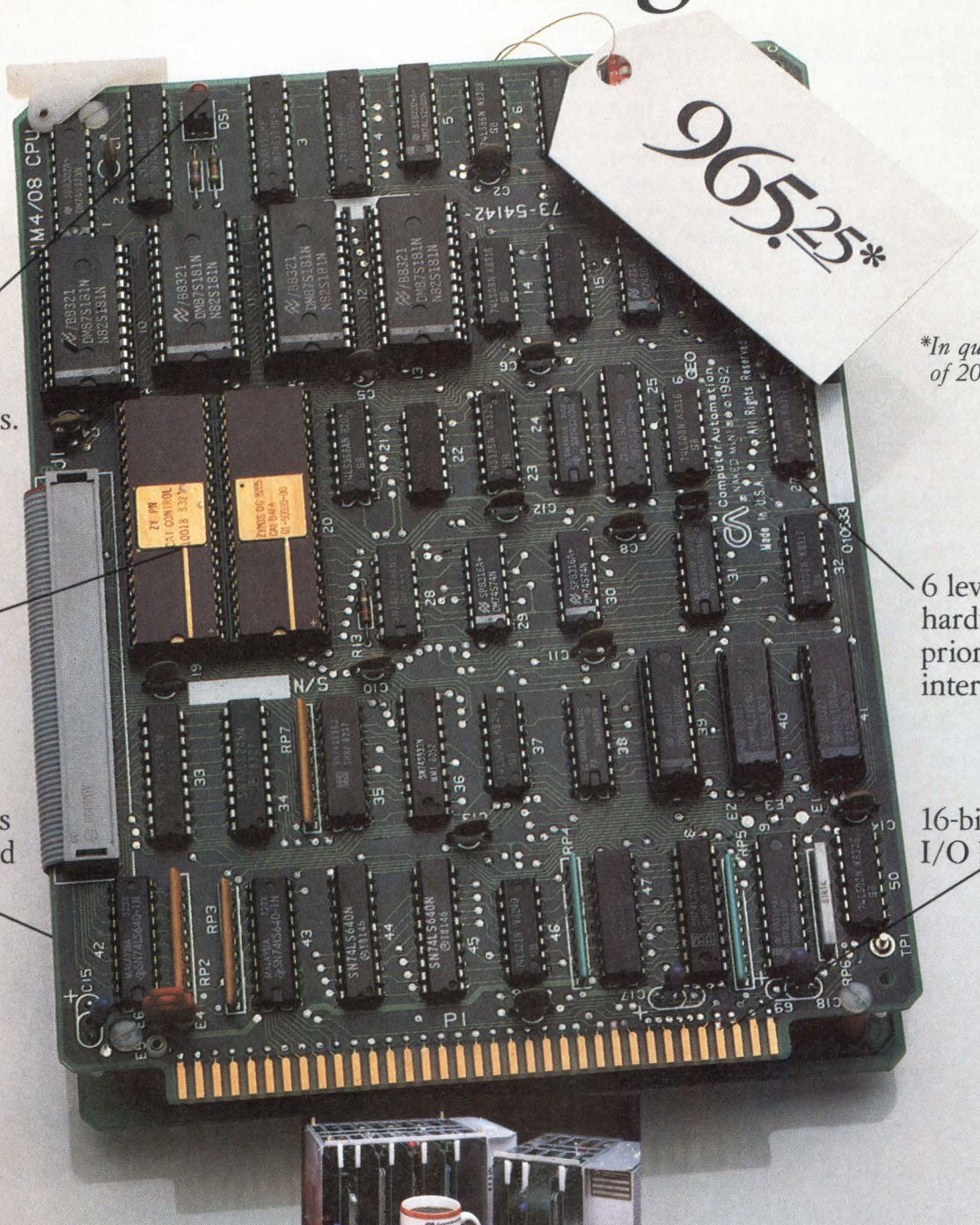

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CIRCLE 23

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DoD struggles

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using this practice to inflate the cost of government contracts. Because the development of parts and suppliers is considered "out of scope" (ie, not part of the price bid on a contract), this activity can be billed directly to the government, driving up the cost of the contract, without technically overruning the budget.

"These SDCs typically run $2000 to $6000 per drawing," according to DESC's Hill. "Some people are making a lot of money by generating SCDs," he says. At Viking Labs (Santa Clara, Calif), Gene Hnatek, head of that independent test lab's microcircuit qualification testing department, says, "Some parts as common as a TTL quad gate can have as many as 4000 to 5000 source control drawings in existence which specify that one, simple part."

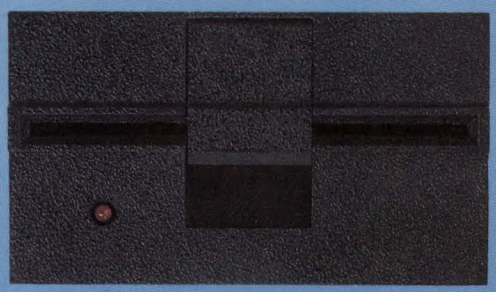
Contractors counter that they are forced to issue SCDs for many valid reasons. They claim SCDs allow them to hold down the costs of a contract, especially in noncritical applications. Often, according to the prime contractors, SCD parts are required to meet contract schedules when long delivery times prohibit the use of the military parts or when JAN parts are inadequate. "But DESC doesn't seem to be addressing the problem of cutting the time it takes to get JAN approval," says TRW's Jonas.

Semiconductor manufacturers, taking yet a third perspective, see SCDs as a massive paper jam. A few years ago, National Semiconductor Corp refused to test to contractors' SCDs. "I can sympathize," says Hnatek. "Software control can be horrendous if you start testing to SCDs because each company will want a few things to be different on each item." But semiconductor makers are divided on this issue.

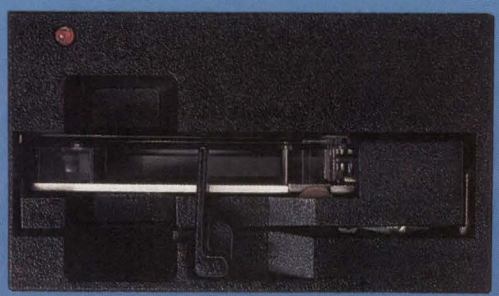
One of the newer companies to achieve JAN certification of its lines is Zilog (Campbell, Calif). Kirk Lemon, military marketing manager there, says Zilog is very interested in JAN and 883 business. In reference to SCD parts he says, "I am not saying that we would turn any of it down. It would depend on the order and the pricing, but the only SCD business we actively encourage is where the contractors use our part specification for their SCDs. If they don't, then we have to take another look at the bid."

But at Fairchild Semiconductor (Mountain View, Calif), John Migliori, vice president of marketing and sales, says his company will remain responsive to requests for parts to SCD specifications. Viking's Hnatek offers this advice to defense contractors: "Don't fool around with SCDs, buy JAN parts."

One of the major issues defense contractors and the DoD are debating concerns SCD parts, JAN parts, and MIL-STD-883. If the DoD doesn't



THE END OF THE SECONDARY STORAGE SPECTRUM EVERYONE FORGOT ABOUT WAS THE MIDDLE.



want these parts used, why not the "JAN look-alikes?" Why did it prepare and impose revision C to the spec last year, specifically allowing the practice? DoD claims it wants to increase the reliability assurance levels of the ICs purchased under this document.

Some contractors feel, however, that the government simply wants more control over fabrication processes and test procedures. Some also feel that the DoD only wanted 883 to serve as the master test document for JAN-qualified parts, too. And others believe that the DoD, (specifically DESC) is using the JAN-part issue to expand the role of the agency, with little regard to overall costs or systems performance.

Representatives for the government agencies continuously use catch phrases to describe the current standards they see as standing in the way of the goals of new standards. "Truth in advertising" and "JAN look-alikes" regularly crop up in conversation with government officials. The DoD's tendency to use catch phrases, along with a pronounced fondness for speaking "off the record" does little to counteract the charges from industry.

The DoD and industry have focused their major differences on one key paragraph (specifically 1.2.1) of the C revision. The DoD insists that too many companies have made too many interpretations of the testing called for under 1.2.1.

Again, DoD officials revert to catch phrases. "What we are talking about here is really truth in advertising," they say. "If a manufacturer claims to test to MIL-STD-883 Rev C, that manufacturer must test to all the requirements of that document." To further this goal, the DoD has already discontinued Class C (not to be confused with Rev C) testing from 883.

This was basically the lowest testing level, and did not include burn-in screening of parts, the most important single item in component testing, according to Hnatek. This leaves many manufacturers asking how such divergent interpretations of 883 ever came into existence in the first place. Ambiguity, both of meaning and wording on the government's side, is one part of it. Cost cutting by the manufacturers is part of it too, the DoD claims.

A combination of the ambiguity of 883 and the proliferation of SCDs has led to the many recent cutoffs of parts from such suppliers as Texas Instruments, National Semiconductor, Signetics, Fairchild, and Advanced Micro Devices.

In every one of these cases, highly publicized by the government, the problem has been that the named manufacturers may have made innocent errors of documentation. Also in every case, the parts in question were purchased according to the

(continued on page 52)

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CIRCLE 24

DoD struggles

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requirements of SCDs, not 38510 or 883. With the huge number of SCDs (over 100,000 currently exist), it is nearly impossible for manufacturers to effectively review and test to the exact requirements of each.

The manufacturers involved are very careful in their response to inquiries about the problem. Norman Nuereiter, a corporate spokesman at Texas Instruments (Dallas, Tex), explains that in recent incidents involving parts from his company, there were 6300 part numbers being manufactured and tested for use in military systems.

Each one has now been reviewed, and the formal report of the audit has been submitted to DoD. "We found nothing but trivial differences," Nuereiter says. He blames the SCD process for the problems. Since the same part can be ordered under so many different SCDs, it is very difficult to detect small changes in the test requirements if the customer does not flag them. But worse, Nuereiter dislikes the way his company was abused. "It was a disaster because of the way the Pentagon used the press," Nuereiter says. His complaint is that almost daily the Pentagon would announce some ramification of TI's testing deficiencies to the general press, without hard technical details and without thorough background. Needless to say, TI is supporting the new DoD stance that SCDs should no longer be used.

But if the procurement of parts to an SCD is such a dangerous practice, is it much safer to procure JAN-qualified parts? At DESC, 18 vendors are qualified to manufacture ICs to the standards of MIL-M-38510. According to a DESC representative, six vendors were removed from the qualified list over the last few years. One-third of the JAN qualified suppliers had lost their JAN certification, at least temporarily. A government source said this is a very unusual happening, but any explanation as to how the problem developed would be pure speculation.

The major question that remains is why has the DoD publicized test problems that occur under the SCD program, but not the ones that occur under JAN—especially since some companies appear on both lists?

Is there a good side?

Caught up in the turmoil of the military market, it is easy to forget that the reliability requirements of aerospace programs have paid large dividends to the rest of the electronics industry.

Dan McCranie, vice president of marketing and sales at Seeq Technology, (San Jose, Calif), credits military requirements for many recent gains in electrically erasable PROM development. For example, the shift to TTL-voltage levels for programming, instead of higher voltages originally required, and advances in packaging were among those gains. "Military requirements are so high that they are still driving the advancement," McCranie says. "For example, the market went to leadless chip carriers, almost overnight, to achieve the densities that were needed. And the military has provided the major push toward reliability in the EEPROM market."

—Bill Furlow, Senior Editor

Standardization effort focuses on interchange of design data

An ambitious standardization effort could make it much easier to transfer electronic design data among silicon foundries, computer aided engineering equipment, and automatic test systems. Initiated by semiconductor manufacturers and CAE vendors, the Electronic Design Interchange Format is an attempt to develop a universal format for IC and printed circuit board design data. The initial EDIF specification, released for public review in January 1985, focuses on design and layout information for gate array and semicustom ICs.

"EDIF is an attempt to describe any electronic design in a standard way, so that somebody else can always read and understand it," says EDIF committee chairperson Dick Smith, director of computer aided design and engineering at National Semiconductor (Santa Clara, Calif). To accomplish this wide-ranging goal, EDIF proposes a Lisp-like syntax to define every phase of design—including cell libaries, netlists, mask layouts, test and simulation data, and documentation. Hardware description languages are nothing new, but most are proprietary, and none have attempted to convey the range of information proposed by EDIF.

Since EDIF defines the postprocessing of design data, it should be transparent to engineers. However, EDIF will permit engineers to transfer design data among CAD/CAE tools from different vendors. Ultimately, it will allow transfer of design data to silicon foundries and test data to ATE systems, without a clumsy interface process. Because the interface process is simplified, the data is more likely to be correct.

Wide-ranging effort

Representatives from Daisy, Mentor Graphics, Tektronix, Motorola, National Semiconductor, and Texas Instruments are on the EDIF steering committee. Many other companies participate on EDIF subcommittees. Over 600 individuals from 60 institutions in the United States, Europe, and Japan are reviewing the specifications. "We've been getting support from everybody," Smith says. "It's an incredibly needed thing."

(continued on page 54)

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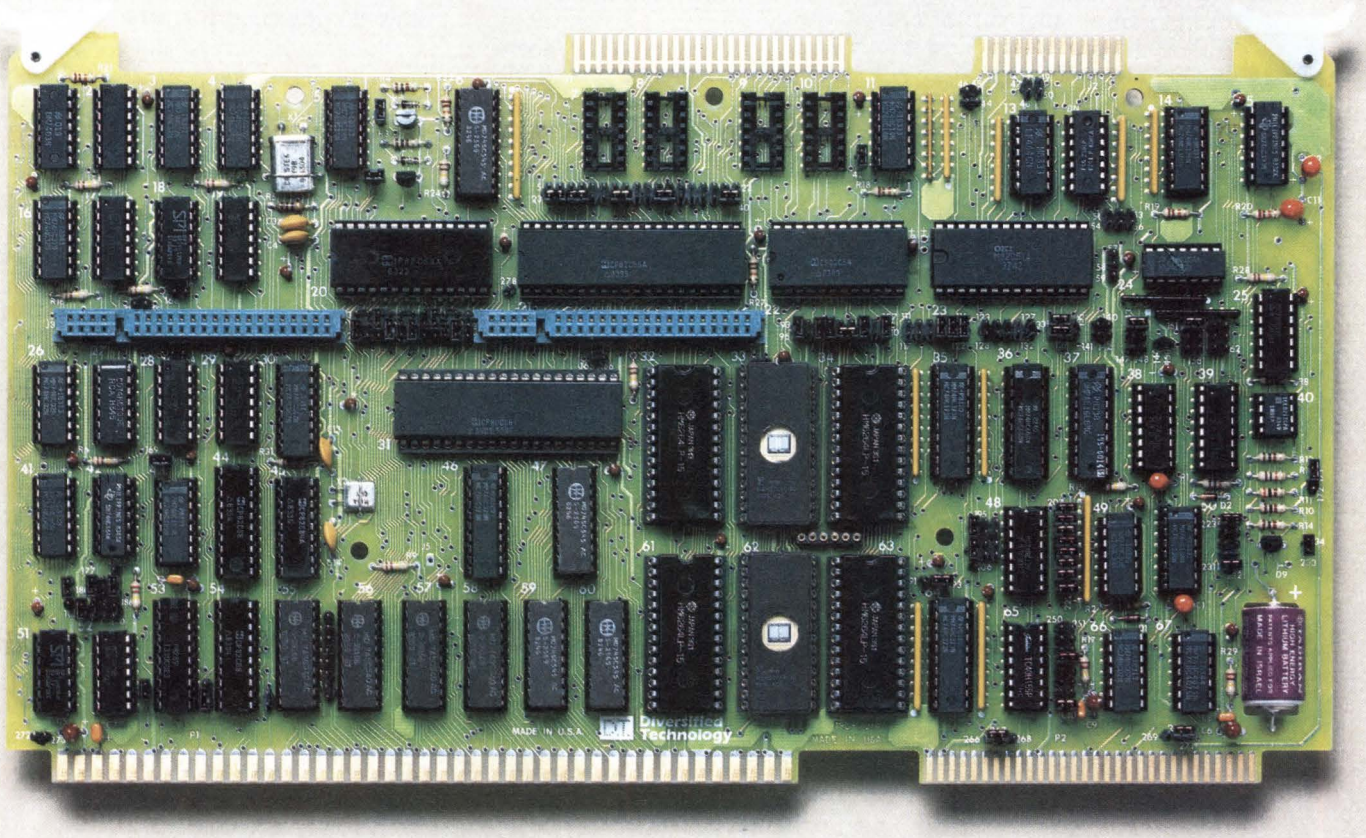

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CIRCLE 25

Inside an EDIF file

Although EDIF has a syntax similar to Lisp, it is a data structure rather than a programming language. EDIF is not executable, and there is no specification on how to interact with an EDIF file. An EDIF file does not have to be complete at any given time—it can contain partial descriptions of a design, or of several designs.

An EDIF file has a hierarchical structure that gets progressively more detailed. It may contain separate cell libraries for a number of technologies. A design block points to a cell within a library that contains the top level of a design. Different representations or "views" of a design are brought together within each cell.

A view is a way of looking at design data. For example, a mask layout view describes geometric figures for representing mask layout; the schematic view defines logic diagrams; the symbolic view specifies symbolic layouts; and the netlist view conveys connectivity information. A view generally includes an interface block that describes the communication between cells and a contents block that represents the contents of the cell.

EDIF syntax supports many types of documentation, including comments within test procedures, annotation in drawings, and full textual descriptions of design elements. A status block documents how and when the design information was generated.

Standardization effort

(continued from page 52)

CAE companies hope EDIF will get them out of the business of designing proprietary interfaces. "Now that we're a workstation vendor, the issue of the Tower of Babel is very much our concern," says Henry Alward, senior software engineer at Tektronix (Beaverton, Ore) and technical coordinator for EDIF. "We want to give our users the facility to pick and choose among foundries, and even other workstations."

Motorola plans to use EDIF to supply its gate array libraries to customers. The Phoenix, Ariz company also hopes its customers will provide routing and simulation data in EDIF. "Up to now, we've been using all kinds of ad hoc methods, none of them very satisfactory," says Mike Waters, senior staff engineer and EDIF project manager. Motorola has eight people working full time on EDIF, and plans to use it whether or not it becomes a standard, Waters says.

EDIF began in late 1983 as an attempt to combine the best features of several existing interface formats. EDIF's Lisp-like syntax is derived from the Common Interchange Description Format, a project of the University of California at Berkeley. Daisy's Gate Array Interface Language and Texas Instruments' TIDAL hardware description language have also contributed to EDIF.

An evolving standard

The initial EDIF specification, version 1.0, is intended to provide all necessary information for exchanging gate array or semicustom data between a CAD/CAE system and a foundry. The specification defines formats for netlists, mask layout, and stimulus/response vectors for simulation. It also defines data usually provided by foundries, including macro libraries, base arrays, logic models, and circuit models.

Topics such as test data formats for automatic test equipment, printed circuit board layout, design rules, and behavioral descriptions will be included in future specifications. These topics are under development by subcommittees. The testing subcommittee, with representation from such companies as GenRad, Hewlett-Packard, and Cybernetics Technology, has recently handed the steering committee a proposed format for transferring data to ATE systems.

Behavioral descriptions may be the most difficult—these provide models for the simulation process. Nobody has tried to develop a universal standard for these descriptions before, and the variety of simulators available will pose a problem. "There are some things nobody knows," Alward says. "You can't design a model for all simulators; and once you have a model, how do you send patterns to it?"

Addition of procedural constructs to EDIF presents another tough issue. This would permit such applications as control of layout tools. Some subcommittee members have proposed links to languages such as Pascal or Fortran while others, such as Alward, feel procedural capabilities should be provided by Common Lisp.

CAE-to-ATE networking

Although the initial version of EDIF focuses on design data transfer between foundries and CAE environments, EDIF will also provide an interface between CAD/CAE systems and ATE systems. CAE-to-ATE networking has become an important issue because of the rapidly increasing cost of test programming. In the absence of an interface standard, a number of companies have developed proprietary interfaces.

The goal of the testing subcommittee, according to chairperson Daniel D'Souza, is to "allow designers to specify a test and directly transfer it to an ATE environment—in a way that's transparent to the designer." D'Souza, staff software engineer at Gould AMI Semiconductors (Santa Clara, Calif) says EDIF should allow engineers to transport test vectors to any EDIF-compatible ATE system. It will therefore complement, and perhaps ultimately replace, some of the proprietary schemes now in existence.

The current EDIF specification includes stimulus/response vectors for simulation. To extend this specification for testing, several additions are needed: ac and dc parametrics, chip initializing sequences, and timing information for driving testers. The initial proposal from the testing subcommittee is basically a procedural language for driving a Sentry-type tester.

Several other efforts are underway to standardize design data interchange. The Initial Graphics

(continued on page 56)

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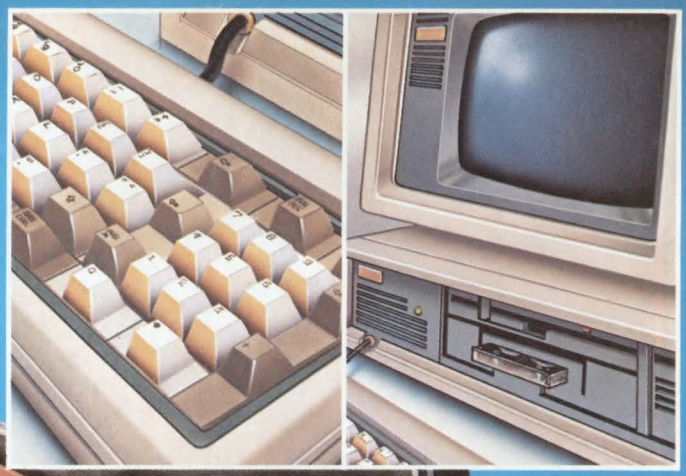

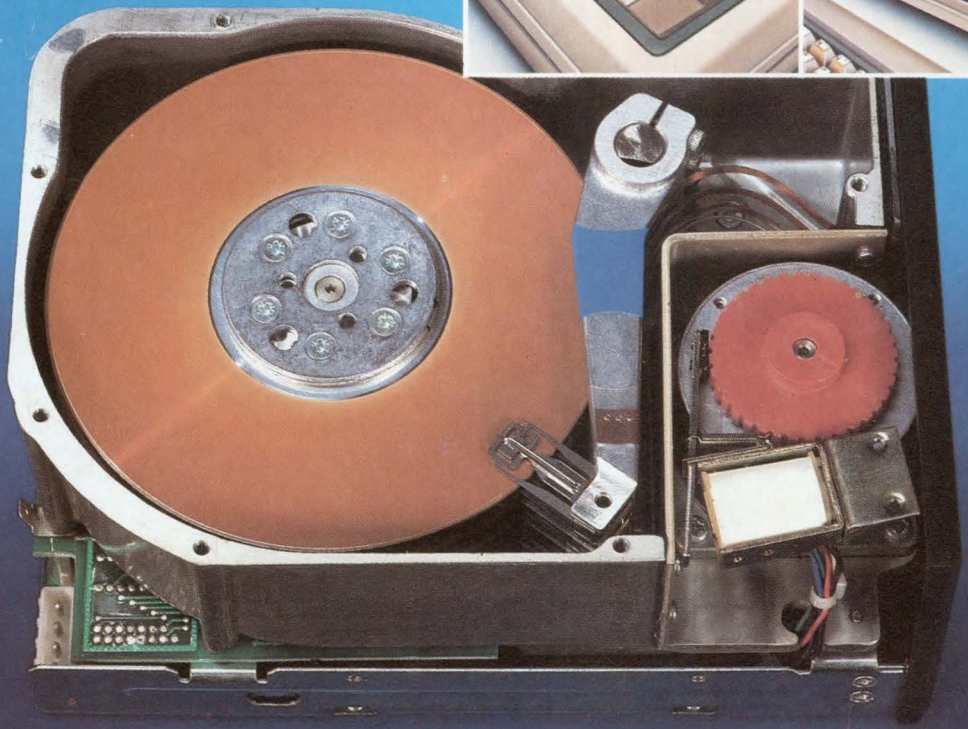

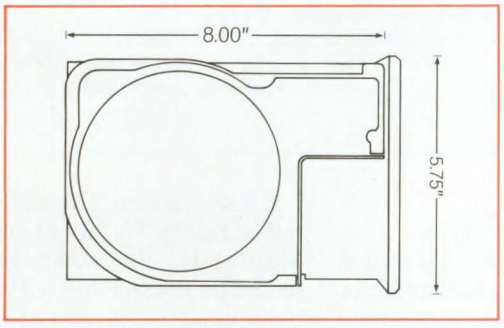

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CIRCLE 27

Some proprietary interfaces linking CAE to ATE

Company	Product	CAE Link	ATE Link	Comments
Cybernetics Technology (Eden Prairie, Minn)	CTAS	Tegas-based workstations, others under development	Viking 200 VLSI tester	Part of automatic test generation package.
Factron (Billerica, Mass)	Daisy-to-Factron interface	Daisy workstations	Factron board testers	Allows downloading of board data, stimulus vectors.
GenRad (Santa Clara, Calif)	Hipost	Hilo – 2 logic simulators	Genrad GR16, GR18; Sentry VLSI testers	Translates logic simulator results.
Hewlett-Packard (Palo Alto, Calif)	Cadvantage	HP, Applicon, Racal-Redac, Computervision, others	HP 3065 board testers	For PC boards. Reformats CAD outputs in test system.
Marconi Instruments (Sunnyvale, Calif)	CADlink	Requires .PCB format	Marconi Series 80 board testers	For PC boards. Also designs graphics for repair stations.
Sentry (San Jose, Calif)	Cadport	Tegas-based workstations	Sentry 20/21 VLSI testers	Translates simulator truth tables into test vectors.
Teradyne (Boston, Mass)	Various postprocessors	Lasar – 6 logic simulator	Teradyne, Genrad, HP board and VLSI testers	Specific packages for each link.

Standardization effort

(continued from page 54)

Exchange Specification, sponsored by the National Bureau of Standards, is an attempt to develop a common CAD interface language. The Institute for Printed Circuits is defining a board-level CAD output format for test systems. The Very High Speed Integrated Circuits project includes a U. S. Department of Defense effort to build a hardware description language. There may be some overlap between EDIF and these efforts, particularly when EDIF addresses printed circuit board layout.

EDIF Version 1.0 will be under public review for about six months. Meanwhile, the companies represented on the steering committee will build implementations of their own. Specifications may be obtained from Henry Alward at Tektronix (Mail Stop 92-826, Box 4600, Beaverton, Ore 97075).

—Richard Goering, Field Editor

SYSTEM TECHNOLOGY

(continued on page 65)

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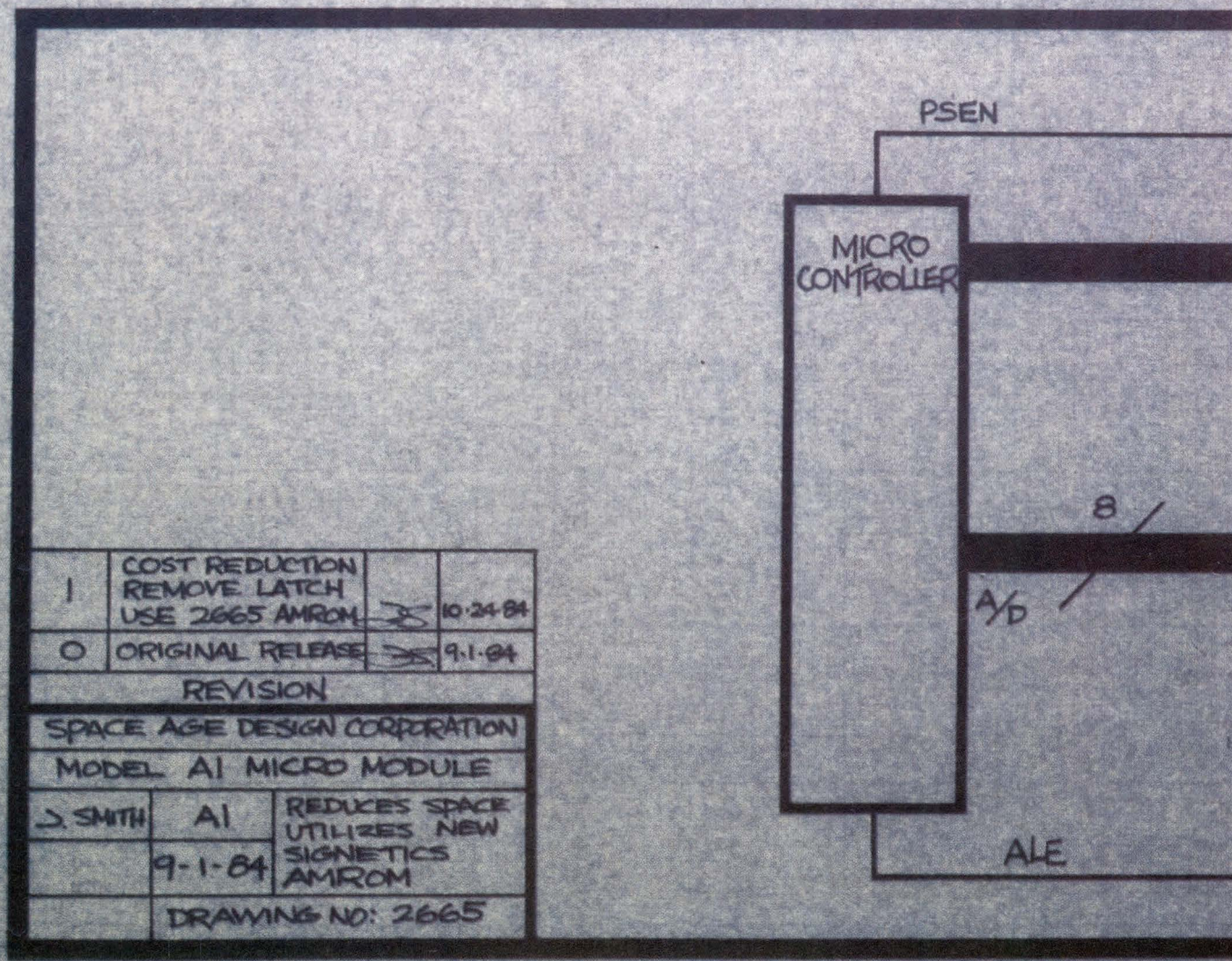

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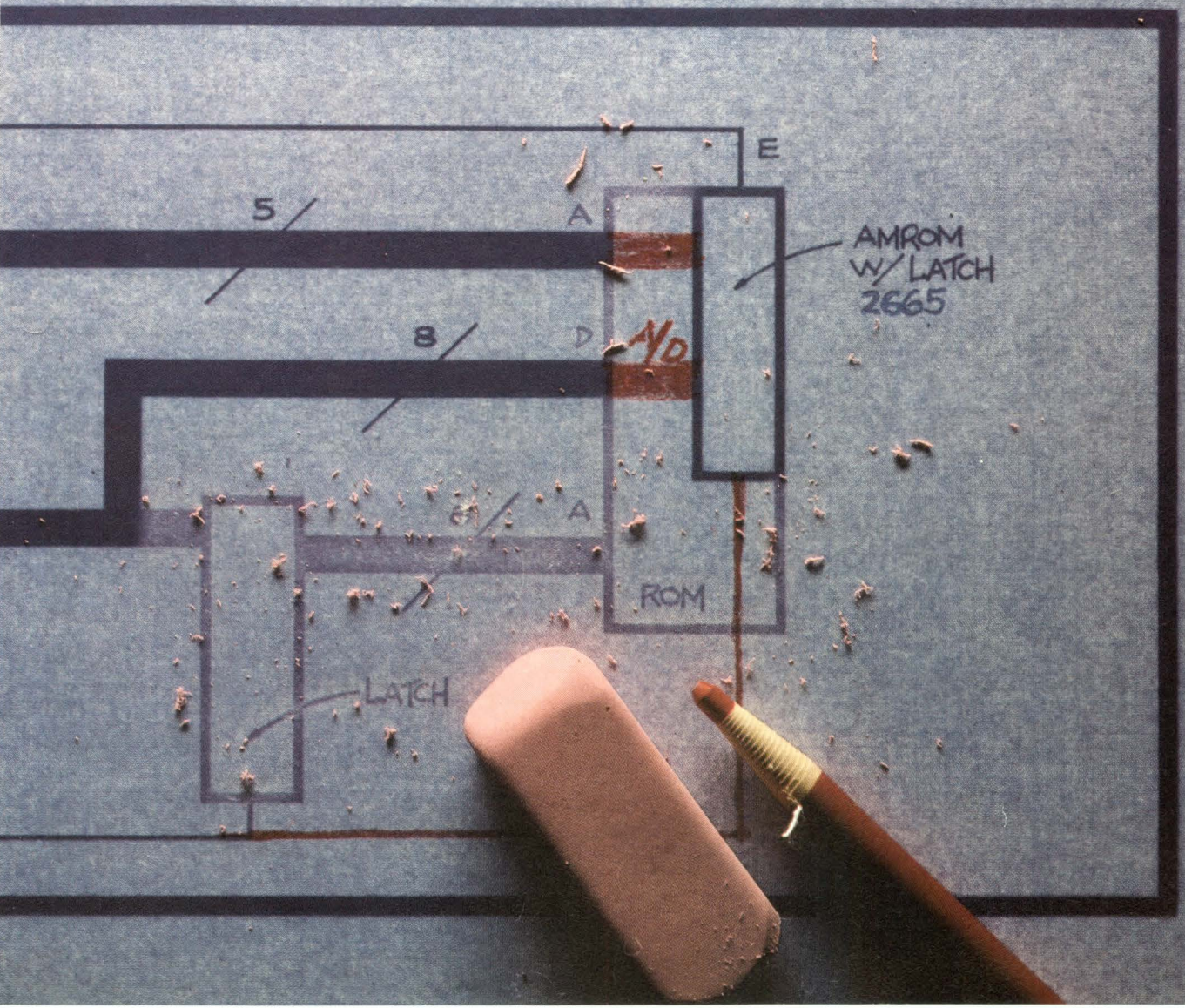

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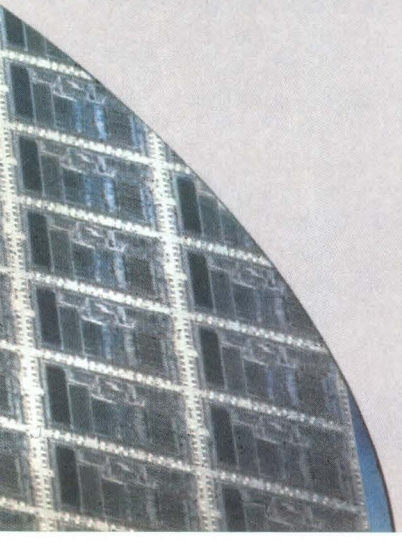

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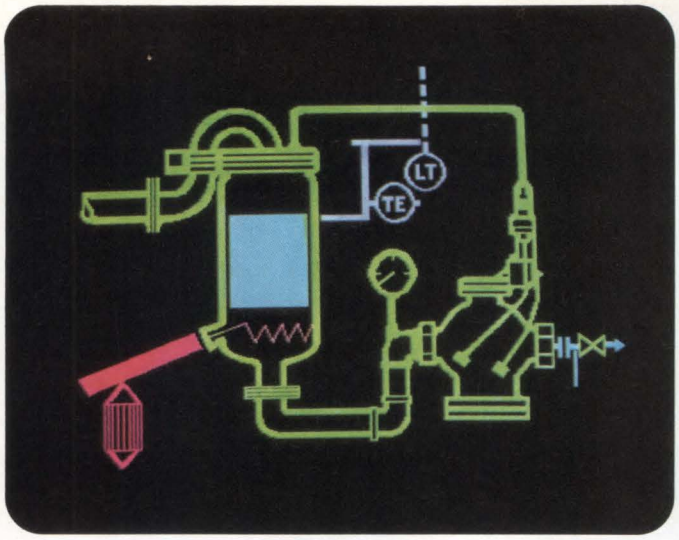

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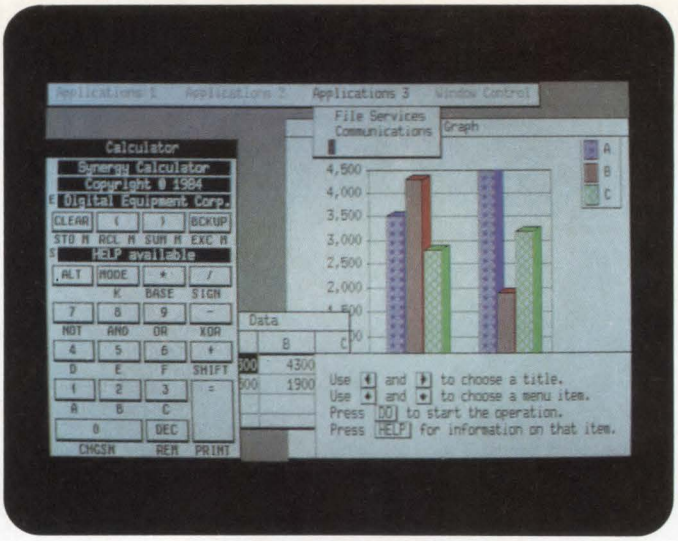

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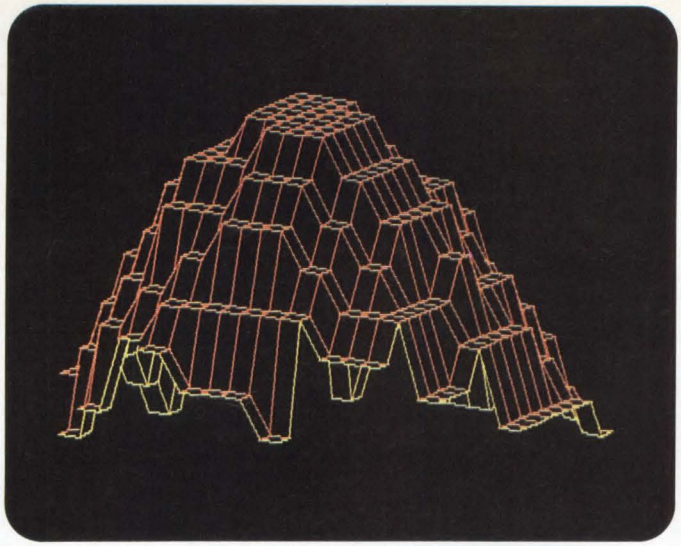

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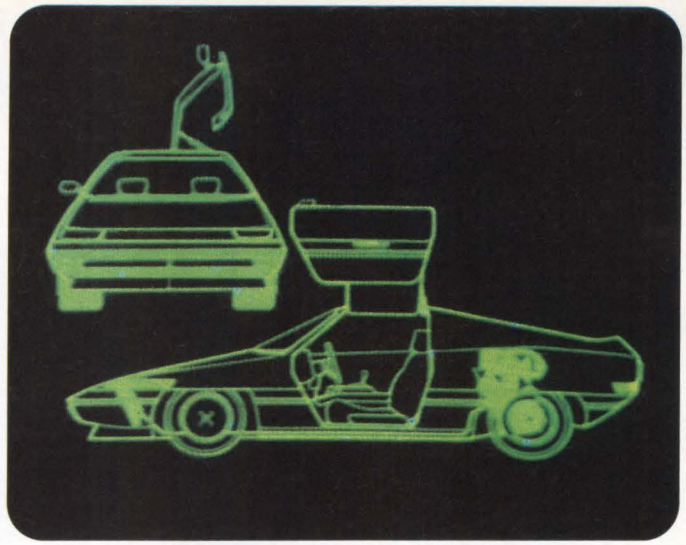

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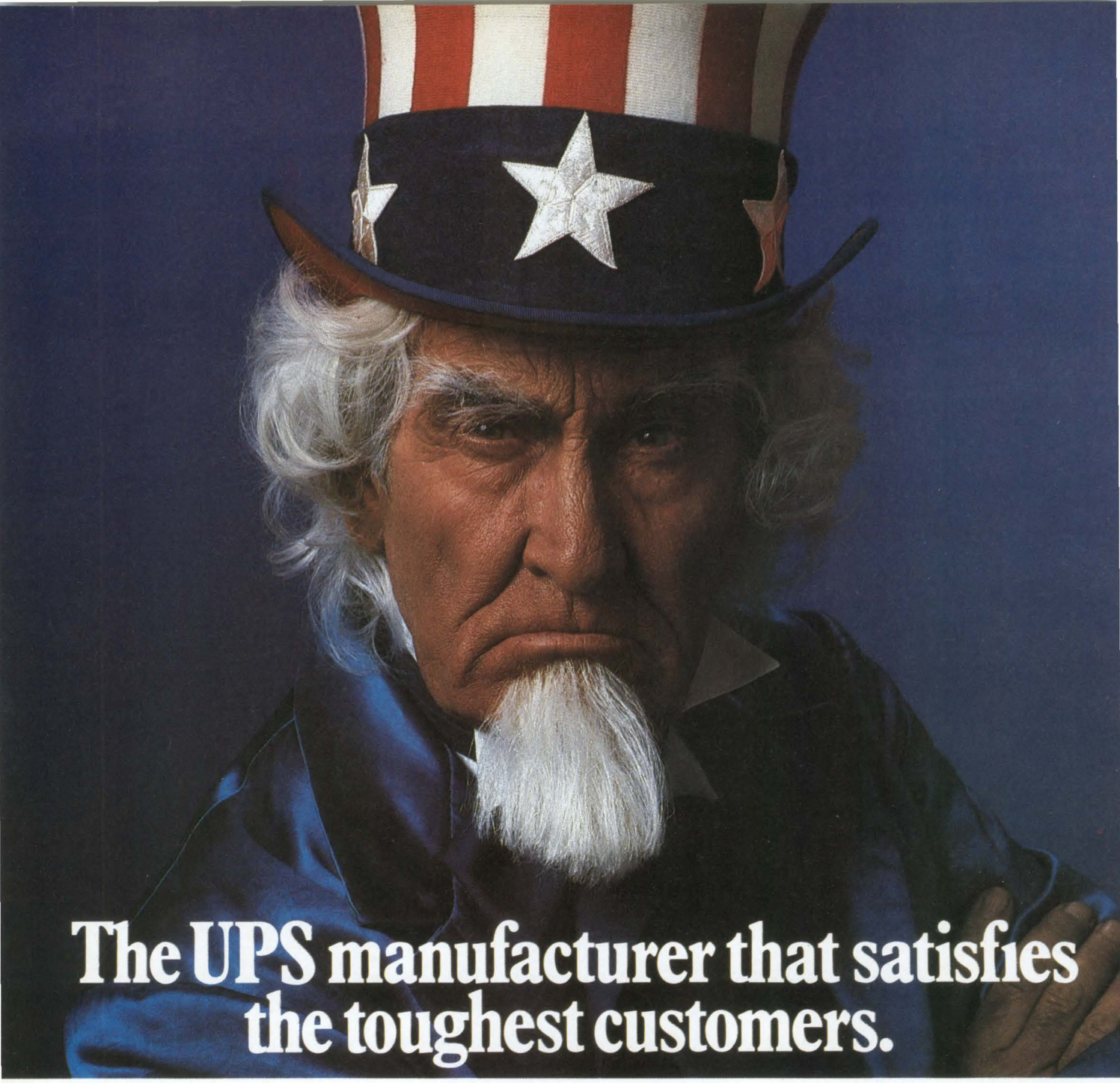

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CIRCLE 30

Changes in CAE/CAD requirements affect workstation design

Just when designers of computer aided engineering/computer aided design workstations thought they had the formula for future products, the requirements changed. Designers made it a tradition to provide standalone systems that could interface with a local area network when necessary. But they knew those systems would need more capability, more power, and lower cost. Now, however, at least one company offers a "dumb" workstation that must be tied into a LAN to access memory.

Sun Microsystems of Mountain View, Calif recently introduced a "diskless" version of this "dumb" workstation. Sun-2/50 workstations share a mass storage disk via high speed paging over an Ethernet LAN. The system runs on Unix 4.2 and is based on an MC68010 microprocessor. From 1 to 4 Mbytes of physical memory and up to 16 Mbytes of virtual address space per process are available.

Another workstation introduced by the company—the Sun-2/160—is also based on the MC68010, but has standalone capability. It can operate in a LAN with compatible equipment from Sun or other vendors. Mass storage options offer from 71 to 380 Mbytes of formatted capacity. Quarter-inch and half-inch streamers are available for backup.

Both Sun systems have 19-in. color displays with 1152- x 900-pixel resolution. Eight color planes can display 256 colors simultaneously from a palette of 16.7 million. The display controller can instantly zoom in integer multiples of 1-16 and pan in increments of one pixel.

Tektronix (Wilsonville, Ore) has also entered the CAE workstation field with its 6000 family, consisting of the 6100 and 6200 series. All units within the two series of "intelligent graphics workstations" are software compatible. There are distinct differences in capability among the members of the two families—but all are standalone/network oriented.

The 6100 series workstations are based on National Semiconductor NS32016 microprocesssors, while all but one of the 6200 series use NS32032 CPUs. (The low end member of the 6200 series uses the 32016.) Memory for the 6100 ranges from 256 Kbytes to 1 Mbyte, storage is handled by a 360-Kbyte diskette, and displays are either 15-in. monochrome or 13-in. color. The 6200 offers 1 or 4 Mbytes of memory, a 40- or 80-Mbyte Winchester for storage, and 19-in. monochrome or color displays.

All members of the family are object code compatible, and most run an enhanced version of Unix. One exception, the 6110 instrument controller, runs its own realtime operating system but executes object programs generated by other family members.

The Tektronix implementation of Unix includes major features of System V and Berkeley 4.2, along with local area networking and demand paged virtual memory for execution of very large programs. Language support includes compilers for Fortran 77, C, Pascal, and the proposed ANSI Basic.

Interfacing options are based on "industry standards": RS-232 and RS-422, IEEE 802.3 Ethernet, Centronics, Multibus, Small Computer System Interace, and IEEE 488. Tying workstations into an Ethernet-based LAN makes them compatible for communication with Digital Equipment

(continued on page 66)

Elements of Tektronix 6000 family workstations interface with one another on an Ethernet-based local area network to make up the unique system required for a specific computer aided engineering/computer aided design application. The system can be used for either mechanical or electronic design and analysis as well as process control.

Changes in CAE/CAD

(continued from page 65)

Corp VAX computers running VMS-compatible Unix versions.

DEC's VAXstation I, also intended for CAE/CAD engineers, is claimed to be the Maynard, Mass company's "first true 32-bit single-user workstation system." The unit is based on a MicroVAX I computer and provides VAX/VMS operating system resources, including high resolution graphics and multiwindowing capabilities. The Graphical Kernel System, which DEC considers to be "the emerging industry standard," is supported by this workstation. Connection to DECnet/Ethernet LANs provides access to larger VAX computers or workstations.

The system monitor is a 19-in., 60-Hz, noninterlaced monochrome display with a 960- x 864-pixel resolution. Full-page documents and multiple windows can appear concurrently, including both DEC VT100 and Tektronix 4014 terminal emulation. A basic configuration includes a 1-Mbyte main memory, 1-K x 2-K bit-mapped video RAM, dual 400-Kbyte 5¼-in. diskette drive, 31-Mbyte 5¼-in. mini-Winchester drive, 19-in. monitor, and a mouse. The Ethernet interface is an option.

Ethernet interfacing will also be provided in the D-2300 CAE/CAD workstation from McDonnell Douglas Automation Co (McAuto) of St Louis, Mo. This tabletop design station is still in prototype stages of development, but it has been shown at industry conferences. Production models will not be available for some months.

This workstation offers dynamic viewing of "extremely realistic" three-dimensional shaded models—including rotation and translation of shaded and hidden line displays. A Megatek Merlin 9200 graphics engine allows a display of up to 3072 x 2304 addressable and viewable positions. McAuto claims this pixel phasing technology allows for "highest number of addressable display positions available in an engineering design station." Furthermore, up to 4 Mbytes of displayless memory are available.

Dual monitors are included in the system. A 19-in. color graphics screen provides a choice of 4096 colors for surface shading from a 16.7-million color palette; a 12-in. monochrome screen functions as a message monitor.

Aria—a standalone color workstation from Applicon of Burlington, Mass—is a VAX/VMS compatible graphics processor. It is based on a 32-bit CPU and includes a 13-in. color graphics terminal, 3 Mbytes of memory, and a 160-Mbyte built-in Winchester disk. The 8-color terminal has 672- x 504-pixel resolution and is driven at 60 Hz, noninterlaced. All of the company's BRAVO! software required for two- and three-dimensional design is included. The Aria workstations can be used as

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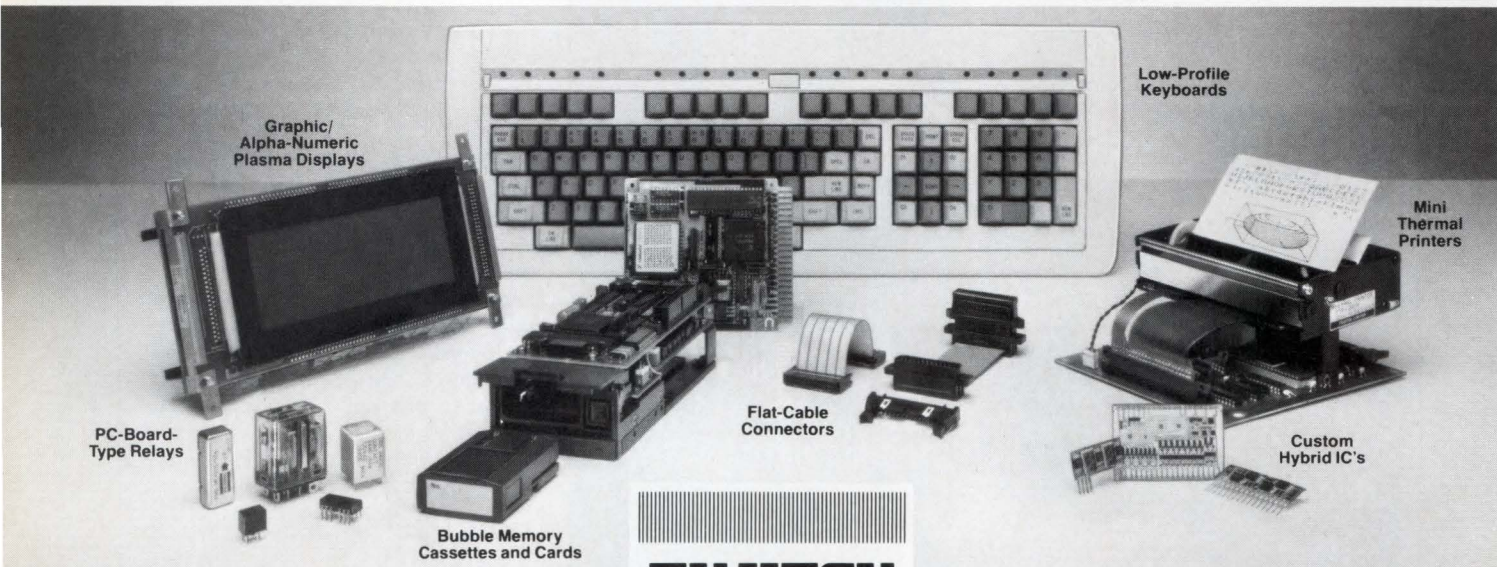

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CIRCLE 31

standalone systems, but they can connect to an Ethernet or DECnet LAN. In this configuration, multiple workstations can be linked to the company's NetServer to access peripherals and mass storage resources.

Celerity Computing's (San Diego, Calif) C1200 professional workstation comes in two versions. Both claim to execute 2 million single-precision and 1.5 million double-precision instructions/s. Up to 24 Mbytes of physical memory and up to 720 Mbytes (formatted) of integrated disk storage can be included. A quarter-inch streaming tape drive is built in for backup. The system I/O bus is Multibus compatible for interface to peripherals.

System software is based on the Berkeley 4.2 version of Unix. The graphics support library is compatible with SIGGRAPH Core standards. Interconnection can be made to systems of other vendors that are compatible with 2780/3780 protocols.

The two systems have different graphics display subsystems; both are color. A high resolution version has a 1280- x 1024-pixel, 19-in. display with up to 24 bit planes of image memory, yielding a palette of 16.7 million colors. Update speed is 9.5 ns/pixel. A medium resolution version has a 640- x 512-pixel, 17-in. display window. Vector writing rate is 1 million pixels/s. An RS-232 19.2-kbaud interface is provided.

Future workstation designs differ

The future of workstations is tied to networking, according to Dr Alex N. Beavers, president of Applicon. "There is a need for more powerful local processing, a lower cost of ownership, and more features and capabilities on a local basis." He says, however, "We realize that engineering workstations by themselves are not the total solution. In fact, an interesting side effect of engineering workstation technology is the need to manage data and data bases over networks—to provide network level functionality."

Many others in the field agree a need exists for dual capability. Jeff Barnell, hardware product manager at McDonnell Douglas Automation Co, for example, said he feels his company's workstations are designed as standalones even though they interface to Ethernet. "Intelligence of the design station keeps the amount of information being passed on the line relatively low. The only time the [workstation needs] to talk to the host CPU is for a database modification," Barnell says.

Networking capability, of course, implies compatibility—with the products of only one company or with those from a number of manufacturers. Ted W. Gary, marketing manager of Tektronix engineering computing systems, says he believes "major customers want compatibility

(continued on page 68)

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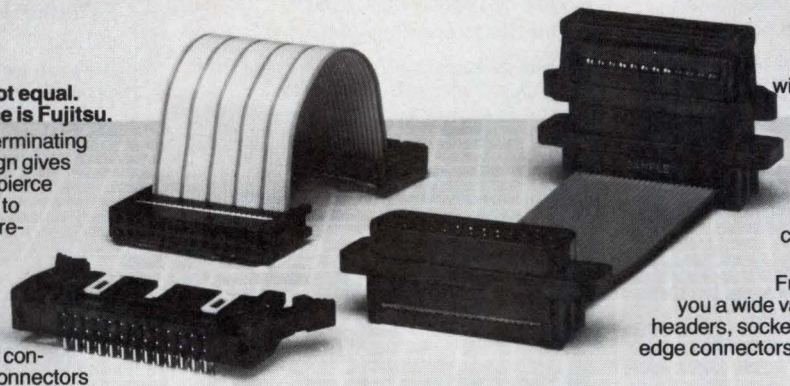

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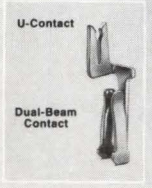

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CIRCLE 32

Changes in CAE/CAD

(continued from page 67)

among their different disciplines." At the same time, "many companies are predominantly—but not totally—either mechanical or electrical. And the electrical engineers must be able to talk to the mechanical and vice versa, or at least talk to a common data base," he says. "Having a family of workstations that can interface over a common network provides the compatibility necessary." Emphasis for future CAE workstation developments at Tektronix will be along three directions, according to Gary. " One is providing the range of processing power. The second is the range of display cases. And the third is software," he says. " We are continuing to invest in these areas—with the intent to improve performance and reduce the price where that is possible."

Gary says he sees a need for standards, and feels that Unix has almost become a *de facto* standard for operating systems already. "Even though there are several variations of Unix, such as System V and Berkeley 4.2, there is enough commonality among them to maintain compatibility. So much software is being developed for Unix that you have more options with Unix workstations," he says.

Some networking standards exist, he adds, "but no one standard is overwhelming." The one receiving the widest acceptance for some time, is the IEEE 802.3, he maintains. This is the Ethernet standard with TCP/IP.

The direction developments are likely to take in the next two to five years, according to Jeff Barnell of McDonnell Douglas, "will be toward a series of low to medium range workstations, each having its own processor integrated into the graphics. Above that you will see very high performance, fully animated graphics design stations, requiring a great deal of power."

Midrange terminals, however, will be able to do anything that high end terminals do now. Some of the dedication to specific tasks now existing on high end systems will be dropped. High end terminals, therefore, will be able to get maximum use of each feature integrated into the software.

—Sydney F. Shapiro,
Managing Editor
SYSTEM TECHNOLOGY

(continued on page 76)

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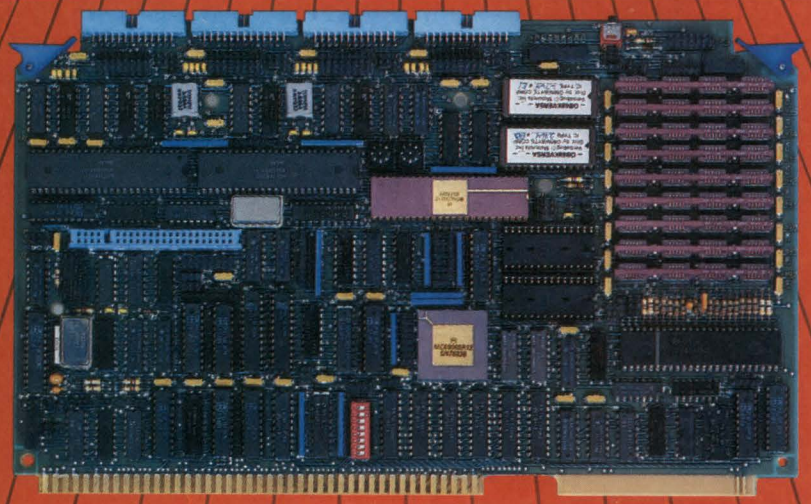

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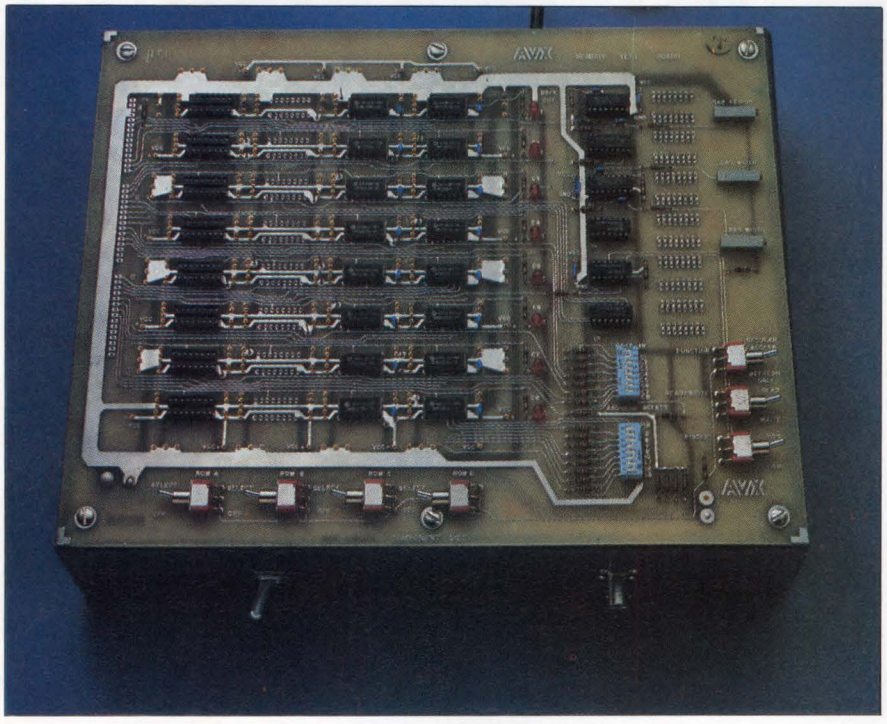

MLC Decoupling of 256-K Dynamic RAMs

A dynamic RAM's sensitivity to decoupling-induced "soft-errors" (random loss of one or more bits of memory) increases dramatically with higher speeds, higher density, and an increased number of sense amplifiers. The new 256-K DRAM designs have large, instantaneous current demands which must be satisfied by a local current source.

That source is the decoupling capacitor directly adjacent to the RAM package. And the capacitor most often used for this application is a multilayer ceramic capacitor (MLC) because of its low series inductance, low series resistance, and high capacitance in a small size.

Test Results

Tests were conducted by AVX on a 256-K DRAM memory board to determine the noise level obtained with various values of MLC capacitors. Figure 1 compares the results obtained using 256-K DRAMs with those from similar board tests on 64-K DRAMs. As indicated, 0.33-µfd capacitors are required on the 256-K DRAM board to obtain a noise level equivalent to that obtained using 0.1-µfd capacitors on the 64-K DRAM board. Performance improvements on the 256-K DRAM

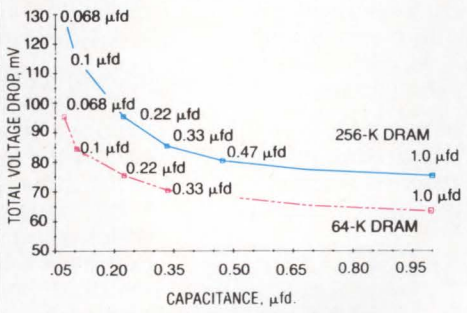

Fig. 1. Decoupling characteristics for 64-K and 256-K DRAMs with AVX MLC capacitors (including V-bump and V-droop).

test board leveled off between 0.33-µfd and 1.0-µfd, indicating that the preferred value for decoupling is about 0.33-µfd.

Figure 2 shows the scope traces obtained during refresh cycle on the 256-K DRAM test board with a 0.33-µfd AVX MLC. In all tests, the general decoupling scheme used was one MLC capacitor for each DRAM, with no board-level bulk capacitors.

Discussion

General-application ceramic formulations, such as Z5U, show considerable change in capacitance with temperature. However, this change has

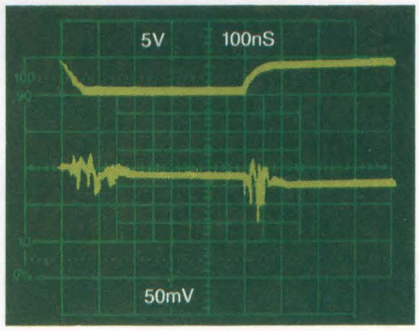

Fig. 2. Scope traces for refresh cycle on 256-K DRAM test board with 0.33-µfd AVX MLCs.

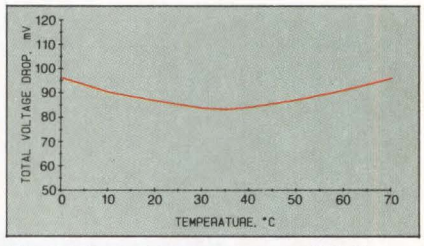

Fig. 3. Effect of temperature on 256-K DRAM decoupling with 0.33-µfd AVX MLCs (Z5U).

little affect on the total noise level for 256-K DRAM when the correct value is chosen. Thus, the 0.33-µfd value is high enough to meet the 256-K DRAM's current requirements over its full operating temperature range, as shown in Fig. 3.

For a complete technical paper describing these tests in detail, complete and return the coupon below.

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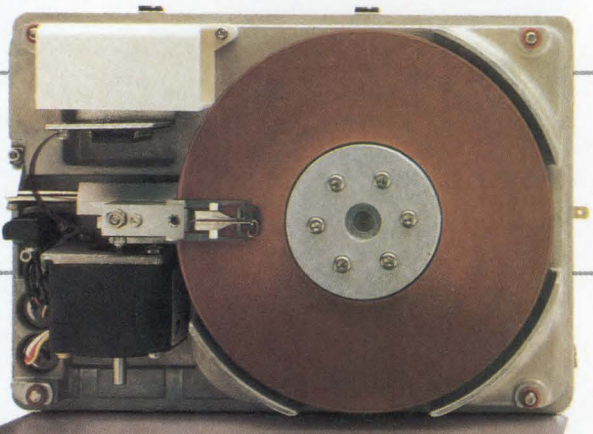

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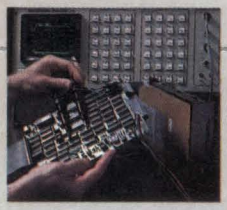

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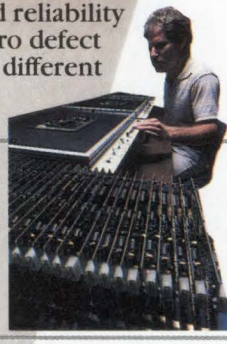

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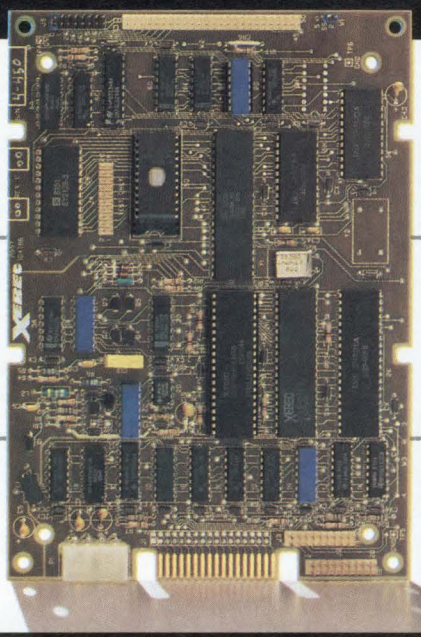

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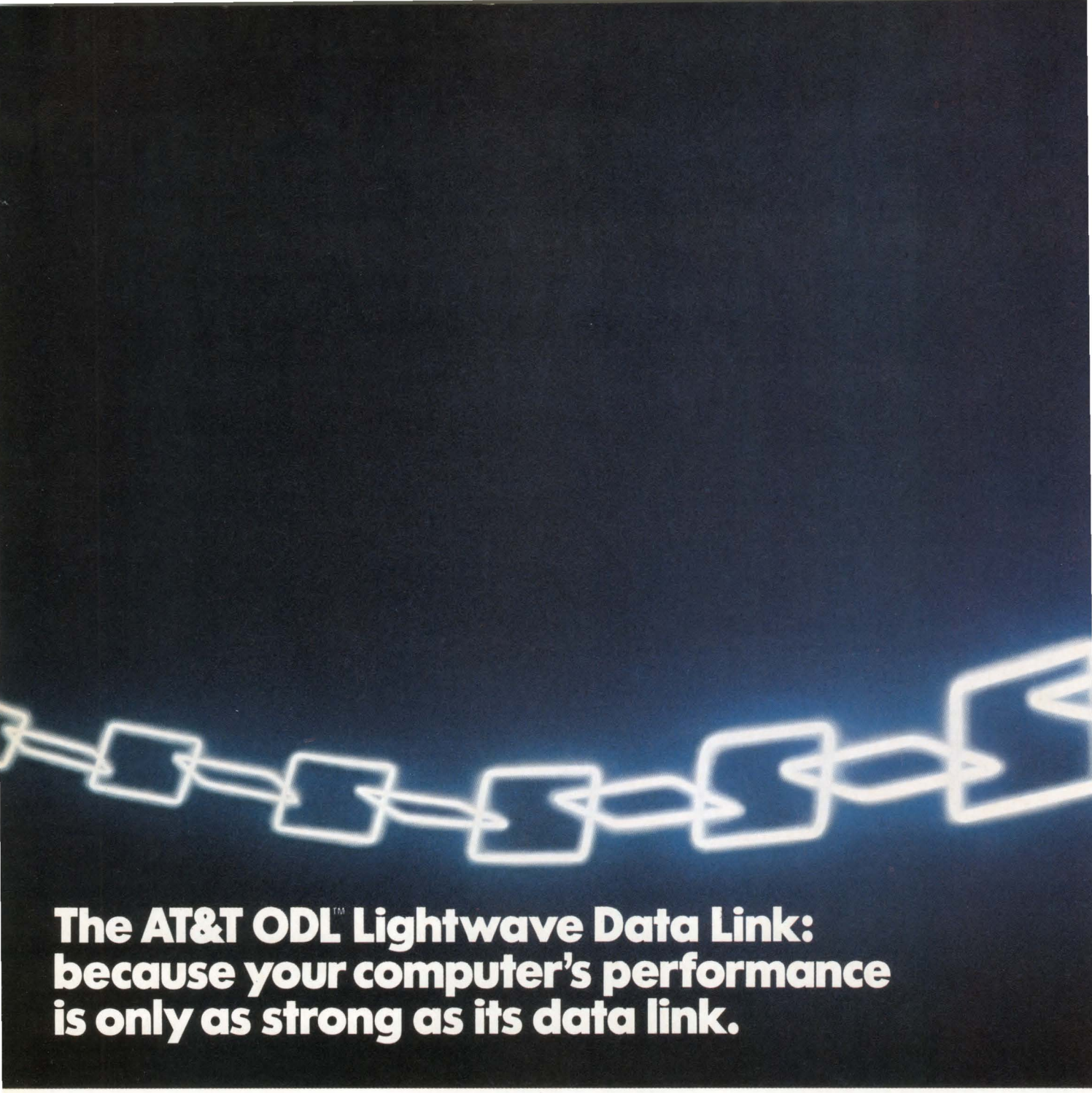

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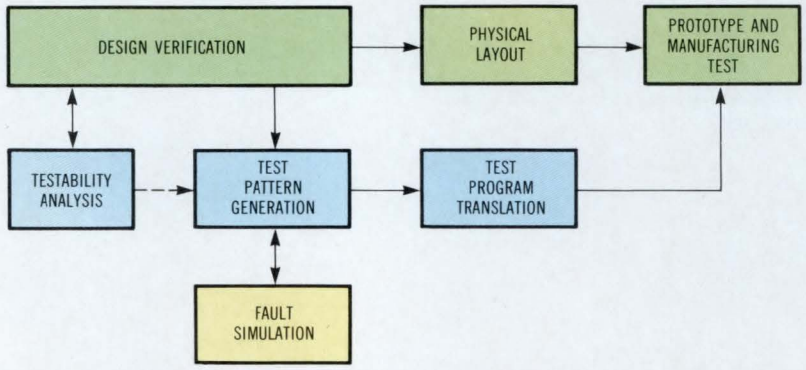
CIRCLE 37

Testability analysis becomes commonplace in CAE environment

The growing complexity of VLSI makes it harder to design products that can be tested. Because untestable products usually come back for expensive redesign, testability is becoming a concern in the design environment. As a result, many companies are turning to testability analysis, a software tool that provides an evaluation of testability and suggests ways to make designs more testable.

Testability analysis is usually sold with a fault simulator, a program for determining the fault coverage (the percentage of nodes that can be tested) for a given set of test vectors. Generally, testability analysis runs after the design verification stage. It is usually an interactive process in which an engineer modifies a design until it reaches an acceptable level of testability. Test vectors are then generated, and the fault simulation is run to see if the vectors adequately test the product.



Testability analysis is generally run after the design verification stage. The engineer modifies the design and adds test points until it can be adequately tested. Test patterns are then generated and fault simulation determines the fault-coverage percentage for a specified set of test vectors.

Proponents of testability analysis say it provides an easy way to help designers build testable products. Since fault simulation is a computationally demanding process, testability analysis can be used first to ensure that adequate test coverage is possible. In addition, testability analysis can help identify such design errors as opens and shorts.

"Testability has been the domain of the test engineer in the past," says John Hengesbach, product marketing manager for the GenRad (Santa Clara, Calif) HITAP testability analysis program. "Now we're telling the design engineer he has to produce a testable design. HITAP gives him a tool to do that." Hengesbach notes the demand for such programs has been fueled by the advent of semicustom ICs.

However, testability analysis is not without its critics. Prabhu Goel, designer of the AIDSSIM fault simulator and president of Gateway Design Automation Corp (Littleton, Mass), maintains that "testability analysis is being oversold. It's very hard to correlate the measures it gives with the actual test coverages you come out with." Although other researchers have voiced the same criticism, vendors of testability analysis programs claim proper use of the programs will give useful and accurate results.

Controllability and observability

Testability analysis measures controllability and observability by examining each node in a product. Controllability is the ability to control a logic value at a node from a primary input. Observability is the ability to observe the node at a primary output. Although each node has controllability and observability values, testability analysis reports usually provide maximum and average values for a circuit.

The Calma (Austin, Tex) COPTR program and the Daisy (Sunnyvale, Calif) Testability Analyzer are based on the Sandia Controllability/Observability Analysis Program (SCOAP). This algorithm, developed at Sandia National Labs in Albuquerque, NM, provides six values: combinational-0 and combinational-1 controllability, sequential-0 and sequential-1 controllability, and combinational and sequential observability. The higher the value, the less testable the circuit.

Combinational-0 and combinational-1 measurements show the number of nodes that must be controlled to set a given node to 0 or 1. Sequential-0 and sequential-1 measurements represent the number of logic states that must be set before a given node can be set to 0 or 1. Combinational observability measures the number of nodes that must be set to observe a given node, while sequential observability measures the number of logic states that must be set to observe a desired value.

Both Calma and Daisy have enhanced the original algorithm. Calma adds a seventh value for test observability called "testability" that shows the number of nodes required for a sensitized value to be observed at an output. A sensitized value is one that changes when a fault is introduced in a circuit that is presumed to be good. Testability can differ from combinational observability if the output of a node is observable only through an unpredictable element.

Calma's COPTR program also serves as a kind of pathfinder for its automatic test generation program. Observability values identify the fan-ins most likely to result in the propagation of a fault to an output. Controllability helps the automatic test generation program select most promising paths and patterns for

(continued on page 78)

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CIRCLE 38

Testability analysis
(continued from page 76)
sensitizing. COPTR is part of the TEGAS-5 based TCAT package. It includes the automatic test generation program and a fault simulator.

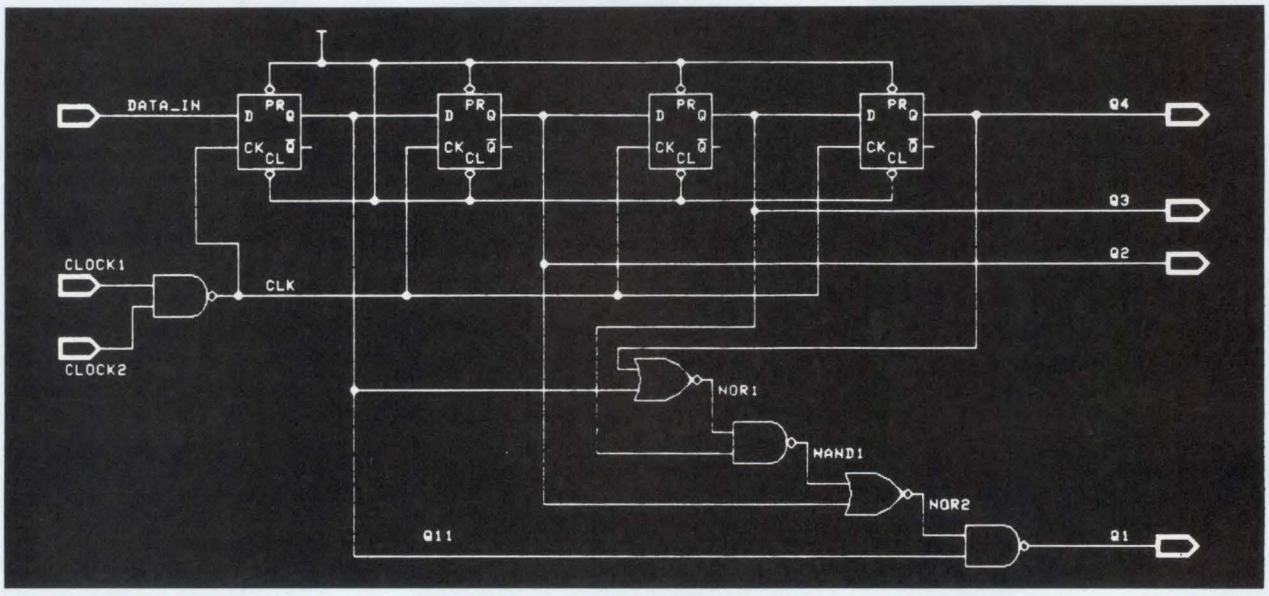
The Daisy Testability Analyzer speeds up SCOAP by adding selective trace, event-driven techniques. It also provides test point insertion commands. These recommend the placement of test points and allow the engineer to add test points without having to edit the original circuit drawing. The Daisy analyzer runs off the same data base as Daisy's fault simulator and logic simulator. This allows it to share common libraries with other Daisy design tools.

Return to CAMELOT

GenRad's HITAP is based on the Computer Aided Measure of Logic Testability (CAMELOT) algorithm, a product of Sears Computers in the United Kingdom. CAMELOT provides normalized values for controllability and observability, with a range between 0 and 1. CAMELOT does not provide separate combinational and sequential measurements, nor does it distinguish between 0 and 1 controllability. However, HITAP can distinguish input that will have a direct effect on output from input that will have a clocked effect on output.

"SCOAP has a large number of controllability and observability criteria," says Hengesbach. "It goes through and acts like a simulator to determine how the paths affect each other. CAMELOT has a set of equations that solve the problem from the outside going in." This approach, Hengesbach suggests, makes CAMELOT-based programs faster and easier to use.

(continued on page 81)




```
                    **** DTA OPTIMAL TESTABILITY REPORT ****

                                          MAXIMUM    COUNT    AVERAGE      %
                                           VALUE    MAX VAL    VALUE    IMPROVEMENT

COMBINATIONAL Ø-CONTROLLABILITY (CCØ)       31         1         8        52
COMBINATIONAL 1-CONTROLLABILITY (CC1)       27         1         7        52
SEQUENTIAL Ø-CONTROLLABILITY (SCØ)          11         1         3         Ø
SEQUENTIAL 1-CONTROLLABILITY (SC1)          1Ø         1         3         Ø
COMBINATIONAL OBSERVABILITY (CO)            18         1         4        69
SEQUENTIAL OBSERVABILITY (SO)                6         1         2        41

MEAN                                         -         -         4        5Ø
STANDARD DEVIATION                           -         -         2        6Ø

THE AUTO INSERT (INPUT OUTPUT I/O) NUMBER IS (Ø Ø 1)

THE OPTIMAL I/O POINT IS          @TVG 1:CLK
```

This sample report from Daisy's Testability Analyzer gives maximum and average values for controllability and observability. It also shows how values are improved by the addition of test points.

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"...investing $675 million in plant expansions over the past five years assures reliable capacity today."

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Ferdinando Beccalli
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CIRCLE 39

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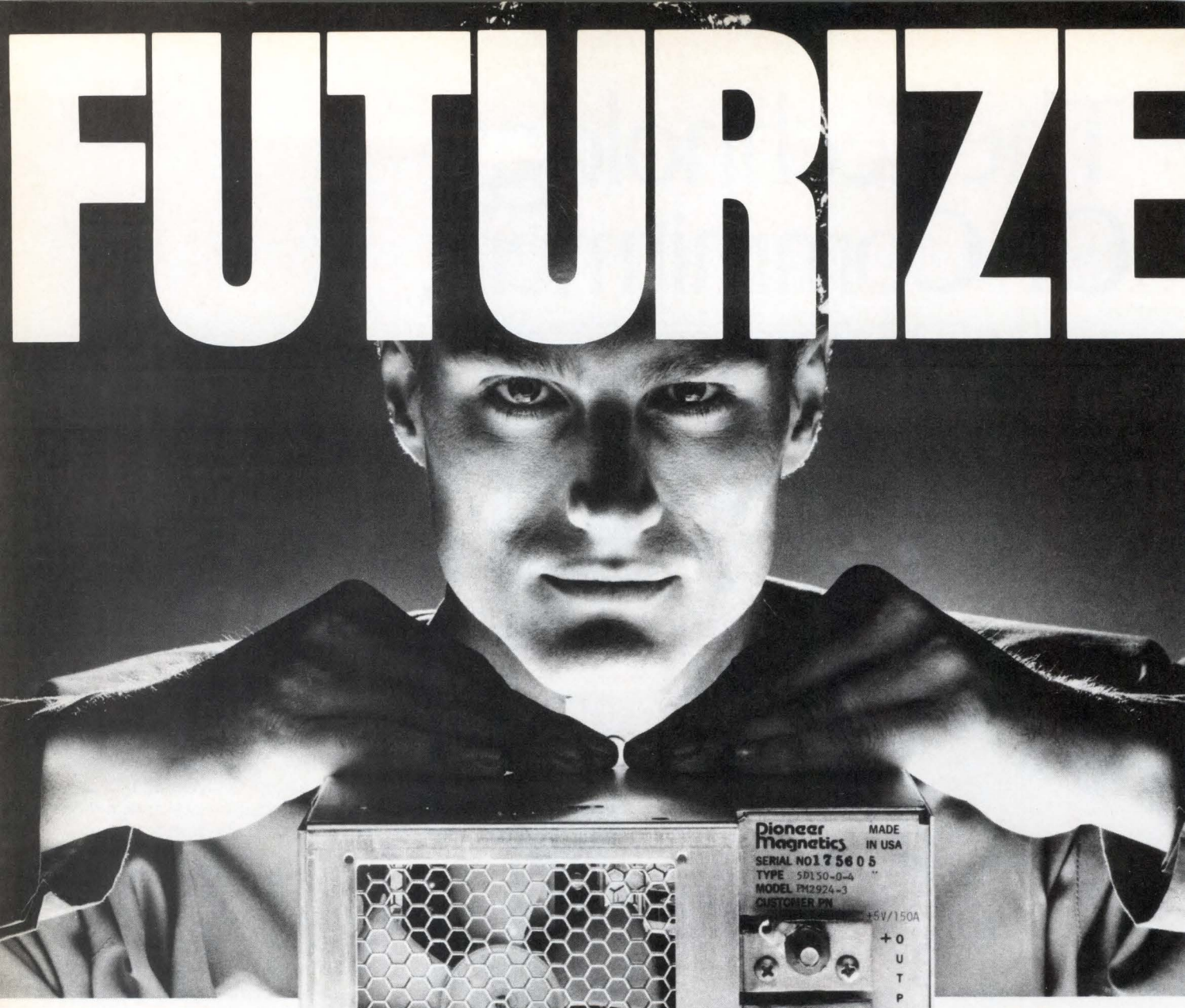

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CIRCLE 40

Testability analysis

(continued from page 78)

HITAP provides ratings of "good," "fair," and "poor" for controllability and observability. Unlike SCOAP, higher values indicate that the design is more testable. HITAP characterizes the range from .1 to 1 as "good," .01 to .1 as "fair," and less than .01 as "poor." HITAP adds a third value, "testability," that is simply a product of controllability and observability.

HITAP also has an algorithm that recommends the selection of specific test points. This repetitive algorithm starts at the least observable node and locates a small number of test points on each pass. The algorithm can be rerun until a desired number of test points are selected.

HITAP can come as a separate package, but it uses the circuit description language from GenRad's HILO-2 logic and fault simulator. "It's pretty dependent on HILO being around," Hengesbach says. HITAP currently runs on VAX/VMS systems, and may be ported to other systems running HILO-2 in the future. It is specifically designed for gate array and standard cell ICs.

Back to the lab

Several research efforts are underway to improve the accuracy and expand the applications of testability analysis. While these efforts have not produced commercial products, they point to future directions in testability analysis, which appear to be blending with fault simulation.

The COP algorithm, an internal product of Bell-Northern Research (Ottawa, Ont), predicts fault coverage for a given number of random vectors without actually simulating the vectors. Thus, it gives a measurement of random pattern testability. COP can also perform fault simulation using random vectors, at a much faster speed than full-fledged fault simulation. COP's designer, Franc Brglez, says his method provides a very high correlation between testability assessments and fault detection.

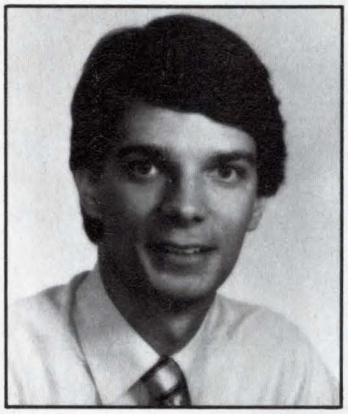
STAFAN, a product of AT&T Bell Labs (Murray Hill, NJ), uses test vectors to calculate controllability and observability as probabilities. It then estimates the fault coverage from these methods—thus, it combines testability analysis and fault simulation techniques. A "test counting" algorithm under development at Tektronix (Beaverton, Ore) estimates the number of vectors needed to test a product from the circuit description. It also helps generate the actual test vectors.

—Richard Goering, Field Editor

SYSTEM TECHNOLOGY

(continued on page 86)

Central Data Acquires AMD Multibus Board Business*



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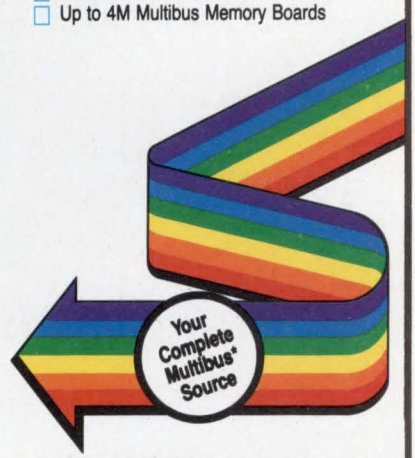

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CIRCLE 41

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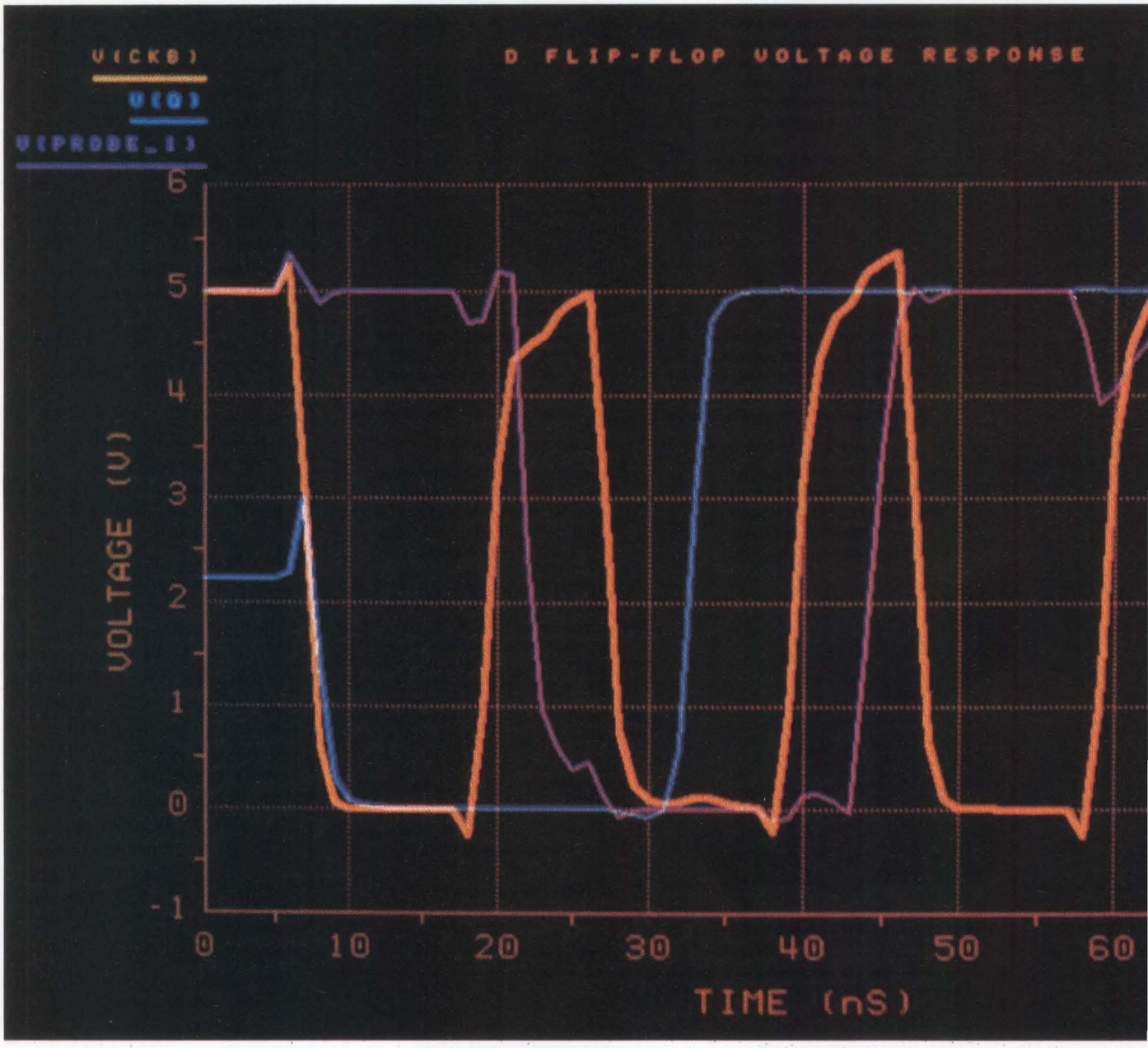

If you're familiar with generic SPICE analog simulation, you're probably aware that the deck is stacked against you from the start.

To change a circuit parameter and see the results, you've got to return to the SPICE input deck, change the value in question, rerun the entire simulation and then review the printed output.

A lot of work just to tweak a resistor, or apply a bit more voltage.

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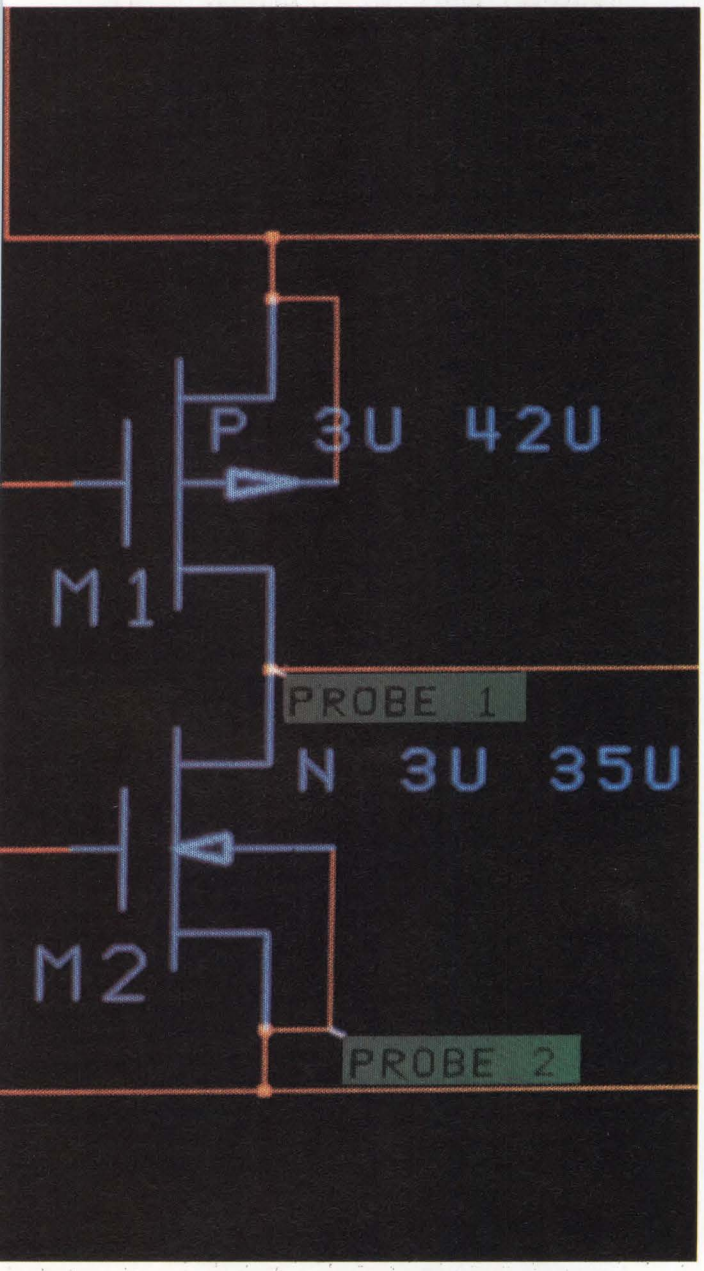

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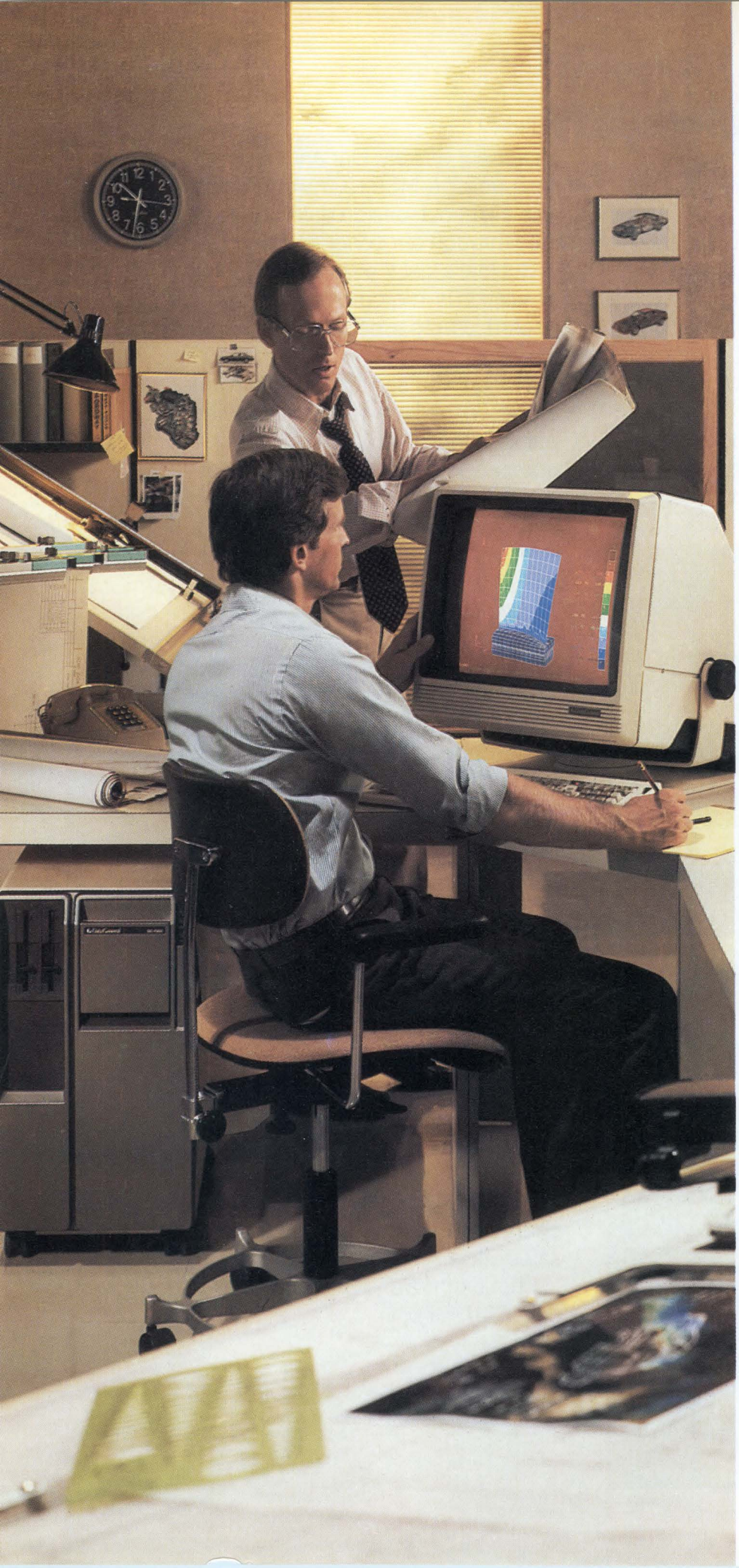

Eliminate problems

The new TMS4161 Multiport Video RAM from Texas Instruments is the first high-density dynamic RAM with two separate and independent ports. You can quickly move data out of or into the memory through the serial port at the same time the CPU is accessing the memory through the random-access port. Thus, the TMS4161 can supply video data to a bit-map display at the same time the graphics processor updates the video memory. This breaks the "bottle-neck" of conventional DRAMs.

A 256-bit shift register is built in on the chip. As a result of this unique architecture, display refresh overhead consumes as little as 4% of available memory accesses rather than the typical 70% required by systems with standard DRAMs. This effectively eliminates memory contention problems inherent in computer graphics systems.

You also quadruple memory update bandwidth through the random access port. And the separate serial port can supply video data to support pixel rates to beyond 150 MHz—with a resolution exceeding 1,280 pixels per line.

These performance advantages are responsible for the Data General DS/4200 advanced engineering work station shown here, which has more functionality packed into an extremely compact system.

Proven technology for greater reliability

The TMS4161 Multiport Video RAM is built using the same proven high-volume technology as TI's industry-leading TMS4164 64K DRAM. Timing for the TMS4161 is compatible with the TMS4164—meaning that both of these top-quality memories can be mixed in the same memory system. Address pin locations are also the same on both devices, making PC board layout easy.

◀ **Improved memory efficiency** is produced by the unique multiport architecture of TI's new TMS4161 Video RAM. It increases memory system functionality while reducing system size and cost for applications such as this advanced Data General engineering work station.

27-4972
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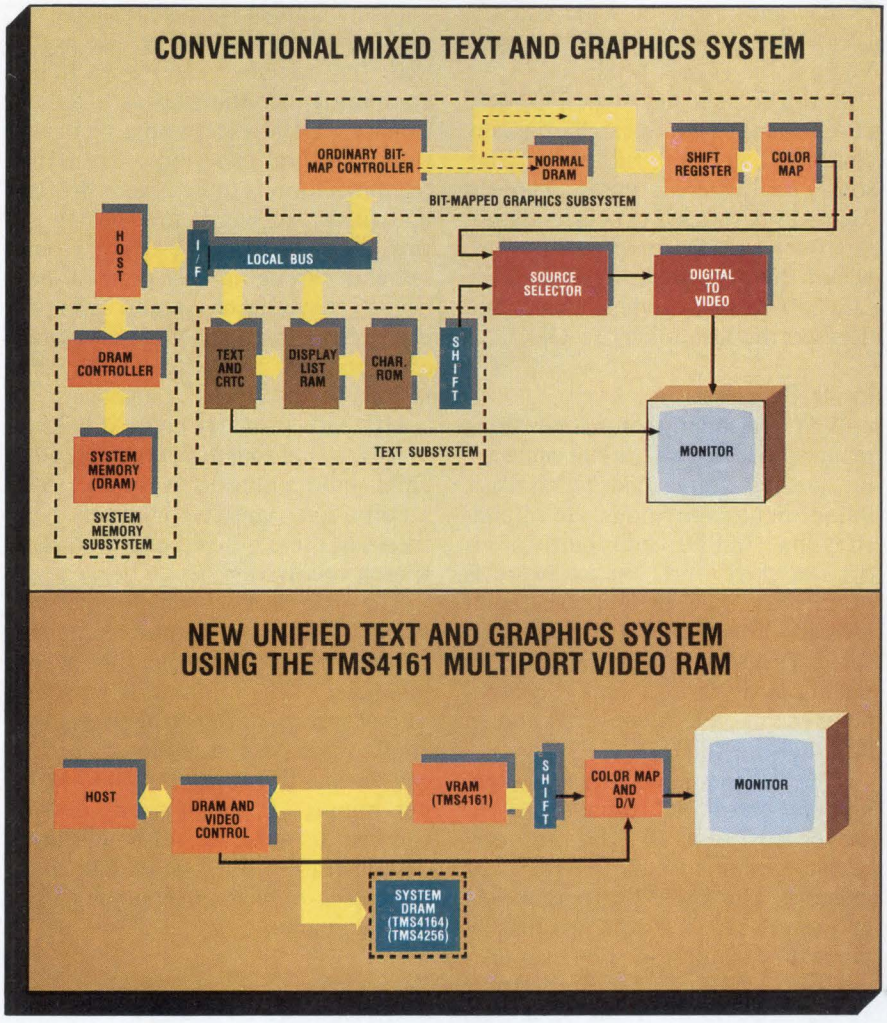
video memory bandwidth with TI's new Multiport RAM.



Major reductions in system component count and board area are achieved by using the TMS4161 Multiport Video RAM in the unification of graphics and text into a totally bit-mapped system.

Design higher-performance graphics systems using fewer parts with new Multiport Video RAM.

Because TI's TMS4161 Multiport Video RAM integrates the shift register and associated control logic onto the memory chip, you can reduce your overall system parts counts dramatically. Thus, system reliability is substantially improved.

As illustrated in the charts above, TI's Video RAM helps unify and consolidate memory arrays, simplifying system design even more. This unification of memory makes feasible new system architectures not possible with single-port memories.

The most significant advances are in the area of bit-mapped graphics. The higher update bandwidth of the TMS4161 allows a major step forward in graphics system design—the treatment of characters as graphic elements in a totally bit-mapped display.

TI's TMS4161 will allow the development of even higher-performance graphics systems, with a more efficient use of memory resources. Your designs will gain simplicity, flexibility, and improved performance with reduced system costs and increased reliability.

Nonvideo uses, too

The dual-ported architecture and the ability to move data rapidly make the TMS4161 ideal for other, nonvideo applications such as image processing of video data streams, bulk data transfers between disk and main memory, radar, and even laser printers.

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Detailed applications information on TI's unique new TMS4161 is available in a

series of five Application Notes. For your set, plus a data sheet and reprints of Video RAM articles, call the telephone number above. For additional technical information, contact the TI field sales office or Regional Technology Center nearest you.

TEXAS INSTRUMENTS

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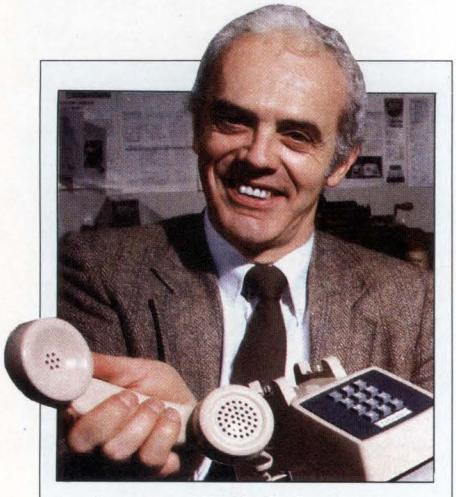
CIRCLE 42

Voice output systems make it hard to distinguish real from synthetic

Synthesized voices now regularly provide information on telephone directory assistance, bank balances, and product inventory. Casual listeners usually cannot distinguish between synthesized and "real" voices and probably don't care. Certainly, workers in a foundry don't care if the voice warning of an overheated unit is real or synthesized as long as that voice is loud—and clear.

Applications for text-to-speech synthesis vary widely. They are now being used for such diverse tasks as proofreading documents during the typesetting process, instructing a jet engine quality control inspector which checks to make next, or telling a maintenance person how to troubleshoot and repair a factory workstation.

The most prominent of the text-to-speech voice synthesizers is DECtalk, from Digital Equipment Corp (Maynard, Mass), but other capable voice output systems do exist. Among them are MITalk-79 from the Massachusetts Institute of Technology (Cambridge, Mass), Prose 2000 from Speech Plus Inc (Mountain View, Calif), and Type 'n Talk and the LVM Business Communicator from Votrax, Inc (Troy, Mich).



Access to DECtalk is commonly made via telephone, as demonstrated by senior engineering manager Walt Tetschner. Capabilities of the host computer determine the number of telephones in any system. A typical VAX-based system, for example, could handle 100 or more access lines simultaneously.

Both DECtalk and Prose 2000 were developed through research originally conducted at MIT, although along somewhat different paths. Type 'n Talk was developed concurrently but separately. Dr Dennis Klatt, a member of the MIT staff, developed the DECtalk software independently and licensed the technology to DEC.

Inside DECtalk

Walt Tetschner, senior engineering manager of DEC's terminal engineering group, claims that DECtalk is unique in its capabilities. He emphasizes that "all DECtalk hardware is off the shelf; only the software is proprietary." The system uses a commercial Motorola 68000 microprocessor, a Texas Instruments TMS32010 signal processor, and support components such as a D-A converter and an anti-aliasing filter.

The 68000 was chosen as system microprocessor, according to Tetschner, because of its 10-MHz clock and because it can address 16 Mbytes of memory. The TMS32010 was chosen because it can perform fast mathematical computation. For example, the TMS32010 can execute a 16- x 16-bit multiplication in 0.200 μs. Because it can perform a basic computation in less than 10 μs, this signal processor has most of its time free for other tasks.

The software approach used for speech synthesis involves three separate levels of processing. In the first, Tetschner says, unambiguous digital representations of speech sounds are generated from 8-bit ASCII text. The character sequences at the input do not matter. At the second level, the digital representations are accepted as input and a total of 18 acoustic control parameters are calculated. These parameters control the third level, which is the synthesis of voice output by digital signal processing.

According to Larry Twaits, a DEC product manager, "This three-tiered approach helps DECtalk achieve authentic human vocal characteristics and unlimited vocabulary." In practice, the system creates speech by comparing incoming words to a dictionary of 500 exceptions, contractions, and abbreviations. Then the pronunciation is pulled from the list and filed. For words not located in this main dictionary, the system searches through a user-defined dictionary that contains jargon and special words. Only 40 phonemic symbols are required to represent all the sounds of the English language.

DECtalk provides eight standard voices—including male, female, and child—and a ninth that the user can modify. Each voice is completely synthesized; there is no recorded human speech involved.

The user chooses which voice or voices will be used. Simple commands permit the user to change the speaking voice, sex, intonation pattern, rate of speech, and special effects for emphasis if desired. Rate of speech can be varied from 120 to 300 words per minute. Pronunciation control can also be achieved (although in a demonstration, the system had considerable trouble in pronouncing this writer's name).

No accents

All DECtalk voices are in "American English" only. "There have been no attempts to achieve regional accents—but this has not caused a lack of acceptance," says Tetschner. The ninth voice, of course, could be manipulated by the system user to develop a special voice if necessary. "We're working on other major languages," Tetschner says, "but none are ready for market. Spanish is likely to be the first foreign language available."

Prose 2000 responds to input of English words or whole sentences in standard computer code. The system dictionary contains about 1500 words. If the required word is not found in the dictionary, the word is assigned a phoneme string and a

(continued on page 88)

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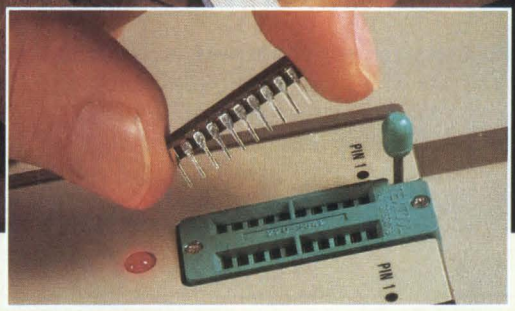

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DATA I/O

Voice output systems

(continued from page 86)

stress pattern is chosen by a set of about 300 context-sensitive rules.

The system controller in the Prose 2000 system is an 8086 microprocessor. Other components include a formant synthesizer, D-A converter, 96 Kbytes of ROM for the program, 8 Kbytes of RAM for retention of temporary data, and Multibus interface.

Alan Yatagai, a Speech Plus marketing manager, says that Prose 2000 accomplishes an accurate representation of the required pronunciation by assigning variants of phonemes based on surrounding speech sounds. This system also uses rules of metrical structure to determine duration of sounds as well as the frequency patterns of words. The result is speech with human-like qualities.

Automatic conversion

Both DECtalk and Prose 2000 are programmed to automatically convert abbreviations, numbers, and symbols to colloquial speech. Lesser systems, for example, would pronounce "St. Botolph's St." as "S T period Botolphs S T period." The more sophisticated DECtalk and Prose 2000 systems would recognize the term and pronounce it as "Saint Botolph's Street." In the same manner, dollar terms such as "$375.25" would be pronounced as "three hundred and seventy five-dollars and twenty-five cents," just as the listener would expect.

Type 'n Talk, according to Tad Jones, sales manager for Votrax's consumer division, is intended only for low end applications. It has a robot-like sound, but sells for only $120.

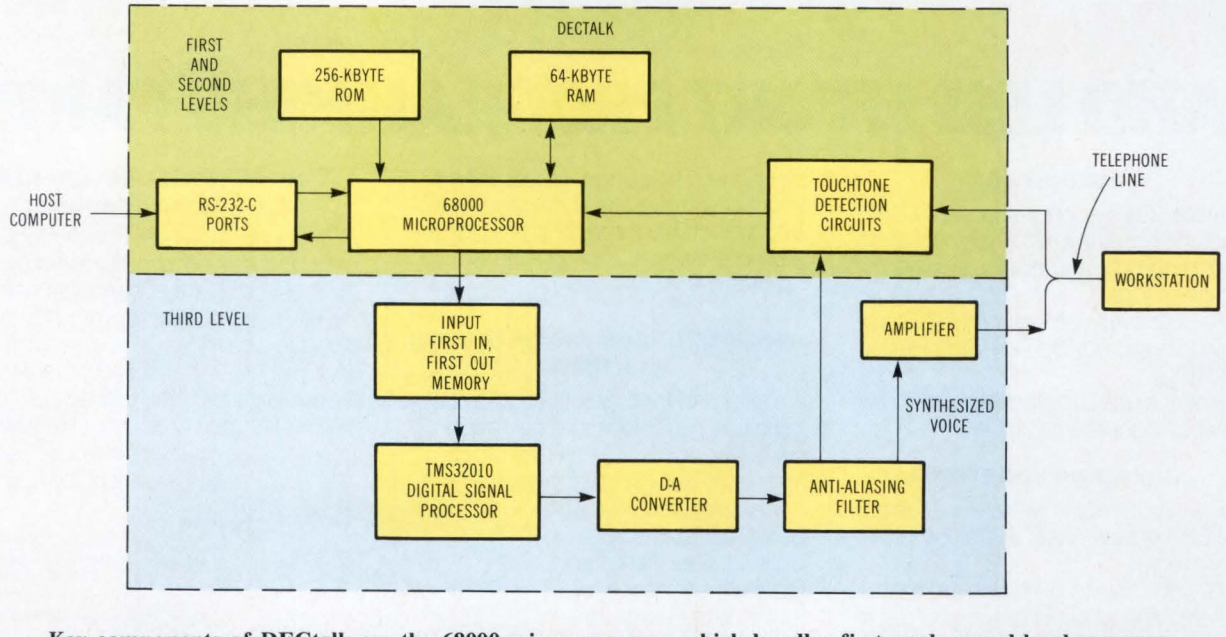
The Votrax LVM Business Communicator, on the other hand, is on a par with DECtalk and Prose 2000 in many ways. It has several voices—both male and female. The customer chooses words and phrases that Votrax includes in a fixed vocabulary within the system's 64-Kbyte ROM. This must be done by Votrax, and field modifications cannot be made by the user. In addition, up to 64 users can simultaneously access the system through a multiplex routine.

At the University of Indiana's Speech Research Lab, Howard C. Nusbaum and David B. Pisoni conducted an independent evaluation of DECtalk, MITalk, Prose 2000, and Type 'n Talk. They found that system capabilities vary significantly, particularly in the quality of voice generation.

In Modified Rhyme Tests, for example, which compare the intelligibility of synthetic speech to natural speech, DECtalk was significantly ahead of the others. At 96.7 percent correct, the synthetic speech generated by DECtalk is now the most intelligible. It is also the synthetic speech closest to the benchmark of 99.4 percent correct observed with natural speech. According to the Indiana University report, test results of other systems varied from a low of 67.2 percent to a high of 93.1 percent (achieved by MITalk-79).

Greater consistency seems to have been achieved with male voices as compared to female voice synthesis. For example, the study found that for word recognition in meaningful sentences, listeners identified 95.3 percent of the words correctly for Perfect Paul (a male voice), compared to 90.5 percent for Beautiful Betty (a female voice).

(continued on page 90)



Key components of DECtalk are the 68000 microprocessor, which handles first- and second-level processes, and the TMS32010 digital signal processing chip set, which handles voice synthesis on the third level. Half of the 256-Kbyte ROM is used for the basic dictionary. The input first in, first out buffer decouples the high speed signal processor from the slower second-level process output.

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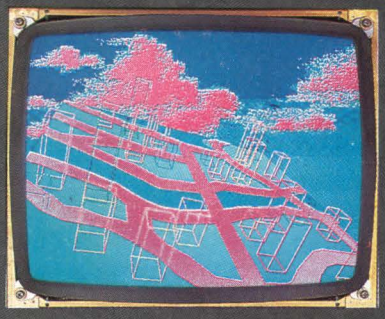

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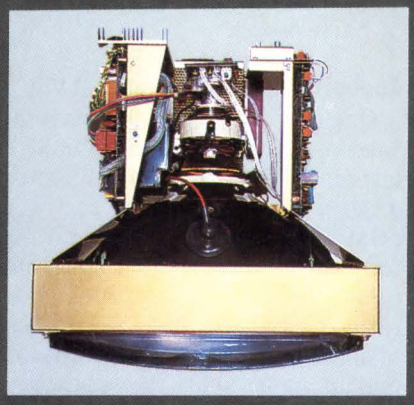

same monitor in every system you sell no matter where in the world it is used.

Keeping a low profile
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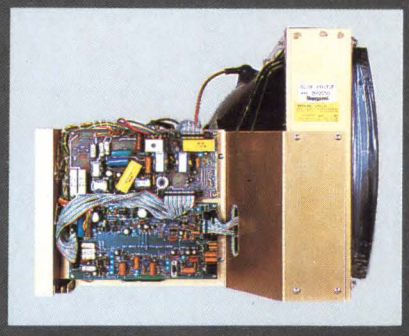

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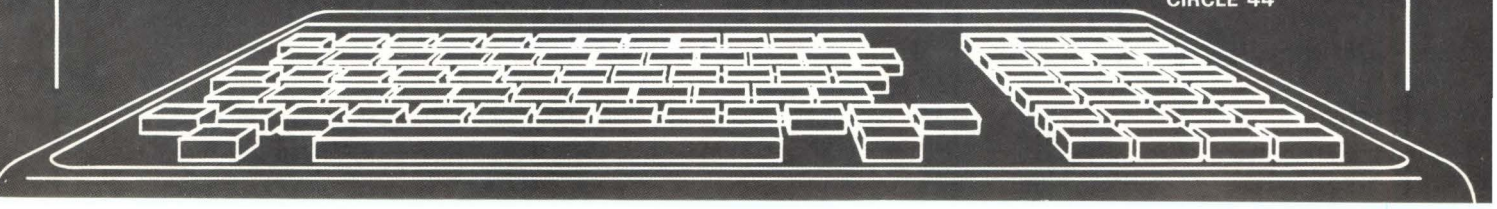
CIRCLE 44



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Voice output systems

(continued from page 88)

Applications—potential and actual—vary over a wide range, within many areas of automated office operations, factories, and the military. A typical voice synthesis response system might include a mainframe computer with 35 to 100 or more telephone lines. The 35 to 100 or more lines, therefore, could accommodate that many calls simultaneously. Systems are limited only in the number of phone lines that can be connected economically. The computer can handle an almost unlimited number of passwords.

Applications increase productivity

One factory application for synthesized voice involves a critical series of inspection steps in the manufacture of jet engines. The procedure is very detailed and the inspector must perform and verify every step. This often means that the inspector must move from one part of the inspection site to another and back in order to carry out all steps. With the synthesized voice system, the inspector receives verbal instructions at various points in the inspection routine and indicates completion of the inspection step by inputting information on a portable touchtone device. The Government Printing Office, which produces the *Congressional Record* and many other critical federal documents, is experimenting with a synthesized proofreading system. Normally, the GPO uses 900 proofreaders, who perform two-person proofs. In this procedure, after a document has been input to the typesetting system, one person reads the input copy from a CRT screen and a second person compares that copy with the original. Only after verification is the copy typeset.

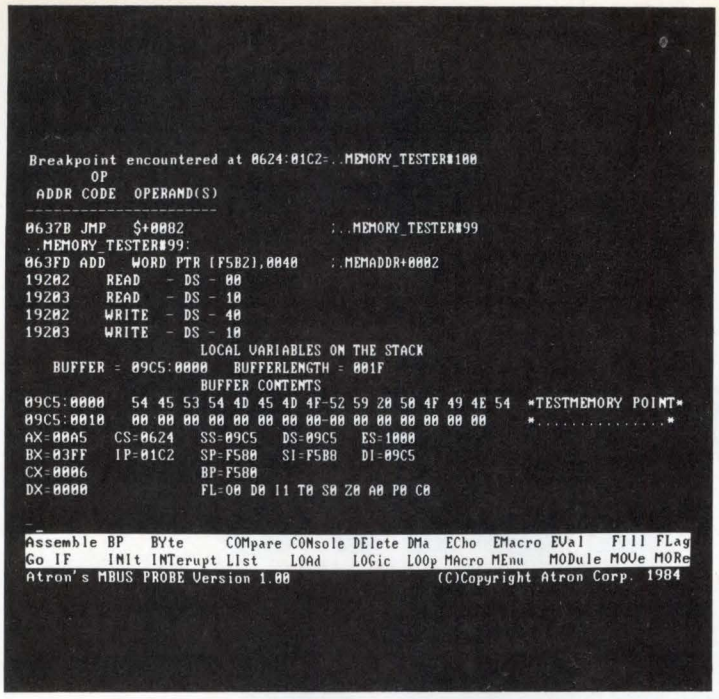
If the synthesized voice system is accepted, the proofreading staff will be reduced to about 100. The system will "read back" the input copy and the only human proofreader required will be the verifier. Most important, however, accuracy will be improved. Very often, a human proofreader sees what that person expects to see, not what is actually there. The synthesized voice system, however, reads back exactly what has been input. Another practical application for synthesized voice systems is programmed instruction on an assembly line. This has routinely been accomplished by "written" instructions on a CRT. "Many people follow voice instructions better than those viewed on screen," Tetschner says. "There are also time/motion savings with voice instructions because the eye movement from screen to work object and back to screen is eliminated." And, according to Tetschner, verbal instructions are more efficient. "In some areas of the United States, many members of the work force often cannot read English. Most, however, can understand English with little problem, and English verbal instructions are therefore effective."

Other industrial applications of synthesized speech response have achieved success. At a large aluminum producer, a Votrax LVM Business Communicator operates with a monitoring system in the company's pot lines. The speech subsystem gives critical information such as "temperature is too high at pot line number three" or "pot line two is losing energy" verbally rather than in a visual display that humans in the system might miss.

Military applications now being studied by such companies as TRW and Raytheon, Tetschner says, include experiments with cockpit simulation and training aids for pilots. Other systems are being developed to give weather reports to pilots for preflight checks—as well as to skiers before they head for the mountains.

Despite dramatic improvements in realism of voice synthesis systems, costs of most such systems are still too high for many applications. Telephone companies, banks, and other large organizations can afford to amortize the costs over long periods and for extensive use. They can afford the sophisticated synthesis systems—the ones that sound real. Smaller (and possibly less profitable) companies, however, must accept the crude "robotic" sounds of the less expensive systems or choose to have humans answer their telephones.

—Sydney F. Shapiro, Managing Editor



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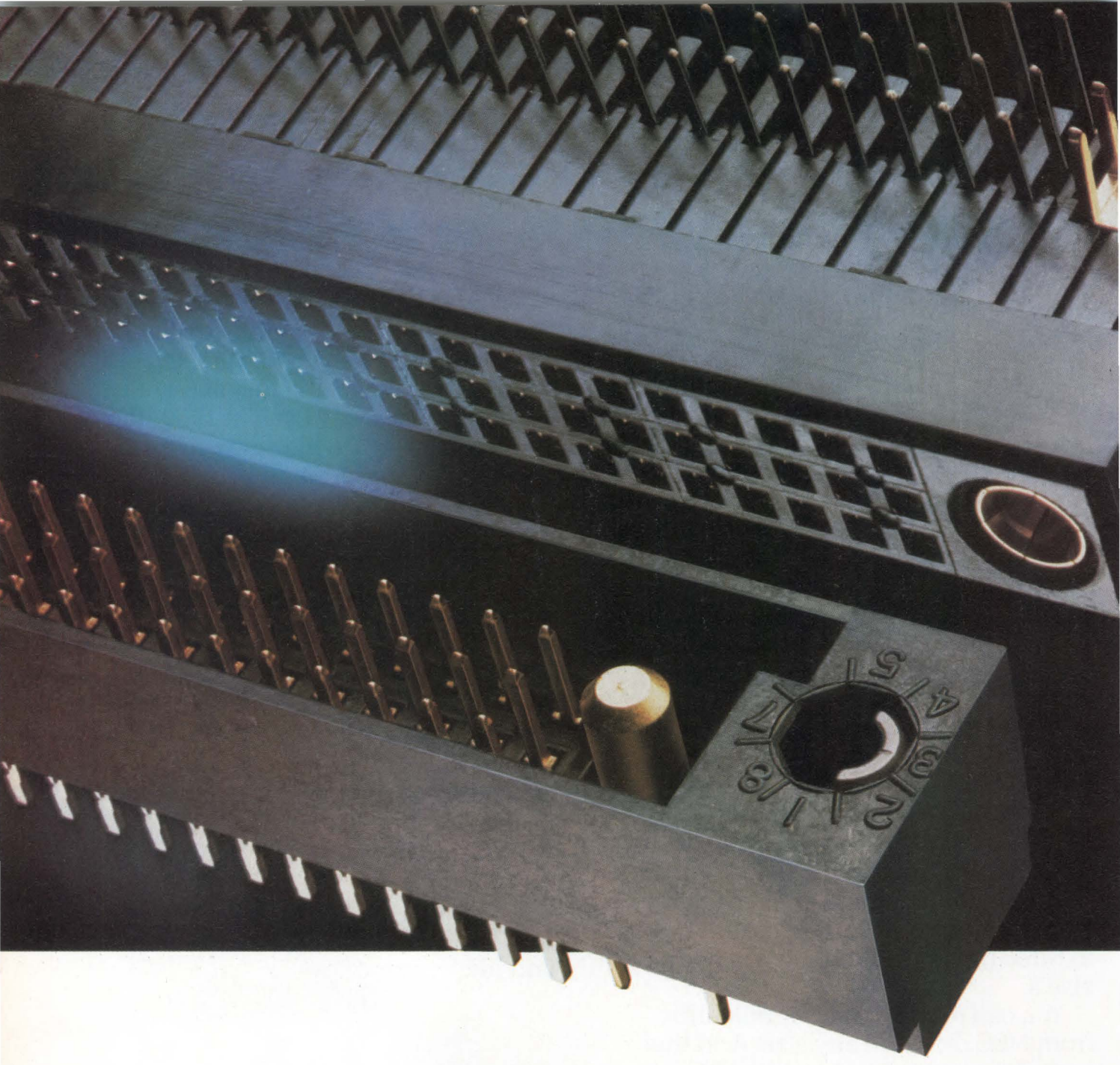

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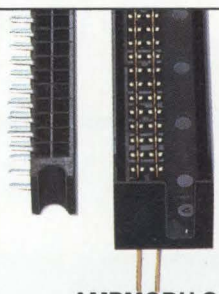

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CIRCLE 49

SPECIAL REPORT ON

DATA COMMUNICATIONS

With the flurry of activity in new local area networks and the influx of personal computers (serving as intelligent nodes and making these LANs practical), the year 1984 can now be proclaimed "The Year of the LAN." Market figures, analyzed by at least one research firm (International Resource Development, Inc of Norwalk, Conn), show that 3.1 million personal computers were sold in 1984, with 4.5 million expected to be sold this year. This increase, coupled with the projected growth of the OEM LAN market from $300 million in 1984 to $405 million in 1985, makes the LAN a viable technology in data communications. Thus, if 1984 is labeled "The Year of the LAN," then 1985 can be called "The Year of the PC LAN."

With this healthy LAN market come the technical challenges of connecting LANs with each other, and with larger, wide area networks. Whereas technologies for LANs are primarily hardware components that meet the specifications of the first two layers of the well-established Open Systems Interconnection (OSI) model, the challenges to interconnecting networks lie in developing protocols for the upper five layers of the model. And the farther one moves up the layers, the more software intensive the challenges become.

Now that LANs are a dime a dozen, being able to choose the proper configuration for specific applications makes life easier for the system designer. And, as more standards are defined, designers who opt for a LAN that adheres to one of the IEEE 802 standards will find that these LANs have a better chance for continued availability and support than those that do not.

Until the protocols for all levels are developed, several approaches to network interconnection offer some relief to the designer. If the need to link different types of networks is unavoidable, gateways are one solution. Gateways have the necessary protocols converted at both ends of the communication path. (This avoids centralizing the conversion process in a large switch.)

The international packet-switching X.25 protocol can act as a switch for different LAN configurations. Designing gateways for the X.25 network is a matter of implementing protocol translators in VLSI chips. With the OSI model as a standard and the availability of VLSI network controllers, such gateway design is possible.

With today's plethora of communication protocols, designers must implement different ICs for each individual protocol. To overcome this problem, semiconductor companies are developing chips that can be used with several protocol standards simultaneously, and with minimum additional hardware.

Nicolas Mokhoff
Senior Editor

Where will your network be after the fault?

ABLE's ATTACH System keeps your CPUs and terminals on solid ground. ATTACH, the multi-host terminal network system for DEC UNIBUS computers, provides the level of fault tolerance required for any application.

ATTACH can guard your system and users with fail-safe rerouting onto redundant paths. ATTACH hot-swappable modules maximize uptime because failed modules are replaced without interfering with the continued operation of most users.

FULL REDUNDANCY

The ATTACH network can be configured for complete redundancy. Should one ATTACH subsystem or module fail, users can be detoured around the failed component. On-board battery backup sustains configuration assignments in memory for up to one month.

1,000 terminals or more can access the many host computers in the ATTACH network, with each computer requiring only a single host interface and single cable to support 128 terminal users in remote or local sites.

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In an ordinary multi-host environment, if one host computer goes down, lots of users could be left sitting idle. The ATTACH network system eliminates user down time, by allowing users to switch to a working CPU, maximizing human and computer resources.

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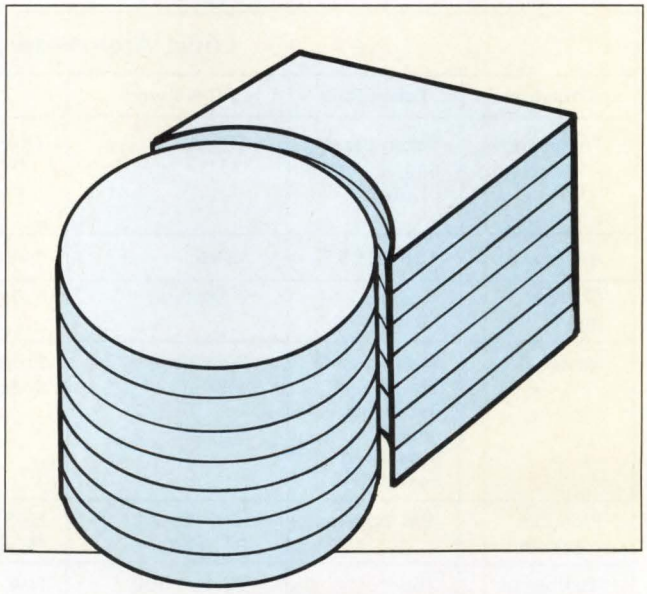
CIRCLE 50

LANs TEAM UP TO WIDEN THE NETWORK CONNECTION

The next step in creating a global network is developing protocols to match those of different local area networks.

by Nicolas Mokhoff,
Senior Editor



Now that local area networks are abundant, designers are focusing their attention on how to interconnect different types of LANs with wide area networks. Whereas LANs are usually specified in terms of the two lowest layers of the Open Systems Interconnection model, the interconnection between LANs and larger networks deals with upper layers three to seven of the OSI model. The design emphasis is changing from pure hardware to hybrid software/hardware for the lower layers, and is migrating to pure software for the higher levels in the OSI model.

This change has become especially evident with the proliferation of personal computers (mainly from IBM). Designers are faced not only with the challenge of interconnecting them within the networks, but must also find ways to gain access to IBM's System Network Architecture. Thus, protocol conversions and gateways must be designed for both SNA networks and the non-IBM world that adheres to the OSI model. Over the past several years, protocol converters have basically met this challenge. They provide the best way to communicate between a non-IBM device and the IBM environment. (The protocol converter market for IBM interfaces—estimated to be around $120 million in 1984—is expected to grow at an annual rate of 50 percent.)

The main advantage of using protocol converters is cost reduction. For example, the cost of outfitting each peripheral with synchronous data link control capability and an expensive synchronous modem can be $1000 or more. Protocol converters, on the other hand, allow any device with an RS-232 interface to connect to the host. This makes dial-in ports, private branch exchanges, and remote dial-up terminals possible. These features are not usually available in the IBM environment.

While protocol converters offer cost advantages for individual devices, the more efficient way of interconnecting peripherals within a geographical area is via the LAN. LANs also offer perhaps the most promising method of interconnecting to IBM mainframes as well. Independent manufacturers are currently offering many LANs. These LANs present a

choice of the three most popular media access techniques: carrier sense multiple access/collision detection (CSMA/CD), token bus, and token ring. Most of these networks use a gateway to a mainframe through hardware and software that convert the LAN's protocol to any one of IBM's protocols. IBM has recently announced LAN offerings for its various families of computers.

The IBM PC network, for instance, resulted from the collaboration with Sytek, Inc of Mountain View, Calif. Sytek's LocalNet/PC, the backbone of IBM's PC Network, is basically a communication architecture supporting personal computers on broadband local networks. It is a peer network conforming to the OSI model, and its cabling system is based on broadband cable distribution systems.

The cabling system not only supports LocalNet/PC, but also LocalNet and other industry standard broadband networks. The cabling system is compatible with the in-development broadband network standards of the IEEE 802.7 broadband standards committee. This committee considers a large broadband cable system as a collection of small (hundreds of nodes) broadband, small area networks integrated via a common broadband trunking system.

LocalNet/PC provides communication functionality up to OSI's session layer. Since presentation and application functions are not included within the architecture because of their user specific characteristics, they are combined in a "user application" layer. These user applications, such as file access, would be typically implemented as software executing on the main processor of a personal computer or server. This software would send network commands to the LocalNet/PC protocol interpreters in a manner similar to a procedure call. Thus, software modules are shown performing procedure calls on lower level software modules.

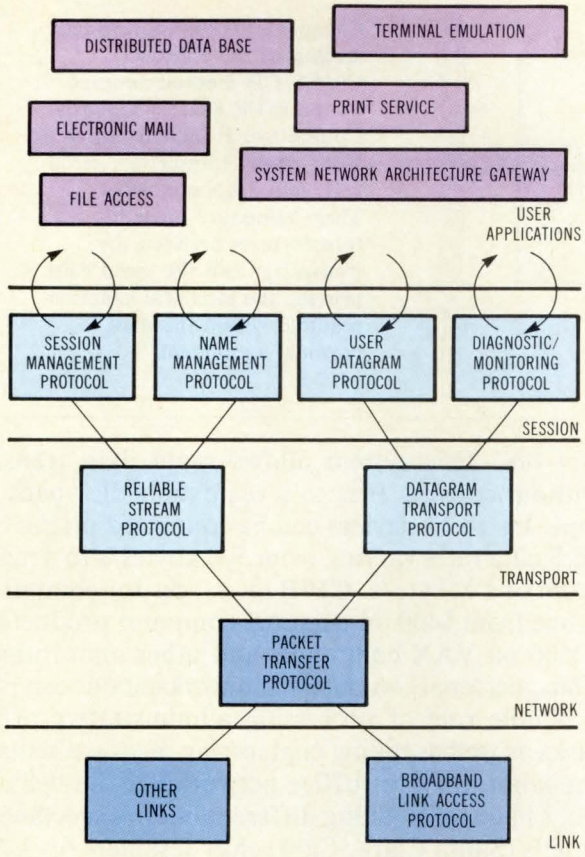
A protocol for every level

Residing on a physical medium such as a broadband cable, the network can handle 2-Mbit/s broadband channels using a frequency modulated carrier. At the link level, the link access protocol provides

Local Area Networks Offered by IBM

System	Token Ring	PC Network	Industrial	3270 PC System	Cluster Kit
Technology	Token-passing ring as subset of SNA	CSMA/CD bus	Token-passing bus	327X Communications	CSMA/CD bus
Availability	1986-1987	1985	1985	1985	1984
Channel rate	4 to 16 Mbits/s	2 Mbits/s	1,5, or 10 Mbits/s	Low speed	256 Kbits/s
Media	Twisted-pair, Optical pair, Baseband coaxial, Broadband coaxial	Broadband coaxial	Broadband coaxial	IBM 3270 point to point coaxial	Baseband coaxial
Products supported	IBM systems	IBM PC, XT, AT, Portable	5531, Series 1 PC line	327X controllers 3270 PCs	PC,XT, PCjr
Number of devices on LAN	256	72 to 1000	N/A	32	64
Intended users	Large corporations	Small businesses	Factories	327X community	Small businesses, schools
Responsible IBM division	Communication products	Entry systems	Industrial	Communication products	Entry systems
Other companies collaborating	Rolm Corp	Sytek, Inc	General Motors, Concord Data Systems, Hewlett-Packard, Prime, Allen-Bradley, Gould, and others	—	—

Note—Intel Corp provides interface circuits for most LANs.



The protocol layers for Sytek's LocalNet/PC cover all the upper layers of the Open Systems Interconnection (OSI) model. The session layer protocols make their services available to the user for such applications as file access. The structure can be interpreted as software modules performing procedure calls on lower level software modules. The usual presentation and application layers of the OSI model are combined in this network into the user application layer.

basic CSMA/CD channel arbitration functions as well as addressing and error detection. The packet transfer protocol routes packets at the network level between separate link-level channels. The two protocols in the transport layer provide two distinct services. The reliable stream protocol furnishes a virtual connection service with full-duplex, flow-controlled data streams while the datagram transport protocol supplies end-to-end exchanges of simple best-effort datagrams.

In the session layer, the session management protocol builds stream-oriented sessions on top of the reliable stream protocol's virtual connections. This allows session participants to acquire an identification by using symbolic names. Users have a complementary protocol—the name management protocol—to register symbolic names with the network. The user datagram protocol allows datagrams to be sent using location independent symbolic names rather than network addresses. The diagnostic and monitoring protocol provides users with node status and network statistics information. By implementing these protocols, users obtain an open broadband architecture that can accommodate up to 1000 different type nodes per channel at distances of 10 km or more.

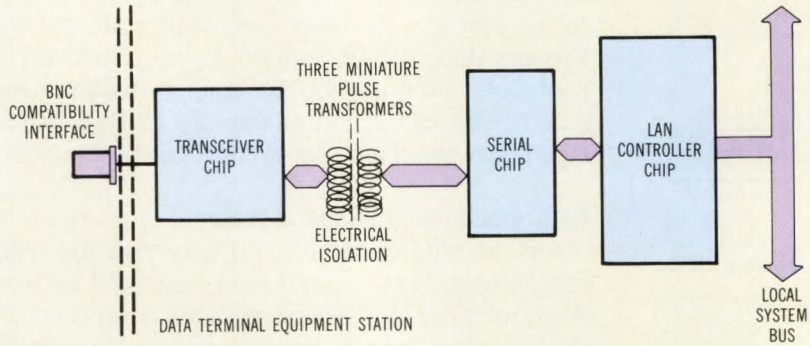
New standard provides a choice

On the whole, broadband networks are usually more expensive to install than baseband networks. And, with the increase of personal computers, even the Ethernets are not the most efficient propositions for small businesses. Therefore, the IEEE 802 LAN Standards Committee has made a move to create a marketplace for a new standard. This standard would be a simple, low cost, and user manageable open system network called Cheapernet. The technology adopted for the IEEE 802.3 standard CSMA/CD LAN has been optimized for wide area coverage and relatively high performance. Cheapernet, on the other hand, has been created simply by performing a series of adjustments that effectively trade off geography for economy.

The major differences between the two networks include a single segment of Cheapernet, which is limited to 600 ft, as opposed to 1600 ft of cable for the standard CSMA/CD LAN. Also, only 30 nodes per segment of Cheapernet cable are permitted, whereas 100 nodes per segment are allowed for the standard version. The biggest departure from the standard CSMA/CD LAN is the physical integration of the transceiver function into the Cheapernet data terminal equipment (DTE). (This change in construction results in significant cost savings.) Cheapernet DTEs are then linked to the thin-segment cable in a daisy chain fashion via a coaxial cable.

In addition to full-fledged LANs, a number of companies have begun to offer partial LANs—networks that are specific to a class of peripherals. There are applications where a full LAN cannot be justified even when price and the standardization effort settle down. Basically, for slow transmission such as 300 baud to 19.2 kbaud, LANs can be overkill. In such application areas as the factory, many types of peripherals and controllers are used which cannot be supported by today's LANs. Thus one company has developed a peripheral network concept to satisfy the slow transmission rates associated with RS-232 or Centronics parallel interfaces. Compared to some of the most popular LANs on the market today, Advanced Systems Concepts, Inc's (Pasadena, Calif) peripheral network costs significantly less on a price per node basis.

Even more specific to the engineering environment is a file transfer software package for high speed data



Cheapernet is an abbreviated version of the Ethernet CSMA/CD method adopted by the IEEE 802.3 Standards Committee. It includes three VLSI chips: transceiver, serial I/O, and LAN controller. Three miniature pulse transformers between the transceiver and the serial chip provide the electrical isolation required within the data terminal equipment.

transfer between computers sharing the IEEE 488 bus. Also known as the general-purpose interface bus (GPIB), the IEEE 488 has become the accepted high speed parallel communication technique between computers and programmable instruments and peripherals. Its use is growing at 30 to 50 percent/year. (Over 40,000 new systems were installed in 1984.)

National Instruments of Austin, Tex has developed a file transfer package for a network called the Net-488. This system allows rapid data transfer without copying files to a removable disk pack or tape. Up to 15 devices can be connected on the bus with data rates varying from 500 kbytes/s to a maximum of 1 Mbyte/s. GPIB interfaces for computers range from $400 on personal computer products to $2500 on VAX computers and other mainframes. Thus, personal computers and workstations can play a double role of processing administrative office tasks as well as taking engineering measurements in the laboratory. In office networking, the delineations have fallen along different lines. According to Intel's (Santa Clara, Calif) chip designers for LAN applications, office networking is evolving into a three-tiered structure. Each tier cost/performance ratio is optimized to a particular application.

Standard Ethernet Parameters versus Cheapernet

Parameter	Standard CSMA/CD LAN	Cheapernet
Data rate	10 Mbits/s	10 Mbits/s
Segment length	1600 ft	600 ft
Network span	8000 ft	3000 ft
Nodes per segment	100	30
Nodes per network	1024	1024
Node spacing	At 2.5-m intervals (on cable marker bands)	0.5-m minimum separation
Segment cabling system	0.4-in. diameter 50-Ω coaxial N-Series connectors	0.25-in. diameter 50-Ω coaxial with BNC connectors
Transceiver interface	0.38-in. diameter multiway cable with 15-pin D-Series connectors (length up to 165 ft)	Not applicable
Installation	Electricians required	Simple—mainly by user

Tier 1, a high speed link, is used primarily between mainframes but can also interconnect different LANs. Here, the rate is in the 20- to 100-Mbit/s range and is mostly fiber optic-based. Tier 2 covers the 2- to 10-Mbit/s data rate range. This tier can serve several applications. One, a LAN backbone, interconnects the clusters of personal computers and terminals of tier 3. Another provides access to data bases and expensive peripherals so that they can be shared. And, the third supports high end workstations.

With a data range of 1 to 2 Mbits/s, tier 3 has the largest volume and the most cost sensitive network. The IBM PC Network is a prime example. The Intel 82586 LAN coprocessor acts as the VLSI controller for the data link layer of this PC Network. Handling up to 762 nodes, the IBM PC Network can cover a radius of up to 1000 ft.

Chips for LANs

The 82586 has an onchip processor that works in parallel with the system CPU, and handles the data communication processing. The system side of the 82586 supports high level command functions from the host CPU, such as the transmit command. This allows the CPU to deal with the 82586 on a

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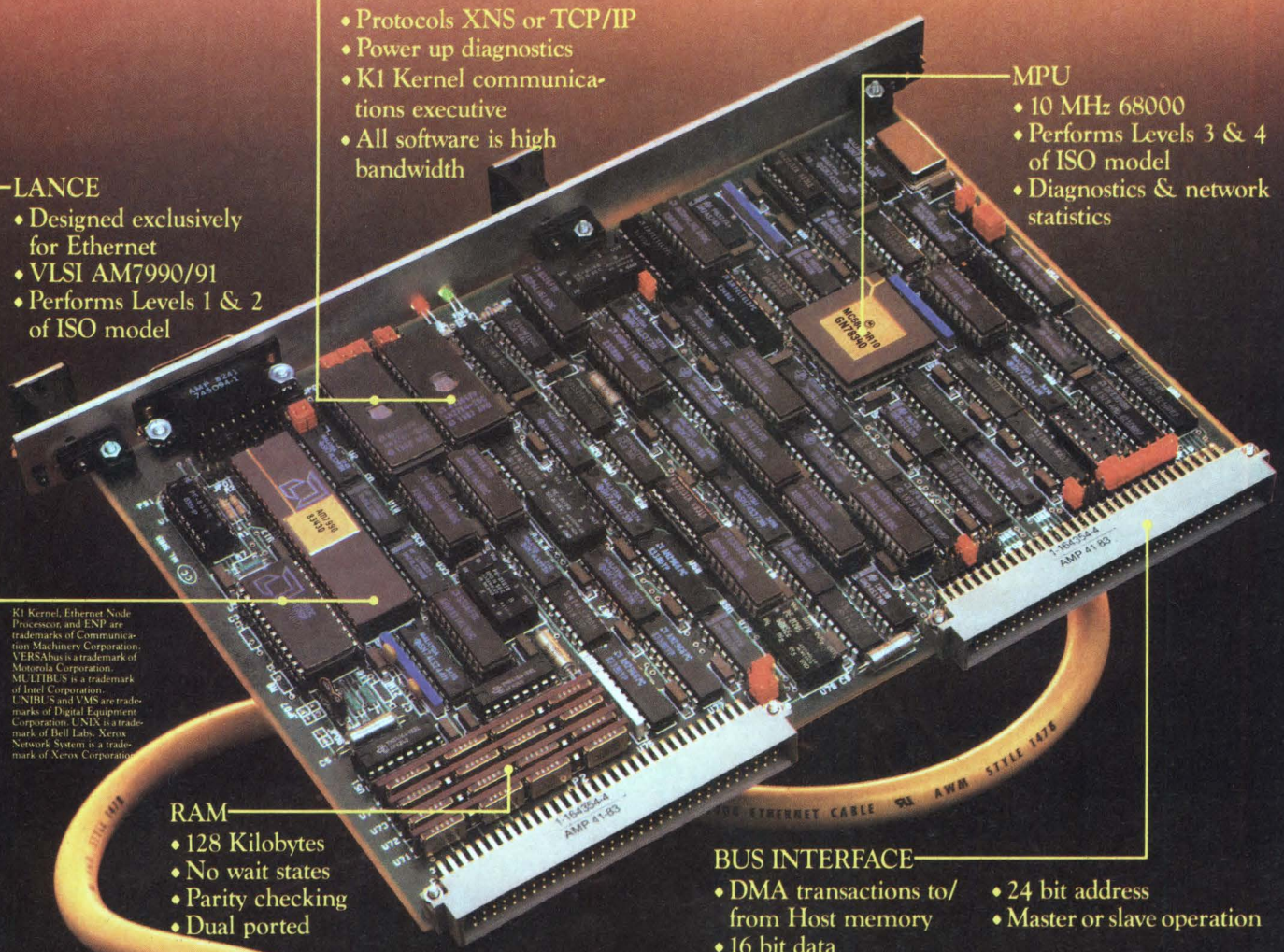

RAM
- 128 Kilobytes
- No wait states
- Parity checking
- Dual ported

BUS INTERFACE
- DMA transactions to/from Host memory
- 16 bit data
- 24 bit address
- Master or slave operation

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CIRCLE 51

Cost Per Node Comparison for Various LANs

Company	Network	Topology	Price Per Node Connection
Advanced Systems Concepts, Inc	Peripheral	Star	$110
ALSPA Computer	Zero-net	Bus	$1195/ workstation
Altos Computer Systems	Ethernet Altos-net	Bus Bus	$2500/ interface card $295/ interface card
Datapoint Corp	ARCNET	Star clusters (logical ring)	$500/ workstation
Nestar Systems	Plan 4000	Star clusters (logical ring)	$595/ interface card
Proteon Associates	Pronet	Ring	$2500
3Com Corp	EtherSeries products for Ethernet	Bus	$950/ interface card
Vector Graphic	LINC	Ring	$3750/ workstation

packet basis rather than on a byte basis, as with other controllers.

Besides Intel, National Semiconductor of Santa Clara, Calif, Advanced Micro Devices in Sunnyvale, Calif, and Texas Instruments of Dallas, Tex are also developing LAN chips. One of the more ambitious projects is the five-chip set expected from TI by the middle of the year. Its token-ring LAN adapter is just one of many joint efforts with IBM. The adapter is in a VLSI chip set and mounted on a printed circuit card within the attaching product. The chip set consists of a 16-bit communication processor with an onboard 2.75-Kbyte RAM, an IEEE 802.5 protocol handler with 16-Kbyte ROM, a system interface chip compatible with both the 8086 and the 68000 microprocessors, and a two-chip media interface set.

The TI adapter will be compatible with both the IEEE 802.5 cabling specifications of a balanced, shielded twisted-pair attachment to a trunk cable and to the IBM cabling system. When used with the IBM cabling system, the ring interface circuits will meet the less than 1-bit/billion-bit transmitted error rate specified by IEEE 802.5. The adapter will be capable of transfer rates of 40 Mbits/s, 5 Mbytes/s. The adapter's integrated buffer memory will free the attaching product's processor from the processing LAN frames not explicitly required by applications in the attaching product. Most other LAN adapters also feature buffer memory onboard.

Because the ring adapter has such dense circuitry and needs to be 100 percent reliable with error-free operation, TI established a design methodology called RAS—reliability, availability, and serviceability. This program was conceived to ensure that the token-ring LAN adapter has a highly reliable, easily maintainable, and "zero escape" error environment. A zero escape environment is possible with built-in features such as error detection, fault isolation, parity on all address and data paths, and power-on, self-test diagnostics. These features ensure proper functioning of the adapter before inserting it into the network. They also guarantee that the adapter maintains the data integrity as data is passed through the network.

Working with IBM on the token-ring adapter led TI to adopt a strict design methodology program. The goal of the program is to prove that the VLSI design is based on specifications defining the functional requirements of a token-ring adapter. The program known as ratification, verification, and validation is used to show that the VLSI chip under design fulfills the end user's requirements.

The functional specification, based on the system requirements of a token-ring network, includes such items as the media access control, physical transmission layer, system interface software and hardware description, software control interface, environmental considerations, power requirements, and rror procedures. Verification is applied by placing multiple identical hardware emulators in a ring test environment. This is done to prove that the actual implementation specification, including the microcontroller instruction set, fulfills the functional specification requirements.

In the ratification phase, the specifications are confirmed within the many error conditions possible. All error conditions are handled properly without lock-up of the ring. In validation procedures, the hardware emulators are connected to an IC tester to verify test patterns against those from a software model output. This ensures that the hardware emulators and software models are identical to the VLSI module boundaries.

While IBM has recently made significant progress in the LAN market, the company has a substantial investment in all kinds of data communication equipment that may not easily fit into the LAN environment. Such is the case with synchronous terminals

that were basically designed for the company's internal System Network Architecture. Last year the company celebrated the tenth anniversary of the SNA, claimed to be "the most successful computer architecture in the information processing industry today." Currently, IBM's customers around the world are using SNA in more than 20,000 host computers.

Latching on to the SNA giant

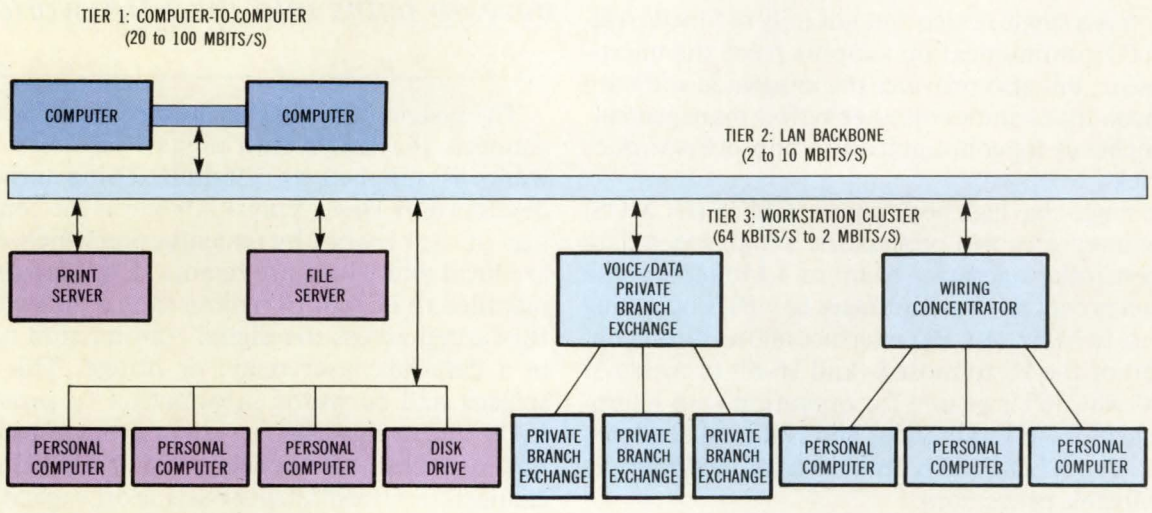
SNA resembles the seven-layer structure of the OSI model. But IBM divides SNA into three distinct entities: a specification, a plan for structuring a network, and a set of products. SNA specifies the operating relationship of IBM products as part of a system. It also provides a coherent structure to manage networks, and in response to new requirements, to change and expand them.

IBM's set of products includes a large number of computer terminals for both specific industries and general applications. The predominance of IBM products has forced the rest of the industry to develop paths into the SNA world. On the other hand, market pressure by its competitors has caused IBM to react by opening up the SNA environment to non-SNA equipment. As such, IBM has announced the 3710 network controller, which enables a variety of SNA and non-SNA devices to communicate with any host computer on the network. In addition, the company has made available enhanced software products that extend the number of logical addresses from 84,000 to 8 million for workstations and other devices in a single SNA network.

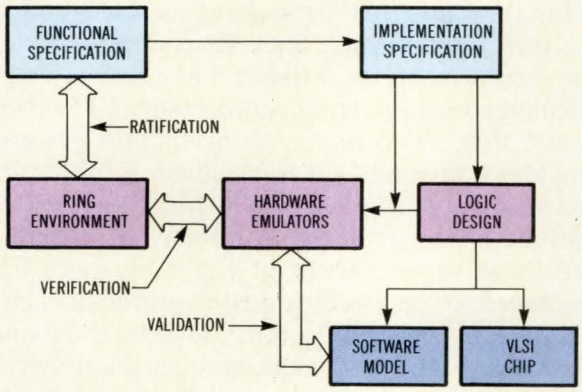
Still, there are companies that want to hook up to Big Blue, and they are making interface products for such applications. Exel Microelectronics, Inc (San Jose, Calif), for instance, has developed a bit-oriented communication coprocessor (XL88C565/XL68C565). The company claims that the processor provides a much higher level silicon solution than previously available chips by off-loading the CPU realtime I/O interfacing. A number of integrated circuits at varying levels of capability have been developed to support bit-oriented protocols such as synchronous data link control, high level data link control, and advanced data communications control procedures. Although they are effective communication interfaces, these devices leave a substantial portion of the realtime communication control and buffer management up to the system processor. This affects CPU throughput for other tasks adversely.

Some devices, such as Zilog's Z8030 serial communication controller and Signetics' (Sunnyvale, Calif) SCN68562 dual universal serial communication controller, handle multiple protocols of the character-, byte-, or bit-oriented types. They are principally designed to operate as a slave to a microprocessor.

When used with a microprocessor, these communication controllers are first initialized for the correct frame format. Then, by polling, or via interrupt, the microprocessor must read received data, or write data for transmission directly to or from the controller on a character by character basis if the device incorporates a first in, first out register. This type



To provide a wide variety of solutions for the various network configurations, the goals for which LAN chips should be designed are categorized into three tiers. The tiers are assigned according to the data transfer speeds that each has to provide for the end user. Chips are starting to appear for the workstation cluster tier and the LAN backbone tier. For the fiber optic-based tier that links large computers, optical transceiver chips and high speed ECL chips are on their way.



Token-ring access technology requires 100 percent reliability. As part of Texas Instruments' reliability program, the company follows a strict design methodology for its token-ring VLSI chips that are slated for IBM's token-ring LAN. TI's ratification, verification, and validation procedures ensure that the VLSI chip under design can meet IBM's, or any other customer's, specifications for a token-ring LAN.

of operation can severely limit available microprocessor time for other tasks. In LAN applications where the data speeds are high, communication support may not even be possible, or at best, a dedicated CPU may be required to handle the communication tasks.

If a DMA controller is added to the chip as in the AMD 9517A, the processor overhead is substantially reduced. However, much CPU support is still needed for buffer management of linked lists because these lists not only rob the processor throughput, but also add to the software complexity. Thus, the better solution is a single device that not only off-loads real-time I/O communication support from the microprocessor, but also provides the integrated software on silicon that handles message buffer management. Exel believes its communication coprocessor does the trick.

The single-chip high performance CMOS (HCMOS) device integrates two processors: a high speed data link controller operating at up to 4 Mbits/s, and a channel processor that interfaces to CPUs operating at up to 10 MHz. A CPU interface allows direct connection of the IC to most 8- and 16-bit processors. The XL88C565 is geared for operation with microprocessors from Intel, Zilog, and National Semiconducter. The XL68C565 is optimized for the Motorola and Mostek processors.

The giant link between DNA and SNA

A monumental attempt was made in 1984 to connect to IBM's SNA world when Digital Equipment Corp (Maynard, Mass) introduced its DECNet/SNA gateway. The gateway serves as a transparent and bidirectional communication link between the DEC and IBM data networks. The company's Digital Network Architecture (DNA) is proprietary like the SNA, but also follows the general outline of the OSI model. DNA defines the standard protocols, interfaces, and functions that enable DECnet nodes to share data and resources. Its hierarchical framework provides flexibility for adding communication technologies such as Ethernet without affecting user applications. Ethernet protocols are added to the two lowest layers of DNA and the structure of all other layers remain unchanged.

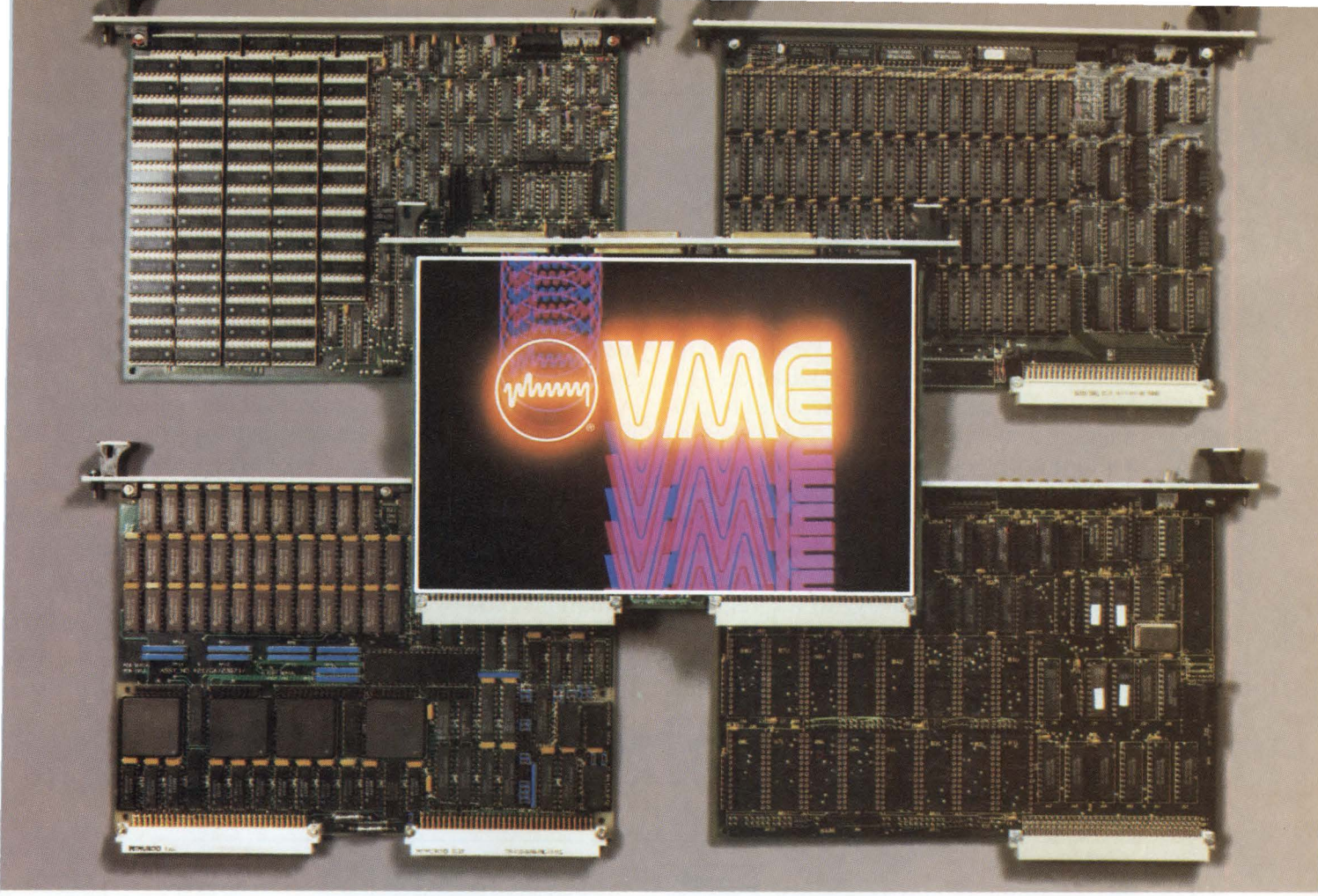
DEC's latest software links for connecting to the SNA environment include DDXF, a document exchange facility; DHCF, a distributed host command facility; PrE, a printer emulator; and MicroVMS operating system versions of the 3270 terminal emulator and gateway management. These products provide users with the decentralized resources of IBM SNA networks while delivering the power of the VAX environment.

DEC also became involved in another attempt to link LANs last year. Together with Mountain View, Calif-based Vitalink, DEC is marketing TransLAN, a combined hardware and software product that transparently connects LANs via satellites and/or terrestrial lines. Ethernet 802.3 LANs connected via TransLAN appear to any LAN station as a single LAN.

The predominance of IBM products has forced the rest of the industry to develop paths into the SNA world.

The system of bridge hardware and software that connects the LANs with digital transmission networks is supplied by Vitalink. Using technology developed by DEC, TransLAN learns the configuration of the network by remembering which stations are local and which are remote. LAN information intended to be sent to remote sites is automatically forwarded across the digital transmission network in a data-link-layer relay, or bridge. This bridge screens and forwards information to protect the LAN and transmission system from unnecessary traffic. TransLAN has eight V.35 or RS-232 satellite channels or terrestrial link ports. Port capacity is 224 kbits/s. The frame processing rates are 4000-frame/s filtering and 1500-frame/s forwarding.

Developmental work is also progressing on complete fiber optic LANs. AT&T Information Systems has already based its Information Systems Network on fiber optic cable which, the company feels, is



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2 Mbyte DRAM	PME 048D	•		8/16	190	300
1 Mbyte DRAM*	PME 512EP	•		8/16/32	150	270
3/4 Mbyte DRAM	PME 256EA		•	8/16/32	150	300
512 Kbyte DRAM	PME 012D	•		8/16	190	300
512 Kbyte EPROM or ROM; 128 Kbytes SRAM	PME CRR-1†			8/16	User Adjustable	
128 Kbytes SRAM	PME 128S†			8/16	140	140

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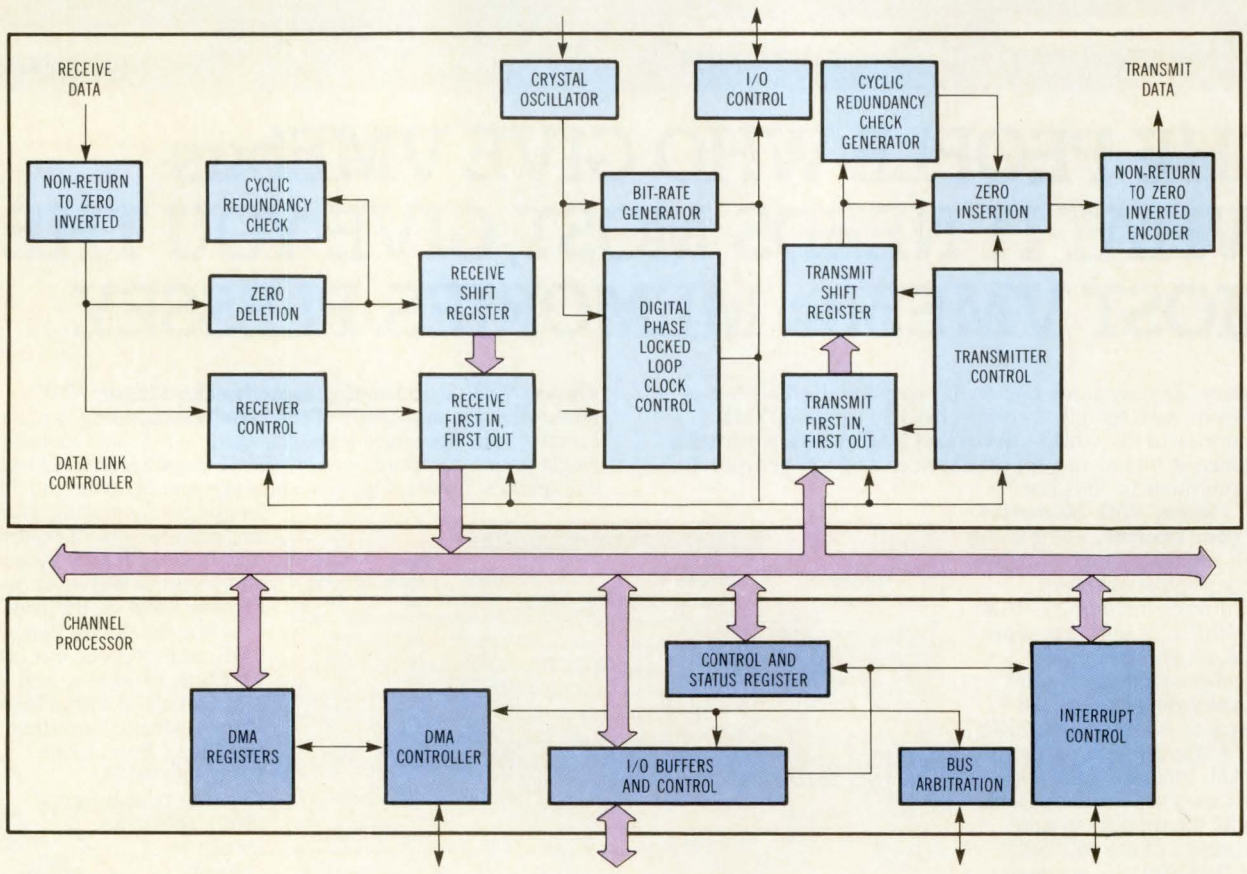
clearly the medium for efficient, secure, and high capacity distribution of multimode information (voice, data, and video). ISN is a high performance packet controller network for high speed (8.64 Mbits/s) data handling and switching. The network architecture can allocate bandwidth on demand to individual users with the Datakit virtual circuit switch (VCS) protocol. The switch is based on a kit of compatible modules that can be assembled to provide a range of network functions. According to AT&T, a major problem in some LANs is that protocol and switching schemes do not allow communication between nodes without gateways. The Datakit VCS solves this problem with its unique interconnection scheme. Whole series of nodes can be connected while keeping transmission delays to a minimum.

Functionally, the Datakit VCS is a digital virtual circuit switch that uses an internal high speed packet switch. Combining the high speed internal 8-Mbit/s backplane bus with relatively small packets (16 bytes long) provides little delay and high throughput even across a wide area network made up of several such switches.

Forming backend networks that can adapt mainframes, file servers, and full-fledged LANs, becomes essential as more LANs are connected and more throughput is required. Such a network would implement a Fiber Distributed Data Interface (FDDI) currently being defined by the ANSI X3T9.5 Committee. A wideband 100-Mbit LAN such as FDDI can supplement frontend LANs of lower speeds by providing backend interconnections of dissimilar networks.

Fiber optic standards for LANs

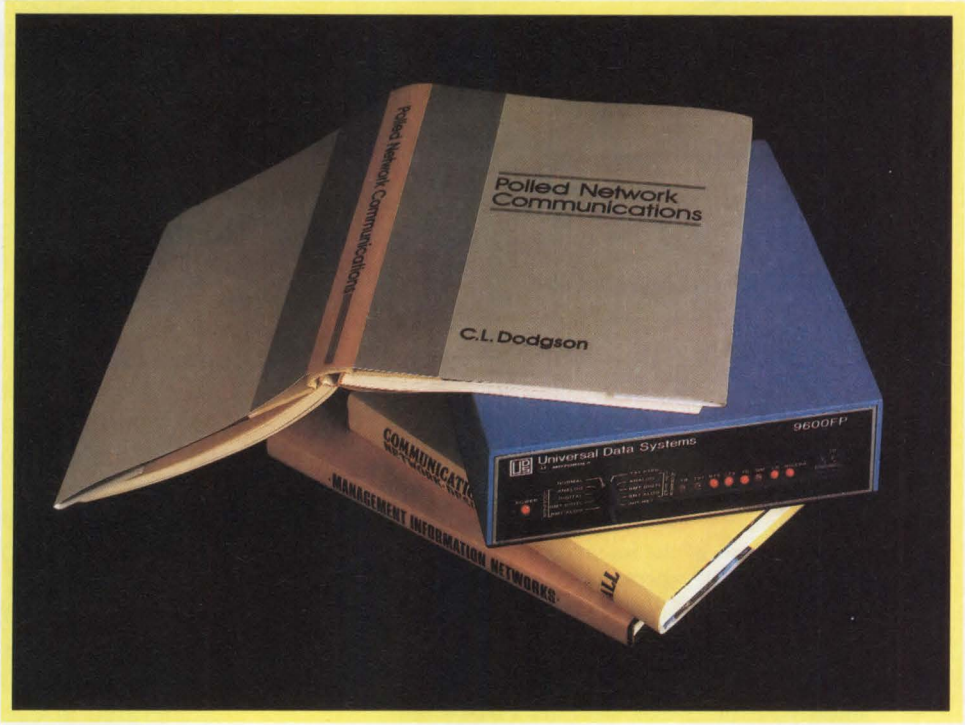
The FDDI is a ring topology LAN with a token-passing access scheme. It is specifically designed for communication over fiber optic cables at up to 100 Mbits/s for distances of 1 to 2 km. Data rates above 50 Mbits/s usually dictate a fiber optic communication medium since it has inherent advantages over coaxial cable. FDDI performance is depicted relative to other interfaces in logarithmic scale.



A typical communication coprocessor IC accommodates the basic functions for transmitting, receiving, and buffering the data between the LAN and a microprocessor. Exel's chip comes in two versions for the 8086 and the 68000 family of parts. It incorporates circuitry to support all bit-oriented protocols. The device integrates two processors: a data link controller operating at 4 Mbits/s and a channel processor that interfaces to the CPUs operating at 10 MHz.

Quick Study!

New UDS 9600 bps Fastpoll Cuts On-line Training Time 33%



The new 9600 bps fastpoll modem from Universal Data Systems means extra throughput for your polled multipoint network! Until now the fastest on-line training time available anywhere has been 12 milliseconds. Since training time is non-productive time, UDS has increased system throughput by trimming the training cycle to 8 ms, producing a corresponding increase in overall system efficiency.

The device is suitable for operation over unconditioned four-wire leased lines in either fastpoll or conventional CCITT V.29 mode. Integral test features allow for system performance evaluation and fault isolation within the communications link.

The UDS design incorporates LSI and microprocessor technologies to achieve significant size and power consumption advantages. For detailed specifications, contact Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Phone 205/837-8100; Telex: 752602 UDS HTV.

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CIRCLE 53

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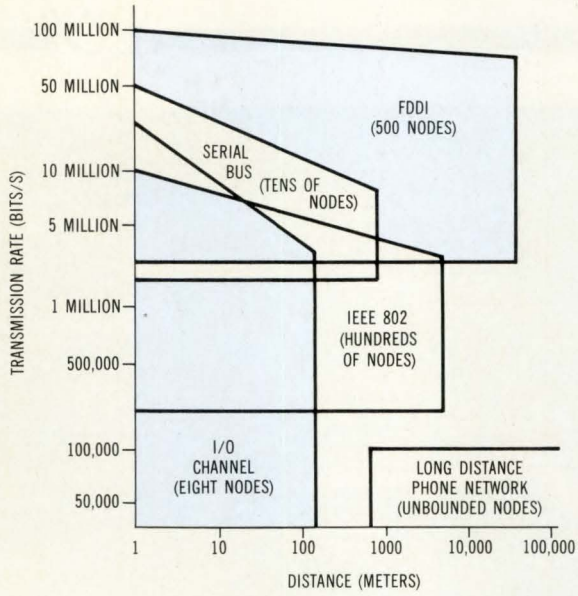


A comparison of the intended Fiber Distributed Data Interface (FDDI) spectrum of parameters—transmission rates, the number of nodes, and the extent of its reach—against those of other types of communication schemes shows the tremendous advantage offered by FDDI. Plotting this data linearly for the Y-axis identifies FDDI's full potential. Also, because fiber is in its youth and the other schemes are mature technologies, even more significant data improvements can be expected.

The advance offered by FDDI can be seen if the plot is drawn on a linear scale. Close to 500 nodes are permitted on the network and, despite the high transfer rate, more than 80 percent of the peak transfer rate can be sustained even at the maximum extent. Also, since FDDI, as specified, is actually two counter-rotating rings, the basic available data rate can be doubled. In addition, fiber technology is still advancing and promises significant data rate improvements whereas the other plots represent the performances of mature technologies. Properly configured then, FDDI will support sustained transfer rates as high as 80 Mbits/s, between 1000 nodes, over a 200-km data path. Currently, the ANSI Committee is defining a standard for the physical layer (1) and the media access control layer (2), conforming to layers 1 and 2 of the OSI model.

Design trade-offs

A possible node configuration for this type of network would entail a 32-bit microprocessor, RAM, FDDI, controller, and host interface. Without VLSI components, the FDDI node processor would be prohibitively expensive. Thus, one semiconductor manufacturer, AMD, has already announced a chip set that will conform to the FDDI specifications. Three VLSI devices that will attach a 32-bit microprocessor with closely coupled RAM to FDDI networks are planned for 1986. They include a link protocol processor, a media access controller, and an encoder/decoder.

Engineers working on these designs are faced with some difficult design options. Foremost, when going from the relatively slow 10-Mbit/s data rates of Ethernets to FDDIs 100-Mbit/s rate, a processing bottleneck appears. In effect, the network interface hardware has to convert 8-, 16-, and 32-bit wide parallel data into a serial bit stream while the data is transmitting. A network interface also has to provide buffering for this data. To accommodate all these requirements at high speeds requires the use of ECL logic at the medium's end.

Many of the design trade-offs can be better evaluated if a comparison is made between the FDDI specifications and the IEEE 802.5 token ring standards. Both the FDDI and the 802.5 standards specify token passing ring protocols. In such rings, stations are serially connected by the transmission medium to form a closed loop. Packets are transmitted sequentially from one station to the next downstream station. Packets are retimed and the signal levels are regenerated at each station before transmission to the next station. Idle stations can be bypassed or can act as active repeaters. The addressed station can copy the packet as it passes through the station. Finally, the station that transmits the packet strips it off the ring.

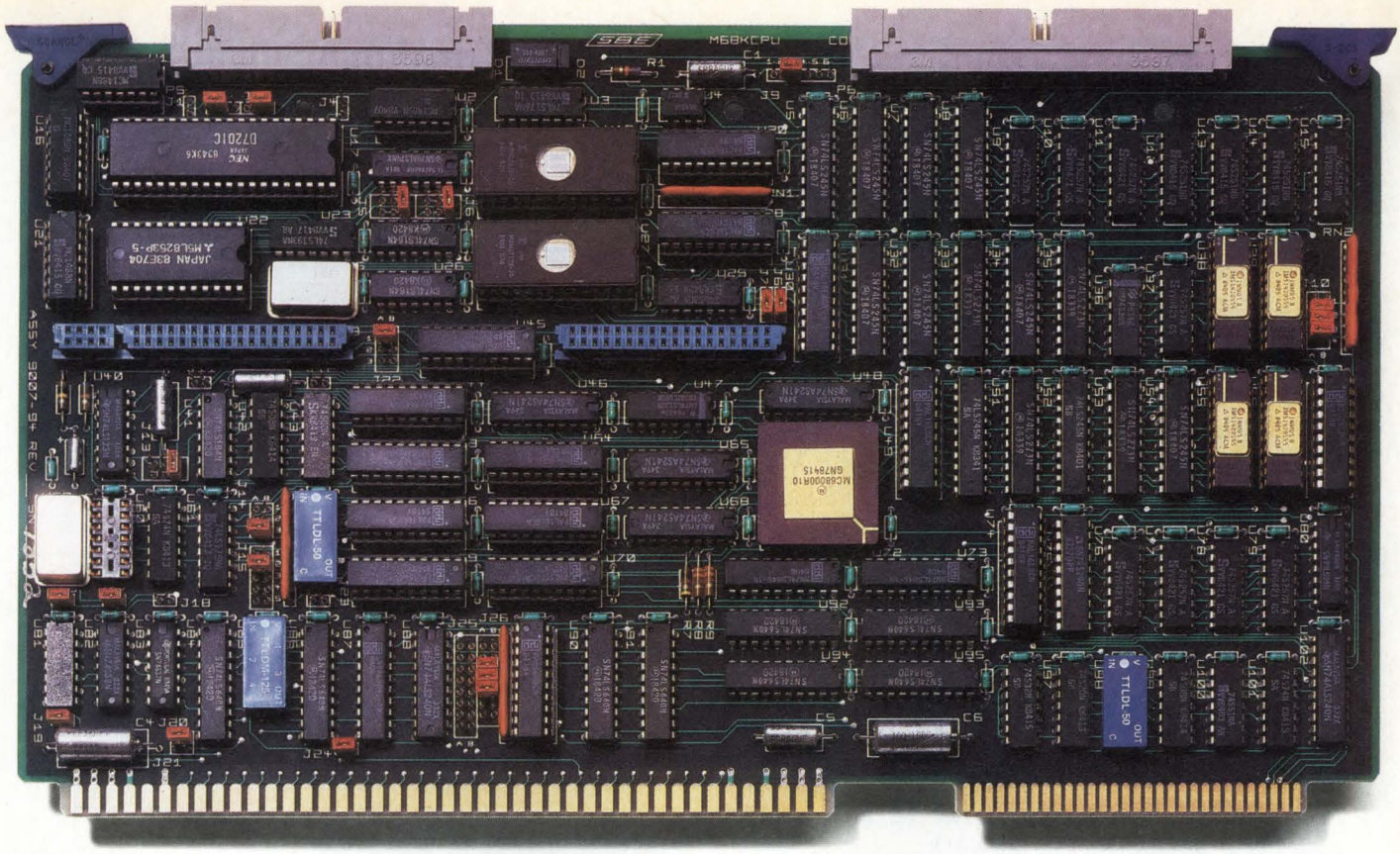
Transmitting tokens

In token-passing protocols, a station gains the right to transmit when it has the token, a special packet that circulates on the ring. When a station needs to transmit, it captures the token, transmits its packet(s), and releases a new token which the downstream node can use for its transmission.

FDDI has tried to retain the services and facilities of the 802.5 standard. But since FDDI is designed as a 100-Mbit/s standard and the maximum speed of the 802.5 is 4 Mbits/s, several key aspects have to be taken into consideration when streamlining the protocols for the higher data rates.

For more modest data rates, of course, a number of companies are offering either baseband or broadband cable solutions. One company, however, has developed the capability of serving its customers with LAN systems operating on four different media: baseband, broadband, optical fiber, and thin coaxial cable.

In 1984, Ungermann-Bass Inc of Santa Clara, Calif, introduced the industry's first commercially available fiber optic, Ethernet-compatible LAN,



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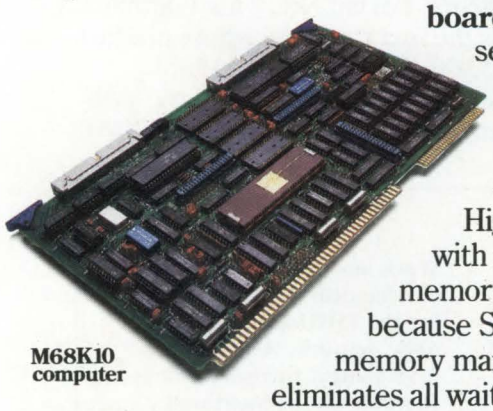

M68K10 computer

Our M68K10 runs at 10 MHz, accessing 128 KB to 1 MB RAM on the same board. This CPU is an amazingly powerful single-board computer for communications, process control, data analysis, ATE, and other systems applications. Contains up to 1 MB of dual-ported RAM accessible with no wait states. Has a 16-bit counter/timer and 24-bit parallel port right on board.

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Computer boards and systems.

CIRCLE 54

adding to an already impressive stable of LAN hardware and software offerings. According to PC Netline, a Hyatt Research Corp newsletter (Andover, Mass) that keeps track of the network industry, Ungermann-Bass has in the past five years become the largest third-party supplier of general-purpose LAN systems. A family of Network Interface Units (NIUs) form the core of the company's Net/One LAN architecture, which is based on the Ethernet specifications. The NIUs range from the single-port onboard personal NIU to the expandable 24-port NIU-2A. Communication between NIUs is handled by Net/One software which is not specific to any one vendor's system hardware.

Ungermann-Bass currently offers four versions of its Net/One system: a 10-Mbit/s Ethernet-compatible baseband system, a 10-Mbit/s thin coaxial baseband system, a 5-Mbit/s cable TV-compatible broadband version, and an Ethernet-compatible optical fiber system. Also its Personal Connection is an extension of Net/One for networking IBM personal computers which can be connected to any host or peripheral device on the network.

The company's latest offering, fiber optic Net/One, consists of fiber optic cables, optical star couplers, and Ethernet—compatible optical transceivers. Baseband models of Net/One use the optical transceivers to provide the transmission interface to the optical fiber cable. At the transceiver, the electrical signal is converted to an optical signal coupled to an optical fiber cable. The data travels to the star coupler, which outputs the signal onto all the fibers leaving the star coupler. The data is then received by all the other transceivers.

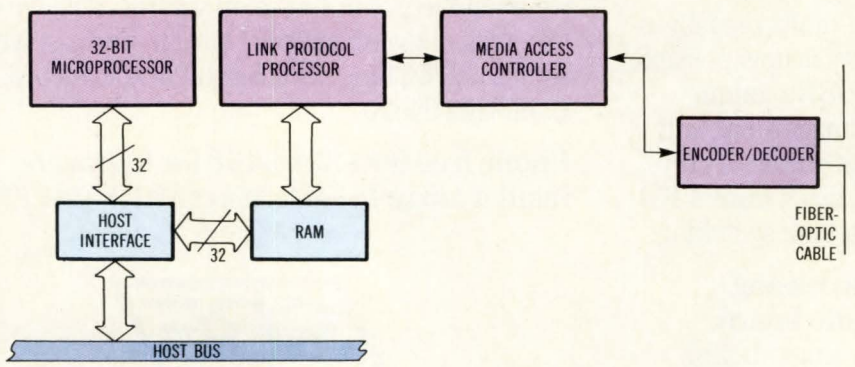
Using a 64 x 64 star coupler, a maximum of 64 optical transceivers per star segment can be implemented. The maximum length of the transceiver cable can be 50 m while the separation between stations cannot exceed 2800 m. Network repeater units can be used to extend the range of the transmission medium beyond a single segment. Repeaters regenerate the signal from segment to segment. As a result, multiple star couplers can be interconnected to a coaxial cable segment. Standard Ethernet transceiver cables are used to connect stations to the optical transceivers, whose access method and collision detection signals are identical to those of a coaxial Ethernet system. These products are also implemented with the same software.

While Ungermann-Bass has shown a strong position in the CSMA/CD media access world, its recent announcement of a new venture with General Electric may catapult the company into the deterministic end of the business. In September 1984, the two companies signed a letter of intent to form an independent joint venture company to develop, manufacture, and market LAN communication systems for the industrial market. This means that the resultant product must be based on a token-passing access method to ensure that, in a factory environment, each station can "talk" whenever it needs to, and not rely on the probabilistic CSMA/CD scheme.

Products answer to standards

The new company's principal goal is to provide products that will interconnect all industrial automation equipment, and other intelligent devices such as computer aided design/computer aided manufacturing systems, regardless of the system brand. The products will be sold on an OEM basis and will be compatible with the Ungermann-Bass LAN systems. They will also be made according to General Motors' manufacturing protocol specifications and the IEEE 802.4 standards. A working model of the manufacturing protocol network was demonstrated at the 1984 National Computer Conference. The underlying token-passing LAN for that demonstration was Concord Data Systems' Token/Net. This Waltham, Mass company was the first company whose product met the IEEE 802.4 token-passing standard.

In the Token/Net Interface system, the basic hardware is the Token/Net Interface Module (TIM),



Work has begun on the development of VLSI chips for the FDDI-based fiber optic network. AMD's development focuses on three ICs that can be interfaced with a 32-bit microprocessor and its associated RAM. A link protocol processor, a media access controller, and an encoder/decoder should be available in 1986.

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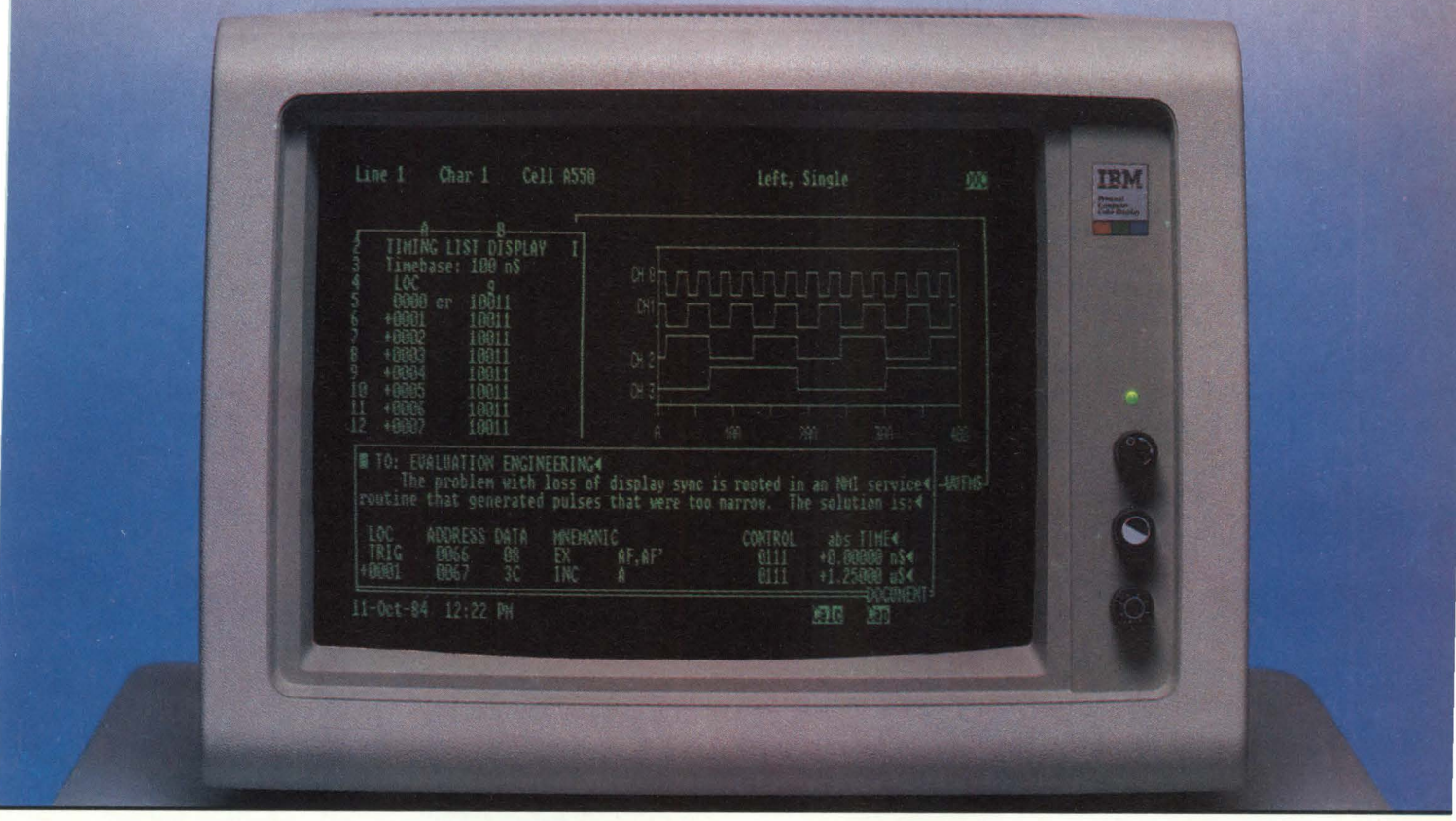

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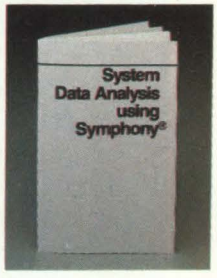

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Proposed FDDI and IEEE 802.5 Features		
Features	Fiber Distributed Data Interface	IEEE 802.5
Transmission scheme	Half-duplex; byte-level manipulation	Full-duplex; bit-level manipulation
Traffic control	Via timed token	Via priority and reservation bits in each packet
Encoding	Group with 10 percent dc component variation	Differential Manchester; no dc component
Architecture	Decentralized ring, individual clocks; limited packet size	Ring with one active monitor and one clock; very long packets

which connects to the broadband cable. This cable serves as a high speed (5-Mbit/s) broadcast medium to all other TIMs on the network. Within each TIM is a modem, a TIM access unit, a TIM control unit, and a power supply assembly. The access unit monitors receive signals from the modem and watches the medium for proper token operation. It checks to determine that all received messages pass a 32-bit frame check sequence and then passes good frames to the control unit via shared memory receiver queues.

In ongoing operations, the control unit provides the session establishment and packet addressing functions for its own serial interfaces and port option boards within the base unit. The control unit can connect to any ASCII terminal capable of 9.6-kbit/s start/stop operations.

Another Massachusetts company believed to be the first to fully comply with the IEEE 802.3 Ethernet CSMA/CD standard is Westford-based Interlan, Inc. Its NT100 transceiver is the latest addition to the company's NET/PLUS product line. Featuring a nonintrusive cable tap, the transceiver permits nodes to be attached or removed from an active network without disturbing network communications. An alternative tap is available for initial installation with preassembled coaxial wire. Interlan provides a plethora of Ethernet-based products to interconnect equipment ranging from personal computers to DEC hosts and Data General host computers including servers, transceivers, device driver software, cabling, and controllers. It also supports multiple operating systems including MS-DOS, VMS, RSX, Unix, and AOS.

Interlan was also one of the first companies to support Microsoft's announcement of Microsoft Networks, a file server for the MS-DOS environment. In relation to the OSI model, Microsoft Networks provides an application interface, presentation and session layers, and a well defined interface to the transport layer. Interlan's NET/PLUS begins with the IEEE 802.3 Ethernet specification for the physical and data link layers, implements the network and transport layers according to Xerox Network System's Internet Transport Protocols, and extends through the application layer in its server products. With Interlan offering Microsoft Networks at the upper layers, the personal computer user's capabilities can be extended beyond the personal computer-only environment into a wide range of host computers potentially spread across a number of internetworked LANs.

One company has shown exactly how internetworking can tie various LANs together. Novell Inc of Orem, Utah collaborated with 3M's Interactive Systems (St Paul, Minn) to demonstrate the capabilities of Novell's Advanced NetWare 1.0 at the 1984 Comdex show in Las Vegas. Interactive Systems' LAN/PC was used in conjunction with the Advanced NetWare 1.0 operating system to form a network of between 20 to 30 different LANs. The connection between separate LANs was accomplished via NetWare Bridges.

When it comes to personal computers, not all users will need the full Ethernet transfer rate of 10 Mbits/s.

Advanced NetWare 1.0 allows simultaneous use of files residing on different networks and will support workstation access to as many as eight file servers simultaneously. Thus, the NetWare operating system brings file server flexibility and true multiuser functionality to a number of popular LANs including Corvus Systems' Omninet, Gateway's 0-Net, Proteon's proNET, 3Com's EtherLink, Nestar's Plan 2000, Davong's MultiLink, SMC's ARC PC, Televideo's Personal Mini, and Novell's own S-Net Network.

Novell's NewWare Bridges essentially act as servers in their own right and communicate through a normal LAN link. The NetWare Bridge Box consists of three boards. One contains up to 2704 PROMs that hold the firmware while the other two contain the communication circuits for the bridge to link the LANs. The PROMs contain the routines necessary to translate packet data between LANs for ultimate use at the receiving station. Reception and transmission are completely transparent to the user and the file server access is identical to a multiple

server environment. Up to 84 personal computers can share up to 150 Mbytes of disk storage attached to the NetWare file server. The file server is a dedicated personal computer or file server/workstation that requires a minimum of 250 Kbytes of memory.

Using several operating systems in the same network is accomplished via a software shell. This shell translates the commands of each operating system into the native command structure of the file server. All workstations, regardless of their operating system, can view the same directories and share the same files.

Another company that is trying to make a dent in the LAN internetworking market is California Network Systems. The Milpitas-based company has its own NetServer communication system, a special-purpose communication processor designed to support multiple LAN interface cards in personal computers. The system supports up to 13 card slots compatible with the IBM personal computer, with one extra card designated as the bus master. This SysCard and the control ComCard have their own dedicated 80188 and onboard RAM. An optional OEM/SNA GateWay software package is available for the ComCard that converts the personal computer into a gateway to an SNA network. The result is that the network emulates an IBM 3274 cluster controller with the attached display stations and printers. The gateway software is written in C and supports up to 32 concurrent SNA sessions.

More moderate data rates for LANs

When it comes to personal computers, not all users will need the full Ethernet transfer rate of 10 Mbits/s. Thus, IBM's PC Network is specified for 2 Mbits/s while the upcoming StarLan from AT&T is scheduled to carry data at half that rate. Starlan's major advantage is that it is based on the already installed twisted-pair wires that can be found in most buildings where telephones are used. As a result, Starlan can be installed without rewiring—an advantage not found in Ethernet.

A total of 21 companies have formed a task force of the IEEE 802.3 CSMA/CD committee to investigate the possibilities of a standard for a 1-Mbit/s baseband CSMA/CD StarLan. A major stumbling block to making such a standard effective lies in deciding whether or not the twisted pairs are the proper medium for data transmission over meaningful distances and immune to electrical interference. AT&T, so far, has not committed the StarLan concept to the product stage, pending the verdict of the task force.

One semiconductor company that is a member of the task force, however, has committed itself to produce a controller chip for a 1-Mbit/s CSMA/CD baseband network. Intel's 82588 is a programmable LAN controller that can operate in both a 1-Mbit/s baseband network such as StarLan as well as in a 2-Mbit/s broadband system such as the PC Network, the IBM/Sytek collaboration. Some of the programmable parameters include framing for end-of-carrier or for synchronous data link control, address field length, station priority, interframe spacing, slot time, CRC-32 or CRC-16, and nonreturn to zero inverted or Manchester encoding/decoding.

Advantages in the VLSI chip

Embedded in the VLSI chip is a high level command interface, such as the CPU sending commands (eg, Configure or Transmit). This alleviates the task of the designer in developing low level software. This feature saves CPU memory by having the receive frames saved in buffers that are chained together in system memory, an important advantage for personal computers with limited memory. Similar features are included in the higher performance chip 82588 that is used in most Ethernet applications. But because of the lower bit rates, which require less sophisticated circuitry, a higher level of integration can be achieved. Thus, the CSMA/CD controller functions of the 82586, except for the coprocessor portion, are on this chip. Also included are the data encoder/decoder function of the 82501 Ethernet Serial Interface and the collision detection functions of a transceiver.

Networks using collision detection can attain theoretical throughput rates of 98 percent, compared to only 38 percent on networks with collision avoidance. For this reason, Intel has incorporated two kinds of collision detection on the 82588 to increase the total data throughput. The first collision detection method checks to determine whether or not incoming bits violate Manchester or nonreturn to zero inverted schemes. If these bits do violate these schemes, they are assumed to have been "damaged" by a collision. This method is useful in short bus LANs, such as AT&T's DataKit LAN, from which the StarLan is derived.

In the second collision detection method, the chip performs a bit comparison on its transmitted message as it returns on the receive channel. This method is used in networks with the separate transmit and receive channels usually found in broadband systems. Both methods permit detection of the collision while the message is still being transmitted; therefore, both methods have the advantage of immediate back off and retry.

As one addresses the layers above the physical and datalink, one leaves pure specifications and enters the software realm. Intel has joined the ranks of those who address the higher levels of the OSI

model. (It is not resting on its laurels by providing Ethernet-based chips that respond only to the two lower layers.) The company has made available its iNA 960, a software package that meets the ISO 8073 Class 4 Service requirements for the transport layer of the OSI model. This layer's task is to ensure that a message arrives at its destination. While CSMA/CD guarantees that only a single frame will be transmitted on the network at any one time, the transport layer breaks a message up into frames and sees that each message is properly received. The transport layer also sees that the message is correctly placed back together again at the receiving end.

A high level command interface saves CPU memory by reserving the receive frames in buffers that are chained together in system memory.

The iNA 960 comes in two configurations. The first one allows it to run as a task under Intel's iRMX 86 operating system at speeds of 150 kbytes/s. The second configuration has the iNA 960 run as a completely independent transport engine in which a speed of 300 kbytes/s can be achieved.

Toward umbrella protocols

Although designing neat packages for each of the OSI model layers may seem simple enough, the fact is that the model defines only the functions of each layer, but does not specify the interlayer communication standards. Thus, there are differences between various LAN vendors—even between Ethernet providers. The interlayer communication techniques often result in the inability of vendors to provide satisfactory multivendor networks.

Network Research Corp of Santa Monica, Calif has developed a C-based portable LAN program called Fusion. It implements the upper level protocols to accommodate a wide variety of normally incompatible computer processors, operating systems, LAN hardware, and network interfaces. Fusion provides full implementation of the XNS internet transport protocols, including the datagram, error, echo, routing, and packet exchange and sequenced package protocols. Fusion also implements the ARPANET TCP/IP protocols.

Another company that supports the XNS and TCP/IP protocols with its products is ACC of Santa Barbara, Calif. Its family of ACCES products consist of modular hardware and software packages designed for multivendor, multi-operating system environments. Its latest offering is the ACCES Network File Management System (FMS) that provides complete file management devices for VAX VMS and Unix operating systems. With FMS complete files, individual blocks and even individual records can be manipulated across a network regardless of the different operating systems' file management structures. Every complete file transferred is accompanied by a file header that provides critical information to the receiving host computer regarding the incoming file format. Thus, the network file header ensures that information is not lost as the file is moved, even though each host may maintain different file attributes.

In general, ACC is in the forefront of providing solutions for distributed processing systems. The company has set up a LAN center in Soquel, Calif whose sole purpose is to develop interconnectivity solutions for equipment from different vendors. 'Here, computers are ripped apart, inserted with Ethernets and intelligent communication controllers, plastered back together, and then made to talk with each other. The center becomes the proving ground for the next generation of higher level communication products under the ACCES umbrella. It uses the Xerox-developed courier Presentation/Session level protocol as the vehicle between its application-oriented packages such as the FMS and the bit-oriented TCP/IP and XNS protocols.

The company keeps close tabs on the standardization efforts for the higher level protocols of the OSI model. As such, the company's products follow on the heels of new developments in that arena. Thus, one can almost suspect that L. Brian McGann's predictions may one day come true. The manager of ACC's LAN center, referring to the capabilities of the center, says "Our current capabilities are really foreshadowing the next giant step in computing, that of tying computers into a network as functional blocks."

According to McGann, these blocks will then make many new services available to the end user. The final verdict on this will be delayed for a while. It remains to be seen whether the ACCs of this industry will be able to match the network solutions that companies like IBM offer for their products. In the final analysis, the network industry needs both types of companies to wire our global village called Earth.

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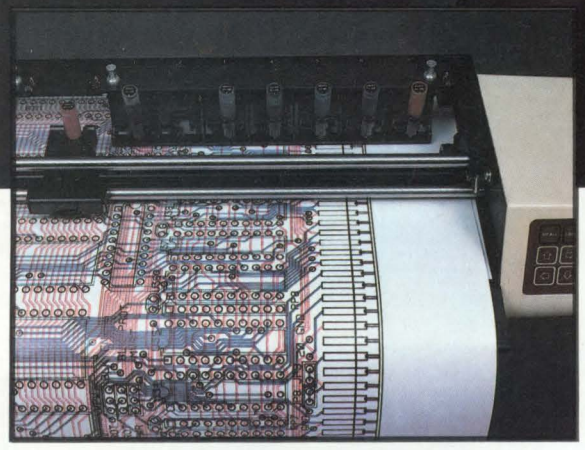

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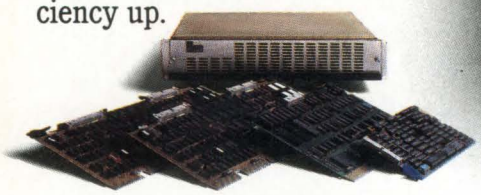

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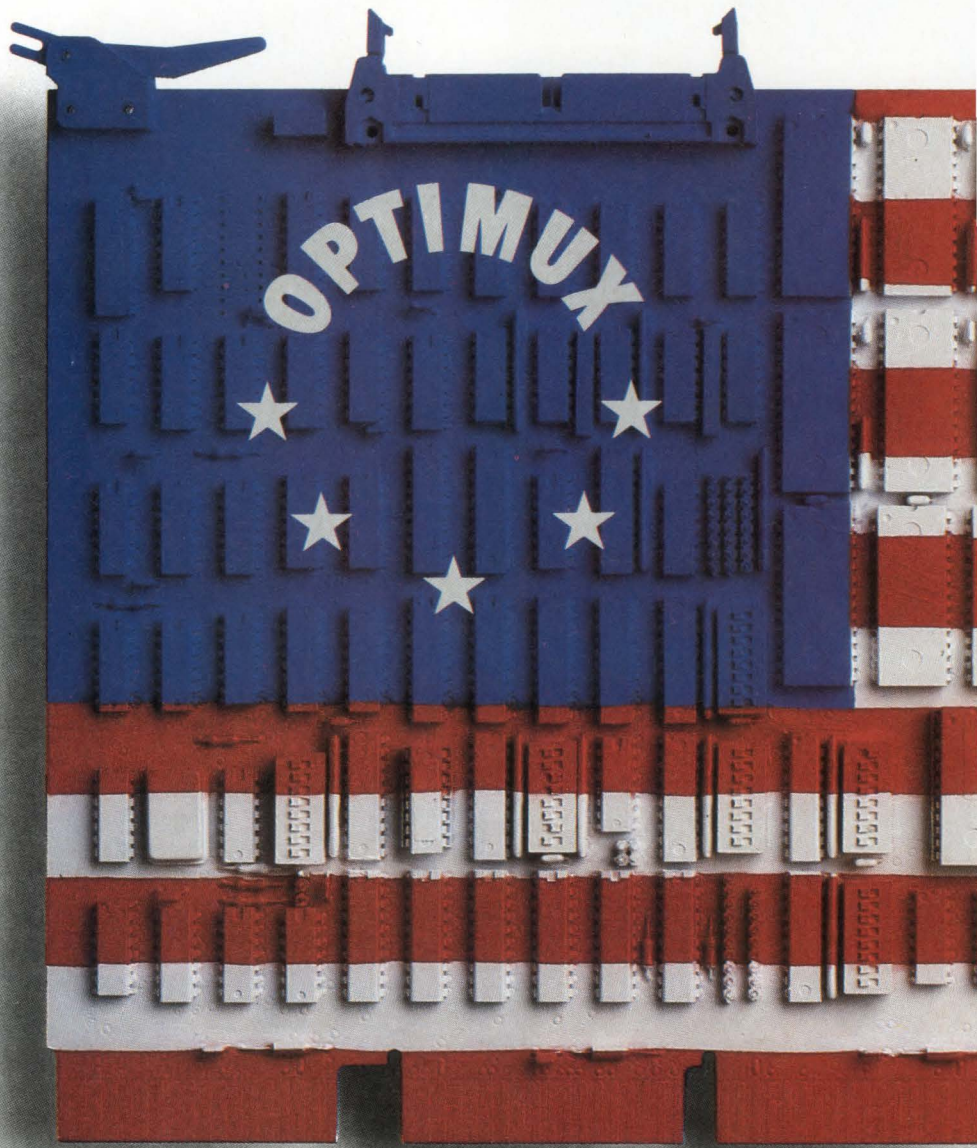

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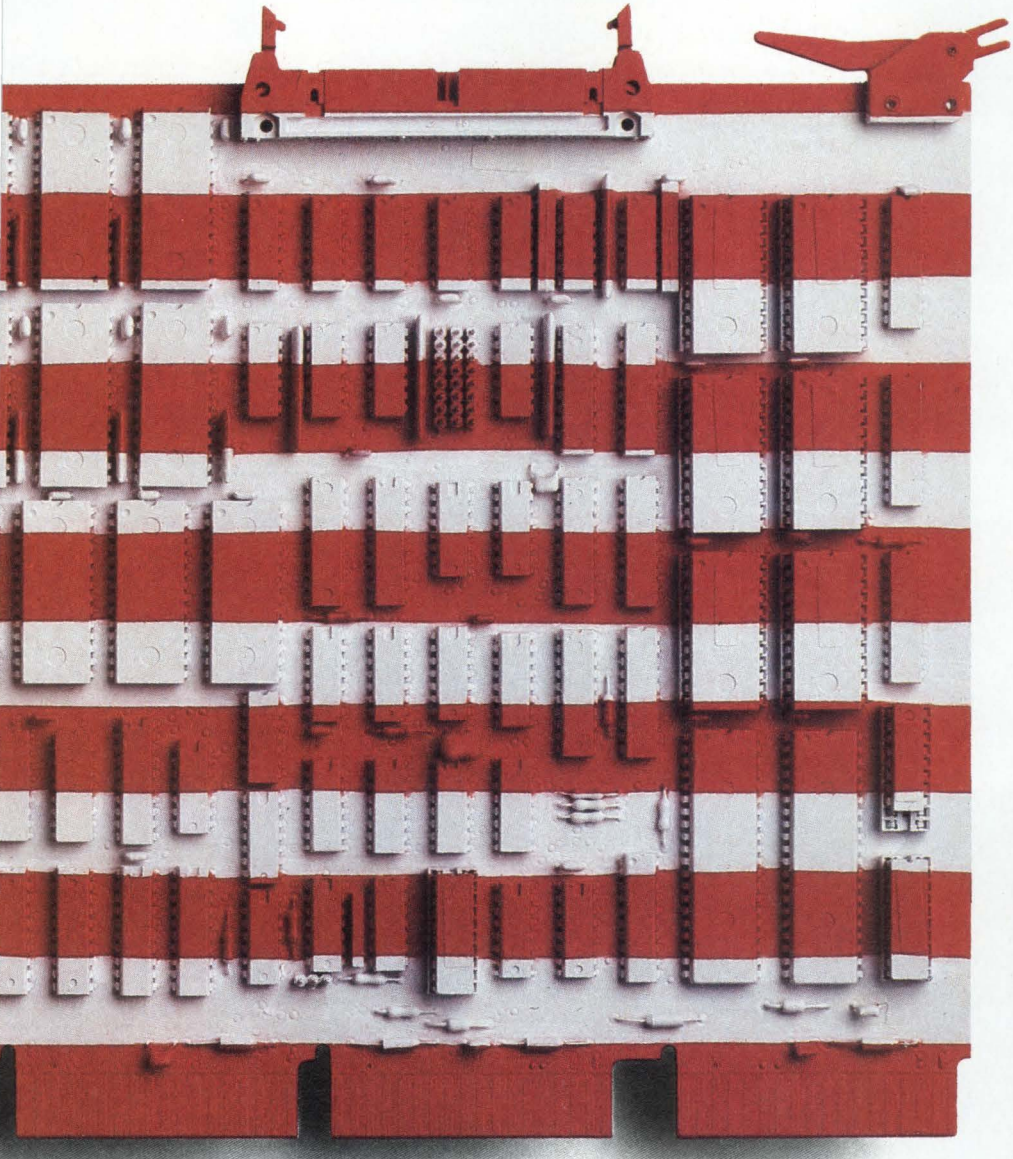

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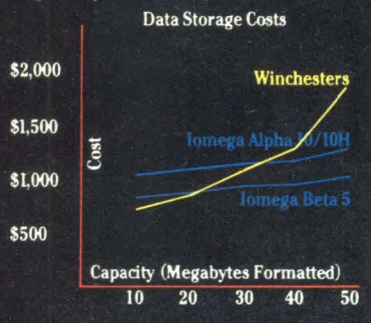
CIRCLE 57

A DECLAR
DATA INDE

When In The Course Of Business Events . . .

OEMs designing systems for today's businesses face two realities. One, data processing is rapidly becoming more decentralized. It is pushing outwards into individualized work units, defined more by job function and applications, performed by more people in more places, demanding more data flexibility—more data independence.

Which brings OEMs face to face with a second reality. Winchesters. Because the prevailing mass storage technology—in the form of large storage units used for access or downloading, or smaller, high capacity desk-top mechanisms—continues to head in the opposite direction. Rather than freeing users to operate effectively in the new environments of distributed data processing, Winchesters keep them device-dependent, keep them tied to a shared system of storage.



Slavery By Any Name . . .

There are lessons here. That the central issue isn't more data, but more data dynamics. And that Winchesters are hardly data dynamic at all.

Consider the aggravations of "wait your turn" access, or the need for lots of "system savvy" on the user's part. Consider the time consumed in backing up and restoring data. And consider the ever-present risk of a system going down or files lost to expensive head crashes.

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Data Transfer Rate	5.0 Mbits/Sec	9.0 Mbits/Sec	5.0 Mbits/Sec
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CIRCLE 58

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Wire-Wrap can't be used with High Speed Logic

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An aeronautical engineer once "proved" that bumblebees can't fly, because they couldn't possibly move their wings fast enough. And a lot of people still believe that.

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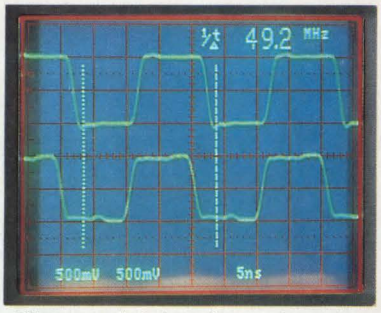
So you can have high-speed logic, plus all the advantages of Wire-Wrap: faster time to market, design flexibility, better thermal management, component pluggability, and the lowest possible development costs. Along with the kind of engineering support you would expect from the market leader.



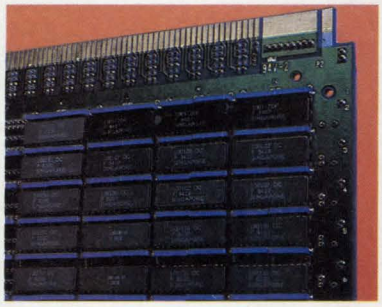
This unretouched photo shows a .6 nsec rise time pulse at the entry point (top wave form) and at the end (bottom wave form) of a 21" Wire-Wrap transmission line. By using twisted pair and properly terminating the line, ringing and reflections are minimal.

VAX-BASED WIRING SOFTWARE MAKES IT FLY

The key to making high-speed logic perform in Wire-Wrap is Augat's VAX-based wiring software.

You might expect problems with crosstalk, uncontrolled high impedance, and propagation delays.

But, in fact, crosstalk can be minimized through the selective use of twisted pair wiring, and transmission line reflections can be nearly eliminated by the proper wiring of terminating resistors. Orthogonal wiring is always routed to minimize line length, and even point-to-point wiring is automated.



F100K ECL devices and terminating resistors on a Wire-Wrap panel.

Once the VAX is done routing and analyzing your circuit requirements, a machine-readable set of documentation is provided to you to assist you in debugging the board and back-annotating your CAE database.

WIRE-WRAP BRINGS YOU A BEEHIVE OF BENEFITS

Wire-Wrap offers numerous advantages in developing and producing high-speed logic boards.

The inherently low capacitance of a Wire-Wrap transmission line increases signal velocity. Circuit changes are easy to make, without incurring sudden, unexpected costs or delays.

Wire-Wrap boards run much cooler than multilayer, because the pins act as radiators. One test showed that the ambient temperature for a large Wire-Wrap board was a full 7 degrees C. cooler than the same circuit in multilayer. That means increased component life and product reliability.

Pluggability makes it easy to replace parts when they fail or upgrade with new components when they become available. Or to work around component scarcity, building boards in advance and plugging in components as they arrive.

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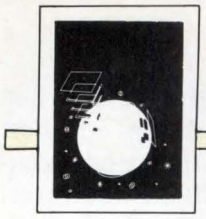


GATEWAYS LINK ASSORTED NETWORKS

Connecting identical networks is straightforward, but handling different types of networks with multiple protocols, priorities, and multiplexing calls for gateways.

by Eugene von Taube

Developing efficient, multipurpose gateways to link local area networks and/or long-haul networks (wide area networks) is the coming challenge in high speed data transmission. Such gateways must support multiple protocol conversions among networks, and at the same time, provide efficient routing of data packets. In addition, gateways perform operational functions such as enhanced control, multiplexing, the forwarding of packets by priority, and temporary packet storage.

Packet switching, the key to efficient gateways, began in the very successful and well known DARPANET fielded by the Defense Advanced Research Projects Agency in the early 1970s. As a result of DARPANET's success, packet switching has become standard practice in modern data networks.

LAN to LAN communications

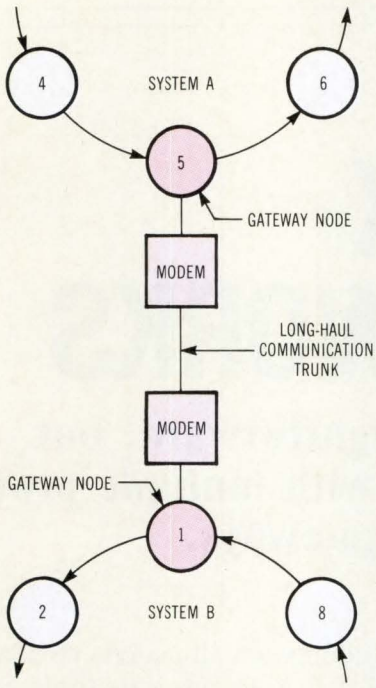
In its simplest form, LAN to LAN communication presupposes LANs that use identical communication protocols and operate at the same speed. When there is a need to connect two such LANs, a simple bridge or gateway node suffices. When there is a packet to be transferred from LAN A to LAN B, the functions of the gateway node are relatively simple. Like any other node on LAN A, the gateway reads the address on all packets circulating within that LAN, but it accepts only those addressed to LAN B. Once accepted by the LAN A gateway, the packet is forwarded to the LAN B gateway. Inasmuch as the protocols and speeds of both LANs are the same, there is no requirement for protocol or speed conversion.

The main purpose of such gateways is throughput. At a minimum, the gateway should be able to process at least 1000 packets/s. This figure is arbitrary, but it satisfies commonly accepted speed requirements. Because the gateway node is identical to all other nodes in the LAN, each node must have the same 1000-packet/s minimum throughput. This throughput is equivalent to a little over a million bits/s—a speed well within the ability of the microcomputers in the interface units.

The best way to optimize throughput is to use modular expandable gateways. This technique presupposes a gateway architecture—hardware and software components—that initially provides only minimum throughput (eg, 1000 packets/s). But, this gateway can be expanded to handle ever larger volumes (at least 10,000 packets/s), to let engineers change the design for specific volume requirements.

Linking several LANs in one overall network not only provides data transport over a wide area, but permits the implementation of dedicated subnets on a hierarchical basis. Dedicated subnetworks can reduce the load on primary gateway nodes. Throughput increases because packets not intended for other LANs or WANs do not pass through the major gateways. As computer devices attached to LANs grow in processing power and diversity, dedicated subnetworks become even more important. But, taking

Eugene von Taube is senior product manager at Codex Corp (Mansfield, Mass). He holds an MBA from the University of Minnesota, and an MS in electrical engineering.



When connecting two homogeneous local area networks, a simple gateway node can be used to transfer packets between system A and system B. The designated node on system A reads all packets transmitted by the other LAN and accepts only those designated for system A. In this case, protocols and speeds of both LANs are the same.

advantage of this increased power and diversity requires the appropriate choice of data routing.

The best path between any two communicating nodes in a single LAN (or two nodes in separate LANs), which communicate through gateways and WANs, is the shortest and least congested one. Although the concept is simple, the gateway designer should be aware that there is no single ideal algorithm to determine that path. Depending on network conditions, one particular algorithm can perform better than another.

One common and simple algorithm, called flooding, floods the network with many identical packets. The packets, traveling in different directions on many random routes, eventually lead to the same final destination. This is considered to be an extremely "robust" algorithm, but it can congest the network with redundant packets. Although reliable, this algorithm reduces throughput because of network congestion and time lost in processing redundant packets. In addition, it requires complex software for the gateway and node microcomputers.

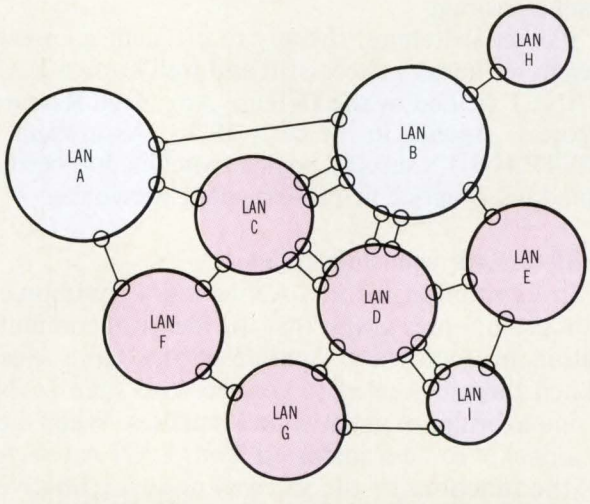
Static, or directory, routing is another widely used routing algorithm. It is based on a routing table that contains preselected optimal routes to each destination. Each node in the LAN has the table. When the table receives a packet, it "looks up" the best path to the packet destination. The routing table cannot adapt to changing traffic conditions, however. For this reason, static routing works well only if the network topology and the traffic volume do not change appreciably.

If the traffic conditions on the network change dramatically, static algorithms cause congestion. In this situation, a centralized routing algorithm is more efficient. This algorithm is similar to the static, but optimal routes are not determined in advance. A central routing control facility computes the best routes based on the conditions of the entire network.

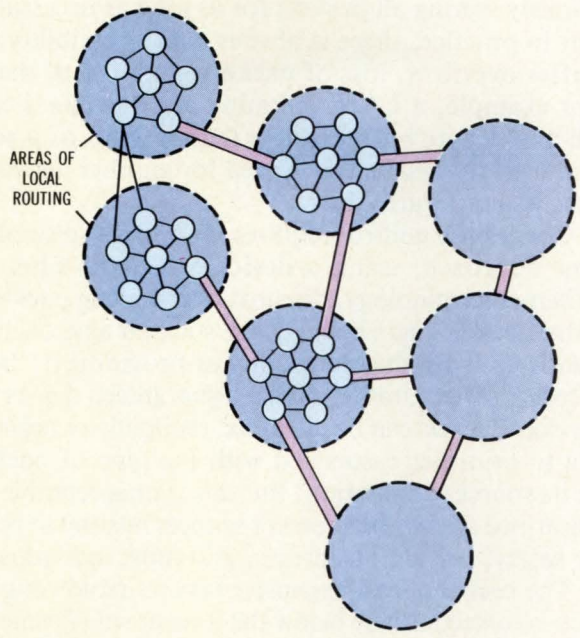
Overcoming routing problems

Although centralized routing is a successful technique, it creates a dependency on one central point of command. If the control center fails, routing fails, and data transmission stops. In addition, routing traffic information to the central control point causes still another problem—overhead functions compete with data packets for the use of the transmission medium. This often increases congestion and reduces throughput.

To overcome the shortcomings of the centralized routing algorithm, the isolated adaptive routing algorithm was created. This algorithm decentralizes the routing decisions and lets each node make such decisions, as required. Each node tries to forward the packet as soon as possible via the least congested route. For direction purposes, a variation of this



A routing bridge can be used to reroute data onto another LAN when the link between any two LANs becomes congested or breaks down. Thus, when the link between LAN A and LAN B is out of service, the bridge routes the data from LAN A to LAN B via LAN C or via any other connected LAN in the network.



As more LANs are interconnected, an enormous amount of detail must be considered to optimize the routing. One method is to create a hierarchical two-tier routing scheme. Here, packets are routed up the hierarchy between superclusters and then down the hierarchy to the destination.

algorithm combines the static algorithm with the isolated adaptive method.

If the transmission channel goes down or becomes overloaded, there is no mechanism to correct the direction of the immediate traffic. To deal with these conditions, a variation of isolated adaptive routing—the backward learning algorithm—has been formulated. This algorithm directs packets along routes where packets traveling in the opposite direction have just passed. The major advantage of the backward learning algorithm is its efficiency and ease of implementation.

Routing within multiple networks

Serious routing problems arise in a network made up of many interconnected LANs because of the very size of the network and the difficulty in determining optimal routes. A hierarchical structure using two-tier routing provides a possible solution. In very large networks, an in-depth hierarchy using superclusters could be established. Packets would be forwarded up the hierarchy, between superclusters, and then down the hierarchy to the destination.

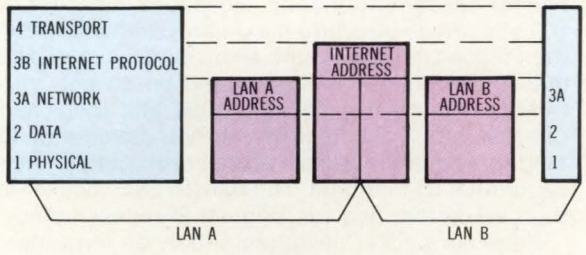
The gateway switch can be expanded to an internetwork gateway which can be used to interconnect not only similar LANs, but also LANs and X.25 packet assembler/dissassemblers and other combinations. Essentially, the gateway is a hybrid packet switch. Such a gateway is needed in multiple linked LANs and to transmit data among these networks using WANs.

Any network or point to point transmission medium that connects geographically dispersed LANs can be viewed as a WAN. WANs can be subdivided into public switched telephone networks, analog leased circuits, and packet data networks. The first two are self-explanatory, but the packet data network is described in more detail.

There are two types of packet data networks—point to point and packet switching data networks. A point to point data line is economical for multiplexed high volume communication traffic and for short distance communications. The most often used PSDN conforms to the X.25 network standard. Such PSDNs are widely used to link dissimilar LANs.

Linking geographically dispersed LANs often requires transporting data through intermediate networks which may be dissimilar. If this is necessary, a PSDN X.25 network in combination with an Internet Protocol (IP) provides an inexpensive solution.

An essential IP feature is the sharing of a common protocol for internetwork traffic by the gateway and LAN nodes. Data transmitted by a network is encapsulated in a packet and forwarded over the intermediate network. After transportation through that network, the address information is removed from the packet header by the receiving gateway located in some other LAN. The IP fits between the network routing and transport layers of the International Standards Organization's Open Systems Interconnection model. To support communications between dissimilar networks requires an extra level of addressing within the network layer. Within any single LAN, the IP is transparent and is dispensable,



Internetworking geographically dispersed LANs often requires transporting data through an intermediate network that may be dissimilar in architecture. An Internet Protocol (IP) provides a common protocol for gateways and LAN nodes on internet traffic. As data is transmitted from network A, it is encapsulated by an address that is removed by the receiving gateway on network B.

although it is useful for data transport among various multiple networks.

Easing traffic congestion

Congestion in intermediate networks often results in lost data packets. The effects of this are seen in the large differentials that can exist in the transmission speeds of the transmitting LAN and intermediate WANs. While LANs currently operate in the megabit range, WANs usually operate at much slower speeds. In addition, the WANs usually process packets through intermediate switching nodes. The fast transmission of packets from the LAN into the intermediate WAN can flood the intermediate network with data packets, causing the intermediate WAN to discard the excess packets.

To avoid the loss of data packets, congestion control is required. In principle, an infinite supply of buffers can be used to prevent congestion by temporarily storing all packets for as long as necessary. But in practice, there is always some possibility of buffer overflow, loss of packets, and loss of data. For example, a LAN operating at 10 Mbits/s can fill a 64-Kbyte buffer in less than a tenth of a second if all the traffic is intended for another network that is temporarily busy.

Congestion control requires innovative solutions. One approach, using a device called the filter in Ethernet terminology, discards overflowing packets. Ethernet designers believe that such an approach is consistent with the philosophy of providing a "best efforts" service, rather than a "guaranteed delivery" service. Packets can be discarded randomly or according to priorities associated with the type of packet or its source/destination. But this is unacceptable to the armed forces, government services relating to public safety, private businesses, and most individuals.

The best and least expensive way to avoid congestion is to keep traffic below the level at which general congestion occurs. The congestion control technique based on this principle is called isarithmic. It keeps the number of packets at or below a critical level. The technique is effective within a single network, but it tends to lose efficiency in network interoperations since it does not guarantee that an individual gateway will not suddenly be flooded with packets from an outside source.

But regardless of the type of congestion control adopted, the gateway nodes can form a bottleneck. Increased internetwork traffic causes increased contention for the gateway resources and, although routing algorithms can send traffic down alternate routes, unexpected congestion can occur at other nodes. Specifying an efficient congestion avoidance mechanism in a large network is difficult because traffic congestion can occur in some other, possibly quite remote, overloaded part of the network.

While much attention is given to routing and addressing in large interconnected networks, flow control is often neglected in gateway design. Because of the long distances that can exist between sources and destinations, any flow control technique must give priorities to the packets coming from the remotely located LAN. If this is not done, then very slow data flow rates may be seen on the longer paths.

All gateways modify the content and format of the packets they handle. For example, gateways may encapsulate the packets into larger packets as in the IP approach. An even more technically complex gateway is needed when LANs of different types and/or data devices, whose protocols differ from the ones on the LAN, are interconnected. Reconciliation of the dissimilar protocols is usually achieved by terminal emulation and protocol conversion.

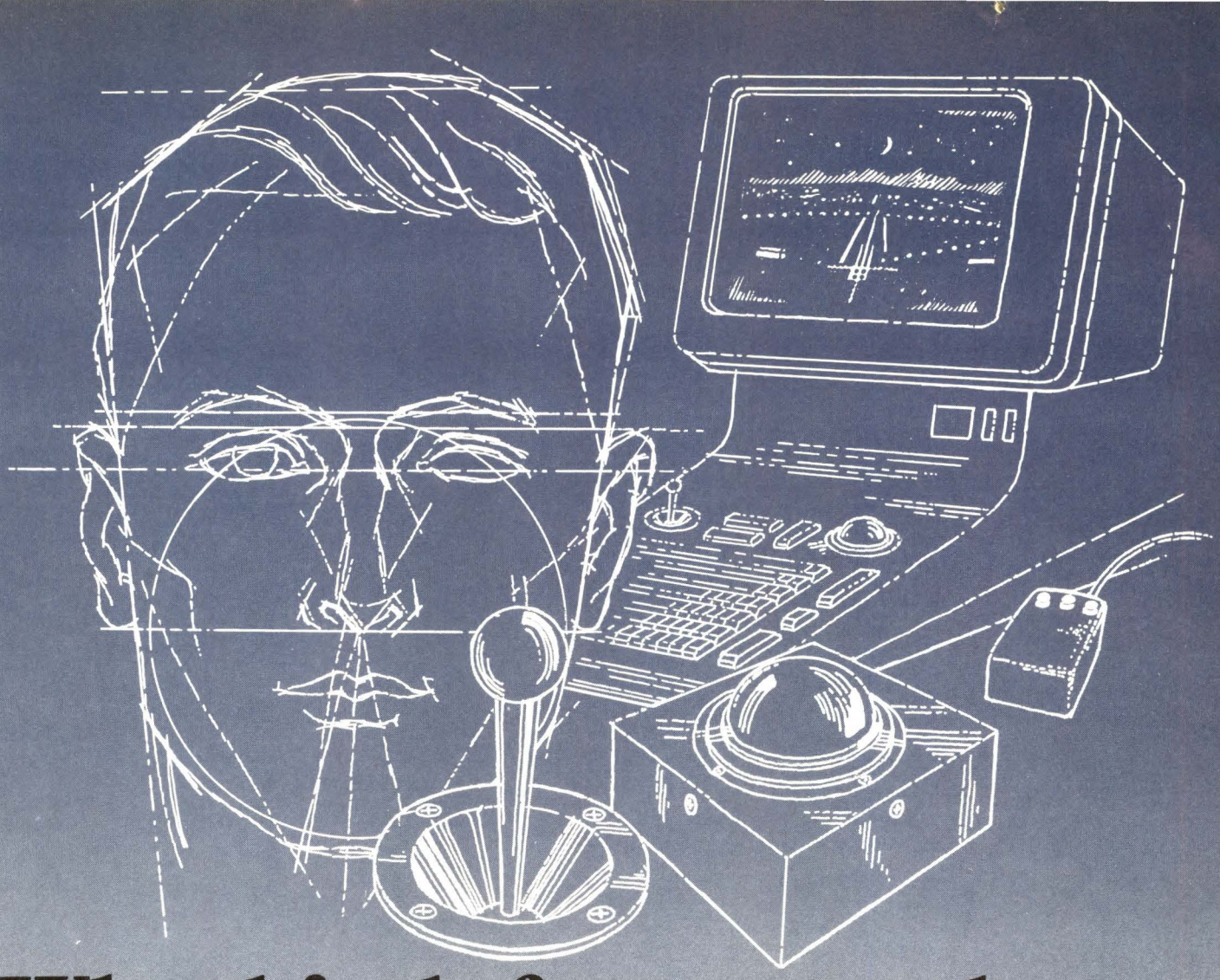
The packet switching method

By definition, packet switching is a technique for switching message packets. In concept, a message packet is identical to an envelope in the postal system. The packet bears an address and other header information and contains a message or a part of a message. The message in the packet is the data being forwarded.

In electronic communication, a packet is a string of bits of any length up to an arbitrary maximum. There is no standard packet length, but 1096 bits is a common length. This corresponds to 137 eight-bit ASCII characters. ASCII characters may be defined by only 7 bits, but if a character by character parity check is desired, the eighth bit is needed.

Data to be forwarded over a network or among networks is deposited in packets. Packets bear the address of the message contained in the packet envelope, a sequential identification number, and other header data. In a 1096-bit packet, for example, 800 bits are reserved for the message and 296 bits for header information. Messages in excess of 800 bits are divided into maximum 800-bit lengths, then placed in packets. As an example, a message that is 2888 bits in length would be divided into three packets—two packets 1096 bits long, and one, 696 bits. Packets arrive at their destination in random sequence and are sorted according to their sequential ID numbers. The data in each packet is then extracted, and the original is reassembled.

Because packet switches subdivide long messages into shorter packets, many messages from many sources—messages that are both long and short—time share a single transmission channel. Short messages are not delayed by long messages. Packet switch hardware is minimal and an inexpensive microcomputer comprises most of the hardware. The software is also simple. As a result, packet switching systems are economical to build and operate, and message transmission is fast and efficient.



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Emulation can provide connectivity and supply the users with the necessary information. The information being delivered to the user can be printed or viewed on the screen. However, emulation has certain limitations. With emulation, personal computers appear to be dumb terminals when they are integrated into some other network with a different architecture. In this case, users cannot use the full power of personal computer application programs. As application programs or personal computers become more sophisticated, this limitation becomes more critical.

Another drawback of emulation is the limited throughput capabilities on a gateway that uses emulation to integrate networks with dissimilar protocols. Bottlenecks will always exist in certain segments of a datacomm network, so the issue becomes the minimum throughput acceptable for the network. The inherent inconsistency in speed affects the desired throughput level—LANs are designed for megabit data rates while terminal emulation is often done at 300-bit to 19.2-kbit/s data rates.

In addition, terminal emulation does not provide a data recovery mechanism and integrated LANs forward data at high speed rates over large distances and diverse media. Bits of the data are inevitably lost or damaged. Therefore, having an error correcting mechanism to help restore the integrity of the received data is essential.

The modern approach to the reconciliation of dissimilar protocols is protocol conversion. A gateway based on true protocol conversion can provide better throughput, better error recovery, and better network integration than terminal emulation. Protocol conversion in theory is rather simple, but implementation is rather complex. The challenge becomes apparent when comparing the levels in the International Standards Organization's Open Systems Interconnection to those of IBM's System Network Architecture. In both schemes, the lowest level is the physical or electrical interface. The data level is next. It governs the lowest level data protocol conversion that can be accomplished using one VLSI chip. Next come the network and transport level protocols. To achieve true protocol conversion, all differences in architecture and protocols should be accounted for.

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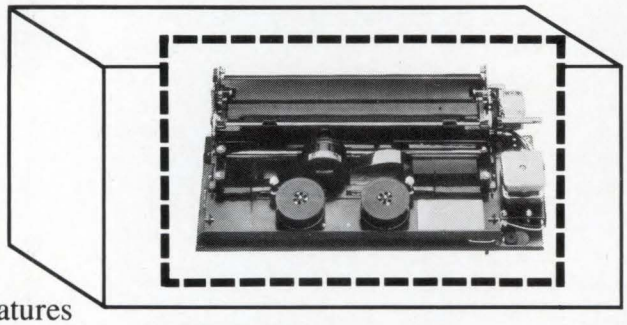

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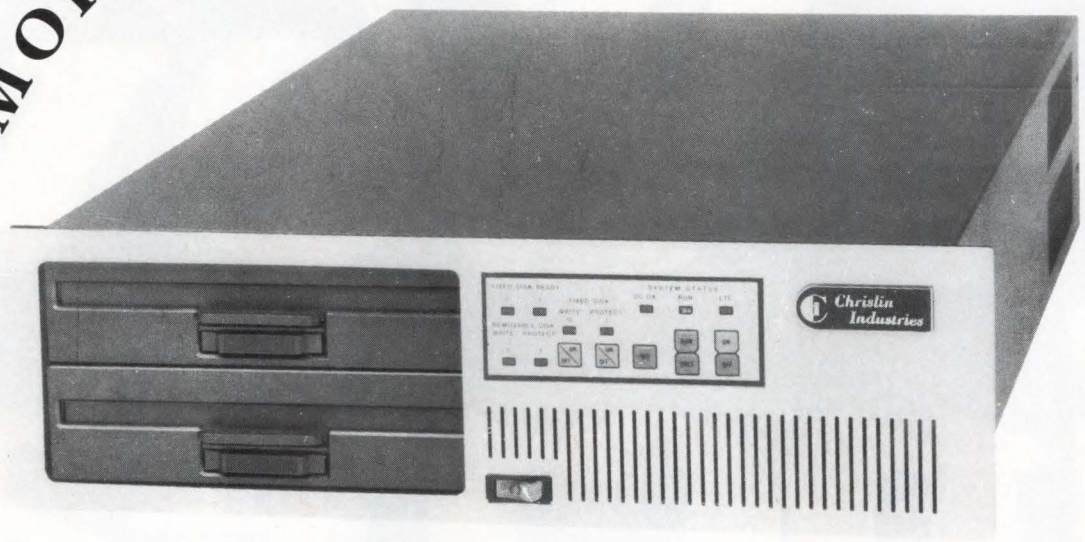

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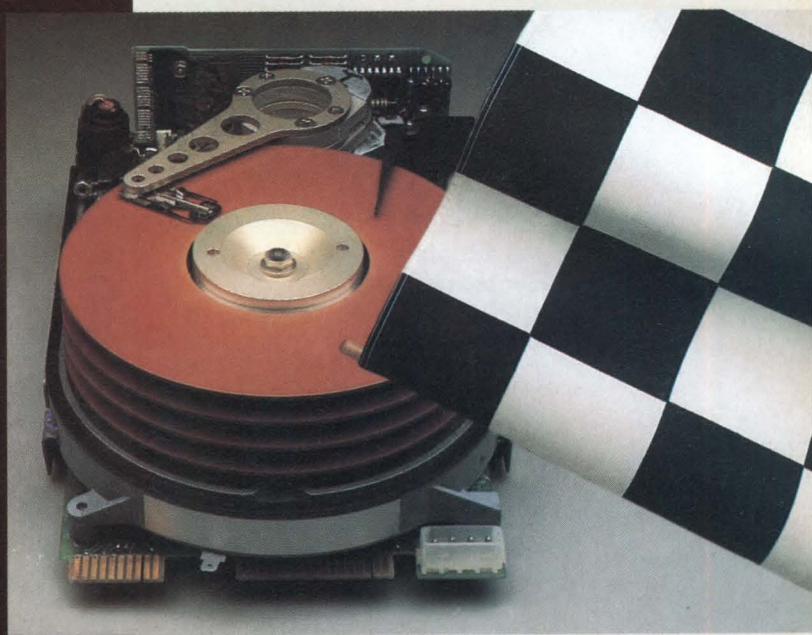

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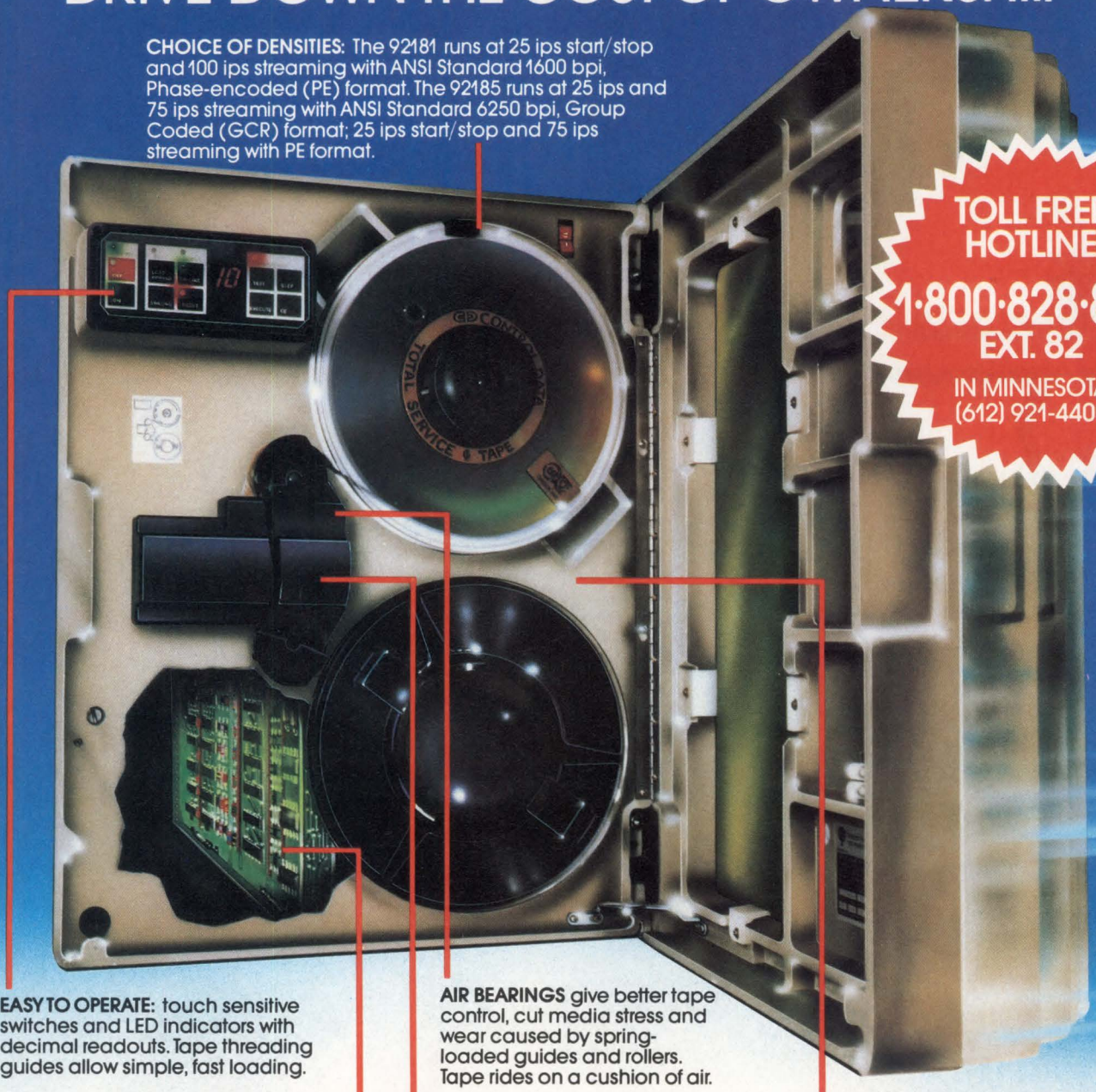

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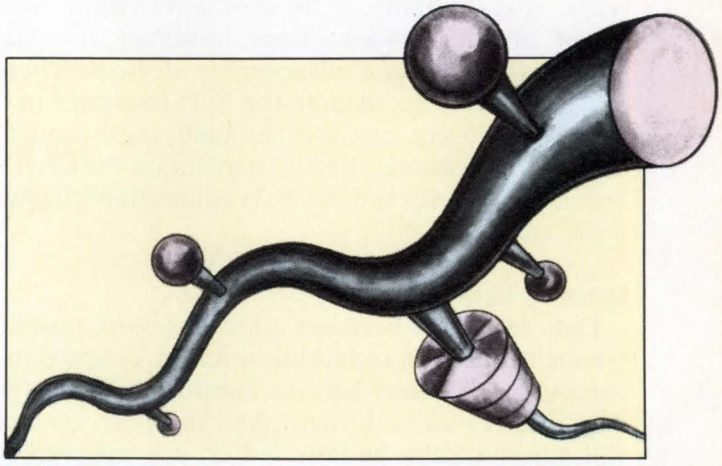
CONTROL DATA

X.25 STANDARD SIMPLIFIES LINKING OF DIFFERENT LANs

Interconnecting with the X.25 protocol allows networks to encompass different local area network configurations in wide area, packet-switching systems.

by Mark Stieglitz

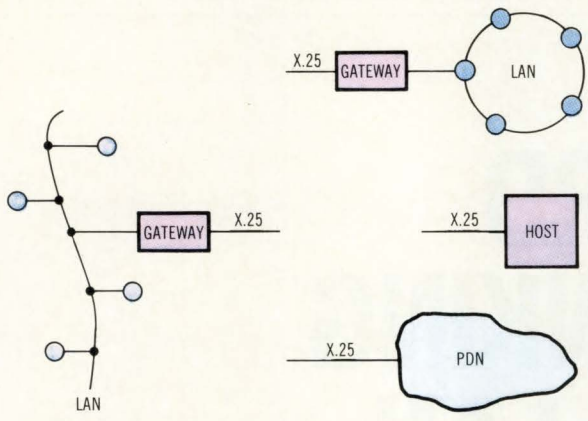


Today's finely tuned local area networks are the link between personal computers or workstations located in single organizations or departments. Since the capabilities needed by these LANs are usually determined by the environment in which they will be used, the underlying communication protocols are usually restricted. Although these protocols have in common the transmission of data frames, the data formats in these frames (and the error correction techniques used) need not be the same for all LANs.

While ideal for an office, a LAN cannot directly interconnect workstations and data bases in multiple facilities. Such communications over longer distances (ie, a mile or more), are provided by a public or private wide area network. The WAN protocol is substantially different from that of the LAN because it must provide for alternate routing, potentially high error rates, and lengthy propagation delays—especially on satellite links. Communication between the two networks requires a gateway to interface with the low level protocols. With a gateway available to connect the popular LANs to long-haul networks (WANs), it becomes a simple matter to interconnect different LANs, even in the same organization.

The ideal gateway protocol needs three elements. It must be in common use, be efficient over long distances to complement the LAN protocol, and be affordable. The X.25 protocol standard for data communications over public data networks fills the bill. Since the mid-1970s, communication over PDNs such as Telenet and Tymnet has been popular due to its reasonable cost. Both cost and data reliability of such a packet-switching system are insensitive to the distances covered. And, because the transmission facilities are used only when sending data, charges reflect only the amount of data transmitted. Such a pervasive and attractively priced infrastructure is a prerequisite for a useful and cost-effective LAN gateway.

Mark Stieglitz is director of LAN marketing at AST Research, Inc (Irvine, Calif). He holds a BS in industrial technology from the University of California at Long Beach.



An X.25 interface augments a local area network in three ways. It eases interconnection to another LAN of the same or other type, directs LAN to a mini- or mainframe computer, and directs interface with a private long-haul data network or public data network (PDN).

Although such services have existed for several years, users seeking PDN cost advantages have dialed in with asynchronous terminals to local packet assembly and disassembly devices. These PADs then connect them to the X.25 backbone network. LAN users, on the other hand, must connect to the X.25 network directly to maintain the LAN's high data integrity and the X.25 connection's higher serial speed.

Ensuring data integrity

Data reliability becomes critical as more people, especially those not technically oriented, use personal computers. As users become comfortable with the data integrity of a chosen LAN, this performance will automatically be imposed on any intervening data communication link. Users will not tolerate an occasional data error simply because personal computers, which look to LANs for specific data, need something that the LAN system has routed through a gateway. The entire data communication system must be closed from an error control point of view. It thus becomes the network architect's responsibility to ensure data reliability. This requires the use of error controlled protocols throughout the network.

The cyclic redundancy check, used for error detection and the sliding window method in the retransmission protocol, ensures end-to-end data integrity in X.25. In normal operation, a sender transmits its sequenced frame or frames into the network. While sending, the full-duplex X.25 continues to watch for incoming frames.

In the gateway, the incoming X.25 data frames are routed to the LAN destination while incoming control frames (or data frame control headers) are used to acknowledge earlier message transmissions. A typical X.25 system can transmit up to seven frames before the first is acknowledged. Because of the time required for an acknowledgment to come back, the X.25 approach is more efficient. Data transmission and error recovery procedures are performed in parallel.

Using X.25, the sender cannot free the transmission buffers immediately after transmission, but must wait for acknowledgment in case the frame must be retransmitted. Buffering is usually no problem as seven, 512-byte buffers usually suffice for transmission. A bigger challenge for the gateway software is the full-duplex nature of X.25. The gateway can choose to ignore any incoming data that it cannot process immediately (as many LANs do), but this is inefficient. A better way to reduce or "flow control" incoming data is to send the X.25 network a receiver-not-ready control message. This holds the network until the gateway software frees a buffer.

Matching serial speed

Efficient flow control is a key consideration in gateway design because of the unpredictable data profile passing through the gateway. For example, many LAN users, or none at all, may decide to access the gateway at any given time. Moreover, the raw data rates of the networks are seldom close.

On a homogeneous LAN, flow control is usually handled by a low level protocol. As a result, only a limited amount of data can be generated on a shared wire at a time. In fact, data frame pre- and post-ambles are often added to all messages to ensure that receivers have at least a nominal amount of setup time before any transmitter on the LAN can start. With the receiver properly set up, data that cannot be stored is simply ignored, and retransmitted later.

By design, X.25 does not have a similar "throw it away, it will come back" luxury. Because of the slower transmission speed and longer transmission distances in X.25 applications, anything thrown away is much more costly in terms of bandwidth than a corresponding message on a high speed LAN. Thus, a major portion of the X.25 protocol involves cutting down on data retransmissions. Anything discarded wastes bandwidth—a chargeable commodity on a PDN. Since the PDN bandwidth is shared, proper flow control is necessary to allow others to use the X.25 channel while an individual user or node is busy.

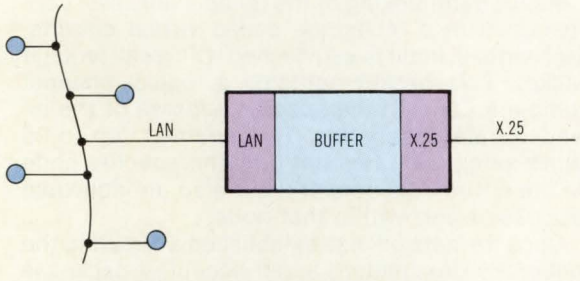
Applications of efficient gateway protocols are not limited to the LAN and PDN connection. X.25 is also valuable for connecting the LAN to another

LAN or to a local host within a single building. A few of the most popular LANs have direct native bus interfaces for some of the most popular minicomputers. On the other hand, the LAN vendor often supplies a generic interface unit with asynchronous ports that can be directly connected to ports on the host.

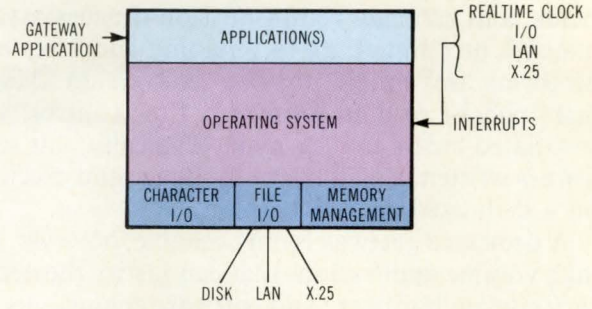
Additional X.25 advantages

In addition to the cost, installation, and reliability concerns when using multiple cables, this method is generally limited to speeds of 9.6 kbits/s. The convert to asynchronous LAN-to-host gateway technique is too simple. It forces users to take high speed data from the personal computer, transmit it over an efficient LAN, and then squeeze it into a tiny serial channel, on its way to a high speed mini- or mainframe. This method effectively limits LAN-to-mainframe applications to interactive I/O. On the other hand, X.25 provides an efficient and standardized communication link between LAN and host. The X.25 protocol is already implemented by virtually all mini- and mainframe computer manufacturers, partially due to its inherent technical capabilities and partially due to X.25's status as an international communication standard.

With the LAN-to-X.25 gateway, a single connection between the LAN network interface unit and the host supports efficient, high speed (typically 64 kbits/s to 1.544 Mbits/s) data exchange. An added benefit to the multiple asynchronous approach is X.25's ability to allocate the LAN-to-host bandwidth as needed. This allocation, which is transparent to the user, is accomplished with a multiplexing technique known as virtual circuits. Using this standard feature of X.25, one user may have the total link bandwidth, or many may share it, depending on the instantaneous system need and user's system configuration.



The gateway is a store-and-forward protocol converter. Incoming user data is error checked and separated from the network frame. It is then placed into a buffer where it is encapsulated with the transmission protocol and sent out on the other side when that protocol allows.



A gateway can be built on a single- or multitasking operating system, depending on required gateway throughput and power of the underlying processor. The LAN and X.25 I/O protocol drivers map into the file system when they resemble block-oriented devices.

X.25's virtual circuits allow one or more users on a LAN to access multiple host sessions. This feature is becoming both feasible and necessary with today's windowing personal computer operating systems. Since X.25 is a packet-oriented protocol, it is typically integrated into the file management portion of an operating system. In the personal computer environment, simultaneous X.25 virtual circuits are often managed with the technique called "drive aliasing." With this technique, spare disk drive designators map user and application software requests for information to the proper X.25 virtual circuit.

Gateway implementation

The gateway is simply a store-and-forward protocol converter. It receives messages from the LAN like any other LAN node by comparing each message's destination address with its own. If a match is found, the gateway uses a combination of the message's source and destination address along with included control information. Thus, the gateway computes the address for which the data is destined on the other network. This computation is really a gateway table lookup. Using the X.25 gateway, the LAN user must have set up the X.25 connection by originally supplying the complete X.25 address. The gateway at this point deals only with logical channel numbers.

Like LANs themselves, there are many possible gateway implementations, depending on the required cost/performance ratio. A gateway is implemented with a combination of hardware and software. The hardware usually consists of a general-purpose high level data link controller (HDLC), such as the Zilog SIO (serial I/O) chip or the Intel 8274, a DMA controller, and miscellaneous hardware counter/timers. The HDLC chip handles all framing and cyclic redundancy check generation/verification.

The gateway software interprets the X.25 control and arranges retransmission if necessary. It ...nes incoming data to outgoing addresses and ...rforms any simple protocol conversion. Major tasks consist of data buffering, flow control, and associated buffer management. Typically, this software is written in a high level language and executed on a dedicated microprocessor.

A dedicated gateway is only suitable, however, for high volume applications that can justify the necessary custom hardware and software engineering. A more general solution is to use off-the-shelf components. These components consist of hardware and software, on a personal computer base, to configure a gateway for the given protocol pair.

The personal computer as a gateway

The gateway software can be viewed as an application program running on top of an interrupt-driven operating system. The operating system typically executes the gateway application, an additional user application, or idles, until an interrupt occurs. When a data-received interrupt is detected from either the LAN or X.25 controller, for example, the system checks the incoming message's destination address. It then routes it to another running application, the local disk storage subsystem, or to another communication controller. Sending the message to another communication controller merely involves adding it to the appropriate transmission queue. In addition to its communications and disk I/O control, the operating system manages the realtime clock and memory pools. The realtime clock is used by the X.25 section of the gateway program primarily to detect unacknowledged (presumed lost) messages. This differs from failsafe timers associated with conventional I/O requests. The X.25 protocol actually includes many states that are driven by configurable timers. This protocol dependence on discrete time requires the timer operation to be not only consistent but accurate. Also, since these timers are usually programmed to be in the hundreds of milliseconds range, it is not feasible for the X.25 application to "loop" in order to detect expiration.

Memory management is one of the real challenges to a successful gateway design. It must buffer data between the two communication interfaces to smooth any temporary bursts from either end. In addition, it must provide speed matching through efficient flow control. The memory management system also deals with potentially different buffer management techniques used by the different protocols. The LAN controller typically has an open-ended first in, first out scheme. The X.25 section uses a simple indirect lookup through a table reflecting the protocol's need to retain the transmitted data until it is ultimately

Communicating by means of X.25

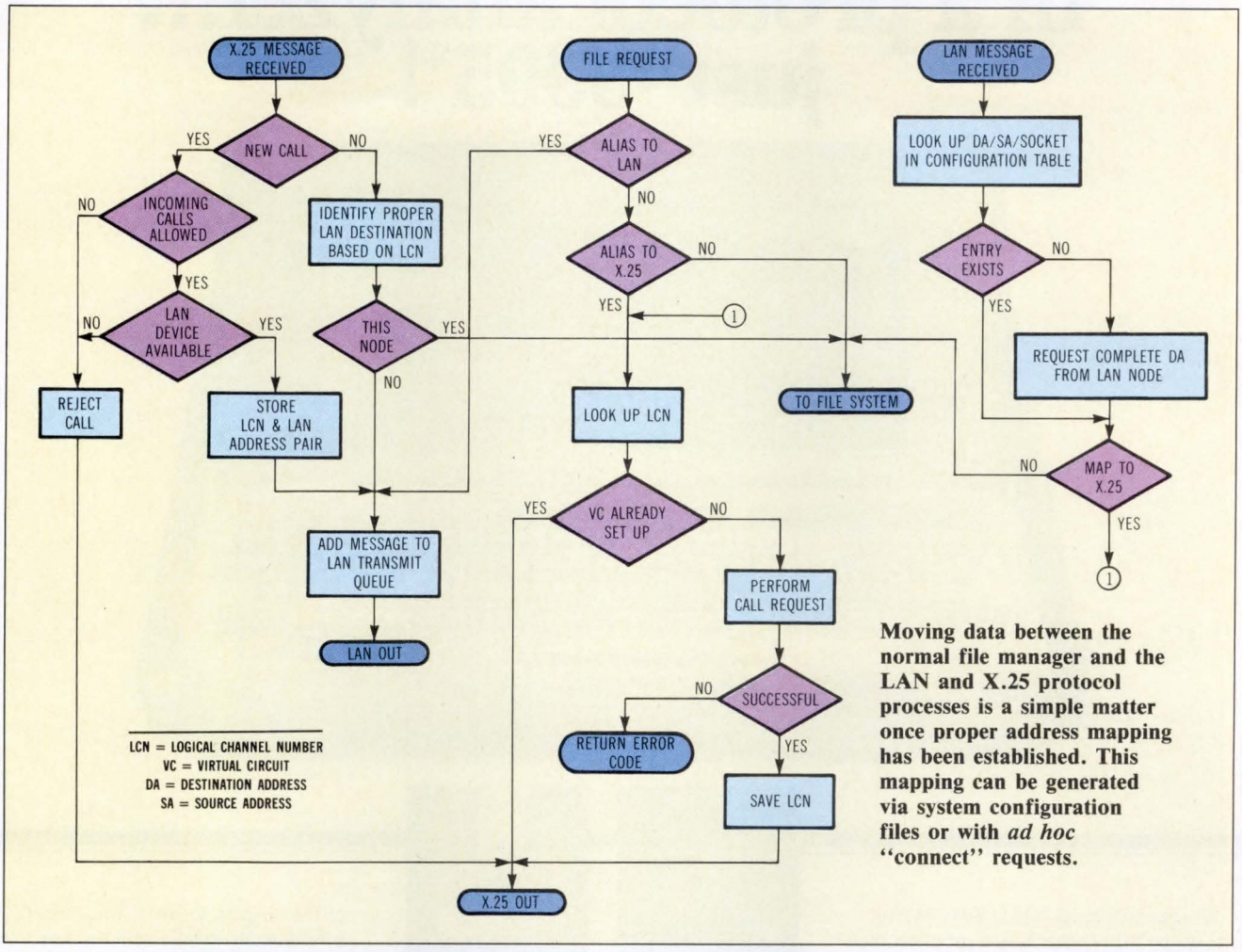
X.25 is designed to make communications between intelligent digital equipment in a packet mode on public data networks easier. It is an evolving standard first approved in 1976 by the International Consultative Committee for Telephone and Telegraph. A revised edition, X.25-1980, widely used today with a minor 1984 update available, is offered as an option by some vendors. The X.25 standard is defined in terms of the lower three layers of the seven layer reference model for the Open Systems Interconnection from the International Standards Organization.

The X.25 physical layer sends binary information over the communication channel, including control and data signaling. It is typically implemented with X.21*bis*, a method virtually identical to the common RS-232 interface. X.21 is a more elaborate physical connection method with fewer electrical signals, but it is not yet in common use.

Corresponding to layer 2 of the OSI model, the X.25 link level is primarily responsible for sending error free data over the physical channel. The link level protocol supports a pair of communicating units connected point to point. These two entities build control and information frames on the physical bit transportation service provided by the physical layer. The control frames are used to establish synchronization in an initial connection. Link level information frames have control information (sequence numbers), level 3 control and header information, and user information. Each link level information frame contains a sequence number which, with defined protocol timers and control messages, ensures that any frame lost or corrupted by the physical layer is retransmitted. The link level ensures data transparency and reliable frame delimitation with the HDLC technique of bit-stuffing.

The X.25 packet level, also known as X.25 level 3, allows multiplexing of the reliable link level connection with a technique called virtual circuits. Each virtual circuit is established with a call request packet. This packet contains a logical channel number (LCN) and the specific address of the intended data destination. This address, (up to 15 digits long), identifies not only the specific node on the entire X.25 network, but also an individual process or port within that node.

Once the network has established a circuit to the requested destination, a call accepted packet is generated on the same LCN. From this point, all information packets with a given LCN are routed to the previously addressed destination. Then an X.25 node can be configured with a number of permanent virtual circuits and the specific addresses are pre-associated with LCNs.



Moving data between the normal file manager and the LAN and X.25 protocol processes is a simple matter once proper address mapping has been established. This mapping can be generated via system configuration files or with *ad hoc* "connect" requests.

acknowledged. Each buffering method is optimized for the characteristics of its associated protocol and must be matched by the gateway.

A personal computer can accommodate many different LAN types. Since the LAN interface need not have been designed explicitly for gateway application, even proprietary interfaces such as the IBM PC Network can be used. The ability to simply swap LAN modules is being made even easier with IBM's migration to a common NETBIOS interface whereby all different LANs appear the same to the higher level software.

There is a rich hardware selection on the X.25 side as well. Simple HDLC protocol modules, such as the CC-232 from AST Research, are popular. These hardware intensive controllers leave much of the actual protocol processing to the host, which is cost effective whenever sufficient processing power is available. Such processing power is becoming especially available and cost effective with the introduction of personal computers like the IBM PC/AT.

The CC-232 is a two-channel controller with each channel configurable as either data terminal equipment (DTE) or data circuit terminating equipment (DCE). Serial rates can be up to 38.4 kbits/s, though this is typically limited by the X.25 protocol software to 9.6 kbits/s. The controller supports full modem control and contains the interrupt-driven hardware interface needed for gateway applications.

The primary advantage of a comparatively simple controller is its system reliability. By not duplicating the host microprocessor and the onboard memory, the simple communications controller uses less power and generates less heat. Also, reduced component count translates into more available real estate for additional (but not necessarily communication related) functions to reside on the card. Keeping the protocol software on the host instead of in adapter firmware (ROM-based) eases upgrades as protocol standards evolve. Lastly, a simpler adapter costs less than more complex offerings.

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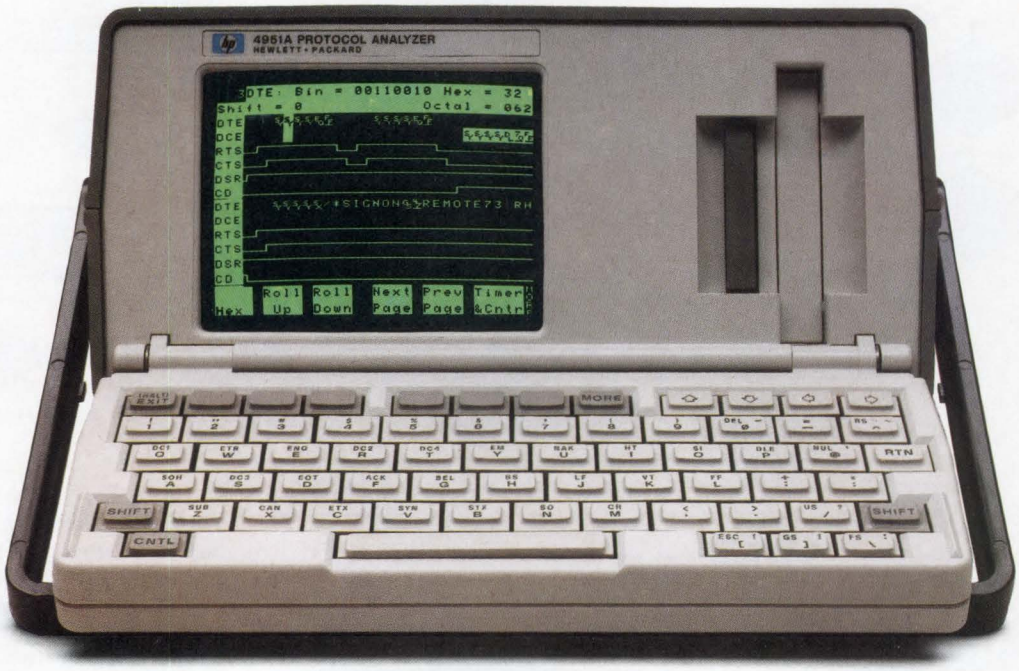

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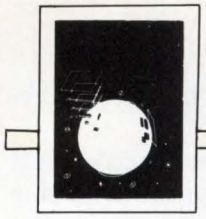

CHOOSING THE BEST LOCAL AREA NETWORK FOR ANY APPLICATION

Regardless of the application, a LAN that adheres to some standard provides the most cost-effective, long-term approach to networking.

by Richard I. Wittlin and Daniel V. Ratner

When choosing a local area network, the first and most important decision to make is whether to use a LAN that adheres to an existing or emerging standard, or to go with a unique or proprietary solution. While it is certainly true that a unique solution is best in some applications where performance is the overriding issue, most data communication requirements can be met with a standard solution.

A standard solution is beneficial for many reasons. One key benefit is that there are usually a number of vendors supplying products that adhere to the standard. This fosters competition, resulting in continual development and enhancement of the product offerings, as well as lower cost. It also means that a particular LAN technology can be obtained from more than one source, which helps prevent obsolescence due to the whims of a vendor's product strategy.

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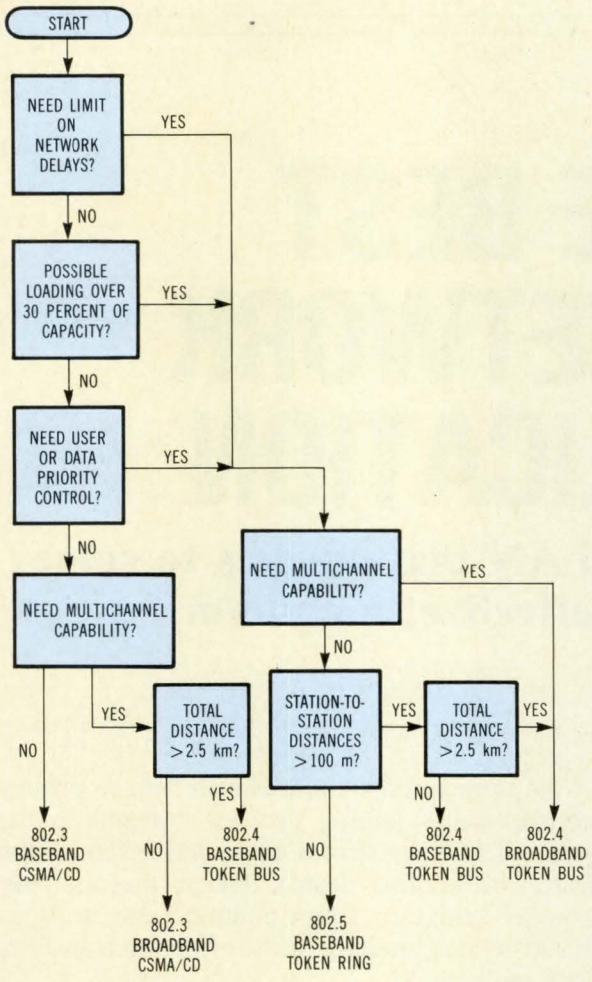
Communication standards also help to promote interoperability among devices attached to data communication systems. Once a device can communicate with another device, device vendors have a strong incentive to adopt common protocols and data structures, making the information transferred easily understood.

Facing crucial performance issues

Basic considerations for any LAN choice are whether or not the network can transfer the amount of data sent at a required rate, among a required number of users, and over a required distance. No one access method and medium can cover all the bases and be the best under all conditions. Each has its strengths and weaknesses. Carrier sense multiple access/collision detection methods excel where network traffic is "bursty" and frame arrival times are not critical (eg, for asynchronous terminal communications). As network use increases, collisions between transmitted frames become more likely. The collision resolution method does not guarantee that further collisions will not occur when a station makes repeated attempts to access the network. For this reason, the CSMA/CD network cannot supply an upper bound on the time required to transfer data across the network.

The traffic load threshold at which CSMA/CD becomes less efficient due to repeated collisions is approximately 30 percent of maximum capacity. If network loading is less than this and occasional long



Using criteria such as network delay, capacity, priority control, multichannel capability, and distance helps network designers choose a LAN that adheres to one of the IEEE 802 Committee standards.

transfer times can be tolerated, CSMA/CD is the desirable choice. However, if present or future requirements involve heavy network loading of process control, digitized voice, high speed computer aided design/computer aided manufacturing, or synchronous traffic, then a token-passing network is more appropriate.

It is important to consider peak loading situations as well as average traffic volume when determining the network throughput requirements. Although a CSMA/CD system might appear ideal for a network with hundreds of stations that rarely transfer data, certain emergency situations (eg, plant-wide power failure), could result in an instantaneous loading far above average. As all stations on the network attempt to report the problem and request reinitialization from the network manager, throughput could go to nearly zero because of repeated collisions. It is important, therefore, to consider networking requirements under all conditions.

If the network is expected to experience periods of heavy loading, there is a feature of token passing that makes it attractive—the ability to set priorities for data frames and users. Critical users can be given increased access to the media by lengthening their allowed token hold time.

In addition, the token bus protocol defines four priorities of data frames. The highest priority frames are sent providing that the token hold time is not exceeded. The lowest priority frames are sent only if the time for the token to make a complete rotation around the ring is less than the predetermined amount. Low priority frames are sent as quickly as high priority frames if the network loading is low. They defer to high priority traffic if the loading is high.

The token ring approach has the most controlled priority scheme of the three access methods endorsed by the IEEE 802 Committee. Stations circulate tokens that have a priority associated with them. If a station has high priority data to send, it requests a high priority token from the frame originator by changing bits in a special priority request field in the token or data frame as it passes. The originator raises the priority of the token and sends it around the ring. Only stations with that priority of data or higher can use the token. This enables stations that have high priority data to access the ring first, regardless of the network load. This is desirable in some special applications.

Another factor that affects media access performance, as well as influences the choice of media, is the length of the network. To detect collisions accurately, CSMA/CD has data rate/system length and system length/frame size trade-offs. For the 802.3 baseband network, these parameters have been optimized at a 10-Mbit data transfer rate, a 512-bit minimum frame size, and a 2.5-km maximum end-to-end distance. The broadband proposal, currently being finalized in IEEE 802.3, has nearly identical limits as those for baseband. In cases where broadband is chosen as the desirable medium because the network is large in geographical extent, the distance limitation may be unacceptable. In this case, IEEE 802.4 token bus would be the best choice.

Deciding which medium is best

The media options chosen for the 802 LANs include shielded twisted-pair cable, baseband coaxial cable, and broadband coaxial cable. When choosing a LAN, network designers must consider that some access methods are better suited to a particular medium than others. Shielded, twisted-pair cable is the only medium presently supported by the token

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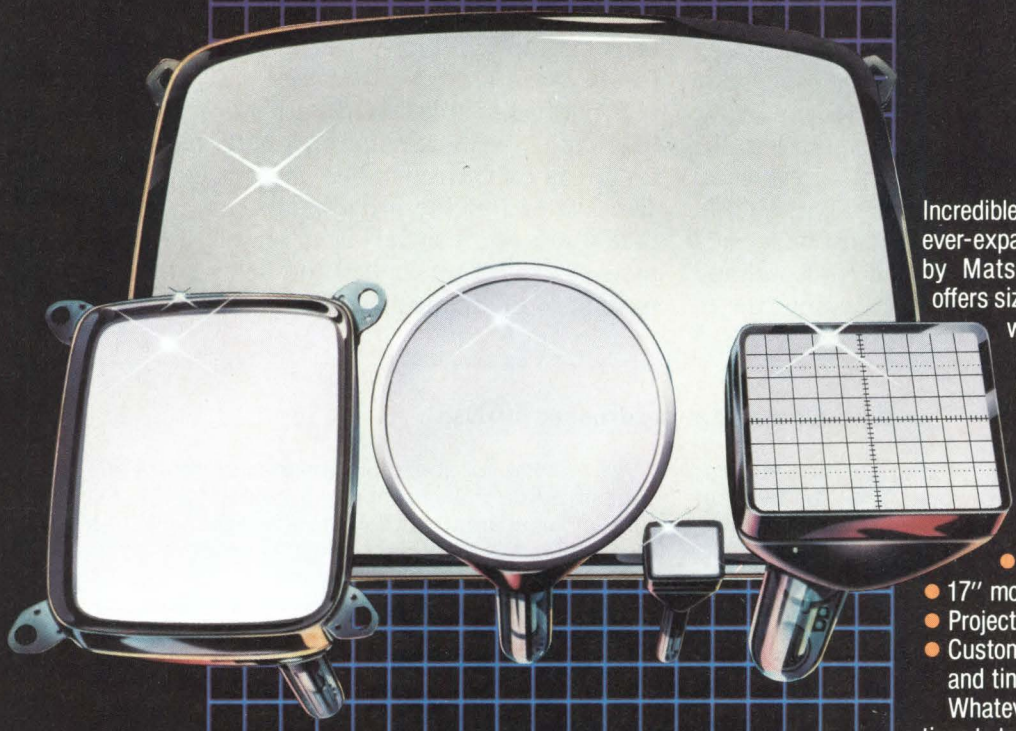

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ring method. It is limited in its frequency response and ability to run long distances, but has excellent noise rejection. This medium is ideal for the token ring method because it need only run from station to station. Each station functions as a repeater to restore the signal to its original state.

Coaxial cable has been the medium of choice for the baseband bus topologies of CSMA/CD and token-passing networks. It can run longer distances than shielded, twisted-pair cable but is not as noise immune. When stations interface with the baseband coaxial cable, transmission properties of the cable cannot be disturbed. This constrains how and where the interface assemblies are allowed to attach to the cable. For example, 802.3 specifies that the cable can be tapped only at specific intervals along its length. The access unit drivers and receivers must be located right at the tap. The 802.4 standard for baseband transmission at 1 Mbit uses a "tee" connector to couple to the cable, but the cable length from the bus to the station cannot exceed 1 ft.

At this time, only the 802.4 standard token bus employs broadband cable as the transmission medium. Broadband cable systems have superior frequency handling characteristics, can run the longest distances, have excellent noise rejection, and can carry signals for several independent networks at once. The network interface units need not be located at the main cable. Impedance matching taps allow drop cables of up to 30 m to be run from the bus trunk to the station.

Broadband cable systems are more complex than baseband systems. Signals in a particular frequency range can only travel in one direction on the system. The low end of the broadband frequency range is used to transport signals from remote sites to a common central point, called the head-end. The high portion of the frequency spectrum is used for signals

IEEE Committee addresses LANs

The IEEE 802 project is making a major effort to standardize local area networks. The primary focus of this effort is to develop standards for the lower two layers of the International Standards Organization's Open System Interconnection reference model, namely the physical and link control layers. In the IEEE 802 standards documents, these layers are subdivided into sublayers, known as the logical link control, media access control, physical, and medium layers.

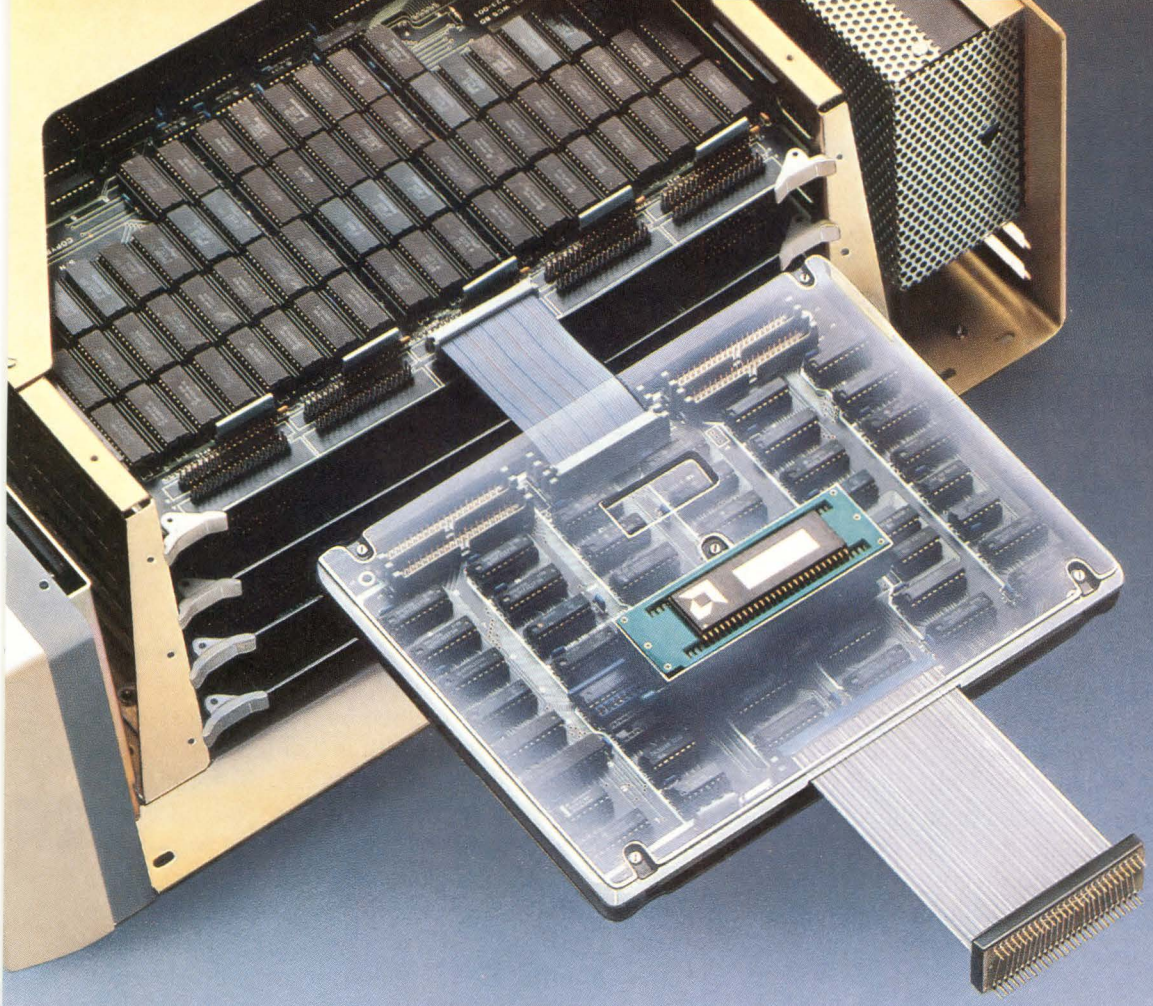
The logical link control sublayer is the common interface to the higher software layers. All the access methods to the logical link control sublayer allow the station processes to deal with data transfer without knowledge of the exact access method used. The media access control sublayer arbitrates between users when they attempt to transfer data on the common communication media. Three access methods have been endorsed by the IEEE 802 Standards Committee. They are described in three documents that include physical specifications and media requirements: the 802.3 CSMA/CD method and physical layer specification; the 802.4 token bus access method and physical layer specification; and the 802.5 token ring access method and physical layer specification.

All three access methods have several common characteristics. First, data rates on the media fall within the 1 - to - 20 Mbit range. In addition, access control to the network is decentralized and a failure of one station will not render the network inoperable. Finally, robust error detection is implemented by a 32-bit frame check sequence included in all data frames.

The physical sublayer serves to connect the media access circuitry to the media being employed. The IEEE 802 standards are written to make the physical layer provide for the requirements of the media access protocol. The exact method of interconnection is transparent to the media access layer. As new media, such as fiber optic cable become available, new physical sublayer standards can be written to use the proven access methods. Thus, for example, the IEEE 802.3 standard specifies the CSMA/CD method. Supported only by a bus medium, the standard enables users to simultaneously hear all transmissions. All of the stations on the bus that have data to send wait until the media is not busy before attempting to transmit. After initiating a transmission, a station monitors the media in order to determine if another station began transmitting at the same time. Upon detecting a collision, all stations are required to cease transmission. Each station waits for an unequal amount of time before attempting retransmission.

Token bus, on the other hand, as defined in 802.4, uses a more deterministic approach to allow access to the media. A special data frame, called a "token," continually circulates among the stations on the bus. A station is allowed to send data only if it is the last station to receive the token frame (in effect it "holds" the token). Once a station has completed transmission of data frames, it passes the token to the next station.

The token ring access method (IEEE 802.5) is similar to the token bus method (IEEE 802.4) except that its order of token passing corresponds to a physical ring rather than one arranged by an address number. The protocol is optimized for the ring topology and differs significantly from that of token bus. Receipt of a token frame still controls the right to access the medium, but each station on the ring can only "hear" frames from one preceding station on the ring and can only send frames to its successor.



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that originate at the head-end and are broadcast to all users. This topology has resulted in IEEE 802.4 including specifications for a "remodulator" located at the head-end of the cable system to receive signals in one "upstream" channel and remodulate them to a channel in the "downstream" band.

The remodulator not only adds cost to broadband cable networks, it represents a potential single point of failure. Broadband cable network suppliers are well aware of this failure potential and have manual and automatic switches available to allow for backup of the network's remodulator.

The overriding cost trade-offs

The two primary costs associated with communication systems are the hardware costs for the backbone media hardware, and the cost of the communication node. Typically, total component costs for broadband cable TV systems are somewhat higher than for comparable baseband coaxial or shielded twisted-pair systems. This is particularly true in smaller cable installations where the additional cost of a head-end unit and amplifiers (if required) can be a significant percentage of the total system component cost. In larger systems however, the cost differential between the 802.3 baseband coaxial cable and the 802.4 broadband coaxial cable implementations becomes less significant. This is due to the higher per meter cost of the special 50-Ω coaxial cable, the higher cost of the special drop cables, and the higher cost of the active taps required in an 802.3 baseband system.

Media costs for shielded, twisted-pair cable systems are typically lower than costs for broadband and baseband coaxial cable. There is, however, an additional cost associated with the node bypass switching mechanism required in 802.5 token ring systems. (The switching mechanism is required to remove inoperative stations from the token ring.)

Installation costs for the three types of cable systems are comparable, although installing coaxial systems requires somewhat more specialized knowledge and may be more labor intensive. In addition, broadband installations normally require a preinstallation design which may add to the system cost.

Node costs for CSMA/CD and token bus systems typically stay within $500 to $1000 per connection. CSMA/CD nodes range from the lower to middle part of this range, while token-bus node costs occupy the middle to upper portion of this range.

The lower cost of CSMA/CD implementations, due to the maturity of both the access method and the 802.3 standard, has led to silicon implementations of the CSMA/CD protocol. This, in turn, has allowed many vendors to offer CSMA/CD-based products. The token bus, on the other hand, is relatively early in its maturity cycle, with only one company at present offering an 802.4-based product. A number of companies, however, have announced that they will soon be offering 802.4 products. Silicon implementation of the 802.4 token bus scheme are also under development. Vendors anticipate that the cost per connection for token bus-based products will follow an evolutionary path similar to that of CSMA/CD.

Growing needs of LANs

When a LAN is installed, the network manager should expect system requirements to change. It is therefore very important to understand the degree of flexibility offered by the different types of LANs. One of the key differences between baseband and broadband implementations, for example, is the large amount of bandwidth offered by broadband systems.

The broadband bandwidth is divided into discrete channels, each capable of carrying different information. Because of this division, a broadband system can support a variety of data channels (eg, token bus, CSMA/CD, and point-to-point systems), video channels, and voice channels all simultaneously. Baseband systems, by their very nature, support only a single channel. This is an important consideration when a LAN must support multiple applications or be ready to accommodate growth.

Another flexibility issue is the ease with which stations are added to the existing network. Adding stations to the bus topologies of 802.3 and 802.4 is easier than adding a station to an 802.5 ring architecture. Typically, adding a station to a broadband bus is simply a matter of attaching one end of a drop cable to an already existing tap on the trunk cable and the other end of the drop cable to the station.

In baseband 802.3 systems, the drop cable must be added to an existing trunk cable tap. If no tap exists, a cable piercing "vampire" tap can be added at one of the designated places along the cable. To add a station to an 802.5 ring topology, the cable system must be physically severed and the new station added, thus temporarily rendering the system inoperable. Depending on how the splicing method is implemented, the ring's operation could be disrupted for a period of time ranging from milliseconds to minutes.

Another consideration is the ease with which the media can be extended to include locations not originally intended for the LAN. Baseband systems have distance limitations that may prevent the LAN from reaching a new area. Broadband systems, on the other hand, can be designed to easily extend from a small local system to one that encompasses a metropolitan area.

One area of LAN communication systems that is gaining importance is the management of an

operational network. Performance monitoring tools on a network spot potential trouble areas before serious problems occur. Also, configurable parameters can be altered to optimize network throughput.

The IEEE 802 committee is at work on a station management specification that will result in a standard format to transfer status and configuration information for each media access method. This is being written for each media access method under guidelines set forth by IEEE 802.1 subcommittee.

A predictable, ordered access technique, such as token passing, is beneficial in that it readily lends itself to being managed and to providing information about how the system is functioning. Because each system error may be detected and resolved by a well-defined set of protocol rules, tracking and reporting the errors is easily implemented within each station.

The 802.4 and 802.5 token-passing methods have defined many configurable network parameters that can be used to change and optimize network performance for different applications. For example, 802.4 stations (whose access to the media is noncritical) can be configured to temporarily drop out of the token-passing logical ring when they do not have any data to send. This lets a network dynamically reconfigure itself to minimize token passing overhead for high priority users.

Regardless of the application, the implementation of the access method calls for configurable parameters that can be used to optimize system performance, to provide mechanisms to aid in diagnosing system problems, and to provide the flexibility to meet ever-changing system requirements. Another point to consider when determining the best LAN for a particular application is that the software above the 802 layers provides functions and features that could outweigh media access considerations in the decision making process. Although the higher layers can enhance the performance of a LAN, they cannot overcome absolute limitations imposed by the media access technique and the media used.

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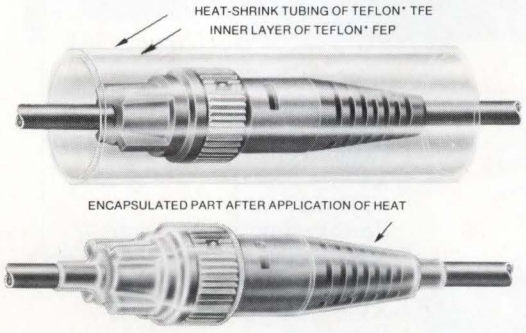

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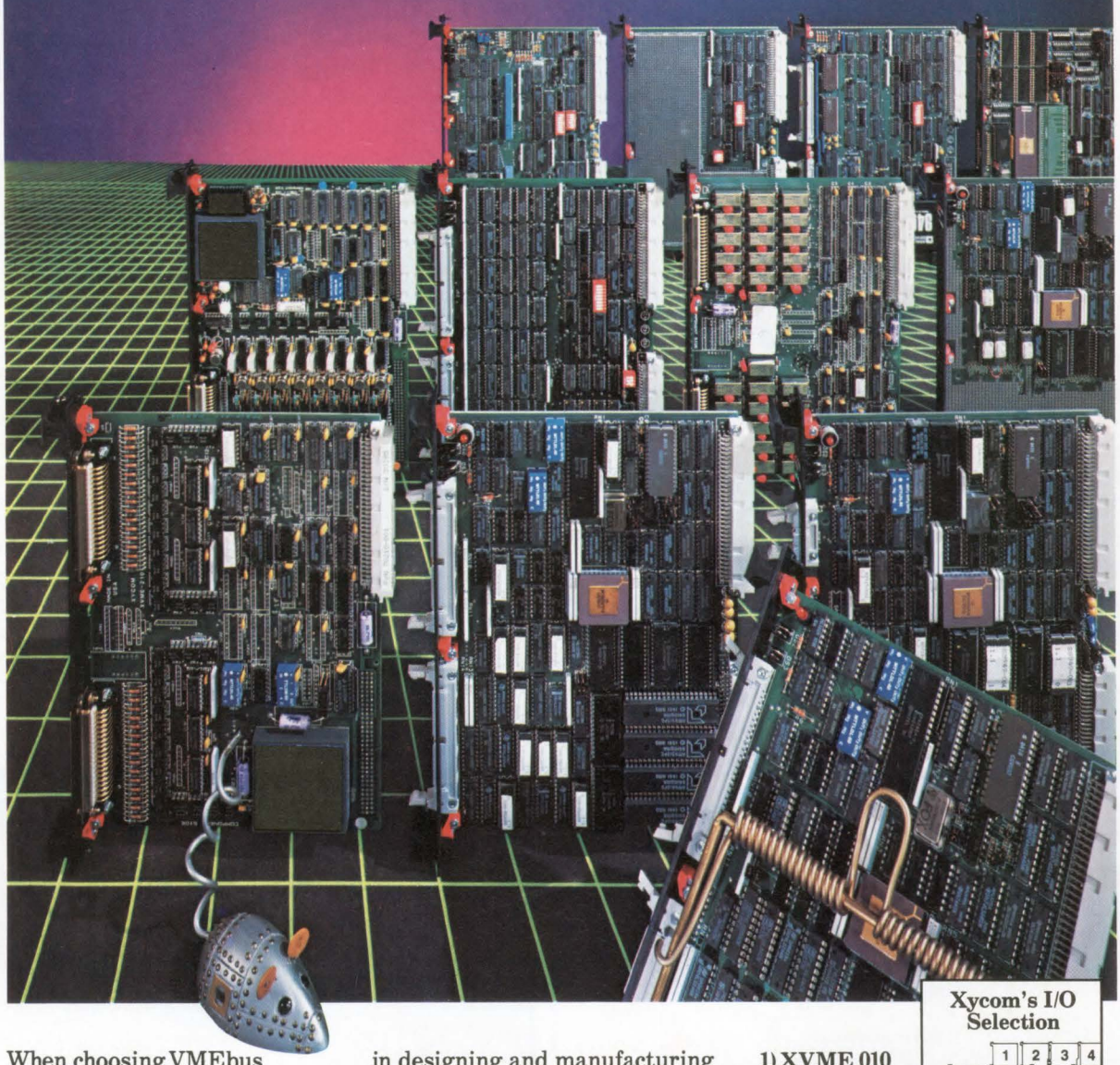

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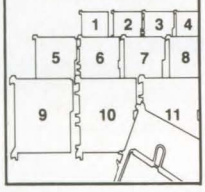

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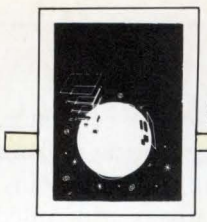


CONTROLLER IC CONTENDS WITH MULTIPLE PROTOCOLS

The most widely used data communication protocols are now supported by a single-chip controller that requires minimum external hardware.

by Jim Magill and George Wong

The need to transfer large amounts of data at high speed between several different local workstations and large computer systems has generated a variety of message transaction schemes or protocols. While several protocols have evolved, development of dedicated controller ICs to handle them has not kept pace.

Now a single-chip VLSI device, the SCN68562 Dual-Channel Universal Synchronous Communications Controller (DUSCC), incorporates circuitry for virtually all subsystems and functions required in advanced data communication systems. The chip provides interfacing to advanced DMA controllers and supports such interrupt structures as vectored, daisy chained, priority, and masked using minimum external logic. In many applications, the DMA and interrupt interfaces are implemented easily through direct connections from the DUSCC's request and acknowledge lines to the control bus.

The DUSCC's two independent data communications channels permit substantial programming flexibility for handling multiple protocols. Because of variations in bit- and character-oriented protocols, a controller must provide a more encompassing solution for high performance data communication systems. For example, when the transmitter/receivers can be operated either as full-duplex synchronous or asynchronous channels, the chip can embrace a broad range of advanced bit- and character-oriented protocols, including HDLC/ADCCP, SDLC, X.25, X.75 link level, IBM Bisync, DDCMP, and X.21.

Jim Magill is a marketing manager at Signetics Corp (Sunnyvale, Calif). He holds an MS in operations management from City University, London, England.

George Wong is a senior applications engineer at Signetics. He holds an MS in electrical engineering from the University of Kentucky.

An architectural overview

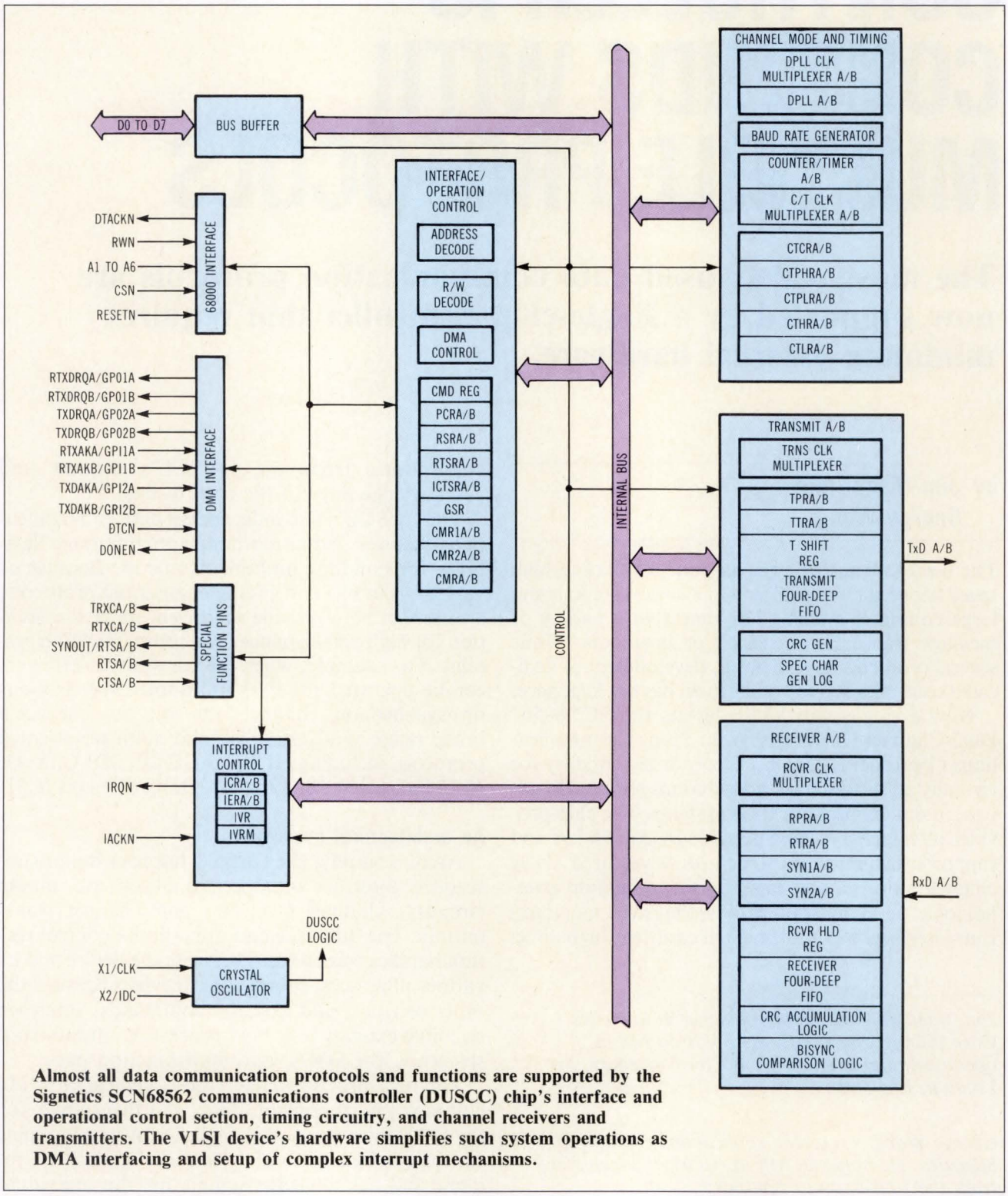
Architecturally, the DUSCC has four major subsections: interface and operational controls, timing circuitry, channel receivers, and channel transmitters. The interface and operational control section handles transactions between the device and its various interfaces, coordinates activities between the other sections, and executes commands. Interface circuitry extends to a host processor, an interrupt structure, the DMA, and multifunction pins.

The host processor interface is dedicated to the complete set of control, data, and bus signals for the 68000 microprocessor. Eight DMA interface pins can be configured to provide individual DMA request and acknowledge signals for the individual

transmitters and receivers. An additional control signal, DONE, provides flow control. For example, it can signify the completion of a message sequence and the termination of DMA operation.

A triple set of registers configures each channel. The channel-mode configuration pair (CMR1 and CMR2) selects the channel protocol/transmission mode, message format, and error-check sequence. The system interface and pin configuration register (PCR) selects the function of the multifunction pins.

Each channel's interrupt structure is controlled through the interrupt control (ICR) and interrupt enable (IER) registers. (The second diagram shows the interrelationship between these registers and the



Almost all data communication protocols and functions are supported by the Signetics SCN68562 communications controller (DUSCC) chip's interface and operational control section, timing circuitry, and channel receivers and transmitters. The VLSI device's hardware simplifies such system operations as DMA interfacing and setup of complex interrupt mechanisms.

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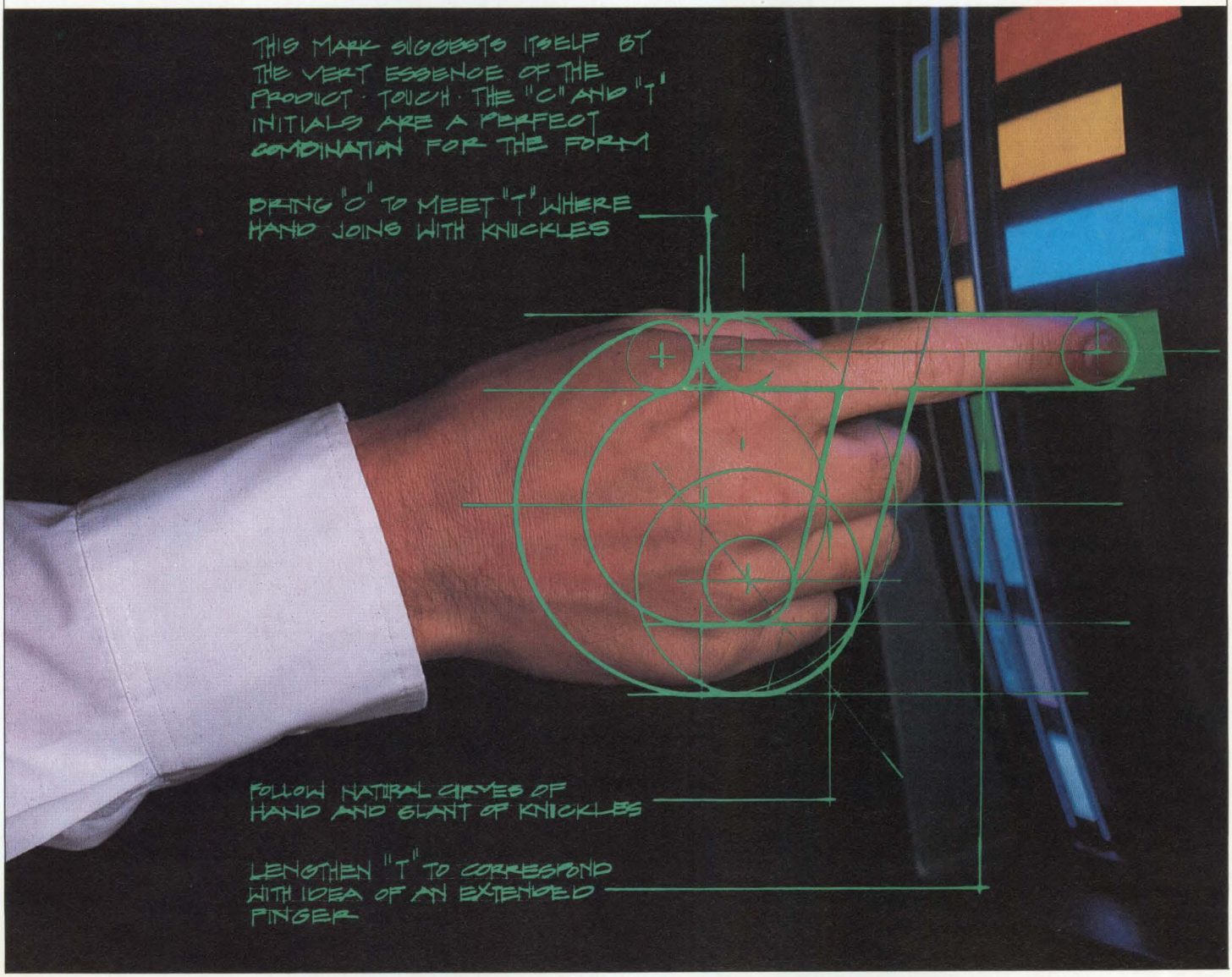

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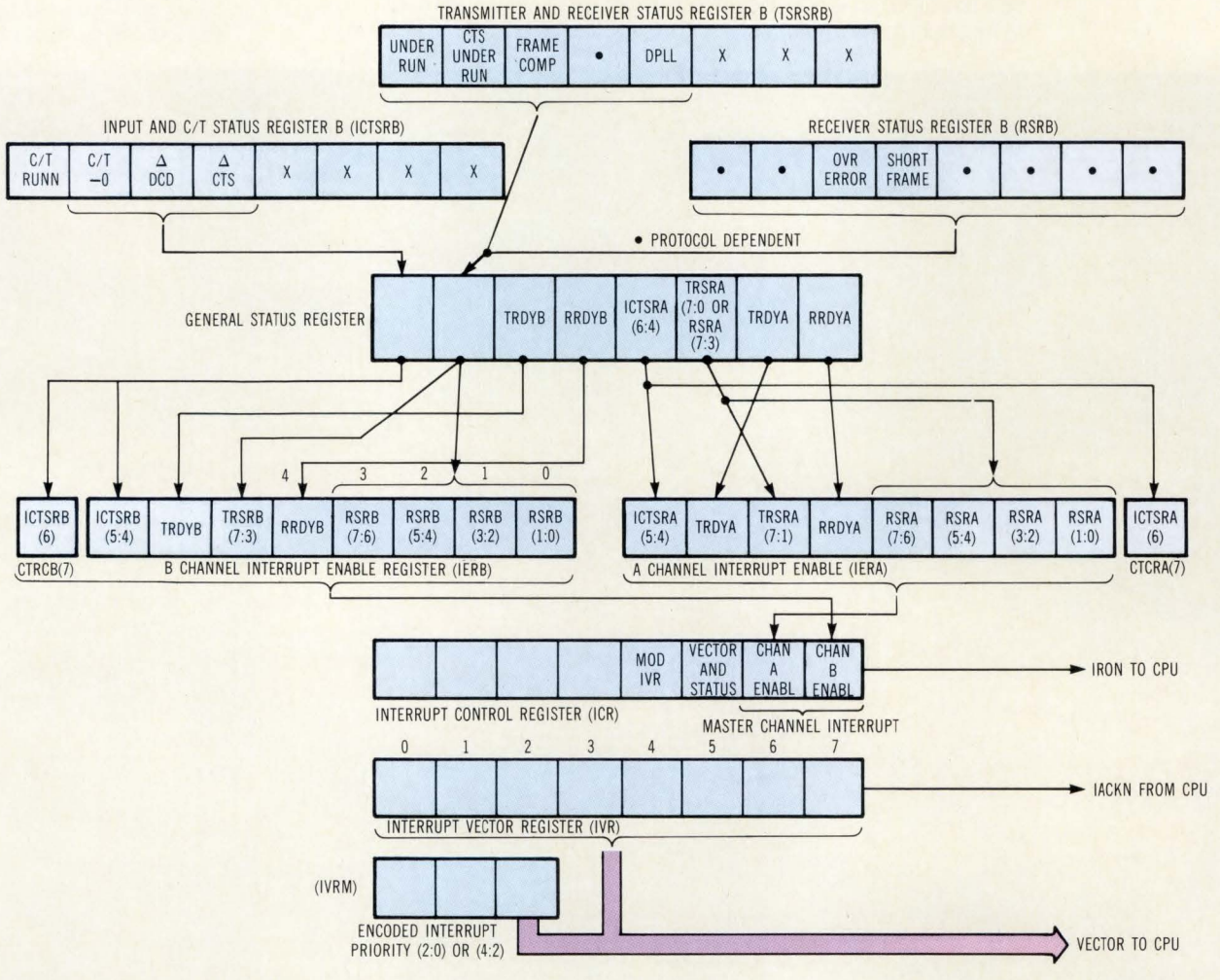
kinds of information stored.) Channels follow a fixed interrupt priority starting with receiver ready, transmitter ready, receiver or transmitter status condition, and finishing with external event or counter/timer ready. The relative priority of interrupts of one channel with respect to the other is selected through the ICR. These priority combinations are A before B, B before A, and alternating priority with either A or B as highest. Other bits in the ICR select vectored or nonvectored interrupt operation and vector format when the vectored mode is selected.

Interrupt masking can be performed either on individual groups or channel interrupt conditions using the IER, or on an entire channel under control of the ICR. In addition to handling interrupt request and acknowledge signals, the DUSCC provides a mechanism to create interrupt daisy chains using its X2/IDC pin to propagate the interrupt acknowledge signal. Most application timing functions can be derived from the DUSCC's internal timing circuitry. This section consists of independent 16-bit timer/counters and digital phase locked loop (DPLL) circuits for each channel, and a common crystal clock and baud rate generator. Clock signals for the transmitters and receivers can be selected from an external source or from one of the internal sources mentioned above.

The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2/IDC pins or from an external clock connected to the Xl/CLK pin. The oscillator's output provides the clock signal for the DUSCC's logic and other internal timing circuits.

The baud rate generator runs off the oscillator signal or on the external signal, generating 16 baud rates simultaneously. These signals are made available to



A variety of interrupt schemes including vectoring, daisy chaining, and masking can be set up through the DUSCC's interrupt control register (ICR) and interrupt enable register (IER). The ICR determines the relative interrupt priorities of one data communication channel with respect to the other. Channel interrupt conditions are enabled in the IER.

the receiver, transmitter, DPLL, and counter/timer. Since the 16 baud rates are available simultaneously, each receiver and transmitter can select its baud rate independently.

Each channel includes a DPLL that is used in synchronous modes to recover clock information from the received data stream. The DPLL contains a 6-bit counter that is incremented by sampling a clock signal at 32 times the nominal data rate. The clock source can be from an external input, the receiver baud rate, the counter/timer, or the crystal oscillator. The DPLL uses the sampling clock signal together with the received data to construct a data clock that can be used as the DUSCC receiver data clock, transmitter clock or both. This results in a DPLL square wave output clock at a data rate that can be programmed to be sent out on a special pin. Users can select NRZ/NRZI, FM0, FM1, or Manchester as the encoding format of the received data.

Transmitter/receiver flexibility

Dedicated hardware is integrated within the transmitter and receiver circuits to generate and detect special character sequences, to generate various error sequences and to handle many of the overhead tasks associated with advanced message formats. The large number of operational registers for each channel and the concise set of control commands allow easy setup and operation of the DUSCC.

Each transmitter channel consists of three major sections: clock multiplexer and control registers; first in, first out and shift register; and special character generation logic. After a channel is configured for a protocol/transmission mode, transmitter operation is refined by the contents of the transmitter parameter register (TPR) and the transmitter timing register (TTR).

The transmitter's clock source is selected from inputs to the transmitter-clock multiplexer. Inputs are the channel counter/timer, the other channel's counter/timer, baud rate generator, DPLL, or an external clock signal. The TPR selects the clock source and baud rate if the baud rate generator is chosen as the transmitter clock signal.

The transmitter accepts parallel character data from the data bus and loads the data into the transmitter FIFO register (TxFIFO), which consists of four 8-bit holding registers. Data is then moved to the transmitter shift register (TxSR), which serializes it according to the transmission format. The TxSR can also be loaded from special character logic or from the cyclic redundancy check/longitudinal redundancy check.

The transmitter-ready signal, TxRDY, indicates the status of the TxFIFO and is set either when an empty position exists in the FIFO or if the entire FIFO is empty. The user can choose the frequency of service requests because the DMA and interrupt service request follow the state of TxRDY.

The receiver architecture is basically similar to that of the transmitter. The receiver consists of a clock multiplexer and control registers, FIFO and shift register, receiver data path, and error accumulation logic. After a channel is configured for the transmission mode, receiver operation is refined by the contents of the receiver parameter register (RPR) and receiver timing register (RTR). The RPR selects the number of bits per character and controls operation of an external enable control line for all receiver transmission modes. The interpretation of the remaining bits in the RPR depends on the transmission mode selected.

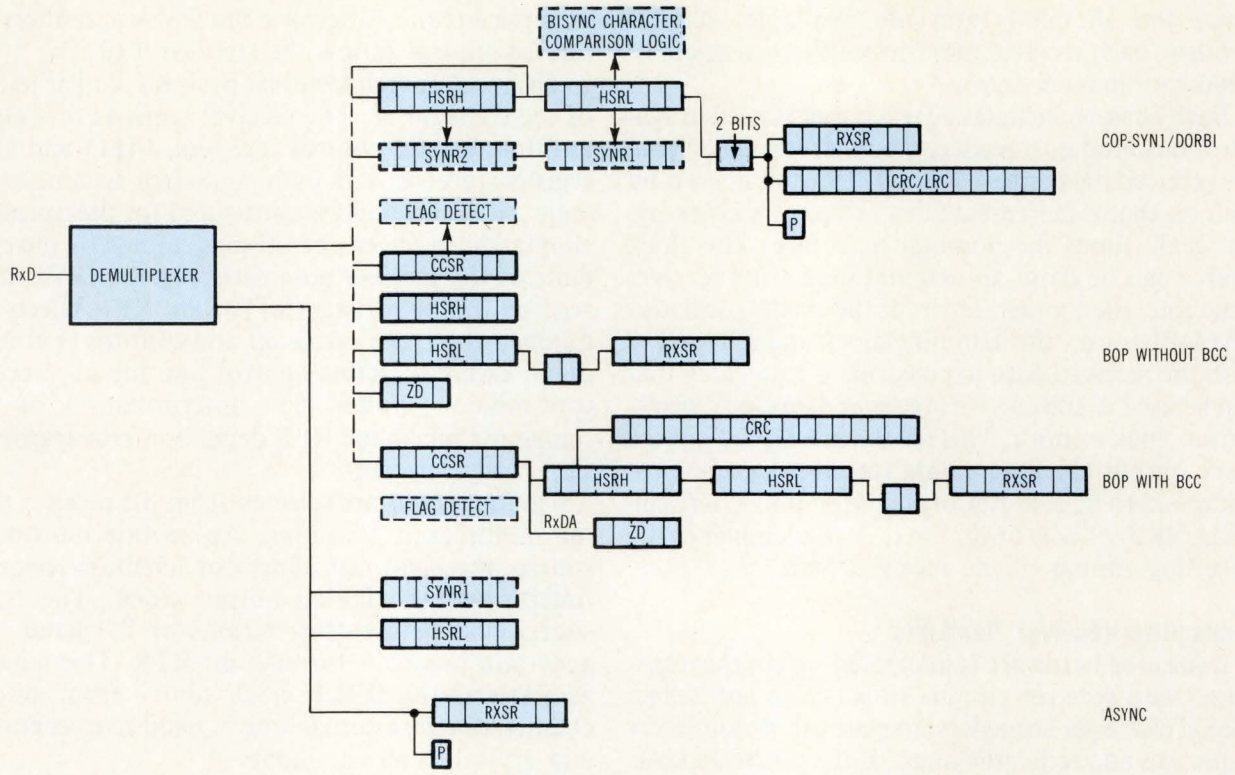
Timing signals are selected from the receiver timing multiplexer. Its inputs are an external timing source, the baud rate generator, channel counter/timers, and the DPLL output clock. The clock source and data rate selections of the baud rate generator are made through the RTR. This register also selects the DPLL clock source from among counter/timers, external source, baud rate generator, and crystal oscillator inputs.

No single data path can support the diverse requirements of the various transmission modes efficiently. Thus, the DUSCC data path can be viewed as four separate paths—an asynchronous path and three paths to support the requirements of different protocols. Each data path is responsible for assembling characters into the receiver shift receiver (RxSR). After assembly, characters are sent to the receiver FIFO along with appropriate status information.

The receiver FIFO consists of four 8-bit holding registers with appended status bits. Data is loaded into the FIFO after a character is assembled; data is removed when a character is read. The state of the receiver FIFO (RxFIFO) is indicated by the receiver ready status signal (RxRDY). As in the operation of the transmitter, a user can choose when the RxRDY bit is set.

Down the data paths

The asynchronous path of the DUSCC is comprised of the holding register (HSRL) and the RxSR in parallel. The HSRL path is active only if a character comparison option is selected. In this case, all incoming data is matched against the contents of the SYN1 register on a bit-by-bit basis to determine a character match. If a match is obtained, a flag in the receiver-status register is set. This feature can be used to generate an interrupt. If the character comparison option is not selected, character data is shifted only to the RxSR. After a character is assembled in the RxSR, it is loaded into the RxFIFO.



To support the requirements of various protocols, the DUSCC provides a number of internal data paths. One path is asynchronous—the holding register (HSRL) in parallel with receiver shift register (RxSR) configuration at the bottom of the figure—while the other three paths are synchronous. Synchronous paths are used for the bit-oriented protocol (BOP) without CRC, BOP with CRC, and the character-oriented protocol (COP) including Bisync data communication protocols.

Synchronous data paths can be pictured as one of three parallel paths that become active in the following channel conditions: a character-oriented protocol (COP) with or without a block-check character (BCC); a bit-oriented protocol (BOP) without BCC and BOP with BCC. The COP path contains the two 8-bit holding registers (HSRH and HSRL) in series with the shift register, CRC accumulation logic, two synchronizing flipflops, and special Bisync comparison logic. Data entering this path is held first in either or both of the holding registers. During each bit time, data in the register (or registers) is compared against the contents of either the SYN1 register or the SYN1 and SYN2 registers. Comparison depends on the synchronizing pattern chosen—whether the pattern uses single or dual SYN characters. A match is indicated by the setting of a status bit in the receiver status register (RSR).

The BOP without a BCC path uses three parallel inputs to the character comparison (CCSR), HSRH, and HSRL registers, in series with the receiver register. In this arrangement, data is shifted into the three registers simultaneously. The holding pair of shift registers compares their contents with the SYN1 and SYN2 registers to determine if the correct station address has been received. All data entering this path is compared in the CCSR for the flag sequence. When a match occurs, the status bit in the RSR is set. Data entering the HSRL is assembled in character form in the RxSR and then transferred to the FIFO. Zero deletion occurs on all data received unless a flag or abort is detected.

In the case of the BOP with BCC data path, the CCSR, the holding registers, and the RxSR, are arranged in series. The CCSR remains active throughout a message frame and compares the incoming bit stream to determine the flag sequence. The address is compared using the 16-bit holding registers. As character data bits are shifted from the CCSR to the holding register pair, they generate the received BCC character according to the selected accumulation format of the CRC/LRC logic.

In Bisync mode, special comparison logic checks for control sequences and is active for both normal and transparent operation. Comparisons can be made either with EBCDIC or ASCII text messages as selected in the channel mode register. When detected, these sequences cause either a status bit in

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the RSR to be set or initiate special processing. This comparison logic makes the DUSCC a powerful tool for processing Bisync text. It frees the processor from searching for these special sequences and eliminates the need for additional processing associated with such sequences.

Minimum of hardware

An advanced two-channel data communication system can be implemented with the DUSCC. (The Table depicts the specifications for a typical data communication system supporting the different protocols.) Because so much of the hardware is already in the device, few additional parts are required.

Since the DUSCC provides separate DMA request and acknowledge signals for the transmitter and receiver, the full-duplex requirement for channel A is satisfied with a minimum of hardware between the DMA controllers and the DUSCC.

The complex vectored interrupt scheme for channel B is established by programming the interrupt control register for vectored interrupts and their formats. Separate interrupt vectors can be generated for the transmitter, receiver, and counter/timer by selecting bits in the interrupt control register. An interrupt masking can be performed through the interrupt-enable register. The interrupt interface involves simply connecting the interrupt request and acknowledge signals to the appropriate control bus signals. No additional hardware is necessary to complete this portion of the design.

A minimum of design is required to select the various interfaces for both channels. For channel A, five registers are used to select the channel interfaces and to set up the protocol requirements. Channel-configuration registers CMR1 and CMR2 establish the DMA structure and define operation of the data channel. External inputs are defined by the pin-control register and the address of the secondary station is stored in the SYN1 and SYN2 registers. Channel B is set up just as easily. But it requires additional programming of the interrupt control and enable registers to establish the interrupt structure.

Operating refinements for each channel are made through the transmitter and receiver parameter registers (TPR and RTR). These define the message format and select automatic features that are invoked under various transmitter and receiver conditions. The channel A transmitter, for example, is set up to terminate the BOP message automatically by sending an end of message sequence and then mark the data line when an underrun occurs. In similar fashion, channel B is set up to linefill with a sync pattern until another character is loaded into the transmitter when an underrun occurs. These actions do not require the intervention of the host processor.

Advanced Dual-channel DMA

	Channel A	Channel B
System interface	Full-duplex DMA	Vector interrupt Separate vectors channel, Transmit/receiver, end of message characters, and mask off all other conditions
	Tx req on FIFO empty	Tx req on FIFO not full
	Rx req on FIFO full	Rx req on FIFP not empty
Tx clock	Ext clock	Ext clock
Rx clock	DPLL-Manchester encoded internal sampling clock	Ext clock
Protocol	Bit-oriented protocol—secondary address CRC CCITT preset to 0's single control byte	Bisync CRC-16 preset to 1's

Once the interfaces are established, transmitter and receiver operations are controlled and monitored through the command and the transmitter/receiver status registers. The DUSCC provides a set of commands that directly supports transmission of Bisync and BOP messages. Each command performs an action necessary to generate a message in the specific protocol. In Bisync, the first character of a message after the SYN pattern is an SOH, STX, or DLE-STX pattern. The send-DLE command not only sends the DLE-STX sequence, but the command can be appended to any character to transmit special control sequences as the protocol requires.

In BOP mode, the message frame after the flag character consists of 0 to n address bytes, followed by 1 or 2 control bytes. The sequence is transmitted by loading the data into the transmitter FIFO. After the last control byte, the transmitter switches automatically to the programmed character length. A feature of the transmitter is its ability to send the last character for a bit count less than the programmed character length by specifying a shorter character length in the output/miscellaneous register.

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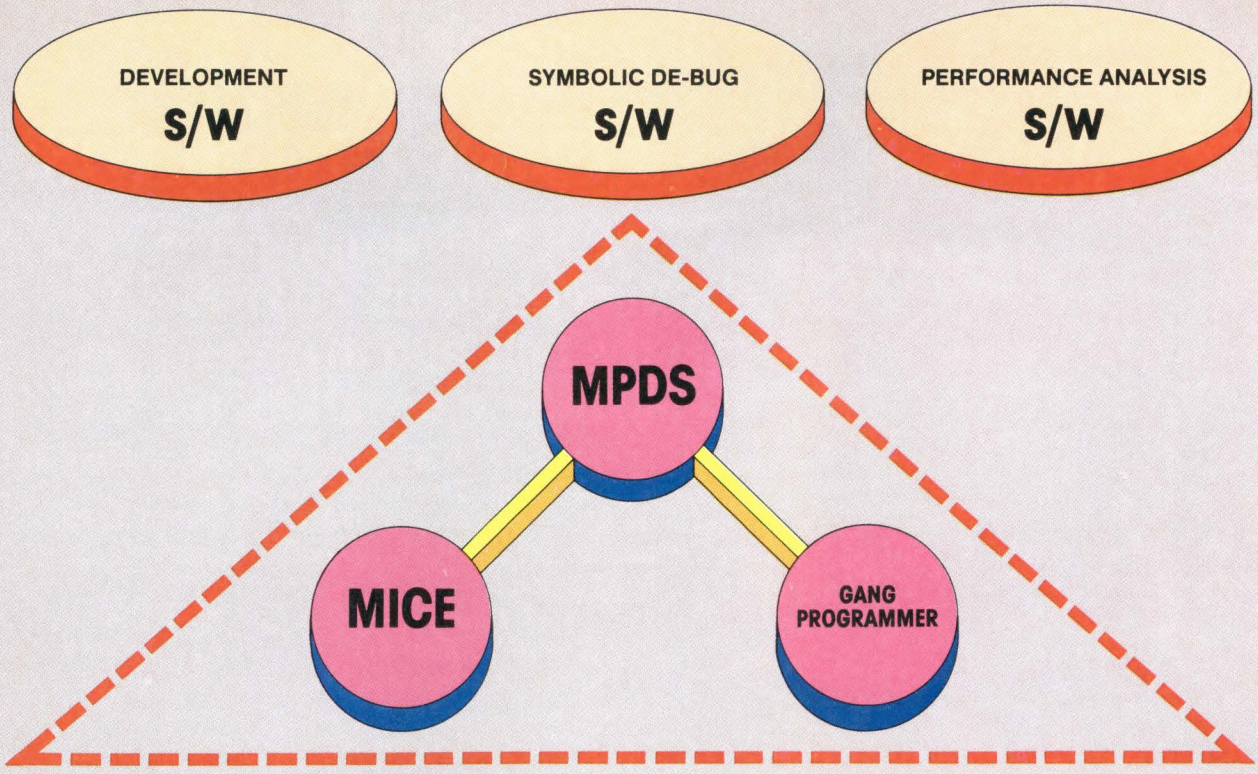

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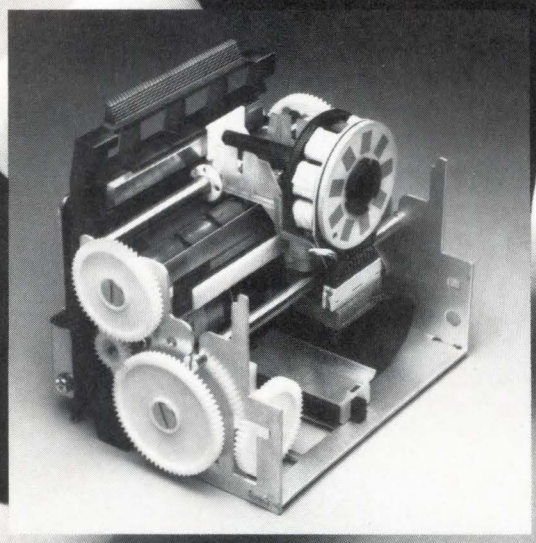

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BUILDING BLOCKS STACK UP TO HIGH PERFORMANCE

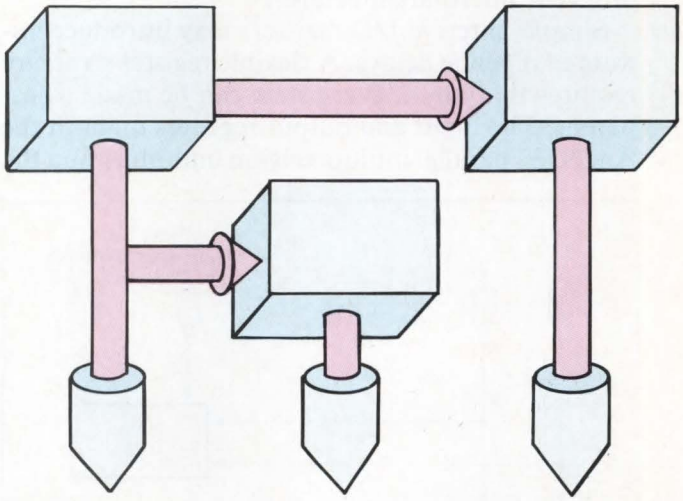
Designed using concepts of functional partitioning, three-bus architecture, and fault detection, a family of 32-bit building blocks can satisfy the needs of both general-purpose computing and signal processing.

by Timothy J. Flaherty

As processing rates, machine densities, and system reliability requirements increase, functional integration at the device level becomes mandatory in high performance controllers and processors. When used as standalone devices or combined in a high speed system, functional building blocks can provide solutions to a wide range of design problems. They fit equally well into a general-purpose computer and a digital signal processor, despite the great functional differences between these two systems.

As device densities have increased over the years, system word widths have grown, bringing greater precision and allowing a larger memory space to be addressed. The jumps from 4- to 8-bit and from 8- to 16-bit systems occurred relatively quickly. The leap to 32-bit systems has already taken place, bringing with it a slowdown in the quest for wider system words. Partitioned into 32-bit building blocks, Advanced Micro Devices' Am29300 family integrates functions that are difficult, if not impossible to implement with bit-slice devices. These functions include barrel shifting, priority encoding, and mask generation.

Whenever carry-lookahead logic can be contained in the same device as the arithmetic logic it supports, cycle time is improved. In fact, by reducing the amount of intrafunction communication across chip boundaries, cycle time no longer has to depend on the speed of the interface between components. Because of this, all intrafunction communications were eliminated in the Am29300 family. Pipelining can result in the faster execution of certain highly repetitive operations, but system latency increases. In some cases, this latency will actually degrade throughput. In a recursive algorithm, where a calculation depends on the immediately preceding result, true throughput can be lost while waiting for intermediate results to work their way through the pipe. To maximize performance without sacrificing architectural flexibility, intrafunction pipelining was also eliminated in the Am29300 devices.



A three-bus, flow-through architecture complements functional partitioning in this chip family.

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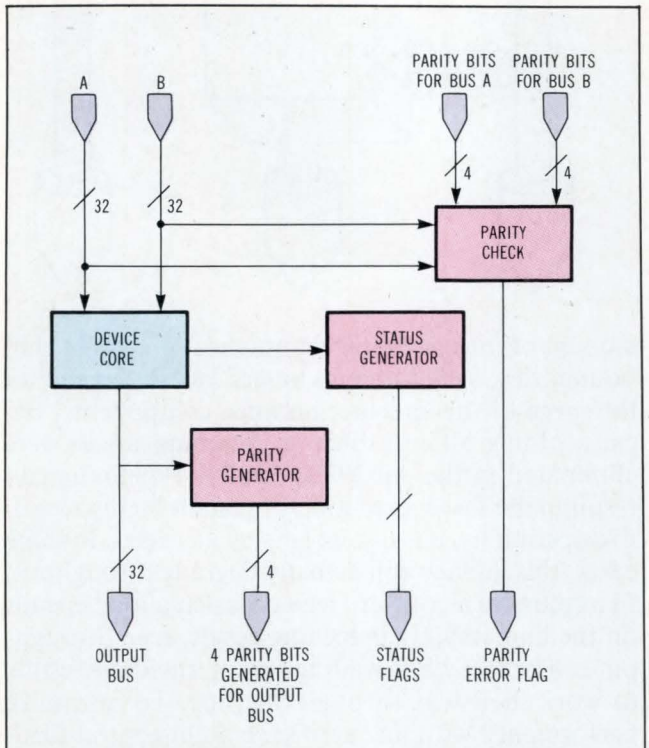
The data path members share a common bus configuration with two input operand buses and one output bus. Independent of each other (neither bidirectional nor shared), these buses provide maximum accessibility.

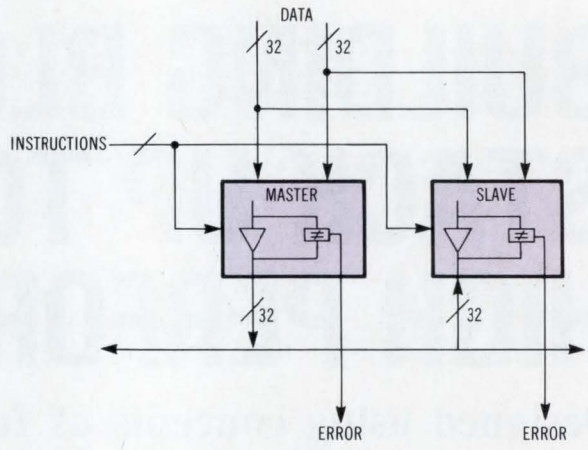
Bidirectional or shared I/O buses limit the speed at which information can be transferred between different parts in the system. Achieving rapid turnaround of bidirectional TTL data buses is often an arduous task. And shared input buses require greater timing restrictions than do nonshared buses. These limitations have been eliminated in the Am29300 data path devices by removal of shared or bidirectional buses.

A high data transfer bandwidth is achieved with the flow-through architecture. This direct access allows the designer to tailor the system's register file to the specific application rather than forcing use of a fixed, more general memory organization. The beauty of the three-bus architecture lies in its simplicity. This straightforward structure permits many possible component configurations optimized for different micro-architectures.

Simple, internal I/O registers may introduce unwanted pipeline delays. A flexible register structure requires that any I/O registers can be made transparent. The input and output registers on both the Am29323 parallel multiprecision multiplier and the Am29325 floating point processor can be made transparent independently, providing a number of different register configurations including flow-through.



The three-bus, flow-through architecture affords the greatest access to the device cores. Byte-parity checking detects connection failures between devices.



Master/slave checking provides device failure detection using redundant parallel devices. This happens without incurring the delay of a "voting" scheme often used in high reliability designs.

Fault detection

The philosophy governing this chip family is maximum functionality with minimum impact on system cycle time. The methods used for fault detection put this idea into practice.

The 32-bit family addresses fault detection at the component level using a twofold scheme—byte parity and master/slave checking. To detect interconnection failures, byte parity is both generated and checked by the data path elements of the family. The byte parity circuitry checks for single bit failures across each byte of the two input operands. Even parity checking was chosen for this family of TTL-compatible parts instead of odd parity to provide the additional check for bus failure. Any parity faults detected cause assertion of the parity error (PARERR) flag.

Master/slave checking detects failures at the device level. When using this mode, two devices are operated in parallel, each receiving the same data and instructions. The master device generates its result and transfers this information to the output bus. The slave device generates its own result from the same inputs; instead of delivering this data, however, the slave reads the output bus and compares the master's results with its own. The hard error (HARDERR) flag indicates any discrepancies between the two outputs. Moreover, the assertion level of both the parity and hard error flags indicates device failure due to loss of power and error signal faults.

Both error checking schemes operate on a cycle-by-cycle basis so any detected fault triggers an interrupt at the microinstruction level. Unlike other redundant schemes, specialized software is not required, and system performance is not affected by the communication between redundant functional units.

Cycle time and control paths

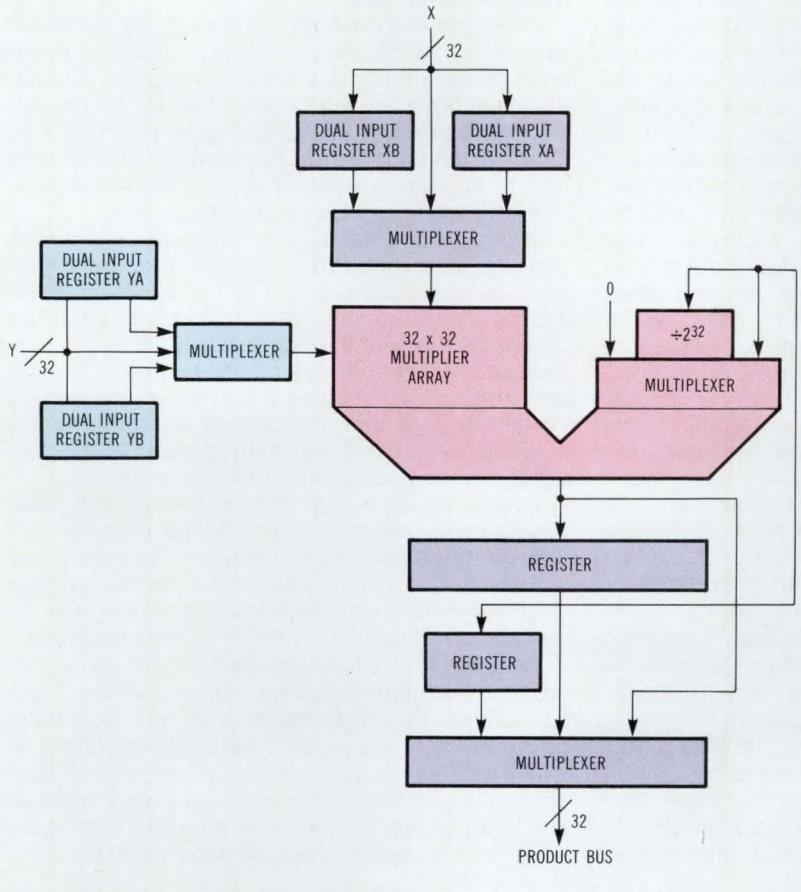
In high performance system design, the system's intended operations must be given, with careful consideration paid to required cycle time. The cycle time depends on the type of operation the system performs. The design should be optimized for quick execution of the instructions that make up the largest percentage of the system's operations.

Complex operations requiring long cycle times, but used infrequently, should be performed over multiple cycles. For example, a complicated arithmetic procedure such as division should not determine the cycle time of the system if the operation only used a small portion of the time. On the other hand, if this operation is used frequently, the system should be made to handle it efficiently.

Comparing the instruction mixes of a general-purpose processor and a dedicated array processor illustrates this point well. Multiplication operations dominate the array processor's instruction set, while the general-purpose machine's set would be less multiplication intensive. The Am29323 parallel multiplier would enhance an array processor by providing a high speed, single cycle 32- x 32-bit multiplication. The general-purpose machine might not need a dedicated multiplier and could fare well with the Am29332 ALU chip and its multiple cycle multiplication capability.

When optimizing the system for speed, a designer should remember the control path. By causing a change in the normal flow of information in the control path, conditional branching often becomes the system bottleneck. Conditional codes must be checked to determine the next address, but this checking can extend the cycle time. The speed of the control path must remain on a par with the speed of the data path. The Am29331 microprogram sequencer architecture balances the timing between the control and data paths.

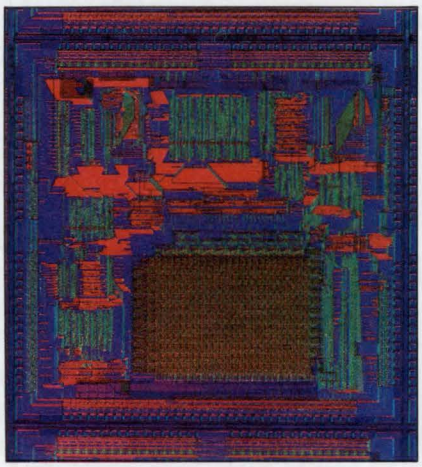
By integrating the conditional code multiplexer, test logic, and polarity control logic in the same device, cycle time is reduced by eliminating intrafunction delays. The microprogram sequencer can perform four sets of 16-way branches upon the simultaneous



The 32- x 32-bit parallel multiprecision multiplier provides dual input registers to support extended multiplications. An internal wrap-back path and shifter eliminate transferring data offchip for shifting.

A family gathering

A member of the Am29300 family, the Am29332 32-bit noncascadable ALU chip, was designed for systems requiring fast number crunching, high data transfer rates, and powerful bit-manipulation capabilities. The internal data path of the ALU chip interconnects several functional blocks. These blocks include a mask generator, a funnel shifter, an ALU, and a priority encoder. The ALU chip allows operations that once took multiple cycles to be executed in a single cycle.



The ALU chip uses a 64- to 32-bit funnel shifter to perform a full complement of N-bit shifts, N-bit rotates, field extractions, and field logical operations in a single cycle. This funnel shifter works on either one or both input operands. Such shifting is extremely useful in such operations as floating point mantissa normalization or denormalization, and in applications where packing and unpacking of data is a frequent task. Also, the ability to extract a 32-bit contiguous field from two operands provides a useful function in many graphics-related operations. The output of the funnel shifter is directed to the R input of the ALU, allowing logical operations to then be performed on the shifted word. The ALU section of the Am29332 has three input ports. One input comes from the funnel shifter, another from the mask generator, and a third can be selected from various sources including both input buses. This three-input ALU allows merger of two instructions into a single cycle.

The Am29325, a single-precision floating point processor, integrates a fully combinatorial 32-bit floating point adder/subtractor, multiplier, and data path in a single chip. This integration minimizes processing overhead. The floating point processor supports both IEEE P754 and Digital Equipment Corp floating point formats. All instruction—addition, subtraction, multiplication, floating point/integer conversions, and IEEE/DEC conversions—are performed in a single clock cycle. There are no internal pipeline delays to limit true throughput.

The core of the floating point processor is a 3-port arithmetic unit containing a mantissa processor, an exponent processor, and additional logic required to implement floating point operations.

The Am29323 is a 32- x 32-bit parallel multiplier with multiprecision capabilities designed to perform a 32- x 32-bit multiplication in a single cycle. The parallel multiplier also supports multiple cycle, multiprecision multiplications. Using a 67-bit onboard accumulator and internal wrap-back paths, this device can perform a 64- x 64-bit multiplication every four cycles. This part also supports 96- x 96-bit and 128- x 128-bit multiplications. These expanded multiplications offer support to extended and double-precision format floating point multiplications.

To provide a flexible interface for a variety of applications, the parallel multiplier has dual 32-bit registers on each input bus. Both halves of a 64-bit input word can be loaded, stored, and selected as needed when extended multiplications are performed. The input registers can be made transparent and the outputs can be selected directly from the array core to provide a high speed multiplier accelerator in a system designed with the other members of the Am29300 family.

The task of reducing cycle time in a microprogrammed system—a primary goal for the Am29300 family—is assisted by the Am29331 program sequencer. The critical path in the control section of a system typically passes through the status register through test logic, test multiplexer, sequencer, and microprogram memory. The microprogram sequencer removes the "control bottleneck" by integrating the test logic, multiplexer, and sequencer.

Handling interrupts

Interrupts and polling both handle asynchronous events. But in interrupts, unlike in polling, explicit tests in the microcode are not required. Quicker response times and less microcode are the reasons the microprogram sequencer uses interrupt handling. When an interrupt is received, the interrupt return address is pushed on an internal 33-level stack allowing nested interrupts.

Interrupts are handled by the sequencer at the end of a microcycle. Traps, on the other hand, must be handled before the end of the microcycle. Because they indicate an unexpected condition caused by the current microinstruction, traps cause the sequencer to halt the operation before the current instruction changes the state of the system. When a trap occurs, the current microinstruction must be aborted and re-executed after the trap handling routine has taken corrective measures.

The Am29334, a high speed, 64- x 18-bit, dual-access RAM, provides the Am29300 family with flexible, configurable memory. The device's dual read/write ports allow simultaneous access for two operations every cycle: two operand fetches, a read and write to two locations, or two write operations.

Because it can be expanded in both width and depth, the register file allows several memory configurations. Two of these devices may be hooked together in an expanded 6-port configuration, for example. This setup allows two processors to operate on the same memory simultaneously. Four reads and two writes every cycle could provide high speed local memory, possibly configured as a cache.

occurrence of four external test conditions. This ability to handle multiway branching greatly reduces the branching delay penalty.

Data routing

A system should be able to route data punctually to the proper location—a task as important as reducing cycle time. Cycles wasted while waiting for results to work their way out of the pipeline and into the arithmetic unit where they are needed degrade performance. Bus bandwidth is lost by the redundant transferring of intermediate results back and forth from memory. And cycles lost shuffling data reduce true throughput.

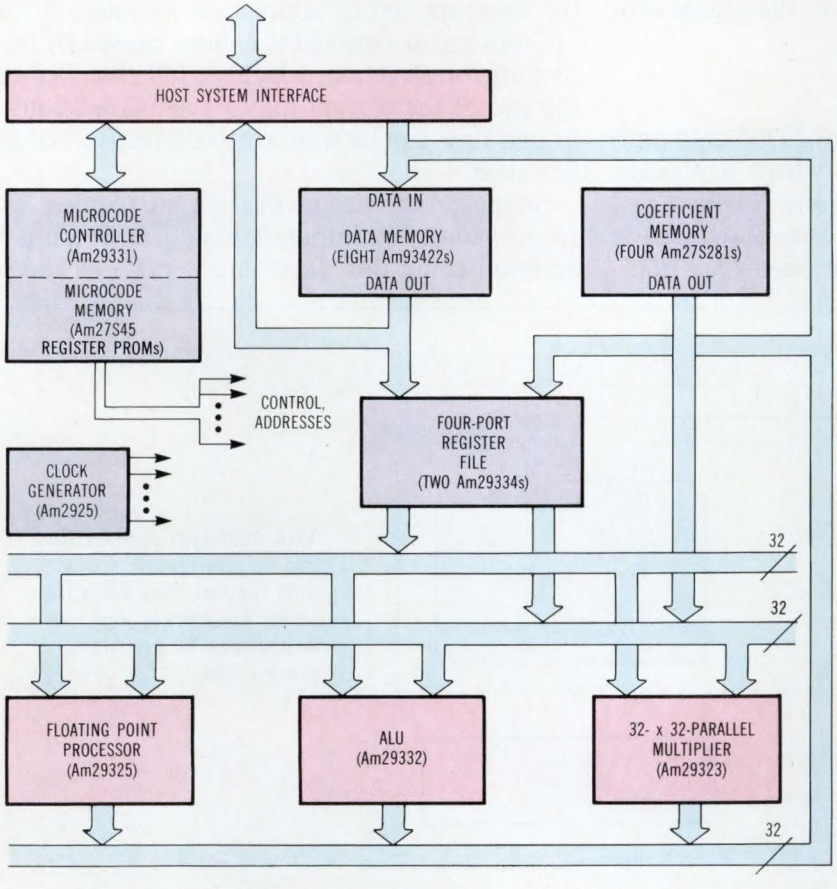
Often data is fetched from one memory location, processed, and the result of the operation returned to the original memory location. The Am29334 register file supports these read/modify/write operations by allowing a single cycle read and write memory operation to the same location. The register file's internal circuitry makes this operation possible without requiring external hardware to store the modified data temporarily.

Maximum bus bandwidth requires operands to be in the right place at the right time without monopolizing the bus structure. Redundant data transfers, such as returning intermediate sums from a sum-of-products operation to memory, only congest the bus structure and reduce bandwidth. The Am29325 floating point processor provides internal wrap-back paths and handles such data routing onchip. These internal wrap-back paths for sum-of-products operations with intermediate results double the bandwidth of a bus shared between multiple processors.

The Am29323 parallel multiplier also provides internal wrap-back paths and shifting circuitry for extended multiplications. These elements eliminate the delays resulting from data leaving the chip, being adjusted by an external shifter, and then returning to the device. The parallel multiplier has dual 32-bit input registers to support the cross-products needed for multiprecision multiplications. These registers also reduce bus congestion by eliminating the need for redundant memory fetches.

System bus structures

A general-purpose CPU falls short of today's number crunching requirements because it cannot take advantage of highly structured array and digital signal processing algorithms. The differences



A 32-bit floating point/ integer processor can be designed using a parallel configuration. In the system shown, the floating point processor shares three 32-bit buses with the ALU chip and the parallel multiplier.

between a general-purpose CPU design and an array processor design allow optimization of the configurations to serve specific needs.

Different system designs often have different data bus requirements. Parallel configurations are useful and easily implemented. In a general-purpose machine, for example, several processing units might share the same data buses. The Am29332 ALU chip can share three 32-bit buses with the parallel multiplier and the floating point processor. Data could be passed from one processor to another through the shared register file.

Although parallel configurations fit a general-purpose design, specific processors may require different bus structures. With a dedicated bus structure and paired Am29331 RAMs configured as a 6-port register file, for example, a high speed system that is well-suited for matrix processing can be designed. For array processing this arrangement offers a distinct advantage over the shared bus system.

To perform a multiplication/accumulation, the Am29323 multiplies two 32-bit numbers, the product is passed through the register file and added to the previous product by the ALU chip. Performing the multiplication and the addition in parallel, results in an effective throughput of one multiplication/accumulation per clock cycle—twice that of the system with shared buses.

Status generation

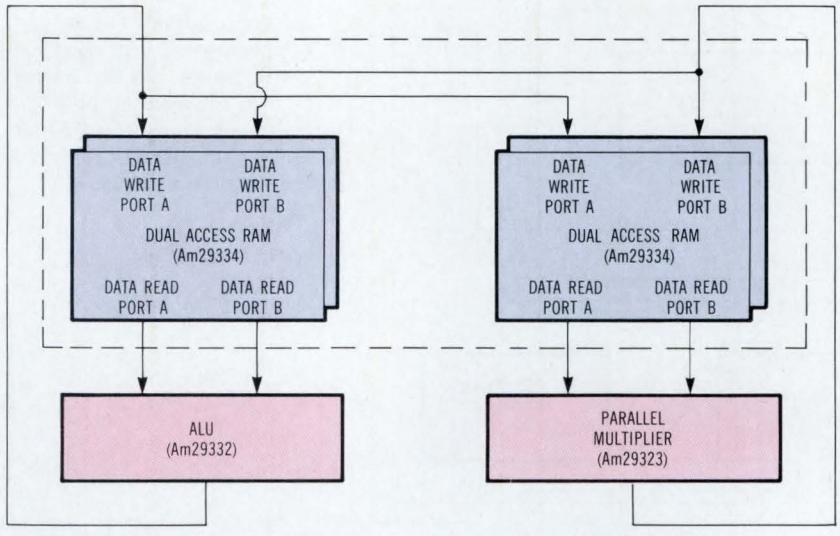
The status flag generators on Am29300 data path devices create flags that indicate where significant events occur during the calculations. These flags, generated as the operation is performed, reduce the processing overhead. The fully decoded flags minimize the amount of hardware needed for status interpretation. Such special conditions as a zero result or a byte carry may provide the user with important information about the calculation. A zero result—reported via the ZERO flag—is useful in comparison operations, for example.

Many of the status flags report such exception conditions as underflow, overflow, and invalid. Each of these conditions would indicate that the result obtained is not correct. These flags are active whether or not the output bus is enabled. In this way, the status of such iterative operations as floating point multiplication/accumulation can be monitored without enabling the output bus to check each intermediate calculation for exception conditions. This will reduce both hardware requirements and bus congestion.

Many of the conditions reported by the status flags indicate a problem with the current operation. The INVALID flag on the floating point processor, for example, indicates an invalid operation has been attempted. This flag can be used to generate an interrupt. The microprogram sequencer handles this interrupt at the microprogram level. After accepting the interrupt, the sequencer allows an external interrupt handling address to gain access to the microprogram address bus. This address begins the interrupt handling routine. The microprogram sequencer saves the interrupt return address on an internal stack.

Traps are unexpected situations caused by the current microinstruction, which must be handled before the end of the current microcycle. Conditions such as overflow can be trapped so corrective action can be taken.

Suppose the current instruction requires a read from memory locations A and B, a floating point addition using this data, and a write of the result



Two dual-port register files can be configured as a six-port register file. With this setup, four reads and two writes may be performed every cycle.

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back into location A. If this addition operation results in an overflow and the result is written back into location A, information may be lost. This may happen if the OVERFLOW flag is used to generate an interrupt. A trapping setup, however, offers a different scenario.

If the OVERFLOW flag is used to indicate a trap, the operation can be interrupted before the overflow result can be written over the data in memory location A. An overflow trap handling routine scales both operands. Upon re-execution of the addition operation, the result does not overflow. The microprogram sequencer pushes the address of the current microinstruction onto its internal stack and allows the trap handling address to gain access to the microprogram address bus. After completion of the trap handling routine, the trapped instruction address is popped from the stack and re-executed.

Multiway branching

The Am29331 address sequencer's multiway branch instructions allow the selection of 16 consecutive addresses as a branch target. Generated in a single cycle, the address consists of the upper 12 bits from the D bus concatenated with 4 bits from the multiway inputs. This type of branching allows the testing of up to four conditions in a single clock cycle.

Four multiway sets of 4 bits each allow designers to group test conditions according to type. The 2 least significant bits of the D bus, D0 and D1, control which 4-bit multiway is selected.

The multiway-branch feature provides designers with a hardware solution to the problem of performing certain high level software instructions in a single cycle. Many combinations of conditions could be arranged. For example, CARRY, ZERO, and NEGATIVE flags from the Am29332 ALU chip might be used to perform If (AND/OR)-Then (AND/OR)-Else operations. By using multiway branching, the AND/OR functions in the If-Then-Else statement do not incur the penalty of additional gates or additional delay.

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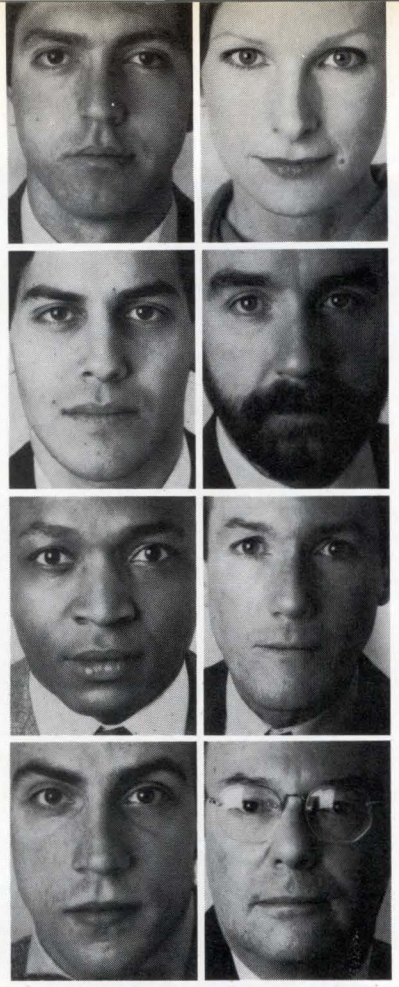

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TeleVideo 922

DEC VT220

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2. Our ESCAPE key is located above the TAB key, right where you'd expect to find it.

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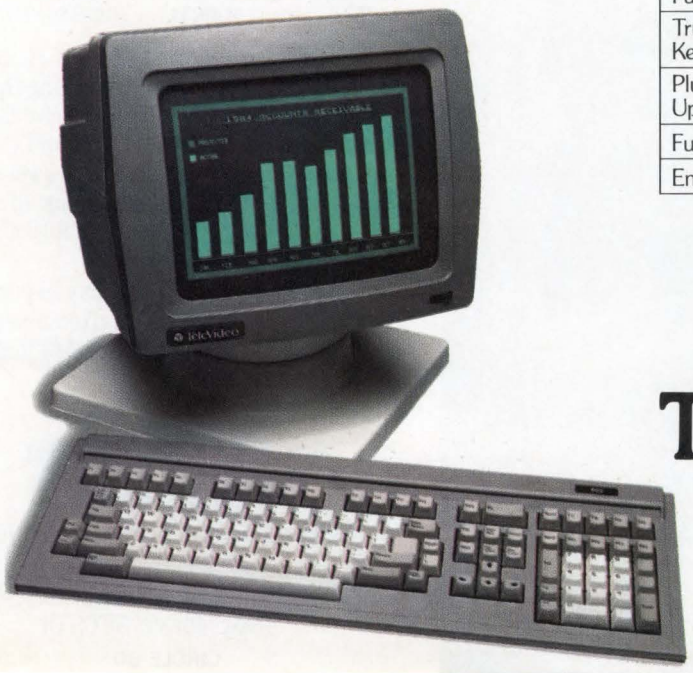
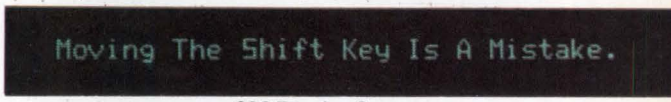
Where's the VT220 ESCAPE key?

3. Take a look below at the 922 keyboard. That's a true accounting keypad, complete with a Clear Entry, Double Zero and a TAB key. Not merely the numeric keys you get with the VT220.



4. Our SHIFT key is exactly where it should be, so it does exactly what it should do—shift. Their SHIFT key is shoved over by the < and > key to create lots of < and > on the CRT. Of course with a little practice, you could relearn their keyboard. But why, now that you've seen our 922?



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6. Here are 5 more advantages to the 922.

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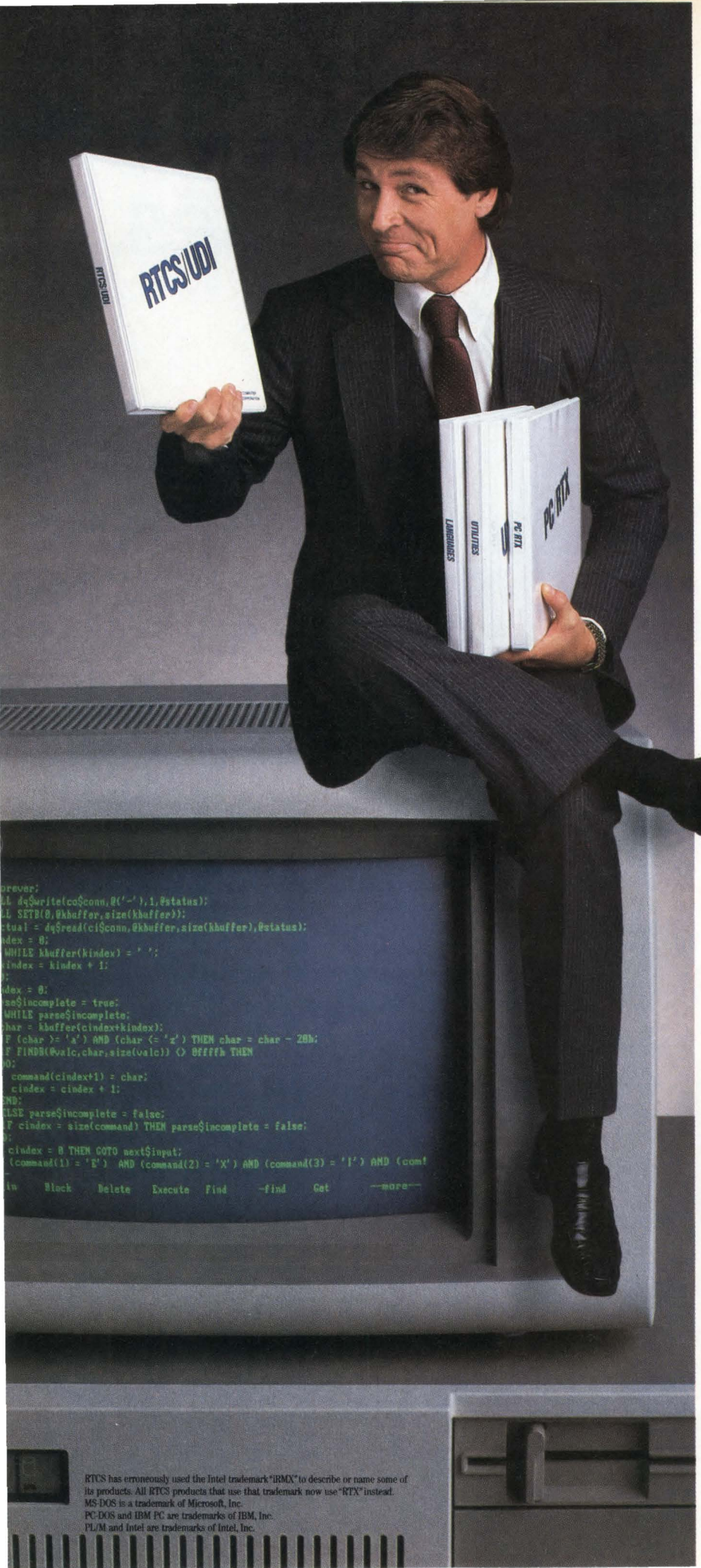

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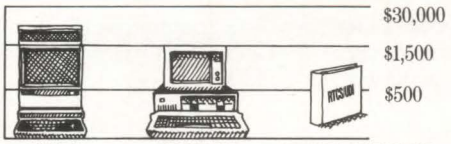

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MULTIBUS II DESIGNS EXPLOIT ADVANCED BUS CONCEPTS

With several bus architectures available, designers face the problem of choosing one that provides the features and flexibility needed for new multiprocessor designs.

by Amy Shuen and John Beaston

New bus concepts that provide higher performance and increased reliability are becoming more important in multiprocessor system design. The Multibus II architecture and the products that use it incorporate these bus concepts, including interconnect space, cache-based memory, and message passing.

The family of products incorporating the Multibus II bus architecture ranges from the iSBC 286/100 CPU board to bus interface silicon. At the lowest level of the family are the bus arbiter controller (BAC) and the message interrupt controller (MIC). With their generic local bus interfaces, these CMOS components make it easier to develop boards and systems using any processor family or architecture. Most importantly, standardizing the bus interface portion of a board design ensures that board-level products from multiple vendors can communicate with one another, even with diverse processor or memory technologies.

The BAC and MIC components provide the interface standard for the parallel system bus (iPSB) of the Multibus II architecture. They implement the full data transfer and reliability features of this bus, as well as support for the interrupt message subset of the Multibus II message passing. The BAC performs all the arbitration and system control functions and the MIC transmits and receives interrupt messages.

The first of a family of Multibus II bus interface silicon, BAC and MIC offer the advantages of VLSI. With these components, bus interface real estate requirements are 70 percent less than those of equivalent programmable logic array implementations. The next generation of Multibus II bus interface silicon will integrate this combination of capabilities into one component with full message-passing support.

Amy Shuen is a product marketing engineer for Multibus II products at Intel (Hillsboro, Ore). She holds an MBA from Harvard University.

John Beaston is marketing manager for Multibus II products at Intel. He holds an MS in electrical engineering from the University of Illinois.

Bus interface in silicon

The BAC and MIC combination is so flexible that all intelligent Multibus II boards can take advantage of their features. A 286-based CPU board can handle central processing and multiple 186-based boards can perform file serving and other I/O functions in the same backplane. The board designer does not have to worry about mixing and matching bus interface components; the BAC and MIC combination provides a modular, multipurpose standardized interface to the system bus for any intelligent board.

The BAC performs the complete bus arbitration and system control line management for the board. It functions much like a combination of the 82289 bus arbiter and the 82288 system controller Multibus I interface components that has been optimized for the Multibus II specification. When the onboard CPU wishes to access the bus, it activates a bus request input to the BAC. The BAC then performs the appropriate arbitration algorithm (either fairness or priority algorithms are dynamically selectable) and returns a grant signal to the CPU once the bus is

acquired. During the data transfer, the BAC performs all the necessary handshaking and error checking on the system control lines.

The MIC component helps solve the fundamental problem of communicating interrupts among multiple boards. In a multimaster, multiprocessing system, the number of interrupts often exceeds the capacity of the traditional dedicated interrupt lines. Since the onboard MIC sends and receives all interrupt messages, it eliminates the hardware bottleneck. This controller manages up to 255 interrupt sources and destinations.

To send an interrupt message, the CPU simply tells the MIC which module to interrupt and the MIC does the rest. The MIC asks the BAC to gain access to the bus and once that is done, the MIC runs the appropriate message interrupt bus cycle. The CPU and its local bus are free to continue processing rather than waiting for arbitration and access to the system bus. Decoupling the CPU and local bus from the iPSB can dramatically improve CPU utilization.

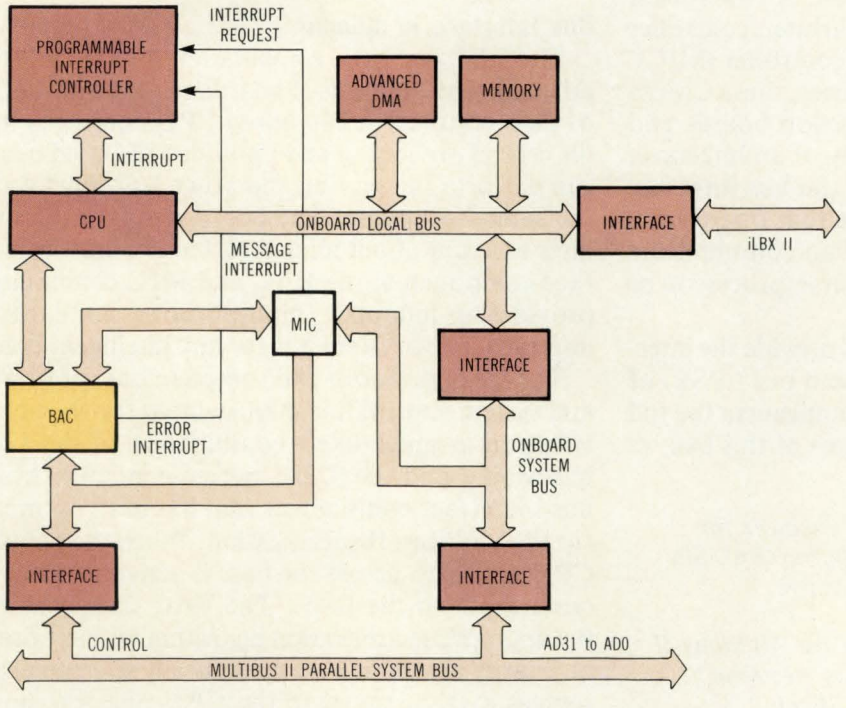
For receiving interrupt messages, the MIC monitors the bus, looking for interrupt cycles containing its message destination address. When one is received, the message goes in an internal 4-deep first in, first out queue, and the CPU is interrupted. The CPU may then read the message from the queue. The CPU is involved only when a message is received.

The new bus interface components can identify bus parity errors and check for interrupt message accuracy. Any detected errors are registered on the appropriate component and are reported to the onboard CPU. The CPU may then read the error registers to identify the cause and take appropriate action.

The iSBC 286/100 single-board computer takes advantage of the Multibus II system architecture for OEM applications. The combination of the iAPX 286 processor and two new bus structures, the iPSB and the local bus extension II (iLBX II), makes the iSBC 286/100 board uniquely suited to high performance multimaster system application. This board supports the new Multibus II features of interconnect space, built-in-self-test diagnostics, and message-based interrupt.

The board is a complete microcomputer system on an 8.7- x 9.2-in., double-high Eurocard printed circuit board—roughly the same real estate as a Multibus I board. It has the complete functional capability of a single-board computer, including iSBX bus expansion, 80287 numerical coprocessor options, advanced DMA control, JEDEC memory sites and expansion, SCSI configurable parallel interface, serial I/O, and programmable timers.

The ever-increasing performance of CPUs coupled with their larger addressing ranges poses a dilemma to the board designer. The best CPU-to-RAM access performance comes with a high price tag. In addition, the CPU board cannot hold enough RAM to approach the CPU's maximum address size. These constraints have led designers to develop the



The bus arbiter controller (BAC) and the message interrupt controller (MIC) are two CMOS components that implement the full data transfer and reliability features of the parallel system bus. They also include support for the interrupt message subset of Multibus II message passing.

THE MULTIBUS*-
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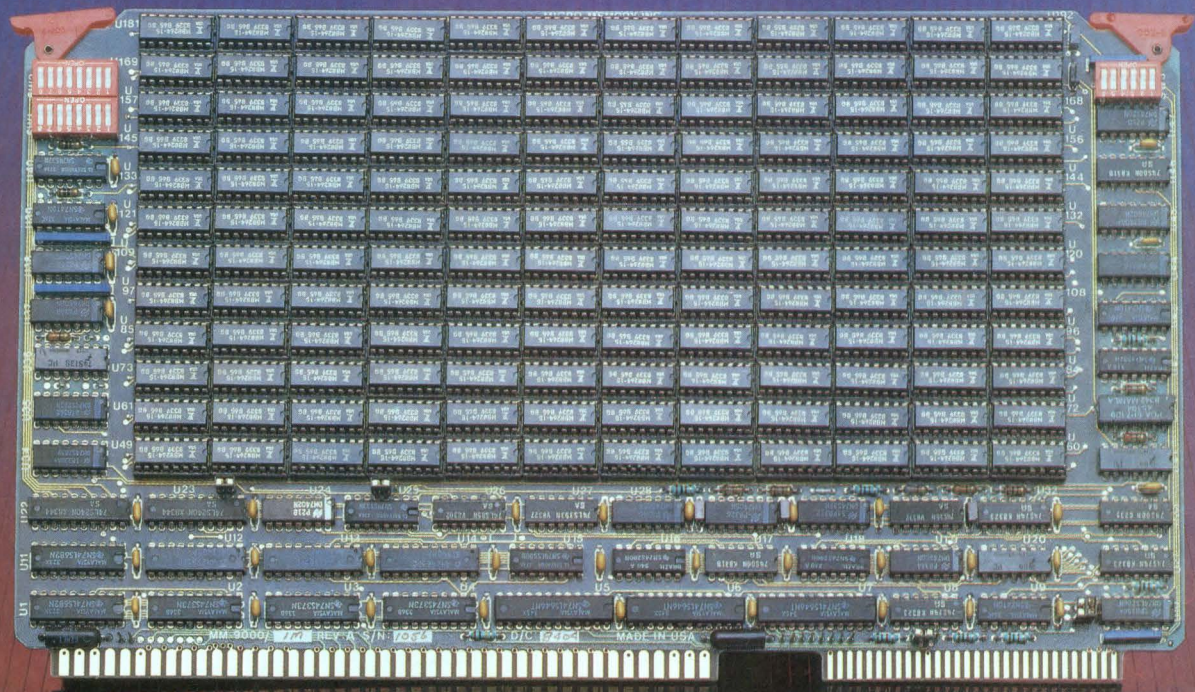

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local extension memory bus concept, such as the iLBX II for the Multibus II.

The iSBC MEM/3xx memory boards in the family are cache-based, 32-bit dynamic RAM boards with dual-port support (iLBX II and iPSB). They provide both the performance and the memory capacity needed. The memory boards, together with the iSBC 286/100 CPU board, give 0 wait-state iLBX II access performance for up to 16 Mbytes of memory.

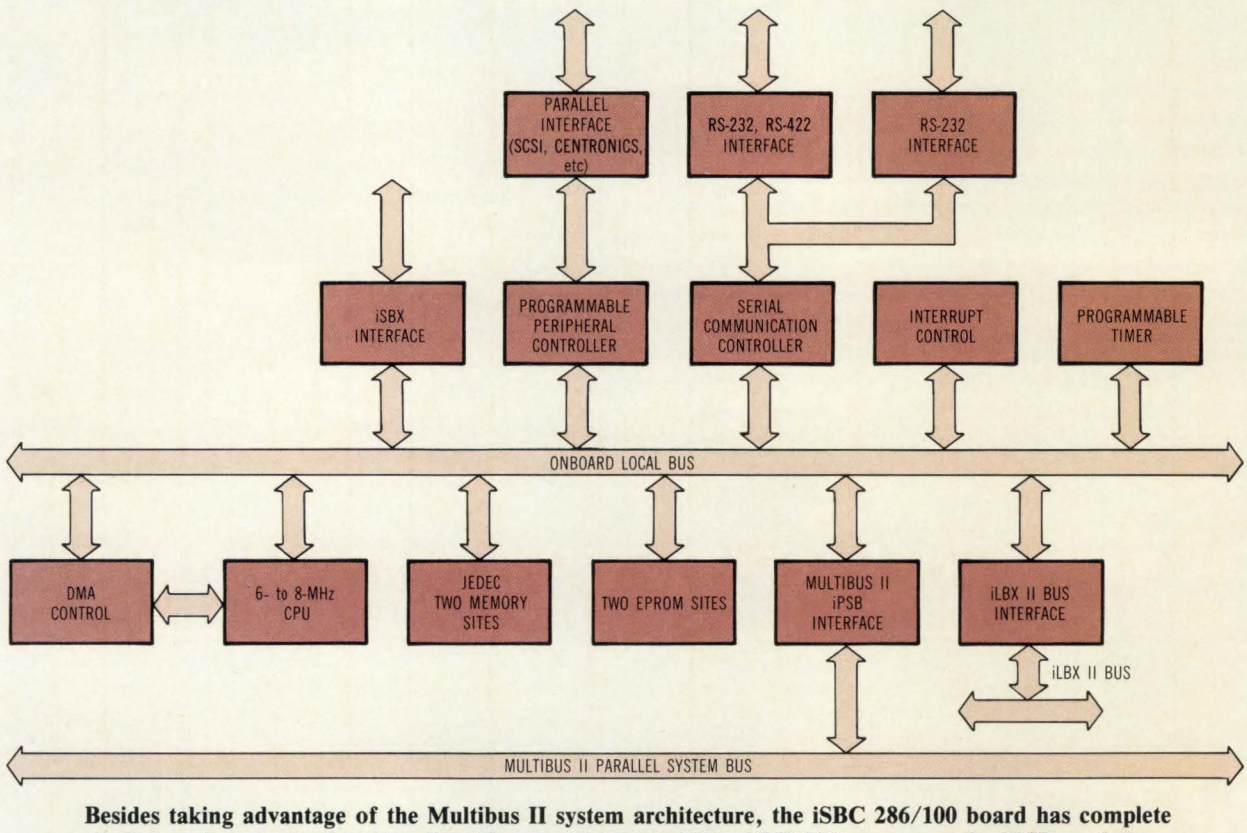
Cache memory concept

To illustrate the cache concept, imagine a desk drawer and a filing cabinet farther away—both are places to store documents. Frequently used files are in the desk drawer and the less frequently accessed files are in the filing cabinet. Correctly planned, 80 percent of the files needed will be in the drawer, limiting the number of trips to the file cabinet.

The desk drawer is a good analogy for the 8-Kbyte high speed cache memory on the iSBC MEM/3xx memory boards. Data requested by the iSBC 286/100 CPU from the memory board over the iLBX II bus is retrieved with 0 wait-states, if the data is in the cache. Depending upon the application code, 80 percent or more of the time the cache algorithm ensures that the data requested is in the cache. This is called a cache "hit." If the data requested is not in the cache memory, this is called a cache "miss." In the iSBC MEM/3xx and iSBC 286/100 combination, a cache miss takes 1 wait-state. These performance numbers refer to up to 16 Mbytes of iLBX II memory, the full physical addressing range of the 286 CPU. Each memory board added to iLBX II adds an additional 8 Kbytes of cache.

Going back to the desk drawer and file cabinet analogy, a search will go outside the desk drawer less than 20 percent of the time. Some of the unused less current documents from the desk drawer can go into the filing cabinet. The documents needed immediately, as well as some that might be used later, return to the desk. This simple, but effective, algorithm increases the probability that the desk drawer will contain the most useful documents, and that processing time will be used efficiently.

The cache replacement algorithm works in a similar way. On any miss or write access, the contents of one cache entry are updated to maintain consistency with the corresponding entry in the DRAM array. In addition, a full 32 bits, two sequential 16-bit words, are moved each time.



Besides taking advantage of the Multibus II system architecture, the iSBC 286/100 board has complete single-board computer functionality. The combination of the iAPX 286 processor, the iPSB, and the iLBX II enables this board to handle high performance, multimaster system applications.

The cache control and most of the logic required on the iSBC MEM/3xx memory boards are implemented in VLSI. This proprietary cache controller supports the 32-bit architecture of both the iLBX II and iPSB interfaces. A VLSI solution saves real estate for putting large amounts of DRAM (64- or 256-Kbits) on the memory boards along with an 8-Kbyte high speed static RAM. These new cache-based, 32-bit memory boards come in 1/2-, 1-, 2-, or 4-Mbyte sizes.

Software and hardware converge

One of the advanced concepts of the Multibus II architecture is the definition of the interconnect address space, which integrates hardware and software. This integrated approach makes building and dynamically configuring a Multibus II system easier and faster. Multibus II interconnect space is a combination of a standardized set of read-only and software configurable registers on every board and the ability to access them by any bus master.

An integrated approach makes building and dynamically configuring a Multibus II system easier and faster.

The read-only registers hold information, such as board type, revision number, and serial number. This allows board manufacturers to code this information into the hardware so that software can determine what boards are being used in a system, and configure itself automatically. The software configurable registers allow software to write to these registers for board configuration purposes or to access or control diagnostics. This facility can help reduce or completely eliminate hardwired jumpers or DIP switches and gives new flexibility for local and remote diagnostics.

Geographic or by-slot addressing allows the software to address individual boards via their physical position in the backplane. Automatically at power-up, the iSBC CSM/100 assigns slot IDs to the boards located on the iPSB backplane. These IDs are picked up and saved by the onboard BAC. After this assignment, software can identify which boards are in the system and where they are located. This becomes system configuration information.

By using the interconnect address space to perform geographic addressing, the iRMX 86 Multibus II operating system automatically configures all memory boards at power-up. The system software is aware of the hardware characteristics of the memory boards because each of the iSBC MEM/3xx boards has read-only registers in its onboard interconnect space registers. These registers indicate the size of the DRAM array of that particular board.

The iRMX 86 Multibus II operating system identifies which memory boards are in the system and where they are in the iPSB backplane and then assigns the starting and ending address of each board. This assignment is made by the system software writing to the software configurable interconnect registers located on each board. As a result, no hardwired jumpers are necessary on the iSBC MEM/3xx boards. Changing the memory size or swapping memory boards is an easy and straightforward process—simply put new boards in the backplane and power-up the system and the software does the rest.

The central services module also supplies the system clocks and contains front panel reset and interrupt switches. In addition, it provides a battery-powered time-of-day clock so that software can access time/date records and initialize local clocks. It also forms one side of a link to Multibus I systems. Also, it contains an 8751 microcontroller to perform built-in-self-test (BIST) diagnostics.

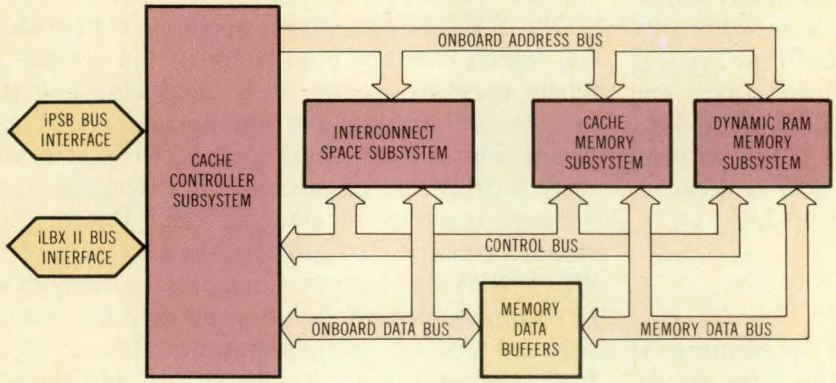
Every Intel Multibus II board has an 8751 microcontroller onboard and firmware to run these BIST system confidence tests at power-up or at software command to check out each board's vital functions. These confidence tests and diagnostics improve reliability and error reporting capability and reduce manufacturing and maintenance costs for the user.

A microcomputer watchdog

The BIST diagnostics combined with the use of interconnect space provides a powerful diagnostics and development environment. The BISTs provide vital board status and error information at power-up. Because this error information is recorded in each board's interconnect space registers, the information can be accessed from software on a system-wide basis for logging, display, or remote diagnostic purposes. Additionally, during development, modification, or manufacture of a Multibus II system, you can evoke specific BISTs for status information significant to a particular application.

The BIST results are indicated in two ways. First, an LED on the front panel indicates the status of the power-up diagnostics. It is on when the BIST starts running and off when the BIST completes successfully. Second, the diagnostic test results are stored in the onboard interconnect registers accessible to system software.

In a large, complex multiprocessing system it is often difficult to determine the specific hardware source of a system failure. The interconnect space allows software to access board status and diagnostic information. The system software can identify which



The iSBC MEM/3xx boards have four main subsystems. These boards have capacities ranging from 0.5 to 4 Mbytes and they incorporate 32-bit data paths.

boards in a system passed or failed their power-up diagnostics and by examining the appropriate error register contents determine the possible sources of the failure. The software can then dynamically change the memory size to disable a nonfunctioning memory board. It can also check for correct installation of the iSBX bus or PROM on a remote iSBC 286/100 board. Additionally, the iRMX 86 Multibus II operating system can interrogate the boards in the system for their system-wide go/no go status and thus determine problem boards.

As an example of the BISTs, a memory board will not function properly if the DRAM array, the cache RAM array, or the parity detection are not functioning properly. The BIST performed by the onboard microcontroller checks vital functions; an address ripple RAM test on DRAM array in Miss Only operation mode, a cache RAM test on all the cache memory, a Refresh check on a small portion of DRAM, and a parity test which injects parity errors in the DRAM and verifies that the board detects them accurately.

Until now, system performance enhancements have come primarily from improvements in CPU technology: higher clock speeds and wider data paths. There have been very few similar technology improvements applied to the system architecture. The Multibus II architecture is specifically designed to accommodate CPU improvements while allowing technology to be applied to the system architecture. Enhanced CPUs give raw performance improvements, but the message-passing concept allows similar improvements in system architecture.

Performance improvements lie in the efficient support of multiprocessing. Multiprocessing is not a new concept, however. The problems encountered in implementing it tend to reduce its promised benefits. Many systems contain multiple processors such as a host CPU, an intelligent disk controller, and other intelligent I/O subsystems. The job of communication and data movement among boards has typically been a system software and dual-ported memory task. Multibus II message passing standardizes the communication and data movement functions among the boards. This standardization allows the application of VLSI to the problem. It gives a hardware-based solution to the problem, alleviating the software development burden and giving hardware assistance to data movement.

The message-passing protocol specified by the Multibus II architecture achieves full multiprocessing capability. The next generation of bus interface silicon provides a hardware solution to off-loading the CPU during the interprocessor communication and data movement functions. Very much like a distributed smart DMA controller, this message-passing coprocessor communicates with other intelligent boards to transfer data and information over the system bus. The CPU that initiates this communication is free to continue its computing process until the data is received.

The benefits of this silicon-supported approach are significant. First the message-passing interface can take full advantage of the bus bandwidth—32-bit data and burst transfer mode—independent of the type, word width, or architecture of communicating processors. Hardware transfer rates and I/O system performance is higher than a software-based I/O transfer where the software must copy and check each transfer and CPU intervention is required. Also, since the message-passing interface effectively decouples the local-system-local bus transaction, each portion of the transfer can proceed at the maximum transfer rate of that bus. The communicating boards utilize as little of the all important system bus bandwidth as possible, freeing it for additional communication.

Second, the Multibus II message-passing interface provides a uniform software interface for all boards in the system. Since modules communicate through

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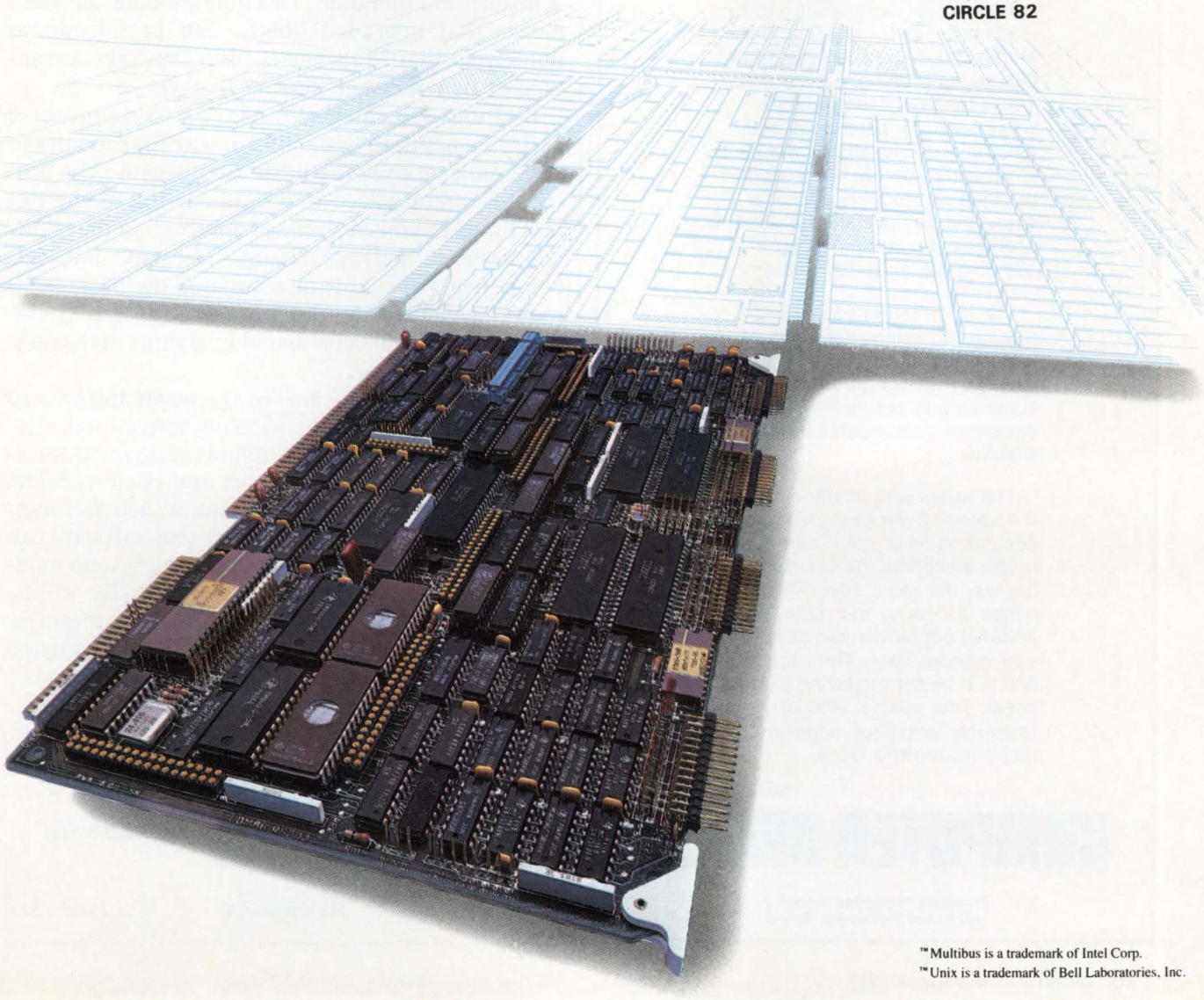

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either control or data messages over the system bus, boards can be added or replaced without any software changes in the controlling boards' operating system software. This makes it easy for users to add new capability, such as new disk controllers, without completely rewriting the driver software.

The system software's standardized protocol for passing data and communicating over the system bus opens the door to multi-operating systems communicating via message passing over the Multibus II system bus. The message-passing silicon interface would decouple the operating systems so that multitasking can take place in one functional unit while human interfacing and timesharing can take place in another.

A distinguishing characteristic of the iSBC 286/100 CPU board is the bus interface multimodule that isolates the BAC and MIC silicon on a piggyback connected to the baseboard by a pin grid array socket. When full message-passing silicon is available, this BAC/MIC multimodule will be replaced by a pin-compatible, full message-passing bus interface controller multimodule. This multimodule approach means that upgraded boards can be introduced quickly so that Multibus II users can take advantage of new message-passing features.

Multibus II's integral message-passing protocol defines a standard and uniform way for modules to communicate over the iPSB bus. Because the protocol is standardized and modularized at the bus level, Intel has taken a phased approach to the implementation of message passing. The BAC and MIC components available now provide the basic iPSB requirements for development of Multibus II systems including message-based interrupts in the message address space.

In the system software for the newly introduced Multibus II boards, the operating system uses messages only for intermodule signals and synchronization. A conventional dual-port approach transfers data between boards in a system. When full message passing is supported, the system software can use messages for passing data between system modules. Although both types of data transfer will be supported by the system software, the message-passing solution will offer substantially increased system performance for multiprocessing systems.

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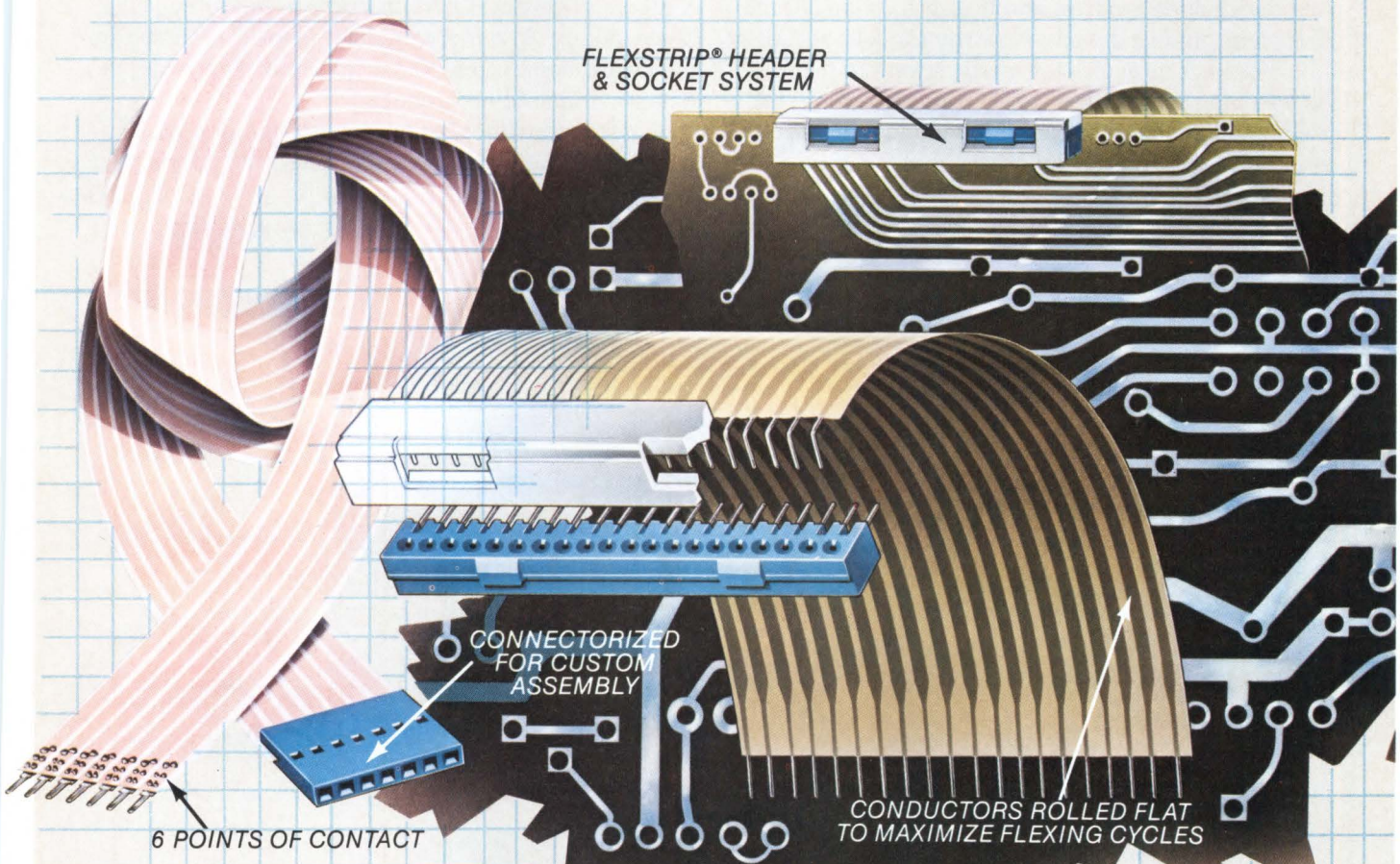

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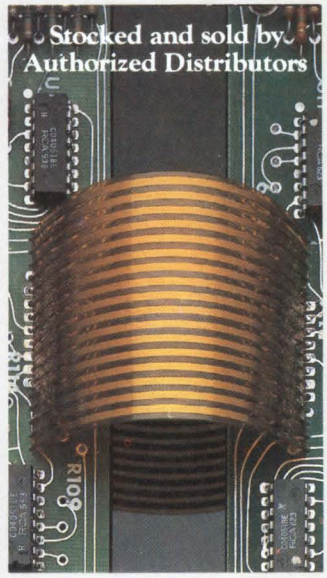

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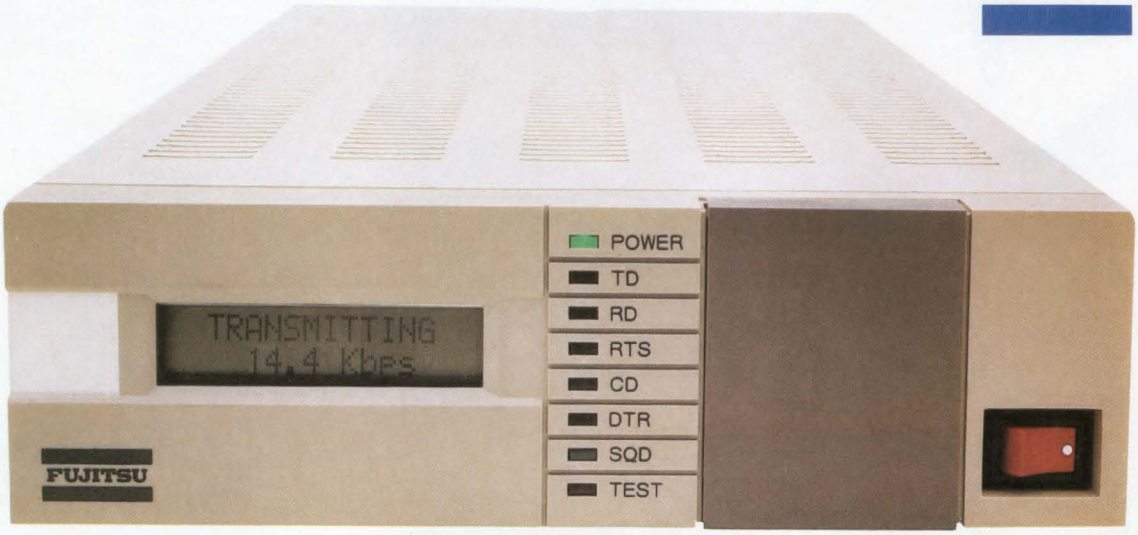
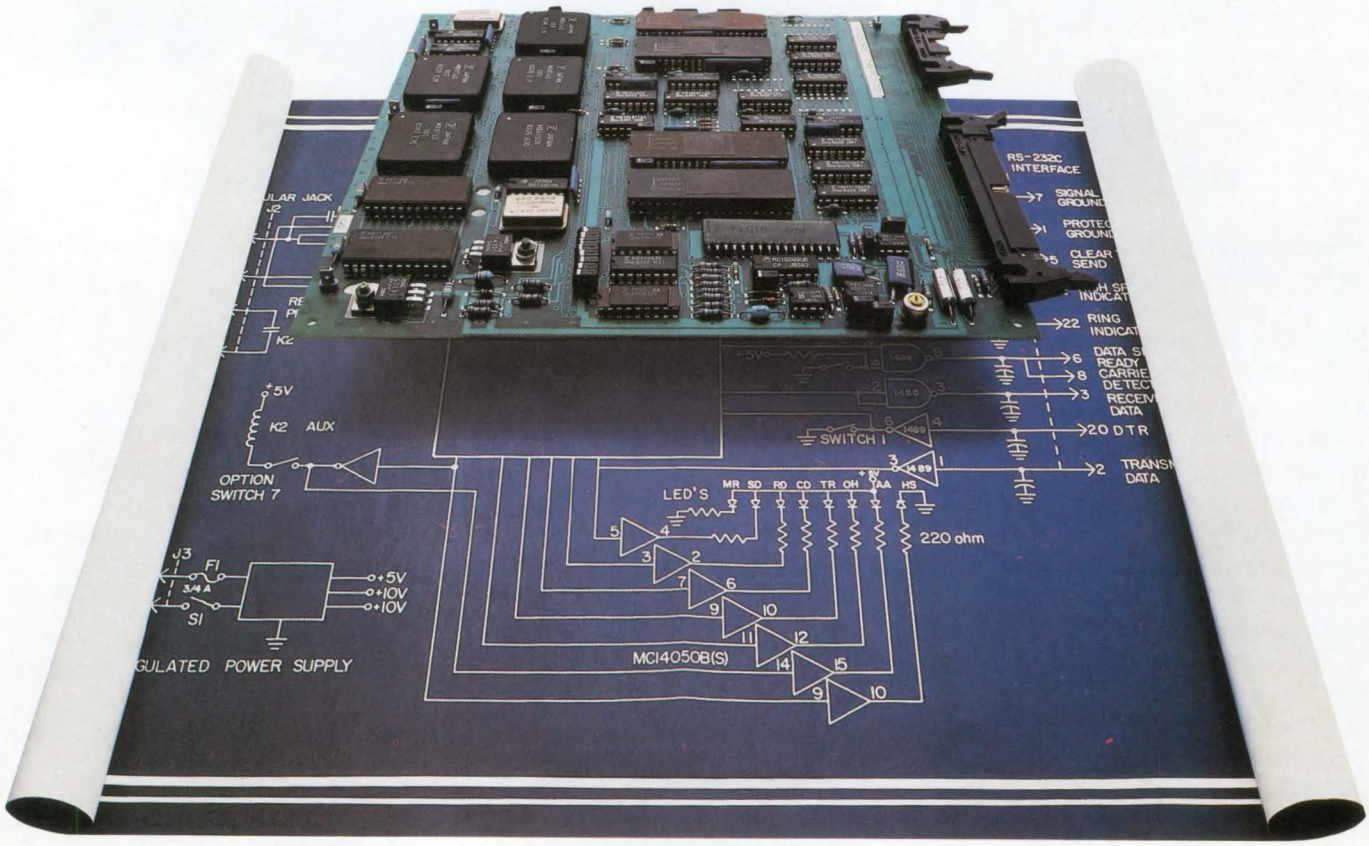
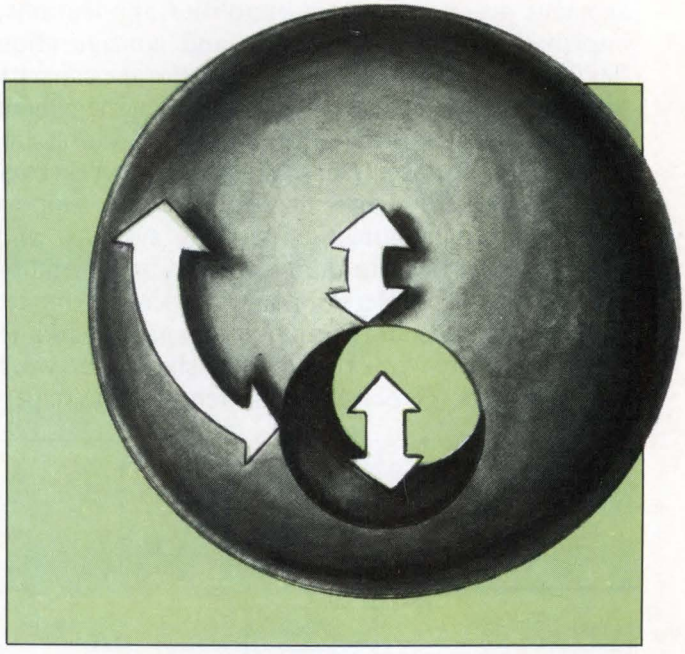




CIRCLE 84

COMPUTERS TAILORED TO EFFICIENT EXPANSION

Sharing utilities and applications as well as automatic code and data segmentation can give today's user needed power. Future computing, however, requires virtual machines that can handle multistate architectures.



by Thomas C. Boos

The computer industry has a critical need for large scale systems with much more than sheer processing power. Trying to fulfill this need are huge numerical arrays and information management applications coupled with major data processing tasks. This combination only emphasizes the need for machines with near limitless virtual memories, large real memory, wide I/O bandwidths, shared data bases, and high level application development tools. An effective system must also let multiple users share system utility codes, application instructions, and data easily.

Two additional challenges are application development costs and security requirements. Even with the advent of higher level (fourth-generation) languages, the cost of application development has increased. Purchasing predeveloped, packaged applications is often a viable solution. Software portability, however, can be a severe problem if the target system architecture does not lend itself to portability easily. The proliferation of data terminals and microcomputers that access mainframe computers increases the risk of unauthorized access to programs and data bases. This risk must be minimized to effectively meet the security requirements of a large, diverse user base. The Control Data CYBER 180 design addresses all these issues with its instruction set and ring-based security scheme.

The development strategy of this line of computers is based on a total system architecture. A key design objective was to create a system that could exploit hardware features to support an advanced operating system, high level language, large amounts of memory, and information management technology. The thrust of the CYBER 180 hardware approach is to implement hardware features that support the advanced concepts in operating system technology—an innovation, since previously advanced concepts for operating systems were introduced on outdated hardware.

The new system architecture had to remain compatible with previous Control Data products, allowing migration to the new systems without a total reinvestment in application software. This required any new machines to support multiple instruction sets and word lengths. By developing a virtual machine that tightly coupled the new architecture to the existing CYBER 170 series, both existing real

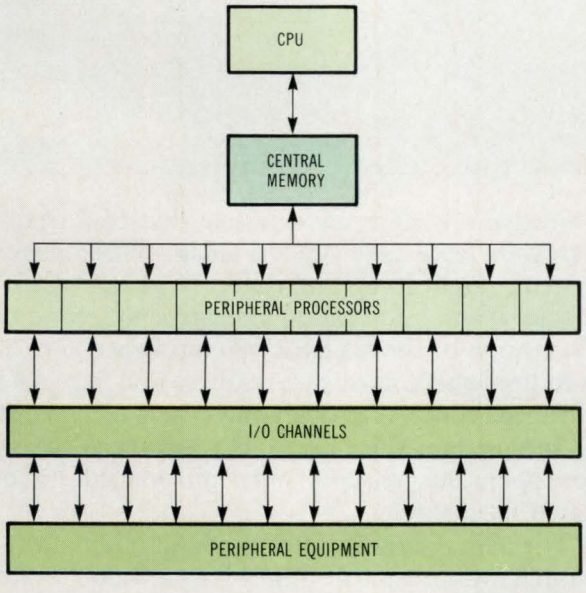
Thomas C. Boos is general manager of the Computer Development Division at Control Data (Arden Hills, Minn). He graduated from the Brown Institute of Electronics in Minneapolis.

memory code and new virtual memory code could run in the same machines.

The design objectives for the system cover several areas. Architecturally, a distributed approach moves the I/O overhead from the central processor to the peripheral processors. In memory, code and data are automatically separated into segments and combined with virtual addressing to ease both portability and application development. A dual-state ability allows two operating systems at once. The operating systems share the central processor; an extended "virtual machine" supports other states. The machine also incorporates cost-effective data security features that do not limit the machine's usability.

Some architectural features

The CYBER 180 systems include a storage-management architecture that simplifies applications, improves software portability and configuration flexibility, and supports large main storage capacity and secure data sharing. The storage-management architecture also provides large virtual addressing capabilities. For example, the system can access over 8 trillion bytes of virtual memory, allowing support for advanced languages, operating systems, and security concepts. The architecture supports multitasking jobs, compilers that automatically generate fully reentrant code, recursive languages, and 15 rings of security for optimal code sharing between jobs and tasks. To place these system features in perspective, consider the IBM XA, the closest comparable system. It has a virtual address space of only 2 Gbytes of central memory—1/4096th the capability of the CYBER 180.



Although only one program can use the central processor at a time, many programs can have peripheral processors performing operations for them. Thus, many programs, in some state of execution, can be in the system at the same time.

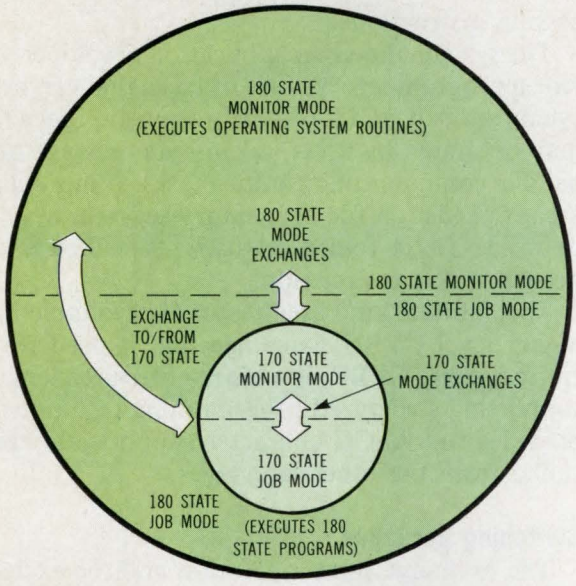
In the CYBER 180 architecture, a program's address space can include up to 4096 unique segments. The size of each segment can increase and decrease independently. (A segment is the unit of sharing between programs. It partitions the virtual address space, plus typically provides the natural divisions of code and data in a program.) One segment is equal in size to the maximum total address space of a program executing on a XA system. Other IBM systems in that product line restrict a program's address space to even less than one CYBER 180 segment.

Another aspect of the multiple virtual shared segment architecture is its effect on I/O operations. The system can declare data sets to be segment access files, which allows a programmer to view a file as an array or a repeating group. Since the data is referenced directly as though it were a table in memory, no program I/O is required.

Combined with this is a powerful and unique feature of the CYBER 180 I/O system that allows a user to state "intent" when opening a data set for processing. Certain "intent" declarations turn the CYBER 180's huge memory into a highly efficient "global cache" that supports I/O page level read-ahead and write-behind processing. Data processing industry analysts agree that a large memory global cache approach is the most efficient way to access data sets between tasks and jobs.

The architectural design objective was to have the main processor (or processors) directly linked to the process. Each model has a large central processor that executes all user programs. Smaller peripheral processors (integrated microcomputers) execute all I/O operations and various operating system functions, keeping the central processor free from these tasks. This distribution of functions in a parallel processing context is a cornerstone upon which all CYBER systems have evolved. Offloading much of the I/O tasks to peripheral processors increases system throughput, thus the central processor can concentrate on processing user programs. Based on this concept of parallelism, the computers will achieve up to a 125-Mbyte/s I/O bandwidth with minimal CPU involvement. Central memory isolates the central processor from the peripheral processors and serves as the communications vehicle between them. Data is read from peripheral equipment by the peripheral processors and then stored in central memory. The central processor then accesses data and program instructions from the central memory.

Central memory words are read and written between central memory and peripheral processor



In dual state, two operating systems—NOS (6-bit/60-bit words) and NOS/VE (8-bit/64-bit words)—run simultaneously in the same memory and CPU. The 170 state environment is actually supported as if it were a special-purpose 180 state program. Thus, parts of the 180 state support the 170 state but the 180 state is transparent to any user programs executing in the 170 state environment.

memory by the peripheral processors using a buffer register that assembles and disassembles the words in a first in, first out fashion. When a central memory word is read, it is disassembled into a fixed number of peripheral processor words (there are four 16-bit peripheral processor words in each 64-bit central memory word) and sent to successive locations in the peripheral processor's memory. To write a central memory word, the hardware assembles several successive peripheral processor words into one large word and sends it to central memory. The hardware that performs this function is called a read/write pyramid. The main benefit of this process is maximizing bandwidth while minimizing hardware complexity.

Another reason for accelerated system throughput is the concurrent processing by the central processor and peripheral processors. For example, while the peripheral processors perform I/O operations, the central processor continues executing other programs. Furthermore, because peripheral processors operate independently, they can be performing operations for many programs at the same time.

The CYBER 180 memory architecture simplifies application development and improves software portability by combining virtual addressing capabilities with automatic separation of code and data into segments. For instance, one segment can hold data files used by the process, another executable code unique to the process, and another a duplicate copy of the operating system code shared with other users. Each segment has a capacity of 2000 Mbytes or 262 million words. Segment size varies according to the amount of information it contains. Over 65,000 segments can exist systemwide for all user processes.

Since peripheral processors operate independently, they can perform operations for several programs at the same time.

This segmentation scheme is utilized by all of the system compilers. All compiler-generated instructions are automatically loaded into an instruction segment without any explicit intervention by programmers. All data related to specific tasks is automatically loaded into data segments. This type of structure enables the system to easily have one copy of a program—such as the Fortran compiler or a user application—work on multiple problems. In other words, the concept of instruction and data segmentation allows the CYBER 180 architecture to share programs and data systemwide. Further, the ability to share data segments makes it possible to easily implement complex data processing tasks such as concurrent file access and subjob-level multiprocessing.

Moreover, since data sets can be declared segment access files and file I/O is not required, users can directly address file contents as though they were tables. This feature separates storage management functions from applications and runtime services. Thus, application programs are not dependent on media size, type, and location. The user does not have to rewrite or modify programs to take advantage of more real memory and different types of storage media, or to execute on smaller or degraded configurations.

Dual-state virtual machine advantage

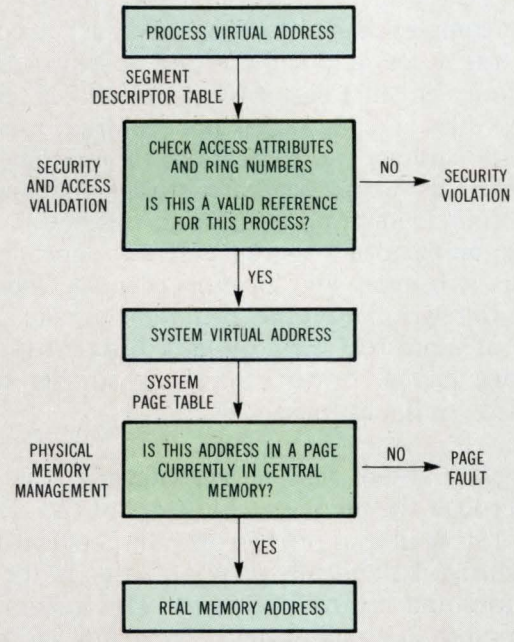
Through the unique architecture of the CYBER 180, it is possible to run two operating systems simultaneously, dynamically on a job basis, in the same memory and central processor. This capability is referred to as "dual-state." The actual mechanics of the dual-state are invisible to the user, who sees only one operating system at a time.

The memory organization of the CYBER 170 network operating system is 6-bit bytes and 60-bit words. The memory organization of the network operating system/virtual environment is 8-bit bytes and 64-bit words. Although the environments for each state are present, the central processor executes

in either one state or the other. High performance is ensured in both states since neither state is an emulation mode.

NOS is an established, feature-rich system, based on user-friendly, menu-driven programming tools, such as full-screen editors, online documentation, and interactive debuggers, which operate in both Cobol and Fortran environments. The NOS instruction set supports real memory addressing of up to 131,000 60-bit words per program (131 Mbytes) and a 12-bit mode for the peripheral processors.

NOS/VE is an easy-to-use operating system that provides access to large memory spaces using an address range of about 8.8×10^{12} bytes. Further, all NOS/VE programs, utilities, and procedures are automatically and completely reentrant or shared. Both the virtual memory and the reentrance capability are automatically available to all applications writers. One of NOS/VE's most advantageous features is its ability to run customer programs originally developed by other vendors with either minimal or no code conversion. The instruction set running NOS/VE is 8-bit-byte-oriented, supports virtual memory addressing, and handles packed instructions of 16, 32, and 64 bits. It includes powerful scientific and engineering instructions (with vectors in one model) and a comprehensive set of business data processing instructions.



Even though code and data can be shared in a virtual memory system, security features constrain each task to an address space and prevent it from reading, writing, or executing code or data outside of this space. Because every memory reference requires a translation from a virtual address to a real address, it is appropriate to check for security violations prior to accessing real memory.

The system allows an application developer to divide a program into a series of tasks that can be run synchronously and/or asynchronously. Since tasks may be shared by users, a 256-byte message queue handles communication among tasks. If more shared area is needed, a file or memory segment may also be used. Tasks return status when called and, if needed, upon completion.

This multitasking architecture is available in the higher level CYBIL language that is used for the entire system. CYBIL is a block-structured language supporting structured programming techniques. It provides full ASCII character support and can be called from the other languages.

Switching packages

The exchange jump operation and the exchange package switch programs in and out of execution. The exchange jump occurs whenever one program must enter an inactive state and another program has to be executed. A single instruction starts and performs the exchange operation, then writes this information to an exchange package. The exchange package in every program contains all the information necessary to start or resume program processing: a description of the central memory used by the program, the next instruction word to be executed, the contents of all central processor registers, and the contents of certain status registers.

The crucial feature of dual state is the dynamic sharing of the central processor. Since the software systems can coexist on the same mainframe and in the same central processor, the user can introduce NOS/VE in a controlled, nondisruptive manner—choosing the operating system that best suits the application. In this mode, if the central processor is executing a program and has to wait for some action to be taken before continuing, it can switch programs and process a different one. On the other hand, if the central processor has to wait for some action before continuing a program in one state and an unfinished program exists in the other state, it is able to switch states and work on the other program. The advantage is that the central processor never has to wait in one state if there is a higher priority task in another state. In addition, the operation of NOS is not affected when the user implements NOS/VE other than for some minor resource utilization—the functioning of NOS/VE is invisible to the NOS user.

Transferring operating states is an easy task for the user. After logging into NOS, the user enters NOS/VE by switching applications, either explicitly or implicitly by procedures. At that point, the user

regards NOS/VE as a natural timesharing system. Input and output files are automatically linked to the terminal. Interactive users, if so validated, may switch states if they need to work at first with NOS and then return to NOS/VE. Since the full screen editor is the same for NOS and NOS/VE, the application writer has the same access view of both states. Batch access (or remote job entry) is also user-transparent.

Multistate architecture, which permits 16 machine states to operate in one CPU, is an extension of dual-state virtual machine capabilities.

During the development of the CYBER 180 architecture, the designers predicted that users would require machines capable of executing other, more specialized instruction sets, such as symbolic primitives for artificial intelligence or specialized codes for relational data bases. As a result, they extended the dual-state "virtual machine" capability to support additional machine states. Called multistate architecture, this currently permits up to 16 different machine definitions to operate in the same CPU. The user benefits by having a computer that can not only expand technologically, but also perform at optimum levels while allowing the change.

Greater data security

The increasing number of computer users coupled with the well-publicized incidents of computer crime point to the need for improved computer security. As a result, data processing managers are implementing plans to safeguard computer resources from system errors and to monitor the access of sensitive data. The CYBER 180 computers contain extensive built-in security features to protect valuable computer resources cost-effectively without compromising use of the system.

The CYBER 180 security levels are based on the address space of the program, access attributes, and rings of protection. As previously discussed, the systems address space can have from 1 to 4096 segments, with up to 2 Gbytes per segment. The segments' ability to separate programs into sections of executable code and data and further separate these segments into rings so that code can be shared (but not changed), dumped, or viewed is a built-in security feature.

The access attributes also contribute to data security by determining what can be done in a segment. Every segment has certain access attributes associated with it, such as read, write, execute, or a combination of these three. Because of the access attributes associated with it, each segment is safeguarded from inappropriate use. For example, no data can be written into an execute or read-only segment, so the information contained there is safe.

A program's virtual address space also includes layers, or rings, of protection to ensure the safeguarding and management of memory. The segment ring number determines the levels of privilege, which determine use of that segment. Fifteen levels of privilege can be assigned to each segment. Each ring, or level, is more privileged or less privileged than those adjacent to it. The lower the ring number, the more privileged and, thus, more secure the information. Most operating system codes execute in the lower, or inner, rings; while less secure user programs execute in the higher, or outer, rings. This mechanism allows one group of users access to certain machine capabilities, such as information retrieval and loading, and allows another group the ability to add or alter stored data. In addition, rings allow code that has different levels of protection to execute in the same address space using the same conventions and rules for procedure calling and parameter passing as code in an environment with single-level protection.

Another security feature results from CYBER 180 I/O, which is controlled by separately programmed computers, rather than directly through the CPU. Although users indirectly request I/O through the system server, the actual I/O is performed by these peripheral processors. This form of I/O isolation protects the operations of the requested central processor from tampering.

Furthermore, because of the central processor's exchange jump mechanisms, the CYBER 180 security system does not limit system performance. Through a form of "context switching," user operations are separated from other users and system operations, even though they are able to run concurrently. Thus, security controls cause little delay in user operations.

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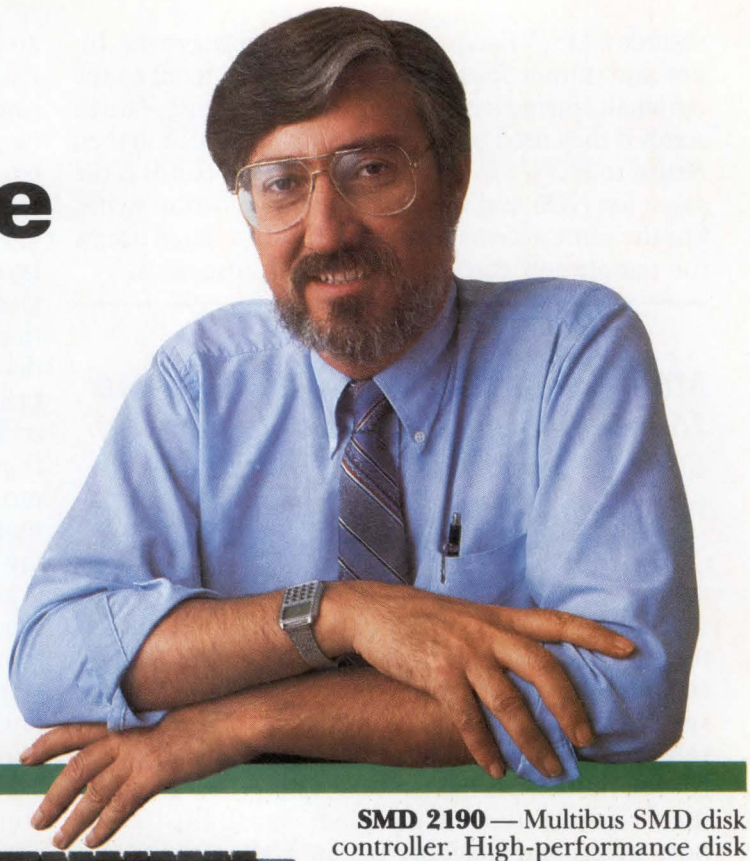

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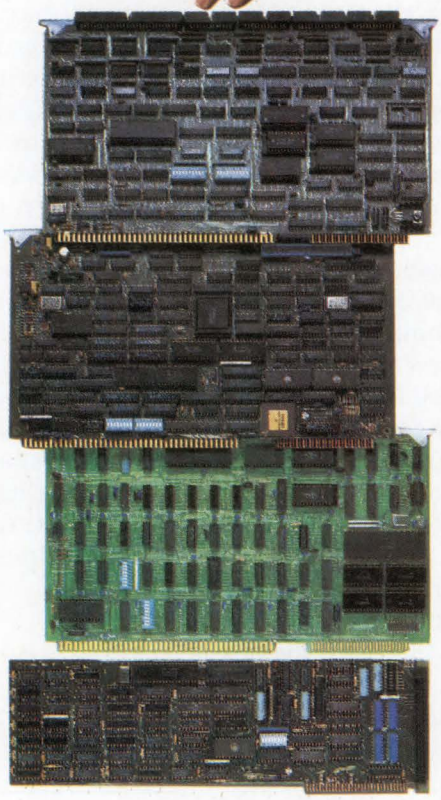

SMD 2190 — Multibus SMD disk controller. High-performance disk controller with intelligent cache memory for UNIX,™ RMX and similar operating systems. Supports four SMD drives, 1:1 interleave, 20 Mb/S data rate, 32-bit ECC, automatic error correction, 4.5 MBytes DMA, 24-bit addressing.

LNC 5180 — Multibus token passing network controller. Supports up to 255 devices on a star or bus network. Data rates up to 2 Mb/S on coax or T1 lines. Higher throughput than Ethernet,™ automatic flow control and error recovery, ISO levels 1-5 on board. Simplified software interface with features for real-time applications.

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CIRCLE 85

Wide range of configurations marks Multibus microcomputer package

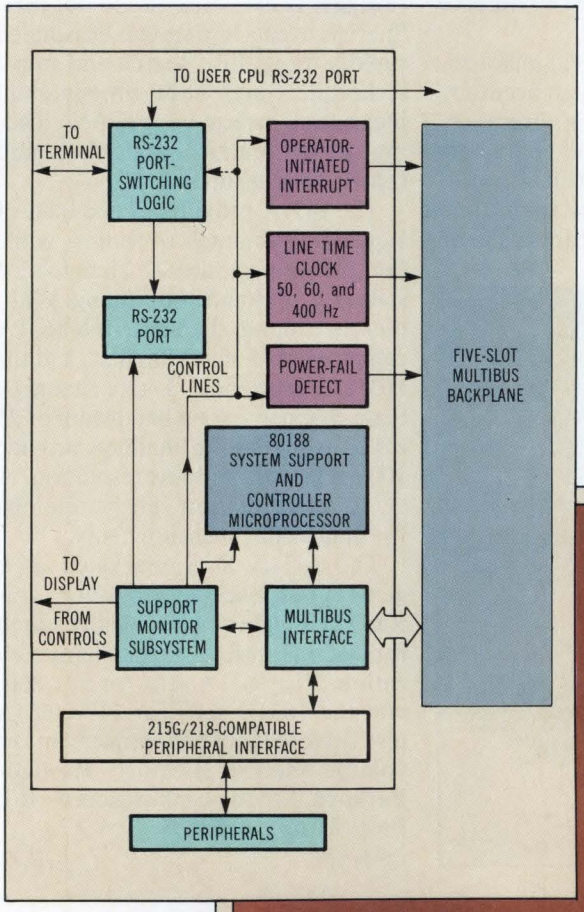
A flexible, packaged microcomputer lets designers mold diverse configurations. This system, dubbed the SMS 8000 model 40, includes a Multibus backplane, a single-board Foundation module for disk control and subsystem diagnostics, a front panel, and a high output dc power supply. Designers can choose boards to connect to the backplane or use manufacturer supplied boards.

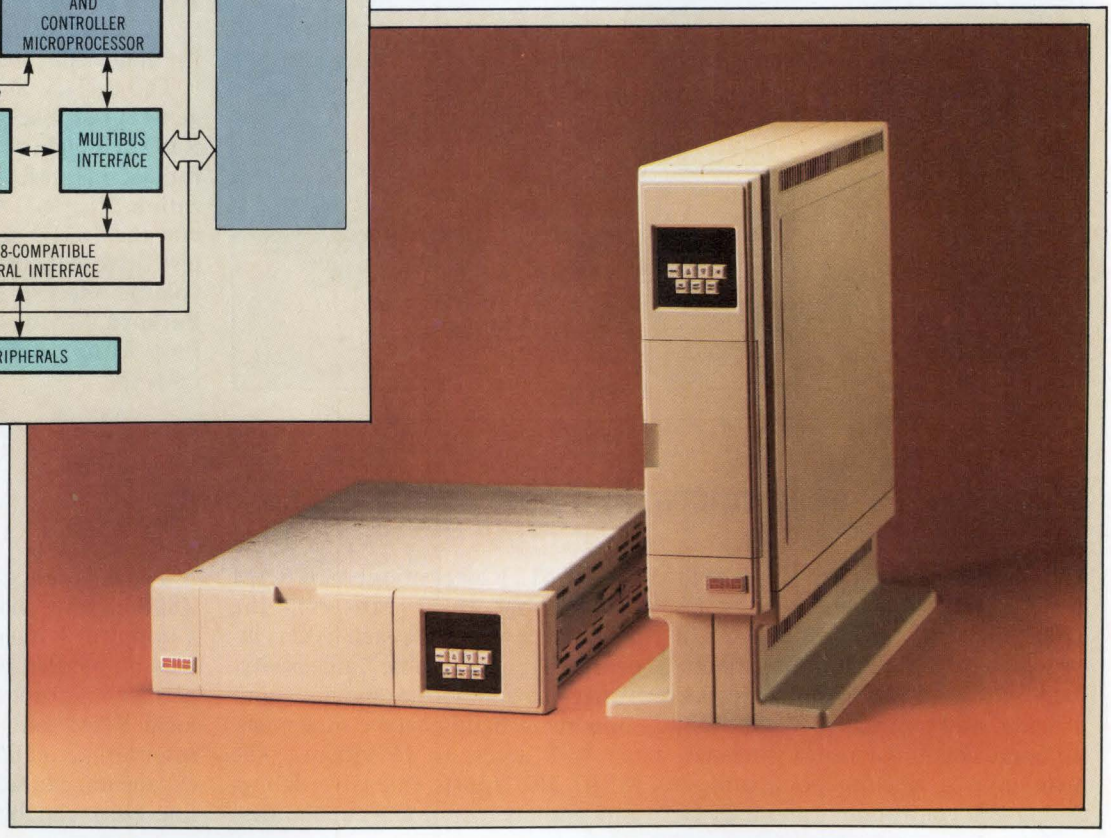
The model 40 boasts a five-slot Multibus backplane that accepts user-selected CPUs, memory cards, and other modules. This 24-bit backplane (which provides communications among the CPU, memory, peripherals and system control units) supports emulation of the Intel 215 controller. Applications developed for the 215 controller reportedly run without modification on the system. The model 40 can be configured with any Multibus-compatible CPU and with up to 16 Mbytes of memory (including iLBX support). A separate P2 module allows the customized interconnection of P2 backplane signals. Systems can include setups that are based on the 86/05, 86/35, or 286/10 CPUs. Memory options range from 512 Kbytes to 2 Mbytes of RAM.

The Foundation module is a single-board that does not require a Multibus backplane slot. Included in the module are Winchester, tape, and floppy disk controllers, plus hardware to operate a Support Monitor Subsystem. The Foundation module provides port-switching logic to control communication between the RS-232 port of a CPU board (or the RS-232 port of the Foundation module) and an external unit. The module connects to the backplane via two DIN two-piece connectors, so size and mating of the module differ from Multibus standards. It sports full software compatibility with the Intel iSBC 215/iSBX 218 combination.

The Support Monitor Subsystem is a group of diagnostic and monitoring programs residing within ROM on the Foundation modules. These programs oversee system parameters, run system diagnostics, perform backups, and format disks.

Flexible memory configurations are key to model 40 performance. A





"Chinese" menu of 5¼-in. Winches- and floppies, 8-in. floppies, and 5¼-in. tape drives highlight this offering. The integral 5¼-in. Winchester disk delivers fast data access—transfer rate is 625 Kbytes/s and average access time hits 30 ms—and provides a wide range of capacity choices. RMX-86 is offered for real-time applications, and a BIOS and utilities for CP/M-86 are also available. **Scientific Micro Systems, Inc**, 777 E Middlefield Rd, Mountain View, CA 94043.

Circle 260 —*J.V.*

Logic analyzer furnishes two oscilloscope channels

Designers can find both digital and analog test capabilities in the HP 1631A/D logic analyzer. Billed as the first logic analyzer with two digitizing oscilloscope channels, this instrument allows simultaneous cross-domain analysis of state, timing, and analog channels. By viewing timing and analog channels simultaneously, users can correlate parametric activity with hardware timing problems.

The two analog channels provide a 200 megasample-per-second digitizing rate. These channels permit simultaneous single-shot capture and storage of waveforms up to 50 MHz. Combined with pretrigger viewing, these features allow users to observe parametric faults.

Single-shot time interval measurements can be made with an accuracy of up to ± 1.5 ns. Such accuracy lets the engineer examine and characterize designs requiring critical pulse-edge placements. At the same time the engineer can also locate faults or measure hardware performance. Post-acquisition triggering allows the unit to compare data with a preset specification, and automatically retrigger if user criteria are not met. Specific events in time can be isolated rapidly using this "search and stop" technique. Single-shot, time-interval measurements can be specified, leading to automatic single-shot and repetitive measurements.

The 1631A provides 27 channels of state and 8 channels of timing, while the 1631D provides 27 channels of state and 16 channels of timing. Without the timing channels, the 1631A can provide 35 state channels, and the 1631D can provide 43 state channels. State channels have a bandwidth of 25 MHz, while timing channels provide 100 MHz with ± 10-ns resolution. A ± 1.5-ns resolution can be attained for single-shot measurements.

The 1631A/D is marketed as a general-purpose logic analyzer. This R&D debugging tool is ideally suited for system integration and characterization. The 1631A sells for $11,000, and the 1631D sells for $13,000. A disk drive ($1000) can supplement the volatile analyzer memory. **Hewlett-Packard**, 1830 Embarcadero Rd, Palo Alto, CA 94303.

Circle 261 —*R.G.*

Single-board supermicro handles 32-bit processing

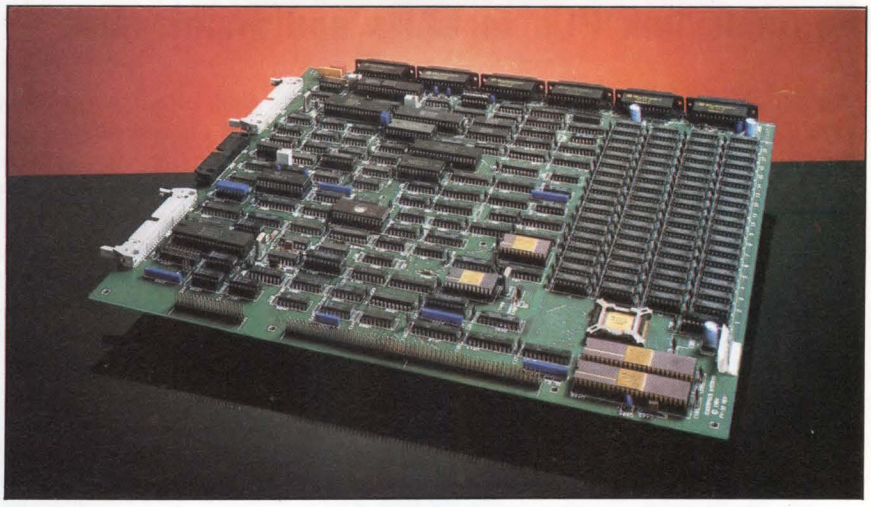
The dual-processor GS-32 is built around National Semiconductor's 32000 microprocessor series. A Z80B coprocessor handles onboard interfaces to hard and floppy disks, printers, and terminals. In addition, the board contains a memory management unit, a floating point unit, a timing and control unit, and a CPU.

With 512 Kbytes of onboard RAM (expandable to 2 Mbytes), the machine ensures that each byte is individually addressable and parity-protected. The virtual memory unit supports demand-paged virtual memory with access to 16 Mbytes. The MMU also sports extensive debugging and error trapping capabilities.

The I/O subsystem consists of the Z80B, a four channel DMA device, a floppy disk interface, an SCSI link, a 24-bit parallel port, six serial channels, an interrupt controller, and both local RAM and PROM. Character interrupts, echo, queueing, tab expansion, character translation, and line edits can be executed without

interrupting the main processor. The board becomes a complete system with the addition of a power supply, disk drives, and terminals. Single-card design eliminates the need for a card cage and motherboard, thus reducing the cost and size of a system. The system can, however, be expanded through either a proprietary bus or a compatibility module, which links the board with standard buses.

In addition to the bus, other features of the design are proprietary. A unique dynamic RAM controller design that uses a programmable logic array and random logic has jurisdiction over the 16 Mbytes of main memory. Another programmable logic array implementation allows a 16- or 32-bit system master. Also, the board incorporates techniques allowing an 8-bit microcomputer to achieve complete access over the 32-bit main memory of the CPU, as well as allowing a single 8-bit ROM to boot both the 8- and 32-bit micros.



Regardless of the availability of the 32032, the board can be used now for design-ins since it can implement the 32016 16/32-bit processor or the 32032 "true" 32/32-bit chip. The substitution is 100 percent software transparent. At higher speeds, the preferred processor is the 32032, with Texas Instruments named as a second source for the chip.

A single unit costs $5500 with 512 Kbytes of DRAM. **Goodspeed Systems, Inc**, PO Box 29, East Haddam, CT 06423.

—M.B.

Circle 262

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C68K-11/84

Systems link PCs to LANs and mainframes

Aiming a product at the IBM PC establishment can be a challenging development effort. Most companies would stumble at the prospect of introducing three new products to both software and hardware market targets—not so with the fledgling company, California Network Systems. This month it presents a family of products that link the PC, XT, or AT to the SNA world, as well as to local area networks outside the IBM realm.

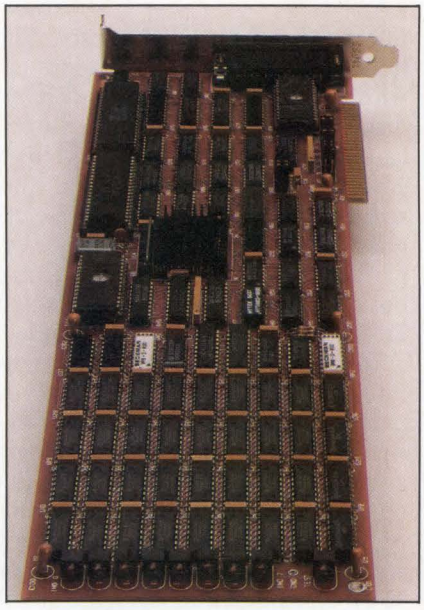
Hardware offerings consist of a ComCard communication card for the PC bus backplane that holds a 16-bit microprocessor supporting one channel of synchronous or asynchronous communication. The NetServer, a special-purpose communications processor, can support these cards, as well as several LAN interface cards. Basic systems include a 1-Mbyte floppy diskette drive and a backplane that supports up to 14 card slots wired on one bus.

To top it off, California Network Systems is introducing an OEM/SNA GateWay software package as an option on the ComCard. The package converts the IBM PC family into a gateway to SNA setups. The gateway also connects other workstations, printers, and related devices to the SNA network. Thus, the system emulates an IBM 3274 cluster controller with attached display stations and printers. Software provides standard session layer interfaces, including MSNET, IBM PC-LAN, NETBIOS, and a subset of CCITT X.25 session layer functions. The 80188 microprocessor onboard the ComCard supports the SNA/SDLC protocol at speeds up to 9.6 kbits/s.

Pricing for the ComCard is $990 in quantities of 250. The NetServer is priced at $2170. The initial OEM/SNA GateWay offering will be $580 for an eight-station configuration. **California Network Systems,** 372 Turquoise St, Milpitas, CA 95035.

—N.M.

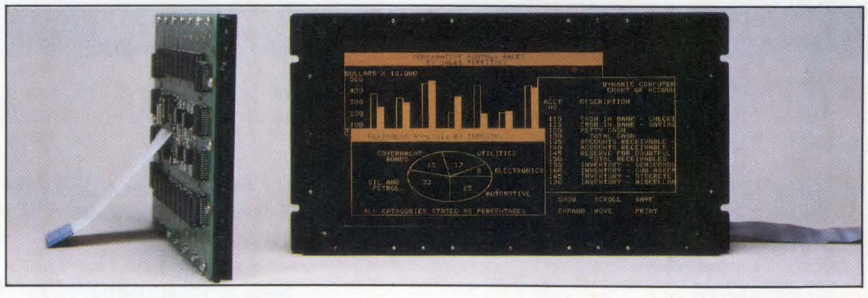
Circle 263



Full-screen EL panel stirs up display waters

Electroluminescent flat-panel displays possess an inherent complexity that probably precludes head-on competition with CRTs in mass markets. But, expected production volume upswings may significantly cut today's $700-plus price tags, according to James Hurd, president of Planar Systems, Inc. Hurd's firm has just announced a 25-line, 80-column EL display that is only 3/4-in. thick. It costs $775 in production volumes of 1000. "I would expect that high volume users will be paying about $250 for displays of this sort within two to three years," Hurd says.

To justify presently higher unit costs, makers of EL displays have turned to value-added techniques to reduce the cost differential versus competing technologies. This makes their displays more attractive on an overall systems cost basis. When drive and control circuits comparable to those provided with EL displays are added to CRT systems, the prices that Hurd projects will become more competitive. In applications where size, weight, and ruggedness are important factors, the EL displays may already be cost effective.



The EL6648 MX has been reduced to one-half the thickness of the original Planar panel, introduced last year. This size reduction resulted from the aggressive redesign achieved by Planar engineers, who used custom standard cell LSI and surface-mount techniques. The EL panel works in virtually all lighting conditions.

Designers can work with the same signals used to interface conventional CRT monitors because the EL6648 MX controller board converts signals provided by many standard CRT controllers. The 256-row x 512-columns of pixels are individually addressable and can provide excellent graphic displays. Planar's EL displays have also been environmentally tested and proven to withstand shocks of up to 100 G in all axes. Operating temperatures are rated between 0 and 55 °C. Overall dimensions are 10.3 x 5.7 x 0.75 in. and the unit weighs 16 oz. **Planar Systems, Inc,** 1400 NW Compton Dr, Beaverton, OR 97006.

—B.F.

Circle 264

Advanced touch screens expand input options

Smart-Frame touch input systems are lower cost, higher reliability touch screens. These products signal this technology's ascent to an important plateau. The number of parts (220) for this device is almost half the number its predecessor requires. Since this opto-matrix frame sports built-in intelligence, it does not require a controller to handle communication with a host computer.

Central to the input system is the opto-matrix frame. This frame contains the infrared LEDs and photo-transistor detectors. Encircling the screen of a flat panel or CRT display, the frame creates a transparent grid of infrared beams. When the beams are broken by the touch of a finger (or stylus), a command is sent to the computer to perform a predefined action. Microprocessors on the frame notify the host computer of touch activity and convey related messages among the host, application software, and the user.

Touch-screen devices find uses in many applications (eg, public information displays, database retrieval, and process control). Here, a Honeywell unit sports touch systems from Carroll Touch.

Smart-Frame features include improved ambient light compensation, which prevents adverse lighting conditions from affecting accuracy; enhanced resolution, which precisely defines the point of the stylus; and four operating modes (Enter Point, Exit Point, Track, and Continuous).

Reduction in the number of parts, use of automated test and insertion equipment, as well as rising volume requirements, have contributed to Smart-Frame price cuts. The Smart-Frame costs $595 for the 13-in. version and $795 for the 19-in. model. A 9-in. Smart-Frame, available next month, may be priced as low as $150 in high volume quantities. The 13- and 19-in. versions are scheduled for April and May, respectively. **Carroll Touch**, PO Box 1309, Round Rock, TX 78680.

Circle 265 —*J. V.*

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CIRCLE 87

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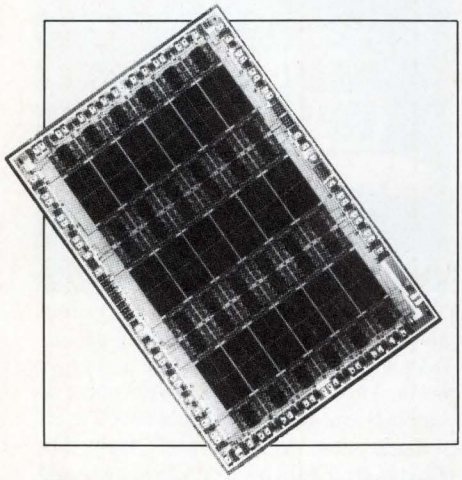
CIRCLE 88

Systolic array speeds high resolution imaging



The geometric arithmetic parallel processor (GAPP) provides 72 parallel processors on each IC for dramatic increases in image processing speed. Each GAPP IC contains a 6 x 12 array of 1-bit processor elements, each with 128 bits of local RAM. The GAPP ICs can be cascaded and large arrays can provide one processor per pixel for large images. The processors on each IC work in parallel. Instructions in the form of 13-bit control words are broadcast from the external control store to every processor element in the array. Each processor element executes 10 MIPS. Image data is input from one edge of the array and output on the opposite edge through a separate I/O bus that passes through the array. Thus, I/O can occur simultaneously with computation in the array. Samples are priced at $545 for an 84-pin ceramic pin-grid array package and $495 for an 84-lead plastic J-lead chip carrier version. **NCR Microelectronics**, 2001 Danfield Ct, Fort Collins, CO 80525. **Circle 266**

Bipolar macro arrays have internal gate delays of 800 ps

V1200, V1700, and V3500 bipolar macro arrays simultaneously interface with external ECL and TTL. High performance oxide-isolated, two-level metal process technology provides equivalent internal gate delays of 800 ps at 1 mW/gate. The V1200 has 1338 equivalent gates (maximum), the V1700 has 1712, and the V3500 has 3632. The arrays are composed of two basic cells: the logic cell and the I/O cell. Up to four adjacent cells can be utilized for physical macro placement without using routing channels. These arrays are available in a variety of packages including pin-grid arrays, leadless ceramic chip carriers, and ceramic DIPs. The V3500 is available starting in the second quarter. The other chips are available now. **Vatic Systems, Inc**, 761 University Ave, Mesa, AZ 85203. **Circle 267**

Dynamic RAM stores 64 Kbits, sports 150-ns maximum access time

A yield-enhanced high speed version of the MCM6665A incorporates a 150-ns maximum access time with low maximum power dissipation of 302.5 mW (active) and 22 mW (standby). This 64-Kbit HMOS dynamic RAM—dubbed the MCM4164BP15—features laser redundancy and smaller die size. With a 128-cycle, 2-ms refresh and fast page mode cycle time of 155 ns, the MCM4164BP15 maintains upward pin compatibility with the MCM4116 and MCM4517, and is TTL compatible. The part is available for $5.18 each in lots of 250 to 299. **Motorola Inc, Memory Products Div**, 3501 Ed Bluestein Blvd, Austin, TX 78721. **Circle 268**

Modem applications use SRAM with power-fail detection

A 16-Kbit static RAM is specially designed for battery backup protected memory. Designated the MK48C02, this component eliminates the need for external power-fail detection and battery switching circuitry. The MK48C02 has write-protection circuitry. A power-fail detect output can be used to disable other devices sensitive to low Vcc or to provide a power-fail output for system control. Intelligent terminal and modem applications especially suit the device. In 1000-piece quantities, MK48C02s are priced at $15.90 (150 ns), $12.60 (200 ns), and $12.25 (250 ns) each. **Mostek Corp**, 1215 W Crosby Rd, Carrollton, TX 75006. **Circle 269**

FIFO buffer sized at 128 x 8 bits can connect in series

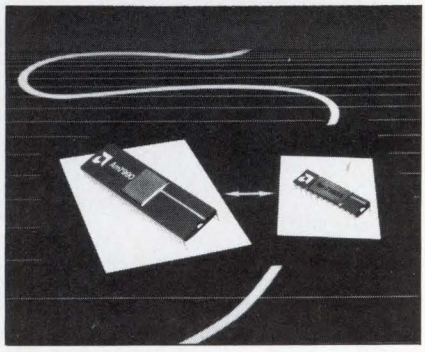
The Z8060 features bidirectional, asynchronous data transfer. This FIFO buffer and expander unit offers 128- x 8-bit buffer memory and three-state data outputs. A two-wire interlock handshake protocol also distinguishes the device. Any number of FIFOs can connect in a series to form a buffer of any desired length. Operating traits include 4- and 6-MHz clock frequencies, as well as −0.3- to 7-V maximum operating voltages. The Z8060 comes in 28-pin plastic or ceramic DIP. Samples are ready now. Devices cost $15 each in quantities of 1000 or more. **SGS Semiconductor Corp**, 1000 E Bell Rd, Phoenix, AZ 85022. **Circle 270**

Hybrid CMOS SRAMs with 100-ns typical access store 256 Kbits

Thick-film hybrid memories feature a low operating current of 40 mA and a typical standby current of 10 μA at 25 °C. Typical room temperature memory access time is 100 ns. Dubbed the CMOS 256-03 and CMOS 256-03M, these are static RAMs. The 256-03 combines four SMOS SRM2064 RAM chips and a 74SC138 decoder chip to produce an 8-bit word x 32-Kbit CMOS RAM. Standard 256-Kbit pinout is used. Hermetically sealed in a ceramic and metal package, the 256-03M is a high reliability, rigorously specified part. The 256-03 costs $297 each in lots of 100, while the 256-03M is $347. **Integrated Circuits Inc**, 10301 Willows Rd, Redmond, WA 98052. **Circle 271**

Version of the 80186 adds instructions to present set

The AMD 80186 is a highly integrated 16-bit microprocessor that combines 10 iAPX 86 components onto a single chip. Aimed at applications that include multitasking, industrial control, and graphics systems, the chip adds 10 instructions to the existing set, and is upwardly compatible with 8086 and 8088 software. Versions running at 6 MHz and 8 MHz are also available. The 10-MHz AMD 80186, packaged in a 68-pin leadless chip carrier, is priced at $98 each in 100-piece quantities. **Advanced Micro Devices, Inc**, 901 Thompson Pl, Sunnyvale, CA 94086.



Circle 272

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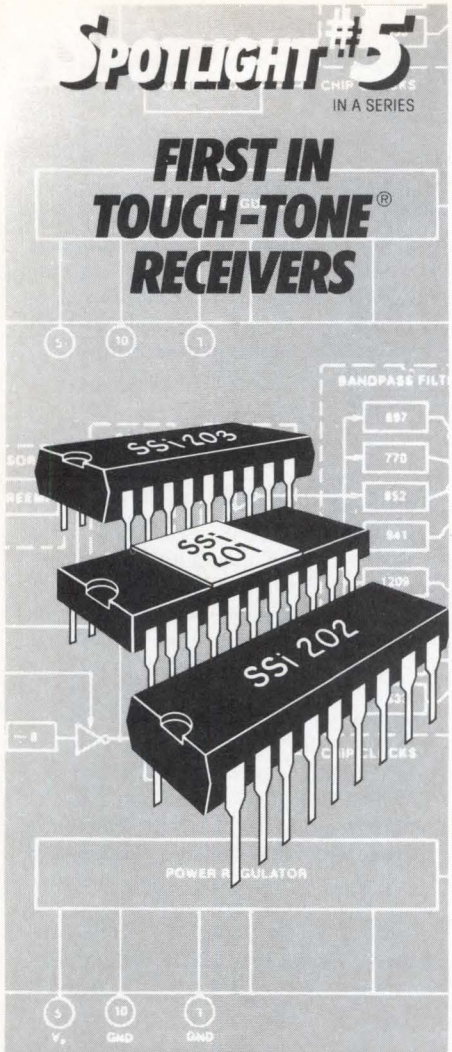

The SSI 201 DTMF receiver is the industry-standard one-chip solution for many telecom applications. It detects a selectable group of 12 or 16 digits, with no front-end filtering required. And its innovative design eliminates the need for all external components except a 3.58 MHz crystal and an inexpensive resistor.

The SSI 202 incorporates the features of the SSI 201 in a low-cost, 18-pin, plastic package. This lower cost unit also dissipates lower power and operates on 5 volts, making it compatible for use with microprocessors and suitable for consumer electronics. An additional "early detect" feature is provided in the SSI 203, the newest unit in SSI's growing line of Touch-Tone circuits.

To find out more about the industry's First Family of DTMF receivers, contact: **Silicon Systems,** 14351 Myford Road, Tustin, CA 92680, **(714) 731-7110** Ext. 575.

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CIRCLE 89

LSI-11/73-based design sports floor or rackmount configuration

LSI-11/73-based systems, designated the MDB-Micro/73s, contain a high speed Winchester disk subsystem with an 18-ms average access time. The systems provide a capacity of 67 Mbytes in RM03 emulation or 105 Mbytes in RM05 emulation mode. A streaming tape cartridge subsystem with 60 Mbytes of formatted capacity is also included. The 11/73 CPU has 8 Kbytes of cache memory, floating point instruction set, memory management for up to 4 Mbytes of memory, and a programmable line time clock. The standard MDB-Micro/73 is packed as a 5¼-in. rackmount unit, with floor mount pedestal configuration available. Systems are priced from $21,295 to $23,050, with discounts available. **MDB Systems,** 1995 N Batavia St, Box 5508, Orange, CA 92267.
Circle 273

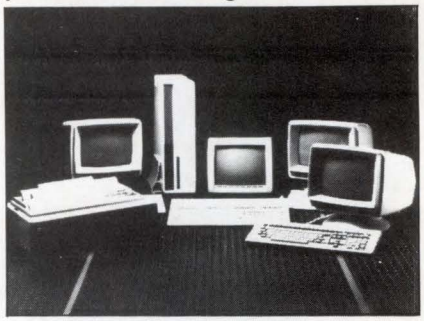
High end member joins PDP-11 minicomputer family

Rackmounting and free-standing configurations spell flexibility for the PDP-11/84 minicomputer. The central processor features the 15-MHz J-11 microprocessor chip set supporting the full PDP-11 instruction set (including extended and floating point instructions, memory management, dual-register set, 22-bit addressing, separate instruction and data space, and three operating modes). Both versions store a minimum of 1 Mbyte of memory. The complete PDP-11 operating system range is supported. Rackmount version costs $16,000. The free-standing (or subsystem-kernel) version is $20,000, with quantity discounts available. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754.
Circle 274

Lap system weighs in at 6 lb, 6 oz and features built-in modem

Communications and word processing power accentuate the IS-11C portable computer. A built-in modem is touted, as is a full-size (25 line x 80 char) LCD screen. The machine runs a 3.4-MHz CMOS Z80A and has a realtime clock. It weighs 6 lb, 6 oz. Internal NiCad batteries drive the unit, with an ac adapter/charger also available. Optional software resides on ROM cartridges. **Sord Computer of America, Inc,** 645 5th Ave, New York, NY 10022.
Circle 275

Supermicro gains high I/O performance running Unix on 68000



The PE 7350A supermicro system achieves high I/O and processing performance levels while supporting up to five users. This system uses a Uniplus port of Unix III and has a Motorola 68000 as its main engine. Memory sizes from 512 Kbytes to 3 Mbytes are supported, and users can choose a 15- or 28-Mbyte fixed disk, a floppy diskette, and monochrome or color graphics. This machine offers an optional IEEE 488 bus. The PE 7350A combines high speed dual memory bus architecture and 256-Kbit RAM chips for local memory. The 8-MHz processor operates without wait states. Programming languages supported include C, Fortran-77, Basic-Plus, and RM-Cobol. An Ethernet interface is anticipated. In 100-unit quantities, the basic 7350A is $3937, with a complete system costing $5115. **Perkin-Elmer, Data Systems Group,** 2 Crescent Pl, Oceanport, NJ 07757.
Circle 276

Voice recognition among input options on compact model

The Apricot Portable features voice recognition, an infrared keyboard and mouse/trackball, plus a full size 25-line x 80-col LCD screen. The machine weighs 13 lb. The 8086 resides at the heart of the unit, with 512-Kbyte RAM (expandable) and a 720-Kbyte, double-sided 3.5-in. disk drive. A color monitor can be attached, as well as a 10-Mbyte Winchester. This is an MS-DOS based machine. **ACT Computer (North America) Inc,** 3375 Scott Blvd, Santa Clara, CA 95054.

Circle 277

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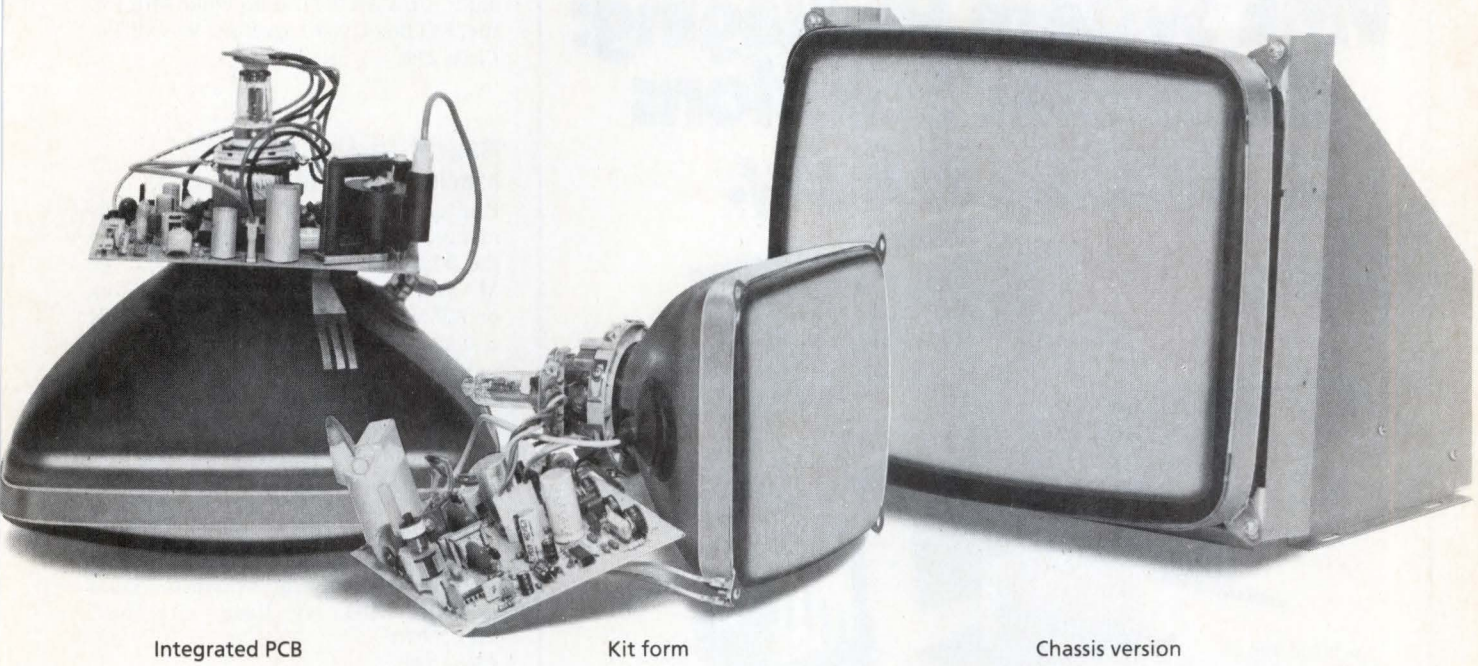

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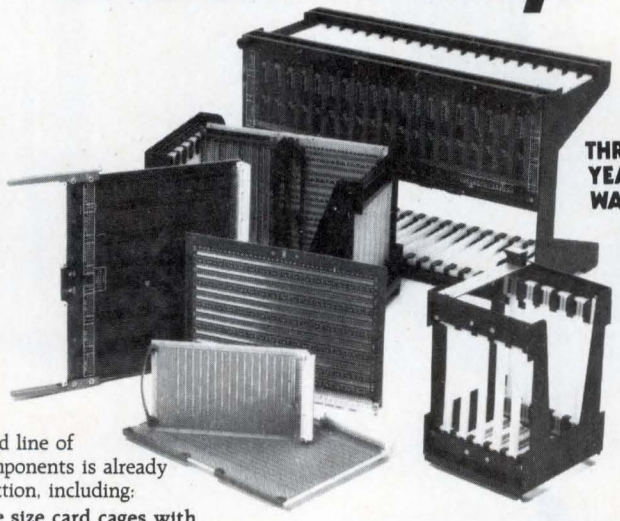
CIRCLE 90

Single-slot communications unit melds PC to controllers

The ICM-4 is a full size, single-slot communications board that plugs into the IBM PC. It handles serial communication between the PC and intelligent devices. The device provides four serial ports. Dual-ported, 8-Kbyte memory relieves the PC of character-interrupt chores. An onboard Z80 microprocessor manages protocols, data conversion, and message sequencing. Transmission rates from 300 bits to 19.2 kbits/s are supported. **Intellution, Inc**, 35 Perwal St, Westwood, MA 02090.
Circle 278

VME System Packaging: Electronic Solutions Makes it Easy.



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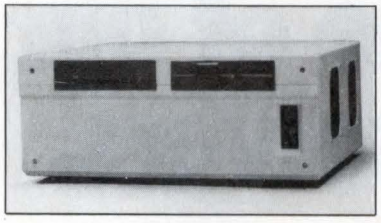

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Multibus is a trademark of Intel Corp.

CIRCLE 91

Data acquisition and control software simplify system operation

Monitoring and control, as well as data acquisition, are handled by the ProGen application software package. This software runs on the Fluke 2452 measurement and control system. With ProGen, users can program up to 500 I/O channels. Menu-prompted, the software requires no programming skills. It automatically chains scan tasks together, performs limit checking, and runs the defined procedures. Cost is $2990. **John Fluke Mfg Co, Inc**, PO Box C9090, Everett, WA 98206.
Circle 279

Material tracking module handles control of lots

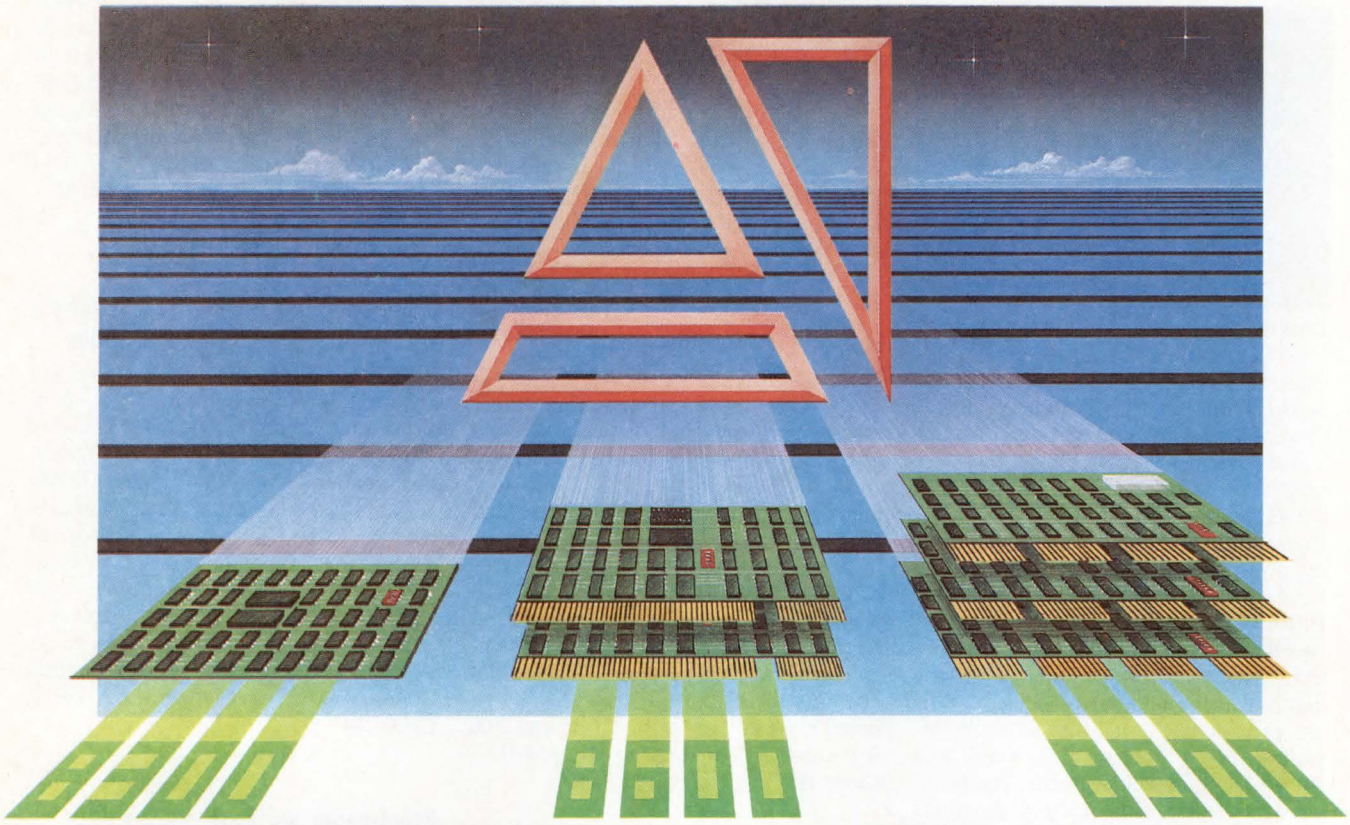
Production, material use and performance, and inventory are tracked using the Material Tracking module of the MAS-Manufacturing system. Operating on HP 3000 and the IBM 4300 and 30XX systems, the MAS-Material Tracking module handles lot control, lot traceablility, lot performance analysis, and by-product material resource planning. The module tracks the movement of purchased material lots from receiving, through issuance, to production while also providing traceability through the production process to eventual customer shipments. **Martin Marietta Data Systems**, 6303 Ivy Lane, Greenbelt, MD 20770.
Circle 280

Memory expansion units offer industrial-strength solutions

Three versions of the universal memory expansion board join the CMOS Industrial Microcomputer device family. The CIM-110 with no RAM installed, the CIM-114 with 32 Kbytes of RAM, and the CIM-118 with 64 Kbytes of RAM support any static memory device that meets JEDEC's 24- or 28-pin forms. The boards also support bank switching. **National Semiconductor Corp**, 2900 Semiconductor Dr, Santa Clara, CA 95051.
Circle 281

Let's hear from you
We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

The OEM's IBM Mainframe Connection



Auscom High-Speed Interfaces to The IBM Channel

Auscom offers a variety of solutions that permit direct connection of your devices to an IBM or FIPS-60 compatible channel. Why settle for slow serial connections when your product really needs high data transfer rates to maximize its capabilities? All of our channel interfaces appear as standard control units to the mainframe and require no changes to the host operating system. All are fully programmable.

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The 8300 Series is a single board not based on any external bus architecture. Transfer rates of up to 500K bytes per second can be achieved. It talks to a downline device via an 8- or 16-bit programmable parallel or serial interface. If necessary, the functionality of the 8300 can be put on your desired form factor or bus to facilitate incorporation directly into your device.

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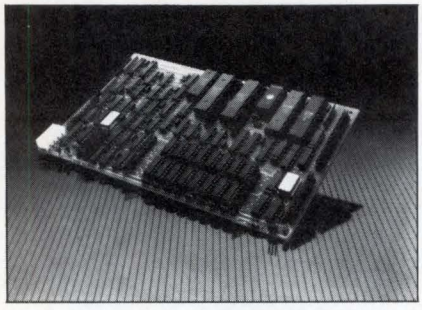
CIRCLE 92

Compact single-board units allow fast I/O transfers



DSB 6000 series microcomputers deliver I/O flexibility in an advanced, non-external bus design format. DSB 6000 boards reduce circuitry and heat generation, allowing fast I/O transfers. An onboard 50-pin expansion bus eases device interface. At the heart of the unit is a 6-MHz Z80B. The basic DSB 6000 configuration includes 128 Kbytes of 150-ns dynamic RAM (expandable to 256 Kbytes), 2 to 32 Kbytes of ROM or EPROM (expandable to 128 Kbytes), and two RS-232 serial ports. Additionally, a Centronics parallel port, onboard floppy disk controller and hard disk SASI port are provided. Compatible software includes CP/M 2.2 and 3.0, Oasis and Turbo-DOS, as well as Forth. The product costs $695, with quantity discounts available. **Davidge Corp**, 1951 Colony St, Mountain View, CA 94043.
Circle 282

Based on the 68010, VMEbus board has 4-Kbyte associative memory

Image processing, communications and industrial control applications stand out among uses for the MVME120 board. This is a VMEbus-compatible microprocessor board, based on the 68010, that provides a 4-Kbyte associative memory (or cache) for improved program execution. The basic board has 128 Kbytes of dual-ported dynamic RAM for reduced bus loading. An MC68451 memory management unit is also onboard. This system is supported by realtime Versados Release 4.4. **Motorola Semiconductor Products, Inc**, PO Box 20912, Phoenix, AZ 85036. **Circle 283**

AT-compatible board claims storage expansion to DOS 3.0 limits

Maestro multifunction boards from Tecmar add memory power to the IBM PC AT. Expansion on Maestro provides two memory blocks. The first upgrades the AT to a maximum of 640 Kbytes of RAM, which Tecmar indicates is the maximum memory that DOS 3.0 can use. The second block is upgradable to 2 Mbytes of memory. (This latter block can be upgraded using 64- or 256-Kbit chips.) Single-board design saves real estate and cuts heat dissipation. Parallel and serial ports can be used to connect printers, plotters, modems, and mice. **Tecmar, Inc**, 6225 Cochran Rd, Solon, OH 44139.
Circle 284

Full 32-bit Multibus board features NCR/32 chip set

The NCR/32-796A consists of three members of the NCR/32 chip set: the microprogrammable central processor chip, the address translation chip (for memory management), and the extended arithmetic chip (which operates as a floating point math booster). External microprogrammability is supported with 16 Kwords of RAM microcode instruction storage. There is also a 128-word scratchpad memory. Dual-port main memory can be accessed via the Multibus or iLBX. The board is priced at $4995. **NCR Corp**, 1700 S Patterson Blvd, Dayton OH 45479.
Circle 285

SOFTWARE

Multitasking MS-DOS and Xenix combine via interpreter system

The Poppy OS software package allows MS-DOS-based software to run under the Xenix operating system. Single-user MS-DOS applications programs can thus migrate to a 12-user setting. Poppy OS is an MS-DOS interpreter, operating as a Xenix shell. The shell enables MS-DOS-based software to work on the Durango Poppy 286/186 Xenix 80286-based system, as though it were operating under MS-DOS. **Durango Systems, Inc**, 30003 N First St, San Jose, CA 95134.
Circle 286

Potent Ada development package available for VAX/Unix

The Verdix Ada Development System (VADS) centers on a production-quality Ada compiler, which is fully compliant with ANSI/MIL-STD-1851A. The system includes the compiler, debugger, program library utilities, and runtime system. The compiler system operates on any DEC VAX-11/7XX series computer running under Unix 4.2 BSD. The compiler operates as a reentrant process that can be shared under Unix. It makes full use of Unix facilities. The compiler, on a typical VAX-11/780, is said to process an average of 1000 Ada source statements per minute. **Verdix Corp**, 7655 Old Springhouse Rd, McLean, VA 22102.
Circle 287

Cobol compiler highlighted by access and display management utilities

Programmers can easily create a variety of screen displays using the display manager utility within the DR Level II Cobol compiler. This compiler meets ANSI specifications. An access manager utility also marks this product. Access management provides a versatile file access method for maintenance of data records. DR Level II Cobol supports the PC-DOS and MS-DOS operating systems and generates native code for iAPX series 16-bit microprocessors. Price is $700. **Digital Research**, Box DRI, Monterey, CA 93942.
Circle 288

Proofreader software spotlighted by use of AI techniques

RightWriter provides automatic document proofreading on the IBM PC and PC compatibles. This software package uses artificial intelligence to analyze documents for errors in grammar, punctuation, and style. Software works with WordStar and other word processors, requiring only one additional command. RightWriter flags wordy phrases, weak sentences, and overused words. It calculates the reading grade level of the document using the MIL-M-38784B standard. Price is $75. **Decisionware, Inc**, 4030 Gulf of Mexico Dr, Longboat Key, FL 33548.
Circle 289

WordStar update adds the 3270 PC to machines it covers

WordStar Professional software for the IBM PC now enables the program to run during micro-mainframe sessions. Windows supported by the 3270 PC also can run simultaneously with WordStar. Printers in the NEC line, plus TI 855, and others are supported by the software program. **MicroPro International Corp**, 33 San Pablo Ave, San Rafael, CA 94903.
Circle 290

THE NEW PCI-20000 FOR PERSONAL COMPUTERS. MODULAR I/O YOU CAN NEVER OUTGROW.

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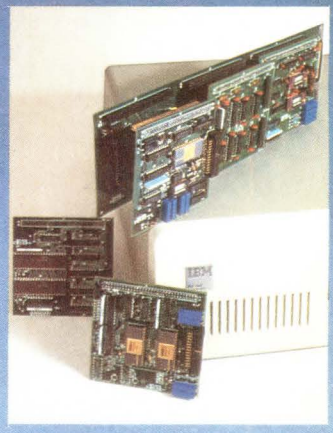

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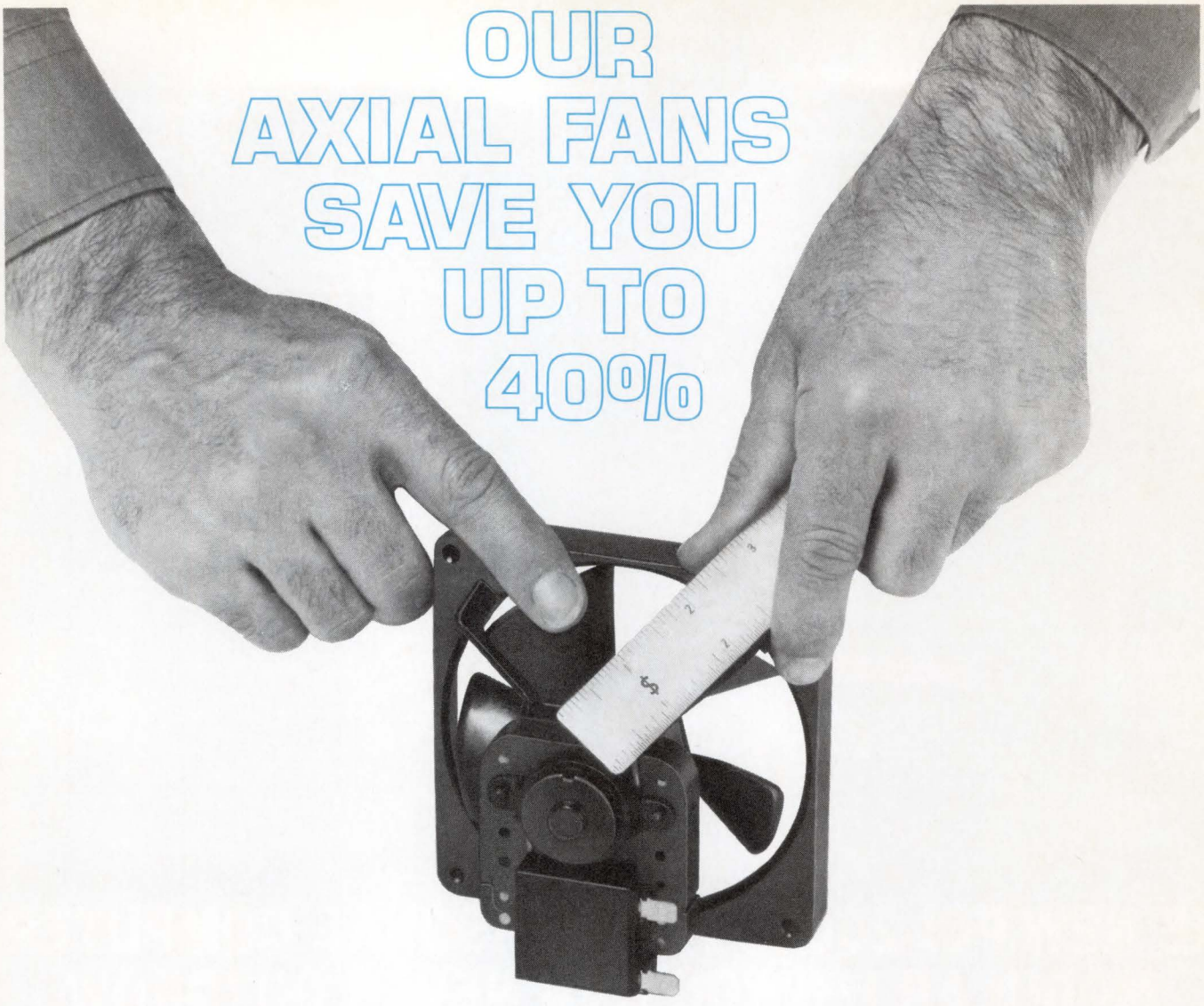

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CIRCLE 94

High resolution device delivers low cost image scanning

With quantity price set under $1000, the MS-200 expands image scanning applications. The MS-200 accepts documents sized at up to 8½ x 24 in. and digitizes the image at a 200-pixel/in. resolution. It then transfers the image to host computer memory. Switch-selectable scanning modes include text, picture, and mixed modes. The MS-200 scanner performs Group 3 1-D CCITT data compression at a 10 to 1 ratio for text and comparable compression for graphics. This compact device uses state-of-the-art sensor array and image processing techniques. **Microtek Lab Inc,** 17221 S Western Ave, Gardena, CA 90247.

Circle 291

Liquid crystal shutter featured in intelligent printer

Electrophotographic technology combines with a liquid crystal shutter (LCS) in a laser printer known as the GQ-3000. The unit prints 7 pages/min with character density of 240 dots/in. It has a photo receptor drum with a minimum life span of 60,000 prints. Any font or type of character can be downloaded into a 128-Kbyte RAM. The machine is capable of portrait (vertical) or landscape (horizontal) printing, gray scaling, underlining, and justification. The LCS page printer interfaces via standard 8-bit parallel and RS-232-C links. The unit is 17-in. high and weighs under 100 lb. Prices range from $4000 to $4500. **Epson OEM Products Div,** 23600 Telo Ave, Torrance, CA 90505. **Circle 292**

Scanner creates electronic files from diverse sources

Automatic graphic digitizing and text input is provided by the Personal Scanner. The device converts drawings, photographs, typewritten documents and other visual material into electronic files. This system provides both optical character recognition input and image processing capabilities in a single unit. Personal Scanner hardware consists of a desktop scanner, a cable, and a half-size interface card for the PC or XT microcomputers. Interfacing to Apple and Motorola 68000-based machines is planned. Unit price is $2487. **Electronic Information Technology, Inc,** 373 Route 46 W, Fairfield, NJ 07006.

Circle 293

Handheld unit tackles problems in the field

The IXO TC2000 provides full upper and lower case ASCII capabilities from a tactile typewriter-style keyboard. It links over the phone to a remote host or locally via RS-232-C and cable. The TC2000 can auto-dial, log on, receive, verify, and display messages from any host computer. From 1200 to 8000 characters of data received can be saved in memory and reread after disconnection. The TC200 costs $395. **iXO, Inc,** 5757 Uplander Way, Culver City, CA 90230. **Circle 294**

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Repair station software links with testers and central data base

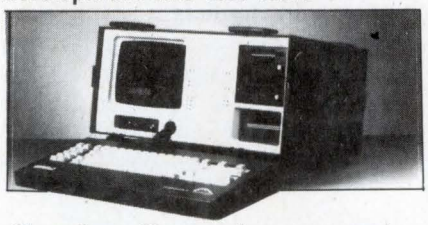
A software package for the 700 Net Workstation allows interaction of subassembly repair data to interact with the 700's relational data base. The software provides improved repair station throughput, plus greater production control and manufacturing productivity. Known as Zehntel Iris, the software creates an electronic link that unites the tester, repair station, and central data base. Data entry can be done via a bar-code reader. Iris can handle input from multiple in-circuit test systems (including the 310, 800, 810, and 860) connected via Ethernet or RS-232-C links. This software package is standard with purchase of the 700 Net Workstation. The dedicated repair station terminal, which includes a color CRT with light pen interface and bar-code reader with wand, sells for $7695. **Zehntel Automation Systems,** 2625 Shadelands Dr, Walnut Creek, CA 94598. **Circle 297**

In-circuit VLSI tester option handles wide bus structures

Synchronous logic tester modules provide intelligent control of each test pin in a Marconi in-circuit printed circuit board test system. The SLT option allows flexibility in complex (16- to 64-bit wide) board testing. It incorporates a 1-Kbit x 4-bit RAM chip behind each test pin with a separate 1-Kbit x 32-bit control RAM that allows conditional branching, subroutine loops, and other functions. This allows the chip to maximize data handling and limit the program code necessary for complex testing. The SLT consists of an interface to the test system controller, a microprogrammed bit-slice microprocessor, test point switching modules, and a power supply. Synchronization goes up to 16 MHz. Price is $23,000. **Marconi Instruments, Automatic Test Equipment Div,** PO Box 60279, Sunnyvale, CA 94088.

Circle 296

Data comm protocol unit handles development and test tasks



Chameleon IIs are data communication protocol simulator/analyzers that include a realtime clock board and diverse protocol support software. Realtime analysis, automatic program loading, automatic remote functions, and simple menu presentation are featured. Software additions include X.25 statistics, SDLC statistics, and Direct-to-Disk analysis. Priced at $19,500, the Chameleon II basic systems include 92-key keyboard, dual 3.5-in. drives, 74-Kbyte RAM, 40-Kbyte PROM, and status LEDs. **Tekelec Inc,** 2932 Wilshire Blvd, Santa Monica, CA 90403.
Circle 295

Reliability software automates prediction of product operation

RelCalc 2 features an automated MIL-HDBK-217D part stress procedure. It allows easy integration of reliability considerations into the design process. RelCalc 2 provides part-forms with menu windows for each entry field, global editing functions, reports that organize results for quick analysis, and fast error trapping. RelCalc 2 runs on the IBM PC/XT and costs $1500. A $50 demo package is also available. **T-Cubed Systems,** 31220 La Baya Dr, Westlake Village, CA 91362.
Circle 298

Workstations offer easy upgrade from 2-D to 3-D

Progressive degrees of 2-D and 3-D performance are provided by the 4120 Series of color graphics workstations. The 4125, 4128, and 4129 Graphics Workstations feature 2-D, 3-D wireframe, and 3-D solid shading capabilities, respectively. These stations include 80286/80287 microprocessors for high performance graphics. Host communication is provided over an RS-232-C link at speeds up to 38.4 kbaud. The series is compatible with 4100 and 6000 workstations. The 4120 series uses a 60-Hz noninterlaced display with a 1280- x 1024-pixel resolution. Models include local pan and zoom, rotation, and convergence correction capabilities. The 4129 aims at the mechanical engineering market. It includes 16 predefined translucency patterns so users can see through 3-D surfaces. Dithering provides smooth transition of colors, and allows the user to perceive up to 1024 separate shades. Local lighting sources and shading effects are user controllable. The 4125 has the same display, processors, keyboard, and 2-D performance as the 4128 and 4129. It is aimed at electrical engineering and mechanical engineering applications. The 4125, 4128, and 4129 are priced at $19,950, $25,000, and $35,000. **Tektronix,** Box 500, Beaverton, OR 97077.
Circle 299

Scope melds waveform capture and logic triggering

The HP 54200A/D is a fully programmable, 200 megasample per second digitizing oscilloscope. Especially apt in uncovering transient fault conditions, the machine captures transients as narrow as 10 ns. A 50-MHz bandwidth combines with various automatic measurement capabilities, as well as sophisticated triggering modes. Pretrigger viewing allows the R&D engineer to see what happened before the trigger event. A designer can trigger on a fault, then look back in time to find its cause. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.
Circle 300

Computer aided drafting system runs on low cost micros

The CAD Graphics System is a general purpose program that allows creation of a wide variety of drawings through a keyboard or digitizing tablet. AutoCad, which provides onscreen menus, is integral to this system. Full bidirectional zoom allows the user to work on a drawing at any level of detail. Eight colors can be used with AutoCAD, which is fully compatible with the Heath/Zenith Z-100 series computer. **Heath Co,** PO Box 1288, Benton Harbor, MI 49022.
Circle 301

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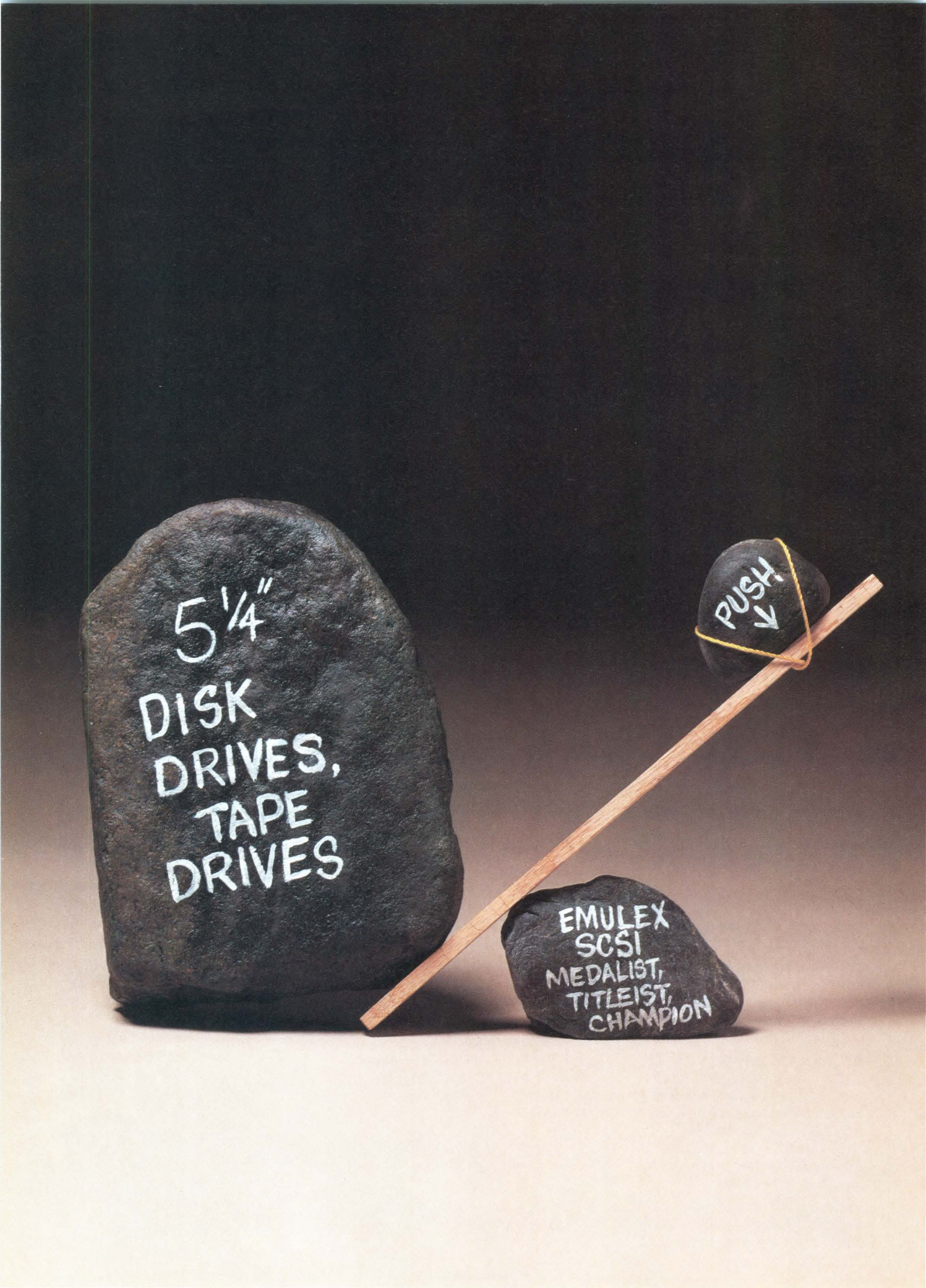
CIRCLE 96


5¼"
DISK
DRIVES,
TAPE
DRIVES
PUSH
EMULEX
SCSI
MEDALIST,
TITLEIST,
CHAMPION

EMULEX'S LEVERAGE GIVES COMPUTER MANUFACTURERS TOTAL SCSI CONTROL.

INTRODUCING MEDALIST, CHAMPION AND TITLEIST

With Emulex's wide range of SCSI controllers for both disk and tape, you now have the leverage you need to boost real I/O power and flexibility into your system's design.

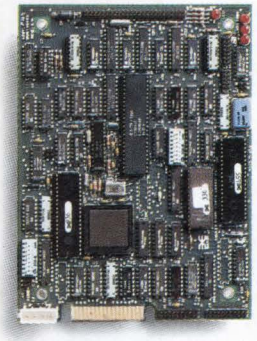
Our compact Medalist, Champion and Titleist controllers give you this leverage through a long list of high-performance features. Features everyone has learned to expect – and get – from Emulex.

Our SCSI-based micro-controllers offer you a convenient vehicle to build, update, mix or interchange different types of peripheral storage devices to your mini/micro computer systems. With Emulex's unique commitment to full SCSI development and support, the Medalist, Champion, and Titleist take advantage of the widest range of advanced SCSI enhancements. Enhancements like arbitration, disconnect/reselect, and full SCSI Copy.

All of these powerful controllers include the following high-performance features that give you extra leverage.

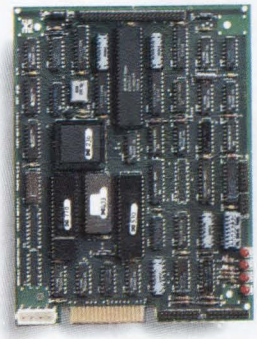
- Custom MOS VLSI chips that increase reliability, reduce power consumption and lower costs.
- A 14 KB data buffer to ensure high performance in disk and tape operations.
- Support of two ST506, or ESDI drives and one ¼" tape drive.
- Automatic self-test as part of each power up.
- On-board operation configuration switches.
- Fault and activity LEDs.
- An on-board front panel connector for drive status indications.
- Medalist and Champion controllers perform defect media management.
- Only +5 VDC power required.*

Now let's take a closer look at the specifics of each new Emulex controller.



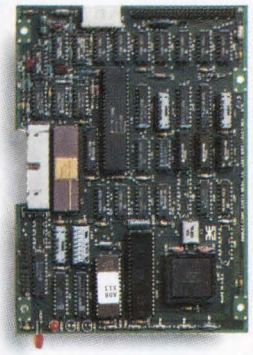
MEDALIST ST506/SCSI DISK CONTROLLER.

The Medalist combines SCSI with the popular ST506 Winchester disk drive interface. This gives you a wide selection of full or half-height 5¼" disks to choose from, varying in capacity from 5 to 140 megabytes. The Medalist also supports 16 Read/Write heads.



CHAMPION ESDI/SCSI DISK CONTROLLER.

With Champion, you can interface two serial-mode ESDI 5¼" Winchester drives to the SCSI bus. These large capacity drives support up to 10 MBits-per-second disk transfer rates, higher bit densities per track and range from 110 to 380 megabytes. The Champion also features hard and soft sectoring capability.



TITLEIST TAPE/SCSI CONTROLLER.

Titleist is a high-performance, ¼" streaming tape controller compatible with the QIC-24 standard tape data format. The versatile Titleist controller has been quality engineered to interface to most of today's popular ¼" streaming tape drives of various capacities.

OTHER EMULEX/SCSI PRODUCTS THAT ADD TO YOUR LEVERAGE.

Emulex/SCSI host adapters are available for Q-Bus and Unibus systems, IEEE 796 Multibus systems, the IBM PC, PC/XT and PC/AT and "compatibles." User-developed SCSI host adapters developed by other vendors are also viable for use with Emulex/SCSI controllers.

GET YOUR MAXIMUM SCSI LEVERAGE FROM EMULEX.

With Emulex's unparalleled commitment to full SCSI development and support, and with our wide range of products, you have the leverage you need for full SCSI control.

For detailed information on Emulex/SCSI products, call toll-free (800) 854-7112. In California (714) 662-5600. Or write Emulex Corporation, 3545 Harbor Blvd, P.O. Box 6725, Costa Mesa, CA 92626.

EMULEX®

*Titleist MTO2 requires +12 VDC.

CIRCLE 97

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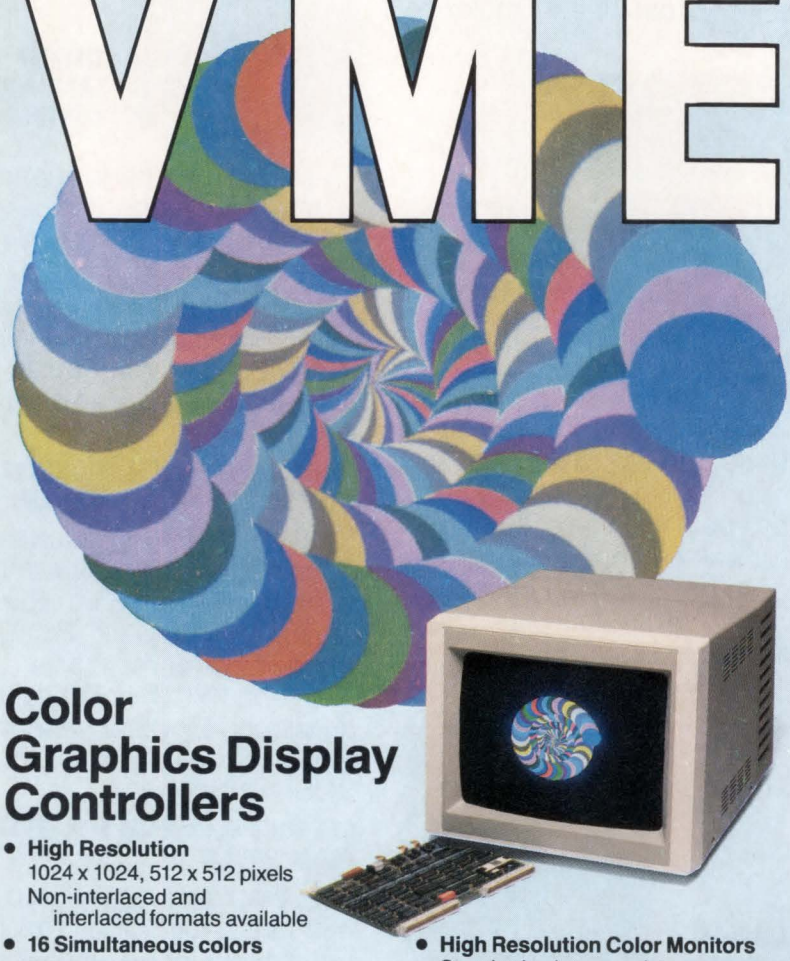

Color Graphics Display Controllers

- **High Resolution**
  1024 x 1024, 512 x 512 pixels
  Non-interlaced and interlaced formats available
- **16 Simultaneous colors**
- **Blink at 1 Hz**
- **High Performance**
  Graphics generated at up to 1,200,000 pixels-per-second
  Fill operations at up to 19,200,000 pixels-per-second
  All planes drawn simultaneously
  Line by line vertical scroll
  Multiple cursors
- **GPS Subroutine Package**
  Available for popular operating systems
- **Other bus architectures available**

- **High Resolution Color Monitors**
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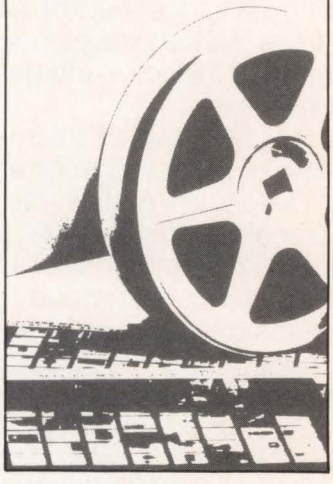

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CIRCLE 98

LITERATURE

Interconnection buzzwords

A glossary of Interconnection Buzzwords updates terms, phrases, symbols, acronyms, and definitions proliferating in the interconnection/backpanel industry. **Elco Corp,** Santa Ana, Calif.
Circle 410

Gate arrays

NEC's gate array product line is outline in a 12-page, four-color brochure. Charts show interface options, technologies, and densities available. CMOS, TTL, and ECL technologies are utilized in the semicustom IC line. **NEC Electronics Inc,** Mountain View, Calif.
Circle 411

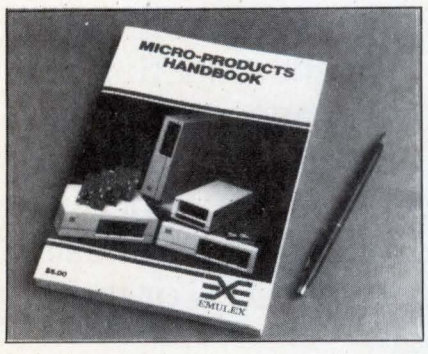
Protocol analyzers

Comstate II high level protocol analyzers are pictured in a four-page color flier. The devices sport diverse testing abilities and are highlighted by a wide test library. **Atlantic Research Corp,** Alexandria, Va.
Circle 412

Imaging applications

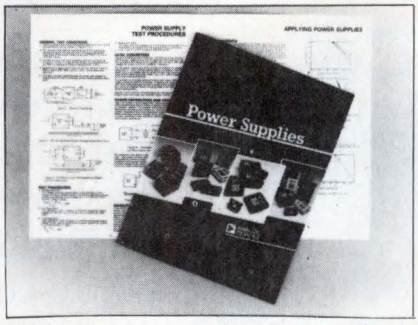
Application and performance details on the Quantimet 920 advanced image analyzer compose a 12-page booklet. Dual, flicker-free, high resolution color displays join image editing and digitizing tablet enhancements to complete this unique system. **Cambridge Instruments, Inc,** Monsey, NY.
Circle 413

Interfacing systems



The *Micro-Products Handbook* provides information on a line of host adapters, disk and tape controllers, micro subsystems, and the Persyst line of products for the IBM PC. Most products highlighted implement the SCSI standard. Qualified technical users can request this material by writing on their company letterhead to **Emulex Corp**, 3545 Harbor Blvd, PO Box 6725, Costa Mesa, CA 92626.

Power supplies



Analog Devices' catalog features linear ac/dc power supplies and modular dc/dc converters. Data on transients and a chart listing several protective devices commonly employed by circuit designers mark this document. **Analog Devices,** Norwood, Mass.
Circle 414

Realtime CAD

Free, color technical tract describes the design, features and capabilities of the MC-500 32-bit realtime system. Ten pages illustrate system details and applications (eg, CAD, CAM, and CAE). **Masscomp,** Westford, Mass.
Circle 415

Backplane packaging control

In-house backplane building, testing, and servicing capabilities from Stanford Applied Engineering are described in a brochure. Custom or standard PC board and metal backplane manufacturing, connector and IC packaging system construction, multilevel testing, and backplane-chassis integration are shown. **Stanford Applied Engineering,** Santa Clara, Calif.
Circle 416

Semiconductor newsletter

Harris Semiconductor now offers a newsletter devoted to reporting developments in its wide range of IC offerings. The first issue highlights the CMOS 80C80 and 80C86, which have made a splash in the portable marketplace. **Harris Semiconductor,** Melbourne, Fla.
Circle 417

Cobol generator

A 12-page booklet details features, functions, and benefits of PROMACS/CICS—a structured CICS command level Cobol generator. Examples of the free-form, nonprocedural language and the structured code generated with inline documentation are included. **MACS/Management and Computer Servics, Inc,** Valley Forge, Pa.
Circle 418

In-circuit emulators

Literature describing a line of realtime in-circuit emulators centers on support for Intel's 16-bit microprocessors. Realtime clock speeds, menu-driven interfacing, and emulator configuration techniques are detailed. **Microcosm, Inc,** Beaverton, Ore.
Circle 419

IEEE 488 interface bus

The emerging GPIB (IEEE 488) standard is pictured, as is a line of GPIB interface boards, in a free catalog. Bus extenders, controllers, and testers are also covered. **National Instruments,** Austin, Tex.
Circle 420

Personal computer vision

A 16-page, full-color brochure explains the PC-Eye video capture board which, along with the IMiGIT icon-driven graphics system and PhotoBase software, merges pictures with data bases for diverse applications on the PC. **Chorus Data Systems,** Merrimack, NH.
Circle 421

Data comm applications guide

Network planners can enhance their understanding of T1 using the *T1 Voice/Data Applications Guide* from Coastcom. Off-premise extensions, drop-and-insert networks, PBX tie-lines, and CAD/CAM applications are covered. **Coastcom,** Concord, Calif.
Circle 422

Industrial automation

A line of programmable data acquisition and control systems, which aim at automating test and other operations in the industrial environment, are depicted in a brochure. **CompuDAS Corp,** Ithaca, NY.
Circle 423

Image composer

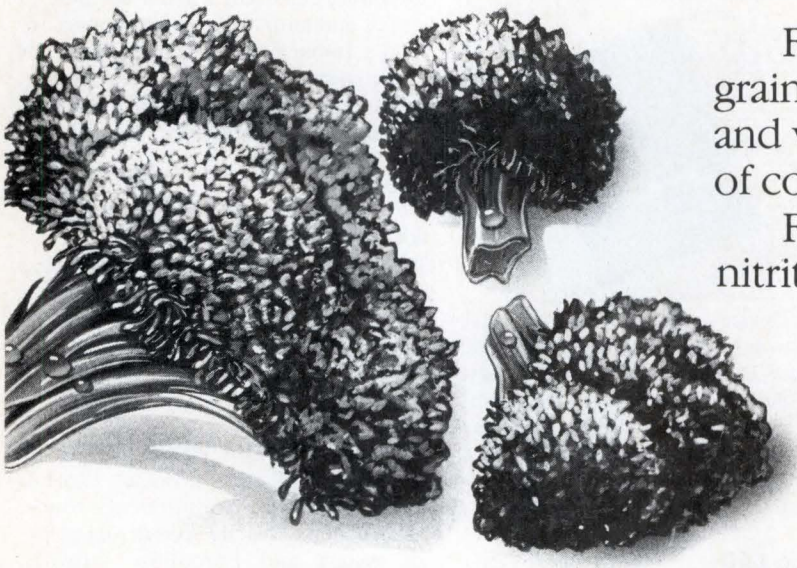
A complete text and image pagination system, the Royce Image Composer, is described in a 16-page pamphlet. Illustrations detail the system's interactive display and user-definable programming routines. **Royce Data Systems,** Inc, Hopkinton, Mass.
Circle 424

Personal PC board CAD system

A hardware/software combination for computer aided design is presented in a four-page format. Running on the PC and XT, the system features joystick control, onscreen menus, and a built-in communications package. **TIW Systems, Inc,** Sunnyvale, Calif.
Circle 425

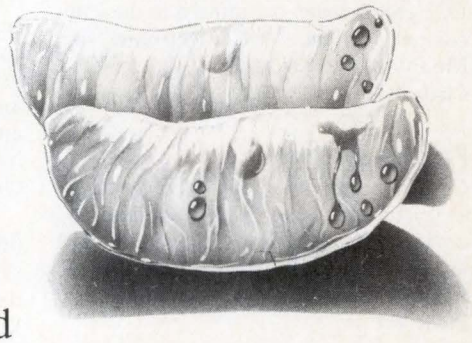
THIS SPACE CONTRIBUTED AS A PUBLIC SERVICE

A defense against cancer can be cooked up in your kitchen.



Fruits, vegetables, and whole-grain cereals such as oatmeal, bran and wheat may help lower the risk of colorectal cancer.

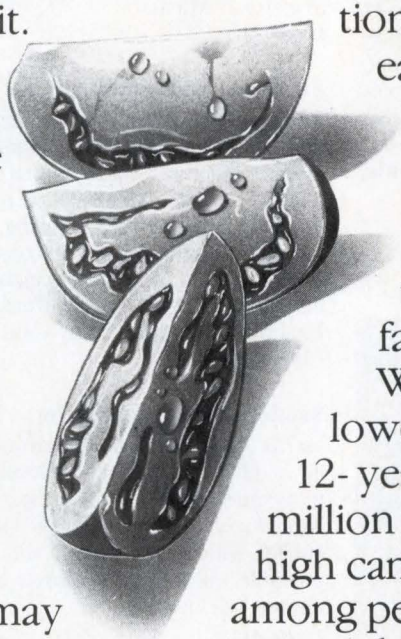
Foods high in fats, salt- or nitrite-cured foods like ham, and



fish and types of sausages smoked by traditional methods should be eaten in moderation.

There is evidence that diet and cancer are related. Some foods may promote cancer, while others may protect you from it.

Foods related to lowering the risk of cancer of the larynx and esophagus all have high amounts of carotene, a form of Vitamin A which is in cantaloupes, peaches, broccoli, spinach, all dark green leafy vegetables, sweet potatoes, carrots, pumpkin, winter squash and tomatoes, citrus fruits and brussels sprouts.



Be moderate in consumption of alcohol also.

A good rule of thumb is cut down on fat and don't be fat.

Weight reduction may lower cancer risk. Our 12- year study of nearly a million Americans uncovered high cancer risks particularly among people 40% or more overweight.

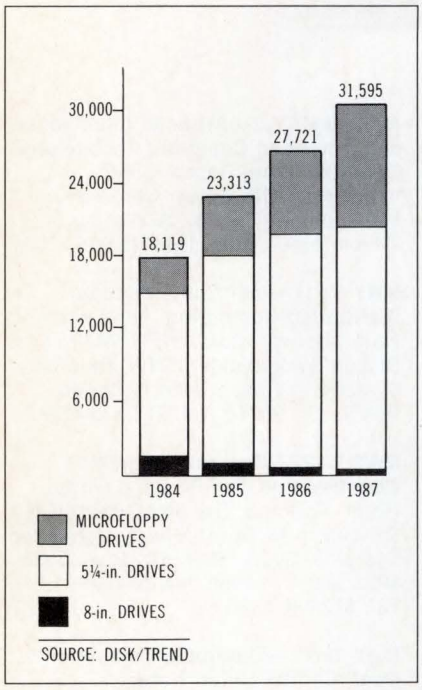
Foods that may help reduce the risk of gastrointestinal and respiratory tract cancer are cabbage, broccoli, brussels sprouts, kohlrabi, cauliflower.

Now, more than ever, we know you can cook up your own defense against cancer. So eat healthy and be healthy.

No one faces cancer alone.

AMERICAN CANCER SOCIETY®

Flexible disk drives



Worldwide flexible disk drive shipments exceeded 12.5 million units in 1983, with a 44 percent increase estimated for 1984, according to the *1984 Disk/Trend Report* on flexible drives. For 1987, the *Disk/Trend* prognosticators anticipate worldwide unit shipments of over 31.5 million drives, valued at $4.7 billion. The report also concludes that half-height models will compose 99.7 percent of the 5¼-in. floppy drive market in 1987, with PC AT-type, two-sided, 1.6-Mbyte, 5¼-in. floppies accounting for about three-quarters of the two-sided 5¼-in. sector in 1987. Microfloppies currently represent the fastest growing segment, reaching annual sales of 9.7-million units in 1987. The report also concludes that IBM will ramp-up internal production of drives this year. Subscriptions to the *1984 Disk/Trend Report*, including both the rigid and flexible disk drive sections, are available for $1530. Separately, the flexible disk drive report costs $775. **Disk/Trend, Inc,** 5150 El Camino Real, Los Altos, CA 94040.

Circle 469

Design automation

Estimated revenues for the CAD/CAM/CAE industry segment in 1984 were $2.8 billion according to Daratech, Inc. This implies a prodigious 52 percent annual growth rate. The firm put the annual growth rate for 1983 at 40 percent. Central to the increase are surges in the CAE/CAD speciality sector, where sales of electronic circuit design systems grew at a 180-percent clip and accounted for 8 percent of the $2.8 billion total. Systems based on personal computers also exhibit major strength. Personal computer-based systems for mechanical and architectural drafting, solids modeling, and electronic circuit analysis and layout accounted for $40 million of 1984 revenue. This survey of CAD/CAM/CAE reviews 114 vendors and 236 systems. A one-year subscription costs $368. **Daratech, Inc,** 16 Myrtle Ave, PO Box 410, Cambridge, MA 02238.

Circle 470

Artificial intelligence

Total artificial intelligence industry revenues will exceed $375 million in 1985, according to DM Data, Inc, an Arizona consulting group that focuses on AI. The firm sets AI industry revenues (primarily measuring the software value of the open market companies, excluding computers) for 1984 at $200 million. This year will be a shake-out year, the firm notes, with some of the initial AI products floundering partly due to incomplete programs and overstated capabilities. A one-year subscription to DM Data's *AI Trends* newsletter is $295. **DM Data, Inc,** 6900 E Camelback Rd, Scottsdale, AZ 85251.

Circle 471

Printers and graphics

Ink-jet and thermal printer technologies will exhibit substantial gains through 1987, according to Datek Information Services. However, the firm does not expect thermal transfer to grab a major market share in the monochrome or color graphics printer market. In *Graphics and Color Hardcopy*, Datek estimates that thermal transfer color printers will achieve a 15-percent share of color printer types shipped in 1987, with impact dot-matrix printers garnering a 43 percent share, and pen-plotter and ink-jet technologies each holding 20 percent of a 1.34-million unit total. The report's authors see market log-jams breaking as graphics standards emerge. **Datek Information Services, Inc,** PO Box 68, Newtonville, MA 02160.

Circle 472

Semiconductor industry

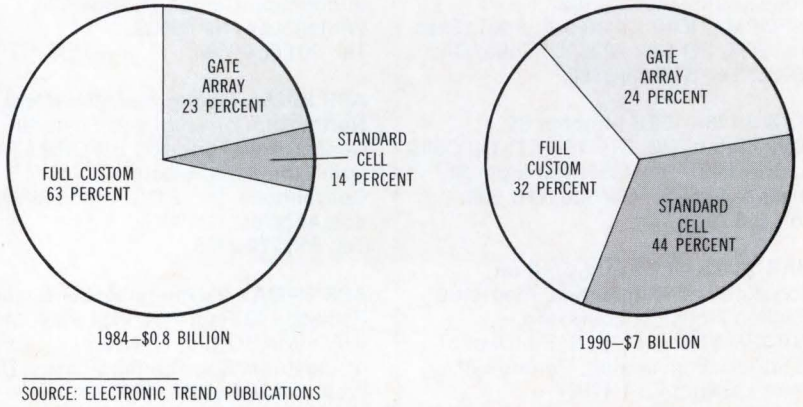
The price of 256-Kbit DRAMs will decline to about $9.50 in mid-1985, according to the *Icecap Report*. Produced by Integrated Circuit Engineering Corp, the report tentatively endorses a 12 percent growth rate scenario for the IC industry in 1985, with a possible 5 to 7 percent IC dollar growth. **Integrated Circuit Engineering Corp,** 710 Lakeway, Sunnyvale, CA 94086.

Circle 473

Custom/semicustom ICs

By 1990, more than 50 percent of ICs produced will emerge from the custom realm. This, according to Electronic Trend Publications in a report entitled *Customizing VLSI Integrated Circuits*, mandates careful consideration of design trade-offs for gate array, standard cell, and full-custom techniques. The 320-page report also forecasts a 68 percent combined share for gate array and standard cell custom circuits in 1990. Criteria for IC design selection are summarized, with availability of IC engineers, design cycles, and CAD/CAE tools factored in. The report costs $795. **Electronic Trend Publications,** 10080 N Wolfe Rd, Cupertino, CA 95014.

Circle 474



CALENDAR

CONFERENCES

MAR 5-7—Southcon & Mini/Micro Southeast, Georgia World Congress Center, Atlanta, Ga. INFORMATION: Dale Litherland, Electronic Conventions, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

MAR 7-8—Int'l Conf on Industrial Automation, Hong Kong. INFORMATION: Conf Secretary, Autotech Hong Kong, Hong Kong Productivity Center, 12/F, World Commerce Center, 11 Canton Rd, Tsimshatsui, Hong Kong. Tel: 3-723-5656

MAR 11-14—National Design Engineering Show, McCormick Place, Chicago, Ill. INFORMATION: Cahners Expo Group, PO Box 3833, Stamford, CT 06905. Tel: 203/964-0000

MAR 13-15—Picosecond Electronics and Optoelectronics, Hyatt Lake Tahoe, Incline Village, Nev. INFORMATION: Optical Society of America, 1816 Jefferson Pl, NW, Washington, DC 20036. Tel: 202/223-0920

MAR 13-15—Simulation Symposium, Tampa, Fla. INFORMATION: Alexander Kran, IBM Corp, East Fishkill Facility, Hopewell Junction, NY 12533. Tel: 914/894-7142

MAR 14-15—ACM Computer Science Conf. New Orleans Marriott Hotel, New Orleans, La. INFORMATION: Della T. Bonnette, Computing and Information Services, Univ of Southwestern Louisiana, Lafayette, LA 70504. Tel: 318/231-6306.

MAR 20-22—Phoenix Conf on Computers & Communications, Hyatt Regency Hotel, Tampa, Fla. INFORMATION: Doug Powell, Motorola, Inc, PO Box 2953, Phoenix, AZ 85062. Tel: 602/244-3965

MAR 24-27—Eastern Simulation Conference, Williamsburg Hospitality House, Williamsburg, Va. INFORMATION: Charles A. Pratt, Exec Dir, SCS, PO Box 2228, La Jolla, CA 92038. Tel: 619/459-3888.

MAR 25-28—IEEE Infocom 85, Washington, DC. INFORMATION: Celia L. Desmond, Rm 1855, 160 Elgin St, Ottawa, Ontario, Canada K1G 3J4. Tel: 613/239-4510

MAR 25-29—IEEE Int'l Conf on Robotics and Automation, Marriott's Pavilion Hotel, St Louis, Mo. INFORMATION: Dr K. S. Fu, Dept of Electrical Engineering, Purdue Univ, West Lafayette, IN 47907. Tel: 317/494-3433

MAR 26-28—Applied Machine Vision Conf, Cobo Hall, Detroit, Mich. INFORMATION: Robotics Industry Assoc, PO Box 1366, Dearborn, MI 48121. Tel: 313/271-7800

MAR 31-APR 3—Softcon, Georgia World Congress Center, Atlanta, Ga. INFORMATION: Northeast Expo, 822 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

APR 1-2—IEEE VLSI Test Workshop, Bally Park Place Hotel, Atlantic City, NJ. INFORMATION: Bob Tigue, IBM Dept 69J/422, Neighborhood Rd, Kingston, NY 12401. Tel: 914/385-7440.

APR 2-4—IEEE Microprocessor Forum, Bally Park Place Hotel, Atlantic City, NJ. INFORMATION: Helen Yonan, IEEE Office, Moore School of Electrical Engineering, Univ of Pennsylvania, Philadelphia, PA 19104. Tel: 215/898-8106.

APR 14-18—Computer Graphics Conf, Dallas Conv Center, Dallas, Tex. INFORMATION: National Computer Graphics Assoc, 8401 Arlington Blvd, Ste 601, Fairfax, VA 22031. Tel: 703/698-9600

APR 16-18—Computer Integrated Mfg and Communications Conf, Disneyland Hotel, Anaheim, Calif. INFORMATION: CASA/SME Public Relations, One SME Dr, PO Box 930, Dearborn, MI 48121. Tel: 313/271-0777

APR 17-24—Hannover Fair '85, Hannover, West Germany. INFORMATION: Hannover Fairs Information Center, PO Box 338, Whitehouse, NJ 08888. Tel: 201/534-9044

APR 23-25—Electro and Mini/Micro Northeast, Coliseum and Sheraton Center, New York, NY. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

APR 29-MAY 2—Intermag Conference, Radisson St Paul Hotel, St Paul, Minn. INFORMATION: J. H. Nyenhuis, Dept of Electrical Engineering, Purdue Univ, West Lafayette, IN 47907. Tel: 317/494-3524.

APR 30-MAY 2—Artificial Intelligence and Advanced Computer Technology Conf/Exh, Long Beach, Calif. INFORMATION: Tower Conference Management Co, 331 W Wesley St, Wheaton, IL 60187. Tel: 312/668-8100.

MAY 13-17—Int'l Conference on Distributed Computing. The Fairmont Hotel, Denver, Colo. INFORMATION: Dr Earl Swartzlander, TRW, Defense Systems, 1 Space Park, Redondo Beach, CA 90278. Tel: 213/535-4177.

MAY 20-22—Custom Integrated Circuits Conf. The Portland Hilton Hotel, Portland, Ore. INFORMATION: Dr Wesley N. Grant, Sperry Computer Systems, Sperry Park, PO Box 43525 MS Y11B1, St Paul, MN 55164. Tel: 612/456-4130.

MAY 20-22—Electronic Components Conf, Capital Hilton Hotel, Washington, DC. INFORMATION: Tom Pilcher, 3029 E Washington St, PO Box 372, Indianapolis, IN 46206. Tel: 317/261-1592.

MAY 21-22—Trends and Applications Conf on Utilizing Computer Graphics, IEEE Computer Society and National Bureau of Standards, Sheraton NW Washington Hotel, Silver Springs, MD. INFORMATION: Mark Skall, NBS, Technology Bldg, Room A265, Gaithersburg, MD 29899. Tel: 301/921-2431.

SHORT COURSES

MAR 25-26—(WPI campus, Worcester, Mass), **JUNE 17-18** (Hilton Hotel, Natick, Mass)—**Introduction to CAD/CAM.** INFORMATION: Kathy Shaw, Office of Continuing Education, Higgins House, Worcester Polytechnic Institute, Worcester, MA 01609. Tel: 617/793-5517.

MAR 25-27—Local Area Networks Univ of Wisconsin, Madison, Wis. INFORMATION: Dept of Engineering & Applied Science, Univ of Wisconsin, 432 N Lake St, Madison WI 53706. Tel: 608/262-2061.

APR 24-25—(WPI campus, Worcester, Mass), **JUNE 19-20** (Sheraton Tara Hotel, Nashua, NH)—**Industrial Local Area Networks.** INFORMATION: Kathy Shaw, Office of Continuing Education, Higgins House, Worcester Polytechnic Institute, Worcester, MA 01609. Tel: 617/793-5517.

DESIGNER'S BOOKCASE

ENCYCLOPEDIA OF INTEGRATED CIRCUITS: A PRACTICAL HANDBOOK OF ESSENTIAL REFERENCE DATA

By *Walter H. Buchsbaum*

This remarkable reference condenses volumes of manufacturer's data into one, easy-to-use handbook. It gives full details on even the most advanced integrated circuits. Clear illustrations of simple logic and block diagrams plus a list of key parameters and applications help you to capitalize on the most recent developments in microprocessors and various supporting chips.

$24.95 **Circle 445**

THE AI BUSINESS: COMMERCIAL USES OF ARTIFICIAL INTELLIGENCE

Edited By *Patrick H. Winston and Karen A. Prendergast*

This book explains what Artificial Intelligence is and how the technology has moved out of university research laboratories and into real-world applications. It describes systems in the computer industry that help configure, sell and install computers and it discusses intelligent workstations that increase the productivity of electronic design engineers.

$15.95 **Circle 447**

DESIGNING AND IMPLEMENTING LOCAL AREA NETWORKS

By *Dimitris N. Chorafas*

Local area networks allow users to hook up their office automation systems to centralized information resources. This practical book shows how to design and use such a system and how it can improve productivity and job performance. The book emphasizes both the hardware and software of local area networks, the databases that users can access online through distributed information systems, and the importance of bringing computer power to the end user's desk.

$35.95 **Circle 448**

MICROELECTRONICS: A STANDARD MANUAL AND GUIDE

By *John Douglas-Young*

Here you'll find clear, concise explanations about what integrated circuits are, how they operate and why trouble-shooting ICs differs from locating defects in conventional circuits. You'll also find complete data, with practical applications, for flip-flops, counters, bubble memories, I/O devices, MOSFETs, converters, opto-isolators and more.

$21.95 **Circle 446**

ROBOT MOTION: PLANNING AND CONTROL

Edited By *Michael Brady, John Hollerbach, Timothy Johnson, Tomas Lozano-Perez and Matthew Mason*

Nine papers of fundamental importance to the development of robotics—for researchers and engineers in industry and academia—are grouped in five sections: Dynamics; Feedback Control: Trajectory Planning; Compliance and Force Control; Task Planning. Each section begins with a substantial analytic survey.

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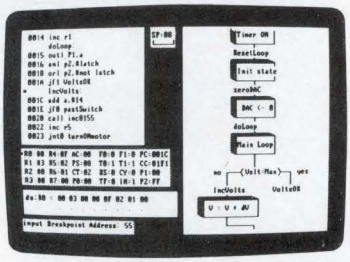

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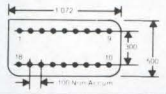

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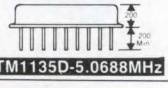

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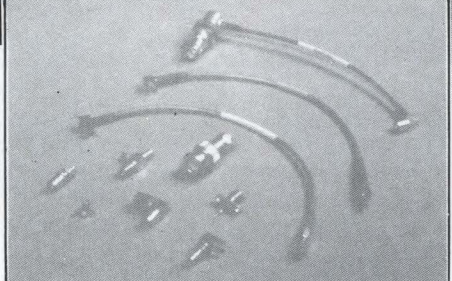

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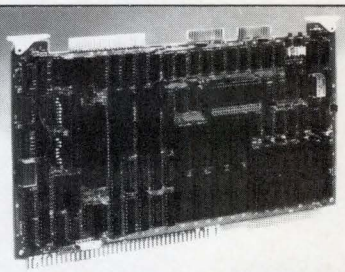

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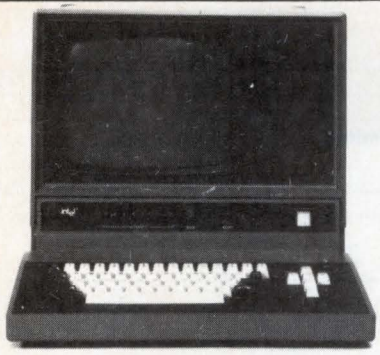

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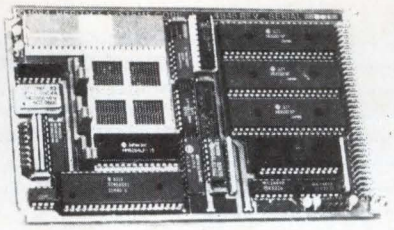

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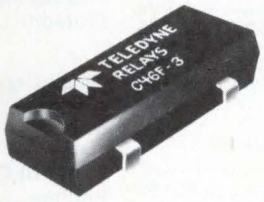

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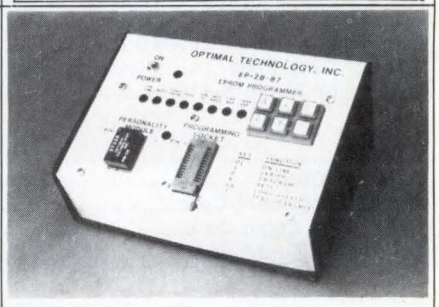

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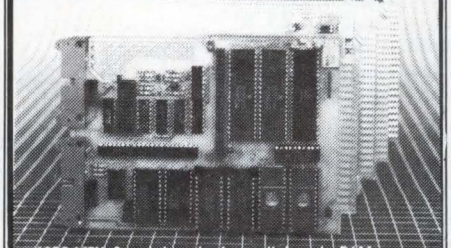

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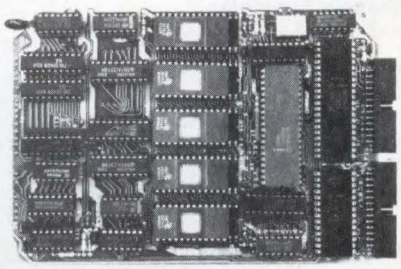

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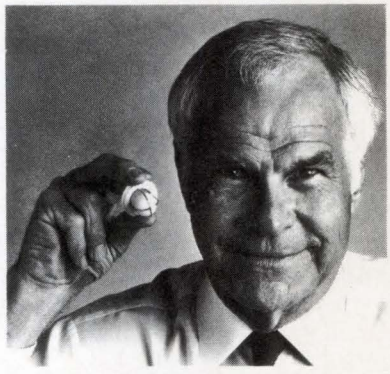

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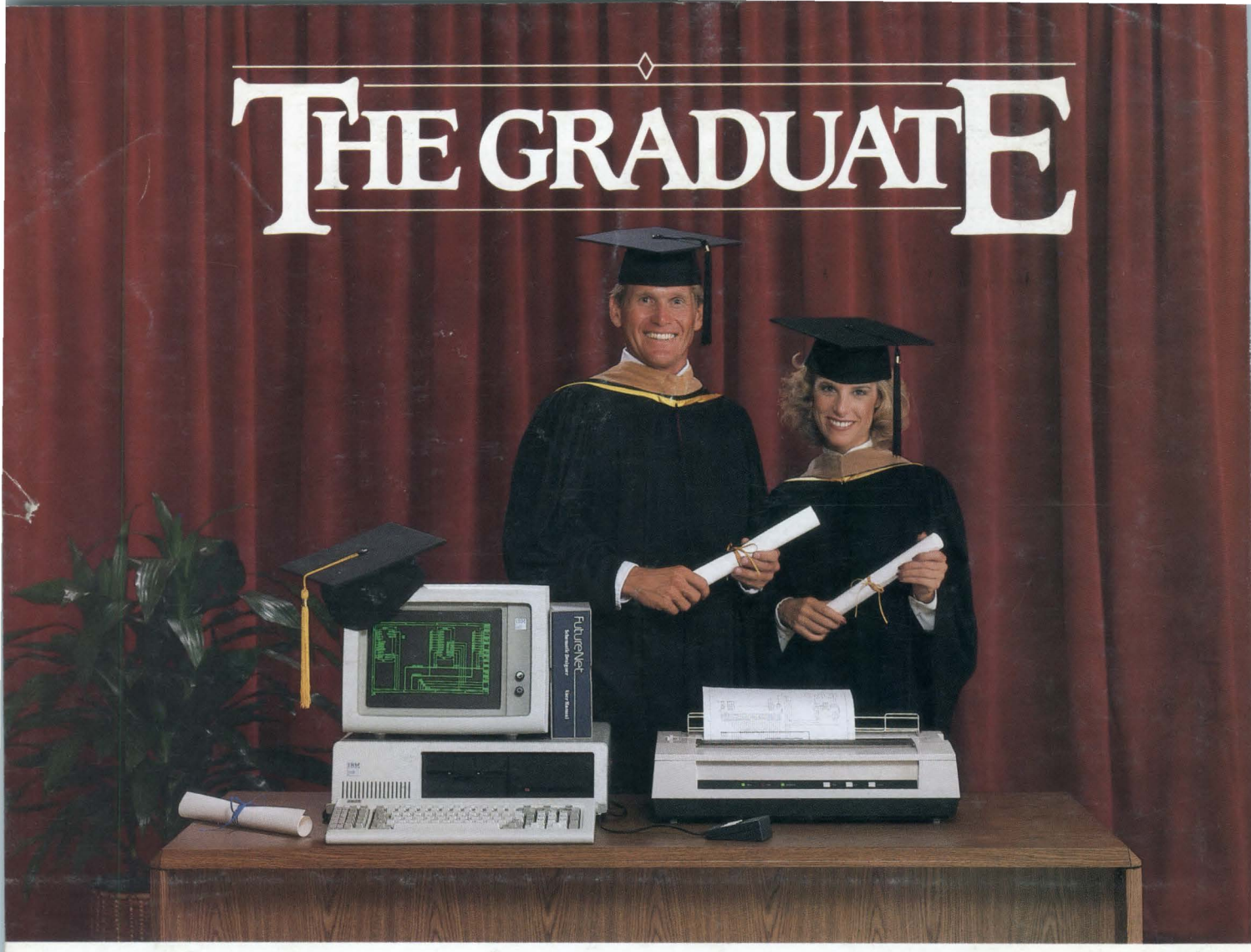

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