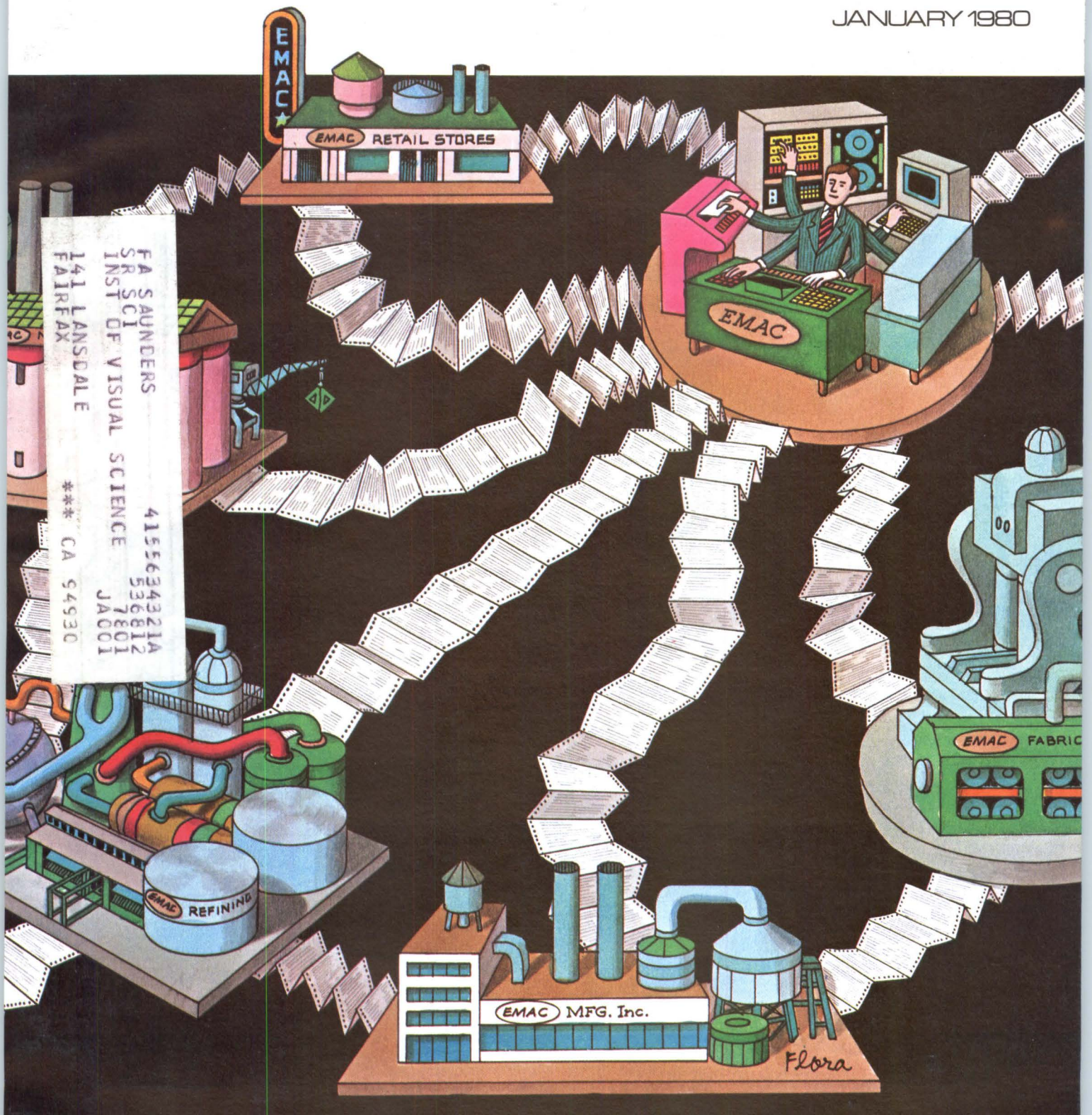


COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

JANUARY 1980



MULTITASKING EXECUTIVE SIMPLIFIES REALTIME MICROPROCESSOR SYSTEM DESIGN
SEMICONDUCTOR MEMORY UPDATE—PART 2: RAMS
CRT TERMINAL ARCHITECTURE PROVIDES COST EFFECTIVE CUSTOMIZING VERSATILITY



Anything's possible with a WHIZZARD™ 7000.

Fast refresh graphics throughput. Unequaled vector quality. Dynamic display versatility. You get it all with a WHIZZARD 7000.

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For even mightier magic, you can add hardware rotate, scale, clip, zoom, and multi-viewports. You can even work in 3-D or color.

Choose the WHIZZARD 7000 that solves your graphics problem. A basic monitor/processor that'll connect to any 16-bit or 32-bit computer. An intelligent refresh terminal with computing power already built-in. Or a stand-alone graphics processing system, complete with peripherals and software.

Pick from lots of WHIZZARD 7000 graphics peripherals. Joysticks with push-button interrupt. Data tablets, digitizers and light pens. Pen plotters and electrostatic printer/plotters. And, more.

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The Visible Difference



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CORPORATION

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Kennedy's vacuum column digital tape transports weren't designed yesterday to grab a piece of a growing market. In fact, they virtually founded the vacuum column market. They were the first to have such features as a capacitive tape-location detector for improved tape life; air bearings and hardcoated read-after-write heads to reduce tape wear and improve data integrity.

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Data densities are 200/556 cpi or 556/800 on 7-track units and 800 cpi, 1600 cpi or 800/1600 cpi on 9-track transports. The format is NRZ1/PE.

Models 9100/9300 offer more features, more performance, and most important, more time-in-the-field than any competitive units.

Why do we think so? Simple. Our figures show that we are about 3000 satisfied users ahead at this point.

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Phone (206) 251-5524.



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PRINTERS
WORLDWIDE



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CIRCLE 3 ON INQUIRY CARD

JANUARY 1980

VOLUME 19, NUMBER 1

DEPARTMENTS

12 CALENDAR

16 COMMUNICATION CHANNEL

Disciplines that enable application computers to communicate with one another via a network have evolved over the past decade. Widespread implementation of computer communication systems emphasizes a need for protocol standardization

42 DIGITAL TECHNOLOGY REVIEW

Inappropriate or incomplete procedures used within an organization can be revealed and revised by institution of a periodic audit reviewing all areas

78 DIGITAL CONTROL AND AUTOMATION SYSTEMS

Coal analysis system under microcomputer control can supply analyses previously provided by large, distant wet chemistry laboratories, but more quickly, at less expense, and with improved accuracy

152 MICRO DATA STACK/COMPUTERS, ELEMENTS, AND SYSTEMS

Compilation of microcomputer signal timing conventions clarifies representations found in assorted combinations of signal transitions and logic levels

168 AROUND THE IC LOOP

Flexibility of devices within 8-bit slice family challenges designers in combining functions to develop high speed LSI ECL systems from standard parts

194 PRODUCT FEATURE

Entry level scientific computer system provides high performance computational capability

214 LITERATURE

215 GUIDE TO PRODUCT INFORMATION

217 ADVERTISERS' INDEX

Reader Service Cards
pages 219-222

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FEATURES

**MULTITASKING EXECUTIVE SIMPLIFIES
REALTIME MICROPROCESSOR SYSTEM DESIGN 109**

by Y. P. Chien

To overcome problems associated with realtime, event driven programming for microprocessor based systems, multitasking executive establishes efficient and flexible software management and maintenance organization

SEMICONDUCTOR MEMORY UPDATE—PART 2: RAMS 119

by Eugene R. Hnatek

This second of three parts surveys merits and restrictions of random access memories, specifically focusing on differing RAM organizations for current implementations and probable evolutions

**CRT TERMINAL ARCHITECTURE PROVIDES
COST-EFFECTIVE CUSTOMIZING VERSATILITY 133**

by Gerald Pisano and Robert Yablonski

Customizing a smart CRT terminal for different applications can be simplified and made less costly with a proper architectural design

**REALTIME ANALYZER AIDS
HARDWARE/SOFTWARE INTEGRATION 140**

by Robert Francis and Robin Teitzel

A realtime trace of in-process execution lessens the designer's burden when linking complicated hardware and software into a coherent microprocessor based system

CONFERENCES

**IEEE INTERNATIONAL SOLID STATE
CIRCUITS CONFERENCE 100**

Highly diversified papers to be presented at ISSCC '80, focusing on VLSI and LSI and exploring the limits of technology, underscore the growing complexity of chips

COMPCON SPRING 80 104

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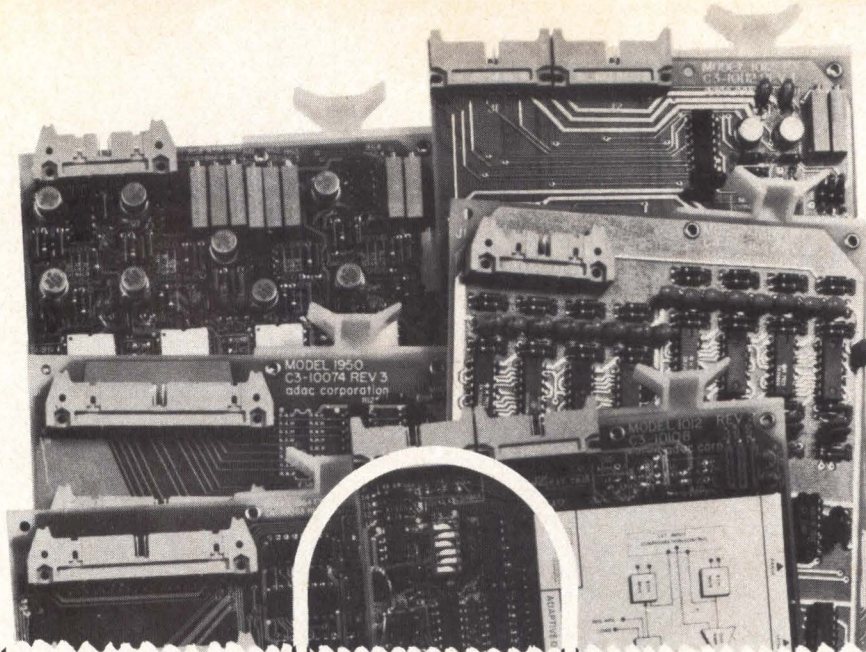
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When it comes to I/O functional cards for DEC LSI-11 microcomputers, ADAC has the biggest selection available.

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- 1014** 16 channels, high level inputs, 14 bit
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- 1023EX** 32-64 channel high level inputs, LSI-11/23 interrupt compatible
- 1030** 16-64 channels, high level inputs, 12 bit, 2 DACs
- 1112RL** 8-16 differential low level and thermocouple inputs, 12 bit
- 1112RX** 8-16 differential low level and thermocouple inputs, mux expander
- 1113** 8-16 differential low level and thermocouple inputs, 12 bit, LSI-11/23 interrupt compatible
- 1113EX** 8-16 differential low level and thermocouple inputs, mux expander, LSI-11/23 interrupt compatible
- 1412DA** 1-4 D/A channels, voltage or current loop outputs

CLOCK CARDS

- 16016PT** Programmable crystal clock/timer

SERIAL I/O CARDS

- 1750** Asynchronous line interface with two I/O ports

DIGITAL I/O

- 1604/OPI** 2-4 optically coupled pulse-input channels
- 1604/POC** 2-4 pulse output channels
- 1616CCI** 16 discrete inputs, contact closure detect
- 1616/MIC** 16 discrete inputs with priority encoder
- 1616/OIO** 16 parallel outputs, optically isolated
- 1616/OII** 16 parallel inputs, optically isolated, can cause interrupt
- 1620TTL** 16 latched inputs and outputs for DMA operation
- 1616HCO** 16 discrete outputs, high current drive
- 1632HCO** 32 discrete outputs, high current drive
- 1632TTL** 32 TTL I/O lines
- 1664TTL** 64 TTL I/O lines

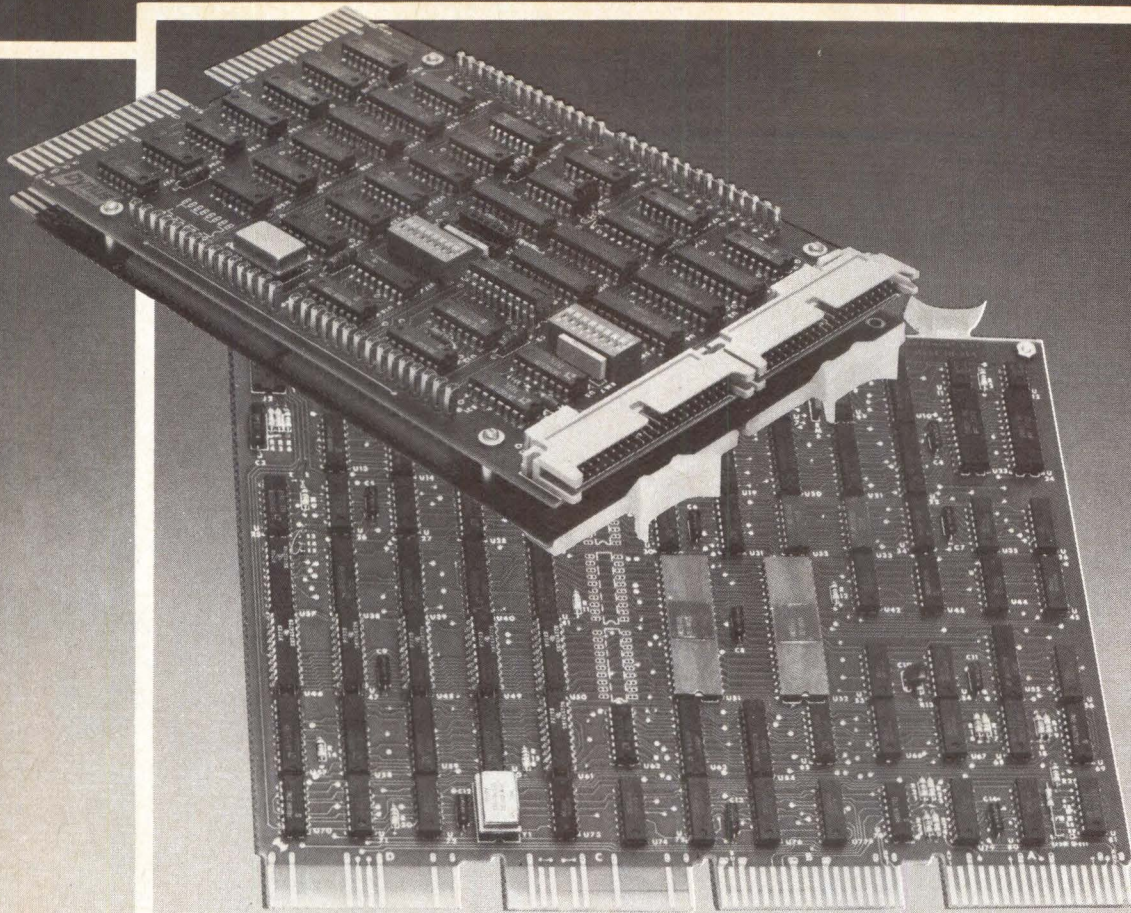
BUS INTERFACE

- 1620DMA** Direct memory access controller
- 1900** Unibus to LSI-II translator
- 1950** Bus repeater
- 1900CT** Cable terminator card

Whatever your DEC system—Unibus, Qbus or Omnibus, write or call for full details on the industry's widest line of compatible cards and complete system enclosures.



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They're all ready to plug into your LSI-11 or PDP-11 backplane...they're all totally software compatible...they're all available now...and they're offered with confidence, not promises.

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CIRCLE 5 ON INQUIRY CARD



Sure Winners

Competitive systems start with Intel® static RAMs.

Now you can choose a champion for any design.

High performance memory design is a fast track. The winners are those who match advanced components precisely with today's system requirements. When it comes to static memory, only one supplier has the broad selection of high speed, low power RAMs, and the delivery you need to bring your product to market ahead of the field.

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From the beginning, Intel has been the leader in practical, producible MOS memory technology. First NMOS. Then high performance HMOS,* the high reliability technology that's produced more than 14 million fast static RAMs—as well as our industry standard 16-bit microcomputer, the 8086. Now HMOS II* is here, bringing you the same reliability and a new generation of even higher speed static RAMs.

Today, Intel gives designers the widest selection of 1K and 4K static RAMs in the industry. Over 50 different versions let you tailor speed, power, density and organization precisely to your system requirements.

Record breakers for high speed systems

Nowhere is the precision matching of memory components to function more important than in high speed cache, buffer, control store and main memory. At Intel, you'll find static RAMs to cover your full range of design goals.

*HMOS and HMOS II are patented processes of Intel Corporation.



	1K x 1	4K x 1	1K x 4
20	2115H/25H (20-35ns)	2147H (35-55ns)	2149H* (45-55ns)
40	2115A/25A (45-70ns)	2147 (55-85ns)	2148H* (45-55ns)
60			2148 (55-85ns)
80			
100			
200		2141 (120-250ns)	2114A (120-250ns)
300			

*Available Q1, 1980

For highest speed and low power, no bipolar can touch our HMOS II 2115H/25H 1K static RAMs. One version gives you record access times of 20ns; three others let you choose speed/power combinations to 35ns. For designs requiring speeds from 45-70ns, our 16-pin industry standard HMOS 2115A/25A series covers the spectrum. All of these 1Ks are pin-compatible replacements for 93415/25 bipolars, and all give you dramatically lower power, too.

In a 4K x 1 format, our HMOS 2147 is the industry standard for low power and speeds to 55ns. Today, designers requiring even higher performance will find a winner in our new HMOS II 2147H—with versions as fast as 35ns and standby power dissipation of only 30mA.

Finally, for special wide-word memories, including control store and bit slice designs, Intel's 1K x 4 bit 2148 is out in front. It gives you all the performance advantages of the HMOS 2147, plus the modularity that lets you save 75% on board

space compared with 1K designs. And, you can expect even faster speeds in the future as we apply HMOS II to wide-word memory devices.

Pick the best performer for microcomputers

For years, microcomputer system designers have relied on Intel's 18-pin industry standard 2114 static RAM in 1K x 4 designs. Now we've used HMOS technology to improve performance with our new 2114A. It's a direct descendent of our 2114, but with a 30% smaller die size, 40% faster speeds, and 43% less power dissipation. The 2114A gives you performance equal to that of our 4K x 1 bit 2141, so you get optimum efficiency no matter what modularity you need—no matter how basic or how advanced your microcomputer application.

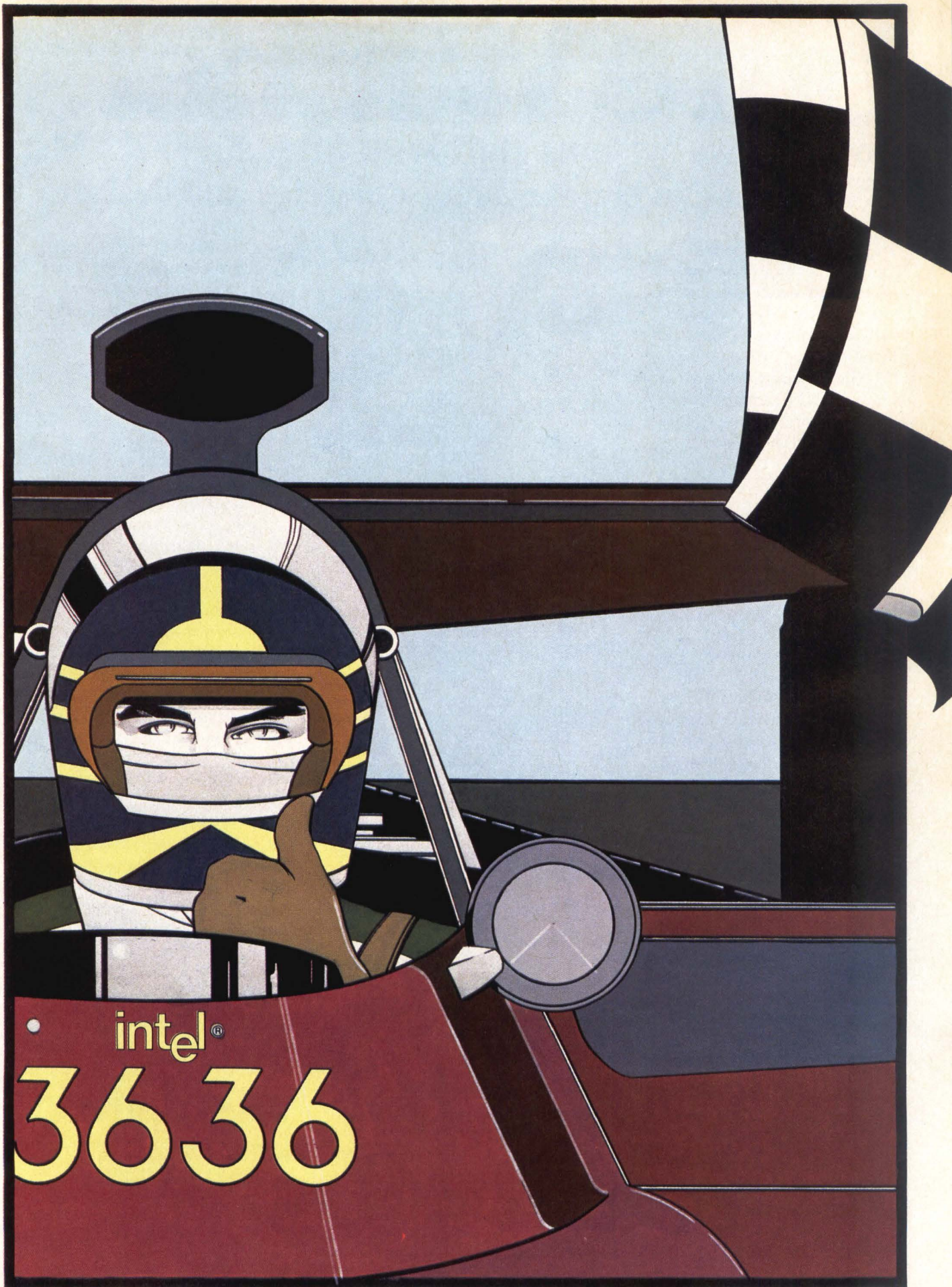
Intel gets you off and running now

We're delivering all of these fast static RAMs today. To order, or for more information, including our HMOS Reliability Report, RR18, contact your local Intel sales office or distributor. Or write Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

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CIRCLE 6 ON INQUIRY CARD



intel®
3636

16K Speed Champ

Intel's new 3636 bipolar PROM breaks the 16K speed barrier with 65ns access. It's a victory for bit slice designs.

Streamlined performance is the whole point of today's advanced bit slice computers. High speed. High density. High reliability. Now Intel delivers the 16K 3636, manufactured with our new Stacked Fuse Bipolar* process to produce the highest performance microprogram memory yet.

Design for speed and comfort

Our 2Kx8-bit 3636 gives you four times the density of 4K bipolar PROMs with no speed penalty. The 3636's maximum access of 65ns makes it the ideal memory for fast, high density bit slice designs, as well as look-up table and other program store applications.

Using the 3636 instead of 4K PROMs lets you reduce component count and microprogram board requirements up to 75%. By designing program store on the CPU board, you can even save up to a full board slot for I/O or other functions.

For designs requiring extended temperature ranges, our 80ns military device, the M3636, is ideal.

No matter what your application, you're certain to reduce power requirements. Power consumption per bit for the 3636 is only one fourth that of most 4K bipolar PROMs and only half that of most 8Ks.

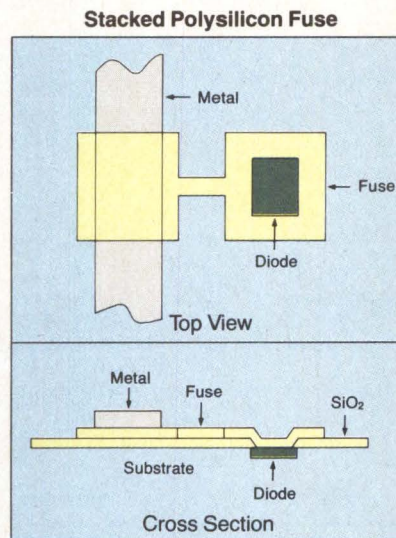
Whether you're replacing 4K or 8K bipolar devices, the 3636 makes it simple. It's packaged in the industry standard 24-pin DIP, so you won't have to redesign in order to upgrade.

And you can program the 3636 in seconds using Intel's UPP103 or any standard PROM programmer.

Our formula: Stacked Fuse Bipolar

The most efficient way to improve speed characteristics of bipolar PROM's is to reduce die size. Very simply, smaller geometries reduce capacitance, thus speeding access time.

Intel achieved the 3636's high speed and dramatically smaller die size with a new "stacked" bipolar process. Stacked Fuse Bipolar combines Intel's expertise in Large



Intel's new Stacked Fuse Bipolar process allows a 30% reduction in the 16K cell size. This dramatic density improvement yields faster access speeds than ever before possible. The illustration shows the "stacking" of our polysilicon fuse over the diode instead of placing them side by side as in older designs.

Scale Integration with dual layer metalization and polysilicon fuses. (See diagram.) The result is the highest density and performance ever in a 16K bipolar PROM.

Intel's 3636 Bipolar PROMs			
	3636-1	3636	M3636
Maximum Access Time (ns)	65	80	80
Typical Power Per Bit (mW)	0.05	0.05	0.05

Intel's 3636 also means high reliability. We've already proven the producibility and dependability of Stacked Fuse technology with our 3625A 4K bipolar PROM. Hundreds of thousands of these components are already in operation, including military versions for hi-rel applications. In addition, millions of device-hours of tests with zero fuse failures confirm Stacked Fuse Bipolar's reliability. Further details on Intel's bipolar PROM reliability are found in our Summary Evaluation Report, RE1, available on request.

Get on the fast track today

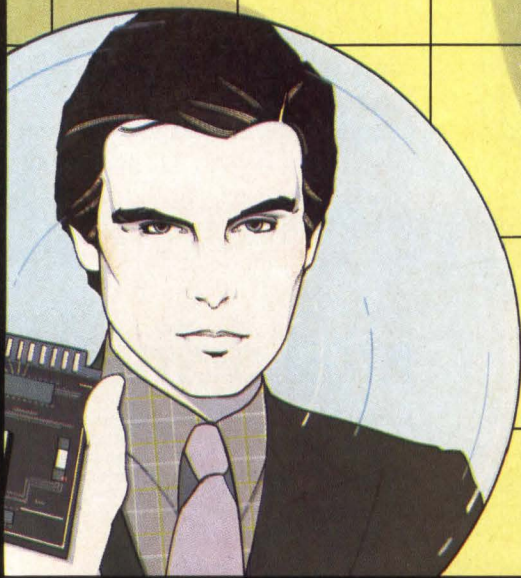
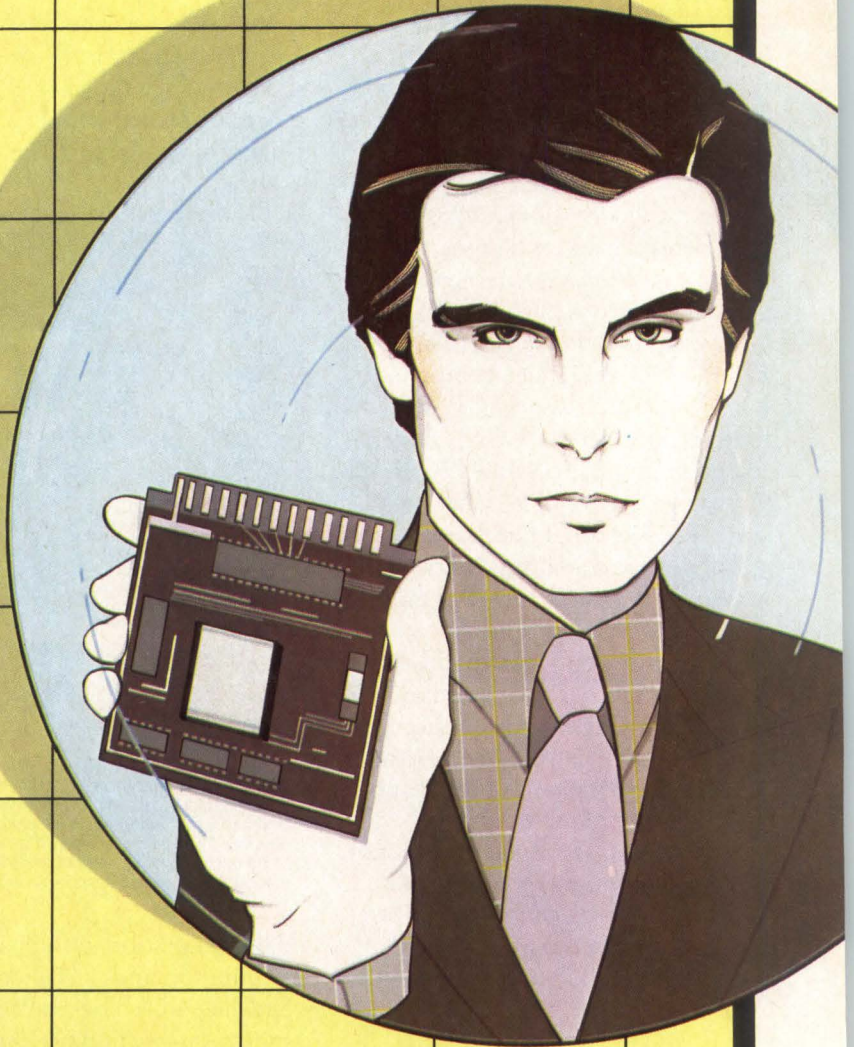
Our high performance 3636 is available now. To order, or for complete data and reliability information, contact your local distributor or Intel sales office. Or write Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051. Or call (408) 987-8080.

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*Stacked Fuse Bipolar is a patented process of Intel Corporation.

CIRCLE 7 ON INQUIRY CARD



Million Bit Memory Kit

Intel delivers the first megabit bubble system and all the support you need to start designing today.

Step into the megabit bubble. You'll find an entirely new class of non-volatile storage—and vast new opportunities to exploit the microcomputer.

Bubble memory for microcomputers

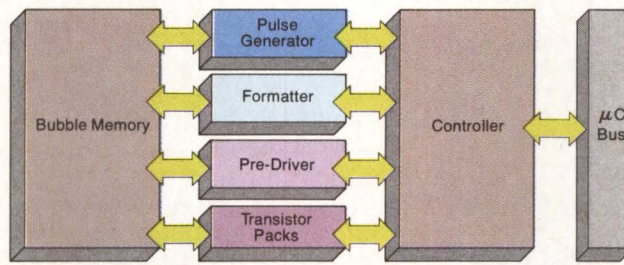
System designers have always been attracted to bubble memory for compact, low power, high reliability applications. Until now, though, bubble memories have been difficult to use and costly, since they require complex address, control and interface circuitry.

Today, Intel introduces a million bit bubble system perfectly matched in size and performance to the world of microcomputers. Intel's bubble memory gives you 128K bytes of low power read-write memory, plus all the system components you need for compatibility with advanced microcomputers like our 8-bit 8080, 8085 and 8088 and our 16-bit 8086.

Our system makes it simple

To simplify designing and manufacturing, Intel's bubble memory system consists of only seven components. All of them fit easily on a pc board as small as 4"x4".

The heart of the system is our 7110 Magnetic Bubble Memory chip. It interfaces directly with our 7242 Formatter/Sense Amplifier, 7230 Current Pulse Generator, 7250 Coil Pre-Driver and two 7254 Quad Transistor Packs.



Intel® Bubble Memory System

The user interface, system timing and control functions are provided by our 7220 Controller, available Q1, 1980, or by our Controller Emulator Kit CPK-72, here today.

For systems exceeding a megabit, you can design with the same component family. Since one 7220 Controller will accommodate up to eight megabit chips and their support devices, larger system designs are simplified dramatically.

Bubble you can believe in

Intel's bubble memory means unparalleled data integrity. It's a rugged, solid state device. And it's completely non-volatile, so your data remains when the power goes off. No battery backup is necessary.

But the bubble system goes even further to ensure reliability. Intel's megabit chip works with the 7242 Formatter to give your

system built-in error correction and detection. The 7110's ECC detects and corrects burst errors.

Start designing today

Intel's megabit bubble memory system is an ideal solution for microcomputer-based instrumentation, terminals, process controls and telecommunication systems. Everything you need to start designing is here today. Build your own system with our bubble memory prototyping kit.

It gives you all the components for a one megabit system, plus complete documentation for easy designing. Or get a head start with our ready-to-use development board with complete system software. For a copy of our Bubble Memory Design Handbook, contact your local sales office or distributor. Or write Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call (408) 987-8080.

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CALENDAR

CONFERENCES

FEB 6, MAR 25, AND MAR 27—Invitational Computer Conf, Ft Lauderdale, Fla; Dallas, Tex; and Houston, Tex. INFORMATION: B. J. Johnson & Assoc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

FEB 12-14—Data 80 Data Communications Conf and Exhibition, Harbour Castle Hilton Hotel and Convention Ctr, Toronto, Ontario, Canada. INFORMATION: Whitshed Publishing Ltd, 2 Bloor St W, Suite 2504, Toronto, Ontario M4W 3E2, Canada

FEB 13-15—Internat'l Solid State Circuits Conf (ISSCC), Hilton Hotel, San Francisco, Calif. INFORMATION: Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134. Tel: 305/446-8193

FEB 19-22—Southwestern Computer Conf, Myriad Convention Ctr, Oklahoma City, Okla. INFORMATION: Oklahoma State U Technical Institute, 900 N Portland, Oklahoma City, OK 73107. Tel: 405/947-4421

FEB 25-28—COMPCON Spring, Jack Tar Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

MAR 3-5—NCC Office Automation Conf, Georgia World Congress Ctr, Atlanta, Ga. INFORMATION: Jerry Chiffreller, 210 Summit Ave, Montvale, NJ 07645. Tel: 201/391-9810

MAR 4-5—Midwest Digital Equipment Exhibit and Seminar, Thunderbird Motel, Minneapolis, Minn. INFORMATION: John Bastys, Countryman Associates Co, 1821 University Ave, St Paul, MN 55104. Tel: 612/645-9151

MAR 14-16—West Coast Computer Faire, Civic Auditorium and Brooks Hall, San Francisco, Calif. INFORMATION: Computer Faire, 333 Swett Rd, Woodside, CA 94062. Tel: 415/851-7075

MAR 17-19—Industrial Control & Instrumentation Applications of Mini & Microcomputers (IECI), Sheraton Hotel, Philadelphia, Pa. INFORMATION: Dr Paul Russo, RCA Labs, Princeton, NJ 08540. Tel: 609/452-2700, X3234

MAR 17-20—Interface '80, Miami Beach Convention Ctr, Miami Beach, Fla. INFORMATION: Peter Young, Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502

MAR 19-21—Simulation Sym, Holiday Inn Resort, Tampa, Fla. INFORMATION: Sudesh Kumar, NCR Corp, 1511 Tucker Ln, Encinitas, CA 92024

MAR 19-21—Design Technology for Computers & Datacomm Systems '80, Disneyland Hotel Convention Ctr, Anaheim, Calif. INFORMATION: Industrial & Scientific Conf Management, Inc, 222 W Adams St, Chicago, IL 60606. Tel: 312/263-4866

MAR 24-28—Eurocon '80 (European Conf on Electrotechnics), Stuttgart, Germany. INFORMATION: Prof Dr W. E. Proebster, IBM Deutschland GmbH, Postfach 80 08 80, D-7000 Stuttgart 80, Germany

MAR 31-APR 2—Internat'l Computer Aided Design Conf and Exhibition, Metropole, Brighton, England. INFORMATION: The Organisers, CAD 80, IPC Science and Technology Press Ltd, PO Box 63, Westbury House, Bury St, Guildford, Surrey GU2 5BH, England

APR 9-11—Internat'l Conf on Acoustics, Speech and Signal Processing (ICASSP), Fairmont Hotel, Denver, Colo. INFORMATION: J. Robert Ashley, Chm, Electrical & Computer Engineering, University of Colorado, 1100 14th St, Denver, CO 80202. Tel: 303/629-2554

APR 14-17—Conf on Computer Graphics, Detroit, Mich. INFORMATION: Carol Lynn, Engineering Society of Detroit, 100 Farnsworth Ave, Detroit, MI 48202. Tel: 313/832-5400

APR 16-17—Peripherals 80, Bloomsbury Ctr, London, England. INFORMATION: Iliffe Promotions Ltd, Dorset House, Stamford St, London SE1 9LU, England

APR 21-24—Internat'l Magnetics Conf, Sheraton-Boston Hotel, Boston, Mass. INFORMATION: D. I. Gordon, Conf Chm, Naval Surface Weapons Ctr, White Oak, Silver Spring, MD 20910. Tel: 202/394-2167

APR 28-MAY 2—Society for Information Display Internat'l Sym, Town-Country Hotel, San Diego, Calif. INFORMATION: Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134. Tel: 305/446-8193

MAY 6-8—Internat'l Sym on Computer Architecture, Casino, La Boule, France. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

MAY 13-15—ELECTRO, Boston-Sheraton/Hynes Auditorium, Boston, Mass. INFORMATION: Dale Litherland, Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

MAY 19-22—National Computer Conf, Anaheim, Calif. INFORMATION: AFIPS, 1815 N Lynn St, Arlington, VA 22209. Tel: 703/243-4100

JUNE 3-5—Networks 80, Bloomsbury Centre Hotel, London, England. INFORMATION: Online, Cleveland Rd, Uxbridge UB8 2DD, England

JUNE 17-19—Internat'l Microcomputers Minicomputers Microprocessors/DATACOMM '80 Conf, Palais Des Expositions, Geneva, Switzerland. INFORMATION: Industrial & Scientific Conf Management, Inc, 222 W Adams St, Chicago, IL 60606. Tel: 312/263-4866

JUNE 25-27—IFAC Sym on Large Scale Systems: Theory and Applications, Toulouse, France. INFORMATION: Symposium Secretariat, AFCET-156, Bd Péreire-75016 Paris, France

SHORT COURSES

FEB 25-29—Data Communication Systems and Networks, and Microprocessor and Microcomputer Theory and Application, George Washington University, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC. Tel: 202/676-6106

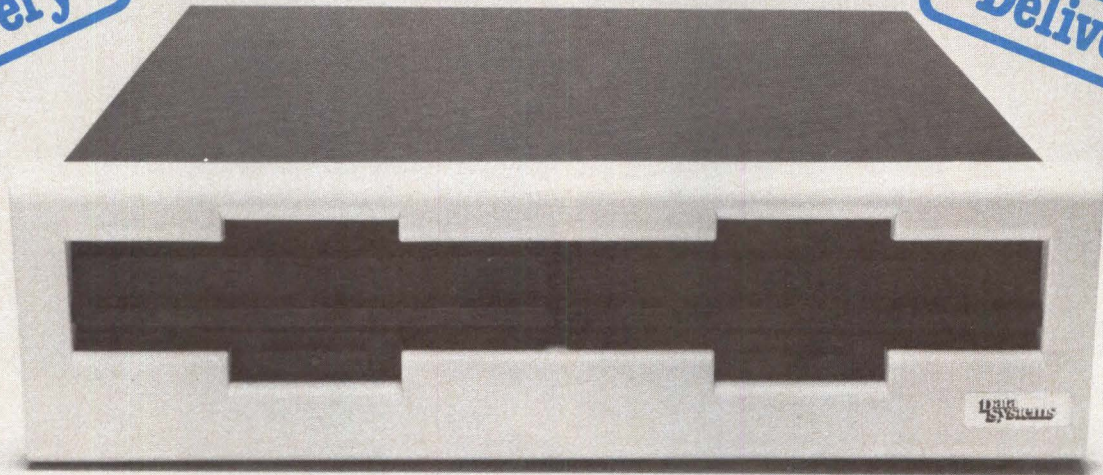
MAR 24-27—Principles of Database Systems, and MAR 24-28—Programming in Pascal, New York, NY; and San Francisco, Calif. INFORMATION: Computer Science Education Extension, Computer Science Press, Inc, 9125 Fall River Ln, Potomac, MD 20854. Tel: 301/299-2040

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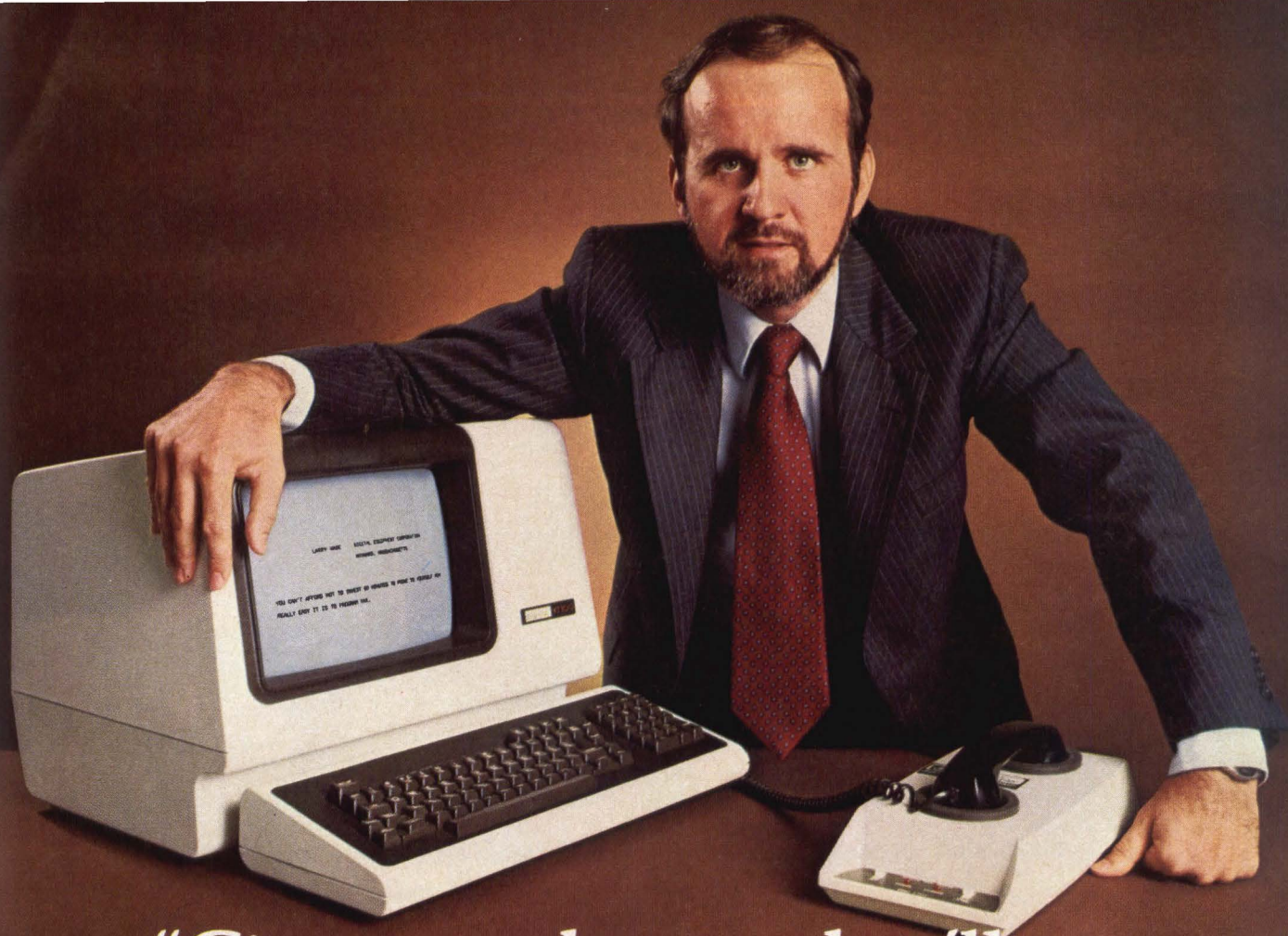
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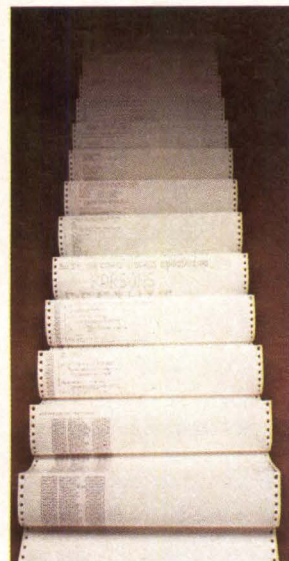
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THE DEVELOPMENT OF HOST PROTOCOLS

David C. Walden

Bolt Beranek and Newman Inc., Cambridge, Massachusetts

No aspect in the implementation of computer networking has been more difficult than the development of the procedures and conventions to be used by the variety of application computers in attempting to communicate with each other across a network. To distinguish them from the machines used in the network itself, these application computers are called "hosts." Hosts can be made by different manufacturers and use different operating systems, and they can be attached to a communication subnetwork that provides either very sophisticated or very primitive communications capability. These facts of life have led to the evolution of host communication procedures and conventions, called "protocols." All protocols with which we will be concerned appear to have two common elements, the definition of path control procedures and the establishment of path conventions.

Path control procedures are designed to establish between the communicating entities a virtual communications path with certain characteristics that the physical medium may not possess, such as provision for addressing, synchronization, error control, and flow control. Examples of path conventions are timing considerations (eg, to a 1200-baud terminal), encoding considerations (eg, using the EBCDIC character set), and procedures for the sharing of the same communication path by control information and data (eg, provision of certain distinguishable control characters used to signal that the transmission should be aborted).

Early Developments

The earliest protocols were used with point to point or star networks and treated the "network" as a simple data pipeline; they were implemented as single monolithic programs. As communication circuits began to be shared among many terminals, the protocols had to be enhanced to resolve conflicts between the terminals. The addition

of frontend processors resulted in the protocol package being centralized in these processors, but required a new interface protocol between mainframe and front end. Similarly, the development of terminal cluster controllers, data concentrators, and remote front ends each resulted in protocol changes.

"Common user" communications networks, capable of simultaneously serving many applications, required a new level of host protocol. With such networks the user must be able to provide addressing information to the network specifying where each unit of information is to be delivered, something not provided by a data pipeline that can merely be tapped at two or more points. A common user system makes possible the interconnection of any set of terminals and computers, but requires that hosts and terminals follow standard protocols in order to communicate with each other.

The ARPANET Approach

In 1968 the U.S. Department of Defense began construction of the ARPANET, first of the common user networks. A "layered" approach to communication protocols was adopted in the ARPANET, wherein the higher level protocols use the services of the lower level protocols.¹ The lowest layer specifies the electrical interface, link control, and message format for communication between the switching node in the ARPANET and a host. The next layer specifies methods of establishing communication paths between hosts, managing buffer space at each end of a communication path, and handling related procedures. The following layer specifies a standard way for a remote user or process to attract the attention of a network host, preparatory to using that host. The next layer was designed to support terminal access to remote hosts and provides a specification for a network standard terminal and the protocol for communicating between

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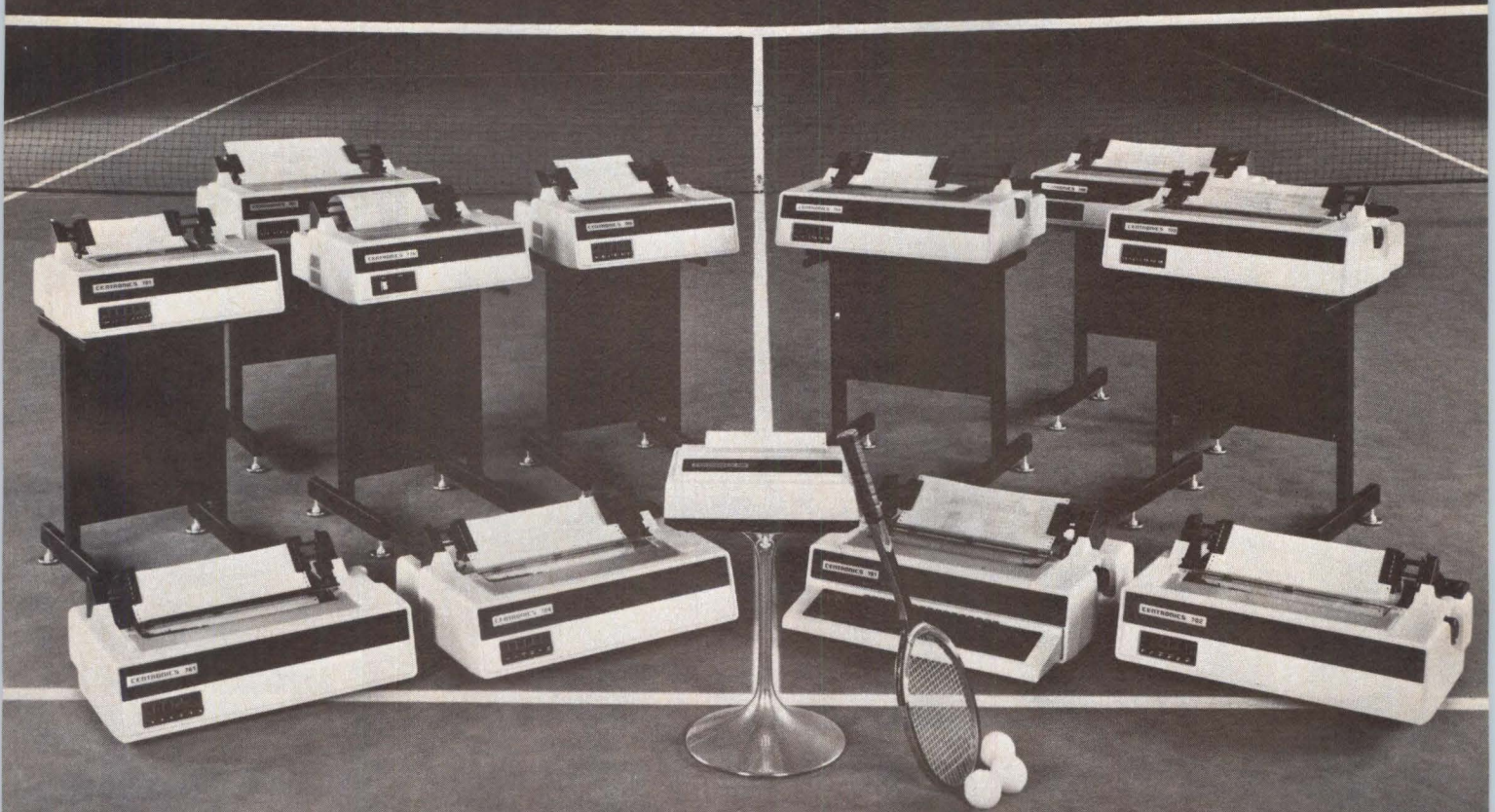
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this standard terminal and a host. Finally, there are protocol layers for file transfer and other functions.

The ARPANET host protocol is illustrated in Fig 1. Before two processes in different hosts can communicate, a data connection must be set up between a socket in one process's host monitor and a socket in the other process's host monitor. A socket is an element in a network-wide name space into which each monitor maps its own internal name space. For two processes to make a data connection, each process makes a connection request to its own monitor. The two monitors then exchange these requests via messages over a control connection, a special logical connection between each pair of hosts that is always reserved for control messages. If both monitors are in agreement, the data connection is established. This new data connection exists until it is explicitly terminated, again using intermonitor control messages over the control connection.

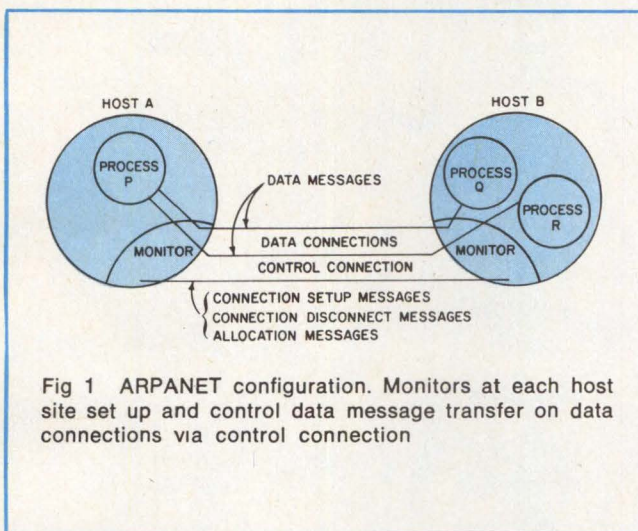


Fig 1 ARPANET configuration. Monitors at each host site set up and control data message transfer on data connections via control connection

During the "life" of a data connection, many messages may be sent from the socket at one end to the socket at the other. However, since the data connection exists over a series of many messages, a mechanism is provided to stop the flow of messages when a receiving process's host is overloaded. The mechanism is a buffer allocation system and a requirement for the sender to stop transmitting when it has exhausted the allocated capacity. A control message is used to replenish buffer allocations. Multiple data connections may be in effect simultaneously.

The ARPANET host protocol provides what have come to be called "virtual circuits" between communicating hosts. Specifically, a virtual circuit provides for the transmission of separate information units, at a rate acceptable to the receiver, with extremely low probability of loss, duplication, or mis-ordering of any information unit.

Transmission Control Program

The desire to have a host protocol which is suitable for use in a multinet environment (something not addressed by the ARPANET host protocol) led to the specification of a new protocol known as Transmission Control Program (TCP).² TCP makes minimal assumptions about the network or networks with which it is used. It accom-

modates communication between networks using different basic message sizes; provides for end-to-end error control, retransmission, and data reassembly and reordering; provides for more than one message to be in transit at a time; provides resynchronization for the end-to-end flow control mechanism; and provides for very general host addressing conventions. Of course, the generality provided by TCP has its cost, and TCP puts a potentially large processing burden on the host.

Datagram Approach

Shortly after the ARPANET became operational, development began on the French Cyclades network. Where the ARPANET subnetwork followed a virtual circuit approach, Cyclades followed a "datagram" technique. Operation of a datagram packet network is more analogous to a high-speed electronic postal system than to a circuit switching system: addressed packets are input at many points, mixed, and delivered; some are occasionally lost, and the delivery sequence is only loosely related to the input sequence. Such a system puts a greater burden on the hosts but simplifies construction of the communications subnetwork. This philosophy has been carried over into larger European research networks.

Datagram service provides the advantage of supporting applications in which low delay, or variance in delay, is more important than the high level of reliability and message accountability provided by virtual circuits. An example is digitized voice transmission. Datagrams may also be suitable for very short independent communications such as data base inquiries from credit terminals.

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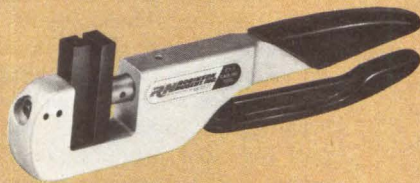
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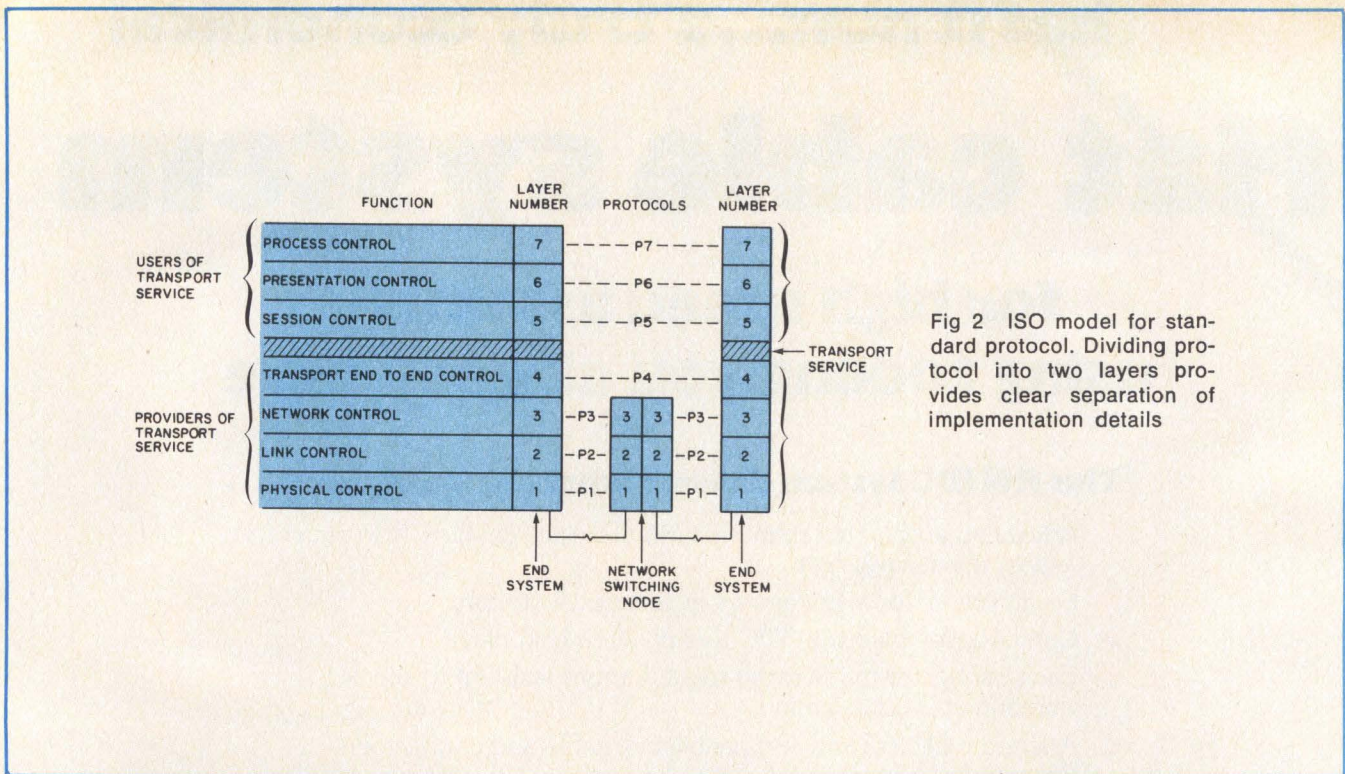


Fig 2 ISO model for standard protocol. Dividing protocol into two layers provides clear separation of implementation details

Recommendation X.25

Because public packet networks were being built in many countries, in 1976 the Consultative Committee on International Telegraphy and Telephony (CCITT) defined a standard interface for packet networks, called Recommendation X.25. The X.25 protocol defines three protocol levels: the physical link level (called X.21); the logical link control provided by a subset of high level data link control (HDLC); and the "Packet Level Interface" (called X.25 Level 3), which defines packet format and control procedures in terms of "virtual circuits." Goal of the X.25 interface is to provide a circuit oriented service to host system designers that is almost identical to the physical circuits they are used to, but with such low error rates, and with enough flow control, that higher level and end-to-end protocols need not be concerned with error and flow control. Control packets between host and network provide for call establishment and call clearing; data packets are sent over established circuits. Flow and error control over each virtual circuit are handled by HDLC-type "window" mechanisms applied to the host-to-network portion of the virtual circuit. Once the communication subnetwork has acknowledged a packet on Level 3 at the input end, the network accepts responsibility for delivering to the destination address a correct copy of the packet, in the correct order with regard to other packets sent over the virtual circuit.

Movement Toward Standardization

The widespread availability of computer communication has brought into focus the need for greater standardization of communications protocols. In particular, a study committee of the International Standards Organization (ISO) has recently formulated a model (Fig 2) that identifies seven hierarchical protocol levels, divided into two groups, "providers of transport service" responsible for moving the data from one place to another, and "users of transport service" which are the programs which generate and process the data. The purpose of dividing the

architecture into a number of layers is primarily to provide a clear separation of implementation details. Thus, for example it should be possible to make changes to the physical link without affecting levels 2-7, or to change a packet-switching network to a circuit-switching network without affecting levels 4-7.

All of the developments relating to host protocols mentioned above have been aimed at facilitating the interconnection of products from many vendors. Of course, many major vendors have developed their own network architectures, attempting both to maintain a level of support for older products, enabling customer network evolution, and to provide unique facilities or modes of operation which will further lock existing customers into using the vendor's own products. The dominant vendor in this category is International Business Machines with its Systems Network Architecture (SNA).

Knowledge of host protocols will continue to develop for the next few years, especially in research environments. However, even as knowledge is increasing, international standards and vendor architectures will be solidifying rapidly and there will be growing resistance to change by the majority of computer network users. It is likely that X.25 will, more and more, become the standard host protocol, possibly with some modifications in its current form. Vendor architectures may also move toward the standards, even though this has not been the case, especially with IBM, in the past. The average institution will have multiple computers, they will not be all from the same maker, and the owner will want them to communicate. Standard host protocols are the mechanism to make this possible.

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1. S. D. Crocker *et al*, "Function-Oriented Protocols for the ARPA Computer Network," *AFIPS Conference Proceedings* 36, June 1970, pp 271-279
2. V. G. Cerf and R. E. Kahn, "A Protocol for Packet Network Interconnection," *IEEE Transactions on Communications*, May 1974, pp 637-648

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Just one more thing: We know it hurts to drop Intel for somebody else. We've been through it

ourselves. But it's going to hurt a lot more next year. By then your competitors could be so far ahead of you, you might never catch up.

Call Advanced Micro Devices and we'll send you everything we've got on the AmZ8000. Or come to one of our seminars. Or sign up for a course on the AmZ8000.

Better yet, buy an AmZ8000. Check it out for yourself. Put it through its paces. Compare it with the 8086.

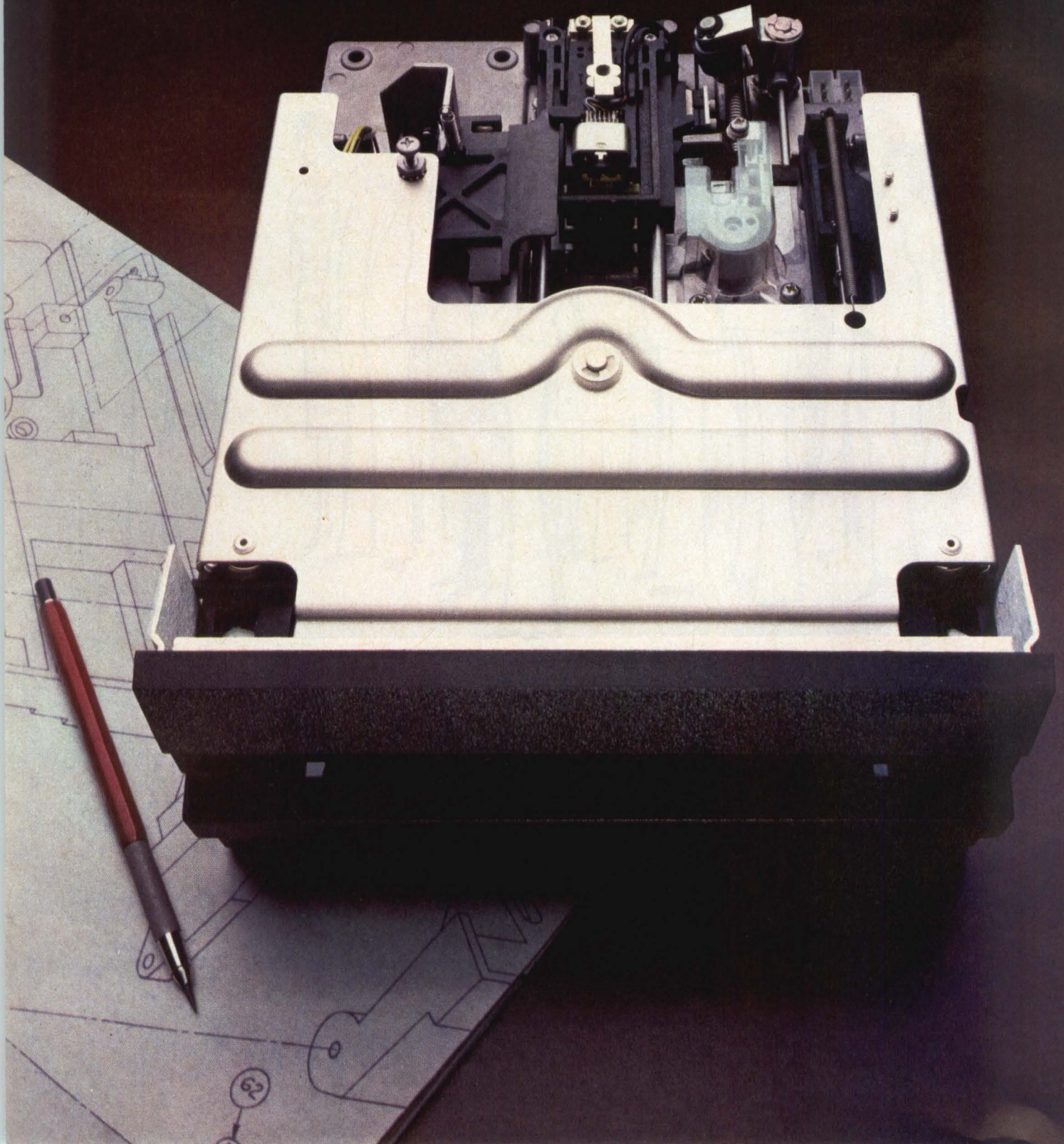
Intel can beat their chests all they want. But they can't beat the AmZ8000.

Advanced Micro Devices 

901 Thompson Place, Sunnyvale, CA 94086

CIRCLE 16 ON INQUIRY CARD

**HOW MFE CAME UP
WITH THE MOST ACCURATE,
MOST RELIABLE, AND
MOST EFFICIENT
DOUBLE-SIDED FLOPPY EVER BUILT.**



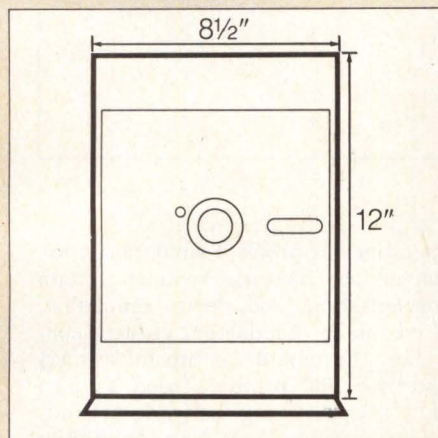
When diskettes went double-density, and later double-sided, drive manufacturers tried to adapt their original single-sided technology.

But at MFE, we saw that the old technology would simply be stretched to its limits. It was time to start again.

So based on where diskettes already were, and where they were headed in the future, we designed an entirely new disk drive from the ground up. For totally new levels of precision. And the results are dramatic.

Our drive not only handles double-sided diskettes with ease, it even anticipates still greater disk densities—such as double-track and quad-density designs.

SMALLER IS BETTER.



The smaller package is a more stable base for high density disks.

We started with the packaging scheme.

If you lay a standard 8" diskette on top of the MFE drive, you'll discover that the drive is barely larger than the diskette itself. It actually approaches the theoretical minimum size for a drive.

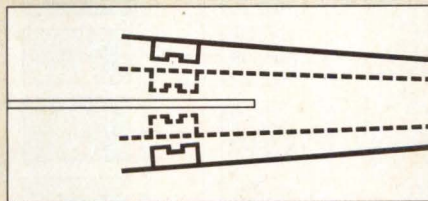
By keeping internal dimensions small, we achieved the tightest mechanical tolerances of any drive on the market. For example, only 3.4" separate the disk spindle from the stepper capstan, a reduction of 54% over the largest selling drive. And the baseplate, on which everything else is built, is a full 2 1/2" to 3" shorter. So no moving part in the drive moves further than it has to.

And since we were designing from scratch, we made the entire drive

modular. You can get to all the important components easily, and remove them without scraping your knuckles or taking apart the drive.

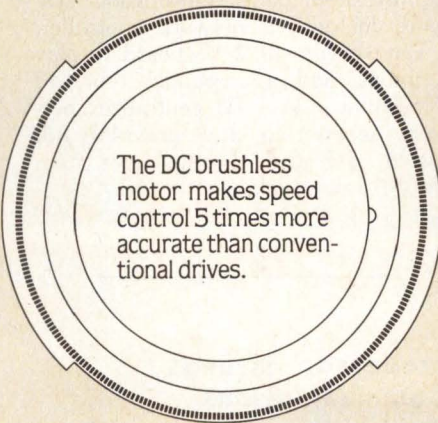
The new packaging alone yielded significant improvements. But we went much further.

THREE KEY INNOVATIONS.



IBM-compatible head eliminates scoring. Both heads move when unloaded.

1. To handle the double-sided problems, we designed a true IBM-compatible head, including tunnel erase. Both heads, when unloaded, move completely away from the diskette surface, eliminating any head or media wear.
2. We introduced a unique half-step positioning motor that drastically reduces error tolerances in track registration. Because the motor takes 154 steps per diskette side, instead of the usual 77, it operates far more smoothly and more accurately. In fact, it is 3 1/2 times more accurate than the largest selling drive. And it's designed to be able to handle twice the number of tracks per inch.
3. Finally, we developed an optional DC brushless motor. In one stroke, we reduced speed variation of the disk spindle from 2% to a mere 0.4%. We decreased power consumption by 30 watts, and increased drive efficiency by



an incredible 60-80%. And the DC motor runs so cool, you may even be able to mount multiple drives without a fan.

A NEW GENERATION.

The MFE drive is the only second generation double-sided drive, built from the ground up for higher precision and more reliable performance.

Where other companies have reached the end of their technology, we're just beginning.

And you can get our advanced design in single-sided versions, as well as double-sided.

WE'RE SHIPPING NOW.

In volume. From manufacturing facilities in the U.S. and Europe.

If you'd like a complete demonstration, call toll-free 800-258-3884.

And we'll show you the next generation of floppy disk drives.

(If you're outside the continental U.S. call the appropriate office listed below.)

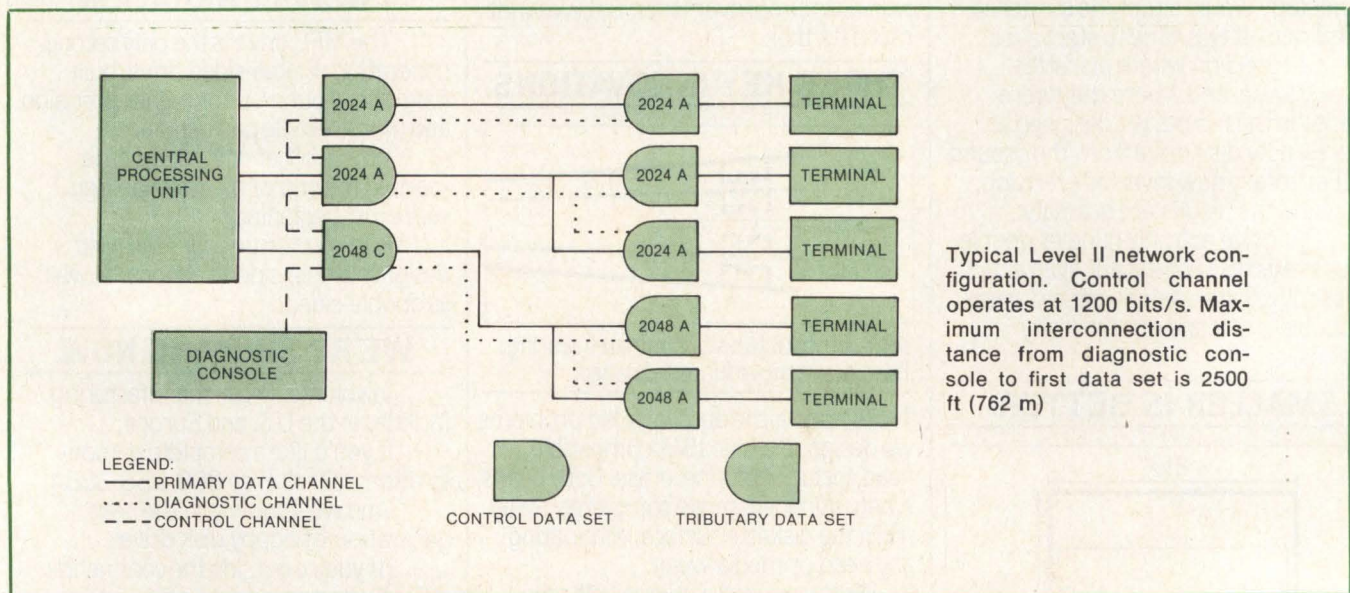
U.S. Headquarters: MFE Corporation, Salem, NH 03079, Tel. (603) 893-1921, TELEX 947477.
West Coast Sales Office: Irvine, CA, Tel. (714) 851-0281.

European Headquarters: MFE Limited, West Lothian, Scotland, Tel. (0589) 410242, TELEX 727827.
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MFE has worldwide distribution. In Europe, contact MFE Products Sa, Vevey, Switzerland, Tel. 021/52 80 40, TELEX 451173, for the distributor nearest you.



Modular Data Transmission and Diagnostic Subsystem Services Three Levels of Network Complexity



Dataphone[®] II is a hierarchical modular service offered in three levels for applications in data transmission systems, ranging from a simple single channel to large sophisticated networks. The service is based on a new generation of microprocessor based data sets that incorporate realtime diagnostic management in synchronous, 4-wire, full-duplex private line service at 2400, 4800, and 9600 bits/s, on either multipoint or point to point circuits. Tariffs have been filed for the service by Bell operating companies, with a uniform tariff rate throughout all participating telephone companies, according to AT&T, 195 Broadway, New York, NY 10007.

The new datasets are the 2400-bit/s 2024A, 4800-bit/s 2048A and 2048C, and the 2096A, which provides 9600-bit/s transmission plus multiplexing capabilities. The 2048C offers 20-ms quick startup for use in multipoint applications.

Level I systems management consists of one or more basic systems; a control data set and one or more tributary sets comprise a basic system. Level I offers central site control, continuous system monitoring, automatic location and diagnosis of system faults, and test and command menus. RS-449 and RS-232 interfaces can be intermixed with user terminals and frontend processors. With

the new RS-449 interface, data sets can be located as much as 4000 ft (1219 m) from user devices.

Level II includes all the capabilities of Level I, but also provides a single central site diagnostic console for control of multiple "basic systems." Testing and commands can be issued to any data set in the network (see Figure). Network faults are displayed on the console front panel in real-time; a maximum of 50 faults can be retained in memory.

Level III of Dataphone II service, designed for the management of more sophisticated data transmission systems, includes a network controller, a Dataspeed[®] 40/2 keyboard display terminal, and an optional type 43 teleprinter. Level III centralizes network monitoring and provides full system diagnostic management from the 40/2 terminal.

Processor Extends Communications Capabilities

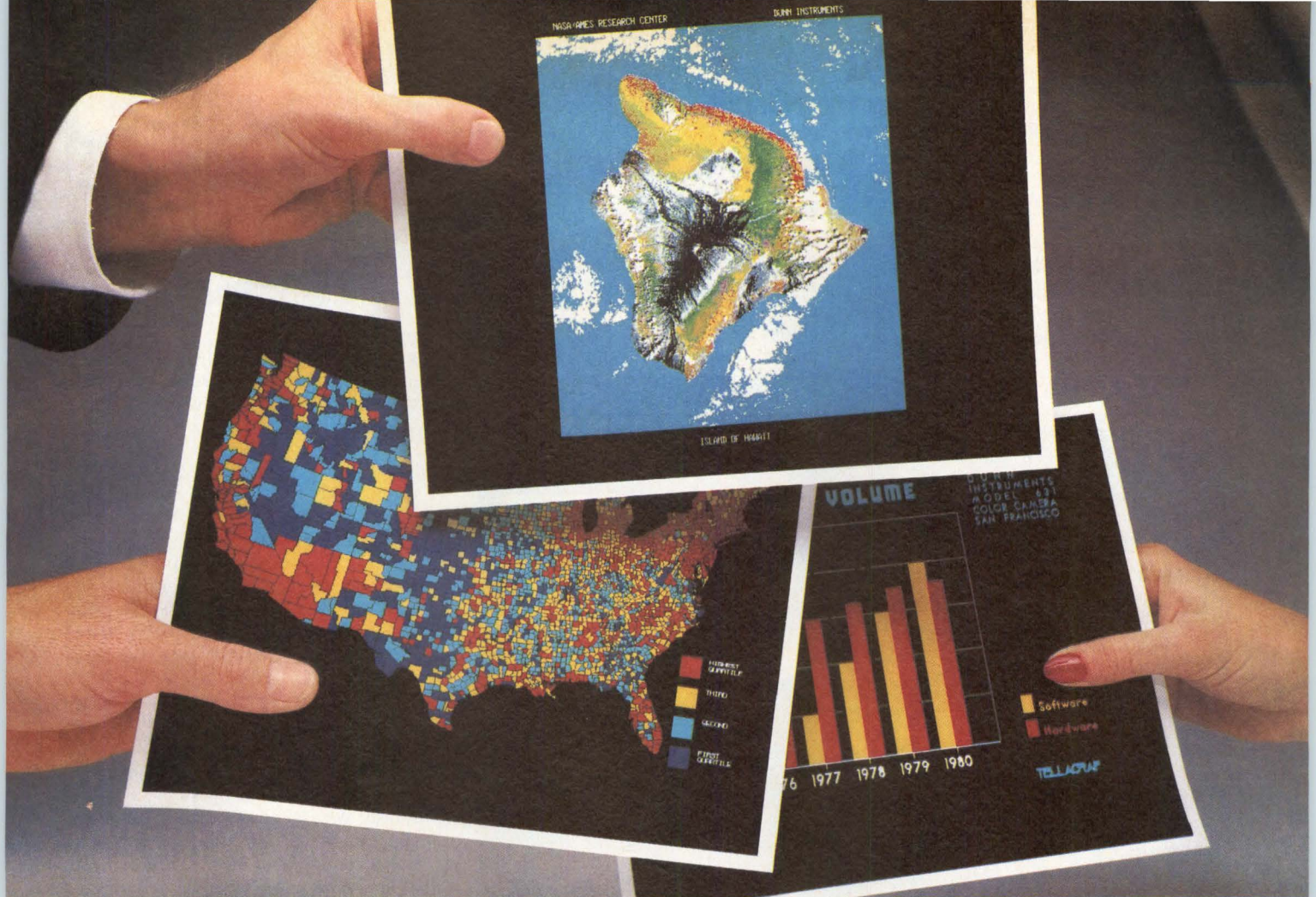
A microprocessor based extended communications processor (ECP) offers in a single unit such functional

operations as protocol emulation, code conversion, message switching, data concentration, and device emulation. Used as a standalone cluster controller, the unit drives up to 16 CRTs and two line printers; used as part of a teleprocessing network, it adds extensive communications capabilities to existing systems without software modifications.

Available from Datastream Communications, Inc, 430 Valley Dr, Brisbane, CA 94005, ECP can accept any RS-232-C device and translate its function to line protocol for transmission, or emulate another RS-232-C device for message switching, permitting full compatibility and data transparency with the data products of a broad range of manufacturers.

Resource data switching capabilities offer work stations a menu choice between minicomputers, mainframes, or service bureaus, enabling distribution of large applications over more than one system, or dedication of any application to specific machines.

The ECP comes programmed with standard line protocols and display drivers, or programmed for special user requirements. The system drives any combination of asynchronous TRV-compatible ports, CRT display stations, and synchronous communications, direct connect, and printer ports, up to a maximum of 20 ports.



Actual 631 images on Polaroid instant 8x10 film.

Color hard copy is finally at hand!

Color hard copy: the luminescent electronic image, captured in the permanence of photographic prints and transparencies. Dunn Instruments makes it brilliant, accurate and effortless to obtain from an affordable system. At last you can hold the new computer graphics and digital images in your hands.

The source is the 631 Color Camera System. It packs a high resolution, high linearity CRT, sophisticated optics and microprocessor exposure control into a compact, fast and friendly unit. For instant hard copy for immediate analysis, use it with Polaroid Type 808 film to make stunning 8x10 color



prints. Add the optional motor-driven 35mm system for beautiful color slides. Or load 8x10 transparency film and produce

images you can project overhead.

The 631 economically records the data from any raster scan CRT, for presentation, reproduction, access and display. Applications range from management information graphics to satellite remote sensing. Call or write for more information. We'll arrange for you to get your hands on actual results from the 631 Color Camera System.

Dunn Instruments, Inc.,
544 Second Street, P.O. Box 77172,
San Francisco, CA 94107.
415/957-1600.

The 631 COLOR CAMERA SYSTEM

DUNN INSTRUMENTS

"Polaroid" is a registered trademark of the Polaroid Corporation.

LANDSAT image courtesy NASA-Ames Research. Cartographic study courtesy Harvard Laboratory for Computer Graphics. Management information graphics courtesy ISSCO.

CIRCLE 18 ON INQUIRY CARD

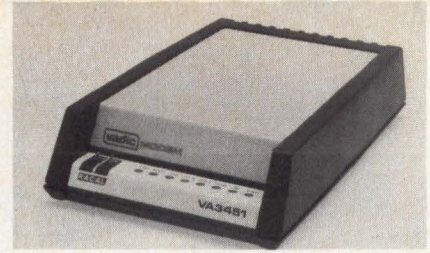
ECP may be upgraded by plugin of new discrete and independently operating CPUs. It will operate up to eight CPUs simultaneously, and address as much as 1M bytes of main memory.

A rack, completely integrated with Bell-compatible direct-connect modems, is optional. It features an autodialer for servicing up to eight modems of any speed or line mix for the DDD network.

Circle 400 on Inquiry Card

Triple Modem Serves Remote Originate/Answer Functions

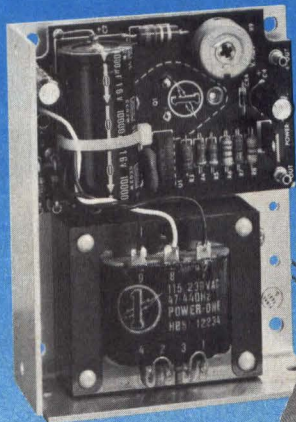
The VA3450 series of triple modems combines Bell types 212A, 103, and VA3400 in a standalone package and has been specifically designed for remote terminal use. The series includes six switched network originate/answer models, all registered for direct connect under part 68, FCC



VA3450 triple modem. In addition to 212A and 103 modes, remote terminal user gets VA3400 features, including capability for acoustic coupling

\$24.95

...AND HOLDING



Model HB5-3/OVP

5V at 3A with Built-in OVP

Power One's B Case models started at \$24.95. Over 100,000 models and five years later, they're still only \$24.95!

- 115/230 VAC Input
- OVP Built-in
- .05% Regulation
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- 2-Hour Burn-in
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rules. There is also a version for leased line applications. According to spokesmen for Racal-Vadic, 222 Caspian Dr, Sunnyvale, CA 94086, a single modem at the remote terminal site can satisfy every conventional originate/answer application for switched network full duplex data transmission from 0 to 1200 bits/s.

A VA3450 at the remote terminal can call three different types of modems, 212A, 103, or VA3400, with automatic identification of the called modem. The unit operates synchronously or asynchronously. Circuit design prevents initiation of false remote loop when in the 212A mode. When combined with the company's previously announced VA3467 central site triple modem, the result is a flexible microprocessor based system for protection against obsolescence.

Diagnostics include idle test, analog loopback and busy out, digital loopback, and self test. A switch controlled "standard option" mode returns the unit to a standard configuration to speed up and simplify diagnostic procedures.

Prices for the VA3451 (212A, 103, VA3400) start at \$900; for the VA3452 (212A and VA3400), \$850; and VA3453 (103 and VA3400), \$825. Delivery is 90 days ARO.

Circle 401 on Inquiry Card

Programmable Data Monitor Features Operational Simplicity

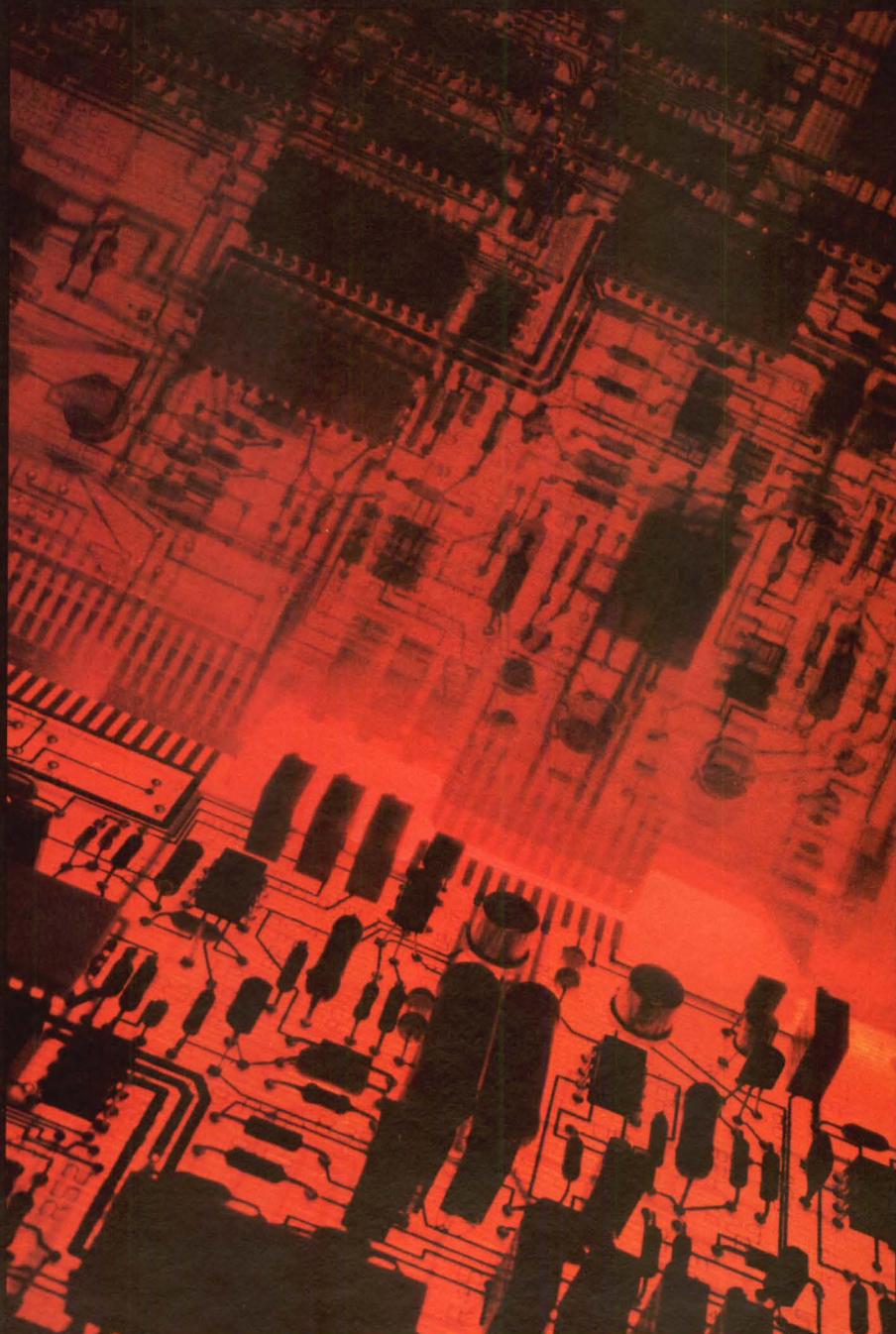
Self-teaching displays and color-coded keyboard simplify operation of the INTERVIEW 3000 series programmable data analyzers while enabling all modes of operation from basic data monitoring to sophisticated controlled monitoring. The unit comes

NATIONAL ANTHEM

SEMICONDUCTOR NEWS FROM THE PRACTICAL WIZARDS OF SILICON VALLEY

New 12 μ W LM385

Lowest power reference available.



LM335 — hot new linear temperature sensor.

LM359 amplifies on current amplifiers.

Dan Sowin talks about Maxi-ROMs.

Mil-temp PROMs for the masses.

Data Acquisition	Logic	Transistors	Hybrids	Linear	Interface	Bubble Memory
Memory Boards	RAMs/ROMs/PROMs	Transducers	Development Systems	Displays	Custom Circuits	Modules
	Microprocessors				Microcomputers	


LM335—the hot new temperature sensor that makes others obsolete.

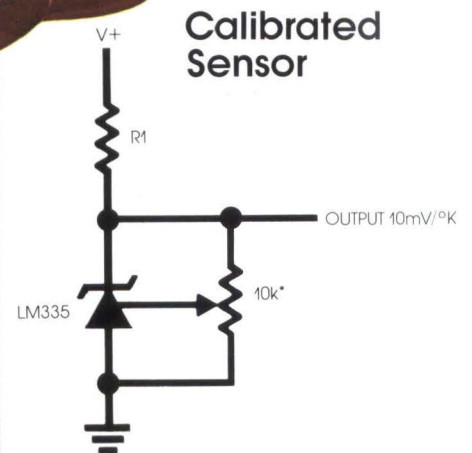
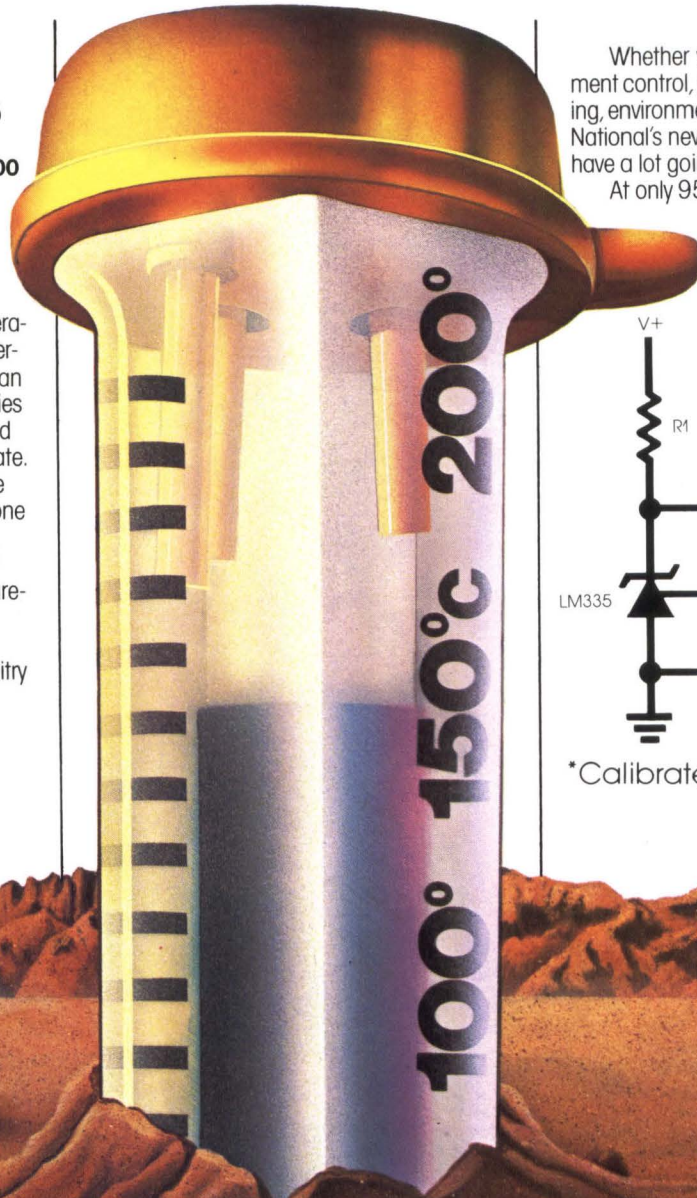
And since it's so easy to use and costs so little, the LM335 opens a whole new world of applications that were previously too expensive or too difficult.

The LM335 is a two terminal I.C. that looks like a zener with a $+10\text{mV/K}$ temperature coefficient. The LM335 is rated for operation over -55°C to $+100^\circ\text{C}$, and has an over-range up to $+200^\circ\text{C}$. Initial accuracies are available at 1°C , 3°C , 6°C ; but a third lead makes the LM335 very easy to calibrate. Typically, 1°C accuracy is achieved over the entire range when it's calibrated at only one temperature.

The low operating current means low error even for remote temperature measurement. Further, the LM335 eliminates the need for linearizing circuits, thus making interfacing to a readout or to control circuitry even simpler still.

Whether you're designing measurement control, protection circuitry, solar heating, environmental control or thermostats, National's new series of temperature sensors have a lot going for them.

At only 95¢, it's time to start sensing temperature with I.C.'s. 



*Calibrate for 2.982V at 25°C

New LM385 12 μ W micropower reference.

The lowest power reference available.

LM385 Design Features

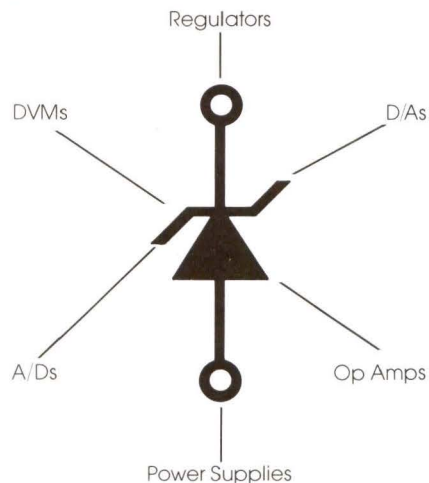
- operating current of 10 μ A to 20mA
- 1% and 2% initial tolerance
- low voltage reference (1.235V)
- stable under large capacitive loading
- low temperature coefficient
- low noise, good long-term stability
- 1 dynamic impedance
- replaces older devices with a tighter tolerance

The new LM385 is yet another example of National Semiconductor's commitment to supply high-performance references. Where power is a primary concern (as in battery-powered equipment, portable meters, or general-purpose analog circuitry with battery life approaching shelf life), this device provides performance unmatched by traditional discrete devices.

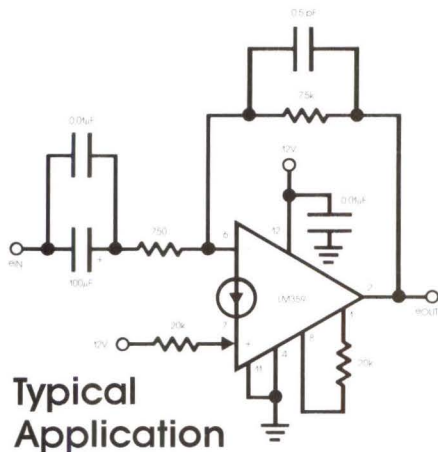
For applications requiring other reference voltages or performance specifications, National Semiconductor has the device you're looking for. For example:

V_{ref} 2.5V; 5.0V; 6.9V; 10V
Initial Tolerance as low as .01%
 T_{Cmax} as low as 0.5 ppm/ $^{\circ}$ C

Is it any wonder that more and more design engineers are looking to National Semiconductor's linear references to solve problems.



Amplifying on current amplifiers: National's new LM359.



When design engineers said they needed a low-cost dual that was similar to the quad LM3900, but with operation in the video frequency range, the R&D Group at National Semiconductor came up with the answer. It's the LM359 Dual, High Speed, Programmable, Current Mode Norton Amplifier.

The primary design emphasis was placed on high frequency performance and providing user-programmable amplifier operating characteristics.

Each amplifier is broadbanded to provide a high gain bandwidth product, up to

400MHz fast slew rate, 60V/ μ sec and stable operation. They're designed to operate from a single supply and can accommodate input common-mode voltages greater than the supply.

The LM359 solves a lot of applications problems: general purpose video amplifiers;

high frequency, high Q active filters; photo-diode amplifiers; wide frequency range waveform generation circuits.

Now design and application engineers have what they need, thanks to National Semiconductor.



"National is throwing its full sales and support strength behind its Static Maxi-ROM™ effort."

"When it comes to Static Maxi-ROMs, National Semiconductor is easy to do business with. In fact, the word around the industry is that National is just about the easiest company to do business with.

"It's not just that we have an outstanding line of products – 2K x 8 bits, 4K x 8 bits,



Dan Sowin
Director of MOS/LSI

and 8K x 8 bits. I think it's the fact that customers have come to realize, in ever-increasing numbers, that when they deal with National, they can order with complete confidence. All they do is submit their loaded PROM, sit back, relax, and their ROMs are delivered when they need them.

"National has a number of sales offices for customer convenience and a wealth of customer service personnel to handle orders quickly and smoothly.

"And to be quite honest about it, National is making an all-out push to dominate this marketplace. Obviously, that goes a long way toward explaining their outstanding prices, delivery schedules, and service.

"They're aggressively pursuing new business in a lot of different markets – for example, terminals, computers, home computers, mini-computers, instruments, toys and games, and word processing, to name but a few.

"So when you need Static Maxi-ROMs, call your local National Semiconductor sales office. If they can't help you, no one can."

Full Mil-temp 2716 ready at National Semiconductor.

There's good news for design and applications engineers who require full military temperature range 2716s. National Semiconductor now offers the part over the full military range, for all military and industrial applications – and it's available now.

The MM2716QM is a 2K x 8 μ V electronically programmable read only memory (ROM) in industry standard pin-outs, featuring a single +5V power supply and a guaranteed operating temperature range of -55°C to $+125^{\circ}\text{C}$. Maximum access time is 450 ns.

This new National Semiconductor product is used in support of their BLCs and microprocessors. It is also programmable using Starplex™. And it is designed and produced especially for military and extended temperature industrial systems where the extra margin of a full temperature part is needed.

The MM2716QM is functionally compatible with other existing 5V only 2K x 8 EPROMs. National Semiconductor is the first to make this product available in the full military temperature range – and it's stocked and ready for immediate shipping.

With National Semiconductor being the first to offer a full military temperature 2716, people will soon be talking about them as the source for MOS military EPROMs.

The Practical Wizards of Silicon Valley have done it again.

What's new from the National archives?

001 BLC 8737 Data Sheet

006 Special Functions Data Book (\$6.00)

007 Interface Data Book (\$6.00)

008 Pressure Transducer Data Book (\$3.00)

009 ROM MM 52116 Data Sheet

010 ROM MM 52132 Data Sheet

011 ROM MM 52164 Data Sheet

015 MST Program Brochure

016 LM159/LM359 Data Sheet

017 LM185/LM285/LM385 Data Sheet

018 LM135/LM235/LM335 Data Sheet

019 New BLC-8222 Double Density Floppy Disc Controller Data Sheet

020 MM 2716M Data Sheet

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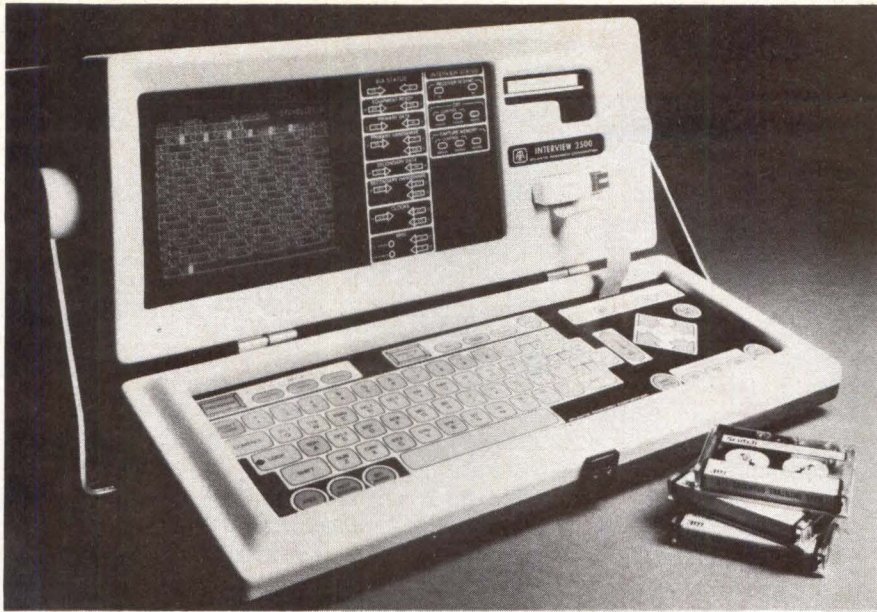
CD



National Semiconductor

The Practical Wizards of Silicon Valley.

NA4



INTERVIEW 3500 data analyzer. 7" (17.8-cm) CRT screen displays microprocessor prompted menu for operator choices, network characteristics, status information, and measurement results. Color coded, clearly labeled function keys simplify operator entries and commands

in either basic model 3000, or the 3500, which includes a tape drive. According to the manufacturer, Atlantic Research Corp, 5390 Cherokee Ave, Alexandria, VA 22134, a new concept in non-sequential programming allows the user to specify up to eight "trigger" conditions that will cause desired actions. This feature eliminates the need to learn a list of programming instructions such as jumps, subroutines, interrupts, or macroinstructions. Triggers are available to sense any combination of characters, interface leads, and internal flags.

Units operate in two modes. Monitor mode is for display and analysis, and gives operator realtime access to view data, a summary of program characteristics, and results from counters and timers. Program mode is for editing and entering the data monitoring program. A menu format and other prompting features guide the operator.

Data storage tapes hold 4M bits of data and interface status, plus the "capture" program to simplify later analysis of test results. Network performance measurements can be observed and reinitialized any time during the test. Statistical measurements include four counters and two timers.

The unit includes automatic self-test to verify proper operation of internal logic modules and firmware. Visual indicators and status messages

continually advise operator of operating mode and status. Software automatically controls, positions, and rewinds the tape.

The series allows simultaneous search for eight complex character strings of up to eight characters each. Strings include don't care, not equal, bit mask, and combined not equal and bit mask characters.

In bit oriented protocol (HDLC framing) mode, the CRT indicates good or bad blocks. Strings of up to eight characters permit indexing into definition bytes for SNA (SDLC) and for packets (X.25). Character string bit mask ability can select specific bits and ignore others, and the CRT can be controlled to display only a given address, group, packet, or form of a frame. Bytes are expanded into bits for detailed classification. NRZI is a standard feature.

Three preprogrammed training tapes for async, bisync, and bit oriented protocols, each with its training manual, are furnished with each unit, for significant reduction of operator training time.

Circle 402 on Inquiry Card

New

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can be separated

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<p>TAPE PUNCH \$1315</p> <p>50 ch/s - 50-60 hz - 5, 6, 8 Level Roll & Fanfold Payout</p> <p>Options</p> <p>RS-232C Interface* Take-up Reel/Bins - TTS Tape</p>	<p>TAPE READER \$670</p> <p>1,000 ch/s - 50-400 hz - 8 Level</p> <p>Options</p> <p>RS-232C Interface* Unwinder/Rewinder - Fanfold Bins 5, 7, 8 Level, TTS Tape</p>
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Based on CCITT Recommendation X.25 international packet switching protocol, the XODIAC network management system is a series of software packages that allow transparent data communications and resource sharing among multiple Eclipse[®] computers. This software enables advanced operating system (AOS)-based Eclipse users to establish direct computer-to-computer communications in a local environment, as well as connections on a global basis via public

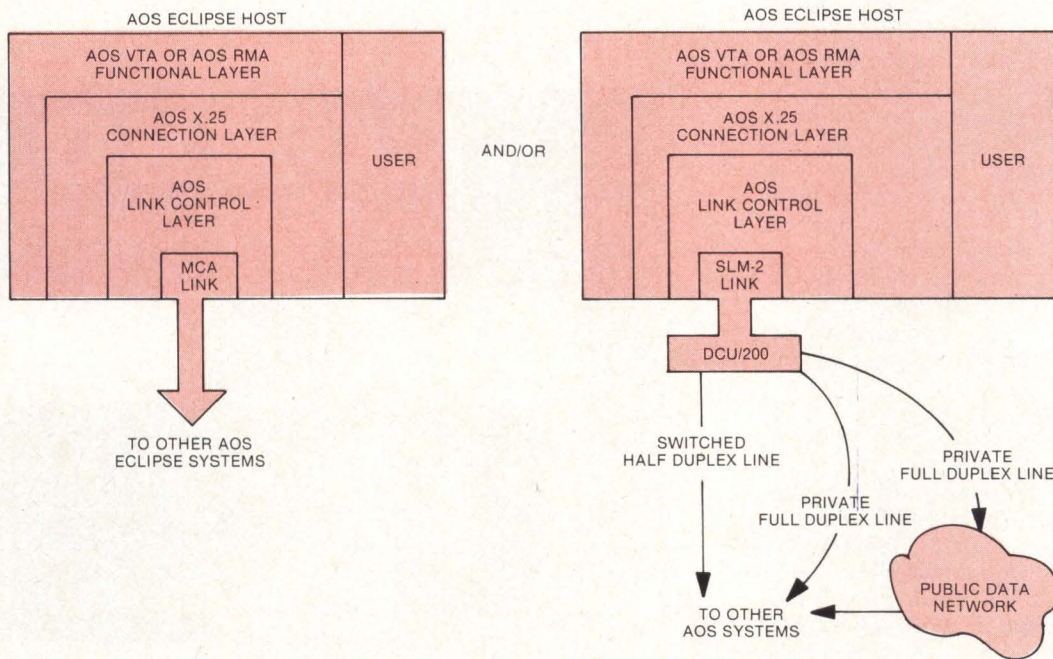
packet switched data networks that use the X.25 protocol. The system has been introduced by Data General Corp, Westboro, MA 01581, and has been certified by public data networks GTE Telenet in the U.S., DATAPAC in Canada, and TRANSPAC in France.

Hardware requirements for the XODIAC network are any Eclipse computer licensed to run AOS, at least 512k bytes main memory, and a synchronous line multiplexer (SLM-2) with a data control unit (DCU-200) for network connection or a multi-processor communications adapter (MCA) for high speed (1M bytes/s)

data transfer between locally connected Eclipse systems.

Specific software products include AOS X.25 (connection protocol X.25); AOS remote management agent (RMA); virtual terminal agent (VTA); network operator process (NETOP); and network generator program (NETGEN).

Modular architecture provides a transparent interface allowing resources on remote AOS-based systems to operate as if they were in the same location as the local system. It allows users to log on to remote AOS systems, access remote terminals and files, transfer files between systems,



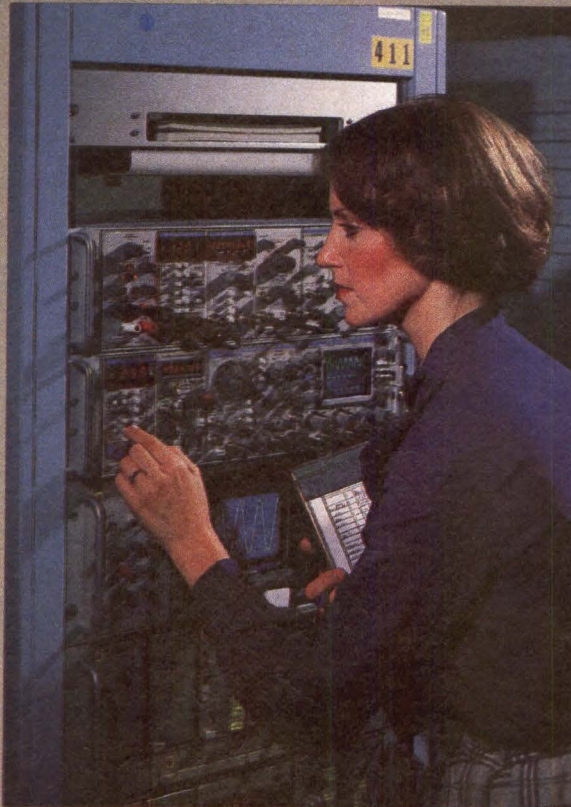
XODIAC/AOS software and hardware products. Link layer includes actual hardware used for intersystem links. Link control layer is software interface to physical link level. Connection layer segments messages into network packets and establishes and maintains logical connections between local and remote hosts. Functional layer performs necessary actions that permit users on one system to access resources and facilities on another

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Nearly 40 plug-ins let you create a per- sonalized instru- ment line-up.

With most test gear, it takes a lot of space and effort to create an instrument setup you can live with. The Tektronix TM 500 family makes it easy. All your instruments fit neatly and trimly into a single mainframe. One that contains almost any testing combination imaginable.

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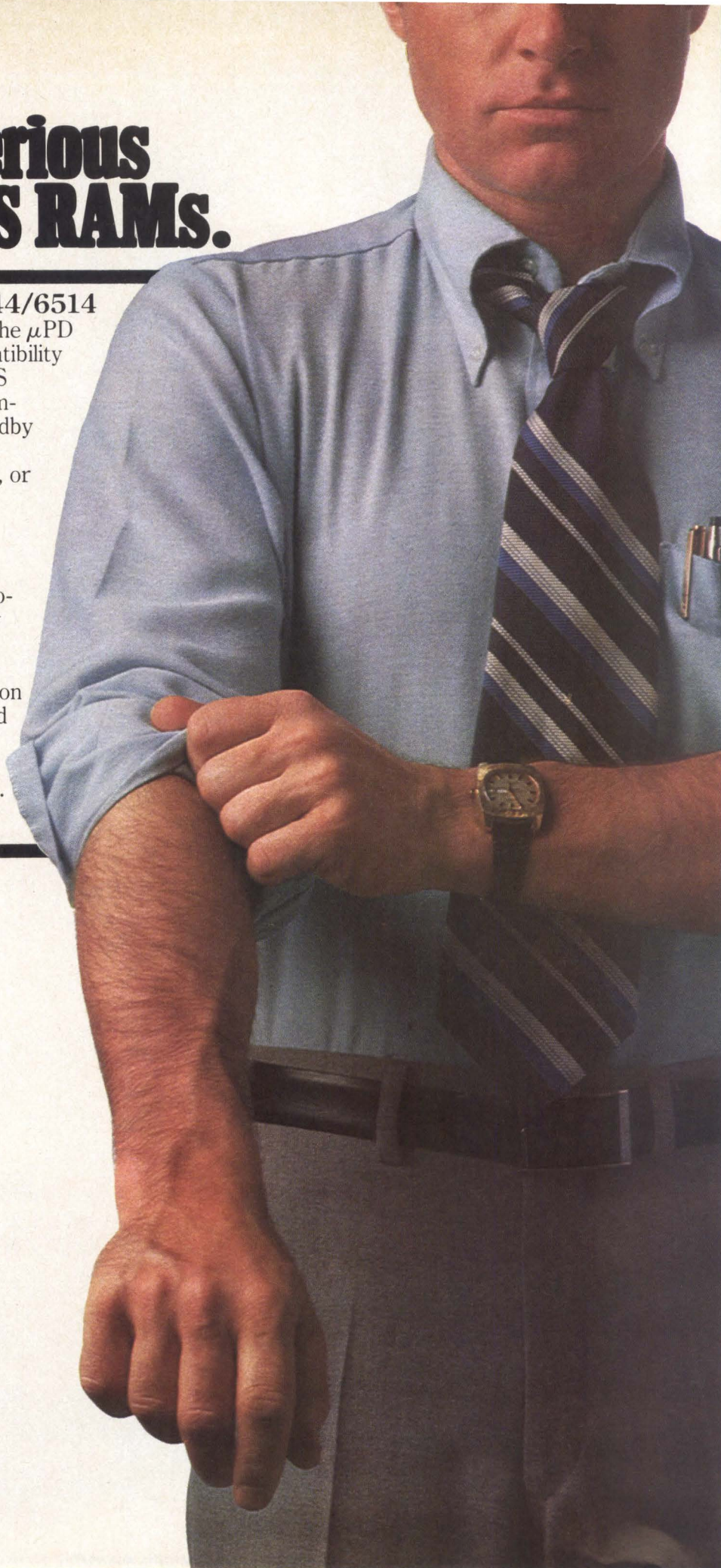
NEC gets serious about CMOS RAMs.

Introducing the μ PD444/6514

Our new 1K x 4 CMOS RAM, the μ PD444/6514, offers pin for pin compatibility with our industry-standard NMOS μ PD2114L. So whether your memory requirements call for low standby power down to 0.065 μ W, or high speed applications down to 150 ns, or a combination of both, NEC has exactly the part you need.

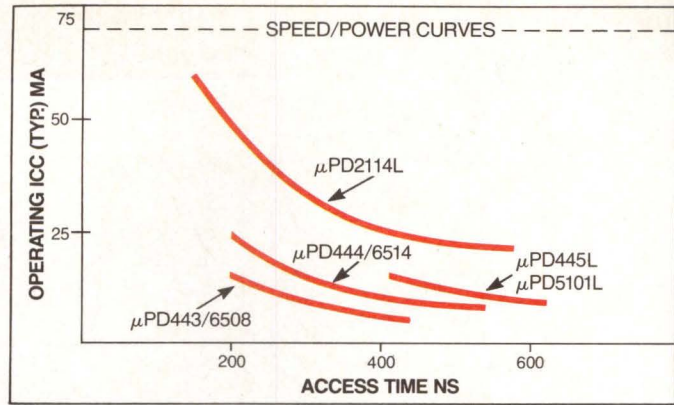
With our unique short channel length CMOS technology, we've designed the μ PD444/6514 to provide access and cycle times as low as 200 ns in the industry standard 300 mil wide 18-pin package. Like the μ PD2114L, it's manufactured on four-inch wafers — for low cost and high volume production. And the μ PD444/6514 will operate in a fully static or asynchronous mode.

The μ PD444/6514 is the latest



addition to our growing line of CMOS RAMs—a line that includes a 20-pin 4K RAM (μ PD 445L), a 22-pin 1K RAM (μ PD5101L), and an 18-pin 1K RAM (μ PD443/6508). And besides depth in products, we offer depth in support—including engineers available to help with specific application problems, plus complete documentation, testing, and special selection. Our 1979 product catalog contains full details on our complete line of memories, plus our 8-bit and 4-bit microprocessors and peripherals.

If you are in North America, you may obtain a copy by attaching your business card or letterhead stationery to this page and sending it to:
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PART NUMBER	ACCESS TIME	OP. POWER (TYR)	NO. PINS	STANDBY POWER (TYR)	LOW V _{CC} POWER (TYR)
μ PD444/6514C	450 ns	45 mW	18	.065 μ W	.022 μ W
μ PD444/6514C-1	300 ns	60 mW	18	.065 μ W	.022 μ W
μ PD444/6514C-2	250 ns	75 mW	18	.065 μ W	.022 μ W
μ PD444/6514C-3	200 ns	95 mW	18	.065 μ W	.022 μ W
μ PD445LC	650 ns	45 mW	20	100 μ W	1 μ W
μ PD445LC-1	450 ns	75 mW	20	100 μ W	1 μ W
μ PD5101LC	650 ns	45 mW	22	1 μ W	.016 μ W
μ PD5101LC-1	450 ns	75 mW	22	1 μ W	.016 μ W
μ PD443/6508C/D	450 ns	25 mW	16	5 μ W	.3 μ W
μ PD443/6508C/D-1	300 ns	45 mW	16	5 μ W	.3 μ W

Next time, think NEC.

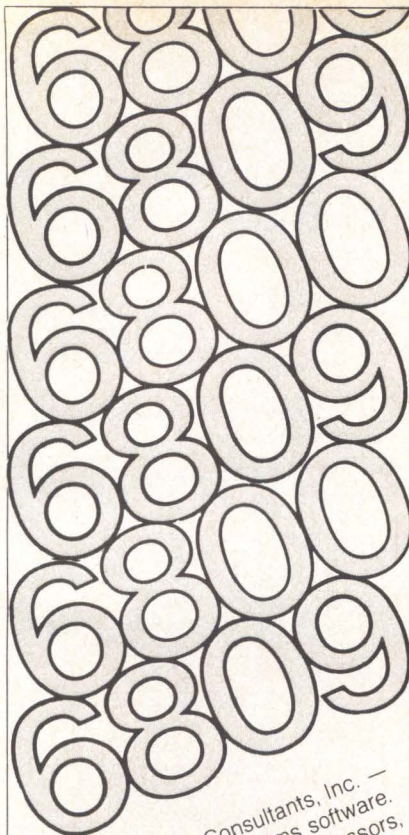
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COMMUNICATION CHANNEL

communicate with programs running on remote systems, access and use devices on remote systems, transfer data between the full range of the company's mini- and microcomputers, and control processes on remote AOS systems.

Compatibility of system software with Recommendation X.25 provides

the option of configuring networks using common carrier facilities or using public packet-switched data networks. The software may also be used for data transfer or resource sharing through hardwired links, or private facilities such as microwave links.

Circle 403 on Inquiry Card

CBEMA Files for Telecommunications Market Deregulation

The Computer and Business Equipment Manufacturers Association (CBEMA) has called for government deregulation of basic telecommunications services and equipment except in the case of monopoly-based common carriers such as AT&T and other carriers owning basic communications facilities.

In a filing with the FCC, CBEMA's comments on the FCC's tentative order on the restructure of the communications market (Computer Inquiry II) specifically stated that resale services (those services acquired from a common carrier through access to its transmission pipeline and subsequently resold) should not be subject to FCC regulation. The association said in its filing, "If the commission's goal is truly to foster a multiplicity of competitive suppliers with attendant price and innovation advantages, the intrusion of government supervision can only be self-defeating."

CBEMA urged free competition in enhanced nonvoice services, which use computer processing applications to act upon the form, content, or code of the information transmitted, and in customer premises equipment such as data terminals, telephone sets, and switchboards. The FCC proposed making some of this equipment available subject to tariff. The association pointed out that the competitive supply of much customer premises equipment was hampered by artificial constraints imposed by carrier tariff restrictions.

A key point in the CBEMA filing was a requirement for maximum separation between the common carrier and its resale entity, with the latter having separate officers, personnel, facilities, and accounting.

The association noted that a significant portion of the FCC's tentative decision dwells on the extent to which AT&T may be able to participate in the telecommunications market on an unregulated basis under the 1956 AT&T consent decree with the Justice Department (*Computer Design*, Sept 1978, pp 14-18). "The Commission should not be preoccupied with the marketplace status of any single entity—service supplier or user—and it should not design its overall policies simply to accommodate the unique circumstances of any one market participant."

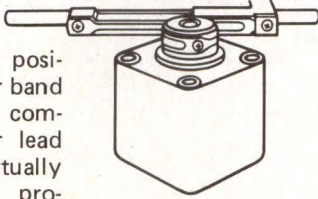
Computer Inquiry II was instituted by the FCC because of an apparent blurring of the distribution between regulated communications service and nonregulated data processing services which occurred since the Commission's initial inquiry into the question. Under Inquiry II, the FCC classified common carrier network services into three categories: voice, basic nonvoice, and enhanced nonvoice. The Inquiry proposed that enhanced nonvoice services be provided on a resale basis, with access to network services and the acquisition of underlying transmission facilities provided subject to tariff.

CBEMA is a national trade association of 36 small and large companies who represent more than 85% of the total business activity in the manufacture, sales, and service of computers and business equipment. □

Five Reasons Why Engineers Rate MPI's Dual-Head Mini "Technically The Best":

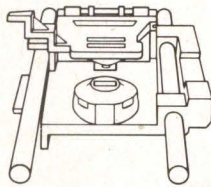
1. BAND POSITIONER

MPI's patented stepper-band positioner provides the industry's fastest access time (5ms) and most accurate positioning. The stepper band is simpler in design compared to a cam or lead screw. It is virtually frictionless, which provides extremely accurate and reliable positioning, yet requires the lowest power. As a result, it moves five times faster than other positioning systems.



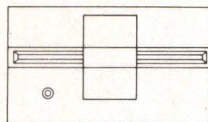
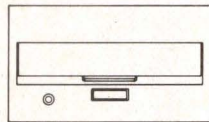
2. HEAD & CARRIAGE

Our high-performance mini floppy drive was developed as a dual-head, double-track, double-density unit. It is not an up-graded single-head, single-density design. The carriage and head concepts are based on IBM's — except for one important innovation: our bottom head is fixed, while only the top head loads. The heads are centered between two parallel rods (not cantilevered) to eliminate radial-positioning errors. To minimize media wear, we designed the longest head carriage which insures flatter head landings.



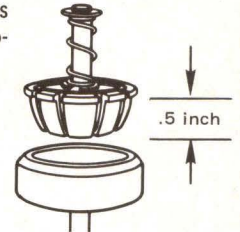
3. HUMAN ENGINEERING

Our dual-head (Model 52) and single-head (Model 51) drives are human engineered. Key features include: a full-closing, push-button front door to provide greater media protection; a patented ejector mechanism that makes diskette removal easier; and a choice of bezels.



4. DISKETTE CENTERING

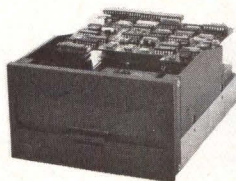
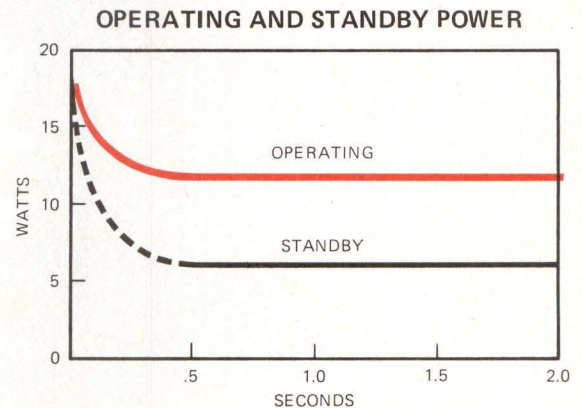
True diskette centering is accomplished by MPI's proprietary clutch mechanism. As the front door is closing, our extra-long clutch expands and gently engages the mylar media. When the clutch is seated, the diskette is locked securely in position to within .0008 inches. The result: most accurate positioning, longer diskette life, and trouble-free operation. MPI's diskette ejector — an industry first — pops the diskette out within easy finger-tip reach.



5. POWER CONSUMPTION

MPI drives have the industry's lowest power consumption (6W standby, 12W operating) due to the following:

- A high-precision stepper motor with Samarium-Cobalt magnets. This motor is accurate to 3%, has less heat dissipation, and longer life;
- Proprietary electronics, packaged on a single PCB, incorporating low-power Schottky; and
- A low-friction positioning mechanism.



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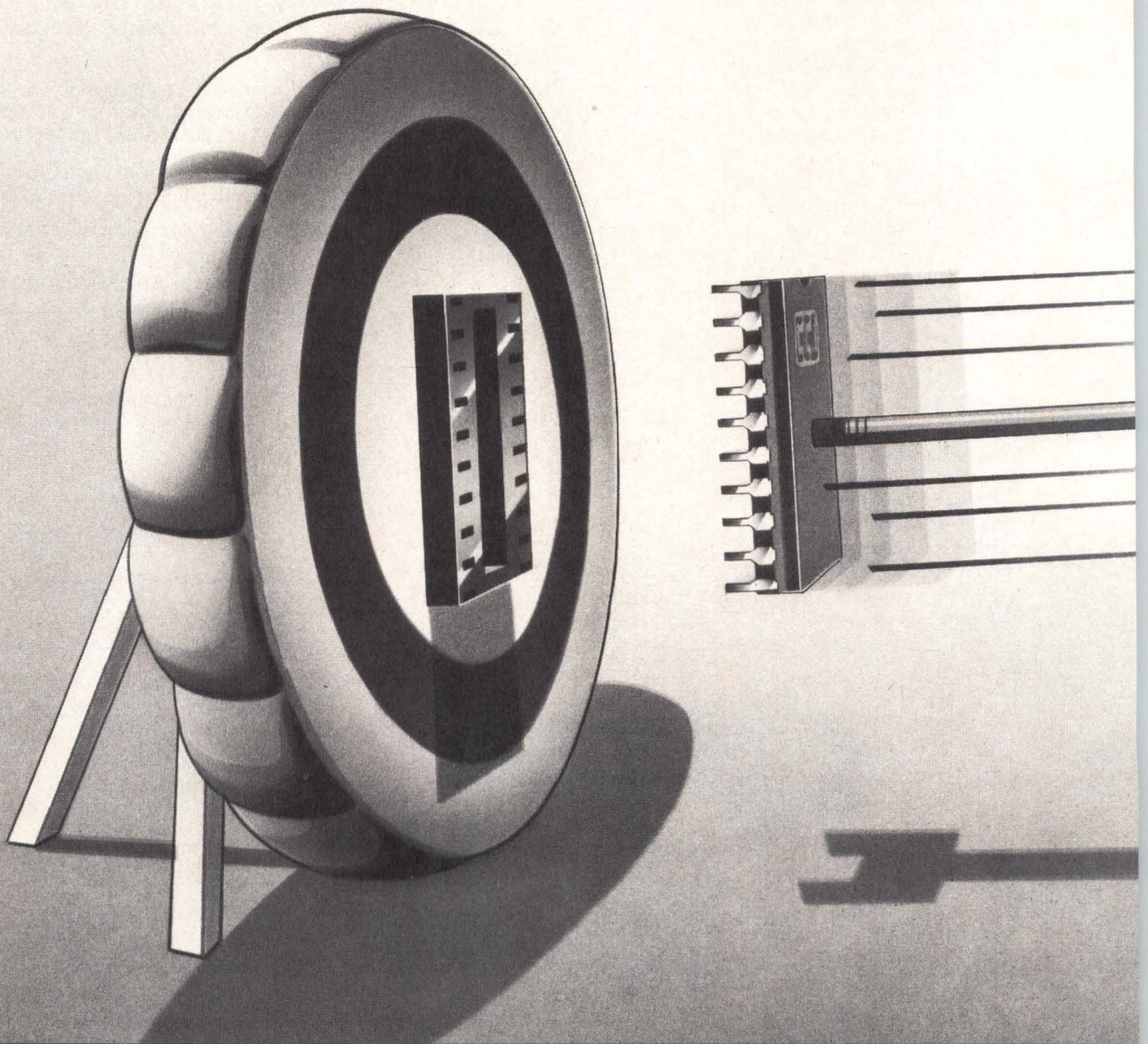
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You can choose from standard devices including the 74LS373 latch or 74LS374 register. Or save a socket with our optional inverted-output equivalents of these parts. A 32mA output option is available on several S latches and registers.

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And now . . . an octal transceiver.

Good news. We're adding to our line of interface and have begun production on a drop-in replacement for the popular 74LS245 transceiver.

Plus, six-week delivery on MIL-STD 883B interface.

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Cut your interfacing costs with a new line of interface devices, the 68 series, specially selected by MMI for microprocessor applications.

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TECHNOLOGY AND ECONOMICS: THE ENGINEERING AUDIT

Montgomery Phister, Jr

Systems Consulting
Santa Monica, California

A product's integrity—its capability, reliability, and safety—depends on the quality of the procedures which govern its development, manufacture, maintenance, and use, and on the care with which individuals follow those procedures. Where the product is complex, basic procedures are embodied in drawings and other documents which are created, updated, and controlled by the engineering or development organization. Other procedures in the manufacturing, maintenance, and sales organizations also affect product integrity, and many of them involve the interpretation and use of engineering controlled documents.

When an organization grows, both it and its procedures change, as responsibilities move from individual to individual, as operations are distributed geographically, and as problems arise and are identified and solved. The result may be a set of loosely connected procedures which, because of the way they evolved, insure product integrity under most circumstances but can lead to problems when people move, or when vendors, materials, parts, or responsibilities change.

A periodic audit of product related procedures in use throughout an organization should be conducted, to examine the procedures as a whole, and thus to identify areas where they are inappropriate or (more likely) incomplete. Simultaneously, or preferably as a second step, the audit should check to see whether the procedures are in fact followed properly, or whether they are misinterpreted or ignored. The audit may be conducted by someone from general management, by someone from one of the affected organizations, by a committee made up of members of the affected organizations, or by an outside consultant. This article will set

forth a possible framework for such an audit, and will provide a list of questions which might be asked.

The diagram shows those parts of the organization whose operations affect product integrity, and indicates the functions which should be audited. Answers to the following questions will help determine whether existing procedures are sufficiently complete to keep products intact despite external or internal changes.

In The Development Organization

Design Functions

(1) Choosing parts. (Designers should be encouraged to use parts already documented and used in the organization's other products.)

Is the collection of existing, documented parts suitably catalogued or described in a format useful to and available to the design staff? Is there a procedure for keeping this "recommended list of parts" up to date?

Is there a procedure for authorizing the addition of a new part as soon as the possible need for that part is identified—while there is still time to find an alternative, if the requested part is in fact not justifiable?

Does the set of procedures which govern introduction of a new part include:

Specifications for the content of documentation which describes the part?

Method for qualifying vendors authorized to supply the part, and for creating and maintaining a list of authorized vendors?

Method for procuring high level (eg, vice-presidential) approval for "sole source" parts—parts which only one vendor is able to supply?

NEC Spinwriters. Super terminals.

Six feature-laden models to fit any teleprinter network.

NEC Spinwriter™ terminals are fine-quality communications devices that are enriching thousands of terminal networks.

Users call them "super" terminals because Spinwriter devices are versatile, user-configurable, quiet, dependable, and print at rates up to 55 CPS.

They come in six models, including an APL/ASCII model. They have numerous operator convenience features. They are available in both RO and KSR configurations. And they offer a wide variety of forms handling options.

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Spinwriter terminals offer more forms-handling options than other terminals: vertical, horizontal or bidirectional tractors; and pin-feed, friction-feed, bottom-feed, front-feed and cut-sheet devices. Most are operator-changeable.

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CIRCLE 25 ON INQUIRY CARD

Introducing Microstreamer.TM The 100% solution to disk backup.

The Low Cost Solution! The MicrostreamerTM Tape Drive provides the unique disk backup benefits of ½ inch tape for a cost of less than half of a standard tape drive. Microstreamer's price includes formatting electronics, power supply, chassis – even UL and CSA approval. There is no more economical tape based backup device.

The Capacity Solution! Cipher's Microstreamer Tape Drive provides up to 46 Mbytes of data to backup even the largest capacity disk.

The Speed Solution! At 100 ips, the Microstreamer transfers 46 Mbytes of data in 4.8 minutes with full error correction. No waiting.

The Size Solution! 8¾ inches vertical. That's all the operator sees, since Microstreamer provides fully automatic loading from the front and is designed to be mounted in a compact desk system.

The Compatibility Solution! The phase encoded Microstreamer is ANSI and IBM compatible using standard 10½, 8½ or 7 inch reels so the user gets worldwide interchange and access to common database.

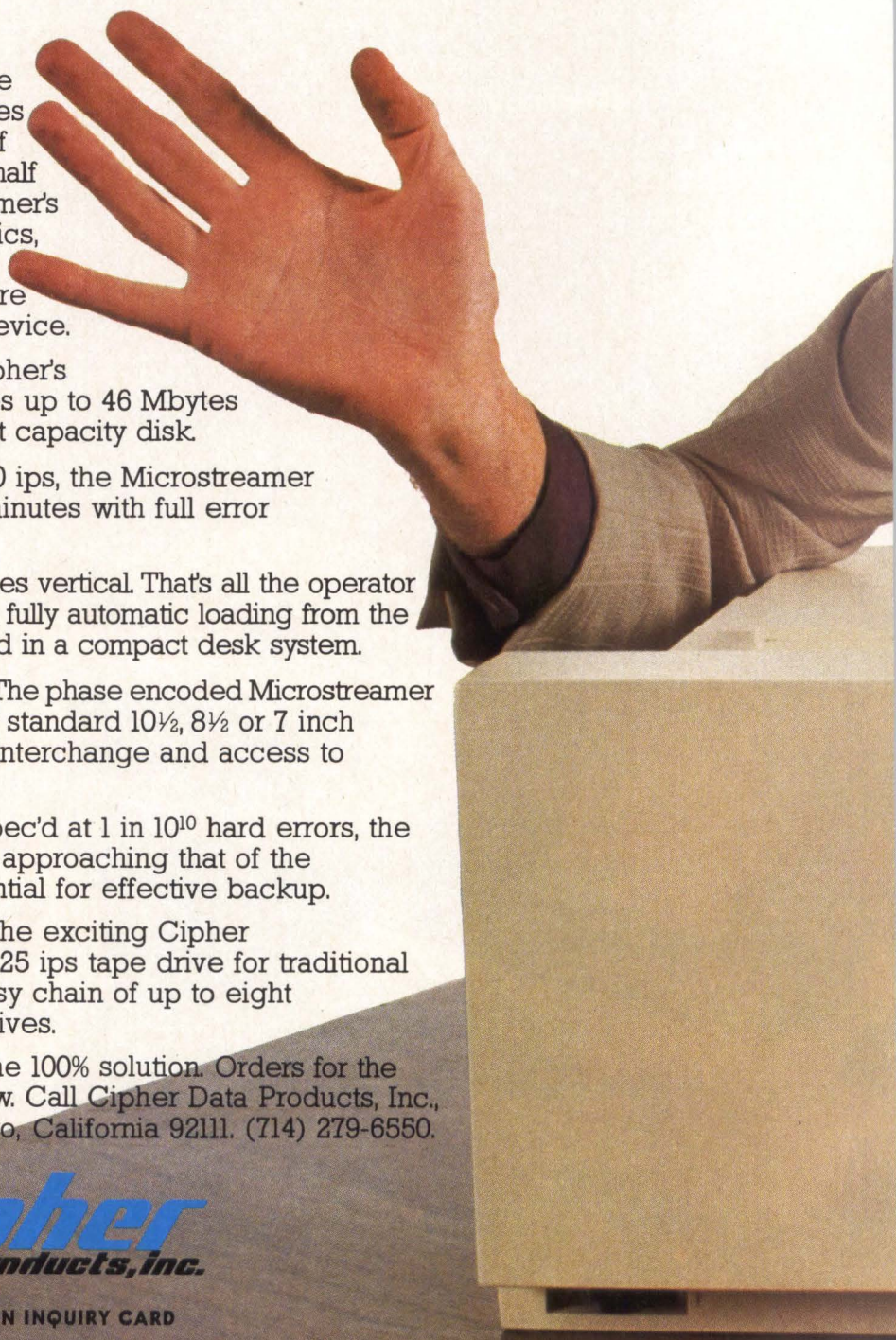
The Reliability Solution! Spec'd at 1 in 10¹⁰ hard errors, the Microstreamer provides reliability approaching that of the Winchester disk – absolutely essential for effective backup.

The Tape Drive Solution! The exciting Cipher Microstreamer also functions as a 25 ips tape drive for traditional applications and operates in a daisy chain of up to eight streamers and/or standard tape drives.

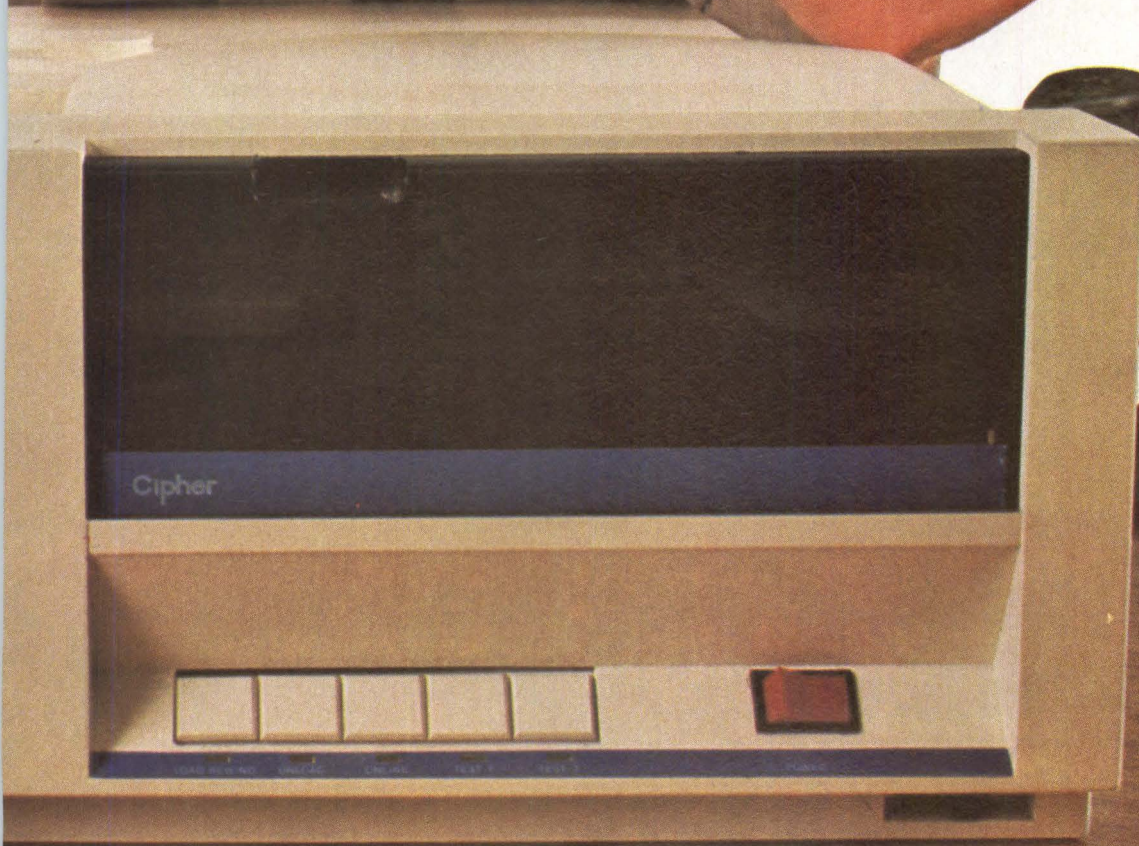
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0.3121AEJ

0.3120

0.3119

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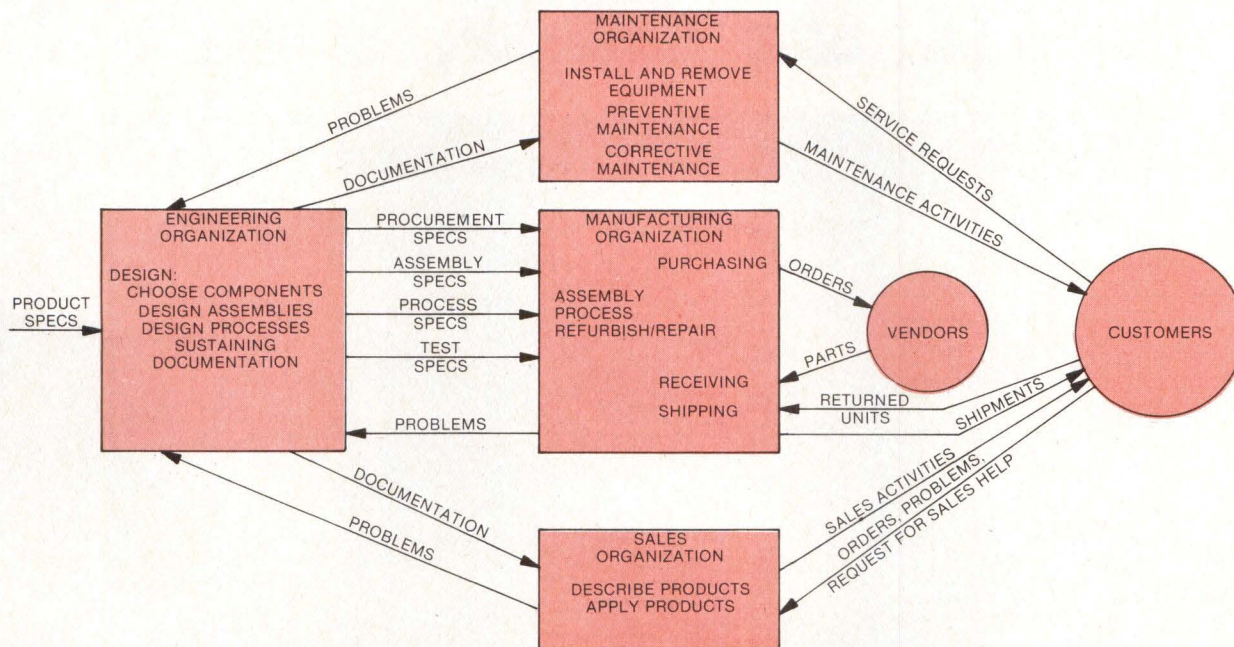
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CIRCLE 131 ON INQUIRY CARD



Organizations and functions subject to engineering audit. Blocks represent major organizational units whose procedures and operations affect product integrity. Major functions affected by engineering audit are shown in blocks. Lines connecting blocks show important formal communications between organizations. This discussion assumes that engineering controls product documentation during entire product life, that purchasing and receiving are part of manufacturing, and that maintenance is independent organization. However, audit questions are appropriate no matter how functions are organized. For example, manufacturing or maintenance may take over control of product sustaining (and therefore documentation) at some point, maintenance may be part of sales organization, or purchasing may be independent entity

Specifications for special tests or measurements that should be made by the receiving organization in manufacturing, when a batch of parts is received?

(2) Designing subassemblies and assemblies. (An assembly is a combination of two or more parts connected together by mechanical means.)

Do design procedures encourage system planners to make use of existing assemblies and subassemblies wherever possible in the design of new products?

Are design reviews, conducted by senior engineers and aimed at insuring product integrity, a regularly scheduled part of the development process? Do members of the manufacturing and maintenance organizations participate in these reviews, as appropriate, to provide suggestions regarding product reliability, maintainability, and manufacturability?

Is the product specification, which serves as the basis for the development project, complete? Does it include sections covering functional, performance, environmental, user safeguarding, reliability/maintainability, and manu-

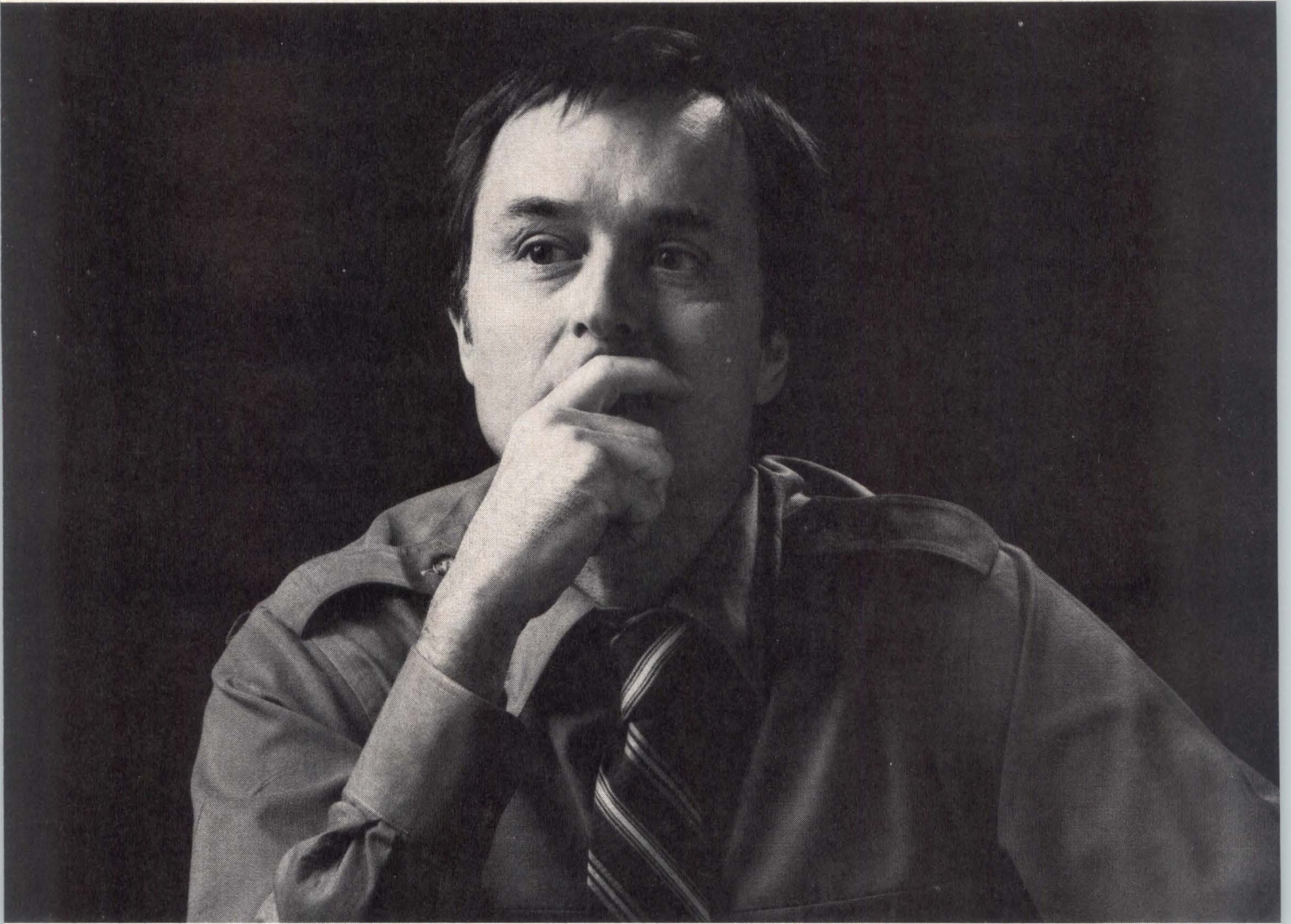
facturing cost objectives? Do the development test (including product verification) steps in the development process explicitly measure product characteristics against this specification?

(3) Designing processes. (A process is a method for creating a part by combining materials, wherein a physical change of state or a chemical action takes place. Soldering and molding are examples of physical processes; etching and plating are examples of chemical processes.)

Are processes documented in enough detail that they can be set up and carried out by manufacturing with no help or participation by the development organization? Does process documentation include specifications for input materials, for process equipment, conditions, and procedures, and for in-process measurements and tests? Are the details of process documentation consistent with the purchase specifications used in procuring materials used in the process?

Many processes cannot be so documented, and are typically developed over a period of time in a joint

"WHAT THIS COUNTRY HIGH SPEED, SUPER-



YOU GOT IT.

It's called the IM7147. And Intersil makes it. It's a low-power, 4K static RAM with 55ns access times.

	Operating Power	Standby Power	Access Time
IM7147	125mA	20mA	70ns
IM7147L	100mA	10mA	70ns
IM7147-3	125mA	30mA	55ns
IM7147L-3	110mA	20mA	55ns
(military) IM7147LM	125mA	20mA	85ns

Now, you're probably thinking you'll have to pay an arm and a leg for that combination of performance. Not so. Intersil 4K statics are super competitive with anything even near to equivalent in the market today.

SAVE BIG BUCKS.

Sure, you'll save when you buy from Intersil. But, you're going to see even greater savings when you start designing the 7147 into new systems. It's great for high-speed, large memory applications. Because it runs on a smaller power supply and it needs only a fraction of the cooling other RAMs require. Lower power dissipation also means greater reliability for the entire system.

NEEDS IS A LOW-POWER 2147."

A FAMILY THAT WON'T QUIT.

Don't get us wrong. We have the high-performance 4Ks, but we also have a raft of the regular 4Ks. So, if you need standard 2147s for existing sockets, we've got you covered. Same with 2114s and 7141s (2141s).

Any way you slice it — 1K x 4 or 4K x 1, low-power or industry standard, commercial or military — Intersil's got your part. At a competitive price. And we're quoting immediate delivery. Off the shelf. It you don't believe it, just try us with an order.

COMING ATTRACTIONS.

Sounds like we have our act together, right? Well, we're not stopping there.

To give just a peek at the future, in first quarter 1980, we'll be bringing out the IM7148. It's a new high-performance, low-power 4K especially well-suited to mainframe memories.

FROM THE LOW-POWER WHIZ KIDS.

Actually, it shouldn't surprise you that Intersil is doing all this. Since we're known for our innovation in CMOS technology. But it hasn't been by accident. We've focused on it. Because one of the things we thought this country needed was a good low-power technology company.

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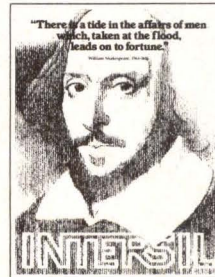
Advent (IND, IA) • Alliance • Arrow • Bell Industries • CESCO • Component Specialties • Components Plus • Diplomat (FLA, MD, NJ) • Harvey (upstate NY) • Intermark • Kierulff • LCOMP • Parrott • R.A.E. Ind. Elect. Ltd. • RESCO/Raleigh • Schweber • Summit • Wyle • Zentronics Ltd.

INTERASIL NMOS STATIC RAM FAMILY		Operating Power	Access Time
1K x 4	IM2114-2 (D2114-2)	100	200ns
	IM2114-3 (D2114-3)	100	300ns
	IM2114 (D2114)	100	450ns
	IM2114L2 (D2114L2)	70	200ns
	IM2114L3 (D2114L3)	70	300ns
	IM2114L (D2114L)	70	450ns
	IM7114L2	50	200ns
	IM7114L3	50	300ns
	IM7114L	50	450ns
	4K x 1	IM7141-2	70
IM7141-3		70	300ns
IM7141		70	450ns
IM7141L2		50	200ns
IM7141L3		50	300ns
IM7141L		50	450ns
1Kx4		D2147	160
	D2147L	140	70ns
	D2147-3	180	55ns
	IM7147	125	70ns
	IM7147L	100	70ns
	IM7147-3	125	55ns
	IM7147L-3	110	55ns
	MD2147	180	85ns
	IM7147LM	125	85ns

Military temperature available in all devices.

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Wow! Am I ever interested in your 4K static RAMS.

____ Please send me information on your RAM line.
____ And include your 20 x 24" Shakespeare poster. I like that idea, too.

Name _____

Company _____

Address _____

City/State/Zip _____

engineering/manufacturing pilot operation. Such processes are potential sources of trouble and should be examined with care. Is existing documentation up to date—did process modifications derived in the pilot line get incorporated into the documentation? Is process operation critically dependent on the participation of some key individual, or on the proper functioning of some special equipment? Can the process be put into operation at some other plant?

Sustaining Functions

Are there procedures which:

Establish the communications paths and documents used by manufacturing, maintenance, and sales to describe problems to engineering?

Govern engineering's response to such problem descriptions? The response should include setting priorities, assigning responsibilities, and committing to a resolution date.

Insure that changes made in a subsystem to correct a local problem are tested at the system level before being released?

Determine the effectivity of changes, including the question of when they will be put into new production, under what circumstances they will be installed in the field, what system configurations require their presence, and what change levels are required of other equipments in a system?

Insure that the economics of any change are considered when the effectivity of the change is specified? When the engineer signs the change order, does he know and take into account how many parts or assemblies on hand will have to be scrapped? Is the cost of reworking assemblies in process and in finished products in the field known?

Documentation Control Functions

Does everyone understand which part of the organization has control over and responsibility for documentation? Is there any evidence that uncontrolled documents are in use or have been used?

Is the "document release" function clearly defined, so that unreleased documents are not used? Is the release of a new product to manufacturing authorized at an appropriately high organizational level? Is it conditional on completion of product tests, and on correction of problems identified in those tests?

When documents are released, are they *immediately* distributed to pertinent parts of the organization? Are released documents accompanied by transmittal sheets, which list the drawing numbers of distributed documents and which are checked off, signed, and returned, thus helping insure that *all* changes are properly distributed?

Is there some procedure (eg, in data processing) by which the document-using organizations can periodically check that the various documents they are employing are the latest released by Engineering? Are there procedures within manufacturing, maintenance, and sales which cause these organizations to act immediately on the released documents? When a document describes a change, is it put into effect promptly—so that, for example, purchasing cancels orders for obsolete parts, maintenance prepares to make changes in equipment in the field, and sales revises brochures and manuals which must be modified?

In The Manufacturing Organization

Purchasing Function

When a product is released to manufacturing are there procedures which identify long-lead-time parts, and in-

sure that documentation for such parts is released suitably far in advance of other documentation?

When a document release identifies an engineering change, is its handling by purchasing appropriate to its effectivity? Does purchasing management have good visibility on the status of orders for parts and assemblies which are in the process of change? Eg, are unfilled orders for obsolete parts promptly canceled, and are the parts disposed of if cancellation is impossible? When a new part is to replace an old one at a specified effectivity point in manufacturing (starting with units of a given serial number), are orders for the old and new parts phased out and in properly? When specs for a purchased assembly have been changed, do the new specs get properly transmitted to the vendors, and are they formally incorporated into subsequent orders? If purchasing requires the vendor to make changes to his work in process (in the vendor's shop), is the effectivity of such changes clearly spelled out in purchase documentation, and is that documentation transmitted to receiving, so that incoming assemblies can be checked for compliance?

For certain critical parts or purchased assemblies, there may be an engineering-derived and controlled list of qualified vendors. Are there procedures which insure that purchasing notifies engineering when such vendors cease to supply that part or assembly, or fail to bid when purchasing is placing orders? When a previously qualified vendor supplies unsatisfactory goods, are there provisions to review and perhaps revoke his qualification?

Receiving Function

When parts or assemblies are received, does the purchase documentation make it clear what specs govern the purchase, and therefore what specs should be used to check the shipment?

Are the sampling algorithms, which determine what proportion of a shipment is checked or tested and what percentage of the sample must pass the tests, appropriate for the various classes of goods received?

Are the instructions which determine how the receiving department personnel inspect and test received goods—instructions specifying which dimensions should be measured, which properties should be tested, what functions should be tested, what instruments should be used, what measurement or test readings are acceptable—appropriate for each class of goods, and easily understood by receiving personnel? Are there provisions for modifying those instructions as a result of experience with the received goods and with vendors?

Is the measuring and test equipment used in receiving suitable for the tests and measurements which must be made? Is it accurate? Does it measure the proper things, or are its measurements readily interpreted to correspond to specified parameters? How is it calibrated or checked?

Assembly and Processing Functions

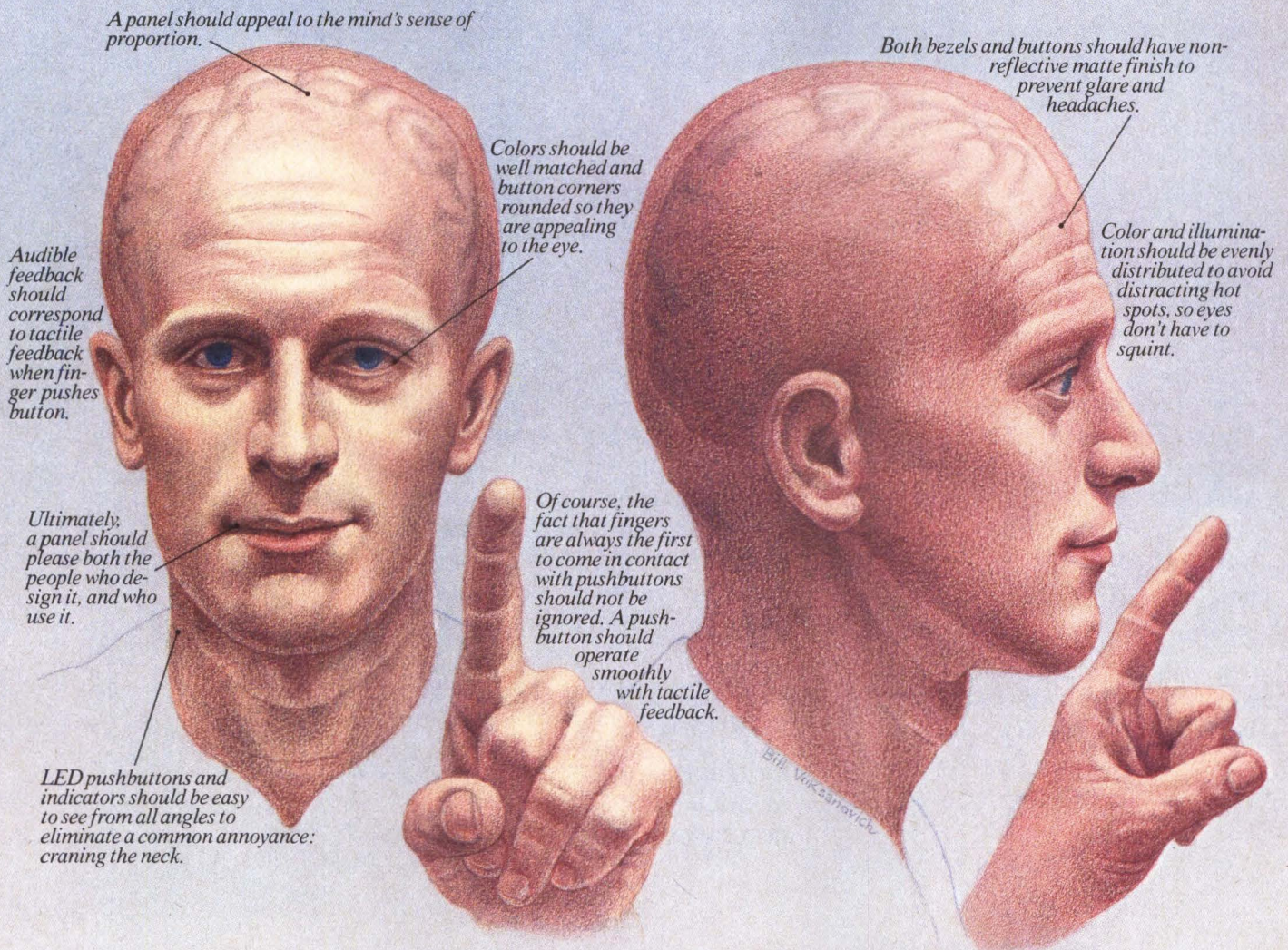
Are there procedures which insure that the assembly and process operations always employ the latest drawings?

Where in-process measurements and tests have been specified by engineering, are the test procedures and equipment used appropriate? Accurate? Calibrated?

Do the final unit tests check that the completed model meets all functional and performance specifications? Should system tests also be carried out, regularly or periodically, to insure that the unit works properly in a system? Do those final tests actually used agree with those specified in the released documentation?

When work in process in the factory is reworked in response to engineering changes, are there procedures which insure that the reworked units are also retested?

A pushbutton panel should be designed for parts of the body besides fingers.



When we designed the Advanced Manual Line (AML), we included everything a designer could want.

Like a broad selection of pushbuttons, indicators, paddles and rockers. In a variety of shapes, sizes and colors. With LED, incandescent or neon illumination.

But what really makes AML unique is a small detail that others seem to have overlooked.

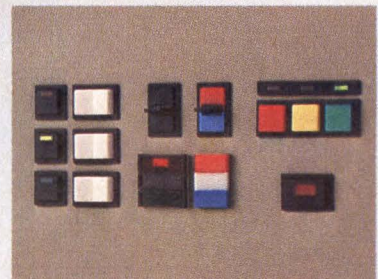
The people who use them. Which is why they're not only appealing to fingers, but other parts of the body as well.

That isn't to say we've neglected the person who puts the panel together. Because AML has single level termination for easy wiring and low installation cost. And electrical flexibility that ranges from solid state to electronic and power duty control.

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For details, and the location of our sales offices and distributors around the world, write MICRO SWITCH, Freeport, Illinois 61032. Or call 815-235-6600.

CIRCLE 28 FOR DATA



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When it comes to developing development systems that support more microprocessors, no one can touch us. Our universal development system doesn't box you in with a single chip or chip family. Our system sets you free to design with any or all of the most popular processors.

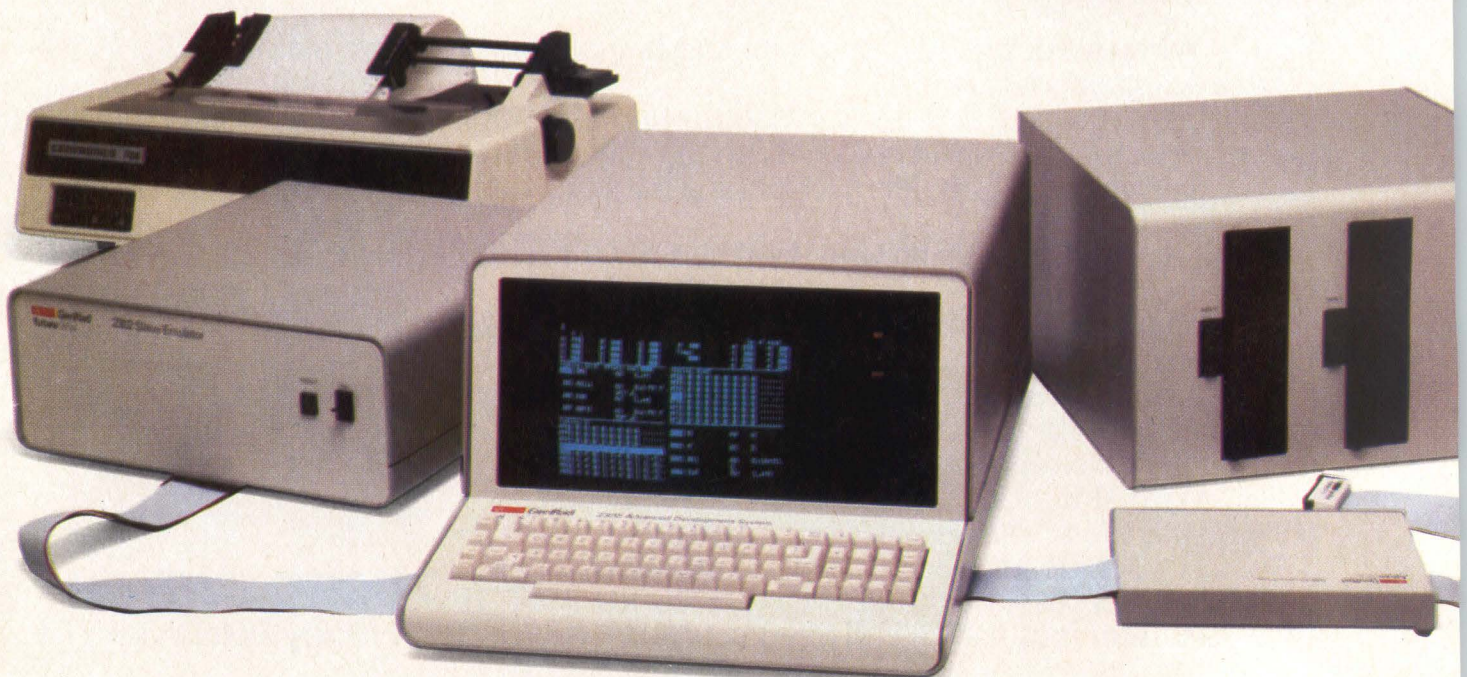
In your smart-product race through the '80's, switching development systems will be the pits. With our system that won't be necessary.

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Thanks to our unique slave emulation system we can add new chips to your system in a matter of weeks. Remember, we don't make the chips - just the development system. And we don't have to redesign our system for each new chip - we just add another slave emulator. And, that's all you pay for. So, we're faster and more economical, too.

WE SET THE PACE FOR EMULATION

Ours is the only system capable of delivering transparent, non-stop, full-speed emulation



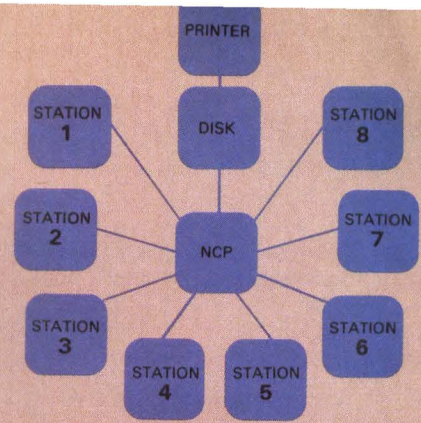
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systems

to 10 MHz. And it's the only system capable of emulating many different processors simultaneously.

Transparent, non-stop, full-speed emulation takes all the guesswork out of choosing the right microprocessor for your application. It allows you to evaluate each chip thoroughly, accurately and objectively.

The ability to emulate several different chips simultaneously paves the way to development of smart products using more than one processor.



2300 Series multi-station networks share disk and printer with up to eight stations. Each station is universal and may be ordered with the software and/or hardware capabilities required.

WE DELIVER THE MOST COST-EFFECTIVE SOLUTION

Lower initial cost, universality and expandability make our system a prudent, long-term investment. Any of our systems can be upgraded to network status. By sharing costly and under-utilized resources (disks, printers, emulators, analyzers and even software) you can stop paying your designers to stand in line. Networking can lower your cost-per-station by 20% or more.

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The 2302 Slave Emulator allows you to view your program in single-step, snapshot or logic analyzer modes. This view can be formatted to match your requirements even for the most complex memory segmentation, interrupt-driven or multi-processor environments.

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Our system has been designed to make hardware and software development fast, efficient and productive. With our high-speed CRT, high-level language programming and powerful software, things happen fast – sometimes instantaneously. Now available with highly block structured PASCAL compilers, our system can cut your programming time by 50% or more.

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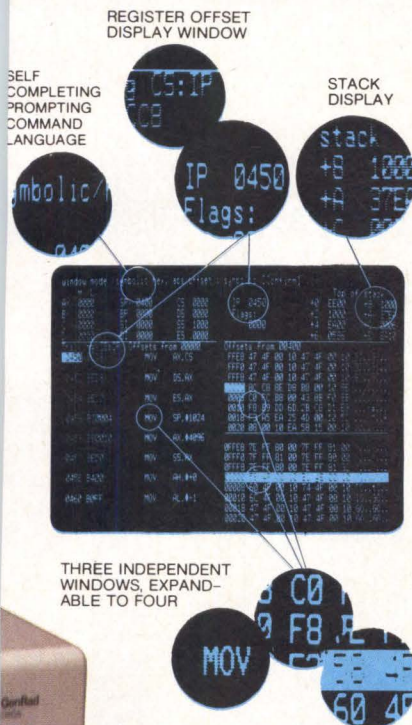
There is no finish in the smart-product race. To stay ahead you're going to need flexible, productive, expandable development systems and a supplier with staying power capable of giving you in-depth, after-sale service and support. Ask for a demonstration of the 2300 Series Advanced Development System. Sales and service offices in major cities.

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CIRCLE 29 ON INQUIRY CARD



THREE INDEPENDENT
WINDOWS, EXPAND-
ABLE TO FOUR

Shipping Functions

Are there procedures governing the way that equipment is packed for shipment to customers? Are the methods and materials used suitable for the equipment shipped and for the transport facility used? Eg, is equipment adequately protected from shock and vibration, and from temperature, pressure, and humidity changes, etc? If it must be disassembled for shipment, are the various pieces properly marked so reassembly is easy?

Repair and Refurbishing Functions

When a failed or replaced subassembly, unit, or system is returned from a customer site, are there procedures which govern its disposition? Under what circumstances is it scrapped? If it is to be refurbished or repaired, what determines the change-order level which applies—is it brought up to the latest set of released drawings, or to some earlier level? Is it subject to the same in-process and final tests as would apply to any *new* item coming from manufacturing?

In The Maintenance Organization

Are the training and reference manuals prepared by the maintenance organization consistent with engineering documentation for the various products? Are there procedures to revise this maintenance documentation when change orders are released by Engineering?

Are the training and reference manuals complete? Do they cover such things as equipment installation, unit and system test, preventive maintenance schedules and techniques, corrective maintenance diagnosis and repair, installation of engineering changes, equipment removal, and site configuration control?

Do the tests carried out by maintenance at the customer site, just before returning the equipment to the customer after a maintenance, installation, or change-order installation action, insure that the equipment still meets its functional and performance specifications?

In The Sales Organization

Are the reference, applications, and sales manuals and brochures prepared by the sales organization consistent with engineering documentation for the various products? Are there procedures which govern the revision of such documentation as applicable change orders are released by engineering?

Conclusion

By examining the product-related procedures which are actually in use, an organization can identify areas where those procedures are inappropriate or incomplete. Modifications to the defective procedures as revealed by this audit should help ensure the integrity of the manufactured product.



WIRE FOR WIRE-WRAPPING



CUT TO LENGTH AND PRE-STRIPPED ON BOTH ENDS

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1	30B-010	30W-010	30Y-010	\$4.88	28B-010	28W-010	28Y-010	\$5.25	26B-010	26W-010	26Y-010	\$5.75
1.5	30B-015	30W-015	30Y-015	5.19	28B-015	28W-015	28Y-015	5.63	26B-015	26W-015	26Y-015	6.23
2	30B-020	30W-020	30Y-020	5.50	28B-020	28W-020	28Y-020	6.00	26B-020	26W-020	26Y-020	6.68
2.5	30B-025	30W-025	30Y-025	5.82	28B-025	28W-025	28Y-025	6.38	26B-025	26W-025	26Y-025	7.13
3	30B-030	30W-030	30Y-030	6.13	28B-030	28W-030	28Y-030	6.75	26B-030	26W-030	26Y-030	7.60
3.5	30B-035	30W-035	30Y-035	6.44	28B-035	28W-035	28Y-035	7.13	26B-035	26W-035	26Y-035	8.05
4	30B-040	30W-040	30Y-040	6.75	28B-040	28W-040	28Y-040	7.50	26B-040	26W-040	26Y-040	8.50
4.5	30B-045	30W-045	30Y-045	7.07	28B-045	28W-045	28Y-045	7.87	26B-045	26W-045	26Y-045	8.98
5	30B-050	30W-050	30Y-050	7.38	28B-050	28W-050	28Y-050	8.25	26B-050	26W-050	26Y-050	9.43
6	30B-060	30W-060	30Y-060	8.00	28B-060	28W-060	28Y-060	9.00	26B-060	26W-060	26Y-060	10.35
7	30B-070	30W-070	30Y-070	8.63	28B-070	28W-070	28Y-070	9.75	26B-070	26W-070	26Y-070	11.25
8	30B-080	30W-080	30Y-080	9.25	28B-080	28W-080	28Y-080	10.50	26B-080	26W-080	26Y-080	12.18
9	30B-090	30W-090	30Y-090	9.88	28B-090	28W-090	28Y-090	11.25	26B-090	26W-090	26Y-090	13.55
10	30B-100	30W-100	30Y-100	10.50	28B-100	28W-100	28Y-100	12.00	26B-100	26W-100	26Y-100	14.00

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100 ft. roll	R30B-0100	R30W-0100	R30Y-0100	\$3.65	R28B-0100	R28W-0100	R28Y-0100	\$4.05	R26B-0100	R26W-0100	R26Y-0100	\$4.35
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1000 ft. roll	R30B-1000	R30W-1000	R30Y-1000	16.82	R28B-1000	R28W-1000	R28Y-1000	21.10	R26B-1000	R26W-1000	R26Y-1000	23.15

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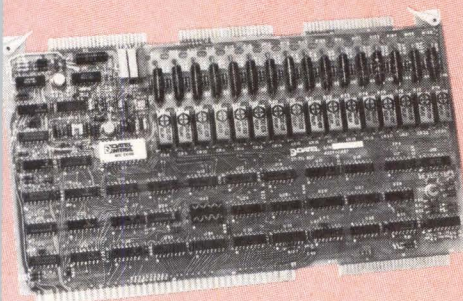
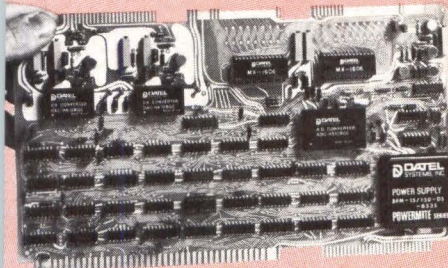
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ST-711 \$625 SINGLES
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- ▶ Model ST-711: 32S/16D A/D Channels, no D/A Channels..... \$625 (Singles)
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- ▶ Full mechanical, electrical, and pinout compatibility to Intel's SBC-711/732 Analog I/O Boards.
- ▶ Operates with all Multibus and SBC-Series compatible microcomputers including the 16-bit SBC-86/12 (except SBC-80/04).
- ▶ Works directly from Intel's RMX-80 Analog I/O Driver operating software.
- ▶ Includes program-gatable Pacer start clock, 1 mS to 1 sec., crystal-controlled.
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- ▶ Differential amplifier for high gain up to X1000 (10 mV full scale range).
- ▶ Includes Programmable Gain Amplifier.
- ▶ Includes Diagnostic Program tape for immediate TTY or CRT print-out.
- ▶ 12 bit binary conversion; 20 microsecond throughput period.

ST-711RLY8D \$683 SINGLES
ST-711RLY16D... \$1045 SINGLES

(ISOLATED)

- ▶ 8 or 16 differential A/D channels using a "Flying Capacitor" relay multiplexer for high common mode noise rejection (126 dB) and high isolation ($\pm 250V$ RMS).
- ▶ Complete hardware and software compatibility to Multibus and SBC-Series microcomputers. Uses identical programming and register assignments to SBC-711/732, and ST-711/732 A/D-D/A boards.
- ▶ 10 mV to 2V input ranges including Programmable Gain Amplifier. 12 binary bit A/D resolution.
- ▶ Includes Diagnostic Program for immediate TTY or CRT printout.
- ▶ Includes 10-stage Pacer Start Clock.
- ▶ ST-711RLY8D (8 Channels) \$683, singles
- ▶ ST-711RLY16D (16 Channels) \$1045, singles

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- ▶ 4 D/A Channels plus 4 4-20 mA current loop amplifiers.
- ▶ 12 binary bits, Multibus compatible.

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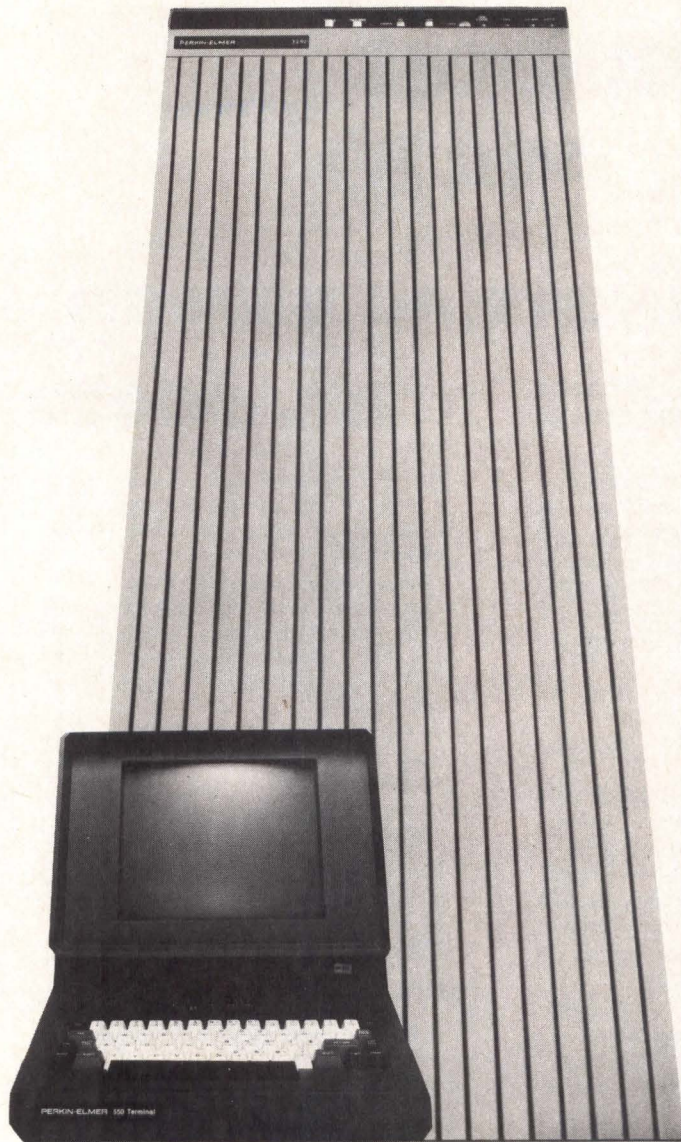
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the supermini solution to
your application
megaproblems.**

**The new 3240 ultra-high
performance supermini.***



**System prices start at \$125,500 (OEM quantity 1) which includes 512 KB of memory, writable control store, floating point processor, battery back-up, Model 550 console terminal, 80 MB disc, and 75 ips/800 cpi tape. Prices are U.S. only.*

PERKIN-ELMER

**I have massive
input/output
requirements.**

For tough jobs like simulation, the new 3240 delivers 40MB/second I/O bandwidth, four separate and independent DMA busses, 64MB/second peak system throughput rate, and multi-level interrupts. From 8 to 32 DMA ports can be configured on a 3240 system, each port capable of controlling up to 16 devices. This yields extensive on-line storage capability (up to 115 gigabytes worth) and throughput. Ask for details. Perkin-Elmer, 2 Crescent Place, Oceanport, NJ 07757

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Title _____

Company _____

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Please have a salesman call.

CIRCLE 32 ON INQUIRY CARD

CD 1

**I must have instantaneous
response.**

For high-performance transaction processing, such as an on-line reservation system, the power of the 3240 can be combined with RELIANCE, a software system that integrates COBOL, data management, and transaction processing software. Even with a 128-terminal system, you get instantaneous terminal response. And your data base is protected from media faults and system failures. Add to this Perkin-Elmer's industry-compatible RPG II. Ask for details. Perkin-Elmer, 2 Crescent Place, Oceanport, NJ 07757.

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CIRCLE 38 ON INQUIRY CARD

CD 1

My applications need big memory space.

For scientific research, such as seismic exploration, the 3240 offers 16MB of directly addressable MOS memory with our unique hierarchical storage scheme for fast access. By linking as many as eight Model 3240s to Perkin-Elmer's industry-pioneering shared memory system, total memory space can be increased dramatically. A fully expanded shared memory system accommodates both processors and peripherals. Ask for details. Perkin-Elmer, 2 Crescent Place, Oceanport, NJ 07757

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CD 1

I don't want to spend a fortune on software.

No one does in any application. You start with Perkin-Elmer's highly efficient operating system that's evolved from use in more than 2500 of our 32-bit computer installations worldwide. Add our Multi-Terminal Monitor and you can have 32 programmers doing concurrent development work in any mix of our high-level languages—ANSI-standard COBOL, FORTRAN VII (with its separate development and globally optimizing compilers), and RPG II. Combine this with our comprehensive telecommunications software that supports a wide variety of data communications protocols and work-station emulators. Perkin-Elmer, 2 Crescent Place, Oceanport, NJ 07757

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Title _____
Company _____
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Please have a salesman call.

CIRCLE 36 ON INQUIRY CARD

CD 1

I'm trying to solve complex problems no one has attempted before.

When applied to problems such as command and control or computer-aided design applications, the 3240 system really pays off. You benefit from our user-alterable writable control store (another pioneering effort from us), which enables you to tailor your programs with microcode to suit your application needs. And there's more. You benefit from our separate FORTRAN VII globally optimizing compiler by getting assembly language execution speeds with the efficiency of high-level programming. Perkin-Elmer, 2 Crescent Place, Oceanport, NJ 07757

Name _____ Tel. _____
Title _____
Company _____
Street _____
City _____ State _____ Zip _____

Please have a salesman call.

CIRCLE 40 ON INQUIRY CARD

CD 1

I need exceptional accuracy.

In such accuracy-critical applications as satellite or missile tracking, the 3240, with full 32-bit architecture, features a single- and double-precision Floating Point Processor with accuracy unsurpassed in the minicomputer industry. The accuracy of the 3240 hardware is also complemented by a state-of-the-art Math Function Library that is part of our industry-leading FORTRAN VII. Ask for details. Perkin-Elmer, 2 Crescent Place, Oceanport, NJ 07757

Name _____ Tel. _____
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Company _____
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City _____ State _____ Zip _____

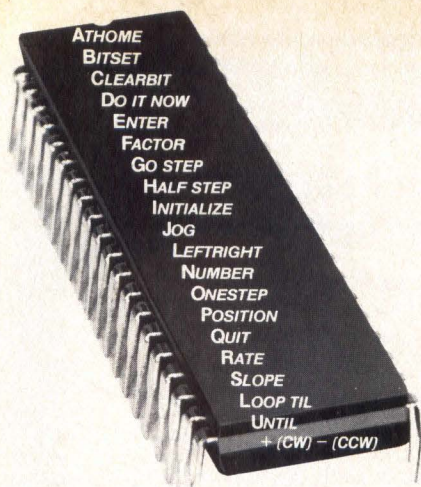
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CIRCLE 42 ON INQUIRY CARD

CD 1

OR CALL 800-631-2154

In New Jersey (201) 229-6800



Tell it and forget it...

... the new CY500 stored program stepper motor controller runs its own program, freeing your host computer for other jobs.

No more one-pulse, one-step operation requiring your host computer to tie itself down to a stepper motor. Now Cybernetic Micro Systems brings you a function-oriented stored program stepper motor controller that allows the user, or host computer, to program it and forget it...

The CY500 executes 22 hi-level instructions, either in command mode or as a sequence of internally-stored commands, using single byte code such as 'P' for position, 'R' for rate, and 'S' for slope. Parameter values can be expressed in ASCII-decimal for keyboard programming or binary code from the host computer. Parallel or serial communication.

The stored program capability allows the use of 'DO-WHILE' program looping and 'WAIT-UNTIL' operation. Ten different operational modes allow absolute or relative positioning, full- or half-step operation, hardware or software control of direction, start/stop, ... and many more.

Numerous input and output control lines allow synchronizing the CY500 with external events or devices and allow each step to be triggered. Stepping at rates up to 3500 steps/sec, the CY500 also provides ramp-up, slew, and ramp-down operation, all under software control. Two interrupt lines request the host's attention if needed.

This +5 volt N-MOS TTL-compatible controller is available from stock, today, for only \$95.00. Contact Cybernetic Micro Systems. We want to see you program your stepper motor and then ... forget it.



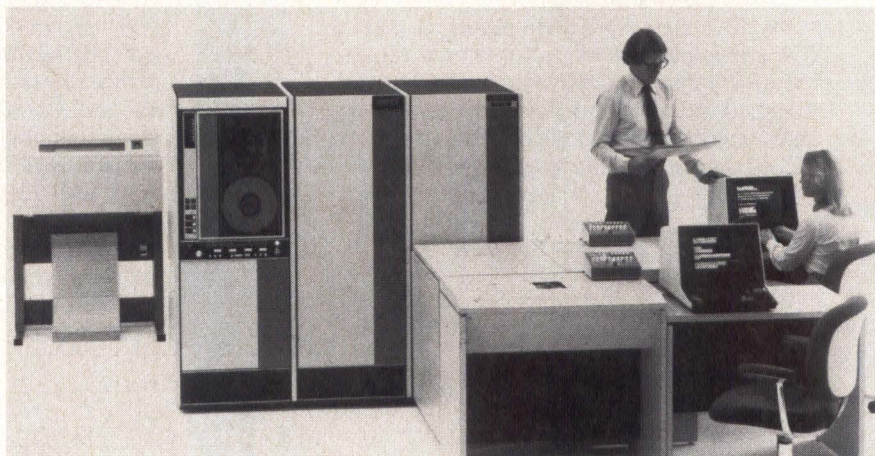
Cybernetic Micro Systems
445-203 South San Antonio Road
Los Altos, California 94022
(415) 949-0666

(Use your MASTER CHARGE or VISA charge card)

CIRCLE 33 ON INQUIRY CARD

DIGITAL TECHNOLOGY REVIEW

LSI Test System Exercises 30-Pin Chips at 20-MHz Rate



Sentry series 20 from Fairchild's Test Systems Group tests high speed 60-pin LSI devices at 20 MHz and offers 5-ns strobe width to allow accurate characterization and timing comparisons

A 20-MHz general purpose LSI test system, the Sentry[®] series 20 fully exercises high speed devices such as microprocessors, associated support chips, logic arrays, and bipolar and mos memories. The system, developed by Fairchild Camera and Instrument Corp, Test Systems Group, 1725 Technology Dr, San Jose, CA 95110, can test LSI devices at 20 MHz for 60-pin devices and at a 40-MHz rate with 30-pin chips. Introduced as the high speed member of the series, the unit meets needs for a test system that provides accurate characterization of device timing parameters.

The machine's 5-ns strobe width affords increased ability in determining device margins, and offers accuracy for characterization and timing comparisons. Sixteen mask and functional invert registers shorten test times and increase flexibility in testing device parameters by providing more efficient use of the test system's local memory.

I/O mode 8 simplifies programming by controlling eight I/O pins from one pin, permitting byte-oriented bus operations to be performed in one cycle instead of eight. 5-ns test rate resolution allows users to set up timing for minimum cycle time device testing of fast devices.

The ability to program tests in different I/O states is provided through 16 I/O registers. Sixteen timing gen-

erators, each with 16 timing values, provide up to 32 independent edges with 160-ps resolution for accurate placement of clocks, permitting better device characterization and quality control.

Configured with a maximum of two 60-pin test heads, the system has three bays including an FSR-2 controlling computer, test measurement system, and high speed test controller. Standard peripherals are a line printer, video keyboard terminal, and magnetic tape unit. Controlling computer is a 24-bit general purpose CPU with 96k memory that expands to 196k bytes. The high speed tester has 4k of local memory, a 20-MHz sequence processor, and a 20-MHz pattern processor. 100k ECL devices are used in critical paths and pipeline sections throughout the system to provide the speed necessary. An 18M-byte fixed head disc unit with 8-ms access time offers the throughput necessary to shorten test times.

M³ operating software is compatible with the family's existing operating and testing languages, yet enhances the ability to write software packages by improving multitasking and use of foreground and background operations. Software compatibility provides access to the large library of existing utility programs available for use with other members of the series.

Circle 175 on Inquiry Card

The OEM Tape Transport For The 80's.

Now, Datum innovation brings you the next generation in mini-computer magnetic tape transports, the D-451. A transport that thinks for itself thanks to Datum's smart new single-board microprocessor.

Self diagnostics, a reduced electronic component count and hybrid chip read amplifiers are examples of Datum's entirely new microprocessor design architecture.

You won't need an external test box with the D-451. Fault-isolation, and skew verify alignment are among internal microprocessor controlled self-test diagnostics.

An embedded Dual/Density formatter controls up to four tape transports.

Every aspect of the intelligent D-451's design and engineering makes its contribution in superior performance

and reliability when reading and writing IBM/ANSI-compatible, 1/2" magnetic tape. Featured are: 7-or 9-track, NRZI and PE formats; dual format is standard for 9-track. Phase Encoded density is 1600 BPI, while densities of 800, 556 and 200 BPI are available for NRZI.

And Datum's painstaking research provides the D-451 with IBM tape-path geometry, ceramic blade tape cleaners, photoelectric write ring detection, low-inertia capstan drive and digital write deskew control.

Find out more about the reel thing, the tape transport that thinks for itself. Call or write your local Datum representative or Datum Inc., 1363 South State College Boulevard, Anaheim, California 92806. (714) 533-6333.



**AVAILABLE
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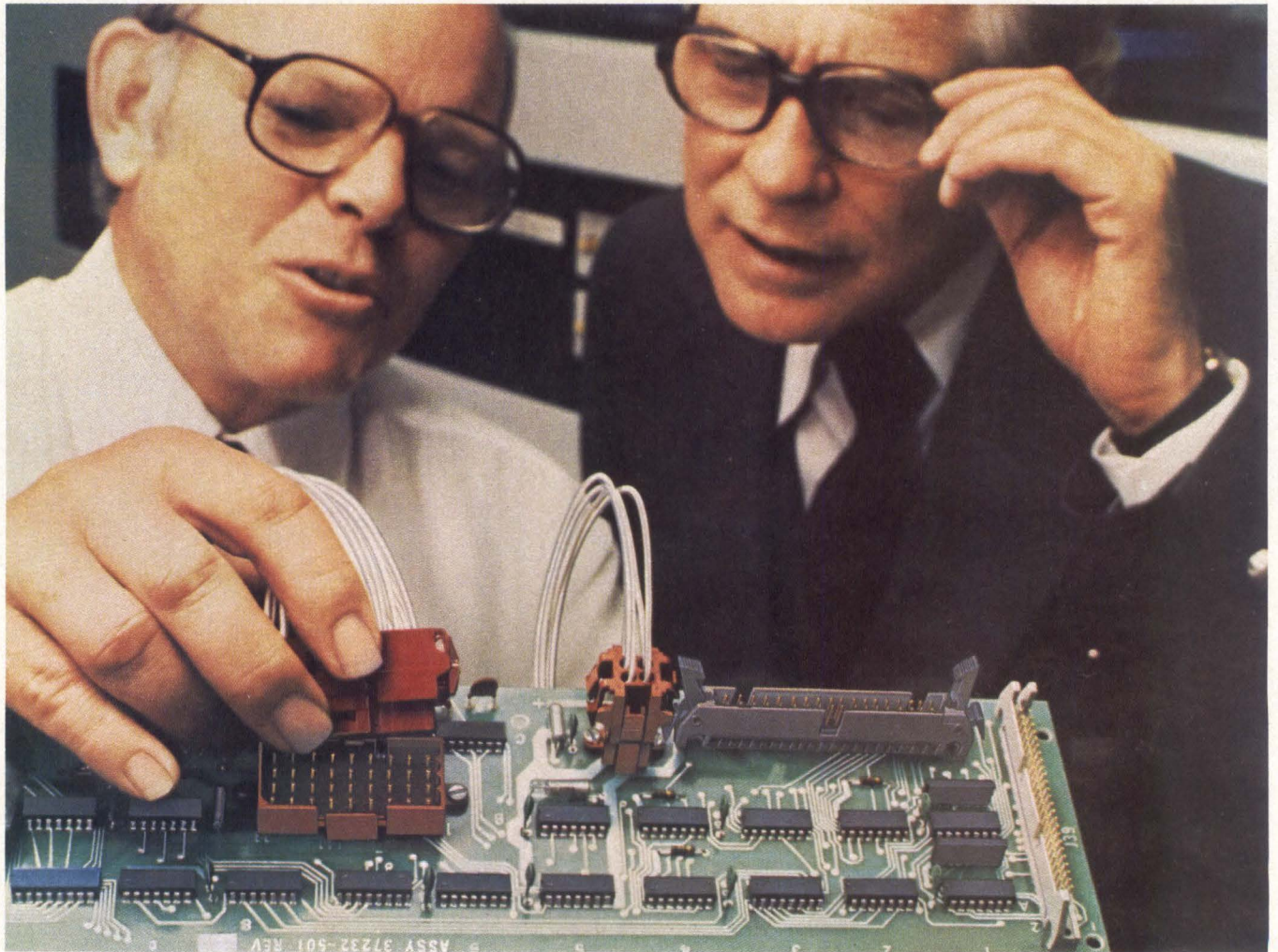
CORPORATE HEADQUARTERS 1363 S. State College Blvd., Anaheim, CA 92806, Tel: 714/533-6333, TWX: 910/592-1289, Telex: 68-5579 • **EUROPEAN HEADQUARTERS, DATUM (ELECTRONICS) LTD.**, DATUM House, Harlington, Middlesex, England, Tel: 01-897-0456, Telex: 935-398 • **DATUM SALES OFFICES, CANADA**, Willowdale, Ontario, Tel: 416/491-6960, Telex: 06-966857 EOR TOR; **MOUNTAIN STATES**, Denver, Colorado 80232, Tel: 303/693-3414; **EAST COAST**, Mountainside, New Jersey 07092, Tel: 201/654-5590; **MIDWEST**, Des Plaines, Illinois 60018, Tel: 312/296-1064; **SAN JOSE**, San Jose, CA 95117, Tel: 408/249-5370; **NEW ENGLAND**, Framingham, MA 01701, Tel: 617/872-6911.

PPD105R

CIRCLE 35 ON INQUIRY CARD



"I need a cost-saving connector I can apply simply, anywhere in the world. And that's a perfect description of the AMP Metrimate line."



Metrimate is our internationally accepted rack and panel connector. Internationally accepted because no matter what standard of approvals you go by—UL, CSA, or VDE, Metrimate meets or exceeds them all.

Internationally accepted because Metrimate housings and contact spacings are designed to true metric dimensions.

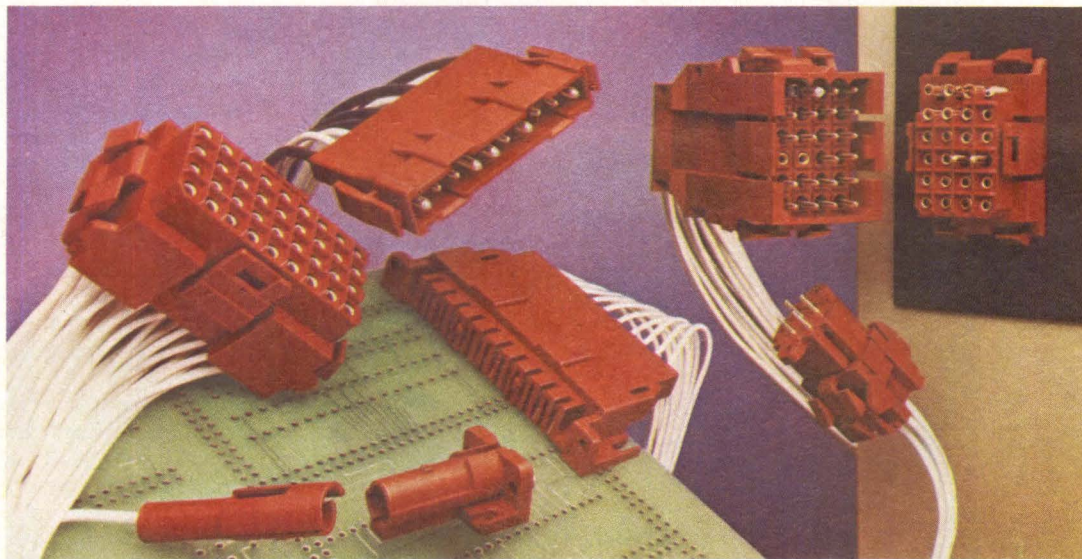
And, because AMP can supply these connectors to you anywhere in the world, along with the technical service and support to back them up.

But the first description—"a cost-saving connector you can apply simply"—really tells the whole story. Because every time you use a Metrimate connector, it saves you money. With

features like low cost thermoplastic housings, shield accessories, strain reliefs, and the elimination of mounting hardware. And the incredible variety of automatic contact application equipment available to you. Now, with the addition of a new commoning power distribution header, Metrimate is cost effective in an even wider variety of applications.

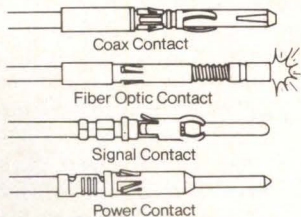
Of course, descriptions only go so far. It's the application that counts. So to find out how you can start saving money with the connectors you can apply anywhere, call or write us for more information.

AMP has a better way.



Some facts worth knowing about AMP Metrimate Connectors

Description: Part of AMP's exclusive Multimate Family that accommodates common contacts in a variety of connector housing styles and saves on both tooling and inventory costs.



Voltage rating: 380 VAC, 450 VDC (VDE), 600 VAC (UL); 250 VAC (CSA).

Dielectric strength: 1500 volts rms at sea level.

Temperature: -55°C to $+105^{\circ}\text{C}$.

Current rating: Signal and Power Contacts; 13A max. per contact (limited only by connector block working temperature).

Insulation resistance: 5000 megohms, min.

Contact resistance: 5.5 milliohms, max.

Durability: 250 cycles, tin-plated contacts, 550 cycles, gold-plated contacts.

Where to telephone: Call the Metrimate Information Desk (717) 780-8400.

Where to write: AMP Incorporated, Harrisburg, PA 17105.

AMP is a trademark of AMP Incorporated.

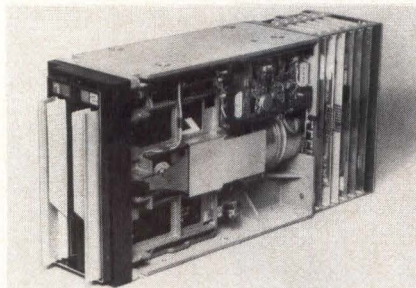
AMP

CIRCLE 37 ON INQUIRY CARD

Dual Diskette Drive Stores 6M Bytes With 158-ms Access

Using two 8" (20.3-cm) flexible discs, the MD 122 stores 3M bytes of formatted data on each to offer 6M-bytes total capacity. The unit, developed by Burroughs Corp, OEM Div, PO Box 1226, Plainfield, NJ 07061, incorporates a microprocessor controller that performs many functions normally required of the host system controller or host CPU. Occupying slightly more space than a conventional floppy drive, the unit offers five times the capacity, permitting designers to streamline or expand their systems.

The system achieves an average access time of 158 ms by sharing a high performance voice coil actuator between the two discs. A combination of fast access, high storage capacity, and dual removable media permits the system to serve either as a main file unit or as a load/dump device for fixed disc drives.



Storing 6M bytes of data on two 8" flexible discs, Burrough's MD 122 off-loads host using built-in microprocessor controller to handle data channel and positioner functions

Among the functions performed by the built-in controller are CRC generation; error detect, retry, and correct; sector relation; file search using host supplied parameters; and dual sector buffers. This also handles media wear monitoring and warning, error logging, and analysis, and confidence and diagnostic tests. In addition, the controller is used to control basic positioning and data channel functions within the soft sectored device.

Within the drive, two discs are mounted on a common spindle and

are rotated by a single motor. Four heads, mounted on a common assembly, are moved across the surface of the discs by a voice coil actuator. Seek positioning is handled by a photoelectric position grating system. To maintain position accuracy at 150 tracks/in (59/cm), alignment tracks are located on each disc for the microprocessor to use in periodically realigning the positioner.

The device records 256 data bytes/sector at a density of 7100 bits/in (2795/cm) using MFM recording mode. Seek time is specified as 100 ms average, 200 ms maximum (including settling time). Latency is given as 57.25 ms average, 114.50 ms maximum. Transfer rate is 1M bits/s at 524 r/min. Data error rate is said to be 1 in 10^{11} bits maximum.

A unique outer sleeve protects the media from damage. The unit is designed so that the discs can only be inserted and removed with the outer sleeve in place. A mechanism in the drive ensures that when a disc is inserted, it is fully home and latched before the outer sleeve can be removed.

The drives are designed to be incorporated in host system cabinetry with host supplied dc voltages. They provide interface compatibility with the RD210 series of fixed disc drives. Circle 176 on Inquiry Card

Logic Simulation System Uses Multiple Algorithms To Generate ATE Programs

A logic simulation system that combines proprietary test generation methodology with other advanced techniques not previously available on commercial units, the CAPABLE[®] 4814 offers automatic test program generation at one-third the cost of other systems. To provide this capability, Computer Automation Inc, Industrial Products Div, 2181 Dupont Dr, Irvine, CA 92713 has equipped the CPU with 320k bytes of semiconductor memory, alphanumeric CRT terminal, 256k-byte floppy disc drive, and 10M-byte dual moving head disc drive. MONTOS[™] operating software, ATG II,

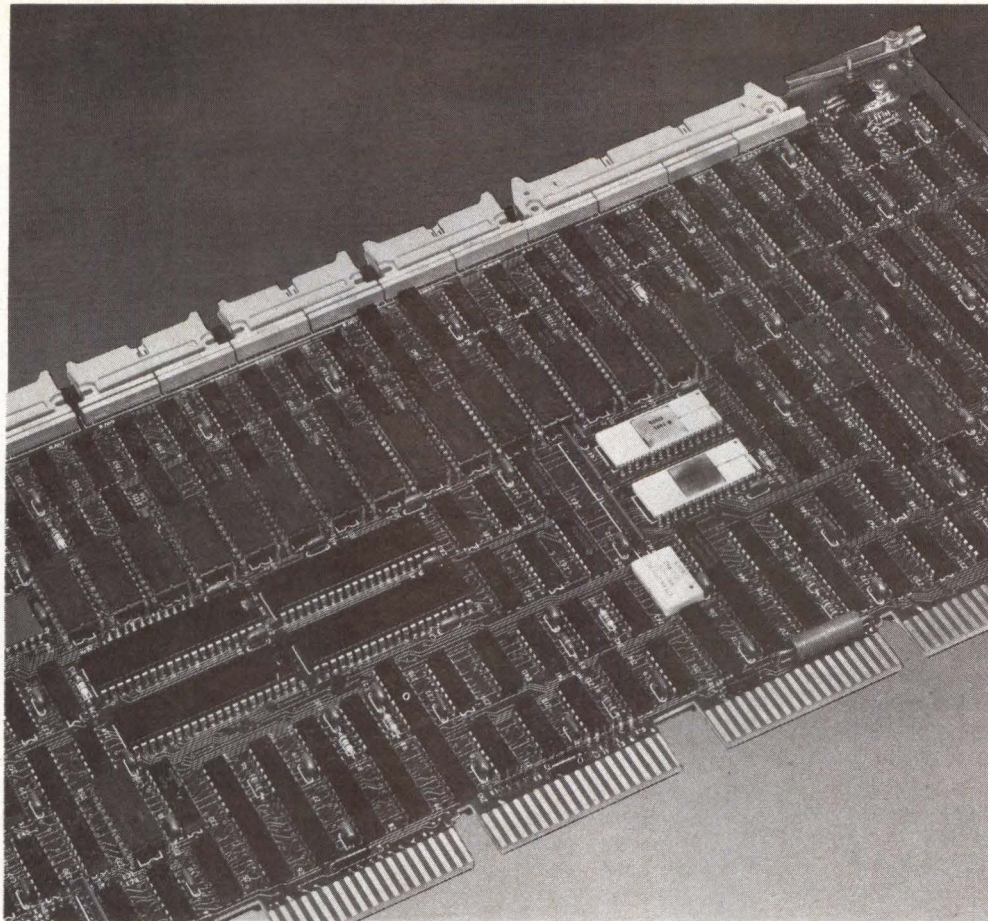
functional emulation and DES logic simulation packages are also provided along with associated libraries.

Automatic text generation uses a computer program to analyze a software model of a complex circuit board, calculates a list of conditions in which the device may be failure prone, and then generates programs to test for these faults. ATG II algorithms used overcome drawbacks of previous algorithms, permitting the system to be assigned to search for circuit faults in a computerized model and then be left to carry out the assignment without additional inputs. The system will continually analyze sections of the model in increasing detail to uncover a greater percentage of faults than previously possible.

Testing methodology of the 4814 incorporates two proprietary advances. Previous automatic test pattern generation programs have used a single algorithm to select a fault pattern from a table of undetected faults, and then determined the propagation path, calculated the stimulus for that path, and generated the stimulus to drive the fault out using the same algorithm. ATG II, however, switches among four highly refined algorithms automatically to provide maximum fault detection. Computer time is optimized by having the system work on easy faults first and then proceed to more difficult areas.

The second advance is contained in the system's optional library. While previous ATG logic propagated faults in the forward direction only, the ATG II library contains entries that describe both forward and reverse fault propagation through electronic parts. This enables intelligent selection and synthesis of the most efficient path for the fault to be propagated out for detection. The system can then actually drive the fault along this path for identification.

In addition to ability to generate test programs, the package contains functional emulation and logic simulation capabilities for use during design, prototype, or production. Guided fault isolation and automatic fault isolation diagnostics provide effective diagnosis of faulty logic boards. Various listings can be produced during the ATG process to serve in fault detection analysis and internal state timing analysis. Circle 177 on Inquiry Card



ONE-BOARD PDP-11 SMD CONTROLLER, SOFTWARE COMPATIBLE...A FIRST!

Dataram's S33 interfaces Digital Equipment Corporation's (DEC®'s) PDP-11 series to a wide selection of SMD (storage module drive) and Winchester type disk drives. The S33 emulates DEC's RM02 and is fully software compatible with RM02 diagnostics and RM02-supporting operating systems. Up to four drives per S33 controller, almost 300 MB of disk storage. The microprocessor-based S33 controller has 2 KB of data buffering, multiple sector transfers, and built-in self-test capability. And media compatibility with DEC's RM02 drive. All this and amazingly packaged on one DEC hex board...the only controller to make this claim!

One-board means you need only one hex SPC slot. One-board means easy insertion and optimum air flow.

One-board with its attendant features of minimized interconnections and low component count means lower power, complete accessibility, higher reliability...and best of all, lower cost.

If you're interested in one of our one-board S33 controllers, or a whole bunch of them, we'd like to hear from you. If you operate in the LSI-11® world, still contact us. Our LSI-11 cousin of the S33 is on the way.

DEC, LSI-11 and PDP are registered trademarks of Digital Equipment Corporation



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CIRCLE 39 ON INQUIRY CARD

Portable Data System Aimed at Aiding Distribution Industry

Remote processing capabilities of the 101XL terminal are combined with a remote portable printing device in the Route Commander™ data system, providing an integrated approach to portable data processing in almost any environment. Developed by Norand Corp, 550 Second St se, Cedar Rapids, IA 52401, the system offers continuous adjustment of inventory and printout of receipts as well as facilities for transmitting to a main-frame computer through adapter and standard telephone lines.

A basic configuration consists of a 101XL portable data collection terminal, 16k data memory, 26-col printer, and battery charger for overnight recharging. Optional equipment includes 32k memory, auxiliary battery pack, a charger that works from an automobile cigarette lighter, and 2-way telecommunications. Units operate from a 24-Vdc lead cell with integrated batteries. The system is offered in an attache case package or for mounting in the cab of a van or truck.

The terminal incorporates an 8-bit parallel processing microprocessor and provides a 12-character position alphanumeric display using a 64-character set. Input is through the unit's keyboard, which provides 20 keys in a 4 x 5 layout. Communications occur through a 202 compatible 1200-baud modem that provides transmit only (simplex) with reverse channel error corrective capability, or transmit/receive (half-duplex) capability.

System printer offers 2.4-line/s output using a serial dot matrix impact mechanism. This unit has a 7-line/s paper feed speed and provides 26-char/line normal print or 13-char/line in bold print. The optional van mount printer supplies 40 columns of full alphanumeric data and prints a dot matrix format at 3 lines/s. This unit mounts securely inside a delivery van and takes power from the vehicle's battery.

Contained in a case measuring 15.5 x 14.75 x 5.5" (39.4 x 37.5 x 13.9 cm), the system records and adjusts inventory as it is loaded. It computes prices, extends and totals for quantity purchases, prints a multicopy receipt



Norand's Route Commander combines data collection terminal, data storage capacity, and printer with processing and telecommunications capabilities in portable unit to extend benefits of computer data processing into distribution industry

as well as daily cash reconciliation and sales reports, and can transmit daily information reports to a central computer and receive updates during the telecommunications process. Priced at \$2695, the unit promises

to pay for itself over a 7-month period through elimination of computational errors, overages, and shortages; and through increased productivity of personnel.

Circle 178 on Inquiry Card

Memory Board/System Tester Offers 10-MHz Rate, 24-Bit Addressing

The 10-MHz MD-207/11 is optimized for dynamic testing of memory boards and complete memory systems. Capable of 24-bit addressing and 144-bit algorithmic data I/O, the system can test semiconductor, core, plated wire, and bubble memory technologies in production or engineering environments.

Hardware components making up the system, from Macrodata Corp, PO Box 1900, Woodland Hills, CA 91365, include the Digital Equipment Corp LSI-11, dual-floppy disc drive, and vt-100 video keyboard for full computer control. The system features a programmable split cycle clock generator with up to 16 independently programmable phases to accommodate the increasingly com-

plex testing relationships of synchronous and asynchronous semiconductor memory systems.

The 10-MHz test system has a variety of user oriented software packages for performing engineering operations such as automatic shmoo plotting, data logging, and statistical analysis. Production oriented packages include automatic board diagnostics and realtime error logging, management summaries, and a prompting menu for use by production test system operators. A 10-MHz data buffer memory option allows truth table pattern storage.

Interfacing to board or system through the company's logic link, the -207/11 can be remote sited or used for burn-in oven testing. The unit retains compatibility with its predecessor while providing more capability at a price of \$78,500.

Circle 179 on Inquiry Card

Black/White and Color Display Terminals/Printers Offer User Setup

A Teletype compatible modular display terminal and printer and a color display station and printer communicate with System/370, 4300, and 8100 processors as well as the Series/1. Announced by IBM Corp, Data Processing Div, 1133 Westchester Ave, White Plains, NY 10604, the modular units are designed so that users can put them into operation.

The low cost 3101 display terminal includes 12" (30.5-cm) CRT screen that displays 1920 characters on 24 lines, logic unit on which the screen rests, and a separate 87-key keyboard. The unit's low profile and compact dimensions adapt it for use in space limited areas. Built-in diagnostic capability aids in identifying and resolving problems. Display screen, logic unit, or keyboard can be replaced without aid from service representatives.

Attaching to the terminal, the 3102 printer provides a copy of information displayed on the screen. The printer, like the terminal, contains self-diagnostic functions.

Shipments of the terminal are scheduled to begin fourth quarter 1979; printer deliveries will begin in second quarter 1980. Terminal prices range from \$1295 to \$1520 in quantities up to 24, depending on transmission mode selected. Purchase price of the 3102 printer is \$1295 each in the same quantity.

Capable of transforming existing data to 4-color alphanumerics, and displaying up to seven colors as well as graphics on its 14" (36-cm) screen, the 3279 color display station simplifies complex data and speeds comprehension for operators. Two models of the unit display alphanumeric data in four colors with either 1920 characters on 24 lines or 2560 characters on 32 lines. Two models offer 7-color displays with the same number of characters, adding pink, yellow, and turquoise to the red, green, blue, and white of the 4-color models.

To maintain a sharp image, the color display unit uses very small dots to form full size characters and patterns. A 3-electron-beam-gun system activates red, green, and blue emitting phosphor dots in the CRT. The unit also contains an advanced color convergence system to ensure

color definition. Using the keyboard, an operator can align colors across the screen at different points provided by a test pattern.

A bidirectional wire matrix printer, the 3287 printer uses a 4-color cartridge ribbon. Attaching to 3274 or 3276 control unit, the printer has the same functions as existing 3287 printers. Two models provide speeds of up to 80 and 120 char/s.

The 10 x 8 matrix cell has all locations available for printing, allowing continuous horizontal and vertical lines to be printed. Operators can control color on a dot basis, as well as by character, permitting multi-colored symbols and graphics to be designed.

Prices for the 3279 color display terminal with keyboard range from \$4300 to \$6700 depending on screen capacity, colors, and graphic display options. The color printer sells for \$6125 or \$6500 depending on speed. First shipments are scheduled to begin in second quarter 1980.

Circle 180 on Inquiry Card

Test Systems Meet Special Requirements of Magnetic Bubble Memory

Computer controlled test systems capable of handling the specific requirements of testing magnetic bubble memory devices, ADATE 1450 and 1475 provide high volume production test capability. Watkins-Johnson Co, 3333 Hillview Ave, Palo Alto, CA 94304, developed the machines with the capacity and drive requirements necessary to test the devices.

A dedicated system controller contains realtime electronics for minimizing test times and allows alteration of text patterns while still operating at maximum device data rates. Software controlled function drivers and detectors provide automatic operation for testing all currently available device architectures up to 65M bits maximum capacity.

Inherent in the Pascal based software are the advantages of a high level language as well as simplified implementation of algorithmic procedures necessary for testing magnetic bubble devices. In addition,

test patterns are also specified at a high level rather than in assembly language. These features allow the user to generate test patterns in a minimum of time.

Test generation software creates device independent test programs that allow magnetic bubble memory architectures to be tested using existing test programs. Thus a new program need not be written each time a new architecture is tested.

The ADATE 1475 offers standalone test capability while ADATE 1450, an enhanced version, provides ease of program development. Options available for both systems include wafer probe interfaces, parallel test capability, and networking of test systems.

Circle 181 on Inquiry Card

Electroluminescent Lamps Backlight Flexible Membrane Keyboards

A technique developed for backlighting flexible membrane keyboards capitalizes on the space saving attributes of the thin keyboards which have been previously compromised by the use of bulky, heat producing incandescent lighting components. Electroluminescent CAPSUL lamps, produced by Luminescent Systems, Inc, Lebanon, NH 03766, operate at low power levels to provide a uniform cold light source in a thin profile package.

The 0.032" (0.813-mm) profile of the electroluminescent lamps makes high density packaging possible and greatly reduces the amount of space required. In some applications total thickness of an entire lighted keyboard assembly is approximately 0.150" (3.81 mm). The cold light source lamps operate at low power levels, generate no hot spots, and add no heat to the assembly.

Operating from -55 to 40 °C, the useful life of the standard lamp exceeds several thousand hours. Long-life lamps extend this five to ten times. A variety of colors are available, with two or more colors possible on a single lamp. All lamps are free from radiation and emit no radioactive or electromagnetic interference.

Circle 182 on Inquiry Card

Multiport Memory Option Extends System Throughput To 11M Bytes/s

MA780, a multiport memory subsystem, permits as many as four VAX systems to use 4M bytes of shared memory in addition to each system's local memory complement. The op-

tion was designed by Digital Equipment Corp., Maynard, MA 01754, to extend the performance and uptime characteristics of VAX-11/780 series computers.

Containing 256k bytes of ECC MOS memory, expandable to 2M bytes, the multiport memory subsystem can be shared by from two to four 11/780

systems. Each CPU will accommodate two memory subsystems. A single CPU with its maximum 8M bytes of local memory can therefore access 12M bytes of directly addressable memory. Enhancements resulting from the ability to share data among several systems and to perform inter-processor communications at memory speeds provide the performance and uptime necessary for high throughput applications in simulation, power monitoring, and acquisition and analysis of data from high data rate devices.

Each port of the memory subsystem has a buffer for commands and data. The controller services these ports in order of request for access, bypassing inactive ports. These factors, plus ability to pass interrupt commands directly between any two ports, supply total throughput of up to 11M bytes/s. Integrity of data is ensured since the unit maintains parity and error checks on all internal buses and continually updates data within the CPUs' caches.

Interprocessor communications through the unit is supported by extensions to the VAX/VMS operating system. Sharing of data regions is achieved by extending the VMS facility for global sections to shared memory and by allowing placement of VMS mailboxes—record oriented virtual devices for interprocess communication that accommodate messages up to 64k bytes long. Use of common event flags provides a simple fast mechanism for synchronization of one process with others. An interlock protects a shared memory location from simultaneous update attempts.

Sufficient isolation between VAX systems is provided to prevent a failure in one system from having much effect on the total configuration. The unit's features enable separate power down of a port and its associated CPU. Extensive diagnostic routines allow online testing of the subsystem from a single port; the unit also generates interrupts to notify ports of power failures and error conditions as soon as they are detected.

The subsystem with controller, 256k bytes of ECC MOS memory, two port interfaces, cabling, and power supply is priced at \$34,900. Deliveries are planned to begin in midyear. A second subsystem, mounting in the same cabinet as the first, will cost \$30,000. The unit can be field installed on existing systems.

Circle 183 on Inquiry Card

Small DC Motors a new series from Canon

A new line of small, permanent magnet and brushless d.c. motors for rated loads ranging from 6 to 75 g-cm and speeds to 8300 rpm for voltages from 1.8 to 24 is now available from Canon. This line includes both governed and ungoverned models and units incorporating an a.c. tachometer. Most can be fitted with Canon gearheads which offer speed reductions up to 3000 to 1.

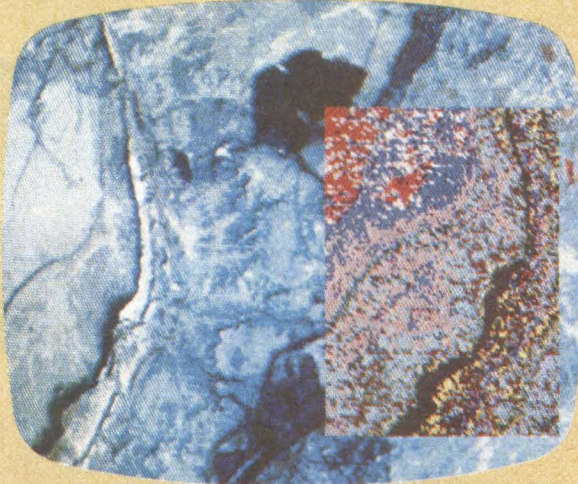
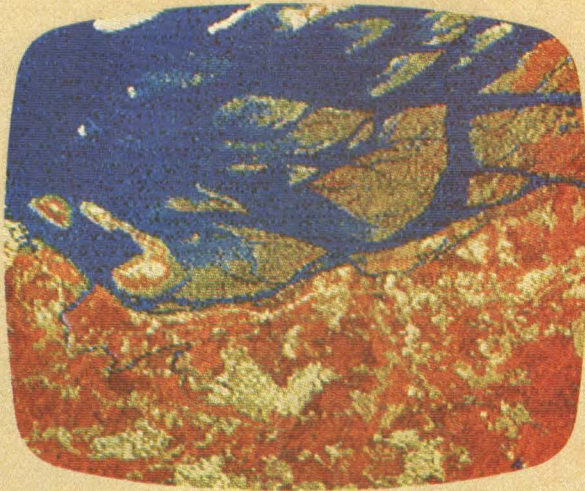
If you are an OEM presently using such motors or designing equipment in which they are incorporated you are invited to call Phil Spector at 516-488-6700 or to send for a free set of individual data sheets which contain detailed specs and performance curves. (Canon's d.c. motor line also includes more than 50 other models of permanent magnet and brushless d.c. motors.)

Canon
Canon U.S.A., Inc.

Electronics Components Div. • 10 Nevada Drive, • Lake Success, L.I., N.Y. 11042
516/488-6700 • Telex No. 96-1333 • Cable - Canon USA LAKS



Image processing. Your way.



Now, with the Grinnell GMR-270 Image Processing System, you can have pipeline image processing tailored to fit your application.

The GMR-270 combines the best features of our proven GMR-27 line of high speed graphic display systems with a special package of sophisticated image processing features. The result is a modular image processing system that can be furnished with any or all of the following:

- Convolution
- Image multiplication and ratioing
- Zoom and pan
- 512 x 512 panning window on a 1024 x 1024 image
- Function memories
- Pseudo-color tables
- Video digitizers with frame averaging
- Split screen and image toggling
- Full graphics and alphanumerics
- Up to four overlay memory planes
- Independent cursors
- Trackballs and joysticks
- External synchronization
- Plug compatible interfaces for most minicomputers

In addition, the GMR-270 has a display resolution of 512 x 512 pixels and a video format that is RS-170 compatible. It is housed in a rack-mountable chassis and drives standard TV monitors.

Besides the GMR-270, Grinnell manufactures two complete lines of graphic television display systems: the GMR-27 Series and the GMR-37 Series. GMR-27 units are high speed, graphic and image display systems; GMR-37 units are low cost graphic display systems. Both are available with display resolutions from 256 x 512 to 1024 x 1024.

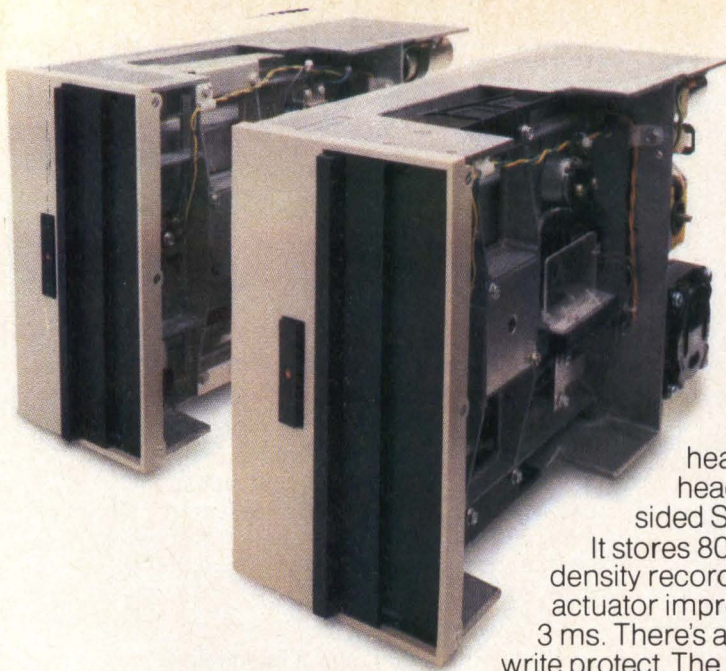
So, whether you want to analyze images from outer space or monitor a process in a plant, Grinnell has a system that can do it. For detailed specifications and/or a quotation, call or write today.

Photographs provided by Stanford University Department of Applied Earth Sciences, Palo Alto, California.

GRINNELL SYSTEMS

2159 Bering Drive, San Jose, California 95131 (408) 263-9920

CIRCLE 43 ON INQUIRY CARD



Want 400-1600 Kbytes? Choose our SA801/851 series. With the SA801 8-inch floppy, you have a choice of 400 or 800 Kbytes in single or double density, on the same drive for the same price. More than 400,000 of these standard-setting drives have been specified by OEM's around the world. They know that they can count on Shugart's proprietary read/write head technology to deliver media life of over 3.5 million passes per track, and head life of more than 15,000 hours. That's headstrong performance. And the double-

sided SA851 drive gives you even more capacity. It stores 800 to 1600 Kbytes using single or double density recording. The 851's proprietary Fasflex™ band actuator improves track-to-track access time to a fast 3 ms. There's also a programmable door lock and write protect. The headstrong SA801/851.

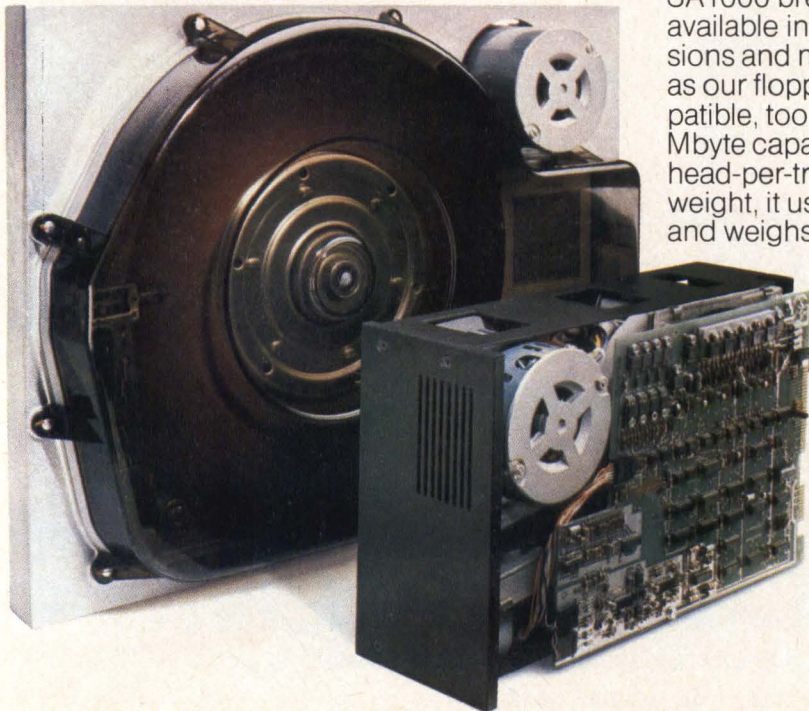
Solid performers from the leader in floppy technology.

The head Choose your

Moving up to 5-29 Mbytes? Check Shugart's SA1000 and SA4000 fixed disk drives with the lowest cost per Mbyte in their capacity range. The new 8-inch

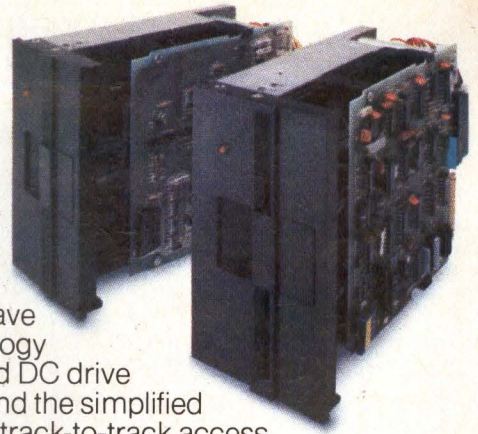
SA1000 breaks the \$1,000 price barrier and is available in 5 and 10 Mbyte versions. Its dimensions and mounting holes are exactly the same as our floppy drives, and it's electrically compatible, too. The SA4000 offers 14.5 and 29 Mbyte capacity with an optional 144 Kbytes of head-per-track storage. Compact and lightweight, it uses only 5¼ inches of panel space and weighs only 35 pounds. All Shugart fixed

disk drives use proven Winchester head and media technology to ensure better data integrity and longer trouble-free life. And system integration is easy because both the SA1000 and SA4000 can share a power supply with your floppy drives. Shugart fixed disk drives. The head of the family in capacity and cost/performance.



Need 110-440 Kbytes? The famous Minifloppy™ is the right choice. The Minifloppy stores from 110 to 440 Kbytes in a package about half the size of a standard floppy. We invented the Minifloppy family just two years ago and there are already well over 150,000 installed world wide.

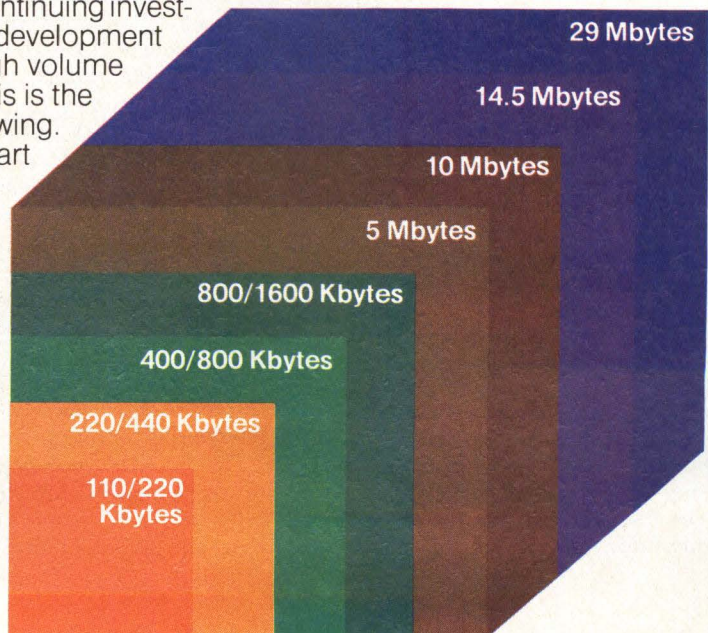
Compact size, reliability, and lowest cost per function are the reasons. Minifloppy drives have the same headstrong read/write head technology as their big brothers. The servo-controlled DC drive motor eliminates AC power requirements and the simplified actuator with direct drive spiral cam gives you track-to-track access as fast as 25 ms. The little drives offer the lowest heat dissipation of any floppy drive and feature positive media insertion, write protect, and activity light. Minifloppy. The original, and still the most popular 5¼-inch floppy drive in the world.



strong family. capacity.

The Shugart Family. Headstrong and proud of it. We're headstrong about our commitment to our customers. This means supplying you with a family of highly reliable, low cost disk drives in the quantities you need. And it means providing you with the best technical support and documentation in the industry. But it goes deeper. Like maintaining in-house control over the design and manufacture of 100% of our floppy read/write heads. And the continuing investment of financial and human resources in the development of new products and the most modern high volume manufacturing facilities in the business. This is the commitment that keeps our family growing.

Headstrong? You bet. And proud of it. Shugart Associates Headquarters: 435 Oakmead Parkway, Sunnyvale, California 94086 (408) 733-0100; West Coast Sales/Service: (408) 737-9241; Midwest Sales/Service: (612) 574-9750; East Coast Sales/Service: (617) 893-0560; Europe Sales/Service: Paris (1) 686-00-85; Munich (089) 176006; Shugart products are also available off the shelf from local Hamilton Avnet outlets.



 **Shugart**
The Headstrong Company

CIRCLE 44 ON INQUIRY CARD

Universal/Frequency Counters Add Features/Reliability

Series 99 Hundred counters from Racal-Dana Instruments Inc, 18912 Von Karman Ave, Irvine, CA 92715, encompass universal and frequency counters for bench and systems use. Significant features include 0.43" LED displays, rfi/emi shielding, GPIB interface, and high input overload protection. Indicative of the instrument's reliability is the lifetime guarantee given on a custom bipolar chip within the unit, and the 2-year warranty on all other parts.

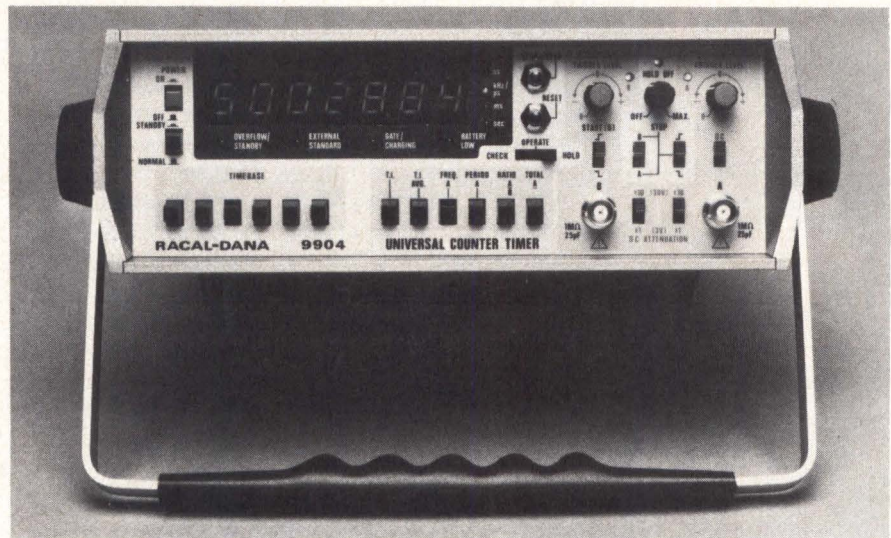
Every counter in the series is based on a bipolar LSI counter chip that has the computing power of a microprocessor but operates in excess of 60 MHz. This chip is manufactured to specification using the Collector Diffusion Isolation process. The CDI process provides benefits of high speed, excellent signal handling ability, and high intrinsic reliability. Accelerated life tests on the chip indicate a life expectancy of at least 20 years.

Universal counter/timers cover the dc to 1.1-GHz frequency range and have better than 10-mV input sensitivity. Measuring functions include frequency, period, time interval, ratio, time interval average, and totalize. Among the features are 20-MHz bandwidth on all dc amplifiers. 1-M Ω scope-probe compatible input, and overload protection up to 100 V.

Most sophisticated is the 9904—a dc to 50 MHz, 7-digit instrument for operation from either ac line voltage or optional Ni/Cad batteries. Timing measurement accuracy is increased by "trigger hold-off" and "inhibit start" features. Three-state level indicators simplify trigger level adjustment.

The 9902 is a 50-MHz counter/timer with frequency autoranging and a 6-digit display. It includes fixed trigger delay to overcome inaccuracies caused by contact bounce when measuring relay circuit for high frequency measurements. The 9906 has the same functional capabilities as the 9902, but with a 200-MHz frequency range and an 8-digit display.

The 9908 is available for uhf communications measurements with a



99 Hundred series universal counter/timer from Racal-Dana has frequency range from dc to 50 MHz and 7-digit display. Operating from ac line or battery, unit provides variable trigger hold-off and inhibit start to increase timing measurement versatility

frequency range extending to 1.1 GHz. Trigger delay and start inhibit are featured in the timing circuits. An economy bench version, the 9900 has a 30-MHz frequency range, 6-digit display, and full universal counter/timer functions.

Covering the 10-Hz to 3-GHz frequency spectrum, eight frequency counters are offered as bench, battery portable, and GPIB compatible models. Each offers superior rfi/emi performance, achieved by use of rf sealed cases, ac line filters, and specially developed circuitry to prevent input amplifier kickback. The instruments withstand overloads of 50 W rf on their signal input connectors. To ensure increased measurement accuracy, the counters incorporate optional high stability frequency oscillators with accuracy traceable to the National Bureau of Standards. Input sensitivity is better than 10 mV and input amplifiers feature automatic gain control optimizing the sensitivity when measuring high noise signals.

The 9914 is an 8-digit instrument for measurements up to 200 MHz; 9912 has a frequency limit of 120 MHz and a 7-digit display. Both in-

struments incorporate a special pulse mode for measuring submicrosecond pulse trains encountered in many logic circuits.

For the vhf/uhf spectrum, the 9917A is a precision bench instrument with a direct-gated 10-Hz to 560-MHz range, a 9-digit display, and a built-in low frequency multiplier for fast measurement and enhanced accuracy of frequencies below 25 kHz. For portable use the 8-digit, 520-MHz 9916 can be supplied with an optional battery pack. For systems applications, the fully programmable 9918 has a 9-digit display and is directly gated throughout the 10-Hz to 560-MHz frequency range.

The 9919 and 9921 uhf/microwave instruments have remote programming capabilities. Covering the 10-Hz to 1.1-GHz band, the 9919 has an 8-digit display and can be powered from ac line voltages or from internal rechargeable batteries. The 9921 is a 3-GHz microwave instrument which incorporates a 9-digit display. Options include three different internal crystal oscillators with aging rates up to 5 parts in 10¹⁰/day and GPIB interface. □

Circle 184 on Inquiry Card

WEDNESDAY

10

SEPTEMBER						
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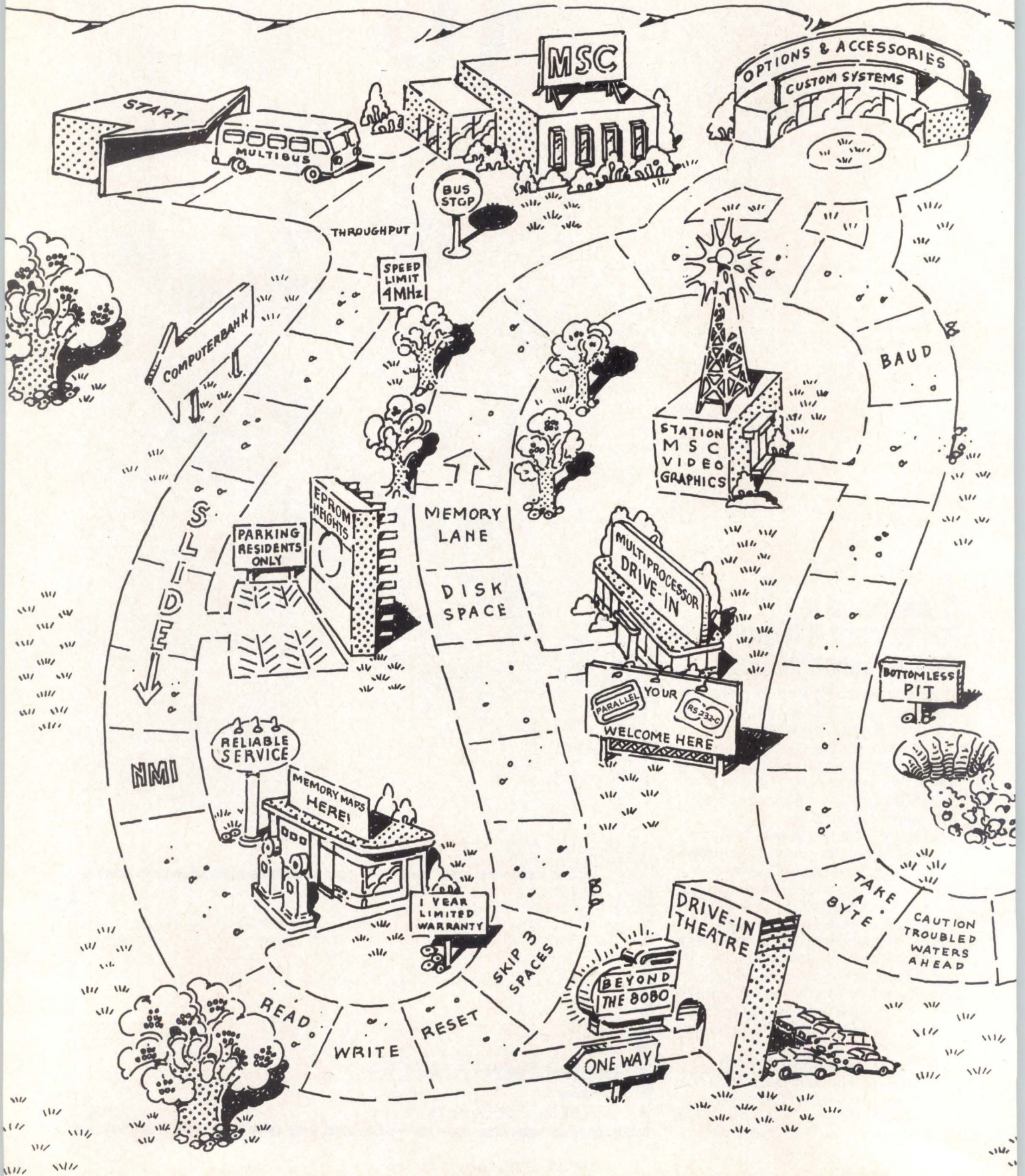
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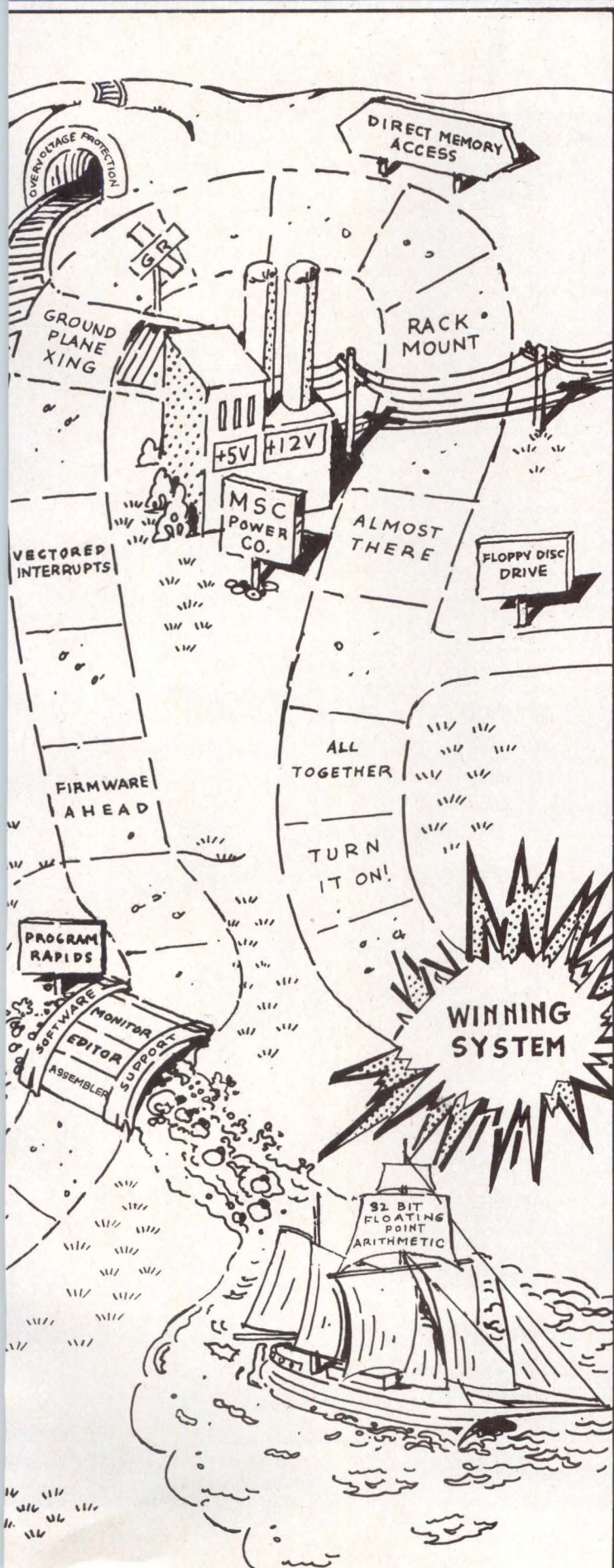
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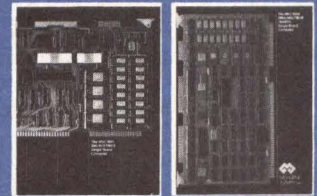
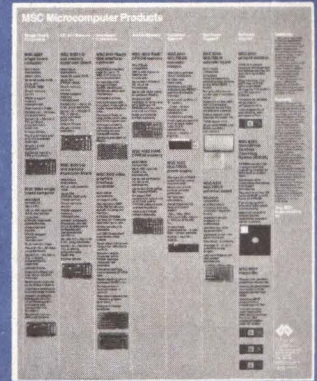
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CIRCLE 46 FOR LITERATURE
CIRCLE 139 FOR QUOTATION

AED ANNOUNCES ITS NEW DEC TEAM.

Single card RM-02[®] emulation

The fullback for the PDP-11 team is AED's new STORM-02, a hex-card controller/formatter for storage module drives.

We tried out a lot of fullbacks for the team but STORM-02 was the only player that could offer everything! Single hex-card electronics; RH-11, RM-02 and RM-03 emulation; the ability to plug right into the SPC slot on your PDP-11; plus the ability to get along with the media. That's the kind of compatibility we like!

A standard single board STORM-02 handles 4 SMDs. With an optional second hex-card, the STORM-02 can accommodate four more drives for a total capacity of over 500 megabytes.

Our big surprise was the bottom line on the contract. The OEM price for the STORM-02 is just \$2370 for the hex-card electronics — far less than any fullback in the league. The complete system with one 80-megabyte storage module drive, in quantities of one, is \$13,500 . . . about half the price of a comparable DEC fullback.

For the complete statistics and quick delivery, call or write Bob Deisher, Rigid Disk Products Manager.



ADVANCED
ELECTRONICS
DESIGN, INC.
COMPUTER PERIPHERALS DIVISION
440 Potrero Ave., Sunnyvale, CA 94086
Phone 408-733-3555, Boston 617-275-6400

RL-01[®] compatible Winchester

The linebacker for our LSI-11 team, the WINC-01, is surprisingly small for a pro. He consists of just two PCBs — one a micro-processor-based formatter/controller mounted with a SA-4008 drive, and the second, a dual-width Q-BUS interface card that inserts directly into the CPU backplane.

However, when WINC-01 proved he could deliver Winchester technology to DEC LSI-11, -11/2, -11/23 users, we signed him up immediately. He amazed us by playing with up to three SA-4008 Winchester drives and tackling up to a total of 60 megabytes of data. Additionally, he has the capacity to include a plug-in floppy disk drive.

Best of all, he bunked with the DEC RL01 driver software and we can report they are very compatible up to 20 megabytes.

In contract talks, the WINC-01 demanded considerably less than the DEC hardware: his two boards sell together for under \$1150 in OEM quantities. The complete system, including the two PCBs, an AED power supply, one SA-4008 drive and a DEC look-alike cabinet sell for \$6700 in quantities of one.

For WINC-01 technical information and quick delivery, contact Bob Deisher, Rigid Disk Products Manager.

Full color graphics system

The coach of PDP-11's team is our new AED512 graphics generating system that makes the blackboard obsolete. Now, when he plots the plays, the FIVE TWELVE's compact video terminal will display all the action in high-resolution detail using up to 256 simultaneous colors and 16.8 million different hue/intensity combinations on a 512 x 480 pixel screen. The AED512 is microprocessor controlled, and has the largest refresh memory of any system in the league.

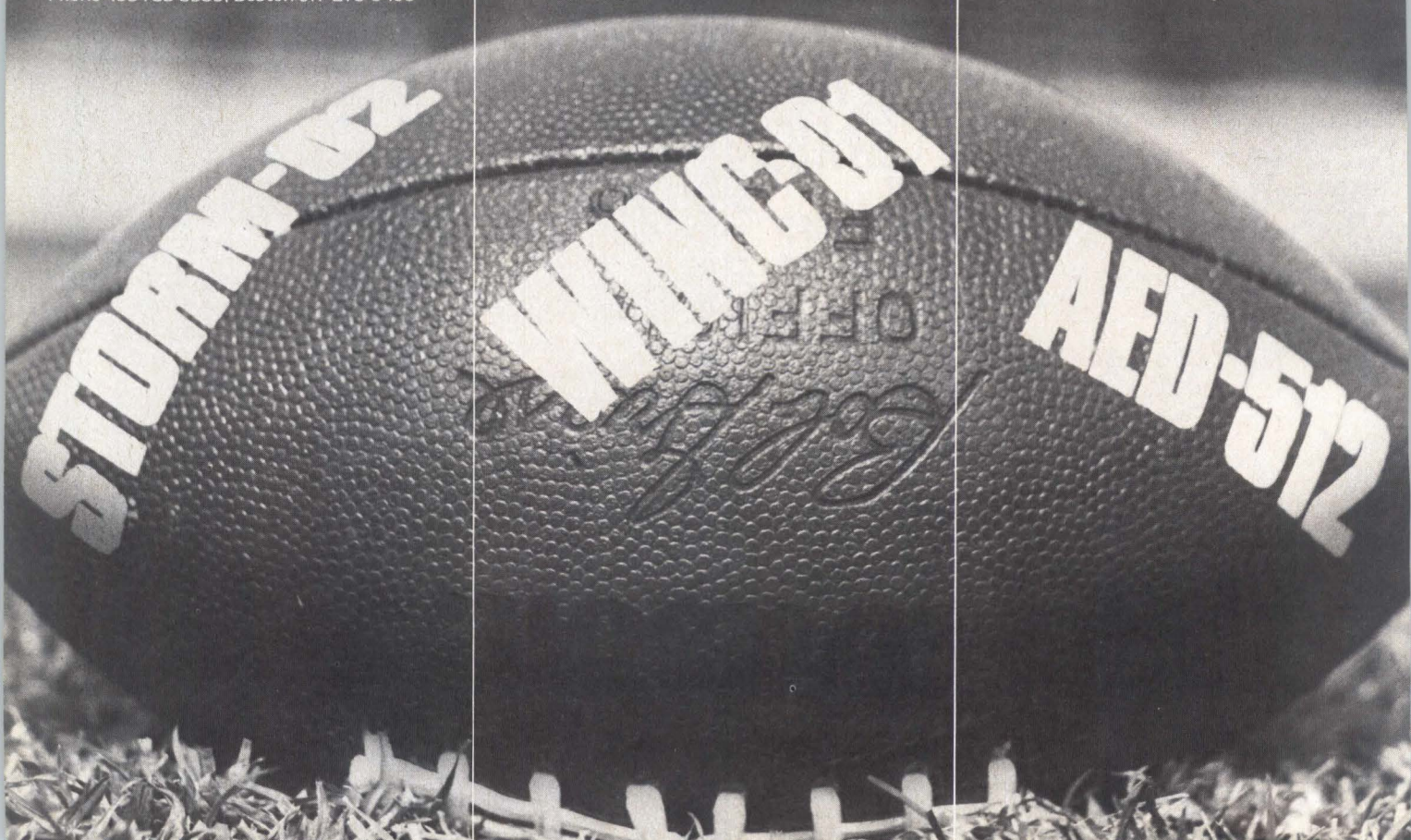
Other features that make the new PDP-11 'coach' a cost/performance leader include:

- DMA interfaces (Q-BUS[®] or UNIBUS[®]) available.
- 2:1, 3:1 . . . 16:1 zooming. Panning via integral joystick.
- Vector and circle generation. Curve fill. Single-point addressability.
- Crosshair cursor with programmable color.
- SUPEROAM panning over 1024 x 2048 contiguous pixels.
- Programmable character fonts and 8 programmable special function keys.
- \$6,875 with two colors only, excluding monitor and DMA.

For delivery information, write or talk to Jerry Kennedy, VP Marketing.

[®] Registered trademarks of Digital Equipment Corp.

CIRCLE 147 ON INQUIRY CARD



DEC LSI-11* USERS MAKE THE ANALOG CONNECTION.

WITH 5 NEW PLUG-N-PLAY RTI-1250 SERIES ANALOG I/O SUBSYSTEMS.

The RTI-1250 Series Analog I/O boards† come pre-wired, ready-to-go from the factory. Just plug them into your DEC LSI-11 chassis. Connect your analog signals. And start collecting data.

MEASUREMENT AND CONTROL MADE EASY.

Build a complete, 12-bit measurement and control system using one or more of the RTI-1250 Series boards and any LSI-11 microcomputer including the LSI-11/23. Each RTI board offers convenient wire wrap feature selection and operates directly from the microcomputer 5V supply. Memory-mapped I/O and a broad range of user-selectable features simplify board operation.

■ RTI-1250 12-bit analog input systems.

- Up to 32 single-ended analog inputs.
- 10mV to 10V full scale input range, resistor or software programmable gain.
- Software control of interrupt, auto multiplexer increment and gain ranging.
- From \$560.

■ RTI-1251, 12-bit combination analog I/O system.

- 16 single-ended analog inputs and 2 analog outputs.
- 10mV to 10V full scale input range, resistor programmable.
- Two 12-bit multiplying DAC outputs.
- From \$695.

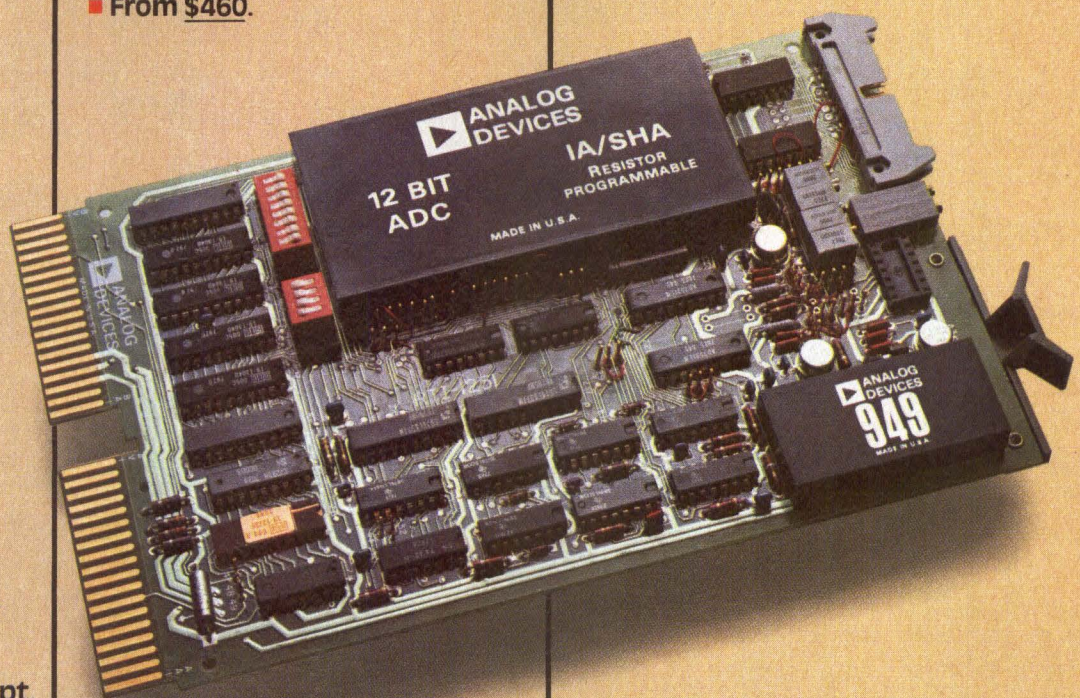
■ RTI-1252, 2 or 4 channel 12-bit analog output system.

- Field-expandable from 2 to 4 output channels.
- 4 high current digital logic drivers.
- Optional 4 - 20mA voltage-to-current loop converters.
- From \$460.

COST EFFECTIVE VERSATILITY FOR THE TOUGHEST APPLICATIONS.

Whether your application is in the laboratory or out on the shop floor, you can depend on the RTI-1250 Series for accurate and reliable measurements.

For complete information on the RTI-1250 Series or any of the other boards in the RTI family, call (617) 329-4700. Or write Analog Devices, P.O. Box 280, Norwood, MA 02062.



†Dual height size

*Registered trademark Digital Equipment Corporation.

ANALOG DEVICES

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CIRCLE 48 ON INQUIRY CARD

Microcomputer Based Coal Analysis System Replaces Large Wet Chemistry Laboratory

Whether or not coal ever returns to its former status as a primary fuel for industrial uses may be questionable. Certainly it exists in huge amounts in the U.S. as well as in other countries. However, those supplies differ in characteristics that can affect whether or not mining certain veins of coal is practical.

Before a potential source is mined at a commercial level it is necessary to measure several intrinsic values of the coal: moisture content, ash content, oxidation level, volatile matter, BTU or calorific value, and—extremely important because of current federal regulations—sulfur content. As examples, for bituminous coal an ash content of 2 or 3% is considered good, 10% is high, and 15% is bad; a 10,000 BTU measurement is considered average and 14,000 is very good. It is also important that results of the analyses be available with the least possible amount of delay.

For many years the measurement procedures to determine these characteristics were conducted in large wet chemistry laboratories, often located at some distance from the coal fields. Now, however, the same sophistication in test procedures is provided at smaller facilities closer to the sources of the coal. In addition, these small laboratories—requiring only one to three persons and using systems controlled by microcom-

puters—are easy to operate, even with unskilled personnel, and are claimed to provide improved accuracy.

Nova-Coal 1, developed by Standard Instrumentation, Inc, 3322 Pennsylvania Ave, Charleston, WV 25302, allows an operator to schedule and perform major test functions under American Society for Testing and Materials (ASTM) standards. Control is maintained by a Data General Corp microNova microcomputer with a 32k-word core memory (Fig 1). Other system components include dual floppy disc drive, 30-char/s printer, CRT terminal, and interfaces to the measuring devices. This system schedules work flow; acquires and logs data from an electronic balance, an oxygen bomb calorimeter, a sulfur analyzer, an ash fusion furnace, and several other devices (Fig 2); and controls the temperatures of four furnaces. All interim and final results are provided as hard copy by the printer; the operators do not have to make notes and are automatically alerted to equipment problems.

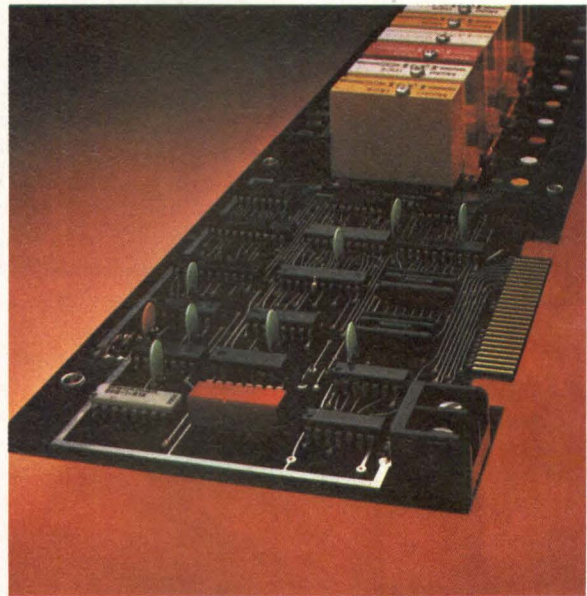
Basic Functions

There are four subsystems in Nova-Coal 1: logging in, scheduling, laboratory equipment control, and reporting. Both logging in and scheduling are entirely software. Programs are based on ASTM methodologies and are

ADDRESSABLE I/O SYSTEMS FROM OPTO 22



(PB 16S1)



(PB 16P1)

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SERIAL ADDRESSABLE RACK (PB 16S1)

Communication with multiple input/output stations.
32 station address capability per serial loop.
Up to 16 power I/O modules per station.

Switch selectable baud rate.

Opto 22 provided firmware includes message protocol, event counter, self test, watch dog timer and more.

Plug in modules provide choice of:

1. 20 Ma Current Loop.

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4. RS 232

PARALLEL ADDRESSABLE RACK (PB 16P1)

Bidirectional Communication with input or output modules.

64 station address capability.

Up to 16 Power Input/Output modules per station.

50 Conductor Daisy-Chain cable connects all racks to host controller.

On-board station address select switch.

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opto 22

Another Opto 22 product available for immediate shipment.

CIRCLE 49 ON INQUIRY CARD

DIGITAL CONTROL AND AUTOMATION SYSTEMS



Fig 1 Micro-Coal 1 control console. MicroNova microcomputer is in cabinet at right, just above dual floppy disc drive. Interfacing circuitry and audio alarm are in upper section of cabinet. CRT displays main menu, allowing operator to choose laboratory functions. Balance at left corner of desk weighs samples of up to 30 g at accuracy to 0.0001 g. Pedal switch to left of CRT terminal strobesc microcomputer for reading balance

set up to prompt the operator on every action. Because operator capabilities vary from area to area, the commands are organized on two levels—one for the beginner and another for the advanced technician. Specific instructions prompt an inexperienced operator from step to step, but an experienced operator is instructed by only one or two key words and can ignore the remaining details.

During logging in, the console asks the operator specific questions about each sample, such as the day's date, sample identification, and what analyses are required. The computer schedules the work for the day according to predetermined priorities, but priority interrupts occur whenever an analysis of higher priority than the one currently in progress requires immediate attention.

Furnace controllers vary according to the specific type of furnace to be controlled. For an ash fusion furnace, the controller is a power-proportioning type that

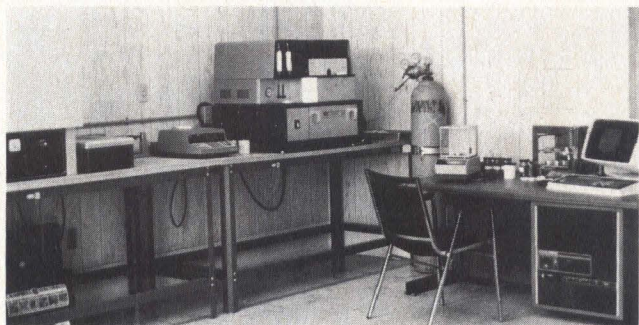


Fig 2 View of laboratory. Components (from right to left) include control console, sulfur analyzer and controller, printer, and moisture oven

increases power to the furnace in proportion to an increase in the input signal. The computer determines the amount of power by comparing its reading of actual furnace temperature and the programmed time/temperature relationship. Other furnaces, not as sensitive to power changes, are controlled by time-proportioning units.

Reports of analyses are available in several formats, either on the CRT or as hard copy from the printer. Trial summaries, for instance, can be requested at the end of the day or anytime during the day. Also, intermediate calculations can be provided on completed analyses for any specific sample. At the end of the day, reports on all completed analyses can be provided as hard copy, including the number of tests run that day,

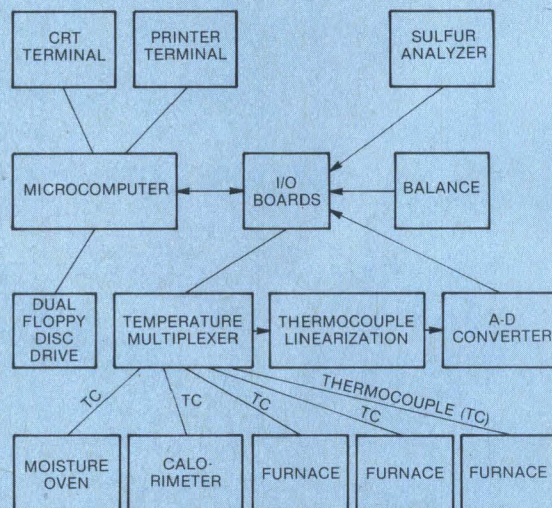


Fig 3 Hardware block diagram. Microcomputer with 32k-word core memory interfaces to laboratory instruments through I/O boards and temperature multiplexer. Each I/O board has 16 input and 16 output lines. MUX routes thermocouple signals through linearization network and then to ADC. Since calorimeter requires no linearization, it is actually read directly to the ADC (circuit not shown on diagram)

Qume introduces the Wide-Body Terminal.



Thanks to our new Sprint 5 WideTrack™ Terminal, the days of worrying about wide-document preparation are over. The Sprint 5 WideTrack is a high-quality, letter-perfect printer that's wide enough to handle balance and ledger sheets, accounting reports, over-size-paper printing masters, multiple-page form letters, charts, visual aids, and even special word processing applications. And you can interface it to the Serial RS-232C interface port of your minicomputer. The possibilities are endless.

The Sprint 5 WideTrack is the widest printer on the market today. It spaces 264 columns at 10 characters per inch, 316 columns at 12 characters per inch, and can space in increments of 1/120-inch left or right. Vertical spacing is 1/48-inch up or down, and you control it through the MOS/LSI microprocessor's extensive set of software commands.

As the newest member of the proven

Sprint 5 family of terminals, the Sprint 5 WideTrack offers all of the features that have made Sprint 5 an acknowledged leader in the quality font terminal industry. Features like MOS/LSI microprocessor electronic logic. Like the same printer mechanism that guarantees letter-perfect printing and RS-232C Serial Interface. Plus all of the things that have earned Qume its reputation for uncompromising quality and reliability in the thousands of printers that have been produced and delivered worldwide.

The Sprint 5 WideTrack. It's just one more in a continuing supply of innovative new products that Qume has developed to meet the needs of your growing market. And it's available today.

For more information on Sprint 5 WideTrack and our complete family of quality data terminals, just contact your nearest terminal dealer or Qume, 2350 Qume Drive, San Jose, California 95131.

Qume®

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CIRCLE 50 ON INQUIRY CARD

Pick a PCC that'll



Pick this Microperipheral® bundle and you can put together a floppy disk sub-system to meet *your* design needs.

One more example of how we save you development time and money. Because we do all the work for you. We "bundle" together the ideal sub-systems, provide all the equipment (our own) and service them, too.

Example—the 3812. A full megabyte of microcomputer formatted storage. Two floppy disk drives. Power supply. Built-in dual-density controller that handles up to four drives.

The 3812 lets you use your current programs because it reads and writes in single- or double-density. You save on design simplification.

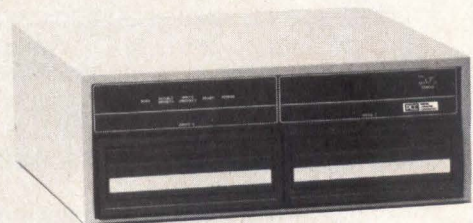
You can use S-100 bus, Intel Multibus™, Motorola Exorcisor™ and other interfaces.

It's IBM format compatible. Its retractable heads are long-lasting ferrite.

You can have an optimal direct memory access data transfer to and from disk.

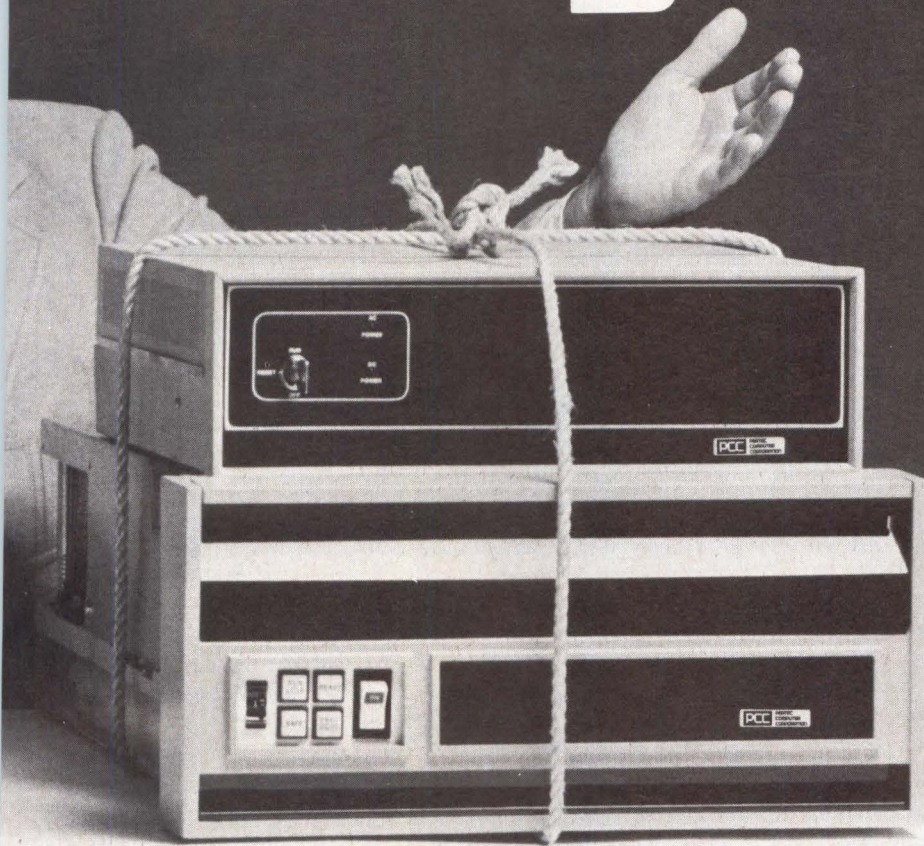
The 3812 operates under CP/M®. It supports Microsoft's FORTRAN, COBOL and BASIC.

It's the best sub-system we make. Except for the bundle on the right.



PCC SYSTEMS
PERTEC COMPUTER CORPORATION

bundle save you one.



Pick this Microperipheral bundle and you can put together 40MB from one hard disk sub-system. One more example of how we save you development time and money. Because we do all the work for you. We "bundle" together the ideal sub-systems, provide all the equipment (our own), software and interfaces. And we service them, too.

The 4511. We start with 10MB—5MB fixed, 5MB removable. We then include a controller that lets us daisy-chain three drives to it. Which means it can go all the way up to 40MB.

We also include performance in the bundle. The 4511 has 40 Msec average access time. It transfers data at 2.5MHZ. It has a security controller that's bus-oriented, with key-lock.

It speaks FORTRAN, COBOL and BASIC. It has CP/M®

It's the best sub-system we make. Except for the bundle on the left.

The 4511 and 3812 are products of Pertec Computer Corporation, an international company that designs, manufactures and services computers and computer equipment.

Microperipherals® is a registered trademark of Pertec Computer Corporation.



For more information, write Ray Kristiansen, Pertec Computer Corporation, 20630 Nordhoff Street, Chatsworth, California 91311. Or call toll-free 800-331-1001 in the continental U.S. (In Oklahoma, call collect 918-664-8300).

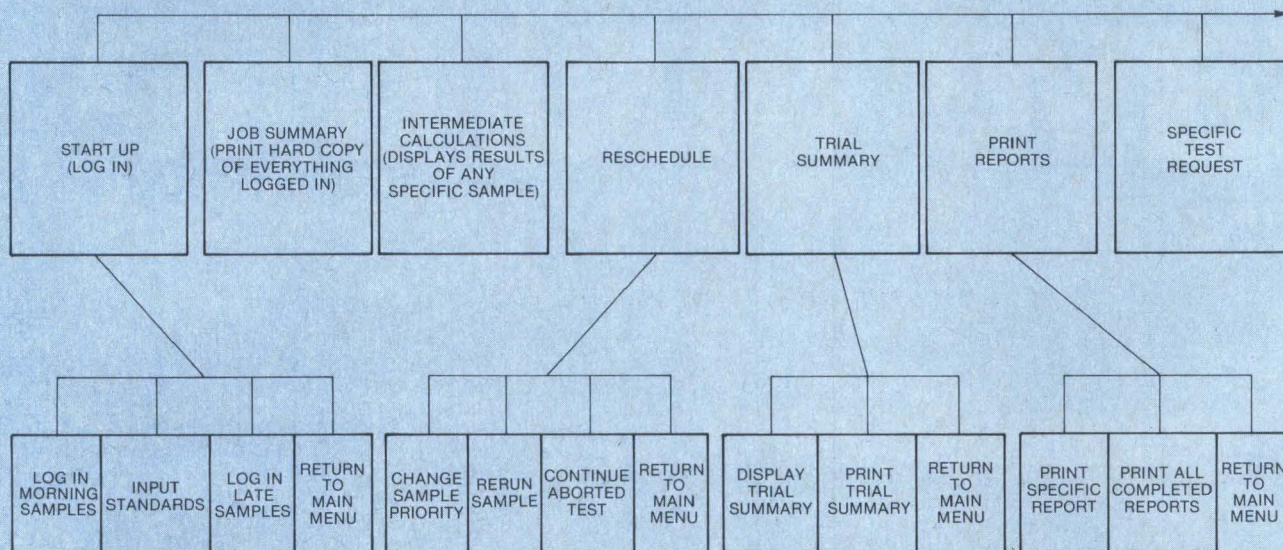


Fig 4 Software block diagram. ASTM based programs prompt beginning operators at every step, but allow experienced operators to proceed with only key word instructions. CRT reports are available at any time during analyses; hard copy reports from printer are available at end of day or at specified intervals

the amount of time required for those tests, and the number of samples completed.

Hardware

As shown in Fig 3, the microcomputer system interfaces to all measurement devices and furnaces through digital input/output (I/O) boards, each with 16 input and 16 output lines. A multitasking realtime operating system combines data from all subsystems to increase speed and precision. Two I/O boards interface to a balance that has a capacity of either 30 or 160 g, depending on the model, and can measure to 0.0001 g. Output of the balance is in BCD, requiring 4 bits/digit; one board carries digits to the right of the decimal, the other carries digits to the left. Two other boards are used to read temperatures from a multiplexing system that interfaces to the moisture oven, calorimeter, and furnaces.

The temperature multiplexer (MUX) reads temperatures from as many as 16 different sources of three thermocouple types. Since different thermocouples require different linearization circuits, the multiplexer decides which thermocouple is being read and routes the incoming signal to its appropriate thermocouple linearization network and then to the analog to digital converter.

Temperatures at various measurement devices vary widely. The moisture oven is at about 106 °C, the calorim-

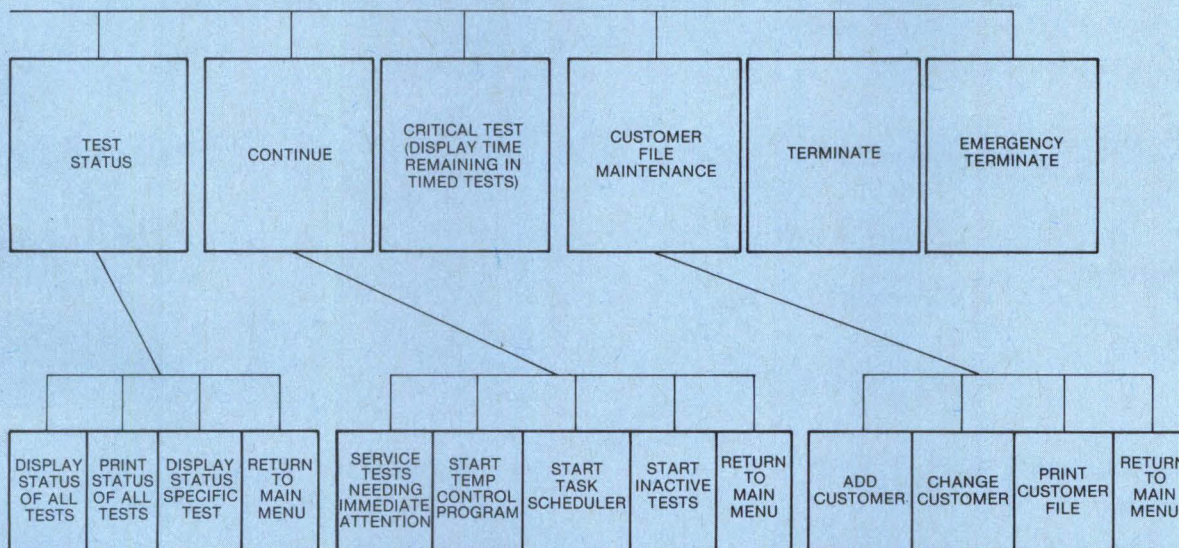
eter is at 26 or 27 °C, and a volatile matter furnace runs at from 950 to 970 °C. Yet actual temperature measurements are read to 0.001 °C.

The CRT terminal has a 1920-char display and a detached keyboard; the 30-char/s, 132-col line printer also has a keyboard for inputting instructions. A dual-diskette drive provides 752k bytes of mass memory (a hard disc drive can be included for larger systems).

Software

After turning on power to the system and inputting reference information such as day, date, and time, the operator calls the laboratory program. The main menu, or the major procedures that are to be conducted (Fig 4), include Start Up, Job Summary, Intermediate Calculations, Reschedule, Trial Summary, Print Reports, Specific Test Request, Test Status, Continue, Critical Test, Customer File Maintenance, Terminate, and Emergency Terminate. Routinely, unless a priority problem occurs, these procedures are run consecutively in the order shown on the main menu.

Start Up involves logging in identification of the sample, customer code, and tests to be run. For example, one customer might want to analyze moisture, ash, and BTU; another might want moisture, ash, and sulfur. As an option, a customer might want a standard sample to be run along with the specified tests as a check on



the accuracy of that day's analyses. Other samples can also be logged in for later processing.

Job Summary allows a hard copy to be printed of everything logged in, including sample numbers and a list of tests to be run. Intermediate Calculations is included in the main menu to enable a customer to obtain results of all tests completed at some time prior to the end of full test procedures.

The fourth function, Reschedule, allows a change to be made in priority so that the sequence of tests to be run can be varied according to a reestablished need for specific information. It also enables a sample to be rerun if some results do not seem to be correct, or if an aborted test is to be continued.

Next, Trial Summary offers the capability to request an abbreviated report of the day's tests, either as a CRT display or as a hardcopy printout. Print Reports provides the option of printing a specific report or printing all completed reports. Any given sample can be printed on its particular report form, whether or not the analysis is complete. This function is the only one that permits an incomplete analysis to be printed on a report form.

Specific Test Request allows complete data for any sample to be displayed on the CRT screen. Such data include, for example, weights of all crucibles without samples, with samples before testing, with samples after testing, and with samples after extended drying.

Similar data are maintained on all other test areas in order to assure a review of all factors if any test results are questioned. For example, if an analysis indicated an 80% ash content but the operator knew that it should never be more than 30%, all data could be recalled to determine if there had been an improper reading from the balance or some other wrong input. Test Status informs the operator which tests are complete and which are not, allows the operator to display the status of all tests on the CRT or to print them on the printer, and permits the status of any specific test to be displayed.

After all samples are logged in and the main menu is back on the screen, the operator's first action is to strike the key that initiates the Continue function, possibly the most frequently used. This begins actions of the multiplexer so that temperatures are read into the computer. It also starts the task scheduler so that the order of items presented to the operator on the CRT are controlled. Then it begins the inactive tests and services tests that require attention.

Critical Test displays the time remaining in timed tests. Customer Maintenance allows a customer to be added or changed and prints customer files. Terminate provides an orderly shutdown of the system at the end of a day's operations, while Emergency Terminate enables a quick shutdown of the system but saves all data for later recovery.

THE NEXT GREAT

Six years ago Biotation brought you the first logic analyzer. Today we bring you the industry's broadest selection. And there's more on the way.

Keeping abreast of the latest technological advances is half the battle these days. If you're designing with digital logic — especially microprocessors — you know how fast things are changing.

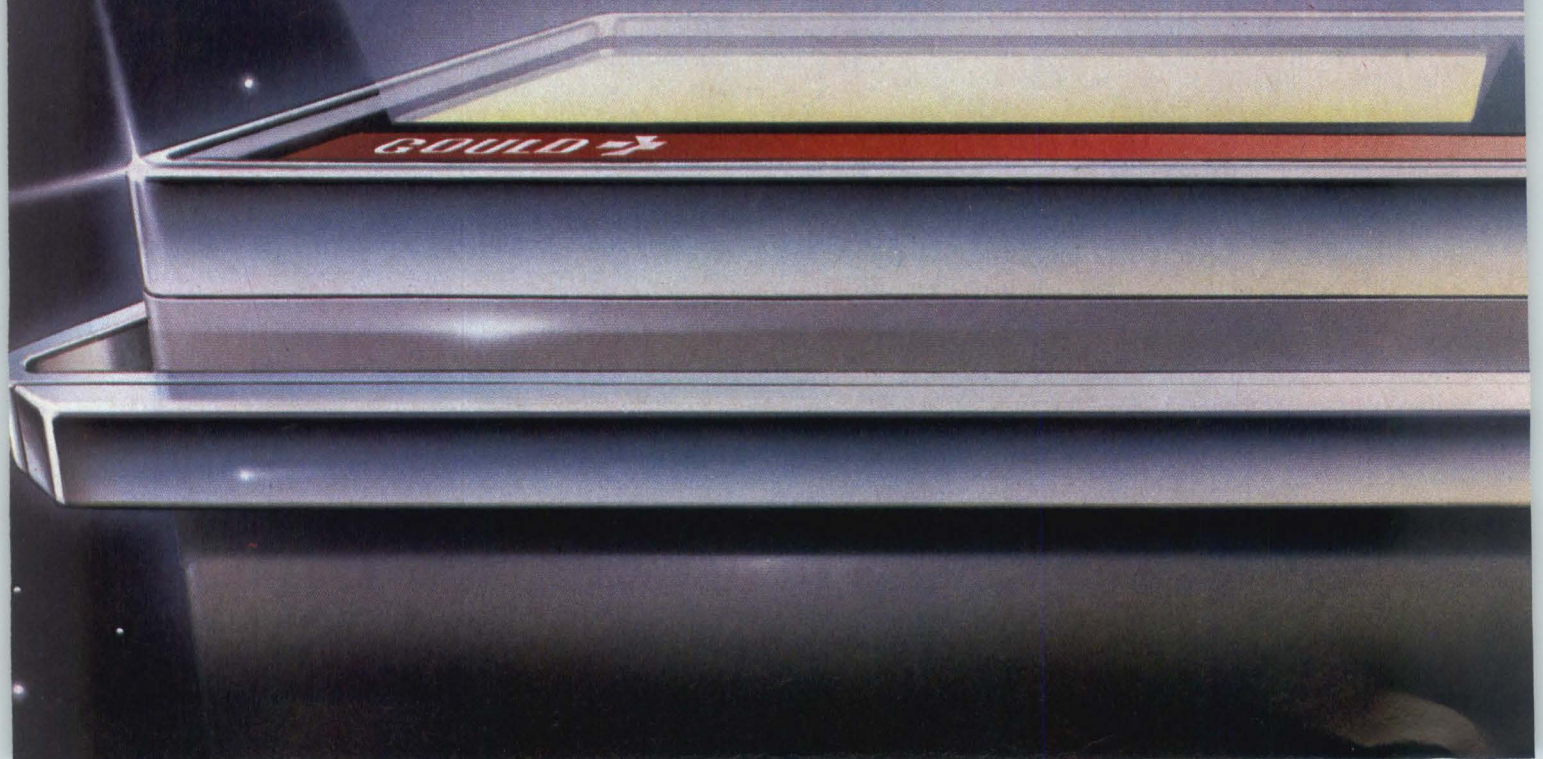
The new demands of digital logic are what Bill Moore, Biotation's first chief engineer, had in mind when he developed the logic analyzer, back in '73. He called it a "glitch fixer," designed to track and unravel the mysterious electronic glitches that plague digital logic designs.

Bill Moore was named Man of the Year by Electronics magazine for his invention.

We're proud of that. In fact, pride is a big part of everything we do. It's the secret ingredient in each logic analyzer in our broad line.

Our other "secret ingredient" is good hearing. We listen carefully to our customers. Then design our products to meet your needs. And we keep a finger on the pulse of technology. So we can understand the special demands it puts on you.

As a result, we've been first with each important logic analyzer advance. For example, when we developed "latch mode" we gave you the capabilities to latch onto glitches — random pulses — as narrow as 2 nano-seconds in current models.



GLITCH FIXER.™

Today our K100-D includes latch mode — and much more. It's the premier logic analyzer for the most complex logic problems. It combines built-in display, keyboard input, 16 channels (up to 32 with adapter) and 100 MHz sampling rate.

Not every application requires such a powerful tool. To meet your special needs, we can deliver seven models, with 8, 9, 16, 27 or 32 channels, sampling rates to 200 MHz and memory lengths to 2048 words.

Which glitch fixer is best for your application? Call us at (408) 988-6800 to discuss your needs — or any time you need technical assistance. Our application engineers are here to help. For more information on our complete line of logic analyzers, write for our catalog.

Write Gould Inc., Santa Clara Operations, 4600 Old Ironsides Dr., Santa Clara, CA 95050.

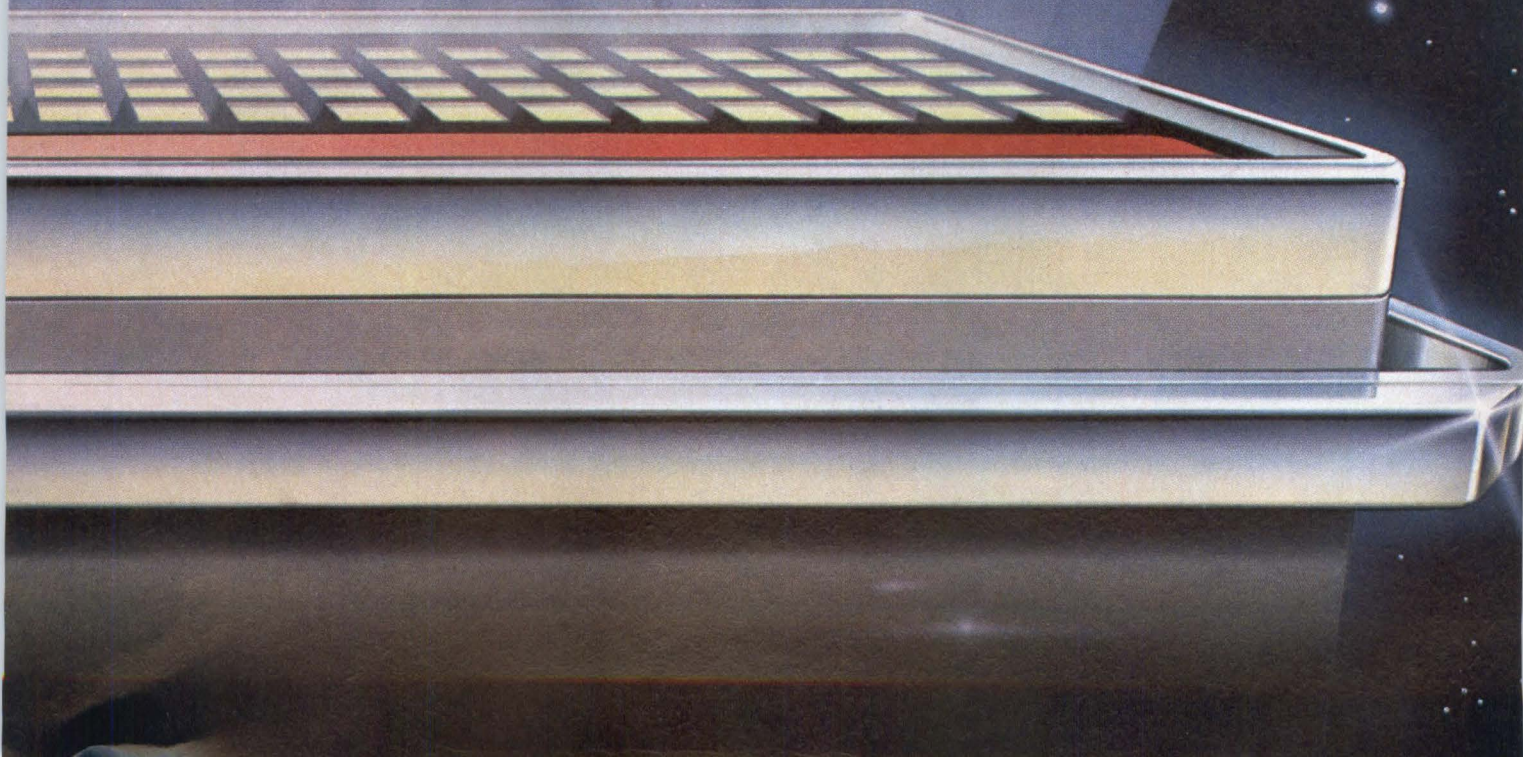
And the next great glitch fixer? One thing you can be sure of. It — and the one after it — will be wearing our name.



 **GOULD**

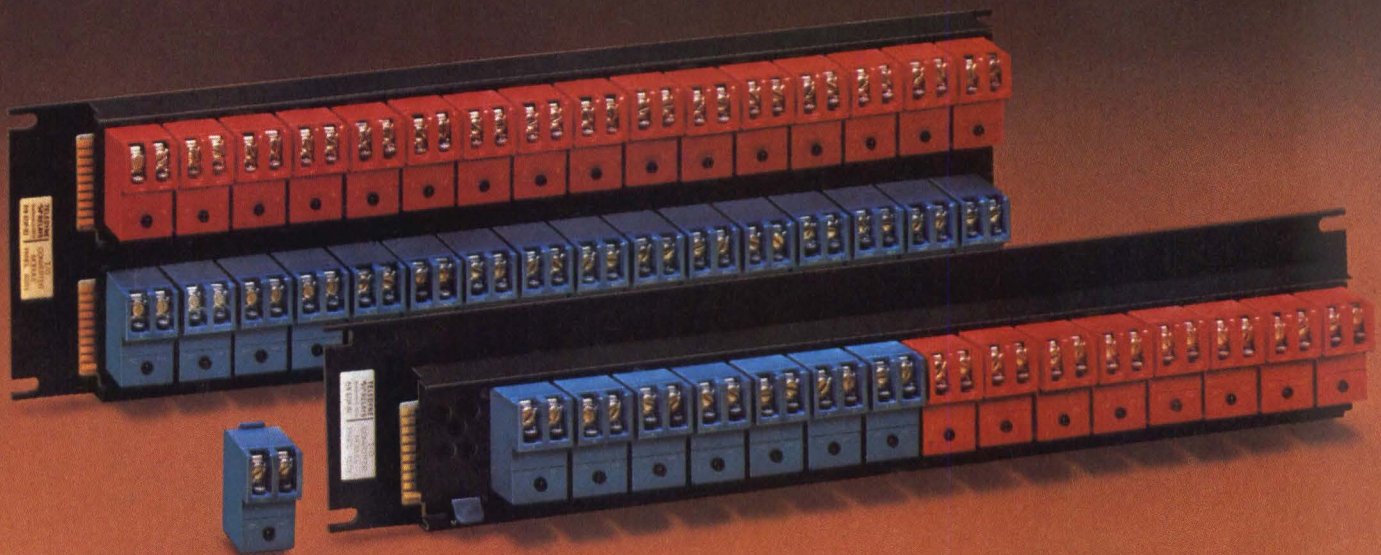
An Electrical/Electronics Company

CIRCLE 53 ON INQUIRY CARD



SSR UPDATE

We put a generation of know-how into this industrial I/O system



We brought you the first solid state I/O Interface modules for computerized industrial controls. With 5 years of experience to guide us, our 2nd generation I/O system (Teledyne 673 Series) features significant refinements in both modules and mounting panels.

The modules are smaller and more efficient. Transient and noise immunity so critical in industrial control applications are exceptionally high. Thermal ratings have been substantially improved. And the price is lower.

An all new mounting track design combines convenience, safety, appearance, and economy. Modules snap in and out, requiring no mounting screws. No exposed PC boards. AC and DC line voltages are kept off the board. Up to 16 modules fit on the single panel, 32 on the dual. Logic connections are made via a 20-pin edge connector or a rear-facing D connector. And again, the price is lower.

If you want the best in I/O systems compatible with today's microprocessor-based single board computers, call on the folks who started it all — Teledyne Relays.

 **TELEDYNE RELAYS**

12525 Daphne Avenue, Hawthorne, California 90250 • (213) 777-0077

CIRCLE 52 ON INQUIRY CARD

Seven Reasons Why Perkin-Elmer Computer Users Prefer MDB Interface Products:

1. Superior Performance
2. Quality Workmanship
3. Comprehensive Product Mix
4. Competitive Pricing
5. Better Delivery
6. One-Year Warranty
7. Worldwide Sales

Find your reason here!

■ PERIPHERAL DEVICE CONTROLLERS

MDB-46-206 Line Printer Controller; long line capability available
MDB-46-235 Card Reader Controller (Device controllers above include 15 foot cable)
MDB-46-234 Hollerith to ASC11 Converter

■ SYSTEMS MODULES

MDB-48-000 Universal Clock Module with line frequency clock
MDB-48-012 Line Frequency Clock Module
New! MDB-48-488 IEEE Instrumentation Bus Controller

■ COMMUNICATIONS/TERMINAL MODULES

New! MDB-47-102 Programmable Asynchronous Single Line Adapter (PASLA), single channel
MDB-47-102D Dual PASLA, two channels on a half-board, includes current loop; RS422 long line optional
MDB-48-024 Current Loop/RS232 Interface

■ GENERAL PURPOSE INTERFACE MODULES

MDB-48-002 General Purpose Interface Board, provides 197 user IC positions, accepts all sizes DIP packages; wire wrap pins and/or lo-profile sockets optional
New! MDB-48-002H General Purpose Interface Half-Board, provides for 91 user IC positions, wire wrap pins and/or lo-profile sockets optional
MDB-48-013 Universal Logic Module, basic 16-bit I/O board; options include second device con-

troller, two output register options; wire wrap pins and/or lo-profile sockets for 92 positions of user IC logic

New! MDB-48-013H Universal Logic Half-Board; same, with 42 user IC logic positions

■ ACCESSORY HARDWARE

New! MDB-16-398 Half-Board Mounting Kit
MDB-ULLAB-01, 02 Universal RS232 Long Line Adapter Box, six or twelve RS422 differential long line receivers/drivers converted to RS232
MDB-ULLAB-03 Universal TTL Long Line Adapter Box, twelve RS422 differential long line receivers/drivers converted to drivers/receivers
GPIO Cable Subassemblies for 20, 26, 34, 40 and 50 conductor ribbon cable; connector with 10 foot unterminated cable

MDB interface products always equal or exceed the host computer manufacturer's specifications and performance for a similar product. MDB interfaces are completely hardware compatible and software transparent to the host computer. MDB products are competitively priced, delivery is 30 days ARO or sooner. MDB places a limited one-year warranty on its controllers and tested products.

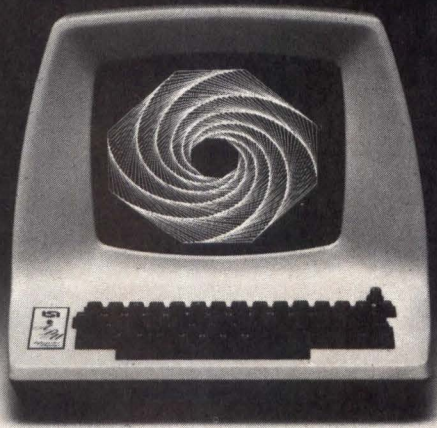
MDB also supplies similar interface modules for DEC PDP*-11, and LSI*-11, Data General,** and IBM Series/1 computers. MDB has also announced new interface modules for use with Intel Multibus Single Board Computers.^Δ Product literature kits are complete with data sheets, pricing and discount schedules.

MDB 1995 N. Batavia Street
SYSTEMS INC. Orange, California 92665
714-998-6900
TWX: 910-593-1339

* TM Digital Equipment Corp. ** Data General is a computer manufacturer unrelated to MDB

Northern California: 408/733-3950 □ Mid-Atlantic: 301/652-2173 □ New England: 617/444-1800 □ Mid-Western: 312/266-1032 □ Southeastern: 305/254-2511 □ Southwestern: 713/438-1238
Australia & New Zealand: (03) 543 2077 □ Belgium & Luxembourg: 02-720.90.38 □ Canada: 416/625-1907 □ England: (0734) 669335 □ Finland: 580377787 □ France: 630 68 39
Greece: 9514.944 9520.589 □ Hawaii: (808)524-8633 □ Hong Kong: 5-771768 □ India: 234343 □ Italy: 02/220230 □ Japan: 03-437-5371 □ Malaysia: 944 404 □ Netherlands: 03404-21344
Philippines: 89-10-96 □ Singapore: 295-2381-2389 □ Sweden: 08 38 0065 □ Switzerland & Liechtenstein: 01/730 48 48 □ W. Germany: 0 89/80 60 61-62

SOPHISTICATED GRAPHICS TERMINAL



SMALL BUSINESS SYSTEM



INVENTORY CONTROL



PORTABLE I/O DEVICE



HOME COMPUTER SYSTEM



VERSATILE DATA TERMINAL



What could anyone possibly do with 85,000 Dumb Terminals®?

That's how many ADM-3A's there are out in the field working right now. And more being shipped each day. Now just what accounts for such remarkable popularity?

Sure, it's the definitive dumb terminal, adaptable enough to fit a host of applications. It has a 12-inch diagonal screen. Full or half duplex operation at 11 selectable data rates. 1920 easy-to-read characters in 24 rows of 80 letters. 59 entry keys. An RS232C interface extension port. And direct cursor addressing.

But we wondered if all 85,000 Dumb Terminals were being used for just everyday data entry. So we checked around.

And found that people are using Dumb Terminals for things even we never thought of.

THE ADM-3A GOES INTO BUSINESS.

More and more OEM's are putting the Dumb Terminal into small business systems. They assemble a package that usually contains a disk, memory, a printer, and a video display terminal — the adaptable ADM-3A.

So the chances are that when you buy a small business system from someone, it'll contain, you guessed it, the amazing Dumb Terminal.

IT TAKES STOCK OF THE SITUATION.

Many businesses are using the Dumb Terminal, along with a light pen (Universal Product Code Decoder), to keep track of their inventory. The decoder is interfaced to the Dumb Terminal, and when a piece of merchandise imprinted with a Universal Product Code passes under it, the item is entered into a computer for tallying.

Simultaneously, the item is also displayed on the ADM-3A's screen — so it's instantly available for quick double-checking.

PROGRAMMERS LIKE IT, TOO.

Surprisingly enough, many computer programmers use the ADM-3A as an effective, portable I/O device. They can take it into a back room or, along with an acoustic coupler, to their homes if they wish, and compile programs nearly anywhere.

By using telephone lines, they can have direct access to a computer. Or, with the addition of an inexpensive cassette, the programmer can store the program on tape and enter it into the mainframe at a later date — with no loss of data.

THE DUMB TERMINAL PUTS ON A NEW FACE.

Some of our more ambitious customers have transformed their ADM-3A's into sophisticated graphics terminals. Simply by installing another PCB, they've enabled their terminals to perform complex plotting, graphics, and even draw charts.

And the Dumb Terminal is so adaptable that these industrious people had no trouble with installation — the graphics PCB required not the slightest cutting or soldering. It simply slipped right in and started working, all in a matter of minutes.

YOU CAN EVEN TAKE IT HOME TO MEET THE FAMILY.

We discovered that many computer buffs are using the Dumb Terminal as an inexpensive way to upgrade their systems. After all, the equipment found on most microcomputers leaves a lot to be desired. Such as the tiny five or six-inch screen, for instance.

By upgrading to the ADM-3A, they get a full 12-inch screen that's easy on the eyes. Not to mention

DUMB TERMINAL SMART BUY



LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

Dumb Terminal® terminal is a registered trademark of Lear Siegler, Data Products Division.

a lot of capabilities they wanted, but just didn't get on their systems.

All for only \$895.

THE DUMB TERMINAL. THE HALLMARK OF VERSATILITY.

When you get right down to it, the Dumb Terminal's applications are pretty amazing.

It can be interfaced with a staggering variety of RS232 devices. Such as cassettes, disks, floppy disk drives, printers, paper tapes, and readers, to mention just a few.

In fact, the ADM-3A is compatible with just about any RS232 device you can name. Even other video terminals, if you wish.

And people call this a "dumb" terminal?

WHAT WILL THEY THINK OF NEXT?

Who knows? But it seems that as long as there are Dumb Terminals, people will find new, unsuspected uses for them.

Of course, the ADM-3A will continue to be the same dependable data entry terminal that's made it an industry legend.

With good, reliable features and a minimum of frills. Nothing could change that. The fact is, we think that's probably the main reason that so many people have come up with so many uses for the ADM-3A.

Who said you can't teach a Dumb Terminal new tricks?

Lear Siegler, Inc./Data Products Division, 714 N. Brookhurst Street, Anaheim, CA 92803. (800) 854-3805. In California (714) 774-1010. TWX: 910-591-1157. Telex: 65-5444. Regional Sales Offices: San Francisco (408) 263-0506. Los Angeles (213) 454-9941. Chicago (312) 279-5250. Houston (713) 780-2585. Philadelphia (215) 968-0112. New York (212) 594-6762. Boston (617) 423-1510. Washington, D.C. (301) 459-1826. England (4867) 80666.

DC&AS BRIEFS

**Variations of Data Acquisition Systems Meet
Range of Factory Automation Needs**

Three configurations of microcomputer controlled "data gathering centers" differ only in the power offered to the control system designer. All 2300 series subsystems, from Logicon, Process Systems Div, 10398 Democracy Lane, Fairfax, VA 22030, are housed in NEMA enclosures for operation on the plant floor. Communication is over standard RS-232 or -422 data links at up to 9600 baud.

The DCC-2310, most powerful of the series, includes a 16-bit microcomputer and will multiplex and control up to 254 I/O points, including up to 100 analog. Digital I/O may be on/off or pulse, supervised or unsupervised. Analog inputs and outputs have a resolution of 10 bits. The -2320 offers a similar capability but for a maximum capacity of 64 I/O points and uses an 8-bit microcomputer for task scheduling and communication. Various models of the -2330 group will handle 32 on/off digital inputs only, a mix of 8 pulse and 16 on/off inputs, or a combination of 16 digital inputs, 8 digital outputs, 4 analog inputs, and 1 analog output.

Circle 160 on Inquiry Card

**Weather Station Conducts Environmental
Observations Automatically**

The MILOS automatic weather station measures, processes, and logs realtime data on temperature, wind speed and direction, humidity, atmospheric pressure, solar radiation, rain amount, precipitation, and sunshine. Hydrological and pollution sensors can also be linked. The microcomputer based automatic weather station developed by Vaisala Oy, PL 26, SF-00421 Helsinki 42, Finland, produces a weather message with the data already scaled to meteorological units and ready for distribution.

As many as nine sensors can be plugged into the station. Power consumption is 1 W with all sensors attached; solar cells or batteries can be used if desired. Sensor power is on only during measurement periods: once every 4 s for wind sensors and once every 60 s for all others. Data collected can be transmitted in real time over public telephone lines or vhf radio either automatically or through interrogation. A magnetic recorder logs up to six months of meteorological data on a single cassette. Printers, video displays, or other output peripherals can be attached through an RS-232-C port.

Circle 161 on Inquiry Card

Improve Communications Performance...

...While You Save

Just put our Model 400 Communications Storage Unit in the RS-232 link between your modem and terminal and watch your system performance improve. The 180 Kbyte flexible disk will store messages for unattended transmission or reception. The Z80A based microcomputer offers file management and operator prompted editing to build and interrogate files.

AVAILABLE IN 30 DAYS FOR UNDER \$2000.

Then count the ways you save. Compose messages at operator entry speeds, edit them, and then transmit at your system's maximum asynchronous rate — up to 19,200 baud. Use the disk to store incoming or transmit outgoing messages while unattended... at night when the phone rates are lower. But most of all, save by keeping your terminal off-line—except during actual transmission of compressed messages.

COLUMBIA
DATA PRODUCTS, INC.

**Columbia Data Products, Inc.
Peripherals System Division**

9050 Red Branch Rd., Columbia, MD 21045
(301) 992-3400 TWX 710-862-1891

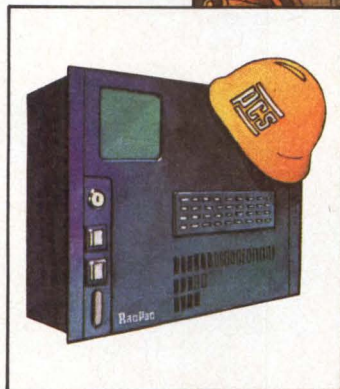
Our computers and modules wear hardhats

While others modified their existing general purpose computers to try to do factory work, we specially designed a full line of modules and microcomputer packages for rugged "hardhat" plant environments.

On Line, On the Firing Line— Full Time

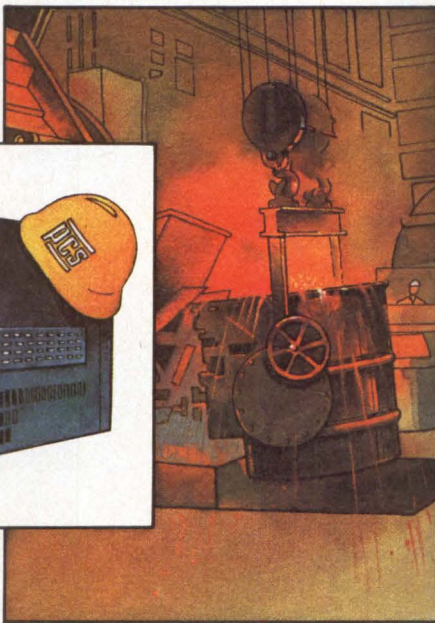
The reason our customers want to hang computers such as RacPac right at the job is simple. The computer functions are more reliable when the microcomputer puts on a hardhat and goes right out on the job. Also, it puts the controls of the machine and the information with the operator for more efficient operation and maintenance.

In a manner of speaking, our computers do wear hardhats. We don't want our industrial computers going out in the plant looking like bankers. They're engineered to withstand the industrial environment—dust, dirt, vibration and wide temperature variations.



We test components when they arrive. Then we test during and after assembly.

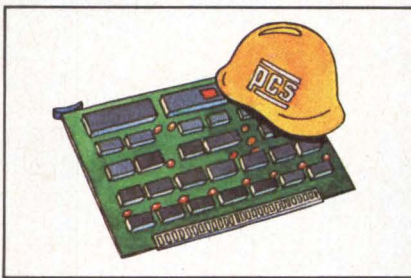
Finally, every assembly is exposed to "Shake and Bake." We vibrate products more and expose them to higher heat. Then we subject them to more power cycles. They get the same rough treatment they'll get in your plant. If something is going to fail, we want it to fail here in our plant, so that it doesn't shut down your plant.



Shake and Bake. It isn't for chickens.

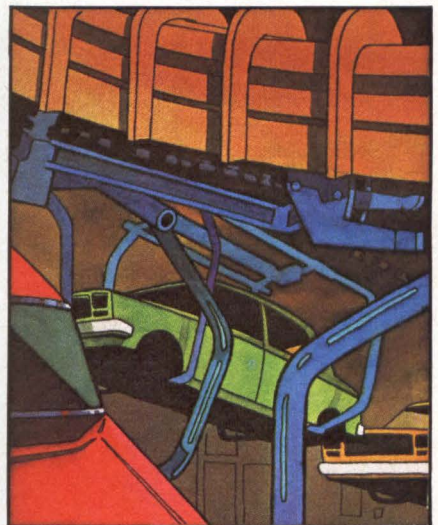
Most general purpose computers are tested prior to shipment. But test specifications vary widely. In fact, many marginal component flaws that may show up in a hostile plant, may not be discovered during typical general purpose tests.

But, the plant environment requires tougher components. That's why we test to industrial specifications.



Wide Variety of Modules

There are over 20,000 PCS microcomputers working around the world, covering virtually every conceivable industrial application. We have a wide variety of modules readily available to quickly solve your unique application—sensors, resolvers, process

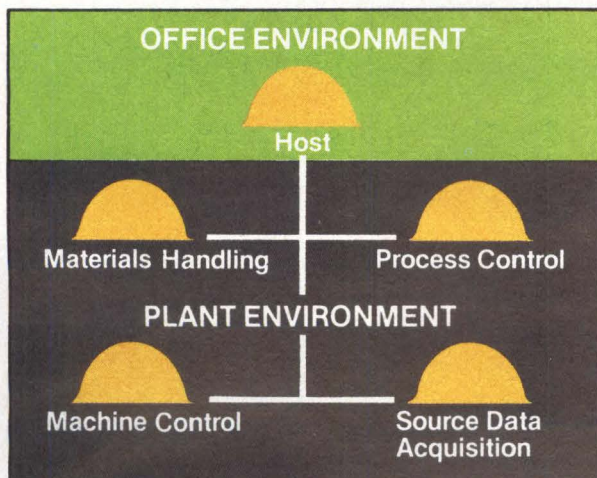


loops, A.C. motors or almost any other industrial control application. So, we probably have the modules to solve an OEM or Integrator problem now—faster, better, and more cost effectively.

One Stop Shopping

PCS takes you a step closer. We supply all the tools you need (module level, package level, software, documentation) to interface our computers with your equipment.

So, give us a call and see how quickly PCS can help solve your problem.



Plant and Host environment

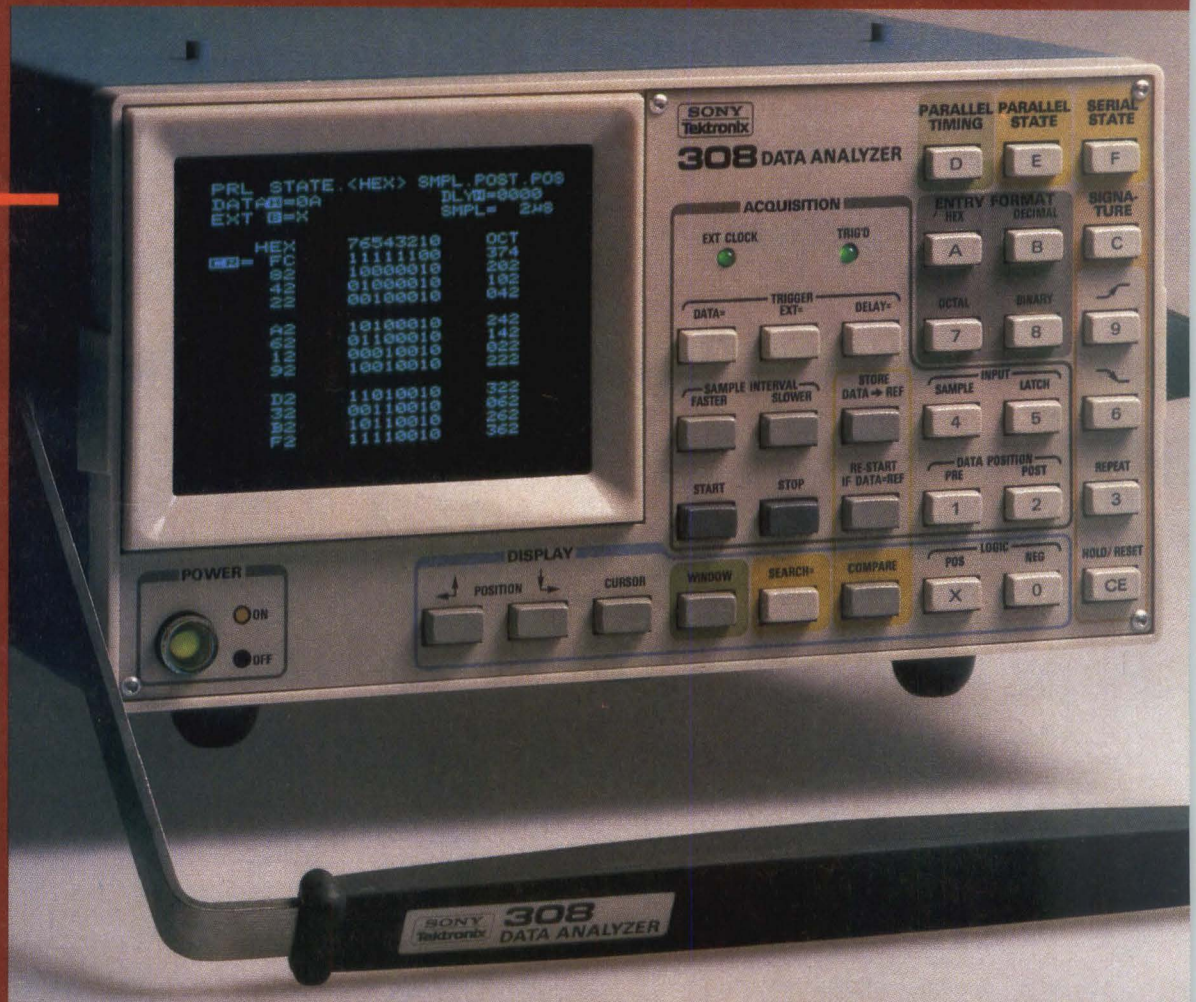
Our systems go right out into the hostile plant environment to control machines, processes, materials flow and acquire data at the source. Production data can then be supplied to a MicroHost computer located in a supervisors office and transmitted to data processing. It supplies management information that is vital for cost effective operation.



750 North Maple Road
Saline, Michigan 48176
(313) 429-4970 TWX: 810-223-8153

THE HARDHAT COMPUTER PEOPLE

308 DATA ANALYZER



308 display of parallel state data.

```

PRL STATE <HEX> SMPL POST POS
DATA=0A DLY=0000
EXT 0=X SMPL= 2MS

HEX 76543210 OCT
11111100 374
10000010 202
01000010 102
00100010 042

W-00 10100010 242
W-01 01100010 142
W-02 00010010 082
W-03 10010010 042

T-00 11010010 322
T-01 00110010 162
T-02 10110010 082
T-03 11110010 042
    
```



Parallel timing diagram can also be displayed as a state table in hex, binary and octal.



Signature display will hold and display up to 8 signatures at once.

```

SER STATE <HEX> SMPL POST POS
POS=001-002

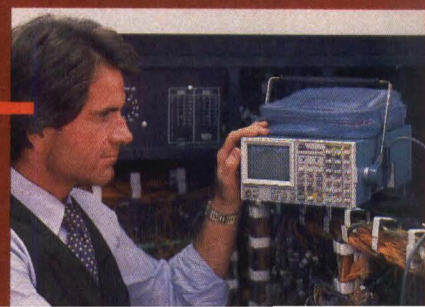
HEX 76543210 ASCII PE
00 00001010 CR LF
004***01010100**** T *
40 01001000 H

44 01000101 E
0024 00100000
01010001 Q
01010101 U

44 01001001 I
44 01000011 K
00 01001011 K
00 00100000
    
```

Serial display includes ASCII readout in addition to hex and binary.

The 308 is lightweight (3.6 kg/8 lb) and portable.



All logic analyzers handle parallel data. Only one also does serial and signature.



Introducing the 308 Data Analyzer.

Until now, logic analyzers have been confined to parallel state and timing data. Unfortunately, digital problems haven't. They might originate at a serial data port. Or appear as a faulty signature output.

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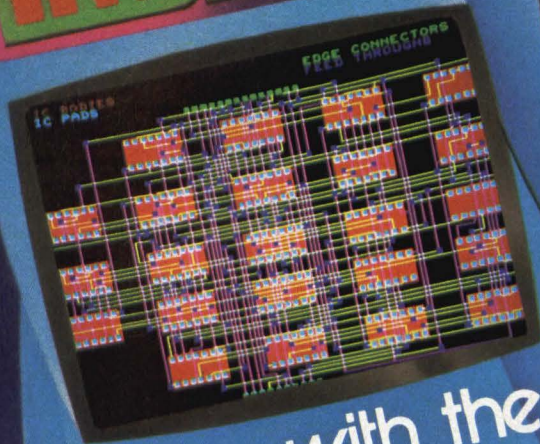
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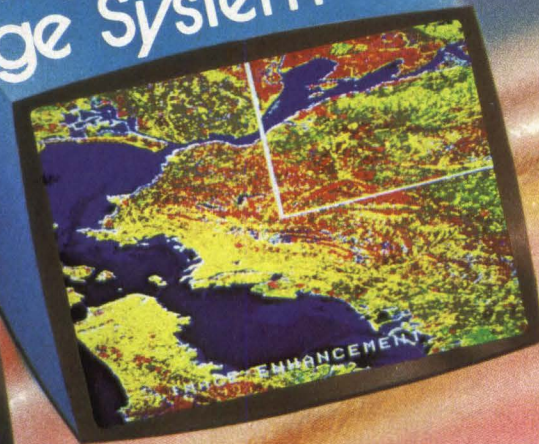
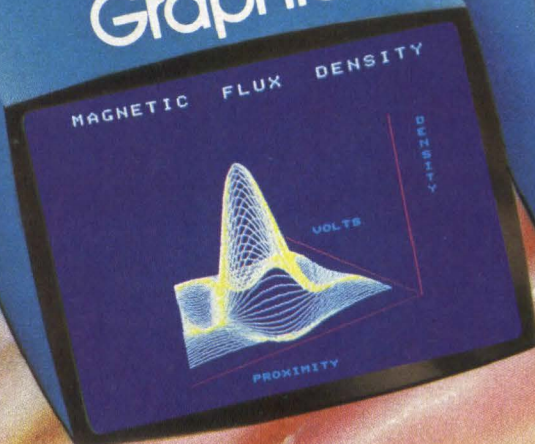
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CIRCLE 63 ON INQUIRY CARD

DIGITAL CONTROL AND AUTOMATION SYSTEMS

Multibus Compatible Intelligent Analog Peripherals Offer Diverse Data Acquisition Capabilities

Fully expandable data acquisition systems, the DT3752 and DT3754 are claimed to be the industry's first single-board intelligent analog peripherals (IAPs). Introduced by Data Translation, Inc, 4 Strathmore Rd, Natick, MA 01760, the IAPs are compatible with the Intel Multibus™ backplane. Each contains an 8085A microprocessor (CPU) based microcomputer and has an architecture that enables parallel processing relative to the CPU and the Multibus bus master.

In addition to the microprocessor and the data acquisition system, onboard components and architecture include 16k of dual-ported RAM, complete vectored interrupt system, complete direct memory access (DMA) system, two independently programmable timers, serial I/O interface with current loop, RS-232-C drivers and modem control, software programmable baud rate generator, and four P/ROM sockets. Microcomputer architecture is based upon an independent local bus structure (IAP-BUS) brought out to an external connector to allow expansion. The dual-ported RAM is the sole communication link between the onboard CPU and the Multibus bus master. Multibus communicates with one RAM port, and the local bus with the other.

Three modes of operation are possible. As a slave device on the Multibus, the IAP performs high speed intelligent data acquisition utilizing DMA while the microprocessor performs frontend data conditioning at throughput rates to 125 kHz; as a remote data acquisition system, the IAP MODEM control feature is used for long distance TTY data transmission; and as a low end, Multibus controlled data acquisition system, the IAP is capable of serial or parallel I/O.

The high level model DT3752 accepts full-scale analog input ranges of 0 to 5, 0 to 10, ± 5 , and ± 10 V. A standard unit has a 35-kHz throughput rate and 12-bit resolution. The user can externally jumper pins to obtain binary, offset binary, and 2's complement output data coding. Options include 14- and 16-bit resolution plus 100- and 125-kHz throughput rates for the 12-bit resolution model. The 14- and 16-bit versions are available with an optional high level programmable gain amplifier that provides gains of 1, 2, 4, and 8.

Users of the low level, wide performance range DT3754 can vary the value of a single external resistor to scale for any unipolar or bipolar analog input range between 10 mV and 10 V. A standard unit has 12-bit resolution with jumper selectable input polarity and output data coding; throughput rate is 31 kHz at a gain of 1. Options include 14- and 16-bit resolution and a low level, software programmable gain option with gains of 1, 10, 100, and 500.

Circle 162 on Inquiry Card

NEW! Standard yokes and flybacks for CRT terminals

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CIRCLE 64 ON INQUIRY CARD

Packaged System Provides Communication Between Process Operator and Control Computer

PROSYS I, a process/industrial measurement and control system, introduced by ADAC Corp, 70 Tower Office Park, Woburn, MA 01801, consists of a 64k-byte LSI-11/2 micro-computer, dual-port serial I/O interface, single-drive double-density floppy disc unit, and up to 18 I/O modules—all in a rollaround cabinet—plus a CRT terminal. Less than 32k bytes of RAM are assigned to software, leaving the remaining 32k bytes for user programs and data.

Analog input modules include low level millivolt digitizers, thermocouple digitizers, and high level, high speed digitizers. Output modules include digital to voltage converters as well as digital to current converters for driving industrial current loops.

Digital input modules include contact closure detectors, standard TTL inputs, and optically isolated inputs. Output modules include high current latched outputs, optically isolated outputs, and standard TTL outputs.

An isothermally designed panel with cold junction compensation allows thermocouple extension wires to be connected directly to the terminal blocks. Optical panels allow monitoring and switching of 120-Vac power.

Specific configurations vary from system to system, depending upon user requirements. However, a typical

fully loaded system could contain 32 thermocouple inputs, 16 high level analog inputs, 16 current loop drivers, 16 contact closure detectors, 16 optically isolated inputs, 128 TTL inputs, 128 TTL outputs, 32 high current outputs, and 16 optically isolated outputs.

The software package supplied is a high level, user oriented language written especially for process control and industrial automation. PRO is a completely self-contained, standalone software package, requiring no auxiliary storage, assemblers, loaders, or other utility software packages. Four main software elements allow the system to accept user statements written in higher level source language, compile and assemble these statements internally, provide the necessary operating executive and scheduling functions, and provide for execution of the user defined tasks and communications between the computer and human or process type I/O equipment. Operation is as a multitask system, capable of handling numerous tasks concurrently. User statements may be entered from the system terminal or input from offline storage media. Statements may be added, listed, deleted, and changed at will while other activated programs are being executed and process I/O points are being scanned.

Circle 163 on Inquiry Card



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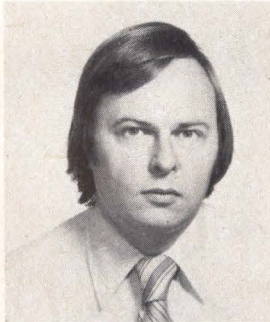
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CIRCLE 66 ON INQUIRY CARD

IEEE International Solid-State Circuits Conference



James D. Plummer
Program Chairman

February 13-15
San Francisco Hilton Hotel
San Francisco, California



J. Fred Bucy
Keynote Speaker

In its 27th year, ISSCC will focus on the expanding and complex chip circuitry that is emerging from the advances in chip techniques and technologies. More than 80 papers, presented by authors from the U.S., Japan, the United Kingdom, and Europe, will explore circuit techniques and limits of technology, VLSI, LSI systems, developments in and applications of memories, analog/digital techniques, and data acquisition. Eleven panel sessions, scheduled for Wednesday and Thursday evenings, will focus on VLSI, gigabit logic, advances in data acquisition peripherals, and universal versus dedicated microprocessors.

J. Fred Bucy, president and chief operating officer of Texas Instruments, will present the keynote address, speaking on "Semiconductor Industry Challenges" in the decade ahead, at the formal opening of the conference at 2:15 pm, Wednesday, Feb 13. In his address, Mr Bucy will assess whether the forces on the semiconductor industry—the rate of growth, magnitude of technology advances, demands by device users, pressure to conform to and to define standards, and competition—present challenges that require new approaches and strategies.

Welcoming remarks by program chairman Professor James D. Plummer, Stanford University, and the awards ceremonies will precede this address. Among the awards to be presented are the IEEE Jack Morton Award

for Outstanding Contributions in the Field of Solid-State Devices, the Cleo Brunetti Award for Outstanding Contributions in the Field of Miniaturization in the Electronic Arts, the ISSCC Beatrice Winner Award for Editorial Excellence, and the ISSCC Best Paper Awards.

Techniques and Technologies

Several of the techniques to be advanced in Digital Circuits Techniques (session 6, Feb 13, 3:15-6 pm) involve MOS logic. MOS buried logic uses buried JFET loads in a 4-stage binary counter application. Static CMOS RAMs, used in conjunction with a 150- μ W battery, provide back-up memory capability. A buried channel MOS frequency divider fabricated by dry process with electron-beam-made masks attains gigabit frequency division. Another technique that will be presented is emitter-coupled injection logic, a high density, high speed bipolar logic, with self-isolating gates, that provides the functional density of TTL and the speed performance of ECL. The final paper of this session will describe a static induction transistor logic that is compatible with 1-GHz ECL circuits.

Continuing the coverage of advances in the industry is Design Aids and Technology Limits (session 7, Feb 13, 3:15-6 pm). Papers will evaluate the effects of cosmic

The Power Paradox:

The AC power your computer needs in order to operate is also a major cause of computer error, malfunction and damage.

The computers that control your operations (and therefore your profits) are designed to operate from a clean, steady supply of ac power.

This ac power *must* be kept within manufacturer-specified tolerances in order for the computers to operate properly and safely.

In fact, the U.S. Department of Commerce states that "if a computer's voltage exceeds 120% [of the rated voltage] for a duration as short as 1 to 10 milliseconds, the computer will make errors."¹ Unfortunately, interruptions and disturbances of this nature are commonplace occurrences within most computer facilities.

A comprehensive study of power line disturbances which affect sensitive computerized equipment was conducted by two IBM researchers. They concluded that such disturbances occur on an

average of 128 times each month.² For users of computer-based equipment, power disturbances can and do create a variety of costly problems.

Effects upon data processing computers.

When these power disturbances occur in your data processing center they can cause entry errors, program changes or loss, head crash, data loss, the generation of false or garbled data, the need to rerun programs, and computer downtime.

Effects upon computerized process control equipment.

Process control equipment is also vulnerable to power disturbances. Common problems created by these

disturbances include improper batch termination and even program changes. The program changes can result in the repetition of process errors and in downtime while equipment is being reprogrammed.

Effects upon energy management systems.

Most energy management systems use small computers to make energy-saving decisions, but their effectiveness can be offset by these same disturbances. Program changes and errors may prevent useful operation of these systems as energy savers.

Thus, the computers your company depends on to reduce operating costs actually may be increasing them.

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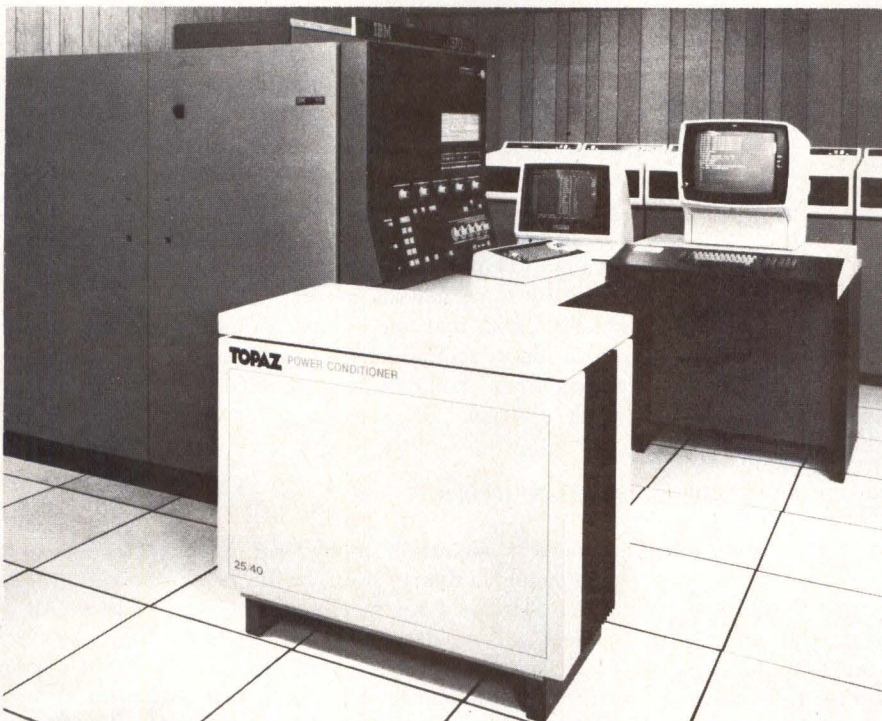
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CIRCLE 67 ON INQUIRY CARD



Topaz peripherals solve the power paradox by conditioning normal ac power for your computer and computer-based equipment.

rays on computer memories, report on an analytic MOST model that accurately measures MOST behavior and predicts fundamental limits for E/D inverters, and cover the use of thermally-grown silicon nitride films as a gate insulator for submicron-channel IGFETs. A finite element algorithm that simulates in three dimensions mobile carrier transport in semiconductors, as well as a batch fabricated monolithic capacitive pressure sensor that replaces piezoresistive transducers, will also be discussed. One of the Wednesday evening panel sessions will be surveying and comparing GaAs IC, silicon IC, and Josephson junction implementations of gigabit logic.

VLSI and LSI

Two evening panel sessions will focus on VLSI. The first, on Wednesday evening, will question whether the capability to produce chips with greater and greater levels of integration is outstripping applications. Panelists will assess whether applications for VLSI other than larger memories and more complex microprocessors exist. A panel on Thursday evening will discuss the fundamental limits and practical barriers in VLSI developments. Considered will be reliability and yield effects of scaling, hot electron trapping, soft errors, current density limitations, leakage, and circuit design tradeoffs.

LSI Systems (session 9, Feb 14, 9 am-12:15 pm) is one of two sessions to cover microprocessors. Two papers to be presented in this session will deal with a high end silicon-gate CMOS microprocessor comprised of 10,000 gates and a 4-state single-chip math processor. An 18-bit VLSI bipolar RALU (register arithmetic logic unit) will also be described. Other presentations will be a family of NMOS devices for a CPU chip, and a 1M-bit bubble memory that includes the bubble device on garnet material, and five silicon support chips fabricated with bipolar, CMOS, VMOS, NMOS, and HMOS processes. A Thursday evening panel session will address the question of universal versus dedicated microprocessors.

Memories

Leading off session 12, entitled ROMs, P/ROMs, and EROMs (Feb 14, 1:30-5 pm), will be a paper describing a 16k-bit static MOS EPROM that combines a 2-layer poly self-aligned memory cell with NMOS periphery technology. Following papers will cover a 200-ns UV-erasable EPROM fabricated in double-poly HMOS technology, a static 64k device using a floating gate type cell plus yield optimizing circuitry, and a 16k electrically erasable, nonvolatile P/ROM (EEROM). A 16k-bit P/ROM fabricated on a 140-mil square chip will be reported, as will a 4M-bit full wafer mask programmable ROM with multigate MOS structure similar to CCD.

Session 17 (Feb 15, 9 am-12:15 pm) will be devoted entirely to RAMS. The first paper will present a 1/N fractional device bipolar memory cell, the FET 1-device memory cell equivalent—that combines FET technology and bipolar speed by reversing the orientation of the transistor and capacitor. Also to be described are

an experimental 16k-bit static MTL/IIL memory chip, 2k x 8 HCMOS static RAMs, a fully static 16k-bit bulk CMOS RAM, and two 5-V 64k dynamic RAMs.

Nonvolatile solid state memory will be the topic of a Wednesday evening panel session. Developments and advances in low power MOS, EPROM, EEROM, and magnetic bubbles will be considered with the discussion focusing on functionality, performance, cost, and availability.

Analog and Digital

Traditional analog functions of filtering, tone generation, and mixing may be done today with digital processors surrounded by DACs. On the other hand, due to the same technological advances, complex multi-amplifier systems can be implemented entirely in the analog domain. One of Wednesday evening's panel sessions will discuss two approaches to analog signal processing—digital and linear VLSI.

Two ADCs will be covered in session 1 (Feb 13, 9-11:45 am). One is a 12-bit plus sign successive approximation A-D converter. The other uses a time interleaved sampling technique to afford a 400-ns conversion time. Three DACs on the agenda include an 8-channel NMOS chip with programmable ranges and endpoints; an 8-bit subsystem with 5-ns settling capability, 1.3-ns comparator, and a reference with <80-ppm/°C stability that provides analog functions for 5-MHz successive approximation A-D conversion; and a monolithic bipolar device that is compatible with both microprocessor bus and 5-V power supply.

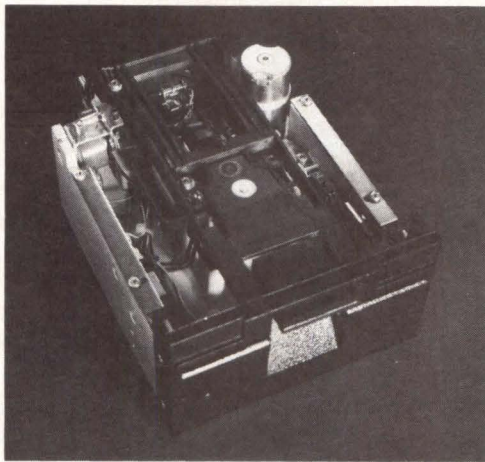
Session 11 will introduce the topic of data acquisition. This Thursday morning (9 am-12:15 pm) session promises to discuss a latching comparator chip that utilizes a junction isolated circuit to provide 0.1 LSB error for 12-bit successive approximation, a sample and hold IC with autozeroing of dc errors that provides accuracy adequate for use in 12-bit data acquisition applications, a 0.01% linear instrumentation amplifier chip, and a monolithic 5-V reference chip for A-D conversion that is accurate to ± 1 LSB. Also to be considered is an 8-channel, 8-bit CMOS data acquisition system that includes 8-word dual-port memory and onchip DMA.

Rounding out the coverage of data acquisition, a panel session (Thursday evening, 8 pm) will explore the data acquisition peripheral of the future, examining performance limits that are unique to large scale MOS and bipolar data acquisition ICs and comparing competing partitioning methods for LSI based analog microcomputer systems.

Registration

Advance registration is \$50 for members and \$70 for nonmembers. Registration at the conference is an additional \$10 for both members and nonmembers. All attendees will receive a copy of the ISSCC *Digest of Technical Papers* that includes edited and illustrated condensations of all papers. Programs with registration forms are available from Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134. Tel: 305/446-8193.

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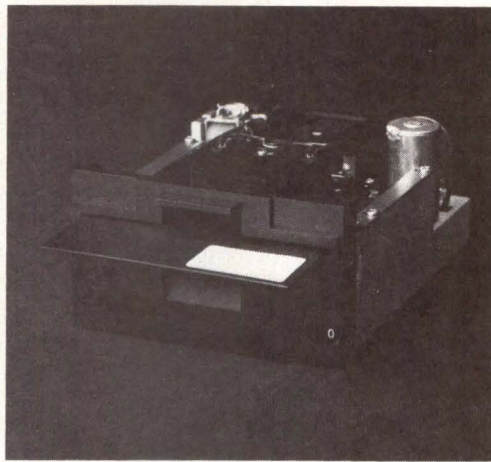
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CIRCLE 68 ON INQUIRY CARD



COMPCON

Spring 80

IEEE

Computer Society

International Conference

February 25-28

Jack Tar Hotel, San Francisco, California

Attendees will explore VLSI, networks, architecture, and applications through parallel technical themes and pre-conference tutorials at COMPCON Spring 80. Serving as General Chairman, Fred Buelow, president of Microtechnology Corp, will officially open the conference Tuesday, February 26 at 9 am. Following Mr Buelow's welcoming remarks will be the presentation of awards by IEEE Computer Society President Tse-yun Feng, professor at Wright State University. The program introduction by Technical Program Chairman Don Senzig, Hewlett-Packard, and the Keynote Address by Erich Bloch of IBM will conclude the opening session.

VLSI

VLSI is a topic that will receive considerable coverage at COMPCON Spring 80. Session 1 (Feb 26, 1:30-3 pm) will outline limits to improvements in silicon IC technology, challenges VLSI circuit design will encounter in the 80s, and the pros and cons of VLSI high performance processors. Two panel sessions (session 24, Feb 28, 10:30 am-12 noon and session 31, Feb 28, 1:30-3 pm) will explore alternative implementation techniques, and the current state of LSI technology, respectively.

Several sessions will consider aspects of import to the manufacture of VLSI chips. Session 5 (Feb 26, 3:30-5 pm) will discuss VLSI testing. Session 12 (Feb 27, 10:30 am-12 noon) will present facets of VLSI layout in-

cluding VLSI and IIL gate array layout systems, and a hierarchical approach to layout. Direct step on wafer, 1:1 projection alignment lithography, and electron beam lithography are VLSI patterning topics to be discussed in session 18 (Feb 27, 3:30-5 pm). Packaging for VLSI will be detailed in session 20 (Feb 28, 8:30-10 am).

Session 2 (Feb 26, 1:30-3 pm) will cover the evolving role of LSI and VLSI in the telecommunications industry. A language for CAD and a hierarchical VLSI design of a CAD system will be presented in session 8 (Feb 27, 8:30-10 am). Serial communications subsystems, implementation of speech synthesis algorithms, and speech recognition are the uses to be outlined in session 14 (Feb 27, 1:30-3 pm).

Networks

Service support in a network operating system, dynamic binding as a network management tool, and the guest kernel ADAPT are among the topics to be discussed in session 27 (Feb 28, 1:30-5 pm). Session 16 (Feb 27, 1:30-5 pm) will review aspects of backend networks including approaches, performance issues, trends in the technology, and their use in providing network data services, culminating with a panel discussion of alternatives to backend networks.

Two network sessions also will present architectures. Session 19 (Feb 27, 3:30-5 pm) will cover aspects of



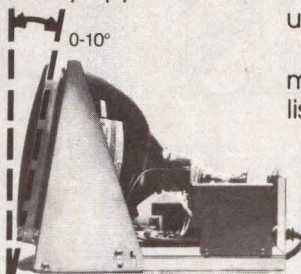
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CIRCLE 70 ON INQUIRY CARD

the architecture of computer mail systems including addressing and delivery, message protocols definition, and experience at CINCPAC with the SIGMA system. Session 32 (Feb 28, 8:30-10 am) will explore the architecture of local networks with papers presenting local networks in process control, the architecture of a microprocessor based local network, and a preliminary report on the performance of an Ethernet local network.

Architecture

Architectures to be presented in session 6 (Feb 26, 3:30-5 pm) include the data kit network architecture, that of the IBM 4300 system, and that of the HITAC-200H. Among the microprocessor based architectures to be discussed in session 28 (Feb 28, 1:30-3 pm) are the architecture of Nu-TRIX, a scalable personal computer; Pascal and virtual memory in a Z8000 based design station; and the prevention of software piracy with crypto-microprocessors.

The multiple microcomputer X-Tree will receive considerable coverage in session 22 (Feb 28, 8:30 am-12 noon). To be reported on are switching and architectural support for programming languages in the processor, the

bottom layer of its operating system, and the system in general. Also to be discussed are the distributed operating system TRIX, and a multimicroprocessor approach to discrete system simulation.

The principals and practice of dataflow systems will be expounded in session 10 (Feb 27, 8:30-10 am) and session 13 (Feb 27, 10:30-12 noon), respectively. These sessions will cover dataflow concepts for hardware design; processing element concepts for structured process description; applicative languages, dataflow, and pure combinatory code; automatic partitioning of programs in multiprocessor systems; a cellular computer architecture for functional programming; and a computer music synthesis study on a tree structured data driven machine.

Applications—Horizons

Four sessions will deal with innovations and improvements in scientific computing. Efficient memory utilization when using FORTRAN on minicomputers, dynamic memory management for structured programs, and big codes on little computers are the applications to be presented in session 7 (Feb 26, 10:30 am-12 noon). The architecture of Dorado and SPICE, a proposed personal scientific computer, will be the subjects of session 32

WHY CAN'T MICROPOLIS DO THINGS LIKE EVERYONE ELSE?

(Feb 28, 3:30-5 pm).

Papers on floating point standardization within the IEEE Computer Society, and a binary floating point arithmetic standard for new computers will be heard in session 29 (Feb 28, 1:30-3 pm). The potential of vector processors will be explored in session 17 (Feb 27, 1:30-5 pm), detailing basic requirements for a very high throughput system using second generation vector processors, multiprecision arithmetic on a vector machine, vector numerical linear algebra, optimal use of a vector processor, and cache based vector processing with a multiprocessing system.

Two applications oriented sessions will present four uses of pattern recognition and will suggest several applications for numerical analysis. Session 26 (Feb 28, 10:30 am-12 noon) will cite papers on syntactic pattern recognition and applications, application of statistical pattern recognition to speech recognition and voice authentication, survey of hand printed recognition, and engineering considerations in OCR. Papers in session 30 (Feb 28, 3:30-5 pm) will cover floating point arithmetic, numerical methods for stiff differential equations, parts and tools for FORTRAN programming, and numerical methods for unconstrained minimization.

Tutorials

The three preconference tutorials covering VLSI, distributive processing architecture, and interactive graphics will be conducted the day before the conference, Tuesday, February 25. Rex Rice will instruct "VLSI from a

User's Perspective." Designed to provide a broad interdisciplinary perspective on present and potential uses of VLSI, this tutorial will emphasize economic considerations rather than details of processors. "Distributed Processor Communication Architecture," to be taught by Kenneth J. Thurber, staff scientist with Sperry Univac, is an introductory level course on digital path and interconnect switch design for intercomputer communications. Herb Freeman, professor at Rensselaer Polytechnic Institute, will teach "Interactive Computer Graphics," presenting an overview of the problems and techniques of interactive computer graphics. The major topics will include graphics devices, system architecture, algorithms for display generation, graphic language and data structures, hidden-line and hidden-surface removal, and generation of shaded (half-tone) images.

Registration

Prior to February 8, 1979, tutorial or conference registrations are each \$50 for IEEE members. Fees for non-members are \$65 each. Late registrations will be accepted at the Jack Tar Hotel beginning Sunday evening, February 24; the late registration fee is an additional \$10. Tutorial registration includes luncheon and notes. Conference attendees will receive one copy of the *Proceedings* and two complementary drink tickets for each of the conference hosted parties Tuesday and Wednesday nights. Advance registration should be mailed to Ms Jean W. Sherman, IBM, E23/61C, 5000 Cottle Rd, San Jose, CA 95193. □

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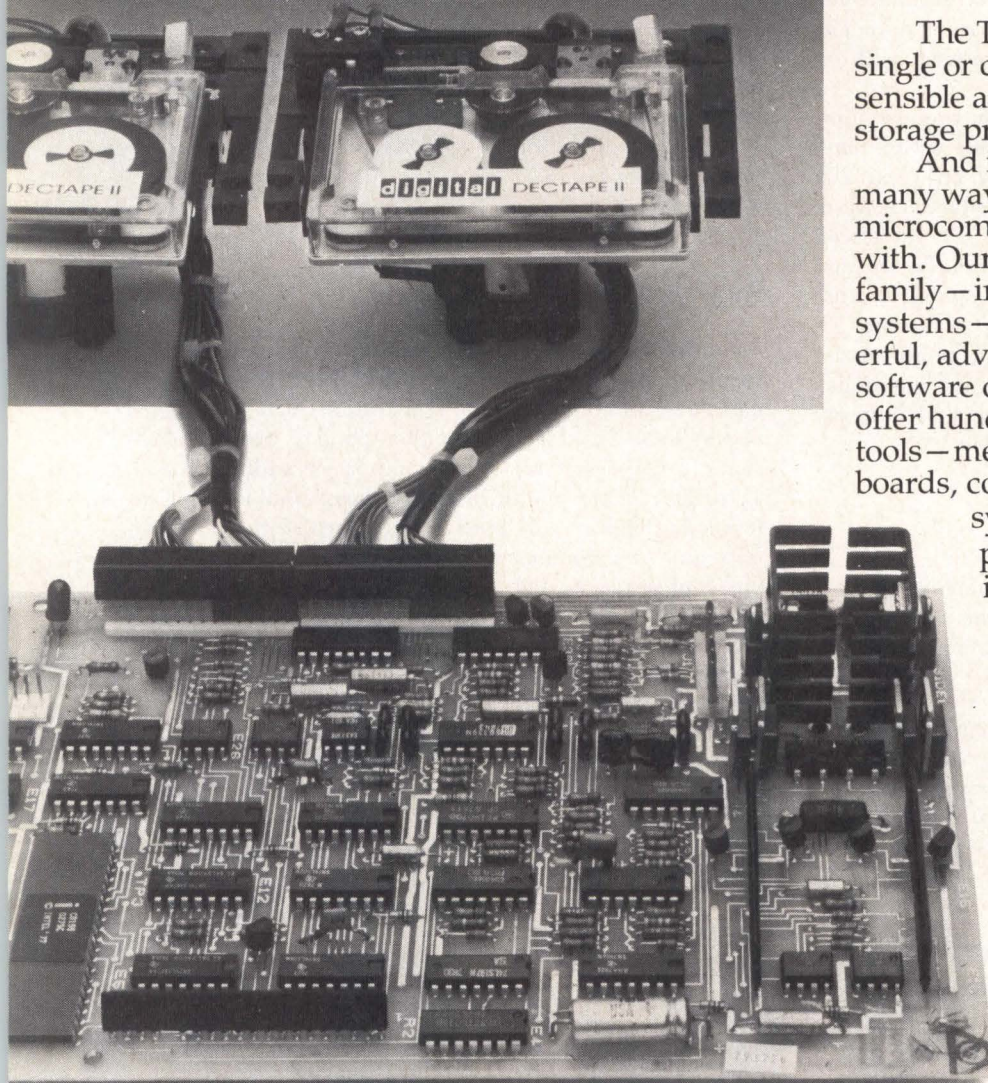
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MULTITASKING EXECUTIVE SIMPLIFIES REALTIME MICROPROCESSOR SYSTEM DESIGN

Design difficulties encountered within process control and data management microprocessor based systems are eased by imposing engineering disciplines on software designs, and by establishing standard data structures and interface protocols

Y. P. Chien Systems & Software, Incorporated, Downers Grove, Illinois

Low cost and simple architecture have made the microprocessor both technically and economically feasible for use in control applications where relatively simple inputs and outputs are required. In the majority of these applications, however, the microprocessor is inherently faster than the input/output processes under control. Therefore, the use of microprocessor technology in many applications is justifiable only when the microprocessor controls several operations at the same time. This facility is achieved by dividing the microprocessor activity among several tasks. Using this arrangement, the central processing unit time may be redirected to other activities if current task processing is precluded by delays caused by central processor synchronization with slower devices.

Performing several activities at virtually the same time—the concept of concurrency¹—overcomes the inherent speed limitations of a computer system and leads to more efficient utilization of the central processing unit (CPU). Additionally, concurrency can increase system throughput since potentially parallel operations can occur nearly simultaneously. When concurrency is applied in a typical microprocessor based system, time dependency must be introduced to facilitate proper coordination of activities, and activity scheduling and resource arbitration must be performed separately from concurrent activities within the same system.

*REX-80 is a trademark of Systems & Software, Inc, 1979.

Since concurrent operations must be coordinated and maintained within certain time constraints, the concept of real time becomes an important design aspect. In a realtime environment, additional constraints are introduced and programs become more difficult to organize and debug.² System resources require efficient management so that they can be utilized concurrently by several competing tasks. Specifically, the CPU must have the capability to direct its attention to several demanding operations.

The requisite organization for a more advanced software architecture calls for more effective software engineering disciplines. Without these disciplines, programs inevitably need modification for use in conceptually similar applications. Hence, engineering design burdens are greatly increased. The dedicated allocation of limited resources, such as memory, severely inhibits potential system performance, especially in cases where a small system, such as a single board computer (SBC), is used.

To increase software reliability and maintainability, and to alleviate problems related to concurrency in the realtime application of microprocessor based systems, a Realtime Event-Driven Executive (REX-80*)³ has been developed. This multitasking executive supplements a Z80 or 8080/8085 based system and provides the organization and facilities necessary to increase microprocessor efficiency and programming productivity.

Specific design goals are:

- (1) Provision of standard system interfaces through standardization of data structures and definition of operations.
- (2) Organization of system management based on engineering design disciplines.
- (3) Maximization of engineering resources resulting from improved software modularity.
- (4) Implementation of a software foundation suitable for multiple processor and multiple programming applications.

Design Overview

Practical limitations of the microprocessor have been carefully evaluated in implementing REX-80. The presence of the executive program, however, introduces a need for additional read only memory (ROM) and random access memory (RAM) support. In addition, any time spent processing in the executive program decreases the time available for processing the application program. Any other approach to a realtime problem will impose a similar overhead on processing time and memory space, although in many cases such processing may be more difficult to identify as overhead. Due to its organization, in all but trivial applications, REX-80 presents less overhead in both memory and processing time than other known approaches. Overhead processing is minimized through careful design of the data structures used in operations essential for the management of a realtime system.

Typical applications often involve a small dedicated computer characterized by ROM in the range of 4k to 32k bytes, and RAM in the range of 2k to 16k bytes. As a result, memory usage, particularly in RAM, is an important design consideration in most applications. The standard version of REX-80 has been implemented in a fixed configuration that should provide a solution to most applications. The implementation limits the number of tasks that can exist in the system to 255, and the number of channels for intertask communication and for interrupt processing to 32 each. As a result, the executive requires only 512 bytes of RAM and fits in 2k bytes of ROM (Fig 1). Within the 2k bytes of ROM there is still ample space for future expansion. Other hardware components necessary for the support of this version include a realtime clock and a priority interrupt controller. In an 8080/8085 based system, these components are assumed to be the Intel 8253 and 8259, respectively. In a Z80 based system, prioritization is performed by the CPU under the Mode 2 Interrupt Structure, and the realtime clock is assumed to be a Z80 ctc.

The number of channels is limited to 32 because an increase in the number of interrupts leads to an increase in the overhead imposed upon the system in terms of processing time and software management by the executive itself. Overburdening can be avoided by using multiple microprocessors in cases where an application dictates system performance beyond the practical limitations of a single 8080 or Z80 microprocessor. Limita-

tions imposed by the linkable object version of REX-80 are not absolute, and may be modified at the source level to accommodate applications requiring up to 256 communication channels, although this modification requires additional RAM.

Executive Organization

The first important design step in addressing problems of concurrency involves separation of the system into independent sequential processes or tasks. A task is an independent program or module which competes for system resources. Each task exists in a protected environment which is known as a virtual processor.^{1,4} This processor has the attributes of a hardware processor, and executes from time to time on the REX-80 virtual machine. In accordance with this concept, resources such as the CPU can be shared by several tasks, and each task appears to have control of the hardware system in the course of its processing work. Separate tasks can communicate with other tasks and I/O devices, and can compete for hardware resources. In turn, the task can terminate itself or cause another task to be activated. Significance of a task is identified by eight levels of software priority. Management of these activities is the primary function of the executive.

By establishing a virtual machine model, the executive makes programming efforts for realtime concurrent ap-

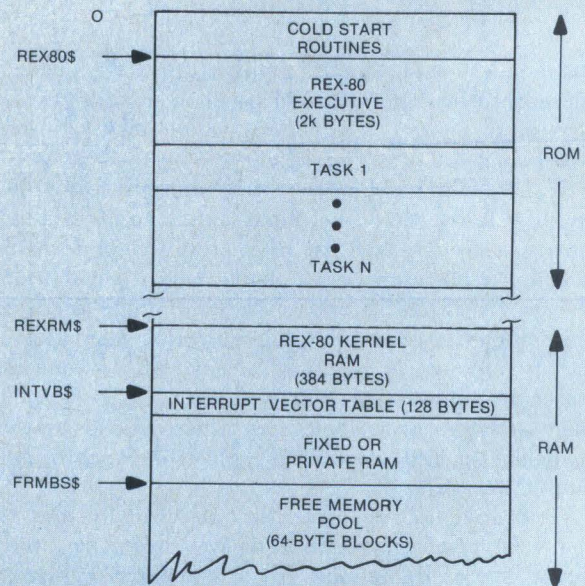


Fig 1 REX-80 memory allocation. Typically program codes reside in ROM, and cold start routine starts at location ϕ . RAM area normally starts with REX-80 kernel RAM (REXRM\$ base address) followed by interrupt vector table—INTVB\$. Application program RAM and free memory pool—FRMB\$—occupy remainder of RAM

plications more manageable, and provides an organization for regulating normal activities that arise among tasks which are sharing resources. It also supplies management for communications between tasks and external devices, facilities to provide tasks with exclusive rights to certain resources when required, and interaction with time domain parameters. Thus, the realtime executive can be divided into functional modules as shown in Fig 2. These modules and their functions are: task manager—task switching and event control, channel manager—intertask communication in software channel and I/O handling in interrupt channel, free memory manager—allocation and deallocation of RAM buffer space in a predefined block of memory called the free memory pool, and realtime manager—time-dependent event control.

Logical Abstractions

Asynchronous and dynamic operations driven by external stimuli present programming difficulties in realtime systems. To overcome these difficulties, the executive provides logical structures that mask off nonessential physical properties of the hardware. These logical structures are based upon three major abstractions: tasks, events, and channels.^{5,6} Concurrent programs may now be divided into independent sequential processes (tasks). Programming of these tasks to react to asynchronous stimuli is simplified by the concept of events. Furthermore, by utilizing the channel mechanism,

tasks may communicate with each other or with external devices and gain controlled access to critical regions. Critical regions are segments of code or resources which are, by nature, nonsharable.

Tasks and Events

Tasks are independent sequential programs which execute asynchronously and perform application processing. Under the executive, each task appears to have its own program counter, stack pointer, and machine registers. In addition, each task has interrupts and I/O, giving each all the attributes of a complete computer. Although the concept of a task as a complete computer is an abstraction, each task is treated as a unique entity in practice, and tasks are executed independently of each other. As a result, it is important that tasks conform to a predefined system protocol when accessing a resource that may be used simultaneously by other tasks. Each task occupies its own environment and, thus, does not inadvertently interface with other tasks.

Realtime demands or events are important abstractions in the executive since they form the task's interrupt structure. An event may be labeled with an event flag, which the task associates with an activity to be synchronized with in the future. Although the characteristics of events are different from those of hardware interrupts, both achieve the same important function

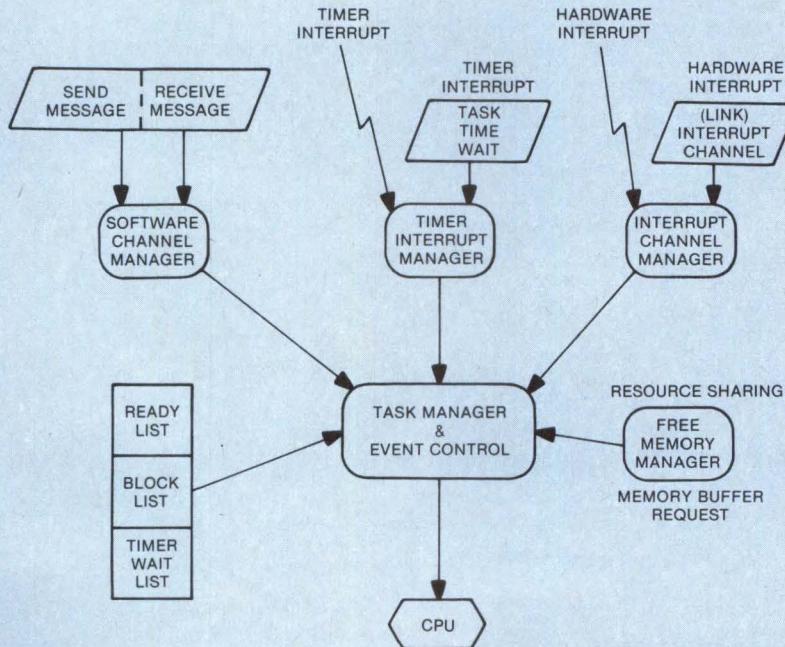


Fig 2 REX-80 organization. This structure consists of several layers of management. Interrupt functions are processed by timer interrupt handler and interrupt channel manager. Communication operations are regulated by software channel manager, and resource allocation is performed by free memory manager. These four managers operate under direction of task manager, which assigns tasks to run on hardware CPU

of synchronizing the processor with asynchronous activities. When synchronization is desired, the task waits for the event flag to change state. This action of waiting for the event flag is not performed by entering a busy-check loop, but instead is performed by the executive on behalf of the task. Task processing in effect is suspended until the event occurs; during this time period, the CPU processing time is allocated to other tasks. With this method, activation and termination of tasks are dependent on actual system processing requirements, and a more efficient utilization of CPU power is realized.

Channels

A channel is a form of monitor² with predefined data structures and operations used for intertask and external communication. Intertask communication becomes necessary when particular interactions and synchronizations need to be established in a controllable fashion between multiple tasks. In communication between a task and an external device, the channel provides the abstraction that "masks" the details of the operation of the specific hardware and provides a logical structure that makes linkage to interrupt handlers coherent.

Each of the two types of channels—software and interrupt—is assigned and referenced by a number from 0 to 31. Both types of channels are distinguished

by the context in which they are defined (channel creation), and referenced (channel invocation). Channel creation is of interest primarily at system integration time, although channels may be created dynamically at run time. From the task's viewpoint, the two channel types perform the same functions, ie, information transfers on behalf of the task. Information transfer is invoked by the task through the channel manager and handled by the I/O interrupt service routine. Functional similarity between the two types of channels is a key design feature promoting the organization of multiple microprocessors. In a multiple microprocessor environment, a task residing in one microprocessor may communicate with a task residing in either the same or a different microprocessor. Thus, the channel communication mechanism can reduce the need for re-engineering in multiple microprocessor organizations.

Channel Data Structures

Basic data structure used in channel communication is called the message control block (MCB). For discussion purposes, the MCBs used for communication in either the software or the interrupt channel are identical at the programming level (Fig 3). The MCB is a 10-byte block of RAM storage defined by the following structure:

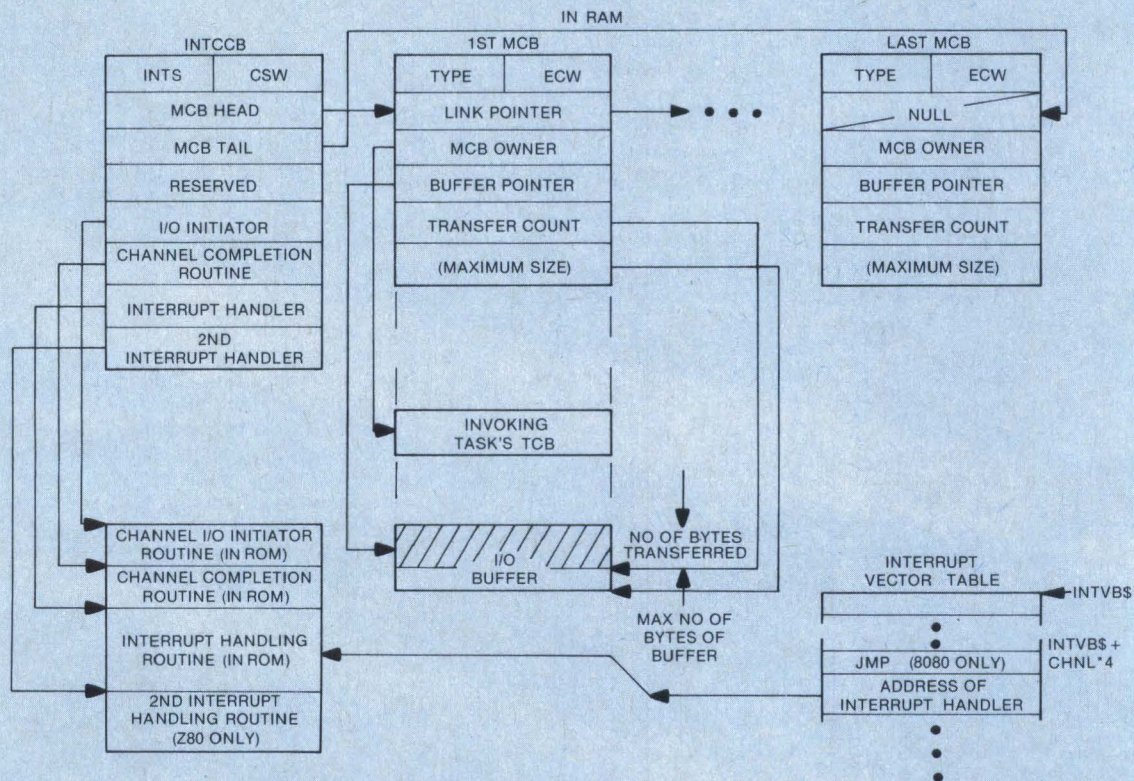


Fig 3 Channel data structure. Interrelationships between data structures used in interrupt handling and interrupt channel invocation are shown. All control blocks are allocated in RAM while interrupt handling routines are most likely located in ROM

Word Offset	Message Control Block
0	Type/Event Control Word
1	Channel Queue Link
2	Task Pointer
3	Message Buffer Pointer
4	Transfer Count

The event control word and the following two words are maintained automatically by the executive, and are not intended for interface with the task. The event control word is used to provide an association between channel operation and one specific event flag. The channel queue link is used by the channel manager in maintaining a linked list or queue for the particular channel. The task pointer is used by the channel manager to locate the sending task's event flags. The remaining five bytes—type, message buffer pointer, and transfer count—are intended for task interface. They are under complete control of the programmer, and are not referenced by the executive. The type byte may be used to indicate the kind of message service required, while the message buffer pointer and transfer count may be used to indicate the location and length of the actual message.

The MCB signifies a request for a message transfer on a particular channel. The request is maintained within another data structure called the channel control block (CCB). CCB management is the responsibility of the channel manager. The CCB describes the channel itself and the dynamic status of the channel as either busy, empty, or undefined. By contrast, the MCB represents a channel request and specifies the type, meaning, and data for the message transfer. In the case of the interrupt channel, this control block (INTCCB) contains the linkage to the actual physical device which is logically connected to the channel. In addition, this control block specifies short routines which enable and disable interrupts from the hardware, and routines for response to hardware errors. The following structure defines the interrupt channel control block.

Word Offset	Interrupt Channel Control Block
0	Interrupt Channel State/Channel Status Word
1	Channel Request Link Head
2	Channel Request Link Tail
3	Reserved
4	Interrupt I/O Initiator Routine
5	Interrupt Completion Routine
6	Primary Interrupt Handler
7	Secondary Interrupt Handler

A subset of the INTCCB, the channel control block (CCB) used in the software channel contains only the first three words of the INTCCB. The INTS (interrupt channel state) field is a byte that indicates the current status of the channel: busy, empty, or undefined. The CSW (channel status word) is a byte which may be used for passing the hardware status of the channel, for example, parity error or read on write-only channel, to an operating system. The link head and tail fields are channel queue links handled by the channel manager.

An interrupt driven device is "connected" to a particular channel in a process known as "channel creation," which may occur automatically at startup time, or at runtime under task control. Physical characteristics

of the channel are specified through the engagement of three or four programmer written routines related to the device hardware. First of these routines is a device initialization routine, called the channel preamble or channel initiator. This routine enables interrupts into the system from the hardware.

The second routine is the actual interrupt handler for the device. This routine performs the actual interrupt response, making a transfer into or out of the message control block or the buffer pointed to by the MCB per programmer standards. In addition, this routine also detects the end of service condition: for input channels, end-of-transmission recognition (ETX) and for output channels, buffer empty recognition. Since operation of the microcomputer hardware causes the interrupt handler to obtain unconditional control of the CPU in response to the interrupt, the programmer must transfer control of the interrupt process to the executive by invoking an interrupt save directive (.INTSV) as the first statement in the interrupt handler routine. The return from interrupt service is made via the interrupt exit directive (.INTEX) with the carry flag set if I/O completion has occurred, and reset if it has not.

An interrupt completion routine is the third routine which must be provided. This routine normally disables interrupts from the hardware. Like the initiation routine, this routine must not perform any interim processing, and is executed only when the channel queue becomes empty.

A fourth routine may be provided, and may be required when using certain devices in the Z80 family. This secondary interrupt handler may be provided for response to interrupts which occur as the result of a device error or failure.

Separation of channel operations into the task level and the interrupt hardware level forms the basis for homogeneous task communication. Homogeneous task communication not only makes interrupt handling easier to understand and program, but also enables the programmer to address applications of a multiple microprocessor network without being bothered with the specific details of information transfers between processors.

Software Channel Operations

After a hardware device is attached to a channel, subsequent channel requests may be invoked at the task level. The following operations are available from the channel manager in the channel request process for the software channel.

- (1) Send a message into a channel and suspend task operation until the message is received by the target task (.SENDW).
- (2) Send a message into a channel and associate the acknowledgement with an event flag (.SEND)—see (5).
- (3) Test for the presence of a message at the channel; receive waiting message or error status, a Test-and-Set function (.RECV).
- (4) Receive waiting message from channel, or suspend task operation until a message is available (.RECVW).

- (5) Return message service acknowledgement to sending task (.SIGNL).

The software channel operates as a message posting mechanism, and is bidirectional. A number of messages may be posted in the channel, and are retrieved by receiving tasks on a first-in first-out basis. Similarly, when messages are scarce, a number of tasks may cause themselves to be queued and suspended in the channel pending the appearance of messages, also in a first-in first-out manner. In either case, the software channel causes no real data transfer in terms of movement of data into and out of buffers. The channel merely transfers possession of the message's MCB from one task to another.

Interrupt Channel Operations

- (1) Link an I/O request to an interrupt channel; suspend task operation until the I/O is completed (.LINKW).
- (2) Link an I/O request to an interrupt channel; associate the I/O completion with an event flag and continue processing (.LINK).
- (3) Cancel channel operation in progress (.RSTIN).

The interrupt channel is unidirectional in most cases, and causes movement of data into and out of memory. As a result, only messages (MCBs) may be queued into a channel. A task receives messages from an interrupt channel by providing an MCB and buffer into which the message data are placed, or transmits messages into the channel by providing an MCB and buffer from which the message data are taken.

In interrupt channel operations, the task may make either single-byte or buffered transfers. In either case, the location and length of the transfer is contained in the MCB which represents the transfer. In addition, the programmer may allow the task to make the transfer in either a synchronous or asynchronous manner. In a synchronous transfer, the task initiates the transfer and then suspends itself until the transfer is completed. In this manner, the task remains synchronized with the channel activity. In an asynchronous transfer, the task initiates the transfer, either byte or block, and continues operation while the transfer takes place. The task may later synchronize with the completion of the transfer by waiting for an event associated with the transfer. In a sense, an asynchronous transfer is an abstraction of a normal direct memory access (DMA) transfer, while the synchronous transfer is an abstraction of normal programmed I/O techniques.

Virtual Machine

Events, tasks, and channels represent logical abstractions of interrupts, processors, and I/O, respectively. The significance of dealing with an application through abstractions rather than directly with the concrete entities that they represent is that they create a coherent or homogeneous work environment for the programmer. Thus, the mechanism the programmer uses in dealing with communication, for instance, is always the same regardless of the source or destination. These

three abstractions, taken together, lead to a fourth abstraction: the environment is itself an abstraction of a hardware computer, and is called a Virtual Machine.^{4,7}

The REX-80 virtual machine extends the basic hardware instruction sets to include higher level instructions that facilitate the scheduling and resource sharing caused by multiple tasks sharing the same physical processor, and that regulate realtime events such as interrupts. The extended level of instructions is handled in the form of subroutine calls termed "System Directives,"⁵ normally in the form of macroinstructions. The macro set, which defines the mnemonics of the new set of extended instructions, together with the micro-processor's native instruction set, constitutes the instruction set of the virtual machine.

Communication Handling Task

Data acquisition and process control are typical functions performed by a realtime control system. When the collected data and system status monitored by a remote system must be reported to another system in a different geographic location, interprocessor communication becomes a key design consideration. The following example illustrates the design factors taken into account by the executive's system structures. Major considerations include message error detection, communication links, and the interrupt processing used to handle a communication protocol.

Communications in the system are carried out by a dedicated task called the communication task. The primary function of this task is to continuously send requests to other processors through serial communication links (eg, UARTS). The underlying communication format is resolved and verified at the interrupt handler level. When a request is received, the processor at the other end sends a return message. Included with this message are checksums used to verify the validity of the message. If the message is correct, the task sends an acknowledgement message; otherwise, a negative acknowledgement message is sent, and the task requests a re-send. If these attempts exceed a predefined time limit, a failure will be indicated in the communication link, and an error handling routine may be invoked (Fig 4). The time-out facility is an additional precaution preventing the processor from going into an infinite loop should a break occur in the communication link.

To accomplish the preceding operations, several system directives are used.

- (1) .ALLOC n—allocates a buffer of size $n * 64$ bytes.
- (2) .LINK CHN, MCB, EFG—invokes interrupt channel (CHN) with message control block (MCB) and associates with event flag (EFG).
- (3) .MRKT n, EVG—marks a time delay of n system-time units and associates with event flag (EFG).
- (4) .CMRKT—cancels previous time-based request.
- (5) .WAITE EFG or EVG—waits for event specified in the list to occur before resuming operation.

System directives consist of a sequence of 8080 instructions in the form of macroinstructions. The sequence of instructions for a particular system directive is nor-

mally invoked at the assembly language level as macro calls. A macro library in combination with the system directives can be used to alleviate the programming load of the designer and provide a logical interface between the programmer defined task and the executive system (see Communication Task Program).

In this sequence, the I/O buffer is first obtained from the free memory pool by invoking ALLOC system directive. The transmit channel is then invoked, and sends a predefined command message to the remote processor. At the same time, the receiver channel is invoked to receive the return message. The entire communications process must be accomplished within a predefined time limit. A time-out normally signifies unsuccessful communication efforts that may be due to a noisy or dead line. The time limit is established using .MRKT system directive.

Microprocessor Networks

Technological trends have clearly indicated the need for microprocessor based systems with high performance and low cost. The use of several microprocessors within a system can achieve throughput beyond the physical limitations of even a full sized minicomputer, at considerably lower cost. Furthermore, with the advance of microprocessor architecture technology, specialized microprocessors are now capable of performing dedicated processing operations. Examples include Intel's universal peripheral interface processor (8041) and 8089 I/O processor.⁸ Both are programmable to handle specific applications and I/O intensive processing.

Modern technology has made the concept of a microprocessor network more feasible economically. In such a network, several microprocessors work simultaneously, communicating through I/O ports and/or shared system memories. The network form of distributed processing presents a feasible approach to realtime applications. This is made evident not only by the introduction of intelligent peripheral processor chips, but also by the introduction of board level intelligent slave processors, such as the SBC-544 communication processor. However, by connecting several microprocessors together into a network of microprocessor systems, new concerns and challenges in terms of system development and testing arise.⁹

Program Testing in Microprocessor Networks

Since REX-80 is based on the idea of the virtual processor, it provides a conceptual solution to the above problem through two system attributes.

- (1) Separation of the task from the actual hardware I/O operation—homogeneous task communication.
- (2) Separation of the task from the actual hardware processor—processor transparency

By example, examine a situation in which interprocessor communication is established between two identical processors A and B.¹⁰ There is one task in Processor A, labeled TA, and one in Processor B, labeled TB. Each task is responsible for the maintenance of communication between the two processors. Residence of the tasks in different machines makes their interaction difficult to test and debug.

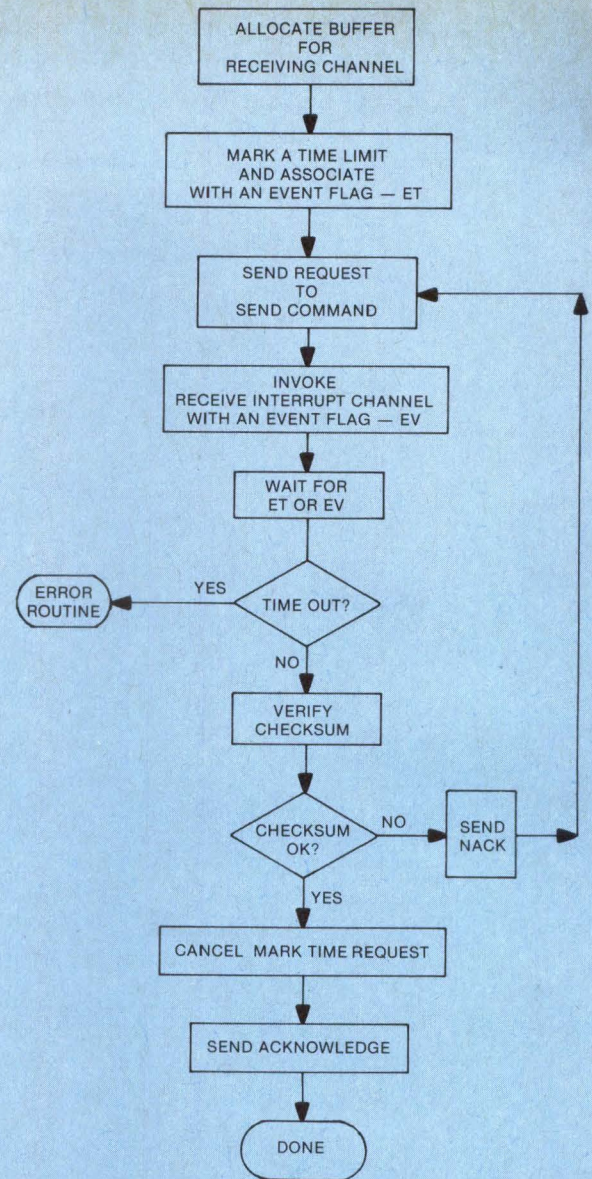


Fig 4 Communication task. When message is received through interrupt channel, checksums are used to determine its validity. If error is detected, re-sends are issued until predefined time interval has elapsed

Task TA-----Interrupt Channel-----Hardware Interface
< Machine A >

X

Task TB-----Interrupt Channel-----Hardware Interface
< Machine B >

Since a task defines a virtual processor, it makes no difference to the task which processor (A or B) it actually runs on, because it assumes that it is a processor. Furthermore, with the channel mechanism, the sending and receiving tasks are unaware of the location of one another. Actually, the exact location of the tasks should be of no concern in requesting the message exchange. This processor transparency together with the hardware independence of the interrupt channel at the task level allows program logic to be tested on a single processor. As shown in the diagram below

Communication Task Program

```

RELMCB                                ;private storage
XMTMCB                                ;private storage
TIMDLY EQU 5                          ;wait for 5 system time unit
XMTCHL EQU 1                          ;Channel 1 for send
REVCHL EQU 2                          ;Channel 2 for receive
EVG EQU 1                             ;Event flag 1 for receive channel
ETG EQU 2                             ;Event flag 1 for receive channel
EBG EQU 3                             ;event flag to use SFTMCB
SIZE EQU 2                            ;message maximum block size
MCB.BUF EQU 6                         ;offset to buffer pointer
MCB.SIZ EQU 10                        ;offset to buffer length
COMTSK EQU $                          ;

.ALLOC SIZE ;allocate buffer for receive message
SHLD RECMCB+MCB.BUF
;return address in [HL]
LXI H,SIZE*64 ;maximum buffer size
SHLD RECMCB+MCB.SIZ
;

;
; Set-Up Request Message Buffer
;
LXI H,REQST ;
SHLD XMTMCB+MCB.BUF
;transmit buffer message address
LXI H,SIZE*64 ;set arbitrary size
SHLD XMTMCB+MCB.SIZ
;
.SNDREQ: .MRKT TIMDLY,ETG ;set up a time limit
.LINK XMTCHL,XMTMCB
.LINK RECVCHL,RECMCB,EVG
;invoke receive channel
.WAITE ETG or EVG ;wait for events to occur
CPI ETG ;event number return in [A]
JZ TIMEOUT ;time out if event ETG occurs
;
;
; Verify Checksum
;
LHLD RECMCB+MCB.BUF
;get message buffer
LDA RECMCB+MCB.CNT
;get # of bytes received
CALL VERIFY ;check sum
JNC GDBUF ;good buffer assumes no carry
;
;
; Bad Message
;
LXI H,NACKMG ;send nack
SHLD XMTMCB+MCB.BUF
;
GDBUF: JMP SNDREQ ;request to send again
;
;
; Good Message Received
;
; Then Send ACK
;
.CMRKT ;cancel mark time
LXI H,ACKMG ;acknowledge message
SHLD XMTMCB+MCB.BUF
;
.LINKW XMTCHL,XMTMCB
;send acknowledgement
LHLD RECMCB+MCB.BUF
;get message again
SHLD SFTMCB+MCB.BUF
;send received message
.WAITE EBG
.SEND SFTCHL, SFTMCB,EBG
;the message buffer must be
JMP COMTSK ;deallocated by the receiving task

```


tasks TA and TB are installed into one machine for initial testing of program logic and task interaction.

Task TA-----Software Channel-----Task TB
< Machine A >

After the proper functioning of tasks TA and TB have been verified in Machine A, a pair of hardware interfaces may be installed and linked together in Machine A.

Task TA-----Interrupt Channel-----Hardware Interface

< Machine A >

X

Task TB-----Interrupt Channel-----Hardware Interface

Network concepts are tested using the final hardware configuration on a single machine. This allows the interaction of tasks with hardware to be examined in an environment which is easy to test.

Finally, the two tasks, interrupt handlers, and hardware interfaces are installed in separate machines to create the desired network. The advantage of this staged approach to network creation is that there can be much better certainty of detecting significant programming errors before the two tasks are installed into a hardware environment which does not lend itself to straightforward testing.

Program Development for Microprocessor Networks

The abstraction of I/O handling in an interrupt channel provides several advantages. Since the details of I/O operations, as well as interactions with external devices such as other processors, are not visible at the task level, the task's only concern is to initiate channel operations based on predefined data structures and communication protocols. The I/O specifics and details of external interactions are handled by the interrupt handler routines. With the multiprocessor and distributed processing approach, the intelligence of handling the I/O operations is distributed between the interrupt handler and the external I/O processors. This level of I/O handling is also transparent to the task.

Implications of these considerations are two-fold. First, distribution of I/O processing intelligence between the main processor and the I/O processor is done at the interrupt handler level and not at the task level. Thus, organizing programs into tasks is not affected by the introduction of new intelligence at the I/O level.

Second, since the separation of application software into tasks is based on the function to be performed, it is natural to divide the system into separate subsystems of local processors in which each performs its own dedicated functions. Different tasks may eventually run on separate processors based on these dedicated functions. Since the interaction between tasks is made through the channel mechanism and the task operates on a virtual processor, the development of programs for these tasks is not hampered by eventual separation into multiprocessors.

Summary

In order to replace manual methods for such operations as process control and data management, industry has

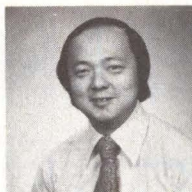
turned to computer technology. As the level of technology has increased, microprocessors have emerged as the system tools with the best combination of low cost and high performance. Taking this evolutionary process one step further, REX-80, designed as a microprocessor supplement, establishes the engineering disciplines that enable a microprocessor to process operations concurrently and thus utilize its full potential. However, the full utilization of microprocessing power can only be realized if proper management is imposed.

The realtime executive is organized into levels of management which direct system activities based on three primary abstractions—tasks, events, and channels. Tasks are independent modules that can be individually programmed or debugged before integration into the complete program. Events are stimuli that suspend or activate tasks in coordination with realtime constraints, and channels are the communication lines that bind the entire system together. The interactions of these abstractions provide the basis for all system activity. This fundamental organization expedites programming and debugging, and facilitates maximum resource utilization.

In terms of application usage, REX-80 is extremely flexible. By implementing macroinstructions to obtain system facilities, language difficulties are alleviated and future expansion is promoted. The system can be tailored to suit specific requirements since all tasks are designer defined. Also, since the executive can utilize the effects of transparency to allow a base microprocessor to be connected with other microprocessors, powerful multiprocessor organizations can be formed.

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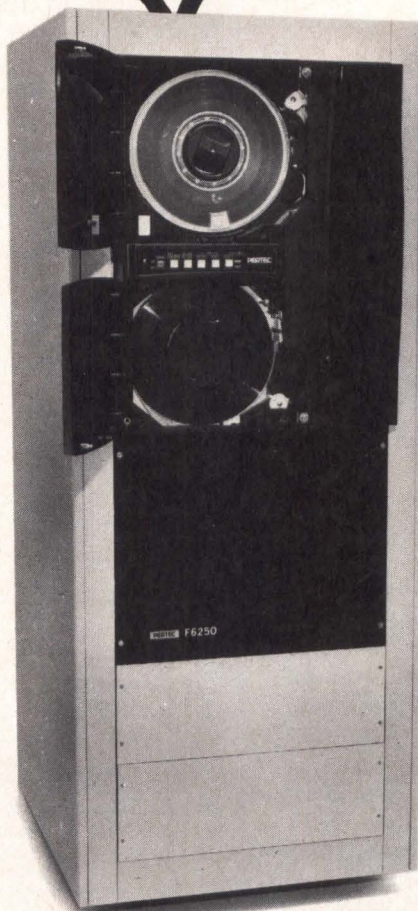
Dr Y. P. Chien obtained his PhD in Electrical Engineering from Purdue University and served as a professor in the Department of Information Engineering at the University of Illinois for five years. Responsible for the design and specifications of REX-80, he is currently general manager of Systems & Software, in charge of system development for realtime microprocessor applications.

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SEMICONDUCTOR MEMORY UPDATE—PART 2: RAMS

Levels of activity in random access memory technology—including bipolar, TTL, ECL, static and dynamic MOS, and C-, N-, and VMOS—disclose present capabilities as well as future trends

Eugene R. Hnatek Monolithic Memories, Incorporated, Sunnyvale, California

Part 1 of this 3-part article, published in December, detailed a comprehensive summary of state of the art read only memories. In a parallel approach this month, Part 2 continues the analysis of semiconductor memory technology by researching random access memories. Concluding the coverage, part 3, to appear in February, will investigate higher density memory techniques, such as charge-coupled devices, magnetic bubbles, Josephson junction, and gallium arsenide technologies.

A generalized scheme of depicting end equipment application versus the type of random access memory required encompasses the continuum from very high speed emitter-coupled logic scratchpad usage through the medium range mainframe and relatively slow microprocessor applications using metal oxide semiconductor random access memories. Each category contains overlapped areas of application where several technologies of random access memory may suffice (Table 1).

Bipolar RAMs

Bipolar random access memory (RAM) improvements are expanding continuously on two fronts—density (slowly) and speed (rapidly)—but not as rapidly as with MOS. Bipolar transistor-transistor logic (TTL) RAMs

using oxide-isolation technology in combination with various processing techniques provide high density, high speed writable stores for buffer, cache, and scratchpad memory applications. Shallow and controlled emitter-coupled logic (ECL) junctions provide even faster (7-ns) access times. Again as with bipolar programmable read only memories (P/ROMs), since newer high speed microprocessors are emerging, slow metal oxide semiconductor (MOS) RAMs can no longer be tolerated, nor can various functions such as refresh intervals be buried in microprocessor overhead without impairing system performance. High speed RAM is mandatory. At present, the Fairchild 93415A/93F415 1024 x 1-bit 30/20-ns RAMs and 93412/93422 256 x 4-bit 45-ns RAMs dominate. They use an oxide-isolation technique to obtain greater chip density and faster operating speed (lower address access time, T_{AA}).

TABLE 1
RAM Type Versus Application

Progressive Applications	Performance (T_{AA} in ns)	Type
Scratchpad	<50	Bipolar RAM (ECL/TTL)
Cache Memory*	20 to 80	Bipolar RAM, Static MOS RAM
Translated Buffer	20 to 80	Bipolar RAM, Static MOS RAM
Writable Control Stores	50 to 120	Bipolar RAM, Static MOS RAM
Large Mainframe	100 to 350	Dynamic MOS RAM, Bipolar RAM (ECL)
High Performance Medium Range Mainframe (VAX, Eclipse, HP3000)	200 to 500	Dynamic MOS RAM, Static MOS RAM
Minicomputer	100 to 250	Dynamic MOS RAM, Bipolar RAM
Microprocessor	200 to 500	Static MOS RAM, Dynamic MOS RAM

*Development of 32-bit CPU with high speed onchip cache will significantly decrease role of bipolar RAMs.

The transistorized flipflop forms the bipolar RAM cell, resulting in ultra high speed performance, larger die size (as compared with MOS), higher power supply current (I_{CC}), and higher cost. However, the Fairchild 93470/471/F471 4k isoplanar RAM represents the future technology trend. It has a smaller die size than competitive 4k dynamic n-channel MOS (NMOS) memories, thereby providing more die per wafer, higher yield, and lower unit cost than MOS devices (even though more masks are required). Performance characteristics are superior to those of the latest 4096-bit dynamic MOS RAM—the MK 4027: 30-ns T_{AA} and 850-mW power dissipation for the 93470/471 versus 120 ns and 462 mW for the MK 4027-1.

Static NMOS RAMs, however, are making a direct attack on the domain of bipolar RAMs, which covers high speed cache and scratchpad applications. Devices, such as the Intel 2115H 1024 x 1-bit static NMOS RAM with maximum T_{AA} of 20 ns and power dissipation of 656 mW, the Intel 2147H 4k x 1-bit static NMOS RAM with maximum T_{AA} of 35 ns and power dissipation of 990 mW, and the Intel 2148H 1k x 4-bit static NMOS RAM with maximum T_{AA} of 55 ns and power dissipation of 825 mW, provide stiff competition and should push the performance level of a 4k NMOS RAM to 25 ns by the end of 1980. Bipolar TTL RAMs have almost reached their speed plateau of about 20 to 25 ns. They can barely keep pace with scaled MOS.

These performance achievements on the part of NMOS static RAMs lead to the conclusion that NMOS will dominate at densities of 4k and greater while ECL will lead very high speed applications. This conclusion is substantiated because Fairchild was the only semiconductor manufacturer up until now working on dense bipolar RAMs, although with difficulty. The 4k 93470/71

and 93481 were introduced over two years ago and still are not readily available. The 16k 93483 has been discussed for almost as long without tangible results. Apparently these parts are not a production reality. The part number has been changed to 93480 as well. Whether or not these products will be abandoned remains to be seen. However, without a second source, the chances of success, apart from a producible process, are indeed slim. If TTL RAMs are to survive, the 16k level will be the deciding factor, and Motorola is working on a 16k TTL RAM. Because of these conditions, the main thrust of bipolar RAM manufacturers has focused on the super high speed arena of ECL designs. This is the future of bipolar RAMs.

ECL is a circuit design technique, not a process technology. A transistorized flipflop similar to that of a TTL RAM forms the basic ECL RAM cell. Consequently, many TTL RAMs (and P/ROMs) have internal ECL arrays to obtain circuit speed objectives; they use an ECL to TTL level translator on outputs and a TTL to ECL level translator on inputs such that the device looks like a TTL circuit.

Several years ago, ECL usage was hard to justify because, although it was faster than TTL, its increased speed on an incremental level did not adequately affect development cost. With the emergence of ECL gate arrays and bit slice circuits, system speed became very impressive. ECL RAMs continue to be used in speed intensive cache, buffer memory, and valuable control store applications, in conjunction with faster ECL mainframe memory controllers and with 16-bit bipolar microprocessors, such as the 100-ns Am29116. Consequently, there is increased activity in the design of ECL RAMs by National Semiconductor, Motorola, Signetics, Fujitsu, and Fairchild, as well as in the support of next genera-

TABLE 2
Typical Available TTL RAMs

Manufacturer	Part No	Organization	T _{AA} (ns max)	P _{DISS} (mW)	Pins	Outputs
National Semiconductor	85S68	16 x 4	40	500	16	Edge triggered
Advanced Micro Devices (AMD)	27S02A/S03A†	16 x 4	25	500	16	TS*, OC**
TI	SN74S189/289	16 x 4	35	525	16	TS, OC
TI	SN74LS216/316	64 x 4	N/A	N/A	16	TS, OC Common I/O
TI	SN74LS217/317	64 x 4	N/A	N/A	20	TS, OC Sep I/O
TI	SN74LS218/318	32 x 8	N/A	N/A	20	TS, OC Common I/O
Signetics	82S09	64 x 9	45	1000	28	OC
Fairchild	93419/A	64 x 9	30, 45	750	28	OC
TI	SN74S200A/300A†	256 x 1	30	500	16	TS, OC
TI	SN74S202/S302†	256 x 1	65	100	16	TS, OC
Fairchild	93410/410A	256 x 1	45, 60, 70	675, 700	16	TS
Signetics	82S16/116/ 17/117	256 x 1	40	600	16	TS, OC
Fairchild	93412/422†	256 x 4	45	675	22	TS, OC
TI	SN74S207/208†	256 x 4	40	600	16/20	TS, OC Edge triggered
AMD	27S207/208†	256 x 4	40	600	16	TS, OC
Fairchild	93F415/425†	1024 x 1	20, 35	600	16	TS, OC
Signetics	82LS10/LS11	1024 x 1	45	400	16	TS, OC
Hitachi	HM2510/11	1024 x 1	35, 60, 70	512	16	TS, OC
Fairchild	93475	1024 x 4	45	900	18	TS
Signetics	82S208/82S210	256 x 8	55	675	22/24	TS
Fairchild	93477/478	256 x 8	45	900	22	TS, OC
Signetics	82S212	256 x 9	45	675	24	TS
Fairchild	93478/93479	256 x 9	55, 45	900	24	TS, OC
Fairchild	93470/471/F471	4096 x 1	30, 35, 45	850	18	TS, OC
Fairchild	93L471	4096 x 1	45/60	472	18	TS
TI	74S400/401†	4096 x 1	75	500	18	TS, OC
Signetics	82S400/401	4096 x 1	45	675	18	TS, OC
Fairchild	93480	16384 x 1	45	700	16	TS

Notes:

All RAMs have a single 5-V power supply.

†Available in low power versions as well

*TS—3-State Outputs

**OC—Open Collector Outputs

N/A—Not available

tion computer developments of Burroughs, NCR, Amdahl, Univac, and CDC.

ECL RAMs lead in performance with 1k devices having 10-ns maximum T_{AA}, and 1k x 4- and 4k x 1-bit devices having 25-ns maximum T_{AA}. Their speed, however, is not without penalty. ECL dissipates a large amount of power. By 1982 to 1983, the speed for a 1k ECL RAM is projected at 2 to 5 ns, and for a 4k ECL RAM, 10 to 15 ns. Improved ECL RAMs should appear shortly.

Also, MOS manufacturers should be building ECL compatible MOS RAMs in the future. Tables 2 and 3 summarize the commercially available TTL and ECL bipolar RAMs, according to memory organization, maximum access time, and power supply current. The future of bipolar RAMs lies with ECL, which will be used extensively in super computers. Static MOS RAMs and lack of second sources have brought the virtual termination of dense bipolar TTL RAMs.

TABLE 3
ECL Random Access Memories

Manufacturer	Part No	Organization	T _{AA} (ns max)	P _{DISS} (mW)	Package (DIP)
Motorola	MCM10148	64 x 1	15	546	16
Motorola	MCM10145	16 x 4	15	676	16
Motorola	MCM10147	128 x 1	15	520	16
Fujitsu	MBM7047	128 x 1	12, 14	520	16
Fairchild	F10405	128 x 1	15	676	16
Fujitsu	MBM10410	256 x 1	35	680	16
Fairchild	F10410	256 x 1	30	676	16
Fujitsu	MBM7042	256 x 1	15	750	16
Motorola	MCM10152	256 x 1	15	702	16
Motorola	MCM10144	256 x 1	26	702	16
Fairchild	F100414/10414	256 x 1	10	728	16
National Semiconductor	DM10414	256 x 1	10	460	16
Hitachi	HM2106	256 x 1	15	460	16
Siemens	GXB100473	256 x 1	8	691	16
Fairchild	F10415/A	1024 x 1	20, 30	780	16
Fujitsu	MBM10415A	1024 x 1	20	780	16
Fairchild	F100415A	1024 x 1	10, 20	780	16
Hitachi	HM2110	1024 x 1	20, 25, 35	512	16
Hitachi	HM2112	1024 x 1	7	820	16
Motorola	MCM10146	1024 x 1	29	755	16
Fujitsu	MBM7071/72	256 x 4	15	1000	24/22
National Semiconductor	DM100422	256 x 4	10	1000	16
Fairchild	F100422/10422	256 x 4	10	936	16
Hitachi	HM2120	256 x 4	10	1040	16
Fairchild	F100470/10470	4096 x 1	35	936	16
National Semiconductor	DM10470	4096 x 1	35	1000	16
Hitachi	N/A	4096 x 1	25 (typ)	N/A	16
Fairchild	F100474	1024 x 4	25	900	22
Fujitsu	MB10474	1024 x 4	25	900	22
Siemens	GXB100475	1024 x 4	25	819	22
Fairchild	F10480/100480	16,384 x 1	35	936	16

Notes:

All devices have -5.2-V power supplies.
All devices have ECL outputs (open emitter).
N/A—Not available

MOS RAMs

The level of activity in MOS RAMs is proceeding rapidly in scattered directions. Consequently, it is difficult to summarize the salient facts. Both static and dynamic MOS RAMs have access times that overlap those of bipolar RAMs, even rivaling those of the Fairchild 93415A/425A/F415 RAMs, but with lower power drain. Dynamic MOS RAMs are used in peripherals and buffers, as well as in small and large mainframe computers. Static and

dynamic MOS RAMs are suited to applications in which power is at a premium, such as battery powered portable equipment and small terminals.

New high speed static RAMs are being used in traditional bipolar RAM applications such as cache and writable control stores. Static memories are internally regenerative; they are designed to protect against false or ambiguous operation and are faster than dynamic RAMs. In addition, they do not require refresh circuitry, are less subject to noise generated by current surges during ad-

dressings, and require less interface and support circuits. Dynamic memories are denser than static and require refreshing at periodic intervals, but they generally cost less, are simpler, and need less silicon. Moreover, less standby power is necessary. However, dynamic and static RAM designs are merging. With the redesigned 16k and the new 64k dynamic RAMs, both static and dynamic RAMs operate from a single 5-V power supply, require low standby power, and to an extent are becoming byte organized.

Profound advances in MOS RAM circuits since the acceptance of the 4k RAM in 1974 have met the density and performance requirements of the first 16k dynamic RAMs, anticipated 64k dynamic RAMs, and performance objectives of static RAMs. In static MOS RAM cells, information is stored in a bistable flipflop (as with bipolar RAMs), whereas, for a dynamic MOS RAM, it is stored as an electrical charge in a capacitor of a single transistor cell.

Evolution of smaller memory array cell sizes and thus smaller chips and higher density RAMs, in which the 3-transistor 1k RAM cell gave way to the 3-transistor 4k RAM cell, led ultimately to the 1-transistor 16k RAM cell. From a schematic viewpoint, however, this reduction in memory topology occurred concurrently with a further reduction in cell size by going from a single-level poly interconnect layer to a dual poly layer (Fig 1).

The 64k RAM combines a single transistor cell with double-level polysilicon and scaled NMOS technologies, resulting in a storage cell area one-half that of the 16k RAM. Furthermore, the 64k RAM utilizes thinner gate oxide, more compact layout (due to a single 5-V supply), and has a bit line capacitance reduction of 30%. Several innovative techniques for reducing cell size still further are shown in Figs 2 and 3. Fig 2 depicts the new taper isolated cell developed by Texas Instruments (TI), in which the storage capacitor has been eliminated. This cell stores charges within two regions of the transistor (physically located directly underneath the gate at the silicon surface) rather than in a capacitor. Presence or absence of charge (holes) determines whether or not the transistor has a high or low threshold voltage. The taper isolated cell is easy to fabricate since it requires only a single layer of polysilicon, as opposed to two or three for conventional RAMs. However, this concept has yet to be put into practical use; its real impact should be realized with the 256k RAM.

Fig 3 depicts the memory cell used in the National Semiconductor 64k RAM—dubbed the triple poly cell interconnect structure. Two polysilicon plates (poly 1 and poly 2), separated by a thin dielectric layer, form the memory capacitor. The transfer switch is a single poly device (poly 3), which is self-aligned. The drain of this device is connected to the poly 1 plate of the capacitor by a buried contact, the source is connected to the metal bit line by a conventional contact, and the poly 2 plate is grounded. One major advantage of this cell is the storage medium, which is a high quality capacitor. Only one-fifth of the total area of the storage node is subject to substrate leakage. This provides not only improved refresh characteristics over an equivalent sized inversion capacitor, but also a high degree

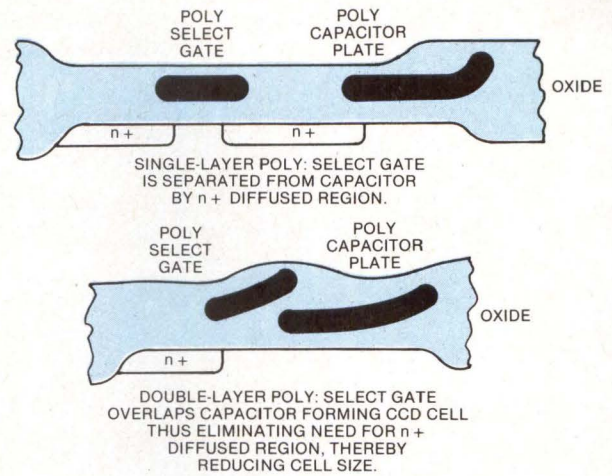


Fig 1 MOS interconnect evolution. One-transistor cells are located in single- and double-layer poly. Notice reduction in internal dimensions in going from single-layer polysilicon interconnect to dual layer

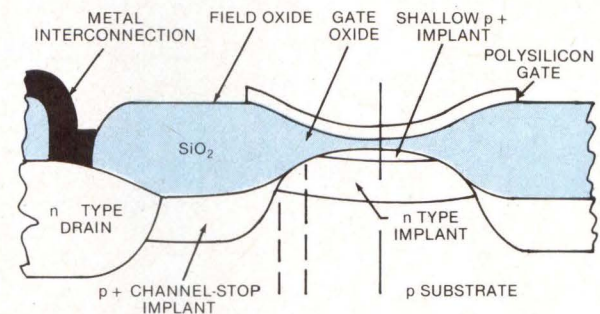


Fig 2 TI taper isolated dynamic RAM cell. This cell holds potential for 256k RAMs. In this configuration, storage capacitor has been eliminated, reducing memory cell size even further

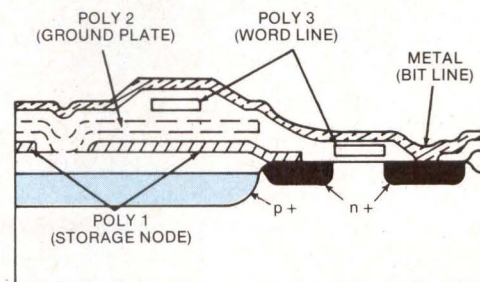


Fig 3 National Semiconductor triple poly storage cell (195 μm²). Cell is used on 64k RAMs. This development decreases memory cell size, improves refreshing, and increases immunity to soft errors

TABLE 4
Memory Cell Size Evolution

Bipolar		MOS	
Development	Cell Size (mil ²)	Development	Cell Size (mil ²)
Schottky TTL (6T to 8T*)	30	PMOS 3T*	2.15
Oxide isolation	11	NMOS 3T	1.70
Walled emitter oxide isolation	3	NMOS 1T, single-layer polysilicon	1.008 (MK 4027)
Shrink	2.3 (93415A)	NMOS 1T, dual-layer polysilicon	0.55 to 0.697 (MK 4116)
Merged transistor cell (2T)	0.68	NMOS 1T, triple-layer polysilicon	195 μm ²

*T—Transistor(s)

TABLE 5
Typical 16k Dynamic RAMs

Manufacturer	Part No	Org	Pins	Power Supplies (V)	Access Time (ns)	P _{DISS} (mW) (Operating/Standby)
Mostek	MK 4116	16k x 1	16	±5, 12	150, 200, 250	462/20
Hitachi	HM4716	↓	16	±5, 12	120, 150, 200, 250	462
National Semiconductor	MM5290		16	±5, 12	150, 200, 250	40 mA
Advanced Memory Systems	4116		16	±5, 12	150, 200, 250	550/27
Motorola	MCM4116		16	±5, 12	150, 200, 250, 300	462/20
Toshiba	TMM416		16	±5, 12	250, 350	N/A
TI	TMS4116		16	±5, 12	150, 200, 250	462/20
Intel	2117		16	±5, 12	150, 200, 250	462/20
Hitachi	HM4816		16	5	100	440
Motorola	MCM4516		16	5	120	200/20
National Semiconductor	MM5295		16	5	150, 200, 250	150/30 mA
Mostek	MK 4516	16k x 1	16	5	80, 100, 120	140/10
Mostek	MK 4816*	2k x 8	28	5	150, 200, 250, 300	150/25
Intel	2118	↓	16	5	80, 100, 120, 150	Latched output 157, 137, 121 mA/(22 mW)

Notes:

All manufacturers for the 16k x 1 RAM have adopted and changed to the unlatched output structure as the industry standard.
N/A—Not available
*Pseudostatic RAM with onchip refresh

of immunity to soft errors caused by high ionizing particles. More efficient utilization of the cell area is the second advantage, since the space separating the capacitors can accommodate the transfer switch.

The dramatic change in memory storage cells over the past five to six years is summarized in Table 4, which compares memory cell development for both bipolar and MOS RAMs. Reduced die size (higher density) and increased performance are accomplished by device scaling. Applicable to both bipolar and MOS integrated circuits, this method reduces all physical dimensions (horizontal and vertical) and operating voltages by a

scaling factor. The resulting RAMs have shorter access times (such as the Intel 2115H and 2147H), lower power dissipation, and less chip area, producing more die per wafer and lower cost. On the other hand, device scaling increases the number of masks used (and thus device cost), requires extremely low fabrication defect density, and pushes current photolithographic and process limits. Device scaling is denoted commercially by processes such as HMOS, HMOS II, XMOS, SMOS, and Poly 5. All MOS RAM manufacturers use scaling to optimize device performance and yield. Decreasing device geometries promise improved speed-power product with

some devices concentrating on higher speed and others emphasizing ultra low power.

Dynamic MOS RAMs

Dynamic 4k RAMs were the first semiconductor memory to provide a cost-effective solution to main memory and data intense (4k- to 6k-byte) applications. Initially, industry confusion existed because of the promulgation of different package types and pinouts, as each integrated circuit manufacturer attempted to have its 4k RAM accepted as the standard. Further confusion resulted when the focus changed from 4k to 16k dynamic RAMs before volume production of 4k units was even achieved, and just as most designers were incorporating them.

The 16k dynamic RAMs provide a further cost incentive for semiconductor main memory usage, with specifications comparable to those of 4k dynamic RAMs. Table 5 summarizes salient electrical characteristics of some common 16k dynamic NMOS RAMs. (For comparison, a listing of dynamic 4k NMOS RAMs can be found in "Current Semiconductor Memories" by Eugene Hnatek, *Computer Design*, Apr 1978, p 121.) Since only primary sources are listed, the information neither provides comprehensive data for all available memories nor lists all second sources. Manufacturers of 16k parts have all adopted the industry standard Mostek 16-pin dual-inline package (DIP), thus eliminating the confusion that existed with 4k parts. However, the 16k RAM did present some points of perplexity; those centered mainly on unlatched versus latched outputs, and refresh cycle times. Again, as with the 4k, the Mostek MK 4116 with unlatched outputs has emerged as the industry standard and is widely second-sourced.

A major milestone in increased data storage power is the 64k RAM. It is the precursor of increased computer performance in a smaller physical volume, at significantly lower cost. As such, it represents the start of a new cycle of memory product design. Emergence of the 64k RAM is due to advanced combinations of fabrication developments, specifically, projection versus contact printing, positive rather than negative photo resists, electron beam fabricated masks, and dry etch.

The 64k RAM will bridge the gap between large scale integration (LSI) and forthcoming very large scale inte-

gration (VLSI) designs. It will decline in cost faster than previous generation devices, while the cost per bit will actually be less than that of preceding generations. Systems costs will drop faster than the cost per bit despite the fourfold enhancement of bit density, because there is a factor of four fewer printed circuit boards required, fewer interface/buffer circuits, two-thirds the number of outboard capacitors, 50% decrease in power requirements, and two less power supplies, as well as increased reliability.

In large capacity memories, the per bit dissipation of power must be kept low in order to keep power supply, as well as cooling requirements, within limits. It is essential that the memory element dissipate very little power when not being accessed, since the majority of devices in large memories are on standby most of the time. The dynamic RAM is well suited to these conditions, since the ratio of active to standby power in most 4k dynamic RAMs is about 20 to 1. The curves of Fig 4 show the relationship of average per bit power dissipation as a factor of total memory size for 4k, 16k, and 64k RAMs. Furthermore, there has been very little increase in package power with increase in bit density. Power per array board has remained about the same whether populated with 4k or 16k RAMs, although the bit capacity is increased by four when using 16k RAMs. The transition to 64k RAMs promises even greater reduction in power, since reduced geometries and lower drain voltage will result in a substantial reduction in package power. Lower power should also increase device reliability. Dynamic MOS RAMs provide more capability per dollar mainly because fewer interconnections are required for a given function. The 64k dynamic RAM is an optimized LSI part for interconnections, and microprocessor family design should use these concepts for optimum system cost-effectiveness.

A 64k RAM was announced by TI in 1978, and pre-production was scheduled for the first half of 1979. However, devices did not materialize in time. Because of increased requirements for data storage and new applications, as well as the uncertainty of the producibility of the 64k RAM, demand for both 4k and 16k dynamic RAMs has exceeded expectations and continues to be strong. In addition, for applications that require higher density than 16k and because of the unavailability of 64k RAMs, several manufacturers have introduced 32k dynamic RAMs (Table 6), which encased two 16k RAMs in an 18-pin DIP.

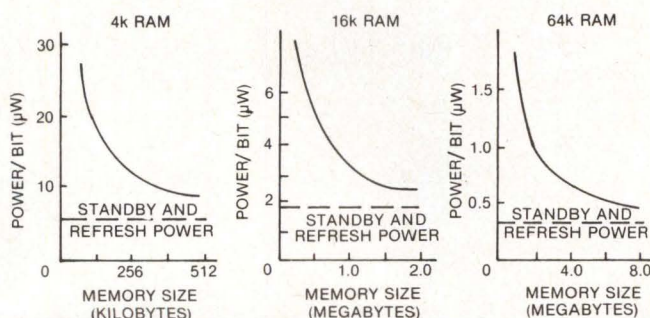


Fig 4 Power/bit vs memory size. Conditions include four bytes/word, one word active at all times, and 2-ms refresh. Comparison of memory system power dissipation on per bit basis shows exponential type drop as function of system size for 4k, 16k, and 64k dynamic RAMs

The life span of 16k dynamic RAMs is being extended by semiconductor manufacturers because of several factors: (1) the immense technical challenges of the 64k RAM, which require new manufacturing techniques, new fabrication facilities, and lack of overall fabrication capacity; (2) the emergence of a single 5-V high speed (100-ns) 16k dynamic RAM to enhance system throughput; (3) increased memory usage due to storage consuming high level languages; and (4) applications in intelligent terminals, personal and small business computers, and new microprocessor based systems, which require 5-V only operation but do not need 64k bits per chip. The single-supply (5-V) 16k RAM represents an upgrade and a bridge between the current generation 3-power supply 16k RAM and the 64k RAM. Both designers and manufacturers will use the 5-V 16k RAM to get ready for the 64k RAM.

Because of fabrication process and circuit design problems with the 64k RAM, limited samples will probably not appear until the last quarter of 1979 and the first quarter of 1980, with a buildup of production quantities occurring in the last half of 1980. However, even though encased in a standard 16-pin DIP, the 64k RAM is not without standardization problems. These include single- vs multiple-power supplies; no connection vs a power supply pin vs a special function on pin 1; and 128- vs 256-cycle refresh. Again, a shakeout will occur as to which manufacturer's version will become the established industry standard 64k RAM. Salient performance characteristics of announced 64k RAMs are listed in Table 7.

Once an industry standard is selected, the electrical performance parameters will be greatly refined (80-ns T_{AA} and 150-mW max P_{DISS}). Originally, dynamic RAMs

TABLE 6
Available 32k Dynamic RAMs

Manufacturer	Part No	Org	T_{AA} (ns)	P_{DISS} (mW) (Operating/Standby)	Power Supplies (V)	Pins
Mostek	MK 4332	32k x 1	200	482/40	12, \pm 5	18
TI	TMS4132	32k x 1	150/200/250	380/18	12, \pm 5	18

TABLE 7
Typical 64k RAMs (65,536 x 1 Bits)

Manufacturer	Part No	Chip Size (mil ²)	T_{AA} (ns max)	P_{DISS} (mW)	Power Supplies (V)	Refresh	DIP Package And Pins
IBM*	Not commercially available	62,500	300	360	8.5 3.5 -2.2	128 cycles 2 ms	Special (nonstandard) 40
Mostek	MK 4164	35,000	120	300	5	128 cycles 2 ms	Standard 16
TI	TMS4164	33,000	100, 150	200	5	256 cycles 4 ms	Standard 16
Motorola	MCM6664	37,700	150 200	250/30	5	128 cycles 2 ms	Standard 16
Fujitsu	MB8164	48,000	120 150 200	385	7 -2.5	128 cycles 2 ms	Modified 16
National Semiconductor	MM5264	37,200	150, 200, 250	200	5	256 cycles 4 ms	Standard 16
Intel	2164	43,000	150 200	330	5	128 cycles 2 ms	Standard 16
Hitachi	HM4864	48,000	120	300	5	128 cycles 2 ms	Standard 18
NEC	N/A	52,000	510 (typ)	400	5	128 cycles 2 ms	Standard 16
Toshiba	N/A	40,000	N/A	N/A	8, -2	N/A	16
Siemens	N/A	35,000	N/A	N/A	8, -2	N/A	16
Mitsubishi	M58746S	41,648	120	200/22	5	256 cycles 4 ms	Standard 16

Notes:

*Contains redundant onchip array and peripheral circuitry.

N/A—Not available

Different options for pin 1 are:

National Semiconductor, TI, Intel, Hitachi, Toshiba, and Mitsubishi—No connection

Mostek—Refresh control function

Motorola—Automatic refresh control

Fujitsu—Power supply

were primarily used for minicomputer and mainframe bulk storage applications, thus the proliferation of x1-bit organizations. This allowed large computers to utilize the word depth possible with an x1-bit organization. However, x4- and x8-bit organizations are possible with dynamic RAMs and will be offered shortly (2k x 8, 8k x 8, and 16k x 4).

The 256k dynamic RAM will require new production techniques (such as electron beam masks), as well as either modified or new fabrication processes and circuit design innovations, such as the TI taper isolated cell. Preproduction samples of the 256k RAM should be available in the 1983 to 1984 time frame. Depending upon availability, the 256k RAM could cause the demise of charge-coupled devices. The 256k RAM will further increase computing power and will significantly impact medium performance large computers.

Static MOS RAMs

Amidst the developments in dynamic NMOS RAMs, significant achievements are appearing in NMOS and complementary MOS (CMOS) static RAMs, with an inherent speed edge over dynamic devices. Static RAMs are now pressing dynamic RAMs in the area of power dissipation; various power-down techniques such as power gating, edge activation, and address activation have made this possible.

Static MOS RAMs possess impressive performance specifications and are available in both byte-wide and non-byte organizations. However, the density of dynamic RAMs is greater by a factor of 4. Scaled high performance NMOS and CMOS technologies are providing very high speed RAMs, which are attacking the domain of

bipolar RAMs; high speed cache and scratchpad applications are led by the Intel 2115H 1k static RAM and the 4k 2147H and 4148 static RAMs.

The variety of static RAMs becoming available is staggering. Examples of the increased design activity are displayed in Tables 8, 9, 10, 11, and 12. The future will portend both 32k (4k x 8 and 8k x 4) and 64k (16k x 4 and 8k x 8) static RAMs with access times of 60 to 70 ns max, utilizing a variety of power-down modes. Mostek's 4864 pseudostatic 8k x 8-bit RAM should be available for sampling sometime in 1980. Both static and bipolar RAMs are also expected to be available in x9 organizations. This ninth or extra bit is a parity bit used to detect an error in the first eight bits of the word.

Use of CMOS technology for memory fabrication is increasing due to the greater demand for energy conservation. Low power is certainly important, but CMOS has outgrown this sole characteristic; its complementary nature holds the promise of its becoming the fastest technology. As such, the speed, density, and cost of CMOS memories is approaching that of the static NMOS counterparts due to process and circuit design advances now possible only with CMOS; many circuit components can be eliminated by using the parasitic capacitance and overdrive characteristics of digital CMOS circuits properly during chip design. The cost differential between NMOS and CMOS is disappearing with the number of masks used to fabricate scaled NMOS approaching and equaling the number of masks used to fabricate CMOS. The true growth and application of CMOS technology is in LSI circuits. Consequently, the development of CMOS memories (RAM and EPROM) is proceeding at a hectic pace. Table 13 presents a sampling of available CMOS RAMs.

TABLE 8
4k (4k x 1) NMOS Static RAMs

Manufacturer	Part No	T _{AA} (ns max)	P _{DISS} (mW)	Power Supplies (V)	Pins
Motorola	MCM2147	55, 70, 85, 100	180, 170, 140, 130 120, 110/30, 25, 20	5	18
Intel	I2147/H	35, 45, 55, 70	990, 880, 770/ 165, 110, 165	5	18
Intel	I2141	120 to 250	385 to 220/110 to 28	5	18
Mostek	MK 4104	125, 200, 250, 300, 350	150/28	5	18
TI	TMS4044	150, 200, 250, 450	440/156	5	18
TI	TMS40L44	200, 250, 450	275/96	5	18
TI	TMS4046	150, 200, 250, 450	440/13	5	20
TI	TMS40L46	200, 250, 450	275/13	5	20
TI	TMS4244	120	300/50	5	18
Motorola	MCM6641/ 66L41	200, 250, 300, 450	500/385; 225/150	5	18
Hitachi	HM4847	45, 55, 70	945, 893, 840	5	18

TABLE 9
Available 4k (1k x 4) NMOS Static RAMs

Manufacturer	Part No	T _{AA} (ns max)	P _{DISS} (mW)	Power Supplies (V)	Pins
Intel	N/A	200	30mW/40μW	5	N/A ¹
Intel	I2148/H	45, 55, 70, 85	800/150	5	18
Intel	I2114/A	120, 150, 200, 250, 300, 450	200, 350, 370	5	18
Intel	I2149H ²	45, 55	900	5	18
AMD	9130	200, 300, 400, 500	710	5	22
AMD	91L30	200, 300, 400, 500	350	5	22
AMD	9135	80 to 150	750	5	18
TI	TMS4045	150, 200, 250, 450	550/170	5	18
TI	TMS40L45	200, 250, 450	330/110	5	18
TI	TMS4047	150, 200, 250, 450	550/13	5	20
TI	TMS40L47	200, 250, 450	330/13	5	20
TI	TMS4245	120	350/70	5	18 ³
Hitachi	HM472114	200, 300, 450	330	5	18 ⁴
National Semiconductor	MM5255	250	400	5	18 ⁵
National Semiconductor	MM5256	250	400	5	22
Intel	I2142	200, 300, 450	525, 375	5	20
AMD	AM9124/91L24	200, 300	350/250	5	18 ⁴
EMM	SEMI2114/ L2114/S2114	200, 300, 450	500/350/200	5	18 ⁴

Notes:

N/A—Not available

¹Experimental

²Same as I2148 but with CS and without power-down mode

³Contains chip enable (CE)

⁴114 equivalent

⁵Common I/O

TABLE 10
Typical 8k Static and Dynamic RAMs

Manufacturer	Part No	Type	Org	T _{AA} (ns max)	P _{DISS} (mW)	Power Supplies (V)	Pins
Intel	I8185	Static	1k x 8	200, 300	N/A	5	18
Mostek	MK 4118*	Static	1k x 8	120, 150, 200, 250	420/315	5	24
Mostek	MK 4801	Static	1k x 8	55, 70, 90	656	5	24
Mostek	MK 4808/09	Pseudo- static	1k x 8	150, 200, 250, 300	150/25	5	28
NEC	UPD421	Static	1k x 8	85	788/105	5	22
EMM	SEMI8108	Static	1k x 8	300	270/60	5	22
EMM	SEMI8118**	Static	1k x 8	300, 500	270/60	5	24
National Semiconductor	MM5298-2	Dynamic	8k x 1	150, 200, 250	200	±5, 12	N/A
Intel	2109	Dynamic	8k x 1	200, 250	462, 436/20	±5, 12	16

Notes:

N/A—Not available

*2716 EPROM/ROM pin compatible

**2708 EPROM/ROM pin compatible

TABLE 11
Representative 16k Static RAMs

Manufacturer	Part No	Org	T _{AA} (ns, max)	P _{DISS} (mW)	Power Supplies (V)	Pins
TI	TMS4016	2k x 8	150, 200, 250	495	5	24*
Intel	I2167	16k x 1	45 (typ)	550/85	5	20
Mostek	MK 4802	2k x 8	N/A	N/A	N/A	N/A
Mostek	MK 4167	16k x 1	N/A	N/A	N/A	N/A
Intel	I2118	2k x 8	80, 100, 120	190, 120, 99	5	16
Mitsubishi	M58725	2k x 8	200	400/50	5	16
Matushita	N/A	2k x 8	100	725/150	5	N/A
Mostek	MK 4816**	2k x 8	150, 200, 250, 300	150 mA/25 mW	5	28

Notes:
N/A—Not available
*Pin compatible with 2516 EPROM
**Pseudostatic RAM with onchip refresh

TABLE 12
Typical Large Static RAMs

Manufacturer	Part No	Org	T _{AA} (ns)	P _{DISS} (mW) (Operating/Standby)	Power Supplies (V)	Pins
Zilog	Z6132	4k x 8	200	200/110	5	28
Zilog	Z6164	8k x 8	150	200/20	5	28
National Semiconductor	NMC4864	8k x 8	150	200/20	5	28
Mostek	MK 4864	8k x 8	150, 200, 250	N/A	5	28

Note:
N/A—Not available

At the 4096-bit level, CMOS low power and comparable speed versions of the industry standard NMOS static 2147 4k x 1 and 2114 1k x 4 RAMs are widely available from many sources. A 12k RAM (1k x 12), the 6312/12A, is available to support the 6100 12-bit microprocessor. At the 16,384-bit density level, RCA, Hitachi, Harris, and Toshiba are developing 2k x 8 RAMs. CMOS RAMs have speeds of 180 to 240 ns for 1k parts, 85 to 350 ns for 4k units, and 80 to 250 ns for 16k units; power consumption ranges from 250 μ W for RCA's CMOS/silicon-on-sapphire (SOS) 4k design to 175 mW for other units. (Note that even this high end power dissipation is lower than that which most dynamic RAMs or NMOS static devices can achieve.) However, speed and power consumption specifications for CMOS devices can be very misleading, because power consumption relates directly to device speed, which in turn relates directly to supply-voltage level. Some CMOS memories are designed for a single supply level—typically 5 V—with speed and power consumption optimized there. A wide power supply range, on the other hand, increases noise immunity, but compromises speed. The specification must therefore be reviewed carefully.

Key to CMOS development is SOS technology, which capitalizes on the advantages of CMOS while achieving the speed and density of NMOS. SOS technology which

solves the primary speed-limitation problem of CMOS was evolved mainly to reduce parasitic capacitance, thereby significantly increasing the speed of CMOS (by a factor of 3:1) while maintaining its low power benefits. CMOS circuits are fabricated in a thin silicon layer grown on a sapphire substrate. Being a nonconductive material, the sapphire virtually eliminates the problem of capacitance between the aluminized conductors and the substrate. The choice of sapphire as the nonconductor stems from two properties: first, large sapphire crystals can be grown, and more importantly, its thermal coefficient of expansion is virtually identical to that of silicon. If the thermal coefficients for the two materials were not matched, silicon circuits grown on sapphire would buckle and dislodge as the circuits heated. Circuit capacitance is further reduced through elimination of the large horizontal junction structures used in other fabrication technologies. In SOS, these are replaced by vertical junctions, diminishing junction capacitance.

A side benefit is the elimination of a processing problem that in other technologies causes chip failures. In SOS, as in other technologies, the aluminum interconnects run on top of an insulating layer of SiO₂. With SOS, a pinhole in the SiO₂ layer is usually not catastrophic, because below the SiO₂ is the insulating sap-

TABLE 13
CMOS RAMs

Manufacturer	Part No	Org	T _{AA} (ns)	P _{DISS} P _{stabv} (mW)	Single Power Supply (V)	Pins
National Semiconductor	MM54C/74C89	16 x 4	280 (10 V) 650 (5 V)	4.5	3 to 15	16
RCA	CD4061A	256 x 1	380 (10 V) 750 (5 V)	0.1 (10 V) 0.025 (5 V)	3 to 15	16
Motorola	MCM14552	256 x 1	3150, 6300	1.5	-0.5 to 18	24
National Semiconductor	MM54C/74C910	64 x 4	700	20	5	18
AMI	S2222/A	512 x 1	350, 700	25.0/0.002	10	16
Intersil	IM6508/18	1024 x 1	200 to 600	2.5 to 0.05	5	16/18
National Semiconductor	MM54C/74C929	1024 x 1	240, 315	20	5	16
National Semiconductor	MM54C/74C930	1024 x 1	240, 315	20	5	18
Intel	I5101	256 x 4	45 650 800	135, 110/ 0.075 135, 110/ 1.0, 0.075 150, 125/ 2.5, 0.25	5 5 5	22
Intersil	IM6551	256 x 4	180, 360	2.5/0.5	5	22
Harris	HM6551	256 x 4	215, 375	15	5	22
Intersil	IM6561	256 x 4	180, 360	2.5/0.5	5	18
Harris	HM6561	256 x 4	215, 375	15	5	18
Harris	HM6562	256 x 4	215, 375	15	5	16
National Semiconductor	MM54C/74C920	256 x 4	250, 325	20, 15	5	22
National Semiconductor	MM54C/74C921	256 x 4	250, 325	20, 15	5	18
Harris	HM6513	512 x 4	270, 320	30/MHz/ 50 μW, 5 mW	5	18
Harris	HM6503	2048 x 1	250, 300	20/MHz/ 50 μW, 5 mW	5	18
Harris	HM6504	4096 x 1	270, 330	0.03, 0.05	5	18
Intersil	IM6504	4096 x 1	150	100/≪≪1	5	18
Hitachi	HM6174P ¹	4096 x 1	55/70	75/10 μW	5	18
Harris	HM6514 ²	1024 x 4	270, 320	30/0.05, 2.5	5	18
RCA	MWS5114 ^{2,3}	1024 x 4	650	0.25	5	18
NEC	UPD444 ²	1024 x 4	200, 250 300, 450	210/262 μW	5	18
NEC	UPD445	1024 x 4	450, 650	150/210 μW	5	20
Harris	HM6533	1024 x 4	350	35/0.005	5	22
Hitachi	HM6148 ⁴	1024 x 4	55, 70	150/0.05	5	18
RCA	N/A ³	4096 x 4	80/150	14/0.005/0.05	5	22
Toshiba	TC5516P ⁵	2048 x 8	100	200/1	5	24
Harris	HM6516	2048 x 8	200	5	5	24
Hitachi	HM6116	2048 x 8	100, 120, 150	175/0.02	5	24

Notes:

All electrical parameters are guaranteed at 25 °C.

N/A—Not available

¹2147 CMOS equivalent

²2114 CMOS equivalent

³CMOS/SOS technology

⁴2148 CMOS equivalent

⁵Pin compatible with 2716 EPROM

phire; therefore, penetration does not result in a short circuit. In contrast, a pinhole in a nonsos device could cause a short circuit between the conductor and the underlying silicon layer, leading to device failure.

Packing density of CMOS/SOS devices is improved by a factor of 4:1 over bulk CMOS since the guard bands used in CMOS technology are eliminated in SOS devices. Processing steps of the simpler SOS structure are reduced by one third by virtue of the same reasoning, thereby cutting costs and increasing yield. Perhaps the only major disadvantage of SOS is its relatively complex processing and higher wafer cost, resulting in higher finished product cost. CMOS/SOS wafers are very expensive to produce using the basic silicon ingot growing techniques. A more promising technique presently undergoing examination is sapphire ribbon technology which produces square type wafers cut from a long drawn ribbon. RCA is attempting to significantly reduce sapphire ribbon costs by improving fabrication techniques.

CMOS/SOS has been faced with some obstacles that are only now being resolved. Despite apparent advantages of SOS technology, many years of research and development efforts by many companies failed to produce significant results until 1977 when Hewlett-Packard announced the development of a 16-bit single-chip microprocessor built with CMOS on sapphire. In production since that time, it is used in the HP300 small business system and the HP3000 series 33 computer. At present RCA's 4k x 1 MWS5114 and 1k x 4 CDP 1825 static RAMs are the only CMOS/SOS RAMs available.

All CMOS RAM manufacturers have initiated major projects with the aim of making their processes more competitive with both NMOS and SOS. First improvements from such firms as Harris, Intersil, and National Semiconductor will center on shrinking line widths from the current 7.5- μm standard to about 5 μm —a development that will halve the chip area and increase the speed by a factor of three. By mid-1980 many of these manufacturers will be using completely revamped CMOS processes that will push the performance of NMOS static RAMs.

Both NMOS and CMOS static RAMs allow easier interfacing and greater flexibility with microprocessor based systems. Future trends anticipate many 16k, as well as 8k (2k x 4 and 1k x 8), CMOS RAMs, emphasizing ultra low power consumption and access times of less than 100 ns.

VMOS ROMs and RAMs

Designers are utilizing VMOS technology to obtain high density and high performance in lower cost devices. VMOS is an NMOS logic structure integrated on a 3-dimensional surface, in which the transistor elements are arranged vertically up the sides of a V-shaped groove. Device speed for a VMOS device is maximized by the short channel length. VMOS cell size can be the same width as the connector lines to it, rather than larger, as in NMOS. The net result is a considerable increase in circuit density over both standard NMOS and bipolar technologies. VMOS can easily provide more circuits for a given chip area, or a smaller chip area

for a given circuit. Its density is increased because the n+ substrate also serves as the common source for all transistors, thereby eliminating the ground "lines" required on NMOS circuits. Consequently, the saving in surface area is substantial. Circuit density on such a chip exceeds that of any available or projected competing technology, primarily because of the added vertical dimension.

The problem with VMOS technology is that only AMI is producing commercially available VMOS memories (and not in large volumes). Even though TI has a technology exchange with AMI, they have yet to introduce a product. In fact, TI has recently revealed that they will use their scaled NMOS process (SMOS), rather than VMOS, to produce a fast 2147 4k static RAM, because VMOS represents a wide departure from current techniques. While the VMOS process allows for easier layout and final smaller die size than SMOS, the cost of setting up the new process is prohibitive at this time.

Up until October 1979, VMOS held the promise of furthering MOS's density/performance advantages for semiconductor memories with a "viable" alternative technology. However, AMI's October announcement that it was ceasing all VMOS memory efforts has just about finished VMOS memories. According to AMI sources, VMOS had much more limited application than originally thought and it moved too quickly from development to production without enough testing and failure analysis. This leaves Siemens AG as the only supplier using VMOS technology for memory fabrication: a 64k dynamic RAM. The VMOS process, due to its complexity, was more expensive than high performance NMOS, but had high yield and apparently could not be cost-effective when compared with NMOS and CMOS memory technologies. VMOS is a viable technology for power transistors. However, for all practical purposes, VMOS will remain as a research and development technology as far as memories are concerned.

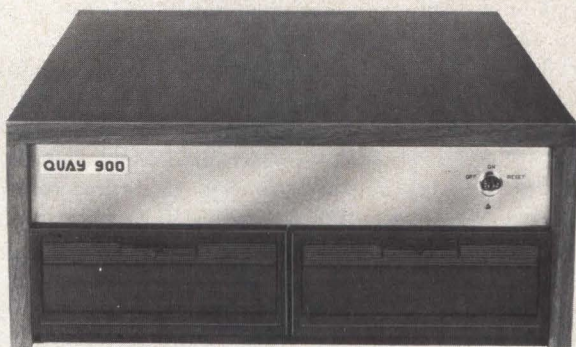
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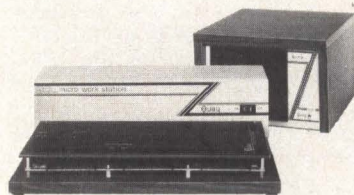
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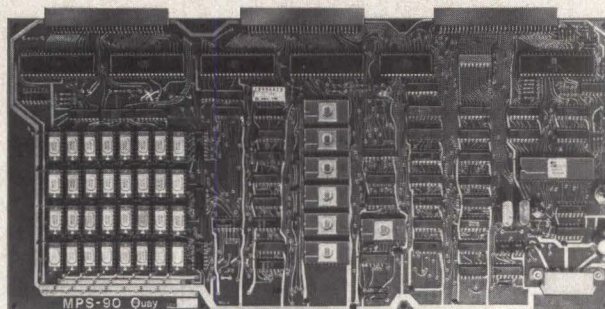
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CRT TERMINAL ARCHITECTURE PROVIDES COST-EFFECTIVE CUSTOMIZING VERSATILITY

A microprogrammable, bus oriented architecture and firmware control enable this CRT terminal to provide the flexibility and cost-effective features necessary to customize it for different system applications

Jerry Pisano and Robert Yablonski

EECO Incorporated, Santa Ana, California

For most CRT terminal applications, the term customizing generally implies a cosmetic process; the user's choice is limited to a specified cabinet color and label. However, the customizing process becomes quite intricate when the OEM system designer or user requires an array of special screen features, operating modes, and communications protocols. Proper architectural design of the terminal can greatly simplify and lower the cost of implementing such customizing requirements.

As an example, a microprogrammable bus oriented terminal provides maximum flexibility and capability. The one terminal, tailored to different applications, can eliminate the need to use a different terminal for each task. Use of microprocessor based programs (firmware) makes it relatively simple to add such CRT screen features as field limits and comparisons, must-fill fields, blinking, blanking, and half- and low-intensity. In addition, communications protocols can be tailored for emulation of any other terminal, or for the ability to

work with any host computer. Such operating modes as scrolling, paging, windowing, and polling are quickly accommodated.

Special keyboard layout is another area of customizing that is frequently required. When a microprocessor controlled keyboard is part of the intelligent terminal, virtually any key on the board can be specified to perform any function. A customized character font is often desired. A socket-mounted character generator read only memory (ROM) allows the user to change fonts by simply plugging in another ROM. Downline loading of character sets is also made possible by utilizing random access memory (RAM) storage.

Customizing Features

Flexibility of the microprogrammable architecture is related to the type of data transmitted by the terminal to

the host computer. If all characters displayed on the screen are transmitted simultaneously, communication lines could be overloaded. One solution to the problem would be to establish specific fields of data that are transmitted individually by depressing a key on the keyboard. Another method would be to send only alphabetic or numeric characters, whichever are appropriate. Regardless of the approach, control over the data transmitted to the host computer can be specified by firmware in the terminal. Polling is another customizing feature that illustrates the input/output (I/O) flexibility of this terminal design. Operating over a direct cable connection or a single modem, several terminals can be daisy chained using the auxiliary I/O port, thereby saving modem and line costs.

The capability to emulate another terminal is accomplished by customizing the protocol characteristics that include specific poll, specific select, fast select, and multipoint contention modes. Group poll and group select are also available as options. Five unique characters are used for terminal and group addresses, and all are switch-selectable in the field for operating and servicing convenience. Paging also demonstrates the flexible intelligence of this terminal. Paging control on the keyboard provides the ability to page backward or forward in predefined increments of 24 lines. When this is done, the line number may be displayed in the status line.

In a customized problem-solving mode, all characters entered from the keyboard as well as those received from the host computer, including control characters, can be displayed. Because no function character is op-

erated on while in this mode, commands like carriage return, line feed, blank screen and other terminal controls are displayed in their control code representation. Scrolling, a feature found in many intelligent terminals, is usually available only in the vertical screen dimension. However, the microprogrammable terminal can be customized to scroll horizontally as well. Another feature that can be implemented is windowing. This is usually associated with graphic displays that present only a portion of the entire picture on the screen. In this terminal, the windowing operation uses four cursor locations to specify points on the screen for the display of data contained only within this rectangle. In effect, this capability provides a "mini screen" that is totally independent of all other data on the display.

As well as facility in customizing, the inherent intelligence provides capability for standard features not found in all terminals. One of these is a flexible forms mode that can be used to duplicate printed forms, through the use of a variety of graphic characters. This can be used to display a "fill-in-the-blanks" format for data entry applications. Compared to the use of a nonintelligent terminal, a terminal with microprogrammable architecture unloads the host processor and allows each terminal in a distributed network to be customized individually. In practice this eliminates the need to interrupt operation of the host computer while terminal oriented software modifications are implemented.

Terminal Operation

Inherent design of this microprogrammable CRT terminal incorporates all of the customizing capability required for most applications. There are four main sections: bipolar central processing unit (CPU), program memory, I/O, and monitor control circuits (Fig 1).

Two 24-bit word structures are used in the CPU, (Fig 2). This structure allows parallel processing of all terminal functions for maximum throughput.

Of the two CPU buses (Fig 3), the A-bus multiplexes all I/O handled by the terminal. The 8-bit D-bus handles only internal data within the processor. Receiving data from the D-bus, the stack pointer addresses a pushup stack. The stack stores the return address for subroutine nesting as well as register data that must be saved during an interrupt. General purpose registers of the CPU can store 16 words of 8 bits each. These are under absolute program control and may be used for any purpose. Determining the data flow in the terminal, the arithmetic-logic unit (ALU) sends data to the D-bus through either the B-register or literal inputs from the control memory. The other ALU input is obtained from the A-bus data selector.

Condition output from the ALU and inputs from the control memory control the program counter. The program counter supplies the 12-bit control memory address that is divided into 8- and 4-bit segments and sent to the A-bus data selector. The program counter counts incrementally or jumps on command when the conditional word is used. Load strobes for all the D-bus registers are generated by the destination decoder. Receiving strobed inputs from the control memory, the destination decoder selects one of the operational registers as

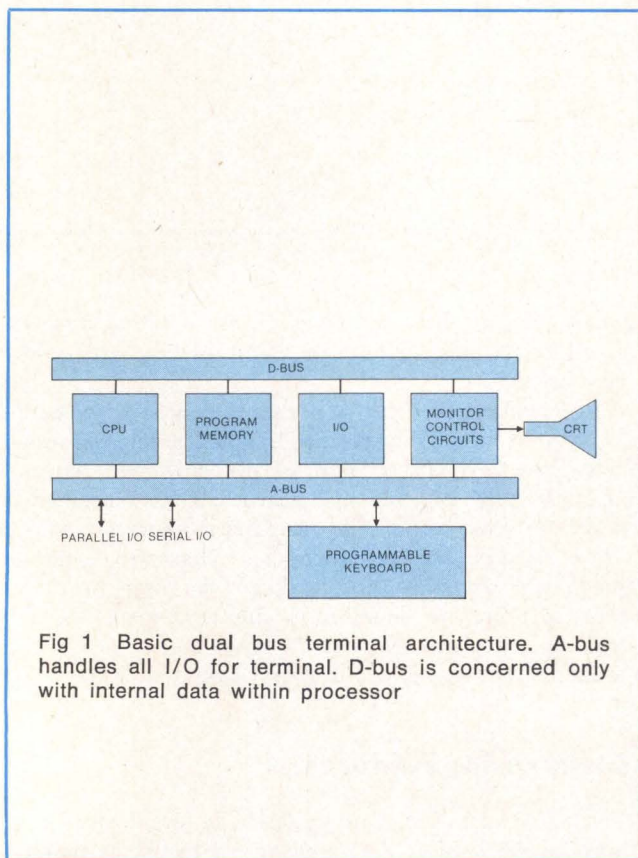


Fig 1 Basic dual bus terminal architecture. A-bus handles all I/O for terminal. D-bus is concerned only with internal data within processor

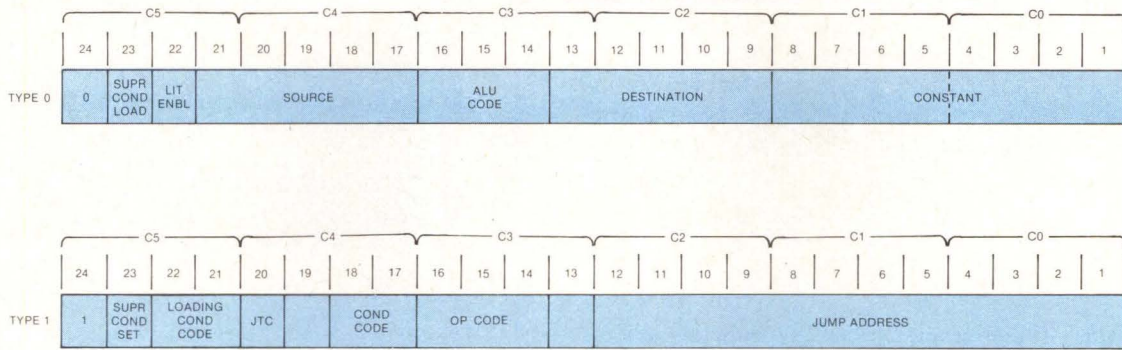


Fig 2 Terminal word organization. In type 0 word, bits 1 through 8 are constant; 9 through 13, destination; 14 through 16 are ALU code; 17 through 21, source; 22, literal enable; 23, suppress condition load; and bit 24 is 0. In type 1 word, bits 1 through 12 are jump address; 13, not used; 14 through 16, opcode; 17 and 18, condition code; 19, not used; 20, jump on carry; 21 and 22 are loading condition code; 23, suppress condition set; and bit 24 is 1

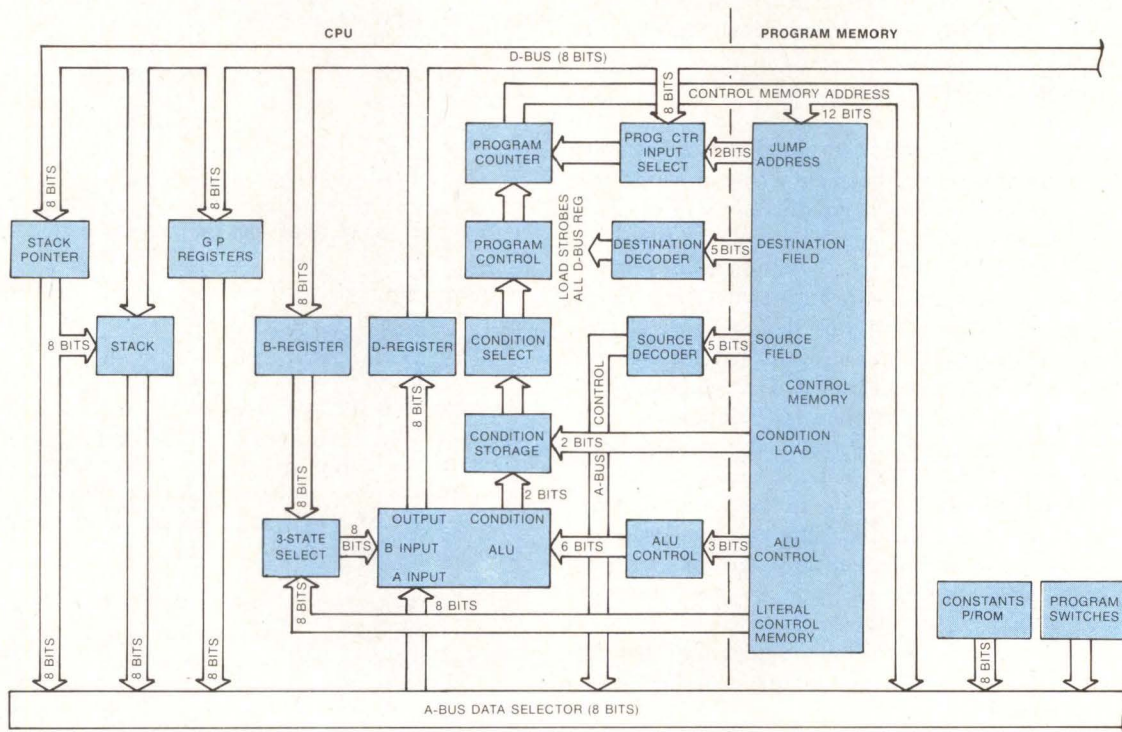


Fig 3 Terminal CPU and program memory organization. CPU employs fast bipolar circuitry and two 24-bit word structures. Firmware used for terminal customization resides in microprogrammable control memory

the destination register. Based on five control memory bits, the source decoder decides which source is to supply data to the A-bus. It then enables one of the 16 possible 8-bit sources to be multiplexed on the A-bus. Firmware in P/ROM and manually settable switches make up the program memory section; it controls the terminal attributes, operating modes, and I/O.

Control Memory

This portion of the program memory contains micro-instructions that control the internal program and is the key to the terminal's ability to be easily customized. The control memory typically contains 0.5k words of P/ROM, which can be expanded to 1.5k words. Since the word length is 24 bits, three 8-bit, 0.5k P/ROMs make up the typical configuration. Expansion is obtained through use of six IC sockets that can accept similar P/ROMs. A simple modification can expand the control memory to 4k words.

Customizing a specific terminal is achieved by inserting the appropriate instructions into control memory firmware. Depending on the word format, the control memory, in association with hardware registers, controls specific functions within the terminal. These functions include serial I/O communications, printer operation, video blanking, audible alarm, cursor position, and parallel and auxiliary I/O ports. In addition, the control memory is used to control the stack pointer, general purpose registers, refresh memory, and destination register.

Communications protocols for terminal emulation and host computer interfaces can be handled by a combination of firmware and hardware modifications. Terminal emulation is accomplished by control memory firmware. Operation with a specific computer is obtained by simply inserting the appropriate firmware into control memory; system architecture then establishes the required handshake routine. Polling discipline is achieved by control memory firmware and the addition of a plugin card. For bisync operation, firmware plus an additional card are required. Adequate space is provided for the insertion of additional cards. In all cases terminal architecture allows the different protocols to be implemented. Working with the control memory, the constants P/ROM contains program information that may also be changed to suit a customer's application. Data in the constants P/ROM control the request to send (RTS) delay for modem timing, an audible beep on the keyboard, length of the break signal, and carriage return and line feed when a printer is used.

Four other forms of data are contained in the constants P/ROM. One is message delimiters for the main I/O port, including the start and end of message, skipping over protected fields code, and end of line. There are also printer delimiters, such as message start, protect field, end of line, and start of message. Some typical field delimiters are blink, blank, reverse video, low intensity, and protected fields. Others used in more

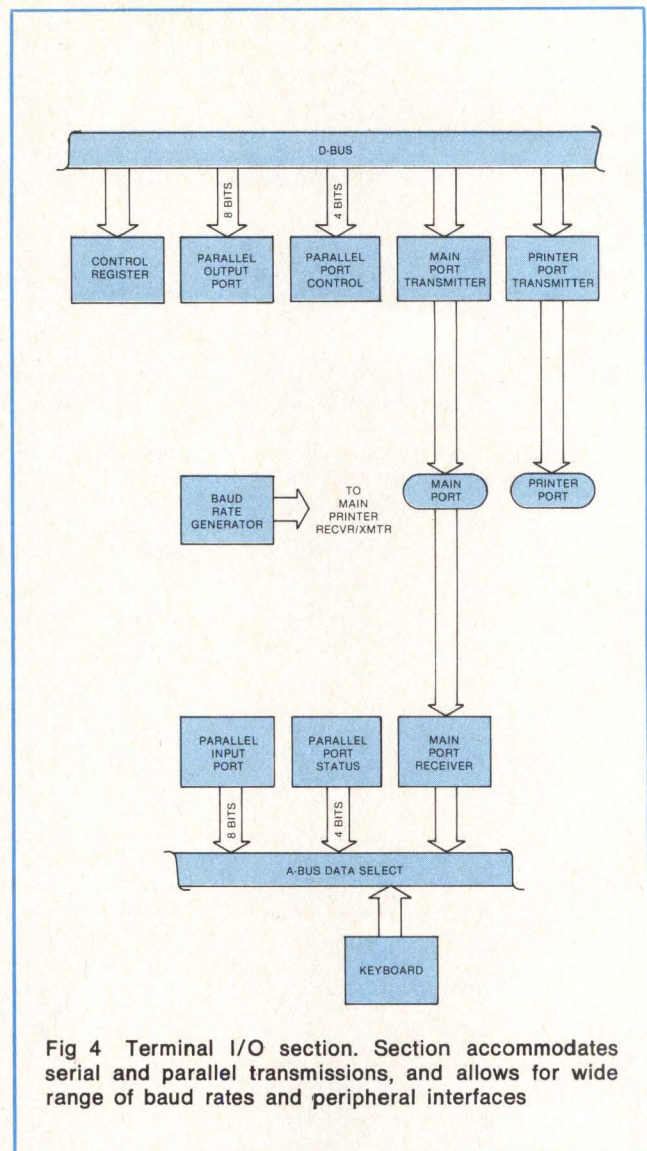


Fig 4 Terminal I/O section. Section accommodates serial and parallel transmissions, and allows for wide range of baud rates and peripheral interfaces

sophisticated applications include field limits, must fill, modulo "n," alpha only, and numeric only. All may be used in any combination. The final category is function key leaders and trailers. Included are the ASCII characters start of text (STX), leader; shift in (SI), leader; and end of text (ETX), trailer.

Switches connected to the A-bus via the data selector control operating conditions of the terminal. Some of the functions include terminal address; half/full duplex; segmented, poll, and end of transmission (EOT) modes; printer and edit options; and scroll.

The I/O section (Fig 4) is equipped to handle serial and parallel transmissions. It contains two universal asynchronous receiver/transmitters (UARTs), one for main I/O port and one for printer I/O port. Parallel I/O consists of eight data and four status bits. Serial data may be in either in RS-232-C or 20-mA current loop format. Also associated with the I/O is the control

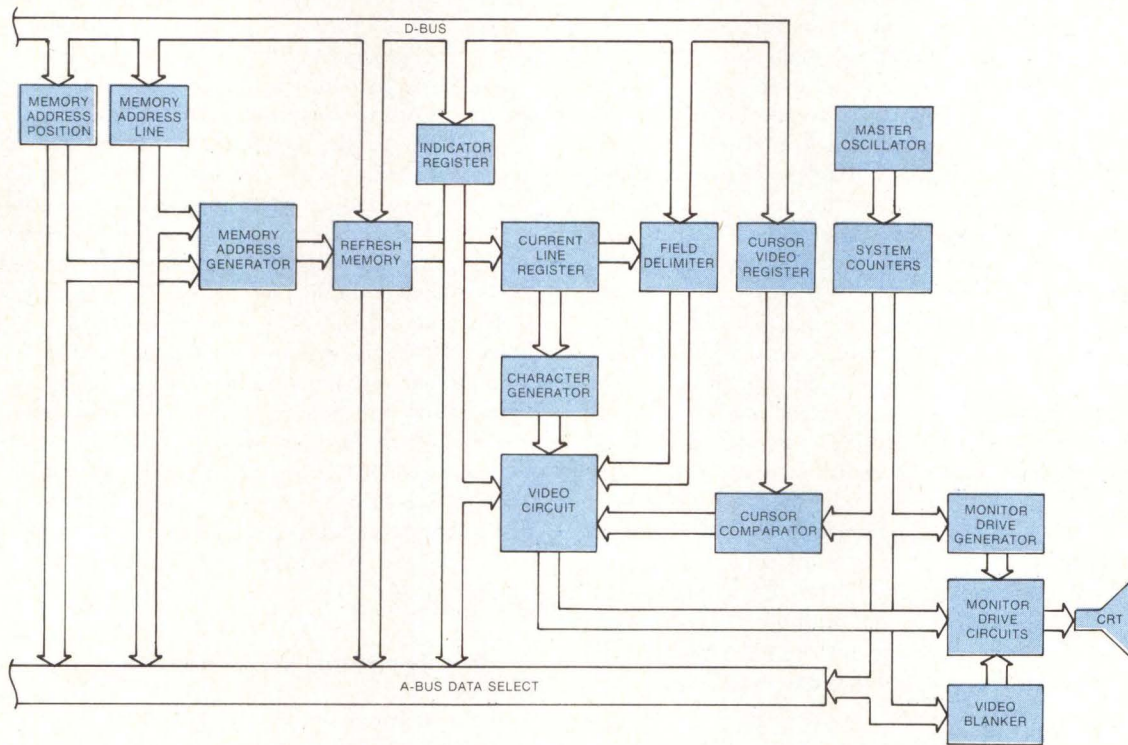


Fig 5 Monitor control circuits. Data from D-bus are processed and then displayed on CRT. Full cursor control, and field delimiters that provide for significant customizing capabilities, reside in this section

register which receives six bits from the D-bus and uses them to enable or disable certain hardware control functions. These functions are internal line feed delay, used for the printer; disable auxiliary port; video on, used to blank the screen; break, a Teletype[®] break function on the output port; beep, an audible alarm on the keyboard; and RTS.

The final section contains the monitor control circuits (Fig 5), which retrieve data from the D-bus, process them, and allow the data to be displayed on the CRT. Central to this section is the expandable RAM refresh, which continuously supplies data for display. It receives eight bits of data from the D-bus and stores them in a location determined by the memory address position and memory address line registers. The refresh memory contains all data to be stored on the screen, plus 128 word locations for general purpose use.

The memory address position register accepts eight bits of data from the D-bus and uses them to select a

memory address that corresponds to one of the 80-char columns on the CRT screen. With the memory address line (MAL) register, six bits are obtained from the D-bus to select the memory address that corresponds to one of the 24 lines. The MAL register also selects the current page of memory.

The current line of data in the refresh memory is stored in the current line register, consisting of two 80-bit shift registers. Output of these shift registers is stored and applied to the character generator and field delimiters. The character generator is a ROM that provides the video control necessary to produce alphanumeric characters. Since a socket is used to insert the ROM, the character font may be changed simply by changing ROMs. Also in the monitor control circuits is the indicator register, which accepts eight bits from the D-bus and stores them as screen edge indicator information. Outputs of this register are gated with clock signals to control a square block of video, used to identify the

operating modes of the terminal on the right edge of the screen.

Receiving inputs from the D-bus as well as current line register, the field delimiters decode these data to determine if a present character should be enhanced by a field delimiter. If so, it generates the appropriate logic signal to enable delimiter action.

Cursor control is handled within the monitor circuits. The cursor video register receives eight bits from the D-bus and stores the current cursor location. The cursor comparator compares the present line and column count against the data in the cursor video register. If coincidence is found, the cursor is displayed in that character location. On the screen, the cursor appears as a bright rectangular marker displayed in a 7 x 10 dot matrix, indicating the entry point for the next character to be typed.

Outputs from the indicator register, character generator, field delimiters, and cursor comparator are applied to the video circuit, which combines them to obtain a video control signal for the CRT monitor. Other monitor inputs are the horizontal, vertical, and synchronization signals from the monitor drive generator, and the video blanking signal from the video blanker. The end result is an alphanumeric presentation in a 5 x 9 dot matrix format. It can consist of 80 chars/line and 25 lines, for a total of 2000 upper and lower case characters. In addition, an optional line drawing package permits generation of horizontal, vertical and slanted lines composed of a combination of dots that can be used for limited graphics.

Programmable Keyboard

Adding to the customization capability of the multiprocessing terminal is the microprocessor based keyboard, which can be programmed so that any code can be assigned to any key position with the exception of shift keys (Fig 6). The keyboard is controlled by the 8035 microprocessor in conjunction with a 2708 UV-erasable P/ROM containing the program.

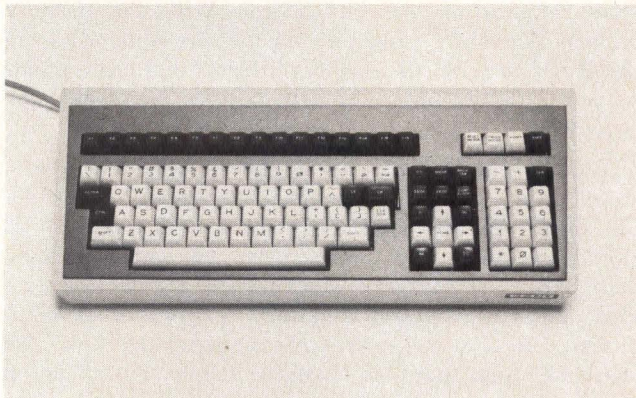


Fig 6 Standard keyboard module. Microprogrammability is key to customization process. Basic arrangement provides 56-key typewriter keyboard, 15-key edit function keypad, 15-function numeric pad, plus rows of 16 special function keys and four special function keys

In operation, the program scans the keyboard looking for a key closure. Upon detecting a closure, the scan routine is sequenced to locate the column and row in which it occurred. The row and column data are applied to the lookup table in the P/ROM and the desired code (unshifted, shifted, control, etc) is produced. All of the ASCII codes are stored in the P/ROM and are sent, through a buffer register, to the A-bus. Thus, the keyboard can be customized for a particular application by storing the appropriate program in the P/ROM. Control functions have an additional eighth bit to indicate to the keyboard program that the character is a control bit. The extra bit is stripped off by the program before the character is transmitted.

A useful feature of the keyboard is generation of a click each time a key is actuated to provide audible feedback that duplicates the sound of a typewriter. The audio level of the click is controllable by a potentiometer. The keyboard also can implement a repeat function, either by individually setting each key to repeat (controlled by data in the P/ROM), or by including a repeat key in the keyboard.

The keyboard is mounted on its own printed circuit board and has its own onboard regulator to provide power to its circuits. It also has line drivers that permit the keyboard to operate up to 100 ft (30.5 m) from the terminal.

Hotel Terminal Application

One customized terminal application, using the architecture described, was designed for a hotel management system. This particular system uses up to 42 of the intelligent terminals.

The easiest way to consider the function of the hotel system is to trace the manner in which a guest is accommodated from the time a telephone call is made for a reservation until the bill is paid. When the telephone reservation is made, a clerk enters the pertinent information into the terminal, which transmits it to the host computer data base. The same information may also be used by the sales department and by the front desk manager to aid in forecasting and in determining the availability of rooms.

When the guest checks in, the previously obtained data are displayed on the terminal screen and any omitted data are entered by the desk clerk. Once this is done, terminals located in the hotel's restaurants and gift shops and at the telephone operator console can be used to add charges to guest's bill.

Terminals in the accounting office keep track of guest billing. If the guest leaves without paying, the information is entered and a bill is printed out and mailed. When a guest leaves after paying the bill, the accounting office receives notification and enters it into its records. In addition, management reports are generated in accordance with information contained in the data base.

Terminals in the hotel system are customized to meet the needs of this special application. Along with firmware in the control memory, the keyboard is customized to be consistent with the functions performed in the



Fig 7 Keyboard variation for hotel system. Volume control adjusts level of clicks that simulate typewriter sounds. Multiple transmit keys reduce hand travel required to transmit data

hotel environment (Fig 7). One example of the combination of keyboard and tailored firmware is in the use of the segmented mode in front office applications. In this mode, only that block of data contained between two specific points on the screen is transmitted to the system computer. This is accomplished by using the cursor to designate the starting point and pushing an appropriate key. The cursor is positioned to the end point and the data are transmitted to the system computer by pressing the transmit key.

The formatted mode is used primarily in the back office for accounting functions, and involves display of a fixed format on the screen, with spaces available for the operator to insert data. This is a "fill-in-the-blanks" operation where the operator tabs across the screen from top to bottom to insert appropriate information. When this is completed, only unprotected areas of the format are transmitted to the system computer.

Two levels of brightness and blinking data aid the operator in the formatted mode. Half intensity brightness is used to present the fixed format, while full intensity is used for operator-entered data. In this way the source of data is apparent to the operator. Blinked characters guide the operator in detecting incorrect data entries that must be reentered. The segmented mode is a conversational question-and-answer operation where the questions lead to various paths related to hotel operation.

To provide additional information to the operator, printed annunciator messages are displayed on the right side of the CRT screen. These indicate the operating mode, whether the terminal is available for receipt of information, and whether the keyboard is "locked" so data cannot be entered. Annunciator messages are displayed next to the printed legend, and serve as guides to a novice operator. Another operator aid is the use of multiple transmit keys. These are used because there are usually two types of operators, one a typist who wants to use the transmit key associated with the typewriter-like keyboard, and the other who is accounting-oriented and wants to use a transmit key located near the numeric keypad.

Polling minimizes I/O hardware in both the host computer and the terminal. In this mode, the terminals are polled to see if they have any information they want to send to the computer. The operation is controlled by unique addresses assigned to each terminal; these are set by DIP switches located on the rear of the main PC

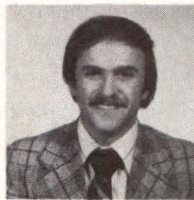
board. When a terminal is polled, it recognizes its address and dumps its message onto the I/O line.

Summary

A flexible, programmable terminal unloads much of the overhead associated with computer-terminal systems. However, terminals produced for OEM applications must have inherent flexibility that allows them to be cost effectively customized to meet a wide variety of applications. This can be achieved in intelligent terminals through the use of proper architecture that centers around easily developed and implemented firmware.

A terminal has been designed that incorporates these features. Firmware within the terminal is contained in a control memory that may contain up to 4k 24-bit words, plus a constants P/ROM with 32 bytes. The control memory holds program information contained in 24-bit instructions. The constants P/ROM contains message, field, and printer delimiters along with timing controls and function key leaders and trailers. Internal RAM can be expanded to 32k words.

A 2-bus 8-bit architecture is employed. The A-bus multiplexes all I/O handled by the terminal, whereas the D-bus involves only internal terminal data. The I/O section provides both serial and parallel communication modes. The serial interface supports both RS-232-C and 20 mA current loop formats. Parallel I/O provides eight data bits and four status bits.



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Robert Yablonski is a Senior Engineer at EECO. His work experience includes Basic Four, Texas Instruments, and Autonetics. He has a BSEE from Montana State University, and is currently pursuing graduate studies at California State University, Long Beach.

Realtime Analyzer Aids Hardware/Software Integration

By allowing designers to observe how a prototype microprocessor based system performs in realtime, an analyzing aid helps in evaluating both hardware and software for precise integration

Robert Francis and Robin Teitzel Tektronix, Incorporated, Beaverton, Oregon

After software has been coded and assembled and hardware circuits have been formulated, designers of microprocessor based systems enter a complex phase of prototype development—software/hardware integration. Program flow must be monitored and tested, software and hardware must be exercised and verified for correct interaction, and, finally, the integrated prototype system must be evaluated while executing in realtime. Throughout these integration steps, a Real-Time Prototype Analyzer can prove to be an invaluable aid. A previously published article*

*R. Francis and R. Teitzel, "Realtime Prototype Analysis As A Microprocessor Design Aid," *Computer Design*, Dec 1978, pp 65-73

covered the capabilities of this analyzer and demonstrated its commands. Used during the hardware/software integration phase, the unit identifies design problems.

Operating Principles

The Real-Time Prototype Analyzer (RTPA) operates within the Tektronix 8002A or 8001 Microprocessor Lab, enhancing system debugging capabilities with a realtime trace of prototype activity, plus extensive triggering and breakpoint capabilities. Instead of spending hours single-stepping through complex software code, the designer employs RTPA with the prototype system executing at full speed. A high speed memory buffer stores 128 sequential cycles of pro-

gram bus transactions, and two identical but independent triggers may be used in various break modes to ensure the acquisition of pertinent data. Since triggering is contingent on address, data, or control bus activity, or on an input from the analyzer's 8-channel external probe, virtually any specific signal occurrence, internal or external to the microprocessor, may be specified.

For example, attention is focused on the software and hardware that provide communication between a microprocessor system and a terminal keyboard, via an RS-232 interface. Using the RTPA, this software is verified as it executes on the prototype hardware design.

The prototype system is built around an Intel 8085A microproces-

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- Modular firmware keyboard

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 - Line drawing character set
 - Printer interface
 - ADM-3A mode

- #### OPTIONAL FEATURES
- 8-user program-mable function keys
 - Composite video output
 - 220 volt operation

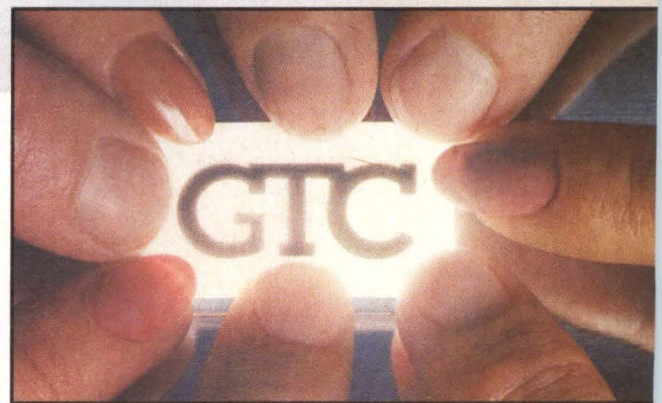
GT-400

ENGINEERING HIGHLIGHTS

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- Modular firmware
- Function keys (8 std./24 option)

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143

sor, a Motorola mc6850 asynchronous communications interface adapter (ACIA), and several RS-232 buffers (Fig 1). All system firmware is contained in 1k of read only memory (ROM), with 2k of random access memory (RAM) set aside for stack storage and workspace.

Testing Interrupt Handler Routine

System integration involves testing the program code for the ACIA interrupt handler routine. When a key on the terminal keyboard is depressed and a character is sent, an interrupt signal (RST 6.5) is generated and delivered by the ACIA to the microprocessor to initiate the interrupt handler routine.

The first step in testing the new code is monitoring prototype activity during an actual interrupt sequence. A single-step trace of the handler routine allows a detailed examination of the interaction of the

code with prototype hardware. The analyzer's command set permits a routine to be set up that will execute prototype software in real time, except for the interrupt handler program.

With the Event (EVT) command, two event comparators located in the analyzer module are invoked. By implementing the EVT address (A) parameter, the two comparators specify the section of program to be monitored in a single-step manner. For example, the first comparator is set to trigger on any address greater than or equal to 346 (EVT 1 A > 346); the second comparator is set to trigger on any address less than or equal to 386 (EVT 2 A < 386). (Note that > and < are implemented as \geq and \leq , respectively.) By ANDing the two EVT triggers, a resulting trigger occurs only in the section of memory containing the interrupt handler routine.

Furthermore, triggering conditions are limited to a specific instruction

cycle type by using the EVT instruction cycle (B) parameter. By specifying B = F as an additional qualifier for both event comparators, a trigger is generated only when an attempt is made to fetch an instruction from any address located within the designated memory range.

Using the Break If (BIF) command, conditions are defined on which a break in program execution is initiated. By designating the BIF LIM mode parameter, a break in program execution occurs only if the triggering conditions of both event comparators are met simultaneously.

Two returns are available with the BIF command to specify control of the program after a breakpoint occurs. The default value, Step (S), automatically returns control to the 8002A console monitor. Implementation of the Continue (C) command, however, causes control to automatically revert to the program. To achieve the desired single-step trace,

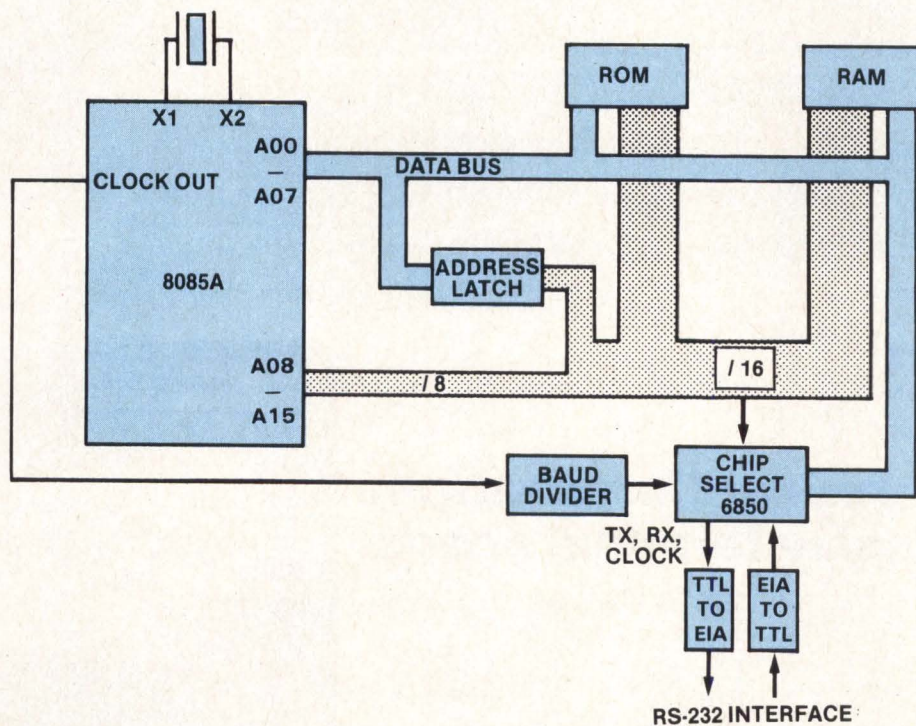


Fig 1 8085 based prototype hardware system. Address latch and upper eight address lines from microprocessor form address for system ROM and RAM. 6850 converts parallel data to RS-232 serial format

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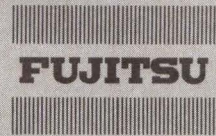
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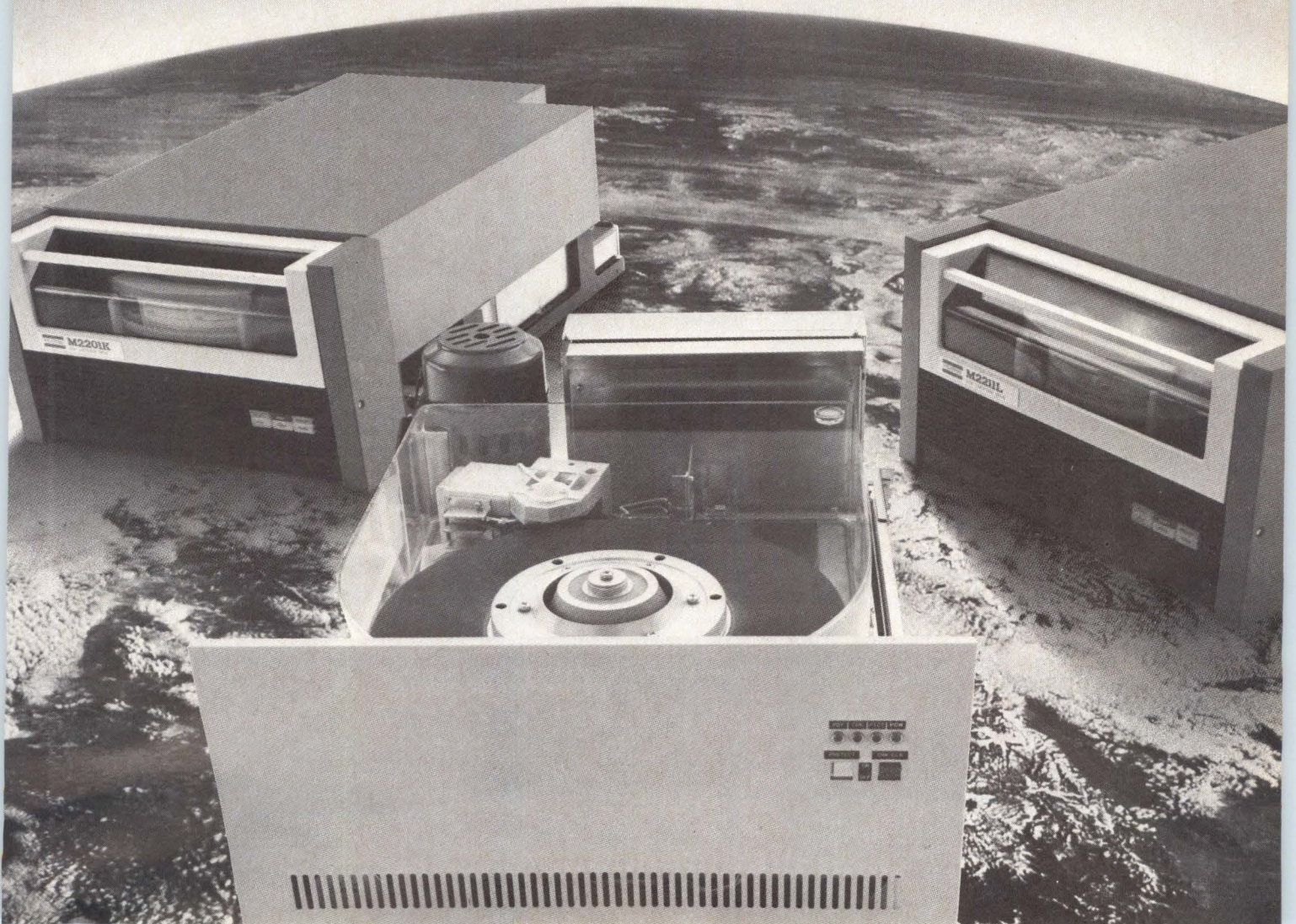
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the C return is designated. In this manner, as each breakpoint occurs, the program maintains control so that execution of the code may continue.

By implementing the specified triggering and break logic, an effectively devised scheme enables a localized single-step trace of interrupt handler code (Fig 2). With the GO command, program execution is initiated and realtime trace is started. The analyzer monitors prototype activity synchronous to the microprocessor cycle, loading data into the realtime trace buffer. To activate the interrupt handler routine, a character key is depressed. Then, the prototype system ACIA generates an interrupt to the 8085A, causing the microprocessor to begin the interrupt sequence. With the occurrence of the first interrupt handler instruction, the RTPA initiates the first breakpoint, thus verifying that the ACIA is generating an interrupt request.

Since the continue command is implemented, control continuously

reverts to the program; thus, program execution continues with each instruction being displayed in proper sequence. In this single-step trace, the prototype appears to be executing properly. Using the 8002A system debugger DUMP command, memory address 2100 is observed to ensure that the microprocessor has written the specified character in the buffer.

Next, the carriage return key is depressed to examine the microprocessor's execution of an end-of-line message. Throughout the single-step trace, the prototype appears to be functioning correctly, with the microprocessor outputting a line feed to the terminal and reinitializing the buffer pointer.

Complete Prototype Evaluation

To obtain a complete evaluation of the prototype system, testing procedures are expanded one step further. Through the single-step trace, logic flow of the program has been verified, but the procedure has not

guaranteed system performance in real time. With the RTPA, prototype performance is monitored as it executes at the microprocessor's full rated speed, thereby verifying system operation in a real-world environment.

Initially, all previous EVT and BIF command parameters are cleared so that the RTPA will not generate a break during program execution. Then, using the GO command, prototype activity is initiated and the realtime trace is started. As the program executes, 43-bit data words are sequentially acquired from the prototype and loaded into the analyzer's realtime buffer. Each word contains 16-bit data from the address bus, 8-bit data from the data bus (8 additional bits for handling 16-bit data are ignored in this application), 8-bit data from the test probe, and 3-bit data identifying cycle type. Up to 128 of the most recently acquired bus transactions are retained in the buffer at all times. When program execution is stopped,

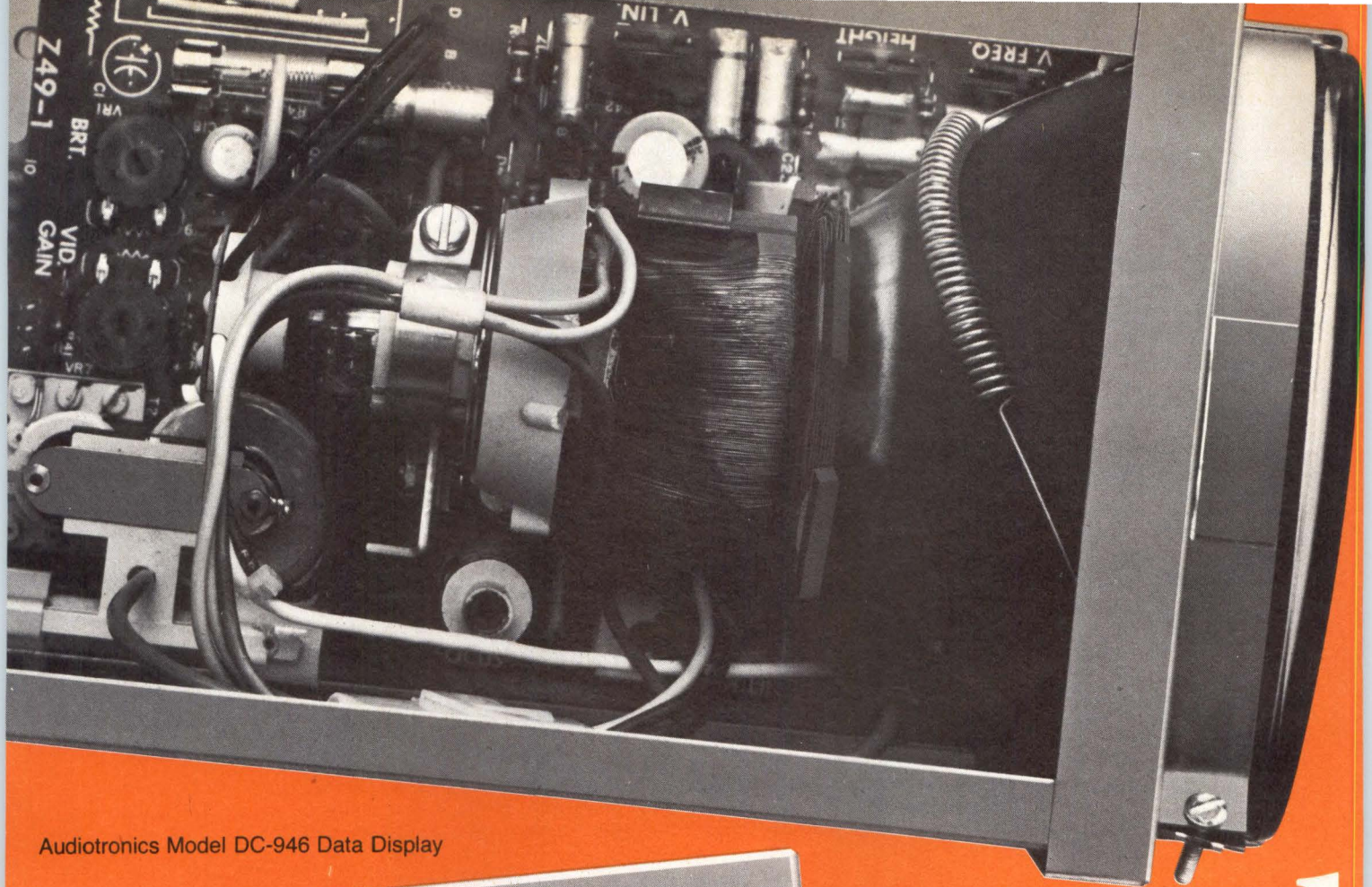
```

>EV 1 CLR A>33F B=F
>EV 2 CLR A<386 B=F
>BIF LIM C
>GO 0

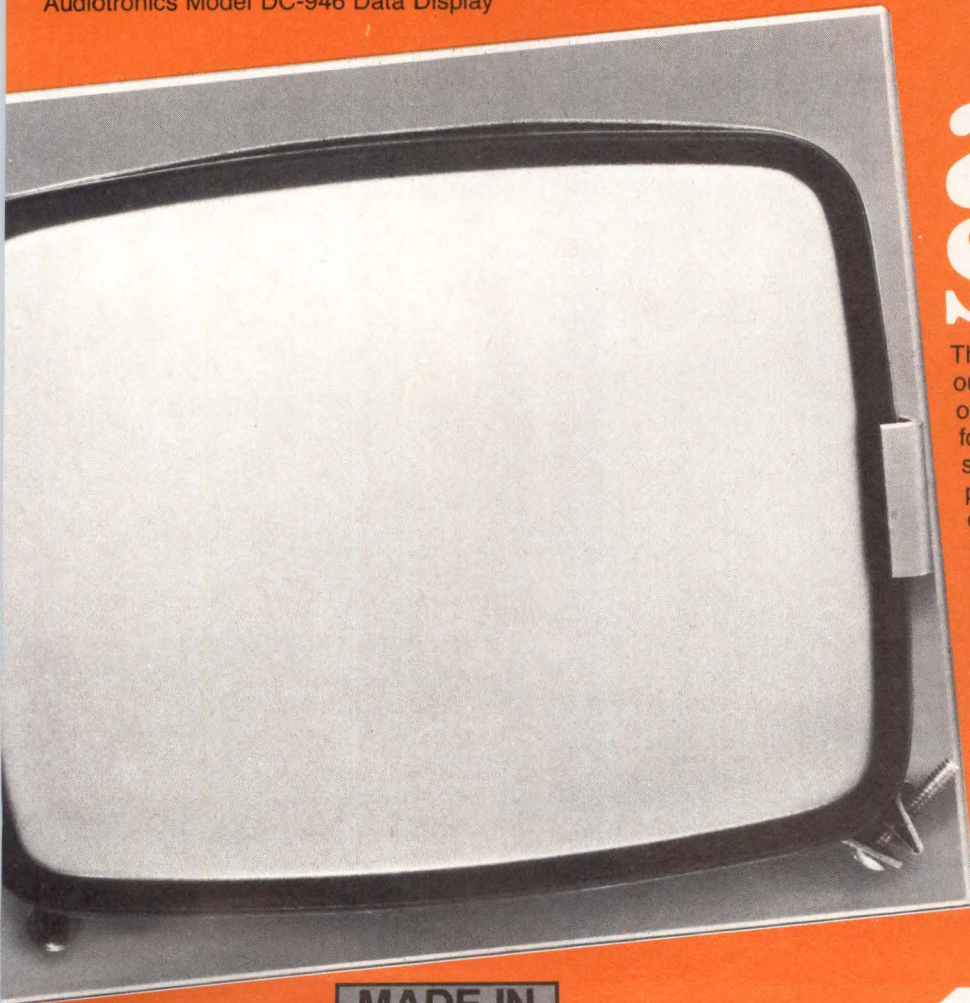
```

LOC	INST	MNEM	OPER	SP	RF	RA	RB	RC	RD	RE	RH	RL	IM	SOD
0346	F5	PUSH	P	27FB	44	58	00	00	20	10	21	00	10	0
0347	E5	PUSH	H	27F9	44	58	00	00	20	10	21	00	50	0
0348	DBE2	IN	E2	27F9	44	83	00	00	20	10	21	00	50	0
034A	E67C	ANI	7C	27F9	54	00	00	00	20	10	21	00	50	0
034C	CA5C03	JZ	035C	27F9	54	00	00	00	20	10	21	00	50	0
035C	2A1020	LHLD	2010	27F9	54	00	00	00	20	10	21	00	50	0
035F	DBE3	IN	E3	27F9	54	C1	00	00	20	10	21	00	50	0
0361	D3E3	OUT	E3	27F9	54	C1	00	00	20	10	21	00	40	0
0363	E67F	ANI	7F	27F9	14	41	00	00	20	10	21	00	40	0
0365	77	MOV	M,A	27F9	14	41	00	00	20	10	21	00	40	0
0366	FE0D	CPI	0D	27F9	00	41	00	00	20	10	21	00	40	0
0368	CA7203	JZ	0372	27F9	00	41	00	00	20	10	21	00	40	0
036B	23	INX	H	27F9	00	41	00	00	20	10	21	01	40	0
036C	221020	SHLD	2010	27F9	00	41	00	00	20	10	21	01	40	0
036F	C38303	JMP	0388	27F9	00	41	00	00	20	10	21	01	40	0
0383	E1	POP	H	27FB	00	41	00	00	20	10	21	00	40	0
0384	F1	POP	P	27FD	44	58	00	00	20	10	21	00	40	0
0385	FB	EI		27FD	44	58	00	00	20	10	21	00	40	0

Fig 2 Trace of interrupt handler code. Commands which set up event triggers are followed by single-step trace that occurs when microprocessor accesses range of instruction set up by EV1 and EV2 commands. RTPA commands allow designer to see execution of interrupt handler routine when key on terminal (other than CR) is depressed; remainder of prototype software executes in real time. Trace shows that interrupt routine is working correctly



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a portion (or all) of these transactions are displayed to obtain a snapshot view of prototype activity.

With the prototype running, real-time execution of the software can be evaluated. By depressing a character key on the terminal keyboard, prototype response to an interrupt is examined. The response appears to be correct, since the receive and echo portions of the interrupt handler rou-

tine are executed. As each character key is depressed, a character is sent back to the terminal.

To complete software evaluation, the carriage return key is depressed. At this point, an error occurs in the prototype. When the carriage return is entered, the terminal receives only the return and fails to detect a line feed. Since this section of the monitor program executed correctly dur-

ing the single-step trace, a timing problem is considered; however, as logic flow of the program code has already been verified, perhaps the line feed character is being sent to the ACIA before the transmitting buffer is empty.

To test this assumption, a program patch is inserted to display ACIA status just before the line feed instruction is sent. By substituting a

```
>PA 400 DBE200
>EVT 1 CLR A=400
>BIF 1
>GO 0

LOC INST      MNEM  OPER   SP    RF  RA RB RC RD RE RH RL IM  SOD
0400 DBE2     IN    E2     27F9  54   00 00 00 20 10 21 05 00  0
0400 BREAK
```

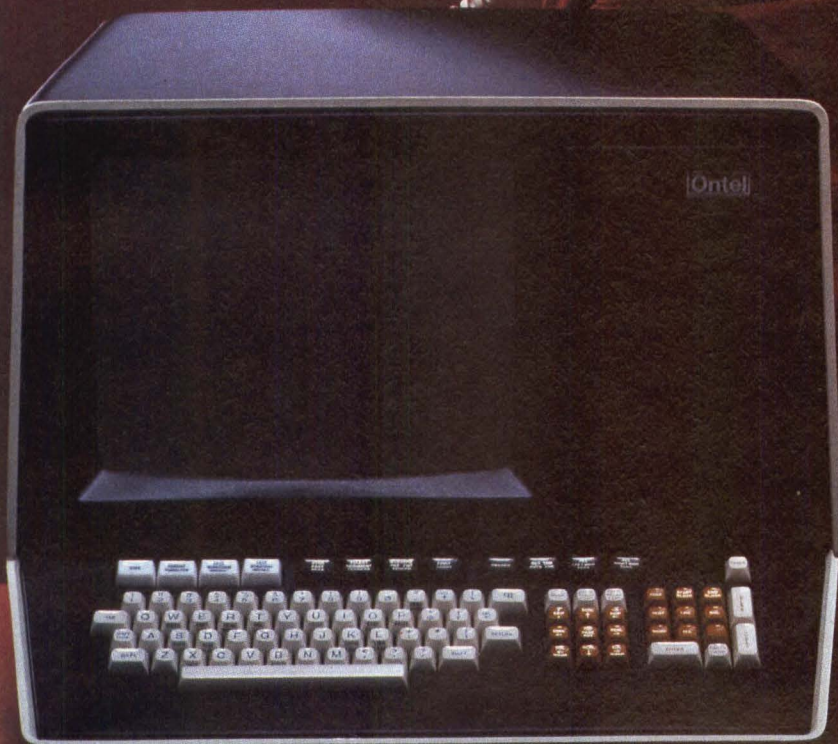
Fig 3 Commands to implement test for software problem. Test is patched to see if ACIA is ready to accept another character. In trace, accumulator shows status of ACIA after execution of IN ER instruction. Value of 00 indicates not ready

```
LOC INST      MNEM  OPER   SP    RF  RA RB RC RD RE RH RL IM  SOD
0346 F5       PUSH  P      27FB  44   58 00 00 20 10 21 00 10  0
0347 E5       PUSH  H      27F9  44   58 00 00 20 10 21 00 10  0
0348 DBE2     IN    E2     27F9  44   83 00 00 20 10 21 00 50  0
034A E67C     ANI   7C     27F9  54   00 00 00 20 10 21 00 50  0
034C CA5C03   JZ    035C 27F9  54   00 00 00 20 10 21 00 50  0
035C 2A1020   LHLD  2010 27F9  54   00 00 00 20 10 21 00 50  0
035F DBE3     IN    E3     27F9  54   8D 00 00 20 10 21 00 50  0
0361 D3E3     OUT   E3     27F9  54   8D 00 00 20 10 21 00 40  0
0363 E67F     ANI   7F     27F9  10   0D 00 00 20 10 21 00 40  0
0365 77      MOV   M,A  27F9  10   0D 00 00 20 10 21 00 40  0
0366 FE0D     CPI   0D     27F9  54   0D 00 00 20 10 21 00 40  0 TEST FOR CR
0368 CA7203   JZ    0372 27F9  54   0D 00 00 20 10 21 00 40  0 CR FOUND
0372 2L0021   LXI   H,2100 27F9  54   0D 00 00 20 10 21 00 40  0
0375 221020   SHLD  2010 27F9  54   0D 00 00 20 10 21 00 40  0 STORE REINITIALIZED BUFFER POINTER
0378 DBE2     IN    E2     27F9  54   02 00 00 20 10 21 00 40  0 READ ACIA STATUS
037A 1F      RAR           27F9  54   01 00 00 20 10 21 00 40  0
037B 1F      RAR           27F9  55   00 00 00 20 10 21 00 40  0
037C D27803   JNC   0378 27F9  55   00 00 00 20 10 21 00 40  0 TEST FOR TRANSMIT ACIA BUFFER EMPTY
037F 3E0A     MVI   A,0A 27F9  55   0A 00 00 20 10 21 00 40  0
0381 D3E3     OUT   E3     27F9  55   0A 00 00 20 10 21 00 40  0 ACIA BUFFER EMPTY, SEND LE
0383 E1      POP   H      27FB  55   0A 00 00 20 10 21 00 40  0
0384 F1      POP   P      27FD  44   58 00 00 20 10 21 00 40  0
0385 FB     EI           27FD  44   58 00 00 20 10 21 00 40  0

00C0 76      HLT           27FF  44   58 00 00 20 10 21 00 08  0
00C0 BREAK
```

Fig 4 Trace verification of code. Single-step of when carriage return is pressed on terminal keyboard is shown. From trace, conditional jump occurrence can be determined. Special processing for CR can be verified from trace

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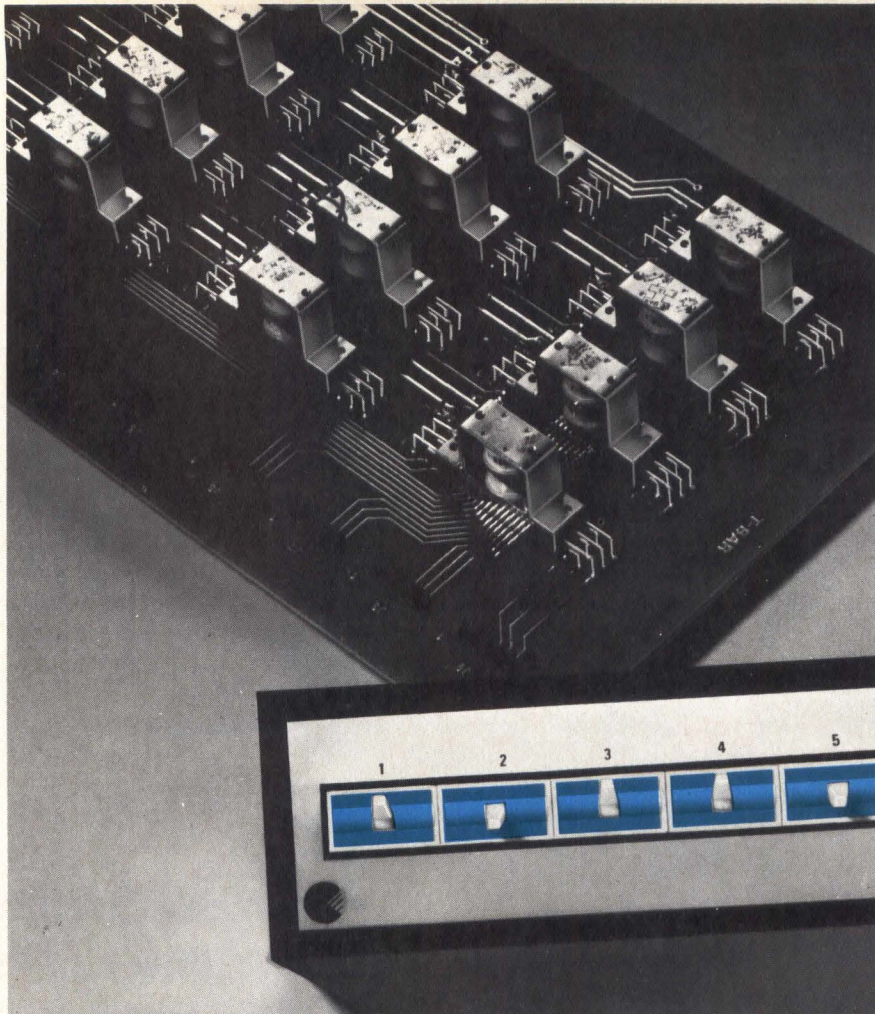
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Jump (JZ) 400H for the JZ FINR instruction in the assembled code, the microprocessor is forced to jump to address 400 (Fig 3). At this address, an In Port (E2) instruction is inserted to read the status of the ACIA.

Then, with the EVT command, the first event comparator is set to generate a trigger when address 400 is accessed—EVT 1 A = 400. Next, the BIF command is set to generate a breakpoint in program execution when EVT 1 is activated.

Again, the prototype system is energized. When the carriage return key is depressed, the RTPA generates a breakpoint at address 400. Examination of 8085A accumulator status reveals that the ACIA is not yet ready to accept a new character, verifying that the problem is occurring because the transmit buffer is not yet empty.

To try out the solution before reassembling the program, a conditional loop is patched in, beginning at address 400. This loop delays continuation of interrupt handler program execution until the ACIA is ready for another character. After clearing the RTPA command parameters, the real-time trace of prototype activity is implemented again. This time, the interrupt handler routine functions correctly.

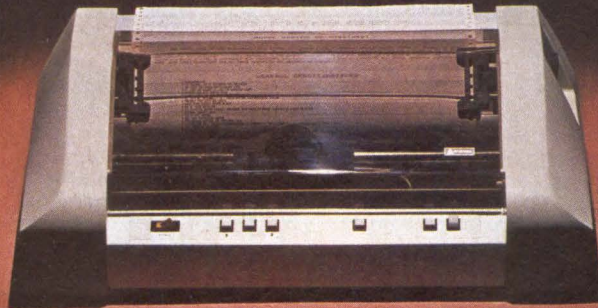
Having confirmed the software problem, the original source code is modified to include the conditional timing loop. Trace verification of the code is shown in Fig 4.

Summary

These application procedures illustrate how RTPA can aid designers during the step by step process of integrating a prototype system. Operating within the Microprocessor Lab, this design tool enhances in-circuit emulation by offering several testing capabilities essential for the thorough evaluation of prototype system execution. Designers are able to center on a specific area of prototype activity for in-depth examination; also, with an external logic probe, they can view both software and hardware functional states. In effect, the RTPA offers an easy, yet powerful, method of observing how the microprocessor is performing within a prototype system and, more importantly, how the overall system is executing. □

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INTERFACING FUNDAMENTALS: TIMING DIAGRAM CONVENTIONS

Peter R. Rony

Virginia Polytechnic Institute and State University
Blacksburg, Virginia

Users should be aware of timing diagram conventions that are likely to be encountered in the study of signal timing in microcomputer systems. This summary draws together the different conventions and illustrations (adapted from Refs 1 and 2) to provide users with the necessary information.

Conventions used in the representation of a single signal are given in Fig 1. A low level typically is a voltage that is near ground potential. A high level, for transistor-transistor logic inputs and outputs, typically is a potential that ranges from 3.5 to 5.0 V. A floating signal occurs when the output from a 3-state device is in its high impedance state; the representation is a dashed line that is half-way between the low and high logic levels. Positive edge and negative edge transitions are shown as diagonal rather than vertical lines to account for the fact that the transitions are not instantaneous, as well as to permit the choice of a specific voltage when delay times are provided on the timing diagram. If the time when the transition occurs can vary, then a series of parallel diagonal lines are used to represent this fact, as shown in Fig 1.

Several timing diagram conventions apply when one signal influences another signal (Fig 2). Signal A is the input signal, and Signal B is the resulting output signal. As a function of time, signal A exhibits both steady logic levels (logic 0 and logic 1) and also transitions between these two levels (the 0 to 1 transition, known as a positive edge, and the 1 to 0 transition, known as a negative edge).

Depending upon the type of digital function—gate, edge triggered latch, transparent latch, 3-state buffer, etc—that is employed, signal B can respond to signal A in four ways. As depicted in Fig 2, a transition in signal A can cause either a transition in signal B, as would occur in a simple gate or gating circuit, or else a steady logic level, as would occur with an edge-triggered flipflop such as the 7474 chip. When signal A reaches and remains at a specific logic level, then signal B can exhibit a steady logic level, as would be the case for a transparent latch (such as the 7475) or a 3-state buffer;

otherwise, signal B can undergo a transition in logic levels—a situation that is not common.

There are several ways of representing delay times that occur when one signal influences another signal. Four possibilities are indicated in Fig 3. The small circle represents the time when a specific logic level is reached; the cross represents that specific amplitude on a logic level transition from which the time is measured.

Fig 4 presents some conventions that represent parallel buses containing two or more signals. "Signals change" notations in the first and last diagrams indicate that one or more of the parallel signals change level, but that the transition is unspecified. A floating bus is represented by a dashed line that is halfway between the two logic levels. In the third illustration, the 3-state buffers become active at time a, but the output is not guaranteed to be stable until time b. In the fourth, the 3-state buffers can become active at any time between a and b.

Several applications of the previous conventions* (from Figs 2 and 4) are identified in Fig 5, which has been adapted from Ref 1. In the first diagram, a low level from signal A triggers a bus change of state. In the second, a low level from signal A and a transition in signal B trigger a third event. In the third, a positive edge from signal A triggers changes in both signals B and C. Finally, two signals at different logic levels can result in a third signal's transition, while one signal can produce transitions in two other signals.

References

1. A. Osborne and J. Kane, *An Introduction to Microcomputers, Volume 2, Some Real Products*, Osborne & Associates, Inc, Berkeley, Calif, 1978, p xlvi
2. J. D. Nicoud, *MicroScope 1*, Apr 1977, MicroScope, po Box 141, CH-1000, Lausanne 13, Switzerland

*The author is interested in obtaining other references from readers who know of more detailed and systematic listings of these types of timing diagram conventions. Dr Rony may be reached by writing him at the Dept of Chemical Engineering, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061.

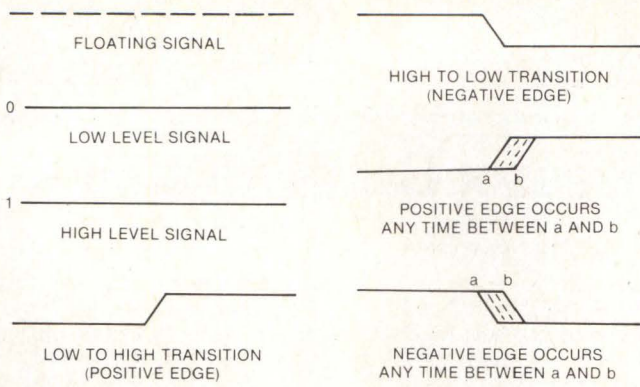


Fig 1 Timing diagram representations for single signal. Horizontal lines combine with diagonal lines, which indicate transitions in logic levels

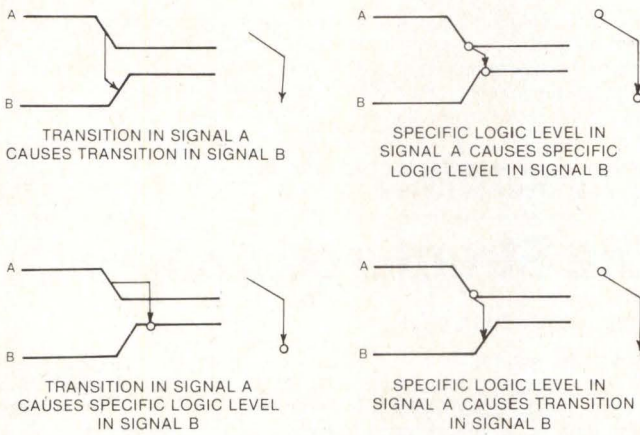


Fig 2 Timing diagrams. Conventions for pair of signals illustrate four ways in which one signal can gate or trigger another signal

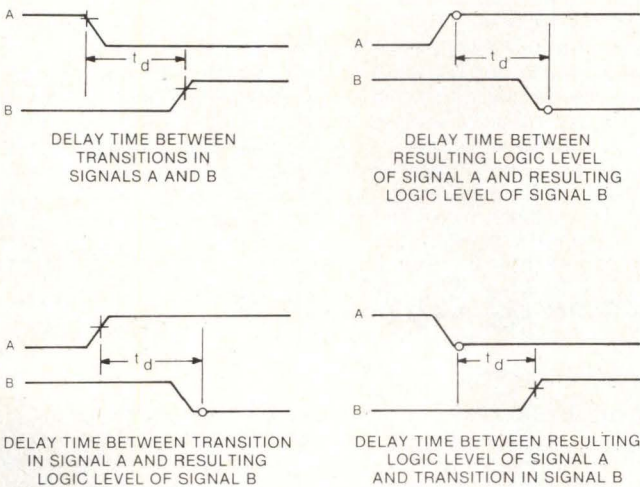


Fig 3 Delay times. Representations are shown of delay times in timing diagrams for pair of signals

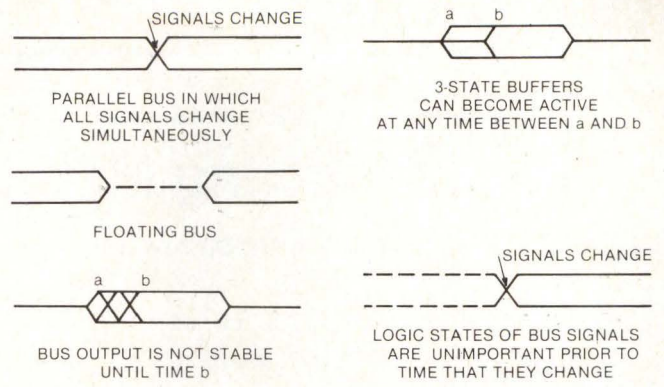


Fig 4 Bus timing diagrams. Representations illustrate five conventions for bus with two or more signals

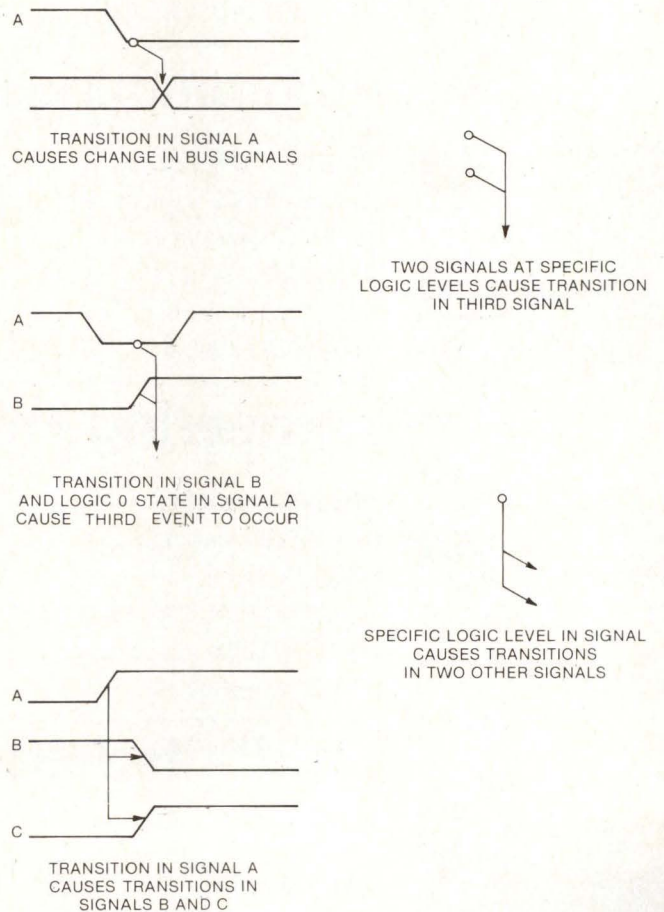


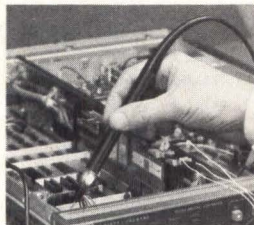
Fig 5 Applications. Combinations of signal transitions and logic states cause changes in other signals

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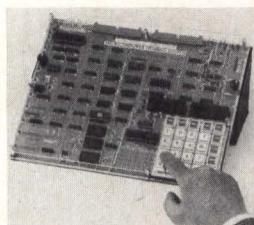


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```
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11. VAR RF:INTEGER;
12. BEGIN
13. DOTS(LEVEL);
14. IF N>1 THEN
15.   RF:=RFIB(N-
16.   ELSE
17.   IF N=1 THEN
18.     ELSE RF:=0
19.   RFIB:=RF;
20. DOTS(LEVEL);
```

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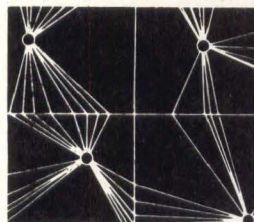


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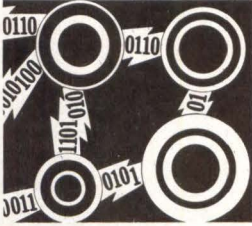


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WASHINGTON, D.C. April 29-May 2

Course 350 - Four days

This course provides a comprehensive introduction to distributed processing and computer network design techniques. It covers the individual elements of a distributed processing system and how these elements are synthesized to form a system which best meets application specific objectives. Throughout the course, application examples provide concrete examples of concepts presented, with emphasis on the factors affecting key planning, design and implementation decisions.

Computer Communication Networks

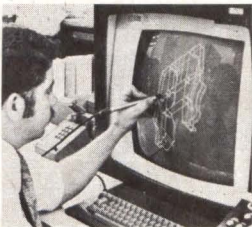


WASHINGTON, D.C. Feb. 26-29
DENVER March 4-7
LOS ANGELES March 25-28
ATLANTA April 15-18
BOSTON April 22-25
MINNEAPOLIS May 6-9

Course 355 - Four days

This course emphasizes the practical aspects of network design, interfacing, protocols and packet switching. Participants will learn how to: implement network communication and control protocols; utilize packet and message switching techniques; evaluate available network hardware and software components; interface local systems to value added networks; design and build private user networks; recognize the motivations and tradeoffs for specific designs. The course has been prepared for design engineers, systems analysts, programmers, systems architects and project managers.

Computer Graphics State of the Art Techniques and Applications



WASHINGTON, D.C. Feb. 12-15
SAN DIEGO March 18-21
NEW YORK April 15-18
SAN FRANCISCO April 22-25
BOSTON April 29-May 2
WASHINGTON, D.C. May 6-9

Course 365 - Four days

Hardware elements of computer graphics systems are presented at the level required for detailed system specification, selection and acquisition. Software techniques for computer graphic systems are developed from the elementary level of line generation and continue through advanced approaches to animated three-dimensional color displays with hidden surface removal. Off-the-shelf, commercially available software packages are analyzed and evaluated. Emphasis is placed on hardware/software tradeoffs, cost effectiveness and the advantages and limitations of alternative approaches.

Computer Aided Design and Manufacturing

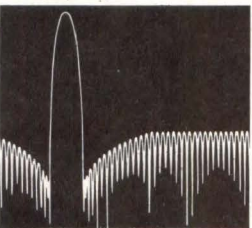


SEATTLE Feb. 25-28
DALLAS March 3-6
SAN FRANCISCO March 17-20
NEW YORK March 24-27
BOSTON April 14-17
CINCINNATI April 21-24

Course 370 - Four days

This course presents a total overview of CAD/CAM technology in numerous industries and disciplines and provides state-of-the-art fundamentals for further in-depth involvement. Emphasis is placed on the design and manufacturing processes, on the design/manufacturing (CAD/CAM) interface, and on the critical role of management in the implementation of CAD/CAM systems. The course has been prepared for design and development engineers, programmers and systems analysts, planning and operations managers, and others who will be involved with CAD/CAM systems.

Digital Signal Processing



ATLANTA Feb. 25-29
DENVER March 10-14
LOS ANGELES March 17-21
BOSTON April 14-18
WASHINGTON, D.C. April 21-25
SAN DIEGO April 28-May 2

Course 412 - Five days

The objective of this course is to present the necessary fundamentals of digital signal processing in a clear and comprehensive manner, to develop an understanding of new processing techniques, to survey the state of the art of hardware and software available, and to apply this information to a range of concrete design examples. The course is of benefit both for those who wish to achieve a basic understanding of this exciting area, and for those whose interest is in advanced techniques and the implementation of practical systems.

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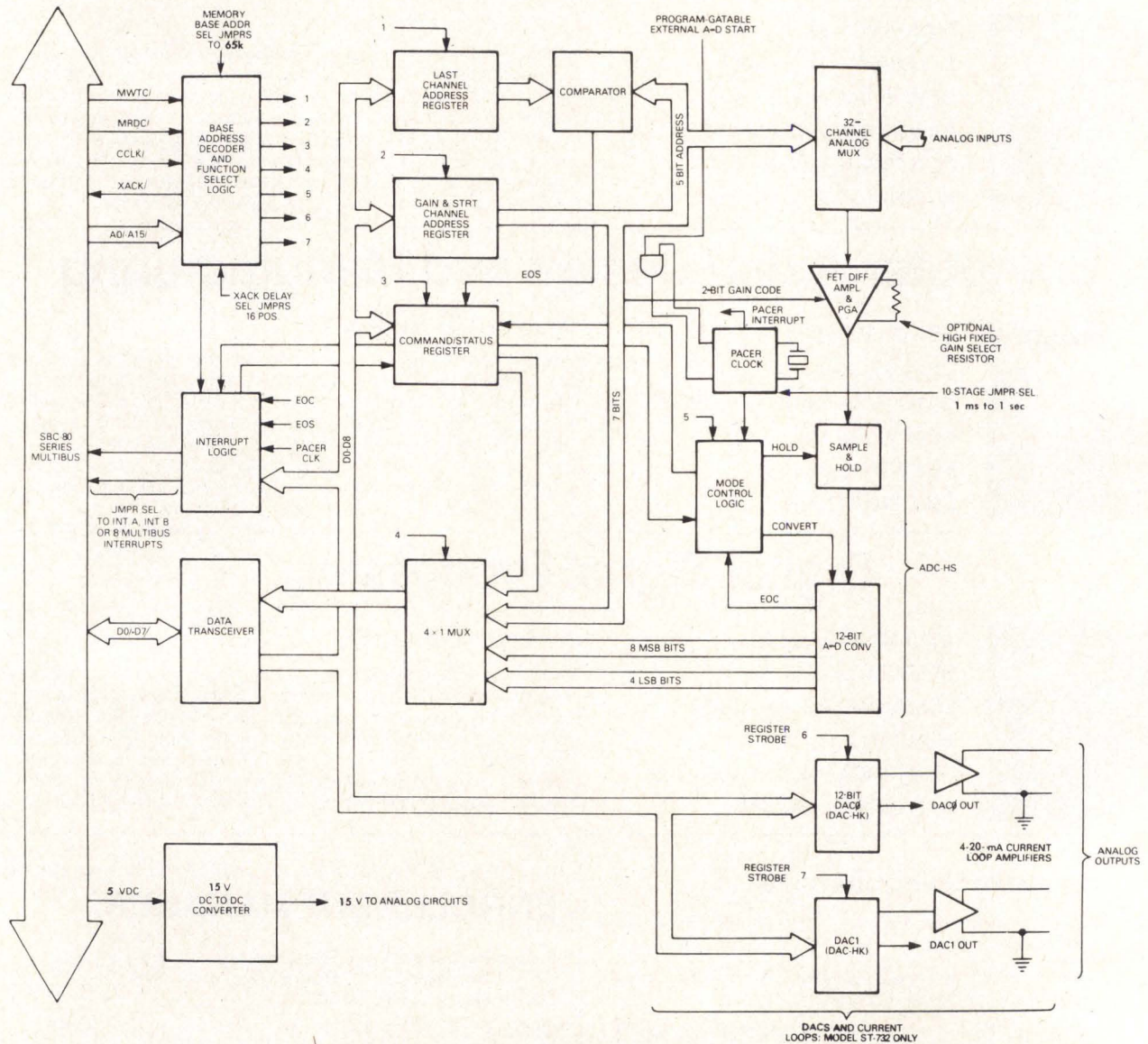
Slide-In Multibus Compatible Boards Reduce Cost of Analog Input and Output

A-D/D-A analog input and output systems—mechanically, electrically, and pinout compatible with Intel's SBC-711/732 analog I/O boards—attach to an Intel iSBC-80/05, 80/20, or other SBC series and Multibus™ compatible microcomputer. They interface the microcomputer to instruments in manufacturing process, laboratory, or environmental control systems that

use analog voltages and require signal processing.

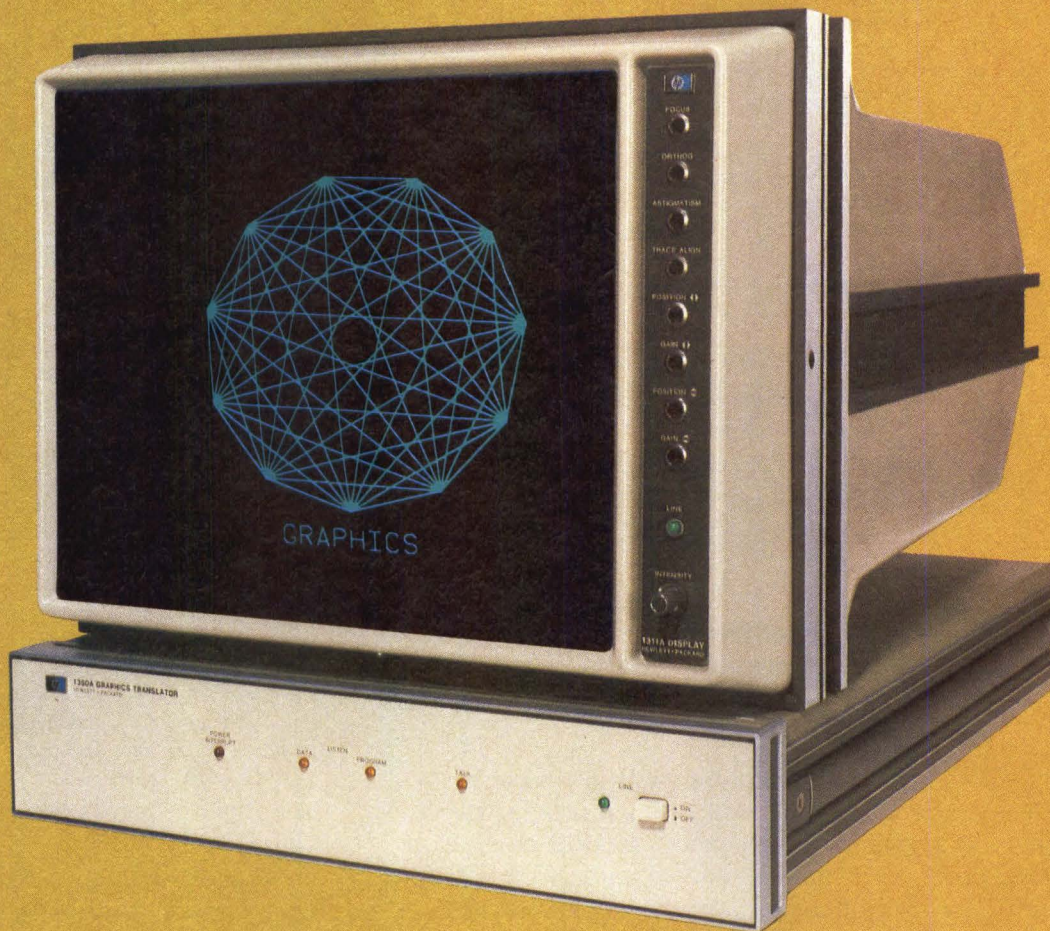
There are 32 single-ended (or 16 differential) A-D channels on both the ST-711 and ST-732. The latter also features two D-A channels with built-in current loop output compatibility for further use with servo controlled systems, oscilloscopes, and analog displays.

Working directly from Intel's RMX-80 analog I/O driver operating software, the 12 x 6.75 x 0.5" (305 x 171 x 13-mm) boards use a high impedance FET input differential amplifier. Programmable gain amplifier offers X1, 2, 4, or 8; a fixed amplifier gain to X1000 is optional. Common mode noise reduction ranges from 120 dB at dc to 60 dB at 60 Hz. Power



Slide-in A-D/D-A I/O systems from Datal interface to Intel SBC series and Multibus microcomputers. ST-711 and -732 are identical, with latter containing two 12-bit DACs with input registers. A-D sections use successive approximation ADC and S/H amplifier. Also included is FET input differential amplifier

Now, high-performance graphics for minicomputer-based systems don't have to be expensive.



HP's 1350S Display System provides high speed interaction, brightness and high resolution . . . at low cost.

When your minicomputer-based graphics systems require high-quality, real-time displays — with no price premium — you'll want the HP 1350S.

With the 1350S, you get a high-resolution display system that generates bright, sharp vectors and alphanumerics at fast writing speeds. Which means higher speed and 1000 x 1000 addressable resolution at a lower cost than high-resolution raster graphic systems.

That's because the 1350S offers a choice of high-perform-

ance random scan graphic displays in a variety of CRT sizes, plus digital storage and refresh. The bottom line to you is display flexibility, and an exceptional price/performance value.

Other system features include rapid updating of information displayed and simultaneous display of different information on up to three additional CRTs.

For compatibility with a variety of minicomputers, two easy-to-use interfacing alternatives are available: The serial RS-232C with baud rates to 57k; and the HP-IB parallel interface.

The HP 1350S, priced at \$8,900*, provides a cost-effective graphics solution for computer aided design, data acquisition, analytical instrumentation, simulation, medicine or radar — anywhere a high speed, bright and clear graphics display is required. For more information, write to Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304. Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.

*Domestic U.S.A. price only.

089/14



HP-IB: Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a measurement system.

CIRCLE 83 ON INQUIRY CARD

consumption is 5 Vdc, 25 A max. An onboard dc-dc power converter, incorporated by Datel Systems, Inc, 11 Cabot Blvd, Mansfield, MA 02048, operates from the computer's 5-V supply to provide ± 15 V for linear circuits.

The A-D section uses a 12-bit ($\pm \frac{1}{2}$ LSB) converter with typical tempcos of ± 25 ppm of FSR/ $^{\circ}$ C for gain drift and ± 20 μ V/ $^{\circ}$ C zero drift. Specs include overall system throughput rate of 23k samples/s, analog input im-

pedance of 100 M Ω , A-D conversion time of 8 μ s, and for the s/H amplifier, an aperture delay time of 100 ns and acquisition time of 6 μ s. Standard A-D/D-A input ranges are ± 10 V full scale (or jumper selected to ± 5 V, or 5 or 10 V unipolar); low level ranges to 10 mV are resistor selected. The user may add resistors to provide current loop inputs and outputs.

Op amps with 200-m Ω output impedance and short circuit protection are used in the D-A outputs of the ST-732. D-A channels have a temperature drift of ± 50 ppm of FSR/ $^{\circ}$ C; D-A settling time is 4 μ s. Current loop output of 4 to 20 mA can be provided.

Other components are a 10-stage, jumper selected, program gatable Pacer start clock from 1 ms to 1 s, and EOC, EOS, and external start trigger interrupts. When operated differentially, the A-D inputs can take up to 16 user supplied shunting resistors for current inputs. Standard digital coding is offset binary (bipolar). Jumper changes select straight binary (unipolar) or 2's complement (bipolar). The systems appear to the CPU as memory mapped functions, which may be placed anywhere in memory using 16 consecutive addresses.

A diagnostic program, provided on paper tape, checks all data paths and registers and permits A-D hexadecimal scans to be printed out on a teletypewriter or displayed on a CRT. The diagnostic listing contained in the systems manual was written such that the user may extract portions and write them into an applications operating program.

Circle 410 on Inquiry Card

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**Multibus Development/
Control Unit Rackmounts
For Industrial Service**

A single-board computer and floppy disc controller comprise the DCS/80, which together with dual 8" (20-cm) floppy discs, 5-slot terminated backplane, and heavy duty power supply, fits in a standard 10.5" rack space. If the system is to be used for software development, Distributed Computer Systems, 223 Crescent St, Waltham, MA 02154, provides high level

Presenting the first 6 megabyte floppy drive!



Now get 6 megabytes of memory in about the same space as a 1 megabyte drive.

That's right. Until now, the only way you could build up to 6 megabytes of floppy disk memory into your product was to add on drive after drive.

The new Burroughs MD122 memory unit drives two 8-inch, double-sided floppies, each with a formatted capacity of 3 megabytes.

Now you can do all these applications that require more capacity, yet keep the advantages of low cost, removable media. And your system's performance will improve, too, due to the MD122's voice coil actuator with a 100 ms average access time.

We've already built in an Advanced Microprocessor Controller (AMC) which performs many of the functions

normally required of the host system controller and the host CPU.

We've already interfaced it!

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- Error detect/correct
- Sector relocation
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Burroughs OEM Marketing, Burroughs Place, Detroit, MI 48232, (313) 972-8031. In Europe, High Street, Rickmansworth Hertfordshire, England, Telephone 09237-70545.

Burroughs

CIRCLE 85 FOR GENERAL INFORMATION

CIRCLE 86 FOR DETAILED SPECIFICATIONS.

languages, including Pascal and Process Control BASIC, and cross assemblers for Intel, Signetics, TI, National Semiconductor, Motorola, RCA, Synertek, and Zilog microprocessors.

The Multibus™ compatible CPU, an enhanced version of the Intel iSBC 80/10, can have up to 4k of RAM, 16k of P/ROM-ROM, 48 programmable I/O lines, and 2 independent serial I/O channels with optional opto isolation for noisy environments. This card drives other Multibus compatible options such as a video controller, cartridge disc, and magnetic tape. A TTL compatible 60-Hz line clock for realtime applications is controlled from the front panel.

Containing its own 8080 microprocessor, the floppy disc controller is an intelligent Multibus compatible unit offering concurrent operation with the main CPU as well as extensive system error reporting. It performs standalone diagnostics and testing. With up to 2k of internal memory, it will perform buffered I/O operations using optional software. A total of four CDC floppy discs are accommodated.

Both dynamic and static memory boards are available, as is a special board with two additional serial I/O ports. IBM bisynchronous telecommunications software is available. Among the disc operating systems offered are CP/M and CP/PLUS, which features batch processing, logical to physical device mapping, instant error detection, command files, and buffered I/O operation using the disc controller. It also includes a text editor, assembler, and debugger.

Circle 411 on Inquiry Card

Support Products Develop And Debug Systems Based On 8-Bit Microprocessor

Support of the mc6809 microprocessor is now available in the form of the mc6809 EXORCISER II and EXORterm 220 development systems and six update packages to adapt existing EXORCISER I, IA, or II systems. The mc6809 module to be added serves to provide clock timing and to function as the processor for the development system and the user system

being emulated. The clock circuit provides 1.0-, 1.5-, and 2.0-MHz signals as well as dynamic memory refresh. Further software support to be announced by Motorola Microsystems, PO Box 20912, Phoenix, AZ 85036, are the Pascal interpreter, Pascal compiler, MPL compiler, FORTRAN compiler, BASIC interpreter, and IBM 370 and PDP-11 cross assemblers.

New mc6809 EXORCISER II and EXORterm 220 systems differ from mc6800 units as they contain the 6809 MPU module and extend other internal module capabilities to meet 6809 specs. To upgrade existing development systems, users may add the basic update package with MPU module, DEBUG module, floppy disc controller P/ROM firmware, and mc6809 MDOS™ diskette (with macro assembler and CRT editor).

Upgrading an EXORCISER I, IA, or EXORterm 200 or 220 for mc6809 operation achieves performance features of an EXORCISER II. These are dual memory map, memory parity, 2-MHz operation, dynamic systems bus, second level interrupt vectors, and EXBUG 2™.

Complete mc6809 based EXORCISER/EXORterm development systems can be ordered with either 32k dynamic or 32k static memory versions of each. All of the updates and full systems can be ordered with the user system evaluation (USE) module along with the standard MPU module, thus permitting the systems to interconnect with a user's external prototype for more flexibility.

Circle 412 on Inquiry Card

Versions of 4-Bit Control Processors Are Available Without ROM

ROMless n-channel MOS Microcontrollers manufactured by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, are 40-pin devices containing a CPU, 64 x 4-bit RAM, and I/O. COP402 and 402M are similar to the COP420 (see *Computer Design*, Dec 1978, pp 130, 132) with the addition of pins to output the ROM address and to input ROM data; performance of the devices is identical, facilitating develop-

ment and debug of 420 programs prior to final masking.

Other suitable applications are for low volume requirements using up to 1k x 8 bits of external ROM or P/ROM, or for situations requiring program changes. A reduction in clock frequency permits the 402 to emulate the COP410L, 411L, 420L, or 420C. The 402M has the further advantage of MICROBUS™ compatibility. It can serve as a peripheral to input and output data to and from a 4-, 8-, or 16-bit host microprocessor.

A single 4.5- to 6.3-V supply, true vectored interrupt plus restart, 3-level subroutine stack, internal timebase counter for time processing, and external event counter register with serial I/O capability are featured. Instruction execution time is 4- μ s.

Members of the COPS family are all software and hardware compatible. In addition, the company has developed a COPS Product Development System (PDS) built around a 16-bit microprocessor, 32k-byte RAM, and 12k bytes of ROM-P/ROM firmware. Easing programming, the disc based system features an editor and assembler to handle source code entry, convert to object code, and maintain documentation.

Plug-in ROM Software Converts Computer Into Z80 Development System

The Sorcerer microcomputer with CRT can be turned into a cassette based Z80 development system with the Development PAC™ software package. While not a complete system for major development programs, it does offer an alternative for smaller users or manufacturers seeking lower cost development of Z80 software packages. Upgrading to an Exidy disc system while maintaining tape file compatibility is possible through the CP/M operating system via a software package that converts tape files to disc.

A Designer's Debugging Tool (DDT), line oriented text editor, relocating assembler, and linking loader are the four modules in the package; all operate with the computer's dual cassette interface to allow tape based system development. With the

You can count on experience. Beehive has been a forerunner in the terminal marketplace since 1968 when we were known as Beehive Electrotech and had only one terminal product.

Beehive has pioneered terminal graphics, the use of microprocessors and was the first to develop the concept of CRT modularity. We have remained firmly entrenched within diverse, growing and rapidly changing markets by utilizing a planned and calculated approach to the design and development of a reliable terminal product array that now ranges from dumb to very smart, from standard to custom. At the same time, we have not lost sight of our

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most important asset, you the customer. Quality is just part of the package.

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CIRCLE 87 ON INQUIRY CARD

161

MICRO DATA STACK

COMPUTERS, ELEMENTS, AND SYSTEMS

DDT, the user can display and modify any RAM location or Z80 register. It allows single breakpoints to be set and includes a hexadecimal calculator for programming relative and indexed addressing instructions.

Lines of source code or text may be entered, changed, deleted, or moved using the editor. It also features built-in automatic tabbing. The 2-pass assembler permits relocation and supports global symbols. Output is in standard Intel hexadecimal format. The relocating linking/loader module permits the programmer to design large programs in smaller modular subsystems, debug them separately, and then link and relocate

them to their final executable memory locations.

To ease programming, Exidy Data Systems, 969 W Maude Ave, Sunnyvale, CA 94086, has incorporated modular construction of various length programs and global (external) symbols for intermodule communication. Further, the concept of predefined symbolic addresses for Z80 registers, I/O device vectors, and other frequently used memory locations is carried over as well into the RAM, which is partitioned so that two predefined buffers can be addressed as if they were devices for storing either source or assembled object code. Circle 413 on Inquiry Card

Emulator Terminal For Six μ Processors Speeds Development Times

MicroSystem Emulator-Series 2000 connects to a host computer, allowing that computer to act as a hardware and software development system for the 6800, 6802, 8048, 8080, 8085A, and Z80—all emulated microprocessors. Future support will cover the 8049, 8041, 8039, 8035, and 8748. Even dedicated development systems from Intel, Motorola, and Zilog can support any of these six microprocessors with the addition of this

terminal. The keyboard can also be used as a standalone instrument to share the host's resources among several users.

Capabilities of the 8-bit emulator are realtime operation at speeds up to 6 MHz, optional realtime trace, and DMA operation. The unit also includes a high speed serial data link. The 8k of RAM used during debugging allows the user to download programs for execution in the emulator. Manufactured by Millennium Systems, Inc, 19020 Pruneridge Ave, Cupertino, CA 95014, the terminal performs software and hardware integration. Circle 414 on Inquiry Card



Host computer acts as multiprocessor development system with addition of Millennium Systems Series 2000 emulator that uses discrete microprocessor cards

Modular Board Offers Multicommunications Over Range of Baud Rates

Synchronous and asynchronous communications are handled by the 6-port EIA/RS-232 board that contains a Zilog Z80A-sio/0 IC and two realtime clocks that are programmable in several modes. Meeting proposed IEEE S-100 standards, the board configures for two, four, or six channels with or without the realtime clocks. Asynchronous baud rates are 150 to 38.4k, and internal synchronous baud rates are 9.6k, 19.2k, 76.8k, and 614.4k.

Functions performed by the board include both async parity generation/checking and sync CRC generation/checking CRC-16 or CCITT, as well as support of SDLC, HDLC, and Bisync protocols. Inco, Inc, 7916 Westpark Dr, McLean, VA 22102, has suited the unit to both multiple terminal to computer and computer to computer communications. The receiver section has triple buffering of errors and data. Power requirements are 8 V at 1 A and ± 16 V at 0.3 A.

Circle 415 on Inquiry Card

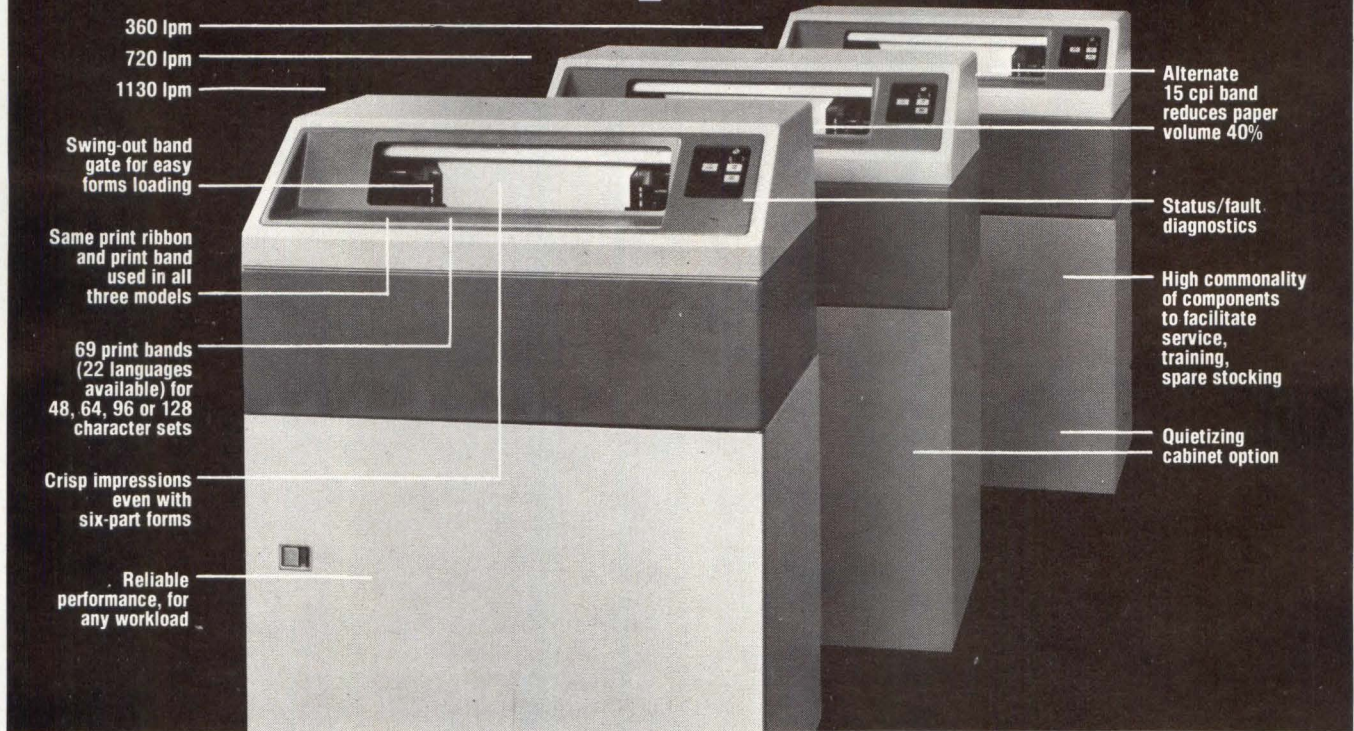
Development Lab Support Emulates MCS 48 Family At Full Speed

An emulator board and prototype control probe for the 8001/8002A Microprocessor Development Labs (MDL) support the Intel MCS 48 family of 8048, 8049, 8039, 8035, and 8021 devices (with an adapter), aiding designs incorporating these microcomputers in new products or in products upgraded from hardwired TTL or 4-bit processors. The 8039 and 8035 processors can be emulated to their full 11-MHz rating, whereas they were previously limited to support at 6 MHz.

The added external probe on the MDL's optional Realtime Prototype Analyzer enables checking of other chips in the system, along with the 8048 circuit in a realtime mode. Tektronix, Inc, PO Box 500, Beaverton, OR 97077, has scheduled delivery by February 1980. Support for the 8041A and 8022 members will be available in the first quarter of 1980.

Circle 416 on Inquiry Card

Quality impressions are made easily with OEM band printers from CDC



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Swing-out band gate for easy forms loading

Same print ribbon and print band used in all three models

69 print bands (22 languages available) for 48, 64, 96 or 128 character sets

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If you're an OEM, you already know what Control Data has done for disk technology. Now we're determined to earn the same reputation for excellence in band printer technology. By giving *you* versatility and maintainability. By giving *your customer* reliability, superior print quality and economical operation.

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High transfer rate, up to 48,000 bits-per-second...

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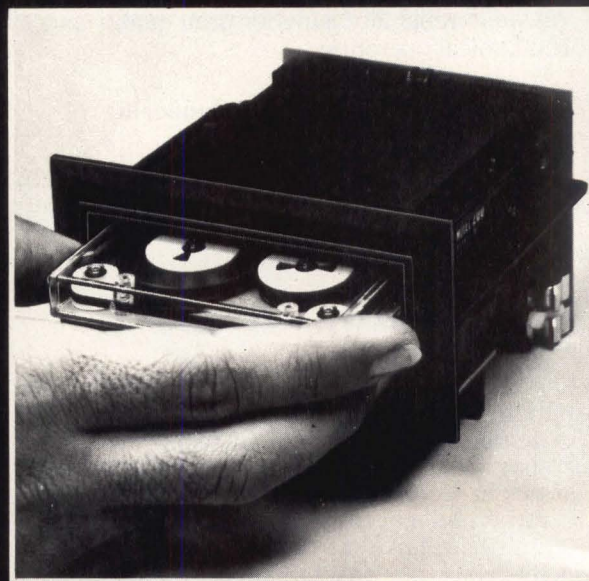
Flexible configurations range from basic OEM building blocks to complete tape memory systems...

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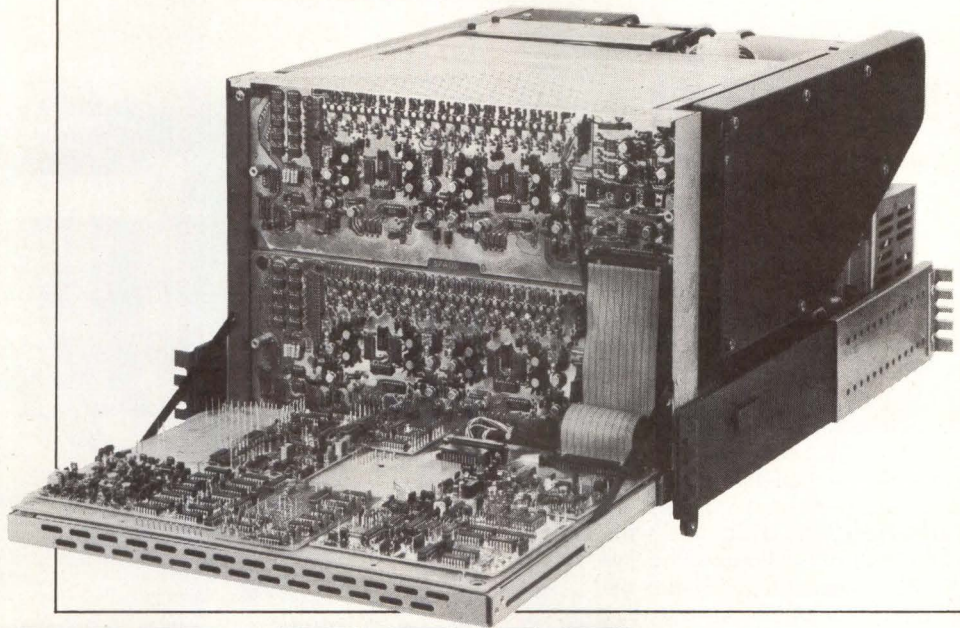
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VRC MODEL 4016 MEMORY

When it comes to speed, reliability and low cost, systems users in 25 countries in every continent of the world depend on the VRC 4016 head-per-track memory.

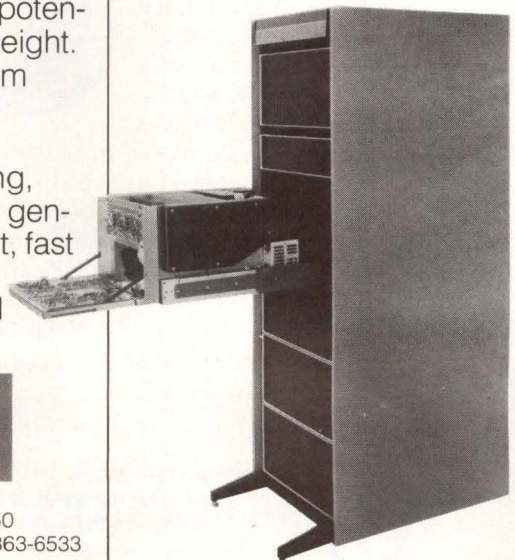
It features a fail-safe actuation system that eliminates the potential of media damage and data loss. It's compact and lightweight. All electronics, drive components and head retraction system are mounted outside the drum, making service simple and eliminating risk of contamination.

Applications are endless. Telecom and message switching, process control of all kinds, geophysical exploration, power generation, news editing, typesetting. Wherever low cost-per-bit, fast access and high data storage capacity are required.

For proven reliability, worldwide support, field service and predictable high quality, you can rely on VRC.

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MEAN TIME TO REPAIR . . . Less than 1 hr.



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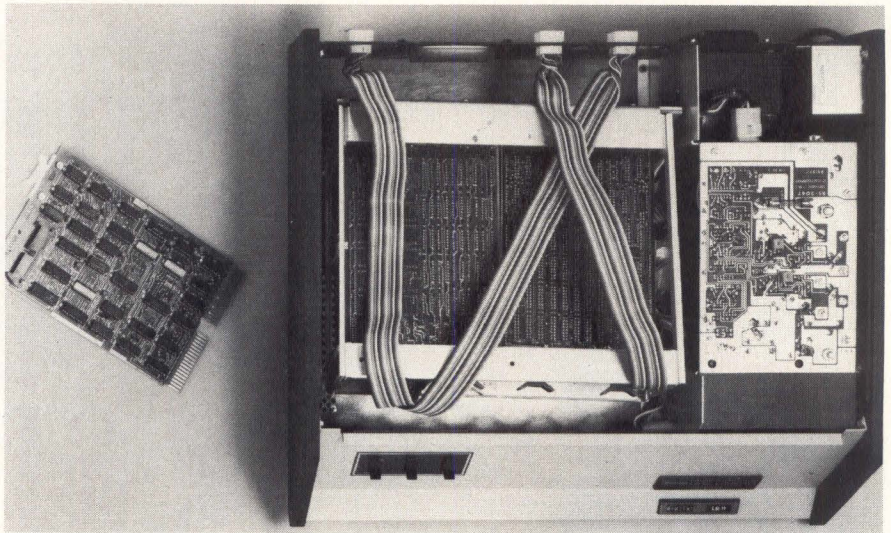
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CIRCLE 133 ON INQUIRY CARD

16-Bit Computer Combines Low Cost Elements For Business Functions

The 16-bit WH11A mainframe and WH27 dual-drive floppy disc system, enhanced by operating system software, video terminal, and accessory components (16k RAM and serial interface UART), are interchangeable with Digital Equipment Corp's PDP-11/03 16-bit mainframes and system components. Heart of the system is the WH11A which features the DEC KD11 HA half-size CPU board. Initial memory must be added for basic operation. The 512k-byte WH27 is a Z80 controlled floppy disc system. Fully compatible with the DEC RX 01, this system adds self-test diagnostic on power-up, a mechanical interlock, a write-protect function, and a reformatting procedure for writing in IBM 3740 standard format.

Heath Data Systems, PO Box 167, St Joseph, MI 49805, supplies the



At lower cost, 16-bit WHS11A small business computer improves performance over compatible DEC PDP-11/03 computers and system components. Shown with cover removed, Heath's WH11A is basis of system, housed in card cage with heavy duty switching power supply; backplane holds up to seven memory and I/O accessory cards in addition to DEC's KD11 HA CPU

BELTING INDUSTRIES'...
Semi-Stretch Belt Users All Say —

"THANKS for the MEMORY"

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CIRCLE 134 ON INQUIRY CARD

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Final component for the system is a Z80 controlled WH19 video terminal with keyboard and 12-key numeric pad. The keyboard or computer can control 32 separate functions (see *Computer Design*, Dec 1979, p 124, 126). Compatible with the DEC VT52, the terminal prints the full upper and lower case ASCII character set. Advanced features that it offers include insert character mode, cancel character command, special graphic symbols, and 12 keyboard selectable baud rates.

Circle 418 on Inquiry Card



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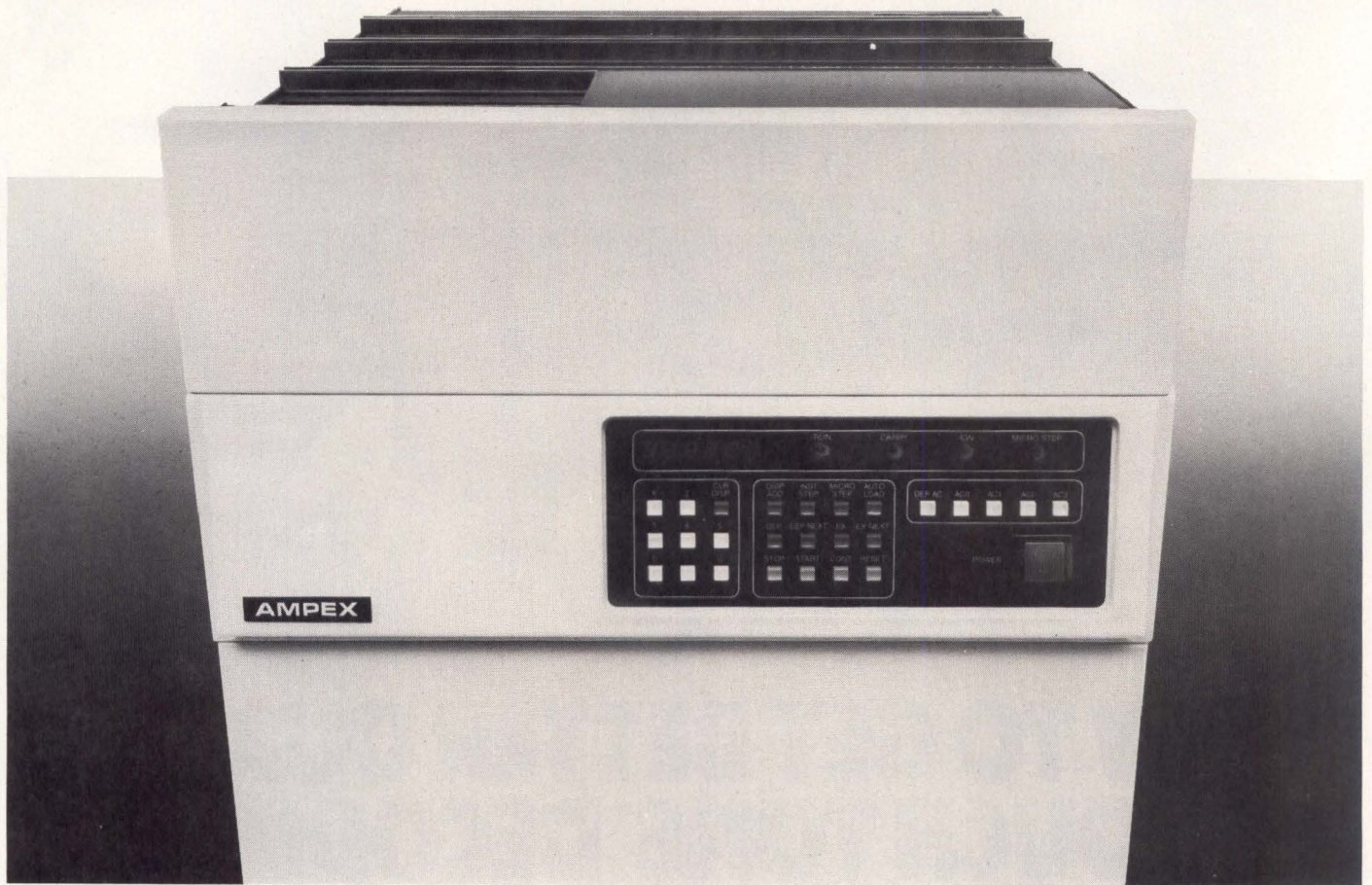
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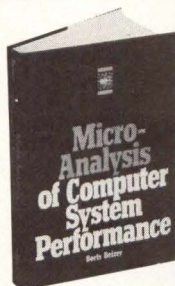
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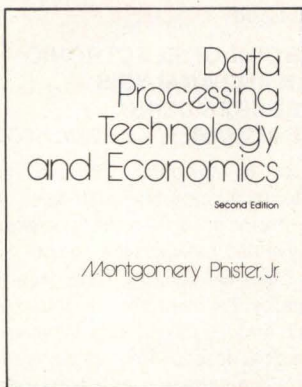
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CIRCLE 138 ON INQUIRY CARD

MICRO DATA STACK

COMPUTERS, ELEMENTS, AND SYSTEMS

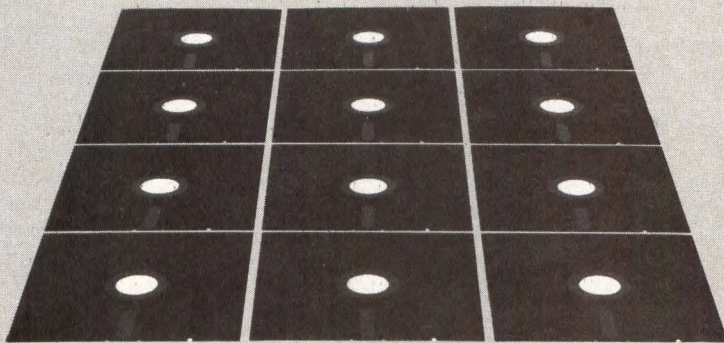
Floppy Disc Controller Interfaces LSI-11/23 With Shugart Disc Drive—Compatible with rx01, rx02, and 3740 media, mxv21 is offered by Micro Development Associates, 378 N Christine, Orange, CA 92669, with such features as transparent firmware bootstrap, 4-level interrupt/acknowledge programmability, and write protection during power transitions. (Circle 420 on Inquiry Card) . . . Serial/Parallel I/O Module Is EXORciser™ and Micromodule™ Compatible—Available from Creative Micro Systems, 11642-8 Knott Ave, Garden Grove, CA 92641, the 9622 combines two full-duplex asynchronous serial ports with rs-232-C conditioning, 12 8-bit parallel ports with control lines, and an onboard bit-rate generator with 14 standard rates. (Circle 421 on Inquiry Card) . . . 160-Char/s Printers Interface With TRS-80, Apple II, and PET Microcomputers—EX-800 series of MicroPrinters and MicroPlotters with built-in interfaces plug directly into the computers. Axiom Corp, 5932 San Fernando Rd, Glendale, CA 91202, has supplied the 801 with upper/lower case alphanumeric characters and graphic symbols; the 802 precisely aligns horizontal and vertical dot patterns. (Circle 422 on Inquiry Card)

Data Encryption/Protection Software Permits Multi-User Operation—Z80-DES is a high speed implementation of the NBS data encryption standard allowing throughputs of more than 6000 bits/s to provide secure links between home computers and remote data bases. Also announced by Interface Technology, PO Box 745, College Park, MD 20740, is a floating point arithmetic package consisting of 14 routines for the 9900. (Circle 423 on Inquiry Card) . . . Language Brings Pascal Together With File Handling Capabilities of CP/M™—Announced by Digital Marketing, 2670 Cherry Ln, Walnut Creek, CA 94596, Pascal/M™ for 8080/8085 or Z80 CPUs gives the user full access to CP/M data files written in other languages such as BASIC and stored under CP/M. All CP/M utilities are available for managing Pascal programs and files. (Circle 424 on Inquiry Card)

Microprocessor Solves Information Processing and Control Problems—Sampling of the 40-pin unsegmented AmZ8002 microprocessor has been announced by Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086. Hardware support for the 16-bit CPU includes the AMC 96/4016 evaluation board and Amsys™ 8/8 development system. (Circle 425 on Inquiry Card) . . . Single-Card Cache Memory Increases Total Throughput—PM-KK11A high speed 1k-word cache memory resides next to DEC's PDP-11/34A CPU to capture data from the Unibus™ during data transfers. With a write-through feature, the memory from Plessey Peripheral Systems, 17466 Daimler, Irvine, CA 92714, has a 450-ns cycle time and a 120-ns read hit access time. (Circle 426 on Inquiry Card) . . . Computer Peripheral Accepts Hand Printed Characters—Adapting to the user's style of hand printed characters, PrestoDigitizer™ for the Commodore PET™ recognizes the upper case alphabet, numerals, and punctuation marks. Innovision, PO Box 1317, Los Altos, CA 94022, has selected stroke direction and sequence as the parameters to be transmitted to the host processor. (Circle 427 on Inquiry Card) . . . Microcomputer Adds Software To Compete Against Minicomputers—COBOL with multikeyed ISAM and an IBM 2780/3780 emulator using BSC protocol and leased/switched telephone lines support the C8000 computer, manufactured by Onyx Systems Inc, 10375 Bandy Dr, Cupertino, CA 95014 (see *Computer Design*, July 79, p 169). This extends the microcomputer to advanced small business and distributed processing applications. (Circle 428 on Inquiry Card)

Multitasking Disc Operating System Expands Capabilities—Device independent (virtual) I/O, HEAP memory management for efficient I/O buffer memory allocation, and command indirection are minicomputer features provided by the WIZRD system. Wintek Corp, 1801 South St, Lafayette, IN 47904, offers the DOS separately or with the 48k dual-drive SPRINT 68 microcomputer. (Circle 429 on Inquiry Card)

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Meet the Mini Wini™ The new 8" fixed disk drive that stores 20 megabytes.

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SOFTWARE

Assembler Runs On Host That Is More Powerful Than Microprocessor

Creation of programs for the Motorola 6809 microprocessor on a Digital Equipment Corp PDP-11, DECSYSTEM-10, and -20 or Data General Nova and Eclipse results in multi-user capability, greater execution speed and peripheral handling capacity, and host system support of more sophisticated assembly language features. Each relocatable cross assembler is written in the host's assembly language, thus customizing it to the respective host computer.

Specific features of the cross assembler are relocation capability with base page relocatable and extended relocatable modes; testing of 14 conditions during conditional assembly, as well as an ELSE direc-

tive to handle the false condition; and macro facility including macro definition and redefinition, calls to other macros, and 10 or more levels of nesting for macros. Boston Systems Office, Inc, 469 Moody St, Waltham, MA 02154, further enhanced the assembler's capability with the addition of debugger support, assembly time error listing, listing format options, default radix control, and external and internal global symbols.

Indefinite repeat involves the application of macros to permit unlimited command string repetitions, including slight modifications. To incorporate source text from library files into the program, the user may employ the include directive. Lastly, local symbol block capability allows identically named symbols to be used to improve program clarity.

Circle 436 on Inquiry Card

Rigid Disc Software Enlarges Low Cost Microcomputing Concept

Development of the osm multiuser operating system for the 8" (20-cm) rigid MicroDisk™ has resulted in an integrated disc subsystem—drive, intelligent disc adapter/interface card, and software package—that plugs into 8080, 8085, or Z80 based S-100 bus microcomputer systems. Providing performance and formatted storage of up to 31.2M bytes at lower cost, the software offers high speed, keyed access to large files and creation of a multi-user environment.

The executive program operates on applications programs written in BASIC or assembly language, which is supported by an 8080 assembler using Intel's mnemonics. Besides the executive, the main OSM module resident in

digi-pad™ vs ??? PAD

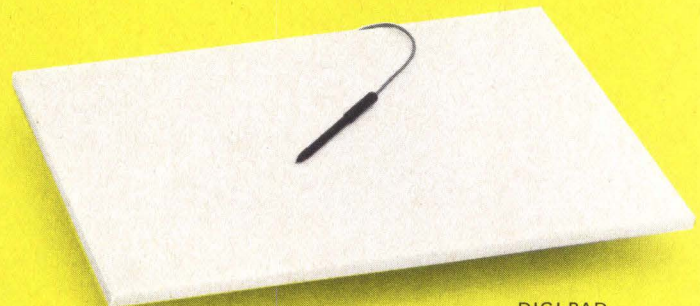
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Accuracy	± 0.005"	_____
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Tablet Warranty	2 Years	_____
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Digitizing Sensitivity	Thru 1" Thickness	_____
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Preventive Maintenance	None	_____
Quality	Industrial	_____
Unit Price	\$1685*	_____
Micro Option with Graphics Firmware**	Yes	_____

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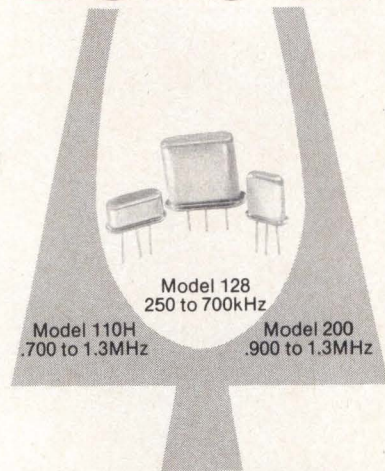
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MICRO DATA STACK

COMPUTERS, ELEMENTS, AND SYSTEMS

host computer memory includes programs for interrupt servicing, processor control, physical device drivers, logical device handlers, memory management, task management, program resource management, system supervision, and debugging programs.

Nonresident osm modules are loaded from disc when required. Among these are the Micropolis Disk Extended BASIC interpreter, an 8080 assembler, source text editor, and utilities for general system management. The operating system is compatible with the company's pds so that BASIC programs developed under either pds or osm will run under the other with very few changes. Data files may be transferred between MicroDisk and pds formatted floppy discs.

Micropolis Corp, 7959 Deering Ave, Canoga Park, CA 91304, has retained the same OEM hardware configurations. Storage capacities of 6.2M, 18.7M, and 31.2M bytes are offered with variations determined by the number of nonremovable 200-mm platters.

Circle 437 on Inquiry Card

Extensions Expand Pascal To Commercial/Industrial Microprocessor Uses

Language support of 8080 and 8085 software development on Intellec[®] microcomputer development systems has been introduced by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, in the form of the high level, structured Pascal-80 package. Extensions to the standard academic language include three data types—string type, untyped files, and interactive files—and 28 predeclared procedures and functions (variables for frequently used functions). Other facilities that aid development and maintenance of application programs are data type definitions, TRACE to monitor program execution, segmented procedure definitions for modular breakdown of large programs, and compile and runtime error diagnostics.

Developed under an exclusive license agreement with Queue Computer Corp of Berkeley, Calif, the software package includes a diskette with compiler, pseudocode interpreter, and demonstration programs that run under the ISIS-II operating system on

Intellec Series II and MDS-800 models. Source programs created using the software and development tools are converted to intermediate p-code by the compiler. The optimized pseudocode increases execution speed and saves memory space. The p-code is then executed by the interpreter.

Circle 438 on Inquiry Card

Async Package Transfers Data Between Mainframes And Microcomputers

Distributed processing capability can be applied to any Z80 based microcomputer system (MCZ) with an asynchronous communication package that allows data transfers to another MCZ or mainframe computer via telephone lines. A reduction in mainframe time and cost factors is effected as the programmers write, compile, debug, and test programs using the MCZ as a workstation and transferring the finished source program to the mainframe.

ASYNCH runs on the standard RIO operating system offered by Zilog, Inc, 10340 Bubb Rd, Cupertino, CA 95014. It operates using asynchronous ASCII communications; it does not support synchronous, 2780, or SDLC protocols.

A RIO hardware driver (\$SIBDRIVER) and an asynchronous protocol terminal emulator (COMM) comprise the \$500 package. With the communications driver, the user can write programs that communicate with other computer systems. It operates over an asynchronous serial port; this is provided by a serial interface board in the MCZ system, and by an auxiliary serial and parallel I/O board in a ZDS system. Input from the port is interrupt driven and characters are stored in an internal 256-byte circular buffer.

Using this driver as its interface, the emulator enables an operator at the system console to access a host system or transfer data and high level language source code files between the disc and host system. Alternatively, it transfers data from the host system to the printer. High level commands are used to set parameters, such as baud rate and parity, that affect data transfer. The mode that transfers procedure files between systems checks for errors and retransmits erroneous data. □

Circle 439 on Inquiry Card

WHEN IT COMES TO PUTTING IT ALL ON DISPLAY, THE ORION-60/S4 STANDS ALONE.



Magnavox combines the superior display and control features of the plasma-panel-based Orion-60 terminals with the powerful S4 Micro-Computer System.

The result is a stand alone graphics system that allows you the freedom to develop a wide variety of graphics application and development programs—while maintaining complete control over program storage, program-generated data, library routines and other facilities.

The Orion-60 display terminal offers full graphics with floppy-disc storage, as well as optional

rear-projection functions. It lets you create your own displays and enter data by simply touching the screen with your finger. So you can program your own character sets and generate vectors of any length to absolute coordinates. And because the Orion-60 is plasma-based, you'll get bright, high-contrast images free of jitter or distortion.

The S4 Micro-Computer has system software with development

capabilities that are as good or better than those found in many larger computer systems.

Features include CP/M* 8080 system utilities, Fortran with 32K RAM, and a full range of graphic utility routines including window, zoom, sub-image movement and rotation.

The Orion-60/S4.

For a demonstration, call or write Tyler Hunt at Magnavox Display Systems, 2131 South Coliseum Boulevard, Fort Wayne, Indiana 46803, (219) 482-4411.

Magnavox
DISPLAY SYSTEMS

*CP/M is a trademark of Digital Research.

CIRCLE 92 ON INQUIRY CARD

Implementing a Multifunction Network in LSI

Paul Chu

Fairchild Camera and Instrument
Mountain View, California

The bit-slice architecture examined in last month's column was made possible through advanced techniques in the large scale integration of emitter-coupled logic components. The subnanosecond 8-bit slice family using this architecture, developed through the best attainable compromise between semiconductor processing economics and packaging constraints, was designed to provide a set of flexible building blocks. Elements of that family are:

ADIU	Address and Data Interface Unit	F100220
MFN	Multiple Function Network	F100221
DAS	Dual Access Stack	F100222
PIU	Programmable Interface Unit	F100223
MSU	Microprogram Sequencer Unit	F100224

These devices provide a wide set of logic functions which may be utilized to construct ultra high speed computing systems. The flexibility that is provided in each component challenges the designer to exercise ingenuity, using the combination of functions provided, to develop high speed, sophisticated large scale integration (LSI) emitter-coupled logic (ECL) systems.

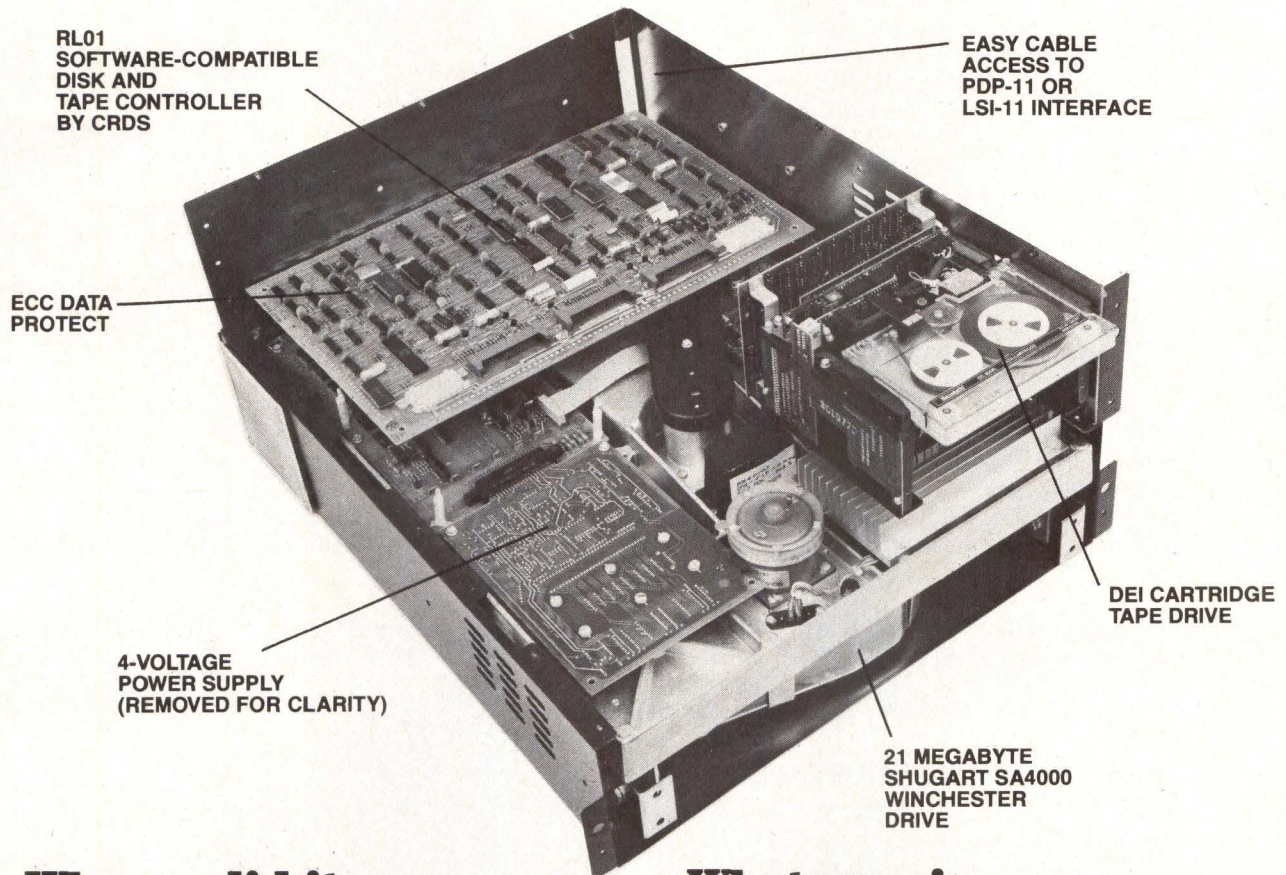
One significant attribute of a family of this kind is the combination of versatile and even widely differing kinds of operational capabilities within a component which enable it to fulfill a variety of roles in a single circuit

location, or for several such components of identical design to be utilized in a circuit, each in a specialized role, utilizing only part of the available functions. This kind of capability is well illustrated by the multifunction network (MFN), which combines an unusually diverse set of functions (Fig 1).

MFN Mode Control

Code	Operation
00	Bidirectional bus multiplexer/demultiplexer Four buses, A, B, C, or D can be routed to E or E can be routed to either of A, B, C, or D
01	ECC Assist Performs XOR and data move operations
10	Register/memory addressing Four 4-bit index registers and two 4-bit page registers form an indirect address
11	Multipoint file Four 5-bit latches

The inside story of our DEC-11[®] Winchester disk system with fail-safe cartridge tape back-up.



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MFN Functions

The MFN bit-slice component may act as a bus multiplexer and demultiplexer, transferring information from one bus to another. This MUX/DEMUX capability also makes the chip usable in data transfer between interfaces of differing widths, for instance, in parallel to serial or serial to parallel data conversion. In another mode, this component performs the function of an exclusive-or logic array for error correcting code (ECC). It finds use, furthermore, in register file addressing, accessing two 5-bit page registers and four 5-bit index registers. The four modes of operation are summarized in "MFN Mode Control."

All MFN buses are five bits wide. Ideally, buses for an 8-bit slice family would be nine bits wide, including eight data bits and one check bit. However, pin limitations on the package forced a compromise, resulting in the 5-bit path. In some cases this bus width finds use as a half byte of data (four bits) plus check bit. However, in general, MFNs can be combined to form a data path as wide as desired.

Bus Connections

The device incorporates 35 bidirectional bus drivers and receivers organized to interconnect five buses (A, B, C, D, and E), each five bits wide. Although the F bus is 12 bits wide (F_1-F_{12}), these bus bits are used in subgroups rather than as a single bus. They may be used either as controls or as data, depending on the operating mode selected by two control bits. A chip enable for drivers and one for receivers complete the controls. Four onchip 5-bit latch registers can be enabled to allow data to be propagated through them or

latched to match the inputs. Two additional 5-bit registers, A-latch and B-latch, are included and may be loaded by pulsing the clock input.

MUX/DEMUX Mode

Fig 2 illustrates the data flow paths and control bit combinations, that provide bidirectional bus operations in mode 0 for multiplexing and demultiplexing. The buses selected and the directions of information flow are illustrated by the bus select table in the figure.

Another function performed in this mode is an exclusive-or operation on data routed out on the E bus. When $F_1 = 0$, $F_4 = 0$, and $F_5 = 1$, bits F_6 and F_7 are used to select one of the four exclusive-or patterns illustrated in the table. This function may be used to invert one of the four bits on the E output.

One example of mode 0 operation is shown in Fig 3. In this specific example a 16-bit bus, D_0-D_{15} , is connected through four MFNs to another 16-bit bus whose outputs are E_0-E_{15} . A-E and E-A operations transmit the data through the MFN unchanged. The B-E operation is connected, in this case, to transmit the low four (ie, zoned decimal) bits of each 8-bit byte from the D_n inputs to the E_n outputs (ie, packed decimal).

$D_0-D_3 \rightarrow E_0-E_3$	} MFN
$D_8-D_{11} \rightarrow E_4-E_7$	
$D_{16}-D_{19} \rightarrow E_8-E_{11}$	
$D_{24}-D_{27} \rightarrow E_{12}-E_{15}$	
etc	} IN OUT
	} B→E

Conversely, a demultiplexer operation from E to B would take a packed decimal (four bits/digit) format

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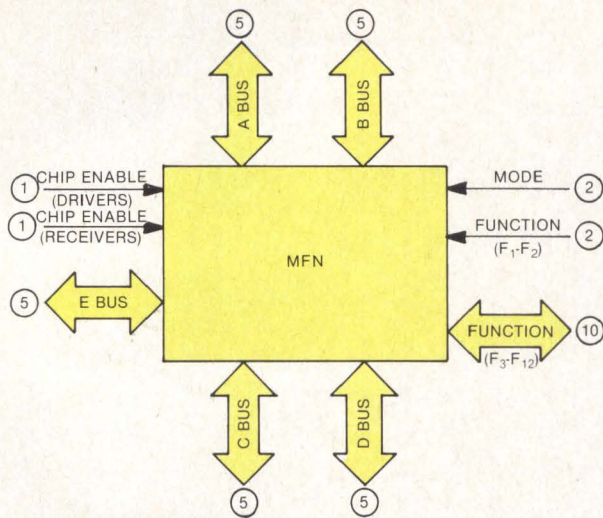
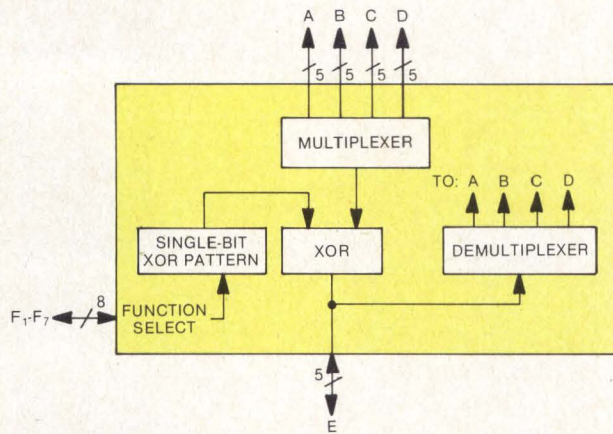


Fig 1 MFN block diagram. Multifunction network, MFN, is ECL bit-slice component that interfaces with five 5-bit buses. Device combines diverse capabilities



REGISTER SELECT			
F ₁	F ₂	F ₃	
0	0	0	A→E
0	0	1	B→E
0	1	0	C→E
0	1	1	D→E
1	0	0	E→A
1	0	1	E→B
1	1	0	E→C
1	1	1	E→D

FUNCTION SELECT		SINGLE-BIT XOR PATTERN			
F ₁	F ₄	F ₅	F ₆	F ₇	
0	0	1	0	0	1
0	0	1	0	1	0
0	0	1	1	0	1
0	0	1	1	1	0

Fig 2 Bidirectional bus multiplexer and demultiplexer. In mode 0, MFN operates as bus MUX/DEMUX. Exclusive-OR function is also performed in this mode

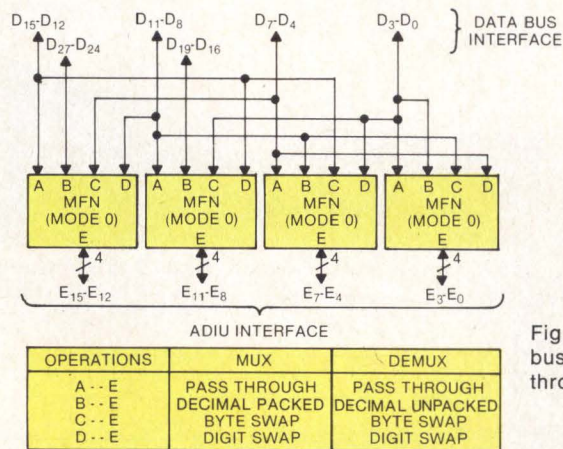


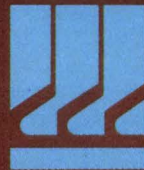
Fig 3 Data alignment operation using bidirectional bus multiplexing. Two 16-bit buses are connected through configuration of four chips

OPERATIONS	MUX	DEMUX
A--E	PASS THROUGH	PASS THROUGH
B--E	DECIMAL PACKED	DECIMAL UNPACKED
C--E	BYTE SWAP	BYTE SWAP
D--E	DIGIT SWAP	DIGIT SWAP

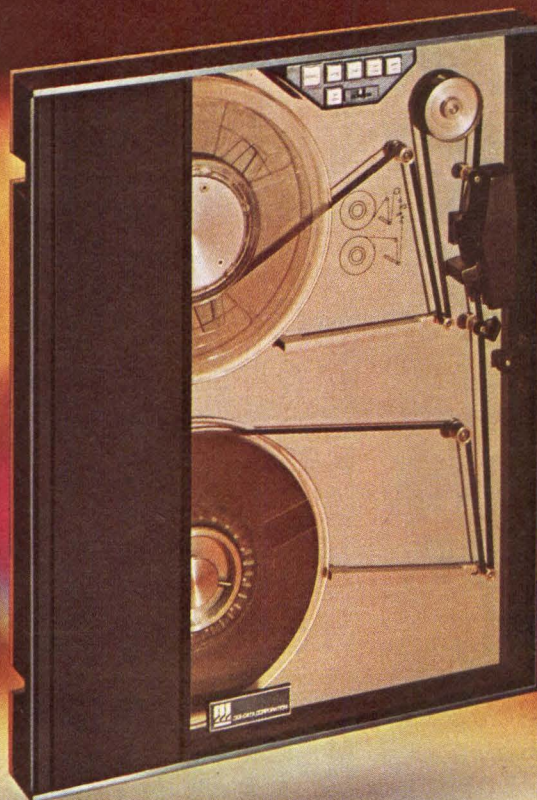
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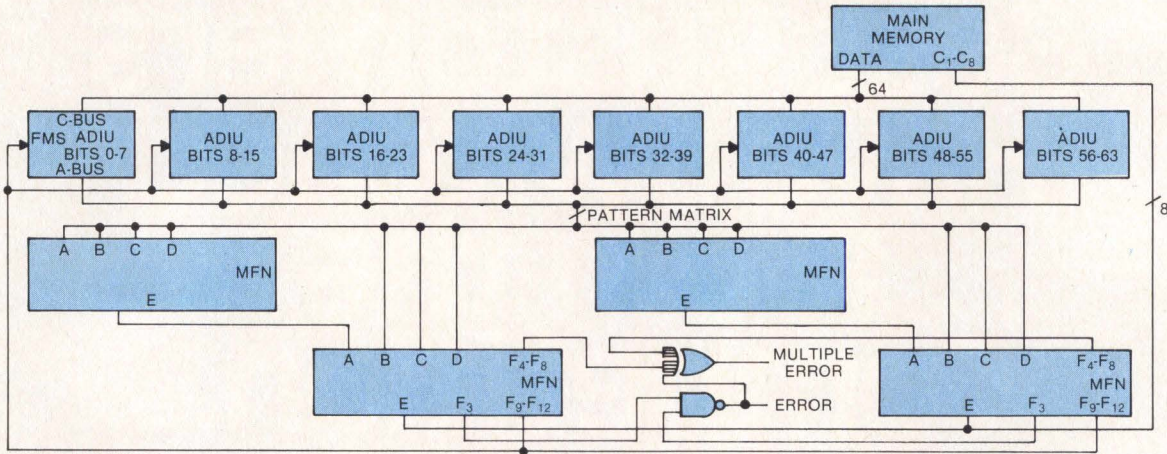
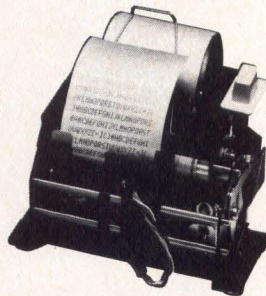


Fig 4 Mode 1 error correction. MFNs and ADIUs operate together in error correction for 64-bit data word, utilizing check and syndrome bits



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and place the decimal code in the low four bits of each 8-bit byte on the B bus. In this example, the fifth bit is not utilized.

An 8-bit byte swap operation is illustrated by connection of the following for a C-E operation:

$$\left. \begin{array}{l} D_0 - D_3 \rightarrow E_8 - E_{11} \\ D_4 - D_7 \rightarrow E_{12} - E_{15} \\ D_8 - D_{11} \rightarrow E_0 - E_3 \\ D_{12} - D_{15} \rightarrow E_4 - E_7 \\ \text{etc} \end{array} \right\} \begin{array}{l} \text{MFN} \\ \text{IN OUT} \\ \text{C} \rightarrow \text{E} \end{array}$$

Demultiplex operation, E to C, would also swap bytes.

A 4-bit group swap in each byte occurs in the D to E operation.

$$\left. \begin{array}{l} D_0 - D_3 \rightarrow E_4 - E_7 \\ D_4 - D_7 \rightarrow E_0 - E_3 \\ D_8 - D_{11} \rightarrow E_{12} - E_{15} \\ D_{12} - D_{15} \rightarrow E_8 - E_{11} \\ \text{etc} \end{array} \right\} \begin{array}{l} \text{MFN} \\ \text{IN OUT} \\ \text{C} \rightarrow \text{E} \end{array}$$

Demultiplex operation, E to D, would also swap 4-bit groups.

ECC Assist Mode

As indicated in last month's article, the ADIU encodes ECC parity bits. If a single-bit error is detected by the MFN logic, the byte-slice ADIU containing the incorrect bit can be selected and directed to decode a 3-bit address on one of its buses to invert and correct that bit. Fig 4 shows eight ADIUs and four MFNs used in error correction for a 64-bit data word. Together they perform the following functions: generate check bits and write them into memory with data; read from memory, using data and check bits to generate syndrome bits; and use syndrome bits to correct data in ADIU.

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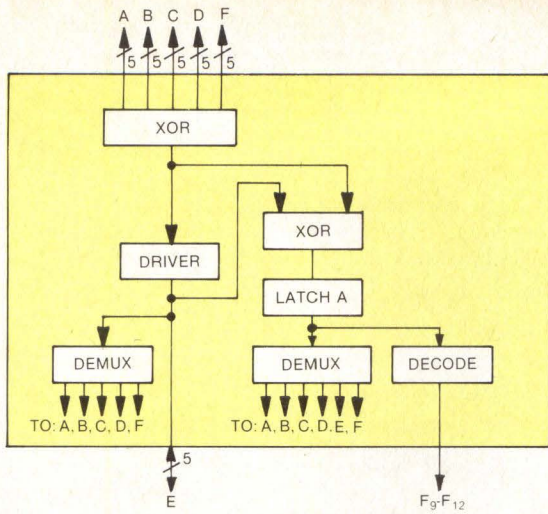
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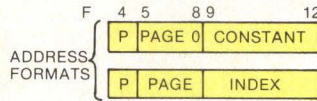
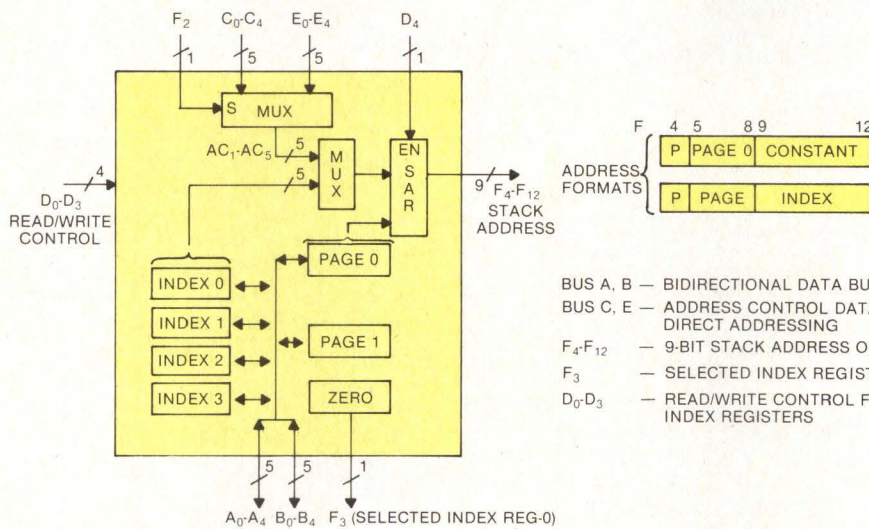


F_1 - F_2 —FUNCTION CONTROL
 F_3 —NO ERROR INDICATION
 F_9 - F_{12} —BYTE IN ERROR
 BUS A, B, C, D—ENCODED BIT IN ERROR

FUNCTION SELECT		FUNCTION
F_1	F_2	
0	0	DO NOTHING
1	0	$A \nabla B \nabla C \nabla D \nabla E \nabla F$ TO OUTPUT OF LATCH A
0	1	$A \nabla B \nabla C \nabla D \nabla F$ TO E
1	1	E TO A, B, C, D, F

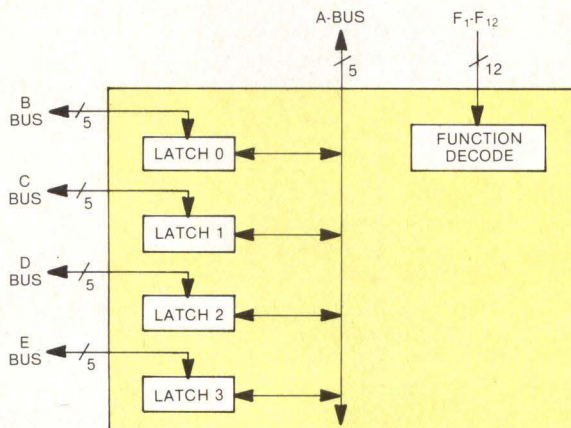
\uparrow = LEADING EDGE
 ∇ = EXCLUSIVE - OR

Fig 5 MFN ECC assist. Error correction circuits in multifunction network are based on exclusive-OR logic



BUS A, B — BIDIRECTIONAL DATA BUS
 BUS C, E — ADDRESS CONTROL DATA FOR DIRECT ADDRESSING
 F_4 - F_{12} — 9-BIT STACK ADDRESS OUTPUTS
 F_3 — SELECTED INDEX REGISTER EQUALS ZERO
 D_0 - D_3 — READ/WRITE CONTROL FOR PAGE AND INDEX REGISTERS

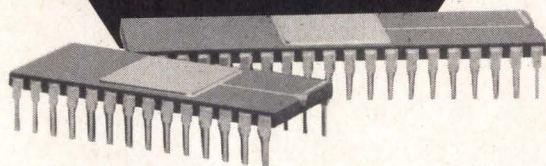
Fig 6 MFN register stack addressing. In mode 2, register stack addressing is carried out by MFN. Operation makes use of six onchip 5-bit latch registers



F_1 - F_2 —SELECT LATCH 0-3 VIA A-BUS
 F_3 —LATCH ENABLE VIA A-BUS
 F_4 - F_7 —SEPARATE WRITE ENABLES FROM B, C, D, E TO LATCH 0, 1, 2, 3
 F_8 —BUS ENABLE ONTO A-BUS
 F_9 - F_{12} —SEPARATE BUS ENABLES FOR BUS B, C, D, E

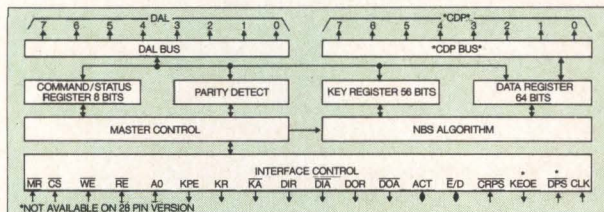
Fig 7 MFN multiport file. Mode 3 utilizes MFN as 4-latch data file. This mode also allows data transfers between buses of differing widths

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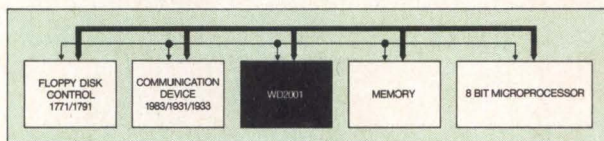


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Fig 5 illustrates the data path and logic functions of the MFN that are used in mode 1. The MFN utilizes exclusive-OR logical operations to assist the ADIU chip in carrying out error correction functions.

Register/Memory Addressing

In the addressing mode (Fig 6), bidirectional A and B buses load and access six onchip 5-bit latch registers, four of which are "index registers," the other two being "page registers." These operations are carried out in various combinations under the control of D-bus inputs as follows:

- (1) Read index registers
- (2) Sense selected index register value = 0
- (3) Read page registers
- (4) Load page registers and index registers

Inputs C₀-C₄ and E₀-E₄ serve as two sets of five bits of address selection control which, when selected by F₂ and output from the mux, are referred to as AC₁-AC₅. Input D₄ controls the loading of the stack address register. Lines F₄-F₁₂ function as a 9-bit output bus used for direct or indirect addressing.

Multiport File

When mode 3 is used, the chip functions as a multiport file (Fig 7). This mode provides four 5-bit latches, accessed or loaded by the bidirectional buses. Also data can be transferred in this mode between buses of differing widths, as all four latches are accessible by a common bus (A) and a dedicated bus (B, C, D, E). Latches B, C, D, E can be loaded simultaneously. Later simultaneous or separate readouts may occur on the respective buses. Other uses include serial readin/parallel readout or parallel readin/serial readout.

Serial readin/parallel readout

In:

- (A)0 → (LATCH 0)
- (A)1 → (LATCH 1)
- (A)2 → (LATCH 2)
- (A)3 → (LATCH 3)

Out:

- (LATCH 0) → B, (LATCH 1) → C,
- (LATCH 2) → D, (LATCH 3) → E

Parallel readin/serial readout

In:

- B → (LATCH 0), C → (LATCH 1),
- D → (LATCH 2), E → (LATCH 3)

Out:

- (LATCH 0) → A
- (LATCH 1) → A
- (LATCH 2) → A
- (LATCH 3) → A

Summary

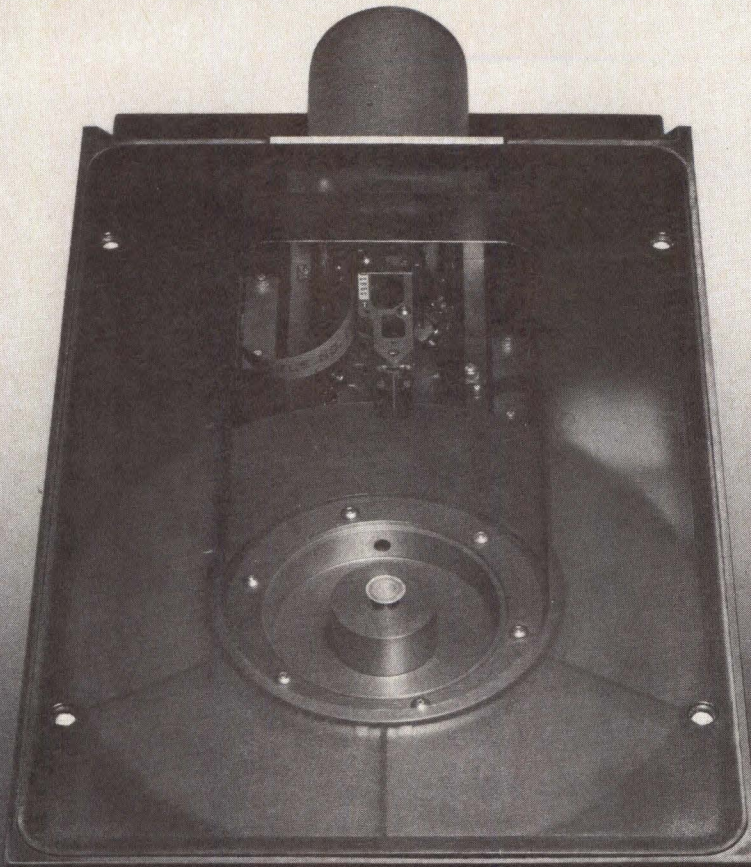
The multifunction network is a diversified member of the Fairchild 8-bit slice family, providing a flexible set of functions in an LSI ECL component. The device's utility is illustrated by the fact that its use as a bus multiplexer involves a propagation delay of 8 ns (typ). Offering the options of functioning in several modes or in a single specialized mode, a chip with this kind of versatility allows the component manufacturer to operate on a standard part basis, thereby achieving higher volume production, and, consequently, reductions in component pricing.

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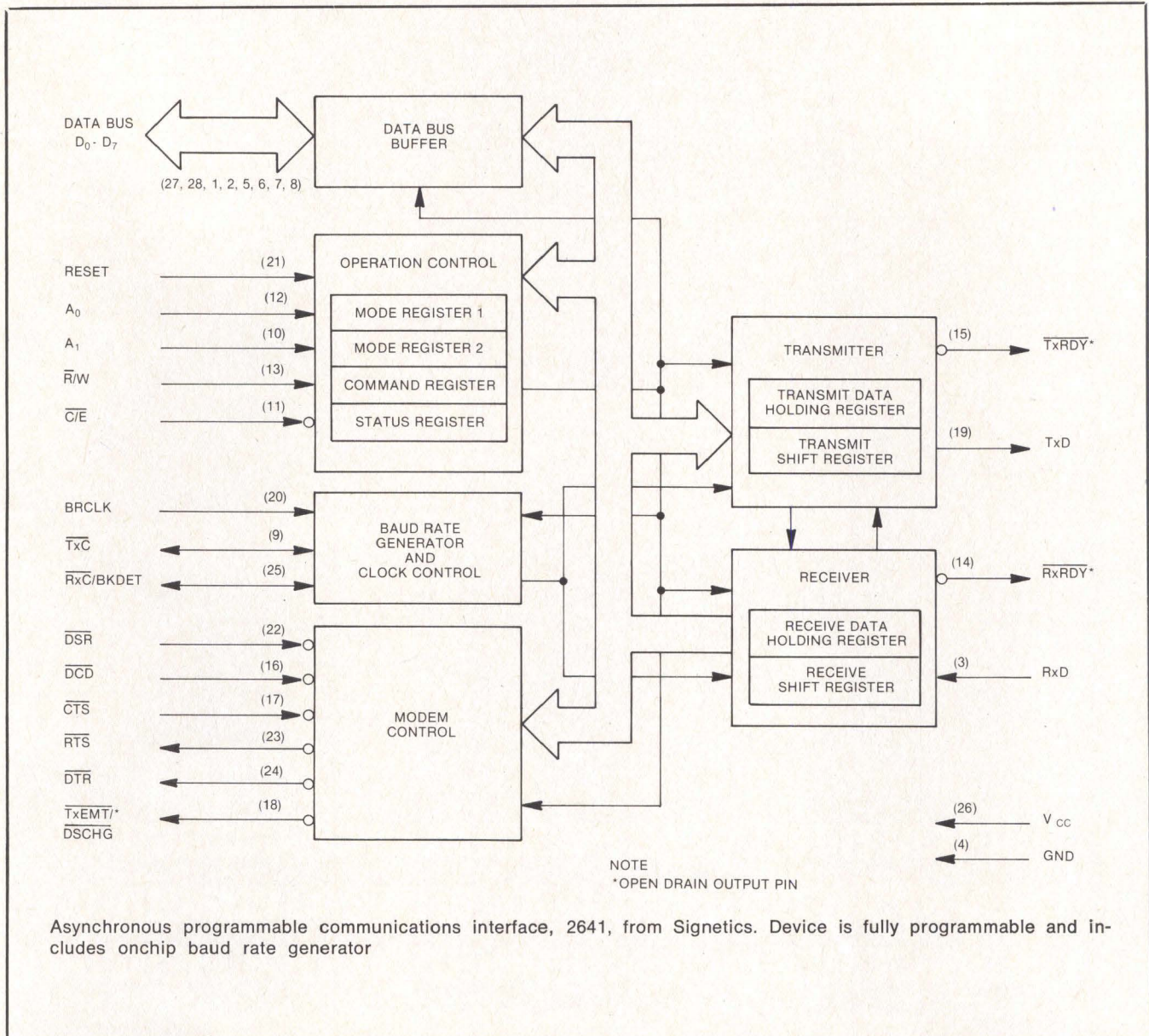
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UART Interfaces to 8-Bit Microprocessors In Data Communications Control Function

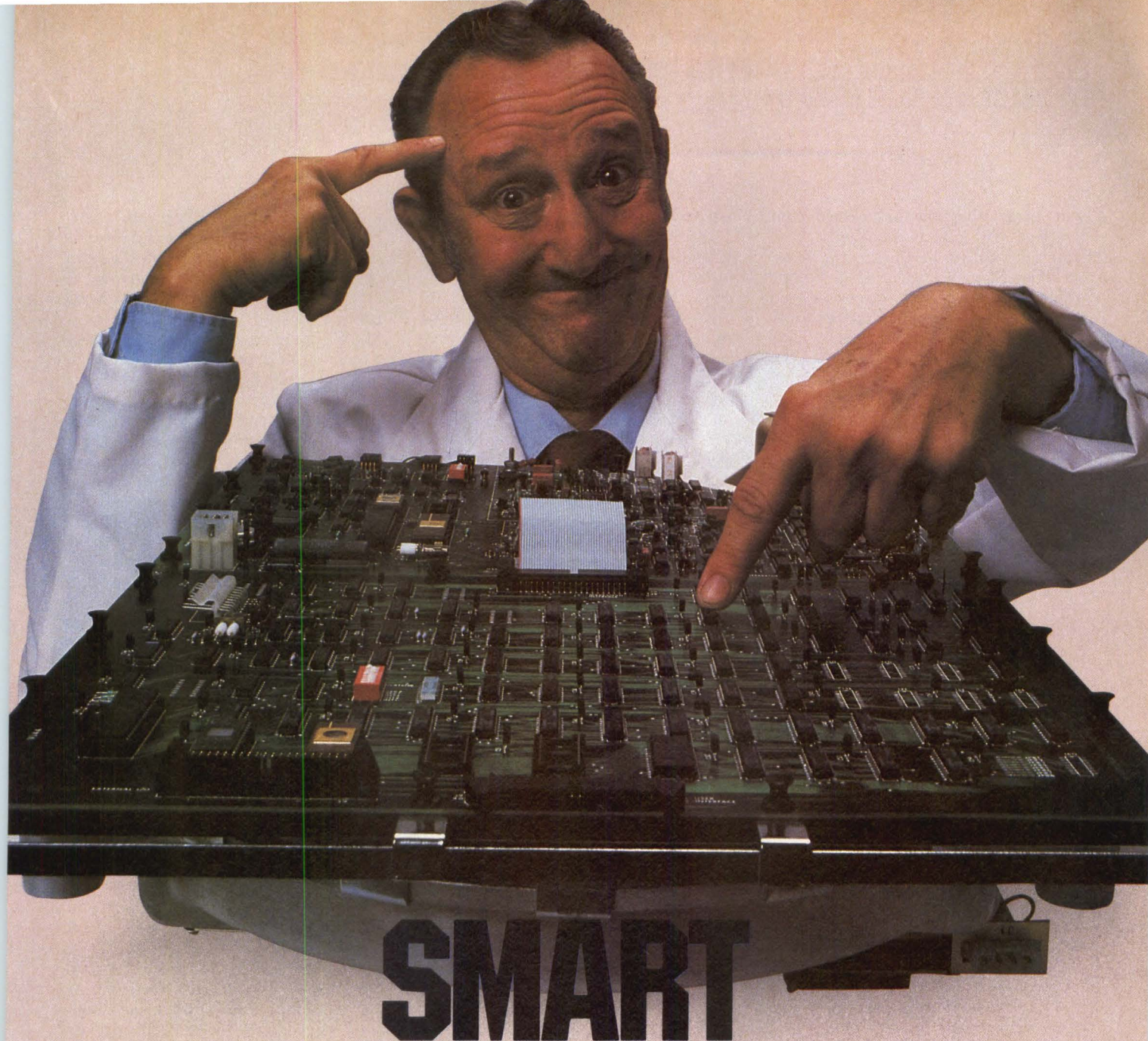


Usable in a polled or interrupt-driven system environment, the 2641 universal asynchronous data communications controller chip interfaces directly to most 8-bit microprocessors. The device from Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086, accepts programmed instructions from the microprocessor while supporting asynchronous serial data communications in full- or half-duplex mode.

This UART serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert them into parallel data characters for input to the microcomputer. It contains a baud rate generator that can be programmed either to accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud

rates can be selected under program control during operation in the internal clock mode. Uses for the chip are found in front end processors, network processors, intelligent terminals, serial peripherals, and remote data concentrators.

The device consists of five major sections: the receiver, transmitter, timing, operation control, and modem control. These sections communicate



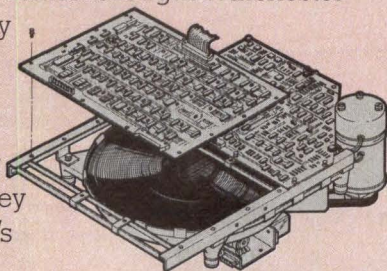
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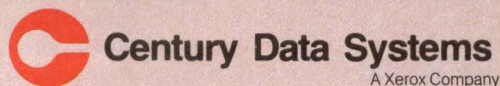


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with each other via an internal control bus and an internal data bus, which interfaces to the microprocessor data bus by means of a buffer.

Serial data enter the receiver, which converts them to parallel format, checks for certain errors, and sends an assembled character to the CPU. The transmitter accepts parallel data from the CPU, appends start and stop bits and, optionally, a parity bit, and outputs a composite serial data stream.

An onchip baud rate generator is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. This unit can generate 16 commonly used baud rates, any one of which can be selected for full duplex operation.

The operation control block stores configuration and operation commands from the CPU and generates signals appropriate to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus, and contains mode registers 1 and 2, as well as the command and status registers. The modem control section provides interfacing for three input and three output signals used for handshaking and status indication between the CPU and a modem.

Prior to the start of data communications, the operational mode must be programmed through write operations input to the mode and command registers. The UART can be reconfigured at any time during program execution. The mode registers define the general operational characteristics, while the command register controls the operation within this basic framework.

Bits MR10 through MR17 are inputs to mode register 1. When external clock input option is selected, a pair of bits (MR10/11) select a baud rate multiplier of 1X, 16X, or 64X. Inputs MR12/13 select a character length of 5, 6, 7, or 8 bits. Another input bit (MR14) controls parity generation, enabling or disabling the addition of a parity bit to the transmitted character and the performance of a parity check on incoming data. Bit MR15 determines whether this parity is to be odd or even. The final pair of control bits,

MR16/17, select character framing of 1, 1.5, or 2 stop bits. If 1X baud rate is programmed, 1.5 stop bits defaults to 1 on transmit. Those bits in the mode register that affect character assembly and disassembly (MR12-16) can be changed dynamically during active receive/transmit operation.

Mode register 1 must be written before mode register 2, which need not be programmed if external clocks are used. In the absence of external clocks, inputs to mode register 2 control the frequency of the internal baud rate generator.

A pair of input bits to the command register allow the enabling or disabling of the transmitter or receiver. Other bits entering this register govern such functions as the resetting of error flags in the status register and the choice of four operational submodes.

Additional features of the chip include TTL compatible I/O, single 5-V power supply, and three open drain MOS outputs which can be wire-ORed. There are capabilities for parity, overrun and framing error detection, line break detection and generation, and false start bit detection.

Constructed using proprietary n-channel silicon gate depletion load technology, the device is provided in a 28-pin DIP and is pin compatible with the 2651 USART by the same manufacturer. Absolute maximum ratings limit operating ambient temperature to a 0 to 70 °C range, and storage temperature to a -65 to 150 °C range. All voltages with respect to ground must lie between -0.5 and 6.0 V.

Circle 350 on Inquiry Card

ICs Drive Displays In Dot or Bar Mode

A single pin change in an integrated circuit converts a moving dot display to a bar graph display. The LM3914 series of monolithic display drivers from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, are capable of driving

LEDs, incandescent bulbs, vacuum fluorescent displays, or liquid crystal displays. Readout can be linear, log, or VU. Family members include a 10-step linear model (3914), a logarithmic version (3915) that covers a 30-dB range in ten 3-dB steps, and a volume unit version (3916) covering a range of 3 to -20 VU.

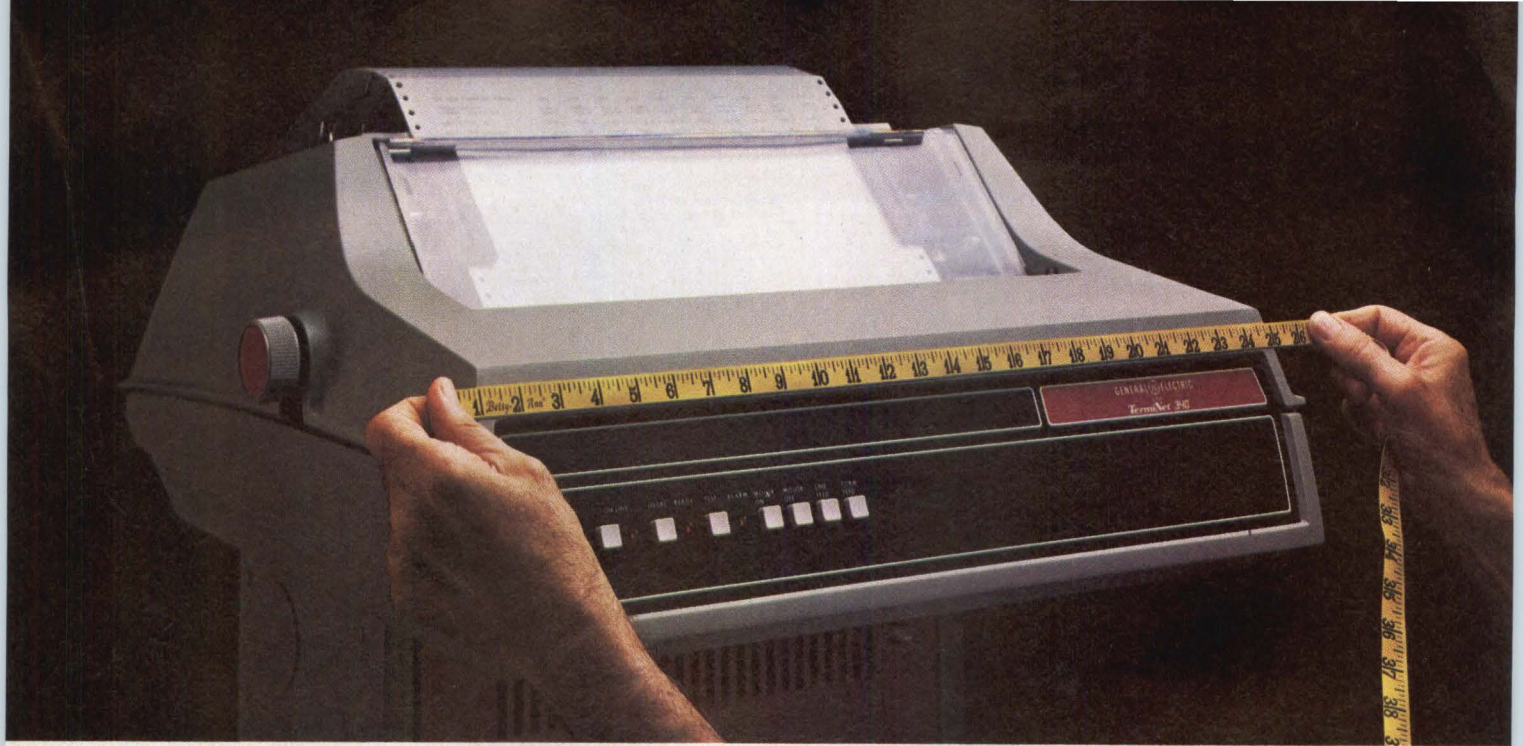
The manufacturer indicates that this family makes electronic driver/display combinations competitive with mechanical meters. Multiple devices can be cascaded for a dot or bar mode display with a range of 60 to 90 dB. Furthermore, the decibel version can be cascaded with linear versions for a linear/log display or with VU versions for an extended range VU meter.

These are large scale ICs, each containing 10 precision comparators, with a divider to give millivolt accuracy at each trip point, a built-in voltage reference, bar-dot logic circuitry, and constant current output drivers. It can be operated from power supplies from 3 to 20 V, and is easily scaled to accept signals from millivolts to volts. In addition, the devices are protected from input overvoltages to ± 35 V.

The output current from free collector transistors can be programmed from less than 1 mA to over 20 mA, and the signal input buffer boasts a guaranteed 50-nA max input current. This allows the device to be used even with high impedance sources. Another advantage of the family is the ease with which the devices can be expanded to 50 or more outputs for high resolution displays. For example, the logarithmic version can easily be used to monitor a range of audio signals wider than 90 dB.

Additional characteristics include internal voltage reference from 1.2 to 12 V, current-regulated open collector outputs with output current programmable from 1 to 30 mA, and the capability for directly driving TTL or CMOS. The internal logic allows chaining even in dot mode. Dot mode displays and low supply voltages make the devices useful in battery operated applications.

Rated for operation over a 0 to 70 °C temperature range, the series is suitable for audio and instrumentation displays, as well as in electronic controllers. All versions are provided in 18-pin DIPs.



Solid engineering and 340 lpm speed make the TermiNet 340 a more rugged, productive line printer.

Don't let the compact size of the General Electric TermiNet 340 line printer fool you. Because no matter how hard you work it, it won't quit on you. It's that tough, that dependable and that much better than typical line printers. And it's available now.

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From top to bottom, the compact TermiNet 340 line printer is engineered with long-life components designed to keep the printer on-line. And businesses on schedule.

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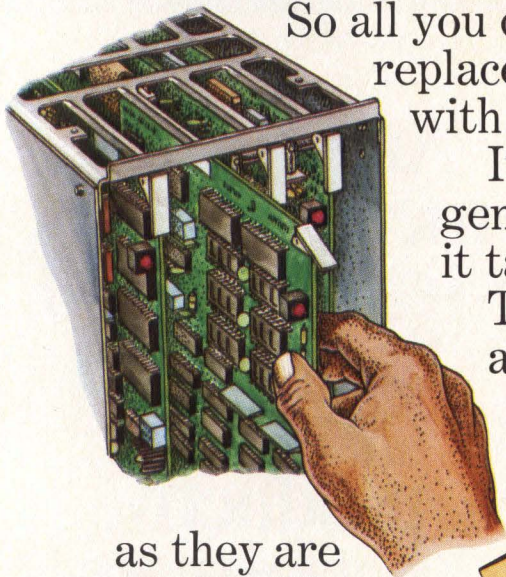
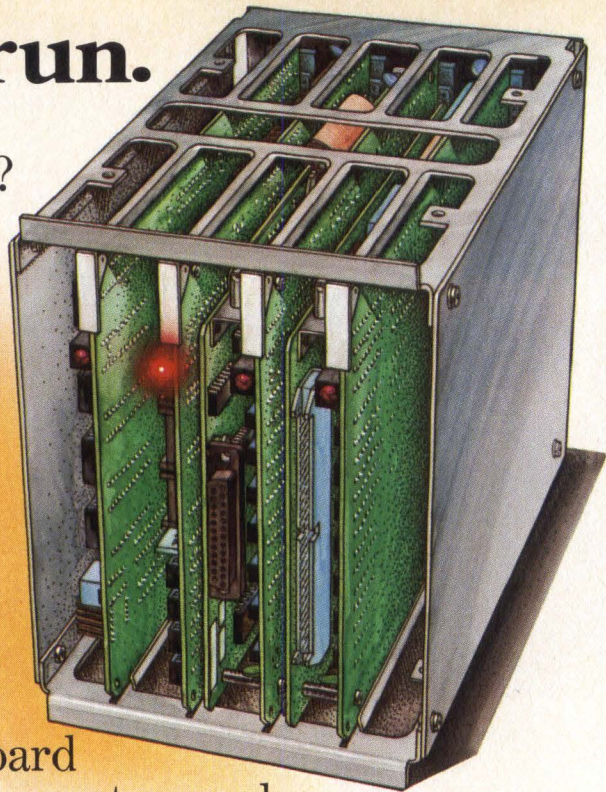
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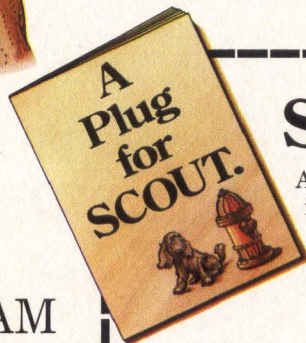
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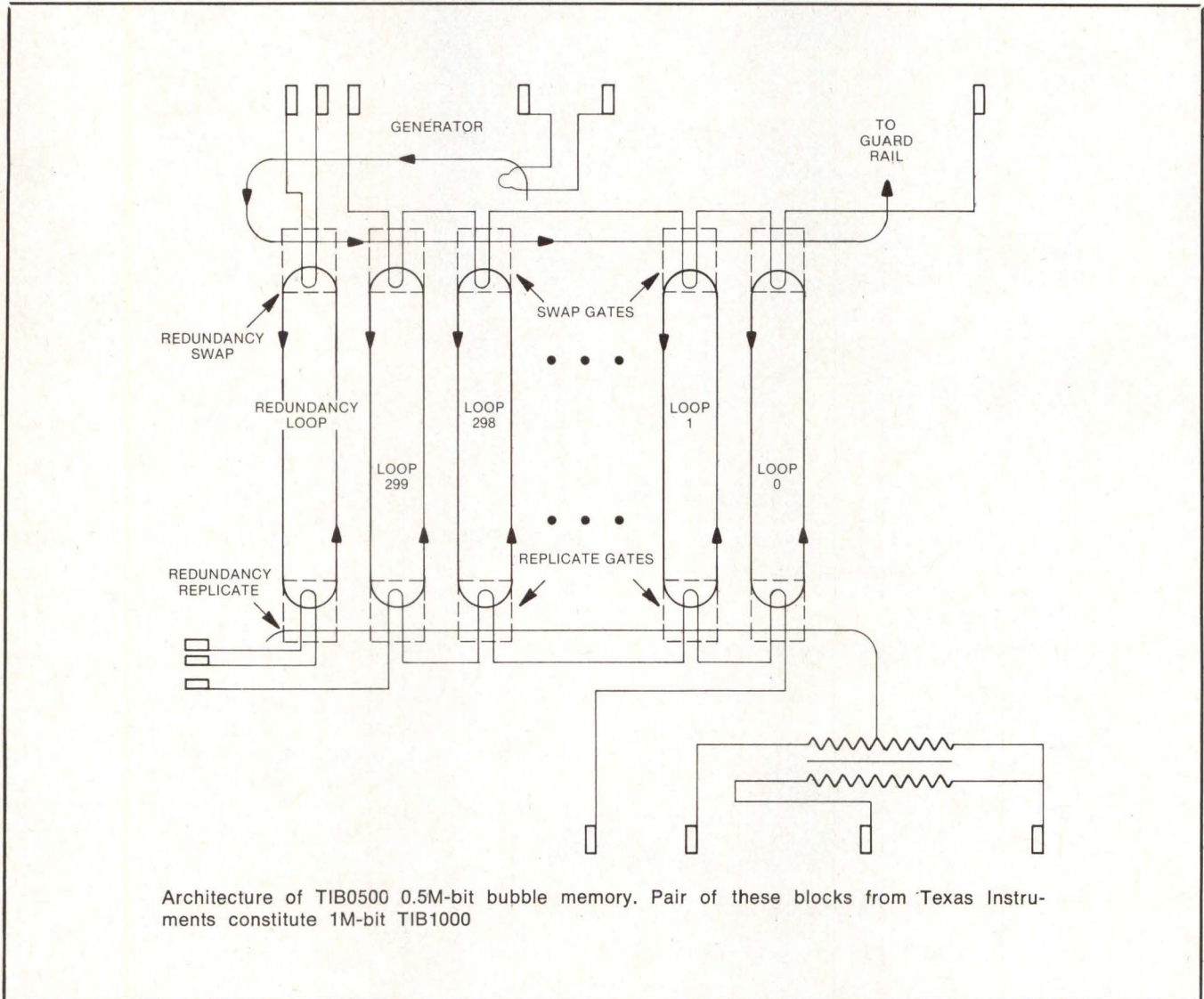
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**Megabit Chip
Heads Pin Compatible
Bubble Memory Family**



Offering an access time of 11.2 ms (typ), this 1M-bit memory is the highest density member of an electrically interchangeable series of magnetic bubble chips from Texas Instruments Inc, PO Box 225012, Dallas, TX 75265. The TIB1000, a binary megabit device organized as 512k x 2, and the TIB0500, a 0.5M-bit device with 512k x 1 organization, are to be available as board level systems. In the second quarter of 1980, a binary 0.25M-bit memory, compatible with the two larger devices, will be available. The family approach

will allow designers to vary system storage capacity by interchanging the bubble memory chips.

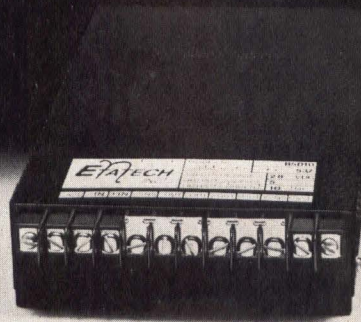
A 2- μ m bubble diameter and a proprietary planar process providing 1- μ m gating and propagation geometries make possible the bit density in these chips. The megabit memory achieves over one million bits of storage on a 149,000 mil² chip (<1 cm²). Other members of the family are scaled proportionally.

The 1M-bit memory has a maximum nonvolatile storage capacity of 1,229,400 bits. A portion of this storage

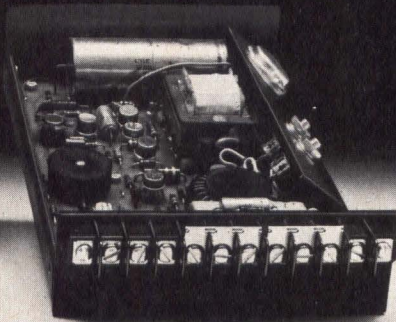
is used for redundancy handling and error correction. The available data storage capacity with error correction capability is 1,049,088 bits or a full 128k bytes of storage. A block replicate architecture is employed, with organization into two identical sections of 512k bits each. There are 300 minor loops per section with 2049 bits per loop. A page of data consists of bubbles from 256 of the loops. Of the remaining loops, 18 are used for error correction information and as many as 26 are allowed to be defective. The field frequency, cor-

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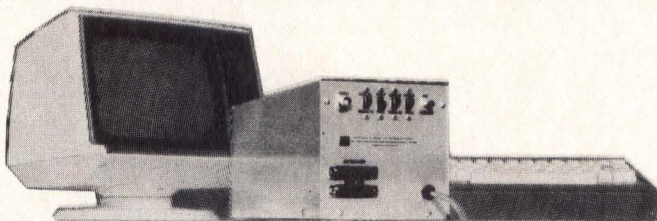
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AROUND THE IC LOOP

responding to an 11.2-ms access time, is 100 kHz, and data rate is 160k bits/s.

Initially, the 1M-bit and 0.5M-bit memories will be available for evaluation or design-in as complete systems in two board formats. The TBB5005 or TBB5010, a 4 x 6" (10 x 15 cm) board with half-megabit or megabit memory, respectively, and all support ICs, offer minimum size configurations. In addition, two TM990 microcomputer compatible memory subsystems with 1M-bit and 2M-bit storage capacity will be available in the first quarter of 1980. These products, designated TBB9910 and TBB9920, also have all support ICs and error correction capability.

All members of the bubble chip family are packaged as 24-pin 3.3 x 3.56-cm units with pins on 100-mil centers. They use the same support circuits, one of which is the TIB0903 monolithic custom controller that provides the interface to many popular buses, including the TMS9900, 8080, and Z80. Other support circuits used by the memory family are the TIB0804 coil driver, TIB0953 function timing generator, TIB0833 sense amplifier, and TIB0863 and TIB0883 function drivers. This set of support circuits will be extended using higher level IC integration and will be available in the second quarter of 1980. The compatibility between the memory chips and the support elements will enable designers to change memory capacity without changing system design.

Circle 351 on Inquiry Card

High Density 4k-Bit Static RAM Surpasses Standard Model

Featuring current consumption of 40 to 70 mA and speeds of 120 to 250 ns, this 1k x 4-bit static random access memory is a pin compatible version of the industry standard 2114. The 2114A from Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, utilizes the proprietary HMOS process to attain a 40% speed improvement over its predecessor. It is considered to be of particular interest to designers of microprocessor applications, buffer memories, and main memory systems.

Logical organization is identical to that of the standard part (see *Computer Design*, Apr 1978, p 200). Among the common factors are 1024 x 4 organization, a single 5-V supply, direct TTL compatibility on all inputs and outputs, common data input and output, 3-state outputs, and a completely static memory with no clock or timing strobe required. A separate chip select (\overline{CS}) lead allows easy selection of an individual package when outputs are or-tied. Simplicity of data access characterizes the upgraded model as it does the original, with address setup times not required. Data are read out non-destructively with the same polarity as the input data. The memory is provided in an 18-pin DIP.

Absolute maximum ratings are, for the most part, identical to those of the earlier memory, with temperature limits of -10 to 80 °C under bias and -65 to 150 °C in storage, max allowable power dissipation of 1.0 W, and dc output limited to 5 mA or less. However, the voltage on any pin with respect to ground is constrained

to a range of -3.5 to 7 V, in contrast to the -0.5 to 7-V constraints on the standard device.

Circle 352 on Inquiry Card

Fast Combinatorial Multiplier Operates With No Clock

Performing a full 8-bit x 8-bit multiplication in only 45 ns, this combinatorial multiplier uses an array of full adders to form and add partial products in a single unlocked operation, resulting in a 16-bit parallel output product. The Am25S558 from Advanced Micro Devices, Inc, 901 Thompson Pl, Sunnyvale, CA 94086, is a pin-for-pin replacement for the similarly numbered part (67/57558) from Monolithic Memories (see *Computer Design*, Nov 1977, p 162). Planned for subsequent announcement, the Am25S557 will add a 16-bit transparent latch between the multiplier array and the 3-state output buffers.

Key features of these devices are their multimode operations and expandability. They also operate on unsigned, 2's complement, or mixed operands. And, by outputting both the most significant bit and its complement, the multiplier can be expanded in either the signed or unsigned mode. In a 16-bit x 16-bit configuration (32-bit output), the typical multiply time is 110 ns.

A single 5-V supply is required, and power supply current (max) is 280 mA. Maximum ratings require that supply voltage relative to ground lie between -0.5 and 7 V. The dc voltage applied to outputs for high output state must remain between -0.5 V and V_{CC} max, and the dc input voltage must remain between -0.5 and 5.5 V. Output current (dc) into the outputs must not exceed 30 mA, and dc input current must stay between -30 and 5.0 mA. The device undergoes 100% product assurance screening to MIL-STD-883 requirements and is packaged in a 40-pin DIP.

Circle 353 on Inquiry Card

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Precision Comparator With Strobe Control Operates at High Speed

A response time of 40 ns (typ), an input offset voltage of 1.0 mV (typ), and a total uncertainty band of $\frac{1}{2}$ LSB ($\pm 150 \mu\text{V}$, max) characterize this 12-bit, strobed IC comparator. Produced by Harris Semiconductor Group, PO Box 883, Melbourne, FL 32901, the HA-4950 is constructed using a proprietary high frequency bipolar dielectric isolation process.

The monolithic comparator consists of three amplifier stages, a latch, strobe control circuitry, and a TTL compatible digital output stage. In operation and with the strobe input TTL level high, both outputs remain high while the amplifiers sense, amplify, and track differential input signals. With a strobe transition of high to low state, the latch is activated and its output is transferred to the complementary output stages,

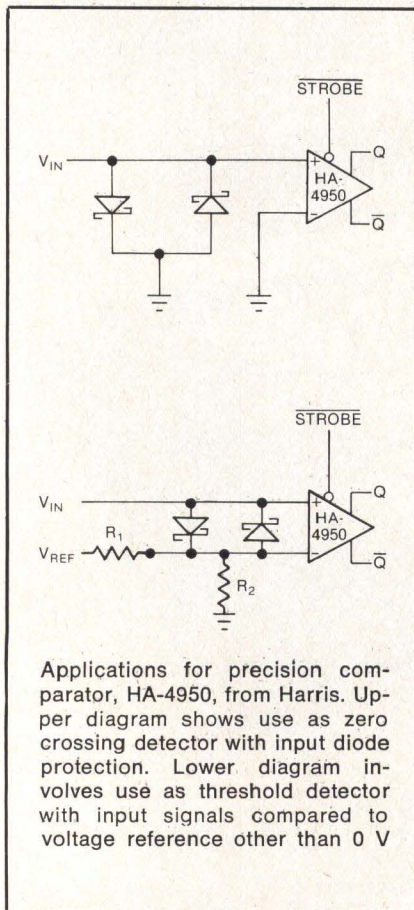
with digital outputs (Q and \bar{Q}) reflecting the polarity of the differential input signal.

This device is designed for uses requiring accurate and fast detection of low level signals as in high speed A-D converters. Other applications include zero crossing and threshold detectors, high resolution comparisons in servo-positioning systems and other feedback loops, and high speed, high accuracy measurement applications such as determining the settling times (to 0.01% of full scale output) of fast amplifiers and high speed D-A converters.

The manufacturer claims that this IC comparator is unique in its combination of speed and sensitivity, pointing out that input sensitivities as low as $50 \mu\text{V}$ may be achieved at lower frequencies. It is adaptable to precision systems without requiring special system trims and additional components.

Three models are available, a commercial version (suffix -5) specified for operation from 0 to 75 °C, a military version (suffix -2) specified from -55 to 125 °C, and a high reliability version (suffix -8) also specified over the military range and conforming to MIL-STD-883. These are available in 14-pin ceramic DIPs. Absolute maximum ratings require that the voltage between V^+ and V^- not exceed 40 V, with the logic supply voltage not to exceed V^+ . Differential input voltage is limited to a $\pm 6\text{-V}$ range. Strobe input must not exceed 7 V (high) nor fall below -5 V (low). The limits on peak output current are $\pm 10 \text{ mA}$, and maximum allowable power dissipation is 549 mW. Storage temperature is constrained to a -65 to 150 °C range.

Circle 354 on Inquiry Card



CMOS Static RAMs Operate at High Speeds With Low Dissipation

Two series of CMOS fully static random access memories from Hitachi America Ltd, 707 W Algonquin Rd, Arlington Heights, IL 60005, have speed capabilities enhanced through use of a $3\text{-}\mu\text{m}$ gate dimension. The HM6148 is a 4k-bit memory organized

as $1\text{k} \times 4$, and the HM6116 is a 16k-bit memory organized as $2\text{k} \times 8$. Each of these operates from a single 5-V $\pm 10\%$ supply, and each has TTL compatible I/O.

The 4k RAM provides a 70-ns max value for address access time and also for chip select time. A higher speed version (suffix -3) offers 55 ns for these two parameters. Power consumption (typ) for both versions is 150 mW during operation, 25 mW on standby (deselected), and $5 \mu\text{W}$ on standby deselected with all inputs either floating or high, for extremely power critical usages. Packaging is in an 18-pin DIP, compatible with the Intel 2114 NMOS static RAM.

Providing a low speed power product of 2.1 pJ, the 16k-bit memory is offered in three versions. Max address and chip select access times for each are 120 ns (suffix -2), 150 ns (suffix -3), and 200 ns (suffix -4). Power dissipation (typ) for all of these versions is 175 mW in operation and 25 mW or $20 \mu\text{W}$ in the same two levels of standby used with the 4k device. This RAM is provided in a 24-pin DIP, compatible with the Intel 2716 EPROM.

Circle 355 on Inquiry Card

Second Sourced EPROM Available With Three Access Times

An electrically programmable, ultra-violet erasable, 16,384-bit read only memory, the sy2716 is the first EPROM to be offered by Synertek Inc, PO Box 552, Santa Clara, CA 95052. It is a plug-in replacement for the industry standard 16k EPROM, Intel's 2716, sharing common characteristics with it, such as 2048×8 organization, operation from a single 5-V supply, and max power dissipation of 525 mW active and 132 mW on standby.

Three versions are available, having max access time of 450 ns (no suffix), 350 ns (suffix -1), and 390 ns (suffix -2). The device is also pin compatible with 16k and 32k mask programmable ROMs (sy2316B and sy2332) from the same manufacturer. It is provided in a 24-pin DIP.

Circle 356 on Inquiry Card

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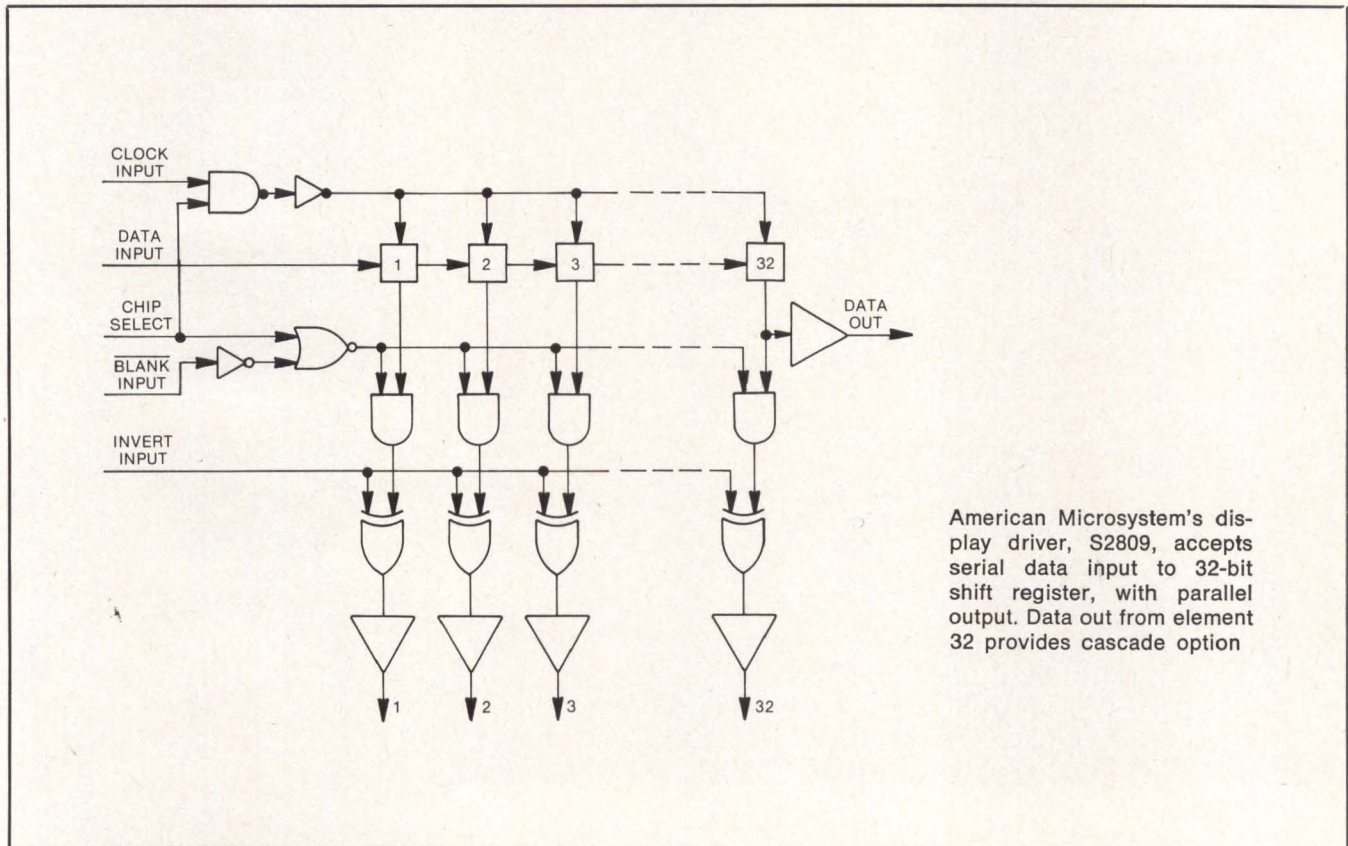
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CIRCLE 109 ON INQUIRY CARD

Display Driver IC Offers Cascade Option



American Microsystem's display driver, S2809, accepts serial data input to 32-bit shift register, with parallel output. Data out from element 32 provides cascade option

The S2809 universal display driver, consisting of a 32-bit master-slave shift register, versatile output drivers and control logic, can drive LED, LCD, or vacuum fluorescent displays. The PMOS IC from American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051, has the ability to drive four 7-segment display digits plus four annunciators. Several of the devices, cascaded, can drive longer displays.

Input data are clocked serially into the 32-bit shift register for outputting to the display drivers. Register element 32 also generates an in-phase data output for cascading purposes. Simple control logic adds flexibility, and integrated capacitors suppress rfi. Positive or negative drive polarity is accomplished via an invert pin to

accommodate various kinds of displays.

The shift register stores data to be used for driving 32 output buffers, which may be used to drive display segments or other circuitry. Data are clocked serially into the register by the signal applied to the clock input whenever a logic 1 level is applied to the chip select input. During this time, outputs are not driven by the shift register, but will go to the logic level of the invert input. With a logic 0 level applied to the chip select input, the 32 outputs are driven in parallel by the shift register.

Invert input is used to invert the state of the outputs, when required. With a logic 0 on this input, the logic level of the outputs is the same as the data clocked into the shift

register. A logic 1 level on the invert input causes all outputs to invert.

The blank input can be used to control display intensity by varying the output duty cycles. With a logic 0 level at this input, all outputs will turn off (ie, outputs will go to the logic level of the invert input). When there is a logic 1 level at the blank input, outputs are again driven in parallel by the 32 shift register elements, assuming the chip select input is at logic 0.

Absolute maximum ratings limit supply voltage, V_{SS} , to 25 V and positive voltage on any pin to $V_{SS} + 0.3$ V. Operating ambient temperature, T_A , must remain between 0 and 70 °C and storage temperature must remain between -65 and 150 °C. □
Circle 357 on Inquiry Card

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The thing that impresses me most about Hughes, however, is the work environment... there's very little tension because there's a lot of job security. Other places I've been, it was dog-eat-dog.

All the way down the line, supervision is helpful rather than dictatorial... they encourage you to make decisions, use your own initiative. Encouragement is everything.

In this environment... I mean Hughes and Southern California... I feel better about myself as a human being... and that's a good place to be."

Excerpted from an interview with Owen Davies, January 8, 1979, Hughes Aircraft, El Segundo, California.

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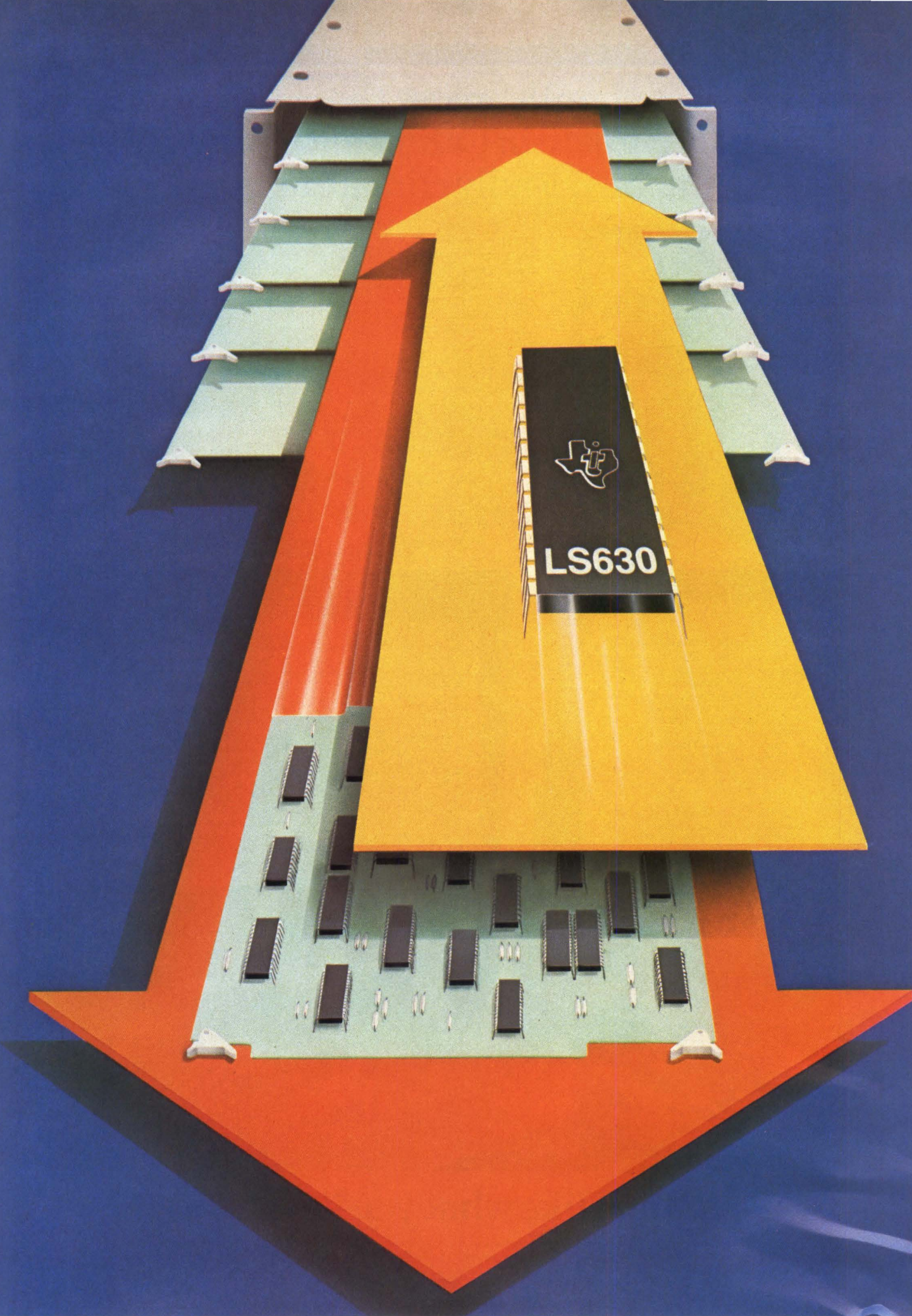
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CIRCLE 110 ON INQUIRY CARD



LS630

Replace 23 ICs and 26 discretes with one 28-pin package. New error detection/correction circuits.

More LS LSI innovation from Texas Instruments.

Here's a new milestone product for all your data transmission applications — the first LSI Low-Power Schottky TTL circuits.

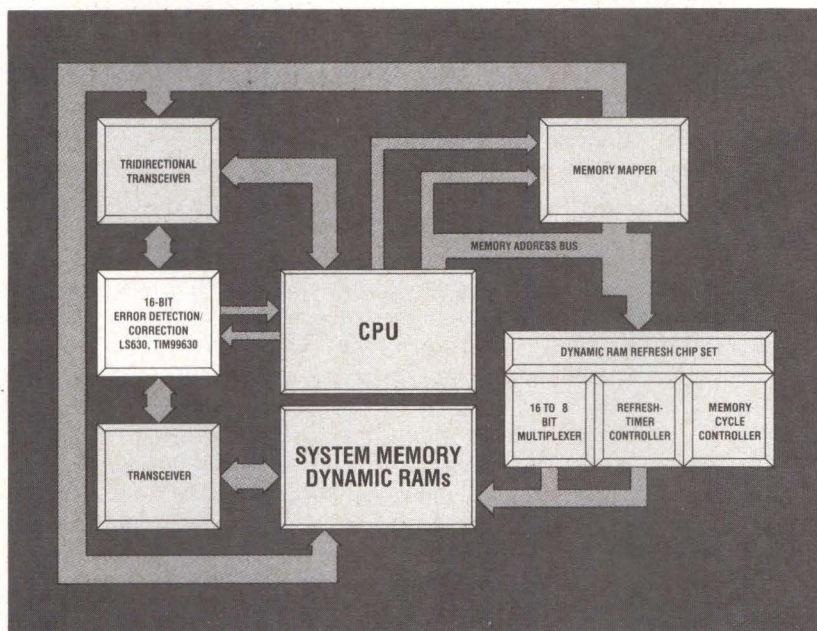
New, single-chip, 16-bit parallel error detection and correction (EDAC) circuits with 3-state (SN54/74LS630) or open-collector (SN54/74LS631) outputs.

Now, for the first time, you can detect single or dual-bit errors — all on one chip.

And processing times are fast. Checkwords are generated in 35 ns typically. Errors flagged in 40 ns.

TI's new EDAC circuits use a modified Hamming code to generate a 6-bit checkword from a 16-bit data word. This checkword is stored in memory along with the data word. During the memory read cycle, the 22-bit word is processed by the EDAC to determine if errors have occurred in memory. Single-bit errors are corrected. Dual-bit errors are flagged. And, a gross error condition of all highs and lows will also be detected.

Your present design uses more ICs. More power. More time. And more board space. The solution is fast, easy and more cost effective.



This is the first in a series of innovative Low-Power Schottky devices to be introduced by Texas Instruments over the next few months. Watch for the new Octal Transceivers announcement and find out how you can save design time and production costs.

One LS circuit that dissipates a low 600 mW. Also designated TIM99630 and TIM99631 for the 9900 Family, LS630 and LS631 are available in a 28-pin, 600-mil ceramic or plastic DIP.

TI's continuing commitment to innovative Low-Power Schottky technology means that you can continue to design with confidence — tapping the broadest product line available.

So, design with the line that serves

more of your LS needs — the broadest line in the industry.

For every low-power, high-performance application — whether it's military systems, data processing, telecommunications, process control and more.

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So, for the widest range of effective bipolar state-of-the-art solutions, turn to the leader. Turn to Texas Instruments for more LS LSI innovation.

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CIRCLE 135 ON INQUIRY CARD

Scientific Computer Provides High Performance at Entry Level Price

Eclipse[®] S/140, an entry level scientific computer system designed for application in computational, communications, and larger process control environments, has been introduced by Data General Corp. The basic 16-bit system is said to offer the industry's highest performance in its price class and can be economically upgraded through the addition of options.

Features and Capabilities

System design is based on a single-board, microprogrammed CPU with a prefetch processor that accelerates the execution of programs. MOS memory is expandable from a basic 128k

bytes to 1M bytes in 128k- and 256k-byte increments. Standard 4-way interleaving on all memory boards results in an effective memory cycle time of 400 ns. Error checking and correction is a standard feature and memory is supported with a standard memory allocation and protection unit. The latter unit supports privileged instructions, I/O device protection, and main memory write and validity protection in a multiuser environment.

A 56-bit microword used in microprogrammed implementation permits execution of parallel overlapped CPU operations every microcycle in order to increase system throughput. The prefetch processor decreases CPU

latency and thereby reduces execution time further for demanding applications. As many as 13 instructions are prefetched, eliminating the fetch cycle from the instruction sequence.

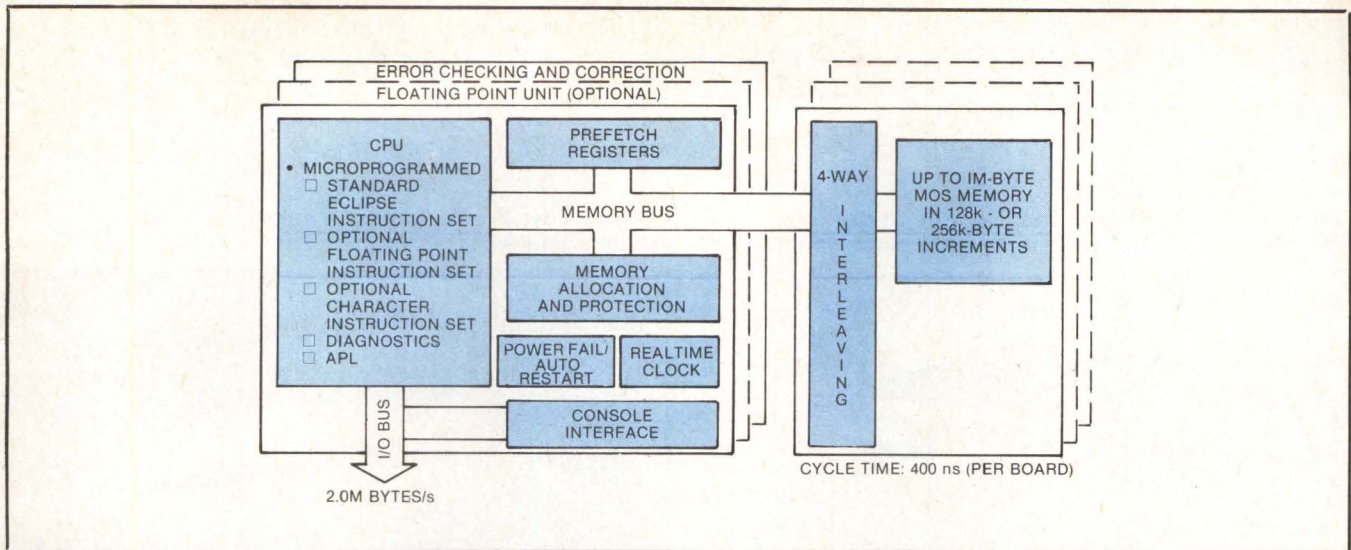
An optional hardware floating point unit is available for very high computational performance. This unit, on a separate board, can perform a double precision multiply in 9.2 μ s.

Stress on system reliability and data integrity is exemplified by features such as automatic diagnostics that test CPU, memory, and I/O bus operations; error checking and correction (ERCC); and battery backup. ERCC, implemented on a separate board, detects and corrects single-bit errors and detects multiple-bit errors for data integrity. A battery backup unit provides power to a single 256k-byte memory board for up to 90 min.

All system boards fit into the 16-slot rack mountable chassis from the front, enabling easy service access. Power is provided by an offline 120-A supply, adequate for the largest standard system configuration.

Available peripherals include 10M- and 20M-byte hard disc drives; 12.5M-byte disc subsystem; 50M-, 96M-, and 192M-byte disc mass storage subsystems; 315k-byte flexible disc drive; and 75-in (190-cm)/s, 800/1600- and 6250-bit/in (315/630- and 2460-bit/cm) magnetic tape subsystems. Dasher[™] displays and printers can be attached as well.





Software

All Eclipse operating systems, languages, and utilities—including the Advanced Operating System (AOS) and the Realtime Disc Operating System (RDOS)—can be accommodated. Under AOS, system resources in a hardware/software protection organization are optimized for concurrent multiuser job string batch applications. Speed of the high performance hardware floating point unit can create a system that supports computational timesharing and program development. An optional firmware implemented floating point instruction set is available for less demanding computational throughput.

RDOS, in realtime sensor based applications such as process control or

image processing, provides optimal character response characteristics with foreground/background memory management of single and multi-tasked operations. A data acquisition and control subsystem can be supported by sensor access manager software for sensor I/O control.

A character instruction set option supports data communications applications with a repertoire of bit, byte, and byte string instructions. Data strings can be of either fixed or variable length. The XODIAC network management system (see pp 34, 38) permits the S/140 to share hardware and software resources with other Eclipse systems in a network environment.

System throughput can be accelerated in communications and sensor

I/O environments by using an optional data control unit as a frontend processor. Interrupt processing, line protocol, and error control functions can be offloaded from the main processor.

Among the languages available under AOS and/or RDOS are FORTRAN IV, FORTRAN 5, Algol based DG/L, Extended BASIC, Business BASIC, PL/I, and assembler. Utilities for remote job entry and communications include HASP II and RJE/80 for IBM 2780/3780 batch protocol emulation. X.25, the international packet switching protocol, is offered under RDOS; AOS supports AOS RCX/70 for IBM 3270 interactive protocol emulation.

Price and Delivery

An Eclipse S/140 computer with 128k-byte memory is priced at approximately \$16,500. A system with 256k-byte memory, console printer, 4-line asynchronous communication multiplexer, four CRT displays, 12.5M-byte disc subsystem, 800-bit/in (315-bit/cm) magnetic tape subsystem, and cabinet costs about \$46,000. With 512k-byte memory, hardware floating point unit, 50M-byte disc subsystem, 300-line/min printer, and synchronous communication line, plus the console printer, magnetic tape subsystem, multiplexer, displays, and cabinet, the price is about \$88,000. Initial deliveries are 90 days ARO. Data General Corp, Rt 9, Westboro, MA 01581. Tel: 617/366-8911.

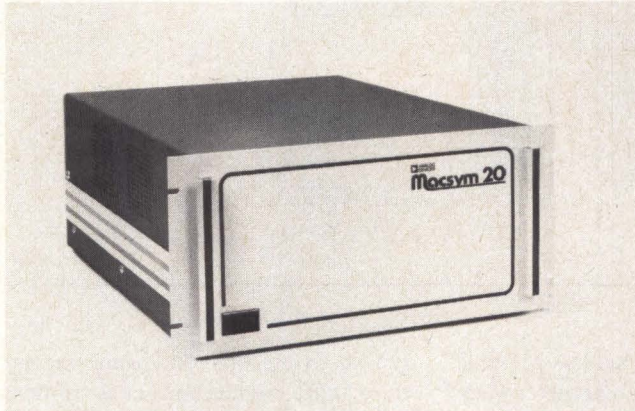
For additional information circle 199 on inquiry card.

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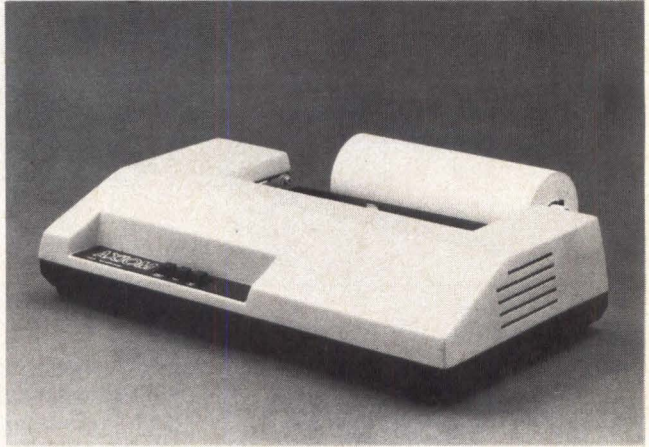
PRODUCTS

Realtime Measurement and Control System Operates Either Standalone or With Host Computer



Macsym 20, an intelligent measurement and control system for both industrial and laboratory applications, provides complete signal conditioning for direct connection to sensors and control elements. It functions as either a complete standalone unit or as a frontend for a host computer in either a remote or a local environment. Included are an 8-bit CPU, 16k bytes of RAM (expandable to 48k), room for up to 16k bytes of user EPROM, precision high speed ADC, realtime clock, and all logic for support of up to 16 signal conditioning cards in any combination of analog and digital I/O. Optional extension chassis allow processing of up to 240 cards. Communications interface is provided through optional RS-232-C serial I/O, IEEE 488, and RS-170 video ports. User programming is achieved through either a powerful command set available in EPROM or custom programs written in A^{PLUS} on a companion development system and burned into EPROM on the same system. **Analog Devices, Inc.**, PO Box 280, Norwood, MA 02062. Circle 200 on Inquiry Card

Ultra Low Profile Impact Printers Have Full ASCII Character Set

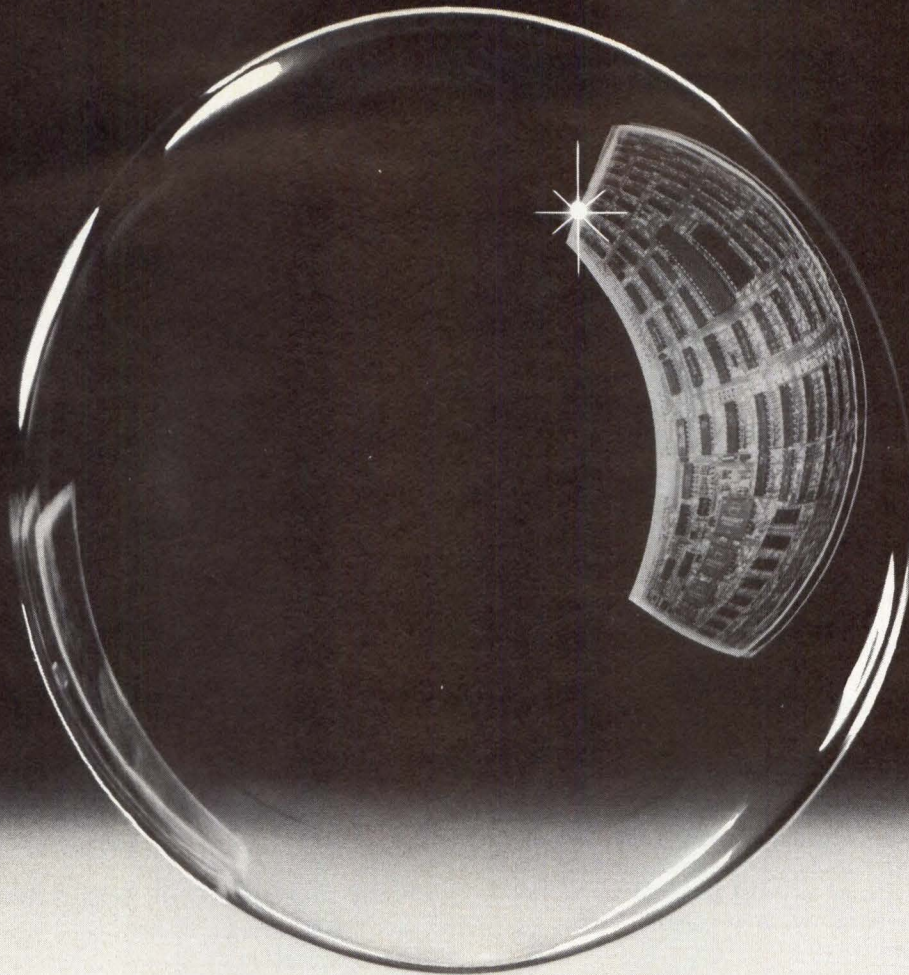


Only 3.5" (8.9 cm) high, 8.75" (22.2 cm) deep, and 17.5" (44.5 cm) wide, IMP-1 and -2 impact printers include Centronics parallel and RS-232-C/20-mA serial standard inputs for up to 1200 baud, and 9600 baud serial as an option. Each prints 80, 96, or 132 columns at 1 line/s with 7 x 7 dot matrix characters. The -1 has friction feed and can make 3 copies on plain 8.5" (21.6-cm) wide paper or can use teleprinter rolls; -2 provides tractor feed as well as friction feed and handles paper from 2.5 to 9.5" (6.4 to 24.1 cm) in width. The -2 also can process graphics under software control. A 96-character ASCII set is standard on both, but special sets are available as options. Double-width characters are provided for headlining or accenting. Each unit has a 512-char buffer, with 2k char optional, for fast screen dumps. 117/230 V, 50/60 Hz is standard. **Axiom Corp.**, 5932 San Fernando Rd, Glendale, CA 91202. Circle 201 on Inquiry Card

Programmable, Functional Benchtop Logic Tester Isolates Faulty PCB Components

Automatic high speed testing of digital PC boards and component level fault isolation are provided by the Logic Test System (LTS). The low cost benchtop system includes high speed pass/fail testing for boards with dynamic logic, automatic guided probing fault isolation to the component level, software programmable power supplies, and up to 384 software programmable driver/sensor pins for boards containing up to 12 different logic families. Interactive software features and high speed peripherals simplify test program coding and debugging. Interface to boards under test is through a combination of zero insertion force connectors, a 90° rotatable adapter fixture, and a stake-pin DIP switch layout. Included in the system are CRT display, dual floppy disc drives, printer interface, and IEEE 488 standard interface bus. **Omnicom, Inc.**, PO Box 32295, Phoenix, AZ 85064. Circle 202 on Inquiry Card





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Now you can confidently incorporate magnetic bubble memories in your next product development: Plessey is fully equipped to design and produce to your spec. Or you can buy add-in bubble memory cards for your Intel SBC systems. Plessey has a range of compatible systems actually in production. Shouldn't you be talking to us now?

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Reliable products from a specialist manufacturer with many years' experience of standard and custom-built memories — made from both magnetic and semiconductor devices.

Contact Plessey Microsystems sales office to discuss your needs for the future, or send for your copy of the Bubble Memory Systems literature folder.



PLESSEY
MICROSYSTEMS

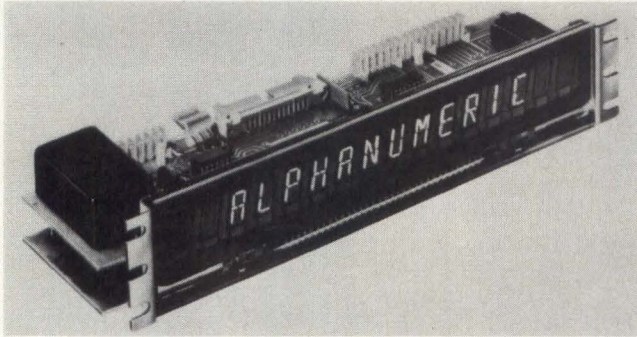
Plessey Microsystems Limited, Water Lane, Towcester,
Northants NN12 7JN.
Telephone: Towcester (0327) 50312. Telex: 31628.

Plessey Microsystems Inc, 19546 Clubhouse Road,
Gaithersburg, Maryland 20760.
Telephone: (031) 948 2791. TWX: 710 828 9708
and at 1641 Kaiser Avenue, Irvine, California 92714.
TWX: 910 595 1930.

*Intel trademark.

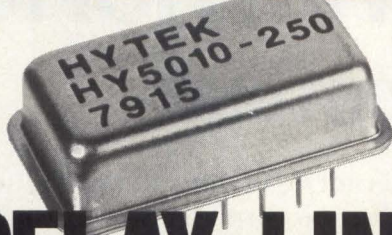
PRODUCTS

14-SEGMENT INTELLIGENT DISPLAYS



The 16- (W416-1051) and 20-char (W420-1051) microprocessor controlled systems contain electronic circuitry including drivers, memories, buffered I/Os, serial interface char generator, and dc input power supply. Installed by plugging in data and power connections, displays are bus compatible, self-initializing, and addressable with 19 ASCII codes that control 19 built-in display modes. End of line modes are left entry with auto line feed carriage return, writeover carriage return, and horizontal scroll. Brightness levels are programmable over 6 to 1 range of light output control in 4-dB steps. Also featured are fully addressable flashing visual cursor and full ASCII parallel or serial input. **Cherry Electrical Products Corp**, 3600 Sunset Ave, Waukegan, IL 60085. Circle 203 on Inquiry Card

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- Hermetic, metal 14-pin DIP (.870"L x .498"W x .250"D)
- 50ns-250ns Delays (ten 10% taps)
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WINCHESTER DISC SYSTEM WITH CARTRIDGE TAPE BACKUP



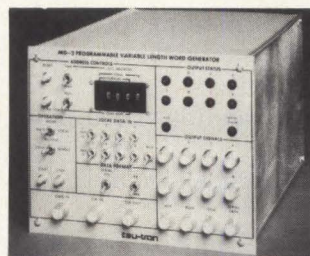
The 21M-byte HD-11—a Shugart industry standard SA4000 Winchester drive with optional 15M-byte DEI cartridge tape backup module—solves data loss if the sealed disc is ever unrecoverable. This packaging of a disc and tape drive in the same chassis is a method of fail-safing disc drives or allowing large offline

storage. Software compatible with the RL01, the system also runs DEC's RL01 disc diagnostics. Features include ECC data protect on both disc and tape, Q-bus and Unibus compatibility, 4 write-protect switches, 4-voltage power supply, DMA transfer in 4-word bursts, and 2 complete sector-buffers. Single-track transfers occur at RL01 rate of approx 400k bytes/s. **Charles River Data Systems, Inc**, 4 Tech Circle, Natick, MA 01760. Circle 204 on Inquiry Card

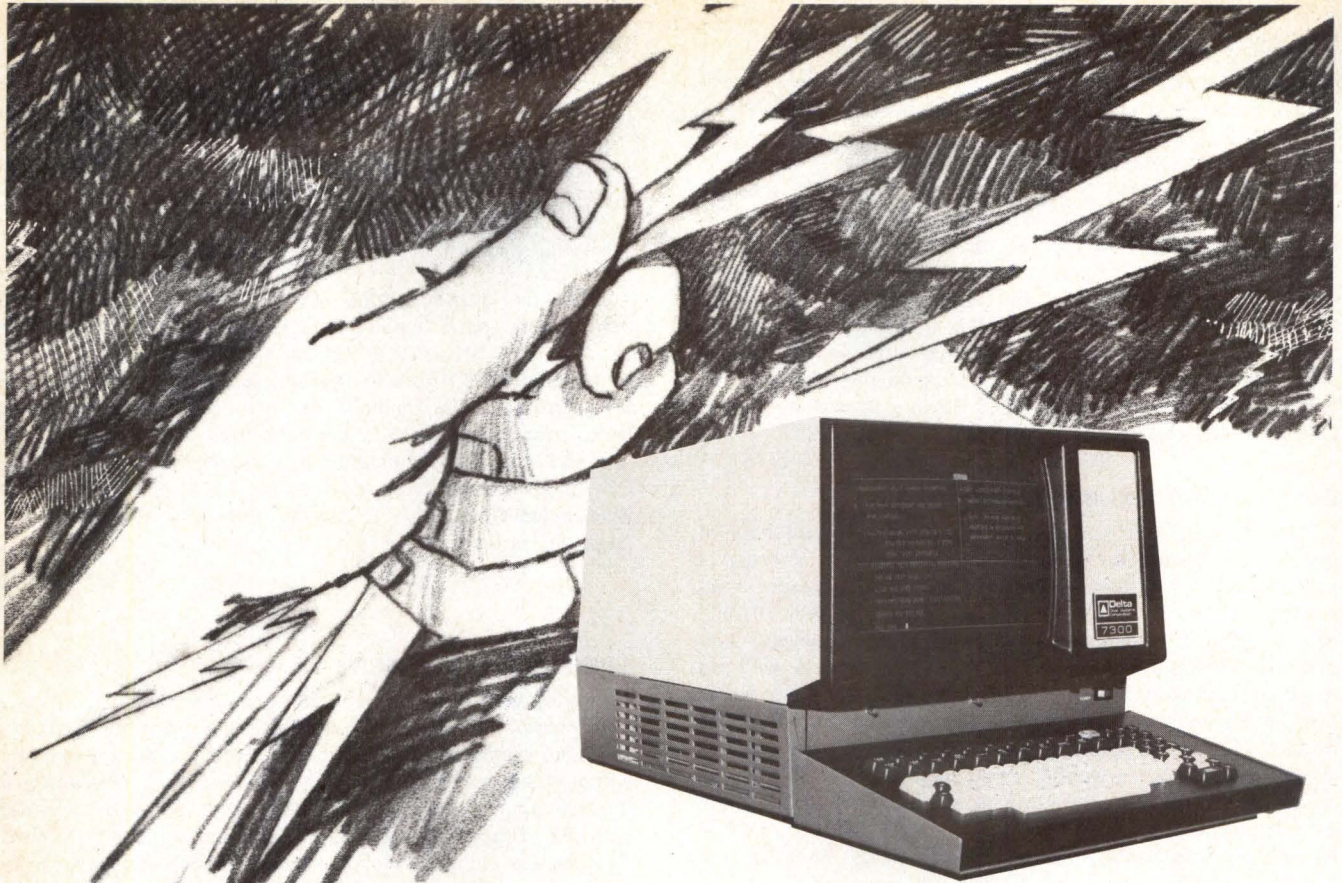
16-BIT ANALOG TO DIGITAL CONVERTER

Model A-8016 is a 16-bit second source to the Analogic MP8016. Capable of converting in as fast as 16 μ s, the unit offers inputs of 0 to 10 V or -10 to 10 V, pin selected either fully differential or single ended. Output levels are TTL compatible and available codes are binary, offset binary, and 2's complement. Differential linearity versus temp is rated at 1 ppm/ $^{\circ}$ C. Gain and offset tempcos are 6 ppm/ $^{\circ}$ C and 1.5 ppm/ $^{\circ}$ C, respectively. Specs include power supply sensitivity per 1% change in power supply voltage of 0.0005%, and operation over the 0 to 60 $^{\circ}$ C temp range with relative humidity rating of 5 to 95% noncondensing. Common mode voltage is 11 V max, while common mode rejection ratio is 75 dB min. **Intech, Inc**, 282 Brokaw Rd, Santa Clara, CA 95050. Circle 205 on Inquiry Card

IEEE 488 COMPATIBLE WORD GENERATOR OPTIONS



Option MG-3LM expands the MG-3 word generator's programmable memory to 1024 words by 9 bits/word, while MG-3IB provides IEEE 488 interface capability for remote programming of the generator (required for the MG-3CB card reader accessory). The generator operates as a 9-bit parallel output word or serial data generator. In the latter mode, the 8 main bits of the data word are serialized to provide a max serial word of 8192 bits. The 9th bit serves as a variable position sync in either serial or parallel operation. RZ or NRZ output format, and continuous or single-burst operation may be selected. Output word length is integer variable from 1 to 1024 words, or 8192 bits in serial mode. **Tau-tron Inc**, 27 Industrial Ave, Chelmsford, MA 01824. Circle 206 on Inquiry Card



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CIRCLE 115 ON INQUIRY CARD

MULTIFUNCTION ADD-IN MEMORY BOARD

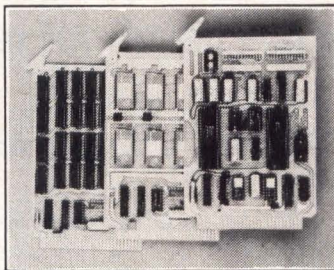
High speed memory board with onboard cache for several Data General Eclipse models stores up to 64k words (128k bytes). Std features include error checking circuitry with single-bit error correction capability, error logging and error display, address select DIP switches, and low power dissipation of 65 W operating, 50 W standby. ECC function facilitates the location of faulty memory chips and enables no-supervision testing without software error logging support. Generating control signals and operating asynchronously, the 5150 offers interleaving capability that allows a computer system processor to access data from several memory boards simultaneously. Interleaved onboard cache permits a 200-ns data access time. **Intel Corp**, 3065 Bowers Ave, Santa Clara, CA 95051. Circle 207 on Inquiry Card

EXACT LENGTH PCB CONNECTORS

OEMs can specify a PC connector with the exact number of positions or contacts required without having to order a custom design or std product with more contacts than necessary. From 10 to 85 contact positions with 0.100" (0.254-cm) contact center spacing are offered in the Amphenol[®] 225A series connectors. They also come with up to 50 contact positions on 0.156" (0.396-cm) center spacings. DIP solder, solder eyelet, or wirewrappable contacts are available, as are 3 optional styles of polarizing keys. Mountings include flush, stepped, open metal end foot, closed metal end foot, or no mounting at all. Industrial grade units with flame retardant housing conform to MIL-C-21097. **Bunker Ramo Corp, Amphenol North America Div**, 2122 York Rd, Oak Brook, IL 60521. Circle 208 on Inquiry Card

THE STANDARD CARDS FROM NORTHWEST MICROCOMPUTER SYSTEMS

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BUS MODULES?



NORTHWEST MICROCOMPUTER SYSTEMS proudly offers you the flexibility of cards built to work with the STD BUS.

NMS over the years has continually demonstrated its leadership in the field of systems design and integration. For instance, the NMS 85/P was the first microcomputer development system to offer PASCAL as a standard feature.

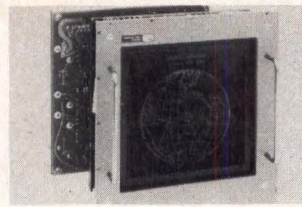
NMS further demonstrated its leadership by releasing a series of cards for the STD BUS. These cards offer systems developers optimal performance and unheard of ease of implementation, thereby saving the system developer time and money.

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749 River Ave. Eugene, Oregon 97404 Phone (503) 688-7100

OEM THIN-PROFILE PLASMA DISPLAY



Models PDA 300 and 301—7.75" (19.69-cm) deep flat-panel assemblies—provide alphanumeric and graphics capabilities in very rugged or military type applications. Optional remote mounting of the power supply module further

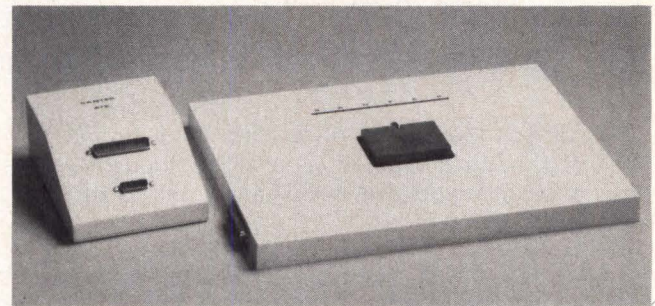
reduces the display profile to only 5" (13 cm). TTL compatible units have usable display area of 8.5 x 8.5" (22 x 22 cm) with 512 x 512 individually addressable elements (dots), spaced 60 dots/in (24/cm); 51 lines of 85 char/line are displayed. For military systems, the 300 uses series 5400J circuitry; the 301's series 7400N circuitry suits it to reduced range environments of rugged industrial systems. Operating life for both devices is >10k hours. **Interstate Electronics Corp**, 1001 E Ball Rd, Anaheim, CA 92803.

Circle 209 on Inquiry Card

EPROM PROGRAMMER

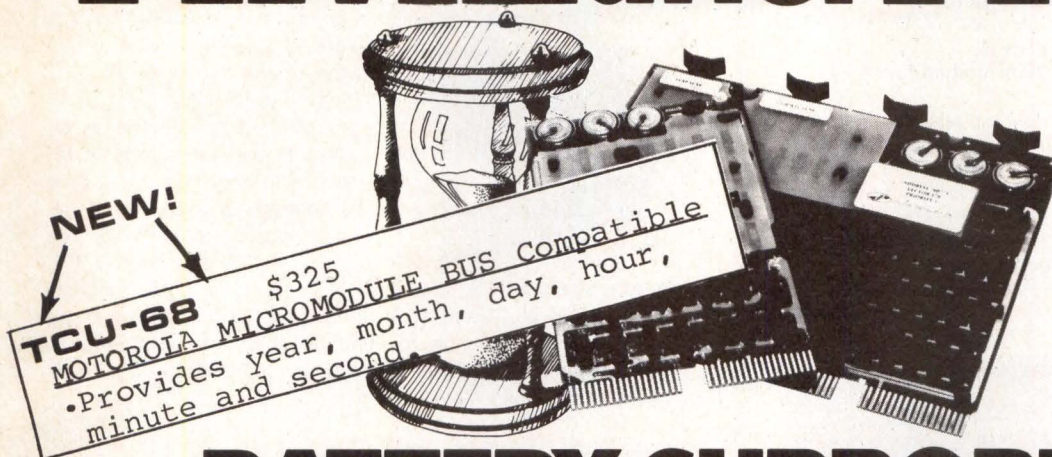
Operating with the Intel[®] microcomputer development system, model 2778 programs 8k, 16k, 32k, and 64k EPROMs, the 8748 microcomputer, and the 8755A expansion memory, without the need for personality modules. Operation is through normal console devices, using software provided with the programmer on single- and double-diskette formats. Devices are plugged into zero insertion force sockets on the front panel of the programming box, which is connected to the development system through a flat cable to a single PC board. A LED display shows which device the unit is set up to program, and which socket is to be used. Plug and socket arrangement allows device types to be changed quickly. **Texas Microsystems, Inc**, 10503 Rockley Rd, Suite 108, Houston, TX 77099. Circle 210 on Inquiry Card

TEST HEADS FOR ATE CODEC TESTING



Programmable test heads convert existing digital automatic test equipment for total codec testing in 1 pass, performing accurate measurements to the D3 channel bank. Retrofit systems conduct a typical ac test sequence in <3.5 s total. Measurements can be done full channel, closed loop, or half-channel open loop. Configurations meet customer test specs for A-law, μ -law, or No-law (skewed parameter) codecs, for either discrete ICs or multiple function chip sets. Test sequencing is resident in firmware in the test head; power is supplied by the mainframe. Upon command, the test head is activated for the programmed parameters and data are fed to the mainframe or stored and strobed. Output can be digital or analog. **Santek, Inc**, 4095 N 28th Way, Hollywood, FL 33020. Circle 211 on Inquiry Card

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TCU-100 • \$495

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Lockheed SUE

TCU-200 • \$550

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Computer Automation (Naked Mini)

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- Provides year, month, day, hour, minute and second.

*Trademark of Digital Equipment Corporation

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- Provides year, month, day, hour, minute and second.
- SBC/BLC compatible.

HP 2100

TCU-2100 • \$395

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- Connects between any terminal and host computer.
- Provides date, time and more!

All Digital Pathways TCUs have on board NICAD batteries to maintain time and date during power down. Timing is provided by a crystal controlled oscillator. Prices are U.S. domestic single piece. Quantity discounts available.

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DIGITAL PATHWAYS

CIRCLE 117 ON INQUIRY CARD

Tarbell Double Density Floppy Disk Interface

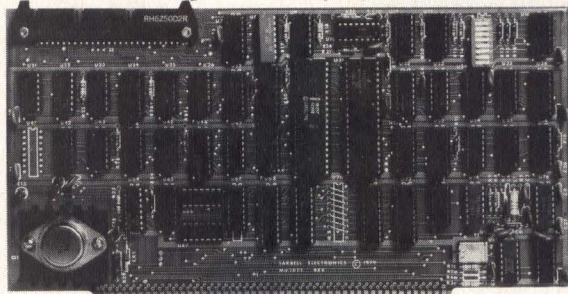
FOR 8" DISK DRIVES

Under Tarbell Double-Density CP/M, single and double density disks may be intermixed. The system automatically determines whether single or double density is in place.

- Software select single or double density.
- Phase-locked-loop and write precompensation for reliable data recovery and storage.
- On-board phantom bootstrap PROM is disabled after bootstrap operation so all 64K memory address space is available to user.
- DMA in single or double density permits multi-user operation.
- Extended addressing provides 8 extra address bits, permitting direct transfer anywhere in a 16 megabyte address range.
- Select up to 4 drives, single or double sided.
- New BIOS for CP/M included on single-density diskette.

Assembled and Tested \$425

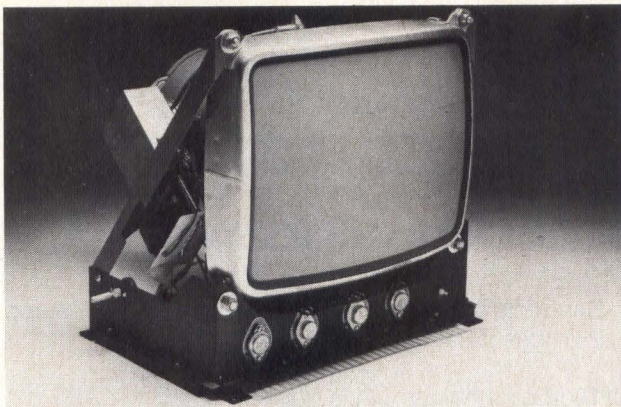
CP/M is a reg. trademark of Digital Research.



Tarbell
Electronics

950 Dovlen Place, Suite B, Carson, Ca. 90746
(213) 538-4251 (213) 538-2254

CIRCLE 118 ON INQUIRY CARD



No Frills Color. Just the basics. If you're a black and white terminal manufacturer, the Intecolor 813 is all you need to upgrade your terminals to color.

It consists of an 8-color, 13" CRT, plus a special Analog Module System with all the circuitry necessary to perform deflection and video drive functions for the CRT. The completely self-contained circuitry is on a single printed wiring board which also generates the low voltage, high voltage and CRT bias, mounted on a sturdy aluminum frame for heat sinking the power transistors needed for the circuitry.

With our Nine Sector Convergence System, perfect color registration takes only three to five minutes. And this convenient control panel can be located anywhere for easy access.

Available in standard 262 Raster line or 400 Raster line high scan versions. If you're ready to upgrade to a color line, call 404/449-5961 for a demonstration.

Color Communicates Better

Intelligent Systems Corp.



225 Technology Park / Norcross, Georgia 30071
Telephone 404/449-5961 TWX: 810-766-1581

CIRCLE 119 ON INQUIRY CARD

TRACKBALL OPTICAL ENCODER

Trackball's accurate X-Y positioning of a cursor or data on a CRT graphic display adapts it to computer peripherals or X-Y positioning systems requiring interactive realtime control. The operator can control both X and Y axis movement of the cursor with 1



2 incremental encoders sense the movement as the operator rotates the ball. Incremental digital output of the encoders represents direction and magnitude of rotation in each axis. Operation is over a 0 to 55 °C range, with power input of 5 Vdc ±5% at 200 mA max to TTL

operation. Both HTL and CMOS compatible output signals are available at 12 and 15 V. Line driver and up/down pulse logic with resolution up to 2048 bits/ball turn are optional. **Disc Instruments, Inc.**, 102 E Baker St, Costa Mesa, CA 92626. Circle 212 on Inquiry Card

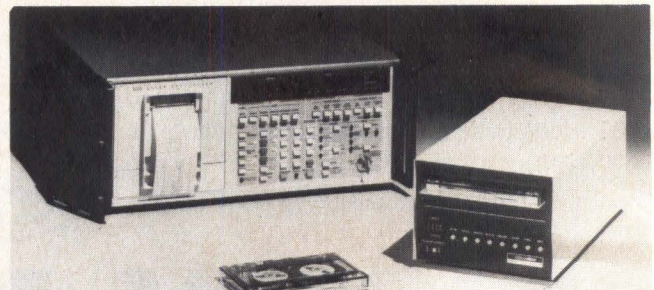
IEEE 488 TO PARALLEL INTERFACE ADAPTER

Connecting printers and other equipment with standard parallel interfaces to the IEEE 488 bus, this adapter operates at the printer's maximum rate and with the basic interface supplied on most printers. Board version is configured to plug directly into a Centronics' interface slot; a boxed version with cabling for printers is available without this feature. A power supply is included for use with printers that do not provide 5 V at 350 mA. Fabrication meets full IEEE 488 electrical specs; 2 onboard ribbon cable connectors offer inexpensive daisy chaining of bus compatible devices. The unit's address, as well as polarity of each parallel side's signals, are DIP switch selectable. **Proline, Inc.**, 135 Liberty St, Copiague, Long Island, NY 11726.

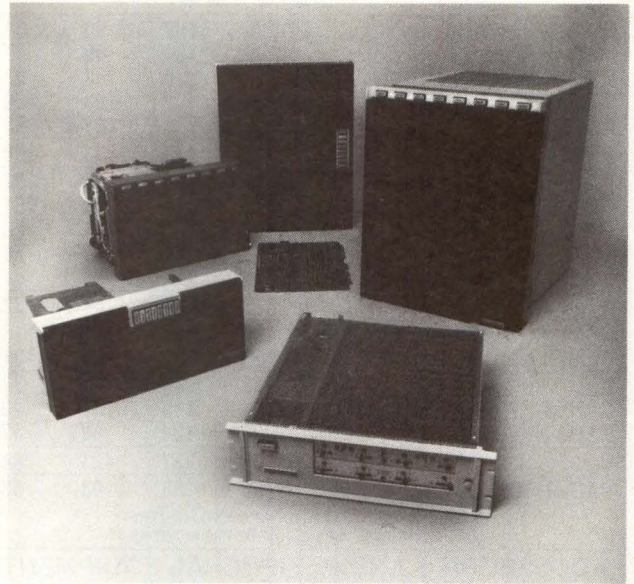
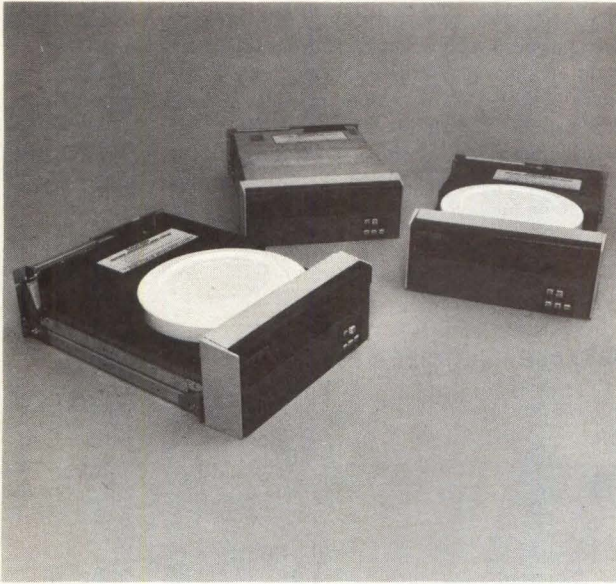
Circle 213 on Inquiry Card

CARTRIDGE RECORDER FOR DATA LOGGER BULK STORAGE

Microprocessor controlled model 300D stores 3.5M bytes of data in any block length using std computer compatible 1600-bit/in (630/cm) phase encoded recording. Read after write check assures that data have been recorded without error. Overall data reliability is 1 error in 10⁶ bits. Communicating in remote or unattended data logging applications, the recorder operates at rates up to 19.2k baud. Serpentine recording technique eliminates rewind time to start the next data track. All status conditions are recorded in nonvolatile memory in case of power failure. On power-up, the system automatically initializes itself and resumes data recording. **Columbia Data Products, Peripherals System Div.**, 9050 Red Branch Rd, Columbia, MD 21045.



Circle 214 on Inquiry Card



Delivery That's OEM Responsive

Perkin-Elmer tape and disk drives are available now. When we saw the demand for our drives grow, we responded by making the investments necessary to be responsive to OEM delivery requirements. Our commitment to OEMs includes a new 250,000 square foot manufacturing complex with the production capacity that can meet today's requirements.

Our OEM Commitment Our commitment to the OEM goes beyond new facilities. It's a multi-faceted corporate commitment that involves a powerful combination of investments in advanced production and testing equipment, responsive management, financial strength and competitive products. A commitment that assures product reliability, on-time delivery, and responsiveness for our OEM customers.

Responsive Products We offer the OEM tape and disk drives that have become the industry standards. Our tape drives are available in sizes from 7 inches to 10½ inches with speeds ranging from 12.5 ips to 75 ips and recording densities up to 1600 cpi. Our Super Series cartridge disk drives are available in front-loading and top-loading configurations. Storage capacities are from 2.5 to 20 megabytes.

Responsive Answers For a responsive answer to your tape or disk requirements, write or call today. Then, you'll see what it means when we say we're OEM responsive.

Perkin-Elmer, Memory Products Division,
7301 Oranewood Avenue, Garden Grove,
CA 92641 (714) 891-3711

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FROM TRANSNET

PURCHASE FULL OWNERSHIP AND LEASE PLANS

DESCRIPTION	PURCHASE PRICE	PER MONTH		
		12 MOS.	24 MOS.	36 MOS.
LA36 DECwriter II	\$1,695	\$162	\$ 90	\$ 61
LA34 DECwriter IV	1,295	124	69	47
LA120 DECwriter III KSR	2,295	220	122	83
VT100 CRT DECscope	1,895	182	101	68
VT132 CRT DECscope	2,295	220	122	83
DT80/1 DATAMEDIA CRT	1,895	182	101	68
TI745 Portable Terminal	1,595	153	85	57
TI765 Bubble Memory Terminal	2,795	268	149	101
TI810 RO Printer	1,895	182	101	68
TI820 KSR Printer	2,195	210	117	79
TI825 KSR Printer	1,695	162	90	61
ADM3A CRT Terminal	875	84	47	32
QUME Letter Quality KSR ...	3,195	306	170	115
QUME Letter Quality RO	2,795	268	149	101
HAZELTINE 1410 CRT	875	84	47	32
HAZELTINE 1500 CRT	1,195	115	64	43
HAZELTINE 1552 CRT	1,295	124	69	47
DataProducts 2230 Printer ..	7,900	757	421	284
DATAMATE Mini Floppy	1,750	168	93	63

FULL OWNERSHIP AFTER 12 OR 24 MONTHS
10% PURCHASE OPTION AFTER 36 MONTHS

ACCESSORIES AND PERIPHERAL EQUIPMENT

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TWX 710-985-5485

CIRCLE 121 ON INQUIRY CARD

THE INDUSTRIAL ROBOT MARKET

The industrial robot market has yet to exhibit the explosive growth predicted in the 1960's and early 1970's. The circumstances are changing and the robot market will have solid growth in the first half of the 1980's. Industrial robots may be broadly classified as to how they move, either point to point, or continuous path, and as to how the movements are controlled, with or without servo mechanisms. In addition, on the continuous path robots they may be either tape or solid-state actuated. Many additional subcategories of industrial robots can be made and these relate to control complexity and source of robot power — drum controller vs. microprocessor, hydraulic vs. electric. The advent of the microprocessor and minicomputer now allow a robot controller to have extensive memory capabilities.

Frost & Sullivan has completed a 250-page report on The Industrial Robot Market through the 1980's considering the market prospects by end user industry and within by type of robot. Detailed product specifications are provided by supplier for company comparisons.

Price: \$800. Send your check or we will bill you. For free descriptive literature, plus a detailed Table of Contents, contact:

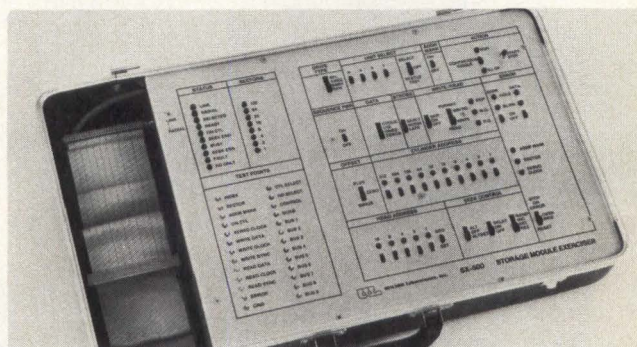


FROST & SULLIVAN
106 Fulton Street
New York, New York 10038
(212) 233-1080

HIGH DENSITY THERMAL PRINTHEADS

For high density graphic printing applications, series DM 48256, DM 48288, and DM 69414 have corresponding densities of 88, 91, and 100 dots/in (35, 36, and 39/cm) across 3, 3.3, and 4.3" (7.6, 8.4, and 10.9 cm), respectively. Inter-leaved interconnect arrangement of dot address lines doubles dot density and improves cost-effectiveness since each on-board isolation diode services 2 dot elements instead of 1. Printing speeds range up to 5 lines/s of alphanumeric text and up to 0.5" (1.3 cm)/s of graphics. Min MTBF is rated at 100M dot pulses/dot element and 10M char lines. Print-heads can be driven by simplified microcomputer interface circuitry using std 10-bit BiMOS latched driver packages. **Gulton Industries, Inc.**, 212 Durham Ave, Metuchen, NJ 08840. Circle 215 on Inquiry Card

PORTABLE EXERCISER



Model SX-500 exercises and tests many Winchester technology storage module drives such as Ampex DM980, CDC 9760 series, and Kennedy 5300. Lightweight attache case packaging promotes field service evaluation in addition to in-plant QA testing. Operation may be either single step or continuous with error indication or stop-on-error; 4 modes enable the unit to format, read/write, read, or write all 0s, all 1s, alternate 1s and 0s, or cyclic data pattern. Seek controls enable rezero, set, increment, or random seeks with or without a seek delay. Indicators are provided for drive status, sector count, write or read in progress, head address, and error flag; 26 test points are brought out to the front panel for accessibility. **Wilson Laboratories, Inc.**, 2237 N Batavia St, Orange, CA 92665.

Circle 216 on Inquiry Card

HIGH CAPACITY DISC SYSTEMS

Storage capacity per disc drive for Hewlett-Packard 3000 computers is quadrupled by 2 disc systems based on 1694 and 1696 intelligent disc controllers. They handle up to 8 industry std disc drives with capacities of 300M and 600M bytes, respectively. Online storage expands up to 2G and 4G bytes. Each system includes a controller, host adapter, and up to 8 disc drives. The controllers emulate characteristics of HP 7925 disc drives. In addition to software transparency with the std HP 3000 MPE operating system and hardware compatibility, other features are data buffering, automatic track seek and position verification, error checking and correction, and extensive resident diagnostics. **Microcomputer Systems Corp.**, 432 Lakeside Dr, Sunnyvale, CA 94086.

Circle 217 on Inquiry Card



Of course our Floppys aren't cheap. Quality never is.

It's no use trying to hide the fact: Maxell Floppy Disks give you the finest quality you can buy no matter how much you spend. And more and more of you are agreeing that your data is worth our perfection.

Our floppys work better with your drive.

Naturally, our floppys conform to ISO and IBM specifications. More important, they have also been approved by major OEMs, the people who recommend only those few floppys they are certain will work best with their hardware. So although we obviously don't know which drive system you are using, it makes no difference. Maxell Floppy Disks are so good they actually work better with any drive.

What it all means for you.

Yes, you can pay less for some other floppys. But lost data is a terrible price to pay when quality is what you want. And Maxell Floppy Disks help you profit in the very parameters you use this medium for: storing more data with virtually no down-time.

The level of modulation uniformity in every Maxell floppy is vital to double density recording and readout. It

means no peak shift, complete freedom from dropouts, total absence of particle orientation. Plus longer life, greater overall durability, and significantly less oxide build-up and head abrasion.

So when you have to depend on full data retrieval, a few cents can make a big difference. Depend on Maxell Floppy Disks. They can really save you.

Maxell offers the full range of Floppy Disks from standard 8-inch to 5 1/4-inch plus Data Cassettes. *Dealer inquiries invited.*



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CIRCLE 123 ON INQUIRY CARD

205

PRODUCTS

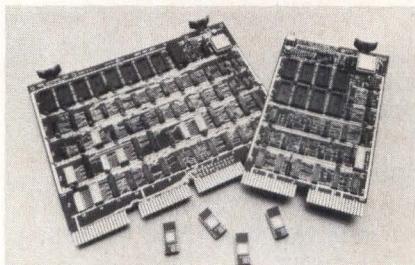
UNIBUS COMPATIBLE COMMUNICATIONS INTERFACE

CDZ-11 provides a multiplexed interface for the PDP-11 Unibus and 8 or 16 asynchronous channels. Designed to connect multiple local or remote terminals to a computer system, it is fully compatible and interchangeable with DZ-11 hardware and operating and diagnostic software. Voltage levels and pinning conform to EIA RS-232-C and CCITT V.24. A max of 128 lines may be connected to a single computer using the interfaces. **Computer Interface Technology**, 201 W Dyer Rd, Suite C, Santa Ana, CA 92707. Circle 218 on Inquiry Card

WIDE VIEWING ANGLE MINIATURE LED

OSL series GaP lamps, packaged in a metal coaxial header, are available in single- or double-lead versions. High efficiency, omnidirectional electroluminescence from GaP diodes is reflected forward to provide a 100-mil dia source of light with 180° viewing angle. Typ luminous intensities range from 0.55 to 2.5 mcd with forward voltages from 2.1 to 2.6 V at currents of 15 to 40 mA, respectively. Model numbers are OSL-1, 1S, 5, 50 red; -11, 11S green; and -31, 31S yellow. **OPCOA Div of IDS Inc**, 330 Talmudge Rd, Edison, NJ 08817. Circle 219 on Inquiry Card

P/ROM PROGRAMMER MODULES



MR-004 accommodates 2716 and 2732 UV erasable P/ROMs and provides a switch or program selectable onboard programmer with status register for programming write, interrupt enable, and done. P/ROM, status register, and vector addresses are switch selectable; bus request levels are selectable. Module requires one quad slot in the PDP-11 chassis. MRV-004, for use with LSI-11, accommodates 2716 and 2758 UV erasable P/ROMs, and requires one-half quad slot in the chassis. **MDB Systems, Inc**, 1995 N Batavia St, Orange, CA 92665. Circle 230 on Inquiry Card

Circle 230 on Inquiry Card

SOLID STATE CAMERA PROGRAMMABLE CONTROLLER

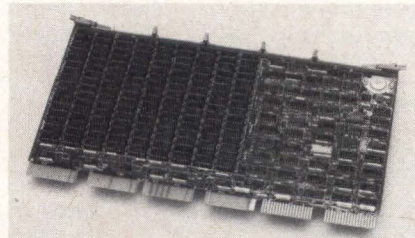


For use with linear and 2-dimensional (matrix) photodiode array camera systems, RS8500 is a 2-board expandable system including power supply and an 8085 CPU design incorporating AMD math chip. Unit can perform up to 8 simultaneous mathematical functions relating to an extensive list of measurement and pattern recognition applications. Up to 60 programmable parameters configured in a scroll operating system can be assembled by following a prompted 20-char alphanumeric fluorescent display. **EG&G Reticon**, 345 Potrero Ave, Sunnyvale, CA 94086. Circle 221 on Inquiry Card

HALF-DUPLEX BUS LINKS

For use between 2 PDP-11 Unibus, 2 LSI-11 Q-bus, or LSI-11 and PDP-11 systems, Buslink/Uni™ and /U-Q™ use computer DMA facilities to transfer data at up to 500k or 125k words/s, respectively. Software supported by RSX-11M, -11S, DECNET-M and -S, the links are software and diagnostic compatible with DA11-B or DAV11-B, but require only one-half the power and one-fourth the space. A handler is available from DEC for RSX-11D. **Able Computer**, 1751 Langley Ave, Irvine, CA 92714. Circle 222 on Inquiry Card

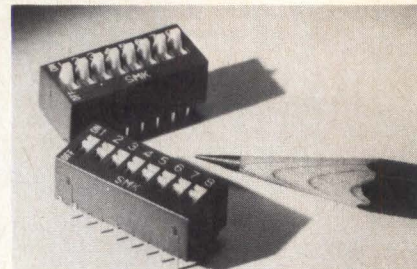
128k x 18 ADD-IN MEMORY SYSTEM FOR PDP-11



A single-card system, MK8012 is totally hardware and software compatible with PDP-11/04, /34, /05, /10, /15, /35, /40, /45, /50, /55, and /60. It plugs into either a core or semiconductor powered 04-34 slot with only minor jumper changes. Density options include 64k x 18, 96k x 18, or 128k x 18; a parity option is also available. 16k RAM technology results in low operating power and high speed. **Mostek Corp, Memory Systems**, 1215 W Crosby Rd, Carrollton, TX 75006. Circle 223 on Inquiry Card

Circle 223 on Inquiry Card

DIP SWITCHES



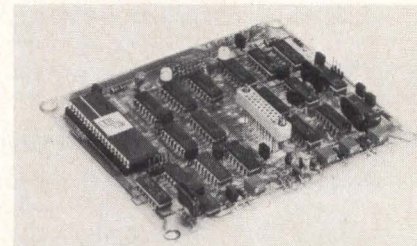
Slide type JS-8770 toggle lever and -8766 flush lever types are available in 1 to 10 circuit positions. They are sealed at the base with a thermosetting plastic and oven cured to provide complete protection against solder flux contamination during cleaning. A double-sided clip-type wiping contact provides self-cleaning action, resulting in high reliability, long life, and excellent shock and vibration characteristics. **SMK Electronics Corp of America**, 113 E Savarona Way, Carson, CA 90746. Circle 224 on Inquiry Card

SWITCHING POWER SUPPLIES

An internal filter allows SM series regulated supplies to meet VDE 0871 conducted emissions requirements, governing units that operate above 10 kHz. With this filter the units not only meet the requirements but exceed them by 5 dB. The filter is available as a std option on SM series switchers with power ratings between 750 and 1000 W, and with 1 to 4 outputs. **LH Research, Inc**, 1821 Langley Ave, Irvine, CA 92714. Circle 225 on Inquiry Card

Circle 225 on Inquiry Card

I/O BOARD FOR HOSTILE ENVIRONMENTS



Option 214 PAR'H provides a universal 8-bit parallel interface between the company's 250BH hostile environment digital cassette tape transports and mini or microcomputer, supplying >95% of required I/O circuitry and timing control; users supply only address line decoding. Parallel to serial and serial to parallel conversion circuitry is integrated into the board. Operating over the -40 to 70 °C range, board provides 8 data input and 8 data output lines. **MFE Corp**, Keewaydin Dr, Salem, NH 03079. Circle 226 on Inquiry Card

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Look What's Happening at Teleray!



Teleray is on the move in smart terminals. Our list of satisfied users is growing rapidly, and for good reason. These terminals are:

- **ESPECIALLY SMART** — 32 programmable keyboard functions, full editing, formatting and tabular control, interactive and block mode communications.
- **APPLICATION DESIGNED** — APL with true overstrike, DEC, DG or Microdata replacements, expanded display memory (48 lines — scrolling).
- **PACKAGED TO SUIT** — Detached or integral keyboard, tilt screen, molded, metal or rack mount (depending on application and model).
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(313) 354-6421
(408) 744-1930
(412) 243-8421
(513) 223-8421

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(714) 273-4771

(714) 552-7850
(716) 381-4120
(801) 969-4034
(808) 523-1326

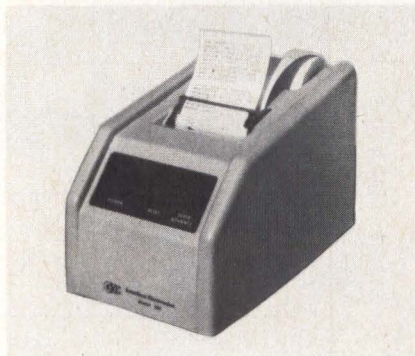
CIRCLE 124 ON INQUIRY CARD

PRODUCTS

EBCDIC TO ASCII CONVERTER

BAC-3270T sends and receives EBCDIC data via IBM 3270 bisync protocol, performs all required error checking functions, translates data to ASCII, and outputs in serial asynchronous format to and from most Tektronix 4000 series devices. The unit and attached devices emulate an IBM 3271 controller with from 1 to 3 attached 3270 CRT/keyboards, allowing equipment operation at high data rates, and insuring error free operation by using CRC-66 error checking. **KMW Systems Corp**, 8307 Hwy 71 W, Austin, TX 78735. Circle 227 on Inquiry Card

27-COL DOT MATRIX IMPACT PRINTER



Model 100 incorporates C. Itoh/Epson model 210 printer, HIF-210 microprocessor based single-board printer controller, and modular power supply in 6 x 6.5 x 11" (15.2 x 16.5 x 27.9-cm) unit. Unit prints 96 ASCII u/lc char set under software control using 5 x 7 matrix to produce 27-col line at 2.4 lines/s. Parallel input is Centronics compatible; serial input accepts TTY, 20-mA current loop, or EIA RS-232-C signals at selectable baud rates from 110 to 9600. **Interface Electronics Div, Capitol Circuits Corp**, 24 Denby Rd, Allston, MA 02134. Circle 228 on Inquiry Card

ALL PURPOSE EMI FILTERS

APF-11, -21, and -31 filters have current ratings from 1 to 30 A, 115/250 Vac, and power line frequency of 50/400 Hz. International connector devices are rated 1, 3, and 6 A at 115/250 Vac and 50/60 Hz. Medical series 1-, 3-, and 6-A units feature integral IEC connector. High performance international devices feature higher common mode inductance and greater line to line capacitance. **Cornell-Dubilier Electric**, 150 Ave L, Newark, NJ 07101. Circle 229 on Inquiry Card

BASIC LANGUAGE FOR SYSTEM/34

System/34 BASIC features an interactive compiler that combines ease of use characteristics of interpreter with performance advantages of compilers. Interactive compiler checks syntax of each line of programming code entered by operator. If syntax error occurs, user presses "help" key to display correct syntax. Users can stop execution of program, examine or change variables, and resume execution. 48k bytes of main storage are required. **International Business Machines Corp, General Systems Div**, Atlanta, GA 30301. Circle 220 on Inquiry Card

SONIC DIGITIZER

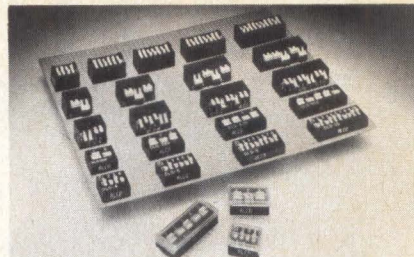


Model GP-6-3D GRAF/PEN is capable of tracing and digitizing the contours of existing objects and also of synthesizing imaginary 3-dimensional shapes within the cube defined by the sensors. The electronic control unit is a microprocessor controlled GP-6 programmed to output 4 slant ranges. A second model converts slant ranges to X, Y, Z Cartesian coordinates, and a third permits 2-dimensional and 3-dimensional digitizing with 2-dimensional calculations of area, line length, and variable scaling. **Science Accessories Corp**, 970 Kings Hwy W, Southport, CT 06490. Circle 231 on Inquiry Card

VOICE I/O TERMINAL

Cognivox plugs into Exidy's Sorcerer computer, offering a 16-word recognition vocabulary plus voice response with up to 16 words or phrases. Recognition accuracies of up to 98% are possible with cooperative speakers. Self-contained unit includes microphone and amplifier/speaker. A talking calculator program allows the computer to be used as a 4-function calculator without looking at the CRT screen, and a vocal memory dump program can read out loud its memory in hexadecimal format. **Voicetek Inc**, PO Box 388, Goleta, CA 93017. Circle 232 on Inquiry Card

DIP SWITCHES



Designed for soldering onto PC boards or for use with std DIP sockets, all switch models have terminals and contacts of beryllium copper with heavy gold plate over nickel to assure low level switching service. Terminals are molded in or epoxied to provide a full seal. Rockers, slides, and piano types with side actuation are available in 4-through 10-pole configurations as normally open or spdt types. **Alco Electronic Products, Inc**, PO Box 568, Lawrence, MA 01842. Circle 233 on Inquiry Card

COMPUTER-MAGNETIC TAPE INTERFACE BOARD

A single interface imbedded in Nova or Eclipse computer controls up to 2 of the company's formatters, each capable of handling up to 4 transports. This allows interface to control up to 8 tape units. Interface will drive formatters with NRZI, PE, or dual-density format, and system will handle a mix of 7- and 9-track transports at any std speeds. Data transfers to and from a selected tape unit occur via DMA. **Digi-Data Corp**, 8580 Dorsey Run Rd, Jessup, MD 20794. Circle 234 on Inquiry Card

MINIATURIZED SWITCHING POWER SUPPLY



TV-1036 provides 5 Vdc at 40 A from an input source of 104 to 125 Vac, 47 to 500 Hz. A 3-output model outputs 5 Vdc at 35 A and ± 15 V at 1 A each. Measuring 8.85 x 1.57 x 3.57" (22.48 x 3.98 x 9.06 cm), the unit's 71% efficiency remains constant over the input voltage range. Line and load regulation are 0.1% and tempco is 0.01%/°C. MTBF is 70k hours at 45 °C ground base per MIL-HDBK-217. Features include overload protection, input voltage surge protection, and inrush current limiting. **Arnold Magnetics Corp**, 11530 W Jefferson Blvd, Culver City, CA 90230. Circle 235 on Inquiry Card

This is the fastest serial matrix printer in the world. At 600 cps, it races like a line printer. (Special 900 cps compressed character capability for even greater data processing output.)

It is also the most durable printer of its kind. Because of its revolutionary design, the life of the print head will exceed one billion characters.

No other serial printer is as advanced. The print head is four times more efficient at converting electrical energy into mechanical print energy. The incredibly sophisticated print mechanism combines heavy-duty hardware with unmatched speed and accuracy. A programmable micro-processor-based control offers an almost unlimited choice of type fonts, full graphics and extended character format.

Line printer speed. Line printer reliability. Serial printer prices.

Serial number one . . . comes from Florida Data.

**Florida Data Corporation,
3308 New Haven Avenue,
West Melbourne FL 32901,
(305) 724-6088**



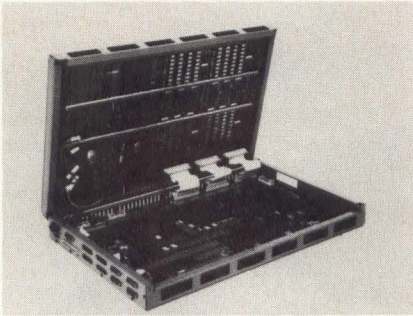
Serial of Champions

**FLORIDA
DATA**

CIRCLE 125 ON INQUIRY CARD

PRODUCTS

ASCII 8-CHANNEL I/O PROCESSOR



Handling 8 ASCII channels at up to 19.2k baud, F6420 has 2 onboard microprocessors operating in parallel. One is dedicated to I/O, the other (with resident multiuser BASIC) to applications code. Half the address space of each microprocessor is paged into a 0.25M-byte triplexed synchronous common memory. The other half is used for I/O and for onboard private memory. Rated at 150 W, 5 and ± 15 Vdc, the I/O processor uses flexible cable interconnects. **Functional Automation, Inc.**, 3 Graham Dr, Nashua, NH 03060. Circle 236 on Inquiry Card

NETWORK CONTROLLER

Both digital and tone commands are accepted by controller for remote control of modem substitution switches, digital A/B fallback switches, and channel access switches. Two output buses allow connection of up to 64 switches, each having 16 channels. All 1024 channels may be separately addressed by either digital or tone commands. Four built-in fallback switching channels may be locally or remotely controlled. **Dynatech Data Systems**, 7644 Dynatech Ct, Springfield, VA 22153. Circle 237 on Inquiry Card

GRAPHICS CAPABILITIES FOR VIDEO DISPLAY TERMINALS

ADM-31 and -42 terminals have been enhanced to provide business graphics capabilities. Featuring more than 10 graphics char, including corners, T-bars, crosses, and vertical and horizontal lines, enhancement can produce bar charts and customized business forms. For hardcopy output, terminals link to printers and plotters through an RS-232 interface. **Lear Siegler, Inc.**, Data Products Div, 714 N Brookhurst, Anaheim, CA 92803. Circle 238 on Inquiry Card

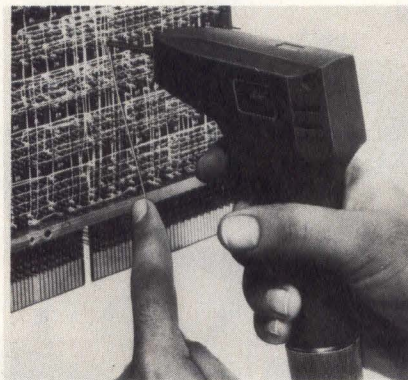
DUAL ALPHANUMERIC LEDS

Hercules LR3784/85R end stackable displays with common cathode and righthand decimal point consist of 2 0.54" (1.37-cm) high, red 14-segment char in a single package. Composed of GaAsP emitting material, solid state displays have a typ 600 μ cd/segment luminous intensity at 20 mA/1.6 V_F. The 18 horizontal double DIP pins on 0.100" (2.54-mm) spacing are set up for multiplex drive for max pinout economy. **Industrial Electronic Engineers, Inc.**, 7740 Lemona Ave, Van Nuys, CA 91405. Circle 239 on Inquiry Card

HIGH OUTPUT 500-W SWITCHING POWER SUPPLIES

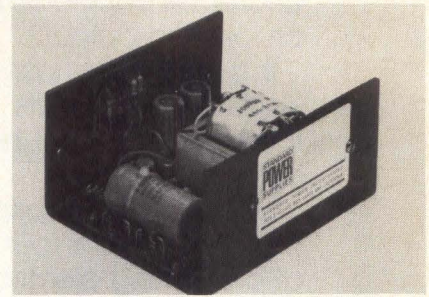
With outputs rated at 12, 15, and 24 V, MG series units are packaged in a 5 x 8 x 11" (127 x 203 x 280-mm) case. MG12-43 is rated at 12 V, 43 A; 15-34 at 15 V, 34 A; and 24-21 at 24 V, 21 A. Output voltage regulation is 0.1% max for worst case combination of 0 to 100% load change and $\pm 10\%$ line change. Ripple is rated at 10 mV rms and 50 mV pk-pk (30-MHz bandwidth). Overload protection is constant current set at 110% $\pm 5\%$ full load. **Gould Inc, Electronic Power Supply Div**, 4323 Arden Dr, El Monte, CA 91731. Circle 240 on Inquiry Card

BATTERY POWERED WIREWRAPPING TOOL



BW-2630 operates on 2 std C size NiCad batteries and accepts either of 2 specially designed bits. Bit BT-30 is for wrapping 30 AWG wire onto 0.025" (0.635-cm) sq pins; BT-2628 wraps 26-28 AWG wire. Both produce the preferred modified wrap. Both positive indexing and anti-overwrapping mechanisms are provided. Pistol grip design and rugged ABS construction assure performance and durability. **OK Machine and Tool Corp.**, 3455 Conner St, Bronx, NY 10475. Circle 241 on Inquiry Card

TRIPLE-OUTPUT DC POWER SUPPLY



Model 40T provides a triple output of ± 5 Vdc at 2.5 A and two each ± 12 Vdc at 0.75 A. Regulated dual 12-Vdc output and 5 Vdc make supply suitable for powering op amps. Regulation of $\pm 0.1\%$ line or load, 5-mV ripple, and 500- μ s response time enable unit to handle small computer and peripheral needs. Weight is 2.9 lb (1.3 kg) and overall dimensions are 2.88 x 4.75 x 5.50" (7.31 x 12.06 x 13.97 cm). Universal ac input is 115/230 Vac, 1 ϕ 47 to 440 Hz. **Standard Power, Inc.**, 1400 S Village Way, Santa Ana, CA 92705. Circle 242 on Inquiry Card

SUBMINIATURE LED INDICATORS

Intended for circuit board mounting, Super-Brite 5310 presses into holes in the PC board and provides precise LED location. Device spaces LED to same height as switch or component, providing exact alignment to fit panel hole opening or behind lens. Ultra high intensity LEDs are available in red, green, and yellow. High dome lens permits max light output over 90° viewing angle. Typ forward voltages of approx 2 V at 20 mA produce 4 to 5 mcd. **Industrial Devices, Inc.**, 7 Hudson Ave, Edgewater, NJ 07020. Circle 243 on Inquiry Card

4-OUTPUT OPEN FRAME SWITCHER

Model 912 delivers 5 V at 15 A, ± 12 V at ± 1.5 A, and -5 V at 0.5 A. Total power capability is 111 W. Line regulation is $\pm 0.1\%$ on all outputs. Load regulation is better than $\pm 0.5\%$ on all outputs. The unit will accept 100/115/220/240-Vac inputs, selectable on the barrier strip. All outputs have short circuit and current limiting protection. Self-recovering overvoltage protection and remote sensing are std on the 5-V output. **RO Associates, Inc.**, 246 Caspian Dr, Sunnyvale, CA 94086. Circle 244 on Inquiry Card

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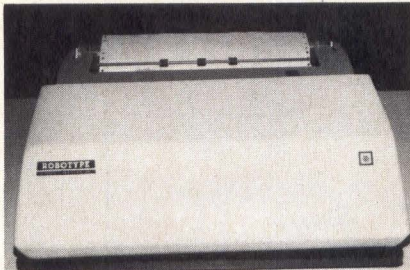
For more information about these new data display monitors, contact Bell & Howell-Fernseh Display Devices, 4000 Birch Street, Newport Beach, CA 92660, (714) 752-7602.

***FERNSEH* INC.**

*the Video Corporation of
Bell & Howell and Robert Bosch*

PRODUCTS

TYPEWRITER TO PRINTER CONVERTER



Robotype model 2100 converts typewriters into computer printers at one-third the cost of conventional printers. Unit interfaces with parallel, RS-232-C serial, 20-mA current loop, or TTL interface. RS-232-C has switch selectable 110-, 134.5-, or 150-baud rates. Attaching to IBM Selectric, Remington Rand, Olympia, or Facit typewriter with no modifications, unit is placed over keys of typewriter; plungers rest on keys and push them down on computer command. **Applied Computer Systems, Inc.**, 77 E Wilson Bridge Rd, Worthington, OH 43085. Circle 245 on Inquiry Card

RECTANGULAR LED LAMPS

Rectangular 521 series lamps feature flat, even intensity light emitting surfaces that can be stacked for flush mounting. Lamps are LEDs with rectangular epoxy encapsulation that is tinted and diffused. Series 521-9264 is a high efficiency red GaAsP on GaP, -9265 is yellow GaAsP on GaP, and -9266 is green GaP. Horizontal or vertical stacked units form an uninterrupted light emitting surface. **Dialight, A North American Philips Co.**, 203 Harrison Pl, Brooklyn, NY 11237. Circle 246 on Inquiry Card

ALPHANUMERIC MESSAGE DISPLAY

Message Central is a compact 8-digit alphanumeric display with 1" (2.5-cm) high char that form tailored messages readable from 75 ft (22.8 m). Three colored lights mounted on top of the display can be programmed to flash for attention or can be lighted in different combinations to communicate specific instructions. From 1 to 256 individually addressable and dispersed displays can be located anywhere in a facility and controlled individually from a central CRT or similar input device. **SMS**, 26 Olney Ave, Cherry Hill, NJ 08003. Circle 247 on Inquiry Card

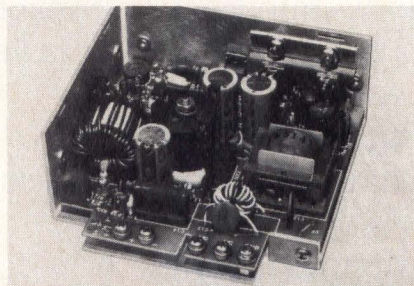
TOGGLE SWITCH SEAL ASSEMBLY

1-piece seals, consisting of flexible rubber seal bonded to threaded metal insert that replaces panel mounting nut, hold switch in place while sealing handle and encapsulating bushing to panel. Assembly protects against oil, dirt, dust, most solvents, and many acids, while allowing handle to protrude. Various elastomers and colors are available as well as a military version designed to meet MIL-B-5423 requirements. **Ame Corp.**, 101 E Main St, Little Falls, NJ 07424. Circle 248 on Inquiry Card

DISCRETE COMPONENT BOARDS

Permitting users to mount discrete components to design special circuits, boards have same outlines and mounting dimensions as the company's M, R, and W series, and plug into card cages containing boards in these series. Board field area where components are mounted is not copper clad. Only I/O field has wirewrapped pins and copper traces for interconnecting between components and I/O. Holes must be drilled by user. **Augat Inc, Interconnection Systems Div.**, 33 Perry Ave, Attleboro, MA 02703. Circle 249 on Inquiry Card

50-W SWITCHING POWER SUPPLY



Open frame switching regulated supplies with outputs from 5 to 36 V at currents from 10 to 1.5 A, ES-E series measure 2 x 4 x 5" (5 x 10 x 12.7 cm) and are from 70 to 84% efficient. Line and load regulation is 0.2%. A monolithic chip contains all regulation, modulation, and protective circuitry, allowing parts reduction of 20%, and MTBF of >50k hours. Units accept dual ac input of 85 to 132 and 170 to 264 Vac, 47 to 63 Hz, for positive brownout protection. **Power/Mate Corp.**, 514 S River St, Hackensack, NJ 07601. Circle 250 on Inquiry Card

COMPUTER PROGRAMMABLE LOW NOISE PREAMPLIFIER

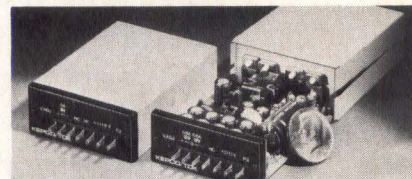


Computer control and programmability of model 1201 are enabled by 2 custom LSI chips. Gains are selectable from 10 to 25k with an accuracy of better than 1%; gain stability is better than 0.03%/°C. Control outputs indicate over-load status, remote operation, and high pass/low pass filter selection. Gating of preamplifier is via TTL compatible or any waveform input. Specs include common mode rejection to 140 dB and common mode input to 10 V pk-pk. **ITHACO, Inc.**, 735 W Clinton St, Ithaca, NY 14850. Circle 251 on Inquiry Card

LCD HEATER

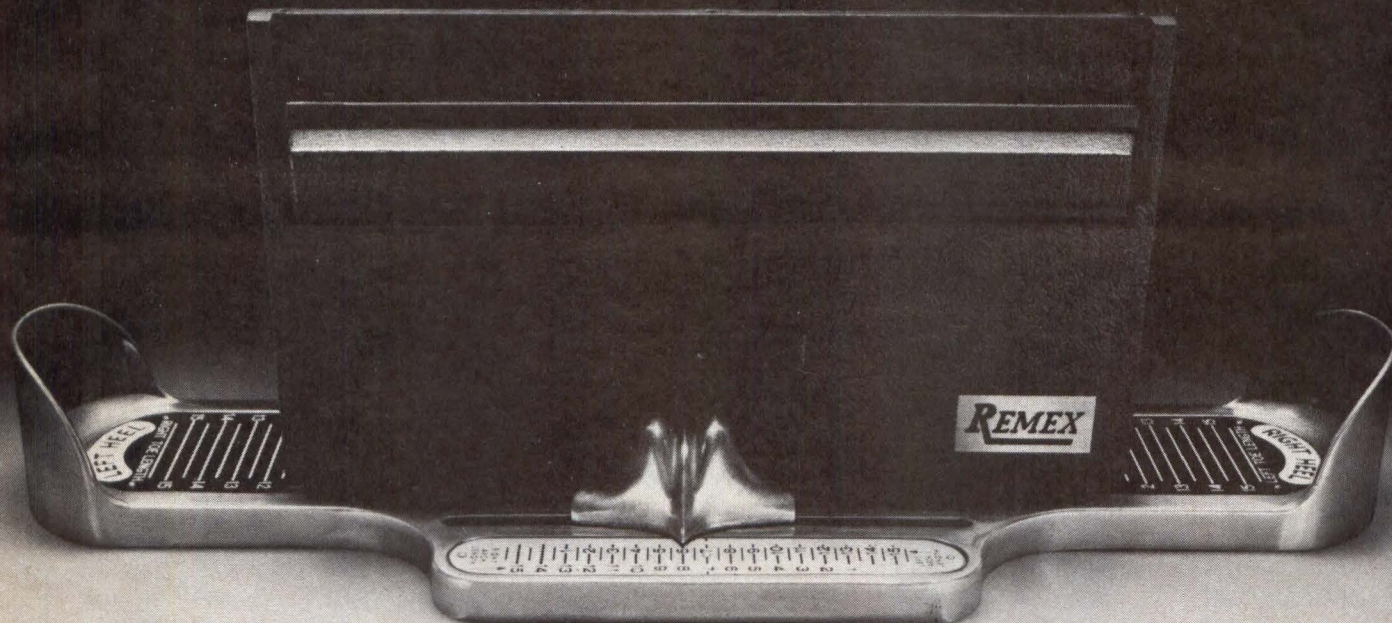
Self-regulating heating effects of specially doped ceramics are used to heat liquid crystal or other temperature sensitive displays, allowing them to function properly at cold temperatures. Devices produce heat at cold temps and curtail heating at normal or high temps. They can be used in battery operated instruments due to low normal current drain. **Midwest Components Inc.**, PO Box 787, 1981 Port City Blvd, Muskegon, MI 49443. Circle 252 on Inquiry Card

10-W SWITCHING POWER SUPPLIES



Single- and dual-output repairable units have a 2-piece aluminum housing for protection and emi shielding. They use AMP Faston 110 series solder tabs for input and output connections, and mount with 6-32 hardware. Ratings of 73% efficient MP series are 5 V at 2.0 A, 9 V at 1.1 A, 12 V at 1.0 A, and 15 V at 0.8 A. With 75% efficiency, CMP series are rated at ±12 V, 0.5 A; ±15 V, 0.4 A; 12 and -5 V, 0.5 A; 15 V, 0.4 A and -5 V, 0.5 A; and 12 and -9 V, 0.5 A. **Kepeco, Inc.**, 131-38 Sanford Ave, Flushing, NY 11352. Circle 253 on Inquiry Card

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REMEX DIVISION

DATA WAREHOUSE

LITERATURE

Metal Replacement Molding Compound

Strength retention, dimensional stability, flexural modulus, and heat resistive and compressive strengths of GENAL[®] CF-7000, an asbestos-free glass-filled phenolic molding compound, are listed in brochure. **General Electric Co, Plastics Div**, Pittsfield, Mass. Circle 300 on Inquiry Card

Readout Displays

LED, incandescent, and neon readouts, and decoder/drivers are detailed in selection guide with mechanical, electrical, and materials specs, dimensions, and mounting and wiring diagrams. **Dialight, A North American Philips Co**, Brooklyn, NY.

Circle 301 on Inquiry Card

Industrial Communication System

Brochure reviews attributes of Modbus distributed control system that integrates programmable controllers, computers, terminals, and monitoring, sensing, and control devices. **Gould Inc, Modicon Div**, Andover, Mass.

Circle 302 on Inquiry Card

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1621

Communication Fiber Optics

Catalog supplies specs and application recommendations for optical fibers and cables, fiber optic modems and interfaces, and baseboard video lines. **Valtec Corp**, West Boylston, Mass.

Circle 303 on Inquiry Card

Factory Data Collection

DATA CAP/1000, an applications software tool, collects and applies manufacturing operations data that can minimize costs, boost productivity, and avoid major quality problems in the field. **Hewlett-Packard Co**, Palo Alto, Calif.

Circle 304 on Inquiry Card

Precision Resistors

Tables of tolerances and TCR aid in selection of correct resistor family; resistance, tolerance, power, TCR, and dimensional specs are listed in brochure for each of the series. **Vishay Resistive Systems Group, Vishay Intertechnology, Inc**, Malvern, Pa.

Circle 305 on Inquiry Card

LED Lens/Mounts

Performance graphs illustrating advantages of PCB and panel lens/mounts over other mounting methods are included in brochure with specs and dimensions. **Visual Communications Co**, El Segundo, Calif.

Circle 306 on Inquiry Card

Disc Drives

Brochure lists specs and descriptions of 8 and 14" (20- and 35-cm) single- or double-density and double-sided floppy, fixed, and minifloppy disc drives. **Shugart Associates**, Sunnyvale, Calif.

Circle 307 on Inquiry Card

Microprocessors

Second edition of guide to the selection and use of microprocessors examines, among other topics, the STD BUS and 6800, 8080/8085, and Z80 architectures. **Pro-Log Corp**, Monterey, Calif.

Circle 308 on Inquiry Card

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—not the reader service number. Please do **not** circle the page number on the reader service card.

	PAGE		PAGE
MATERIALS AND FORMS	PAGE		PAGE
MAGNETIC MATERIALS AND FORMS			
CRT Yokes and Flybacks			
Litton Triad-Utrad	97		
OTHER MATERIALS AND FORMS			
Crystals			
Bulova Watch	166		
HARDWARE			
CONNECTORS AND INTERCONNECTION SYSTEMS			
Connectors			
AMP	60, 61		
PCB Connectors			
Bunker Ramo/Amphenol North America	200		
Interconnection Components			
Spectra-Strip	189		
Flat Cable/Connector Systems			
Brand Rex	165		
Robinson-Nugent	22, 23		
INDICATORS; READOUTS; DIGITAL DISPLAYS; LAMPS			
Displays			
Cherry Electrical Products	198		
Alphanumeric Message Displays			
SMS	212		
PANELS AND BACKPLANES			
Discrete Component Boards			
Augat/Interconnection Systems	212		
WIRE AND CABLE (See also Connectors)			
Wire			
OK Machine & Tool	54		
COMPONENTS AND ASSEMBLIES			
FILTERS			
EMI Filters			
Cornell-Dublier Electric	208		
MOTORS; ROTATIVE COMPONENTS			
Motors			
Robbins & Myers	46		
PHOTODEVICES; PHOTODEVICE ASSEMBLIES			
LEDs			
OPCOA/IDS	206		
Dual Alphanumeric LEDs			
Industrial Electronic Engineers	210		
LED Indicators			
Industrial Devices	210		
LED Lamps			
Dialight/North American Philips	212		
POWER SOURCES, REGULATORS, AND PROTECTORS			
Power Supplies			
Power-One	32		
Standard Power	210		
Switching Power Supplies			
Arnold Magnetics	208		
Etatech	218		
Gould/Electronic Power Supply	210		
LH Research	206		
Power/Mate	212		
RO Associates	210		
Power Peripherals			
Topaz	101		
SWITCHES			
Pushbutton Switches			
Micro Switch/Honeywell	51		
DIP Switches			
Alco Electronic Products	208		
SMK Electronics	206		
Toggle Switch Seal Assemblies			
Ame	212		
THERMAL COMPONENTS			
LCD Heaters			
Midwest Components	212		
CIRCUITS			
DIGITAL AND INTERFACE INTEGRATED CIRCUITS (See also Semiconductor Memories under Memory/Storage Equipment)			
RAMs			
NEC Microcomputers	36, 37		
Static RAMs			
Hitachi America	188		
Intel	6, 7, 186		
P/ROMs			
Intel	8, 9		
EPROMs			
Synertek	188		
Microprocessors			
Advanced Micro Devices	25, 26, 27		
Multipliers			
Advanced Micro Devices	187		
UARTs			
Signetics	180		
D-A Converter ICs			
Analog Devices	196		
Encryption ICs			
Western Digital	178		
Stepper Motor Controller Chips			
Cybernetics	58		
Bubble Memory Chips			
Texas Instruments	185		
Control Processor Chips			
National Semiconductor	160		
DRIVERS AND DECODERS			
Display Drivers			
American Microsystems	190		
National Semiconductor	182		
LINEAR INTEGRATED CIRCUITS			
Interface ICs			
Monolithic Memories	40, 41		
Comparators			
Harris Semiconductor	188		
OSCILLATORS			
Crystal Oscillators			
Vectron Laboratories	65, 66		
MEMORY/STORAGE EQUIPMENT			
BUBBLE MEMORIES			
Bubble Memory Systems			
Intel	10, 11		
Plessey Microsystems	197		
Bubble Memory Chips			
Texas Instruments	185		
FLEXIBLE DISC UNITS			
Flexible Disc Drives			
BASF Systems	179		
MFE	28, 29		
Micro Peripherals	39		
Pertec Computer/PCC Peripherals	103		
Qume	195		
Shugart	70, 71		
Flexible Disc Interfaces			
Tarbell Electronics	202		
Flexible Disc Systems			
Data Systems Design	13		
MAGNETIC DISC AND DRUM UNITS (See also Flexible Disc Units)			
Disc Drives			
Fujitsu America	145		
Fixed Disc Drives			
Pertec Computer/PCC Peripherals	163		
Disc Controllers			
Xylogics	99		
Disc Systems			
Century Data	181		
Microcomputer Systems	204		
Pertec Computer/PCC Systems	82, 83		
Winchester Disc Systems			
Charles River Data Systems	169, 198		
Drum Memories			
Vermont Research	162c		
MAGNETIC TAPE UNITS			
Tape Drives			
Cipher Data Products	44, 45		
Digi-Data	173, 208		
Tape Transports			
Datum	59		
Cartridge Tape Drives			
Mohawk Data Sciences	171		
Cartridge Tape Systems			
Digital Equipment	108		
Cassette Transport Interfaces			
MFE	206		
ROM/RAM PROGRAMMERS AND SIMULATORS			
P/ROM Programmer Modules			
MDB Systems	208		
EPROM Programmers			
Texas Microsystems	200		
SEMICONDUCTOR MEMORIES			
RAMs			
NEC Microcomputers	36, 37		
Static RAMs			
Hitachi America	188		
Intel	6, 7, 186		
P/ROMs			
Intel	8, 9		
EPROMs			
Synertek	188		
Semiconductor Memory Systems			
Mostek/Memory Systems	206		
OTHER TYPES OF MEMORY/STORAGE EQUIPMENT			
Add-In Memories			
Intel	200		
INPUT/OUTPUT AND RELATED EQUIPMENT			
AUDIO RESPONSE EQUIPMENT			
Voice I/O Terminals			
Voicetek	208		
COMPUTER PERIPHERALS—GENERAL			
Microcomputer Peripherals			
Andromeda Systems	98		
DATA TERMINALS (See also Graphic Equipment)			
Printer Terminals			
Qume	81		
CRT Display Terminals			
Ann Arbor Terminals	218		
ADI/Applied Dynamics International	186		

	PAGE
Beehive International	161
Delta Data Systems	199
Hazeltine	141
Lear Siegler	90, 91
Ontel	149
Telery/Research	207
DISPLAY EQUIPMENT	
(See also Data Terminals and Graphics Equipment)	
CRT Display Monitors	
Audiotronics/Video Display	147
Sanyo	107
Color Display Subsystems	
Intelligent Systems	202
GRAPHICS EQUIPMENT	
Digitizers	
GTCO	164
Science Accessories	208
Plasma Displays	
Interstate Electronics	200
Graphics Display Systems	
Grinnell Systems	69
Color Graphics Display Equipment	
Ramtek	Cover IV
Graphics Display Terminals	
Lear Siegler/Data Products	210
Tektronix	35
Color Graphics Display Terminals	
Magnavox Display Systems	167
INTERFACE EQUIPMENT, CONTROLLERS	
Flexible Disc Interfaces	
Tarbell Electronics	204
Communications Interfaces	
Computer Interface Technology	206
Instrument-Microcomputer Interfaces	
Datel Systems	156
Bus Links	
Able Computer	206
Printer Interface Adapters	
Protoline	202
Typewriter-Printer Converters	
Applied Computer Systems	212
Disc Controllers	
Xylogics	99
Programmable Camera Controllers	
EG&G Reticon	206
PLOTTING EQUIPMENT	
Plotters	
Houston Instrument	Cover III
PRINTING EQUIPMENT	
Printers	
Anadex	151
Axiom	196
Centronics Data Computer	17
Florida Data	209
Tally	2
Printer Systems	
Interface Electronics/Capitol Circuits	208
Digital Printers	
Hycom	200
Printer Interface Adapters	
Protoline	202
Typewriter-Printer Converters	
Applied Computer Systems	212
Thermal Printheads	
Gulton Industries	204
PUNCHED TAPE EQUIPMENT	
Tape Punch/Readers	
Chalco Engineering	33
COMPUTERS AND COMPUTER SYSTEMS	
BUSINESS COMPUTERS	
Business Microcomputer Systems	
Heath Data Systems	162d
GRAPHICS PROCESSORS	
Graphics Processors	
Megatek	Cover II
MICROCOMPUTERS AND MICROPROCESSORS	
Microprocessors	
Advanced Micro Devices	25, 26, 27

	PAGE
Control Processor Chips	
National Semiconductor	160
Communications Processors	
Inco	162
I/O Processors	
Functional Automation	210
Microcomputers	
Monolithic Systems	74, 75
Quay	132
Synertek Systems	188
Industrial Microcomputers	
Process Computer Systems	93
Business Microcomputer Systems	
Heath Data Systems	162d
Microcomputer Development Systems	
GenRad/Futuredata Computer	52, 53
Development/Debug Systems	
Motorola Microsystems	160
Development/Control Systems	
Distributed Computer Systems	158
Development Lab Emulator Boards	
Tektronix	162
Development System Emulator Terminals	
Millennium Systems	162
Development Software Packages	
Exidy Data Systems	160
MINICOMPUTERS; SMALL- AND MEDIUM-SCALE COMPUTERS	
Minicomputers	
Ampex	162f
Perkin-Elmer	56, 57
Sperry-Univac	20, 21
Medium-Scale Computers	
Digital Equipment	14, 15
Scientific Computer Systems	
Data General	195
Militarized Computers	
ROLM	176
DATA COMMUNICATIONS EQUIPMENT	
COMMUNICATIONS INTERFACES	
Communications Interfaces	
Computer Interface Technology	206
Communications Converters	
KMW Systems	208
COMMUNICATIONS SYSTEMS	
Communications Processors	
Inco	162
Network Controllers	
Dynatech Data Systems	210
COMMUNICATIONS TERMINALS	
Communications Terminals	
Columbia Data Products/Peripheral Systems	92
MODEMS; DATA SETS	
Data Modems	
Penril	18
DATA ACQUISITION AND CONTROL EQUIPMENT	
A-D AND D-A CONVERTERS	
A-D/D-A Converter Systems	
Datel-Intersil	55
A-D Converter Modules	
Intech	198
D-A Converter ICs	
Analog Devices	196
ANGLE AND POSITION ENCODERS	
Trackball Optical Encoders	
Disc Instruments	202
DATA TRANSFER AND INTERFACE EQUIPMENT	
I/O Modules	
Opto 22	79
I/O Subsystems	
ADAC	4
Analog I/O Systems	
Analog Devices	77
Burr-Brown	175
I/O Processors	
Functional Automation	210

	PAGE
Instrument-Microcomputer Interfaces	
Datel Systems	156
MONITORING AND CONTROL EQUIPMENT	
Realtime Measurement/Control Systems	
Analog Devices	196
TEST AND MEASUREMENT EQUIPMENT; INSTRUMENTATION	
DATA GENERATORS	
Word Generator Options	
Tau-Tron	198
DIGITAL EQUIPMENT TESTERS	
Logic Testers	
Omnicom	196
Logic Analyzers	
Gould/Biomation	86, 87
Data Analyzers	
Tektronix	94, 95
Memory Exercisers	
Wilson Laboratories	204
CODEC Test Heads	
Santek	200
INSTRUMENTATION RECORDERS	
Data Logger Cartridge Recorders	
Columbia Data Products/ Peripherals System	202
OTHER TEST AND MEASUREMENT EQUIPMENT	
Instrumentation	
Tektronix	35
VIDEO DIGITIZERS	
Color Camera Systems	
Dunn Instruments	31
Programmable Camera Controllers	
EG&G Reticon	206
OTHER PRODUCTS; SERVICES	
EDP ACCESSORIES AND SUPPLIES	
Flexible Discs	
Maxell Data Products	205
EDUCATION	
Seminars	
Integrated Computer Systems	154, 155
EMPLOYMENT OPPORTUNITIES	
Employment Opportunities	
GTE Automatic Electric	218
Hughes Aircraft	191
Naval Surface Weapons Center	158
EQUIPMENT BUYING, SELLING, AND LEASING	
Equipment Rentals	
Rental Electronics	73
Distributors	
TransNet	204
MARKET REPORTS	
Market Reports	
Frost & Sullivan	204
PRODUCTION AND ASSEMBLY EQUIPMENT	
Wirewrapping Tools	
OK Machine & Tool	210
PUBLICATIONS	
Books	
Van Nostrand Reinhold	162g
SOFTWARE	
Software	
Technical Systems Consultants	38
BASIC Language	
International Business Machines/ General Systems	206
Disc Operating Systems	
Wintek	162h
Rigid Disc Software	
Micropolis	164
Development Software Packages	
Exsidy Data Systems	160
Commercial/Industrial Software	
Intel	166

ADVERTISERS' INDEX

ADAC	4	Intel Corp.	6-11
Advanced Electronic Design, Inc.	76	Intelligent Systems Corp.	202
Advanced Micro Devices	25-27	Intersil, Inc.	48, 49
AMP, Inc.	60, 61	Kennedy Co.	1
Ampex Memory Products Div.	162f	Lear Siegler, Inc.	90, 91
Anadex	151	Magnavox Display Systems	
Analog Devices	77	Div. of North American Philips	167
Andromeda Systems, Inc.	98	Maxell Corp. of America	205
Ann Arbor Terminals, Inc.	218	MDB Systems, Inc.	89
Applied Dynamics International.	186	Megatek Corp.	Cover II
Audiotronics Video Display Div.	147	MFE Corp.	28, 29
Aydin Controls	96	Micro Peripherals, Inc.	39
BASF Systems	179	Micropolis Corp.	104, 105
Beehive International	161	Micro-Switch	
Bell & Howell Display Devices.	211	a Div. of Honeywell	51
Belting Industries Co., Inc.	162d	Micro/Sys.	171
Brand Rex Company	165	Mohawk Data Sciences Corp.	19
Bulova Watch Co., Inc.	166	Monolithic Memories	40, 41
Burr-Brown Research Corp.	175	Monolithic Systems Corp.	74, 75
Burroughs OEM Div.	159	National Semiconductor Corp.	32a-32d*
Canon USA, Inc.	68	Naval Surface Weapons Center	158
Centronics Computer Data Corp.	17	NEC Information Systems, Inc.	43
Century Data		NEC Microcomputers, Inc.	36, 37
a Xerox Co.	181	Northwest Microcomputer Sysms	200
Chalco Engineering Corp.	33	OK Machine & Tool Corp.	54
Charles River Data Systems	169	Ontel Corp.	149
Cipher Data Products, Inc.	44, 45	Opto 22	79
Columbia Data Products, Inc.	92	Penril Corp.	18
Comark	170	Perkin-Elmer Corp.	
Computer Automation, Inc.	184	Computer Systems Div.	56, 57
Control Data Corp.		Memory Products Div.	203
Peripheral Products Group	162a	Pertec Computer Corp.	
Custom Systems	187	Peripherals Div.	103, 118, 163
Cybernetic Micro Systems, Inc.	58	Systems Div.	82, 83
Dataram Corp.	5, 63	Plessey Microsystems, Inc.	197
Data Systems Design, Inc.	13	Power One, Inc.	32
Datel-Intersil	55	Process Computer Systems, Inc.	93
Datum, Inc.	59	Qantex	
Delta Data Systems	199	Div. of North Atlantic Industries	162b
Digi-Data Corp.	173	Quay Corp.	132
Digital Equipment Corp.		Qume Corp.	81, 195
Microcomputer Group	14, 15, 108	Ramtek Corp.	Cover IV
OEM Group	162h	Rental Electronics, Inc.	73
Digital Pathways, Inc.	201	Research, Inc.	207
Dunn Instruments, Inc.	31	Robbins & Meyers, Inc.	
EECO	214	Electric Motors Div.	46
Estatech	186	Robinson Nugent, Inc.	22, 23
Ex-Cell-O Corp.		Rolm Corp.	176
Remex Div.	213	Sanyo Communications Div.	107
Florida Data Corp.	209	Shugart Associates.	70, 71
Frost & Sullivan	204	Spectra-Strip, Inc.	189
Fujitsu America, Inc.	145	Sperry-Univac Mini-Computer Operations	20, 21
General Electric		Tally Corp.	2
Terminet Div.	183	Tarbell Electronics	202
General Terminals	142, 143	T-Bar, Inc.	150
GenRad/Futuredata.	52, 53	Technical Systems Consultants, Inc.	38
Gould, Inc.		Tektronix, Inc.	35, 94, 95, 98a**, 98b**
Biomation Div.	86, 87	Teledyne Relays	88
Grinnell Systems, Inc.	69	Teleray	207
GTCO Corp.	218	Teltone Corp.	162e
GTE Automation Electric Laboratories	204	TEXAS INSTRUMENTS SEMICONDUCTORS	192, 193
Hazeltine Corp.	141	Topaz Electronics	101
Hewlett Packard Co.	157	TransNet Corp.	204
Houston Instruments		Triad-Utrad	97
Div. of Bausch & Lomb	Cover III	Van Nostrand Reinhold Co.	
Hughes Aircraft	191	a Div. of Litton Educational Publishing Co.	162g
Hycom, Inc.	174	Vectron Laboratories, Inc.	65, 66
HYTEK Microsystems, Inc.	198	Vermont Research Corp.	162c
Integrated Computer Systems, Inc.	154, 155	Western Digital Corp.	178
		Xylogics, Inc.	99

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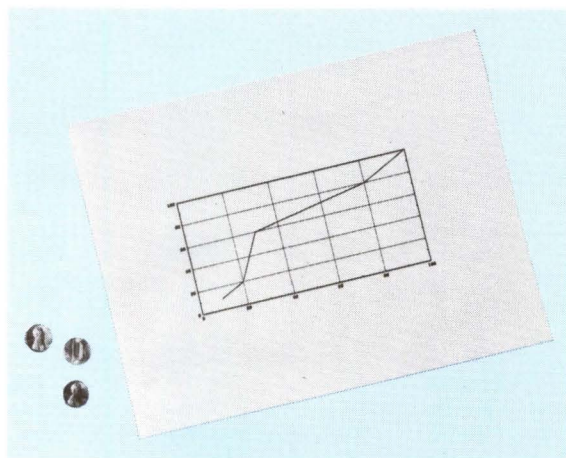
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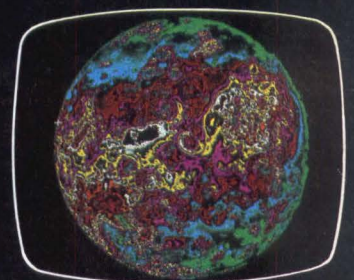
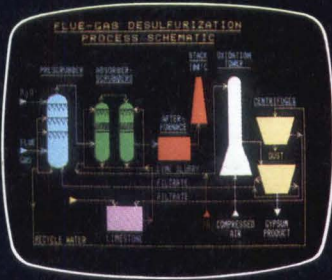
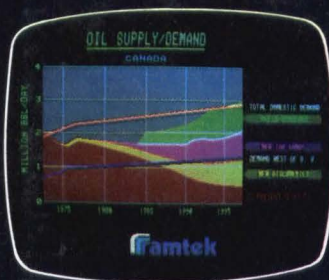
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